PLANAR SILICON TRANSISTORS AND DIODES

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ABSTRACT

This paper describes the design and fabrication of silicon transistors and diodes of planar geometry, in which the lateral extent of the diffused layers is controlled by oxide masking. The process also incorporates the silicon oxide layer as an integral part of the device protecting the junctions at their intersection with the surface of the device. Comparison with the mesa process shows that the planar process yields values of the transistor parameters which are particularly surface sensitive (such as reverse leakage current noise figure and low current beta), as well as a tighter distribution of the same parameters for different units. Preliminary life test data are included in the discussion.

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It is well known that with the introduction of diffusion techniques, a significant improvement was made in the way of controlling the penetration and the distribution of a doping impurity under the surface of a piece of semiconductor material. Other techniques were needed at the same time, however, namely ways of limiting the area over which a given diffusion has to take place. An obvious method is, of course, to limit this area by etching off the unwanted diffused material. This is the familiar mesa process. Another process is the oxide masking technique. It is based on the fact that the penetration of many of the standard dopants in silicon is prevented by the presence of a layer of silicon oxide on the surface.

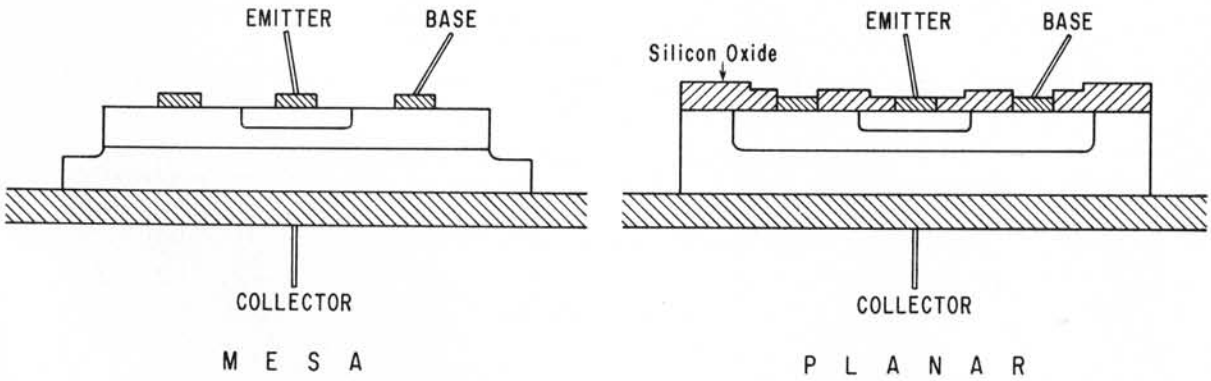

Fig. 1. Transistor Structures

Fig. 1 shows on the left a usual mesa transistor where the base collector junction area is limited by the mesa process and the emitter base junction area by the oxide masking process. For comparison, a planar structure is shown on the right. In this case, both junctions are limited by a masking process. The diagrams also show the transition from a mesa to a planar diode by simply omitting the emitter of the transistor.

The planar process permits the passivation of the surface by an oxide layer at an early stage of manufacture of the device. In fact, the silicon oxide coating is applied to the surface before the junction is driven in by diffusion. This results in a great improvement in the parameters which are particularly sensitive to surface conditions at the point of emergence of the junction from the bulk of the silicon. Such parameters are reverse leakage currents, breakdown voltages, noise figure, low current h_{FE}. The silicon oxide passivation also brings about a greatly improved reliability of the device.

Another advantage of planar structures is that they are the natural first step in any integrated approach where several elements, transistors or diodes, are built simultaneously on the same piece of semiconductor. It is obviously more convenient to deal with an integrated system having a planar surface than a collection of mesas and valleys.

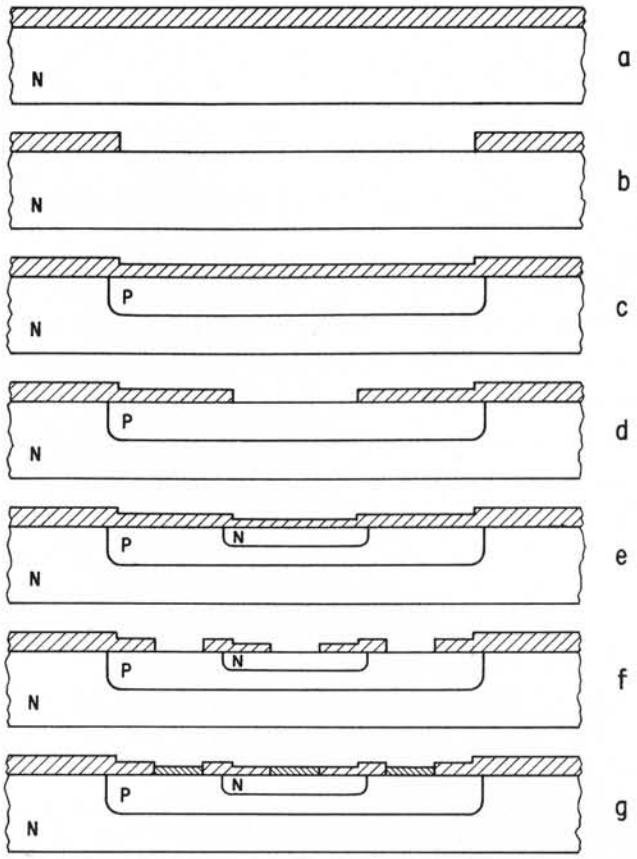

Fig. 2. Steps in Planar Transistor Fabrication

Let us now consider the various steps involved in the fabrication of a planar transistor. These steps are shown on Fig. 2 for the case of an NPN transistor. We start with a suitably etched or polished wafer and oxidize it to a thickness of about 1 μ (Fig. 2a). By standard photo-processing techniques, the oxide is selectively etched off on a series of circular dots (Fig. 2b).

The wafer is then exposed to a vapor of the base diffusant. In the case of NPN transistors, boron is a suitable base diffusant; in the case of PNP transistors, Sb, As or P can be used. The base impurity is then diffused to the required penetration (Fig. 2c). Oxygen carrier gas is used during this operation so that the previously exposed area of the wafer is reoxidized. It is important to point out that during the diffusion, the point of emergence of the junction has moved laterally under the original oxide mask by an amount equal to the junction depth. This means that this particular point of emergence was protected during the previous masking and etching operation and had no risk of being contaminated at that stage.

By means of another masking and etching process, a portion of the regrown oxide on the base area is removed (Fig. 2d). The wafer is then exposed to the emitter diffusant, phosphorus or boron, and the emitter area reoxidized during this diffusion (Fig. 2e). Except for the doping level, this step is similar to the base diffusion step and is also, of course, identical to the one used in making the emitter of a double-diffused, oxide-masked mesa transistor. After emitter diffusion, the wafer is again selectively etched to provide for alloyed contacts (Fig. 2f).

Metal contacts are then deposited on the etched areas and alloyed in (Fig. 2g).

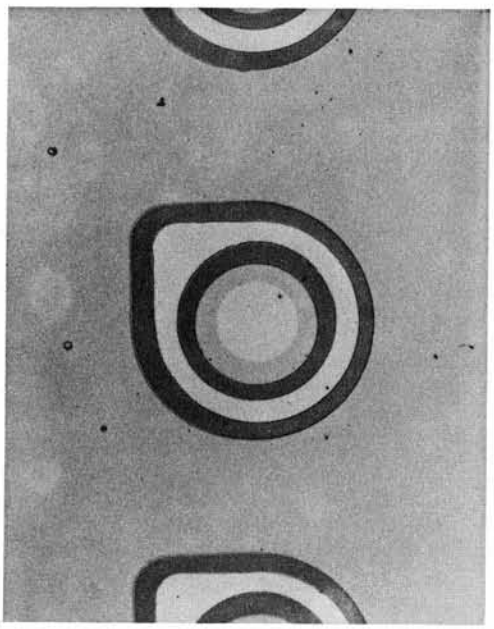

Fig. 3. 2N1613 Transistor

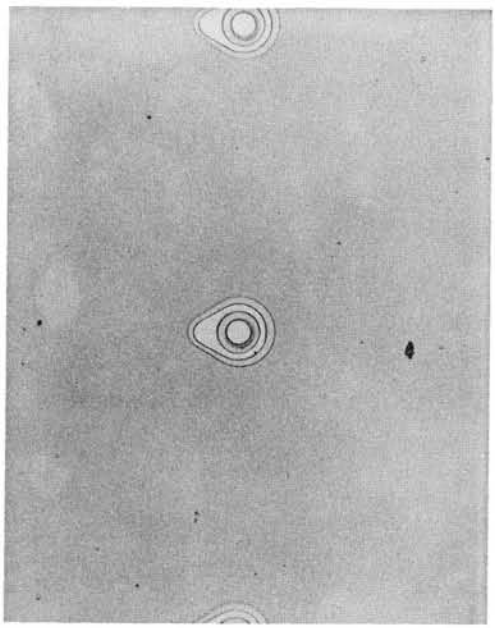

Fig. 4. Planar 2N706

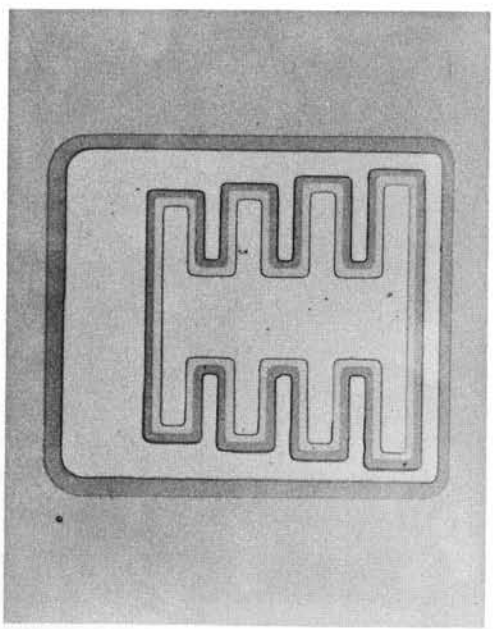

Fig. 5. Power Transistor

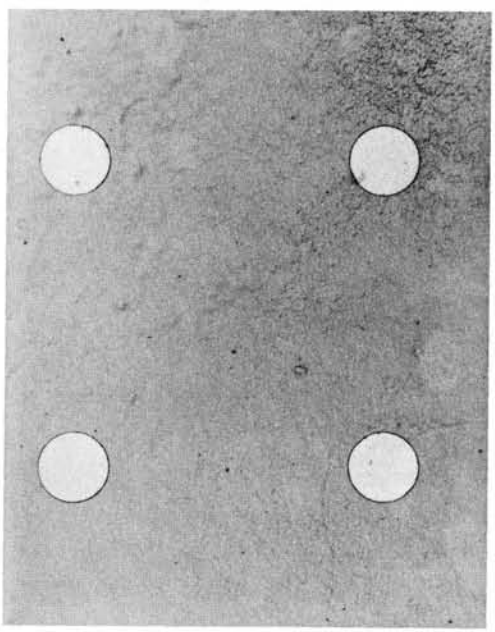

Fig. 6. Diodes

Figs. 3, 4 and 5, respectively, show a top side view of 3 different transistors, the 2N1613 type, a planar version of the 2N706 type, and a power transistor. The different shadings in the oxide coating correspond to different thicknesses. The junctions are embedded under the oxide everywhere. Except for the lateral motion previously mentioned, the junctions are approximately located under the lines of discontinuity in oxide thickness.

The wafer is then diced, mounted on suitable header for collector contact, and leads are bonded to the metal emitter and base contacts. It can be noted here that the planar structure readily provides for the possibility of a collector contact at the top side of a transistor, allowing, therefore, for electrical isolation at the back of the transistor. It would only be necessary to provide for this purpose an extra metal ring around the base collector junction.

As was mentioned, planar diodes can be made by a process similar to the one used in the diffusion of the base material of a transistor. Fig. 6 shows a wafer with such diodes after the metallizing step.

Let us now consider some electrical characteristics of planar devices, with particular emphasis on the 2N1613 planar transistor. The dimensions and the design of this transistor were chosen to match closely the 2N697 mesa transistor. We will only be concerned here with the parameters which are significantly different for the two structures. The most important parameter is the base collector junction reverse current I_{CBO}, with the emitter open.

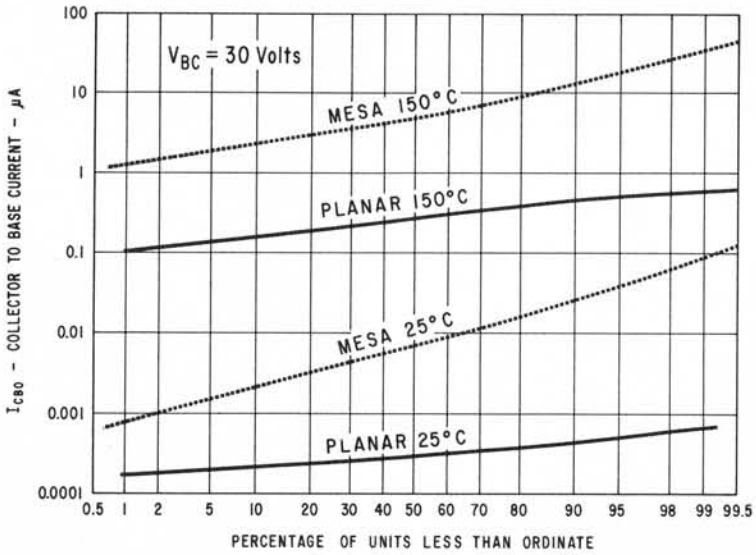

Fig. 7. I_{CBO} Distributions for Planar and Mesa Transistors

Fig. 7 shows I_{CBO} distributions for two groups of 50 units each of planar and mesa transistors, at the temperatures of 25°C and 150°C. Base collector voltage in every case is 30 V. It will be observed that at either temperature, the median planar I_{CBO} values (at the 50 percentile level) are about 50 times lower than the mesa values. Also, the distribution is much tighter in the planar case. If we use the theoretical expression for the reverse current generated in the space charge layer, we determine a lifetime value in the collector material of about 10 μsec, which is consistent with recovery measurements made on the transistor. This agreement indicates that the usual surface leakage has essentially been eliminated, and that the observed reverse current is of the order predicted by the bulk properties of the junction. Further evidence on this point is given by high speed planar diodes of type FD100, where higher reverse current is quantitatively accounted for by the considerably lower lifetime in the material.

The study of reverse current with voltage indicates a law of variation as between $V^{1/2}$ and $V^{1/3}$, which again can be accounted for by the bulk properties of the junction.

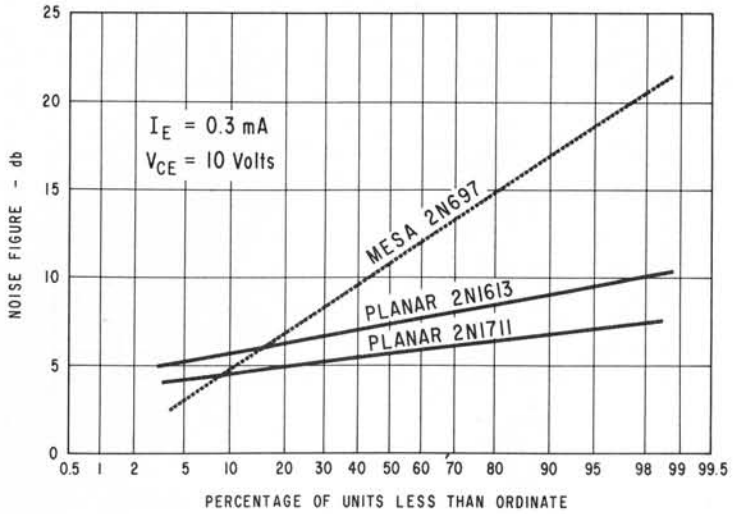

Fig. 8. Noise Figure Distributions

A consequence of the reduced surface leakage component of collector current is the observed smaller noise figure on the planar than on the mesa structure. Again, the planar distribution is tighter (Fig. 8). A typical noise figure at 1 kc., 1 cycle band width, is 2 to 3 db.

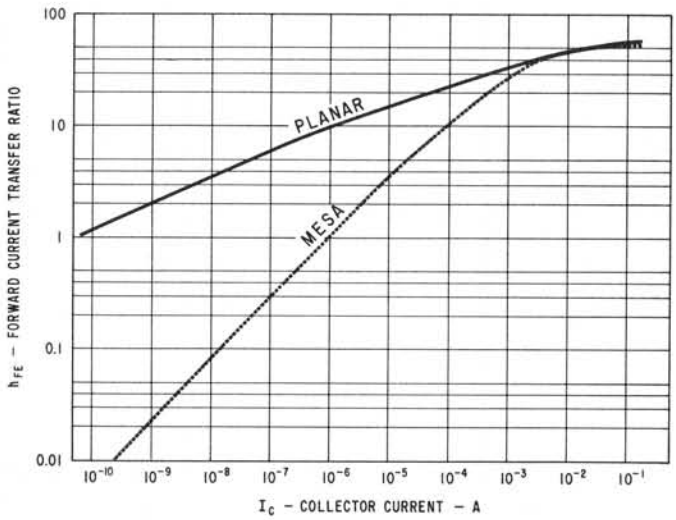

Fig. 9. Variation of h_{FE} with Collector Current

Let us now consider the effect of the oxide protection on the emitter base diode. Here again, typical reverse currents at, say, 5 Volts, are of the order of a fraction of 1 mμA. This low value has an interesting effect on the variation of h_{FE} with collector current. The decrease of h_{FE} at low currents is due to a bulk factor, recombination in the emitter-base space charge layer, and to a surface factor, straight leakage over the junction. The elimination of surface leakage in the planar case results in a smaller h_{FE} decrease at low current and in an increased range of usefulness of the transistor. Fig. 9 shows the variation of h_{FE} over 10 decades of current for two typical planar and mesa transistors of same maximum h_{FE}. At the h_{FE} = 10 level, it is seen that the range of usefulness of the transistor has been increased from 3 to 5 decades of current by using the planar process.

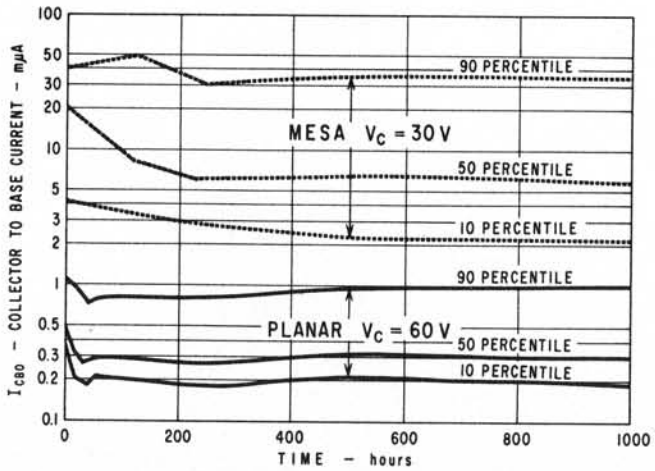

Fig. 10. Life Test Data at 300°C Storage

We will now discuss the reliability of the new structure. A standard life test consists of storage at elevated temperature. Fig. 10 shows I_{CBO} current measured at room temperature and at a voltage of 30 Volts for the mesa group and 60 Volts for the planar group. Here again, in spite of the higher voltage applied to the planar group, it is worth noticing the much lower and tighter distribution for the planar group.

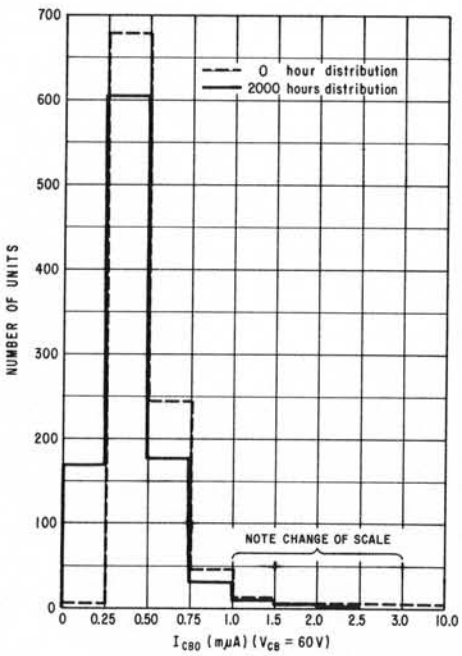

Fig. 11. Life Test Data at 200°C Storage

Fig. 11 shows some results from a life test experiment made on a thousand 2N1613 transistors. The distributions of I_{CBO} at 60 Volts are shown at the beginning of the test and after 2,000 hours of storage at 200°C. It is worth pointing out that the peak of the distribution occurs at a current value more than 20 times lower than the maximum current (10 mμA) allowed by the specification on this device.

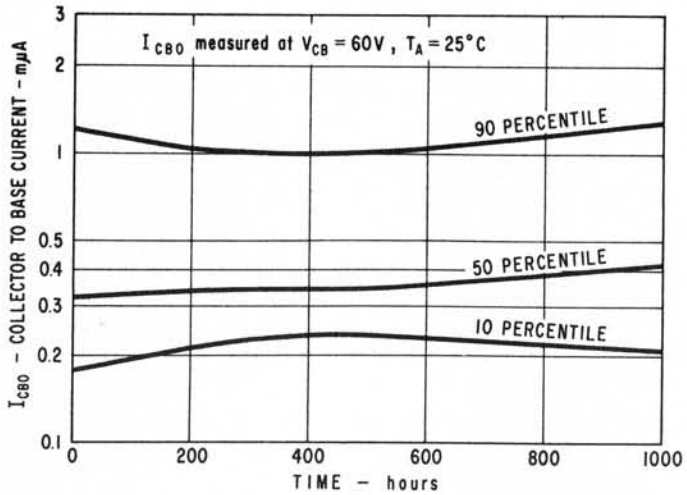

Fig. 12. Operating Life Test Data at 200°C and 80 Volts

Fig. 12 shows an operating test at 200°C with a reverse voltage of 80 Volts applied to the base collector junction of 2N1613 transistors. Here again, no long range drift is observed. This test was undertaken in order to test possible drift effects of ionic impurities at the silicon-silicon-oxide interface under an applied field at moderately high temperature. The results show that no such effect was present here.

Tests have just been started recently on the reliability of the planar structure on unencapsulated units. In a preliminary experiment, the can of a 2N1613 transistor was opened, the transistor was placed in an oven at 200°C, a voltage of 80 V was applied to the base collector junction, a flow of nitrogen bubbling through boiling water passed over the transistor. The leakage current was monitored continuously under these conditions and did not show any significant change during the two days over which the test took place.

Other preliminary results indicate so far that most reliability problems on unencapsulated units are traced to the various coatings or plastics, themselves, rather than the planar chips that they are supposed to protect.

In summary, the planar design offers considerable improvement and stabilization of the parameters most likely to suffer from surface contamination. We believe that it will also prove attractive in the design of integrated semiconductor circuits and in low cost encapsulation techniques.

Acknowledgements:

The author wishes to thank L. Reis and Dr. C. T. Sah for supplying the data shown in Figs. 7 to 12.