Notes from Interview with Wendell Sander

Interviewer: Jeff Katz July 16, 2006

SANDER'S STATED BACKGROUND INFORMATION

- Started at FSC shortly after graduating college in 1956.
- Worked on both chip design and system design at various times.
    - Developed test chip for 256 b (16 x 16) SRAM (part FBM C75A) in 1967-68, which later was the basis of the 4100 SRAM designed by H.T. Chua. Did this work under Bob Seeds (now deceased, who worked for Will Steffi, who reported to Gordon Moore). Doug Peltzer and Dick Abraham (spouse of well known patent attorney for Brown & Bain, Lois Abraham) also worked in and managed this bipolar SRAM group.
    - Performed system design for Illiac IV memory, and later 1 MB semiconductor main memory for IBM mainframe, both using 4100 chips. Did this work with Frank Greene (now a VC, and possibly a trustee for Santa Clara University) under Rex Rice (now deceased).
    - Was part of the team that developed 4Kb and 16 Kb bipolar DRAMs. Impressive speed advantage and competitive cost vs MOS DRAMS by many competitors, but commercial failure due to incompatible pinout with all the MOS DRAMs. Did this work under guidance from Dave Hodges, then a professor at UC Berkeley who had previously been at Bell Labs, where he had worked on bipolar DRAM inventions.
- Developed first RTL Gate Array, under Jim Downey (later a VP at AMD) who worked for Rice. Believed to be the first Gate Array, this was never a commercial success due to production difficulties with then-novel two-layer metal interconnects. Also developed CTL Gate Array. Worked with Hugh Mays and Jim Cofert, an early pioneer in CAD tools for Gate Arrays.
- Later worked at Apple, (2 digit employee number). Has significant knowledge and artifacts from Apple III, especially peripherals. Currently works in Apple's iPOD hardware group.

DISCUSSION OF EARLY SRAM DEVELOPMENT

- The 256 b test chip was used in same basic form by HT Chua, who developed a manufacturable version, the 4100. It had partial, not full, address decoder on-chip; requiring off-chip decodes for some of the address bits. This produced a chip that was virtually all cell-array, with very little peripheral overhead area. The resistors were made in otherwise unused areas using EPI, making a fairly small flip-flop cell.
- While the 4100 was important for being the first semiconductor memory chip with sufficient capacity to be used for computer main memory, not just register files, it was soon eclipsed commercially by 1Kb and 4 Kb versions that became and remained standards for a long time. FSC was for a while the acknowledged leader in bipolar SRAMs.
- The 256b development was not revolutionary; it was an evolutionary step beyond the increasingly common 64 b (16 x 4) register file memories. At the time and for at least a year after its introduction, 4100 had no meaningful competition.

- Even though the 4100-based memory systems demonstrated reliable semiconductor main memory for computers, there was a price to pay. With their small capacity per chip they consumed considerable power in a system. The 1 MB memory system for IBM included four 600A 5V power supplies (12 Kilowatts!).

ADDITIONAL MEMORY DEVELOPMENTS (not done by Sander)

- Prior work on the 16 x 4 memories at FSC was mostly done by Tom Longo, who had arrived from Transitron where he worked on early SRAM circuits.
- FSC was active also in MOS DRAMs (though later than others, while they concentrated on bipolar), magnetic film memories, even core memories and flexible media (floppy disc) memories. The leader of the magnetic memory developments was Art Pohm (now believed to Professor Emeritus at Iowa State Univ.).
- As a vertically integrated company FSC made its own ferrite cores and magnetic disc coatings. There was a black-art to this, in that the correct iron oxide material had to be found, tested and selected and mixed, in order to achieve the desired properties. The sources for iron oxide were paint manufacturers, who used the material to make red paint. So each core maker needed a good “mud mixer” the person who could find barrels of the appropriate stuff, comparison-test supplies from various paint makers, then mix the ferrite material properly for producing core elements. FSC was fortunate to have a good mud mixer (name un-remembered by Sander).

ADDITIONAL USEFUL CONTACT FOR SIG

FSC had an in-house micro-photographer and an archive of chip and system development photos. The photographer was for many years Steve Allen. Sometime after the acquisition of FSC by NSC, in an effort to save expenses the in-house photography department was disbanded and external contractors were hired for that purpose. The main external contractor was Steve Allen, who was given the entire archive of photos and negatives. He still maintains the archive, and may be a valuable source for the SIG, for not only memory chips but SSI/MSI logic, Gate Arrays, Processors and LSI chips.

ITEMS LOANED FOR SCANNING INTO CHM SEMICONDUCTOR ARCHIVES

ITEM	DESCRIPTION
Conference Paper	Semiconductor memory circuits and technology. by Wendell Sander Presented at Fall Joint Computer Conference, 1968.
	Includes circuit and architecture description of the pre-4100 256 b test chip, including detailed description of the on-chip partial address decoder, and a serious discussion of how the bipolar SRAM cell is much less complex than an equivalent CMOS cell of the time.
Article Reprint	Address Selection by Combinatorial Decoding of Semiconductor Memory Arrays by F.S. Greene and W.B. Sander published in IEEE Journal of Solid State Circuits, Oct, 1969.
	Describes the off-chip decoding required in the memory system to use 4100 chips. Though this was for the ILLIAC IV memory system, the computer is not named in the article.
Article Reprint	Design Considerations Leading to the ILLIAC IV LSI Process Element Memories. by R. Rice, W.B. Sander and F.S. Greene published in IEEE Journal of Solid State Circuits, Oct, 1970.
	Describes the ILLIAC IV Process Element Memory (PEM) boards. Including circuits; chip, board and system photos; test pattern development; and chip yield discussion. The test development was the first known dedicated semiconductor memory test, claimed by Sander to have been the model for much future memory testing. The 256 bit 4100 chips are described as LSI.
US Patent 3,654,610	Use of Faulty Storage Circuits by Position Decoding Inventors: W.B. Sander, F.S. Greene Applied Sept, 1970, awarded Apr, 1972
	Describes memory system with redundant devices, which can tolerate defective bits by mapping them to spare devices. Technique widely used by many competitors later.
Conference Paper	Design considerations for a MOS Complex Array

	By L. Vadasz and W.B. Sander No conference ID or date available, est. ~1967 (Vadasz was later one of the early and long-time Intel executives.)
	Describes a Gate Array of MOS circuits, configurable into logic functions of 80-160 gates using two-layer metal interconnect. Demonstrates equivalent performance to bipolar arrays. Requires further investigation by SIG's logic sub-group to determine whether and where this may fit on the logic seminal events timeline.
Original Photographs	Die Photos: FBMC75A 256 b test chip, precursor to 4100 MR40002 4Kb(??) SRAM Three RTL Gate Arrays CTL Gate Array Board Photo of 43069-A memory system (ILLIAC IV ?) Two small photos of board layouts made from blown-up chip layouts, used to check and debug the on-chip interconnect circuits.