

A STEPPING TRANSISTOR ELEMENT

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Summary - A more complete realization of the capabilities of the stepping transistor in logical circuit design has been obtained by the use of a new form of the stepping transistor. This result has been achieved by showing that the principles of operation of the stepping transistor can also be applied to a four-terminal device. The method of fabrication of these devices will be described and their performance will be discussed. The uses of some typical configurations of interconnected devices will be given.

INTRODUCTION

The stepping transistor originally described by Ross, Loar, and D'Asaro¹ is analogous to the gas stepping tube². Both of these stepping devices utilize a bistable V-I characteristic which is obtained between each one of their multiple electrodes and a single common electrode. The gas tube uses the bistable characteristic of a gas discharge, while the stepping transistor in the form described in¹ uses a PNP transistor as the bistable element. A means of transfer between electrodes is provided in the gas stepping tube by the diffusion of ions from the discharge region to an adjacent electrode. A preferential direction of transfer is built into the structure by the use of a nonsymmetrical geometry. In the stepping transistor, transfer is provided by emission of minority carriers from a PN junction common to all the PNP elements. As in the gas tube, a nonsymmetrical geometry provides a preferential direction of transfer.

In this paper it will be shown that the close physical proximity which is necessary in the gas stepping tube is not basically required in the stepping transistor. Thus, single four-terminal stages can be separately encapsulated and interconnected externally. In the following, a general analysis of such elements will be given, the procedure for fabrication will be described, and their physical performance will be discussed.

GENERAL ANALYSIS

Typical V-I characteristics for a PNP transistor³ are shown in Fig. 1. Base current I_b causes a decrease in the peak voltage of the V-I characteristic. If the base current is made sufficiently large, the peak disappears entirely. Thus, with a given load resistance and battery voltage, the base current can switch the device into a low impedance state. Once the low impedance state is obtained, the base current loses control and the low impedance state will remain, even with $I_b = 0$.

These effects can as well be discussed in terms of the potential V_b applied to the base. A sufficiently large base potential will cause the device to switch into the low impedance state.

With the PNP transistor in the low impedance state all the junctions are forward biased. The bias across one of the emitters can then be applied to a second PNP transistor. Such a connection will somewhat increase I_{T0} , the lowest current at which either of the devices can remain in the low impedance state. With sufficient current through the first device, the second device will show a V-I characteristic without a peak.

Suppose that a PNP transistor such as shown in Fig. 2 has an emitter near one end of the device and connections at both ends of the N-type base region. If the device is in the low impedance state, the junctions are all forward biased. The electron current from the N-type emitter is collected at J_2 and flows laterally in the N-type base. This electron current causes an IR drop which makes the bias across J_3 a maximum just under the N-type emitter. As a result, the voltage V_d is larger than V_c .

By interconnecting three units as shown in Fig. 3, one can use the higher voltage V_d to remove the peak in the V-I characteristic of the right hand unit while the peak in the left hand unit is not removed by the effect of the smaller

voltage V_c . If equal potentials V_1 and V_3 are applied to the right and left hand unit, only the right hand unit will attain a low impedance state. The right hand unit will then remain in the low impedance state even when the voltage V_2 becomes equal to zero. Thus, the low impedance state is transferred one stage to the right. A detailed analysis shows that variations in the electrical properties of the different stages can be tolerated without impairment of the operation of the circuit.

FABRICATION

The techniques of diffusion and oxide masking were used to control the dimensions of the N and P-type regions. A sequence of such operations makes it possible to produce many devices in one wafer as illustrated in Fig. 4.

After gold-silver alloy contacts are evaporated onto the N-type diffused emitters, the wafer appears as shown in Fig. 5. The wafer is then etched to define the boundaries of each device and sawed into the shape shown in Fig. 6. Contact is made to the large P-type emitter by alloying with gold to a Kovar header. Contact to the N-type regions is made with thermocompression bonded gold wires. The device then appears as shown in Fig. 7. The second N-type emitter shown there is not used in the circuit, but is only fabricated to preserve symmetry in the device.

PERFORMANCE MEASUREMENTS

The V-I characteristic of a typical device in a sequence of interconnected devices is found in Fig. 9 in the curve labelled $I = 0$. The turn-on current is 1.7 ma and the breakdown voltage is 65 volts. Measurement of an isolated single unit shows a turn-on current of 0.8 ma. The larger value of the turn-on current with the devices interconnected is due to the previously mentioned reduction of α which results from emission beneath an adjacent stage. This increase in turn-on current does not impair the operation of the device.

The voltage and current outputs from the base connections of a typical device are shown in Fig. 8 as a function of the current through the N-type emitter of the device. The current through the base connection close to the N-type emitter is seen to be at least 10 times the current through the base connection distant from the emitter. By a proper

choice of turn-on currents, this difference in base current is used to ensure that the adjacent device in the forward direction will be switched into the low impedance state while the adjacent device in the reverse direction will remain in the high impedance state. The current asymmetry is large enough so that two devices can be driven by one output, thus allowing more complex structures.

The influence of these base currents on the V-I characteristics of devices in the forward and reverse directions respectively is shown in Fig. 9. The V-I characteristic of any one of the devices in an interconnected sequence is shown in the curve labelled $I = 0$. When a device just to the right of the one under examination is operated at a current of 3 ma (just above I_{to}), the V-I characteristic of the observed device is altered into the form shown in the curve labelled " $I = 3$ ma, reverse direction". The peak is still present. Even with a current of 30 ma through the device to the right, the peak still remains and has the form shown in the curve labelled " $I = 30$ ma, reverse direction". On the other hand, when a device just to the left of the one under examination is operated at a current greater than I_{to} , the V-I characteristic of the observed device becomes essentially just the forward characteristic of a diode, shown in the curve labelled " $I > I_{to}$, forward direction". These results mean that a device to the right of the one which is in the low impedance state is switched into the low impedance state, while a device to the left can remain in the high impedance state.

These devices have been operated in a circuit shown schematically in Fig. 10 in which the low impedance state progresses one device to the right each time the switch S is thrown. A circuit which is used to count pulses is shown in Fig. 11. Each time the switch S is closed and opened, the low impedance state progresses by two stages to the right. This circuit has also been used as a decoding circuit by supplying two independent pulse generators connected to different stages.

INTEGRATED DEVICES

As discussed above, stepping transistor elements can be interconnected to form an extended array without any necessity for additional circuit elements.

Since the connections are always from N to N-type or P to P-type, a solid layer of semiconductor can be used. Therefore, these devices are particularly suitable for fabrication as an interconnected array in one piece of silicon. The previously described four-stage ring counter¹ is an example of such a structure, a top view of which is shown in Fig. 12. The fabrication steps resulted in the formation of silicon dioxide layers of differing thicknesses on the various diffused regions. Thus, these regions are clearly visible in the photograph.

CONCLUSIONS

The transfer mechanism between stepping transistor elements is provided by the effect of a transfer of potential. Thus, close physical proximity is not required. The stepping transistor element may be used as a basic stage in

the construction of certain logic circuits, such as a counting circuit and a decoding circuit. Versatile decoders can be made by using one element to drive two others. Any of these arrangements can be fabricated on a single piece of silicon, thus forming a compact, integrated device.

REFERENCES

1. AIEE-IRE Semiconductor Device Research Conference, Purdue University, (1956).
2. M. A. Townsend, "Construction of Cold-Cathode Counting Tubes", Elec. Eng. 69, p. 810, (September 1950).
3. I. M. Mackintosh, "The Electrical Characteristics of Silicon PNP Triodes", Proc. IRE, 46, pp. 1229-1235, (June 1958).

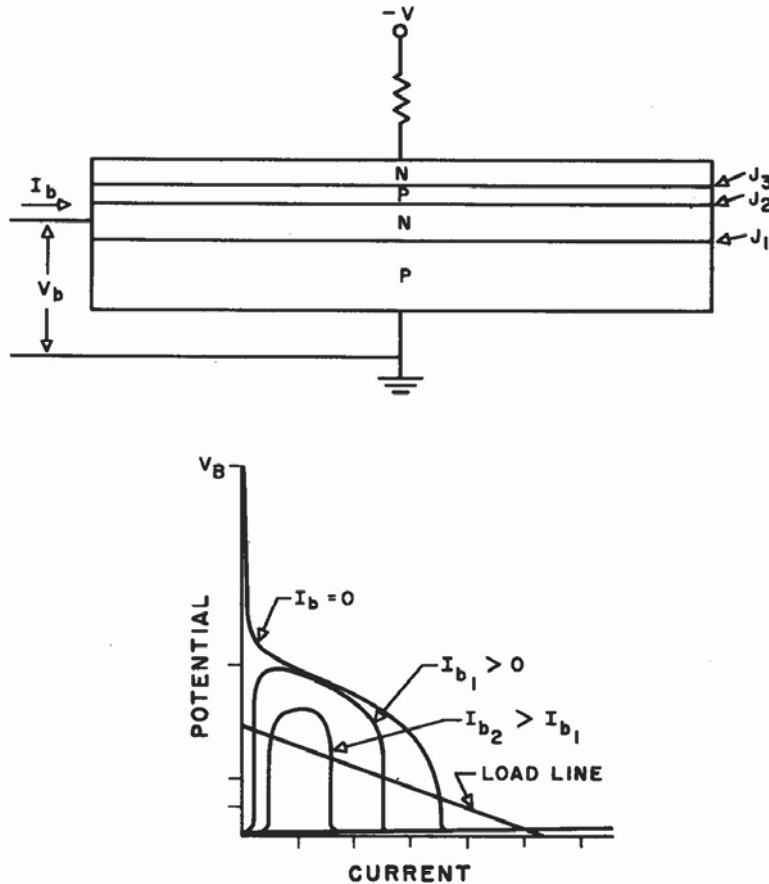


Fig. 1. Diagram of a PNP transistor triode and its V-I characteristics measured from the N type emitter to ground.

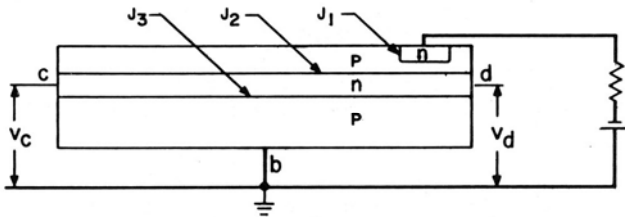


Fig. 2. A PNP transistor with the emitter near one end of the device. Connections are made to both ends of the N type base region. With the transistor in the low impedance state, voltage V_d is larger than V_c .

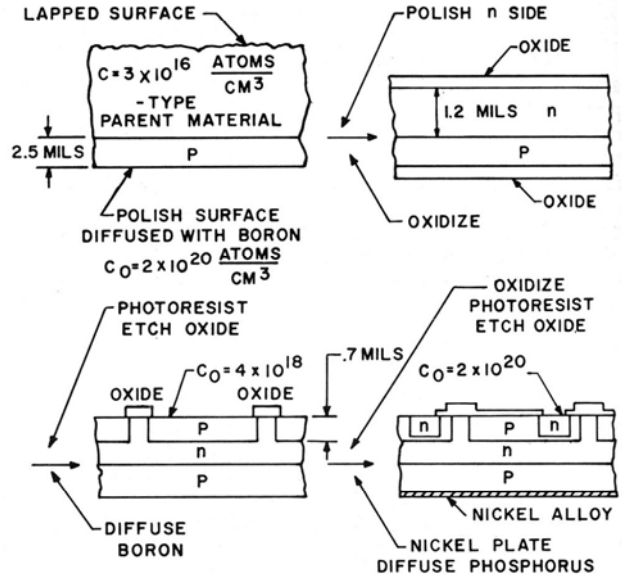


Fig. 4. The sequence of operations used to fabricate the stepping transistor elements.

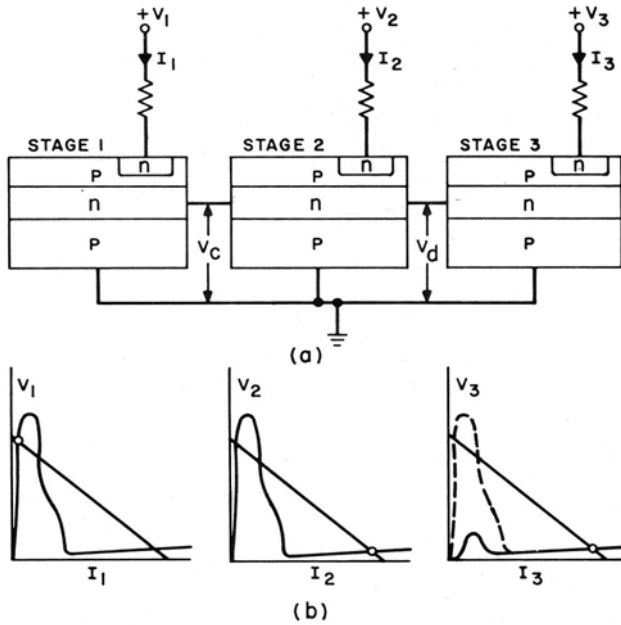


Fig. 3. Three stepping transistor elements connected together. When the center device is in the low impedance state, the voltage V_d is large enough to remove the peak in the V - I characteristic of the right hand device, but V_c is not large enough to affect the left hand device.

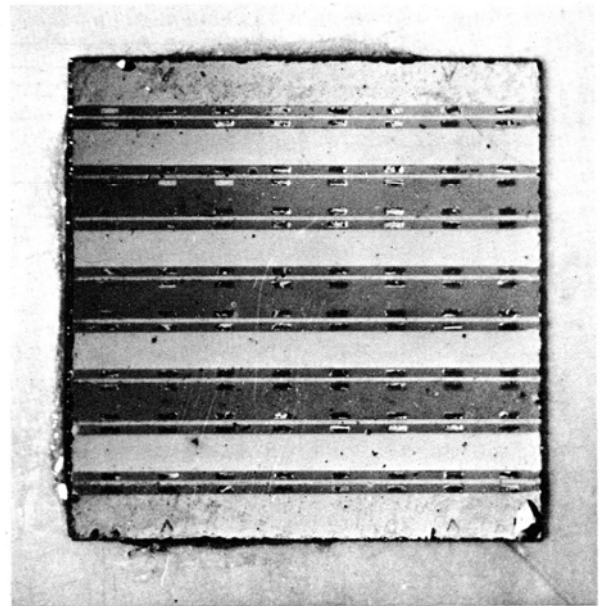


Fig. 5. A 1/4 inch square wafer of silicon which has been treated as in Fig. 4, and which also has gold-silver alloy contacts evaporated onto the N type regions. The light and dark stripes correspond to colored regions produced by light interference in the layers of silicon dioxide on the surface.

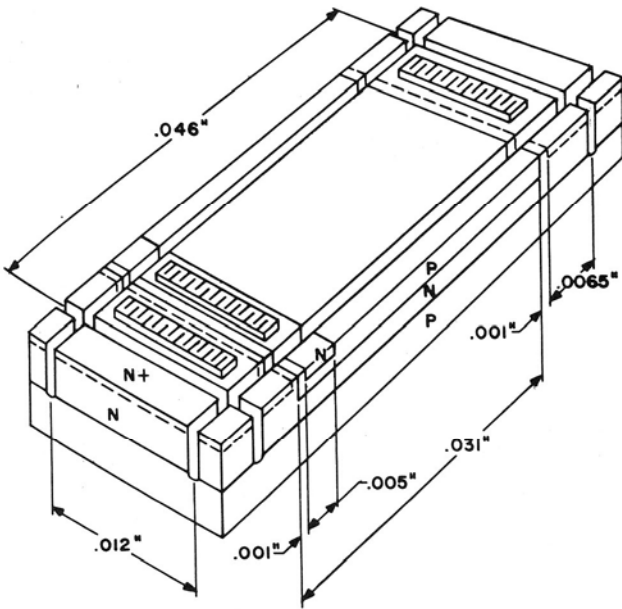


Fig. 6. Diagram of a single stepping transistor element showing junctions, etched regions, and contacts.

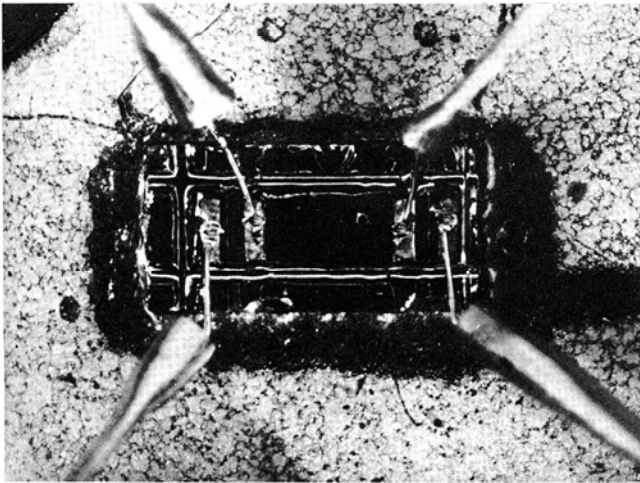


Fig. 7. Photograph of a stepping transistor element which is bonded to a Kovar header and contacted with thermocompression bonded gold wires.

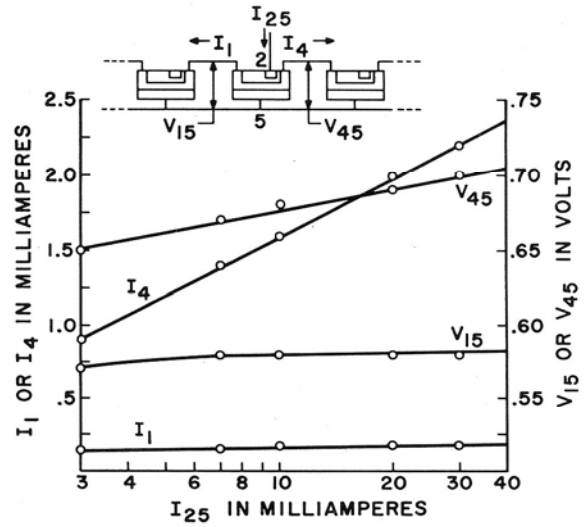


Fig. 8. Voltage and current outputs from the base connections of one stepping transistor element in a chain vs. current through its N type emitter.

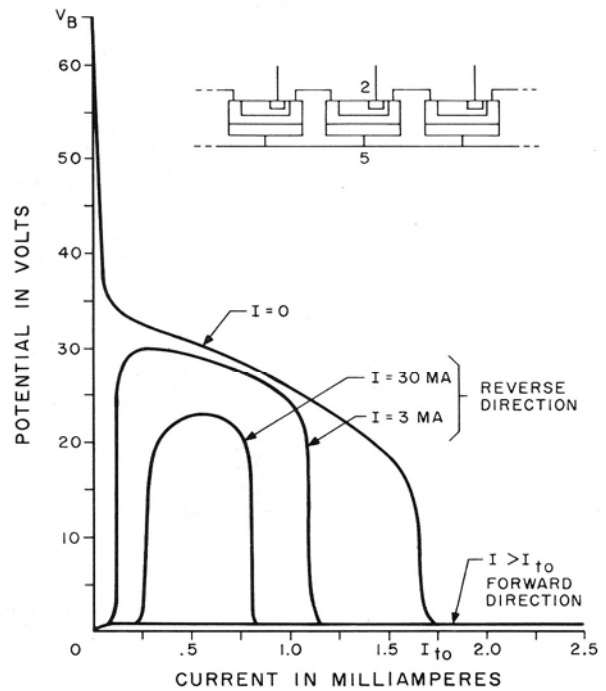


Fig. 9. V-I characteristics of one stepping transistor element in a chain. A current as large as 30 ma in the device to the right does not remove the peak, while a current just greater than I_{to} in the device to the left removes the peak completely.

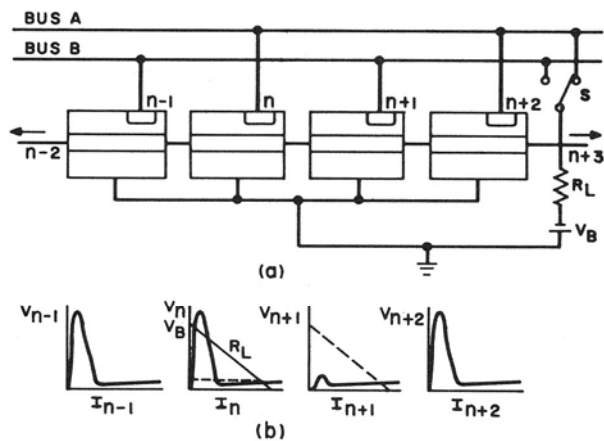


Fig. 10. A circuit in which the low impedance state moves one stage to the right each time the switch S is thrown. The V-I characteristics are for the case when stage n is in the low impedance state.

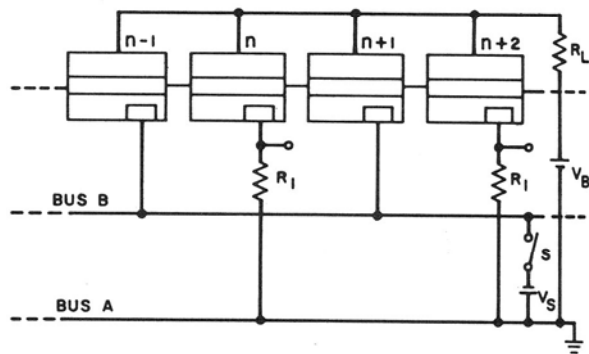


Fig. 11. A circuit used to count pulses. Each time the switch S is closed and opened, the low impedance state moves two stages to the right.

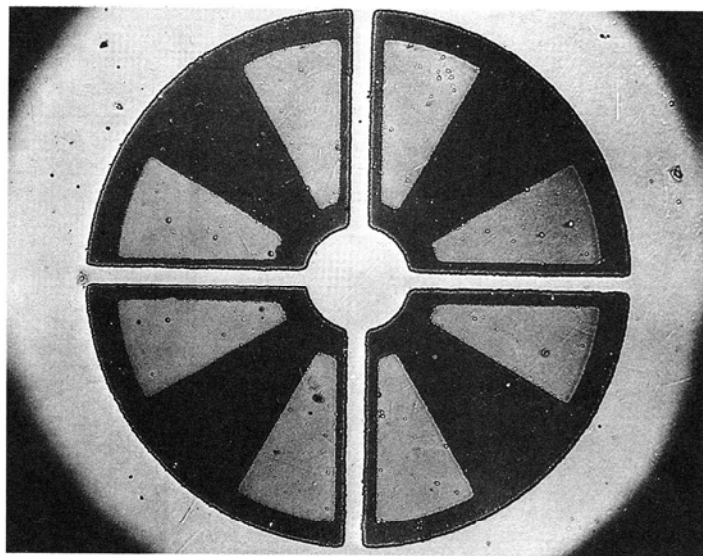


Fig. 12. Top view of a 4 stage ring counter fabricated in one piece of silicon. The diameter of this circular structure is 40 mils. The light and dark regions correspond to colored regions which result from light interference in silicon dioxide layers on the surface.