UNITED STATES DISTRICT COURT
DISTRICT OF MINNESOTA
FOURTH DIVISION

HONEYWELL INC., Plaintiff v. SPERRY RAND CORPORATION and ILLINOIS SCIENTIFIC DEVELOPMENTS, INC., Defendants	Consolidated Civil Action No. 4 - 67 Civ. 138

EXHIBITS OF AFFIDAVIT OF

ARTHUR W. BURKS

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EXHIBIT A

Contributions of Arthur W. Burks, Thomas Kite Sharpless and Robert F. Shaw to the Design and Construction of the ENIAC (Electronic Numerical Integrator and Computer)

REPORTS AND NOTEBOOKS

(R1) We issued three reports describing the progress of our work on the ENIAC (Project PX). Each had the heading "The ENIAC (Electronic Numerical Integrator and Computer)" and the notation "Submitted in accordance with Contract #W-670-ORD-4926." I will refer to them as the "First ENIAC Progress Report," etc. The periods covered are as follows:

First ENIAC Progress Report - To December 31, 1943.

The Preface was written in mid-February, 1944.

Second ENIAC Progress Report - January 1 to June 30, 1944.

This report was written about July 31, 1944.

Third ENIAC Progress Report - July 1 to December 31, 1944.

There is reference to experience gained after December 31, 1944.

(R2) I used three notebooks as engineering workbooks and as record books for conferences of engineers and others on the design of the ENIAC (Project PX) and later on the EDVAC (Project PY). I will refer to these as follows:

First Engineering Notebook Z16

Issued on June 17, 1943. The latest dated entry is April 27, 1944.

Second Engineering Notebook Z17

The first dated entry is May 1, 1944 and the last is December 17, 1945.

Third Engineering Notebook Z12

This is mostly about the EDVAC (Project PY), though on p. 11 there are some ENIAC assignments made on January 18, 1946.

SYSTEM DESIGN

(S1) The ENIAC was composed of nine different kinds of units: accumulator (of which there were 20), function table unit (of which there were 3), high-speed multiplier, divider and square-rooter, master programmer, cycling unit, initiating unit, constant transmitter (the input unit) and printer (the output unit). All these units had to function as one coordinated, synchronous system. They were interconnected in a number of ways. Trays and cables carried the frame of cycling unit pulses around the back of the machine. Direct current voltages were provided by a common power supply, and alternating current went to the filament transformers of the units. Semi-permanent connections were made between some of the units by means of cables. The multiplier selector of the high-speed multiplier received the digital contents of the multiplier accumulator in this way. To program the ENIAC, temporary interconnections were made at the front of the machine by means of cables and trays. These interconnections were of two kinds, digital and program.

(S2) While the design, development, construction, and test of each unit proceeded separately, all of these designs had to be coordinated at both the logical and the electronic levels. Logical design included such matters as the decimal representation of digits, processing all digits of a number in parallel, and the type of complement system used. Electronic design included the voltage level and swing of a signal, the exact timing of the signal, the power involved, and similar engineering matters.

(S3) The ENIAC units were constructed from gating and counting circuits, arranged in logical patterns that would permit a programmed sequence of arithmetic and conditional operations. By the end of the summer of 1943 we had individual gating and counting circuits which operated reliably and fast. The big problem was to design the tremendously large ENIAC system so it would be reliable and fast. Toward this end, general rules for operating and designing the ENIAC were decided on. Since the counters worked satisfactorily at a rate of 200,000 pulses per second, it was decided to operate the machine at the rate of 100,000 pulses per second, each pulse being about 2 microseconds wide. A tentative arrangement of cycling unit pulses and gates was planned. Pulses were not to be generated from within a unit; when a pulse was needed, an appropriate pulse from the cycling unit was to be gated. This was to prevent successive degeneration of pulses. Pulses were never to be gated against pulses but only against gates; this was to avoid sensitive timing problems.

(S4) Operational safety factors were introduced. For example, gate circuits were to be designed so that in normal circumstances they would operate in half the available time, and so that each tube in the circuit would produce three times the voltage needed to drive the following tube.

These design rules were all carefully planned to guarantee the reliability of the computing system that we had yet to design, build, experiment with and make operative. These rules, and simple logical and electronic design, were the main answer to those who said: A machine with twenty thousand vacuum tubes will never work; at every moment at least one tube will be out of order, and the answer will be wrong! I participated in many discussions of these design rules and became familiar with all of them.

(S5) The ENIAC was a very complicated system. The process of developing this system was simplified by concentration on the key units first: accumulator, high-speed multiplier, function table, and cycling unit. The arithmetic treatment of numbers, the basic logic of local programming, and the electronics of communication were developed for these units. However, the principles adopted for these key units had to be sufficiently general and flexible so as to cover the remaining units, even though the detailed design of the remaining units could be made to conform to these principles.

(S6) The "whole-part" nature of the design of the ENIAC is worth emphasis. This applied both to the system as a whole and the individual units. In designing a circuit, we didn't know how much signal power would be needed to perform a certain function until we knew how long the signal

wires were, and we didn't know this until we knew how many tubes would be needed. Hence design proceeded by successive approximations. We would make a tentative design of the whole, analyze it to see if it worked, and revise it. Moreover, the characteristics of the whole system were dependent on the characteristics of its units, and vice versa. Therefore, in designing a unit we had to keep in mind the whole system. The rules governing the whole system had to be held in mind since the system was constantly changing, and was designed over a long period, and the drawings lagged behind the design and sometimes even the construction.

(S7) The ENIAC was the first really large electronic system to be built. Much of the system design was done with little prior experimentation. Circuit drawings were revised frequently. Designs were sometimes changed as the result of discussions, and the women who were doing the wiring were informed of the change before the drawings could be updated. Changes were even made in the units after they were wired and before they were tested. In this connection, I recall a meeting of all wiremen, technicians, and engineers. The morale of the wiremen (mostly women) had become bad because we kept changing circuits after they were wired and before they were finished and could be tested. Eckert explained that this was because the ENIAC was a large, complicated system which was under development, and that because it was needed for the war effort we

didn't have time to make sure the design was correct before building it. This greatly increased the morale of the wiring group.

(S8) It is clear from this that the ENIAC was a very large electronic system, and that its design, construction, and testing were a team effort. I participated strongly in the development of the whole system as well as in the development of ~~the~~ many individual units. ~~already described.~~ Though each of us worked on various units of the system, we held group meetings to discuss common problems and coordinate the design. In addition, I had many discussions with Eckert and Mauchly about the design. I think that next to Eckert I had the best overall understanding of the ENIAC system and that on some matters, such as the operation of the multiplier, I had a better understanding than he did.

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(S9) I will illustrate the system aspect of the ENIAC design with two examples. First, we had discussions and made decisions about the frame of pulse sequences and gates which was to be produced by the central "clock" or cycling unit. This frame of signals had to be such that each unit could be designed to act on the basis of it. For example, in designing this frame we had to leave enough time between the program pulse and the first digit pulse so that the gate circuits activated by the program pulse would be ready to respond to the digit pulses. The longest

signal produced by the cycling unit was the carry-clear gate. This was used to clear the decades and PM units of accumulators back to zero (or 5 in the case of round-off) and also to control the final carry-over in an accumulator. The latter took the longest time. During the addition process, sequences of pulses representing the number to be added entered all decades (and the PM unit) in parallel. If there was a carry-over (i. e., if a decade cycled from 9 back to 0), a pulse was to be added to the next decade (or PM unit) to the left. It was not safe to do this immediately. Instead, the fact of carry-over was held in the carry flip-flop until the sequence of digit input pulses ended. Then the cycling unit sent out the carry-clear gate and a pulse which produced the carry signal. Now a carry could give rise to another carry, which would immediately pass to the next decade. In the worst case the carry would ripple all the way from right to left, and if two accumulators were connected together (to handle a 20 digit number), there could be a transit through 19 decades. The cycling unit had to be designed so that the carry-gate was left on long enough for this to be completed. After the two accumulators were built, this transit time was measured. As I recall, we then extended the duration of the carry-clear gate.

(S10) My second example of system design concerns the length of the numbers used in the ENIAC. In the end we decided on decimal numbers which had ten digits, with provision for pairing accumulators to handle 20 digit numbers. But at the beginning of the project we did not know how long to make the numbers. We knew how many digits of accuracy were needed for firing tables, but we did not know what the cumulative effect of two kinds of errors would be. Truncation errors result from approximating continuous differential equations by discrete difference equations. Round-off errors are the statistical accumulation of the errors due to rounding-off answers. We planned for the ENIAC to use a less sophisticated method of integration than was used by girls with mechanical calculators. These less sophisticated methods would require many more steps of integration, and hence round-off errors and truncation errors would be more important when the ENIAC solved a trajectory than when the trajectory was integrated by hand. The solution of this difficulty was to make the numbers used in the computation longer and hence more precise than the input data and answers. There were many discussions of these matters and some mathematical research was done before we decided on 10-decimal digits. These discussions and decisions involved mainly John Mauchly, Herman Goldstine, Professor Hans Rademacher (of the Mathematics Department), Dr. Leland Cunningham (of Aberdeen), and myself.

(S11) The ENIAC computing system consisted of 40 panels (each two feet wide by about eight feet high), 3 portable function tables, and two IBM card machines. All of these were interconnected by cables and "trays." In terms of functions the machine is best divided into these four parts:

(I) The basic computing units, or units which stored numbers or computed, and had their own local program controls. There were 20 accumulators, the multiplier, 3 function table units, and the divider square-rooter. Together these basic computing units constituted about three-quarters of the machine.

(II) The master programmer, which supervised the program controls of the preceding units.

(III) The input and output units: the constant transmitter and its card reader, and the printer and its card punch.

(IV) The cycling unit, which provided the basic reference frame of electrical signals (various sequences of pulses and the carry-clear gate) used for synchronizing the preceding units.

(S12) We designed the main computing units of the ENIAC first: the accumulator, the multiplier, and the function table, along with the cycling unit to operate them. (The divider square-rooter was left until later.) When most of the circuits of these main computing units had been

designed and drafted, Sharpless and I were assigned to review and analyze the complete system. We were to determine as far as possible at that stage whether the logical and circuit designs were correct and would perform the computing functions we had planned for them. This included the interaction of the various units, as well as their internal operations. We corrected faults and made suggestions for improvement. When we were part way through (I think we had finished the accumulator and the multiplier), Sharpless was asked to devote full time to the cycling unit, and Shaw and I finished the task. We did the function table together and perhaps looked at some of the remaining units.

(S13) I did some work on programming the whole system, as well as on programming the high-speed multiplier and its associated accumulators during the test period. Under my direction, Don Hunt drew up a connection diagram for an ENIAC program, probably for a ballistic trajectory. Hunt recently wrote me that he did this in the first half of 1944.

(S14) Most of the logical and electronic design of the ENIAC was done in a 21-month period, which is a surprisingly short time for such a complicated and novel machine. The original proposal for ENIAC, "Report on an Electronic Diff.* Analyzer," by Eckert and Mauchly, was dated April 2, 1943. The logical and electronic design of the ENIAC was

essentially complete at the end of 1944, just 21 months later. A model machine with two accumulators and a small cycling unit was made operational in the summer of 1944. The main design drawings of the accumulator, multiplier, function table, and master programmer had been drafted, approved, and checked by the end of 1944. Most of the ENIAC units were under construction at that time.

(S15) Though the logical and electronic design of the ENIAC was essentially complete by the end of 1944, the ENIAC was far from being operational at that time. No complete units had been constructed except for those in the model machine. After the units were constructed they would have to be tested, modified, corrected, and made operational. For example, the zero-line error in the high speed multiplier was not even discovered until the summer of 1945 (see paragraphs M17 to M19 below). Moreover, some logical and electric design work was done in 1945. The main diagrams for the divider square-rooter were not drafted until the spring of 1945. Some design work was done on the cycling unit in 1945; many of the drawings for this unit were not checked by Sharpless until August, 1945. And in the case of those units whose logical and electronic design had been essentially completed in 1944, later design modifications were needed to make them operational. For example, many of the changes in the accumulator and multiplier drawings which we called "semi-final revisions" are dated June and July, 1945.

(S16) I made several non-inventive contributions to the ENIAC project which show the extent of my involvement in and knowledge of the whole system. Because of my ability to write I was given considerable responsibility for the ENIAC progress reports. This gave me an opportunity to follow developments intimately. I designed the direct-current power supplies for the ENIAC and ordering special transformers for them. We needed 78 different voltage levels and used 28 separate power supplies to obtain them. The remaining voltages were obtained from resistor dividers.

(S17) Summary: The ENIAC was a very large and complicated system. Its essential electronic and logical design was completed in the surprisingly short time of 21 months. The design of all the units had to be coordinated at both the logical and electronic levels. I participated in and contributed to discussions on the design of the whole system. I was the only person to make a complete analysis and check of the circuit design of the basic ENIAC units.

HIGH-SPEED MULTIPLIER

(M1) I did much of the logical and electronic circuit design of the high-speed multiplier, completing the conception of the invention of this unit. At the time I began this work, Eckert and Mauchly had worked on the general method of multiplication. There was to be a multiplier selector, a resistor matrix multiplication table, a multiplicand selector, and shifting circuits. Sharpless had built a sample slice or "cross-section" of the proposed electronic multiplication circuits. His experimental work with this cross-sectional circuit showed that the Eckert-Mauchly method of multiplication was electronically feasible. Sharpless had also done some preliminary work on the programming circuits of the multiplier.

(M2) The multiplier unit was to operate in conjunction with four accumulators: one to store the "multiplier," another to store the "multiplicand," and two to store the partial products, with the final product appearing in one of these. The multiplier unit was to accomplish the following in one addition time: Select one digit from the multiplier accumulator, multiply the entire multiplicand by this digit, and shift the partial products to the correct decimal position. After this, complement corrections were to be made and the partial products combined. All of this was to be controlled by programming circuits yet to be designed.

(M3) I then worked out and completed the logical and electronic design of the high-speed multiplier. Because logical design and circuit design were interdependent, they had to be done together. The logical design of a gating circuit might be correct, but then analysis of its electrical behavior would show that the voltage available to operate a tube was marginal, or that the capacitance contributed by a long wire was so great that a gate barely operated by the time the relevant pulse arrived from the cycling unit. Something must then be done to provide the required safety factors. Another tube would probably be added to amplify the signal. But this tube would usually reverse the polarity of the signal, and might change the physical arrangement of the circuit, so the whole design had to be revised.

(M4) The resistor matrix which stored the multiplication table through nine times nine was the heart of the high-speed multiplier. It was a matrix of horizontal and vertical wires, interconnected by resistors. There was a horizontal wire for each possible digit, and a set of vertical wires (about 50) controlling gates which received pulses from the cycling unit. At each intersection of a horizontal and vertical wire of the multiplication table matrix, these two wires were or were not connected through a resistor, according to what arithmetic demanded. In this resistor matrix, a desired connection between a horizontal wire and a particular vertical wire

was direct, passing through only one resistor. An undesired connection (between a horizontal wire and a vertical wire which it should not operate) was indirect, passing through at least three resistors. Unfortunately, there were many such back paths.

(M5) This led to the problem of parasitic signals. The multiplication table and its associated circuits had to be designed so that there was ample signal voltage to operate a gate which should be operated, but not enough parasitic signal voltage to operate a gate which should not be operated. The preliminary design of the multiplication table had determined whether a resistor should or should not be placed at an intersection. Part of my task was to calculate the resistor values and design the associated circuits so that this part of the multiplier operated reliably.

(M6) Sharpless made the following inventive contribution to the logical design of the program control circuits of the multiplier unit. The multiplier unit was to use two addition times to prepare for the multiplication process proper. The multiplier unit was then to carry out the multiplication process for a variable number (2 to 10) of decimal places of the multiplier, according to the setting of a "places switch" associated with each program control. (There were to be many such program controls and the operator was to pre-set the places switch for each according to the accuracy he wanted for that particular multiplication.) Finally, the multiplier unit was to use two

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more addition times to complete the multiplication by making complement corrections and combining the left-hand and right-hand partial products.

(M7) Thus a multiplication was to be accomplished in three successive time periods: two addition times for preparation, followed by two to ten addition times for multiplying each multiplier digit by the multiplicand, and finally, two addition times to complete the multiplication. We planned to use counters and possibly flip-flops to control all this. The problem was: How were we to get a variable number (2 to 10) of addition times in the middle of the process?

(M8) Sharpless' inventive solution was to use a single control counter, and to clear it to a selected point other than its initial position by gating from a stage of the counter with the signal coming through the places switch. His solution is shown in Fig. 42A (Sheet 40) of the ENIAC patent 3,120,606. Each of the gates numbered 4 (P14) through 12 is fed on one control grid from the program counter ring and on the other grid by a signal from a program control (tube P37 of Fig. 42B Sheet 41) passing through a places switch. When these grid signals occur in coincidence, the counter jumps from stage 4, 5, ..., 11, or 12 to stage 13. Stages 13 and 14 control the last two addition times, and hence the final steps, of the multiplication.

(M9) Sharpless once wrote that this solution to the multiplier control problem was his idea. In his March 4, 1946 "Copy of Letter to J.P.E., Jr." i.e., Eckert, Sharpless says "In addition under item 5 of 'Outline of Patent Application Material,' is a note about clearing counters to selected points by gating from a stage of the ring, as in the multiplier program ring. This, too, I believe is my idea." See Exhibit F.

(M10) On pages 1 and 2 of Chapter X of the First ENIAC Project Report (to December 31, 1943) it says: "The circuit design of the multiplier, excepting for the programming circuits, is completed." This was true in the sense that the general method of multiplication had been conceived, a cross-section of these circuits had been built and was under test, and some preliminary design work had been done on the programming circuits. But the actual logical and electronic design had not yet been worked out, so that the conception of the high-speed multiplier was not yet complete. I will show that this is so on the basis of the materials included in the report, by reference to entries in my Project PX Engineering Notebooks, and by the dates on the drawings of the high-speed multiplier.

(M11) Only two drawings of the multiplier were included in the First ENIAC Progress Report. The first was PX-6-54 (Simplified Diagram of the High-Speed Multiplier.) This diagram was highly schematic, showing only the general method of multiplying two 4-digit numbers. As we said

in the Report: "It is important to note that this diagram is only for the purpose of explaining the operation of the multiplier and is not a wiring diagram. Not only are such circuit details as screen grids, etc., omitted, but also load resistors, amplifiers and buffer tubes, phase inverters, etc. Furthermore, the multiplication table to be used (see Drawing PX-6-70 in this chapter) is a complement of the table shown in the diagram...." (p. 1 of Ch. X). Moreover, this Drawing PX-6-70 contained an important error, which was not discovered until the summer of 1945; this error will be explained in paragraph (M18) below. Thus the First ENIAC Progress Report contained only two multiplier drawings, and the multiplication table resistor matrix was incorrect in both.

(M12) It is stated in this Report that "the program circuits of the multiplier are now being designed. Since they are the same in many essential respects as those used in the accumulator, the work already done on the accumulator programming is being utilized" (p. 11 of Ch. X). This is only true in a general sense. At the time this was written the design of the accumulator program circuits had not yet been completed, so to a considerable degree I had only verbal ideas and incomplete drawings of the accumulator program circuits to use as a model when I designed the multiplier program circuits. Moreover, the problem of controlling a variable number (2 to 10) of addition times in the middle of the multiplication

process did not occur in the accumulator. This is the problem that Sharpless solved so neatly with his idea of clearing the control counter to a selected point other than its initial position; see paragraphs (M6) to (M9) above.

(M13) The following entries on the multiplier occur in my Engineering Notebook Z16. On page 211, with date March 9, 1944, there is a mechanical layout of the three panels of the multiplier unit, showing how the various circuits would be arranged. This is followed by several pages of analysis of the "Parasitic Actions in the Multiplier Table." The next pages give the status of the design and construction of various ENIAC units. The first model of the accumulator had been designed and construction was under way. We planned to use the receiver and transceiver plug-in units of the accumulator in the multiplier, though in the end we used only the latter type. Not counting these plug-in units, the electronic design of the various parts of the multiplier ranged from 50% complete to 90% complete, and no construction had yet been done (page 220). Following this there are various other entries about the multiplier, the last occurring late in April, 1944, near the end of Notebook Z16.

(M14) My Second Engineering Notebook Z17 was issued April 28, 1944. Page 17 contains "Experimental Tests to be Made on the Multiplier." The test described is related to Sharpless' idea of clearing the multiplier

control counter to a selected point other than its initial position; see paragraphs (M6) to (M9) above. On June 4, 1944, we decided to remove the "direct digit input" of the accumulator so as to improve the reliability of the input circuits (p. 29). This required changes in the multiplier design, since we had planned for the multiplier digit outputs to go into the partial products accumulators through these direct inputs. On about May 8, 1944 (page 25) and on July 26, 1944 (pages 36-37), I re-analyzed the parasitic signals in the multiplication table resistance matrix to see whether the operation was safe if the resistance values should vary as much as 10%. About a year later I analyzed these parasitic signals again in connection with an error I discovered in the multiplication table when I tested it; see paragraphs (M17) to (M19) below.

(M15) After completing the logical and circuit design of the multiplier unit, I informed the draftsman of the details and saw that he drew correct diagrams of the design. To this end, I prepared rough drafts of the circuit diagrams, supervised the drafting of them, and prepared cross-sectional drawings to facilitate checking and revision. Many of the diagrams for the multiplier were drawn by F. Robert Michael, and most were finished in October and November, 1944. Sharpless and I went over the design together to verify its correctness and its compatibility with the rest of the ENIAC system. We signed most of the drawings in December, 1944.

(M16) The multiplier circuits were wired under my direction. I checked this wiring to see that it was correct, and supervised the assembly of the three panels of the multiplier unit. Using a version of the cycling unit and some accumulators, I set up and ran programs to see if the logical and arithmetical design of the multiplier was correct. I also conducted electronic tests and measurements. I supervised the correction of the defects of the multiplier, and finally, certified that the unit was operational. This testing and correcting of the circuits was started in the summer of 1945 and completed in November of that year. There are entries in my second Engineering Notebook Z17 concerning this work at pages 54-56 (July, 1945), pages 58-59 and 62 (August 23), pages 64-73 (the first of these pages is dated September 11), pages 77-80, and pages 81-83 (the first of these pages is dated November 2, 1945). I was assisted by Bob Michael in much of the work described in this and the next three paragraphs. Kite Sharpless also helped.

(M17) There were some small errors in the multiplier, but the chief error occurred in the multiplication table resistor matrix and its associated circuits. Suppose, for example, that the multiplier digit being used at a given addition time was 7. The voltage on horizontal wire 7 of the multiplication table was lowered, causing currents to flow through all the resistors connected between it and the vertical wires of the multiplication

table matrix. These currents lowered the voltage on these vertical wires, turning off the output gates they controlled. The desired pulses then passed through the gates that were not turned off and passed into the multiplicand selector circuits. If the multiplier digit were zero, then all of the output gates should be turned off. In other words, even though the product of zero and any multiplicand is zero, a horizontal wire for a zero multiplier digit was needed in the table matrix.

(M18) When first tested, the multiplier gave a wrong answer for most numbers. By testing different cases and analyzing the circuits, I isolated the trouble to the multiplier digit zero, and immediately realized where the error was and how it had arisen. The original design of the multiplication table resistor matrix had assumed that the output gates would normally be off, so that only the gates needed would be turned on, and of course, no gates were needed when the multiplier digit was zero. Hence for this mode of operation we had not needed a zero-input line to the table matrix. However, for polarity reasons we had later reversed this mode of operation and used a "complement" table. We had changed all the resistor connections for the lines already there, but had overlooked the fact that we needed a zero-input line.

(M19) To correct the mistake I had the following circuits added to the multiplier: a "zero" row of tubes in the multiplier selector, a "zero" row of resistors in the multiplication table, and the needed amplifying tubes in between. Drawing PX-6-101 (Multiplier Selector Chassis) was corrected on August 2, 1945 and initialed by Bob Michael. Drawing PX-6-70 (Multiplication Table Variation 6-Complementary Table) was corrected on July 31, 1945 and initiated by Kite Sharpless; it was renumbered as PX-6-170 at the same time. I recalculated the parasitic signals in the multiplication table resistor matrix to make sure that the table operation was still reliable; these calculations are on pages 54-56 of my Second Engineering Notebook Z17 and were made in July, 1945. At a meeting of August 23, 1945 (called "Final Work Meeting") we listed what remained to be done on the ENIAC units. The first two items under the multiplier were "Put in 0 line" and "change table" (p. 59).

(M20) The high speed multiplier was the most complicated electronic unit of the ENIAC. It occupied three two-foot wide panels and operated in conjunction with 4 or 6 accumulators. It had more than a thousand vacuum tubes. We made more circuit design drawings for it than for any other unit.

(M21) Summary of my contributions to the high speed multiplier unit:
I completed the conception of the invention of this unit. Starting from the general design principles of Eckert and Mauchly and from Sharpless' experimental work with a cross-section of some of the circuits, I worked out the logical and electronic design of the high-speed multiplier. This included the programming circuits, and required careful analysis of the parasitic signals in the multiplication table resistor matrix. I then supervised the drafting and wiring of the unit, tested it, and saw that the errors in it were corrected.

(M22) Summary of Sharpless' contributions to the multiplier:
He did early experimental design work on the multiplier. Sharpless also made a specific inventive contribution to its control circuits. In controlling the multiplication process, we needed to obtain a variable number of addition times in the middle of the process. Sharpless invented this solution to the problem: clear the control counter to stage 13, rather than to its initial position, by means of a gate signal coming from a places switch.

ACCUMULATOR

(A1) Each accumulator was to perform the following functions: Store a 10-digit number with sign, receive a number over a trunk in pulse form and add that number to its contents, and transmit its contents in pulse form either positively or negatively. It was to contain its own programming circuits for controlling and directing these functions.

(A2) Eckert and Mauchly worked out the general principles of the accumulator design. Most of the actual design was done by Eckert, with assistance first from Frank Mural and later from John Davis. Sharpless, Shaw and I all made contributions to the design of the accumulator. Mauchly conducted the two-accumulator test in the summer of 1944, with Sharpless working on the small cycling unit, which provided the pulses and gates for this test.

(A3) My first important contribution to the design of the accumulator was a logical design contribution involving the complement system of handling negative numbers.

(A4) The complement system we first adopted is called the "tens" complement system. A positive ten-digit number is represented in the normal way, with zero in the PM counter. A negative number is represented by its tens-complement. The tens-complement of any number is calculated by reversing its sign digit (changing zero to one and one to zero), complementing each digit with respect to nine (i.e., taking the difference between that digit and 9), and

adding one pulse in the units place. The effect of these operations is to complement every digit with respect to 9 except the units digit, which is complemented with respect to 10. Hence the name, "tens-complement."

(A5) We originally adopted the tens-complement system because it was the complement system we were familiar with. We began to design the accumulator to operate in accord with this system. The choice of complement system also affected many other units of the ENIAC. Indeed, it affected in some way any unit that handled negative numbers. The effect on the high-speed multiplier unit was greatest of all. The central part of the multiplication process ignored the sign (PM) digits of the multiplier and multiplicand; but if either the multiplier or the multiplicand was a complement, corrections were made near the end of the multiplication process.

(A6) During the ENIAC project a few of us made trips to Aberdeen to report on our work and consult with people there, particularly Dr. Leland Cunningham. Of the people at Aberdeen, he was in closest contact with the project and knew most about digital computing. I took at least two such trips, including one with John Mauchly and one with Pres Eckert. On one of these trips John and I learned about another complement system, called the "nines" complement system. This differs from the tens-complement

system in the treatment of the units digit. As mentioned earlier, the units digit is complemented with respect to ten in the tens-complement system, whereas the other digits are complemented with respect to nine. In the nines-complement system the units digit is complemented with respect to nine, as are the other digits, but a cyclic carry circuit is established from the left of the number back to the units place.

(A7) The nines-complement system came to our attention when we examined and discussed the Aberdeen IBM machines with Cunningham. We learned then that this system has certain advantages over the tens-complement system. After we returned to the Moore School, John and I considered the two alternative systems in terms of their applicability to the ENIAC and discussed their relative merits with Pres. As I recall, there was a discussion of this topic at a meeting of the ENIAC engineers. We concluded that the nines-complement system would be better, and decided to change to it.

(A8) I started to make the necessary changes in the design plans of the accumulator. Though everything seemed all right, and Mauchly thought the new method for handling complements would work correctly, I nevertheless decided on my own initiative to re-think the implications of the nines-complement system for the ENIAC. I analyzed complementation for the

accumulator and the multiplier, taking into account related matters. Most importantly, I considered the effect of the nines-complement system on our method of rounding-off numbers in an accumulator. We planned to design the accumulator so that it could be cleared to 5 (rather than 0) in a selected decade position, this position being selected by the "significant" figures switch. The decade cleared to 5 was, of course, immediately to the right of the least significant digit to be kept. The unwanted digits (insignificant figures) were to be deleted by means of a "deleter" inserted into the digit transmission cables. The significant figures switch also re-routed the complement pulse when an accumulator transmitted subtractively, that is, transmitted the complement of its contents.

(A9) In our original analysis of the effect of changing from the tens-complement to the nines-complement system, no one had thought to consider the effect of this change on our round-off procedure. In my re-analysis I did consider this effect, and found that our changed design did not work correctly. We had left the round-off procedure unchanged. This procedure gave the wrong answer when the number being rounded off was a complement in the nines-complement system. In this case, the number was rounded down one unit too much. I determined that the correct procedure for the nines-complement system was to add five for positive numbers and subtract five for negative numbers (complements). I further

determined that this procedure was not easy to implement in the ENIAC system. For on this procedure the round-off process depended on whether the number being rounded-off was or was not a complement. But at the time an accumulator was cleared it could not be known whether the number to be ~~eventually transmitted~~ rounded off would or would not be a complement. AWB 1/31/72

(A10) I could not see any practical way around this difficulty, and concluded we would have to go back to the tens-complement system, even though we had recently decided to abandon it. The new nines-complement system was also going to lead to complexity in the arithmetic design of the multiplier. I discussed the matter with John and Pres, and they agreed with me. Hence we decided to return to our original complement system. Only in the case of the accumulator had the design been carried out far enough to necessitate revisions in the drawings. But the designs of the multiplier, function table, divider square-rooter, constant transmitter, and printer were all influenced by our choice of complement system.

(A11) My work on complements which is described in the preceding four paragraphs was done sometime in late 1943 or very early in 1944. There is pasted in my Engineering Notebook Z16 a typed rough draft of a report which has corrections in my hand. The title is "Report for Project PX. September 22, 1943. ACCUMULATORS AND TRANSMITTERS." This report

explains the tens-complement system, and does not mention the nines-complement system. But my work on complements was done before our First ENIAC Progress Report (to December 31, 1943) was written, for on page IV (23) of this report we discuss the nines-complement system and give reasons for adopting the tens-complement system.

(A12) On page 2 of the Preface of the First ENIAC Progress Report it says "In the month and a half following the date (December 31, 1943) of this report, final wiring diagrams and construction drawings have been prepared for most of the circuits not reported in detail here, and construction of complete panels has been begun." This was probably intended as a statement about the first model of the accumulator, though many of the accumulator drawings bear later dates. It is definitely not true of any of the other units, as the dates of their drawings show. Moreover, many changes were made in the accumulator design after mid-February, 1944, and some were made after the test of two accumulators of the first model which began in about May, 1944. Indeed, several of the accumulator drawings have "semi-final revisions" dated in the summer of 1945.

(A13) My second important contribution to the design of the accumulator was made in about May, 1944. It was an electronic contribution, and in the end affected circuits throughout the ENIAC. My discovery occurred in the following way.

(A14) After the diagrams for the first model of the accumulator were drawn, Pres Eckert asked me to make a careful analysis of the accumulator circuits to see if they were correct and to suggest changes that would improve them. I distinctly recall making the following important discovery. Each of the program controls of an accumulator operated the common gate circuits of that accumulator. The program controls controlled these gate circuits through vacuum tubes we called "buffers." There were a total of twelve program controls (eight "transceivers" and four simpler "receivers") in the final design, though this exact number may not have been fixed at the time. In one particular gating circuit there were twelve buffers (triodes) operating in parallel with a common plate load resistor. This was a twelve input disjunction: if any buffer was turned on, current would flow through that tube and through the common load resistor, the latter current then turning off a tube of the gating circuit.

(A15) By our rules, a tube was regarded as "off" if only a small current was flowing through it. In analyzing this circuit, and the different conditions of its operation, I discovered that the small currents through all these buffers, even when they were off, could add up to enough current to operate the following tube when it should not operate. In other words, leakage currents through this common resistor of the gate circuits might be sufficient to partially operate the accumulator when it should not be operated, producing

incorrect results. I also saw that this buffer leakage problem would be much worse in the high-speed multiplier, because it was to have many more program controls. As finally designed and built the multiplier had twenty-four program controls.

(A16) I mentioned this buffer leakage error problem to John Mauchly, who agreed it was a problem. He then mentioned it to Pres Eckert, who soon came to talk to me about it. (I remember this vividly, and I can still remember the place in the ENIAC design room where I was working when Pres came to talk to me about it.) Pres said that I was correct in seeing that it was a problem. He said that to solve it we should "overdrive" the grid of the gate tube (bias it positively) by connecting it through a resistor to a voltage higher than the cathode voltage. This overdrive (positive bias) provided leakage currents through the program control buffers without allowing the grid of the gate circuit tube to go negative.

(A17) I will illustrate this solution by reference to Drawing PX-5-115 (Accumulator Cross Section). In the Receiver Plug-in-Unit, the lower triode of tube number 62 drives point CPB, which goes to the grid of Gate Unit tube G50. In the Transceiver Plug-in-Unit, the left-hand triode of tube number 61 also drives point CPB at the grid of Gate Unit tube G50. Hence there are twelve tubes (triodes) driving the grid of G50. The leakage

currents through all of these tubes add up, and might turn tube G50 off when it should be on, causing an incorrect calculation. But this is prevented by biasing the grid of tube G50 positively. The cathode of this tube is at -385 volts; its grid is connected through L_{CPB} to a 12K resistor and thence to -375 volts, so there is a positive 10 volt bias on this grid. The leakage currents in the eight triodes driving this grid do not lower the grid voltage appreciably because of the positive bias or overdrive. Hence these leakage currents will not turn tube G50 off when it should be on.

(A18) Several groups of revisions are listed on drawing PX-5-115. The second group is signed by me and dated 6/3/44. This gives a rough indication of when I worked on the accumulator circuits. The next group of revisions was signed by Robert Shaw on November 28, 1944, but it covers an extended period. The first entry of the group is "voltages changed and resistors added to provide positive bias on grids"; it was signed "JD" (John Davis) and dated "6/9". This shows when the circuits of the accumulator were changed to introduce positive biasing on the grids.

(A19) Sometime later Robert Shaw and I measured the grid currents of some tubes so we engineers would know how to design circuits with these tubes that had the correct amount of grid overdrive. Two pages of my

Engineering Notebook #17 are devoted to overdrive measurements. The heading "Overdrive Measurements" is written in my handwriting and many entries in the table are in my handwriting. However, other entries are not in my handwriting. The dates 10/13/43 and 10/21/44 are given, the latter occurring with the signature "R. F. Shaw". The table gives the grid and plate currents for various voltage values for tube types 6L6 and 6AC7.

(A20) This overdrive solution to the buffer leakage problem led to a general improvement in the reliability of the ENIAC circuits. For we then saw that the action of most tubes would be safer if we biased the grids so that when on, they would be positive with respect to the cathode. This positive bias protected the circuits from spurious signals or "cross-talk".

(A21) As a consequence of my discovery, we made a general design rule applicable to the tubes used for switching in the ENIAC: their control grids were to be biased or driven positively ("overdriven"). This rule contributed to the reliability of the ENIAC and thereby to its success. This rule and its rationale are stated on pages III-1 and III-2 of our Second ENIAC Progress Report (January 1, 1944 to June 30, 1944). The rule is <u>not</u> mentioned in our First ENIAC Progress Report (to December 31, 1943).

(A22) Summary: My first important contribution to the accumulator included the complement system for handling negative numbers. We began to design the accumulator on the basis of the tens-complement system. We then learned of the nines-complement system and decided it would be better. On my own initiative I analyzed its use in the ENIAC further and discovered that our planned use of it would give us incorrect round-off, and that it would be difficult to employ the nines-complement system in the ENIAC. As a consequence, we returned to the tens-complement system. This choice affected the design of the other units of the ENIAC, particularly the multiplier.

(A23) Summary, continued: I discovered that when many tubes operating as buffers were connected in parallel to operate a single gate tube, the leakage currents through these buffers might operate the gate tube incorrectly. Though I discovered this leakage error problem in the accumulator circuits, the problem would have occurred in many other units, and would have been particularly dangerous in the multiplier. Eckert said that to solve this problem we should "overdrive" (bias positively) the grid of the gate tube. This discovery of the buffer leakage problem and its overdrive solution, led to a general improvement in the reliability of the ENIAC circuits, for we then saw that the action of most tubes would be safer if we overdrove their grids.

FUNCTION TABLE UNIT

(F1) Robert Shaw joined Project PX in September, 1943. His first work involved the design and construction of test equipment, such as pulse generators and oscilloscopes. He next worked on the logical and circuit design of the function table unit. The general pattern of the design of this unit had been planned by Eckert and Mauchly.

(F2) The function table units, of which we built three, were intended primarily for storing mathematical functions used in a computation, such as the numerical table giving the resistance of the air to a shell as a function of the shell's velocity. There was a large portable function table resistor matrix associated with each unit. It was a bank of nearly 1500 switches by means of which the programmers could change the interconnections of a resistor matrix. This part of the function table unit was so bulky that it was built as a separate structure, called a "portable function table."

(F3) There were 104 "horizontal" lines into this matrix, corresponding to the 104 argument values -2, -1, 0, 1, ..., 98, 99, 100, 101. There were 124 vertical wires for two sign digits and twelve decimal digits. To set a given function value into the resistor matrix, the programmer would set the switches in positions corresponding to this value. Suppose, for example, f(23) = +357942. The programmer would set switches in the

number 23 row of the table as follows: the PM switch at zero (for plus), the next switch at 3, the next at 5, the next at 7, etc. In setting these switches the programmer would be connecting resistors between horizontal and vertical wires. When, for example, the number 23 was activated (i.e., had its voltage lowered), currents through these resistors would activate inverters and then gates so that the number + 357942 would be emitted from the function table in pulse form.

(F4) The two-digit argument value representing the "x" of "f(x)" was to be stored in two decades of an accumulator. The original plan for using the information in these two decades was to use a direct current (or "gate") connection rather than to send digit pulses. Relatively slow output signals ("gates") would be taken from each stage of these decades and fed into the function table unit, where they would be gated against each other to produce a signal that would activate the correct horizontal wire (in our example, wire 23) of the resistor matrix.

(F5) The logical structure of the function table was complicated by the fact that two-digit accuracy in the argument value of a function is usually not enough. A more accurate function value may be obtained by "interpolation," a computational process using a function value and its neighbors. Suppose the machine needs the function value f(23.72). Rather than use f(23), it is

better to interpolate and use 28% of f(23) and 72% of f(24). An even better value of f(23.72) can be obtained by making a calculation from the five function values f(21), f(22), f(23), f(24), and f(25). We therefore felt it necessary to design the function table unit so that it would provide any of these values automatically when instructed to do so.

(F6) Each program control of the function table unit was to have an "argument switch" which could be set at -2, -1, 0, +1, +2, to control which of the function values $\underline{f}(\underline{x} - 2)$, $\underline{f}(\underline{x} - 1)$, $\underline{f}(\underline{x})$, $\underline{f}(\underline{x} + 1)$, or $\underline{f}(\underline{x} + 2)$ was to be transmitted by the function table when that particular program control was active. We needed a satisfactory circuit which would use this information (-2, -1, 0, +1, or +2), together with the two-digit argument value $\underline{x}$ coming from the associated accumulator decades, to select the proper horizontal wire of the function table ($\underline{x} - 2$, $\underline{x} - 1$, $\underline{x}$, $\underline{x} + 1$, or $\underline{x} + 2$).

(F7) Shaw's design problem was compounded by the fact that the function table resistor matrix was very large and had variable connections. At each point where a horizontal wire went past a group of 10 vertical wires, there was to be a switch which connected a resistor from the horizontal wire to any one of the ten vertical wires, thereby determining a digit value (0, 1, 2, ..., 8, 9). This made the parasitic signals of the matrix worse and more difficult to handle than in the multiplier resistor matrix. To calculate the harmful

effects of parasitic signals in the multiplication table, I had to consider only the fixed connections of that small table. To calculate the harmful effects of parasitic signals in the function table resistor matrix, Shaw had to survey all possible tables formed by all possible switch settings in this much larger table, find the worst case, and analyze it.

(F8) Because of these difficulties in the design of the function table unit, the tube types we were using in the accumulator were not adequate. Shaw therefore carried out an experimental investigation of various kinds of tubes to find some that would be suitable for the matrix drivers and matrix output gates. He tested various tubes and measured their characteristics. Since there was a large signal loss through the resistor matrix and high distributed capacitances, he could not use pulse techniques (and hence capacitively coupled circuits), and so he designed large "pile-ups" of DC-coupled circuits.

(F9) After Shaw had worked out a fairly detailed design, I went over the circuits with him. He had analyzed the parasitic signals of the function table resistor matrix in terms of what he had thought was the worst case, that is, the worst combination of settings for the approximately 1500 switches of the table. However, I found a case that was considerably worse. Hence the design of the circuit had to be changed to accommodate this case.

(F10) My analysis of Shaw's function table design showed it to be marginal in reliability; there was not enough power to drive the circuits safely. Normally, we would have added another "layer" of tubes, but in this case there were difficulties. There were 104 tubes, and another layer would have meant 104 additional tubes. There was not enough room to add that many tubes, and we didn't want to allocate a third two-foot wide panel to each function table unit. Using the results of his earlier investigations of tubes, and perhaps making more measurements, Bob redesigned the circuits so they were satisfactory.

(F11) I also suggested the dynamic method of shifting used in the function table unit. I do not remember making this contribution but rely on Shaw's memory of it. Bob Shaw and I met with Yuter in early August, 1964 to discuss our contributions to the ENIAC. At that time Shaw told me he remembered very distinctly my suggesting to him the dynamic method of shifting.

(F12) In his letter to Sharpless, Yuter and me, of October 31, 1964, Shaw described my contribution as follows. "Kite's experience with the multiplication table proved helpful, as previously noted, and for a while I was hopeful that I could use his shift circuit designs in mechanizing the function table interpolation feature. Tying these into the system, however,

proved a bit troublesome, and Art came up with a very ingenious suggestion for dynamic shifting, which involved the offsetting of connections by two columns in tying the argument register outputs to the matrix, so that by selecting anywhere from zero to four shift pulses and feeding them into the argument rings after the argument was stored, it was possible to obtain any of the functions f(x - 2), f(x - 1), f(x), f(x + 1), or f(x + 2). This appreciably simplified the circuits." (PX 18, 580)

(F13) Shaw's problem with the shifting circuits arose from the requirement that the function table provide any of the function values $\underline{f}(\underline{x} - 2)$, $\underline{f}(\underline{x} - 1)$, $\underline{f}(\underline{x})$, $\underline{f}(\underline{x} + 1)$, $\underline{f}(\underline{x} + 2)$ as requested by the setting of the argument switch. How should he combine the two digits of information $\underline{x}$ in the argument decades with the information (-2, -1, 0, +1, +2) set in the argument switch so as to actuate the proper horizontal wire ($\underline{x} - 2$, $\underline{x} - 1$, $\underline{x}$, $\underline{x} + 1$, $\underline{x} + 2$) into the function table matrix? Shaw had attempted to use a shifting circuit, like that used in the multiplier, for this purpose. This required more voltage levels and more tubes, when he already had too many of both.

(F14) I considered Shaw's problem and invented the following solution. Instead of using direct current ("gate") signals from the two decades holding the function argument $\underline{x}$, we transmitted $\underline{x}$ from these decades in pulse form to two counters in the function table unit. Then we offset the connections

between the two argument counters and the horizontal lines of the table matrix by two units so that when the counters stored the number x, the table matrix thought it stored $x - 2$. For example, when the argument counters stored the number 23, the number 21 wire of the table was active, corresponding to the function value $f(x - 2)$. If the argument switch called for $f(x - 2)$, nothing needed to be done. But if the argument switch called for a value other than $f(x - 2)$, pulses were sent into the argument counters to advance them accordingly.

(F15) I will illustrate my method with an example. Suppose a function table control was set to transmit $f(x)$, i.e., the argument switch was set at zero (0). Suppose further that on a particular occasion when this control was activated, the associated accumulator stored $x = 23$. The function table program circuits first called for x, the two digits of x (2 and 3) were transmitted from the argument accumulator into the argument counters so that the latter registered 23, and the gate circuits activated wire 21 of the function table. The function table program circuits then sent two pulses into the units argument ring (since the argument switch of the active control was set at zero), the argument counters advanced to 25, and the gate circuits then activated wire 23 of the function table. This was the wire which should be activated, since the function value $f(23 + 0)$ or $f(23)$ was desired.

(F16) My method of shifting was dynamic, in contrast to the static method which was used in the high-speed multiplier and which Bob had tried to apply to the function table unit. The dynamic method led to much simpler circuits and fewer voltage levels in the function table unit.

(F17) My invention of the dynamic shifting method occurred sometime between April 22, 1944 and July 31, 1944. Page 260 of my first Engineering Notebook Z16 has notes of a meeting of the former date which show a block diagram design employing a static "selector-shifter" as well as a selector. This design is not satisfactory, because no provision is made for carry-over from the units position of the two-digit argument to the tens position. On the other hand, my dynamic shifting method was described in our second ENIAC Progress Report (January to June, 1944 - written about July 31, 1944), Chapter IV, pages 25 and 29, as follows: "The basic design of the function table has been altered in some fundamental respects (see Drawings PX-7-116, PX-7-117, PX-7-118, which follow). The function selector (of about 140 tubes) which was to operate from the static outputs of two decades of the argument accumulator has been replaced by two decade counters (see the argument register circuits, Drawing PX-7-117). During the addition times allowed at the beginning of the program cycle for the function table proper to reach a steady-state condition, the two-digit argument is transmitted to the decade counters. From zero to four pulses are then added into the units decade to give the value of the function or any of the four neighboring function values (see the argument shifter circuits, Drawing PX-7-117). In addition to saving tubes, this arrangement has the advantage that the argument need not come from the adjacent accumulator."

(F18) Shaw supervised the drafting of the electronic design of the function table unit. Most of the drawings were completed and checked by Shaw during September, October, November of 1944. He then supervised the construction of three copies of the function table unit. After they were constructed, he carried out tests on them and supervised the modifications needed to make them operate correctly and reliably.

(F19) Summary of Shaw's contributions to the function table unit: Shaw completed the conception of this unit. Starting with the general design principles of Eckert and Mauchly, Shaw worked out the logical and electronic design of the function table unit. This included experimental work with different tube types to find suitable vacuum tubes to drive the function table resistor matrix and to use as its output gates. Shaw supervised the drafting of the function table unit and the wiring of three copies of it. He carried out tests on these three function table units and supervised the modifications needed to make them operate correctly and reliably.

(F20) Summary of my contributions to the function table unit: I invented the dynamic method of shifting used in the function table unit. This led to much simpler circuits and fewer voltage levels than the static shifting circuits originally planned. My analysis of the parasitic signals in the function table resistor matrix led to an improvement in the design of the table and its associated circuits, greatly increasing the reliability of this part of the function table unit.

MASTER PROGRAMMER

(P1) I invented the fundamental organization of the master programmer. This unit was to supervise the program controls of the other units, so to understand it one first needs to understand these "local" program controls.

(P2) Each of the ENIAC computing units (accumulators, multiplier, function tables, divider square-rooter) and each of the input-output units (constant transmitter and printer) had its own local program controls. A program control operated in response to a program pulse received over a program trunk wire. When a program pulse went into a program control it flipped the flip-flop of that control. The flip-flop would in turn activate the gate circuits of the unit, thereby causing the unit to execute the instruction set on the switches associated with that program control.

(P3) There were two main types of program controls: transceivers and receivers. A "transceiver" operated in conjunction with a counter so it could be used to direct a process which took more than one addition time; at the end of its operation the transceiver sent out a program pulse which could be used to initiate the next instruction of the program sequence. A "receiver" stayed on for only one addition time and did not produce a program pulse output. These local program controls provided facilities for setting up what are today called "sub-routines." Besides the program control unit

itself (transceiver or receiver), there were associated switches and terminals for program pulses. Program controls could be interconnected by means of program cables and program "trays" (trunks of 11 wires which ran around the front of the machine).

(P4) To set up a sub-routine on the ENIAC the programmer selected the program controls to be used, set their switches so they would direct their units to perform the desired operations, and interconnected the program control input and output terminals so as to achieve the correct sequence of parallel operations. He also had to establish the correct interconnections of the digit inputs and outputs of the units involved by interconnecting them with digit cables and digit trays. The use of local program controls is illustrated by the following example.

(P5) Suppose that the ENIAC was being programmed to do a computation, and that one step of the computation consisted of adding the contents of accumulator 1 to the contents of accumulator 17. To instruct the ENIAC to do this operation the human programmer would make the following connections and switch settings. He would connect the program pulse output from a transceiver which directed the preceding step of the computation into the program controls of these accumulators, for example, into transceiver 5 of accumulator 1 and receiver 2 of accumulator 17.

These electrical connections would be established by means of program trays and program cables. The programmer would set the switches corresponding to these program controls so as to direct accumulator 1 to transmit additively and accumulator 17 to receive on digit terminal alpha (for example). Finally, the programmer would establish a digit connection from the add output of accumulator 1 to the alpha digit input of accumulator 17. The program pulse to direct the next step of the computation would come from transceiver 5 of accumulator 1.

(P6) In this way one could program the ENIAC to perform a sub-routine or sequence of operations, such as those needed to accomplish a single step of a numerical integration. To solve a complete problem, such as computing a single trajectory of a shell, it was necessary to execute this and other sub-routines, each a certain number of times, and in a certain order. Moreover, the number of times a sub-routine was executed or the order in which sub-routines were executed might depend on the numbers being computed. For example, we might want the ENIAC to stop integrating a trajectory when the shell had reached the level of the ground.

(P7) This last requirement would be accomplished today by means of a conditional or branch instruction. We had planned to accomplish it by using sign pulses from an accumulator and converting them into program pulses. Suppose accumulator 11 holds the height (y) of a shell, and control is to be shifted from one sub-routine to another when y becomes negative. Then the add output from the plus-minus unit (PM) of accumulator 11 would not emit any pulses when y was zero or positive but would emit nine pulses when y was negative. These nine digit pulses could be taken to a "dummy" transceiver to produce a single program pulse. Hence each time a branch instruction was to be executed, accumulator 11 would be instructed to transmit additively, and if y was negative a program pulse would be emitted from a certain terminal.

(P8) When we were designing the accumulator, the high-speed multiplier, and the function table unit, we intended to have a separate central program control unit to perform this supervisory function automatically. However, we had given very little thought to how this unit would operate. I recall going to John Mauchly's home one Sunday to discuss with him and Pres Eckert various basic problems of ENIAC design that yet had to be thought about and solved. One of these was the question of how to design the central program control unit, which we decided to call the "master programmer."

(P9) After this discussion I thought about the problem and invented a solution to it. The solution is best presented in terms of an example. Suppose a program was to consist of a single execution of sub-routine A, 50 executions of sub-routine B, 100 executions of sub-routine C, and then one execution of sub-routine D. There were then four program loops, each with a program input and a program output. The problem was to design circuits which could be used to combine these four sub-routines into a single program. Such circuits had to be sufficiently flexible to handle program composition in general.

(P10) My solution to this problem was to provide several master counters, each operating in conjunction with a group of auxiliary counters. Each master counter and its auxiliary counters would control a sequence of local sub-routines. The auxiliary counters had a distinct set of switches for each stage of the master counter, so the auxiliary counters could make a different count for each sub-routine.

(P11) The program was initiated by sending a pulse into the input of sub-routine A. The output pulses from all four sub-routines went into an input controlled by the master counter. The first output pulse would cause the master counter to move to stage two, corresponding to sub-routine B, and would also go to start sub-routine B. The outputs from B would be routed back to B until B had been executed 50 times, and then the master counter

would advance to the next stage and start sending pulses to sub-routine C. After C was executed 100 times the master counter would advance again, send a single pulse to sub-routine D, and finally give out a "finish" pulse.

(P12) Moreover, this master counter would be advanced one stage when it received a pulse as a special input, regardless of the state of the auxiliary counters associated with it. When a conditional transfer to the next sub-routine was desired, an accumulator and transceiver would be connected in the way indicated earlier, so that a program pulse would be emitted from that transceiver when the transfer was to be made. This program pulse would go directly into the master counter and advance it to the next stage, thereby causing the next sub-routine to be operative.

(P13) I discussed my proposed design with John and then with Pres and they accepted it, so it became the basic idea of the master programmer. The master counter just referred to was called a "stepper" and the auxiliary counters were called "decades." There were changes and improvements in the design, though I don't remember exactly what they were. They probably included the ability to switch decade counters from one stepper to another so as to provide more flexibility in associating decades with steppers. They probably also included the addition of direct inputs to decade counters, so these could be advanced by pulses which produced no return (output) pulses.

(P14) My design of the master programmer was conceived sometime between the middle of February and July 31, 1944. For the design is not described in our First ENIAC Progress Report (to December 31, 1943), finished about the middle of February, 1944. . But my design is described in our Second ENIAC Progress Report (January 1 to June 30, 1944) which was written about July 31, 1944 (Preface). The description occurs in Chapter IV, Section II ("The Master Programmer"), pages 35 and 37-39. It is stated at the beginning of Section II that "some of the work described in this section has been done since June 30, 1944."

(P15) Shaw carried out the logical and electronic design of the master programmer. He then supervised the drafting and construction of the master programmer. Most of the drawings were finished, and checked by Shaw, in the last three months of 1944. After the master programmer was constructed, Shaw programmed it, tested its operation, located errors, and supervised the necessary circuit corrections and modifications.

(P16) Summary of my contributions to the master programmer: The master programmer was to govern, in an automatic manner, the subroutines set up on the local program controls of the ENIAC units. Mauchly, Eckert and I met one Sunday to discuss some basic design problems which had not yet been solved. One problem was: how should we design the

master programmer so it would perform this supervisory function automatically? After the meeting, I thought about the problem and invented the fundamental organization of the unit. A sequence of local sub-routines was to be governed by a master counter operating in conjunction with a group of auxiliary counters. We later called the master counter a "stepper" and the auxiliary counters "decades." A group of decades had associated with it a distinct set of switches for each stage of the stepper, so the group of decades could make a different count for each sub-routine.

(P17) Summary of Shaw's contributions to the master programmer: Shaw completed the conception of the invention of this unit. Starting with my general design plan, he worked out the logical and electronic design of the master programmer. He supervised the drafting, wiring and testing of it, and also the modifications needed to make it operate correctly and reliably.

DIVIDER AND SQUARE-ROOTER

(D1) The divider was the last ENIAC unit to be designed and constructed, though its general mode of operation was decided on by Eckert and Mauchly fairly early. Division was to be accomplished by repeated subtraction, with numerator, denominator, and quotient being stored in accumulators. The denominator was to be shifted back and forth between two accumulators; this made it unnecessary to build shifting circuits (like those used in the multiplier to shift the partial products). Thus, in contrast to the high speed multiplier, the divider was not to perform many arithmetic operations itself, but was to be mainly a control unit, controlling the operations of various accumulators. Later it was decided to have the unit also do square-rooting, which can also be accomplished by a process involving repeated subtraction. The name of the unit was then changed to "divider-square rooter."

(D2) I was given responsibility for the design of this unit. Chuan Chu, who had recently joined the ENIAC project, was assigned to help me. He worked out the logical and electronic circuit design under my direction. The actual design turned out to be quite complicated. This resulted from the fact that there were many different things that the divider square-rooter might be doing at each step of its operation. To show this, I will explain the division process in more detail.

(D3) For division, the numerator and denominator were each stored in designated accumulators, and an accumulator was provided to store the quotient. The divider square-rooter sensed the signs of the numerator and denominator and acted on the basis of this sign information. Assume, for example, that both numerator and denominator were positive. The divider square-rooter ordered the denominator subtracted from the numerator until there was an overdraft, and for each such addition sent a "one" to the quotient accumulator in the correct decimal position. The divider square-rooter then shifted the remainder (i.e., the balance left in the numerator accumulator) one place to the left by ordering it sent to the shift accumulator (over a cable with shifted wires) and returned.

(D4) This process was then repeated, except that now the divider square-rooter ordered the denominator added into the numerator accumulator, and sent minus one to the correct decimal position of the quotient accumulator. This alternate subtraction and addition of the denominator made it unnecessary to restore the numerator after overdraft, as is required in the usual form of division by repeated subtraction. I think this idea came from John Mauchly. It reduced the time required for division and simplified the circuits which controlled division. The divider square-rooter directed a similar process for square-rooting.

(D5) The divider square-rooter had a unique program control feature, not used on the accumulator, multiplier, or function table units. This was a program interlock. As I recall, Pres Eckert suggested that we design the program controls of the divider square-rooter to include this feature. When the programmer set up programs on the other units just mentioned, he always knew how many addition times they would take to perform the instruction he gave. This was not so for the divider square-rooter, for its operation time depended on the numbers involved. To make it possible for the ENIAC to do other operations in parallel with division or square-rooting, each program control on the divider square-rooter had two inputs; the normal input (which started division or square-rooting) and an interlock input. When its interlock feature was used, the program control did not give out its output pulse until the operation was completed and a pulse had been received on its interlock input.

(D6) After Chu worked out the logical and circuit design of the divider and square-rooter, he supervised the drafting and wiring of the unit. Finally, he tested it and corrected its defects. In these activities, he worked under my general direction.

(D7) Summary: The general mode of operation of the divider and square-rooter was decided on by Eckert and Mauchly. Under my direction, Chuan Chu worked out the logical and electronic design of the unit, supervised the drafting and wiring of it, tested it, and corrected its defects.

CONSTANT TRANSMITTER, PRINTER AND CYCLING UNIT

(C1) The constant transmitter and the printer were the input and output units, respectively, of the ENIAC. Both units used electromagnetic relays as well as vacuum tubes. The constant transmitter received signals from an IBM card reader, and the printer transmitted signals to an IBM card punch. Shaw did much of the design work for these units, following the general pattern of design developed by Eckert and Mauchly. Shaw was in charge of testing and debugging at least the electronic parts of these units.

(C2) I definitely recall that Shaw worked on the input-output part of the ENIAC, that is, on either the constant transmitter or printer or both. However, I had much less to do with these units than with the rest of the ENIAC system. In the preceding paragraph I rely on Shaw's own statements concerning the extent of his contributions to the input-output units. In his letter of October 31, 1964 to Sharpless, Yuter, and me (PX 18, 580), Shaw says "The constant transmitter, including the electronic circuitry associated with the data circuits of the card reader, was my next project, and proceeded fairly quickly as a result of experience gained with the function table and master programmer design. Finally, I designed the data circuits for the card punch, which presented no particular problems." The card punch was an IBM machine which operated in conjunction with the printer. Later in

the same letter, Shaw continues, "After construction of the function tables, master programmer, and other units for which I was responsible, I carried out tests on the completed units, making various small modifications which proved necessary to assure proper and reliable operation."

(C3) The cycling unit was the basic electronic clock of the ENIAC system. We planned to operate the ENIAC at a basic pulse rate of 100,000 pulses per second (or 10 microseconds per pulse), though we designed it so that it would also operate correctly at a slower rate. Each pulse was about two microseconds wide. The cycling unit was to provide a basic "frame" of pulses and gates. The frame was changed during the course of and as a result of our research. In final form it consisted of nine different sequences of pulses and one longer signal, the "carry-clear gate", which lasted seven pulse times (70 microseconds). Each of these nine pulse sequences and the carry-clear gate were sent around the ENIAC on separate wires, from which they could be taken by the various ENIAC units.

(C4) The relative timing of these signals was very important for the correct operation of the ENIAC. For the ENIAC was a highly parallel machine, in which many units operated at the same time, sending numbers and program pulses to each other. The cycling unit signals synchronized these operations. One of our fundamental design rules was to use the cycling unit pulses wherever possible. Pulses were not to be generated

from within a unit; when a pulse was needed an appropriate pulse from the cycling unit was to be gated. This prevented the repeated degeneration of pulses in size, shape, or phase, and contributed to the reliability of the ENIAC. I think this rule was due mainly to Pres Eckert.

(C5) The temporal operation of the ENIAC was organized on the basis of an "addition time" or the time required to perform a single addition. This consisted of twenty pulse times: ten pulse times to process a single decimal digit and ten more pulse times for handling carry-over, transferring program signals, setting up switching circuits, etc. Hence, a normal addition time lasted 200 microseconds. If the basic pulse rate was decreased, an addition time lasted longer. Each addition time, the cycling unit repeated the same frame of nine pulse sequences and the carry-clear gate.

(C6) Besides its normal mode of operation, the cycling unit (and hence the whole machine), had three other modes of operation. These were useful when the machine was not operating properly or the program was incorrect. In the first mode, the basic pulse rate was less than 100,000 pulses per second. The machine might not operate correctly at the standard rate, but for electrical reasons might operate correctly at a slower rate, in which case this mode was used.

(C7) The cycling unit could also operate in a "one-addition time" mode and a "one-pulse time" mode. In these modes, whenever the operator pushed a button, the machine would perform for one addition time (or one pulse time) and then stop. An operator or maintenance man could then examine the state of the machine by reading neon lights attached to counters and flip-flops or by measuring direct-current signal voltages at crucial places in the circuits. The one-addition and one-pulse time modes of operation were very useful in finding circuit mistakes and faults and also in locating errors in the program.

(C8) When Shaw and I met with Yuter in early August, 1964 to discuss our contributions to the ENIAC, Shaw said that Sharpless conceived the one-addition time and one-pulse time modes of operation of the cycling unit. I do not remember this, and now wonder if Shaw remembered this correctly. These two modes of operation were described on pages IV (17) and IV (18) of our first progress report, "The ENIAC (Electronic Numerical Integrator and Computer) Volume I, A Report Covering Work until December 31, 1943; submitted in accordance with Contract #W-670-ORD-4926." This report was written about the middle of February, 1944, and I do not recall whether Sharpless had worked on the cycling unit by that time or not.

(C9) In all modes of operation, special as well as normal, the cycling unit had to produce pulses of standard size, shape, and strength so that the units would operate correctly. Moreover, these signals had to be strong enough to pass around the whole machine with little attenuation and loss of shape, so they could drive the circuits of the various units.

(C10) Two prototype accumulators were designed and constructed during the first year of Project PX. To test them we needed a small prototype cycling unit. This was built by Sharpless, working closely with Eckert. It operated successfully and the two accumulators and it were tested in the summer of 1944. The design of the accumulator was modified considerably as the result of this test. Valuable experience was gained with the cycling unit, but we recognized that much work would have to be done before we would have a cycling unit adequate for the whole machine. For one thing, the power requirements for the frame of pulses and gates would be much greater for the whole machine. Moreover, as we gained more experience we changed the specification of the frame of pulses and gates to be produced by the cycling unit.

(C11) Sharpless built a full-scale prototype of the cycling unit and after considerable experimental work, got it working. This worked well enough to test the whole ENIAC. On the basis of what he learned from this full-scale prototype, he designed the final version of the cycling unit. In

developing both of these units he was guided by Eckert, and Eckert sometimes worked on the cycling unit when Sharpless was not there. But there were long periods when Sharpless worked without consulting Eckert. Sharpless was also responsible for the final testing of the cycling unit and for making it work correctly.

(C12) Summary of Shaw's contributions: Shaw completed the conceptions of the constant transmitter and the printer, following the general patterns of design developed by Eckert and Mauchly. Shaw was in charge of testing these units and correcting their defects.

(C13) Summary of Sharpless' contributions: Sharpless, working with Eckert, completed the conception of the cycling unit. This unit was the basic electronic clock of the ENIAC. It provided nine different sequences of pulses and one gate; these signals were used to synchronize the operation of the different ENIAC units. Sharpless worked out the electronic design of the cycling unit, supervised the drafting and wiring of the unit, experimented with it, and modified it so that it worked correctly.

Arthur W. Burks

ARTHUR W. BURKS

Above sworn to and subscribed before me this 1st day of February, 1972.

Alan Henderson
Notary Public

OFFICIAL SEAL
ALAN HENDERSON
NOTARY PUBLIC-CALIFORN
SANTA CLARA COUNTY
My Commission Expires Mar. 5, 1

202 Junipero Serra Blvd., Stanford, Calif. 94305

A

UNIVERSITY OF PENNSYLVANIA
PHILADELPHIA

MOORE SCHOOL
OF ELECTRICAL ENGINEERING

Harold Pender, *Dean*

September 27, 1944

Dear Dr. Burks:

We expect to make application for U.S. patents on all novel apparatus and their arrangements of any value to an electronic or high-speed electromechanical computing machine. We may also patent uses to which the instrumentations may be put other than computing uses. However, our main purpose will be to protect the government's interest in the ENIAC and any of its future computing devices or associated equipment.

The patents must be taken out in the name or names of the inventor or inventors in order to be valid. In order that we fulfill this requirement and so that we may not have any future misunderstandings, I would appreciate it if you would write out any claims you feel entitled to and submit them to Dr. Mauchly or myself.

This, of course, only covers developments to date, so that if you do not have any such claims at present, please give us a statement to this effect in the assurance that this does not affect your future position.

Very truly yours,

J. Presper Eckert Jr.

J. P. Eckert, Jr.

Dr. Arthur W. Burks
Moore School

I have no such claims at present.

Arthur W. Burks

Def Ex 29 (2 sheets)

Copy of Letter to J. P. E. Jr

June 4, 1946

Dear Pres,

I am writing this to cover a couple of matters in the patent set up

I mentioned to you previously in a letter that I felt I had some interest in the mercury line, namely, the business of polishing the crystal. I note that this point is specifically covered in claim 82 of the patent application in your and John's names which covers all sorts of delay lines, both electric and acoustic, and their applications. In addition, under item 5 of "Outline of Patent Application Material" is a note about clearing counters to selected points by gating from a stage of the ring, as in the multiplier programming. This too I believe is my idea.

I am writing this not in the spirit of annoyance but rather in the hope that

the engineers on both PX and PY may soon have a meeting to discuss ways and means of definitely establishing patent rights and doing something about the oft mentioned patent pool. If you want to talk these matters over with me personally I shall be very happy.

Sincerely

Kirk

shut 2 Z Dy & 29

Note: ΔEx 39

Mar 10, 47

In reply to letter from J.P.E Jr. of 27 Sept '44 I wrote saying in effect that I felt I had certain interests in the patents which might arrise from work on PL and PX. I stated that I could make no definite claim until specific patent applications were made out.

No copy of this letter is in my possession - at that time engineers were not provided with desks or facilities for keeping personal or ~~for that matter~~ project records.

I received no written reply to my letter of Mar 4, 1946. Conversation with Pres only got to the point of his denying that I had contributed either of the ideas. It being a matter of my memory versus his I let the matter drop with the understanding

that details be worked out later.

C. H. Hayden

July 24, 1964

Mr. Robert F. Shaw
569 Bayville Road
Locust Valley, L.I., N.Y.

Re: ENIAC

Dear Bob:

In connection with your investigation to determine whether you may be a joint inventor of the ENIAC, the following quotation may be of interest. It is from De Laski & Throop v. William R. Throop & Sons, 218 Fed. 458, 464 (1914), aff'd. 226 Fed. 941 (3 Cir. 1915).

> "In order to constitute two persons joint inventors, it is not necessary that exactly the same idea should have occurred to each at the same time, and that they should work out together the embodiment of that idea in a perfected machine. The conception of the entire device may be due to one, but if the other makes suggestions of practical value, which assisted in working out the main idea and making it operative, or contributes an independent part of the entire invention, which is united with the parts produced by the other and creates the whole, he is a joint inventor, even though his contribution be of comparatively minor importance and merely the application of an old idea. (Citing cases.)"

Sincerely,

SCY:d
cc: Mr. Kite Sharpless

PX17534

July 24, 1964

Mr. Robert F. Shaw
569 Bayville Road
Locust Valley, L.I., N.Y.

Re: ENIAC

Dear Bob:

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Sincerely,

SCY:d
cc: Mr. Kite Sharpless

1413 Morton Avenue
Ann Arbor, Michigan
August 11, 1964

Seymour Yuter
407 Cedar Drive West
Briarcliff Manor, New York

Robert Shaw
Bayville Road
Locust Valley, New York

T. K. Sharpless
629 Walnut Lane
Haverford, Pennsylvania

Gentlemen:

I give below a list of contributions that Bob, Kite, and I made to the ENIAC. This is the list that Bob and I drew up last Sunday, except that in my own case I have thought about the matter further and added to my list. I thought it desirable to do this since I will be out of the country until September 5. Bob should think further about what his contributions were. In Kite's case the list gives only what Bob and I recall and is meant primarily as a stimulus to Kite's memory.

Hereafter, the notion "completion of concept" includes both logical and electronic design, supervision of construction and testing, and deciding on the modifications to be made in order to make the equipment operative. For example, when the multiplier was first operated I discovered that the resistor matrix used as a multiplication table did not take account of

the fact that we were using a complement system at that stage of the circuitry, and I saw that the matrix was rewired.

It should be noted for the record that the basic concepts and problems were due initially to Eckert and Mauchly, and that Eckert, and to some extent Mauchly, directed the work of Shaw, Sharpless, and Burks.

Contributions of A. W. Burks

Completion of the concept of the multiplier, using the results of Sharpless's experimental work.

Completion of the concept of the divider-square-rooter; directed Chuan Chu, who carried out many of the details.

Master programmer: suggested original idea of using auxiliary counters or groups of counters for combining subsequences into complete programs. The general problem was raised in a private discussion of various problems concerning the development of the EMIAC; this discussion was held by Eckert, Mauchly, and me at Mauchly's home one Sunday. After the discussion I thought about the problem and came up with this idea, discussing it first with Mauchly and then with Eckert.

Accumulator: One day I was going over the circuit diagram of the accumulator to see if it would work. I am not sure when this was, but it was probably after the design of the accumulator used in the two-accumulator prototype was frozen. In thinking about the operation of the accumulator the following

occurred to me. The accumulator gate circuitry directed the operation of the accumulator. This gate circuitry was in turn controlled by any one of a number of transceivers or receivers. The mechanism of this control was disjunctive, with a resistor in the gate circuitry through which current could be drawn by any transceiver or receiver; this current would in turn operate a vacuum tube in the gate circuitry. The number of transceivers and receivers was significantly large; in the end there were eight of the former and four of the latter, though these numbers may not have been frozen at the time. It occurred to me that the leakage current through this common resistor of the gate circuitry might be sufficient to operate the accumulator when no control (transceiver or receiver) was on. Indeed, in terms of the design criteria we employed, the circuit was not safe. The problem was worse in the multiplier, where there were twenty-four transceivers. I mentioned this problem to Mauchly, who mentioned it to Eckert, and Eckert agreed with me. The problem was solved by putting a bias voltage on the resistor of the gating circuitry so that even if the leaking current were maximal the accumulator (or multiplier) would not operate unless a transceiver or receiver were on. I think this general technique may have been used elsewhere, but I am not sure. This incident is rather vivid in my mind for the following reason. I had earlier worked on the magnetic coil for mine sweeping and on the parabolic antennae for radar. I had also worked on counters for the ENIAC. But this accumulator suggestion was the first electronic idea of importance that I had had.

I also worked on the problem of what complement system to use in the ENIAC. This involved the multiplier as well as the accumulator, of course. It also involved the divider, but we didn't worry about that unit at the time we selected the complement system for the machine. We originally decided on the tens complement system. Then we took a trip to Aberdeen to discuss the ENIAC. I was along, and Mauchly was, as I recall. I think we had discussions with Cunningham of Aberdeen. We learned of the nines complement system, which was used in some IBM machines. There were discussions and conferences at the Moore School after we returned, and we decided to use the nines system, though this involved changing diagrams, and perhaps wiring. I continued to think about the problem and work out examples. I discovered that the nines system, as embodied in our proposed design of the moment, would lead to errors when our round-off system was used. There were further conferences, mainly among Eckert, Mauchly and me. We decided to return to the tens system. It is possible that our treatment of round-off was different after the return from what it had been before, but I am not sure.

Function tables suggested the use of a dynamic method of interpolation instead of the static method of shifting as used in the multiplier.

At one stage, Sharpless and I were responsible for the coordination of the entire system to insure compatibility. We checked the logical and electronic design of most of the units to make sure they were correct internally and to make sure that

the units interacted correctly, both logically and electronically. We made various suggestions for change of design. As I recall it, Shaw and I went over the function table together, and Sharpless and I went over the rest of the units together.

I had the first program drawn up for the ENIAC. The student who did it was Donald Hunt. He now teaches electronics in New York, at Brooklyn Polytechnic Institute, I believe.

I participated in the development of the overall system design. There were many sessions with all of the engineers, and I participated in many discussions with Eckert and Mauchly. For example, I participated in discussions and decisions about the pulse sequences of the cycling unit. A frame of pulses had to be designed that would be satisfactory for the accumulator, the multiplier, and the function table. Topics discussed were: how much delay was needed for carrying in the accumulator in the worst case of twenty decades, how much delay was needed for the set-up of the multiplier shifting circuits, how much delay was needed for set-up of control gate circuits after the program pulse was received by a receiver or transceiver, etc. I studied the multiplier circuits with this in mind and made suggestions, and perhaps I studied other units also.

Contributions of J. K. Sharpless

Completion of concept of cycling unit, including experimental work on two preliminary models and the final model. The

first model was the cycling unit of the two-accumulator prototype, and Sharpless worked on this model when it was part of this two-accumulator computing system. Conceived of the one pulse and one addition mode of operation of the ENIAC.

Built and experimented with prototypes of the function table and the shift circuits of the multiplier.

Contribution to counter control: suggested use of signal derived from a particular stage of a counter to control its clearing. Perhaps suggested the circuitry used for clearing a decade selectively to either 0 or 1.

Worked on the coordination of the entire system to insure compatibility. See the description of this item under Burks.

Played an active role in testing and completing the two-accumulator prototype.

Perhaps worked on the initiating unit.

Contributions of Robert F. Shaw

Completion of the concept of the function table. Built, tested, and modified prototypes of parts of circuitry. Supervised testing of tubes to determine suitability and develop standards for pile-ups of circuits.

Completion of the concept of the master programmer.

Did card reader pulse circuitry and logical design. Did constant transmitter circuitry and logical design. Did electronics of the punch circuits.

Participated in some discussions of the use of the function table as a programming device.

Bob and Kite should use these lists to think out their contributions in further detail and, in Kite's case, possibly to add other units he worked on. I will continue this letter now with some materials that are relevant to our case.

Shaw, Burks, and Sharpless approved and/or checked many drawings, both circuit drawings and block diagrams (logical drawings). They also wrote progress reports. Burks edited most reports. Adele Goldstine wrote the final report; as far as circuit design and logical design are concerned, she just used the earlier reports. The application for the ENIAC patent seems to be mostly a compilation of these reports, except of course for the claims. These claims were clearly written with the EDVAC, and von Neumann's use of the ENIAC function table for automatic programming, in mind.

The ENIAC was a large system and its design and construction were a team effort. The characteristics of the whole system were dependent on the characteristics of its units, and vice versa. Hence, in designing a unit one had to keep in mind the whole system. The rules governing the whole system had to be held in mind since the system was constantly changing, and was developed over a long period, and the drawings lagged behind the design and sometimes even the construction. There were

many cases where we changed a design on the basis of verbal discussions, perhaps had the girls change the wiring, and only later updated the drawings. There were few if any cases where we were given completed drawings to work with. There were no cases where we were given completed drawings of whole units (e.g., accumulator) or even of substantial parts of whole units (e.g., the multiplier shift circuits) and told to build and test from there.

I made more than one technical trip to Aberdeen with others (principally Eckert and Mauchly) to discuss technical arrangements of the ENIAC. There were also visits from Cunningham to the Moore School. I participated in discussions with Mauchly, Rademacher, and Goldstine concerning Rademacher's research into round-off and truncation errors. This problem was given to Rademacher in the hope that we could base our decision on the number of decimals needed on his researches, but his results came too late for that.

I had very little notion of what ideas were or were not patentable at the time. I would have thought that the use of vacuum tubes to realize truth-functions was in principle patentable. A paradigm case of what I would have thought patentable on the ENIAC was the use of the cathode resistors (1640 ohms and 19.4K in Fig. 1 of my IRE article) of the decade ring counter in such a way as to deter two flip-flops from being "on" at once.

My wife Alice (313-66-2-9630) has my itinerary, and I am sending Seymour a list of my European addressees.

Sincerely yours,

Arthur W. Burks

569 Bayville Road
Locust Valley, N. Y. 11560
October 31, 1964

Dr. Arthur W. Burks
1413 Morton Avenue
Ann Arbor, Michigan

Mr. T. Kite Sharpless
629 Walnut Lane
Haverford, Penna.

S. C. Yuter, Esq,
485 Lexington Avenue
New York 17, N. Y.

Dear Art, Kite, and Sy:

After rather lengthy delays I have finally put together on paper my recollections of the development of the ENIAC and the contributions made to it by thew various people involved, with particular reference to those of Art, Kite, and myself.

My own connection with the ENIAC project began about the middle of September, 1943. At that time Harry Gail and I joined the project after having taught in a Navy Department school for inspectors of radio equipment. To the best of my recollection the project at that time was still in its very early stages, with investigations in progress on design of reliable flip-flops and ring counters, and investigation of suitable tube types for these and for related circuits such as amplifiers and gates. Work was also being done on design of pulse drivers which would be suitable for a cycling unit to time the entire system. I believe the work on rings and flip-flops was being done mostly by Frank Mural and Jack Davis under Pres Eckert's direction, and the work pn pulse drivers by Kite.

My first work, along with Harry Gail and with some assistance from Joe Chedaker (whose duties as purchasing agent later occupied his time to the practical exclusion of technical work), involved the design and construction of test equipment such as pulse generators and oscilloscopes.

Some time during this period I recall that Kite was beginning to develop circuits for the multiplier, and built prototypes (which I seem to remember were at the time hopefully to be used in the final machine) of the multiplication table and shift circuits. As work on the rimgs and flip-flops progressed, Frank and Jack proceeded to put the resulting circuits together with others, under Art's and Pres's direction, into what finally became the accumulator.

Meanwhile Kite, also working with Art and Pres, further developed the cycling unit, and whenever he had time continued work on the multiplier. As an important test was to be made using two accumulators and a cycling unit, the latter got priority over the multiplier.

Upon completion of the test equipment, my own efforts shifted to design of the function tables. Kite's experience with the multiplication table proved helpful here, but it was necessary to go considerably further in circuit design, since much larger resistor matrices were involved. Therefore I carried out an investigation of various tube types to determine suitable driving circuits for the tables, making ~~xxxxx~~ tests on 6L6 tubes and later on 807s, as they had essentially similar characteristics to those of the 6L6 but were designed for higher voltages.

Having settled on 807 drivers (particularly in view of the fact that ny tests had shown that their screen control characteristics made them adaptable to screen gating), and having adopted 6AC7 tubes for output amplification (because of their short grid base and high perveance), I had to design suitable overall circuits. Because of the large attenuation through the matrix, and the high distributed capacitances which made pulse techniques and hence capacitively coupled circuits unsuitable, I had to design rather large pile-ups of DC-coupled circuits, as a result of which the function table had the widest range of DC power supply voltage requirements in the ENIAC, and several supply voltage levels had to be added to those reuired by other units. The idea of the use of bias voltages to counteract the effects of leakage currents, suggested by Art in connection with the accumulator, proved helpful in the function table, which also required a careful analysis of the effects of parasitic signals in the matrix. I recall making such an analysis to * determine the worst combination of switch settings, so that the worst case could be provided for.

I was able to adopt several standard units (transceivers, repeater, etc.) for function table control; these had meanwhile been developed for the accumulator. Kite"s experience with the multiplication table proved helpful, as previously noted, and for a while I was hopeful that I could use his shift circuit designs in mechanizing the function table interpolation feature. Tying these into the system, however, proved a bit troublesome, and Art came up with a very ingenious suggestion for dynamic shifting, which involved the offsetting of connections by two columns in tying the argument register outputs to the matrix, so that by selecting anywhere from zero to four shift pulses and feeding them into the argument rings after the argument was stored, it was possible to obtain any of the functions f(x - 2), f(x - 1), f(x), ~~f(xxx+2)xxxxxf(xxx+2)~~.f(x + 1), or f(x + 2). This appreciably simplfied the circuits.

* I recall checking this. AWB

After completing the function table design and turning it over to production, I went on to the design of the master programmer, using the broad concepts laid down by Art, again with Pres offering helpful suggestions. As a high degree of flexibility in associating decade counters with steppers was desired, it was necessary for me to work out in detail the switching circuits and switch designs which would produce the desired results, always taking into account such factors as the effects of varying loads on the tubes. In order to handle this situation the master programmer used what was to the best of my memory the only multiple coincidence (parallel-tube) gating circuit in the ENIAC; as these circuits were DC-coupled, they led to they led to DC voltage pile-ups similar to, but somewhat less extensive than, those in the function tables. Thus I was able to apply techniques developed in the function table design and fit the circuits into the already-established pattern of power supply voltages.

The constant transmitter, including the electronic circuitry associated with the data circuits of the card reader, was my next project, and proceeded fairly quickly as a result of experience gained with the function table and master programmer design. Finally I designed the data circuits for the card punch, which presented no particular problems.

Meanwhile the two-accumulator system had been thoroughly tested and led to certain modifications in units such as transceivers which were also used elsewhere, and changes and additions in power supply voltages. Also, Kite had completed the multiplier design and turned it over to production. With several people working in parallel it became quite important to assure overall compatibility of the system. This job fell to Art and Kite primarily, although I worked with Art in checking over the function table and other circuits. I became involved in another way with the compatibility survey through follow-up of changes and corrections, partly in production but especially in having drawings brought up to date. As I had become familiar with practically all the basic circuits in the system in the course of my design work, I found it easy to spot errors and omissions in drawings and have them corrected; thus my initials appear on a majority of the circuit drawings, either on revision notes or on final checks or approvals, or both.

The divider unit was started rather late in the program, with Chuan Chu working on the design under Art's direction.

After construction of the function tables, master programmer, and other units for which I was responsible, I carried out tests on the completed units, making various small modifications which proved necessary to assure proper and reliable operation. Kite did the same with the final model of the cycling unit, which had to be in operation before other units could be tested, and later with the multiplier and initiating unit. The testing of the function tables and especially of the master programmer required me to set up test programs in which these were used in conjunction with accumulators.

As soon as a reasonable number of units were in operation, Art, John Mauchly, Herman Goldstine, and others also began to set up test programs to check the ability of the system to perform its intended operations. We all discussed certain of these programs from time to time, and among other things the use of data signals to control the program was discussed and tried, leading naturally to use of the function table for the same purpose.

Each of us wrote reports describing the construction and operation of the major units for which we were responsible, and Art edited and coordinated these reports (incidentally acquiring the nickname "Author" Burks). These reports became the basis for the final report, which in turn appears to have formed the basis for the specification and drawings of the ENIAC patent.

In compiling the above I found it easier to set down my recollections in the form of a brief history of the project, even though the contributions of the various people are not so neatly summarized as they are in Art's letter of August 11. I have gone through that letter carefully and find nothing in it to which I can take exception.

Best regards,

Bob

Robert F. Shaw

November 27, 1964

T. Kite Sharpless
629 Walnut Lane
Haverford, Pennsylvania

Robert Shaw
Old Poverty Road
Southbury, Connecticut

S. C. Yuter
485 Lexington Avenue
New York 10017, New York

Dear Kite, Bob, and Syl

I have studied Bob's letter of October 31 carefully. It jogged my memory and so I will make a few comments.

At the bottom of page one it is stated:

> As work on the rings and flip-flops progressed, Frank and Jack proceeded to put the resulting circuits together with others, under Art's and Pres's direction, into what finally became the accumulator.

My memories on this point are rather vague. I do recall working some on the accumulator at this stage, but I don't recall playing as strong a role as this formulation suggests. In any case, most of the direction must have come from Pres. I think he supervised the accumulator more closely than he supervised any other unit. It was the first unit to be designed, and there were to be far more of them than any other unit.

Page 2, paragraph 1, sentence 1: I don't think I ever worked on the cycling unit, in the sense of helping to design or construct the circuits; I did have a hand in the design of the frame of the cycling unit pulses.

Page 2, paragraph 1, sentence 2: As I recall it, Kite did very little work on the logical design of the multiplier after I entered the picture. He had done the experimental work on a cross-section of the proposed circuitry, from the places counter through the multiplier selector, the multiplication table matrix, the multiplicand selector,

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and the shifters. Someone had done design work on the multiplication table matrix. When I received this matrix design it was supposed to be correct, but I discovered when the multiplier first operated that this design did not provide nine pulses for the output corresponding to "zero". Since we were using a complement system at that stage, the case of "zero" output required nine pulses, not zero pulses.

The last two sentences of paragraph three on page two read:

> The idea of the use of bias voltages to counteract the effects of leakage currents, suggested by Art in connection with the accumulator, proved helpful in the function table, which also required a careful analysis of the effects of parasitic signals in the matrix. I recall making such an analysis to determine the worst combination of switch settings, so that the worst case could be provided for.

I recall checking Bob's analysis. The problem of finding the worst case was very much more difficult in the function table matrix than in the multiplier, because the multiplication table matrix was fixed, whereas the function table matrix varied with the switch settings.

With respect to the use of bias voltages to counteract the effects of leakage currents, I do not claim sole credit (or even major credit) for the solution of the problem, but I do claim full credit for discovering that there was a problem. An account of this occurs on pages two and three of my letter of August 11, 1964. When I discovered that there was a problem I mentioned it to Mauchly, who mentioned it to Eckert. I recall Eckert coming to see me and acknowledging that it was a problem. I do not recall what role I had in the solution. Pres probably thought about the problem before coming to see me; this was usually the way he worked. Whether John and I had come up with the solution already, I don't recall.

Part of the first sentence of page three reads:

> I went on to the design of the master programmer, using the broad concepts laid down by Art, again with Pres offering helpful suggestions.

My account is given on page 2 of my August 11 letter. My idea was to use groups of auxiliary counters for combining subsequences into complete programs. I do not recall the details, but I recall this much about it. I had a definite logical design which would work. The actual system of decoders and steppers was different; it was a variation on my idea, and, as I recall it, an improvement of my idea.

In the first paragraph of page three Bob states:

> ... the master programmer used what was to the best of my memory the only multiple coincidence (parallel-tube) gating circuit in the ENIAC; as these circuits were DC-coupled, they led to DC voltage pile-ups similar to, but somewhat less extreme than, those in the function tables.

The last part fits with my memory. Since I had the responsibility of designing the power supplies, I was familiar with all the voltage levels of the machine, and there were very many. The switches on the initiating unit provide for 8 x 11 (=88) different voltages, but the actual number may have been smaller. I recall working with Bob at one stage to see if we really needed the extra levels introduced by the function table, and concluding that we did, though our discussion may have led to eliminating a few levels Bob though he needed. In particular, the wide range of voltage levels we had was unavoidable.

My memory supports Bob's assertion that the master programmer led to DC voltage pile-ups similar to those of the function tables. But I am unable to confirm that this is so for the reason he gives, namely, that the master programmer used "the only multiple coincidence (parallel-tube) gating circuit in the ENIAC." I assume that the circuit he refers to is that of Figure 1, which is enclosed. But the multiplier circuit of Figure 2 seems to involve a greater pile-up.

Page four, paragraph one, sentence one: As mentioned on page five of my August 11 letter, I had Bob Gaunt draw up a connection diagram for an ENIAC program, probably for a ballistics trajectory. I believe some use was made of this large drawing, but I'm not sure. Adele Goldstine would probably know. I must have set up test programs for the multiplier, for I had full charge of testing that unit. I don't recall participating in the set-up of any full-scale problems on the machine. I think the girls under the direction of Adele Goldstine did most of that.

Sincerely yours,

Arthur W. Burks
Professor of Philosophy

AWB:dlw
Enclosures

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From sheet 91,
Fig. 73 D

From sheet 90,
Fig. 73C

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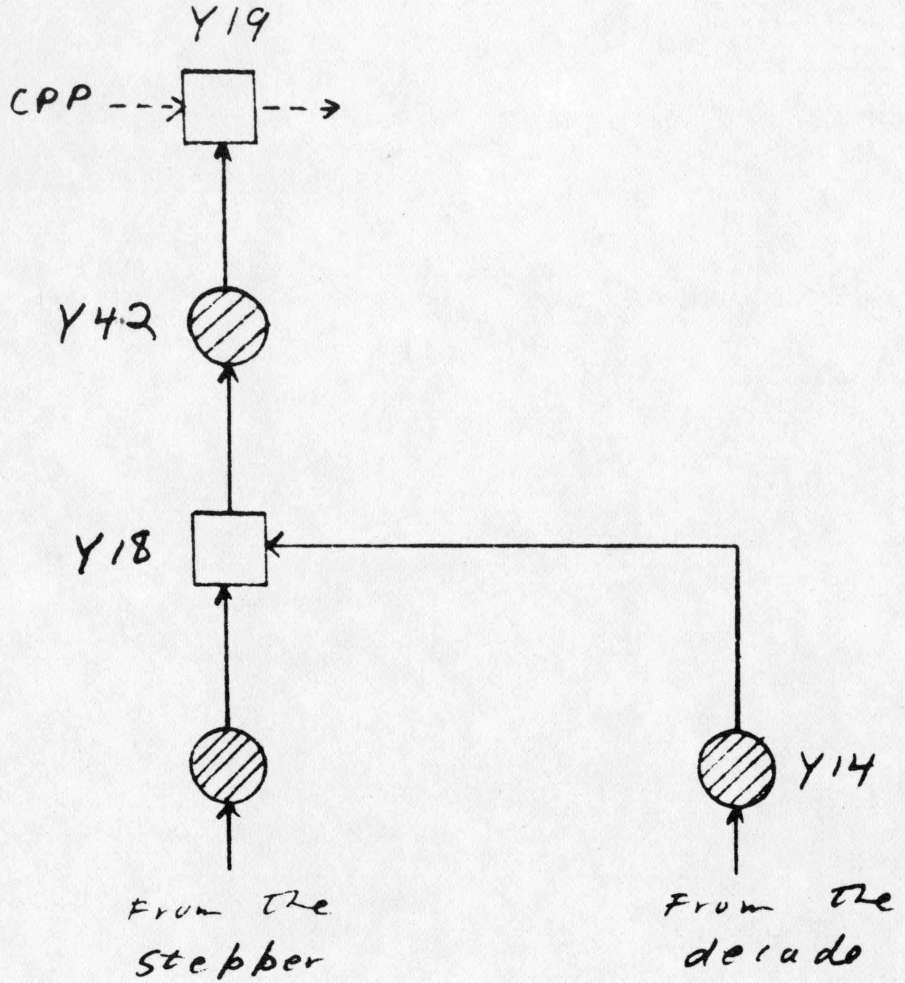
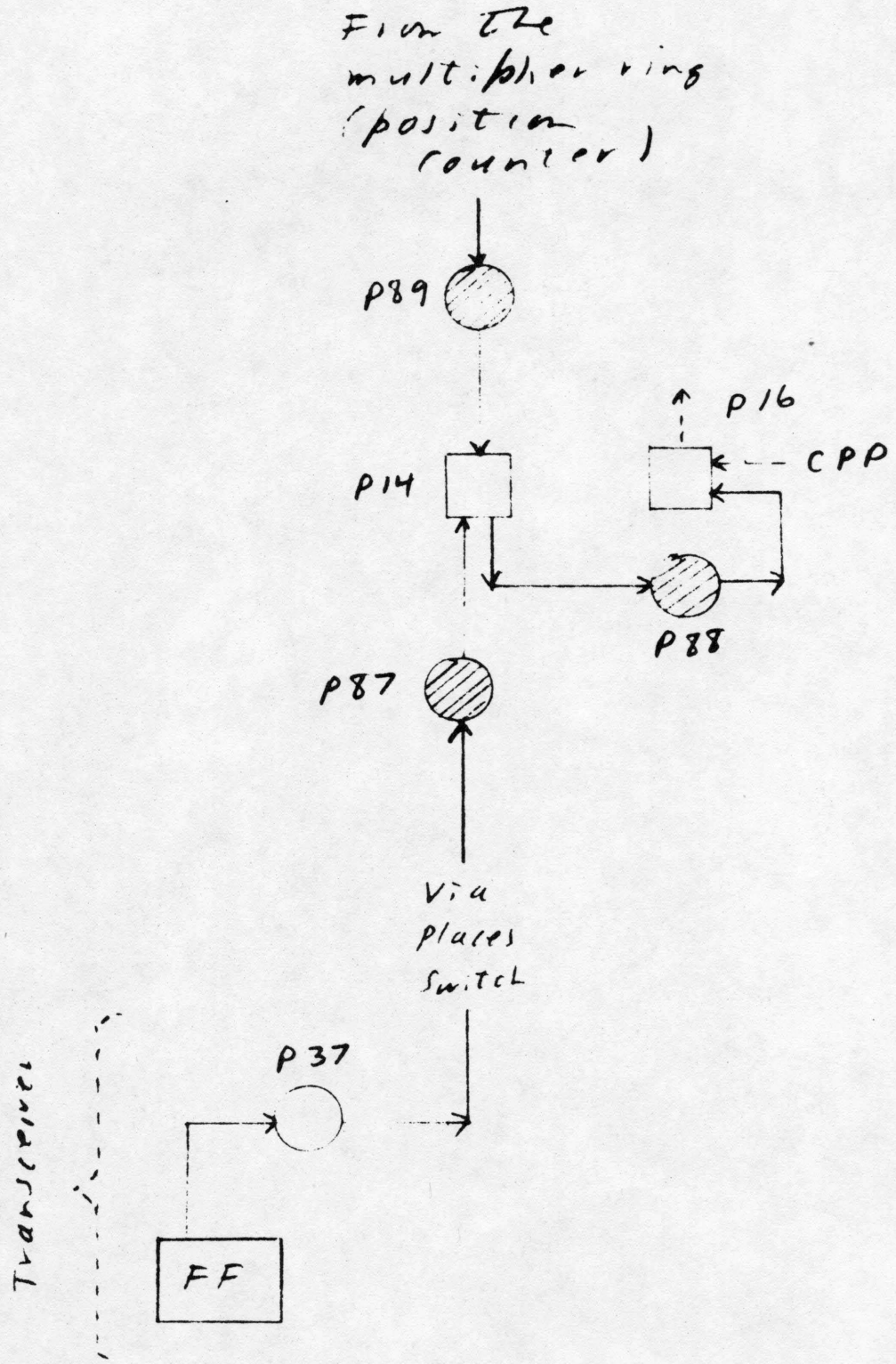


DC Gating Circuit of the Master Programmer

Figure 1

AWB



Sheet 41
Fig. 42B

Sheet 40
Fig. 42A

DC Gating Circuit of the Multiplier

Figure 2

PX 18832
AWB

My Copy #1

February 18, 1965

Dr. H. H. Goldstine
Thomas J. Watson Research Center
I.B.M. Corporation
P.O. Box 218
Yorktown Heights, New York

Dear Herman:

In my telephone conversation with you from Sy Yuter's house last summer, you asserted that Kite Sharpless, Bob Shaw, and I were joint inventors of the ENIAC. Kite, Bob and I would appreciate very much having a written statement from you to that effect.

Bob and I composed lists of the contributions that all three of us made to the ENIAC. These are contained in one letter by Bob (October 31, 1964) and two letters by me (August 11, 1964 and November 27, 1964). I am enclosing copies of these letters, since they may be of help in refreshing your memory concerning our work. If you agree with the substance of these letters, we would appreciate your saying that also.

Since the meaning of "joint inventor" is crucial in this matter, I am enclosing a copy of Yuter's letter to Shaw of July 24, 1964, which contains a relevant quotation.

Let me add my understanding of why Kite, Bob, and I are joint inventors of the ENIAC. The ENIAC was a joint team effort. John Mauchly and Pres Eckert gave us the general idea and raised many problems. We solved these problems in a non-obvious, non-routine way, as well as other problems which we formulated as the work progressed. Kite, Bob, and I are joint inventors because we completed the conception of the ENIAC; we did not merely reduce to practice the already completed concept of John and Pres. The notion of "completing the conception" includes logical and electronic design, supervision of construction and testing, and deciding on the modifications needed to make the equipment operative. Kite, Bob, and I completed the conception of various units and various aspects of the whole system to the place where technicians could carry out the rest of the design.

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Kite, Bob, and I would appreciate very much a written expression of your opinion that we are joint inventors of the ENIAC.

I look forward to seeing you February 27 or 28. Best regards.

Sincerely yours,

Arthur W. Burks

AWB:law

July 24, 1964

Mr. Robert F. Shaw
569 Bayville Road
Locust Valley, L.I., N.Y.

Re: ENIAC

Dear Bob:

In connection with your investigation to determine whether you may be a joint inventor of the ENIAC, the following quotation may be of interest. It is from De Laski & Throop v. William R. Throop & Sons, 218 Fed. 458, 464 (1914), aff'd. 226 Fed. 941 (3 Cir. 1915).

> "In order to constitute two persons joint inventors, it is not necessary that exactly the same idea should have occurred to each at the same time, and that they should work out together the embodiment of that idea in a perfected machine. The conception of the entire device may be due to one, but if the other makes suggestions of practical value, which assisted in working out the main idea and making it operative, or contributes an independent part of the entire invention, which is united with the parts produced by the other and creates the whole, he is a joint inventor, even though his contribution be of comparatively minor importance and merely the application of an old idea. (Citing cases.)"

Sincerely,

SCY:d
cc: Mr. Kite Sharpless

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H. H. Goldstine
Thomas J. Watson Research Center
Yorktown Heights, New York

March 3, 1965

Dear Art:

I have read over in detail your letter of February 18 together with the accompanying letters of contribution.

I am in complete agreement as to the things which you and your colleagues, Kite Sharpless and Bob Shaw, assert that you did. I remember the points that you raise in your letters and agree that you people actually did the things which you have asserted.

On the basis of what I know about joint inventors, and on the basis of the quotation which was contained in the letter from Mr. Yuter to Bob Shaw dated July 24, 1964 in which a definition is given of joint inventor, I completely agree that you people are joint inventors of the ENIAC.

With best regards.

Sincerely,

Herman

Professor A. W. Burks
Department of Philosophy
The University of Michigan
Ann Arbor, Michigan

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