Semiconductor User Information Service Volume I

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Semiconductor User Information Service Volume II

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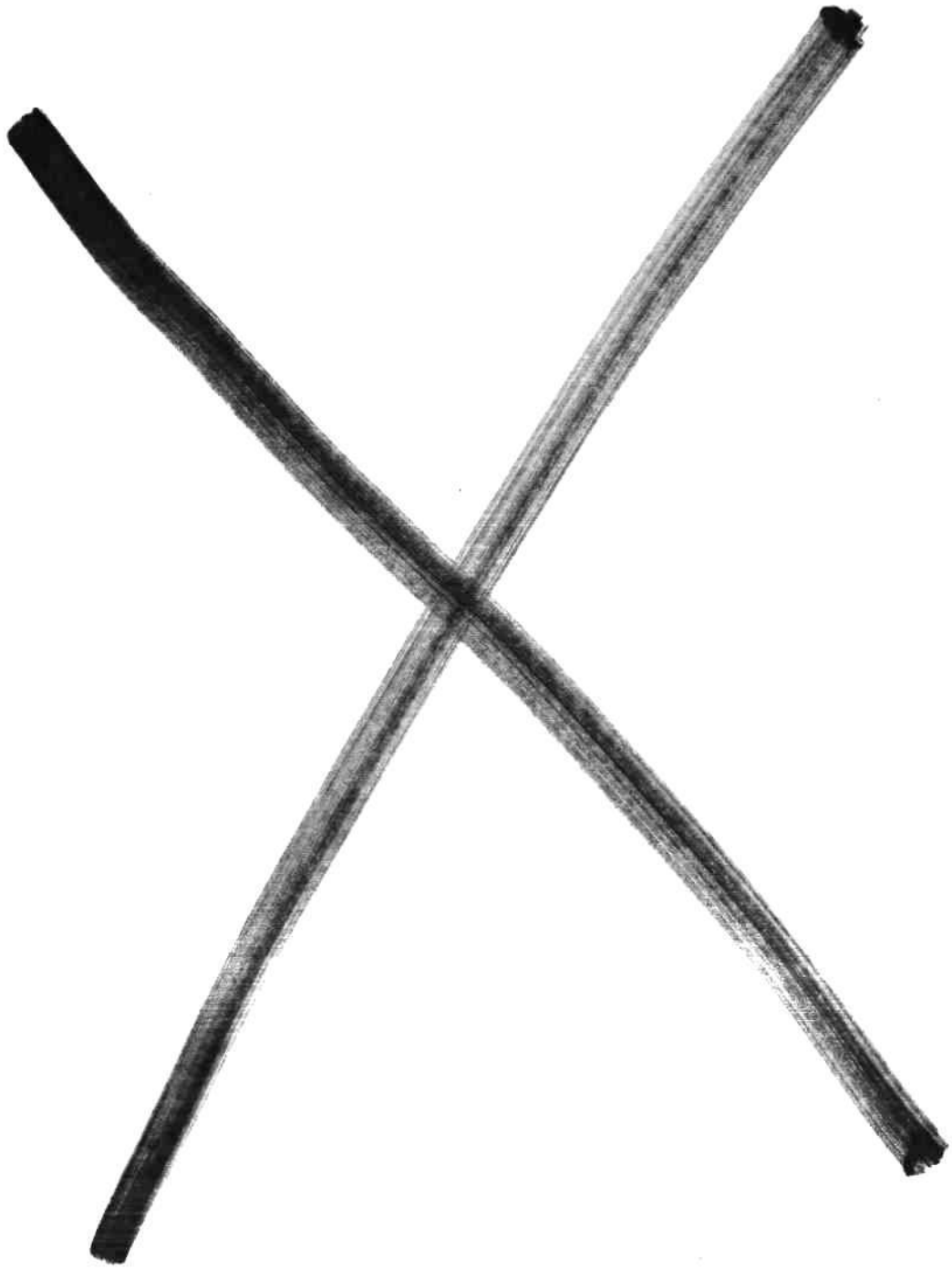


Introduction

This volume of DATAQUEST's Semiconductor User Information Service contains specific information on individual semiconductor manufacturers. The company profiles that form the main part of the volume are filed alphabetically by company name behind the appropriate tabs. Where a semiconductor company is owned by a parent company with a different name, the company discussion is filed under the name of the parent company; e.g., discussion of American Micro Systems, Incorporated, is filed under the name of its parent company, Gould, Incorporated. Only those companies that have their own wafer fabrication facilities and sell semiconductor devices on the merchant market are included in this section.

The section called Semiconductor Services discusses those companies that offer services in the areas of semiconductor design, production, and testing.

The index at the back of this volume is identical to that in Volume I of the service. It includes a detailed index of Volume I and a list of the companies covered in this volume.

The wall-chart that accompanies this volume lists semiconductor manufacturers and indicates the types of devices that they manufacture.

COMPANY PROFILES

Each company profile in the main body of the volume discusses the following kinds of information:

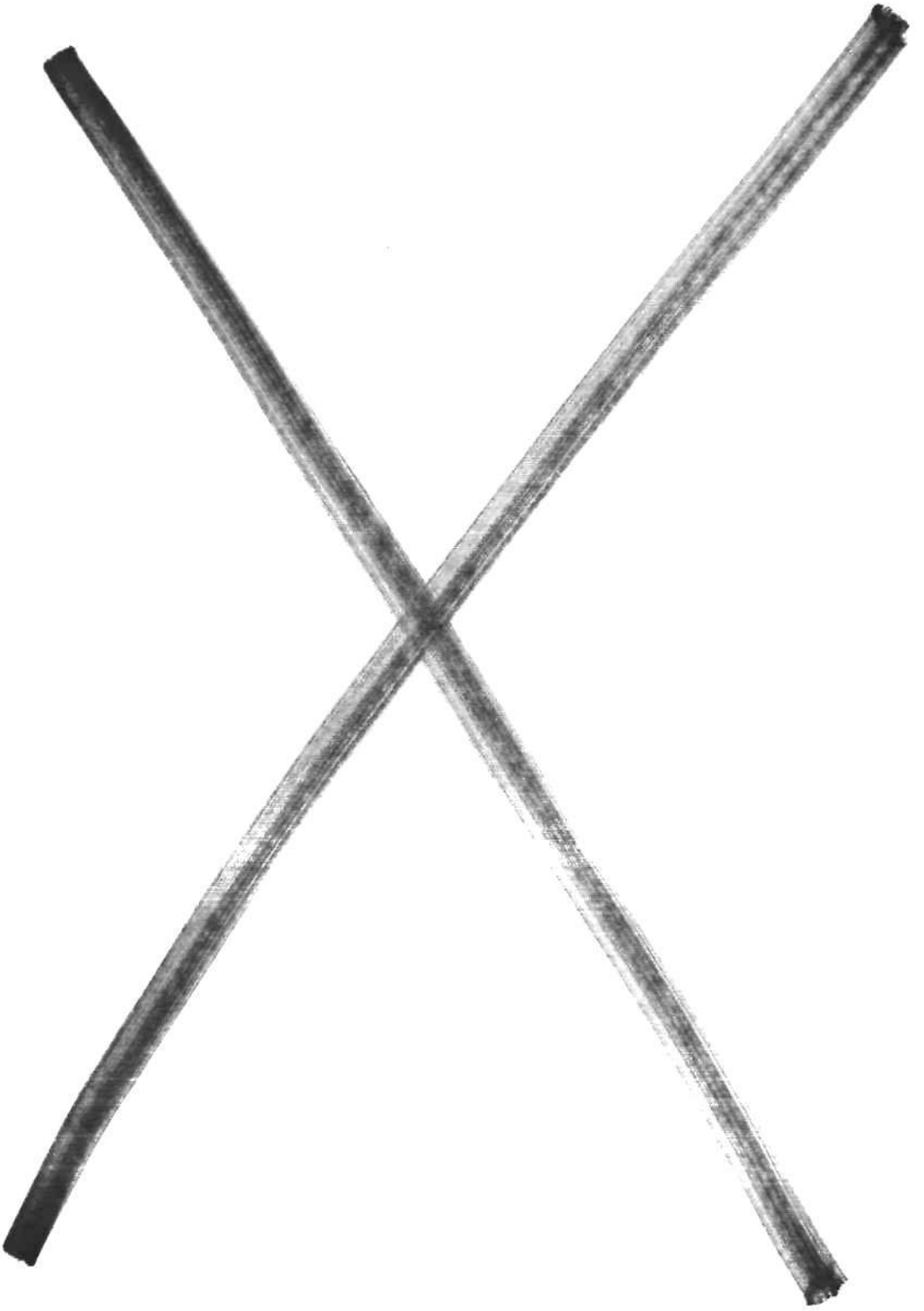
- Background - Where and when the company was founded. Major shareholders. General description of the company and the focus of its market.
- Operations - The divisions of the company. The company's facilities and their locations.
- Marketing - The company's marketing channels: direct sales, OEM sales, representatives, distributors. Specific marketing agreements. Overseas marketing channels. We also include the address and telephone number of the company's marketing and sales headquarters.
- Research and Development - R&D expenditures. Recent inventions or developments. Special focus of research efforts.
- Employees - Number of employees. Changes in the total compared with previous years. Percentage of the workforce employed in engineering and in research and development.

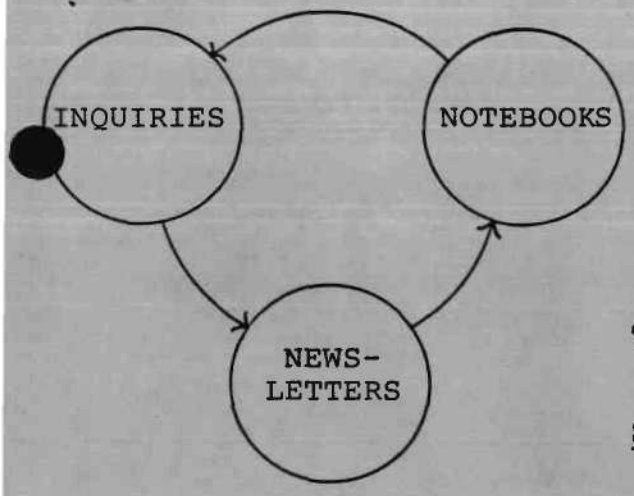
Introduction

- Products - Focuses on the company's semiconductor products. Main product areas, main product families. Major cross-licensing and second-source agreements. Recent product introductions not covered in the R&D section.

- Other Activities - Brief description of the other divisions of the company. The impact, if any, of other divisions on the semiconductor division (e.g., in-house use of products).

Wherever possible we include a financial synopsis for publicly held companies, as well as our estimates of the company's revenues from major categories of semiconductor sales.





SEMICONDUCTOR USER INFORMATION SERVICE

THE THREE-RING CIRCUS

SUIS Product Bulletin

SELLING SEMICONDUCTOR SERVICES TO USERS
SUIS OR SIS...OR BOTH??

Generally speaking, all semiconductor users should buy SUIS. This is because information contained in SUIS answers the kinds of questions asked by purchasers of semiconductors while SIS generally talks to semiconductor manufacturers. A comparison of clients interests in three areas of interest show how the services differ.

Business trends - Manufacturers want to know the effect of product demand trends on semiconductor revenues and average prices so that they can project company growth and profitability, and determine their company and competitor's market shares. Users want to know the effect of the demand trends on specific product prices and delivery lead times.

As a result, SIS provides revenue history and forecasts by product group and by company, and unit shipment data by manufacturer and product group. SUIS provides price and lead time data by product family as well as cost information for representative product types.

Products - Manufacturers want to know how many competitors exist for certain products, what end markets/applications exist for those products, what competitor's positions are and how important specific product families are to a competitor's total business. Users want to know what types of products are available of a given family, and what differences there are between different manufacturers products (are they compatible?). Users also want to know which are becoming industry standards and which will serve specific market niches. They want to know if there are enough suppliers to meet their requirements.

As a result, SIS provides market oriented product information such as shipment information by various categories of products and by end user categories. SUIS provides information about different kinds of products that are available, their characteristics, who supplies them, cost data, future product trends.

Companies - Manufacturers want to know the financial structure of major competitors. They want to know their business strategies and plans to determine who they will be competing against and their strengths and weaknesses. Users want to know what products suppliers offer, their financial viability as a long term supplier, what their production capability is, how they interface with and support customers, and how they do business.

As a result, SIS and SUIS provide financial reports of publicly held companies and estimated sales by product category for all companies. However, SIS provides this information and reports from analysts' meetings for about 20 major manufacturers. SUIS will be providing more extensive company profiles. These profiles will contain the following information.

COMPANY PROFILES

SUIS will cover a total of 100 companies in the company profile section of the notebook. We will profile 50 companies by the end of 1983 and 100 companies by the end of 1984. Each profile will be updated annually. The following information will be provided.

- BACKGROUND - Where and when founded, sources of start-up capital, how much, major stockholders, general company product/market/service focus.

- OPERATIONS - Divisions of the company, facilities and locations, usage of contract resources.

- MARKETING - channels, marketing organizations, how to contact marketing headquarters, unique marketing approaches, overseas channels and contacts, target market/applications general marketing/sales philosophy.

- RESEARCH AND DEVELOPMENT - R&D expenditures, technology directions, recent inventions, implications for users, special programs.

- EMPLOYEES - Number of employees. Percent employed in R&D and engineering.

- PRODUCTS - Important semiconductor product lines, literature support, other product support. Major cross licensing and second source agreements, support offered, product support philosophy.

- TECHNICAL CAPABILITIES - Types and general description of processes, CAD tools and interfaces for users, silicon foundry services offered.

While we are developing the service, this information is available on an inquiry basis.

There have been some semiconductor users who have purchased SIS. They seem to fall into three groups.

- Companies who have captive semiconductor manufacturing capability.
- Companies who sell equipment to semiconductor manufacturers or that test or program semiconductors.
- Large companies with purchasing departments that do strategic analysis of the semiconductor industry and/or want to know what share they purchase of a company's total business.

In the first two cases the SIS subscription will generally be held by a strategic planning or marketing group. In the last case it will be held by the purchasing department. In all cases the companies need to buy SUIS to provide them with the purchasing information that they need. In the first two situations you will be selling SUIS as a new group in the company that will have a separate budget. In the last case you will be selling SUIS to the group that already has SIS. Once they understand the differences between the two services, they will want to have both. The SUIS introduction has been revised to tell existing and prospective clients how the service can help them. A copy is attached.

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Introduction to the Service

The Semiconductor User Information Service (SUIS) is a comprehensive, worldwide business research service for managers involved in selecting and procuring semiconductors. Trends important to semiconductor procurement managers are monitored and analyzed by SUIS and reported in a timely manner. The following three elements of the Service provide clients with information they need for making important procurement decisions:

- Two looseleaf reference notebooks that provide information about semiconductor prices, costs, manufacturers, products, and other procurement-related topics
- Newsletters that report on significant industry developments in a timely manner
- Inquiry privileges that enable users to access the comprehensive SUIS data base and research team for answers to specific questions or more in-depth information on a particular area of interest.

By using the information provided by the Semiconductor User Information Service, procurement managers can reduce purchasing costs in a number of ways, including the following:

- Writing contracts that take advantage of projected price declines rather than being locked in at a fixed contract price while market prices decline
- Reducing cost of vendor selection by prescreening vendors' capabilities before surveying candidates for a new product program. Reduce time spent at each vendor; visit only the really promising candidates; reduce total travel costs
- Reducing training costs for new procurement personnel by using the notebooks and newsletters as a training resource to increase productivity faster and reduce purchasing costs

Examples of typical procurement decisions and approaches describe how SUIS can save time and money. Properly used, the service can pay for itself very quickly as illustrated in the following examples:

- Example 1: A company/division is estimating the cost of materials for the next year in order to determine manufacturing costs to be input into the company's/division's annual operating budget.

  Utilizing the SUIS Price Trends Newsletter, the cost models in the notebooks, and the inquiry service, users can establish the amount that prices will change. DATAQUEST can also provide background information that will answer the question of why they will change.

- Example 2: A new product is being developed that requires a nonstandard logic solution to meet cost/performance objectives. More than 60 semiconductor manufacturers make semicustom or standard cell products. More than half of these companies have been formed in the past five years.

  The SUIS notebooks identify all companies making products that could satisfy the requirement. By reading the company profiles, the user can obtain more specific information about a company (operations, employees, sales, financial results), the products it offers, its marketing strategies, its style of interfacing with customers, the design tools it has available, and other facts. After the users narrow the list of possible vendors, SUIS can provide more detailed information about each company and help in selecting the group of companies that the users will meet with in order to choose vendors to supply the semiconductor requirements. Since DATAQUEST is not associated with any semiconductor company, we can provide objective analysis of prospective vendors' capabilities. Users will often find that the best source(s) are the one(s) that might not have been considered otherwise.

- Example 3: A rapidly growing company must regularly add semiconductor purchasing people, some of whom have limited experience with semiconductors.

  The SUIS notebooks are an excellent training resource for people unfamiliar with the semiconductor industry. Notebook sections cover everything from basic semiconductor technology to economic effects on semiconductor procurement decisions. By reading the SUIS notebooks, new people can quickly familarize themselves with the industry, products, and manufacturers. This will help them become productive more quickly.

SERVICE ORGANIZATION

Client Data Base

The client data base is organized in two looseleaf notebooks. The information in these notebooks is updated annually to keep it current with the state of the industry. The date of publication is noted at the bottom of each page.

Volume I is organized into sections relating to specific procurement decisions or areas of interest.

Section Name	Decision(s)/Area(s) of Interest
Industry Overview	Training/Introduction to industry
Semiconductor Trends	Planning/Trends that affect buying decisions

Introduction to the Service

Semiconductor Procurement Challenges	Procurement strategy development/Impact of industry changes on procurement activities
Economic Factors	Planning/Effects of economy on procurement activities
Technology Tradeoffs	Product selection/Comparision of alternative product-technology approaches
Sources and Logistics	Procurement strategy development/Alternative channels of supply and characteristics
Capacity	Planning/Capacity utilization and supply-demand effects on purchasing decisions
Semiconductor Technology	Training/Basic description of semiconductor products and how they are made

Volume I also includes a glossary of terms and a topical index. These items help users learn the language of the semiconductor industry and also help them find information about specific topics of interest.

Each notebook section is reviewed once per year and updated as required to include new information.

Volume II contains profiles of semiconductor manufacturers. These profiles are designed to be part of a system for evaluating vendors' capabilities and selecting companies as suppliers. For each company covered we discuss:

- Background
- Marketing methods and channels
- Research and development
- Employee information
- Product information
- Nonsemiconductor business activities
- Financial background

A financial balance sheet and income statement are provided for publicly held companies. Sales by product category are provided for manufacturers with multiple product lines.

Introduction to the Service

A semiconductor service section lists companies that provide specific manufacturing and testing services. The services provided include:

- Custom-chip design and layout (including CAD services)
- Wafer processing (silicon foundries)
- Assembly
- Testing/screening
- Microanalysis

Semiconductor users can implement some or all of the steps for developing and manufacturing custom integrated circuits using these services.

A vendor selection wall chart is also included in Volume II. This wall chart lists more than 160 semiconductor manufacturers and identifies the types of products they manufacture.

Volume II is a useful tool for methodically selecting suppliers for new products that a company is developing. For example, a company is going to use gate arrays in a new system design. The required specifications are known and a supplier has been identified. The procurement manager wants to know if any other suppliers make the product or similar products, and then select several sources to ultimately supply the company's production requirements. Although several suppliers can satisfy the technical requirements, the buyer wants to select those that will also be able to support production demands and work closely with the company.

The first step is to use the wall chart to identify all suppliers making gate arrays. Next the procurement manager reads the company profiles and learns how each company markets and supports its gate arrays. This step should allow the buyer to narrow the list to a smaller group that must be evaluated further. Next a list of questions and requirements is developed; this helps the buyer to know each supplier's capabilities in detail. DATAQUEST can help develop the questionnaire and provide answers to some of the questions in advance, thus shortening the time required to conduct vendor surveys and focusing on critical areas where information is not available.

Newsletters

Monthly newsletters tell users about new developments that could affect procurement decisions. Each quarter we provide data on price trends and lead times for more than 30 categories of semiconductor products. We also publish a quarterly economic review covering critical trends that affect semiconductor supply/demand. In addition we provide new information about products and companies. Product/company topics generally include analysis of product types offered, supplier capabilities and strategies, future product plans, price trends, supply

demand considerations, cost models, and other factors that affect purchasing decisions. Newsletters also address nonproduct issues, such as quality, packaging, logistics, and others.

Inquiry Privilege

DATAQUEST offers a unique unlimited inquiry privilege for notebook holders who want to explore an area of interest in more depth than is provided by the notebooks or newsletters. Through inquiries, users are able to access DATAQUEST's extensive files on the semiconductor industry or talk to our staff of electronics specialists. The questions clients ask often contribute to the selection of a topic for a future newsletter.

When appropriate, inquiries are answered in writing with an inquiry response letter. These letters are sent to all notebook holders at the client company with instructions for filing them. In this manner, a company's notebooks are tailored to its specific needs and interests. Documented inquiries often indicate areas where we should write newsletters or add to notebook sections. Through the interactive use of the service, we are able to stay on top of areas of immediate interest to our clients.

These are examples of some of the questions that clients have asked:

- What will be the pricing of 74F and 74ALS relative to 74S and 74LS, respectively, over the next five years?
- What companies manufacture 8Kx8 static RAMs? What are prices now? What will they be in a year, in two years?
- What work is going on in the area of static discharge and its effects on ICs?
- What is the manufacturing cost structure of 64K dynamic RAMs? What will happen to costs in the next two years?
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Most inquiries are answered in one day or less. A few may take several days. In a few cases it may be necessary to do an extensive amount of research to answer an inquiry. When this situation occurs, we may propose a consulting project to provide you with the needed in-depth information for a nominal consulting fee.

Introduction to the Service

Semiconductor User Staff Capabilities

The DATAQUEST Semiconductor User Information Service staff has a continuing, long-term commitment to the semiconductor and related electronic industries. The staff has in-depth expertise in all facets of the electronics industry and represents more than 50 years of industrial and consulting experience within the field.

Members of the DATAQUEST professional staff are frequent speakers at industry seminars and symposia. We participate in the leading professional societies related to the electronics industry. We maintain contact with a large user base through sophisticated sampling and interviewing techniques. Our staff regularly reviews all important publications related to the semiconductor industry and associated user industries.

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The Service begins on the date of the first billing. At that time, the subscriber receives a set of binders containing complete, up-to-date material and copies of all recent newsletters. For the duration of the subscription, the subscriber receives a copy of each additional or replacement section of the binders and each newsletter published. The inquiry privilege is valid throughout the subscription period.

Add-On Subscriptions

Subsidiaries, divisions, regional offices, majority-owned affiliates, and parent companies of the subscribing organization are eligible for "add-on" subscriptions at a percentage of the base price for each additional subscription. These add-on subscriptions include complete copies of all published material and full inquiry privileges.

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Introduction to the Service

SERVICE STAFF

Stan Bruederle

Mr. Bruederle is Manager of DATAQUESTs Semiconductor User Information Service. He is responsible for applied research in the semiconductor and related industries. Before joining DATAQUEST in 1982, Mr. Bruederle spent 10 years with Signetics Corporation, where he held a variety of management positions in marketing and strategic planning. He has 17 years of engineering and marketing experience in the semiconductor industry. Mr. Bruederle received his B.S. in electrical engineering from the University of Wisconsin and has completed work toward an M.B.A. at Arizona State University.

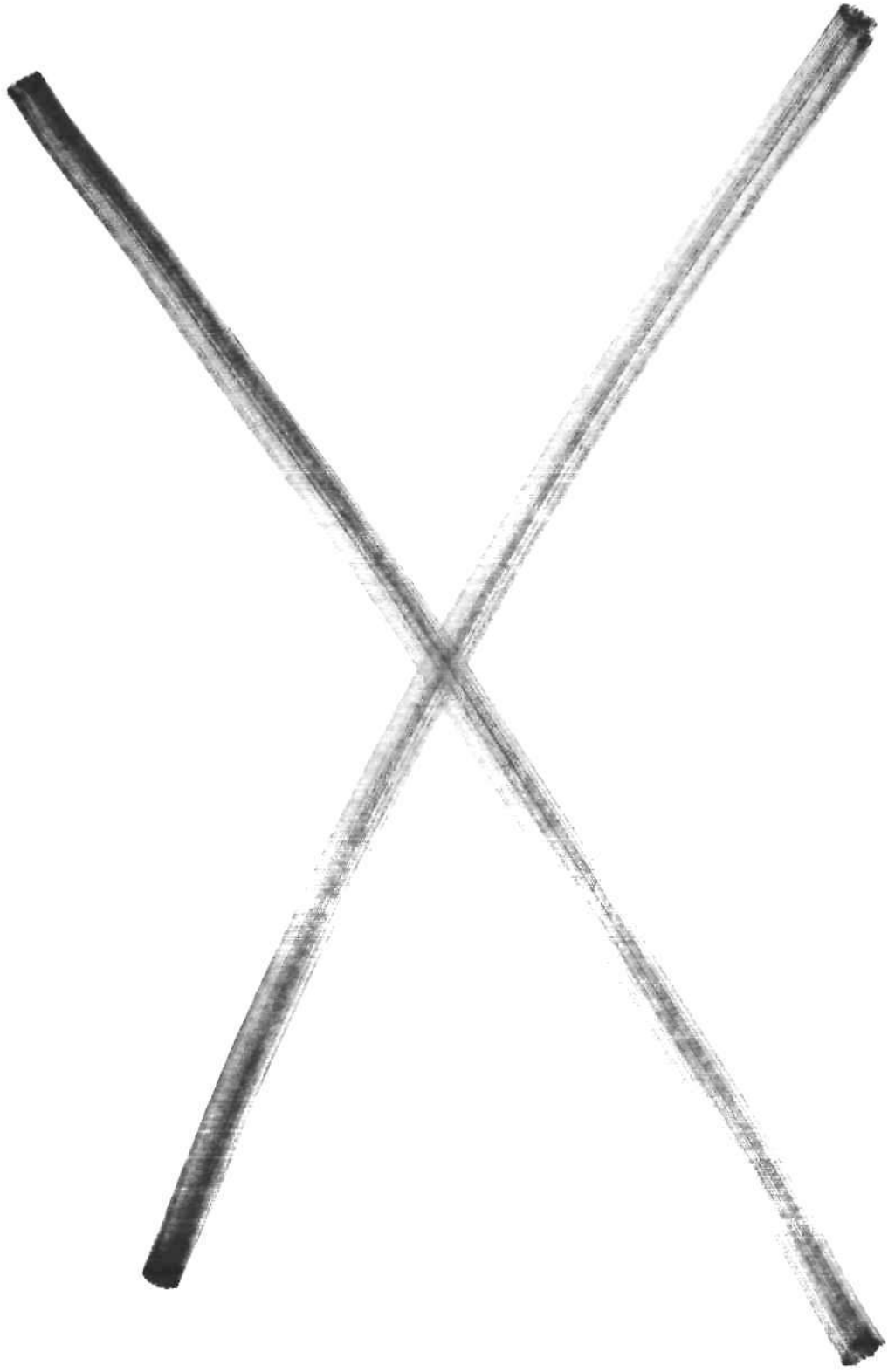
Jean Page

Ms. Page is a Research Analyst for DATAQUESTs Semiconductor User Information Service. She is responsible for worldwide research regarding semiconductor suppliers, and for handling client inquiries. She has been with DATAQUEST for more than three years, most recently as a member of the European Semiconductor Industry Service. Before joining DATAQUEST, Ms. Page worked for 10 years in libraries and information research departments and spent one year in Switzerland as a technical translator. Ms. Page studied library science at North-Western Polytechnic in England and holds a B.A. degree from the Open University in England.

Introduction to the Service

Daniel L. Klesken

Dr. Klesken is Director of DATAQUESTs Semiconductor Group. He specializes in the areas of semiconductor memory, microprocessors, major users of semiconductors, applications, and strategic planning. He is often called upon to speak on key issues facing the semiconductor industry and has addressed many audiences in the United States and Europe. Prior to joining DATAQUEST in July 1976, he was with Texas Instruments for nine years as a member of the technical staff. At TI he was in the Central Research Laboratories where he did corporate strategic planning and market research. His earlier research was in the area of computers and digital communications systems. Dr. Klesken received his B.S. and M.S. degrees in electrical engineering from Lehigh University and his Ph.D. in electrical engineering from Carnegie-Mellon University.



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Volume I

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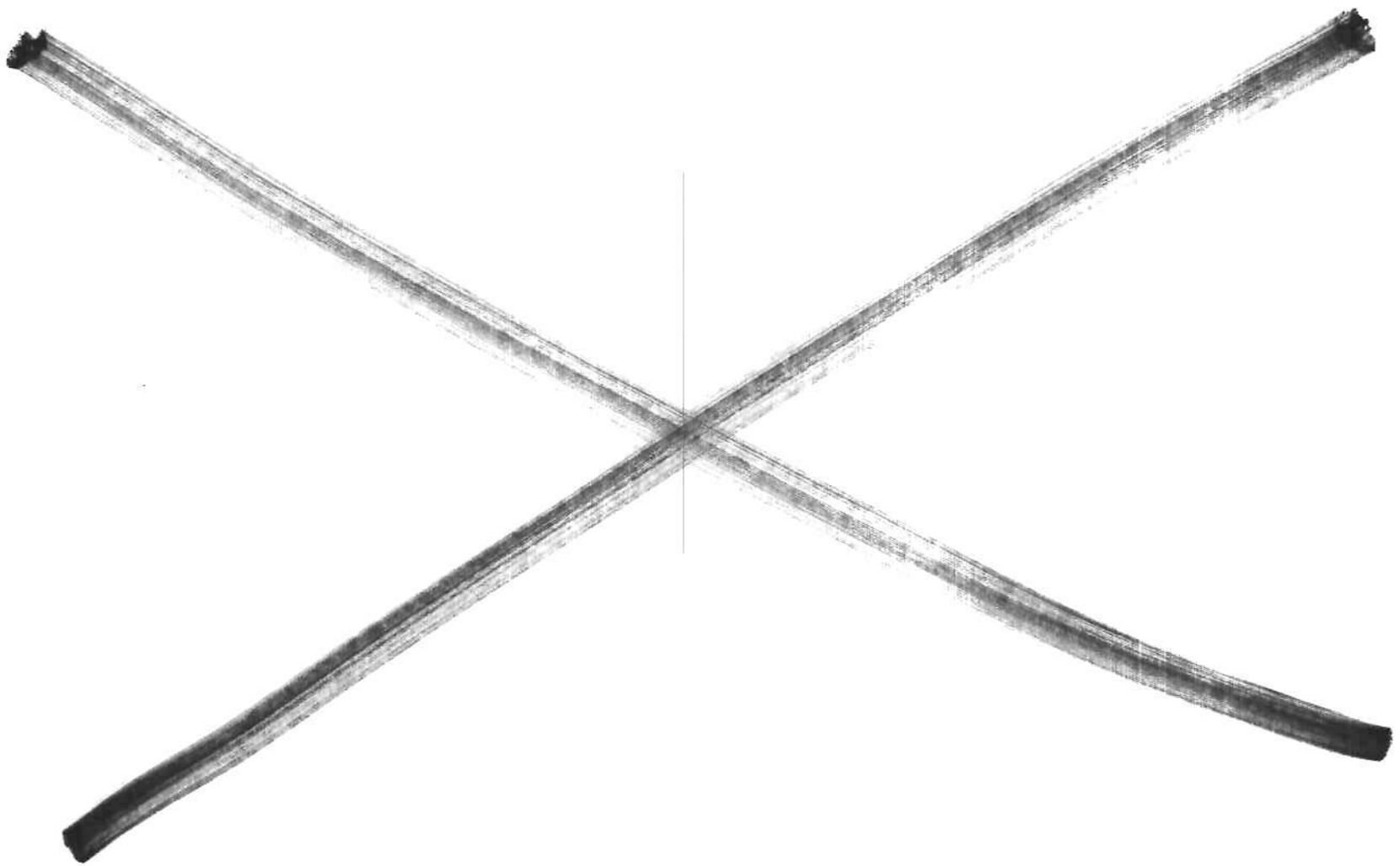


1. Industry Overview

The purpose of this section is to give the semiconductor user a brief description of the semiconductor industry, including its history, structure, special characteristics, and market size and growth.

Semiconductor usage has become key to the success of an ever-increasing number of modern corporations. Semiconductor devices are the basic components of computers and other data processing equipment, telecommunications, industrial automation, television and radio, defense electronics, and other important products. Both directly and indirectly, semiconductor devices are important in nearly every facet of our lives.

In 1981, the worldwide consumption of semiconductor devices exceeded $13 billion. Industry used literally billions of devices consisting of thousands of types of individual products—including integrated circuits, diodes, transistors, and optoelectronic devices. Despite their wide diversity, these products share the common bond that their basic electronic functions are performed by semiconducting materials.

About 200 companies actively compete in the merchant semiconductor industry worldwide. Many of these companies are small, with semiconductor revenues of less than $20 million annually. However, at least 26 companies each supply more than $100 million of semiconductors annually. These companies produce about 80 percent of worldwide semiconductor shipments. Major U.S., West European, and Japanese merchant manufacturers of semiconductors are shown in Table 1-1.

1. Industry Overview

Table 1-1

MAJOR MERCHANT SEMICONDUCTOR SUPPLIERS

United States	Western Europe
AMD	AEG-Telefunken
AMI (Gould, Incorporated)	Philips
Fairchild (Schlumberger)	SGS-Ates
General Electric	Siemens
General Instrument	Thomson-CSF
Harris	
Intel	Japan
ITT	
Mostek (United Technology Corporation)	Fujitsu
Motorola	Hitachi
National Semiconductor	Matsushita
RCA	Mitsubishi
Signetics (Philips)	Nippon Electric
Texas Instruments	Sanyo
	Toshiba

Source: DATAQUEST, Inc.
April 1982

1. Industry Overview

HISTORY

This section gives a brief chronology of the development of the semiconductor industry. Major events are summarized in Table 1-2.

The first transistor was successfully demonstrated at Bell Laboratories on December 23, 1947. It heralded the beginning of the semiconductor industry. Technical breakthroughs in the manufacture of transistors followed rapidly, and by 1952 a number of companies were producing devices commercially. These devices, however, were made using germanium as the semiconductor material.

In 1954, Texas Instruments (TI) began to manufacture silicon transistors on a commercial scale. Prior to that time, TI had not been a factor in the semiconductor industry. Within three years TI and Transitron had about a 35 percent market share between them. The other major suppliers of the day included General Electric, Philco, RCA, Raytheon, Sylvania, and Westinghouse. In the late 1950s, the industry was still in its infancy with sales just beginning to pass the $100 million mark. The major market for semiconductor devices was provided by the military, which had seen the potential of semiconductors and actively supported the industry's development. Another large market was created by transistor radios.

In 1959, Fairchild Camera and Instrument developed the planar technology for making transistors, which later became the basic technology for the manufacture of integrated circuits (ICs). Integrated circuits themselves were not commercially produced until 1961, when they were first marketed by Fairchild and Texas Instruments. At about the same time, a wider variety of semiconductor devices was developed, including MOS devices, junction field effect transistors, and Schottky diodes. At this time, several improvements in manufacturing technology occurred, allowing rapid increases in productivity and device reliability.

In the mid-1960s, the use of integrated circuits grew rapidly, and by 1965 worldwide industry sales had passed the $1 billion mark. This period also marked an expansion of uses for semiconductor devices, including many markets for industrial products, data processing systems, and communications equipment. During this time, MOS devices became commercially available. U.S. companies began to assemble their products overseas and both the West European and Japanese markets became important. In 1968, the first light-emitting diodes were sold commercially by Hewlett-Packard following their development by Bell Laboratories four years earlier.

The late 1960s and early 1970s marked some major changes to the semiconductor industry. During this span, more than 36 new merchant companies were established. At the same time, many companies set up captive semiconductor facilities for in-house production. These new companies added technical and competitive impetus to an already fast-moving industry. This period also saw the rapid rise of MOS integrated circuits as a major product area in the semiconductor industry. Major new products included semiconductor memory, custom devices, and complex linear circuits such as operational amplifiers, voltage regulators, analog to digital (A/D) and digital to analog (D/A) converters, and others. The early 1970s

marked the advent of large scale integration (LSI) devices, and consumer applications such as calculators and watches. The era of low-cost electronics was under way.

The late 1970s saw the establishment of a large worldwide semiconductor industry, with competition on an international scale. The emergence of very large scale integration (VLSI) devices included various types of customizeable semiconductors such as 8- and 16-bit microcomputers, single-chip microcontrollers, 64K ROMs and EPROMs, and gate arrays.

As the industry celebrates its thirty-fifth anniversary, 256K RAMs, 128K ROMs, 64K EPROMs, and 32-bit microprocessors are realities, as are 100-GHz transistors.

1. Industry Overview

Table 1-2

SEMICONDUCTOR INDUSTRY MILESTONES

Year	Technological Advance	Pioneering Company
1947	Point Contact Transistor Invented	Bell Laboratories
1948	Junction Transistor Proposed	Bell Laboratories
1950	High-Purity Germanium Developed	Bell Laboratories
1950	Junction Transistor	Bell Laboratories
1951	Zone Refining of Semiconductors Developed	Bell Laboratories
1951	Junction Devices Sold Commercially	General Electric and others
1951	Gallium Arsenide Material	Siemens
1952	Alloy Transistor	Bell Laboratories
1953	Surface Barrier Transistor	Philco
1953	Unijunction Transistor	General Electric
1953	Silicon Solar Cells	Bell Laboratories
1954	Junction Field Effect Transistor Proposed	Bell Laboratories
1954	Diffusion Process Developed	Bell Laboratories
1954	Oxide Masking	Bell Laboratories
1954	Photolithographic Techniques	Bell Laboratories
1954	Zener Diode	National Semiconductor and others
1954	Transistor Radio	Texas Instruments, Regency
1954	Silicon Transistor	Texas Instruments
1954	Interdigitated Transistor	Transistor Products
1955	Diffused Base Transistor	Bell Laboratories
1956	Silicon Controlled Rectifier	General Electric
1956	Commercial Unijunction Transistors	General Electric
1957	Mesa Transistor	Motorola
1958	First Integrated Circuit	Texas Instruments
1958	Tunnel Diode	Sony
1958	Step Recovery Diode	Hewlett-Packard
1958	Planar Transistor	Fairchild
1959	Planar Process	Fairchild

(continued)

Table 1-2 (continued)

SEMICONDUCTOR INDUSTRY MILESTONES

1960	Epitaxial Transistor	Bell Laboratories
1960	MOS Field Effect Transistor	Bell Laboratories
1960	Schottky Barrier Diode	Bell Laboratories
1961	First Commercial ICs	Fairchild, Texas Instruments
1961	First Planar Field Effect Transistors	Amelco
1961	RTL logic ICs	Fairchild, Texas Instruments
1962	Solid State (GaAs) Laser	General Electric, IBM
1962	DCTL logic ICs	Fairchild
1963	Gunn Diode	IBM
1963	TTL logic ICs	Sylvania
1963	ECL logic ICs	Motorola
1963	Commercial MOS Discretes	Fairchild
1963	Linear IC	Fairchild, TI, Westinghouse
1964	Light-Emitting Diode	Bell Laboratories
1964	GaAsP LED	Bell Laboratories
1964	MOS ICs	General Microelectronics
1964	First Static Flip-flop IC	Fairchild
1965	IMPATT Diode	Bell Laboratories
1965	LSA Diode	Bell Laboratories
1965	High-Speed TTL	Texas Instruments
1965	First Integrated Operational Amplifier	Fairchild
1965	Epoxy IC Package	Fairchild
1965	Dual In-line Package	Fairchild
1966	NMOS	Fairchild
1967	ROM	Fairchild
1968	Commercial Light-Emitting Diode	Hewlett-Packard, Monsanto
1968	Low Power TTL ICs	Texas Instruments
1968	CMOS ICs	RCA
1968	1,024-bit ROM	Philco-Ford
1969	GaAs Junction FET	IBM
1969	Silicon gate MOS	Intel

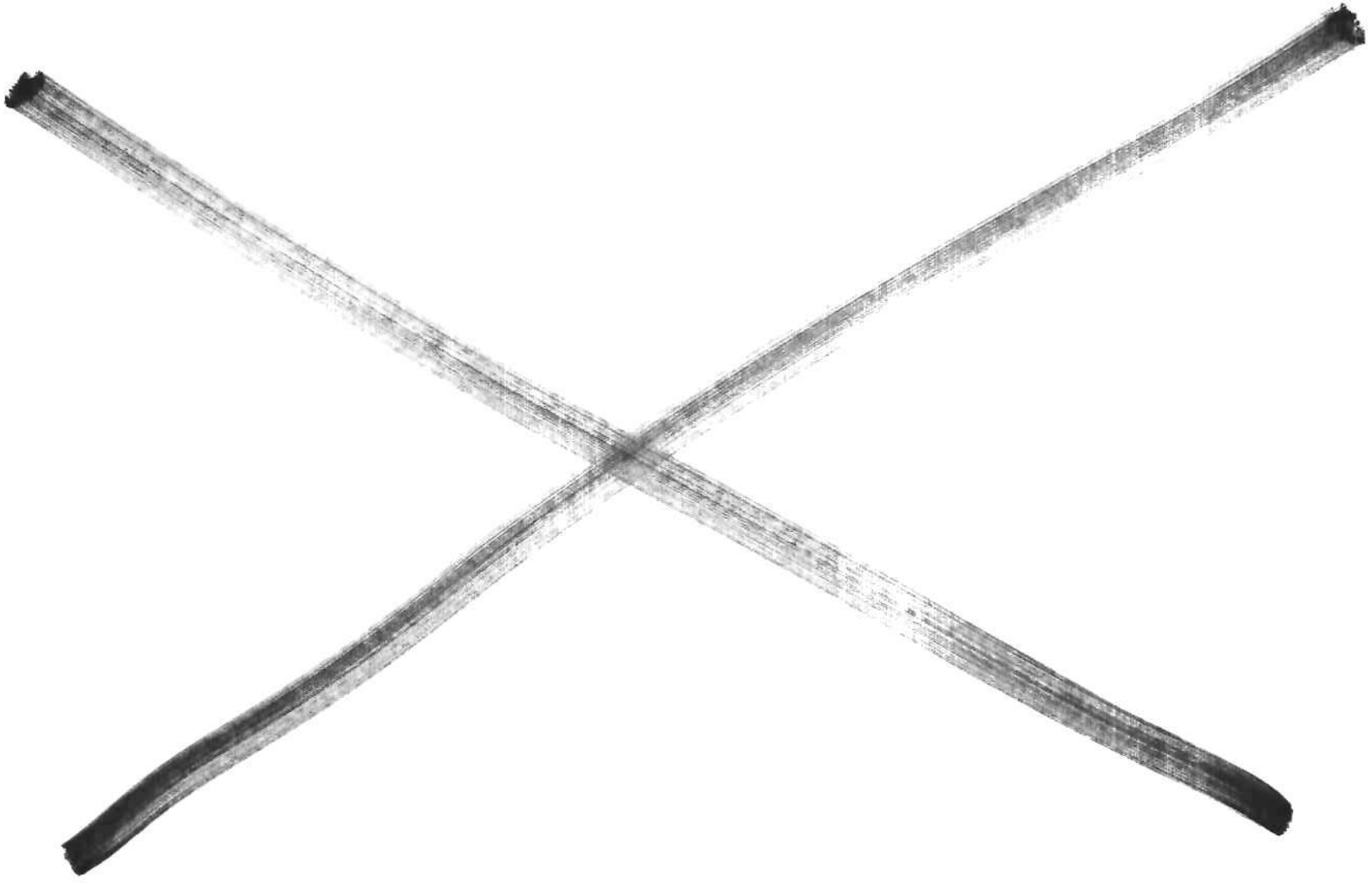
(continued)

Table 1-2 (continued)

SEMICONDUCTOR INDUSTRY MILESTONES

1970	Charge Coupled Device	Philips
1970	Schottky TTL	Intel, Texas Instruments
1970	Single Chip for Calculator	Texas Instruments
1971	Isoplanar Process	Fairchild
1971	Commercial Silicon on Sapphire	Interlek
1971	Ion Implantation	Lintott, Extrion
1971	Bipolar PROM	Monolithic Memories
1971	EPROM	Intel
1972	Low-Power Schottky TTL	Texas Instruments
1972	Microprocessor	Intel
1972	I^2L Circuits	Philips, IBM
1973	Electrically Erasable Non-Volatile Memory	Hitachi, NCR
1975	Bit Slice Bipolar Microprocessor	MMI, AMD
1976	Power MOS FET	Siliconix
1977	Random Access Memory with On-Chip Redundancy	IBM
1977	Microprocessor Controlled Automobile Engine	GM
1978	Speech Synthesis Chip	Texas Instruments
1980	Single Chip Color TV Sensor	Sony
1981	Speech Recognition Chip	Weitek
1981	High-Temperature (325°C) CMOS	Harris, Sandia Labs

Source: DATAQUEST, Inc.
April 1982



Nielsen Dataquest

INQUIRY RESPONSE

DATE: 12/8/83

TO: Bob Hatch/Kaiser Electronics

FROM: Mary Olsson/SUIS

This information has been compiled in response to your inquiry of Nov. 1983

Please file in Vol.I, Sec.2 for future reference.

Subject: Availability of Linear Device Groups

LINEAR DEVICE GROUPS
LCC% OF TOTAL LINEAR SHIPMENTS

Company	Availability	Comments
Motorola	4%-5%	883B & JAN
Texas Instruments	1%-2%	Slight increase in LCC in linear in 1984-1985

Motorola does not track the percentage of LCC by linear device groups. Motorola has the ability to do 883B and JAN type processing in LCC (ceramic) in all of their linear device groups.

Motorola is presently doing volume production of SOIC in 8-, 14-, 16-pins. Samples are available in 20-, 28-pin. Quad packs in plastic LCC. Motorola's selector guides and data books will be available in December 1983. Their predominant technology for LCC (ceramic) is FAST.

TI does not track individual linear device groups but they do provide 883B and JAN processing upon request.

	Dataquest	Kaiser Electronics
cc:	Stan Bruederle	Ed Moravick
	Jean Page	John Martein
		Bob Tose
		Dave O'Brien
		Jim Sprague
		William Olson
		Richard Colson

:tg

Nielsen Dataquest

INQUIRY RESPONSE

DATE: 11-15-83

TO: Ed Macaruso/Signetics

FROM: Mary Olsson/Semiconductor User Information Service

This information has been compiled in response to your inquiry of Nov. 1983

Please file in for future reference Vol.I, Sect.2

Subject: HCMOS Market

Table 1 lists our estimate of production availability of HCMOS, by vendors from 1983 through 1984.

Company	1983	1984
Toshiba	57	N/A
National	70-80	170-200
Motorola (2.5u)	50-60	100-150
RCA (3u)	30 (20 sampling)	70-100

Table 2 lists our estimate of HCMOS sales in United States and Japan in millions of dollars.

	1983	1984
U.S.	17	50
Japanese	8	26

We are presently working on an HCMOS newsletter which should be ready by December of this year.

cc: Stan Bruederle
Jean Page

:tg

Nielsen Dataquest

INQUIRY RESPONSE

DATE: November 9, 1983

TO: Gianalfredo Vecchi
Italtel SIT, Italy

FROM: Jean Page, Semiconductor User Service

This information has been compiled in response to your inquiry of Nov. 1983

Please file in Section 2 for future reference.

Our estimates of the worldwide fibre-optics, active components market is:

	1982	1987
Total components	$81 million	$294 million
Laser diodes	$10 million	$ 74 million

Major optoelectronics suppliers offering fiber-optic components include, Hewlett Packard, Honeywell, TRW, T.I., and Motorola. I am sending you a more detailed list by mail.

Prices are expected to rise by 10-15% in 1984. Demand is very strong for military parts in this area.

cc: Gianni Bertolini

Enclosure

:tg

Nielsen Dataquest

INQUIRY RESPONSE

DATE: 10/11/83

TO: Gianni Bertolini/Italtel Sit

FROM: Jean Page/Dataquest

This information has been compiled in response to your inquiry of 10/11/83

Please file in Vol.I, Sec.2 for future reference.

SUBJECT: 8086 Microprocessors

In response to your telex dated 11/10/83:

1. We estimate that 345,000 8086s were shipped in the first quarter of 1983 and 478,000 in the second quarter of 1983. We expect the 8086 share of the market to decline slightly in favor of the 80186 in coming quarters.

2. Sources other than Intel are AMD, Fujitsu, Matra-Harris, NEC, and Siemens.

3. CMOS versions of the 8086 are expected from Harris and Oki.

4. We do not anticipate a complete takeover of Intel's capacity by IBM as a result of the IBM investment in Intel. Intel's production capacity far exceeds our estimates of IBM's needs.

cc: Bud Mills/Dataquest, France
Stan Bruederle, DQ USA
Mary Olsson, DQ USA

:tg

Nielsen Dataquest

INQUIRY RESPONSE

DATE: Sept. 23, 1983

TO: Bob Hatch/Kaiser Electronics

FROM: Mary Olsson/Dataquest, SUIS

This information has been compiled in response to your inquiry of Sept. '83

Please file in Vol.I, Sec. 2 for future reference.

Subject: Availability of Linear Device Groups and Surface Mounted JAN TX

Linear Device Groups
LCC% of Total Linear Shipments

Company	Availability	Comments
Motorola Emory Baxter Linear Marketing	3% - 4%	
Texas Instruments Gordon Ratcliff Packaging	1% - 2%	Slight increase in 1984-1985. TI does not track individual device groups.
National Hugh Wright Linear	0%	No LCC in linear devices in commercial. Plastic packages only.

I do not have data on the individual device groups from National and Motorola. I will send you this information as soon as it becomes available.

Discrete Semiconductors
Surface Mounted JAN transistors
1983

Company	Availability	Comments
National	4Q83-1Q84	SOT 3 leaded package. Presently have surface mounted ICs.
Motorola	1984	
Texas Instruments	-	Low emphasis on discretes.

Surface Mounted Components
(Manufacturers)

Company	Availability	Comments
Sprague	Now	JAN qualification, October 1983.
Allen Bradley	4Q83	Surface mounting in chip resistors & attachable resistor networks. Power Transistor Corporation, a recent acquisition, JAN TX available.
Amphenol/Bendix Sidney, N.Y.	-	Will have full array of surface mounted products soon.
AMP	-	Surface mounted connectors. Surface mounting in other products, probable in future.

Distribution:

Ed Moravick
John Martein
Bob Tose
Dave O'Brien
Jim Sprague
William Olson
Richard Colson

:tg

Nielsen Dataquest

INQUIRY RESPONSE

DATE: September 14

TO: Paul Bartlett/Mannesmann Tally

FROM: Mary Olsson/SUIS

This information has been compiled in response to your inquiry of Sept. 1983

Please file in Vol.I, Sec. 2 for future reference.

Subject: Semiconductor Suppliers

DATAQUEST's Chart of Semiconductor Suppliers was compiled April 1982. Recent updates to this chart are listed below.

SEMICONDUCTOR UPDATES

Company	Founded	Technology/Products	Comments
Array Devices, Inc. San Diego, CA	Sept. 1982	Custom & semicustom CMOS	
Custom MOS Arrays, Inc. Milpitas, CA	Aug. 1982	Custom & semicustom CMOS	
Cypress Semiconductor Santa Clara, CA	Feb. 1983	CMOS memory, logic	
Communications Transistor Corp. San Carlos, CA	1969	MOS microprocessors	Purchased by Acrian, Inc.1982
Excel Microelectronics, Inc. Milpitas, CA	March 1983	EEPROM & related products	Samples 2Q84 25 employees
Gigabit Logic, Inc. Westlake Village, CA	1982	GaAs IC's	
Iridian Microwave Corp. Chatsworth, CA	1982	GaAs microwave components	
Lattice Semiconductor Corp. Portland, Oregon	April 1983	MOS memories, logic	Samples 2Q84 25 employees
Maxim Integrated Circuits Sunnyvale, CA	May 1983	CMOS linear IC's	

SEMICONDUCTOR UPDATES

Company	Founded	Technology/Products	Comments
Omtac Palo ALto, CA	Feb. 1983	Custom IC's	
Telmos, Inc. Santa CLara, CA	Jan. 1981	Custom & semicustom IC's	
Ultra Logic Cupertino, CA	1981	MOS memories	Purchased by Zytrex Advanced Memories, Feb.1983.
Zytrex Corp. Sunnyvale, CA	May 1981	CMOS Memory logic	

Enclosure: (2)

cc: Marvin Crumb, President
Mannesmann Tally

:tg

Nielsen Dataquest **INQUIRY RESPONSE**

DATE: Sept. 9

TO: Monte Seifers/Northern Telecom

FROM: Stan Bruederle/Dataquest

This information has been compiled in response to your inquiry of September

Please file in Vol. I, Sec. 2 for future reference.

Subject: 64K DRAM Data

CERAMIC PACKAGE SUPPLIERS

In 1982 39 percent of 64K DRAM shipments were in ceramic packages. Manufacturers have estimated that in 1983 this will drop to 33 percent. Companies that have estimated significant ceramic shipments in 1983 and appear to be willing to continue shipping ceramic parts are Hitachi, Intel, National, and possibly Fujitsu. Fujitsu and Hitachi have told us that for 256K DRAMs, all non-plastic packages will be treated as special requirements. We will probably see this approach adopted for 64K DRAMs as well, as soon as everyone can ship plastic devices. You will then see prices for ceramic devices increase relative to plastic parts. You should see a price premium of as high as $1.00, probably within the next year.

SHIPMENT DATA

Package shipment data for 64K DRAMs is as follows:

64K DRAM SHIPMENTS
(millions of units)

	1982	1983
Ceramic	25.9	16.2
Cerdip	13.1	17.0
Plastic	58.5	263.9
Other	3.9	13.4
TOTAL	101.4	310.5

Table 1 is our package shipment forecast for Northern American semiconductor manufacturers.

Table 1

ESTIMATED NORTH AMERICAN SHIPMENTS
(millions of units)

	1982	1983	1984	1985	1986	1987	CAGR%
Plastic DIP	6,730	7,850	9,160	10,655	12,200	14,020	16
CERDIP	1,050	1,140	1,230	1,330	1,440	1,570	8
Ceramic DIP	75	80	85	90	95	100	6
Flatpak	40	36	33	30	27	25	(8)
Ceramic Chip Carrier	15	35	80	130	225	375	90
Plastic Chip Carrier & Quad	8	25	75	175	345	600	137
SO	5	30	80	150	250	410	141
PGA	2	5	10	20	35	50	90
Header	60	65	70	75	80	80	5
Other	250	435	605	795	1,025	1,250	37
TOTAL Packages	8,235	9,700	11,428	13,450	15,722	18,480	

PRICE DATA

Table 2 shows specific price data for 500,000 unit purchases of ceramic packages.

Table 2

CERAMIC PACKAGE COSTS

Pin Count	Cerdip	DIP	LCC
14	$.099	$0.48/0.83	-
16	$.129	$0.50/0.85	-
18	$.239	$0.53/0.93	-
20	-	$0.55/0.95	$0.50/0.95
24	$.404	$0.70/1.25	-

Note: For ceramic DIP and LCC, the first price is a glass sealed package while the second is a metal sealed package.

We expect ceramic package costs to increase in the future as shown by Table 3.

Table 3

CERAMIC PACKAGE PRICE TRENDS

1983	1984	1985	1986
-	+2 to 5%	+5%	+5%

DIP and LCC should follow the same trend although LCC will be lower cost for a given number of leads.

Projected price trends for 64K DRAMs are discussed in our newsletter 83-6 titled "Market Conditions for the 64K Dynamic RAM".

:tg

Nielsen Dataquest

INQUIRY RESPONSE

DATE: August 10, 1983

TO: Jean-Jacques Grimaud/Micro-Archi

FROM: Stan Bruederle

This information has been compiled in response to your inquiry of August

Please file in Section 2 for future reference.

SUBJECT: Memory and Microprocessor Forecast

This is the second quarterly forecast for the three specific products that you requested. The forecasts are limited to a two year outlook broken down by half years. The prices projected in this forecast are overall average prices. Prices for 10,000 and 100,000 unit purchases will be estimated in the next report. It will require additional research.

The 16-bit microprocessor, 1Mbit ROM, and packaging forecasts have been revised since the last report because of developments during the last quarter, and new information.

16-bit Microprocessor:-

Harris introduced the 80C86 and a family of support devices. The die size and pricing were more aggressive than we had expected. As a result, we moved our unit shipment forecast ahead and decreased prices. We believe that there will be five suppliers for the 80C86 by 1985. Harris has announced, Intel will introduce a product by the third quarter of 1984, Matra Harris will offer the product and two Japanese manufacturers will introduce the product by the end of 1984. While the product is of great interest to manufacturers of government electronics systems, first shipments will be to commercial equipment. Consequently, we believe that most of the packages will be dual in-line. We believe the leaded chip carriers will be the next most common package, particularly for the 28 to 68 pin range. In general, we believe that high density systems with standard logic and packages up to 80 pins will be manufactured with a combination of small outline (SO) and leaded chip carriers.

Our projected shipment forecast is still very conservative for the 80C86 and related microprocessors. This is not because we don't believe there is a market for the products, but that we believe that production capability for the industry will take some time to develop. These are the reasons:

- Harris is not yet a volume producer of CMOS VLSI commercial products. We estimate that they have shipped a total of 180 thousand of their much less complex 6100 CMOS microprocessor in 1981.
- Intel is still developing their CMOS process. It is the first process they have developed without the benefit of a memory product to take into production. We expect there may be delays in production start up of this process.

- We expect 1 1/2 to 2 years after introduction by several suppliers (at least Harris and Intel) before production volumes will start because of the design-in time for new systems.

1 Mbit ROM:-

The average selling prices have been revised downward for 1984 and 1985. We expect 1986 and 1987 prices to be as we projected last quarter. Of the three companies presently offering the part, Hitachi appears to be the only one who has a product targeted at the computer market. The Oki design is very large (1 sq. inch) and the NEC design is very slow (3 microseconds). While Hitachi's die size is large at 79K sq. mils, they have incorporated ECC as a yield enhancement approach. As a result, they expect to be able to support prices in the 25 tO 30 dollar range during the next two years. The Hitachi product will be available in a 28 pin pakage versus NEC's 40 to 52 pin configurations. One point that came out of my survey was that the Hitachi product has very high standby power relative to their 256K ROM. The 256K has 30 micro amperes maximum standby versus 10 milliamperes for the 1 megabit part. The 1 megabit part does have lower maximum active power (80 ma) than the 256K (30 ma) on an equivalent basis.

I have nothing new to report for the 64K static RAM.

FORECAST OF WORLDWIDE CONSUMPTION
(units, dollars in millions unless otherwise stated)

		1983		1984		1985	
		1st Half	2nd Half	1st Half	2nd Half	1st Half	2nd Half
1Mbit ROM (CMOS)	1	0	S	S	0.5	1.2	2.8
	2	0	-	-	15.0	33.0	67.0
	ASP	0	-	-	30.00	27.50	23.90
64K SRAM (CMOS)	1	1	2	5	10	17	33
	2	32.0	43.0	55.0	80.0	110.5	165.0
	ASP	32.0	21.50	11.0	8.0	6.5	5.0
16-bit Micro-Processor (CMOS)	1	0	S	20K	55K	.1	.3
	2	0	0	.5	.85	1.4	3.4
	ASP	0	0	25.00	15.45	14.00	11.30

S = Sample quantities; 1 = units; 2 = U.S. dollars

FORECAST OF PACKAGE DISTRIBUTION
(percent of unit shipments)

		1983		1984		1985	
		1st Half	2nd Half	1st Half	2nd Half	1st Half	2nd Half
1Mbit ROM (CMOS)	D	-	-	100	100	100	100
	F	-	-	-	-	-	-
	L	-	-	-	-	-	-
	C	-	-	-	-	-	-
64K SRAM (CMOS)	D	100	98	96	96	93	93
	F	-	-	1	1	2	2
	L	-	2	3	3	5	5
	C	-	-	-	-	-	-
16-bit Micro-processor (CMOS)	D	-	-	90	90	95	95
	F	-	-	-	-	-	-
	L	-	-	10	10	5	5
	C	-	-	-	-	-	-

Codes:
D = DIP; F = FP; L = LDC; C = CHIP

cc: Bud Mills

:tg

Nielsen Dataquest

INQUIRY RESPONSE

DATE: June 20, 1983

TO: Del Morsette &
Norm Kelly/Altos Computers

FROM: Stan Bruederle

This information has been compiled in response to your inquiry of June 1983

Please file in Section 2 for future reference.

Subject: 1. Projected 256K DRAM Prices and Availability
2. Standard PAL Availability

1) This is our projection of 256K dynamic RAM shipments and prices from 1982 through 1986. We are projecting the price per bit cross over point with the 64K dynamic RAM will be 1986.

Year	256K Unit Shipments (millions)	256K A.S.P.	64K A.S.P.	Production Suppliers
1982	Samples	$80.00	5.05	
1983	.7	$50.00	3.75	Fujitsu, Western Electric
1984	10	$25.00	2.90	NEC, Toshiba, Oki, Intel Mostek, T.I., Micron Tech.
1985	65	$12.00	2.20	Motorola, AMD, Mitsubishi
1986	300	7.00	1.80	

Note: Volume production will begin in late 1983 with most of the 700K units shipped in the fourth quarter.

This should help you with your decision for your next design.

2) I checked with MMI regarding the availability of standard speed PALs. They are continuing to manufacture that product. Someone at Anthem apparently became confused by a series of occurances that happened recently. MMI has set prices of all PALs of the same series to be the same regardless of the speed/power specification (you are probably aware of that). A few weeks ago the standard devices were in short supply for a brief time. MMI told their salesmen and distributors to suggest to customers that they use the half power advanced design devices as an alternative since they have the same speed specification. Apparently someone at Anthem interpreted this to mean that they weren't supplying standard speed devices any more.

Since shipments are growing so rapidly you can expect periodic shortages to occur. You should determine if you can use the standard speed and half power advanced design alternately.

Nielsen Dataquest

INQUIRY RESPONSE

DATE: March 25, 1983

TO: Jean Claude Bassiere
Telemecanique

FROM: Stan Bruederle
Manager SUIS

This information has been compiled in response to your inquiry of March 1983

Please file in _____ for future reference.

There are presently three manufacturers of FAST Logic. Fairchild originated the family and presently produces 57 types. Signetics and Motorola are alternate sources. Signetics produces 19 types while Motorola produces 11. Fairchild is planning to have 80 types available by the end of 1983 while Signetics and Motorola are expected to have about 60. All companies will be emphasizing MSI and LSI functions and plan to have 120 to 140 types in their families. Texas Instruments is an indirect competitor with the advanced schottky 74AS family. This family has not been as well received by customers as FAST. Dataquest believes that in the next two to three years TI will make the 74AS family compatible with FAST and become a fourth source. We have not included TI in our forecast at this time.

Prices of FAST devices are presently 30 to 50 percent higher than comparable schottky TTL types. We expect FAST prices to approach parity with 74S equivalent types by 1985. Averages selling prices for the FAST family will always be higher than for the schottky 74S family because of a larger mix of MSI and LSI types.

FAST LOGIC MARKET DATA
Worldwide Sales (millions)

	1980	1981	1982	1983	1984	1985
Total Dollars	2	10	25	50	100	170
Numbers	1.6	10	33	71	154	283
ASP	1.25	1.00	.75	.70	.65	.60

WORLDWIDE SHARE
(millions of dollars)

	1980	1981	1982	1983	1984	1985
FAIRCHILD	2	10	24	41	60	85
SIGNETICS	-	-	1	7	25	55
MOTOROLA	-	-	-	2	10	30

FAST LOGIC SHIPMENTS BY GEOGRAPHY
(percent)

	1980	1981	1982	1983	1984	1985
U.S.	100	90	80	70	60	60
EUROPE	-	10	15	20	30	30
JAPAN	-	-	5	10	10	10

This is a permanent copy for your files of our telex to you dated March 25, 1983.

cc: Bud Mills/DQ - Paris

SAB/pg

2. Semiconductor Trends

This section discusses trends in the semiconductor industry. It considers changes in the cost of information processing, the changing product life cycle, general semiconductor technology trends, and the technological trends for specific types of semiconductor devices. This section also covers the developments in manufacturing technology and their future direction.

COST OF INFORMATION PROCESSING

The growth of the semiconductor industry has been predominantly fueled by the rapid decline in the price of semiconductors. Figure 2-1 gives an example of this. It shows the decline in price per function for integrated circuits rather than the price changes in specific devices. The y-axis is a log scale and shows a decline from a price of more than $1.00 per function in 1964, to less than 0.1 cents in 1980. DATAQUEST expects this trend to continue.

Section 8 of this volume gives a more detailed discussion of the factors involved in the price decline, as well as current cost models for specific devices.

PRODUCT LIFE CYCLES

Standard and semicustom semiconductor products follow the traditional life cycle stages of development, introduction, growth, maturity, market saturation, decline, and phase-out. For integrated circuits, the relative length of these phases has been changing. The development time of many complex products, such as microprocessors and speech synthesis chips, is increasing, while the growth, maturity, and saturation phases are decreasing in length. Because the life cycle of many semiconductor products is seven years or less, macroeconomic factors, such as recessions, have a major effect on their duration. Figure 2-2 illustrates a typical IC life cycle.

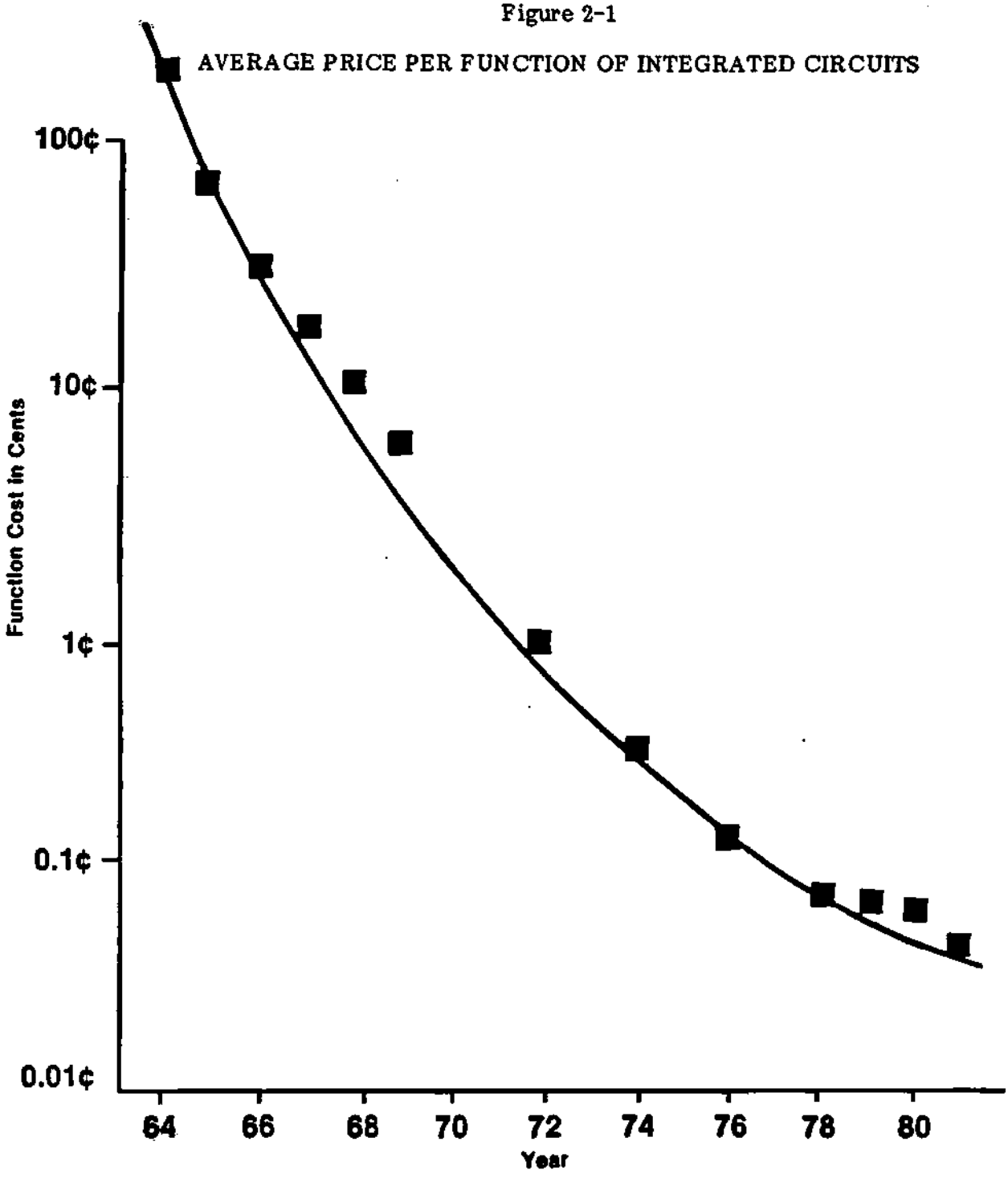
It is important that procurement personnel be aware of the suppliers' planned life cycles for each of the semiconductor products and families being used.

During the development stage, the product may be sampled (market tested) and refined, more than once in the case of many complex LSI circuits. The supplier races the calendar, knowing that the profitability of a potentially high-volume product can be adversely affected by a delay of only a few weeks because of competition. Increased interest in their domestic semiconductor industries by several governments in recent years has intensified the competition, causing many semiconductor companies to enhance their market research during the development phase, and to evaluate new product introduction decisions more carefully.

2. Semiconductor Trends

Figure 2-1

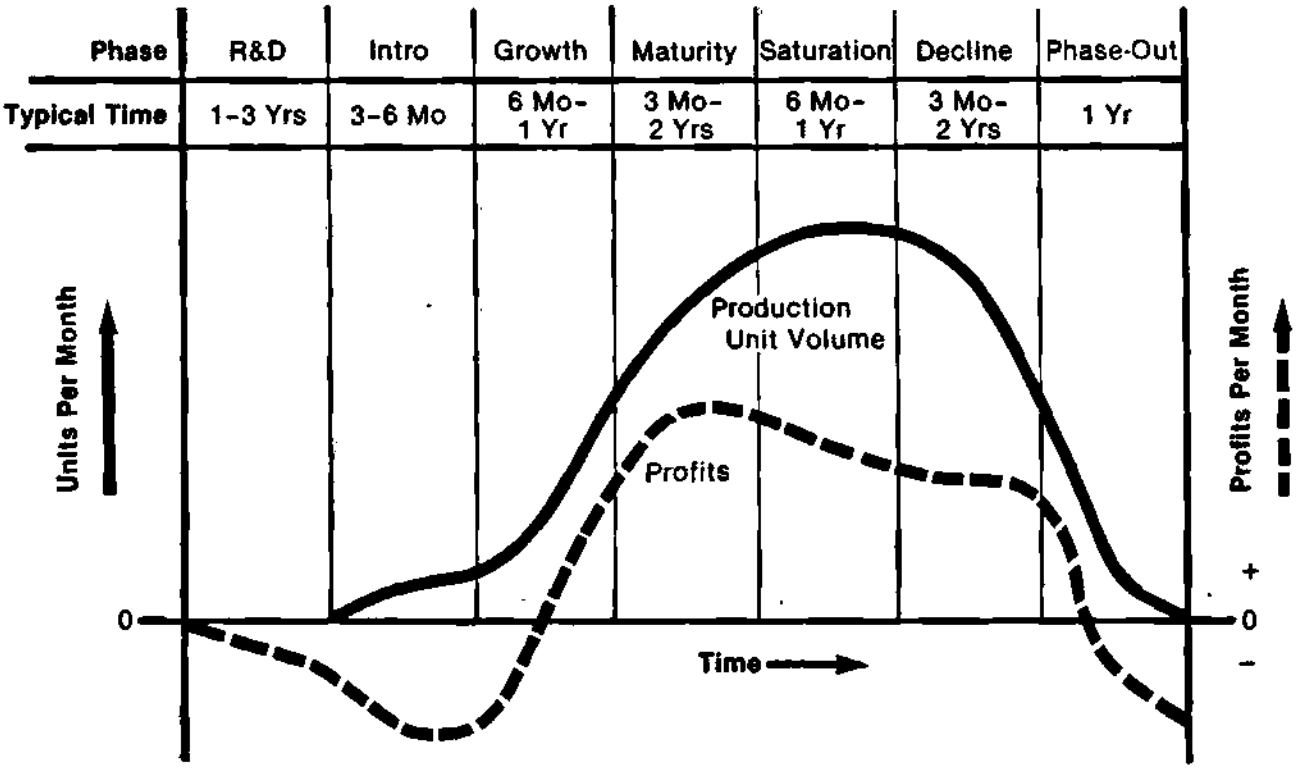
AVERAGE PRICE PER FUNCTION OF INTEGRATED CIRCUITS



Source: DATAQUEST, Inc.
April 1982

Figure 2-2

TYPICAL INTEGRATED CIRCUIT LIFE CYCLE



Source: DATAQUEST, Inc.
April 1982

2. Semiconductor Trends

During the introduction phase, potential large-volume customers perform qualification tests on the product. The test sample may vary from 10 to 100 devices, in the case of a new microprocessor, to 1,000 to 5,000 devices in the case of a dynamic RAM. The complexity and cost of the device usually dictates the quantities used in the sample. These tests usually include accelerated life tests involving burn-in (e.g., 500 to 2,000 hours at 70°C to 125°C) and actual equipment usage conditions. Semiconductor products, particularly LSI and VLSI products, are almost universally unprofitable during this phase.

During the growth (production buildup) phase, the supplier attacks production yield problems, and often increases yields by a factor of three to ten. This period is usually characterized by significant price decreases as the suppliers seek long-term user commitments, so that production facilities can be sized and capacity allocated appropriately. The first one to four suppliers of a device may become profitable during this phase if competition is not too intense.

As the semiconductor product matures, product cost reductions are implemented. These usually take the form of die shrinkage (circuit scaling and other refinements), or package cost reductions (introduction into CERDIP and/or plastic). Production tests are often refined during this phase as another cost reduction mechanism. Some customers run additional qualification tests during this phase, and some suppliers who come into the market at this point may offer price reductions as an incentive to be allowed to participate in qualification tests. Such activities can lead rapidly to the saturation phase of the life cycle.

During the saturation phase, there is a shakeout of suppliers. Customers who hedged against shortages by qualifying a large number of suppliers may be forced to choose from a lesser number when placing volume production orders. These commitments range from approximately three to six months in a soft market (weak economy), to one to two years in a strong market (economic upswing). Suppliers who remain profitable and can afford the capacity commitment usually maintain their production volumes. The less competitive suppliers often retreat to lower volumes at acceptable pricing levels, or shift their capacity to other products.

The product phase-out stage dictates that lifetime purchasing requirements be established in advance of production shutdown by the supplier. The best protection against phaseout surprises is frequent communication between supplier and user. Many suppliers have implemented formal obsolescence procedures including advance notification to the supply channels and to direct customers. The cost of failing to shut down production of a product at the appropriate time can easily exceed $1 million per month (if a process or if diffusion furnaces are involved). The user should be sensitive to the cost involved before requesting that a supplier extend the production life of a semiconductor device.

2. Semiconductor Trends

Awareness of semiconductor product life cycles makes it possible to provide the necessary feedback to the research and development, design components, test engineering, quality control, and manufacturing activities of the user's organization to avoid product usage too early or too late in the life cycle. Some of the major factors that affect semiconductor life cycle length and timing are:

- Technology changes:
  - Device and circuit innovations; e.g., single transistor RAM cell, EEPROM, NVRAM
  - Process evolution; e.g., scaled NMOS, silicon gate CMOS
  - Revolutionary processes; e.g., gallium arsenide (GaAs)
- Economic factors:
  - Extreme pricing pressure on suppliers; e.g., 64K RAM in 1981
  - Excessive number of competitors relative to total volume demand; e.g., 16K RAM in 1981
  - Soft market causing acceleration of new product introductions; e.g., 64K CMOS EPROM and 256K RAM in 1982
- Manufacturing constraints:
  - Phaseover to new production equipment; e.g., from obsolete tooling used for older products, or from 3-inch to 4- or 5-inch wafers
  - Delays in availability of new test or production methods; e.g., projection alignment equipment in 1978-1979

It is not unusual for an IC product to be introduced, to mature, and then to become obsolete in three years, especially in such products as semiconductor RAMs, EPROMs, and ROMS. This can adversely affect the market position of the semiconductor user's end product. The best protection against this occurrence is for the user to work with the supplier base to anticipate the next one or two generations of product evolution. This would allow for incorporating the next generation of semiconductor devices into the final product with minimal engineering changes.

2. Semiconductor Trends

TECHNOLOGY TRENDS

The pace of technological advancement is increasing and several trends in the technology are evident, each of which will shape the semiconductors of the future. These include:

- Increasing pervasiveness of CMOS structures
- Fine-line processing—many new products introduced in 1982 and 1983 will be based on 2.0 micron and 2.5 micron geometries
- Increasing research and development activity in GaAs ICs including LSI
- "Systems on chips"—single-chip microcontrollers, 32-bit microprocessors, and similar functions
- Complex processing, allowing the integration of high-level digital and analog functions on a single chip; e.g., speech synthesizers

These trends are driving the proliferation of product functions, as described next.

TRENDS IN SEMICONDUCTOR PRODUCTS

The year 1982 is significant in the evolution of semiconductors. Only 35 years have passed since the invention of the transistor, and already the 64K dynamic RAM is considered a commodity item. The cost of a 64K dynamic RAM was less than 20 millicents per bit before the end of 1981, and approached 10 millicents per bit by mid-1982. Progress is accelerating in all areas of technology. This section concentrates on some of the product trends.

Integrated Circuits

It is convenient to classify integrated circuits by process technology and function. This section will discuss trends in bipolar digital, MOS digital, and analog integrated circuits.

Bipolar Digital Circuits

Bipolar digital integrated circuits evolved from the earliest forms of Resistor Transistor Logic (RTL) gate structures. The earliest gates had gate delays in the range of 100 nanoseconds, and consumed approximately 100 milliwatts of power per gate. By 1970 bipolar memory arrays were replacing these earlier gate structures.

2. Semiconductor Trends

Bipolar RAM development continued during the 1970s and early 1980s. The earliest arrays of 4 x 4 storage elements evolved into today's ECL RAMs containing as many as 4,096 bits on a single chip. Currently, several companies produce 16K bipolar PROM devices, and at least two companies have announced 4K x 8, or 32K, bipolar PROMs.

One of the primary user benefits of bipolar memory technology is wide temperature operation. Many manufacturers offer devices that operate over the full temperature range of -55°C to +125°C. Bipolar memory is expected to continue to enjoy a niche market where high performance and wide temperature operation are required and where the very highest performance is required in commercial temperature range applications. However, the medium- and slower-speed bipolar RAMs are being displaced by lower-cost, high-speed MOS devices, such as 16K NMOS and CMOS static RAMs.

Bipolar logic technology has benefited from fine-line lithography, ion implantation, and other innovations in semiconductor processing. During 1981, several companies announced advanced low-power Schottky logic families that, in time, will displace part of the market for standard and Schottky TTL devices. Several companies have announced and are producing field-programmable logic arrays (FPLAs) or programmable logic array devices (PLAs). These devices are user-programmable, and provide the advantages of reduced parts count and decreased number of part types inventoried. In addition, the user realizes some measure of design security by being able to program the devices in-house.

MOS Digital Products

By far the largest market for semiconductor products has developed around MOS memories, microprocessors, and logic devices. The year 1982 marks the eleventh anniversary of the MOS microprocessor, and already four companies are in the advanced development and marketing phases on 32-bit microprocessors. MOS memory density is now in the 256K bit range for both RAMs and masked ROMs. UV-erasable EPROMs of 64K bit density are in volume production. In MOS logic, there is keen competition among a growing number of suppliers to enter the gate array business. Current product announcements describe devices of greater than 5,000 gate density, and research and development programs are under way to push this number well beyond 10,000 within the next two to three years.

Memory Devices - The most intense competition in semiconductor history was observed in 1980 and 1981 in the 16K dynamic RAM market, as prices plunged from more than $6 per unit to spot market pricing of less than $1 in two years. By early 1982, at least four manufacturers were in volume production on 64K dynamic RAMs, offering 150 nanosecond maximum access time performance, 16-pin packaging, and bit costs approaching 10 millicents a bit at the component level. By late 1981, at least one supplier was sampling the 256K dynamic RAM.

2. Semiconductor Trends

The advent of 64K dynamic RAMs led to increased usage of redundancy at the chip level. Customer acceptance of devices incorporating this technique is growing. Both IBM and Bell have made use of redundancy in their 64K and higher density RAM designs, and the non-captive suppliers are gradually introducing devices containing redundancy. For example, the incorporation of redundancy in a wide range of memory devices was discussed at the 1982 International Solid State Circuits Conference (ISSCC). Redundancy has been reported to increase yield from the range of 5 percent good die per wafer up to the range of 15 percent good die per wafer at the 64K RAM level. Such improvement in yield is obviously helpful in supporting memory pricing at 10 millicents per bit and below. At least three techniques are being used to implement redundancy: metal fuse links, polysilicon fuse links, and laser beam techniques. There is continuing controversy as to which method is best.

Static RAMs using NMOS and CMOS process technology are increasing in density and performance. Several suppliers now offer 16K bit density devices that function with access times of 55 to 70 nanoseconds. At least three suppliers use redundancy techniques in implementing static MOS RAMs. The controversy over whether CMOS or NMOS is the best technical approach to static RAMs will continue. While CMOS offers lower power consumption at the 16K bit level, there is a cost difference that results in somewhat higher pricing for a given performance level.

At least five suppliers now offer electrically erasable programmable read-only-memories (EEPROMs). EEPROMS provide an advantage over UV-erasable PROM devices because they do not have to be removed from the user's system in order to be erased and reprogrammed. At least one supplier has collected reliability data indicating that EEPROMs are capable of 100 years of read operation and 10,000 or more erase-write cycles under normal operating conditions.

Microprocessors - Microprocessors and single-chip microcomputers are diverging somewhat in their development trends. Microcomputers are becoming more features-oriented, while microprocessors are emphasizing improvements in speed.

On each succeeding generation of single-chip microcomputers the on-board memory, both RAM and ROM, is increasing. Current devices have 4 Kbytes of on-board memory, and the next generation is expected to include 8 Kbytes of on-board memory.

The main limitation to the development of microcomputers is in their packaging technology. Devices are currently produced in 40-pin packages. We expect a 68 lead chip carrier to become the standard package.

Microcomputers are particularly features-oriented. We expect the inclusion of primitive network interfaces on the chip in the near future. Such a device would be valuable for both communications and ease of testing.

2. Semiconductor Trends

We expect the trend in process technology to be toward CMOS rather than NMOS. CMOS offers the advantages of high speed and low power consumption. Currently 80 percent of microcomputers are NMOS, but by 1985 we expect production to be 50 percent NMOS and 50 percent CMOS. Microcomputers are also moving away from on-chip EPROM and toward on-chip EEPROM. This eliminates the need for a UV-transparent window, and means that an inexpensive plastic package can be used.

The continuing trend in microprocessor devices is toward very high-speed processors. Eight-bit microprocessors are expected to become more sophisticated, with architectures and instruction sets compatible with 16-bit microprocessors.

DATAQUEST believes that future 16-bit microprocessors will evolve into virtual memory architectures. This type of device reduces the amount of physical memory required and provides a low-cost, high-performance system based on modern, cost-effective peripherals. The human/machine interface of such a machine is good, and the total system cost is lower than that of a linear memory architecture.

The growth in the 16-bit microprocessor market has been slower than was anticipated. DATAQUEST expects that the 16-bit microprocessor market will be refined to the point where there are two or three major device families.

Intel introduced a 32-bit microprocessor in 1981. It is significantly different from current 16-bit devices, and uses a multi-chip architecture. Several other companies are expected to introduce 32-bit devices, but the long acceptance time of 16-bit devices suggests that it will be some time before 32-bit microprocessors are widely used.

The trend toward processor-independent software, such as that based on UNIX or CP/M, could have a significant effect on the user's selection of a microprocessor. This will give users more freedom of choice among the various devices on the market.

Gate Arrays

At least 40 companies have entered the gate array manufacturing business. Most of them offer CMOS and some offer bipolar gate array devices. The trend toward CMOS has been driven by the need for low-power operation, such as in equipment containing batteries for portable operation or for back-up in case of main power failure. Another important aspect of the trend toward CMOS involves the power dissipation of complex functions. Where 2,000 or more gates are required on a single chip, the speed of operation may dictate the use of CMOS rather than NMOS because of the difference in power dissipation. For gate arrays to become generally useful, at least five problem areas must be overcome:

- Computer-aided design (CAD). Where CAD is used, the equipment used by both the customer and the gate array manufacturer must be compatible.

- Second sourcing. Most customers require the availability of a second source if they are to commit to a gate array.

- Packaging. Gate arrays typically require packages with a high pin count. Such package types must be readily available.

- Testing. The scarcity of test engineers available to write adequate test programs, and the time required to write such programs, may be limiting factors in the use of gate arrays.

- Manufacturing turnaround time in production. As the use of gate arrays increases, the lead times for their production may vary dramatically.

While it is true that logic errors and interconnect errors should not occur in array design, human nature dictates that such errors do occur. Perhaps the biggest factor contributing to the success of the higher cost PROMs and EPROMs in both bipolar and MOS technology is their ability to correct design errors and other human errors quickly and at very low cost using programming equipment within the user's facility. Gate array technology must offer rapid, low-cost solutions to such problems if it is to be accepted on a similar scale.

Major advances have been made recently in MOS VLSI in the areas of speech synthesis and telecommunication circuits. During 1981, algorithms were implemented for generating words of speech using only a few hundred bits per word, and progress was made in the application of digital filtering techniques to speech regeneration.

Analog Integrated Circuits

Continuing evolution in linear and other analog integrated circuits has resulted in improvements in the following areas: low noise bipolar operational amplifiers, higher-density and higher-resolution converters, and system level data converters.

Amplifiers

At least four companies have introduced new operational amplifiers featuring low noise of 12 $nV/(Hz)^{1/2}$ or less. DATAQUEST expects that the evolution of operational amplifiers will continue, and that laser trimming and refinements in zener trimming will allow noise voltages to be reduced even further than the 3 $nV/(Hz)^{1/2}$ that represent today's state-of-the-art.

Voltage Regulators

Integrated circuit voltage regulators are available for an increasing variety of operating conditions. By 1980, some production monolithic regulators were capable of operating at limits of 5 amps and 33 volts (positive) with output range adjustable

from 1.2 to 33 volts. Wider output ranges of up to 57 volts were achievable at 1.5 amps maximum. By 1980, negative voltage regulators were capable of regulating at any value between -1.2 to -4.7 volts at 1.5 amps maximum output current. Currently available package types include TO-3, TO-5, and TO-39 hermetic headers, and TO-92, TO-202, and TO-220 plastic cans.

Analog to Digital—Digital to Analog (A/D—D/A) Converters

CMOS technology has recently been applied to the implementation of flash converters for video signal multiplexers and other applications. The result is a device that is as fast as comparable bipolar converters, with the additional benefits of higher packing density and lower power consumption.

The first CMOS flash converter was introduced in 1981. It features a resolution of 8 bits, power dissipation of 250 mW, 20,000 square mil chip size, and 15 MHz sampling rate.

CMOS technology has been applied to high-resolution A/D and D/A converters. The state-of-the-art today is 16-bit D/A converters and 14-bit A/D converters on single chips. The recent trend is toward the use of PROM or EPROM elements on the chip for accuracy trimming. D/A converters will continue to have higher resolution on chip than A/D converters for the foreseeable future because the chip must integrate a large digital successive approximation circuit with precision analog circuits, and because constraints are imposed by the physical size of the resistor ladder network.

Data Converters

There is a trend toward higher levels of integration to include elements that were previously located off-chip. Such devices offer lower cost, higher system speed, or better system noise performance because buffers, drivers, and inter-connections are incorporated on a single substrate. The chip may also include reference sources, scaling resistors, temporary storage latches, and other elements allowing direct interface with microprocessors. DATAQUEST expects these trends to continue.

V/F—F/V (Voltage to Frequency—Frequency to Voltage) Converters

The trend in V/F and F/V circuits is toward refinements in frequency response and accuracy. By 1978 monolithic devices operating in the 10 KHz to 1 MHz range were available. Improvements in temperature stability and linearity characteristics continue to be made. The present state-of-the-art is represented by devices such as the Analog Devices voltage-to-frequency converter AD 650, which has an output frequency of up to 1 MHz with a non-linearity characteristic of 10 parts per million (ppm).

2. Semiconductor Trends

Discrete Devices

Many of the material processing and manufacturing techniques used in LSI and VLSI lend themselves to the improvement of discrete devices, resulting in smaller, higher-performance components. Application of these techniques has enabled the General Electric R&D Center to develop a power MOSFET capable of conducting 60 amperes with an on-resistance of 0.014 ohms and a blocking voltage of 60 volts. Die size is 300 mils x 300 mils. General Electric has also developed a recessed gate JFET capable of blocking up to 400 volts and having a unity power gain cut-off frequency above 500 MHz.

In power field-effect devices, breakdown voltages now exceed 1 kilovolt (kV). Power MOSFETs are expected to displace bipolar transistors in such applications as switching power supplies and motor control. Bipolar technology will continue to dominate in the area of thyristor switches for the foreseeable future.

Other advances in power field-effect transistor (FET) technology have resulted in solid state replacements for electro-mechanical relays used in military applications. Such devices make it easier for the system designer to accomplish interface with the other elements in the system comprised of VLSI circuits and other ICs. This trend will continue, making it easier for microprocessors to interface with low-level analog devices such as thermocouples and other transducers.

N.V. Philips has implemented a thyristor gate turn-off capability with the ability to switch 5 amps at 1.5 kV. The state-of-the-art for high-power switching SCRs is represented by AEG-Telefunken's production devices, with ratings of 930 amps average on-current and a blocking voltage of 2 kV.

The use of gallium arsenide (GaAs) technology in microwave applications has resulted in devices that operate above the 8 gigahertz (GHz) range. At 8 GHz a gain figure of 14 decibels (dB) and a noise figure of 1.1 dB have been achieved. At 12 GHz a gain of 6 dB with a maximum noise figure of 3.5 dB have been realized. The use of electron beam lithography and multi-layer metallization are expected to provide for further refinement of these figures.

The trend in microwave diodes has been toward higher frequency, higher sensitivity, and lower noise. Schottky barrier, silicon varactor, and gallium arsenide varactor techniques have been applied. Current state-of-the-art devices operate at frequencies up to 40 GHz.

Optoelectronics

With the advent of fiber-optic technology and its increasing use in communications applications, optoelectronic technology is expected to develop even more rapidly than in previous years. The joint effort by the Japanese Ministry of International Trade and Industry (MITI) in the development of optoelectronic GaAs devices is also expected to speed up technological innovation.

2. Semiconductor Trends

LED Lamps

Developments in LED lamp technology are mainly in the areas of brighter lamps and more varied colors. Red and green have been the most readily available colors up to the present, but amber lamps are also available and Matsushita and Sanyo both announced blue LED lamps in 1981.

LED Displays

The developments in LED lamps in terms of brightness and color variation are also being seen in LED displays. However, displays are also becoming more sophisticated in terms of their drivers. The drivers are integrating more functions onto a single circuit. For example, a TRW Optron device includes on-chip circuitry to control a display's brightness in response to ambient light conditions.

Liquid Crystal Displays

Although not truly semiconductor devices, LCDs are usually considered along with semiconductor optoelectronics. LCDs have virtually replaced LED displays in calculators and digital watches. Trends in LCDs are toward assorted colors, which are produced by using dichroic guest-host materials. The speed at which LCDs can change is still a limiting factor in the potential uses for these devices.

Optocouplers

Optocouplers, also called opto-isolators, provide economical, high-performance solutions to problems caused by ground loops and by induced common mode noise for both analog and digital applications. Developments in industrial controllers and robotics should cause increased demand for these devices. DATAQUEST anticipates improvements in both speed and gain in these devices.

Other Optoelectronics

Advances in the use of fiber optics in communications applications are expected to enhance the development of optoelectronic devices, especially transmitters and receivers for fiber optic data transmission.

Imaging and image-sensing is another fast-growing segment of the optoelectronics field. Charge-coupled devices, discussed later in the Emerging Semiconductor Products part of this section, are finding wide application in the field of imaging. Other image-sensing developments include the use of RAM arrays in imaging applications. Infra-red image sensors are being developed and are of special interest for military applications.

The choice between laser-based and capacitance-based video disk systems has not yet become clear. Laser-based systems would stimulate demand for laser diodes. A number of Japanese companies are also developing laser diodes, emitting visible light, for audio disk playback.

2. Semiconductor Trends

DATAQUEST anticipates a trend toward lower-cost packaging for optoelectronic devices and a continuing decline in ASPs for commodity optoelectronic products.

Emerging Semiconductor Products

While silicon continues to be the mainstay of all facets of semiconductor production, there is increased activity in gallium arsenide (GaAs), bubble memory, and Josephson junction technologies. DATAQUEST believes that continuing research and development and market analysis in these areas is vital to the future of the semiconductor industry.

Gallium Arsenide Technology

Silicon technology is firmly entrenched for digital applications and will remain so for most users for many years. GaAs is a relatively expensive, ultra-high performance, low-density alternative semiconductor approach to signal processing that has previously been limited to microwave analog applications. However, the performance advantage promised by higher electron mobility (eight times that of silicon) has intrigued researchers for many years.

DATAQUEST expects GaAs to be used in a growing number of digital applications in the near future. Chip development and applications work are already under way at Fujitsu, Hewlett-Packard, Rockwell, and other companies. The Japanese Ministry of International Trade and Industry (MITI) has established a joint government and business research laboratory with a number of major Japanese semiconductor manufacturers. The purpose of the venture is to develop optoelectronic integrated circuits based on GaAs technology. The Japanese government is investing $78 million in the project, which is scheduled for completion in 1986. Present research and development activities should lead to products such as random access memories with densities up to 1,024 bits and cycle times of less than two nanoseconds, within the next two years.

Both Hewlett-Packard and Rockwell have developed depletion mode GaAs processes. Rockwell has implemented a 32 x 32 bit imaging array, and is working on charge-coupled GaAs devices expected to be capable of information processing more than one billion multiplications per second. Hewlett-Packard has developed an MSI GaAs word generator capable of 5 Gb data rates. Lockheed and McDonnell-Douglas have reported static GaAs devices utilizing both enhancement and depletion mode devices to implement random-access memories. Fujitsu is planning to use GaAs technology to implement a super high-speed computer. Fujitsu has developed high electron mobility transistors that reportedly approach the speed of Josephson junctions without having to operate at temperatures near absolute zero.

In the analog area, DATAQUEST expects increasing competition for the potential market of over 30 million receiver/down converters for use in television sets receiving direct satellite broadcasts. Additional large markets are developing for military applications in high-speed communications, higher-performance radar, and ECM systems.

Previous limitations restricting the application of GaAs technology were:

- Costly starting material (wafers)
- Difficulty in obtaining high purity starting material
- Wide variations in device characteristics causing very low manufacturing yields

These limitations are being overcome by the development work in crystal growth and by the use of ion implantation to replace conventional diffusion. The Czochralski method of crystal growth has replaced the Bridgeman method, resulting in a reduction of impurity levels. Ion implantation provides more accurate control of doping levels during manufacture than does conventional diffusion, and minimizes channeling effects because lateral diffusion is eliminated.

Charge-Coupled Devices (CCD)

The technology of CCD integrated circuits has progressed rapidly since the introduction of the first linear image sensors in 1974. In the late 1970s, several suppliers developed arrays of 64K density, directed toward low-cost serial/parallel digital data storage applications. These programs were curtailed in favor of bubble memory, which offered non-volatility and was more cost-effective than CCD at high densities (one megabyte).

Recent activities in CCD are directed toward programmable filters, 1,000 and 2,000 element linear arrays, and matrix imagers for TV and solid state camera applications. Devices capable of 484 x 380 resolution and 74 dB signal-to-noise ratio for TV applications were available by 1981, and several companies are directing R&D efforts toward resolution acceptable to 35mm camera users. DATAQUEST expects the emergence of solid state camera products utilizing CCD technology in the near future.

Video delay lines are now available that are capable of 2,000 samples at 20 to 50 MHz, and the announcement of larger linear arrays is expected in 1982. CCD will find many other applications, such as electronic eyes in robotics equipment.

2. Semiconductor Trends

Bubble Memory

Current producers of bubble memories are Fujitsu and Hitachi in Japan, and Intel and Motorola (both merchants), and Western Electric (captive) in the United States. Japanese companies have about 57 percent of the worldwide market for these devices, with terminals and telecommunications equipment used by Nippon Telephone and Telegraph (NTT) as the principal application.

When Texas Instruments and National Semiconductor decided to drop out of the bubble memory market, it created some confusion for both users and suppliers of bubble memories. DATAQUEST believes that Texas Instruments and National Semiconductor chose to deploy their resources in other programs whose anticipated return on investment was higher.

DATAQUEST believes that there is a viable market niche for bubble memories. The most attractive applications will be those that use the special characteristics of the device, which include non-volatility high density and relative insensitivity to hostile environments. Japanese companies plan to enter the U.S. market during 1982.

Josephson Junctions

For many years IBM and others have devoted research and development activities to Josephson junction (JJ) technology. This technology takes advantage of the superconductivity of materials at temperatures very close to absolute zero. Data based on laboratory experiments and computer simulations indicate that a power-delay product of 125 attojoules (10^{-18} joules) is achievable. This figure is at least three orders of magnitude lower than that of GaAs devices. DATAQUEST believes that several years or more will be required before JJ technology is commercially feasible.

MANUFACTURING TECHNOLOGY TRENDS

Semiconductor manufacturing operations may be divided into the following categories, representing the sequence in which they are performed:

- Wafer fabrication, including the photolithographic steps, furnace operations, ion implantation, and metal deposition
- Wafer probe testing, including any required laser trimming or fuse-burning operations

- Assembly, including scribing, sawing or breaking, die attachment, and package assembly and sealing operations

- "Final" test, including AC and DC checks, related fusing operations if required, and any infant mortality removal operations

The trends in manufacturing in the late 1970s have been toward moving wafer fabrication and wafer test facilities away from Silicon Valley, and toward relocating as many final test operations as possible to the assembly site (Southeast Asia for most commercial products). Automation of VLSI operations may slow the latter trend for some applications.

Trends in Wafer Processing

By the end of 1982, more than 200 stepping projection aligners will be installed worldwide, driven primarily by the marketplace for 64K dynamic RAMs. Many laser-trimming machines are being installed by 64K dynamic RAM and high-density static RAM manufacturers, for use in breaking connections to defective cell rows or columns. Five-inch (125mm) fab equipment is considered the current production state-of-the-art, and is expected to remain so into the mid-1980s.

CMOS processes are proliferating, and manufacturing processes are becoming more complex to accommodate the added steps. Dual-layer metal is becoming more popular for gate arrays and other VLSI applications. Silicon, not sapphire or garnet, is expected to remain the basic raw material into the late 1980s.

Dry etching is becoming standard in an increasing number of applications, but there are still problems with uniformity. The use of ion implantation is allowing fundamental process changes, and may soon eliminate the need for epitaxial deposition associated with buried layer formation.

Photolithography improvements will allow the majority of processes to shift from today's 3.5 micron to 4.0 micron range, to 2.5 microns to 3.0 microns by 1985. Some submicron processing based on X-ray lithography will be in high volume operation by that time.

The trend toward automation continues, with air-bearing transport systems, automatic cassette loading/unloading, and other robotics gaining in popularity. Traffic control is receiving increased attention, since humans are the main cause of clean room contamination.

A typical wafer fab facility today costs more than $400 per square foot to build and equip. This cost will exceed $500 per square foot before 1985. Thus, equipment size reduction is increasingly important.

2. Semiconductor Trends

Semiconductor Assembly Trends

With the exceptions of some military programs and isolated high-technology commercial applications, semiconductor assembly operations ran at approximately 90 percent of capacity during 1981. As a result, package material suppliers and assembly equipment suppliers had a difficult year and competition grew more intense.

The increased expenditures for military and government electronics, especially hybrid microelectronics, allowed some assembly subcontractors to continue expansion programs. The other bright spot in 1981 for semiconductor packaging was in the area of high-density pinout packages for VLSI circuits.

Automation of assembly operations is continuing. Tape Automated Bonding (TAB) technology is being extended to VLSI chips with lead counts of 80 or more. Robotics will be applied to automated assembly with increasing frequency during the next few years. General Electric, Fujitsu, and other companies have major efforts under way in this area.

MANUFACTURING TRENDS

Significant changes are taking place in the way semiconductor manufacturing plants are sited, constructed, equipped, and staffed. This section summarizes these changes and highlights their important aspects.

Facility Site Selection

A significant trend is the move away from the established semiconductor areas such as the Santa Clara Valley in California and the Houston-Dallas areas in Texas. In these areas, job opportunities are still abundant but the wealth generated by the industry has increased the price of available housing such that technical staff cannot afford it, limiting the incoming population flow. The price of real estate for expansion of manufacturing facilities has also risen sharply.

During the past five years, the established semiconductor manufacturers have looked elsewhere to begin new operations. New locations include Santa Cruz, Sacramento, Lodi, Santa Rosa, and Rancho Bernardo, California; Portland and Corvallis, Oregon; Orem and Salt Lake City, Utah; Austin and Arlington, Texas; Colorado Springs, Colorado; and Chandler, Arizona.

Technology and Equipment

The trend toward greater device complexity (in excess of 256 kilobits of memory per device) and larger die size has been intensified by lowered defect

densities. As device geometries approach the 2 micron level and below, processing, environmental, and equipment technologies must come together.

Of the many process technologies that have arisen, photolithography has been one of the key factors in determining the pace of very large scale integration (VLSI) design and manufacture. The trend has been away from contact printing and toward proximity and projection printing. Dry etching techniques are being developed as a necessary concomitant of projection printing in order to etch fine patterns in a variety of materials. Ion implantation techniques have kept pace in order to achieve, quickly and inexpensively, control of impurity concentrations and junction depths. Clean room facilities in 1982 are geared toward Class 100 rating rather than the Class 1,000 rating that was acceptable until 1978. Deionized (DI) water is being elaborately treated and tested to meet the new clean standards. The water is pretreated through activated carbon and diatomaceous earth filters before it goes through reverse osmosis and deionization stages.

Although it is complex and expensive and requires longer delivery times, wafer fabrication and related equipment is proving to be cost effective. The equipment is increasingly controlled by integrated circuits. The result is greater automation, control, and reproducibility of results, as well as lower defect levels due to lower operator-wafer interfacing.

These technological advances have made possible higher wafer processing rates and lower die costs.

A facility processing 10,000 wafers out per period, at a manufacturing cost of $80-$150 per wafer with gross revenues of $300 to $1,000 per wafer, can realize at least $3 million dollars per period.

Although in 1982 4-inch wafers are the predominant wafer size, equipment purchases for today's use must be chosen to handle 5-inch and 6-inch diameter wafers. With the high capital cost of some equipment, care must be taken to obtain maximum usage of such equipment while it is in service.

Plant Layout and Design

Several factors determine the way in which a particular plant is laid out. The space allocated and the relationships among pieces of equipment are determined by:

- The technologies employed and the available equipment to realize them
- Line balance resulting from a particular product mix
- Resulting material and process flow

- The volume of product scheduled out per period
- The particular constraints imposed by city building codes that, in the main, are designed for operator safety

There are, however, other factors that profoundly affect plant layout:

- Cleanliness for VLSI production is influencing the decision about which portion of the equipment remains in the clean room. Only the loading end of diffusion furnaces are being allowed in the clean room. The heat and dust generating portions are being separated from the clean room by a fire wall. The same is true for ion implanters, and the trend will continue for other equipment where appropriate.
- Servicing of equipment and work stations in old facility designs meant frequent entry of personnel into the clean room to deliver bottles of chemicals, replace furnace tubes, and repair plumbing. New layouts obviate the need for these entries by surrounding the clean room with a service corridor from which all plumbing and most maintenance can be done. Furnace tubes can be pulled and replaced behind the fire wall and outside the clean room.
- Philosophies of equipment design have shifted toward single wafer and in-line processing and wafer handling, away from the purely batch-type handling. Thus, there is greater interplay between different processing areas (as opposed to the strict quarantine that existed before) as long as cleanliness is maintained, material flow is facilitated, and cross-contamination is avoided. New demands for material accountability have made production control supervision the heart of the entire operation and this fact has also affected the overall layout. Increased use of computers and terminals will make this an even more effective approach.

Manufacturing Processes and Methods

Increased pressure for production economies, higher productivity, device reliability and yield, and the stringent demands of complex fine geometry devices have resulted in several developing trends in semiconductor manufacturing.

Automation

Perhaps the most persistent and pervasive trend is toward automatic sequencing of events. Also popular is the drive toward computer automation for

control, reproducibility, and data collection and analysis. The benefits include:

- Less wafer handling
- Process monitoring and control
- Correct process sequencing
- Proper routing of material
- System self-diagnostics and self-correction
- Data collection for off-line processing
- Elimination of paper work
- Material accountability (especially useful since lot sizes vary for different operations in the manufacturing process)

Automation now exists in the areas of diffusion/oxidation, physical and chemical vapor deposition, ion implantation masking, alignment, maskmaking, mask inspection, testing, plasma etching, and environmental monitoring.

Exciting as it is, the prospect of a fully computerized, semiconductor manufacturing facility is not foreseen before the mid-1980s, although an experimental automated line has been constructed at Texas Instruments, and automated production lines are used by several captive manufacturers. The determining element is equipment development. Although much of the equipment today is being "updated" by adding microprocessors for sequencing, very few pieces of equipment are designed with adequate consideration for the computer interface.

Computer terminals are common in today's wafer fab areas. Their major function is to provide management information about each lot of wafers being processed and the specific process variables required for that lot. These terminals have largely done away with the set of documents (travelers) that used to accompany each lot of wafers through wafer processing.

The development cycle for very sophisticated equipment can range from two to five years. Delivery times of equipment costing more than $200,000 often range from nine to eighteen months. Development costs are also often high, as is the rate of obsolescence. Hence, only the largest merchant and captive manufacturers are pursuing the concept of the fully automated factory of the future.

2. Semiconductor Trends

Wafer Handling

Batch processing will probably not disappear in the foreseeable future. However, more and more equipment manufacturers are offering cassette-to-cassette wafer systems to eliminate tweezer and vacuum probe handling. Manual handling of wafers is a well-known cause of damaged patterns, silicon particle generation, and wafer defects. In properly automated equipment, each wafer is subject to almost the same set of process parameters.

Energy and Resources Conservation

Manufacturers are implementing the following operations to conserve energy and other resources:

- Diffusion/oxidation furnace temperatures are being reduced to a lower holding temperature when not in use and at the end of high temperature processing. Not only does this practice conserve electrical energy, but it also helps to avoid silicon crystal damage.

- Deionized water is being reclaimed at great savings to the manufacturer and society. Water for chilling is being stored for re-use.

- Organic chemicals and precious metals are being collected after use and resold for reclamation.

- Plasma dry etching and stripping are saving one-third to one-half of net processing costs, compared with wet processing methods.

- Projection printing is resulting in considerable economies in mask costs. Whereas a mask used for contact printing can be used on 50-100 wafers before being discarded, a chrome master, starting out with defect levels of approximately 1 defect per square inch, can be used on up to 100,000 wafers with final defect levels not much above the starting values. Since defects are transmitted back and forth between mask and wafer during contact printing, higher device yields and reliability result from projection printing. Equipment costs are usually justifiable within about a year, based on mask cost savings alone at current production levels.

Environmental Control

The manufacturing environment has become the focus of intense monitoring and control procedures. Some of these measures have already been discussed under the heading Plant Layout and Design. Clean rooms are being established as Class 100, and more care is being taken with the room's ceiling materials, paint, tile

composition, material flow, personnel movement, and gear. "Bunny suits" expose the wearer's face and hands only, and plastic booties are becoming the standard. Operators (perhaps the primary source of contamination) access the production floor by passing through air showers. Air-handling units must be adequate to provide more positive pressurization in the areas most sensitive to contamination. The return air ducts must be sized and spaced to avoid noise and turbulence and must be smoke-tested for assurance.

Janitorial training and service are being addressed with greater care. Hoods and sinks are designed with consideration for janitorial service. Wafers are stored in clean boxes on wire mesh racks under laminar flow hoods fitted with ion generators.

Much of the new equipment is highly sensitive to temperature, while many processes already sensitive to humidity are becoming more sensitive to particulate contamination. The monitoring and control of these aspects of manufacturing are of the utmost importance to manufacturing managers concerned with high yields. Sensors are located strategically around the production floor, and readouts are sometimes shown on computer terminals.

Apart from the production area, the general environment is a subject of continuing concern. Social and economic pressures have resulted in a goal of limiting the amount of chemical effluents, both liquid and gaseous, that are discharged into the environment. Thus, dry processing, computer-controlled chemical dispensers, and energy resource conservation are all part of the continuing program to preserve the living environment.

Human Engineering

This facet of manufacturing addresses operator health and safety. Some aspects of health and safety precautions are legislated, but optimization beyond legal standards often results in higher productivity. More care is being taken to detect and reduce acid and solvent fume levels. The colors of equipment, walls, and floors are chosen to keep operators comfortable and productive. Noise levels in equipment and air handling units are difficult to reduce except by design. High noise levels are known to reduce productivity in the short term and to affect operators adversely in the long term.

Another aspect being more closely studied is the velocity of air flowing past the operator. Too rapid a flow of air is not only unhealthy, but also results in turbulent dissemination of particulates around the room.

Staffing

The cumulative effects of the recessions of 1970 and 1974 are now evident in the acute shortage of trained engineering staff. The trend toward decreased

enrollment in engineering colleges since these recessionary periods has not been reversed at rates compatible with industry growth. For those engineers who remained, it has become a seller's market. In Santa Clara (Silicon) Valley, California, unemployment at 4.7 percent in September 1979 was at a five-year low, unparalleled anywhere in the country. At the lower end of the wage scale, turnover rates among operators ranged from 50-100 percent per year. Many semiconductor companies maintained a policy of no layoffs throughout 1981, to avoid a recurrence of the 1976-1977 "labor crunch" as economic conditions recover and strengthen in 1982-1983. Labor shortage problems are also being addressed by providing child care centers in industrial parks, enabling more women to join the work force.

Nielsen Dataquest

INQUIRY RESPONSE

This information has been compiled in response to your inquiry of June 1983

Please file in Section 3.0 for future reference.

DATE: June 7, 1983

TO: Hewlett-Packard
Jim Lee

FROM: Stan Bruederle
Manager Semiconductor User Information Service

Subject: Hewlett-Packard Position as Semiconductor User.

This list is our estimate of 1981 and 1982 semiconductor purchases of the largest semiconductor purchasers in the U.S. and Europe. We are going to be updating this in more detail this summer and will have more accurate data is September/October.

Purchases from Merchant Market
Millions of Dollars

	1981	1982
IBM	$400	$450
Western Electric	$300	$300
General Motors	$200	$170
Philips	$200	$180
Siemens	$180	$170
Texas Instruments	$175	$175
Atari	$150	$130
Hewlett Packard	$140	$155
Honeywell	$130	$130
G.E.	$130	$130
Digital Equipment	$130	$140
Sperry	$110	$110

:pg

3. Semiconductor Procurement Challenges

The rate of change in our environment is continually increasing. Electronics technology has multiplied human capabilities, and is having a greater impact on society than did the Industrial Revolution. Nowhere is this impact more evident than in the semiconductor industry where product life, frequently measured in decades in other industries, is measured in years or months. Rapid obsolescence is a way of life. The semiconductor buyer faces unique challenges.

PROCUREMENT IN THE 1980s

The classic procurement functions are:

- To establish and maintain a continuity of supply to support development and production schedules
- To minimize material inventory consistent with corporate safety and economic advantage
- To avoid material duplication, waste, and obsolescence
- To maintain material quality standards based on suitability for use
- To acquire material at the lowest cost consistent with required quality and service
- To maintain the company's competitive position and conserve profits from the standpoint of material costs
- To analyze and inform management about long-range costs and availability of major or critical material
- To continually seek new and alternative procurement procedures and material, the adoption of which might enhance corporate profitability or efficiency, or both

These functions are representative of any procurement activity, whether it be part of a competitive corporation, a utility or other monopoly, a military activity, or a government agency. In some cases the term "profit" should be replaced by "economic advantage" to enhance the meaning of the function to the organization.

Challenges to semiconductor procurement in this decade include:

- The gestation period of new semiconductor products now approaches and sometimes exceeds the product life.
- The production lifetime of an electronic system often far exceeds the product lifetime of the semiconductor devices from which it is made.

3. Semiconductor Procurement Challenges

- While the rate of inflation experienced in recent years may lessen, the economic uncertainty that tends to increase the real cost of money may not, thus heightening the need for an effective procurement activity.
- In some cases the internal IC supply of captive manufacturers has not met expectations—this increases the pressure on the procurement function across the market.
- It may not be possible for present sources of semiconductors to expand at a rate sufficient to cope with increased demand, thus dictating the need for additional suppliers.
- During a soft economic period, new product introductions are made by semiconductor users and suppliers as a means of gaining a competitive edge. This may force the need for changes in the supplier base as a result of evolutionary or revolutionary changes in semiconductor needs.
- Raw material shortages develop in each economic upturn, causing severe changes in lead times for critical components. Labor shortages may contribute to the resulting problems.
- Changes in ownership of one or two suppliers may affect the total supply of some devices, necessitating a review of the supplier base.
- Many governments are taking an increased interest in the semiconductor capabilities of their domestic corporations. This will affect the competitive relationships of suppliers as efforts to alter import/export balances are increased.

THE COST OF MONEY

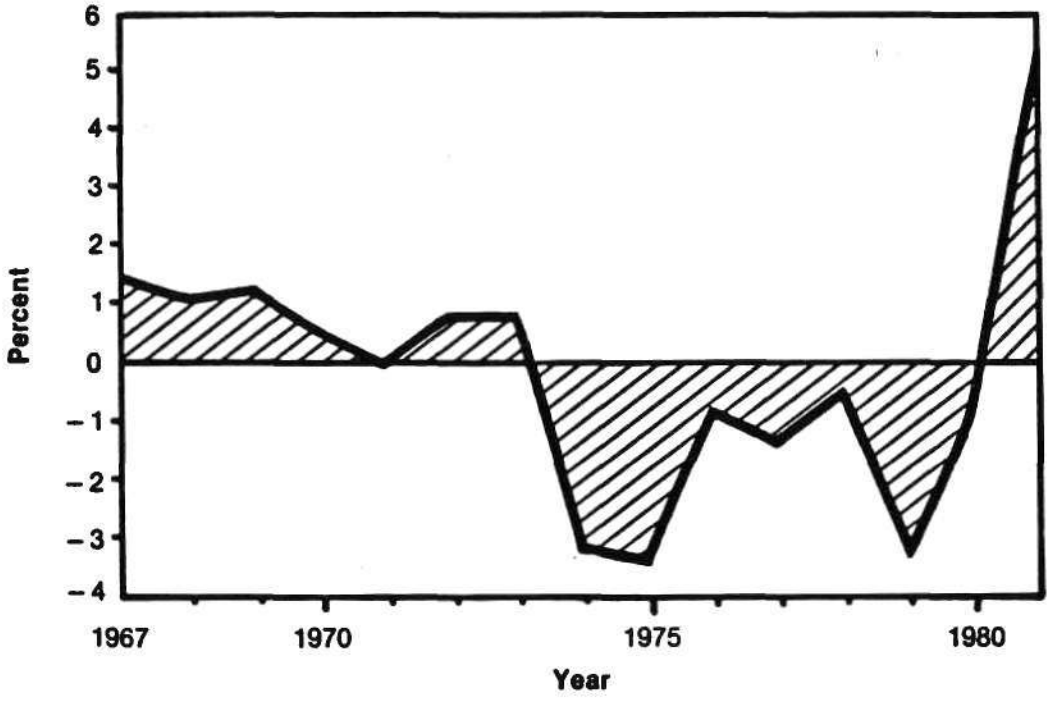
Corporations are vitally interested in the cost of money. Financial management is often as big a challenge as procurement. Floating currencies, varying interest rates, varying tax structures, inflation, and other economic uncertainties contribute to the difficulty of determining the cost of money. One facet of the "real" cost of money is addressed here in some detail because of the future impact of the cost of money on semiconductor procurement. The particular measure discussed here is, however, only one of several methods that may be used to measure the cost of money.

A popular notion in the business world has been that the real rates of interest in recent years normally were approximately 3 percent higher than the inflation rate. The chart in Figure 3-1, based on data from the U.S. Federal Reserve Board and the Bureau of Labor Statistics, shows that the concept is unfounded.

3. Semiconductor Procurement Challenges

Figure 3-1

REAL INTEREST RATE
(Percent)



This figure shows the average rate for 3-month Treasury bills minus the year-to-year percentage change in the Consumer Price Index.

Source: U.S. Government Statistics
DATAQUEST, Inc.
April 1982

3. Semiconductor Procurement Challenges

The real interest rate shown in Figure 3-1 was derived by subtracting the average change in the consumer price index from the average interest rate for three-month U.S. Treasury bills and plotting the resulting difference for the time period 1967 through 1981. The plot shows that until late 1980, only once in 15 years did the value approach 2 percent, and that the total area between the curve and the axis was negative. Of more importance, and a major issue for the near term, is the fact that the real interest rate has risen by 9 percent since 1979 and exceeded 5 percent during 1981. This means that the real rate of interest no longer allows loans that can be repaid in currency depreciating faster than the nominal rates charged by lenders. Thus the needs for inventory controls, careful scheduling, and well-managed procurement activities are greater today than ever before in the history of the semiconductor industry.

The method described here is only one of a number of methods for evaluating factors related to the cost of money, and does not apply equally across the electronics industry. The semiconductor user should evaluate the real cost of money as it relates to the particular business conditions the user faces, and plan procurement funding accordingly. Appendix E provides a data base that may assist the user in this activity.

PROCUREMENT TIMING

Many corporations gear their procurement activities to their fiscal calendars. Usually some latitude is provided to allow purchasing discretion in taking advantage of changing market conditions. This is most frequently noticed in soft economic conditions, when a "spot" market develops. However, there are major advantages to be gained by using a longer-term procurement cycle that extends beyond the fiscal year.

Two approaches are possible:

- A project-oriented procurement cycle, with major milestones
- A three- or five-year procurement program, updated annually and reviewed quarterly

The project-oriented cycle suits large-scale government and military programs as well as the start-up firm that is founded initially to develop and produce one or a few major products and services. Some examples of major procurement milestones are:

- Review of suppliers—request for information (RFI) activity

3. Semiconductor Procurement Challenges

- Initial selection of supplier base
- Requests for quotations (RFQ) made and responses submitted
- Prototype awards made
- Qualifications completed
- Production releases made
- Periodic reviews of supplier performance
- Final production and spares orders placed

The project-oriented approach usually results in a high level of supplier support because it provides long-term visibility and frequent feedback. Some of the disadvantages of this approach include:

- A lack of synchronization with the suppliers' business planning cycles
- No provision for rapidly changing market conditions, which, therefore, must be handled on an exception basis

The three- or five-year plan approach is better suited to a well-established multiproject or multidivisional company that has sufficient resources to fund and support a corporate procurement activity. If the level of business justifies doing so, synchronization with suppliers' activities is simplified by staging quarterly review meetings and alternating the meeting locations between the supplier's facility and the purchaser's facility. Quarterly reviews also provide a forum for addressing rapid changes in industry conditions such as increasing lead times, product obsolesence, and materials shortages.

HOW THE PROCUREMENT FUNCTION AFFECTS SUPPLIERS' COSTS

Almost all interactions between the semiconductor buyer and seller have economic implications. This section discusses some of the ways in which the procurement function may have beneficial or detrimental effects on the suppliers' costs of doing business.

Specification Requirements

Suppose a company decides that it wants to use the "industry standard" 64K bit NMOS dynamic RAM for a particular application. Design engineering and

components engineering personnel are then faced with the challenge of defining "industry standard" in a meaningful way. The equipment being developed will be required to function over a range of environmental conditions, and the buyer is responsible for arranging a production volume flow of parts acceptable to manufacturing.

So long as the desired specification limits fall within the capabilities of multiple suppliers, "industry standard" does not pose a supply problem, unless the entire industry is in an undercapacity condition, or the buyer's lead time requirements are too short. Supplier costs are not adversely affected in this case.

It is possible, however, that insufficient attention to detail will result in one or more suppliers' parts being rejected at incoming inspection or at production test. In the case of the 64K dynamic RAM, a standard data sheet specifies approximately 20 DC parameters, approximately 40 AC parameters, and several timing diagrams, with numerous footnotes. Without an engineering background it is very difficult to comprehend the meaning of all these data, so oversights and misinterpretations are not uncommon. Writing a procurement specification frequently adds to supplier confusion, and should be done only when the higher cost of vendor compliance is more than offset by the overall cost savings to the user. Every line item in a procurement specification should be carefully scrutinized and properly justified before the specification is imposed on suppliers, because compliance affects semiconductor yields and yields affect semiconductor cost and availability.

Specification Mix

Again using the example of the 64K RAM, specification mix is an important cost factor. There are at least three variations in the access time specifications of this product, e.g., 120, 150, and 200 nanoseconds (ns). If the specification for all of the products the user requires is skewed significantly from the center of the production distribution, yield is adversely affected. An example is a user requiring only 120 ns parts from a supplier whose center of yield distribution is at 150 ns. Such a requirement means that early in the product life cycle the user may not be able to get sufficient volume delivery, and later will pay an excessive premium for the product.

Other Cost Factors and Control Methods

Some of the effects of procurement on suppliers' costs are less obvious than those previously described. Examples are:

- Order quantity and value
- Number of device types required

3. Semiconductor Procurement Challenges

- Number of line items on order
- Delivery constraints
- Monitoring activities (e.g., expediting of status)
- Documentation requirements
- Product marking constraints
- Special processing
- Inspection requirements

Each of these aspects, if carefully reviewed prior to order placement, may be optimized to reduce semiconductor procurement costs. Many companies are using materials review planning (MRP), manufacturing resources planning (MRP II), and distribution resources planning (DRP) as techniques for addressing the costs of these and other factors involved in procurement and ownership of semiconductor products.

EFFECTS OF TECHNOLOGY TRENDS ON PROCUREMENT

A substantial factor in the growth of the semiconductor industry has been the rapid pace of technological development. Procurement decisions should be made with consideration of current technology trends.

Increasing Levels of Integration

The increasing complexity of integrated circuits has had a profound effect on procurement activities. Procurement personnel are often involved in the complex issues of CAD, silicon software, EPROM versus masked ROM tradeoffs, and other factors that did not exist in the days of core memory and discrete switching transistors. Today one must "speak the language" of integrated circuits. The Glossary at the end of this volume is designed to aid those who must cope with the increasing number of "buzzwords" and technical jargon resulting from the explosive growth of the IC industry.

As a result of the trend to VLSI usage in more and more systems, the procurement issues are more complex than ever. It is essential that a close working relationship exist among the material, research and development, product

development, and manufacturing engineering functions, because the costs of errors in judgment are skyrocketing. A single bit reversal in a 128K bit ROM mask can cost thousands of dollars and two months or more schedule slippage. An error in gate array logic can be even more costly, depending upon the nature of the error and whether or not it is detectable before the end-user equipment is shipped.

When selecting a supplier base it is important to establish the suppliers' abilities to meet the full range of user needs. For example, a 1975 procurement activity may have been responsible for purchasing more than one million pieces of TTL SSI/MSI per year and very few LSI products. Today, the quantities may have decreased for the TTL devices but could exceed one million pieces of LSI. This could dictate a change in supplier base. With the recent increase in startups in Silicon Valley and elsewhere, the issue is increasingly more important.

Standard Versus Non-Standard

The tradeoffs involved in deciding whether to purchase custom, semicustom or standard devices are becoming more complex. An example of semiconductor technology tradeoffs involves the decision whether to use EPROMs or masked ROMs. This is usually an economic decision and the factors to be considered in this case include:

- Number of patterns used
- Total volume of devices required
- Number of devices per month per pattern type
- Anticipated number of engineering changes during equipment lifetime
- Number of sources required
- Cost of EPROM programming equipment and labor
- Bit density requirements
- Design (bit pattern) security needs
- Reliability needs

This subject is addressed in greater detail in Section 5, Technology Tradeoffs.

3. Semiconductor Procurement Challenges

JAPANESE IMPACT ON THE SEMICONDUCTOR INDUSTRY

During the 1970s, several major Japanese companies directed their long-term strategic planning toward increasing their share of the rapidly growing worldwide semiconductor marketplace. By the late 1970s, these plans began to materialize as companies including Fujitsu, Hitachi, NEC, Oki, and Toshiba began volume deliveries of high-density, high-performance memory devices such as 16K and 64K dynamic RAMS. The Japanese companies first emphasized availability, then quality, and currently technology in their promotional activities. Many Japanese companies have established marketing, design, and manufacturing facilities in the United States and in West European countries to facilitate their market penetration. Throughout this time, these companies have maintained an aggressive marketing approach, making use of native salespersons motivated to lead pricing, while at the same time avoiding an appearance of "dumping product" (which in the United States is illegal). Other Japanese marketing tactics have included the purchase of major advertising sections in respected publications and publicizing new products at technical symposia.

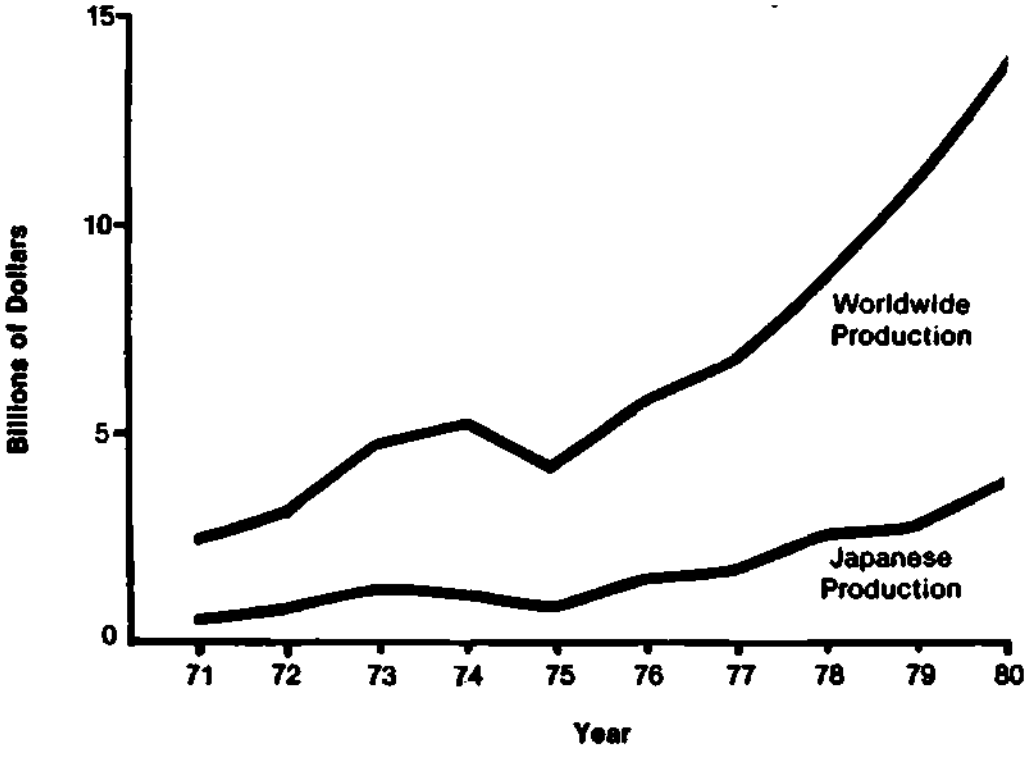
It is important to note that at present none of the Japanese companies successfully competing in the semiconductor industry were originally organized for that purpose. They are all successful in other lines of business and have the financial resources required to make the necessary continuing investment to penetrate this field. Equally important is the fact that under Japanese law and in the Japanese financial community capital formation by these companies is easier than in most other free world countries. This implies that Japanese semiconductor market participants will intensify the economic pressure on non-Japanese semiconductor firms for the foreseeable future.

The Japanese Ministry of International Trade and Information (MITI) works closely with Japanese semiconductor manufacturers to fund research and development programs. The current project, started in 1979 and due for completion in 1986, is for the development of an optoelectronic integrated circuit. MITI will invest $78 million over the course of the project, which is also supported by nine Japanese manufacturing companies. The research undertaken includes work with GaAs substrates.

Examples of the Japanese companies' progress in semiconductor market penetration are given in Figures 3-2, 3-3, 3-4, and 3-5.

Figure 3-2

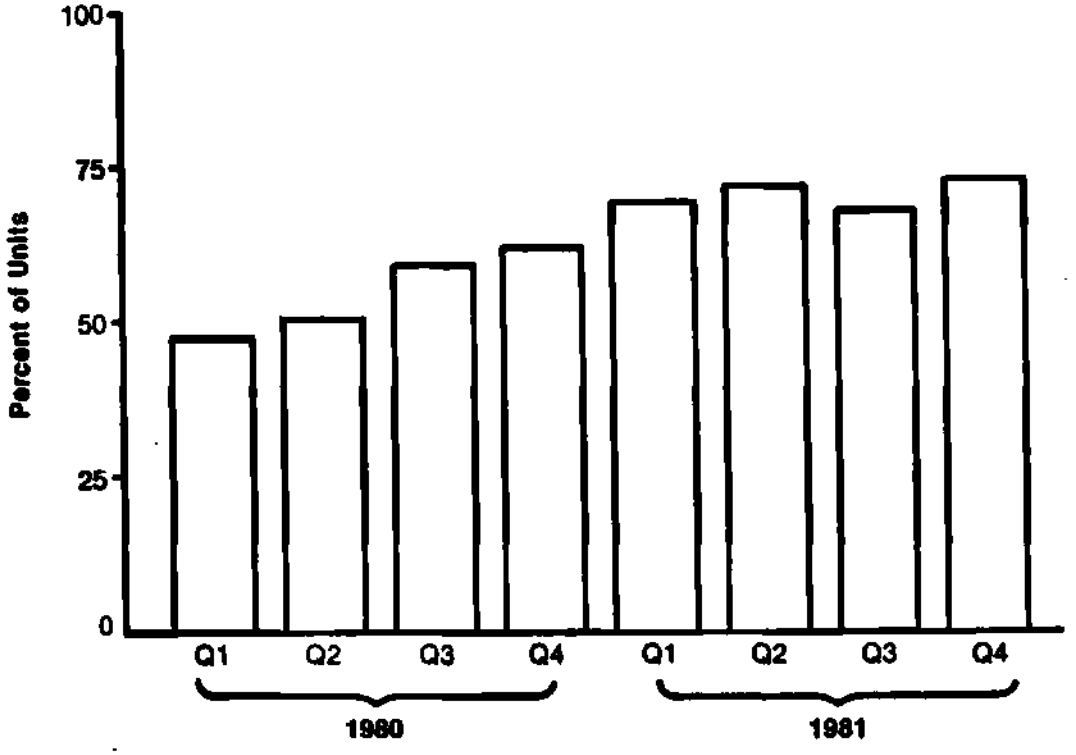
SEMICONDUCTOR PRODUCTION BY
JAPANESE COMPANIES
(Billions of Dollars)



Source: DATAQUEST, Inc.
April 1982

Figure 3-3

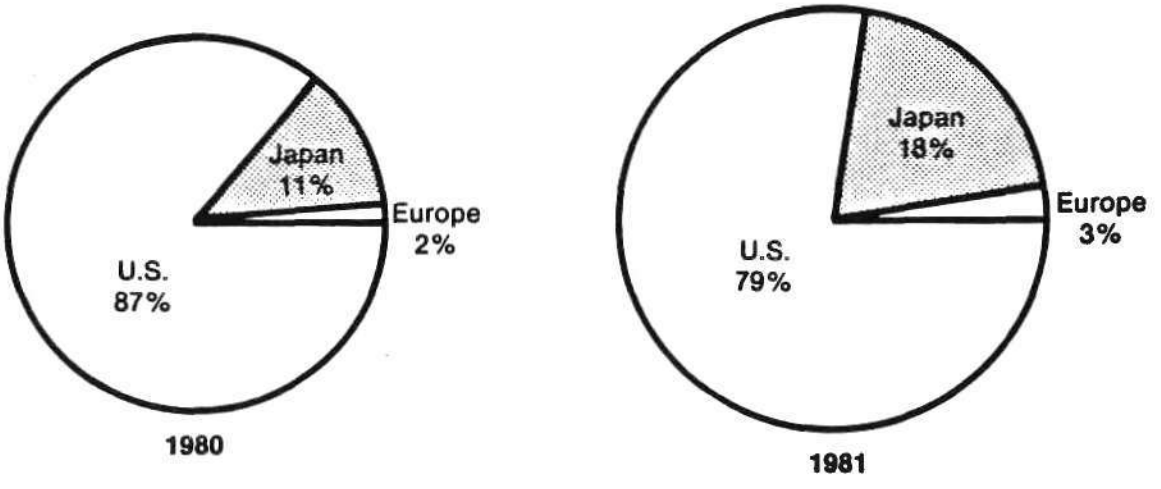
JAPANESE COMPANIES' GROWTH IN 64K RAM MARKET SHARE
(Percent of Units)



Source: DATAQUEST, Inc.
April 1982

Figure 3-4

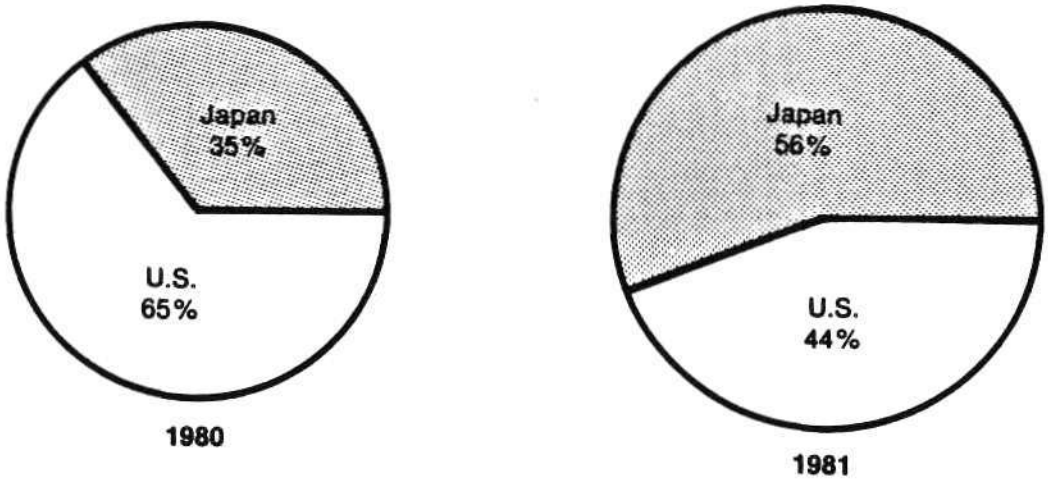
JAPANESE COMPANIES' GROWTH IN 8-BIT MPU MARKET SHARE
(Units)



Source: DATAQUEST, Inc.
April 1982

Figure 3-5

JAPANESE COMPANIES' GROWTH IN
4-BIT MCU MARKET SHARES
(Units)



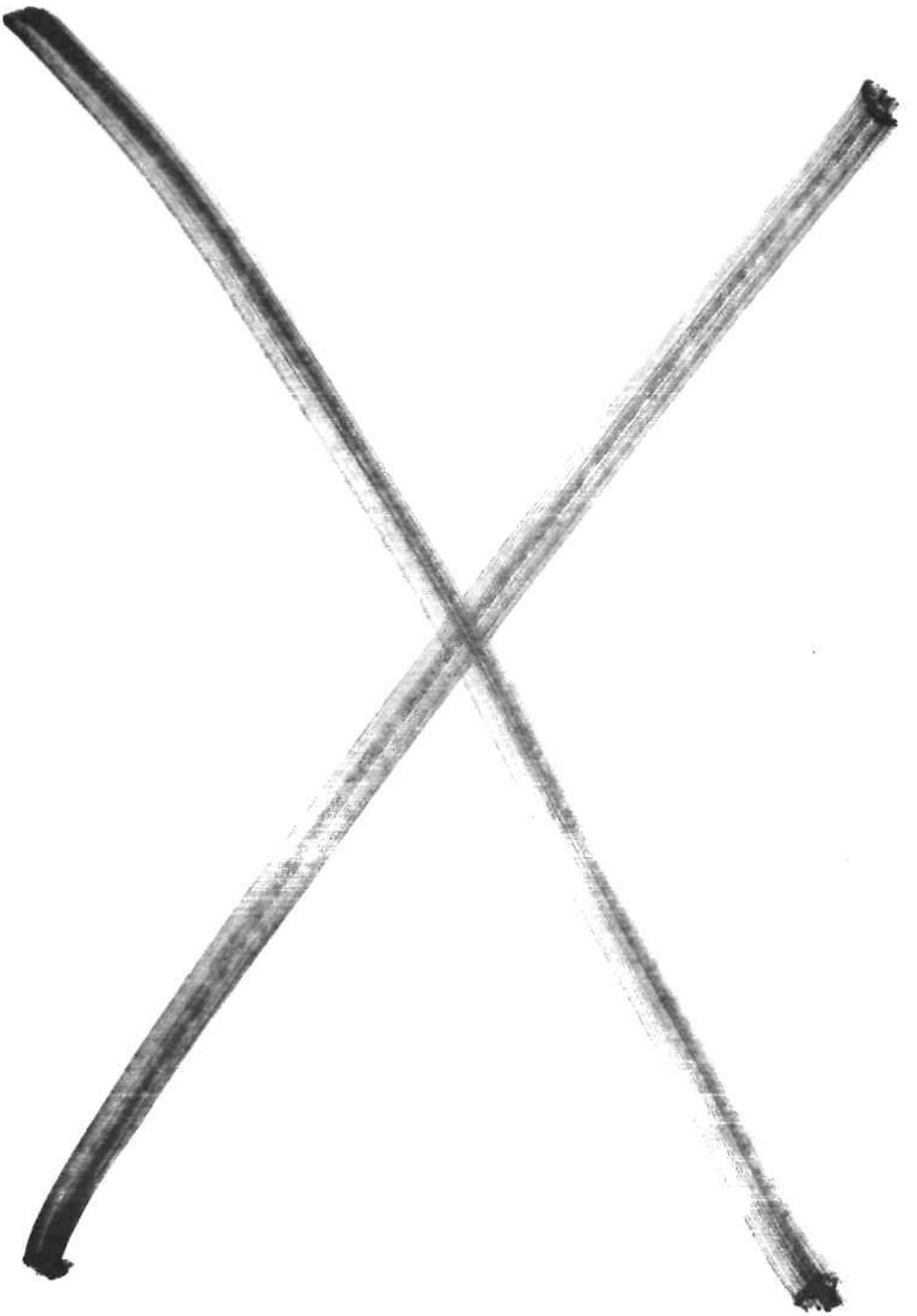
Source: DATAQUEST, Inc.
April 1982

3. Semiconductor Procurement Challenges

COPING WITH THE CHANGES

We have addressed a number of challenges, issues, and changes unique to semiconductor usage in the preceding discussion. The semiconductor user can cope with these challenges:

- In-house by:
  - Organizing for efficiency
  - Consolidating needs and buying for the corporation, not just for one project or one division
  - Automating highly repetitive tasks—low-cost distributed computing has made these tasks easier:
    - Preparation of complex RFQs
    - Comparison of complex quotes
    - Scheduling and schedule revisions
    - Planning—scenario development
    - Budgeting
    - Data base management
- When working with suppliers by:
  - Increasing knowledge of the semiconductor industry and its participants
  - Analyzing potential suppliers more carefully at:
    - Management interface
    - Technical interface
    - Sales interface
  - Improving internal and user/supplier communications
  - Building long-term relationships with suppliers, based on compatible business strategies, economic volume levels, and competent technical and business teamwork
  - Measuring and reporting on the quality of mutual commitments, and providing for feedback in both directions via periodic supplier reviews



Nielsen Dataquest

INQUIRY RESPONSE

DATE: 4/5/84

TO: Joe Campbell/Spinnaker Software

FROM: Mary Olsson/Dataquest

This information has been compiled in response to your inquiry of April 1984

Please file in Sec. 4, Vol. 1 for future reference.

Subject: OTP EPROMs. Who manufactures OTPs in 64K and 128K. Prices of OTPs and projected trends.

PROMs are basically Bipolar. They are manufactured with fuse-link technology and can only be programmed once, with the customer doing the programming. OTP EPROMs are fabricated with a metal oxide process. OTP EPROMs can only be programmed once by the customer.

Table 1 shows the estimated average selling prices of one-time programmable (OTP) EPROMs.

Table 1
One-Time Programmable EPROMS (OTP)
Average Selling Prices

	1983	1984	1985	1986	1987	1988
32K	3.50	2.00	1.75	1.75	1.75	N/A
64K	6.00	3.75	2.50	2.00	1.85	2.00
128K	N/A	5.50	3.30	2.25	2.00	1.85

I have enclosed the Dataquest Research Newsletter "OTP-One-Time Programmable EPROMs Promise to Impact MOS Read-Only-Memory Market," dated 18 October 1983, for a fuller discussion of this market.

cc: Mr. Dick Bratt/Spinnaker Software

Nielsen Dataquest

INQUIRY RESPONSE

DATE: 4/4/84

TO: Paul Bartlett/Mannesmann Tally

FROM: Mary Olsson/Dataquest

This information has been compiled in response to your inquiry of April 1984

Please file in Vol I, Sec.4 for future reference.

SUBJECT: Historical Data on 8088, 8-bit Microprocessor

Price Data

Table 1 shows estimated average selling prices of the 8-bit microprocessor from 1983 through 1988.

TABLE 1

8-BIT MICROPROCESSOR PRICE TRENDS
AVERAGE SELLING PRICES

1983	1984	1985	1986	1987	1988
3.25	3.00	2.75	2.50	2.35	2.20

The attached tables include historical 8-bit MPU market estimated from 1977 through 1982, and 1981 and 1982 quarter-to-quarter estimates of 8088 MPU shipments. I have also included the Third Quarter 1983 Microprocessor Shipments newsletter. An updated quarterly newsletter on microprocessor shipments will be published this month and forwarded to your office.

In general, the microprocessor book-to-bill ratio has been declining. The first and second quarter 1983 surge in demand for microprocessors, due to consumer market demands, is not expected to continue through 1984. No significant price increases are expected in 1984. Overall, 2Q84 prices have not changed over 1Q84. Lead times for 8-bit and 16-bit microprocessors are presently holding at 20 to 40 weeks.

Allocation Programs

Manufacturers are presently attempting to maintain stable lead times on S, LS, FAST, Microprocessor and Microcontroller products through allocation programs. The book-to-bill ratio is still high. Product availability is expected to improve during the third and fourth quarters of 1984. I have listed two companies that can be contacted as alternate sources for additional product requirements. These two

companies are strictly service companies. They offer computerized data exchange, listing excess inventory from OEMs. They require that companies using their service maintain a no-fee membership contract. Their fees are derived from sellers. They offer a 100% guarantee for all parts sold. The guarantee lasts for the life time of the part. All of the ICs are cross-referenced. Source 2, Inc., presently lists products from 1,200 companies. Source 2, Inc., is headquartered in Los Gatos, California, with nationwide offices in Boston and Dallas. Source 2, Inc., differs from a broker service in that it is a source of information only. Brokers usually buy products by lots and store the products in warehouses.

Source 2, Inc.
Los Gatos, California
(408) 727-2200
Joyce Wunderlich

Technical Information Services
Rochester, New York
(716) 594-1633
Ellen Haskin

Dataquest's Semiconductor Industry Update newsletter will be published in April 1984, and will be forwarded to your office.

:tg

cc: Marvin Crumb, President

Nielsen Dataquest

INQUIRY RESPONSE

DATE: 7-8-83

TO: Jim Lee/Hewlett-Packard

FROM: Stan Bruederle/SUIS

This information has been compiled in response to your inquiry of June 1983

Please file in Section 4 for future reference.

Subject: Semiconductor Capital Expenditures

Capital expenditures by U.S. merchant manufacturers for 1980, 1981, and 1982 were as follows:

	Expenditures($ millions)
1980	$1,356
1981	$1,339
1982	$1,180

We have also estimated expenditures by major manufacturer in millions of dollars.

	1980	1981	1982	1983 (projected)
AMD	46	64	65	90
AMI	13	17	27	28
Fairchild	83	140	156	131
Intel	156	157	138	150
Mostek	85	98	47	47
Motorola	177	175	175	190
National	116	105	82	80
Signetics	90	115	55	53
T.I.	270	120	130	147

:pg

4. Economic Factors

Many factors affect the economics of procurement. These factors include the impact of the overall economy, supply/demand relationships, the use of value analysis, the economics of multiple sourcing, the value of forward buying, and consideration of the relative sizes of semiconductor suppliers and users.

IMPACT OF THE ECONOMY

Overall economic conditions have a major impact on semiconductor procurement. Changing circumstances can cause major shifts in the supply/demand relationships, necessitating changes in procurement strategies. Recent trade press headlines illustrate the nature of the potential economic impact and the resulting problems:

- "Surge in LS Orders Drives Lead Times Out"
- "Vendor Visits Will Be a Top Priority in '82"
- "New Space Policy Directives Expected"
- " . . . . . Resigns"
- "Buyers Hedging on Long-Term 64K Pacts . . . . ."
- ". . . . . Company Agrees To Sell . . . . . Company"

Macroeconomic conditions represent one very important set of inputs to procurement persons involved in forecasting semiconductor needs. The analysis of trends and changes in trends is a fundamental part of the forecasting procedure. DATAQUEST has included the economic data in Appendix E as a part of the Semiconductor User Information Service, to assist semiconductor procurement teams in their forecasting activities.

SUPPLY/DEMAND RELATIONSHIPS

The supply/demand issue is important to anyone making procurement decisions. Purchasing decisions made in an "up" market where demand exceeds supply may be very different from those made in a "down" market when many suppliers have excess capacity. A "steady-state" market is a rare phenomenon in the semiconductor area, but such a market also has specific characteristics.

4. Economic Factors

Purchasing Semiconductors in an "Up" Market

Semiconductor procurement in a period of rising economic activity has the following characteristics:

- Lead times stretch quickly. The lead time on a product may go from two weeks ARO to 26 weeks ARO in less than one week.
- Prices firm, and some prices may increase as overtime is necessary to keep up with demand.
- Yields initially suffer, aggravating pricing and lead times. This is caused by addition of new and untrained personnel as capacity is expanded. A year or more may be required for yields to recover.
- New product introductions slip, as resources are reallocated to accommodate changes in demand.
- Some customers over-order, aggravating lead times.
- Distributor stocks turn over rapidly, and users experience spot shortages.
- The opportunities for human error multiply, causing spot quality problems such as shipment of wrong parts or wrong quantities.
- Pressure to renegotiate contracts may increase as suppliers and users strive to achieve their business objectives.

An "up" market condition may last for two years or more, and the user should plan according to the best forecasts possible. Accurate demand forecasting and lead-time forecasting are critical during periods of increasing economic activity.

Purchasing Semiconductors in a "Down" Market

Semiconductor procurement in a market experiencing recessionary or depressed conditions has the following characteristics:

- Lead times for many products drop to zero.
- Suppliers and distributors experience excess inventories.
- Prices may deteriorate rapidly on commodity products.
- Additional sources of many products appear.

4. Economic Factors

- State-of-the-art semiconductor products rapidly become commodities, especially in an extended recession.
- Semiconductor suppliers obsolete many of their unprofitable products.
- New product introductions proliferate.
- Yields on many volume products are optimized.
- The risk of business failure of a supplier or a distributor increases.
- Supplier-distributor relationships may change dramatically as franchise agreements gyrate.

In a "down" market, forecasting needs are reduced to the critical requirements of predicting lifetime usage of obsolete products, and to the early detection of reversals in economic conditions and trends. Semiconductor procurement management often seeks to optimize its contractual positions during the latter part of a "down" market interval. Such a practice should be followed with great caution if supplier loyalty is to be maintained when market conditions reverse to an upward trend.

Purchasing Semiconductors in a "Steady-State" Market

The following characteristics describe the conditions that prevail in a prolonged "steady-state" market for semiconductors:

- Lead times become more predictable and settle to 4-16 weeks for production-worthy products.
- Semiconductor yields are higher and more stable than in an "up" market.
- Experience and efficiencies of scale take effect, and price movement becomes more orderly and somewhat more predictable than in a changing market.
- New product introductions and production buildups are scheduled and timed more accurately.

Unfortunately for semiconductor users, the number of suppliers in competition for market share and the rapid pace of technological change prevent a steady-state market condition for more than a few months at a time. This is one reason it is very difficult to apply experience curve or learning curve theory to semiconductor pricing behavior.

4. Economic Factors

VALUE ANALYSIS

The application of value analysis techniques in semiconductor procurement is most effective when it is a cooperative effort involving participation by the marketing, engineering, manufacturing, incoming inspection, reliability, and other departments within the using company. When properly applied, value analysis results in overall lower costs, improvement in quality, enhanced maintainability, greater reliability, and increased chances of market penetration in the user's marketplace. These ends are not necessarily achieved by buying lower-cost semiconductors. Reallocation of resources throughout the user organization may dictate that higher prices be paid for semiconductors that have special characteristics in order to accomplish lower overall user costs. On the other hand, value analysis programs have also shown that some organizations may benefit from combining purchases across divisional lines. By doing so, many companies are able to achieve lower overall costs of doing business without sacrificing any of the end-product qualities.

Value analysis may be usefully applied in semiconductor situations such as:

- Relying upon a large number of suppliers
- Using broadline suppliers to supply one or a small number of the total semiconductor part types in use
- Making large annual dollar-volume purchases
- Purchasing large quantities
- Supporting complex hardware design consisting of many part types, which may benefit from higher levels of integration
- Using or not using third parties, including independent design, wafer fab, packaging, or test houses
- Using semiconductors that have been in production three or more years
- Working with a distributor or distributors
- Employing semiconductors having high reject rates or field failure rates
- Using proprietary or single-sourced semiconductors

4. Economic Factors

The major areas to be addressed by value analysis include:

- Technology
- Logistics
- Demand
- Capacity
- Cost
- Pricing
- Product considerations
- Macro-economic considerations
- Micro-economic considerations

There are three main steps in value analysis:

- Brainstorming
- Analysis
- Data reduction

An important preliminary step in a systematic approach to value analysis is developing a questionnaire. Table 4-1 is a check list intended to serve as a guide in designing a value analysis questionnaire.

The questionnaire can be used as the basis for the brainstorming or freethinking phase of the program.

The second phase involves in-depth analysis and data collection, at which time the ideas resulting from the freethinking phase are thoroughly investigated. Extensive supplier contact may be necessary during this second step. Dollar values are assigned to the various ideas and detailed data is collected to support the next step.

4. Economic Factors

Table 4-1

CHECKLIST FOR DESIGNING A VALUE ANALYSIS QUESTIONNAIRE

Value Analysis Questions

	Yes	No	Remarks
Is the feature provided by this part necessary?			
Is the part too complex?			
Will another part do the job better?			
Are the electrical specs too severe?			
Are the mechanical specs too severe?			
Can the specs be simplified?			
Is high-reliability required?			
Is this the right package?			
Is programmability required?			
Will a standard part suffice?			
Will a less expensive part work here?			
Are special tools required here?			
Are the tests too complex?			
Is special marking essential?			
Is special handling necessary?			
Does this part compromise safety?			
Does this part reduce maintainability?			
Is the lead time excessive?			
Does the cost of the part justify its benefits?			
Would you spend your money for this part?			
Is the ordering quantity correct?			
Is the best shipping method used?			
Can a distributor add value to the use of this part?			
Does the supplier have suggestions for improvements in this part?			

Source: DATAQUEST, Inc.
April 1982

4. Economic Factors

The third step of value analysis addresses data reduction and decision-making. As the data are reduced and decisions are made, the semiconductor user should stress the need for adequate solutions to problems, and avoid overkill. Adequate solutions usually minimize costs whereas excessive constraints may cause costs to rise again. The resulting output from the decision-making phase should be a written plan of execution that will lead to the desired results. It is important that management continuity be maintained throughout the program execution.

HOW MANY SOURCES?

The issue of multiple-sourcing should always be considered as a part of the supplier selection process. Within limits, increasing the number of potential sources of a product reduces the risks of acquiring sufficient quantities at the right times and at the right prices. Many government contracts require second-sourcing or multiple-sourcing as a necessary condition for using a semiconductor product in a system.

During the 1960s and early 1970s, it was often very difficult to establish multiple sources for semiconductor products because, relative to today, testing was less sophisticated and user specifications were often too stringent. As users gained experience and as products and the industry as a whole matured, many of these problems were resolved. At present, a popular product is almost always multiple-sourced within one to two years after introduction. It is not unusual for commodity products such as many TTL logic part types to have five or more sources of supply, each capable of supporting large-volume (100,000-piece) orders from 100 or more customers.

Problems can arise, however, when seeking multiple sourcing of new products or patented products. Because of the keen, frequently extreme competition in the semiconductor industry, it would be poor business practice for a supplier to aggressively encourage second-sourcing of a leadership product too early in its life cycle. Most leading suppliers prefer to engage with a "believable" second-source candidate that will not be a serious threat to the leader's position. The one major exception to this rule occurs when national or political interests are at stake.

Table 4-2 summarizes the approximate number of sources for a variety of semiconductors currently in production, and illustrates current trends in second-sourcing. MOS memories, which account for the highest dollar volumes per product type, tend to have the largest number of sources.

Table 4-2

EXAMPLES OF SEMICONDUCTOR MULTIPLE-SOURCING

Semiconductor Part Type	Estimated Number of Suppliers
64K D RAM	16
16K NMOS EPROM	15
8086 MICROPROCESSOR	8
68000 MICROPROCESSOR	7
4K TTL PROM	10
741 OP AMP	16

Source: DATAQUEST, Inc.
April 1982

Exceptions to the rule of requiring multiple sourcing of a semiconductor product or family may occur when:

- The need for secrecy outweighs the risk of program delay or failure
- A custom chip design is involved, with relatively high non-recurring costs
- The source is a distributor who will commit to a guaranteed inventory or who carries a multi-sourced line
- A one-time purchase is being made, with no future need to repurchase

FORWARD BUYING

Forward buying of semiconductors is essential to assure continuity of supply. This is especially true if the user's application is seasonal or otherwise experiences large swings in demand. For example, in certain consumer applications there is a heavy demand placed on semiconductor suppliers during the third calendar quarter of each year. The manufacturing pipeline for many semiconductor suppliers is on the order of from 12 to 16 weeks (from initial wafer start to tested devices ready for shipment). This means that the user must anticipate peak buying intervals and provide adequate lead time for supplier response.

4. Economic Factors

It is virtually impossible for any narrow-based (limited product line) semiconductor supplier practicing a full employment policy to respond to major seasonal changes in demand and remain profitable. This is especially true in a rapidly rising economic situation, when semiconductor capital equipment lead times can exceed 52 weeks. Forward buying, therefore, is critical where narrow-based semiconductor suppliers are utilized.

While forward buying of semiconductors may increase the apparent cost of doing business, the cost of not practicing the technique may be much greater. The biggest risk in the short-range buying approach is the possibility of semiconductor stock outages and the resulting production line downtime at the user's plant or plants. Such shutdowns cause severe long-term losses in terms of market share and customer goodwill. Short-term losses include increased need for overtime and increased labor disruptions resulting from production line imbalances.

Factors to be considered in establishing a forward buying program include inventory holding costs, the potential risks of technological change (product revisions) and obsolescence (discontinued products), supply/demand changes, and changes in prices. Any of these factors will affect the lead-time aspect of forward buying. The practice of forward buying also may result in increased research costs, increased planning costs, and increased overhead cost of managing the forward buying activity. Relatively speaking, these increased costs are almost always outweighed by the potential savings from forward buying and by avoiding the losses resulting from failing to practice forward buying. When international considerations are involved, forward buying properly applied reduces the associated risk of doing business.

RELATIVE SIZES OF SEMICONDUCTOR SUPPLIERS/USERS

The relative sizes of semiconductor users and suppliers affect the procurement function in several possible ways. One example of this is the present trend toward installation of data terminals at the facilities of large semiconductor users ($500 thousand or more annual consumption) by some semiconductor distributors. Procurement strategies should take into account the relative economic power of the user and supplier and how they relate in rising, steady-state, and declining market conditions.

For purposes of the following discussion, a large supplier is defined as having semiconductor sales of at least $100 million per year, and a large user is defined as one buying semiconductors at a rate of at least $5 million per year, or approximately 5 percent of a large supplier's output. To a degree, in the semiconductor industry as in other industries, "money talks," and economic power considerations play a large role in business strategies. The following possibilities should be considered before establishing or revising purchasing strategies.

4. Economic Factors

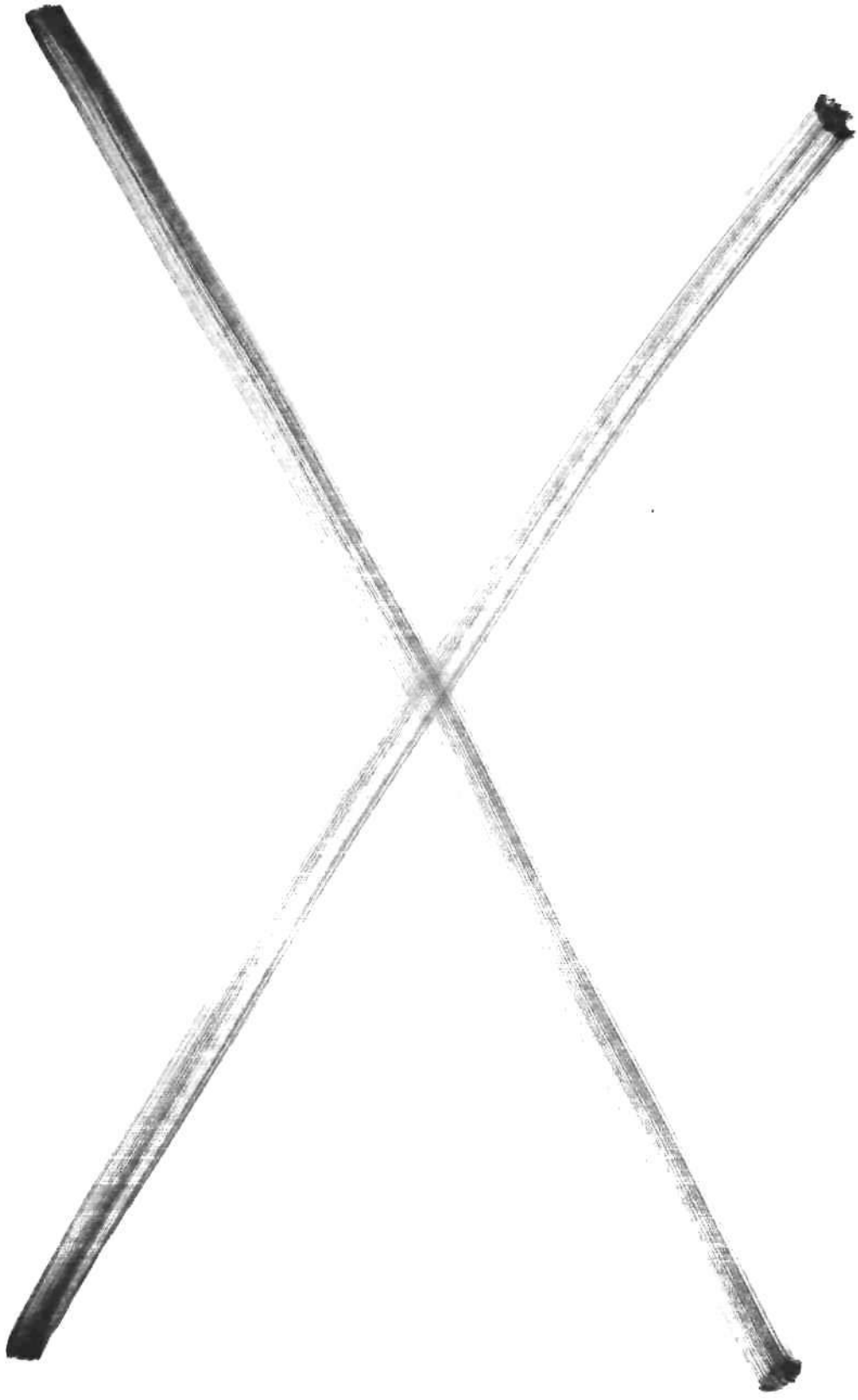
Large Supplier, Small User

In a declining market, the small user may get increasing attention from all suppliers, including large suppliers. The attention increases as the market remains soft. As the market turns upward and some products go on allocation, the small user may be impacted more than large users unless the small user's growth rate is sufficient to show the large supplier a need for long-term support. The small user should select suppliers with the long-term view in mind, and should be careful to align with those suppliers who 1) will provide continuing support in all market conditions, and 2) will not be a future strong competitor in the user's market. The small user should carefully consider the role of distribution in helping to avoid these pitfalls.

Small Supplier, Large User

In a declining market, the large user can create havoc for the small supplier if procurement is not carefully managed. Since the large user represents more than 5 percent (sometimes as much as 30 percent) of the small suppliers' business, major changes in delivery schedules and severe price pressure may cause the small supplier to become unprofitable, or to make major changes in business strategies in an effort to remain profitable. Procurement plays a vital role in helping the user company avoid involvement in such situations.

In a rising or steady-state market, the small semiconductor supplier may not keep pace with the large user's growth rate and changes in demand. If this occurs in a rising market, the user may be forced to seek additional sources at a time when they are least likely to be found. To summarize, procurement should choose suppliers only after considering the long-term prospects as well as the short-term demand.



5. Technology Tradeoffs

As semiconductor technology becomes more sophisticated and devices become more complex, the user is often offered several solutions to the same technical problem. Inevitably there are tradeoffs to be made between the various alternatives. One device may offer a more cost-effective implementation, while another offers lower power dissipation or higher speed. This section discusses some current tradeoffs to be made when choosing a semiconductor for a particular application.

CUSTOM VS. SEMICUSTOM VS. STANDARD

As semiconductor technology progresses, the user has more alternatives from which to choose a cost-effective approach to hardware implementation. During the early 1960s, very few standard MSI/LSI functions existed, and all high-density ICs were custom designed to meet a single customer's needs. During the early 1970s standard LSI functions came into widespread use, and a growing number of supplier companies concentrated on increasing the availability and number of types of standard products. More recently, semicustom devices have evolved and provided a compromise solution to the standard versus custom problem. Semicustom ICs combine the benefits of standard devices with those of custom devices. The relative advantages and disadvantages of the three approaches are given in Table 5-1. In Table 5-1, standard circuits include user-programmable PROMs, EPROMs, EEPROMs, PLAs, and FPLAs. Semicustom circuits include mask-programmable ROMs and gate arrays.

CMOS VS. BIPOLAR

The technology of complementary MOS (CMOS) integrated circuits advanced rapidly in the late 1970s and early 1980s. Some of the former advantages of bipolar circuits are now available in CMOS form, including:

- Gate speeds of less than 3 nanoseconds
- Standard SSI/MSI logic families
- High-density LSI memories
- TTL-compatible interface levels
- Fuse-link PROMs
- Military temperature range (-55 to +125°C) operation

5. Technology Tradeoffs

Table 5-1

HARDWARE IMPLEMENTATION ALTERNATIVES
ADVANTAGES AND DISADVANTAGES

Standard Product	Semicustom Product	Custom Product
Usually multiple-sourced	Frequently multiple-sourced	Frequently single-sourced
No design time	Short design time	Longest design time
No design cost	Low design cost	High design cost
Least design security	Some design security	Greatest design security
Least package flexibility	Better package flexibility	Most package flexibility
Highest overall cost/used function in high volume	Medium overall cost/used function in high volume	Lowest overall cost/used function in high volume
Distributor supported	Not presently distributor supported	Not distributor supported
Lowest risk	Medium risk	Highest risk

Source: DATAQUEST, Inc.
April 1982

5. Technology Tradeoffs

In addition, the following standard, multisourced NMOS functions are also available in CMOS form:

- 16K RAMs
- 16K and 64K UV-erasable PROMs (EPROMs)
- 8-bit and 16-bit microprocessors
- High-density (1.5K to 6K) gate arrays

It is now possible to build all-CMOS systems using the available peripherals, telecom circuits, interface circuits, and other CMOS ICs. All-CMOS systems offer the end customer greatly reduced power consumption, enhanced portability, and potentially greater reliability than is presently available in NMOS technology. DATAQUEST expects a rapid growth in CMOS applications because of these advances in IC technology. Semiconductor users should be prepared to take advantage of the benefits offered by CMOS devices in order to remain competitive in their end markets.

CHOOSING A MICROPROCESSOR

There are many technical considerations to be addressed by the user before selecting a microprocessor for a particular application. This section addresses the major issues.

Microprocessor architecture has progressed from the 4-bit structures produced in 1972 to the 16-bit families produced in 1982. The 16-bit microprocessor families (Intel 8086, Motorola 68000, National 16000, Texas Instruments (TI) 9900, and Zilog Z8000) offer powerful, system-oriented architectures and processing capabilities that rival the performance of many minicomputers and some mainframe computers. Table 5-2 shows the basic features of these microprocessors.

The following tradeoff factors are important in choosing a microprocessor:

- Computational capability, which is a function of clock speed and micro-instruction set, and which must meet the minimum requirements of the application
- Memory address capability, which ranges to 16 Mbytes for some 16-bit architectures
- Manufacturing process, which may be CMOS, NMOS, or bipolar, and which has a direct bearing on speed, power, and cost

5. Technology Tradeoffs

Table 5-2

BASIC FEATURES OF 16-BIT MICROPROCESSORS

Features	Intel 8086	Motorola 68000	National 16000	TI 9900	Zilog Z8000
Max. Memory Address	1Mb	16Mb	16Mb	16Mb	8Mb
Address Method	Segment	Linear	Linear	Mapper	Segment
Clock Speeds	5 mHz 8 mHz 10 mHz	4 mHz 6 mHz 8 mHz 10 mHz 12.5 mHz	10 mHz	3 mHz	4 mHz 6 mHz 10 mHz
MOS Process	HMOS	HMOS	XMOS	NMOS	NMOS
Internal Data Path	16-bit	16-bit	32-bit	16-bit	16-bit
External Data Bus					
Multiplexed	MPX		MPX		MPX
Nonmultiplexed		NMPX		NMPX	
Registers					
General Purpose	4(16-bit)	15(32-bit)	8(32-bit)	None	15(16-bit)
Dedicated	8(16-bit)	2(32-bit)	5(32-bit)	4(16-bit)	3(16-bit)
Pin-Count/Pkg.	40	64	48	64	40/48
Number of Second Sources	8	7	3	2	4

Source: DATAQUEST, Inc.
April 1982

5. Technology Tradeoffs

- Package size/pin count, which is dictated by chip architecture and system form factor
- Interface requirements, which includes type of external data bus and other system constraints
- Peripheral support requirements, which includes the need for external signal processing, dynamic memory refreshing, telecommunications interface, and others
- Future architecture compatibility, which allows the user to upgrade the end system without requiring that software be rewritten
- Environmental factors, which includes operating temperature range, system reliability requirements, and others

The technical risks involved in microprocessor selection are much greater than those involved in choosing the system memory approach. As a means of reducing this risk, some users perform benchmark tests on hardware prototypes to compare the performances of two or more microprocessors before making a final choice. Benchmark testing is most appropriate when it simulates the range of actual applications of the final hardware.

The technical risks inherent in the software aspects of microprocessor selection are far more important than the hardware considerations. The user should be aware that the software investment may exceed the hardware investment by a factor of ten or more, and this investment is wasted if future generations of microprocessors are not compatible with the existing software. DATAQUEST suggests that the user resolve the software issues prior to hardware prototyping and benchmark testing.

NON-VOLATILE MEMORY

Semiconductor technology has produced a variety of non-volatile memory during the last ten years. At present, the user can choose from bipolar, MOS, and bubble (garnet substrate) technologies, and from a wide range of programming methods including masking during manufacture, fuse links, UV-erasable buried layers, and read-write RAMs (battery backup). Densities vary from one kilobit to one megabit per chip, and speeds range to 20 MHz (50 nanosecond cycle times). Table 5-3 summarizes the non-volatile IC memory technologies available in 1982.

5. Technology Tradeoffs

Table 5-3

NON-VOLATILE IC MEMORY CHARACTERISTICS

Type	IC Density	Power (mW) Active/Standby	Cycle Time (ns)	Comments
Masked ROM	128K	385/0	400	Factory programmed
NMOS EPROM	64K	550/0	200	UV-erasable
CMOS EPROM	64K	110/0	200	UV-erasable
Bipolar PROM	64K	960/0	50	Fuse link
EEPROM	16K	600/0	250	
Bubble Memory	1Mb	5,000*/0	500	Not random access
NMOS RAM/Battery	16K	450/150	70	Short battery life
CMOS RAM/Battery	16K	200/0.1	200	
NV RAM	1K	300/0	300	

*Includes control circuit power

Source: DATAQUEST, Inc.
April 1982

5. Technology Tradeoffs

EPROMs VS. MASKED ROMs

The semiconductor user may purchase quantities of EPROMs, masked ROMs, or both. There are technical reasons and economic reasons for choosing either approach, or a combination of the two.

Technical Considerations

A masked ROM is programmed at the time of manufacture by using a customized mask representing the desired bit pattern. There is a setup cost incurred by the manufacturer for this operation. It is not possible to change the contents of the masked ROM after it is shipped. The ROM storage element has an extremely long-lasting data retention characteristic, which is measured in thousands of years under normal operating conditions. In contrast, an EPROM has a data retention characteristic estimated at from 10 to 100 years under similar conditions, but it may be reprogrammed by the user as often as desired. If memory permanence is more important than economics or reprogrammability, the masked ROM is the obvious choice. If, however, reprogrammability is required, the EPROM would be the better choice.

Economic Considerations

If a 10-year data retention characteristic is acceptable to the user, an economic decision must be made. EPROMs are more complex than ROMs, and the manufacturing cost for large volumes of EPROMs is greater than that for ROMs of the same bit density. However, lead times for masked ROMs are usually longer than EPROM lead times. Semiconductor distributors are generally not equipped to process ROM orders. The desired program must be communicated to the manufacturer, and later verified. Any errors in programs involve manufacturing replacement parts. Suppliers usually require a volume commitment of 1,000, and preferably more, parts per mask, and the user must pay for the cost of all of the parts produced because they are custom parts. These factors have contributed to a recent upsurge in the popularity of EPROMs. The resulting higher volume of EPROMs manufactured has driven costs down and allowed prices to decline such that the price differential between EPROMs and ROMs at low volumes (1,000 to 2,000 pieces) is almost non-existent. DATAQUEST expects this trend to continue.

DYNAMIC RAMs VS. STATIC RAMs

Semiconductor memory has progressed from small-scale integrated (SSI) flip-flops through shift registers to large scale integrated (LSI) read/write random access memories (RAMs). The user now has a choice of IC RAMs ranging up to 256K bits in complexity and to less than ten millicents per bit component cost. There are technical as well as economic decisions involved in choosing the best approach to RAM hardware implementation.

5. Technology Tradeoffs

Assuming the user does not need bipolar speed or CMOS low power, lower hardware cost is possible with NMOS dynamic or static RAMs. However, technological considerations may override cost.

Dynamic RAMs must be refreshed; that is, the dynamic RAM storage cell (a capacitor accessed by a transistor switch) must have its charge restored to a minimum level at frequent intervals. Worst-case specifications for today's dynamic RAMs dictate a maximum refresh interval of four milliseconds. If the user's hardware design and operating requirements cannot tolerate the interruptions needed for refreshing, then the only other choice is the use of static RAMs. If refresh can be tolerated, equipment complexity and cost must then be considered. Static RAMs are a factor of four lower density than are dynamic RAMs, at a given level of technology. The user must compare the total complexity and cost of the alternative designs, including the complexity and cost of refresh circuitry, in order to choose the optimum solution. Single-chip automatic refresh circuits reduce the memory size at which dynamic RAM becomes cost-effective.

GaAs VS. SILICON SEMICONDUCTORS

Gallium arsenide (GaAs) technology has been in use since the implementation of GaAs lasers by General Electric and IBM in 1962 (parallel efforts), and light emitting diodes by Bell Labs in 1964. There are three overriding considerations when comparing GaAs and silicon integrated circuits at the present time:

- GaAs wafer fabrication is approximately 50 times as costly as silicon.
- GaAs circuit operation is much higher speed than that of silicon.
- Achievable silicon circuit complexity is 100 to 500 times that of GaAs circuitry.

The above factors drive the user to continue to rely on silicon wherever possible, and to use GaAs technology only when performance is clearly the overriding factor. Currently, GaAs IC technology is being applied in high-performance military hardware, instrumentation, and optoelectronics. GaAs is being studied by a large number of suppliers and systems houses as a means of implementing future generations of high-speed computers. DATAQUEST expects product announcements of high-performance GaAs ICs during 1982/1983, and a continuing trend toward the use of GaAs ICs for high-speed signal processing applications.

The current suppliers of GaAs semiconductors are identified in Volume II of this service.

5. Technology Tradeoffs

IC PACKAGE TRADEOFFS

The integrated circuit user has a wide range of package types available for system implementation. At present, this variety includes plastic and ceramic dual in-line packages, chip carriers, flat packs, and hybrid (multi-chip) packages. Each of these forms has special characteristics suitable to specific needs.

The package tradeoff algorithm for many applications is complex and should be designed to account for all of the following factors:

- System form factor
- Cost
- System density
- Thermal characteristics
- Hermeticity
- Other environmental characteristics
- Availability
- Multiple sourcing
- Expected lifetime of system

In new system designs, the system form factor may already be established. For example, conformity with existing system designs may be a requirement. If so, this may severely limit the packaging alternatives for the new system.

The effect of IC package cost on the total system cost is dependent upon the IC cost percentage of the total system. In some data processing applications, ICs may account for as much as 17 percent of the total system cost. In this case, a 12 percent savings in IC cost would reduce the total system cost by two percent.

System density constraints may necessitate higher IC package costs. This is the usual case for hybrid, flatpack, and chip carrier packaging. Of these, the hybrid approach offers the highest density, but it may dictate very high costs of multiple sourcing.

Environmental factors such as heat transfer, hermeticity, vibration, and shock vary widely by application. Temperatures may range from air-conditioned environments (25°C) to automotive and military operating environments of -55°C to +125°C and storage environments of -70°C to +150°C. Humidity conditions may consist of extended exposure to a salt spray atmosphere or to relative humidity of 95 percent at elevated temperature. The package selection should include consideration of environmental factors to avoid reliability problems in the field.

5. Technology Tradeoffs

Product availability and the availability of multiple sources are sometimes functions of the required packaging. For example, some IC suppliers may introduce a product in only one type of package, and may not offer all possible packaging forms for a particular product. This has occurred in certain microprocessor and memory products in the past. Such situations are driven by economics; some IC suppliers may be interested in increasing package variety in a soft market to stimulate sales, and in decreasing package/chip combinations in a rising market to improve efficiency and reduce costs. This situation causes fluctuations in device/package multiple sourcing. Hybrid packages may be particularly vulnerable to this type of problem, making multiple-sourcing costs of hybrid packages prohibitive for some IC users.

The user should be aware of the significance of total industry volume for the various package types. Plastic dual in-line packaging (DIP) accounts for as much as 80 percent of units shipped for many commodity ICs such as TTL, SSI, and MSI devices. It is possible for a large IC supplier to produce more than one million plastic DIPs per normal production day. Such a supplier may have very little interest in making DIP package changes to accommodate the needs of one customer, because of the economics involved.

Table 5-4 summarizes the package tradeoff factors encountered by most IC users. This matrix may be useful in arriving at hardware packaging decisions. DATAQUEST suggests that the user quantify the entries in the tradeoff matrix and add weighting factors to each of the parameters, based on the user's system constraints and the required IC product functions.

5. Technology Tradeoffs

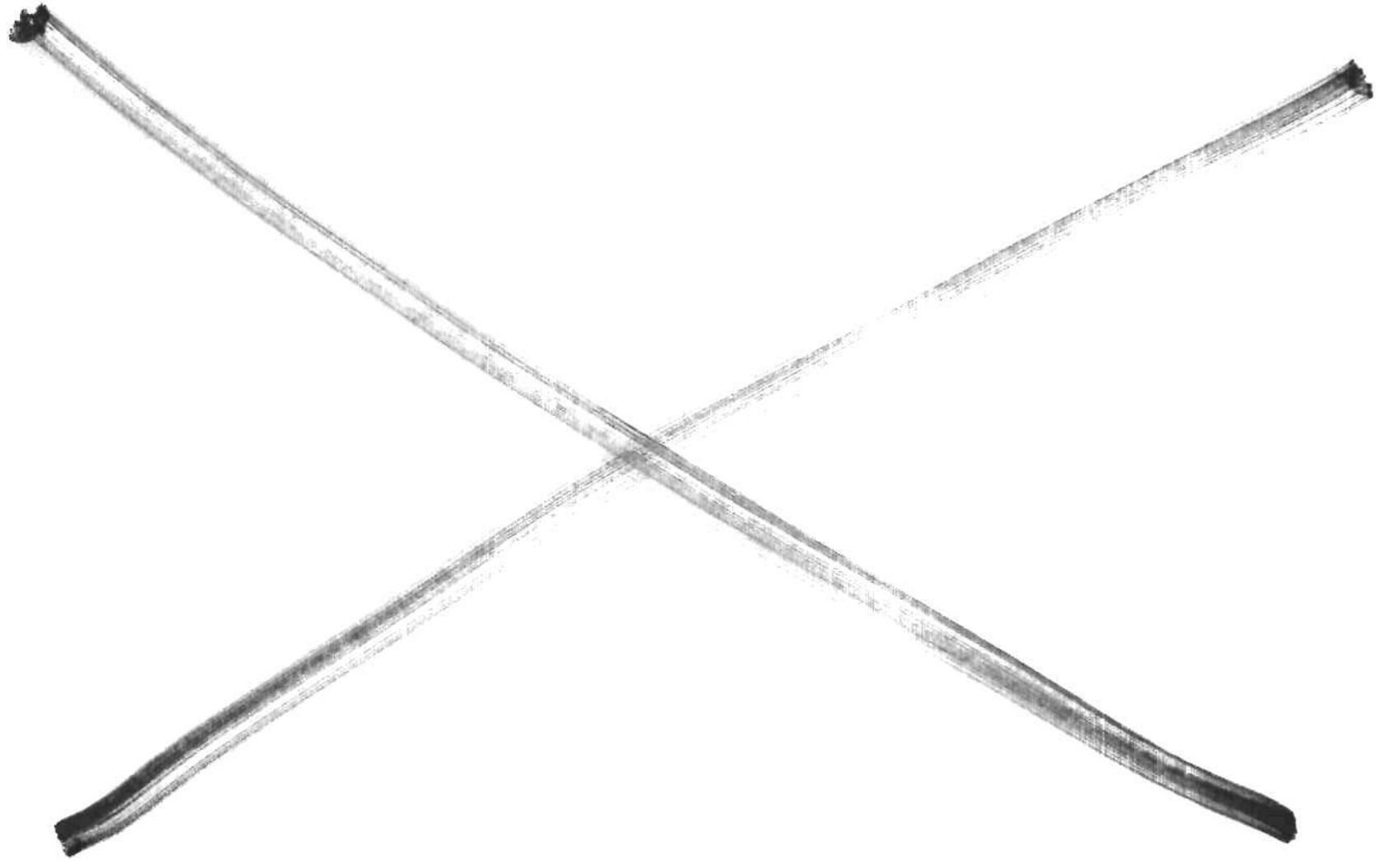
Table 5-4

IC PACKAGE TRADEOFFS

Factor	Plastic DIP	Cerdip	Ceramic Chip Carrier	Metal Lid Flatpack	Multi-Chip Hybrid
Cost	low	low	medium	medium	high
Package Density	low	low	medium	medium	high
Thermal Coefficient	high*	medium	medium	low	low
Hermeticity	low	medium	medium	high	high
Socket Cost (if used)	medium	medium	-	-	high
Number of Suppliers	large	large	medium	medium	medium
Multiple Sourcing	yes	yes	yes	yes	no**

*May be reduced to approach cerdip through use of metal slug, which increases cost
**Except for certain multi-chip memory devices

Source: DATAQUEST, Inc.
April 1982



Nielsen Dataquest

INQUIRY RESPONSE

DATE: 12/5/83

TO: Paul Bartlett/ Mannesmann Tally

FROM: Mary Olsson/SUIS

This information has been compiled in response to your inquiry of Nov. 1983

Please file in Vol.I, Sec. 6 for future reference.

Subject: International Procurement

1) Volume I, Section 6, pg 6-6 to 6-9. provides you with references to international procurement.

The following is an additional list of sources to assist you in international procurement decisions.

- Price Waterhouse Information Guides for Doing Business Abroad
  1251 Ave. of the Americas
  New York, NY 10020
  (212) 489-8900

Individual guides for each country.

- International Group of the National Association of Purchasing Management
  496 Kinderkamack Road
  P.O. Box 418
  Oradell, NJ 07649
  (201) 967-8585

- Superintendent of Documents
  U.S. Government Printing Office
  Washington, D.C. 20402
  (202) 275-2051

Articles: "U.S. Trade Classification"
"U.S. Foreign Trade Imports"

Government publications on which commodities are being imported from particular regions.

- U.S. Bureau of Census

Reports: FT135 "U.S. General Imports, Schedule A: Commodity by Country"
FT410 "U.S. Exports, Schedule E: Commodity by Country"
FT990 "Highlights of U.S. Export and Import Trade"

- Consular offices of foreign countries in the U.S.

Great Britain Chancellery Washington, D.C. (202) 462-1540	Japanese Consulate Office San Francisco, CA (415) 921-8000

- U.S. Embassies located in foreign countries

U.S. Embassy Great Britain and Ireland London, England	U.S. Embassy Japan Tokyo, Japan

- Brokers, importers and sales offices in the U.S. (see attachment).

- Other buyers or companies purchasing offshore that would provide you with experiences and sources.

2) The following is a list of factors involved in worldwide purchasing that a user should be aware of before making international purchasing decisions.

- Prices and Profits: The best price for material goods and services will provide greater profit margins, more competitive pricing and offset other costs.

- Cost considerations
  Transportation costs
  Additional inventory costs
  Import taxes
  Container/packaging costs
  Insurance
  Duties
  Brokerage fees
  Breakage and damage
  Currency fluctuations (see attached)

- Verification of supplier quality through:
  Facility visitation
  Sample shipments
  References from other companies
  Product availability and delivery times
  Financial stability of the company

cc: Marvin Crumb/Mannesmann Tally

:tg

JAPANESE SEMICONDUCTOR SALES AND LIAISON OFFICES IN THE UNITED STATES

Parent Company	U.S. Company	Location
Fujitsu Limited	Fujitsu Microelectronics, Inc.	Headquarters: Santa Clara, CA
Hitachi, Ltd.	Hitachi America, Ltd.	Headquarters: New York, NY Sales Offices: Los Angeles, San Francisco, San Jose, CA; Atlanta, GA; Chicago, IL; Detroit, MI; Houston, TX
Matsushita Electric	Matsushita Electric Corporation of America (Matsushita Electronic Components Company)	Secaucus, NJ
	Microelectronic Technology Corporation	Santa Clara, CA
Mitsubishi Electric Corporation	Mitsubishi Electronics America, Inc.	Headquarters: Rancho Dominguez, CA Sales Offices: Sunnyvale, Torrance, CA; Boca Raton, FL; Mt. Prospect, IL; Bloomington, IN; Woburn, MA; West Piscataway, NJ; Irving, TX
NEC Corporation	NEC Electronics U.S.A. Inc.	Headquarters: Mountain View and San Mateo, CA Sales Offices: Cupertino, Los Angeles, Santa Clara, Sunnyvale, CA; Pompano Beach, FL; Chicago, IL; Natick, Woburn, MA; Columbia, MD; Detroit, MI; Edina, MN; Melville, NY; Dallas, TX
Oki Electric Industry Company, Limited	Oki Semiconductor, Inc.	Headquarters: Santa Clara, CA Liaison Office: Hackensack, NJ
Sharp Corporation	Sharp Electronics Corporation	Headquarters: Paramus, NJ Sales Offices: Carson, CA; Norcross, GA; LaGrange, IL; Boston, MA; New York, NY; Arlington, VA; Richardson, TX
Tokyo Sanyo	Sanyo Semiconductor Corporation	Headquarters: Allendale, NJ Office: Santa Clara, CA
Toshiba Corporation	Toshiba America, Inc.	Headquarters: Tustin, CA Regional Offices: Newport Beach, CA; Boston, MA; Southfield, MI; Edina, MN

Source: DATAQUEST

No. 1550. Foreign Exchange Rates: 1965 to 1982

(In U.S. cents per unit of foreign currency)

COUNTRY	Currency unit	1965	1970	1975	1977	1978	1979	1980	1981	1982, Aug.
Australia	Dollar	222.78	111.36	130.77	110.82	114.82	111.77	114.00	114.95	97.83
Austria	Schilling	3.87	3.87	5.75	6.05	6.90	7.46	7.73	6.29	5.74
Belgium	Franc	2.01	2.01	2.73	2.79	3.18	3.41	3.42	2.70	2.11
Canada	Dollar	92.74	95.80	98.30	94.11	87.73	85.39	85.53	83.41	80.30
Denmark	Krone	14.46	13.33	17.44	16.66	16.16	19.01	17.77	14.08	11.56
France	Franc	20.40	18.09	23.35	20.34	22.22	23.50	23.69	18.49	14.43
Germany, Fed. Rep	Deutsche mark	25.04	27.42	40.73	43.09	49.87	54.56	55.09	44.36	40.30
India	Rupee	20.94	13.23	11.93	11.41	12.21	12.27	12.69	11.55	10.44
Ireland	Pound	279.59	239.59	222.16	174.49	191.84	204.65	205.77	161.32	138.54
Italy	Lira	.16	.16	.15	.11	.12	.12	.12	.09	.07
Japan	Yen	.28	.28	.34	.37	.48	.46	.44	.45	.39
Mexico	Peso	8.01	8.01	8.00	4.42	4.39	4.38	4.35	4.08	1.11
Netherlands	Guilder	27.77	27.65	39.63	40.75	46.28	49.84	50.37	40.19	36.64
Norway	Krone	13.98	13.99	19.18	18.79	19.08	19.75	20.26	17.46	14.97
Portugal	Escudo	3.48	3.50	3.93	2.62	2.28	2.04	2.00	1.63	1.16
South Africa	Rand	139.27	139.24	136.47	114.99	115.01	118.72	128.54	114.77	86.77
Spain	Peseta	1.67	1.43	1.74	1.33	1.31	1.49	1.40	1.09	.89
Sweden	Krona	19.39	19.26	24.14	22.38	22.14	23.32	23.65	19.86	16.28
Switzerland	Franc	23.11	23.20	38.74	41.71	56.26	60.12	59.70	51.03	47.35
United Kingdom	Pound	279.59	239.59	222.16	174.49	191.84	212.24	232.56	202.43	172.50

Source: Board of Governors of the Federal Reserve System, *Federal Reserve Bulletin*, monthly.

No. 1551. Foreign Exchange Rates, by Country: 1979 to 1981

[National currency units per U.S. dollar. As of December 31. Represents mid-point market quotations to extent available. For countries with fixed relationships to a third currency, represents exchange rates of the third currency, times the fixed relationships. For currencies not quoted in exchange markets, represents official rates. For countries with multiple exchange rate systems, represents rate applicable to principal trade transactions]

COUNTRY	Currency unit	EXCHANGE RATE			COUNTRY	Currency unit	EXCHANGE RATE		
		1979	1980	1981			1979	1980	1981
Algeria	Dinar	3.76	3.97	4.38	Kenya	Shilling	7.33	7.57	10.29
Argentina	Peso	1,619	1,993	7,248	Korea, Rep. of	Won	484	660	701
Australia	Dollar	.905	.847	.887	Kuwait	Dinar	.273	.271	.281
Austria	Schilling	12.4	13.8	15.9	Liberia	Dollar	1.00	1.00	1.00
Belgium	Franc	28.0	31.5	38.5	Libya	Dinar	.296	.296	.296
Bolivia	Peso	24.5	24.5	24.5	Malaysia	Ringgit	2.19	2.22	2.24
Brazil [2]	Cruzeiro	42.5	65.5	127.8	Mexico	Peso	22.8	23.3	26.2
Canada	Dollar	1.17	1.19	1.19	Netherlands	Guilder	1.91	2.13	2.47
Chile	Peso	39.0	39.0	39.0	New Zealand	NZ Dollar	1.01	1.04	1.21
Colombia [1]	Peso	44.0	50.9	59.1	Nicaragua	Cordoba	10.05	10.05	10.05
					Nigeria	Naira	.561	.544	.637
Costa Rica	Colon	8.57	8.57	36.1	Norway	Krone	4.93	5.18	5.81
Denmark	Krone	5.37	6.02	7.33	Pakistan	Rupee	9.90	9.90	9.90
Egypt [3]	Pound	.700	.700	.700	Peru	Sol	250.1	341.2	505.2
Finland	Markka	3.71	3.84	4.36	Philippines	Peso	7.42	7.60	8.20
France	Franc	4.02	4.52	5.75	Portugal	Escudo	49.8	53.0	65.2
Germany, Fed. Rep. of	D. Mark	1.73	1.96	2.25	Saudi Arabia	Riyal	3.37	3.33	3.42
Ghana	New Cedi	2.75	2.75	2.75	Singapore	Dollar	2.16	2.09	2.05
Greece	Drachma	38.3	46.5	57.6	South Africa	Rand	.827	.746	.957
Honduras	Lempira	2.00	2.00	2.00	Spain	Peseta	66.1	79.3	97.5
					Sri Lanka	Rupee	15.45	18.00	20.55
India	Rupee	7.91	7.93	9.10	Sweden	Krona	4.15	4.37	5.57
Indonesia	Rupiah	627	627	644	Switzerland [3]	Franc	1.58	1.76	1.80
Iran	Rial	70.5	72.3	79.5	Tanzania	Shilling	8.22	8.18	8.32
Iraq	Dinar	.295	.295	.295	Thailand	Baht	20.4	20.6	23.0
Ireland	Pound	.466	.527	.632	Turkey	Lira	35.4	90.1	133.6
Israel	Shekel	3.535	7.548	15.604	United Kingdom	Pound	.450	.419	.524
Italy	Lira	804	931	1,200	Uruguay [1]	New Peso	8.46	10.03	11.59
Ivory Coast	CFA Franc	201	226	287	Venezuela [1]	Bolivar	4.29	4.29	4.29
Jamaica	Dollar	1.781	1.781	1.781	Yugoslavia	Dinar	19.2	29.3	41.8
Japan	Yen	240	203	220	Zaire	Zaire	2.025	2.985	5.465
Jordan	Dinar	.295	.308	.339	Zambia	Kwacha	.779	.803	.883

[1] Selling rates: The rates at which monetary authorities (or commercial banks) sell foreign exchange for national currency to those making payments abroad. [2] Represents official rate. [3] Buying rates: The rates at which the monetary authorities (or the commercial banks) buy foreign exchange for national currency from recipients of foreign exchange.

Source: International Monetary Fund, Washington, D.C., *International Financial Statistics*, monthly.

6. Sources and Logistics

As the semiconductor industry has grown, the sources of supply have multiplied and the logistics of procurement have become more complex. Today the procurement of semiconductors often involves global considerations, including multinational transactions and multiple currencies. This section addresses semiconductor sources and logistics as an aid to procurement planning. The user should refer to Volume II of this service for detailed information on specific suppliers and distributors.

SEMICONDUCTOR SUPPLIER MARKETING CHANNELS

There are numerous legal and economic factors to be considered by users and suppliers in the worldwide semiconductor marketplace. The product distribution channels must be selected to minimize their adverse impact on efficiency and profitability. As the industry has developed, each supplier has chosen the marketing channels best suited to its overall strategy. Most suppliers use one or a combination of the following approaches:

- Direct sales offices
- Direct sales via corporate headquarters
- Authorized factory representatives
- Franchised distributors
- Local agents (importers)
- Retail outlets
- Telephone/mail order outlets

Each approach is usually supported by some level of technical assistance. Such support may range from the provision of design or product engineering assistance by smaller firms, to the building and staffing of local design centers by the larger corporations.

The method of marketing used by a particular supplier depends on the level of business of the supplier, the complexity of support and service requirements, and the legal aspects of the supplier-customer relationship. For example, a standard product family may be well documented and its applications easily understood by the technical community. In this case, a sale can be made and follow-up accomplished as a straightforward distributor transaction with very little or no factory management involvement. On the other hand, a user may require a custom, special-purpose controller, and need design confidentiality. This would require an in-depth technical interface as well as special security provisions throughout production life, necessitating assignment of design engineering support, program management, and other resources.

6. Sources and Logistics

For shipments crossing national boundaries, legal considerations become more complex. The question of ownership becomes more important, since customs duties may be involved. The need to return products across national boundaries for reprocessing or replacement may create both legal and economic problems that would not occur when dealing with a domestic source. Thus it is important for the user to understand the supplier's channels of distribution when selecting the supplier base, as a means of preventing trouble later.

U.S. MARKETING CHANNELS

The United States is the largest geographic market in the world for semiconductors. All of the market channels identified in this section are used in the U.S. marketplace. The large international distributors such as Hamilton-Avnet originated in the United States, and today more than 150 U.S. distributor firms sell semiconductors.

There are approximately 2,500 firms representing electronics suppliers in the United States, and many of them represent semiconductor suppliers. Some semiconductor suppliers, such as National Semiconductor Corporation, sell exclusively through representatives (reps) rather than direct salespeople, while others, such as TRW Incorporated, use a combination of direct sales and representatives. Two primary reasons for using reps are: they are considered "territory geniuses" with a good understanding of their clients' needs; and economic (cash flow and cost) factors often favor the use of reps. In the United States the rep usually does not assume ownership of the semiconductor products, or title to the products. In fact the representative usually carries only a kit of samples, and all deliveries are made by direct shipment from the supplier to the customer.

WEST EUROPEAN MARKETING CHANNELS

Sales of semiconductors in Western Europe are made in a number of ways, but can be divided into two main categories, direct sales by the manufacturers and sales through distribution. The majority of semiconductor devices in Europe are sold directly; we estimate direct sales at 85 percent of total West European consumption.

The pattern of distribution versus direct sales is not consistent throughout Europe. The distribution sector is probably most highly developed in the United Kingdom, with about 25 percent of semiconductor sales occurring through distribution. The French market also has a relatively high proportion of sales through distribution, but the West German distribution sector is far less developed. The European distribution sector is growing as a proportion of total semiconductor sales, however, and the West German distribution sector is currently one of the fastest growing in Europe.

6. Sources and Logistics

In Europe the relationship between distributor and semiconductor manufacturer differs somewhat from that in the United States. U.S. distributors take products on a consignment basis, which means that the manufacturer still owns them. This arrangement makes return of the products comparatively easy. However, European distributors typically take title to the products when they take delivery, meaning that the manufacturer views the distributor in the same light as a direct purchaser and that returns are more difficult. To a large extent, this situation occurred because the majority of the semiconductors consumed in Europe were (and still are) imported. This makes the consignment system very difficult to operate because of customs problems.

One result of the separation between distributors and their suppliers is the way in which European distributors support their clients. Distributors vary widely, both in the range of products they carry and in the amount of technical information and support they give their clients.

European distributors tend to offer more support to their customers in terms of technical assistance and design information, sometimes including the translation of relevant information into the local language. Because of this technical orientation, European distributors tend to direct their sales efforts toward the engineering force where design-ins occur.

The largest distributor of electronic components in Europe is R.S. Components, which is part of the Electrocomponents group. This company is virtually unique in the European distribution scene, since it sells only own-brand components.

Of the franchised distributors in Europe, the largest is probably Unitech, which operates mainly in the United Kingdom and West Germany. Unitech achieved its position partly by the acquisition of the West German distributor Enatechnik. Other major European distributors include Diploma, Farrell, ITT Electronic Services, and Jermyn, based in the United Kingdom; CDME and Tekelec in France; and Spoerle in West Germany. Several of these distributors operate in a number of West European countries. There is also a large number of small distributors, with sales of $2 million to $10 million, operating throughout Western Europe.

Most of the U.S. and Japanese companies operating in Western Europe rely on a combination of direct sales and distribution, with the proportion varying from company to company. The establishment of manufacturing facilities in Europe by a number of U.S. and Japanese manufacturers will allow them to sell directly into the European market without the handicap of the 17 percent customs tariff imposed by the European Economic Community.

6. Sources and Logistics

MARKETING CHANNELS IN THE FAR EAST AND REST OF WORLD

Semiconductor marketing channels in the Far East, including Japan and Rest of World (ROW) countries, sometimes include the services of agents resident in the customer's country. Due to local law, custom, or tradition, some semiconductor customers cannot buy, or they refuse to buy, directly from foreign suppliers, and local agents (importers) are invaluable in establishing a mechanism for sales transactions to take place.

Local representatives and distributors are used extensively by many international semiconductor suppliers. In many countries in the Far East and ROW, these representatives and distributors function as stocking representatives; they often offer substantially more technical and applications support than regular distributors.

WHY USE DISTRIBUTION?

Procurement of semiconductors involves some element of risk and creates a short-term need for credit. In a sense, a semiconductor distributor acts as a financial institution and as an insurance company.

From the standpoint of risk assumption, a distributor provides a means of smoothing out the "peaks and valleys" of product shipment flow from supplier to customer. If shortages occur, the distributor usually anticipates the general market condition and has stock on the shelf to compensate. The distributor may also carry alternate source products, which may help. If the customer reschedules an order to a later date, there may be less legal obligation on the part of the customer regarding interruption of product flow.

Smaller user organizations often use the distributor as a souce of financial aid, especially during startup of a new enterprise. It may not be desirable or even possible to negotiate an annual purchasing agreement with semiconductor suppliers until the user has established a "trade record" or has reached a business level that warrants doing so. In this case, the user can establish a level of business, with associated terms and conditions, through a local distributor and use the often precious startup capital for other aspects of the business. Also, many order sizes are too small to be economically processed on a direct factory basis. In addition, it is sometimes possible to negotiate more liberal terms of payment with a distributor than with a supplier.

Larger and more established companies frequently use a combination of distribution and direct purchases to achieve a more balanced business posture, for all of the reasons described above.

6. Sources and Logistics

WHY BUY DIRECT?

Under certain circumstances, it may be to the user's advantage to deal directly with the semiconductor manufacturer. These circumstances are different for the purchase of standard products compared with purchase of custom and semicustom products.

Standard Products

The semiconductor user who makes annual purchases of $500,000 or more of semiconductor devices may benefit in a number of ways from dealing directly with a semiconductor manufacturer. Since the purchase is made directly, the buyer should be able to obtain more favorable pricing than that available from a distributor. In times of product shortage the purchaser has the advantage of having fewer allocation points between him and the source of supply. Direct contact between the semiconductor purchaser and the manufacturer is almost certain to lead to better business and technical communication than is possible through intermediaries. In the case of a really large purchaser, a direct vendor/purchaser relationship becomes almost essential if the vendor is to be able to commit adequate resources to satisfying the purchaser's needs.

The user who needs an assured source or sources of supply will need to meet a number of conditions in order to be able to purchase directly from a semiconductor manufacturer. Most semiconductor manufacturers require a commitment to purchase at least $250,000 worth of devices per year. (Some large manufacturers may demand an even higher commitment.) Semiconductor manufacturers are usually only willing to establish a direct sales agreement with companies whose credit history is acceptable to them, and whose current and projected growth rate equals or exceeds the overall electronics industry growth rate. The need for a relatively small number of product families or part types makes the user more acceptable as a direct customer because the semiconductor manufacturer is looking not only for a large total order but also for large orders for individual parts. Because the user needs to commit to relatively large order releases with infrequent rescheduling, the ability to forecast semiconductor requirements accurately a year or more in advance is very important, especially in an expanding economy.

Custom and Semicustom Products

Another reason for dealing directly with suppliers is the requirement for custom or semicustom semiconductors. It would be very difficult to maintain design security and integrity when dealing through a third party, and the resulting delays and increased costs could be disastrous. Some considerations are:

- Who owns the parts?

- Who is responsible if the design is compromised?
- Who pays for rejects?
- Who pays for design errors?

All of these problems tend to become less difficult to resolve in a direct user-supplier relationship. In any case, the level of business must be such as to command the required attention to detail.

INTERNATIONAL PROCUREMENT

Many difficulties may arise due to the complexity of international procurement of semiconductors. It is very important that users dealing internationally be aware of some of the possible pitfalls. Consider the following example:

> A West European customer in country A buys semiconductor components from a Silicon Valley supplier through a West European sales office in country B. The customer's assembly plant is in Southeast Asia while the semiconductor supplier's assembly and test facilities are elsewhere in Southeast Asia. The customer is presented with a very interesting problem in the economics of negotiating an annual pricing agreement, and with an even bigger challenge in minimizing the cost of losses due to component fallout at systems test (at a facility in Western Europe). If the product involved is a transistor, the solutions to these problems may be quite different from those for a VLSI device.

Semiconductor purchasing at the international level can be classified as the following:

- Import procurement—product is purchased from a non-domestic supplier for domestic use
- Export procurement—product is purchased domestically for non-domestic use
- Foreign (non-domestic) procurement—product is purchased in another country for use in another country

Each of these situations requires special expertise because of the complexities introduced by additional laws, multiple currency transactions, language barriers, customs, licensing, and cultural and ethical differences.

6. Sources and Logistics

There are many organizations throughout the world designed to facilitate international trade. These include the following regional pacts:

- Organization of American States (OAS), formed in 1948, has broad economic, political, and defense goals for North and South America.

- European Economic Community, comprises Belgium, Denmark, France, Greece, Italy, Luxembourg, the Netherlands, West Germany, the United Kingdom, and Ireland. This community has special agreements with the United States, several Middle East nations, and many African countries. All trade tariffs between members were abolished in 1968, and the goal of the members is to eliminate all trade barriers among themselves.

- Benelux Economic Union, formed in 1948, with the same objectives as the European Common Market. Members are BElgium, the NEtherlands, and LUXembourg. A trade agreement between Benelux and the Soviet Union has existed since 1971.

- European Free Trade Association (EFTA), comprises Austria, Ireland, Norway, Portugal, and Sweden. Finland is an associate member of EFTA. EFTA does not regulate trade outside its group.

- Other organizations, such as the North Atlantic Treaty Organization (NATO), Southeast Asia Treaty Organization (SEATO), Warsaw Pact, World Bank, and International Monetary Fund (IMF), have varying effects on international trade. The possibility of embargo always exists, and could have a major impact on semiconductor supplies in the international marketplace.

Import procurement requires a knowledge of political as well as cultural implications. Communications problems are magnified because of the high cost of travel and the resulting greater reliance on telephones, telexes, and the printed word. Attitudes toward contractual obligations are often different from those experienced in domestic relationships.

Semiconductor procurement for military and government applications may place severe limitations on the use of non-domestic products because of the strategic implications of supply-demand fluctuations. This problem is of particular importance to programs that have stringent cost limitations. It is not unusual for a semiconductor supplier to locate 100 percent of its high-volume plastic and cerdip assembly and test capacity for a particular product in Southeast Asia. Requiring such a supplier to perform all its operations in Western Europe or the United States could dictate the need for a multimillion dollar capital investment requirement on the part of that supplier.

6. Sources and Logistics

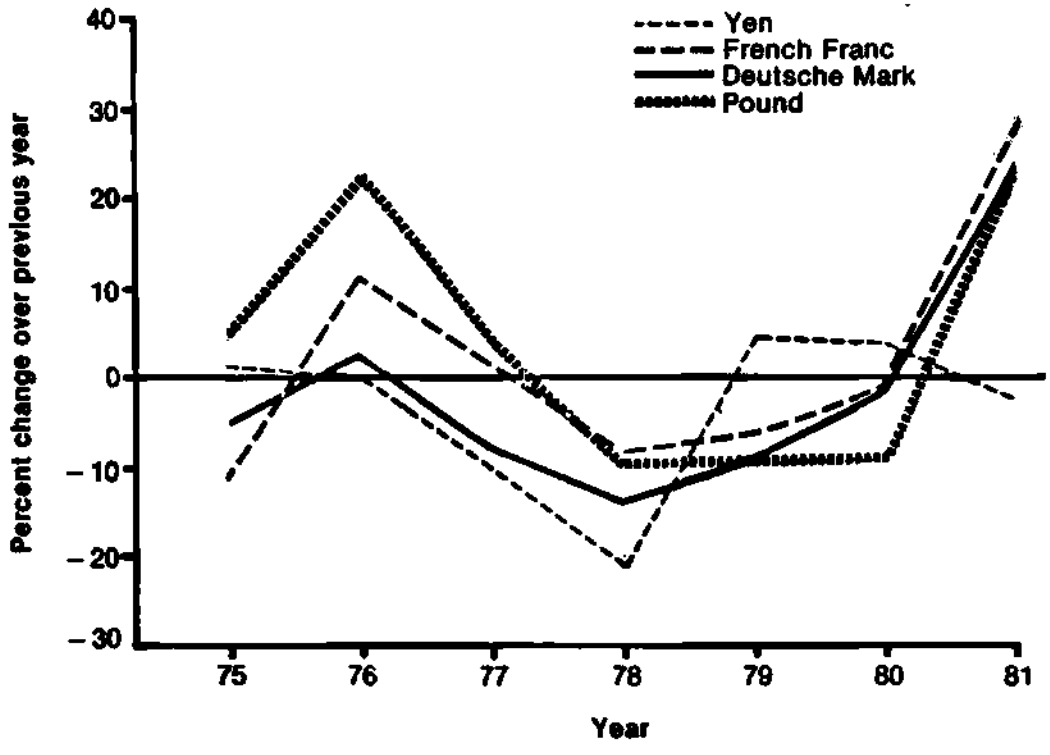
Demands that reciprocal trade occur as a condition of doing business internationally, are increasing. Such trade requirements involve offset purchases or counter purchases, and may be satisfied by bartering in some cases. Some U.S. companies have formed their own trading companies as a means of accommodating these requirements.

Currency fluctuations present unique risks in international procurement of semiconductors. These risks include sudden currency devaluations by government mandate, currency strengthening or weakening as a result of international money market supply/demand changes, and the costs of exchange or currency conversion. Fortunately for U.S. buyers, payment for imports in U.S. dollars is the general rule. The semiconductor buyer involved in importing semiconductor products from non-domestic sources should seek the assistance of the financial, accounting, and legal departments to reduce currency risks. Figure 6-1 illustrates the year-to-year fluctuations of the Deutsche mark, the French franc, the pound sterling, and the yen against the U.S. dollar between 1975 and 1981.

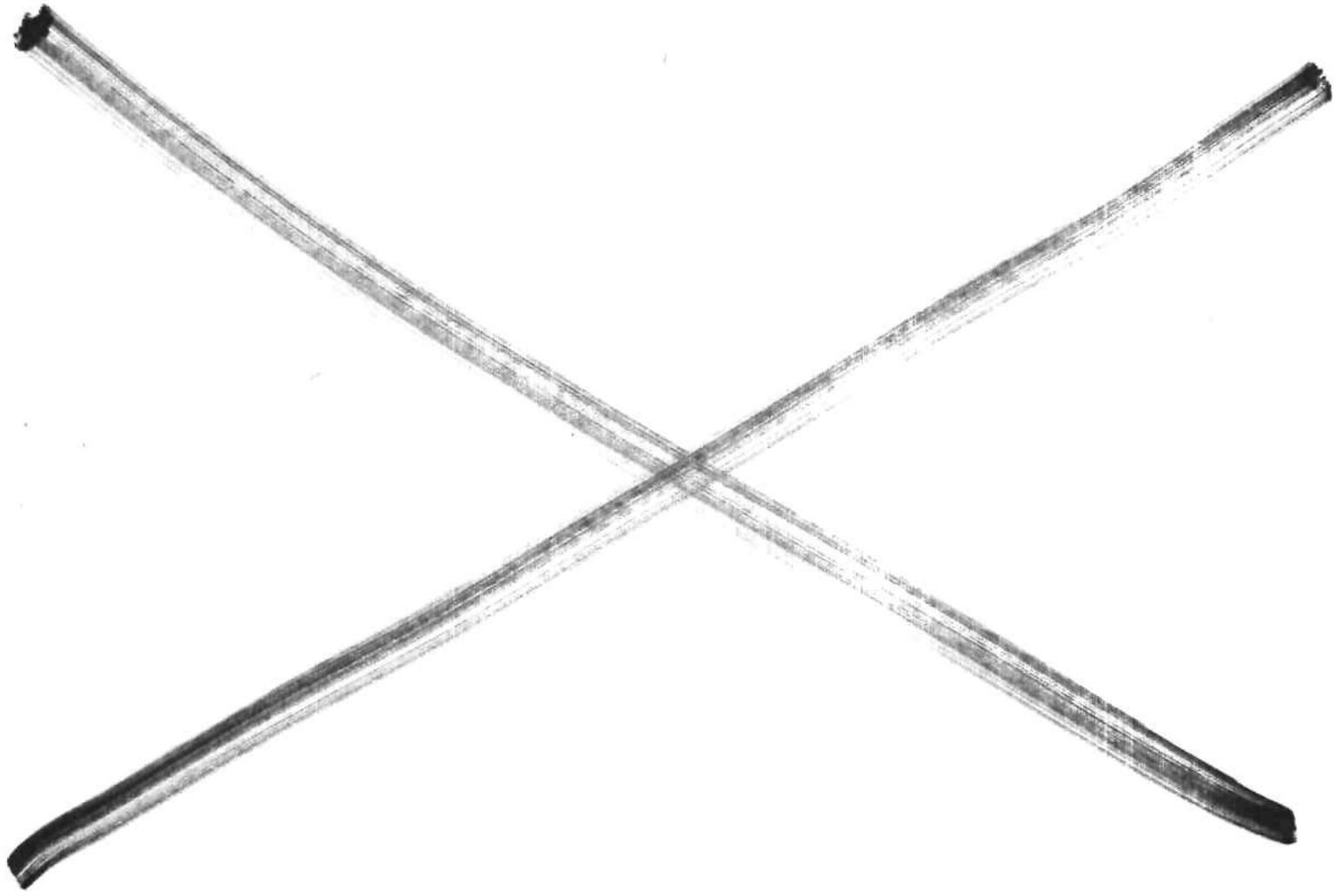
6. Sources and Logistics

Figure 6-1

YEAR-TO-YEAR CHANGES IN THE EXCHANGE RATE
BETWEEN THE U.S. DOLLAR AND OTHER MAJOR CURRENCIES
(Percent)



Source: DATAQUEST, Inc.
April 1982



Nielsen Dataquest

INQUIRY RESPONSE

DATE: 4/4/84

TO: Don Anker/Fisher Controls

FROM: Jean Page/Dataquest

This information has been compiled in response to your inquiry of March 1984

Please file in Section 7 for future reference.

1. Who is supplying 2-port RAMs? What is the trend?

Answer: Current suppliers include Texas Instruments, Synertek, and Mostek. The Mostek part is 512x9 (includes a parity bit). There is a definite trend to smart memory devices, fueled by the growth of co-processors.

2. What is the future of 2Kx8 static RAMs in terms of availability?

Answer: Hitachi currently has 30-35% of this market but is not trying to increase its share. They are not even increasing production to match growth in demand.

The 8Kx8 device is a better buy. Current ASP is $20. ASP for 1984 is expected to be $15. Hitachi is producing 500K parts/month and has two-thirds of the market. Toshiba has about 20% of the market. Sony is just entering the market. U.S. suppliers will come along later.

:tg

cc: Bob Case, Manager

Nielsen Dataquest

INQUIRY RESPONSE

DATE: 2/14/84

TO: M. Allie/D.A.I.I.

FROM: Stan Bruederle/Dataquest

This information has been compiled in response to your inquiry of January 1984

Please file in 7. Product Analysis for future reference. Volume I

Subject: Telex relating to OTP EPROMs.

Over the past several years, EPROMs have continually made inroads into the MOS ROMs market. This has been due to improving price competitiveness of EPROMs of any given density as well as the fact that EPROMs are generally easier to use; can be stored and inventoried, do not require the lengthy turnaround that mask ROMs do, and can be economically used with smaller volume runs. The OTP, which has begun to emerge in 1983, will further increase this penetration.

Initial pricing of OTP, at about 10 percent less than conventional windowed EPROMs, will probably lead to a greater impact on the EPROMs market initially than on the ROMs. However, the 10 percent discount does not, by any means, reflect the expected manufacturing cost savings. As the OTP market becomes more competitive, it is expected that the OTP discount, compared with EPROMs, will get larger and larger, thereby increasing the impact on the ROMs market. We expect this to occur over the 1984 to 1988 timeframe. By 1988, windowed EPROMs will be used only in prototyping applications and in the initial product of any given density that is introduced on the market. In these two instances, the reprogrammability feature is required:

1. to insure that recoding can be done to reflect the changes in the software or correct errors in the initial coding, or

2. from an economic basis, where the part is too expensive to be used only once, but must be reused again and again.

As the EPROM drops in price to 6 to 8 dollars, it is expected that the OTP parts will become the dominant choice for production runs.

ROMs have continually been running at higher densities than EPROMs at any given point in time. It is at these high densities that ROMs are expected to be in their most secure market. However, in the more mature densities, presently 32K and 64K devices, it is expected that OTP can make very significant inroads into the ROMs market, perhaps as much as 30 or 40 percent, once the OTP market price truly reflects the manufacturing cost economics plus a fair margin to the manufacturer.

Applications of EPROMs and initially OTP devices are very widespread and generally follow the same applications that microprocessors do. While many of the highest volume applications utilize a single chip microcontroller, microprocessors with EPROM can be widely found in a variety of microcomputer boards, industrial applications, consumer devices, automotive electronics, and a variety of small office systems. Late in 1982, EPROMs became widely used as a quick turnaround device for the video games industry. However, if the market window had been lengthier, ROMs were, by far, the preferred economic choice. This type of application, should it appear in another form such as cartridges for the IBM PC Jr., would be an attractive application for OTP as well. The table below provides DATAQUEST's estimates of the approximate end-user markets for the combination market utilizing non-volatile memory forms, such as mask ROM, OTP, and UV-EPROM.

ESTIMATED MOS NVM USER MARKETS
(% of Total Units)

	ROM		EPROM/OTP	
	1983	1988	1983	1988
Consumer	42%	32%	18%	30%
Communication	9	15	16	15
Industrial	10	9	25	22
Computer/Office	37	42	38	30
Gov't/Military	2	2	3	3
	100%	100%	100%	100%
Total Units	220M	552M	145M	657M

Source: DATAQUEST
January 1984

:tg

Nielsen Dataquest

INQUIRY RESPONSE

DATE: 2/9/84

TO: Doug Haggen/AT&T Technologies

FROM: Stan Bruederle/Dataquest

This information has been compiled in response to your inquiry of February

Please file in Section 7 for future reference.

I have enclosed all the information that I could find about EEPROMs. The 1983 WESCON paper and EDN article discuss the data protection feature. The other two discuss floating gate vs. MNOS. I have included a list of EEPROM suppliers. As you can see there is a lot of action in CMOS. Hughes will not be the only supplier.

As far as Hughes is concerned there is no specific financial data available on them. However, we believe they are profitable, they have been in the business for a long time, and they have a history of supporting their customer product requirements, even though they move in and out of specific product areas from time to time.

Motorola, SEEQ, Rockwell, Zilog, and T.I. are known to be doing work on microcontrollers with EEPROM on board.

Motorola,	68XX
Zilog-SEEQ,	Z8X
T.I.-SEEQ,	TMS 7000
Rockwell-SEEQ,	65XX

:tg

Nielsen Dataquest

INQUIRY RESPONSE

DATE: 30 August 1983

TO: Tammy Sullivan, Xebex Systems

FROM: Stan Bruederle SAB

This information has been compiled in response to your inquiry of August 1983

Please file in Section 7 for future reference.

Subject: Z80 Shipments

We track quarterly shipment data for the Z80. Shipments for the last six quarters are tabulated below. All manufacturers are presently allocating product as first and second quarter 1983 shipments were 57% higher than fourth quarter 1982. Most of this increase was shipped into consumer applications. Apparently, Zilog's lawsuit against NEC caused NEC shipments to decrease by almost 50%. We do not believe that there should be any long-term effect of the lawsuit on NEC's shipments as any settlement should involve payment for rights to manufacturers rather than stopping production. In the short-term, NEC may have some product available until demand for their products increases again.

We do not have similar data for the two peripheral devices you asked about. There are many different types and numerous suppliers. We are starting a project in this area but won't have data for six months to a year.

Z80 SHIPMENTS
(units in thousands)

Company	1Q82	2Q82	3Q82	4Q82	TOTAL	1Q83	2Q83
Zilog	900	1,100	1,100	1,200	4,300	1,700	1,986
Mostek	350	380	380	540	1,650	1,400	1,700
NEC	800	700	1,100	1,300	3,900	1,810	990
SGS-Ates	200	220	220	330	990	429	600
Sharp	80	90	110	120	400	150	175
TOTAL	2,330	2,490	2,910	3,490	11,240	5,489	5,451
% Change	-	6.9%	16.9%	19.9%	-	57.3%	(0.7%)

cc: Jim Toreson, Xebec
Marsha Glow, Xebec

:tg

7. Capacity

Semiconductor usage has grown dramatically since the 1960s. Utilization of semiconductor functions such as gates and memory bits is growing at a rate of approximately ten times every five years. This section discusses the growth in capacity of the semiconductor industry to meet users' demands, and addresses potential supply/demand mismatches due to the constraints involved in changing industry capacity.

SEMICONDUCTOR CONSUMPTION

Historical data on semiconductor shipments and consumption show the ability of suppliers to respond to demand. This information is, therefore, a first-order measure of industry capacity over an extended period of time. The semiconductor market has grown rapidly in most years. It is highly competitive and comprises a large number of profit-motivated corporations. Because of these factors, overcapacity has not existed in the semiconductor industry for more than one to two years at a time. Historically in every case, overcapacity preceded periods of very long lead times (26 weeks or more) and constrained user growth. Thus, the semiconductor user needs to understand the ability and limitations of the industry in terms of changing its manufacturing capacity.

Figure 7-1 illustrates the growth in free world shipments from the regions shown. Figure 7-2 shows semiconductor consumption of shipments from all free-world sources by each of the regions shown. Figures 7-3 and 7-4 show the market consumption of major categories of semiconductor components. The dramatic growth rates forecast for the years 1983 through 1985, coupled with the increased pervasiveness of semiconductor applications, imply that the 1981-1982 semiconductor overcapacity situation will be short-lived. This means that the user should be prepared to cope with increasing lead times and the possibility of constrained growth, if sufficient forward buying is not possible.

CAPACITY FACTORS

Semiconductor industry capacity is determined by many complex, interrelated factors. As the industry has grown, more of these have become global issues. The primary factors that determine the available capacity for the semiconductor industry are:

- Floor space—equipped and operable
- Equipment—maskmaking, wafer fab, assembly, test
- Raw Materials—wafers, chemicals, package piece-parts, utilities

7. Capacity

- Trained personnel—engineers, operators, assemblers, technicians, inspectors, managers

- Capital—for updating and expansion of facilities

Industry requirements for floor space vary from company to company, depending upon the relative complexity of the products and the degree of product standardization. Thus, actual floor space is a crude measure of capacity and can be misleading.

Installed equipment is also a very rough indicator of industry capacity, because equipment utilization varies widely from initial installation to obsolescence, and obsolescence can occur very rapidly (often 3 to 5 years). Another problem with using installed equipment as a measure of industry capacity concerns the complexity of devices and processes being run on the equipment. For example, a 4-inch wafer fab line may be used to produce 2,000 functional bipolar TTL SSI circuits or 15 functional NMOS 64K RAMs per wafer at a given point in time. The 2,000 TTL SSI circuits would have a net value of $700 at $0.35 ASP, compared to $105 for the 15 pieces of 64K RAM at $7 ASP. This means that equipment count is a poor indicator of dollar volume and unit volume capacity.

Raw silicon wafer production capacity is not a very useful measure of semiconductor industry capacity, because (1) it leads wafer consumption by four years or more, and (2) a large percentage of crystal growth is captive to sources that do not publish or make available production data.

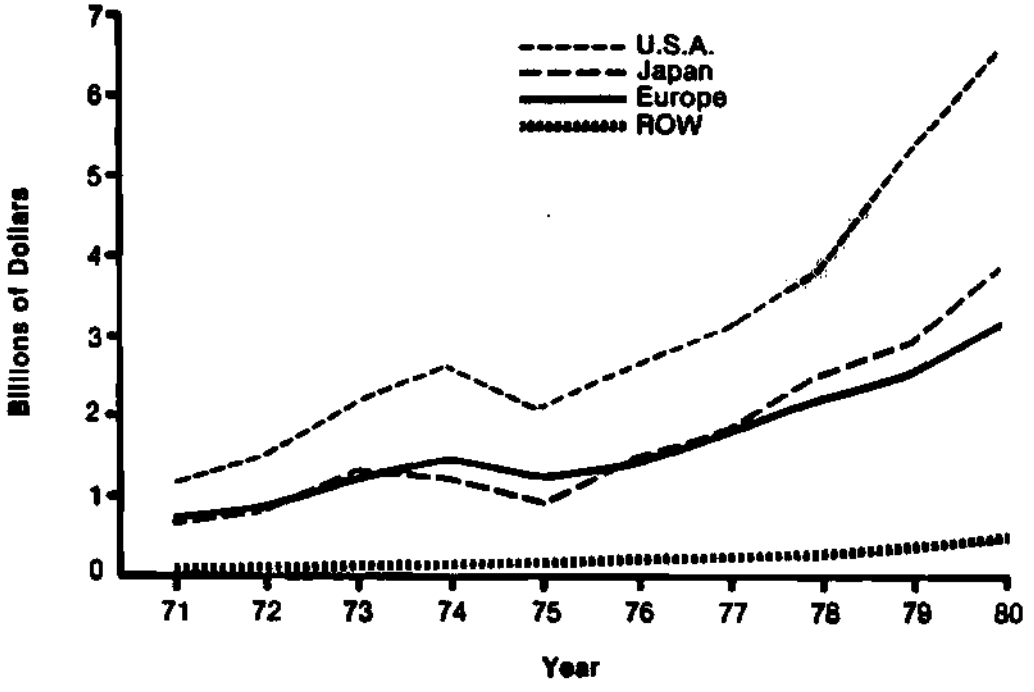
Consumption of raw materials, particularly wafers and package piece-parts, provides a reasonably good measure of industry capacity when the market is supply constrained, as was the case in 1978-1979. In a recession, capacity is more difficult to measure by this method because of raw material surpluses. Studies of U.S. semiconductor suppliers by the Semiconductor Industry Association (SIA) in 1980 indicate that during the 1975-1979 time period, wafer consumption grew at an annual rate of approximately 27 percent, while wafer fab capacity utilization increased from 74.3 percent to 90.1 percent over the four-year period. These data are summarized in Table 7-1.

As shown in Table 7-1, effective capacity grew by a factor of 3.15 (CAGR of 33 percent) during the last period of rapid economic expansion (1975-1979). Sales during this same period grew from $4,373 million to $11,116 million, or a CAGR of 27 percent. Thus, in an inflationary economy, it was necessary for the effective capacity to increase more rapidly than the dollar volume of sales increased. However, expansion in terms of the other parameters, such as floor space and equipment, grew at only 21 percent CAGR. The difference was due to increased efficiency of utilization as indicated in Table 7-1.

7. Capacity

Figure 7-1

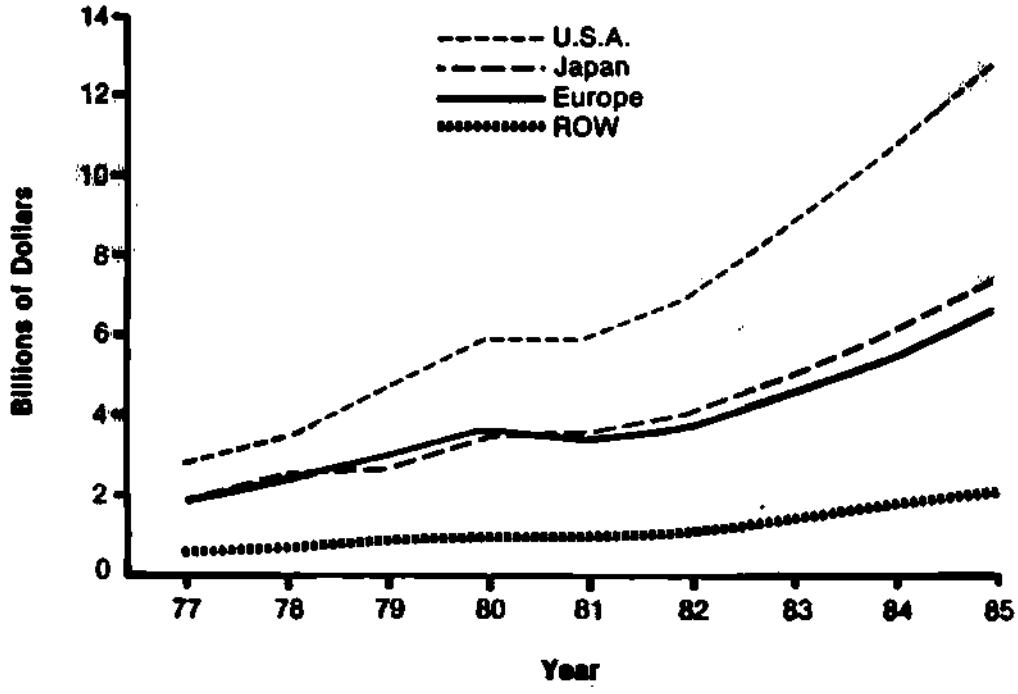
ESTIMATED FACTORY SHIPMENTS
BY REGION
(Billions of Dollars)



Source: DATAQUEST, Inc.
April 1982

Figure 7-2

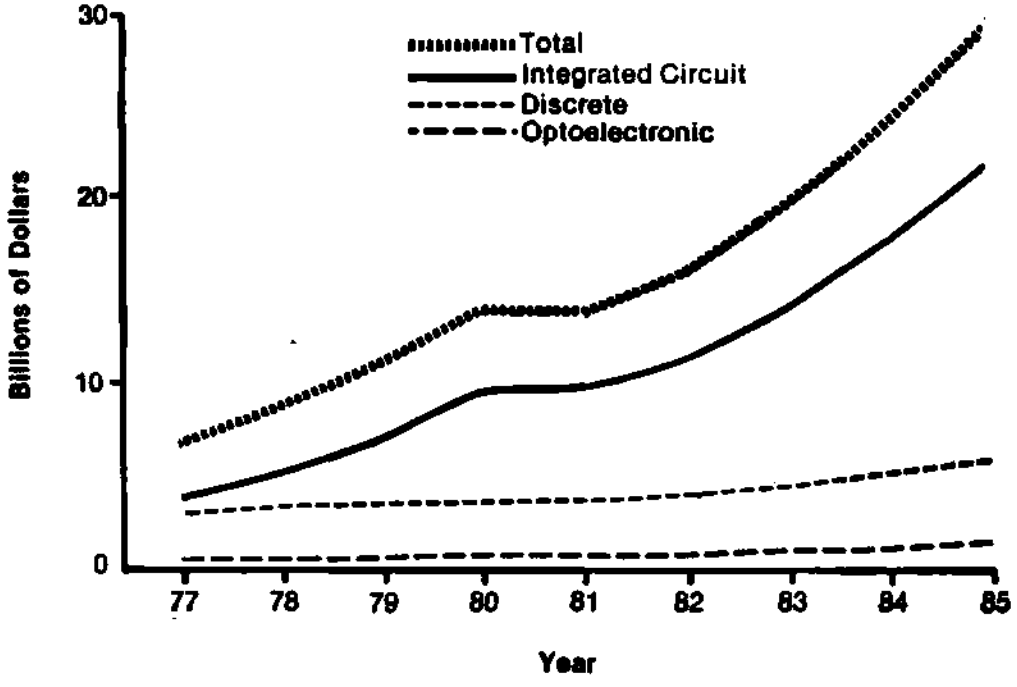
ESTIMATED SEMICONDUCTOR CONSUMPTION
BY REGION
(Billions of Dollars)



Source: DATAQUEST, Inc.
April 1982

Figure 7-3

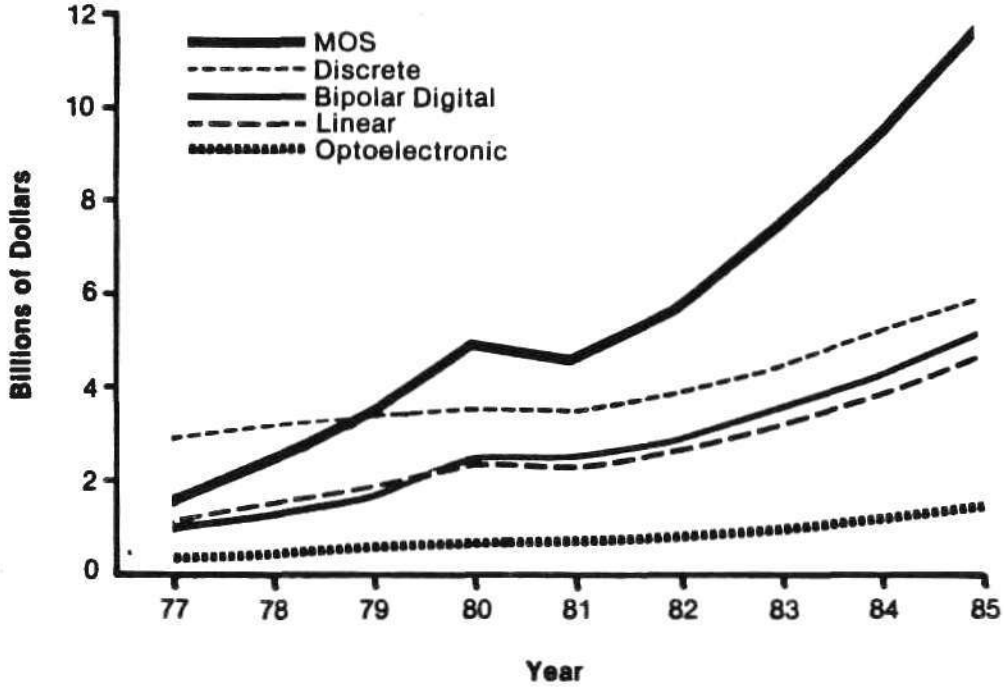
ESTIMATED WORLDWIDE SEMICONDUCTOR CONSUMPTION
BY TECHNOLOGY
(Billions of Dollars)



Source: DATAQUEST, Inc.
April 1982

Figure 7-4

ESTIMATED WORLDWIDE SEMICONDUCTOR CONSUMPTION
BY MAJOR CATEGORY
(Billions of Dollars)



Source: DATAQUEST, Inc.
April 1982

7. Capacity

Table 7-1

1975-1979 SILICON CONSUMPTION AND UTILIZATION

	1975	1976	1977	1978	1979	CAGR
Normalized Wafer Consumption	100	127	161	205	260	27%
Wafer Fabrication Capacity Utilization	74.3%	78.7%	82.1%	85.0%	90.1%	
Normalized Employed Capacity	100	133	178	235	315	33%

Sources: SIA Reports
DATAQUEST, Inc.
April 1982

Assembly seal production comparison is another way to measure change in industry capacity. For the 1975-1979 time period, our estimates of effective seal capacity growth are summarized in Table 7-2 for both integrated circuits and discrete devices. Thus, effective industry capacity to produce integrated circuits grew by a factor of 4.86, or 48.5 percent CAGR during the four-year period. Discrete capacity increased at a much slower rate, 21.5 percent per year. During this time, IC seal facilities and equipment were added at an annual rate of 25.1 percent, and discrete capacity was added at 11.1 percent per year. The higher effective seal capacities shown in Table 7-2 resulted from more efficient usage.

A major capacity-constraining factor during periods of rapid economic expansion and semiconductor industry growth is the availability of trained, experienced personnel. The period from 1977 to 1979 saw record recruitment activities in Silicon Valley and other highly concentrated areas of semiconductor facilities. Special categories of expertise such as fab equipment operators and test equipment maintenance can be extremely difficult to staff once economic recovery has occurred. The need to train newcomers to the industry during rapid economic expansion places a heavy burden on the existing staff and may actually decrease efficiency below that experienced during a recession. This is a primary reason for the reluctance of many semiconductor company managements to reduce staffing through any means other than "normal" attrition during the 1981-1982 soft market conditions.

7. Capacity

Table 7-2

1975-1979 SEAL CONSUMPTION AND USAGE

	1975	1976	1977	1978	1979	CAGR
Integrated Circuits:						
Normalized Seals Consumed	100	140	196	274	384	40%
Seal Utilization	74.25	78.0%	82.3%	86.4%	94.0%	
Normalized Effective Seal Capacity	100	147	217	319	486	48.5%
Discretes:						
Normalized Seals Consumed	100	118	140	166	197	18.5%
Seal Utilization	76.8%	76.2%	76.5%	79.8%	85.0%	
Normalized Effective Seal Capacity	100	117	139	172	218	21.5%

Sources: SIA Reports
DATAQUEST, Inc.
April 1982

SUPPLY/DEMAND RELATIONSHIPS

The semiconductor user must cope with rapid changes in the supply/demand relationship, especially during periods of economic expansion. The following points must be considered when placing new orders or adding requirements to existing orders for semiconductors:

- First in, first out (FIFO)—Good business practice dictates that suppliers satisfy the oldest backlog first.
- "Pipeline" length—The semiconductor manufacturing process can range from 12 to 18 weeks in length for standard commercial products, with an additional 2 to 12 weeks for special processing, assuming no capacity limitations.
- Dice bank to finished goods—This interval can range from 4 to 12 weeks for offshore assembly, assuming no assembly capacity limitations.

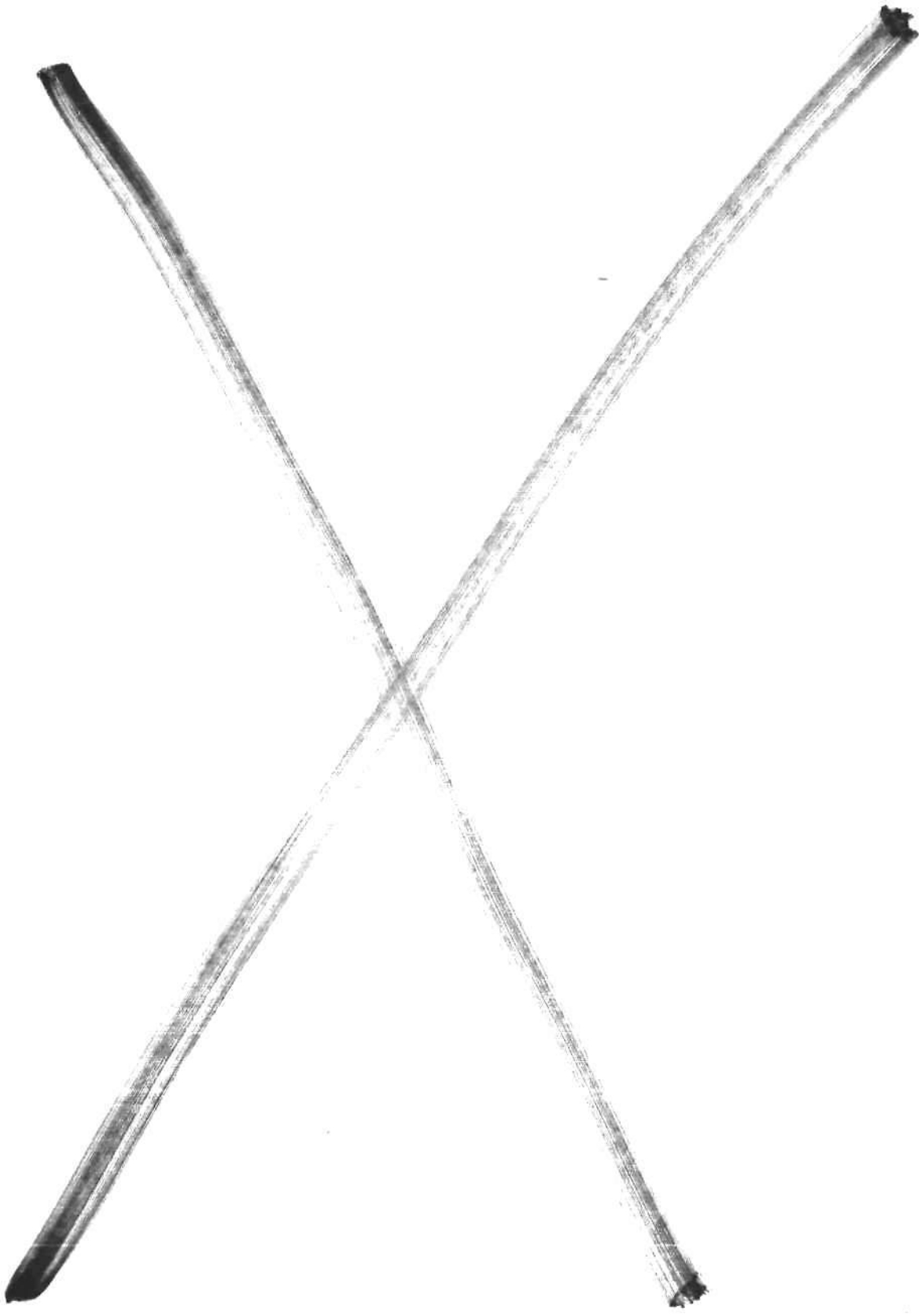
7. Capacity

- Recruitment and training—From time of interview, approximately six weeks of hiring and orientation time plus an additional six weeks or more of training time are required to staff existing idle capacity.

- Equipment lead time—Semiconductor manufacturing equipment lead times vary from a few days, in a very soft market, to 18 months in a strong market.

- Facilities expansion—The time required to expand capacity by enlarging or adding wafer fabrication facilities ranges to 24 months or more.

In a market transition period, the previously mentioned lead time factors may be encountered in rapid succession. A semiconductor product may experience a lead time change of 20 weeks or more within an interval of only 1 to 2 weeks. The situation is driven by the rate at which customers place orders, and the percent of capacity used prior to the rapid upsurge in demand.



Nielsen Dataquest

INQUIRY RESPONSE

DATE: April 12, 1983

TO: Jim Toreson & Marcia Glow
Xebec Corporation

FROM: Stan Bruederle, Manager,
Semiconductor User Information Service

This information has been compiled in response to your inquiry of March '83

Please file in Vol. I, Sect. 8 for future reference.

Subject: Custom IC Costs and Suppliers

I developed a cost model for a 1000 gate array similar to the one you are buying from LSI Logic in Table 1. Since LSI Logic buys their wafers from an outside source their cost structure is different from a company that makes their own wafers. I have estimated LSI Logic's wafer costs at $205. Since they have to pay their suppliers a reasonable profit, their cost will be somewhat higher than if they made them themselves even though they don't have depreciation costs to cover. We also assume that the difference in the die sizes between standard and gate arrays is inactive area, so the yields are essentially the same. The variable margin assumptions are based on experience and generic industry data.

For high volumes, standard cell designs are clearly lower cost than gate arrays. I have found the following companies in our files that make custom products with standard cell approaches. Zymos is clearly one of the more aggressive companies with second sources in Intel and Standard Microsystems. Other companies appear to be sole source at this time for standard cells with analog functions while Telmos is offering gate arrays with analog functons. Companies for which profiles are included in your Semiconductor User Information Service notebooks are indicated by an asterisk (*). We can provide you with information from our files for any other company you are interested in.

Companies making standard cells
or some form of custom ICs

VLSI Technology	Zymos	Alternate Sources
IMP	Intel	
Synertek	Standard Microsystems*	
Array Technology (NCR)	NEC*	
Harris*	Toshiba*	
RCA	Silicon Systems (+ Analog)	
AMI	United Technology/Mostek	
Signetics*	Cherry Semiconductor*	

Note: Telmos* also offers gate arrays with precision analog circuits on chip.

	LSI Logic Gate Array*	Other Gate Array**	Standard Cell*	Standard Cell**
Die Size	210 x 210	210 x 210	165 x 165	165 x 165
Gross Die Per Wafer (4")	256	256	415	415
Wafer Cost (less metal)	165	-	165	-
Processing Cost (metal)	30	-	30	-
Fab Yield	95%	-	95%	-
Finished Wafer Cost	$205	$110	$205	$110
Cost Per Gross Die	$0.80	$0.43	$0.49	$0.27
Probe Cost	$0.10	$0.10	$0.10	$0.10
Probe Yield	40%	40%	40%	40%
Probed Die Cost	$2.25	$1.32	$1.48	$0.91
Assembly Cost (40 per pkg.)	$0.20	$0.20	$0.20	$0.20
Assembly Yield	95%	95%	95%	95%
Assembled Die Cost	$2.58	$1.60	$1.76	$1.17
Final Test Cost	$0.15	$0.15	$0.15	$0.15
Final Test Yield	90%	90%	90%	90%
Tested Unit Cost	$3.03	$1.95	$2.13	$1.47
Mask and Pack Cost	$0.005	$0.005	$0.005	$0.005
Mask and Pack Yield	99%	99%	99%	99%
Total Variable Cost	$3.07	$1.97	$2.15	$1.49
Low Volume Variable Margin	67%	75%	67%	75%
Low Volume Price	$9.30	$7.90	$6.52	$5.95
High Volume Variable Margin	60%	67%	60%	67%
High Volume Price	$7.67	$5.90	$5.38	$4.51

*Wafers purchased from outside source
**Wafers manufactured internally

cc: John Randall

8. Cost Trends

The semiconductor industry is the leader in modern industrial society in terms of productivity gains and resultant cost reductions. The user cost per transistor has decreased at an average rate of more than 35 percent per year for the last 20 years and is expected to continue doing so. This reduction is made possible by the rapid rate of technological progress toward smaller geometries, the efficiencies of scale of mass production existing in the semiconductor industry, and the high degree of competition. This section addresses the experience effects resulting from the above conditions, and discusses cost models and trends for various types of semiconductor products.

LEARNING AND EXPERIENCE EFFECTS

The relationship between accumulated volume of production and the average cost per unit of production has been recognized since the mid-1960s. Available data indicate that the manufacturing cost of producing a semiconductor has been reduced through accumulated experience by about 28 percent for each doubling of accumulated volume. This experience concept is referred to as the learning curve or experience curve. Manufacturers in a competitive environment producing large quantities of particular semiconductors will increase their understanding of the production process as they continue to make the parts. By using the knowledge gained in this way, manufacturers can develop increasingly cost-effective methods of production that will result in a lower total cost of production.

Figure 8-1 illustrates the cost/experience relationship representative of a major bipolar circuit manufacturer. Figure 8-2 shows the generalized learning or experience curve for integrated circuits. The curves are plotted in log-log format. The vertical axis represents production cost per unit in constant dollars. The horizontal axis represents accumulated production experience. The semiconductor user should be aware that the experience curve concept applies to an entire industry or to an entire plant and may not necessarily apply to a single product or product family.

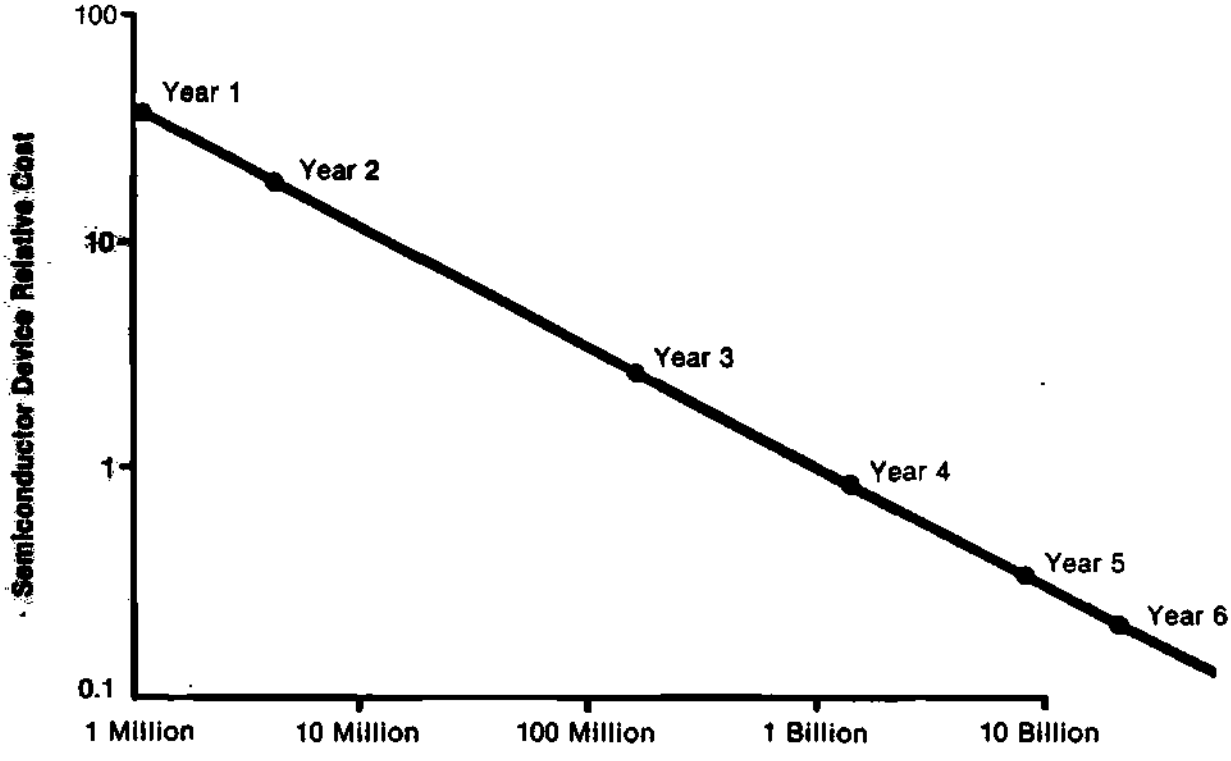
The experience curve concept is relatively complex and therefore easily misunderstood. A common misapplication of the curve is for one to assume that the vertical axis represents current or inflated dollars. It is necessary for the user to convert inflated currency to constant currency (for example, 1972 dollars) before attempting to plot or to make use of an experience curve.

Another common misinterpretation of the curve results when one attempts to modify the horizontal axis with calendar information. It should be noted that considerably more time may be required to increase the factory output or the industry-accumulated output from one billion units to ten billion units than was required to go from one million to ten million units. Thus, there is an irregular compression of the calendar along the horizontal axis, and equal increments of production volume growth do not necessarily occur in equal segments of time.

8. Cost Trends

Figure 8-1

LEARNING CURVE FOR A MAJOR MANUFACTURER'S BIPOLAR CIRCUITS



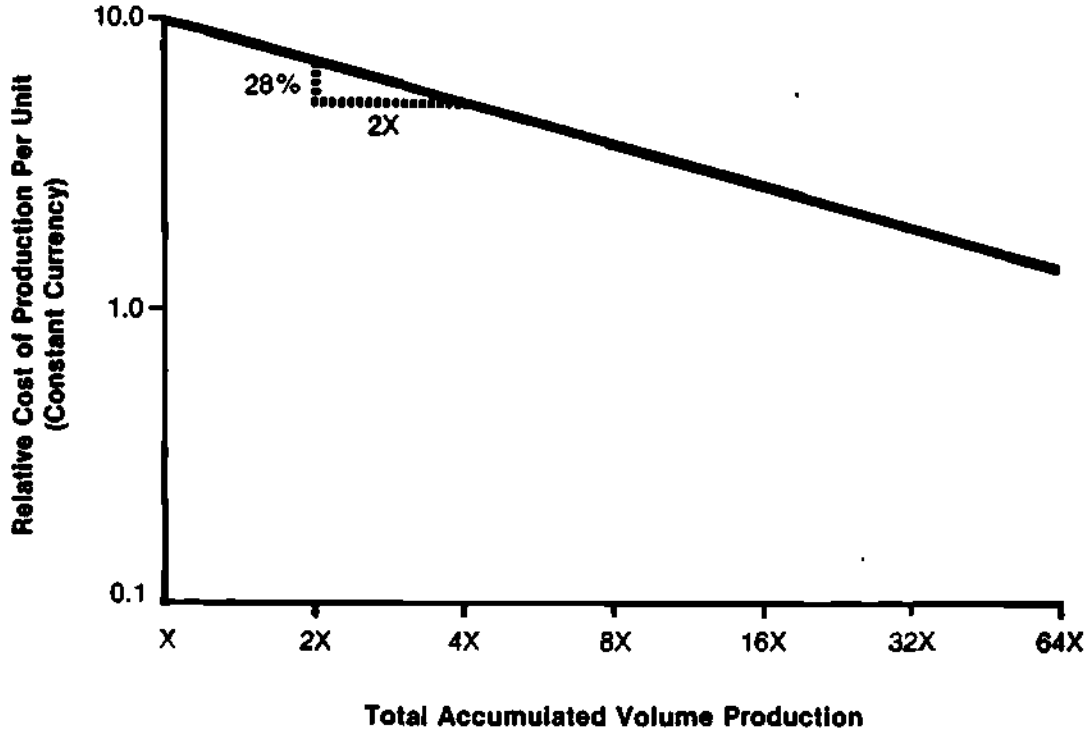
Note: This chart represents a 72 percent learning rate.

Source: DATAQUEST, Inc.
April 1982

A third very common misapplication of the experience curve has to do with the application of the curve to a single product or product family. If a facility or an industry is producing a multiplicity of product types, and if the relative volumes of the product types vary from month to month, an additional variable is introduced into the values assigned to the horizontal axis of the experience curve. For example, a mature product such as the 74S00 TTL gate experiences a different month-to-month production volume variation from that of an ALS MSI device. As a result, total accumulated volume of the two products occurs at different rates, and the two products follow different cost curves with respect to time.

Figure 8-2

GENERALIZED LEARNING CURVE FOR
INTEGRATED CIRCUITS



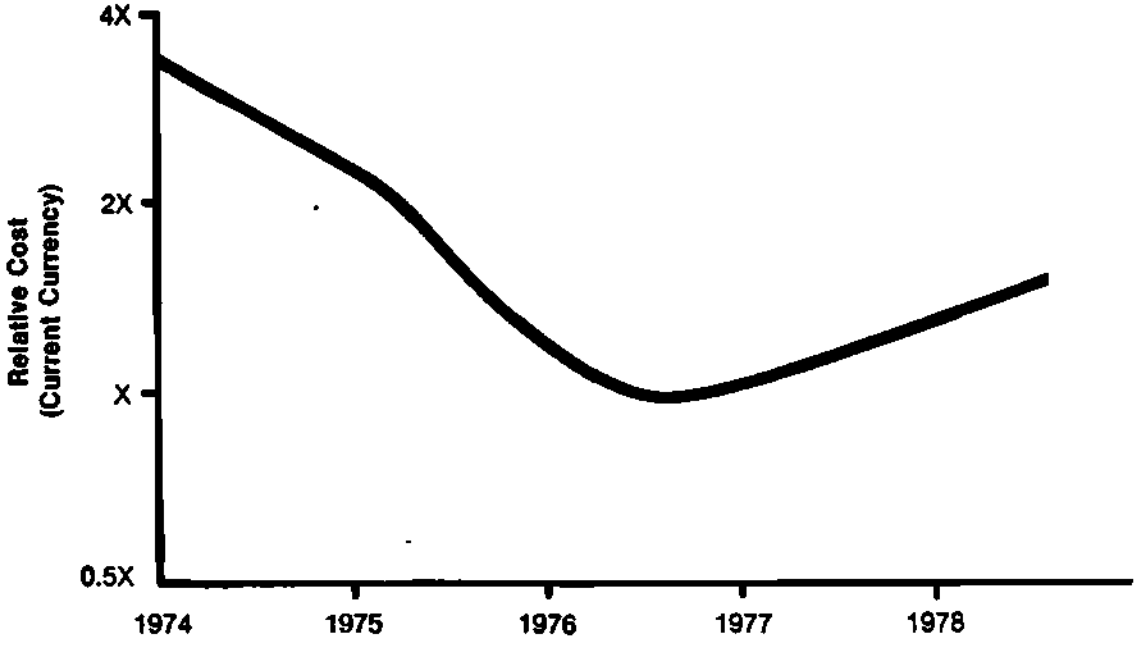
Source: DATAQUEST, Inc.
April 1982

The combination of the three errors described above can result in a graph that is shaped quite differently from the ideal experience curve given in Figure 8-2. One example of accumulated error is illustrated in Figure 8-3. Observe that in this case the total accumulated industry experience is increasing at a rate of less than 2x units per two years of production and that the inflation rate exceeds 10 percent during product maturity. In this particular case, no cost reduction in terms of current dollars was possible after 1977. This trend has also occurred in the automotive industry and in other relatively mature industries, with the net result

8. Cost Trends

Figure 8-3

4K DYNAMIC RAM RELATIVE COST
OVER TIME



Source: DATAQUEST, Inc.
April 1982

being current dollar cost increases from year to year which, in a long-term pure competitive environment, would have an adverse impact on pricing. In such a situation, if profitability in current dollars were a continuing requirement for doing business (as is the case in the United States), such a situation would result in increased pricing.

8. Cost Trends

The cost/experience relationship encompasses all aspects of the product costs. Two examples are the introduction of engineering changes to improve yields and the application of statistical testing techniques to enhance quality assurance. Both represent the application of learning through experience in an attempt to lower the production cost of the product. Thus, it is important for the user to recognize that user feedback to suppliers is an integral part of this overall learning and experience procedure. The following are some of the ways in which the user may assist the supplier in reducing overall costs:

- Provision of data regarding future applications on an on-going basis. This aids the suppliers in developing new products to meet future market requirements.
- Providing data on incoming quality rejects. This gives the supplier feedback regarding the manufacturing and outgoing inspection procedures.
- Providing reliability data regarding field failures of semiconductor devices in the customer's end product. The cost of obtaining these data can be prohibitive for a small semiconductor supplier who is not in the systems business. However, such information may flag minor design or production discrepancies which, when corrected, can result in overall cost reduction.

COST SHARING AND OTHER EXPERIENCE CONSIDERATIONS

The previous discussion may seem to favor the large-volume supplier as having the lowest costs. Indeed, it is true that the large supplier can apply the economies of scale accomplished during past performance to new products as they are introduced into the production line. For example, when a new product is introduced, it is very useful to have in place standards that were established for quality control, testing, and other considerations.

On the other hand, the small supplier need not start from zero. Few companies enter an industry without experienced personnel, and even fewer develop all new production tooling and manufacturing procedures. Therefore, some industry experience has been brought to bear even in the newly organized company; otherwise, it would be impossible for the company to survive. A small company serving a niche market may, in fact, accumulate experience in that niche faster than large competitors. A new company may be able to start with automated equipment that was developed by the industry over the preceding two to five years, giving it a further edge over a larger supplier that has not been able to upgrade equipment in all areas.

8. Cost Trends

The procurement decisions to be made should include careful consideration of the supplier's expected cost of manufacturing. There are many variables, and it is not easy to determine which suppliers will produce which products at the lowest costs in the future. The need for applying sophisticated cost analysis techniques is increasing.

OFFSHORE ASSEMBLY

Intense competition among semiconductor suppliers early in the history of the industry caused many of them to seek nondomestic sources of assembly as a means of maintaining low costs of doing business. Today all of the major companies own or lease facilities in the Far East, and others subcontract assembly operations. The following are examples of Far East cities and countries where semiconductor assembly plants are situated:

- Bangkok, Thailand
- Hong Kong
- Jakarta, Indonesia
- Kuala Lumpur, Seramban, and Penang, Malaysia
- Manila, Philippines
- Seoul, Korea
- Singapore
- Sri Lanka
- Taipei, Illan, and Taoyuan, Taiwan

The advantages of "offshore" assembly operations are many. The cost of labor in the locations named is lower than in the countries where wafers are fabricated. In many instances, tax holidays of as many as 10 years are provided, along with other government concessions such as relaxed depreciation schedules and tax rates. Employee loyalty and consistency are also factors. A six-day work week is not uncommon. Drug usage carries severe penalties, including death, in some countries. All of these factors combine to reduce assembly costs by as much as a factor of three where high volumes are involved.

However, the increased cost of air freight to these offshore sites is causing a careful re-evaluation of offshore assembly. Some companies have made deliberate moves to bring their offshore assembly closer to home (Mexico, for example). Others are seriously considering highly automated assembly plants in the same location as the fabrication plant. The Japanese have been doing this for several years and have relatively little offshore assembly.

COST MODELS

It is important that the user of large volumes of semiconductors have an understanding of the cost of producing those semiconductors. Because manufacturers usually intend to remain profitable, purchasing products below cost, for example, during soft market conditions, would be short-sighted and could cost the user critical sources of supply in the next economic upswing. The motivation of a supplier to sell below cost should always be understood by the user.

Tables 8-1 to 8-6 are cost models that have been developed to assist the user in understanding semiconductor manufacturing costs. They are intended as a guide and should not be interpreted literally. They illustrate the interaction of some of the major variables involved. The user should note that many costs go into each of the line items. For example, the percent yield at wafer sort relates to the quality and mean time between failures (MTBF) of wafer probe equipment; the quality of the chemicals, photolithography, and clean room environment; the experience of the personnel involved; and many other factors. It may be helpful for the user, who may be relatively unfamiliar with semiconductor manufacturing processes, to refer to the manufacturing process flow in Section 12, before attempting to use the cost models.

In the cost models, the processed wafer cost, number of dice per wafer, tester cost per hour, and assembly cost are all empirical data, as are the yield percentages used in each step. The following outline shows how each line of the cost model is derived:

Wafer Sort

Fab cost per gross die (Processed wafer cost/Number of dice on wafer)	= A
Wafer Sort cost per gross die (Tester cost per hour/(Dice on wafer x Wafers tested per hour))	= B
Cost per gross die at Wafer Sort	= A + B
Wafer Sort yield	= C
Therefore, cost per net die at Wafer Sort	= (A + B)/C = D

8. Cost Trends

Assembly	
Cost of die from Wafer Sort	= D
Assembling cost per Wafer Sort die	= E
Assembly yield	= F
Therefore, cost per Wafer Sort die	= D + E
And cost per assembled die	= (D + E)/F = G
Final Test	
Assembled die cost	= G
Test time/die in seconds	= H
Test cost/die (Tester cost per hour/60 x (60/H))	= J
Final test yield	= K
Therefore cost per final tested unit	= (G + J)/K = L
Mark, Pack, and Ship	
At X percent yield	= M
Therefore, total variables cost per net unit	= (L + M)/X = N
Assume overhead	= 110 percent
Therefore, breakeven cost per unit	= 210 percent x N

We have used 110 percent overhead in our calculations, but this could vary depending on the cost structure and accounting practices of the company concerned. The final figure derived in each model is a breakeven cost that makes no allowance for profit, or for transporting and warehousing the finished goods.

The six models shown illustrate the wide range of costs of semiconductor manufacture. The smallest device modeled is a TTL SSI gate chip of a type that has been available for more than 12 years, and the models range to a 256K RAM, which will not be generally available to the merchant market until late 1983.

8. Cost Trends

Assumptions Used in the Cost Models

In preparing the cost models presented on the following pages, we established for each a number of assumptions regarding such factors as wafer size, die size, and package type. These assumptions are representative of industry practice in the early 1980s unless otherwise noted. Cost assumptions are based on the past experience and expected performance of high-volume, efficient semiconductor manufacturers.

8. Cost Trends

TTL SSI Cost Model

Table 8-1 shows a cost model for a TTL SSI part. Costs were based on the experience representative of a facility producing 10 million TTL parts per month. The production process used is 5-micron geometry Schottky. The assumptions used in preparing the model are:

- Wafer size - 3-inch
- Fabricated wafer cost - $78
- Die size - 35 x 35 mils
- Test cost - $26 per hour
- Test times - 2 wafers per hour, and 2 packaged devices per second
- Package type - 16-pin plastic DIP

8. Cost Trends

Table 8-1

TTL SSI COST MODEL

	Cost
Wafer Sort:	
Fab cost per gross die ($78.00/5,250) =	$0.0149
Wafer Sort cost per gross die ($26.00/(5,250 x 2)) =	$0.0025
Cost per gross die at Wafer Sort =	$0.0174
Wafer Sort yield = 70%	
Therefore, cost per net die at Wafer Sort =	$0.0248
Assembly:	
Cost of die from Wafer Sort =	$0.0248
Assembly cost per Wafer Sort die =	$0.0380
Assembly yield = 93%	
Therefore, cost per Wafer-Sort die =	$0.0628
and cost per assembled die =	$0.0675
Final Test:	
Assembled die cost =	$0.0675
Test time/die = 0.5 seconds	
Test cost/die ($26.00/(60 x 120)) =	$0.0036
Final test yield = 90%	
Therefore, cost per final tested unit =	$0.0790
Mark, Pack, and Ship	
At 99.9% yield =	$0.0160
Therefore, Total Variables Cost Per Net Unit =	$0.0951
Assume overhead = 110%	
Therefore, breakeven cost per unit =	$0.1997

Source: DATAQUEST, Inc.
April 1982

8. Cost Trends

TTL MSI Cost Model

The TTL MSI device modeled in Table 8-2 is a 5-micron geometry Schottky TTL part. The following assumptions are used:

- Wafer size - 3-inch
- Fabricated wafer cost - $78
- Die size - 40 x 80 mils
- Test cost - $42 per hour
- Test times - 3 wafers per hour, and 1 packaged device per second
- Package type - 24-pin plastic DIP

Table 8-2

TTL MSI COST MODEL

	Cost
Wafer Sort:	
Fab cost per gross die ($78.00/1,940) =	$0.0402
Wafer Sort cost per gross die ($42.00/(1,940 x 3)) =	$0.0072
Cost per gross die at Wafer Sort =	$0.0474
Wafer Sort yield = 65%	
Therefore, cost per net die at Wafer Sort =	$0.0729
Assembly:	
Cost of die from Wafer Sort =	$0.0729
Assembly cost per Wafer Sort die =	$0.0650
Assembly yield = 90%	
Therefore, cost per Wafer-Sort die =	$0.1379
and cost per assembled die =	$0.1532
Final Test:	
Assembled die cost =	$0.1532
Test time/die = 1 second	
Test cost/die ($42.00/(60 x 60)) =	$0.0117
Final test yield = 85%	
Therefore, cost per final tested unit =	$0.1940
Mark, Pack, and Ship	
At 99% yield =	$0.0250
Therefore, Total Variables Cost Per Net Unit =	$0.2212
Assume overhead = 110%	
Therefore, breakeven cost per unit =	$0.4645

Source: DATAQUEST, Inc.
April 1982

8. Cost Trends

Operational Amplifier Cost Model

The Table 8-3 cost model is representative of a high-volume, medium-performance bipolar operational amplifier. The model is based on the following assumptions:

- Wafer size - 3-inch
- Fabricated wafer cost - $56
- Die size - 44 x 44 mils
- Test cost - $56 per hour
- Test times - 1.5 wafers per hour, and 1 packaged device per 3 seconds
- Package type - 8-pin minidip

8. Cost Trends

Table 8-3

OPERATIONAL AMPLIFIER COST MODEL

	Cost
Wafer Sort:	
Fab cost per gross die ($130.00/6,400) =	$0.0203
Wafer Sort cost per gross die ($56.00/6,400 x1.5) =	$0.0058
Cost per gross die at Wafer Sort =	$0.0261
Wafer Sort yield = 60%	
Therefore, cost per net die at Wafer Sort =	$0.0436
Assembly:	
Cost of die from Wafer Sort =	$0.0436
Assembly cost per Wafer Sort die =	$0.0450
Assembly yield = 92%	
Therefore, cost per Wafer-Sort die =	$0.0886
and cost per assembled die =	$0.0963
Final Test:	
Assembled die cost =	$0.0963
Test time/die = 3 seconds	
Test cost/die ($56.00/(60 x 20)) =	$0.0467
Final test yield = 85%	
Therefore, cost per final tested unit =	$0.1682
Mark, Pack, and Ship	
At 99% yield	$0.0180
Therefore, Total Variables Cost Per Net Unit =	$0.1881
Assume overhead = 110%	
Therefore, breakeven cost per unit =	$0.3950

Source: DATAQUEST, Inc.
April 1982

8. Cost Trends

16-Bit Microprocessor Cost Model

The cost model shown in Table 8-4 represents an NMOS device produced using eight mask steps and 3-micron geometry. Yield assumptions shown are achievable in 1982 by larger volume producers. Assumptions for the model are:

- Wafer size - 4-inch
- Fabricated wafer cost - $85
- Die size - 225 x 225 mils
- Test cost - $125 per hour
- Test times - 3 wafers per hour, and 1 packaged device per minute
- Package type - CERDIP

8. Cost Trends

Table 8-4

16-BIT MICROPROCESSOR COST MODEL

	Cost
Wafer Sort:	
Fab cost per gross die ($85.00/198) =	$0.4293
Wafer Sort cost per gross die ($125.00/(198 x 3)) =	$0.2104
Cost per gross die at Wafer Sort =	$0.6397
Wafer Sort yield = 20%	
Therefore, cost per net die at Wafer Sort =	$3.1985
Assembly:	
Cost of die from Wafer Sort =	$3.1985
Assembly cost per Wafer Sort die =	$1.8500
Assembly yield = 80%	
Therefore, cost per Wafer-Sort die =	$5.0485
and cost per assembled die =	$6.3106
Final Test:	
Assembled die cost =	$6.3106
Test time/die = 60 seconds	
Test cost/die ($125.00/(60 x 1)) =	$2.0833
Final test yield = 80%	
Therefore, cost per final tested unit =	$10.4924
Mark, Pack, and Ship	
At 99% yield =	$ 0.1100
Therefore, Total Variables Cost Per Net Unit =	$10.7095
Assume overhead = 110%	
Therefore, breakeven cost per unit =	$22.4899

Source: DATAQUEST, Inc.
April 1982

8. Cost Trends

64K CMOS EPROM Cost Model

The device described in Table 8-5 is made using 12 mask steps with 2.5-micron minimum geometry in a projection-aligned process. The model is based on a 1983 production volume of 25,000 units per month. Assumptions for this model are:

- Wafer size - 4-inch
- Fabricated wafer cost - $130
- Die size - 170 x 200 mils
- Test cost - $85 per hour
- Test times - 3 wafers per hour, and 1 packaged device per 18 seconds
- Burn-in cost - $0.095 per device
- Pre- and post-burn testing
- Package type - 28-pin CERDIP (quartz window)

8. Cost Trends

Table 8-5

64K CMOS EPROM COST MODEL
(Prototype Production Volume)

	Cost
Wafer Sort:	
Fab cost per gross die ($130.00/340)	$0.3824
Wafer Sort cost per gross die ($85.00/(340 x 3))	$0.0833
Cost per gross die at Wafer Sort	$0.4657
Wafer Sort yield = 15%	
Therefore, cost per net die at Wafer Sort	$3.1049
Assembly:	
Cost of die from Wafer Sort	$3.1049
Assembly cost per Wafer Sort die	$1.3600
Assembly yield = 80%	
Therefore, cost per Wafer Sort die	$4.4649
and cost per assembled die	$5.5811
First Test:	
Assembled die cost	$5.5811
Test time/die = 18 seconds	
Test cost/die ($85/200)	$0.4250
Final test yield = 85%	
Therefore, cost per first-tested unit =	$7.0660
Final Test:	
Cost per first-tested unit =	$7.0660
Burn-in cost =	$0.0950
Final test time = 18 seconds	$0.4250
Burn-in and final test yield = 90%	
Therefore, cost per final tested unit =	$8.4289
Mark, Pack, and Ship	
At 99% yield, operations cost =	$0.0600
Therefore, variables cost per net unit =	$8.5746
Assume overhead = 110%	
Therefore, breakeven cost per unit =	$18.0068

Source: DATAQUEST, Inc.
April 1982

8. Cost Trends

256K Dynamic RAM Cost Model

The 256K dynamic RAM is a leading-edge technology device that will not be available before mid-1982. The model was prepared assuming a 1985-1986 production volume of one million units per month. The device is made using NMOS technology, with an 8-layer process and 2.5-micron minimum geometry. The assumptions for Table 8-6 are:

- Wafer size - 5-inch
- Fabricated wafer cost - $110
- Die size - 182 x 500 mils.
- Test cost - $125 per hour
- Test times - 3 wafers per hour, and 2 packaged devices per minute
- Package type - 16-pin ceramic chip carrier

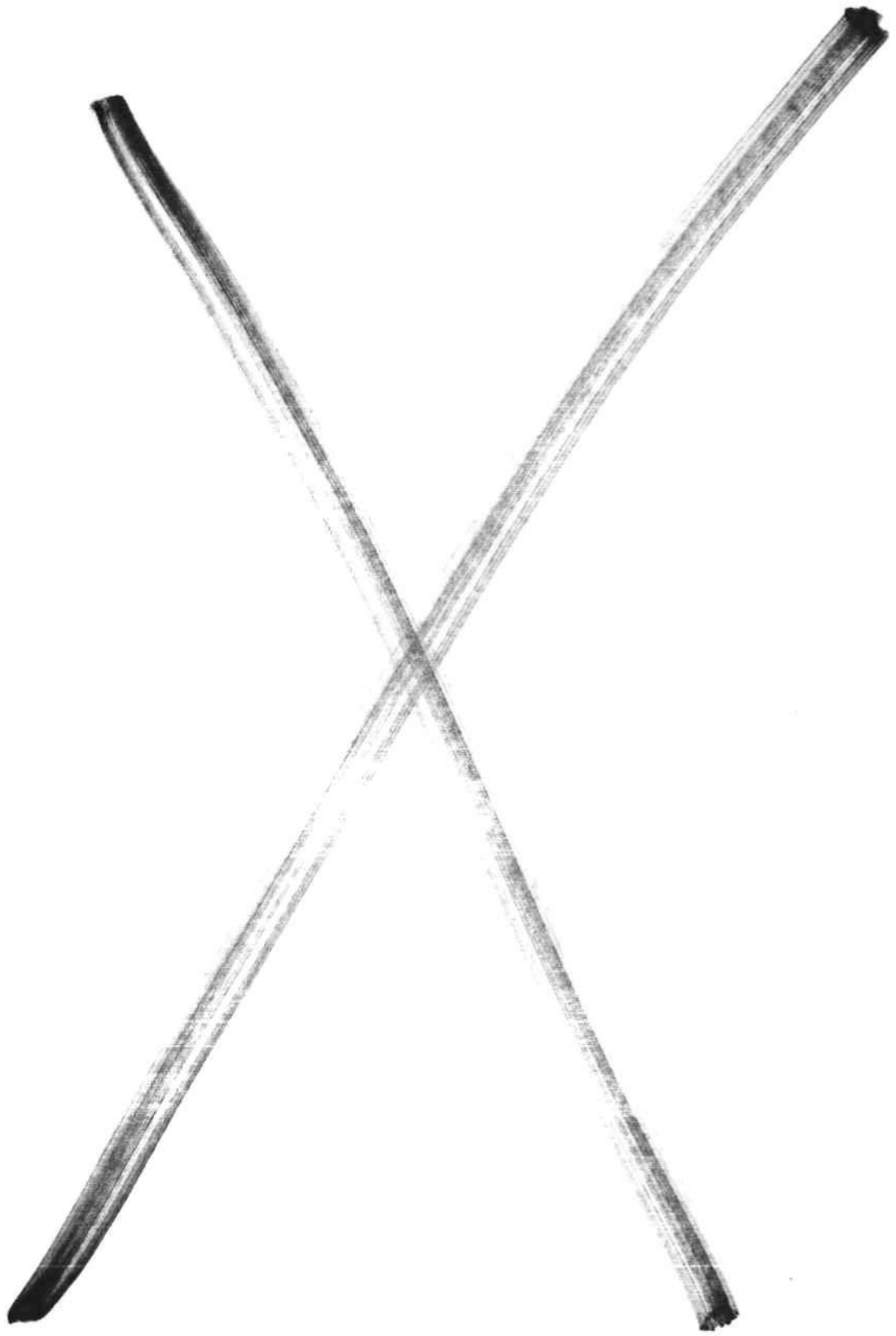
8. Cost Trends

Table 8-6

256K RAM COST MODEL

Wafer Sort:	Cost
Fab cost per gross die ($110.00/158) =	$0.6962
Wafer Sort cost per gross die ($125.00/(158 x 3)) =	$0.2637
Cost per gross die at Wafer Sort =	$0.9599
Wafer Sort yield = 24%	
Therefore, cost per net die at Wafer Sort =	$3.9996
Assembly:	
Cost of die from Wafer Sort =	$3.9996
Assembly cost per Wafer Sort die =	$0.3600
Assembly yield = 90%	
Therefore, cost per Wafer Sort die =	$4.3596
and cost per assembled die =	$4.8440
Final Test:	
Assembled die cost =	$4.8440
Test time/die = 30 seconds	
Test cost/die ($125.00/(60 x 2)) =	$1.0417
Final test yield = 80%	
Therefore, cost per final tested unit =	$7.3571
Mark, Pack, and Ship	
At 100% yield =	$0.0400
Therefore, Total Variables Cost Per Net Unit =	$7.3971
Assume overhead = 110%	
Therefore, breakeven cost per unit =	$15.53

Source: DATAQUEST, Inc.
April 1982



Nielsen Dataquest

INQUIRY RESPONSE

DATE: 12/8/83

TO: Rollie Griep/Honeywell

FROM: Stan Bruederle/SUIS

This information has been compiled in response to your inquiry of Dec. 1983

Please file in Vol.I, Sec. 9 for future reference.

Subject: Price Ranges

We estimate the following contract and spot price ranges for the TTL products that you requested. Contract price ranges are estimated for contracts that have been recently negotiated. The changes are consistent with our price trend section of our notebooks. For reference purposes I have also included price data that we presented to you last year in the third quarter. Contract prices for LS have increased by over 40 percent in that time frame while spot prices have increased by 80 to 150 percent.

4th. QTR 1983 PRICES
(cents)

Type	Contract Price	Spot Price
LS00	19-22	25
LS74	25-27	35
LS138	32-36	42
LS161	32-37	45
LS175	30-34	40
LS244	60-70	85
7407	50-55	Dlrs 3.00-5.00
7417	50-55	Dlrs 2.00
7438	25-30	35
74154	55-60	70
500	20-25	30
874	30-35	45
5373	98-108	120
5138	45-50	60
H04	35-40	50
H51	35-40	50

This information is based on our estimates, a survey of the important suppliers of TTL products, and companies buying TTL products. Different companies said they thought prices were at different points in the range for different device types, but no one appeared to be consistently higher or lower priced.

3rd. QTR 1982 PRICES
(cents)

Type	Contract Price	Spot Price
LS00/03/05/08/11	13-14	10-12
LS109/113	15-18	18-19
LS161/163	29-32	low 30's
LS164/165/166	40-44	-
LS174	25-27	25-30
LS240/241	45-50	45-50

cc: Harry Tyrpa

:tg

Nielsen Dataquest

INQUIRY RESPONSE

DATE: 12/13/83

TO: Alessandra Guarracino/Italtel SIT

FROM: Jean Page/SUIS

This information has been compiled in response to your inquiry of Dec.'83

Please file in Vol. 1, Sec.9 for future reference.

Re: Your tlx regarding Bipolar Memory 93L422 256x4

This part has been available for some time and is in the mature phase of its life-cycle. The part is offered by AMD, Fairchild, and Motorola.

Many 1K Bipolar RAMs are being replaced by higher density bipolar devices or by CMOS static RAM. However, the 93L422 is a fast part and is expected to remain popular for products with a small memory requirement.

Prices are expected to remain flat throughout 1984 and lead times are estimated at 16-18 weeks throughout the year.

:tg

Nielsen Dataquest

INQUIRY RESPONSE

DATE: September 20, 1983

TO: Ron Bond/Apple Computer, Inc.

FROM: Stan Bruederle/Semiconductor User Information

This information has been compiled in response to your inquiry of ~~9/7/83~~

Please file in ~~Vol. I, Sec. 9~~ for future reference.

Subject: Price Trends and Availability of 64K and 256K D RAMs, 68K Microprocessors, and PALs.

64K and 256K D RAMs

The attached newsletter is a recent status of the 64K dynamic RAM. There are 18 companies producing or planning to produce 64K dynamic RAMs. Shipments in 1983 will be more than three times 1982 shipments, as shown by Table 1.

TABLE 1

ESTIMATED WORLDWIDE 64K DYNAMIC RAM PRODUCTION

1980	1981	1982	1983	1984	1985	1986
0.4	12.6	104.0	310	620	850	1,000

Source: DATAQUEST
May 1983

In the last quarter we have revised our 1983 shipment figures up to 340 million units. The product is still on allocation. We expect it to remain on allocation through mid 1984, at least. One variable that is hard to predict is the effect of company failures that are occuring periodically. To-date they have simply made some product available to help reduce the effects of present shortages. Average prices for 64K devices have stabilized at around $4.00 in the third quarter. We have heard of quotes of over $4.50 for 150 to 200 nanosecond devices during the last two months. We expect prices to increase by up to 5 percent between now and the second quarter of 1984. Then prices should start on their downward trend again. Five year ASP projections are shown on Table 2.

TABLE 2

64K DYANAMIC RAM ASP

1982	1983	1984	1985	1986
$5.50	$4.10	$3.35	$2.50	$2.35

We monitor 64K shipments by speed selection each year. Table 3 shows the breakdown of worldwide shipments for each access time range.

TABLE 3

SHIPMENT DISTRIBUTION BY ACCESS TIME

	≤100 ns	≤120 ns	≤150 ns	≤200 ns
1982	0.2%	2.3%	44.9%	52.7%
1983	3.2%	10.0%	56.0%	30..8%

Manufacturers have indicated to us that speed distributions in manufacturing have moved toward higher performance during the last two years as manufacturers have shrunk die and designed to tighter process rules. Production distribution in each speed selection group is somewhat greater than customer demands. We estimate the price relationships between speed selections to be as shown by Table 4. These factors relate to the 1983 A.S.P. from Table 2.

TABLE 4

RELATIVE PRICES OF 64K ACCESS TIME SELECTIONS

≤100 ns	≤120 ns	≤150 ns	≤200 ns
1.6	1.2	1.0	.85

We project shipments of 256K dynamic RAMs to be as shown by Table 5.

TABLE 5

256K DYNAMIC RAM SHIPMENTS
(units, thousands)

1982	1983	1984	1985	1986
20-30	700	12.5K	80K	360K

Prices of 256K D RAMs are presently averaging $50.00. We expect prices to be $20.00 to $22.00 by the second half of 1984 as production capacity increases. Table 6 projects average prices for 256K D RAMs.

TABLE 6

256K DYNAMIC RAM AVERAGE PRICES ($)

1982	1983	1984	1985	1986
$100.00	$ 50.00	$ 25.00	$ 12.50	$ 7.00

At this early stage of the product's life we have no data on speed distributions. We expect the same supply-demand situation to occur for 256K devices in 1985-1986 as occured with 64K and 16K devices. Demand will exceed supply.

68000 Microprocessor

We have made the shipment estimates of Table 7 for the suppliers of 68000 microprocessors in 1982 and the first half of 1983.

TABLE 7

68000 MICROPROCESSOR SHIPMENTS
(units, thousands)

	1Q82	2Q82	3Q82	4Q82	1982	1Q83	2Q83
Motorola	30	35	40	55	160	75	90
Hitachi	10	12	20	26	68	40	45
Mostec	1	2	2	4	9	6	7
Signetics	-	-	-	-	-	5	7
Rockwell	-	-	-	-	-	1	1
EFCIS	-	-	-	-	-	-	-
Total	41	49	62	85	237	127	150

There has been a significant increase in demand for 68000's in the first half of 1983. We believe book-bill ratios have exceeded 3:1 for several months. This is causing temporary shortages of product. However, we believe there is sufficient capacity to meet the increased demand for the 68000 by the end of 1983. Prices have incresed by 5 percent in the second quarter over first quarter prices. We expect prices to increase another 5 percent by the end of the year, then decrease again in 1983 as competition increases. As suppliers bring in additional capacity, you should see very competitive pricing between Motorola and Hitachi as they battle for leadership. Signetics and Mostek will also become competitive as production yields improve and they become recognized suppliers. At the present time we don't have specific data on price related to speed selection. We also do not publish A.S.P. data for specific types where only one or two suppliers dominate.

PALs

We estimate that PAL prices will decline by 20 percent from 1982 to 1983. PAL revenues will grow by between 2.1 and 2.3 time 1982 revenues of 30 million to $63 to $70 million. Unit shipments are expected to grow 2.5 to 2.7 times. There has been adequate capacity to support this rapidly growing demand during 1982. However,

demand for PROMs has grown rapidly since the beginning of 1982. We believe that growing PROM production along with doubling of PAL production will cause shortages to appear around the middle of 1984. Industry sources expect PAL prices to remain stable next year. We feel that this is a good assumption.

MMI is pricing all speed-power variations of PALs the same. Unlike MOS devices where speed variations are selected by testing from a single design, PAL speed selections are different metalization patterns. With MOS, speed selections fit a yield distribution. For PALs, all speed selections have the same yield.

If you want to discuss any of these areas in more detail, please call and tell me what you need.

cc: John Randall, Marketing/DQ

Apple
W.L. Stalcup, Director of Materials
J. Devlin

Attachment

:tg

Nielsen Dataquest

INQUIRY RESPONSE

This information has been compiled in response to your inquiry of September

Please file in Vol.I, Section 9 for future reference.

DATE: Sept. 9

TO: Haaken Sammelin/Swedish Telecommunications

FROM: Stan Bruederle/SUIS Dataquest

SUBJECT: CMOS 16K Static RAMs

CMOS STATIC RAM CONSUMPTION

	1982	1983	1984	1985	1986
Worldwide	20	45	100	110	60
Europe	3.6	9.5	24	30	19
Europe percent	18	21	24	27	32

We have recently seen dramatic growth caused by use of CMOS RAMs for portable personal computers. Europe share of worldwide comsumption is a higher share of the total at 21 percent of unit shipments for memory products in general. We expect this share to continue to increase.

European prices are lower than the worldwide average. We expect the worldwide ASP to be 4.00 US dollars for 1983 while the Europe ASP is expected to be 3.50 US dollars. The following table shows projected ASPs for Europe and worldwide consumption for 1982 through 1986.

CMOS STATIC RAM ASP

	1982	1983	1984	1985	1986
Worldwide	6.25	4.00	3.35	3.25	3.00
Europe	5.50	3.50	3.00	2.75	2.30

Lead times have been increasing all year. By the fourth quarter we expect them to reach 10 to 12 weeks. They should stay at 10 to 12 weeks in 1984. Lead times should generally be the same in the U.S. and Europe.

Table 9-4c in Volume I, Section 9 of the notebooks, provides you with quarter by quarter price and lead time trend information for 1983. The same information for 1984 will be published in October.

cc: Edward Mier/DQ UK

:tg

8/8/83

August 1983

Joe Davis/Hewlett-Packard

Section 9

Stan Bruederle

Subject: Discrete Semiconductor Price Trend Forecast

General Overview

We expect 1983 discrete semiconductor shipments to be 4.7 percent higher than 1982. However, second quarter shipments grew 15 percent from the first quarter. We expect strong quarter to quarter growth to continue into 1984. The resulting strong growth will result in higher prices for most discrete products. Lead times will also increase during the period although not as seriously as they have in IC.s. The resulting prices trends are listed below.

Price Trend Forecast

Product Group	Price Trends (1Q84 to 1Q85)
Transistors	
Bipolar small signal	incr. 5%
Bipolar power	incr. 10-15%
FET power	decr. 20-25%
FET small signal	incr. 5-10%
Diodes	
Microwaves	N/A
Switching	incr. 17-20%
Zener	incr. 0-5%
Rectifier	incr. 5-10%
Multiple	N/A
Thyristors	incr. 5-10%
Optoelectronics	
Displays	incr. 0-5%
Devices	incr. 5-10%
Isolators	incr. 10-15%

These projections have been developed from our analysis of the trends for the next year for discrete semiconductors in general along with a survey of the expectations of key manufacturers in each product category. Based on the strength of the 1983 recovery, these increases will appear in whichever quarter contracts are negotiated. Since most companies negotiate contracts in the second half of the year we expect the effect on prices to appear in the first half of 1984.

Nielsen Dataquest

INQUIRY RESPONSE

DATE: 21 June 1983

TO: Francis Lefebvre/CIT Alcatel

FROM: Stan Bruederle/Manager SUIS

This information has been compiled in response to your inquiry of June 1983

Please file in Section 9 for future reference.

Subject: Prices for Selected Semiconductor Products in the U.S.

During our meeting in May you asked for prices of selected device types in the U.S. I have listed below selected 74LS TTL types and price ranges for volume purchases. If you wish information on other devices, please let me know. These prices have increased from 5 percent to 10 percent in the last six months. We expect prices in the U.S. to increase by 5 to 10 percent between now and the end of the year the U.S.

Gates:	16-18 cents (74LS00)
Dual flip-flops:	24-26 cents (74LS74)
Octal drivers/latches:	44-46 cents (74LS244)
Counters:	27-30 cents (74LS160)

cc: CIT Alcatel:
Mr. Jean-Marc Pornet
Mr. Martine Hoet
DATAQUEST:
Bud Mills

SAB:pg

9. Price Trends

This section of the notebook describes the factors that affect semiconductor prices, and provides data for establishing short- and long-term price trends for specific products.

OVERVIEW

Average selling prices of semiconductors have remained at about $0.30 for the past 10 years. Beneath this apparently stable and consistent figure lies the most complex and dynamic price structure of any electronic product. Over any given period of time, average rates of price decrease will vary from 0 to 5 percent per year for mature commodity products, to 60 to 65 percent per year for new, high-growth LSI/VLSI products. Table 9-1 shows examples from the past 10 years.

Table 9-1

TEN-YEAR SEMICONDUCTOR FAMILY PRICE TRENDS

Family	Time Period	Price Change	Change Per Year
Small-signal transistor	1972-1982	(55%)	(7.7%)
Small-signal diode	1972-1982	(43%)	(5.4%)
LS TTL SSI	1974-1982	(41%)	(6.4%)
LS TTL MSI	1974-1982	(55%)	(9.4%)
Operational amplifiers	1973-1982	(44%)	(6.2%)
8-bit MPU	1975-1982	(90%)	(25.0%)
8-bit MCU	1978-1982	(67%)	(19.7%)
16-bit MPU	1980-1982	(50%)	(29.2%)
16K D RAM	1977-1981	(83%)	(30.1%)
64K D RAM	1980-1982	(84%)	(60.1%)
16K EEPROM	1982-1983	(67%)	(67.0%)

Source: DATAQUEST
June 1983

9. Price Trends

To stay on top of pricing trends, semiconductor users must monitor the following three factors that cause semiconductor prices to change:

- Business conditions - Short-term business conditions that affect supply/demand relationships and increase or decrease the rate of price change
- Life cycle - The product's position in its life cycle, which determines the rate and direction of longer-term price trends
- Obsolescence - The introduction of newer, more cost-effective products that replace existing products by offering lower price per functional unit (gate, bit of memory, or amplifier)

BUSINESS CONDITIONS

Semiconductor users comment that semiconductor pricing often bears no relationship to manufacturing cost. There is a reason for this phenomenon, based upon the unique nature of the semiconductor industry and the financial structure of the participants.

First, there is a high degree of price elasticity for semiconductors. For example, memory prices have historically fallen 30 to 40 percent per year, while unit volume has grown 80 to 90 percent per year. Figures 9-1 and 9-2 graphically demonstrate this unit growth. Dynamic RAM shipments will have increased from 20 million units in 1974 to 500 million units in 1984, while complexity will have increased 64 times in that period.

Second, the industry is a growth industry, with the cyclical characteristics of a raw material business. Although average growth of integrated circuit consumption has been 20 percent per year, the year-to-year growth has varied from -15 percent to as high as +40 percent. As a result, the industry spends most of the time either running at full capacity (or more), or at significantly less than full capacity.

Third, the industry's production capacity is a function of manufacturing yields, which can change by factors of two in a matter of months. In addition, chip yields tend to decrease somewhat at high levels of production (high growth periods), and increase dramatically when production levels are reduced (low growth or decline periods). As a result, direct manufacturing costs can decrease in slow business periods, resulting in higher margin contribution for a given price level. Companies can sell products at lower prices and still make the same margins.

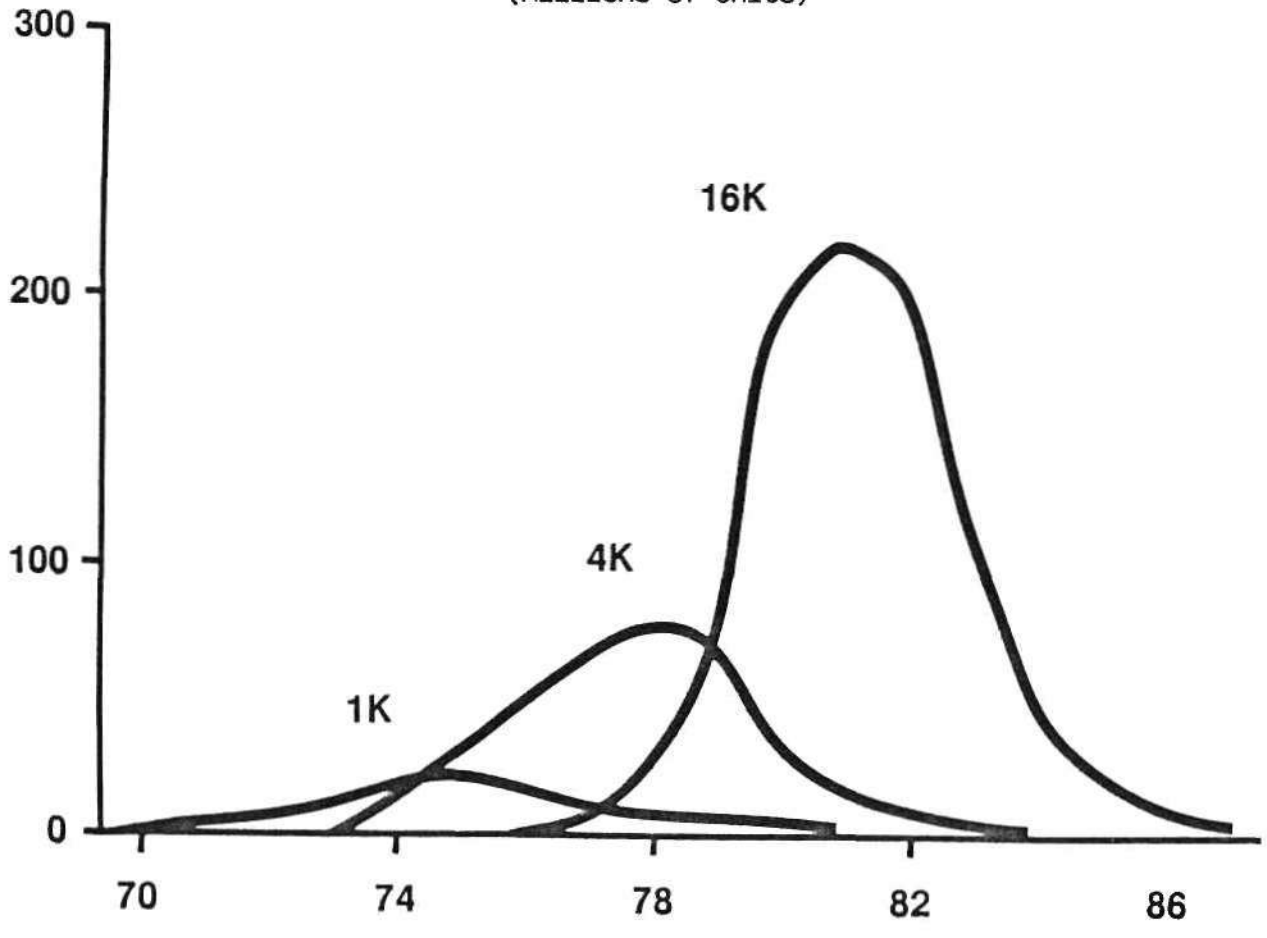
9. Price Trends

Fourth, semiconductor manufacturers have relatively high fixed costs. Fixed manufacturing, selling, and R&D costs of a typical semiconductor company are estimated to average 50 percent of sales. Companies plan for their long-term growth rates and adjust plans downward when business conditions dictate. Fixed costs tend to grow in years of low growth because business downturns are relatively short (1-1/2 to 2 years) compared to the time it takes to construct new facilities. Consequently, companies experience significant declines in profitability when they are unable to maintain their revenue growth rates. Figure 9-3 illustrates the cost-volume-profit curves for a typical semiconductor company with a high mix of commodity products over a period of two years when planned shipment growth is 33 percent. Figure 9-4 shows the same curves for the second year, when sales are the same as the prior year's instead of growing. Although the variable product cost has dropped slightly, from $0.40 to $0.36, fixed costs have increased slightly, from $150 million to $165 million. At the same time, prices have dropped 20 percent because of increased competition among all manufacturers. Most manufacturers expect to increase shipments at the 33 percent projected industry growth rate. As a result of this change, this particular company will experience an operating loss of $30 million, versus a $30 million profit at the same revenue level during the previous year.

9. Price Trends

Figure 9-1

WORLDWIDE DYNAMIC MOS RAM SHIPMENTS
(Millions of Units)

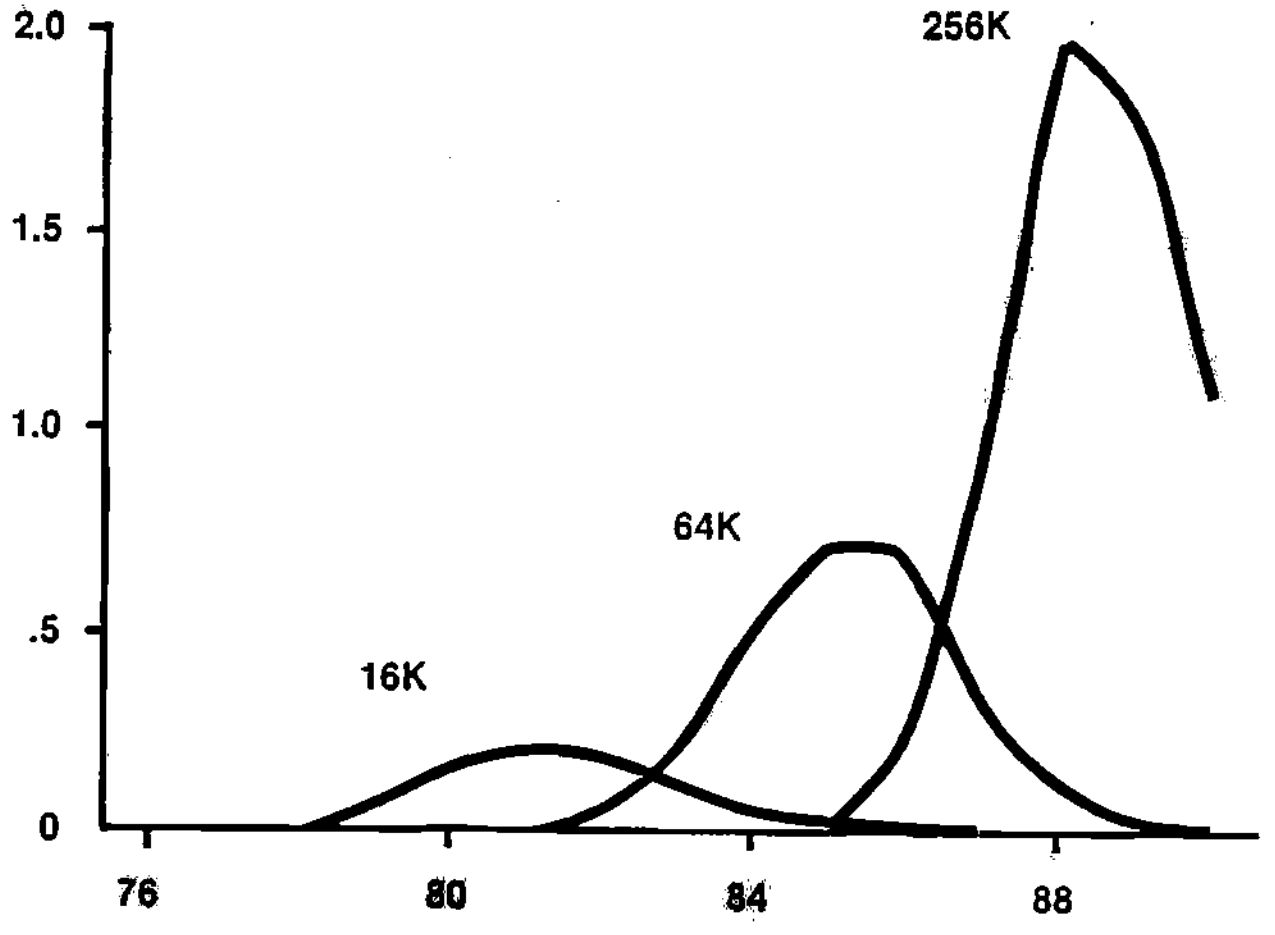


Source: DATAQUEST
July 1983

9. Price Trends

Figure 9-2

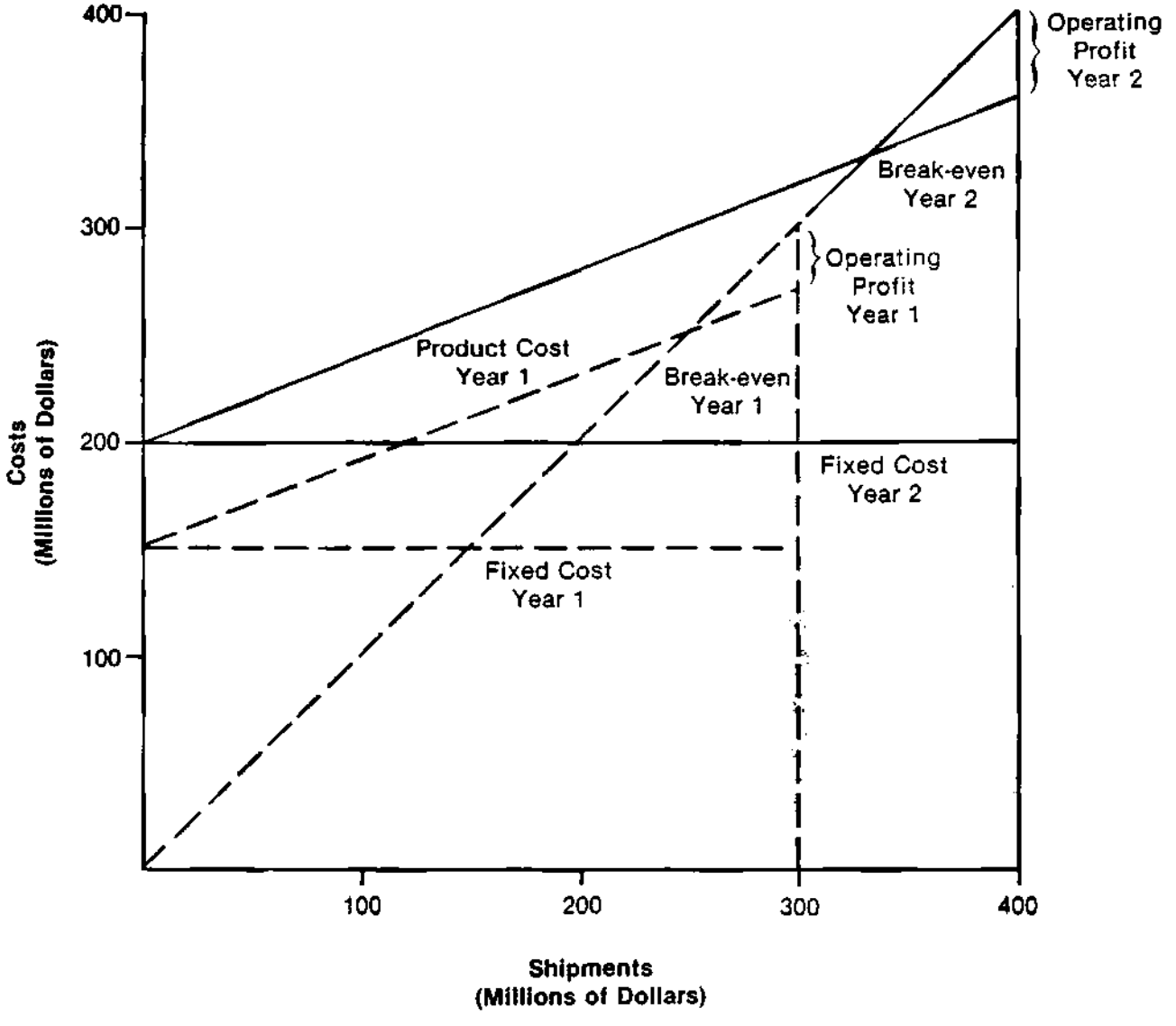
WORLDWIDE DYNAMIC MOS RAM SHIPMENTS
(Billions of Units)



Source: DATAQUEST
July 1983

Figure 9-3

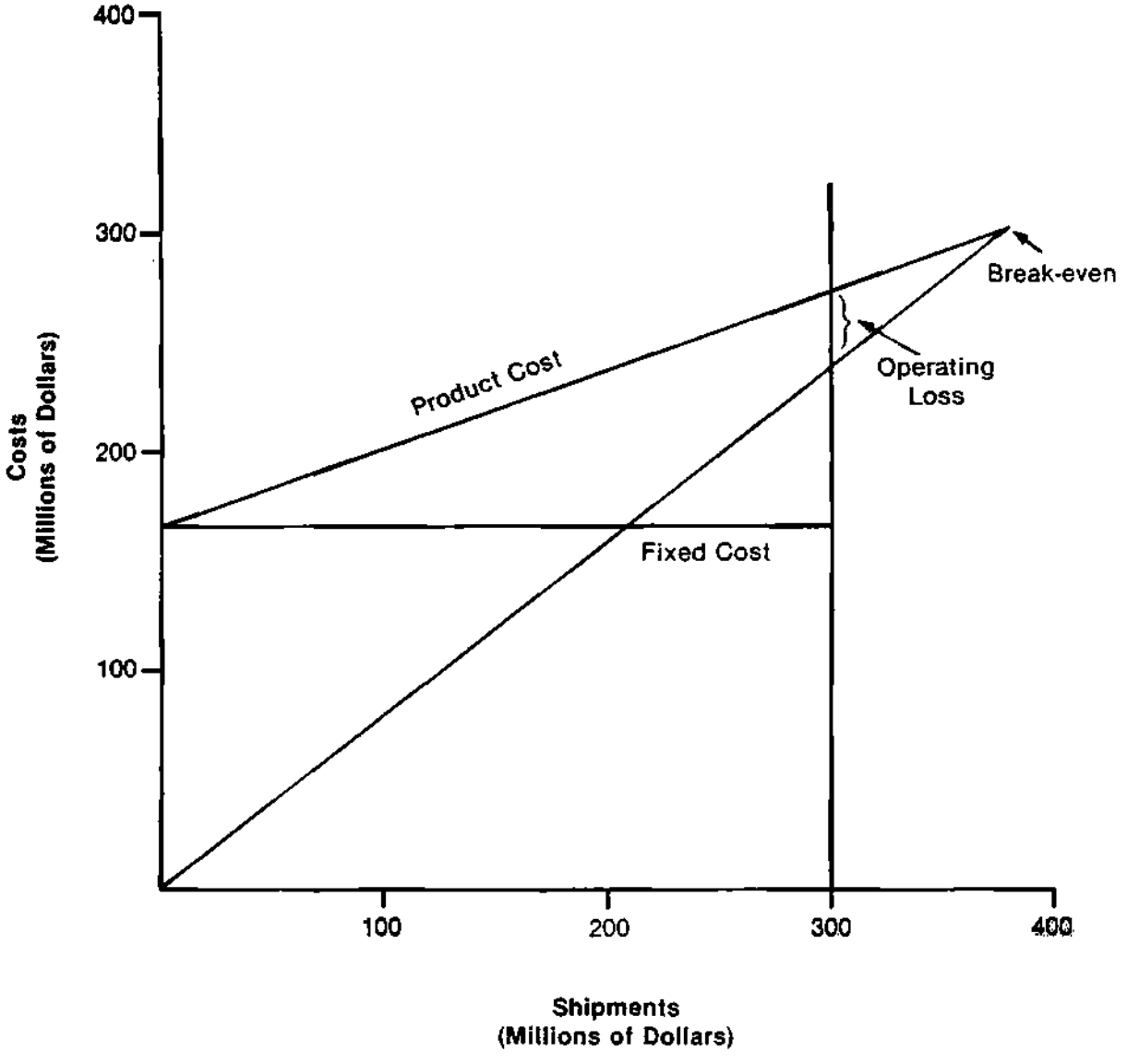
PROFIT-VOLUME-COST MODEL FOR A
HYPOTHETICAL SEMICONDUCTOR COMPANY



Source: DATAQUEST
July 1983

Figure 9-4

PROFIT-VOLUME-COST MODEL FOR A
HYPOTHETICAL SEMICONDUCTOR COMPANY



Source: DATAQUEST
July 1983

9. Price Trends

During both high- and low-growth periods, companies try to enhance their profit margins by improving their product mix (the ratio of high-margin products to low-margin products). The best example of the operation of this strategy is in the area of commodity logic products. As shown in Table 9-2, the variable cost of TTL logic can range from $0.095 for an SSI part to $0.15 for an MSI part, while the prices for these parts range from $0.15 for the SSI part to $0.45 for the MSI part. This means that the variable margin as a percentage of cost ranges from 58 percent at the low end to 200 percent at the high end. Similarly, the contribution margin as a percentage of price ranges from 36.7 percent at the low end to 66.7 percent at the high end. Obviously it is advantageous to the manufacturers to sell more high-end than low-end devices.

Table 9-2

COST COMPARISON OF TTL SSI AND MSI
(Cents)

	TTL SSI	TTL MSI
Variable Cost (cents)	9.5	15.0
Low- and High-End Prices (cents)	15	45
Variable Margin (cents)	5.5	30.0
Variable Margin Percent of Cost	58%	200%
Contribution Margin Percent	36.7%	66.7%

Source: DATAQUEST
June 1983

During slow business periods, companies will quote lower unit prices to customers who have higher MSI/SSI product mixes. Gate prices will appear overly aggressive, but the high complement of MSI will offset the lower margins of the SSI products. On the other hand, companies with low MSI mixes will pay higher prices for gate functions. Manufacturers tend to stock inventories of higher margin products, offering ready availability of those products while extending lead times of SSI types. These types of activities on the part of suppliers create headaches for procurement managers.

9. Price Trends

In past years, a few manufacturers have attempted to offer constant margin pricing to customers in an effort to eliminate the problems caused by the variation in margins under the present pricing structure. This approach has not been accepted when it has been tried. If the industry were to adopt this approach, SSI gates would sell for $0.20, while more expensive MSI functions might drop from $0.45 to $0.35. DATAQUEST does not expect this kind of strategy to be implemented.

Assuming that TTL and CMOS logic price strategies don't change in the foreseeable future, procurement managers should develop long-term strategies to increase their mix of MSI functions and eliminate the use of SSI wherever they can. Education of technical and management people in this area will help shift system design strategies toward elimination of SSI devices from system designs.

FUTURE TRENDS

Average prices of semiconductors will begin to increase during the 1980s, as higher-priced LSI and VLSI become the dominant producers of semiconductor revenues. Prices of LSI and VLSI will continue to decrease rapidly from one generation to the next, while commodity small-scale digital and linear products will remain fairly stable, increasing 10 to 15 percent per year in 1983 through 1984, then declining about the same amount when business slows again. Our estimates of quarter-to-quarter semiconductor shipments, shown in Table 9-3, provide an indication of these short-term price trends during 1983.

Table 9-3

1983 SEMICONDUCTOR SHIPMENT FORECAST
WORLDWIDE SHIPMENTS BY U.S. AND EUROPEAN MANUFACTURERS
(Millions of Dollars)

	Bipolar Logic	% Chg	Bipolar Mem.	% Chg	MOS Mem.	Chg	MOS Logic	% Chg	MOS MPU	% Chg	Linear	% Chg	Discrete	% Chg	TOTAL	% Chg
1982																
1st. Qtr.	368.6	-	91.0	-	389.1	-	213.5	-	179.9	-	368.6	-	648.1	-	2,258.8	-
2nd. Qtr.	403.7	9.5	92.1	1.2	438.0	12.6	235.8	10.4	217.8	21.1	390.0	5.8	661.9	2.1	2,439.3	8.0
3rd. Qtr.	392.2	(2.8)	85.9	(6.7)	460.3	5.1	218.8	(7.2)	217.9	0.0	368.7	(5.5)	584.3	(11.7)	2,328.1	(4.6)
4th. Qtr.	409.6	4.4	84.4	(1.7)	466.5	1.3	221.0	1.0	209.1	(3.9)	376.4	2.1	581.8	(0.4)	2,348.8	0.9
Total 1982	1,574.1	-	353.4	-	1,753.8	-	889.0	-	825.0	-	1,503.7	-	2,476.1	-	9,375.1	-
1983																
1st. Qtr.	395.0	(3.6)	84.0	0.0	423.6	(9.2)	235.0	6.3	210.0	0.0	375.0	0.0	617.0	6.1	2,339.6	(0.4)
2nd. Qtr.	454.3	15.0	96.6	15.0	487.1	15.0	258.5	10.0	241.5	15.0	435.0	12.0	648.0	5.0	2,621.0	12.0
3rd. Qtr.	463.3	2.0	101.4	5.0	511.1	5.0	266.3	3.0	258.4	7.0	450.0	3.6	648.0	0.0	2,698.9	3.0
4th. Qtr.	495.8	7.0	116.6	10.0	567.6	10.0	284.9	7.0	284.2	10.0	480.0	10.3	680.0	5.0	2,904.1	7.6
Total 1983	1,808.4	14.9	393.6	11.4	1,984.8	13.2	1,044.6	17.5	994.2	20.5	1,740.0	15.7	2,593.0	4.7	10,558.6	12.6

Source: SIA Historical Figures
DATAQUEST Forecast
August 1983

9. Price Trends

LIFE CYCLE

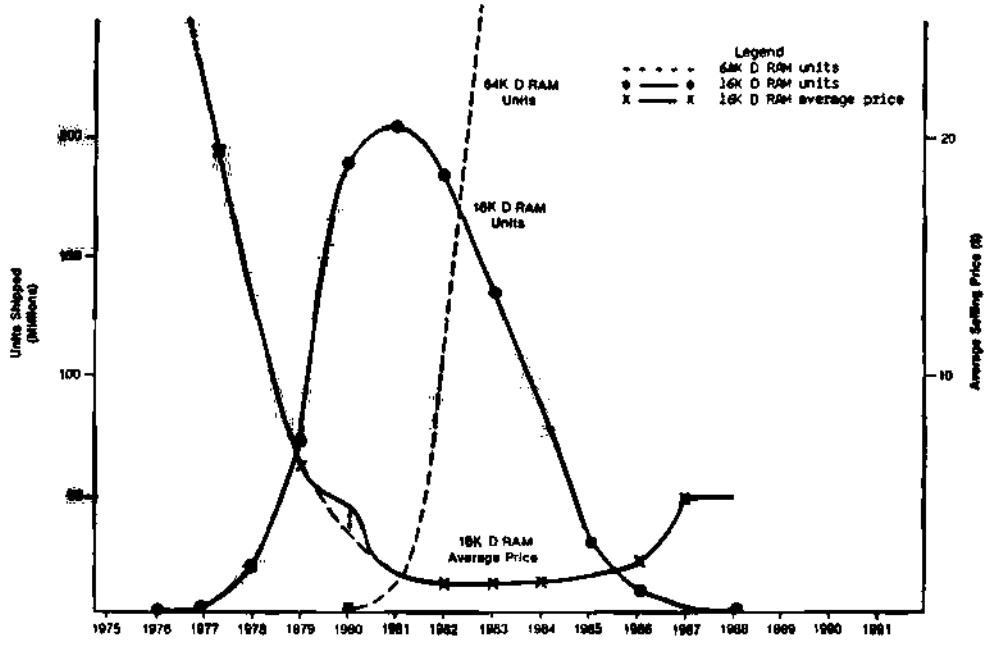
Life Cycle Pricing

Figure 9-5 describes the interaction and effects of the business conditions, life cycle, and obsolescence factors in terms of a product's life cycle. The life cycle of the 16K dynamic RAM is representative of most semiconductor products, although compressed into a shorter time frame. The 16K dynamic RAM began volume production in 1977. The average selling price was $22.00 in 1977, declining 45 percent per year in 1978 and 1979, when the average device sold for $6.50. This rapid decrease of prices is typical of the early stages of a new semiconductor product's life. In 1980 business conditions interrupted the normal supply, and the price decline slowed to 30 percent, with an average selling price of $4.65. During 1981 production caught up with demand and the average price declined rapidly (65 percent) to $1.65. In 1981 production volume peaked as the new 64K dynamic RAM began volume production and displaced 16K D RAMs in newly introduced or upgraded systems. In 1982 16K D RAM shipments declined as the 64K D RAM became the new standard memory product. In the maturing phase of its life, 16K D RAM average prices have stabilized and will now slowly begin increasing as they enter the decline stage until they are phased out of production in the late 1980s. Prices will deviate from the trend during the mature and declining phases as unit demand is affected by business conditions. Customers will buy more product when business conditions are good, and cancel obsolete products when business declines. Prices can increase or decrease 20 to 30 percent in these periods. Timing purchases properly can save money for procurement managers. This timing must be balanced against maintaining close relationships with suppliers to assure deliveries during periods of short supply.

9. Price Trends

Figure 9-5

16K D RAM LIFE CYCLE



Source: DATAQUEST
July 1983

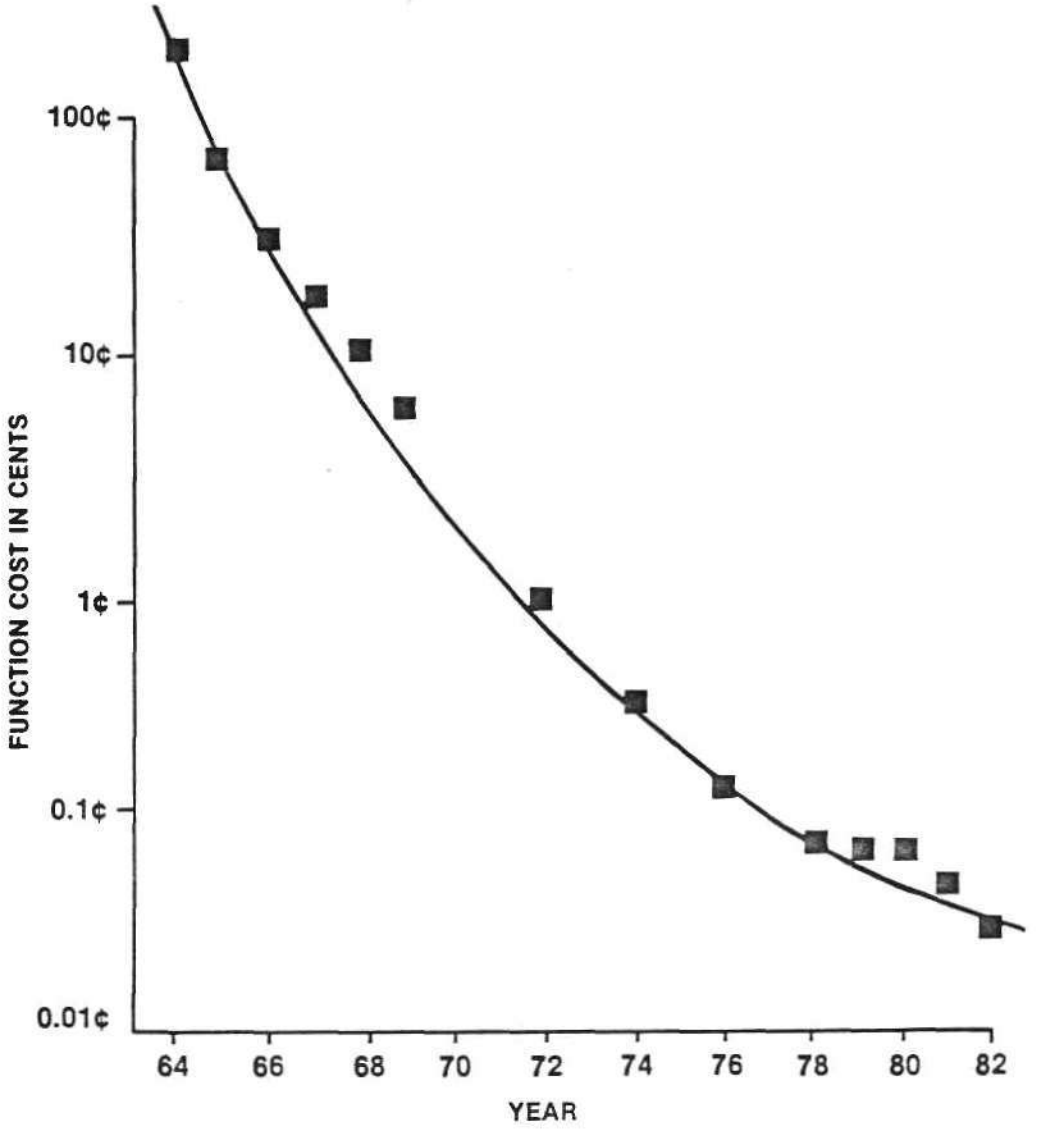
OBSOLESCENCE

Price Per Function

Procurement managers should also be aware of the price per function of integrated circuit products. Continued technological advancement has caused per-function prices to decline at a rate of 40 percent per year as shown by Figure 9-6. Actual price per function and the rate of change are factors that can reduce procurement costs when properly managed. The difference of price per function is most effectively demonstrated by TTL logic products. The price per function for these products varies from as little as one half cent per gate to as much as $0.15 per logic gate. For example, 74LS small-scale integration (SSI) devices are priced from $0.07 to $0.20 in volume. They contain from 1 to 15 gate functions. The price per function is between $0.013 and $0.17. TTL medium scale integration (MSI) devices are priced from $0.20 to $0.70 and contain from 15 to 70 gate functions. The price per function for MSI varies from $0.005 to $0.013 per gate function. Systems that are designed extensively with MSI and LSI devices are the most cost-effective on a per-function basis, even though the price per package for MSI or LSI is greater than for SSI.

Figure 9-6

AVERAGE PRICE PER FUNCTION OF INTEGRATED CIRCUITS



Source: DATAQUEST
July 1983

9. Price Trends

The rapid change of price per function from one generation of product to the next is demonstrated most effectively by MOS dynamic RAM devices and other memories. At less than $2.00 in 1977, a 1K dynamic RAM cost just under 200 millicents per bit. The next generation 4K dynamic RAM cost around $2.00 at its lowest point in 1981, or roughly 50 millicents per bit. The 16K dynamic RAM prices reached $1.40 in 1982, or 8.5 millicents per bit. Per-bit prices of 64K dynamic RAMs became lower than 16K devices in 1982 and are expected to continue to decline further, to less than 4 millicents per bit in 1985. Our projections indicate that 256K and 1-Mbit prices per bit will follow the same trend, reaching 1 millicent per bit by 1990, a 200 times improvement in less than 20 years. To take advantage of these improvements, semiconductor users must know when to convert systems from one generation of product to the next. Tables 9-4a through 9-4k provide information about product replacement trends. Tables 9-5a and 9-5b provide price-per-bit projections for selected MOS memory products to assist users in choosing products for new or upgraded system designs.

PRICE TREND TABLES

These tables provide short-term price and lead time trends, product life cycle information, and product obsolescence information for more than 65 different device groups. The informaton is compiled from surveys of semiconductor manufacturers, users, and distributors.

Tables 9-4a through 9-4k provide specific price and lead time, life cycle, and product replacement information. Tables 9-5a and 9-5b indicate price-per-bit projections for selected MOS memory products to assist in choosing the right memory devices for new and upgraded system designs.

Table 9-4a - SSI/MSI Logic

Orders for industry standard TTL and CMOS products in the first and second quarters of 1983 were two to three times the order rates in the second half of 1982. As a result, lead times have lengthened, prices are increasing, and manufacturers have started allocation programs. The 74F logic family is replacing 74S in high-speed TTL applications. The 74ALS and 74HC CMOS families are competing to ultimately replace 74LS in selected new system designs with lower power and comparable performance.

Table 9-4b - Dynamic Random Access Memories

The 64K D RAM will become the first billion dollar semiconductor device in 1983. Prices will continue to decline, but lead times will lengthen as unit shipments grow to 3 to 3.5 times 1982 shipments.

9. Price Trends

Table 9-4c - Static Random Access Memories

Availability of static RAMs is generally good. CMOS products will be established as general purpose industry standards, while NMOS devices will be designed-in for high performance in the 1984-85 time frame.

Table 9-4d - EPROMs

High-density EPROM prices are declining rapidly as design-ins grow. Products are generally readily available and are expected to remain so. NMOS products are expected to be the industry standard products, while CMOS products are used in military and other low-power applications.

Table 9-4e - ROMs

MOS ROM prices are decreasing, while lead times are stable. A slowdown in the consumer market has offset growth in computer/industrial demand. DATAQUEST believes that CMOS products are becoming the industry standard products, while NMOS parts will be designed-in for high-performance applications.

Table 9-4f - EEPROMS

EEPROM prices will decline rapidly as production volumes increase, yields improve, and competition drives prices down.

Tables 9-4g, h - Bipolar Memories

PROM prices will increase in 1983 and 1984 as overall orders grow two to three times over late 1982 rates. Lead times in 1983 increased in the second quarter and are expected to increase in the third quarter, but should decrease again in the fourth quarter. Adequate capacity is available to support demand once inventories are stabilized. Bipolar RAMs are also readily available. Higher-density 16K ECL RAMs have longer lead times, particularly for larger quantities.

Table 9-4i - Bipolar LSI

All bipolar LSI products are readily available, with prices declining for newer programmable logic and 16-bit microcontroller products.

Table 9-4j - MOS Microprocessors

Lead times for high-end 8-bit microcontrollers (8051, Z8, 6801) will lengthen each quarter. Sixteen-bit microprocessor lead times are also expected to increase throughout 1983 and into 1984.

Table 9-4k - Linear

Lead times are lengthening and prices are increasing for linear ICs. This trend is expected to continue into 1984.

9. Price Trends

Table 9-4a

1983 PRICE AND LEAD TIME TRENDS
SSI/MSI LOGIC

Product/Family		1983 PRICE/LEAD TIME TRENDS				
		1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Year
74OO LOGIC	Price	0%	+20%	+5%	+10%	+39%
	Lead-Time	6-8 wks.	8-16 wks.	24-28 wks.	26-30 wks.	-
74LS LOGIC	Price	0%	+20%	+5%	+10%	+39%
	Lead-Time	6-8 wks.	8-16 wks.	24-28 wks.	26-30 wks.	-
74S LOGIC	Price	0%	+20%	+5%	+10%	+39%
	Lead-Time	6-8 wks.	10-16 wks.	24-28 wks.	26-30 wks.	-
74F LOGIC	Price	-5%	-5%	-5%	-5%	-19%
	Lead-Time	8-10 wks.	10-26 wks.	10-26 wks.	10-26 wks.	-
74ALS LOGIC	Price	-2%	-2%	-8%	-8%	-19%
	Lead-Time	8-10 wks.	12-20 wks.	12-20 wks.	12-20 wks.	-
ECL 10K LOGIC	Price	-2%	-1%	-1%	-1%	-5%
	Lead-Time	6-12 wks.	12-16 wks.	12-16 wks.	12-16 wks.	-
ECL 10KH ECL 100K	Price	-5%	-5%	-10%	-10%	-27%
	Lead-Time	4-16 wks.	6-16 wks.	6-12 wks.	6-10 wks.	-
CMOS 4000 74C	Price	0%	+10%	+5%	+10%	+39%
	Lead-Time	8-10 wks.	8-10 wks.	20-28 wks.	20-28 wks.	-

9. Price Trends

Table 9-4a

1983 PRICE AND LEAD TIME TRENDS
SSI/MSI LOGIC

Product/Family	Comments	Product Life Cycle Trends	Product Replacement Trends
7400 LOGIC	Companies will raise prices as demand decreases.	Product is in decline phase. No new system designs. Five suppliers. Expect three by 1985.	Has been replaced in all new system designs with 74LS.
74LS LOGIC	Companies starting allocation programs.	Product mature. Prices to move up and down with business conditions.	Semicustom CMOS and bipolar LSI being used in many new designs.
74S LOGIC	Prices to rise as manufacturers focus on FAST, 74S demand declines.	Product is mature. Will begin decline in next two years as 74F is widely used in new designs.	74F FAST logic is becoming standard for new high speed system designs.
74F LOGIC	Prices to decline as Motorola, Signetics start production, demand increases.	In design-in stage. Prices to drop rapidly for next two years to 1.1 x 74S price by 1985.	New familly, no replacement yet.
74ALS LOGIC	Price to decline as new designs enter production, volume grows.	In design-in stage. Prices to drop rapidly for next three-four years to equal 74S by 1986/87.	Possible replacement by HCMOS by 1985/1986, in selected applications.
ECL 10K LOGIC	—	Product mature. Prices not expected to decline dramatically.	Higher performance new designs shifting to ECL 10KH or ECL 100K. ECL gate arrays more cost effective.
ECL 10KH ECL 100K	ECL 100K lead times 16-20 wks.for several customer specifications.	10KH in design stage. 100K early production.	—
CMOS 4000 74C	Prices to increase slightly as demand grows.	Product mature. Prices to move up and down with business conditions.	New designs will move to HCMOS during next three to five years.

(Continued)

9. Price Trends

Table 9-4a (Continued)

1983 PRICE AND LEAD TIME TRENDS
SSI/MSI LOGIC

Product/Family		1983 PRICE/LEAD TIME TRENDS				
		1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Year
CMOS 74HC	Price	-5%	-5%	-5%	-5%	-19%
	Lead-Time	8-12 wks.	8-12 wks.	8-12 wks.	8-12 wks.	-
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					

9. Price Trends

Table 9-4a

1983 PRICE AND LEAD TIME TRENDS
SSI/MSI LOGIC

Product/Family	Comments	Product Life Cycle Trends	Product Replacement Trends
CMOS 74HC	Prices declining rapidly as new designs increase. Seven major suppliers.	Design-in stage. Prices to equal 4000 CMOS in next three years.	Some designs will use HCMOS semi-custom products rather than logic.

Source: DATAQUEST
August 1983

9. Price Trends

Table 9-4b

1983 PRICE AND LEAD TIME TRENDS
DYNAMIC RANDOM ACCESS MEMORIES

Product/Family		1983 PRICE/LEAD TIME TRENDS				
		1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Year
4K D RAMs	Price	+2%	+2%	+2%	+2%	+8%
	Lead-Time	14-16 wks.	14-16 wks.	14-16 wks.	14-16 wks.	-
16K D RAMs (3 supply)	Price	0%	0%	+2%	+3%	+5%
	Lead-Time	14-16wks.	14-16 wks.	14-16 wks.	14-16 wks.	-
16K D RAMs single 5v supply	Price	-10%	-15%	-10%	-10%	-34%
	Lead-Time	14-16wks.	14-16 wks.	14-16 wks.	14-16 wks.	-
64K D RAMs	Price	-15%	-5%	-2%	-3%	+23%
	Lead-Time	4-20 wks.	16-20 wks.	16-24 wks.	16-24 wks.	-
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					

Table 9-4b

1983 PRICE AND LEAD TIME TRENDS
DYNAMIC RANDOM ACCESS MEMORIES

Product/Family	Comments	Product Life Cycle Trends	Product Replacement Trends
4K D RAMs	Expect suppliers to offer last time buys in 1983/1984.	Product in decline, approaching phase-out.	Has been replaced by 64K D RAMs.
16K D RAMs (3 supply)	—	Product in decline phase. Expect suppliers to start dropping out in next two years.	Replaced by 64K D RAM in 1981, 1982. No new design ins.
16K D RAMs single 5v supply	—	Product entering decline.	Replaced by 64K D RAM in 1982, 1983 for all but systems with small memory configuration.
64K D RAMs	Price declines to slow as demand approaches production capability.	Growth phase. Unit shipments to increase 2.5 to 3 times between 1982 and 1983.	256K D RAM to replace 64K in new designs in 1985/86.

Source: DATAQUEST
August 1983

Table 9-4c

1983 PRICE AND LEAD TIME TRENDS
STATIC RANDOM ACCESS MEMORIES

Product/Family		1983 PRICE/LEAD TIME TRENDS				
		1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Year
NMOS 1K SRAM	Price	-2%	0%	-2%	0%	-4%
	Lead-Time	5-6 wks.	5-6 wks.	5-6 wks.	5-6 wks.	-
NMOS 4K SRAM slow 1K x 4	Price	0%	0%	0%	0%	0%
	Lead-Time	5-6 wks.	5-6 wks.	5-6 wks.	5-6 wks.	-
NMOS 4K SRAM slow 4K x 4	Price	0%	0%	0%	0%	0%
	Lead-Time	5-6 wks.	5-6 wks.	5-6 wks.	5-6 wks.	-
NMOS 4K SRAM fast 1K x 4	Price	0%	0%	0%	0%	0%
	Lead-Time	5-6 wks.	5-6 wks.	5-6 wks.	5-6 wks.	-
NMOS 4K SRAM fast 4K x 1	Price	-2%	-1%	-1%	-1%	5%
	Lead-Time	5-6 wks.	5-6 wks.	5-6 wks.	5-6 wks.	-
NMOS 8K SRAM	Price	-3%	-2%	-3%	-2%	-10%
	Lead-Time	4-8 wks.	4-8 wks.	4-8 wks.	4-8 wks.	-
NMOS 16K SRAM 2K x 8 sub 100 ns	Price	-10%	-10%	-10%	-10%	-35%
	Lead-Time	10-12 wks.	12-14 wks.	12-14 wks.	16-18 wks.	-
NMOS 16K SRAM 2K x 8 slow	Price	-7%	-7%	-7%	-7%	-25%
	Lead-Time	8-10 wks.	10-12 wks.	10-12 wks.	10-12 wks.	-

Table 9-4c

1983 PRICE AND LEAD TIME TRENDS
STATIC RANDOM ACCESS MEMORIES

Product/Family	Comments	Product Life Cycle Trends	Product Replacement Trends
NMOS 1K SRAM	Manufacturers maintaining ready availability. Prices to increase in 1984.	Decline stage. Expect suppliers to phase out production in next two years.	Used only for special purpose applications.
NMOS 4K SRAM slow 1K x 4	Manufacturers maintaining ready availability. Prices to increase in 1984.	Decline stage. Production to continue for foreseeable future.	Users should upgrade to 16K SRAMs where possible for lower bit prices.
NMOS 4K SRAM slow 4K x 4	Manufacturers maintaining ready availability. Prices to increase in 1984.	Decline stage. Expect suppliers to phase out production in next 3-4 years.	Users should upgrade to 16K SRAMs (4K x 4) or (2K x 8) where possible for lower per bit prices.
NMOS 4K SRAM fast 1K x 4	Manufacturers maintaining ready availability. Prices to increase in 1984.	Decline stage. Product never achieved significant volume. Expect production phase out in next 4-5 years.	Users should upgrade to 16K SRAMs (2K x 8) where possible for lower per bit prices.
NMOS 4K SRAM fast 4K x 1	Manufacturers maintaining ready availability. Prices to increase in 1984.	Decline stage. Expect production phase out in next 3-4 years.	Users should upgrade to 16K SRAMs (2K x 8 or 4K x 4) where possible for lower per bit prices.
NMOS 8K SRAM	Prices to increase in 1984.	Mature, moving into decline stage. Expect product to be available for next 5 years.	Users should upgrade to 16K SRAMs for lower per bit prices.
NMOS 16K SRAM 2K x 8 sub 100 ns	Price per bit to be lower than all other fast SRAMs by 1984.	Early growth stage. Most new designs using 16K products.	Users who can will switch to 64K SRAMs in new designs in 1984, 1985.
NMOS 16K SRAM 2K x 8 slow	Lowest price per bit of any static RAM product.	Late growth stage. Expect consumption to peak in 1984.	Users who can will switch to 64K SRAMs in new designs in 1984, 1985.

(Continued)

9. Price Trends

Table 9-4c (Continued)

1983 PRICE AND LEAD TIME TRENDS
STATIC RANDOM ACCESS MEMORIES

Product/Family		1983 PRICE/LEAD TIME TRENDS				
		1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Year
NMOS 16K SRAM 4K x 4	Price	-8%	-8%	-8%	-8%	-30%
	Lead-Time	8-10 wks.	10-12 wks.	10-12 wks.	10-12 wks.	-
NMOS 16K SRAM 16K x 1	Price	-10%	-10%	-10%	-10	-35%
	Lead-Time	8-10 wks.	10-12 wks.	10-12 wks.	10-12 wks.	-
CMOS 1K SRAM	Price	0%	0%	0%	0%	0%
	Lead-Time	6-8 wks.	6-8 wks.	6-8 wks.	6-8 wks.	-
CMOS 4K SRAM	Price	-7%	-7%	-7%	-7%	-25%
	Lead-Time	4-6 wks.	4-6 wks.	4-6 wks.	4-6 wks.	-
CMOS 16K SRAM (4K x 4, 16K x1)	Price	-10%	-10%	-10%	-10%	-35%
	Lead-Time	6-8 wks.	6-8 wks.	8-10 wks.	10-12 wks.	-
CMOS 16K SRAM (2K x 8)	Price	-10%	-10%	-10%	-10%	-35%
	Lead-Time	6-8 wks.	6-8 wks.	8-10 wks.	10-12 wks.	-
CMOS 64K SRAM (see Note 1)	Price	-20%	-20%	-20%	-20%	-60%
	Lead-Time	6-8 wks.	6-8 wks.	6-8 wks.	6-8 wks.	-
	Price					
	Lead-Time					

Table 9-4c

1983 PRICE AND LEAD TIME TRENDS
STATIC RANDOM ACCESS MEMORIES

Product/Family	Comments	Product Life Cycle Trends	Product Replacement Trends
NMOS 16K SRAM 4K x 4	Price to continue to decline into 1984.	Early growth stage.	Will replace 4K x 1 and 2K x 8 in new designs starting in 1983, 1984.
NMOS 16K SRAM 16K x 1	Price to continue to decline into 1984.	Growth stage.	No direct replacement in foreseeable future.
CMOS 1K SRAM	—	Product in phase-out.	Replaced by 16K products.
CMOS 4K SRAM	—	Early decline stage.	Being replaced by 16K products.
CMOS 16K SRAM (4K x 4, 16K x1)	These products designed for higher speed performance.	Late design phase/early production.	—
CMOS 16K SRAM (2K x 8)	—	Early growth stages.	Expect to be replaced by 64K CMOS SRAM in 1985/86.
CMOS 64K SRAM (see Note 1)	Will become lowest price per bit static RAM in 1985.	Early design-in stage. Volume consumption to start in late 1983-84.	Replacement by 256K in larger memory systems expected to start by 1987, 1988.

Note 1: DATAQUEST believes that NMOS static RAMs will be designed for higher performance requirements while CMOS SRAMs will be offered as lower performance low cost products. This will be particularly true for 16K and larger products. Therefore, by 1984 CMOS SRAMs prices will be lower than equivalent NMOS products.

Source: DATAQUEST
August 1983

9. Price Trends

Table 9-4d

1983 PRICE AND LEAD TIME TRENDS
EPROMS

Product/Family		1983 PRICE/LEAD TIME TRENDS				
		1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Year
16K EPROMs NMOS	Price	0%	0%	0%	0%	0%
	Lead-Time	10-16 wks.	10-16 wks.	10-12 wks.	10-12 wks.	-
32K EPROMs NMOS	Price	0%	0%	0%	-5%	-5%
	Lead-Time	10-16 wks.	10-16 wks.	10-16 wks.	10-12 wks.	-
64K EPROMs NMOS	Price	0%	0%	0%	-5%	-5%
	Lead-Time	8-10 wks.	8-10 wks.	8-10 wks.	8-10 wks.	-
128K EPROMs NMOS	Price	-30%	-30%	-30%	-30%	-76%
	Lead-Time	4-6 wks.	4-6 wks.	4-6 wks.	4-6 wks.	-
16K EPROMs CMOS (see Note 1)	Price	-5%	0%	-5%	0%	-10%
	Lead-Time	8-12 wks.	8-12 wks.	8-12 wks.	8-12 wks.	-
32K EPROMs CMOS (see Note 1)	Price	-5%	-10%	-8%	-5%	-25%
	Lead-Time	8-12 wks.	8-12 wks.	8-12 wks.	8-12 wks.	-
64K EPROMs CMOS (see Note 1)	Price	-15%	-15%	-15%	-15%	-48%
	Lead-Time	8-12 wks.	8-12 wks.	8-12 wks.	8-12 wks.	-
256K EPROMs NMOS & CMOS (see Note 1)	Price	-15%	-15%	-15%	-15%	-48%
	Lead-Time	10-12 wks.	10-12 wks.	10-12 wks.	10-12 wks.	-

Note 1: DATAQUEST believes that NMOS EPROMs will be the generally used industry standard. CMOS products will be used primarily in low power and military applications.

Table 9-4d

1983 PRICE AND LEAD TIME TRENDS
EPROMS

Product/Family	Comments	Product Life Cycle Trends	Product Replacement Trends
16K EPROMs NMOS	—	Decline stage. We expect phase out in 1986, 1987.	Being replaced by 64K and 128K EPROMs for most applications.
32K EPROMs NMOS	—	Late mature stage. Expect unit demand to decline in 1984.	Being replaced by 64K and 128K EPROMs for most new designs.
64K EPROMs NMOS	Supply exceeds demand. Lowest price per bit EPROM in 1982.	Growth stage.	Displacement by 128K EPROMs in many applications to start in 1985.
128K EPROMs NMOS	New product will become lowest price per bit EPROM in 1983.	Early production stage.	Displacement by 256K EPROM in many applications in 1985.
16K EPROMs CMOS (see Note 1)	Very low volume product. Peak annual volume expected to be 3 million units.	Mature product.	32K and 64K products are used in most designs.
32K EPROMs CMOS (see Note 1)	Low volume product. Peak annual shipments expected to be 10 million units.	Early growth stage.	Replacement by 64K EPROMs in many applications in 1984 and 1985.
64K EPROMs CMOS (see Note 1)	—	Design-in stage.	Replacement by 128K EPROMs expected in many applications in 1985.
256K EPROMs NMOS & CMOS (see Note 1)	1983 mix is 90% NMOS, 10% CMOS. Prices to decrease rapidly for next two years.	Early design-in stage Will be principal software carriers by 1985.	—

Source: DATAQUEST
August 1983

9. Price Trends

Table 9-4e

1983 PRICE AND LEAD TIME TRENDS
ROMS

Product/Family		1983 PRICE/LEAD TIME TRENDS				
		1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Year
16K ROMs PNMOS	Price	-2%	-1%	-2%	-1%	-6%
	Lead-Time	4-8 wks.	6-8 wks.	6-8 wks.	6-8 wks.	-
32K ROMs PNMOS	Price	-3%	-1%	0%	0%	4%
	Lead-Time	6-8 wks.	8-10 wks.	8-10 wks.	8-10 wks.	-
64K ROMs PNMOS	Price	-7%	-7%	-7%	-7%	-25%
	Lead-Time	6-8 wks.	8-10 wks.	8-10 wks.	8-10 wks.	-
128K ROMs PNMOS	Price	-9%	-9%	-9%	-9%	-31%
	Lead-Time	8-12 wks.	8-12 wks.	8-12 wks.	8-12 wks.	-
256K ROMs PNMOS (see Note 1)	Price	-11%	-11%	-11%	-11%	-37%
	Lead-Time	8-12 wks.	8-12 wks.	8-12 wks.	8-12 wks.	-
16K ROMs CMOS	Price	-5%	-5%	-5%	-5%	-19%
	Lead-Time	8-12 wks.	8-12 wks.	8-12 wks.	8-12 wks.	-
32K ROMs CMOS	Price	-8%	-8%	-8%	-9%	-28%
	Lead-Time	8-12 wks.	8-12 wks.	8-12 wks.	8-12 wks.	-
64K ROMs CMOS	Price	-9%	-9%	-9%	-9%	-31%
	Lead-Time	8-12 wks.	8-12 wks.	8-12 wks.	8-12 wks.	-

Table 9-4e

1983 PRICE AND LEAD TIME TRENDS
ROMS

Product/Family	Comments	Product Life Cycle Trends	Product Replacement Trends
16K ROMs PNMOS	—	Decline stage. Expect phase out in next 2-3 years.	Being replaced by 64K, 128K ROMs in most applications.
32K ROMs PNMOS	—	Early decline stage. Expect product to be available for next 5 years.	Being replaced by 64K, 128K ROMs in most applications.
64K ROMs PNMOS	—	Growth stage. Peak consumption expected in 1984.	Replacement in many new designs expected in 1984, 1985.
128K ROMs PNMOS	—	Early growth stage.	Applications split between 128K and 256K ROMs depending on memory size needs.
256K ROMs PNMOS (see Note 1)	—	Early growth stage.	CMOS 256K ROMs to be used in most 256K applications.
16K ROMs CMOS	—	Growth stage. Usage limited to military and very low power application.	—
32K ROMs CMOS	—	Early growth stage. Usage limited to military and very low power applications.	—
64K ROMs CMOS	—	Early growth stage. Usage limited to military and very low power applications.	—

(Continued)

Table 9-4e (Continued)

1983 PRICE AND LEAD TIME TRENDS
ROMS

Product/Family		1983 PRICE/LEAD TIME TRENDS				
		1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Year
128K ROMs CMOS	Price	-14%	-14%	-13%	-13%	-44%
	Lead-Time	8-12 wks.	8-12 wks.	8-12 wks.	8-12 wks.	-
256K ROMs CMOS (see Note 1)	Price	-17%	-17%	-18%	-17%	-53%
	Lead-Time	8-12 wks.	8-12 wks.	8-12 wks.	8-12 wks.	-
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					

Note 1: DATAQUEST estimates that CMOS technology will become the standard ROM technology starting with 256K bit ROMs. By 1986, cost per bit for 256K CMOS ROMs will be less than cost per bit for 256K NMOS ROMs.

Table 9-4e

1983 PRICE AND LEAD TIME TRENDS
ROMS

Product/Family	Comments	Product Life Cycle Trends	Product Replacement Trends
128K ROMs CMOS	—	Early growth stage.	—
256K ROMs CMOS (see Note 1)	—	Design in stage. Volume production starts during 1983.	256K CMOS ROMs expected to be the industry standard ROM product from 1985 to 1988.

Source: DATAQUEST
August 1983

9. Price Trends

Table 9-4f

1983 PRICE AND LEAD TIME TRENDS
EEPROMS

Product/Family		1983 PRICE/LEAD TIME TRENDS				
		1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Year
16K EEPROM	Price	-14%	-14%	-14%	-13%	-44%
	Lead-Time	12-16 wks.	12-16 wks.	12-16 wks.	12-16 wks.	-
32K EEPROM	Price	N/A	N/A	N/A	N/A	-
	Lead-Time	N/A	N/A	4-8 wks.	4-8 wks.	-
64K EEPROM	Price	N/A	N/A	N/A	N/A	-
	Lead-Time	8-12 wks.	N/A	N/A	48 wks.	-
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					

9. Price Trends

Table 9-4f

1983 PRICE AND LEAD TIME TRENDS
EEPROMS

Product/Family	Comments	Product Life Cycle Trends	Product Replacement Trends
16K EEPROM	—	Growth stage.	64K, 128K products expected to become volume industry standard products by 1985, 1986.
32K EEPROM	Industry standards not established. Will be several different types.	Introduction stage.	—
64K EEPROM	Industry standards not established. Will be several different types.	Introduction stage.	—

Source: DATAQUEST
August 1983

9. Price Trends

Table 9-4g

1983 PRICE AND LEAD TIME TRENDS
BIPOLAR MEMORIES

Product/Family		1983 PRICE/LEAD TIME TRENDS				
		1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Year
1K PROMs & less TTL	Price	0%	+5%	+5%	+5%	+16%
	Lead-Time	2-12 wks.	6-16 wks.	8-16 wks.	8-16 wks.	-
2K PROM TTL	Price	0%	+5%	+5%	+5%	+16%
	Lead-Time	4-6 wks.	6-16 wks.	8-16 wks.	8-16 wks.	-
4K PROM TTL	Price	0%	+10%	+5%	+5%	+21%
	Lead-Time	4-6 wks.	6-16 wks.	8-16 wks.	8-16 wks.	-
8K PROM TTL	Price	0%	+10%	+5%	+5%	+21%
	Lead-Time	4-6 wks.	6-16 wks.	8-16 wks.	8-16 wks.	-
16K PROM TTL	Price	0%	+10%	+5%	+5%	+21%
	Lead-Time	4-6 wks.	6-16 wks.	8-16 wks.	8-16 wks.	-
32K PROM TTL	Price	0%	0%	0%	0%	0%
	Lead-Time	8-12 wks.	8-12 wks.	8-16 wks.	8-16 wks.	-
	Price					
	Lead-Time					
	Price					
	Lead-Time					

Table 9-4g

1983 PRICE AND LEAD TIME TRENDS
BIPOLAR MEMORIES

Product/Family	Comments	Product Life Cycle Trends	Product Replacement Trends
1K PROMs & less TTL	—	Mature phase.	Will eventually be replaced by low cost programmable logic devices.
2K PROM TTL	—	Mature phase.	Will eventually be replaced by low cost programmable logic devices.
4K PROM TTL	—	Mature phase.	Some conversion to EPROMs, EEPROMs in lower performance applications
8K PROM TTL	—	Mature phase.	Some conversion to EPROMs, EEPROMs in lower performance applications.
16K PROM TTL	—	Mature phase.	Some conversion to EPROMs, EEPROMs in lower performance applications.
32K PROM TTL	Mostly military designs now. Low performance product.	Design in stage.	Many commercial applications use EPROMs or EEPROMs.

Source: DATAQUEST
August 1983

9. Price Trends

Table 9-4h

1983 PRICE AND LEAD TIME TRENDS
BIPOLAR MEMORIES

Product/Family		1983 PRICE/LEAD TIME TRENDS				
		1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Year
1K RAM TTL	Price	0%	0%	0%	0%	0%
	Lead-Time	1-2 wks.	1-2 wks.	1-2 wks.	1-2 wks.	-
1K RAM ECL	Price	0%	0%	+2%	+3%	+5%
	Lead-Time	2-8 wks.	2-8 wks.	2-6 wks.	2-6 wks.	-
4K RAM ECL	Price	0%	0%	-3%	-2%	-5%
	Lead-Time	4-8 wks.	4-8 wks.	4-10 wks.	4-10 wks.	-
16K RAM ECL	Price	-10%	-10%	-10%	-10%	-34%
	Lead-Time	10-12 wks.	10-12 wks.	12-14 wks.	12-14 wks.	-
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					

Table 9-4h

1983 PRICE AND LEAD TIME TRENDS
BIPOLAR MEMORIES

Product/Family	Comments	Product Life Cycle Trends	Product Replacement Trends
1K RAM TTL	—	Decline stage. Some companies to start phasing out in 1-2 years.	Products being replaced by high speed MOS memories.
1K RAM ECL	—		Replaced by 4K ECL RAM in new designs.
4K RAM ECL	—	Growth stage.	Presently industry standards for high spend systems.
16K RAM ECL	Lead times are for 1,000 quantities. Larger quantities will take longer in 1983.	Early production stage.	—

Source: DATAQUEST
August 1983

9. Price Trends

Table 9-4i

1983 PRICE AND LEAD TIME TRENDS
BIPOLAR LSI

Product/Family		1983 PRICE/LEAD TIME TRENDS				
		1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Year
Programmable Logic (PAL and IFL)	Price	-5%	-5%	-5%	-5%	-19%
	Lead-Time	4-6 wks.	4-10 wks.	12-16 wks.	12-18 wks.	-
Microprocessors 2900	Price	0%	0%	0%	0%	0%
	Lead-Time	2-4 wks.	2-4 wks.	2-4 wks.	2-4 wks.	-
Microprocessors 8 x 300	Price	-2%	0%	-2%	0%	-4%
	Lead-Time	6-8 wks.	6-8 wks.	6-8 wks.	6-8 wks.	-
Microprocessors 29116	Price	-10%	-10%	-10%	-10%	-35%
	Lead-Time	2-4 wks.	2-4 wks.	2-4 wks.	2-4 wks.	-
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					

9. Price Trends

Table 9-4i

1983 PRICE AND LEAD TIME TRENDS
BIPOLAR LSI

Product/Family	Comments	Product Life Cycle Trends	Product Replacement Trends
Programmable Logic (PAL and IFL)	—	Growth stage.	—
Microprocessors 2900	—	Late growth stage.	—
Microprocessors 8 x 300	—	Late growth stage.	—
Microprocessors 29116	—	Design in/early production stage.	—

Source: DATAQUEST
August 1983

9. Price Trends

Table 9-4j

1983 PRICE AND LEAD TIME TRENDS
MOS MICROPROCESSORS

Product/Family		1983 PRICE/LEAD TIME TRENDS				
		1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Year
4-bit Microcontrollers	Price	0%	0%	-6%	-2%	-8%
	Lead-Time	12-22 wks.	12-22 wks.	12-22 wks.	12-22 wks.	-
8-bit Microcontrollers	Price	-2%	-1%	-1%	-1%	-5%
	Lead-Time	12-22 wks.	14-25 wks.	18-30 wks.	30-35 wks.	-
16-bit Microcontrollers	Price	-3%	-3%	-3%	-3%	-11%
	Lead-Time	12-18 wks.	12-18 wks.	12-18 wks.	12-18 wks.	-
8-bit Microprocessors	Price	-6%	-2%	-0%	-0%	-8%
	Lead-Time	8-12 wks.	12-18 wks.	18-30 wks.	18-30 wks.	-
16-bit Microprocessors	Price	-10%	-3%	-2%	-2%	-16%
	Lead-Time	12-15 wks.	12-15 wks.	12-15 wks.	12-15 wks.	-
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					

9. Price Trends

Table 9-4j

1983 PRICE AND LEAD TIME TRENDS
MOS MICROPROCESSORS

Product/Family	Comments	Product Life Cycle Trends	Product Replacement Trends
4-bit Microcontrollers	NMOS product prices to stabilize. CMOS prices to decline 15-20%.	Mature phase. Peak usage in 1984. Unit volume to decline 14% per year 1984-1988.	Replaced by 8 bit microcontroller. Unit volume crossover in 1985.
8-bit Microcontrollers	High end products maintaining price. (Z8, 6801, 5051). Other low end products decrease 10-15% per year.	Growth stage. ROM based types to mature by 1985. EPROM, E^2PROM types to grow through 1990.	50% of ROM based types to be replaced by EPROM and E^2PROM based types by 1985, 1986.
16-bit Microcontrollers	—	Design in stage.	—
8-bit Microprocessors	8088 on allocation.	Mature products.	New products like 80188 will replace 8088 and Z80 in new designs.
16-bit Microprocessors	—	Growth stage.	80186 to replace 8086 in new designs starting in 1984. 68010 to replace 68000 in new designs in 1984.

Source: DATAQUEST
August 1983

9. Price Trends

Table 9-4k

1983 PRICE AND LEAD TIME TRENDS
LINEAR

Product/Family		1983 PRICE/LEAD TIME TRENDS				
		1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Year
Operational Amplifiers	Price	0%	0%	-5%	+5%	+10%
	Lead-Time	8-12 wks.	8-12 wks.	10-16 wks.	10-18 wks.	-
Comparators	Price	0%	0%	+5%	+5%	+10%
	Lead-Time	8-12 wks.	8-12 wks.	10-16 wks.	16-18 wks.	-
8-bit D/A Converters	Price	0%	0%	0%	0%	0%
	Lead-Time	8-16 wks.	8-16 wks.	8-16 wks.	8-16 wks.	-
12-bit D/A Converters	Price	0%	0%	-0%	-0%	-8%
	Lead-Time	8-16 wks.	8-16 wks.	8-16 wks.	8-16 wks.	-
Voltage Regulators	Price	0%	0%	+5%	+5%	+10%
	Lead-Time	8-12 wks.	6-10 wks.	6-10 wks.	10-12 wks.	-
	Price					
	Lead-Time					
	Price					
	Lead-Time					
	Price					
	Lead-Time					

9. Price Trends

Table 9-4k

1983 PRICE AND LEAD TIME TRENDS
LINEAR

Product/Family	Comments	Product Life Cycle Trends	Product Replacement Trends
Operational Amplifiers	—	Mature products.	Bifet devices becoming widely used as standard.
Comparators	—	Mature products.	—
8-bit D/A Converters	—	Mature products.	Higher precision products being used in new designs.
12-bit D/A Converters	—	Growth stage.	—
Voltage Regulators	—	Mature products.	—

Source: DATAQUEST
August 1983

9. Price Trends

Table 9-5a

PROJECTED PRICES PER BIT
(millicents)
DYNAMIC MOS RAMS

Memory Size (bits)	1982	1983	1984	1985	1986	1987	1988	1989
16K	8.5	8.9	9.2	9.5	9.8	11.0	15.0	20.0
64K	8.4	6.5	4.9	3.8	3.6	3.4	3.2	3.1
256K	38.1	19.1	9.5	4.8	2.7	2.0	1.9	1.8
1,000K	-	-	14.3	6.7	3.3	2.5	1.8	1.5

Table 9-5b

PROJECTED PRICES PER BIT
(millicents)
STATIC MOS RAMS
(100 ns access times)

Memory Size (bits)	1982	1983	1984	1985	1986	1987	1988	1989
4K	61.0	61.0	63.5	65.9	67.1	70.0	100.0	-
16K	33.6	24.4	19.8	16.8	16.8	17.2	17.8	18.2
64K	91.6	38.1	15.3	10.7	7.6	7.2	7.0	6.8
256K	-	-	30.5	15.3	9.5	6.8	6.4	6.0

Source: DATAQUEST
July 1983

9. Price Trends

PRICE FACTORS

One view of price is that it is the only variable in the marketing mix that generates income, while all the others, including research and development, materials, labor, equipment, sales, general and administrative expenses, and distribution, are cost factors The user should be sensitive to the fact that small changes in price have a large impact on supplier profitability. This is especially true if the semiconductor product timing is premature, and the user is pressing for forward pricing before the suppliers have had enough time for production refinements to reduce costs.

A supplier of semiconductors or a user of semiconductors may each be considered to be passive or active in its attitude and approach toward pricing. That is, either may be a "price-taker" or a "price-maker." A semiconductor user may be a price-taker for any of the following reasons:

- The industry capacity to produce a product may be less than the demand for the product. The user must be a price-taker for the duration of this situation, or must find a substitute product to meet the need.
- The price may be dictated by the opportunity costs of the lowest-cost producer or a competitor, and demanding a lower price would result in supplier withdrawal from the market. The user becomes a price-taker at this point.
- The price may be government controlled.
- The product may be sole-sourced.

For a semiconductor user to be a price-maker, the following two conditions must be met:

- The planned product consumption must be a relatively large percentage of the total industry capacity available to produce the product.
- The user must be able to increase consumption at least as rapidly as industry capacity can expand.

Pricing of semiconductors has developed a reputation of almost invariably dropping rapidly during the early life of a product, and continuing to drop as the product approaches maturity. This characteristic has contributed significantly to the pervasiveness of semiconductors and to the rapid increases in demand in many end markets for products and equipment using semiconductors.

9. Price Trends

The semiconductor industry is currently characterized by a large number of high-technology suppliers, each capable of offering a range of goods and services. As the technology has evolved, subsets of these suppliers have emerged as specialists in one or more particular areas of expertise. Competitive relationships and other conditions change so quickly that published pricing is not always the best indicator of the high-volume pricing available at any particular time. In the case of custom products, semi-custom products, and new or unannounced products, published pricing may not even exist.

There are three traditional pricing conventions, as follows, and all three are used in the semiconductor industry:

- Cost-based pricing, as may occur, for example, in the case of a cost-plus-fee contract with a sole source of a custom product
- Market-based pricing, as in the case of multiple-sourced commodity items
- Competitive bid pricing, which is the approach often preferred by semiconductor users when the suppliers do not willingly arrive at pricing through discussing their costs with customers, and when the prices are not purely market-determined for one or more reasons

COST-BASED PRICING

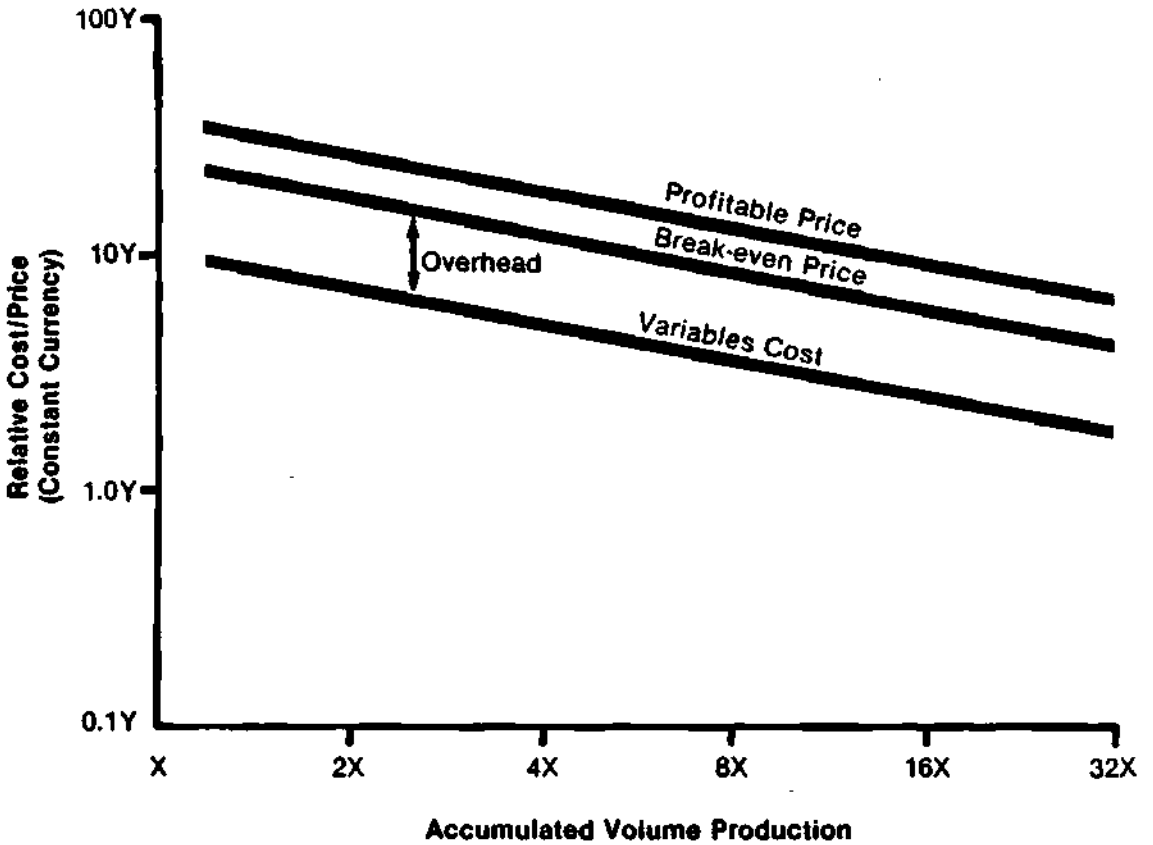
A primary factor in the price decline of most semiconductors is the experience (learning) effect discussed in Chapter 8, Cost Trends. If a supplier follows a strategy of cost-based pricing during early product life and accumulates experience rapidly, it is not unusual for a new product price to decline by a factor of two or more during the first one to two years of product life. On the other hand, when a product is mature, the effects of inflation may offset the decline in production costs to the point where the price begins to rise again.

Figure 9-1 illustrates a cost-based price curve for a new product assumed to have a 20 percent learning factor and 110 percent overhead. The curve is plotted in constant currency and shows a steady decline in costs. In this case, break-even sales price and profitable price follow the slope of the cost curve, displaced by the overhead and profit margin, respectively. Profit margin is represented on the graph as the difference between break-even price and profitable price.

9. Price Trends

Figure 9-1

PRICE TREND FOR NEW PRODUCT WITH COST-BASED PRICING STRATEGY



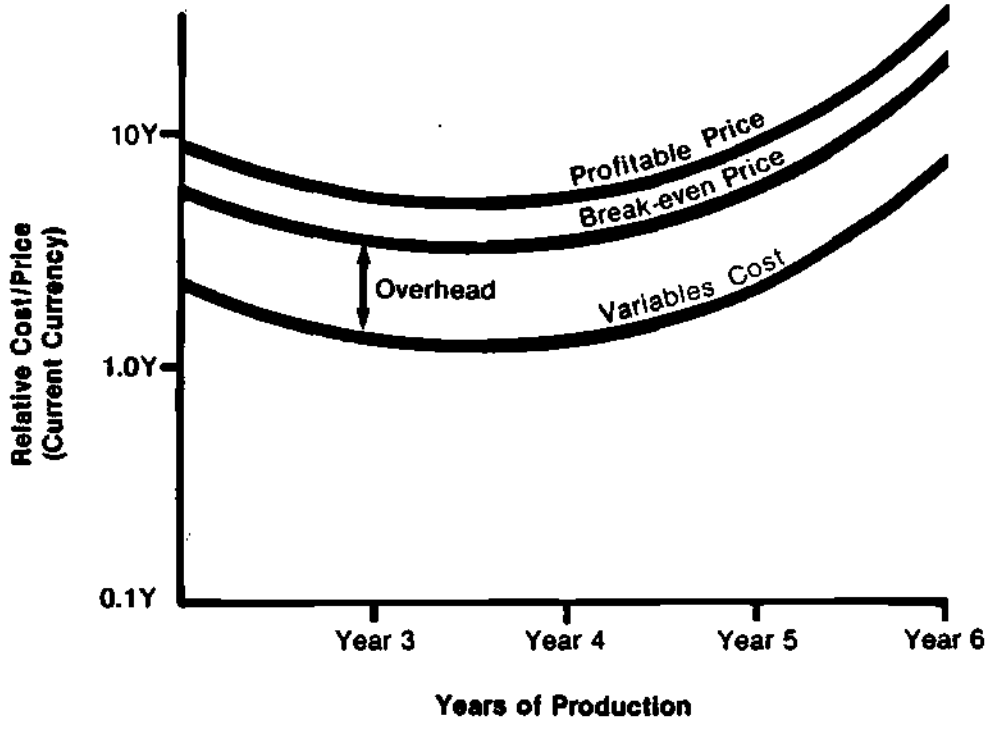
Source: DATAQUEST, Inc.
April 1982

As a product approaches maturity, its pricing behavior, in the case of cost-based pricing, follows the pattern illustrated in Figure 9-2. In this figure we use current currency so that the effects of inflation may be taken into account. The years shown (3 through 6) are for illustration only and vary widely by product type. Some price increases may occur during the mature phase of a product's life cycle, due to inflation overriding the advantages of improved cost-effectiveness. However, it is during the declining phase of the product life cycle, when the production volume is declining, that very rapid price increases occur.

9. Price Trends

Figure 9-2

PRICE TREND FOR MATURE PRODUCT WITH
COST-BASED PRICING STRATEGY



Source: DATAQUEST, Inc.
April 1982

MARKET-BASED PRICING

As the semiconductor industry has grown and competition has increased, market-based pricing has become a major factor. Thus the user needs to be aware of the effects of various market conditions on pricing.

9. Price Trends

In a softening market, suppliers may become more willing to accept low-margin business to avoid layoffs and production cutbacks. The most efficient suppliers may be able to increase market share under such conditions, and thus continue in a profitable mode longer than the low-volume suppliers under equivalent conditions. In the semiconductor industry, weak commodity pricing tends to occur in soft market conditions.

As the economy recovers, conditions improve, and commodity lead times usually lengthen because the suppliers cannot increase effective capacity to keep pace with demand. Efficiency of production decreases, and prices tend to increase to compensate. Demands by users for quick delivery cause suppliers to increase shift and overtime premiums to keep pace, causing further price increases.

In any competitive situation, such as the semiconductor industry, opportunity costs have a bearing on price. Any time that a user demands more and more of a supplier's capacity, the user must be prepared to compensate the supplier for lost opportunities that would otherwise be pursued. This is a fundamental characteristic of the free enterprise environment.

NEGOTIATED OR COMPETITIVE BID PRICING

The negotiated pricing approach is often used when purchasing for government programs or when making very large or long-term procurements of semiconductors. This approach can be advantageous to both user and supplier if it is done carefully and professionally. Semiconductor business negotiation strategies and tactics are not discussed here, as they exceed the scope of this document.

Both buyer and seller involved in transactions in the United States must be very cautious about inducing or granting discriminatory pricing in violation of the Robinson-Patman Act. This act is violated if a seller provides lower prices to one customer than to other customers competing in that customer's marketplace, unless the lower price is also offered to that customer by a competitor of the seller. The act is also violated if a buyer knowingly induces a discriminatory price by misleading the supplier into thinking that in providing such a price the supplier is meeting the equally low price of a competitor. In other countries, negotiated pricing regulations vary widely and may or may not pose similar constraints. When in doubt in such matters, the user should seek corporate legal advice.

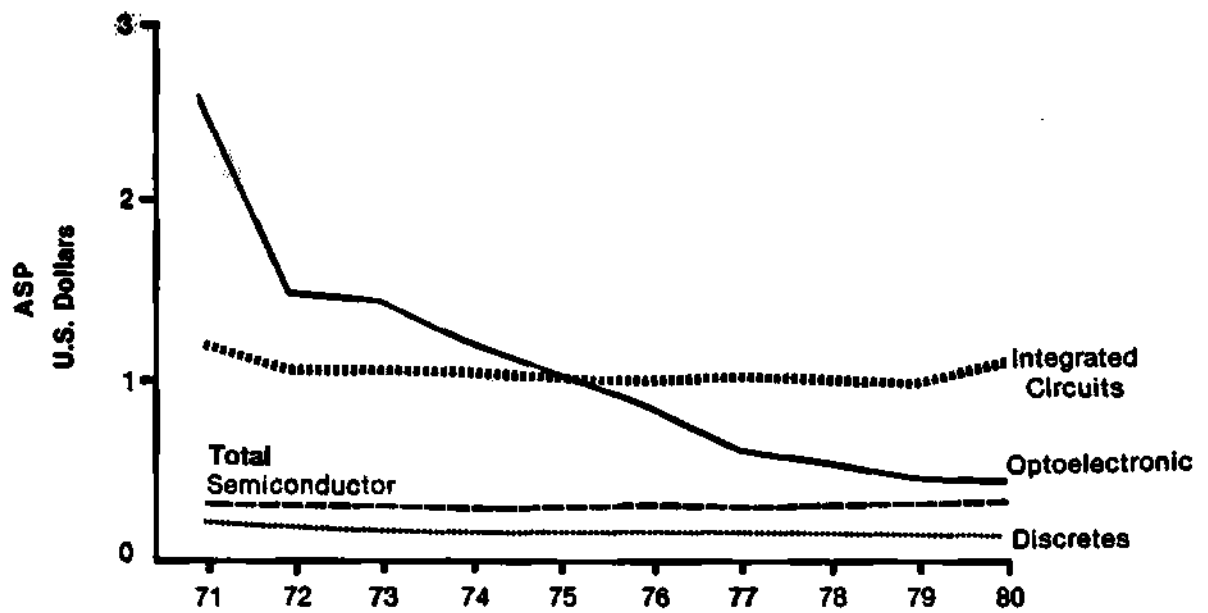
9. Price Trends

ESTIMATED AVERAGE SELLING PRICES

Average selling prices for semiconductors have tended to approach a lower boundary dictated by packaging, testing, and handling costs as each given technology matures. Price trends during the last 10 years by major technology category are illustrated in Figures 9-3, 9-4, and 9-5. The experience factor and its impact on MOS and optoelectronics is graphically represented by the steep slopes of their respective price curves (Figures 9-4 and 9-5). DATAQUEST believes that new technologies such as bubble memories and gallium arsenide will realize similar ASP trends during the mid and late 1980s.

Figure 9-3

ESTIMATED AVERAGE SELLING PRICES
OF SEMICONDUCTORS
(U.S. Dollars)

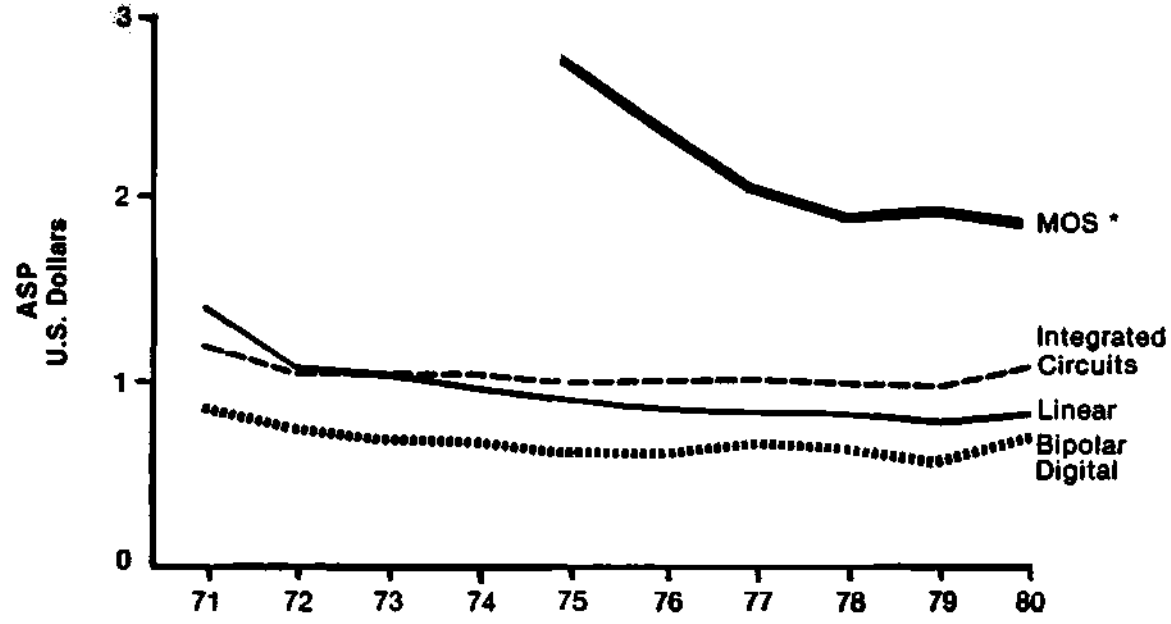


Source: DATAQUEST, Inc.
April 1982

9. Price Trends

Figure 9-4

ESTIMATED AVERAGE SELLING PRICES OF
INTEGRATED CIRCUITS
(U.S. Dollars)



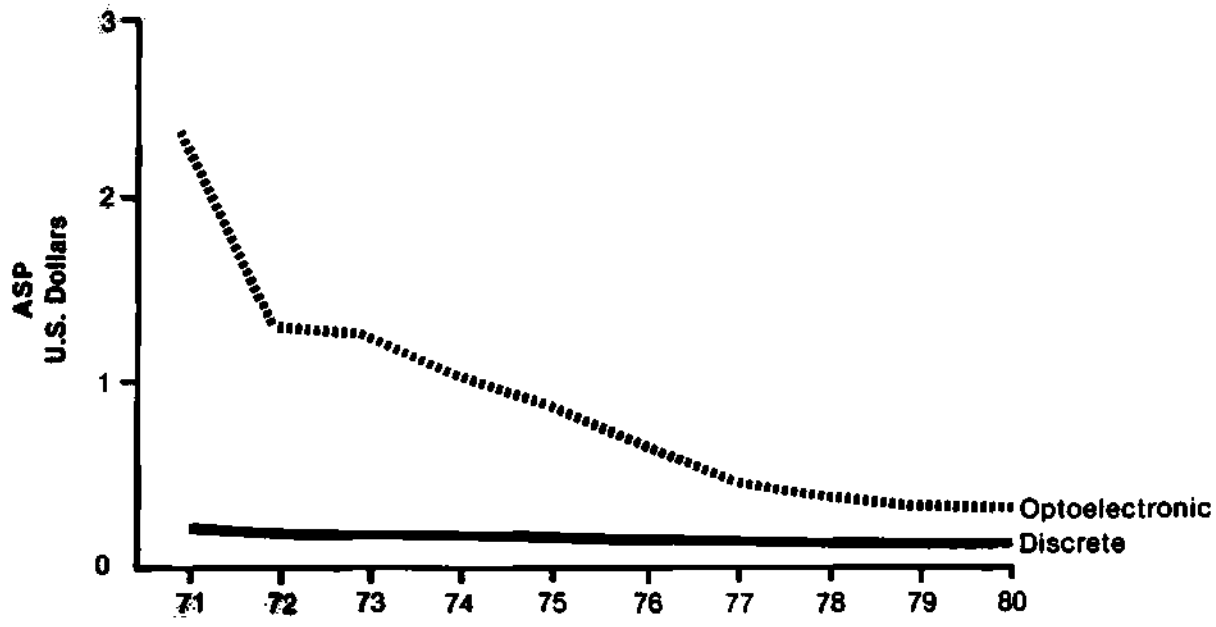
* (MOS) 1971-1974 Off Scale

Source: DATAQUEST, Inc.
April 1982

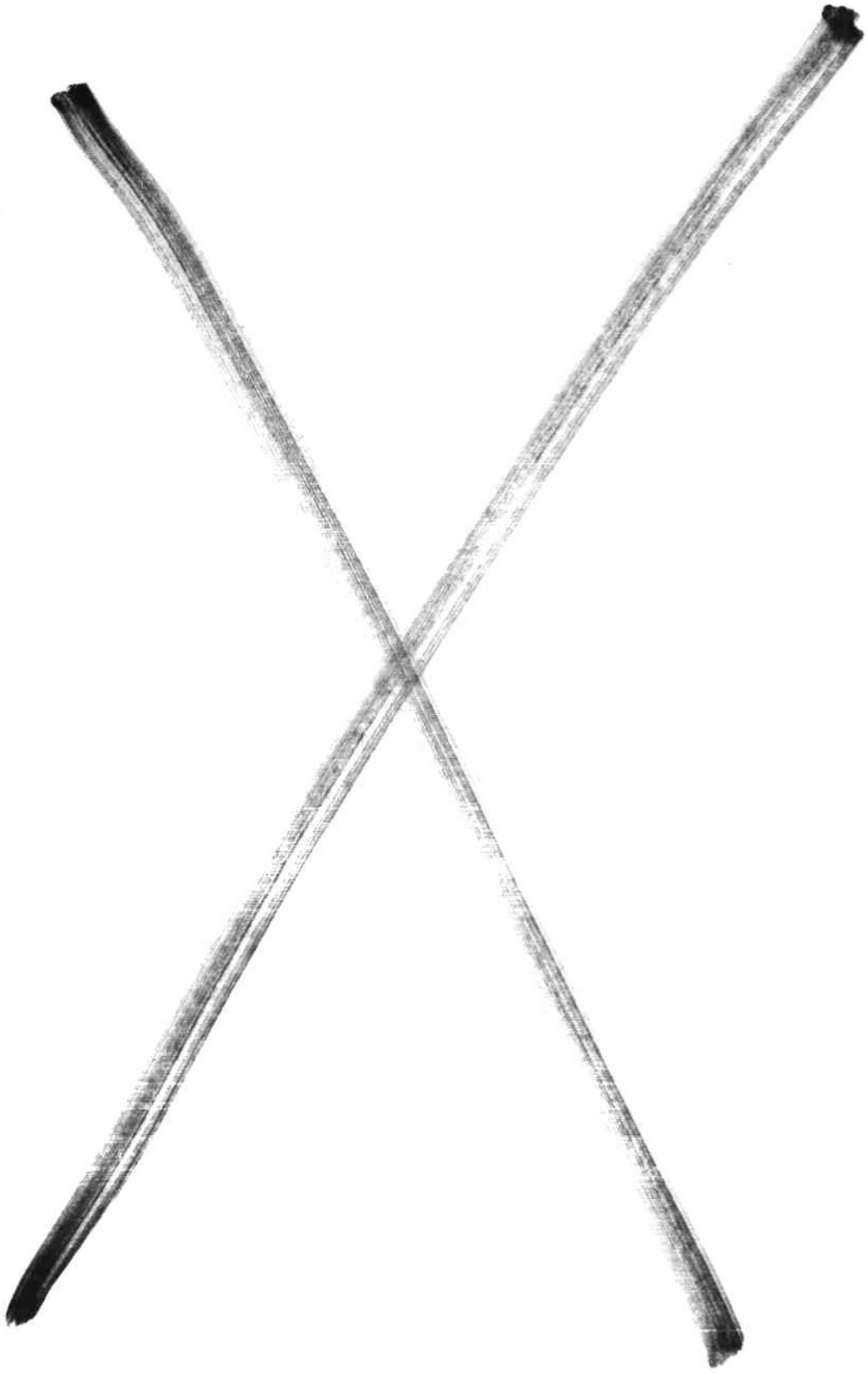
9. Price Trends

Figure 9-5

ESTIMATED AVERAGE SELLING PRICES OF DISCRETE
AND OPTOELECTRONIC DEVICES
(U.S. Dollars)



Source: DATAQUEST, Inc.
April 1982



Nielsen Dataquest

INQUIRY RESPONSE

DATE: September 8, 1983

TO: Richard Bishop/Kaiser Electronics

FROM: Mary Olsson

This information has been compiled in response to your inquiry of August

Please file in Section 10, Vol.1 for future reference.

Projected Production Availability Price Curves and Package Costs of LCC Devices.

Leads, 883B, 38510, LCC vs. DIP price

1) Company	Product	Samples	Production	Comments
Fairchild	54F00L		now-14 pin; full MIL	54F series on allocation
	54F04L		now-14 pin; full MIL	74F product available
	54F08L		now-14 pin; full MIL	Leadtimes 26 weeks
	54F10L		now-14 pin; full MIL	Equivalent Motorola
	54F32L		now-14 pin; full MIL	parts 2-3 weeks
	54F64L		now-14 pin; full MIL	leadtime
	54F74L		now-14 pin; full MIL	
	54F151L		now-16 pin; full MIL	
	54F163		now-16 pin; full MIL	
	54F164		now-14 pin; full MIL	
	54F158L		now-16 pin; full MIL	
	54F244L		now-20 pin; full MIL	
	54F374L		N/A	54F374-eng. problems
	54S139L		now-16 pin; full MIL	54S139TI - 28 weeks
	54LS377L		now-20 pin; full MIL	54S & LS leadtime
	932565		now-24 pin; full MIL	18-20 weeks
	54F240L		now-14 pin; full MIL	
Texas Instruments	54S00		now-14 pin; full MIL	54F and LS on allocation
	54S30		now-14 pin; full MIL	Leadtime 22 weeks
	54S64		now-14 pin; full MIL	
	54S74		now-14 pin; full MIL	
	54S86		now-14 pin; full MIL	
	54S241		now-20 pin; full MIL	
	54LS122		now-14 pin; full MIL	
	54LS125		now-14 pin; full MIL	
	54LS123		now-16 pin; full MIL	
	54LS157		now-16 pin; full MIL	
	54LS166		now-16 pin; full MIL	
	54LS241		now-20 pin; full MIL	
	54LS245		now-20 pin; full MIL	
	54LS257		now-16 pin; full MIL	
	54LS273		now-20 pin; full MIL	
	54LS299		now-20 pin; full MIL	
	54LS378		now-16 pin; full MIL	
	54LS174		now-16 pin; full MIL	
	54LS374		now-20 pin; full MIL	
	54LS377		now-20 pin; full MIL	
	54AS04		now-20 pin; full MIL	54AS and ALS leadtime 18 weeks

Leads, 883B, 38510, LCC vs. DIP price

Company	Product	Samples	Production	Comments
Texas Instruments	54AS05		now-20 pin; full MIL	
	54AS74		now-20 pin; full MIL	
	54AS251		now-20 pin; full MIL	
	54ALS00		now-20 pin; full MIL	
	54LS02		now-20 pin; full MIL	
	54ALS08		now-20 pin; full MIL	
	54ALS10		now-20 pin; full MIL	
	54ALS20		now-20 pin; full MIL	
	54ALS28		now-20 pin; full MIL	
	54ALS32		now-20 pin; full MIL	
	54ALS74		now-20 pin; full MIL	
	54ALS109		now-20 pin; full MIL	
	54ALS163		now-20 pin; full MIL	
	54ALS169		now-20 pin; full MIL	
	54ALS175		now-20 pin; full MIL	
	54ALS138		now-20 pin; full MIL	
	54ALS240		now-20 pin; full MIL	
	54ALS244		now-20 pin; full MIL	
	54ALS273		now-20 pin; full MIL	
	54ALS374		now-20 pin; full MIL	
Intel	8251A		now-28 pin; full MIL	20 week lead-time on peripherals & support products
	8254		now-24 pin; full MIL	
	8287		now-20 pin; full MIL	
	8286		now-20 pin; full MIL	
	27128		now-28 pin; full MIL	10-12 weeks leadtime
Harris	HA4-4902-8 (4900)		now-16 pin; full MIL	
	82S105FPLS	N/A	N/A	
	HPL77153(82S153)		now-20 pin; full MIL	
	HPL77209(16L8)		now-20 pin; full MIL	
MMI	PAL 16R4AML		now-20 pin; full MIL	4-6 weeks leadtime
	PAL 16R6AML		now-20 pin; full MIL	4-6 weeks leadtime
	PAL 16R8AML		now-20 pin; full MIL	4-6 weeks leadtime
	PAL 16L8AML		now-20 pin; full MIL	4-6 weeks leadtime
	PAL 20x8AML		now-24 pin; full MIL	4-6 weeks leadtime
	PAL 20L10AML		now-24 pin; full MIL	4-6 weeks leadtime
	PAL 20L10AML	3Q83-24 pin; 883B	4Q83	
	PAL 20R4AML	3Q83-24 pin; 883B	4Q83	
	PAL 20R6AML	3Q83-24 pin; 883B	4Q83	
	PAL 20R8AML	3Q83-24 pin; 883B	4Q83	
	PAL 20L8AML	3Q83-24 pin; 883B	4Q83	
AMD	2950LM		now-28 pin; 883C	16-18 weeks leadtime
	2957LM		now-20 pin; 883C	16-18 weeks leadtime
	2911LMB		now-20 pin; 883C	16-18 weeks leadtime
	29825LMB		now-28 pin; 883B	16-18 weeks leadtime
	27S43ADM		now-24 pin; 883B	12 week leadtime
	27S43ALM		LCC not available	
	27S25DM		now-24 pin; 883B	12 week leadtime
	16H8DM		now-20 pin; 883B&C	12 week leadtime
	16H8ALMB		LCC not available	
	27S29DM		now-20 pin; 883B	12 week leadtime
	27S29ALM		LCC not available	

ESTIMATED DEVICE COST
LCC vs DIP
(TTL)

1983	1984	1985	1986
LCC 3 x DIP	LCC 1-2 x DIP	LCC 1 x DIP	LCC = DIP

ESTIMATED PACKAGE COST TRENDS
STANDARD DIP

1983	1984	1985	1986
0%	2%	2%	2-5%

CERAMIC PACKAGE SUPPLIES

Advanced Hybrid Technology
Airpax Corporation
AMP, Inc.
Augat, Inc.
Barry & Associates
Brush Wellman
Burndy, Inc.
Ceramic Systems
Diacon Inc.
Gibson-Egan Co.
Interamics
Interlek, Inc.
Kyocera International
3M Tech Ceramics
Methode Electronics, Inc.
Rosenthal Technik, N.A., Inc.
Western Electric

Nielsen Dataquest

INQUIRY RESPONSE

DATE: 30 August 1983

TO: Richard Bishop/Kaiser

FROM: Mary Olsson/Dataquest

This information has been compiled in response to your inquiry of August 1983

Please file in Section 10, Vol.I for future reference.

Subject: Projected Production Availability Price Curves and Package Costs of LCC Devices

1) Company	Product	Samples	Production	Comments
Raytheon	29673	2Q84-32 lead; 38510	now-32 lead;883B	
	Other		now-20,28,44,68 lead packages, 883C	
Signetics	825105	4Q83-28 pin/square	1Q84-28 pin	Leaded & leadless full 883B & 38510 available
	825153	4Q83-20 pin/square	1Q84-20 pin	
Xicor	2816	3Q83-24 pin	4Q83-24 pin; 883B	
Idt	6116S/L		now-28 & 32 pins	Full 883B & 38510 available
	6168S/L		now-20 pin	
	Others			
	7m864/8m864	1Q84-24 pin	1Q84-24 pin; 883B	
	7m464	1Q84-24 pin	1Q84-24 pin; 883B	
	7m164	1Q84-24 pin	1Q84-24 pin; 883B	
Motorola	68000		now 68 lead; 883B	
	68000		now 68 lead; 38510	
	68010	1Q84,48 pin		Full MIL process

ESTIMATED PACKAGE COST TRENDS
STANDARD DIP

1983	1984	1985	1986
0%	2%	2% to 5%	5%

ESTIMATED DEVICE COST
LCC vs. DIP
(LSI products)

1983	1984	1985	1986
LCC 2-3 x DIP	LCC 1.4-1.7 x DIP	LCC 1.2 x DIP	LCC 1.1 x DIP

:tg

10. Product Factors

Many product factors affect the semiconductor procurement function and can upset the supply/demand equation if improperly addressed. These include:

- Electrical specifications
- Package requirements
- Quality constraints
- Reliability needs
- Computer aided design (CAD) considerations
- Environmental constraints
- Multiple-sourcing requirements

ELECTRICAL SPECIFICATIONS

Electrical specifications cover one of the most important areas of semiconductor product documentation. These specifications are the reference for the functional performance characteristics and requirements of semiconductors. Users employ one or more of the following approaches regarding electrical specifications when purchasing semiconductors:

- The purchase order may call for the devices to meet user-prepared specifications.
- The purchase order may require that the devices meet vendor-prepared specifications.
- The purchase order may require that the devices meet Government or Military Standard (MIL-STD) specifications.
- The purchase order may specify a generic part type or a vendor's name and part number.

In any of the above cases, the purchase order should list any applicable exceptions, to avoid confusion.

It is general practice in the semiconductor industry to use supplier or military standard part numbers when purchasing parts from a distributor. Most distributors are not equipped to process semiconductors to special electrical specifications. Most distributors, however, are equipped to perform PROM and EPROM programming, and some distributors subcontract burn-in and other special screening. Unless very large quantities of parts are involved, it is uneconomical for a distributor to process orders for non-standard products.

10. Product Factors

The electrical specification for a standard semiconductor product is usually part of a data sheet that may range in length from one page (for a gate or transistor) to sixteen or more pages (for a microprocessor). The data sheet often includes the following types of functional information:

- Device description
- Pin names and signal definitions
- Functional diagram
- Critical signal waveshapes and timing relationships
- Maximum ratings for the device
- Package description and dimensions
- DC electrical characteristics and worst-case limits
- Transient electrical characteristics and worst-case limits
- Applications data

Information that may not appear on the data sheet, but which may be important to the buyer includes the following:

- Worst-case timing for the user's application
- Thermal characteristics of the package
- Worst-case mechanical dimensions
- Die revision level
- Quality assurance provisions, product screening, and product test methods
- Expected mean time between failures (MTBF) or other reliability data
- Warranty data
- Patent data

Some of the items listed here require direct customer/supplier interface on an ongoing basis for complete resolution. The semiconductor user should weigh the risks and the economics involved, and then select a course of action that will successfully fulfill the specification requirements.

10. Product Factors

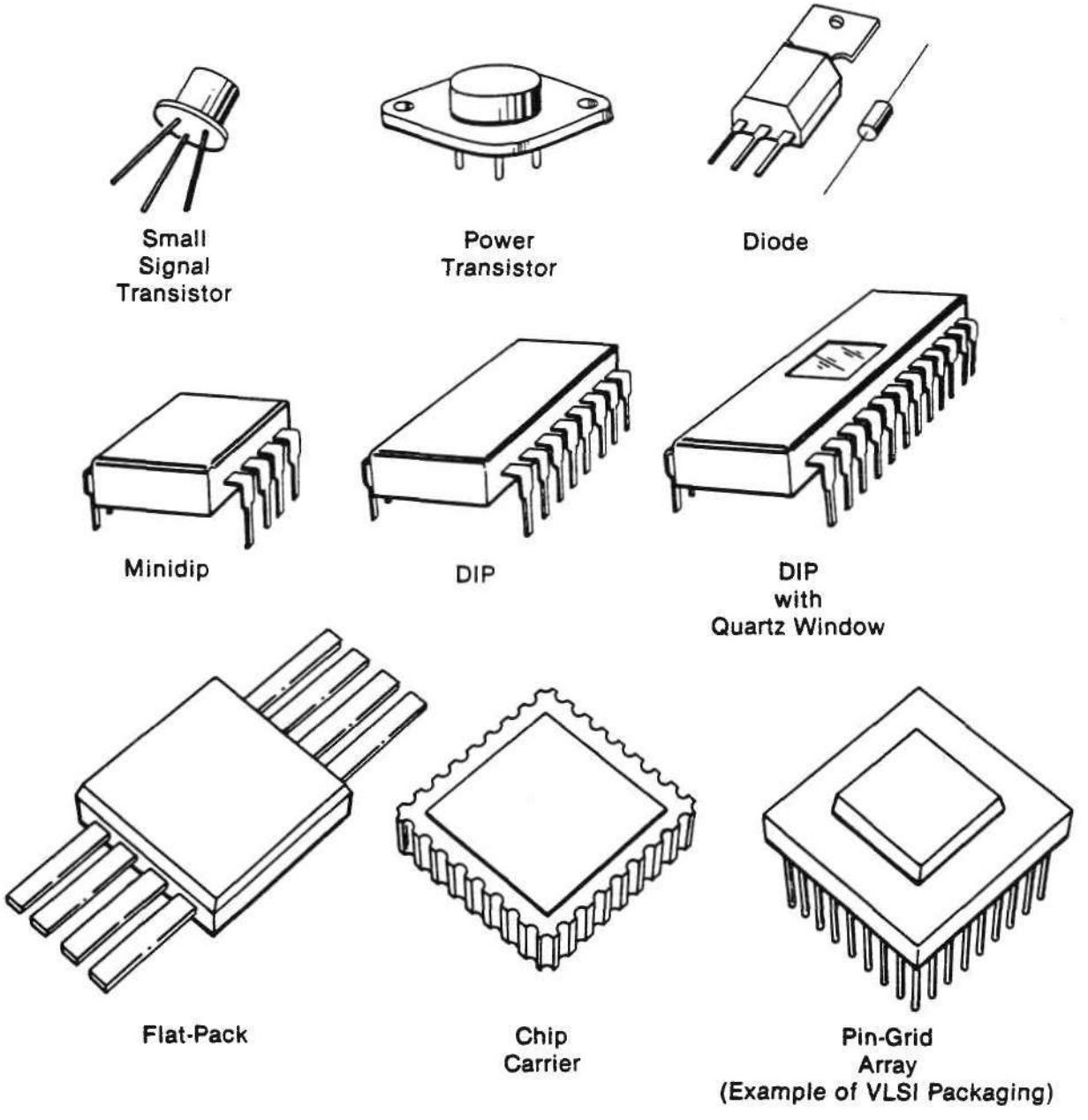
SEMICONDUCTOR PACKAGING

If semiconductor devices are to be useful and to function under varying conditions, they must be properly packaged. Packaging offers protection from external and environmental conditions and provides a convenient means of handling. To be useful, proper packaging must minimize the requirements for special tooling. The design of the package depends upon the intended use of the device. Simple packages may be used for equipment intended to operate in normal settings such as a laboratory or home. More complex, rugged packages must be used for hostile environments such as a steel mill, oil well applications, or space exploration. Figure 10-1 shows some of the package types currently in use.

10. Product Factors

Figure 10-1

SEMICONDUCTOR PACKAGE TYPES



Source: DATAQUEST, Inc.
April 1982

10. Product Factors

Although some semiconductor devices are still assembled by hand, development activities aimed at automating the assembly process have resulted in high volume packaging at greatly reduced costs. Continued cost improvements in semiconductor and integrated circuit devices will require additional automatic assembly and test technology. DATAQUEST expects the efforts to automate the assembly and packaging processes to continue, with increasing success.

The semiconductor manufacturer must consider the characteristics of mechanical design, hermetic seal, stress, and similar factors as part of the device development process. The general considerations fall under the areas of:

- Electromechanical requirements
- Attachment techniques
- Package materials

Electromechanical Requirements

Semiconductor packages must carry current between the external elements and the device terminals and provide suitable isolation between the current leads. The package should not degrade the operation of the device by adding additional parasitic elements to the electronic circuit. Electrical design factors such as circuit speed, current-carrying capability, and series impedance must be considered.

The package must be strong enough to withstand the handling stresses of device and circuit assembly. The designer must consider bending of leads, dropping, soldering, and so forth, as well as temperature, pressure, and other environmental ambient extremes. The package must protect the circuit from these extremes. The configuration of the package for handling, layout, and system assembly must also be carefully reviewed.

Since the devices generate large amounts of heat, the package must provide a heat path from the device to the outside environment. Without a good thermal path, the chip can easily exceed the maximum allowable operating temperature. The package must therefore be constructed of materials with good thermal conductivity for efficient heat removal.

Attachment Techniques

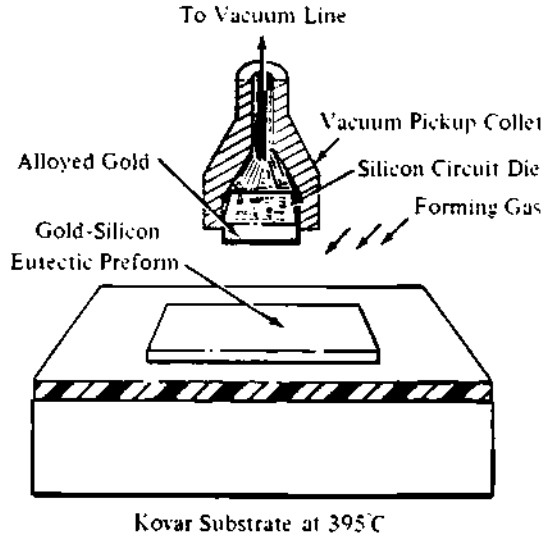
Silicon chips or dice may be mounted in the package by alloying, soldering, or brazing, as well as by the use of cement. If electrical insulation is required, as in high-frequency circuits, the chip is mounted on metallized islands on an insulator adapted to fit into the package. Figure 10-2 illustrates a basic alloy die attach operation.

10. Product Factors

Package metals and metallized islands are usually made of metals that have mechanical expansion coefficients matching that of silicon. Eutectic alloying preforms are used so that the alloying temperature, which is necessary to secure the chip to the package, is lower than the temperature used in making the chip. This method is used to prevent shorting the chip by re-alloying the contacts or other problems. In most cases, gold doped with a trace of germanium or silicon (to slightly lower its solubility in the silicon chip at the alloying temperature) is used for a preform.

Figure 10-2

BASIC DIE ALLOY ATTACH OPERATIONS

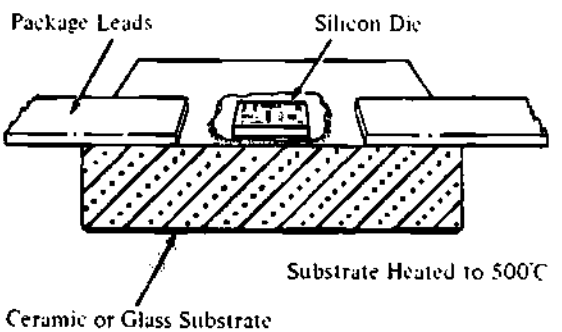


Source: DATAQUEST, Inc.
April 1982

Circuit dice may also be attached to ceramic or glass packages with a low temperature glass frit as shown in Figure 10-3. This packaging technique can be used because the back of the integrated circuit die is generally not used for electrical connections. The electrical connections are brought to the chip through the package leads, which were brazed to the ceramic substrate in an earlier operation.

Figure 10-3

DIE ATTACH USING LOW TEMPERATURE GLASS FRIT



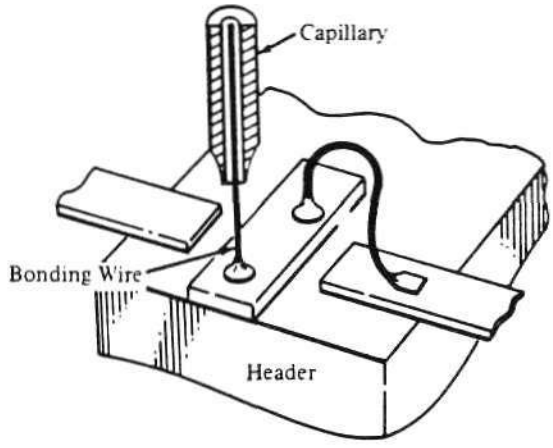
Source: DATAQUEST, Inc.
April 1982

10. Product Factors

After the integrated circuit die has been attached to the package, it is necessary to make electrical connections between ohmic-contact areas of the circuit and package leads. The most commonly used method consists of attaching extremely fine wires to the various areas to be interconnected, by thermocompression bonding. This process requires the simultaneous application of heat and stress, leading to the deformation of at least one of the members being joined. A variety of bonding machines, including the so-called wedge bonders, nail head or ball bonders, and stitch bonders, have been developed to accomplish thermocompression bonding. Although ball bonding, illustrated in Figure 10-4, requires individual attachment of the bonding wire to each contact pad, it is currently the most commonly used technique because of its reliability and bond strength.

Figure 10-4

GOLD BALL BONDING



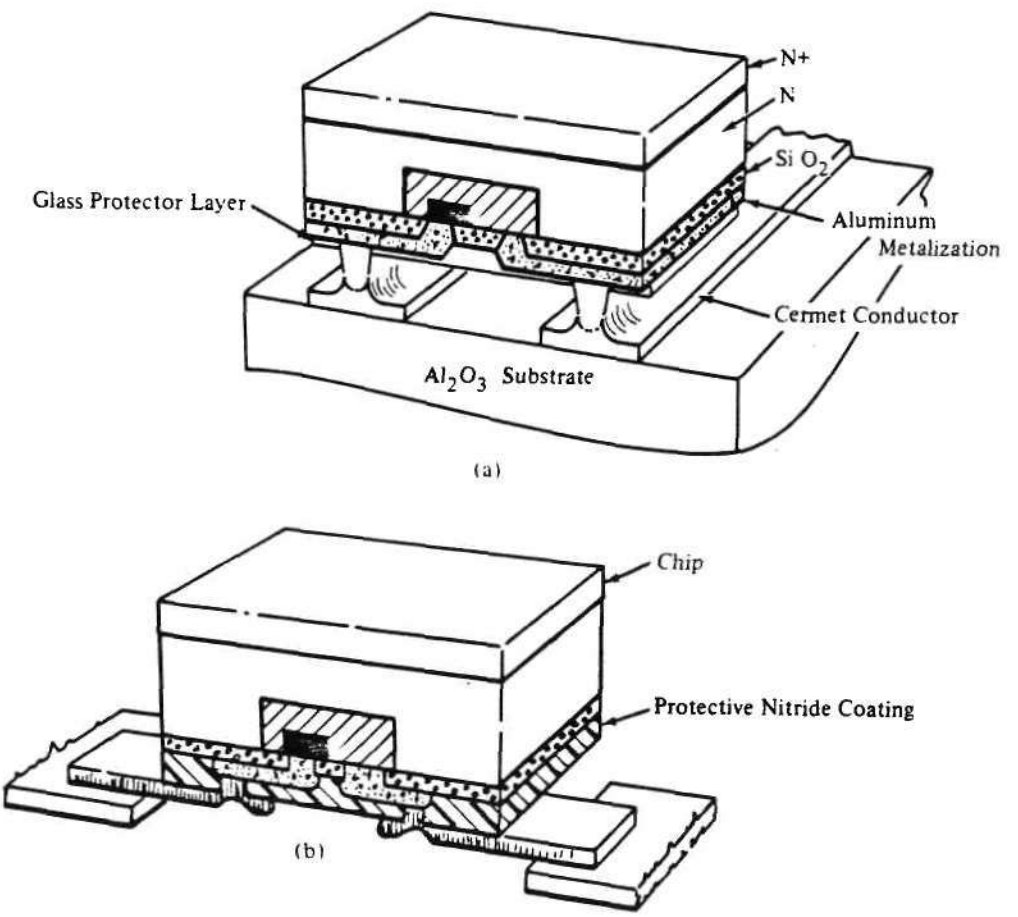
Source: DATAQUEST, Inc.
April 1982

10. Product Factors

Two alternate approaches for lead connection and die attaching are illustrated in Figure 10-5. The first of these, flip chip attachment, has been extensively used by IBM in its Solid-Logic-Technology (SLT). It employs plated solder bumps to connect to small raised lands on a ceramic substrate. The chief disadvantage of this approach is the extreme care that must be used during die placement to solidly connect to the circuit or device chip. A second "upside down approach" was developed in the mid-1960s by Bell Telephone Laboratories, and is also illustrated in

Figure 10-5

FLIP-CHIP ATTACHMENT METHODS



Source: DATAQUEST, Inc.
April 1982

Figure 10-5. Beam lead attachment is used for some integrated circuits in defense applications, but has not been extensively employed elsewhere. The chief disadvantage of this type of attachment is the large silicon area that is required for the extended plated-gold beams. This large silicon area detracts from the useful device area and increases the cost of the die by increasing the number of wafers that must be processed.

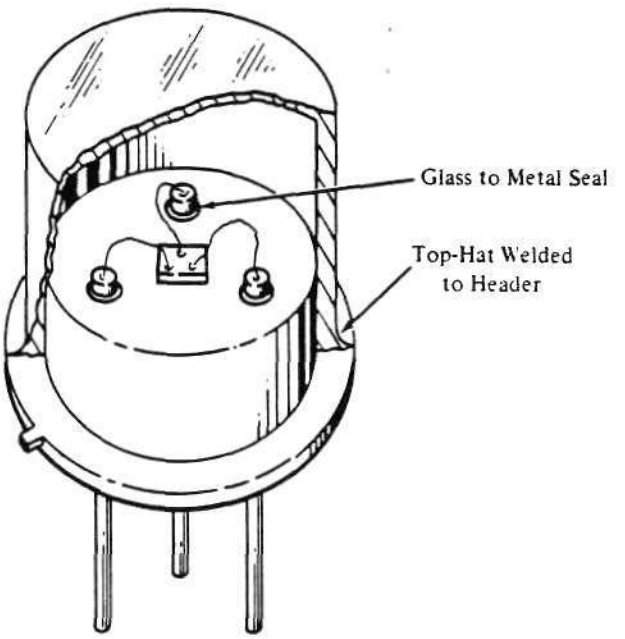
In the past few years extensive work has been done on eliminating wire bonding and lowering assembly costs. The most successful to date is based on the "mini-mod" process originally developed by General Electric. In this process raised bumps are placed on the contact pads in a second metallization process. The lead frame for the circuit is fabricated on a piece of Kapton film, which is slightly transparent. In the process, the yield loss due to improper die placement is reduced because the operator can see through the lead frame carrier. Once the mini leads are attached to the circuit, the circuit and frame are encapsulated in a plastic resin. Extremely high production rates may be achieved by this technique in the future. Rates in excess of 2,000 units per hour, per operator, have been accomplished. These rates compare favorably with the 100 to 200 units per hour for conventional chip and wire bond technology.

Package Materials

Transistor technology caused a revision in electronic component packaging. Earlier active devices, such as vacuum tubes, were encapsulated in glass or metal-cased vacuum evacuated tubes. The small size and simplicity of the transistor necessitated the development of a new packaging concept that would be compatible with the device. One approach to transistor packaging, which was finally standardized, uses a series of "cans." As shown in Figure 10-6, these cans use a header, through which the leads protrude, and a "top hat" shaped cover. After the chip and bond wires are attached, the cover is welded to the header in an inert atmosphere chamber. The glassed metal assures the hermeticity of the package where the leads protrude through the header.

Figure 10-6

TO CAN

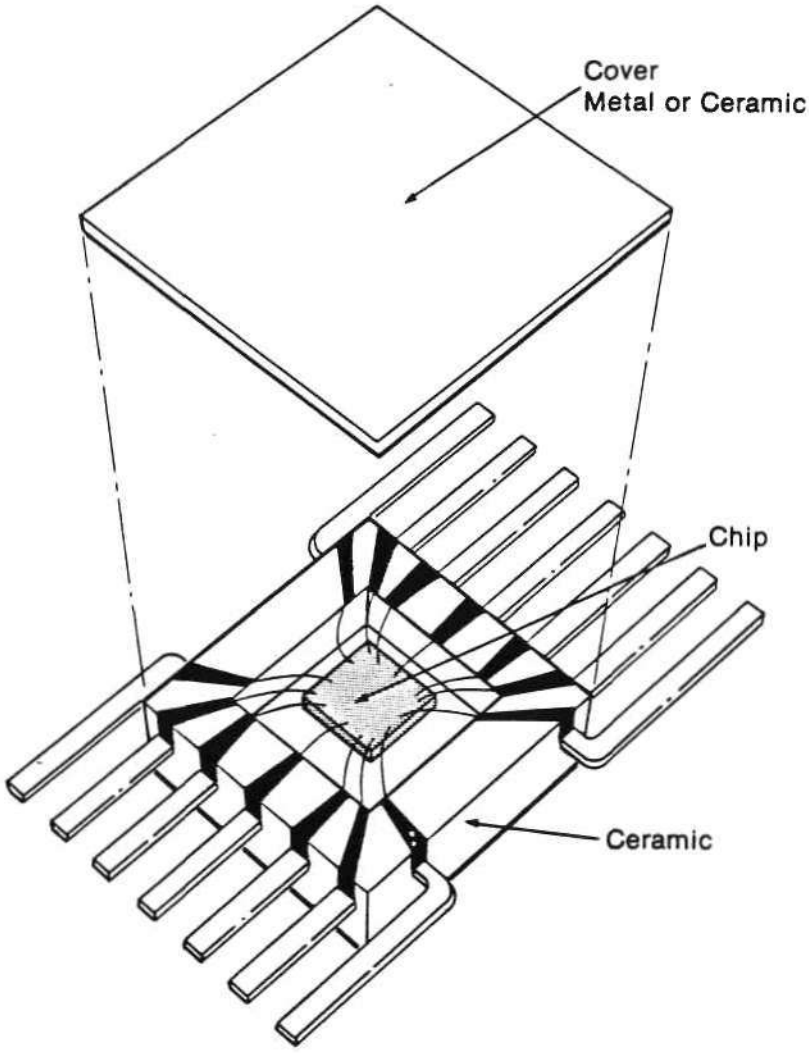


Source: DATAQUEST, Inc.
April 1982

Whereas the cans were designed as a container for transistors and later adapted to integrated circuits, the flat pack was specifically designed as a container for ICs. To minimize the wasted volume of the cans, the flat pack was designed to conform as closely as possible to the geometry of the "chip" that it was to contain. This was accomplished by passing the leads through the walls of the package rather than through the case, as with the cans. Passing the leads through the side of the package offered several advantages. First, projecting the leads from the sides of the package is more compatible with planar packaging systems. Second, by using the walls, more leads can be brought through the package for a given size and still retain reasonable spacing between them. There are many types of flat pack manufacturing technologies. The initial packages were based on the glass to metal seal technology of the cans. Later packages have been manufactured using ceramic to metal brazing processes and ceramic sandwiching processes. The ceramic sandwich process has proven to be the strongest package and the least expensive to produce. Figure 10-7 shows an example of a flat-pak.

Figure 10-7

FLAT-PAK



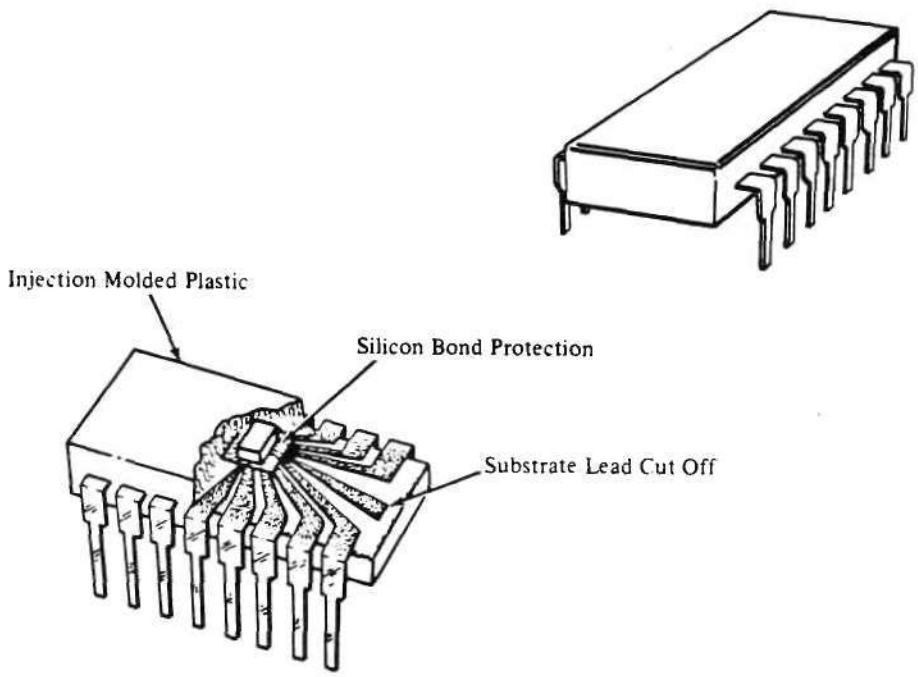
Source: DATAQUEST, Inc.
April 1982

10. Product Factors

The most commonly used integrated circuit package is the dual-in-line package (DIP). (See Figure 10-8.) This package was designed primarily to overcome the difficulty encountered when handling packages and inserting them into mounting boards. The DIP package is easily inserted either by hand or by machine. It requires no spreaders, spacers, insulators, or lead forming. A plastic DIP package is finding wide use in commercial applications, whereas a number of military and computer systems use a ceramic form.

Figure 10-8

DUAL IN-LINE PACKAGE (DIP)



Source: DATAQUEST, Inc.
April 1982

10. Product Factors

The most cost-effective packaging technology developed to date has been the variety of plastic packaging techniques using epoxy, phenolic, and silicon. These packages employ a stamped or etched lead frame of relatively thick metal onto which the chip is attached and the leads bonded. The assembly is subsequently run through a plastic molding process employing specific temperature and pressure conditions. Such devices are usually specified for use over limited temperature ranges, in commercial applications.

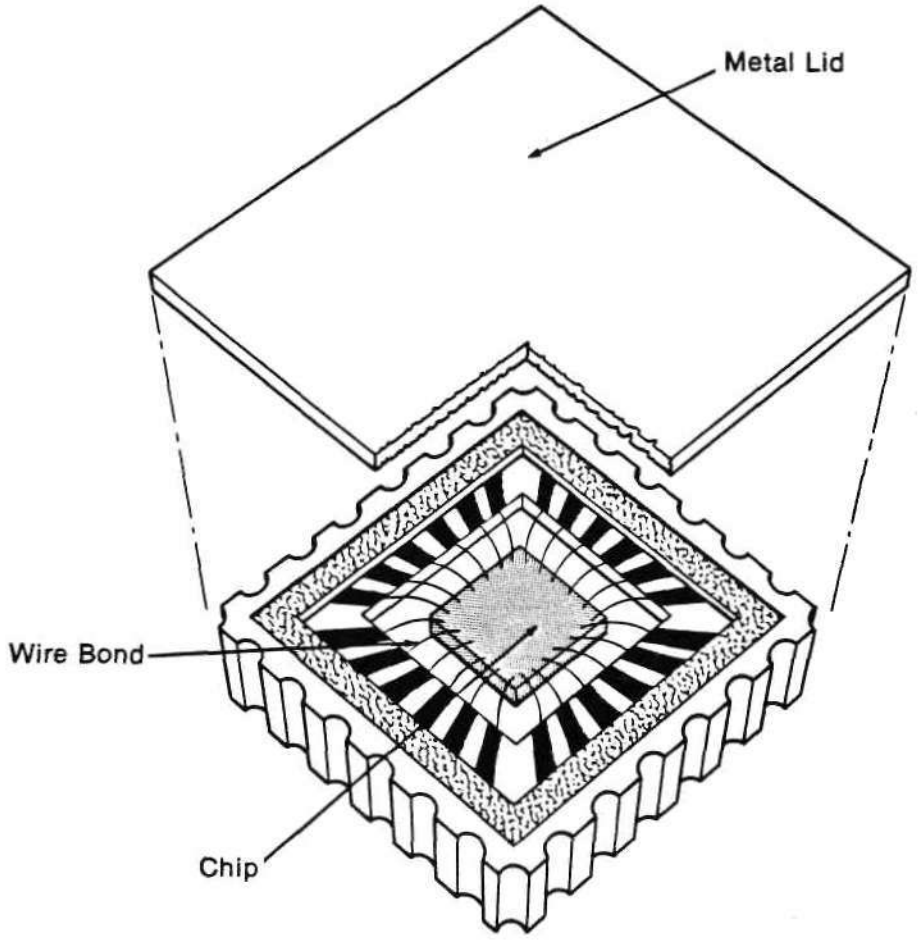
Although a great deal of reliability testing has been done on plastic packages, controversy surrounds their use. Some users have resisted efforts to allow wide use of plastic encapsulated devices in their equipment. One of the primary reasons for their reluctance is the belief that the plastic may not provide the necessary hermeticity for high-performance applications. The most serious problem with plastic devices is their inability to make an effective seal at the lead-plastic interface. This failing allows moisture to penetrate the device at the interface and corrodes the metallization, which causes conversion layer leakage on the chip.

Leadless Chip Carriers

As a means of increasing density in the next generation of hardware, many users are considering using leadless chip carrier (LCC) packaged semiconductors to replace DIPs. Major semiconductor suppliers are producing products based on this packaging approach. Costs are expected to decline as the industry gains experience in this technology. A leadless chip carrier is shown in Figure 10-9.

Figure 10-9

LEADLESS CHIP CARRIER



Source: DATAQUEST, Inc.
April 1982

10. Product Factors

VLSI Packaging

The advent of VLSI has outpaced semiconductor packaging technology. One of the reasons for this situation is that the earliest VLSI devices were memory devices that were accommodated by existing 16-, 18-, 22-, 24-, and 28-pin dual in-line packages. However, the advent of gate arrays with higher pin-counts has dictated the need for provision of pin arrangements in excess of 40 pins per package. The most judicious partitioning of VLSI circuitry dictates that pin counts on the order of 80 to 100 pins would be useful for the next several years. It is possible that the need for replacing entire printed circuit boards with monolithic VLSI chips can demand pin counts even greater than 100 pins.

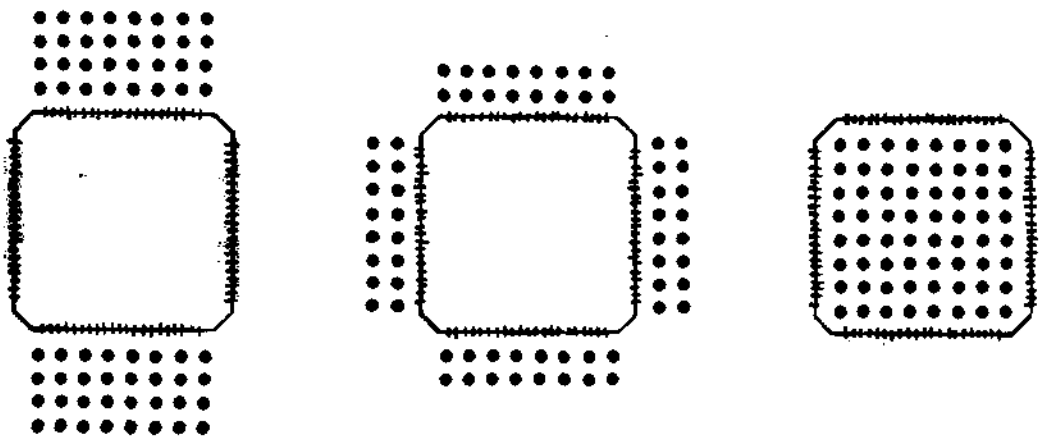
Evolutionary changes in the dual in-line package have led to packages with pins on 50-mil centers as compared to the long standing standard dual in-line package (DIP) with pins on 100-mil centers. A significant amount of activity is under way at present, which may lead to an industry-wide trend in surface-mounting techniques. For VLSI packaging, at least three pinout approaches are being considered for future standards.

- High-density packing—alternating lead positions on opposite sides of the package
- Peripheral fan-out—having leads positioned on four sides of a rectangular package
- The bed-of-nails or solid fan-out—having the leads extend perpendicular to the plane of the chip in a grid format under the entire area of the package

Figure 10-10 gives an example of each of the above approaches for packaging a 64-pin function.

Figure 10-10

VLSI PACKAGING METHODS



Alternating Lead Positions | Peripheral Fanout | Bed-of-Nails (Solid Fanout)

Of the three approaches, the bed of nails provides the highest packing density at the board level.

Source: DATAQUEST, Inc.
April 1982

10. Product Factors

Important items for the semiconductor user to consider when purchasing VLSI products that incorporate new package technology are:

- Impact on manufacturing methods
- Impact on incoming inspection equipment
- Impact on equipment maintenance procedures and technology
- Impact on supplier second-sourcing relationships
- Impact on overall logistics costs

Military Semiconductor Packaging Considerations

Most military applications involve operating equipment over a wide range of environmental conditions. In the commercial world, only automotive applications and civil aircraft applications place similar demands on suppliers. Typical military requirements are temperature ranges of -55°C to +125°C, with storage temperatures that exceed both ends of this range. The standard military voltage range requirements are for 10 percent tolerances on power supplies, whereas commercial tolerances are usually 5 percent. Other military environmental considerations include a wide range of atmospheric pressure, shock, vibration, moisture, and corrosion conditions, and extreme exposure to radiation in some environments.

Environmental Factors

With the possible exceptions of automotive and civil aircraft applications, military environments are the most severe conditions encountered by semiconductors. Vibration, corrosion, and radiation constraints dictate the necessity for special metals in the package body. Some examples of MIL-S-19500 screening requirements that illustrate the severity of military environments are:

- 20,000G minimum constant acceleration
- Five shocks of 1,500G minimum (0.5 ms rise time) in each of two perpendicular planes
- 30 second vibration at 60 plus or minus 30 cycles per second 0.1 inch minimum displacement
- Maximum leakage rate of 5×10^{-8} atmosphere per cubic centimeter per second
- 48 hours minimum at 150°C minimum, with reverse bias voltage applied

10. Product Factors

Military devices are required to function properly after exposure to the above mentioned conditions whenever MIL-S-19500 is specified.

Effects of the VHSIC Program

Two approaches to VHSIC packaging are under consideration by program participants. One approach is to innovate, adding new designs that resolve the problems inherent in current techniques. This approach is being followed by companies such as Honeywell, IBM, Texas Instruments, and 3M. Other companies are pressing existing packaging technology to its limits. These companies include the Motorola-TRW team, Hughes, and Westinghouse. Packaging techniques under consideration are chip carriers and flatpacks having leads on 25-mil centers, and a 200-lead chip carrier in conjunction with a 50-mil grid printed circuit board having 3-mil lines and spaces.

Quality and Reliability

The world of semiconductors is experiencing greater technical complexity, proliferation of part types, and tremendous growth in production volumes. There is a corresponding increase in the demands for product quality and reliability assurance. At present, quality control procedures are founded on sound business principles and well-established mathematical tools and techniques. There is also a greater reliance on sampling plans to reduce inspection costs without sacrificing quality protection.

There is a growing need for long-term reliability of semiconductor products. As humans rely more on semiconductors to provide improved quality of life, safety, security, and even survival in a sometimes hostile environment, the need for enhanced reliability grows more critical.

Quality Assurance

As defined in the glossary, quality refers to initial acceptability of a product for an intended use, whereas reliability refers to the expected ability of a product to perform its intended function over its expected lifetime. The user should be aware of the distinction between quality control and quality assurance. Quality control usually occurs after the fact; that is, a control mechanism is used to gate or to stop the movement of products, depending on whether their quality is acceptable. On the other hand, quality assurance extends all the way back to design concept. No amount of quality control in itself will correct a design deficiency. Thus, for a quality program to be effective, appropriate feedback must be provided so that the results of the quality control mechanisms can be used to assure higher quality in the future.

10. Product Factors

There are three major methods available for the inspection and testing of semiconductors during production. These are: 100 percent screen testing, sample testing on a lot-by-lot basis, and process inspection. All three methods are extremely valuable and cost-effective if applied with the following considerations in mind:

- A 100 percent screening or inspection program does not guarantee 100 percent acceptable results. Human beings are involved in the screening process, and the monotony of 100 percent screening often results in fatigue and reduced attention. While robotics are being applied to reduce this probability, it is important to remember that the robots themselves are designed by human beings and humans are, again, capable of error.

- Some product features cannot be 100 percent tested. For example, the fuse links in a programmable read-only-memory device (PROM) obviously cannot be 100 percent tested prior to shipment without destroying the product. This demonstrates the need for statistical screening methods.

Statistical screening procedures are founded upon the branch of mathematics known as probability theory. When using probability theory to assess a situation and applying sampling techniques as a tool, the risk of error is always inherent. Figure 10-11 shows two possible types of errors that may occur when applying any sampling plan. First, consider the situation where a given lot being sample-tested is good, and as a result of sampling error, management chooses to reject the lot. This situation is defined as a Type 1 error and results in increased cost of goods reaching the production floor. In the situation where the lot is bad but management chooses to accept the lot due to sampling error, a Type 2 error occurs. This can be a more serious situation than that created by a Type 1 error, because faulty products are incorporated into a higher level of assembly before it is detected.

Process inspection, referred to as source inspection, goes beyond the lot by lot inspection when performed by the user or sample testing method described previously. The process inspector is concerned with all the possible causes of defective work prior to and including final testing. This inspection identifies defective equipment, operations, raw materials, operator procedures, and other causes of defective products when and where they occur. One of the limitations of process inspection is that it is uneconomical and often impossible to have inspectors located at all points in the process at all times. As a result, discoveries by the inspector may not occur until after considerable damage has been done.

For many years, semiconductor manufacturers have used control chart techniques to provide quick feedback regarding process defects. An effective control chart system simplifies the quality control task and reduces the inspector's need for mathematical expertise. The most frequently used format for a control chart is a graph of the parameter to be controlled (vertical axis) versus time (horizontal axis).

10. Product Factors

Figure 10-11

RESULTS OF ACTIONS TAKEN AFTER SAMPLING

Action Taken:	PRODUCTION SITUATION: The Lot is Good	The Lot is Bad
Lot is Accepted	Action is Correct	Type 2 Error
Lot is Rejected	Type 1 Error	Action is Correct

Source: DATAQUEST, Inc.
April 1982

Acceptable Quality Level (AQL)

Acceptable quality level (AQL) is usually expressed as a percentage and denotes the maximum percentage of rejects acceptable at incoming inspection. It is the most commonly used method of defining commercial semiconductor product quality. AQL means the poorest level of quality acceptable as a process average for the purposes of acceptance sampling. Since it is a statistical term, AQL does not imply that there are no unacceptable lots shipped (or received) at 100 percent certainty. AQL is a constraint used in the judicial act of inspection and is not itself a specification.

At any time when inspection sampling techniques are used, it is important to establish AQL limits. When a lot is rejected as the result of sampling, and it is economically feasible to rescreen the lot, a second screening may be performed to sort the defective devices. If the rescreened lots with defects removed are now combined with the imperfect lots, the total percentage of defective parts that finally pass will not exceed the AQL. This procedure is referred to as average

outgoing quality limit protection, and may be used by suppliers as an outgoing inspection technique or by users as an incoming inspection technique for quality control. Some semiconductor suppliers now ship to stated AQL limits. The present practice of those suppliers is to state a limit at or below 0.3 percent AQL, with some products being shipped to 0.1 percent AQL.

For military applications, the United States Department of Defense established two documents for use in quality control, MIL-STD-105 and MIL-STD-414. MIL-STD-414 was developed to reduce the cost of inspection through the use of smaller sample sizes. In the early 1970s the British government published Def. Std. 05-30/1, based on MIL-STD-414, for use in military applications. Def. Std. 05-30/1 includes a review of relevant statistical theory and a discussion of tests for detecting departure from normality.

Many commercial semiconductor product users prefer to do no incoming acceptance testing, and rely on the suppliers to provide appropriate screening. These users accept the added risk that a small but finite percentage of the products used may be defective, increasing the user's manufacturing cost. The user must compare the total cost (including downtime) of repairing assembled equipment against the cost of sample testing incoming lots as a part of the decision analysis.

As an example, consider a small desktop terminal containing eight 16K RAMs and a large computer with a 20 MB mainframe memory. Troubleshooting at the system level may cost less than $0.50 for replacement of a single RAM in the terminal, but may be greater than $100 for replacement of a RAM device in the large mainframe. The higher mainframe repair cost may justify component incoming inspection, whereas such inspection may not be justifiable for the terminal.

The user should be aware of the cost implications of sample testing and of the demands that are placed by AQL limits. In this sense, quality is not free but rather quality is the result of application of feedback, at some cost, to reduce human error. The trend toward automation and the increased use of robotics in implementing semiconductor manufacturing lines will inevitably lead to higher levels of quality in semiconductor production. The need for close relationships between suppliers and users is becoming correspondingly greater.

RELIABILITY

Equipment reliability is an essential part of human existence. Requirements for reliable semiconductors have become an increasingly larger percentage of this total reliability need, as the applications for semiconductors have multiplied.

Reliability is usually measured in terms of mean time between failures (MTBF). The MTBF of silicon semiconductors is on the order of millions of hours at 25°C, and must be derated for operation at higher temperatures. The derating factor varies by process and by device type, and it may be as high as a factor of two for each ten degrees of ambient temperature variation.

10. Product Factors

Reliability engineers have defined three types of failures:

- Infant mortality (early failures)
- Random failures (chance)
- End of life failures (wear-out)

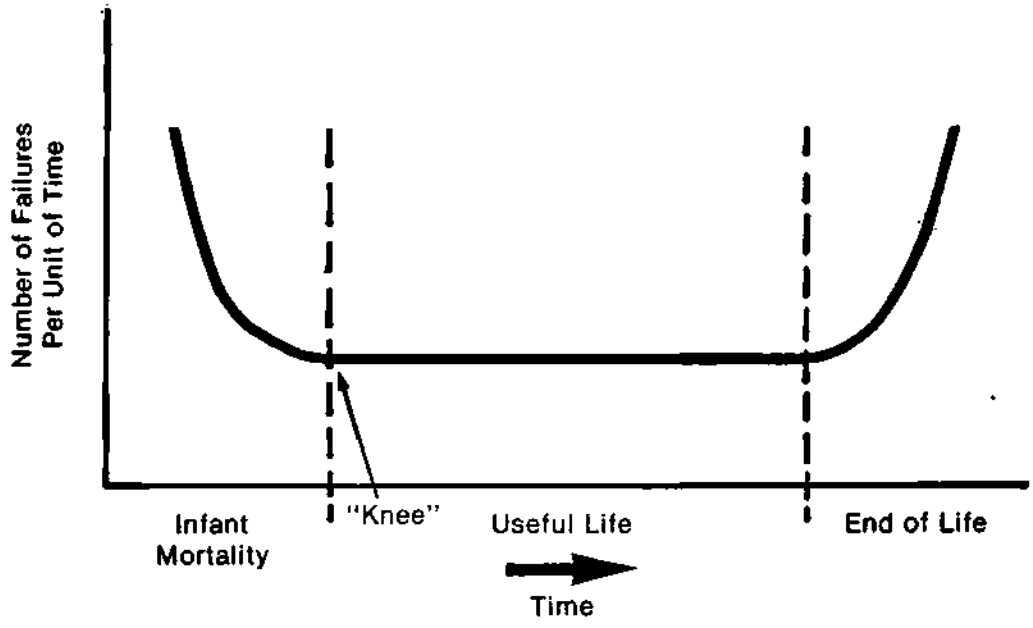
Figure 10-12 illustrates the occurrence of these types of failures. As the figure shows, the transition from infant mortality to random failures is often referred to as the "knee" of the reliability curve. In silicon semiconductors this knee frequently occurs within the range of the first 100 to 160 hours of operation at 125°C. This is the reason for performing device burn-in when it can be economically justified.

The so-called random failures or chance failures that occur during the normal life of many devices can result from a number of causes. These causes may include one or more of the following, depending on the particular semiconductor design and manufacturing procedure:

- Metal open
- Metal short
- Oxide pinhole
- Overstress during testing
- Bonding failure
- Loose particles in package cavity
- Transistor breakdown

Figure 10-12

MORTALITY CURVE FOR SEMICONDUCTOR DEVICES



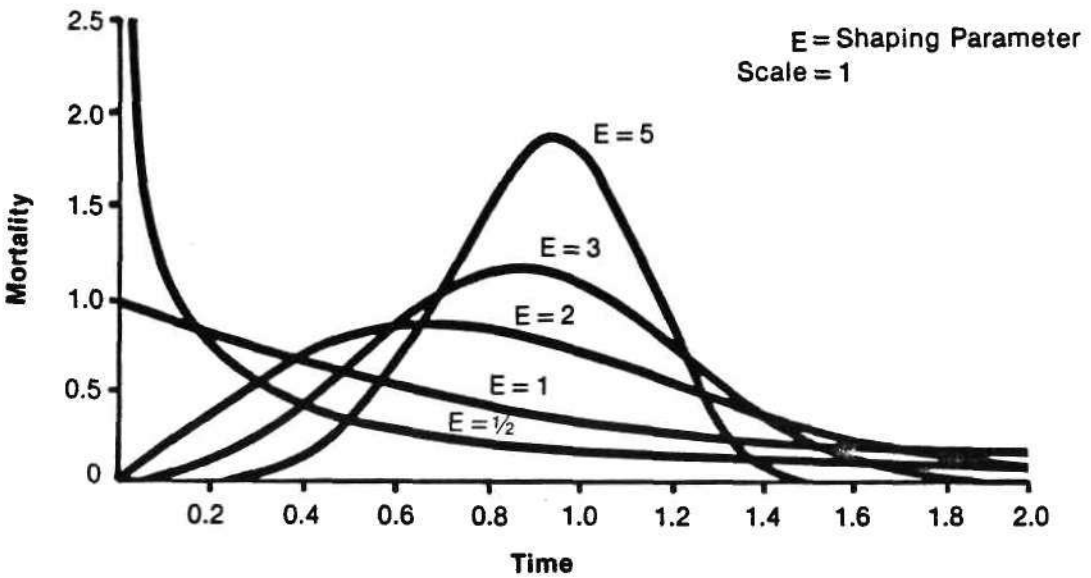
Source: DATAQUEST, Inc.
April 1982

10. Product Factors

During the early years of semiconductor technology, analysis of random or chance failures was often based on the assumption that a constant failure rate exists throughout the mature life of the product. Experience has proven this to be a poor assumption. In recent years a sophisticated mathematical technique has evolved for describing failure patterns other than constant failure rates. This technique makes use of a curve or plot known as the Weibull distribution. In addition to the statistical parameters of mean and standard deviation, the Weibull distribution uses three additional parameters referred to as the "shape," the "scale," and the "location." Figure 10-13 illustrates the Weibull function, relating the values

Figure 10-13

WEIBULL MORTALITY RATES



Source: DATAQUEST, Inc.
April 1982

of the three parameters. Semiconductor users who need maximum reliability regardless of cost should consider the application of Weibull function analysis techniques as a part of an exhaustive reliability study of failure frequencies and distributions.

End of life (EOL) or fatigue failures exist in semiconductors just as in any other physical devices. However, it is not unusual for the expected life of many types of semiconductors to be measured in thousands of years under certain reasonable conditions. Examples of EOL failures in semiconductors include metal migration (or creep), causing a conductor to become a resistor, and the loss of memory in an EPROM, resulting from very slow leakage or from radiation.

Semiconductor suppliers and users have continually devised tests to determine semiconductor reliability. These are usually referred to as accelerated life tests and are, by definition, destructive. Very high voltage and temperature combinations are used to compress the time of the occurrence of random failures and end of life failures. The results of many such tests have been empirically related to experience at lower combinations of temperature and voltage, and the results of the comparisons give an indication of the expected life of the semiconductors. The U.S. government has a military standard referred to as MIL-STD-883, which describes in detail such reliability testing methods.

Other forms of reliability tests are used to eliminate or reduce the possibility of shipping lots containing infant mortality candidates. These tests are often referred to as burn-in tests and may be performed by a semiconductor supplier, the semiconductor user, an independent test house, or by a combination of two of the three. The purpose of such tests is to assure that the semiconductors have accumulated experience beyond the point at which the knee of the curve of Figure 10-12 occurs. As stated earlier, burn-in of 100 to 160 hours at 125°C accomplishes this procedure for silicon semiconductors.

Using an independent test house offers advantages such as reduced investment in test equipment, but increases risk. The additional risk is due to at least two potential problems. First, the question of who pays for the reject—addition of a third party may make it more difficult to establish liability. Second, more parties handling the product increases the risk of introducing new quality or reliability problems through human error.

While no amount of reliability offers unconditional guarantees, there is much practical value to reliability information. For example, the semiconductor user's design and development functions should anticipate and account for the life expectancy and failure mechanisms of the components in use. This allows the user's organization to make appropriate maintenance provisions and to add sufficient repair capabilities. Reliability information also aids procurement in determining spare parts requirements.

Failure mechanism information is also useful from the standpoint of safety. For example, the automotive industry must make provisions for failures in

microprocessors and other semiconductors used in engine controls. Security systems must take into account failure mechanisms in all semiconductors they use if they are to be fail-safe.

There is a correlation between product reliability requirements and product costs. For example, it is not necessary to use relatively expensive military-rated devices with radiation hardening characteristics in a hand-held calculator or a personal computer.

In summary, the semiconductor product user has a vital interest in the level of quality and the expected reliability of the semiconductor products being purchased and applied. A shared responsibility for design engineering, development engineering, procurement, components engineering, incoming inspection, and materials management exists in the selection and application of semiconductor components. The best results will be obtained when the user and the selected suppliers work together on a continuing basis in specifying, providing, and controlling the required levels of quality and reliability.

COMPUTER AIDED DESIGN

The evolution of integrated circuits toward greater levels of complexity has been accompanied by an increase in component count from less than 100 in the early 1960s, to approximately one-half million in today's most complex circuits. There has been a corresponding evolution in approaches to design and design verification of these circuits. However, due to the extremely high cost of computer time during the 1960s, computer aided design (CAD) techniques were used very sparingly. As the cost of computing came down, CAD usage became more common. This usage usually resulted from a need to employ computer aids in a specific step of the design process, however, and it was not developed as part of an overall integrated system. At present, most CAD systems are comprised of a series of programs that require human intervention and data base manipulation to move from one step in the design process to the next.

The VLSI design process involves several complex steps. First, a manufacturing process must evolve that will provide for construction of the desired devices (such as transistors, capacitors, resistors, and diodes), which are to be integrated into a single monolithic chip. The CAD task at this point is one of modeling the characteristics of the various devices and identifying and accounting for the electrical interactions of these devices when they are in close proximity.

Once the device interactions are characterized and the manufacturing process is defined, CAD is then applied to the task of defining functional elements for use in complex circuit design. Examples of these designs are logic gates, flip flops, interface circuits, buffer circuits, drivers, programmable elements such as PROMs and EPROMs, and programming energy distribution networks. At this stage, CAD is used to perform worst-case analysis of the various circuit elements. It takes into

account all of the effects of stray parameters between components in the circuits. The worst-case analysis includes worst-case limits for the manufacturing process variations. Once the circuit building blocks are established, CAD may be used to address the problems of circuit layout, topology considerations, and interconnect routing on-chip.

PRODUCT STANDARDIZATION

Numerous forces influence suppliers to increase the level of product standardization of semiconductors. Some examples include:

- Second-source agreements—customer driven
- Second-source agreements—market driven
- JEDEC standardization activities

Second-Source Agreements

In many instances, customers require or strongly desire an uninterrupted supply of semiconductor products over the application lifetime. To influence supplier behavior positively in achieving this objective, a second-source clause might be written into the customer-supplier contract. Such a clause would specify the conditions and approximate time frame by which the prime supplier is expected, or required, to develop, or assist in developing, a second-source capability. Care must be exercised to avoid legal problems in such an agreement.

The second-source need may be met by redundancy built into any area or areas of the logistics as required. This redundancy may range widely, from an approach as simple as the use of distributor buffer stock, to a requirement that the backup source be an independent semiconductor manufacturer, isolated geographically and politically from the prime source. On custom and semicustom programs, care may be necessary to avoid having two or more suppliers dependent on the same subcontractor, or on a common source of raw materials such as wafers, chemicals, or package piece-parts.

An alternative to the contractual clause approach is for the customer to specify form, fit, and function requirements with respect to another supplier as a part of the purchase order for the product or products. In this approach, care must be taken to avoid misinterpretation of the requirements by the supplier, since product engineers almost never have cause to review purchase orders, much less interpret "fine print" and "legalese." An even greater concern may be the potential schedule delay caused by non-standard processing of the purchase order to include an engineering review. Supplier conformance, or ability and willingness to conform, to a second-source requirement should be established prior to issuing a purchase order.

10. Product Factors

Supplier-Driver Multiple Sourcing

It is often in the users' best interest to let market forces drive the multiple sourcing and standardization of semiconductor chip functions. This becomes even more important when a new package is involved, since manufacturing tooling hardware as well as software is almost always affected. It is not unusual for 10 to 25 suppliers to enter a marketplace once a new product starts to emerge. This almost always results in lower pricing over the product lifetime, because the industry experience of producing millions or billions of units is brought to bear, with resulting efficiencies of scale. Some classic examples of this experience effect are the TO-92 transistor case, the 16-pin DIP, the 16K and 64K dynamic RAMs, the integrated operational amplifier, and TTL logic. Market forces, with few exceptions, drive semiconductor technology to produce functions years ahead of what can be accomplished by a single customer's actions.

JEDEC Standardization Activities

The Joint Electron Device Engineering Council (JEDEC) was founded in 1941 as a joint activity between the Electronics Industries Association (EIA) and the National Electronics Manufacturers Association (NEMA), focused on electron tube standardization. Over the years it has evolved to its present concentration on solid state products. JEDEC Council members are appointed by the sponsoring associations or nominated by solid state product manufacturers who are JEDEC members. Technical competence is a prerequisite for JEDEC Council membership.

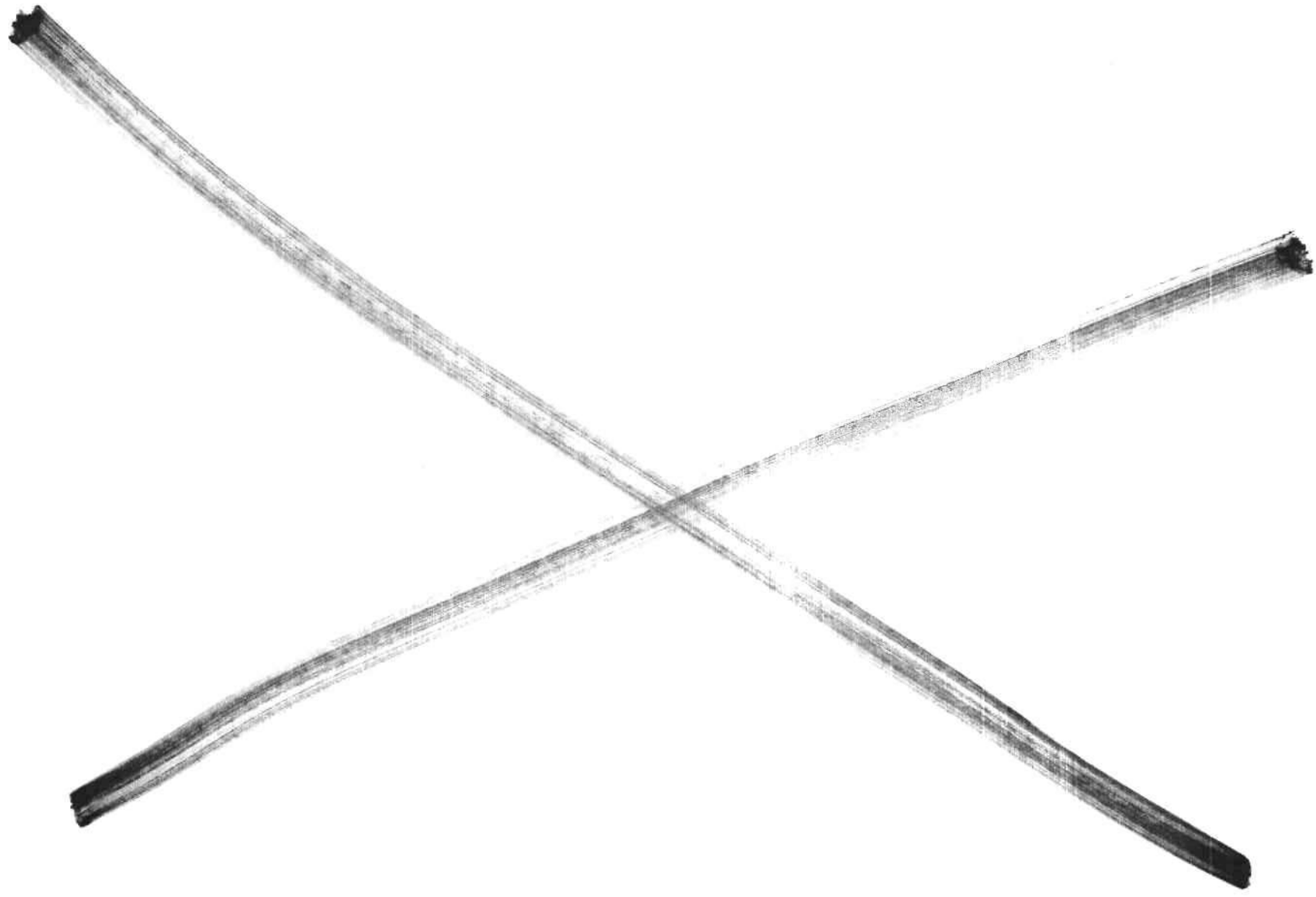
A number of product and service committees have been established to propose standards and formulate policies, procedures, and other documents for JEDEC Council action or approval. These committees include:

- Service Committees
  - JC-10 Committee on Terms and Definitions
  - JC-11 Committee on Mechanical Standardization
  - JC-12 Committee on International Standardization
  - JC-13 Committee on Government Liaison
  - JC-14 Committee on Non-Military Product Reliability
- Product Committees
  - JC-22 Committee on Diodes and Thyristors
  - JC-23 Committee on Optoelectronic Devices
  - JC-25 Committee on Transistors

10. Product Factors

- JC-30 Committee on Hybrid Microcircuits
- JC-40 Committee on Digital Integrated Circuits
- JC-41 Committee on Linear Integrated Circuits
- JC-42 Committee on Solid State Memories
- JC-43 Committee on Microprocessors and Microcomputers

Some examples of recent activities of JEDEC subcommittees include efforts involving dynamic RAMs, CMOS circuits, and leadless chip carriers. Such activities often are very influential in increasing the number of sources offering a particular semiconductor product or product family.



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The cost of producing state-of-the-art semiconductor products has continued to rise and has become increasingly capital intensive. Today even a prototype line capable of processing only a few thousand five-inch wafers a month costs in excess of $10 million to implement. Large semiconductor manufacturers may expend $50 million to $100 million over a two-to-three-year period to update or upgrade a wafer fabrication facility from four-inch to five-inch capacity. The make or buy decision for a small user of semiconductors who cannot justify such expenditures is clear-cut, and the decision becomes one of whether to buy custom, semi-custom, standard, or a combination of these three approaches to semiconductor implementation.

ADDING CAPTIVE CAPACITY

Approximately 65 captive semiconductor manufacturers are currently active. As a semiconductor user corporation grows to an annual sales level in the range of $500 million, the decision to buy 100 percent of the semiconductors the company uses may be reviewed. The company's long-range planning may already have allowed for in-house design of semiconductors. In any case, the decision of whether or not to add in-house fabrication capability becomes important. The decision to create or add captive semiconductor fabrication and manufacturing capacity requires initial expenditures in excess of $10 million.

The following two capacity models are intended to give guidelines to help in the collection of information to support making such a decision. The first model applies to the situation in which the user must decide whether to add a high-volume fabrication line capable of producing 5-micron N-channel MOS LSI products. The second model is useful in making a go, no-go decision regarding the addition of a lower efficiency, fast turn-around 2-micron CMOS LSI capability for use in such applications as gate arrays.

5-Micron NMOS Fab Facility Cost Model

This subsection addresses the schedule and cost requirements and related factors involved in the startup of an NMOS wafer fabrication facility. The semiconductor user should be aware that costs in addition to the ones described here are involved; e.g., those incurred in establishing assembly capability. This model is representative of mid-1980 startup costs and does not take into account inflation and other cost increases since that time.

Plant Construction, Design, and Layout

The construction phase of a semiconductor facility is an important and sensitive stage that generally requires almost eight months. Although this phase

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includes many conventional construction techniques, it is characterized by the many highly technical approaches peculiar to the semiconductor industry.

The model described calls for ten-foot high ceilings above the work area so that the laminar air flow required for the clean rooms will be efficient. Above the ceiling, but below the roof, a six-foot high space is specified. This space is an essential area for gas piping, ducting for air conditioning, pump location, and controls. Such an area, although expensive to construct, will guarantee the integrity of the fabrication area and allow maintenance personnel to avoid the actual manufacturing area.

Trenching, as a construction technique, does at a physically lower level what the extended space does above the ceiling. Trenching saves valuable manufacturing floor space by placing service corridors below ground. If the space is properly sealed, contamination of the fabrication area due to chemical leakage can be avoided. Trenching tends to avoid wall openings for pipes and control functions that otherwise would have required absolute seals around each opening. Floor drains (required for cleanup) and safety showers are also more easily installed and maintained with floor trenches.

Clean rooms are very expensive, and they require workmanship of the highest caliber. High energy particulate air (HEPA) filter coverage for the ceiling ranges from 35 to 90 percent in most installations. The requirement for an air plenum above the ceiling in addition to the weight of the filtration apparatus, adds an extra burden to the roof load of approximately 15 pounds per square foot. This requirement almost always exceeds the support capabilities of existing roofs and structural strengthening is required, increasing costs.

Provision for off-site chemical storage and supply installations is not only highly desirable but in most cases is a necessity. Better control of chemical usage and employee safety are guaranteed by this construction technique. Federal and state safety requirements for this kind of installation require not only isolation but also "catch-basin" arrangements beneath the storage tanks. In earthquake-prone areas, seismic studies dictate construction requirements. This model requires the installation of five acid tanks and two chemical tanks at a cost of $220,000. Although it is difficult to prove, DATAQUEST believes that the added cost of these tanks is recovered through better control of chemical usage and inventory, and through improved yields. The improved yields result because it is unnecessary for extra personnel to pass through the clean room to deliver chemicals. (Every time a worker enters a clean room, the dust particle count increases.) There is also less danger of chemical spillage when chemicals are piped in rather than being delivered in bottles.

The construction of support areas (i.e., non-fab), such as wafer sort and offices, conforms more to routine construction requirements and is much lower in cost. Standards exist for office sizes, ceilings, walls, and floors in most industries, and these standards are easily applied to this phase of construction.

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The heat and dust generating portions of the diffusion furnaces and ion implanter are sealed off by fire walls from the clean rooms and processing areas. Service corridors surround the Fab area so that stations using wet chemicals can be serviced from outside the controlled environment. This construction plan results in a lower heat load, better particulate control, and reduced traffic across the manufacturing floor.

Figure 11-1 shows schematically the movement of data and material during the manufacturing process. The production or manufacturing control center is the heart of the operation as shown in the area block diagram (Figure 11-2). There is a unidirectional, closed-loop relationship, for instance, among Production Control, Masking, and Etch. Production Control accesses all areas by means of "pass throughs" so that each area can maintain its integrity. Entry to the factory floor is through three stages: primary entrance, gowning room, and air shower. At each stage the worker becomes progressively cleaner.

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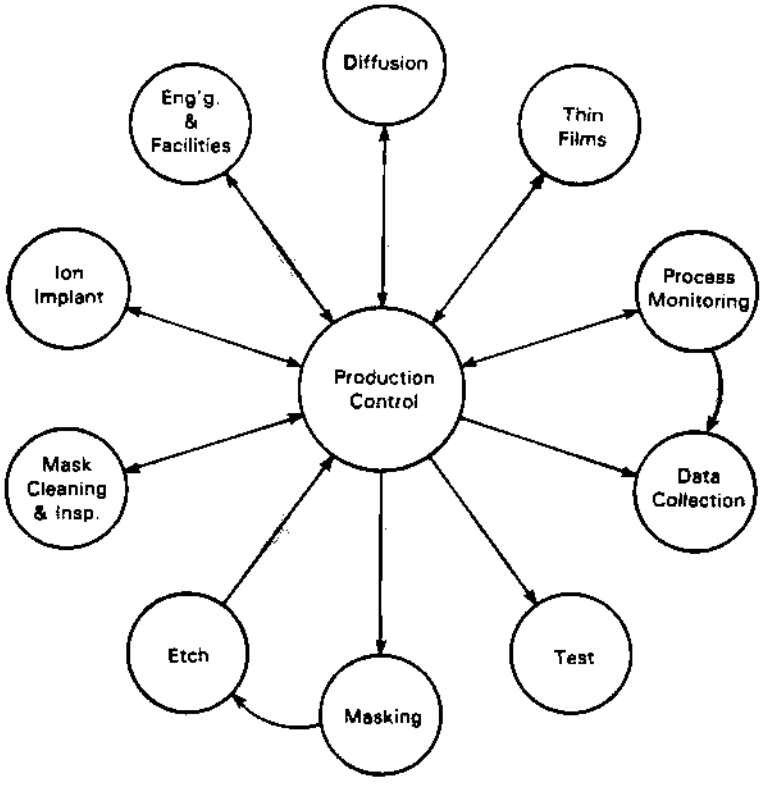
Figure 11-1

DATA AND MATERIAL FLOW



Source: DATAQUEST, Inc.
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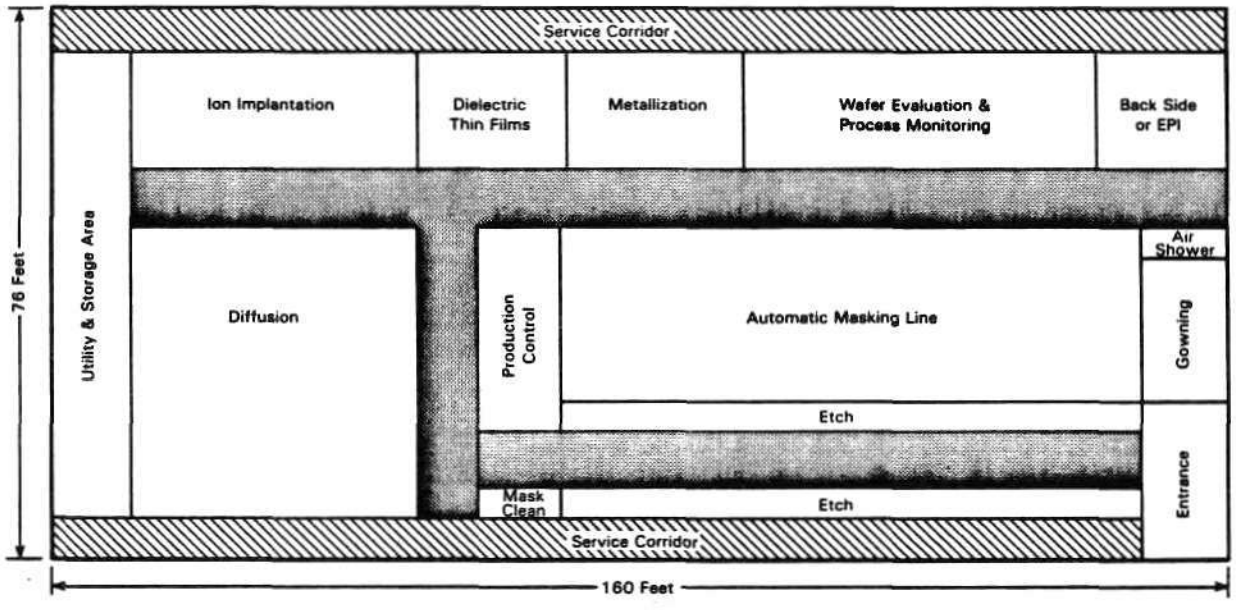
Figure 11-2

MANUFACTURING AREA BLOCK DIAGRAM



Source: DATAQUEST, Inc.
April 1982

The diffusion area is large enough to accommodate five banks of 4-stacker diffusion furnaces. This size will be useful if the model is to be adapted for 8-layer bipolar or 10-layer CMOS devices. Space allocated for the automatic masking line is enough for eight or more projection aligners. Amost 80 linear feet have been reserved for etch and inspection stations. The ion implantation and dielectric thin film areas are designed so that the dividing wall can be moved to accommodate the operation with the greater need.

The entrance to the fab area has been staged to conform with clean room requirements. Data collection has been removed from the manufacturing floor since computer record keeping and data processing still involve paper work that would be intolerable there.

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Cost Reductions

Loss of yield over the useful life of the fab area makes cost cutting in construction of a state-of-the-art facility an extremely delicate exercise ("penny wise and pound foolish").

As previously mentioned, the extended space between the fab ceiling and roof is expensive to construct. Instead of this approach, some plants simply install a maze of catwalks above the fab ceiling. However, this approach usually requires that maintenance crews enter this space from within the manufacturing area. The resulting contamination problems are severe even if maintenance is done during off-production periods. Catwalks usually accommodate the piping and ductwork and are not necessarily near the problem area. The entire Fab area is usually shut down to accommodate the maintenance exercise with resulting loss of revenue. The catwalk approach to construction also results in loss of positive pressure in the room below. Finally, this type of construction makes any attempt at expansion impossible without gross contamination in adjacent manufacturing operations.

This discussion of cost reduction possibilities is intended to alert the reader to the ramifications inherent in reducing expenses in high-technology manufacturing. With care, a diligent engineer can find many areas in which appreciable savings can be effected without downstream damage. In Facilities Engineering, as in Process Engineering, there is no such thing as a "small engineering change."

Nevertheless, construction expenses can be reduced or avoided without penalty in some areas. Chilled water storage, although desirable, is unnecessary as long as the chilled capacity is less than 500 tons. For capacities above this limit, however, chilled water storage becomes more attractive as energy costs accelerate. An 85 percent efficiency level should be achieved to justify this expense.

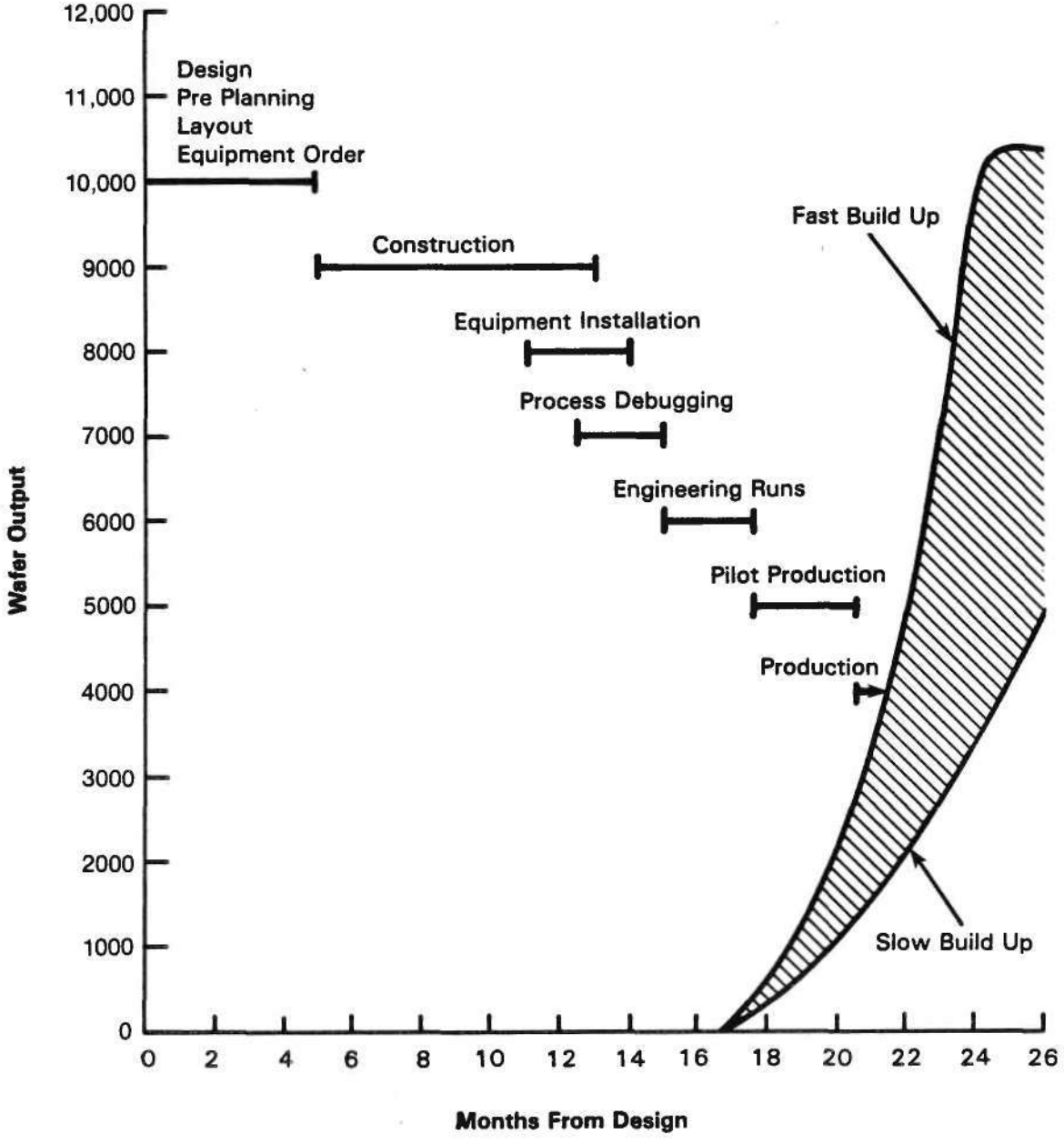
Time Requirements

Because of the special facility requirements of the semiconductor industry, it is usually more effective in the long run to construct a facility rather than to try to adapt an existing building. Prior to the construction phase, particular attention must be given to the design of the facility so that all special requirements are met. Attention must also be given to the time required to install support equipment, plumbing, air conditioners, and other hardware before the facility can be used. Adequate time for equipment to be ordered, manufactured, shipped, and installed must be allocated. Large equipment, such as that used for gas storage and deionizing water, requires additional lead time.

The time required to design, construct, debug, and build a facility ranges from 18 months to 2 years. Construction time is affected by such factors as strikes, material shortages, late deliveries, adverse weather, and changed orders due to imperfect planning. Figure 11-3 illustrates the time required for building a new manufacturing facility. If a new building is required, it can take up to 15 months (barring any serious disruptions) from the design stage before the initial engineering runs are processed through the area.

Figure 11-3

START UP TIME REQUIREMENTS



Source: DATAQUEST, Inc.
April 1982

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Time can be saved by moving into an existing facility, provided extensive modifications are not required. Very often, however, considerable tradeoffs have to be made, particularly regarding working space and material flow. For a new facility, the slowest area to reach production is almost always wafer fabrication and its processes. Test equipment and assembly equipment can usually be debugged and be on-line several weeks before the wafer fabrication processes. The time required to debug equipment and processes varies from company to company.

Most companies choose to install the latest and best manufacturing equipment in any new facility for two reasons:

- The equipment becomes obsolete so rapidly that it is not always economical to install older models, even though they are well-proven machines
- Most companies buy their IC equipment from the same vendors and, therefore, they all have the same basic manufacturing capability

The advantage, however slight, supposedly goes to the company getting the newest, best equipment into production first. More often than not, however, the latest models have operating problems that may take days or even months to resolve.

In the wafer fabrication area, there is close interaction among processes, process equipment, and yields. New equipment at a process step often forces redefinition or redevelopment of that process, sometimes causing it to be subtly different from the previous process. Manufacturers then find that the process has worse yields than previously. The subsequent questions raised are: (1) Is the problem one of equipment, process, or both? (2) Which process steps are involved? Considerable time may be required to answer these questions and to find an acceptable solution.

Wafer volume buildup is loosely tied to the availability of trained operators. Even experienced operators have to be retrained on new equipment, which lowers their productivity for days or weeks at a time. During the volume buildup, output per operator does not necessarily indicate true efficiency, since most of the effort goes into establishing the work-in-process inventory. Furthermore, operators are hired in advance of the actual growth of volume to allow for training.

Manufacturing Cost Analysis

For the model in this subsection a 6-layer process utilizing 4-inch wafers was chosen as the simplest way to fabricate a workable 16K DRAM device. In fact, many companies use an 8-layer process with an isoplanar structure and threshold shifting implantation. This necessitates the use of a silicon nitride deposition and the growth of a thick layer of oxide in the field regions of the device.

The assumptions we made in developing wafer and die costs are listed below. Companies were surveyed and the data analysed for certain cost elements. The standard deviations represent, for the most part, regional, management, and accounting differences. Equipment and facilities costs are also summarized. These

costs have shown a rapid increase in recent years due to the escalation of labor rates and the price inflation of metals (e.g., copper) and petroleum-based products (e.g., PVC, formica, mypolam). Also included in this section are fab construction and planning schedules. Assembly is assumed to be contracted out as a service. Costs for wafer sort and final test are predicated on a dollar-cost-per-hour basis that covers labor and materials.

The assumptions used to develop the model for this cost analysis have been summarized below for easy reference. Although a 6-layer MOS model has been used, the analysis can readily be adapted to an 8-layer model by making adjustments in the equipment list, direct labor rate, and package type. Facilities costs would remain essentially unchanged. Wafer fab materials can be ratioed to accommodate the extended processing.

Technology - The devices that are to be processed in this fab facility are as follows:

- 16K DRAM, MOS N-channel
- 6-layer double-poly process
- 5-micron geometry
- 140 mil x 140 mil chip size (approximately 20,000 mil^2)
- 16-pin DIP plastic package
- 4-inch diameter silicon wafer
- 1:1 projection aligners (UV)
- Negative photoresist
- Wet etching
- Plasma etching of photoresist

Production - The important production parameters considered in this model are:

- Two full shifts per day (skeleton graveyard shift mainly for maintenance)
- Seven hours effective work per shift
- Five days per week = 20 days per period
- 12.5 productive periods per year, 13 accounting periods per year
- 25 percent benefit package including shift premiums

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- Minimum throughput at any step = 60 wafers per hour
- 10,000 wafers out per period
- Productivity at approximately 42 wafers out per operator per week (6 layers)
- All assembly operations offshore

Yields and Assumptions - The following yield factors are representative of mid-1980 production experience for devices chosen for this model:

- Cumulative fab yield, 80 percent
- Wafer sort, 16 percent
- Assembly yield, 90 percent
- Final test yield, 80 percent

Facilities - The facilities required are:

- Building rented as shell at $1.00 per square foot, per calendar month
- Space rented = 25,000 square feet
- Minimum of 15 percent inflation rate on construction, materials, and equipment
- All facilities and services supplied from scratch
- All design services contracted to outside engineering firms
- All chemicals (except photoresist) to be pumped into the fab area from storage tanks to points of use
- Masking can accommodate up to 10 projection aligners
- Diffusion can accommodate 20 furnaces
- Fab area = 12,160 square feet; wafer sort, test, offices = 12,840 square feet total

Equipment - The assumptions made for equipment selection include:

- Highly automated operation
- Convertible for use on 5-inch (125mm) diameter substrates

- Equipment may be used eventually on 2 to 3 micron gates and shallow junctions (less than 1.0 micron)
- Need filled for data collection and information management to facilitate trend analysis

Cost of Facility - The costs of the facility described in this model are shown in Table 11-1.

Table 11-1

FACILITIES COST SUMMARY

Fab Construction	$ 884,000
Wafer Sort, Test Area, Offices, etc., Construction	513,000
DI Water Plant	350,000
Air Conditioning	438,000
Chemical Storage	220,000
Electrical Power Plant	258,000
Equipment Installation	320,000
Cooling Water and Tower	82,000
Architectural and Engineering Designs	493,000
Other Equipment Systems and Alarms for Fab and Test	274,300
Grand Total	$3,832,300

Source: DATAQUEST, Inc.
April 1982

(Note: No allowance has been made in this subsection for contingencies such as inflation, moving and storage, cost overruns, and other demons of real life. A practical allowance for contingencies ranges from 10 to 15 percent of the total shown in Table 11-1.)

It must be mentioned here that "construction" refers to specific items including ceilings, floors, perimeter walls, roof screens, and trenching.

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Fixed Costs - Fixed monthly costs are estimated at $161,598 per period. Equipment costs have established a new plateau for a fab facility producing 10,000 wafers per period. Depreciation on this equipment exeeds the combined total of all other fixed monthly costs. However, the productive life of most of this equipment is much shorter than the 60 months allowed for its depreciation. The industry would welcome a depreciation period of 36 months, since equipment represents the major capital outlay. As it ages, very little of this equipment can be adapted to challenge the demands of new technology. Consequently, this protracted 60-month depreciation period constitutes a major drawback for would-be entrepreneurs. The cost of electrical power is by no means insignificant and could rise sharply over the next few years. It appears that the only answer to the inflationary spiral in which equipment and energy costs are trapped lies in increased productivity and yields. This fact cannot be repeated too often to planning and production teams.

Variable Costs - In general, there is more variation in costs due to yields than to any other parameter involved in processing 4-inch substrates. Raw silicon wafer costs vary from $9 to $11, depending on whether epitaxial material is used.

Mask costs vary tremendously, depending on the mix between projection and contact printing. For well-established products with a long history in the marketplace, the data we researched showed projection mask costs of well below 10 cents. The model described increases this cost to 25 cents to reflect shorter product lifetimes, superseded designs, new development costs, breakage, and yield losses from mask cleaning and inspection. Additional cost variations may occur, depending on whether masks are purchased or produced in-house.

Deionized (DI) water usage ranges from 80 gallons to 260 gallons per yielded wafer out, and is typically 140 gallons per wafer. DI water costs per gallon range from 1.0 cents to 0.65 cents; the typical cost is 0.7 cents per gallon.

Table 11-2 shows $59.84 as the total cost per wafer out for the N-channel MOS model used. The percentage contributions of the various cost elements are also shown.

Die Cost Analysis - An analysis of the survey data indicates that isolation of testing costs incurred by specific device types is difficult and unrewarding. The trend is toward consolidating the wafer sort and final test areas. Costs are then allocated to each product type according to the time each wafer spends on testers. The average tester cost-per-hour was found to be $48.86 with a standard deviation of $7.97. Device yields on 16K DRAMs tend to lie between 15 and 25 percent at wafer sort. This percentage is up from the 5 to 15 percent yields seen in 1978. The less bullish figure of 16 percent was adopted for our model. At this rate, almost four 4-inch wafers per hour can be tested. Paradoxically, higher yielding wafers may cost more to test because a good die is tested more completely—testing ceases for a bad die at the first failure. A large component of the testing cost is for wafer placement, or setup, during which the wafer is mounted and inspected and the probes set.

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Table 11-2

COST PER WAFER OUT

		Cost		Percent
Fixed Monthly Costs		$16.16		27.0%
Fab Materials		21.81		36.4
Fab Labor:				
Direct	$ 5.75		9.6%	
Indirect	2.59		4.3	
Allocated	13.53		22.7	
Subtotal		21.87		36.6
Total		$59.84		100.0%

Source: DATAQUEST, Inc.
April 1982

Table 11-3 details our cost calculations for a packaged die. The model assumes assembly operations are "offshore" (Malaysia, Mexico, Philippines, Southwest Asia), following the established trend within the industry. An assembly cost of $0.180 is assumed for this model.

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Table 11-3

PACKAGED DIE COST
(16-Pin DIP Plastic)

Wafer Sort		
• Cost per wafer at wafer sort = (Cost per hour)/ (No. of wafers sorted per hour) = $48.86/4 =	$12.2200	
• Wafer sort cost per gross die = $12.22/550 =	$ 0.0222	(a)
• Wafer fab cost per gross die = $59.84/550 =	$ 0.1088	(b)
• Total cost per gross die	$ 0.1310	(a+b)
Cost per net die at wafer-sort 0.1310/(16% wafer sort yield)	$ 0.8188	(c)
Assembly		
• Cost of die from wafer sort =	$ 0.8188	(c)
• Assembly cost per gross die =	$ 0.1800	(d)
• Assembly yield =	90%	
• Cost per gross die = (c) + (d) =	$ 0.9988	(e)
Therefore, cost per net die = (e)/90% =	$ 1.1100	(f)
Final Test		
• Test time per die =	15 sec.	
• Test cost per second = $48.86/3600 =	$ 0.01357	(g)
Therefore, Test cost per gross die = (g) x 15 =	$ 0.2036	(h)
• Total cost per gross die = (f) + (h) =	$ 1.3136	(i)
• Final test yield =	80%	
Therefore, cost per net die = (i)/80% =	$ 1.6420	(j)
Pack and Ship		
• @ 99.9% yield =	$ 0.0200	(k)
Therefore, (j + k) = Total Cost Per Net Die =	$ 1.6620	

Source: DATAQUEST, Inc.
April 1982

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Plastic packages are increasing in versatility. Important advances have been made recently in heat dissipation and, at present, they represent a cost advantage over ceramics of three to four times.

Equipment Costs - Table 11-4 summarizes the costs of equipment required for wafer fabrication.

Table 11-4

N-CHANNEL MODEL EQUIPMENT COSTS

	Capital Cost	Percent of Total
Diffusion Area	$1,339,450	21.0%
Masking Area	2,283,300	35.9
Deposition Area	1,039,700	16.3
Fab Support and Test Areas	1,287,900	20.3
Backside Processing	414,600	6.5
Total (6-1/2% Tax included)	$6,364,950	100.0%

Source: DATAQUEST, Inc. April 1982

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Total Cost - Table 11-5 summarizes the total costs of the NMOS wafer fab facility described in this model.

Table 11-5

COST OF A 1980 NMOS WAFER FAB FACILITY

	Capital Cost	Percent of Total
Equipment	$ 6,364,950	62%
Facilities	3,832,300	38
Grand Total	$10,197,250	100%

Source: DATAQUEST, Inc.
April 1982

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Fast Turn 2-Micron CMOS Capability

This subsection addresses the design and manufacturing cost analysis of a facility dedicated to the prototype production of semi-custom or custom ICs. These ICs incorporate a 2-micron complementary MOS (CMOS) process having a double layer of metal for interconnections. The treatment mainly applies to a small-size facility "pilot line," where initial investment in processing equipment is kept to a minimum, and where the emphasis is on fast turnaround time. In such a facility the skills and intelligence of the technical people are more important than their wafer fabrication productivity.

The emphasis on fast turnaround time (10 to 15 working days) leads to low productivity of labor and extremely low productivity of capital equipment, even though equipment costs are minimized. As a result, wafer costs are about $360 per four-inch wafer; such a wafer would probably be priced in excess of $1,000, if this facility were to supply wafer processing services on the open market. These figures well exceed the current market prices of $120 to $240 for a four-inch CMOS wafer. Some of the price increase can be attributed to the high number of masking levels (13) and to the expensive equipment required for the reproduction of two micron lines. The rest is due to production inefficiency.

We believe that these high manufacturing costs can be justified by the fast turnaround time achieved—2 weeks instead of the 6 to 12 weeks normally obtained on a semiconductor manufacturing line. Having a product ready 4 to 10 weeks earlier might lead to benefits such as increased market share.

Fast turnaround time can also be achieved on a conventional manufacturing line by using the "hot-lot" technique. In this method a portion of the wafers are processed without having to wait in the in-process inventory. This technique is valid until an emergency—such as high yield loss—occurs. At such a time the economics of the situation demand that all resources of the line be applied to returning the line to full production. Any hot-lot runs are delayed for the duration of the emergency. Because emergencies occur frequently on most lines, the availability of this hot-lot service is at best somewhat unpredictable.

Any high-volume custom circuits developed on this line may be produced in another higher volume facility, and for this reason the processes must be compatible. This is possible because in the last few years, major developments have taken place in the areas of semiconductor materials, chemicals and gases, and in wafer processing equipment used in the industry. These developments, together with the availability of accurate computer simulation tools for semiconductor processes and devices, enable a small-scale wafer fabrication area to approach the type of process control formerly obtainable only on large manufacturing lines.

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A system house is strongly motivated to set up an IC fabrication facility as a means of implementing proprietary designs into silicon rapidly and with complete control. Alternatively, this need may be filled by small, efficient companies dedicated to the production of custom ICs.

Productivity Considerations

Organization - The pilot line is intended to produce a small quantity of wafers using state-of-the-art technologies and with fast turnaround time. It is not intended to be a laboratory dedicated to developing process technologies. Once the individual pieces that are part of the process flow have been installed and characterized, and a complete process flow has been defined and specified in detail, the line has to run with the same general organization and discipline as a normal (high-volume) production line.

The division of labor and level of experience required for the people in this type of organization are different from those of a high-volume production line. The division of labor in the wafer fab area is different because operators are cross-trained on several pieces of equipment. This allows them to hand-carry a batch of wafers through several sequential process steps, eliminating any inventory delay. In some firms these individuals might be given the title of modelmaker to distinguish them from conventional fab operators. A higher level of experience is generally required for most workers in the organization. The relatively small number of individuals in the pilot line must have the aggregate experience of the staff of a much larger production line if they are to be technologically competitive.

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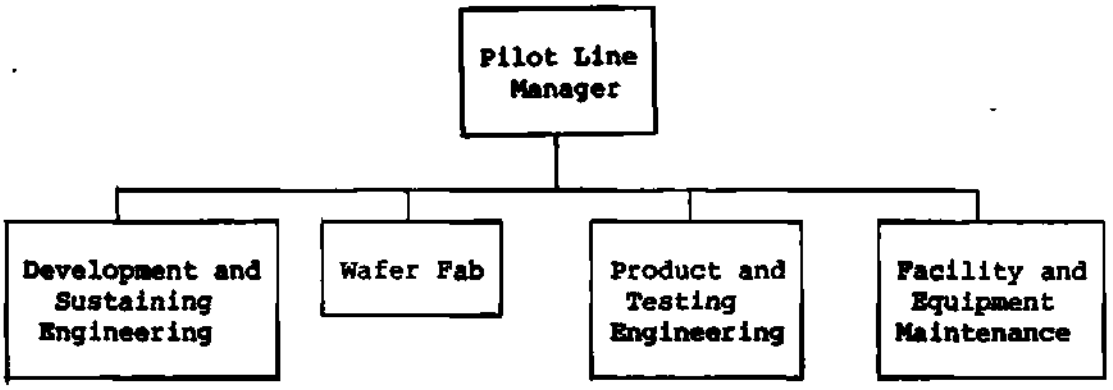
A typical organization chart is shown in Figure 11-4.

Figure 11-4

ORGANIZATION CHART



Source: DATAQUEST, Inc.
April 1982

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The development and sustaining engineering group comprises the engineers who will develop and install the technologies and train the operators to run the various process steps. They will be responsible for the quality of the material produced and for the correct use and maintenance of all equipment. Each engineer will have responsibility for more than one process technology and must be completely familiar with the equipment used and all the steps of the process. Because of the broad range of responsibility of the job, he or she must be familiar with the physics of semiconductor devices and have experience in both semiconductor research and development, and in production environments.

The wafer fab group comprises all the equipment operators. This group is directed by one supervisor who is responsible for scheduling the movement of the material, and for the line throughput. To enhance turnaround time, the operators (or modelmakers) must be able to perform several related steps. For example, a diffusion operator will run all the diffusion, low-pressure chemical vapor deposition (LPCVD) and ion implantation operations, together with wafer cleaning and resist stripping operations. Having all operators capable of doing all the processing steps is ideal for reducing turnaround time because it reduces or eliminates problems. Unfortunately this goal is practically impossible to achieve because of the long time required for training. It is also dangerous because of the lack of doublechecking. However, one or two operators of this kind (senior modelmakers) are invaluable for processing batches of wafers that have priority over the other batches.

The size of the product engineering and testing group depends on how much the customer is going to do in terms of testing the circuits. Even if the customer does all the testing at the wafer level and all the debugging of the circuits, the pilot line still needs product engineers who use specifically designed test patterns that will constantly monitor the stability of device parameters and the defect level of the wafers. These product engineers can be much more effective if they are also responsible for at least limited device testing, and if they have good communications skills and a good understanding of both processing and circuit design.

Fast turnaround requires that most equipment performs properly most of the time. Responsive and professional maintenance of the facility infrastructures and processing equipment is key to this goal. Preventive maintenance should be done at specified times, even if the process engineers think that it is unnecessary. Whenever possible, maintenance contracts that cover preventive and emergency equipment care should be negotiated at the time of purchase. The availability of such contracts usually directly determines the reliability level of the equipment.

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Staffing - For a 500-wafer-out operation of this kind, our estimate of personnel requirements is shown in Table 11-6.

Table 11-6

STAFFING REQUIREMENTS

Classification	Job Function	Personnel Required	Estimated Wage Rate Per Period* (Thousands of Dollars)
Direct	Wafer Fab Operators (Model Makers)	10	$1.40
Indirect	Line Manager	1	$4.50
	Wafer Fab Supervisor	1	$2.50
Allocated	Development and Sustaining Engineers	5-6	$4.00
	Product and Testing Engineers	2	$3.00
	Facility and Equipment Maintenance Engineers	3-4	$2.80

*Period equals four weeks

Source: DATAQUEST, Inc.
April 1982

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Number of Shifts - For most operations, the presence of all the process engineers is essential. Consequently, the number of shifts cannot exceed two; for example, a large shift from 7:00 a.m. to 3:30 p.m., and a reduced-staff shift from 2:00 p.m. to 10:30 p.m. This small second shift can complete time-consuming operations that take longer than eight hours such as high-dose implants and long diffusions.

The only exception is in the masking area. There, a full staff of experienced operators and sustaining engineers should operate on two shifts because of the limited throughput of the wafer stepper equipment.

Equipment Selection Criteria - For easy transfer of the technology to a production line, the equipment of the pilot line should be compatible with production-type equipment. The decision of whether to use an R&D or a production version of the equipment requires a good knowledge of, and familiarity with, the process in question, and a detailed study of all the factors that might affect the duplication of the operation. Such a decision should be made by the development engineer under the guidance of the line manager. Some money can be saved by not selecting many of the equipment options offered for operation by inexperienced and untrained operators, but automation that saves labor and enhances productivity and safety should be included.

Maximum Output - With only one wafer stepper used on two full shifts, the pilot line production is limited to 500 wafers out per period (four weeks). For such output, all other equipment will be used a maximum of 60 percent of the time it is available. This allows plenty of time for maintenance, and enhances turnaround time.

To reduce the load on heavily utilized equipment (wafer stepper, ion implanter, oxide etcher, and one furnace) even further, the equipment might be duplicated. Additional space is provided for that purpose in the layout and design of the facility.

For photolithography, the pilot line will use one 10:1 wafer stepper for all the masking levels requiring high resolution and/or the smallest registration error to the previous pattern, and a 1:1 scanning projection system for all other layers. For a CMOS circuit with double layer metal, the critical masking levels are the same as for an NMOS circuit. These are the masks for fields, gates, contacts, vias, and metal.

All but one of the remaining mask levels are oversize masks, and alignment tolerances can be relaxed. The exception is the p-well mask. For some types of circuits where the spacing between p- and n-channel devices could significantly affect the die size, it may be advantageous to use the wafer stepper for defining the p-wells, but this was not done in our model.

Because of the high degree of control required for positional accuracy of the patterns and the size accuracy of their dimensions, 1:1 masks and 10:1 reticles must be generated with electron-beam maskmaking equipment.

11. Captive Decisions

Fab Layout and Facility Requirements

Designing the layout of the fab area for a pilot line is very challenging. It is a compromise between various and often contradictory needs. The requirements are to:

- Ensure a smooth flow of the wafers through the steps of the main process that is going to be used in the facility
- Allocate space and equipment for new technology developments so that they will not interfere with standard production
- Simplify the layout of process piping, air and exhaust ducting, and power distribution for ease of maintenance and for cost reduction during construction
- Facilitate equipment maintenance, so that it will not disturb work on any other equipment
- Ensure the highest achievable level of cleanliness, particularly in the masking and deposition areas

Process Flow - While the n-channel silicon gate process flow is well established, the same is not true for the CMOS process.

Ten is the minimum number of masking steps necessary for producing two-layer metal CMOS circuits. Three extra implant protection masks are usually added for better control of device characteristics, and for reducing the spacing between p- and n-channel devices. These are added in our process flow.

The critical masking levels for which the wafer stepper equipment will be used are fields, gates, contacts, vias, and metal. These levels require accurate image resolution and layer-to-layer registration.

Clean Room Layout - A typical layout for the equipment in the wafer fab area is shown in Figure 11-5. There are three distinct areas:

- Photolithography area, which includes the process line for the wafer stepper and the area for the projection aligner; as shown in Figure 11-5, the process lines can easily accommodate two steppers and two 1:1 projection aligners; the photolithography area is isolated from the rest of the clean room and uses a dedicated air conditioning system
- Etching and metal deposition area, which requires a high degree of cleanliness, but a less stringent climate control than the masking area
- Diffusion, thin film deposition, and ion implantation area

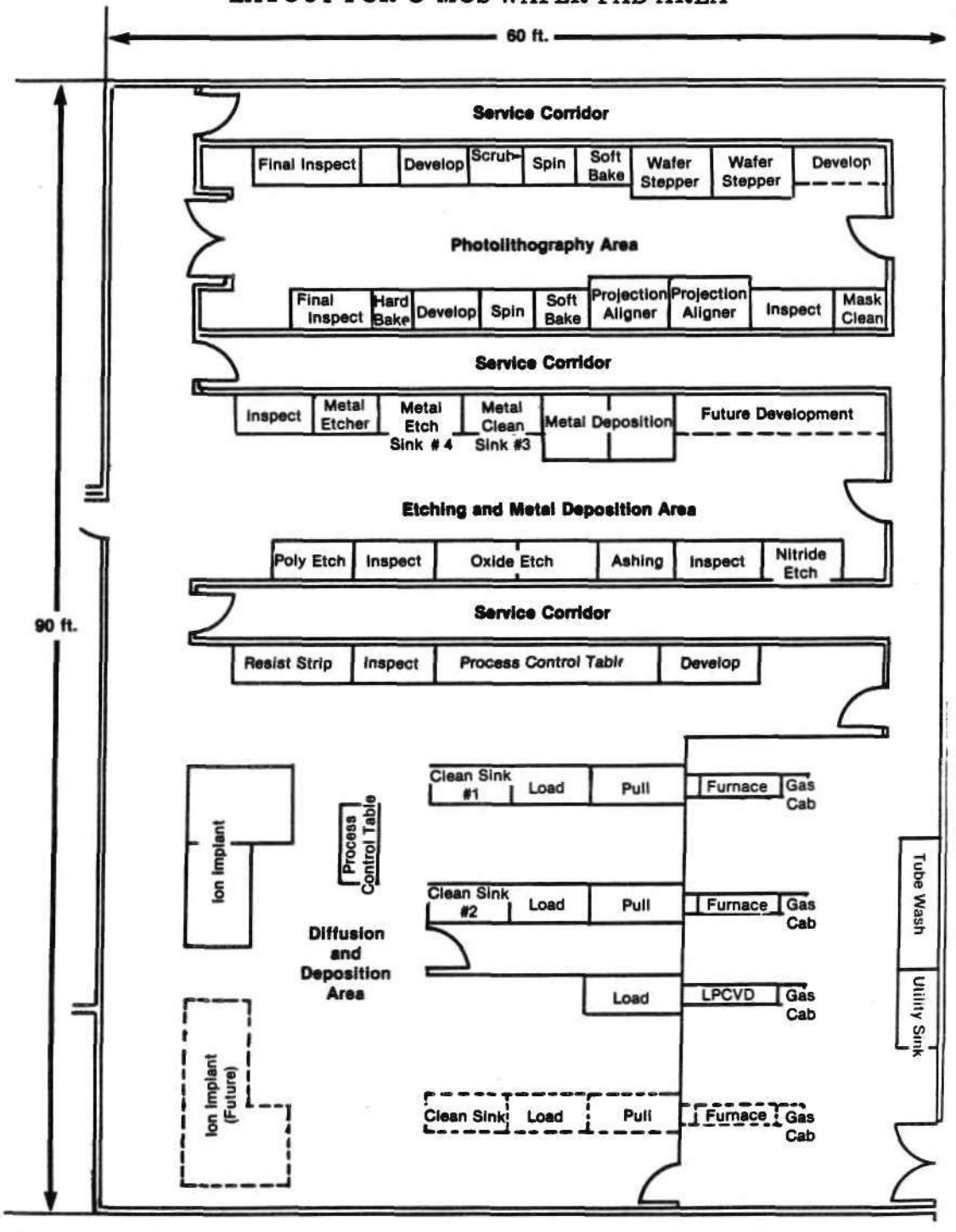
11. Captive Decisions

Service aisles are provided behind the lithography and etching process lines. All the "dirty" equipment (such as pumps, power generators, canisters containing liquids, and specialty gas cylinders), the gas and liquid pipes, and the electrical wiring are located in the service aisles. This approach allows most of the maintenance work to be done outside the clean areas. The resulting reduction of traffic makes it easier to keep the clean areas particle free.

The overall wafer fab area is 5,400 square feet. The service aisle area is about 1,300 square feet, leaving a net effective clean area of 4,100 square feet.

Figure 11-5

LAYOUT FOR C-MOS WAFER FAB AREA



Source: DATAQUEST, Inc.
April 1982

11. Captive Decisions

Facility Requirements

The major systems for the wafer fab area are listed in Table 11-7. Non-recoverable cost is the portion of the cost that is due to physical additions to the building, such as process piping or clean room construction. These items generally have a longer depreciation cycle.

Table 11-7

FACILITIES IMPROVEMENTS FOR WAFER FABRICATION AREA
(Thousands of Dollars)

System	Average Cost	Nonrecoverable Cost
Fab Construction	$ 555	$360
DI Water System (with 80-percent Reclamation)	163	60
Air Conditioning (with Cooling System and Tower)	190	60
Chemical and BOH6 Storage	22	22
Electrical	175	125
Totals	$1,105	$627

Source: DATAQUEST, Inc.
April 1982

11. Captive Decisions

Tooling - The costs of the reticles and masks used for wafer production are not included in the wafer cost analysis because they are usually included in circuit design costs. Mask-making costs are very high, ranging from $1,000 to $3,500 for 10:1 reticles and masks.

Facilities - For this model we assume that the building is rented as a shell at $1.00 per square foot per period. The total space rented is 12,000 square feet (5,000 square feet for wafer fab, the remainder for offices and service areas). Facility design is contracted to an outside engineering firm and all facilities and services are supplied from ground zero.

As shown in Table 11-7, the total cost of construction and equipment of the systems supporting the fab area is $1,105,000, of which $627,000 is nonrecoverable. In terms of depreciation, the latter portion of the cost is treated as fab construction cost. Construction cost for office, test area, and service areas is estimated at $40 per square foot for a total cost of $280,000.

Equipment - Table 11-8 gives our estimates for the equipment costs for this model.

Table 11-8

EQUIPMENT COSTS FOR FAST-TURN
2-MICRON CMOS FAB FACILITY
(Thousands of Dollars)

Equipment	Cost
Diffusion Area Equipment	$ 751.5
Deposition and Implantation Equipment	635.5
Etching Equipment	628.9
Masking Equipment	1,346.2
In-process Test Equipment	289.0
Total Cost for Fabrication Equipment	$3,651.1

Source: DATAQUEST, Inc.
April 1982

11. Captive Decisions

Wafer Costs - The cost per wafer is shown in Table 11-9. It is based on all the fixed costs and variable costs of materials and labor; the percentage of total cost that each represents is shown in the right-hand column.

Table 11-9

COST PER WAFER FOR A FAST-TURN
2-MICRON CMOS FAB FACILITY
(Dollars)

	Cost	Percent of Total
Fixed Costs per Period	$189.58	52.3%
Fab Materials	35.90	9.9
Fab Labor	137.00	37.8
Total Cost per Wafer for 500 Wafers Out	$362.48	100.0%

Source: DATAQUEST, Inc.
April 1982

Increasing Productivity

The productivity of the pilot line, in terms of wafers per operator and per square foot of fab area, is quite low if one compares these results with those achieved in n-channel dynamic RAM production lines. Productivity is low for the following reasons:

- The equipment utilization is low and the batch size is small to achieve fast turnaround time.
- The CMOS process is more complicated than a conventional n-channel process.
- The investment in expensive equipment (e.g., aligners) is limited, which creates throughput bottlenecks.

11. Captive Decisions

Certain expensive equipment is significantly underused in this model, but productivity can be improved by duplicating the more heavily used equipment. This has the additional benefit of avoiding a complete paralysis of the line in case a heavily used piece of equipment breaks down.

The following subsection modifies the plan to increase wafer throughput from 500 wafers out per period to 1,000 wafers out per period. Substantial cost savings result. While output could be increased still further and give still more cost savings, DATAQUEST does not believe the 10- to 15-working-day turnaround time can be maintained under such conditions.

Duplication of Equipment - The line throughput can be doubled by adding:

- One wafer stepper, used on two shifts
- One furnace, used on two shifts
- One ion implanter, used on two shifts
- One oxide etcher, used on one shift

Wafer stepper utilization still remains at 85 percent, which is very high, but this assumes a wafer throughput of only 15 wafers per hour. The expected improvements in existing equipment (automatic alignment and automatic reticle exchange) and the introduction of completely new models should increase equipment throughput by at least a factor of two, thus reducing the equipment utilization to levels more acceptable for a fast turnaround time.

Wafer Cost Analysis for Increased Line Throughput - For increased throughput, these cost figures will change:

- Fab equipment depreciation
- Labor

No other costs will change significantly. The fab equipment depreciation per month will increase from $60,851 to $76,938. This will add depreciation of $14,850 per period. The direct labor cost per wafer will decrease from $35.00 (10 fab operators), to $26.25 (15 fab operators), and the allocated labor cost will decrease from $84.50 per wafer to $60.75 per wafer (with the addition of two sustaining engineers and one maintenance engineer).

Table 11-10 shows the total wafer cost for 1,000 wafers out per period in comparison to the cost for 500 wafers out.

11. Captive Decisions

Table 11-10

COST PER WAFER

	500-Wafers-Out*		1,000-Wafers-Out*	
	Cost	Percent	Cost	Percent
Fixed Cost*	$189.58	52.3%	$109.69	45.4%
Fab Materials	35.90	9.9	35.90	14.9
Fab Labor:				
Direct	$ 35.00		$ 26.25	
Indirect	17.50		8.75	
Allocated	84.50		60.75	
Total Labor	$137.00	37.8	$ 95.75	39.7
Total Cost Per Wafer	$362.48	100.0%	$241.34	100.0%

*Per Period (4 weeks)

Source: DATAQUEST, Inc.
April 1982

Using Captive Capacity

Large semiconductor users that have been in business for several years have established "Make or Buy" policies and procedures that guide semiconductor and other purchasing decisions. The make/buy decision usually occurs at the corporate management level, although corporations that have captive facilities may delegate this responsibility to the procurement function.

There are many reasons for periodically reviewing the supplier base list and for reviewing the make/buy decisions for particular semiconductor products and services. These include:

- New suppliers entering the marketplace
- Major changes in available technology, such as availability of EEPROMs, gate arrays, or GaAs technology

11. Captive Decisions

- Significant changes in available services, such as addition of EPROM or PROM programming capacity by a local distributor
- The need for secrecy—has it changed?
- Deterioration in product quality to a level below the required minimum
- Captive sources' inability to deliver on time and within budget
- Semiconductor suppliers' inability to deliver
- Major increases or decreases in the need for a product or products
- Major changes in semiconductor product mix requirements
- Internal or external economic pressure
- The desire to avoid a layoff, reassignment, or retraining of personnel
- The need to accelerate availability of a new semiconductor product
- Withdrawal of a semiconductor product by a supplier
- Withdrawal of a supplier from the market
- The acquisition of a source of supply
- The acquisition of a supplier by another company
- Major price increases (rare in the history of semiconductors)

The classic problem of deciding whether to purchase semiconductor products from within or to buy from outside can be solved more readily through the use of a detailed checklist. There are seven major categories of questions to be considered: suppliers, skills, quality, capacity, labor, scheduling, and cost. The following checklist includes major questions in each of these categories.

- Suppliers:
  - If we make the device, will sales relationships be jeopardized? Do we depend on the representative or distributor for support in other areas?
  - Is stability of supplier relationships a factor?
  - Does the supplier meet all governmental and other requirements for location and stability of capacity?

11. Captive Decisions

- Skills:
  - Is this the most profitable use of our management's time?
  - Do we have adequately experienced device, process, test, and follow-up engineering and other technical talent in place to execute the results of this decision?
  - Can we measure our progress efficiency as we proceed?
- Quality:
  - Will the completed products conform to all electrical and mechanical specifications?
  - Are the necessary equipment and procedures in place for measuring and maintaining quality?
  - What is our experience to date in this type of activity?
  - Who pays for and replaces rejects? When?
- Capacity:
  - Is clean room and other space available to meet our requirements as well as those of others within the corporation?
  - Is the space we are considering already committed to other uses?
  - Are furnaces and other process equipment available when needed?
  - Are maskmaking services in place and usable?
  - Is assembly capacity in place and usable?
  - Is test capacity in place and available?
  - Are the test programs available at reasonable cost and at the appropriate time?
  - How much capital investment is required? When?
  - How much working capital is required? When?
  - How will the facility be used in the future after this need is met?
  - When will the facility become obsolete? What then?

- Which activities and services must be subcontracted? Are the subcontractors competent, properly equipped, and able to meet the needs, on time, at reasonable costs?
- Are the required raw materials available at the right time and at reasonable prices?
- Is absorption of internal overhead a factor?
- What is the expected rate of return on capital expended? On equity? Is this rate acceptable to management?

• Labor:

- Would layoffs be created? Could talent be reassigned?
- Must staff be increased? At what cost and when?
- What additional training is needed? At what cost? When and by whom?
- Are there union pressures to be considered?

• Scheduling:

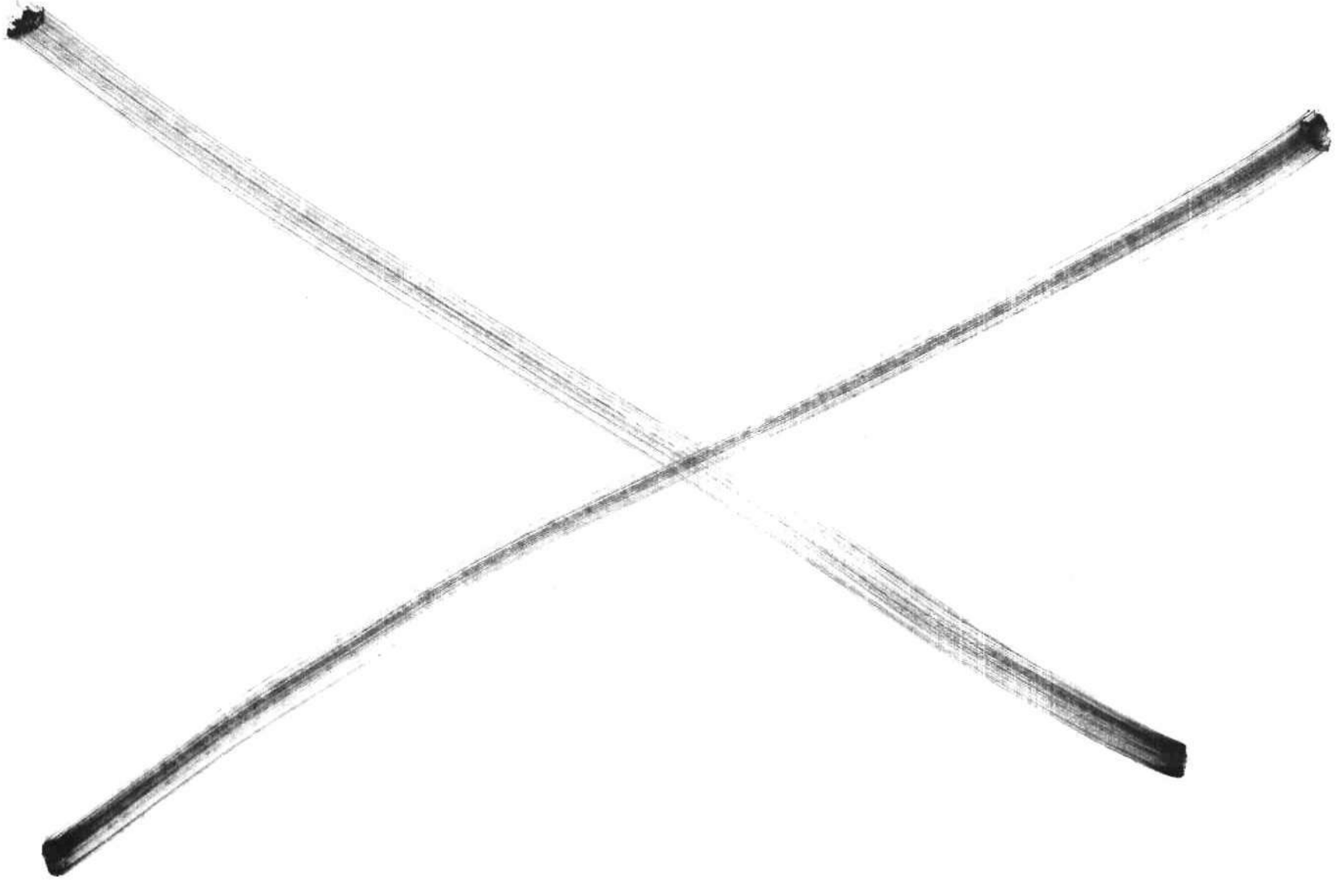
- Can capacity be adjusted for peak loading?
- What is the impact of slowdowns?
- Would risk be decreased with added resources?
- How often do engineering changes occur?
- How do engineering changes affect the schedule?
- Are the necessary controls in place to measure and maintain conformance to schedule?
- How often should schedules be reviewed?

• Costs:

- What are startup costs?
- What initial and continuing development costs are incurred?
- Are patents involved? Are royalty payments necessary?
- What are the estimated total first-year costs?

11. Captive Decisions

- What are the estimated total costs over project/program/product life? (This analysis should include careful attention to all labor, materials, operations, setup, inventory, tooling, subcontracting, packing and shipping, overhead, returns, flooring, and other lifetime costs.)



Nielsen Dataquest

INQUIRY RESPONSE

DATE: June 13, 1983

TO: Guy Robert/Thomson CSF

FROM: Stan Bruederle/Dataquest

This information has been compiled in response to your inquiry of June 1983

Please file in Section 12 for future reference.

Subject: Process Information

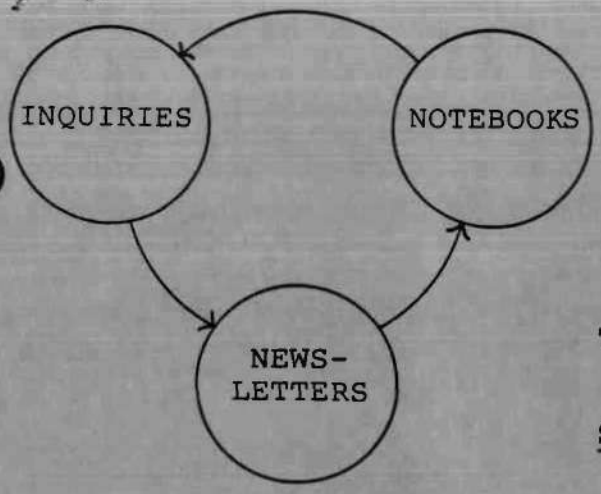
The number of basic mask steps for specific bipolar and MOS processes is identified below. I have included them for both single and dual layer metal procedures.

Process	Number of steps Single Layer	Dual Layer
Schottky TTL	7	9
ECL	8	10
NMOS	8	10
HMOS	9	11
CMOS	10	12
HCMOS	11	13
Bipolar Linear	7-9	9-11

The number of steps varies from manufacturer to manufacturer. These represent the basic process steps for typical processes. As you can see, MOS processes have become more complicated than bipolar processes.

I will send you bipolar RAM and static MOS RAM forecasts next week.

cc: Bud Mills



SEMICONDUCTOR USER INFORMATION SERVICE

THE THREE-RING CIRCUS

SUIS Product Bulletin

Introducing - - - The SUIS Inquiry Response letter!!

This is an example of the inquiry response letter we told you about at the sales meeting. Any significant inquiry will be answered in writing to the client with a copy to the responsible salesman. Each response will include instructions for filing in the SUIS notebooks. Users will then have a notebook tailored to their specific needs, and you will have a record of our inquiry support for renewal discussions.

The inquiry used for this example is typical of the types of questions that we get asked. We will provide you with other examples, with client names removed, that you can show prospects.

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The logo in the left-hand corner of this bulletin offers an eloquent demonstration of the way the various parts of SUIS interact. We call it the Three-Ring Circus--and this is the first of a series of product bulletins bearing that name.

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INQUIRY RESPONSE

DATE: January 24, 1983

TO:

FROM: Jean Page, Research Analyst
Semiconductor User Information Service

This information has been compiled in response to your inquiry of 1/12/83

Please file in Section 2 for future reference.

Here is the information you requested on 8Kx8 static RAMs.

Hitachi - is already sampling parts and ramping up to production quantities. Prices are currently in the $100 range and expected to be below $50 by mid-year.

Toshiba - are offering two parts, one CMOS, and one NCMOS during this year. I do not have any information from them on prices.

Fujitsu - will be sampling parts at $70 in the second quarter on this year and expect the price to decline to $35 by third quarter.

NEC - plan to offer parts in July and expect the price to be in the region of $25.

Mitsubishi - will sample parts in second quarter 1983 and plans volume production by the end of the year.

Harris - are offering a hybrid module with 4x16K static RAM in it.

IDT - will probable enter the market in 1984 since this is a logical extension of their current product line.

Intel - Since your message suggested that you are still in the design phase, you may also be interested in Intel's 8Kx8 IRAM which offers dynamic RAM density with integrated refresh circuitry.

Despite some of the above statements, we expect pricing to be in the area of $40 by July 1983 and, assuming that all suppliers come reasonable close to their stated plans, the price should be in the region of $12 by July 1984.

Semiconductor Technology

OVERVIEW

This section of the Semiconductor User Information Service is intended as a resource for the reader who has a limited background in semiconductors. It can be used either as a tutorial to gain a general understanding of semiconductor technology or as a reference tool for information on a specific topic. The first part of this section discusses semiconductor materials—how they function and how they are used to make semiconductor devices. The discussion continues with an explanation of how semiconductors are manufactured and tested. The last and major part of the section looks at the individual types of devices, from discrete components through integrated circuits including VLSI. It discusses how the devices are used and how they function. The glossary included in this volume defines in detail many of the terms used in this discussion.

SEMICONDUCTOR MATERIALS

Semiconductor technology pragmatically combines chemistry, physics, and mathematics to create some of society's most complex tools.

A semiconductor material falls midway between a conductor and an insulator in its ability to conduct electrical current, and can be made to conduct electricity readily by introducing impurities into its crystalline structure. The process of introducing impurities into a semiconductor material to modify its electrical properties is called doping. If the doping procedure reduces electron density, it results in positively charged (P) material. If, on the other hand, the doping increases electron density, the result is negatively charged (N) material. Electron density can thus be varied during wafer fabrication by varying the concentration of impurities through doping.

Semiconductor materials may be purified natural elements such as germanium (Ge) or silicon (Si), or they may be compounds such as gallium arsenide (GaAs) or gallium phosphide (GaP). Silicon is the most popular semiconductor material in use at the present time. It belongs to group IV in the periodic table of elements, and can operate at higher temperatures than can germanium. Silicon is used as the basic ingredient of diodes, transistors, integrated circuits (ICs), optoelectronic devices, transducers, solar cells, detectors, and other semiconductor devices.

Germanium is also a group IV (periodic table) element. The very first transistor was a germanium device, and germanium was used extensively during the 1950s and early 1960s for diodes and transistors. However, because germanium is useless as a semiconductor above approximately 80^{o}C, and because germanium is not easily fabricated using planar technology, silicon became the workhorse of the industry in the early 1960s.

Gallium arsenide (GaAs) is useful for very-high-performance semiconductors. It was first used for high-frequency amplification and light emission (light emitting diodes (LEDs), injection lasers, etc.). GaAs is a group III-V compound that has high electron mobility. Considerable research into the potential use of GaAs in very-high-speed LSI applications is currently under way.

Gallium phosphide (GaP) is a III-V compound that finds application in the manufacture of some types of photodiodes. It can be doped to form LEDs that emit either red or green light.

The crystalline forms of carbon (another group IV element) have been researched as semiconductors, but their low electron mobilities make them inappropriate.

SEMICONDUCTOR MANUFACTURING

This subsection gives a brief general description of semiconductor device manufacturing, followed by a more detailed discussion of the specific characteristics of bipolar and MOS processing. Those readers who require only a general understanding of the subject should find all the information they need in the first part of the discussion. Semiconductor manufacturing operations involve the following activities:

- Raw wafer preparation
- Wafer fabrication, including oxidation, photomasking, diffusion, ion implantation, and vapor deposition
- Wafer test
- Dicing operation
- Assembly, including bonding and sealing
- Final test, marking, packing
- Shipment

Wafer Fabrication

Most semiconductor devices are fabricated on wafers of pure crystalline silicon. The wafers are disks, usually 100 millimeters (approximately four inches) in diameter and 14 to 20 mils (thousandths of an inch) thick. The wafers are heated in a furnace tube filled with wet or dry oxygen so that a layer of oxide is formed on the surface of each wafer.

The next step in wafer fabrication is photo-masking (shown in Figure 12-1). This is the process of defining the physical design of the device for each layer. In very complicated devices there may be as many as 13 layers or mask steps.

For each step, the oxidized wafer is first coated with a layer of photoresist—a substance similar to the emulsion on ordinary photographic film or paper. A mask with the design for that layer is then placed between the wafer and a source of ultraviolet light. Those parts of the wafer that were protected from the light source by the mask have a different level of solubility from those that were exposed. The unexposed sections can be washed away with an appropriate solvent leaving a negative image of the mask on the wafer. (This is analogous to the way a positive print is made from a photographic negative.)

Acid is then used to etch away the exposed oxide from the surface of the wafer. The next step is to remove the remaining photoresist using an appropriate solvent.

The wafer is then ready for doping, using diffusion, ion implantation, or both. This is the process of introducing impurities into the silicon to create the various circuit elements.

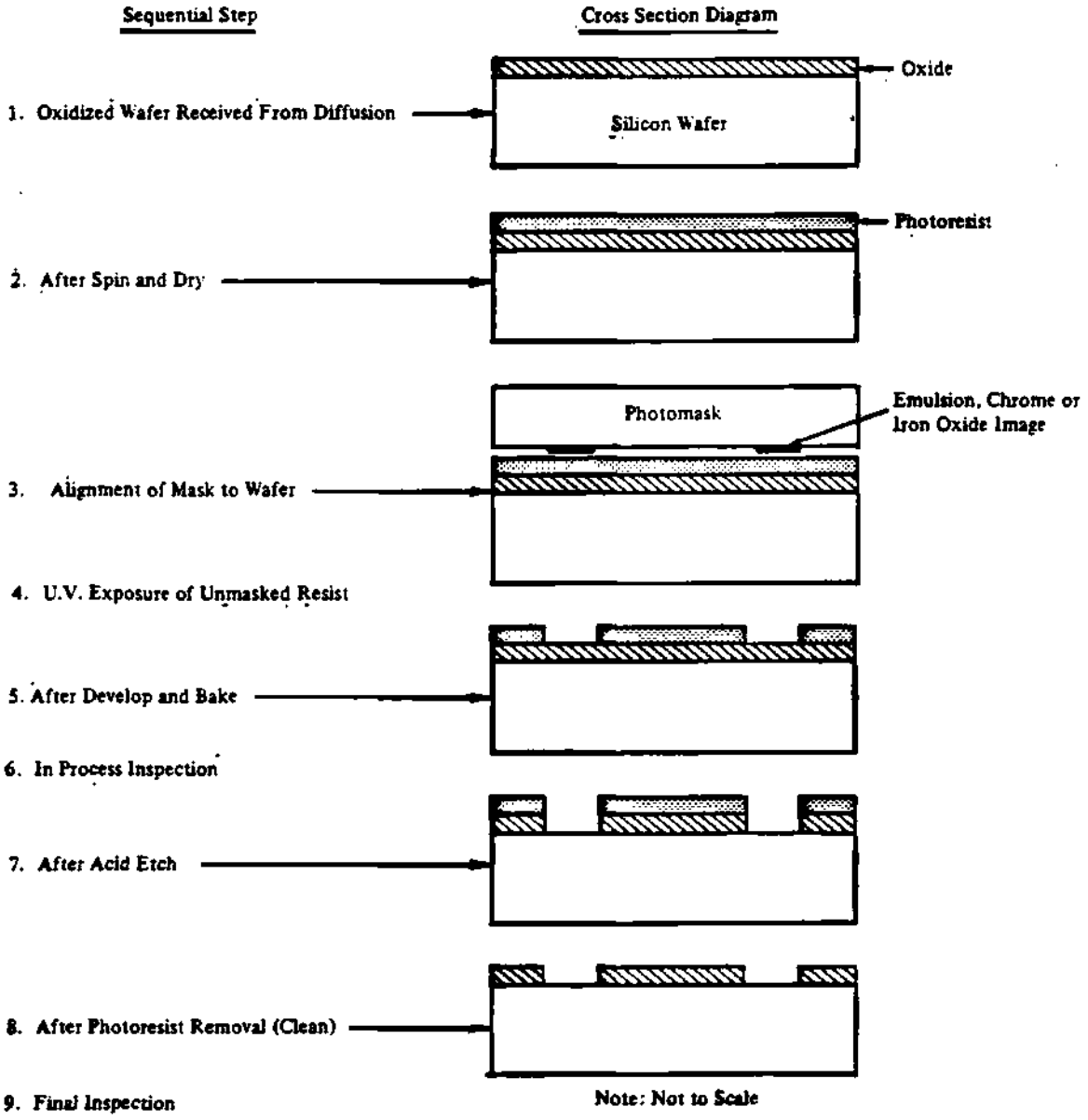
The sequence of steps or some of the steps may be repeated several times for complex devices. The next to last layer of an integrated circuit is usually a metallization or interconnect pattern that establishes the desired electrical relationships among all the elements of the circuit. The last layer is a protective layer.

Once the wafer fabrication process is completed, each die on the wafer is tested and the defective dice are identified by inking. The wafer is then divided into individual circuits or dice, and those dice that passed inspection are packaged ready for use.

A more detailed explanation of specific types of wafer processing techniques and of the subsequent steps in producing a finished component is given below.

Figure 12-1

PHOTOMASKING PROCESS STEPS



Source: DATAQUEST, Inc.
April 1982

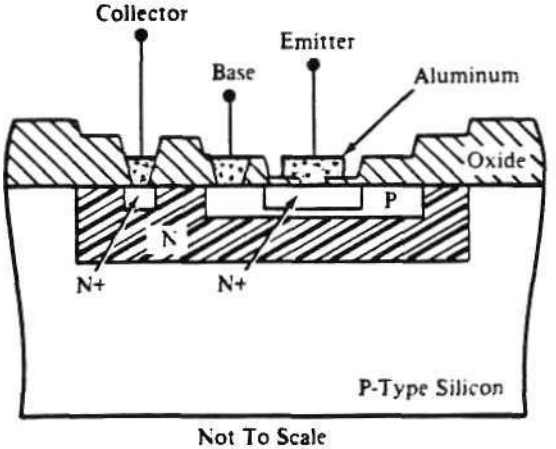
Bipolar Structures and Processing

A number of bipolar process technologies are available, producing a multitude of product families. The basic fabrication technologies are derived from two processes: multidiffused and epitaxial. A cross-section of a multidiffused bipolar device is shown in Figure 12-2. The particular device shown is called a triple-diffused transistor, because three separate diffusions are needed to form its three electrodes.

The triple-diffused transistor in Figure 12-2 is formed sequentially by a series of three vertical diffusions, with intermediate photomask steps defining the areas to be doped. Each successive diffusion is to higher dopant concentration and of opposite dopant type than the previous layer. The dopant is placed within the previous diffused area or "well". The final N diffusion is performed into the P diffusion, which was made into the first N diffusion. The final high concentration contains 100 to 1,000 times more dopant than the initial N diffusion. In the fabrication of many devices, gold is also diffused into the wafer during the last N+ diffusion to enhance the speed of the transistors.

Figure 12-2

CROSS-SECTION OF A TRIPLE-DIFFUSED BIPOLAR TRANSISTOR



Not To Scale

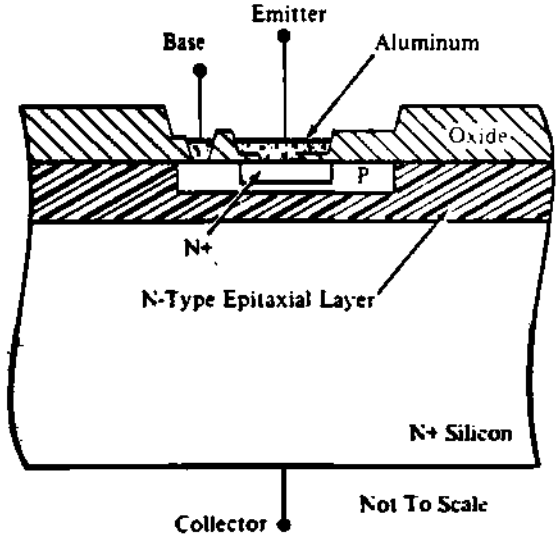
Source: DATAQUEST, Inc.
April 1982

The triple-diffused process formed the basis for the introduction and early production of many bipolar discrete devices and ICs that are discussed later. Although the process is simple by today's standards, it represented a radical step forward in process technology when it was introduced in the 1950s. Multidiffused processes are still being used today, primarily for discrete devices. However, most bipolar integrated circuits currently in production use the epitaxial process to gain improved device performance and cost.

In the early 1960s a number of semiconductor companies announced products that used an epitaxial (epi) structure and manufacturing process. The cross-section of an epitaxial transistor is illustrated in Figure 12-3. The N epi layer in this structure serves the same function as the diffused N layer in Figure 12-2, and the subsequent processing is similar to that used in the triple-diffused process. The epi layer is deposited on a highly doped N substrate, as compared to the P substrate used in the multidiffused device.

Figure 12-3

CROSS-SECTION OF AN EPITAXIAL BIPOLAR TRANSISTOR



Source: DATAQUEST, Inc.
April 1982

The most significant advantages of the epitaxial approach are:

- An epitaxial (epi) layer of either polarity, N or P, and of lower dopant concentration than the substrate can be deposited on the silicon wafer. Figure 12-3 illustrates the case where a lower concentration N epi layer is deposited on an N+ substrate. This combination is not realizable with a triple-diffused process.

- Unlike the triple-diffused process, an epi layer has a uniform dopant concentration throughout. In the triple-diffused process, the initial concentration of dopant is highest near the surface and lowest where the N diffusion meets the P substrate.

- The P and N+ diffusions can be shallower in an epitaxial process, so that parasitic effects are less. This gives higher speeds and lower power dissipation, and allows smaller geometries.

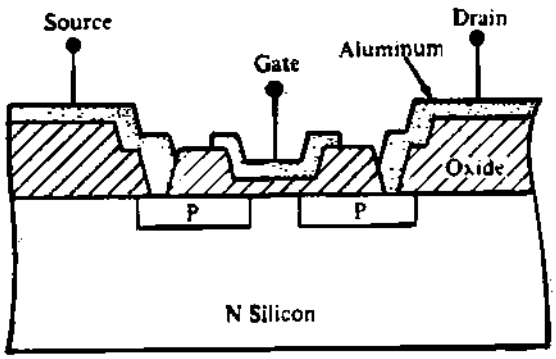
These three advantages allow for the design and fabrication of transistors and circuits that have higher voltage, higher current, and higher frequency performance than their triple-diffused counterparts.

MOS Structures and Processing

The controlling electrode of a metal gate MOS transistor consists of metal (typically aluminum) covering a thin oxide layer grown over the silicon. The cross-section illustrated in Figure 12-4 is typical of this class of MOS products, although variations to the structure are added by some manufacturers.

Figure 12-4

P-CHANNEL
METAL GATE TRANSISTOR



Source: DATAQUEST, Inc.
April 1982

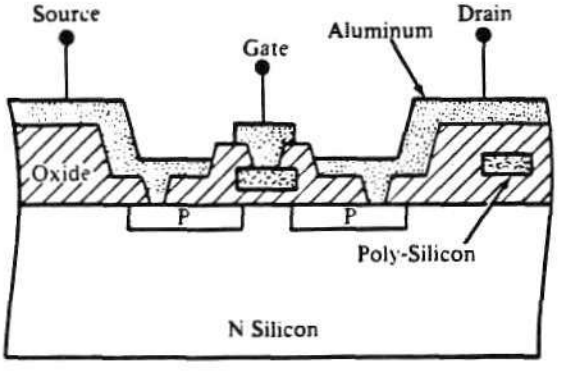
The advantage of the initial metal gate process, which dates back to 1963, was its process simplicity, particularly when compared with bipolar epitaxial processes. No epitaxial layer, or buried layer of isolation diffusion, was necessary. In fact, only one dopant diffusion and four masking steps were needed to manufacture a device.

The disadvantages of this process are in circuit performance and density. The initial P-channel products were very slow, and the density of components was limited by the single metallized interconnection layer. To overcome performance limitations, many variations on the P-channel process were attempted, and N-channel metal gate processes were introduced. However, none of these metal gate processes were able to blunt the thrust of the newer silicon gate process.

The silicon gate process, introduced commercially in 1968, produced the first major significant change in MOS processing. In a device produced using this process, the metal electrode was replaced by a highly doped layer of polycrystalline silicon, as shown in Figure 12-5.

Figure 12-5

P-CHANNEL
SILICON GATE TRANSISTOR



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Initially applied to P-channel devices, the silicon gate process generates the following benefits:

- The voltage required to turn on the device (threshold voltage) is halved (from 4 volts to 2 volts), resulting in higher speeds and voltage compatibility with bipolar TTL circuits.
- The conductive polysilicon may be used as an additional interconnection layer; thus, die size may be reduced.
- The silicon electrode is self-aligned to the diffused electrodes, since this electrode is formed first in the masking process and thereby automatically defines the location of the other two electrodes. This self-alignment significantly reduces parasitic capacitances, increasing speed and allowing the transistors to be smaller.

Within the metal gate and silicon gate process technologies, there are three types of MOS transistors: P-channel, N-channel, and complementary. These devices in turn can operate in either of two ways: enhancement-mode or depletion-mode.

An enchancement-mode transistor is normally "off"; i.e., it does not conduct current unless voltage is applied to its gate electrode. This type of device consists of two diffusions (P, in this example) separated by a region of opposite polarity (N (see Figures 12-6 and 12-7)). The latter region is covered by a thin layer of oxide that is covered by metal or silicon.

When a voltage of the same polarity as the substrate (negative for N, positive for P) is applied to the gate, a thin layer of silicon (a few hundred angstroms (A) thick) under the gate oxide converts to the same polarity as the diffused beds. A "channel" is thus formed, connecting the two diffusions. This channel allows current to flow from one diffused bed (electrode) to the other. As the applied input voltage is increased, current flow increases or is "enhanced."

The channel of a depletion-mode device is formed during the manufacturing process. Figures 12-4 and 12-5 would be modified to show a shallow P layer under the gate oxide connecting the two P beds. With no applied gate voltage, these devices are normally "on" or conducting. If a gate voltage of opposite polarity to the substrate is applied, the carriers in the channel are reduced or "depleted" and the current diminishes.

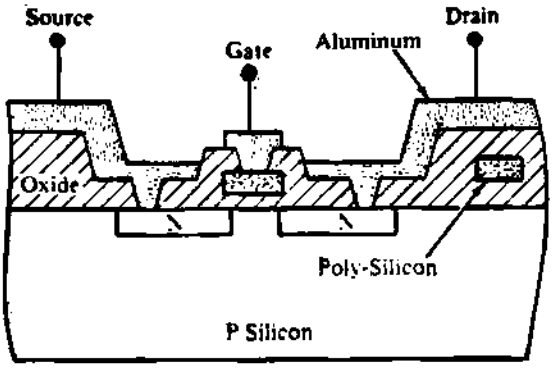
P-channel (PMOS) is the oldest of the three types of MOS devices and was the first MOS technology to become commercially available. The structure of this device is illustrated in Figures 12-4 and 12-5, where the diffused source and drain electrodes are P. A channel formed either by application of a negative voltage (same polarity as N substrate) or during the manufacturing process would be P. Thus, it is designated P-channel.

The N-channel (NMOS) structure is shown in Figure 12-6. It consists of two N wells diffused into a P substrate and separated by the gate electrode. In contrast to P-channel devices, the polarities of the dopants, carriers, and voltages are exactly reversed. The diffusion of a shallow N region connecting the two beds (depletion-mode) or the application of a positive voltage to the gate creates an N channel. N-channel presents three main advantages over P-channel devices:

- The speed is two to three times faster.
- For equivalent speeds, N-channel devices can be made smaller than P-channel devices.
- The polarities of applied and generated voltages and currents are consistent with bipolar devices.

Figure 12-6

N-CHANNEL
SILICON GATE TRANSISTOR



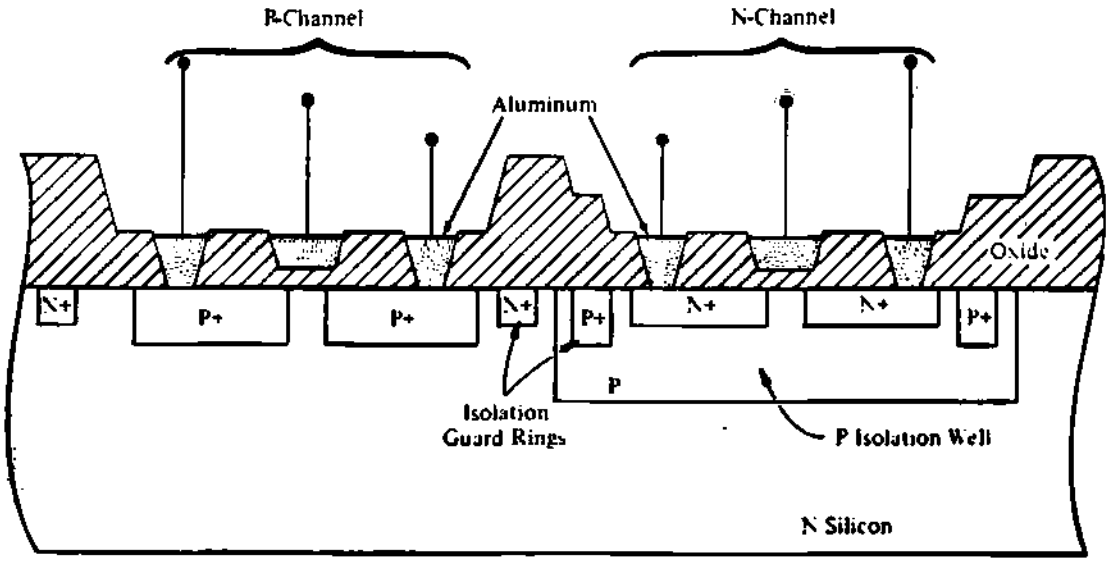
Source: DATAQUEST, Inc.
April 1982

The disadvantage is that N-channel devices are far more sensitive to minute amounts of contamination during the manufacturing, test, and assembly processes. This sensitivity can reduce yields and create reliability problems. Most suppliers, however, have found that the silicon gate process substantially reduces N-channel MOS sensitivity to contamination, as compared with the metal gate process.

CMOS transistor pairs consist of one N-channel device and one P-channel device connected as indicated in Figure 12-7. The PMOS transistor replaces the diffused or MOS resistor usually used in an NMOS circuit and operates such that it is "off" when the NMOS device is "on" and vice versa. Consequently, the CMOS device consumes much less standby power than a single-polarity device, since the two transistors are in series and one is always "off".

Figure 12-7

METAL GATE CMOS TRANSISTOR



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Other advantages of CMOS over NMOS and PMOS are:

- The input signal always forces one transistor to turn "off" while forcing the other to turn "on." This active participation of both transistors makes CMOS faster for equivalent functions and processes.
- CMOS is less sensitive to electrical noise on the input signal.
- CMOS devices can operate over a wider range of power supply voltages.

The disadvantages relate predominantly to processing. CMOS processes are more complex than NMOS and PMOS processes because of the need to fabricate both types of transistors on the same substrate. Second, the use of two transistors causes additional silicon real estate to be consumed to form the P isolation well and the guard rings that protect against parasitic interaction between the two devices. As a result, CMOS devices are more costly.

Planar Processing

Processing of integrated circuits starts with a polished, virtually defect-free semiconductor wafer that was sliced from a grown silicon crystal. A four-inch or 100-millimeter (mm) wafer is typically 20 mils thick.

Planar processing is used to manufacture bipolar ICs as well as MOS ICs. A brief discussion of bipolar IC component processing illustrates how transistors, diodes, resistors, and capacitors may be formed using a common set of steps, as shown in Figure 12-8.

The structure of bipolar circuit components is shown in Figure 12-8. We have chosen to limit the discussion to this epitaxial approach, since it is the predominant bipolar IC process technology at present.

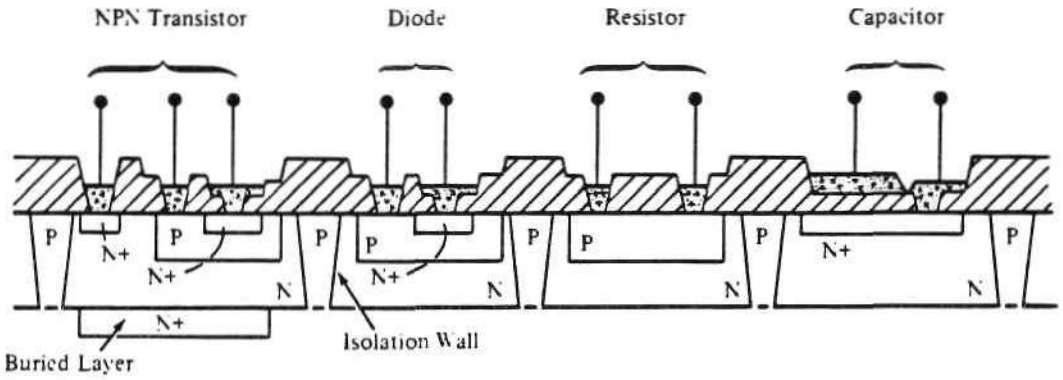
This transistor structure differs from that of the mesa transistor in two significant ways:

- The transistor now has a highly conductive N+ "buried layer" that is formed prior to deposition of the epi layer. This N+ layer provides a lower resistance path for electrons to flow to the collector contact than the thin N layer under the base. The result is improved electrical performance over that of the triple-diffused transistor.

- A P "isolation" well has been diffused through the epi layer to the P substrate surrounding the sites where the components are to be formed. As shown in the figure, the N epi layer and its corresponding buried layer are now completely surrounded by P silicon and are "isolated" from other similar N epi islands.

Figure 12-8

BIPOLAR INTEGRATED CIRCUIT COMPONENTS



Source: DATAQUEST, Inc.
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Other components of the circuit are formed as follows:

- Diode—The planar diode is formed basically as a transistor without the buried layer and with only two electrode connections, as shown in Figure 12-8. It is a junction consisting of N+ for one electrode and P for the other.

- Resistor—The diffused planar resistor is created simultaneously with the formation of the transistor base region. Its value depends on its length, width, and dopant concentration. The longer and narrower its geometry, the higher its resistance value. The lower the dopant concentration, the fewer carriers are available to conduct current; hence, the higher the resistance to current flow. Resistors are used to limit current flow and to adjust voltage levels.

- Capacitor—A capacitor is formed by sandwiching metal (aluminum), a thin layer of oxide, and an N+ layer formed during the diffusion of the emitters. The oxide does not conduct current when voltage is applied between the metal and the N+ electrodes. Instead, it behaves like a "bucket" that stores charge, the amount of charge being directly proportional to the applied voltage.

Components may be interconnected in a number of combinations, depending on the circuit design and the desired electrical function. Interconnection of the respective electrodes by the metallization (and sometimes polysilicon and diffusion) patterns forms the final circuit function. Most bipolar circuits are divided functionally into two categories—digital integrated circuits and linear or analog integrated circuits; digital ICs can be further subdivided into logic devices and memory devices.

Other circuit components are easily formed during planar IC processing. In addition to diffused resistors and capacitors, it is possible to make resistors and capacitors by taking advantage of the electrical properties of silicon dioxide, polysilicon, nitrides, various metal elements, and metal alloys. For example, a fuse link in a PROM is a low-value resistor formed by a thin strip of metal or polysilicon. Capacitors may be formed by using a metal interconnect layer as one of the capacitor plates, separated from a second layer plate of metal or polysilicon using an intermediate insulator such as silicon dioxide. In very-high-frequency circuits, the inductive properties of the various semiconductor structures become important components and must be factored into the design.

In the process of integrating thousands of transistors, diodes, resistors, and capacitors on a single die, measures must be taken to ensure that the components will not interact electrically in undesirable modes. Moreover, additional process steps are added to improve specific transistor and circuit performance characteristics.

As the level of integration increases, IC design must account for the interactions of adjacent components. Occasionally unintended interactions that go unnoticed until a product is running in high-volume production, can be the cause of very expensive, time-consuming production changes. Many computer-aided design (CAD) techniques attempt to eliminate this type of problem, but the effectiveness of such aids remains a function of the quality of the design team's efforts.

Figure 12-9 illustrates a typical N-channel wafer fabrication process flow chart. The various operations listed are described in detail by the manufacturer's internal (usually proprietary) specifications. Such flow charts include special instructions to the operator to maintain the quality and integrity of the process. Quality control and quality assurance provisions are not included in the sequence of steps shown here.

Figure 12-9

SAMPLE PROCESS FLOW CHART[1]

Process: N
Technology: N-channel, Silicon Gate

Division: MOS

Revision: A
ECN # : 306
Orig. : J. Doe
Date : 1-1-74

Operation	Spec. Ref.	Special Instructions
1. Raw Wafers	10001	3-4 ohm-cm, (100)-orientation
2. Initial Clean	20001	10 minutes
3. Initial Oxidation	20002	1150°C, 1 hr. 40 min., wet O_2. T_{ox} = 10,000A
4. Mask: P-Beds	30001-6,9	6 min. Buffered HF
5. Gate Oxidation	20003	1150°C, 40 min. dry O_2 + 15 min. dry N_2. T_{ox} = 1350A
6. Poly Deposition	20004	Thickness = 5000A ± 500A
7. Oxidation	20005	1100°C, 55 min., T_{ox} = 1200A
8. Mask: Gate	30001-5,7,9	
9. Phosphorus Deposition	20006	V/I = 1.0, 1075°C, $POCl_3$
10. Field Vapox Deposition	20007	9000A ± 1000A
11. Anneal	20008	1100°C, 20 min., dry N_2
12. Mask: Contacts	30001-6,9	
13. Aluminum Evaporation	20009	6-9's pure, 12,000A ± 1000A
14. Mask: Metal	30001-5,8	
15. Glass Deposition	20010	9000A ± 1000A
16. Mask: Pad	30001-6,9	
17. Alloy	20011	450°C, 30 min.
18. Wafer Evaluation	20012	V_{to} = 1.8 – 2.2V, $BV_{DSS} \geq 25V$, $V_{TM} \geq 25V$, $V_{TP} \geq 25V$

[1] For illustration only; not intended to describe a working process

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April 1982

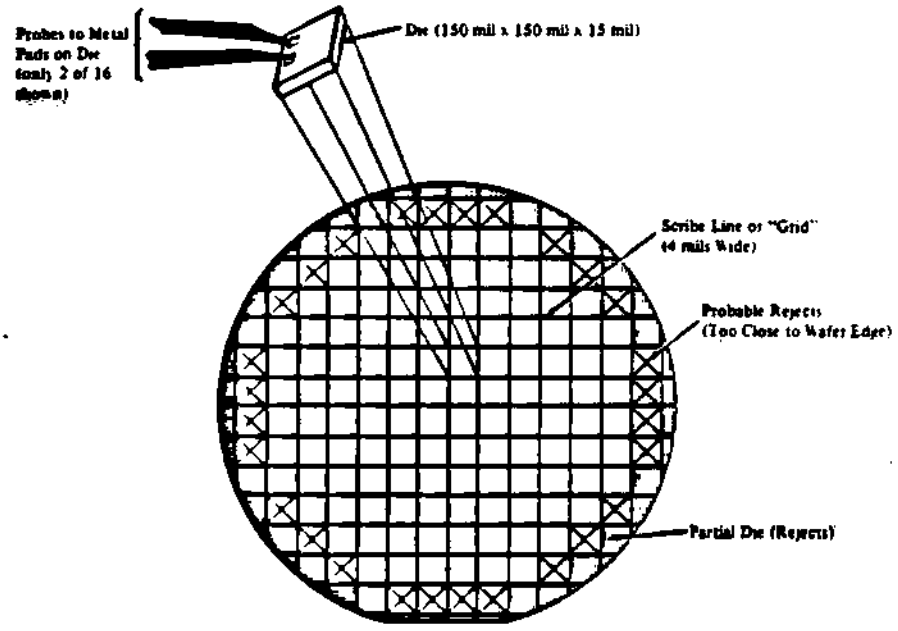
Wafer Test

After fabrication, wafer-sort testing is performed to identify electrically good candidate dice to be packaged. The wafer-sort test is also referred to as "electrical sort," "E-sort," "wafer probe," or "probe." Figure 12-10 shows the technique used to accomplish this. The bad dice are dotted with magnetic ink to allow easy removal later on—in the early part of the assembly operation. The objectives of wafer-sort testing are:

- To reject potentially bad dice, so that no additional costs (such as assembly) will be incurred by them
- To subject each die to a test stringent enough to assure a better than 70 percent chance of passing final test when it reaches that point
- To feed information back to the wafer fab area on potential processing problems, particularly if the wafers have an inordinately high number of rejected dice

Figure 12-10

WAFER SORT



Source: DATAQUEST, Inc.
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Assembly

This section describes the assembly processes used in packaging a 64K RAM after it has been tested in wafer form. A typical assembly flow is illustrated in Figure 12-11 and is described below.

Wafers are received from the wafer sort area and the bad dice have already been marked with magnetic ink. The wafers are placed onto scribers, which are machines that automatically pass a diamond needle along "grids" on the wafers. These grids were outlined in the circuit pattern during the masking operations and delineate the boundaries of the rectangular dice. The purpose of this process is to lightly score the silicon surface (to a depth of 0.001 to 0.002 inches) so that the wafer may be easily broken along the scored lines. This process is very similar to that used by glass workers when they score flat glass plates with a diamond tip to cut them.

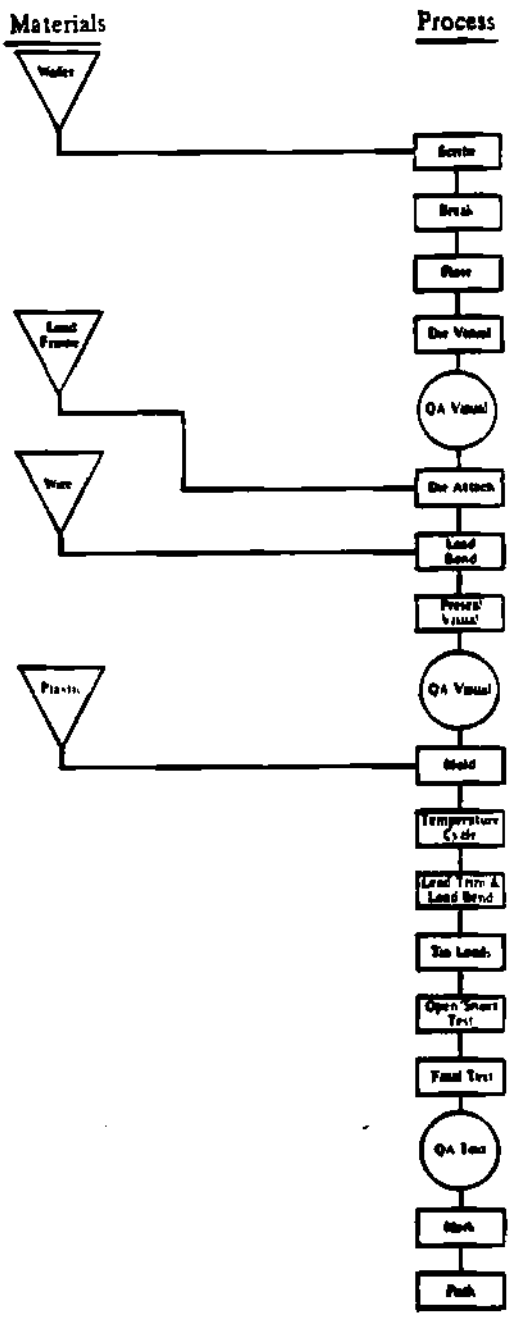
Recently, laser scribers have been used, with the laser beam performing the "scribe." Lasers offer lower breakage loss and greater productivity. However, the heat generated by the laser has caused some reliability problems with N-channel silicon gate devices. Even more recently, wafer saws have become popular. These units actually saw the wafer using a diamond impregnated saw blade. Sometimes the wafer is sawn completely through and sometimes the saw cut (kerf) is only part way through the wafer ("scribe mode"). Sawing is popular for thicker wafers that do not scribe and break well. It is also popular for very small dice since the allowance for saw kerf can be much smaller than that for the normal scribe line. This process greatly increases the number of die per wafer for small die since the space between dice occupies a large percentage of the wafer area.

After scribing, the wafers are placed on flexible holders and aligned so that one set of parallel scribe grids is registered against a fixed calibration mark. The holder and wafer are fed into a machine (wafer breaker) that flexes the holder and wafer around a fixed radius, so that the wafer breaks along one set of grids. The process is similar to running the wafer and holder through the wringers on an old-fashioned washing machine. After the wafer is broken in one direction, the holder is turned perpendicular to the first pass and put through the flexing process again, to break it along the second set of scribe lines. When the wafer comes out of this second pass, all the individual circuits have been separated and each circuit is now referred to as a "die." Sawn wafers do not have to be broken.

The operator separates the good and reject dice at this point, using a magnetic pick-up tool. All rejected dice, with ink dots on them, are discarded and all good dice are placed in orderly rows on a square plate. This operation is not necessary if sawn dice are cut from wafers backed with sticky tape. This tape holds the dice in position. The plate of dice is placed under a microscope and each die is inspected according to preset visual quality criteria. Gross contamination, scratches, and broken dice are reasons for rejection.

Figure 12-11

ASSEMBLY WORK FLOW



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April 1982

The good dice are now mounted into packages. An empty package frame is placed on a heating block and heated to 400°C. In some cases, a thin square of gold, slightly smaller than the die itself, is then placed on the package where the die is to be attached. Most companies, however, do not use this approach, but purchase packages with thicker gold on the die bond area to save time and labor. The die is gently lifted and placed onto the thick-plated gold area. The gold immediately becomes a conductive "glue" that holds the die to the package. Recent developments in package technology have reduced or eliminated the gold content.

Bonding is accomplished in either of two ways. Due to its superior strength, gold wire is used in plastic packages to connect the individual 4-mil x 4-mil aluminum pads on the die to the corresponding leads on the package. For ceramic packages, either gold or aluminum wire is used.

In gold bonding, the package is heated to 340°C. The assembly equipment positions the tip of a gold wire directly over a pad on the die. When the alignment is complete, the gold wire (0.001 to 0.0015 inches in diameter) is forced down on the pad and a thermocompression bond is made. Gold wire is then trailed out to a point over the corresponding pad in the package. Again, after alignment, the wire is brought down on the package pad and the excess wire is automatically severed on the pad. This process is repeated until all pads on the die have been bonded to the corresponding package pads.

In aluminum bonding, the basic bonding operation is the same except that, instead of heating the package, ultrasonic agitation of the wire is used to make contact with the pads by a "scrubbing" action.

By 1976, microprocessor-controlled automatic bonders had become popular. In the early versions of these machines, the operator bonded only the initial unit. After that the machine "remembered" where to place the bonds on subsequent dice and packages. On the most recent automatic bonding equipment, even the initial orientation is accomplished automatically.

Preseal visual inspection is performed to screen out any units that may have been damaged during the previous assembly steps. Unbonded pads, broken wires, chipped dice, and loose dice are reasons for rejection.

Plastic packaging is currently the lowest cost of all methods of semiconductor encapsulation. In this method, the frame holding the die is placed in a mold, and molten plastic is injected into the mold to form the package body. After removal from the mold, the packages are cured in an oven at approximately 200°C.

Ceramic packages must be sealed with a metal lid to make them airtight. Different methods are used, but all require heating the device (with the lid) in a sealing furnace.

The units may then be temperature cycled, usually five times at temperatures between -55°C and +150°C to check for lead bond integrity. This is normally done on a sample basis for commercial grade products.

The centrifuge test is sometimes used for ceramic or metal packages. In this test, a centrifuge is used to accelerate the packages to 30,000g to stress the leads and bonds. This check not only tests for mechanical integrity, but also serves as a screen to determine whether the bonding wire is too close to the bottom of the lid, thereby representing a potential circuit failure. This test is not performed on plastic packages because the leads are buried in the plastic encapsulant.

The purpose of the leak test is to ensure that the lids are properly sealed to the package so that the die is protected from ingression of contaminants. Fine and gross leak tests are not necessarily performed on plastic packages that have no cavities.

Until this point in the assembly process, the plastic packages are connected by additional metal between the leads on the packages. At this step, a special lead trimmer cuts off this extra metal, separating both the packages and the individual leads on each package. The leads are then bent at angles of approximately 90 degrees to the bottom of the package.

The open-short test is a simple electrical test (usually performed on a homemade test set) that checks package leads to determine whether any are electrically shorted together or are open. It is performed primarily by assembly plants as a monitor of assembly quality.

Figure 10-1 and Figures 10-6 through 10-9 in Section 10 show examples of the various semiconductor package types currently in use.

Final Test

The final test is performed after the dice have been packaged. Since the packaged units now have external leads that operators or machines can handle, this process is usually automated. The packages are received from assembly in long plastic tubes, with the units stacked end-to-end. Each tube is placed vertically, one end down, in an automatic package handler. The handler, in turn, releases one package at a time, allowing it to slide to a set of contacts that match its leads. The contacts are wired to the automatic tester.

Each unit is stringently tested at this step, across "worst case" conditions. The circuits are exercised for maximum and minimum speeds, for power dissipation, and for many combinations of inputs and outputs—i.e., they are tested to ensure that they will meet all of the manufacturer's specifications and guarantees. Literally thousands of separate tests are performed in a matter of seconds by the sophisticated automatic test equipment. A typical final test by the manufacturer runs from less than one second on a TTL logic device up to twenty seconds or more for some 64K RAMs.

Since most circuits are guaranteed to operate over certain temperature ranges, final test must be stringent enough to ensure that the performance standard will be met. The environmental conditions are usually assured in one of two ways:

- All devices are tested at the high-temperature end of the specification, or
- The devices are tested at room temperature over sufficiently wide tolerances (guard bands) so that operation at the temperature extremes is assured.

The first approach is obviously the safer, but it is also expensive in terms of labor and the amount and type of test equipment required. As a result, many semiconductor manufacturers will correlate the room temperature characteristics with the characteristics at temperature extremes, add a safety guard band to the room temperature test parameters, and then test at room temperature. Samples are taken regularly from the production lots and tested across the full range of environmental conditions to ensure that the correlation continues to be accurate.

Interrelationship of Wafer Sort and Final Test

There is a very close interplay between wafer sort and final test. In fact, in many operations, both test activities are located in the same room and often the same equipment is used for both; only the test programs are different.

As mentioned earlier, one of the functions of wafer sort is to minimize the amount of additional labor and materials that would be assigned in producing bad circuits. This factor is especially important for semiconductors with lower die costs and, therefore, relatively higher assembly costs. However, wafer sort cannot eliminate all potentially defective dice for several reasons:

- Most sophisticated circuits, such as the 64K RAM, cannot be completely tested in wafer form because of the parasitic effects resulting from the probes and wiring, incident room light, and other factors.
- Some of the dice may be damaged during the entire assembly process.
- The dice cannot be tested across the temperature range in wafer form because the wafer (and contact probes) cannot be easily maintained at temperatures below ambient.

The objective of wafer sort is to ensure that enough of the potentially rejectable circuits have been discarded so that final test yields will be high enough to support the desired level of profitability. Excessively high final test yields are not necessarily acceptable. This may mean that potentially good devices are being thrown away at wafer sort. As a result, many manufacturers will adjust the tightness or severity of their wafer-sort tests to allow the final test yields to fall in the range of 70 to 85 percent good units.

Manufacturing Support Activities

To this point, no mention has been made of the other support groups that are vitally important to the success of the manufacturing operations. We will briefly discuss the key support groups.

Circuit or Product Design

The function of the design group is to take marketing and customer inputs and design the circuits needed to perform the desired electrical functions. The inputs take the form of a specification of a function to be performed. The design group then determines the best circuitry and technology to generate the function. A designer simulates the circuit, section by section, on a computer-aided design (CAD) system to determine the optimum design. The circuit is designed using the outputs of these simulations, and photomasks are generated for use in the manufacturing area.

Product Engineering

Product engineering is generally considered to be an integral part of the manufacturing operation, even though circuit design is not. The function of the product engineer is multifaceted and, in many respects, is one of the most important functions in the manufacturing operation.

The product engineer works with the circuit designer as a product is being conceptualized and designed. As the circuit reaches the hardware stage in the form of wafers, the product engineer either writes the electrical test programs for wafer sort and final test or aids the designer in writing them. After the first devices are obtained, the product engineer is responsible for fully characterizing the circuits over the full performance range to ensure that they meet the specifications.

Once the product has been released to the manufacturing area, it is the product engineer's responsibility to ensure that it continues to be manufactured economically, and that there are good yields. The product engineer's other responsibilities include:

- Resolving wafer-sort problems
- Assuring that wafer-sort specifications are met

- Resolving final test problems
- Ensuring that the product is and continues to be reproducible

The product engineer who neither designs nor manufactures the product is in a unique position for coordinating the communication between these two areas, and for isolating problems and determining whether a reject is process related or design related. This function is important because most process engineers have limited knowledge of designing circuits, and most designers have limited processing knowledge.

Process Engineering

Process engineering comprises manufacturing or sustaining engineering and process development.

Sustaining engineering is usually just that—solving the day-to-day problems as they arise so that production can be sustained. It is commonly referred to as "fire fighting." In most companies, the function of sustaining engineering is to "keep the product running." Like the product engineer, the process engineer is often faced with the problem of maintaining a high level of quality versus "getting products out the door."

Process development, in a manufacturing operation, relates to short-term work aimed at desensitizing a particularly troublesome process, improving productivity through a process modification, and developing other methods of lowering costs (methods for reducing chemical usage, etc.).

Quality Assurance

The function of Quality Assurance (QA) is to ensure that documentation is maintained on every process, that controls are established at the critical steps, that the controls are monitored (and meaningful), and that warning flags are raised when out-of-specification conditions occur. These responsibilities hold throughout the manufacturing operations, including assembly and test.

Quality Assurance is extremely important in any manufacturing process, especially in MOS manufacturing. Since an MOS circuit or transistor cannot be tested until the last step of the process, many process controls are implicit. That is, test wafers are run through individual process steps to qualify that process as being "in specification." The production wafers are then put through the process based on the observation that the test vehicle met the proper specifications. In other IC processes, it is often possible to measure the results of that process step directly on the production wafer as soon as it comes out of the process. In MOS, one assumes or infers that the product is "within specification" because the test vehicle was within the specified tolerances.

Obviously, the interpretation of "in specification" may vary considerably among operators, foremen, and engineers. It is QA's responsibility to limit that interpretation by maintaining uniform standards, specifications, and tolerances.

Equipment Maintenance

Maintenance and preventive maintenance are becoming important functions in wafer fabrication operations. Process equipment and test equipment are becoming more sophisticated all the time. Process equipment contains many of the same integrated circuits that it builds, and testers have become small special-purpose computers. Each of these must be continually maintained and repaired so that the manufacturing operation can run smoothly and economically.

Facilities Maintenance

Facilities maintenance was discussed in detail in Section 11, Captive Decisions. Among the major functions performed are environmental control (temperature, humidity, and particulates); purity of gases, DI water, and chemicals delivered to the fab area; and regulation of the pressures of gases for pneumatic and processing functions, as well as proper disposal of all wastes. It is evident, therefore, that the preventive and on-going maintenance provided for the facilities is critical.

SEMICONDUCTOR DEVICES

This part of Section 12 discusses specific semiconductor device types, their uses, and the way they function.

Discrete Semiconductor Components

A discrete semiconductor is an individual semiconductor circuit element packaged as a single device. This is in contrast to an integrated circuit that is equivalent to several discrete components (many thousands in the case of VLSI devices). This section discusses the uses and functions of diodes, thyristors, and transistors.

Diodes

When a P semiconductor and an N semiconductor are brought into contact, a P-N junction is formed. The P-N junction allows electrons to flow from N to P when a forward bias voltage is applied but impedes the flow from P to N when reverse-biased. Such a semiconductor is called a diode.

A diode is a two-terminal device that conducts current in one direction but not in the other. In semiconductor technology a diode is formed by a P-N junction, usually fabricated in silicon. A single diode per silicon chip is called a discrete diode.

Small-Signal Diodes - Small-signal diodes (which DATAQUEST defines as diodes rated at less than 1 ampere current handling capability) are the basic building blocks of electronic circuits. They can function as switches, demodulators, or variable resistors.

Zener Diodes - A reverse voltage applied to a zener diode causes it to break down at a specific voltage. Because this voltage can be accurately determined, these devices are used as voltage references and voltage regulators. At the breakdown point (zener voltage), the resistance of the device drops dramatically, requiring that a series resistor be used to limit current flow to prevent damage.

Power Diodes - A silicon P-N junction capable of high current operation is called a power diode or silicon rectifier. Rectifiers are mainly used in power supplies as a means of converting alternating current to direct current. DATAQUEST defines a power diode as a discrete diode capable of operating at 1 amp or higher. Ratings of some currently manufactured power diodes exceed several hundred amperes. The power diode typically has a forward resistance of less than one-half ohm, and a reverse resistance of several million ohms (megohms). Because of their high operating currents, power diodes generate a lot of heat and require a "heat-sink" to avoid damage. This is accomplished in many cases by stud-mounting.

Tunnel Diodes - Tunnel diodes are made from germanium, silicon, or gallium arsenide, and are used in such applications as detectors, amplifiers, and oscillators. A P-N junction capable of negative resistance may be formed by heavily doping both the P and N regions so as to generate a thin depletion layer. This results in an effect called tunnelling, which allows a relatively large current flow at very small forward bias voltage.

Light-Emitting Diodes (LEDs) - Light-emitting diodes may be used either as individual lamps or in matrix displays to form intelligible characters in such applications as electronic games, calculators, or digital clocks. By carefully controlling the construction of certain GaAs diodes during manufacture, it is possible to operate the resultant semiconductor in the reverse-biased breakdown region and cause it to emit light. Gallium arsenide phosphide devices usually emit red light, and gallium phosphide gives green light.

Photodiodes and Phototransistors - Photodiodes and phototransistors are used in light- and infrared-sensing applications. Because the phototransistor is an amplifier, it is more sensitive to a given intensity of light than a photodiode of similar construction. If a P-N junction of appropriate construction is exposed to light, the photons from the light beam cause a small current to flow (photocurrent). The greater the light intensity, the greater the resulting photocurrent. If the P-N junction is part of a transistor, the device is called a phototransistor. If not, it is called a photodiode.

Optocouplers - An optocoupler, also called an optoisolator, consists of a light-emitting diode optically connected to a photo-detector. This configuration allows signals to be transmitted while providing virtually perfect electrical isolation.

Thyristors

Thyristors, also called silicon-controlled rectifiers, are useful as power switches because they can control very high currents (10 to 100 or more amperes) with very low signals. A thyristor is a P-N-P-N device constructed on a silicon die with the intent of operating it as a gated current switch. A forward bias current flowing through the junctions causes the voltage drop across the device to decrease (breakover) to a very low level. The current flow is then limited by the series impedance in the circuit. The breakover voltage can be varied by injecting a control current (signal) at one of the intermediate nodes.

If both of the intermediate nodes are gated with low-level currents, the resulting device is called an SCS (silicon controlled switch). SCSs are used primarily in low-power digital applications as logic switches.

Schottky Barrier Diodes

Schottky barrier diodes have very fast turn-off capability and low noise properties. For these reasons they are useful as detectors where high sensitivity is required, in low-level detection voltage instruments for example. Schottky barrier diodes are formed by depositing a suitable metal—such as platinum, aluminum, or molybdenum—on a semiconductor surface, thus forming an effective junction with relatively high-resistivity semiconductor materials. They are used in high-speed transistor-transistor logic (TTL) as clamping diodes to enhance speed.

Transistors

The term "transistor" is a contraction of the phrase "transfer resistor," which describes the apparent function of such a device in an electronic circuit. The earliest transistors were formed by closely spaced wire springs contacting a semiconductor surface, and were called point-contact transistors.

Bipolar Transistors

The term "bipolar" defines a class of semiconductor devices in which the conduction of electrical current is via two oppositely charged carriers. One of the carriers is negatively charged (negative polarity) and is called an electron; the other is positively charged (positive polarity) and is called a hole. Both carriers contribute to the total flow of current. In contrast to MOS devices, which are discussed later, the critical flow of current in a bipolar device takes place within

the bulk silicon substrate rather than at the silicon surface. Consequently, bipolar devices have been relatively insensitive to the surface contamination that degrades MOS yields and reliability.

In the manufacture of transistors it is possible to form P-N-P junctions or N-P-N junctions, depending on the impurity doping material used. Most junction transistors today are constructed of silicon, and, like diodes, may be formed by alloying or diffusion. Diffusion is preferred for most applications because it provides better control over physical and electrical characteristics of the resulting transistors.

Transistors formed by early diffusion methods were called mesa transistors, because each of the N-P-N layers extended to the edges of the die. A modification of the diffusion process in the late 1950s led to planar construction, where each of the three junctions is brought to a common layer or plane. The properties of planar transistors are more easily controlled than those of mesa transistors because the junctions may be protected beneath silicon dioxide or another insulating layer. The planar process led to the invention of the integrated circuit, which is discussed later in this section.

Bipolar transistors are essentially current-mode (current-amplifying) devices. A bipolar transistor consists of three electrodes called emitter, base, and collector. A small emitter-base current induces a larger (amplified) emitter-collector current. Typical voltage drops under saturated current-flow conditions, in a silicon switching transistor for logic circuit application, are 0.7 volts (base-emitter) and 0.3 volts (collector-emitter), and typical collector current multiplication or gain is 10 to 50 times the base current. Actual size of such a transistor is less than 50 square mils of chip area.

DATAQUEST defines bipolar transistors rated at one watt or less as small-signal transistors; silicon and germanium transistors rated at greater than one watt are defined as power transistors. These include microwave, radio frequency (RF), and Darlington power transistors.

Field-Effect Transistors (FETs)

Field-effect transistors are used in switching power supplies, in inverters for motor control, and in radio-frequency amplifier applications.

The two types of field-effect transistors are called junction FETs (JFETs) and insulated gate FETs. The predominant device today is the insulated gate metal-oxide-silicon or MOS FET. Its name is derived from the key elements used in its manufacture. Field-effect transistors are voltage mode transistors, usually manufactured using a metal-oxide-silicon (MOS) process.

Like the bipolar transistor described in the previous section, MOS transistors are generally three-terminal devices. The controlling electrode is called a "gate" (not to be confused with the logic circuit) consisting of a sandwich of metal, oxide, and silicon. The gate is similar to the base of a bipolar transistor in that it controls the flow of current from one electrode to the other. The other two electrodes are the "source" and "drain," which are analogous to the bipolar emitter and collector. The source is the electrode from which carriers flow, and drain is the electrode where they are collected.

Unlike bipolar transistors, MOS devices are "unipolar" and bilateral. Current is conducted by either positive or negative carriers, but not both. The device is symmetrical about the gate, such that the source and drain are the same and therefore are interchangeable. Current conduction takes place at the surface of the silicon rather than within its bulk; thus, MOS devices are far more sensitive to surface effects. Finally, current flow is modulated by a voltage applied to the control or gate electrode of a MOS transistor, rather than by a current.

There are two basic processes or technologies for producing MOS circuits: metal gate and silicon gate. Metal gate is the oldest of the MOS technologies, dating back to 1963 when the first discrete transistors were offered. By the mid-1960s, with the development of planar processing, it became possible to integrate hundreds of MOS transistors on a single die. Thus the MOS LSI era was born.

Integrated Circuits (ICs)

The planar process made possible the formation of many transistors on a single chip or die of silicon. This quickly led to the invention of the integrated circuit (IC), which incorporates transistors, diodes, resistors, capacitors, fuses (when desired), and interconnections all on a single die.

By using a sequential combination of photolithographic and high-temperature chemical processes, tens of thousands of circuit elements may be produced simultaneously on a single die. Each four-inch wafer may contain several hundred dice (depending on die size). The wafers are processed in batches through each manufacturing step. The cost of producing a die can be low because of the low labor content per device that results from batch processing. Moreover, each die occupies very little space and consumes minimal amounts of power. This approach is contrasted with previous techniques that required tedious hand soldering of hundreds of individual discrete components onto a printed circuit board. Today, ICs containing more than one million components are being fabricated on silicon chips that are less than 0.3 inch per side.

Digital Integrated Circuits

Digital ICs operate on a binary number system. The binary system permits only two possible states, "1" or "0." The "1" may be represented by the presence of a voltage and the "0" by the absence of a voltage, or any other present/absent, on/off, or yes/no relationship. For example, a light switch may be considered to be a simple digital "system." The light is on if the switch is up, and off when it is down. Regardless of the physical or electrical process involved, each "1" or "0" is referred to as an information "bit." The function of the digital circuit is typically to perform a logic operation, i.e., perform operations on binary signals.

Returning to our example of the light switch, suppose that the light is controlled by two switches, one in the room and one at the circuit breaker box. For the light to go on, both switches must be up simultaneously; i.e., the room switch AND the breaker switch must be up. In other words, if both switches are "on" (1s), then the light is "on" (1). This example serves as an analogy for a very simple digital logic circuit, called a two-input AND "gate." The circuit works on the same principle: if both applied inputs are "on," the output will be "on," but if either of them is "off," the circuit will be "off." These simple switches are the basic building blocks for all computer logic circuits.

Bipolar transistors function extremely well as electrical "switches." If no current is applied to the input or base of the transistor, no current flows through the collector, and the transistor is "off." Conversely, an excess amount of current applied to the base (over and above that needed to turn it "on") forces both junctions to conduct current readily, and the transistor is fully "on." A transistor operating such that both junctions are fully conducting is said to be in the "saturated" mode. This operation is typical of the bipolar logic families that are available at present.

The digital circuits available today are far more sophisticated than our simple light switch example. A digital IC may have hundreds or thousands of gates on a chip, interconnected so that the information may be processed through a number of parallel and serial logical operations before the outputs are determined. These operations or calculations can be performed in billionths of a second (nanoseconds), with the small consumption of power measured in thousandths of a watt (milliwatts). Small, high-speed computers are available today because of these digital ICs. To meet the needs of users, semiconductor manufacturers have developed various families of digital integrated circuits.

Digital Logic Families

Two circuit performance measures—speed and power dissipation—are critical and should be observed closely. As speed increases, so does power dissipation. Most users of ICs would like as much speed as possible for their particular application. However, the increased power dissipation is a problem because the cost of removing the generated heat is very high. Consequently, the user is forced to make a compromise between speed and power dissipation, depending on the application. Table 12-1 shows typical operating speed and power usage of several types of ICs. The burden of resolving the speed-power dilemma is on the semiconductor manufacturers, who have responded by generating the types of standard logic families summarized in the following text.

Table 12-1

OPERATING SPEED AND POWER CONSUMPTION
FOR A TYPICAL LOGIC GATE (DRIVING EXTERNAL LOADS)

Circuit	Speed (ns)	Power (mW)	Speed-Power Product (pJ)
Standard TTL-54/74	10.0	10	100
Schottky TTL	4.0	15	60
LS TTL	6.0	2	12
ALS	5.0	1	5
CMOS-4000	25.0	1	25
ECL-10K	2.0	25	50
ECL-100K	0.7	30	20

Source: DATAQUEST, Inc.
April 1982

Transistor-Transistor Logic (TTL)

Transistor-transistor logic (TTL) is the most popular form of standard logic circuit today. Unlike other logic or linear circuit forms, a single transistor with multiple emitters diffused into the base handles the signal inputs to the circuit. Each emitter serves as an input, and the collector of the first transistor transfers the resultant signal to the base of a second transistor; hence, the description transistor-transistor logic.

The multiple emitter structure eliminates the need for the resistors and diodes that are required in other input structures, and provides a significant space saving. At the time of its introduction in the early 1960s, TTL offered the significant advantages of higher speed and lower power dissipation over the existing logic families. However, it did not become cost effective until the late 1960s. During the past decade, TTL has become the dominant logic family. Its primary competition has been from variations on the basic TTL concept that improve speed and power dissipation.

Schottky TTL

This standard logic family stems from process evolution in the early 1970s. It represented a significant step forward in achieving higher speeds without the attendant substantial increase in power dissipation. It is a modification of, and is electrically compatible with, the standard TTL family.

The Schottky TTL circuit uses a Schottky diode connected between the base and collector of each of its transistors. This special diode prevents excess charge from being forced into the base of the transistor when it is first turned on, thus preventing the transistor from becoming saturated. Because it is not forced into saturation, less power and time are required to turn it on and off. Furthermore, less power is dissipated while the transistor is on, and there is a threefold increase in speed over standard TTL, with a penalty of increasing power dissipation by only 50 percent.

Low-Power Schottky TTL (LSTTL)

Low-power Schottky TTL is an addition to the standard TTL families that became popular in the mid-1970s. This product line succeeds in combining most of the benefits of the two previous families. Power dissipation is reduced by using high-valued resistors, and Schottky diodes are incorporated for fast switching characteristics. The result is a family that operates at a speed higher than that of standard TTL, with only 20 percent of the TTL's power dissipation.

Advanced Low-Power Schottky TTL (ALS)

ALS logic is the most recent addition to the standard TTL logic families. ALS offers the following advantages over other TTL forms:

- Improved speed—3 to 5 nanoseconds gate delay
- Low power—one-third to one-half less than LSTTL power
- Higher complexity functions—some MSI not in standard TTL family

ALS is already multiple sourced by Motorola, National, and Texas Instruments, with others expected to follow.

Emitter-Coupled Logic (ECL)

Commonly referred to as ECL, emitter-coupled logic families consist of circuits in which the transistors are not driven fully on ("saturated"). ECL circuits are designed for high-speed performance and are more than 30 percent faster than Schottky TTL products. Because it is designed to drive low-impedance transmission lines, each logic gate draws power continuously, and this power is increased as each of the inputs is turned on. Consequently, the higher speed is combined with a substantial increase in power dissipation. ECL circuits dissipate 50 to 100 percent more energy than Schottky TTL, which limits their use to more specialized applications where speed is of paramount importance. The two most popular ECL families are ECL 10K and ECL 100K, which have typical gate propagation delays of 2ns and 0.7ns, respectively.

Integration Injection Logic (I^2L)

I^2L is a form of logic that uses common emitter N-P-N transistor gate structures. Base drive is provided by a lateral P-N-P transistor. Since the collector of the P-N-P can be the same P region as the base of the N-P-N transistor, I^2L is compatible with other bipolar forms of logic. Another, possibly more important, benefit is that I^2L is compatible with many forms of analog circuitry. This characteristic allows the designer to incorporate high-density digital logic capability with linear or other analog circuitry on the same die. Typical I^2L functions include gates, flip-flops, counters, decoders, multiplexers, and other complex logic forms.

I^2L gates are usually formed by diffusing more than one collector into the P base. This capability improves the fanout capability and the flexibility of I^2L logic. Because of this feature, I^2L logic may also be referred to as merged-transistor logic (MTL).

Programmable Logic

Several approaches to semiconductor logic circuits allow the user to take advantage of the density and complexity of MSI/LSI and the flexibility of programming after the devices have been shipped from the supplier's facility. These include field-programmable logic arrays and gate arrays (FPLAs and FPGAs), and programmable array logic (PAL, a trademark of Monolithic Memories, Incorporated). Of these devices, the PAL has become the most widely accepted. A PAL is a combination of PROMs and MSI logic elements on a single chip. The advantage of the PAL is more efficient integration of digital functions into less space at lower power, reducing parts count and costs. The PAL family has grown to more than 20 device types. They can be programmed to duplicate the functions of the majority of MSI device types, and the family is alternate-sourced.

Gate Array Technology

The advent of LSI has led to the development of gate arrays, logic arrays, and other types of semicustom logic and digital/analog hardware in single-chip form. The driving force is economic; the cost per function is reduced as the number of functions per chip is increased. Another major benefit of the semicustom approach is that design cycle time is greatly reduced. An important advantage of semicustom over custom is that the user realizes a cost reduction through the efficiency of scale achieved by the manufacturer. One or a small number of basic chip designs are produced in volume by the suppliers to meet the needs of many customers; yet each customer has the benefit of maintaining uniqueness through the use of custom interconnections.

The IC industry has offered gate arrays since the mid-1960s with little economic success until recently. Ferranti's uncommitted logic arrays (ULAs), Texas Instruments' Master Slice approach, and Fairchild's Micromatrix were among the earliest arrays available. In the late 1960s TI offered a Discretionary Routed Array (DRA), which involved wafer probing to identify inoperative cells prior to final metallization. Raytheon marketed TTL arrays of 30 to 300 gates complexity at about the same time. All of the significant commercial programs were curtailed by the time of the mid-1970s recession for economic reasons.

The recent resurgence in gate array activity is a result of changes in circuit density, system constraints, and other market forces such as IBM's usage of gate arrays in its 4300 series computers. Lower cost CAD design tools are also contributing to the growth of gate array applications. At least 40 semiconductor suppliers have announced gate array products, and their 1981 sales are estimated at approximately $112 million.

The value of gate arrays is perceived as the following:

- System design security is maintained
- Lower system cost results from system package size reduction

- Lead times are reduced (compared to those of full custom chips)
- Logistics are simplified

Table 12-2 illustrates the relative design costs and complexities of the various logic implementation techniques in use today.

Table 12-2

COMPARISON OF DESIGN APPROACHES

Approach	Relative Design Cost	Typical Gate Count
Full Custom	100%	3,000 - 7,500
Standard-Cell Custom	60%	1,500 - 5,000
Gate Arrays	10%	500 - 2,500
Field Programmable Logic	1%	30 - 90
SSI/MSI	0%	12 - 15

Source: DATAQUEST, Inc.
April 1982

Gate arrays require higher pin counts than other forms of semiconductor logic, and packages with as many as 200-300 pins are being developed to meet this need.

Memory Devices

Memory ICs fall into two major groups: read-only memories (ROMs), and random access memories (RAMs). ROMs are non-volatile memories that can only be read and are used to store permanent information or instructions that will be required regularly. Information stored in RAM can be changed easily. RAM is typically used for temporary storage of data used to execute a computer program. The various types of ROMs and RAMs are discussed below.

Read-Only Memories (ROMs)

Read-only memories (ROMs) are programmed during the manufacturing process. This is usually achieved by customizing the design of one or more layers of the ROM IC. Before metallization, the IC is a standard product. These customized devices, called masked ROMs, are generally chosen when a company requires a relatively large quantity of identical devices.

Programmable Read-Only Memories (PROMs)

Programmable read only memories (PROMs) give the user added flexibility over factory-programmed ROMs. PROMs may be one-time programmable, as in the case of fuse-link devices, or may be reprogrammable after being erased electrically (EEPROMs) or with ultraviolet light (UV EPROMs).

A major advantage of these devices to both customer and manufacturer is that the customer can maintain a supply of unprogrammed PROMs, held by the distributor or at the user factory, and program them as necessary. It is also possible to program the devices at service depots and other field locations. This approach minimizes the need for an inventory of specialized parts, and facilitates engineering and production changes.

PROM implementations with bipolar technology offer higher speed over MOS types, but MOS PROMs offer lower power consumption and lower cost per bit.

Read/Write Random Access Memories (RAMs)

The memories discussed so far have the disadvantage that their stored information is fixed, which is not the case for read/write random access memories (RAMs). RAMs are memories in which each bit of stored information can be accessed with equal ease independently of the other bits, and information can be written into or read out of any bit location at any time while power is applied. Semiconductor RAMs, except NVRAMs, are volatile, meaning that loss of standby power causes loss of the stored information.

Because of their read/write and random access capabilities, semiconductor RAMs find widespread application in computer memories, where large amounts of data are stored and frequently changed. Bipolar RAMs are limited at present to computer applications where speed is primary and the higher power dissipation and cost associated with these devices can be tolerated. Applications include high-speed mainframe memories, cache, scratchpad, and small virtual memories. MOS RAMs are applied to most large, mainframe computer memories, where the need for high speed is overshadowed by memory costs. MOS RAMs account for most semiconductor RAM consumption.

Most bipolar RAMs operate in a static mode, whereas MOS RAMs are available in both static and dynamic versions. A static RAM indefinitely retains the latest information written into it, provided the basic or standby power is supplied to the circuit. Furthermore, data stored at any bit location is changed only when different information is written into it. When a storage location is accessed to read the stored bit, the data stored at that location is not destroyed—i.e., the bipolar memory has "non-destructive read out." High-speed bipolar RAM cells consume more silicon area than MOS dynamic RAM cells. In 1982 high-volume production state-of-the-art is 4,096 (4K) bits per device for bipolar static RAMs and (64K) bits for NMOS dynamic RAMs.

Microprocessors

The monolithic semiconductor microprocessor was first introduced commercially by Intel in 1971. It is usually defined as a programmable logic element capable of performing arithmetic, logic, and control operations. The first microprocessors were MOS devices that operated on four bits of data at a time; these evolved to 32-bit devices by 1982. More than 95 percent of all microprocessors produced are MOS, predominantly NMOS. However, CMOS is becoming an important technology for microprocessors, especially single-chip microcomputers.

Operation of a microprocessor unit (MPU) requires either internal or external clocking and, except for special purpose microcomputers, requires external memory and peripheral support circuits. Single-chip microcomputers usually have on-chip ROM or PROM for dedicated program storage.

Microprocessor Peripherals

Current microprocessor chips usually require additional hardware to complete a system function. This subsection briefly describes several examples of peripheral or support chips that are currently available to aid VLSI implementation.

Dynamic RAM Controller - Because dynamic RAMs require periodic refreshing to maintain data integrity, a method of accomplishing refresh control is needed. Single-chip dynamic RAM controllers accomplish the generation and sequencing of multiplexed address signals, strobes, enable signals, transfer indicators, and acknowledge signals.

Arithmetic Processor - For increased computing power, the semiconductor industry has developed high-performance support chips capable of floating-point arithmetic, double-precision arithmetic, and other special purpose algorithms. Such arithmetic processor units (APUs) or floating-point processor units (FPUs) are implemented with MOS technology for optimum cost/performance ratio, and with bipolar structures for maximum performance.

CRT and Disk Controllers - These are single-chip solutions to the problems of controlling cathode-ray tubes (CRTs) and other peripheral devices such as floppy disk drives. Both bipolar and MOS technologies have been used to implement CRT and disk controller functions.

Data Encryption - For security in the communication of data into and out of microprocessor systems, data encryption/decryption chips have been developed. Such chips are applied in situations involving the transfer of sensitive business and government data such as electronic funds transfer operations.

Analog Integrated Circuits

While digital integrated circuits operate with signals that are either on or off, analog integrated circuits function with continuously changing signals.

Amplifiers

An amplifier, as its name suggests, increases the strength of a signal without appreciably altering its characteristic waveform. It functions by transferring power to the signal from an external source. A familar example of the uses of amplifiers is the audio amplifier used to drive a speaker in a radio. Another example is the solid-state relay that takes a small signal and amplifies it into a current capable of performing work.

Voltage Regulators

The basic function of an integrated circuit voltage regulator is to provide a stable, fixed-level supply voltage under varying conditions of input voltage and load impedance. Key specifications include input regulation, ripple rejection, load regulation, and output voltage temperature coefficient. Because of the high current requirements of series IC regulators, the package is designed for excellent heat transfer characteristics. One application example is the 5-volt regulated power supply in a personal computer.

Analog-to-Digital (A/D) and Digital-to-Analog (D/A) Converters

Although they combine features of both digital and analog devices, A/D and D/A converters are usually considered with analog devices. A digital voltmeter uses an A/D converter to convert the voltage readings into digital output for the display. An example of the use of D/A converters is in automotive engine control where a digital signal from the microprocessor is converted to an analog signal for controlling the engine.

Voltage-to-Frequency (V/F) and Frequency-to-Voltage (F/V) Converters

Voltage-to-frequency converters convert analog voltage or current levels to logic-compatible forms at frequencies that are accurately proportional to the analog quantity. The output continuously tracks the input signal and responds directly to the input signal. V/F converters are used in analog-to-digital converters with high-resolution, long-term, high-precision integrators; two-wire, high-noise-immunity; digital transmission; and digital voltmeters.

Frequency-to-voltage converters accept a wide variety of periodic waveforms and produce an analog output proportional to frequency. F/V converters are used in a wide variety of applications where conversion of frequency to an analog voltage is required. Examples of their use include motor-speed controllers, power-line frequency monitors, and voltage-controlled oscillator stabilization circuits.

Custom Digital and Analog Functions

Many manufacturers, as discussed in Volume II, offer custom-integrated circuit fabrication using supplier-designed tooling or customer-owned tooling (COT). Both bipolar and MOS processes are available, covering a very wide range of applications and needs. Contracts for custom services are negotiated on an individual basis according to the economic constraints of the supplier and the customer.

Emerging Technologies

Although DATAQUEST expects silicon bipolar and MOS devices to dominate the semiconductor industry for some time to come, there are a number of emerging technologies that deserve consideration in this section.

Charge-Coupled Devices

Charge-coupled devices (CCDs) were first introduced in 1970 by Willard Boyle of Bell Laboratories. He and his co-workers proposed that such devices could readily be used for imaging and other applications. Three years later, circuits became commercially available for the first time.

There are four areas of applications for CCD devices:

- Imaging
- Memory
- Delay lines
- Filters

In imaging applications, incident light is focused either on the front or back of the CCD device. This incident light creates electrical charge wells within the silicon close to the electrodes. Different wells will have different amounts of charge according to the amount of light focused on them. On electrical command, the wells of charge can be shifted serially out of the CCD sensors. For example, the information can be redisplayed on a video screen. The advantage of CCD imaging equipment devices over conventional TV cameras is that the bulk of image processing can be performed on a single silicon chip. This approach eliminates the need for an electron scanning beam, high voltages, and the associated circuitry required by conventional TV cameras. Moreover, the CCD chip is small, operates at high speed, has low power dissipation, and offers solid-state reliability. One drawback to the use of CCDs as video sensors is their poor response to blue light, a characteristic of any silicon sensor. On the other hand, CCDs have exceptionally good sensitivity at very low light levels and can be fabricated to be sensitive to infrared light. These advantages make the CCDs applicable for many special uses such as military applications and security devices.

Industrial quality CCD video cameras are now available. A number of companies are producing arrays of 484 x 380 pixels. The success of these and future advancements in CCD technology will determine the impact of this technology on the video market. Simpler CCD devices have also found use in other optical-sensing applications, such as optical readers. Such usage should become more prevalent in the near future.

Since there are no diffusions for contacts between or to any of the charge storage areas, the density of information storage can be very high for CCD memories. The serial nature of the charge storage and shifting in CCD devices also makes them adaptable to many serial memory applications, such as picture storage and recycling on CRTs and video screens. However, the relatively high production costs of CCD compared to dynamic RAM and bubble memory technologies have limited the widespread application of CCD in memory systems.

One particular application that cannot readily be performed by other semiconductor devices is the use of CCDs as signal delay lines. The delay can be varied according to the clock rate applied to the electrodes of the devices and the number of bits used. An important attribute of these devices is that the delay can be used to accommodate either analog or digital signals. One potential application, for example, would be to correct delay errors in video recording and video playback from disk.

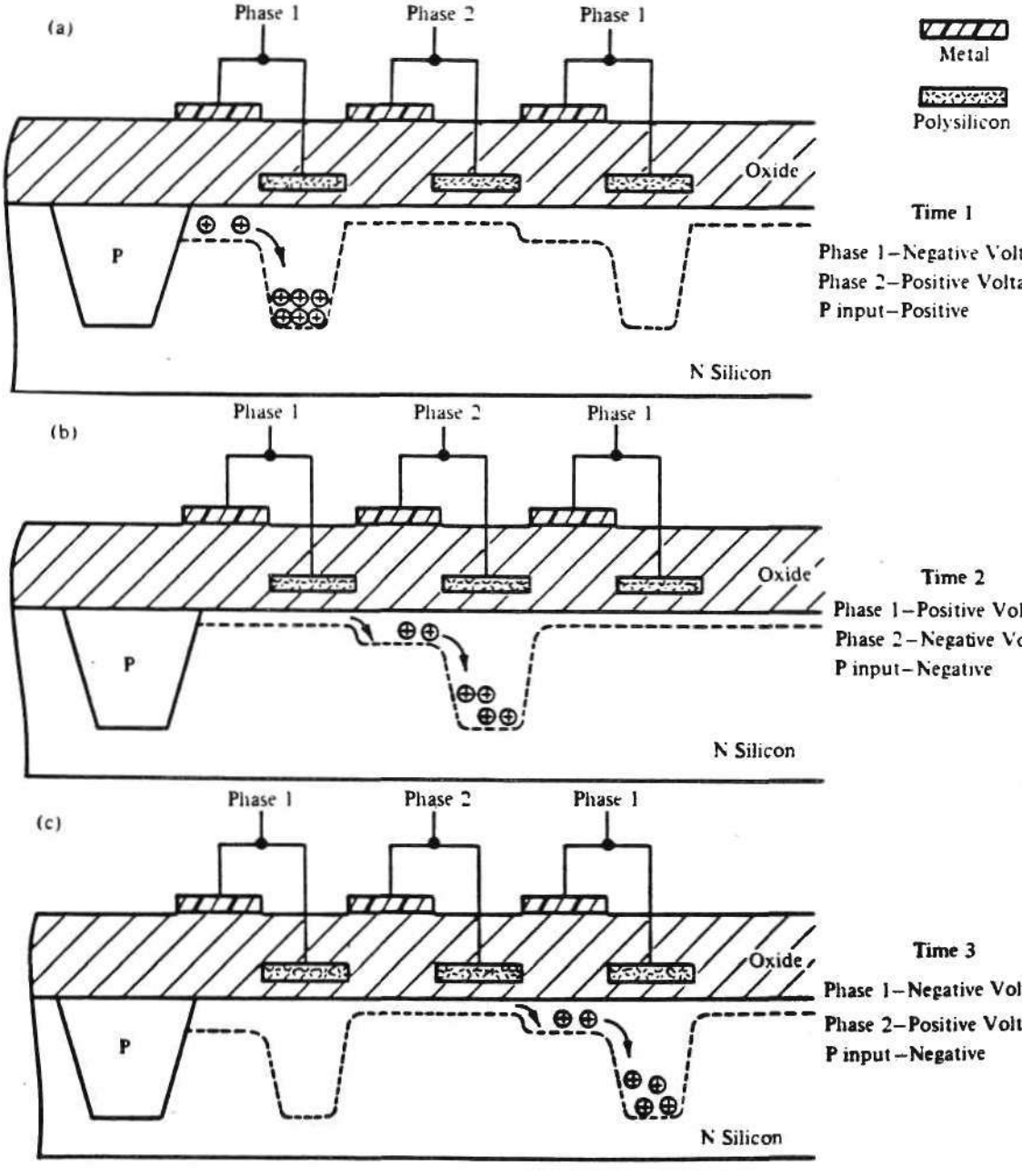
The delay line characteristics of CCDs can also be adapted to make the device function as a filter for electronic signals. This characteristic has several applications. CCDs can perform narrow-bandwidth high-Q filtering centered around a particular frequency, which is determined by the clock rate of the device. These filters are especially competitive at very low frequencies. CCD filters can also be designed to filter non-sinusoidal signals.

Figure 12-12 illustrates the cross-section of a silicon-gate, two-phase, CCD. A CCD retains information by storing electronic charges in depletion "wells" created by the voltage on metal or polysilicon near the surface of the wafer. Information is moved by transferring the charge along, much like an old-time bucket brigade. If the metal or polysilicon has the proper voltage, the well will be created, and it will disappear when the voltage is removed. Although the well holds the charge, the charge must be introduced into it at the time it is formed. Charges can be introduced either by incident light, as in the case of imaging applications, or by an applied electrical signal.

In Figure 12-12a, a charge is introduced by a P-diffusion when it is at the proper voltage. If the P material is not at the proper voltage, charges will not be introduced and the well will remain empty. In Figure 12-12b the voltage phase is changed so that Phase 2 has a negative voltage and Phase 1 has a positive voltage. When this change occurs, the charge is transferred from the original well to a newly created adjacent one. In the next time period, as shown in Figure 12-12c, the voltage on the phase lines changes back to the original levels, and the charge back to the original levels, and the charge is again transferred. Since the P-diffusion no longer has a positive voltage, the first well (on the left) has no charge transferred to it.

Figure 12-12

CHARGE-COUPLED DEVICE OPERATION



Source: DATAQUEST, Inc.
April 1982

In this manner information is moved serially by alternately changing the magnitudes of the voltages applied to the phase electrodes. Because the amount of charge in a particular well can vary over an entire range and need not be binary, a CCD can function as an analog memory; that is, the information stored in a well can be proportional to an input signal. Depending on the type of operation, CCDs can operate with three-phase or four-phase clocking as well as variations of the two-phase circuit described here.

Magnetic Bubble Memories

Memory is the primary application for magnetic bubble devices (MBDs). With information stored in bubbles as small as 1 micron, bit densities in excess of 10^6 bits per square inch can be achieved. The primary advantages of MBDs are their non-volatility and their ruggedness in hostile environments. For these reasons they are finding application in industrial robotics and in military applications, especially where portability is a consideration.

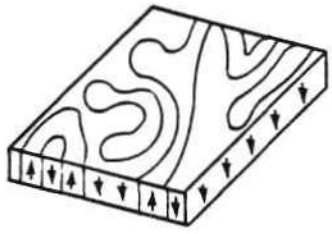
Magnetic bubble devices were discovered in 1967 by Bell Laboratories engineers who found that stable magnetic bubbles could be created, propagated, and detected for use in memory applications. In 1976, the first MBD memory chips became commercially available, and current devices offer 1 megabit of memory storage.

Magnetic bubble devices are built on gadolinium gallium garnet (GGG) substrates, which are non-magnetic. A thin garnet film containing iron is deposited on this substrate. In this single-crystalline thin garnet film, magnetic domains exhibit a preferred axis of magnetization perpendicular to the film surface. In the absence of any external magnetic field, the thin film will break up into magnetic domains in which the magnetization is uniformly "up" or "down." The serpentine magnetic domains arrange themselves in such a way that the garnet film is magnetically neutral, with half of the serpentine domains pointing up and the other half pointing down (Figure 12-13a). If a small magnetic field is applied perpendicular to the film, the magnetic domains whose polarity is opposite to that of the applied field shrink (Figure 12-13b). As the applied magnetic field is further increased, the serpentine magnetic domains shrink into cylinders (Figure 12-13c) whose diameter depends upon the film thickness, the applied field, and certain material parameters. When viewed under a polarized light source, these magnetic cylinders can be seen, and they appear as bubbles. If the applied magnetic field is further increased, the opposing magnetic domains collapse entirely (Figure 12-13d).

If the applied bias field is reduced to a level where magnetic bubbles are stable, magnetic bubble domains can then be generated by passing current pulses through a "hairpin" conductor loop. The resulting bubbles appear in the garnet film under the loop and can be moved around inside the film. Bubble propagation is accomplished by using an overlay permalloy pattern, which determines the bubble propagation path, and an in-plane rotating magnetic field, which moves the bubbles. The in-plane rotating field is generated by a set of orthogonal coils that surround the bubble chip.

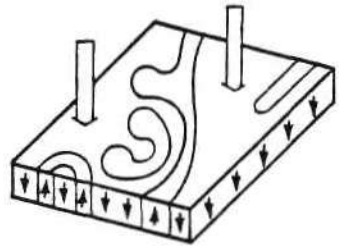
Figure 12-13

MAGNETIC DOMAINS IN A
THIN GARNET FILM



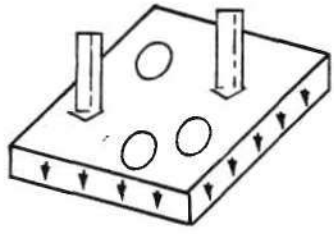
a

Serpentine magnetic domains under no external field. Half of the domains are pointed up and half are pointed down.



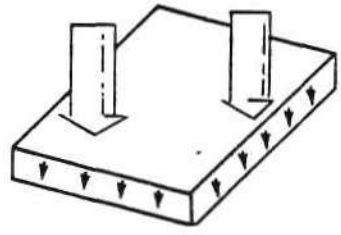
b

Serpentine magnetic domains under applied magnetic field. More than half of domains are oriented with external field.



c

Opposing magnetic domains shrink to cylinders as applied magnetic field increases.



d

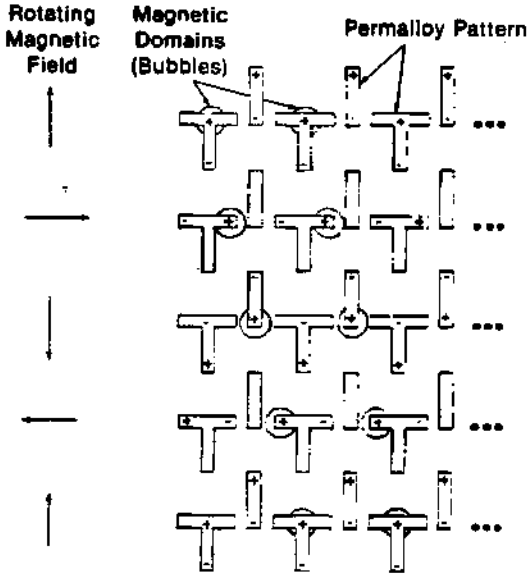
Opposing magnetic domains disappear as applied magnetic field is further increased.

Source: DATAQUEST, Inc.
April 1982

Figure 12-14 illustrates the details of magnetic bubble propagation. A common overlay pattern known as a "TI-bar pattern" is processed on the thin garnet film. It consists of magnetically soft permalloy material that polarizes along the in-plane field. Any bubbles under the permalloy overlay move to positions under the appropriate poles. Rotating the in-plane field causes the positioning magnetic poles to move across the TI-bar array, which carries the underlying bubbles along. (See the bubble movements in the successive rows of Figure 12-14.) Other overlay patterns that have been successfully demonstrated include the Y-bar, chevron, and contiguous disk. The overlay pattern requires no conductors in the central area of the bubble chip. The only conductors required are for generation, detection, replication, and transfer of bubbles, and these are positioned along the edges of the bubble chip.

Figure 12-14

TI-BAR PROPAGATION TECHNIQUE

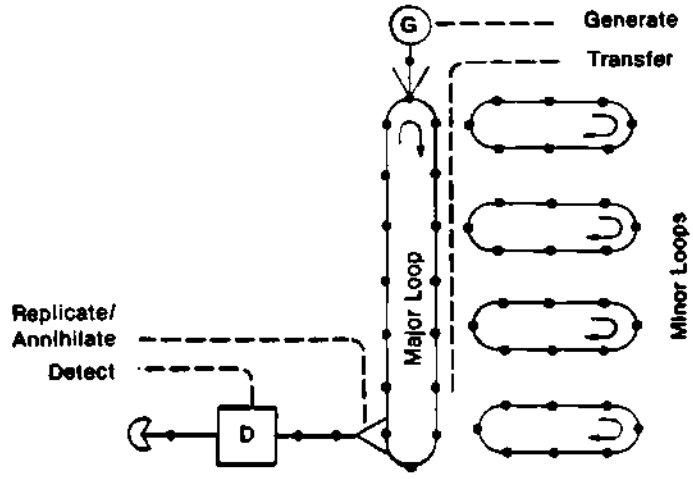


Source: DATAQUEST, Inc.
April 1982

The preferred architecture for MBD chips is the major/minor loop shown in Figure 12-15. This architecture consists of one major loop and multiple minor loops. An incoming stream of "1"s and "0"s is converted by the bubble generator into a serial stream of bubbles and no bubbles. As bubbles are generated in the major loop, they are shifted around the loop until a block of data lines up with the minor loops. Under external control, the transfer gate enables the transfer of bubbles between the major and minor loops. This process can continue until all the bubble positions in the minor loops are filled. To read the bubble memory contents, an entire block (one bit from each minor loop) is transferred to the major loop. Actually, a copy of each bit is transferred to the major loop and the original bit is left behind in the minor loop to preserve the memory contents. The bubbles in the major loop are then propagated around the loop and detected.

Figure 12-15

MAJOR-MINOR LOOP ARCHITECTURE
FOR MAGNETIC BUBBLES



Source: DATAQUEST, Inc.
April 1982

The advantage of the major/minor loop architecture is that every bit location in the minor loops does not have to be perfect. Some level of defect can be tolerated. By accepting all chips that have no more than 8 percent of the minor loops defective, a higher yield and lower cost can be achieved. The defective loops are noted during testing and are omitted from the address list of good minor loops.

Since magnetic bubbles are not TTL-compatible, special interface circuits must be used. The interface circuits actually serve two purposes. First, they provide a TTL 8-bit parallel interface that is ideal for minicomputer and microcomputer applications. Second, they format the parallel data into a serial stream for input to the MBD package, and they provide the precise timing and control necessary to operate the magnetic bubble memory.

Josephson Junctions

Josephson junctions can perform a similar function to transistors in a computer. Their advantage is that they work two to three orders of magnitude faster than current semiconductor logic devices. Their major disadvantage is that they have to be maintained at temperatures close to absolute zero.

Josephson junctions rely on the fact that certain metals lose all resistance to electrical current and become superconductors at temperatures of a few degrees above absolute zero. A Josephson junction is formed by separating two layers of superconducting metal using a very thin layer of insulating oxide (about 50 Angstroms thick). Because these devices can be very densely packed, and because the junctions have switching times of less than 50 picoseconds, a computer made with this technology can operate many times faster than today's fastest semiconductor-based computer. The power consumption of a Josephson junction device is thousands of times less than an equivalent semiconductor function.

At the 1982 International Solid State Circuits Conference (ISSCC), IBM introduced a Josephson logic element, consisting of 102 logic gates, that operated with a cycle time faster than 700 picoseconds. This is a significant step towards a Josephson junction computer.

SUMMARY

This section has given the user general information on the manufacture and uses of individual semiconductor devices. To further assist the client, Section 2, Semiconductor Trends, discusses DATAQUEST's analyses of potential developments in these areas.

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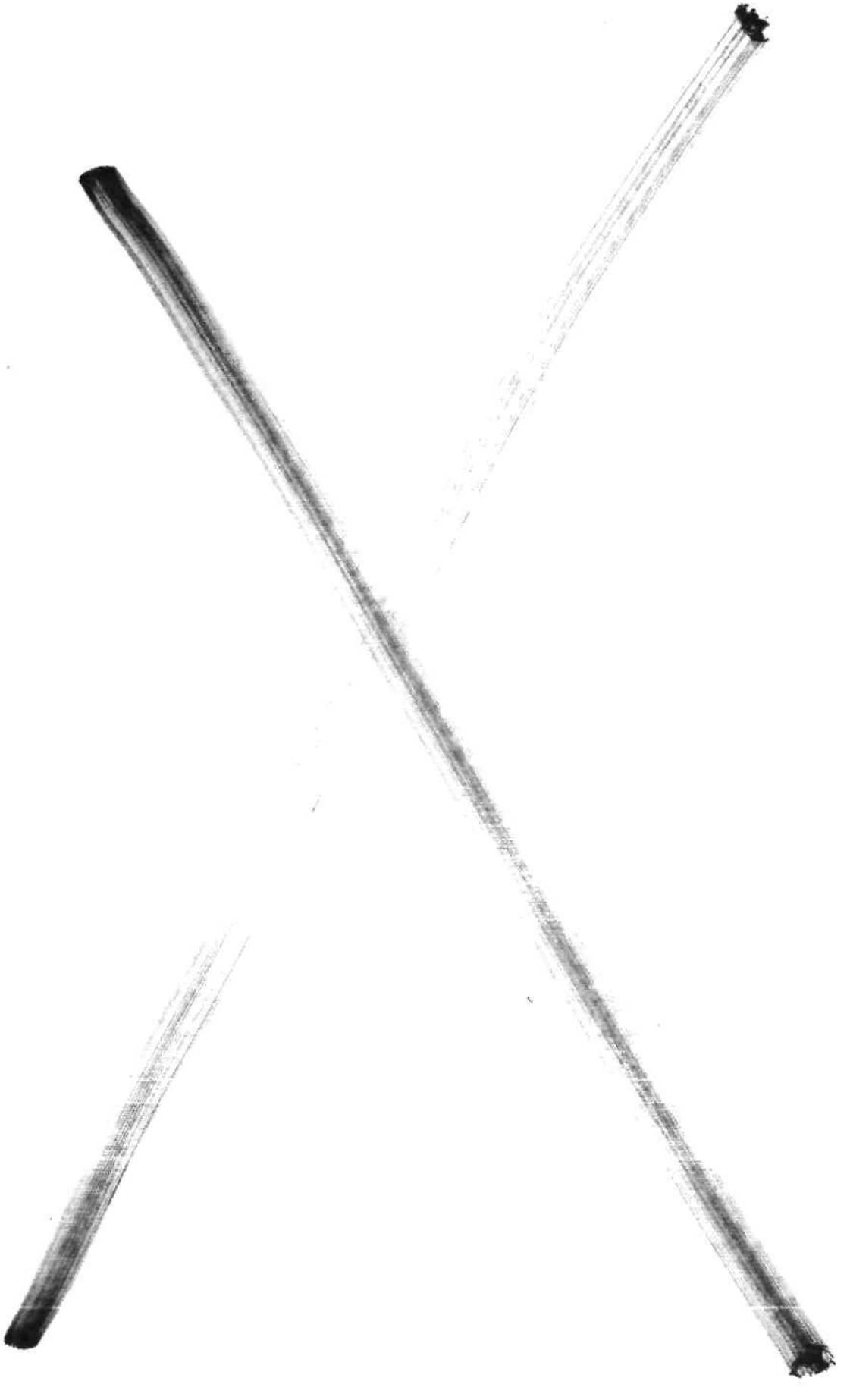


Appendix E—Economic Data and Outlook

THE UNITED STATES

Review and General Comments

After an explosive growth during the first half of 1983, the U.S. economy is expected to expand through 1983, 1984, and beyond. Though the pace will probably slow later this year, we believe that the rebound will continue. The advance during 1984 and 1985 will depend largely on when and to what extent the business community decides to step up its investment in new plants and equipment.

The plusses will keep mounting as the 1983 third quarter upturn progresses into a broader spectrum of the industrial sectors. Business inventories touched bottom at the end of the first quarter, but there is growing evidence of an inventory turnaround. For the second half of 1983, we believe that accelerated consumer spending and business restocking of inventories will continue the upward thrust of the first half.

The recovery is now getting sustenance from the classical source--consumer spending. Real consumer income is rising and savings rates are moving down. This trend is providing the thrust that will ensure that gains in business activity can continue to advance this fall. In our opinion, the economic advance has reached a self-energizing stage.

The tax cut at midyear not only boosted consumer take-home pay, it prompted pre-tax cut spending. Consumers usually begin to spend even before the extra income shows up in their paychecks. Another favorable factor in the consumer picture is the behavior of prices: Inflation is considerably below earlier estimates and inflationary expectations are decreasing.

The pickup in retail sales is directly related to the U.S consumers' growing optimism about the economy in the past few months. Unemployment has diminished as job opportunities have improved, and this trend is expected to continue. For the second quarter in a row, surveys indicate that a significant proportion of employers intend to increase their workforces. Hiring plans for the third quarter are up in many sections of the United States and are notably strong in construction, manufacturing, and service industries.

Productivity is clearly on the mend. For the first time in a decade it has increased five quarters in a row, and the first quarter's rise matched the biggest single gain in the past six years. Foreign and domestic competition forced many businesses to trim their budgets, purchase more efficient equipment, and seek other ways to cut costs.

DATAQUEST's forecast for the 1983-1985 U.S. economy is presented in Tables E-1.1 and E-1.2.

Appendix E—Economic Data and Outlook

Table E-1.1

ESTIMATED U.S. ECONOMIC INDICATORS
($ Billions, Seasonally Adjusted at Annual Rates)

	Quarterly							
	82:3	82:4	83:1	83:2*	83:3*	83:4*	84:1*	84:2*
GNP	$ 3,088.2	3,108.2	3,171.1	3,262.3	3,365.5	3,416.9	3,492.9	3,573.1
Real GNP ($1972)	$ 1,481.1	1,477.7	1,486.7	1,520.9	1,546.8	1,563.8	1,579.8	1,594.4
Percent Change	0.7	-1.6	2.4	9.2	6.8	4.4	4.1	3.7
GNP Deflator (1972=100)	208.5	210.4	213.3	214.5	215.7	218.5	221.1	224.1
Percent Change	4.9	3.7	5.6	2.2	2.2	5.1	4.8	5.5
Real Final Sales	$ 1,477.7	1,497.5	1,502.3	1,513.8	1,537.6	1,550.4	1,561.1	1,579.5
Percent Change	-1.4	5.4	1.3	3.1	6.3	3.3	2.8	4.7
Savings Rate (Percent)	6.9	5.9	5.9	5.9	6.1	5.9	5.9	6.1
Real Disposable Income	$ 1,058.3	1,059.1	1,064.6	1,075.1	1,087.7	1,101.6	1,110.1	1,119.1
Percent Change	1.3	0.3	2.1	3.9	4.7	5.1	3.1	3.3
Real Consumption Spending	$ 956.3	967.1	973.1	983.7	994.2	1,004.3	1,013.1	1,024.3
Percent Change	0.5	4.5	2.5	4.4	4.3	4.1	3.5	4.4
Unemployment Rate (Percent)	10.0	10.7	10.4	10.1	9.4	9.2	9.1	9.0
Wholesale Prices (1967=100)	300.0	300.3	300.5	301.4	303.9	307.6	311.4	315.4
Percent Change	1.7	0.4	0.3	1.2	3.3	4.9	4.9	5.2
Consumer Prices (1967=100)	292.8	293.4	293.2	296.9	300.1	305.3	309.3	313.3
Percent Change	7.7	0.8	-0.3	5.1	4.3	6.9	5.3	5.2
Industrial Production (1967=100)	138.2	135.3	138.5	144.1	149.3	152.2	154.1	156.1
Percent Change	-3.2	-8.3	9.6	16.5	14.7	7.8	5.1	5.2
Bus. Fixed Investment ($1972)	$ 163.4	160.9	162.9	163.3	163.6	164.7	167.9	171.5
Percent Change	-7.8	-6.1	4.9	0.9	0.7	2.7	7.8	8.7
Private Housing Starts (Millions)	1.12	1.26	1.69	1.68	1.61	1.47	1.45	1.55
Money Supply (M1)	$ 459	474	490	503	520	529	539	549
Percent Change	6.2	13.3	13.7	10.8	13.7	6.9	7.7	7.5
3-Month Treasury Bills (Rate: Percent)	9.7	7.9	8.1	8.3	8.5	8.8	8.8	8.6
U.S. Population (Millions)	232.3	232.9	233.5	234.1	234.7	235.3	235.9	236.6
Percent Change	1.0	1.0	1.1	1.0	1.1	1.0	1.1	1.0
Per Capita Real GNP	$ 6,375	6,342	6,367	6,497	6,591	6,646	6,697	6,739
Percent Change	-0.3	-2.1	1.6	8.2	5.8	3.3	3.0	2.5

*DATAQUEST estimate

Source: U.S. Department of Labor
U.S. Department of Commerce
Federal Reserve Board
DATAQUEST

Appendix E—Economic Data and Outlook

Table E-1.2

ESTIMATED U.S. ECONOMIC INDICATORS
($ Billions, Seasonally Adjusted at Annual Rates)

		Yearly								
		1977	1978	1979	1980	1981	1982	1983*	1984*	1985*
GNP	$	1,918	2,164	2,418	2,663	2,937	3,059	3,296	3,615	3,974
Real GNP ($1972)	$	1,370	1,439	1,479	1,474	1,502	1,476	1,530	1,599	1,661
Percent Change		5.6	5.1	2.8	-0.3	1.9	-1.7	3.7	4.5	3.9
GNP Deflator (1972=100)		140.0	150.4	163.5	178.6	195.6	207.1	215.4	226.1	239.2
Percent Change		5.7	7.4	8.7	9.2	9.5	5.9	4.0	5.0	5.8
Real Final Sales	$	1,357	1,423	1,472	1,479	1,493	1,486	1,526	1,584	1,649
Percent Change		5.1	4.9	3.4	0.5	0.9	-0.5	2.7	3.8	4.1
Savings Rate (Percent)		5.9	6.1	5.9	5.8	6.4	6.5	6.0	6.1	6.5
Real Disposable Income	$	943	969	1,016	1,018	1,043	1,054	1,082	1,122	1,168
Percent Change		4.0	2.8	4.9	0.2	2.5	1.1	2.7	3.7	4.1
Real Consumption Spending	$	864	905	928	931	947	956	988	1,027	1,067
Percent Change		4.9	4.8	2.5	0.3	1.7	0.9	3.4	3.9	3.9
Unemployment Rate (Percent)		7.0	6.0	5.8	7.1	7.6	9.8	9.8	9.2	7.8
Wholesale Prices (1967=100)		194.2	209.3	235.5	268.8	293.1	299.3	303.4	317.5	336.9
Percent Change		6.2	7.8	12.5	14.1	9.1	2.1	1.3	4.6	6.1
Consumer Prices (1967=100)		181.5	195.4	217.4	246.8	272.3	289.1	298.9	315.4	334.4
Percent Change		6.5	7.7	11.3	13.5	10.3	6.2	3.4	5.5	6.0
Industrial Production (1967=100)		138.1	146.1	152.5	147.0	150.9	138.7	146.1	154.6	160.9
Percent Change		5.9	5.8	4.4	-3.6	2.7	-8.1	5.3	5.9	4.1
Bus. Fixed Investment ($1972)	$	140.3	158.3	169.9	161.1	171.9	165.8	163.6	172.8	184.9
Percent Change		11.7	12.8	7.3	-5.2	6.8	-3.6	-1.3	5.6	7.1
Private Housing Starts (Millions)		1.99	2.02	1.74	1.30	1.10	1.06	1.61	1.57	1.65
Money Supply (M1)	$	325	351	372	398	430	458	510	554	596
Percent Change		7.6	8.1	5.9	6.9	8.1	6.5	11.4	8.6	7.6
3-Month Treasury Bills (Rate: Percent)		5.3	7.2	10.0	11.6	14.1	10.7	8.4	8.6	8.8
U.S. Population (Millions)		220.0	222.6	225.1	227.7	229.9	232.0	234.4	236.8	239.3
Percent Change		1.0	1.2	1.1	1.2	0.9	1.0	1.0	1.1	1.0
Per Capita Real GNP	$	6,222	6,465	6,572	6,534	6,564	6,364	6,527	6,753	6,941
Percent Change		4.5	3.9	1.7	-1.5	0.9	-2.6	2.6	3.5	2.8

*DATAQUEST estimate

Source: U.S. Department of Labor
U.S. Department of Commerce
Federal Reserve Board
DATAQUEST

Appendix E—Economic Data and Outlook

The Forecast

The forecast for 1984 and 1985 GNP is essentially the same as in our last outlook. Despite the threats posed by the deficits, interest rates, inflation, foreign debt burdens, and protectionism, there is a good chance that this upswing could be one of the longest in recent U.S. history. In a recent survey, more than two-thirds of the company officers said they were confident about the outlook for 1984. Nevertheless, the majority of executives still say they are proceeding with caution in respect to their own business policies. These apparently contradictory impressions may reflect the executives' feelings that although competition will continue to be tough, their increased confidence will promote inventory purchasing and capital spending.

DATAQUEST's forecast for 1983 has been increased slightly to a 3.3 percent growth in real GNP. The quarterly patterns for 1983 have been modified due to the faster than expected rebound during the first half. Nearly every forecaster overlooked one simple fact: Even though unemployment was high, total employment had remained near the 100 million level since 1980 (we noted this in our last report, but underestimated its short-term importance). When inflation dropped faster than expected, real incomes rose and consumers increased their purchases--thus propelling the rapid upturn of the first half.

The one cloud that casts a shadow on the economic horizon is the Federal budget, or, more specifically, the effect that the large Federal deficits will have on the interest rates during 1984 and 1985. The Reagan Administration apparently believes that this will not be a serious problem because the expanding economy will provide higher revenues and lower welfare payments, thus reducing the previously estimated deficits. Many independent economists say these deficits will keep interest rates near their current levels.

The key area to watch during the next few months is the level of long-term interest rates. This will set the tone of the U.S. and world economies during 1984, due to the effects of interest rates on the price of the dollar and in turn on the volume of world trade.

Monetary Policy and Interest Rates

Money market analysts believe that the Federal Reserve Board is more likely to push rates up than down. Chances are good that the Federal Reserve Board can execute a neat bit of fine-tuning by tightening the money just enough to reassure the capital markets that it has not forgotten about inflation, but not tightening so much as to make credit really scarce. Currently there is sufficient money around and business demand for it is not yet all that robust.

Appendix E—Economic Data and Outlook

Money managers and economists do not expect a rise in interest rates. Due to the already achieved slowdown in inflation, the high real rate of interest (nominal rates minus the inflation rate), and the problems of funding enormous international debts, significant tightening by the Federal Reserve Board is effectively ruled out.

A dramatic tightening is not likely unless the Federal Reserve Board is convinced that its modest-recovery scenario is imperiled. As the Board views it, the strong second quarter is no cause for alarm because it was largely the result of a massive one-time inventory liquidation by business. Federal Reserve Board officials say that the second quarter growth should be averaged with the weaker first quarter, resulting in a first half rate in line with the Federal Reserve Board's strategy of a modest recovery. It will take another six months of solid numbers to determine if inflation will remain quiescent as the economy expands.

Business Fixed Investment

The capital spending picture is looking brighter than most economists thought possible. The uptick that occurred in the first half of 1983 remains something of a mystery, since the fundamentals that govern investment activity remain relatively weak. Capacity utilization is still well below the level needed to trigger sustainable growth in investment. However, current operating rates are slightly above 70 percent for all of manufacturing.

The second quarter U.S. Commerce Department survey indicates that business intends to step up its plant and equipment spending in the fourth quarter. Other indicators suggest that increased spending may occur during the third quarter. Executives may no longer choose to postpone these decisions in hopes of still lower interest rates. Until the recovery broadens to include more of the basic industries, do not look for a dramatic increase in spending. In some industries, such as steel and oil, cutbacks in investments are still taking place.

U.S. Trade Balance

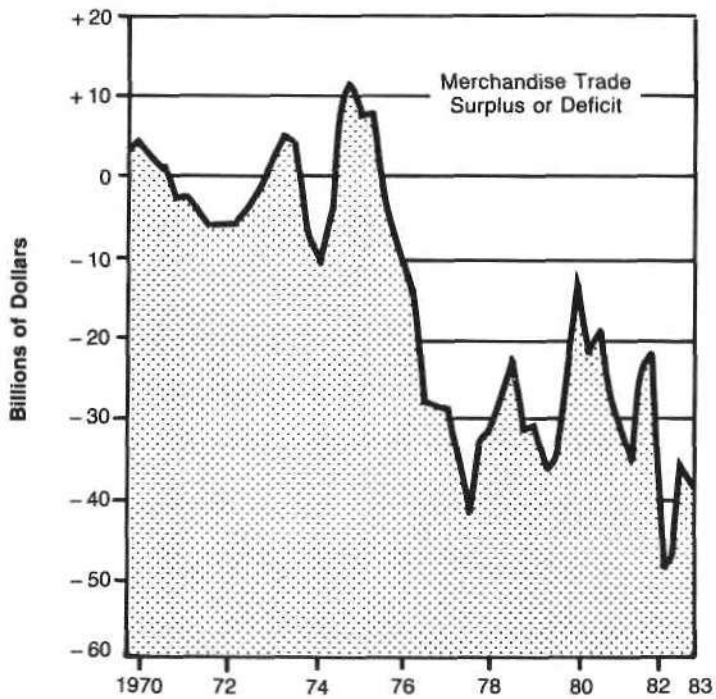
The chief depressant of the trade balance is the high value of the dollar relative to other currencies (a brief overview of the high-priced dollar follows in the next section). This discourages U.S. exports by making them more expensive in foreign markets. The U.S. Department of Commerce estimates that the trade deficit will swell to approximately $60 billion by the end of the year. (See Figure E-1.)

This will continue to be a drag on the U.S. economy for the forseeable future. During the recession, the trade deficit equalled nearly 75 percent of the decline in real GNP. The current deficit also is causing a loss in GNP, but more dramatic is the loss of an estimated one million jobs.

Appendix E—Economic Data and Outlook

Figure E-1

WEAKENING U.S. TRADE



Source: U.S. Commerce Department

The Strong Dollar

Forecasters still expect the dollar to drop--as they were saying a year ago--but they concede that the fall will not be as steep as they expected earlier. A few analysts look for the value of the currency to rise slightly. The dollar will probably continue to strengthen against other currencies for a short time until late-summer or fall.

Since 1980, on a trade-weighted basis, the dollar has climbed dramatically against the world's key trading currencies, especially the Deutsche mark and the yen. It is clearly overvalued. Chances for an easing in the dollar's strength will be helped by events abroad as other industrialized countries show signs of economic recovery.

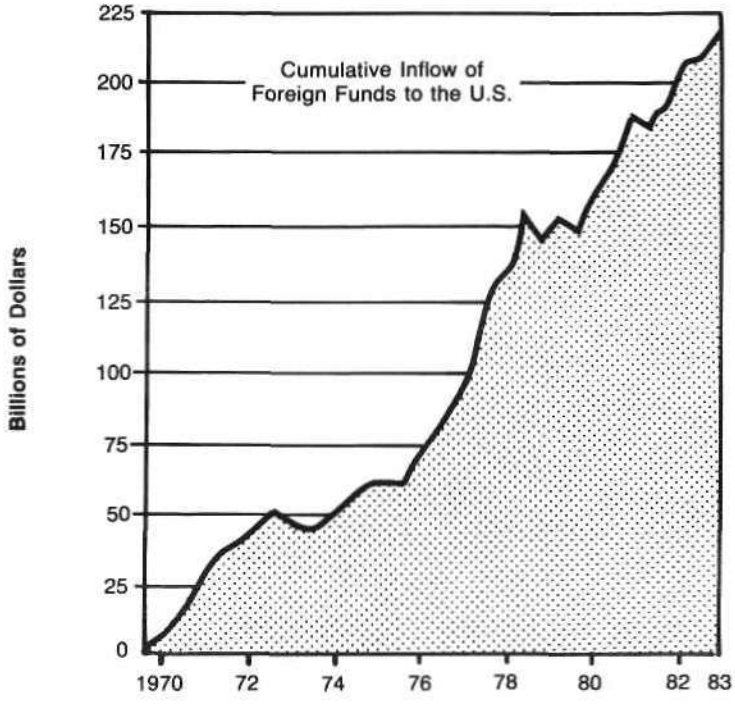
Appendix E—Economic Data and Outlook

The main reason for the strength of the dollar is the level of U.S. real interest rates (market rates minus inflation). Real interest rates have remained high in the United States at above 5 percent. In comparison, Japanese and German real interest rates stand at 2 percent and 3.5 percent, respectively.

Since 1980, nearly $70 billion net of foreign capital has poured into the U.S. equity market. The unrest in several countries, in addition to the possibility of an international liquidity crisis, has further enhanced the dollar's position as the world's premiere currency. (See Figure E-2.)

Figure E-2

FOREIGN MONEY INFLOWS



Source: Federal Reserve Board

Appendix E—Economic Data and Outlook

INTERNATIONAL

There have been four key areas of concern in the world economies during the past few years:

- Inflation
- Unemployment
- Debt burden of developing nations
- Growing protectionism

Inflation is no longer the major area of concern. In most of the industrialized nations it has decreased dramatically from the levels of just one year ago. This is due in large part to the worldwide recession, but it is also due to the more conservative fiscal policies adopted by most governments. We believe that the inflation rates will increase from their current levels as the respective economies expand--but at slower rates than we expected a few months ago.

Unemployment is still a "minus" in the long-term outlook. Current levels are too high and are unlikely to decrease proportionately to the advances of the major economies.

The current debt burden of the developing nations has reached an estimated $700 billion and the lending agencies (both government and private) are demanding that these developing nations put in place austere governmental programs before their loans are extended or refinanced. This means these nations will have to decrease their imports, which implies fewer exports from the industrialized nations. The OPEC nations will also be forced to import less, due to the lower oil prices.

DATAQUEST believes that the forces that drive the export markets will not improve significantly until mid-1984. Thus, we have moderated our growth estimates for all International economies for 1983 and 1984. The United States and Japan will lead the recovery, supported by the United Kingdom and West Germany.

DATAQUEST's forecast for France, Japan, the United Kingdom, and West Germany are presented in Tables E-2 through E-5, respectively. Table E-6 shows the month-end selling prices for bank transfers.

Appendix E—Economic Data and Outlook

France

In France, expectations of consumers and producers were dimmed by the shift to more restrictive economic policies forced on the government by the weakness of the franc. The austerity programs have increased taxes and slashed governmental expenditures. A wage-price spiral is still increasing along with foreign debt. Capital investment is heading down and industrial production is slack.

France is paying the price for the 1.2 percent GDP growth in 1982, the highest of any major European country. The 1981 attempt at expansion that increased inflation and foreign debt is the primary reason for the high growth. We expect France to have an estimated 1 percent decline in real GDP this year, and possibly a 1 to 2 percent growth in 1984.

Japan

Early signs of an upturn are appearing in Japan, but preliminary first quarter data suggest that they lack force. Even so, the Japanese economy may expand by about 3 percent in 1983, missing Tokyo's target of 3.4 percent. Despite stable commodity prices, the pace of consumer spending is slow. Non-manufacturing industries are beginning to step up investments but expenditures on the manufacturing side are still declining and are expected to continue to decline for most of 1983.

A recent report by the Japan Economic Research Center predicted that the economy will achieve recovery (faster upturn) in the latter half of fiscal 1983 on the strength of growing exports and progress in inventory adjustments. Although exports to oil producing and debt-ridden developing nations will decline, those to Europe and North America will increase because stocks of unsold products in these markets are nearly depleted.

United Kingdom

The forecast for the United Kingdom is essentially the same as in our last report. Current estimates of real GDP growth in 1982 are higher than earlier data. The United Kingdom is expected to grow approximately 2 percent in 1983, the highest growth of any major European country. The growth in 1984 should improve to about 2.5 percent.

Consumer price increases are currently down to levels not seen in a decade. This has increased purchasing power and consumer confidence for those still working. Unemployment has nearly doubled in the last four

years to three million persons. Industrial production was up a surprising 5 percent during the first quarter and is expected to continue its upward trend.

West Germany

The view from West Germany is that the United States will have to "pull" the European economies along. There are signs of recovery but it is uncertain if the recovery will gather much momentum this fall. Thus, the official government position is for little or no growth this year. Independent sources are projecting a 2 percent growth in 1983, even though they expect Bonn to continue its cautious course aimed at reducing budget deficits and inflation.

German experts say several elements favor better business: falling oil prices, reduced inflation, and the easing debt crisis. However, the long-range outlook remains clouded by trade protectionism, export trade, pinched profits, high loan costs, and big budget deficits.

As with most other economies, German consumer and wholesale prices are down significantly, which should lead to increased consumer buying power and an improved outlook for 1983. DATAQUEST is estimating a 1.2 percent real GNP growth this year and a stronger 2.7 percent increase in 1984.

NOTE ON QUARTER GROWTH RATES

In preparing the numbers presented in this report, we employed two primary analytical techniques--judgmental and econometric. The judgmental aspect employs the knowledge we have gathered from various sources to further refine our estimates now and in the future. Therefore, important inputs are reports published by various sources, e.g., governmental agencies and economists from the business and academic communities. The econometric technique involves the use of statistical methods to make the reported quarterly time series consistent with the annual data.

We have adopted a standard methodology of reporting growth rates. For the data, most quarterly series are seasonally adjusted and reported at annual rates (multiplied by four). Yearly figures are merely the average of the four quarterly seasonally adjusted numbers.

For the percent changes, the year-to-year growth is the percentage difference between the respective averages of the relevant quarters. The

quarterly growth rate, however, is computed in comparison with the immediately perceding quarter. The quarter-to-quarter percentage differece is compounded to produce an annual rate. This computation is illustrated in the following example:

1983 U.S. ECONOMY

Real GNP		Difference	Percent Difference
Q1	Q2		
1,486.2	1,515.8	1,515.8 - 1,486.2 = +29.6	+29.6/1,486.2 = = +0.0199

Compound Annual Percentage Rate

$((1 + 0.0199)^4 - 1) \times 100 = 8.1\%$

THE PROBLEM WITH TIME SERIES REVISIONS

The basic source for the international historical data is the International Monetary Fund (IMF). The IMF revises selected series almost monthly as it receives additional reports from the respective governments.

Recently, the IMF changed the base year for all index series from 1975 = 100 to 1980 = 100. Although a simple arithmetic change, it causes distortions in the time series (the base year should be at least five years back to provide adequate trend analysis). DATAQUEST has reconverted the respective data back to the original 1975 = 100 base for your convenience and an easier comparison with previous reports.

Table E-2

ESTIMATED FRENCH ECONOMIC INDICATORS
(FF Billions, Seasonally Adjusted at Annual Rates)

		Yearly				Quarterly					Yearly		
		1978	1979	1980	1981	82:2	82:3	82:4*	83:1*	83:2*	1982	1983*	1984*
GDP	FF	2,140.9	2,439.5	2,758.4	3,087.4	3,509.6	3,500.1	3,568.8	3,642.5	3,710.4	3,488.1	3,748.1	4,134.8
Real GDP (FF1975)	FF	1,635.1	1,689.3	1,708.5	1,712.7	1,746.9	1,730.3	1,727.4	1,721.4	1,715.4	1,733.3	1,716.4	1,741.7
Percent Change		3.8	3.3	1.1	0.2	4.3	-3.8	-0.7	-1.4	-1.4	1.2	-0.9	1.5
GDP Deflator (1975=100)		130.9	144.4	161.5	180.3	200.9	202.3	206.6	211.6	216.3	201.2	218.4	237.4
Percent Change		9.5	10.3	11.8	11.7	11.9	2.7	8.6	9.8	8.9	11.7	8.5	8.7
Industrial Production (1975=100)		112.2	117.9	115.7	113.1	112.2	109.9	109.9	109.5	109.2	110.8	109.5	111.9
Percent Changes		2.1	5.2	-1.9	-2.3	4.2	-8.2	0.0	-1.4	-1.3	-2.1	-1.2	2.2
Fixed Capital Formation	FF	458.9	521.0	597.1	649.5	732.1	726.4	724.4	722.4	720.4	720.6	719.9	758.1
Percent Change		9.3	13.5	14.6	8.8	18.9	-3.1	-1.1	-1.1	-1.1	10.9	-0.1	5.3
Wholesale Prices (1975=100)		118.2	133.9	145.8	161.8	178.7	182.1	183.7	188.5	193.6	179.7	195.1	212.2
Percent Change		4.4	13.3	8.8	10.9	10.5	7.6	3.5	10.6	10.9	11.1	8.6	8.8
Consumer Prices (1975=100)		130.8	144.8	164.2	185.9	207.5	210.3	214.2	219.8	224.7	208.3	226.9	247.7
Percent Change		9.2	10.7	13.4	13.3	12.7	5.4	7.6	10.6	9.1	12.0	8.9	9.1
Money Supply (M1)	FF	536	599	635	739	783	804	821	844	869	821	909	999
Percent Change		11.2	11.8	6.1	16.3	13.4	10.9	8.5	11.4	12.1	11.1	10.7	9.9
Official Discount (Rate: Percent)		9.5	9.5	9.5	9.5	9.5	9.5	9.5	9.5	9.5	9.5	9.5	9.5
Exchange Rate (US$/FF)		0.22	0.24	0.24	0.18	0.16	0.14	0.14	0.15	0.14	0.15	0.13	0.14

*DATAQUEST estimate

Source: International Monetary Fund
DATAQUEST

Table E-3

ESTIMATED JAPANESE ECONOMIC INDICATORS
(Yen Trillions, Seasonally Adjusted at Annual Rates)

		Yearly				Quarterly					Yearly		
		1978	1979	1980	1981	82:2	82:3	82:4	83:1*	83:2*	1982	1983*	1984*
GDP	¥	200.7	218.9	235.8	251.1	263.2	267.5	267.1	270.2	273.3	263.9	276.4	293.1
Real GDP (¥1975)	¥	171.2	180.2	188.8	196.1	201.6	203.4	204.4	205.8	206.9	201.8	208.1	215.6
Percent Change		5.1	5.2	4.8	3.9	7.9	3.7	1.8	2.8	2.1	2.9	3.1	3.6
GDP Deflator (1975=100)		117.2	121.5	124.9	128.1	130.6	131.5	130.7	131.3	132.1	130.8	132.8	135.9
Percent Change		3.6	3.6	2.8	2.5	1.1	2.7	-2.3	1.8	2.4	2.1	1.6	2.3
Industrial Production (1975=100)		126.8	136.1	142.4	143.8	144.9	144.7	142.9	144.3	145.9	144.6	147.7	153.5
Percent Changes		6.3	7.3	4.7	1.0	-2.3	-0.4	-4.7	3.6	4.6	0.5	2.2	3.9
Fixed Capital Formation	¥	62.4	70.2	75.4	78.1	77.1	79.2	79.5	78.5	77.5	79.5	75.3	77.5
Percent Change		11.1	12.6	7.4	3.6	0.3	11.1	1.3	-5.1	-5.1	1.7	-5.3	3.0
Wholesale Prices (1975=100)		104.4	112.1	131.9	133.8	135.7	136.9	136.8	134.2	133.1	136.2	133.4	137.9
Percent Change		-2.6	7.3	17.8	1.4	1.2	3.9	-0.4	-7.6	-3.5	1.8	-2.1	3.4
Consumer Prices (1975=100)		122.6	127.1	137.2	143.9	147.5	148.2	149.4	148.9	149.7	147.7	151.1	156.2
Percent Change		3.8	3.6	7.9	4.9	4.1	1.9	3.4	-1.1	1.9	2.6	2.3	3.4
Money Supply (M1)	¥	64.8	66.9	65.6	72.2	77.1	79.1	76.4	77.1	77.8	76.4	78.8	81.4
Percent Change		13.4	3.2	-1.9	9.9	6.6	11.4	1.6	3.5	3.6	5.8	3.1	3.4
Official Discount (Rate: Percent)		3.5	6.3	7.3	6.1	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5
Exchange Rate (¥/US$)		210	219	226	220	244	258	259	235	236	248	234	230

*DATAQUEST estimate

Source: International Monetary Fund
DATAQUEST

Table E-4

ESTIMATED U.K. ECONOMIC INDICATORS
(£ Billions, Seasonally Adjusted at Annual Rates)

		Yearly				Quarterly					Yearly		
		1978	1979	1980	1981	82:2	82:3	82:4*	83:1*	83:2*	1982	1983*	1984*
GDP	£	165.4	193.4	226.1	251.5	264.8	276.2	283.4	286.4	289.6	271.2	290.8	314.6
Real GDP (£1975)	£	113.7	115.5	113.3	110.9	111.1	113.7	114.6	114.9	115.3	112.9	115.3	118.2
Percent Change		3.7	1.7	-1.9	-2.1	-3.9	9.7	3.1	1.1	1.3	1.7	2.1	2.5
GDP Deflator (1975=100)		145.6	167.5	199.6	226.6	238.4	242.9	247.2	249.2	251.2	240.2	252.2	266.2
Percent Change		10.9	15.1	19.2	13.5	11.1	7.6	7.2	3.3	3.2	5.9	5.1	5.6
Industrial Production (1975=100)		110.5	113.1	105.9	100.5	101.2	101.7	101.6	102.9	103.7	101.3	103.7	106.5
Percent Changes		4.2	2.4	-6.4	-5.2	1.3	2.1	-0.4	5.1	3.2	0.8	2.3	2.7
Fixed Capital Formation	£	29.7	34.5	39.4	39.3	38.6	41.6	38.8	39.4	40.6	40.4	41.5	42.6
Percent Change		15.6	15.9	14.3	-0.1	-35.7	31.7	-25.5	6.2	11.8	2.6	2.7	2.6
Wholesale Prices (1975=100)		153.4	172.1	200.1	221.2	238.2	242.1	246.8	251.2	254.4	240.4	256.1	273.9
Percent Change		9.1	12.1	16.3	10.6	6.5	6.4	8.1	7.2	5.1	8.6	6.5	6.9
Consumer Prices (1975=100)		146.1	165.8	195.6	218.7	238.4	239.6	241.3	243.3	245.9	237.5	249.2	263.4
Percent Change		8.3	13.5	17.9	11.9	12.7	1.9	2.9	3.3	4.4	8.6	4.9	5.7
Money Supply (M1)	£	27.1	29.5	30.6	35.7	37.5	37.9	39.9	39.1	40.1	39.9	42.1	45.1
Percent Change		16.3	9.1	3.9	16.5	10.3	4.8	21.1	-7.9	10.1	11.9	5.5	7.1
Official Discount (Rate: Percent)		12	17	14	12	12	12	12	12	12	12	12	12
Exchange Rate (US$/£)		1.92	2.12	2.24	2.03	1.78	1.73	1.65	1.53	1.54	1.75	1.55	1.75

*DATAQUEST estimate

Source: International Monetary Fund
DATAQUEST

Table E-5

ESTIMATED WEST GERMAN ECONOMIC INDICATORS
(DM Billions, Seasonally Adjusted at Annual Rates)

		Yearly				Quarterly					Yearly		
		1978	1979	1980	1981	82:2	82:3	82:4	83:1*	83:2*	1982	1983*	1984*
GDP	DM	1,290.1	1,395.3	1,484.1	1,543.1	1,589.5	1,606.1	1,618.1	1,636.4	1,661.7	1,599.11	1,667.1	1,799.1
Real GDP (DM 1975)	DM	1,164.6	1,211.1	1,233.1	1,230.8	1,223.5	1,209.5	1,208.6	1,214.1	1,225.6	1,217.3	1,231.2	1,264.3
Percent Change		3.5	4.0	1.8	-0.2	-1.3	-4.6	-0.3	1.8	3.8	-1.1	1.2	2.7
GDP Deflator (1975=100)		110.8	115.2	120.4	125.4	129.9	132.8	133.9	134.8	135.6	131.4	136.2	142.3
Percent Change		4.2	4.1	4.5	4.2	3.1	8.9	3.3	2.7	2.4	4.8	3.7	4.5
Industrial Production (1975=100)		112.9	118.9	118.9	115.6	114.1	110.5	108.2	109.4	111.6	112.1	113.6	117.1
Percent Changes		2.2	5.3	0.0	-2.8	-4.1	-12.3	-8.5	4.4	8.3	-3.1	1.4	3.1
Fixed Capital Formation	DM	266.8	304.8	337.9	339.4	329.2	333.2	330.1	325.1	332.2	328.1	333.5	343.2
Percent Change		9.8	14.2	10.9	0.4	11.7	4.9	-3.8	-6.0	8.7	-3.3	1.7	2.9
Wholesale Prices (1975=100)		107.8	112.9	121.5	130.9	138.2	139.5	139.9	139.6	140.7	138.6	141.7	146.4
Percent Change		1.1	4.9	7.5	7.8	3.9	3.5	1.4	-1.1	3.2	5.9	2.2	3.3
Consumer Prices (1975=100)		111.1	115.6	122.1	129.2	135.5	136.9	137.9	138.6	139.4	136.1	140.2	146.1
Percent Change		2.8	4.1	5.6	5.8	5.9	4.3	2.9	1.8	2.5	5.3	3.1	4.2
Money Supply (M1)	DM	219.1	225.8	234.2	230.6	239.9	242.1	247.3	255.8	264.8	247.3	275.8	305.5
Percent Change		14.5	3.1	3.7	-1.5	8.6	3.7	8.7	15.6	9.4	7.2	11.5	10.8
Official Discount (Rate: Percent)		3.0	6.0	7.5	7.5	7.5	7.0	5.0	4.0	4.0	6.8	4.5	5.0
Exchange Rate (US$/DM)		0.50	0.55	0.55	0.44	0.42	0.40	0.40	0.42	0.41	0.41	0.41	0.46

*DATAQUEST estimate

Source: International Monetary Fund
DATAQUEST

Appendix E—Economic Data and Outlook

Table E-6

MONTH-END SELLING PRICES FOR BANK TRANSFERS
(Expressed in U.S. Dollars)

Year	Month	Canada (US$/Can$)	France (US$/FF)	Japan (US$/¥)	United Kingdom US$/£	W. Germany (US$/DM)
1981	January	0.8363	0.2071	0.004891	2.3995	0.4769
	February	0.8317	0.1993	0.004778	2.2020	0.4695
	March	0.8430	0.2010	0.004732	2.2370	0.4744
	April	0.8305	0.1914	0.004640	2.1490	0.4550
	May	0.8311	0.1799	0.004472	2.0730	0.4293
	June	0.8326	0.1747	0.004407	1.9240	0.4180
	July	0.8099	0.1701	0.004158	1.8375	0.4042
	August	0.8314	0.1699	0.004324	1.8390	0.4073
	September	0.8281	0.1800	0.004300	1.8060	0.4305
	October	0.8326	0.1786	0.004307	1.8700	0.4505
	November	0.8498	0.1790	0.004674	1.9605	0.4522
	December	0.8435	0.1757	0.004554	1.9170	0.4460
	Average	0.8337	0.1839	0.004519	1.8741	0.4429
1982	January	0.8258	0.1696	0.004387	1.8800	0.4316
	February	0.8139	0.1643	0.004211	1.8195	0.4188
	March	0.8140	0.1595	0.004037	1.7850	0.4145
	April	0.8205	0.1642	0.004248	1.8150	0.4297
	May	0.8041	0.1634	0.004111	1.7840	0.4259
	June	0.7725	0.1462	0.003900	1.7340	0.4060
	July	0.7968	0.1464	0.003891	1.7410	0.4072
	August	0.8071	0.1436	0.003848	1.7200	0.4013
	September	0.8089	0.1402	0.003726	1.6950	0.3958
	October	0.8157	0.1382	0.003640	1.6780	0.3909
	November	0.8083	0.1435	0.003997	1.6300	0.4055
	December	0.8089	0.1485	0.004271	1.6200	0.4199
	Average	0.8080	0.1523	0.004022	1.7418	0.4123
1983	January	0.8087	0.1430	0.004171	1.5240	0.4056
	February	0.8141	0.1452	0.004190	1.5125	0.4105
	March	0.8104	0.1375	0.004187	1.4840	0.4119
	April	0.8159	0.1355	0.004204	1.5600	0.4063
	May	0.8131	0.1318	0.004183	1.6050	0.3956
	June	0.8147	0.1308	0.004117	1.5275	0.3931

Source: The Wall Street Journal
DATAQUEST

Glossary

Accelerated life testing—Operating semiconductors beyond maximum ratings to induce premature failures as an aid to estimating semiconductor life expectancy.

Acceptance of offer—The agreement by the buyer to meet the terms and conditions of the offer by the seller.

Acceptance of order—The agreement by the seller to transfer the goods and services ordered by the buyer for the stated consideration.

Acceptance sampling—Inspection of a sample for the purpose of predicting the number of defects present in the entire lot of semiconductors.

Access time—The time required to retrieve data from a memory location.

Acknowledgment—A form used by a supplier to advise a purchaser that the order has been received; usually implies acceptance of the order.

A/D (Analog to Digital)—A circuit that transforms a linear (analog) representation formation to a digital representation. The digital representation is usually in the binary format of 1s and 0s.

Administered price—Price established by the conscious policy of a seller rather than by competitive market forces.

Administrative lead time—The interval between initiating a requisition and placing an order.

Ad valorem (according to value)—A term usually applied to a customs duty charged upon the value only of goods that are dutiable, regardless of quality, size, or other considerations. The ad valorem rate of duty is expressed as a percentage of the value of the goods, usually determined from the invoice.

Agent—One acting on behalf of another, called a principal, in dealing with third parties.

Aligner—A type of wafer fab equipment used for applying a mask to a wafer.

Alpha particles—A form of radiation that has low penetration ability and is emitted by certain radioactive elements or isotopes.

ALS—Advanced Low-power Schottky logic, a family of TTL integrated circuits.

ALU (Arithmetic Logic Unit)—(1) A type of bipolar MSI circuit. (2) The part of a computer's CPU that performs numerical operations.

Ambient temperature—The temperature of the adjacent medium.

Glossary

Amplifier—An integrated circuit that increases signal amplitude without a significant change in waveform.

Analog—(1) A quantity whose values are continuous rather than discrete. (2) A type of circuit (also known as a linear circuit) in which the variables are continuous rather than discrete values.

ANSI—American National Standards Institute.

Approved list—List of suppliers who have been evaluated and are believed to be capable of acceptable performance.

AQL (Acceptable Quality Level)—Denotes the maximum tolerable percentage of rejects occurring during test or inspection.

ASP—Average Selling Price.

Arrival notice—Information sent by the carrier to the consignee advising of the arrival of a shipment.

ARO—After Receipt of Order.

Array—A regular pattern (gates, cells, devices).

As is—The goods are offered for sale without warranty or guarantee. The purchaser has no recourse against the seller for quality or condition of the goods.

Assembly—The IC manufacturing steps of mounting a die in a package, bonding the pads to the package leads, and sealing the package.

Asset turns—The ratio of sales to total assets.

Assignment—Transfer of property title to another party. Frequently used in connection with bills of lading that are endorsed (assigned) over to another party (the assignee) by the owner (assignor). Such endorsement gives to the party named the title to the property covered by the bill of lading.

Asynchronous—Not having a fixed time reference.

Atto—A prefix meaning 10^{-18}.

ATE (Automatic Test Equipment)—Used in the production test or incoming inspection of ICs.

Automatic refresh circuitry—Circuitry that periodically restores the charge in a semiconductor memory cell to maintain data retention.

Backdoor selling—The bypassing of the purchasing function by a salesperson, who visits the department using the product.

Glossary

Back order—That portion of an order that cannot be shipped by the seller at the scheduled time and has been reentered for shipment at a later date.

Bank(er's) acceptance—An instrument used in financing foreign trade, allowing the payment of cash to an exporter to cover all or part of the amount of a shipment. Such an arrangement originates with the foreign importer, who instructs his local bank to provide for a commercial acceptance credit with, for example, a San Francisco bank in favor of a named American exporter; the San Francisco bank then issues an acceptance credit, in effect guaranteed by the foreign bank, to the exporter, under the terms of which a time bill of exchange maturing in 60 or 90 days may be drawn. Supported by the required evidence of shipment, the bill of exchange is accepted by the exporter's bank by endorsement on the face of the bill, thus signifying that it will pay the bill at maturity. The exporter may retain the bill until maturity or sell it on the discount market.

Barter—Exchange of one kind of goods for another instead of an exchange involving money.

Base—The control electrode of a bipolar transistor.

BASIC (Beginners All-purpose Symbolic Instruction Code)—A computer language used in personal computers and time-shared systems.

Baud rate—The rate at which bits are transferred in a communication link. One baud equals one bit per second.

Best case—A situation in which all parameter values are at their most desirable limits.

Biased sampling—Sampling procedures that may not guarantee a truly representative or random sample.

Bid—An offer, such as pricing, whether for payment or acceptance. A quotation specifically given to a prospective purchaser upon request, usually in competition with other suppliers. An offer, by a buyer, to a supplier.

BiFET (Bipolar Field Effect Transistor)—Refers to a type of semiconductor comprising both bipolar and MOS structures.

BI-FET—A trademark of National Semiconductor Corporation, used in reference to BiFET products.

Bill back—A contract provision for the customer to pay a price premium for the parts received in the event the customer does not take the full dollar value originally committed.

Bill of entry—A detailed statement by an importer showing the nature and value of goods entered at customs.

Glossary

Bill of materials—An engineering drawing that lists all purchased components in a piece of electronic equipment.

Bill of sight—A customs document allowing the consignee to see goods in the presence of a customs officer before paying duties. The inspection is requested by the importer to obtain details that will facilitate preparation of a correct bill of entry. This bill of entry must be completed within three days of the bill of sight; otherwise goods are removed to a government warehouse.

Binary—(1) A two-valued numbering system that usually uses the symbols "1" and "0." This numbering system is used with computers because computer logic and memory devices are two-valued: "on"/"off" or "high"/"low." (2) A flip-flop.

Bipolar transistor—A device used to control current flow in solid matter. A small base current controls the large emitter-to-collector current flow, similar to a valve controlling the flow of a liquid. Refer to Section 12 for a detailed description of a bipolar transistor structure.

Bit (BInary digiT)—A digit having a value of "1" or "0."

Blanket order—A master contract for reducing the number of small orders, providing for the supplier to furnish products for a specified period of time and either at predetermined prices or according to a formula for revising prices due to market or other conditions.

Bonded warehouse—Warehouse approved by customs or government officials for the storage of dutiable goods prior to trans-shipment or payment of duty.

Bonding pads—Metalized areas on a semiconductor chip to which lead connections may be made.

Brand-name product—A product whose manufacturer is named or otherwise identified on the product or on the container of the product.

Bubble—(1) A sharp increase in IC supply for a limited time. (2) A polarized magnetic domain, usually representing a binary digit, that looks like a bubble when examined under polarized light at high magnification. See Section 12 for a description of magnetic bubble memories.

Buffer stock—A quantity of material kept in storage to safeguard against unexpected shortages. See "safety stock."

Buyer's market—A situation considered to exist when goods can easily be obtained and when the market conditions (usually more supply than demand) cause goods to be priced at the purchaser's estimate of value.

Buyer's option—The privilege of buying within a given period of time, usually at a price and under terms and conditions agreed upon in advance of the actual sale. The seller expects the prospective buyer to pay for an option.

Glossary

Burn-in—Refers to the operation of semiconductor devices at an elevated temperature or temperatures over a time interval, usually with the intent of identifying early-life failures in ICs.

Bus—In an electronic system, a line or lines for transferring information or control between the elements of the system.

Byte—A group of eight bits. A byte is usually used to represent an alphabetic or control character, a digit, or a punctuation mark.

CAD—Computer Aided Design.

CAD/CAM—Computer Aided Design and Computer Aided Manufacturing.

CAGR—Compound Annual Growth Rate.

CAM—(1) Content Addressable Memory. (2) Computer Aided Manufacturing.

Captive line—A semiconductor production facility owned by the user.

Carrier's lien—A carrier's claim on merchandise to assure collection of freight charges.

CAS—Column Address Strobe. (See RAS.)

Caveat emptor ("Let the buyer beware")—A warning that goods or services are bought at the buyer's risk.

Caveat venditor ("Let the seller beware")—A warning that the seller, in some situations, is liable to the buyer if the goods delivered are different from those described in the contract of sale.

CCD (Charge Coupled Device)—An MOS device used for information storage or imaging applications.

Cerdip—Ceramic dual in-line package.

Certificate of compliance—A supplier's certification that the goods or services in question meet certain specified requirements.

Change order—Purchaser's written authority to the supplier to modify a purchase order.

Chip—A small piece of silicon containing one semiconductor component, circuit, or function, ranging from a diode to a microcomputer.

Chip carrier—A type of small IC package.

Glossary

Class—(1) Refers to the purity of the atmosphere in the clean room of a semiconductor fabrication facility; e.g., class 100 means a maximum of 100 particles 0.5 microns or larger in each cubic foot of air. (2) Refers to the level of semiconductor screening and documentation for government use; e.g., class S (space and satellite programs), class B (manned flight), class C (ground support).

Clean room—An environmentally controlled area, usually a wafer fabrication or inspection facility. Temperature, humidity, and purity of the environment are all carefully controlled.

Clock rate—The repetition frequency of the basic timing signal applied to a logic function.

CML (Current Mode Logic)—A bipolar, emitter-coupled logic form.

CMOS (Complementary MOS)—An integrated circuit that uses both P-channel and N-channel transistors to gain the primary advantages of very low standby power and high noise immunity.

C.O.D. (Cash on Delivery)—Payment is due when delivery is made.

CODEC (COder DEcoder Circuit)—An integrated circuit that codes a voice signal into a binary waveform or decodes a binary waveform into a voice signal. Such circuits are now used in digital communications applications.

Collector—The majority receptor in a transistor; the major source of electrons in a pnp transistor.

Collector-OR—A logical OR NOT function achievable by interconnecting certain ICs having uncommitted collector outputs.

Commission merchant—An agent, broker, or factor employed to sell goods and services consigned or delivered by the principal, for a compensation called a commission.

Competitive bid—A competitive price offer.

Composite sample—A sample taken by mixing together parts from several areas of a product lot.

Conditional sale—Title is retained by the supplier as security for payment, although possession transfers to the buyer.

Consignment—Goods shipped for future sale or other purpose, title retained by the shipper (consignor), for which the receiver (consignee), upon acceptance, is accountable. Consigned goods become part of the consignor's inventory until sold. The consignee may be the eventual purchaser, may be the agent through whom the sale is effected, or may otherwise dispose of the goods as agreed to with the consignor.

Glossary

Consular invoice—A document required by a foreign government showing specific information about the consignor, consignee, value, description, and other details of a shipment being imported.

Contingent inventory—Stock items that are held against a possible future order.

Contracts, types of—(1) Firm fixed-price payment of a specific amount when the goods and services called for are delivered and accepted. (2) Cost reimbursement—seller is reimbursed for all costs of performance as outlined in the contract. A cost reimbursement contract may be written as: cost-plus-incentive fee, cost-plus-fixed fee, or cost sharing.

Co-op advertising—Distributor advertising that is partially paid for by a credit from the manufacturer of the advertised product.

COS/MOS (COmplementary-Symmetry MOS)—Trademark of RCA to represent its special type of CMOS circuit.

Cost breakdown—Detailed analysis of the supplier's quoted pricing.

Cost-plus—A pricing method whereby the purchaser agrees to pay the supplier the costs incurred in producing the goods plus a stated percentage of the cost of the goods or a fixed amount.

COT—Customer Owned Tooling, usually referring to masks for a semiconductor device prepared and owned by the customer.

CP/M—Control Program for Microcomputers, a trademark of Digital Research Incorporated, denoting an operating system that is widely used in microprocessors and microcomputers.

Custom Circuit—A semiconductor circuit designed to meet the needs of one specific customer.

Customs duties—Taxes, tolls, or duties levied upon products that cross a political boundary.

Cycle stock—The active part of inventory, i.e., the quantity that is depleted, resupplied, depleted, and resupplied over and over. Safety stock is excluded.

Cycle time—The minimum interval required to complete a full operation, such as writing into a RAM or performing an instruction.

DAC—Digital to Analog Converter.

D/A converter (Digital to Analog Converter)—A circuit that transforms a digital representation to linear (analog) representation.

Glossary

DESC (Defense Electronics Supply Center)—The U.S. Government Command, located at Dayton, Ohio, responsible for implementing and monitoring specifications and for supervising supplier certifications and qualifications according to MIL-M-38510 and MIL-S-19500.

Design rules—Rules constraining IC topology to assure fab process compatibility.

Dice—Two or more semiconductor chips.

Dice bank—An inventory of chips maintained as a hedge against delays due to problems in the manufacturing of semiconductors.

Die—One semiconductor chip.

Dielectric isolation—An IC design and process technique used to improve breakdown characteristics and/or increase resistance to radiation.

Diffusion—The use of a fab furnace to drive an impurity into a wafer.

Digital Circuit—A circuit whose values or levels are binary.

Digitizing—(1) Converting an analog signal into a form recognizable by a digital circuit. (2) The process of encoding information into a form recognizable by CAD/CAM equipment.

Diode—A semiconductor element that favors unidirectional current flow; a PN junction.

DIP—Dual In-line Package.

Discrete device—A single circuit element packaged separately; e.g., a transistor or a diode.

Double-sampling plan—An inspection method in which the inspection of the first sample of a lot leads to a decision to accept, to reject, or to take a second sample. The inspection of the second sample, when required, then leads to a decision to accept or reject the lot.

Double poly—The use of two layers of polysilicon for increased IC density.

Drag business—Component sales that are the by-product of sales of related devices.

Drain—The majority carrier collector in an MOS transistor.

DRP (Distribution Resource Planning)—The application of the materials requirements planning (MRP) technique to the management of product or materials distribution. DRP includes computerized financial planning, business simulation, and closed loops (feedback).

Glossary

Duty—A tax levied by political body on the import, export, or consumption of products.

Dynamic RAM—A memory device that must be electrically refreshed frequently (many times each second) to maintain information storage.

E. and O.E. (Errors and Omissions Excepted)—An abbreviation placed on a quotation or invoice by a supplier reserving the right to change the amount charged if this amount is later found to be incorrect.

EAROM—Electrically Alterable Read Only Memory.

E-beam—A sophisticated system that uses an electron beam for maskmaking or for projecting patterns onto wafers. E-beam equipment enables smaller geometries (typically less than 1 micron) than are possible under other production methods.

ECL (Emitter Coupled Logic)—A form of integrated circuit used to implement very-high-speed logic functions.

Economic lot size—The number of units required to minimize costs over a specified time period.

Edge triggered—A circuit actuated by an input signal transition.

EEPROM—Electrically Erasable Programmable Read-Only Memory.

EIA—Electronic Industries Association. A U.S. association of companies involved in the electronics business.

E^2PROM—(See EEPROM).

ELECTRO—An electronics trade show held annually in the northeastern United States.

Emitter—The source of majority carriers in a transistor; the electron receptor in a pnp transistor.

Emulator—Hardware or a combination of hardware and software that exactly reproduces the operation and performance of other hardware.

EOL—End Of Life

EOQ (Economic Order Quantity)—The best quantity to buy at one time to achieve the lowest unit cost to the user.

Epitaxial—Silicon grown on a crystalline silicon substrate.

EPROM (Erasable Programmable Read-Only Memory)—IC that can be erased with an ultraviolet light source and reprogrammed by the user.

Glossary

Established book price—A price included in a price list or other form that is regularly maintained by a supplier and is published or made available for inspection by customers.

Established market price—A current price, established in the usual and ordinary course of trade between buyers and sellers free to bargain, that can be substantiated from sources independent of the manufacturer or vendor.

Ethernet—A cable-based communications network designed to link office equipment originated by Xerox Corporation.

Eutectic (alloy)—That combination of two or more metals that gives the lowest possible sharply definable melting point.

Evaporator—Semiconductor production equipment used for depositing a thin film on a wafer.

Expediting—Maintaining constant pressure on a supplier to obtain punctual deliveries. Field expediting occurs when the purchaser uses a representative at the supplier's plant during the manufacturing period.

Experience curve—An expression of the relationship between unit cost and the total accumulated production volume (initially popularized by the Boston Consulting Group).

Fab—Abbreviation of wafer fabrication.

FAE—Field Applications Engineer.

Fanout—The driving capability of an IC output lead, usually expressed in the number of inputs that can be driven.

FAST—A Fairchild Semiconductor trademark denoting a Family of Advanced Schottky TTL.

Femto—A prefix meaning 10^{-15}.

FET—Field Effect Transistor (MOS transistor).

FFT (Fast Fourier Transform)—An IC or other circuit used for time-to-frequency domain conversion.

FIFO (First In, First Out)—The first put in is the first taken out. Usually refers to inventory handling and accounting. May also refer to a type of memory or shift register.

Finished goods inventory—Products that are ready for shipment and are on the shelf in anticipation of customer orders.

Firmware—Instructions committed to some form of ROM hardware.

Glossary

Firm offer—A definite proposal to sell at specified terms, binding the proposer until the stated time of expiration. A firm bid is a similar proposal to buy.

Fixed-price contract—Contract based on pricing that will not differ from that agreed upon at the time the contract is mutually accepted.

Flash converter—A type of digital to analog converter that performs a parallel, as opposed to serial, conversion. Used primarily in applications requiring high speed, such as video.

Flat-pack—A type of IC package that has its leads in a plane parallel to the chip.

Flip-chip—A packaging technique in which the IC chip is mounted face down.

Flip-flop—A logic IC or part of an IC that can remember a "1" or a "0."

F.O.B. (Free On Board)—Means the seller must transfer the goods to the transporting carrier without cost to the buyer. The term f.o.b. must be qualified by the name of a location, such as shipping point. The stated f.o.b. point is usually the location where title passes from the seller to the buyer.

FORTH—A high-level computer language.

FPGA—Field Programmable Gate Array in which programming is accomplished by blowing fuse links or shorting base-emitter junctions.

FPLA—Field Programmable Logic Array in which programming is accomplished by blowing fuse links or shorting base-emitter junctions.

Franchise agreement—An agreement between a distributor and a manufacturer that sets the price at which the distributor buys products and defines other terms and conditions such as price protection and stock rotation. The Wright-Patman Act gives the legal definition of a franchise.

Free goods—Goods not subject to a customs duty.

Free list—A list of materials or products exempt from customs duties.

Frit—Material used to attach a die to a package.

Furnace—Fab equipment that performs diffusion at approximately 1,200°C.

Fuse links—Structures used in PROMs, PLAs, or other ICs to allow the customer to store data or modify logic functions using programming hardware.

Glossary

GaAs (Gallium Arsenide)—A type of semiconductor material offering very high speed operation in excess of 10 Gigahertz.

Gain-bandwidth product—A measure of transistor or amplifier efficiency.

Gate—(1) The MOS transistor equivalent of the base electrode in a bipolar transistor; the control electrode of an MOS transistor. (2) Part of an IC that performs a simple logic function such as NAND or NOR. (3) A quality control point in a manufacturing process.

Gate array—An IC consisting of a structured pattern of logic devices that are processed except for the final interconnect metalization. These devices are offered as a standard product and then customized to meet each customer's unique requirements.

Geometry—Sometimes used to refer to the minimum feature size of a semiconductor structure, such as gate length or line width.

Gigahertz (GHz)—One billion cycles per second.

Gray market—A market for components other than the conventional market among manufacturer, distributor, and OEM.

HAL (Hardwired Array Logic)—A trademark of Monolithic Memories, Incorporated, referring to a mask-programmed version of programmable logic array devices.

Hand-to-mouth buying—Procuring a smaller-than-normal quantity for immediate requirements only, based on the expectation of market oversupply or price reduction.

Hardware—ICs and other electronics and their associated boards, connectors, and mechanical packaging.

Hedge—Any purchase intended to reduce losses arising from price fluctuations; specifically, a purchase entered into for the purpose of balancing a purchase already made, or under contract, to offset the effect of price fluctuation.

Hybrid—A package containing two or more IC chips and associated electrical components in a single cavity.

Hot lot—An expedited production run of ICs.

IC—Integrated Circuit.

IEEE—Institute of Electrical and Electronic Engineers.

IEEE-488—An electronic bus interface standard developed by the IEEE.

I^2L (Integrated Injection Logic)—A low-power bipolar IC form.

Glossary

Industrial distributor—A distributor that buys from a components or parts manufacturer and sells to an equipment manufacturer.

Integrated circuit—A semiconductor structure combining the functions of many electronic components (i.e., transistors, resistors, capacitors, and diodes) interconnected on a single chip.

INT STD 123—A quality standard introduced and trademarked by Advanced Micro Devices, Inc.

Inventory turns—The number of times inventory is turned over in a given year. Derived by dividing revenues by average inventory.

Inventory turnover—Average inventory level compared with withdrawals in a given time interval.

I/O (Input/Output)—A bidirectional IC lead or port.

Invoice—A bill showing the character, quantity, price, terms, nature of delivery, and other particulars of goods sold or of services rendered.

Ion implantation—The use of an ion beam to bombard a silicon wafer, altering the concentrations of P-type or N-type material. This method of doping allows for very precise control of the device parameters.

ISSCC—International Solid State Circuits Conference, usually held in February.

JAN (Joint Army Navy)—A registered trademark of the U.S. Government used to mark semiconductors that fully comply with MIL-M-38500 or MIL-S-19500.

JAN TX—Used to identify a diode or transistor that has been subjected to special burn-in screening according to MIL-S-19500.

JAN TXV—Used to identify a diode or transistor subjected to special screening according to MIL-S-19500, including pre-cap visual inspection witnessed by a U.S. Government source inspector.

JEDEC—Joint Electronic Devices Engineering Council, a U.S. group working on IC standardization and other electronic industry problems.

Jellybean—A commodity-type product.

JFET—Junction Field Effect Transistor.

JJ—Josephson Junction.

Joint venture—When two or more parties enter into a single enterprise for their mutual benefit without the intention of continuous pursuit, they have entered a joint venture. They are essentially partners in the venture.

Glossary

Josephson junction—A form of very-high-speed IC device that is based on superconductivity at very low temperature.

Juice sales—A selling technique that relies primarily on the salesperson's rapport with the purchaser. This rapport may be enhanced by green stamps, football tickets, lunches, or other "juice."

K—(1) 1,000. (2) 1,024, when defining memory size.

Kilobit—1,024 bits.

Kilohertz (KHz)—1,000 cycles per second.

Laser—A collimated light beam source.

Laser trimmer—Fab equipment used for opening metal connections on IC chips.

Latch—A pair of cross-coupled gates that stores a "1" or "0."

LCC—Leadless Chip Carrier, a form of high-density packaging for IC chips.

LCCC—Leadless Ceramic Chip Carrier.

LCD- Liquid Crystal Display device.

Lead time—The interval from date of ordering to date of delivery that the buyer must reasonably allow the supplier to prepare product for shipment.

Learning curve—(1) Refers to efficiency gained through accumulated knowledge. (2) Refers to the experience curve (see experience curve).

LED—Light Emitting Diode.

Letter of credit—A letter containing a request that the addressee sell the person named therein commodities on credit, or give him something of value, with the intention that the addressee later seek payment from the writer of the letter. It is used by a buyer to secure goods without cash available at the time of the purchase.

LIFO (Last In, First Out)—Refers to products held in inventories. May also refer to a form of semiconductor memory.

Linear—A semiconductor circuit that operates with continously variable signals at the input, output, or both.

Line item—A component listing on an order.

Logic—The use of digital signals in structured ways to perform tasks such as addition, accumulation, comparison, and inference.

Glossary

LOI (Letter Of Intent)—A preliminary contract used in situations where some items, quantities, prices, and delivery dates are known, but where the principal contract provisions require additional negotiations. It is an interim agreement to permit the start of production or delivery of the products.

Love 'em, load 'em, leave 'em—A process whereby a components manufacturer induces a distributor to stock product but does not provide any follow-up support.

LS (Low-power Schottky)—Usually refers to LSTTL.

LSI (Large Scale Integration)—ICs comprising 100 to 10,000 gates or gate equivalents.

LSTTL (Low-power Schottky TTL)—A popular bipolar logic IC form.

LTPD (Lot Tolerance Percent Defective)—A measure of IC quality.

Lump sum—The price agreed upon between purchaser and supplier for a group of items without breakdown of individual values; a lot price.

Make or buy—The decision that determines which semiconductors should be manufactured in the buyer's plant and which semiconductors should be purchased.

Mask—A thin sheet of material with a design pattern on it, used in selectively exposing areas on a wafer during the semiconductor fabrication process. The mask is used in the same way that a photographic negative is used to produce a positive print.

Masked ROM—A read-only memory programmed to the customer's specified pattern during the manufacturing process.

Mb (Megabit)—1,048,576 bits.

MB (Mega Byte)—1,048,576 bytes.

MBD—Magnetic Bubble Device.

MBM—Magnetic Bubble Memory.

Mega—(1) One million. (2) 1,048,576 when defining memory size.

Megabit (Mb)—1,048,576 bits.

Megabyte (MB)—1,048,576 bytes.

Memory—An IC designed for the storage and retrieval of information in binary form.

Glossary

Metal gate—An older but still popular technique for controlling MOS transistor current flow by applying a control voltage to an aluminum gate.

MHz—MegaHertz. One million cycles per second.

Micro—(1) Very small. (2) One millionth.

Microampere—One millionth of an ampere.

Microcell—Frequently used IC elements, standardized for design simplification.

Microcircuit—An IC.

Microcomputer—An IC or a board containing ICs than can perform all the functions of a computer.

Micron—One millionth of a meter.

Microprocessor—An IC capable of performing CPU and other functions, including memory.

Microsecond—One millionth of a second; the period of a 1-MHz signal.

MIDCON—An electronics trade show held in the midwestern United States.

Mil—One thousandth of an inch.

MIL-M-38510—The general U.S. military specification for integrated circuits.

MIL-S-19500—The general U.S. military specification for diodes and transistors.

MIL STD—MILitary STandarD.

MIL-STD-750—A U.S. military standard that defines environmental processing, screening conditions, and test methods for diodes and transistors.

MIL-STD-883—A U.S. military standard that defines integrated circuit environmental processing, screening conditions, and test methods.

Milli—One thousandth.

Mixing privileges—A contract provision allowing a purchaser to vary the quantity of various part types without a cost penalty, provided the total dollar volume of the order is maintained.

MNOS (Metal Nitride Oxide Semiconductor)—An IC technique used to make some types of EAROMS.

Glossary

Monolithic—A device constructed from a single piece of material.

MOS—Metal Oxide Silicon.

MOS Transistor—A voltage mode device used to control current flow in solid matter. The device uses a gate conductor, such as silicon or metal (usually aluminum), over a very thin insulator (usually oxide). A voltage applied to the gate controls the flow of current between source and drain.

MOSFET—MOS Field Effect Transistor.

MPU—MicroProcessor Unit.

MRP (Material Requirements Planning)—A scheduling technique that involves calculating material requirements for the purposes of (a) rescheduling open orders to meet changing requirements, and (b) generating replenishment orders.

MRP II (Manufacturing Resource Planning)—An evolutionary form of computerized material requirements planning that encompasses financial planning, business simulation, and closed loops (feedback) that cross organizational lines.

MRO—Maintenance and Repair Order.

MSI (Medium Scale Integration)—ICs comprising of 10 to 1,000 gates or gate equivalents.

MTBF (Mean Time Between Failures)—A measure of IC reliability, usually expressed in hours.

MTL (Merged Transistor Logic)—A high-density bipolar logic form, also referred to as integrated injection logic (I^2L).

Multiplier—A linear IC used for generating the product of two binary numbers.

Muscle—The ability to command the distributor's attention or "muscle out" other manufacturers. Used to describe a manufacturer of a component that sells well.

NAND Gate—Part of an IC that performs the logic function AND-Not.

Nano—One billionth part.

Nanosecond—One billionth of a second. In this time electrical pulses travel approximately 12 inches.

Narrow line (supplier, distributor)—One having a limited number of products in its product line.

Glossary

NCC (National Computer Conference)—A computer trade show held annually in the United States.

N-channel—A type of MOS transistor.

NEDA—National Electronics Distributors Association.

NEMA—National Electronics Manufacturers Association.

Nibble mode—An operating mode of a dynamic RAM in which a short sequence (nibble) of bits is accessed at a higher than normal random access rate.

Niche market—A small, specialty market, as opposed to the "mainstream" market.

NMOS—N-channel Metal Oxide Silicon, a type of semiconductor in which the majority carriers are electrons.

Non-volatile—A semiconductor device that does not lose information when power is removed.

NOR gate—Part of an IC that performs the OR-NOT logic function.

NOVRAM—Trademark of Xicor, Inc., that refers to NVRAM products.

NPN—A type of bipolar transistor constructed using a P-type base.

ns (Nanosecond)—One billionth of a second.

NVRAM (Non-Volatile Random Access Memory)—A read/write semiconductor memory device that does not forget (or lose information) when power is removed.

OEM (Original Equipment Manufacturer)—A purchaser who acquires goods for incorporation into a product manufactured for sale, usually without changing the purchased items.

Off the shelf—Available for immediate shipment.

Op amp—Operational Amplifier, a type of IC that generates an amplified output that is exactly proportional to its input.

Open-end order—Specifies price, terms, conditions, and the period covered, but not necessarily the quantity. Shipments are made against purchase orders, according to the buyer's requirements.

Opto (Optoelectronic)—A type of IC used for converting electricity to light or vice versa.

Ordering costs—Fixed costs associated with placing a purchase order, regardless of the dollar amount or number of units in the order.

Glossary

OS&D (Over, Short, and Damage report)—A report showing discrepancies in billing received and freight on hand.

Oven—Equipment used to burn-in ICs.

P^2CMOS (Poly-Poly CMOS)—Trademark of National Semiconductor Corporation; used in reference to a unique CMOS structure that uses two layers of polysilicon.

Package—The container used to encapsulate a semiconductor chip.

Packing list—A document itemizing the contents of a specific package or shipment.

Pad—A metallized area on a chip, usually 10 to 35 square mils, used for bonding or test probing.

PAL (Programmable Array Logic)—PAL is a trademark of Monolithic Memories, Inc, referring to a family of logic devices that are customer programmable.

Parasitic effects—The results of the interaction of the stray electrical components in an IC. Such stray components result from the high-speed operation of circuit elements in close proximity.

Pascal—A high-level computer language.

Passivation—The use of a protective layer on the surface of a chip.

Pattern Generator—(1) Equipment used in IC maskmaking. (2) Equipment used to create test sequences.

P-channel—A type of MOS structure, in which the majority carriers are holes.

Photoresist—A light-sensitive coating used in photolithography.

Photolithography—The manufacturing process step of coating and selectively exposing a wafer for selective etching.

Piggyback orders—Assume a distributor agrees to supply a portion (e.g., 10 to 20 percent) of the materials needed by a high-volume equipment manufacturer, and the distributor provides a buffer stock to take up the month-to-month variation in the quantities needed, charging a price slightly higher (10 to 20 percent) than the component manufacturer charges. The orders placed by the distributor in this case are called piggyback orders.

Pico—One trillionth part.

Picosecond—One trillionth of a second. Light or electrical pulses travel about 12 mils (0.012 inches) in one picosecond.

Glossary

PLA (Programmable Logic Array)—A form of LSI containing a structured, partially interconnected set of gates and inverters that are mask programmed.

Planar—Refers to a semiconductor structure in which the circuit elements are located within a thin layer near the chip surface.

Plasma etch—Refers to the use of a highly ionized gas (plasma) as a step in the manufacture of high-density semiconductors.

Plastic package—A molded IC package, usually a DIP. The majority of ICs and discretes are manufactured in plastic packages.

PLL (Phase Locked Loop)—A type of linear IC used in frequency modulated (FM) circuits.

PMOS—P-channel MOS.

PN—Positive-Negative, usually refers to a diode.

PNP—A type of bipolar transistor that has an N-type base.

Port of entry—A port officially designated by the government at which foreign goods are admitted legally into the receiving country.

Polysilicon—A silicon layer grown on a wafer in a furnace.

Power transistor—A transistor designed for high-current, high-voltage applications.

Presence—A supplier organization that effectively communicates with the market and has an understanding of the customers' needs, is said to have presence.

Price analysis—Evaluating a prospective price without evaluating the separate cost elements and proposed profit of the individual offerer. It may be accomplished by company current quotations; by company price quotations and contract prices with current quotations for the same or similar items; by using rough rules of thumb; or by company proposed prices with independently developed estimates.

Price maintenance—The price of a product established by a supplier below which the product may not be sold.

Price/Performance—A ratio used as a measure of intrinsic merit of a hardware solution to a signal processing or information processing problem. It allows for comparison of alternative approaches.

Price protection—(1) An agreement between a supplier and a purchaser to grant the purchaser any reduction in price that the supplier may establish for the product. (2) A clause in a distributor agreement that gives the distributor credit for inventory when prices are lowered by the manufacturer, preventing the distributor from losing money on the affected stock.

Glossary

Probe—A test lead designed to make contact with a bonding pad or other test point on a chip.

Probe card—A test card containing two or more probes and used for probing IC chips.

Programming—(1) Writing binary patterns into ROMs and other ICs. (2) Writing a sequence of instructions for use by a CPU.

Projection alignment—An optical alignment procedure in semiconductor fabrication in which the mask does not touch the wafer.

PROM (Programmable Read Only Memory)—A ROM that may be altered by the user by blowing fuse links or shorting base-emitter junctions.

Promo—A promotional activity.

Propagation delay—Time required for a signal to travel along a wire or to be processed through an IC.

Proprietary product—A product made and marked by a supplier having the exclusive right to manufacture and sell it.

Pseudostatic—A dynamic memory IC that includes on-chip automatic refresh circuitry.

Pull through—A manufacturer's promotional efforts that are said to pull product through the distribution channel.

Purchase order—The purchaser's document used to formalize a procurement transaction with a supplier.

Push money—Incentive payments to distributor salespersons that cause them to favor a given manufacturer's products.

Purchase requisition—A form used to request the purchasing department to procure goods or services from suppliers.

QPL (Qualified Parts List)—Refers to semiconductors that have been certified by the U.S. Government for use on government programs.

QUIP (QUad In-line Package)—An IC package with four rows of leads.

Quotation—A statement of price, terms of sale, and description of goods or services offered by a supplier to a prospective purchaser. When given in response to an inquiry, it is usually considered an offer to sell.

Glossary

Rad—A unit of measure of radioactive dosage.

Rad hard (Radiation hardened)—a type of IC used in higher-radiation military or aerospace environments.

RADC (Rome Air Development Command)—The government organization, located at Griffiss Air Force Base, New York, that develops specifications for all U.S. military services.

RAM (Random Access Memory)—Currently means read/write random access memory one that may be "written into" or "read out of" with equal ease.

RAS (Row Address Strobe)—Input signal used by address-multiplexed RAMs.

Rebate—A sum of money returned by the supplier to the purchaser in consideration of the purchase of a specified quantity or value of goods within a specified time.

Redundancy—The addition of functions that may be substituted for other functions in the event of a manufacturing defect or a hardware failure, to greatly improve yield, reliability, or both.

Refresh—The restoration of a logic level to its original voltage/current value.

Register—A set of latches or flip-flops organized as a row; it may operate in serial or parallel mode or both.

Rep—A manufacturer's representative.

Requirements contract—A contract covering long-term needs that is used when the total quantity needed cannot be fixed but can be stated with maximum and minimum limits, with deliveries on demand.

Restocking charge—A charge to cover the cost of preparing returned merchandise for resale.

Retail distributor—A distributor who sells to consumers.

Reticle—A master plate from which masks are made.

Returns—Items returned to a seller because of faulty performance, misshipment, or lack of need.

RF—Radio Frequency.

RFI—(1) Request For Information. (2) Radio Frequency Interference.

RFP (Request For Proposal)—A solicitation document used in procurement. In governmental purchasing, when an RFP so states, the government reserves the right to award a contract based on initial offers received without any written or oral discussion with offerers.

Glossary

RFQ (Request For Quotation)—A solicitation document used in negotiated procurements. An RFQ is a request for data. Quotes submitted in response to it are not offers that the buyer will accept without some confirmation or discussion with offerers.

ROM (Read Only Memory)—An IC memory that is usually programmed during manufacture and is not normally altered during its use.

RS-232—A communications standard that defines electrical and timing parameters for interface.

RTL (Resistor Transistor Logic)—A form of low-power bipolar IC logic used extensively in the 1960s.

Safety stock—Stock maintained in stores to protect against stockouts.

Sales Agency Agreement—An agreement between a representative and manufacturer that defines the sales territory and establishes a commission structure.

SAM (Served Available Market)—The market available to a supplier and served by that supplier's products, services, or both.

Sampling—(1) Acquiring statistics from a mass of data without taking a complete census of the data. (2) The early phase of a product life cycle in which the supplier provides the user with limited sample quantities for evaluation purposes.

Schottky diode—A type of diode, invented at Bell Laboratories in 1960, that has a relatively fast response time due to its low capacitance.

Schottky TTL—A form of transistor-transistor logic using Schottky diodes as transistor clamps to enhance speed and/or producibility.

SCR—Silicon Controlled Rectifier.

SDLC—Synchronous Data Linked Communications, an IBM standard communications protocol.

Second source—A supplier that offers one or more products that are available from a total of two or more suppliers.

Seller's market—A situation that exists when goods cannot easily be secured and the goods are priced by suppliers; caused by more supply than demand.

Semiconductor—(1) A material that is neither a good conductor or insulator and whose electrical properties can be altered by the selective introduction of impurities into its crystalline structure. (2) An electronic device made using semiconductor material.

Glossary

SEM (Scanning Electron Microscope)—A type of microscope used for semiconductor die examination at very high magnification.

SEMI (Semiconductor Equipment and Materials Institute)—A U.S. trade organization of semiconductor equipment and materials manufacturers.

Semicustom—(See Gate array; see Masked ROM.)

Shift register—An IC used for temporary synchronous storage of data.

Ship and debit—Usually applies to orders beyond the quantities covered by published price lists. The distributor ships the parts and debits the component manufacturer for the difference between the distributor cost and a pre-negotiated high-quantity cost. Shipment is from distributor stock.

Si—Symbol for Silicon, the basic ingredient of most semiconductors in use today.

SIA (Semiconductor Industry Association)—An organization of members of the semiconductor industry, formed to promote their interests.

Side-brazed package—A type of ceramic IC package that has the metal leads brazed to the sides of the package.

Si gate (Silicon gate)—A form of MOS processing using polysilicon rather than metal to form the gates.

Silicide—Refers to a type of metal alloy used to improve semiconductor performance by reducing resistivity.

Silicon dioxide—A material often used as an insulating layer in semiconductor manufacture. It may be formed by heating the silicon wafer in a furnace in the presence of wet or dry oxygen.

Silicon foundry—An IC manufacturer specializing in processing using customer owned tooling (COT).

Silicon software—Refers to the use of large ROMs or other non-volatile semiconductor memory for storage of computer programs.

SIP (Single In-line Package)—A type of IC package that has a single row of leads.

Slice—A wafer.

Sole source—The only supplier, regardless of the marketplace.

Software—(1) A program or set of instructions used by a computer. (2) Merchandising material such as data sheets and application notes.

Solid state—Hardware made up of ICs.

Glossary

SOM—Share Of Market.

SOS (Silicon On Sapphire)—A form of integrated circuit that offers high-speed operation but is relatively expensive because of the cost of the sapphire substrate used in its manufacture.

Source—(1) In an MOS transistor, the majority carrier emitter. (2) A semiconductor supplier or distributor.

SOUTHCON—An electronics trade show held annually in the southeastern United States.

Specialist—A seller that concentrates on one product category, e.g., RAMs.

Specification—A complete statement of the technical requirements of a product or service, and of the procedure to be followed to determine if the requirements are met.

Spif—A promotional prize awarded to distributor salespersons when they achieve a given quota of sales of a component manufacturer's product.

Spot market—A localized market of short duration.

Sputterer—A type of IC manufacturing equipment used for depositing metal on wafers.

SSI (Small Scale Integration)—An IC containing fewer than 10 gates or gate equivalents.

Stagnant inventory—Stock items that do not sell.

Standard—A semiconductor product generally available from one or more suppliers.

Static RAM—A RAM that maintains memory as long as power is applied, and does not require refreshing.

Stockout—Condition that exists when the supply of a product in stores is completely exhausted.

Stock rotation—A policy instituted by the components manufacturer that allows the distributor to return older parts periodically so that they can be replaced with newer ones.

STTL (Schottky TTL)—A high-speed form of TTL.

Synchronous—A signal with a fixed time reference.

S-100—A microcomputer bus interface standard based on a 100-pin connector.

Glossary

TAM—Total Available Market.

TC—Temperature Coefficient.

Telecom—Contraction of telecommunications.

Threshold—The point at which a semiconductor starts to conduct.

Ti-Tungsten—An alloy, used for IC fuses, comprised of titanium and tungsten.

TO-3, TO-5, TO-18, etc. (Transistor case Outlines)—TO-3, TO-5, etc., refer to specific case sizes.

Tracer—A request to a transportation line to locate a shipment for the purpose of expediting its movement or establishing delivery.

Transistor—An active semiconductor that has three electrodes; used for amplification or switching.

TRI-state—Describes an IC output that may source current, sink current, or be turned off. TRI-state is a trademark of National Semiconductor Corporation.

TTL or T^2L (Transistor-Transistor Logic)—A popular form of bipolar logic IC.

UART (Universal Asynchronous Receiver Transmitter)—An IC used for communications interface of digital data.

ULA (Uncommitted Logic Array)—A form of gate array.

USART (Universal Synchronous Asynchronous Receiver Transmitter)—An IC used for communications interface.

UV EPROM (UltraViolet Electrically Programmable ROM)—An EPROM that is erasable with an ultraviolet light source.

VHSIC (Very High Speed Integrated Circuit) Program—An advanced development program that is intended to develop advanced semiconductors for U.S. Government and for defense purposes.

Visual inspection—An inspection performed without the use of test instruments.

VLSI (Very Large Scale Integration)—An IC chip containing more than 10,000 devices.

VPA—Volume Purchase Agreement.

Wafer—A thin (10 to 20 mils) disk of semiconductor material usually 3 inches (75mm), 4 inches (100mm), or 5 inches (125mm) in diameter, from which dice are fabricated.

Glossary

Wafer fab—The IC production process, from raw wafers through a series of diffusion, etching, photolithographic, and other steps, to finished wafers.

Wafer stepper—Fab equipment used for exposing multiple images of an IC pattern onto a wafer.

Warehouse (bonded)—A warehouse in which products are held under bond to the government subject to transshipment or payment of customs on the products.

Waybill—A document prepared by a carrier at the point of origin of a shipment, showing the point of origin, destination, route, consignor, consignee, description of shipment, and amount charged for transportation, and forwarded to the carrier's agent at the transfer point.

WESCON (WEStern electronics CONference)—A trade show usually held in September in the western United States.

Working plates—Masks used in wafer fab.

Worst case—The situation that exists when all parameter values are at the least desirable limits.

Yield—The ratio of acceptable parts to total parts attempted; a measure of production efficiency.

Zener—A diode that has a controlled, reverse-voltage/current relationship.

10K ECL—A popular form of ECL ICs having gate delays of approximately 2 ns.

100K ECL—A popular form of ECL ICs having gate delays of approximately 1 ns.

5400 series—A popular line of TTL logic for military applications.

7400 series—The most popular line of TTL logic for commercial applications.

Glossary

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SEMICONDUCTOR USER INFORMATION SERVICE INDEX

The following index includes topics covered in Volume I of the Semiconductor User Information Service. The Index will be updated quarterly and a temporary index for any section updated during the course of a quarter will be sent with that section.

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