Semiconductor Equipment and Materials Service 1985–1986 Newsletters and Bulletins

Dataquest
a company of The Dun & Bradstreet Corporation

1290 Ridder Park Drive
San Jose, California 95131
(408) 971-9000
Telex: 171973
Fax: (408) 971-9003

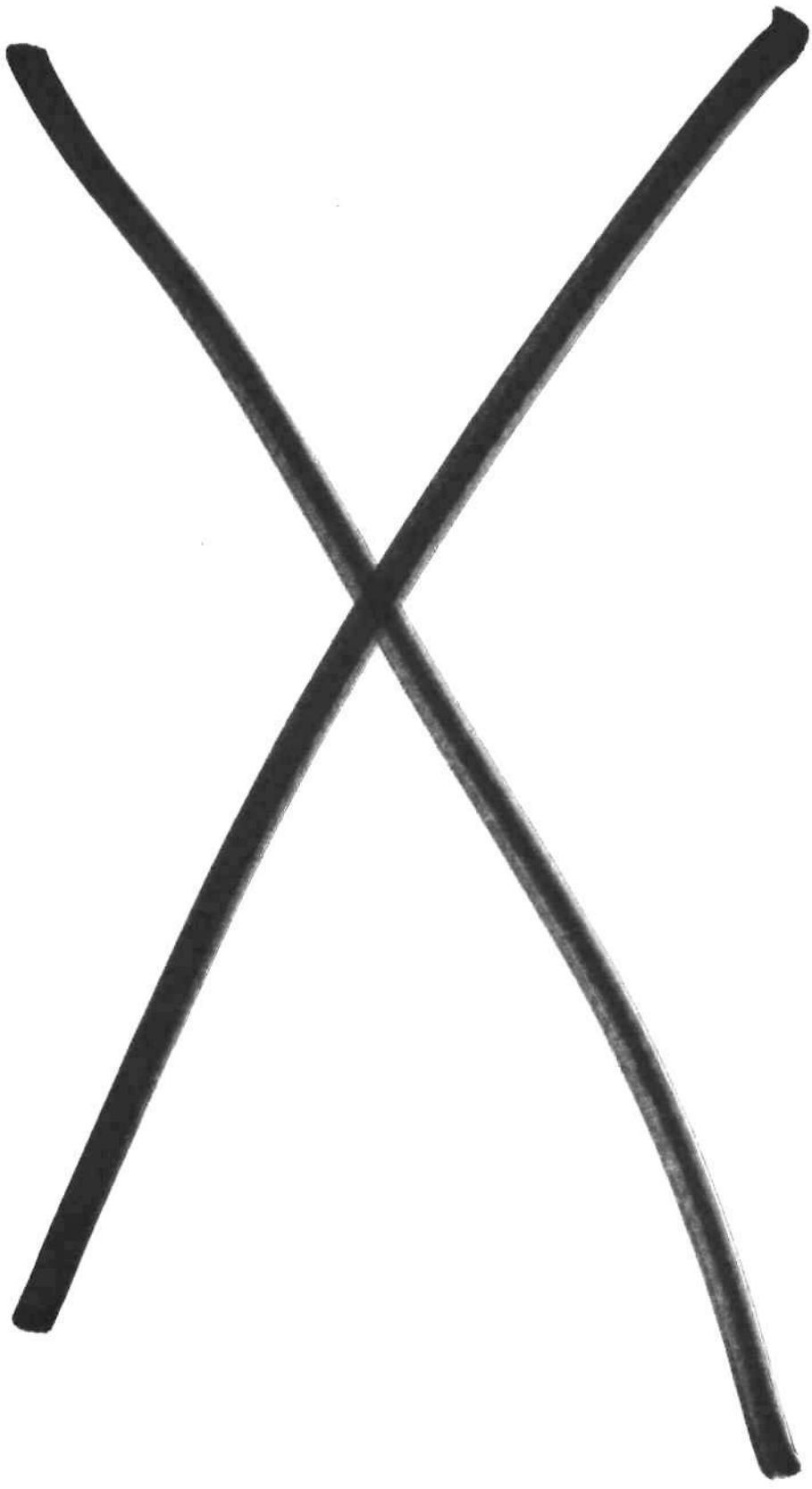
Sales/Service offices:

UNITED KINGDOM
DATAQUEST UK Limited
144/146 New Bond Street
London W1Y 9FD
United Kingdom
(01) 409-1427
Telex: 266195
Fax: (01) 491-2790

GERMANY
DATAQUEST GmbH
Rosenkavalierplatz 17
D-8000 Munich 81
West Germany
(089) 91-1064
Telex: 5218070
Fax: (089) 91-2189

FRANCE
DATAQUEST SARL
41, rue Ybry
92522 Neuilly-sur-Seine Cedex
France
(1)47.58.12.40
Telex: 630842
Fax: (01)46.40.11.23

JAPAN
DATAQUEST Japan, Ltd.
Taiyo Ginza Building
7-14-16 Ginza, Chuo-ku
Tokyo 104, Japan
(03) 546-3191
Telex: J32768
Fax: (03) 546-3198



Dataquest
a company of
The Dun & Bradstreet Corporation

November 24, 1986

Dear SEMS Client:

A recent newsletter from Dataquest's Semiconductor User Information Service came to my attention and I wanted to provide you with a copy because I believe that it presents a clear and thorough analysis of a very complex issue. The newsletter, entitled "The Semiconductor Agreement: Intentions and Reality," describes the U.S.-Japan semiconductor trade agreement and explores the near- and long-term impact of the trade agreement on procurement, pricing and market access. I believe that the information and analysis contained in this newsletter is important for our clients because of the impact of the semiconductor trade agreement on the dynamics of the semiconductor industry worldwide. I hope that you find this newsletter interesting reading.

Best Regards,

Peggy Marie Wood

Peggy Marie Wood
Research Analyst
Semiconductor Equipment
and Materials Service

Enc.

1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 971-9000 Telex 171973 Fax (408) 971-9003

Dataquest
A company of The Dun & Bradstreet Corporation

USER UPDATE

SUIS Code: Newsletters
1986-33

THE SEMICONDUCTOR AGREEMENT: INTENTIONS AND REALITY

SUMMARY

This newsletter concerns the near- and long-term pricing repercussions of the U.S.-Japan semiconductor agreement reached on July 31, 1986. It reviews the agreement's main points and the potential effects and resulting strategies for semiconductor manufacturers and users. It analyzes the agreement's intentions and potential near- and long-term effects and concludes with specific suggestions for how the situation can best be managed.

AGREEMENT OVERVIEW

The semiconductor agreement between the United States and Japan revolves around two key issues:

- Cost/price monitoring of semiconductor devices to insure that prices of semiconductors exported into the United States do not fall below costs
- Increased Japanese market access by U.S. semiconductor manufacturers

Cost/Price Monitoring

The agreement resulted in the suspension of dumping charges on all EPROMs and 256K and 1Mb DRAMs by the U.S. Department of Commerce (DOC). Instead, the DOC will monitor on a quarterly basis the prices and costs of certain Japanese-manufactured and exported semiconductor products.

The DOC uses a formula to construct the quarterly Foreign Market Values (FMVs). This formula (A + B + C + D = Foreign Market Value) is made up of the following four parts:

- Material costs, including some R&D
- Fabrication costs
- General sales and administration expenses, including some R&D (not less than 10 percent of the above two costs)
- Profit (not less than 8 percent of the above three costs)

The formula is applied on a company-by-company basis using proprietary cost information to determine the minimum price of each company's products. This method uses real-time fabrication cost data in determining FMVs. The capacity utilization of a given company at a given time will determine in large part what that company's FMV will be. A company running at 80 percent capacity will have lower fabrication costs per unit than a company running at 50 percent capacity. The initial capacity utilization rate used can determine which companies will be continually competitive and which will continue to be uncompetitive, since a profit always has to be added to a higher manufacturing cost. Using these same guidelines, Japan's Ministry of International Trade and Industry (MITI) has agreed to monitor the following volume Japanese-exported semiconductors:

- MOS SRAMs
- ECL RAMs
- 8- and 16-bit microprocessors
- 8-bit microcontrollers
- ECL logic
- Gate arrays
- Standard cells

Market Access

The second part of the agreement facilitates greater access by U.S. semiconductor manufacturers to the Japanese market, which a Japanese governmental organization has been formed to support. The organization will:

- Provide sales assistance for foreign semiconductor producers as they attempt to penetrate the Japanese market
- Make quality assessments of foreign semiconductor products, upon request, and organize such things as research fellowship programs, seminars, and exhibitions for foreign firms

- Promote long-term relationships between Japanese semiconductor purchasers and foreign producers, including joint product development with Japanese customers

AGREEMENT EFFECTS

The effect of capacity utilization on price is illustrated by the cost model shown in Table 1.

The first round of FMVs created significant problems for Japanese semiconductor companies and for users in the United States. Larger users appeared to have managed to source product from U.S.-based suppliers or to be prebuying before the September 15, 1986, deadline. Many smaller users got caught in the crossfire.

Table 1

CONSTRUCTED PRICES FOR 256K DRAM

	Capacity			
	100%	75%	50%	25%
Processed-Wafer Cost	$178.00	$220.00	$280.00	$500.00
Cost/Chip	$ .27	$ .33	$ .42	$ .75
Test Cost/Hour	$ 27.00	$ 34.00	$ 54.00	$100.00
Wafer Probe Cost/Chip	$ .07	$ .10	$ .15	$ .28
Wafer Probe Yield	70%	70%	70%	70%
Cost/Good Chip	$ .49	$ .61	$ .81	$ 1.47
Assembly Cost	$ .14	$ .19	$ .24	$ .36
Assembly Yield	85%	85%	85%	85%
Assembly Chip Cost	$ .74	$ .94	$ 1.24	$ 2.15
Test Cost/Pkg.	$ .25	$ .36	$ .54	$ 1.01
Test Yield	90%	90%	90%	90%
Tested Device Cost	$ 1.10	$ 1.44	$ 1.98	$ 3.51
Mark, Pack, Ship	$ .20	$ .20	$ .20	$ .20
Total Mfg. Cost/Unit	$ 1.30	$ 1.64	$ 2.18	$ 3.71
R&D Expense (15%)	$ .20	$ .25	$ .33	$ .56
SG&A Expense (10%)	$ .15	$ .19	$ .25	$ .43
Profit (8%)	$ .13	$ .17	$ .22	$ .38
Foreign Market Value	$ 1.78	$ 2.25	$ 2.98	$ 5.08

Source: Dataquest
October 1986

Japan-based semiconductor companies have seen their exports to the United States decrease as prices based on yen have continued to drop in Japan, impacting company profits. The price for 256K DRAMs was ¥450 in 1985. Today the price is ¥289. The agreement has helped yen-based average selling prices increase to ¥375 or higher for sales made into the U.S. market.

It appears that the new FMVs that will become effective on October 15 will be much more palatable to customers. We expect 256K DRAMs to range in price from $2.50 to $4.00, and we expect 1Mb DRAMs to be in the $20 to $25 range for the lowest-cost suppliers. EPROM prices are outlined in our recent Research Newsletter number 1986-28, "Pricing and the Market at Odds: Revised EPROM and 256K DRAM Estimates."

Dataquest believes that the new FMVs will make life easier for U.S. buyers. The new prices indicate that buyers may expect prices to continue to decrease throughout 1987. By the end of 1987 we expect 256K DRAM prices to be close to $2.20, as shown below:

	1986		1987			
	Q3	Q4	Q1	Q2	Q3	Q4
256K DRAMs	$2.85	$2.85	$2.85	$2.50	$2.35	$2.20

We also expect 1Mb DRAMs to return to more competitive pricing than we had previously expected. We now believe that they will approach the crossover point by the end of 1987.

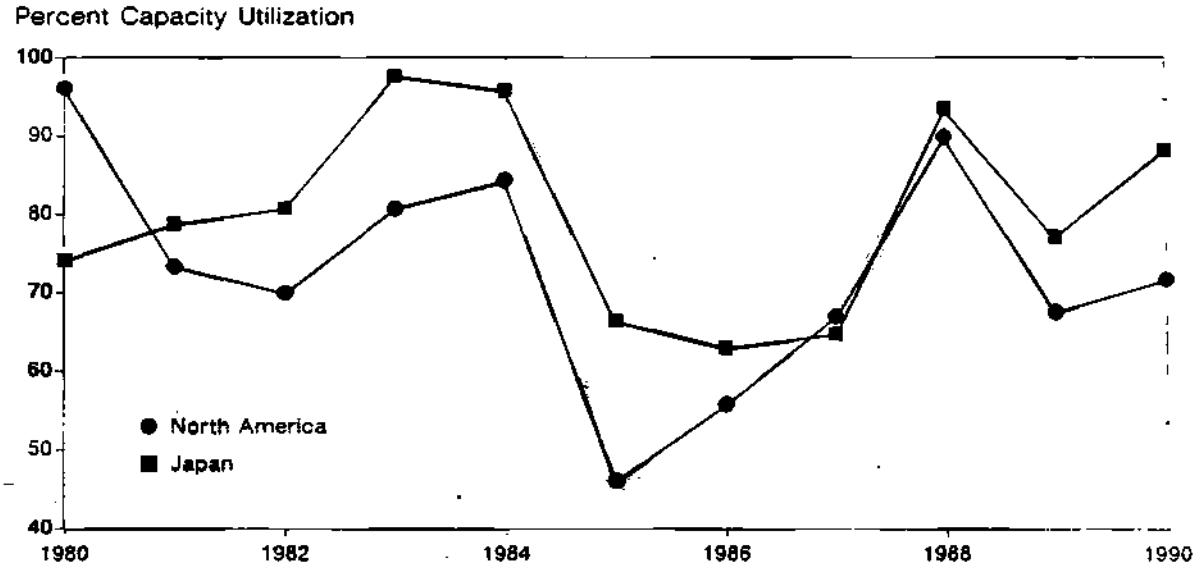
As prices in the United States reach more stable levels, the focus of the program is expected to move to other regions. We expect the Department of Commerce to take up this issue with MITI in the near future. Dataquest surveys prices in Europe, Japan, and Taiwan every two weeks, and prices in Europe and Taiwan have remained at $2.00 or less during the last month. However, our European research indicates that prices in Europe will increase from current levels in the next two quarters.

LONG-TERM IMPLICATIONS OF THE AGREEMENT

This agreement presents interesting opportunities for users and semiconductor manufacturers. Because the models used to determine the FMVs are based on capacity utilization, FMVs will decrease during market growth periods and increase during recessions when capacity utilization drops. Figure 1 shows our projection of capacity utilization for the industry for the next five years. By combining this with the data shown in Table 1, we can analyze the impact of the business cycle on FMVs. As capacity utilization drops, FMVs will tend to increase; this will effectively remove uneconomic foreign capacity from the U.S. market as demand declines and will direct more business toward U.S.-based suppliers who are not affected by the FMVs. Our current forecasts project that this will occur in 1989.

Figure 1

CAPACITY UTILIZATION--NORTH AMERICA VERSUS JAPAN



Source: Dataquest
October 1986

Another concern arising from the first round of FMVs was the price of new technologies--in this case, the 1Mb DRAM. Third quarter FMVs were double the prior market price. This had the impact of delaying the introduction of the latest technology into U.S.-manufactured equipment, giving Japanese companies a lead in this area. The long-term implications of this are far more important than any other action resulting from the agreement.

New technology has far greater impact on system cost than declining prices. Figure 2 shows how this works. Cost per function can decline by a factor of five or more for a much smaller decrease in price. Figure 3 shows how it works for memories. Each new level of cost occurs when the next generation of memory enters the market. Each new generation decreases the cost from the previous generation by a factor of five. A one-year lag in pricing causes a one-year lag in system technology. The anticipated 1Mb FMVs will prevent a near-term U.S. versus Japan system technology dichotomy.

The new FMVs of $20 to $25 for 1Mb DRAMs should correct this situation, but the impact on future generations of DRAMs remains to be seen. This is not a problem with EPROMs, however, because U.S. companies are leaders in introducing next-generation EPROMs.

Figure 2

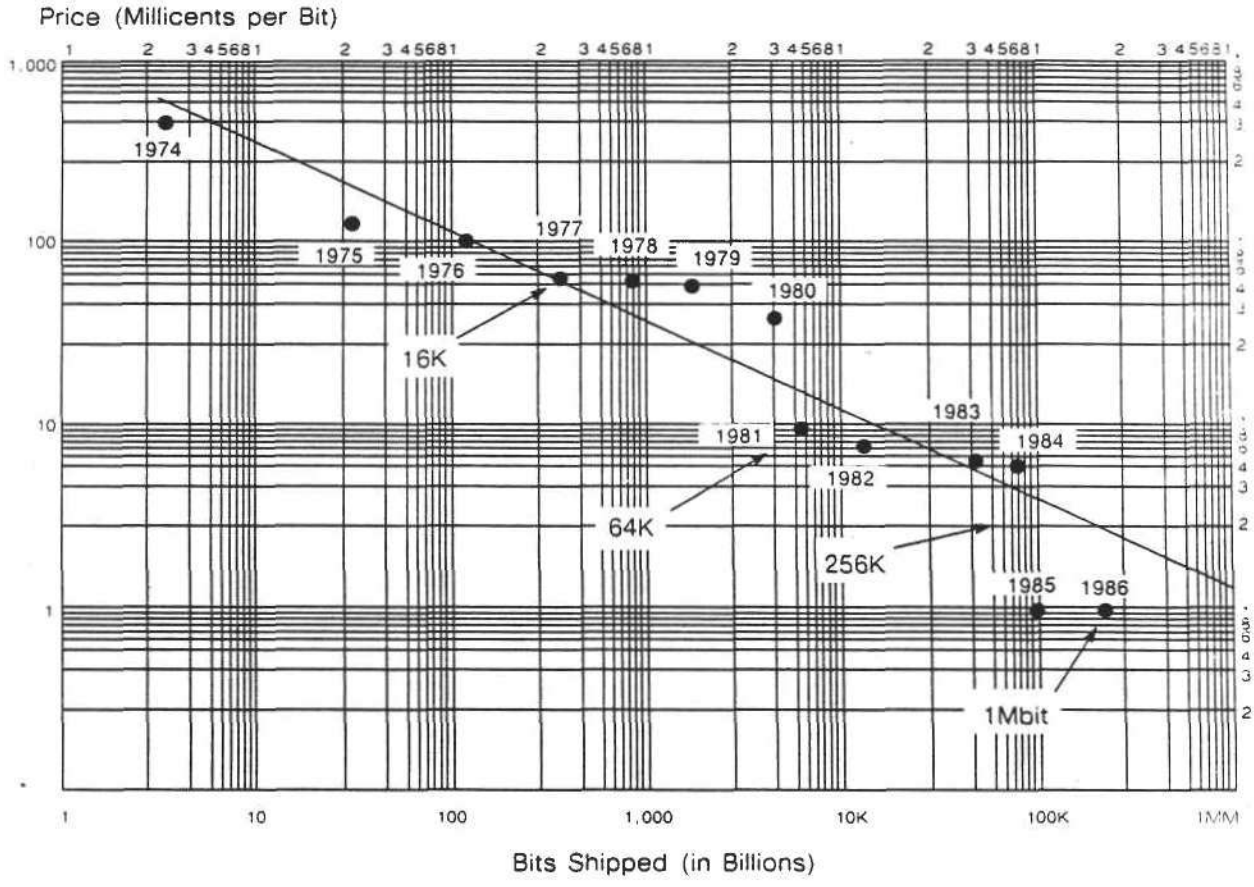
HYPOTHETICAL CHIP COST MODEL

	1984	1986
Minimum dimension	3 microns	2 microns
Wafer size	4 in.	6 in.
Processing cost	$140	$220
Chip size (mils per side)	200	250
Yield	30%	50%
Chip cost to product cost	4X	4X
Good chips	100	200
Finished chip cost	$1.49	$1.10
Finished package cost	$5.96	$4.40
Transistors/chip	50,000	211,000
Cost/transistor	9.9m¢	2.1m¢

Source: Dataquest
October 1986

Figure 3

DRAM EXPERIENCE CURVE



Source: Dataquest
October 1986

STRATEGIES FOR THE TRADE-AGREEMENT ENVIRONMENT

The trade agreement has precipitated a number of responses by semiconductor users. These responses and their implications are discussed in the following paragraphs.

Some U.S. companies are considering having memory PC boards manufactured in Japan and exported to the United States. Through this transformation of product, the FMVs are avoided. This is a good plan, but the government could close this loophole if it becomes a serious impediment to making the agreement work.

A number of users have benefited from agreements with NEC, which has manufacturing capacity in both the United States and Japan. The short-term effect obviously has been to lower prices. This will not appear to be so important with the new FMVs, but we believe that all users should develop a balanced U.S./Japanese supply base. It will enable them to shift sourcing during recessionary periods, when we expect the FMVs to increase as capacity utilization decreases. This will minimize the price impact on customers during down markets.

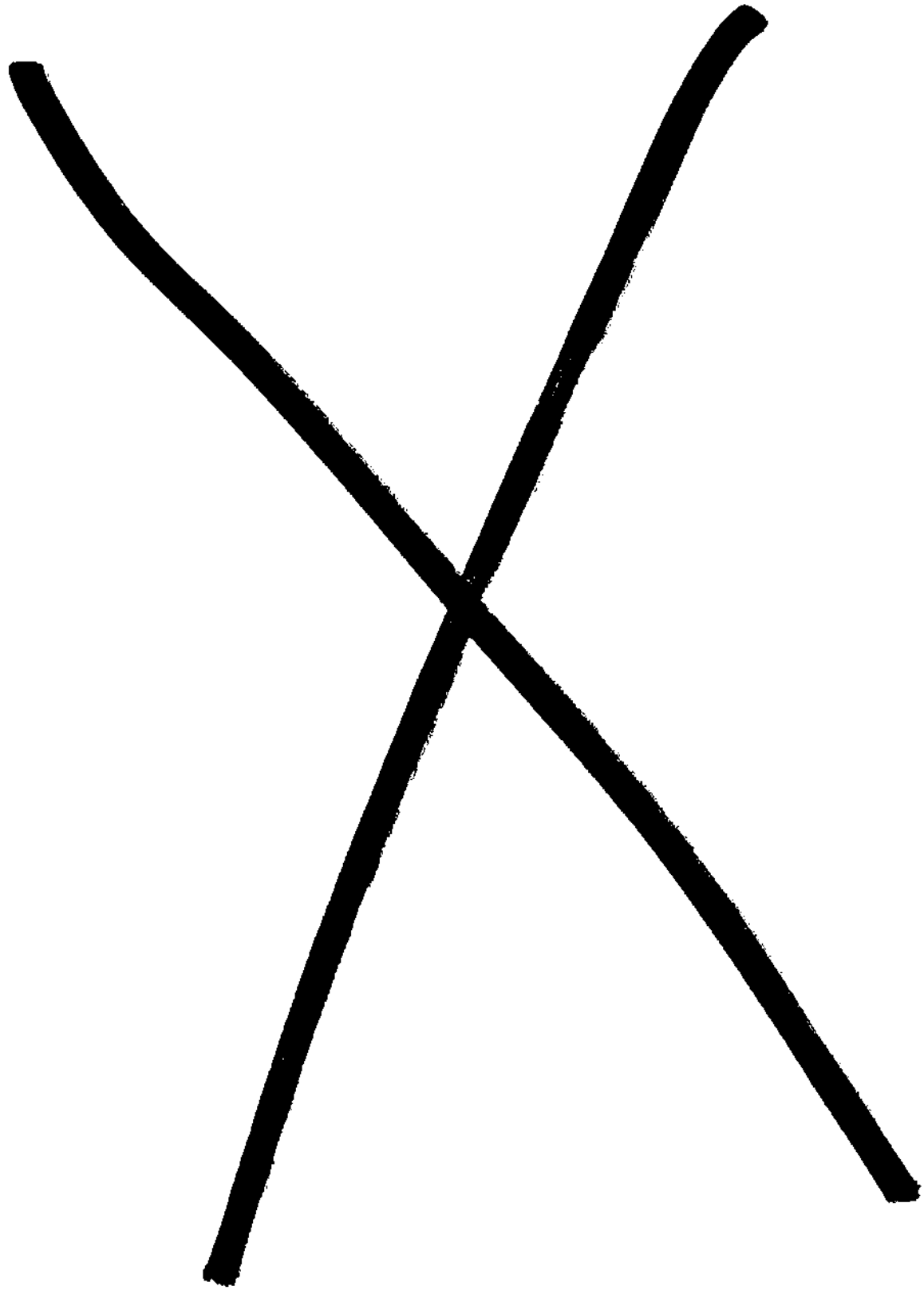
Moving to offshore manufacturing is another possible strategy. However, we believe that companies should be very careful with this, as the agreement could equalize prices worldwide (except in Japan) if it works as intended.

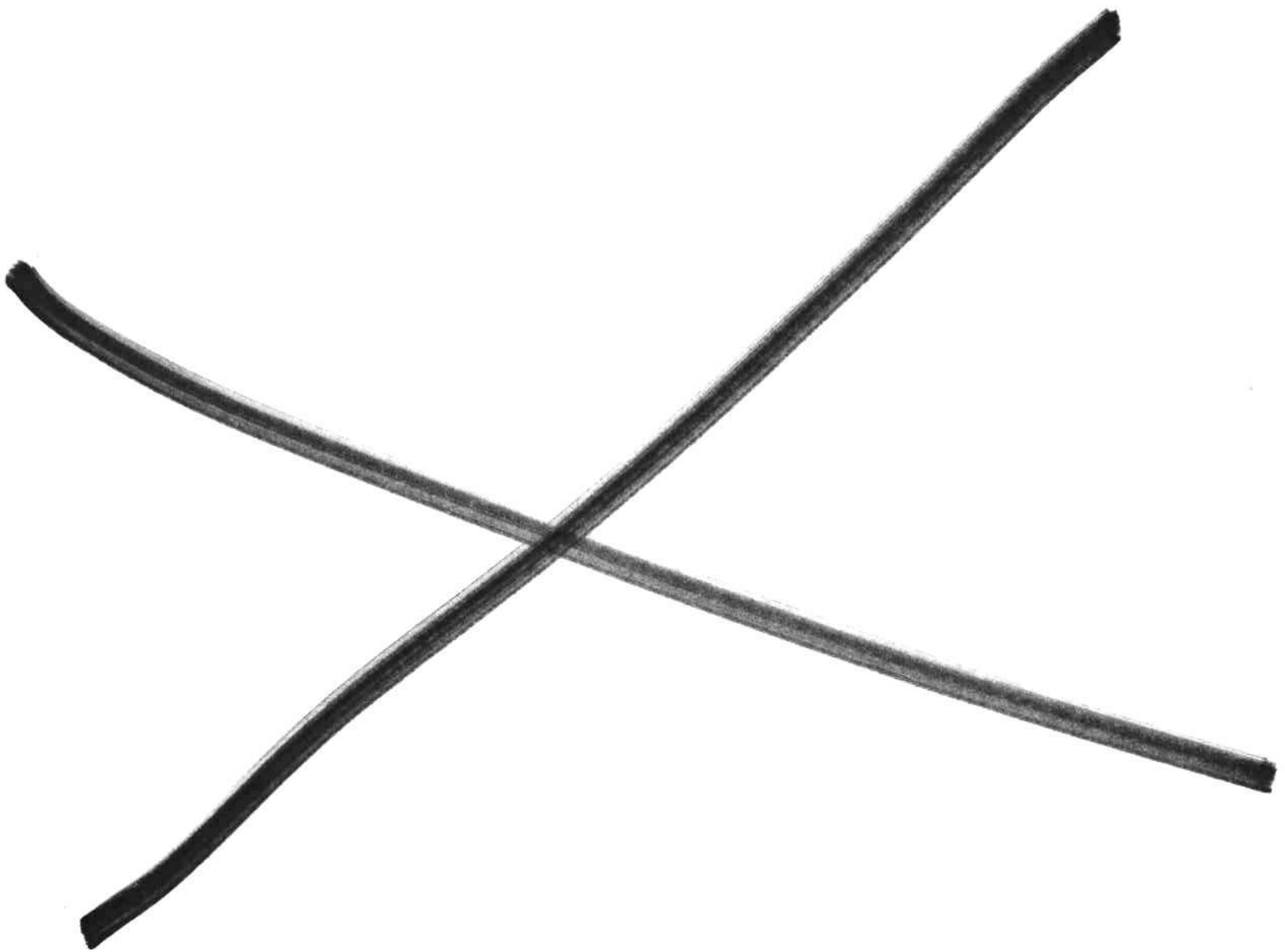
Korean suppliers offer another opportunity for lower prices, but this should be considered a short-term strategy. Korea currently supplies a small part of the market. If the U.S. government becomes interested in controlling Korean suppliers as a major source of DRAMs, we believe that Korean FMVs would be substantially higher than current prices.

DATAQUEST CONCLUSIONS

Procurement strategies under the trade agreement should remain extremely flexible. Companies should balance U.S. sources with foreign sources to be able to adjust to changes in the current business environment. Any actions taken to get around the agreement could be affected by government actions to close loopholes that could affect the intent of the agreement. We believe that the major negative effects of the agreement will subside when the new FMVs are released on October 15. The groundwork has to be done now for dealing with the long-term effects of the agreement.

Stan Bruederle
Mark Giudici





February Newsletters

The following is a list of the material found in this section:

- World Consumption Update: World Semiconductor Rebounds in 1986

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: 1986-1987 Newsletters, February 1986-1

WORLD CONSUMPTION UPDATE: WORLD SEMICONDUCTOR CONSUMPTION REBOUNDS IN 1986

WORLD OVERVIEW

In 1985, semiconductor sales were down sharply in all major regions of the world. Of the four major regions--North America, Japan, Europe, and Rest of World (ROW)--North American sales showed the strongest decline at 27.0 percent. DATAQUEST believes that the worst is behind us, however. We expect growth in the first quarter of 1986 in all world regions, including North America. This projected first quarter growth should point the industry on the way to recovery and allow it to realize world growth of 16.4 percent in 1986. We believe that 1987 will be an exceptional year in all regional markets, with the world averaging 32.6 percent growth.

JAPAN BECOMES THE LARGEST MARKET

Our regional forecast points to some startling news in market size. As shown in Table 1, the Japanese market is projected to exceed the North American market in 1986.

Table 1

REGIONAL GROWTH RATES AND MARKET SHARE
(In Percent)

	Yearly Growth			Market Share		
	1985	1986	1987	1985	1986	1987
North America	(27.0%)	10.8%	34.9%	38.8%	36.9%	37.5%
Japan	(2.8)	28.4	30.6	34.8	38.4	37.8
Europe	(3.6)	6.3	29.8	18.7	17.1	16.7
ROW	(16.6)	14.7	37.1	7.7	7.6	8.0
Total	(15.0%)	16.4%	32.6%	100.0%	100.0%	100.0%

Source: DATAQUEST
February 1986

The U.S. market is expected to pick up some share again in 1987, although it is not expected to recover its former status. Note that much of the growth that Japan realizes in 1986 is due to currency exchange. Japan gains about 19.0 percent merely from currency exchange because of a strengthening yen to dollar. Our forecast also indicates that European consumption will decline as a percentage of the total between 1985 and 1987. The European market, however, gained considerable market share in 1985 relative to its 1984 level. That market is actually leveling to a normal growth cycle. Our data also indicate that the ROW region will grow slightly to 8.0 percent in 1987.

END MARKETS KEY TO MARKET STRENGTHS AND WEAKNESSES

The severity of regional market declines in 1985 was determined largely by each region's end-market focus. The computer/data processing market was exceptionally weak and, consequently, hurt those markets focusing heavily on this area. More stable were the applications areas of consumer electronics and telecommunications.

North America/U.S. Market

With a heavy 40 percent emphasis on computers, the North American market witnessed the most severe decline of all regional markets. The U.S. market noted a sales decline of 27.0 percent. Key to the weakness of the computer market was the computer OEMs' misjudgement of actual consumption. A buying/production cycle was created at the computer level that impacted component suppliers. Inventory in 1984 was accumulated far in excess of actual needs. This inventory is now perceived to be leveling to a more normal volume, which will lead to steady booking and shipment activity. Booking and shipment levels appear to be correcting in many product areas. It is this expectation that points to a 3.9 percent North American market growth in the first quarter of 1986. DATAQUEST believes that normal inventory depletion will continue the quarterly growth pattern through 1986, for a yearly total of 10.8 percent. In 1987, we expect quarterly growth to continue. We believe that 1987 will be a year of strong growth (34.9 percent) in the U.S. market. In terms of levels of consumption, however, it is not until 1987 that we expect consumption to return to the level of 1984.

Japanese Market

The Japanese market was among the more favorable in terms of the 1985 market decline. A heavy emphasis on consumer applications was largely responsible for this stability. DATAQUEST identifies the sales decline in the Japanese market at a modest 2.8 percent in 1985. As stated earlier, we expect the Japanese market to surpass the U.S. market in dollar volume in 1986. The exchange rate is responsible for a good

portion of this increase. In yen, the Japanese market is expected to grow about 9.4 percent. Current exchange notes that the U.S. dollar is worth about 203 yen, down significantly from 1985's average of about 237 yen. Our current forecast, incorporating the yen valuation, shows the Japanese market growing 28.4 percent in 1986, far beyond the world average of 16.4 percent. In 1987, we expect Japanese market growth to be on a par with the world, at 32.6 percent.

European Market

With end-market focus primarily in the relatively stable and growing area of telecommunications, the European market was not as seriously affected as either the North American market or ROW market. The European market declined by approximately 3.6 percent in 1985. This modest decline allowed Europe to pick up market share relative to the world in 1985. It is expected, however, that this market share will revert to its normal level of about 16.6 percent (in 1984) of total sales. Note that Table 1 overstates Europe's market share because Europe gained over 2.0 percentage points in total market size in 1985. The decline in total percentage shown for years 1986 and 1987 brings Europe back to its 1984 market share of 16.6 percent.

ROW Market

The ROW region, like the Japanese market, focuses primarily on consumer-oriented products, a market that was relatively stable in 1985. Yet the ROW region also sees a large amount of activity from foreign and North American companies building computer equipment abroad. It is the balance of these factors that caused a market decline of 16.6 percent in 1985. As in other regions, we expect quarterly growth to be effective throughout 1986 and 1987. DATAQUEST projects ROW growth at 14.7 percent in 1986 and 37.3 percent in 1987.

WORLD PRODUCT TRENDS

In our quarterly world product forecast shown in Table 2, we project that MOS products will make a comeback in 1986. MOS and bipolar digital were the areas most strongly affected in 1985; both were down approximately 21 percent. The product area that noted the strongest decline, however, was MOS memory, which dropped about 36.3 percent worldwide. In this memory area, steep quarterly growth is required to pull it up from its 1985 trench. We believe that this growth is realistic and forecast that MOS memory will be up 12.0 percent in 1986. MOS microprocessor devices and MOS logic are also expected to show good growth that will continue to build momentum into 1987. Our estimated MOS technology growth in 1987 is a lofty 49.5 percent, raised through high recovery expectations for MOS memory and MOS micro devices. Bipolar

products are also projected for growth, but they are not as dramatic in percentage terms as MOS digital products. Other product areas of linear, discrete, and optoelectronics that did not decline severely in 1985 are not expected to ramp up as quickly as harder hit product areas.

(This newsletter is reprinted with the permission of DATAQUEST's Semiconductor Industry Service.)

George Burns
Barbara A. Van
Howard Z. Bogert

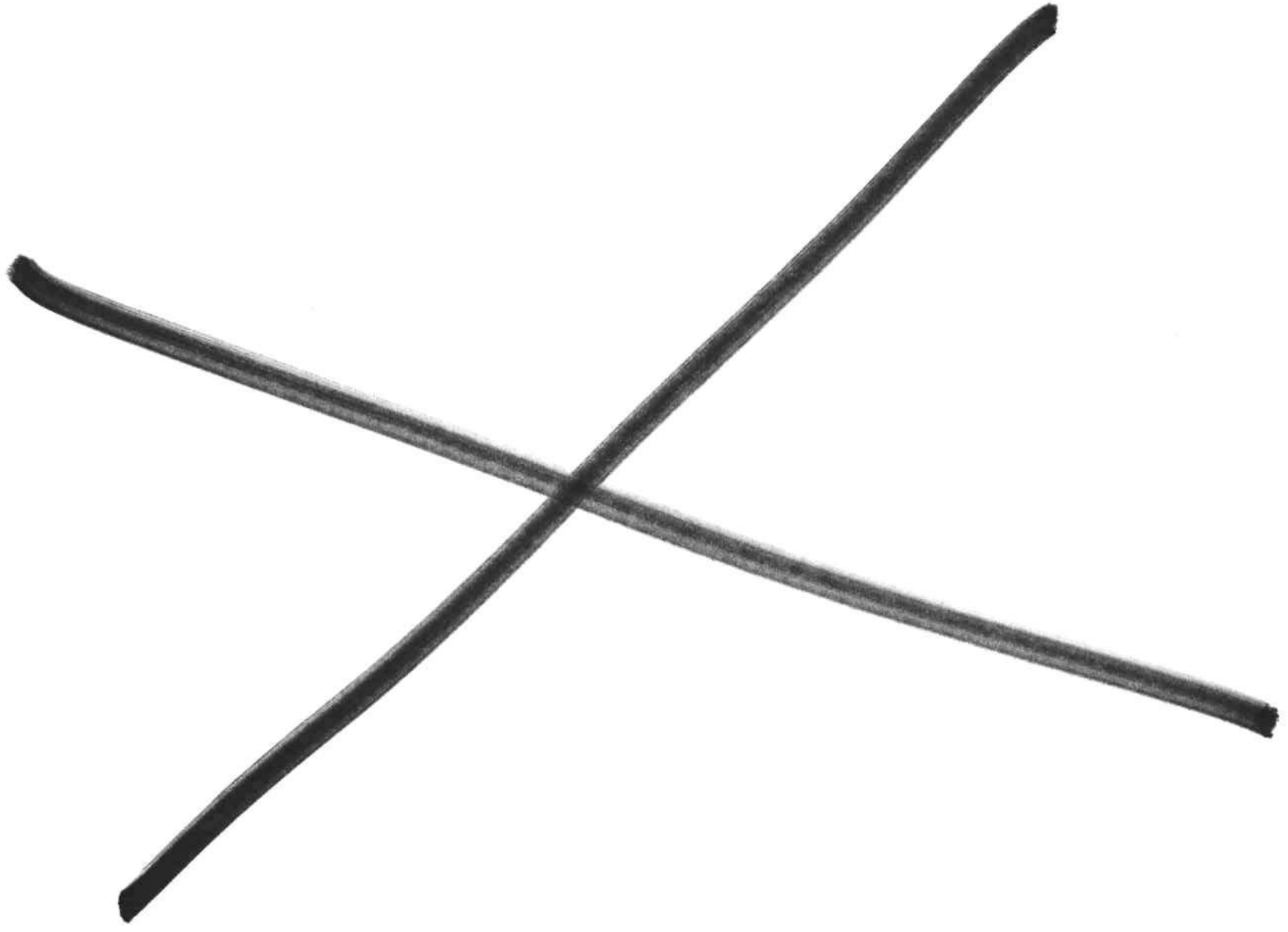
Table 2

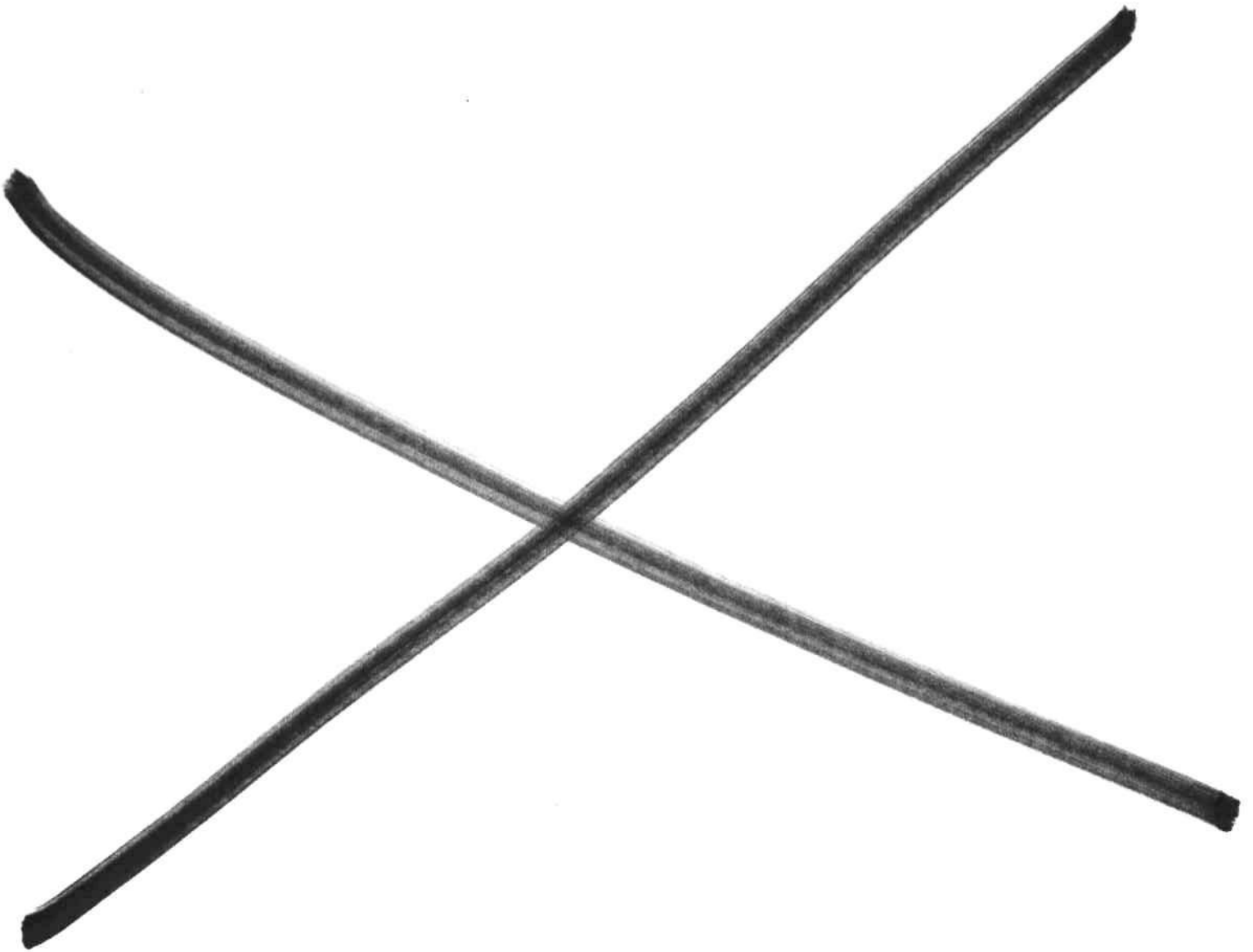
ESTIMATED WORLDWIDE QUARTERLY SEMICONDUCTOR CONSUMPTION
(Millions of Dollars)

	1985	Q1/86	Q2/86	Q3/86	Q4/86	1986	% CHG 1985-86
Total Semiconductor	24737	6354	6862	7389	8178	28783	16.4%
Total IC	18858	4751	5176	5642	6334	21903	16.1%
Bipolar Digital	3778	895	962	1053	1172	4082	8.0%
Memory	595	143	154	167	178	642	7.9%
Logic	3183	752	808	886	994	3440	8.1%
MOS Digital	10313	2551	2834	3147	3653	12185	18.2%
Memory	4008	903	1048	1186	1446	4583	14.3%
Micro Devices	2751	735	792	857	971	3355	22.0%
Logic	3554	913	994	1104	1236	4247	19.5%
Linear	4767	1305	1380	1442	1509	5636	18.2%
Discrete	4691	1258	1323	1370	1450	5401	15.1%
Optoelectronic	1189	345	363	377	394	1479	24.4%

	Q1/87	Q2/87	Q3/87	Q4/87	1987	% CHG 1986-87
Total Semiconductor	8657	9240	9827	10439	38163	32.6%
Total IC	6800	7339	7920	8439	30498	39.2%
Bipolar Digital	1233	1275	1302	1299	5109	25.2%
Memory	179	183	188	194	744	15.9%
Logic	1054	1092	1114	1105	4365	26.9%
MOS Digital	3973	4332	4746	5156	18207	49.4%
Memory	1584	1733	1928	2103	7348	60.3%
Micro Devices	1071	1192	1325	1467	5055	50.7%
Logic	1318	1407	1493	1586	5804	36.7%
Linear	1594	1732	1872	1984	7182	27.4%
Discrete	1445	1471	1468	1540	5924	9.7%
Optoelectronic	412	430	439	460	1741	17.7%

Source: DATAQUEST
February 1986





April Newsletters

The following is a list of the material found in this section:

- Semicon Europa--Cautious Optimism
- 1986 Capital Spending: Stormy Weather In Japan Send Clouds Over The Industry

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: 1986-1987 Newsletters, April
1986-2

1986 CAPITAL SPENDING: STORMY WEATHER IN JAPAN SENDS CLOUDS OVER THE INDUSTRY

SUMMARY

DATAQUEST expects that worldwide capital spending will bottom out in 1986 at $6.3 billion, down 5.4 percent from 1985's level of $6.7 billion. Fundamental changes in the Japanese market for semiconductor capital equipment are primarily responsible for this decline. Japanese capital spending for calendar year 1986 is expected to decrease by approximately 11 percent from $3.3 billion in 1985 to just under $3.0 billion in 1986 (see Table 1). North American capital spending is forecast to be basically flat in 1986, declining only 0.8 percent to $2.193 billion. European capital spending is expected to increase almost 13 percent from $381 million to $430 million. The Rest of World (ROW) region is also forecast to increase its capital spending from $242 million in 1985 to $263 million in 1986, an increase of almost 9 percent. We believe that capital spending by captives will basically reflect spending patterns in the U.S. merchant market and will be basically flat, declining slightly from $486 million in 1985 to $482 million in 1986.

JAPAN: A STORMY TRANSITION YEAR WITH FOURTH-QUARTER SUN

Skies Darker in Yen than in Dollars

The decline of the dollar relative to the yen masks the actual magnitude of the decline of the Japanese equipment market. Table 2 illustrates this point, which is explained below. It is also possible that any further appreciation of the yen could cause a decline in Japanese semiconductor revenues. Such a decline would, of course, further weaken the demand for capital goods.

In 1985, when the yen/dollar rate was 237, Japanese capital spending was ¥793 billion, down 6.3 percent from 1984. (It should be emphasized that this 6.3 percent decline is for calendar 1985.) For the fiscal year ending March 31, the decline in capital spending was more severe,

15.9 percent. In 1986, Japanese capital spending is expected to decline 23.7 percent to ¥605 billion. However, because the yen will buy more dollars in 1986, the decline expressed in dollars is only an estimated 10.9 percent, going from $3,346 million in 1985 to $2,980 million in 1986. The yen/dollar rate in 1986 is assumed to be 203 yen to the dollar.

Whether expressed in dollars or yen, there is no escaping the fact that the market for semiconductor equipment in Japan will likely be down by a large amount in 1986. The reason for this steep decline is that the industry is in a state of overcapacity, and the industry is now in a position to do something about it. Japanese semiconductor manufacturers are in this position because they now, in effect, own the markets in which they participate. They therefore no longer have to scramble to build market share.

DATAQUEST believes that this steep decline represents the beginning of a fundamental readjustment in the Japanese semiconductor industry. If the Japanese semiconductor industry had continued to spend at its historic capital spending-to-revenue ratio of 30 percent, its revenue-per-dollar value of property, plant, and equipment (PPE) would have fallen to below unity. To avoid this, we believe that the capital spending-to-revenue ratio will fall from a 30 percent level to slightly below 22 percent (see Table 3).

Japanese Company Spending

Several of the larger Japanese semiconductor manufacturers have cut back their capital spending plans for calendar 1986 by amounts greater than 30 percent. Among those that we believe have done so are Hitachi, Matsushita, Mitsubishi, and Toshiba. (See Table 4 for a list of changes in the Japanese semiconductor companies' capital spending in yen.)

Because of the appreciation of the yen relative to the dollar, some companies' capital spending expressed in dollars will increase (Rohm or Sony, for example), while expressed in yen they will decrease. (See Table 5 for the same companies' capital speding changes in dollars.)

This could be an opportunity for North American equipment manufacturers. The yen will now buy more dollars than it did a year ago. Therefore, the cost of purchasing North American equipment expressed in yen is now less for Japanese semiconductor manufacturers.

Long-Term Forecast

The long-term growth for capital spending in Japan is basically sound since it is basically a function of the growth of the Japanese semiconductor industry. DATAQUEST believes that Japanese capital spending will bottom out in the third quarter of calendar 1986, and will thereafter begin to rise at a compound annual growth rate (CAGR) of 17 percent between 1986 and 1990.

NORTH AMERICA: POSSIBILITIES OF SUNSHINE

Ambiguous Winds

There are differing signs in the wind about which way the North American industry will go in 1986. DATAQUEST has unofficially surveyed the major semiconductor companies, and the results are a disheartening decline of 18 percent from $2,227 million in 1985 to $1,827 million in 1986. In spite of these results, we are forecasting merchant capital spending to be substantially higher in 1986 than our survey indicates--at a level of $2,193 million.

The reason for our optimism is because at $1,827 million, the capital spending-to-revenue ratio is less than 13 percent. The industry has not been at this level since 1978. It is DATAQUEST's opinion, confirmed by industry sources that we contacted, that as the market for semiconductors increases, plans that were generated in the depths of 1985 will be revised upward. We are therefore adding an adjustment factor of $365 million onto our survey for our 1986 forecast, resulting in only a 0.8 percent decline (see Table 6).

North American Equipment Spending Up

A decline of 0.8 percent is still a decline. However, when one subtracts the spending for bricks and mortar, we believe that merchant capital spending for equipment will increase from $1,632 million in 1985 to $1,821 million in 1986. This is because equipment as a percent of total PPE is expected to increase from 74 percent in 1985 to 83 percent in 1986 (see Table 7).

This shift from bricks and mortar toward equipment is a continuation of a trend that DATAQUEST noted previously. (See the SEMS Research Newsletter dated October 4, 1985, entitled "Capital Spending: Japan to Continue to Outspend the United States"). The industry is continuing its shift away from areas of overcapacity and toward those technologies where future demand is expected to exceed capacity, such as devices with submicron geometry. Because of the industry's continuing need to achieve better line balance, increase utilization, and lower both contamination and breakage from handling, spending for automation should be robust. We also expect the demand for sub-2-micron equipment to be vigorous.

AFTER THE STORM: 1987 THROUGH 1990

DATAQUEST believes that semiconductor capital spending in Japan will begin to rebound in the third quarter of 1986 and will increase a robust 31 percent in 1987. We expect it to have healthy growth in 1987 even though capital spending as a percent of revenue will continue to decline. We expect this ratio to approach stability in the 21 to 22 percent range (see Table 8). Because of this fundamental readjustment of the Japanese industry, we have lowered our earlier forecast from 22 percent to 17 percent--which is still a healthy growth.

We expect North American semiconductor merchant capital spending to experience a CAGR of 25 percent from 1986 to 1990. As we have noted previously, the North American merchant semiconductor industry has been more tied to the ups and downs of business expansions and contractions than the Japanese industry has. Specifically, North American industry has matched its capacity to the business cycle. We therefore expect North American capital spending to be more in line with historical patterns than the Japanese industry.

We forecast European semiconductor capital spending to increase from $381 million in 1985 to $430 million in 1986. This reflects the continuing commitment of both European companies and their governments to re-emerge into the forefront of the industry. We expect capital spending to grow at a CAGR of 27 percent through 1990 and to break the $1 billion mark in 1990.

Rest of World capital spending was the only area that did not experience a downturn in 1985. It grew from $201 million in 1984 to $244 million in 1985. We expect ROW capital spending to reach $263 million in 1986, up 8 percent from 1985. Overall, ROW capital spending will grow at an estimated CAGR of 30 percent, the highest of any region, and reach an estimated $751 million by 1990.

George Burns

Table 1

ESTIMATED WORLDWIDE CAPITAL SPENDING
(Millions of Dollars)

	1985	1986	1987	1988	1989	1990	CAGR 1986-1990
North America	$2,211	$2,193	$3,569	$ 4,579	$ 4,528	$ 5,410	25%
Japan	3,346	2,980	3,905	4,495	4,679	5,509	17%
Europe	381	430	589	817	950	1,119	27%
ROW	242	263	394	533	593	751	30%
Captive	486	482	785	1,007	996	1,190	25%
Total	$6,667	$6,349	$9,242	$11,432	$11,746	$13,980	22%

*Columns may not total due to rounding

Source: DATAQUEST
March 1986

Table 2

ESTIMATED 1986 DECLINE IN YEN AND IN DOLLARS
(Billions of Yen, Millions of Dollars)

	Japanese Capital Spending in Yen	Percent Change in Yen	Japanese Capital Spending in Dollars	Percent Change in Dollars
1985	¥793	(6.3%)	$3,346	(7.1%)
1986	¥605	(23.7%)	$2,980	(10.9%)

Source: DATAQUEST
March 1986

Table 3

ESTIMATED JAPANESE CAPITAL SPENDING/REVENUE RATIOS
1984-1990
(Billions of Yen)

	1984	1985	1986	1987	1988	1989	1990
Revenue	¥2,733	¥2,325	¥2,355	¥3,445	¥4,119	¥4,458	¥5,177
Capital Spending	¥ 846	¥ 793	¥ 605	¥ 793	¥ 913	¥ 950	¥1,118
Spending/ Revenue	31.0%	34.1%	25.7%	25.2%	22.5%	21.3%	21.6%

Source: DATAQUEST
March 1986

Table 4

ESTIMATED CHANGES IN JAPANESE COMPANIES' CALENDAR CAPITAL SPENDING
1985-1986
(Billions of Yen)

Company	1985	1986	Percent Change
Fujitsu	¥ 72	¥ 58	(19%)
Hitachi	92	65	(30%)
Matsushita	87	58	(33%)
Mitsubishi	62	40	(35%)
NEC	123	102	(18%)
Oki	26	22	(13%)
Sanyo	47	42	(10%)
Sharp	36	32	(12%)
Fuji Electric	12	8	(33%)
Shindengen	1	1	-
Seiko Epso	8	4	(50%)
NJRC	5	6	20%
Japan Semiconductor	-	11	-
Toshiba	123	85	(31%)
Sony	36	32	(12%)
Rohm	9	8	(8%)
Sanken	6	3	(50%)
NMB	14	3	(78%)
Others	32	24	(25%)
Total	¥793	¥605	(24%)

Note: Columns may not add to totals shown due to rounding.

Source: DATAQUEST
March 1986

Table 5

ESTIMATED CHANGES IN JAPANESE COMPANIES' CALENDAR CAPITAL SPENDING
1985-1986
(Millions of Dollars)

Company	1985	1986	Percent Change
Fujitsu	$ 303	$ 287	(6%)
Hitachi	390	318	(18%)
Matsushita	368	287	(22%)
Mitsubishi	260	198	(24%)
NEC	520	500	(4%)
Oki	108	109	1%
Sanyo	199	208	5%
Sharp	152	156	3%
Fuji Electric	52	42	(20%)
Shindengen	4	5	20%
Seiko Epso	35	21	(40%)
NJRC	22	31	44%
Japan Semiconductor	-	52	-
Toshiba	520	417	(20%)
Sony	152	156	3%
Rohm	39	42	7%
Sanken	27	16	(42%)
NMB	61	16	(74%)
Others	134	119	(11%)
Total	$3,346	$2,980	(11%)

Note: Columns may not add to totals shown due to rounding.

Source: DATAQUEST
March 1986

Table 6

ESTIMATED CHANGES IN NORTH AMERICAN CAPITAL SPENDING
1985-1986
(Millions of Dollars)

Company	Capital Spending	Percent Change From 1985
AMD	$ 143	(21%)
Gould-AMI	20	(33%)
Fairchild	150	11%
Intel	180	(16%)
MMI	35	(28%)
Motorola	250	(24%)
National	145	(40%)
Others	574	(19%)
Signetics*	70	40%
Texas Instruments	260	(7%)
Subtotal	$1,827	(17%)
Adjustment Factor	$ 365	
Total	$2,193	(0.8%)

*Signetics is a subsidiary of Phillips of the Netherlands.

Source: DATAQUEST
March 1986

Table 7

ESTIMATES OF SELECTED NORTH AMERICAN COMPANIES' EQUIPMENT SPENDING
1986
(Millions of Dollars)

Company	Equipment Spending	Equipment PPE	Weighted Average
Gould-AMI	$ 18	92%	2%
Fairchild	100	87%	7%
Intel	130	72%	10%
MMI	30	85%	3%
Motorola	225	90%	22%
National	116	80%	10%
Signetics*	58	83%	5%
Texas Instruments	234	95%	23%
Subtotal	911		83%
Others	910		
Total	$1,821		

*Signetics is a subsidiary of Phillips of the Netherlands.

Source: DATAQUEST
March 1986

Table 8

ESTIMATED CAPITAL VS. REVENUE: NORTH AMERICA, JAPAN, AND EUROPE
1985-1990
(Million of Dollars)

	1985	1986	1987	1988	1989	1990
North American Revenue	$11,272	$14,209	$18,329	$22,518	$22,622	$26,584
Capital Spending	$ 2,227	$ 2,193	$ 3,569	$ 4,579	$ 5,639	$ 5,410
Capital/Revenue	20%	15%	19%	20%	20%	20%
Japanese Revenue	$10,185	$11,600	$15,494	$20,291	$21,962	$26,584
Capital Spending	$ 3,346	$ 2,980	$ 3,905	$ 4,495	$ 4,679	$ 5,509
Capital/Revenue	33%	26%	25%	22%	21%	21%
European Revenue	$ 2,301	$ 2,732	$ 3,780	$ 5,031	$ 5,398	$ 6,573
Capital Spending	$ 381	$ 430	$ 589	$ 817	$ 950	$ 1,119
Capital/Revenue	17%	16%	16%	16%	18%	17%

Source: DATAQUEST
March 1986

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: 1986-1987, Newsletters, April 1986-3

SEMICON EUROPA 1986--CAUTIOUS OPTIMISM

OVERVIEW

Semicon Europa 1986 was held at the Zuspa Convention Center in Zurich, Switzerland, from March 4 to 6. This was the twelfth time that this show, organized by the Semiconductor Equipment and Materials Institute (SEMI), had been held in Zurich.

This show, which was the first of the year in the SEMI Calendar of Events for 1986, will be followed by other shows as shown in Table 1.

Table 1

SEMICON SHOW LOCATIONS FOR 1986

Show	Location	1986 Dates
SEMICON West	San Mateo, California	May 19-22
SEMICON Osaka	Osaka, Japan	July 1-3
SEMICON East	Boston, Massachusetts	September 16-18
SEMICON Southwest	Dallas, Texas	October 14-16
SEMICON Japan	Tokyo, Japan	December TBA Technical Sessions 10-11

Source: SEMI

SHOW REVIEW

In addition to the exhibition, which allowed the equipment and materials industry that supplies European semiconductor manufacturers to demonstrate the latest technological advances, the event was supported by technical sessions under the broad title "Advanced Wafer Technology." The sessions covered wafer ecology, facility automation, and VLSI patterning. Papers of high technological content were presented by leading scientists and process engineers from Europe, Japan, and the United States.

The first session, dealing with wafer ecology, included five papers covering contamination and defect control during materials and wafer handling, together with clean room design and equipment.

The second session concentrated on facility automation and included developments in the field of factory automation, automated fabrication steps, and third-generation test systems. Aspects of an integrated front-end line were also discussed. Session three dealt with VLSI patterning and included papers on optical processing, E-Beam direct write processing, X-ray lithography processing, and plasma processing, with emphasis on the software equipment and processing aspects.

To accommodate the increased number of exhibitors, up from some 350 companies in 1985 to some 400 this year, the show filled five halls, compared with three last year. European companies were well represented in their display of the very latest in processing equipment and materials.

Table 2 lists the major European-owned companies that exhibited broken down into the principal product areas of:

- Chemicals
  - Silicon suppliers
  - Other chemicals
- Wafer process equipment
- Maskmaking
- Assembly

Table 2

EUROPEAN-OWNED SEMICONDUCTOR EQUIPMENT AND
MATERIALS COMPANIES EXHIBITING AT SEMICON/EUROPA 1986

Company	Location	Comments
Chemicals		
Silicon Suppliers		
Dynamit Nobel Silicon	Italy	Silicon Wafers
ICI Wafer Technology	United Kingdom	III-V Semiconductor Materials
Rhone Siltec	France	Silicon Wafers/Ingots
Topsil	Denmark	Float Zone Silicon NTD and HPS
Wacker-Chemitronic	West Germany	Hyper Pure Silicon Slices, Solar Grade Multicrystalline Silicon Slices
Other Chemicals		
BOC	United Kingdom	Process and Specialty Gases
Heraeus	West Germany	High Purity Materials, Aluminum Nitride Substrates
Hoechst Chemicals	West Germany	Photoresists and Related
Johnson Matthey	United Kingdom	Precious Metals for Sputtering
L'Air Liquide	France	Process and Specialty Gases, Gas Equipment
Merck	West Germany	Photoresists, High-purity Chemicals
Messer Griescheim	West Germany	Specialty Gases and Associated Equipment
Micro-Image Technology	United Kingdom	High-purity Chemicals, Clean Room Accessories
M.I.T.-Halbleiterchemie	West Germany	UV, E-B, X-Ray Photoresists, and High-purity Chemicals

(Continued)

Table 2 (Continued)

EUROPEAN-OWNED SEMICONDUCTOR EQUIPMENT AND MATERIALS COMPANIES EXHIBITING AT SEMICON/EUROPA 1986

Company	Location	Comments
Wafer Process Equipment		
Riedel-de-Haan	West Germany	High-purity Chemicals
Soprelec	France	See Micro-Image Technology
A.E.T.	France	Rapid Anneal, Dry Etch/Strip
ASM Europe	Holland	Epitaxial Reactors, Diffusion Furnaces, Driers, Purifiers, 4-Point Probe, Steppers
Balzers	Liechtenstein	Sputtering, Evaporation, Plasma Etch, Thin-film Products
BOC	England	Wet Etch Equipment, Vacuum Coaters
Cambridge Instruments	England	EB Lithograph, MOC VD
Centrotherm	West Germany	Diffusion Systems, Clean Room Technology, Quartz Tube Etching Systems
CIT Alcatel	France	Dry Etch, Vacuum Deposition
Convac	West Germany	Wafer Photolithography, Photomask Equipment, Robotic Systems
Electrotech	United Kingdom	Sputtering, PECVD, Dry Etch
ISA Riba	France	MBE, Surface Epitaxy
Kummer	Switzerland	Plasma Etch/Plasma Deposition, Ion Sources, Process Furnaces
Nordiko	United Kingdom	Reactive Ion Etch/Plasma Deposition, Sputtering
Philips	Holland	E-Beam Lithography

(Continued)

Table 2 (Continued)

EUROPEAN-OWNED SEMICONDUCTOR EQUIPMENT AND MATERIALS COMPANIES EXHIBITING AT SEMICON/EUROPA 1986

Company	Location	Comments
Phoenix Semiconductor Equipment	United Kingdom	Wet Etching/Stripping
Plasma Technology	United Kingdom	(See Krummer)
SAPI Equipments	France	Wet Benches, Cleaning Stations
Semy Engineering	France	LPCVD, PECVD, Diffusion Furnace
Suss, Karl	West Germany	Contact/Proximity Aligners
Vickers Instruments	United Kingdom	E-Beam System for Inspection and Measurement
Wellman Furnaces	United Kingdom	LPCVD Gas Systems, Furnace Loading
Wilde & Leitz	Switzerland	Stereomicroscopes, Wafer Inspection Systems
Maskmaking		
Compugraphics	Scotland	
IC Masks	United Kingdom	
Nanomask	France	E-B photomasks
Assembly		
Alphasem	Switzerland	Wafer Loaders, Die/Wire Bonder
ASM Europe	Holland	Die/Wire Bonder, Dicing, Molding Presses
Cryophysics	Switzerland	Laser Coding
ESEC	Switzerland	High-speed Die Bonders and Dicing Saws

(Continued)

Table 2 (Continued)

EUROPEAN-OWNED SEMICONDUCTOR EQUIPMENT AND
MATERIALS COMPANIES EXHIBITING AT SEMICON/EUROPA 1986

Company	Location	Comments
Farco	Switzerland	TAB, Flat-pack Bonding Machines
Slee Semiconductor-Technik	West Germany	Encapsulation
Suss, Karl	West Germany	Wafer Dicer, Prober

Source: DATAQUEST
March 1986

This table shows a good representation of European-owned companies in all the leading areas of equipment and materials supply. Some of them are highlighted below.

Chemicals

In the area of chemicals, European companies are well in the forefront. Wacker-Chemitronic is the leading supplier of silicon wafer substrates in Europe and accounts for more than 40 percent of worldwide demand for polycrystalline silicon. Exports account for about 80 percent. European suppliers of other chemicals, including gases, included Merck displaying chemicals with particle class specification for the manufacture of ICs, positive and negative photoresists, and other process chemicals. Hoechst showed its AZ positive photoresists, and its associated companies, Messer Grieshiem and Riedel-de Haen, showed gases and low-particle chemicals, respectively. Micro-Image Technology, a leading supplier in the United Kingdom, was showing high-purity chemicals and clean room accessories, together with its affiliated companies, Soprelec (France) and M.I.T.-Halbleiterchemie (West Germany). In addition to Messer Griesheim, process and special gases and related equipment were represented by BOC and L'Air Liquide.

Wafer Process Equipment

Wafer process equipment is well represented by European-owned companies. AET is now recognized as a European leader in the field of thermal management applied to semiconductor manufacture. The company exhibited its large range of rapid annealing systems, including one system working under vacuum using specialty gases that is specifically designed for III-V compounds. CIT Alcatel demonstrated the latest advances in vacuum deposition equipment, Convac wafer photolithography,

and maskmaking equipment. Electrotech exhibited its new PLASMAFAB M4 multichamber, fully automated, single-wafer etching system, which is available in plasma, reactive ion, and triode configuration. Nordiko displayed the new NS-2050 Multielectrode Sputtering System, which features continuous or indexed rotation between targets, R.R. Etch, Bias, heating to 500°C, and temperature control. Plasma Technology showed its new RIE 8000 reactive ion etch system. Karl Suss Manufacturers showed mask aligning, probing, and scribing equipment. It also displayed its new SUSS RA 120 GaAs Scriber for III-V compound materials and a new 6-inch contact/ proximity lithography tool for mix-and-match applications, designated SUSS MA 150 Production Mask Aligner. Vickers Instruments introduced its new fully automated C.D. measurement system, QUAESTER CD07A. This system features cassette-to-cassette handling of wafers up to 6 inches in diameter and is easily upgradable for the next generation of 8-inch wafers.

Maskmaking

In the area of maskmaking, Nanomask showed electron beam photomasks and its CAD tool service.

Assembly

In assembly, there were a number of European-owned companies. Cryophysics displayed laser coding of components and its CRYO-TOOR-8 Cryopump Retrofit kit. ESEC featured its new Die Bonding System Model 2005, which offers a fully automated die attacher for automated factory environments with host communication based on SECS I & II protocol. The company also showed its High-performance Dicing Saw Model 8003 and its High-speed Auto Die Bonding System for power devices--Model 2004 A-PLF.

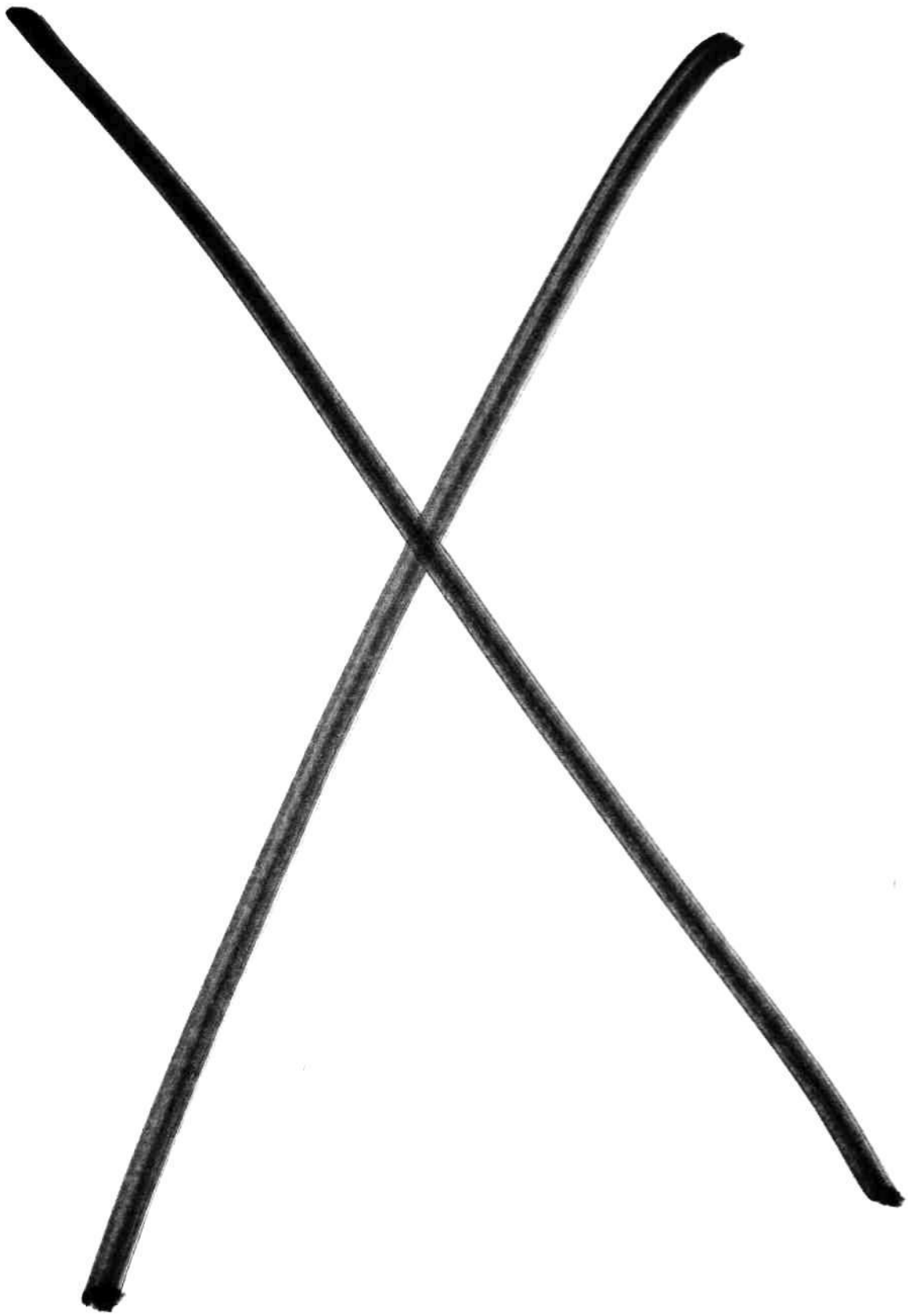
DATAQUEST SUMMARY

It is apparent that European-owned companies are at the forefront of leading-edge technology and that they are well aware of the challenge to meet the local needs of European semiconductor manufacturers. It is likely, therefore, that local competition in Europe will make the going far more difficult for American and Japanese companies trying to improve their market penetration.

Europe has weathered the recent recession in the electronics industry comparatively well, and there are now optimistic signs of recovery. DATAQUEST estimates growth in 1986 at about 6.3 percent over 1985. Indeed, DATAQUEST estimates that the semiconductor market in Europe will reach US$9,809 million by 1990; thus, the opportunities for European equipment and material suppliers abound.

Finally, a word must be said on the latest in-topic, namely, application-specific integrated circuits (ASICs), in which what previously was on the PCB has been integrated onto the silicon. As a result, densities will increase further and more VLSI computer-aided design tools will be required. Manufacturing facilities will have to adapt in order to facilitate fast turnarounds of small runs on a range of specially designed ICs. The development of this market, which holds great potential over the next 5 to 10 years but is so very different from the present memory technology requirements, will mean even closer liaison between equipment and materials suppliers and semiconductor manufacturers. To this end, the emergence of more European suppliers of equipment and materials oriented to the needs of the local semiconductor manufacturers' requirements is judged as a good omen for Europe, as it prepares for the impact that ASICs will have in the market.

Robert McGeary
Jim Beveridge



May Newsletters

The following is a list of the material found in this section:

- Silicon: Fuel For The Semiconductor Industry
- Activity In The Fabs: GaAs Abuilding; Shutdowns And New Lines in Silicon
- SECS In The Semiconductor Industry

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: 1986-1987 Newsletters, May
1986-6

SILICON: FUEL FOR THE SEMICONDUCTOR ENGINE

INTRODUCTION

When Walter Brattain, John Bardeen, and William Shockley developed the first transistors in 1947 and 1948, the technology requirements that would lead to the preeminence of silicon as a volume semiconductor material were not yet understood. Germanium, the semiconductor material first used, was naturally occurring and easily worked, but it had two distinct shortcomings. The first problem was thermal. Because of its narrow band gap (0.66 eV versus 1.1 eV for Si), the operating temperature range of Ge devices is limited. The second problem was that early germanium oxides could not be thermally grown, and were volatile at diffusion temperatures. And, moreover, they were not good diffusion barriers. In contrast, thermally grown silicon dioxide was easily processed and was an effective diffusion barrier. After development of the silicon planar process at Fairchild Semiconductor in 1958, the use of germanium declined rapidly except for special devices and detectors.

Actually, the early utilization of semiconductor silicon would have been accelerated even more were it not for the scarcity of high-quality material. During the late 1950s, silicon capacity could not keep up with demand. In 1963, General Electric developed the plastic-encased silicon transistor, and the silicon device market finally outpaced the germanium device market. Silicon capacity was growing.

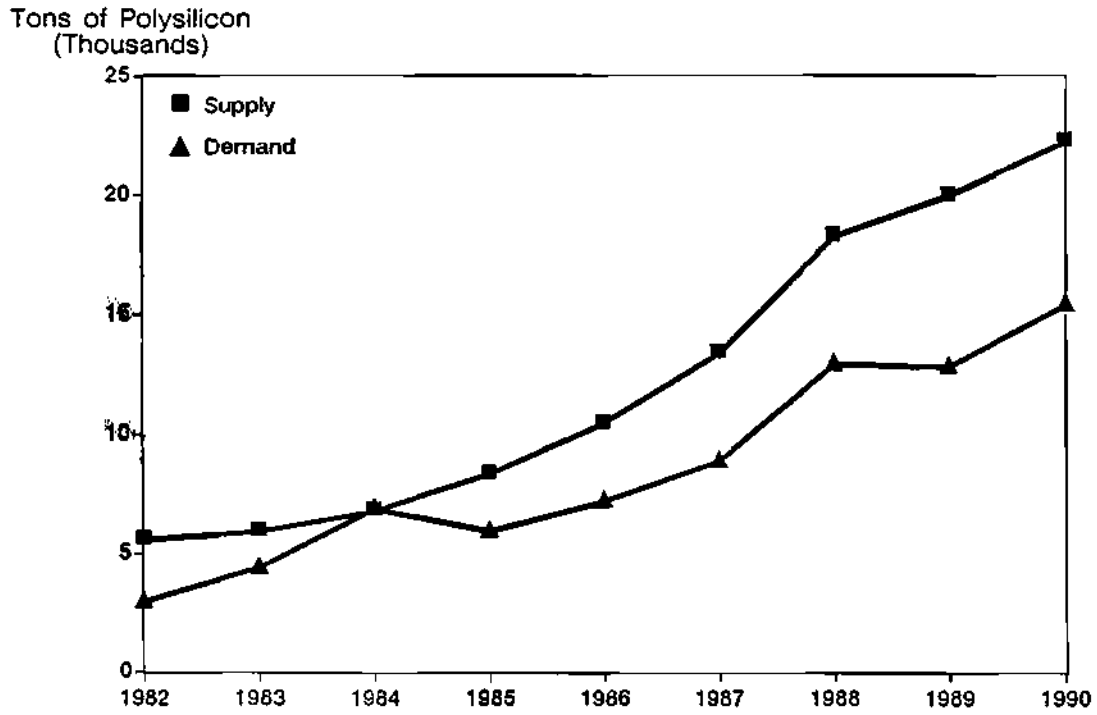
In 1960, Dow Corning was the leading supplier of polysilicon. Today, that distinction belongs to Wacker Chemitronic, which has double the capacity of its nearest competitor. Recently, however, several companies, including some major Japanese firms, have committed to becoming major suppliers of polysilicon or single-crystal silicon.

THE POLYSILICON MARKET

The contemporary polysilicon market situation is as follows. In 1984, the polysilicon market was at the $300 million level while the merchant single-crystal silicon market was valued at $1,371 million. Polysilicon capacity was 6,870 metric tons but increased to 8,425 metric tons by 1985. We believe that the recent U.S. and Japanese entries to the field will cause polysilicon production capacity to grow at a 21.5 percent compound annual growth rate (CAGR) through 1990. Figure 1 shows data and projections for polysilicon supply and demand from 1982 through 1990.

Figure 1

ESTIMATED WORLDWIDE POLYSILICON CAPACITY
1982-1990



Source: DATAQUEST
May 1986

The free world consumed nearly all the polysilicon that it produced in 1984. In 1985, as the recession took its toll--decreasing merchant wafer revenue by nearly 50 percent--wafer manufacturers continued to add to their inventories of polysilicon. Thus there is an oversupply of this material. With new companies entering the market and process productivity increasing, we expect this oversupply to continue through the end of the decade.

Silicon Process Productivity

Figure 2 shows U.S. and Japanese silicon process productivity measured in terms of revenue per square inch of silicon since 1980. During the later 1970s, U.S. device manufacturers realized that their Japanese competitors were achieving better yields at die sort. This realization caused a general increase in U.S. process productivity. There also has been an increasing movement into application-specific integrated circuits (ASICs), which yield higher than average financial return on each processed wafer. We believe that ASICs will register a 35 percent CAGR through 1990 and that per-wafer revenue will continue its upward trend.

It can be argued that Japan has pursued a strategy designed to capture industry-wide market share. From 1979 to 1985, Japanese manufacturers increased their installed base of capital equipment by 8.6 times. Figure 2 shows the effects of the Japanese companies' aggressive move into commodity MOS devices with low average selling prices. As these low-end markets fall to the Japanese market share strategy, we expect to see a marked decrease in the growth rate of Japanese capital spending and a firming of average selling price for commodity products. Japanese revenue per square inch will increase from an average of about $18 in 1985 to $23 in 1990.

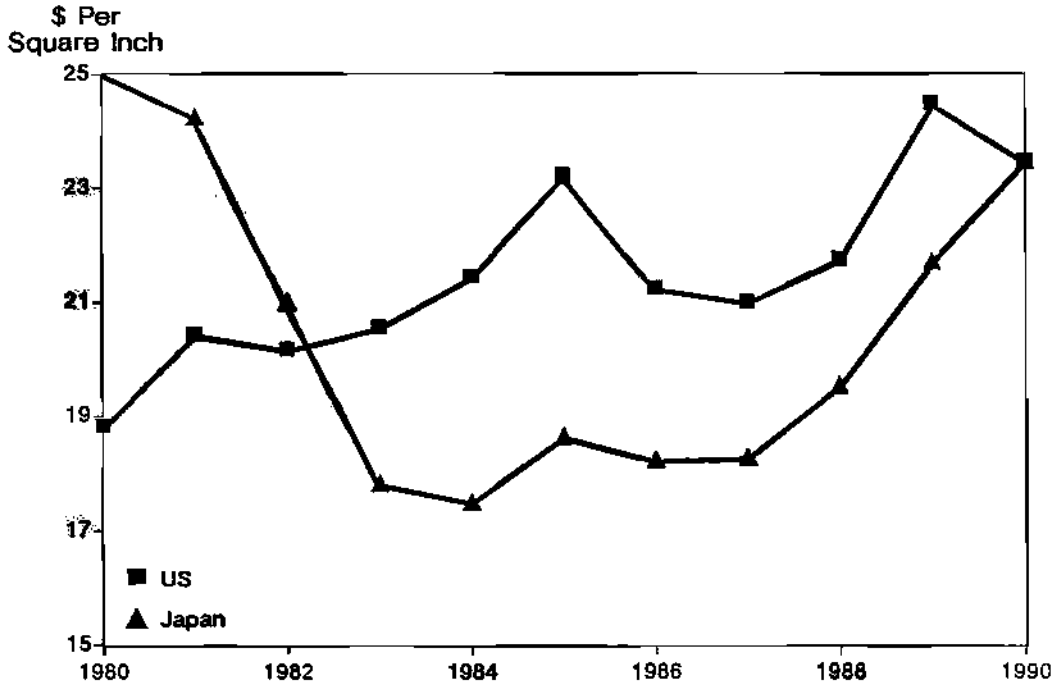
ASIC Production

The Japanese manufacturers are actively pursuing the ASIC market. They have already gained a significant share of the world market through sales to their home market. Fujitsu, for example, is the leading supplier of bipolar gate arrays and is second in MOS gate arrays. European companies are also aggressively pursuing the market for these custom-made, quick-turnaround devices, and are expected to maintain a dominant share of the West European ASIC market.

In current ASIC production, small lot cost-effectiveness is achieved through the use of direct-write electron beam (e-beam) systems. E-beam systems decrease turnaround time by eliminating the delay associated with delivery of the mask sets. It is interesting to note that of 198 direct-write electron beam systems installed worldwide, 26 percent were produced by U.S. companies (mostly IBM), 28 percent by European companies, and 41 percent by Japanese companies. Clearly, Europe and Japan have ASIC-adaptable direct-write technologies of their own. Because of this widespread ASIC capability, silicon process productivity will generally increase throughout this decade, causing silicon markets to grow more slowly than device markets.

Figure 2

ESTIMATED SILICON WAFER PROCESS PRODUCTIVITY
(United States versus Japan)



Source: DATAQUEST
May 1986

Merchant Silicon Market

Of the nearly 1.7 billion square inches of silicon consumed worldwide in 1984, the United States, with its large captive semiconductor community, used 817 million square inches (msi), while Japan and Europe consumed 661 msi and 153 msi, respectively. Only 74 percent of U.S. consumption came from merchant silicon suppliers. Worldwide merchant silicon revenue was $1,371 million. The 1985 figures for U.S., Japanese, and European consumption were 633 msi, 550 msi, and 138 msi, respectively, down 18.3 percent overall. The U.S., Japanese, and European silicon merchant market was 458 msi, 550 msi, and 138 msi, respectively, with a corresponding dollar value of $1.1 billion. At present, silicon sales are at about 50 percent of capacity.

Merchant silicon suppliers were hit extremely hard by the 1985 recession. Many companies had geared up for a boom market, believing that the 40 percent and 45 percent growth of 1983 and 1984, respectively, was going to continue. Instead, the bottom fell out, leaving many companies with much more excess capacity than they had going into 1983. Japanese manufacturers, which support their suppliers by maintaining a very high equipment utilization, watched their utilization fall from 95 percent in 1984 to 69 percent in 1985. In Western Europe, however, markets fell only 10 percent because of the relative strength of the European semiconductor business.

We expect merchant suppliers of single-crystal silicon to increase their output by 20 percent in 1986. This will still be short of the amount they shipped in 1984, however. Growth will continue through 1987 (up 35 percent again) and on into 1990. We believe that the 1985 to 1990 CAGR will be 16.8 percent. This, however, is below the 18.4 percent CAGR anticipated for semiconductor device production (silicon based) for the same period.

DATAQUEST ANALYSIS

Although silicon consumption in square inches will grow at a slower rate than semiconductor productivity, silicon manufacturing revenue will grow more rapidly, due to three factors. First, the move to larger wafer sizes is associated with a higher average selling price per square inch. Second, as the technology becomes more demanding, silicon manufacturers will be able to realize at least the same percentage of the device manufacturers' revenue dollar as they have been able to obtain historically. This too will lead to ASP increases, allowing merchant silicon revenue to keep pace with device revenue. The third factor will be the transfer of value-added from the device manufacturer to the silicon manufacturer. By supplying wafers with a high-quality epitaxial layer for the growing CMOS market, silicon vendors will be able to realize a profit from the critical epitaxial processing step. These factors will allow the silicon market to increase at a higher rate than the 18.4 percent CAGR of the semiconductor device market.

Robert McGeary

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: 1986-1987 Newsletters, May 1986-5

ACTIVITY IN THE FABS: GaAs ABUILDING; SHUTDOWNS AND NEW LINES IN SILICON

SUMMARY

This newsletter describes some of the activity centered around semiconductor fab facilities--both new construction and closings.

DATAQUEST expects that total spending in 1986 for North American semiconductor facilities will be approximately $428 million. This is down from the approximately $790 million spent for facilities in 1985. The reason for this decline is that capital spending for semiconductor facilities will absorb a smaller percentage--16 percent in 1986 compared to 26 percent in 1985--of semiconductor capital spending (See the April 1986 SEMS Newsletter entitled "1986 Capital Spending: Stormy Weather in Japan Sends Clouds Over the Industry.") However, there is still a significant amount of activity that DATAQUEST has noted recently.

The following paragraphs detail some of this recent activity.

GALLIUM ARSENIDE

Anadigics

Anadigics has begun pilot production in Morristown, New Jersey, and the company expects to be capable of full production by the third quarter of this year. The facility, which currently employs 35 people, contains an 8,000-square-foot class 100 clean room and will run 3-inch wafers at 0.5-micron line geometries. Most of the products produced will be linear ASICs.

Avantek

Avantek is constructing a 90,000-square-foot gallium arsenide facility on nine acres in Newark, California.

Gain Electronics

Gain Electronics (formerly Pivot III-V) in Branchberg, New Jersey, is expecting to complete a new 60,000-square-foot facility featuring a 6,600-square-foot class 10 clean room in the third quarter of 1986. The company expects to be in pilot production by the end of this year and in full production by the second quarter of 1987. This new facility will have a capacity of 800 wafer starts per month/shift and will be running 3-inch wafers at geometries as low as 0.25 microns. The facility currently employs 20 people, expects to employ 50 by December, and ultimately plans to employ a total of 150. It is being equipped with direct write E-beam and direct step wafer equipment; it will also be used as a beta test site for a new molecular beam epitaxy machine. Products will include GaAs HEMT ASICs.

Hewlett-Packard

Hewlett-Packard plans to update its discrete optoelectric division in San Jose, California, to run 3-inch GaAs wafers by mid-1987. Reportedly, the company is also considering automating this new line. The facility currently contains a 25,000-square-foot class 100 clean room that is operating at 5-micron line geometries.

Hughes Aircraft

Hughes Aircraft in Torrance, California, plans to complete its new gallium arsenide wafer fab by the fourth quarter of 1986. This fab, which will be contained in an existing Hughes building, is expected to have a minimum capacity of 500 wafer starts per month/shift and be fully operational by the middle of 1987. It will run 3-inch or 4-inch wafers, with line geometries as low as 0.5 microns. All front-end equipment will be fully automated. The 66,000-square-foot facility will house approximately 12,000 square feet of class 100 clean room. The facility will be producing monolithic microwave integrated circuits. In addition to the fab line, there will be an on-site circuit design school where engineers will be able to design their own circuits.

Hughes also plans to build another GaAs facility in Malibu, California, which is scheduled to be completed by the first quarter of 1988.

Microwave Semiconductor

Microwave Semiconductor's 90,000-square-foot facility in Somerset, New Jersey, is due to be completed by the fourth quarter of this year. The facility will produce monolithic microwave ICs and will feature a class 10 clean room. Microwave Semiconductor, a subsidiary of Siemens Components, plans to invest $45 million over the next three years to develop submicron extremely high speed ICs.

Rockwell

Rockwell International at Newbury Park, California, has begun producing 1K and 4K RAMS and process evaluation chips during its current pilot stage, which will lead to eventual production of 16K RAMs and 6K gate arrays. The facility will have a capacity of 2,000 starts per month, based on the planned two-shift production schedule that it should be capable of by early 1987. It will run 3-inch wafers with 1-micron line geometries in a 4,500-square-foot class 10 clean room. This clean room is expandable to 5,500 square feet. The $19 million, 41,000-square-foot facility employs 52 people. This facility will also serve as a foundry for Department of Defense contractors to obtain GaAs devices fabricated to their own designs.

SILICON FABS--OUT WITH THE OLD AND IN WITH THE NEW

As the industry begins to pick itself up from the 1985 slump, old fabs are being closed or refurbished or sold--and some new fabs are being built.

Adolph Coors and Siemens Components

Siemens Components has sold two of its lines in Broomfield, Colorado, to Adolph Coors for approximately $10 million. The 115,000-square-foot facility will include rectifier and diode lines. The diode line has a 2,000-square-foot class 1,000 clean room and runs 4-inch wafers with 5-micron line geometries; it has a start capacity of 3,000 wafers per month. The rectifier line has a 5,000-square-foot class 10,000 clean room and runs 3-inch wafers. Together, both lines employ 20 operators.

Not included in the deal is the Siemens power transistor line, which has a 2,350-square-foot class 100 clean room and a start capacity of 1,700 wafers/month for two shifts.

Advanced Micro Devices

Advanced Micro Devices (AMD) is closing two of its fabs in Sunnyvale, California. Fab 8, a 4-inch bipolar R&D line, is being closed for an upgrade and is scheduled to be reopened "when business conditions

improve." Fab 4 will be closed permanently. Most production from these facilities will be shifted to Austin and San Antonio, Texas. However, some of Fab 4's production will be shifted to Fab 2 in Sunnyvale.

Two AMD lines, Fab 5 and Fab 10, in Austin, Texas, are being shut down for revamping. Fab 5 is a 4-inch MOS line, and Fab 10 is a 5-inch NMOS line. Both of these lines will be upgraded to 6-inch CMOS. These lines will each feature 1.5-micron geometries and have 20,000 square feet of class 10 clean room.

RCA/Sharp

RCA/Sharp has suspended construction at its Camas, Washington, facility. This three- to four-month suspension will allow time for evaluation of the effects of RCA's acquisition by General Electric.

NEW FABS ABUILDING

AT&T

AT&T's new fab in Orlando, Florida, is reportedly in a preproduction mode of operation. The facility, which will produce 1MB DRAMs, is said to be capable of running 5-inch wafers with 1.25-micron line geometries. This is reportedly a highly automated fab and is claimed to have the largest start capacity of any wafer fab in the world.

Cypress Semiconductor

Cypress Semiconductor will complete a new fab in the third quarter of 1986 in Austin, Texas. It has reportedly placed an order for $10 million worth of GCA steppers.

General Electric

General Electric (GE) may have a 1.25-micron pilot line at Research Triangle Park, North Carolina, that could begin production in 1987. GE is currently running 2-micron CMOS at Research Triangle Park.

International Rectifier

International Rectifier in Rancho Seco, California, should be in pilot production by the end of the second quarter of 1986. Full production capability is planned for early 1987. Inside the 285,000-square-foot facility will be a 12,800-square-foot class 10 clean room that will produce MOS power transistors on 5-inch wafers with 5-micron line geometries. The facility will employ 700 people and will operate 3 shifts with a total of 60 front-end operators.

VLSI Technology

VLSI Technology has purchased 100 acres of property in San Antonio, Texas, as the home of a future 6-inch fab.

Xicor

Xicor has just completed a new fab building equipped with acid tanks and water systems in the Milpitas, California, area. The building is not being equipped at present because Xicor does not yet need the capacity and also because Xicor reportedly believes that there will be a major evaluation of production equipment within the next two years.

CONCLUSIONS

Even at the end of a very long and difficult downturn, new processes and technologies continue to be developed. Much of this new activity is for gallium arsenide. We expect that, as gallium arsenide moves from an R&D mode to preproduction, significant opportunities will develop for manufacturers of submicron equipment such as direct write E-beams and molecular beam epitaxial equipment. We also note that there is new fab activity for advanced products. AT&T's 1MB DRAM facility in Orlando, Florida, is an example of this.

These new facilities will not only provide opportunity for manufacturers of sub-2-micron equipment. The majority of these new facilities are designed to provide a class 10 environment. We, therefore, expect to see significant opportunities for those manufacturers who can help provide, maintain, and measure a class 10 environment.

Downturns are times to economize, to retire facilities, and to upgrade facilities. However, as this newsletter demonstrates, there is significant activity in building new fabs. And we believe that this activity will increase.

George Burns
Mark Reagan

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: 1986-1987 Newsletters: May 1986-4

SECS AND THE SEMICONDUCTOR INDUSTRY

SUMMARY

There is a lot of discussion about the SECS protocol in the semiconductor industry as major manufacturers adopt a strategy for automation of fabrication facilities in the 1980s. The SEMI Equipment Communications Standard (SECS) communications protocol is designed to provide communication capabilities between semiconductor processing equipment and an upstream node or host computer. SECS was proposed and developed by SEMI (the Semiconductor Equipment and Materials Institute) in the early 1980s in response to the need for a communications protocol that specifically focused on manufacturing in the semiconductor environment. DATAQUEST recently completed a survey of major semiconductor equipment manufacturers in order to evaluate the level of vendor commitment to the SECS protocol. Survey results reveal that:

- Thirty-nine of 42 equipment models surveyed have existing SECS capability or have implementation currently under development.
- A great deal of variety exists in the interpretation and number of messages from the SECS protocol that vendors have chosen to specify for their equipment.
- Not one of 27 equipment models for which SECS message set information was provided can meet the minimum requirements for SECS specifications from both Intel and Texas Instruments.

DATAQUEST believes that equipment manufacturers that can satisfy the needs of IC manufacturers in the automation arena will gain a strategic market advantage in providing equipment to the semiconductor industry. Equipment manufacturers have an important opportunity to participate in the formative stages of automation in the industry and, in the process, establish firm relationships with the automation leaders in semiconductor manufacturing.

This newsletter presents highlights from an upcoming Semiconductor Equipment and Materials Service (SEMS) service section entitled "Equipment Communications." DATAQUEST believes that this topic is of significant importance to our clients as the industry prepares for factory automation in the 1980s.

DATAQUEST EQUIPMENT SURVEY

Overview

Twenty-six equipment manufacturers representing eight general types of front-end processing equipment participated in the DATAQUEST study in which a total of 42 models of equipment were discussed. The eight categories of front-end equipment include chemical vapor deposition (CVD) reactors, diffusion furnaces (including annealers), epitaxial reactors, ion implanters, lithography, sputtering, dry etch, and automatic photoresist processing (track) equipment. The 26 survey participants combined represented 50 percent overall market share of the 1984 worldwide semiconductor front-end processing equipment market. The combined market share of survey participants in each equipment category is presented in Table 1.

Table 1

SURVEY PARTICIPANTS' 1984 WORLDWIDE MARKET SHARE, BY EQUIPMENT CATEGORY

Equipment Category	Participants' Sum Market Share
CVD	14%
Diffusion/Anneal	55%
Dry Etch	62%
Epitaxy	58%
Ion Implantation	79%
Lithography	75%
Sputtering	54%
Track	61%

Source: DATAQUEST
May 1986

The equipment manufacturers that participated in the study are identified in Table 2. The number beneath each equipment category indicates the number of equipment models that were discussed in the survey. In some instances, several models of equipment from the same vendor have been included. Vendor responses were for existing equipment models that are considered to be the most advanced, as well as for next-generation equipment currently under development.

Table 2

EQUIPMENT SURVEY PARTICIPANTS

	CVD	Diffusion/ Anneal	Dry Etch	Epitaxy	Ion Implant	Lithography	Sputtering	Track
Models of Equipment	4	6	9	3	3	6	4	7
Companies								
Advanced Crystal Sciences, Inc.		X						
ASM America		X						
Anicon Incorporated	X							
Applied Materials, Inc.			X	X	X			
BTU Engineering Corporation		X						
Drytek Inc.			X					
Eaton Corporation					X	X		X
GCA Corporation			X			X		X
Gemini Research				X				
Genus Incorporated	X							
Lam Research Corporation			X					
Machine Technology, Inc.								X
Materials Research Corporation			X				X	
Nikon Precision, Inc.						X		
Perkin-Elmer			X			X	X	
Semiconductor Systems, Incorporated								X
Silicon Valley Group, Inc.	X							X
Solitec, Inc.								X
Tegal Corporation			X					
Temescal							X	
Thermco Systems, Inc.		X						
Tylan Corporation		X						
Ultratech Stepper						X		
Varian Associates	X	X			X		X	
Veeco Instruments Inc.								X
Zylin Corporation			X					

Note: In some cases, more than one model of equipment from the same vendor has been included in a given equipment category.

Source: DATAQUEST
April 1986

Survey Results

Of the 42 equipment models that were surveyed, 39 models have SECS capability. Of those 39 equipment models, 28 models already have an existing SECS protocol implementation, while 11 models have their SECS implementation currently under development such that a software release will be available in 1986.

No Two People Do SECS Protocol the Same Way

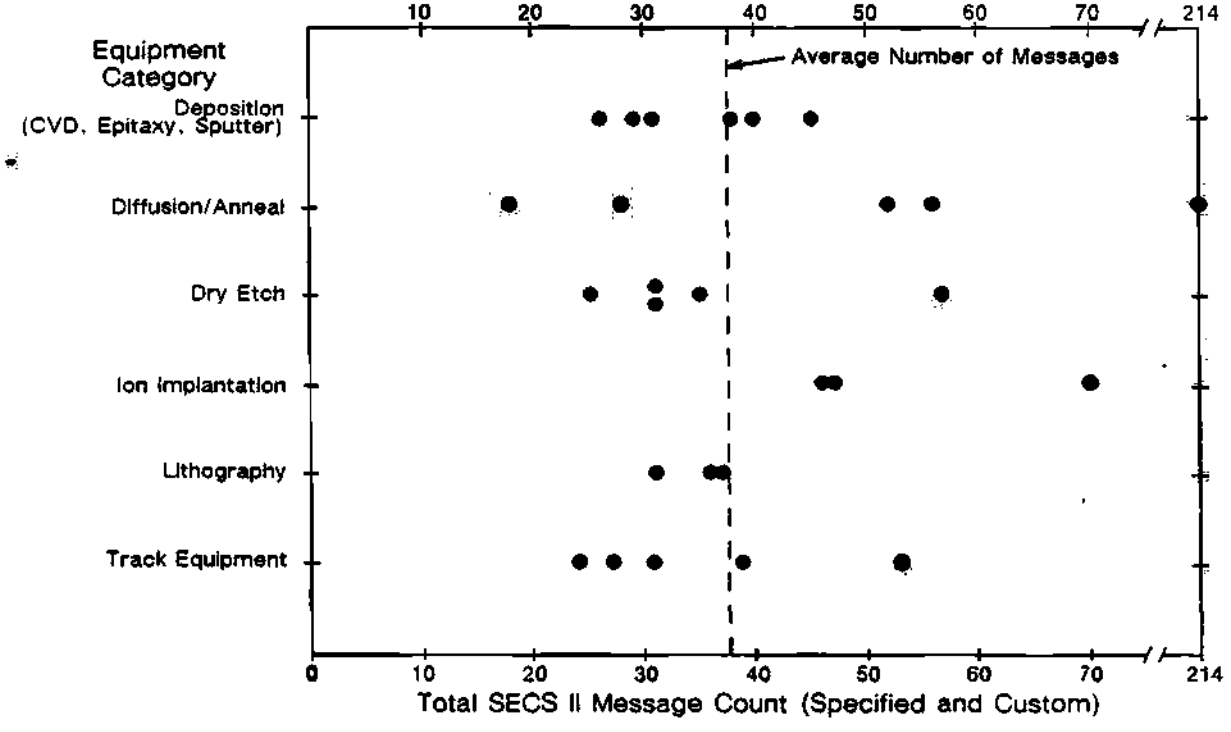
One part of the SECS protocol, known as SECS II, specifies a general message set for transactions between processing equipment and an upstream node or host computer system in an automated semiconductor fabrication environment. The SECS II protocol classifies the different types of messages into 11 streams, or general message subjects. Within each

stream, there are a number of function codes that identify the associated subtopics of each stream. Equipment manufacturers choose the messages from the SECS II message set that they feel are applicable for their equipment. The SECS II protocol also provides the option of implementing custom messages for equipment-specific applications. In order to quantify the level of vendor implementation of the SECS protocol, equipment manufacturers were requested to provide specific information from their SECS II message set, particularly the total number of SECS II messages.

DATAQUEST analyzed SECS II message detail for 27 models of front-end processing equipment. Each point in Figure 1 represents the total number of SECS II messages (both specified and custom) that have been implemented for a particular model of equipment. For example, the three models of lithography equipment have message sets consisting of 31, 36, and 37 messages, respectively. Not only is there a wide range in the number of messages between the various categories (18 to 214), but also within a given equipment category. The average number of total messages implemented by equipment vendors in Figure 1 is 38 (excluding the one diffusion entry of 214 messages). (Sputtering equipment, epitaxial, and CVD reactors have been classified in a general deposition equipment category in this figure to maintain equipment vendor anonymity.)

Figure 1

TOTAL SECS II MESSAGE COUNT (SPECIFIED AND CUSTOM), BY EQUIPMENT CATEGORY



Source: DATAQUEST
May 1986

The absolute number of messages implemented by a given equipment manufacturer does not necessarily reflect the level of protocol software sophistication for the equipment. It is possible that some equipment manufacturers have chosen to implement a very efficient, compact message set, while others have included a large number of special function custom messages to enhance their protocol's capabilities.

What is most important is not the absolute number of messages that have been chosen but rather that the implemented message set includes all of the necessary functional components of the protocol such as recipe management (uploading and downloading), process and equipment status, and alarm information. Two factors--specific message code implementation and functionality of the message set--could well be represented by a unique set of stream/function codes, which, if detailed in the exact same manner by all equipment manufacturers, would ensure a standardized implementation across the board for all types of equipment. However, in reality, vendor interpretation and implementation of the SECS II messages can vary considerably, and yet still meet the necessary requirements for functionality of the message set.

SEMICONDUCTOR MANUFACTURERS' SPECIFICATIONS FOR SECS

A majority of semiconductor manufacturers now require SECS compatibility for new equipment purchases. However, many offer little else for guidance. Equipment vendors have commented that most manufacturers do not seem to know what they want with regard to automation or in the specifications of a SECS II message set. Many equipment vendors thus are faced with the prospect of developing a SECS protocol that will require special customization when the equipment is finally installed in an automated environment at a given semiconductor manufacturer's facility. In addition, the customization is likely to be different for each semiconductor manufacturer.

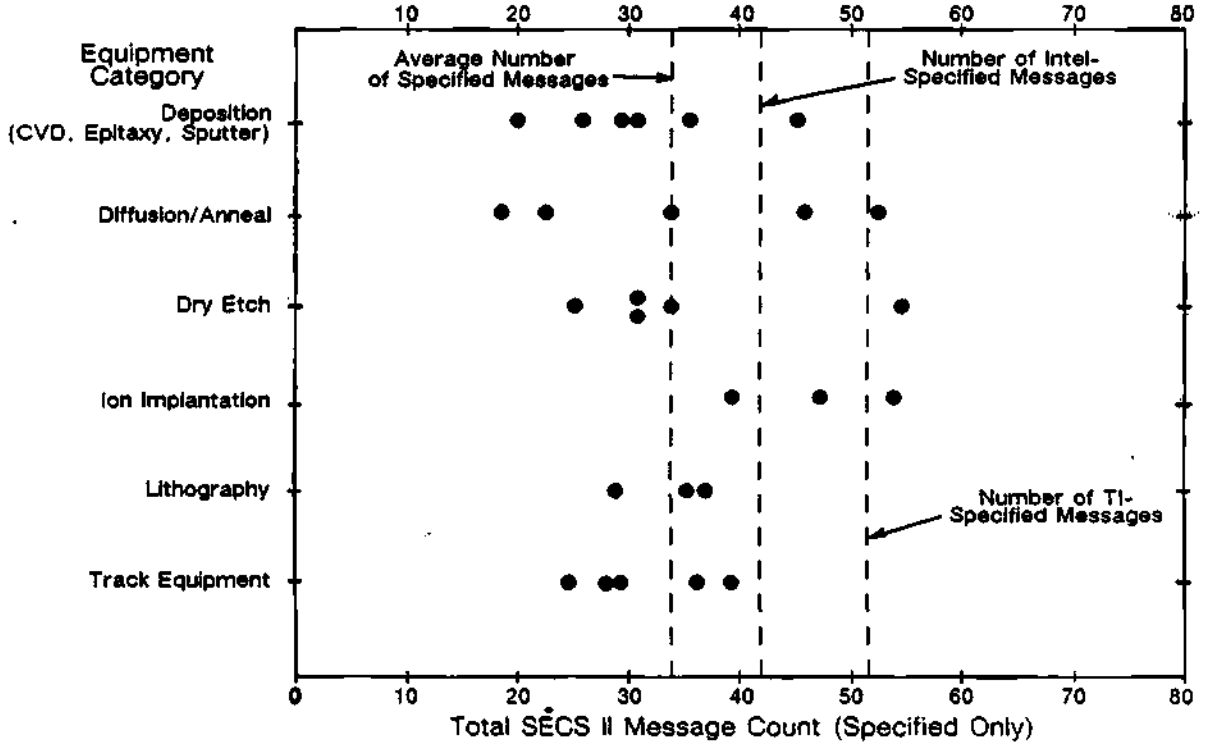
Some semiconductor manufacturers, such as Intel, Texas Instruments (TI), and Thomson Components-Mostek Corporation (TCMC), have taken the first step in equipment-level automation and have provided equipment manufacturers with minimum SECS II message set requirements. These manufacturers feel that their minimum message sets include the essential functionality of the SECS II protocol. In addition, they are attempting to ensure standardization throughout their own facilities by providing clear guidelines to the equipment industry. Other semiconductor manufacturers have chosen to specify the broad functional components of the protocol that they consider necessary for equipment/host communication in an automated facility. The details of the protocol implementation are left to their equipment vendors.

Figure 2 compares the number of protocol-specified messages implemented by equipment manufacturers with the number of messages specified by Intel and Texas Instruments in their minimum SECS message sets. The information in Figure 2 is essentially the same as that in Figure 1, except that custom messages have been removed from the total message count for 14 of the 27 equipment models that include these

equipment-manufacturer-defined functions. On the basis of specified message count, the average number of messages implemented for the 27 equipment models is 34.

Figure 2

TOTAL SECS II MESSAGE COUNT (SPECIFIED ONLY), BY EQUIPMENT CATEGORY



Source: Intel Corporation
Texas Instruments, Inc.
DATAQUEST
May 1986

Intel's SECS II specification identifies 42 messages as the minimum set necessary for implementation on process and analytical equipment. In the case of Texas Instruments, 51 messages have been specified. Only 6 equipment models of the 27 represented in Figure 2 can meet Intel specifications and only 3 of 27 models can meet the TI requirements based on specified message count alone. In addition, only 14 of the 27 survey participants that provided detailed information on their SECS II message sets included any abort messages in their protocol implementation. Both Intel and Texas Instruments require that abort messages be implemented in every general message category (stream) in which messages have been specified.

If an equipment manufacturer chose to comply with the number of messages that would satisfy both Intel and TI specifications (based on the overlap of the message sets of TI and Intel), a total of 73 specified messages from the SECS II protocol would be required. Not a single equipment model of the 27 that provided detailed protocol information in the DATAQUEST survey can meet both Intel and TI's minimum message set specifications on the basis of message count alone. DATAQUEST believes that this is an extremely important finding to come out of this survey.

Intel and Texas Instruments recognize that minimum SECS II requirements from semiconductor manufacturers should be focused on specific categories of equipment rather than on a general message set for all wafer processing equipment. Both manufacturers are willing to negotiate their minimum message set requirements with equipment vendors since, in some cases, the messages may not be appropriate for a given type of equipment. However, these semiconductor manufacturers will not negotiate when an equipment vendor has chosen to implement his own custom messages when existing messages in the protocol would have sufficed. The generic minimum message sets from Intel and TI are meant as guidelines for equipment protocol development to ensure that equipment purchased for Intel and TI facilities has sufficient communications capability to operate in an automated environment. Clearly, if Intel's and Texas Instruments' message sets are indicative of the minimum requirements for general SECS II implementation in the industry, the majority of equipment vendors face major customization of their SECS protocol at some stage when a semiconductor manufacturer decides to automate his facilities.

ADDITIONAL SPECIFICATIONS

Up to this point, discussion in this newsletter has centered only on the total number of function codes that have been specified. For a more accurate comparison of protocol specifications between equipment and semiconductor manufacturers, the actual function code numbers in each stream used to identify the messages must be compared. An equipment manufacturer that has 42 messages in his SECS II protocol implementation may not have specified the same 42 messages that Intel has identified in its requirements. Even if an equipment manufacturer has implemented the stream/function codes required by Intel, this protocol specification may still not satisfy another semiconductor manufacturer since even between semiconductor manufacturers, the overlap in the actual stream/function codes may be small. A comparison of Intel's set of 42 messages and Texas Instruments' set of 51 has an overlap of only 20 of the same stream/function code numbers. Total message count is really only the first step in meeting semiconductor manufacturers' protocol needs, and must be followed up with a comparison of actual stream/function codes.

In addition, the data structure of each message must also be specified. The data structure includes the data element name and the format and length of the data. The SECS II protocol does provide data element names, but data format, of which there are 14 options in the protocol, and data length are variable. Therefore, even if semiconductor

and equipment manufacturers specify the identical stream/function codes, it is still possible that the message sets are not entirely compatible due to differences in the data format and length. Equipment and semiconductor manufacturers must come to a common consensus for data structure as well as protocol specifications in order to achieve some level of standardization in equipment communication throughout the industry.

DATAQUEST believes that semiconductor manufacturers involved in the automation effort need to take the first step and establish a clear consensus on what they feel is necessary for SECS protocol implementation by equipment manufacturers. It has been suggested that a SECS Users Group for IC manufacturers be organized as a forum for identifying protocol and automation needs from a manufacturing perspective. Equipment manufacturers would participate in the SECS Users Group and provide their current protocol documentation as an aid in evaluating the status of protocol implementation. Some equipment manufacturers, however, regard their protocol implementation as confidential information. Semiconductor processing equipment should not be competing on the basis of protocol implementation but rather on equipment design and special features. The time and cost for linking equipment to an automation system in a semiconductor fab would be reduced considerably if the SECS protocol and its implementation offered a standardized procedure for interactive communications.

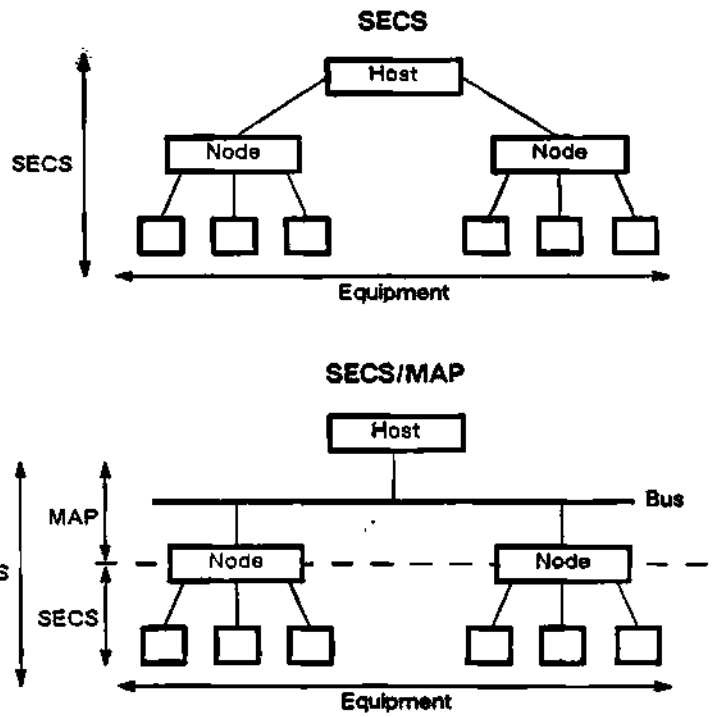
SECS: WHERE IS IT GOING?

There has been discussion that SECS might eventually be replaced by MAP, General Motors' Manufacturing Automation Protocol. MAP is a seven-layer, broadband, token bus-based communications protocol for the general manufacturing environment. It is based on internationally accepted standards, and its broadband transmission characteristics provide high-speed communications along the multichannel transmission line of the bus. However, MAP is still in the development stages and does not possess a message set, such as SECS II, that is focused directly on semiconductor manufacturing concerns.

SEMI's Communications Subcommittee established the Network Implementation Task Force (NITF) in 1985 to develop network standards for the semiconductor industry. In particular, the NITF has decided to evaluate the potential for implementing the MAP protocol in a semiconductor manufacturing environment. Figure 3 illustrates the point-to-point arrangement of computers and equipment specified by the SECS protocol and presents for comparison the topology that DATAQUEST expects will be employed in a SECS/MAP environment. This scenario retains the SECS protocol for communications between equipment and cell-level and node-level computers. Upper-level communications between host and node computers would follow the MAP specifications for a broadband, token-bus network. The SECS II message set would be maintained throughout the network environment because of its specificity to semiconductor manufacturing. MAP's message set is currently free-form in design and does not focus on the specific message needs of any given industry.

Figure 3

SECS AND SECS/MAP TOPOLOGIES



Source: DATAQUEST
May 1986

DATAQUEST ANALYSIS

DATAQUEST believes that equipment host communications is a critical component in the automated manufacturing environment. Our current evaluation of this topic concludes that:

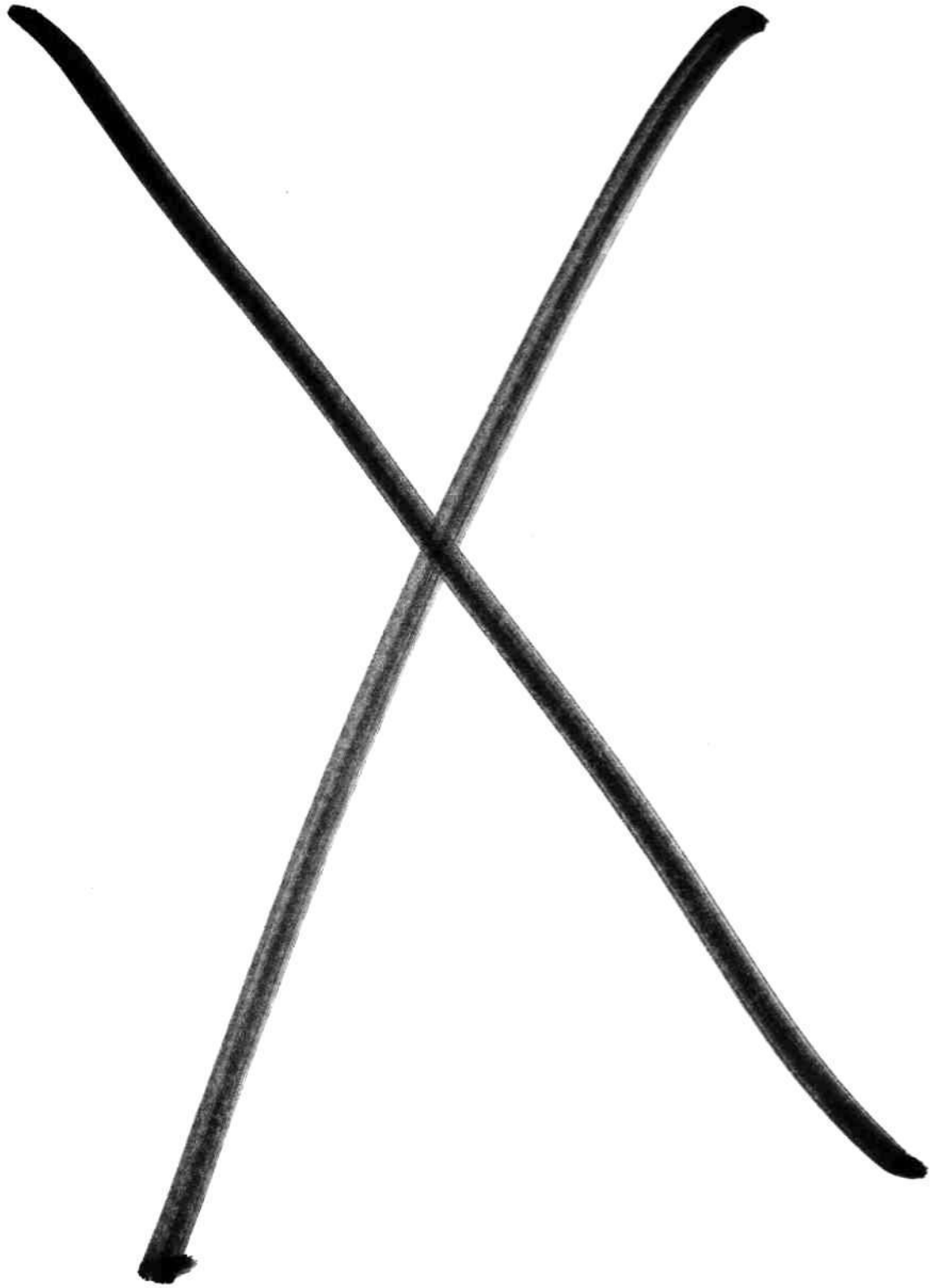
- The SECS protocol has been accepted as the industry standard for communications.
- While MAP may have a future in the semiconductor industry, it will not replace SECS at the equipment level.
- The opportunity exists for equipment manufacturers to gain a strategic market advantage with active participation in SECS protocol development.
- Equipment protocol implementation should not be a proprietary issue.
- DATAQUEST strongly encourages IC manufacturers to establish a clear consensus on SECS protocol specifications.

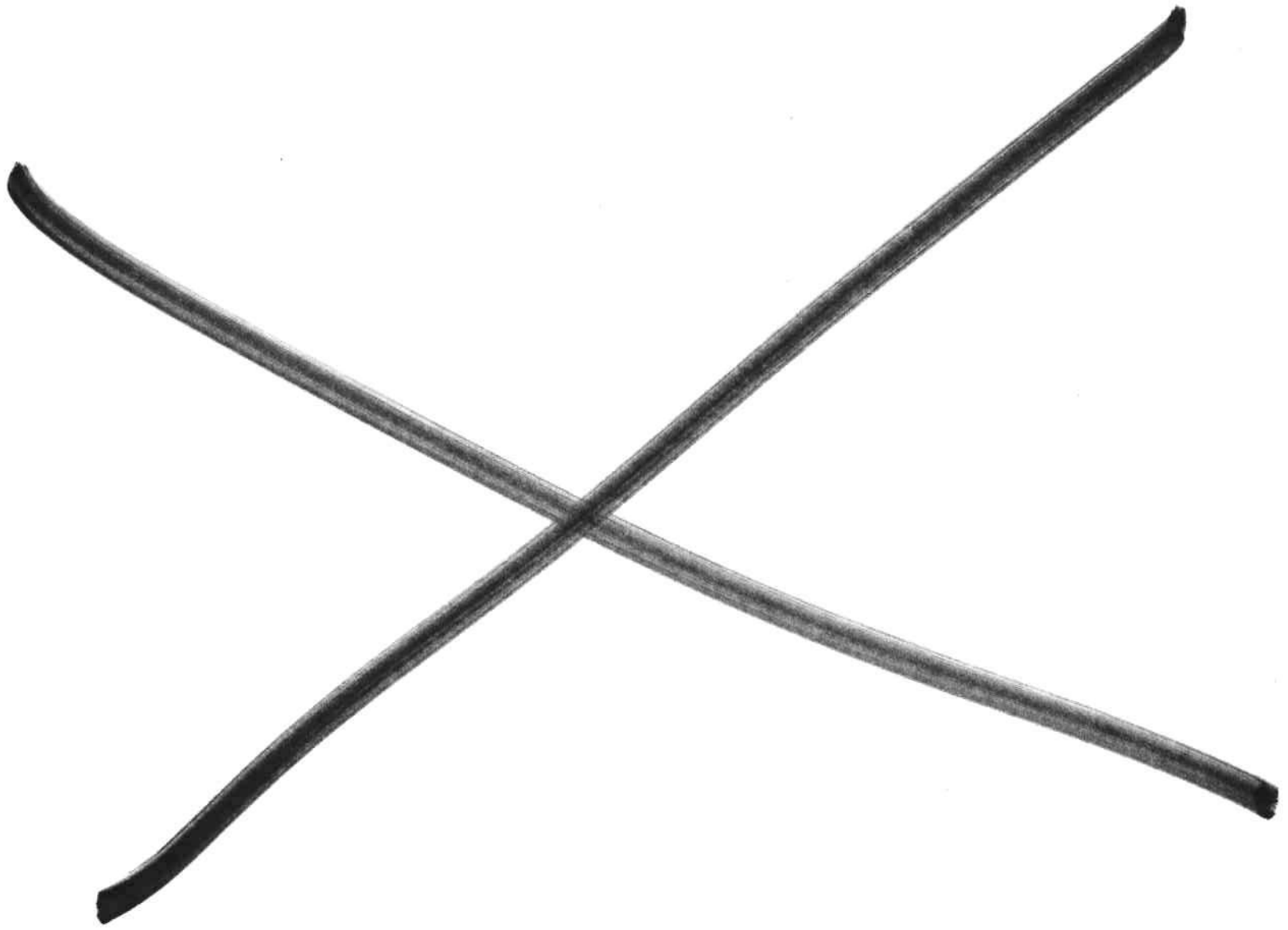
The SECS protocol clearly has been established as the standard for communications in the U.S. semiconductor industry. European and Japanese semiconductor manufacturers are also adopting the protocol in their own facilities. To assist in the distribution of information on the protocol, the SEMI Communications Subcommittee has made presentations in Japan and the SECS protocol document has been recently translated into Japanese. Japanese equipment and computer manufacturers are contributing to protocol modifications and development through JEIDA (the Japan Electronic Industry Development Association) in order to achieve standardization of the SECS protocol.

DATAQUEST believes that equipment manufacturers that actively participate in developing the SECS protocol and formulating the protocol specifications for their specific equipment categories will gain a strategic market advantage in providing equipment to the semiconductor industry. Equipment manufacturers have the opportunity to participate in the formative stages of automation in the semiconductor industry and, in the process, can establish firm relationships with the automation leaders. Semiconductor manufacturers that are not yet active in the automation arena will evaluate their future equipment purchases not only on equipment performance, but also on equipment manufacturers' proven automation experience and protocol acceptance.

The potential for incorporating the MAP protocol into the automation networks of semiconductor manufacturing facilities is still under evaluation. SECS, however, is the protocol that manufacturers are specifying today. DATAQUEST believes that the SECS protocol, in one form or another, will survive the transition to any MAP-based system in the future. Regardless of which protocol is employed, the need for better communication between equipment and semiconductor manufacturers mirrors the automation goal itself: to develop reliable, interactive communications between the various components in an integrated, automated, manufacturing environment.

Peggy Marie Wood





July Newsletters

The following is a list of the material found in this section:

- SEMICON/West 1986: Equipment Frontiers
- A Visit To The Canon Factory
  Utsunomiya, Japan

DataQuest
a company of The Dun & Bradstreet Corporation

NEWSLETTER

SEMS Code: 1985-1986 Newsletters, July 1986-7

SEMICON WEST 1986: EQUIPMENT FRONTIERS

Each year, DATAQUEST surveys the Semicon West Equipment and Materials Exposition at San Mateo, California. This industry trade show is sponsored by the Semiconductor Equipment and Materials Institute (SEMI) and is a yearly milestone for semiconductor equipment and materials vendors. This newsletter reports on our survey and features some of the major new products that were introduced at the show.

OVERVIEW

There were more than 50,000 attendees at this year's show. This is the largest attendance of any Semicon show yet, including the yearly shows in Boston, Dallas, Zurich, Tokyo, and Osaka. Semicon Tokyo had passed Semicon West last year as the largest show, but this year San Mateo regained the record.

Last year's equipment vendors were reeling from the sudden and deep decrease in orders, but this year's vendors had accepted the low level of production and were looking for signs that orders would increase. We found from our research that, although production had not increased for many months, there has been a significant increase in quote activity since the beginning of the year.

Materials suppliers had universally experienced growth in the first quarter and were cautiously looking at each month's shipments to see if the slight increase were real. Silicon had experienced an increase in levels and epitaxial wafers were in great demand. U.S. capacity utilization for epitaxial wafers was nearing 1984 levels.

In summary, the mood at this year's show was one of cautious optimism. We noted almost universal agreement with DATAQUEST's forecast that the European market had turned up in the first quarter, and that the U.S. and Japanese markets would turn up in the third and fourth quarters, respectively. This optimism is reflected in the inclination of equipment

and materials vendors to turn a negative situation into one replete with opportunity; there were more new product introductions this year than we have seen in the past.

NEW PRODUCTS

Semicon West has proved to be a favorite time of year to introduce new products. This year was no exception. Many new products and new product generations were unveiled, pushing the state of the technology toward submicron production.

This year's Semicon West show was particularly attractive for product introductions. For new products, the time interval from introduction to volume production is very critical. Each new system has engineering and process improvements that must be incorporated to make it production-worthy. It is very beneficial to have this period occur during a slump in the industry because there is less of a chance of losing market share and less of an incentive to rush to production before the product is ready. Since the industry is in its most severe downturn, these new product introductions are very timely.

SEMS personnel have surveyed the product introductions this year and will report on them in this newsletter. We have concentrated on the major fabrication equipment classifications. For more detailed information, please contact the manufacturer directly.

LITHOGRAPHY

The key developments in lithography were in X-ray and stepper technologies as these two technologies draw closer to direct confrontation. The developments by the X-ray equipment manufacturers indicate that they foresee the emergence of the X-ray market in the next year or so and that they are now getting into position for this market to take off. On the other hand, the developments by the stepper manufacturers (submicron resolution and better registration) indicate that the stepper vendors want to forestall the emergence of the X-ray market as long as they can continue to push optical technology into the submicron realm.

Another significant development was the announcement by an Austrian company of an ion-beam projection lithography system for sub-0.5-micron lithography in the laboratory.

The new developments in e-beam lithography and maskmaking were concerned largely with software and data processing. No new significant hardware developments were announced. Perhaps the lack of new e-beam lithography equipment indicates the relative maturity of this technology, and/or the difficulty of producing a high-throughput e-beam system that will compete against X-ray and stepper technology on the production line.

DATAQUEST did not perform a detailed survey of the contact/proximity and projection aligner market. However, two new products in these areas included the Perkin-Elmer Model 600 D projection aligner (a less expensive version of the Model 600 HT) and the Karl Suss MA 150 contact/proximity aligner for 150mm wafers.

X-ray Lithography

Several significant announcements were made in X-ray lithography as the X-ray equipment vendors begin to anticipate the emerging X-ray market of the late 1980s and beyond. The advantages of X-ray lithography, including resolution down to 0.2 micron, large depth of focus, high throughput, and wide process latitude, will become more and more important as the industry continues its inexorable push to smaller and smaller geometries and the concomitant tougher demands on optical lithography.

Micronix

Micronix introduced its MX-1600, a production-oriented step-and-repeat X-ray aligner with a resolution of 0.5 micron and an alignment accuracy of plus/minus 0.1 micron (2 sigma). The MX-1600's automatic laser alignment system performs site-by-site alignment with alignment continuously being done during the exposure. Dynamic alignment should provide better overlay accuracy when exposing large fields that may require longer exposure times. For alignment of the wafer and mask, a z-axis alignment is provided in addition to the traditional x, y, and theta alignments.

The MX-1600, which can handle 100mm to 150mm wafers, uses a 6kW stationary palladium X-ray source with a reduced spot size. Exposing field size can be varied from 20mm x 20mm to 50mm x 50mm, and using a 40mm x 40mm field, a 150mm wafer can be exposed in seven steps. Throughput is 10 to 20 wafers per hour, depending on the field size.

Source-to-mask distance is adjustable as is the nominal 25-micron mask-to-wafer gap. An environmental chamber is required. The MX-1600, priced at $900,000, will be available for delivery this year.

Micronix's first product was the MX-15, a full-field X-ray aligner for 100mm wafers that was introduced in May 1983. A few MX-15s have been sold to date.

Karl Suss

Suss made its U.S. introduction of the XRS-200 step-and-repeat X-ray aligner, which was previously unveiled at Semicon Europa in March. Suss is a partner in the German cooperative X-ray development program, which also includes the Fraunhofer-Institut fur Mikrostrukturtechnik (IMT), as well as AEG-Telefunken, Eurosil, Hoechst, Siemens, and Valvo/Philips. IMT is the steering organization for the group. As part of the development program, Suss built the Max-1 X-ray stepper, which was first installed at the BESSY synchrotron radiation electron storage ring at

IMT's lithography laboratory in Berlin in 1984. The Max-1 was equipped with Siemens' alignment system, and since it was a research tool, it was not optimized for high throughput.

The XRS-200 X-ray aligner is a second-generation system designed to be used with a compact storage ring for synchrotron radiation (COSY). Since it is designed for use with an electron storage ring source, the mask and wafer are held in a vertical position. Mask-to-wafer distance is nominally 40 microns with a range of 0 to 70 microns. The XRS-200 is capable of 0.2-micron resolution with the synchrotron radiation source at a 40-micron mask-to-wafer gap.

The XRS-200 features automatic wafer and mask handling and will expose 20 wafers per hour. Alignment accuracy is 0.1 micron (2 sigma). Maximum wafer diameter is 200mm, and field size can vary from 25mm x 25mm to 45mm x 45mm. Alignment and stepping time are each 1 second. Exposure time is 2 seconds per 30mm x 30mm field with a resist of sensitivity of 100 mJ/cm^2. Wafer change time is 10 seconds.

Suss will also be offering an X-ray plasma source developed by IMT (Aachen). Source wavelength is 7 to 10 angstroms, X-ray output per pulse is 25 joules, pulse frequency is 1Hz and exposure time per field is less than one minute. The LSX-10 plasma source is designed for use with the XRS-200 aligner, in which the mask and wafer are in a vertical position. The resolution of the XRS-200 with the LSX-10 plasma source will be about 0.5 micron. The LSX-10 will be available in the second half of 1987, but Suss will start quoting next month the XRS-200 aligner with the LSX-10 source for a price of $1 million.

COSY Micro Tec GmbH

COSY Micro Tec announced its COmpact storage ring for SYnchrotron radiation (COSY). This company was founded to develop and manufacture a smaller storage ring for X-ray lithography based on the results and experience of the research done on the larger BESSY storage ring in Berlin. The COSY is intended to be used by semiconductor manufacturers for high-volume IC production using X-ray lithography. The COSY will be marketed by Leybold-Heraeus, the majority shareholder in COSY Micro Tec.

The commercial version of the COSY is in the shape of an oval racetrack and will use superconducting magnets to bend the electrons at either end of the racetrack. The COSY will be the first synchrotron radiation source for X-ray lithography to use superconducting magnets, which also help to reduce the footprint of the COSY to make it more compatible with IC fabrication facilities.

The COSY's critical wavelength is 12 angstroms with a 4.5 tesla magnetic field and 630-MeV electron energy. Maximum radiative power at a distance of five meters is 250 mW/cm^2. Electron storage time is about 10 hours, and the time for refilling is 15 minutes.

The first version of the COSY (with conventional magnets and a lower electron energy) is being built at BESSY and should be completed by spring 1987. Three Suss XRS-200 X-ray steppers are scheduled to be

installed on the COSY, the first this fall and the remaining two in the spring of 1987. The commercial version of the COSY, with superconducting magnets, will accommodate 8 to 10 of the XRS-200s and will be available for delivery in 1988.

The COSY is expected to cost about $7 million. With 10 Suss XRS-200 aligners at a price of $750,000 apiece, the total cost for such a production system will be $14.5 million, or $1.45 million per stepper port.

Steppers

Hitachi was the only one of the nine stepper vendors not to exhibit its product at Semicon. Among the eight vendors that did, however, the emphasis was on submicron capability and price. Every one of the eight, including Ultratech, now has submicron capability, although Eaton did not actually exhibit its new submicron stepper because it is still under development. The new advanced submicron reduction steppers ranged from $900,000 to $960,000 in price. Even Ultratech's new submicron stepper is priced at $800,000. Whereas, in 1985 the average selling price (ASP) of all steppers sold was $633,000, we can now expect the ASPs to climb in 1987 and beyond.

Canon, Nikon, and Ultratech provide their own lenses. However ASET, ASM, Eaton, GCA, and Perkin-Elmer now not only all use Zeiss lenses, but the same Zeiss lenses. Although GCA does use some Tropel lenses and Perkin-Elmer uses some Wild Heerburg lenses, there is a concern about the ability of Zeiss to satisfy all the demand for lenses. This is a problem the Japanese stepper vendors do not have, and it remains to be seen whether this will be a factor in the overall stepper market dynamics.

GCA

GCA featured the Model 8000 Wafer Stepper, which is an advanced submicron stepper available with a family of g-line and i-line lenses. Production resolution to 0.9 micron is achieved with the g-line series of lenses, and resolution to 0.7 micron is obtained with the i-line lenses. The 8000 currently uses a global alignment system, called the Automatic Wafer Alignment Digitized (AWAD), to provide an alignment accuracy of plus/minus 0.2 micron (3 sigma) for a single machine and a machine-to-machine overlay accuracy of plus/minus 0.3 micron (3 sigma). The new field-by-field alignment system, which will provide a better alignment accuracy than mentioned above, will be released in July 1986. Other features of the 8000 include the new Maximus 2000 illuminator, a new metrology system, a new Class 10 environmental chamber, and the new backside wafer handler.

The 8000 equipped with the 0.9-micron g-line lens (20mm-diameter field) has a throughput of 46 and 37 wafers per hour for 125mm and 150mm wafers respectively. The base price of the 8000 with the g-line lens is $960,000.

Ultratech

Ultratech introduced the Model 1100 1:1 stepper, which can handle wafers up to 200mm. The system's standard lens provides a 1-micron resolution with a 3-micron total depth of focus. Available as an option is a lens providing 0.85-micron resolution with a 2-micron total depth of focus. The 1-micron lens is already in the field, since it has been an option previously available on the Model 1000 stepper. Deliveries for the 0.85-micron lens will begin at the end of this summer.

The 1100 provides alignment accuracy of 0.13 micron (2 sigma) and 0.16 micron (98 percent). Overlay registration is 0.3 micron (98 percent). The resolution and alignment specifications are obtainable over the entire 292mm^2 field. Illumination uniformity has been improved to plus/minus 2 percent. Throughput is 80 100mm wafers, 40 150mm wafers, and 24 200mm wafers per hour. A particulate specification is also provided; less than 0.1 particles (1-micron size) per cm^2 per pass.

The 1100 is priced at $800,000, including the 1-micron lens, with limited deliveries to begin at the end of 1986.

American Semiconductor Equipment Technologies (ASET)

In March 1986, TRE Corporation sold its semiconductor equipment subsidiary to ASET, a new venture-capital-backed company formed expressly for the buyout. ASET purchased the assets and technology of TRE's maskmaking, photolithography, and flat-substrate operations and transferred TRE's entire personnel team to the company.

ASET displayed at Semicon the Model 800 Series Wafer Stepper enclosed in a new Class 10 environmental chamber. New features on the 800 include magnification and focus control for barometric pressure changes, a new cassette loader, upgraded software, a Hewlett-Packard 9220 computer, SECS II compatibility, a higher precision stage (lambda/32), and nonactinic alignnment.

The 800 offers a lineup of Zeiss lenses, including a 10X, 0.315 numerical aperture (NA), i-line; a 10X, 0.42 NA, i-line; a 5X, 0.38 NA, g-line (10-78-46); and a 10X, 0.38 NA, g-line lens. ASET currently has two i-line systems in the field for gallium arsenide work (RCA and Triquint). Both systems use the 10X, 0.315 NA lens; the 10X, 0.42 NA lens will be available this June. In addition to these, a third i-line lens (5X, 0.42 NA) will be available in the third quarter.

ASET announced, but did not exhibit, the 900 SLR Series Wafer Stepper, which incorporates the features of the 800 but is designed for 200mm wafer capability.

ASET also introduced its new line of substrate steppers for liquid-crystal and flat-panel applications. Based on the 800 wafer stepper technology, the substrate steppers use large-travel x-y stages and are the first commercial reduction steppers for flat-panel displays. Flat-panel displays are currently printed with special 1:1 contact printers.

Two models are available, the Model 800 substrate stepper, which accommodates panel substrates from 5 x 5 inches to 8 x 10 inches, and the Model 1500, which handles substrates up to 15 inches square. Both systems use a Zeiss 5X, 29mm field diameter, 0.20 NA, g-line lens to obtain a resolution of 1.75 micron. Throughput is about 17 substrates per hour but will have to be improved to be price competitive with 1:1 contact printers. Price of the 800 is $650,000, and the price of the 1500 is $800,000. ASET has shipped systems to General Electric and IBM.

ASM Lithography

Although it was announced in May 1985, this was the first time that the PAS 2500 has been exhibited in the United States. This machine (serial number 5) will be returned to Europe after the show, leaving ASM without a 2500 in the United States; it will probably be August when the first U.S. delivery is made to Cypress Semiconductor. Until a demonstration system is installed at ASM in Tempe, Arizona, sometime in early fall, wafer demonstrations will be done at ASM in Holland.

The PAS 2500 is available with two Zeiss lens options, the 2500/10, which uses the 5X, 0.38 NA, g-line lens (10-78-46), and the 2500/20, which uses the 5X, 0.32 NA, i-line lens (10-78-52). Although both lenses are specified with a production resolution of 0.9 micron, the i-line lens has a larger field than the g-line lens (23mm versus 20mm diameter). Exposure time for 1-micron thickness of HPR photoresist is 300 msec for the 2500/10 and 200 msec for the 2500/20. Throughput on the 2500/10 is 55 150mm wafers per hour with global alignment versus 70 wafers per hour for the 2500/20. Besides the high throughput, the PAS 2500 offers exceptional overlay accuracy of plus/minus 0.10 micron (3 sigma), any layer to zero layer, global alignment.

The PAS 2500 has a capacity for seven reticles (the 2000 could only handle two) and uses an electromagnetically driven stage. Although not a specification yet, ASM is shooting for a particulate specification of six particles greater than 0.3 micron on a 150mm wafer.

The PAS 2500 with either lens is priced at $925,000 in contrast with a base price of $600,000 for the PAS 2000B, which is still being offered.

Canon

Canon exhibited the new FPA-1550 MII Fine Pattern Aligner, which incorporates several improvements over the FPA-1550. These include a new lens, better alignment accuracy, automatic change in lens magnification to compensate for fluctuations in barometric pressure, new software to allow easier operation, and a smaller footprint obtained by a more compact control system.

The new lens offered on the FPA-1550 MII is a dual-telecentric, 5X, 0.43 NA, g-line lens with a field of 21.2mm diameter (15mm X 15mm). Resolution of the lens is 0.8 micron, and the depth of focus is plus/minus 1 micron. For comparison, the FPA-1550 uses a dual-telecentric, 5X, 0.35 NA, g-line lens with a field of 20mm diameter. Resolution of this lens is 1 micron, and the depth of focus is plus/minus 1.4 micron.

Alignment accuracy has been improved from 0.25 micron (3 sigma) on the FPA-1550 to 0.225 micron (3 sigma) on the FPA-1550 MII, die-by-die mode.

The price of the FPA-1550 MII is approximately $900,000. The system at Semicon was the first MII in the United States; a few MIIs have been installed in Japan.

Eaton

Eaton displayed the 8605 Reduction Wafer Stepper, which has been on the market for some time. However, Eaton announced the development of the 9800 Reduction Wafer Stepper, a system designed for submicron resolution using the Zeiss family of lenses. This will be the first Eaton stepper to use Zeiss lenses; the 8600 Series uses Tropel lenses. Lens options include the 5X, 0.38 NA, g-line (10-78-46); the 5X, 0.42 NA, i-line (10-78-52); and the 10X, 0.42 NA, i-line (10-78-48) lenses. Production resolution will be 0.91 micron with the 10-78-46 lens. Overlay accuracy will be plus/minus 0.15 micron (3 sigma) for field-by-field alignment or plus/minus 0.25 micron (3 sigma) for blind stepping.

The 9800 will use an inertial stabilization system to eliminate the vibration caused by starting and stopping the laser-aligned stage. This will allow use of a rigid tower with bottom focusing at the wafer plane. Additional features include a library of 16 reticles (the 8600 Series could handle four) and backside wafer handling. The 9800 will handle wafers up to 200mm. Throughput for 150mm wafers will be 45 and 32 wafers per hour for global and field-by-field alignment, respectively.

The 9800 is currently in the prototype stage with first deliveries to start in the fourth quarter of 1986. The price of the 9800 with the 10-78-46 lens will be $950,000; the price of the 8605 is $775,000.

Nikon

Nikon exhibited the NSR-1505G stepper, which featured two new 5X g-line lenses: the 5A3 0.8-micron, 0.42 NA lens with a 1.5-micron depth of focus (total), and the 5A2S 0.9-micron, 0.35 NA lens with a 2-micron total depth of focus. Both lenses have a field size of 15mm x 15mm. These new lenses are in addition to Nikon's four other 2.5X/5X/10X g-line lenses. Nikon currently has a 10X, 0.8-micron, 0.35 NA, i-line lens with a field size of 10mm x 10mm and is developing a 5X i-line lens for introduction later this year.

Nikon has also recently introduced a faster reticle changer specifically designed for the special needs of ASIC manufacturers. With the new robotic reticle changer, reticles can be changed in one minute versus 4.5 minutes on the previous reticle handler.

Perkin-Elmer

Perkin-Elmer exhibited the SRA-9000 Series stepper, which is available in two versions. The SRA-9528 uses a Zeiss 5X, 0.28 NA, h-line lens (10-78-41) with a resolution of 1.25 micron and a field size of

29mm diameter. The SRA-9535 uses a Wild Heerbrugg (parent company of Leitz) 5X, 0.35 NA, h-line lens with a resolution of one micron and a field size of 24mm diameter.

Features of the SRA-9000 series include field-by-field alignment, leveling and focusing, laser prealignment, and an optional laser stage global alignment system. The automatic reticle-handling system can handle from 7 to 15 reticles, depending on the pellicle standoff. Reticles can be changed in 16 seconds. The SRA-9000 uses a backside pick-and-place wafer-handling system that can handle wafers up to 150mm.

Alignment accuracy is plus/minus 0.15 micron (98 percent) for field-by-field alignment and plus/minus 0.35 micron (98 percent) in the global alignment mode. Throughput for 150mm wafers is 50 to 55 wafers per hour on the 9528 and 40 wafers per hour on the 9535.

The price of either the 9528 or 9535 is $815,000 plus an additional $100,000 for the optional laser stage. Deliveries of the SRA-9000 series began approximately one year ago.

E-Beam

The e-beam manufacturers' emphasis this year at Semicon was clearly not on hardware, but on software and data processing enhancements. Although JEOL made a hardware upgrade by adding 150mm wafer capability to its e-beam system, JEOL and the other e-beam manufacturers emphasized the introduction of new software packages for their systems.

Perkin-Elmer

New for Perkin-Elmer at Semicon was the MEBES III Data Processing System (DPS). This is an off-line data processing system using Concurrent Computer Corporation's 3252 computer. The DPS allows the user to do pattern data preparation off-line from the MEBES III, thus freeing the MEBES III from some data preparation tasks and enabling it to spend more time writing masks and reticles. The multiuser DPS allows multiple data preparation tasks to be run simultaneously on the system. Priced at $375,000, it will be available for delivery in July.

Perkin-Elmer also announced the MEBESNET, a LAN-like network that allows MEBES data to be transferred via a data link to the MEBES from the DPS. It will also interface with the KLA Klaris inspection system. Previously, data had to be transferred via magnetic tapes that were carried from point to point. The first MEBESNET link costs $65,000 and each additional link is $32,500.

JEOL

JEOL introduced the JBX-6AIII. This latest model in the JBX-6 series has a larger chamber that is capable of processing 150mm wafers and 7-inch plates. In addition, buffer memory storage on the JBX-6AIII was expanded to 150 megabytes from the 9-megabyte memory on the JBX-6AII. The memory expansion is to accommodate the postprocessing sizing-and-scaling feature available on the JBX-6AIII. It may be that, upon

examination of the critical dimensions after the wafer is written and processed, it is determined that a change in device scaling is required. Previously, the procedure was to return to the CAD system to generate new JEOL data tapes with the new scaling factor. With the time-saving sizing-and-scaling feature of the JBX-6AIII, the original data tape is still used and the scaling changes are automatically done in the e-beam column.

The JEOL-6AIII is priced at $3.2 million with all the features. Two units have been sold in Japan and none in the United States.

Cambridge

New for Cambridge was an improved e-beam deflection system to make it more stable, with the result that the resolution of the EBMF 10.5 e-beam system on gallium arsenide is now less than 0.1 micron; it was previously in the range of 0.15 to 0.20 micron. Cambridge has also differentiated the EBMF 10.5 into two application-specific versions: the EBMF 10.5CS, which is intended for the direct writing of compound semiconductors, and the EBMF 10.5RM, intended for maskmaking applications.

The major differences between the CS and RM versions are in the new software packages provided with the machines. The CS model has added software specifically for direct writing of fine-line geometries, including a proximity correction program. The RM version has specific software for reticle writing, including a job management package.

A fully configured EBMF 10.5 CS or RM version is priced at $2 million with delivery now available.

Ion-Beam Lithography

Ion Microfabrication Systems (IMS), of Vienna, Austria, was founded in 1985 with the help of venture capital funding to pursue the opportunities that the various ion-beam technologies will offer in submicron device fabrication. At Semicon, IMS announced the development of the first of several potential products to utilize ion-beam technology, the IPLM-01 Ion Projection Lithography Machine. This system is designed to be a research tool for the investigation of sub-0.5-micron-resolution lithography.

The IPLM-01 is an ion-optical reduction wafer stepper using an ion source, stencil mask or reticle, and electrostatic ion focusing lenses to provide either a 5X or 10X reduction of the mask and an x-y stage. The system can perform die-by-die alignment. Alignment is done in two steps: a coarse mechanical alignment performed by the x-y stage and a fine alignment accomplished with fast electrostatic fine adjustment of the ion beam in x, y, and theta dimensions. No mechanical motion is required for the fine adjustment.

The IPLM-01 is capable of sub-0.5-micron resolution with an alignment accuracy of 0.02 micron and a depth of focus of more than 100 microns. With current equipment, die size is limited to 4mm, but with further development the use of reticles with an active area of 50mm x 50mm

will allow the use of 10mm x 10mm die with 0.2-micron resolution at 5X reduction and 5mm x 5mm die with a resolution of 0.1 micron at 10X reduction. Both resistless techniques using direct modification of the substrate material and resist techniques using conventional organic resists are being investigated.

The first IPLM-01 research tool has been delivered to the Fraunhofer-Institut fur Mikrostrukturtechnik in Berlin. This is the same organization that is heading the German cooperative X-ray program mentioned above. A commercial pilot production version of the IPLM-01 may be available as soon as 1987 at a price exceeding $1 million. A production ion-optical wafer stepper is not expected until 1990 to 1992.

AUTOMATIC PHOTORESIST PROCESSING EQUIPMENT

Eaton, GCA, Machine Technology, Inc., Semiconductor Systems, Inc., Silicon Valley Group, and Solitec introduced new features to their track equipment at Semicon West. Semix, a U.S. distributor for Japanese manufacturers, became a new player in the U.S. track market with the introduction of two new systems.

Eaton

Eaton's System 6000 Photoresist Processor features improved contamination control and touch-screen input. This is an enhanced version of the company's previous 6000 system. The enhanced System 6000 has optical sensors that replace the processor's air sensors and thereby reduce particle contamination. The enhanced System 6000 also features a touch-sensitive screen that replaces the standard keyboard, enabling English I/O communication with the system. The software conforms to SECS II, facilitating PC control or host interfacing.

GCA

The GCA Wafertrac 1006 features remote racks for bottles of gas and for controls for out-of-clean-room maintenance. Remote racks can be located up to 20 feet away from the 1006 system. Also introduced was the Interface II, which is used to interface the Wafertrac 1006 and DSW Stepper systems into integrated lithography cells.

Machine Technology (MTI)

MTI introduced its FlexiFab product line, which it claims is the industry's first system to be composed of independent wafer processing modules connected only by computer data links. Up to 16 process modules can be combined to build each system to the customer's specifications. Each module has its own controller, handler, characteristic process assembly, and automatic facilities connections. The FlexiFab can handle 125mm to 200mm wafers as well as squares.

MTI also displayed another product line, the TargeTrack parallel processing system. Currently available in coat/bake and develop/bake configurations, TargeTrack is equipped with automatic cup rinse and is programmable for dynamic, static, and radial dispensing. The TargeTrack has three independent load arms. TargeTrack's open-top design and internal vacuum plenum maintain environmental laminar flow through the machine itself, which minimizes contamination. TargeTrack's controller contains an EEPROM programmable for 99 process steps applicable to 20 recipes of 20 steps each.

General Signal/Semiconductor Systems Inc. (SSI)

SSI introduced the GlasMaster, which it claims is the first dedicated production system for spin-on-glass applications for interlayer dielectric planarization.

Silicon Valley Group, Inc. (SVG)

SVG introduced an SVG/ASM lithography interface that interfaces the SVG 8600 series track to the ASM PAS-2500 Waferstepper. Also shown at Semicon was the 8640 Multiple Hot Plate Bake Oven. This is claimed to be the first system completely designed for long bake time processes. It has an intelligent beltless wafer handler for transferring wafers between the hot plates and coater or receiver. With SVG's "oven priority baking," the handler responds to a wafer culminating baking prior to other wafer transfer operations.

Reid-Ashman/Solitec

Solitec displayed its 9200 Series track equipment. The 9200 features a self-contained vertical laminar flow, which Solitec claims provides better than a Class 10 environment. The 9200 is SMIF (Standard Mechanical Interface) compatible and has a beltless vacuum indexer and a beltless "tray and pocket" transport through the system. It also features remote diagnostics and top- and bottom-edge bead removal.

Tazmo (Semix)

Displayed for the first time in the United States by Semix were two new products from Tazmo Corporation, a Japanese company. Semix introduced the TR-8000 and the TR-6000. The TR-8000 is a 200mm spincoat/bake/develop/etch system. The TR-8000 can also include ultraviolet curing and cleansing and can handle 125mm, 150mm, 175mm, and 200mm circular masks and wafers as well as 125mm and 150mm square masks and wafers. Its transport system features a SCARA robotic arm with automatic size recognition, obviating the need for equipment modification. The TR-6000 series is a line of spincoat/bake systems for 150mm wafers. Both the TR-6000 and TR-8000 have been designed for spin-on-glass applications.

DRY PROCESSING

Parallel Plate Etchers

Parallel plate etching is represented by about 20 companies. The market has been able to support these companies in their various niches for several years without an appreciable shakeout, although there have been considerable shifts in market share.

Balzers

Balzers introduced its SWE 654 Single Wafer Etcher. This system can use a 13.56-MHz (or optionally a 100-kHz) RF generator to power the top, bottom, or both electrodes. Balzers features processes for silicon dioxide (HTO), PSG, aluminum (with 1 percent silicon), and silicon trench etching. It has capability for 100mm, 125mm, or 150mm wafers. Balzers claims typical throughputs of 55 wafers per hour for silicon dioxide, 70 wafers per hour for PSG, 45 wafers per hour for aluminum, and 8 wafers per hour for silicon trench (7 micron). The system is manufactured in Hudson, New Hampshire, and the company had shipped five systems as of Semicon West. The system sells for $250,000.

Drytek

Drytek introduced a flush-mount version of its Quad System, which was introduced last year at Semicon West. It also introduced a single-wafer, R&D version of the Quad System. Most notably, the company introduced several new processes for the Quad. Drytek claims that it has characterized more than 40 different processes for the Quad. The Quad is a four-chamber system with independent control of each chamber. It is capable of processing up to 200mm wafers and sells for $395,000.

Lam Research

Lam introduced a flush mounting for its AutoEtch 690 aluminum etcher. These "bulkhead" systems, also available on the AutoEtch 490 polysilicon etcher and AutoEtch 590 oxide etcher, conserve floor space and allow maintenance to be done in the corridor behind the clean-room walls. These systems are cassette-to-cassette, single-wafer etchers with capability for 3-inch to 150mm wafers. The sales prices are $250,000 for the 490, $260,000 for the 590, and $365,000 for the 690.

Materials Research Corp. (MRC)

MRC introduced its ARIES system to the United States. It was first introduced at Semicon Europa in March. It has a magnetron-enhanced, single-wafer reactive ion etcher capability of 3-inch, 100mm, 125mm, and 150mm wafers. MRC is offering dry development of photoresist, planarization, polymide, and bilevel and trilevel etching with this system. Because of the magnetron plasma enhancement, etching can proceed at very low pressures, less than 10 millitorrs, while maintaining adequate throughputs. The price of the system is $395,000.

Tegal

Tegal introduced the Model 1500e enhancement of the previous Model 1500. It is a single-wafer, trielectrode, dual-frequency etcher with capability for 3-inch to 150mm wafers. The 1500e is said to reduce the particulate generation during processing. The applications include polysilicon, aluminum alloys, silicon dioxide, silicide, and silicon trench etching. The system's price ranges from $310,000 to $390,000.

The company also introduced the 980 Series for 200mm wafers. These are single-wafer, tabletop etchers for strip/descum/backside etch, polysilicon, and silicon dioxide etching. The system's price ranges from $110,000 to $220,000 and it will be available November 1986.

Tegal has also formed a Special Products Department within the 900 Operations Group. This department will pursue a "custom" business. This type of business can seriously degrade a production line's profitability unless the engineering and production are managed as a separate business segment.

Tokuda

The Hirrie 100 is an improved version of the single-wafer, magnetron etcher that was introduced two years ago. This version has a different magnet configuration that scans back and forth below the wafer chamber. Tokuda has added a DI rinse-and-bake module at the output of the exit loadlock. The system price is about $500,000.

Varian/Zylin Division

The new Zylin 100 is a single-wafer etcher that is positioned to etch the composite films that will be a part of submicron semiconductor devices. It has the facility to add up to five processing chambers. Unlike the previous Zylin 10, it will etch silicon dioxide, polysilicon, aluminum and its alloys, and composite films. Wafer size capabilities range from 3 inches to 200mm. The price of the system depends on the number of chambers and on the configuration but begins at about $100,000 more than its predecessor, which was $400,000.

Single-Wafer Strippers

One of the most interesting new product areas this year was that of single-wafer stripping. This technology is required to minimize gate oxide damage and gate thickness loss and to increase stripping efficiency. Gate oxide damage occurs because, during stripping, the oxide is exposed to a plasma environment that contains high-energy ions and electrons, X-ray radiation, and sputtered contaminants from the processing chamber. Yield losses result from this oxide damage, since there is an attendant C-V shift and threshold voltage degradation. Although the results are not conclusive, one solution is to remove the wafer from this plasma environment by creating the plasma in an upstream chamber. In addition, by increasing the free radicals that impinge on

the wafer, the etch efficiency is increased, which facilitates the removal of tenacious resist deposits that result from high-current implantation.

DATAQUEST has surveyed nine companies that have recently introduced single-wafer ashers. All but three of these products use remote plasma generation.

Alcan Tech, Inc.

This joint venture between CIT/Alcatel and Canon is marketing a Canon design, the MAS 800 Dry Etcher and Asher, which produces the plasma in a microwave waveguide with a magnetron. The system uses oxygen as a source of free radicals that flow through a quartz flow distributor to the wafer. The wafer sits on a temperature-controlled platen that can be raised to 250 °C. The company claims etch rates of up to 2.5 microns per minute, C-V shifts of less than 0.02 volts, and breakdown voltage shifts from 40V to 39V on 400 angstroms of SiO_2. The price of the system is approximately $100,000 including pumps.

Branson/IPC

Branson has introduced its L3200 Resist Stripper. This system uses two quartz chambers at 13.56 MHz to produce the plasma, typically from oxygen only. The dual chambers and wafers are independently pumped and controlled. The wafers sit on elevated quartz pedestals so that resist can be removed from both sides. The wafers are heated with quartz halogen lamps to between 200 °C and 275 °C. Branson claims 60 wafers per hour with 1.5 microns of resist on 150mm wafers. The system has capability for 200mm wafers. The price of the system is $130,000 without the pumping package.

Emergent Technologies

This new start-up has introduced the Phoenix 2320 NORD Photoresist Stripper. The plasma is produced in a remote chamber at 2.45 GHz. The wafer sits on pins so that the photoresist can be removed from both sides. The wafer is heated by infrared lamps to high temperatures. Processing is typically done at 275 °C. The company claims etch rates of 7 microns per minute at 275 °C at 80 100mm wafers per hour using an oxygen/halogen gas mixture. The price of the system is $110,000 including the pumping package.

Gasonics

The Gasonics Aura stripper produces the plasma in a 2.45-GHz waveguide made from alumina. The oxygen free radicals are introduced to the wafer through a quartz gas distribution ring. The wafer sits on pins so that the photoresist can be removed from both sides of the wafer. The system can be configured for 3-inch to 150mm wafers. Gasonics claims throughputs of up to 60 wafers per hour. The Aura stripper processes at less than 100 °C. The price of the system is $78,000 without pumping package.

Machine Technology Inc. (MTI)

MTI's AfterGlo DPR produces the plasma in an upstream microwave cavity at 2.45 GHz. The 1-to-5-torr chamber is maintained with a 150 standard cubic feet per minute oxygen service pump. The wafer sits on a temperature-controlled hot plate that is typically heated to 250 ^{o}C to increase the etch rate, which MTI claims is greater than 5 microns per minute. MTI uses oxygen, plus a second proprietary gas to act as a catalyst to promote dissociation of the oxygen, as the reactive gas. The price of the system is approximately $110,000 including the pumping package.

Matrix

The Matrix system is a later generation of the original system introduced last year. It produces the plasma in an upstream chamber using an RF generator at 13.56 MHz. The chamber material was changed from passivated aluminum to quartz to remove any possibility of contamination on the wafer. The system has a temperature-controlled electrode and holds the temperature between 100 ^{o}C and 200 ^{o}C, depending on application. The etchant gas is oxygen. The price of the system is $87,500 including the pumping package.

Contact Plasma Systems

Three companies employ in-contact plasma processing in the single-wafer mode. They are Plasma Systems (Semix), Plasma-Therm, and Tegal. These systems are used for both resist removal and planarization techniques.

Plasma Systems (Semix)

The PE 615 fully automated single-wafer planar plasma system can be used for a variety of etching processes. This system is being marketed by Semix in the United States for the first time. The system is a contact plasma system that sells for $125,000 including the pumps. Plasma Systems has been building plasma etchers since 1970. In 1984 it had annual sales of about $8 million.

Plasma-Therm

The Plasma-Therm system is a single-wafer, in-line system with entrance and exit loadlocks. Plasma-Therm claims a throughput of 40 to 60 wafers per hour and the system is capable of etching 3-inch to 150mm wafers. The wafer is in contact with the plasma. The system price is $95,000 without pumps.

Tegal

The Model 900e is a single-wafer, in-line stripper with no exit or entrance loadlock. The system has capability for 100mm, 125mm, or 150mm wafers and the RF frequency is 13.56 MHz. The system price is $110,000.

Remote Plasma Barrel Systems

One interesting product introduction was a remote plasma barrel stripper unveiled by Psi Star. The 8200 system produces the plasma in an RF chamber above the fused-quartz barrel chamber. The active species are pumped into the field-free region past the wafers. The wafers sit in quartz boats (75 wafers for 150mm to 200mm or 150 wafers for 3 inches to 125mm). Typical processing temperatures are between 130 ^{o}C and 160 ^{o}C. Psi Star claims typical throughputs of 100 to 125 wafers per hour. The price of the system is $90,000 excluding the pump.

CHEMICAL VAPOR DEPOSITION

Semicon West 1986 was the coming-out party for the CVD equipment segment of wafer fabrication equipment, as many significant developments were announced. Several start-up companies introduced their first products, and several established companies introduced their first CVD products.

What is the impetus behind this rash of new CVD products? Whereas, equipment developmental attention has been focused on the areas of lithography, ion implantation, and dry etching for submicron and near-micron devices, little attention has been given to deposition technology. Consequently, CVD deposition technology has lagged, and it is not adequate for the requirements of advanced devices.

The CVD equipment market was previously dominated by horizontal-tube reactors, and, consequently, it was somewhat intermeshed with the diffusion furnace market. Semicon witnessed the emergence of new vendors and the introduction of numerous machines dedicated to CVD processing. As a result, the older CVD equipment market is dynamically evolving into a clearly defined CVD market that will be shaped by the technological and entrepreneurial forces clearly in abundance at this year's Semicon.

Besides film quality, the emphasis was on automation and cleanliness. Of the eleven new models introduced by the ten companies listed below, ten offer cassette-to-cassette operation as standard and nine offer through-the-wall installation. Note that no horizontal-tube reactors are included; they are still struggling with cassette-to-cassette operation.

Novellus

A venture capital-backed start-up firm, Novellus, introduced its first product at Semicon, the LTP-2 Thermally Enhanced Plasma Chemical Vapor Deposition (TPCVD) reactor. The LTP-2 is a cassette-to-cassette, vacuum loadlocked system that can process wafers up to 200mm in diameter in a through-the-wall or standalone configuration. Films presently available include silicon oxides and silicon nitride. Films of SiO_2, PSG, and BPSG can be deposited on 150mm wafers at a rate of

6,000 angstroms per minute with a uniformity of plus/minus 1 percent across the wafer and a throughput of 80 wafers per hour (8,000-angstrom film).

The reaction chamber consists of eight deposition stations placed around a circular chamber. Underneath the stations is a rotating horizontal platen with positions for eight wafers. Each wafer rotates under the eight deposition stations such that the final film is built up of eight sequential depositions. Wafers are continuously loaded and unloaded between the rotating platen and the cassette of wafers in the loadlock. During the backfill of the loadlock for cassette exchange, an in situ chamber clean cycle can be done in parallel so as not to affect the throughput of the system.

Another feature of the LTP-2 is that no quartzware is used. The price of the LTP-2 starts at $450,000, with first deliveries to begin at the end of 1986.

As this newsletter goes to press, Applied Materials has agreed to acquire Novellus for $12 million; Novellus would operate as an independent, wholly owned subsidiary.

Focus Semiconductor Systems

Focus, a venture capital-backed firm founded in May 1984, introduced its first product at Semicon. The F1000 is a fully automated, cassette-to-cassette, low-pressure CVD (LPCVD) system for wafers up to 200mm.

The F1000 reactor is a "multiplexed" system that processes 18 wafers simultaneously in 18 single-wafer chambers. The reactor module consists of a vertical heater block to which are attached the 18 single-wafer reaction chambers. The 18 chambers are positioned in a vertical plane in a three-by-three array on either side of the vertical heater block. Each reaction chamber has its own gas injection system to optimize the gas dynamics, a system that Focus developed and calls the Focused Flow gas system. The 18 wafers are all heated to the same temperature from the common heater block. No quartzware is used in the reactor module.

Films currently characterized include silicon oxide, PSG, and BPSG, with other films under development. The deposition rate is up to 3,000 angstroms per minute with a uniformity of plus/minus 2 percent. The maximum deposition temperature is 700 ^{o}C. With the high deposition rate, a cyle time of 15 minutes per run can be obtained; this translates into a throughput of 70 wafers per hour for up to 150mm wafers and 35 wafers per hour for 200mm wafers.

The F1000 can be installed either in a standalone or through-the-wall configuration. The price of the system is $400,000, with first deliveries to begin in June 1986.

Varian Associates

Varian exhibited two new CVD systems at Semicon. The Model 5101, first introduced at Semicon Japan last December, is a cassette-to-cassette, single-wafer, cold-wall reactor that can operate in either a low-pressure (LPCVD) or plasma-enhanced (PECVD) mode. The cassette of wafers is vacuum loadlocked. The 5101 processes wafers up to 200mm in a facedown position and can be installed in either a standalone or through-the-wall configuration.

The 5101 is primarily intended for metallization and can deposit tungsten, tungsten silicide, and selective tungsten films. Throughput for refractory metals and silicides is from 8 to 15 wafers per hour. Film uniformity is plus/minus 5 percent for silicides and plus/minus 6 percent for refractory metals. The price of the 5101 is $360,000, with the first delivery to be in June 1986.

Varian also introduced the 5150 hot-wall CVD system intended for low-temperature oxides, nitrides, and polysilicon. The 5150 is a vertical-tube reactor using a quartz tube and an external resistance heater that can be installed in a standalone or through-the-wall configuration. It is a cassette-to-cassette system that can process 200mm wafers in 75- to 100-wafer loads. Wafers are processed facedown to reduce particulate contamination. Another feature that helps reduce particulates is the nitrogen loadlocked reactor tube, which keeps the reactor tube from being exposed to the atmosphere.

The reactor uses a proprietary cross-flow gas injection system to eliminate depletion effects. It also has a plasma clean mode that uses a titanium electrode placed outside the quartz tube. Since nothing is inserted into the reactor tube, this feature also aids in the reduction of particulates.

The 5150 is now in the process development stage undergoing determination of process specifications. The target for first shipments is mid-1987. The 5150 is expected to be priced in the $400,000 range.

Spectrum CVD

A Motorola New Enterprise Group company, Spectrum CVD was, however, not acquired by Motorola, but was a start-up company founded in 1984 by J. B. Price, of Motorola, with venture capital provided by Motorola. Spectrum introduced its first products at Semicon: the 211 and 202 CVD reactors for deposition of tungsten silicide and selective tungsten.

The 211 reactor is a fully automatic, cassette-to-cassette, vacuum loadlocked, single-wafer reactor. Wafers are transferred from the plastic cassette into another cassette in the loadlock; they are then transferred into the reaction chamber. Wafers are processed facedown with the backside of the wafer in contact with a horizontal quartz window. Thus, since the reactor is a cold-wall design, deposition occurs only on the active side of the wafer. The wafer is radiantly heated through the quartz window.

For film deposition, the reactor operates in a thermally enhanced or plasma-enhanced CVD mode. It can also operate in a plasma clean mode between deposition cycles, and in a plasma etch mode for the removal of native oxide just prior to selective tungsten deposition.

The deposition rate for tungsten silicide is 1,500 angstroms per minute; for selective tungsten the rate is 1,600 angstroms per minute. For selective tungsten, films greater than 1 micron can be deposited. Throughput is approximately 20 wafers per hour. The 211 can be installed in either a standalone or through-the-wall configuration.

The 202 uses the same reactor as the 211 but is a manual system designed for engineering development work. Spectrum currently has five prototype 202/211s operating at its facility.

The price of the 202 is $225,000, with first deliveries to begin in September. The price of the 211 is $400,000, with deliveries to begin in December.

Silicon Valley Group (SVG)

SVG introduced its new 6000 VTR vertical-tube reactor for diffusion and low-pressure CVD processing. It is a fully automated cassette-to-cassette system that utilizes a robotic transfer mechanism to directly load the vertical quartz carrier from the plastic cassettes. The system will handle up to nine cassettes of live and dummy wafers; the transfer mechanism can be programmed to select either type of wafer for insertion into the quartz carrier.

There are two vertical quartz carriers on a "lazy Susan" rotating table; while one carrier is being loaded/unloaded the other carrier is undergoing processing in the vertical quartz tube reactor. Upon completion of processing, the carrier in the reactor is withdrawn and the table rotates to insert the newly loaded carrier and unload the processed carrier. The wafers are placed faceup in the carrier, which can accommodate 160 wafers.

Films currently characterized are silicon nitride and flat-temperature polysilicon. Future CVD films include low-temperature oxides. The 6000 VTR has also been characterized for oxidations when operating in the diffusion furnace mode.

The 6000 VTR can be installed either in a standalone or through-the-wall configuration. The price of the system ranges from $130,000 to $200,000, depending on the configuration. The first two systems were to be shipped in June.

Electrotech

Electrotech introduced its PLASMAFAB ND8200 plasma-enhanced CVD system for the deposition of silicon nitride, silicon oxide, PSG, and BPSG films. The cassette-to-cassette ND8200 is an improved version

of the ND6200, and it can process wafers up to 200mm. Other improvements were made on the ND8200 to reduce particulates, such as changes in the process chamber and a redesign of the loadlock chamber. Although not a specification, Electrotech's goal on particulates for the ND8200 is less than 0.1 particles larger than 0.5 micron per cm^2.

At a deposition temperature of 300 ^oC, typical deposition rates on a 200mm wafer are 700 angstroms per minute for silicon nitride and 1,070 angstroms per minute for silicon dioxide. Throughput is 30 to 35 wafers per hour for 150mm wafers and 20 to 25 wafers per hour for 200mm wafers.

The ND8200 can be installed in a standalone or through-the-wall configuration. Price of the ND8200 with pumps is $530,000, and first deliveries will begin in the third quarter of 1986.

Plasma-Therm

Plasma-Therm introduced its new plasma-enhanced vertical reactor system for the deposition of silicon nitride, silicon oxide, and silicon oxynitride. It is a fully automatic cassette-to-cassette system with dual-cassette load and unload that can handle 150mm wafers. The vertical reactor has a capacity of 25 wafers per load, and for a 1-micron nitride film, throughput is approximately 25 wafers per hour. Film uniformity is plus/minus 5 percent.

The design of the vertical reactor is such that the plasma electrode and wafer carrier move vertically upward from the reactor for loading and then descend into the reactor for processing. This configuration has the advantage that, when the electrode is in the up position, the entire reactor can be removed from the rear for maintenance or cleaning of the quartz reactor tube. As the reactor can be removed hot, it takes only 1.5 hours to completely swap out reactors and be back to processing.

The system can be installed in either a standalone or through-the-wall configuration. The price of the system is $500,000, and first deliveries will begin in October.

Anicon

Anicon exhibited the Pro-II, an upgraded version of its previous CVD system. The key changes in the Pro-II, which were incorporated to make the system more production-worthy, include a rear-mounted gas panel and a major redoing of the whole control system; the Pro-II now uses an IBM PC AT in lieu of the former control panel. The new control system can be retrofitted to systems in the field. Other features include a guaranteed 90 percent uptime and stainless steel skins.

Anicon also exhibited a standalone Proconix loader to automatically transfer wafers between plastic cassettes and the Anicon quartz boats. However, the quartz boats still have to be manually transferred to/from the loader to the Pro-II. Anicon is working on a true cassette-to-

cassette system using robotics, but it will not be available until January 1987. The Anicon system is the only one of the eleven CVD models discussed in this section that does not have cassette-to-cassette capability.

The Pro-II handles up to 150mm wafers. The base price is $340,000, and first deliveries were to occur in June. The Proconix loader is priced at $100,000.

Machine Technology

MTI exhibited its new single-wafer cassette-to-cassette AfterGlo CVD system, a further development of its downstream plasma technology as used in the AfterGlo Resist Stripper introduced at Semicon Southwest 1985. In the AfterGlo CVD system, the plasma is created by the dissociation of nitrous oxide by microwave energy at 2.45 MHz in a plasma generation chamber that is remote or upstream from the wafer. The excited molecules and dissociated species flow out of the plasma generation chamber to the wafer process chamber located about 12 inches, or downstream, from the plasma generation chamber. The wafers are not immersed in the plasma but are downstream from it. Thus, the wafer is not subjected to high levels of possibly damaging radiation.

A high concentration of reactive species is obtained with the microwave generator, and, consequently, high deposition rates can be obtained. Presently, the system has been characterized for the deposition of silicon dioxide, although the doped oxides and silicon nitride will be characterized in the future. For SiO_2, a deposition rate of 3,500 angstroms per minute can be obtained with a uniformity of plus/minus 2 percent on a 100mm wafer, and the process gas is silane, which is introduced into the wafer process chamber. The wafer can be heated over a range of 175 ^{o}C to 375 ^{o}C, although typically, SiO_2 is deposited at a temperature of 270 ^{o}C.

Another advantage of downstream plasma deposition is the reduction of particulates. In a conventional plasma deposition system the process gas is introduced directly into the plasma chamber, where the gas can combine with the plasma products to produce a "snowing" effect. In downstream systems this effect is minimized as the process gas is introduced downstream from the plasma.

The AfterGlo CVD system can process wafers up to 150mm with throughputs on the order of 20 wafers per hour for a 1-micron film of SiO_2. The AfterGlo is a standalone system that occupies very little floor space (approximately 4 square feet). The price of the system is $250,000, with first deliveries to begin in June 1986.

Genus

Genus focused on process development, such as the new interlayer dielectric (IDL) planarization techniques. In a reactor very similar to its 8402 tungsten reactor, Genus can provide three different topologies

of undoped silicon dioxide for metal line coverage: conformal coverage, 45-degree slope coverage, and full planarization. The two latter topologies can be achieved with only minimal software changes to the system. The bias CVD technique that provides such topologies is based on simultaneous plasma enhanced CVD and argon sputter etch technology.

EPITAXIAL REACTORS

Because of the requirements for epitaxial films for future MOS production, there is great activity in systems development. The perceived product goal is to reduce the cost per epitaxial layer to about 50 percent of the bare wafer cost. With the previous generation of systems, this cost was 3 to 4 times the wafer cost. At Semicon West this year, three vendors introduced their systems. Epsilon, an R&D partnership funded by ASM America, is also developing a system.

Anicon

Anicon's V-EPI System is very similar to its CVD reactor. It employs a quartz isothermal hot-wall chamber within a larger bell jar. The isothermal chamber is resistance heated and the single-pass gas flow coats both sides of the wafer. This combination should produce a stress-free wafer, eliminating slip planes in the epi film.

The wafers are loaded robotically from plastic to quartz boats and the boats are then robotically loaded into the isothermal chamber. The wafer loading is 100 wafers. Anicon claims that the epitaxial layer cost is 25 percent of the wafer cost. The deposition cycle time is typically 2 hours from load to unload. The processing temperature is from 950 ^{o}C to 1,050 ^{o}C at pressures of less than 10 torr. The quartz isothermal chamber must be changed or cleaned after depositing 100 microns of epitaxial films, which would typically be every 8 to 10 cycles. The price of the system is $750,000.

Applied Materials

Applied's new Precision Epi 7010 was introduced for the first time in the United States at the show this year. The system was introduced at Semicon Europa in March. This reactor deviates from Applied's previous radiant heating technology by using an inductively heated susceptor. The heat is also reflected from a gold-coated process chamber to effect the radiant heating of the wafers. This modification allows Applied to cool the process chamber, thus producing a cold-wall process. The cold-wall process reduces the deposition on the process chamber, allowing many more runs before the chamber must be cleaned.

Applied claims that this system's benefits include higher intrinsic resistivity, cleanliness, lower autodoping, and less pattern distortion. The system loading is 27 125mm or 21 150mm wafers. DATAQUEST's epi cost

studies indicate that the cost per wafer is about 35 percent of silicon cost without accounting for yielded wafers. The price of the system is about $1.5 million with a spares package.

Gemini

Gemini had a mock-up of its new system, the Tetron One. (Tetron is a wholly owned subsidiary of Gemini.) The system processes 50 125mm or 150mm wafers per run. The wafers sit in a circular cluster through which single-pass process gas flows. Resistance heaters above and below the wafers produce infrared radiation, which produces an isothermal region at the wafers. This configuration should reduce thermal stress and eliminate slip planes in the epitaxial film. The wafers coat on front and back. Gemini claims throughputs of 40 to 50 150mm wafers per hour. The system is capable of storing up to eight 25-wafer cassettes on the cassette buffer wheel, which presents cassettes to a robot one at a time. The system sells for $1.5 million.

ION IMPLANTATION

Although there were several interesting developments in ion implantation, we will feature high-current systems in this report. In high-current implantation, there is a requirement for high-current implants at low energies. Low energy is desired to dope the shallow junctions that occur in today's VLSI devices. To maintain throughput, the high beam currents must be maintained at low energies; however, beam currents typically fall to a fraction of the currents that are available at high energies.

Three new systems, following Applied Material's introduction of the Precision Implant 9000 in September 1985, were introduced at Semicon West. Applied's system obtains currents of 11mA of boron and 30mA of arsenic and phosphorus at full beam energy of 120 keV and falls to 6mA of boron at 10 keV beam energy. The system sells for $1.9 million.

Eaton/Nova

Eaton introduced its NV-20-200 High Current Implanter. This system doubles the current of the previous NV-10-80 from 10mA to 20mA and increases the available energy from 80 keV to 200 keV. It also employs a new end station that can handle up to 200mm wafers. Eaton claims that the end station can handle 50,000 wafers without operator assistance. It also claims less than 0.03 particulates/cm^2 (greater than 0.5 micron) added per wafer. The beam current available at 10 keV energies falls to about 3mA. The price of the system is $1.2 million.

Nissin Electric Co. Ltd.

Mitsubishi International has introduced Nissin's new PR-80 High Current Implanter. Mitsubishi will market the system in the United States. The system has effective beam energies from 30 keV to 200 keV. The maximum current at full energy is 5mA of boron and 13mA of phosphorus on the target. The beam current for boron falls to 2mA at 10 keV beam energy and rises to full beam current above 40 keV. Nissin has produced ion implanters since 1971 and is featuring high reliability as a major benefit. The price of the system is $900,000 to $1 million, depending on the spares package.

Varian/Extrion Division

Varian introduced three new high-current implanters: the 80 XP, the 120 XP, and the 160 XP. The number part of the model number refers to beam energies for singly charged ions. These systems can handle wafers from 100mm to 200mm in a dual-end station. The improvements over the previous design include better particulate control and higher currents at low energies. The boron beam current falls to about 2mA at 10 keV beam energy, which is a factor of two improvement over the previous model 120-10. The price of the system is about $1.5 million.

Veeco

Veeco introduced a solid boron source that eliminates the necessity for bottled gas for implantation. The boron source is $LiBF_4$, which decomposes into BF_4 as a by-product when heated.

RAPID THERMAL PROCESSING

Semicon West witnessed the introduction of several new machines in the area of rapid thermal processing (RTP) as this market begins to emerge from its embryonic stage to a market that will be characterized by high growth rates. Varian and AG Associates introduced new models, Peak Systems introduced its first product, and Thermco introduced its Japanese-made RTP. Only Eaton, of the companies involved in the U.S. market for RTP, failed to introduce new features for its RTP. Prior to Semicon, only AG Associates had been a significant player in this emerging market. However, with more players and process equipment better suited to the requirements of the market, the RTP market should prove to be very interesting as it moves into a high-growth mode.

Varian

Varian introduced its RTP 8000 rapid thermal processor. The RTP 8000 is a fully automated cassette-to-cassette system that can handle wafers up to 200mm at a maximum mechanical transfer rate of 300 wafers per hour. The load and unload stations each use a robotic arm that can

accommodate dual cassettes. Operating range is 400 °C to 1,400 °C. The heat source is an upper bank of 18 tungsten lamps with a gold-plated reflective system for uniform wafer heating. The light source is sealed from the process chamber with a quartz window.

The wafer is placed on three quartz pins and the wafer temperature is monitored from the backside with an infrared pyrometer located beneath the wafer. The process chamber can be purged with gases. The system, which uses touch-screen control with a full alphanumeric keyboard, can be installed in a through-the-wall configuration. It is priced at $185,000 and first deliveries will begin in the fourth quarter of 1986.

Varian also has available the RTP 800 rapid thermal processor that was introduced at Semicon Japan in 1985. The RTP 800 is a manual version of the RTP 8000 and is intended for R&D applications. However, the light source and process chamber are identical for the two models, so the process characteristics would be the same. The RTP 800 is priced at $75,000 and several units have been installed in the field.

Peak Systems

Peak, a venture capital-backed start-up company established in 1983, introduced its first product, the ALP 6000 rapid thermal processor. The ALP 6000 is a fully automatic system capable of handling wafers up to 200mm at wafer throughputs of more than 240 wafers per hour. The load and unload stations each use a robotic arm that accommodates dual cassettes. The temperature range of the system is 400 °C to 1,300 °C, and the temperature ramp rate can be programmed up to 250 °C per second.

The heart of the ALP 6000 is the new Peak-developed SP35X "silicon specific" long-arc, AC, gas discharge lamp using a proprietary mixture of gases to make the spectral output of the lamp closely match the absorption characteristics of silicon. Peak claims that 70 percent of the spectral output of the lamp is absorbed by the wafer, more than five times that from conventional tungsten halogen lamps. An advantage of this lamp over tungsten halogen lamps is that, because of the spectral output of the lamp, free carrier absorption is eliminated, thus, providing repeatable time-temperature profiles regardless of varying dopant concentrations or defect conditions. Also, the gas discharge lamp has a zero thermal mass, in contrast with tungsten lamps that employ filaments. Thus, Peak claims, better process control and faster wafer thermal response profiles can be obtained with this lamp. The lamp, constructed of two concentric cylinders with the inner cylinder for water cooling, is rated at 35kW.

The light source is separated from the process chamber by a quartz window. The wafer is placed on quartz pins and the temperature of the wafer is monitored from the backside by an optical pyrometer located beneath the wafer. The sealed process chamber can be purged with process gases.

The operator interface is a membrane panel or an optional alpha-numeric keyboard. The system uses 3.5-inch microfloppies for operating system storage as well as data logging or archival storage.

The price of the system is $175,000, with first deliveries to begin in July. DATAQUEST believes that Peak presently has beta-site installations at National and Intel.

Thermco

Thermco made its U.S. introduction of the LA-14AD thermal processor. This system is manufactured by TEL/Thermco in Japan and will be marketed by Thermco in the United States. This system features a bank of seven tungsten halogen lamps above the wafer and another bank of seven below the wafer. In addition to these lamps, the wafer is placed on a circular quartz halogen lamp. This latter lamp supports the wafer, is the same size as the wafer, and is intended to increase wafer temperature uniformity.

The LA-14AD will provide heat rates of up to 180 ^{o}C per second and cool-down rates of 50 ^{o}C per second for up to 150mm wafers. The automatic load and unload stations will each accommodate a single cassette.

The LA-14AD is a second-generation TEL/Thermco system, and Thermco says that 20 systems have already been sold in Japan. Thermco also says that the predecessor of the LA-14AD also used tungsten halogen lamps and that 100 systems have been installed in Japan. The U.S. price of the LA-14AD is $200,000.

AG Associates

AG introduced the Heatpulse 2146 rapid thermal processor as a further development of its Heatpulse 2101 and 2106 RTP product line. The 2146 is targeted at the thin-gate oxidation market. It has basically the same wafer-handling system and lamp source as the Heatpulse 2101 and 2106 but is optimized to handle corrosive and noncorrosive gases in the process chamber.

Specifically, the 2146 can handle six process gases, including argon, nitrogen, oxygen, forming gas, ammonia, and hydrogen chloride. Although the 2101/2106 models could handle up to four noncorrosive gases, they did not have the sophisticated gas-control software and hardware available on the 2146. The 2146 can process multistep cycles in which a single wafer can be oxidized, nitridized, and annealed without removing it from the process chamber. The required gases for each step of the multistep process are automatically programmable.

Like the 2101 (125mm wafers) and 2106 (150mm wafers), the 2146 uses top and bottom banks of 11 tungsten halogen lamps for a total of 22 lamps. The steady-state temperature range is 700 ^{o}C to 1,220 ^{o}C, and the heating rate can vary up to 220 ^{o}C per second. An optical pyrometer is used to monitor the backside wafer temperature. The load

and unload stations each handle a single cassette with wafers up to 150mm. Throughput, which is process dependent, can be up to 60 wafers per hour.

The price of the 2146 is $185,000 (the 2106 sells for $126,000). Deliveries of the 2146 began in April, and there are, to date, four or five units in the field.

Eaton

Although Eaton did not introduce any new features on its ROA-400 rapid thermal processor, it is mentioned here to complete the discussion of companies offering RTP machines in the United States. The ROA-400 uses as a heat source a water-wall, DC argon arc lamp originally developed by the Canadian government for outdoor, nighttime illumination. The lamp is rated at 100kW.

The ROA-400 is a fully automatic, cassette-to-cassette (single-cassette load/unload) system that can process 150mm wafers at throughputs up to 350 wafers per hour for a typical postimplant anneal. The temperature range is 450 ^{o}C to 1,400 ^{o}C, and temperature is monitored with an infrared pyrometer. The wafer is placed on quartz pins in the process chamber, which can be purged with four different noncorrosive gases.

The first version of the ROA-400 was introduced in 1982, and DATAQUEST estimates that approximately 15 units are in the field. DATAQUEST believes that slow sales for this unit were due to its very large footprint and its high price of $250,000 (versus about $100,000 for competitive machines). However, the new models introduced at Semicon this year were in the range of $175,000 to $200,000, so possibly the higher price of the ROA-400 may not be a key issue now.

DIFFUSION FURNACES

Every diffusion furnace vendor visited by DATAQUEST had some form of cassette-to-cassette wafer-handling capability. Other features included smaller footprints, modularity, and throughput.

Reid-Ashman/ACS

Reid-Ashman's recently acquired ACS displayed its Falcon series of horizontal furnaces. One interesting new feature of the Falcon series is that it is modular and expandable. A customer can purchase one or two tubes initially and then later add more tubes vertically as the need arises.

ACS has carried the concept of modularity beyond the tube itself to the gas-control cabinet of the furnace and also to the gas pumps. In its gas-control cabinets, mass flow controllers, mechanically operated valves, and their interconnections are laid out on vertical planes rather

than on a horizontal plane. This is claimed to be advantageous for maintenance and for purging noxious gases, since a vertical plane eliminates "pancake" layers in which pockets of gases could be trapped. Pumps for the Falcon system are also modular and can be located remotely.

The Falcon system also features a retractable, soft-land/loader mechanism that retracts from the tube during deposition. This is claimed to have three advantages: the loader does not obstruct gas flows, it eliminates thermal loading (absorption of heat by the loader), and the loader does not get dirtied by deposition. The Falcon also features a new automatic Direct Digital Control (DDC), which, after the operator pushes the start button, loads the wafers, monitors all the parameters, starts the process, shuts it off, and removes the wafers.

BTU/Bruce

BTU/Bruce's horizontal furnace featured an automated transfer/loading station. However, the software for the transfer/loading station will not be fully developed until this summer.

Semitherm

Semitherm introduced the Advantage 801. The 801 is a vertical thermal processor that features a heater element that can be raised and lowered and a process chamber that also can be raised and lowered inside and independently of the heater. The advantages of this configuration claimed by Semitherm are that uncontrolled reactions caused by backstreaming are eliminated. The Advantage 801 also features a Black Max by Thermtec as a furnace element. Semitherm claims that it can ramp a load of wafers faster than any system available because of the low-mass heater wire and double furnace/process bell jar lift features. The Advantage 801 can work with cassette-to-cassette and integrated process islands.

Silicon Valley Group (SVG)

SVG introduced a vertical furnace, the SVG 6000 VTR, for diffusion and LPCVD. The 6000 VTR features automatic wafer handling with direct loading into the quartz boat from cassettes. It has a small footprint and, reportedly, can handle up to 160 150mm wafers per hour.

Tempress

Tempress' Model 2000 Vertical Integrated Processor featured an autoloader/unloader with bottom-up loading that Tempress claims minimizes contamination and heat loss. The 2000 also features a closed, retort-type chamber that uses 20 percent to 30 percent less process gas per run. The 2000 uses only 50 percent as much energy to operate at the same temperature as a horizontal furnace.

Thermco

Thermco introduced an automated load station that uses two elevators to handle plastic and quartz. Wafers are loaded into the system by means of four input/output drawers that extend from the end of the load station. All quartz and plastic cassettes are stored within WIP areas internal to the systems. Wafer loading and unloading to the diffusion furnaces is done with Atmoscan-controlled atmospheric loaders and silicon carbide paddles.

Tylan

Tylan's horizontal furnace features a significantly smaller footprint for a horizontal furnace (60 square feet). Tylan claims that this is smaller by a third than most horizontal furnaces. Tylan is able to achieve this by shortening the length of its tube. It can do this because it has quartz-wool end plugs at each end of the tube that add insulation and thus reduce heat loss. This gives the tube better control over temperature and allows the coils to be put closer together and thus make a shorter tube.

PHYSICAL VAPOR DEPOSITION

In the PVD segment, most of the new product announcements and equipment upgrades were related to automated, cassette-to-cassette, magnetron sputtering equipment. At Temescal, however, several evaporator models were converted to through-the-wall machines. The equipment listed in this section is volume production equipment. This equipment has been announced since Semicon West 85.

Varian

Varian's new 3290 is a fourth-generation product from Varian's 3180 family. This product line has been the workhorse for Varian. The company claims to have sold 500 systems since the introduction of the 3180 five years ago. The 3290 is a vertical, single-wafer processing machine that the company claims can process 125mm or 150mm wafers at a throughput of 45 wafers per hour. Now equipped with three targets, the 3290 allows for 50 percent more uptime between target changes. It also features a new combined preheat and sputter etch station. This station allows for simultaneous heating and sputter etching of silicon substrates to desorb volatile contaminants before metal deposition. This is part of the Vacuum Isolated Process Station (VIPS) that contains and pumps away desorbed gases at the preheat/etch station. The new VIPS feature can be retrofitted to the Varian 3180, 3190, and 3280. The average selling price for the new 3290 will be $650,000, depending on the options selected.

The XM-8, which is based on the recently acquired GARTEK system, is designed primarily for gallium arsenide and backside metallization. The system is capable of sequential deposition of up to four materials with

no cross talk. It also features plasma shields for precious metal recapture capability. The XM-8 is a horizontal, single-wafer process machine. Three-inch to 150mm wafers can be processed at a claimed throughput of 40 wafers per hour. The system's gentle wafer-handling system contributes to high yields for deposition on fragile gallium arsenide or backlapped silicon substrates. The system is also said to be reliable for two-layer interconnection, bump fab applications for tape automated bonding, deposition of precious metals, and hybrid circuit metallization. The average selling price of the Varian XM-8 is in the range of $350,000.

Perkin-Elmer

The new Perkin-Elmer 8880 is basically a 4400 series machine with a cassette-to-cassette loadlock and an Intel 310 microcomputer terminal added on. It features 100mm, 125mm, and 150mm wafer-handling capability, along with power to the table. The 8880 uses four targets in one chamber and allows alloy mixture changes on-site by adjustment rather than replacing the target(s). The machine uses a rotary cage and holds the wafers vertically. Step coverage is claimed to be 50 percent. The average selling price for the 8880 is $300,000.

Materials Research Corporation (MRC)

MRC's new product, the Eclipse, is its latest through-the-wall product for sputtering. Available with either two or three targets, the Eclipse is equipped with four or five fully isolated chambers. The three-target model comes with one loadlock chamber, one sputter etch chamber, and three deposition chambers. The two-target model is the same as the three-target system except that it does not have the third deposition chamber. The chambers of both systems are equipped with individual cryopumps for process flexibility. The independent chambers have the advantages of quicker pump-down times (one hour), no cross contamination, the ability to vent chambers individually, 15-minute target changes, and the ability to have a different gas flow/pressure within each chamber. The Eclipse can be set up to run 125mm, 150mm, or 200mm wafers using a vertical, single-wafer process. Throughput is claimed to be 60 wafers per hour depositing 1-micron aluminum. Step coverage is said to be greater than 40 percent at a 1 x 1-micron step. The average selling price of the system is $1 million.

Ulvac

Ulvac's new MCH-9000 is now available in the United States for the first time. Forty units are said to have been delivered worldwide--two-thirds of them in Japan. The MCH-9000 features six separate chambers with vacuum provided by six cryopumps. Each chamber is connected by a minimum slit that can be monitored by an optional slit valve, thus providing total isolation of each chamber. The chambers, in process order, are loading, etch-cleaning, first sputtering, second sputtering, third sputtering, and unloading.

There is only one target in each chamber, which eliminates target cross contamination. In the chamber, the number of contaminating particles larger than 0.5 micron on a 125mm wafer is claimed to be less than 10. The machine is capable of handling 125mm, 150mm, or 200mm wafers at a throughput of 35 wafers per hour when doing advanced applications of metal such as aluminum, titanium, and titanium nitride for 1Mb DRAMs. When applying a much simpler aluminum-silicon film, throughput is claimed to be around 65 wafers per hour. Step coverage of a 1 x 1-micron step is said to be approximately 30 percent using no bias. Bias is claimed to enhance step coverage but also develop a less satisfactory metal layer. The system processes single wafers horizontally and has been developed primarily for advanced applications of metals for products such as the 1Mb and 4Mb DRAMs. The average selling price for the MCH-9000 is $800,000.

Balzers

The new Balzers 900 (based on the 801) is a through-the-wall, cassette-to-cassette, rotary cage, vertical sputtering machine. Equipment availability is slated for 1987. The 900 can be set up to handle 125mm, 150mm, or 200mm wafers. Throughput is said to be 70 wafers (150mm) per hour at a sputter deposition of 1-micron. Step coverage capability is said to be between 40 percent and 50 percent. The 900 has two isolated chambers, one loadlock chamber, and a sputter/etch chamber. The substrates remain in their vertical position during the trip from the cassette to the process chamber. The 900 uses two targets for cosputtering and will sell for $750,000 to $900,000.

Temescal

Temescal introduced three new through-the-wall evaporation machines. The machines have been turned up on their sides and have square doors, which replace the bell jars on previous machines. Also new is the user-friendly, touch-screen CRTs. Only the door and the CRT is left in the clean room.

The VES 2000 and FCE 2000 are through-the-wall versions of the BJD 1800 and FC 1800. The 2000 series machines are primarily used in GaAs fabs for lift-off processing. Both machines handle up to 3-inch wafers and can hold 75 wafers when set up for planetary motion. Capacity goes down when a 90-degree angle of incidence is used for lift-off techniques. Both evaporators use 20-inch, cube-shaped boxes.

The VES 3000 is the through-the-wall version of the DES 2550 and is designed to handle up to 150mm wafers. Capacity, when set up for planetary motion, is 51 100mm, 36 125mm, and 15 150mm wafers. Again, the capacity will decrease if lift-off techniques are used. The 3000 uses a 32-inch, cube-shaped box. The average selling price for all the through-the-wall machines is $300,000 to $350,000.

AUTOMATION

There were numerous participants active in the semiconductor automation arena at Semicon West this year, with new products and support announcements coming from the manufacturers of CIM (computer-integrated manufacturing) packages, material handling and robotics companies, and a facilities construction firm. This section covers highlights and product announcements from Consilium, PROMIS Systems, Qronos Technology, Asyst Technologies, Flexible Manufacturing Systems, Veeco Integrated Automation, and Bechtel/Varian.

CIM Manufacturers

Consilium

Consilium, a major supplier of CIM software systems to the semiconductor industry, demonstrated a new equipment interface to BTU Engineering Corporation's furnace equipment. The equipment interface consists of a software link that provides communications capability between the BTU furnace and Consilium's COMETS (Comprehensive Online Manufacturing and Engineering Tracking System) software package. The COMETS package is designed to run on VAX and MicroVAX hardware available from Digitial Equipment Corporation. Consilium has provided the COMETS integrated software system for factory automation to more than 49 semiconductor manufacturers.

The BTU furnace interface joins the growing list of equipment interfaces that are currently available from Consilium. The list of equipment interfaces includes diffusion furnaces (BTU FACS, Thermco TMX 9001, and Tylan), ion implantation (Varian), automatic guided vehicles (both Veeco's V2 and V3), and six interfaces to metrology tools (Leitz MPV/CD, Nanoline II, Nanoline IV, Nanoline V, Nanospec AFT180, and OSI VLS-1). In addition, the Consilium/BTU equipment interface also supports communications between Gasonics' HiPOx (high-pressure oxidation) furnace and the COMETS package.

PROMIS Systems

PROMIS Systems, the wholly owned subsidiary of I.P. Sharp Associates, of Canada, announced the availability of its PROMIS software for semiconductor manufacturing automation on IBM computers, specifically IBM's System/370 architecture. The PROMIS (PROcess Management and Information System) software package previously had been available only on VAX and MicroVAX II hardware. The availability of PROMIS on IBM computers will allow those manufacturers with existing IBM mainframes to tie directly to the PROMIS package. In addition, some smaller manufacturers that may need to expand to IBM hardware systems for future computing needs will be able to preserve the PROMIS package for factory automation.

Current PROMIS customers include AT&T, General Electric, IBM, LSI Logic, Polaroid, Rockwell International, Siliconix, Silicon Systems, and Texas Instruments. In addition, Tokyo Electron Limited (TEL), the sales

and support arm for PROMIS Systems in Japan, is near closing its first order for the PROMIS package from a Japanese semiconductor manufacturer.

Qronos Technology

Qronos Technology announced the first in its family of products for CIM. The new product offering, known as HEADSTART, is a software package that combines application programs and software development tools (including security, help, and calendar functions) to facilitate application programming on the IBM System/88. The HEADSTART product has generic applications for numerous industries that rely on continuous, 24-hour-a-day operations, such as semiconductor and chemical manufacturing and financial institutions.

The entire Qronos Advantage family of products is being designed to run on, but will not be limited to, the IBM System/88 and System/370 architectures. Gi Schaefer, product manager for factory automation at Qronos, stated that Qronos regards the IBM System/88 as "the most efficient, cost-effective approach to nonstop computing available to the semiconductor industry today."

The Qronos Advantage product line is designed on a modular basis, similar to other CIM software packages. The chief product in the Qronos family is known as the Qronos Connection, which is a proprietary software program that enables the user to access and move data base information between the IBM System/88 and other hardware systems, such as Digital and Hewlett-Packard computers. The Qronos Connection thus will allow users to connect a wide variety of computing and application software modules together to obtain a synergistic use of resources. This, in turn, would allow users to preserve existing CIM software implementations on non-IBM hardware and at the same time provides a pathway of options for future CIM system applications. The Qronos Connection is still under development but is expected to be released in the first half of 1987.

Material Handling and Robotics

Asyst Technologies

Asyst Technologies announced two new products that complement its SMIF (Standard Mechanical Interface) family of automated particle-control products. The new SMART-Traveler system represents an alternative to the traditional use of paper traveler logs that accompany wafer lots throughout the processing sequence. The SMART-Traveler is available in two configurations, but central to either configuration is the SMART-Tag, a memory device that contains routing information, processing specifications, history, and lot status. A 16-character LCD display on the SMART-Tag identifies lot number, successive processing steps, and processing equipment identity.

The second new product is the ARM-2000, a robotic wafer-transfer mechanism. This product has been specifically designed for OEM applications and, as such, provides a fully automated robotic transfer system

on semiconductor processing equipment to allow particle-free loading and unloading of wafer cassettes from SMIF carrier boxes (SMIF-Pods). The ARM-2000 is also available to users that are incorporating SMIF products in their manufacturing facilities.

In addition to the new product announcements from Asyst, six models of processing equipment that have been integrated with Asyst-SMIF products were on display at the show this year. Equipment-SMIF compatibility was demonstrated by automatic photoresist processing equipment manufactured by Eaton, Silicon Valley Group, and Solitec, by wafer inspection systems manufactured by Nikon Instruments and ROBOP-TEK, and by Semifab's automated wet processing station.

Flexible Manufacturing Systems

Flexible Manufacturing Systems (FMS) had the full line of products of its Computer Integrated Manufacturing System on display this year, including its Mobile Transport Unit (MTU), Docking Module (DM), Tool Interface (TI), Central Control Computer (CCC), and Intelligent Work In Process (WIP) Station. FMS currently has one system installed at AT&T in Orlando, Florida, and a second system will be going to the AT&T Kansas City facility later this year.

In a recent press release (June 26), FMS announced an agreement with Nippon Kogaku K.K. (Nikon), of Japan, under which Nikon will market FMS' automation systems in Japan and Pacific Rim countries. The first system will be delivered to Nikon in September.

Veeco Integrated Automation Inc.

Veeco, a major manufacturer of automatic guided vehicles and material transfer and storage systems for the semiconductor industry, has taken an innovative approach to the issue of processing equipment and robotic compatibility in an automated manufacturing environment. This year at the show, Veeco provided equipment manufacturers with a new document that specifies the physical and communications requirements for successful interactions between processing equipment, CIM host computer system, and the Veeco automation systems.

The "Semiconductor Process Equipment Interface Specification" document, authored by Carl Fiorletta, vice president and general manager of Veeco Integrated Automation Inc., outlines the elements necessary to ensure that adequate provisions have been made for communications compatibility between equipment and CIM host, as well as for physical compatibility between equipment and the Veeco mobile robotic system. For example, Veeco has developed custom SECS (SEMI Equipment Communications Standard) messages to support material distribution and emphasizes that processing equipment must be able to detect the presence of a cassette and determine whether it is full or empty. Veeco has made the specifications document available to semiconductor manufacturers to be included as a purchasing specification and requirement to equipment manufacturers so that equipment and robotics will be compatible on the shop floor.

Veeco expects the installed base of its V3000 AGV system to grow to nine units by the end of 1986. Existing installations include Thomson Components-Mostek Corporation (Carrollton, Texas), Siemens (West Germany), and Fairchild (Portland, Maine), with additional units going to Philips (Netherlands), RCA/Sharp (Camas, Washington), Siemens (West Germany), and three additional semiconductor manufacturers, whose identities are still confidential at this time.

Facilities Construction

In August 1985, the Bechtel Group and Varian Associates announced a corporate agreement to offer an inclusive package to semiconductor manufacturers for the design, construction, and equipping of state-of-the-art fabrication facilities. At the Semicon show this year, representatives from Bechtel National, one of the Bechtel companies, were on hand to describe the Bechtel/Varian team approach to providing integrated services to the semiconductor industry. Historically, the fab facility and its equipment and processing requirements have been managed as separate entities. Bechtel/Varian's view is that as the semiconductor industry adopts a strategy for automation of its fab facilities, this conventional approach to planning, construction, and procurement will no longer adequately meet the stringent requirements necessary for a sophisticated, automated wafer fabrication environment.

The combined expertise of Bechtel, one of the world's largest engineering and construction firms, and Varian Associates, a major international manufacturer of semiconductor processing equipment, will provide semiconductor manufacturers with a state-of-the-art facility built and equipped to order by a single firm. This novel approach to a truly integrated manufacturing facility will warrant attention in the months ahead as new fabs are being planned for the automated manufacturing environment of the future.

George Burns
Joe Grenier
Robert McGeary
Mark Reagan
Peggy Wood

a company of The Dun & Bradstreet Corporation

NEWSLETTER

SEMS Code: Newsletters 1985-1986, July 1986
1986-8

A VISIT TO THE CANON ALIGNER FACTORY UTSUNOMIYA, JAPAN

Dataquest recently had an opportunity to visit the new Canon aligner factory at Utsunomiya, Japan. This newsletter is a report on that visit.

CANON BACKGROUND

First, some background information on Canon may be helpful. Canon, whose total sales were $4.05 billion in 1985 (based on ¥237 per dollar), is organized into three main product groups: Camera Operations, Business Machine Operations, and the Optical Products Group. Together these three groups account for 98 percent of total Canon sales.

Camera Operations includes hand-held cameras, video camera-recorders, and the just-introduced Color Electronic Still Camera, which looks and feels like a 35mm SLR camera, but records video images as electronic data on magnetic floppy disks. Camera Operations accounted for 20 percent of Canon sales in 1985.

Business Machine Operations, which accounted for 71 percent of total 1985 sales, includes copiers, laser beam and ink jet printers, electronic typewriters, calculators, facsimile transceivers, and microcomputers. The Optical Products Group accounted for 7 percent of Canon's sales and includes semiconductor equipment, medical X-ray equipment, retinal cameras, and lenses for television broadcasting.

Semiconductor equipment manufactured by the Optical Products Group includes contact/proximity, projection, and reduction stepper mask aligners; coater/developer (track) equipment; epitaxial spike crushers; laser-scanning flatness testers; photoresist ashers; and mask/reticle scrubbers. Aligners are by far the major products; the others contribute relatively little to the total semiconductor equipment revenue. Only the aligners, coater/developers, and flatness testers are exported.

The Optical Products Group has two main factories: one at Kosugi and the other at Utsunomiya. The Kosugi factory produces most of the group's products other than mask aligners, which were manufactured at Kosugi before the Utsunomiya factory became operational. Kosugi is also where the main semiconductor equipment R&D is done, although a small portion of R&D is done at Utsunomiya. The Utsunomiya factory is currently dedicated solely to the production of Canon contact/proximity, projection, and reduction stepper mask aligners.

UTSUNOMIYA--AN EMERGING TECHNOPOLIS

Utsunomiya City, about one hour north of Tokyo by bullet train, has been selected by Japan's Ministry of International Trade and Industry (MITI) as one of the 19 candidate technopolis sites throughout Japan. MITI announced the Technopolis Concept in 1980; it is a plan to build a network of high-technology cities linked to Tokyo by bullet trains, airports, and communications systems.

Several high-technology companies have built, or are in the processing of building, new facilities at Utsunomiya, including Tokyo Ohka, the leading photoresist manufacturer in Japan; Sumitomo Bakelite (IC molding materials); Mitsui Toyo (measuring equipment); and Monsanto, which is building a silicon wafer factory with a planned ultimate investment of $100 million. Directly across the street from Canon's mask aligner factory is the vast Canon factory built in 1977 for the production of camera lenses and other optical products (but not aligner optics).

THE CANON UTSUNOMIYA ALIGNER FACTORY

Canon's Utsunomiya mask aligner factory was built in 1983, and production of the PLA and MPA series of contact/proximity and projection aligners began in March 1984. Production of the FPA reduction stepper began in December 1984. All of Canon's aligners are now produced at this factory. The factory occupies a floor space of 412,000 square feet, although not all of this space is under use; the unused space is for future expansion. Dataquest believes that this is the largest aligner factory in the world and can be compared with GCA's Andover facility, which has a floor space of approximately 300,000 square feet. Nikon actually has more stepper capacity than Canon, but manufactures at two separate facilities.

Total employees number approximately 556 as shown in Table 1. Although not directly related to this newsletter, Dataquest thought the information in Table 1 interesting from a cultural point of view.

Table 1

UTSUNOMIYA FACTORY PERSONNEL

	Male	Female
Number	477	79
Average Age (years)	27.7	21.6
Average Service Length (years)	6.4	1.2

Source: Canon

Canon's Utsunomiya aligner factory consists of four buildings and includes a machine shop, an optics shop, and aligner assembly and test. The machine shop produces 40 percent of the parts for the aligners, not including the x-y stage, which is produced at another Canon factory (Ami). The machine shop is almost fully computerized and numerical control (NC) machines were in abundance; there appeared to be only a few manual machines. A flexible manufacturing system, using NC machines and automatic guided vehicles (AGVs), was installed in one area of the shop. The AGVs transfer raw material from floor-to-ceiling stockers to the NC machines for machining, and back to another set of stockers after machining. No machine operators are required in this area, and the area is capable of running unattended around the clock.

Immediately upon entering the Utsunomiya facility, visitors are asked to remove their shoes and don slippers. Slippers were worn on the walk through the machine shop as well, and it is to be noted that the shop floor was gleaming and absolutely spotless. In fact, the whole shop was incredibly clean, well beyond expectations.

All of the optics for the aligners are fabricated at Utsunomiya including grinding, coating, and assembly operations. This includes the smaller optics used in the aligners as well as the large mirror used in the projection aligner and the refractive 0.35 and 0.43 numerical aperture lenses used in the FPA-1550 and FPA-1550 MII steppers. Final assembly of the stepper lens is done under computer control using a laser alignment system. Time to manufacture a stepper lens is about five months, and Canon's goal is to cut this time in half.

The projection and stepper aligners are assembled in an open Class 10,000 area. In order to enter this area, a visitor must first don a clean room garment and cap and pass through an air shower tunnel. Stepper assembly takes about two weeks. After assembly, the steppers are transferred to an adjacent area for test and adjustment. This area consists of 36 individual enclosed bays that have cleanliness better than Class 1000. Each stepper spends about two months in the bay undergoing final test. Dataquest noted that there were 20 to 25 steppers in the bays. It is not clear to Dataquest if these same bays are used for projection aligners or if they undergo final test in another area.

Near the final test area is a coater/developer lab for the coating, developing, and evaluation of test wafers from the machines undergoing final test. Canon coater/developers were used in the lab.

Altogether it takes about five months to produce a stepper, including two months for parts production (not including the stepper lens), two weeks for assembly, and two months for final test and adjustment. Four months are required to produce a projection aligner, and three months for a contact/proximity aligner. Contact/proximity aligners are assembled and tested in a separate area from the projection and stepper area.

Canon said that the stepper capacity was 300 units per year. However, assuming two months in final test and 36 bays, this projects to about 216 units per year. Apparently, Canon has room for expansion of the final test area if production of 300 units per year is required. In 1984, a boom year for the semiconductor equipment industry, the Canon Utsunomiya factory produced 300 projection and 400 contact/proximity aligners. Since Dataquest is forecasting low growth for the latter two aligner markets due to the emergence of all-stepper semiconductor fabrication, we foresee that the production capacity attained in 1984 should be sufficient for future needs.

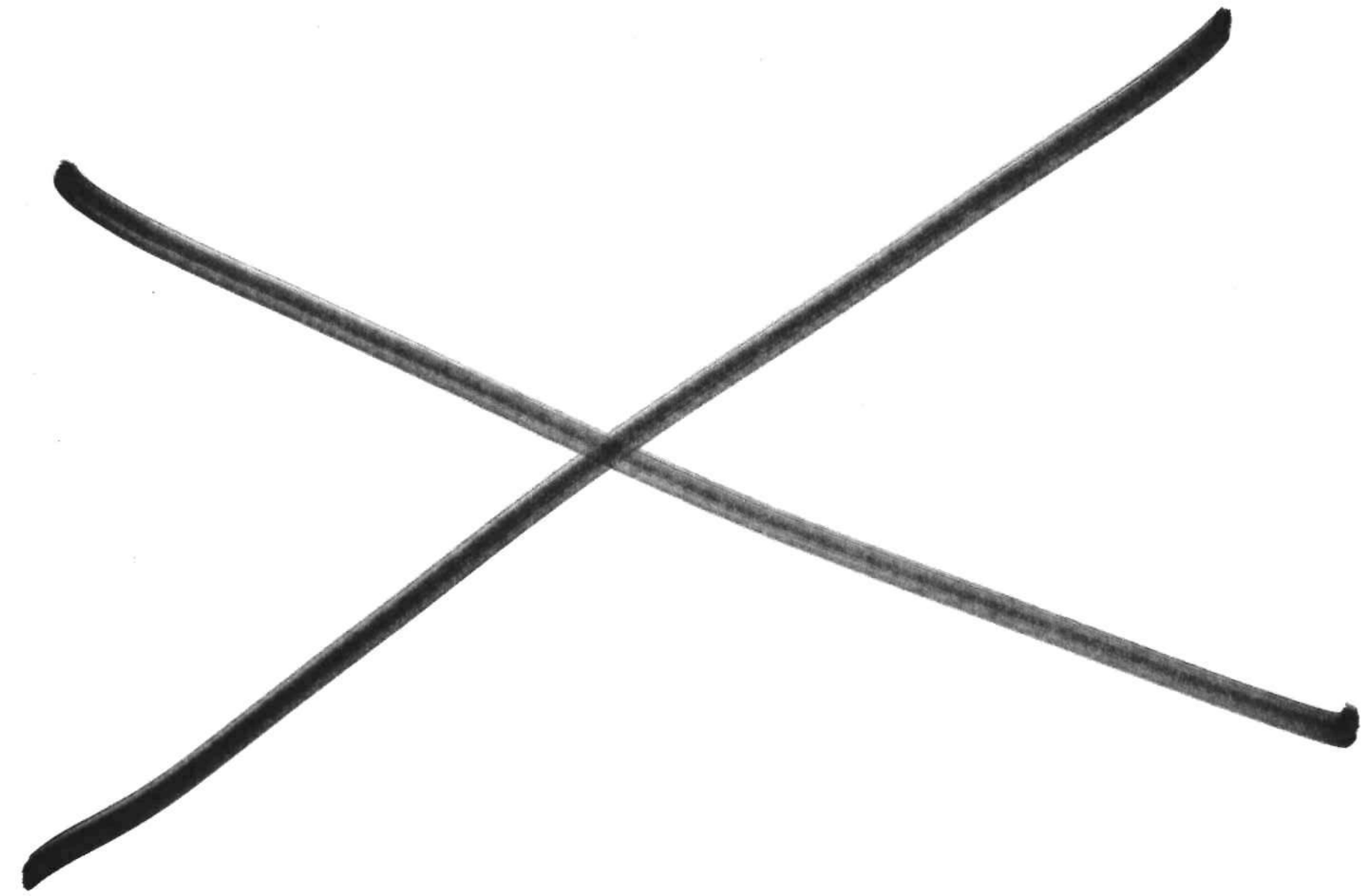
DATAQUEST CONCLUSIONS

Impressions of the factory include words like cleanliness, organization, efficiency, quietness, and productivity. Regarding productivity, although it is not clear what level of employment is required for full capacity, it does appear that the average productivity in terms of sales per employee of a Canon Utsunomiya factory worker is high.

The low growth of the contact/proximity and projection aligner markets should also indicate that Canon will become aggressive in the stepper market in order to offset its lower growth rate for sales in these areas. In addition, Canon has a huge factory to fill, and we expect that Canon will be aggressive in the marketplace in order to keep production up at Utsunomiya.

(Note: For further information on MITI's Technopolis Concept, see the new book entitled The Technopolis Strategy, Japan, High Technology, and the Control of the 21st Century by Dataquest's Sheridan Tatsuno.)

Joseph Grenier



August Newsletters

The following is a list of material found in this section:

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: Newsletters: 1985-1986
1986-9

THE GALLIUM ARSENIDE MATERIAL INDUSTRY: A PLETHORA OF PLAYERS

SUMMARY

Gallium arsenide (GaAs), a III-V compound semiconductor material, is presently the most widely used substrate for device applications requiring high-speed, high-temperature operation and radiation hardness. A plethora of players has entered the gallium arsenide material market over the last few years in expectation of substantial development and rapid growth in the gallium arsenide device market. In a recent analysis, Dataquest identified 34 manufacturers of gallium arsenide and other compound semiconductor materials in the worldwide market with 19 companies in the United States (including two firms in Canada), 11 in Japan, and 4 in Europe. Manufacturing activities include production of polycrystalline material, single-crystal ingots, and wafers, and growth of epitaxial films.

Sumitomo Electric in Japan is acknowledged as the world market leader with an estimated share of approximately 50 percent. Dataquest believes that due to the number of players in this arena and the relative strength of Sumitomo Electric's position, GaAs material companies will become increasingly aggressive in their attempts to establish a significant presence in this market.

This newsletter contains an overview of the gallium arsenide and compound semiconductor material manufacturers in the free world. This information has been compiled from company literature and recent trade press announcements. We believe that the number and type of companies active in gallium arsenide and compound semiconductor materials are of significant importance to our clients. Dataquest is following both the gallium arsenide material and device markets through our Semiconductor Equipment and Materials Service and the upcoming Gallium Arsenide Industry Analysis, respectively.

COMPOUND SEMICONDUCTOR MATERIALS

Gallium arsenide is just one of many substrates classified as a compound semiconductor material. These materials are identified by number designations, III-V and II-VI, which identify the number of outer shell electrons of the respective atoms that constitute the compound semiconductor material. Besides GaAs, other common III-V materials include gallium antimonide (GaSb), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), and indium phosphide (InP). Examples of II-VI substrates include cadmium telluride (CdTe), mercuric telluride (HgTe), and cadmium mercuric telluride (CdHgTe). Because commercial silicon technology is not presently capable of yielding production circuits operable above 10 GHz, GaAs is the substrate of choice for ultrahigh-speed ICs.

Starting Materials

Gallium does not occur in nature as a pure material. Economically recoverable deposits of gallium occur in bauxite and zinc ores, and gallium is typically refined as a by-product of aluminum or zinc recovery. It is believed that the earth's reserve of gallium is 110 million kilograms; the free world demand approximates 20,000 kilograms per year. Arsenic, an extremely toxic element, is found to a small extent as a pure material in nature, as well as in ores of antimony, silver, and in many sulfides. Arsenic has been designated as a carcinogen and its usage is carefully controlled by government health agencies.

Major suppliers of gallium in the free world include Alusuisse of Switzerland, purchased in 1985 by Alcan Aluminum (Montreal, Canada); Dowa Mining in Japan; Ingal, a joint venture between the Billiton subsidiary of Royal Dutch Shell of the Netherlands and aluminum producer VAW of West Germany; Musto Explorations (Canada), owners of the Apex mine in Utah, a major source of gallium and germanium in the world; Rhone-Poulenc of France; and Sumitomo Chemicals of Japan. Gallium is also produced in China, Hungary, and Czechoslovakia, but specific company activity in these countries is unknown. Furukawa Mining is believed to be Japan's largest supplier of high-purity arsenic, while Dowa Mining and Nippon Mining are major suppliers of high-purity indium, another important element present in compound semiconductor materials.

MATERIALS SUPPLIER OVERVIEW

Table 1 identifies manufacturers of polycrystalline material, single-crystal ingots, and wafers of gallium arsenide as well as other compound semiconductor materials. The information is not meant to represent an exhaustive analysis, but rather, has been formulated to give our clients an indication of the level of activity in this material segment on a worldwide basis. Information is based on company literature and recent announcements in the trade press, and has been organized alphabetically by company name.

Twenty-six of the 34 companies in Table 1 manufacture and supply the semiconductor industry with gallium arsenide wafers. Two companies (Hitachi Metals and Nippon Mining) are active in compound semiconductor materials but are not supplying gallium arsenide wafers to the industry at this time. Several GaAs wafer manufacturers also sell to companies that grow epitaxial layers of GaAs; these GaAs epitaxial wafers, in turn, are sold to semiconductor manufacturers. Six North American companies are participating in the epitaxial gallium arsenide market; these companies include U.S. companies Em-Core, Epitronics, Raytheon, Spire Corporation, and United Epitaxial Technologies, as well as Canadian start-up OMVPE Technologies. (Morgan Semiconductor is expected to start sampling its epi wafers by the end of 1986.)

The suppliers of compound semiconductor materials presented in Table 1 can be broadly classified as mining interests, cable manufacturers, silicon companies, chemical firms, and start-ups. For the cable manufacturers in particular, such as Furukawa Electric, Hitachi Cable, and Sumitomo Electric, the thrust into the compound semiconductor material market reflects a strategic transition from the more mature cable industry to fiber-optic technologies that rely on advanced optoelectronic materials and devices.

In addition to merchant materials suppliers, several vertically integrated semiconductor companies manufacture their own III-V substrates. Those semiconductor manufacturers that have captive production and consumption of GaAs include General Instruments, Harris, Hewlett-Packard, Hughes, M/A-Com, NEC, NTT, Rockwell, Siemens, Sony, Texas Instruments, Toshiba, and Westinghouse. Varian Associates, manufacturers of GaAs digital, microwave, and night vision devices, recently announced that it has ceased its captive production of GaAs substrate material because material of consistent quality is now available from merchant suppliers.

The fourth column in Table 1 includes the method of single-crystal growth for a given company's gallium arsenide, where known. The most common growth techniques are horizontal Bridgman (HB) and liquid-encapsulated Czochralski (LEC); both high-pressure and low-pressure LEC techniques have been developed. Horizontal Bridgman GaAs material is used in the fabrication of optoelectronic devices. However, silicon or silica doping can occur during horizontal Bridgman material growth, which renders the material useless for GaAs integrated circuits. Thus, LEC-grown GaAs material typically is used in the fabrication of digital and analog devices. Other methods of GaAs crystal growth that are used include vertical Bridgman, gradient freeze, Czochralski, liquid-encapsulated Kyropoulus (LEK), float-zone, horizontal- and vertical-zone melting, and MLEC (magnetic LEC).

GALLIUM ARSENIDE DEVICE MARKETS

The GaAs market initially developed in at least two independent areas. Since the mid-1960s, the demand for microwave communications and radar has driven the evolution of analog ICs (MMICs). Concurrently, the light-emitting properties of GaAs allowed the development of low-cost display devices (LEDs). In recent years, the emergence of fiber-optic communications heightened the need for GaAs lasers and photo detectors. Other recent applications include devices for electronic warfare (EW) and electronic countermeasures (ECM), Hall effect sensors, high-speed SRAMs and gate arrays, high-frequency phase-locked loops (PLLs), and linear and digital application-specific ICs (ASICs).

GaAs merchant market shipments in 1985 exceeded $1.3 billion. Optoelectronic devices represented $1.10 billion in merchant shipments, or essentially 80 percent of the GaAs merchant market sales. Analog IC shipments were approximately $80 million in 1985, while digital ICs represented only $26 million in merchant shipments. The remaining segment of the GaAs merchant market shipments is represented by other discrete devices including solid-state and power transistors.

Dataquest estimates that worldwide GaAs merchant device shipments will exceed $3.7 billion by 1990, which represents an overall CAGR of 22 percent. The optoelectronic device segment is expected to double between 1985 and 1990 to approximately $2.1 billion, with a CAGR of approximately 15 percent. In contrast to this moderate growth rate, Dataquest estimates that analog IC shipments will be in excess of $380 million in 1990 (37 percent CAGR), and digital IC shipments will approach $600 million (86 percent CAGR). Dataquest believes that the influx of new players in the gallium arsenide material market in the United States and Europe will be focusing on LEC material for IC devices, as Bridgman GaAs material (and optoelectronic devices) are mature markets in Japan.

DATAQUEST ANALYSIS

Dataquest has identified the level of worldwide industrial activity in GaAs in 1985. Thirty-four compound semiconductor materials manufacturers have been identified, 26 of which are supplying the semiconductor industry with GaAs wafers. Companies that produce GaAs devices include 28 merchant market suppliers of ICs, 26 merchant suppliers of GaAs discretes, and 21 captive-only houses manufacturing GaAs devices. Included in the count of 54 GaAs merchant device suppliers are 9 start-up companies that are expected to start shipping product in the 1986/1987 time frame.

It is important to maintain a perspective on gallium arsenide's role compared with silicon-based components in the semiconductor product families. GaAs and other III-V compound devices will displace silicon on a direct competitive basis only in applications where GaAs offers a distinct advantage over silicon-based devices, such as those requiring superior upper-frequency limits, better radiation hardness, or higher operating temperatures.

Table 2 indicates that the 1985 gallium arsenide IC market at $106 million still represented less than 1 percent of worldwide IC consumption, while the total GaAs merchant consumption of devices represented 5.5 percent of the worldwide semiconductor market. (Gallium arsenide devices include analog and digital ICs as well as discrete and optoelectronic devices.) In 1990, Dataquest estimates that gallium arsenide ICs will represent approximately 2 percent of worldwide IC consumption, while total GaAs merchant consumption of devices will represent 6.7 percent of the worldwide semiconductor market.

In contrast to the relative size of the device market segments, the number of companies currently producing wafers of silicon and gallium arsenide is essentially the same, which indicates that the gallium arsenide field is crowded. Sumitomo Electric in Japan is acknowledged as the world market leader in gallium arsenide and compound semiconductor materials, with an estimated market share on the order of 50 percent. The captive production and consumption of gallium arsenide by 13 semiconductor companies further reduces the size of the potential GaAs wafer market for merchant materials manufacturers. Dataquest believes that over the next few years, even as the gallium arsenide device market experiences growth, the gallium arsenide material companies will have to aggressively compete for sales, for share, and for survival.

Peggy Marie Wood
Gene Miles

Table 1

GaAs AND COMPOUND SEMICONDUCTOR MATERIALS SUPPLIERS WORLDWIDE

Company	Country	Products	Comments
Airtron	U.S.	GaAs wafers	Growth method: LEC Airtron--division of Litton Industries. 2", 2.5", 3" GaAs wafers available
Bertram Labs	U.S.	GaAs wafers	Growth method: HB 2" GaAs wafers available
Boliden Finemet AB	Sweden	GaAs wafers	Growth method: HPLEC 2 and 3" GaAs wafers available
Cominco Electronic Materials	Canada	GaAs, GaSb, InSb, InAs, CdTe, HgTe, and CdHgTe wafers	Growth methods: HPLEC, HB Completed expansion of LEC GaAs wafer production facility in Trail, British Columbia, in August 1985; capacity 250,000 square inches/year. 2", 3", 4" wafers available from Cominco
Commercial Crystal Labs, Inc.	U.S.	GaAs, GaP, InP wafers	Growth methods: LEC, HB 2" wafers available
Cryscon Technologies	U.S.	GaAs wafers	Growth method: LEC Subsidiary of Alcan Aluminum of Canada. Started shipping GaAs Q4/85. Cryscon supplies 2", 3" GaAs wafers produced by LEC and electrodynamic gradient freeze (EGF) technique. Annual capacity approximately 2 million square inches/year. Epitronics (other Alcan subsidiary) potential customer for Cryscon wafers
Crystal Specialties	U.S.	GaAs wafers, MOCVD epi reactors	CSI became subsidiary of Kollmorgen Co. in summer 1984. Wafer facility to be relocated to Colorado Springs, Colorado, from Ephraim, Utah, in Q3/86; reactor facility in Portland, Oregon

(Continued)

Table 1 (Continued)

GaAs AND COMPOUND SEMICONDUCTOR MATERIALS SUPPLIERS WORLDWIDE

Company	Country	Products	Comments
Dowa Mining	Japan	GaAs, InP wafers, poly InP, high purity In	Growth method: HB Research lab located in Akita
Em-Core	U.S.	GaAs epitaxial wafers, MOCVD epi reactors	Small start-up in New Jersey, started in late 1984
Epitronics	U.S.	GaAs epitaxial wafers	Subsidiary of Alcan Aluminum of Canada, like Cryscon Technologies
Furukawa Electric	Japan	GaAs, InP wafers, GaAs epitaxial wafers	Growth method: LEC Wafers produced at Tokyo lab
Galaris Corporation	U.S.	GaAs wafers, poly and single-crystal GaAs ingots	Growth method: HB Started in 1983 as research organization. Marketing of GaAs materials primarily focused toward R&D facilities
Gallium Arsenide Substrates	U.S.	GaAs wafers, poly and single-crystal GaAs ingots	Using gradient freeze process with less than 1000 dislocation defects/square centimeter. Company capitalized with $1 million in private funding
Hitachi Cable	Japan	GaAs, InP wafers, single-crystal GaAs ingots	Growth method: LEC Main production facility for III-V materials at Takasago plant in Ibaraki prefecture
Hitachi Metals	Japan	Single-crystal GaAs ingots	Growth method: LEC Working on single-crystal undoped GaAs

(Continued)

Table 1 (Continued)

GaAs AND COMPOUND SEMICONDUCTOR MATERIALS SUPPLIERS WORLDWIDE

Company	Country	Products	Comments
ICI Wafer Technology	U.K.	GaAs, InP wafers, poly and single-crystal GaAs and InP ingots	Growth method: LEC ICI announced in July 1985 plans to establish GaAs plant in U.S. (West Coast) in next 2 years to produce GaAs and other III-V compound wafers. ICI purchased Cambridge Instruments' III-V operations in January 1985. 2" and 3" GaAs, and 2" InP wafers available
Iwaki Handotai	Japan	GaAs wafers	Growth method: LEC 50-50 joint venture between Furukawa Mining and Shin-Etsu Handotai, established in 1982. Plant in Fukushima prefecture began producing 2" and 3" wafers in June 1983. Shin-Etsu Handotai started shipping 2" GaAs wafers to its U.S. subsidiary, SEH America, from Iwaki Handotai in June 1985. 3" wafers available in R&D quantities
M/A-Com Semiconductor Products	U.S.	GaAs wafers	Growth method: LEC Merchant sales as well as captive consumption of GaAs wafers. Microwave Associates, Ltd., is distributor for M/A-Com in the United Kingdom
MCP Limited	U.K.	GaAs wafers	Located in Wembley, Middlesex
Metal-specialties, Inc.	U.S.	GaAs, GaP, GaSb, InAs, InP, InSb wafers	Growth methods: LEC, HB

(Continued)

Table 1 (Continued)

GaAs AND COMPOUND SEMICONDUCTOR MATERIALS SUPPLIERS WORLDWIDE

Company	Country	Products	Comments
Mitsubishi Metal Corporation	Japan	GaAs wafers	Growth methods: LEC, HB Wafer plant located in Omiya, Saitama prefecture. Nissho Iwai Corp., distributor in the United Kingdom
Mitsubishi Monsanto Kasei (MMK)	Japan	GaAs, GaP wafers	Growth method: LEC Production system for 3" nondislocation GaAs wafers developed at Tsukuba plant. Plant capacity expected at 500 wafers per month. MMK using NTT's vertical magnetic CZ technology to produce the 3" wafers with only 10 defects per square centimeter. Monsanto Electronic Materials Co. (MEMC) to market MMK's GaAs wafers in the U.S.
Morgan Semiconductor	U.S.	GaAs wafers, GaAs epitaxial wafers	Growth method: LEC Started sampling low-pressure LEC 3" GaAs wafers in 1984; medium-pressure LEC 3" GaAs sampling due September 1986. Sampling of 2" and 3" GaAs epi wafers due by end of 1986
OMVPE Technologies	Canada	GaAs epitaxial wafers	Start-up located in St. Laurent, Quebec, Canada
Nippon Mining	Japan	InP wafers, poly and single-crystal InP, single-crystal GaAs and CdTe ingots	Growth method: LEC First Japanese company to grow low-dislocation density 3" InP crystal material. Nimic (Cupertino, CA) is a Nippon Mining subsidiary; purpose is to promote sales of GaAs, InP, CdTe, and other compound semiconductor materials in the U.S.

(Continued)

Table 1 (Continued)

GaAs AND COMPOUND SEMICONDUCTOR MATERIALS SUPPLIERS WORLDWIDE

Company	Country	Products	Comments
Raytheon	U.S.	GaAs epitaxial wafers	Growth methods: LEC, HB
Showa Denko	Japan	GaAs, InP wafers	Growth method: LEC First company in Japan to produce InP wafers by magnetic LEC. Sampled reduced-defect GaAs wafers in summer 1985
Siemens Company Inc., Opto Div.	U.S.	GaAs wafers	Growth method: HB Facility located in Cupertino, CA. 1.6 to 3" wafers available.
Spectrum Technology	U.S.	GaAs wafers	Growth method: LEC Spectrum founded in 1982, acquired in Q2/85 by Nerco Advanced Materials, Inc. (Portland, Oregon), a large mining interest in the Pacific Northwest
Spire Corporation	U.S.	GaAs epitaxial wafers and equipment	Located in Bedford, Massachusetts
Sumitomo Electric	Japan	GaAs, GaP, InP, InSb, InAs, GaSb wafers	Growth method: LEC, HB Largest III-V substrate supplier in the world; estimated GaAs worldwide market share of 50 percent. Has capacity for 3,000 3" GaAs wafers/month. GaAs material produced at wafer plant in Itami City (north of Osaka), Hyogo prefecture
Sumitomo Metal Mining	Japan	GaAs, GaP, and CdTe wafers	Growth method: LEC

(Continued)

Table 1 (Continued)

GaAs AND COMPOUND SEMICONDUCTOR MATERIALS SUPPLIERS WORLDWIDE

Company	Country	Products	Comments
United Epitaxial Technologies	U.S.	GaAs and AlGaAs epitaxial wafers	Start-up in Oregon; received approximately $5 million first round of venture funding. Company founded in mid-1984. Working with Crystal Specialties to develop MOCVD equipment
Wacker	West Germany	GaAs, GaP, InP wafers	Growth methods: LEC, HB

Source: Company Literature
Dataquest
August 1986

Table 2

WORLDWIDE CONSUMPTION OF SEMICONDUCTOR DEVICES
(Millions of Dollars)

	1985	Forecast 1990
Total Semiconductor	24,823	55,458
Total GaAs Devices*	1,371	3,720
Percent GaAs Devices	5.5%	6.7%
Total IC Devices	19,003	46,108
Total GaAs ICs	106	972
Percent GaAs ICs	0.6%	2.1%

*Includes analog and digital ICs, discretes, and optoelectronic devices.

Source: Dataquest
August 1986

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: 1985-1986 Newsletters
1986-11

WAFER FAB UPDATE--
WHAT'S NEW IN SILICON

SUMMARY

At least 17 companies have announced plans to put leading edge wafer fabs into production in the United States before the end of 1988. Of these fabs, 11 will handle silicon and 6 will handle gallium arsenide. Dataquest has noted at least 25 publicly announced fabs that will go into production by 1990, but we have also seen at least 20 fabs closed since early 1985.

Table 1 summarizes the current and future fab activity that Dataquest has tracked. This newsletter presents a detailed summary of some of the companies listed in the table. For more information about the fabs marked with an asterisk, please see SEMS newsletter number 1986-5, "Activity in the Fabs: GaAs Building; Shutdowns and New Lines in Silicon."

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 971-9000, Telex 171973, Fax (408) 971-9003

Table 1

CURRENT AND FUTURE FAB ACTIVITY

Company	Location	Begin Production	Wafer Size	Class	Line Width	Process Technology	Status
Advanced Micro Devices*	Austin, Texas	N/A	150mm	10	N/A	CMOS	Upgrade
Advanced Micro Devices* (Fab 8)	Sunnyvale, California	On hold	150mm	10	2	CMOS	Upgrade
Advanced Micro Devices* (Fab 4)	Sunnyvale, California	N/M	100mm	N/A	N/A	Bipolar	Closed
Anadigics*	Morristown, New Jersey	Q3, 1986	3 in.	100	0.5	GaAs	New
AT&T Technologies*	Orlando, Florida	1986	125mm	10	1.25	CMOS	New
Avantek*	Newark, California	N/A	N/A	N/A	N/A	GaAs	New
Coors Components*	Broomfield, Colorado	Q2, 1986	100mm	1000	5	Power MOS	Bought
Cypress Semiconductor	Round Rock, Texas	Q2, 1987	150mm	1	0.8	CMOS	Upgrade
Dallas Semiconductor	Addison, Texas	Jan., 1987	150mm	< 10	N/A	CMOS	New
Gain Electronics*	Branchberg, New Jersey	Q4, 1986	3 in.	10	0.25	GaAs	New
Hewlett-Packard*	San Jose, California	mid-1987	3 in.	100	5	GaAs OPTO	Upgrade
Hitachi, Ltd.	Irving, Texas	Q4, 1987	N/A	N/A	N/A	CMOS	New
Hughes*	Torrance, California	mid-1987	3 in.	100	0.5	GaAs	New
Hughes*	Malibu, California	Q1, 1988	3 in.	10	N/A	GaAs	New
International Rectifier*	Rancho, California	Q1, 1987	125mm	10	5	Power CMOS	New
Micron Technology (Fab 1)	Boise, Idaho	1987	125mm	< 100	N/A	CMOS	Upgrade

(Continued)

Table 1 (Continued)

CURRENT AND FUTURE FAB ACTIVITY

Company	Location	Begin Production	Wafer Size	Class	Line Width	Process Technology	Status
Microwave Semiconductor*	Somerset, New Jersey	Q1, 1987	3 in.	N/A	N/A	GaAs	New
Mitsubishi	Research Triangle, North Carolina	N/A	N/A	N/A	N/A	CMOS	New
NEC							
Phase 1	Roseville, California	1985	125mm	N/A	N/A	NMOS	Production
Phase 2	Roseville, California	Q3, 1987	N/A	N/A	N/A	NMOS/ CMOS	Expansion
Phase 3	Roseville, California	1990	150mm	10	N/A	CMOS	Expansion
RCA/Sharp	Camas, Washington	N/M	150mm	10	2	CMOS	Canceled
Rockwell*	Newbury Park, California	Q2, 1986	3 in.	10	1	GaAs	New
Samsung	San Jose, California	Q2, 1987	125mm	N/A	< 1	N/A	New
SGS	Phoenix, Arizona	First half of 1987	150mm	1	< 1	CMOS	New
Siemens	Santa Clara, California	Q1, 1987	125mm	100	< 3	Power MOSFET	Bought
Siliconix	Santa Clara, California	1987	150mm	100	N/A	Power CMOS	Expansion
Sprague Electric	Worchester, Massachusetts	Q3, 1988	150mm	10	2	N/A	New
TRW	Los Angeles, California	Q3, 1986	N/A	10	0.5	VHSIC	New
VLSI Technology*	San Antonio, Texas	1988	150mm	10	1.25	CMOS	New
VTC	Bloomington, Minnesota	Q1, 1987	150mm	1	1	CMOS	New

N/A = Not Available
N/M = Not Meaningful

*These companies' fab activities were summarized in SEMS Newsletter 1986-5.

Source: Dataquest
August 1986

FAB ACTIVITY

Cypress Semiconductor

Cypress has revised plans to build a new 150mm fab from the ground up in Round Rock, Texas, in favor of refurbishing an existing fab there. Cypress has leased a 63,000-square-foot building equipped with a class 100 clean room. This facility previously was used to manufacture disk drives. The clean room will be upgraded to class 1 and will run the Cypress 0.8-micron CMOS process. This change in plans will allow Cypress to meet its goal of shipping wafers out of Texas by the second quarter of 1987. However, Cypress does not expect the fab to reach its 12,000-wafer-per-month capacity before mid-1989.

Cypress will move its administrative staff into a new 60,000-square-foot building during October of this year. The building is next to the current Cypress facility in San Jose, California. This will allow the entire original building to be used for fab, assembly, and test. The extra space will be used to expand the test and assembly capability of Cypress.

Dallas Semiconductor

Dallas Semiconductor is constructing a CMOS fab at its Addison, Texas, facility. Production of 150mm wafers is expected to begin by January of 1987 with 10,000 wafers to be run during that year. The fab is being installed in an empty wing at an existing 65,000-square-foot building. The clean room will be expandable to 30,000 square feet, will cost $2 million, and will be rated sub-class 10. The company has ordered three GCA steppers. Total equipment cost for the fab is expected to be $7.5 million.

General Electric

GE recently announced that it is cancelling the RCA/Sharp joint venture at Camas, Washington. Sharp, however, will continue to provide CMOS wafers to RCA from its Fukuyama, Japan, facility. GE and Sharp reportedly have agreed to define potential areas of future technology development. Prior to cancellation, the joint venture employed 91 people, 40 of whom will be offered positions with their parent companies. The remainder will receive a layoff package from the joint venture.

RCA/Sharp had a technology pact with WaferScale Integration to jointly develop a 1-micron cell library. The pact will now continue between WaferScale and Sharp.

General Electric has begun consolidating its recently acquired RCA fabs into GE's operations in Syracuse, New York, and in Research Triangle Park, North Carolina.

RCA recently brought up a new clean room area equipped with two 5X steppers at Findlay, Ohio. It will be running 100mm wafers at 1.2-micron line geometries. RCA is said to have plans to bring up a 125mm line sometime during 1987.

Hitachi

Hitachi is accelerating construction of its Irving, Texas, fab, which originally was to be completed by the third quarter of 1987. This fab will most likely produce ASICs, DRAMs, and EEPROMs. Capacity will also be expanded at the current test and assembly operation at Irving. The total investment will be around $100 million for the entire facility.

Micron Technology

Micron Technology is upgrading Fab 1 at Boise, Idaho. The fab, which was constructed in 1981, will be upgraded to as near a class 10 fab as possible. Start capacity will be increased and the fab will be set up for CMOS processing. Fab 1 is running 125mm wafers.

Mitsubishi

Mitsubishi is planning to build a fab at its current test and assembly facility on 80 acres at Research Triangle Park, North Carolina. Plans call for fully integrated production of mainly DRAMs and ASICs.

NEC

Phase 1 of NEC's three-phase project at Roseville, California, is coming into full production now. The 200,000-square-foot facility runs 125mm wafers and has a start capacity of 10,000 wafers per month. The facility currently employs 600 people (160 in production) and is producing SRAMs, DRAMs, and gate arrays.

Phase 2 is scheduled to be completed by the third quarter of 1987. This phase will add 70,000 square feet to the building and will allow NEC to double production of ASICs, memories, and other products.

Phase 3 is scheduled for completion during 1990. In this phase, the fab will be highly automated and will run 150mm wafers or perhaps larger. This phase will add 130,000 square feet to the facility, and NEC expects to employ at least 3,000 people at Roseville as a result. The total investment for all three phases is expected to be in the area of $750 million.

Samsung

Samsung has purchased a $5 million building in San Jose, California, which will be the home of a state-of-the-art fab. The facility is expected to receive its equipment before January and to begin pilot production by the second quarter of 1987. The fab will run 125mm wafers and will be capable of sub-micron processes. Samsung plans to spend about $11 million for equipment and other items. The South Korean chip maker may have further expansion plans. The company has right of first refusal on an existing 70,000-square-foot building next door, as well as a one-acre site that could be used for additional parking.

SGS

The SGS facility at Phoenix, Arizona, is now complete and is ready for equipment installation. Pilot production, which was recently planned to begin by the end of 1986, has now been pushed back to sometime during the first half of 1987. The shell of the building covers 280,000 square feet and is located on five acres of land. The 22,500-square-foot, class 1 clean room will run 150mm wafers, and a sub-micron CMOS process will be used. SGS estimates that the market will bring the new fab to full capacity by the end of 1987.

Siemens

Siemens has purchased Hyundai's Santa Clara, California, wafer fab and has broken off talks with Sperry regarding the purchase of Sperry's Egan, Minnesota, facility. Hyundai originally paid approximately $40 million for the 98,000-square-foot facility, which contains a 11,000-square-foot, class 100 clean room. It is not known if any equipment is included in the sale of the fab. Siemens expects to employ 300 people at the Santa Clara facility by the end of 1987.

At least some of the production at the Santa Clara facility will involve sub-3-micron Power MOSFET production. This production is being transferred to Santa Clara from the Sipmos line at Broomfield, Colorado, which will be shut down by the end of 1986. Twenty-seven of Siemens' Broomfield employees will be relocated to the Santa Clara facility.

Siemens is attempting to enlarge the manufacturing base of its semiconductor operations in the United States and has set aside large cash reserves for such purchases. This is the first successful fab purchase for Siemens in recent years.

Siliconix

Siliconix plans to expand capacity at its existing fabs in Santa Clara, California, during 1987. Up to 15 steppers will be ordered to fill the empty areas of the fabs, which, when combined, equal 45,000 square feet. The facility currently runs 150mm wafers with CMOS and MOS processes for power devices.

Sprague Electric

Sprague Electric at Worchester, Massachusetts, is making room within an existing building for a new 30,000-square-foot clean room. It will hold new 150mm equipment that will be capable of 2-micron production. The addition is scheduled to be completed by the third quarter of 1987. Production should begin by the third quarter of 1988 and capacity is expected to be reached by 1990.

TRW

TRW has started production at a new fab at Space Park Center near Los Angeles, California. The VLSI fab is located in a 215,000-square-foot building housing a 15,000-square-foot, class 10 clean room. VHSIC chips with claimed 0.5-micron line geometries will be produced at this location.

VTC

VTC has completed a new $25 million VHSIC facility that has been built to meet strict physical and electronic security requirements. These security requirements include 14-inch-thick concrete walls with offset double rows of case-hardened iron bars. These walls are lined with copper sheeting for radio frequency shielding. Metal sheets are set between double layers of concrete in the floors and roofs to provide additional electronic security. This design will allow VTC to design and fabricate highly confidential military and aerospace ICs.

The facility contains a 30,000-square-foot, class 1 clean room and will run a 1-micron CMOS process. The facility is also set up for CAD testing and assembly within the secured building. The facility has received two SRA-9000 Perkin-Elmer steppers that will run 150mm wafers. The fab is expected to start running wafers at the end of this year and to begin production during the first quarter of 1987. VTC's future plans feature production of sophisticated semiconductor devices including memories and ASICs.

DATAQUEST'S CONCLUSIONS

We have noted 25 fabs on Table 1 that will begin operations by 1990. We have also noted 20 recent fab closings. Semiconductor companies are not sure that an upturn is coming in the near future and if it does, most feel they have plenty of capacity to handle it. We estimate that total U.S. semiconductor capacity utilization is in the neighborhood of 60 percent.

One trend that may favorably affect North American capital spending is the movement of some Japanese semiconductor manufacturing to the United States. The favorable yen-to-dollar exchange rate and current trade friction issues are making the United States look more attractive for Japanese capital spending.

On the other hand, the force of technological change may, in some cases, slow capital spending in North America. The current level of technology and capacity appears to be capable of satisfying the anticipated demand for 1Mb DRAMs but not demand for 4Mb DRAMs. If semiconductor companies believe that the market is going to leapfrog the 1Mb era quickly, they may wait for the next generation of equipment technologies to become available.

One thing is clear: The number of fab openings and closings reflects the state of the industry. Our industry has recently closed almost as many fabs as it has announced it will open, which reflects the recent downturn. However, since most of the openings are for state-of-the-art facilities and most of the closings involve outdated technologies, we believe that this reflects the industry's technological emphasis, from which new equipment and fabs will eventually emerge.

Mark Reagan

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: 1985-1986 Newsletters, August
1986-10

A $650 MILLION FAB IN THE YEAR 2000?

INTRODUCTION

The semiconductor industry has changed dramatically in the past 25 years, and will change more as we approach the year 2000. In this month's newsletter, we will examine how much revenue a state-of-the-art fab can be expected to generate in the year 2000. This number is in turn an estimate of the optimum market size necessary to support an economically efficient fab. Dataquest believes that such estimates will be of great value to both start-ups and captives in determining whether to build a fab or buy capacity from foundries.

Three things determine the revenue that a fab can generate: output in wafers per period, revenue per square inch, and wafer size. Revenue per fab is equal to the number of wafers per fab per period times the size of the wafer in square inches times revenue per square inch.

Our analysis will show that revenue per fab will be a significant barrier to entry by the year 2000.

REVENUE PER SQUARE INCH

Dataquest currently has a data base on all of the fabs in the United States. Based on this data base, which we are constantly updating, we estimate that revenue per square inch for MOS wafers is $19.91.

We believe that revenue per square inch will show an upward trend because both average selling prices (ASPs) and yields will be up. Although average selling prices tend to rise and fall with the ups and downs of the business cycle (just ask any veteran of 1985), we believe that the long-term trend is upward for ASPs for three reasons. The first is because the value of devices will increase as they become more complex and contain an ever-larger number of functions. Second, ASPs will

increase because as device complexity drives fabrication costs higher, manufacturers will seek to maintain constant margins. Third, the more expensive ASIC devices will become a larger part of the product mix.

Increasing yields also favorably affect revenue per square inch. As yields increase, a manufacturer is able to get more devices per square inch, and thus, at a given ASP, more revenue. We expect yields to increase slightly because of automation and process innovations. Automation and process innovation will reduce particulate contamination caused by human contact. Automation will also decrease cycle time, work in process (WIP), and pipeline inventories, which will shorten the amount of time in which contamination and breakage can occur. We also expect that there will be better quality control and better quality of materials, and that these will affect yields positively.

The one factor that can bring yields down is larger die sizes. Increasing die sizes basically increases the area of probability in which a killer defect can occur. However, we believe that the effects of increasing yields and increasing ASPs will keep the effects of larger die sizes under control. We expect MOS revenue per square inch to grow from $15.50 in 1980 and $19.91 in 1985 to $20.93 in 1990, and to rise slightly thereafter at a CAGR of 1 percent per year to $21.99 in 1995 and $23.11 in the year 2000.

WAFER SIZE

Wafer sizes have been growing, and they will continue to do so. The reason for this increase in size is that manufacturers can get many more devices, and hence reap more revenue, from a larger wafer. The increased revenue more than offsets the increased production costs associated with larger-diameter wafers.

Table 1 provides an example of how this works. Let us assume that in 1985, as the industry began to change from processing 100mm wafers to 150mm wafers, line geometries and yields were constant. That is, that the number of die per square inch remained constant. Even though processing costs per wafer doubled, cost per gross die decreased by 12 percent. To take advantage of this cost reduction, semiconductor manufacturers have moved strongly to become 150mm capable.

This concurs with our data base of U.S. fabs, which shows that 150mm wafers consumed more silicon in 1985 than did 3-inch wafers, and, also in 1985, 125mm wafers accounted for almost 200 million square inches of consumption.

Because of these continuing economies of scale associated with larger wafers, we believe that by 1990, 3-inch wafers will all but disappear, and 150mm wafers will account for the consumption of more square inches than any other size of wafer (see Table 2). We also believe that 200mm wafers, which we expect to appear in 1988, will account for 4 percent of total square inches consumed by 1990.

Table 1

EFFECTS OF INCREASED WAFER SIZE

	100mm	150mm
Square inches	12.68	28.53
Gross die/inch	16.48	16.48
Gross die/wafer	209	470
Processing cost/wafer	$ 100	$ 200
Cost/gross die	$0.48	$0.42

Table 2

DISTRIBUTION OF SQUARE INCHES BY WAFER SIZE--1985-1990

Wafer Size	1985	1986	1987	1988	1989	1990
2"	1%	0%	0%	0%	0%	0%
3"	7	5	3	1	1	1
100mm	55	51	47	39	33	25
125mm	30	30	32	34	35	36
150mm	7	14	18	25	29	34
200mm	0	0	0	1	2	4
Total	100%	100%	100%	100%	100%	100%

Source: Dataquest
August 1986

Looking beyond 1990, we think that it is not unreasonable to expect to see 250mm wafers by 1995 and 300mm wafers by the year 2000.

OUTPUT PER FAB

Each fab has an optimum level of production. If it operates below its optimum level, it underutilizes the facility and thus is not economically efficient. An output above the optimum causes problems with line balancing, scheduling, materials shortages, increased costs, and yields.

An optimum level of output may of course vary, depending on the process, the number of mask layers per wafer, and the equipment used. Some manufacturers estimate that 10,000 wafers per four-week period is an optimum output; some of the newer fabs coming on-line are designed for 20,000 starts per four-week period.

Currently at Dataquest, we are assuming that 14,000 wafers per four-week period is an optimum output for a state-of-the-art CMOS fab. We will also assume that over the period of this analysis, this optimum level will remain constant. This is a conservative assumption; optimum operating sizes will probably increase between now and the beginning of the next millenia. Any increase beyond our assumed 14,000 starts per four-week period will increase the force of our argument that it will be much more difficult for a small or medium-size firm to operate a state-of-the-art fab by the year 2000.

THE YEAR 2000

As Table 3 illustrates, if the minimum optimum level of operating a fab is 14,000 wafers per four-week period in the year 2000, then a state-of-the-art facility will produce $476 million dollars worth of devices in a year. This output of one fab is equivalent to slightly less than Fairchild Semiconductor's total semiconductor sales in 1985.

Table 3

REVENUE PER FAB
(Millions of Dollars)

	1980	1985	1990	1995	2000
Wafer size	100mm	150mm	200mm	250mm	300mm
Rev/In^2*	$15.50	$19.91	$20.93	$21.99	$23.11
Rev/Fab	$35	$102	$191	$314	$476

*Assumes CAGR of 1 percent from 1985 to 2000

Source: Dataquest
August 1986

It should be emphasized that the assumptions underlying this analysis are conservative: 300mm (12-inch) wafers by the year 2000 are very likely; a 1 percent CAGR of revenue per square inch is not aggressive; and finally, the optimum operating level of a state-of-the-art CMOS fab will probably increase. We believe that it will increase because of increasing equipment costs. The increasing cost of equipment will drive up fixed costs, and higher fixed costs need high volume to be economically justified. If we assume an optimum of 20,000, 300mm wafers per four-week period, a year's output grows to more than $670 million--which is more than AMD's 1985 revenues.

DATAQUEST ANALYSIS

If a strategic planner were to ask himself or herself the question, "Should we build a fab or buy from merchants or a foundry?", one of the variables they would look at is output per fab. In 1980, in order to justify building a fab, all a strategic planner had to do was to find $35 million worth of business. By the year 2000, we expect the magic number to be at least $400 million, and it could be as high as $670 million.

Dataquest projects that custom and semicustom circuits will account for approximately 35 percent of all ICs produced by the end of the decade. By the year 2000, this proportion should be even higher. This analysis suggests an answer. As the market conditions favor custom and semicustom devices, manufacturing economics are bringing about conditions favorable to a thriving foundry industry.

Already today, there are more than 40 foundries in the United States. The list includes companies as large as National Semiconductor and companies as small as Acrian. We expect the list to get longer. In the year 2000, a merchant manufacturer will not only have to be concerned with how many systems houses will buy its product, but also how many will use its facilities for foundry work.

George Burns

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: 1985-1986 Newsletters, August 1986-12

NMB SEMICONDUCTOR: A NEW AUTOMATED JAPANESE SEMICONDUCTOR FACILITY

We recently visited NMB Semiconductor's new facility in Tateyama City, Japan. NMB is a new kind of Japanese semiconductor company with a fully automated wafer fabrication facility. Consequently, information on this company should be of interest to our clients. In addition to the description of NMB's facility, we have included a discussion on our perspective on automated fabs in general.

THE COMPANY

NMB Semiconductor Co. was established in May 1984 by Minebea Co., the world's leading manufacturer of precision ball bearings. Besides Minebea, which has an 18 percent investment share and responsibility for all management and operations, other investors include major Japanese investment companies and banks. Minebea has recently begun to diversify into electronics, and although manufacturing integrated circuits is a new area for Minebea, it feels that its automated production techniques developed to manufacture precision ball bearings in clean rooms can be adapted to the manufacture of VLSI devices as well. Minebea's diversification into electronics is similar in concept to the recent movements by Japanese steel companies into silicon wafer manufacturing.

NMB is considered somewhat of a maverick company by the other Japanese semiconductor companies. The major Japanese semiconductor manufacturers are huge horizontally and vertically integrated companies with large semiconductor R&D programs. NMB, in contrast, has limited R&D capability and has purchased its chip-making technology through technology agreements. An advantage of buying the technology is that the few percent royalty fee required by technology agreements is less than the 10 percent or more of sales that a typical semiconductor company will spend on R&D. This translates directly into cost savings. To gain

market share, NMB intends to produce chips at lower prices by coupling this cost saving with that resulting from the higher yields obtained from an automated facility.

The effectiveness of this strategy remains to be seen. NMB was founded in 1984 during the height of the best year ever for the worldwide semiconductor industry, when prices were high and factories were operating at near-capacity levels. The ensuing recession of 1985/1986 has been calamitous for the industry: prices have fallen, in some cases drastically, and factories are greatly underutilized. NMB's factory became operational in August 1985, right in the midst of the turmoil when conditions were abnormal. We believe that little of NMB's product has appeared on the market, so we cannot yet gauge the effectiveness of NMB's strategy; a return to more normal times is required first.

THE PRODUCT

NMB is currently producing four CMOS products: a 256K DRAM, a 64K SRAM, a 16K SRAM, and a 1Mb DRAM. The 256K DRAM and 64K SRAM are high-end parts intended for high-value-added systems and are not meant to compete against the more conventional parts. For instance, the price of NMB's 256K DRAM is $4.50, versus $2.50 for a commodity 256K DRAM. We will discuss later the implications of choosing such niche parts for production in an automated fab.

A licensing agreement with Inmos provided the mask designs, circuit designs, and other basic technology for NMB's first product, a fast 60ns 256K DRAM. In addition to a 2 percent royalty fee, the agreement gives Inmos the right to buy back half of NMB's output. This part is available in three 256Kx1 versions: static column decode, nibble, and enhanced page modes. The chip is 4mm x 8mm (47,329 $mils^2$) and is fabricated in N-well CMOS with 1.7-micron design rules. Fabrication requires 13 masks and more than 600 processing steps. The device has a gate oxide thickness of 75 angstroms and uses polysilicon/tungsten silicide gate interconnects. First samples were produced in October 1985.

NMB has a licensing agreement with an undisclosed American company for the production of a fast 35ns 64K SRAM. This 64Kx1 device is fabricated in N-well CMOS with 1.5-micron design rules and has a size of 45,832 $mils^2$. Fabrication requires 15 masks. Substrate biasing is used to prevent latch-up. First samples were produced in November 1985.

Vitelic Corp. has licensed its 1Mb DRAM CMOS technology to NMB in return for a manufacturing commitment. This 1Mb x 1 device is fabricated with 1.2-micron design rules and requires 13 masks. It is currently in the sampling stage, with production expected by year-end.

NMB can sell the above three parts on the merchant market. In addition to these parts, NMB is also producing a 4Kx4 SRAM on a foundry basis for an unnamed partner.

Wafer starts range from 10,000 to 13,000 per four-week period in contrast with a capacity of 20,000 to 24,000 wafers. Approximately 65 percent of the starts are 256K DRAMs; the remaining 35 percent are the 16K and 64K SRAMs and 1Mb DRAM samples.

THE FACILITY

The facility is located in a beautifully wooded area in Tateyama City, on the Boso Peninsula, a two-hour train ride from Tokyo. The facility covers an area of 85 acres and consists of a 17,732 m^2 (191,000 $ft.^2$) plant building, a 2,113 m^2 (23,000 $ft.^2$) energy plant, an office building, a 2,771 m^2 (30,000 $ft.^2$) guest house, 50 dormitory rooms for unmarried employees, and 21 employee cottages. There are also two tennis courts and a swimming pool for the employees. Initial investment in the land and facilities was about $150 million (200 yen per dollar).

The energy plant provides on-site generation of nitrogen and oxygen and ultrapure deionized (DI) water. The DI water system is a closed recirculating system in which the waste water is continually recycled; thus, any danger of pollution is eliminated.

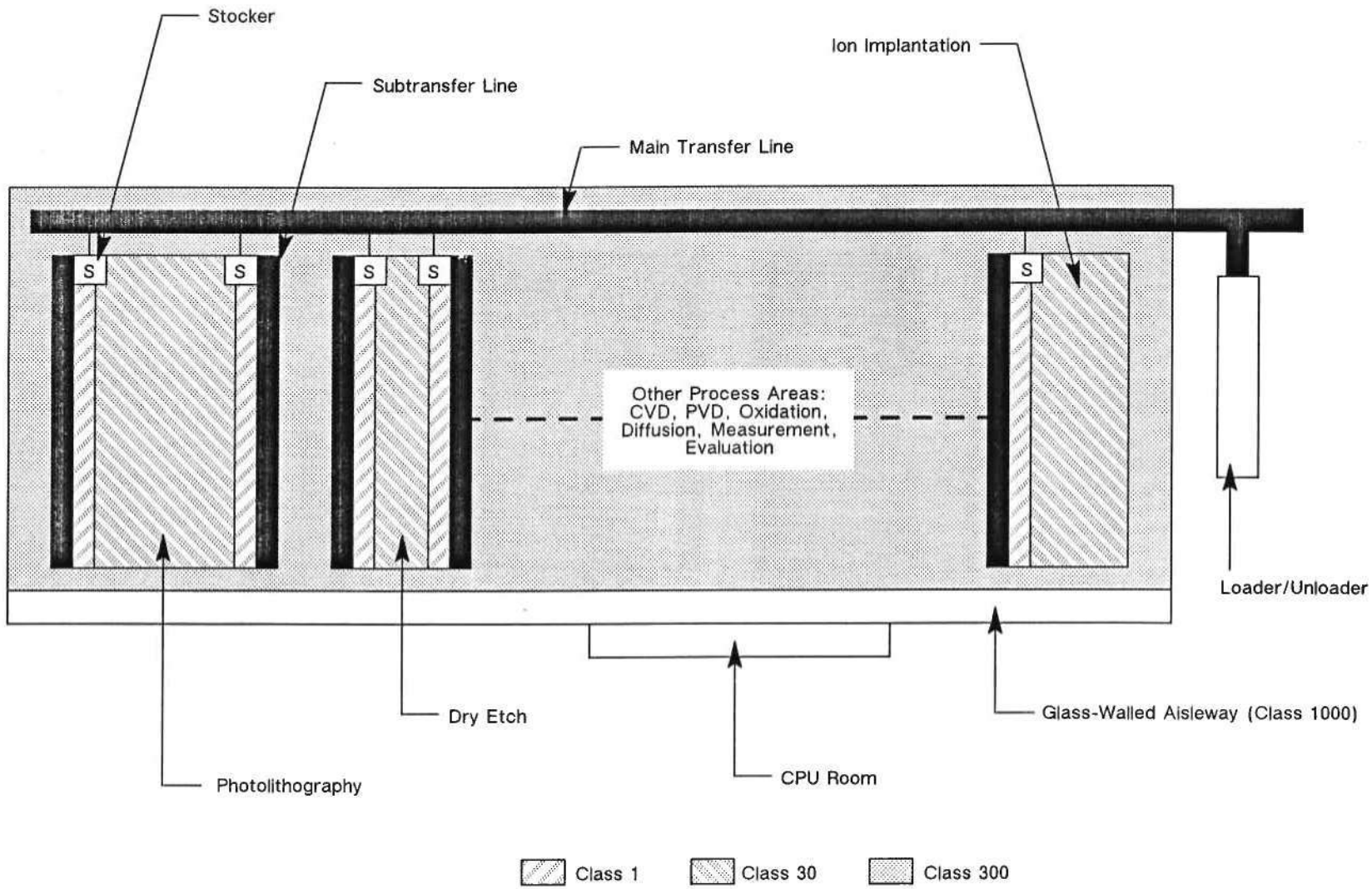
Although assembly and test are also conducted in the plant building, only the wafer fabrication facility is fully automated; automation of assembly and test will be done at a later date.

The wafer fabrication facility is a new concept in automation and clean room design, requiring the adaptation and modification of processing and automation equipment. Ground breaking occurred in August 1984; installation of processing equipment took three months and was completed by April 1985; first wafers were started in May 1985; and first working samples were obtained in August 1985. The elapsed time between ground breaking and first wafer starts was only nine months, a truly prodigious accomplishment, particularly considering the logistics and engineering required to construct and integrate this fully automated wafer fabrication facility. American semiconductor manufacturers should heed well the speed with which the Japanese are able to respond to changes in the marketplace.

The wafer fabrication area is divided into two large clean rooms, or modules, each 100 meters by 36 meters (38,750 $ft.^2$). Module 1, a 125mm line, is in operation, while installation of equipment in Module 2, a 150mm line, is scheduled to begin at the end of this year. Figure 1 shows a plan view of Module 1. The 100 x 36-meter clean room is divided into subareas of three types. Cassettes of wafers are transported by robots on tracks and transferred to the input stations of the process equipment in the Class 1 active area A. No operators are allowed in the Class 1 area. The Class 30 area M provides rear access to the process equipment for maintenance. The operators work in the Class 300 area P, and the equipment operator consoles are also located there.

Figure 1

PLAN VIEW OF MODULE 1



Source: NMB Semiconductor Company

Floor-to-ceiling glass walls separate the Class 300 area from the Class 1 area and the Class 1 area from the Class 30 area. In fact, the entire 100 x 36-meter area is partitioned with glass walls. Visitors can walk the length of the module and view the entire area through a glass wall. The effect of such large-scale use of glass walls is to give the fab a futuristic look.

The individual Class 1 areas are of varying size, depending on the process equipment and the requirements for access to it. For instance, in the dry etch area, the Class 1 area appeared to be a few feet wide, and only wide enough to allow room for the tracked robot and the transfer of the wafers into the etch equipment. Approximately 25 percent, or 900 m^2 (9,700 $ft.^2$), of the module area is Class 1.

Air return is through the module floor, and air turnover in the Class 1 area is 300 to 400 times per hour. Equipment pumps and other support equipment are located in the basement below the module. A centralized supply system for chemicals and special reactive gases is located in the basement and from there distributed to the process equipment throughout the module. Wet chemicals are stored in large containers and distributed to the process areas in coaxial plastic tubing: the inner tubing carries the chemical, while the outer tubing acts as a containment in the event of a rupture of the inner tubing.

Wafer handling in the module is fully automated: at no time does a human operator handle the wafers. The transport system consists of a main transfer line running the length of the module and subtransfer lines branching from the main line to the various process areas. The main transfer line is an overhead system using cars on a monorail to transport two open cassettes at a time. Any particulates generated by the rails are exhausted below the car. Stockers, or I/O stations, are located at the junctions of subtransfer lines with the main line. The cassettes are transferred from the car to the stocker via an elevator system; the cassettes are then transferred from the stocker to the subtransfer line robot running on an electric track.

The automation system, including software, was designed and developed by NMB but subcontracted to a robot vendor and to a software house. The system is controlled by a VAX 11/750 host computer connected to 18 CRTs located throughout the fab. The control system uses bar code readers and has the capability of lot and individual wafer tracking. The robot's location in the clean room, and possibly other information, is transferred between the robot and the host computer via robot sensors located on the subtransfer lines. Sixteen CCTVs are used in the control room to monitor various areas in the module, as well as some areas in test and assembly.

Module 1 has a capacity of 20,000 to 24,000 wafers per month, or 4 million finished parts per month. The number of operators in wafer fabrication, assembly and test required to support this capacity is 144 divided into four groups of 36 operators per shift. There are two 12-hour shifts per day, and each group works three days on, three days

off, four days on, and four days off. Saturday mornings are set aside to do as much of the weekly preventive maintenance as possible. Altogether, there are 300 employees including the 144 operators plus process engineers and energy center and administrative personnel.

The initial investment of $150 million included $59 million for equipment, of which 70 percent was for front-end equipment and 30 percent for assembly and test equipment. Approximately 10 percent of the cost of the front-end equipment was for automation; it is not clear to us whether this includes the cost of the host computer and software as well.

NOTES ON PROCESS EQUIPMENT

Module 1 is an all-stepper facility that uses steppers for the noncritical levels as well. There are 12 Nikon steppers, capable of 1-micron resolution, interfaced to Dainippon Screen photoresist processing equipment. The original Inmos design for the 256K DRAM used 12 masks, and we believe that NMB's original intent was to dedicate a stepper to each mask level. But since the 256K DRAM design is now 13 masks and the 64K SRAM is a 15-mask design, there are steppers running multiple masks. Only positive photoresist is used. The photolithography cell is mounted on vibration-isolated concrete pillars that are decoupled from the rest of the building and extend 10 meters down through the floor of the cell, through the basement, and into the ground.

NMB is using advanced films in the area of thin-film deposition. Tungsten silicide is used as a gate interconnect and is deposited with Genus low-pressure CVD reactors. BPSG is used as an interlayer dielectric and is deposited with a Watkins-Johnson atmospheric pressure CVD reactor. Plasma-enhanced CVD reactors are used to deposit oxynitride passivation layers.

AUTOMATION RESULTS

What has been the effect of automation on yields? NMB would not comment on its yields, but it did say that the defect density was one to two defects/cm^2/wafer for all levels and a particle size greater than 0.17 micron. For the 256K DRAM, using this defect density in Murphy's Law results in a theoretical yield of 56 to 74 percent. Note that the minimum feature size for the 256K DRAM is 1.7 micron and that NMB considers a killer defect to be 0.1 times the minimum feature size.

For the 1Mb DRAM with a feature size of 1.2 micron, the killer defect size is 0.12 micron. NMB has said that its goal is 95 percent yield on the 1Mb DRAM; this would imply a defect density of 0.1 defect/cm^2/wafer for particles larger than the 0.12-micron killer defect size.

Another key advantage of automation is the decreased cycle time. However, NMB's cycle time from wafer start through final passivation is about six weeks. We believe this to be on the high side since the fully automated Mitsubishi Saijo facility has a cycle time on the order of three weeks, and some efficient nonautomated facilities in the United States have six- to eight-week cycle times. It is possible that NMB's cycle time will come down with more production experience.

FULLY AUTOMATED FABS--DATAQUEST'S PERSPECTIVE

A fully automated fab is generally dedicated to the production of a single product or a small family of products with similar fabrication processes; it tends to be highly mechanized and is generally inflexible because of limited automation software capability. The best use of such a fab, and perhaps the only economic justification for it, is volume production of product that can sell into a large preestablished market. To amortize the relatively high fixed costs of such a fab, it is absolutely necessary to run the fab at near-maximum capacity. This means that the proper choice of product must be made to fill the fab quickly, the accounts must be identified, and the marketing and distribution channels must be established to sell the manufactured product.

For this reason, very few products are appropriate for efficient manufacture in highly automated fabs. Only at certain times in the product life cycle, when there is good visibility into future market needs, are such fabs economical. It is the high-volume product that fits best into dedicated, inflexible, fully automated fabs, and these fabs require planning and commitment of funds often years in advance of their actual output. However, there is a clear conflict for the semiconductor manufacturer: planning has to be done years in advance, yet semiconductor markets are characterized by a lack of forward visibility in terms of unit volume demand.

Timing is paramount: when the fab goes on-line, the product must be manufacturable and the market must be available and be sustainable for several years to fully recoup the capital investment. Few markets are appropriate for such undertakings, and although MOS memory is the clearest example, even in this area the product chosen must be the correct one, and the market timing in the larger industry context must also be appropriate.

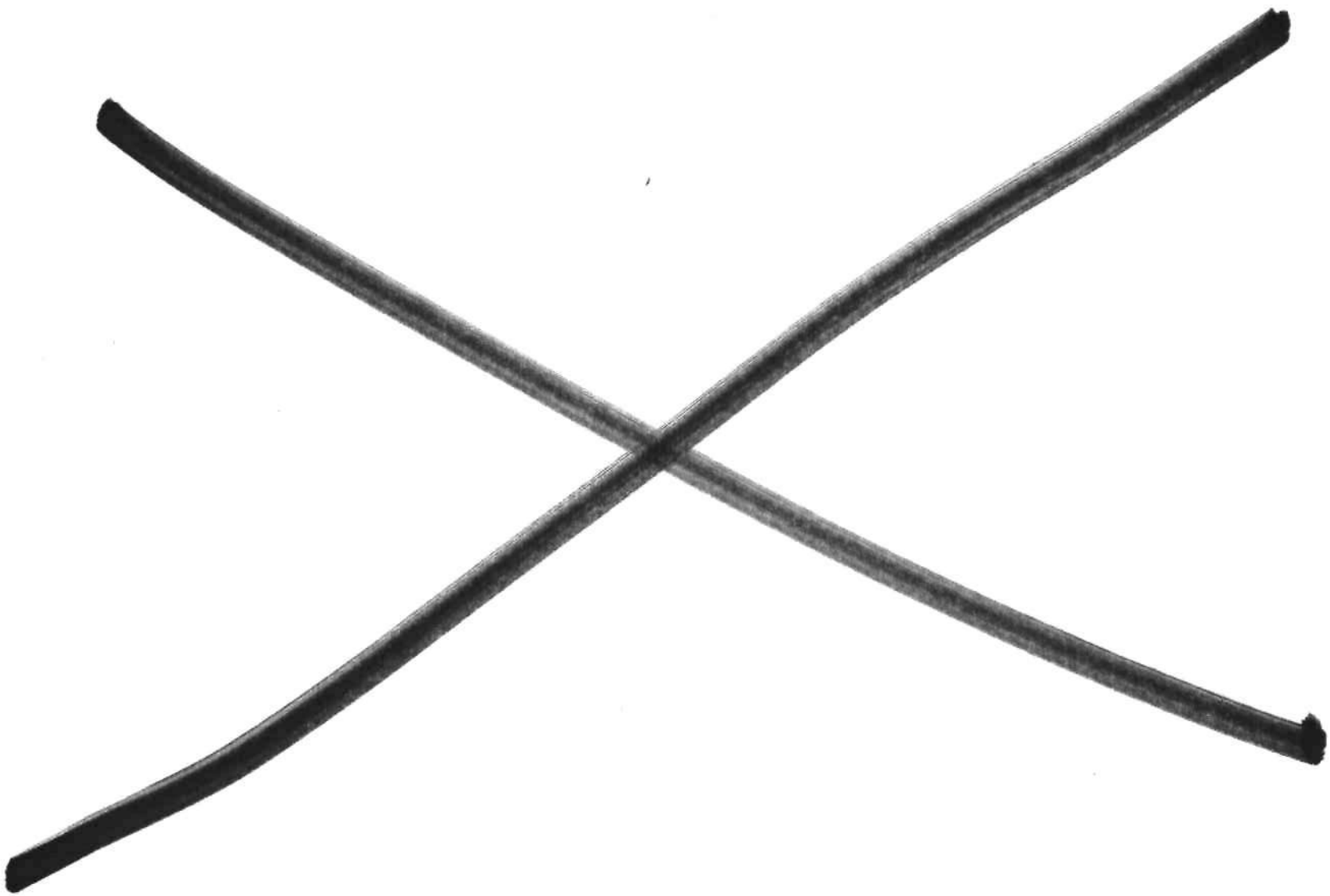
Automation should ultimately translate into lower-cost product, which will give a company a competitive edge in a normal market. However, the risks of highly automated, single-product fabs in a down market have become apparent. The high fixed costs of these factories make it imperative that they run at near-maximum capacity to amortize the costs over a reasonable period of time. The industry is currently in the midst of a severe industry recession, and companies with underutilized, highly automated fabs are painfully aware of the burden of high fixed costs.

Foundry relationships may be sought in an attempt to fill the fab in periods of slack capacity. However, a highly mechanized fab with limited-capability automation software can be inflexible when operating as a foundry. Few fabrication processes are universal enough to accommodate more than a few state-of-the-art products, and sophisticated automation software (and associated hardware) is required to handle the process changes associated with running multiple products with multiple processes.

Furthermore, it is increasingly recognized in foundry relationships that there is a close relationship between the product being designed, the process used in the manufacture of the product, and the specifics of the foundry fab. This makes arm's-length foundry relationships, especially for state-of-the-art products, extremely difficult to manage. It is becoming absolutely necessary for circuit designers to work closely with the foundry's process engineers. This is the justification for having circuit designers on-site at the foundry, and, in the case of NMB, for example, there are Vitelic engineers on-site.

There are several fully automated fabs in Japan, and we believe that almost all, except for possibly one, are dedicated single-product (or a small family of products), single-process fabs designed for high-volume production. On the other hand, there is yet no fully automated fab in the United States; the approach in the United States is to first develop the sophisticated software and then mechanize the fab later. U.S. fabs, when automated, will be flexible multiple-product, multiple-process fabs. However, we believe that the Japanese semiconductor manufacturers recognize the limitations of single-product, single-process fabs and are looking toward more flexible fabs. The U.S. semiconductor manufacturers have been extremely slow in their automation efforts. The question is, Will the Japanese manufacturers beat the U.S. manufacturers in building automated flexible fabs--the fabs of the future?

Joseph Grenier
Lane Mason



September Newsletters

The following is a list of material found in this section:

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH BULLETIN

SEMS Code: 1986-1987 Newsletters, September 1986-13

REVISION OF NORTH AMERICAN CAPITAL SPENDING FORECAST: THE DOWNWARD SLIDE IS ALMOST OVER

In our previous capital spending forecast, we noted both an optimistic and a less-than-optimistic scenario for capital spending in 1986. We have recently resurveyed North American semiconductor manufacturers and, unfortunately, the less-than-optimistic scenario is coming to pass (see Table 1). Therefore, this bulletin revises our previous forecast for merchant capital spending in North America.

One of the reasons for this revision is the third-quarter pause in the growth of IC shipments; the other reason is the continuing overcapacity in the industry. Capacity utilization in 1985 was an anemic 46 percent; in 1986 it will still be low, at approximately 56 percent (see Table 2). Our original forecast for 1986 merchant capital spending was $2,193 million, down 0.8 percent from our previous 1985 estimate. We are now revising that estimate to $1,926 million, down 16.0 percent from 1985.

We are also revising our estimate of captive semiconductor capital spending upward to $635 million in 1986. Overall, we expect merchant and captive capital spending in North America to be down 15 percent to $2,561 million (see Table 3).

In addition to capital spending in North America by North American companies, our forecast also now includes spending by all European, Japanese, and ROW companies in North America.

While this is the second year of decline in a row for the equipment industry, there is some solace in the fact that the rate of decrease in sales is lower than last year: 15 percent in 1986 versus 22 percent in 1985. The other good news is that we expect to see a 14 percent increase in merchant capital spending in 1987 to $2,189 million. Captive spending will also increase in 1987 to $722 million, up 14 percent. Total capital spending in 1987 will increase 14 percent to $2,911 million.

This growth will be fueled by growth in production in North America. Total production in North America by all companies (including those based in Europe, Japan, and ROW countries) will increase 15 percent in 1986 to $12,280 million and 21 percent in 1987 to $14,892 million (see Table 1).

Growth in capital spending will also be affected by an increase in equipment productivity, which will no longer slide downward but will begin to climb before the end of this decade. This change will be primarily due to the advent of computer-integrated manufacturing. Increased equipment productivity will have the effect of slowing the growth of capital spending. These changes will be explored in greater detail in forthcoming capital spending newsletters and service section revisions.

George Burns

Table 1

NORTH AMERICAN MERCHANT CAPITAL SPENDING
(Millions of Dollars)

	1985	1986	1987	1988	1989	1990	1991	CAGR 1985-1991
Semiconductor Production	$10,679	$12,280	$14,892	$19,317	$18,318	$21,037	$26,328	16%
Percent Change	(20%)	15%	21%	30%	(5%)	15%	25%	
Capital Spending	$ 2,291	$ 1,926	$ 2,189	$ 2,819	$ 2,464	$ 2,998	$ 3,647	8%
Percent Change	(25%)	(16%)	14%	29%	(13%)	22%	22%	

Table 2

CAPACITY UTILIZATION

	1984	1985	1986	1987	1988	1989	1990	1991
Percent of Capacity Used	84%	46%	56%	67%	90%	67%	75%	92%

Table 3

TOTAL NORTH AMERICAN CAPITAL SPENDING
(Millions of Dollars)

	1985	1986	1987	1988	1989	1990	1991	CAGR 1985-1991
Merchant	$2,291	$1,926	$2,189	$2,819	$2,464	$2,998	$3,647	8%
Captive	714	635	722	930	813	989	1,203	9%
Total	$3,005	$2,561	$2,911	$3,749	$3,277	$3,877	$4,850	8%
Percent Change	(22%)	(15%)	14%	29%	(12%)	18%	25%	

Source: Dataquest
September 1986

November Newsletters

The following material is a list of material found in this section:

- The Changing Landscape of Capital Spending

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: 1986-1987 Newsletters
1986-14

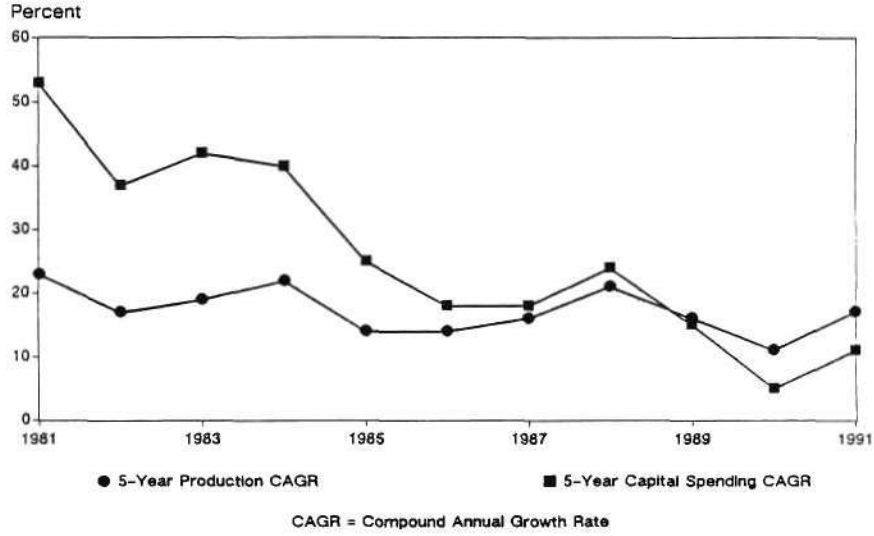
THE CHANGING LANDSCAPE OF CAPITAL SPENDING

INTRODUCTION

The familiar landscape in which equipment vendors have operated is changing. This new environment is shown in Figure 1, which shows the difference between five-year growth rates for both capital spending and production (worldwide, excluding captives). For the first five-year period ending in 1981, capital spending was growing at a rate that was 25 percent higher than the growth rate for production. For the five-year period ending in 1986, the growth rate of capital spending is only 5 percentage points higher than the growth rate of production. We believe that by the end of the decade, the growth rate of production will exceed the growth rate of capital spending. In other words, equipment productivity will increase, and because of this increase, equipment sales will not grow as fast as production.

Figure 1

GROWTH OF CAPITAL SPENDING COMPARED WITH PRODUCTION GROWTH



CAGR = Compound Annual Growth Rate

Source: Dataquest November 1986

There are other changes to note in the landscape. Capacity utilization is at an all-time low. At the same time, manufacturing is becoming more international than ever before. Japanese manufacturers will be building plants in regions outside of Japan; European and ROW manufacturers will be building and buying facilities in North America; and North American manufacturers will be doing the same.

Because a company's capital spending is no longer limited to spending within the borders of its country of origin, we are changing the way in which we report capital spending. Unless otherwise noted, regional capital spending will refer to spending within that region by all companies, regardless of where their home offices are located.

NORTH AMERICAN CAPITAL SPENDING

Our latest estimates for North American capital spending for property, plant, and equipment (PPE) are shown in Table 1. Overall, 1986 spending is expected to be down 16 percent from 1985. This percentage is close to what we had forecast at the beginning of the year. Of the two possible scenarios we presented at that time, the pessimistic one has come to pass. Advanced Micro Devices (AMD), National Semiconductor, and Thomson/Mostek are expected to decrease their spending by more than 40 percent. Those that will probably increase their spending this year include Philips-Signetics (40 percent), Fairchild (11 percent), General Electric (11 percent), and Intel (5 percent).

Table 1

ESTIMATED NORTH AMERICAN COMPANY CAPITAL SPENDING
(Millions of Dollars)

Company	1985 PPE	1986 PPE	Percent Change
AMD	$ 172	$ 91	(47%)
Analog Devices	64	44	(31%)
Fairchild	135	150	11%
General Electric	81	90	11%
Harris	40	40	0
Intel	214	225	5%
MMI	49	35	(28%)
Motorola	330	275	(17%)
National Semiconductor	184	104	(43%)
Philips-Signetics	50	70	40%
Texas Instruments	275	245	(11%)
Thomson-Mostek	39	21	(45%)
Others	695	536	(19%)
Total	$2,291	$1,926	(16%)

Source: Dataquest
November 1986

WORLDWIDE CAPITAL SPENDING

Our latest estimates for capital spending to 1991 are shown in Table 2.

Worldwide, capital spending in 1986 is expected to decline by 4.7 percent. However, different regions of the world will have different rates of decline and, in the case of ROW and Europe, there will be more growth. ROW countries, led by South Korea, are leading a charge to become major players on the world semiconductor scene and are forecast to grow 25 percent in 1986. We expect capital spending in Europe by European and North American companies also to increase in 1986, by a healthy 12.9 percent. Spending in North America by all companies will be down an estimated 16 percent in 1986. This is right in line with the low end of our forecast at the beginning of 1986.

In dollars, 1986 does not look bad for Japan, down a slight 0.6 percent. However, in yen, Japanese capital spending is down a lot: 30 percent from a previous year that was itself low.

We believe that 1987 will show some improvement, although it will be slight: 7.9 percent growth on a worldwide basis. Again, there will be variations between regions. We expect spending in ROW countries and Europe to lead the way with growths of 47.5 percent and 35 percent, respectively. Spending in North America is forecast to increase 13.7 percent in 1987. (Although this seems like a large percentage increase, it still does not bring spending up to 1985's level.) We expect spending in Japan to decline slightly in 1987; this will be the third consecutive year of declining Japanese capital spending.

Looking beyond 1987, our estimate of the compound annual growth rate (CAGR) for 1985 through 1991 is 11 percent. Again, we anticipate ROW countries and Europe to be the regions of the world where capital spending will grow at the highest rates. We forecast merchant capital spending in North America to grow at a CAGR of 8 percent. Spending by captives is expected to grow at a CAGR of 9 percent.

We expect Japan's capital spending to begin recovering in late 1987. Expressed in dollars and influenced by currency exchange rates, it will have a forecast CAGR of 10 percent from 1985 to 1991. However, expressed in yen, Japanese capital spending will only grow at an estimated CAGR of 2 percent from 1985 to 1991.

As a result of this, the Japanese industry will no longer gain a worldwide market share at the expense of North America. We expect both regions' shares of worldwide production to remain around 40 percent for the remainder of the decade.

Table 2

CAPITAL SPENDING FORECAST

	1980	1981	1982	1983	1984	1985	1986
Japanese Production	$3,856	$5,252	$5,584	$7,722	$12,007	$10,655	$14,292
Capital Spending	$ 639	$ 851	$ 931	$1,694	$ 3,570	$ 3,332	$ 3,311
Capital Spending/ Production	17%	16%	17%	22%	30%	31%	23%
Percent Change	55.7%	33.2%	9.5%	81.8%	110.8%	-6.7%	-0.6%
North American Production	$7,646	$7,267	$7,260	$8,850	$13,428	$10,679	$12,223
Capital Spending	$1,373	$1,349	$1,212	$1,452	$ 3,051	$ 2,291	$ 1,926
Capital Spending/ Production	18%	19%	17%	16%	23%	21%	16%
Percent Change	26.9%	-1.7%	-10.2%	19.8%	110.1%	-24.9%	-16.0%
European Production	$2,561	$2,237	$2,289	$2,434	$ 3,428	$ 3,150	$ 3,793
Capital Spending	$ 255	$ 283	$ 272	$ 421	$ 686	$ 581	$ 655
Capital Spending/ Production	10%	13%	12%	17%	20%	18%	17%
Percent Change	37.8%	11.0%	-3.9%	54.8%	62.9%	-15.3%	12.9%
ROW Production	$ 35	$ 45	$ 98	$ 170	$ 240	$ 339	$ 368
Capital Spending	$ 10	$ 20	$ 45	$ 91	$ 201	$ 220	$ 275
Capital Spending/ Production	29%	44%	46%	53%	84%	65%	75%
Percent Change	233.3%	100.0%	125.0%	102.2%	120.9%	9.6%	25.0%
Captive Capital Spending	0	$ 436	$ 423	$ 522	$ 806	$ 714	$ 635
North America	$1,373	$1,349	$1,212	$1,452	$ 3,051	$ 2,291	$ 1,926
Japan	639	851	931	1,694	3,570	3,332	3,311
Europe	255	283	272	421	686	581	655
ROW	10	20	45	91	201	220	275
Captive	0	436	423	522	806	714	635
Worldwide Capital Spending	$2,277	$2,940	$2,883	$4,179	$ 8,314	$ 7,138	$ 6,803
Percentage Change	351.%	29.1%	-1.9%	44.9%	98.9%	-14.1%	-4.7%

(Continued)

Table 2 (Continued)

CAPITAL SPENDING FORECAST

	1987	1988	1989	1990	1991	CAGR 1980 to 1991
Japanese Production	$16,555	$21,104	$21,253	$24,088	$29,181	18%
Capital Spending	$ 3,241	$ 4,254	$ 4,112	$ 4,745	$ 5,814	10%
Capital Spending/ Production	20%	20%	19%	20%	20%	
Percent Change	-2.1%	31.3%	-3.3%	15.4%	22.5%	
North American Production	$14,599	$18,923	$17,959	$20,638	$25,852	16%
Capital Spending	$ 2,189	$ 2,819	$ 2,464	$ 2,998	$ 3,647	8%
Capital Spending/ Production	15%	15%	14%	15%	14%	
Percent Change	13.7%	28.8%	-12.6%	21.7%	21.7%	
European Production	$ 4,734	$ 6,090	$ 5,890	$ 7,359	$ 8,936	19%
Capital Spending	$ 787	$ 1,062	$ 1,136	$ 1,363	$ 1,636	19%
Capital Spending/ Production	17%	17%	19%	19%	18%	
Percent Change	20.0%	35.0%	7.0%	20.0%	20.0%	
ROW Production	$ 510	$ 750	$ 827	$ 1,063	$ 1,305	25%
Capital Spending	$ 406	$ 606	$ 648	$ 810	$ 953	28%
Capital Spending/ Production	80%	81%	78%	76%	73%	
Percent Change	47.5%	49.2%	6.8%	25.0%	17.7%	
Captive Capital Spending	$ 722	$ 930	$ 813	$ 989	$ 1,203	9%
North America	$ 2,189	$ 2,819	$ 2,464	$ 2,998	$ 3,647	8%
Japan	$ 3,241	$ 4,254	$ 4,112	$ 4,745	$ 5,814	10%
Europe	$ 787	1,062	1,136	1,363	1,636	19%
ROW	406	606	648	810	953	28%
Captive	722	930	813	989	1,203	9%
Worldwide Capital Spending	$ 7,344	$ 9,671	$ 9,173	$10,905	$13,253	11%
Percentage Change	7.9%	31.7%	-5.2%	18.9%	21.5%	

Source: Dataquest
November 1986

CAPACITY UTILIZATION

In 1984, capital spending increased 99 percent over 1983. This, combined with the longest slump in the industry's history, has driven capacity utilization in both North America and Japan to record lows. Today, we estimate that capacity utilization in Japan is the lowest it has ever been: 63 percent. In North America, the capacity utilization hit 46 percent in 1985; in 1986, it rose to the less-than-Himalayan level of 56 percent.

The spending in Japan and North America has been cut severely in response to overcapacity. In North America, capital spending declined 25 percent in 1985 and 16 percent in 1986. Capital spending in Japan is down 30 percent in yen in calendar 1986. We expect it to fall another 9 percent in yen in calendar 1987.

Overcapacity has particular impact on capital spending in Japan because of the recent antidumping agreement. Under the agreement, prices for memories and microprocessors will be equal with their cost, and there will be a markup for profit. This selling price is called the foreign market value (FMV). The cost that is factored into the FMV is based on the variable cost and the amortized cost of capital per unit output. Therefore, the more equipment that a company has that is underutilized, the higher its amortized cost of capital per unit output. This will cause its FMV selling price to rise. At the higher FMV or required price, a company with excess capacity will lose market share and will therefore have even more excess capacity. FMV pricing, however, does not apply to devices made in facilities located in the United States.

The Japanese industry, therefore, has a special incentive to keep its excess capacity in Japan to a minimum. We expect that its spending as a percentage of revenue will decline from the 30 percent levels of 1984-85 to 21 percent in 1988.

Manufacturers in both regions are determined to get as much out of their equipment as they possibly can before they add more equipment. In both Japanese and English, the now-common phrase is: "Never again." Never again will manufacturers add so much capacity all at once. Their reaction to any increases in demand is likely to be much more cautious than in the past. We believe that this will be true for equipment to produce 1Mb and 4Mb devices. Manufacturers are likely to use existing equipment for 1Mb production and put off buying the next generation of equipment until it is needed for 4Mb production.

PRODUCTIVITY AND CAPACITY

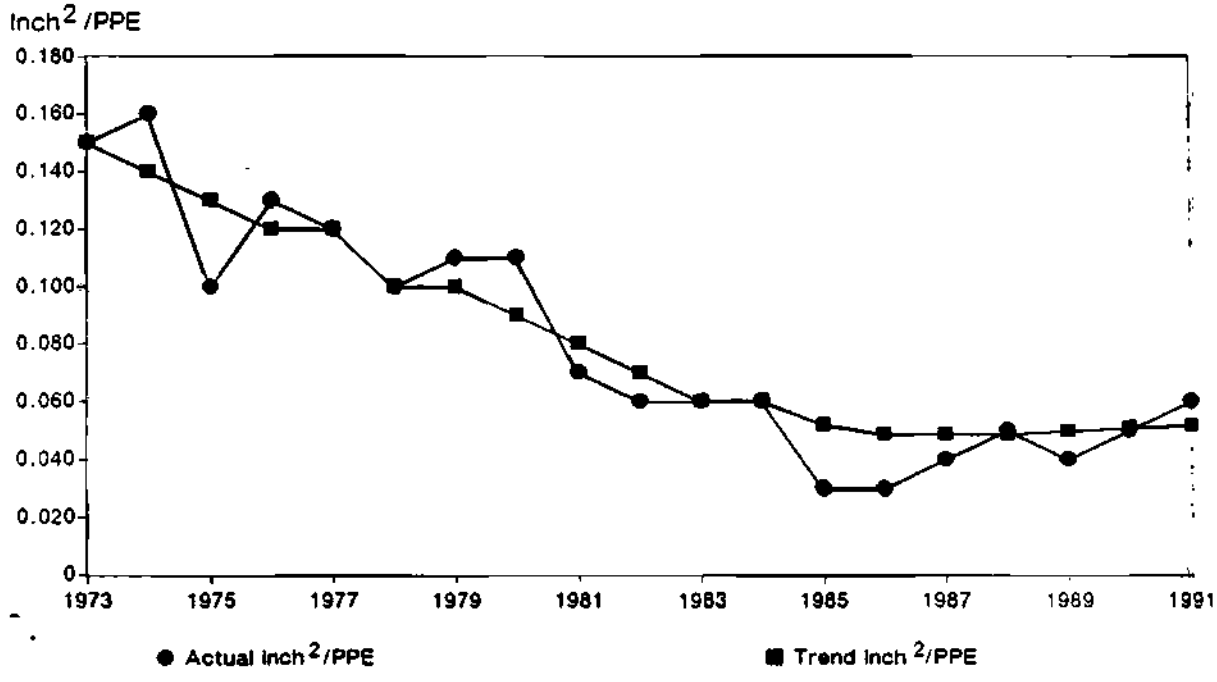
The expenditures that semiconductor manufacturers are making and will continue to make are those to increase equipment and process productivity; that is, to increase equipment reliability, utilization, throughput, and device yields. We believe that expenditures for productivity-increasing

equipment (such as inspection equipment) and for automation (for both increased cleanliness and real-time control) will increase much faster than expenditures for other types of equipment.

Historically, equipment productivity (which we define as square inches of silicon output per dollar value of PPE) has shown a long-term trend to decline. However, because of the focus on productivity, we believe that the downward slope in equipment productivity is now in the process of changing its direction (see Figure 2). Because of this change of slope, the landscape in which equipment vendors operate will be different from the past; equipment sales will not grow as fast as production.

Figure 2

EQUIPMENT PRODUCTIVITY
(Square inches/$PPE)



Source: Dataquest
November 1986

PRODUCTION

Production is one of the basic forces that shape capital spending. Capital spending is a derived demand. If semiconductor end users do not have a strong demand for their products, this will also weaken the demand for capital equipment. We believe that the dollar value of semiconductor production will increase 19 percent in 1987 in nominal terms. (However, when the effects of continuing yen appreciation relative to the dollar are factored out, worldwide growth in 1987 will only be 15 percent.)

There are several reasons for our (cautious) optimism about production in the upcoming year. We believe that the end-user market for semiconductors will grow in 1987. Business and technical computers and PCs are expected to experience some growth, however slight; telecommunications, computer storage, printers, CAD/CAM, and software are expected to experience more robust growth. The growth of these end-use markets will not only stimulate demand directly, it will have the additional effect of stimulating demand indirectly as end-use manufacturers and distributors strive to increase the absolute levels of their inventories. In addition to the effects of growing end markets, we believe that the dollar value of production will be up in 1987 because of the increased prices causd by the recent antidumping agreement.

The landscape in which production takes place is also changing. Historically, production in Japan was done by Japanese companies. Now, Texas Instruments and Motorola have significant fabrication presence in Japan. Similarly, fabrication in North America was done by North American-based companies. This too is changing. NEC has fabs in Roseville, California, and in Livingston, Scotland; and Fujitsu has just acquired majority interest in Fairchild. Philips owns Signetics and Thomson owns Mostek. Philips, in a joint venture with ERSO and local Taiwanese companies, is building a $200 million fab in Taiwan. We expect these trends to continue.

As manufacturers try to have manufacturing presence close to the markets where their devices are consumed, the growth of regional consumption is expected to differ increasingly from growth of regional production. In North America, for example, Dataquest expects consumption for 1985 through 1991 to grow at a CAGR of 12 percent. Merchant production in North America, on the other hand, is forecast to grow at a rate of 16 percent. This faster growth rate for production in North America is due to the growing presence of foreign-based manufacturers in North America and to U.S. manufacturers exporting more of their products.

The recent antidumping agreement will not only have an effect on capacity as discussed earlier, but it will also influence where Japanese capital spending dollars are spent. We believe that the Japanese will build more fabs in North America, since as mentioned earlier, FMV pricing does not apply to devices made in Japanese facilities located in the United States.

JAPAN AND NORTH AMERICA

Japan and North America together represented 79 percent of the world-wide capital spending in 1985. Even though their forecast growth rates between now and 1991 will be less than ROW countries and Europe, we expect that they will still account for more than 70 percent of the spending in 1991. They are big; they merit special attention.

As discussed earlier, both regions have capacity utilization rates that are low. However, although the two regions are similar in utilization rates, they differ in the relative ages of their plants.

From 1984 through 1986, spending in Japan will have outpaced spending in North America by 40 percent. More capital equipment has been installed in Japan since 1984 than in North America. Of the installed base in the two regions, 75 percent of Japan's base has been installed since the beginning of 1984, compared with 64 percent for North America. In other words, there is less new, state-of-the-art capacity in North America than in Japan. Consequently, North American manufacturers will have to buy state-of-the-art capacity sooner than manufacturers in Japan, and it will be North America that will lead the equipment industry out of its current trough.

An important difference between Japan and North America is the productivity of capital. While each region's share of production in 1991 will be approximately equal, the Japanese capital spending to support that production will be significantly higher. When we look at installed base, we see the same story: the revenue-per-dollar value of property, plant, and equipment is less in Japan than in North America. The reason for this difference is twofold: first, the product mix of the Japanese industry commands a lower average selling price. And secondly, Japanese industry is in a societal and governmental environment that protects it from risk.

Japanese semiconductor manufacturers exist within large, vertically integrated electronics companies. These companies are in turn part of large banking groups or associations. They have significantly higher debt/equity ratios than their North American counterparts. Therefore, Japanese manufacturers feel less pressure from stockholders and others when making strategic decisions. Furthermore, the Japanese government, through MITI, provides capital and R&D incentives that decrease a company's risk. Therefore, Japanese companies are able to pay less in risk premiums or interest rates than their North American counterparts.

DATAQUEST CONCLUSIONS

Capital spending is driven by production and capacity utilization. As production rises and falls, so does capital spending. As production moves from one region to the other, so does capital spending. U.S. companies will be manufacturing in Japan; Japanese and European companies

will be manufacturing in North America. As semiconductor manufacturing becomes global, structural differences, such as those that exist between Japan and the United States, may become harder to maintain. For example, Japanese companies may use their increased manufacturing presence in North America to learn the more flexible manufacturing processing techniques that U.S. manufacturers use to address higher-margined markets such as ASICs. This would increase the capital productivity of Japanese companies, which historically has not been as high as the capital productivity of U.S. companies.

Productivity is the key to equipment sales in this new landscape. Expenditures that increase reliability, utilization, and yield are the expenditures that semiconductor manufacturers can justify. Expenditures that only add to capacity without increasing productivity will be difficult to justify over the next few years.

George Burns

Dataquest

Conference Schedule

1986

Semiconductor	October 20–22	Hotel Inter-Continental San Diego, California
Technical Computer	November 3–5	Silverado Country Club Napa, California
Asian Peripherals	November 5–7	Hotel Okura Tokyo, Japan
Semiconductor Users/ Semiconductor Application Markets	November 10	Sheraton Harbor Island San Diego, California
Electronic Publishing	November 17–18	Westin Copley Place Boston, Massachusetts
CAD/CAM EDA	December 4–5	Santa Clara Marriott Santa Clara, California

1987

Semiconductor Users/ Semiconductor Application Markets	February 4–6	Saddlebrook Resort Tampa, Florida
Copying and Duplicating	February 23–25	San Diego Hilton Resort San Diego, California
Electronic Printer	March 23–25	Silverado Country Club Napa, California
Japanese Semiconductor	April 13–14	The Miyako Kyoto, Japan
Telecommunications	April 13–15	Silverado Country Club Napa, California
CAD/CAM	May 14–15	Hyatt Regency Monterey Monterey, California
Display Terminals	May 20–22	San Diego Hilton Resort San Diego, California
European Semiconductor	June 4–5	Palace Hotel Madrid, Spain
European Copying and Duplicating	June 25–26	The Ritz Hotel Lisbon, Portugal
Financial Services	August 17–18	Silverado Country Club Napa, California
Western European Printer	September 9–11	Palace Hotel Madrid, Spain
European Telecommunications	October 1–2	Monte Carlo, Monaco
Semiconductor	October 19–21	The Pointe Resort Phoenix, Arizona
Office Equipment Dealers	November 5–6	Hyatt Regency Monterey, California
Electronic Publishing	November 16–17	Stouffer Hotel Bedford, Massachusetts
CAD/CAM EDA	December 10–11	Santa Clara Marriott Santa Clara, California

Dataquest

Product Offerings

Industry Services

Business Computer Systems
CAD/CAM
Computer Storage—Rigid Disks
Computer Storage—Flexible Disks
Computer Storage—Tape Drives
Copying and Duplicating
Display Terminal
Electronic Printer
Electronic Publishing
Electronic Typewriter
Electronic Whiteboard
European Semiconductor*
European Telecommunications
Gallium Arsenide
Graphics
Imaging Supplies
Japanese Semiconductor*
Office Systems
Personal Computer
Personal Computer—Worldwide Shipments and Forecasts
Robotics
Semiconductor*
Semiconductor Application Markets*
Semiconductor Equipment and Materials*
Semiconductor User Information*
Software—Artificial Intelligence
Software—Personal Computer
Software—UNIX
Technical Computer Systems
Technical Computer Systems—Minisupercomputers
Telecommunications
Western European Printer

Executive and Financial Programs

Corporate Alliance Program
Coporate Technology Program
Financial Services Program
Strategic Executive Service

Newsletters

European PC Monitor
First Copy
Home Row
I.C. ASIA
I.C. USA

Focus Reports

The European PC Market 1985-1992
European PC Retail Pricing
PC Distribution in Europe
PC Software Markets in Europe
PC Local Area Networking Markets in Europe
The Education Market for PCs in Europe
Japanese Corporations in the European PC Markets
Home Markets for PCs in Europe
Integrated Office Systems—The Market and Its Requirements
European Market for Text Processing
Image Processing in the Office
Work Group Computing
Translation Systems
Vendor Support
The IBM 3270 Market: 1986 and Beyond
Korean Semiconductor Industry Analysis
Diskettes—The Market and Its Requirements

Directory Products

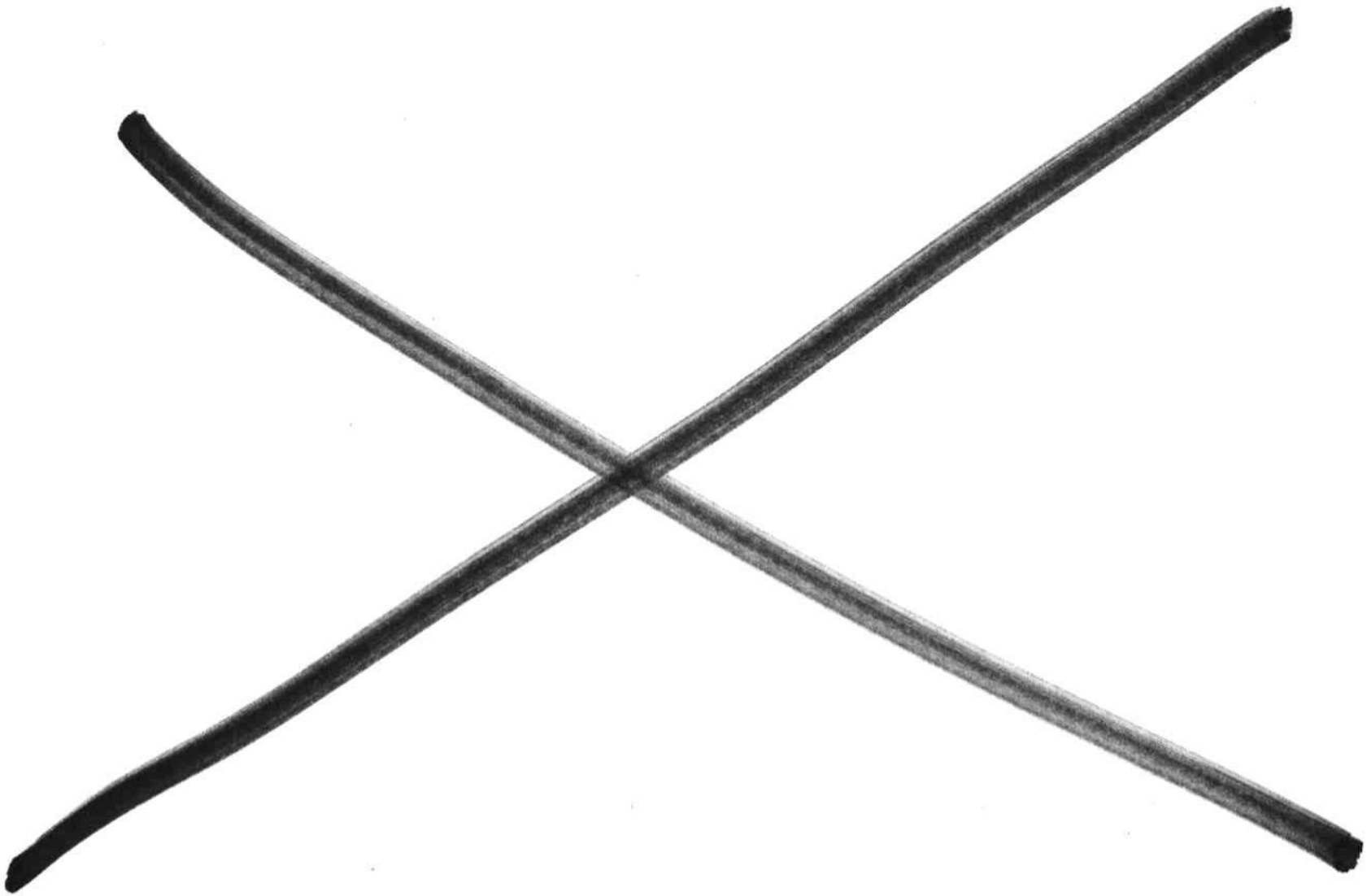
I.C. Start-Ups—1987
SpecCheck—Competitive Copier Guide
SpecCheck—Competitive Electronic Typewriter Guide
SpecCheck—Competitive Whiteboard Guide
Who's Who in CAD/CAM 1986

Future Products

- Industry Services
  - Manufacturing Automation
  - Computer Storage—Optical
  - Computer Storage—Subsystems
- Focus Reports
  - Japanese Printer Strategy
  - Japanese Telecommunications Strategy
  - Canon CX Laser—User Survey
  - Digital Signal Processing
  - PC-based Publishing
  - Taiwan Semiconductor Industry Analysis
  - China Semiconductor Industry Analysis
  - PC Distribution Channels
- Directory Products
  - SpecCheck—Competitive Facsimile Guide
  - SpecCheck—Competitive Electronic Printer Guide

*On-line delivery option available

For further information about these products, please contact your Dataquest sales representative or the Direct Marketing Group at (408) 971-9661.



1985 SEMM NEWSLETTERS

Semiconductor Equipment and Materials Service 1985–1986 Newsletters and Bulletins

Dataquest
a company of The Dun & Bradstreet Corporation

1290 Ridder Park Drive
San Jose, California 95131
(408) 971-9000
Telex: 171973
Fax: (408) 971-9003

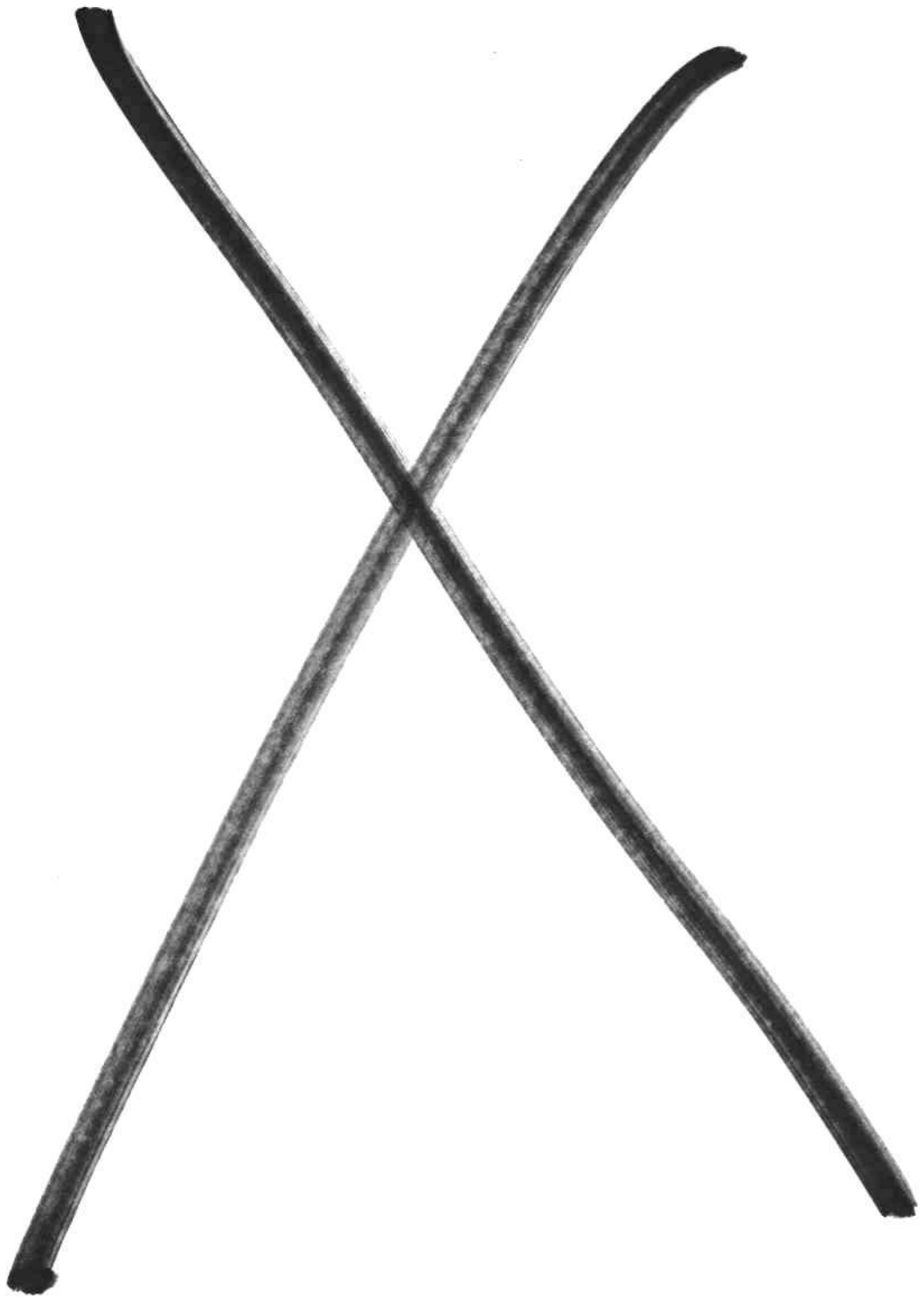
Sales/Service offices:

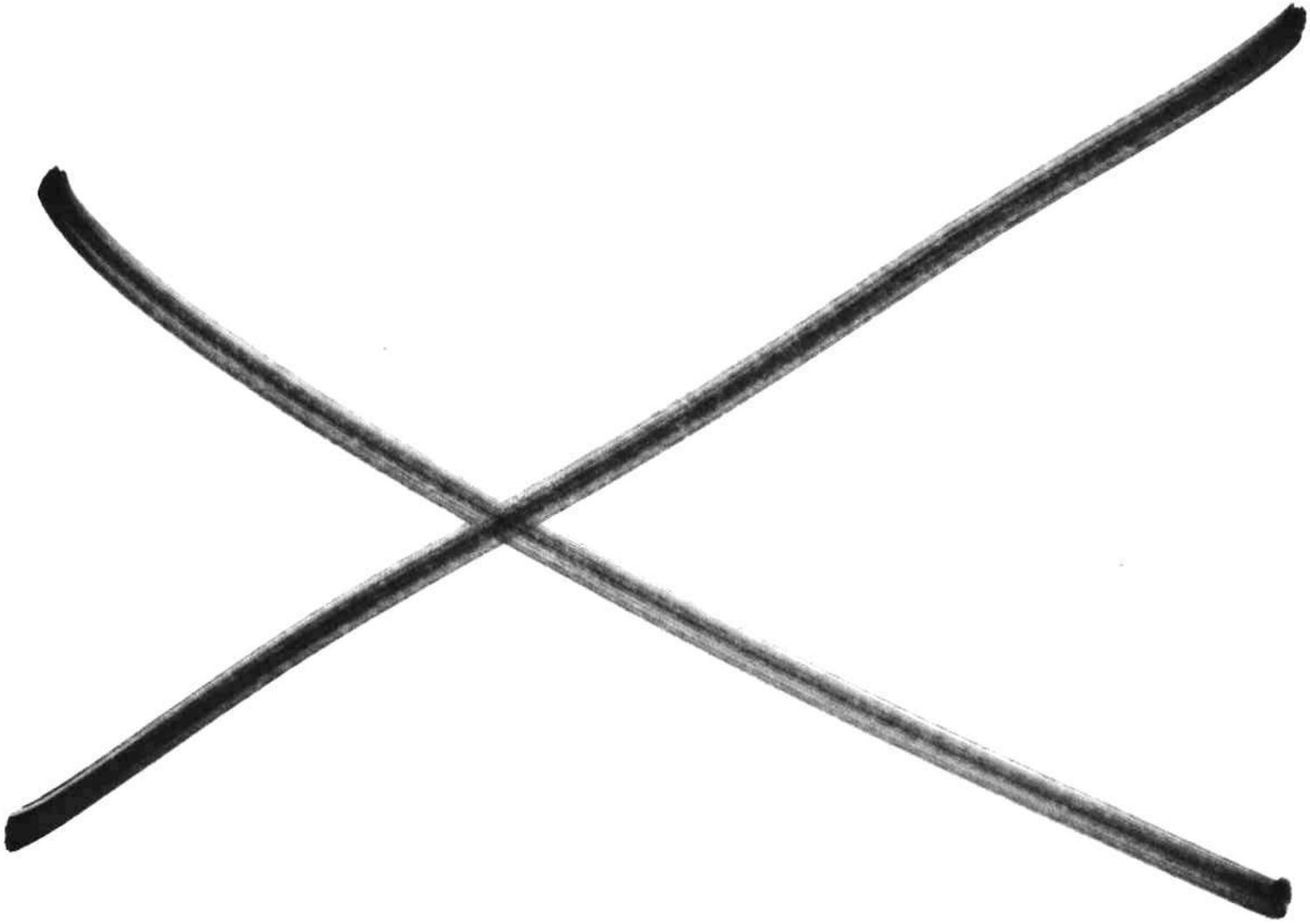
UNITED KINGDOM
DATAQUEST UK Limited
144/146 New Bond Street
London W1Y 9FD
United Kingdom
(01) 409-1427
Telex: 266195
Fax: (01) 491-2790

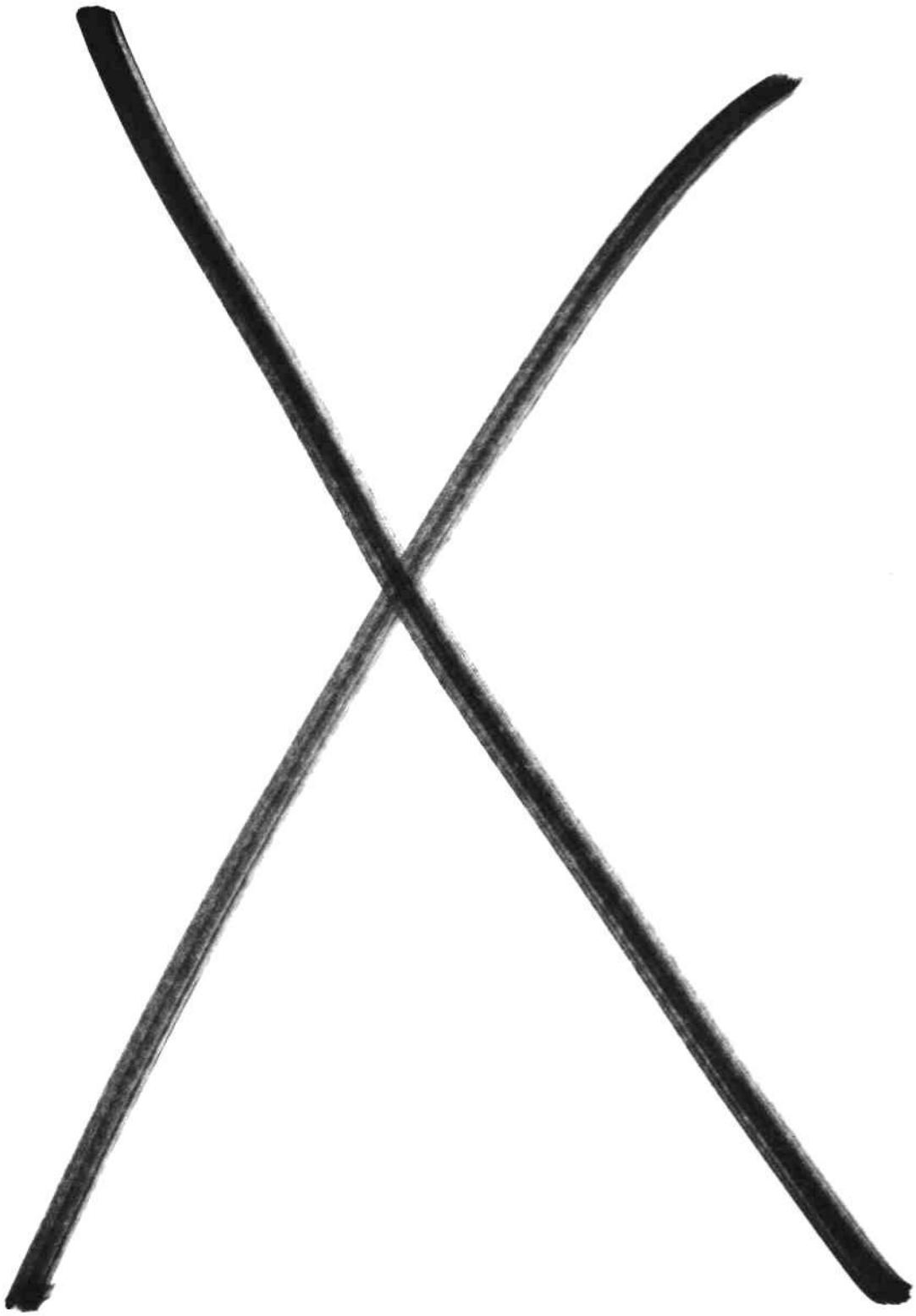
GERMANY
DATAQUEST GmbH
Rosenkavalierplatz 17
D-8000 Munich 81
West Germany
(089) 91-1064
Telex: 5218070
Fax: (089) 91-2189

FRANCE
DATAQUEST SARL
41, rue Ybry
92522 Neuilly-sur-Seine Cedex
France
(1)47.58.12.40
Telex: 630842
Fax: (01)46.40.11.23

JAPAN
DATAQUEST Japan, Ltd.
Taiyo Ginza Building
7-14-16 Ginza, Chuo-ku
Tokyo 104, Japan
(03) 546-3191
Telex: J32768
Fax: (03) 546-3198







April Newsletters

The following is a list of the material in this section:

April Newsletters

(Page intentionally left blank)

Nielsen Dataquest RESEARCH NEWSLETTER

SEMS Code: 1985 Newsletters: April

SEMICON EUROPA 1985--A MOOD OF OPTIMISM

INTRODUCTION

The European-owned semiconductor equipment and materials industry is coming of age. With the recent emergence of many equipment and materials suppliers, the European-owned industry is becoming more and more capable of meeting the needs of the European semiconductor production industry. The situation in Europe today is reminiscent of the situation in Japan several years ago when the Japanese equipment and materials industry was also coming of age.

The mood of the European suppliers is one of optimism, compared to the more pessimistic mood currently prevailing in the United States. This optimism springs from the aggressive investment plans announced by the European-owned semiconductor companies as they attempt to regain lost world semiconductor production market share. As a result, the above-average European capital spending projected over the next five years provides opportunities for the further emergence and growth of the local equipment and materials industry as well as market opportunities for the U.S. and Japanese suppliers that have in place the proper infrastructures.

OVERVIEW

The 1985 SEMICON Europa show was held for the eleventh consecutive year at the Zuspa Convention Center in Zurich, Switzerland, on March 12-14. Organized by the Semiconductor Equipment and Materials Institute (SEMI), SEMICON Europa is one of six strategically located shows sponsored annually by SEMI. Table 1 gives the locations and dates for this year's other shows.

SEMICON Europa has become the most important show in Europe for the semiconductor equipment and materials industry, allowing them to showcase their products and technological advancements to the European semiconductor manufacturers. In addition, the show provides a valuable opportunity for equipment and materials manufacturers, particularly the American companies, to interact with the European device makers.

Table 1

SEMICON SHOW LOCATIONS

Show	Location	1985 Dates
SEMICON Europa	Zurich, Switzerland	March 12-14
SEMICON West	San Mateo, California	May 21-23
SEMICON Osaka	Osaka, Japan	June 25-26
SEMICON East	Boston, Massachusetts	September 17-19
SEMICON Southwest	Dallas, Texas	October 22-24
SEMICON Japan	Tokyo, Japan	December 5-7

Source: SEMI

SHOW REVIEW

This year's attendance reached a record 5,500 (last year's attendance was 5,000). Traditionally, attendance at SEMICON Europa is low compared with attendance at SEMICON West or SEMICON Japan. There are several reasons for this. First, European semiconductor production, including production by both European- and U.S.-owned companies, represents only a 12 percent share of the worldwide semiconductor production market. Second, unlike in Japan or the United States, where the semiconductor industries tend to be concentrated near the show sites, semiconductor production in Europe is dispersed (with the exception of Silicon Glen in Scotland) and, therefore, European companies tend to be more selective about who they send to attend the show. Consequently, the attendees at SEMICON Europa are generally decision makers and key people in their companies.

Approximately 355 equipment and materials companies exhibited their products this year--55 more than in 1984. Of the 355 companies, almost one-third were European-owned and are now manufacturing products for most areas of IC manufacturing. Table 2 lists the major European-owned companies that exhibited in the areas of maskmaking, silicon supply, and wafer fabrication and assembly equipment. A few companies that did not exhibit are included to give an overall perspective of the industry. European-owned companies that produce photoresists, chemicals, and gases are not included in Table 2, although these areas were amply represented at the show.

Table 2

EUROPEAN-OWNED SEMICONDUCTOR EQUIPMENT AND MATERIALS COMPANIES EXHIBITING AT SEMICON EUROPA 1985

Company	Location	Comments
Maskmaking		
Nanomask	France	
Compugraphics	Scotland	
CSEM	Switzerland	
IC Masks[1]	England	
SAC[4]	England	
Silicon Suppliers		
Wacker-Chemitronic	West Germany	Wafers and Polysilicon
Dynamit Nobel Silicon	Italy	
Topsil	Denmark	Float Zone Silicon
Rhone Siltec[2]	France	
ICI Wafer Technology	England	III-V Materials Only
Wafer Fabrication Equipment		
Philips	The Netherlands	Stepper, E-Beam Lithography
Karl Suss	West Germany	Contact/Proximity Aligner
Sulzer Electro-Technique	France	Contact Aligner, Laser Wafer Marker
Censor[3]	Liechtenstein	Stepper
Balzers	Liechtenstein	Sputtering, Evaporation, Dry Etch, Ion Implantation
CIT Alcatel	France	Dry Etch, Deposition
Nordiko	England	Sputtering, Dry Etch
Plasma Technology	England	Dry Etch/Strip, PECVD
AET	France	Dry Etch/Strip, Rapid Anneal
Technics	West Germany	Dry Etch/Strip
Plasma-Electronic	West Germany	Dry Etch/Strip, PECVD
E.T. Electrotech	England	Dry Etch, Sputtering, PECVD
Wellman Furnaces	England	Diffusion Furnace, LPCVD
Centrotherm	West Germany	Diffusion Furnace
Helmut Sier Electronic	Switzerland	Diffusion Furnace, Strip
Semy Engineering	France	Diffusion Furnace, LPCVD, PECVD
ASM	The Netherlands	Diffusion Furnace, LPCVD, PECVD, 4-Point Probe

(Continued)

Table 2 (Continued)

EUROPEAN-OWNED SEMICONDUCTOR EQUIPMENT AND MATERIALS COMPANIES EXHIBITING AT SEMICON EUROPA 1985

Company	Location	Comments
Wafer Fabrication Equipment (Continued)		
Timesa Microelectronics	Switzerland	Epitaxial Reactor
ISA Riber	France	Molecular Beam Epitaxy, Surface Analysis
Slee Semiconductor Equipment	England	Photoresist Processing, Wet Benches
SAPI Plastiques	France	Wet Benches
Convac	West Germany	Photoresist Processing, Wafer Inspection
Zeiss	West Germany	Wafer Inspection
Leitz	West Germany	Wafer Inspection, SEM
Wild Heerbrugg	Switzerland	Wafer Inspection
Vickers	England	Line Width Measurement
Sagax	Sweden	Ellipsometer
Cambridge Instruments[4]	England	MOCVD, SEM, E-Beam Lithography, Reticle and Wafer Inspection
Laser Optronic	West Germany	Laser Wafer Marker
Eichhorn & Hausmann	West Germany	Wafer Measurement
Assembly		
Foton	West Germany	Die/Wire Bonder
Sulzer Electro-Technique	France	Prober, Die Bonder, Die Sort
Gustav Wirz	Switzerland	Die Bonder, Die Sort
Adelco	Switzerland	Wire Bonder
Farco	Switzerland	TAB, Wafer Dicer
Slee Semiconductor Equipment	England	Encapsulation
ESEC	Switzerland	Die/Wire Bonder, Wafer Dicer
Cryophysics	Switzerland	Laser Marking
Karl Suss	West Germany	Wafer Dicer, Prober
ASM	The Netherlands	Die/Wire Bonder, Encapsulation
Dage	England	Die Separation

(Continued)

Table 2 (Continued)

EUROPEAN-OWNED SEMICONDUCTOR EQUIPMENT AND MATERIALS COMPANIES EXHIBITING AT SEMICON EUROPA 1985

Company	Location	Comments
Test		
Deltest[4]	England	Linear Tester
Siemens[4]	West Germany	LSI Tester
Schlumberger[4]	France	Sentry Tester
Enertec[4]	France	

[1]Joint venture between TRE and Imperial Chemical Industries
[2]Joint venture between Rhone-Poulenc and Siltec
[3]Purchased by Perkin-Elmer in 1984
[4]Did not exhibit at SEMICON Europa

Source: DATAQUEST
April 1985

As the table indicates, European companies are well represented in the area of maskmaking. In addition to the five European-owned facilities, an American company, Align-Rite, has recently established a maskmaking facility in Wales. European-owned companies are also well represented in silicon wafer supply. Wacker-Chemitronic is the leading silicon wafer supplier in Europe and the world leader in polysilicon supply. Monsanto, an American company, is the number two wafer supplier in Europe, but does not presently manufacture wafers in Europe. Monsanto will build a silicon facility in the United Kingdom in 1985. Rhone-Siltec, a joint venture based in France between Rhone-Poulenc and Siltec, will begin silicon wafer shipments in 1985.

In the area of front-end wafer fabrication equipment, European-owned companies are well represented in lithography, physical vapor deposition, chemical vapor deposition, dry etch, and diffusion. They are singly represented in automatic photoresist processing equipment (Convac), rapid anneal (AET), and epitaxy (Timesa Microelectronics). Balzers is currently the only manufacturer of ion implantation equipment and currently provides equipment only by special order. European companies are also represented in the areas of reticle and wafer inspection, wafer measurement, surface analysis, and laser wafer marking.

In back-end equipment, there were several European-owned companies exhibiting assembly equipment. There were no companies exhibiting IC device test systems, although there are at least four European companies manufacturing test systems, as shown in Table 2.

It is apparent that the European semiconductor equipment and material industry has emerged from a nascent, formative stage in which there were relatively few suppliers to a growing local industry of many suppliers who are becoming more and more capable of meeting the needs of the European semiconductor manufacturers. Thus, the American and Japanese suppliers who hope to do business in Europe will have tougher local competition in the future. DATAQUEST believes that the American suppliers, in particular, may have to reassess their marketing strategies in Europe if they wish to maintain their market shares against the growing local competition. For instance, American companies that have well-developed sales and service infrastrutures in Europe will have a better opportunity to maintain or increase market share against the rising local competition than those companies that do not have established infrastructures.

Another consideration is the strong dollar, which makes imported American equipment more expensive than locally manufactured products. American companies that have European manufacturing facilities will be better positioned in the European marketplace than those that do not manufacture locally.

Japanese suppliers currently do not have a large presence in Europe and only 12 Japanese companies exhibited at SEMICON. DATAQUEST believes that this minimal attention to the European market is primarily due to the Japanese suppliers' focusing on their own rapidly growing market in Japan. In addition, the Japanese suppliers have directed their export activities to the United States where capital spending has also grown rapidly. Table 3 shows the estimated capital spending by Japanese, American, and European semiconductor manufacturers in 1983, 1984, and 1985.

Table 3

ESTIMATED MERCHANT
SEMICONDUCTOR MANUFACTURERS' WORLDWIDE CAPITAL SPENDING
(Millions of Dollars)

	1983	1984	1985
Japanese Companies	$1,902	$3,278	$3,362
U.S. Companies	1,452	2,909	2,934
European Companies	300	650	600
Total	$3,654	$6,837	$6,896

Source: DATAQUEST
April 1985

As can be seen from Table 3, European capital expenditures are at a relatively low level compared with American and Japanese spending. Actual investment in Europe is somewhat higher than the European company expenditures shown in Table 3 because of investment by American and Japanese companies in their European facilities. The smaller European capital market has been the major factor shaping the marketing strategy of both Japanese and American suppliers.

Nevertheless, the Japanese are stepping up their activities in Europe. For instance, Nikon opened a European office in January 1985, Canon has begun marketing its stepper in Europe (it has been marketing its proximity and projection aligners for some time), and Shin-Etsu Handotai (SEH) has announced plans to build a wafer facility in Scotland in 1985. DATAQUEST believes that there are two reasons for the Japanese to increase their marketing presence in Europe. First, the Japanese IC manufacturers have several front-end facilities planned for Europe over the next few years. Their facilities will likely be equipped with Japanese equipment to facilitate process transfer and, consequently, a network of Japanese service offices will be developed to support this equipment. DATAQUEST believes that the Japanese will increase their marketing activities once a solid service network is formed. The Japanese are very cautious in this regard and do not attempt to penetrate a market unless a solid infrastructure is in place.

The second reason for the Japanese (and Americans) to increase their activities in Europe is the projected growth of the European semiconductor industry over the next five years. This will be discussed in more detail in the next section.

A MOOD OF OPTIMISM

The mood at SEMICON Europa was definitely upbeat and encouraging, and the equipment and materials suppliers were overhwelmingly optimistic about 1985 and beyond. Many of the companies surveyed expected 1985 revenues to be up 20 percent or more over 1984, and 1985 to be their best year ever. This optimism is in stark contrast to the mood in the United States, where device manufacturers are tightening their belts. DATAQUEST forecasts that 1985 U.S. semiconductor consumption will be down 3.2 percent from 1984. U.S. device manufacturers are cutting back on their planned 1985 capital expenditures such that U.S. capital expenditures for 1985 will be essentially at 1984 levels (Table 3). As a result, U.S. equipment and materials suppliers are experiencing a slowdown in orders, delivery push-outs, and in some cases, cancellations of orders. In contrast, DATAQUEST forecasts that the European semiconductor market will grow about 8 percent in 1985 as the Europeans pursue their goal of regaining worldwide semiconductor production market share.

Thus, the main reason for optimism is the recent aggressive capital spending plans announced by the European-owned semiconductor companies. In 1978, European-owned semiconductor production accounted for 14 percent of worldwide production; but since then, the European share has steadily

eroded to a low of 9 percent in 1984 (the total European production market share of 12 percent includes 3 percent contributed by U.S.-owned companies). This erosion was due mainly to a lower level of capital spending by the European companies compared with that of the U.S. or Japanese companies. However, the European companies have begun to invest more aggressively in their attempt to regain lost market share and are expected to continue above-average capital investment through the 1980s.

As a result, DATAQUEST believes that 1984 represents a turning point for the European-owned semiconductor companies. The low 9 percent share of world production recorded by the European companies in 1984 represents the nadir of their decline in world market share. DATAQUEST believes that the European market share will steadily increase over the next five years as the European companies recover their lost market share with their above-average investment plans.

Table 4 shows European production by European-owned, U.S.-owned, and Japanese-owned companies. In 1984, European companies produced $2.2 billion; DATAQUEST forecasts that they will produce $6.6 billion in 1989. Note that the European-owned companies are expected to triple their production by 1989, while the U.S.-owned companies are expected to only double their production in Europe by the same time. In 1984, production by U.S.-owned companies was 31 percent of total Europe production, but this is expected to fall to 22 percent by 1989 as European and Japanese facilities come on-line. Net imports are estimated to fall from 33 percent in 1984 to 13 percent in 1989.

Table 4

ESTIMATED SEMICONDUCTOR PRODUCTION IN EUROPE

	1984		1989		CAGR 1984-1989
European Companies	$2.2	69%	$ 6.6	71%	24.7%
U.S. Companies	1.0	31	2.1	22	16.0
Japanese Companies	-	-	0.7	7	N/M
Total European Production	$3.2	100%	$ 9.4	100%	24.5%
Net Imports	1.6		1.4		
European Consumption	$4.8		$10.8		17.7%

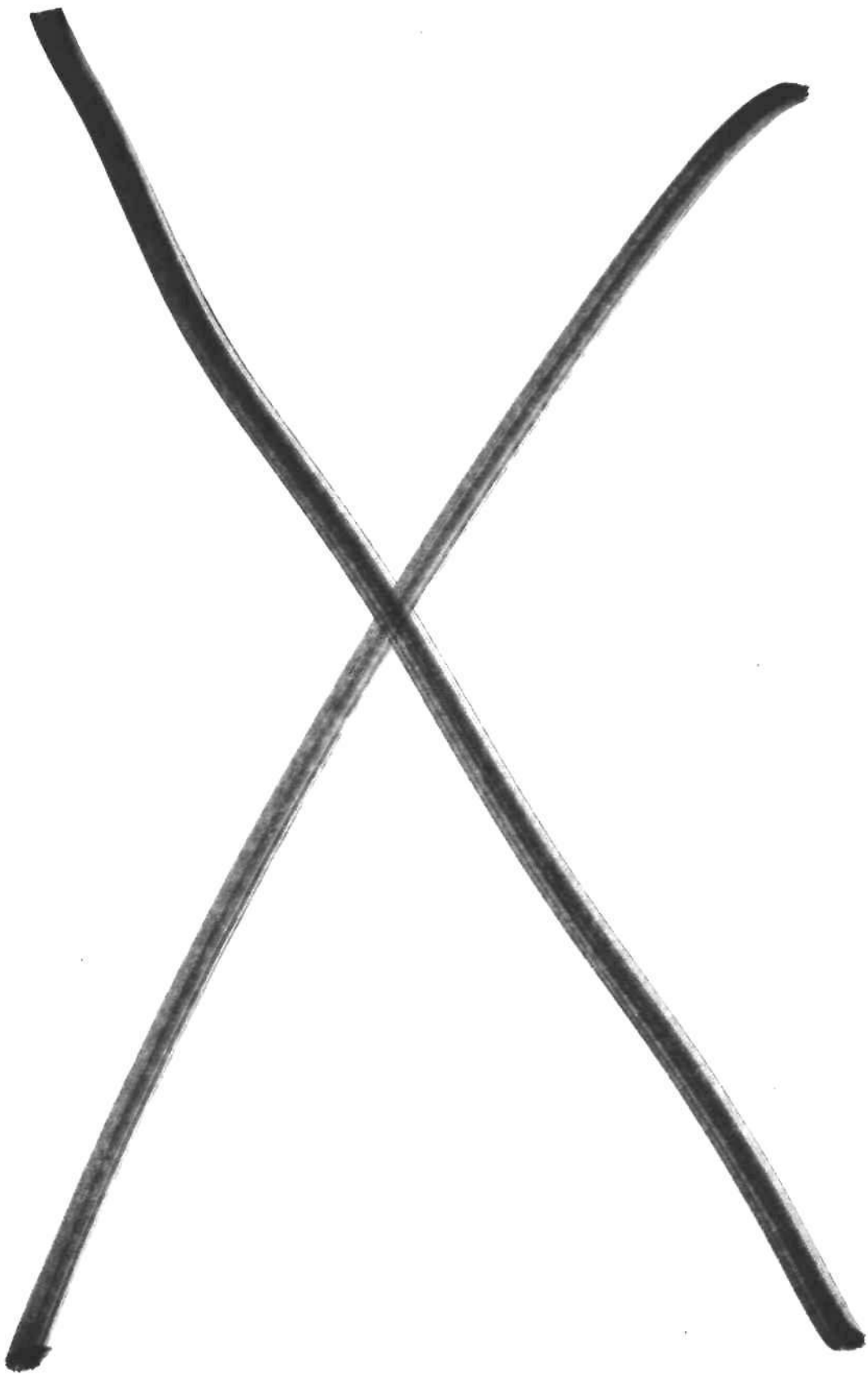
N/M = Not Meaningful

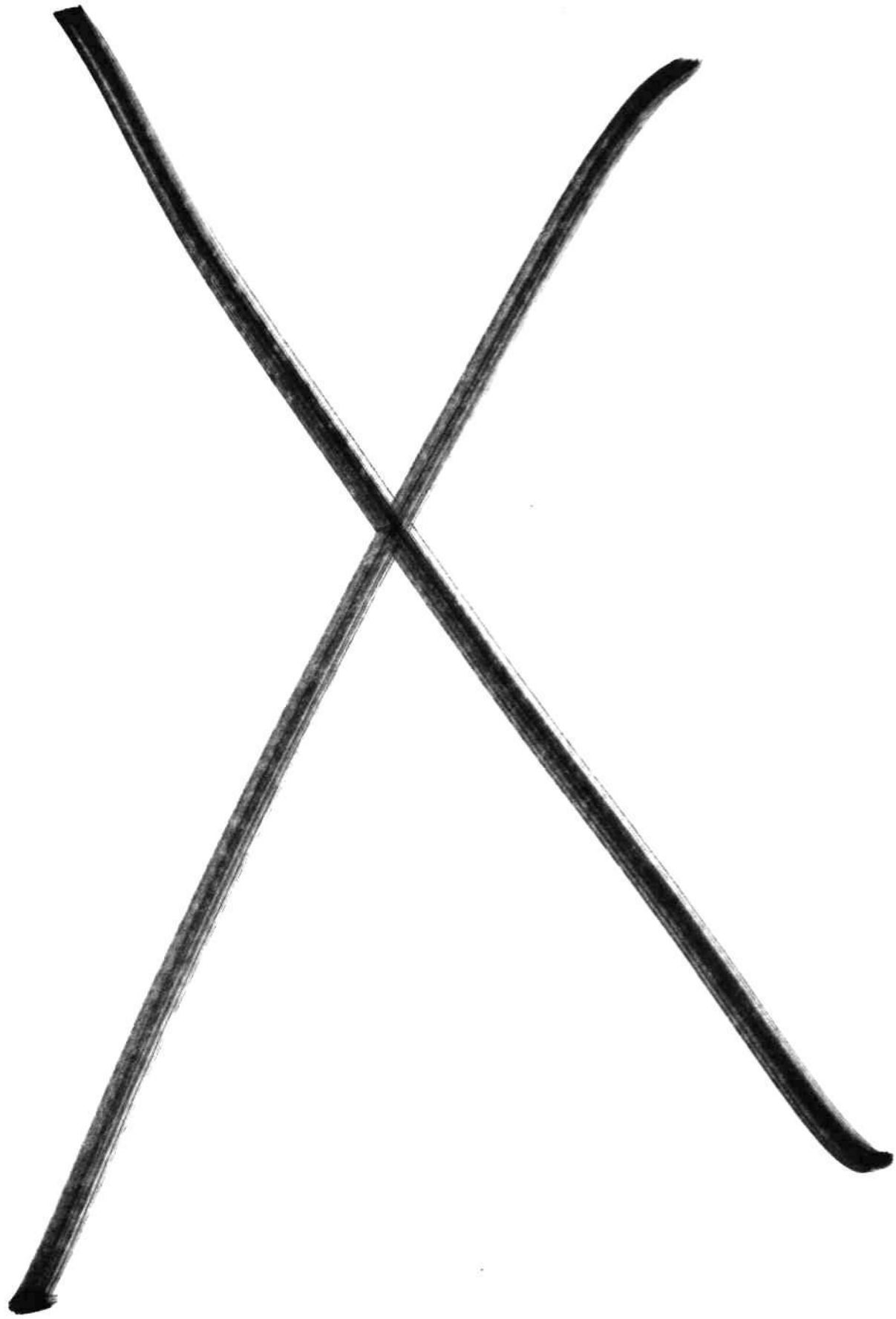
Source: DATAQUEST
April 1985

Total European production will grow from $3.2 billion in 1984 to $9.4 billion in 1989. To meet this $6.2 billion increase in production, substantial new capacity needs to be added over the next five years. DATAQUEST estimates that to meet these capacity requirements, 60 new facilities will have to be added, representing a capital investment of about $4.5 billion.

Of the 60 new facilities needed, 48 have already been announced or planned or are in progress and will be installed in Europe by the end of 1987. An additional 12 announcements are anticipated within the next 18 months. Twenty-eight of the new facilites will be European-owned, 27 American-owned, and 5 Japanese-owned. U.S.-owned companies are continuing to invest heavily in Europe, and with AMD and Mostek now both committed to major wafer fabrication investments, Intel remains the only U.S.-owned manufacturer of any size without a European fabrication facility. By 1987, DATAQUEST anticipates that at least four Japanese-owned facilities will be in IC production in Europe. Interestingly, it now appears that Europe's very first 150mm wafer facility to go into production will be European-owned, not U.S.-owned.

Joseph Grenier
Malcolm G. Penn





June Newsletters

The following is a list of the material in this section:

- Semicon/West 1985
- U.S.-Japanese Trade Tensions--The View of American Business in Japan
- Capacity Utilization: The Harbinger of Recession

June Newsletters

(Page intentionally left blank)

Nielsen Dataquest RESEARCH NEWSLETTER

SEMS Code: 1984-1985 Newsletters: June

SEMICON/WEST 1985

HISTORY

The SEMICON trade shows are sponsored by the Semiconductor Equipment and Materials Institute (SEMI), a trade organization that services semiconductor equipment and materials suppliers. The first industry trade show in 1971 was simply called SEMICON. It had 100 exhibitors and 2,000 visitors. Its purpose was to provide a valuable link between buyers and sellers and to provide a place where materials and equipment products could be displayed. By 1984, SEMI was producing six SEMICON shows on three continents. Attendance had grown to 115,000 persons worldwide. Table 1 lists the locations and times of the six SEMICON trade shows.

Table 1

1985 SEMICON TRADE SHOWS

Show	Location	Month
SEMICON/EUROPA	Zurich	March
SEMICON/WEST	San Mateo	May
SEMICON/OSAKA	Osaka	July
SEMICON/EAST	Boston	September
SEMICON/SOUTHWEST	Dallas	October
SEMICON/JAPAN	Tokyo	December

Source: DATAQUEST

SEMICON/WEST 1985

This year's SEMICON/WEST, in San Mateo, California, was the largest ever for the San Mateo show. There were 2,135 booth spaces this year, up 28 percent over 1984. The fair attracted more than 1,000 exhibitors, which was a new record. Attendance was 45,000. In contrast, the most recent SEMICON/JAPAN, held in December 1984, had 768 exhibitors but 48,000 attendees, which makes the Japan show the largest show of 1984. It appears that the recession in semiconductor sales has taken its toll on travel budgets since December 1984. We did hear many comments that decision makers and influencers comprised a much higher percentage of the visitors than at previous shows.

New products were in abundance at the fair. DATAQUEST estimates that 167 companies introduced a total of 246 new products. There was also the addition this year of three new pavilions for test, assembly, and handling equipment.

The presence of Japanese companies was much stronger this year than in 1984 (see Table 2). DATAQUEST believes that this reflects a concerted effort by Japanese vendors to penetrate North American markets. Since Japanese equipment and materials companies are generally started as captive units of larger, vertically integrated companies (zaibatsu), they can develop considerable manufacturing expertise and capacity before they begin selling on the open market. In periods of downturn, if the parent companies cannot use the capacity of these subsidiaries, they will often give them permission to sell outside. The subsidiaries first sell to Japanese companies, developing the products in domestic markets. In this way, the products are made very reliable before they are exported.

Table 2

JAPANESE EXHIBITORS
1984 VERSUS 1985

	1984	1985	Percent Change
Test Assembly and Packaging	8	14	75%
Inspection and Measurement	7	9	29%
Maskmaking	3	4	33%
Front-End Equipment	9	13	44%
Materials	6	14	133%
Total Exhibitors	33	54	64%

Source: DATAQUEST

We believe that this semiconductor recession and its concomitant excess manufacturing capacity, both in the United States and Japan, will permit Japanese vendors to look to offshore markets. We have already seen a great penetration of these vendors into the materials markets. Table 3 is a partial listing of Japanese companies that have appreciable shares of the U.S. materials market. We believe that Japan is ready to make the commitment that will be necessary to penetrate equipment markets.

The three-day technical symposium covered the following subjects:

- Focus on automation
- Special sessions
- Packaging automation
- Process and equipment automation
- Contamination control in the automated production line
- Software experiences resulting from the installation and operation of automated systems

There were also four days of SEMI standards meetings.

Table 3

JAPANESE PENETRATION INTO U.S. MATERIALS MARKET

Company	Material
SEH America	Quartz Photomask Substrates
	Silicon and GaAs
Nippon Silica Glass	Quartz Photomask Substrates
TDK Corporation	Quartz Photomask Substrates
Hoya	Photomask Blanks
Dainippon Printing	Photomask Blanks
	Photomasks
Ulcoat	Photomask Blanks
Toppan Printing	Photomasks
	Photomask Blanks
Osaka Titanium	Silicon
Komatsu	Silicon and GaAs
Sumitomo Metal Mining	III-IV Materials
Kyocera	Ceramic Packaging
Tanaka	Gold Bonding Wire
Mitsui	Lead Frames
Nitto	Molding Compounds

Source: DATAQUEST

DATAQUEST Seminar

DATAQUEST sponsored its yearly SEMICON/WEST seminar. This year's special event was the public announcement of DATAQUEST's new Semiconductor Equipment and Materials Service (SEMS). The seminar was presented as follows:

- Introduction--Dr. David Crockett
- Semiconductor Industry Update--Fred Zieber
- Japanese Semiconductor Market--Gene Norrett
- Semiconductor Memory Market--Lane Mason
- Capital Productivity and Capacity--Robert McGeary

PRODUCTS

It is not practical in a short newsletter to even briefly describe the many new products introduced at SEMICON/WEST this year. However, there are two areas that warrant some discussion--mask repair and automation. These two emerging technologies will have high growth rates and, consequently, there is considerable interest in them.

Mask Repair Systems

SEMICON/WEST witnessed the worldwide introduction of the first focused ion beam (FIB) mask repair systems. Three companies introduced systems for repairing both opaque and clear defects: KLA/Micrion, Ion Beam Technologies, a start-up company located in Beverly, Massachusetts, and Seiko Instruments (Japan). The KLA/Micrion system is manufactured by Micrion but marketed by KLA. Micrion, a spin-off from Ion Beam Technologies, is also located in Beverly, Massachusetts. Seiko actually introduced its system in Japan one month before SEMICON/WEST. These are the first product offerings in the mask repair area for these companies.

All three of these systems use a focused ion beam to repair opaque defects by ion milling, but they differ in their approach to repairing clear defects. For clear defects, KLA/Micrion uses a focused ion beam to etch a microstructure on the surface of the glass to render the area opaque. Ion Beam Technologies and Seiko both use a focused ion beam to deposit a carbon film. Prices of the equipment range from $800 thousand to $1 million. Seiko has already delivered two systems, including one to Dianippon Printing in Japan. KLA/Micrion will ship its first system at the end of June to National Semiconductor, and Ion Beam Technologies will begin shipping at the end of 1985.

The mask repair market was previously shared by Quantronix (Smithtown, New York) and NEC (Japan), which both provided laser systems for repairing opaque defects only. However, at SEMICON this year, Quantronix introduced its new laser system for repairing both opaque and clear defects. For clear defects, a metal organic gas is introduced into the repair area and chromium or another metal is deposited only on the area heated by the laser. Although the minimum deposition area is 2um, smaller clear defects can be repaired by trimming the deposited area with the laser. The system is priced at $445 thousand and first shipments will begin at the end of June.

The NEC laser system can only repair opaque defects. For repairing clear defects, it has UV exposure capability. In this method, also used by Quantronix before the introduction of its new system, the clear area to be repaired is exposed on a photoresist-coated wafer. The wafer is removed from the machine and developed by conventional methods. A metal film is then sputtered on the developed wafer. Photoresist lift-off techniques are used to leave the clear area coated with the deposited metal. This system costs $150 thousand and has been on the market for about two years.

Table 4 lists all the mask repair systems currently available.

Table 4

MASK REPAIR SYSTEMS

	KLA/Micrion	IBT	Seiko	Quantronix	NEC
Opaque Defects					
Source	FIB	FIB	FIB	Laser	Laser
Defect Size	0.25um	0.25um	0.2um	<1.0um	<1.0um
Clear Defects					
Source	FIB	FIB	FIB	Laser	-
Technique	Etch	Carbon	Carbon	Metal	-
	Surface	Deposit	Deposit	Deposit	-
Defect Size	0.25um	0.25um	0.2um	<2.0um	-
Cost (thousands)	$1,000	$800	$1,000	$445	$150

Source: DATAQUEST

Automation

Automation was the theme of this year's technical session, which was entitled "Wafer Fab to Packaging Automation." Appropriately, automation at both the process equipment level and factory level was much in evidence this year in the exhibit halls.

Process Automation

At the process level, manufacturers continued their efforts to introduce cassette-to-cassette machines. This was accomplished in many cases by using robots. For instance, both Advanced Semiconductor Materials (ASM) and BTU Engineering had fully automatic cassette-to-cassette diffusion furnaces employing robotics to transfer the wafers from the plastic cassettes to the quartz boats. The boats were then inserted into the diffusion tubes by an elevator and automatic loaders. It was visually evident that automating a horizontal diffusion furnace is expensive--and, in fact, the price tag on the ASM furnace was $1 million.

Tylan's diffusion furnace had an interesting setup that used Asyst Technologies' standard mechanical interface (SMIF) system to transfer cassettes into a controlled environment in the load area of the furnace, where a Berkeley Glass Lab loader was used to transfer the wafers from the cassettes to quartz boats. The boats were then inserted into the tubes by an elevator and automatic loader. It appeared to be a simpler approach to automating a diffusion furnace.

Robots were used in other types of process equipment as well, including sputterers, wet stations, annealers, and rinser/dryers. The main suppliers of OEM robots to the semiconductor equipment industry appeared to be Intelledex, Precision Robots, and United States Robots. GCA had an interesting approach that used one of its overhead robots moving on rails to transfer cassettes among the various pieces of equipment in a photolithography island. This is a new approach for GCA, having previously focused on an in-line automated lithography island. Eaton and Ultratech, however, took the in-line approach and both companies had their steppers connected to their track equipment. Ultratech, a unit of General Signal, had its stepper connected to track equipment made by Semiconductor Systems, another General Signal unit.

Factory Automation

At the factory automation level, several companies offered hardware, including Asyst Technologies, Flexible Manufacturing Systems, Nacom, and Veeco. Asyst introduced its SMIF system, which is used to isolate the wafer cassettes from the ambient environment during transfer of the cassette among the various pieces of process equipment. Wafers are transported in sealed boxes that are placed on SMIF units on each piece of process equipment. The SMIF unit opens the box and removes the cassette in a controlled environment in the process equipment. When processing is completed, the SMIF unit replaces the cassette in the sealed box and the operator moves the box to another piece of equipment. An advantage of this system is that the wafers are always in a controlled environment and, hence, particulate contamination is reduced.

Flexible Manufacturing Systems introduced its computer-integrated manufacturing (CIM) system for the robotic transfer, storage, and inventory control of wafers in the fab area. The system consists of a mobile transport vehicle (MTV), which is a self-propelled vehicle used to transfer cassettes from one piece of process equipment to another or to the intelligent work-in-process (WIP) stations that are also part of the system. The MTV has an inertial navigation system and uses sonar to detect obstacles in its path. The path is not restricted and does not require any tape or stripes on the floor. The MTV communicates with the central control computer via a transmitted infrared (IR) signal. The price of a system including the MTV, two intelligent WIP stations, operations console and process equipment interfaces, and the control computer is $450 thousand. Systems will be installed at beta sites in the third quarter of 1985.

Nacom presented its Namtrak system for transporting wafers in overhead controlled-environment tunnels from one area of the fab to another. The system consists of a tunnel, elevators to move the cassettes (or boxes) between floor levels, and the tunnel and turntables to route the cassettes when more than one tunnel is used in an installation. The enclosed tunnels can be controlled to a Class 10 level. Nacom has installed several systems to date. Namtrak is being used to transfer wafers both within a clean room area and between one clean area and another where the wafers have to traverse a dirty area such as a hallway.

Veeco showed its factory automation system, which is also used for the robotic transfer, storage, and inventory control of wafers. Veeco's system consists of mobile transport vehicles, WIP stations, and a central control computer. There are three different types of MTVs, depending on the type of installation. The MTV is guided by a tape or stripe on the fab floor and stops at each equipment location as directed by the bar code on the floor. It uses a radio frequency (RF) system for detecting objects and, like the Flexible Manufacturing System vehicle, communicates with the central computer (a MicroVAX) with an IR link. The first system will be installed at the Fairchild/South Portland, Maine, plant in the near future.

Computer-Automated Manufacturing (CAM)

In addition to the companies involved in factory automation hardware, the factory automation software companies also exhibited at SEMICON/WEST, some with impressive booths. These companies included Consilium, CTX, Hewlett-Packard, and IP Sharp. Sentry/Schlumberger, now marketing the Incyte II software developed by Fairchild, chose not to exhibit any of its products, including testers, at SEMICON/WEST this year.

Joe Grenier
George Burns
Robert McGeary

Nielsen Dataquest RESEARCH BULLETIN

SEMS Code: Newsletters

U.S.-JAPANESE TRADE TENSIONS-- THE VIEW OF AMERICAN BUSINESS IN JAPAN

DATAQUEST attended the Japan Society of Northern California's presentation on U.S.-Japanese trade relations at the Red Lion Inn in San Jose, California, on June 12, 1985. This presentation was sponsored jointly by the AEA, the SEMI, the SIA, and the Japan Society. The speaker was Herbert F. Hayde, chairman of Burroughs Company, Ltd., Japan, and president of the American Chamber of Commerce in Japan.

Mr. Hayde has worked for Burroughs since 1956 and has served as chairman of Burroughs, Ltd., Japan, since June 1982. He has been part of the negotiations between the U.S. and Japanese governments concerning trade relations and has just finished a tour of more than 100 visits to U.S. senators and representatives.

Mr. Hayde began his speech by saying that anyone who is offering a panacea for the U.S.-Japanese trade deficit problems does not understand the situation. He said that, in 1985, the deficit will increase every month. Fear of future trade barriers has caused Japanese manufacturers to begin stockpiling inventory in the United States. Mr. Hayde's own fears about U.S. trade sanctions against Japan were not assuaged by the lack of understanding of the trade issues that he found in many of the U.S. congresspeople he met. Nor was he encouraged by the support some representatives voiced for sanctions.

He went on to say that Japan's prime minister, Mr. Nakasone, has publicly stated his support for a package that would open Japanese markets to foreign competition. Mr. Hayde said that the first move in this package has already opened the telecommunication and pharmaceutical markets. However, the goals of this package may not be accomplished without support from the Diet, the Japan legislative body. Although most members of the Diet have told Mr. Hayde that they support the package, he has formally requested the Diet to publicly announce its support in order to send the message to the Japanese people.

Mr. Hayde listed some steps that the United States might take to help. He emphasized the need to increase the number of personnel supporting U.S. trade in Japan. By way of contrast, he said that the Japanese External Trade Organization (JETRO), the trading arm of MITI, maintains 100 people in the United States. We have 15 people in Japan. In addition, Japan spends more than $30 million lobbying in Washington alone, not including state and local government lobbying. The United States spends about $5 million.

Mr. Hayde also suggested that the fundamental cause of the trade deficit with Japan is the U.S. budget deficit, which is maintaining a strong dollar with respect to the Japanese yen. We must reduce our budget deficit.

He also said that we must station our negotiators in Japan. Of the current U.S. negotiators, five are leaving to pursue other activities. Since relationships are everything in Japanese business, such attrition severely impedes any agreements that might be reached. Finally, he said that the U.S. government and financial institutions must support U.S. companies that wish to compete in Japan.

Mr. Hayde re-emphasized that it is crucial that the Diet publicly state support for the open-market package that is being considered. He said that it is also crucial that the Japanese government support foreign investment in Japan. At about half the U.S. interest rate, Japanese loans are very attractive to U.S. companies. When asked about a pending bill that would allow MITI to offer 3 percent loans to companies that purchase semiconductor equipment, he said that these were R&D loans that would be available to foreign companies, although he felt that the assurance of this availability should be written into the bill.

Mr. Hayde was optimistic about the prospects of U.S. companies penetrating Japanese markets. However, the current protectionist mood is an ominous sign, particularly when our two industrial bases are becoming increasingly interdependent. He compared protectionism to a titanic glacier that could bring the end to cooperative trade between our countries. He said that Japan has spent the last 40 years since the war building protections that were vital to the survival of its industrial base and now cannot easily tear them down.

Robert McGeary

Nielsen Dataquest RESEARCH NEWSLETTER

SEMS Code: Newsletters
June 1985

CAPACITY UTILIZATION: THE HARBINGER OF RECESSION

SUMMARY

An analysis of manufacturing productivity can provide valuable insight into the relationship between capacity and recessionary forces in the semiconductor industry. We are in a severe recession now; this analysis discusses its causes and DATAQUEST's assessment of the next 18 months.

DATAQUEST has constructed a capacity analysis that accurately measures capacity utilization since 1970. This analysis indicates that capacity utilization is currently at 73 percent and that it will remain below 80 percent until the end of 1986. This level of capacity utilization will tend to maintain negative price pressures so that average sales prices (ASPs) will not improve until 1987. Semiconductor manufacturers will attempt to improve margins by moving their product mixes into more advanced products.

We estimate that capital spending by North American merchant semiconductor companies in 1985 will decrease 13 percent from 1984 levels. Capital spending in 1986 will show a slight improvement of 4 percent over 1985. Japanese capital spending will decrease 6 percent in 1985 but will increase 31 percent in 1986. European companies will spend 4 percent less on capital in 1985, with spending remaining flat in 1986.

Silicon wafer manufacturers in North America are currently at about 60 percent of their capacity utilization. Although unit shipments by North American semiconductor manufacturers will decrease about 10 percent in 1985 from 1984 levels, silicon consumption will decrease 30 percent. Silicon consumption will not return to 1984 levels until 1987.

INTRODUCTION

The semiconductor industry is currently in a period of deep recession. We say this in contrast to previous announcements that the current level of sales is only a period of adjustment. All recessions are periods of adjustment--adjustment of production to the "real" demand curve. Our present adjustment is particularly severe.

This newsletter analyzes the causes of this adjustment and gives our estimate of what can be expected over the next 18 months. Our analysis focuses on industry capacity. We will investigate the elements of productivity that give rise to overcapacity and will show the historic and future trends of these elements as they will affect the semiconductor industry.

PRODUCTIVITY

Productivity is usually defined as unit of output per unit of input. The productivity of concern here is capital productivity of revenue per dollar of installed property, plant, and equipment. This ratio can be decomposed into the product of process productivity and equipment productivity. The following equation expresses this relationship:

$$P_c = P_p * P_e$$

$$\frac{\text{revenue}}{\text{PPE}} = \frac{\text{revenue}}{\text{inches}^2} * \frac{\text{inches}^2}{\text{PPE}}$$

where:

P_c = Capital productivity

P_p = Process productivity

P_e = Equipment productivity

PPE = Dollars of property, plant, and equipment

inches^2 = square inches of silicon

Both of these productivity measures give insight into the state of affairs of the semiconductor manufacturers and their suppliers.

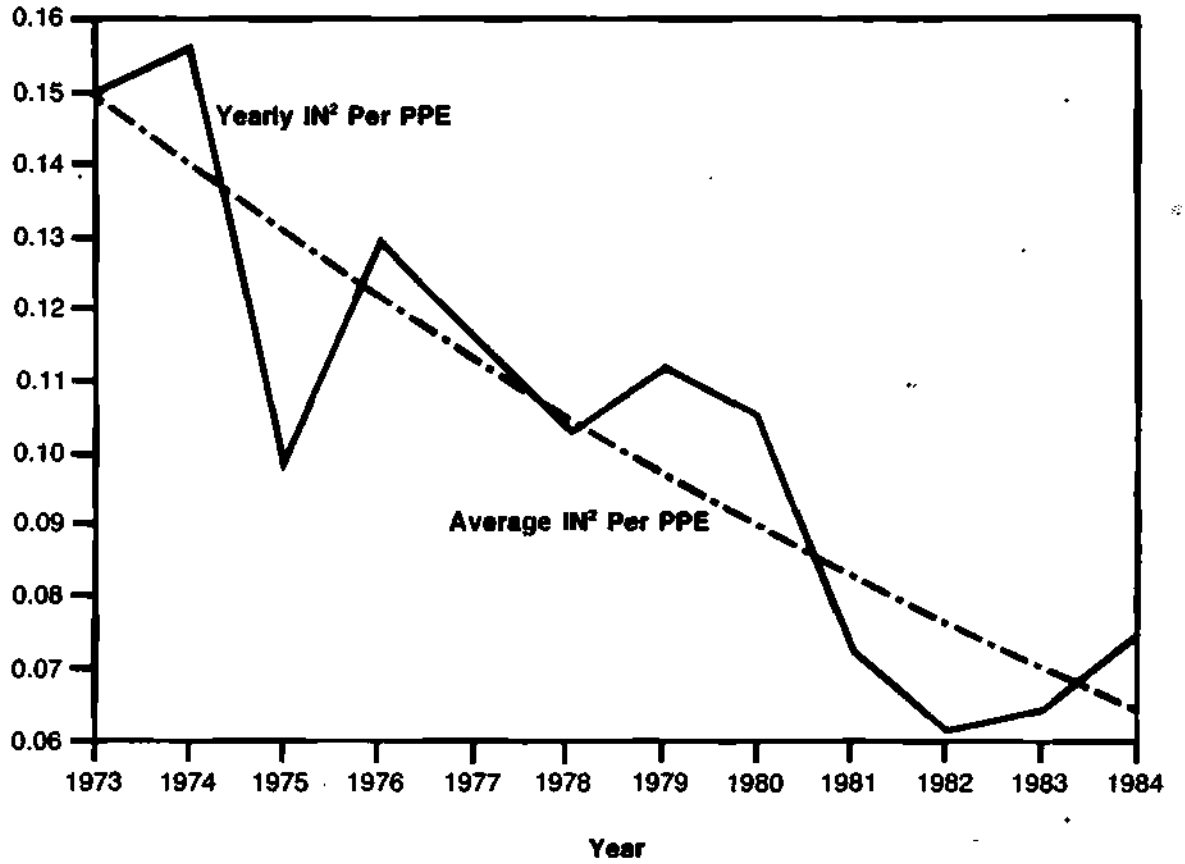
Historic Equipment Productivity

Equipment productivity is measured in square inches of silicon processed per dollar of installed property, plant, and equipment. Figure 1 shows the yearly values and long-term trend of this ratio since 1973. It shows that this ratio has been trending steadily down since 1970. This decrease is responsible for the large increase in fixed cost

as a percentage of manufacturing cost, which increased from 20 percent in 1975 to more than 50 percent in 1984. The yearly fluctuation of equipment productivity varies with sales growth, increasing with increasing sales, decreasing with slower sales. It is interesting to note that long-term equipment productivity has decreased even though average wafer size has steadily increased.

Figure 1

EQUIPMENT PRODUCTIVITY



Source: DATAQUEST

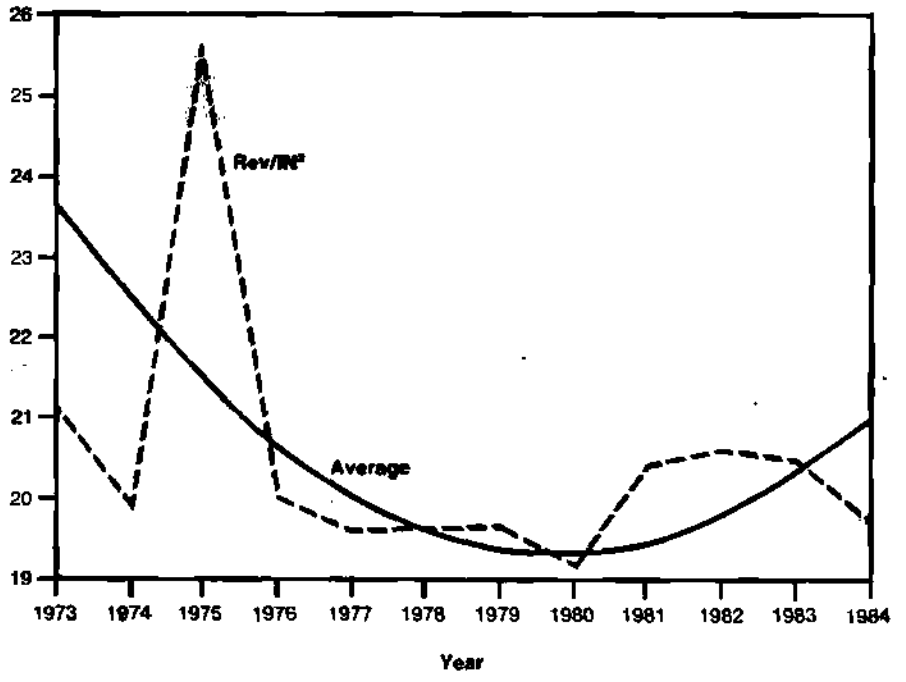
Historic Process Productivity

Process productivity is measured in revenue per square inch of silicon. The general trend of this ratio has been to decrease from $28.00 per square inch in 1970 to $19.29 in 1980. Since 1980, it has begun to increase, reaching $21.01 in 1984. This general trend is a value about which the ratio fluctuates from year to year depending on sales growth.

Process productivity is a function of average sales price (ASP), manufacturing yields, and die size. In addition, silicon consumption varies with sales growth as work in process (WIP) balloons to meet increasing unit demand. Although ASPs increase during high-growth years, yields tend to decline because new equipment, new processes, and new labor are being brought on to meet the burgeoning unit volume requirements. The increase in average die sizes is not large enough to affect productivity on a yearly basis. The net effect of these factors is to decrease process productivity with increasing sales growth and vice versa. For example, in 1984, when semiconductor sales grew 45 percent in the United States, revenue per square inch dropped below the trend line of $21.01 to $19.66. Figure 2 shows the yearly values and long-term trend of this ratio since 1973.

Figure 2

PROCESS PRODUCTIVITY



Source: DATAQUEST

CAPACITY

Capacity is the ability to manufacture wafers. In this analysis, we choose to ignore other wafer materials and define capacity in terms of silicon. We chose silicon as a material parameter for the following reasons:

- The raw material used in wafer fabrication plants is silicon; fabs process silicon.
- Silicon consumption is a measurable variable.
- Good die per square inch is a good indicator of yield.
- Using square inches removes wafer size as an intermediate variable.

Therefore, the unit of capacity measurement is square inches of silicon.

The average capacity utilization of the industry over many years has been 80 percent, although the actual yearly value fluctuates about this level. Industry capacity is derived from equipment productivity. The long-term trend in this ratio (which represents 80 percent of maximum productivity) is divided by 0.8 to obtain the maximum productivity possible. This is then multiplied by the total installed base of property, plant, and equipment to obtain the maximum square inches of silicon that could be processed in a given year. The actual silicon that has been processed in a given year can be compared with this capacity measure to determine the capacity utilization.

It must be kept in mind that equipment productivity is an industry aggregate and can vary considerably for individual semiconductor manufacturers. The maximum equipment productivity is determined by both equipment and manufacturing practices in terms of equipment reliability, equipment utilization, and wafer throughput.

Equipment Utilization

The average equipment utilization for North American semiconductor manufacturers is 30 percent. In other words, equipment sits idle 70 percent of the time that it is available for processing. This is a function of inefficiencies in production planning over large mixes of products to many customers. This inefficiency has not improved very much over many years. In addition, there are inefficiencies due to queuing problems caused by unreliable equipment. The improvement of equipment utilization is the most important gain that manufacturers will derive from computer-aided manufacturing systems.

Equipment Reliability

As mentioned above, unreliable equipment causes havoc with manufacturing lines. Line balance is extremely important for maintaining

maximum efficiency, since any disruption creates large queues of wafers at the malfunctioning equipment. Thus, in addition to the direct time that is lost because of repairs, there is a penalty to be paid in lost utilization of other equipment. Mean time to repair (MTTR) and mean time between failure (MTBF) are extremely important factors to be measured in a manufacturing operation. Both of these factors have a profound effect on equipment productivity.

Throughput

Wafer throughput as measured in square inches of silicon has been improving steadily over the last 20 years. Development of cassette-to-cassette equipment and increases in wafer diameters have served to improve this factor. However, the cost of the equipment has increased much more rapidly than the improvements in throughput. As shown in Figure 1, the value of equipment productivity has decreased at about 9 percent per year. If we assume that reliability and utilization are relatively unchanging, then it is throughput per dollar that is responsible for the decreasing equipment productivity.

THE CAUSES OF RECESSION

As mentioned above, recessions are caused by adjustments to real demand. In a rapidly growing market such as the semiconductor industry, it is extremely difficult to match capacity to real demand. In 1984, North American semiconductor manufacturers added 100 percent more capital than they did in 1983, serving to increase the installed base of equipment by 33 percent. The 45 percent increase in semiconductor production took the industry to 94 percent capacity utilization. While unit volumes increased 32 percent, the use of silicon by merchant semiconductor companies increased 54 percent.

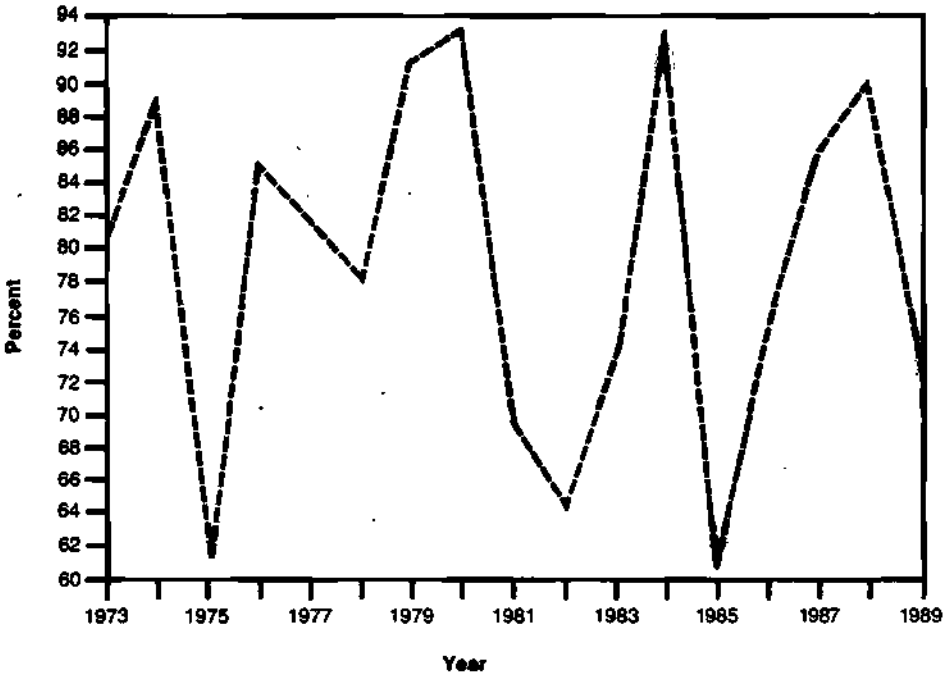
Industry capacity utilization has fallen to 73 percent in mid-1985; a result of new capacity continuing to come on-line while unit shipments decrease. In addition to new equipment coming on-line, process productivity is increasing due to better yields, exacerbating the utilization of capacity even further. It is excess capacity that drives recessions. It is excess capacity that drives ASPs down, reducing margins and increasing competitive struggles.

The Next 18 Months

Many of our clients have told us that this is the most severe decrease in booking that they have experienced. While semiconductor manufacturers have seen the worst of this cycle, it will be several months before an improvement in business is apparent. Even with an improvement in bookings, an improvement in industry capacity utilization will be longer coming. Figure 3 shows the capacity utilization cycles since 1973 and DATAQUEST's estimates for the next five years.

Figure 3

CAPACITY UTILIZATION



Source: DATAQUEST

Our estimates indicate that price pressures will continue as capacity utilization falls to 60 percent by the end of 1985 and remains below 80 percent until the end of 1986. Not only will semiconductor manufacturers continue to experience low margins, but low capacity utilization and increased process productivity will take their toll from equipment and materials vendors as well.

In the United States, capital spending cycles lag semiconductor sales cycles by seven months. In 1985, equipment manufacturers will ship only 87 percent of 1984 levels, and in 1986, shipments will increase only 4 percent over 1985 levels. In Japan, capital spending is coincident with semiconductor revenue cycles. Japanese capital spending will decrease 6 percent in 1985 and will increase 31 percent in 1986. European companies will spend 4 percent less on capital in 1985, with spending remaining flat in 1986. As an indication of the state of materials sales, silicon use will fall 30 percent in 1985. DATAQUEST estimates that silicon wafer manufacturers are currently operating at 60 percent capacity. Silicon use will not return to 1984 levels until 1987.

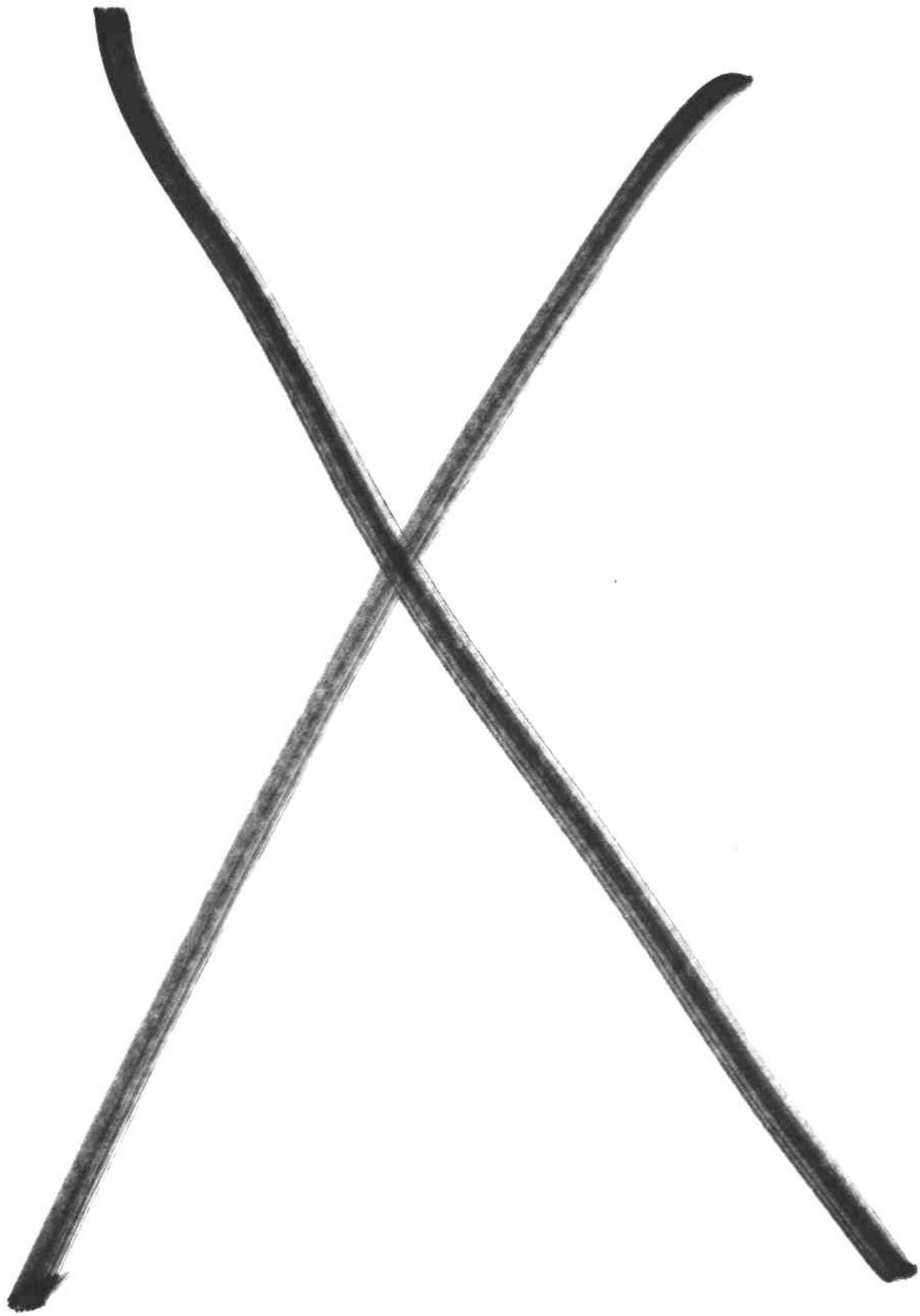
DATAQUEST CONCLUSIONS

Participants in the U.S. semiconductor industry can take solace in three things. First, the picture looks as bad in worldwide markets. While U.S. companies will drop 13.5 percent in sales this year, Japanese companies will fall 6.5 percent, and European companies will fall 9 percent. Since North American chip consumption is falling 20 percent in 1985, U.S. chip vendors may pick up market share in the world markets.

Second, while equipment sales will be down to flat for 18 months, there are some areas that will do well. Chip manufacturers will move their product mixes toward higher-margin products areas in which capacity utilization is not as low. Sales of equipment, such as reduction steppers, that will be used to manufacture new products, such as the 1-megabit DRAM, should remain relatively good. In addition, recessions are excellent periods in which to introduce new products, since semiconductor manufacturers continue to funnel money into R&D and pilot lines, readying themselves for the coming recovery.

Finally, real demand is marching inexorably onward, albeit more slowly than previously thought.

Bob McGeary



July Newsletters

The following is a list of the material in this section:

July Newsletters

(Page intentionally left blank)

Nielsen Dataquest RESEARCH NEWSLETTER

SEMS Code: 1984-1985 Newsletters: July

THE SEMICONDUCTOR START-UP BOOM CONTINUES

Despite the industry downturn, semiconductor start-ups are alive and well. As shown in Table 1, DATAQUEST has recorded 48 semiconductor start-ups since late 1983--a record for the industry. This figure tops the 29 start-up companies recorded for the same period covered by our last newsletter on this subject ("The Boom in Semiconductor Start-ups," December 19, 1983). Twenty-eight of the start-ups are located in Silicon Valley. Moreover, DATAQUEST believes that at least 10 more companies have not yet been publicly announced, since they are maintaining their secrecy while seeking first-round financing and developing their products.

Since 1977, 98 start-up companies have entered the industry, while only a handful have gone bankrupt. We believe that this continuing start-up boom and high survival rate reflects the emergence of new market niches in application-specific ICs (ASICs), CMOS memory and logic, gallium arsenide (GaAs), linear, digital signal processing (DSP), and silicon compilers. Major developments include the following:

- Emergence of nine GaAs start-ups
- Proliferation of ASIC vendors due to the availability of improved CAD systems and excess plant capacity
- Shift to silicon compilation (Cirrus Logic, Seattle Silicon, and Silicon Design Labs)
- Appearance of specialized CMOS memory and logic manufacturers (application-specific standard circuits)
- Growth in linear products for telecommunications, consumer, and military markets
- Initial companies offering DSP, graphics chips, sensors, and DMOS discrete chips

During the summer, DATAQUEST will survey these start-up companies and issue an industry update newsletter. We would appreciate hearing news of any other start-ups.

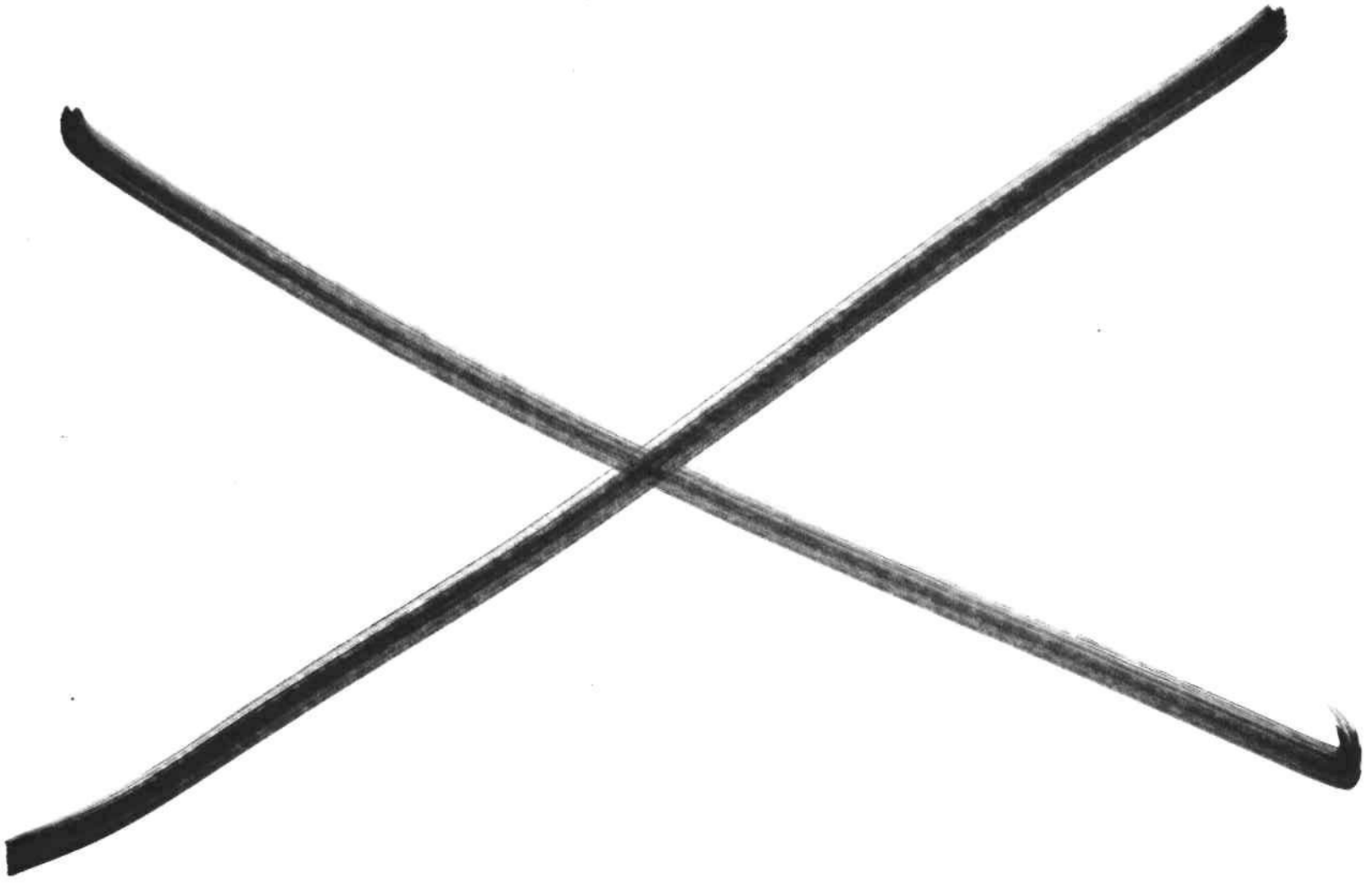
Table 1

SEMICONDUCTOR START-UPS
(1983 to 1985)

Company	Location	Products
Anadigics	Morristown, NJ	GaAs A/D converters
Array Logic	Melbourne, England	CMOS and bipolar ASICs
Barvon Research	Milpitas, CA	ASICs
Calmos	Kanata, Ontario	ASICs
Calogic	Fremont, CA	ASICs
Celeritek	San Jose, CA	GaAs FETs
China Micro	China	MOS ICs
Chips & Technologies	Milpitas, CA	ASICs
Cirrus Logic	Milpitas, CA	Silicon compilers
Crystal Semiconductor	Austin, TX	Telecom ICs
Custom Silicon	Lowell, MA	ASICs
Dallas Semiconductor	Dallas, TC	CMOS memories
Electronic Technology	Cedar Rapids, IA	ASICs
Inova Microelectronics	Campbell, CA	SRAMs
Integrated Logic Systems	Colorado Springs, CO	ASICs
Integrated Power Semiconductor	Santa Clara, CA Livingston, Scotland	Linear
Isocom	Campbell, CA	GaAs couplers
Ixys Corporation	Santa Clara, CA	Power monolithics
Logic Devices	Sunnyvale, CA	CMOS multipliers
Micro MOS	Santa Clara, CA	EPROMS
Microwave Technology	Fremont, CA	GaAs amplifiers
Modular Semiconductor	Santa Clara, CA	CMOS memories
Mosel	Sunnyvale, CA	EPROMs, SRAMs
NMB Semiconductor	Tokyo, Japan	CMOS memories
Pacific Monolithics	Sunnyvale, CA	GaAs monolithic ICs
Panatech Semiconductor	Santa Clara, CA	CMOS memories
Performance Semiconductor	Sunnyvale, CA	CMOS SRAMs, MPUs
Pivot III-V Corp.	Unknown	GaAs digital ICs
Quasel	Santa Clara, CA	CMOS memories
Seattle Silicon	Bellevue, WA	Silicon compilers
Sensym	Sunnyvale, CA	Pressure sensors
SID Microelectronics SA	Sao Paulo, Brazil	MOS ICs
Sierra Semiconductor	Sunnyvale, CA	Reconfigurable MPUs
Silicon Design Labs	Liberty Corner, NJ	Silicon compilers
Silicon Macrosystems	Santa Clara, CA	Static ROMs
Teledyne Microwave	Mountain View, CA	GaAs analog
Topaz Semiconductor	Santa Clara, CA	DMOS discretes
Triquint Semiconductor	Beaverton, OR	GaAs analog and digitizer
Unicorn Microelectronics	San Jose, CA	ASICs
Vatic Systems	Mesa, AZ	ASICs
VTC Inc.	Eagan, MN	CMOS logic
VISIC	San Jose, CA	CMOS RAMs
Vitelic	San Jose, CA	CMOS memories
Vitesse Electronics	Camarillo, CA	GaAs digital ICs
Xilinx	San Jose, CA	CMOS logic arrays
Xtar Electronics	Elk Grove, IL	Graphics chips
Zoran	Sunnyvale, CA	DSP

Source: DATAQUEST

Barbara Van
Sheridan Tatsuno



August Newsletters

The following is a list of the material in this section:

- The New Mitsubishi Saijo Factory--A Fully Automated Facility
- Chemical Vapor Deposition

Nielsen Dataquest RESEARCH NEWSLETTER

SEMS Code: 1985-1986 Newsletters: August

THE NEW MITSUBISHI SAIJO FACTORY-- A FULLY AUTOMATED FACILITY

INTRODUCTION

DATAQUEST recently had the exceptional opportunity to visit Mitsubishi Electric Corporation's impressive new semiconductor factory located in Saijo on the island of Shikoku, Japan. DATAQUEST was escorted on the factory visit by Dr. Hiroyoshi Komiya, Deputy Manager of the Saijo factory, and Mr. Shigeru Funakawa, Semiconductor Overseas Marketing Manager for Mitsubishi. This factory, the first semiconductor facility on the island of Shikoku, was completed in early 1984 and is a fully automated front- and back-end facility dedicated to the production of DRAMs. The entire production process from bare silicon wafer start to final packaged and tested part is completely automated.

Dr. Komiya bas been invited to give a talk on the Saijo facility at DATAQUEST's annual Semiconductor Equipment and Materials Conference held October 14 through 17 in Tucson, Arizona. The theme of the Conference will be "An Industry in Transition." Dr. Komiya's talk on the Saijo facility at the Conference should, indeed, be a very interesting topic as attested to by the following brief overview of our visit to the facility.

THE SAIJO FACTORY

Presently, the Saijo factory consists of production buildings B and C, each of which has three floors covering 22,000 square meters of floor space. Building B is dedicated solely to the production of 64K DRAMs and has a capacity of 10 million parts per month. It was constructed at a cost of $127 million, including all capital equipment and automation hardware and software. Volume production of 64K DRAMs on 5-inch wafers began in March of 1984. Building C is dedicated to 256K DRAM production and was constructed at a cost of $190 million. It has a capacity of 7 million parts per month and volume production was scheduled to begin in July 1985. Next to Building C is an empty lot--yes, you guessed it--for a 1-Mbit DRAM facility, which is scheduled to be in production in the near future.

DATAQUEST visited the Building B 64K DRAM facility and the following discussion pertains to that facility. It is our understanding that the 256K DRAM facility is constructed along similar lines.

Device production occurs on two floors. The wafer fabrication area is located on the first floor and is a Class 10/Class 100 facility designed with a "main street" and "side street" concept. Up and down the wide main street move trackless but optically guided, automatically guided vehicles (AGVs) carrying cassettes of wafers. Branching off from main street at right angles are narrower side streets dedicated to the various wafer fabrication processes. For instance, there is a photolithography side street along which are clustered steppers and photoresist processing equipment. Dry etchers are clustered along another side street.

The AGVs in main street transfer their cassettes of wafers to I/O stations located at the junctions of the main and side streets. Robots moving in the side streets transfer the cassettes from the I/O stations to the various pieces of processing equipment located up and down the side street. The entire wafer fabrication production sequence is entirely automated; at no point in the production sequence do operators handle the wafers. Inspection at various points in the production process is done via CCTV by operators outside the clean room.

The first floor also includes the wafer test area laid out in the same main and side street approach. This area was designed to be Class 1000, but because of the reduction of people present (there appeared to be two) Class 100 levels were actually being reached. DATAQUEST noticed that in the wafer test area there were additional stationary robots transferring cassettes among several pieces of equipment clustered about them.

At the completion of wafer fabrication and probing, the wafers are automatically moved in an elevator up to the second floor where assembly and test occurs. On the second floor, overhead robots running on ceiling tracks transfer the devices among the various types of test equipment. All phases of assembly and test are fully automated including encapsulation and burn-in. Optical pattern recognition systems are used for automatic inspection of the marking step.

Communications and Control

The following is a brief overview of the factory automation system. A central factory computer interfaces with two control computers, one for each floor. For the first floor wafer fabrication and test area, the control computer interfaces to several process control CPUs, each of which interfaces with several individual pieces of process equipment. The first floor control computer also interfaces to another CPU for traffic control of the AGVs in main street. The AGVs communicate to the traffic control CPU through the I/O stations. The AGV receives its instructions from the I/O station. This is in contrast to the U.S.-manufactured Veeco and Flexible Manufacturing Systems AGVs, both of which communicate directly to their control computer via an infrared

link. The control computer on the second floor has a similar architecture.

In the factory computer control center, operators sit at a long console and monitor factory status via CRT monitors in the console. In front of the console is a large illuminated electronic board that schematically depicts the entire two-floor production process and the various pieces of equipment. Every bare wafer is marked and, although lots are usually tracked, individual wafers can be called up and located in the factory by the monitoring and tracking system.

Process data are collected by the system and analyzed. Dr. Komiya noted that as the human element has been removed, the process data have tended to exhibit a very tight distribution about the mean. The factory central computer also communicates with Mitsubishi's Kita-Itami Works. For instance, quality control data are sent to Kita-Itami for further analysis, the results of which are fed back to the Saijo factory computer.

Mitsubishi built all robots and AGVs in the factory as well as writing the factory automation software. It took Mitsubishi three years to complete the system.

Results of Automation

DATAQUEST was told that the 64K DRAM facility was obtaining a defect density of 0.1 defects/mask level/cm^2. This should be compared to a world class Class 100 facility that can obtain 0.5 defects/level/cm^2. Mitsubishi has paid much attention to the reduction of particulate levels in the fab. All robotic equipment and AGVs were designed to contribute minimum levels of particulates. Mitsubishi worked closely with the equipment vendors to minimize the equipment particulates and, further, the process equipment was cleaned before it was installed in the clean room.

Cycle time for the wafers for the first floor (wafer fabrication and probing) is about three weeks. This should be compared to the 6 to 10 weeks required for an average U.S. fab cycle, with 6 weeks being a very good cycle time. Cycle time for the second floor (assembly and test) is about one week.

Although Mitsubishi would not disclose its device yields, it indicated that automation resulted in about a 20 percent relative increase in yields. Mitsubishi also believes that the Saijo facility can produce the lowest-cost 64K DRAM in the world. Taking all factors into consideration, DATAQUEST estimates that this facility is obtaining yields of between 85 percent and 90 percent for 64K DRAMs. DATAQUEST also estimates that the factory capacity of 10 million parts per month corresponds to 20,000 wafer starts per month at these yields.

Joseph Grenier

Nielsen Dataquest RESEARCH NEWSLETTER

SEMS Code: Newsletters

CHEMICAL VAPOR DEPOSITION

INTRODUCTION

DATAQUEST's Semiconductor Equipment and Materials Service recently conducted an extensive study of the worldwide chemical vapor deposition (CVD) market. This newsletter gives a quick overview of the contents of the study, which may be found in the SEMS Markets and Technology notebook behind the Wafer Fabrication Equipment tab.

This newsletter summarizes the three major CVD areas of atmospheric pressure CVD (APCVD), low pressure CVD (LPCVD), and plasma enhanced CVD (PECVD) from both a markets and technology point of view. Other CVD technologies are discussed in the study.

ATMOSPHERIC PRESSURE CVD

APCVD films have been used since the early days of the semiconductor industry, and this method is, historically, the oldest of the CVD techniques in use today. The advantage of APCVD is its high throughput. However, as LPCVD and PECVD technologies were developed, the use of APCVD declined because of the higher quality of films deposited by these newer processes.

Equipment Configuration

APCVD equipment is of two general types: the continuous-belt design, which has a reactor open to the ambient atmosphere, and the batch design, which has a reactor closed to the atmosphere. In belt reactors, wafers are continually transferred through the reactor chamber on endless belts. In the batch type, a lot of wafers is either manually or automatically loaded onto a horizontal susceptor in the reactor chamber for processing. Continuous-belt manufacturers include Amaya Manufacturing (Japan), Applied Materials, Pacific Western Systems (modified belt design), and Watkins-Johnson. Batch reactors are provided by Tempress, which manufactures a manually loaded batch reactor, and Hitachi (Japan), which introduced an autoload batch reactor in 1984.

Applications

APCVD reactors are used predominantly to deposit doped (PSG or BPSG) and undoped oxide films for either final passivation or interlayer dielectric applications. APCVD reactors deposit these films at low temperatures with a high throughput. The main disadvantages of APCVD films are the relatively poorer conformal step coverage, poorer uniformity, higher particulate count, and rougher surface compared with LPCVD or PECVD films. It was the disadvantages of APCVD films that were responsible for the shift from APCVD reactors to LPCVD and PECVD reactors and the consequent slowdown and stagnancy of the APCVD market. Another factor contributing to the slowdown of the APCVD market was the increasing use of PECVD silicon nitride as a passivation layer in lieu of APCVD oxides.

Market Data

Table 1 shows the worldwide market demand for APCVD equipment for the last three years. U.S. demand was flat not only from 1982 to 1983, but for several years prior as well. The Japanese APCVD market is larger than the U.S. market, as the Japanese tend to use APCVD films more in IC manufacturing than do the U.S. firms. APCVD market demand in Japan has been growing at a respectable 23 percent over the last two years.

Table 2 lists the APCVD manufacturers by estimated market share. Note that Amaya is the world leader in APCVD reactors and that the belt manufacturers accounted for 71 percent of the total market. The reason for this is the higher throughput of the belt reactors compared to the batch reactors.

Table 1

WORLDWIDE APCVD EQUIPMENT MARKET DEMAND
(Millions of Dollars)

	1982		1983		1984	
	Sales	Share	Sales	Share	Sales	Share
United States	$ 8.6	38%	$ 8.8	34%	$11.1	34%
Japan	13.3	59	16.3	62	20.0	62
ROW	0.8	3	1.0	4	1.3	4
Total	$22.7	100%	$26.1	100%	$32.4	100%

Source: DATAQUEST

Table 2

1984 WORLDWIDE APCVD EQUIPMENT MARKET SHARE
(Millions of Dollars)

	Sales	Share
Amaya Manufacturing	$10.0	30.9%
Tempress	6.0	18.5
Watkins-Johnson	6.0	18.5
Applied Materials	5.6	17.3
Hitachi	3.0	9.3
Pacific Western Systems	1.4	4.3
Others	0.4	1.2
Total	$32.4	100.0%

Source: DATAQUEST

LOW PRESSURE CVD

There is currently more activity in the LPCVD area than in any of the other CVD technologies. Horizontal furnaces, which have been the workhorses for LPCVD processes, are reaching the limits of their present designs and new approaches are being taken to meet the needs of VLSI fabrication. New companies with new reactor designs are entering the LPCVD market; recent LPCVD start-ups include Focus Semiconductor, Novellus Systems, and Rome-Union. Because of the opportunities in this market, we could see more start-ups as well.

Equipment Configurations

LPCVD equipment is of three general designs: the horizontal tube reactor, the nontube reactor, and the vertical tube reactor. The horizontal tube reactor is the oldest of the techniques; vertical tube reactors are the newest and are just now entering the marketplace. Nontube reactors are also recent designs, having only been around for the last two years.

Horizontal Tube Reactor

Horizontal tube LPCVD reactors were originally designed to fit into the bore of diffusion furnaces, which were then in widespread use in the semiconductor industry. The main advantage of the horizontal tube reactor is its ability to deposit uniform and conformally coated films on large batches of wafers. The LPCVD reactor consists of a quartz tube that is inserted into the bore of the furnace. The wafers, which are placed on quartz boats, are heated by the furnace's three-zone heater surrounding the quartz tube.

Because the walls of the quartz tube also get hot, this type of reactor is also called a "hot wall" reactor. Since the reaction is thermally driven, film deposition will take place not only on the wafers, but also on the walls of the quartz tube, the wafer boats, and anything else in the tube. The unwanted film deposition on the walls of the tube builds up and eventually flakes off, causing particulates. Particulate formation from this cause has been the major problem with horizontal LPCVD reactors.

Other problems associated with today's horizontal tube reactors include heavy power consumption, a large clean room footprint, long downtimes associated with the frequently required tube cleanings, and the high cost and difficulty of automation.

Nontube Reactor

The LPCVD horizontal tube reactor was adapted to then existing diffusion furnaces and, therefore, advances in LPCVD technology have been closely tied to advances in furnace technology. In contrast, nontube LPCVD reactors, typified by the Anicon and Genus reactors, were originally designed to be dedicated to the deposition of LPCVD films only.

The Anicon reactor uses a hot wall "bell jar" approach consisting of a chamber-within-a-chamber design to produce uniform films. The design is such that Anicon claims that particulate formation is less than in horizontal reactors. Other advantages of the system include lower power consumption, less cleaning time, and a smaller footprint.

The Genus reactor is dedicated to the deposition of tungsten and tungsten silicide films. It is a "cold wall" reactor because the outer wall of the deposition chamber is water cooled so that film deposition does not take place on the wall, thereby reducing particulates. Before the advent of this reactor, these materials (mostly the silicides) were deposited by sputter deposition. The availability of this reactor broadened the LPCVD market at the expense of the sputtering market.

Vertical Tube Reactor

Vertical tube diffusion furnaces are just now being introduced into the marketplace. However, LPCVD capability for these furnaces is still being developed. The advantages of vertical furnaces include lower power consumption, a smaller footprint, ease of automation, and the ability to handle large loads of large-diameter wafers. Denko (Japan), Helmut Seier (Switzerland), and Tempress have introduced furnaces; Silicon Valley Group has a furnace under development.

Applications

LPCVD is used to deposit high-temperature silicon nitride, high-temperature oxide, low-temperature oxide, polysilicon, TEOS oxide, tungsten, tungsten silicide, and other films as well. The first four films account for about 95 percent of the films deposited by LPCVD. The remaining films are just now beginning to be deposited, as these films are used more and more in VLSI device fabrication.

Market Data

Table 3 shows the worldwide LPCVD equipment demand for the last three years. The 1984 worldwide demand of $141.5 million represents a hefty growth of 85 percent over the 1983 level of $76.4 million. U.S. growth for 1984 over 1983 was even stronger at 100 percent. The main reason for this exceptional growth was the increased capital spending by both U.S. and Japanese semiconductor companies. Table 4 ranks the leading LPCVD manufacturers by 1984 sales. Note that Thermco is first, followed by Genus and Anicon. These latter two companies both manufacture nontube reactors and have only been in the market for two years. Also, the worldwide LPCVD market is dominated by U.S. companies. Of the $141.5 million in worldwide sales, the three Japanese companies (TEL/Thermco, Kokusai, and Koyo Lindberg) accounted for only $32.8 million, or 23 percent, and two of these companies are actually joint ventures with U.S. firms.

Table 3

WORLDWIDE LPCVD EQUIPMENT MARKET DEMAND
(Millions of Dollars)

	1982		1983		1984	
	Sales	Share	Sales	Share	Sales	Share
United States	$23.9	47%	$37.6	49%	$ 75.3	53%
Japan	19.7	39	28.9	38	47.5	34
ROW	7.0	14	9.9	13	18.7	13
Total	$50.6	100%	$76.4	100%	$141.5	100%

Source: DATAQUEST

Table 4

1984 WORLDWIDE LPCVD EQUIPMENT MARKET SHARE
(Millions of Dollars)

	Sales	Share	Reactor Design
Thermco	$ 20.8	14.7%	Horizontal Tube
Genus	18.0	12.7	Nontube
Anicon	17.6	12.4	Nontube
TEL/Thermco	15.0	10.6	Horizontal Tube
Kokusai	14.5	10.2	Horizontal Tube
Advanced Semiconductor Materials	13.4	9.5	Horizontal Tube
Advanced Crystal Sciences	12.0	8.5	Horizontal Tube
Tylan	9.0	6.4	Horizontal Tube
BTU Engineering	7.0	5.0	Horizontal Tube
Tempress	5.2	3.7	Horizontal Tube*
Process Technology	4.7	3.3	Retrofit Kits
Koyo Lindberg	3.3	2.3	Horizontal Tube
Others	1.0	0.7	-
Total	$141.5	100.0%	

*Tempress recently introduced a vertical tube furnace.

Source: DATAQUEST

PLASMA ENHANCED CVD

The main advantage of PECVD, the newest of the major CVD technologies, is low temperature. Silicon oxide and silicon nitride films, which make up the majority of the films deposited by PECVD, are deposited at temperatures of less than 400 degrees C, and it was these lower-temperature deposition processes that caused PECVD to gain rapid acceptance.

Equipment Configurations

PECVD equipment is of two major types: the parallel plate design and the horizontal tube design. The parallel plate design was developed first, but the throughput limitations of this design led to the development of the horizontal tube reactor.

Parallel Plate Reactor

The Applied Materials AMP 3300 is an example of a parallel plate reactor. The AMP 3300 reactor consists of two 26-inch-diameter, horizontal, circular, parallel plates that are 2 inches apart. Wafers are placed on the heated lower plate and a uniform plasma is created between the plates (electrodes). Plasma-Therm also manufactures a line of parallel plate reactors. Both of these companies provide only manual systems in which the wafers have to be manually loaded and unloaded. E.T. Electrotech provides a load-locked cassette-to-cassette system that has a number of advantages, including higher throughput than the manual systems.

Horizontal Tube Reactor

In the horizontal tube, or "hot wall," reactor, a quartz tube is inserted into a furnace dedicated to PECVD. Wafers are placed on a graphite boat assembly, which is then inserted into the quartz tube. RF power is applied to the boat assembly to create a plasma. The main advantage of this type of reactor is the higher throughput resulting from larger wafer loads. Advanced Semiconductor Material (ASM), which pioneered the horizontal reactor, dominates the market, followed by Pacific Western Systems (PWS).

Applications

Silicon nitride accounts for 75 percent of the films deposited by PECVD, silicon oxide accounts for 20 percent, and other films such as polysilicon, amorphous silicon, oxynitride, and titanium silicide account for the remaining 5 percent. The major application for PECVD silicon nitride is for passivation. Another emerging application for nitride is its use as a capping layer when annealing GaAs devices.

Market Data

Table 5 shows the worldwide market demand for PECVD equipment for the last three years. Worldwide demand in 1984 was $71.3 million. Comparing 1984 PECVD data with 1984 APCVD data (Table 1) indicates that Japanese demand for APCVD equipment ($20.0 million) was close to Japanese demand for PECVD equipment ($22.6 million) while U.S. demand for PECVD equipment ($36.8 million) was much larger than the U.S. APCVD demand ($11.1 million). DATAQUEST believes that this reflects the tendency of the Japanese to use APCVD processes more than do U.S. manufacturers. Also, there is no major manufacturer of PECVD equipment in Japan; DATAQUEST believes that most of the PECVD equipment used in Japan is imported from U.S. manufacturers.

Table 6 shows the market shares of the leading manufacturers. The two leading companies (Advanced Semiconductor Materials and Pacific Western Systems), which both provide horizontal reactors, together accounted for 66.2 percent of the market.

Table 5

WORLDWIDE PECVD EQUIPMENT MARKET DEMAND
(Millions of Dollars)

	1982		1983		1984	
	Sales	Share	Sales	Share	Sales	Share
United States	$17.0	54%	$22.3	50%	$36.8	51%
Japan	10.0	31	14.6	33	22.6	32
ROW	4.8	15	7.3	17	11.9	17
Total	$31.8	100%	$44.2	100%	$71.3	100%

Table 6

1984 WORLDWIDE PECVD EQUIPMENT MARKET SHARE
(Millions of Dollars)

	Sales	Share
Advanced Semiconductor Materials	$34.7	48.7%
Pacific Western Systems	12.5	17.5
E.T. Electrotech	6.4	9.0
Applied Materials	6.2	8.7
Plasma-Therm	5.7	8.0
Others	5.8	8.1
Total	$71.3	100.0%

Source: DATAQUEST

TRENDS IN INTERCONNECTION TECHNOLOGY

Aluminum is widely used in IC device fabrication for making contacts and as a metallization material. Likewise, highly doped polysilicon is widely used for making interconnections at the gate level. However, as device geometries continue to shrink, these technologies will not be able to meet the challenge. The problem is that, while shrinking geometries improves device performance, it also increases interconnection resistance, thus nullifying the device speed gains promised by the reduction in chip geometries. Other problems associated with scaling include increased contact resistance, shorted or leaky junctions, and electromigration failures. Thus, new interconnection technologies are needed in the major areas of contacts, gate interconnect, and metallization.

Contacts

When aluminum is used to contact the underlying silicon source/drain region, the aluminum and silicon interdiffuse, resulting in a junction that could be shorted out. Alloying aluminum with 1 percent silicon has alleviated the problem, but this is not a satisfactory method for the very small contact areas used in advanced devices. Refractory metals like molybdenum, tungsten, titanium, and tantalum have been considered as contact barrier metals to prevent the diffusion of aluminum. The refractory metals are usually sputtered, with the exception of tungsten, which can be selectively deposited in an LPCVD reactor. Although many contact metals are being investigated, a clear choice has not yet emerged. However, there are certain advantages to using CVD tungsten, and the current availability of LPCVD reactors to deposit tungsten will be a factor in choosing a technology.

Gate Interconnect

Even with highly doped polysilicon, resistance becomes a limiting factor below 2-micron geometries. This has led to the use of the polycide structure in which the gate interconnect is made up of a refractory metal silicide deposited on top of doped polysilicon. The silicides that have been the leading contenders for this structure are $TiSi_2$, $MoSi_2$, $TaSi_2$, and WSi_2. The main problem associated with the silicides has been in the deposition area. Several physical vapor techniques have been used to deposit the silicides, but all have their limitations. These limitations have been the driving force in developing CVD processes for depositing silicides.

All four of the silicides have their advantages and disadvantages, and it is not clear at this point which of the silicides, if any, will become the dominant choice. The choice of one silicide over another will depend not only on the film characteristics, but also on the deposition technique. DATAQUEST believes that tungsten silicide is currently most widely used in the United States, as several semiconductor manufacturers are using it in production. The advent of the Genus LPCVD tungsten

silicide reactor gave this silicide a head start over the others. Genus is currently the major supplier in this area, although other manufacturers are developing processes as well.

Metallization

Two problems associated with aluminum metallization include hillock growth and its lack of resistance to electromigration failure. Alloying copper with aluminum reduces these problems, but aluminum/copper alloys are difficult to etch. Alloying aluminum with titanium instead of copper solves these problems, since titanium alloys can be dry etched. Two metallization schemes being considered are the homogeneous Al/Ti alloy and the layered Al/Ti structure. As device geometries continue to shrink, conventionally sputtered aluminum and its alloys become less suitable because of line thinning and nonconformal step coverage. Because of these limitations, refractory metals are being considered for 1-micron geometries. The metal with the most promise appears to be tungsten. Tungsten can also be deposited with CVD processes, while aluminum and its alloys cannot as yet.

TRENDS IN INTERLAYER DIELECTRICS

No discussion of interconnection trends would be complete without considering the trends in interlayer dielectrics, for the two are intimately related. Two interlayer dielectrics in which there is rising interest are BPSG and TEOS oxide.

BPSG

BPSG is being increasingly considered as a replacement for the widely used PSG, particularly in advanced VLSI devices. The main driving force for this is the lower flow temperature of BPSG, which is about 800 degrees C, in contrast with 1,000 degrees C for PSG. Lower process temperatures offer a number of advantages, including reduced dopant diffusion in the junctions and reduced wafer warpage. The BPSG process was developed by RCA on APCVD reactors and has been extensively used in IC fabrication by RCA since 1980.

BPSG can be deposited by any of the three CVD technologies. However, the APCVD process is better understood because the process was originally developed on APCVD reactors. DATAQUEST believes that the majority of production BPSG films are currently being deposited in APCVD reactors but that LPCVD and PECVD BPSG processes will be used extensively once they are fully developed and understood. CVD equipment manufacturers, in general, report a steeply rising interest in BPSG-configured reactors.

TEOS

TEOS is an organic silicon compound that can be used in lieu of silane or dichlorosilane to produce a high-quality doped or undoped silicon dioxide interlayer dielectric. The advantages of TEOS oxide include better electrical properties, higher density, and excellent conformal step coverage. Because of its excellent as-deposited step coverage, TEOS oxide does not need to be flowed like PSG or BPSG. A disadvantage of TEOS is the high deposition temperature of 700 degrees C.

For 2- to 3-micron devices, the flowed glasses, PSG and BPSG, are adequate, but for 1-micron devices, TEOS may be the preferred film for interlayer dielectrics. However, it is not clear at this time which film will be used, and, more likely, there will be applications for all three films in advanced VLSI production. AT&T is currently using TEOS in production.

MARKET FORECAST

Table 7 gives the forecast for CVD equipment from 1985 through 1989. APCVD equipment is expected to grow slowly at an 8.4 percent CAGR over the next five years. In 1984, APCVD equipment accounted for 13 percent of the total CVD market; in 1989, the APCVD share is expected to be 8 percent.

The LPCVD market is expected to grow the fastest at a 22.7 percent CAGR. LPCVD equipment accounted for 58 percent of the CVD market in 1984 and is expected to account for a 66 percent share in 1989.

The PECVD market is expected to grow at a CAGR of 17.4 percent. PECVD equipment accounted for a 29 percent share of the CVD market in 1984 and is expected to decrease to 26 percent in 1989.

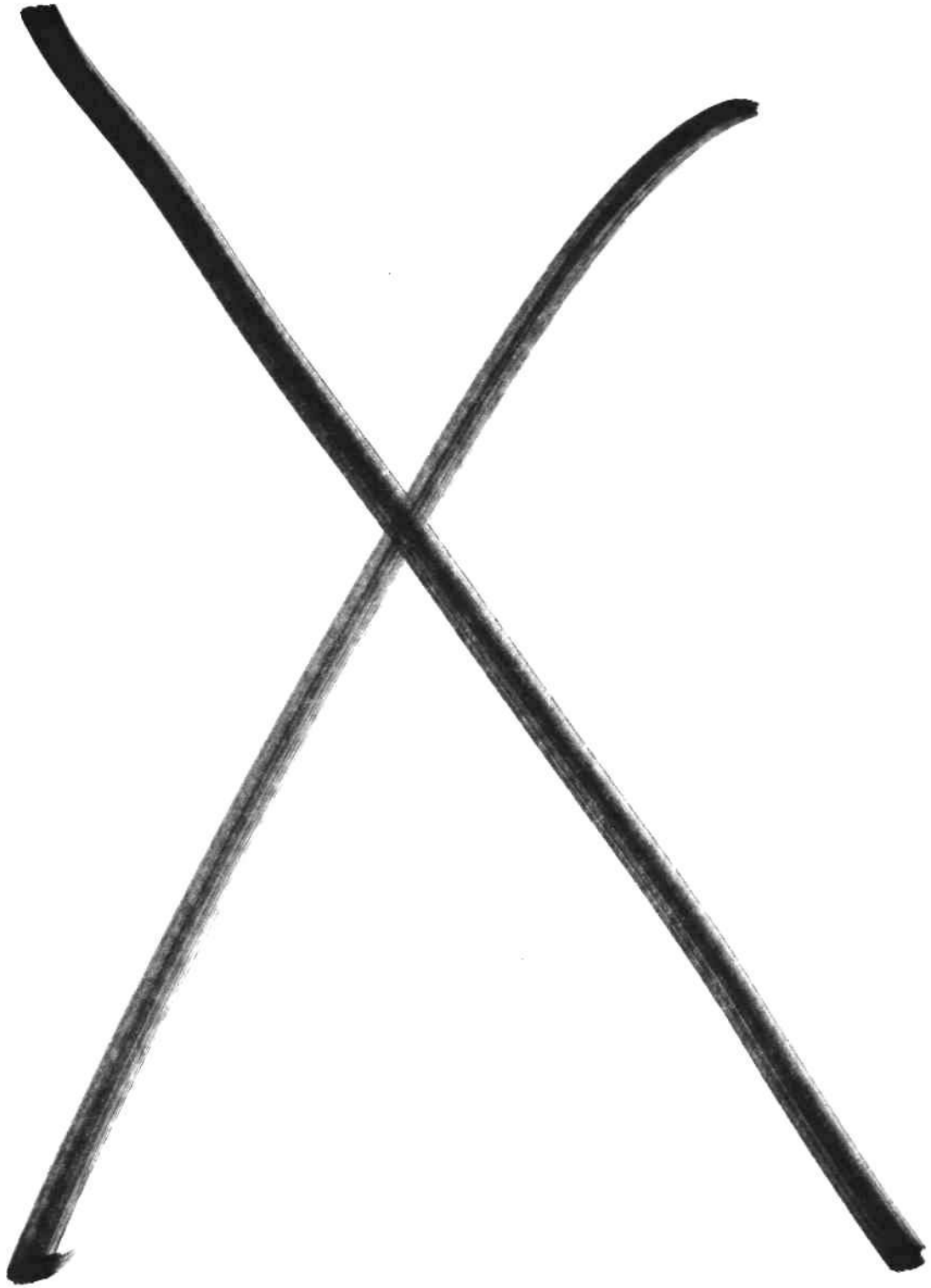
Joseph Grenier

Table 7

WORLDWIDE CVD EQUIPMENT FORECAST
(Millions of Dollars)

	1982	1983	1984	CAGR (1982-1984)	1985	1986	1987	1988	1989	CAGR (1985-1989)
APCVD	$ 22.7	$ 26.1	$ 32.4	19.5%	$ 29	$ 30	$ 34	$ 38	$ 40	8.4%
LPCVD	50.6	76.4	141.5	67.2%	135	148	207	279	306	22.7%
PECVD	31.8	44.2	71.3	49.7%	64	$ 68	88	110	121	17.4%
Total	$105.1	$146.7	$245.2	52.8%	$228	$246	$329	$427	$467	19.6%

Source: DATAQUEST



September Newsletters

The following is a list of the material in this section:

Nielsen Dataquest RESEARCH NEWSLETTER

SEMS Code: Newsletters

CIS: AN INTEGRATION OF SEMICONDUCTOR MANUFACTURING AND SCIENCE

A FRAGMENTED RESEARCH SYSTEM

While strong in the areas of entrepreneurship and invention, America's semiconductor research and development has been criticized as being fragmented and wasteful of effort and resources. The industry, especially under the glare of foreign competition, has now come to recognize this. Research cooperatives are the industry's response to this problem.

Research Cooperatives

Cooperatives generally plan, promote, coordinate, sponsor, and conduct generic research on semiconductor materials, design, and fabrication. They generally involve the cooperation of several semiconductor manufacturers, equipment and materials vendors, a university, and a state or federal government.

The university usually serves as the hub or physical location of the cooperative. Examples of such cooperatives are: The Semiconductor Research Corporation, The Microelectronics Center of North Carolina, The Center for Contamination Control centered at the University of Arizona, The Microcontamination Research Center at the University of Minnesota, and the Center for Integrated Studies at Stanford University.

THE CENTER FOR INTEGRATED SYSTEMS

DATAQUEST recently visited The Center for Integrated Systems (CIS) at Stanford University in Palo Alto, California. CIS is a joint effort by government, industry, and the university for the design and fabrication of VLSI chips. It was conceived, in part, as a response to the success Japan has had in cooperative research. CIS, however, emphasizes that it is not an imitation of the Japanese model; it respects the cultural differences between the two countries. CIS stresses that it is American, and that it plans to draw on American institutions to achieve cooperation and coordination of basic research objectives among competitors.

CIS has 20 industry sponsors. Each sponsor contributed $750,000 for the construction of CIS' 71,000-square-foot, state-of-the-art facility. The sponsors are able to send researchers to the CIS facility to help plan and engage in basic semiconductor research. Each sponsor is provided with permanent office space at CIS. The 20 sponsors are listed in Table 1.

The research facility occupies 13,000 square feet of class 100/10 fab area, which is separated from the rest of the facility by vibration dampers. A computer controls both humidity and temperature, with maximum temperature fluctuations of 1 degree C in the main laboratory and 0.2 degree C tolerance range in the lithographic and electron beam areas. Cost of the fab area is estimated at $600 per square foot.

Manufacturing Science

At CIS, professionals from computer science, information science, applied physics, chemical engineering, material science, and from the Stanford University School of Business work together to produce systems that they probably could not have developed working alone. Research is carried out on the fundamental principles of integrated circuits by physicists, integrated circuit engineers, and application engineers. Working right alongside these physicists and engineers are computer and information scientists, who develop tools to design and test the circuits.

Of particular interest to SEMS is the emphasis that CIS has put on research into semiconductor factory-level productivity relationships or manufacturing science. Research is under way in such areas as manufacturing automation, equipment models, manufacturing process models, testing and yield modeling, and factory modeling and management.

Manufacturing science is beginning to be recognized as essential to the advancement of microelectronics. Manufacturing science research at CIS is now investigating throughput and turnaround time as functions of operating policy, the nature of demand, and the gross characteristics of equipment and supervisory control mechanisms.

CIS is currently working on a computer-automated fabrication project. This project is bringing state-of-the-art techniques to bear on problems of operation, control, management, and measurement of the fabrication facilities.

CIS is also engaged in developing models for control and automation of the steps involved in VLSI circuit fabrication. These models will be of two kinds--one for equipment and one for process.

Stanford University's IC lab has developed a model called SUPREM (Stanford University Process Engineering Model) for simulating the IC fabrication process. SUPREM is able to simulate such fabrication steps as ion implantation, impurity diffusion, oxide growth, and interconnection in its program. CIS plans to use SUPREM to study both the application

and development of these processes in the manufacturing environment. With its state-of-the-art fab and SUPREM, CIS will focus on 1-micron CMOS fabrication process variations.

CIS is also studying the areas of testing and yield modeling. Its overall goal is to develop tools and methodologies to reduce development time of new IC technologies. CIS has already developed many such tools and methodologies. For example, CIS developed ion implant and linewidth uniformity evaluation test structures for in-process monitoring, and contact resistance distribution and metal defect density test structures for determining of end-of-process defect density statistics.

In addition to focusing research on manufacturing productivity at the level of individual wafers or lots, CIS will focus on system-level productivity relationships. It will seek to understand how aggregate measures of factory performance depend on operating policy, on the nature of demand, and on the gross characteristics of equipment and supervisory control mechanisms.

RESEARCH COOPERATION ACHIEVED

DATAQUEST has noted a comparative lack of cooperation between U.S. device manufacturers and equipment vendors when contrasted with similar relationships in Japan. CIS, through beta-site relationships, is a deliberate attempt to change this situation. Genus, Inc., for example, in association with the CIS staff, was able to test its tungsten silicide reactor before its introduction.

In summary, CIS is trying to break down the traditional separation of manufacturing and science, to the benefit of both disciplines. CIS is a unique partnership between academia, industry, and government for the study and advancement of integrated systems. It brings together researchers from such fields as computer science, integrated circuit engineering, solid-state physics and others, to advance not only the science of integrated circuits, but also their practical arts.

George Burns

Table 1

CIS SPONSORS

Digital Equipment	Monsanto
Fairchild Semiconductor	Motorola
GTE	Northrop
General Electric	Philips/Signetics
Gould	Rockwell International
Hewlett-Packard	TRW
Honeywell	Tektronics
IBM	Texas Instruments
ITT	United Technologies
Intel	Xerox

Source: CIS

Nielsen Dataquest RESEARCH BULLETIN

SEMS: 1985 Newsletters: September

SEMICONDUCTOR INDUSTRY PULSE: FAINT GLIMMERS OF SUNSHINE AMID THE GLOOM

U.S. semiconductor consumption continues to fade as the book-to-bill ratio remains well below one. Currently, it appears that growth in semiconductor consumption will not resume before the first quarter of 1986. Nonetheless, some faint glimmers of sunshine are beginning to pierce this gloomy picture. There are signs that the excess inventory accumulation of 1984 may be nearing an end, that discrete and linear demand has already turned upward, that effective capacity has been significantly reduced, and that semiconductor purchasing managers are even beginning to be concerned about parts shortages in 1986.

CONSUMPTION BY SEGMENT

The table below shows DATAQUEST's estimates for the change in consumption by industry segment. Note the sharp decrease in the memory market.

ESTIMATED U.S. SEMICONDUCTOR CONSUMPTION
(Millions of Dollars)

	1984	1985	Percent Change
Memory	$ 3,773	$2,222	(41.1%)
Microdevices (MOS)	1,750	1,188	(32.1%)
Logic	4,215	2,977	(29.4%)
Linear	1,366	1,070	(21.7%)
Discrete/Opto	2,229	1,688	(24.3%)
Total Semiconductor	$13,333	$9,145	(31.4%)

Source: DATAQUEST

Excessive inventory accumulation always occurs during a rapid growth year as delivery times lengthen and buyers increase their stocks of parts to protect themselves. This reverses on the down side and leads to a demand for semiconductors far below their actual use in end equipment. DATAQUEST believes that this cycle should end sometime during the fourth quarter of 1985, leading to an increase in bookings at that time.

Discrete/opto and linear demand, both bookings and billings, have already turned upward. DATAQUEST believes that inventory accumulation was significantly lower in this sector of the industry and that the upturn in discrete demand will be followed by increased demand for integrated circuits.

Effective capacity has been reduced through shortened workweeks and layoffs, and future capacity will be further reduced through the curtailment of capital spending plans both in the United States and Japan. U.S. spending in 1985 has been reduced 24 percent from 1984 and Japanese spending has been reduced 18 percent in yen. The reduction in Japanese capital spending is particularly significant, since it constitutes the first reduction since DATAQUEST has been keeping records. Estimated quarterly consumption for 1985 and 1986 is shown below.

ESTIMATED U.S. QUARTERLY SEMICONDUCTOR CONSUMPTION
(Millions of Dollars)

	1984	Q1	Q2	Q3	Q4	1985
Discrete	$ 2,229	$ 448	$ 430	$ 403	$ 407	$ 1,688
IC	11,104	2,328	2,068	1,675	1,386	7,457
Total	$13,333	$2,776	$2,498	$2,078	$1,793	$ 9,145
Percent Change	51.5%	(19.5%)	(10.0%)	(16.8%)	(13.7%)	(31.4%)

	1985	Q1	Q2	Q3	Q4	1986
Discrete	$ 1,688	$ 431	$ 465	$ 480	$ 510	$ 1,886
IC	7,457	1,436	1,824	2,184	2,712	8,156
Total	$ 9,145	$1,867	$2,289	$2,664	$3,222	$10,042
Percent Change	(31.4%)	4.1%	22.6%	16.4%	20.9%	9.8%

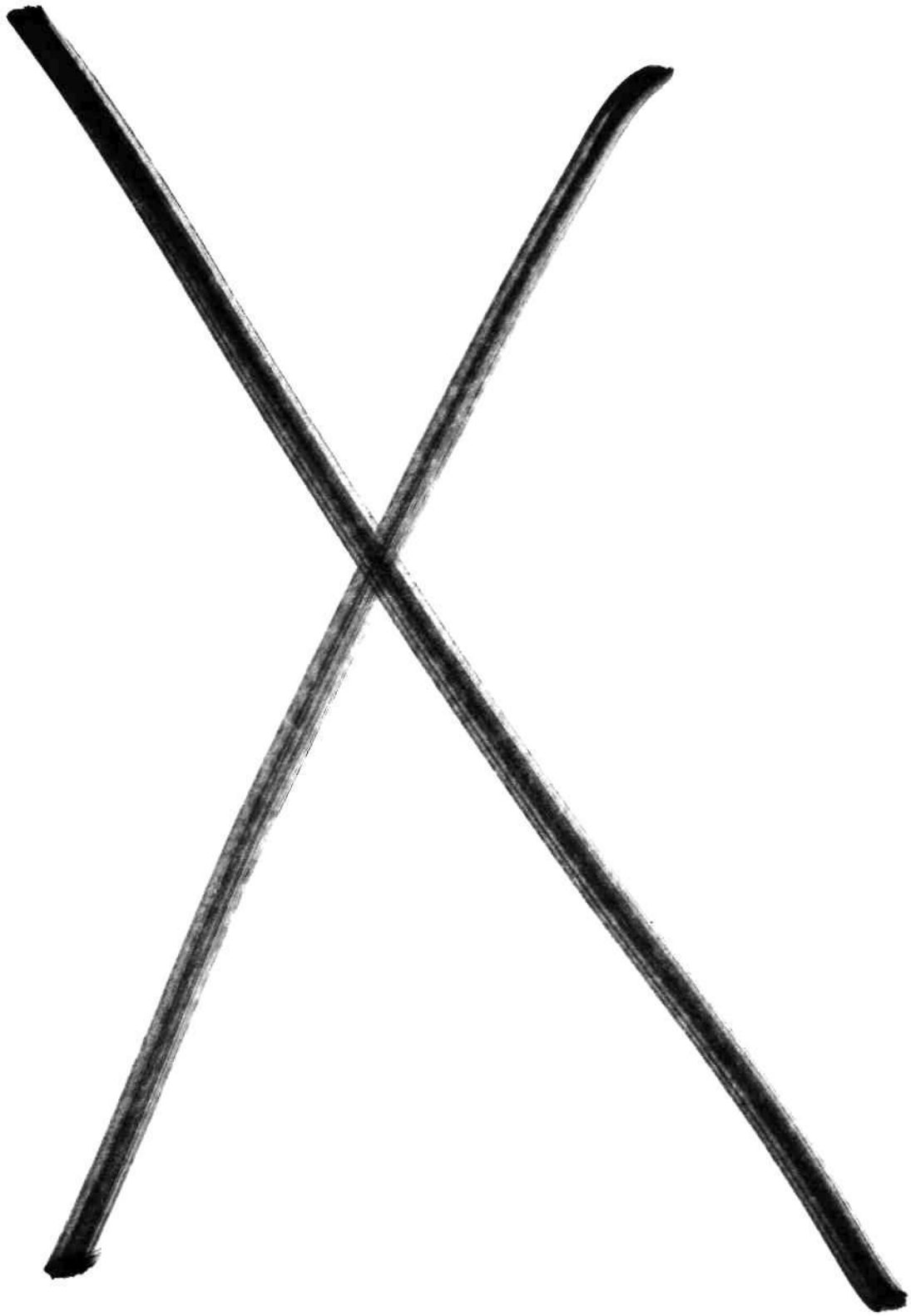
Source: DATAQUEST

THE ECONOMY

DATAQUEST believes that the U.S. economy, while not robust, will not experience a significant decline in 1986. Instead, it will simply stumble along its present course with neither a boom nor a bust. With this scenario, there should be enough growth in end equipment demand to allow semiconductor consumption to return to higher levels as inventories are depleted and prices halt their precipitous decline.

(This newsletter is reprinted with the permission of DATAQUEST's Semiconductor Industry Service.)

Robert McGeary
Howard 2. Bogert
Barbara Van



October Newsletters

The following is a list of the material in this section:

Nielsen Dataquest RESEARCH NEWSLETTER

SEMS Code: 1985-1986 Newsletters: October

NINTH ANNUAL SIA FORECAST DINNER: FORECASTING THE RECOVERY

SUMMARY

The Semiconductor Industry Association's ninth annual forecast dinner was held amid a mood of optimism combined with deep concern for the future viability of the U.S. semiconductor industry.

The evening began with a roast of retiring SIA president Tom Hinkelman and was emceed by Charlie Sporck, president of National Semiconductor Corporation. The featured speakers were Dr. Gil Amelio, president of Rockwell International's semiconductor products division, and Dr. Bob Noyce, vice chairman of Intel Corporation.

Mr. Sporck compared the U.S. semiconductor industry to a football player who is bleeding from an injury in a game where the competition is not penalized for breaking the rules. Although the U.S. industry has managed to survive under these conditions, the bleeding has not stopped. He called for forced change through "forms of leverage that some may call protectionist."

FORECAST

Dr. Amelio presented the consensus forecast for 1985 through 1986, which was prepared by the World Semiconductor Trade Statistics (WSTS) forecast committee, comprising representatives from 30 semiconductor manufacturers worldwide.

The WSTS forecast calls for a worldwide consumption decline of 17 percent in 1985, followed by three years of growth: 18 percent in 1986, 23 percent in 1987, and 23 percent in 1988. Over the long term, Japan will be the fastest-growing market, gaining several points in world market share in 1985 and maintaining them through 1988. Dr. Amelio pointed out that NMOS and PMOS memory are still showing no sign of recovery, while analog ICs are doing well, particularly in Japan, where the consumer electronics market is still fairly strong. Bipolar digital ICs are also doing well, having maintained a book-to-bill ratio of 1.0 since May.

Dr. Amelio pointed to several causes of 1985's disastrous market decline:

- A slowdown in the OEM market, particularly computers, which account for 40 percent of the U.S. semiconductor market
- A huge semiconductor inventory at OEMs (estimated to have been between $2 billion and $2.5 billion)

He believes that end users (i.e., consumers and businesses) have slowed consumption because they want more innovative products. OEMs will continue to slim down their semiconductor inventories as part of better asset management, but eventually demand will firm, as will prices. Finally, new, innovative products will spur end-user demand.

U.S.-JAPAN TRADE

Dr. Noyce's topic was U.S.-Japan trade friction. While admitting that many unfair trade practices do exist on the part of the Japanese, he believes that unfair practices are not the sole cause of the U.S. industry's current dilemma. Prior to 1980, the United States enjoyed years of trade surplus. Since 1980, however, the U.S. trade deficit has escalated dramatically. U.S. manufacturers are no longer competitive in the world market, Americans are substituting foreign sources of goods and services for domestic sources, and thousands of formerly U.S. manufacturing jobs are being moved offshore.

Dr. Noyce stated that the high value of the U.S. dollar bears a direct relationship to the current U.S. savings and trade deficits. The implication of this is that if the U.S. savings rate increases to the point of becoming a savings surplus, the U.S. dollar will fall in value and the trade deficit will become a trade surplus. Approximately 65 percent of U.S. corporate profits go into savings, while only 4.5 percent of personal income is saved. If President Reagan's tax proposal is passed, shifting more of the tax burden onto corporations and off of individuals, the resulting decrease in corporate profits would lower the corporate savings rate, decrease net savings in the country, and increase import penetration by $22 billion.

Dr. Noyce concluded that the solution to the problem is in the hands of the United States, which must produce a surplus of goods to send overseas, rather than bringing in goods from other countries. This can be done by increasing personal and government savings.

DATAQUEST ANALYSIS

A dichotomy of opinion on the trade issue was clearly in evidence at the dinner. Although most attendees agreed that free trade is best in the long run, many called for short-term protectionist measures. Even those against any form of protectionism would probably agree with Mr. Sporck's often-repeated rallying cry: "Protectionism beats extinction any day."

Robert McGeary
Patricia S. Cox

Nielsen Dataquest RESEARCH NEWSLETTER

SEMS Code: Newsletters

PUSHING IMPURITIES TO 1 PPB: JAPANESE CHEMICAL INDUSTRY LEADS THE WAY

Higher device yields, and ultimately higher profits for semiconductor manufacturers, are intimately related to the low levels of particulate and chemical contaminants in the wafer fabrication environment. However, for impurity and particulate levels in process chemicals, the issue of exactly "how low is low enough?" has yet to be determined. Semiconductor manufacturers, in particular, are concerned that the present quality of available chemicals is insufficient for future devices as line geometries continue to approach the submicron range. While the U.S. semiconductor and chemical industries continue to explore the issue of revising current chemical specifications to meet present and future processing needs, DATAQUEST believes that the Japanese chemical industry has a significant lead over U.S. manufacturers in its efforts to reduce contaminants in processing chemicals.

This issue was recently addressed at the Second Annual Microcircuit Pure Materials Conference, held in August in San Jose, California. DATAQUEST believes that the information presented at the conference is of significant importance to warrant the attention of our clients.

TRACE IMPURITIES IN PROCESS CHEMICALS

While the standard maxim in the semiconductor industry has always been "cleaner is better," investigations are underway to establish a direct quantitative relationship between process chemical impurity and particulate levels, and wafer yields. Texas Instruments (TI) has recently embarked on research to examine the difference in the quality of chemicals used in its 256K DRAM facilities in Miho, Japan and Dallas, Texas. The early results on metal impurity levels in liquids supplied by Japanese and American chemical companies is quite revealing. The 1 part per billion (ppb) level that TI is encouraging U.S. chemical companies to meet in 1988 is already a reality today with Japanese process chemicals.

Table 1 is a brief summary of trace metal impurity and particulate levels for several chemicals examined by researchers at Texas Instruments. The Japanese specifications, the majority of which have been verified by the TI researchers, are compared with what TI describes as its 1985 Control Specs, which reflect the average level of metal impurities and particulate levels in liquids supplied by U.S. manufacturers. The Semiconductor Equipment and Materials Institute (SEMI) specifications refer to the levels suggested by SEMI as minimum standards for process chemicals used in wafer fabrication. Chemicals supplied by U.S. manufacturers are typically at least an order of magnitude "cleaner" than a SEMI label designation may indicate. However, researchers at TI have yet to find a single American chemical manufacturer that can meet the Japanese specifications.

Table 1

METAL IMPURITY SPECIFICATIONS IN PROCESS LIQUIDS

Chemical	1985 Japanese Specs	1985 TI Control Specs	1985 SEMI Specs	1988 Proposed Levels
Ammonium Fluoride				
Trace Metal	5 ppb (max)	5-250 ppb	100-1,000 ppb	1 ppb
Particle Count	8,239	40,000	-	10
Hydrofluoric Acid				
Trace Metal	1 ppb (max)	10-500 ppb	10-1,000 ppb	1 ppb
Particle Count	868	30,000	-	10
Nitric Acid				
Trace Metal	1-100 ppb	N/A	50-1,000 ppb	1 ppb

N/A = Not Available

Note: Particle count represents number of particles >0.5 micron per 100 milliliters.

Source: Texas Instruments

LIMITS OF DETECTION

The SEMI specs and 1985 Control Specs in Table 1 are reported as ranges in ppb levels, which represent the ranges of individual contributions of the various trace metals. The Japanese specifications for all trace metals however, are reported at essentially the same level. Determination of trace metal levels is dependent on the detection

limit of the analytical instrumentation being used. For example, when a liquid sample is concentrated, it is possible to "see" product in measurable amounts that previously might have been reported merely as a detection limit. It is clear that for part-per-billion levels to be measured in a reliable fashion, accurate and certified standards for instrument calibration must be developed on an industry-wide basis.

LIMITS OF TOLERANCE

SEMI has proposed guidelines for semiconductor-grade chemical specifications and analytical procedures based on the standards of the American Chemical Society for reagent grade materials. The SEMI standards for chemical impurity levels are recognized as maximum allowable limits of impurities for chemicals used in fabrication processes, and are meant to represent a consensus standard that a variety of sources in the chemical industry can meet. Semiconductor manufacturers are concerned, however, that the range of tolerance for specific impurities allowable by a SEMI specification label is too large. In particular, the issue of lot-to-lot variation in chemical purity for materials supplied by a single vendor is of critical importance as the industry continues to move toward automating fabrication facilities, where the reproducibility of materials and processing performance is essential. With lower levels of impurities, acceptable tolerance ranges will decrease accordingly.

PARTICLE ADHERENCE TO WAFERS

While the level of dissolved impurities in a given liquid is of great significance in judging its quality, it has been recognized by the semiconductor industry that control of particulates is of primary concern. In particular, it is of critical importance to determine how many particles actually adhere to a silicon wafer after being exposed to a wet chemical environment. In a second set of studies, Texas Instruments established an analytical methodology to measure particles adhering to silicon wafers that have been exposed to hydrofluoric acid (HF) supplied by both U.S. and Japanese manufacturers. The analytical determination of particulate contribution from HF entails first measuring the particles already present on bare silicon wafers, rinsing the wafers, drying them, and then repeating the measurement procedures. The results are presented in Table 2, and reflect particulate levels that have been corrected for initial background contamination of the wafers as well as contributions from a deionized water dump rinser and spin rinse dryer. These results are taken as additional evidence that the Japanese chemical companies are able to provide a substantially better quality of low-particulate chemicals.

Table 2

PARTICLE COUNT SUMMARY

Supplier	Particles Added per 6" Wafer (> 0.5 Microns)
49% HF--U.S. Supplier A	450 +/- 50
49% HF--U.S. Supplier B	320 +/- 116
49% HF--Japanese Supplier	111 +/- 47
5% HF--U.S. Supplier A	300 +/- 132
5% HF--U.S. Supplier B	284 +/- 95
5% HF--Japanese Supplier	43 +/- 10
Dump Rinser Contribution	16 +/- 8
Spin Rinse Dryer Contribution	10 +/- 12

Source: Texas Instruments

MAINTAINING PURITY IN A POST-MANUFACTURING ENVIRONMENT

Two other areas that the Japanese chemical companies have addressed are the control of particulate levels in process chemicals after manufacturing and getting the chemicals to the equipment in the fab. Particles are generated from chemical containers and storage vessels. Since filtration efficiency is always based on the removal of a given percentage of particles in a single cycle, the cleaner the chemical is to start with, the better. A major Japanese chemical company, for example, has designed a recirculating filtration system for its liquid chemicals in which the integrity of the material is continuously upgraded during storage at the vendor's site. The 20-liter volume system requires little supervision or maintenance beyond regular replacement of 0.2-micron filter cartridges, and yet provides a constant source of ultralow particulate chemicals directly to the point of packaging. In a sample of nitric acid, the number of particles between 0.5 and 1.0 microns per milliliter has been reduced from 150 to 4 after the equivalent of seven circulation cycles.

In addition, the Japanese chemical industry maintains the integrity of chemical quality in its delivery to semiconductor processing equipment by using direct distribution from vendor-owned drums or other containers that are kept in the chase. While U.S. manufacturers are moving in this direction, we believe that a dedicated commitment on the part of the Japanese chemical industry to returnable containers, teflon containers, and direct distribution systems, has given the Japanese a head start over their U.S. counterparts.

AN ISSUE OF ECONOMICS

Ultimately, the issue of purity translates to one of economics. Are U.S. semiconductor manufacturers willing to specify higher purity levels as a purchasing requirement to the chemical industry, and willing to pay for the corresponding increase in costs? Will those additional manufacturing costs to the semiconductor firms be recovered in increased wafer yield, and thus in a lower manufacturing cost per device? In an alternative approach, what are the economic advantages for a semiconductor company to manufacture high-purity chemicals in-house, or produce low-particulate chemicals on-line? Clear-cut answers to these questions are not available at this time. The one question that must be addressed however, is whether the industry can afford to wait. DATAQUEST believes that the Japanese chemical companies already have a strong interest in supplying the U.S. semiconductor industry as well as their own. Several U.S. semiconductor manufacturers have been approached by Japanese chemical companies with offers for process chemicals free of charge, other than shipping, which we interpret as a bid for a share in an essentially untapped market.

LOOKING AHEAD

We encourage the U.S. chemical industry to continue efforts to reduce particulate levels in wet chemicals and to meet the 1-ppb trace metal impurity levels before 1988, if it wishes to prevent a possible erosion of market share on the home turf. Ongoing research at Texas Instruments and other facilities will continue to probe the issue of contaminant level correlations with subsequent device yield. However, we know that Japanese semiconductor manufacturers regularly obtain higher yields than U.S. manufacturers, and it is apparent that higher-quality chemicals are also being supplied to the Japanese fabs. While chemical quality is only one factor in the manufacturing operation represented by materials, equipment, and processing, it appears that a focused attention to detail continues to benefit the Japanese semiconductor industry in its goal for higher wafer yields, and ultimately higher profits.

Peggy Marie Wood

Nielsen Dataquest RESEARCH NEWSLETTER

SEMS Code: 1985 Newsletters: October

CAPITAL SPENDING: JAPAN TO CONTINUE TO OUTSPEND UNITED STATES

SUMMARY: THE UNITED STATES, JAPAN, AND EUROPE

Nineteen eighty-five, the year that has brought so much pain to semiconductor manufacturers, has also been bad news for capital equipment manufacturers. Total 1985 worldwide capital spending for semiconductor property, plant, and equipment (PPE) is expected to be slightly over $6 billion . This is down almost 22 percent from 1984. U.S. merchant capital spending is expected to be $2.3 billion in 1985, down 24 percent from 1984. Japanese capital spending will be approximately $2.6 billion, a decrease of 24 percent from 1984. European spending is expected to be slightly less than $0.4 billion, a 15 percent decrease from 1984 levels, while the ROW is expected to be up 15 percent to slightly more than $0.2 billion. Captives are expected to spend approximately $0.5 billion in 1985, a 5 percent increase over 1984 (see Table 1).

Table 1

WORLDWIDE MERCHANT CAPITAL SPENDING
(Millions of Dollars)

	1984	1985	1986	1987	1988	1989	1990	CAGR 1984-1990
United States	$3,051	$2,323	$2,291	$3,651	$ 5,073	$ 4,766	$ 5,290	9.6%
Japan	3,460	2,623	2,989	4,117	5,400	5,439	6,676	11.6%
Europe	450	381	430	562	811	926	1,120	16.4%
ROW	201	220	275	406	606	648	810	26.1%
Captive	582	511	504	803	1,116	1,048	1,164	12.3%
Total	$7,744	$6,058	$6,489	$9,539	$13,006	$12,827	$15,059	11.7%
Growth	78.5%	(21.8%)	7.1%	47.0%	36.3%	(1.4%)	17.4%	

Source: DATAQUEST

Spending by U.S. and Japanese companies account for over 80 percent of the worldwide total. In 1983, Japanese capital spending exceeded U.S. merchant capital spending for the first time. Our projections show that they will continue to outspend U.S. merchants through the 1980s. We expect that Japanese capital spending will grow at a compound annual growth rate (CAGR) of 11.6 percent for the period from 1984 through 1990. U.S. capital spending will have a 9.6 percent CAGR for the same period. Capital spending will grow faster in both Europe and ROW (16.4 in Europe and 26.1 percent in ROW). However, since these two areas are starting from a much smaller base, by 1990 they will still barely account for 20 percent of worldwide capital spending.

1985 U.S. CAPITAL SPENDING

As the current industry slump has lengthened, 1985 capital spending estimates by the leading companies that DATAQUEST contacted have also fallen. DATAQUEST now estimates that total U.S. merchant capital spending in 1985 is going to be down 24 percent to $2.32 billion from 1984's $3.05 billion. Capital spending in 1986 will be down again, to $2.29 billion from $2.32 billion in 1985, a decline of 1.4 percent.

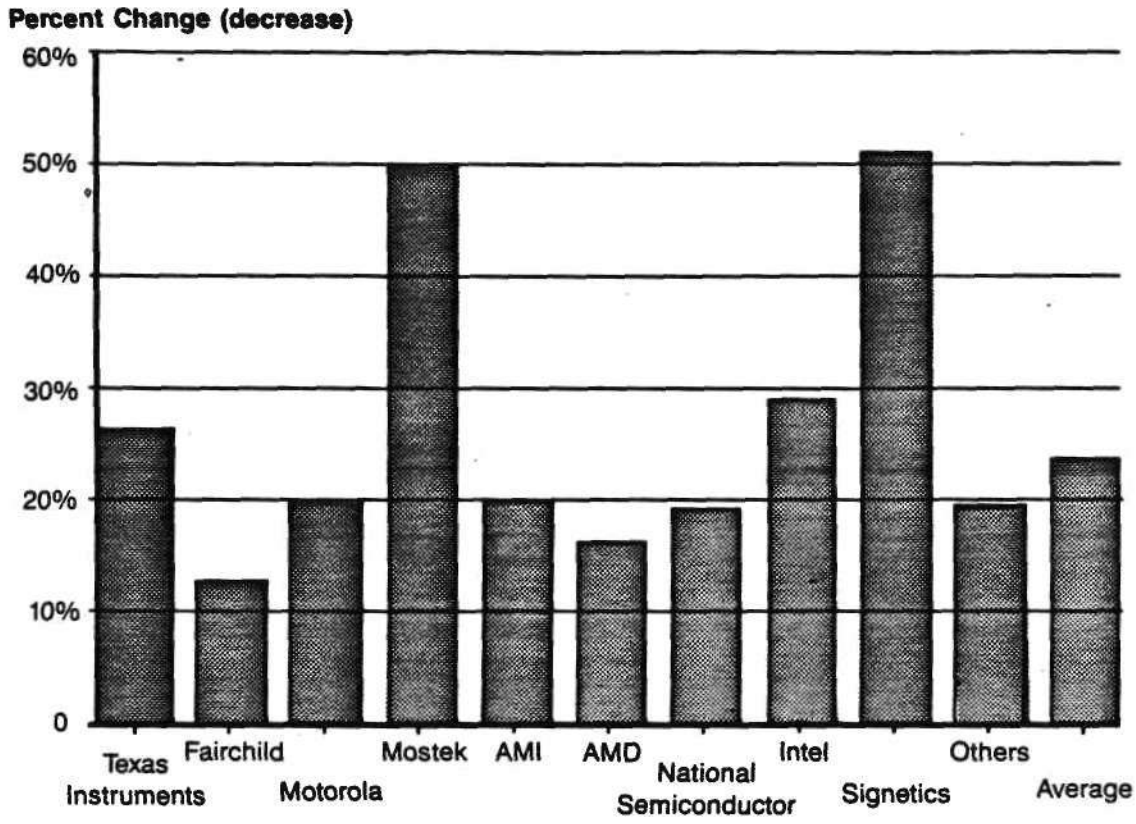
Some companies have cut their spending plans much more than the average (see Figure 1). For example, Signetics plans to cut its capital spending by over 50 percent, and DATAQUEST estimates that Mostek will cut its capital spending by at least that rate.

In overall capital spending, Texas Instruments and Motorola maintained their leadership in the total amount of semiconductor capital spending at $348 million and $330 million, respectively, as shown in Figure 2.

Although capital spending is down sharply from 1984, its drop as a percent of revenue has not been nearly so precipitous. Capital spending as a percent of revenue in 1984 was 21 percent; in 1985, it will be 20 percent. The shape of 1985's capital spending is shifting away from areas of overcapacity toward those technologies where future demand is expected to exceed capacity. Spending to increase sub-2-micron capacity is an example of this. AMD, Fairchild, Intel, Motorola, National Semiconductor, Signetics, and Texas Instruments all report sub-2-micron equipment as a major focus of their spending. Automation to achieve better line balance, increase utilization, and lower contamination and breakage from handling, was also reported to be another major focus of capital spending.

Figure 1

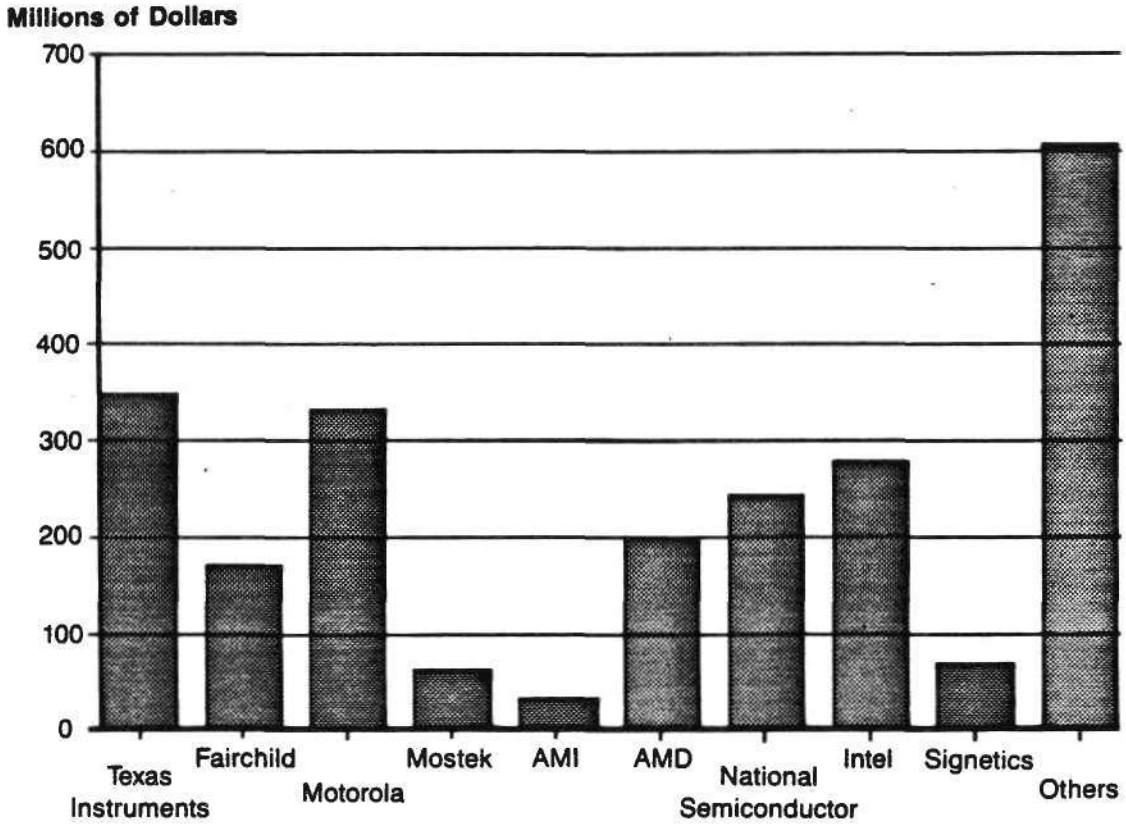
1985 PERCENT DECREASE IN U.S. CAPITAL SPENDING



Source: DATAQUEST

Figure 2

1985 U.S. COMPANY CAPITAL SPENDING



Source: DATAQUEST

JAPANESE 1985 CAPITAL SPENDING

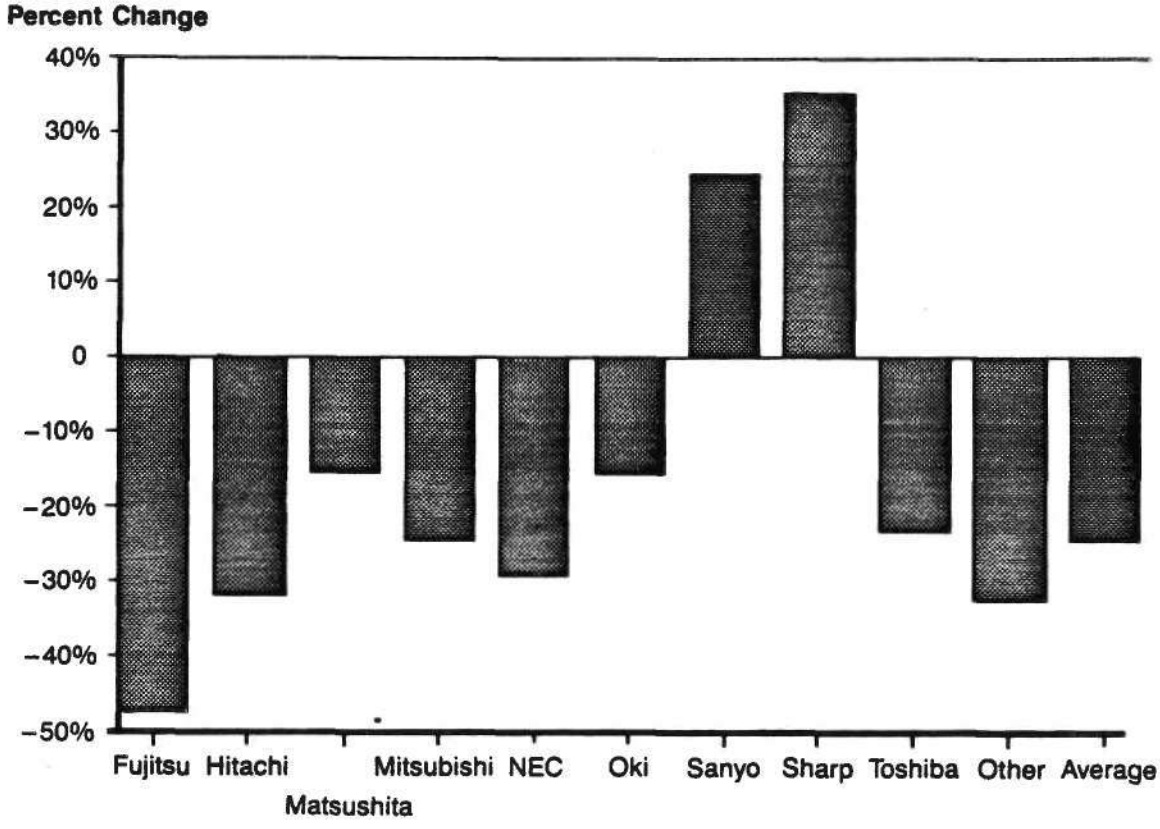
For the first time since DATAQUEST began tracking Japanese capital spending in 1973, Japanese capital spending is down from the previous year. DATAQUEST estimates that expressed in yen, the decrease will be 18.8 percent. Because of the strength of the dollar, this decline expressed in dollars is even greater; DATAQUEST estimates that expressed in dollars, the decline will be 23 percent.

As this newsletter goes to press, Japanese companies are revising their spending plans downward. Hitachi has just announced that it is lowering its capital spending plans even further, to $375 million. This represents a decline of 32 percent from 1984 for Hitachi. Fujitsu plans an even larger percentage decline from 1984. At the 1984 exchange rate, Fujitsu spent $527 billion in 1984. This declined to $280 million in 1985 at current exchange rates, a decline of 47 percent. (See Figure 3 for 1985 Japanese company spending estimates.)

Not all Japanese companies will decrease their spending, however. DATAQUEST is forecasting that Tokyo Sanyo will increase its spending by 25 percent to $148 million, and Sharp will increase its capital spending by as much as 35 percent to $160 million (see Figure 4).

Figure 3

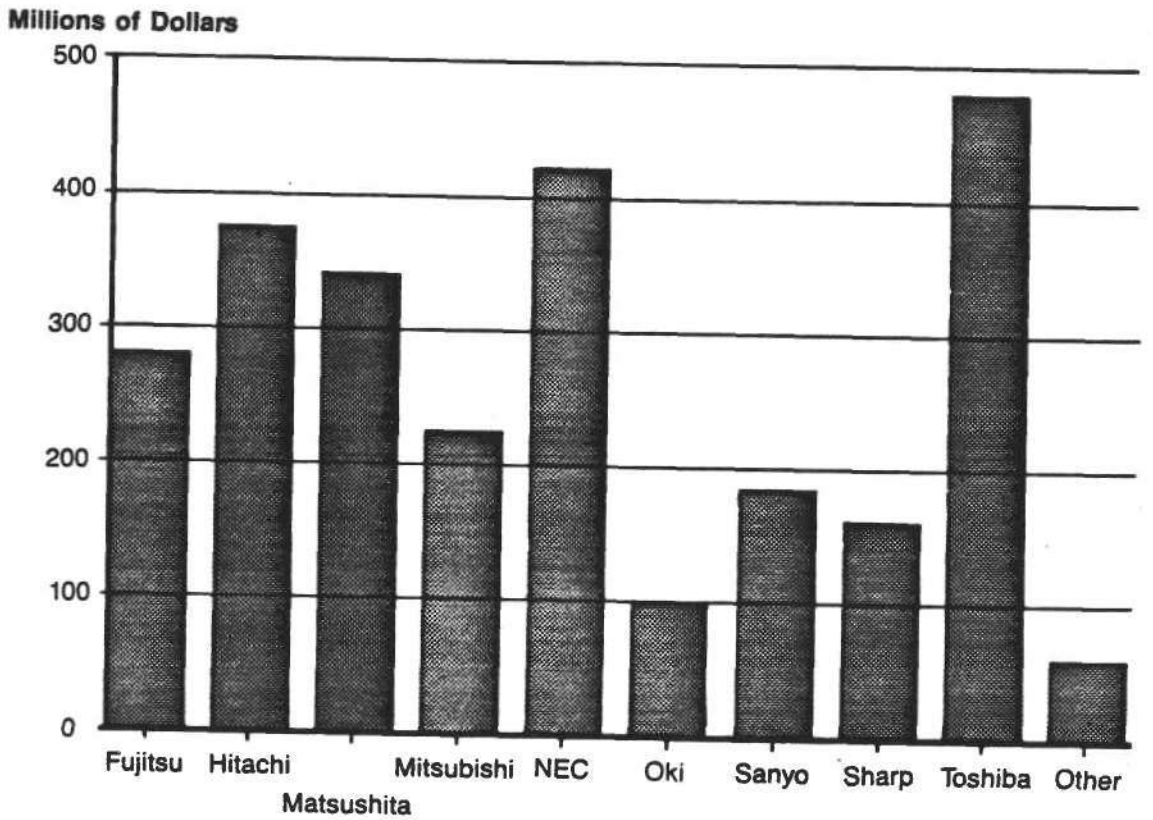
1985 JAPANESE COMPANY CAPITAL SPENDING



Source: DATAQUEST

Figure 4

1985 PERCENT CHANGE IN JAPANESE CAPITAL SPENDING



Source: DATAQUEST

1986 THROUGH 1990 CAPITAL SPENDING

Typically, Japanese capital spending coincides with expansions. That is, as the semiconductor industry enters the expansion phase of the business cycle, Japanese device manufacturers begin to expand their productive capacity. U.S. manufacturers, on the other hand, tend to lag their capital spending approximately seven months behind the semiconductor business cycle. This results in the U.S. industry lacking capacity at the peaks of the business cycle, while their Japanese competitors still have capacity. A further result of this, of course, is that U.S. manufacturers lose market share.

Because Japanese capital spending coincides with expansions and U.S. capital spending lags expansions, we expect that U.S. capital spending as a percent of revenue will fall to 18 percent in 1986, while Japanese spending will increase to 29 percent. Expressed in dollars, this means that U.S. capital spending will decrease 1.4 percent from $2,323 million in 1985 to $2,291 million in 1986. Japanese capital spending, on the other hand, will increase from $2,623 million in 1985 to $2,989 million in 1986, an increase of 14 percent.

European companies and their governments have stated that they are committed to expanding their roles in the semiconductor industry. We are forecasting a capital spending increase from 1985 to 1986 of 16 percent. Over the period covering the rest of the decade, European capital spending will crack the $1 billion barrier in 1990 and will grow at a CAGR of 16.4 percent.

ROW capital spending will experience a CAGR of 26.1 percent from 1984 through 1990, and will reach $810 million in 1990. This is a remarkable growth rate, and certainly represents opportunity for capital equipment manufacturers, as does the European. However, ROW and European capital spending in 1990, will represent less than 25 percent of the market. The United States and Japan will be the powerhouses of the industry throughout the decade. Between them, they will account for almost 80 percent of merchant capital spending in 1990.

STRUCTURAL DIFFERENCES BETWEEN JAPAN AND THE UNITED STATES

We expect Japanese capital spending to be greater than that of the United States through at least 1990 (see Table 1). This is because of some basic structural differences between the two countries. For example, the cost of capital is less in Japan. Furthermore, equity holding and the drive for short-term profits do not drive the industry as strongly as they do in the United States.

Japanese companies are associated with industrial groups, which in turn are centered around leading banks such as Fuji, Mitsubishi, Sumitomo, Mitsui, Sanwa, and Dai-Ichi Kangyo. These associations allow the Japanese companies to carry a higher debt/equity ratio than their U.S. counterparts, and to carry it at about half the cost of capital in

the United States, currently, about 6 percent (Japanese) versus 12 percent (U.S.). In the semiconductor industry, this difference is even greater now that MITI is offering loans for semiconductor equipment at 3 percent rates.

Since Japanese semiconductor manufacturers carry such a high debt/equity ratio, shareholders, and hence profitability, are not as important as in the United States. Some studies indicate that Japanese after-tax margins are one-fourth of United States after-tax margins (1.4 percent Japanese versus 5.6 percent U.S.).

However, cash flow to service the debt is very important to the Japanese. To maintain cash flow, unit volume must be maintained, even in a period of excess capacity. This leads the Japanese industry to emphasize market share rather than short-term profitability. The need to maintain unit volume and cash flow, plus ready access to low-cost capital, gives the Japanese companies a strong impetus to outspend their U.S. rivals in the purchase of capital.

DATAQUEST ANALYSIS

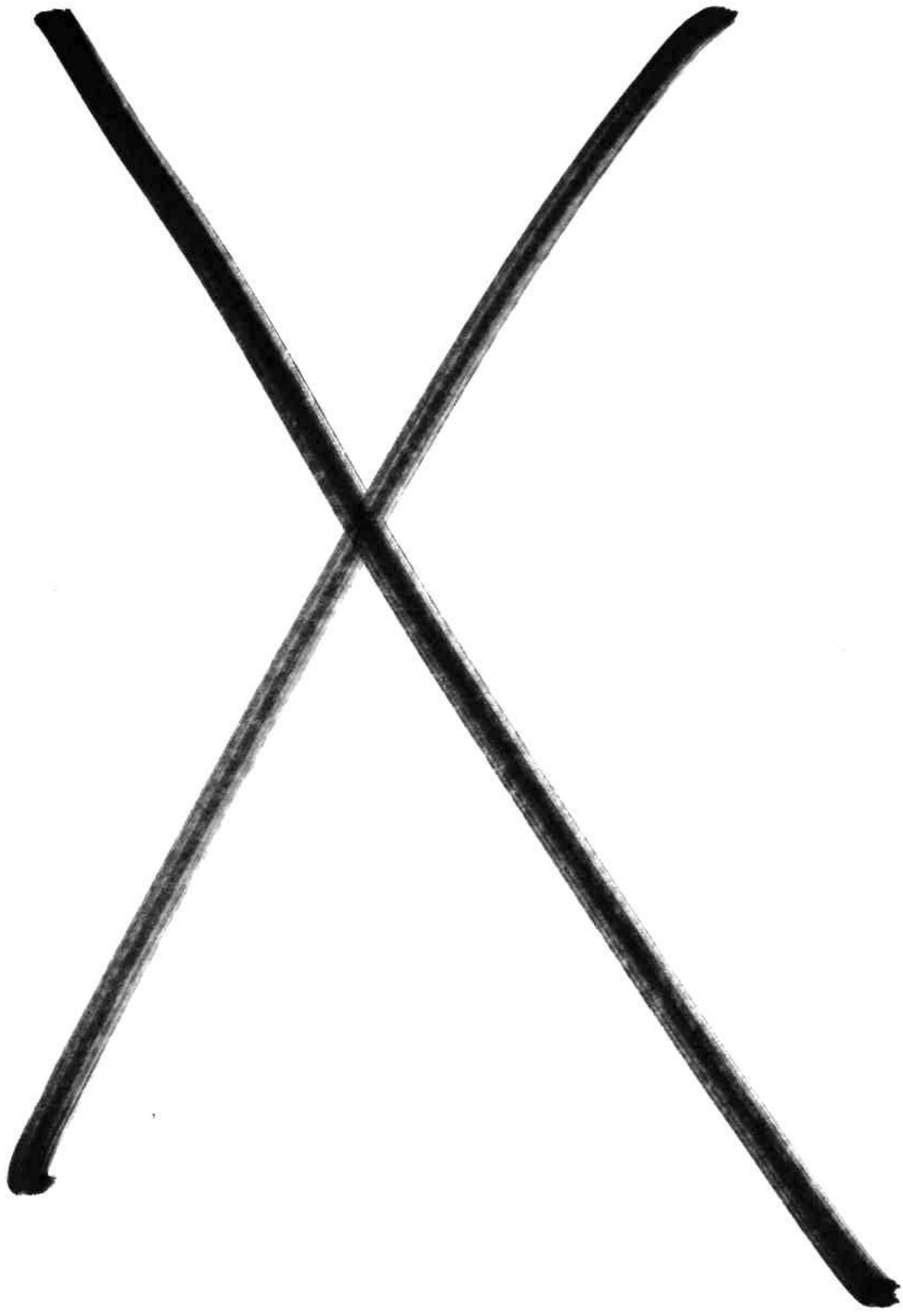
DATAQUEST's latest estimate for North American semiconductor consumption is for a 9.8 percent increase in 1985. This small rise, and the tendency for U.S. semiconductor manufacturers to lag their capital spending by seven months, will cause 1986 U.S. capital spending to be down from $2,323 million in 1985 to $2,291 million in 1986. Japanese spending, on the other hand, will be up 14 percent (from $2,623 million in 1985 to $2,989 million in 1986).

However, despite our forecast of a flat market for the U.S. semiconductor manufacturers in 1986, there will be some opportunity for equipment vendors. Europe, Japan, China, Korea, and Taiwan are expected to increase their capital spending for semiconductor equipment as they attempt to increase market share, and, in the case of China, continue to modernize.

DATAQUEST also expects there to be opportunities for state-of-the-art equipment. Because of products such as 1MB DRAMs, 32-bit MPUs, and VHSIC devices with less than 1.2-micron geometries, we expect to see growing markets for x-ray and E-beam equipment, and for CVD, etch, and reduction steppers, particularly steppers with I-line lenses. Equipment that will increase automation and increase reliability will have a decided advantage and will see a good market.

Slow times are also opportune times for new product introductions and for setting up beta sites. Semiconductor manufacturers are more willing to look at new products when there is less pressure to get existing products out the door. These periods are also excellent for getting feedback from users. This feedback guides vendors in making necessary engineering and manufacturing changes before the next period of high growth--which is inevitable.

George Burns



November Newsletters

The following is a list of material found in this section:

- The Third Wave: The Surge in Semiconductor Start-Ups Continues

Nielsen Dataquest RESEARCH BULLETIN

SEMS Code: SEMS Bulletin

THE THIRD WAVE: THE SURGE IN SEMICONDUCTOR START-UPS CONTINUES

Semiconductor entrepreneurialism is still alive. Despite one of the worst downturns in the industry's history, DATAQUEST observes that semiconductor start-ups are still appearing at a record number. Since 1977, we have recorded 125 start-ups worldwide, an average of one new company every three weeks. Of these 125 companies, 74 start-ups are located in California's Silicon Valley (59 percent), 7 in Southern California, 15 in the Midwest, 9 on the East Coast, 8 in Europe, 8 in Asia, and 4 in Canada. In 1985, there have been 10 new companies, but we expect twice that many by the end of the year. These start-ups have extraordinary staying power. Of the 125 start-ups, only a half dozen have closed their doors.

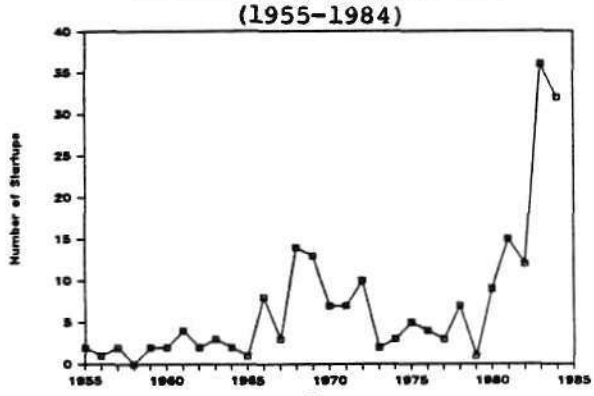
DATAQUEST believes the industry is witnessing its third wave of technological innovation, as shown in Figure 1. During the 1950s, we witnessed the rise of transistor start-ups. In the late 1960s, PMOS and NMOS device makers appeared. Now, a wave of CMOS, gallium arsenide, ASICs, digital signal processing, and specialized linear, power transistor, and graphics start-ups are opening their doors. These start-ups are securing seed capital from foreign venture capitalists, corporate investors, and OEMs, and pursuing strategic alliances. DATAQUEST believes that 1984 will surpass 1983 as the peak year, since most start-ups maintain a low profile for several years (see Table 1).

(This newsletter is reprinted with the permission of DATAQUEST's Japanese Semiconductor Industry Service.)

Robert McGeary
Sheridan Tatsuno

Figure 1

SEMICONDUCTOR START-UPS (1955-1984)



Source: DATAQUEST

Table 1

SEMICONDUCTOR START-UPS
(1983-1985)

1983

Company	Location	Products
Altera Semiconductor	Santa Clara, California	Erasable PLDs
Bipolar Integrated Tech.	Beaverton, Oregon	Bipolar ICs
Calogic Corp.	Fremont, California	DMOS FET arrays
Custom Silicon	Lowell, Massachusetts	ASICs (std. cells)
Elantec	Milpitas, California	High-performance analog
Electronic Technology	Cedar Rapids, Iowa	CMOS ASICs
Exel Microelectronics	San Jose, California	EEPROMs
Hypres	Elmsford, New York	Josephson junction
Inova Microelectronics	Campbell, California	SRAM modules, WSI
Int'l. CMOS Technology	Cupertino, California	Nonvolatile memory
Int'l. Logic Systems Inc. (ILSI)	Colorado Springs, Colorado Santa Clara, California	CMOS and bipolar logic
Iridian Microwave	Chatsworth, California	GaAs FETs
Ixys Corporation	Santa Clara, California	Power monolithics
Lattice Semiconductor	Portland, Oregon	NMOS/CMOS memory/logic
Laser Path	San Jose, California	CMOS logic
Logic Devices	Sunnyvale, California	CMOS DSP
Maxim Integrated Products	Sunnyvale, California	CMOS linear ICs
Metalogic Corp.	Cambridge, Massachusetts	Silicon compiler
Micro Linear Corp.	San Jose, California	IC filters, D/A, A/D
Microwave Technology Inc.	Fremont, California	GaAs FETs, amplifiers
Modern Electrosystems (Hyundai Electronics)	Sunnyvale, California	N/CMOS memory, logic
Mosel	Sunnyvale, California	MOS memory
Novix	Cupertino, California	RISC MPUs
Opto Tech.	Hsinchu, Taiwan	Discretes
Seattle Silicon	Bellevue, Washington	Silicon compiler
Sierra Semiconductor	San Jose, California	CMOS ASICs
Silicon Design Labs	Liberty Corner, New Jersey	Silicon compiler
S MOS Systems (Suwa Seikosha)	San Jose, California	CMOS memory and logic
Texet Corp.	Richardson, Texas	Power ICs, MOS FETs
Tristar Semiconductor (Samsung)	Santa Clara, California	NMOS/CMOS memory and logic
Vatic Systems (Thomsen S.A.)	Mesa, Arizona	ASICs
Visic	San Jose, California	HCMOS memory
Vitelic	San Jose, California	HCMOS memory
Wafer Scale Integration	Fremont, California	ASICs
Xtar Electronics	Elk Grove, Illinois	Graphics ICs
Zoran	Sunnyvale, California	DSP

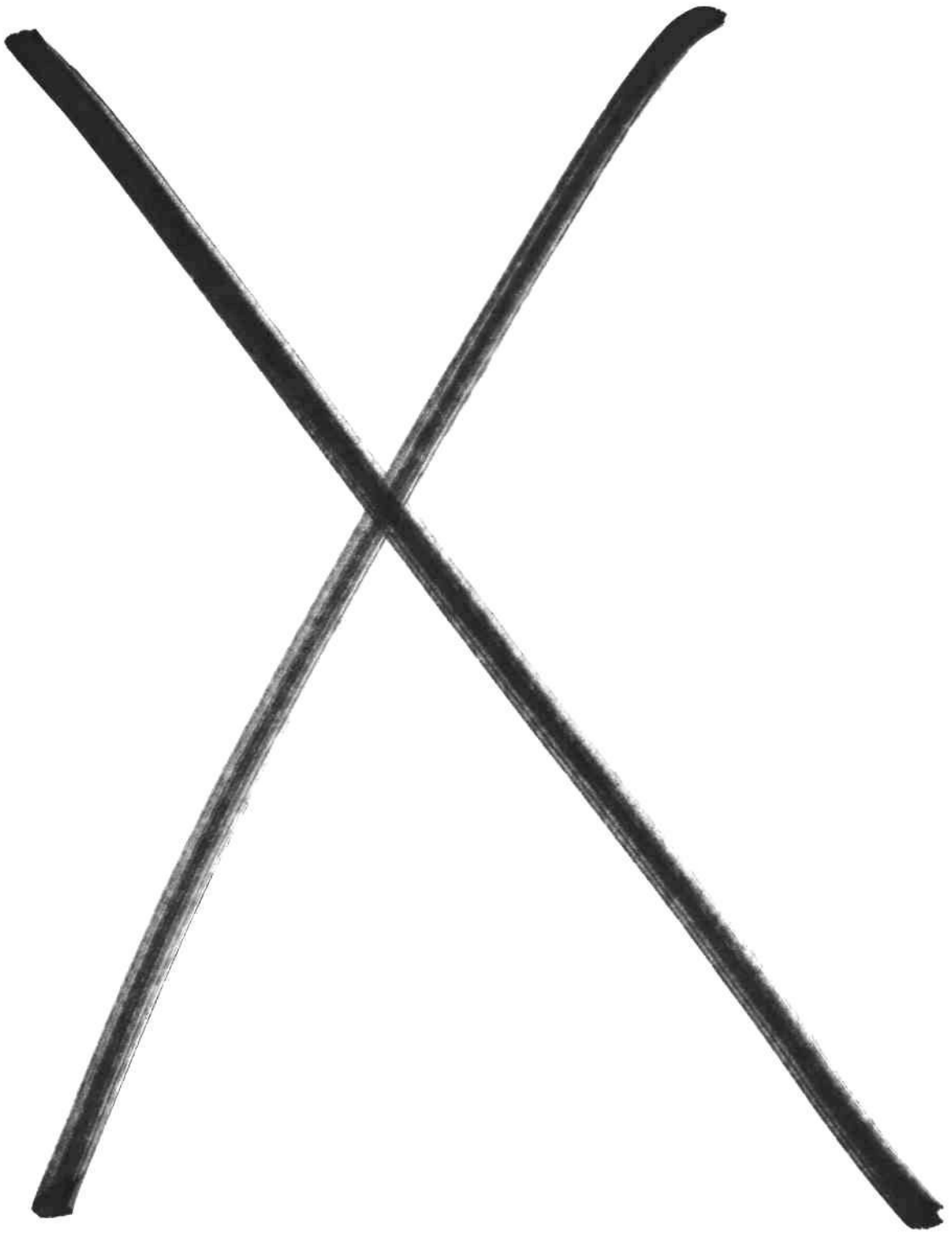
1984

Anadigics	Morristown, New Jersey	GaAs A/D converters
Array Logic	Cambridge, United Kingdom	CMOS, bipolar ASICs
Atmel Corp.	Milpitas, California	EEPROMs
Calmos Systems	Kanata, Ontario, Canada	ASICs
China Ling Lang Microelectr.	Mainland China	ASICs
Chips & Technologies Inc.	Milpitas, California	ASICs
Crystal Semiconductor	Austin, Texas	Telecom ICs
Dallas Semiconductor	Dallas, Texas	CMOS memory
Exmos Semiconductor	Calgary, Alberta, Canada	Telecom ICs
Ikos Systems	Sunnyvale, California	ASICs
Inova Microelectronics	Campbell, California	MMICs, megabit memory
Integrated Logic Systems	Colorado Springs, Colorado	ASICs, PLAs
Integrated Power Semiconduc.	Livingston, Scotland Santa Clara, California	Linear
Les Technologies OMVPE	St. Laurent, Quebec, Canada	GaAs buffers
Micro MOS	Santa Clara, California	CMOS memory
Micron Semiconductor, Ltd.	Lansing, Sussex	Silicon detectors
Modular Semiconductor	Santa Clara, California	CMOS memory & MPR
NMB Semiconductor	Tokyo, Japan	CMOS memory
Pacific Monolithics	Sunnyvale, California	GaAs MMICs
Performance Semiconductor	Cupertino, California	CMOS MPU/mem/logic
Quasel	Santa Clara, California	CMOS ASMs
Silicon Macrosystems	San Jose, California	CMOS memory
STC Components Ltd.	Paignton, England	GaAs, ASICs, foundry
Taisel	Taipai, Taiwan	Hybrid ICs
Teledyne Monolithic Microw.	Mountain View, California	GaAs analog ICs
Topaz Semiconductor (Hytek)	San Jose, California	DMOS ICs
TriQuint Semiconductor	Beaverton, Oregon	GaAs ICs
Vitesse Electronics	Camarillo, California	GaAs ICs
VTC Inc.	Minneapolis, Minnesota	High-perf. bipolar
Yageo	Taipai, Taiwan	Hybrid ICs
Xilinx	San Jose, California	CMOS logic array

1985

AlM Semiconductor	San Jose, California	AlGaAs opto devices
Acumos (old Semi Processes)	San Jose, California	CMOS gate arrays
Advanced CMOS Devices	Cupertino, California	CMOS memories
Celeritek	San Jose, California	GaAs FET amps
Clarity Systems (Israel)	Sunnyvale, California	ASICs
European Silicon Structures	Munich, West Germany	ASICs
Gain Electronics	Princeton, New Jersey	GaAs ICs
Quodos Ltd.	Cambridge, England	ASICs
Tachonics (Grumman)	Bethpage, New York	GaAs ICs
Unicorn Microelectronics	San Jose, California	ASICs
Wolfson Microelectronics	Edinburgh, Scotland	ASICs, DSP

Source: DATAQUEST



December Newsletters

The following is a list of the material in this section:

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: 1985-1986 Newsletters: December

THE U.S. ECONOMY: BOOM OR BUST?

In a recent visit to DATAQUEST, Joseph W. Duncan, Corporate Economist and Chief Statistician of the Dun & Bradstreet Corporation, shared some of his views on the future of the U.S. economy. Due to the universal nature of the subject matter and the impressive credentials of Mr. Duncan, we believe that his views would be of interest to our clients. Mr. Duncan worked eight years as the chief statistician for the Office of Information and Regulatory Affairs of the U.S. Office of Management and Budget. Previously, he was a research and management specialist at Battelle Memorial Institute where he spent 13 years. Mr. Duncan's education includes receiving a B.S.M.E. degree from Case Institute of Technology, an M.B.A. degree from Harvard Graduate School of Business Administration, and a Ph.D. degree in Economics from Ohio State University. He also attended the London School of Economics.

KEY ECONOMIC ISSUES

With respect to the health of the U.S. economy, Mr. Duncan identified three key questions:

- Will there be a recession in the near future?
- Will activity continue in capital markets?
- Will Congress act to reduce the budget deficit?

Recession

In order to address the likelihood of a recession, one must address the health of principal components of the economy. These vital components are consumer spending--which makes up approximately two-thirds of the GNP--housing starts, business starts/failures, unemployment, capital spending, and inflation.

Consumer spending is expected to remain strong. Contrary to widely held beliefs, Mr. Duncan believes that consumers are not over-extended because monthly payments remain a small percentage of disposable income. The housing market appears to be garnering pent-up demand, as mortgage rates have remained at the pivotal 12 percent for some time now. Rates are expected to drift down below 12 percent, however, which should trigger a very strong housing market.

Business starts are at an all-time high. This bears no correlation to interest rates; rather, it is attributed to a more entrepreneurial spirit and willingness to take risks. While business starts are up, so too are business failures. There are several reasons for this: small businesses pay very high interest rates and are at high risk for failure. Also, liberalized personal bankruptcy laws have made it more acceptable to file bankruptcy claims.

Employment has grown continuously during the last five years. Import activity, which would seem to adversely affect the health of the economy, does, in fact, add jobs in the United States. Thus, import activity together with strengthened demand from overseas markets for U.S. exports, should be bolstered.

Capital Market Activity

Capital spending has been depressed due to uncertainty of its treatment under proposed tax reforms. Yet, Mr. Duncan believes that tax reform will not occur until 1987. Spending is expected to pick up in 1986, along with corporate profits. Corporate cash flow will be up 5 percent in 1985, while profits will be down 5 percent. Inflation will increase as well, but is not expected to exceed a 5 percent annual rate.

We believe that there are two sides to the U.S. economy: production, expressed as gross national product (GNP), and consumption, which we refer to as gross final domestic demand (GFDD). To get a good view of the economy, one should look at both. GFDD measures the strength of demand in the economy by factoring net exports and inventory change out of GNP: GFDD = GNP - change in inventory + imports - exports. As shown in Figure 1, the GFDD points to a healthy market with 3.3 percent growth between the fourth quarter of 1984 and the third quarter of 1985. Forecasts of real GNP identify growth of 2.7 percent for 1985, 3.5 percent for 1986, and 4.5 percent for 1987. Growth in GFDD is forecast to remain higher than GNP growth through the end of 1985.

Congressional Action

It is highly probable that the U.S. economy will not experience another recession until 1989. If Congress acts to pass a budget balancing bill, the economy should experience moderate growth for several years. However, if the deficit is not reduced, interest rates could start spiraling as early as spring of 1986, and a recession would soon follow. We believe Congress will act to balance the budget.

SUMMARY

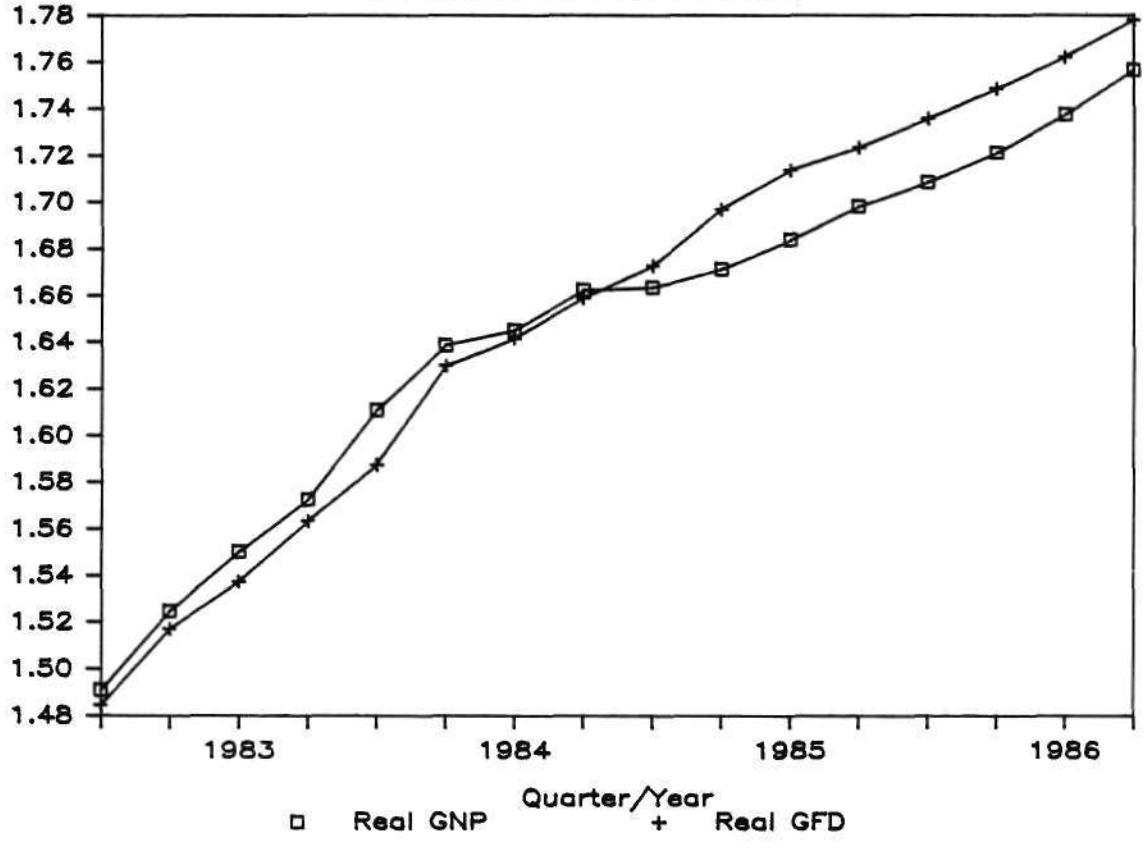
Mr. Duncan identifies a healthy U.S. market. DATAQUEST concurs with his assessment and agrees that 1986 will be a healthy year. Our forecast for semiconductor growth assumes light growth in the first quarter of 1986 with more robust growth in the latter quarters. Our long-range forecast also identifies a recessionary period in 1989. While it is not clear that the semiconductor market clearly follows the GNP, we believe that the overall economy sets the general trend for the health of our industry.

(This newsletter is reprinted with the permission of DATAQUEST's Semiconductor Industry Service.)

George Burns
Barbara A. Van

Figure 1

REAL U.S. GNP VERSUS REAL GROSS FINAL DOMESTIC DEMAND
(Trillions of 1972 Dollars)



Source: Wharton Econometric Forecasting Associates
DATAQUEST

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: 1985-1986 Newsletters: December

GLIMMER OF HOPE DAWNS ON THE SEMICONDUCTOR INDUSTRY

Just as the sky brightens at dawn before the sun rises to warm the earth, the semiconductor industry is showing signs that business will grow, indications that the future looks brighter than we had thought in September. At that time, we could see only "faint glimmers of hope amid the gloom." But the economy now seems to be developing a more robust growth pattern, and this bodes well for the latter part of 1986 and 1987.

THE ECONOMY

DATAQUEST believes that the U.S. economy is strengthening. Inflation is much less dramatic than we thought possible a few years ago, and, indeed, some segments of the economy are experiencing price declines. These segments include agriculture and oil as well as the personal computer and (of course!) semiconductor industries. We believe that the lack of inflation has made it possible for the Federal Reserve to increase the money supply much more rapidly than it could a few months ago. The Fed's accommodative stance should lead to better-than-expected growth in the economy in 1986. The current run-up to new highs in the stock market tends to support this viewpoint.

THE INDUSTRY

Our current forecast for the semiconductor industry is given in Table 1.

Table 1

ESTIMATED U.S. QUARTERLY SEMICONDUCTOR CONSUMPTION
(Millions of Dollars)

	1984	Q1	Q2	Q3	Q4	1985
Discrete	$ 2,229	$ 448	$ 430	$ 402	$ 412	$ 1,692
IC	11,104	2,328	2,068	1,819	1,744	7,959
Total	$13,333	$2,776	$2,498	$2,221	$2,156	$ 9,651
Percent Change	51.5%	(19.5%)	(10.0%)	(11.1%)	(2.9%)	(27.6%)

	1985	Q1	Q2	Q3	Q4	1986
Discrete	$ 1,692	$ 435	$ 471	$ 498	$ 542	$ 1,946
IC	7,959	1,820	2,057	2,226	2,548	8,651
Total	$ 9,651	$2,255	$2,528	$2,724	$3,090	$10,597
Percent Change	(27.6%)	4.6%	12.1%	7.8%	13.4%	9.8%

Source: DATAQUEST

We are still forecasting that U.S semiconductor consumption in 1986 will exceed that of 1985 by 9.8 percent, unchanged from our September forecast. Even so, 1985 will finish out the year some 27.6 percent below the banner year of 1984. However, forecast fourth-quarter consumption of $3,090 million in 1986 will be only 16 percent below the best quarter of 1984 ($3,669 million). If this rate is only sustained in 1987, the growth from 1986 to 1987 will be 17 percent. We do, however, expect growth considerably in excess of this 17 percent in 1987.

There are signs that prices are firming somewhat as producers reduce their effective capacity through layoffs or redirect production into other segments of the market. NEC's recent price increases are encouraging, as is the recent antidumping ruling in the Micron Technology case.

We still have not seen signs that all excess inventory is depleted. Many semiconductor purchasers are still buying directly from their vendors' inventories and, as a result, the "turns" business still constitutes 30 to 50 percent of the shipments of many semiconductor manufacturers. We anticipate that a sharp increase in bookings will occur sometime in the first quarter of 1986, as buyers begin to discover that certain part types are no longer immediately available. This will cause them to place longer-term orders and the "turns" business will decline.

FORECAST COMPARISON

Table 2 compares our current forecast with our previous forecast. Notice that we do not now expect shipments to decline as much in the third and fourth quarters of 1985 as we expected in September. We underestimated the effect of the "turns" business in keeping billings up in the absence of bookings. The higher base of shipments in the last quarters of 1985 makes it possible to achieve the forecast 9.8 percent growth in 1986 with somewhat smaller quarter-to-quarter percentage growth.

Table 2

FORECAST COMPARISON
(Millions of Dollars)

	1985		1986			
	Q3	Q4	Q1	Q2	Q3	Q4
Total Semiconductor						
Sept. Forecast	$2,078	$1,793	$1,867	$2,289	$2,664	$3,222
Dec. Forecast	$2,221	$2,156	$2,255	$2,528	$2,724	$3,090
Percent Change						
Sept. Forecast	(16.8%)	(13.7%)	4.1%	22.6%	16.4%	20.9%
Dec. Forecast	(11.1%)	(2.9%)	4.6%	12.1%	7.8%	13.4%

Source: DATAQUEST

CONCLUSIONS

DATAQUEST believes that the economy is growing stronger and that the semiconductor industry is about to see a resumption of growth. We expect some bookings growth in the fourth quarter and anticipate that the book-to-bill ratio will exceed 1 early next year. With this scenario, 1986 will be a year of recovery and 1987 will be a year of robust growth for the industry.

(This newsletter is reprinted with the permission of DATAQUEST's Semiconductor Industry Service.)

George Burns
Barbara Van

Nielsen Dataquest RESEARCH BULLETIN

SEMS Code: 1985-1986 Newsletters: December

1986 SEMI FORECAST DINNER
TIDINGS FOR THE NEW YEAR: MODEST GROWTH IN 1986

INTRODUCTION

In a climate of mild optimism caused by the news released a few days earlier that the November book-to-bill ratio was 0.90, semiconductor equipment and materials manufacturers gathered for the 1986 SEMI Forecast Dinner. More than 525 people attended this year's dinner, which was held at the Santa Clara Marriott Hotel on December 11. Speech topics included the general economic climate, an analysis of the boom/bust business cycles of the semiconductor industry, and opportunities for equipment manufacturers in the burgeoning ASIC (application-specific integrated circuit) market. The speakers included Jeanette Garretty, an economist and Head of Industry Analysis at Bank of America; Robert Throop, Chairman and CEO of Anthem Electronics, Inc., a semiconductor device distributor; and George Wells, President and CEO of LSI Logic, a major semiconductor manufacturer in the ASIC market. Mel Phelps, Senior Analyst, Research, from Hambrecht & Quist was master of ceremonies for the evening.

MEL PHELPS, HAMBRECHT & QUIST

In his brief introductory remarks, Mr. Phelps noted that semiconductor manufacturers were unusually swift to add capacity during last year's boom in the semiconductor industry. Past history has shown that the semiconductor equipment market usually lags from six and eight months behind the semiconductor industry in the business cycles that characterize the industry. However, during the boom in 1984, equipment manufacturers experienced only a two- to three-month lag behind the peak in semiconductor business. The good news is that 1984 was a great year for the semiconductor equipment industry; the bad news is that sufficient capacity was established in the recent boom to maintain the semiconductor industry through most of 1987.

JEANETTE GARRETTY, BANK OF AMERICA

Ms. Garretty presented a picture of modest economic growth for the United States in 1986; however, she noted that it would not be an easy economy to manage. Bank of America forecasts that the GNP for 1986 will be 2.6 percent versus the 2.4 percent that was observed in 1985. These years of modest growth are in contrast however to 1984 when the GNP established a postwar record of 6.8 percent growth. The United States is experiencing its third year of growth since the 1981/1982 recession, and

Bank of America expects not only relatively stable growth throughout next year, but that the general economic climate will remain unchanged in 1987.

ROBERT THROOP, ANTHEM ELECTRONICS

Robert Throop outlined the inventory dynamics that are the source of the boom/bust nature of the semiconductor industry. In his analysis of the rags-to-riches-to-rags scenario that is typical of the industry, he illustrated that small fluctuations in lead times and demand can cause dramatic shifts in inventory, which in turn affect future lead times. When excess inventories are finally established, the inventory dynamics dictate a lean time of low production levels until the eventual return to the original state of supply and demand, and the cycle can begin anew. Mr. Throop's conclusion was that capacity and demands must be kept in balance, and relatively long lead times must be established to stabilize the boom/bust nature of the semiconductor industry.

GEORGE WELLS, LSI LOGIC

Mr. Wells' talk focused on the opportunities for the semiconductor equipment vendors in the ASICs market segment as this IC market segment continues to grow at high rates. (Note: DATAQUEST estimates that the ASIC market was $3.4 billion of a total IC market of $22.4 billion in 1984 and will grow to $13 billion of a total IC market of $52 billion in 1990.) Clearly, the ASIC equipment market represents a substantial opportunity for the equipment vendors, since historically, semiconductor manufacturers in the United States have poured 20 percent of semiconductor sales back into capital spending.

Mr. Wells noted that ASIC manufacturing is a low-volume, fast turnaround operation typically involving lot sizes of 10 wafers. LSI Logic has 25 new designs per week compared with AMD's chip-per-week program. It is critical in the ASIC market that delivery times for customer prototype chips be kept as short as possible so customers can test the designs in specific applications. Often the delivery time of such chips can mean success or failure for customers in their own markets. The turnaround time for LSI Logic gate arrays was 15 weeks in 1983 dropping to 6 in 1985; its goal is to reach 2 weeks. ASICs will also require that masks be delivered in 24 hours.

ASIC manufacturers will continue to demand that processing equipment allow for substantial reductions in turnaround times. Equipment for ASIC manufacturing has challenging requirements, different from that required for high-volume IC manufacturing. The equipment must be capable of quick turnarounds and have a very fast set-up time. In addition, it should be capable of being operated by semiskilled operators and repaired quickly on a modular basis. Mr. Wells commented that the Japanese equipment vendors were already far ahead of U.S. vendors in this area, and that the United States is in danger of the Japanese gaining penetration in this market. He also noted that he found the U.S. vendors harder to deal with than the Japanese when it came to special equipment requirements. Mr. Wells said that the U.S. equipment vendors should place more emphasis on manufacturing criteria and less on engineering input.

Peggy Wood
Joseph Grenier

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: 1985-1986 Newsletters: December

ROBOTS IN THE SEMICONDUCTOR INDUSTRY: AN APPLICATION IN ITS INFANCY

SUMMARY

The semiconductor industry is being squeezed between two major pressures to adopt advanced automation technology: the market pressure to remain competitive with highly automated Japanese companies, and the push to develop increasingly sophisticated products that require more stringent controls for factory cleanliness. The consensus is that humans must be removed entirely from certain process areas, and possibly the entire fabrication process, to achieve the cleanliness required to manufacture advanced VLSI integrated circuits. There is considerable debate as to the best approach to automating a semiconductor facility. Some of the options include:

- Aisles or tunnels of automation with robots interfacing into the clean tunnels
- Teleoperation in which equipment is controlled from outside the clean room
- Individual work cells where similar types of equipment are clustered together
- A "lights out" factory in which operator-free machines work around the clock, even in darkness

In this newsletter, DATAQUEST examines the issues surrounding robotics automation in the semiconductor industry. Researchers from two DATAQUEST industry sectors, the Robotics Industry Service and the Semiconductor Equipment and Materials Service, combined efforts to explore the following topics:

- Market forces driving the adoption of robots
- Semiconductor manufacturers using robotics
- Channels of distribution and implementation

- Approach to semiconductor automation--United States versus Japan
- Clean room requirements and certification for robots
- Robot vendors--their products, prices, and applications
- Market opportunities and directions for development
- DATAQUEST analysis

Due to the highly competitive nature of the semiconductor industry, there is an unusually high degree of confidentiality surrounding the automation efforts of this industry.

MARKET FORCES DRIVING THE ADOPTION OF ROBOTS

Robots are used in place of humans to interface with process equipment in the clean room. Robots are used in two ways:

- Within a piece of process equipment
- To transfer wafers and/or cassettes between various pieces of process equipment

In some cases, robot systems provide process control feedback into the computer control system.

The major driving forces behind the use of robots include:

- Reducing the number of people present in a fab to lower the defect density, ultimately resulting in increased yields
- Achieving process consistency
  - When the human element is removed, processes are more tightly controlled.
  - Statistical process data collected will show less distribution about the mean.
- Reducing cycle time--perhaps the most significant benefit of automating the factory
  - Cycle time is the time it takes for a batch of wafers to be completely processed; each time a batch is processed, the yields for that process increase because the factory is climbing up the learning curve.
  - If a company's cycle time is less than its competitors', this means that the company is climbing up the learning curve faster and is obtaining higher yields than its competitors--which directly results in a price and market leadership position.

- Achieving shorter product life cycles
  - This motivates manufacturers to be the first to market with new product designs.
  - Robots are particularly advantageous when dealing with leading-edge technology, such as larger and more expensive wafers that must be handled individually rather than in cassettes.
- Making advances in micron/submicron technology with finer circuit lines
  - These advances mandate ultraclean, human-free environments to avoid contamination from ever-decreasing sizes of particulates.
  - New robot models designed for the clean room meet and surpass current Class 10 specifications, and some achieve or approach Class 1 requirements.

SEMICONDUCTOR MANUFACTURERS USING ROBOTICS

The companies currently involved in the automation of semiconductor manufacturing generally are larger, have greater financial resources, manufacture high-volume products, and produce many product designs. These companies include Fairchild, IBM, Mostek, Motorola, National Semiconductor, and Texas Instruments. Initial applications are the most costly, due to engineering design expenses; subsequent applications capitalize on the experience generated from earlier installations, which brings the costs down. Therefore, the multiple system users can make the most cost-effective use of investments in new automation technology.

In many cases, robotic automation is included in the plans for new facilities where the proper emphasis can be given to overall process flow in the facility design and where the location of equipment affects the air flow and cleanliness levels. Robots are also finding their way into existing fabs one at a time, especially as they are incorporated into the process equipment by original equipment manufacturers (OEMs) or by the semiconductor companies themselves.

CHANNELS OF DISTRIBUTION AND IMPLEMENTATION

Distribution of robotic equipment for semiconductor use in the United States differs from distribution in Japan. The following are some of the paths robotic equipment takes to market in the United States:

- Robot vendors provide direct sales and do complete systems installation. This may include clean rooms established by vendors specifically for design and testing of systems prior to sale.

- Robot vendors contract with OEM semiconductor equipment companies to integrate their robots with semiconductor process equipment. A significant number of robot vendors have established or are now negotiating OEM contracts with process equipment suppliers, and DATAQUEST believes that this trend will continue. Robot integration into packaged systems with process equipment is a particularly effective distribution method, as the equipment suppliers have more knowledge of and experience in the semiconductor industry than do most robot manufacturers.

- Systems integrators--companies that integrate robots with other equipment to create functional automated systems--are a major link between robot manufacturers and end users. A number of systems integrators in the United States specialize in electronics applications, and their customers include semiconductor companies. As the new clean room robots become available, these systems integrators are expanding their custom automation services to include semiconductor applications.

APPROACH TO SEMICONDUCTOR AUTOMATION--UNITED STATES VS. JAPAN

Japan is significantly more advanced in the use of robotics in semiconductor production. While the United States takes small, tentative steps to investigate robot capabilities, Japan strides ahead with factory-wide automation of production facilities. A notable example is the new Mitsubishi factory, for which there is no comparable facility in the United States.

Mitsubishi Electric Corporation completed its Saijo semiconductor factory in early 1984. It is a fully automated front- and back-end facility dedicated to the production of 64K DRAMS. It uses automated guided-vehicle systems (AGVSs) that are optically guided to carry cassettes and transfer them to main I/O stations; then robots transfer the cassettes to the processing equipment. The entire wafer fabrication production sequence proceeds without operators ever handling the wafers. All phases of assembly and test, including encapsulation and burn-in, are fully automated. Mitsubishi built its own robots and AGVSs for the factory and even wrote the factory-automation software.

Japan differs from the United States in its reliance on internal resources. There are two reasons for this: it is cost effective to use equipment that was produced internally, and resources from outside suppliers are not as plentiful in Japan. U.S. semiconductor companies turn to vendors and systems integrators because the semiconductor corporations generally do not produce automation equipment. This has resulted in U.S. vendor strengths and breadth of offerings, since equipment vendors have specialized in their efforts to supply the needs of the U.S. semiconductor industry. In fact, North American vendors such as Hewlett-Packard, Consilium, and I. P. Sharp (a Canadian company) are beginning to supply Japanese companies with factory-automation software. They are exploiting the niche of Japanese semiconductor companies that provide consumer products and, therefore, do not have the internal software expertise to develop their own software, in contrast to the computer producers that do.

In Japan, the automated semiconductor manufacturers are generally part of horizontally and vertically integrated megacorporations that provide a wide range of products other than semiconductors. As a result, systems integration of semiconductor production is often performed in-house, using company-built robots, AGVSs, computers, process equipment, and factory-automation software. Since the semiconductor companies have many resources, there are relatively few Japanese companies providing equipment, software, or systems integration. This is in direct contrast to the United States, where semiconductor companies have limited internal resources for automation compared with the Japanese. U.S. semiconductor companies rely on equipment suppliers and third-party vendors/integrators to meet their automation requirements.

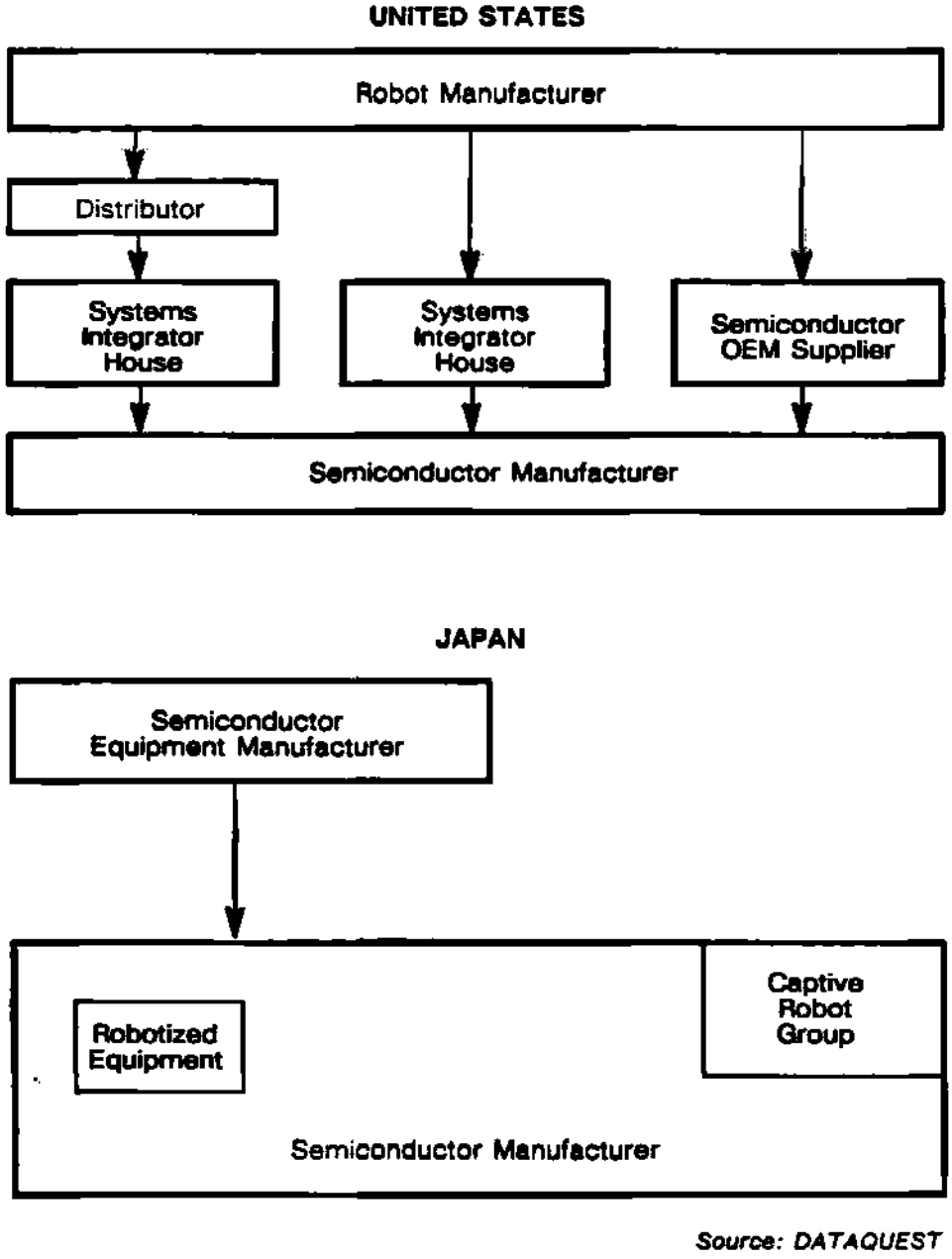
The differences in distribution channels have profound cost implications for installed systems. A company that provides all, or nearly all, equipment and systems integration in-house is able to keep costs to a minimum. A company that purchases robot-integrated process equipment from an OEM vendor is paying the profit margins on the individual pieces of equipment from various suppliers, plus the systems markup. For example, a robot is sold to an OEM for $40,000 to $60,000, which includes the vendor margin. It is combined with a wet bench costing $30,000 to $50,000, again including margin. With controls and software, the integrated product may sell for $125,000 to $155,000.

Figure 1 shows the different channels utilized to deliver robotic products to the semiconductor companies in the United States and in Japan.

Table 1 summarizes the following information for eleven major robot manufacturers in the United States currently supplying robots to the semiconductor industry: products, prices, distribution channels, and customers.

Figure 1

ROBOT DISTRIBUTION CHANNELS
UNITED STATES VERSUS JAPAN



Source: DATAQUEST

Table 1

ROBOTICS PRODUCTS, DISTRIBUTION, AND USERS IN THE SEMICONDUCTOR INDUSTRY

U.S. Robotics Vendors	Products	Approximate Price Range	OEMs/Systems Integrators (Non-inclusive)	Semiconductor Manufacturers (Non-inclusive)
Adept Technology	MegaOne Adept Vision	$40,000 $17,000	OEMs: Perkin-Elmer Systems integrators that handle electronics: Geiser Systems, UAS Automation Systems, Wee-Tech Automation Systems, Western Technologies	Confidential
American Robot	Modified Merlin Series: MR-6240, MR-6540, MR-6260	Base price: $65,000	Dynamac subsidiary: systems house with focus on electronics industry Daikin licensee: Japanese market	Currently in labs, not yet in production
GCA Corporation	XR-6050 Gantry; Factory control systems	Varies with system	Currently negotiating with OEMs; GCA does own systems integration using GCA or other robots, GCA semiconductor equipment	International CMOS Technology; GCA IC Systems Group (corporate division); others confidential
GMF Robotics	E-101, E-201 E-301	$33,000 $40,000	OEMs not available	Confidential
Intelledex	605-S or 605-T (post or table) Intellevue 200 Computer Vision System	$48,000 $14,500	Flexible Manufacturing Systems, FMI, CVC Products	National Semiconductor, Delco Electronics
Microbot	Alpha II WaferMover System	$14,000 $16,200	Machine Technology, Inc., Balteau, Optoscan	Texas Instruments (Texas, W. Germany), Harris Semiconductor, IBM, Motorola, Xerox
Panasonic	Pana Robo Clean Room Robot V-1C	$65,000	Bagaard Engineering, Noel J. Brown, Automation Tooling Systems	Confidential
Precision Robots, Inc.	PRI-1000 (wafers) PRI-2000 (cassettes)	$30,000 to $60,000 systems	Materials Research Corp., Tetron, Santa Clara Plastics, BTU	National Semiconductor, Intel (worldwide), SGS (Italy)
Seiko Instruments USA	RT-3000 RT-2000 XY-3000 XY-2000	$32,850 $34,000 $33,850 $32,850	Automation Tooling Systems, Datum Industries, Dick Schuff & Co., Intelmatec Corp.	GTE, Intel, Motorola, Northern Telecom, RCA-Sharp, Sperry, Westinghouse
Unimation	Clean Room PUMA 560 w/VAL-Plus control sys. w/VAL-II control system	$48,000 $53,000	VEECO (PUMA integrated on Automated Guided Vehicle System); negotiating with OEMs; also use systems integrators, distributors, direct sales force	Confidential
United States Robots	Maker 110	$45,000	OEMs: Semifab; Poly-Flow; WBS, Inc.; Systems Integrators: Penrep Ltd., Durham Technology Group, Contamination Control and Devices	Harris Communications, Intel, Mostek, Motorola, Texas Instruments (Texas)

Source: DATAQUEST

CLEAN ROOM REQUIREMENTS AND CERTIFICATION FOR ROBOTS

Clean Room Requirements for Robots

Of the 60 U.S.-based robot manufacturers, only a handful are focusing on clean room robots, with the majority of robots entering the market between 1984 and 1985. By definition, robots are multifunctional, reprogrammable devices able to perform a variety of tasks. Therefore, robots used in semiconductor applications are largely standard robots modified to meet clean room requirements. They are capable of performing other tasks, however, particularly material handling in the electronics industry. Some have required a year or more of redesign and structural modification to achieve clean room standards. They nevertheless remain general-purpose robots rather than special-purpose designs limited to use in semiconductor applications.

The following are possible steps in modifying a robot to achieve the required clean room specifications:

- Rotary joints are enclosed with ferrofluid seals to prevent particles from escaping from the moving parts.
- External surfaces are made of nonshedding bare metal or painted with a nonflaking paint, epoxy, or polyurethane.
- Lubricants are not exposed or have a very low vapor pressure.
- Motors are brushless to minimize particulate generation.
- Negative-pressure air is pulled through the inside of the robot, or bellows surrounding the robot, and filtered as exhausted.
- A clean suit of fray-resistant material is tailored to the robot.
- End effectors are designed using contaminant-free material, such as stainless steel.

In most of the front-end operations, robots are not required to have high speeds but to move smoothly to avoid generating particles or breakage from water movement inside the cassettes. The trend is toward higher communications capability to integrate a robot into an automated factory control system. Robots interface with material feeders, processing equipment, safety controls, and host computer systems for complete process tracking and control. The communications and integration needs, as well as the complexity of some tasks requiring decision making by the robot, mean that it must be programmed in a high-level language. High robot uptime and mean time between failure (MTBF) are important to keep humans out of the fab as much as possible.

Back-end operations need more speed and precision for assembly and test applications. Cleanliness is less stringent, and robots used in other electronics industry applications are often used.

Clean Room Certification

U.S. government guidelines specify the standards for Class 100 clean room environments. The stricter Class 10 and Class 1 environments are de facto standards currently specified and recognized by the semiconductor industry, but they are not as yet (and may not become) official government standards. Some robot manufacturers do not claim class certification beyond Class 100, but prefer to publish the results of testing by third parties. Testing is performed by four major means:

- Robot vendors use an internal clean room where systems are developed and tested prior to delivery to customers.
- Process equipment suppliers, OEM vendors, or systems integrators integrate the robots with their equipment and then sell custom automation solutions to customers.
- Independent engineering firms or semiconductor consultants, such as Dryden Engineering or the Institute for Microcontamination Control, perform the testing.
- Semiconductor manufacturers, the users of the equipment, certify the systems in their own environment; this includes robot supplier corporations that test their automation products in semiconductor divisions within the corporation.

All systems eventually have to meet standards within each installation, where the unique layout of equipment influences air flow and particulate control and where human traffic affects the level of cleanliness that can be achieved overall.

ROBOT VENDORS--THEIR PRODUCTS, PRICES, AND APPLICATIONS

Table 2 gives a brief description of leading robotic products, features, and specialization. For further detail, a list of the robot manufacturers, OEMs, and systems integrators is presented in Appendix A at the end of this newsletter.

Several additional vendors offer mobile transport vehicles or wafer transport systems.

Flexible Manufacturing Systems has introduced a computer-integrated manufacturing system that has navigation, equipment docking, and robotic-arm transfer capabilities. The system components are: a mobile robotic vehicle for materials transfer and transport; an intelligent work-in-process station that provides local storage of cassettes and wafers; a workstation interface that includes a docking module and operator interface; a computer system with communications network, including SECS (Semiconductor Equipment Communications Standards) link; and software for monitoring and control.

Table 2

PRODUCT/APPLICATION CHART:
ROBOT VENDORS

Company	Products/Applications	Advantages Stated*	Comments
Adept Technology	AdeptOne assembly robot used predominantly in back-end assembly and test. SCARA (assembly) configuration, 13-lb. payload, 32-in. reach. Sample applications: component testing of SIPs, DIPs; load/unload wire bonder; palletize components of molding machines; test station conveyor tending; lead frame alignment in ceramic chip assembly; load/unload lead frame equipment. 10-20 back-end installations; fab applications confidential.	Speed, precision. Looking at applications requiring these characteristics. Uses sophisticated control system, VAL-II, with process control capability.	Currently in early stages of supplying semiconductor industry. Evaluating needs to develop solutions.
American Robot	Turnkey systems integration. 6-axis articulated-arm robots. Models: MR-6240, MR-6260, MR-6540 have work envelopes ranging 40 in.-60 in., payload 20-50 lbs. Targeted to handle heavy quartz boats and large wafers. Equipment targeted: Diffusion furnace and other equipment load/unload; conveyor unload; DIP handler in test area. Work cell approach: Clean Wafer Cassette Handling work cell includes robot system, controller, linear conveyor, to link with wafer processing equipment. Some confidential installation in R&D laboratories.	Heavier payload and extended-reach capabilities. High level communication with host computer system; S&CS-II. Subsidiary Dynamac Inc. emphasizes design of complete automated factories for electronics industry.	New products to reach market in early 1986 for light assembly and material handling; applicable to back-end assembly and test.
GCA Corporation	Turnkey systems integration. XR-Series gantry robots modified for clean room; XR-6050 has 50-lb. payload. Emphasis on total CIM. Performs analysis; designs factory control system; then provides total system of robots, hardware, and software. CIMcell product skips hierarchy channels to communicate directly to host computer. All systems designed to order, not off the shelf. Can upgrade semiconductor equipment to communicate on factory level; GCA systems communicate with process equipment from any vendor. Teleoperation technology provides human control of robots to perform nonstandard, unprogrammed work--such as equipment repair--without human entry into clean room. Installations include several large contracts for whole factory automation.	GCA is leading producer of stepper equipment. In-house experience base with GCA IC Systems Group, which tests and uses the automated systems. Emphasis on factory control and communication.	Clean room material handling system debuted at Semicon West in May, 1985.

(Continued)

Table 2 (Continued)

PRODUCT/APPLICATION CHART: ROBOT VENDORS

Company	Products/Applications	Advantages Stated*	Comments
GMF Robotics	Turnkey systems integration. E-301 is a Class 10 robot, approaching Class 1, uses patented design sealed linear joints. Three to five axes, with a 33-lb. payload in a 3-axis configuration. E-101 and E-201 offer different envelope sizes, are Class 100, and can convert to Class 10. Targeted to handle wafers and cassettes. Twelve installations.	Provides systems or units. Develops and tests systems in an in-house clean room. SECS-II	GMF is just entering clean room market with first product demonstration at Robots 9, June 1985. E-301 will be available on production floor in December 1985. Within GMF Electronics Business Segment, half of efforts are devoted to robots for clean room use.
Intelledex	Turnkey systems integration. Articulated, 6-axis Model 605 can be post, table, or track mounted. Sealed rotary joint, tactile sensors. Applications: predominantly cassette, also wafer handling; lead frame loading. Developed wet chemical processing system for 6 in. wafers in cooperation with Flourocarbon, which makes wafer cleaning systems and particulate detection equipment. Offers 7 systems where robot on track operates Megasonic Cleaning Systems and Superclean 1600 Rinser/Dryers in Class 10 room. System oversees recipe selection; monitors fluid levels, temperatures, and timing decisions. IntelleVue 200 Computer Vision System: aligns wafers for probing by test equipment; process control--assures ink jet defect marker functions and reads characters for part tracking.	Emphasizes smooth motions to avoid contact contamination. High-level communications ability for interface with sensors, process equipment, and process tracking and control. SECS-II, IEEE-488.	Company specialization in 2 markets: semiconductor manufacturing and electronic industry. Starting distribution in Europe.
Microbot	WaferMover: turnkey, standardized systems for wafer handling. Consists of Alpha II robot with 5-axis articulated arm, various vacuum pickups to allow handling of different size wafers, microcomputer control, peripheral equipment. Alpha II system is Class 1. Optional accessory Robot Clean Suit tested to more stringent level of Class 1. Applications: Automates transfers into and out of coater, developer, and aligner; picks wafers out of cassettes, sorts, and takes to inspection systems, then refiles into cassettes. Communicates between equipment.	Pre-engineered package solutions allow faster installation, less risk to user due to proven technology. Two-year use history in fabs. Reliability: 4,500+ hours MTBF; 500 hour stress test at 130 degrees F for whole system	Lowest-cost robot systems available on market.

(Continued)

8+ 163

Table 2 (Continued)

PRODUCT/APPLICATION CHART: ROBOT VENDORS

Company	Products/Applications	Advantages Stated*	Comments
Panasonic	Pana Robo V-IC Clean Room Robot, 6-axis articulated arm with 11-lb. payload; Class 10. Applications in wafer fab and wafer coating processes. Robot transfers wafers between cleaning baths; loads/unloads sputtering equipment. Installations: Nearly 25 in the U.S. since June 6, 1985 announcement to provide robots for semiconductor industry.	High precision, smooth motion to avoid contact contamination, high speed (80 in./second). Clean room testing performed by independent labs and by in-house tests in Japan and in U.S.	Panasonic Industrial Company is a division of Matsushita Electric Corporation of America, which has extensive experience base in electronics, notably in Japan.
Precision Robots, Inc.	Turnkey systems integration. PRI-1000 and PRI-2000 series used for handling wafers, cassettes, wafers mounted to film frames, quartz boats. Articulated arm with up to 6 axes, 10-lb. payload (higher available). Tactile sensor, vacuum pickup. Application in 5 major areas: sputtering, CVD, diffusion, epitaxy, wet chemical processing. Class 10. Nonvolatile computer memory system used to maintain lot identities, communicates with central computer. More than 50 installations to semiconductor manufacturers worldwide.	Reliability, high (98 percent) up-time; MTBF over 1,000 hours. Unique arm structure and mechanical linkage allows precise, smooth linear motion for moving wafers in and out of boats.	Internationally marketed, installations in Japan and Europe. Supplies products to electronics industry, with more than 80 percent of focus on clean rooms.
Seiko	Primary model used is RT-3000 modified for clean room, including negative air pressure system. Also smaller RT-2000. Both cylindrical-coordinate, 4-axis, with payloads of 5.5 to 11 lbs. Two Cartesian models, XY-2000 and XY-3000, featuring high accuracy and repeatability levels. Applications: lead frame handling--robot picks lead frames from cassette, palletizes them for die bonding. Other uses in die/wire bonding area. Turnkey systems available through large network of distributors.	XY-series are accurate to .0008 inch and repeatable to .0002 inch, and can be downloaded directly from host computer. Seiko has extensive experience base in electronics industry.	Developing new clean room products cooperatively with users. Anticipate product announcements in near future.
Unimation	Turnkey systems integration Clean Room PUMA 560, a 6-axis articulated arm with significant internal changes and parts built for low particle emission: negative air pressure, sealed motors, particulate exhaust air filter. Major OEM contract with VEECO Integrated Automation, Inc., which integrates PUMA arm on top of mobile Automated Guided Vehicle System (AGVS). Applications: wafer or cassette equipment handling; furnace, other loading. Several proprietary applications.	High level control and factory integration capability; uses sophisticated controller--VAL-II; SECS-II. Clean room compatibility tested by VEECO in Class 10 room. Unimation publishes the test results.	Internationally marketed. Entered clean room market at beginning of 1985. Anticipate new product announcements toward end of 1985.

(Continued)

Table 2 (Continued)

PRODUCT/APPLICATION CHART:
ROBOT VENDORS

Company	Products/Applications	Advantages Stated*	Comments
United States Robots	Turnkey systems integration. Maker 110 is a spherical-coordinate, 5-axis robot designed for clean room; payload more than 5 lbs. Class 10. Control/communications, work process tracking ability using SECS-II and ASCII interface for monitoring/control by PC, mini, or mainframe. Used almost exclusively for semiconductor industry. Applications emphasize work cell approach: wet bench work cell, dry etch, furnace and rinser/dryer loading. Current focus is work cells, working on full factory systems automation. 30-40 installations after 1 year in the market.	Passed clean room testing and certification by Texas Instruments, Dallas. Targets two major markets: semiconductor front end is 65-70 percent of company focus; electronics industry material handling 30-35 percent.	Internationally marketed. Intends to provide capability to automate all front-end processes.

*All Companies stated that their products meet stringent cleanliness standards; therefore, cleanliness will be assumed for all companies although not listed.

Source: Company Literature
DATAQUEST

Veeco Integrated Automation, Inc., has a Robotic Wafer Fabrication Automation System that uses an automated guided vehicle equipped with a robotic arm to transport wafers from station to station. The system consists of the vehicle, WIP station, and central control computer. The robot arm inserts and removes loaded cassettes from production equipment, stores wafers, and controls wafer inventories. It communicates with the central computer (MICROVAX) via an IR link.

Nacom offers the Namtrak Wafer Cassette Transporter, which includes elevators with load/unload stations and an interlocking track to transport wafers in a clean environment. A pneumatically controlled transfer mechanism loads and unloads cassettes from the transfer tunnel. The tunnel is an enclosed Class 10 environment that allows wafers to be transported between processing equipment and clean rooms. An optional elevator system allows wafers to be moved at ceiling level, thus allowing maximum floor space utilization.

Additional companies that provide this type of conveyor/track equipment system for moving cassettes include: Programmation, Shuttleworth Systems, and Translogic.

MARKET OPPORTUNITIES AND DIRECTIONS FOR DEVELOPMENT

The current state of automation in the United States is work cell automation--or islands of automation--where a robot is combined with a process machine, fixturing, and a controller that oversees the activities of that particular process. The next level of opportunity involves linking together the individual islands so that entire production lines run without human operators. This includes the transfer of wafers within and between processes and control by a central computer system. Recent development efforts and new products focus on mobile equipment that services multiple machines and locations to maximize the use of the equipment.

Specific robot directions for development may include machine assisting: correcting minor malfunctions and jamming, alcohol wipedown and equipment cleaning, and routine maintenance. In addition to targeting these operations for robots, GCA Corporation offers teleoperation equipment originally developed for use in the nuclear industry. It allows a human operator outside the clean room to manipulate robotic equipment with manual control, while receiving sensory feedback as if operating the equipment directly. This method can be used to perform a nonstandard assist or repair without entering the clean environment or shutting down a process.

DATAQUEST ANALYSIS

The semiconductor industry is a very new area for robotics penetration, and Japan is ahead of the United States in adopting robots. The use of robotics in the U.S. semiconductor industry is in its embryonic stages. In the United States, there are no fully automated facilities. Rather, U.S. manufacturers have taken the approach of automating the work cell area first; then they will connect the various work cells together in a fully automated factory. The robots that are in use today in U.S. fabs are being used in the work cell areas of wet benches, photolithography, diffusion, and ion implantation, but even in these areas the use of robotics is limited. It is likely that the majority of currently installed robots are being investigated in R&D laboratories, where the semiconductor manufacturers test and evaluate new methods and equipment prior to using them in production.

The whole semiconductor industry takes a different approach from other industries to justification of robots. While cost is important, DATAQUEST believes it to be second in emphasis to yield improvement, reduced cycle time, and process control. The purpose of reducing the human work force is not only to save labor costs, but primarily to improve cleanliness of the environment and therefore increase product yields. Higher product yields result in lower IC product costs, which are required for a semiconductor manufacturer to remain competitive in the world market.

U.S. semiconductor manufacturers are just starting up the learning curve of adopting advanced manufacturing technology. The companies that act quickly to fully automate their factories will realize significant competitive gains. DATAQUEST sees the U.S. robot vendors responding appropriately to meet the needs of the semiconductor industry. They are making the effort to work closely with semiconductor manufacturers and OEM equipment suppliers to develop products best suited for use in the fabs. The robot vendors are positioning themselves to supply the domestic market and also to seize opportunities overseas where certain market segments lack competitive products. However, it is not up to the robot vendors to drive the market. That responsibility lies with the semiconductor manufacturers, who must fully automate their factories or lose their competitive position in the world market.

(This newsletter is reprinted with the permission of DATAQUEST's Robotics Industry Service.)

Joseph Grenier
Melinda S. Pyle

Appendix A

Robot Manufacturers

The following companies can provide further infomation and specific product details:

Adept Technology
1212 Bordeaux Drive
Sunnyvale, CA 94089
(408) 747-0111

American Robot Corporation
121 Industry Drive
Pittsburgh, PA 15275
(412) 787-3000

GCA Corporation
Industrial Systems Group
One Energy Center
Naperville, IL 60566
(312) 369-2110

GMF Robotics
5600 New King Street
Troy, MI 48098-2696
(313) 641-4201

Intelledex
4575 S. W. Research Way
Corvallis, OR 97333-1098
(503) 758-4700

Microbot
453-H Ravendale Drive
Mountain View, CA 94043
(415) 968-8911

Panasonic Industrial Company
Industrial Equipment Division
One Panasonic Way
Secaucus, NJ 07094
(201) 392-4979

Precision Robots, Inc.
6 Cummings Park
Woburn, MA 01801
(617) 938-1338

Seiko Instruments USA
Robotics/Automation Division
2990 W. Lomita Blvd.
Torrance, CA 90505
(213) 530-8777

Unimation Incorporated
Shelter Rock Lane
Danbury, CT 06810
(203) 796-1188

United States Robots
650 Park Avenue
King of Prussia, PA 19406
(215) 768-9210

Appendix B

Systems Integrators and OEM Equipment Suppliers

The following companies can provide further information on integration of robot systems, as well as specific product details:

Systems Integrators/ OEM Equipment Suppliers	Robot Manufacturers Represented (Non-Inclusive)
Mr. Joe Nava Vice President, Marketing Flexible Manufacturing Systems, Inc. 16780 Lark Avenue Los Gatos, CA 95030-2315 (408) 395-2777	Intelledex
Mr. Rick Heim, Vice President Machine Technology, Inc. 641 River Oaks Parkway San Jose, CA 95134 (408) 942-0800	Microbot
Solitec, Inc. 1715 Wyatt Drive Santa Clara, CA 95054 (408) 980-1355	Microbot
Optoscan Corporation 1250 Charleston Road Mountain View, CA 94043 (415) 961-9451	Microbot
Mr. Roger Awad, Marketing Manager Automation Tooling Systems (ATS) 101 Trillium Drive Kitchener, Ontario CANADA N2E 1W8 (519) 893-7541	Panasonic, Seiko
Mr. Bill Reiersgaard Bagaard Automation 725 S. E. Lincoln Portland, OR 97214 (503) 233-8246	Panasonic, Seiko
Mr. Bill Salvesen, President Datum Industries, Inc. 15 Grand Avenue Palisades Park, NJ 07650 (201) 943-8870	Seiko

Systems Integrators/ OEM Equipment Suppliers	Robot Manufacturers Represented (Non-Inclusive)
Mr. Dick Schuff, President Dick Schuff & Company 2432 W. Peoria Avenue, Suite 1076 Phoenix, AZ 85029 (602) 997-0206	Seiko
Mr. Minoru (Red) Akagawa, President Intelmatec Corporation 28300 Industrial Blvd., Unit H Hayward, CA 94545 (415) 887-8703	Seiko
Mr. Eric Waeldchen, Manager Keller Technology Corporation 2320 Military Road Tonawanda, NY 14150 (716) 693-3840	Seiko
WES, Inc. P.O. Box 800 Brandywine Court Lafayette, NJ 07848 (201) 579-1998	United States Robots
Contamination Control & Devices, Inc. 510 Market Loop West Dundee, IL 60118 (312) 428-5105	United States Robots
Penrep Limited 790 Lucerne Drive Sunnyvale, CA 94086 (408) 733-7176	United States Robots
Durham Technology Group, Inc. 2300 Cypress Point East Austin, TX 78746 (512) 328-0402	United States Robots
Semifab, Inc. 307 Fallon Road Hollister, CA 95023 (408) 637-8101	United States Robots
Veeco Integrated Automation, Inc. 10355 Brockwood Road Dallas, TX 75238 (214) 349-8482	Unimation

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: 1985-1986 Newsletters: December

THE POSSIBILITIES FOR ECONOMIC GROWTH IN 1986

Business Week recently held a panel discussion at the San Francisco Commonwealth Club. The discussion was titled "1986 Business and Economic Outlook; The Editor's Perspective." Members of the panel were: John A. Dierdoff, Managing Editor, Moderator; Ronald Grover, Congressional Correspondent; William Franklin, Business Outlook Editor; David Wallace, Money and Banking Editor; and William Wolman, Editor Overseeing Economic and Financial Coverage.

The panelists agreed that, although large problems must be overcome, it is possible to maintain economic growth through 1986. However, if these problems are not dealt with, there could be a recession as early as mid-1986.

TROUBLES OF AN AGING EXPANSION

Mr. Franklin pointed out that economic expansions usually last 33 to 34 months--and the present expansion is in its third year. Consumer spending, fed by consumer borrowing, is one of the main supports of the expansion. If consumers become worried about their high debt levels, they might cut their spending back after Christmas. Should this happen, the panelists did not see any other sector that could replace the consumer sector.

Capital spending in particular worried the panelists. Capital spending plans are down 1 percent in 1986 from 1985. Mr. Franklin observed that this is the first time that capital spending plans have decreased in a non-recession year.

Not only will capital spending by U.S. firms probably be down in 1986, the U.S. capital goods industry will continue to face stiff competition from overseas. Thus, much of the capital spending that does occur will fuel overseas economies rather than the U.S. economy.

IS A SERVICE-ONLY ECONOMY HEALTHY?

The manufacturing sector continues to be relatively weak. Concern was expressed about this weakness, particularly in conjunction with the continuing shift in the U.S. economy from a manufacturing to a service orientation. Approximately one-half million manufacturing jobs were lost in the past year while more than 3 million jobs were created in the service sector. Panelists observed that manufacturing jobs generally pay more than service jobs and, more importantly, that the health of the service economy depends on a healthy manufacturing sector to underwrite it.

TRADE, DEFICITS, AND POLITICS

The present situation could be best described as gridlock. To balance the budget, there has to be some combination of decreased expenditures and increased revenues. However, the Democrats do not want to touch entitlements, the Republicans are afraid to attack Social Security, and President Reagan wants growth in defense spending but will not agree to raise taxes.

This continued gridlock could lead to a Constitutional Convention to balance the budget. (Only two more states need to ratify a resolution for a convention to be called.)

The value of the dollar will continue to decrease in 1986, according to Mr. Franklin. However, this decline has to be steep in order to affect imports into the U.S. economy. Otherwise, non-U.S. competitors can meet the effects of a declining dollar by simply lowering their prices.

The panelists agreed that in order for the dollar to decline enough to affect imports, the problem of our continuing large federal budget deficits must be faced. Mr. Grover was not overly optimistic about the Graham-Rodman bill currently pending before Congress. This budget balancing bill would set progressively smaller target deficits over the next seven years. If in any one year these targets were not met, then the president would have to order across the board cuts (with certain mandated exceptions such as Social Security) to meet the mandated targets. Even if the House of Representatives and the Senate agree on the bill's form, Congress could always change its mind and rescind its provisions. The continued trade imbalance, Mr. Grover believes, could lead the president to take some protectionist action in 1986. Such a move worries Mr. Wolman, who believes that it could imperil the world economy.

A value-added tax was thought to be likely in 1986. According to Mr. Grover, a 10 percent tax of this sort would add $100 million in revenues. Besides increasing revenue, such a tax could be rebated for export sales and thereby help reduce the trade deficit.

ON THE BRIGHT SIDE

Mr. Wolman was the most optimistic of the panelists. He believes that the economy will grow in 1986. He said that interest rates are down and will stay down. If interest rates begin to rise in the United States, corporations can borrow from banks overseas, which are more highly leveraged than U.S. banks, and thus can offer funds at lower rates.

Mr. Wolman believes that the current bullish run on the stock market is also a good sign for 1986. Although he said that the stock market tends to predict five downturns for every one that actually happens, he believes that it is a fairly good indicator of an expansion.

Another positive sign for 1986 is that inflation is dead. All of the panelists agreed that OPEC will not be able to maintain its present price level in 1986. Mr. Franklin expects inflation in 1986 to be in the 2 to 3 percent range, and in 1987 through 1990, in the 6 to 9 percent range. It is very significant, Mr. Wallace observed, that, although there is an unemployment rate of 7 percent, there is no outcry from the public. Underlying this acceptance is a painfully formed consensus about the harmful effects of inflation on all aspects of our economic life--consumption, savings, investment, and planning. On this evaluation, all the panelists agreed.

DATAQUEST ANALYSIS

DATAQUEST has estimated that U.S. semiconductor consumption will increase 9.8 percent in 1986 followed by a 37.0 percent increase in 1987. This upturn requires that bookings continue the strong growth that they showed in September and October. We believe that semiconductor revenues will turn up in the first quarter of 1986 and that capital spending will turn up in the third quarter.

One concern that we have is the general economy. Although the semiconductor industry is fairly independent of the GNP in its business cycles (witness our industry decline in 1985), general business factors, especially as manifested in a recession, do have an effect. The business factors that concern us most are interest rates, inflation, dollar valuation, consumer debt, and the world economy. The Business Week panel discussion has helped allay some of our fears that a general recession would squelch our incipient semiconductor industry recovery. We believe that our estimates for semiconductor consumption will proceed on schedule.

George Burns
Robert McGeary

Dataquest
a company of The Dun & Bradstreet Corporation

RESEARCH NEWSLETTER

SEMS Code: 1985-1986 Newsletters: December

SEVENTH ANNUAL GaAs SYMPOSIUM
NOVEMBER 12-14, 1985

Interest in gallium arsenide (GaAs) ICs has grown rapidly in recent years. Attendance at the IEEE-sponsored GaAs IC symposium has grown more than 30 percent annually since 1982, reaching 850 at this year's meeting in Monterey, California. Abstract submittals increased 24 percent over 1984, indicating substantial growth in development activity.

HIGHLIGHTS

General

- Forty-nine papers, approximately evenly split among analog ICs, digital ICs, and technology topics
- Authors from 26 companies, 5 universities, and 2 other organizations
- Three panel discussions covering millimeter-wave ICs, LSI issues, foundry operations, and standardization

Key Papers

- A GaAs, 12-bit, 1-GHz digital-to-analog converter (DAC)--Hewlett-Packard Labs
- A 115-GHz, monolithic, GaAs, FET oscillator--Texas Instruments
- A 2.6ns, t_{aa}, 1K x 4 SRAM using enhancement/depletion MESFETs (two papers)--Hitachi
- An ECL-compatible, 1K SRAM (with smallest cell reported to date)--Texas Instruments

- A 400-MHz band prescaler (for hand-held radio)--Toshiba
- An 8 x 8 multiplier (5.6ns at 1.45V) with 20-bit accumulator--Sony
- A high-temperature (180 degrees C) GaAs Hall-effect sensor--Siemens

OBSERVATIONS AND CONCLUSIONS

GaAs IC technology is extending semiconductors to new frontiers of speed, speed/power efficiency, temperature extremes, and radiation resistance. Analog GaAs ICs are already commercially viable, with free-world market shipments exceeding $50 million annually.

However, present merchant market activities in GaAs digital ICs are severely limited by quality of starting material, threshold control, lack of test equipment for use in a production environment, chip interface/packaging standardization, and other restrictions. DATAQUEST believes that the 1985 GaAs digital IC market will be less than $15 million worldwide.

Explosive merchant market growth rates exceeding 100 percent a year for SRAMs, gate arrays, and other LSI devices are achievable as the restrictions mentioned above are resolved. At such time, demand will rapidly grow to more than $1 billion annually. The wafer-processing capacity required to support such a business level is quickly achievable, and the technical expertise is available, as demonstrated by this year's papers.

(This newsletter is reprinted with the permission of DATAQUEST's Japanese Semiconductor Industry Service.)

Peggy Wood
Gene Miles