Semiconductor Equipment and Materials Service Equipment and Materials

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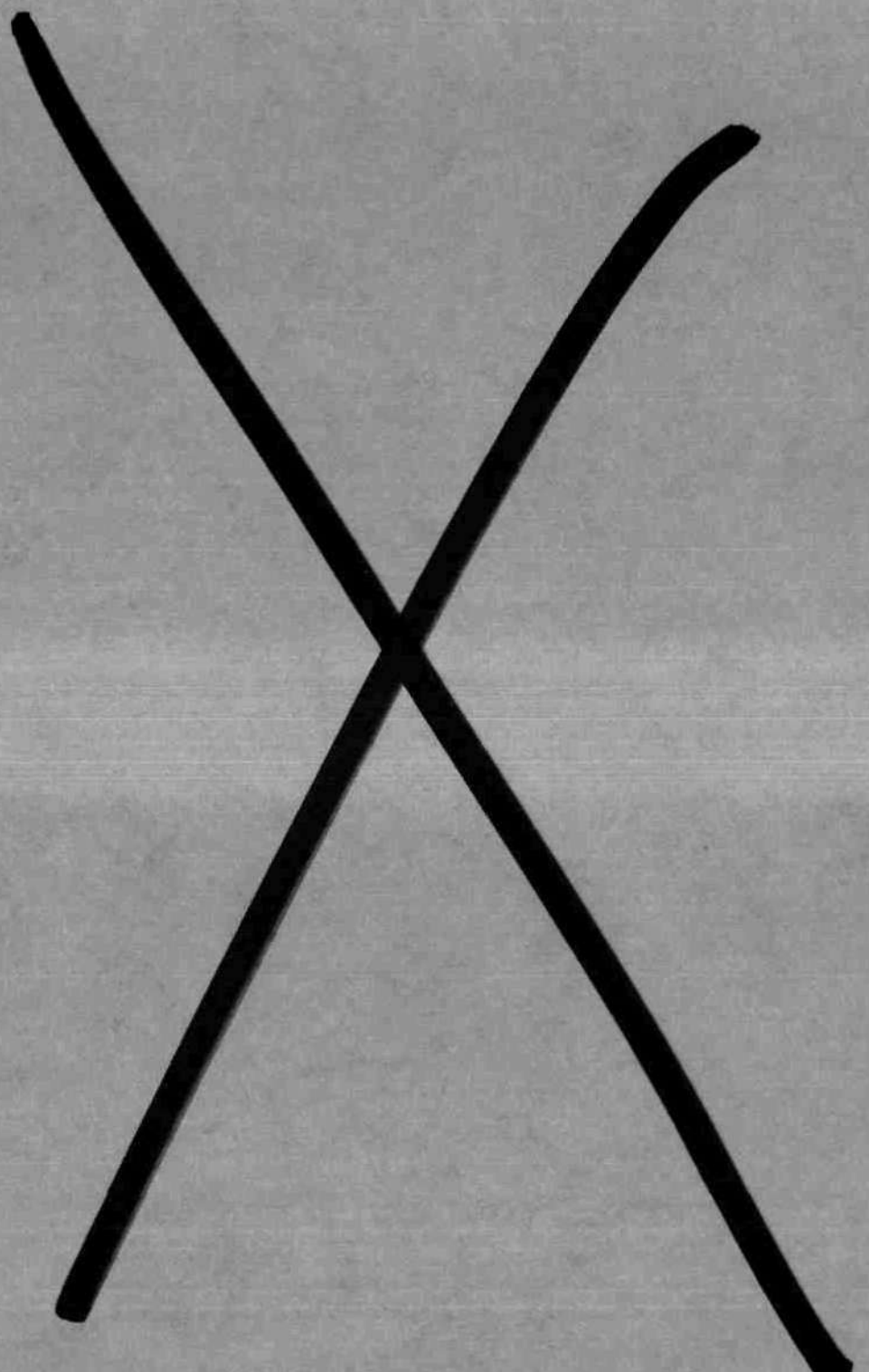

Introduction to the Service

The Semiconductor Equipment and Materials Service (SEMS) is a comprehensive, worldwide information service that documents and analyzes important aspects of the Semiconductor Equipment and Materials Industry. The service consists of:

- Two 3-inch, loose-leaf binders containing reference data base material that is continually revised and updated as developments occur or additional information becomes available
- Newsletters providing executive summaries of key industry events or significant changes in the reference material from the other binders; a newsletter binder is provided for storing this material
- Inquiry privileges for two individuals at each subscribing company; this service provides an open line to the research staff for amplification of data base and newsletter information
- An annual three-day conference with industry experts discussing developments of current interest and importance

The service analyzes and reports on the equipment and materials used in the production of semiconductors and assesses the effects of rapid industry growth, frequent and rapid industry fluctuations, technological complexity, technological innovations, short product cycles, and fierce competition. To answer questions on the industry, the service will:

- Discuss current and emerging technologies and trends, including historical and forecast market data, and market shares for each major type of equipment and materials
- Provide profiles of worldwide equipment and materials companies and company financial reports
- Provide a complete picture of the semiconductor industry including its problems and trends as well as locations of semiconductor facilities and the technologies produced at these locations
- Present current, forecast, and historical capital spending by the worldwide semiconductor industry, analyzed by company
- Provide analyses of industry wafer fabrication capacity and its effect on both the semiconductor companies and the equipment and materials companies including actual wafer starts, excess capacity, and forecasts of capacity utilization
- Present worldwide semiconductor production, revenue/square inch of silicon, and other key ratios for the semiconductor and the equipment and materials industry

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Introduction to the Service

NEED FOR THE SERVICE

The semiconductor equipment and materials industry is characterized by technological complexity, a proliferation of market opportunities, intense competition, and shorter product life cycles. Since this is a rapidly changing environment, it is of crucial importance to many firms to keep abreast of the technological changes and to assess their impact, both on the semiconductor industry and on the equipment and materials industry. No other organization maintains complete or even near-complete statistics on capital spending, capacity, and key semiconductor ratios. This information will be vital input for strategic corporate decisions in both the semiconductor and the equipment and materials companies. Dataquest's aim is to help remove the uncertainty surrounding major capital spending decisions and to give decision makers the tools to make more confident decisions. The Semiconductor Equipment and Materials Service aims to provide this type of data through continuous industry coverage, and careful assemblage and assessment of observed trends.

The service is staffed with veteran industry analysts who maintain continuous contact with key trendsetters in the industry, including industry executives, marketing and engineering managers, start-up firms, and individual technologists who are recognized for their contributions to past technical symposiums. The inquiry privilege provides a means for clients to gain access to the thinking of service analysts while new trends are still developing. Often these trends become apparent before a significant body of market data is available for publication.

We believe that the Semiconductor Equipment and Materials Service offers our clients an excellent tool with which to make solid and confident business decisions. We maintain every possible effort to fulfill our commitment to the semiconductor and related electronic industries through publication of information--in a convenient format--collected during Dataquest's continuous worldwide industry coverage.

SERVICE STRUCTURE AND TERMINOLOGY

The service is divided into two data base reference volumes plus one newsletter volume, as follows:

- Markets and Technology
- Industry Econometrics
- Newsletters and Bulletins

Introduction to the Service

Whenever a section of a data base reference volume is updated, a newsletter is issued summarizing significant changes since the last update. Additional newsletters may be generated from time to time on significant industry events. Portions of these newsletters may be incorporated in the data base volume when the appropriate section is next updated.

The Markets and Technology volume covers semiconductor equipment and materials markets in detail. Currently, coverage is/will be provided on:

- Manufacturing operations
- Maskmaking
- Semiconductor manufacturing automation
- Wafer fabrication equipment
- Wafer fabrication materials
- Equipment data base
- Market share data
- Packaging and materials
- Technology trends

The Industry Econometrics volume covers productivity trends in semiconductor manufacturing and profiles semiconductor equipment and materials companies. Coverage is/will be provided on:

- Companies (with alphabetical tabs)
- Financial aggregates
- Capital spending
- Manufacturing capacity
- Semiconductor manufacturing
- Semiconductor industry ratios
- Economic outlook

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Introduction to the Service

SERVICE ORGANIZATION AND CODING

To minimize difficulties in updating and referencing information, Dataquest has developed a flexible organizational hierarchy and associated coding for the individual components that make up the entire set of binders. This scheme is used to allow the organization of the notebooks to be changed as markets change.

Each data base notebook is organized into a set of subject tabs. A list of these tabs is provided at the front of each notebook. A service section within each tabbed section can be recognized by the title, and each section has its pages numbered consecutively, starting with page one. A list of publications within each tabbed section is filed immediately behind each tab.

The newsletter notebook has monthly tabs, a list of the publications behind each tab, and a cross-reference index.

SERVICE FEATURES AND PROCEDURES

Because of the large quantity of printed information that will be available for insertion, the binders are a multivolume set. The volume name appears on the spine of each volume. Section tabs are included for easy reference, with new ones added as new material is added to the notebook.

The date of preparation is noted on the bottom of each page. When there are major revisions, entire sections or subsections are updated. Each new version replaces the earlier one in its entirety, and is added to the book, behind the appropriate tab. A new list of publications is provided whenever a new publication is added behind the tab.

Newsletters take two forms--reports and analyses. Newsletters that contain information of a general reporting nature, such as trade show reviews, meeting summaries, mergers, and shifts of personnel, are intended for current news and will be utilized in later analyses and updates of sections and subsections. Newsletters are always filed chronologically in the newsletter notebook.

The inquiry privilege permits subscribers to contact Dataquest by mail, telegram, telephone, telex, or in person to ask for copies of printed material, data, or options on topics covered by the service. With the exception of confidential or proprietary material, Dataquest's complete files on the semiconductor industry--as well as its entire staff of electronics specialists--are available to subscribers.

Introduction to the Service

Our annual three-day conference covers topics of timely interest and importance. Programs include outside speakers, panel discussions, and demonstrations. Participants have the opportunity to mingle with skilled industry specialists.

Because we wish the service to be responsive to industry needs, we welcome suggestions for changes. We will periodically poll all subscribers to determine the topics that should be given priority, or new ones that should be added.

SERVICE STAFF

Frederick L. Zieber

Mr. Zieber is Executive Vice President of Dataquest and General Manager of Technology Operations. Technology Operations includes all syndicated industry services, consulting activities, and electronic industries information research. Previously, he was General Manager and founder of Dataquest's Semiconductor Division. Mr. Zieber has 14 years of experience in market research and consulting. Prior to that, he worked in the semiconductor industry for 9 years. He has experience in processing, designing, manufacturing, and testing integrated circuits and discrete devices. He holds two patents in semiconductor processing. Mr. Zieber has a B.S. degree in Electrical Engineering from Stanford University and an M.B.A. degree from the Graduate School of Business at Stanford University.

Gene Norrett

Mr. Norrett is a Vice President of Dataquest and Director of its Semiconductor Industry Group (SIG). In this capacity, he has direct responsibility for all U.S. research and coordinates European and Japan-based research. Prior to becoming SIG Director, he founded Dataquest's Japanese Semiconductor Industry Service and was Acting Managing Director of Dataquest Japan K.K. Before joining Dataquest, Mr. Norrett spent 14 years with the Motorola Semiconductor Product Sector, serving in various marketing and management positions. He has traveled extensively in Japan, Hong Kong, Taiwan, Korea, China, and Europe. Mr. Norrett's educational background includes a B.A. degree in Mathematics from Temple University and an M.S. degree in Applied Statistics from Villanova University. He has also taken graduate courses in Marketing from Arizona State University.

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Robert E. McGeary

Mr. McGeary is the Director of Dataquest's Semiconductor Equipment and Materials Service. Prior to joining Dataquest, he was Product Marketing Manager at Applied Materials, Inc., where he managed the worldwide product marketing activities for the Dry Etch Division and managed product support for the company's European dry etch business. Previously, he worked as Product Marketing Manager at GCA Corporation's IC Systems group, as an Accelerator Physicist at Lawrence Berkeley Laboratories, as a Nuclear Engineer at Mare Island Naval Shipyard, and as a Reactor Operator at the University of Washington. Mr. McGeary received a B.S. degree in Physics and Mathematics from the University of Washington and an M.B.A. degree from St. Mary's College.

Joseph Grenier

Mr. Grenier is a Senior Industry Analyst for Dataquest's Semiconductor Equipment and Materials Service. He is responsible for analyzing the market environment and future technology trends. Prior to joining Dataquest, he was Product Marketing Manager at GCA Corporation, where he was responsible for the reactive ion etch program. He also served as International Marketing Manager at GCA, and was responsible for the overseas marketing of wafer processing equipment. Previously, he worked as a Product Manager at Varian Associates' Instrument Division, as a Systems Engineer at the USAF Satellite Test Center, and as a Test Engineer at General Motors' Noise and Vibration Laboratory. Mr. Grenier received a B.S.E.E. degree from the University of Detroit and an M.B.A. degree from the University of Santa Clara.

George Burns

Mr. Burns is an Industry Analyst for Dataquest's Semiconductor Equipment and Materials Service. He is responsible for the service's Econometrics notebook. Before joining Dataquest, he worked at Plantronics/Santa Cruz, where he was a Product Marketing Analyst and a Product Manager. Among his responsibilities were new product definition, new product introductions, and forecasting. Mr. Burns received a B.A. degree in Economics from the University of California at Santa Cruz and an M.B.A. degree in Marketing from San Jose State University.

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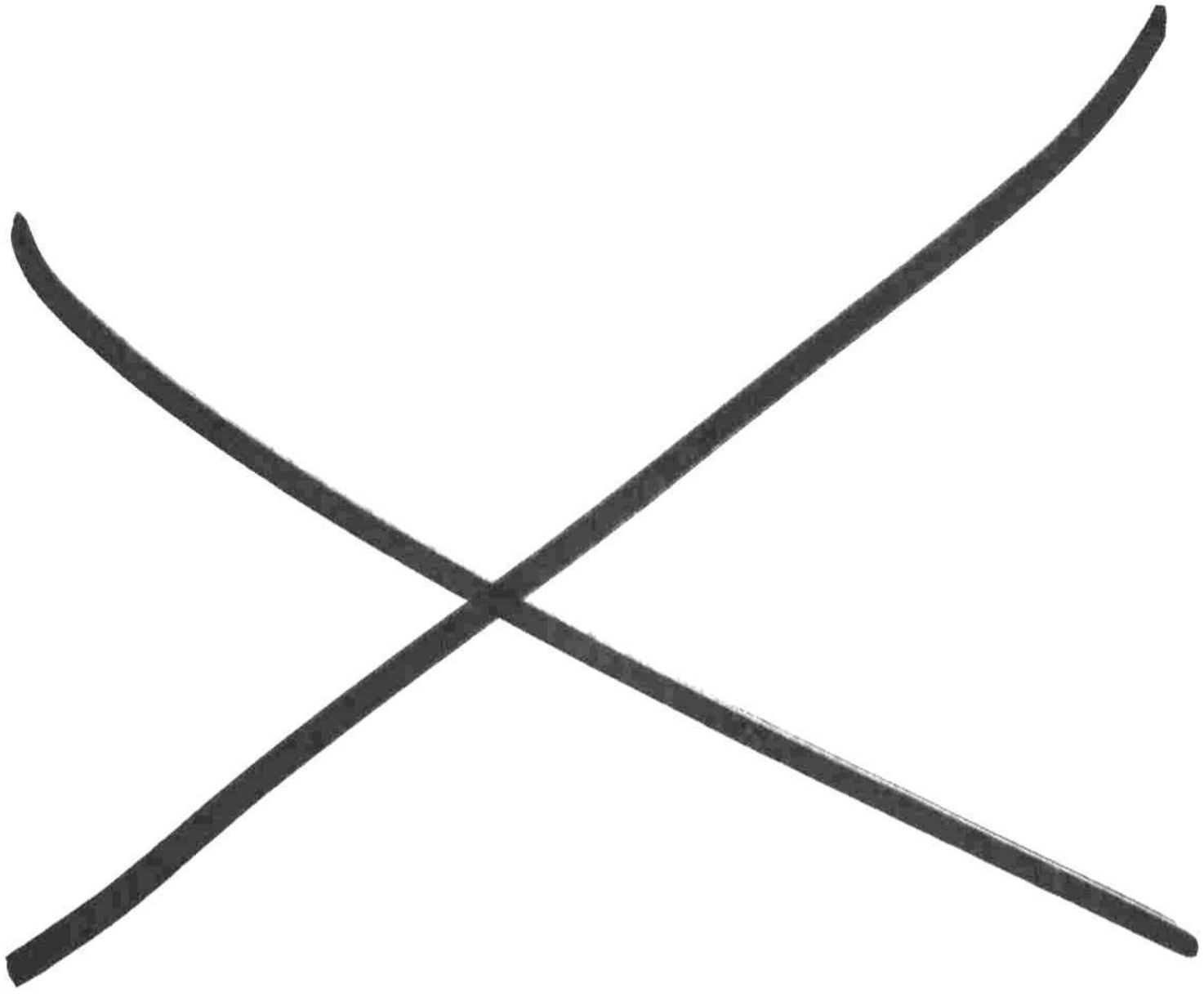
Peggy Marie Wood

Dr. Wood is a Research Analyst for Dataquest's Semiconductor Equipment and Materials Service. Her responsibilities include research and analysis of the semiconductor industry with respect to usage of materials in the semiconductor fabrication process and the technology and trends of semiconductor manufacturing automation. Prior to joining Dataquest, Dr. Wood was a postdoctoral research affiliate in the Department of Chemistry at Stanford University. While at Stanford, she supervised the installation of new research facilities and was responsible for the purchase of optical, electronic, and laser equipment. In addition to pursuing her own research in nonlinear chemical dynamics, Dr. Wood has taught undergraduate laboratory courses and supervised graduate student research. Dr. Wood received a B.S. degree in Chemistry from California State University at Sacramento and a Ph.D. in Chemistry from Stanford University.

Mark Reagan

Mr. Reagan is a Research Analyst for Dataquest's Semiconductor Equipment and Materials Service (SEMS). His primary responsibilities include maintenance of the SEMS worldwide fab data base and research support for the service's Econometrics notebook. Mr. Reagan has also performed research in the chemical vapor deposition, diffusion furnance, and physical vapor deposition equipment areas. Before joining Dataquest, Mr. Reagan worked as an Industry Consultant. In this capacity, he performed consulting projects for Dataquest involving the North American fab data base, financial aggregates, and R&D expenditures and aided in updating the company's worldwide equipment data base. Mr. Reagan received a B.A. degree in Business/Marketing from Western State College of Colorado at Gunnison.



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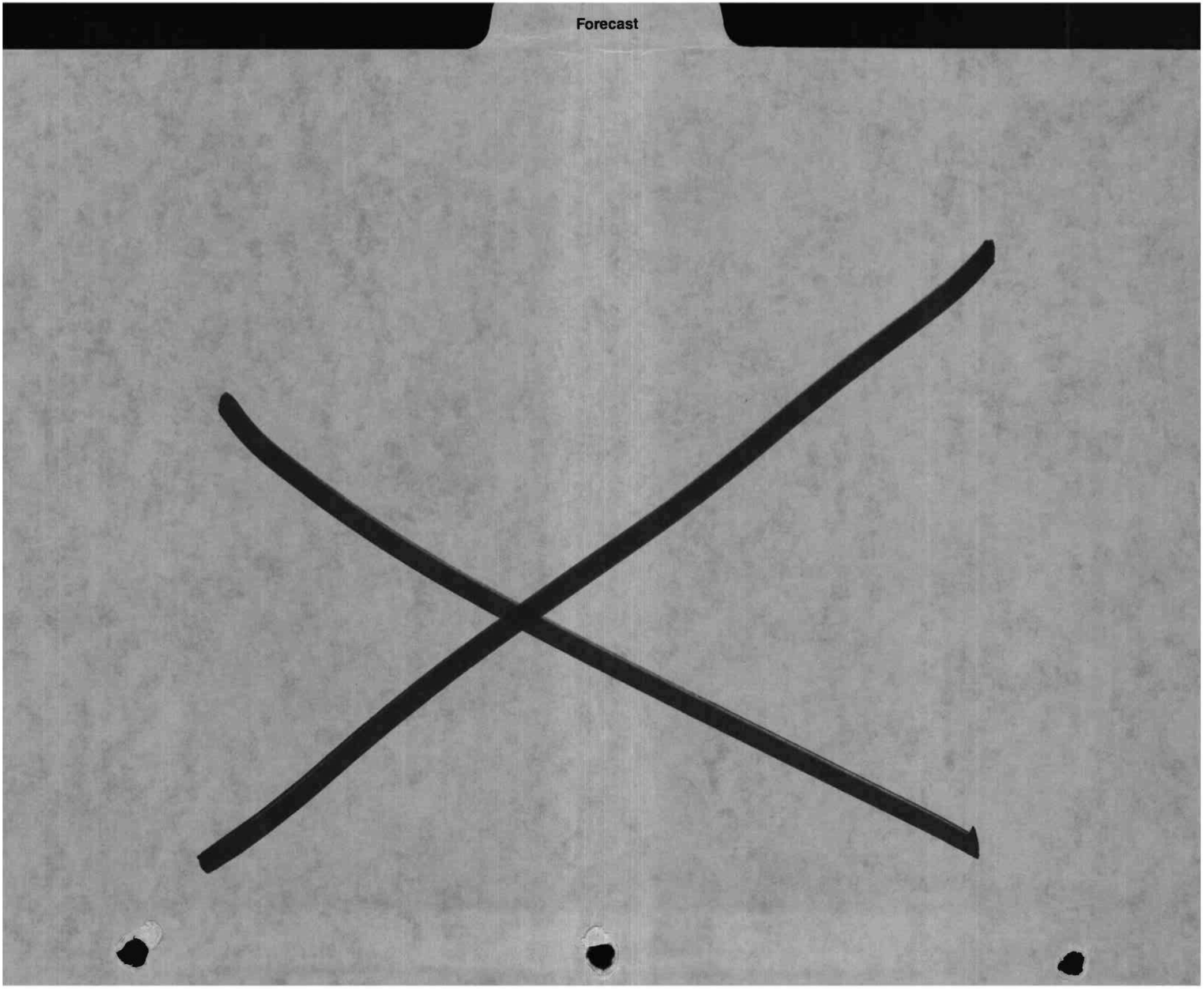

Forecast

The following is a list of the material in this section:

- Introduction to the Forecast
- Semiconductor Consumption
- Semiconductor Production
- Capital Spending
- Wafer Fabrication Equipment
- Silicon

For additional information, please refer to the material behind the Forecast tab in your Newsletter binder.

Semiconductor Consumption

INTRODUCTION

This section presents data on the worldwide semiconductor market by region. The regional semiconductor market, or regional semiconductor consumption, deals with where chips are consumed; this contrasts with regional semiconductor production, which deals with where chips are made. The data presented here are for the merchant market and do not include the value of chips made by captive semiconductor manufacturers for internal use.

SEMICONDUCTOR CONSUMPTION

Table 1 shows the historical regional semiconductor consumption for the years 1985 through 1989; it also breaks down the merchant market by nationality of the merchant semiconductor companies. Table 2 shows forecast semiconductor consumption by region for the period from 1990 through 1994. Figures 1 and 2 illustrate the data from Tables 1 and 2 in graphic format. Figure 3 depicts the share of the worldwide market by nationality of semiconductor company for the period from 1985 through 1989. Figure 4 also graphically illustrates the worldwide market shares by nationality of producer, covering the years 1985 and 1989.

Semiconductor Consumption

Table 1

Worldwide Semiconductor Consumption by Region
Merchant Company Sales Only—Historical
(Millions of Dollars)

	1985	1986	1987	1988	1989	Market Share 1989
North America						
U.S Companies	7,380	8,566	9,671	11,146	11,565	70.3%
Japanese Companies	1,279	1,434	2,110	3,277	4,303	20.7
European Companies	731	751	913	1,006	1,043	6.3
Asia/Pacific-ROW Companies	28	93	164	415	693	2.6
Total	9,418	10,844	12,858	15,844	17,604	100.0%
Japan						
U.S Companies	695	933	1,249	1,965	2,147	9.7%
Japanese Companies	7,387	10,851	13,588	18,630	19,823	89.4
European Companies	60	63	70	115	123	0.6
Asia/Pacific-ROW Companies	7	8	20	62	82	0.4
Total	8,149	11,855	14,927	20,772	22,175	100.0%
Europe						
U.S Companies	2,428	2,580	2,845	3,664	4,005	41.3%
Japanese Companies	549	715	900	1,466	1,913	19.7
European Companies	1,806	2,282	2,714	3,196	3,564	36.7
Asia/Pacific-ROW Companies	12	10	39	165	226	2.3
Total	4,795	5,587	6,498	8,491	9,708	100.0%
Rest of World (ROW)						
U.S Companies	548	730	1,165	1,811	2,056	32.4%
Japanese Companies	929	1,160	1,852	2,569	2,595	40.9
European Companies	254	347	503	600	682	10.7
Asia/Pacific-ROW Companies	248	311	448	772	1,016	16.0
Total	1,979	2,548	3,968	5,752	6,349	100.0%
Worldwide						
U.S Companies	11,051	12,809	14,930	18,586	19,773	35.4%
Japanese Companies	10,144	14,160	18,450	25,942	28,634	51.3
European Companies	2,851	3,443	4,200	4,917	5,412	9.7
Asia/Pacific-ROW Companies	295	422	671	1,414	2,017	3.6
Total	24,341	30,834	38,251	50,859	55,836	100.0%
Percentage Growth	(15.6%)	26.7%	24.1%	33.0%	9.8%	

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
January 1990

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Semiconductor Consumption

Table 2

Worldwide Semiconductor Consumption by Region
Merchant Company Sales Only—Forecast
(Millions of Dollars)

	1990	1991	1992	1993	1994	CAGR 1990-1994
North America	$18,095	$20,661	$24,936	$ 32,876	$ 34,850	18%
Growth	2.8%	14.2%	20.7%	31.8%	6.0%	
Japan	$22,091	$25,233	$30,061	$ 38,642	$ 42,111	18%
Growth	(0.4%)	14.2%	19.1%	28.5%	9.0%	
Europe	$ 9,414	$11,036	$13,735	$ 17,991	$ 20,010	19%
Growth	(3.0%)	17.2%	24.4%	31.0%	11.2%	
Rest of World	$ 6,416	$ 7,708	$10,675	$ 14,803	$ 16,308	23%
Growth	1.1%	20.1%	38.4%	38.7%	10.2%	
Total Worldwide Market	$56,016	$64,638	$79,408	$104,313	$113,279	19%
Percentage Growth	0.3%	15.5%	22.8%	31.4%	8.6%	

Source: Dataquest
January 1990

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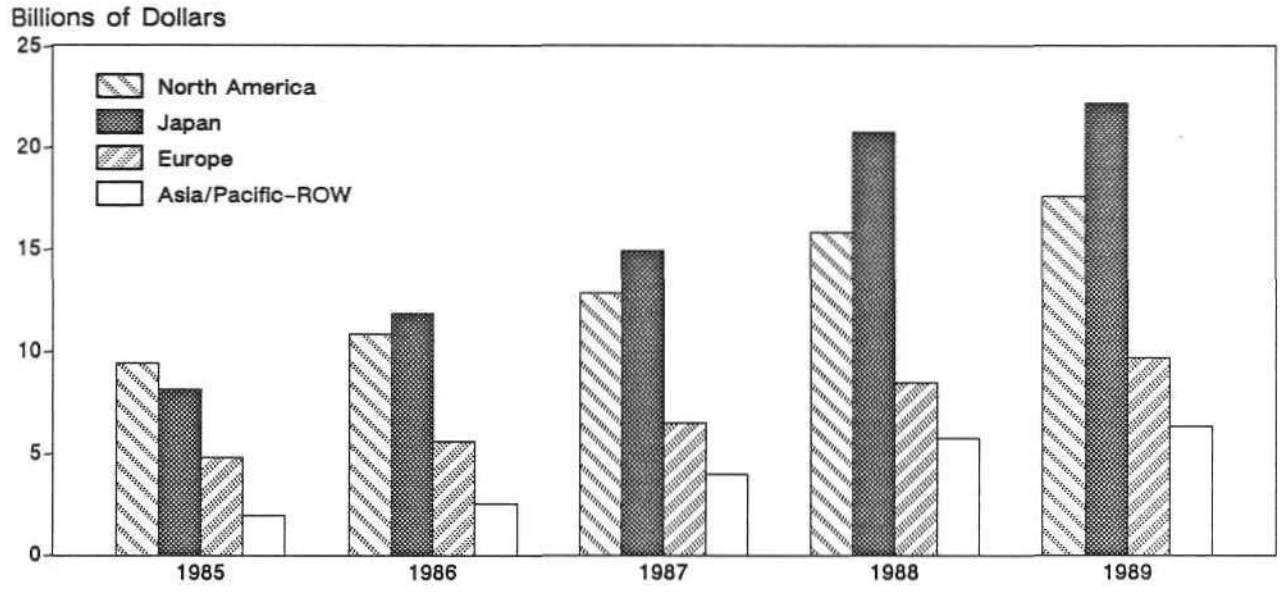
Semiconductor Consumption

Figure 1

Worldwide Semiconductor Consumption
Merchant Market—Historical



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Source: Dataquest
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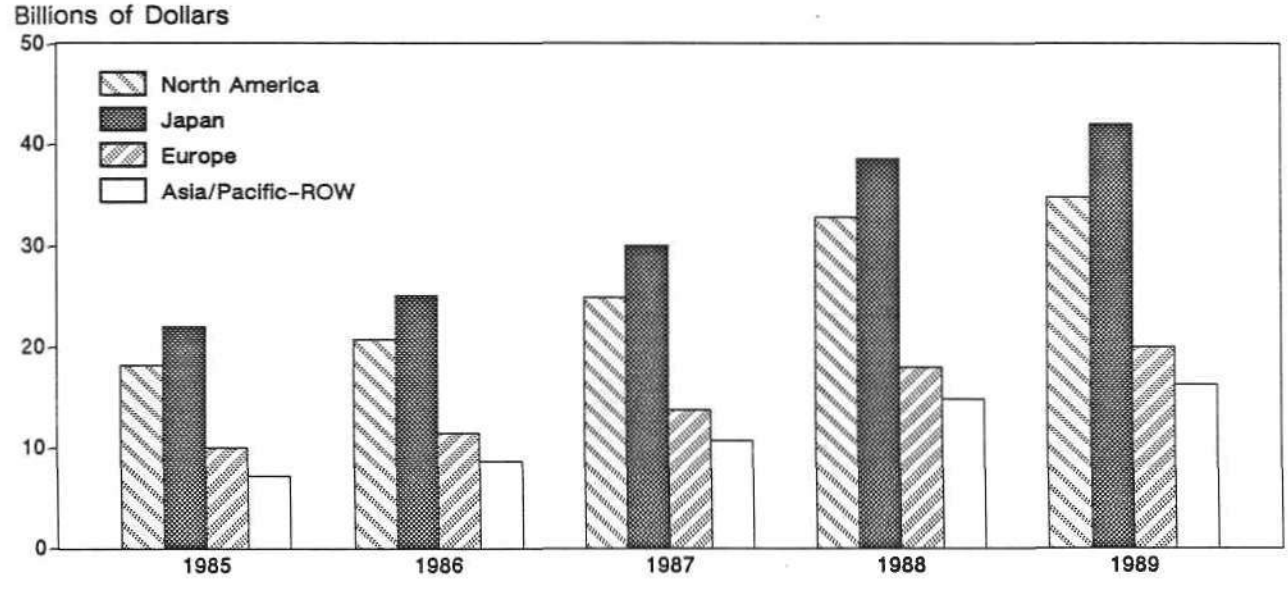
Figure 2

Worldwide Semiconductor Consumption
Merchant Market—Forecast



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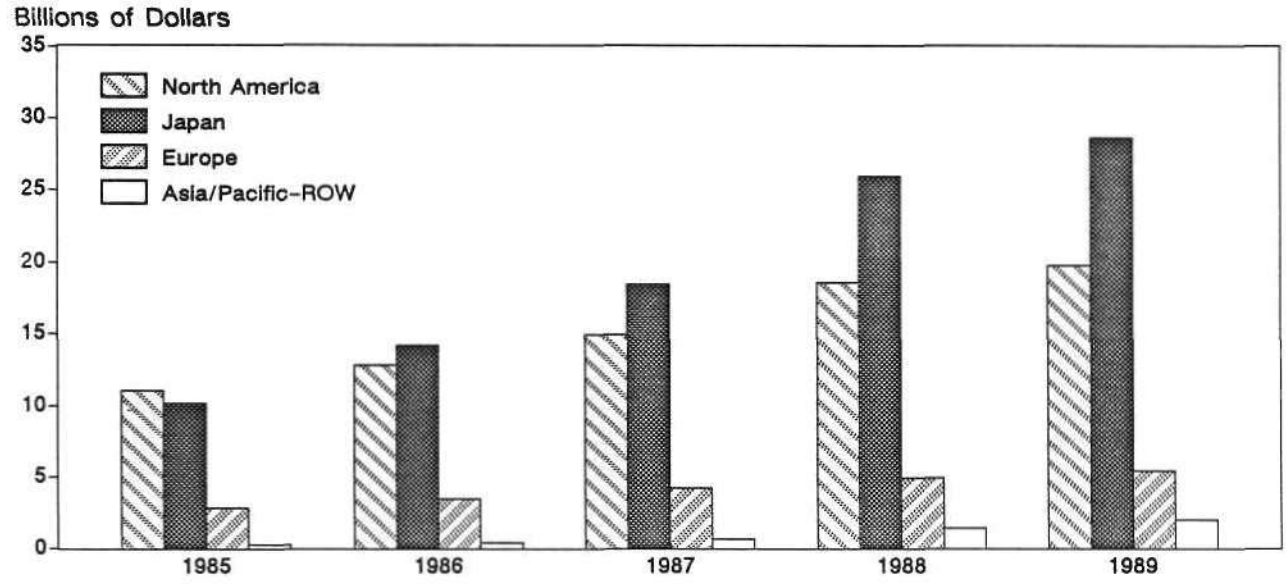
Semiconductor Consumption

Figure 3

Merchant Semiconductor Company Sales Worldwide—Historical



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Source: Dataquest
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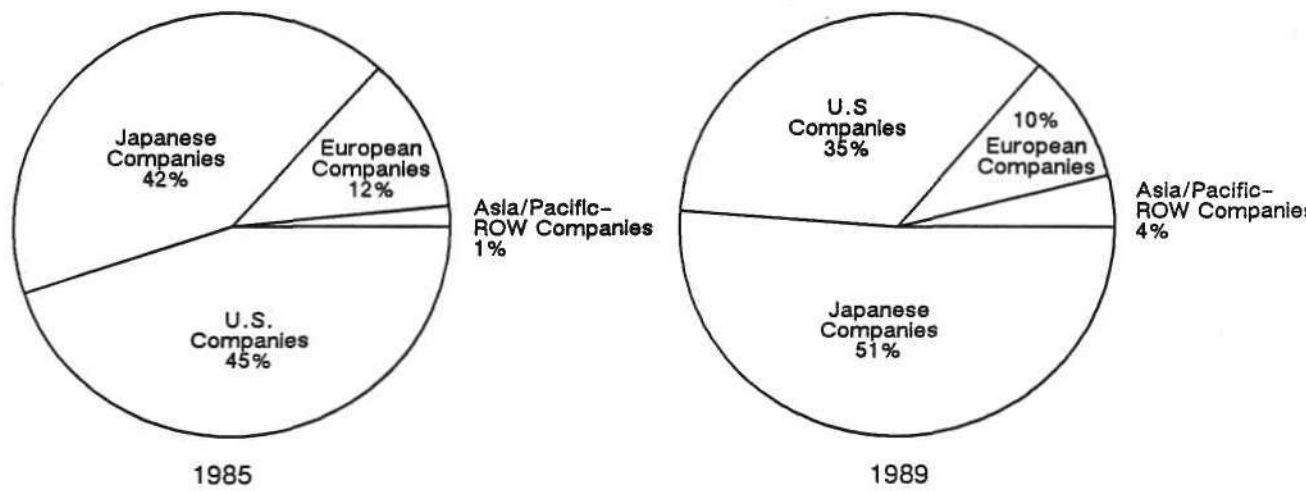
Figure 4

Merchant Semiconductor Company Sales Worldwide by Region



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Source: Dataquest
January 1990

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Semiconductor Production

INTRODUCTION

This section presents data on worldwide semiconductor production by region. Semiconductor production is defined by the place where the wafers are fabricated, and regional semiconductor production includes all production in the region, including merchant and captive producers and all foreign producers. For instance, North American semiconductor production includes IBM and Delco fabs as well as Japanese and European fabs in the United States.

SEMICONDUCTOR PRODUCTION

Table 1 shows historical semiconductor production for the years 1985 through 1989, and Table 2 shows forecast production for the period from 1990 through 1994. Figures 1 and 2 illustrate the same data graphically. Figure 3 depicts the five-year trend for regional production; it shows percent production by region in 1985 and in 1989.

For more detailed information on semiconductor production, please refer to the "Capital Spending" section in the SEMS Semiconductor Manufacturing binder.

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Semiconductor Production

Table 1

Worldwide Semiconductor Production by Region
Merchant and Captive—Historical
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
North America						
Merchant	10,411	12,129	14,116	17,226	18,609	16%
Captive	2,243	2,327	2,596	2,945	3,271	10%
Total	12,654	14,456	16,712	20,171	21,880	15%
Japan						
Merchant	10,500	14,524	18,824	26,488	28,834	29%
Captive	151	162	180	205	227	11%
Total	10,651	14,686	19,004	26,693	29,061	29%
Europe						
Merchant	3,024	3,426	4,220	5,277	5,871	18%
Captive	379	405	451	512	568	11%
Total	3,403	3,831	4,671	5,789	6,439	17%
ROW						
Merchant	406	756	1,088	1,868	2,522	58%
Captive	0	0	0	0	0	N/A
Total	406	756	1,088	1,868	2,522	58%
Total Worldwide						
Merchant	24,341	30,834	38,251	50,859	55,836	23%
Captive	2,773	2,894	3,227	3,662	4,066	10%
Total Production	27,114	33,728	41,478	54,521	59,902	22%
Percentage Growth	(15.6%)	24.4%	23.0%	31.4%	9.9%	

N/A = Not Applicable

Source: Dataquest
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Semiconductor Production

Table 2

Worldwide Semiconductor Production by Region
Merchant and Captive—Forecast
(Millions of Dollars)

	1990	1991	1992	1993	1994	CAGR 1990-1994
North America						
Merchant	17,806	20,557	25,654	34,068	36,582	20%
Captive	3,350	3,834	4,602	6,046	6,521	18%
Total	21,156	24,391	30,256	40,114	43,103	19%
Japan						
Merchant	28,141	30,877	36,599	47,391	50,790	16%
Captive	233	267	320	420	453	18%
Total	28,374	31,144	36,919	47,811	51,243	16%
Europe						
Merchant	6,944	8,985	11,795	15,825	17,748	26%
Captive	582	666	800	1,051	1,133	18%
Total	7,526	9,651	12,595	16,876	18,881	26%
ROW						
Merchant	3,125	4,220	5,359	7,028	8,158	27%
Captive	0	0	0	0	0	
Total	3,125	4,220	5,359	7,028	8,158	27%
Total Worldwide						
Merchant	56,017	64,640	79,408	104,314	113,278	19%
Captive	4,165	4,767	5,722	7,517	8,107	18%
Total	60,182	69,407	85,130	111,831	121,385	19%
Percentage Growth	0.5%	15.3%	22.7%	31.4%	8.5%	

Source: Dataquest
January 1990

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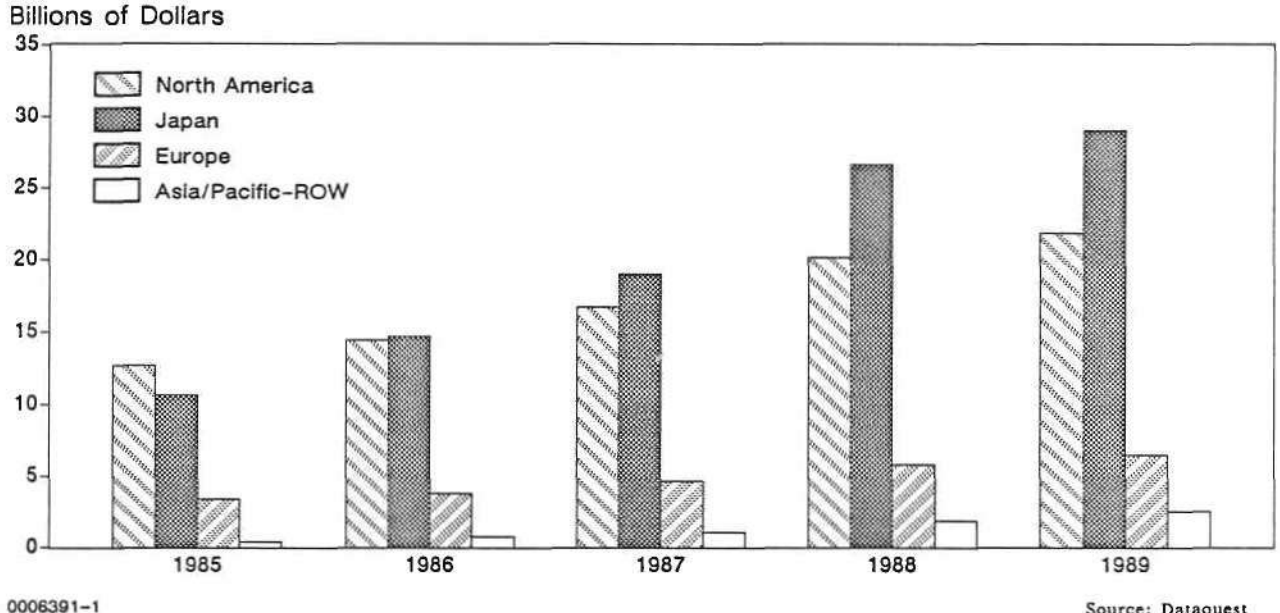
Semiconductor Production

Figure 1

Worldwide Semiconductor Production
Merchant and Captive—Historical

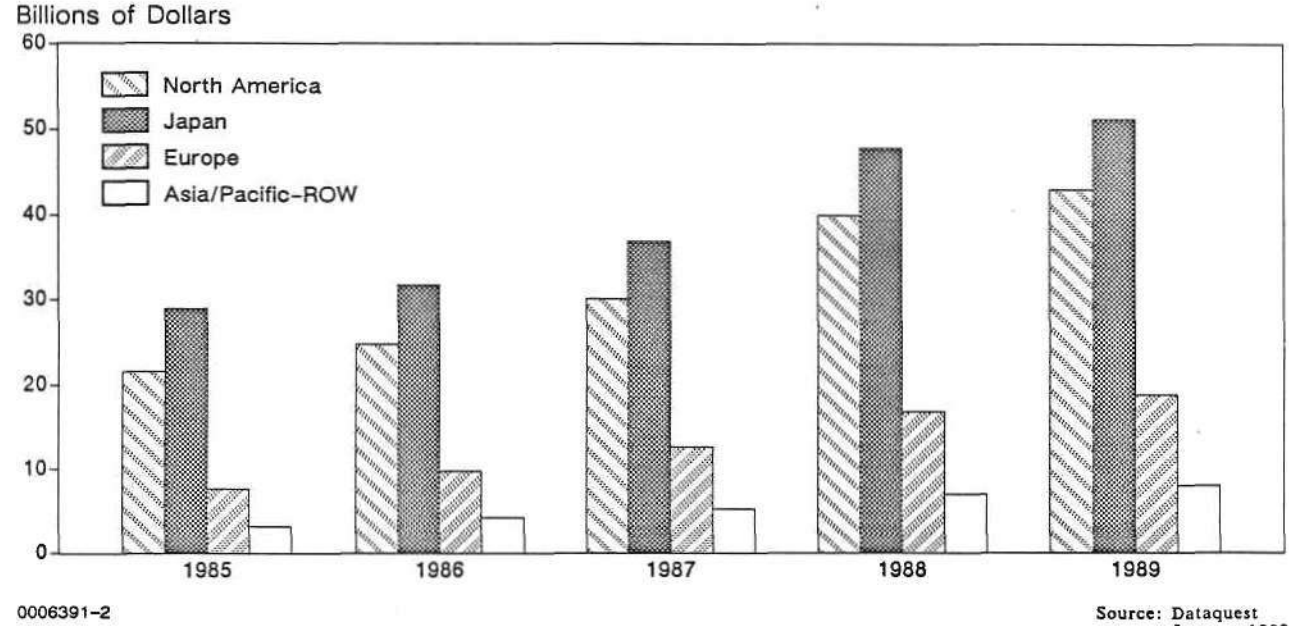


0006391-1

Source: Dataquest
January 1990

Figure 2

Worldwide Semiconductor Production
Merchant and Captive—Forecast



0006391-2

Source: Dataquest
January 1990

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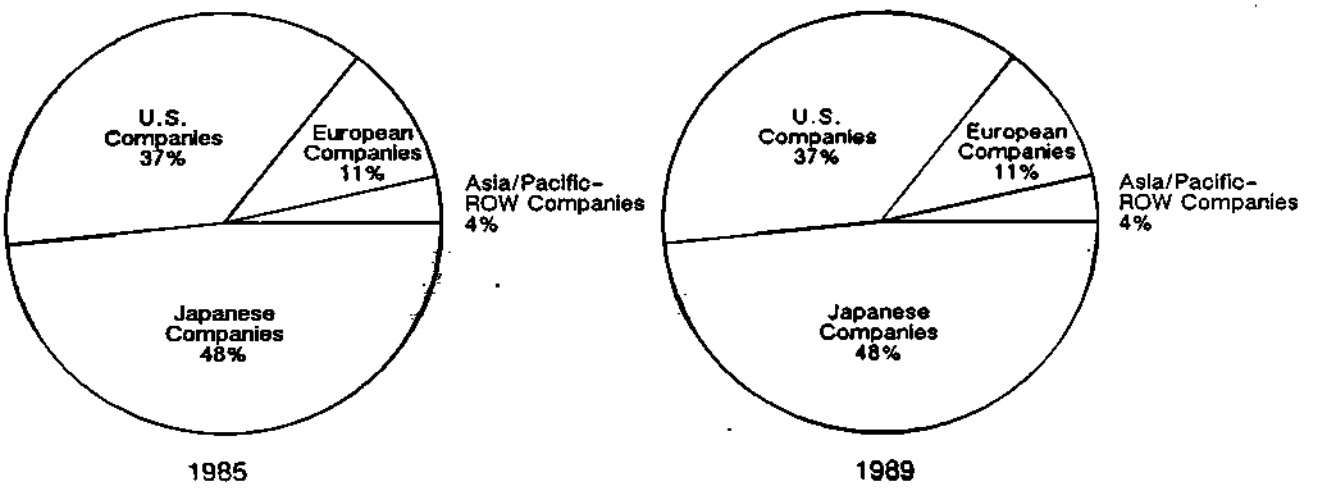
Semiconductor Production

Figure 3

Worldwide Semiconductor Production
Merchant and Captive Regional Share



0006391-3

Source: Dataquest January 1990

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Capital Spending

INTRODUCTION

This section presents data on worldwide semiconductor capital spending by region. Capital spending in a region includes spending by all semiconductor producers in that region, including spending by merchant and captive producers as well as foreign producers. For instance, capital spending in North America includes spending by IBM, Delco, and Japanese and European semiconductor companies building wafer fabrication, assembly, and test facilities in the United States.

CAPITAL SPENDING FORECAST

Table 1 shows historical capital spending for the years 1985 through 1989, and Table 2 shows forecast spending for the period from 1990 through 1994. Figures 1 and 2 illustrate the same data graphically. Figure 3 depicts the five-year trend for regional capital spending; it shows percentage of spending by region in 1985 and in 1989.

For more detailed information on capital spending, please refer to the "Capital Spending" section in the SEMS Semiconductor Manufacturing binder.

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Capital Spending

Table 1

Worldwide Capital Spending by Region
Merchant and Captive—Historical
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
North America						
Merchant	1,978	1,438	1,911	2,569	2,931	10%
Captive	651	644	683	865	891	8%
Total	2,629	2,082	2,594	3,434	3,822	10%
Japan						
Merchant	3,292	1,800	2,384	4,550	5,306	13%
Captive	44	45	47	60	62	9%
Total	3,336	1,845	2,432	4,610	5,368	13%
Europe						
Merchant	690	653	757	834	1,046	11%
Captive	110	112	119	150	155	9%
Total	800	765	875	984	1,201	11%
ROW						
Merchant	534	437	534	1,060	1,854	37%
Captive	0	0	0	0	0	
Total	534	437	534	1,060	1,854	37%
Total Worldwide						
Merchant	6,494	4,328	5,586	9,013	11,137	14%
Captive	805	801	849	1,075	1,108	8%
Total Capital Spending	7,299	5,129	6,435	10,088	12,245	14%
Percentage Growth	(17.4%)	(29.7%)	25.5%	56.8%	21.4%	

Source: Dataquest
January 1990

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Capital Spending

Table 2

Worldwide Capital Spending by Region
Merchant and Captive—Forecast
(Millions of Dollars)

	1990	1991	1992	1993	1994	CAGR 1990-1994
North America						
Merchant	2,872	3,459	4,546	5,769	5,995	20%
Captive	886	1,006	1,289	1,640	1,810	20%
Total	3,759	4,465	5,835	7,409	7,805	20%
Japan						
Merchant	5,028	6,565	8,712	10,976	11,108	22%
Captive	62	70	90	114	126	19%
Total	5,090	6,635	8,802	11,090	11,234	22%
Europe						
Merchant	1,119	1,511	2,106	2,658	2,948	27%
Captive	154	175	224	285	315	20%
Total	1,273	1,686	2,330	2,943	3,262	27%
ROW						
Merchant	1,877	2,333	2,985	3,433	3,983	21%
Captive	0	0	0	0	0	
Total	1,877	2,333	2,985	3,433	3,983	21%
Total Worldwide						
Merchant	10,896	13,868	18,349	22,836	24,034	22%
Captive	1,102	1,251	1,603	2,039	2,251	20%
Total Capital Spending	11,998	15,119	19,951	24,876	26,284	22%
Percentage Growth	(2.0%)	26.0%	32.0%	24.7%	5.7%	

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
January 1990

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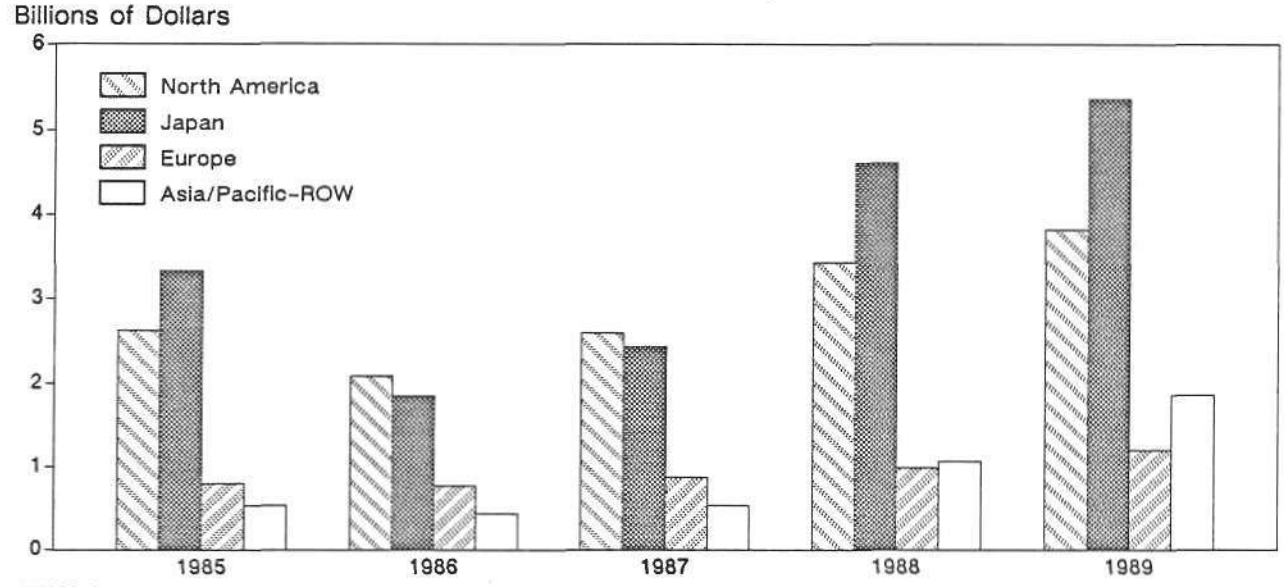
Capital Spending

Figure 1

Worldwide Capital Spending
Merchant and Captive—Historical
(Billions of Dollars)



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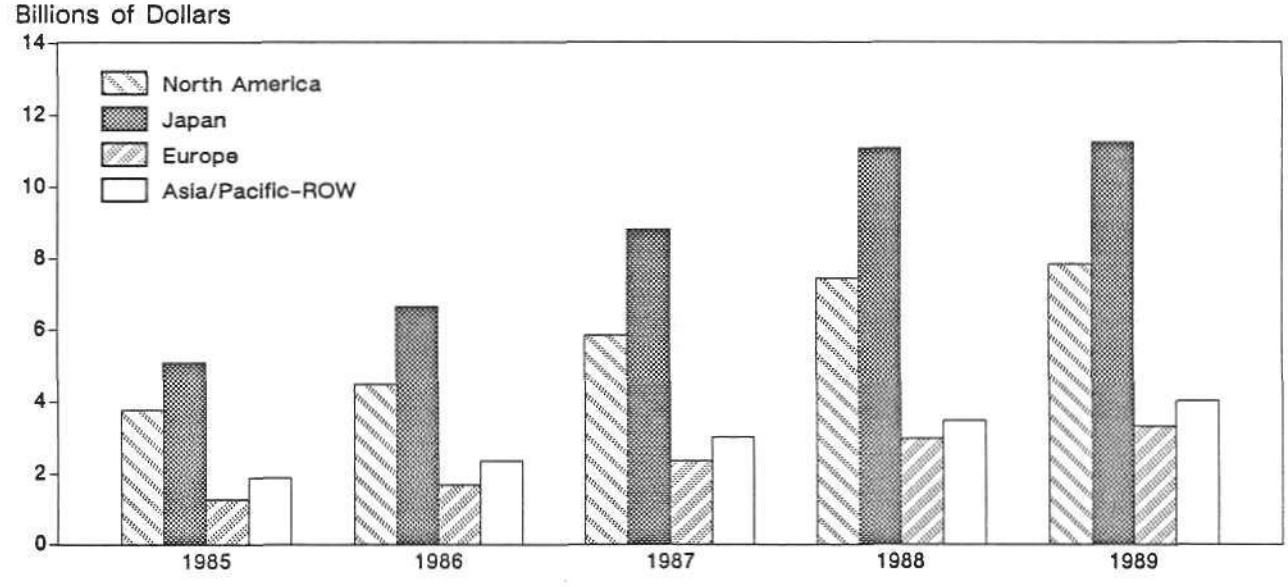
Source: Dataquest
January 1990

Figure 2

Worldwide Capital Spending
Merchant and Captive—Forecast
(Billions of Dollars)



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Source: Dataquest
January 1990

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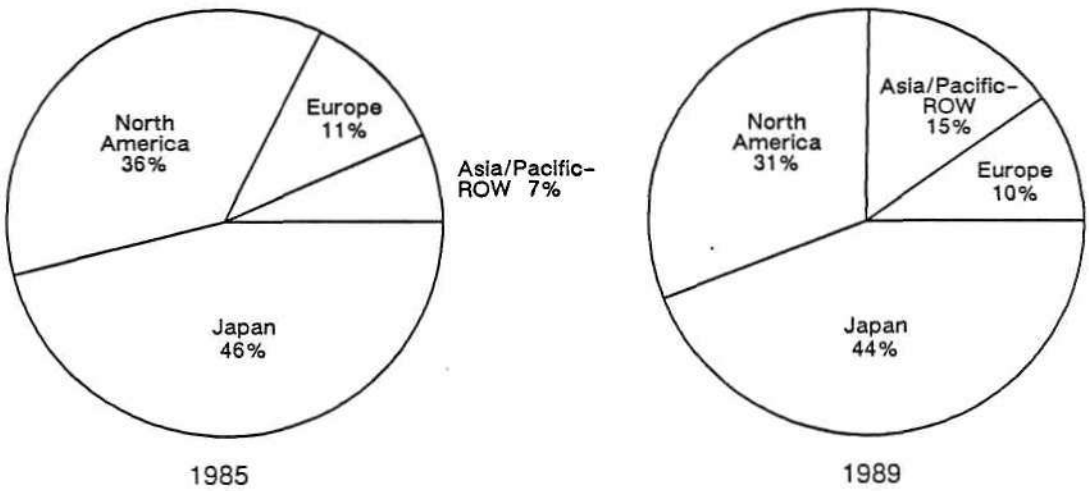
Capital Spending

Figure 3

Worldwide Capital Spending
Merchant and Captive
Regional Share



0006392-3

Source: Dataquest January 1990

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Wafer Fabrication Equipment

INTRODUCTION

This section presents historical and forecast data on the worldwide wafer fabrication equipment market. Table 1 presents the historical data by equipment category for the years 1985 through 1989, and Table 2 shows forecast data by category for the years 1990 through 1994.

PRODUCTION VERSUS SPENDING

Table 3 summarizes the historical worldwide semiconductor production, capital spending, and wafer fab equipment expenditure for the years 1985 through 1989. Table 4 presents Dataquest's forecast regarding these items for the years 1990 through 1994.

MARKET GROWTH

Figure 1 shows year-to-year growth for semiconductor production and wafer fab equipment for the 10-year period from 1985 through 1994. Table 5 shows the compound annual growth rate (CAGR) forecast for semiconductor production, capital spending, and wafer fab equipment.

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Wafer Fabrication Equipment

Table 1

Worldwide Wafer Fab Equipment Market—Historical
(Millions of Dollars)

	1985	1986	1987	1988	1989*	CAGR 1985-1989
World Fab Equipment Market	3,356	2,713	3,148	4,894	5,779	15%
Lithography						
Proximity/Contact	48	31	24	21	20	(20%)
Projection Aligners	266	171	129	159	152	(13%)
Steppers	430	363	503	903	1,084	26%
Direct-Write E-Beam	31	68	67	68	70	23%
Maskmaking E-Beam	81	51	68	59	70	(4%)
X-Ray	2	1	0	9	12	61%
Total	858	685	790	1,219	1,408	13%
Automatic Photoresist Processing Equipment	158	146	164	250	282	16%
Etch and Clean						
Wet Process	157	162	165	235	289	16%
Dry Strip	39	34	52	90	110	30%
Dry Etch	300	237	307	547	650	21%
Ion Milling	7	7	7	8	9	8%
Total	502	440	531	880	1,058	21%
Deposition						
Chemical Vapor Dep.	247	219	254	455	540	22%
Physical Vapor Dep.	263	237	249	315	400	11%
Silicon Epitaxy	72	46	36	85	60	(4%)
Metalorganic CVD	25	32	36	43	52	20%
Molecular Beam Epitaxy	53	69	71	85	100	17%
Total	659	604	646	982	1,152	15%
Diffusion	207	156	173	266	330	12%
Rapid Thermal Processing	14	15	19	22	27	17%

(Continued)

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Table 1 (Continued)

Worldwide Wafer Fab Equipment Market—Historical
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
Ion Implantation						
Medium-Current	125	55	61	118	153	5%
High-Current	167	55	107	241	302	16%
High-Voltage	2	10	18	20	22	80%
Total	293	119	186	379	477	13%
CD/Wafer Inspection	55	71	99	173	221	23%
Other Process Control	368	303	332	427	469	6%
Factory Automation	125	81	99	130	153	14%
Other Equipment	117	94	110	167	202	9%
Total	3,356	2,713	3,148	4,894	5,779	10.1%
Percentage Growth	(4.6%)	(19.2%)	16.0%	55.5%	18.1%	

N/A = Not Applicable
*Preliminary Estimate
Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
January 1990

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Wafer Fabrication Equipment

Table 2

Worldwide Wafer Fab Equipment Market—Forecast
(Millions of Dollars)

	1990	1991	1992	1993	1994	CAGR 1990-1994
World Fab Equipment Market	5,785	7,170	9,299	11,330	12,280	21%
Lithography						
Proximity/Contact	20	22	23	24	25	6%
Projection Aligners	148	180	235	287	303	20%
Steppers	1,142	1,421	1,858	2,335	2,516	22%
Direct-Write E-Beam	75	83	100	125	140	17%
Maskmaking E-Beam	78	91	116	143	150	18%
X-Ray	20	30	40	55	70	37%
Total	1,483	1,827	2,372	3,969	3,204	21%
Automatic Photoresist Processing Equipment	289	356	463	564	609	20%
Etch and Clean						
Wet Process	278	350	450	560	600	21%
Dry Strip	110	140	190	220	240	22%
Dry Etch	640	800	1,505	1,250	1,350	21%
Ion Milling	10	12	14	16	16	12%
Total	1,038	1,302	1,704	2,046	2,206	21%
Deposition						
Chemical Vapor Dep.	530	675	875	1,050	1,150	21%
Physical Vapor Dep.	390	490	650	750	820	20%
Silicon Epitaxy	55	61	85	104	112	19%
Metalorganic CVD	62	74	90	108	128	20%
Molecular Beam Epitaxy	108	123	140	150	165	11%
Total	1,145	1,423	1,840	2,162	2,375	20%
Diffusion	300	375	480	575	625	20%
Rapid Thermal Processing	26	34	45	60	70	28%

(Continued)

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Wafer Fabrication Equipment

Table 2 (Continued)

Worldwide Wafer Fab Equipment Market—Forecast
(Millions of Dollars)

	1990	1991	1992	1993	1994	CAGR 1990-1994
Ion Implantation						
Medium Current	136	168	223	272	259	17%
High Current	262	320	412	484	470	16%
High Voltage	29	40	56	72	85	31%
Total	427	528	691	828	814	18%
CD/Wafer Inspection	257	328	426	522	587	23%
Other Process Control	459	540	685	847	868	17%
Factory Automation	158	206	268	360	492	15%
Other Equipment	202	251	325	397	430	15%
Total	5,785	7,170	9,299	11,330	12,280	21%
Percentage Growth	0.1%	24.0%	29.7%	21.8%	8.4%	

Source: Dataquest
January 1990

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Table 3

Worldwide Semiconductor Production and Capital Spending
1982–1987
(Millions of Dollars)

	1985	1986	1987	1988	1989*	CAGR 1984-1988
Production**	27,114	33,728	41,478	54,521	59,902	22%
Capital Spending	7,299	5,129	6,435	10,088	12,245	14%
Wafer Fab Equipment	3,356	2,713	3,148	4,894	5,779	15%
Percentage Growth	(4.6%)	(19.2%)	16.0%	55.5%	18.1%	

*Preliminary estimate
**Semiconductor production includes worldwide merchant and captive production.

Source: Dataquest
January 1990

Table 4

Estimated Worldwide Semiconductor Production and Capital Spending
1988–1992
(Millions of Dollars)

	1990	1991	1992	1993	1994	CAGR 1990-1994
Production*	61,460	70,678	85,130	111,830	121,386	19%
Capital Spending	11,998	15,119	19,951	24,876	26,284	22%
Wafer Fab Equipment	5,785	7,170	9,299	11,330	12,280	21%
Percentage Growth	0.1%	24.0%	29.7%	21.8%	8.4%	

*Semiconductor production includes worldwide merchant and captive production.

Source: Dataquest
January 1990

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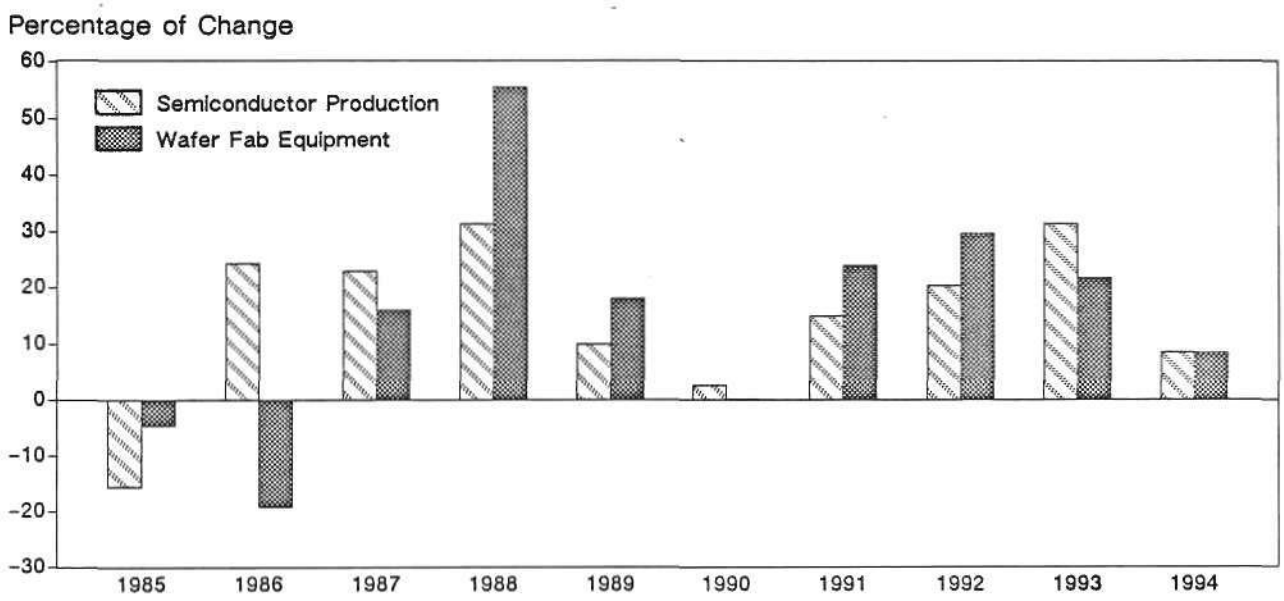
Wafer Fabrication Equipment

Figure 1

Estimated Semiconductor Production and Wafer Fab Equipment
Ten-Year Growth Pattern
1983–1992



0006393-1

Source: Dataquest
January 1990

Estimated Ten-Year CAGR
1985–1994

	CAGR 1985-1994
Semiconductor Production	18%
Capital Spending	15%
Wafer Fab Equipment	16%

Source: Dataquest
January 1990

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Silicon

Tables 1 and 2 present the historical and forecast consumption of silicon in millions of square inches by region. For more detailed information on silicon, please refer to the "Semiconductor Materials" section in the SEMS Equipment and Materials notebook.

Table 1

Historical Silicon Consumption by Region—1985-1989
(Million Square Inches)

	1985	1986	1987	1988	1989	CAGR 1985-1989
United States	398	405	435	496	571	9.4%
Growth	(43.7%)	1.9%	7.3%	13.6%	14.9%	
Japan	588	642	670	772	909	11.5%
Growth	(11.0%)	9.1%	4.4%	15.2%	17.6%	
Europe	148	155	172	196	218	10.1%
Growth	(7.5%)	4.6%	10.9%	14.0%	11.2%	
Rest of World	43	64	78	98	127	31.2%
Growth	(15.7%)	47.9%	22.0%	26.8%	29.4%	
Total	1,177	1,266	1,355	1,562	1,825	11.6%
Growth	(25.5%)	7.5%	7.0%	15.2%	16.7%	

Source: Dataquest (August 1990)

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Table 2

Forecast Silicon Consumption by Region—1989-1994
(Million Square Inches)

	1989	1990	1991	1992	1993	1994	CAGR 1989-1994
United States	571	578	647	757	929	924	10.1%
Growth	14.9%	1.8%	11.9%	17.0%	22.8%	(0.5%)	
Japan	909	985	1,029	1,151	1,368	1,345	8.2%
Growth	17.6%	8.5%	4.5%	11.8%	18.8%	(1.7%)	
Europe	218	253	311	385	483	505	18.2%
Growth	11.2%	15.7%	23.3%	23.7%	25.2%	4.6%	
Rest of World	127	181	217	255	301	315	19.8%
Growth	29.4%	42.4%	19.5%	17.6%	18.1%	4.6%	
Total	1,825	1,997	2,204	2,548	3,081	3,089	11.1%
Growth	16.7%	9.6%	10.4%	15.6%	20.9%	0.3%	

Source: Dataquest (August 1990)

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Introduction to Forecast

The following material is found in this section:

- Introduction to Forecast
- Semiconductor Consumption Forecast
- Semiconductor Production Forecast
- Capital Spending Forecast
- Wafer Fab Equipment Forecast

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Introduction to Forecast

INTRODUCTION

The purpose of this forecast section is to provide the Semiconductor Equipment and Materials Service (SEMS) client with historical and forecast data for semiconductor consumption, semiconductor production, capital spending, and wafer fab equipment in one easily accessible location. Previously, this related information was (and still is) dispersed throughout the two SEMS notebooks; now it has been brought together and presented here in this section as well.

Only top–level data have been located here for quick reference, and no analysis of the data is included here. Such analysis can be found in the more complete discussions of the topics in their respective locations in the notebooks. The intent of this section is to provide a "quick look" at key industry parameters all in one place.

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Semiconductor Consumption

Heading	Page
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Semiconductor Consumption	1

Table	Title	
Table 1	Worldwide Semiconductor Consumption by Region Merchant Company Sales Only - Historical	2
Table 2	Worldwide Semiconductor Consumption by Region Merchant Company Sales Only - Forecast	3

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Figure 3	Merchant Semiconductor Company Sales Worldwide - Historical	5
Figure 4	Merchant Semiconductor Sales Worldwide by Region	5

Semiconductor Consumption

INTRODUCTION

This section presents data on the worldwide semiconductor market by region. The regional semiconductor market, or regional semiconductor consumption, deals with where chips are consumed; this contrasts with regional semiconductor production, which deals with where chips are made. The data presented here are for the merchant market and do not include the value of chips made by captive semiconductor manufacturers for internal use.

SEMICONDUCTOR CONSUMPTION

Table 1 shows the historical regional semiconductor consumption for the years 1984 through 1988; it also breaks down the merchant market by nationality of the merchant semiconductor companies. Table 2 shows forecast semiconductor consumption by region for the period from 1989 through 1993. Figures 1 and 2 illustrate the data from Tables 1 and 2 in graphic format. Figure 3 depicts the share of the worldwide market by nationality of semiconductor company for the period from 1984 through 1988. Figure 4 also graphically illustrates the worldwide market shares by nationality of producer, but it covers the years 1984 and 1988.

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Semiconductor Consumption

Table 1

Worldwide Semiconductor Consumption by Region
Merchant Company Sales Only—Historical
(Millions of Dollars)

	1984	1985	1986	1987	1988	Market Share 1988
North America						
U.S. Companies	9,767	7,380	8,565	9,698	11,290	70.5%
Japanese Companies	2,065	1,279	1,434	2,070	3,241	20.2%
European Companies	1,157	731	751	913	1,062	6.6%
ROW Companies	17	28	93	164	420	2.6%
Total U.S. Market	13,006	9,418	10,843	12,845	16,013	100.0%
Japan						
U.S. Companies	926	695	933	1,248	1,936	9.5%
Japanese Companies	7,787	7,387	10,851	13,654	18,228	89.7%
European Companies	56	60	63	70	106	0.5%
ROW Companies	5	7	8	20	62	0.3%
Total Japanese Market	8,774	8,149	11,855	14,992	20,332	100.0%
Europe						
U.S. Companies	2,548	2,428	2,580	2,828	3,675	43.3%
Japanese Companies	597	549	715	899	1,437	16.9%
European Companies	1,717	1,806	2,282	2,714	3,215	37.9%
ROW Companies	2	12	10	39	165	1.9%
Total European Market	4,864	4,795	5,587	6,480	8,492	100.0%
Rest of World (ROW)						
U.S. Companies	707	548	730	1,157	1,787	31.6%
Japanese Companies	1,007	929	1,160	1,853	2,495	44.1%
European Companies	253	254	347	503	606	10.7%
ROW Companies	214	248	311	448	767	13.6%
Total ROW Market	2,181	1,979	2,548	3,961	5,655	100.0%
Worldwide						
U.S. Companies	13,948	11,051	12,808	14,931	18,688	37.0%
Japanese Companies	11,456	10,144	14,160	18,476	25,401	50.3%
European Companies	3,183	2,851	3,443	4,200	4,989	9.9%
ROW Companies	238	295	422	671	1,414	2.8%
Total Worldwide Market	28,825	24,341	30,833	38,278	50,492	100.0%
Growth Rate	47.5%	(15.6%)	26.7%	24.1%	31.9%	

Source: Dataquest
June 1989

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Semiconductor Consumption

Table 2

Worldwide Semiconductor Consumption by Region
Merchant Company Sales Only—Forecast
(Millions of Dollars)

	1989	1990	1991	1992	1993	CAGR 1989-1993
North America	$18,348	$17,643	$20,304	$24,585	$ 33,340	16.1%
Growth	14.6%	(3.8%)	15.1%	21.1%	35.6%	
Japan	$23,366	$23,060	$26,656	$31,931	$ 42,548	16.2%
Growth	14.9%	(1.3%)	15.6%	19.8%	33.2%	
Europe	$ 9,357	$ 9,594	$11,126	$14,564	$ 17,135	16.3%
Growth	10.2%	2.5%	16.0%	30.9%	17.7%	
Rest of World	$ 7,133	$ 7,593	$ 9,374	$11,954	$ 16,337	23.0%
Growth	26.2%	6.4%	23.5%	27.5%	36.7%	
Total Worldwide Market	$58,204	$57,890	$67,460	$83,034	$109,360	17.1%
Growth	15.3%	(0.5%)	16.5%	23.1%	31.7%	

Source: Dataquest
June 1989

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Semiconductor Consumption

Figure 1

Worldwide Semiconductor Consumption
Merchant Market—Historical

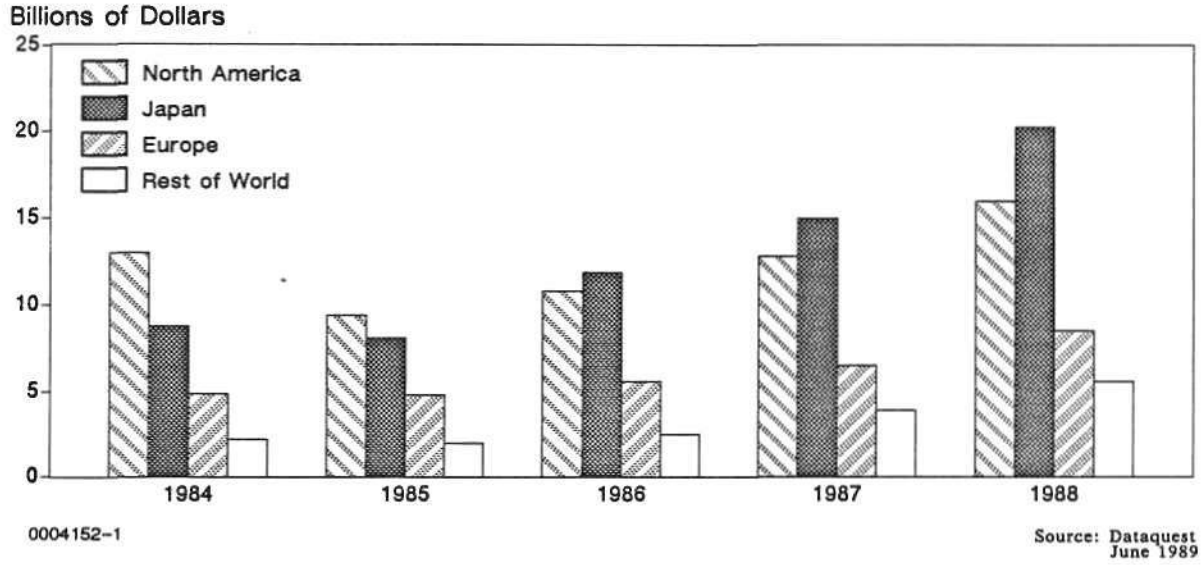
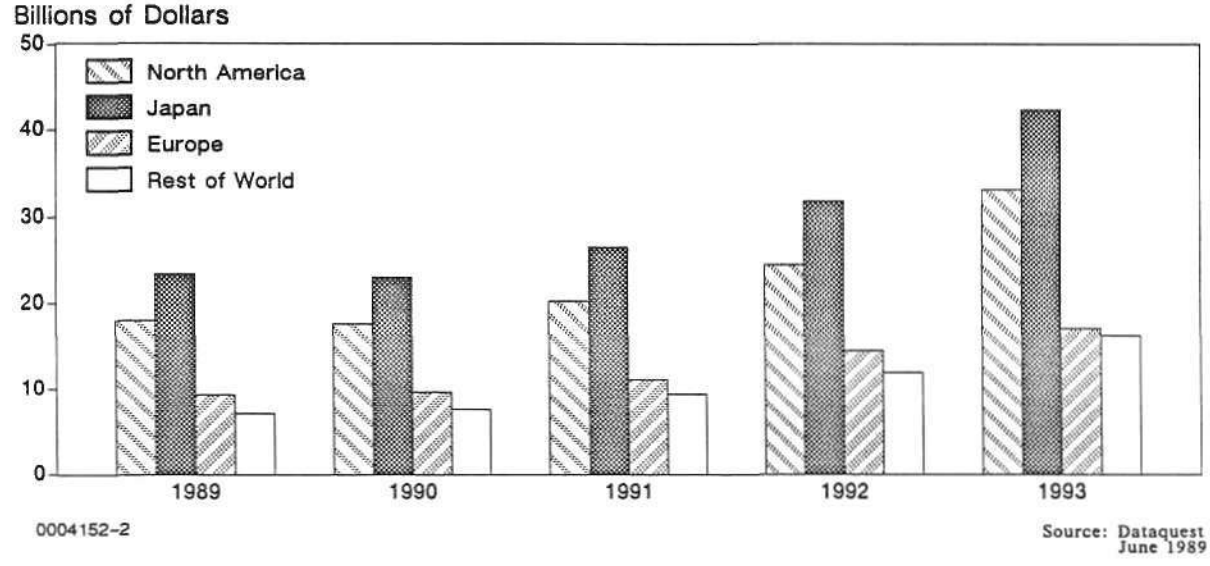


Figure 2

Worldwide Semiconductor Consumption
Merchant Market—Forecast



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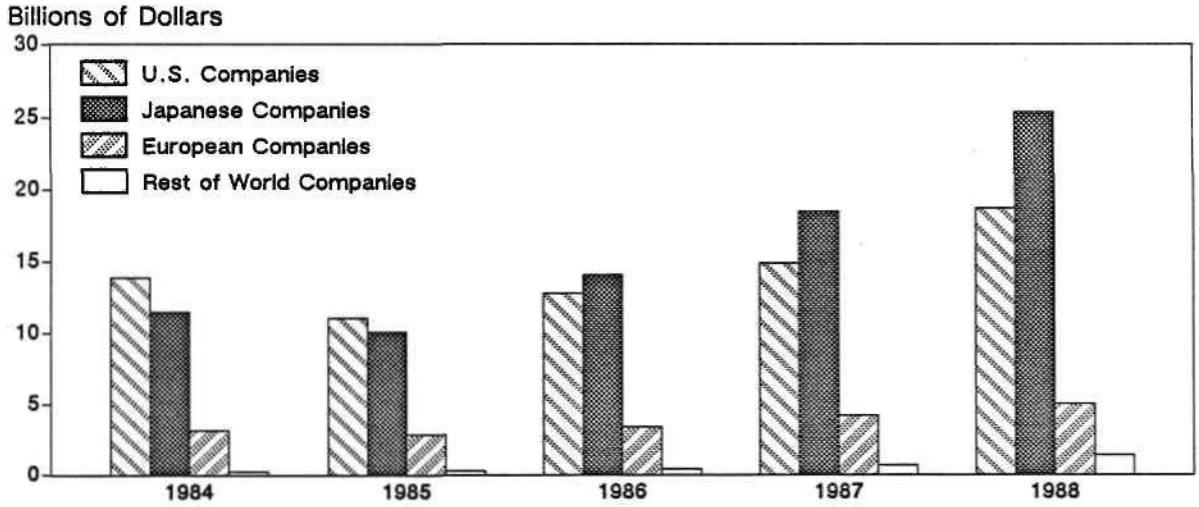
Semiconductor Consumption

Figure 3

Merchant Semiconductor Company Sales Worldwide—Historical

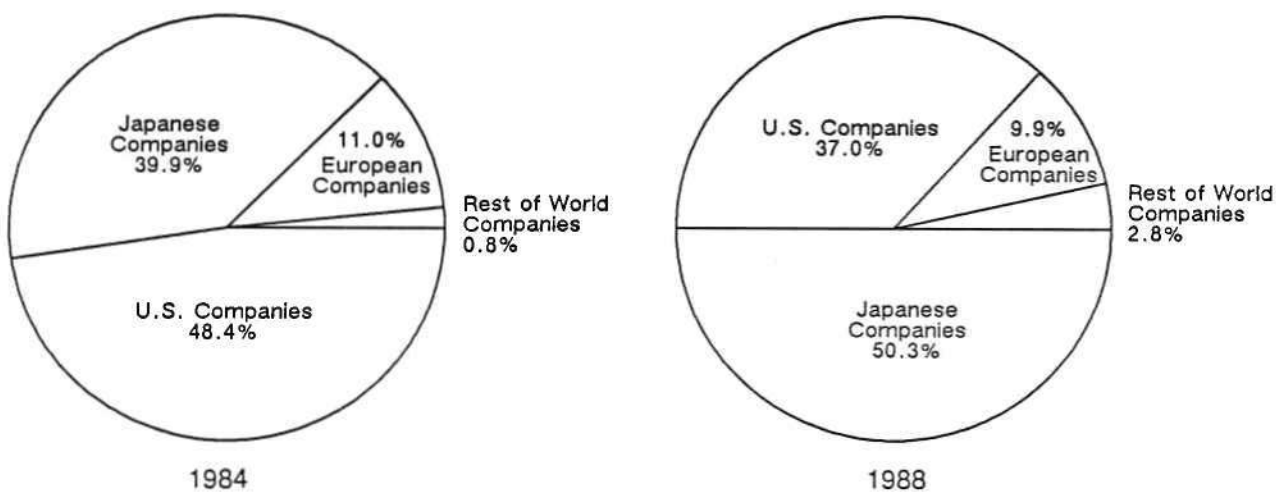


0004152-3

Source: Dataquest June 1989

Figure 4

Merchant Semiconductor Company Sales Worldwide by Region



0004152-4

Source: Dataquest June 1989

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Semiconductor Production

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Semiconductor Production

INTRODUCTION

This section presents data on worldwide semiconductor production by region. Semiconductor production is defined by the place where the wafers are fabricated, and regional semiconductor production includes all production in the region including merchant and captive producers and all foreign producers. For instance, North American semiconductor production includes IBM and Delco fabs as well as Japanese and European fabs in the United States.

SEMICONDUCTOR PRODUCTION

Table 1 shows historical semiconductor production for the years 1984 through 1988, and Table 2 shows forecast production for the period from 1989 through 1993. Figures 1 and 2 illustrate the same data graphically. Figure 3 depicts the 10-year trend for regional production; it shows percent production by region in 1983 and the Dataquest forecast for 1993.

For more detailed information on semiconductor production, please refer to the "Capital Spending" section in the SEMS Semiconductor Manufacturing notebook.

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Semiconductor Production

Table 1

Worldwide Semiconductor Production by Region
Merchant and Captive—Historical
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
North America						
Merchant	$13,569	$10,412	$12,128	$14,115	$17,344	6.3%
Captive	2,027	2,243	2,327	2,596	2,945	9.8%
Total North America	$15,596	$12,654	$14,456	$16,711	$20,289	6.8%
Japan						
Merchant	$11,872	$10,499	$14,524	$18,777	$25,698	21.3%
Captive	135	151	162	180	205	10.9%
Total Japan	$12,007	$10,651	$14,686	$18,958	$25,903	21.2%
Europe						
Merchant	$ 3,034	$ 3,024	$ 3,426	$ 4,298	$ 5,576	16.4%
Captive	338	379	405	451	512	10.9%
Total Europe	$ 3,373	$ 3,403	$ 3,831	$ 4,749	$ 6,088	15.9%
Rest of World (ROW)						
Merchant	$ 349	$ 406	$ 756	$ 1,088	$ 1,868	52.1%
Captive	0	0	0	0	0	N/A
Total ROW	$ 349	$ 406	$ 756	$ 1,088	$ 1,868	52.1%
Total Worldwide						
Merchant	$28,825	$24,341	$30,834	$38,278	$50,486	15.0%
Captive	2,501	2,773	2,894	3,227	3,662	10.0%
Total Production	$31,326	$27,114	$33,728	$41,505	$54,148	14.7%
Growth Rate	44.5%	(13.4%)	24.4%	23.1%	30.5%	

N/A = Not Applicable

Source: Dataquest
June 1989

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Table 2

Worldwide Semiconductor Production by Region
Merchant and Captive—Forecast
(Millions of Dollars)

	1989	1990	1991	1992	1993	CAGR 1989-1993
North America						
Merchant	$19,680	$19,338	$21,946	$27,203	$ 35,946	16.3%
Captive	3,591	4,081	4,435	4,905	6,078	14.1%
Total North America	$23,271	$23,418	$26,382	$32,108	$ 42,024	15.9%
Japan						
Merchant	$29,382	$28,208	$32,229	$38,929	$ 51,113	14.8%
Captive	250	284	308	341	423	14.1%
Total Japan	$29,632	$28,492	$32,537	$39,270	$ 51,536	14.8%
Europe						
Merchant	$ 6,747	$ 7,136	$ 8,866	$11,041	$ 14,310	20.7%
Captive	624	709	771	852	1,056	14.1%
Total Europe	$ 7,371	$ 7,845	$ 9,637	$11,894	$ 15,366	20.2%
Rest of World (ROW)						
Merchant	$ 2,395	$ 3,208	$ 4,419	$ 5,860	$ 7,992	35.2%
Captive	0	0	0	0	0	N/A
Total ROW	$ 2,395	$ 3,208	$ 4,419	$ 5,860	$ 7,992	35.2%
Total Worldwide						
Merchant	$58,204	$57,890	$67,460	$83,034	$109,360	17.1%
Captive	4,465	5,074	5,515	6,098	7,557	14.1%
Total Production	$62,669	$62,964	$72,975	$89,132	$116,917	16.9%
Growth Rate	15.7%	0.5%	15.9%	22.1%	31.2%	

N/A = Not Applicable

Source: Dataquest
June 1989

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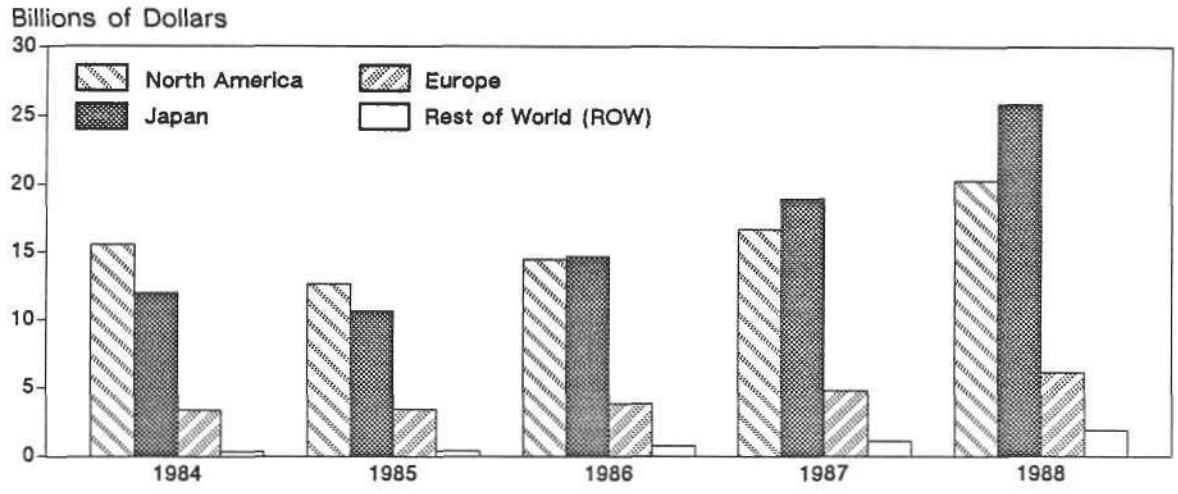
Semiconductor Production

Figure 1

Worldwide Semiconductor Production
Merchant and Captive—Historical



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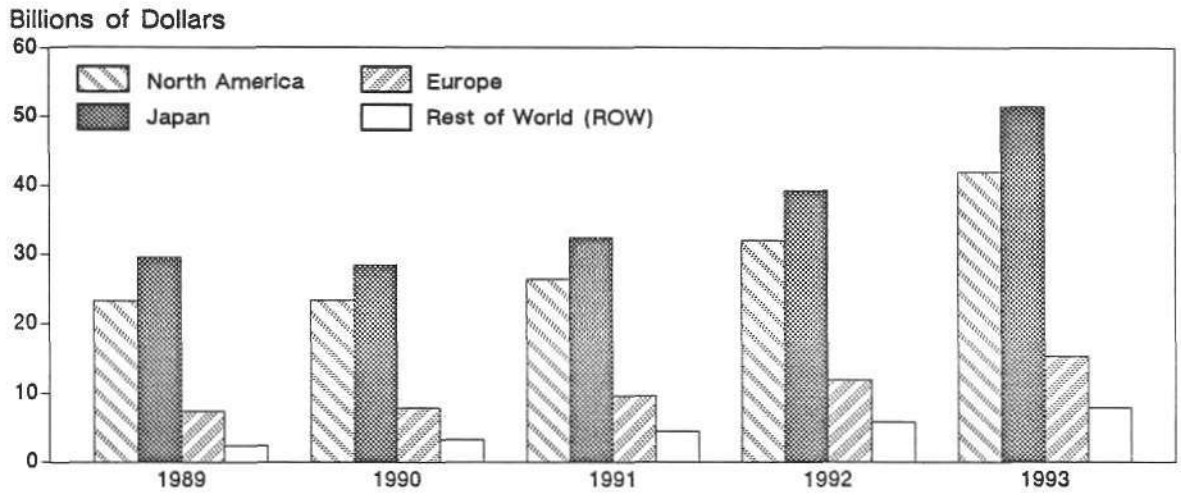
Source: Dataquest
June 1989

Figure 2

Worldwide Semiconductor Production
Merchant and Captive—Forecast



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Source: Dataquest
June 1989

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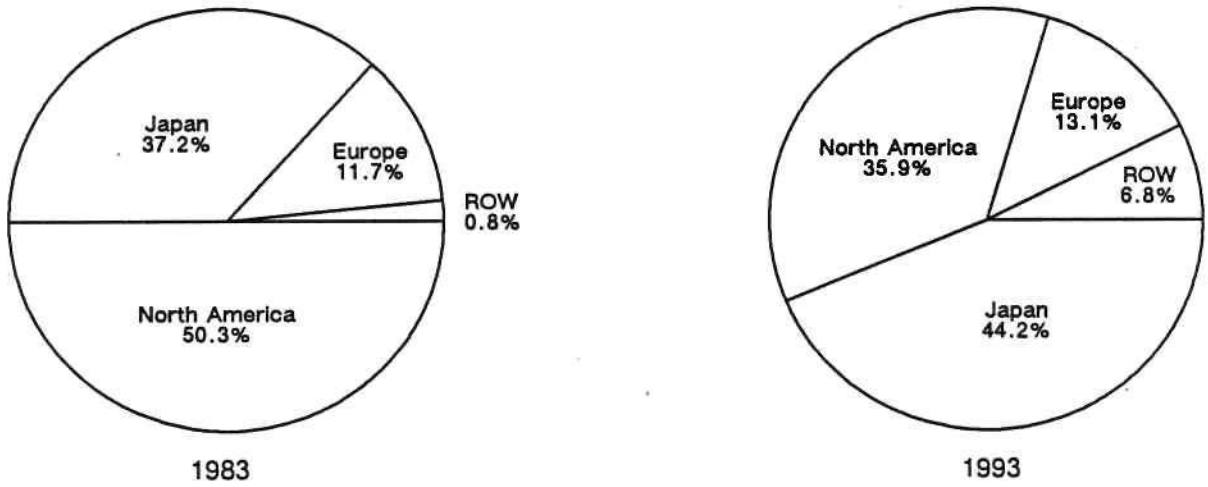
Figure 3

Worldwide Semiconductor Production
Merchant and Captive
Regional Share



0004151-3

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Wafer Fabrication Equipment Forecast

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Wafer Fabrication Equipment Forecast

INTRODUCTION

This section provides the Semiconductor Equipment and Materials Service (SEMS) forecast for wafer fabrication equipment. It includes all capital equipment used in the front-end manufacture of silicon and gallium arsenide semiconductor devices. The wafer fabrication equipment forecast is derived from the SEMS semiannual capital spending forecast and is updated in conjunction with that forecast.

This latest version of the equipment forecast is based on the capital spending forecast published in October 1987 just before the stock market debacle. (For details on the capital spending forecast, please refer to the SEMS newsletter code 1987-23: "The Next Five Years: Sustained Capital Spending Growth.") Dataquest has been assessing the impact of the crash on the semiconductor device and equipment industries. However, it is not yet clear what impact, if any, the crash will have on these industries. The capital spending plans of semiconductor manufacturers have not changed since the crash, and some companies have even increased their spending plans. All of the companies contacted by Dataquest, however, have reported that they are watching developments closely, and that they are prepared to cut their spending plans if necessary.

Therefore, the wafer fab equipment forecast presented here assumes that the crash will have no near-term impact on the equipment industry. Evidence is gathering to support this assumption as the equipment market is beginning to heat up, particularly in Japan, where the mood at SEMICON/Japan, held in December 1987, was definitely one of upsurge and optimism. Nevertheless, a note of caution must be inserted, and SEMS presented the downside risk in the SEMs newsletter code 1987-27: "Stock Market Crash Lowers Level of Optimism." In this newsletter, downside estimates of semiconductor production and capital spending are presented as an alternate scenario.

SEMICONDUCTOR PRODUCTION AND CAPITAL SPENDING

Table 1 shows worldwide semiconductor production and capital spending by merchant and captive semiconductor manufacturers for 1982 through 1987. Note that from 1982 through 1984, semiconductor production grew by a factor of 1.8, while capital spending grew by a factor of 2.8. This, in essence, was the main cause for the ensuing industry recession as the world semiconductor manufacturers added too much capacity in too few years. Semiconductor production and capital spending both peaked in 1984, and then fell off as a result of the recession.

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Wafer Fabrication Equipment Forecast

Table 1 also shows that the semiconductor industry has definitely pulled out of its recession. Semiconductor production in 1987 was already well above the peak of 1984, and profits were returning to the industry. The equipment industry, however, has not been so fortunate. Capital spending in 1987 was well below the 1984 peak of $8,517 million. As indicated in Table 2, which shows spending data for 1988 through 1992, it will not exceed 1984 levels until 1990. Except for a few companies, profits have not returned to the capital equipment industry and, in fact, 1987 was a year of red ink for the industry.

Nevertheless, closer inspection of Table 2 reveals some good news for the equipment industry. Although semiconductor production is expected to grow at a modest compound annual growth rate (CAGR) of 12.5 percent from 1988 through 1992, capital spending is expected to grow at a CAGR of 20.2 percent over the same period. After the incredible surge in capital spending from 1982 through 1984, capital spending fell off during the recession as the semiconductor manufacturers begin to use up the excess capacity. However, they must now step up their rate of spending to add capacity to meet the expected 12.5 percent growth in the world's demand for semiconductor devices.

Basically, the industry underinvested in the recession and now it must make up for that underinvestment if the projected demand in semiconductor devices is to be met. Table 3 shows the long-term growth rates over the ten-year period from 1983 through 1992. This period includes both industry peaks and valleys, but, as Table 3 indicates, the long-term growth rates for semiconductor production and capital spending are essentially the same.

Capital spending includes expenditures for wafer fabrication (front-end) equipment, assembly and test (back-end) equipment, and property and plant. Historical and forecast expenditures for wafer fab equipment are also shown in Tables 1 to 3. As Table 2 shows, year-to-year growth in wafer fab equipment expenditures will average about 25 percent in the period from 1988 through 1992 with the exception of 1989. In 1987, the wafer fab equipment market was $2,725 million; it is expected to be $7,120 million by 1992. This is very healthy growth.

Figure 1 graphically depicts the ten-year growth pattern for semiconductor production and wafer fab equipment expenditures. The ten-year interval shows industry overinvestment followed by underinvestment, then a period of good growth from 1988 through 1992.

Wafer Fabrication Equipment Forecast

Table 1

Worldwide Semiconductor Production and Capital Spending 1982–1987 (Millions of Dollars)

	1982	1983	1984	1985	1986	1987	CAGR 1982-1987
Semiconductor Production*	18,459	23,242	33,464	29,698	36,431	44,508	19.3%
Capital Spending	2,994	4,133	8,517	7,375	5,389	5,924	14.6%
Wafer Fabrication Equipment	1,416	2,127	3,530	3,341	2,598	2,725	14.0%
Percentage Growth		50.2%	66.0%	(5.3%)	(22.2%)	4.9%	

*Semiconductor production includes worldwide merchant and captive production.

Table 2

Estimated Worldwide Semiconductor Production and Capital Spending 1988–1992 (Millions of Dollars)

	1988	1989	1990	1991	1992	CAGR 1988-1992
Semiconductor Production*	54,723	55,332	62,865	73,488	87,778	12.5%
Capital Spending	7,722	7,889	9,897	12,564	16,122	20.2%
Wafer Fabrication Equipment	3,419	3,591	4,459	5,622	7,120	20.1%
Percentage Growth	25.5%	5.0%	24.2%	26.1%	26.6%	

*Semiconductor production includes worldwide merchant and captive production.

Source: Dataquest
January 1988

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Table 3

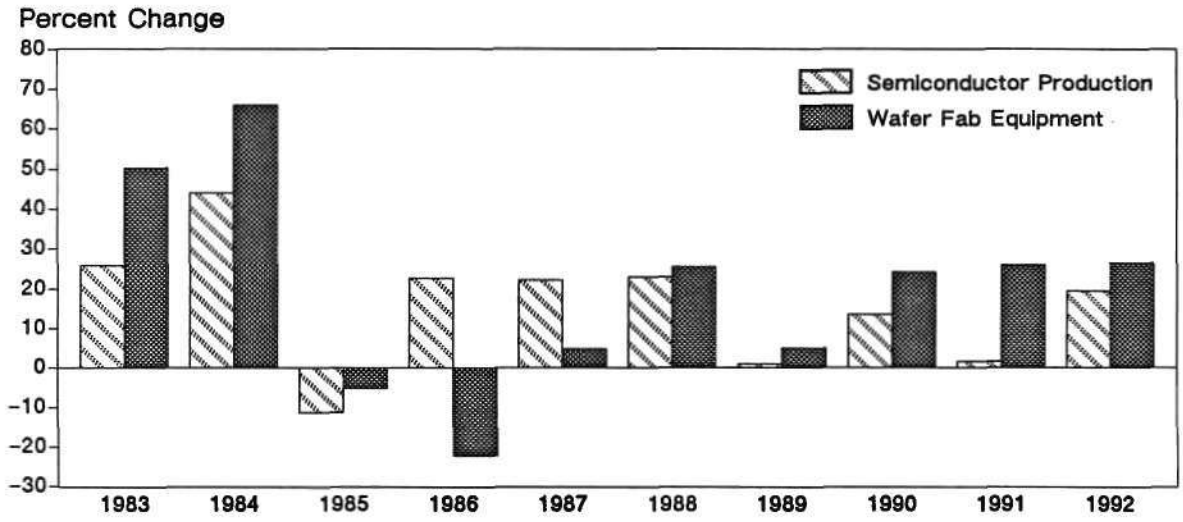
Ten–Year Compound Annual Growth Rates
1983–1992

	CAGR 1983-1992
Semiconductor Production	16.9%
Capital Spending	18.3%
Wafer Fab Equipment	17.5%

Source: Dataquest
January 1988

Figure 1

Semiconductor Production and Wafer Fab Equipment
Ten–Year Growth Pattern
1983–1992



Source: Dataquest
January 1988

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Wafer Fabrication Equipment Forecast

WAFER FABRICATION EQUIPMENT—HISTORY AND FORECAST

Table 4 gives the historical detail on the worldwide wafer fabrication equipment market from 1982 through 1987. The table includes the total front-end spending by the world's merchant and captive semiconductor manufacturers. Front-end equipment is divided into ten major categories: eight wafer fabrication equipment categories that are directly related to the wafer fabrication process and two categories that are nonprocess related. Table 5 gives the same detail, but for the forecast period of 1988 through 1992. The following sections describe the categories along with brief explanations about the forecasts.

Lithography

Lithography includes proximity and contact aligners, scanning projection aligners, steppers (reduction and 1:1), E-beam systems for direct-write and maskmaking, and X-ray aligners. Optical pattern generators and photorepeaters used in maskmaking are not included.

The total lithography market is expected to grow from $667 million in 1987 to $1,749 million in 1992 for a CAGR of 21.3 percent. Over this period, the market for proximity/contact aligners will be flat at about $30 million, while the market for projection aligners is expected to grow 5.2 percent, reaching $200 million by 1992. Because of the low growth rate, projection aligners are expected to account for only 11.0 percent of the lithography market by 1992 as compared with a 23.0 percent share of the market in 1987. However, the advent of step-and-scan projection aligners could increase the growth rate and lithography share if this technology is successful in stemming the shift to all-stepper fabs.

Steppers, which are the largest single equipment segment in the front-end equipment market, will grow from $365 million in 1987 to $1,179 million for a CAGR of 26.4 percent, which is above the total lithography market growth rate of 21.3 percent. Steppers will increase their share of the lithography market primarily because of the shift to all-stepper fabs. They will be the dominant lithography tool and will account for a 67.0 percent share of the total lithography market in 1992, as compared to a 55.0 percent share in 1987.

Key recent developments in steppers include advanced g-line and i-line submicron lenses, variable aperture lenses, and the introduction of the excimer laser stepper. Although the market for excimer laser steppers is still in the future and the steppers themselves need further development in the area of lenses and excimer laser sources, the industry feels confident that excimer laser steppers will be used to push optical lithography technology to below 0.5 micron.

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Wafer Fabrication Equipment Forecast

Table 4

Worldwide Wafer Fab Equipment Market History (Millions of Dollars)

	1982	1983	1984	1985	1986	1987	CAGR 1982-1987
World Fab Equipment Market	$1,416	$2,127	$3,530	$3,341	$2,598	$2,725	14.0%
Lithography							
Proximity/Contact	45	42	66	49	31	30	(7.8%)
Projection Aligners	123	161	244	274	191	155	4.8%
Steppers	139	297	552	468	314	365	21.2%
Direct-Write E-Beam	16	22	30	34	68	50	25.4%
Maskmaking E-Beam	37	46	61	82	57	63	11.0%
X-Ray	0	0	2	2	1	4	N/A
Total Lithography	361	567	954	909	661	667	13.1%
Automatic Photoresist Processing Equipment	77	100	185	166	144	133	11.8%
Etch and Clean							
Wet Process	68	95	132	105	83	91	6.0%
Dry Strip	20	34	45	37	32	36	13.0%
Dry Etch	93	185	314	298	236	250	21.8%
Ion Milling	6	6	8	7	7	7	2.8%
Total Etch and Clean	187	320	499	446	358	384	15.5%
Deposition							
Chemical Vapor Deposition	92	150	226	225	185	200	16.9%
Physical Vapor Deposition	131	155	236	268	245	270	15.6%
Silicon Epitaxy	47	65	112	72	49	55	3.2%
Metalorganic CVD	2	8	16	25	30	35	72.4%
Molecular Beam Epitaxy	22	37	47	60	74	81	29.7%
Total Deposition	294	414	637	650	584	641	16.9%
Diffusion	105	122	199	212	166	160	8.7%
Rapid Thermal Processing	2	4	10	14	16	20	54.1%
Ion Implantation							
Medium Current	57	83	118	132	56	54	(1.1%)
High Current	54	90	167	171	58	71	5.7%
High Voltage	1	1	1	2	15	18	97.4%
Total Implantation	111	174	286	306	129	143	5.1%
Process Control	205	296	509	423	374	400	14.3%
Factory Automation	25	55	125	100	76	82	26.8%
Other Equipment	50	75	125	118	92	95	13.9%
Total World Fab Equipment Market	$1,416	$2,127	$3,530	$3,341	$2,598	$2,725	14.0%
Percentage Growth		50.2%	66.0%	(5.3%)	(22.2%)	4.9%	

N/A = Not Applicable

Source: Dataquest January 1988

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Wafer Fabrication Equipment Forecast

Table 5

Worldwide Wafer Fab Equipment Market Forecast (Millions of Dollars)

	1987	1988	1989	1990	1991	1992	CAGR 1987-1992
World Fab Equipment Market	$2,725	$3,419	$3,591	$4,459	$5,622	$7,120	21.2%
Lithography							
Proximity/Contact	30	30	30	30	31	32	1.3%
Projection Aligners	155	165	165	175	185	200	5.2%
Steppers	365	471	511	673	890	1,179	26.4%
Direct-Write E-Beam	50	60	65	80	100	120	19.1%
Maskmaking E-Beam	63	75	86	98	124	158	20.2%
X-Ray	4	10	20	30	45	60	71.9%
Total Lithography	667	811	877	1,086	1,375	1,749	21.3%
Automatic Photoresist Processing Equipment	133	162	175	217	275	350	21.3%
Etch and Clean							
Wet Process	91	115	115	140	170	205	17.6%
Dry Strip	36	48	55	75	97	130	29.3%
Dry Etch	250	325	335	425	550	710	23.2%
Ion Milling	7	8	9	10	11	12	11.4%
Total Etch and Clean	384	496	514	650	828	1,057	22.4%
Deposition							
Chemical Vapor Deposition	200	265	270	340	430	555	22.6%
Physical Vapor Deposition	270	355	365	460	590	750	22.7%
Silicon Epitaxy	55	70	73	93	120	150	22.2%
Metalorganic CVD	35	42	50	60	75	95	22.1%
Molecular Beam Epitaxy	81	97	108	125	145	165	15.3%
Total Deposition	641	829	866	1,078	1,360	1,715	21.8%
Diffusion	160	170	170	180	190	205	5.1%
Rapid Thermal Processing	20	28	35	48	65	90	35.1%
Ion Implantation							
Medium Current	54	64	64	87	113	147	22.2%
High Current	71	99	99	128	167	209	24.1%
High Voltage	18	25	27	35	49	69	30.8%
Total Implantation	143	188	190	250	329	425	24.3%
Process Control	400	510	515	645	820	1,050	21.3%
Factory Automation	82	105	124	150	185	230	22.9%
Other Equipment	95	120	125	155	195	249	21.3%
Total World Fab Equipment Market	$2,725	$3,419	$3,591	$4,459	$5,622	$7,120	21.2%
Percentage Growth	4.9%	25.5%	5.0%	24.2%	26.1%	26.6%	

Source: Dataquest
January 1988

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In the E-beam area, applications for direct-write include quick-turn prototyping, submicron silicon and gallium arsenide devices, and low-volume ASIC devices. However, it is expected that these will only be small niche markets, and that direct-write E-beam will not be a dominant technology, reaching only $120 million by 1992. Low throughput is the main obstacle for E-beam market growth; however, very high throughput E-beam machines are being developed that could change the upside prognosis for direct-write. On the downside, these niches are themselves being threatened by the rise of alternate technologies. Also to be considered is the opinion of some industry experts who predict the production use of direct-write in an optical mix-and-match strategy in lieu of X-ray lithography. Thus, the future of direct-write E-beam is still not clear.

Also not clear is the prognosis for X-ray lithography, which is expected to reach $60 million by 1992. The X-ray market can be divided into nonsynchrotron-source and synchrotron-source technologies. The advent of excimer laser steppers appears to have extended the life of optical technology and to have pushed out, once again, the market window for nonsynchrotron-source X-ray lithography, although within the last year an advanced high-brightness X-ray system has been introduced for 0.5-micron and below lithography. Thus, it is still not clear what production lithography tool will be used in the 0.5-micron and below region.

Worldwide development of synchrotron sources is increasing. Besides the activity in West Germany, Japan, and IBM's effort at Brookhaven, there is activity in Italy, France, and at other locations in the United States. The Japanese are making huge investments in synchrotron-source research, and have more than 10 separate projects under way. Clearly, the Japanese will be well positioned if this technology becomes a production reality in the 1990s.

Automatic Photoresist Processing Equipment

Track equipment, as this equipment is usually called, includes wafer clean/bake, wafer prime, coat/bake, develop/bake, and resist stabilization equipment. The track market is expected to grow from $133 million in 1987 to $350 million in 1992, and as it is closely tied to the lithography market it has the same five-year CAGR of 21.3 percent. Track equipment has a lot of moving parts and has been a source of contamination in the past. The main concern in this market is to increase device yields by providing equipment that will reduce machine-induced contamination. Accordingly, new-generation beltless equipment is making its appearance. Other major goals are to reduce footprint and to improve photoresist process control and repeatablilty, and we can expect new equipment features to accomplish this.

Wafer Fabrication Equipment Forecast

Etch and Clean

This segment comprises wet process, dry strip, dry etch, and ion milling equipment. Wet processing includes wet etching and wet cleaning equipment including immersion benches, rinsers/dryers, spray processors, and ultrasonic cleaners. Even with the continued growth in dry processing, there will always be a need for some wet processing in the fab. Because cleanliness and better process uniformity are universal goals in VLSI device fabrication, manufacturers are introducing sophisticated wet process stations that are fully equipped with robotics. Chemical reprocessors for wet stations are also being introduced. These systems will reduce contamination, chemical costs, and environmental impact. Wet process has entered the high-technology world. The wet process market is expected to reach $205 million by 1992 for a CAGR of 17.6 percent over the five-year period.

Dry strip comprises barrel strippers and single wafer strippers. This market is expected to reach $130 million in 1992 for a five-year 29.3 percent CAGR, which is higher than the average CAGR for all front-end equipment. Barrel strippers have been the dominant method for removing resists, but have not been effective in removing the tenacious resists that remain after reactive ion etch or high-current implant processes. Thus, there is a growing need for single-wafer strippers that can effectively remove these resists. Single-wafer systems with high power dissipation tend to drive the residual sodium in the resist into the wafer. This causes threshold voltage degradation and C-V shifts. Thus, the market will be driven by the higher-price, low-voltage downstream plasma systems that minimize the problems associated with high plasma voltages.

The dry etch market, which continues to be active, peaked at $314 million in 1984. Dry etch will be one of the few front-end equipment segments to exceed 1984 levels as early as 1988. It will reach $710 million by 1992 for an above-average CAGR of 23.2 percent over the forecast period. High-pressure plasma and low-pressure reactive ion etch systems have been keeping pace. However, advanced devices with high aspect ratios impose severe restrictions on the dry etch systems being developed, and we expect that batch processes will be favored until a high-throughput, single wafer etcher of triode or magnetron design is developed.

Deposition

Three major technologies are included in this category: chemical vapor deposition (CVD), physical vapor deposition (PVD), and epitaxy.

CVD equipment includes atmospheric-pressure CVD (APCVD), plasma-enhanced CVD (PECVD), and low-pressure CVD (LPCVD) techniques. The CVD market continues to be an area of intense activity as CVD technology advances to meet the needs of leading-edge ICs. Still more new equipment of this type was introduced in 1987, and competition in advanced CVD equipment is heating up. Emphasis is on new and improved thin-film processes and reduction of particulates. Historically, the CVD market was split into APCVD, PECVD, and LPCVD technologies since each had its own applications. Now, because of the advanced reactors that are crossing application boundaries, it makes more sense to divide the market by film application rather than by equipment technology.

The CVD market is expected to grow from $200 million in 1987 to $555 million by 1992 for a CAGR of 22.6 percent.

PVD includes sputtering and evaporation. In sputtering, the most notable activity is in the area of aluminum planarization, which is being developed to overcome the topographical problems associated with micron and submicron geometries. Sputtered aluminum will continue to be used, at least in the foreseeable future, as CVD aluminum has not become a reality. In addition, integrated vacuum systems that combine several processing technologies are beginning to appear in the marketplace. These integrated systems will combine sputtering, CVD, etch, and rapid thermal processing into one piece of equipment.

Evaporation, which accounts for less than 20 percent of the PVD market, is used almost exclusively for the aluminum lift-off process in gallium arsenide device manufacture. It is expected that evaporation as a percentage of the total PVD market will decline in the future as sputtered aluminum applications grow faster than gallium arsenide applications.

The PVD market is expected to grow from $270 million in 1987 to $750 million in 1992 for a CAGR of 22.7 percent. In last year's forecast, we said that the CVD market might grow to be larger than the PVD market; however, we do not expect this to happen over the next five years. We now expect that in 1992 the CVD market will be $555 million compared to $750 million for PVD.

The epitaxy market includes silicon epitaxy, metalorganic CVD (MOCVD), and molecular beam epitaxy (MBE). While silicon epitaxy has been making its way into MOS processing, the cost has been prohibitive for all but the most exotic devices. With the recent development of new-generation epitaxy systems that lower the cost of epi layers, it is expected that silicon epitaxy will be used in production of 4-Mbit DRAMs.

Approximately 70 percent of the total 1987 epitaxial market of $171 million was due to MOCVD and MBE equipment. MOCVD equipment, a newer technology, is growing at a faster rate than MBE equipment. By 1992, the total epitaxy market is expected to reach $410 million for a CAGR of 19.1 percent.

The total deposition market is expected to grow from $641 million in 1987 to $1,715 million in 1992. The deposition and lithography markets are the largest of the front-end equipment markets and will be essentially equal to each other each year over the 1987 through 1992 time period. None of the other eight categories of front-end equipment approach these two markets in terms of market size.

Diffusion

The diffusion market peaked in 1985 at $212 million, but is not expected to reach this level again until 1992 when the market is forecast to be $205 million. The five-year CAGR for diffusion furnaces is expected to be only about 5 percent. Nevertheless, this is more optimistic than last year's forecast. The main reason for the more optimistic forecast is that rapid thermal processing is not yet replacing traditional diffusion furnace applications in production.

The low growth in this market was caused by the shift toward film deposition in dedicated CVD reactors and the increased use of ion implantation for devices in which the doping profile needs to be tightly controlled.

Recent developments in diffusion furnace equipment, both horizontal and vertical tube, have focused on robotic wafer handling and software automation as the trend toward larger wafers makes operator handling of the large wafer loads impractical. Contamination also is being addressed and the load stations of the furnaces are now in a Class 10 environment.

In contrast to the United States, the market for vertical diffusion furnaces is beginning to emerge in Japan. At the recent SEMICON/Japan show held in December 1987, there were eight Japanese equipment vendors exhibiting vertical furnace systems compared to only one U.S. exhibitor. The Japanese believe that in two or three years only vertical furnaces will be used in new wafer fabs. They cite as advantages for vertical furnaces the minimization of oxygen draw-in, which results in higher-quality gate oxides, and better contamination control.

Rapid Thermal Processing (RTP)

The RTP market can be subdivided into two broad applications: machines specifically designed for new applications and machines intended to replace the more traditional diffusion furnace applications. In the first case, manufacturers are introducing application-specific equipment in an attempt to broaden the RTP market. Low-temperature machines for contact alloying and systems for the deposition of thin gate oxides are examples of such application-specific equipment.

In the second case, semiconductor manufacturers are not yet buying RTP systems in lieu of diffusion furnaces, which is the reason that the RTP market has not yet shown the expected high growth. However, Dataquest believes that RTP will eventually replace some diffusion furnace applications, particularly as the RTP manufacturers introduce more production-worthy and cost-effective machines. This will accelerate growth and allow the RTP market to reach $90 million by 1992.

Ion Implantation

This market includes medium-current (less than 2mA, less than 200 keV), high-current (greater than 2mA, less than 200 keV), and high-voltage (greater than 200 keV) implanters. The total market is expected to grow from $143 million in 1987 to $425 million in 1992 for a five-year CAGR of 24.3 percent. Although this seems like excellent growth prospects, it should be noted that this market is coming from a very depressed state. The market reached its highest level, $306 million, in 1985, but declined precipitately to $129 million in 1986 because of the excess production capacity. The implanter market actually suffered more than any other front-end equipment segment in the recession, and it is not expected to exceed the 1985 sales level until 1991.

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We believe that there has been a fundamental shift in the way semiconductor manufacturers use implanters. Historically, semiconductor manufacturers tended to dedicate implanters to specific processes in order to simplify operation and to prevent possible cross-contamination of species. Because implanters are expensive and underutilized, there is an incentive to increase their productivity; hence, we expect that implanters will absorb a smaller percentage of the capital spending dollar than in the past. In the peak years of 1984 and 1985, implanter sales represented between 8 and 9 percent of the spending on front-end equipment, but they are expected to account for only 5 or 6 percent over the forecast period.

The medium-current implanter market is expected to grow a little less than the high-current implanter market. Even though low-dose applications will increase slightly faster than high-dose applications, more low-dose applications will be done on high-current implanters than in the past. High-voltage systems will began to find their way into production as 4-Mbit DRAM processes become better understood. High-voltage systems will be used on devices with geometries of less than 0.8 micron and will be used for the formation of retrograde wells and for field isolation in both bipolar and MOS devices.

Process Control

Process control is a broad category that includes equipment for mask and wafer inspection, process monitoring, surface analysis, and analytical quality control. The market is expected to exceed $1 billion in 1992, but it is a highly fragmented market, with dozens of companies selling into many noncompetitive niches.

While some process control equipment segments are mature, slow-growth markets, the automated metrology and wafer inspection areas are expected to experience healthy growth over the next five years. In today's semiconductor industry, line geometries are shrinking, while device complexity, processing steps, wafer size, and mask levels continue to increase.

In response to demands for faster measurements with greater resolution capability, new generations of tools are being developed to meet the requirements of advanced device processing technology. Wafer inspection currently is making a transition from operator-intensive inspection and measurement systems to fully automated tools as the semiconductor industry seeks to overcome the limitations of the human operator. Accordingly, the price of wafer metrology and inspection systems has also increased and, in some cases, has reached the price of a wafer stepper at approximately $1 million.

As line geometries shrink past the resolution limits of traditional optical measurement systems, semiconductor manufacturers also face a variety of technological choices for critical dimension measurement systems. While European and U.S. semiconductor manufacturers are exploring the capability of the newly developed optical-based confocal scanning laser microscope systems, Japanese manufacturers have embraced in-process SEM (scanning electron microscope) tools for submicron linewidth measurements. Dataquest expects that over the next five years, other technologies, such as coherence probe imaging, will be introduced to meet the measurement resolution and throughput requirements of advanced semiconductor fabrication.

Factory Automation

The factory automation market includes computer-integrated manufacturing (CIM) system software for shop floor control; factory host computer systems; cell controllers and interface hardware; and wafer transport systems, including automatic guided vehicles (AGVs), robotics, and rail transport systems. The total market for this segment is expected to reach $230 million by 1992.

In general, the hope and hype of factory automation of the past several years has materialized into relatively few examples of fully automated manufacturing cells within the fab. During the recent recession, many semiconductor automation programs were scaled down, put on hold, or cancelled altogether. In response, software and robotics companies have opted to pursue automation markets outside the semiconductor industry (i.e., printed circuit boards, aerospace, pharmaceuticals) as a strategy for surviving the "boom-bust" business cycles of the semiconductor manufacturers. Future factory automation expenditures will likely remain conservative, with semiconductor manufacturers spending a fixed amount per facility per year to update and automate their manufacturing operations.

Other Equipment

This catch-all category includes various other types of capital equipment used throughout the fab but which do not readily fit into any of the previously discussed major areas of wafer processing. For example, this category includes decontamination systems, wafer markers, gas analyzers, storage systems, tube cleaners, and other similiar equipment that has diverse applications in the front end. We expect that collective expenditures for this category will grow directly as the front-end equipment market grows, and that it should account for 3 to 4 percent of front-end equipment spending, or about $249 million by 1992.

SUMMARY

This January 1988 five-year forecast for the year-to-year trend for the industry as a whole is fundamentally the same as the January 1987 five-year forecast. Last year, however, we expected the turnaround in the wafer fab equipment market to occur earlier than it actually did. Consequently, last year we predicted a 14 percent increase in 1987 spending for front-end equipment but it only increased about 5 percent. Last year we forecast strong growth for the 1988 through 1991 period, with the exception of low growth in 1989. A year later, there is no fundamental change to this outlook.

Indeed, our optimistic five-year forecast stands on even firmer ground this January. We believe that the semiconductor industry has assuredly emerged from its recession, the slack in capacity is being taken up, and new capacity has to be added to meet the world's voracious appetite for semiconductor devices.

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Capital Spending

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Capital Spending

INTRODUCTION

This section presents data on worldwide semiconductor capital spending by region. Capital spending in a region includes spending by all semiconductor producers in that region, including spending by merchant and captive producers as well as foreign producers. For instance, capital spending in North America includes spending by IBM, Delco, and Japanese and European semiconductor companies building wafer fabrication, assembly, and test facilities in the United States.

CAPITAL SPENDING FORECAST

Table 1 shows historical capital spending for the years 1984 through 1988, and Table 2 shows forecast spending for the period from 1989 through 1993. Figures 1 and 2 illustrate the same data graphically. Figure 3 depicts the 10-year trend for regional capital spending; it shows percent spending by region in 1983 and the Dataquest forecast for 1993.

For more detailed information on capital spending, please refer to the "Capital Spending" section in the SEMS Semiconductor Manufacturing notebook.

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Capital Spending

Table 1

Worldwide Capital Spending by Region
Merchant and Captive—Historical
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
North America						
Merchant	$3,068	$1,978	$1,438	$1,911	$ 2,569	(4.3%)
Captive	593	651	644	683	865	9.9%
Total North America	$3,661	$2,629	$2,082	$2,594	$ 3,434	(1.6%)
Japan						
Merchant	$3,860	$3,292	$1,800	$2,384	$ 4,508	4.0%
Captive	40	44	45	47	60	11.0%
Total Japan	$3,900	$3,336	$1,845	$2,432	$ 4,568	4.0%
Europe						
Merchant	$ 717	$ 690	$ 653	$ 757	$ 874	5.1%
Captive	99	110	$ 112	$ 119	$ 150	11.0%
Total Europe	$ 816	$ 800	$ 765	$ 875	$ 1,025	5.8%
Rest of World (ROW)						
Merchant	$ 461	$ 534	$ 437	$ 534	$ 1,019	22.0%
Captive	0	0	0	0	0	N/A
Total ROW	$ 461	$ 534	$ 437	$ 534	$ 1,019	22.0%
Total Worldwide						
Merchant	$8,107	$6,493	$4,327	$5,586	$ 8,971	2.6%
Captive	731	805	801	849	1,076	10.1%
Total Capital Spending	$8,838	$7,299	$5,129	$6,435	$10,046	3.3%
Growth Rate	106.4%	(17.4%)	(29.7%)	25.5%	56.1%	

N/A = Not Applicable

Source: Dataquest
June 1989

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Capital Spending

Table 2

Worldwide Capital Spending by Region
Merchant and Captive—Forecast
(Millions of Dollars)

	1989	1990	1991	1992	1993	CAGR 1989-1993
North America						
Merchant	$ 2,848	$ 2,759	$ 3,455	$ 4,628	$ 6,214	19.3%
Captive	978	1,080	1,164	1,374	1,649	13.8%
Total North America	$ 3,826	$ 3,839	$ 4,619	$ 6,002	$ 7,863	18.0%
Japan						
Merchant	$ 5,420	$ 4,897	$ 6,834	$ 9,343	$12,749	23.1%
Captive	68	75	81	95	115	13.8%
Total Japan	$ 5,488	$ 4,972	$ 6,915	$ 9,439	$12,864	23.0%
Europe						
Merchant	$ 1,080	$ 1,119	$ 1,482	$ 1,993	$ 2,633	24.7%
Captive	170	188	202	239	287	13.8%
Total Europe	$ 1,250	$ 1,307	$ 1,684	$ 2,231	2,920	23.3%
Rest of World (ROW)						
Merchant	$ 1,809	$ 1,810	$ 2,177	$ 2,391	$ 2,845	22.8%
Captive	0	0	0	0	0	N/A
Total ROW	$ 1,809	$ 1,810	$ 2,177	$ 2,391	$ 2,845	22.8%
Total Worldwide						
Merchant	$11,156	$10,584	$13,948	$18,355	$24,442	22.2%
Captive	1,217	1,343	1,447	1,708	2,050	13.8%
Total Capital Spending	$12,373	$11,927	$15,395	$20,063	$26,492	21.0%
Growth Rate	23.3%	(3.6%)	~~29.1%~~	~~30.3%~~	32.0%	

N/A = Not Applicable

Source: Dataquest
June 1989

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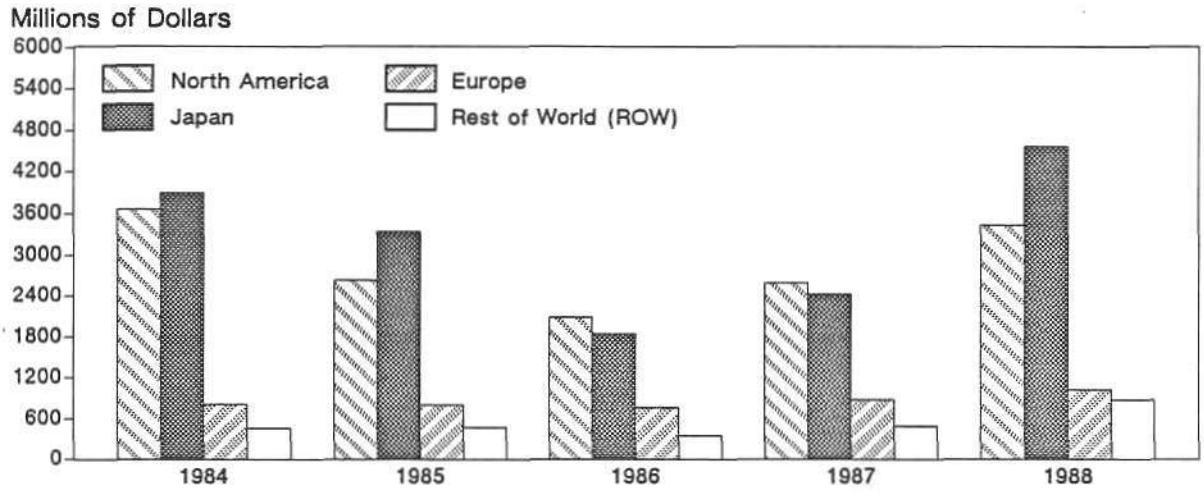
Capital Spending

Figure 1

Worldwide Capital Spending
Merchant and Captive—Historical
(Billions of Dollars)



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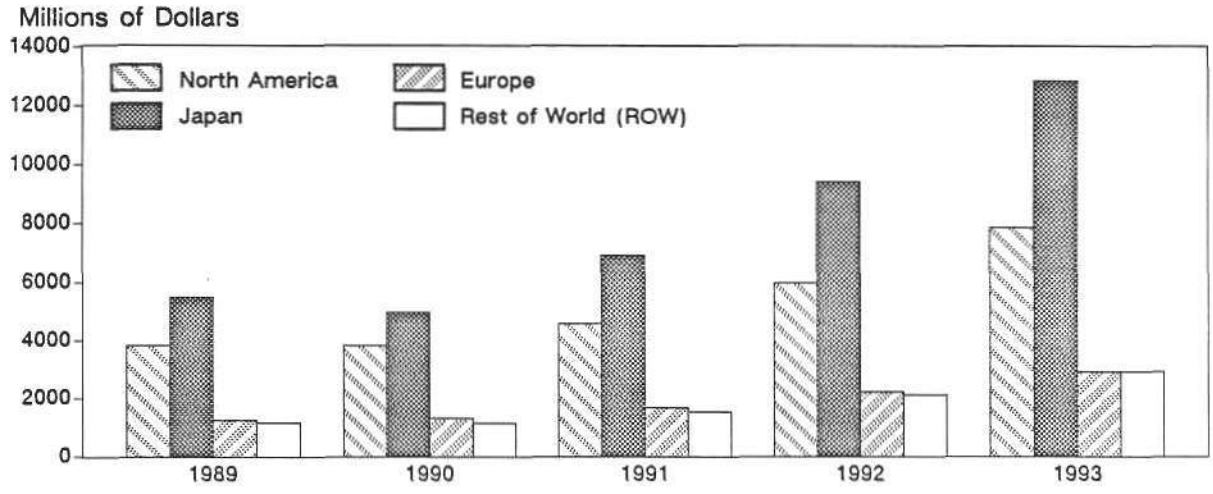
Source: Dataquest
June 1989

Figure 2

Worldwide Capital Spending
Merchant and Captive—Forecast
(Billions of Dollars)



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Source: Dataquest
June 1989

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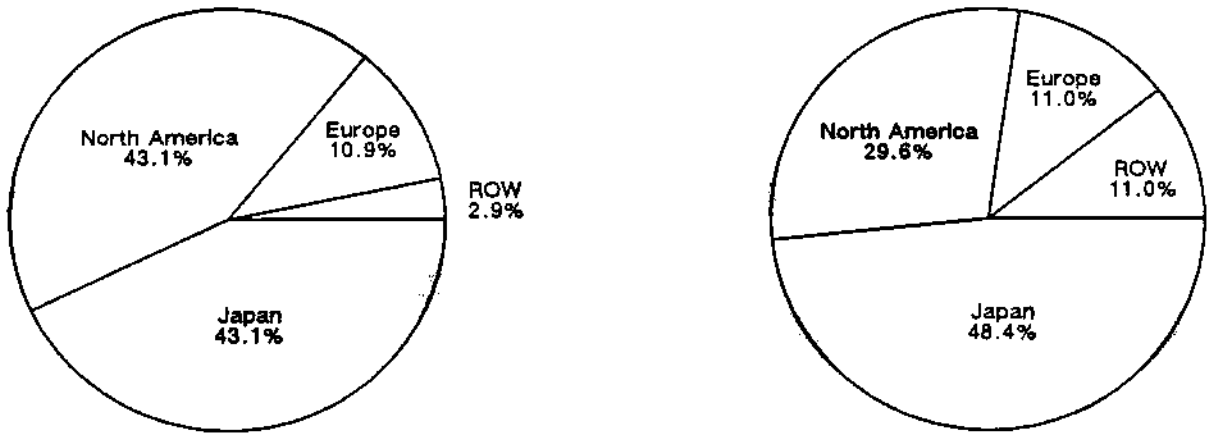
Capital Spending

Figure 3

Worldwide Capital Spending
Merchant and Captive
Regional Share



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Source: Dataquest
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Wafer Fabrication Equipment

INTRODUCTION

This section presents historical and forecast data on the worldwide wafer fabrication equipment market. Table 1 presents the historical data by equipment category for the years 1983 through 1987, and Table 2 shows forecast data by category for the years 1988 through 1992. Dataquest is now in the process of determining the actual data by category and company for 1988; when this task is completed, we will update Table 2.

PRODUCTION VERSUS SPENDING

Table 3 summarizes the historical worldwide semiconductor production, capital spending, and wafer fab equipment expenditures for the years 1982 through 1987. Table 4 presents Dataquest's forecast regarding these items for the years 1988 through 1992.

MARKET GROWTH

Figure 1 shows year-to-year growth for semiconductor production and wafer fab equipment for the 10-year period from 1983 through 1992. Table 5 shows the compound annual growth rate (CAGR) forecast for semiconductor production, capital spending, and wafer fab equipment.

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Wafer Fabrication Equipment

Table 1

Worldwide Wafer Fab Equipment Market
Historical
(Millions of Dollars)

	1983	1984	1985	1986	1987	CAGR 1983-1987
World Fab Equipment Market	2,139	3,518	3,357	2,697	3,138	10.1%
Lithography						
Proximity/Contact	43	67	48	31	25	(12.8%)
Projection Aligners	154	235	265	186	141	(2.0%)
Steppers	287	511	443	366	508	15.3%
Direct-Write E-Beam	24	29	31	68	67	30.0%
Maskmaking E-Beam	49	72	81	51	68	8.5%
X-Ray	0	2	2	1	0	N/A
Total Lithography	556	915	870	703	809	9.8%
Automatic Photoresist Processing Equipment	100	184	158	145	164	13.1%
Etch and Clean						
Wet Process	115	172	157	168	168	9.9%
Dry Strip	34	45	37	32	44	6.9%
Dry Etch	185	316	303	239	258	8.6%
Ion Milling	6	8	7	7	7	1.9%
Total Etch and Clean	341	540	503	445	477	8.8%
Deposition						
Chemical Vapor Dep.	151	226	223	194	251	13.5%
Physical Vapor Dep.	163	234	263	213	246	11.0%
Silicon Epitaxy	65	112	72	49	39	(12.2%)
Metalorganic CVD	8	18	25	32	36	44.8%
Molecular Beam Epitaxy	27	41	53	69	69	26.9%
Total Deposition	413	630	635	557	640	11.6%
Diffusion	122	191	206	157	163	7.5%
Rapid Thermal Processing	4	11	14	15	18	47.0%

(Continued)

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Table 1 (Continued)

Worldwide Wafer Fab Equipment Market
Historical
(Millions of Dollars)

	1983	1984	1985	1986	1987	CAGR 1983-1987
Ion Implantation						
Medium-Current	83	118	132	56	64	(6.2%)
High-Current	90	167	171	58	153	14.2%
High-Voltage	1	1	2	11	16	95.0%
Total Implantation	174	286	306	126	233	7.6%
CD/Wafer Inspection	40	63	55	71	94	23.9%
Other Process Control	256	446	368	303	332	6.7%
Factory Automation	58	130	125	81	99	14.3%
Other Equipment	75	123	118	94	108	9.6%
Total World Fab Equipment Market	2,139	3,518	3,357	2,697	3,138	10.1%
Growth	51.9%	64.5%	(4.6%)	(19.7%)	16.4%	

N/A = Not Applicable

Source: Dataquest
March 1989
Ref. equipfcs

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Wafer Fabrication Equipment

Table 2

Worldwide Wafer Fab Equipment Market
Forecast
(Millions of Dollars)

	1988	1989	1990	1991	1992	CAGR 1988-1992
World Fab Equipment Market	4,263	4,562	4,684	5,934	7,474	15.1%
Lithography						
Proximity/Contact	30	30	30	31	32	1.6%
Projection Aligners	160	170	170	215	270	14.0%
Steppers	800	850	820	1,050	1,300	12.9%
Direct-Write E-Beam	60	65	75	90	105	15.0%
Maskmaking E-Beam	82	99	100	129	160	18.2%
X-Ray	2	8	20	30	40	111.5%
Total Lithography	1,134	1,222	1,215	1,545	1,907	13.9%
Automatic Photoresist Processing Equipment	232	251	249	317	391	13.9%
Etch and Clean						
Wet Process	233	247	253	310	405	14.8%
Dry Strip	45	50	55	75	100	22.1%
Dry Etch	350	370	375	490	640	16.3%
Ion Milling	8	9	10	11	12	10.7%
Total Etch and Clean	636	676	693	886	1,157	16.1%
Deposition						
Chemical Vapor Dep.	380	380	400	530	680	15.7%
Physical Vapor Dep.	292	340	350	470	630	21.2%
Silicon Epitaxy	65	70	80	105	140	21.1%
Metalorganic CVD	43	52	62	74	90	20.3%
Molecular Beam Epitaxy	83	95	108	123	140	14.0%
Total Deposition	863	937	1,000	1,302	1,680	18.1%
Diffusion	205	210	210	245	285	8.6%
Rapid Thermal Processing	25	32	38	52	70	29.4%

(Continued)

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Table 2 (Continued)

Worldwide Wafer Fab Equipment Market
Forecast
(Millions of Dollars)

	1988	1989	1990	1991	1992	CAGR 1988-1992
Ion Implantation						
Medium-Current	73	80	83	106	137	17.0%
High-Current	221	230	229	299	378	14.4%
High-Voltage	21	35	38	50	75	37.5%
Total Implantation	315	345	350	455	590	17.0%
CD/Wafer Inspection	131	153	194	251	325	25.5%
Other Process Control	422	410	410	463	529	5.8%
Factory Automation	155	168	165	218	278	15.7%
Other Equipment	145	158	160	200	262	15.9%
Total World Fab Equipment Market	4,263	4,562	4,684	5,934	7,474	15.1%
Growth	36.1%	7.0%	2.7%	26.7%	26.0%	

Source: Dataquest
March 1989
Ref. equipfcs

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Table 3

Worldwide Semiconductor Production and Capital Spending
1982–1987
(Millions of Dollars)

	1982	1983	1984	1985	1986	1987	CAGR 1982-1987
Semiconductor Production*	17,102	21,681	31,326	27,113	33,728	41,635	19.5%
Capital Spending	2,899	4,283	8,838	7,231	5,039	6,136	16.2%
Wafer Fabrication Equipment	1,408	2,139	3,518	3,357	2,697	3,138	17.5%
Growth		51.9%	64.5%	(4.6%)	(19.7%)	16.4%	

*Semiconductor production includes worldwide merchant and captive production.

Source: Dataquest
March 1989

Table 4

Estimated Worldwide Semiconductor Production and Capital Spending
1988–1992
(Millions of Dollars)

	1988	1989	1990	1991	1992	CAGR 1988-1992
Semiconductor Production*	54,271	59,542	60,652	71,040	85,888	12.2%
Capital Spending	9,319	10,466	10,377	13,709	17,649	17.3%
Wafer Fabrication Equipment	4,263	4,652	4,684	5,934	7,474	15.1%
Growth	36.1%	7.0%	2.7%	26.7%	26.0%	

*Semiconductor production includes worldwide merchant and captive production.

Source: Dataquest
March 1989

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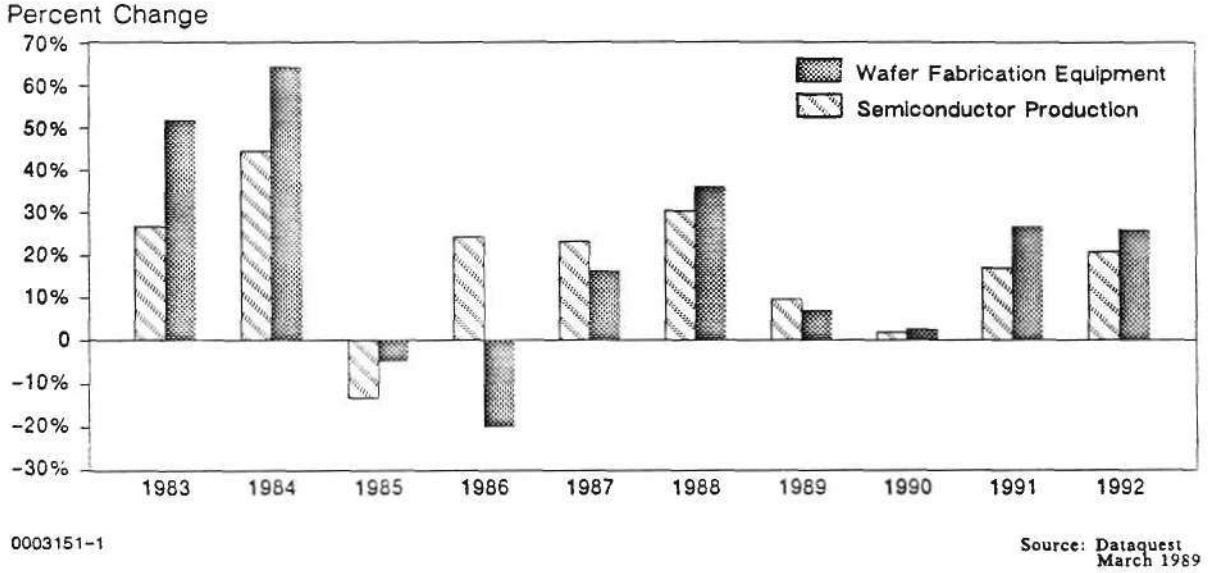
Figure 1

Semiconductor Production and Wafer Fab Equipment
Ten-Year Growth Pattern
1983-1992



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Source: Dataquest
March 1989

Table 5

Ten-Year Compound Annual Growth Rate
1982-1992

	CAGR 1982-1992
Semiconductor Production	17.5%
Capital Spending	19.8%
Wafer Fab Equipment	18.2%

Source: Dataquest
March 1989

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Wafer Fabrication Equipment Forecast

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DATAQUEST WORLDWIDE EQUIPMENT HISTORY

	1980	1981	1982	1983	1984	1985	CAGR(80-85)
LITHOGRAPHY	$288	$399	$371	$540	$945	~~$774~~ 753	21.9%
		38.5%	-7.0%	45.6%	75.1%	-18.1%	
PROXIMITY/CONTACT	~~$53~~ 211	~~$53~~ 143	~~$82~~ 244	~~$86~~ 174	~~$77~~ 167	~~$67~~ 106	4.7%
PROJECTION	$110	$164	$113	$114	$245	$187	11.1%
1X STEPPER	$0	$3	$12	$23	$59	$45	
REDUCTION STEPPER	$75	$139	$110	$249	$469	$358	36.7%
DIRECT-WRITE E-BEAM	$13	$12	$16	$22	$30	$30	17.3%
MASKMAKING E-BEAM	$37	$28	$38	$46	$63	$84	18.1%
X-RAY				$0	$2	$4	
ETCH	$96	$109	$154	$262	$484	~~$392~~ 460	32.5%
		13.5%	41.3%	70.1%	84.7%	-18.9%	
WET	$54	$55	$50	$54	~~$79~~ 96	$58	1.3%
BARREL	$30	$29	$26	$28	$44	$34	2.5%
PLANAR	$4	$17	$70	$166	$343	$284	134.6%
ION MILLING	$8	$8	$8	$14	$18	$16	15.4%
AUTOMATIC PHOTORESIST	$88	~~$72~~ 75	~~$67~~ 91	~~$90~~ 96	~~$157~~ 197	~~$121~~ 114	6.6%
		-18.2%	-6.9%	34.3%	74.4%	-23.0%	
DEPOSITION	$296	$312	$278	$382	$697	$559	13.6%
		5.4%	-10.9%	37.4%	82.5%	-19.8%	
CVD	$70	$80	~~$75~~ 105	~~$118~~ 147	~~$246~~ 245	$199	23.3%
PVD	$165	$153	$140	$178	$300	$239	7.7%
EPITAXY	$61	$79	$63	$86	$151	$121	14.7%
DOPING	$161	$180	$194	$305	$481	~~$382~~ 400	18.9%
		11.8%	7.8%	57.2%	57.7%	-20.6%	
FURNACES	$86	$93	$85	$128	~~$179~~ 215	~~$135~~	9.4%
ION IMPLANT	$75	$87	$109	$177	$302	$247	26.9%
Medium Current	$52	$59	$61	$95	$140	$118	17.9%
High Current	$22	$27	$46	$79	$157	$129	42.4%
High Voltage	$1	$1	$2	$3	$5	$5	38.0%
INSPECTION	$86	$101	$115	$158	~~$350~~ 500	$285	27.1%
		17.4%	13.9%	37.4%	121.5%	-18.5%	
COMPUTER AIDED MFG	$2	$4	$9	$13	~~$52~~ 70	$48	89.2%
		100.0%	112.5%	52.9%	300.0%	-6.8%	
TOTAL	$1,017	$1,177	$1,187	$1,750	~~$3,166~~ 1410	~~$2,566~~ 2649	20.3%
GROWTH		15.7%	.9%	47.4%	80.9%	-18.9%	
CAPITAL SPENDING	$2,583	$2,735	$2,852	$3,725	~~$7,884~~ 3620	$6,666	20.9%
GROWTH	38.1%	5.9%	4.3%	30.6%	111.6%	-15.4%	
PERCENT EQUIPMENT	78.8%	86.1%	83.2%	93.9%	80.3%	77.0%	
TOTAL EQUIPMENT	2035	2355	2373	3498		5133	
PLANT	541	380	479	227		1533	
	.27	.16	.20	.06		.30	

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Wafer Fabrication Equipment Forecast

INTRODUCTION

This section describes the Semiconductor Equipment and Materials Service (SEMS) forecast for wafer fabrication equipment. It includes all capital equipment used in the front-end manufacturing of silicon and gallium arsenide wafers. The wafer fabrication equipment forecast is derived from the SEMS semiannual capital equipment forecast and will be updated together with the capital spending forecast. This version of the equipment forecast is based on the most recent capital spending forecast published in November 1986. For more information, refer to the November 1986 SEMS newsletter: "The Changing Landscape of Capital Spending."

The notebooks contain separate sections that discuss in detail several segments of the front-end equipment market. Each section also contains a forecast for its particular equipment segment, and a note of explanation is required to prevent confusion as to which forecast to use. Use the forecast in this section if the copyright date on the notebook section is dated before October 1986, since the previous forecast was made at an earlier date under a different set of assumed market conditions.

CAPITAL SPENDING

Capital spending includes expenditures for wafer fabrication (front end) equipment, assembly and test (back end) equipment, and property and plant. Dataquest's total capital spending forecast by worldwide merchant and captive semiconductor manufacturers is shown in Table 1. It is derived from our forecast for worldwide semiconductor production (also shown in Table 1). Capital spending is expected to grow from $6,803 million in 1986 to $7,344 million in 1987 for an 8 percent growth. However, the amount spent on wafer fabrication equipment (Table 1) is expected to grow at a higher rate: 14.6 percent from $2,866 in 1986 to $3,284 in 1987.

Spending on front-end equipment will almost double from $3,284 in 1987 to $5,994 in 1991 for a compound annual growth rate (CAGR) of 16.2 percent over this period. Capital spending will grow around the same rate: 15.9 percent over this same period, growing from $7,344 in 1987 to $13,269 in 1991.

Figure 1 shows the growth in wafer fabrication equipment from 1985 to 1991. Although 1985 and 1986 were down years for the equipment industry, it is predicted that 1987 through 1991 will be growth years and some years will show very respectable growth rates.

Wafer Fabrication Equipment Forecast

Table 1

**WORLDWIDE SEMICONDUCTOR PRODUCTION AND CAPITAL SPENDING--
1985 THROUGH 1991
(Millions of Dollars)**

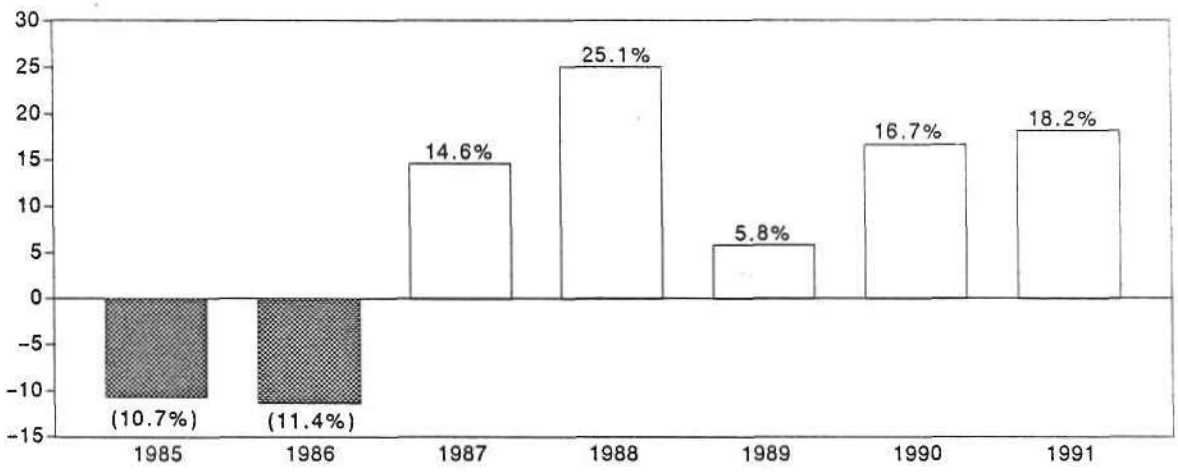
	1985	1986	1987	1988	1989	1990	1991	CAGR 1987-1991
Semiconductor Production*	$28,466	$34,711	$41,135	$52,428	$52,459	$60,814	$74,272	15.9%
Capital Spending	$ 7,138	$ 6,803	$ 7,344	$ 9,671	$ 9,173	$10,905	$13,269	15.9%
	(14.1%)	(4.7%)	8.0%	31.7%	(5.1%)	18.9%	21.7%	
Wafer Fabrication Equipment	$ 3,233	$ 2,866	$ 3,284	$ 4,109	$ 4,346	$ 5,071	$ 5,994	16.2%
	(10.7%)	(11.4%)	14.6%	25.1%	5.8%	16.7%	18.2%	

*Semiconductor Production includes worldwide merchant and captive production.

Source: Dataquest
November 1986

Figure 1

WAFER FABRICATION EQUIPMENT GROWTH



Source: Dataquest
November 1986

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DATAQUEST WORLDWIDE EQUIPMENT FORECAST

	1985	1986	1987	1988	1989	1990	CAGR(85-90)
LITHOGRAPHY	$774	$773	$1,080	$1,332	$1,474	$1,772	18.0%
	-18.1%	-.1%	39.7%	23.3%	10.7%	20.2%	
PROXIMITY/CONTACT	$67	$61	$95	$83	$39	$38	-10.4%
PROJECTION	$187	$173	$225	$258	$266	$297	9.8%
1X STEPPER	$45	$45	$63 66	$77 81	$86 79	$103 93	18.0%
REDUCTION STEPPER	$358	$368	$530 534 600	$673 691 772	$768 813 942	$950 986 979	21.6%
DIRECT-WRITE E-BEAM	$30	$42	$55	$75	$107	$147	37.9%
MASKMAKING E-BEAM	$84	$75	$96	$135	$154	$166	14.5%
X-RAY	$4	$8	$16	$30	$55	$70	77.3%
ETCH	$392	$388	$537	$655	$718	$855	16.9%
	-18.9%	-1.1%	38.3%	22.1%	9.6%	19.0%	
WET	$58	$51	$64	$70	$69	$74	5.2%
BARREL	$34	$32	$42	$49	$51	$57	11.0%
PLANAR	$284	$288	$407	$509	$570	$694	19.5%
ION MILLING	$16	$17	$24	$28	$28	$29	12.3%
AUTOMATIC PHOTORESIST	$121	$114	$149	$173	$180	$204	11.0%
	-23.0%	-6.0%	31.4%	16.0%	4.1%	13.1%	
DEPOSITION	$559	$548	$750	$906	$984	$1,159	15.7%
	-19.8%	-2.0%	36.9%	20.8%	8.5%	17.8%	
CVD	$199	$197	$273	$333	$365	$434	16.8%
PVD	$239	$232	$315	$377	$406	$474	14.7%
EPITAXY	$121	$119	$163	$196	$213	$251	15.7%
DOPING	$382	$370	$502	$601	$645	$753	14.5%
	-20.6%	-3.0%	35.5%	19.6%	7.4%	16.6%	
FURNACES	$135	$124	$158	$176	$176	$188	6.9%
ION IMPLANT	$247	$247	$345	$424	$470	$564	18.0%
Medium Current	$118	$111	$140	$161	$170	$191	10.0%
High Current	$129	$131	$189	$239	$250	$298	18.3%
High Voltage	$5	$10	$15	$25	$50	$75	71.9%
INSPECTION -	$285	$284	$394	$484	$533	$638	17.5%
	-18.5%	-.5%	39.0%	22.7%	10.2%	19.6%	
COMPUTER AIDED MFG	$48	$55	$88	$123	$155	$212	34.4%
	-6.8%	13.8%	59.1%	40.4%	26.0%	36.9%	
TOTAL	$2,566	$2,539	$3,512	$4,287	$4,698	$5,592	16.9%
GROWTH	-18.9%	-1.1%	38.3%	22.1%	9.6%	19.0%	
CAPITAL SPENDING	$6,666	$6,348	$9,242	$11,431	$11,746	$13,979	16.0%
GROWTH	-15.4%	-4.8%	45.6%	23.7%	2.8%	19.0%	
PERCENT EQUIPMENT	77.0%	80.0%	76.0%	75.0%	80.0%	80.0%	

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Wafer Fabrication Equipment Forecast

Since the Japanese equipment market is valued in dollars rather than in yen, the 1986 downturn was actually more severe than the -11.4 percent change indicated due to the appreciation of the yen against the dollar. If 1986 was valued at a constant exchange rate, then the worldwide downturn would be about -22 percent, which is actually closer to what the equipment manufacturers experienced in 1986.

WAFER FABRICATION EQUIPMENT FORECAST

Table 2 forecasts the detail on the worldwide wafer fabrication equipment market. The table includes the total front-end spending by the world's merchant and captive semiconductor manufacturers. Front-end equipment is divided into ten major categories: eight wafer fabrication equipment categories that are directly related to the wafer fabrication process and two categories that are nonprocess related. The following sections describe the categories along with brief explanations about the forecasts.

Lithography

Lithography includes contact and proximity aligners, scanning projection aligners, steppers (reduction and 1:1), e-beam systems for direct-write on silicon and gallium arsenide, e-beam systems for maskmaking, and X-ray aligners. Optical pattern generators and photorepeaters used in maskmaking are not included.

The lithography market is expected to grow from $771 million in 1987 to $1,436 million in 1991 for a CAGR of 16.8 percent over this period. This growth is slightly higher than the total front-end equipment growth rate of 16.2 percent. Note that the contact/proximity and scanning projection aligners have low growth rates compared to steppers. This is due to the drive toward submicron geometries and the emergence of all-stepper fabs.

Steppers will be the dominant lithography tool used over the next five years due to the push to submicron geometries, and they are expected to be used down to the 0.5 micron level. The stepper market, which should show a 17 percent CAGR over 1987 through 1991, is characterized by the emergence of $1 million steppers with submicron resolution and intense competition. Note that the stepper market, which is expected to reach $825 million by 1991, is the largest wafer fabrication equipment market; only the dry etch equipment, at $637 million, approaches the stepper market. (The process control equipment market, which will be $857 million by 1991, is actually a general market consisting of many niche markets and applications.)

Table 2

WORLDWIDE WAFER FABRICATION EQUIPMENT FORECAST
(Millions of Dollars)

	1985	1986	1987	1988	1989	1990	1991	CAGR 1987-1991
Lithography	$831	$659	$771	$963	$1,038	$1,204	$1,436	16.8%
	(12.1%)	(20.7%)	17.0%	24.9%	7.8%	16.0%	19.3%	
Proximity/ Contact	40	32	28	26	26	30	30	1.7%
Projection	170	155	165	195	190	210	230	8.7%
Steppers	503	366	440	550	590	685	825	17.0%
Direct-Write E-beam	30	30	50	70	90	120	147	30.9%
Maskmaking E-beam	84	72	78	102	112	119	144	16.6%
X-ray	4	4	10	20	30	40	60	56.5%
Automatic Photoresist Equipment	$154	$129	$154	$191	$207	$245	$285	16.6%
	(21.8%)	(16.2%)	19.4%	24.0%	8.4%	18.4%	16.3%	
Etch and Clean	$530	$504	$545	$687	$702	$831	$983	15.9%
	(4.3%)	(4.9%)	8.2%	26.0%	2.2%	18.4%	18.3%	
Wet Process	125	117	123	157	155	182	213	14.7%
Dry Strip	45	42	45	60	67	91	107	24.2%
Dry Etch	344	330	361	450	460	535	637	15.3%
Ion Milling	16	15	16	20	20	23	26	12.9%
Deposition	$639	$585	$661	$823	$881	$1,025	$1,225	16.7%
CVD	224	205	240	310	330	390	465	18.0%
PVD	266	240	260	308	336	380	450	14.7%
Epitaxy	149	140	161	205	215	255	310	17.8%
Diffusion	$204	$191	$191	$185	$173	$163	$155	(5.1%)
	(5.1%)	(6.4%)	0.0%	(3.1%)	(6.5%)	(5.8%)	(4.9%)	
Rapid Thermal Processing	$16	$20	$30	$55	$65	$80	$95	33.4%
	60.0%	25.0%	50.0%	83.3%	18.2%	23.1%	18.8%	
Ion Implantation	$256	$200	$265	$342	$350	$410	$498	17.1%
	(15.2%)	(21.9%)	32.5%	29.1%	2.3%	17.1%	21.5%	
Medium Current	132	85	105	130	134	150	182	14.7%
High Current	119	105	145	192	182	208	253	14.9%
High Voltage	5	10	15	20	34	52	63	43.2%
Process Control	$413	$403	$463	$594	$624	$ 724	$857	16.6%
	(18.4%)	(2.4%)	14.9%	28.3%	5.1%	16.0%	18.4%	
Factory Automation	$80	$70	$88	$123	$155	$212	$250	29.9%
	14.3%	(12.5%)	25.3%	40.4%	26.0%	36.9%	17.7%	
Other	$110	$105	$116	$146	$151	$177	$210	16.0%
	(21.4%)	(4.5%)	10.5%	25.9%	3.4%	17.2%	18.6%	
Total Wafer Fabrication Equipment	$3,233	$2,866	$3,284	$4,109	$4,346	$5,071	$5,994	16.2%
	(10.7%)	(11.4%)	14.6%	25.1%	5.8%	16.7%	18.2%	

Source: Dataquest
November 1986

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Direct-write e-beam is expected to be a $147 million market by 1991, which represents a hefty CAGR of 30.9 percent over 1987 through 1991. Dataquest does not believe that e-beam will be used for high-volume IC manufacturing, but it believes that this strong growth will be driven by the use of e-beam in three niche markets. These are the quick-turn prototype market, low volume ASICS, and the gallium arsenide IC market.

X-ray is a technology that, for the last several years, has been seemingly always on the verge of taking off. We believe that the market will, in fact, finally begin to grow around 1988 through 1989 mainly for two reasons: X-ray's several inherent advantages over optical lithography and the resolution of X-ray maskmaking problems. We expect X-ray technology to be a $60 million market by 1991.

Automatic Photoresist Processing Equipment

Automatic photoresist processing equipment, or track equipment as it is more commonly referred to, includes wafer clean/bake, wafer prime, coat/bake, develop/bake, and resist stabilization equipment. Track equipment sales, which are expected to reach $285 million by 1991, are closely tied to sales of lithography equipment, since the processes performed on this equipment are actually part of the lithography process. Thus, the 16.6 percent CAGR for track equipment over 1987 through 1991 is similar to the 16.8 percent CAGR for lithography.

Etch and Clean

This equipment section describes wet process, dry strip, dry etch, and ion milling equipment.

Wet processing includes wet etching and wet cleaning. Wet process equipment includes immersion benches and stations, spray processors, and rinser/dryers. Although fabs are increasingly turning to dry etch processing, there will always be some use of wet processing in the fab. In fact, wet processing is becoming more advanced. For instance, wet benches that originally cost $20,000 have evolved into smart wet stations with advanced robotics that cost $250,000 or more. In addition, chemical reprocessors for use with wet stations costing $350,000 are now being introduced into the marketplace. The 1987 through 1991 CAGR for wet process equipment is expected to be 14.7 percent. That is slightly lower than the overall growth rate of front-end equipment. This market should reach $213 million by 1991.

Equipment for dry stripping of photoresist includes barrel strippers and single-wafer strippers. Single-wafer strippers are now appearing and several companies have recently introduced products in this area. Due to the advent of single-wafer strippers, the dry stripping market is expected to have an above average 24.2 percent CAGR from 1987 through 1991 and is expected to reach $107 million by 1991.

The dry etch equipment, which is forecast to be $637 million by 1991, includes parallel plate batch and single-wafer systems, and hexode systems. Dataquest believes that the market will shift away from the batch etchers toward the single-wafer systems, particularly as wafer sizes continue to get larger. The 1987 through 1991 CAGR for dry etch equipment is expected to be 15.3 percent

Overall, the etch and clean equipment market is expected to grow to 15.9 percent from 1987 through 1991 as compared to 16.2 percent growth rate for all front-end equipment. By 1991, the etch and clean market is expected to reach $983 million. That will make it the third largest wafer fabrication equipment market, surpassed only by the lithography and deposition equipment markets.

Deposition

The deposition equipment market includes chemical vapor deposition (CVD), physical vapor deposition (PVD), and epitaxy.

CVD equipment includes atmospheric pressure CVD (APCVD), low pressure CVD (LPCVD), and plasma enhanced CVD (PECVD) techniques. The CVD equipment segment is expected to grow 18 percent from 1987 through 1991. This is due to the attention being focused on the deposition process to produce higher quality films required in VLSI device fabrication.

Within this segment, LPCVD is expected to grow at a faster rate than the other two technologies and should account for about 65 to 70 percent of the CVD market by 1991. There has been a lot of activity recently in the LPCVD market, as established companies and start-up companies introduce dedicated CVD reactors to the marketplace. It is the emergence of these dedicated CVD reactors that will account for the 18 percent growth rate and a $465 million market by 1991.

PVD equipment includes sputtering and evaporation techniques. Sputtering technology is being challenged by the need for planarized aluminum films for VLSI devices, and it is being threatened by the possibility of CVD metallization. Nevertheless, Dataquest expects that sputtering equipment will continue to increase at healthy rates, at least within the next five years for two reasons: sputter equipment manufacturers will continue to develop processes for planarized aluminum, and CVD aluminum deposition has yet to be proven a reality.

We believe that the use of evaporation technology in the fabrication of silicon devices has decreased over the years and that most evaporation equipment sales are for the aluminum lift-off process that is used in the fabrication of gallium arsenide (GaAs) devices. Therefore, the growth of evaporation equipment is determined by the growth of the GaAs market.

The PVD market for sputtering and evaporation techniques is expected to reach $450 million by 1991. This represents a 14.7 percent CAGR from 1987 through 1991. Historically, the PVD market has been larger than the CVD market, but we expect the CVD market to overtake the PVD market by 1988.

Epitaxy equipment includes silicon epitaxial reactors, molecular beam epitaxy (MBE) reactors, and metal-organic CVD (MOCVD) reactors. Currently, silicon reactors account for most of the epitaxy market at present, and growth in silicon reactors is being driven by the need for high throughput reactors that can deposit a low cost epi layer in CMOS applications.

MBE and MOCVD reactors are used in fabricating optoelectronics and other III-V devices and the market will grow as these device markets grow. Including the three technologies, the total epitaxy market is expected to grow 17.8 percent from 1987 through 1991, and reach $310 million by 1991.

Altogether, the total deposition market is the second-ranking front-end equipment segment. Lithography is ranked first. The deposition market is expected to grow 16.7 percent from 1987 through 1991, and by 1990, the deposition market will reach $1 billion. It will be exceeded only by the $1.2 billion lithography market. The increased high growth rate and large deposition market has caused this equipment segment to attract much more attention from the equipment vendors.

Diffusion

This category includes diffusion furnaces and high-pressure oxidation systems. Dataquest expects that this market segment, which is largely made up of diffusion furnaces, to decline 5.1 percent CAGR from 1987 through 1991. The market, which peaked in 1984, will decline to $155 million in 1991. The decline in this market is due to the rise of alternate technologies for processes that are currently being performed in diffusion furnaces. Another factor in the decline is the reduction of thermal budgets of VLSI devices, which cause process engineers to look for either lower temperature or lower time-at-temperature processes.

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Alternate technologies that are impacting this market include ion implantation, film deposition in dedicated CVD reactors, and rapid thermal processing. Annealing wafers in a rapid thermal processor (RTP) in lieu of a diffusion furnace also helps to reduce or conserve the thermal budget due to the very short time-at-temperature characteristics of RTPs.

Horizontal tube diffusion furnaces also are difficult and extremely costly to automate; in today's advanced furnaces, the automation cost exceeds the basic cost of the furnace. This difficulty may be a factor in the growth of the vertical diffusion furnace, which is considerably easier and less costly to automate. However, vertical furnaces have, so far, encountered slow acceptance in the marketplace.

Rapid Thermal Processing

Rapid thermal processing is an exciting and emerging wafer fabrication technology. Although techniques for doing rapid thermal processing have been around for a number of years, it is only with the very recent appearance of production-worthy techniques and machines that they have attracted increased attention from the process engineers. We expect this segment to have one of the highest rates of all types of wafer fabrication equipment: we expect a 33.4 percent CAGR from 1987 through 1991 and for the market to reach $95 million by 1991.

Current applications for rapid thermal processing include ion implant anneal, glass reflow, silicide formation, and deposition of thin gate oxides. Dataquest believes that as this technology matures more applications will be developed. One RTP manufacturer has predicted that in the future film deposition will consist of thick films deposited in minutes and thin films deposited in seconds by rapid thermal processing.

Ion Implantation

This segment consists of medium current, high current, and high-voltage implanters. Overall, this market is expected to show a CAGR of 17.1 percent over 1987 through 1991 and reach $498 million by 1991. Medium current and high current implanters should grow by 14.7 percent and 14.9 percent, respectively. High-voltage implanters, however, are expected to reach 43.2 percent.

Applications trends in ion implantation, which are driving the forecast, include the use of high-voltage implanters for retrograde wells and low-voltage implanters for shallow junctions. In addition, the low-dose market is growing faster than the high-dose market.

Process Control

Process control is a broad category. It includes mask and wafer inspection equipment, process monitoring equipment, surface analysis equipment, and analytical instrumentation. Although this market is expected to reach $857 million in 1991, it is a highly fragmented market. There are dozens of companies selling into a multitude of noncompetitive market niches. Some of the market niches are dominated by a single vendor, some have only two or three participants, and others have many vendors.

The growth rates among the various niches vary from low to high. The overall growth rate, however, for the process control category is expected to grow at a CAGR of 16.6 percent over 1987 through 1991. It is Dataquest's opinion that the fabrication and manufacturing expertise of the semiconductor industry is maturing and that the industry is entering the next major manufacturing phase--factory automation. Full automation with hands-off operation, however, requires automated process control and inspection equipment, and, in fact, factory automation and process control go hand-in-hand. Although total automation or "lights out" fabrication is still years away, we believe that the industry drive toward this goal will cause the process control vendors to develop the equipment needed to reach the goal, and that subsequent developments in process control equipment will further the state of automation.

Perhaps one of the more exciting and high growth areas in this market is wafer inspection. It includes linewidth measuring equipment and defect detection equipment. Recently introduced, or under development, are several high-end automatic wafer inspection systems designed for volume production. Another area of growth will be process monitoring equipment, such as ion implantation dosage monitors and mapping equipment. The market for process monitoring equipment is being pushed by the drive to devices with ever-decreasing line geometries that require tighter control and monitoring of process parameters.

Factory Automation

This market segment includes CIM software for shop floor control, factory host computer systems, cell controllers and interface hardware, and wafer transport systems including automatic guided vehicles (AGVs), robotics, and rail transport systems.

In the United States, CIM software and host computer systems are being installed by the semiconductor manufacturers. However, there have been almost no installations of wafer transport systems, except for some limited localized use of robotic equipment at the factory cell level. In Japan, many automated facilities use AGVs and other types of wafer

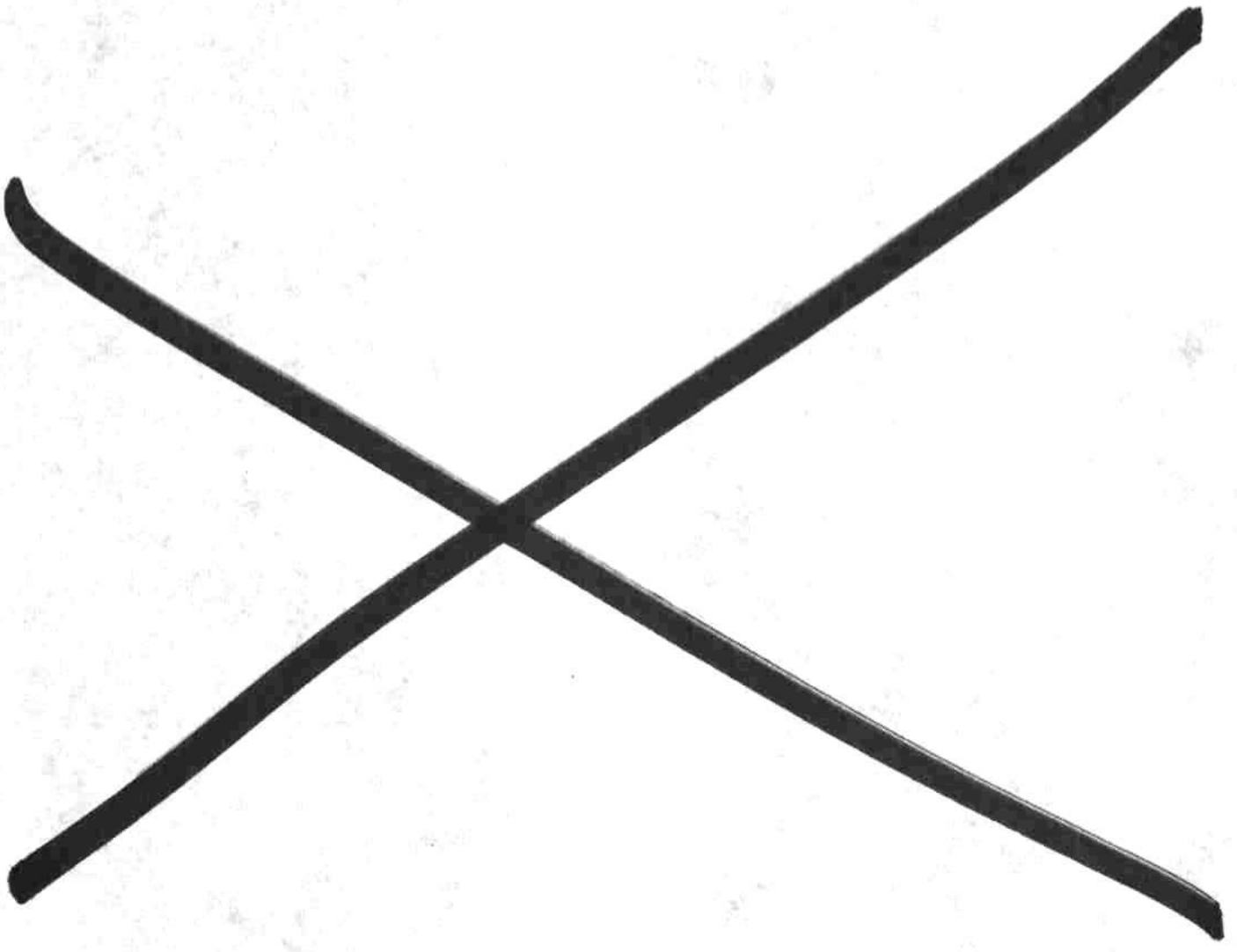
transport systems. We believe, however, that while the automated Japanese facilities use CIM software systems, the systems are not as advanced as the systems used in the United States.

The factory automation market, most of which is currently in Japan, is expected to reach $250 million by 1991 and grow to a 30 percent CAGR from 1987 through 1991. Driving the forecast are the continuing Japanese efforts to automate their facilities, and the emerging efforts of the American manufacturers. Dataquest believes that this forecast could actually be quite conservative should the American manufacturers realize they must automate at a faster pace if they intend to remain competitive in the world market.

Other

This general category includes the other capital equipment used throughout the fab but which does not fit into the previously mentioned major areas of wafer processing. This equipment is included in the forecast because the purchase of this equipment is part of the front-end capital budget.

This segment includes decontamination systems, wafer markers, gas analyzers, storage stations, and other types of equipment. This is not a single market due to the diversity of the products and applications in this area. Nevertheless, the expenditures in this area are expected to grow directly in line with expenditures for all front-end equipment. It should account for about 3 to 4 percent of front-end spending and reach $210 million by 1991.



Equipment Business Index

The following is a list of the material in this section

- Equipment Business Index
- Financial Aggregates

Equipment Business Index

INTRODUCTION

This service section presents the quarterly sales and income data for a select group of wafer fabrication equipment companies. The intent of this study is to provide clients of Dataquest's Semiconductor Equipment and Materials Service (SEMS) with an overview of the direction for the wafer fab equipment industry in general and for select individual companies in particular. Updates will be published at periodic intervals; however, current data are compiled on a continuous basis, so please contact the SEMS staff should you require this information before the update is published.

THE BUSINESS INDEX

The business index shown in Figure 1 presents the aggregate quarterly shipments for the 14 public companies listed in Table 1. These are all U.S. companies except for ASM International, a European company. In order to effectively compile a meaningful quarterly index that truly depicts the direction of the industry, access is required to company quarterly data for specific semiconductor equipment operations. This requirement rules out the public Japanese and European companies, except for ASM, because quarterly reporting is not required. This also rules out General Signal and Eaton because these companies do not break out their semiconductor equipment operations separately. The index is compiled from company financial reports, not from Dataquest estimates.

Table 1

The Fourteen–Company Business Index

Applied Materials (AMT)
ASM International
KLA Instruments
Kulicke and Soffa (K&S)
Lam Research Corporation
Machine Technology, Inc. (MTI)
Materials Research Corporation (MRC)
Nanometrics
Novellus
Optical Specialties, Inc. (OSI)
Perkin-Elmer Semiconductor Equipment Group (PE)
Silicon Valley Group (SVG)
Tylan
Varian Semiconductor Equipment Group

Source: Dataquest
February 1989

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When these requirements are met, we are left with only 14 companies, as shown in Table 1. Since this information was prepared, two additional companies have gone public; these companies will be included in the next edition of the index, along with one or two other small companies. However, Dataquest believes that the index truly reflects the direction of the entire industry, as the 14 companies represent the bulk of the wafer fab equipment industry. (Kulicke and Soffa is included in the index even though it manufactures assembly equipment.)

The equipment index shown in Figure 1 should be compared with Figure 2, which shows data compiled by the Semiconductor Equipment Association of Japan (SEAJ). Figure 2 shows the domestic shipments of Japanese equipment manufacturers in Japan for the three semiconductor equipment categories of wafer processing equipment, assembly equipment, and testing equipment. The data were collected from the 98 Japanese equipment company members of SEAJ and represent more than 90 percent of domestic sales, according to the SEAJ. The data are shown in yen so as to remove exchange rate distortions.

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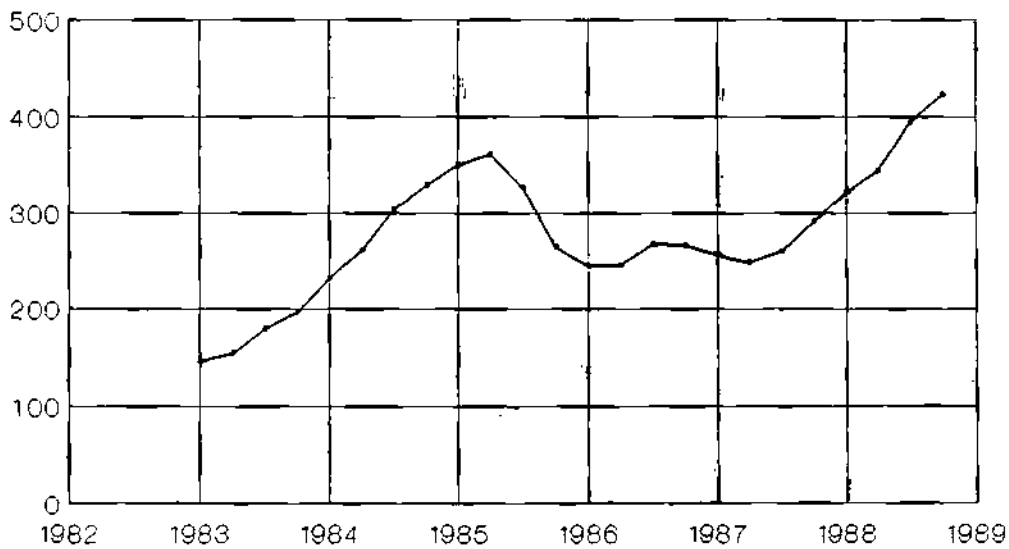
Equipment Business Index

Figure 1

The Fourteen-Company Business Index—Sales by Quarter
(Millions of Dollars)

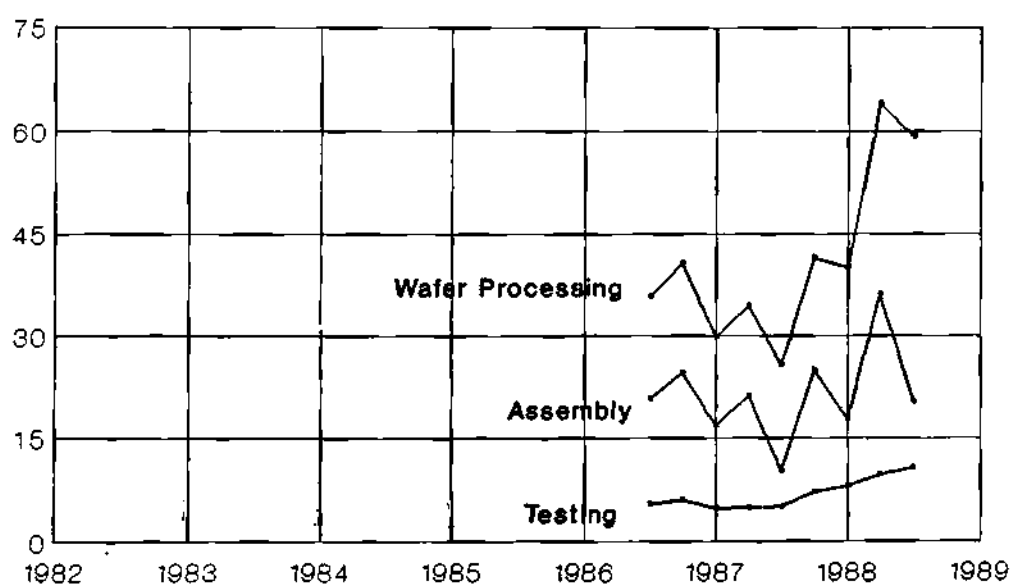


0002533-1

Source: Dataquest
February 1989

Figure 2

Japanese Equipment Vendor Shipments—SEAJ Data
(Billions of Yen)



0002533-2

Source: Dataquest
February 1989

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Equipment Business Index

Because Varian and Perkin-Elmer do not report quarterly operating profit for their semiconductor equipment operations, a 12-company business index was constructed without them in order to show index sales and net income that can be directly compared. This index is shown in Figures 3 and 4. Table 2 summarizes the data in Figures 3 and 4, and it presents the rate of return of income to sales. Figures 5, 6, 7, and 8 graphically compare the sales of various companies in the index on a quarterly basis. Table 3, in turn, presents 1988 fiscal year results by company in tabular form, and Figures 9 and 10 illustrate 1988 fiscal year sales and net income, respectively, for the 14 companies.

Table 2

Total Sales and Net Income of Business Index Companies
By Calendar Year
(Millions of Dollars)

Calendar Year	Sales of All 14 Companies	Sales of 12 Companies	Net Income of 12 Companies	Ratio of Net Income to Sales for 12 Companies
1983	$ 760	$429	$22	5.1%
1984	$1,244	$746	$71	9.5%
1985	$1,197	$694	$12	1.7%
1986	$1,036	$655	($56)	(8.5%)
1987	$1,121	$777	($30)	(3.9%)
1988*	$1,162	$843	$52	6.2%

*First nine months

Source: Dataquest
February 1989

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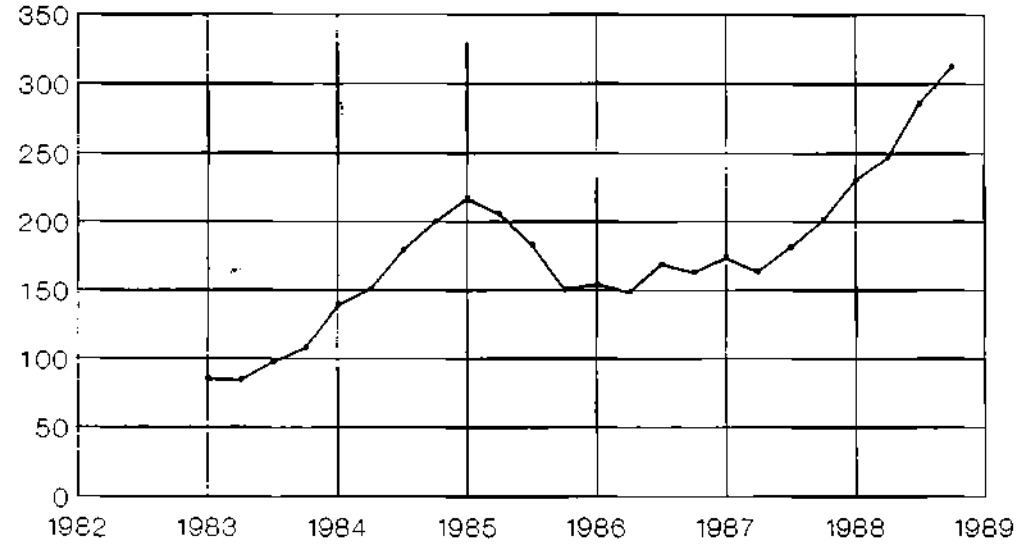
Equipment Business Index

Figure 3

The Twelve-Company* Business Index—Sales by Quarter (Millions of Dollars)

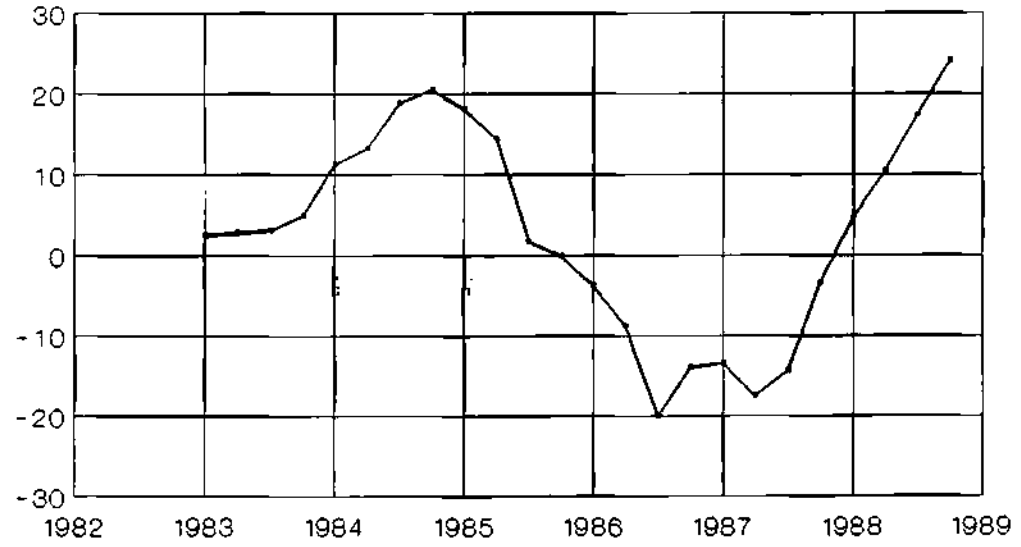


0002533-3

Source: Dataquest February 1989

Figure 4

The Twelve-Company* Business Index—Net Income by Quarter (Millions of Dollars)



0002533-4

Source: Dataquest February 1989

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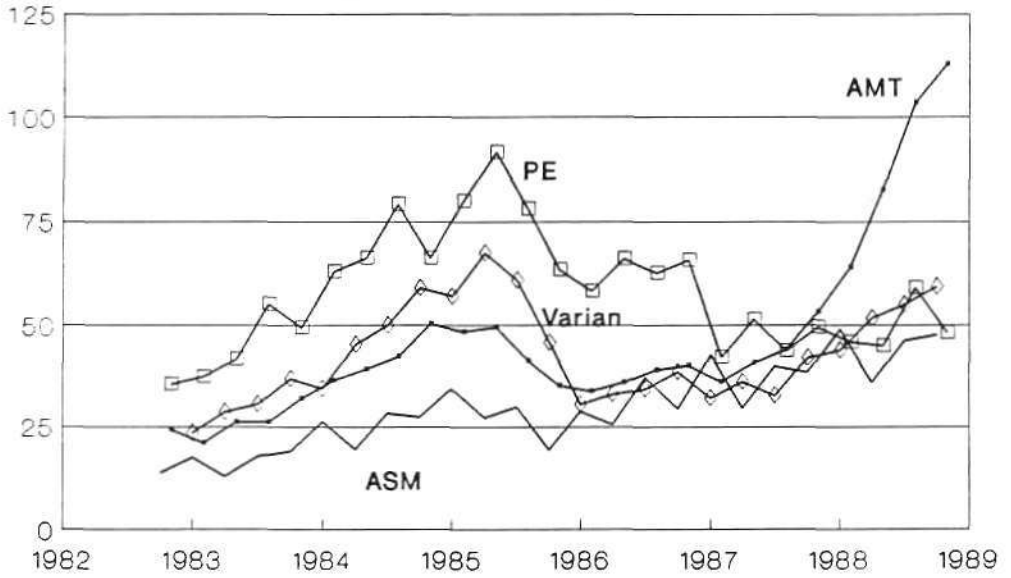
Figure 5

Fab Equipment Company Comparison—Sales by Quarter
Applied, Varian, Perkin-Elmer, ASM International
(Millions of Dollars)

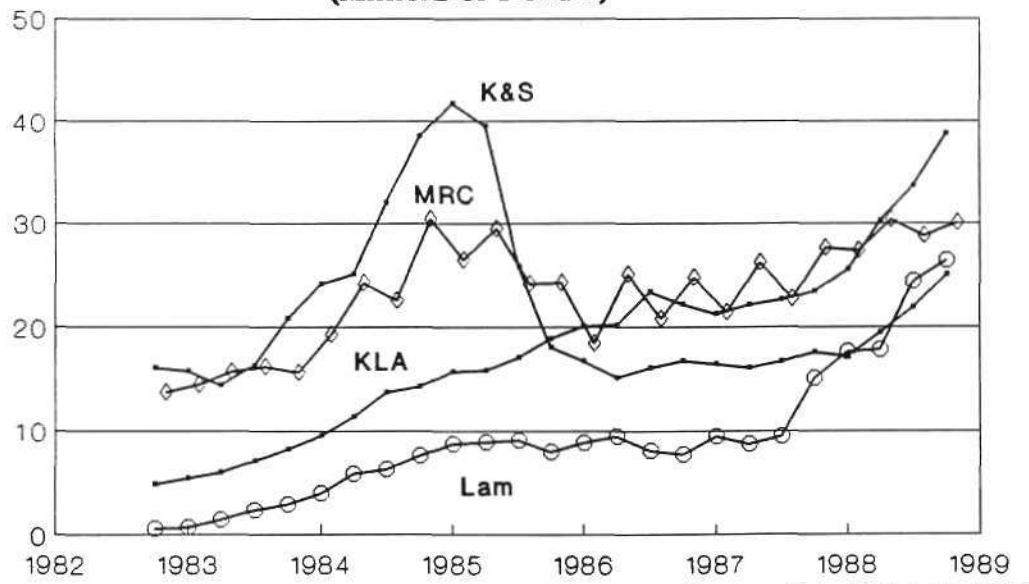


0002533-5

Source: AMT, ASM, PE, Varian

Figure 6

Fab Equipment Company Comparison—Sales by Quarter
Materials Research Corp., KLA Instruments,
Kulicke and Soffa, Lam Research
(Millions of Dollars)



0002533-6

Source: KLA, K&S, Lam, MRC

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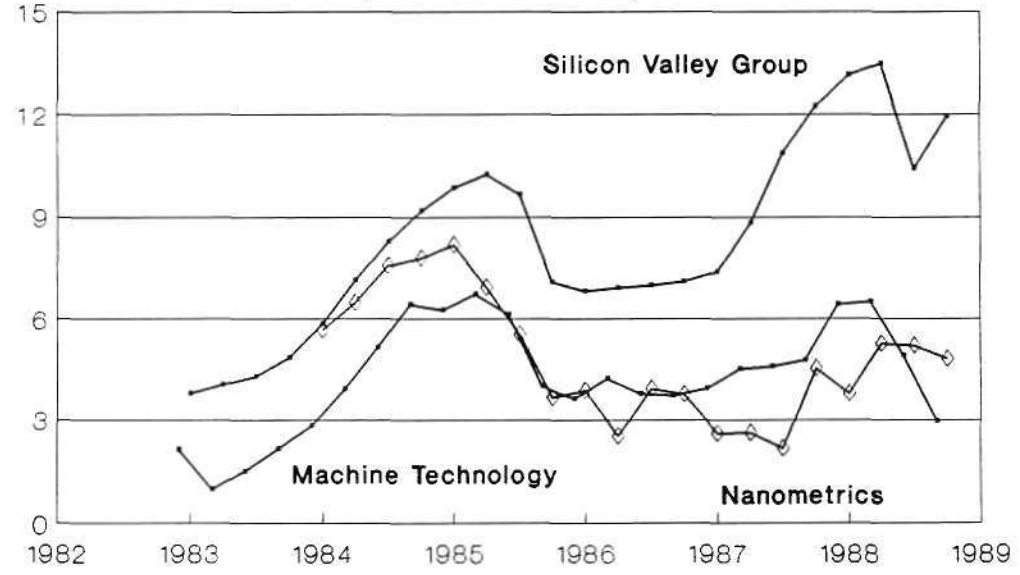
Figure 7

Fab Equipment Company Comparison—Sales by Quarter
Silicon Valley Group, Machine Technology, Nanometrics
(Millions of Dollars)

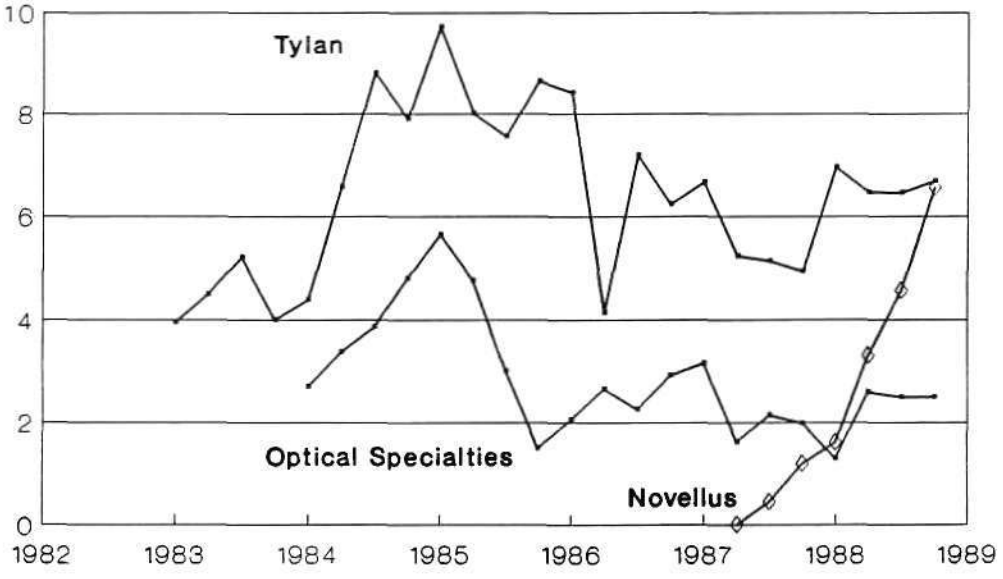


0002533-7

Source: MTI, Nanometrics, SVG

Figure 8

Fab Equipment Company Comparison—Sales by Quarter
Tylan, Novellus, Optical Specialties, Inc.
(Millions of Dollars)



0002533-8

Source: Novellus, OSI, Tylan

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Table 3

Fourteen-Company Comparison
Fiscal Year 1988 Fab Equipment Sales and Net Income
(Millions of Dollars)

Company	Fiscal Year Ends	FY 1988 Sales	FY 1988 Net Income	Ratio of Net Income to Sales
Applied Materials	10/31/88	$362.8	$40.0	11.0%
Varian	9/30/88	$210.1	$ 6.0*	2.9%
Perkin-Elmer	7/31/88	$199.6	$ 3.2*	1.6%
ASM International	12/31/88	$130.0**	$ 2.1**	1.6%
Materials Research Corp.	10/31/88	$116.6	$ 5.9	5.1%
KLA Instruments	6/30/88	$112.9	$ 8.8	7.8%
Kulicke and Soffa	9/30/88	$ 83.5	$ 4.4	5.3%
Lam Research Corp.	6/30/88	$ 75.0	$ 2.5	3.3%
Silicon Valley Group	9/30/88	$ 49.0	$ 4.4	9.1%
Tylan	6/30/88	$ 24.8	$ 3.2	12.9%
Machine Technology	8/31/88	$ 20.8	($ 6.6)	(31.6%)
Nanometrics	12/31/88	$ 15.3**	$ 0.4**	2.6%
Novellus	12/31/88	$ 14.4**	$ 1.7**	11.8%
Optical Specialties	9/30/88	$ 8.9	($ 4.1)	(46.0%)

*Group operating profit
**First nine months

Source: Company Annual Reports
Dataquest
February 1989

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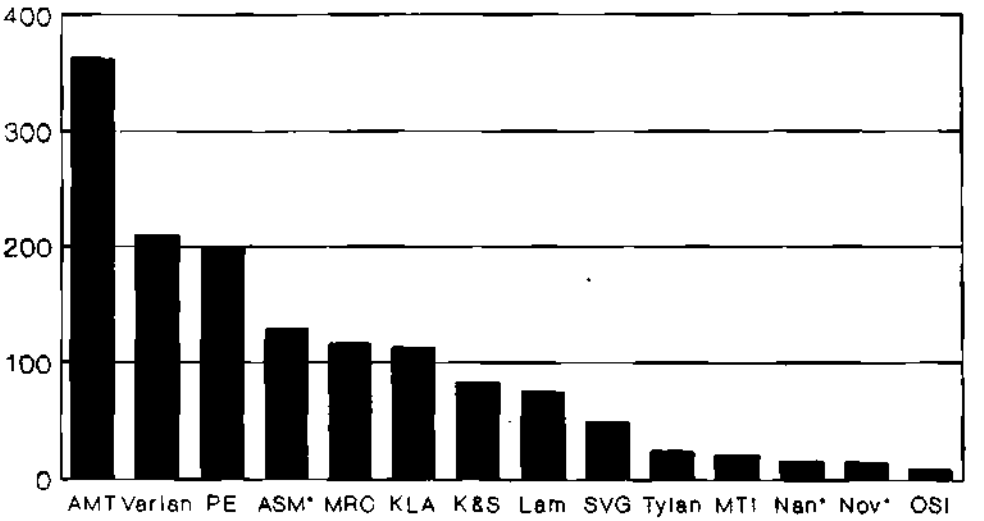
Figure 9

Fourteen–Company Comparison
Fiscal Year 1988 Fab Equipment Sales
(Millions of Dollars)

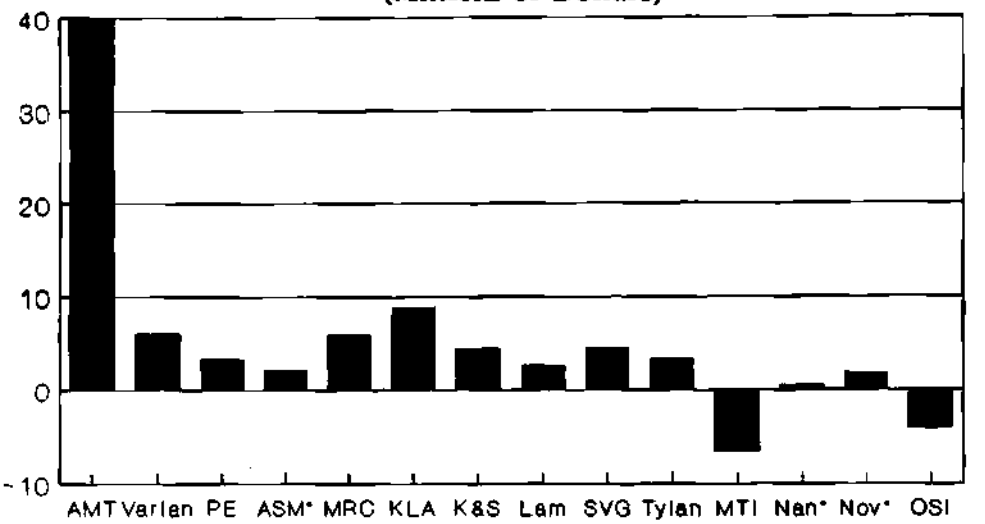


0002533-9

Source: Company Annual Reports
Dataquest
February 1989

Figure 10

Fourteen–Company Comparison
Fiscal Year 1988 Fab Equipment Net Income
(Millions of Dollars)



0002533-10

Source: Company Annual Reports
Dataquest
February 1989

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Individual Company Performance

Figures 11 through 25 illustrate the sales and net income performance for each of the fourteen companies on a quarterly basis. Tables 4 through 18 present the individual fiscal year results. For ASM International, performance is represented in both dutch guilders and dollars so that exchange rate fluctuations in the results can be observed.

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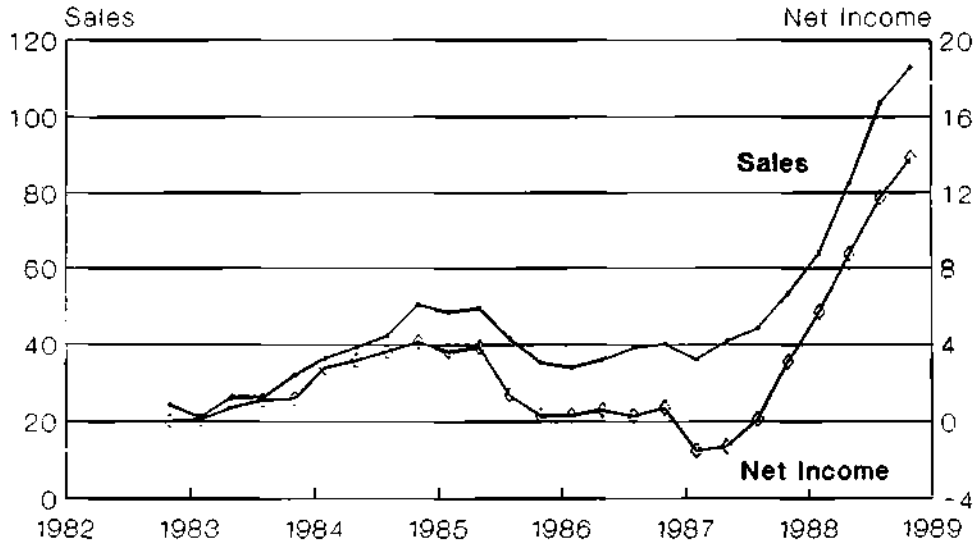
Figure 11

Applied Materials—Sales and Net Income by Quarter
(Millions of Dollars)



0002533-11

Source: Applied Materials

Table 4

Applied Materials—Fiscal Year Sales and Net Income
(Thousands of Dollars)

Fiscal Year (ends 10/31)	Sales	Net Income	Ratio of Net Income to Sales
1982	$ 90,830	($ 9,237)	(10.2%)
1983	$105,527	$ 3,065	2.9%
1984	$168,400	$13,728	8.2%
1985	$174,595	$ 9,187	5.3%
1986	$149,261	$ 1,860	1.3%
1987	$174,444	$ 336	0.2%
1988	$362,758	$40,009	11.0%

Source: Applied Materials
Dataquest
February 1989

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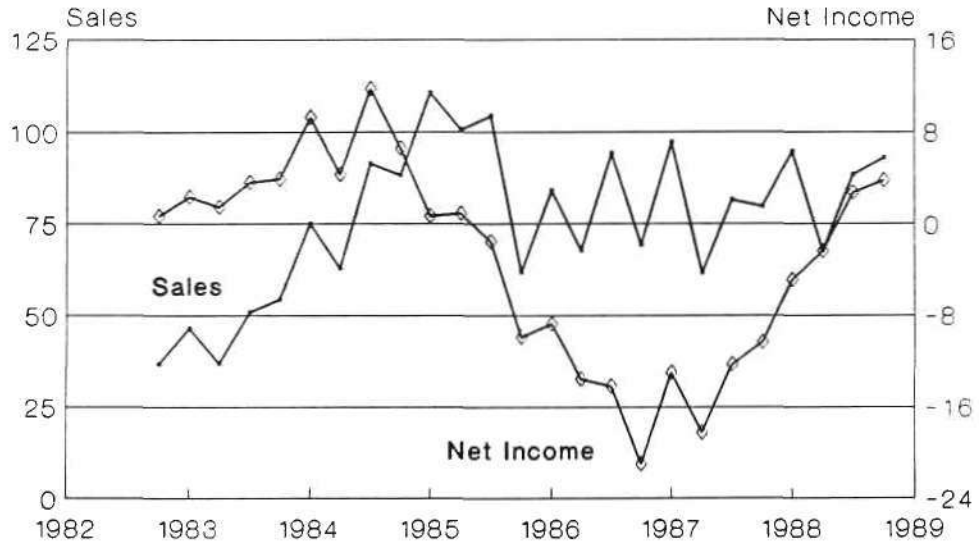
Figure 12

ASM International—Sales and Net Income by Quarter
(Millions of Dutch Guilders)



0002533-12

Source: ASM

Table 5

ASM International—Fiscal Year Sales and Net Income
(Thousands of Dutch Guilders)

Fiscal Year (ends 12/31)	Sales	Net Income	Ratio of Net Income to Sales
1982	F140,664	F 3,532	2.5%
1983	F217,054	F18,340	8.4%
1984	F352,922	F23,277	6.6%
1985	F350,850	(F19,238)	(5.5%)
1986	F328,363	(F61,696	(18.8%)
1987	F317,769	(F45,766)	(14.4%)
1988*	F249,178	F 4,166	1.7%

*First nine months of FY 1988
ASM Lithography not included in 1988 data

Source: ASM International
Dataquest
February 1989

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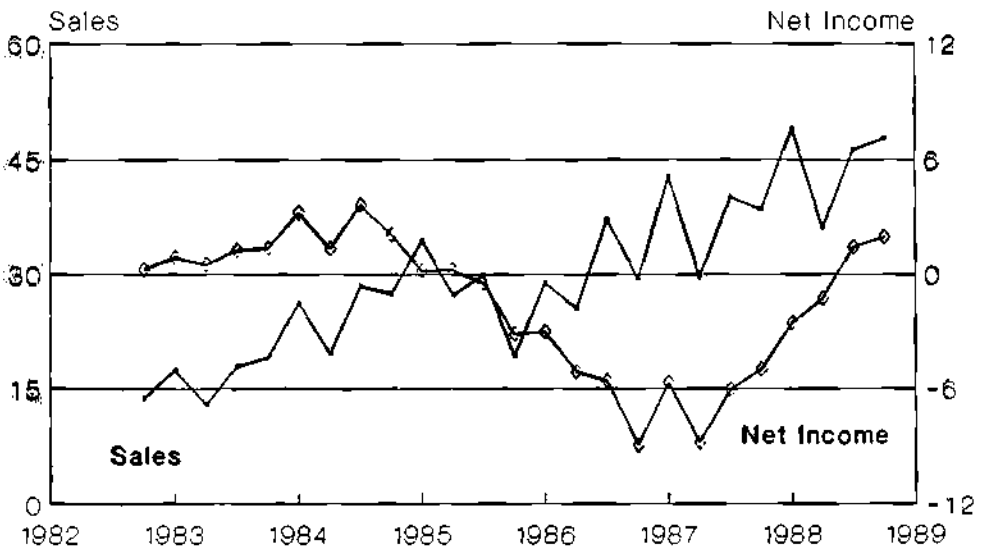
Figure 13

ASM International—Sales and Net Income by Quarter
(Millions of Dollars)



0002533-13

Source: ASM

Table 6

ASM International—Fiscal Year Sales and Net Income
(Thousands of Dollars)

Fiscal Year (ends 12/31)	Sales	Net Income	Ratio of Net Income to Sales
1982	$ 52,683	$ 1,323	2.5%
1983	$ 76,160	$ 6,435	8.4%
1984	$109,944	$ 7,251	6.6%
1985	$105,454	($ 6,281)	(6.0%)
1986	$135,071	($25,367)	(18.8%)
1987	$157,463	($22,355)	(14.2%)
1988*	$130,027	$ 2,120	1.6%

*First nine months of FY 1988
ASM Lithography not included in 1988 data

Source: ASM International
Dataquest
February 1989

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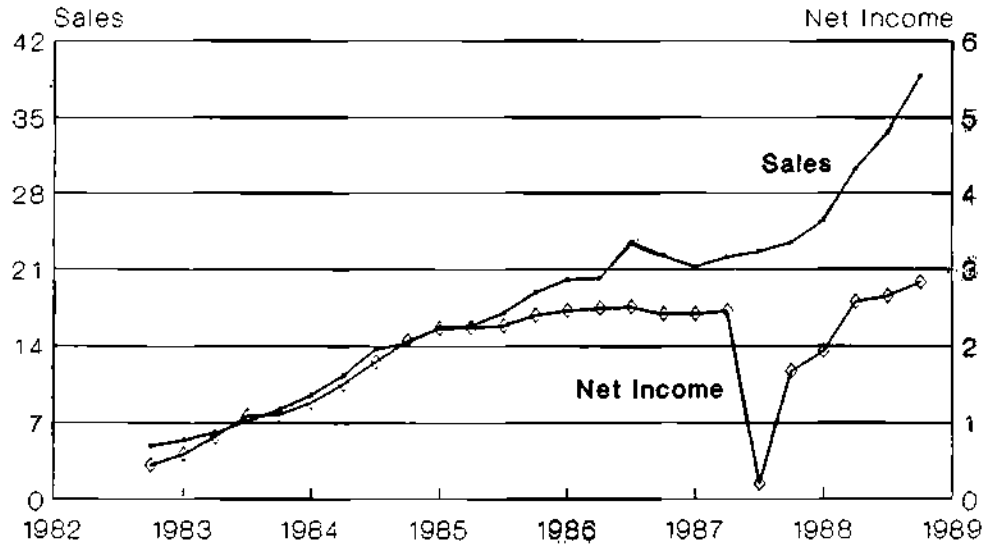
Figure 14

KLA Instruments—Sales and Net Income by Quarter
(Millions of Dollars)



0002533-14

Source: KLA

Table 7

KLA Instruments—Fiscal Year Sales and Net Income
(Thousands of Dollars)

Fiscal Year (ends 6/30)	Sales	Net Income	Ratio of Net Income to Sales
1982	$ 16,162	$1,510	9.3%
1983	$ 23,396	$2,928	12.5%
1984	$ 42,873	$5,664	13.2%
1985	$ 62,878	$8,802	14.0%
1986	$ 82,526	$9,854	11.9%
1987	$ 88,194	$7,489	8.5%
1988	$112,851	$8,827	7.8%

Source: KLA Instruments
Dataquest
February 1989

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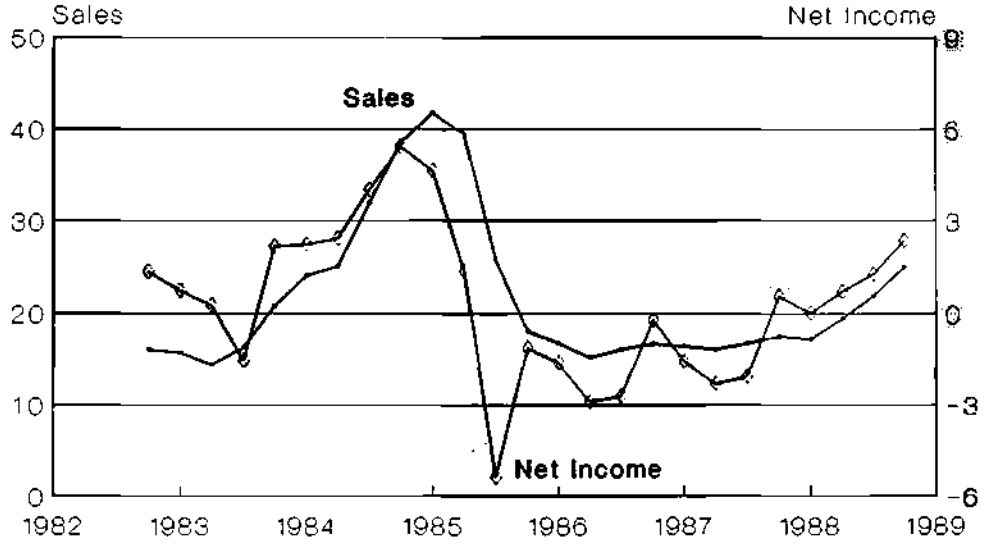
Figure 15

Kulicke and Soffa—Sales and Net Income by Quarter
(Millions of Dollars)



0002533-15

Source: Kulicke and Soffa

Table 8

Kulicke and Soffa—Fiscal Year Sales and Net Income
(Thousands of Dollars)

Fiscal Year (ends 9/30)	Sales	Net Income	Ratio of Net Income to Sales
1982	$ 54,159	$ 3,462	6.4%
1983	$ 67,314	$ 1,656	2.5%
1984	$119,641	$14,123	11.8%
1985	$125,102	($ 489)	(0.4%)
1986	$ 64,771	($ 7,445)	(11.5%)
1987	$ 66,856	($ 5,366)	(8.0%)
1988	$ 83,502	$ 4,357	5.2%

Source: Kulicke and Soffa
Dataquest
February 1989

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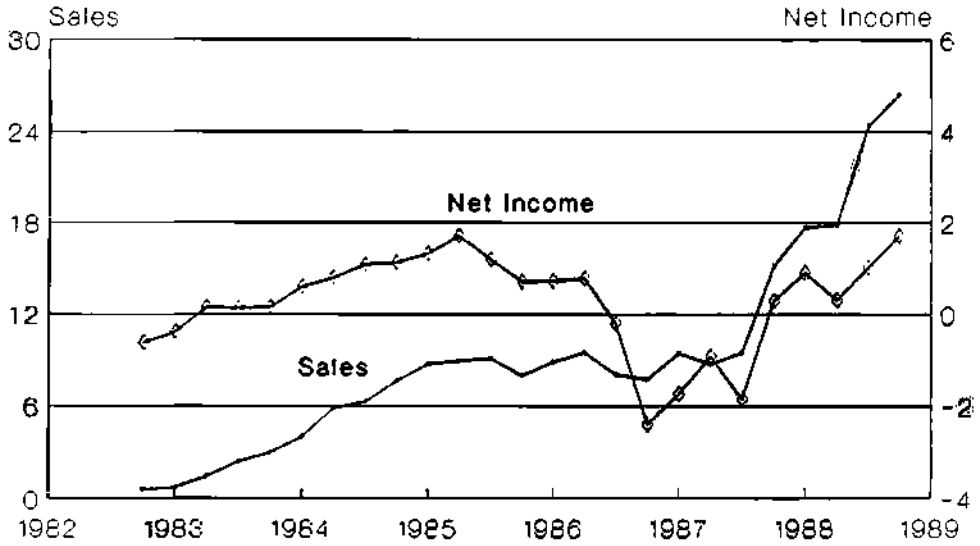
Figure 16

Lam Research—Sales and Net Income by Quarter
(Millions of Dollars)



0002533-16

Source: LAM

Table 9

Lam Research—Fiscal Year Sales and Net Income
(Thousands of Dollars)

Fiscal Year (ends 6/30)	Prior to Gemini Acquisition Sales	Prior to Gemini Acquisition Net Income	After Acquisition of Gemini Sales	After Acquisition of Gemini Net Income	After Acquisition of Gemini Ratio of Net Income to Sales
1983	$ 5,141	($ 715)	---	---	---
1984	$19,135	$2,638	$46,359	$5,853	12.6%
1985	$34,447	$5,367	$62,816	$7,133	11.4%
1986	$34,449	$1,998	$46,738	($ 900)	(1.9%)
1987	$25,486	($2,658)	$35,468	($6,908)	(19.5%)
1988*	$54,723	---	$74,963	$2,505	3.3%

*Lam Research acquired Gemini in February 1988.

Source: Lam Research
Dataquest
February 1989

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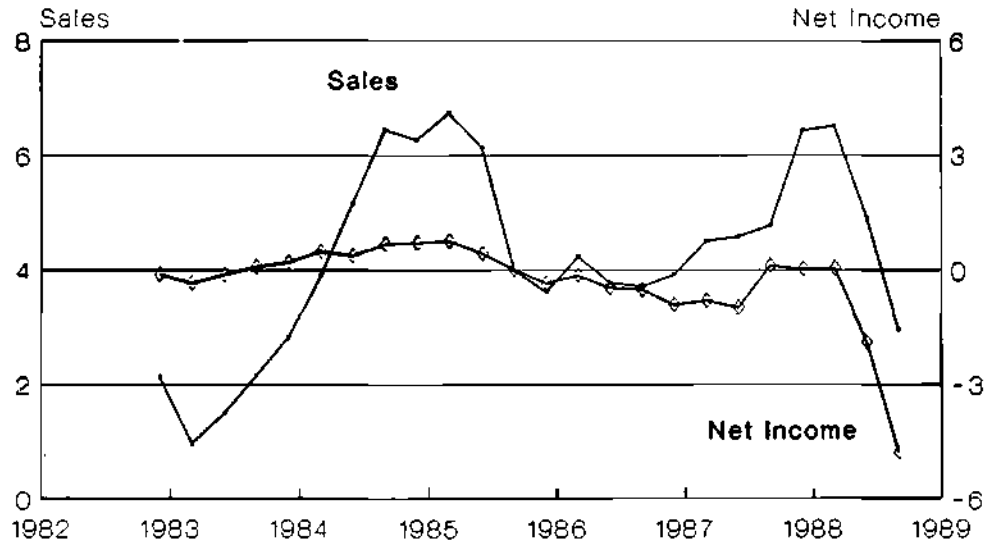
Figure 17

Machine Technology, Inc.—Sales and Net Income by Quarter
(Millions of Dollars)



0002533-17

Source: Machine Technology

Table 10

Machine Technology, Inc.—Fiscal Year Sales and Net Income
(Thousands of Dollars)

Fiscal Year (ends 8/31)	Sales	Net Income	Ratio of Net Income to Sales
1982	$ 9,212	$ 290	3.1%
1983	$ 6,748	($ 499)	(7.4%)
1984	$18,330	$1,730	9.4%
1985	$23,128	$1,933	8.4%
1986	$15,372	($1,428)	(9.3%)
1987	$17,774	($2,525)	(14.2%)
1988	$20,799	($6,570)	(31.6%)

Source: Machine Technology, Inc.
Dataquest
February 1989

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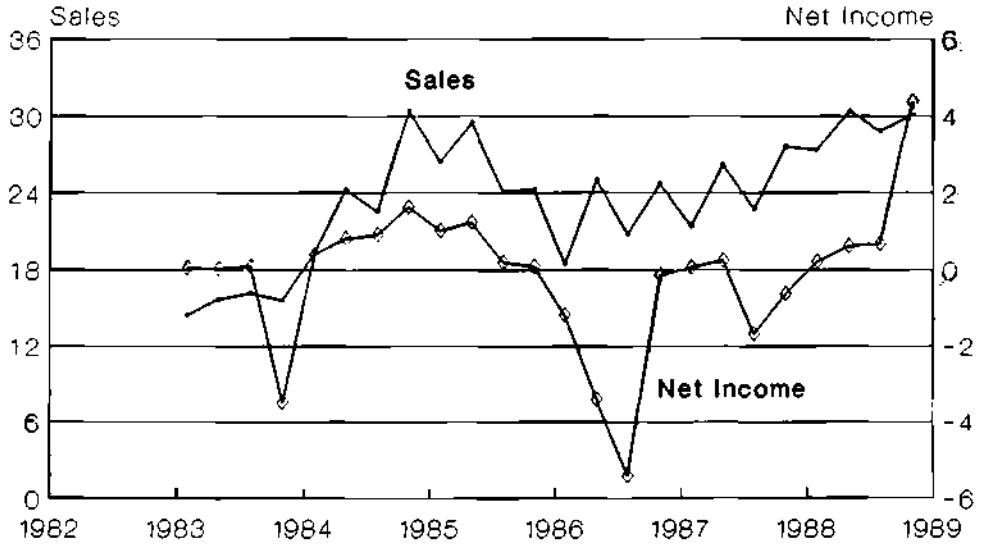
Figure 18

Materials Research Corporation—Sales and Net Income by Quarter
(Millions of Dollars)



0002533-18

Source: Materials Research

Table 11

Materials Research Corporation—Fiscal Year Sales and Net Income
(Thousands of Dollars)

Fiscal Year (ends 10/31)	Sales	Net Income	Ratio of Net Income to Sales
1982	$ 60,109	$ 728	1.2%
1983	$ 62,031	($ 3,284)	(5.3%)
1984	$ 96,559	$ 3,781	3.9%
1985	$104,321	$ 2,560	2.5%
1986	$ 89,095	($10,117)	(11.4%)
1987	$ 97,977	($ 1,964)	(2.0%)
1988	$116,654	$ 5,914	5.1%

Source: Materials Research Corporation
Dataquest
February 1989

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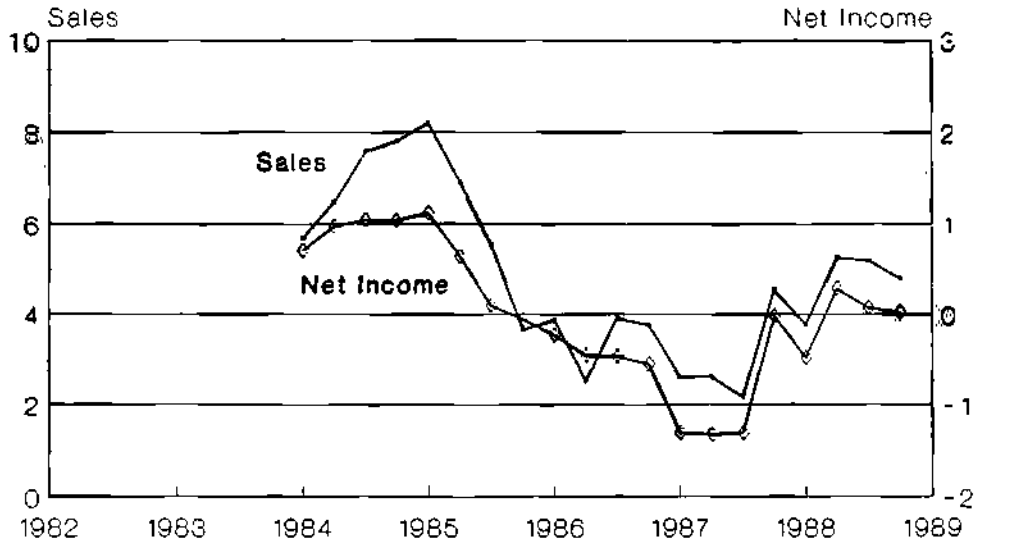
Figure 19

Nanometrics—Sales and Net Income by Quarter
(Millions of Dollars)



0002533-19

Source: Nanometrics

Table 12

Nanometrics—Fiscal Year Sales and Net Income
(Thousands of Dollars)

Fiscal Year (ends 12/31)	Sales	Net Income	Ratio of Net Income to Sales
1981	$13,914	$1,841	13.2%
1982	$13,277	$ 579	4.4%
1983	$19,836	$2,097	10.6%
1984	$30,067	$4,178	13.9%
1985	$20,027	$ 456	2.3%
1986	$12,813	($2,783)	(21.7%)
1987	$13,085	($3,128)	(23.9%)
1988*	$15,254	$ 381	2.5%

*First nine months

Source: Nanometrics
Dataquest
February 1989

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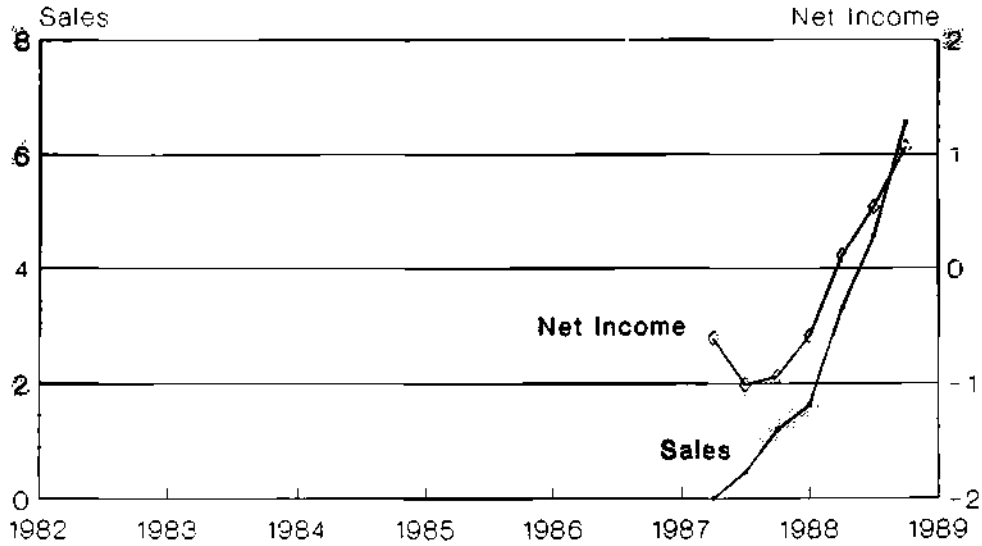
Figure 20

Novellus—Sales and Net Income by Quarter
(Millions of Dollars)



0002533-20

Source: Novellus

Table 13

Novellus—Fiscal Year Sales and Net Income
(Thousands of Dollars)

Fiscal Year (ends 12/31)	Sales	Net Income	Ratio of Net Income to Sales
1985*	---	($ 462)	---
1986	---	($1,744)	---
1987	$ 3,262	($3,150)	(96.6%)
1988	$14,419	$1,710	11.6%

*From April 1984 inception to December 31, 1985

Source: Novellus
Dataquest
February 1989

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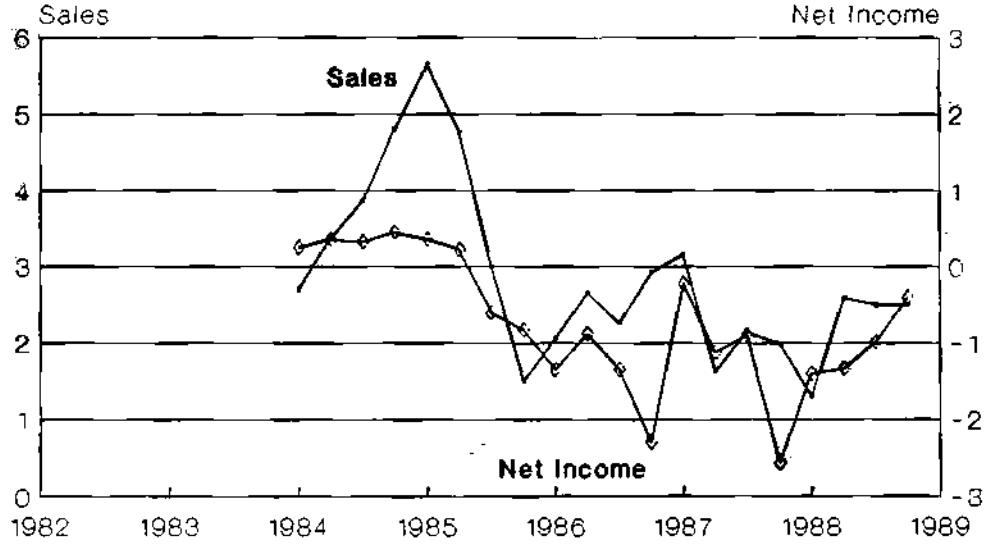
Figure 21

Optical Specialties, Inc.—Sales and Net Income by Quarter
(Millions of Dollars)



0002533-21

Source: Optical Specialties

Table 14

Optical Specialties, Inc.—Fiscal Year Sales and Net Income
(Thousands of Dollars)

Fiscal Year (ends 9/30)	Sales	Net Income	Ratio of Net Income to Sales
1981	$ 2,834	$ 143	5.0%
1982	$ 5,718	$ 382	6.7%
1983	$ 6,466	$ 109	1.7%
1984	$14,750	$1,385	9.4%
1985	$14,909	($ 836)	5.6%
1986	$ 9,887	($5,878)	(59.5%)
1987	$ 8,921	($4,814)	(54.0%)
1988	$ 8,900	($4,100)	(46.1%)

Source: Optical Specialties, Inc.
Dataquest
February 1989

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Figure 22

Perkin-Elmer Semiconductor Equipment Group
Sales and Orders by Quarter
(Millions of Dollars)

0002533-22

Source: Perkin-Elmer

Table 15

Perkin-Elmer Semiconductor Equipment Group
Fiscal Year Sales and Operating Profit
(Millions of Dollars)

Fiscal Year (ends 7/31)	Sales	Pretax Operating Profit	Ratio of Operating Profit to Sales
1982	$165.0	$20.9	12.7%
1983	$170.0	$19.1	11.2%
1984	$257.8	$33.8	13.1%
1985	$315.9	$42.6	13.5%
1986	$250.5	$20.3	8.1%
1987	$203.4	($76.1)	(37.4%)
1988	$199.6	$ 3.2	1.6%

Source: Perkin-Elmer
Dataquest
February 1989

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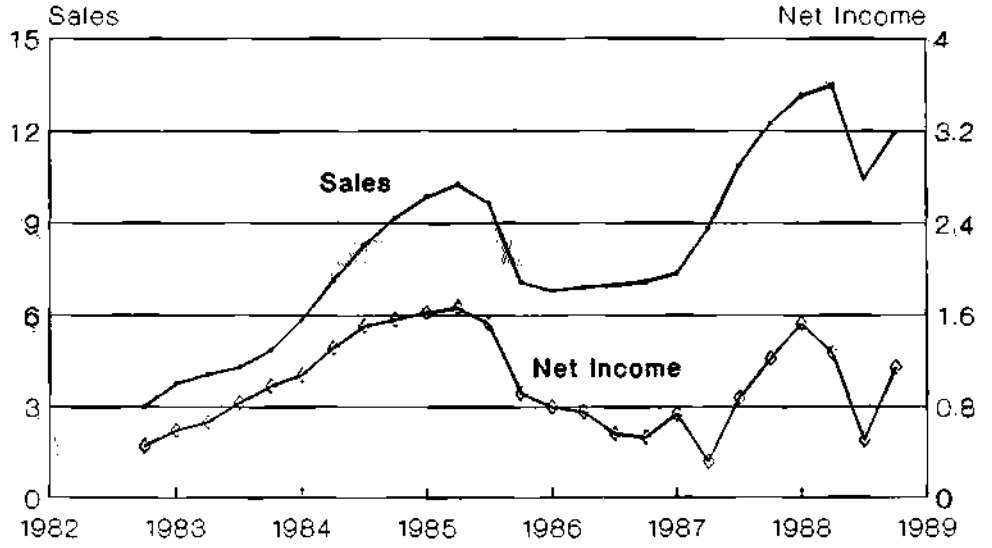
Figure 23

Silicon Valley Group—Sales and Net Income by Quarter
(Millions of Dollars)



0002533-23

Source: Silicon Valley Group

Table 16

Silicon Valley Group—Fiscal Year Sales and Net Income
(Thousands of Dollars)

Fiscal Year (ends 9/31)	Sales	Net Income	Ratio of Net Income to Sales
1982	$12,095	$1,888	15.6%
1983	$16,958	$3,064	18.1%
1984	$30,463	$5,456	17.9%
1985	$30,864	$5,733	18.6%
1986	$27,842	$2,646	9.5%
1987	$39,300	$3,148	8.0%
1988	$48,969	$4,440	9.1%

Source: Silicon Valley Group
Dataquest
February 1989

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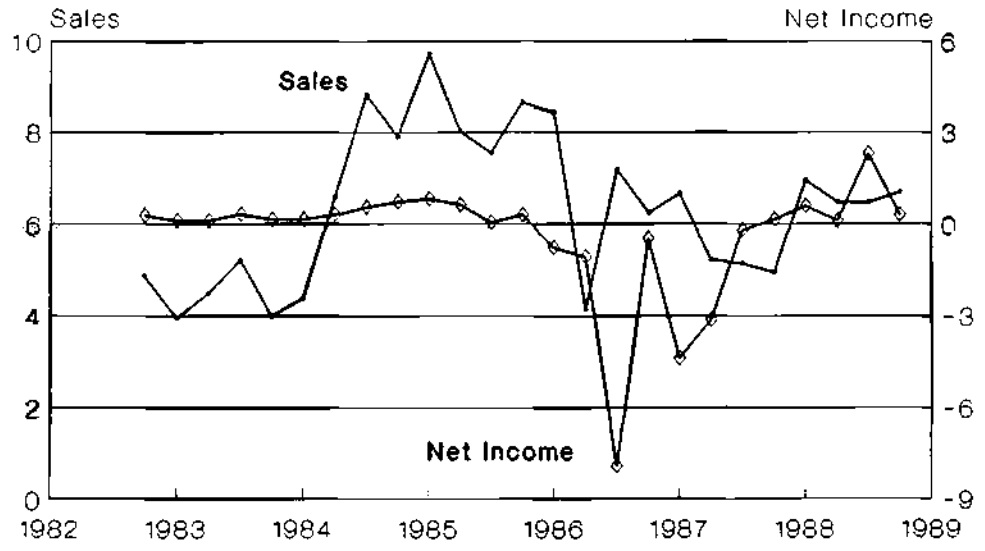
Figure 24

Tylan—Sales and Net Income by Quarter
(Millions of Dollars)



0002533-24

Source: Tylan

Table 17

Tylan—Fiscal Year Sales and Net Income
(Thousands of Dollars)

Fiscal Year (ends 6/30)	Sales	Net Income	Ratio of Net Income to Sales
1982	$18,214	$1,019	5.6%
1983	$18,511	$ 819	4.4%
1984	$23,780	$1,150	4.8%
1985	$33,185	$2,224	6.7%
1986	$28,405	($9,458)	(33.3%)
1987	$23,256	($8,173)	(35.1%)
1988	$24,830	$3,163	12.7%

Source: Tylan
Dataquest
February 1989

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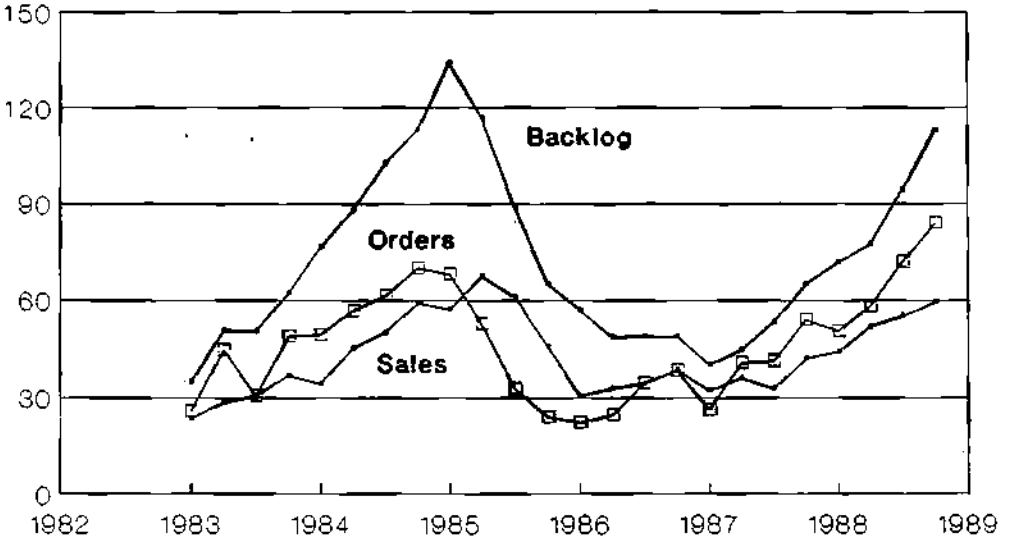
Figure 25

Varian Associates Semiconductor Equipment Group
Sales, Orders, and Backlog by Quarter
(Millions of Dollars)



0002533-25

Source: Varian

Table 18

Varian Associates Semiconductor Equipment Group
Fiscal Year Sales and Operating Profit
(Millions of Dollars)

Fiscal Year (ends 9/30)	Sales	Pretax Operating Profit	Ratio of Operating Profit to Sales
1982	$ 99.0	$ 3	3.0%
1983	$119.8	$ 9	7.5%
1984	$206.0	$40	19.4%
1985	$231.4	$ 8	3.5%
1986	$136.6	($28)	(20.5%)
1987	$143.1	($24)	(16.8%)
1988	$210.1	$ 6	2.9%

Source: Varian Associates
Dataquest
February 1989

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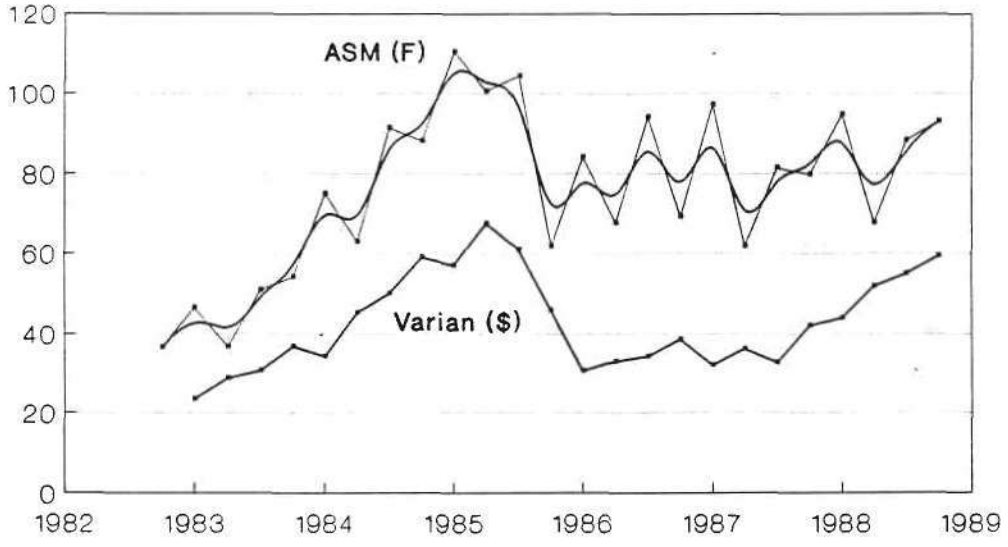
Company Comparisons

Figures 26 through 32 present company comparisons where those comparisons seem appropriate, either because of size of company or because the companies are competitors. For example, Figure 26 compares ASM International and Varian. The comparison is made in Dutch guilders and dollars in order to show the similarity of sales profiles without the effects of exchange rate fluctuations. A smooth curve is drawn through the actual data points for ASM International to more effectively show the sales trend.

Figure 26

ASM International and Varian—Sales by Quarter
(Millions of Dutch Guilders and Millions of Dollars)



0002533-26

Source: ASM, Varian

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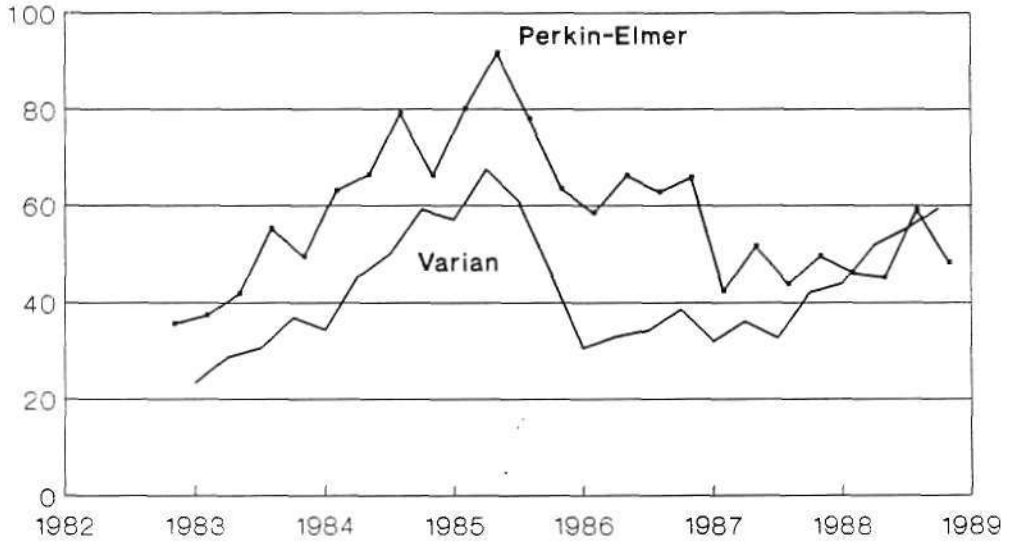
Figure 27

Perkin–Elmer and Varian—Sales by Quarter
(Millions of Dollars)

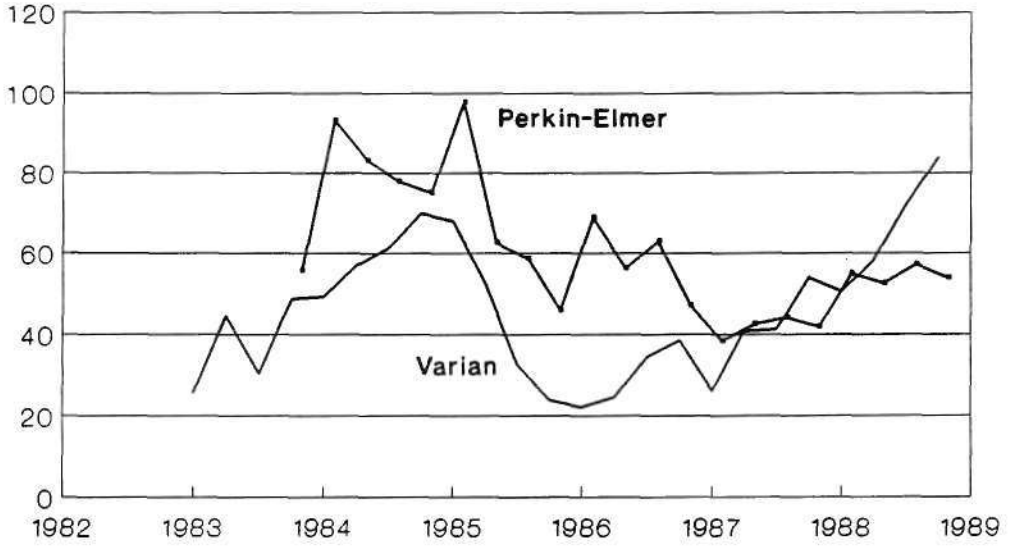


0002533-27

Source: Perkin-Elmer, Varian

Figure 28

Perkin–Elmer and Varian—Orders by Quarter
(Millions of Dollars)



0002533-28

Source: Perkin-Elmer, Varian

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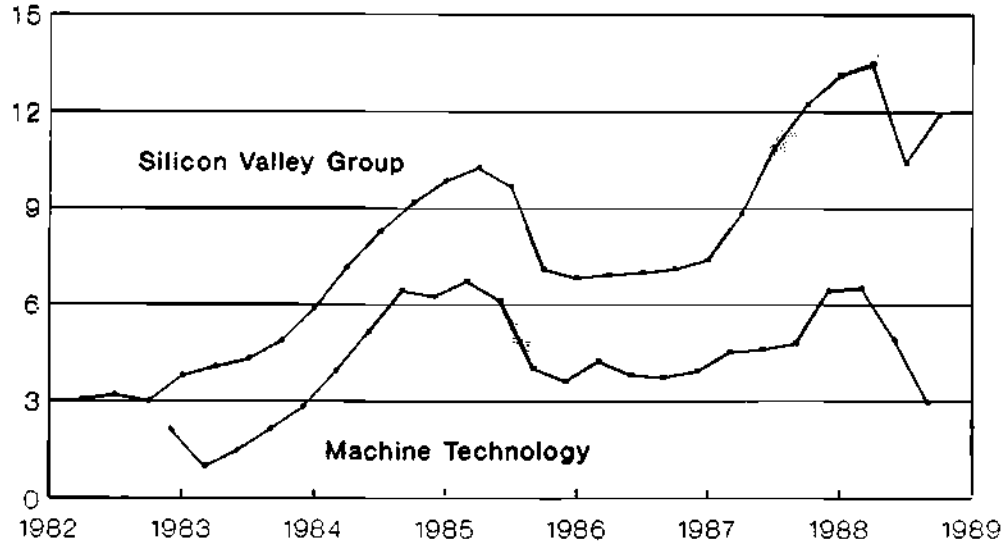
Figure 29

Machine Technology and Silicon Valley Group—Sales by Quarter
(Millions of Dollars)

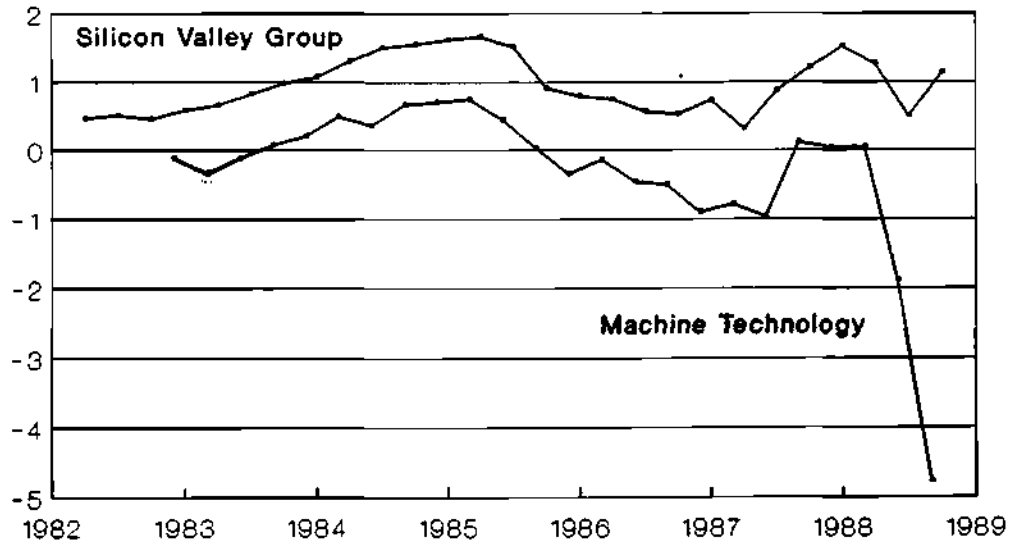


0002533-29

Source: Machine Technology, SVG

Figure 30

Machine Technology and Silicon Valley Group—Net Income by Quarter
(Millions of Dollars)



0002533-30

Source: Machine Technology, SVG

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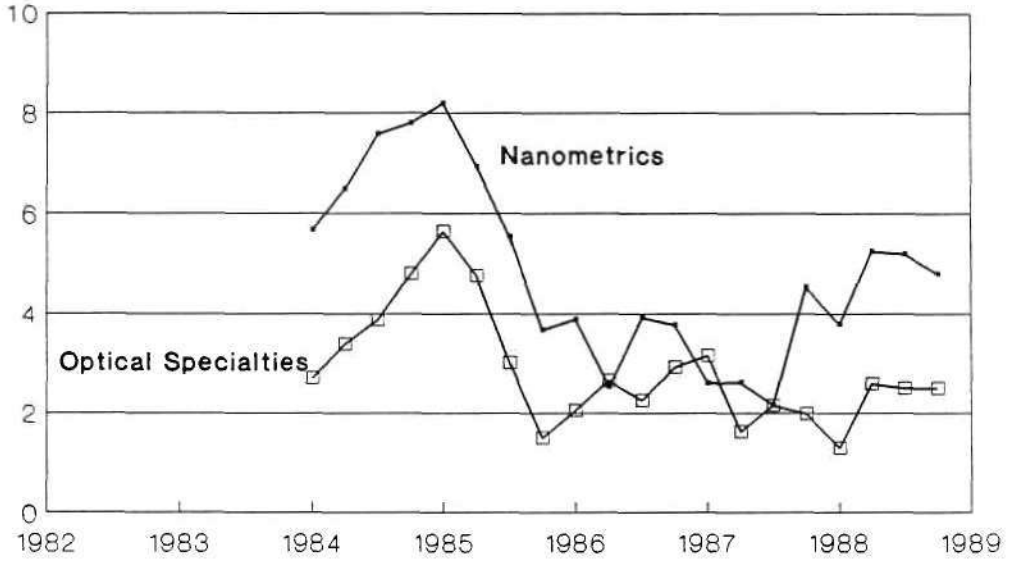
Figure 31

Nanometrics and Optical Specialties—Sales by Quarter
(Millions of Dollars)

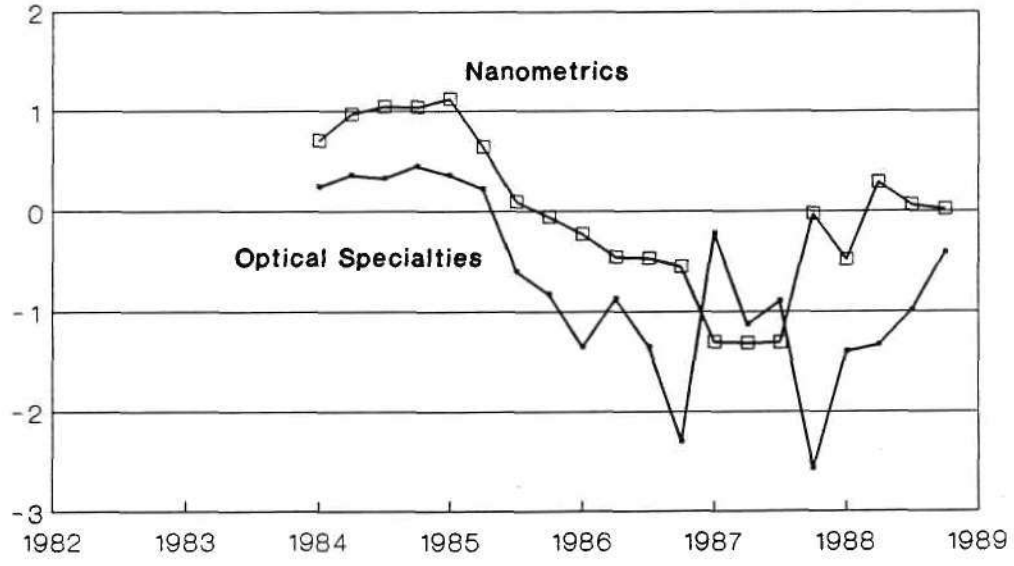


0002533-31

Source: Nanometrics, Optical Specialties

Figure 32

Nanometrics and Optical Specialties—Net Income by Quarter
(Millions of Dollars)



0002533-32

Source: Nanometrics, Optical Specialties

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Financial Aggregates

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PURPOSE

The purpose of this service section is to provide a financial and strategic overview of the major public companies participating in the semiconductor equipment and materials industry. Dataquest has compiled financial information on the companies in this industry from annual reports and 10-K statements. This financial information has then been aggregated, and industry-wide financial and strategic ratios have been calculated from these aggregates.

The ratios in this section include the following:

- Financial
  - Current Ratio (Current Assets/Current Liabilities)
  - Debt/Equity (Long-Term Debt/Average Shareholder's Equity)
  - Gross Margin ((Revenue - Operating Expenses)/Revenue)
  - Net Margin (Earnings Before Taxes/Revenue)
- Strategic
  - Capital Spending (Capital Spending/Revenue)
  - RD&E (RD&E/Revenue)

COMPANIES COVERED

Fifteen companies were included in our survey of the equipment industry. These companies are listed in Table 1.

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Table 1

COMPANIES REFERENCED

Applied Materials
ASM America
Eaton Corporation
GCA
General Signal
KLA
Lam Research
Materials Research Corporation
Machine Technology Incorporated
Perkin-Elmer
Plasma-Therm
Silicon Valley Group
Tylan
Varian
Veeco

Source: Dataquest
August 1986

DATA

The fifteen companies surveyed fall naturally into three categories:

- Pure players
- Mixed players
- General players

These categories correspond roughly to the degree of concentration of a company's business in semiconductor equipment. The first category includes only those companies that derive all their revenue from semiconductor equipment sales (the pure players). These companies include: Applied Materials, ASM America, GCA, KLA, Lam Research, Machine Technology Inc., Plasma-Therm, Silicon Valley Group (SVG), and Tylan.

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The second category (the mixed players) includes all those companies that derive a significant proportion of their revenue from semiconductor equipment sales. This category includes all the pure players, plus Materials Research Corporation, Perkin-Elmer, Varian, and Veeco.

The third category (the general players) includes all those companies that either derive a significant proportion of their revenue from semiconductor equipment sales or are major players in the market. This group includes all the mixed players, plus Eaton Corporation and General Signal.

All data have been converted from a fiscal to a calendar year for the basis of comparison.

General Players

This category contains, besides the mixed players, Eaton Corporation and General Signal Corporation. Both of these companies do a large volume of business outside of the semiconductor industry. Consequently, the ratios in this category are subject to influences extraneous to the semiconductor industry.

The current ratio for this group was relatively stable (see Figure 1), as was the debt/equity ratio (see Figure 2), which improved steadily from 1980 to 1985. Gross margins showed a tendency to rise over this period (see Figure 3). However, net margins did not share in this tendency to improve; in fact, they showed a great deal of volatility (see Figure 4 and Table 2). While capital spending was stable at 5 percent of revenue (see Figure 5), expenditures for RD&E rose steadily from 4 percent to 6 percent (see Table 2 and Figure 6).

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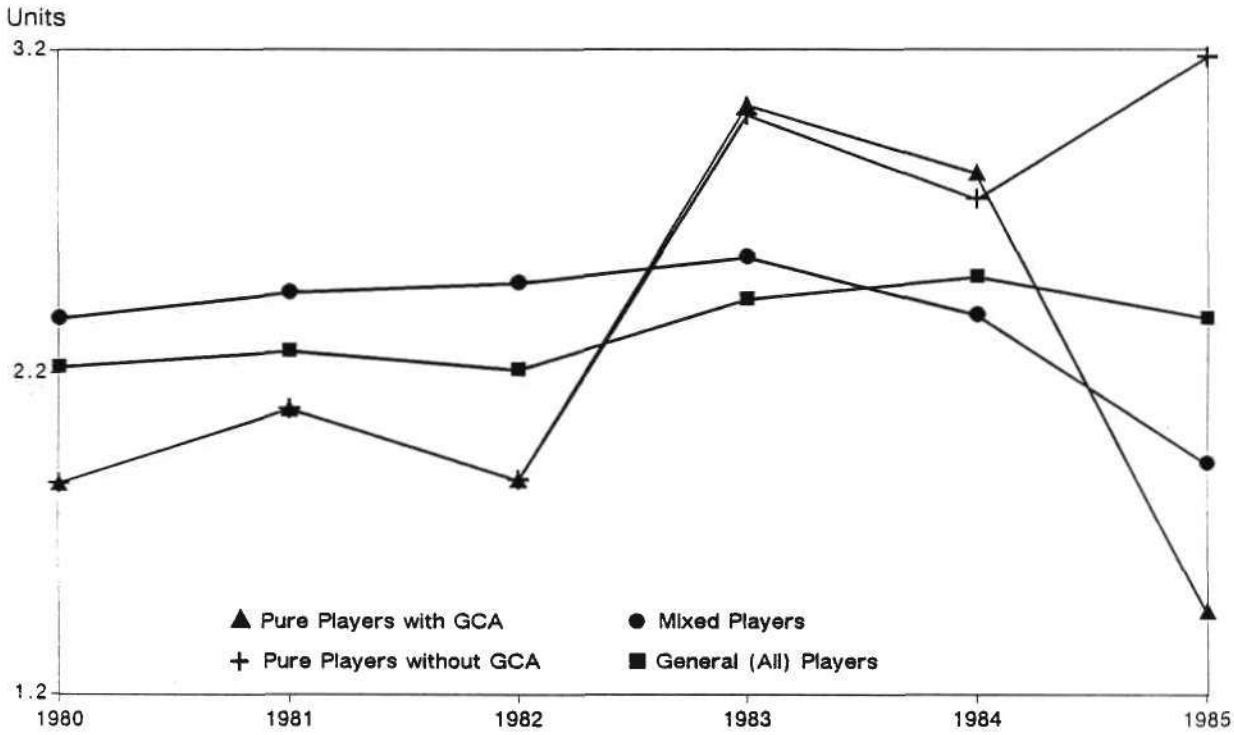
Figure 1

CURRENT RATIO



Source: Annual Reports, 1981 through 1985:
Applied Materials; ASM; GCA; KLA;
Lam Research; Machine Technology, Inc.;
Tylan; Silicon Valley Group; Plasma-Therm;
Varian; Eaton; General Signal; Materials Research Corp.;
Perkin-Elmer; and Veeco
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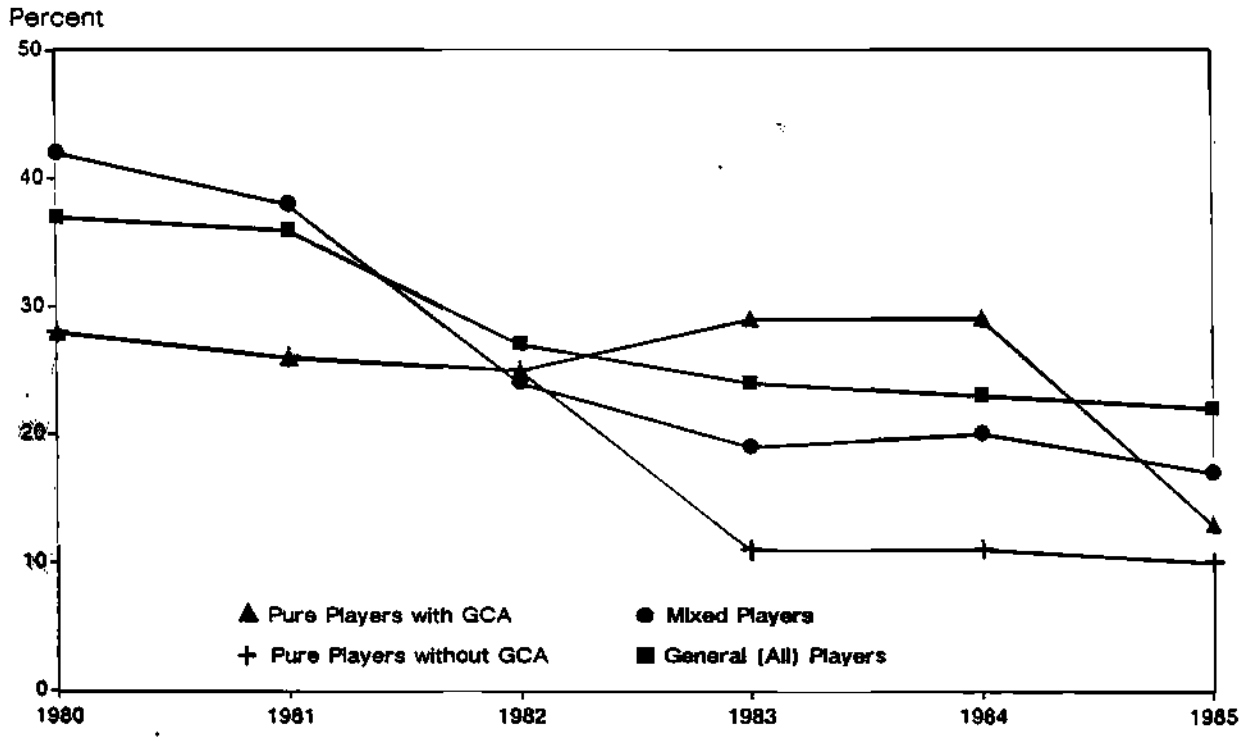
Figure 2

DEBT/EQUITY RATIO



Source: Annual Reports, 1981 through 1985;
Applied Materials; ASM; GCA; KLA;
Lam Research; Machine Technology, Inc.;
Tylan; Silicon Valley Group; Plasma-Therm;
Varian; Eaton; General Signal; Materials Research Corp.;
Perkin-Elmer; and Veeco
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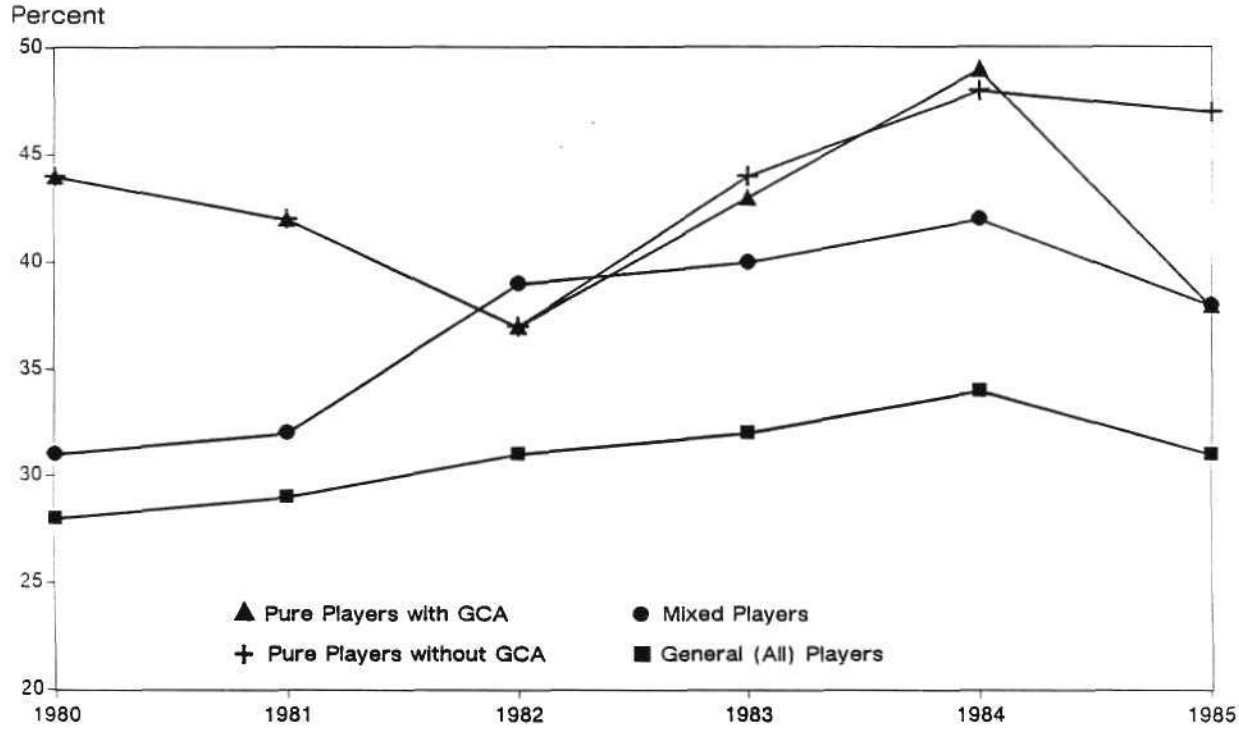
Figure 3

GROSS MARGIN



Source: Annual Reports, 1981 through 1985:
Applied Materials; ASM; GCA; KLA;
Lam Research; Machine Technology, Inc.;
Tylan; Silicon Valley Group; Plasma-Therm;
Varian; Eaton; General Signal; Materials Research Corp.;
Perkin-Elmer; and Veeco
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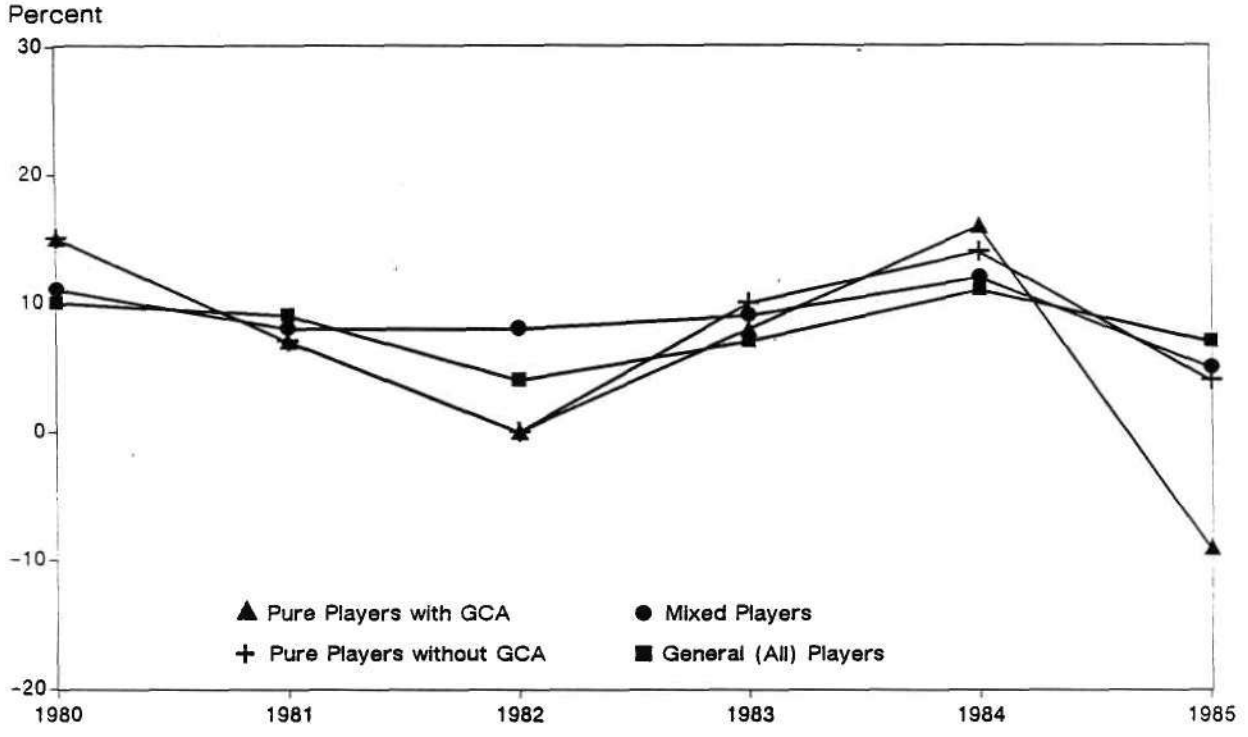
Figure 4

NET MARGIN



Source: Annual Reports, 1981 through 1985:
Applied Materials; ASM; GCA; KLA;
Lam Research; Machine Technology, Inc.;
Tylan; Silicon Valley Group; Plasma-Therm;
Varian; Eaton; General Signal; Materials Research Corp.;
Perkin-Elmer; and Veeco
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Table 2

SEMICONDUCTOR EQUIPMENT COMPANIES

Pure Players (with GCA)

	1980	1981	1982	1983	1984	1985
Current Ratio	1.86	2.09	1.87	3.03	2.82	1.46
Debt/Equity	28%	26%	25%	29%	29%	13%
Capital Spending/ Revenue	5%	9%	7%	8%	9%	12%
RD&E/Revenue	8%	11%	12%	14%	14%	18%
Gross Margin	44%	42%	37%	43%	49%	38%
Net Margin	15%	7%	0	8%	16%	(9%)

Mixed Players

	1980	1981	1982	1983	1984	1985
Current Ratio	2.37	2.45	2.48	2.56	2.38	1.92
Debt/Equity	42%	38%	24%	19%	20%	17%
Capital Spending/ Revenue	6%	6%	6%	6%	8%	7%
RD&E/Revenue	8%	8%	9%	10%	11%	10%
Gross Margin	31%	32%	39%	40%	42%	38%
Net Margin	11%	8%	8%	9%	12%	5%

(Continued)

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Table 2 (Continued)

SEMICONDUCTOR EQUIPMENT COMPANIES

General (All) Players

	1980	1981	1982	1983	1984	1985
Current Ratio	2.22	2.27	2.21	2.43	2.50	2.37
Debt/Equity	37%	36%	27%	24%	23%	22%
Capital Spending/ Revenue	5%	5%	4%	4%	5%	5%
RD&E/Revenue	4%	5%	5%	6%	6%	6%
Gross Margin	28%	29%	31%	32%	34%	31%
Net Margin	10%	9%	4%	7%	11%	7%

Source: Annual Reports, 1981 through 1985: Applied Materials; ASM; GCA; KLA; Lam Research; Machine Technology, Inc.; Tylan; Silicon Valley Group; Plasma-Therm; Varian; Eaton; General Signal; Materials Research Corp.; Perkin-Elmer; and Veeco
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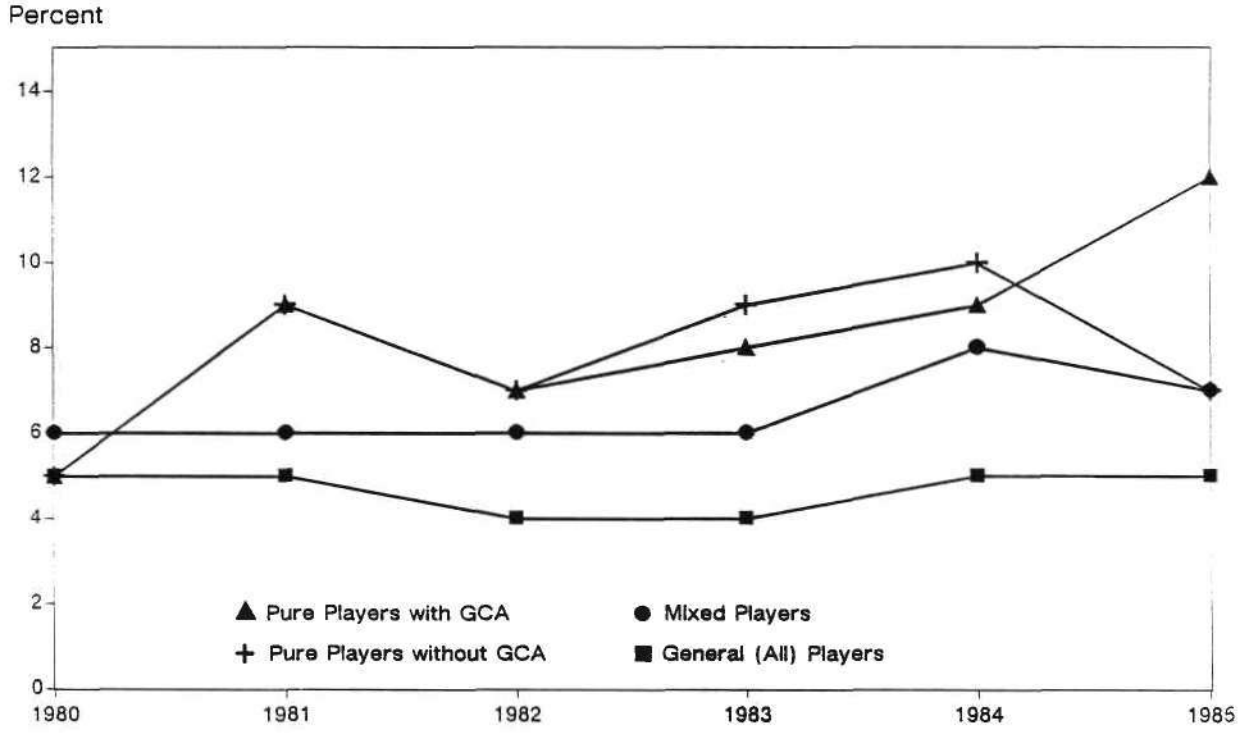
Figure 5

CAPITAL SPENDING/REVENUE



Source: Annual Reports, 1981 through 1985:
Applied Materials; ASM; GCA; KLA;
Lam Research; Machine Technology, Inc.;
Tylan; Silicon Valley Group; Plasma-Therm;
Varian; Eaton; General Signal; Materials Research Corp.;
Perkin-Elmer; and Veeco
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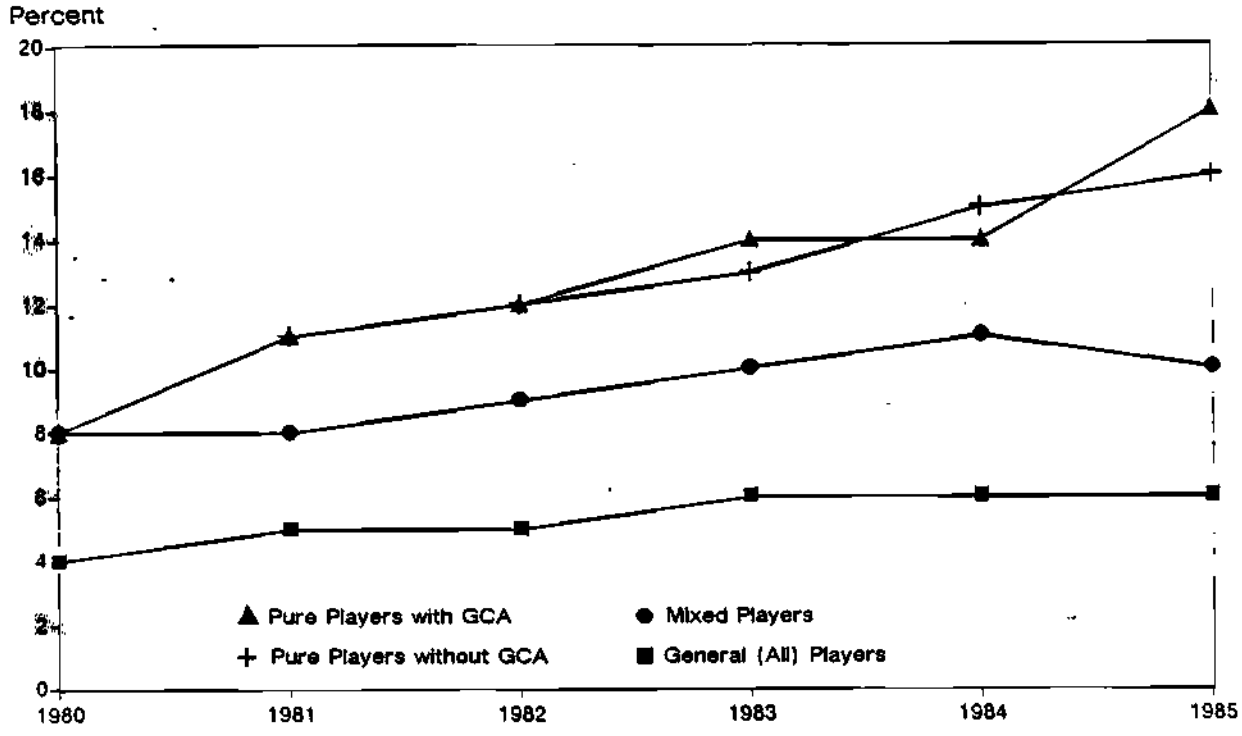
Figure 6

RD&E/REVENUE



Source: Annual Reports, 1981 through 1985:
Applied Materials; ASM; GCA; KLA;
Lam Research; Machine Technology, Inc.;
Tylan; Silicon Valley Group; Plasma-Therm;
Varian; Eaton; General Signal; Materials Research Corp.;
Perkin-Elmer; and Veeco
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Mixed Players

Companies in the mixed players category tend to be more focused on the semiconductor equipment industry. The financial aggregates of the mixed players basically paralleled those of the general players. Current ratios showed the same pattern of movement, though they have shown a somewhat heavier decline in the last two years. The mixed players, on average, had a lower debt/equity ratio than the general players, but the movements of both groups were roughly similar. The profitability ratios of the mixed players averaged higher than those of the general players, though their patterns of movement were similar. Strategic ratios (capital spending to revenue and RD&E to revenue) of the mixed players also showed the same relationship to general players: on average, higher, yet showing the same patterns of movement.

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Pure Players

Data for pure players are shown in Figures 1 through 6 with GCA included and excluded. The reason for this is that GCA has had some severe financial troubles, a situation that in some respects is unique to this company. Data excluding GCA may, therefore, be more indicative of the underlying dynamics of the industry than data including GCA. However, unless otherwise indicated, textual analysis of pure players will refer to ratios built on data that include GCA. The debt/equity ratio for pure players is an example of this: Without GCA, this ratio's movement is very similar to that of the ratio for the general and mixed players.

Financial aggregates for this (pure players) category tend to show more volatility than do the financial aggregates for the other categories. Net margins for the pure players have shown a great deal of volatility (see Figure 4). Gross margins for the pure players have, for the most part, been above those of either the general or the mixed players.

The current ratio for the pure players, excluding GCA, has shown a strong rise since 1980. This same rise is also evident if GCA is included. However, with GCA included the current ratio shows a sharp drop in 1985.

ANALYSIS

In broad terms, as one moves from the general and mixed players to the pure players, strategic ratios tend to rise. Pure players spend more, as a percent of revenue, on RD&E and on capital spending. This is a reflection of the fact that the semiconductor equipment industry is one of the most technology-intensive industries in the world, and one of the fastest changing. The increase in R&D as a percent of revenue, even when revenue declines, is due to the fact that R&D expenses once budgeted are hard to cut off quickly. Another reason is that because the industry is technology intense, equipment companies (or divisions) have to maintain R&D expenditures to maintain their life blood.

Gross margins also tend to rise as one moves from the general players toward the pure players. In general, semiconductor capital equipment manufacturers are able to command a premium price relative to the heterogeneous mix of goods sold by the general players. They are able to do this because competition in the semiconductor capital equipment industry is based primarily on quality, service, and reliability, and only secondarily on price.

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Financial Aggregates

However, the pure players' high gross margins are offset by the tendency for their net margins to react volatilely to the ups and downs of the business cycle. Pure players do not have the diverse markets that the mixed or general players have. Consequently, when the semiconductor business goes down, the pure players do not have another market to balance out the downturn. Additionally, there are some expenses, especially R&D expenses, as previously discussed that cannot be shut off quickly when sales turn down. R&D expenses are also hard to cut because equipment companies are technology intensive and, therefore, have to maintain relatively high R&D expenses.

Current ratios for the pure players have shown a tendency to rise since 1980. This is true not only when GCA is removed from the analysis, but also when SVG and Lam Research are removed. (Both SVG and Lam had current ratios significantly higher than the average. See Table 3.) This long-term tendency for the current ratio to rise is probably due to the increased need for working capital that is attendant on an increase in sales. The falls in the current ratio in 1982 and in 1984 were due to a working off of inventories as a result of increasing sales. In 1985, both current assets and current liabilities fell; current assets did not fall as much as current liabilities, as orders were cancelled in the second half of 1985, because of the difficulty in liquidating both work-in-process and finished goods inventories.

Table 3

PURE EQUIPMENT COMPANIES (WITHOUT GCA)

	1980	1981	1982	1983	1984	1985
Current Ratio	1.86	2.09	1.87	3.00	2.74	3.18
Debt/Equity	28%	26%	25%	11%	11%	10%
Capital Spending/ Revenue	5%	9%	7%	9%	10%	7%
RD&E/Revenue	8%	11%	12%	13%	15%	16%
Gross Margin	44%	42%	37%	44%	48%	47%
Net Margin	15%	7%	0	10%	14%	4%

Source: Annual Reports, 1981 through 1985: Applied Materials; ASM; GCA; KLA; Lam Research; Machine Technology, Inc.; Tylan; Silicon Valley Group; Plasma-Therm; Varian; Eaton; General Signal; Materials Research Corp.; Perkin-Elmer; and Veeco
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Debt/equity ratios for all three categories of players (GCA excluded) have behaved roughly the same, falling from a 1980 high to a plateau in 1983. This is due primarily to the recent decline in the inflation rate. During an inflationary period, since borrowers are able to repay debt with dollars that are worth less, debt is relatively more attractive.

Lower interest rates also make debt more attractive, and interest rates are now at their lowest point in many years. Current low interest rates can be expected to cause debt/equity ratios to rise, especially when business conditions improve and added capacity is needed.

Table 4 lists the individual ratios for the companies discussed.

Table 4

EQUIPMENT COMPANIES RATIOS

	1980	1981	1982	1983	1984	1985
Current Ratio						
Applied Materials	2.19	1.85	1.63	2.66	2.59	2.82
ASM	1.17	1.80	1.32	2.29	1.80	-
GCA	-	-	-	3.09	2.97	0.67
KLA	2.52	2.78	2.81	3.74	3.84	3.28
Lam	-	-	-	6.73	6.35	5.40
MTI	1.75	2.51	2.29	2.81	2.86	3.69
Tylan	2.82	4.09	3.75	3.44	2.98	1.67
SVG	2.77	3.42	5.92	8.92	8.54	8.04
Plasma-Therm	1.44	2.17	2.34	2.41	1.72	1.68
Varian	2.08	2.11	2.37	2.38	2.14	1.99
Eaton	2.11	1.98	1.69	2.25	2.67	3.22
General Signal	2.21	2.46	2.72	2.50	2.48	2.28
MRC	3.91	4.07	3.60	2.94	2.95	3.27
Perkin-Elmer	2.65	2.65	2.65	2.38	2.21	2.03
Veeco	2.51	3.30	3.18	3.11	2.84	3.78

(Continued)

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Table 4 (Continued)

EQUIPMENT COMPANIES RATIOS

	1980	1981	1982	1983	1984	1985
Debt/Equity						
Applied Materials	20%	39%	41%	26%	24%	21%
ASM	83%	23%	15%	4%	3%	-
GCA	-	37%	75%	72%	70%	(50%)
KLA	25%	10%	4%	1%	1%	0
Lam	-	-	-	0	0	0
MTI	6%	4%	14%	16%	2%	16%
Tylan	10%	7%	7%	26%	44%	11%
SVG	0	1%	1%	1%	1%	1%
Plasma-Therm	165%	78%	149%	26%	71%	70%
Varian	58%	48%	23%	11%	10%	11%
Eaton	51%	54%	47%	42%	37%	31%
General Signal	12%	11%	9%	9%	11%	14%
MRC	21%	32%	37%	15%	28%	47%
Perkin-Elmer	35%	31%	26%	21%	21%	21%
Veeco	16%	15%	14%	14%	15%	18%

	1980	1981	1982	1983	1984	1985
Gross Margin						
Applied Materials	45%	40%	29%	42%	49%	45%
ASM	39%	39%	39%	42%	43%	-
GCA	-	-	-	41%	51%	15%
KLA	48%	46%	49%	51%	53%	51%
Lam	-	-	36%	45%	50%	52%
MTI	48%	49%	47%	46%	51%	48%
Tylan	47%	42%	41%	42%	42%	36%
SVG	64%	60%	62%	62%	60%	59%
Plasma-Therm	30%	36%	30%	36%	36%	42%
Varian	28%	32%	34%	35%	35%	31%
Eaton	25%	26%	23%	26%	28%	26%
General Signal	32%	32%	32%	30%	31%	29%
MRC	31%	30%	30%	26%	33%	31%
Perkin-Elmer	43%	44%	43%	42%	43%	44%
Veeco	47%	45%	44%	46%	46%	42%

(Continued)

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Table 4 (Continued)

EQUIPMENT COMPANIES RATIOS

	1980	1981	1982	1983	1984	1985
Net Margin						
Applied Materials	14%	3%	(11%)	7%	15%	16%
ASM	13%	7%	6%	10%	10%	-
GCA	-	-	-	4%	20%	(69%)
KLA	15%	15%	18%	21%	22%	22%
Lam	-	-	(45%)	14%	23%	18%
MTI	21%	17%	7%	13%	21%	4%
Tylan	25%	13%	7%	6%	8%	2%
SVG	32%	28%	29%	34%	34%	28%
Plasma-Therm	6%	8%	(5%)	0	(10%)	(1%)
Varian	4.9%	0.9%	6.7%	10.7%	11.4%	4.8%
Eaton	7.1%	7.5%	(5.0%)	4.3%	11.7%	10.5%
General Signal	12.7%	12.9%	11.9%	9.8%	10.5%	4.5%
MRC	10.5%	4.9%	(1.0%)	(6.9%)	5.8%	0.9%
Perkin-Elmer	12.6%	12.1%	9.6%	8.3%	9.0%	9.6%
Veeco	19.7%	16.6%	14.3%	15.9%	15.7%	10.3%

	1980	1981	1982	1983	1984	1985
Capital Spending/Revenue						
Applied Materials	6%	11%	6%	8%	8%	7%
ASM	0	9%	11%	13%	14%	-
GCA	N/A	N/A	N/A	5%	7%	21%
KLA	7%	7%	7%	10%	9%	3%
Lam	N/A	0	7%	8%	7%	5%
MTI	5%	7%	4%	4%	7%	10%
Tylan	7%	7%	3%	4%	8%	6%
SVG	1%	2%	1%	3%	3%	2%
Plasma Therm	6%	6%	6%	6%	6%	3%
Varian	6%	6%	4%	5%	7%	9%
Eaton	5%	5%	4%	3%	4%	3%
General Signal	3%	3%	3%	4%	5%	4%
MRC	7%	6%	5%	8%	6%	13%
Perkin-Elmer	5%	5%	5%	5%	5%	-
Veeco	5%	4%	5%	5%	5%	5%

(Continued)

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Financial Aggregates

The semiconductor capital equipment industry is a technology-intense, fast-moving industry and will remain so for the foreseeable future. Strategic ratios have been rising for all three groups: general, mixed, and pure players. Capital spending as a percent of revenue for the pure players is now at 12 percent. RD&E as a percent of revenue for the pure players is now at 18 percent. Semiconductor manufacturers will continue to demand more reliability, higher throughput, the ability to process ever smaller geometries, while reducing equipment-generated particulates and achieving SECS compatibility. RD&E and capital expenditures will have to remain high to meet these demands.

Semiconductor equipment manufacturers will continue to seek creative ways to finance these expenditures, such as increased cooperativeness with semiconductor manufacturers and materials vendors, joint ventures, alliances, and RD&E cooperatives. These methods of cooperation reduce the risk because they share it. These methods also have the advantage of not appearing on the income statement. However, when business picks up and extra capacity is needed, we can expect to see the debt/equity ratio rise, since debt is interest sensitive. Additionally, if and when inflation does revive, we can expect even more upward pressure to be placed on debt/equity ratios.

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Financial Aggregates

Table 4 (Continued)

EQUIPMENT COMPANIES RATIOS

	1980	1981	1982	1983	1984	1985
RD&E/Revenue						
Applied Materials	12%	14%	16%	16%	18%	18%
ASM	2%	5%	7%	8%	10%	-
GCA	-	-	-	16%	14%	24%
KLA	12%	14%	14%	14%	16%	15%
Lam	-	-	34%	17%	15%	17%
MTI	1%	5%	9%	9%	11%	18%
Tylan	6%	10%	13%	13%	10%	9%
SVG	10%	8%	9%	9%	10%	13%
Plasma Therm	5%	6%	9%	10%	16%	15%
Varian	7%	6%	6%	6%	7%	8%
Eaton	3%	3%	4%	4%	3%	3%

N/A = Not Applicable

Source: Annual Reports, 1981 through 1985: Applied Materials; ASM; GCA; KLA; Lam Research; Machine Technology, Inc.; Tylan; Silicon Valley Group; Plasma-Therm; Varian; Eaton; General Signal; Materials Research Corp.; Perkin-Elmer; and Veeco
Dataquest
June 1986

DATAQUEST CONCLUSIONS

The behavior of financial and strategic ratios reflects the dynamics of the industry. Profitability ratios, especially the net margins of the pure players, reflect the ups and downs of the semiconductor industry. When they are up, they are very, very up--above those of the general and mixed players. When they are down, they are way down--below those of the general and mixed players. It is likely that profitability ratios for the pure players will continue to follow the cycle of the industry.

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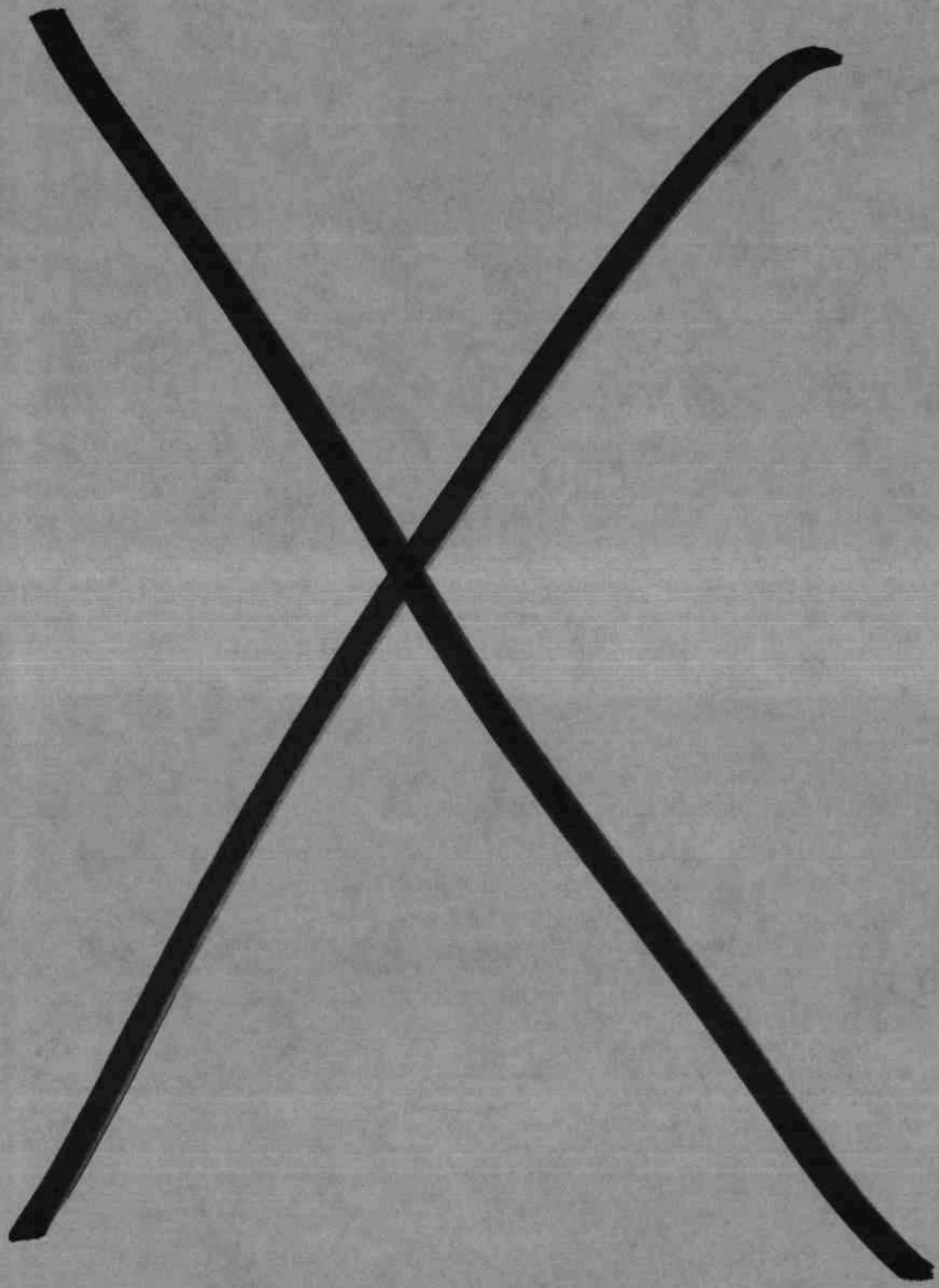

Equipment Data Base

The following is a list of the material in this section:

- Introduction to the Wafer Fab Equipment Data Base
- Wafer Fab Equipment--Summary Data by Category
- Wafer Fab Equipment--Import/Export Data
- Wafer Fab Equipment--Company Shares by Category
- Wafer Fab Equipment--Company Rankings

For additional information, please refer to the material behind the Equipment Data Base tab in your Newsletter binder.

Introduction to the Wafer Fab Equipment Database

Each year, Dataquest's Semiconductor Equipment and Materials Service (SEMS) publishes its Wafer Fab Equipment Database. This database is the result of an extensive research project conducted by SEMS whereby we contact the world's wafer fab equipment manufacturers to obtain detailed regional and company market share data.

Dataquest has organized the wafer fab equipment market into 11 major categories of front-end processing equipment. These categories, along with key subcategories, are shown in Table 1.

Table 1

Wafer Fab Equipment Categories

1. Lithography
   - Contact/Proximity
   - Projection Aligners
   - Steppers
   - Direct-Write Lithography
   - Maskmaking Lithography
   - X-Ray
2. Automatic Photoresist Processing Equipment
3. Etch and Clean
   - Wet Process
   - Dry Strip
   - Dry Etch
   - Ion Milling
4. Deposition
   - Chemical Vapor Deposition
   - Physical Vapor Deposition
   - Silicon Epitaxy
   - Metalorganic CVD
   - Molecular Beam Epitaxy
5. Diffusion
6. Rapid Thermal Processing
7. Ion Implantation
   - Medium Current
   - High Current
   - High Voltage
8. Optical CD/Wafer Inspection
9. Other Process Control
10. Factory Automation
11. Other Equipment

Source: Dataquest (June 1990)

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Dataquest estimates the capital spending by the world's merchant and captive semiconductor manufacturers and publishes this estimate in this binder, behind the "Forecast" tab. We consider capital spending to consist of three components: spending for front-end, or wafer fab equipment; spending for back-end, or assembly and test equipment; and spending for property and plant. Thus, the total world market for the 11 categories of wafer fab equipment defined above should be equal to the total capital spending for front-end equipment by the world's semiconductor manufacturers.

Most of the equipment categories are self-explanatory; however, a few categories require further definition. The Other Process Control category represents a broad market that includes mask inspection and repair equipment, process monitoring equipment, surface analysis equipment, and analytical instrumentation. This market is a highly fragmented market with dozens of companies selling into a multitude of noncompetitive market niches.

Factory Automation includes CIM software for shop floor control, factory host computer systems, cell controllers and interface hardware, and wafer transport systems including automatic guided vehicles, robotics, and rail transport systems.

Other Equipment is a general, catch-all category that includes the other capital equipment used throughout the fab but not classified with the other nine major types of wafer processing equipment. Included in this segment are decontamination systems, wafer markers, gas analyzers, storage stations, and other types of equipment.

CONVENTIONS

The data in the tables represent calendar year shipments, organized by company or by region. For companies with a different fiscal year, calendar year shipments have been estimated. Shipments do not include spare parts or service but do include retrofits and upgrades. Thus, for public companies, the sales reported here may be different from the sales reported in the annual reports. The compound annual growth rate (CAGR) is estimated over the years 1985 to 1989 for each major line item.

EXCHANGE RATES

Japanese-manufactured equipment sold in Japan is valued in dollars in the database tables at the average exchange rate for each year, as shown below:

Yen/Dollar Exchange Rate

1985	1986	1987	1988	1989
238	167	144	130	139

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It should be noted that Japanese equipment sold in Japan in 1986 reflects the high yen appreciation rate rather than a true increase in the total market.

EQUIPMENT COMPANIES

Table 2 presents a list of the equipment companies found in the database tables by region of company ownership. The database comprises a total of 80 US equipment companies, 47 Japanese companies, 29 European companies, and 6 joint venture companies. These 162 companies account for virtually all of the world's wafer processing equipment for lithography, automatic photoresist processing, etch and clean, deposition, diffusion, rapid thermal processing, ion implantation, and optical CD/wafer inspection.

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Table 2

1989 Wafer Fab Equipment Companies

North American Companies

Advantage Production Technology
AG Associates
Alameda Instruments
American Semiconductor Equip. Tech.
Applied Materials
Ateq
Athens
Automatic Cleaning Technology
Branson/IPC
BTU International
CFM Technology
CHA Industries
Crystal Specialties
CPA
CVC Products
CVD Equipment
Denton Vacuum
Dexon
Drytek
Eaton
Emcore
Epitaxy, Inc.
Estek
Focus Semiconductor
FSI International
Gasonics
GCA
General Signal Thinfilm Company
Genus
Hampshire Instruments
Innotec
Insystems
Integrated Air Systems
Ion Tech
IVS, Inc.
KLA Instruments
Kurt J. Lesker
Lam Research
LFE
Machine Technology, Inc.
Materials Research Corp.
Matrix
Micronix
Nanometrics
Nanoquest
Nanosil
National Electrostatics
Novellus
Optical Specialties, Inc.
Pacific Western
Peak Systems
Perkin-Elmer
Plasma-Therm
Poly-Flow Engineering
Process Products
Process Technology Ltd.
Pure Aire Corporation
Rapro
S&K Products International
Santa Clara Plastics
SCI Manufacturing
Semiconductor Systems, Inc.
Semifab
Semitherm
Semitool
Silicon Valley Group
SiScan Systems
Solitec
Spectrum CVD
Spire
Sputtered Films
Tegal
Tempress
Tylan
Ultratech
Universal Plastics
Varian
Veeco
Verteq
Watkins-Johnson

Japanese Companies

Amaya
Anelva
Canon
Chemitronics
Chlorine Engineering
Dainippon Screen
Daiwa Semiconductor
Denko
Disco
Eiko
Elionix
Enya
Ergo Plasma Systems
Fuji Electric
Hitachi
Hohkoh Sangyo
Japan Production Engineering
JEOL
Kaijo Denki
Kokusai Electric
Koyo Lindberg
Kuwano Electric
Musashi
Nidek
Nikon
Nippon EMC
Nippon Sanso
Nissin High Voltage
Olympus
Plasma Systems
Ramco
Ryokosha
Samco
Sankyo Engineering
Seiden Sha
Seiko
Shimada
Sugai
Sumitomo Metals
Tazmo
Tokuda
Tokyo Electron Ltd.
Tokyo Ohka
Toshiba
Toyoko Chemical
Ulvac
Ushio

(Continued)

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Table 2 (Continued)

1989 Wafer Fab Equipment Companies

European Companies

Aixtron	Heidelberg Instruments	Semco Engineering
ASM International	Helmut Seier	Sitesa
ASM Lithography	ISA Riber	Temescal
Balzers	Karl Süss	Thomas Schwonn
Cambridge Instruments	Leybold-Heraeus	VG Instruments
Centrotherm	LPE	Wellman Furnaces
Convac	Micro-Controle	Wild Leitz
CVT	MR Semicon	Wild Leitz Instruments
E.T. Electrotech	Plasma Technology	Zeiss
EEV	Pokorny	

Joint Venture Companies

Alcan Technology	Sumitomo/Eaton Nova	Ulvac/BTU
BTU/Ulvac	TEL/Varian	Varian/TEL

Source: Dataquest (June 1990)

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Wafer Fab Equipment—Summary Data by Category

This section of the equipment database consists of two summary tables for the worldwide fab equipment market. Both tables present sales by equipment category for the years 1985 to 1989. In Table 1, the annual sales for each equipment category are organized by region of equipment sales; in Table 2, annual sales for each equipment category are organized by equipment vendor nationality (United States, Japan, and Europe). Joint venture equipment companies have their own listing.

For example, the total worldwide sales for contact/proximity aligners of $47.8 million in 1985 is the same in both Table 1 and Table 2; however, whereas Table 1 breaks the sales down by region, Table 2 breaks the sales down by nationality of the companies supplying the aligners.

In Table 2, the subtotal fab equipment line item designates that portion of the total worldwide fab equipment market for which detailed company data are available. For some of the categories in Table 2 (Ion Milling, Other Process Control, Factory Automation, and Other Equipment), detailed company data are not yet complete. For these categories, top-down estimates have been made and included in Tables 1 and 2 so that world fab equipment sales are consistent across all tables. Detailed company data are available for approximately 85 percent of the total worldwide wafer fab equipment market for 1989.

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Table 1

Worldwide Wafer Fab Equipment Market
Regional Shares by Category
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Fab Equipment Market	3,355.6	2,709.9	3,135.0	4,937.1	5,886.8	15.1%
Lithography						
Contact/Proximity						
United States	15.6	11.1	10.0	8.9	7.3	(17.3%)
Japan	18.0	9.1	5.2	4.0	3.3	(34.6%)
Europe	7.1	6.0	5.0	5.4	6.0	(4.1%)
Rest of World	7.1	5.2	4.4	4.0	3.6	(15.6%)
Total Contact/Prox.	47.8	31.4	24.6	22.3	20.2	(19.4%)
Projection Aligners						
United States	118.1	98.4	66.4	60.7	22.4	(34.0%)
Japan	105.3	38.4	36.7	63.3	43.9	(19.6%)
Europe	30.6	24.6	17.3	16.3	13.0	(19.3%)
Rest of World	12.1	9.6	8.2	7.4	15.0	5.5%
Total Projection	266.1	171.0	128.6	147.7	94.3	(22.8%)
Steppers						
United States	134.8	152.8	184.0	280.0	344.0	26.4%
Japan	209.5	139.1	212.8	436.6	532.4	26.3%
Europe	54.9	45.7	58.5	90.0	112.2	19.6%
Rest of World	31.1	25.5	47.8	114.4	202.5	59.7%
Total Steppers	430.3	363.1	503.1	921.0	1,191.1	29.0%
Direct-Write Lithography						
United States	11.5	30.4	17.2	13.6	10.0	(3.4%)
Japan	10.0	29.2	32.7	35.9	34.2	36.0%
Europe	9.2	8.5	15.2	17.2	20.4	22.0%
Rest of World	0	0	2.0	2.0	5.2	NA
Total Direct-Write	30.7	68.1	67.1	68.7	69.8	22.8%
Maskmaking Lithography						
United States	39.1	27.0	13.6	16.0	12.2	(25.3%)
Japan	35.5	23.7	38.0	27.5	45.8	6.6%
Europe	4.0	0	13.0	7.6	9.4	23.8%
Rest of World	2.7	0	3.0	11.0	5.5	19.5%
Total Maskmaking	81.3	50.7	67.6	62.1	72.9	(2.7%)

(Continued)

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Table 1 (Continued)

Worldwide Wafer Fab Equipment Market
Regional Shares by Category
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
X-Ray						
United States	0	0	0	3.4	2.0	NA
Japan	0.8	0.8	0	1.6	0	(100.0%)
Europe	1.0	0	0	1.4	2.8	29.4%
Rest of World	0	0	0	0	0	NA
Total X-Ray	1.8	0.8	0	6.4	4.8	27.8%
Total Lithography						
United States	319.1	319.7	291.2	382.6	397.9	5.7%
Japan	379.1	240.3	325.4	568.9	659.6	14.9%
Europe	106.8	84.8	109.0	137.9	163.8	11.3%
Rest of World	53.0	40.3	65.4	138.8	231.8	44.6%
Total Lithography	858.0	685.1	791.0	1,228.2	1,453.1	14.1%
Automatic Photoresist Processing Equipment						
United States	68.5	59.0	60.9	78.0	91.1	7.4%
Japan	54.3	51.5	61.8	107.6	147.4	28.4%
Europe	22.3	27.1	28.5	36.5	38.6	14.7%
Rest of World	12.5	8.2	12.9	25.3	47.7	39.8%
Total Track	157.6	145.8	164.1	247.4	324.8	19.8%
Etch and Clean						
Wet Process						
United States	65.6	63.3	65.9	88.6	104.2	12.3%
Japan	62.8	72.6	69.9	97.4	127.1	19.3%
Europe	22.9	19.6	22.4	34.2	43.0	17.1%
Rest of World	5.9	6.4	10.2	20.2	31.3	51.8%
Total Wet Process	157.2	161.9	168.4	240.4	305.6	18.1%
Dry Strip						
United States	13.8	13.8	14.9	20.4	24.3	15.2%
Japan	16.7	15.6	33.9	63.0	75.1	45.6%
Europe	5.0	3.0	1.9	3.7	5.3	1.5%
Rest of World	3.0	2.0	4.6	7.3	11.5	39.9%
Total Dry Strip	38.5	34.4	55.3	94.4	116.2	31.8%

(Continued)

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Table 1 (Continued)

Worldwide Wafer Fab Equipment Market
Regional Shares by Category
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
Dry Etch						
United States	148.0	100.1	118.1	176.9	190.7	6.5%
Japan	102.0	82.3	113.0	239.0	305.4	31.5%
Europe	32.6	39.7	58.3	78.8	69.9	21.0%
Rest of World	17.0	15.0	18.0	51.1	69.6	42.2%
Total Dry Etch	299.6	237.1	307.4	545.8	635.6	20.7%
Ion Milling						
United States	2.2	3.7	3.7	4.0	3.0	8.1%
Japan	2.8	1.5	1.5	2.0	3.0	1.7%
Europe	1.5	1.6	1.6	2.0	3.0	18.9%
Rest of World	0	0	0	0	0	NA
Total Ion Milling	6.5	6.8	6.8	8.0	9.0	8.5%
Total Etch and Clean						
United States	229.6	180.9	202.6	289.9	322.2	8.8%
Japan	184.3	172.0	218.3	401.4	510.6	29.0%
Europe	62.0	63.9	84.2	118.7	121.2	18.2%
Rest of World	25.9	23.4	32.8	78.6	112.4	44.3%
Total Etch and Clean	501.8	440.2	537.9	888.6	1,066.4	20.7%
Deposition						
CVD						
United States	82.5	62.8	91.3	150.1	188.8	23.0%
Japan	110.2	95.3	95.6	184.3	243.2	21.9%
Europe	35.8	47.2	56.9	73.1	71.9	19.0%
Rest of World	18.0	14.6	16.0	48.7	76.3	43.5%
Total CVD	246.5	219.9	259.8	456.2	580.2	23.9%
PVD						
United States	113.4	95.2	96.8	108.1	117.8	1.0%
Japan	93.9	76.5	99.8	138.1	175.0	16.8%
Europe	45.0	48.2	40.7	36.0	47.4	1.3%
Rest of World	10.7	16.7	16.6	22.8	36.9	36.3%
Total PVD	263.0	236.6	253.9	305.0	377.1	9.4%

(Continued)

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Table 1 (Continued)

Worldwide Wafer Fab Equipment Market
Regional Shares by Category
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
Silicon Epitaxy						
United States	27.3	16.2	13.4	42.0	30.5	2.8%
Japan	26.2	13.5	13.0	23.5	17.2	(10.0%)
Europe	13.0	11.2	6.4	13.4	17.1	7.1%
Rest of World	5.0	5.4	2.7	5.6	6.9	8.4%
Total Silicon Epitaxy	71.5	46.3	35.5	84.5	71.7	0.1%
Metalorganic CVD						
United States	8.9	9.3	11.0	13.8	14.9	13.7%
Japan	11.5	16.0	14.1	16.9	16.6	9.6%
Europe	4.1	5.4	9.2	10.6	9.6	23.7%
Rest of World	0.3	0.7	0.3	0.7	2.7	73.2%
Total MOCVD	24.8	31.4	34.6	42.0	43.8	15.3%
Molecular Beam Epitaxy						
United States	21.3	24.3	19.7	21.3	20.8	(0.6%)
Japan	17.2	23.3	32.6	36.3	20.9	5.0%
Europe	11.8	16.4	11.7	19.0	23.7	19.0%
Rest of World	2.3	1.8	4.0	4.3	7.2	33.0%
Total MBE	52.6	65.8	68.0	80.9	72.6	8.4%
Total Deposition						
United States	253.4	207.8	232.2	335.3	372.8	10.1%
Japan	259.0	224.6	255.1	399.1	472.9	16.2%
Europe	109.7	128.4	124.9	152.1	169.7	11.5%
Rest of World	36.3	39.2	39.6	82.1	130.0	37.6%
Total Deposition	658.4	600.0	651.8	968.6	1,145.4	14.8%
Diffusion						
United States	67.0	45.0	37.1	84.6	85.6	6.3%
Japan	90.3	74.2	59.1	105.4	129.9	9.5%
Europe	35.5	31.2	39.2	46.9	45.2	6.2%
Rest of World	14.4	5.2	10.0	58.0	66.7	46.7%
Total Diffusion	207.2	155.6	145.4	294.9	327.4	12.1%

(Continued)

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Table 1 (Continued)

Worldwide Wafer Fab Equipment Market
Regional Shares by Category
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
Rapid Thermal Processing						
United States	5.8	7.0	10.1	11.7	10.4	15.7%
Japan	5.4	4.5	4.5	6.2	10.0	16.7%
Europe	2.2	2.6	2.7	3.2	4.1	16.8%
Rest of World	0.9	1.0	0.9	1.2	3.6	41.4%
Total RTP	14.3	15.1	18.2	22.3	28.1	18.4%
Ion Implantation						
Medium Current						
United States	35.9	15.8	9.9	17.4	24.4	(9.2%)
Japan	54.9	22.4	29.6	64.1	76.5	8.6%
Europe	22.6	10.4	15.1	17.9	9.7	(19.1%)
Rest of World	11.1	5.9	6.4	18.5	28.9	27.0%
Total Medium Current	124.5	54.5	61.0	117.9	139.5	2.9%
High Current						
United States	42.3	12.8	27.6	44.5	61.1	9.6%
Japan	85.7	16.8	46.3	139.4	160.1	16.9%
Europe	21.3	17.0	21.5	32.6	31.1	9.9%
Rest of World	17.5	7.9	11.5	24.6	53.3	32.1%
Total High Current	166.8	54.5	106.9	241.1	305.6	16.3%
High Voltage						
United States	0.9	8.4	8.1	6.2	7.4	69.3%
Japan	0	1.1	5.9	8.1	14.2	NA
Europe	1.2	0.3	4.0	4.1	0	(100.0%)
Rest of World	0	0	0	0	1.7	NA
Total High Voltage	2.1	9.8	18.0	18.4	23.3	82.5%
Total Implantation						
United States	79.1	37.0	45.6	68.1	92.9	4.1%
Japan	140.6	40.3	81.8	211.6	250.8	15.6%
Europe	45.1	27.7	40.6	54.6	40.8	(2.5%)
Rest of World	28.6	13.8	17.9	43.1	83.9	30.9%
Total Implantation	293.4	118.8	185.9	377.4	468.4	12.4%

(Continued)

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Table 1 (Continued)

Worldwide Wafer Fab Equipment Market
Regional Shares by Category
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
Optical CD/Wafer Inspection Equipment						
United States	23.9	29.3	39.1	69.1	71.2	31.4%
Japan	17.7	26.3	36.8	66.9	62.2	36.9%
Europe	9.0	10.5	16.5	25.7	32.4	37.7%
Rest of World	3.9	4.7	7.6	18.2	21.5	53.2%
Total Optical CD/Insp.	54.5	70.8	100.0	179.9	187.3	36.2%
Other Process Control						
United States	144.1	132.9	123.4	143.0	155.8	2.0%
Japan	158.8	104.8	135.0	191.1	218.2	8.3%
Europe	43.0	47.0	44.5	53.7	58.3	7.9%
Rest of World	22.1	18.0	29.2	39.2	52.7	24.3%
Total Other Process Control	368.0	302.7	332.1	427.0	485.0	7.1%
Factory Automation						
United States	23.0	21.0	24.0	26.0	37.0	12.6%
Japan	83.0	43.0	54.0	76.0	112.0	7.8%
Europe	15.0	14.0	17.0	17.0	25.0	13.6%
Rest of World	4.0	3.0	4.0	11.0	21.0	51.4%
Total Automation	125.0	81.0	99.0	130.0	195.0	11.8%
Other Equipment						
United States	44.0	37.7	38.7	54.0	59.3	7.7%
Japan	49.8	35.5	44.5	77.4	93.3	17.0%
Europe	16.3	15.9	18.4	23.4	25.0	11.3%
Rest of World	7.3	5.7	8.0	18.0	28.3	40.3%
Total Other Equipment	117.4	94.8	109.6	172.8	205.9	15.1%
Total Wafer Fab Equipment						
United States	1,257.5	1,077.3	1,104.9	1,542.3	1,696.2	7.8%
Japan	1,422.3	1,017.0	1,276.3	2,211.6	2,666.9	17.0%
Europe	466.9	453.1	525.5	669.7	724.1	11.6%
Rest of World	208.9	162.5	228.3	513.5	799.6	39.9%
Total Fab Equipment	3,355.6	2,709.9	3,135.0	4,937.1	5,886.8	15.1%

N/A = Not applicable
Source: Dataquest (June 1990), Ref: SUMMREG

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Table 2

Worldwide Wafer Fab Equipment Market Company Shares by Category (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Fab Equipment Market	3,355.6	2,709.9	3,135.0	4,937.1	5,886.8	15.1%
Lithography						
Contact/Proximity						
US Companies	0	0	0	0	0	NA
Japanese Companies	30.3	15.4	11.0	8.6	6.3	(32.5%)
European Companies	17.5	16.0	13.6	13.7	13.9	(5.6%)
Joint Venture Companies	0	0	0	0	0	NA
Total Contact/Proximity	47.8	31.4	24.6	22.3	20.2	(19.4%)
Projection Aligners						
US Companies	138.4	121.8	88.0	78.6	44.9	(24.5%)
Japanese Companies	127.7	49.2	40.6	69.1	49.4	(21.1%)
European Companies	0	0	0	0	0	NA
Joint Venture Companies	0	0	0	0	0	NA
Total Projection	266.1	171.0	128.6	147.7	94.3	(22.8%)
Steppers						
US Companies	217.0	154.2	124.5	198.0	147.2	(9.2%)
Japanese Companies	210.5	199.8	341.9	664.4	912.1	44.3%
European Companies	2.8	9.1	36.7	58.6	131.8	161.9%
Joint Venture Companies	0	0	0	0	0	NA
Total Steppers	430.3	363.1	503.1	921.0	1,191.1	29.0%
Direct-Write Lithography						
US Companies	0	6.4	9.6	12.8	9.6	NA
Japanese Companies	19.5	41.2	39.5	40.7	41.0	20.4%
European Companies	11.2	20.5	18.0	15.2	19.2	14.4%
Joint Venture Companies	0	0	0	0	0	NA
Total Direct-Write	30.7	68.1	67.1	68.7	69.8	22.8%

(Continued)

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Table 2 (Continued)

Worldwide Wafer Fab Equipment Market
Company Shares by Category
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
Maskmaking Lithography						
US Companies	64.8	36.0	28.6	38.2	38.4	(12.3%)
Japanese Companies	13.9	14.7	35.0	16.5	29.6	20.8%
European Companies	2.6	0	4.0	7.4	4.9	17.2%
Joint Venture Companies	0	0	0	0	0	NA
Total Maskmaking	81.3	50.7	67.6	62.1	72.9	(2.7%)
X-Ray						
US Companies	0.8	0.8	0	1.8	2.0	NA
Japanese Companies	0	0	0	0	0	NA
European Companies	1.0	0	0	4.6	2.8	29.4%
Joint Venture Companies	0	0	0	0	0	NA
Total X-Ray	1.8	0.8	0	6.4	4.8	27.8%
Total Lithography						
US Companies	421.0	319.2	250.7	329.4	242.1	(12.9%)
Japanese Companies	401.9	320.3	468.0	799.3	1,038.4	26.8%
European Companies	35.1	45.6	72.3	99.5	172.6	48.9%
Joint Venture Companies	0	0	0	0	0	NA
Total Lithography	858.0	685.1	791.0	1,228.2	1,453.1	14.1%
Automatic Photoresist Processing Equipment						
US Companies	93.3	81.0	80.2	93.4	106.8	3.4%
Japanese Companies	60.5	58.4	73.0	140.2	186.4	32.5%
European Companies	3.8	6.4	10.9	13.8	12.2	33.9%
Joint Venture Companies	0	0	0	0	19.4	NA
Total Track	157.6	145.8	164.1	247.4	324.8	19.8%
Wet Process						
US Companies	99.8	90.9	96.4	115.4	139.5	8.7%
Japanese Companies	55.4	67.9	67.7	120.3	157.9	29.9%
European Companies	2.0	3.1	4.3	4.7	8.2	42.3%
Joint Venture Companies	0	0	0	0	0	NA
Total Wet Process	157.2	161.9	168.4	240.4	305.6	18.1%

(Continued)

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Table 2 (Continued)

Worldwide Wafer Fab Equipment Market
Company Shares by Category
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
Dry Strip						
US Companies	22.6	20.0	22.1	34.4	37.1	13.2%
Japanese Companies	14.9	13.5	28.2	50.8	67.5	45.9%
European Companies	1.0	0	0	0	0	(100.0%)
Joint Venture Companies	0	0.9	5.0	9.2	11.6	NA
Total Dry Strip	38.5	34.4	55.3	94.4	116.2	31.8%
Dry Etch						
US Companies	202.6	176.1	210.3	372.6	383.4	17.3%
Japanese Companies	77.6	50.0	72.5	159.1	231.2	31.4%
European Companies	8.9	5.0	7.2	14.1	15.0	13.9%
Joint Venture Companies	10.5	6.0	17.4	0	6.0	(13.1%)
Total Dry Etch	299.6	237.1	307.4	545.8	635.6	20.7%
Deposition						
CVD						
US Companies	117.7	83.9	133.9	252.0	373.9	33.5%
Japanese Companies	44.6	48.3	39.1	102.2	114.6	26.6%
European Companies	68.2	80.1	78.0	98.5	84.7	5.6%
Joint Venture Companies	16.0	7.6	8.8	3.5	7.0	(18.7%)
Total CVD	246.5	219.9	259.8	456.2	580.2	23.9%
PVD						
US Companies	133.1	113.5	102.0	132.4	161.4	4.9%
Japanese Companies	75.6	75.2	102.7	129.7	161.2	20.8%
European Companies	54.3	47.9	49.2	42.9	54.5	0.1%
Joint Venture Companies	0	0	0	0	0	NA
Total PVD	263.0	236.6	253.9	305.0	377.1	9.4%
Silicon Epitaxy						
US Companies	63.4	42.7	33.4	66.2	48.8	(6.3%)
Japanese Companies	8.1	3.6	2.1	6.2	7.0	(3.6%)
European Companies	0	0	0	12.1	15.9	NA
Joint Venture Companies	0	0	0	0	0	NA
Total Silicon Epitaxy	71.5	46.3	35.5	84.5	71.7	0.1%

(Continued)

Table 2 (Continued)

Worldwide Wafer Fab Equipment Market
Company Shares by Category
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
Metalorganic CVD						
US Companies	6.4	8.9	10.2	13.1	13.7	21.0%
Japanese Companies	8.9	12.1	10.5	13.7	14.5	13.0%
European Companies	7.2	7.4	11.0	13.5	15.6	21.3%
Joint Venture Companies	2.3	3.0	2.9	1.7	0	(100.0%)
Total MOCVD	24.8	31.4	34.6	42.0	43.8	15.3%
Molecular Beam Epitaxy						
US Companies	13.2	18.0	17.1	20.3	17.2	6.8%
Japanese Companies	11.5	14.8	16.6	21.6	14.1	5.2%
European Companies	27.9	33.0	34.3	39.0	41.3	10.3%
Joint Venture Companies	0	0	0	0	0	NA
Total MBE	52.6	65.8	68.0	80.9	72.6	8.4%
Total Deposition						
US Companies	333.8	267.0	296.6	484.0	615.0	16.5%
Japanese Companies	148.7	154.0	171.0	273.4	311.4	20.3%
European Companies	157.6	168.4	172.5	206.0	212.0	7.7%
Joint Venture Companies	18.3	10.6	11.7	5.2	7.0	(21.4%)
Total Deposition	658.4	600.0	651.8	968.6	1,145.4	14.8%
Diffusion						
US Companies	97.7	63.3	65.3	115.3	115.7	4.3%
Japanese Companies	28.9	24.1	33.3	141.2	162.4	54.0%
European Companies	20.1	18.8	21.5	26.9	30.5	11.0%
Joint Venture Companies	60.5	49.4	25.3	11.5	18.8	(25.3%)
Total Diffusion	207.2	155.6	145.4	294.9	327.4	12.1%
Rapid Thermal Processing						
US Companies	11.1	11.9	16.3	19.3	21.2	17.6%
Japanese Companies	2.4	2.1	1.2	1.8	5.4	22.5%
European Companies	0.4	0.7	0.7	1.2	1.5	39.2%
Joint Venture Companies	0.4	0.4	0	0	0	(100.0%)
Total RTP	14.3	15.1	18.2	22.3	28.1	18.4%

(Continued)

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Table 2 (Continued)

Worldwide Wafer Fab Equipment Market
Company Shares by Category
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
Ion Implantation						
US Companies	197.5	82.5	107.0	197.6	235.8	4.5%
Japanese Companies	34.1	20.7	26.8	53.3	82.6	24.8%
European Companies	0	0	2.8	4.2	1.6	NA
Joint Venture Companies	61.8	15.6	49.3	122.3	148.4	24.5%
Total Implantation	293.4	118.8	185.9	377.4	468.4	12.4%
Optical CD/Wafer Inspection Equipment						
US Companies	28.2	36.9	45.8	90.8	114.7	42.0%
Japanese Companies	14.7	22.1	30.6	53.8	47.9	34.4%
European Companies	11.6	11.8	23.6	35.3	24.7	20.8%
Joint Venture Companies	0	0	0	0	0	NA
Total Optical CD/Insp.	54.5	70.8	100.0	179.9	187.3	36.2%
Subtotal Fab Equipment[1]						
US Companies	1,507.6	1,148.8	1,190.7	1,852.2	2,011.3	7.5%
Japanese Companies	839.1	733.1	972.3	1,793.2	2,291.1	28.5%
European Companies	240.5	259.8	315.8	405.7	478.3	18.8%
Joint Venture Companies	151.5	82.9	108.7	148.2	211.2	8.7%
Total	2,738.7	2,224.6	2,587.5	4,199.3	4,991.9	16.2%
Ion Milling						
All Companies	6.5	6.8	6.8	8.0	9.0	8.5%
Other Process Control						
All Companies	368.0	302.7	332.1	427.0	485.0	7.1%
Factory Automation						
All Companies	125.0	81.0	99.0	130.0	195.0	11.8%
Other Equipment						
All Companies	117.4	94.8	109.6	172.8	205.9	15.1%
Total Fab Equipment	3,355.6	2,709.9	3,135.0	4,937.1	5,886.8	15.1%

[1] Subtotal Fab Equipment does not include Ion Milling, Other Process Control, Factory Automation, and Other Equipment categories because detailed company data are not complete for these categories. Aggregate data for these categories are added to provide a consistent total for the worldwide wafer fab equipment market.

NA = Not applicable

Source: Dataquest (June 1990), Ref: SUMMSHR

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Wafer Fab Equipment—Import/Export Data

This section of the equipment database consists of two summary tables that provide information on the import/export markets for the worldwide wafer fab equipment market. In both Table 1 and Table 2, the worldwide fab equipment market total in millions of dollars is listed at the beginning of the table and followed by the subtotal for fab equipment. The subtotal fab equipment line item includes all of the front-end equipment categories for which detailed company analysis has been made and accounts for 85 percent of all front-end equipment for 1989. For some equipment categories (Ion Milling, Process Control, Factory Automation, and Other Equipment), detailed company analysis is not yet complete. For these categories, which account for the remaining 15 percent of wafer fab equipment, a top-down estimate has been made and included in Tables 1 and 2 so that worldwide fab equipment sales are consistent across all tables.

The subtotal fab equipment market includes all of the major wafer fab equipment categories and accounts for the majority of all import/export activity in the worldwide fab equipment market. Relatively little import/export activity exists for the remaining 15 percent of wafer fab equipment for which detailed company data are not yet complete. These equipment markets are largely supplied by domestic suppliers. Significant import/export analysis of the fab equipment market can be done, however, with the aid of the data in Tables 1 and 2.

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Table 1

Worldwide Wafer Fab Equipment Market Import Data
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Fab Equipment Market	3,355.6	2,709.9	3,135.0	4,937.1	5,886.8	15.1%
Subtotal Fab Equipment*	2,738.7	2,224.6	2,587.5	4,199.3	4,991.9	16.2%
Subtotal Percentage	81.6%	82.1%	82.5%	85.1%	84.8%	
Subtotal Fab Equipment						
United States						
US Co. Sales	880.6	716.2	691.2	998.0	1,005.1	3.4%
Japanese Co. Sales	78.4	78.5	116.7	169.2	224.3	30.1%
European Co. Sales	85.2	87.3	107.2	148.1	183.3	21.1%
Joint Venture Co. Sales	0	0	0	0	28.4	NA
Total US Market	1,044.2	882.0	915.1	1,315.3	1,441.1	8.4%
Japan						
US Co. Sales	233.3	131.2	148.7	317.9	362.6	11.7%
Japanese Co. Sales	706.2	580.2	746.1	1,355.4	1,659.0	23.8%
European Co. Sales	36.9	37.9	37.8	43.6	42.5	3.6%
Joint Venture Co. Sales	151.5	82.9	108.7	148.2	176.3	3.9%
Total Japan Market	1,127.9	832.2	1,041.3	1,865.1	2,240.4	18.7%
Europe						
US Co. Sales	257.9	212.1	240.1	312.0	317.3	5.3%
Japanese Co. Sales	28.3	40.5	52.2	79.9	94.8	35.3%
European Co. Sales	104.9	122.0	151.7	181.7	194.2	16.6%
Joint Venture Co. Sales	0	0	0	0	6.5	NA
Total Europe Market	391.1	374.6	444.0	573.6	612.8	11.9%
Rest of World						
US Co. Sales	135.8	89.3	110.7	224.3	326.3	24.5%
Japanese Co. Sales	26.2	33.9	57.3	188.7	313.0	85.9%
European Co. Sales	13.5	12.6	19.1	32.3	58.3	44.2%
Joint Venture Co. Sales	0	0	0	0	0	NA
Total ROW Market	175.5	135.8	187.1	445.3	697.6	41.2%

(Continued)

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Table 1 (Continued)

Worldwide Wafer Fab Equipment Market Import Data
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
Worldwide						
US Co. Sales	1,507.6	1,148.8	1,190.7	1,852.2	2,011.3	7.5%
Japanese Co. Sales	839.1	733.1	972.3	1,793.2	2,291.1	28.5%
European Co. Sales	240.5	259.8	315.8	405.7	478.3	18.8%
Joint Venture Co. Sales	151.5	82.9	108.7	148.2	211.2	8.7%
Subtotal Fab Equipment	2,738.7	2,224.6	2,587.5	4,199.3	4,991.9	16.2%
Ion Milling						
All Companies	6.5	6.8	6.8	8.0	9.0	8.5%
Process Control						
All Companies	368.0	302.7	332.1	427.0	485.0	7.1%
Factory Automation						
All Companies	125.0	81.0	99.0	130.0	195.0	11.8%
Other Equipment						
All Companies	117.4	94.8	109.6	172.8	205.9	15.1%
Total Fab Equipment	3,355.6	2,709.9	3,135.0	4,937.1	5,886.8	15.1%

NA = Not available
*Subtotal Fab Equipment does not include Ion Milling, Other Process Control, Factory Automation, and Other Equipment categories because detailed company data are not complete for these categories. Aggregate data for these categories are added to provide a consistent total for the worldwide wafer fab equipment market.
Source: Dataquest (June 1990), Ref: IMEXSHR

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Table 2

Worldwide Wafer Fab Equipment Market Export Data
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Fab Equipment Market	3,355.6	2,709.9	3,135.0	4,937.1	5,886.8	15.1%
Subtotal Fab Equipment*	2,738.7	2,224.6	2,587.5	4,199.3	4,991.9	16.2%
Subtotal Percentage	81.6%	82.1%	82.5%	85.1%	84.8%	
Subtotal Fab Equipment						
US Equipment Companies						
Sales in United States	880.6	716.2	691.2	998.0	1,005.1	3.4%
Sales in Japan	233.3	131.2	148.7	317.9	362.6	11.7%
Sales in Europe	257.9	212.1	240.1	312.0	317.3	5.3%
Sales in ROW	135.8	89.3	110.7	224.3	326.3	24.5%
Total US Cos.	1,507.6	1,148.8	1,190.7	1,852.2	2,011.3	7.5%
Japanese Equipment Companies						
Sales in United States	78.4	78.5	116.7	169.2	224.3	30.1%
Sales in Japan	706.2	580.2	746.1	1,355.4	1,659.0	23.8%
Sales in Europe	28.3	40.5	52.2	79.9	94.8	35.3%
Sales in ROW	26.2	33.9	57.3	188.7	313.0	85.9%
Total Japanese Cos.	839.1	733.1	972.3	1,793.2	2,291.1	28.5%
European Equipment Companies						
Sales in United States	85.2	87.3	107.2	148.1	183.3	21.1%
Sales in Japan	36.9	37.9	37.8	43.6	42.5	3.6%
Sales in Europe	104.9	122.0	151.7	181.7	194.2	16.6%
Sales in ROW	13.5	12.6	19.1	32.3	58.3	44.2%
Total European Cos.	240.5	259.8	315.8	405.7	478.3	18.8%
Joint Venture Equipment Companies						
Sales in United States	0	0	0	0	28.4	NA
Sales in Japan	151.5	82.9	108.7	148.2	176.3	3.9%
Sales in Europe	0	0	0	0	6.5	NA
Sales in ROW	0	0	0	0	0	NA
Total JV Companies	151.5	82.9	108.7	148.2	211.2	8.7%
Subtotal Fab Equipment	2,738.7	2,224.6	2,587.5	4,199.3	4,991.9	16.2%

(Continued)

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Table 2 (Continued)

Worldwide Wafer Fab Equipment Market Export Data
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
Ion Milling						
All Companies	6.5	6.8	6.8	8.0	9.0	8.5%
Other Process Control						
All Companies	368.0	302.7	332.1	427.0	485.0	7.1%
Factory Automation						
All Companies	125.0	81.0	99.0	130.0	195.0	11.8%
Other Equipment						
All Companies	117.4	94.8	109.6	172.8	205.9	15.1%
Total Fab Equipment	3,355.6	2,709.9	3,135.0	4,937.1	5,886.8	15.1%

NA = Not available
*Subtotal Fab Equipment does not include Ion Milling, Other Process Control, Factory Automation, and Other Equipment categories because detailed company data are not complete for these categories. Aggregate data for these categories are added to provide a consistent total for the worldwide wafer fab equipment market.
Source: Dataquest (June 1990), Ref: IMEXSHR

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Wafer Fab Equipment—Company Shares by Category

This section of the equipment database contains detailed company market share data by region for the major front-end equipment categories as shown in Tables 1 through 57. All of the companies that participate in an equipment segment are listed for each region, regardless of whether or not they have sales in a particular region. Although this approach results in a large number of zeros in the tables, it also indicates that Dataquest has not recorded any sales for the company in that region. We believe that this format gives more positive information than eliminating a company with no sales in a given region.

At the beginning of each table, the total world market for a particular equipment category is presented. This total is the same for each category as the total listed in Tables 1 and 2 in the service section entitled "Wafer Fab Equipment—Summary Data by Category." Thus, all tables are completely consistent as one proceeds from the summary tables to the detailed tables presented here in this section.

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Table 1

Total Lithography Company Shares Worldwide (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Lithography Market	858.0	685.1	791.0	1,228.2	1,453.1	14.1%
Contact/Proximity						
Canon	30.3	15.4	11.0	8.6	6.3	
Karl Suss	17.5	16.0	13.6	13.7	13.9	
Total Cont./Prox.	47.8	31.4	24.6	22.3	20.2	(19.4%)
Projection Aligners						
Canon	127.7	49.2	40.6	69.1	49.4	
Perkin-Elmer	138.4	121.8	88.0	78.6	44.9	
Total Projection	266.1	171.0	128.6	147.7	94.3	(22.8%)
Steppers						
ASET	8.1	11.6	11.3	16.0	4.0	
ASM Lithography	2.8	9.1	36.7	58.6	131.8	
Canon	35.0	63.2	89.8	125.0	182.9	
Eaton	21.8	2.1	0	0	0	
GCA	114.2	74.6	47.4	104.0	68.9	
Hitachi	17.9	8.2	33.3	49.2	75.5	
Perkin-Elmer	22.2	27.0	25.2	5.0	12.0	
Nikon	157.6	128.4	218.8	490.2	653.7	
Ultratech	50.7	38.9	40.6	73.0	62.3	
Total Steppers	430.3	363.1	503.1	921.0	1,191.1	29.0%
Direct-Write Lithography						
ASM Lithography	1.9	6.0	8.0	7.2	7.2	
Cambridge	9.3	14.5	10.0	8.0	12.0	
Hitachi	5.3	11.2	8.7	9.6	9.4	
JEOL	14.2	30.0	30.8	31.1	31.6	
Perkin-Elmer	0	6.4	9.6	12.8	9.6	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Direct-Write	30.7	68.1	67.1	68.7	69.8	22.8%

(Continued)

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Table 1 (Continued)

Total Lithography Company Shares Worldwide (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Lithography Market	858.0	685.1	791.0	1,228.2	1,453.1	14.1%
Maskmaking Lithography						
ASM Lithography	0	0	4.0	2.4	2.4	
Ateq	0	0	1.6	11.2	20.4	
Cambridge	2.6	0	0	5.0	2.5	
Hitachi	5.7	0	13.4	3.8	6.6	
JEOL	8.2	11.7	18.1	5.0	15.8	
Perkin-Elmer	64.8	36.0	27.0	27.0	18.0	
Toshiba	0	3.0	3.5	7.7	7.2	
Varian	0	0	0	0	0	
Total Maskmaking	81.3	50.7	67.6	62.1	72.9	(2.7%)
X-Ray						
Hampshire Instruments	0	0	0	1.8	0	
Micronix	0.8	0.8	0	0	0	
Perkin-Elmer	0	0	0	0	2.0	
Karl Suss	1.0	0	0	4.6	2.8	
Total X-Ray	1.8	0.8	0	6.4	4.8	27.8%
Total Lithography	858.0	685.1	791.0	1,228.2	1,453.1	14.1%

Source: Dataquest (June 1990), Ref: LITHSHR

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Table 2

Contact/Proximity Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Cont./Prox. Market	47.8	31.4	24.6	22.3	20.2	(19.4%)
United States						
Canon	7.8	5.6	4.5	3.0	1.4	
Karl Suss	7.8	5.5	5.5	5.9	5.9	
Total United States	15.6	11.1	10.0	8.9	7.3	(17.3%)
Japan						
Canon	14.7	5.2	3.6	2.7	2.7	
Karl Suss	3.3	3.9	1.6	1.3	0.6	
Total Japan	18.0	9.1	5.2	4.0	3.3	(34.6%)
Europe						
Canon	3.9	2.6	1.5	1.5	0.8	
Karl Suss	3.2	3.4	3.5	3.9	5.2	
Total Europe	7.1	6.0	5.0	5.4	6.0	(4.1%)
Rest of World						
Canon	3.9	2.0	1.4	1.4	1.4	
Karl Suss	3.2	3.2	3.0	2.6	2.2	
Total Rest of World	7.1	5.2	4.4	4.0	3.6	(15.6%)
Worldwide						
Canon	30.3	15.4	11.0	8.6	6.3	
Karl Suss	17.5	16.0	13.6	13.7	13.9	
Total Worldwide	47.8	31.4	24.6	22.3	20.2	(19.4%)

Source: Dataquest (June 1990), Ref: CONTSHR

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Table 3

Projection Aligner Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Projection Market	266.1	171.0	128.6	147.7	94.3	(22.8%)
United States						
Canon	22.0	13.6	8.4	12.0	8.4	
Perkin-Elmer	96.1	84.8	58.0	48.7	14.0	
Total United States	118.1	98.4	66.4	60.7	22.4	(34.0%)
Japan						
Canon	90.3	25.4	21.7	52.3	36.0	
Perkin-Elmer	15.0	13.0	15.0	11.0	7.9	
Total Japan	105.3	38.4	36.7	63.3	43.9	(19.6%)
Europe						
Canon	9.9	6.4	6.3	3.2	2.5	
Perkin-Elmer	20.7	18.2	11.0	13.1	10.5	
Total Europe	30.6	24.6	17.3	16.3	13.0	(19.3%)
Rest of World						
Canon	5.5	3.8	4.2	1.6	2.5	
Perkin-Elmer	6.6	5.8	4.0	5.8	12.5	
Total Rest of World	12.1	9.6	8.2	7.4	15.0	5.5%
Worldwide						
Canon	127.7	49.2	40.6	69.1	49.4	
Perkin-Elmer	138.4	121.8	88.0	78.6	44.9	
Total Worldwide	266.1	171.0	128.6	147.7	94.3	(22.8%)

Source: Dataquest (June 1990), Ref: PROJSHR

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Table 4

Stepper Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Stepper Market	430.3	363.1	503.1	921.0	1,191.1	29.0%
United States						
ASET	7.3	11.6	10.4	14.0	4.0	
ASM Lithography	2.1	5.8	19.6	39.0	88.4	
Canon	4.5	21.6	25.2	25.0	31.2	
Eaton	9.3	2.1	0	0	0	
GCA	42.1	46.4	36.7	80.6	53.0	
Hitachi	0	0	0	0	0	
Perkin-Elmer	16.4	23.1	18.0	5.0	12.0	
Nikon	20.7	14.8	44.0	71.5	112.0	
Ultratech	32.4	27.4	30.1	44.9	43.4	
Total United States	134.8	152.8	184.0	280.0	344.0	26.4%
Japan						
ASET	0	0	0	0	0	
ASM Lithography	0	0	0	0	0	
Canon	25.3	20.9	24.1	45.0	64.7	
Eaton	11.1	0	0	0	0	
GCA	25.7	9.6	4.4	3.9	0	
Hitachi	17.2	8.2	33.3	49.2	75.5	
Perkin-Elmer	0	0	0	0	0	
Nikon	128.6	98.8	151.0	336.2	390.5	
Ultratech	1.6	1.6	0	2.3	1.7	
Total Japan	209.5	139.1	212.8	436.6	532.4	26.3%
Europe						
ASET	0.8	0	0.9	0	0	
ASM Lithography	0.7	3.3	17.1	16.9	24.8	
Canon	5.2	15.3	18.0	20.0	37.5	
Eaton	1.4	0	0	0	0	
GCA	28.1	16.7	6.3	18.2	15.9	
Hitachi	0	0	0	0	0	
Perkin-Elmer	5.8	0	2.7	0	0	
Nikon	1.4	3.7	6.2	22.0	25.2	
Ultratech	11.5	6.7	7.3	12.9	8.8	
Total Europe	54.9	45.7	58.5	90.0	112.2	19.6%

(Continued)

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Table 4 (Continued)

Stepper Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Stepper Market	430.3	363.1	503.1	921.0	1,191.1	29.0%
Rest of World						
ASET	0	0	0	2.0	0	
ASM Lithography	0	0	0	2.7	18.6	
Canon	0	5.4	22.5	35.0	49.5	
Eaton	0	0	0	0	0	
GCA	18.3	1.9	0	1.3	0	
Hitachi	0.7	0	0	0	0	
Perkin-Elmer	0	3.9	4.5	0	0	
Nikon	6.9	11.1	17.6	60.5	126.0	
Ultratech	5.2	3.2	3.2	12.9	8.4	
Total Rest of World	31.1	25.5	47.8	114.4	202.5	59.7%
Worldwide						
ASET	8.1	11.6	11.3	16.0	4.0	
ASM Lithography	2.8	9.1	36.7	58.6	131.8	
Canon	35.0	63.2	89.8	125.0	182.9	
Eaton	21.8	2.1	0	0	0	
GCA	114.2	74.6	47.4	104.0	68.9	
Hitachi	17.9	8.2	33.3	49.2	75.5	
Perkin-Elmer	22.2	27.0	25.2	5.0	12.0	
Nikon	157.6	128.4	218.8	490.2	653.7	
Ultratech	50.7	38.9	40.6	73.0	62.3	
Total Worldwide	430.3	363.1	503.1	921.0	1,191.1	29.0%

Source: Dataquest (June 1990), Ref: STEPSHR

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Table 5

Stepper Company Shares Regional (Units)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Stepper Market	680	456	520	833	954	8.8%
United States						
ASET	9	14	11	14	4	
ASM Lithography	3	7	16	30	57	
Canon	7	22	28	25	25	
Eaton	13	3	0	0	0	
GCA	60	72	41	62	40	
Hitachi	0	0	0	0	0	
Perkin-Elmer	17	24	20	5	3	
Nikon	30	20	50	65	80	
Ultratech	62	44	37	41	45	
Total United States	201	206	203	242	254	6.0%
Japan						
ASET	0	0	0	0	0	
ASM Lithography	0	0	0	0	0	
Canon	39	20	20	45	60	
Eaton	17	0	0	0	0	
GCA	42	10	4	3	0	
Hitachi	24	9	30	40	70	
Perkin-Elmer	0	0	0	0	0	
Nikon	225	110	148	310	325	
Ultratech	3	3	0	3	2	
Total Japan	350	152	202	401	457	6.9%
Europe						
ASET	1	0	1	0	0	
ASM Lithography	1	4	14	13	16	
Canon	8	17	20	20	30	
Eaton	2	0	0	0	0	
GCA	40	26	7	14	12	
Hitachi	0	0	0	0	0	
Perkin-Elmer	6	0	3	0	0	
Nikon	2	5	7	20	18	
Ultratech	22	12	9	14	10	
Total Europe	82	64	61	81	86	1.2%

(Continued)

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Table 5 (Continued)

Stepper Company Shares
Regional
(Units)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Stepper Market	680	456	520	833	954	8.8%
Rest of World						
ASET	0	0	0	2	0	
ASM Lithography	0	0	0	2	12	
Canon	0	6	25	35	45	
Eaton	0	0	0	0	0	
GCA	26	3	0	1	0	
Hitachi	1	0	0	0	0	
Perkin-Elmer	0	4	5	0	0	
Nikon	10	15	20	55	90	
Ultratech	10	6	4	14	10	
Total Rest of World	47	34	54	109	157	35.2%
Worldwide						
ASET	10	14	12	16	4	
ASM Lithography	4	11	30	45	85	
Canon	54	65	93	125	160	
Eaton	32	3	0	0	0	
GCA	168	111	52	80	52	
Hitachi	25	9	30	40	70	
Perkin-Elmer	23	28	28	5	3	
Nikon	267	150	225	450	513	
Ultratech	97	65	50	72	67	
Total Worldwide	680	456	520	833	954	8.8%

Source: Dataquest (June 1990), Ref: STEPUNIT

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Table 6

Direct-Write Lithography Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Direct-Write Market	30.7	68.1	67.1	68.7	69.8	22.8%
United States						
ASM Lithography	1.9	4.0	4.0	2.4	0	
Cambridge Instruments	2.6	10.0	4.0	2.0	4.0	
Hitachi	0	0	0	0	0	
JEOL	7.0	10.0	6.0	6.0	6.0	
Perkin-Elmer	0	6.4	3.2	3.2	0	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total United States	11.5	30.4	17.2	13.6	10.0	(3.4%)
Japan						
ASM Lithography	0	0	0	0	0	
Cambridge Instruments	0	0	0	0	0	
Hitachi	5.3	11.2	8.7	9.6	9.4	
JEOL	4.7	18.0	20.8	23.1	21.6	
Perkin-Elmer	0	0	3.2	3.2	3.2	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Japan	10.0	29.2	32.7	35.9	34.2	36.0%
Europe						
ASM Lithography	0	2.0	4.0	4.8	7.2	
Cambridge Instruments	6.7	4.5	4.0	4.0	6.0	
Hitachi	0	0	0	0	0	
JEOL	2.5	2.0	4.0	2.0	4.0	
Perkin-Elmer	0	0	3.2	6.4	3.2	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Europe	9.2	8.5	15.2	17.2	20.4	22.0%

(Continued)

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Table 6 (Continued)

Direct-Write Lithography Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Direct-Write Market	30.7	68.1	67.1	68.7	69.8	22.8%
Rest of World						
ASM Lithography	0	0	0	0	0	
Cambridge Instruments	0	0	2.0	2.0	2.0	
Hitachi	0	0	0	0	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	0	0	0	0	3.2	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Rest of World	0	0	2.0	2.0	5.2	NA
Worldwide						
ASM Lithography	1.9	6.0	8.0	7.2	7.2	
Cambridge Instruments	9.3	14.5	10.0	8.0	12.0	
Hitachi	5.3	11.2	8.7	9.6	9.4	
JEOL	14.2	30.0	30.8	31.1	31.6	
Perkin-Elmer	0	6.4	9.6	12.8	9.6	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Worldwide	30.7	68.1	67.1	68.7	69.8	22.8%

NA = Not applicable
Source: Dataquest (June 1990), Ref: DWLTHSHR

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Table 7

Direct-Write Lithography Company Shares
Regional
(Units)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Direct-Write Market	16	27	24	22	24	10.7%
United States						
ASM Lithography	1	2	2	1	0	
Cambridge Instruments	2	5	2	1	2	
Hitachi	0	0	0	0	0	
JEOL	4	5	3	3	3	
Perkin-Elmer	0	2	1	1	0	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total United States	7	14	8	6	5	(8.1%)
Japan						
ASM Lithography	0	0	0	0	0	
Cambridge Instruments	0	0	0	0	0	
Hitachi	2	3	2	2	2	
JEOL	2	5	5	5	5	
Perkin-Elmer	0	0	1	1	1	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Japan	4	8	8	8	8	18.9%
Europe						
ASM Lithography	0	1	2	2	3	
Cambridge Instruments	4	3	2	2	3	
Hitachi	0	0	0	0	0	
JEOL	1	1	2	1	2	
Perkin-Elmer	0	0	1	2	1	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Europe	5	5	7	7	9	15.8%

(Continued)

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Table 7 (Continued)

Direct-Write Lithography Company Shares
Regional
(Units)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Direct-Write Market	16	27	24	22	24	10.7%
Rest of World						
ASM Lithography	0	0	0	0	0	
Cambridge Instruments	0	0	1	1	1	
Hitachi	0	0	0	0	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	0	0	0	0	1	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Rest of World	0	0	1	1	2	NA
Worldwide						
ASM Lithography	1	3	4	3	3	
Cambridge Instruments	6	8	5	4	6	
Hitachi	2	3	2	2	2	
JEOL	7	11	10	9	10	
Perkin-Elmer	0	2	3	4	3	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Worldwide	16	27	24	22	24	10.7%

NA = Not applicable
Source: Dataquest (June 1990), Ref: DWUNITS

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Table 8

Maskmaking Lithography Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Maskmaking Market	81.3	50.7	67.6	62.1	72.9	(2.7%)
United States						
ASM Lithography	0	0	0	2.4	2.4	
Ateq	0	0	1.6	1.6	6.8	
Cambridge Instruments	1.3	0	0	0	0	
Hitachi	0	0	0	0	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	37.8	27.0	12.0	12.0	3.0	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total United States	39.1	27.0	13.6	16.0	12.2	(25.3%)
Japan						
ASM Lithography	0	0	0	0	0	
Ateq	0	0	0	8.0	10.2	
Cambridge Instruments	0	0	0	0	0	
Hitachi	5.7	0	10.4	3.8	6.6	
JEOL	8.2	11.7	18.1	5.0	15.8	
Perkin-Elmer	21.6	9.0	6.0	3.0	6.0	
Toshiba	0	3.0	3.5	7.7	7.2	
Varian	0	0	0	0	0	
Total Japan	35.5	23.7	38.0	27.5	45.8	6.6%
Europe						
ASM Lithography	0	0	4.0	0	0	
Ateq	0	0	0	1.6	3.4	
Cambridge Instruments	1.3	0	0	0	0	
Hitachi	0	0	3.0	0	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	2.7	0	6.0	6.0	6.0	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Europe	4.0	0	13.0	7.6	9.4	23.8%

(Continued)

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Table 8 (Continued)

Maskmaking Lithography Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Maskmaking Market	81.3	50.7	67.6	62.1	72.9	(2.7%)
Rest of World						
ASM Lithography	0	0	0	0	0	
Ateq	0	0	0	0	0	
Cambridge Instruments	0	0	0	5.0	2.5	
Hitachi	0	0	0	0	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	2.7	0	3.0	6.0	3.0	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Rest of World	2.7	0	3.0	11.0	5.5	19.5%
Worldwide						
ASM Lithography	0	0	4.0	2.4	2.4	
Ateq	0	0	1.6	11.2	20.4	
Cambridge Instruments	2.6	0	0	5.0	2.5	
Hitachi	5.7	0	13.4	3.8	6.6	
JEOL	8.2	11.7	18.1	5.0	15.8	
Perkin-Elmer	64.8	36.0	27.0	27.0	18.0	
Toshiba	0	3.0	3.5	7.7	7.2	
Varian	0	0	0	0	0	
Total Worldwide	81.3	50.7	67.6	62.1	72.9	(2.7%)

Source: Dataquest (June 1990), Ref: MMLTHSHR

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Table 9

Maskmaking Lithography Company Shares
Regional
(Units)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Maskmaking Market	32	16	21	23	28	(3.3%)
United States						
ASM Lithography	0	0	0	1	1	
Ateq	0	0	1	1	4	
Cambridge Instruments	1	0	0	0	0	
Hitachi	0	0	0	0	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	14	9	4	4	1	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total United States	15	9	5	6	6	(20.5%)
Japan						
ASM Lithography	0	0	0	0	0	
Ateq	0	0	0	5	6	
Cambridge Instruments	0	0	0	0	0	
Hitachi	3	0	3	1	2	
JEOL	3	3	4	1	4	
Perkin-Elmer	8	3	2	1	2	
Toshiba	0	1	1	2	2	
Varian	0	0	0	0	0	
Total Japan	14	7	10	10	16	3.4%
Europe						
ASM Lithography	0	0	2	0	0	
Ateq	0	0	0	1	2	
Cambridge Instruments	1	0	0	0	0	
Hitachi	0	0	1	0	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	1	0	2	2	2	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Europe	2	0	5	3	4	18.9%

(Continued)

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Table 9 (Continued)

Maskmaking Lithography Company Shares
Regional
(Units)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Maskmaking Market	32	16	21	23	28	(3.3%)
Rest of World						
ASM Lithography	0	0	0	0	0	
Ateq	0	0	0	0	0	
Cambridge Instruments	0	0	0	2	1	
Hitachi	0	0	0	0	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	1	0	1	2	1	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Rest of World	1	0	1	4	2	18.9%
Worldwide						
ASM Lithography	0	0	2	1	1	
Ateq	0	0	1	7	12	
Cambridge Instruments	2	0	0	2	1	
Hitachi	3	0	4	1	2	
JEOL	3	3	4	1	4	
Perkin-Elmer	24	12	9	9	6	
Toshiba	0	1	1	2	2	
Varian	0	0	0	0	0	
Total Worldwide	32	16	21	23	28	(3.3%)

Source: Dataquest (June 1990), Ref: MMUNITS

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Table 10

Total Direct-Write and Maskmaking Lithography Company Shares Regional (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Direct-Write and Maskmaking Lithography Market	112.0	118.8	134.7	130.8	142.7	6.2%
United States						
ASM Lithography	1.9	4.0	4.0	4.8	2.4	
Ateq	0	0	1.6	1.6	6.8	
Cambridge Instruments	3.9	10.0	4.0	2.0	4.0	
Hitachi	0	0	0	0	0	
JEOL	7.0	10.0	6.0	6.0	6.0	
Perkin-Elmer	37.8	33.4	15.2	15.2	3.0	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total United States	50.6	57.4	30.8	29.6	22.2	(18.6%)
Japan						
ASM Lithography	0	0	0	0	0	
Ateq	0	0	0	8.0	10.2	
Cambridge Instruments	0	0	0	0	0	
Hitachi	11.0	11.2	19.1	13.4	16.0	
JEOL	12.9	29.7	38.9	28.1	37.4	
Perkin-Elmer	21.6	9.0	9.2	6.2	9.2	
Toshiba	0	3.0	3.5	7.7	7.2	
Varian	0	0	0	0	0	
Total Japan	45.5	52.9	70.7	63.4	80.0	15.2%
Europe						
ASM Lithography	0	2.0	8.0	4.8	7.2	
Ateq	0	0	0	1.6	3.4	
Cambridge Instruments	8.0	4.5	4.0	4.0	6.0	
Hitachi	0	0	3.0	0	0	
JEOL	2.5	2.0	4.0	2.0	4.0	
Perkin-Elmer	2.7	0	9.2	12.4	9.2	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Europe	13..	8.5	28.2	24.8	29.8	22.6%

(Continued)

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Table 10 (Continued)

Total Direct-Write and Maskmaking Lithography Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Direct-Write and Maskmaking Lithography Market	112.0	118.8	134.7	130.8	142.7	6.2%
Rest of World						
ASM Lithography	0	0	0	0	0	
Ateq	0	0	0	0	0	
Cambridge Instruments	0	0	2.0	7.0	4.5	
Hitachi	0	0	0	0	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	2.7	0	3.0	6.0	6.2	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Rest of World	2.7	0	5.0	13.0	10.7	41.1%
Worldwide						
ASM Lithography	1.9	6.0	12.0	9.6	9.6	
Ateq	0	0	1.6	11.2	20.4	
Cambridge Instruments	11.9	14.5	10.0	13.0	14.5	
Hitachi	11.0	11.2	22.1	13.4	16.0	
JEOL	22.4	41.7	48.9	36.1	47.4	
Perkin-Elmer	64.8	42.4	36.6	39.8	27.6	
Toshiba	0	3.0	3.5	7.7	7.2	
Varian	0	0	0	0	0	
Total Worldwide	112.0	118.8	134.7	130.8	142.7	6.2%

Source: Dataquest (June 1990), Ref: DWMMSHR

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Table 11

Total Direct-Write and Maskmaking Lithography Company Shares Regional (Units)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Direct-Write and Maskmaking Lithography Market	48	43	45	45	52	2.0%
United States						
ASM Lithography	1	2	2	2	1	
Ateq	0	0	1	1	4	
Cambridge Instruments	3	5	2	1	2	
Hitachi	0	0	0	0	0	
JEOL	4	5	3	3	3	
Perkin-Elmer	14	11	5	5	1	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total United States	22	23	13	12	11	(15.9%)
Japan						
ASM Lithography	0	0	0	0	0	
Ateq	0	0	0	5	6	
Cambridge Instruments	0	0	0	0	0	
Hitachi	5	3	5	3	4	
JEOL	5	8	9	6	9	
Perkin-Elmer	8	3	3	2	3	
Toshiba	0	1	1	2	2	
Varian	0	0	0	0	0	
Total Japan	18	15	18	18	24	7.5%
Europe						
ASM Lithography	0	1	4	2	3	
Ateq	0	0	0	1	2	
Cambridge Instruments	5	3	2	2	3	
Hitachi	0	0	1	0	0	
JEOL	1	1	2	1	2	
Perkin-Elmer	1	0	3	4	3	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Europe	7	5	12	10	13	16.7%

(Continued)

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Table 11 (Continued)

Total Direct-Write and Maskmaking Lithography Company Shares Regional (Units)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Direct-Write and Maskmaking Lithography Market	48	43	45	45	52	2.0%
Rest of World						
ASM Lithography	0	0	0	0	0	
Ateq	0	0	0	0	0	
Cambridge Instruments	0	0	1	3	2	
Hitachi	0	0	0	0	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	1	0	1	2	2	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Rest of World	1	0	2	5	4	41.4%
Worldwide						
ASM Lithography	1	3	6	4	4	
Ateq	0	0	1	7	12	
Cambridge Instruments	8	8	5	6	7	
Hitachi	5	3	6	3	4	
JEOL	10	14	14	10	14	
Perkin-Elmer	24	14	12	13	9	
Toshiba	0	1	1	2	2	
Varian	0	0	0	0	0	
Total Worldwide	48	43	45	45	52	2.0%

Source: Dataquest (June 1990), Ref: DWMMUNIT

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Table 12

X-Ray Aligner Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World X-Ray Market	1.8	0.8	0	6.4	4.8	27.8%
United States						
Hampshire Instruments	0	0	0	1.8	0	
Micronix	0	0	0	0	0	
Perkin-Elmer	0	0	0	0	2.0	
Karl Suss	0	0	0	1.6	0	
Total United States	0	0	0	3.4	2.0	NA
Japan						
Hampshire Instruments	0	0	0	0	0	
Micronix	0.8	0.8	0	0	0	
Perkin-Elmer	0	0	0	0	0	
Karl Suss	0	0	0	1.6	0	
Total Japan	0.8	0.8	0	1.6	0	NA
Europe						
Hampshire Instruments	0	0	0	0	0	
Micronix	0	0	0	0	0	
Perkin-Elmer	0	0	0	0	0	
Kark Suss	1.0	0	0	1.4	2.8	
Total Europe	1.0	0	0	1.4	2.8	29.4%
Rest of World						
Hampshire Instruments	0	0	0	0	0	
Micronix	0	0	0	0	0	
Perkin-Elmer	0	0	0	0	0	
Karl Suss	0	0	0	0	0	
Total Rest of World	0	0	0	0	0	NA
Worldwide						
Hampshire Instruments	0	0	0	1.8	0	
Micronix	0.8	0.8	0	0	0	
Perkin-Elmer	0	0	0	0	2.0	
Karl Suss	1.0	0	0	4.6	2.8	
Total Worldwide	1.8	0.8	0	6.4	4.8	27.8%

NA = Not available
Source: Dataquest (June 1990), Ref: XRAYSHR

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Table 13

Automatic Photoresist Processing Equipment (Track) Company Shares Regional (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Track Market	157.6	145.8	164.1	247.4	324.8	19.8%
United States						
Canon	0	0	0	0	0	
Convac	1.0	2.0	4.0	5.9	6.4	
Dainippon Screen	1.7	0.2	0.5	3.1	5.7	
Eaton	6.0	5.0	3.7	1.1	1.0	
GCA	6.0	6.5	2.8	2.2	0	
Machine Technology	15.3	11.3	10.1	7.9	10.0	
Semiconductor Systems	7.9	7.9	9.6	19.8	18.7	
Silicon Valley Group	21.3	15.5	20.8	25.4	27.0	
Solitec	4.9	6.3	5.3	5.6	7.0	
Tazmo	0	0.5	2.0	2.0	1.7	
Tokyo Electron Ltd.	0.2	0.9	2.1	5.0	0	
Varian/TEL	0	0	0	0	13.6	
Veeco	4.2	2.9	0	0	0	
Total United States	68.5	59.0	60.9	78.0	91.1	7.4%
Japan						
Canon	0	0.2	0.7	3.8	10.1	
Convac	0	0	0	0	0	
Dainippon Screen	29.4	27.4	27.8	31.7	51.8	
Eaton	0	0	0	0	0	
GCA	1.0	0.8	0.3	0.2	0	
Machine Technology	0.1	0.1	0.3	0.5	0.5	
Semiconductor Systems	0	0	0	0	0	
Silicon Valley Group	0	0	0	0	0.5	
Solitec	0	0	0	0	0	
Tazmo	1.1	1.6	2.1	2.9	6.8	
Tokyo Electron Ltd.	22.7	21.4	30.6	68.5	77.7	
Varian/TEL	0	0	0	0	0	
Veeco	0	0	0	0	0	
Total Japan	54.3	51.5	61.8	107.6	147.4	28.4%

(Continued)

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Table 13 (Continued)

Automatic Photoresist Processing Equipment (Track) Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Track Market	157.6	145.8	164.1	247.4	324.8	19.8%
Europe						
Canon	0	0.3	0.3	0	0	
Convac	2.8	4.4	6.9	7.9	5.8	
Dainippon Screen	0	1.2	1.9	2.7	5.1	
Eaton	5.0	6.0	5.2	6.6	6.3	
GCA	5.0	4.0	3.2	2.5	0	
Machine Technology	2.3	1.3	1.0	1.3	0.6	
Semiconductor Systems	0.9	0.9	1.2	2.2	3.3	
Silicon Valley Group	5.2	7.0	6.9	6.4	10.8	
Solitec	0.1	0.2	0.1	0.4	0.5	
Tazmo	0	0.3	0.3	0.3	0.4	
Tokyo Electron Ltd.	1.0	1.5	1.5	6.2	0	
Varian/TEL	0	0	0	0	5.8	
Veeco	0	0	0	0	0	
Total Europe	22.3	27.1	28.5	36.5	38.6	14.7%
Rest of World						
Canon	0	0	0	0	0	
Convac	0	0	0	0	0	
Dainippon Screen	3.8	1.0	1.0	2.7	5.1	
Eaton	1.0	1.0	1.6	3.3	3.2	
GCA	3.0	1.0	0.7	0.6	0	
Machine Technology	0.1	0.2	1.3	0.3	0.2	
Semiconductor Systems	0	0	0	0	0	
Silicon Valley Group	4.0	3.1	5.3	5.6	15.7	
Solitec	0	0	0.8	1.5	1.5	
Tazmo	0	0.1	0.2	0.5	0.4	
Tokyo Electron Ltd.	0.6	1.8	2.0	10.8	21.6	
Varian/TEL	0	0	0	0	0	
Veeco	0	0	0	0	0	
Total Rest of World	12.5	8.2	12.9	25.3	47.7	39.8%

(Continued)

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Table 13 (Continued)

Automatic Photoresist Processing Equipment (Track) Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Track Market	157.6	145.8	164.1	247.4	324.8	19.8%
Worldwide						
Canon	0	0.5	1.0	3.8	10.1	
Convac	3.8	6.4	10.9	13.8	12.2	
Dainippon Screen	34.9	29.8	31.2	40.2	67.7	
Eaton	12.0	12.0	10.5	11.0	10.5	
GCA	15.0	12.3	7.0	5.5	0	
Machine Technology	17.8	12.9	12.7	10.0	11.3	
Semiconductor Systems	8.8	8.8	10.8	22.0	22.0	
Silicon Valley Group	30.5	25.6	33.0	37.4	54.0	
Solitec	5.0	6.5	6.2	7.5	9.0	
Tazmo	1.1	2.5	4.6	5.7	9.3	
Tokyo Electron Ltd.	24.5	25.6	36.2	90.5	99.3	
Varian/TEL	0	0	0	0	19.4	
Veeco	4.2	2.9	0	0	0	
Total Worldwide	157.6	145.8	164.1	247.4	324.8	19.8%

Source: Dataquest (June 1990), Ref: TRACKSHR

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Table 14

Wet Process Company Shares
United States
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Wet Process Market	157.2	161.9	168.4	240.4	307.8	18.3%
Integrated Wet Systems						
Enya	0	0	0	0	0	
Dexon	0	0	0.7	3.1	4.1	
Dainippon Screen	0	0	0	2.2	4.3	
Integrated Air Systems	1.0	1.4	2.3	1.8	0	
Kaijo Denki	0	1.5	0.6	3.1	3.0	
Kuwano Electric	0	0	0	0.9	2.1	
Pokorny	0	0	0	0	0	
Poly-Flow Engineering	0.1	0.1	0.1	0	0	
Pure-Aire	1.0	1.0	1.5	1.7	2.5	
Sankyo Engineering	0	0.5	1.2	0	0	
Santa Clara Plastics	8.0	8.0	6.0	6.0	7.2	
Sci Manufacturing	0	0	2.8	5.2	6.9	
Semifab	0	1.0	2.6	5.0	6.2	
Shimada	0	0	0	0	0	
Sugai	0	0	0	0	0	
S&K Products Internat.	0.5	1.0	1.5	2.0	4.2	
Universal Plastics	0	0.3	1.6	3.1	4.7	
Verteq	2.0	3.0	0.8	1.8	0.9	
Total Integr. Systems	12.6	17.8	21.7	35.9	46.1	38.3%
Manual Wet Benches						
Enya	0	0	0	0	0	
Dexon	3.5	1.8	2.1	2.3	1.6	
Dainippon Screen	0	0	0	0.4	0.5	
Integrated Air Systems	4.0	2.6	0.7	0.2	0	
Kaijo Denki	0	0	0	0	0	
Pokorny	0	0	0	0	0	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0.7	0.6	0.6	0.5	0.2	
Sankyo Engineering	0	0	0	0	0	
Santa Clara Plastics	10.0	5.0	3.0	1.8	1.2	
Sci Manufacturing	0	0	2.0	2.8	1.3	
Semifab	4.2	4.7	4.3	1.2	0.9	
Shimada	0	0	0	0	0	
Sugai	0	0	0	0	0	
Universal Plastics	0.1	1.2	1.9	4.6	2.9	
Verteq	0	0.1	0	0.4	0	
Total Man. Benches	22.5	16.0	14.6	14.2	8.6	(21.4%)

(Continued)

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Table 14 (Continued)

Wet Process Company Shares
United States
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Wet Process Market	157.2	161.9	168.4	240.4	307.8	18.3%
Rinsers/Dryers						
Dainippon Screen	0	0	0	0.7	0.2	
Enya	0	0	0	0	0	
Estek	0	0	0.8	0.8	0	
FSI International	1.2	0.8	0.7	0.9	1.9	
Kaijo Denki	0	0	0	0.3	0.2	
Kuwano	0	0	0	0.2	0.2	
Poly-Flow Engineering	0.6	0.2	0.2	0.1	0.2	
Sankyo Engineering	0	0	0	0.2	0.1	
Semitool	10.7	9.0	10.9	9.7	11.3	
Shimada	0	0	0	0	0	
S&K Products Internat.	0.3	0.4	0.6	0.9	2.2	
Sugai	0	0	0	0	0	
Verteq	2.2	3.0	2.7	4.0	5.0	
Total Rinser/Dryers	15.0	13.4	15.9	17.8	21.3	9.2%
Acid Processors						
Athens	0	0	1.0	4.0	2.0	
CFM Technology	0	0	0	1.0	1.4	
FSI International	11.0	10.9	7.5	8.4	15.8	
Poly-Flow Engineering	0.1	0.1	0.1	0	0	
Semitool	2.7	2.7	2.2	2.9	3.3	
Total Acid Process.	13.8	13.7	10.8	16.3	22.3	12.7%
Megasonic Cleaners						
FSI International	0.9	1.2	1.2	1.2	2.0	
Kaijo Denki	0	0	0	0	0	
Verteq	0.8	1.2	1.7	3.2	3.9	
Total Megasonics	1.7	2.4	2.9	4.4	5.9	36.5%
Total US Wet Proc.	65.6	63.3	65.9	88.6	104.4	12.3%

Source: Dataquest (June 1990), Ref: WETSHR

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Table 15

Wet Process Company Shares
Japan
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Wet Process Market	157.2	161.9	168.4	240.4	305.6	18.1%
Integrated Wet Systems						
Enya	6.9	7.8	4.9	5.4	6.5	
Dexon	0	0	0	0	0	
Dainippon Screen	13.9	18.0	18.7	25.7	28.9	
Integrated Air Systems	0	0	0	0	0	
Kaijo Denki	8.4	10.8	6.2	7.7	19.4	
Kuwano Electric	2.5	3.3	5.6	8.5	4.0	
Pokorny	0	0	0	0	0	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0	0	0	0	0	
Sankyo Engineering	3.4	4.8	3.1	5.3	10.8	
Santa Clara Plastics	0	0	0	0	0	
Sci Manufacturing	0	0	0	0	0	
Semifab	0	0	0	0	0	
Shimada	0	0	3.4	4.9	8.6	
Sugai	2.8	2.2	2.8	4.2	8.9	
S&K Products Internat.	1.5	1.5	2.0	0	0	
Universal Plastics	0	0	0	0	0	
Verteq	0	0	0	0	0	
Others	5.5	6.0	4.2	6.2	8.2	
Total Integr. Systems	44.9	54.4	50.9	67.9	95.3	20.7%
Manual Wet Benches						
Enya	0.6	0.8	0.8	1.3	4.0	
Dexon	0	0	0	0	0	
Dainippon Screen	1.4	1.6	1.8	2.7	1.1	
Integrated Air Systems	0	0	0	0	0	
Kaijo Denki	1.0	0.7	0.8	1.9	3.2	
Pokorny	0	0	0	0	0	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0	0	0	0	0	
Sankyo Engineering	1.1	0.8	0.9	1.9	0.7	
Santa Clara Plastics	0	0	0	0	0	
Sci Manufacturing	0	0	0	0	0	
Semifab	0	0	0	0	0	
Shimada	0.4	0.3	0.3	0.4	0.2	
Sugai	0.2	0.3	0.3	0.9	1.1	
Universal Plastics	0	0	0	0	0	
Verteq	0	0	0	0	0	
Others	2.3	2.1	2.4	3.7	4.5	
Total Man. Benches	7.0	6.6	7.3	12.8	14.8	20.6%

(Continued)

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Table 15 (Continued)

Wet Process Company Shares
Japan
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Wet Process Market	157.2	161.9	168.4	240.4	305.6	18.1%
Rinsers/Dryers						
Dainippon Screen	0.6	1.0	1.2	2.1	1.9	
Enya	1.3	1.0	0.5	0.9	1.1	
Estek	0	0	0	0	0	
FSI International	1.4	1.2	0.7	0.5	0.7	
Kaijo Denki	0.6	0.5	0.6	1.3	1.4	
Kuwano	0.2	0.6	0.7	0.8	0	
Poly-Flow Engineering	0	0	0	0	0	
Sankyo Engineering	0.8	0.8	0.6	1.2	2.2	
Semitool	0	0	0	0.4	0.4	
Shimada	0.2	0.3	0.2	0.2	0.4	
S&K Products Internat.	3.5	3.3	3.8	4.5	1.2	
Sugai	0.9	1.2	1.4	1.9	2.4	
Verteq	0.1	0.1	0.1	0.4	1.6	
Others	0.4	0.5	0.3	0.5	0.5	
Total Rinser/Dryers	10.0	10.5	10.1	14.7	13.8	8.4%
Acid Processors						
Athens	0	0	0	0	0	
CFM Technology	0	0	0	0	0	
FSI International	0.7	0.9	1.2	1.2	1.8	
Poly-Flow Engineering	0	0	0	0	0	
Semitool	0	0	0	0.3	0.4	
Total Acid Process.	0.7	0.9	1.2	1.5	2.2	33.1%
Megasonic Cleaners						
FSI International	0.1	0.2	0.2	0.1	0.2	
Kaijo Denki	0	0	0.1	0.1	0.1	
Verteq	0.1	0	0.1	0.3	0.7	
Total Megasonics	0.2	0.2	0.4	0.5	1.0	49.5%
Total Japan Wet Proc.	62.8	72.6	69.9	97.4	127.1	19.3%

Source: Dataquest (June 1990), Ref: WETSHR

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Table 16

Wet Process Company Shares
Europe
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Wet Process Market	157.2	161.9	168.4	240.4	305.6	18.1%
Integrated Wet Systems						
Enya	0	0	0	0	0	
Dexon	0	0	0	0	0	
Dainippon Screen	0	0	0	0	0	
Integrated Air Systems	0	0	0	0	0	
Kaijo Denki	0	0	1.8	0	0	
Kuwano Electric	0	0	0	2.3	1.0	
Pokorny	0.3	1.2	2.3	2.5	4.7	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0	0	0	0	0	
Sankyo Engineering	0	0	1.2	3.1	2.8	
Santa Clara Plastics	3.0	3.0	3.0	3.0	4.2	
Sci Manufacturing	0	0	0	0	0	
Semifab	0	0	0	0	0	
Shimada	0	0	0	0	0	
Sugai	0	0	0	0	0	
S&K Products Internat.	0	0	0	1.5	3.5	
Universal Plastics	0	0	0	0	0	
Verteq	0	0	0	0	0	
Total Integr. Systems	3.3	4.2	8.3	12.4	16.2	48.9%
Manual Wet Benches						
Enya	0	0	0	0	0	
Dexon	0	1.3	0.3	0.1	0.4	
Dainippon Screen	0	0	0	0.4	0.5	
Integrated Air Systems	0	0	0	0	0	
Kaijo Denki	0	0	0	0	0	
Pokorny	1.7	1.9	2.0	2.2	3.5	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0	0	0	0	0	
Sankyo Engineering	0	0	0	3.2	0.7	
Santa Clara Plastics	3.0	2.0	1.0	0.8	0.6	
Sci Manufacturing	0	0	0	0	0	
Semifab	0.5	0.1	0.1	0	0	
Shimada	0	0	0	0	0	
Sugai	0	0	0	0	0	
Universal Plastics	0	0.1	0.1	0	0	
Verteq	0	0	0	0	0	
Total Man. Benches	5.2	5.4	3.5	6.7	5.7	2.3%

(Continued)

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Table 16 (Continued)

Wet Process Company Shares
Europe
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Wet Process Market	157.2	161.9	168.4	240.4	305.6	18.1%
Rinsers/Dryers						
Dainippon Screen	0	0	0	0.5	0.2	
Enya	0	0	0	0	0	
Estek	0	0	0.4	0.3	0	
FSI International	1.1	0.4	0.5	0.7	0.4	
Kaijo Denki	0	0	0	0.2	0	
Kuwano	0	0	0	0	0	
Poly-Flow Engineering	0	0	0	0	0.1	
Sankyo Engineering	0	0	0	0.2	0.2	
Semitool	1.6	2.0	2.1	1.6	1.8	
Shimada	0	0	0	0	0	
S&K Products Internat.	0.3	0.7	0.6	0.5	0.5	
Sugai	0	0	0	0	0	
Verteq	0.2	0.2	0.3	0.5	0.6	
Total Rinser/Dryers	3.2	3.3	3.9	4.5	3.8	4.4%
Acid Processors						
Athens	0	0	0	0	0	
CFM Technology	0	0	0	0	0	
FSI International	10.5	5.8	5.1	9.1	11.4	
Poly-Flow Engineering	0	0	0	0.1	4.1	
Semitool	0.5	0.5	0.8	0.4	2.8	
Total Acid Process.	11.0	6.3	5.9	9.6	16.3	10.3%
Megasonic Cleaners						
FSI International	0.1	0.3	0.5	0.5	0.4	
Kaijo Denki	0	0	0	0	0	
Verteq	0.1	0.1	0.3	0.5	0.6	
Total Megasonics	0.2	0.4	0.8	1.0	1.0	49.5%
Total Eur. Wet Proc.	22.9	19.6	22.4	34.2	43.0	17.1%

Source: Dataquest (June 1990), Ref: WETSHR

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Table 17

Wet Process Company Shares
Rest of World
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Wet Process Market	157.2	161.9	168.4	240.4	307.8	18.3%
Integrated Wet Systems						
Enya	0	0	0	0	0	
Dexon	0	0	0	0	0.3	
Dainippon Screen	0	0	0	2.2	8.6	
Integrated Air Systems	0	0	0	0	0	
Kaijo Denki	0	0	0	0	0	
Kuwano Electric	0	0	0	0.9	2.3	
Pokorny	0	0	0	0	0	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0	0.1	0.2	0.2	0.1	
Sankyo Engineering	0	0.5	1.1	1.8	2.4	
Santa Clara Plastics	1.0	1.0	2.0	2.0	2.9	
Sci Manufacturing	0	0	0	0	0	
Semifab	0	0	0.1	0	0	
Shimada	0	0	0	0	0	
Sugai	0	0	0	0	0	
S&K Products Internat.	0.5	0	0	0	0	
Universal Plastics	0	0	0	0	0	
Verteq	0	0.5	0	0.2	0.2	
Total Integr. Systems	1.5	2.1	3.4	7.3	16.8	82.9%
Manual Wet Benches						
Enya	0	0	0	0	0	
Dexon	0	0	0	0	0	
Dainippon Screen	0	0	0	0.4	0.2	
Integrated Air Systems	0	0	0	0	0	
Kaijo Denki	0	0	0	0	0	
Pokorny	0	0	0	0	0	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0.1	0.1	0.1	0.4	0.2	
Sankyo Engineering	0	0	0	6.5	7.2	
Santa Clara Plastics	1.0	1.0	1.0	1.0	0.5	
Sci Manufacturing	0	0	0	0	0	
Semifab	0.1	0.6	0.6	0.8	0.5	
Shimada	0	0	0	0	0	
Sugai	0	0	0	0	0	
Universal Plastics	0	0	0.1	0.8	1.5	
Verteq	0.1	0	0.2	0.1	0	
Total Man. Benches	1.3	1.7	2.0	10.0	10.1	67.0%

(Continued)

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Table 17 (Continued)

Wet Process Company Shares
Rest of World
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Wet Process Market	157.2	161.9	168.4	240.4	307.8	18.3%
Rinsers/Dryers						
Dainippon Screen	0	0	0	0.5	0.8	
Enya	0	0	0	0	0	
Estek	0	0	0	0	0	
FSI International	0.2	0.1	0.2	0.1	0.3	
Kaijo Denki	0	0	0	0	0	
Kuwano	0	0	0	0	0	
Poly-Flow Engineering	0	0.1	0.1	0	0	
Sankyo Engineering	0	0	0	0.4	0.3	
Semitool	1.4	1.6	2.5	0.1	0.2	
Shimada	0	0	0	0	0	
S&K Products Internat.	0	0	0	0	0	
Sugai	0	0	0	0	0	
Verteq	0.2	0.1	0.2	0.4	0.3	
Total Rinser/Dryers	1.8	1.9	3.0	1.5	1.9	1.4%
Acid Processors						
Athens	0	0	0	0	0	
CFM Technology	0	0	0	0	0	
FSI International	1.2	0.5	1.2	0.7	1.7	
Poly-Flow Engineering	0	0	0	0	0	
Semitool	0	0.1	0.3	0	0	
Total Acid Process.	1.2	0.6	1.5	0.7	1.7	9.1%
Megasonic Cleaners						
FSI International	0	0.1	0.2	0.7	0.7	
Kaijo Denki	0	0	0	0	0	
Verteq	0.1	0	0.1	0	0.1	
Total Megasonics	0.1	0.1	0.3	0.7	0.8	68.2%
Total ROW Wet Proc.	5.9	6.4	10.2	20.2	31.3	51.8%

Source: Dataquest (June 1990), Ref: WETSHR

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Table 18

Wet Process Company Shares Worldwide (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Wet Process Market	157.2	161.9	168.4	240.4	305.6	18.1%
Integrated Wet Systems						
Enya	6.9	7.8	4.9	5.4	6.5	
Dexon	0	0	0.7	3.1	4.4	
Dainippon Screen	13.9	18.0	18.7	30.1	41.8	
Integrated Air systems	1.0	1.4	2.3	1.8	0	
Kaijo Denki	8.4	12.3	8.6	10.8	22.4	
Kuwano Electric	2.5	3.3	5.6	12.6	9.4	
Pokorny	0.3	1.2	2.3	2.5	4.7	
Poly-Flow Engineering	0.1	0.1	0.1	0	0	
Pure-Aire	1.0	1.1	1.7	1.9	2.6	
Sankyo Engineering	3.4	5.8	6.6	10.2	16.0	
Santa Clara Plastics	12.0	12.0	11.0	11.0	14.3	
Sci Manufacturing	0	0	2.8	5.2	6.9	
Semifab	0	1.0	2.7	5.0	6.2	
Shimada	0	0	3.4	4.9	8.6	
Sugai	2.8	2.2	2.8	4.2	8.9	
S&K Products Internat.	2.5	2.5	3.5	3.5	7.7	
Universal Plastics	0	0.3	1.6	3.1	4.7	
Verteq	2.0	3.5	0.8	2.0	1.1	
Others	5.5	6.0	4.2	6.2	8.2	
Total Integr. Systems	62.3	78.5	84.3	123.5	174.4	29.3%
Manual Wet Benches						
Enya	0.6	0.8	0.8	1.3	4.0	
Dexon	3.5	3.1	2.4	2.4	2.0	
Dainippon Screen	1.4	1.6	1.8	3.9	2.3	
Integrated Air Systems	4.0	2.6	0.7	0.2	0	
Kaijo Denki	1.0	0.7	0.8	1.9	3.2	
Pokorny	1.7	1.9	2.0	2.2	3.5	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0.8	0.7	0.7	0.9	0.4	
Sankyo Engineering	1.1	0.8	0.9	11.6	8.6	
Santa Clara Plastics	14.0	8.0	5.0	3.6	2.3	
Sci Manufacturing	0	0	2.0	2.8	1.3	
Semifab	4.8	5.4	5.0	2.0	1.4	
Shimada	0.4	0.3	0.2	0.4	0.2	
Sugai	0.2	0.3	0.3	0.9	1.1	
Universal Plastics	0.1	1.3	2.1	5.4	4.4	
Verteq	0.1	0.1	0.2	0.5	0	
Others	2.3	2.1	2.4	3.7	4.5	
Total Man. Benches	36.0	29.7	27.4	43.7	39.2	2.2%

(Continued)

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Table 18 (Continued)

Wet Process Company Shares Worldwide (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Wet Process Market	157.2	161.9	168.4	240.4	305.6	18.1%
Rinsers/Dryers						
Dainippon Screen	0.6	1.0	1.2	3.8	3.1	
Enya	1.3	1.0	0.5	0.9	1.1	
Estek	0	0	1.2	1.1	0	
FSI International	3.9	2.5	2.1	2.2	3.3	
Kaijo Denki	0.6	0.5	0.6	1.8	1.6	
Kuwano	0.2	0.6	0.7	1.0	0.2	
Poly-Flow Engineering	0.6	0.3	0.3	0.1	0.3	
Sankyo Engineering	0.8	0.8	0.6	2.0	2.8	
Semitool	13.7	12.6	15.5	11.8	13.7	
Shimada	0.2	0.3	0.2	0.2	0.4	
S&K Products Internat.	4.1	4.4	5.0	5.9	3.9	
Sugai	0.9	1.2	1.4	1.9	2.4	
Verteq	2.7	3.4	3.3	5.3	7.5	
Others	0.4	0.5	0.3	0.5	0.5	
Total Rinser/Dryers	30.0	29.1	32.9	38.5	40.8	8.0%
Acid Processors						
Athens	0	0	1.0	4.0	2.0	
CFM Technology	0	0	0	1.0	1.4	
FSI International	23.4	18.1	15.0	19.4	30.7	
Poly-Flow Engineering	0.1	0.1	0.1	0.1	4.1	
Semitool	3.2	3.3	3.3	3.6	6.5	
Total Acid Process.	26.7	21.5	19.4	28.1	42.5	12.3%
Megasonic Cleaners						
FSI International	1.1	1.8	2.1	2.5	3.3	
Kaijo Denki	0	0	0.1	0.1	0.1	
Verteq	1.1	1.3	2.2	4.0	5.3	
Total Megasonics	2.2	3.1	4.4	6.6	8.7	41.0%
Total World Wet Proc.	157.2	161.9	168.4	240.4	305.6	18.1%

Source: Dataquest (June 1990), Ref: WETSHR

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Table 19

Dry Strip Company Shares
United States and Japan
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Dry Strip Market	38.5	34.4	55.3	94.4	116.2	31.8%
United States						
Alcan Tech	0	0	0	0	0	
Branson/IPC	7.5	5.0	3.8	8.0	6.4	
Chemitronics	0	0	0	0	0	
Chlorine Engineering	0	0	0	0	0	
Drytek	2.0	1.0	0.8	0.8	1.0	
E.T. Electrotech	0	0	0	0	0	
Gasonics	0	0.7	1.6	2.1	5.3	
Hitachi	0	0	0	0	0	
Hohkoh Sangyo	0	0	0	0	0	
LFE	2.0	1.0	1.0	0.8	1.0	
Machine Technology	0.3	2.0	2.0	3.0	1.0	
Matrix	0	2.1	4.5	4.7	5.5	
Plasma Systems	0	0	0	0	0	
Plasma-Therm	0	0	0	0	1.0	
Ramco	0	0	0	0	0	
Samco	0	0	0	0	0.1	
Tegal	2.0	2.0	1.2	1.0	1.0	
Tokyo Ohka	0	0	0	0	2.0	
Ulvac	0	0	0	0	0	
Total United States	13.8	13.8	14.9	20.4	24.3	15.2%
Japan						
Alcan Tech	0	0.9	5.0	9.2	11.6	
Branson/IPC	1.8	1.2	1.4	1.0	1.5	
Chemitronics	0	0	0	1.4	0	
Chlorine Engineering	0	0	0	0	1.4	
Drytek	0	0	0	0	0	
E.T. Electrotech	0	0	0	0	0	
Gasonics	0	0	0	0	0.1	
Hitachi	0	0	0.7	4.6	5.0	
Hohkoh Sangyo	1.1	0.5	0.6	0	0.6	
LFE	0	0	0	0	0	
Machine Technology	0	0	0.7	1.5	0	
Matrix	0	0	0.2	0.5	0.5	
Plasma Systems	3.2	3.3	4.3	10.4	15.0	
Plasma-Therm	0	0	0	0	0	
Ramco	1.7	4.5	8.7	9.6	11.0	
Samco	0	0	0	0	0.9	
Tegal	0	0	0	0	0	
Tokyo Ohka	8.9	5.2	8.7	19.9	22.0	
Ulvac	0	0	3.6	4.9	5.5	
Total Japan	16.7	15.6	33.9	63.0	75.1	45.6%

Source: Dataquest (June 1990), Ref: DSTRPSHR

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Table 20

Dry Strip Company Shares
Europe and ROW
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Dry Strip Market	38.5	34.4	55.3	94.4	116.2	31.8%
Europe						
Alcan Tech	0	0	0	0	0	
Branson/IPC	3.0	3.0	1.4	2.0	3.2	
Chemitronics	0	0	0	0	0	
Chlorine Engineering	0	0	0	0	0	
Drytek	0	0	0	0	0	
E.T. Electrotech	1.0	0	0	0	0	
Gasonics	0	0	0.4	0.6	0.1	
Hitachi	0	0	0	0	0	
Hohkoh Sangyo	0	0	0	0	0	
LFE	0	0	0	0.5	0	
Machine Technology	0	0	0	0	0	
Matrix	0	0	0.1	0.6	0.5	
Plasma Systems	0	0	0	0	0	
Plasma-Therm	0	0	0	0	0	
Ramco	0	0	0	0	0	
Samco	0	0	0	0	0	
Tegal	1.0	0	0	0	0.5	
Tokyo Ohka	0	0	0	0	1.0	
Ulvac	0	0	0	0	0	
Total Europe	5.0	3.0	1.9	3.7	5.3	1.5%
Rest of World						
Alcan Tech	0	0	0	0	0	
Branson/IPC	2.0	1.0	1.2	4.0	4.9	
Chemitronics	0	0	0	0	0	
Chlorine Engineering	0	0	0	0	0	
Drytek	1.0	1.0	0.2	0.4	0.4	
E.T. Electrotech	0	0	0	0	0	
Gasonics	0	0	0	0.3	0.7	
Hitachi	0	0	0	0	0	
Hohkoh Sangyo	0	0	0	0	0	
LFE	0	0	0	0.2	0.5	
Machine Technology	0	0	0	0	0.5	
Matrix	0	0	0.4	1.4	0.5	
Plasma Systems	0	0	1.1	0	2.0	
Plasma-Therm	0	0	0	0	0	
Ramco	0	0	0	0	0	
Samco	0	0	0	0	0	
Tegal	0	0	1.2	1.0	1.0	
Tokyo Ohka	0	0	0.5	0	1.0	
Ulvac	0	0	0	0	0	
Total Rest of World	3.0	2.0	4.6	7.3	11.5	39.9%

Source: Dataquest (June 1990), Ref: DSTRPSHR

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Table 21

Dry Strip Company Shares Worldwide (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Dry Strip Market	38.5	34.4	55.3	94.4.	116.2	31.8%
Worldwide						
Alcan Tech	0	0.9	5.0	9.2	11.6	
Branson/IPC	14.3	10.2	7.8	15.0	16.0	
Chemitronics	0	0	0	1.4	0	
Chlorine Engineering	0	0	0	0	1.4	
Drytek	3.0	2.0	1.0	1.2	1.4	
E.T. Electrotech	1.0	0	0	0	0	
Gasonics	0	0.7	2.0	3.0	6.2	
Hitachi	0	0	0.7	4.6	5.0	
Hohkoh Sangyo	1.1	0.5	0.6	0	0.6	
LFE	2.0	1.0	1.0	1.5	1.5	
Machine Technology	0.3	2.0	2.7	4.5	1.5	
Matrix	0	2.1	5.2	7.2	7.0	
Plasma Systems	3.2	3.3	5.4	10.4	17.0	
Plasma-Therm	0	0	0	0	1.0	
Ramco	1.7	4.5	8.7	9.6	11.0	
Samco	0	0	0	0	1.0	
Tegal	3.0	2.0	2.4	2.0	2.5	
Tokyo Ohka	8.9	5.2	9.2	19.9	26.0	
Ulvac	0	0	3.6	4.9	5.5	
Total Worldwide	38.5	34.4	55.3	94.4	116.2	31.8%

Source: Dataquest (June 1990), Ref: DSTRPSHR

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Table 22

Dry Etch Company Shares
United States
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Dry Etch Market	299.6	237.1	307.4	545.8	635.6	20.7%
United States						
Anelva	4.0	0	0	0	5.0	
Applied Materials	44.0	35.0	48.1	72.9	77.0	
Branson/IPC	2.0	0	0	0	1.2	
Drytek	20.0	10.0	11.0	23.0	16.0	
Elionix	0	0	0	0	0	
Ergo Plasma Systems	0	0	0	0	0	
E.T. Electrotech	3.0	1.0	1.0	4.2	4.0	
GCA	0.4	1.2	3.0	4.0	0	
Hitachi	0	0	0	0	0	
Kokusai	1.0	0	0	0	0	
Lam Research	25.0	16.0	20.0	29.0	44.0	
Materials Research	2.6	2.4	2.5	6.0	4.0	
Perkin-Elmer	11.0	6.0	0	0	0	
Plasma Systems	0	0	0	0	0	
Plasma-Therm	8.0	8.5	11.4	10.2	12.0	
Samco	0	0	0	0	0	
Sumitomo Metals	0	0	0	0	0	
Tegal	16.0	16.0	20.0	25.1	19.0	
Tokyo Electron	0	0	0	0	0	
Tokuda	3.0	0	1.1	2.5	2.5	
Tokyo Ohka	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian (Zylin)	8.0	4.0	0	0	0	
Varian/TEL	0	0	0	0	6.0	
Total United States	148.0	100.1	118.1	176.9	190.7	6.5%

Source: Dataquest (June 1990), Ref: DETCHSHR

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Table 23

Dry Etch Company Shares
Japan
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Dry Etch Market	290.6	237.1	307.4	545.8	635.6	20.7%
Japan						
Anelva	34.4	16.2	22.3	41.6	35.6	
Applied Materials	17.6	21.0	24.8	76.1	79.0	
Branson/IPC	1.9	1.2	0.6	0	0.7	
Drytek	0	0	0	0	1.7	
Elionix	0	0.2	0.3	0.3	0.3	
Ergo Plasma Systems	0.8	0	0	0	0	
E.T. Electrotech	0.9	0	0	1.5	1.5	
GCA	0	0	0	0	0	
Hitachi	3.6	10.8	18.8	34.6	47.3	
Kokusai	8.4	3.3	1.4	1.5	1.0	
Lam Research	0	0	0	0	5.6	
Materials Research	1.0	0.8	1.0	5.0	2.2	
Perkin-Elmer	2.5	1.2	0	0	0	
Plasma Systems	1.5	1.7	1.9	3.2	3.3	
Plasma-Therm	0	1.5	1.2	1.2	1.6	
Samco	0	0	0	0	2.2	
Sumitomo Metals	0	2.4	5.6	6.2	12.0	
Tegal	0	0.6	0	1.9	3.0	
Tokyo Electron	10.5	6.0	17.4	44.6	70.0	
Tokuda	6.6	4.3	5.0	3.2	8.0	
Tokyo Ohka	7.6	7.2	7.1	10.0	21.7	
Ulvac	4.7	3.9	5.6	8.1	8.7	
Varian (Zylin)	0	0	0	0	0	
Varian/TEL	0	0	0	0	0	
Total Japan	102.0	82.3	113.0	239.0	305.4	31.5%

Source: Dataquest (June 1990), Ref: DETCHSHR

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Table 24

Dry Etch Company Shares
Europe
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Dry Etch Market	299.6	237.1	307.4	545.8	635.6	20.7%
Europe						
Anelva	0	0	0	0	0	
Applied Materials	5.0	14.0	22.0	28.3	31.0	
Branson/IPC	1.0	2.0	0	0	0.8	
Drytek	1.0	2.0	2.0	0	1.7	
Elionix	0	0	0	0	0	
Ergo Plasma Systems	0	0	0	0	0	
E.T. Electrotech	5.0	4.0	6.2	7.7	8.0	
GCA	0.4	0.8	1.0	1.0	0	
Hitachi	0	0	0	0	0	
Kokusai	1.0	0	0	0	0	
Lam Research	3.0	5.0	7.0	13.0	10.0	
Materials Research	1.2	0.9	0.9	1.5	1.2	
Perkin-Elmer	3.0	2.0	0	0	0	
Plasma Systems	0	0	0	0	0	
Plasma-Therm	4.0	1.0	0.8	1.2	1.2	
Samco	0	0	0	0	0	
Sumitomo Metals	0	0	0	0	0	
Tegal	8.0	8.0	15.6	24.0	16.0	
Tokyo Electron	0	0	0	0	0	
Tokuda	0	0	2.8	2.1	0	
Tokyo Ohka	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian (Zylin)	0	0	0	0	0	
Varian/TEL	0	0	0	0	0	
Total Europe	32.6	39.7	58.3	78.8	69.9	21.0%

Source: Dataquest (June 1990), Ref: DETCHSHR

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Table 25

Dry Etch Company Shares
Rest of World
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Dry Etch Market	299.6	237.1	307.4	545.8	635.6	20.7%
Rest of World						
Anelva	1.0	0	0	0	3.6	
Applied Materials	3.0	4.0	7.1	19.4	21.0	
Branson/IPC	0	1.0	1.0	0	0.5	
Drytek	2.0	4.0	4.0	2.0	2.6	
Elionix	0	0	0	0	0	
Ergo Plasma Systems	0	0	0	0	0	
E.T. Electrotech	0	0	0	0.7	1.5	
CGA	0	0	0	0	0	
Hitachi	0	0	0	0	0	
Kokusai	0	0	0	0	0	
Lam Research	6.0	5.0	5.0	23.0	26.0	
Materials Research	0	0	0	0.5	0	
Perkin-Elmer	3.0	0	0	0	0	
Plasma Systems	0	0	0	0	0	
Plasma-Therm	1.0	0	0.3	0.3	0.4	
Samco	0	0	0	0	0	
Sumitomo Metals	0	0	0	0	0	
Tegal	1.0	1.0	0	4.0	4.0	
Tokyo Electron	0	0	0	0	10.0	
Tokuda	0	0	0.5	1.0	0	
Tokyo Ohka	0	0	0	0	0	
Ulvac	0	0	0.1	0.2	0	
Varian (Zylin)	0	0	0	0	0	
Varian/TEL	0	0	0	0	0	
Total Rest of World	17.0	15.0	18.0	51.1	69.6	42.2%

Source: Dataquest (June 1990), Ref: DETCHSHR

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Table 26

Dry Etch Company Shares
Worldwide
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Dry Etch Market	299.6	237.1	307.4	545.8	635.6	20.7%
Worldwide						
Anelva	39.4	16.2	22.3	41.6	44.2	
Applied Materials	69.6	74.0	102.0	196.7	208.0	
Branson/IPC	4.9	4.2	1.6	0	3.2	
Drytek	23.0	16.0	17.0	25.0	22.0	
Elionix	0	0.2	0.3	0.3	0.3	
Ergo Plasma Systems	0.8	0	0	0	0	
E.T. Electrotech	8.9	5.0	7.2	14.1	15.0	
GCA	0.8	2.0	4.0	5.0	0	
Hitachi	3.6	10.8	18.8	34.6	47.3	
Kokusai	10.4	3.3	1.4	1.5	1.0	
Lam Research	34.0	26.0	32.0	65.0	85.6	
Materials Research	4.8	4.1	4.4	13.0	7.4	
Perkin-Elmer	19.5	9.2	0	0	0	
Plasma Systems	1.5	1.7	1.9	3.2	3.3	
Plasma-Therm	13.0	11.0	13.7	12.9	15.2	
Samco	0	0	0	0	2.2	
Sumitomo Metals	0	2.4	5.6	6.2	12.0	
Tegal	25.0	25.6	35.6	55.0	42.0	
Tokyo Electron	10.5	6.0	17.4	44.6	80.0	
Tokuda	9.6	4.3	9.4	8.8	10.5	
Tokyo Ohka	7.6	7.2	7.1	10.0	21.7	
Ulvac	4.7	3.9	5.7	8.3	8.7	
Varian (Zylin)	8.0	4.0	0	0	0	
Varian/TEL	0	0	0	0	6	
Total Worldwide	299.6	237.1	307.4	545.8	635.6	20.7%

Source: Dataquest (June 1990), Ref: DETCHSHR

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Table 27

Chemical Vapor Deposition Company Shares
United States
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CVD Market	246.5	219.9	259.8	456.2	580.2	24.0%
Tube CVD						
Horizontal Tube LPCVD						
ASM International	2.3	1.2	1.7	2.6	2.0	
BTU International	5.5	2.7	3.4	7.4	9.0	
Enya	0	0	0	0	0	
GSTC (Tempress)	5.5	2.5	0	3.0	3.0	
Kokusai Electric	0	0	0	0.8	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0.4	0.5	0	0	0	
Process Technology	4.0	4.5	3.8	4.0	3.2	
SVG (Thermco)	3.1	2.9	3.0	3.5	7.0	
Solitec	10.8	4.1	2.0	4.8	4.0	
Tokyo Electron Ltd.	0	0	0	0	0	
Tylan	0.6	0.4	1.0	1.5	0.5	
Ulvac/BTU	0	0	0	0	0	
Varian/TEL	0	0	0	0	0	
Wellman	0	0	0	0	0	
Total Horizontal LPCVD	32.2	18.8	14.9	27.6	28.7	(2.8%)
Vertical Tube LPCVD						
ASM International	0	0	0	0	0.6	
BTU International	0	0	0	0	0	
Denko	0	0	0	0	0	
Disco	0	0	0	0	0	
Helmut Seier	0.3	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Kokusai Electric	0	0	0	2.5	2.2	
Semitherm	0	0	0	0.5	1.0	
Silicon Valley Group	0	0.2	1.6	1.6	3.0	
Tokyo Electron Ltd.	0	0	0	0	0	
Ulvac/BTU	0	0	0	0	0	
Varian/TEL	0	0	0	0	3.0	
Total Vertical LPCVD	0.3	0.2	1.6	4.6	9.8	139.1%

(Continued)

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Table 27 (Continued)

Chemical Vapor Deposition Company Shares
United States
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CVD Market	246.5	219.9	259.8	456.2	580.2	24.0%
Horizontal Tube PECVD						
ASM International	15.5	14.9	23.1	20.6	16.0	
Pacific Western	4.1	2.9	3.7	2.7	2.0	
Total Horizontal PECVD	19.6	17.8	26.8	23.3	18.0	(2.1%)
Total US Tube CVD	52.1	36.8	43.3	55.5	56.5	2.0%
Nontube CVD Reactors						
APCVD Reactors						
Amaya	0	0	0	0	0	
Applied Materials	1.8	1.2	3.0	3.0	2.0	
GSTC (Tempress)	1.4	1.3	0	0.5	0.5	
Hitachi	0	0	0	0	0	
Kokusai Electric	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0.6	0.4	0	0	0	
Toshiba Machine	0	0	0	0	0	
Watkins-Johnson	3.4	5.6	7.3	10.5	11.0	
Total APCVD Reactors	7.2	8.5	10.3	14.0	13.5	17.0%
LPCVD Reactors						
Anelva	0	0	0	0	0	
Focus Semiconductor	0	0	1.0	1.6	0	
Genus	6.7	4.2	7.1	11.7	22.0	
Silicon Valley Group	6.7	3.3	1.4	1.5	0.6	
Spectrum CVD	0	0.5	2.3	1.1	2.0	
Ulvac	0	0	0	0	0	
Varian	0	1.1	2.5	2.0	0.7	
Total LPCVD Reactors	13.4	9.1	14.3	17.9	25.3	17.2%

(Continued)

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Table 27 (Continued)

Chemical Vapor Deposition Company Shares
United States
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CVD Market	246.5	219.9	259.8	456.2	580.2	24.0%
PECVD Reactors						
Anelva	0	0	0	0	0	
Applied Materials	2.3	1.4	15.5	37.0	56.0	
Enya	0	0	0	0	0	
E.T. Electrotech	3.7	4.0	1.0	4.2	2.5	
Japan Production	0	0	0	0	0	
Novellus	0	0	3.1	16.9	33.0	
Plasma-Therm	3.8	3.0	3.8	4.0	2.0	
Samco	0	0	0	0	0	
Sumitomo Metals (ECR)	0	0	0	0	0	
Ulvac	0	0	0	0.6	0	
Total PECVD Reactors	9.8	8.4	23.4	62.7	93.5	75.8%
Total US Nontube CVD	30.4	26.0	48.0	94.6	132.3	44.4%
Total US CVD	82.5	62.8	91.3	150.1	188.8	23.0%

Source: Dataquest (June 1990), Ref: CVDSHR

Table 28

Chemical Vapor Deposition Company Shares
Japan
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CVD Market	246.5	219.9	259.8	456.2	580.2	24.0%
Tube CVD						
Horizontal Tube LPCVD						
ASM International	4.5	4.8	2.0	3.9	2.0	
BTU International	0.5	0	0	0	0	
Enya	1.3	1.0	0.6	1.8	1.7	
GSTC (Tempress)	0.1	0	0	0	0	
Kokusai Electric	14.6	16.2	7.6	6.4	2.2	
Koyo Lindberg	1.9	1.8	1.0	1.8	3.0	
Pacific Western	0	0	0	0	0	
Process Technology	0	0	0	0	0	
SVG (Thermco)	0	0	0	0	0	
Solitec	0	0	0	0	0	
Tokyo Electron Ltd.	15.0	6.6	8.3	8.5	8.7	
Tylan	0	0	0	0	0	
Ulvac/BTU	0	0	0.5	3.5	4.0	
Varian/TEL	0	0	0	0	0	
Wellman	0	0	0	0	0	
Total Horizontal LPCVD	37.9	30.4	20.0	25.9	21.6	(13.1%)
Vertical Tube LPCVD						
ASM International	0	0.5	0	0	0.6	
BTU International	0	0	0	0	0	
Denko	1.3	2.7	2.1	2.3	3.5	
Disco	0	0	0	0	0	
Helmut Seier	0	0	0.3	0.3	0	
Koyo Lindberg	0	0.4	1.0	2.7	1.1	
Kokusai Electric	0	1.4	2.8	12.3	20.0	
Semitherm	0	0	0	0	0	
Silicon Valley Group	0	0	0	0.8	0	
Tokyo Electron Ltd.	1.0	1.0	0	3.8	6.0	
Ulvac/BTU	0	0	0	0	0	
Varian/TEL	0	0	0	0	0	
Total Vertical LPCVD	2.3	6.0	6.2	22.2	31.2	91.9%

(Continued)

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Table 28 (Continued)

Chemical Vapor Deposition Company Shares
Japan
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CVD Market	246.5	219.9	259.8	456.2	580.2	24.0%
Horizontal Tube PECVD						
ASM International	15.7	16.4	9.8	15.5	17.0	
Pacific Western	3.8	2.7	2.8	2.1	1.0	
Total Horizontal PECVD	19.5	19.1	12.6	17.6	18.0	(2.0%)
Total Japan Tube CVD	59.7	55.5	38.8	65.7	70.8	4.4%
Nontube CVD Reactors						
APCVD Reactors						
Amaya	10.9	6.0	5.5	17.5	19.0	
Applied Materials	6.3	5.4	8.5	8.7	7.0	
GSTC (Tempress)	0.2	0.3	0	0.5	0	
Hitachi	0.3	0.4	0	0.2	0.5	
Kokusai Electric	0.7	0.7	0	0	0	
Koyo Lindberg	0.6	0.4	0.2	1.3	0.6	
Pacific Western	0.5	0.4	0.2	0	0	
Toshiba Machine	0	4.3	5.0	6.0	4.2	
Watkins-Johnson	1.0	0.5	2.0	15.0	22.0	
Total APCVD Reactors	20.5	18.4	21.4	49.2	53.3	27.0%
LPCVD Reactors						
Anelva	0	0	0.7	2.3	1.5	
Focus Semiconductor	0	0	0	0.9	0	
Genus	8.0	1.1	3.3	12.7	23.0	
Silicon Valley Group	4.9	2.0	0.8	1.5	0.7	
Spectrum CVD	0	0	0	0.3	0.6	
Ulvac	0	1.2	1.4	3.8	4.2	
Varian	0	0	2.0	1.4	0	
Total LPCVD Reactors	12.9	4.3	8.2	22.9	30.0	23.5%

(Continued)

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Table 28 (Continued)

Chemical Vapor Deposition Company Shares
Japan
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CVD Market	246.5	219.9	259.8	456.2	580.2	24.0%
PECVD Reactors						
Anelva	0	1.2	2.0	0	1.4	
Applied Materials	1.7	3.4	10.0	25.0	59.0	
Enya	4.2	1.6	1.9	4.2	3.5	
E.T. Electrotech	2.4	0.7	5.2	4.9	4.0	
Japan Production	5.9	6.0	4.5	6.5	7.0	
Novellus	0	0	0.5	3.4	5.6	
Plasma-Therm	0	1.2	0.3	0.5	0.6	
Samco	0	0	0	0	1.0	
Sumitomo Metals (ECR)	0	0	0	0	6.0	
Ulvac	2.9	3.0	2.8	2.0	1.0	
Total PECVD Reactors	17.1	17.1	27.2	46.5	89.1	51.1%
Total Jap. Nontube CVD	50.5	39.8	56.8	118.6	172.4	35.9%
Total Japan CVD	110.2	95.3	95.6	184.3	243.2	21.9%

Source: Dataquest (June 1990), Ref: CVDSHR

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Table 29

Chemical Vapor Deposition Company Shares
Europe
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CVD Market	246.5	219.9	259.8	456.2	580.2	24.0%
Tube CVD						
Horizontal Tube LPCVD						
ASM International	5.5	13.3	16.2	16.7	10.0	
BTU International	0.3	2.9	3.0	3.5	3.5	
Enya	0	0	0	0	0	
GSTC (Tempress)	0.6	0.6	0	0.8	0	
Kokusai Electric	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0	0	0	0	0	
Process Technology	1.6	0.7	0.5	0	0.9	
SVG (Thermco)	4.4	2.1	2.2	1.0	1.0	
Solitec	1.4	0.6	0.3	0.6	0	
Tokyo Electron Ltd.	0	0	0	0	0	
Tylan	0.2	0.3	2.0	0	0	
Ulvac/BTU	0	0	0	0	0	
Varian/TEL	0	0	0	0	0	
Wellman	0	0	0	0.5	0.2	
Total Horizontal LPCVD	14.0	20.5	24.2	25.4	15.6	2.7%
Vertical Tube PECVD						
ASM International	0	0	0	0	1.2	
BTU International	0	0	0	0	0	
Denko	0	0	0	0	0	
Disco	0	0	0	0	0	
Helmut Seier	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Kokusai Electric	0	0	0	0	0.3	
Semitherm	0	0	0	0	0.2	
Silcion Valley Group	0	0	0	0.8	0.5	
Tokyo Electron Ltd.	0	0	0	0	0	
Ulvac/BTU	0	0	0	0	0	
Varian/TEL	0	0	0	0	0	
Total Vertical LPCVD	0	0	0	0.8	2.2	NA

(Continued)

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Table 29 (Continued)

Chemical Vapor Deposition Company Shares
Europe
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CVD Market	246.5	219.9	259.8	456.2	580.2	24.0%
Horizontal Tube PECVD						
ASM International	6.2	9.8	5.8	10.3	9.0	
Pacific Western	0.8	1.3	1.4	0.9	0	
Total Horizontal PECVD	7.0	11.1	7.2	11.2	9.0	6.5%
Total Europe Tube CVD	21.0	31.6	31.4	37.4	26.8	6.3%
Nontube CVD Reactors						
APCVD Reactors						
Amaya	0	0	0	0	0	
Applied Materials	0.9	0.7	3.0	3.0	3.0	
GSTC (Tempress)	0.4	0.5	0	0.3	0.3	
Hitachi	0	0	0	0	0	
Kokusai Electric	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0.3	0.4	0	0	0	
Toshiba Machine	0	0	0	0	0	
Watkins-Johnson	0	0.4	6.7	6.0	7.0	
Total APCVD Reactors	1.6	2.0	9.7	9.3	10.3	59.3%
LPCVD Reactors						
Anelva	0	0	0	0	0	
Focus Semiconductor	0	0	0	0	0	
Genus	1.4	1.1	1.7	3.7	7.0	
Silicon Valley Group	3.0	2.5	1.1	0.5	0.7	
Spectrum CVD	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	0	0	1.5	1.4	0	
Total LPCVD Reactors	4.4	3.6	4.3	5.6	7.7	15.0%

(Continued)

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Table 29 (Continued)

Chemical Vapor Deposition Company Shares
Europe
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CVD Market	246.5	219.9	259.8	456.2	580.2	24.0%
PECVD Reactors						
Anelva	0	0	0	0	0	
Applied Materials	1.3	0.7	3.9	8.9	16.0	
Enya	0	0	0	0	0	
E.T. Electrotech	6.5	8.5	7.1	9.8	7.0	
Japan Production	0	0	0	0	0	
Novellus	0	0	0	1.1	3.7	
Plasma-Therm	1.0	0.8	0.5	1.0	0.4	
Samco	0	0	0	0	0	
Sumitomo Metals (ECR)	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Total PECVD Reactors	8.8	10.0	11.5	20.8	27.1	32.5%
Total Eur. Nontube CVD	14.8	15.6	25.5	35.7	45.1	32.1%
Total Europe CVD	35.8	47.2	56.9	73.1	71.9	19.0%

NA = Not applicable
Source: Dataquest (June 1990), Ref: CVDSHR

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Table 30

Chemical Vapor Deposition Company Shares
Rest of World
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CVD Market	246.5	219.9	259.8	456.2	580.2	24.0%
Tube CVD						
Horizontal Tube LPCVD						
ASM International	1.6	0.7	0	2.6	1.0	
BTU International	0.4	0	1.5	3.6	5.0	
Enya	0	0	0	0	0	
GSTC (Tempress)	1.4	0.7	0	0	0	
Kokusai Electric	0	0	0	2.0	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0	0	0	0	0	
Process Technology	0.1	0.2	0	0	0	
SVG (Thermco)	1.6	1.4	1.8	2.0	2.0	
Solitec	0.7	0.6	1.3	0.6	1.0	
Tokyo Electron Ltd.	0	0	0	3.8	6.0	
Tylan	1.5	0	1.0	0	0	
Ulvac/BTU	0	0	0	0	0	
Varian/TEL	0	0	0	0	0	
Wellman	0	0	0	0	0	
Total Horizontal LPCVD	7.3	3.6	5.6	14.6	17.0	23.5%
Vertical Tube LPCVD						
ASM International	0	0	0	0	0.6	
BTU International	0	0	0	0	0	
Denko	0	0	0	0	0	
Disco	0	0	0	0	0	
Helmut Seier	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Kokusai Electric	0	0	0	6.8	10.0	
Semitherm	0	0	0	0	0	
Silcion Valley Group	0	0	0	0.4	0.5	
Tokyo Electron Ltd.	0	0	0	0	0	
Ulvac/BTU	0	0	0	0	0	
Varian/TEL	0	0	0	0	0	
Total Vertical LPCVD	0	0	0	7.2	11.1	NA

(Continued)

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Table 30 (Continued)

Chemical Vapor Deposition Company Shares
Rest of World
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CVD Market	246.5	219.9	259.8	456.2	580.2	24.0%
Horizontal Tube PECVD						
ASM International	3.0	3.3	5.8	5.2	9.0	
Pacific Western	0	0	0	0.5	0	
Total Horizontal PECVD	3.0	3.3	5.8	5.7	9.0	31.6%
Total ROW Tube CVD	10.3	6.9	11.4	27.5	37.1	37.8%
Nontube CVD Reactors						
APCVD Reactors						
Amaya	0	0	0	0	0	
Applied Materials	0.9	0.5	0	1.0	3.0	
GSTC (Tempress)	0.1	0.1	0	0.5	0.5	
Hitachi	0	0	0	0	0	
Kokusai Electric	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0	0	0	0	0	
Toshiba Machine	0	0	0	0	0	
Watkins-Johnson	1.5	1.6	0	4.5	9.0	
Total APCVD Reactors	2.5	2.2	0	6.0	12.5	49.5%
LPCVD Reactors						
Anelva	0	0	0	0	0	
Focus Semiconductor	0	0	0	0	0	
Genus	1.4	1.1	1.1	5.3	10.0	
Silicon Valley Group	1.0	1.0	0.4	0.5	0	
Spectrum CVD	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	0	0	1.5	0.7	0	
Total LPCVD Reactors	2.4	2.1	3.0	6.5	10.0	42.9%

(Continued)

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Table 30 (Continued)

Chemical Vapor Deposition Company Shares
Rest of World
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CVD Market	246.5	219.9	259.8	456.2	580.2	24.0%
PECVD Reactors						
Anelva	0	0	0	0	0	
Applied Materials	1.0	0.6	1.6	4.5	12.0	
Enya	0	0	0	0	0	
E.T. Electrotech	1.0	2.0	0	1.4	2.0	
Japan Production	0	0	0	0	0	
Novellus	0	0	0	2.3	4.7	
Plasma-Therm	0.8	0.8	0	0.5	0	
Samco	0	0	0	0	0	
Sumitomo Metals (ECR)	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Total PECVD Reactors	2.8	3.4	1.6	8.7	18.7	60.8%
Total ROW Nontube CVD	7.7	7.7	4.6	21.2	41.2	52.1%
Total ROW CVD	18.0	14.6	16.0	48.7	78.3	44.4%

NA = Not applicable
Source: Dataquest (June 1990), Ref: CVDSHR

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Table 31

Chemical Vapor Deposition Company Shares Worldwide (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CVD Market	245.5	219.9	259.8	456.2	580.2	24.0%
Tube CVD						
Horizontal Tube LPCVD						
ASM International	13.9	20.0	19.9	25.8	15.0	
BTU International	6.7	5.6	7.9	14.5	17.5	
Enya	1.3	1.0	0.6	1.8	1.7	
GSTC (Tempress)	7.6	3.8	0	3.8	3.0	
Kokusai Electric	14.6	16.2	7.6	9.2	2.2	
Koyo Lindberg	1.9	1.8	1.0	1.8	3.0	
Pacific Western	0.4	0.5	0	0	0	
Process Technology	5.7	5.4	4.3	4.0	4.1	
SVG (Thermco)	9.1	6.4	7.0	6.5	10.0	
Solitec	12.9	5.3	3.6	6.0	5.0	
Tokyo Electron Ltd.	15.0	6.6	8.3	14.6	14.7	
Tylan	2.3	0.7	4.0	1.5	0.5	
Ulvac/BTU	0	0	0.5	3.5	4.0	
Varian/TEL	0	0	0	0	0	
Wellman	0	0	0	0.5	0.2	
Total Horizontal LPCVD	91.4	73.3	64.7	93.5	80.9	(2.4%)
Vertical Tube LPCVD						
ASM International	0	0.5	0	0	3.0	
BTU International	0	0	0	0	0	
Denko	1.3	2.7	2.1	2.3	3.5	
Disco	0	0	0	0	0	
Helmut Seier	0.3	0	0.3	0.3	0	
Koyo Lindberg	0	0.4	1.0	2.7	1.1	
Kokusai Electric	0	1.4	2.8	21.6	32.5	
Semitherm	0	0	0	0.5	1.2	
Silcion Valley Group	0	0.2	1.6	3.6	4.0	
Tokyo Electron Ltd.	1.0	1.0	0	3.8	6.0	
Ulvac/BTU	0	0	0	0	0	
Varian/TEL	0	0	0	0	3.0	
Total Vertical LPCVD	2.6	6.2	7.8	34.8	54.3	113.8%

(Continued)

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Table 31 (Continued)

Chemical Vapor Deposition Company Shares
Worldwide
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CVD Market	246.5	219.9	259.8	456.2	580.2	24.0%
Horizontal Tube PECVD						
ASM International	40.4	44.4	44.5	51.6	51.0	
Pacific Western	8.7	6.9	7.9	6.2	3.0	
Total Horizontal PECVD	49.1	51.3	52.4	57.8	54.0	2.4%
Total WW Tube CVD	143.1	130.8	124.9	186.1	189.2	7.5%
Nontube CVD Reactors						
APCVD Reactors						
Amaya	10.9	6.0	5.5	17.5	19.0	
Applied Materials	9.9	7.8	14.5	15.7	15.0	
GSTC (Tempress)	2.1	2.2	0	1.8	1.3	
Hitachi	0.3	0.4	0	0.2	0.5	
Kokusai Electric	0.7	0.7	0	0	0	
Koyo Lindberg	0.6	0.4	0.2	1.3	0.6	
Pacific Western	1.4	1.2	0.2	0	0	
Toshiba Machine	0	4.3	5.0	6.0	4.2	
Watkins-Johnson	5.9	8.1	16.0	36.0	49.0	
Total APCVD Reactors	31.8	31.1	41.4	78.5	89.6	29.6%
LPCVD Reactors						
Anelva	0	0	0.7	2.3	1.5	
Focus Semiconductor	0	0	1.0	2.5	0	
Genus	17.5	7.5	13.2	33.4	62.0	
Silicon Valley Group	15.6	8.8	3.7	4.0	2.0	
Spectrum CVD	0	0.5	2.3	1.4	2.6	
Ulvac	0	1.2	1.4	3.8	4.2	
Varian	0	1.1	7.5	5.5	0.7	
Total LPCVD Reactors	33.1	19.1	29.8	52.9	73.0	21.9%

(Continued)

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Table 31 (Continued)

Chemical Vapor Deposition Company Shares Worldwide (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CVD Market	246.5	219.9	259.8	456.2	580.2	24.0%
PECVD Reactors						
Anelva	0	1.2	2.0	0	1.4	
Applied Materials	6.3	6.1	31.0	75.4	143.0	
Enya	4.2	1.6	1.9	4.2	3.5	
E.T. Electrotech	13.6	15.2	13.3	20.3	15.5	
Japan Production	5.9	6.0	4.5	6.5	7.0	
Novellus	0	0	3.6	23.7	47.0	
Plasma-Therm	5.6	5.8	4.6	6.0	3.0	
Samco	0	0	0	0	1.0	
Sumitomo Metals (ECR)	0	0	0	0	6.0	
Ulvac	2.9	3.0	2.8	2.6	1.0	
Total PECVD Reactors	38.5	38.9	63.7	138.7	228.4	56.1%
Total WW Nontube CVD	103.4	89.1	134.9	270.1	391.0	39.4%
Total Worldwide CVD	246.5	219.9	259.8	456.2	580.2	24.0%

Source: Dataquest (June 1990), Ref: CVDSHR

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Table 32

Physical Vapor Deposition Company Shares
United States
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World PVD Market	263.0	236.6	253.9	305.0	377.1	9.4%
Sputtering						
Anelva	3.0	2.6	10.0	10.0	10.9	
Balzers	4.0	5.6	5.0	5.0	4.0	
CHA Industries	1.0	0.7	0.3	0.7	1.1	
CPA	4.5	2.0	2.0	2.6	2.0	
CVC Products	7.0	10.0	6.8	7.5	9.0	
Edwards High Vacuum	0	0	0	0	0	
E.T. Electrotech	3.1	1.3	1.4	1.8	3.0	
Innotec	1.8	1.8	2.4	4.2	1.3	
Ion Tech	0.5	0.5	0.7	0.5	0.8	
Kurt J. Lesker	0.8	0.8	0.8	0.8	0.8	
Leybold-Heraeus	3.8	2.8	6.0	6.0	5.0	
Materials Research	24.0	15.0	13.0	15.0	24.0	
Perkin-Elmer	4.0	3.3	2.1	0.9	1.0	
Sputtered Films	1.0	1.3	1.0	0.6	1.5	
Temescal	1.3	1.3	0	0	0	
Tokuda	0	0	0	0	0	
Ulvac	0.5	1.5	6.3	6.4	6.2	
Varian	32.8	25.6	21.3	24.6	28.0	
Others	0.1	1.0	3.1	5.1	1.9	
Total Sputtering	93.2	77.1	82.2	91.7	100.5	1.9%
Evaporation						
Anelva	0.4	2.3	0	0	0	
Balzers	4.0	1.8	1.1	1.1	1.5	
CHA Industries	7.1	5.6	6.0	6.3	5.5	
CVC Products	0	0	0	1.0	1.0	
Edwards High Vacuum	0	0	0	0	0	
Innotec	0.3	0.2	0	1.0	0.3	
Kurt J. Lesker	0.5	0.3	0.3	0.3	0.4	
Leybold-Heraeus	1.5	1.0	0.5	0.5	0.8	
Temescal	5.5	5.7	5.1	4.5	5.0	
Ulvac	0.8	1.0	1.4	1.5	1.6	
Others	0.1	0.2	0.2	0.2	1.2	
Total Evaporation	20.2	18.1	14.6	16.4	17.3	(3.8%)
Total US PVD	113.4	95.2	96.8	108.1	117.8	1.0%

Source: Dataquest (June 1990), Ref: PVDSHR

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Table 33

Physical Vapor Deposition Company Shares
Japan
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World PVD Market	263.0	236.6	253.9	305.0	377.1	9.4%
Sputtering						
Anelva	27.3	18.0	34.7	43.8	65.0	
Balzers	0	0	0	0	0	
CHA Industries	0	0	0	0	0	
CPA	0	0.9	1.0	0	0	
CVC Products	0	0	0	0.3	0	
Edwards High Vacuum	0	0	0	0	0	
E.T. Electrotech	1.7	0.5	0.6	0.6	1.6	
Innotec	0.8	0	0	0	0	
Ion Tech	0.3	0.2	0	0	0	
Kurt J. Lesker	0	0	0	0	0	
Leybold-Heraeus	0	0	0	0	0	
Materials Research	5.5	0.9	1.9	7.5	13.0	
Perkin-Elmer	3.8	0	0	0	0	
Sputtered Films	0	0	0	0	0	
Temescal	0	0	0	0	0	
Tokuda	5.0	3.3	11.1	7.0	5.6	
Ulvac	16.4	14.7	24.7	40.1	43.6	
Varian	14.9	16.8	12.6	18.7	24.0	
Others	0	0	0	0	0	
Total Sputtering	75.7	55.3	86.6	118.0	152.8	19.2%
Evaporation						
Anelva	0	0	4.9	6.2	4.3	
Balzers	0.8	0.4	0	0	1.4	
CHA Industries	0	0	0	0	0	
CVC Products	0	0	0	0	0	
Edwards High Vacuum	0	0	0	0	0	
Innotec	0	0	0	0	0	
Kurt J. Lesker	0	0	0	0	0	
Leybold-Heraeus	0	0	0	0	0	
Temescal	1.4	1.8	2.4	2.4	3.5	
Ulvac	16.0	19.0	5.9	11.5	13.0	
Others	0	0	0	0	0	
Total Evaporation	18.2	21.2	13.2	20.1	22.2	5.1%
Total Japan PVD	93.9	76.5	99.8	138.1	175.0	16.8%

Source: Dataquest (June 1990), Ref: PVDSHR

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Table 34

Physical Vapor Deposition Company Shares
Europe
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World PVD Market	263.0	236.6	253.9	305.0	377.1	9.4%
Sputtering						
Anelva	0	0	0	0	1.5	
Balzers	6.1	7.6	8.9	6.0	4.2	
CHA Industries	0	0	0	0	0	
CPA	0	0	0	0	0	
CVC Products	2.5	3.5	2.9	3.5	2.0	
Edwards High Vacuum	0	0	0	0	0	
E.T. Electrotech	3.9	3.5	4.0	6.0	10.0	
Innotec	0	0	0	0	0.3	
Ion Tech	0	0	0	0	0	
Kurt J. Lesker	0	0	0	0	0	
Leybold-Heraeus	5.0	6.0	7.0	4.8	6.0	
Materials Research	6.4	3.5	4.0	4.0	5.0	
Perkin-Elmer	1.0	1.0	0.3	0	0	
Sputtered Films	0	0	0	0	0	
Temescal	0.8	0	0	0	0	
Tokuda	0	0	0	0	0	
Ulvac	3.3	4.6	2.0	1.2	5.9	
Varian	4.6	8.3	6.3	6.0	7.0	
Others	0	0	0	0	0	
Total Sputtering	33.6	38.0	35.4	31.5	41.9	5.7%
Evaporation						
Anelva	0	0	0	0	0	
Balzers	5.6	2.8	1.8	1.8	1.5	
CHA Industries	0	0	0	0	0	
CVC Products	0	0	0	0.6	0.6	
Edwards High Vacuum	0	0	0	0	0	
Innotec	0	0	0	0	0.3	
Kurt J. Lesker	0	0	0	0	0	
Leybold-Heraeus	2.5	2.0	1.0	0	1.0	
Temescal	3.3	3.0	2.4	1.8	2.1	
Ulvac	0	2.4	0.1	0.3	0	
Others	0	0	0	0	0	
Total Evaporation	11.4	10.2	5.3	4.5	5.5	(16.7%)
Total Europe PVD	45.0	48.2	40.7	36.0	47.4	1.3%

Source: Dataquest (June 1990), Ref: PVDSHR

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Table 35

Physical Vapor Deposition Company Shares
Rest of World
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World PVD Market	263.0	236.6	253.9	305.0	377.1	9.4%
Sputtering						
Anelva	0.5	1.2	0	0	3.6	
Balzers	0	0	0	0	0	
CHA Industries	0	0	0	0	0	
CPA	0	0	0	0	0	
CVC Products	0	0	0	1.0	1.0	
Edwards High Vacuum	0	0	0	0	0	
E.T. Electrotech	0	0	0	0.6	1.5	
Innotec	0	0	0	0	0.3	
Ion Tech	0	0	0	0	0	
Kurt J. Lesker	0	0	0	0	0	
Leybold-Heraeus	0	0.8	2.0	0	0.8	
Materials Research	1.9	2.5	4.2	7.5	12.0	
Perkin-Elmer	1.1	1.3	0.7	0	0	
Sputtered Films	0	0.3	0	0	0	
Temescal	0	0	0	0	0	
Tokuda	0	0	0	0	0	
Ulvac	2.4	4.6	1.0	1.0	0	
Varian	4.8	6.0	8.1	12.0	14.0	
Others	0	0	0	0	0	
Total Sputtering	10.7	16.7	16.0	22.1	33.2	32.7%
Evaporation						
Anelva	0	0	0	0	0	
Balzers	0	0	0	0	1.0	
CHA Industries	0	0	0	0	1.5	
CVC Products	0	0	0	0	0.4	
Edwards High Vacuum	0	0	0	0	0	
Innotec	0	0	0	0	0	
Kurt J. Lesker	0	0	0	0	0.2	
Leybold-Heraeus	0	0	0	0	0	
Temescal	0	0	0	0	0.6	
Ulvac	0	0	0.6	0.7	0	
Others	0	0	0	0	0	
Total Evaporation	0	0	0.6	0.7	3.7	NA
Total ROW PVD	10.7	16.7	16.6	22.8	36.9	36.3%

NA = Not applicable
Source: Dataquest (June 1990), Ref: PVDSHR

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Table 36

Physical Vapor Deposition Company Shares Worldwide (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World PVD Market	263.0	236.6	253.9	305.0	377.1	9.4%
Sputtering						
Anelva	30.8	21.8	44.7	53.8	81.0	
Balzers	10.1	13.2	13.9	11.0	8.2	
CHA Industries	1.0	0.7	0.3	0.7	1.1	
CPA	4.5	2.9	3.0	2.6	2.0	
CVC Products	9.5	13.5	9.7	12.3	12.0	
Edwards High Vacuum	0	0	0	0	0	
E.T. Electrotech	8.7	5.3	6.0	9.0	16.1	
Innotec	2.6	1.8	2.4	4.2	1.9	
Ion Tech	0.8	0.7	0.7	0.5	0.8	
Kurt J. Lesker	0.8	0.8	0.8	0.8	0.8	
Leybold-Heraeus	8.8	9.6	15.0	10.8	11.8	
Materials Research	37.8	21.9	23.1	34.0	54.0	
Perkin-Elmer	9.9	5.6	3.1	0.9	1.0	
Sputtered Films	1.0	1.6	1.0	0.6	1.5	
Temescal	2.1	1.3	0	0	0	
Tokuda	5.0	3.3	11.1	7.0	5.6	
Ulvac	22.6	25.4	34.0	48.7	55.7	
Varian	57.1	56.7	48.3	61.3	73.0	
Others	0.1	1.0	3.1	5.1	1.9	
Total Sputtering	213.2	187.1	220.2	263.3	328.4	11.4%
Evaporation						
Anelva	0.4	2.3	4.9	6.2	4.3	
Balzers	10.4	5.0	2.9	2.9	5.4	
CHA Industries	7.1	5.6	6.0	6.3	7.0	
CVC Products	0	0	0	1.6	2.0	
Edwards High Vacuum	0	0	0	0	0	
Innotec	0.3	0.2	0	1.0	0.6	
Kurt J. Lesker	0.5	0.3	0.3	0.3	0.6	
Leybold-Heraeus	4.0	3.0	1.5	0.5	1.8	
Temescal	10.2	10.5	9.9	8.7	11.2	
Ulvac	16.8	22.4	8.0	14.0	14.6	
Others	0.1	0.2	0.2	0.2	1.2	
Total Evaporation	49.8	49.5	33.7	41.7	48.7	(0.6%)
Total Worldwide PVD	263.0	236.6	253.9	305.0	377.1	9.4%

Source: Dataquest (June 1990), Ref: PVDSHR

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Table 37

Silicon Epitaxy Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
Total Epitaxy Market	71.5	46.3	35.5	84.5	71.7	0.1%
United States						
Applied Materials	18.7	12.2	6.4	25.5	13.0	
ASM Epitaxy	0	0	0	1.5	3.8	
Kokusai Electric	0	0	0	0	0	
Lam Research	8.6	4.0	7.0	15.0	12.8	
LPE	0	0	0	0	0	
Rapro	0	0	0	0	0.9	
Shimada	0	0	0	0	0	
Sitesa	0	0	0	0	0	
Toshiba Machine	0	0	0	0	0	
Total United States	27.3	16.2	13.4	42.0	30.5	2.8%
Japan						
Applied Materials	14.3	8.1	8.0	16.5	5.4	
ASM Epitaxy	0	0	0	0.8	0	
Kokusai Electric	5.0	2.1	1.5	4.2	5.7	
Lam Research	3.8	1.8	2.9	0	4.8	
LPE	0	0	0	0	0	
Rapro	0	0	0	0	0	
Shimada	0.8	0.5	0	0	0	
Sitesa	0	0	0	0	0	
Toshiba Machine	2.3	1.0	0.6	2.0	1.3	
Total Japan	26.2	13.5	13.0	23.5	17.2	(10.0%)
Europe						
Applied Materials	8.0	8.0	3.6	4.4	3.0	
ASM Epitaxy	0	0	0	0.8	2.4	
Kokusai Electric	0	0	0	0	0	
Lam Research	5.0	3.2	2.8	1.0	3.8	
LPE	0	0	0	2.7	3.0	
Rapro	0	0	0	0	0	
Shimada	0	0	0	0	0	
Sitesa	0	0	0	4.5	4.9	
Toshiba Machine	0	0	0	0	0	
Total Europe	13.0	11.2	6.4	13.4	17.1	7.1%

(Continued)

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Table 37 (Continued)

Silicon Epitaxy Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
Total Epitaxy Market	71.5	46.3	35.5	84.5	71.7	0.1%
Rest of World						
Applied Materials	3.0	3.0	0.6	0.8	0.8	
ASM Epitaxy	0	0	0	0	0	
Kokusai Electric	0	0	0	0	0	
Lam Research	2.0	2.4	2.1	3.0	4.3	
LPE	0	0	0	1.8	1.8	
Rapro	0	0	0	0	0	
Shimada	0	0	0	0	0	
Sitesa	0	0	0	0	0	
Toshiba Machine	0	0	0	0	0	
Total Rest of World	5.0	5.4	2.7	5.6	6.9	8.4%
Worldwide						
Applied Materials	44.0	31.3	18.6	47.2	22.2	
ASM Epitaxy	0	0	0	3.1	6.2	
Kokusai Electric	5.0	2.1	1.5	4.2	5.7	
Lam Research	19.4	11.4	14.8	19.0	25.7	
LPE	0	0	0	4.5	4.8	
Rapro	0	0	0	0	0.9	
Shimada	0.8	0.5	0	0	0	
Sitesa	0	0	0	4.5	4.9	
Toshiba Machine	2.3	1.0	0.6	2.0	1.3	
Total Worldwide	71.5	46.3	35.5	84.5	71.7	0.1%

Source: Dataquest (June 1990), Ref: EPISHR

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Table 38

Metalorganic CVD Company Shares
United States and Japan
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World MOCVD Market	24.8	31.4	34.6	42.0	43.8	15.3%
United States						
Aixtron	0	0	0	0.8	3.5	
Crystal Specialties	1.8	2.2	1.7	2.3	0	
CVD Equipment	1.5	0.6	1.2	1.0	1.0	
CVT	0	0	0	0	0	
Daiwa Semiconductor	0	0	0	0	0	
EEV	0	0.2	0	0	0	
Emcore	0.1	2.3	5.1	6.5	7.5	
MR Semicon (Cambridge)	1.9	1.1	1.5	1.3	1.2	
Nippon EMC	0	0	0	0	0	
Nippon Sanso	0	0	0.2	0	0	
Samco	0	0	0	0	0	
Seiden	0	0	0	0	0	
Semco Engineering	0	0	0	0	0	
Shimada Rika	0	0	0	0	0	
Spire	3.0	2.9	1.3	1.5	1.7	
TEL	0	0	0	0	0	
Thomas Schwonn	0.6	0	0	0.4	0	
Toyoko Chemical	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Total United States	8.9	9.3	11.0	13.8	14.9	13.7%
Japan						
Aixtron	0	0	0	0	0	
Crystal Specialties	0	0.5	0.9	0.4	0	
CVD Equipment	0	0	0	0	0	
CVT	0	0	0	0	0	
Daiwa Semiconductor	0	0.4	0.4	0.5	0	
EEV	0	0	0	0	0	
Emcore	0	0	0	0.5	2.5	
MR Semicon (Cambridge)	0.3	0.4	0	0	0	
Nippon EMC	1.1	1.5	1.4	1.9	2.2	
Nippon Sanso	3.6	4.6	4.7	6.3	5.7	
Samco	0.7	0.7	0.6	1.0	0.6	
Seiden	0.9	1.3	0.6	0.6	0	
Semco Engineering	0	0	0	0	0	
Shimada Rika	0	0.3	0	0	0	

(Continued)

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Table 38 (Continued)

Metalorganic CVD Company Shares
United States and Japan
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
Japan (Continued)						
Spire	0	0	0	0.6	0.7	
TEL	2.3	3.0	2.9	1.7	2.9	
Thomas Schwonn	0	0	0	0	0	
Toyoko Chemical	0.7	1.0	0.7	1.2	0	
Ulvac	1.9	2.3	1.9	2.2	2.0	
Total Japan	11.5	16.0	14.1	16.9	16.6	9.6%

Source: Dataquest (June 1990), Ref: MOCVDSHR

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Table 39

Metalorganic CVD Company Shares Europe and Rest of World (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World MOCVD Market	24.8	31.4	34.6	42.0	43.8	15.3%
Europe						
Aixtron	0.5	1.7	4.9	6.7	6.7	
Crystal Specialties	0	0	0	0	0	
CVD Equipment	0	0	0	0	0	
CVT	0.7	0.4	1.1	1.6	1.1	
Daiwa Semiconductor	0	0	0	0	0	
EEV	1.0	1.2	0.7	0	0	
Emcore	0	0	0	0	0	
MR Semicon (Cambridge)	1.6	1.4	1.5	1.0	0.8	
Nippon EMC	0	0	0	0	0	
Nippon Sanso	0	0	0	0	0	
Samco	0	0	0	0	0	
Seiden	0	0	0	0	0	
Semco Engineering	0	0	0.3	0.9	1.0	
Shimada Rika	0	0	0	0	0	
Spire	0	0.4	0	0	0	
TEL	0	0	0	0	0	
Thomas Schwonn	0.3	0.3	0.7	0.4	0	
Toyoko Chemical	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Total Europe	4.1	5.4	9.2	10.6	9.6	23.7%
Rest of World						
Aixtron	0	0	0	0	0.4	
Crystal Specialties	0	0	0	0	0	
CVD Equipment	0	0	0	0.3	0.3	
CVT	0	0	0	0	0.9	
Daiwa Semiconductor	0	0	0	0	0	
EEV	0	0	0	0	0	
Emcore	0	0	0	0	0	
MR Semicon (Cambridge)	0.3	0.7	0.3	0.4	0	
Nippon EMC	0	0	0	0	0	
Nippon Sanso	0	0	0	0	1.1	
Samco	0	0	0	0	0	
Seiden	0	0	0	0	0	
Semco Engineering	0	0	0	0	0	
Shimada Rika	0	0	0	0	0	

(Continued)

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Table 39 (Continued)

Metalorganic CVD Company Shares
Europe and Rest of World
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
Rest of World (Continued)						
Spire	0	0	0	0	0	
TEL	0	0	0	0	0	
Thomas Schwonn	0	0	0	0	0	
Toyoko Chemical	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Total Rest of World	0.3	0.7	0.3	0.7	2.7	73.2%

Source: Dataquest (June 1990), Ref: MOCVDSHR

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Table 40

Metalorganic CVD Company Shares
Worldwide
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World MOCVD Market	24.8	31.4	34.6	42.0	43.8	15.3%
Worldwide						
Aixtron	0.5	1.7	4.9	7.5	10.6	
Crystal Specialties	1.8	2.7	2.6	2.7	0	
CVD Equipment	1.5	0.6	1.2	1.3	1.3	
CVT	0.7	0.4	1.1	1.6	2.0	
Daiwa Semiconductor	0	0.4	0.4	0.5	0	
EEV	1.0	1.4	0.7	0	0	
Emcore	0.1	2.3	5.1	7.0	10.0	
MR Semicon (Cambridge)	4.1	3.6	3.3	2.7	2.0	
Nippon EMC	1.1	1.5	1.4	1.9	2.2	
Nippon Sanso	3.6	4.6	4.9	6.3	6.8	
Samco	0.7	0.7	0.6	1.0	0.6	
Seiden	0.9	1.3	0.6	0.6	0	
Semco Engineering	0	0	0.3	0.9	1.0	
Shimada Rika	0	0.3	0	0	0	
Spire	3.0	3.3	1.3	2.1	2.4	
TEL	2.3	3.0	2.9	1.7	2.9	
Thomas Schwonn	0.9	0.3	0.7	0.8	0	
Toyoko Chemical	0.7	1.0	0.7	1.2	0	
Ulvac	1.9	2.3	1.9	2.2	2.0	
Total Worldwide	24.8	31.4	34.6	42.0	43.8	15.3%

Source: Dataquest (June 1990), Ref: MOCVDSHR

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Table 41

Molecular Beam Epitaxy Company Shares Regional (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World MBE Market	52.6	65.8	68.0	80.9	72.6	8.4%
United States						
Anelva	0	0	0	0	0	
Eiko	0	0	0	0	0	
ISA Riber	4.8	5.4	7.0	8.0	6.5	
Perkin-Elmer	6.0	7.2	5.0	2.8	0	
Seiko	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	4.5	6.3	5.2	5.4	7.8	
VG Instruments	6.0	5.4	2.5	5.1	6.5	
Total United States	21.3	24.3	19.7	21.3	20.8	(0.6%)
Japan						
Anelva	6.3	7.2	9.7	11.5	7.2	
Eiko	1.0	1.2	1.4	1.2	2.9	
ISA Riber	2.4	3.5	6.0	3.9	1.4	
Perkin-Elmer	0	0	0	0	0	
Seiko	0.8	2.0	1.2	1.4	0	
Ulvac	3.4	4.4	4.3	7.5	4.0	
Varian	0.9	0.8	1.9	5.2	0.5	
VG Instruments	2.4	4.2	8.1	5.6	4.9	
Total Japan	17.2	23.3	32.6	36.3	20.9	5.0%
Europe						
Anelva	0	0	0	0	0	
Eiko	0	0	0	0	0	
ISA Riber	6.0	4.7	4.9	6.9	8.0	
Perkin-Elmer	0	0	0	0	0	
Seiko	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	1.8	3.0	4.4	6.3	8.9	
VG Instruments	4.0	8.7	2.4	5.8	6.8	
Total Europe	11.8	16.4	11.7	19.0	23.7	19.0%

(Continued)

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Table 41 (Continued)

Molecular Beam Epitaxy Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World MBE Market	52.6	65.8	68.0	80.9	72.6	8.4%
Rest of World						
Anelva	0	0	0	0	0	
Eiko	0	0	0	0	0	
ISA Riber	1.2	0	1.4	3.7	6.4	
Perkin-Elmer	0	0	0	0	0	
Seiko	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	0	0.7	0.6	0.6	0	
VG Instruments	1.1	1.1	2.0	0	0.8	
Total Rest of World	2.3	1.8	4.0	4.3	7.2	33.0%
Worldwide						
Anelva	6.3	7.2	9.7	11.5	7.2	
Eiko	1.0	1.2	1.4	1.2	2.9	
ISA Riber	14.4	13.6	19.3	22.5	22.3	
Perkin-Elmer	6.0	7.2	5.0	2.8	0	
Seiko	0.8	2.0	1.2	1.4	0	
Ulvac	3.4	4.4	4.3	7.5	4.0	
Varian	7.2	10.8	12.1	17.5	17.2	
VG Instruments	13.5	19.4	15.0	16.5	19.0	
Total Worldwide	52.6	65.8	68.0	80.9	72.6	8.4%

Source: Dataquest (June 1990), Ref: MBESHR

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Table 42

Diffusion Furnace Company Shares
United States
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Diffusion Market	207.2	155.6	145.3	294.9	327.4	12.1%
Horizontal Tube						
ASM International	3.6	3.3	2.3	3.4	2.5	
BTU International	29.2	18.3	8.3	17.3	18.0	
Denko	0	0	0	0	0	
Gasonics	5.3	6.1	7.5	9.0	8.0	
GSTC (Tempress)	6.0	2.0	0.5	3.0	4.0	
Kokusai Electric	0	0	0	1.2	1.7	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	1.1	0.6	0	0	0	
Process Technology	0	0	0	0	0	
Silicon Valley Group (Thermco)	20.3	12.4	15.7	42.0	34.0	
Solitec	0	0.2	0	0	0.5	
Tokyo Electron Ltd.	0	0	0	0	0	
Tylan	1.2	1.7	2.0	2.5	1.0	
Ulvac/BTU	0	0	0	0	0	
Varian/TEL	0	0	0	0	0	
Others	0	0	0	0	0	
Total Horizontal	66.7	44.6	36.3	78.4	69.7	1.1%
Vertical Tube						
ASM International	0	0	0	0	1.0	
BTU International	0	0	0	1.0	0	
Denko	0	0	0	0	0	
Disco	0	0	0	0	0	
Helmut Seier	0.3	0.2	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Kokusai Electric	0	0	0	2.7	4.1	
Semitherm	0	0	0	0.5	2.0	
Silicon Valley Group	0	0.2	0.8	2.0	3.0	
Tokyo Electron Ltd.	0	0	0	0	0	
Ulvac/BTU	0	0	0	0	0	
Varian/TEL	0	0	0	0	5.8	
Total Vertical	0.3	0.4	0.8	6.2	15.9	169.8%
Total United States	67.0	45.0	37.1	84.6	85.6	6.3%

Source: Dataquest (June 1990), Ref: DIFFSHR

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Table 43

Diffusion Furnace Company Shares
Japan
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Diffusion Market	207.2	155.6	145.4	294.9	327.4	12.1%
Horizontal Tube						
ASM International	0	0	0	0	2.0	
BTU International	0.6	0.4	0	0	0	
Denko	0.6	0.6	0.8	0.9	0	
Gasonics	0	0	0	0	0	
GSTC (Tempress)	0	0	0	0.5	0	
Kokusai Electric	16.8	12.0	16.7	13.4	8.7	
Koyo Lindberg	9.7	6.0	2.6	3.3	5.0	
Pacific Western	0	0	0	0	0	
Process Technology	0	0	0	0	0	
Silicon Valley Group (Thermco)	0	0	0	0	0	
Solitec	0	0	0	0	0	
Tokyo Electron Ltd.	60.0	49.0	22.9	44.6	52.0	
Tylan	0	0	0	0	0	
Ulvac/BTU	0.5	0.4	1.7	9.2	10.0	
Varian/TEL	0	0	0	0	0	
Others	0	0	0	0	0	
Total Horizontal	88.2	68.4	44.7	71.9	77.7	(3.1%)
Vertical Tube						
ASM International	0	0	0	0	2.0	
BTU International	0	0	0	0	0	
Denko	0.4	1.2	1.2	1.8	4.0	
Disco	0.3	0.7	1.5	2.9	3.6	
Helmut Seier	0.3	0.3	0.5	0.7	0	
Koyo Lindberg	0.6	1.8	3.1	3.5	3.1	
Kokusai Electric	0.5	1.8	7.3	13.5	20.3	
Semitherm	0	0	0	0	0	
Silicon Valley Group	0	0	0	0.8	0	
Tokyo Electron Ltd.	0	0	0.7	8.0	16.9	
Ulvac/BTU	0	0	0	2.3	2.3	
Varian/TEL	0	0	0	0	0	
Total Vertical	2.1	5.8	14.3	33.5	52.2	123.3%
Total Japan	90.3	74.2	59.0	105.4	129.9	9.5%

Source: Dataquest (June 1990), Ref: DIFFSHR

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Table 44

Diffusion Furnace Company Shares
Europe
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Diffusion Market	207.2	155.6	145.4	294.9	327.4	12.1%
Horizontal Tube						
ASM International	13.3	13.3	16.2	19.3	16.0	
BTU International	4.9	4.2	7.3	8.2	9.0	
Denko	0	0	0	0	0	
Gasonics	0	0	0	0	0	
GSTC (Tempress)	0	0	0	0.8	1.0	
Kokusai Electric	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0	0	0	0	0	
Process Technology	0	0	0	0	0	
Silicon Valley Group (Thermco)	15.6	11.2	13.2	12.0	12.0	
Solitec	0	0	0	0	0	
Tokyo Electron Ltd.	0	0	0	2.3	0	
Tylan	0.1	0.8	0	0	0	
Ulvac/BTU	0	0	0	0	0	
Varian/TEL	0	0	0	0	0.7	
Others	1.6	1.7	2.5	3.5	1.5	
Total Horizontal	35.5	31.2	39.2	46.1	40.2	3.2%
Vertical Tube						
ASM International	0	0	0	0	3.0	
BTU International	0	0	0	0	0	
Denko	0	0	0	0	0	
Disco	0	0	0	0	0	
Helmut Seier	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Kokusai Electric	0	0	0	0	0	
Semitherm	0	0	0	0	1.0	
Silicon Valley Group	0	0	0	0.8	1.0	
Tokyo Electron Ltd.	0	0	0	0	0	
Ulvac/BTU	0	0	0	0	0	
Varian/TEL	0	0	0	0	0	
Total Vertical	0	0	0	0.8	5.0	NA
Total Europe	35.5	31.2	39.2	46.9	45.2	6.2%

NA = Not applicable
Source: Dataquest (June 1990), Ref: DIFPSHR

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Table 45

Diffusion Furnace Company Shares
Rest of World
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Diffusion Market	207.2	155.6	145.4	294.9	327.4	12.1%
Horizontal Tube						
ASM International	1.0	0	0	0	1.5	
BTU International	1.5	1.1	3.7	8.5	14.0	
Denko	0	0	0	0	0	
Gasonics	0	0	0	0	0	
GSTC (Tempress)	0	0	0	0	0	
Kokusai Electric	0	0	0	4.6	7.0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0	0	0	0	0	
Process Technology	0	0	0	0	0	
Silicon Valley Group (Thermco)	9.2	4.0	6.0	6.0	6.0	
Solitec	0	0.1	0	0	0.2	
Tokyo Electron Ltd.	0	0	0	27.7	21.0	
Tylan	2.7	0	0	0	0	
Ulvac/BTU	0	0	0	0	0	
Varian/TEL	0	0	0	0	0	
Others	0	0	0	0	0	
Total Horizontal	14.4	5.2	9.7	46.8	49.7	36.3%
Vertical Tube						
ASM International	0	0	0	0	1.0	
BTU International	0	0	0	0	0	
Denko	0	0	0	0	0	
Disco	0	0	0	0	0	
Helmut Seier	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Kokusai Electric	0	0	0	10.8	15.0	
Semitherm	0	0	0	0	0	
Silicon Valley Group	0	0	0.3	0.4	1.0	
Tokyo Electron Ltd.	0	0	0	0	0	
Ulvac/BTU	0	0	0	0	0	
Varian/TEL	0	0	0	0	0	
Total Vertical	0	0	0.3	11.2	17.0	NA
Total Rest of World	14.4	5.2	10.0	58.0	66.7	46.7%

NA = Not applicable
Source: Dataquest (June 1990), Ref: DIFFSHR

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Table 46

Diffusion Furnace Company Shares Worldwide (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Diffusion Market	207.2	155.6	145.4	294.9	327.4	12.1%
Horizontal Tube						
ASM International	17.9	16.6	18.5	22.7	22.0	
BTU International	36.2	24.0	19.3	34.0	41.0	
Denko	0.6	0.6	0.8	0.9	0	
Gasonics	5.3	6.1	7.5	9.0	8.0	
GSTC (Tempress)	6.0	2.0	0.5	4.3	5.0	
Kokusai Electric	16.8	12.0	16.7	19.2	17.4	
Koyo Lindberg	9.7	6.0	2.6	3.3	5.0	
Pacific Western	1.1	0.6	0	0	0	
Process Technology	0	0	0	0	0	
Silicon Valley Group (Thermco)	45.1	27.6	34.9	60.0	52.0	
Solitec	0	0.3	0	0	0.7	
Tokyo Electron Ltd.	60.0	49.0	22.9	74.6	73.0	
Tylan	4.0	2.5	2.0	2.5	1.0	
Ulvac/BTU	0.5	0.4	1.7	9.2	10.0	
Varian/TEL	0	0	0	0	0.7	
Others	1.6	1.7	2.5	3.5	1.5	
Total Horizontal	204.8	149.4	129.9	243.2	237.3	3.8%
Vertical Tube						
ASM International	0	0	0	0	7.0	
BTU International	0	0	0	1.0	0	
Denko	0.4	1.2	1.2	1.8	4.0	
Disco	0.3	0.7	1.5	2.9	3.6	
Helmut Seier	0.6	0.5	0.5	0.7	0	
Koyo Lindberg	0.6	1.8	3.1	3.5	3.1	
Kokusai Electric	0.5	1.8	7.3	27.0	39.4	
Semitherm	0	0	0	0.5	3.0	
Silicon Valley Group	0	0.2	1.1	4.0	5.0	
Tokyo Electron Ltd.	0	0	0.8	8.0	16.9	
Ulvac/BTU	0	0	0	2.3	2.3	
Varian/TEL	0	0	0	0	[illegible]	
Total Vertical	2.4	6.2	15.5	51.7	90..	147.5%
Total Worldwide	207.2	155.6	145.4	294.9	327.4	12.1%

Source: Dataquest (June 1990), Ref: DIFFSHR

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Table 47

Rapid Thermal Processing Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World RTP Market	14.3	15.1	18.2	22.3	28.1	18.4%
United States						
AG Associates	4.5	5.4	5.9	6.0	6.0	
Dainippon Screen	0	0	0	0	0	
Eaton	0.7	0.2	0.2	0.2	0	
Kokusai	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Nanosil	0	0	0.3	0.3	0.4	
Peak Systems	0	0.7	2.7	4.2	3.0	
Process Products	0.5	0.5	0.6	0.8	1.0	
Sitesa Addax (AET)	0	0	0.2	0	0	
TEL/Thermco	0	0	0	0	0	
Ushio	0	0	0	0	0	
Varian	0.1	0.2	0.2	0.2	0	
Total United States	5.8	7.0	10.1	11.7	10.4	15.7%
Japan						
AG Associates	2.4	1.6	1.9	2.0	2.0	
Dainippon Screen	1.9	1.8	1.0	1.2	1.8	
Eaton	0	0.2	0	0.2	0	
Kokusai	0.1	0	0	0	0	
Koyo Lindberg	0.1	0.3	0.2	0.6	0.6	
Nanosil	0	0	0	0	0	
Peak Systems	0	0	0.7	2.0	2.5	
Process Products	0	0	0	0	0.1	
Sitesa Addax (AET)	0	0	0	0	0	
TEL/Thermco	0.4	0.4	0	0	0	
Ushio	0.3	0	0	0	3.0	
Varian	0.2	0.2	0.7	0.2	0	
Total Japan	5.4	4.5	4.5	6.2	10.0	16.7%

(Continued)

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Table 47 (Continued)

Rapid Thermal Processing Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World RTP Market	14.3	15.1	18.2	22.3	28.1	18.4%
Europe						
AG Associates	1.2	1.6	2.1	1.6	1.5	
Dainippon Screen	0	0	0	0	0	
Eaton	0.5	0.3	0	0	0	
Kokusai	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Nanosil	0	0	0	0	0	
Peak Systems	0	0	0	0.2	1.0	
Process Products	0	0	0.1	0.2	0.1	
Sitesa Addax (AET)	0.4	0.7	0.5	1.2	1.5	
TEL/Thermco	0	0	0	0	0	
Ushio	0	0	0	0	0	
Varian	0.1	0	0	0	0	
Total Europe	2.2	2.6	2.7	3.2	4.1	16.8%
Rest of World						
AG Associates	0.7	1.0	0.9	1.0	1.5	
Dainippon Screen	0	0	0	0	0	
Eaton	0.2	0	0	0	0	
Kokusai	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Nanosil	0	0	0	0	0	
Peak Systems	0	0	0	0.2	2.0	
Process Products	0	0	0	0	0.1	
Sitesa Addax (AET)	0	0	0	0	0	
TEL/Thermco	0	0	0	0	0	
Ushio	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Rest of World	0.9	1.0	0.9	1.2	3.6	41.4%

(Continued)

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Table 47 (Continued)

Rapid Thermal Processing Company Shares
Regional
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World RTP Market	14.3	15.1	18.2	22.3	28.1	18.4%
Worldwide						
AG Associates	8.8	9.6	10.8	10.6	11.0	
Dainippon Screen	1.9	1.8	1.0	1.2	1.8	
Eaton	1.4	0.7	0.2	0.4	0	
Kokusai	0.1	0	0	0	0	
Koyo Lindberg	0.1	0.3	0.2	0.6	0.6	
Nanosil	0	0	0.3	0.3	0.4	
Peak Systems	0	0.7	3.4	6.6	8.5	
Process Products	0.5	0.5	0.7	1.0	1.3	
Sitesa Addax (AET)	0.4	0.7	0.7	1.2	1.5	
TEL/Thermco	0.4	0.4	0	0	0	
Ushio	0.3	0	0	0	3.0	
Varian	0.4	0.4	0.9	0.4	0	
Total Worldwide	14.3	15.1	18.2	22.3	28.1	18.4%

Source: Dataquest (June 1990), Ref: RTPSHR

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Table 48

Ion Implantation Company Shares
United States
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Implanter Market	293.4	118.8	185.9	377.4	468.4	12.4%
Medium Current						
Balzers	0	0	0	0	0	
Eaton	14.8	6.6	4.0	10.0	9.0	
Hitachi	0	0	0	0	0	
Nissin	0	0	0	1.2	2.2	
Sumitomo/Eaton Nova	0	0	0	0	0	
TEL/Varian	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	19.1	9.2	5.9	6.2	13.2	
Veeco	2.0	0	0	0	0	
Total Medium Current	35.9	15.8	9.9	17.4	24.4	(9.2%)
High Current						
Applied Materials	0	0	4.0	9.1	18.4	
Balzers	0	0	0	0	0	
Eaton	35.1	8.8	17.0	27.0	19.0	
Hitachi	0	0	0	0	0	
Nissin	0	0	0	0	3.9	
Sumitomo/Eaton Nova	0	0	0	0	0	
TEL/Varian	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	4.2	4.0	6.6	8.4	19.8	
Veeco	3.0	0	0	0	0	
Total High Current	42.3	12.8	27.6	44.5	61.1	9.6%
High Voltage						
Eaton	0	2.0	4.5	0	0	
Genus (General Ionex)	0	0	0	3.2	3.4	
HVE Europa	0	0	0	0	0	
National Electrostatics	0.9	2.5	1.8	1.2	4.0	
Nissin	0	0	0	0	0	
Sumitomo Eaton Nova	0	0	0	0	0	
Varian	0	3.9	1.8	1.8	0	
Veeco	0	0	0	0	0	
Total High Voltage	0.9	8.4	8.1	6.2	7.4	69.3%
Total United States	79.1	37.0	45.6	68.1	92.9	4.1%

Source: Dataquest (June 1990), Ref: IMPLSHR

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Table 49

Ion Implantation Company Shares
Japan
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Implanter Market	293.4	118.8	185.9	377.4	468.4	12.4%
Medium Current						
Balzers	0	0	0	0	0	
Eaton	0	0	0	0	0	
Hitachi	0	0	0	0	0	
Nissin	19.3	10.2	11.1	26.2	33.8	
Sumitomo/Eaton Nova	1.1	1.5	2.6	2.9	0.9	
TEL/Varian	26.4	5.2	8.4	24.1	28.0	
Ulvac	6.3	4.8	5.2	7.5	13.8	
Varian	1.8	0.7	2.3	3.4	0	
Veeco	0	0	0	0	0	
Total Medium Current	54.9	22.4	29.6	64.1	76.5	8.6%
High Current						
Applied Materials	0	2.2	2.0	8.6	16.5	
Balzers	0	0	0	0	0	
Eaton	0	0	0	0	0	
Hitachi	4.2	3.2	3.8	9.6	14.4	
Nissin	2.2	1.6	1.8	4.1	9.7	
Sumitomo/Eaton Nova	23.8	3.9	18.4	42.8	47.5	
TEL/Varian	10.5	5.0	16.8	52.5	72.0	
Ulvac	2.1	0.9	2.1	3.8	0	
Varian	39.9	0	1.4	18.0	0	
Veeco	3.0	0	0	0	0	
Total High Current	85.7	16.8	46.3	139.4	160.1	16.9%
High Voltage						
Eaton	0	0	0	0	0	
Genus (General Ionex)	0	0	0	8.1	11.3	
HVE Europa	0	0	0	0	0	
National Electrostatics	0	1.1	0	0	0	
Nissin	0	0	2.8	0	2.9	
Sumitomo/Eaton Nova	0	0	3.1	0	0	
Varian	0	0	0	0	0	
Veeco	0	0	0	0	0	
Total High Voltage	0	1.1	5.9	8.1	14.2	NA
Total Japan	140.6	40.3	81.8	211.6	250.8	15.6%

NA = Not applicable
Source: Dataquest (June 1990), Ref: IMPLSHR

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Table 50

Ion Implantation Company Shares
Europe
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Implanter Market	293.4	118.8	185.9	377.4	468.4	12.4%
Medium Current						
Balzers	0	0	1.4	2.1	0.8	
Eaton	6.0	3.5	7.0	11.0	4.5	
Hitachi	0	0	0	0	0	
Nissin	0	0	0	0.9	0	
Sumitomo/Eaton Nova	0	0	0	0	0	
TEL/Varian	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	16.6	6.9	6.7	3.9	4.4	
Veeco	0	0	0	0	0	
Total Medium Current	22.6	10.4	15.1	17.9	9.7	(19.1%)
High Current						
Applied Materials	0	2.2	4.0	7.2	14.5	
Balzers	0	0	0	0	0	
Eaton	16.1	11.8	12.0	23.0	11.1	
Hitachi	0	0	0	0	0	
Nissin	0	0	0	0	1.9	
Sumitomo/Eaton Nova	0	0	0	0	0	
TEL/Varian	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	4.2	3.0	5.5	2.4	3.6	
Veeco	1.0	0	0	0	0	
Total High Current	21.3	17.0	21.5	32.6	31.1	9.9%
High Voltage						
Eaton	0	0	2.2	2.5	0	
Genus (General Ionex)	0	0	0	1.6	0	
HVE Europa	0	0	0	0	0	
National Electrostatics	1.2	0.3	0	0	0	
Nissin	0	0	0	0	0	
Sumitomo/Eaton Nova	0	0	0	0	0	
Varian	0	0	1.8	0	0	
Veeco	0	0	0	0	0	
Total High Voltage	1.2	0.3	4.0	4.1	0	(100.0%)
Total Europe	45.1	27.7	40.6	54.6	40.8	(2.5%)

Source: Dataquest (June 1990), Ref: IMPLSHR

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Table 51

Ion Implantation Company Shares
Rest of World
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Implanter Market	293.4	118.8	185.9	377 4	468.4	12.4%
Medium Current						
Balzers	0	0	1.4	2.1	0.8	
Eaton	0.6	1.9	2.0	7.0	17.1	
Hitachi	0	0	0	0	0	
Nissin	0	0	0	0	0	
Sumitomo/Eaton Nova	0	0	0	0	0	
TEL/Varian	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	10.5	4.0	3.0	9.4	11.0	
Veeco	0	0	0	0	0	
Total Medium Current	11.1	5.9	6.4	18.5	28.9	27.0%
High Current						
Applied Materials	0	0	0	0	0	
Balzers	0	0	0	0	0	
Eaton	12.3	5.9	6.0	9.0	31.7	
Hitachi	0	0	0	0	0	
Nissin	0	0	0	0	0	
Sumitomo/Eaton Nova	0	0	0	0	0	
TEL/Varian	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	5.2	2.0	5.5	15.6	21.6	
Veeco	0	0	0	0	0	
Total High Current	17.5	7.9	11.5	24.6	53.3	32.1%
High Voltage						
Eaton	0	0	0	0	0	
Genus (General Ionex)	0	0	0	0	1.7	
HVE Europa	0	0	0	0	0	
National Electrostatics	0	0	0	0	0	
Nissin	0	0	0	0	0	
Sumitomo/Eaton Nova	0	0	0	0	0	
Varian	0	0	0	0	0	
Veeco	0	0	0	0	0	
Total High Voltage	0	0	0	0	1.7	NA
Total Rest of World	28.6	13.8	17.9	43.1	83.9	30.9%

NA = Not applicable
Source: Dataquest (June 1990), Ref: IMPLSHR

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Table 52

Ion Implantation Company Shares Worldwide (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World Implanter Market	293.4	118.8	185.9	377.4	468.4	12.4%
Medium Current						
Balzers	0	0	2.8	4.2	1.6	
Eaton	21.4	12.0	13.0	28.0	30.6	
Hitachi	0	0	0	0	0	
Nissin	19.3	10.2	11.1	28.3	36.0	
Sumitomo/Eaton Nova	1.1	1.5	2.6	2.9	0.9	
TEL/Varian	26.4	5.2	8.4	24.1	28.0	
Ulvac	6.3	4.8	5.2	7.5	13.8	
Varian	48.0	20.8	17.9	22.9	28.6	
Veeco	2.0	0	0	0	0	
Total Medium Current	124.5	54.5	61.0	117.9	139.5	2.9%
High Current						
Applied Materials	0	4.4	10.0	24.9	49.4	
Balzers	0	0	0	0	0	
Eaton	63.5	26.5	35.0	59.0	61.8	
Hitachi	4.2	3.2	3.8	9.6	14.4	
Nissin	2.2	1.6	1.8	4.1	15.5	
Sumitomo/Eaton Nova	23.8	3.9	18.4	42.8	47.5	
TEL/Varian	10.5	5.0	16.8	52.5	72.0	
Ulvac	2.1	0.9	2.1	3.8	0	
Varian	53.5	9.0	19.0	44.4	45.0	
Veeco	7.0	0	0	0	0	
Total High Current	166.8	54.5	106.9	241.1	305.6	16.3%
High Voltage						
Eaton	0	2.0	6.7	2.5	0	
Genus (General Ionex)	0	0	0	12.9	16.4	
HVE Europa	0	0	0	0	0	
National Electrostatics	2.1	3.9	1.8	1.2	4.0	
Nissin	0	0	2.8	0	2.9	
Sumitomo/Eaton Nova	0	0	3.1	0	0	
Varian	0	3.9	3.6	1.8	0	
Veeco	0	0	0	0	0	
Total High Voltage	2.1	9.8	18.0	18.4	23.3	82.5%
Total Worldwide	293.4	118.8	185.9	377.4	468.4	12.4%

Source: Dataquest (June 1990), Ref: IMPLSHR

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Table 53

Optical CD/Wafer Inspection Company Shares
United States
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CD/Wafer Inspection Market	54.5	70.8	100.0	179.9	187.3	36.2%
Optical Critical Dimension						
Hitachi	0	0	0	0	0.3	
IVS, Inc.	0	0.5	1.4	6.4	5.2	
KLA Instruments	0	0	0	2.8	3.8	
Micro-Controle	0	0	0	0	0	
Nanometrics	1.2	0.9	1.1	1.4	1.0	
Nanoquest (Vickers Instruments)	0	0	4.9	7.0	5.8	
Nidek	0	0	0	0	0	
Nikon	0.3	0.2	0.3	0.5	0	
Optical Specialties	2.3	1.8	1.1	1.0	1.8	
Perkin-Elmer	0	0	0	2.3	1.4	
Reichert-McBain	0	2.7	0.3	0	0	
Ryokosha	0.1	0.1	0	0.3	0	
SiSCAN Systems	0	1.7	2.3	4.9	6.3	
Wild Leitz	1.7	1.5	2.3	3.3	3.0	
Wild Leitz Instruments	0	0	0.7	1.7	1.4	
Other CD Companies	2.2	1.9	1.5	1.8	1.4	
Total Optical CD	7.8	11.3	15.9	33.4	31.4	41.6%
Wafer Inspection						
Canon	0	0	0	0	0	
Estek (Aeronca)	0.3	0.2	0.1	0.2	0	
Insystems	0	0	1.1	6.4	7.1	
KLA Instruments	0	0	0	7.4	7.5	
Micro-Controle	0	0	0	0	0	
Nidek	0	0	0	0	0.2	
Nikon	1.4	1.6	2.9	3.4	4.4	
Olympus	0	0	0	0	0	
Optical Specialties	3.1	2.2	1.5	1.3	1.3	
Karl Suss	0	0	0	0	0	
Wild Leitz	1.6	1.3	2.2	5.0	1.5	
Zeiss	0	1.0	0.6	0.9	0.9	
Other Waf. Insp. Cos.	1.4	1.2	1.1	1.2	1.0	
Total Wafer Inspect.	7.8	7.5	9.5	25.8	23.9	32.3%

(Continued)

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Table 53 (Continued)

Optical CD/Wafer Inspection Company Shares
United States
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CD/Wafer Inspection Market	54.5	70.8	100.0	179.9	187.3	36.2%
Joint CD/Inspection						
KLA Instruments	6.3	8.8	11.6	9.4	15.9	
Optical Specialties	2.0	1.7	2.1	0.5	0	
Total Joint CD/Insp.	8.3	10.5	13.7	9.9	15.9	17.6%
Total US CD/Insp.	23.9	29.3	39.1	69.1	71.2	

Source: Dataquest (June 1990), Ref: INSPSHR

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Table 54

Optical CD/Wafer Inspection Company Shares
Japan
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CD/Wafer Inspection Market	54.5	70.8	100.0	179.9	187.3	36.2%
Optical Critical Dimension						
Hitachi	0	4.1	6.0	7.1	6.3	
IVS, Inc.	0	0	0	0	0	
KLA Instruments	0	0	0	1.5	1.1	
Micro-Controle	0	0	0	0	0	
Nanometrics	0.5	0.3	0.1	0.4	0.3	
Nanoquest (Vickers Instruments)	0	0	0.8	0	0.3	
Nidek	0	0	0	0.5	0.3	
Nikon	2.5	1.7	4.5	12.9	7.0	
Optical Specialties	0.3	0.2	0	0.7	0.6	
Perkin-Elmer	0	0	0	0.2	0	
Reichert-McBain	0	0	0	0	0	
Ryokosha	1.3	1.4	1.4	1.7	1.4	
SiSCAN Systems	0	0.2	0.2	0	0.4	
Wild Leitz	0.4	0.3	0.5	0.2	0	
Wild Leitz Instruments	0	0	0	0.4	0	
Other CD Companies	1.7	2.3	1.5	2.0	1.6	
Total Optical CD	6.7	10.5	15.0	27.6	19.3	30.3%
Wafer Inspection						
Canon	1.3	1.4	2.0	3.0	3.5	
Estek (Aeronca)	0	0	0	0	0	
Insystems	0	0	1.1	3.4	4.2	
KLA Instruments	0	0	0	8.6	7.1	
Micro-Controle	0	0	0	0	0	
Nidek	1.7	2.2	2.3	5.0	4.5	
Nikon	3.0	4.1	4.4	8.8	10.0	
Olympus	0	0	0	0	0	
Optical Specialties	0.4	0.3	0	0	0	
Karl Suss	0	0	0	0	0	
Wild Leitz	0.1	0.2	0	0	0	
Zeiss	0	0	0	0	0	
Other Waf. Insp. Cos.	0.4	0.4	0.5	0.7	0.7	
Total Wafer Inspect.	7.2	8.6	10.3	29.5	30.0	42.9%

(Continued)

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Table 54 (Continued)

Optical CD/Wafer Inspection Company Shares
Japan
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CD/Wafer Inspection Market	54.5	70.8	100.0	179.9	187.3	36.2%
Joint CD/Inspection						
KLA Instruments	3.5	6.9	11.5	9.8	12.9	
Optical Specialties	0.3	0.3	0	0	0	
Total Joint CD/Insp.	3.8	7.2	11.5	9.8	12.9	35.7%
Total Japan CD/Insp.	17.7	26.3	36.8	66.9	62.2	

Source: Dataquest (June 1990), Ref: INSPSHR

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Table 55

Optical CD/Wafer Inspection Company Shares
Europe
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CD/Wafer Inspection Market	54.5	70.8	100.0	179.9	187.3	36.2%
Optical Critical Dimension						
Hitachi	0	0	0	0	0	
IVS, Inc.	0	0	0.1	0	0	
KLA Instruments	0	0	0	1.9	0	
Micro-Controle	0	0	0	0	2.2	
Nanometrics	0.2	0.2	0.3	0.1	0.1	
Nanoquest (Vickers Instruments)	0	0	2.6	2.0	2.2	
Nidek	0	0	0	0	0	
Nikon	0.1	0.2	0.2	0.3	0.5	
Optical Specialties	0.3	0.2	0.1	0.2	0.3	
Perkin-Elmer	0	0	0	0.2	0	
Reichert-McBain	0	0.3	0	0	0	
Ryokosha	0	0	0	0.3	0	
SiSCAN Systems	0	0	0.5	0	0	
Wild Leitz	1.8	2.5	2.8	5.7	4.0	
Wild Leitz Instruments	0	0	0.9	1.4	0.6	
Other CD Companies	1.0	0.7	0.5	0.7	0.8	
Total Optical CD	3.4	4.1	8.0	12.8	10.7	33.2%
Wafer Inspection						
Canon	0	0	0	0	0	
Estek (Aeronca)	0	0	0	0	0	
Insystems	0	0	0	0	3.0	
KLA Instruments	0	0	0	1.1	2.2	
Micro-Controle	0	0	0	0	3.1	
Nidek	0	0	0	0.4	0.3	
Nikon	0	0	1.1	2.0	2.5	
Olympus	0	0	0	0	0	
Optical Specialties	0.4	0.3	0.1	0	0	
Karl Suss	0	0	0	0	0	
Wild Leitz	2.1	1.7	2.1	4.5	4.8	
Zeiss	0.9	1.4	1.2	0.9	0.9	
Other Waf. Insp. Cos.	0.6	0.4	0.3	0.1	0.1	
Total Wafer Inspect.	4.0	3.8	4.8	9.0	16.9	43.4%

(Continued)

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Table 55 (Continued)

Optical CD/Wafer Inspection Company Shares
Europe
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CD/Wafer Inspection Market	54.5	70.8	100.0	179.9	187.3	36.2%
Joint CD/Inspection						
KLA Instruments	1.4	2.4	3.6	3.7	4.8	
Optical Specialties	0.2	0.2	0.1	0.2	0	
Total Joint CD/Insp.	1.6	2.6	3.7	3.9	4.8	31.6%
Total Europe CD/Insp.	9.0	10.5	16.5	25.7	32.4	

Source: Dataquest (June 1990), Ref: INSPSHR

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Table 56

Optical CD/Wafer Inspection Company Shares
Rest of World
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CD/Wafer Inspection Market	54.5	70.8	100.0	179.9	187.3	36.2%
Optical Critical Dimension						
Hitachi	0	0	0	0	0	
IVS, Inc.	0	0	0	0	2.0	
KLA Instruments	0	0	0	0	1.6	
Micro-Controle	0	0	0	0	0	
Nanometrics	0.4	0.1	0.2	0.4	0.4	
Nanoquest (Vickers Instruments)	0	0	0	0	0.6	
Nidek	0	0	0	0	0	
Nikon	0.1	0.2	0.2	0.6	0.5	
Optical Specialties	0.2	0	0.1	0.4	2.0	
Perkin-Elmer	0	0	0	0.2	0	
Reichert-McBain	0	0	0	0	0	
Ryokosha	0	0	0	0.2	0	
SiSCAN Systems	0	0	0	0	0	
Wild Leitz	0.5	0.5	0.8	0.6	0.8	
Wild Leitz Instruments	0	0	0	0	0	
Other CD Companies	1.0	2.0	2.1	3.2	2.7	
Total Optical CD	2.2	2.8	3.4	5.6	10.6	48.2%
Wafer Inspection						
Canon	0	0	0	0	0	
Estek (Aeronca)	0	0	0	0	0	
Insystems	0	0	0	0	0	
KLA Instruments	0	0	0	4.3	2.4	
Micro-Controle	0	0	0	0	0	
Nidek	0	0	0.8	0.8	0.3	
Nikon	0	0.7	1.1	1.6	2.2	
Olympus	0	0	0	0	0	
Optical Specialties	0.3	0	0.1	0	0.7	
Karl Suss	0	0	0	0	0	
Wild Leitz	0.6	0.3	0.4	0.9	0.6	
Zeiss	0	0	0	0	0	
Other Waf. Insp. Cos.	0.6	0.9	0.8	0.8	0.4	
Total Wafer Inspect.	1.5	1.9	3.2	8.4	6.6	44.8%

(Continued)

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Table 56 (Continued)

Optical CD/Wafer Inspection Company Shares
Rest of World
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CD/Wafer Inspection Market	54.5	70.8	100.0	179.9	187.3	36.2%
Joint CD/Inspection						
KLA Instruments	0	0	0.9	3.7	4.3	
Optical Specialties	0.2	0	0.1	0.5	0	
Total Joint CD/Insp.	0.2	0	1.0	4.2	4.3	115.3%
Total ROW CD/Insp.	3.9	4.7	7.6	18.2	21.5	

Source: Dataquest (June 1990), Ref: INSPSHR

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Table 57

Optical CD/Wafer Inspection Company Shares Worldwide (Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CD/Wafer Inspection Market	54.5	70.8	100.0	179.9	187.3	36.2%
Optical Critical Dimension						
Hitachi	0	4.1	6.0	7.1	6.6	
IVS, Inc.	0	0.5	1.5	6.4	7.2	
KLA Instruments	0	0	0	6.2	6.5	
Micro-Controle	0	0	0	0	2.2	
Nanometrics	2.3	1.5	1.7	2.3	1.8	
Nanoquest (Vickers Instruments)	0	0	8.3	9.0	8.9	
Nidek	0	0	0	0.5	0.3	
Nikon	3.0	2.3	5.2	14.3	8.0	
Optical Specialties	3.1	2.2	1.3	2.3	4.7	
Perkin-Elmer	0	0	0	2.9	1.4	
Reichert-McBain	0	3.0	0.3	0	0	
Ryokosha	1.4	1.5	1.4	2.5	1.4	
SiSCAN Systems	0	1.9	3.0	4.9	6.7	
Wild Leitz	4.4	4.8	6.4	9.8	7.8	
Wild Leitz Instruments	0	0	1.6	3.5	2.0	
Other CD Companies	5.9	6.9	5.6	7.7	6.5	
Total Optical CD	20.1	28.7	42.3	79.4	72.0	37.6%
Wafer Inspection						
Canon	1.3	1.4	2.0	3.0	3.5	
Estek (Aeronca)	0.3	0.2	0.1	0.2	0	
Insystems	0	0	2.2	9.8	14.3	
KLA Instruments	0	0	0	21.4	19.2	
Micro-Controle	0	0	0	0	3.1	
Nidek	1.7	2.2	3.1	6.2	5.3	
Nikon	4.4	6.4	9.5	15.8	19.1	
Olympus	0	0	0	0	0	
Optical Specialties	4.2	2.8	1.7	1.3	2.0	
Karl Suss	0	0	0	0	0	
Wild Leitz	4.7	3.5	4.7	10.4	6.9	
Zeiss	0.9	2.4	1.8	1.8	1.8	
Other Waf. Insp. Cos.	3.0	2.9	2.7	2.8	2.2	
Total Wafer Inspect.	20.5	21.8	27.8	72.7	77.4	39.4%

(Continued)

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Table 57 (Continued)

Optical CD/Wafer Inspection Company Shares
Worldwide
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
World CD/Wafer Inspection Market	54.5	70.8	100.0	179.9	187.3	36.2%
Joint CD/Inspection						
KLA Instruments	11.2	18.1	27.6	26.6	37.9	
Optical Specialties	2.7	2.2	2.3	1.2	0	
Total Joint CD/Insp.	13.9	20.3	29.9	27.8	37.9	28.5%
Total WW CD/Insp.	54.5	70.8	100.0	179.9	187.3	

Source: Dataquest (June 1990), Ref: INSPSHR

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Wafer Fab Equipment—Company Rankings

This section of the wafer fab equipment database presents the ranking of wafer fab equipment manufacturers by 1989 revenue, as shown in Table 1. Line 1 in the table shows the total worldwide wafer fab equipment market. Individual company data shown in the table represent 85 percent of the 1989 total wafer fab equipment market of approximately $5,887 million. The companies listed here represent virtually all worldwide industry sales in the key front-end equipment categories of lithography, automatic photoresist processing, etch and clean, deposition, diffusion, ion implantation, and CD/wafer inspection. The remaining 15 percent of the total worldwide wafer fab equipment includes other process control, factory automation, and other front-end equipment. Company sales for these categories are not included in the table.

Table 1 includes only company sales of front-end equipment; it does not include company sales of assembly and test equipment. For instance, back-end equipment sales by General Signal or ASM International are not included. Likewise, KLA's CD/wafer inspection equipment sales only are included; KLA's sales of mask inspection equipment are not.

The revenue reported in Table 1 is for the calendar year and includes system sales, upgrades, and retrofits, but it does not include service and spare parts. Thus, the revenue reported here will differ from each company's sales as reported in its financial statements. In addition, all company revenue presented in Table 1 includes the revenue associated with any acquisitions that occurred during the 1985 through 1989 period. This has been done to reflect the historical strength of the combined organizations. For example, Silicon Valley Group acquired Anicon in 1987 and Thermco in 1988. The estimates for Silicon Valley Group in Table 1 incorporate the sales of Anicon and Thermco even prior to the acquisition of these organizations. Therefore, the historical revenue reported for Silicon Valley Group will differ from its public financial statements.

Finally, several companies are denoted as being involved in wafer fab equipment joint venture activities. The entries for these companies do not include the revenue of the joint ventures. Instead, the reader should refer to the individual entry for the joint venture equipment company. For example, the estimated revenue of the TEL/Varian or Varian/TEL joint ventures is listed separately from Tokyo Electron Ltd. and Varian.

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Table 1

Semiconductor Wafer Fab Equipment Companies Ranked by Worldwide Sales (Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
World Fab Equipment Market	3,355.6	2,709.9	3,135.0	4,937.1	5,886.8	
Nikon						1
Steppers	157.6	128.4	218.8	490.2	653.7	
Opt. CD/wafer inspection	7.4	8.7	14.7	30.1	27.1	
Total	165.0	137.1	233.5	520.3	680.8	
Applied Materials						2
Dry etch	69.6	74.0	102.0	196.7	208.0	
Silicon epitaxy	44.0	31.3	18.6	47.2	22.2	
APCVD	9.9	7.8	14.5	15.7	15.0	
PECVD	6.3	6.1	31.0	75.4	143.0	
LPCVD	0	0	0	0	0	
Ion implantation	0	4.4	10.0	24.9	49.4	
Total	129.8	123.6	176.1	359.9	437.6	
Tokyo Electron Limited						3
Resist processing equip.	24.5	25.6	36.2	90.5	99.3	
Diffusion	60.0	49.0	23.7	82.6	89.9	
LPCVD	16.0	7.6	8.3	18.4	20.7	
Dry etch	10.5	6.0	17.4	44.6	80.0	
Metalorganic CVD	2.3	3.0	2.9	1.7	2.9	
Rapid thermal processing	0.4	0.4	0	0	0	
Total	113.7	91.6	88.5	237.8	292.8	

Note: Tokyo Electron Limited data include former TEL/Lam and TEL/Thermco organizations. Wafer fab equipment joint venture activity: TEL/Varian, Varian/TEL (not included here; please refer to individual entries)

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Canon						4
Projection aligners	127.7	49.2	40.6	69.1	49.4	
Steppers	35.0	63.2	89.8	125.0	182.9	
Contact/proximity	30.3	15.4	11.0	8.6	6.3	
Resist processing equip.	0	0.5	1.0	3.8	10.1	
Opt. CD/wafer inspection	1.3	1.4	2.0	3.0	3.5	
Total	194.3	129.7	144.4	209.5	252.2	
Wafer fab equipment joint venture activity: Alcan (not included here; please refer to individual entry)						
General Signal						5
GCA						
Steppers	114.2	74.6	47.4	104.0	68.9	
Resist process. equip.	15.0	12.3	7.0	5.5	0	
Dry etch	0.8	2.0	4.0	5.0	0	
Total CGA	130.0	88.9	58.4	114.5	68.9	
Ultratech						
Steppers	50.7	38.9	40.6	73.0	62.3	
Drytek						
Dry etch	23.0	16.0	17.0	25.0	22.0	
Dry strip	3.0	2.0	1.0	1.2	1.4	
Total Drytek	26.0	18.0	18.0	26.2	23.4	
Semiconductor Systems Inc.						
Resist process. equip.	8.8	8.8	10.8	22.0	22.0	
General Signal Thinfilm						
Diffusion	6.0	2.0	0.5	4.3	5.0	
LPCVD	7.6	3.8	0	3.8	3.0	
APCVD	2.1	2.2	0	1.8	1.3	
Total GSTC	15.7	8.0	0.5	9.9	9.3	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
General Signal (Continued)						
Circuits Proc. Apparatus Sputtering	4.5	2.9	3.0	2.6	0	
Total General Signal	235.7	165.5	131.3	248.2	185.9	
Note: General Signal Thinfilm includes former Tempress organization.						
Hitachi						6
Direct write & maskmaking	11.0	11.2	22.1	13.4	16.0	
Steppers	17.9	8.2	33.3	49.2	75.5	
Dry etch	3.6	10.8	18.8	34.6	47.3	
Dry strip	0	0	0.7	4.6	5.0	
Ion implantation	4.2	3.2	3.8	9.6	14.4	
Opt. CD/wafer inspection	0	4.1	6.0	7.1	6.6	
APCVD	0.3	0.4	0	0.2	0.5	
Total	37.0	37.9	84.7	118.7	165.3	
Varian Associates						7
Sputtering	57.1	56.7	48.3	61.3	73.0	
Ion implantation	101.5	33.7	40.5	69.1	73.6	
Molecular beam epitaxy	7.2	10.8	12.1	17.5	17.2	
Dry etch	8.0	4.0	0	0	0	
LPCVD	0	1.1	7.5	5.5	0.7	
Rapid thermal processing	0.4	0.4	0.9	0.4	0	
Direct write & maskmaking	0	0	0	0	0	
Total	174.2	106.7	109.3	153.8	164.5	
Wafer fab equipment joint venture activity: TEL/Varian, Varian/TEL (not included here; please refer to individual entries)						
ASM Lithography						8
Steppers	2.8	5.1	36.7	58.6	131.8	
Direct write & maskmaking	1.9	6.0	12.0	9.6	9.6	
Total	4.7	15.1	48.7	68.2	141.4	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Anelva						9
Sputtering	30.8	21.8	44.7	53.8	81.0	
Dry etch	39.4	16.2	22.3	41.6	44.2	
Molecular beam epitaxy	6.3	7.2	9.7	11.5	7.2	
Evaporation	0.4	2.3	4.9	6.2	4.3	
LPCVD	0	0	0.7	2.3	1.5	
PECVD	0	0.6	1.0	0	0	
ECR CVD	0	0.6	1.0	0	1.4	
Total	76.9	48.7	84.3	115.4	139.6	
Silicon Valley Group						10
Resist processing equip.	30.5	25.6	33.0	37.4	54.0	
Diffusion	45.1	27.8	36.0	64.0	57.0	
LPCVD	24.7	15.4	12.3	14.1	16.0	
Total	100.3	68.8	81.3	115.5	127.0	
Note: Includes former Anicon and Thermco organizations						
Dainippon Screen						11
Resist processing equip.	34.9	29.8	31.2	40.2	67.7	
Wet process	15.9	20.6	21.7	37.8	47.2	
Rapid thermal processing	1.9	1.8	1.0	1.2	1.8	
Total	52.7	52.2	53.9	79.2	116.7	
Lam Research						12
Dry etch	34.0	26.0	32.0	65.0	85.6	
Silicon epitaxy	19.4	11.4	14.8	19.0	25.7	
Total	53.4	37.4	46.8	84.0	111.3	
Note: Includes former Gemini organization						

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Ulvac						13
Sputtering	22.6	25.4	34.0	48.7	55.7	
Evaporation	16.8	22.4	8.0	14.0	14.6	
Ion implantation	8.4	5.7	7.3	11.3	13.8	
Molecular beam epitaxy	3.4	4.4	4.3	7.5	4.0	
PECVD	2.9	3.0	2.8	2.6	1.0	
LPCVD	0	1.2	1.4	3.8	4.2	
Dry etch	4.7	3.9	5.7	8.3	8.7	
Dry strip	0	0	3.6	4.9	5.5	
Metalorganic CVD	1.9	2.3	1.9	2.2	2.0	
Total	60.7	68.3	69.0	103.3	109.5	
ASM International						14
Diffusion	17.9	16.6	18.5	22.7	29.0	
LPCVD	13.9	20.5	19.9	25.8	18.0	
PECVD	40.4	44.4	44.5	51.6	51.0	
Silicon epitaxy	0	0	0	3.1	6.2	
Total	72.2	81.5	82.9	103.2	104.2	
Eaton						15
Ion implantation	84.9	40.5	54.7	89.5	92.4	
Resist processing equip.	12.0	12.0	10.5	11.0	10.5	
Steppers	21.8	2.1	0	0	0	
Rapid thermal processing	1.4	0.7	0.2	0.4	0	
Total	120.1	55.3	65.4	100.9	102.9	
Wafer fab equipment joint venture activity: Sumitomo/Eaton Nova (not included here; please refer to individual entry)						
TEL/Varian						16
Ion implantation	36.9	10.2	25.2	76.6	100.0	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Kokusai Electric						17
LPCVD	14.6	17.6	10.4	30.8	34.7	
Diffusion	17.3	13.8	24.0	46.2	56.8	
Dry etch	10.4	3.3	1.4	1.5	1.0	
Silicon epitaxy	5.0	2.1	1.5	4.2	5.7	
APCVD	0.7	0.7	0	0	0	
Rapid thermal processing	0.1	0	0	0	0	
Total	48.1	37.5	37.3	82.7	98.2	
Perkin-Elmer						18
Projection aligners	138.4	121.8	88.0	78.6	44.9	
Direct write & maskmaking	64.8	42.4	36.6	39.8	27.6	
Steppers	22.2	27.0	25.2	5.0	12.0	
Dry etch	19.5	9.2	0	0	0	
Molecular beam epitaxy	6.0	7.2	5.0	2.8	0	
Sputtering	9.9	5.6	3.1	0.9	1.0	
Opt. CD/wafer inspection	0	0	0	2.9	1.4	
X-Ray	0	0	0	0	2.0	
Total	260.8	213.2	157.9	130.0	88.9	
Genus						19
LPCVD	17.5	7.5	13.2	33.4	62.0	
Ion implantation	0	0	0	12.9	16.4	
Total	17.5	7.5	13.2	46.3	78.4	
KLA Instruments						20
Opt. CD/wafer inspection	11.2	18.1	27.6	54.2	63.6	
Materials Research Corp.						21
Sputtering	37.8	21.9	23.1	34.0	54.0	
Dry etch	4.8	4.1	4.4	13.0	7.4	
Total	42.6	26.0	27.5	47.0	61.4	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
BTU International						22
Diffusion	36.2	24.0	19.3	35.0	41.0	
LPCVD	6.7	5.6	7.9	14.5	17.5	
Total	42.9	29.6	27.2	49.5	58.5	
Wafer fab equipment joint venture activity: BTU/Ulvac, Ulvac/BTU (not included here; please refer to individual entries)						
Nissin High Voltage						23
Ion implantation	21.5	11.8	15.7	32.4	54.4	
Watkins-Johnson						24
APCVD	5.9	8.1	16.0	36.0	49.0	
Sumitomo/Eaton Nova						25
Ion implantation	24.9	5.4	24.1	45.7	48.4	
Tokyo Ohka						26
Dry etch	7.6	7.2	7.1	10.0	21.7	
Dry strip	8.9	5.2	9.2	19.9	26.0	
Total	16.5	12.4	16.3	29.9	47.7	
JEOL						27
Direct write & maskmaking	22.4	41.7	48.9	36.1	47.4	
Novellus						28
PECVD	0	0	3.6	23.7	47.0	
E.T. Electrotech						29
PECVD	13.6	15.2	13.3	20.3	15.5	
Dry etch	8.9	5.0	7.2	14.1	15.0	
Sputtering	8.7	5.3	6.0	9.0	16.1	
Dry strip	1.0	0	0	0	0	
Total	32.2	25.5	26.5	43.4	46.6	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Tegal						30
Dry etch	25.0	25.6	35.6	55.0	42.0	
Dry strip	3.0	2.0	2.4	2.0	2.5	
Total	28.0	27.6	38.0	57.0	44.5	
FSI International						31
Wet process	28.4	22.4	19.2	24.1	37.3	
Varian/TEL						32
Resist processing equip.	0	0	0	0	19.4	
Dry etch	0	0	0	0	6.0	
LPCVD	0	0	0	0	3.0	
Diffusion	0	0	0	0	6.5	
Total	0	0	0	0	34.9	
Sankyo Engineering						33
Wet process	5.3	7.4	8.1	23.8	27.4	
Kaijo Denki						34
Wet process	10.0	13.5	10.1	14.6	27.3	
ISA Riber						35
Molecular beam epitaxy	14.4	13.6	19.3	22.5	22.3	
Semitool and Semitherm						36
Wet process	16.9	15.9	18.8	15.4	18.0	
LPCVD	0	0	0	0.5	1.2	
Diffusion	0	0	0	0.5	3.0	
Total	16.9	15.9	18.8	16.4	22.2	
Ateq						37
Maskmaking lithography	0	0	1.6	11.2	20.4	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Plasma Systems						38
Dry strip	3.2	3.3	5.4	10.4	17.0	
Dry etch	1.5	1.7	1.9	3.2	3.3	
Total	4.7	5.0	7.3	13.6	20.3	
Branson IPC						39
Dry strip	14.3	10.2	7.8	15.0	16.0	
Dry etch	4.9	4.2	1.6	0	3.2	
Total	19.2	14.4	9.4	15.0	19.2	
Plasma-Therm						40
Dry etch	13.0	11.0	13.7	12.9	15.2	
Dry strip	0	0	0	0	1.0	
PECVD	5.6	5.8	4.6	6.0	3.0	
Total	18.6	16.8	18.3	18.9	19.2	
Amaya						41
APCVD	10.9	6.0	5.5	17.5	19.0	
VG Instruments						42
Molecular beam epitaxy	13.5	19.4	15.0	16.5	19.0	
Sumitomo Metal						43
Dry etch	0	2.4	5.6	6.2	12.0	
ECR CVD	0	0	0	0	6.0	
Total	0	2.4	5.6	6.2	18.0	
Enya Seisakusho						44
Wet process	8.8	9.6	6.2	7.6	11.6	
PECVD	4.2	1.6	1.9	4.2	3.5	
LPCVD	1.3	1.0	0.6	1.8	1.7	
Total	14.3	12.2	8.7	13.6	16.8	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Karl Suss						45
Contact/proximity	17.5	16.0	13.6	13.7	13.9	
X-Ray	1.0	0	0	4.6	2.8	
Total	18.5	16.0	13.6	18.3	16.7	
Wild Leitz and Wild Leitz Instruments						46
Opt. CD/wafer inspection	9.1	8.3	11.1	20.2	16.7	
Santa Clara Plastics						47
Wet process	26.0	20.0	16.0	14.6	16.6	
Ulvac/BTU						48
Diffusion	0.5	0.4	1.7	11.5	12.3	
LPCVD	0	0	0.5	3.5	4.0	
Total	0.5	0.4	2.2	15.0	16.3	
Tokuda						49
Dry etch	9.6	4.3	9.4	8.8	10.5	
Sputtering	5.0	3.3	11.1	7.0	5.6	
Total	14.6	7.6	20.5	15.8	16.1	
Balzers						50
Sputtering	10.1	13.2	13.9	11.0	8.2	
Evaporation	10.4	5.0	2.9	2.9	5.4	
Ion implantation	0	0	2.8	4.2	1.6	
Total	20.5	18.2	19.6	18.1	15.2	
Solitec						51
Resist processing equip.	5.0	6.5	6.2	7.5	9.0	
LPCVD	12.9	5.3	3.6	6.0	5.0	
Diffusion	0	0.3	0	0	0.7	
Total	17.9	12.1	9.8	13.5	14.7	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Cambridge Instruments						52
Direct write & maskmaking	11.9	14.5	10.0	13.0	14.5	
Metalorganic CVD	4.1	3.6	3.3	2.7	0	
Total	16.0	18.1	13.3	15.7	14.5	
Insystems						53
Opt. CD/wafer inspection	0	0	2.2	9.8	14.3	
Gasonics						54
Diffusion	5.3	6.1	7.5	9.0	8.0	
Dry strip	0	0.7	2.0	3.0	6.2	
Total	5.3	6.8	9.5	12.0	14.2	
CVC Products						55
Sputtering	9.5	13.5	9.7	12.3	12.0	
Evaporation	0	0	0	1.6	2.0	
Total	9.5	13.5	9.7	13.9	14.0	
Verteq						56
Wet process	5.9	8.3	7.7	12.9	13.9	
Note: Includes the former wet processing equipment operations of Estek						
Machine Technology Inc.						57
Resist processing equip.	17.8	12.9	12.7	10.0	11.3	
Dry strip	0.3	2.0	2.7	4.5	1.5	
Sputtering	0	0.9	3.0	5.0	1.0	
Total	18.1	15.8	18.4	19.5	13.8	
Leybold-Heraeus						58
Sputtering	8.8	9.6	15.0	10.8	11.8	
Evaporation	4.0	3.0	1.5	0.5	1.8	
Total	12.8	12.6	16.5	11.3	13.6	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Koyo Lindberg						59
Diffusion	10.3	7.8	5.7	6.8	8.1	
LPCVD	1.9	2.2	2.0	4.5	4.1	
Rapid thermal processing	0.1	0.3	0.2	0.6	0.6	
APCVD	0.6	0.4	0.2	1.3	0.6	
Total	12.9	10.7	8.1	13.2	13.4	
Toshiba Machine						60
Silicon epitaxy	2.3	1.0	0.6	2.0	1.3	
Direct write & maskmaking	0	3.0	3.5	7.7	7.2	
APCVD	0	4.3	5.0	6.0	4.2	
Total	2.3	8.3	9.1	15.7	12.7	
Sugai						61
Wet process	3.9	3.7	4.5	7.0	12.4	
Convac						62
Resist processing equip.	3.8	6.4	10.9	13.8	12.2	
Alcan Tech.						63
Dry strip	0	0.9	5.0	9.2	11.6	
S&K Products International						64
Wet process	6.6	6.9	8.5	9.4	11.6	
Temescal						65
Evaporation	10.2	10.5	9.9	8.7	11.2	
Sputtering	2.1	1.3	0	0	0	
Total	12.3	11.8	9.9	8.7	11.2	
AG Associates						66
Rapid thermal processing	8.8	9.6	10.8	10.6	1..3	
Ramco						67
Dry strip	1.7	4.5	8.7	9.6	11.0	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Aixtron						68
Metalorganic CVD	0.5	1.7	4.9	7.5	10.6	
Emcore						69
Metalorganic CVD	0.1	2.3	5.1	7.0	10.0	
Kuwano Electric						70
Wet process	2.7	3.9	6.3	13.6	9.6	
Tazmo						71
Resist processing equip.	1.1	2.5	4.6	5.7	9.3	
Shimada						72
Silicon epitaxy	0.8	0.5	0	0	0	
Wet process	0.6	0.6	3.9	5.5	9.2	
Metalorganic CVD	0	0.3	0	0	0	
Total	1.4	1.4	3.9	5.5	9.2	
Universal Plastics						73
Wet process	0.1	1.6	3.7	8.5	9.1	
Nanoquest						74
Opt. CD/wafer inspection	0	0	8.3	9.0	8.9	
Peak Systems						75
Rapid thermal processing	0	0.7	3.4	6.6	8.5	
Pokorny						76
Wet process	2.0	3.1	4.3	4.7	8.2	
SCI Manufacturing						77
Wet process	0	0	4.8	8.0	8.2	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
CHA Industries						78
Evaporation	7.1	5.6	6.0	6.3	7.0	
Sputtering	1.0	0.7	0.3	0.7	1.1	
Total	8.1	6.3	6.3	7.0	8.1	
Semifab						79
Wet process	4.8	6.4	7.7	7.0	7.6	
Denko						80
Diffusion	1.0	1.8	2.0	2.7	4.0	
LPCVD	1.3	2.7	2.1	2.3	3.5	
Total	2.3	4.5	4.1	5.0	7.5	
IVS Incorporated						81
Opt. CD/wafer inspection	0	0.5	1.5	6.4	7.2	
Japan Production Engineering						82
PECVD	5.9	6.0	4.5	6.5	7.0	
Matrix						83
Dry strip	0	2.1	5.2	7.2	7.0	
Nippon Sanso						84
Metalorganic CVD	3.6	4.6	4.9	6.3	6.8	
Optical Specialties						85
Opt. CD/wafer inspection	10.0	7.2	5.3	4.8	6.7	
SiScan Systems						86
Opt. CD/wafer inspection	0	1.9	3.0	4.9	6.7	
Dexon						87
Wet process	3.5	3.1	3.1	5.5	6.4	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Sitesa						88
Silicon epitaxy	0	0	0	4.5	4.9	
Rapid thermal processing	0.4	0.7	0.7	1.2	1.5	
Total	0.4	0.7	0.7	5.7	6.4	
Nidek						89
Opt. CD/wafer inspection	1.7	2.2	3.1	6.7	5.6	
Micro-Controle						90
Opt. CD/wafer inspection	0	0	0	0	5.3	
LPE						91
Silicon epitaxy	0	0	0	4.5	4.8	
Samco						92
Metalorganic CVD	0.7	0.7	0.6	1.0	0.6	
Dry etch	0	0	0	0	2.2	
Dry strip	0	0	0	0	1.0	
PECVD	0	0	0	0	1.0	
Total	0.7	0.7	0.6	1.0	4.8	
Poly-Flow Engineering						93
Wet process	0.8	0.5	0.5	0.2	4.4	
Process Technology Ltd.						94
LPCVD	5.7	5.4	4.3	4.0	4.1	
American Semiconductor Equipment Technologies						95
Steppers	8.1	11.6	11.3	16.0	4.0	
National Electrostatics						96
Ion implantation	2.1	3.9	1.8	1.2	4.0	
Disco						97
Diffusion	0.3	0.7	1.5	2.9	3.6	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Pacific Western Systems						98
PECVD	8.7	6.9	7.9	6.2	3.0	
APCVD	1.4	1.2	0.2	0	0	
LPCVD	0.4	0.5	0	0	0	
Diffusion	1.1	0.6	0	0	0	
Total	11.6	9.2	8.1	6.2	3.0	
Pure Aire Corporation						99
Wet process	1.8	1.8	2.4	2.8	3.0	
Ushio						100
Rapid thermal processing	0.3	0	0	0	3.0	
Eiko						101
Molecular beam epitaxy	1.0	1.2	1.4	1.2	2.9	
Spectrum CVD						102
LPCVD	0	0.5	2.3	1.4	2.6	
Innotec						103
Sputtering	2.6	1.8	2.4	4.2	1.9	
Evaporation	0.3	0.2	0	1.0	0.6	
Total	2.9	2.0	2.4	5.2	2.5	
Spire						104
Metalorganic CVD	3.0	3.3	1.3	2.1	2.4	
Nippon EMC						105
Metalorganic CVD	1.1	1.5	1.4	1.9	2.2	
Denton Vacuum						106
Sputtering	0.1	0.1	0.1	0.1	0.9	
Evaporation	0.1	0.2	0.2	0.2	1.2	
Total	0.2	0.3	0.3	0.3	2.1	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Athens						107
Wet process	0	0	1.0	4.0	2.0	
CPA						108
Sputtering	0.0	0.0	0.0	0.0	2.0	
Note: Formerly Circuits Processing Apparatus (General Signal)						
CVT						109
Metalorganic CVD	0.7	0.4	1.1	1.6	2.0	
MR Semicon						110
Metalorganic CVD	0	0	0	0	2.0	
Nanometrics						111
Opt. CD/wafer inspection	2.3	1.5	1.7	2.3	1.8	
Zeiss						112
Opt. CD/wafer inspection	0.9	2.4	1.8	1.8	1.8	
LFE						113
Dry strip	2.0	1.0	1.0	1.5	1.5	
Sputtered Films						114
Sputtering	1.0	1.6	1.0	0.6	1.5	
Tystar (Tylan)						115
Diffusion	4.0	2.5	2.0	2.5	1.0	
LPCVD	2.3	0.7	4.0	1.5	0.5	
Total	6.3	3.2	6.0	4.0	1.5	
CFM Technology						116
Wet process	0	0	0	1.0	1.4	
Chlorine Engineering						117
Dry strip	0	0	0	0	1.4	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Kurt J. Lesker						118
Sputtering	0.8	0.8	0.8	0.8	0.8	
Evaporation	0.5	0.3	0.3	0.3	0.6	
Total	1.3	1.1	1.1	1.1	1.4	
Ryokosha						119
Opt. CD/wafer inspection	1.4	1.5	1.4	2.5	1.4	
CVD Equipment						120
Metalorganic CVD	1.5	0.6	1.2	1.3	1.3	
Process Products						121
Rapid thermal processing	0.5	0.5	0.7	1.0	1.3	
Centrotherm						122
Diffusion	0.2	0.2	0.5	1.0	1.0	
Semco Engineering						123
Metalorganic CVD	0	0	0.3	0.9	1.0	
Rapro						124
Silicon epitaxy	0	0	0	0	0.9	
Ion Tech						125
Sputtering	0.8	0.7	0.7	0.5	0.8	
Wellman Furnaces						126
Diffusion	1.4	1.5	2.0	2.5	0.5	
LPCVD	0	0	0	0.5	0.2	
Total	1.4	1.5	2.0	3.0	0.7	
Hohkoh Sangyo						127
Dry strip	1.1	0.5	0.6	0	0.6	
Nanosil						128
Rapid thermal processing	0	0	0.3	0.3	0.4	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Elionix						129
Dry etch	0	0.2	0.3	0.3	0.3	
Advantage Production Tech.						—
Wet process	0	0	0	0	0	
Alamada Instruments						—
Wet process	0	0	0	0	0	
Chemitronics						—
Wet process	0	0	0	1.4	0	
Crystal Specialties						—
Metalorganic CVD	1.8	2.7	2.6	2.7	0	
Daiwa Semiconductor						—
Metalorganic CVD	0	0.4	0.4	0.5	0	
EEV						—
Metalorganic CVD	1.0	1.4	0.7	0	0	
Epitaxy Inc.						—
Silicon epitaxy	0	0	0	0	0	
Ergo Plasma Systems						—
Dry etch	0.8	0	0	0	0	
Estek						—
Opt. CD/wafer inspection	0.3	0.2	0.1	0.2	0	
Focus Semiconductor						—
LPCVD	0	0	1.0	2.5	0	
Hampshire Instruments						—
X-Ray	0	0	0	1.8	0	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1985	1986	1987	1988	1989	1989 Rank
Heidelberg Instruments						—
Opt. CD/wafer inspection	0	0	1.6	3.5	0	
Helmut Seier						—
Diffusion	0.6	0.5	0.5	0.7	0	
LPCVD	0.3	0	0.3	0.3	0	
Total	0.9	0.5	0.8	1.0	0	
Integrated Air Systems						—
Wet process	5.0	4.0	3.0	2.0	0	
Micronix						—
X-Ray	0.8	0.8	0	0	0	
Olympus						—
Opt. CD/wafer inspection	0	0	0	0	0	
Reichert-McBain						—
Opt. CD/wafer inspection	0	3.0	0.3	0	0	
Seiden						—
Metalorganic CVD	0.9	1.3	0.6	0.6	0	
Seiko						—
Molecular beam epitaxy	0.8	2.0	1.2	1.4	0	
Thomas Schwonn						—
Metalorganic CVD	0.9	0.3	0.7	0.8	0	
Toyoko Chemical						—
Metalorganic CVD	0.7	1.0	0.7	1.2	0	
Veeco						—
Resist processing equip.	4.2	2.9	0	0	0	
Ion implantation	9.0	0	0	0	0	
Total	13.2	2.9	0	0	0	

Source: Dataquest (August 1990), Ref: CMPRNK89

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Equipment Data Base

The following is a list of the material in this section:

- Introduction to the Wafer Fab Equipment Data Base
- Wafer Fab Equipment--Summary Data by Category
- Wafer Fab Equipment--Import/Export Data
- Wafer Fab Equipment--Company Shares by Category
- Wafer Fab Equipment--Company Rankings

For additional information, please refer to the material behind the Equipment Data Base tab in your 1989 Newsletter binder.

Introduction to the Wafer Fab Equipment Data Base

Dataquest's Semiconductor Equipment and Materials Service (SEMS) is publishing for the first time its comprehensive data base on wafer fabrication equipment. This data base is the result of an extensive research project conducted by SEMS. We contacted the world's major wafer fab equipment manufacturers, obtaining detailed regional and company market share data for the years 1982 through 1986.

Dataquest has organized the wafer fab equipment market into 10 major categories of front-end processing equipment. These categories, along with key subcategories, are shown in Table 1.

Dataquest estimates the capital spending by the world's merchant and captive semiconductor manufacturers and publishes this estimate in the SEMS Industry Econometrics notebook, behind the "Capital Spending" tab. We consider capital spending to consist of three components: spending for front-end, or wafer fab equipment; spending for back-end, or assembly and test equipment; and spending for property and plant. Thus, the total world market for the 10 categories of wafer fab equipment defined above should equal the total capital spending for front-end equipment by the world's semiconductor manufacturers.

Most of the equipment categories are self-explanatory; however, a few categories require further definition. The Process Control category represents a broad market that includes mask and wafer inspection equipment, process monitoring equipment, surface analysis equipment, and analytical instrumentation. This market is a highly fragmented market with dozens of companies selling into a multitude of noncompetitive market niches.

Factory Automation includes CIM software for shop floor control, factory host computer systems, cell controllers and interface hardware, and wafer transport systems including automatic guided vehicles, robotics, and rail transport systems.

Other Equipment is a general, catch-all category that includes the other capital equipment used throughout the fab but not classified with the other nine major types of wafer processing equipment. Included in this segment are decontamination systems, wafer markers, gas analyzers, storage stations, and other types of equipment.

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Introduction to the Wafer Fab Equipment Data Base

Table 1

WAFER FAB EQUIPMENT CATEGORIES

1. Lithography

   Contact/Proximity
   Projection Aligners
   Steppers
   Direct-Write E-Beam
   Maskmaking E-Beam
   X-Ray

2. Automatic Photoresist Processing Equipment

3. Etch and Clean

   Wet Process
   Dry Strip
   Dry Etch
   Ion Milling

4. Deposition

   Chemical Vapor Deposition
   Physical Vapor Deposition
   Silicon Epitaxy
   Metalorganic CVD
   Molecular Beam Epitaxy

5. Diffusion

6. Rapid Thermal Processing

7. Ion Implantation

   Medium Current
   High Current
   High Voltage

8. Process Control

9. Factory Automation

10. Other Equipment

Source: Dataquest
August 1987

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Introduction to the Wafer Fab Equipment Data Base

CONVENTIONS

The data in the tables represent calendar year shipments, organized by company or by region. For companies with a different fiscal year, calendar year shipments have been estimated. Shipments do not include spare parts or service but do include retrofits and upgrades. Thus, for public companies, the sales reported here may be different from the sales reported in the annual reports. The compound annual growth rate (CAGR) is estimated over the years 1982 to 1986 for each major line item.

EXCHANGE RATES

Japanese-manufactured equipment sold in Japan is valued in dollars in the data base tables at the average exchange rate for each year, as shown below:

YEN/DOLLAR EXCHANGE RATE

1982	1983	1984	1985	1986
248	235	237	238	167

It should be noted that Japanese equipment sold in Japan in 1986 reflects the high yen appreciation rate rather than a true increase in the total market.

EQUIPMENT COMPANIES

Table 2 presents a list of the equipment companies found in the data base tables by region of company ownership. There are a total of 61 U.S. equipment companies, 41 Japanese companies, and 23 European companies in the data base. These 125 major companies account for nearly all of the world's wafer processing equipment in lithography, automatic photoresist processing equipment, dry strip and dry etch, deposition, diffusion, rapid thermal processing, and ion implantation.

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Table 2

EQUIPMENT COMPANIES

U.S. Companies	Japanese Companies	European Companies
AG Associates	Alcan Tech	Advanced Semiconductor Materials
American Semiconductor Equipment Technology	Amaya	AET
Anicon	Anelva	Aixtron
Applied Materials	BIPC	ASM Lithography
Branson/IPC	BTU/Ulvac	Balzers
BTU/Bruce	Canon	Cambridge Instruments
CHA Industries	Dainippon Screen	Centrotherm
Circuits Processing Apparatus	Denki	Convac
Crystal Specialties	Eiko	CVT
CVC Products	Enya	Edwards High Vacuum
CVD Equipment	Ergo Plasma Systems	EEV
Denton Vacuum	Hitachi	E.T. Electrotech
Drytek	Hohkoh Sangyo	HVE Europa
Eaton	Japan Production Eng.	Isa Riber
Emergent Technologies	JEOL	Leybold-Heraeus
Emcore	Kokusai	Thomas Schwonn
Epitaxy, Inc.	Koyo Lindberg	Helmut Seier
Focus Semiconductor	Nikon	Sitesa
Gasonics	Nippon FMC	Karl Suss
GCA	Nippon Sanso	Technics
Gemini Research	Nissin High Voltage	Temescal
General Ionex	Plasma Systems	VG Instruments
Genus	Ramco	Wellman Furnaces
Hampshire Instruments	Samco	
Ion Tech	Seiden	
KLA Instruments	Seiko	
LAM Research	Shimada	
Kurt J. Lesker	Sinko Seiki	
LFE	SPC Electronics	
	Sumitomo	
	Tazmo	

(Continued)

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Table 2 (Continued)

EQUIPMENT COMPANIES

U.S. Companies	Japanese Companies	European Companies
Machine Technology	TEL/LAM	
Materials Research Corp.	TEL/Thermco	
Matrix	TEL/Varian	
Micronix	Tokyo Electron Ltd.	
Nanometrics	Tokyo Ohka	
Nanosil	Tokuda	
National Electrostatics	Toshiba	
Novellus	Ulvac	
Optical Specialties, Inc.	Ushio	
Pacific Western	Yawata	
Peak Systems		
Perkin-Elmer		
Plasma-Therm		
Process Products		
Process Technology		
Psi Star		
Semiconductor Systems, Inc.		
Silicon Valley Group		
Spectrum CVD		
Spire Corporation		
Sputtered Films		
Reid-Ashman		
Tamarack Scientific		
Tegal		
Tempress		
Thermco		
Torrvac		
Tylan		
Ultratech		
Varian		
Watkins-Johnson		
Veeco		

Source: Dataquest
August 1987

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Wafer Fab Equipment—Company Shares by Category

This section of the equipment data base contains detailed company market share data by region for the major front-end equipment categories as shown in Tables 1 through 57. All of the companies that participate in an equipment segment are listed for each region, regardless of whether or not they have sales in a particular region. Although this approach results in a large number of zeros in the tables, it also indicates that Dataquest has not recorded any sales for the company in that region. We believe that this format gives more positive information than eliminating a company with no sales in a given region.

At the beginning of each table, the total world market for a particular equipment category is presented. This total is the same for each category as the total listed in Tables 1 and 2 in the service section entitled "Wafer Fab Equipment—Summary Data by Category." Thus, all tables are completely consistent as one proceeds from the summary tables to the detailed tables presented here in this section.

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Wafer Fab Equipment--Company Shares by Category

Table 1

Total Lithography Company Shares
Worldwide
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Lithography Market	931.3	858.0	685.1	789.9	1,218.8	7.0%
Contact/Proximity						
Canon	50.0	30.3	15.4	11.1	8.7	
Karl Suss	17.0	17.5	16.0	12.4	12.0	
Total Cont./Prox.	67.0	47.8	31.4	23.5	20.7	(25.4%)
Projection Aligners						
Canon	84.6	127.7	49.2	40.6	69.1	
Perkin-Elmer	151.2	138.4	121.8	88.0	90.0	
Total Projection	235.8	266.1	171.0	128.6	159.1	(9.4%)
Steppers						
ASET	10.2	8.1	11.6	11.3	16.0	
ASM Lithography	2.7	2.8	9.1	36.7	58.6	
Canon	12.7	35.0	63.2	89.8	140.0	
Eaton	29.1	21.8	2.1	0	0	
GCA	202.8	114.2	74.6	47.4	104.0	
Hitachi	13.6	17.9	8.2	33.3	49.2	
Perkin-Elmer	21.8	22.2	27.0	25.2	5.0	
Nikon	170.4	157.6	128.4	218.8	457.3	
Ultratech	63.0	50.7	38.9	40.6	73.0	
Total Steppers	526.3	430.3	363.1	503.1	903.1	14.5%
Direct-Write E-Beam						
ASM Lithography	0	1.9	6.0	8.0	6.0	
Cambridge	7.8	9.3	14.5	10.0	8.0	
Hitachi	5.3	5.3	11.2	8.7	9.6	
JEOL	12.1	14.2	30.0	30.8	31.1	
Perkin-Elmer	0	0	6.4	9.6	12.8	
Toshiba	2.5	0	0	0	0	
Varian	1.1	0	0	0	0	
Total Direct-Write	28.8	30.7	68.1	67.1	67.5	23.7%

(Continued)

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Table 1 (Continued)

Total Lithography Company Shares
Worldwide
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Lithography Market	931.3	858.0	685.1	789.9	1,218.8	7.0%
Maskmaking E-Beam						
ASM Lithography	1.8	0	0	4.0	0	
Cambridge	3.9	2.6	0	0	5.0	
Hitachi	2.1	5.7	0	13.4	3.5	
JEOL	8.2	8.2	11.7	18.1	5.0	
Perkin-Elmer	47.5	64.8	36.0	27.0	27.0	
Toshiba	6.3	0	3.0	3.5	7.7	
Varian	1.8	0	0	0	0	
Total Maskmaking	71.6	81.3	50.7	66.0	48.2	(9.4%)
Maskmaking Optical Laser						
Ateq	0	0	0	1.6	11.2	N/A
X-Ray						
Hampshire Instruments	0	0	0	0	1.8	
Karl Suss	1.0	1.0	0	0	7.2	
Micronix	0.8	0.8	0.8	0	0	
Total X-Ray	1.8	1.8	0.8	0	9.0	49.5%
Total Lithography	931.3	858.0	685.1	789.9	1,218.8	7.0%

N/A = Not Applicable

Source: Dataquest
July 1989
Ref: LITHSHR

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Wafer Fab Equipment--Company Shares by Category

Table 2

Contact/Proximity Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Cont./Prox. Market	67.0	47.8	31.4	23.5	20.7	(25.4%)
United States						
Canon	15.6	7.8	5.6	4.5	3.0	
Karl Suss	8.1	7.8	5.5	5.0	5.0	
Total United States	23.7	15.6	11.1	9.5	8.0	(23.8%)
Japan						
Canon	24.3	14.7	5.2	3.6	2.7	
Karl Suss	2.2	3.3	3.9	1.9	2.0	
Total Japan	26.5	18.0	9.1	5.5	4.7	(35.1%)
Europe						
Canon	6.3	3.9	2.6	1.5	1.5	
Karl Suss	2.9	3.2	3.4	3.0	3.0	
Total Europe	9.2	7.1	6.0	4.5	4.5	(16.4%)
Rest of World						
Canon	3.8	3.9	2.0	1.5	1.5	
Karl Suss	3.8	3.2	3.2	2.5	2.0	
Total Rest of World	7.6	7.1	5.2	4.0	3.5	(17.6%)
Worldwide						
Canon	50.0	30.3	15.4	11.1	8.7	
Karl Suss	17.0	17.5	16.0	12.4	12.0	
Total Worldwide	67.0	47.8	31.4	23.5	20.7	(25.4%)

Source: Dataquest
July 1989
Ref: CONTSHR

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Table 3

Projection Aligner Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Projection Market	235.8	266.1	171.0	128.6	159.1	(9.4%)
United States						
Canon	10.0	22.0	13.6	8.4	12.0	
Perkin-Elmer	104.9	96.1	84.8	58.0	60.0	
Total United States	114.9	118.1	98.4	66.4	72.0	(11.0%)
Japan						
Canon	62.1	90.3	25.4	21.7	52.3	
Perkin-Elmer	16.0	15.0	13.0	15.0	14.0	
Total Japan	78.1	105.3	38.4	36.7	66.3	(4.0%)
Europe						
Canon	11.0	9.9	6.4	6.3	3.2	
Perkin-Elmer	22.7	20.7	18.2	11.0	13.0	
Total Europe	33.7	30.6	24.6	17.3	16.2	(16.7%)
Rest of World						
Canon	1.5	5.5	3.8	4.2	1.6	
Perkin-Elmer	7.6	6.6	5.8	4.0	3.0	
Total Rest of World	9.1	12.1	9.6	8.2	4.6	(15.7%)
Worldwide						
Canon	84.6	127.7	49.2	40.6	69.1	
Perkin-Elmer	151.2	138.4	121.8	88.0	90.0	
Total Worldwide	235.8	266.1	171.0	128.6	159.1	(9.4%)

Source: Dataquest
July 1989
Ref: PROJSHR

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Wafer Fab Equipment--Company Shares by Category

Table 4

Stepper Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Stepper Market	526.3	430.3	363.1	503.1	903.1	14.5%
United States						
ASET	10.2	7.3	11.6	10.4	14.0	
ASM Lithography	0.7	2.1	5.8	19.6	39.0	
Canon	0	4.5	21.6	25.2	25.0	
Eaton	11.2	9.3	2.1	0	0	
GCA	91.2	42.1	46.4	36.7	80.6	
Hitachi	0	0	0	0	0	
Perkin-Elmer	14.2	16.4	23.1	18.0	5.0	
Nikon	25.2	20.7	14.8	44.0	71.5	
Ultratech	53.1	32.4	27.4	30.1	44.9	
Total United States	205.8	134.8	152.8	184.0	280.0	8.0%
Japan						
ASET	0	0	0	0	0	
ASM Lithography	0	0	0	0	0	
Canon	12.7	25.3	20.9	24.1	50.0	
Eaton	16.5	11.1	0	0	0	
GCA	86.5	25.7	9.6	4.4	3.9	
Hitachi	12.3	17.2	8.2	33.3	49.2	
Perkin-Elmer	0	0	0	0	0	
Nikon	138.6	128.6	98.8	151.0	319.8	
Ultratech	0	1.6	1.6	0	2.3	
Total Japan	266.6	209.5	139.1	212.8	425.2	12.4%
Europe						
ASET	0	0.8	0	0.9	0	
ASM Lithography	2.0	0.7	3.3	17.1	16.9	
Canon	0	5.2	15.3	18.0	20.0	
Eaton	0	1.4	0	0	0	
GCA	16.7	28.1	16.7	6.3	18.2	
Hitachi	0	0	0	0	0	
Perkin-Elmer	7.6	5.8	0	2.7	0	
Nikon	0	1.4	3.7	6.2	16.5	
Ultratech	5.6	11.5	6.7	7.3	12.9	
Total Europe	31.9	54.9	45.7	58.5	84.5	27.6%

(Continued)

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Table 4 (Continued)

Stepper Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Stepper Market	526.3	430.3	363.1	503.1	903.1	14.5%
Rest of World						
ASET	0	0	0	0	2.0	
ASM Lithography	0	0	0	0	2.7	
Canon	0	0	5.4	22.5	45.0	
Eaton	1.4	0	0	0	0	
GCA	8.4	18.3	1.9	0	1.3	
Hitachi	1.3	0.7	0	0	0	
Perkin-Elmer	0	0	3.9	4.5	0	
Nikon	6.6	6.9	11.1	17.6	49.5	
Ultratech	4.3	5.2	3.2	3.2	12.9	
Total Rest of World	22.0	31.1	25.5	47.8	113.4	50.7%
Worldwide						
ASET	10.2	8.1	11.6	11.3	16.0	
ASM Lithography	2.7	2.8	9.1	36.7	58.6	
Canon	12.7	35.0	63.2	89.8	140.0	
Eaton	29.1	21.8	2.1	0	0	
GCA	202.8	114.2	74.6	47.4	104.0	
Hitachi	13.6	17.9	8.2	33.3	49.2	
Perkin-Elmer	21.8	22.2	27.0	25.2	5.0	
Nikon	170.4	157.6	128.4	218.8	457.3	
Ultratech	63.0	50.7	38.9	40.6	73.0	
Total Worldwide	526.3	430.3	363.1	503.1	903.1	14.5%

Source: Dataquest
July 1989
Ref: STEPSHR

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Table 5

Stepper Company Shares
Regional
(Units)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Stepper Market	859	680	456	520	818	(1.2%)
United States						
ASET	15	9	14	11	14	
ASM Lithography	1	3	7	16	30	
Canon	0	7	22	28	25	
Eaton	16	13	3	0	0	
GCA	131	60	72	41	62	
Hitachi	0	0	0	0	0	
Perkin-Elmer	15	17	24	20	5	
Nikon	38	30	20	50	65	
Ultratech	124	62	44	37	41	
Total United States	340	201	206	203	242	(8.1%)
Japan						
ASET	0	0	0	0	0	
ASM Lithography	0	0	0	0	0	
Canon	20	39	20	20	50	
Eaton	25	17	0	0	0	
GCA	122	42	10	4	3	
Hitachi	19	24	9	30	40	
Perkin-Elmer	0	0	0	0	0	
Nikon	249	225	110	148	295	
Ultratech	0	3	3	0	3	
Total Japan	435	350	152	202	391	(2.6%)
Europe						
ASET	0	1	0	1	0	
ASM Lithography	3	1	4	14	13	
Canon	0	8	17	20	20	
Eaton	0	2	0	0	0	
GCA	24	40	26	7	14	
Hitachi	0	0	0	0	0	
Perkin-Elmer	8	6	0	3	0	
Nikon	0	2	5	7	15	
Ultratech	13	22	12	9	14	
Total Europe	48	82	64	61	76	12.2%

(Continued)

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Table 5 (Continued)

Stepper Company Shares
Regional
(Units)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Stepper Market	859	680	456	520	818	(1.2%)
Rest of World						
ASET	0	0	0	0	2	
ASM Lithography	0	0	0	0	2	
Canon	0	0	6	25	45	
Eaton	2	0	0	0	0	
GCA	12	26	3	0	1	
Hitachi	2	1	0	0	0	
Perkin-Elmer	0	0	4	5	0	
Nikon	10	10	15	20	45	
Ultratech	10	10	6	4	14	
Total Rest of World	36	47	34	54	109	31.9%
Worldwide						
ASET	15	10	14	12	16	
ASM Lithography	4	4	11	30	45	
Canon	20	54	65	93	140	
Eaton	43	32	3	0	0	
GCA	289	168	111	52	80	
Hitachi	21	25	9	30	40	
Perkin-Elmer	23	23	28	28	5	
Nikon	297	267	150	225	420	
Ultratech	147	97	65	50	72	
Total Worldwide	859	680	456	520	818	(1.2%)

Source: Dataquest
July 1989
Ref: STEPUNIT

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Table 6

Direct-Write E-Beam Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Direct-Write Market	28.8	30.7	68.1	67.1	67.5	23.7%
United States						
ASM Lithography	0	1.9	4.0	4.0	2.0	
Cambridge	3.9	2.6	10.0	4.0	2.0	
Hitachi	0	0	0	0	0	
JEOL	5.0	7.0	10.0	6.0	6.0	
Perkin-Elmer	0	0	6.4	3.2	3.2	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total United States	8.9	11.5	30.4	17.2	13.2	10.4%
Japan						
ASM Lithography	0	0	0	0	0	
Cambridge	0	0	0	0	0	
Hitachi	5.3	5.3	11.2	8.7	9.6	
JEOL	4.6	4.7	18.0	20.8	23.1	
Perkin-Elmer	0	0	0	3.2	3.2	
Toshiba	2.5	0	0	0	0	
Varian	0	0	0	0	0	
Total Japan	12.4	10.0	29.2	32.7	35.9	30.4%
Europe						
ASM Lithography	0	0	2.0	4.0	4.0	
Cambridge	3.9	6.7	4.5	4.0	4.0	
Hitachi	0	0	0	0	0	
JEOL	0	2.5	2.0	4.0	2.0	
Perkin-Elmer	0	0	0	3.2	6.4	
Toshiba	0	0	0	0	0	
Varian	1.1	0	0	0	0	
Total Europe	5.0	9.2	8.5	15.2	16.4	34.6%

(Continued)

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Table 6 (Continued)

Direct-Write E-Beam Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Direct-Write Market	28.8	30.7	68.1	67.1	67.5	23.7%
Rest of World						
ASM Lithography	0	0	0	0	0	
Cambridge	0	0	0	2.0	2.0	
Hitachi	0	0	0	0	0	
JEOL	2.5	0	0	0	0	
Perkin-Elmer	0	0	0	0	0	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Rest of World	2.5	0	0	2.0	2.0	(5.4%)
Worldwide						
ASM Lithography	0	1.9	6.0	8.0	6.0	
Cambridge	7.8	9.3	14.5	10.0	8.0	
Hitachi	5.3	5.3	11.2	8.7	9.6	
JEOL	12.1	14.2	30.0	30.8	31.1	
Perkin-Elmer	0	0	6.4	9.6	12.8	
Toshiba	2.5	0	0	0	0	
Varian	1.1	0	0	0	0	
Total Worldwide	28.8	30.7	68.1	67.1	67.5	23.7%

Source: Dataquest
July 1989
Ref: DWEBSH

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Table 7

Direct-Write E-Beam Company Shares
Regional
(Units)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Direct-Write Market	15	16	27	24	22	10.0%
United States						
ASM Lithography	0	1	2	2	1	
Cambridge	3	2	5	2	1	
Hitachi	0	0	0	0	0	
JEOL	2	4	5	3	3	
Perkin-Elmer	0	0	2	1	1	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total United States	5	7	14	8	6	4.7%
Japan						
ASM Lithography	0	0	0	0	0	
Cambridge	0	0	0	0	0	
Hitachi	2	2	3	2	2	
JEOL	2	2	5	5	5	
Perkin-Elmer	0	0	0	1	1	
Toshiba	1	0	0	0	0	
Varian	0	0	0	0	0	
Total Japan	5	4	8	8	8	12.5%
Europe						
ASM Lithography	0	0	1	2	2	
Cambridge	3	4	3	2	2	
Hitachi	0	0	0	0	0	
JEOL	0	1	1	2	1	
Perkin-Elmer	0	0	0	1	2	
Toshiba	0	0	0	0	0	
Varian	1	0	0	0	0	
Total Europe	4	5	5	7	7	15.0%

(Continued)

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Table 7 (Continued)

Direct-Write E-Beam Company Shares
Regional
(Units)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Direct-Write Market	15	16	27	24	22	10.0%
Rest of World						
ASM Lithography	0	0	0	0	0	
Cambridge	0	0	0	1	1	
Hitachi	0	0	0	0	0	
JEOL	1	0	0	0	0	
Perkin-Elmer	0	0	0	0	0	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Rest of World	1	0	0	1	1	0
Worldwide						
ASM Lithography	0	1	3	4	3	
Cambridge	6	6	8	5	4	
Hitachi	2	2	3	2	2	
JEOL	5	7	11	10	9	
Perkin-Elmer	0	0	2	3	4	
Toshiba	1	0	0	0	0	
Varian	1	0	0	0	0	
Total Worldwide	15	16	27	24	22	10.0%

Source: Dataquest
July 1989
Ref: DWUNITS

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Table 8

Maskmaking E-Beam Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Maskmaking Market	71.6	81.3	50.7	66.0	48.2	(9.4%)
United States						
ASM Lithography	0	0	0	0	0	
Cambridge	1.3	1.3	0	0	0	
Hitachi	0	0	0	0	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	17.5	37.8	27.0	12.0	12.0	
Toshiba	0	0	0	0	0	
Varian	1.8	0	0	0	0	
Total United States	20.6	39.1	27.0	12.0	12.0	(12.6%)
Japan						
ASM Lithography	0	0	0	0	0	
Cambridge	0	0	0	0	0	
Hitachi	2.1	5.7	0	10.4	3.5	
JEOL	8.2	8.2	11.7	18.1	5.0	
Perkin-Elmer	25.0	21.6	9.0	6.0	3.0	
Toshiba	6.3	0	3.0	3.5	7.7	
Varian	0	0	0	0	0	
Total Japan	41.6	35.5	23.7	38.0	19.2	(17.6%)
Europe						
ASM Lithography	1.8	0	0	4.0	0	
Cambridge	2.6	1.3	0	0	0	
Hitachi	0	0	0	3.0	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	5.0	2.7	0	6.0	6.0	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Europe	9.4	4.0	0	13.0	6.0	(10.6%)

(Continued)

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Table 8 (Continued)

Maskmaking E-Beam Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Maskmaking Market	71.6	81.3	50.7	66.0	48.2	(9.4%)
Rest of World						
ASM Lithography	0	0	0	0	0	
Cambridge	0	0	0	0	5.0	
Hitachi	0	0	0	0	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	0	2.7	0	3.0	6.0	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Rest of World	0	2.7	0	3.0	11.0	N/A
Worldwide						
ASM Lithography	1.8	0	0	4.0	0	
Cambridge	3.9	2.6	0	0	5.0	
Hitachi	2.1	5.7	0	13.4	3.5	
JEOL	8.2	8.2	11.7	18.1	5.0	
Perkin-Elmer	47.5	64.8	36.0	27.0	27.0	
Toshiba	6.3	0	3.0	3.5	7.7	
Varian	1.8	0	0	0	0	
Total Worldwide	71.6	81.3	50.7	66.0	48.2	(9.4%)

N/A = Not Applicable

Source: Dataquest
July 1989
Ref: MMEBSHR

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Table 9

Maskmaking E-Beam Company Shares
Regional
(Units)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Maskmaking Market	31	32	16	20	15	(16.6%)
United States						
ASM Lithography	0	0	0	0	0	
Cambridge	1	1	0	0	0	
Hitachi	0	0	0	0	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	7	14	9	4	4	
Toshiba	0	0	0	0	0	
Varian	1	0	0	0	0	
Total United States	9	15	9	4	4	(18.4%)
Japan						
ASM Lithography	0	0	0	0	0	
Cambridge	0	0	0	0	0	
Hitachi	1	3	0	3	1	
JEOL	3	3	3	4	1	
Perkin-Elmer	10	8	3	2	1	
Toshiba	3	0	1	1	2	
Varian	0	0	0	0	0	
Total Japan	17	14	7	10	5	(26.4%)
Europe						
ASM Lithography	1	0	0	2	0	
Cambridge	2	1	0	0	0	
Hitachi	0	0	0	1	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	2	1	0	2	2	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Europe	5	2	0	5	2	(20.5%)

(Continued)

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Table 9 (Continued)

Maskmaking E-Beam Company Shares
Regional
(Units)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Maskmaking Market	31	32	16	20	15	(16.6%)
Rest of World						
ASM Lithography	0	0	0	0	0	
Cambridge	0	0	0	0	2	
Hitachi	0	0	0	0	0	
JEOL	0	0	0	0	0	
Perkin-Elmer	0	1	0	1	2	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Rest of World	0	1	0	1	4	N/A
Worldwide						
ASM Lithography	1	0	0	2	0	
Cambridge	3	2	0	0	2	
Hitachi	1	3	0	4	1	
JEOL	3	3	3	4	1	
Perkin-Elmer	19	24	12	9	9	
Toshiba	3	0	1	1	2	
Varian	1	0	0	0	0	
Total Worldwide	31	32	16	20	15	(16.6%)

N/A = Not Applicable

Source: Dataquest
July 1989
Ref: MMUNITS

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Table 10

Total E-Beam Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World E-Beam Market	100.4	112.0	118.8	133.1	115.7	3.6%
United States						
ASM Lithography	0	1.9	4.0	4.0	2.0	
Cambridge	5.2	3.9	10.0	4.0	2.0	
Hitachi	0	0	0	0	0	
JEOL	5.0	7.0	10.0	6.0	6.0	
Perkin-Elmer	17.5	37.8	33.4	15.2	15.2	
Toshiba	0	0	0	0	0	
Varian	1.8	0	0	0	0	
Total United States	29.5	50.6	57.4	29.2	25.2	(3.9%)
Japan						
ASM Lithography	0	0	0	0	0	
Cambridge	0	0	0	0	0	
Hitachi	7.4	11.0	11.2	19.1	13.1	
JEOL	12.8	12.9	29.7	38.9	28.1	
Perkin-Elmer	25.0	21.6	9.0	9.2	6.2	
Toshiba	8.8	0	3.0	3.5	7.7	
Varian	0	0	0	0	0	
Total Japan	54.0	45.5	52.9	70.7	55.1	0.5%
Europe						
ASM Lithography	1.8	0	2.0	8.0	4.0	
Cambridge	6.5	8.0	4.5	4.0	4.0	
Hitachi	0	0	0	3.0	0	
JEOL	0	2.5	2.0	4.0	2.0	
Perkin-Elmer	5.0	2.7	0	9.2	12.4	
Toshiba	0	0	0	0	0	
Varian	1.1	0	0	0	0	
Total Europe	14.4	13.2	8.5	28.2	22.4	11.7%

(Continued)

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Table 10

Total E-Beam Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World E-Beam Market	100.4	112.0	118.8	133.1	115.7	3.6%
Rest of World						
ASM Lithography	0	0	0	0	0	
Cambridge	0	0	0	2.0	7.0	
Hitachi	0	0	0	0	0	
JEOL	2.5	0	0	0	0	
Perkin-Elmer	0	2.7	0	3.0	6.0	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Rest of World	2.5	2.7	0	5.0	13.0	51.0%
Worldwide						
ASM Lithography	1.8	1.9	6.0	12.0	6.0	
Cambridge	11.7	11.9	14.5	10.0	13.0	
Hitachi	7.4	11.0	11.2	22.1	13.1	
JEOL	20.3	22.4	41.7	48.9	36.1	
Perkin-Elmer	47.5	64.8	42.4	36.6	39.8	
Toshiba	8.8	0	3.0	3.5	7.7	
Varian	2.9	0	0	0	0	
Total Worldwide	100.4	112.0	118.8	133.1	115.7	3.6%

Source: Dataquest
July 1989
Ref: TEBSHR

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Table 11

Total E-Beam Company Shares
Regional
(Units)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World E-Beam Market	46	48	43	44	37	(5.3%)
United States						
ASM Lithography	0	1	2	2	1	
Cambridge	4	3	5	2	1	
Hitachi	0	0	0	0	0	
JEOL	2	4	5	3	3	
Perkin-Elmer	7	14	11	5	5	
Toshiba	0	0	0	0	0	
Varian	1	0	0	0	0	
Total United States	14	22	23	12	10	(8.1%)
Japan						
ASM Lithography	0	0	0	0	0	
Cambridge	0	0	0	0	0	
Hitachi	3	5	3	5	3	
JEOL	5	5	8	9	6	
Perkin-Elmer	10	8	3	3	2	
Toshiba	4	0	1	1	2	
Varian	0	0	0	0	0	
Total Japan	22	18	15	18	13	(12.3%)
Europe						
ASM Lithography	1	0	1	4	2	
Cambridge	5	5	3	2	2	
Hitachi	0	0	0	1	0	
JEOL	0	1	1	2	1	
Perkin-Elmer	2	1	0	3	4	
Toshiba	0	0	0	0	0	
Varian	1	0	0	0	0	
Total Europe	9	7	5	12	9	0

(Continued)

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Table 11 (Continued)

Total E-Beam Company Shares
Regional
(Units)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World E-Beam Market	46	48	43	44	37	(5.3%)
Rest of World						
ASM Lithography	0	0	0	0	0	
Cambridge	0	0	0	1	3	
Hitachi	0	0	0	0	0	
JEOL	1	0	0	0	0	
Perkin-Elmer	0	1	0	1	2	
Toshiba	0	0	0	0	0	
Varian	0	0	0	0	0	
Total Rest of World	1	1	0	2	5	49.5%
Worldwide						
ASM Lithography	1	1	3	6	3	
Cambridge	9	8	8	5	6	
Hitachi	3	5	3	6	3	
JEOL	8	10	14	14	10	
Perkin-Elmer	19	24	14	12	13	
Toshiba	4	0	1	1	2	
Varian	2	0	0	0	0	
Total Worldwide	46	48	43	44	37	(5.3%)

Source: Dataquest
July 1989
Ref: TEBUNITS

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Table 12

X-Ray Aligner Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World X-Ray Market	1.8	1.8	0.8	0	9.0	49.5%
United States						
Hampshire Instruments	0	0	0	0	1.8	
Micronix	0	0	0	0	0	
Perkin-Elmer	0	0	0	0	0	
Karl Suss	0	0	0	0	1.6	
Total United States	0	0	0	0	3.4	N/A
Japan						
Hampshire Instruments	0	0	0	0	0	
Micronix	8	0.8	0.8	0	0	
Perkin-Elmer	0	0	0	0	0	
Karl Suss	0	0	0	0	2.8	
Total Japan	0.8	0.8	0.8	0	2.8	36.8%
Europe						
Hampshire Instruments	0	0	0	0	0	
Micronix	0	0	0	0	0	
Perkin-Elmer	0	0	0	0	0	
Kark Suss	1.0	1.0	0	0	2.8	
Total Europe	1.0	1.0	0	0	2.8	29.4%
Rest of World						
Hampshire Instruments	0	0	0	0	0	
Micronix	0	0	0	0	0	
Perkin-Elmer	0	0	0	0	0	
Karl Suss	0	0	0	0	0	
Total Rest of World	0	0	0	0	0	N/A
Worldwide						
Hampshire Instruments	0	0	0	0	1.8	
Micronix	0.8	0.8	0.8	0	0	
Perkin-Elmer	0	0	0	0	0	
Karl Suss	1.0	1.0	0	0	7.2	
Total Worldwide	1.8	1.8	0.8	0	9.0	49.5%

N/A = Not Available

Source: Dataquest
July 1989
Ref: XRAYSHR

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Table 13

Automatic Photoresist Processing Equipment (Track) Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Track Market	183.5	157.6	145.8	164.1	249.7	8.0%
United States						
Canon	0	0	0	0	0	
Convac	0.3	1.0	2.0	4.0	5.9	
Dainippon Screen	0.2	1.7	0.2	0.5	3.1	
Eaton	7.2	6.0	5.0	3.7	1.1	
GCA	14.0	6.0	6.5	2.8	2.2	
Machine Technology	18.4	15.3	11.3	10.1	7.9	
Semiconductor Systems	13.0	7.9	7.9	9.6	19.8	
Silicon Valley Group	23.6	21.3	15.5	20.8	25.4	
Solitec	4.4	4.9	6.3	5.3	5.6	
Tazmo	0	0	0.5	2.0	2.0	
Tokyo Electron Ltd.	0	2	0.9	2.1	5.0	
Veeco	3.8	4.2	2.9	0	0	
Total United States	84.9	68.5	59.0	60.9	78.0	(2.1%)
Japan						
Canon	0	0	0.2	0.7	3.8	
Convac	0	0	0	0	0	
Dainippon Screen	36.7	29.4	27.4	27.8	38.5	
Eaton	0	0	0	0	0	
GCA	2.6	1.0	0.8	0.3	0.2	
Machine Technology	0.1	0.1	0.1	0.3	0.5	
Semiconductor Systems	0	0	0	0	0	
Silicon Valley Group	0	0	0	0	0	
Solitec	0	0	0	0	0	
Tazmo	1.2	1.1	1.6	2.1	2.9	
Tokyo Electron Ltd.	26.2	22.7	21.4	30.6	73.8	
Veeco	0	0	0	0	0	
Total Japan	66.8	54.3	51.5	61.8	119.7	15.7%

(Continued)

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Table 13 (Continued)

Automatic Photoresist Processing Equipment (Track) Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Track Market	183.5	157.6	145.8	164.1	249.7	8.0%
Europe						
Canon	0	0	0.3	0.3	0	
Convac	2.7	2.8	4.4	6.9	7.9	
Dainippon Screen	0	0	1.2	1.9	2.7	
Eaton	6.1	5.0	6.0	5.2	6.6	
GCA	8.9	5.0	4.0	3.2	2.5	
Machine Technology	1.7	2.3	1.3	1.0	1.3	
Semiconductor Systems	0	0.9	0.9	1.2	2.2	
Silicon Valley Group	4.0	5.2	7.0	6.9	6.4	
Solitec	0.1	0.1	0.2	0.1	0.4	
Tazmo	0	0	0.3	0.3	0.3	
Tokyo Electron Ltd.	0	1.0	1.5	1.5	2.2	
Veeco	0	0	0	0	0	
Total Europe	23.5	22.3	27.1	28.5	32.5	8.4%
Rest of World						
Canon	0	0	0	0	0	
Convac	0	0	0	0	0	
Dainippon Screen	1.5	3.8	1.0	1.0	2.7	
Eaton	1.2	1.0	1.0	1.6	3.3	
GCA	0	3.0	1.0	0.7	0.6	
Machine Technology	0.1	0.1	0.2	1.3	0.3	
Semiconductor Systems	0	0	0	0	0	
Silicon Valley Group	5.5	4.0	3.1	5.3	5.6	
Solitec	0	0	0	0.8	1.5	
Tazmo	0	0	0.1	0.2	0.5	
Tokyo Electron Ltd.	0	0.6	1.8	2.0	5.0	
Veeco	0	0	0	0	0	
Total Rest of World	8.3	12.5	8.2	12.9	19.5	23.8%

(Continued)

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Table 13 (Continued)

Automatic Photoresist Processing Equipment (Track) Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Track Market	183.5	157.6	145.8	164.1	249.7	8.0%
Worldwide						
Canon	0	0	0.5	1.0	3.8	
Convac	3.0	3.8	6.4	10.9	13.8	
Dainippon Screen	38.4	34.9	29.8	31.2	47.0	
Eaton	14.5	12.0	12.0	10.5	11.0	
GCA	25.5	15.0	12.3	7.0	5.5	
Machine Technology	20.3	17.8	12.9	12.7	10.0	
Semiconductor Systems	13.0	8.8	8.8	10.8	22.0	
Silicon Valley Group	33.1	30.5	25.6	33.0	37.4	
Solitec	4.5	5.0	6.5	6.2	7.5	
Tazmo	1.2	1.1	2.5	4.6	5.7	
Tokyo Electron Ltd.	26.2	24.5	25.6	36.2	86.0	
Veeco	3.8	4.2	2.9	0	0	
Total Worldwide	183.5	157.6	145.8	164.1	249.7	8.0%

Source: Dataquest
July 1989
Ref: TRACKSHR

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Table 14

Wet Process Company Shares
United States
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Wet Process Market	171.7	157.2	161.9	165.0	235.1	8.2%
Integrated Wet Systems						
Enya	0	0	0	0	0	
Dexon	0	0	0	0.7	3.1	
Dianippon Screen	0	0	0	0	2.2	
Integrated Air Systems	0.4	1.0	1.4	2.3	1.8	
Kaijo Denki	0	0	1.5	0.6	3.1	
Kuwano Electric	0	0	0	0	0.9	
Pokorny	0	0	0	0	0	
Poly-Flow Engineering	0	0.1	0.1	0.1	0	
Pure-Aire	1.3	1.0	1.0	1.5	1.7	
Sankyo Engineering	0	0	0.5	1.2	0	
Santa Clara Plastics	4.0	8.0	8.0	6.0	6.0	
Sci Manufacturing	0	0	0	2.8	5.2	
Semifab	0	0	1.0	2.6	5.0	
Sugai	0	0	0	0	0	
S&K Products Internat.	0	0.5	1.0	1.5	2.0	
Universal Plastics	0	0	0.3	1.6	3.1	
Verteq	1.9	2.0	3.0	0.8	1.8	
Total Integr. Systems	7.6	12.6	17.8	21.7	35.9	47.4%
Manual Wet Benches						
Enya	0	0	0	0	0	
Dexon	1.7	3.5	1.8	2.1	2.3	
Dianippon Screen	0	0	0	0	0.4	
Integrated Air Systems	5.6	4.0	2.6	0.7	0.2	
Kaijo Denki	0	0	0	0	0	
Pokorny	0	0	0	0	0	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0.8	0.7	0.6	0.6	0.5	
Sankyo Engineering	0	0	0	0	0	
Santa Clara Plastics	13.0	10.0	5.0	3.0	1.8	
Sci Manufacturing	0	0	0	2.0	2.8	
Semifab	5.2	4.2	4.7	4.3	1.2	
Shimada	0	0	0	0	0	
Sugai	0	0	0	0	0	
Universal Plastics	0	0.1	1.2	1.9	4.6	
Verteq	0	0	0.1	0	0.4	
Total Man. Benches	26.3	22.5	16.0	14.6	14.2	(14.3%)

(Continued)

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Table 14 (Continued)

Wet Process Company Shares
United States
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Wet Process Market	171.7	157.2	161.9	165.0	235.1	8.2%
Rinsers/Dryers						
Dianippon Screen	0	0	0	0	0.7	
Enya	0	0	0	0	0	
Estek	0	0	0	0.8	0.8	
FSI International	1.8	1.2	0.8	0.7	0.9	
Kaijo Denki	0	0	0	0	0.3	
Kuwano	0	0	0	0	0	
Poly-Flow Engineering	0.1	0.6	0.2	0.2	0.1	
Sankyo Engineering	0	0	0	0	0.2	
Semitool	12.8	10.7	9.0	10.9	9.7	
Shimada	0	0	0	0	0	
S&K Products Internat.	0.2	0.3	0.4	0.6	0.9	
Sugai	0	0	0	0	0	
Verteq	2.1	2.2	3.0	2.7	4.0	
Total Rinser/Dryers	17.0	15.0	13.4	15.9	17.6	0.9%
Acid Processors						
Athens	0	0	0	1.0	4.0	
CFM Technology	0	0	0	0	1.0	
FSI International	11.2	11.0	10.9	7.5	8.4	
Poly-Flow Engineering	0	0.1	0.1	0.1	0	
Semitool	2.7	2.7	2.7	2.2	2.9	
Total Acid Process.	13.9	13.8	13.7	10.8	16.3	4.1%
Megasonic Cleaners						
FSI International	0.8	0.9	1.2	1.2	1.2	
Kaijo Denki	0	0	0	0	0	
Verteq	0.6	0.8	1.2	1.7	3.2	
Total Megasonics	1.4	1.7	2.4	2.9	4.4	33.1%
Total U.S. Wet Proc.	66.2	65.6	63.3	65.9	88.4	7.5%

Source: Dataquest
July 1989
Ref: WETSH

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Table 15

Wet Process Company Shares
Japan
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Wet Process Market	171.7	157.2	161.9	165.0	235.1	8.2%
Integrated Wet Systems						
Enya	8.4	6.9	7.8	4.9	5.4	
Dexon	0	0	0	0	0	
Dianippon Screen	22.8	13.9	18.0	18.7	25.7	
Integrated Air Systems	0	0	0	0	0	
Kaijo Denki	11.8	8.4	10.8	6.2	7.7	
Kuwano Electric	2.1	2.5	3.3	5.6	8.5	
Pokorny	0	0	0	0	0	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0	0	0	0	0	
Sankyo Engineering	3.0	3.4	4.8	3.1	5.3	
Santa Clara Plastics	0	0	0	0	0	
Sci Manufacturing	0	0	0	0	0	
Semifab	0	0	0	0	0	
Sugai	3.2	2.8	2.2	2.8	4.2	
S&K Products Internat.	1.0	1.5	1.5	2.0	0	
Universal Plastics	0	0	0	0	0	
Verteq	0	0	0	0	0	
Others	9.5	5.5	6.0	4.2	6.2	
Total Integr. Systems	61.8	44.9	54.4	47.5	63.0	0.5%
Manual Wet Benches						
Enya	1.1	0.6	0.8	0.8	1.3	
Dexon	0	0	0	0	0	
Dianippon Screen	1.9	1.4	1.6	1.8	2.7	
Integrated Air Systems	0	0	0	0	0	
Kaijo Denki	1.1	1.0	0.7	0.8	1.9	
Pokorny	0	0	0	0	0	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0	0	0	0	0	
Sankyo Engineering	1.4	1.1	0.8	0.9	1.9	
Santa Clara Plastics	0	0	0	0	0	
Sci Manufacturing	0	0	0	0	0	
Semifab	0	0	0	0	0	
Shimada	0.7	0.4	0.3	0.3	0.4	
Sugai	0.4	0.2	0.3	0.3	0.3	
Universal Plastics	0	0	0	0	0	
Verteq	0	0	0	0	0	
Others	2.3	2.3	2.1	2.4	3.7	
Total Man. Benches	8.9	7.0	6.6	7.3	12.2	8.2%

(Continued)

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Table 15 (Continued)

Wet Process Company Shares
Japan
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Wet Process Market	171.7	157.2	161.9	165.0	235.1	8.2%
Rinsers/Dryers						
Dianippon Screen	0.7	0.6	1.0	1.2	2.1	
Enya	1.3	1.3	1.0	0.5	0.9	
Estek	0	0	0	0	0	
FSI International	1.5	1.4	1.2	0.7	0.5	
Kaijo Denki	0.8	0.6	0.5	0.6	1.3	
Kuwano	0	0.2	0.6	0.7	0.8	
Poly-Flow Engineering	0	0	0	0	0	
Sankyo Engineering	0.8	0.8	0.8	0.6	1.2	
Semitool	0	0	0	0	0.4	
Shimada	0.4	0.2	0.3	0.2	0.2	
S&K Products Internat.	4.1	3.5	3.3	3.8	4.5	
Sugai	1.1	0.9	1.2	1.4	1.9	
Verteq	0.1	0.1	0.1	0.1	0.4	
Others	0.6	0.4	0.5	0.3	0.5	
Total Rinser/Dryers	11.4	10.0	10.5	10.1	14.7	6.6%
Acid Processors						
Athens	0	0	0	0	0	
CFM Technology	0	0	0	0	0	
FSI International	0.9	0.7	0.9	1.2	1.2	
Poly-Flow Engineering	0	0	0	0	0	
Semitool	0	0	0	0	3	
Total Acid Process.	0.9	0.7	0.9	1.2	1.5	13.6%
Megasonic Cleaners						
FSI International	0	0.1	0.2	0.2	0.1	
Kaijo Denki	0	0	0	0.1	0.1	
Verteq	0	0.1	0	0.1	0.3	
Total Megasonics	0	0.2	0.2	0.4	0.5	N/A
Total Japan Wet Pro.	83.0	62.8	72.6	66.5	91.9	2.6%

N/A = Not Available

Source: Dataquest
July 1989
Ref: WETSH

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Table 16

Wet Process Company Shares
Europe
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Wet Process Market	171.7	157.2	161.9	165.0	235.1	8.2%
Integrated Wet Systems						
Enya	0	0	0	0	0	
Dexon	0	0	0	0	0	
Dianippon Screen	0	0	0	0	0	
Integrated Air Systems	0	0	0	0	0	
Kaijo Denki	0	0	0	1.8	0	
Kuwano Electric	0	0	0	0	2.3	
Pokorny	0	0.3	1.2	2.3	2.5	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0	0	0	0	0	
Sankyo Engineering	0	0	0	1.2	3.1	
Santa Clara Plastics	2.0	3.0	3.0	3.0	3.0	
Sci Manufacturing	0	0	0	0	0	
Semifab	0	0	0	0	0	
Sugai	0	0	0	0	0	
S&K Products Internat.	0	0	0	0	1.5	
Universal Plastics	0	0	0	0	0	
Verteq	0	0	0	0	0	
Total Integr. Systems	2.0	3.3	4.2	8.3	12.4	57.8%
Manual Wet Benches						
Enya	0	0	0	0	0	
Dexon	0	0	1.3	0.3	0.1	
Dianippon Screen	0	0	0	0	0.4	
Integrated Air Systems	0	0	0	0	0	
Kaijo Denki	0	0	0	0	0	
Pokorny	2.2	1.7	1.9	2.0	2.2	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0	0	0	0	0	
Sankyo Engineering	0	0	0	0	3.2	
Santa Clara Plastics	6.0	3.0	2.0	1.0	0.8	
Sci Manufacturing	0	0	0	0	0	
Semifab	0.2	0.5	0.1	0.1	0	
Shimada	0	0	0	0	0	
Sugai	0	0	0	0	0	
Universal Plastics	0	0	0.1	0.1	0	
Verteq	0	0	0	0	0	
Total Man. Benches	8.4	5.2	5.4	3.5	6.7	(5.5%)

(Continued)

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Table 16 (Continued)

Wet Process Company Shares
Europe
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Wet Process Market	171.7	157.2	161.9	165.0	235.1	8.2%
Rinsers/Dryers						
Dianippon Screen	0	0	0	0	0.5	
Enya	0	0	0	0	0	
Estek	0	0	0	0.4	0.3	
FSI International	0.9	1.1	0.4	0.5	0.7	
Kaijo Denki	0	0	0	0	0.2	
Kuwano	0	0	0	0	0	
Poly-Flow Engineering	0	0	0	0	0	
Sankyo Engineering	0	0	0	0	0.2	
Semitool	1.8	1.6	2.0	2.1	1.6	
Shimada	0	0	0	0	0	
S&K Products Internat.	0.3	0.3	0.7	0.6	0.5	
Sugai	0	0	0	0	0	
Verteq	0.2	0.2	0.2	0.3	0.5	
Total Rinser/Dryers	3.2	3.2	3.3	3.9	4.5	8.9%
Acid Processors						
Athens	0	0	0	0	0	
CFM Technology	0	0	0	0	0	
FSI International	5.4	10.5	5.8	5.1	9.1	
Poly-Flow Engineering	0	0	0	0	0.1	
Semitool	0.5	0.5	0.5	0.8	0.4	
Total Acid Process.	5.9	11.0	6.3	5.9	9.6	12.9%
Megasonic Cleaners						
FSI International	0	0.1	0.3	0.5	0.5	
Kaijo Denki	0	0	0	0	0	
Verteq	0.1	0.1	0.1	0.3	0.5	
Total Megasonics	0.1	0.2	0.4	0.8	1.0	77.8%
Total Eur. Wet Proc.	19.6	22.9	19.6	22.4	34.2	14.9%

Source: Dataquest
July 1989
Ref: WETSH

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Table 17

Wet Process Company Shares
Rest of World
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Wet Process Market	171.7	157.2	161.9	165.0	235.1	8.2%
Integrated Wet Systems						
Enya	0	0	0	0	0	
Dexon	0	0	0	0	0.4	
Dianippon Screen	0	0	0	0	2.2	
Integrated Air Systems	0	0	0	0	0	
Kaijo Denki	0	0	0	0	0	
Kuwano Electric	0	0	0	0	0.9	
Pokorny	0	0	0	0	0	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0	0	0.1	0.2	0.2	
Sankyo Engineering	0	0	0.5	1.1	1.8	
Santa Clara Plastics	0	1.0	1.0	2.0	2.0	
Sci Manufacturing	0	0	0	0	0	
Semifab	0	0	0	0.1	0	
Sugai	0	0	0	0	0	
S&K Products Internat.	0	0.5	0	0	0	
Universal Plastics	0	0	0	0	0	
Verteq	0.6	0	0.5	0	0.2	
Total Integr. Systems	0.6	1.5	2.1	3.4	7.7	89.3%
Manual Wet Benches						
Enya	0	0	0	0	0	
Dexon	0	0	0	0	0	
Dianippon Screen	0	0	0	0	0.4	
Integrated Air Systems	0	0	0	0	0	
Kaijo Denki	0	0	0	0	0	
Pokorny	0	0	0	0	0	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0.1	0.1	0.1	0.1	0.4	
Sankyo Engineering	0	0	0	0	6.5	
Santa Clara Plastics	0	1.0	1.0	1.0	1.0	
Sci Manufacturing	0	0	0	0	0	
Semifab	0.7	0.1	0.6	0.6	0.8	
Shimada	0	0	0	0	0	
Sugai	0	0	0	0	0	
Universal Plastics	0	0	0	0.1	0.8	
Verteq	0.2	0.1	0	0.2	0.1	
Total Man. Benches	1.0	1.3	1.7	2.0	10.0	77.8%

(Continued)

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Table 17 (Continued)

Wet Process Company Shares
Rest of World
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Wet Process Market	171.7	157.2	161.9	165.0	235.1	8.2%
Rinsers/Dryers						
Dianippon Screen	0	0	0	0	0.5	
Enya	0	0	0	0	0	
Estek	0	0	0	0	0	
FSI International	0.2	0.2	0.1	0.2	0.1	
Kaijo Denki	0	0	0	0	0	
Kuwano	0	0	0	0	0	
Poly-Flow Engineering	0	0	0.1	0.1	0	
Sankyo Engineering	0	0	0	0	0.4	
Semitool	0.4	1.4	1.6	2.5	0.1	
Shimada	0	0	0	0	0	
S&K Products Internat.	0	0	0	0	0	
Sugai	0	0	0	0	0	
Verteq	0.1	0.2	0.1	0.2	0.4	
Total Rinser/Dryers	0.7	1.8	1.9	3.0	1.5	21.0%
Acid Processors						
Athens	0	0	0	0	0	
CFM Technology	0	0	0	0	0	
FSI International	0.5	1.2	0.5	1.2	0.7	
Poly-Flow Engineering	0	0	0	0	0	
Semitool	0	0	0.1	0.3	0	
Total Acid Process.	0.5	1.2	0.6	1.5	0.7	8.8%
Megasonic Cleaners						
FSI International	0	0	0.1	0.2	0.7	
Kaijo Denki	0	0	0	0	0	
Verteq	0.1	0.1	0	0.1	0	
Total Megasonics	0.1	0.1	0.1	0.3	0.7	62.7%
Total ROW Wet Proc.	2.9	5.9	6.4	10.2	20.6	63.3%

Source: Dataquest
July 1989
Ref: WETSH

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Table 18

Wet Process Company Shares
Worldwide
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Wet Process Market	171.7	157.2	161.9	165.0	235.1	8.2%
Integrated Wet Systems						
Enya	8.4	6.9	7.8	4.9	5.4	
Dexon	0	0	0	0.7	3.5	
Dianippon Screen	22.8	13.9	18.0	18.7	30.1	
Integrated Air systems	0.4	1.0	1.4	2.3	1.8	
Kaijo Denki	11.8	8.4	12.3	8.6	10.8	
Kuwano Electric	2.1	2.5	3.3	5.6	12.6	
Pokorny	0	0.3	1.2	2.3	2.5	
Poly-Flow Engineering	0	0.1	0.1	0.1	0	
Pure-Aire	1.3	1.0	1.1	1.7	1.9	
Sankyo Engineering	3.0	3.4	5.8	6.6	10.2	
Santa Clara Plastics	6.0	12.0	12.0	11.0	11.0	
Sci Manufacturing	0	0	0	2.8	5.2	
Semifab	0	0	1.0	2.7	5.0	
Sugai	3.2	2.8	2.2	2.8	4.2	
S&K Products Internat.	1.0	2.5	2.5	3.5	3.5	
Universal Plastics	0	0	0.3	1.6	3.1	
Verteq	2.5	2.0	3.5	0.8	2.0	
Others	9.5	5.5	6.0	4.2	6.2	
Total Integr. Systems	72.0	62.3	78.5	80.9	119.0	13.4%
Manual Wet Benches						
Enya	1.1	0.6	0.8	0.8	1.3	
Dexon	1.7	3.5	3.1	2.4	2.4	
Dianippon Screen	1.9	1.4	1.6	1.8	3.9	
Integrated Air Systems	5.6	4.0	2.6	0.7	0.2	
Kaijo Denki	1.1	1.0	0.7	0.8	1.9	
Pokorny	2.2	1.7	1.9	2.0	2.2	
Poly-Flow Engineering	0	0	0	0	0	
Pure-Aire	0.9	0.8	0.7	0.7	0.9	
Sankyo Engineering	1.4	1.1	0.8	0.9	11.6	
Santa Clara Plastics	19.0	14.0	8.0	5.0	3.6	
Sci Manufacturing	0	0	0	2.0	2.8	
Semifab	6.1	4.8	5.4	5.0	2.0	
Shimada	0.7	0.4	0.3	0.3	0.4	
Sugai	0.4	0.2	0.3	0.3	0.3	
Universal Plastics	0	0.1	1.3	2.1	5.4	
Verteq	0.2	0.1	0.1	0.2	0.5	
Others	2.3	2.3	2.1	2.4	3.7	
Total Man. Benches	44.6	36.0	29.7	27.4	43.1	(0.9%)

(Continued)

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Table 18 (Continued)

Wet Process Company Shares
Worldwide
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Wet Process Market	171.7	157.2	161.9	165.0	235.1	8.2%
Rinsers/Dryers						
Dianippon Screen	0.7	0.6	1.0	1.2	3.8	
Enya	1.3	1.3	1.0	0.5	0.9	
Estek	0	0	0	1.2	1.1	
FSI International	4.4	3.9	2.5	2.1	2.2	
Kaijo Denki	0.8	0.6	0.5	0.6	1.8	
Kuwano	0	0.2	0.6	0.7	0.8	
Poly-Flow Engineering	0.1	0.6	0.3	0.3	0.1	
Sankyo Engineering	0.8	0.8	0.8	0.6	2.0	
Semitool	15.0	13.7	12.6	15.5	11.8	
Shimada	0.4	0.2	0.3	0.2	0.2	
S&K Products Internat.	4.6	4.1	4.4	5.0	5.9	
Sugai	1.1	0.9	1.2	1.4	1.9	
Verteq	2.5	2.7	3.4	3.3	5.3	
Others	0.6	0.4	0.5	0.3	0.5	
Total Rinser/Dryers	32.3	30.0	29.1	32.9	38.3	4.4%
Acid Processors						
Athens	0	0	0	1.0	4.0	
CFM Technology	0	0	0	0	1.0	
FSI International	18.0	23.4	18.1	15.0	19.4	
Poly-Flow Engineering	0	0.1	0.1	0.1	0.1	
Semitool	3.2	3.2	3.3	3.3	3.6	
Total Acid Process.	21.2	26.7	21.5	19.4	28.1	7.3%
Megasonic Cleaners						
FSI International	0.8	1.1	1.8	2.1	2.5	
Kaijo Denki	0	0	0	0.1	0.1	
Verteq	0.8	1.1	1.3	2.2	4.0	
Total Megasonics	1.6	2.2	3.1	4.4	6.6	42.5%
Total World Wet Pro.	171.7	157.2	161.9	165.0	235.1	8.2%

Source: Dataquest
July 1989
Ref: WETSHR

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Table 19

Dry Strip Company Shares
United States and Japan
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Dry Strip Market	44.6	38.5	34.4	51.7	89.5	19.0%
United States						
Alcan Tech	0	0	0	0	0	
Branson/IPC	10.0	7.5	5.0	3.8	8.0	
Chemitronics	0	0	0	0	0	
Drytek	3.0	2.0	1.0	0.8	0.8	
E.T. Electrotech	0	0	0	0	0	
Gasonics	0	0	0.7	1.6	2.1	
Hitachi	0	0	0	0	0	
Hohkoh Sangyo	0	0	0	0	0	
LFE	3.0	2.0	1.0	1.0	0.8	
Machine Technology	0	0.3	2.0	2.0	3.0	
Matrix	0	0	2.1	4.5	4.7	
Plasma Systems	0	0	0	0	0	
Ramco	0	0	0	0	0	
Tegal	6.0	2.0	2.0	1.2	1.0	
Tokyo Ohka	0	0	0	0	0	
Total United States	22.0	13.8	13.8	14.9	20.4	(1.9%)
Japan						
Alcan Tech	0	0	0.9	5.0	9.2	
Branson/IPC	3.0	1.8	1.2	1.4	1.0	
Chemitronics	0	0	0	0	1.4	
Drytek	0	0	0	0	0	
E.T. Electrotech	0	0	0	0	0	
Gasonics	0	0	0	0	0	
Hitachi	0	0	0	0.7	4.6	
Hohkoh Sangyo	0.4	1.1	0.5	0.6	0	
LFE	0	0	0	0	0	
Machine Technology	0	0	0	0.7	1.5	
Matrix	0	0	0	0.2	0.5	
Plasma Systems	4.2	3.2	3.3	4.3	10.4	
Ramco	0	1.7	4.5	8.7	9.6	
Tegal	0	0	0	0	0	
Tokyo Ohka	8.0	8.9	5.2	8.7	19.9	
Total Japan	15.6	16.7	15.6	30.3	58.1	38.9%

Source: Dataquest
July 1989
Ref: DSTRPSHR

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Table 20

Dry Strip Company Shares
Europe and ROW
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Dry Strip Market	44.6	38.5	34.4	51.7	89.5	19.0%
Europe						
Alcan Tech	0	0	0	0	0	
Branson/IPC	2.0	3.0	3.0	1.4	2.0	
Chemitronics	0	0	0	0	0	
Drytek	0	0	0	0	0	
E.T. Electrotech	1.0	1.0	0	0	0	
Gasonics	0	0	0	0.4	0.6	
Hitachi	0	0	0	0	0	
Hohkoh Sangyo	0	0	0	0	0	
LFE	0	0	0	0	0.5	
Machine Technology	0	0	0	0	0	
Matrix	0	0	0	0.1	0.6	
Plasma Systems	0	0	0	0	0	
Ramco	0	0	0	0	0	
Tegal	2.0	1.0	0	0	0	
Tokyo Ohka	0	0	0	0	0	
Total Europe	5.0	5.0	3.0	1.9	3.7	(7.3%)
Rest of World						
Alcan Tech	0	0	0	0	0	
Branson/IPC	2.0	2.0	1.0	1.2	4.0	
Chemitronics	0	0	0	0	0	
Drytek	0	1.0	1.0	0.2	0.4	
E.T. Electrotech	0	0	0	0	0	
Gasonics	0	0	0	0	0.3	
Hitachi	0	0	0	0	0	
Hohkoh Sangyo	0	0	0	0	0	
LFE	0	0	0	0	0.2	
Machine Technology	0	0	0	0	0	
Matrix	0	0	0	0.4	1.4	
Plasma Systems	0	0	0	1.1	0	
Ramco	0	0	0	0	0	
Tegal	0	0	0	1.2	1.0	
Tokyo Ohka	0	0	0	0.5	0	
Total Rest of World	2.0	3.0	2.0	4.6	7.3	38.2%

Source: Dataquest
July 1989
Ref: DSTRPSHR

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Table 21

Dry Strip Company Shares
Worldwide
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Dry Strip Market	44.6	38.5	34.4	51.7	89.5	19.0%
Worldwide						
Alcan Tech	0	0	0.9	5.0	9.2	
Branson/IPC	17.0	14.3	10.2	7.8	15.0	
Chemitronics	0	0	0	0	1.4	
Drytek	3.0	3.0	2.0	1.0	1.2	
E.T. Electrotech	1.0	1.0	0	0	0	
Gasonics	0	0	0.7	2.0	3.0	
Hitachi	0	0	0	0.7	4.6	
Hohkoh Sangyo	0.4	1.1	0.5	0.6	0	
LFE	3.0	2.0	1.0	1.0	1.5	
Machine Technology	0	0.3	2.0	2.7	4.5	
Matrix	0	0	2.1	5.2	7.2	
Plasma Systems	4.2	3.2	3.3	5.4	10.4	
Ramco	0	1.7	4.5	8.7	9.6	
Tegal	8.0	3.0	2.0	2.4	2.0	
Tokyo Ohka	8.0	8.9	5.2	9.2	19.9	
Total Worldwide	44.6	38.5	34.4	51.7	89.5	19.0%

Source: Dataquest
July 1989
Ref: DSTRPSHR

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Table 22

Dry Etch Company Shares
United States
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Dry Etch Market	298.3	299.6	237.1	307.4	547.0	16.4%
United States						
Anelva	3.0	4.0	0	0	0	
Applied Materials	45.0	44.0	35.0	48.1	72.9	
Branson/IPC	4.0	2.0	0	0	0	
Drytek	22.0	20.0	10.0	11.0	23.0	
Elionix	0	0	0	0	0	
Ergo Plasma Systems	0	0	0	0	0	
E.T. Electrotech	4.0	3.0	1.0	1.0	4.2	
GCA	0	0.4	1.2	3.0	4.0	
Hitachi	0	0	0	0	0	
Kokusai	1.0	1.0	0	0	0	
Lam Research	23.0	25.0	16.0	20.0	29.0	
Materials Research	0.9	2.6	2.4	2.5	6.0	
Perkin-Elmer	12.0	11.0	6.0	0	0	
Plasma Systems	0	0	0	0	0	
Plasma-Therm	10.0	8.0	8.5	11.4	10.2	
Sumitomo Metals	0	0	0	0	0	
Tegal	24.0	16.0	16.0	20.0	25.1	
Tokyo Electron Ltd.	0	0	0	0	0	
Tokuda	3.0	3.0	0	1.1	2.5	
Tokyo Ohka	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian/Zylin	14.0	8.0	4.0	0	0	
Total United States	165.9	148.0	100.1	118.1	176.9	1.6%

Source: Dataquest
July 1989
Ref: DETCHSHR

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Table 23

Dry Etch Company Shares
Japan
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Dry Etch Market	298.3	299.6	237.1	307.4	547.0	16.4%
Japan						
Anelva	24.4	34.4	16.2	22.3	41.6	
Applied Materials	19.0	17.6	21.0	24.8	76.1	
Branson/IPC	2.8	1.9	1.2	0.6	0	
Drytek	0	0	0	0	0	
Elionix	0	0	0.2	0.3	0.3	
Ergo Plasma Systems	0	0.8	0	0	0	
E.T. Electrotech	2.3	0.9	0	0	1.5	
GCA	0	0	0	0	0	
Hitachi	4.9	3.6	10.8	18.8	34.6	
Kokusai	10.5	8.4	3.3	1.4	1.5	
Lam Research	0	0	0	0	0	
Materials Research	0.2	1.0	0.8	1.0	5.0	
Perkin-Elmer	0.6	2.5	1.2	0	0	
Plasma Systems	1.5	1.5	1.7	1.9	3.2	
Plasma-Therm	0	0	1.5	1.2	1.2	
Sumitomo Metals	0	0	2.4	5.6	6.2	
Tegal	0	0	0.6	0	1.9	
Tokyo Electron Ltd.	7.4	10.5	6.0	17.4	44.6	
Tokuda	5.7	6.6	4.3	5.0	3.2	
Tokyo Ohka	8.9	7.6	7.2	7.1	10.0	
Ulvac	4.9	4.7	3.9	5.6	8.1	
Varian/Zylin	0	0	0	0	0	
Total Japan	93.1	102.0	82.3	113.0	239.0	26.6%

Source: Dataquest
July 1989
Ref: DETCHSHR

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Table 24

Dry Etch Company Shares
Europe
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Dry Etch Market	298.3	299.6	237.1	307.4	547.0	16.4%
Europe						
Anelva	0	0	0	0	0	
Applied Materials	4.0	5.0	14.0	22.0	28.3	
Branson/IPC	2.0	1.0	2.0	0	0	
Drytek	1.0	1.0	2.0	2.0	0	
Elionix	0	0	0	0	0	
Ergo Plasma Systems	0	0	0	0	0	
E.T. Electrotech	4.0	5.0	4.0	6.2	7.7	
GCA	0	0.4	0.8	1.0	1.0	
Hitachi	0	0	0	0	0	
Kokusai	0	1.0	0	0	0	
Lam Research	2.0	3.0	5.0	7.0	13.0	
Materials Research	0.3	1.2	0.9	0.9	1.5	
Perkin-Elmer	0	3.0	2.0	0	0	
Plasma Systems	0	0	0	0	0	
Plasma-Therm	2.0	4.0	1.0	0.8	1.2	
Sumitomo Metals	0	0	0	0	0	
Tegal	14.0	8.0	8.0	15.6	24.0	
Tokyo Electron Ltd.	0	0	0	0	1.2	
Tokuda	0	0	0	2.8	2.1	
Tokyo Ohka	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian/Zylin	0	0	0	0	0	
Total Europe	29.3	32.6	39.7	58.3	80.0	28.5%

Source: Dataquest
July 1989
Ref: DETCHSHR

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Table 25

Dry Etch Company Shares
Rest of World
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Dry Etch Market	298.3	299.6	237.1	307.4	547.0	16.4%
Rest of World						
Anelva	1.0	1.0	0	0	0	
Applied Materials	1.0	3.0	4.0	7.1	19.4	
Branson/IPC	0	0	1.0	1.0	0	
Drytek	1.0	2.0	4.0	4.0	2.0	
Elionix	0	0	0	0	0	
Ergo Plasma Systems	0	0	0	0	0	
E.T. Electrotech	0	0	0	0	0.7	
GCA	0	0	0	0	0	
Hitachi	0	0	0	0	0	
Kokusai	0	0	0	0	0	
Lam Research	3.0	6.0	5.0	5.0	23.0	
Materials Research	0	0	0	0	0.5	
Perkin-Elmer	3.0	3.0	0	0	0	
Plasma Systems	0	0	0	0	0	
Plasma-Therm	0	1.0	0	0.3	0.3	
Ramco	0	0	0	0	0	
Sumitomo Metals	0	0	0	0	0	
Tegal	0	1.0	1.0	0	4.0	
Tokyo Electron Ltd.	0	0	0	0	0	
Tokuda	0	0	0	0.5	1.0	
Tokyo Ohka	0	0	0	0	0	
Ulvac	0	0	0	0.1	0.2	
Varian/Zylin	1.0	0	0	0	0	
Total Rest of World	10.0	17.0	15.0	18.0	51.1	50.4%

Source: Dataquest
July 1989
Ref: DETCHSHR

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Table 26

Dry Etch Company Shares
Worldwide
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Dry Etch Market	298.3	299.6	237.1	307.4	547.0	16.4%
Worldwide						
Anelva	28.4	39.4	16.2	22.3	41.6	
Applied Materials	69.0	69.6	74.0	102.0	196.7	
Branson/IPC	8.8	4.9	4.2	1.6	0	
Drytek	24.0	23.0	16.0	17.0	25.0	
Elionix	0	0	0.2	0.3	0.3	
Ergo Plasma Systems	0	0.8	0	0	0	
E.T. Electrotech	10.3	8.9	5.0	7.2	14.1	
GCA	0	0.8	2.0	4.0	5.0	
Hitachi	4.9	3.6	10.8	18.8	34.6	
Kokusai	11.5	10.4	3.3	1.4	1.5	
Lam Research	28.0	34.0	26.0	32.0	65.0	
Materials Research	1.4	4.8	4.1	4.4	13.0	
Perkin-Elmer	15.6	19.5	9.2	0	0	
Plasma Systems	1.5	1.5	1.7	1.9	3.2	
Plasma-Therm	12.0	13.0	11.0	13.7	12.9	
Sumitomo Metals	0	0	2.4	5.6	6.2	
Tegal	38.0	25.0	25.6	35.6	55.0	
Tokyo Electron Ltd.	7.4	10.5	6.0	17.4	45.8	
Tokuda	8.7	9.6	4.3	9.4	8.8	
Tokyo Ohka	8.9	7.6	7.2	7.1	10.0	
Ulvac	4.9	4.7	3.9	5.7	8.3	
Varian/Zylin	15.0	8.0	4.0	0	0	
Total Worldwide	298.3	299.6	237.1	307.4	547.0	16.4%

Source: Dataquest
July 1989
Ref: DETCHSHR

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Table 27

Chemical Vapor Deposition Company Shares
United States
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World CVD Market	228.0	246.5	219.4	254.4	455.0	18.9%
Tube CVD						
Horizontal Tube LPCVD						
ASM	2.3	2.3	1.2	1.7	2.6	
BTU/Bruce	2.8	5.5	2.7	3.4	7.4	
Enya	0	0	0	0	0	
Kokusai	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0.3	0.4	0.5	0	0	
Process Technology	3.2	4.0	4.5	3.8	4.0	
Solitec	8.6	10.8	4.1	2.0	4.8	
Tokyo Electron Ltd.	0.4	0	0	0	0	
Tempress	4.5	5.5	2.5	0	3.0	
Thermco	4.2	3.1	2.9	3.0	3.5	
Tylan	2.0	0.6	0.4	1.0	1.5	
Ulvac/BTU	0	0	0	0	0	
Wellman	0	0	0	0	0	
Total Hor. LPCVD	28.3	32.2	18.8	14.9	26.8	(1.4%)
Vertical Tube LPCVD						
All Companies	0	0.3	0.2	1.6	2.1	
Horizontal Tube PECVD						
ASM	18.9	15.5	14.9	23.1	20.6	
Pacific Western	6.0	4.1	2.9	3.7	2.7	
Total Hor. PECVD	24.9	19.6	17.8	26.8	23.3	(1.6%)
Total Tube CVD	53.2	52.1	36.8	43.3	52.2	(0.5%)

(Continued)

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Table 27 (Continued)

Chemical Vapor Deposition Company Shares
United States
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Nontube CVD Reactors						
APCVD Reactors						
Amaya	0	0	0	0	0	
App. Mat. (2100)	3.1	1.8	1.2	3.0	3.0	
Hitachi	0	0	0	0	0	
Kokusai	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0.7	0.6	0.4	0	0	
Tempress	2.5	1.4	1.3	0	0.5	
Toshiba Machine	0	0	0	0	0	
Watkins-Johnson	3.3	3.4	5.6	7.3	10.5	
Total APCVD Reactors	9.6	7.2	8.5	10.3	14.0	9.9%
LPCVD Reactors						
Anelva	0	0	0	0	0	
Focus Semiconductor	0	0	0	1.0	1.6	
Genus	7.2	6.7	4.2	7.1	11.7	
Spectrum CVD	0	0	0.5	2.3	4.0	
SVG (Anicon)	9.4	6.7	3.3	1.4	1.5	
Ulvac	0	0	0	0	0	
Varian	0	0	1.1	2.5	4.3	
Total LPCVD Reactors	16.6	13.4	9.1	14.3	23.1	8.6%
PECVD Reactors						
Anelva	0	0	0	0	0	
App. Mat. (3300/5000)	2.3	2.3	1.4	16.3	37.0	
Enya	0	0	0	0	0	
E.T. Electrotech	2.0	3.7	4.1	1.0	4.2	
Japan Production	0	0	0	0	0	
Novellus	0	0	0	3.1	16.9	
Plasma-Therm	4.5	3.8	3.0	3.8	4.0	
Ulvac	0	0	0	0	0.6	
Total PECVD Reactors	8.8	9.8	8.5	24.2	62.7	63.4%
Total Nontube CVD	35.0	30.4	26.1	48.8	99.8	29.9%
Total U.S. CVD	88.2	82.5	62.9	92.1	152.0	14.6%

Source: Dataquest
July 1989
Ref: CVDSHR

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Table 28

Chemical Vapor Deposition Company Shares
Japan
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World CVD Market	228.0	246.5	219.4	254.4	455.0	18.9%
Tube CVD						
Horizontal Tube LPCVD						
ASM	2.2	4.5	4.8	2.0	3.9	
BTU/Bruce	0	0.5	0	0	0	
Enya	2.9	1.3	1.0	0.6	1.8	
Kokusai	16.9	14.6	16.2	8.3	5.0	
Koyo Lindberg	1.7	1.9	1.8	1.0	1.8	
Pacific Western	0	0	0	0	0	
Process Technology	0	0	0	0	0	
Solitec	0	0	0	0	0	
Tokyo Electron Ltd.	11.2	15.0	6.6	7.6	12.3	
Tempress	0.3	0.1	0	0	0	
Thermco	0	0	0	0	0	
Tylan	0	0	0	0	0	
Ulvac/BTU	0	0	0	0.5	1.0	
Wellman	0	0	0	0	0	
Total Hor. LPCVD	35.2	37.9	30.4	20.0	25.8	(7.5%)
Vertical Tube LPCVD						
All Companies	0	2.3	6.0	7.3	18.4	
Horizontal Tube PECVD						
ASM	9.2	15.7	16.4	9.8	15.5	
Pacific Western	5.7	3.8	2.7	2.8	2.1	
Total Hor. PECVD	14.9	19.5	19.1	12.6	17.6	4.3%
Total Tube CVD	50.1	59.7	55.5	39.9	61.8	5.4%

(Continued)

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Table 28 (Continued)

Chemical Vapor Deposition Company Shares
Japan
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Nontube CVD Reactors						
APCVD Reactors						
Amaya	13.7	10.9	6.0	5.5	17.5	
App. Mat. (2100)	7.8	6.3	5.4	4.2	8.7	
Hitachi	0.6	0.3	0.4	0	0.2	
Kokusai	1.5	0.7	0.7	0	0	
Koyo Lindberg	1.5	0.6	0.4	0.2	1.3	
Pacific Western	0.7	0.5	0.4	0.2	0	
Tempress	0.4	0.2	0.3	0	0.5	
Toshiba Machine	0	0	4.3	5.0	8.3	
Watkins-Johnson	0.7	1.0	0.5	2.0	15.0	
Total APCVD Reactors	26.9	20.5	18.4	17.1	51.5	
LPCVD Reactors						
Anelva	0	0	0	0.7	2.3	
Focus Semiconductor	0	0	0	0	0.9	
Genus	7.2	8.0	1.1	3.3	12.7	
Spectrum CVD	0	0	0	0	1.5	
SVG (Anicon)	3.3	4.9	2.0	0.8	1.5	
Ulvac	0	0	1.2	1.4	3.8	
Varian	0	0	0	2.0	4.5	
Total LPCVD Reactors	10.5	12.9	4.3	8.2	27.2	26.9%
PECVD Reactors						
Anelva	0	0	0.6	1.0	0	
App. Mat. (3300/5000)	4.8	1.7	3.4	10.0	25.0	
Enya	5.1	4.2	1.6	1.9	4.2	
E.T. Electrotech	1.2	2.4	0.7	5.2	4.9	
Japan Production	5.5	5.9	6.0	4.5	6.5	
Novellus	0	0	0	0.5	3.4	
Plasma-Therm	0	0	1.2	0.3	0.5	
Ulvac	2.7	2.9	3.0	2.8	3.8	
Total PECVD Reactors	19.3	17.1	16.5	26.2	48.3	25.8%
Total Nontube CVD	56.7	50.5	39.2	51.5	127.0	22.3%
Total Japan CVD	106.8	110.2	94.7	91.4	188.8	15.3%

Source: Dataquest
July 1989
Ref: CVDSHR

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Table 29

Chemical Vapor Deposition Company Shares
Europe
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World CVD Market	228.0	246.5	219.4	254.4	455.0	18.9%
Tube CVD						
Horizontal Tube LPCVD						
ASM	3.5	5.5	13.3	16.2	16.7	
BTU/Bruce	0.4	0.3	2.9	3.0	3.5	
Enya	0	0	0	0	0	
Kokusai	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0	0	0	0	0	
Process Technology	1.2	1.6	0.7	0.5	0	
Solitec	0.6	1.4	0.6	0.3	1.6	
Tokyo Electron Ltd.	0	0	0	0	1.4	
Tempress	0.2	0.6	0.6	0	0.8	
Thermco	3.0	4.4	2.1	2.2	1.0	
Tylan	0	0.2	0.3	2.0	0	
Ulvac/BTU	0	0	0	0	0	
Wellman	0	0	0	0	1.0	
Total Hor. LPCVD	8.9	14.0	20.5	24.2	26.0	30.7%
Vertical Tube PECVD						
All Companies	0	0	0	0	0.8	
Horizontal Tube PECVD						
ASM	3.7	6.2	9.8	5.8	10.3	
Pacific Western	0.8	0.8	1.3	1.4	0.9	
Total Hor. PECVD	4.5	7.0	11.1	7.2	11.2	25.6%
Total Tube CVD	13.4	21.0	31.6	31.4	38.0	29.8%

(Continued)

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Table 29 (Continued)

Chemical Vapor Deposition Company Shares
Europe
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Nontube CVD Reactors						
APCVD Reactors						
Amaya	0	0	0	0	0	
App. Mat. (2100)	0.7	0.9	0.7	1.4	3.0	
Hitachi	0	0	0	0	0	
Kokusai	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0.2	0.3	0.4	0	0	
Tempress	0.5	0.4	0.5	0	0.3	
Toshiba Machine	0	0	0	0	0	
Watkins-Johnson	0.4	0	0.4	6.7	6.0	
Total APCVD Reactors	1.8	1.6	2.0	8.1	9.3	50.8%
LPCVD Reactors						
Anelva	0	0	0	0	0	
Focus Semiconductor	0	0	0	0	0	
Genus	0.8	1.4	1.1	1.7	3.7	
Spectrum CVD	0	0	0	0	2.0	
SVG (Anicon)	3.5	3.0	2.5	1.1	0.5	
Ulvac	0	0	0	0	0	
Varian	0	0	0	1.5	2.3	
Total LPCVD Reactors	4.3	4.4	3.6	4.3	8.5	18.6%
PECVD Reactors						
Anelva	0	0	0	0	0	
App. Mat. (3300/5000)	0.6	1.3	0.7	3.9	8.9	
Enya	0	0	0	0	0	
E.T. Electrotech	2.8	6.5	8.5	7.1	9.8	
Japan Production	0	0	0	0	0	
Novellus	0	0	0	0	1.1	
Plasma-Therm	0.7	1.0	0.8	0.5	1.0	
Ulvac	0	0	0	0	0	
Total PECVD Reactors	4.1	8.8	10.0	11.5	20.8	50.1%
Total Nontube CVD	10.2	14.8	15.6	23.9	38.6	39.5%
Total Europe CVD	23.6	35.8	47.2	55.3	76.6	34.2%

Source: Dataquest
July 1989
Ref: CVDSHR

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Table 30

Chemical Vapor Deposition Company Shares
Rest of World
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World CVD Market	228.0	246.5	219.4	254.4	455.0	18.9%
Tube CVD						
Horizontal Tube LPCVD						
ASM	0.7	1.6	0.7	0	2.6	
BTU/Bruce	0.8	0.4	0	1.5	3.6	
Enya	0	0	0	0	0	
Kokusai	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0	0	0	0	0	
Process Technology	0	0.1	0.2	0	0	
Solitec	0.2	0.7	0.6	1.3	1.6	
Tokyo Electron Ltd.	1.2	0	0	0	0	
Tempress	0.9	1.4	0.7	0	0	
Thermco	0.5	1.6	1.4	1.4	2.0	
Tylan	0	1.5	0	1.0	0	
Ulvac/BTU	0	0	0	0	0	
Wellman	0	0	0	0	0	
Total Hor. LPCVD	4.3	7.3	3.6	5.2	9.8	22.9%
Vertical Tube LPCVD						
All Companies	0	0	0	0	0.4	
Horizontal Tube PECVD						
ASM	1.3	3.0	3.3	5.8	5.2	
Pacific Western	0	0	0	0	0.5	
Total Hor. PECVD	1.3	3.0	3.3	5.8	5.7	44.7%
Total Tube CVD	5.6	10.3	6.9	11.0	15.9	29.8%

(Continued)

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Table 30 (Continued)

Chemical Vapor Deposition Company Shares
Rest of World
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Nontube CVD Reactors						
APCVD Reactors						
Amaya	0	0	0	0	0	
App. Mat. (2100)	0.3	0.9	0.5	0	1.0	
Hitachi	0	0	0	0	0	
Kokusai	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0	0	0	0	0	
Tempress	0.2	0.1	0.1	0	0.5	
Toshiba Machine	0	0	0	0	0	
Watkins-Johnson	0.4	1.5	1.6	0	4.5	
Total APCVD Reactors	0.9	2.5	2.2	0	6.0	60.7%
LPCVD Reactors						
Anelva	0	0	0	0	0	
Focus Semiconductor	0	0	0	0	0	
Genus	0.8	1.4	1.1	1.1	5.3	
Spectrum CVD	0	0	0	0	0.5	
SVG (Anicon)	0.6	1.0	1.0	0.4	0.5	
Ulvac	0	0	0	0	0	
Varian	0	0	0	1.5	0.7	
Total LPCVD Reactors	1.4	2.4	2.1	3.0	7.0	49.5%
PECVD Reactors						
Anelva	0	0	0	0	0	
App. Mat. (3300/5000)	0.6	1.0	0.6	1.6	4.5	
Enya	0	0	0	0	0	
E.T. Electrotech	0.4	1.0	2.0	0	1.4	
Japan Production	0	0	0	0	0	
Novellus	0	0	0	0	2.3	
Plasma-Therm	0.5	0.8	0.8	0	0.5	
Ulvac	0	0	0	0	0	
Total PECVD Reactors	1.5	2.8	3.4	1.6	8.7	55.2%
Total Nontube CVD	3.8	7.7	7.7	4.6	21.7	54.6%
Total ROW CVD	9.4	18.0	14.6	15.6	37.6	41.4%

Source: Dataquest
July 1989
Ref: CVDSHR

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Table 31

Chemical Vapor Deposition Company Shares
Worldwide
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World CVD Market	228.0	246.5	219.4	254.4	455.0	18.9%
Tube CVD						
Horizontal Tube LPCVD						
ASM	8.7	13.9	20.0	19.9	25.8	
BTU/Bruce	4.0	6.7	5.6	7.9	14.5	
Enya	2.9	1.3	1.0	0.6	1.8	
Kokusai	16.9	14.6	16.2	8.3	5.0	
Koyo Lindberg	1.7	1.9	1.8	1.0	1.8	
Pacific Western	0.3	0.4	0.5	0	0	
Process Technology	4.4	5.7	5.4	4.3	4.0	
Solitec	9.4	12.9	5.3	3.6	8.0	
Tokyo Electron Ltd.	12.8	15.0	6.6	7.6	13.7	
Tempress	5.9	7.6	3.8	0	3.8	
Thermco	7.7	9.1	6.4	6.6	6.5	
Tylan	2.0	2.3	0.7	4.0	1.5	
Ulvac/BTU	0	0	0	0.5	1.0	
Wellman	0	0	0	0	1.0	
Total Hor. LPCVD	76.7	91.4	73.3	64.3	88.4	3.6%
Vertical Tube LPCVD						
All Companies	0	2.6	6.2	8.9	21.7	
Horizontal Tube PECVD						
ASM	33.1	40.4	44.4	44.5	51.6	
Pacific Western	12.5	8.7	6.9	7.9	6.2	
Total Hor. PECVD	45.6	49.1	51.3	52.4	57.8	6.1%
Total Tube CVD	122.3	143.1	130.8	125.6	167.9	8.2%

(Continued)

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Table 31 (Continued)

Chemical Vapor Deposition Company Shares
Worldwide
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Nontube CVD Reactors						
APCVD Reactors						
Amaya	13.7	10.9	6.0	5.5	17.5	
App. Mat. (2100)	11.9	9.9	7.8	8.6	15.7	
Hitachi	0.6	0.3	0.4	0	0.2	
Kokusai	1.5	0.7	0.7	0	0	
Koyo Lindberg	1.5	0.6	0.4	0.2	1.3	
Pacific Western	1.6	1.4	1.2	0.2	0	
Tempress	3.6	2.1	2.2	0	1.8	
Toshiba Machine	0	0	4.3	5.0	8.3	
Watkins-Johnson	4.8	5.9	8.1	16.0	36.0	
Total APCVD Reactors	39.2	31.8	31.1	35.5	80.8	19.8%
LPCVD Reactors						
Anelva	0	0	0	0.7	2.3	
Focus Semiconductor	0	0	0	1.0	2.5	
Genus	16.0	17.5	7.5	13.2	33.4	
Spectrum CVD	0	0	0.5	2.3	8.0	
SVG (Anicon)	16.8	15.6	8.8	3.7	4.0	
Ulvac	0	0	1.2	1.4	3.8	
Varian	0	0	1.1	7.5	11.8	
Total LPCVD Reactors	32.8	33.1	19.1	29.8	65.8	19.0%
PECVD Reactors						
Anelva	0	0	0.6	1.0	0	
App. Mat. (3300/5000)	8.3	6.3	6.1	31.8	75.4	
Enya	5.1	4.2	1.6	1.9	4.2	
E.T. Electrotech	6.4	13.6	15.3	13.3	20.3	
Japan Production	5.5	5.9	6.0	4.5	6.5	
Novellus	0	0	0	3.6	23.7	
Plasma-Therm	5.7	5.6	5.8	4.6	6.0	
Ulvac	2.7	2.9	3.0	2.8	4.4	
Total PECVD Reactors	33.7	38.5	38.4	63.5	140.5	42.9%
Total Nontube CVD	105.7	103.4	88.6	128.8	287.1	28.4%
Total Worldwide CVD	228.0	246.5	219.4	254.4	455.0	18.9%

Source: Dataquest
July 1989
Ref: CVDSHR

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Table 32

Physical Vapor Deposition Company Shares
United States
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World PVD Market	233.5	263.0	236.6	249.0	314.7	7.7%
Sputtering						
Anelva	1.2	3.0	2.6	10.0	20.0	
Balzers	5.9	4.0	5.6	5.0	5.0	
CHA Industries	0.3	1.0	0.7	0.3	0.7	
Circuits Processing	3.0	4.5	2.0	2.0	2.6	
CVC Products	6.0	7.0	10.0	6.8	7.5	
Edwards High Vacuum	0	0	0	0	0	
E.T. Electrotech	1.7	3.1	1.3	1.4	1.8	
Innotec	0.4	1.8	1.8	2.4	4.2	
Ion Tech	0.3	0.5	0.5	0.7	0.5	
Kurt J. Lesker	0.9	0.8	0.8	0.8	0.8	
Leybold-Heraeus	0.9	3.8	2.8	6.0	6.0	
Materials Research	20.0	24.0	15.0	13.0	15.0	
Perkin-Elmer	6.7	4.0	3.3	2.1	0.9	
Sputtered Films	2.0	1.0	1.3	1.0	0.6	
Temescal	1.0	1.3	1.3	0	0	
Tokuda	0	0	0	0	0	
Ulvac	1.5	0.5	1.5	6.3	6.4	
Varian	23.9	32.8	25.6	21.3	24.6	
Others	0	0.1	1.0	3.1	5.1	
Total Sputtering	75.7	93.2	77.1	82.2	101.7	7.7%
Evaporation						
Anelva	0	0.4	2.3	1.8	1.4	
Balzers	4.5	4.0	1.8	1.1	1.1	
CHA Industries	5.7	7.1	5.6	6.0	6.3	
CVC Products	0	0	0	0	1.0	
Edwards High Vacuum	0	0	0	0	0	
Innotec	0.3	0.3	0.2	0	1.0	
Kurt J. Lesker	0.2	0.5	0.3	0.3	0.3	
Leybold-Heraeus	2.5	1.5	1.0	0.5	0.5	
Temescal	2.8	5.5	5.7	5.1	4.5	
Ulvac	0	0.8	1.0	1.4	1.5	
Others	0	0.1	0.2	0.2	0.2	
Total Evaporation	16.0	20.2	18.1	16.4	17.8	2.7%
Total U.S. PVD	91.7	113.4	95.2	98.6	119.5	6.8%

Source: Dataquest
July 1989
Ref: PVDSHR

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Table 33

Physical Vapor Deposition Company Shares
Japan
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World PVD Market	233.5	263.0	236.6	249.0	314.7	7.7%
Sputtering						
Anelva	25.3	27.3	18.0	29.9	42.3	
Balzers	0	0	0	0	0	
CHA Industries	0	0	0	0	0	
Circuits Processing	0	0	0.9	1.0	0	
CVC Products	0	0	0	0	0.3	
Edwards High Vacuum	0	0	0	0	0	
E.T. Electrotech	1.3	1.7	0.5	0.6	0.6	
Innotec	0	0.8	0	0	0	
Ion Tech	0.2	0.3	0.2	0	0	
Kurt J. Lesker	0	0	0	0	0	
Leybold-Heraeus	0	0	0	0	0	
Materials Research	10.0	5.5	0.9	1.9	7.5	
Perkin-Elmer	3.8	3.8	0	0	0	
Sputtered Films	0	0	0	0	0	
Temescal	0	0	0	0	0	
Tokuda	5.1	5.0	3.3	11.1	7.0	
Ulvac	14.3	16.4	14.7	24.7	40.1	
Varian	19.8	14.9	16.8	12.6	18.7	
Others	0	0	0	0	0	
Total Sputtering	79.8	75.7	55.3	81.8	116.5	9.9%
Evaporation						
Anelva	1.4	0	0	0	0	
Balzers	0.6	0.8	0.4	0	0	
CHA Industries	0	0	0	0	0	
CVC Products	0	0	0	0	0	
Edwards High Vacuum	0	0	0	0	0	
Innotec	0	0	0	0	0	
Kurt J. Lesker	0	0	0	0	0	
Leybold-Heraeus	0	0	0	0	0	
Temescal	0.8	1.4	1.8	2.4	2.4	
Ulvac	16.9	16.0	19.0	5.9	11.5	
Others	0	0	0	0	0	
Total Evaporation	19.7	18.2	21.2	8.3	13.9	(8.3%)
Total Japan PVD	99.5	93.9	76.5	90.1	130.4	7.0%

Source: Dataquest
July 1989
Ref: PVDSHR

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Table 34

Physical Vapor Deposition Company Shares
Europe
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World PVD Market	233.5	263.0	236.6	249.0	314.7	7.7%
Sputtering						
Anelva	0	0	0	0	0	
Balzers	6.3	6.1	7.6	8.9	6.0	
CHA Industries	0	0	0	0	0	
Circuits Processing	0	0	0	0	0	
CVC Products	2.1	2.5	3.5	2.9	3.5	
Edwards High Vacuum	0	0	0	0	0	
E.T. Electrotech	2.5	3.9	3.5	4.0	6.0	
Innotec	0	0	0	0	0	
Ion Tech	0	0	0	0	0	
Kurt J. Lesker	0	0	0	0	0	
Leybold-Heraeus	3.0	5.0	6.0	7.0	4.8	
Materials Research	4.8	6.4	3.5	4.0	4.0	
Perkin-Elmer	1.5	1.0	1.0	0.3	0	
Sputtered Films	0	0	0	0	0	
Temescal	0.8	0.8	0	0	0	
Tokuda	0	0	0	0	0	
Ulvac	1.4	3.3	4.6	2.0	1.2	
Varian	3.7	4.6	8.3	6.3	6.0	
Others	0	0	0	0	0	
Total Sputtering	26.1	33.6	38.0	35.4	31.5	4.8%
Evaporation						
Anelva	0	0	0	0	0	
Balzers	3.9	5.6	2.8	1.8	1.8	
CHA Industries	0	0	0	0	0	
CVC Products	0	0	0	0	0.6	
Edwards High Vacuum	0	0	0	0	0	
Innotec	0	0	0	0	0	
Kurt J. Lesker	0	0	0	0	0	
Leybold-Heraeus	2.5	2.5	2.0	1.0	0	
Temescal	2.8	3.3	3.0	2.4	1.8	
Ulvac	0	0	2.4	0.1	0.3	
Others	0	0	0	0	0	
Total Evaporation	9.2	11.4	10.2	5.3	4.5	(16.4%)
Total Europe PVD	35.3	45.0	48.2	40.7	36.0	(0.5%)

Source: Dataquest
July 1989
Ref: PVDSHR

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Table 35

Physical Vapor Deposition Company Shares
Rest of World
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World PVD Market	233.5	263.0	236.6	249.0	314.7	7.7%
Sputtering						
Anelva	0.5	0.5	1.2	3.0	6.0	
Balzers	0	0	0	0	0	
CHA Industries	0	0	0	0	0	
Circuits Processing	0	0	0	0	0	
CVC Products	0	0	0	0	1.0	
Edwards High Vacuum	0	0	0	0	0	
E.T. Electrotech	0	0	0	0	0.6	
Innotec	0	0	0	0	0	
Ion Tech	0	0	0	0	0	
Kurt J. Lesker	0	0	0	0	0	
Leybold-Heraeus	0	0	0.8	2.0	0	
Materials Research	0	1.9	2.5	4.2	7.5	
Perkin-Elmer	0.8	1.1	1.3	0.7	0	
Sputtered Films	0	0	0.3	0	0	
Temescal	0	0	0	0	0	
Tokuda	0	0	0	0	0	
Ulvac	1.0	2.4	4.6	1.0	1.0	
Varian	4.7	4.8	6.0	8.1	12.0	
Others	0	0	0	0	0	
Total Sputtering	7.0	10.7	16.7	19.0	28.1	41.5%
Evaporation						
Anelva	0	0	0	0	0	
Balzers	0	0	0	0	0	
CHA Industries	0	0	0	0	0	
CVC Products	0	0	0	0	0	
Edwards High Vacuum	0	0	0	0	0	
Innotec	0	0	0	0	0	
Kurt J. Lesker	0	0	0	0	0	
Leybold-Heraeus	0	0	0	0	0	
Temescal	0	0	0	0	0	
Ulvac	0	0	0	0.6	0.7	
Others	0	0	0	0	0	
Total Evaporation	0	0	0	0.6	0.7	N/A
Total ROW PVD	7.0	10.7	16.7	19.6	28.8	42.4%

N/A = Not Available

Source: Dataquest
July 1989
Ref: PVDSHR

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Table 36

Physical Vapor Deposition Company Shares
Worldwide
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World PVD Market	233.5	263.0	236.6	249.0	314.7	7.7%
Sputtering						
Anelva	27.0	30.8	21.8	42.9	68.3	
Balzers	12.2	10.1	13.2	13.9	11.0	
CHA Industries	0.3	1.0	0.7	0.3	0.7	
Circuits Processing	3.0	4.5	2.9	3.0	2.6	
CVC Products	8.1	9.5	13.5	9.7	12.3	
Edwards High Vacuum	0	0	0	0	0	
E.T. Electrotech	5.5	8.7	5.3	6.0	9.0	
Innotec	0.4	2.6	1.8	2.4	4.2	
Ion Tech	0.5	0.8	0.7	0.7	0.5	
Kurt J. Lesker	0.9	0.8	0.8	0.8	0.8	
Leybold-Heraeus	3.9	8.8	9.6	15.0	10.8	
Materials Research	34.8	37.8	21.9	23.1	34.0	
Perkin-Elmer	12.8	9.9	5.6	3.1	0.9	
Sputtered Films	2.0	1.0	1.6	1.0	0.6	
Temescal	1.8	2.1	1.3	0	0	
Tokuda	5.1	5.0	3.3	11.1	7.0	
Ulvac	18.2	22.6	25.4	34.0	48.7	
Varian	52.1	57.1	56.7	48.3	61.3	
Others	0	0.1	1.0	3.1	5.1	
Total Sputtering	188.6	213.2	187.1	218.4	277.8	10.2%
Evaporation						
Anelva	1.4	0.4	2.3	1.8	1.4	
Balzers	9.0	10.4	5.0	2.9	2.9	
CHA Industries	5.7	7.1	5.6	6.0	6.3	
CVC Products	0	0	0	0	1.6	
Edwards High Vacuum	0	0	0	0	0	
Innotec	0.3	0.3	0.2	0	1.0	
Kurt J. Lesker	0.2	0.5	0.3	0.3	0.3	
Leybold-Heraeus	5.0	4.0	3.0	1.5	0.5	
Temescal	6.4	10.2	10.5	9.9	8.7	
Ulvac	16.9	16.8	22.4	8.0	14.0	
Others	0	0.1	0.2	0.2	0.2	
Total Evaporation	44.9	49.8	49.5	30.6	36.9	(4.8%)
Total Worldwide PVD	233.5	263.0	236.6	249.0	314.7	7.7%

Source: Dataquest
July 1989
Ref: PVDSHR

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Table 37

Silicon Epitaxy Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Total Epitaxy Market	111.8	71.5	46.3	35.5	84.5	(6.8%)
United States						
Applied Materials	33.7	18.7	12.2	6.4	25.5	
ASM Epitaxy	0	0	0	0	1.5	
Kokusai	0	0	0	0	0	
Lam Research (Gemini)	10.0	8.6	4.0	7.0	15.0	
LPE	0	0	0	0	0	
Shimada	0	0	0	0	0	
Sitesa	0	0	0	0	0	
Toshiba	0	0	0	0	0	
Total United States	43.7	27.3	16.2	13.4	42.0	(1.0%)
Japan						
Applied Materials	25.3	14.3	8.1	8.0	16.5	
ASM Epitaxy	0	0	0	0	0.8	
Kokusai	6.3	5.0	2.1	1.5	4.2	
Lam Research (Gemini)	13.9	3.8	1.8	2.9	0	
LPE	0	0	0	0	0	
Shimada	2.5	0.8	0.5	0	0	
Sitesa	0	0	0	0	0	
Toshiba	2.1	2.3	1.0	0.6	2.0	
Total Japan	50.1	26.2	13.5	13.0	23.5	(17.2%)
Europe						
Applied Materials	8.0	8.0	8.0	3.6	4.4	
ASM Epitaxy	0	0	0	0	0.8	
Kokusai	0	0	0	0	0	
Lam Research (Gemini)	5.0	5.0	3.2	2.8	1.0	
LPE	0	0	0	0	4.5	
Shimada	0	0	0	0	0	
Sitesa	0	0	0	0	4.5	
Toshiba	0	0	0	0	0	
Total Europe	13.0	13.0	11.2	6.4	15.2	4.0%

(Continued)

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Table 37 (Continued)

Silicon Epitaxy Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Rest of World						
Applied Materials	3.0	3.0	3.0	0.6	0.8	
ASM Epitaxy	0	0	0	0	0	
Kokusai	0	0	0	0	0	
Lam Research (Gemini)	2.0	2.0	2.4	2.1	3.0	
LPE	0	0	0	0	0	
Shimada	0	0	0	0	0	
Sitesa	0	0	0	0	0	
Toshiba	0	0	0	0	0	
Total Rest of World	5.0	5.0	5.4	2.7	3.8	(6.6%)
Worldwide						
Applied Materials	70.0	44.0	31.3	18.6	47.2	
ASM Epitaxy	0	0	0	0	3.1	
Kokusai	6.3	5.0	2.1	1.5	4.2	
Lam Research (Gemini)	30.9	19.4	11.4	14.8	19.0	
LPE	0	0	0	0	4.5	
Shimada	2.5	0.8	0.5	0	0	
Sitesa	0	0	0	0	4.5	
Toshiba	2.1	2.3	1.0	0.6	2.0	
Total Worldwide	111.8	71.5	46.3	35.5	84.5	(6.8%)

Source: Dataquest
July 1989
Ref: EPISHR

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Table 38

Metalorganic CVD Company Shares
United States and Japan
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World MOCVD Market	17.5	24.8	32.1	35.6	42.5	24.8%
United States						
Aixtron	0	0	0	0	0	
Cambridge Instruments	1.9	1.9	1.1	1.5	1.3	
Crystal Specialties	1.2	1.8	2.2	1.7	2.3	
CVD Equipment	1.2	1.5	0.6	1.2	1.0	
CVT	0.5	0	0	0	0	
Daiwa Semiconductor	0	0	0	0	0	
EEV	0	0	0.2	0	0	
Emcore	0	0.1	2.3	5.1	6.5	
Nippon EMC	0	0	0	0	0	
Nippon Sanso	0	0	0	0	0	
Samco	0	0	0	0	0	
Seiden	0	0	0	0	0	
Semco Engineering	0	0	0	0	0	
Shimada Rika	0	0	0	0	0	
Spire	0.8	3.0	2.9	1.3	1.5	
TEL/Thermco	0	0	0	0	0	
Thomas Schwonn	0.5	0.6	0	0	0.4	
Toyoko Chemical	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Total United States	6.1	8.9	9.3	10.8	13.0	20.8%
Japan						
Aixtron	0	0	0	0	0	
Cambridge Instruments	0	0.3	0.4	0	0	
Crystal Specialties	0	0	0.5	0.9	0.4	
CVD Equipment	0	0	0	0	0	
CVT	0	0	0	0	0	
Daiwa Semiconductor	0	0	0.4	0.4	0.5	
EEV	0	0	0	0	0	
Emcore	0	0	0	0	0.5	
Nippon EMC	0.8	1.1	1.5	1.4	1.9	

(Continued)

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Table 38 (Continued)

Metalorganic CVD Company Shares
United States and Japan
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Japan (Continued)						
Nippon Sanso	2.3	3.6	4.6	4.9	6.5	
Samco	1.1	0.7	1.0	1.1	1.2	
Seiden	1.3	0.9	1.3	0.6	0.6	
Semco Engineering	0	0	0	0	0	
Shimada Rika	0	0	0.3	0	0	
Spire	0	0	0	0	0.6	
TEL/Thermco	2.3	2.3	3.0	2.9	1.7	
Thomas Schwonn	0	0	0	0	0	
Toyoko Chemical	0	0.7	1.0	0.7	1.2	
Ulvac	1.5	1.9	2.7	2.4	3.8	
Total Japan	9.3	11.5	16.7	15.3	18.9	19.4%

Source: Dataquest
July 1989
Ref: MOCVDSHR

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Table 39

Metalorganic CVD Company Shares
Europe and ROW
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World MOCVD Market	17.5	24.8	32.1	35.6	42.5	24.8%
Europe						
Aixtron	0	0.5	1.7	4.9	6.7	
Cambridge Instruments	1.6	1.6	1.4	1.5	1.0	
Crystal Specialties	0	0	0	0	0	
CVD Equipment	0	0	0	0	0	
CVT	0	0.7	0.4	1.1	1.2	
Daiwa Semiconductor	0	0	0	0	0	
EEV	0	1.0	1.2	0.7	0	
Emcore	0	0	0	0	0	
Nippon EMC	0	0	0	0	0	
Nippon Sanso	0	0	0	0	0	
Samco	0	0	0	0	0	
Seiden	0	0	0	0	0	
Semco Engineering	0	0	0	0.3	0.9	
Shimada Rika	0	0	0	0	0	
Spire	0	0	0.4	0	0	
TEL/Thermco	0	0	0	0	0	
Thomas Schwonn	0.5	0.3	0.3	0.7	0.4	
Toyoko Chemical	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Total Europe	2.1	4.1	5.4	9.2	10.2	48.5%
Rest of World						
Aixtron	0	0	0	0	0	
Cambridge Instruments	0	0.3	0.7	0.3	0.4	
Crystal Specialties	0	0	0	0	0	
CVD Equipment	0	0	0	0	0	
CVT	0	0	0	0	0	
Daiwa Semiconductor	0	0	0	0	0	
EEV	0	0	0	0	0	
Emcore	0	0	0	0	0	
Nippon EMC	0	0	0	0	0	

(Continued)

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Table 39 (Continued)

Metalorganic CVD Company Shares
Europe and ROW
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Nippon Sanso	0	0	0	0	0	
Samco	0	0	0	0	0	
Seiden	0	0	0	0	0	
Semco Engineering	0	0	0	0	0	
Shimada Rika	0	0	0	0	0	
Spire	0	0	0	0	0	
TEL/Thermco	0	0	0	0	0	
Thomas Schwonn	0	0	0	0	0	
Toyoko Chemical	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Total Rest of World	0	0.3	0.7	0.3	0.4	N/A

N/A = Not Available

Source: Dataquest
July 1989
Ref: MOCVDSHR

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Table 40

Metalorganic CVD Company Shares
Worldwide
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World MOCVD Market	17.5	24.8	32.1	35.6	42.5	24.8%
Worldwide						
Aixtron	0	0.5	1.7	4.9	6.7	
Cambridge Instruments	3.5	4.1	3.6	3.3	2.7	
Crystal Specialties	1.2	1.8	2.7	2.6	2.7	
CVD Equipment	1.2	1.5	0.6	1.2	1.0	
CVT	0.5	0.7	0.4	1.1	1.2	
Daiwa Semiconductor	0	0	0.4	0.4	0.5	
EEV	0	1.0	1.4	0.7	0	
Emcore	0	0.1	2.3	5.1	7.0	
Nippon EMC	0.8	1.1	1.5	1.4	1.9	
Nippon Sanso	2.3	3.6	4.6	4.9	6.5	
Samco	1.1	0.7	1.0	1.1	1.2	
Seiden	1.3	0.9	1.3	0.6	0.6	
Semco Engineering	0	0	0	0.3	0.9	
Shimada Rika	0	0	0.3	0	0	
Spire	0.8	3.0	3.3	1.3	2.1	
TEL/Thermco	2.3	2.3	3.0	2.9	1.7	
Thomas Schwonn	1.0	0.9	0.3	0.7	0.8	
Toyoko Chemical	0	0.7	1.0	0.7	1.2	
Ulvac	1.5	1.9	2.7	2.4	3.8	
Total Worldwide	17.5	24.8	32.1	35.6	42.5	24.8%

Source: Dataquest
July 1989
Ref: MOCVDSHR

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Table 41

Molecular Beam Epitaxy Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World MBE Market	41.4	53.4	69.2	71.3	85.4	19.8%
United States						
Anelva	0	0	0	0	0	
Eiko	0	0	0	0	0	
Emcore	0	0	0	0	0	
ISA Riber	6.1	4.8	5.4	7.0	7.7	
Perkin-Elmer	2.7	6.0	7.2	5.0	2.8	
Seiko	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	4.3	4.5	6.3	5.2	5.4	
VG Instruments	5.0	6.0	5.4	2.5	5.1	
Total United States	18.1	21.3	24.3	19.7	21.0	3.8%
Japan						
Anelva	2.5	6.3	7.2	9.7	15.8	
Eiko	0.5	1.0	1.2	1.4	1.2	
Emcore	0	0	0	0	0	
ISA Riber	5.0	2.4	3.5	6.0	7.0	
Perkin-Elmer	0	0	0	0	0	
Seiko	0	0.8	2.0	1.2	1.4	
Ulvac	3.4	4.2	7.8	7.6	9.2	
Varian	0.9	0.9	0.8	1.9	5.2	
VG Instruments	0.9	2.4	4.2	8.1	5.6	
Total Japan	13.2	18.0	26.7	35.9	45.4	36.2%
Europe						
Anelva	0	0	0	0	0	
Eiko	0	0	0	0	0	
Emcore	0	0	0	0	0	
ISA Riber	5.0	6.0	4.7	4.9	5.6	
Perkin-Elmer	0	0	0	0	0	
Seiko	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	1.7	1.8	3.0	4.4	6.3	
VG Instruments	0.7	4.0	8.7	2.4	5.8	
Total Europe	7.4	11.8	16.4	11.7	17.7	24.4%

(Continued)

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Table 41 (Continued)

Molecular Beam Epitaxy Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Rest of World						
Anelva	0	0	0	0	0	
Eiko	0	0	0	0	0	
Emcore	0	0	0	0	0	
ISA Riber	1.1	1.2	0	1.4	0.7	
Perkin-Elmer	0	0	0	0	0	
Seiko	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	0	0	0.7	0.6	0.6	
VG Instruments	1.6	1.1	1.1	2.0	0	
Total Rest of World	2.7	2.3	1.8	4.0	1.3	(16.7%)
Worldwide						
Anelva	2.5	6.3	7.2	9.7	15.8	
Eiko	0.5	1.0	1.2	1.4	1.2	
Emcore	0	0	0	0	0	
ISA Riber	17.2	14.4	13.6	19.3	21.0	
Perkin-Elmer	2.7	6.0	7.2	5.0	2.8	
Seiko	0	0.8	2.0	1.2	1.4	
Ulvac	3.4	4.2	7.8	7.6	9.2	
Varian	6.9	7.2	10.8	12.1	17.5	
VG Instruments	8.2	13.5	19.4	15.0	16.5	
Total Worldwide	41.4	53.4	69.2	71.3	85.4	19.8%

Source: Dataquest
July 1989
Ref: MBESHR

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Table 42

Diffusion Furnace Company Shares
United States
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Diffusion Market	188.9	207.2	155.6	173.2	265.8	8.9%
Horizontal Tube						
ASM	0.7	3.6	3.3	2.3	3.4	
BTU/Bruce	29.7	29.2	18.3	8.3	17.3	
Denko	0	0	0	0	0	
Gasonics	4.5	5.3	6.1	7.5	9.0	
Kokusai	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	1.8	1.1	0.6	0	0	
Process Technology	0	0	0	0	0	
Solitec	0.5	0	0.2	0	0	
Tokyo Electron Ltd.	1.2	0	0	0	0	
Tempress	0	6.0	2.0	0.5	3.0	
Thermco	25.5	20.3	12.4	15.7	42.0	
Tylan	5.2	1.2	1.7	2.0	2.5	
Ulvac/BTU	0	0	0	0	0	
Total Horizontal	69.1	66.7	44.6	36.3	77.2	2.8%
Vertical Tube						
All Companies	0.2	0.3	0.4	0.8	3.5	104.5%
Total United States	69.3	67.0	45.0	37.1	80.7	3.9%

Source: Dataquest
July 1989
Ref: DIFFSHR

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Table 43

Diffusion Furnace Company Shares
Japan
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Diffusion Market	188.9	207.2	155.6	173.2	265.8	8.9%
Horizontal Tube						
ASM	0	0	0	0	0	
BTU/Bruce	0.2	0.6	0.4	0	0	
Denko	1.1	0.6	0.6	0.8	0.9	
Gasonics	0	0	0	0	0	
Kokusai	25.3	16.8	12.0	16.7	13.4	
Koyo Lindberg	9.7	9.7	6.0	2.6	3.3	
Pacific Western	0	0	0	0	0	
Process Technology	0	0	0	0	0	
Solitec	0	0	0	0	0	
Tokyo Electron Ltd.	44.8	60.0	49.0	55.6	82.3	
Tempress	0	0	0	0	0.5	
Thermco	0	0	0	0	0	
Tylan	0	0	0	0	0	
Ulvac/BTU	0.2	0.5	0.4	1.7	2.0	
Total Horizontal	81.3	88.2	68.4	77.4	102.4	5.9%
Vertical Tube						
All Companies	0.3	2.1	5.8	9.5	18.5	180.2%
Total Japan	81.6	90.3	74.2	86.9	120.9	10.3%

Source: Dataquest
July 1989
Ref: DIFFSHR

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Table 44

Diffusion Furnace Company Shares
Europe
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Diffusion Market	188.9	207.2	155.6	173.2	265.8	8.9%
Horizontal Tube						
ASM	8.9	13.3	13.3	16.2	19.3	
BTU/Bruce	4.2	4.9	4.2	7.3	8.2	
Denko	0	0	0	0	0	
Gasonics	0	0	0	0	0	
Kokusai	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0	0	0	0	0	
Process Technology	0	0	0	0	0	
Solitec	0.1	0	0	0	0	
Tokyo Electron Ltd.	0	0	0	0	4.2	
Tempress	0	0	0	0	0.8	
Thermco	12.8	15.6	11.2	13.2	12.0	
Tylan	0	0.1	0.8	0	0	
Ulvac/BTU	0	0	0	0	0	
Others	1.7	1.6	1.7	2.5	4.0	
Total Horizontal	27.7	35.5	31.2	39.2	48.5	15.0%
Vertical Tube						
All Companies	0	0	0	0	0.8	N/A
Total Europe	27.7	35.5	31.2	39.2	49.3	15.5%

N/A = Not Available

Source: Dataquest
July 1989
Ref: DIFFSHR

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Table 45

Diffusion Furnace Company Shares
Rest of World
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Diffusion Market	188.9	207.2	155.6	173.2	265.8	8.9%
Horizontal Tube						
ASM	2.9	1.0	0	0	0	
BTU/Bruce	1.6	1.5	1.1	3.7	8.5	
Denko	0	0	0	0	0	
Gasonics	0	0	0	0	0	
Kokusai	0	0	0	0	0	
Koyo Lindberg	0	0	0	0	0	
Pacific Western	0	0	0	0	0	
Process Technology	0	0	0	0	0	
Solitec	0	0	0.1	0	0	
Tokyo Electron Ltd.	1.2	0	0	0	0	
Tempress	0	0	0	0	0	
Thermco	4.3	9.2	4.0	6.0	6.0	
Tylan	0.3	2.7	0	0	0	
Ulvac/BTU	0	0	0	0	0	
Total Horizontal	10.3	14.4	5.2	9.7	14.5	8.9%
Vertical Tube						
All Companies	0	0	0	0.3	0.4	N/A
Total Rest of World	10.3	14.4	5.2	10.0	14.9	9.7%

N/A = Not Available

Source: Dataquest
July 1989
Ref: DIFFSHR

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Table 46

Diffusion Furnace Company Shares
Worldwide
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Diffusion Market	188.9	207.2	155.6	173.2	265.8	8.9%
Horizontal Tube						
ASM	12.5	17.9	16.6	18.5	22.7	
BTU/Bruce	35.7	36.2	24.0	19.3	34.0	
Denko	1.1	0.6	0.6	0.8	0.9	
Gasonics	4.5	5.3	6.1	7.5	9.0	
Kokusai	25.3	16.8	12.0	16.7	13.4	
Koyo Lindberg	9.7	9.7	6.0	2.6	3.3	
Pacific Western	1.8	1.1	0.6	0	0	
Process Technology	0	0	0	0	0	
Solitec	0.6	0	0.3	0	0	
Tokyo Electron Ltd.	47.2	60.0	49.0	55.6	86.5	
Tempress	0	6.0	2.0	0.5	4.3	
Thermco	42.6	45.1	27.6	34.9	60.0	
Tylan	5.5	4.0	2.5	2.0	2.5	
Ulvac/BTU	0.2	0.5	0.4	1.7	2.0	
Others	1.7	1.6	1.7	2.5	4.0	
Total Horizontal	188.4	204.8	149.4	162.6	242.6	6.5%
Vertical Tube						
All Companies	0.5	2.4	6.2	10.6	23.2	161.0%
Total Worldwide	188.9	207.2	155.6	173.2	265.8	8.9%

Source: Dataquest
July 1989
Ref: DIFFSHR

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Table 47

Rapid Thermal Processing Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World RTP Market	10.8	14.3	15.1	18.5	22.0	19.5%
United States						
AG Associates	2.3	4.5	5.4	5.9	6.0	
Dainippon Screen	0	0	0	0	0	
Eaton	0.7	0.7	0.2	0.2	0.2	
Kokusai	0	0	0	0	0	
Koyo-Lindberg	0	0	0	0	0	
Nanosil	0	0	0	0.3	0.3	
Peak Systems	0	0	0.7	2.7	4.2	
Process Products	0	0.5	0.5	0.6	0.4	
Sitesa Addax (AET)	0	0	0	0	0	
TEL/Thermco	0	0	0	0	0	
Ushio	0	0	0	0	0	
Varian	0.3	0.1	0.2	0.2	0.2	
Total United States	3.3	5.8	7.0	9.9	11.3	36.0%
Japan						
AG Associates	3.3	2.4	1.6	1.9	2.0	
Dainippon Screen	1.3	1.9	1.8	1.0	1.2	
Eaton	0	0	0.2	0	0.2	
Kokusai	0.1	0.1	0	0	0	
Koyo-Lindberg	0.1	0.1	0.3	0.2	0.6	
Nanosil	0	0	0	0	0	
Peak Systems	0	0	0	0.7	2.0	
Process Products	0	0	0	0	0	
Sitesa Addax (AET)	0	0	0	0	0	
TEL/Thermco	0.4	0.4	0.4	0	0.3	
Ushio	0.3	0.3	0	0	0	
Varian	0.2	0.2	0.2	0.7	0.2	
Total Japan	5.7	5.4	4.5	4.5	6.5	3.3%

(Continued)

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Table 47 (Continued)

Rapid Thermal Processing Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Europe						
AG Associates	0.4	1.2	1.6	2.1	1.6	
Dainippon Screen	0	0	0	0	0	
Eaton	0.8	0.5	0.3	0	0	
Kokusai	0	0	0	0	0	
Koyo-Lindberg	0	0	0	0	0	
Nanosil	0	0	0	0	0	
Peak Systems	0	0	0	0	0.2	
Process Products	0	0	0	0.1	0	
Sitesa Addax (AET)	0.4	0.4	0.7	1.0	1.2	
TEL/Thermco	0	0	0	0	0	
Ushio	0	0	0	0	0	
Varian	0.1	0.1	0	0	0	
Total Europe	1.7	2.2	2.6	3.2	3.0	15.3%
Rest of World						
AG Associates	0.1	0.7	1.0	0.9	1.0	
Dainippon Screen	0	0	0	0	0	
Eaton	0	0.2	0	0	0	
Kokusai	0	0	0	0	0	
Koyo-Lindberg	0	0	0	0	0	
Nanosil	0	0	0	0	0	
Peak Systems	0	0	0	0	0.2	
Process Products	0	0	0	0	0	
Sitesa Addax (AET)	0	0	0	0	0	
TEL/Thermco	0	0	0	0	0	
Ushio	0	0	0	0	0	
Varian	0	0	0	0	0	
Total ROW	0.1	0.9	1.0	0.9	1.2	86.1%

(Continued)

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Table 47 (Continued)

Rapid Thermal Processing Company Shares
Regional
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Worldwide						
AG Associates	6.1	8.8	9.6	10.8	10.6	
Dainippon Screen	1.3	1.9	1.8	1.0	1.2	
Eaton	1.5	1.4	0.7	0.2	0.4	
Kokusai	0.1	0.1	0	0	0	
Koyo-Lindberg	0.1	0.1	0.3	0.2	0.6	
Nanosil	0	0	0	0.3	0.3	
Peak Systems	0	0	0.7	3.4	6.6	
Process Products	0	0.5	0.5	0.7	0.4	
Sitesa Addax (AET)	0.4	0.4	0.7	1.0	1.2	
TEL/Thermco	0.4	0.4	0.4	0	0.3	
Ushio	0.3	0.3	0	0	0	
Varian	0.6	0.4	0.4	0.9	0.4	
Total Worldwide	10.8	14.3	15.1	18.5	22.0	19.5%

Source: Dataquest
July 1989
Ref: RTPSHR

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Table 48

Ion Implantation Company Shares
United States
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Implanter Market	288.3	293.4	118.8	185.9	378.9	7.1%
Medium Current						
Balzers	0	0	0	0	0	
Eaton	13.0	14.8	6.6	4.0	10.0	
Hitachi	0	0	0	0	0	
Nissin	0	0	0	0	1.2	
TEL/Varian	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	35.0	19.1	9.2	5.9	6.2	
Veeco	5.0	2.0	0	0	0	
Total Medium Current	53.0	35.9	15.8	9.9	17.4	(24.3%)
High Current						
Applied Materials	0	0	0	4.0	9.1	
Balzers	0	0	0	0	0	
Eaton	50.4	35.1	8.8	17.0	27.0	
Hitachi	0	0	0	0	0	
Nissin	0	0	0	0	0	
TEL/Varian	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	10.0	4.2	4.0	6.6	8.4	
Veeco	5.0	3.0	0	0	0	
Total High Current	65.4	42.3	12.8	27.6	44.5	(9.2%)
High Voltage						
Eaton	0	0	2.0	4.5	0	
Genus (General Ionex)	0	0	0	0	3.6	
HVE Europa	0	0	0	0	0	
National Electrostatics	1.1	0.9	2.5	1.8	1.2	
Nissin	0	0	0	0	0	
Varian	0	0	3.9	1.8	1.8	
Veeco	0	0	0	0	0	
Total High Voltage	1.1	0.9	8.4	8.1	6.6	56.5%
Total United States	119.5	79.1	37.0	45.6	68.5	(13.0%)

Source: Dataquest
July 1989
Ref: IMPLSHR

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Table 49

Ion Implantation Company Shares
Japan
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Implanter Market	288.3	293.4	118.8	185.9	378.9	7.1%
Medium Current						
Balzers	0	0	0	0	0	
Eaton	0	1.1	1.5	2.6	2.9	
Hitachi	0	0	0	0	0	
Nissin	15.2	19.3	10.2	11.1	26.2	
TEL/Varian	16.9	26.4	5.2	8.4	24.1	
Ulvac	9.7	6.3	4.8	5.2	7.5	
Varian	0.5	1.8	0.7	2.3	3.4	
Veeco	0	0	0	0	0	
Total Medium Current	42.3	54.9	22.4	29.6	64.1	11.0%
High Current						
Applied Materials	0	0	2.2	2.0	8.6	
Balzers	0	0	0	0	0	
Eaton	33.3	23.8	3.9	18.4	42.8	
Hitachi	3.4	4.2	3.2	3.8	9.6	
Nissin	2.3	2.2	1.6	1.8	4.1	
TEL/Varian	10.5	10.5	5.0	16.8	52.5	
Ulvac	2.3	2.1	0.9	2.1	3.8	
Varian	25.9	39.9	0	1.4	18.0	
Veeco	0	3.0	0	0	0	
Total High Current	77.7	85.7	16.8	46.3	139.4	15.7%
High Voltage						
Eaton	0	0	0	3.1	0	
Genus (General Ionex)	0	0	0	0	9.0	
HVE Europa	0	0	0	0	0	
National Electrostatics	0	0	1.1	0	0	
Nissin	0	0	0	2.8	0	
Varian	0	0	0	0	0	
Veeco	0	0	0	0	0	
Total High Voltage	0	0	1.1	5.9	9.0	N/A
Total Japan	120.0	140.6	40.3	81.8	212.5	15.4%

N/A = Not Available

Source: Dataquest
July 1989
Ref: IMPLSHR

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Table 50

Ion Implantation Company Shares
Europe
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Implanter Market	288.3	293.4	118.8	185.9	378.9	7.1%
Medium Current						
Balzers	6.0	0	0	1.4	2.1	
Eaton	2.9	6.0	3.5	7.0	11.0	
Hitachi	0	0	0	0	0	
Nissin	0	0	0	0	0.9	
TEL/Varian	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	12.0	16.6	6.9	6.7	3.9	
Veeco	1.0	0	0	0	0	
Total Medium Current	21.9	22.6	10.4	15.1	17.9	(4.9%)
High Current						
Applied Materials	0	0	2.2	4.0	7.2	
Balzers	0	0	0	0	0	
Eaton	11.7	16.1	11.8	12.0	23.0	
Hitachi	0	0	0	0	0	
Nissin	0	0	0	0	0	
TEL/Varian	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	5.0	4.2	3.0	5.5	2.4	
Veeco	0	1.0	0	0	0	
Total High Current	16.7	21.3	17.0	21.5	32.6	18.2%
High Voltage						
Eaton	0	0	0	2.2	2.5	
Genus (General Ionex)	0	0	0	0	1.8	
HVE Europa	0	0	0	0	0	
National Electrostatics	0	1.2	0.3	0	0	
Nissin	0	0	0	0	0	
Varian	0	0	0	1.8	0	
Veeco	0	0	0	0	0	
Total High Voltage	0	1.2	0.3	4.0	4.3	N/A
Total Europe	38.6	45.1	27.7	40.6	54.8	9.2%

N/A = Not Available

Source: Dataquest
July 1989
Ref: IMPLSHR

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Table 51

Ion Implantation Company Shares
Rest of World
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Implanter Market	288.3	293.4	118.8	185.9	378.9	7.1%
Medium Current						
Balzers	0	0	0	1.4	2.1	
Eaton	0.5	0.6	1.9	2.0	7.0	
Hitachi	0	0	0	0	0	
Nissin	0	0	0	0	0	
TEL/Varian	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	3.0	10.5	4.0	3.0	9.4	
Veeco	0	0	0	0	0	
Total Medium Current	3.5	11.1	5.9	6.4	18.5	51.6%
High Current						
Applied Materials	0	0	0	0	0	
Balzers	0	0	0	0	0	
Eaton	2.7	12.3	5.9	6.0	9.0	
Hitachi	0	0	0	0	0	
Nissin	0	0	0	0	0	
TEL/Varian	0	0	0	0	0	
Ulvac	0	0	0	0	0	
Varian	4.0	5.2	2.0	5.5	15.6	
Veeco	0	0	0	0	0	
Total High Current	6.7	17.5	7.9	11.5	24.6	38.4%
High Voltage						
Eaton	0	0	0	0	0	
Genus (General Ionex)	0	0	0	0	0	
HVE Europa	0	0	0	0	0	
National Electrostatics	0	0	0	0	0	
Nissin	0	0	0	0	0	
Varian	0	0	0	0	0	
Veeco	0	0	0	0	0	
Total High Voltage	0	0	0	0	0	N/A
Total Rest of World	10.2	28.6	13.8	17.9	43.1	43.4%

N/A = Not Available

Source: Dataquest
July 1989
Ref: IMPLSHR

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Table 52

Ion Implantation Company Shares
Worldwide
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Implanter Market	288.3	293.4	118.8	185.9	378.9	7.1%
Medium Current						
Balzers	6.0	0	0	2.8	4.2	
Eaton	16.4	22.5	13.5	15.6	30.9	
Hitachi	0	0	0	0	0	
Nissin	15.2	19.3	10.2	11.1	28.3	
TEL/Varian	16.9	26.4	5.2	8.4	24.1	
Ulvac	9.7	6.3	4.8	5.2	7.5	
Varian	50.5	48.0	20.8	17.9	22.9	
Veeco	6.0	2.0	0	0	0	
Total Medium Current	120.7	124.5	54.5	61.0	117.9	(0.6%)
High Current						
Applied Materials	0	0	4.4	10.0	24.9	
Balzers	0	0	0	0	0	
Eaton	98.1	87.3	30.4	53.4	101.8	
Hitachi	3.4	4.2	3.2	3.8	9.6	
Nissin	2.3	2.2	1.6	1.8	4.1	
TEL/Varian	10.5	10.5	5.0	16.8	52.5	
Ulvac	2.3	2.1	0.9	2.1	3.8	
Varian	44.9	53.5	9.0	19.0	44.4	
Veeco	5.0	7.0	0	0	0	
Total High Current	166.5	166.8	54.5	106.9	241.1	9.7%
High Voltage						
Eaton	0	0	2.0	9.8	2.5	
Genus (General Ionex)	0	0	0	0	14.4	
HVE Europa	0	0	0	0	0	
National Electrostatics	1.1	2.1	3.9	1.8	1.2	
Nissin	0	0	0	2.8	0	
Varian	0	0	3.9	3.6	1.8	
Veeco	0	0	0	0	0	
Total High Voltage	1.1	2.1	9.8	18.0	19.9	106.2%
Total Worldwide	288.3	293.4	118.8	185.9	378.9	7.1%

Source: Dataquest
July 1989
Ref: IMPLSHR

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Table 53

Optical CD/Wafer Inspection Company Shares
United States
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World CD/Wafer Inspection Market	62.6	54.5	70.8	98.6	173.4	29.0%
Optical Critical Dimension						
Heidelberg Instruments	0	0	0	0.7	1.7	
Hitachi	0	0	0	0	0	
IVS, Inc.	0	0	0.5	1.4	6.4	
KLA Instruments	0	0	0	0	2.8	
Nanometrics	4.1	1.2	0.9	1.1	1.4	
Nidek	0	0	0	0	0	
Nikon	0.7	0.3	0.2	0.3	0.5	
Optical Specialties	4.1	2.3	1.8	1.1	1.0	
Perkin-Elmer	0	0	0	0	2.3	
Reichert-McBain	0	0	2.7	0.3	0	
Ryokosha	0.1	0.1	0.1	0	0.3	
SiSCAN Systems	0	0	1.7	2.3	4.9	
Vickers Instruments	0	0	0	4.9	7.0	
Wild Leitz	2.1	1.7	1.5	2.3	3.3	
Other CD Companies	5.5	2.2	1.9	1.5	1.8	
Total CD Equipment	16.6	7.8	11.3	15.9	33.4	19.1%
Wafer Inspection						
Canon	0	0	0	0	0	
Estek (Aeronca)	0	0.3	0.2	0.1	0.2	
Insystems	0	0	0	1.1	6.4	
KLA Instruments	0	0	0	0	7.4	
Nidek	0	0	0	0	0	
Nikon	2.1	1.4	1.6	2.1	2.9	
Optical Specialties	6.8	3.1	2.2	1.5	1.3	
Karl Suss	0	0	0	0	0	
Wild Leitz	2.2	1.6	1.3	2.2	5.0	
Zeiss	0	0	1.0	0.6	0.9	
Other Waf. Insp. Cos.	3.1	1.4	1.2	1.1	1.2	
Total Wafer Inspect.	14.2	7.8	7.5	8.7	25.3	15.5%

(Continued)

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Table 53 (Continued)

Optical CD/Wafer Inspection Company Shares
United States
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Joint CD/Inspection						
KLA Instruments	0	6.3	8.8	11.6	9.4	
Optical Specialties	2.7	2.0	1.7	2.1	0.5	
Total Joint CD/Insp.	2.7	8.3	10.5	13.7	9.9	38.4%
Total U.S. CD/Insp.	33.5	23.9	29.3	38.3	68.6	

Source: Dataquest
July 1989
Ref: INSPSHR

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Table 54

Optical CD/Wafer Inspection Company Shares
Japan
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World CD/Wafer Inspection Market	62.6	54.5	70.8	98.6	173.4	29.0%
Optical Critical Dimension						
Heidelberg Instruments	0	0	0	0	0.3	
Hitachi	0	0	4.1	6.0	1.7	
IVS, Inc.	0	0	0	0	0	
KLA Instruments	0	0	0	0	1.5	
Nanometrics	1.4	0.5	0.3	0.1	0.4	
Nidek	0	0	0	0	0.5	
Nikon	3.5	2.5	1.7	4.5	12.9	
Optical Specialties	0.1	0.3	0.2	0	0.7	
Perkin-Elmer	0	0	0	0	0.2	
Reichert-McBain	0	0	0	0	0	
Ryokosha	2.1	1.3	1.4	1.4	1.7	
SiSCAN Systems	0	0	0.2	0.2	0	
Vickers Instruments	0	0	0	0.8	0	
Wild Leitz	0.5	0.4	0.3	0.5	0.2	
Other CD Companies	2.8	1.7	2.3	1.5	2.0	
Total CD Equipment	10.4	6.7	10.5	15.0	22.1	20.7%
Wafer Inspection						
Canon	2.0	1.3	1.4	2.0	3.0	
Estek (Aeronca)	0	0	0	0	0	
Insystems	0	0	0	1.1	3.4	
KLA Instruments	0	0	0	0	8.6	
Nidek	2.0	1.7	2.2	2.3	5.0	
Nikon	3.7	3.0	4.1	4.4	8.8	
Optical Specialties	0.2	0.4	0.3	0	0	
Karl Suss	0	0	0	0	0	
Wild Leitz	0.3	0.4	0.2	0	0	
Zeiss	0	0	0	0	0	
Other Waf. Insp. Cos.	0.9	0.4	0.4	0.5	0.7	
Total Wafer Inspect.	9.1	7.2	8.6	10.3	29.5	34.2%

(Continued)

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Table 54 (Continued)

Optical CD/Wafer Inspection Company Shares
Japan
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Joint CD/Inspection						
KLA Instruments	0	3.5	6.9	11.5	9.8	
Optical Specialties	0.1	0.3	0.3	0	0	
Total Joint CD/Insp.	0.1	3.8	7.2	11.5	9.8	214.6%
Total Japan CD/Insp.	19.6	17.7	26.3	36.8	61.4	

Source: Dataquest
July 1989
Ref: INSPSHR

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Table 55

Optical CD/Wafer Inspection Company Shares
Europe
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World CD/Wafer Inspection Market	62.6	54.5	70.8	98.6	173.4	29.0%
Optical Critical Dimension						
Heidelberg Instruments	0	0	0	0.9	1.4	
Hitachi	0	0	0	0	0	
IVS, Inc.	0	0	0	0.1	0	
KLA Instruments	0	0	0	0	1.9	
Nanometrics	0.5	0.2	0.2	0.3	0.1	
Nidek	0	0	0	0	0	
Nikon	0.3	0.1	0.2	0.2	0.3	
Optical Specialties	0.5	0.3	0.2	0.1	0.2	
Perkin-Elmer	0	0	0	0	0.2	
Reichert-McBain	0	0	0.3	0	0	
Ryokosha	0	0	0	0	0.3	
SiSCAN Systems	0	0	0	0.5	0	
Vickers Instruments	0	0	0	2.6	2.0	
Wild Leitz	1.5	1.8	2.5	2.8	5.7	
Other CD Companies	0.9	1.0	0.7	0.5	0.7	
Total CD Equipment	3.7	3.4	4.1	8.0	12.8	36.4%
Wafer Inspection						
Canon	0	0	0	0	0	
Estek (Aeronca)	0	0	0	0	0	
Insystems	0	0	0	0	0	
KLA Instruments	0	0	0	0	1.1	
Nidek	0	0	0	0	0.4	
Nikon	0	0	0	0.8	1.7	
Optical Specialties	0.8	0.4	0.3	0.1	0	
Karl Suss	0.2	0	0	0	0	
Wild Leitz	1.5	2.1	1.7	2.1	4.5	
Zeiss	0	0.9	1.4	1.2	0.9	
Other Waf. Insp. Cos.	0.7	0.6	0.4	0.3	0.1	
Total Wafer Inspect.	3.2	4.0	3.8	4.5	8.7	28.4%

(Continued)

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Table 55 (Continued)

Optical CD/Wafer Inspection Company Shares
Europe
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Joint CD/Inspection						
KLA Instruments	0	1.4	2.4	3.6	3.7	
Optical Specialties	0.3	0.2	0.2	0.1	0.2	
Total Joint CD/Insp.	0.3	1.6	2.6	3.7	3.9	89.9%
Total Europe CD/Insp.	7.2	9.0	10.5	16.2	25.4	

Source: Dataquest
July 1989
Ref: INSPSHR

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Table 56

Optical CD/Wafer Inspection Company Shares
Rest of World
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World CD/Wafer Inspection Market	62.6	54.5	70.8	98.6	173.4	29.0%
Optical Critical Dimension						
Heidelberg Instruments	0	0	0	0	0	
Hitachi	0	0	0	0	0	
IVS, Inc.	0	0	0	0	0	
KLA Instruments	0	0	0	0	0	
Nanometrics	0.7	0.4	0.1	0.2	0.4	
Nidek	0	0	0	0	0	
Nikon	0.2	0.1	0.2	0.2	0.6	
Optical Specialties	0	0.2	0	0.1	0.4	
Perkin-Elmer	0	0	0	0	0.2	
Reichert-McBain	0	0	0	0	0	
Ryokosha	0	0	0	0	0.2	
SiSCAN Systems	0	0	0	0	0	
Vickers Instruments	0	0	0	0	0	
Wild Leitz	0.3	0.5	0.5	0.8	0.6	
Other CD Companies	0.6	1.0	2.0	2.1	3.2	
Total CD Equipment	1.8	2.2	2.8	3.4	5.6	32.8%
Wafer Inspection						
Canon	0	0	0	0	0	
Estek (Aeronca)	0	0	0	0	0	
Insystems	0	0	0	0	0	
KLA Instruments	0	0	0	0	4.3	
Nidek	0	0	0	0.8	0.8	
Nikon	0	0	0.7	0.8	1.4	
Optical Specialties	0	0.3	0	0.1	0	
Karl Suss	0	0	0	0	0	
Wild Leitz	0.3	0.6	0.3	0.4	0.9	
Zeiss	0	0	0	0	0	
Other Waf. Insp. Cos.	0.2	0.6	0.9	0.8	0.8	
Total Wafer Inspect.	0.5	1.5	1.9	2.9	8.2	101.2%

(Continued)

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Table 56 (Continued)

Optical CD/Wafer Inspection Company Shares
Rest of World
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Joint CD/Inspection						
KLA Instruments	0	0	0	0.9	3.7	
Optical Specialties	0	0.2	0	0.1	0.5	
Total Joint CD/Insp.	0	0.2	0	1.0	4.2	N/A
Total ROW CD/Insp.	2.3	3.9	4.7	7.3	18.0	

N/A = Not Available

Source: Dataquest
July 1989
Ref: INSPSHR

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Table 57

Optical CD/Wafer Inspection Company Shares
Worldwide
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World CD/Wafer Inspection Market	62.6	54.5	70.8	98.6	173.4	29.0%
Optical Critical Dimension						
Heidelberg Instruments	0	0	0	1.6	3.4	
Hitachi	0	0	4.1	6.0	1.7	
IVS, Inc.	0	0	0.5	1.5	6.4	
KLA Instruments	0	0	0	0	6.2	
Nanometrics	6.7	2.3	1.5	1.7	2.3	
Nidek	0	0	0	0	0.5	
Nikon	4.7	3.0	2.3	5.2	14.3	
Optical Specialties	4.7	3.1	2.2	1.3	2.3	
Perkin-Elmer	0	0	0	0	2.9	
Reichert-McBain	0	0	3.0	0.3	0	
Ryokosha	2.2	1.4	1.5	1.4	2.5	
SiSCAN Systems	0	0	1.9	3.0	4.9	
Vickers Instruments	0	0	0	8.3	9.0	
Wild Leitz	4.4	4.4	4.8	6.4	9.8	
Other CD Companies	9.8	5.9	6.9	5.6	7.7	
Total CD Equipment	32.5	20.1	28.7	42.3	73.9	22.8%
Wafer Inspection						
Canon	2.0	1.3	1.4	2.0	3.0	
Estek (Aeronca)	0	0.3	0.2	0.1	0.2	
Insystems	0	0	0	2.2	9.8	
KLA Instruments	0	0	0	0	21.4	
Micro-Controle	0	0	0	0	0	
Nidek	2.0	1.7	2.2	3.1	6.2	
Nikon	5.8	4.4	6.4	8.1	14.8	
Optical Specialties	7.8	4.2	2.8	1.7	1.3	
Karl Suss	0.2	0	0	0	0	
Wild Leitz	4.3	4.7	3.5	4.7	10.4	
Zeiss	0	0.9	2.4	1.8	1.8	
Other Waf. Insp. Cos.	4.9	3.0	2.9	2.7	2.8	
Total Wafer Inspect.	27.0	20.5	21.8	26.4	71.7	27.7%

(Continued)

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Table 57 (Continued)

Optical CD/Wafer Inspection Company Shares
Worldwide
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Joint CD/Inspection						
KLA Instruments	0	11.2	18.1	27.6	26.6	
Optical Specialties	3.1	2.7	2.2	2.3	1.2	
Total Joint CD/Insp.	3.1	13.9	20.3	29.9	27.8	73.0%
Total WW CD/Insp.	62.6	54.5	70.8	98.6	173.4	

Source: Dataquest
July 1989
Ref: INSPSHR

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Wafer Fab Equipment--Company Shares by Category

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Wafer Fab Equipment—Summary Data by Category

This section of the equipment data base consists of two summary tables for the worldwide fab equipment market. Both tables present sales by equipment category for the years 1984 to 1988. In Table 1, the annual sales for each equipment category are organized by region of equipment sales; in Table 2, annual sales for each equipment category are organized by equipment vendor nationality (United States, Japan, and Europe).

For example, the total worldwide sales for contact/proximity aligners of $67 million in 1984 is the same in both Table 1 and Table 2; however, whereas Table 1 breaks the sales down by region, Table 2 breaks the sales down by nationality of the companies supplying the aligners.

In Table 2, the subtotal fab equipment line item designates that portion of the total worldwide fab equipment market for which detailed company data are available. For some of the categories in Table 2 (Ion Milling, Other Process Control, Factory Automation, and Other Equipment), detailed company data are not yet complete. For these categories, top–down estimates have been made and included in Tables 1 and 2 so that world fab equipment sales are consistent across all tables. Detailed company data are available for 85 percent of the total worldwide wafer fab equipment market for 1988.

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Wafer Fab Equipment--Summary Data by Category

Table 1

Worldwide Wafer Fab Equipment Market
Regional Shares by Category
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Fab Equipment Market	3,519.5	3,356.4	2,713.1	3,147.5	4,894.3	8.6%
Lithography						
Contact/Proximity						
United States	23.7	15.6	11.1	9.5	8.0	(23.8%)
Japan	26.5	18.0	9.1	5.5	4.7	(35.1%)
Europe	9.2	7.1	6.0	4.5	4.5	(16.4%)
Rest of World	7.6	7.1	5.2	4.0	3.5	(17.6%)
Total Cont./Prox.	67.0	47.8	31.4	23.5	20.7	(25.4%)
Projection Aligners						
United States	114.9	118.1	98.4	66.4	72.0	(11.0%)
Japan	78.1	105.3	38.4	36.7	66.3	(4.0%)
Europe	33.7	30.6	24.6	17.3	16.2	(16.7%)
Rest of World	9.1	12.1	9.6	8.2	4.6	(15.7%)
Total Projection	235.8	266.1	171.0	128.6	159.1	(9.4%)
Steppers						
United States	205.8	134.8	152.8	184.0	280.0	8.0%
Japan	266.6	209.5	139.1	212.8	425.2	12.4%
Europe	31.9	54.9	45.7	58.5	84.5	27.6%
Rest of World	22.0	31.1	25.5	47.8	113.4	50.7%
Total Steppers	526.3	430.3	363.1	503.1	903.1	14.5%
Direct-Write E-Beam						
United States	8.9	11.5	30.4	17.2	13.2	10.4%
Japan	12.4	10.0	29.2	32.7	35.9	30.4%
Europe	5.0	9.2	8.5	15.2	16.4	34.6%
Rest of World	2.5	0	0	2.0	2.0	(5.4%)
Total Direct-Write	28.8	30.7	68.1	67.1	67.5	23.7%

(Continued)

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Wafer Fab Equipment--Summary Data by Category

Table 1 (Continued)

Worldwide Wafer Fab Equipment Market
Regional Shares by Category
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Maskmaking E-Beam						
United States	20.6	39.1	27.0	12.0	12.0	(12.6%)
Japan	41.6	35.5	23.7	38.0	19.2	(17.6%)
Europe	9.4	4.0	0	13.0	6.0	(10.6%)
Rest of World	0	2.7	0	3.0	11.0	N/A
Total E-Beam M/M	71.6	81.3	50.7	66.0	48.2	(9.4%)
Maskmaking Optical Laser						
United States	0	0	0	1.6	1.6	N/A
Japan	0	0	0	0	8.0	N/A
Europe	0	0	0	0	1.6	N/A
Rest of World	0	0	0	0	0	N/A
Total Laser M/M	0	0	0	1.6	11.2	N/A
X-Ray						
United States	0	0	0	0	3.4	N/A
Japan	0.8	0.8	0.8	0	2.8	N/A
Europe	1.0	1.0	0	0	2.8	29.4%
Rest of World	0	0	0	0	0	N/A
Total X-Ray	1.8	1.8	0.8	0	9.0	49.5%
Total Lithography						
United States	373.9	319.1	319.7	290.7	390.2	1.1%
Japan	426.0	379.1	240.3	325.7	562.1	7.2%
Europe	90.2	106.8	84.8	108.5	132.0	10.0%
Rest of World	41.2	53.0	40.3	65.0	134.5	34.4%
Total Lithography	931.3	858.0	685.1	789.9	1,218.8	7.0%

(Continued)

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Wafer Fab Equipment--Summary Data by Category

Table 1 (Continued)

Worldwide Wafer Fab Equipment Market
Regional Shares by Category
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Automatic Photoresist Processing Equipment						
United States	84.9	68.5	59.0	60.9	78.0	(2.1%)
Japan	66.8	54.3	51.5	61.8	119.7	15.7%
Europe	23.5	22.3	27.1	28.5	32.5	8.4%
Rest of World	8.3	12.5	8.2	12.9	19.5	23.8%
Total Track	183.5	157.6	145.8	164.1	249.7	8.0%
Etch and Clean						
Wet Process						
United States	66.2	65.6	63.3	65.9	88.4	7.5%
Japan	83.0	62.8	72.6	66.5	91.9	2.6%
Europe	19.6	22.9	19.6	22.4	34.2	14.9%
Rest of World	2.9	5.9	6.4	10.2	20.6	63.3%
Total Wet Process	171.7	157.2	161.9	165.0	235.1	8.2%
Dry Strip						
United States	22.0	13.8	13.8	14.9	20.4	(1.9%)
Japan	15.6	16.7	15.6	30.3	58.1	38.9%
Europe	5.0	5.0	3.0	1.9	3.7	(7.3%)
Rest of World	2.0	3.0	2.0	4.6	7.3	38.2%
Total Dry Strip	44.6	38.5	34.4	51.7	89.5	19.0%
Dry Etch						
United States	165.9	148.0	100.1	118.1	176.9	1.6%
Japan	93.1	102.0	82.3	113.0	239.0	26.6%
Europe	29.3	32.6	39.7	58.3	80.0	28.5%
Rest of World	10.0	17.0	15.0	18.0	51.1	50.4%
Total Dry Etch	298.3	299.6	237.1	307.4	547.0	16.4%

(Continued)

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Table 1 (Continued)

Worldwide Wafer Fab Equipment Market
Regional Shares by Category
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Ion Milling						
United States	3.9	2.2	3.7	3.7	4.0	0.6%
Japan	2.8	2.8	1.5	1.5	2.0	(8.1%)
Europe	1.6	1.5	1.6	1.6	2.0	5.7%
Rest of World	0	0	0	0	0	N/A
Total Ion Milling	8.3	6.5	6.8	6.8	8.0	(0.9%)
Total Etch and Clean						
United States	258.0	229.6	180.9	202.6	289.7	2.9%
Japan	194.5	184.3	172.0	211.3	391.0	19.1%
Europe	55.5	62.0	63.9	84.2	119.9	21.2%
Rest of World	14.9	25.9	23.4	32.8	79.0	51.7%
Total Etch & Clean	522.9	501.8	440.2	530.9	879.6	13.9%
Deposition						
CVD						
United States	88.2	82.5	62.9	92.1	152.0	14.6%
Japan	106.8	110.2	94.7	91.4	188.8	15.3%
Europe	23.6	35.8	47.2	55.3	76.6	34.2%
Rest of World	9.4	18.0	14.6	15.6	37.6	41.4%
Total CVD	228.0	246.5	219.4	254.4	455.0	18.9%
PVD						
United States	91.7	113.4	95.2	98.6	119.5	6.8%
Japan	99.5	93.9	76.5	90.1	130.4	7.0%
Europe	35.3	45.0	48.2	40.7	36.0	0.5%
Rest of World	7.0	10.7	16.7	19.6	28.8	42.4%
Total PVD	233.5	263.0	236.6	249.0	314.7	7.7%

(Continued)

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Table 1 (Continued)

Worldwide Wafer Fab Equipment Market
Regional Shares by Category
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Silicon Epitaxy						
United States	43.7	27.3	16.2	13.4	42.0	(1.0%)
Japan	50.1	26.2	13.5	13.0	23.5	(17.2%)
Europe	13.0	13.0	11.2	6.4	15.2	4.0%
Rest of World	5.0	5.0	5.4	2.7	3.8	(6.6%)
Total Silicon Epi.	111.8	71.5	46.3	35.5	84.5	(6.8%)
Metalorganic CVD						
United States	6.1	8.9	9.3	10.8	13.0	20.8%
Japan	9.3	11.5	16.7	15.3	18.9	19.4%
Europe	2.1	4.1	5.4	9.2	10.2	48.5%
Rest of World	0	0.3	0.7	0.3	0.4	N/A
Total MOCVD	17.5	24.8	32.1	35.6	42.5	24.8%
Molecular Beam Epitaxy						
United States	18.1	21.3	24.3	19.7	21.0	3.8%
Japan	13.2	18.0	26.7	35.9	45.4	36.2%
Europe	7.4	11.8	16.4	11.7	17.7	24.4%
Rest of World	2.7	2.3	1.8	4.0	1.3	(16.7%)
Total MBE	41.4	53.4	69.2	71.3	85.4	19.8%
Total Deposition						
United States	247.8	253.4	207.9	234.6	347.5	8.8%
Japan	278.9	259.8	228.1	245.7	407.0	9.9%
Europe	81.4	109.7	128.4	123.3	155.7	17.6%
Rest of World	24.1	36.3	39.2	42.2	71.9	31.4%
Total Deposition	632.2	659.2	603.6	645.8	982.1	11.6%

(Continued)

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Table 1 (Continued)

Worldwide Wafer Fab Equipment Market
Regional Shares by Category
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Diffusion						
United States	69.3	67.0	45.0	37.1	80.7	3.9%
Japan	81.6	90.3	74.2	86.9	120.9	10.3%
Europe	27.7	35.5	31.2	39.2	49.3	15.5%
Rest of World	10.3	14.4	5.2	10.0	14.9	9.7%
Total Diffusion	188.9	207.2	155.6	173.2	265.8	8.9%
Rapid Thermal Processing						
United States	3.3	5.8	7.0	9.9	11.3	36.0%
Japan	5.7	5.4	4.5	4.5	6.5	3.3%
Europe	1.7	2.2	2.6	3.2	3.0	15.3%
Rest of World	0.1	0.9	1.0	0.9	1.2	86.1%
Total RTP	10.8	14.3	15.1	18.5	22.0	19.5%
Ion Implantation						
Medium Current						
United States	53.0	35.9	15.8	9.9	17.4	(24.3%)
Japan	42.3	54.9	22.4	29.6	64.1	11.0%
Europe	21.9	22.6	10.4	15.1	17.9	(4.9%)
Rest of World	3.5	11.1	5.9	6.4	18.5	51.6%
Total Medium Current	120.7	124.5	54.5	61.0	117.9	(0.6%)
High Current						
United States	65.4	42.3	12.8	27.6	44.5	(9.2%)
Japan	77.7	85.7	16.8	46.3	139.4	15.7%
Europe	16.7	21.3	17.0	21.5	32.6	18.2%
Rest of World	6.7	17.5	7.9	11.5	24.6	38.4%
Total High Current	166.5	166.8	54.5	106.9	241.1	9.7%

(Continued)

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Table 1 (Continued)

Worldwide Wafer Fab Equipment Market
Regional Shares by Category
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
High Voltage						
United States	1.1	0.9	8.4	8.1	6.6	56.5%
Japan	0	0	1.1	5.9	9.0	N/A
Europe	0	1.2	0.3	4.0	4.3	N/A
Rest of World	0	0	0	0	0	N/A
Total High Voltage	1.1	2.1	9.8	18.0	19.9	106.2%
Total Implantation						
United States	119.5	79.1	37.0	45.6	68.5	(13.0%)
Japan	120.0	140.6	40.3	81.8	212.5	15.4%
Europe	38.6	45.1	27.7	40.6	54.8	9.2%
Rest of World	10.2	28.6	13.8	17.9	43.1	43.4%
Total Implantation	288.3	293.4	118.8	185.9	378.9	7.1%
Optical CD/Wafer Inspection Equipment						
United States	33.5	23.9	29.3	38.3	68.6	19.6%
Japan	19.6	17.7	26.3	36.8	61.4	33.0%
Europe	7.2	9.0	10.5	16.2	25.4	37.0%
Rest of World	2.3	3.9	4.7	7.3	18.0	67.3%
Total CD/Wafer Insp.	62.6	54.5	70.8	98.6	173.4	29.0%
Other Process Control						
United States	195.4	144.1	132.9	123.4	143.0	(7.5%)
Japan	188.4	158.8	104.8	135.0	191.1	0.4%
Europe	44.9	43.0	47.0	44.5	53.7	4.6%
Rest of World	17.2	22.1	18.0	29.2	39.2	22.9%
Total Process Cont.	445.9	368.0	302.7	332.1	427.0	(1.1%)

(Continued)

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Wafer Fab Equipment--Summary Data by Category

Table 1 (Continued)

Worldwide Wafer Fab Equipment Market
Regional Shares by Category
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Factory Automation						
United States	24.0	23.0	21.0	24.0	38.0	12.2%
Japan	91.0	83.0	43.0	54.0	63.0	(8.8%)
Europe	13.0	15.0	14.0	17.0	19.0	10.0%
Rest of World	2.0	4.0	3.0	4.0	10.0	49.5%
Total Automation	130.0	125.0	81.0	99.0	130.0	0
Other Equipment						
United States	51.1	44.0	37.4	38.1	54.0	1.4%
Japan	53.4	49.8	35.6	44.9	75.3	9.0%
Europe	13.9	16.3	15.8	18.4	23.2	13.7%
Rest of World	4.7	7.3	5.6	8.1	14.5	32.5%
Total Other Equip.	123.1	117.4	94.4	109.5	167.0	7.9%
Total Wafer Fab Equipment						
United States	1,460.7	1,257.5	1,077.1	1,105.2	1,569.5	1.8%
Japan	1,525.9	1,423.1	1,020.6	1,288.4	2,210.5	9.7%
Europe	397.6	466.9	453.0	523.6	668.5	13.9%
Rest of World	135.3	208.9	162.4	230.3	445.8	34.7%
Total Fab Equip.	3,519.5	3,356.4	2,713.1	3,147.5	4,894.3	8.6%

N/A = Not Applicable

Source: Dataquest
July 1989
Ref: SUMMREG

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Wafer Fab Equipment--Summary Data by Category

Table 2

Worldwide Wafer Fab Equipment Market
Company Shares by Category
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Fab Equipment Market	3,519.5	3,356.4	2,713.1	3,147.5	4,894.3	8.6%
Lithography						
Contact/Proximity						
U.S. Companies	0	0	0	0	0	N/A
Japanese Companies	50.0	30.3	15.4	11.1	8.7	(35.4%)
European Companies	17.0	17.5	16.0	12.4	12.0	(8.3%)
Total Cont./Prox.	67.0	47.8	31.4	23.5	20.7	(25.4%)
Projection Aligners						
U.S. Companies	151.2	138.4	121.8	88.0	90.0	(12.2%)
Japanese Companies	84.6	127.7	49.2	40.6	69.1	(4.9%)
European Companies	0	0	0	0	0	N/A
Total Projection	235.8	266.1	171.0	128.6	159.1	(9.4%)
Steppers						
U.S. Companies	326.9	217.0	154.2	124.5	198.0	(11.8%)
Japanese Companies	196.7	210.5	199.8	341.9	646.5	34.6%
European Companies	2.7	2.8	9.1	36.7	58.6	115.8%
Total Steppers	526.3	430.3	363.1	503.1	903.1	14.5%
Direct-Write E-Beam						
U.S. Companies	1.1	0	6.4	9.6	12.8	84.7%
Japanese Companies	19.9	19.5	41.2	39.5	40.7	19.6%
European Companies	7.8	11.2	20.5	18.0	14.0	15.7%
Total Direct-Write	28.8	30.7	68.1	67.1	67.5	23.7%

(Continued)

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Table 2 (Continued)

Worldwide Wafer Fab Equipment Market
Company Shares by Category
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Maskmaking E-Beam						
U.S. Companies	49.3	64.8	36.0	27.0	27.0	(14.0%)
Japanese Companies	16.6	13.9	14.7	35.0	6.2	(0.6%)
European Companies	5.7	2.6	0	4.0	5.0	(3.2%)
Total E-Beam M/M	71.6	81.3	50.7	66.0	48.2	(9.4%)
Maskmaking Optical Laser						
U.S. Companies	0	0	0	1.6	11.2	N/A
Japanese Companies	0	0	0	0	0	N/A
European Companies	0	0	0	0	0	N/A
Total Laser M/M	0	0	0	1.6	11.2	N/A
X-Ray						
U.S. Companies	0.8	0.8	0.8	0	1.8	N/A
Japanese Companies	0	0	0	0	0	N/A
European Companies	1.0	1.0	0	0	7.2	(10.4%)
Total X-Ray	1.8	1.8	0.8	0	9.0	N/A
Total Lithography						
U.S. Companies	529.3	421.0	319.2	250.7	340.8	(10.4%)
Japanese Companies	367.8	401.9	320.3	468.1	781.2	20.7%
European Companies	34.2	35.1	45.6	71.1	96.8	29.7%
Total Lithography	931.3	858.0	685.1	789.9	1,218.8	7.0%
Automatic Photoresist Processing Equipment						
U.S. Companies	114.7	93.3	81.0	80.2	93.4	(5.0%)
Japanese Companies	65.8	60.5	58.4	73.0	142.5	21.3%
European Companies	3.0	3.8	6.4	10.9	13.8	46.5%
Total Track	183.5	157.6	145.8	164.1	249.7	8.0%

(Continued)

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Table 2 (Continued)

Worldwide Wafer Fab Equipment Market
Company Shares by Category
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Wet Process						
U.S. Companies	94.1	99.8	90.9	96.4	115.8	5.3%
Japanese Companies	75.4	55.4	67.9	64.3	114.6	11.0%
European Companies	2.2	2.0	3.1	4.3	4.7	20.9%
Total Wet Process	171.7	157.2	161.9	165.0	235.1	8.2%
Dry Strip						
U.S. Companies	31.0	22.6	20.0	22.1	34.4	2.6%
Japanese Companies	12.6	14.9	14.4	29.6	55.1	44.6%
European Companies	1.0	1.0	0	0	0	(100.0%)
Total Dry Strip	44.6	38.5	34.4	51.7	89.5	19.0%
Dry Etch						
U.S. Companies	211.8	202.6	176.1	210.3	372.6	15.2%
Japanese Companies	76.2	88.1	56.0	89.9	160.3	20.4%
European Companies	10.3	8.9	5.0	7.2	14.1	8.2%
Total Dry Etch	298.3	299.6	237.1	307.4	547.0	16.4%
Deposition						
CVD						
U.S. Companies	114.9	117.7	83.9	128.4	266.9	23.5%
Japanese Companies	64.9	60.6	55.3	48.0	89.1	8.2%
European Companies	48.2	68.2	80.2	78.0	99.0	19.7%
Total CVD	228.0	246.5	219.4	254.4	455.0	18.9%
PVD						
U.S. Companies	121.1	133.1	113.5	102.0	132.4	2.3%
Japanese Companies	68.6	75.6	75.2	97.8	139.4	19.4%
European Companies	43.8	54.3	47.9	49.2	42.9	(0.5%)
Total PVD	233.5	263.0	236.6	249.0	314.7	7.7%

(Continued)

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Table 2 (Continued)

Worldwide Wafer Fab Equipment Market
Company Shares by Category
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Silicon Epitaxy						
U.S. Companies	100.9	63.4	42.7	33.4	66.2	(10.0%)
Japanese Companies	10.9	8.1	3.6	2.1	6.2	(13.2%)
European Companies	0	0	0	0	12.1	N/A
Total Silicon Epi.	111.8	71.5	46.3	35.5	84.5	(6.8%)
Metalorganic CVD						
U.S. Companies	3.2	6.4	8.9	10.2	12.8	41.4%
Japanese Companies	9.3	11.2	15.8	14.4	17.4	17.0%
European Companies	5.0	7.2	7.4	11.0	12.3	25.2%
Total MOCVD	17.5	24.8	32.1	35.6	42.5	24.8%
Molecular Beam Epitaxy						
U.S. Companies	9.6	13.2	18.0	17.1	20.3	20.6%
Japanese Companies	6.4	12.3	18.2	19.9	27.6	44.1%
European Companies	25.4	27.9	33.0	34.3	37.5	10.2%
Total MBE	41.4	53.4	69.2	71.3	85.4	19.8%
Total Deposition						
U.S. Companies	349.7	333.8	267.0	291.1	498.6	9.3%
Japanese Companies	160.1	167.8	168.1	182.2	279.7	15.0%
European Companies	122.4	157.6	168.5	172.5	203.8	13.6%
Total Deposition	632.2	659.2	603.6	645.8	982.1	11.6%
Diffusion						
U.S. Companies	90.7	97.7	63.3	65.3	114.3	6.0%
Japanese Companies	83.8	89.4	73.5	86.4	124.1	10.3%
European Companies	14.4	20.1	18.8	21.5	27.4	17.4%
Total Diffusion	188.9	207.2	155.6	173.2	265.8	8.9%

(Continued)

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Table 2 (Continued)

Worldwide Wafer Fab Equipment Market
Company Shares by Category
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Rapid Thermal Processing						
U.S. Companies	8.2	11.1	11.9	16.3	18.7	22.9%
Japanese Companies	2.2	2.8	2.5	1.2	2.1	(1.2%)
European Companies	0.4	0.4	0.7	1.0	1.2	31.6%
Total RTP	10.8	14.3	15.1	18.5	22.0	19.5%
Ion Implantation						
U.S. Companies	222.0	222.4	87.9	131.1	244.8	2.5%
Japanese Companies	60.3	71.0	30.9	52.0	129.9	21.1%
European Companies	6.0	0	0	2.8	4.2	(8.5%)
Total Implantation	288.3	293.4	118.8	185.9	378.9	7.1%
Optical CD/Wafer Inspection Equipment						
U.S. Companies	31.3	28.2	36.9	45.8	90.8	30.5%
Japanese Companies	20.8	14.7	22.1	29.2	47.4	22.9%
European Companies	10.5	11.6	11.8	23.6	35.2	35.3%
Total CD/Wafer	62.6	54.5	70.8	98.6	173.4	29.0%
Subtotal Fab Equipment*						
U.S. Companies	1,682.8	1,532.5	1,154.2	1,209.3	1,924.2	3.4%
Japanese Companies	925.0	966.5	814.1	1,075.9	1,836.9	18.7%
European Companies	204.4	240.5	259.9	314.9	401.2	18.4%
Subtotal	2,812.2	2,739.5	2,228.2	2,600.1	4,162.3	10.3%
Ion Milling						
All Companies	8.3	6.5	6.8	6.8	8.0	(0.9%)
Other Process Control						
All Companies	445.9	368.0	302.7	332.1	427.0	(1.1%)

(Continued)

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Wafer Fab Equipment--Summary Data by Category

Table 2 (Continued)

Worldwide Wafer Fab Equipment Market
Company Shares by Category
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Factory Automation						
All Companies	130.0	125.0	81.0	99.0	130.0	0
Other Equipment						
All Companies	123.1	117.4	94.4	109.5	167.0	7.9%
Total Fab Equip.	3,519.5	3,356.4	2,713.1	3,147.5	4,894.3	8.6%

*Subtotal Fab Equipment does not include Ion Milling, Other Process Control, Factory Automation, and Other Equipment categories because detailed company data is not complete for these categories. Aggregate data for these categories are added to provide a consistent total for the worldwide wafer fab equipment market.

N/A = Not Applicable

Source: Dataquest
July 1989
Ref: SUMMSHR

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Introduction to the Wafer Fab Equipment Data Base

Dataquest's Semiconductor Equipment and Materials Service (SEMS) is publishing its 1988 Wafer Fab Equipment Data Base. This data base is the result of an extensive research project conducted by SEMS whereby we contact the world's wafer fab equipment manufacturers to obtain detailed regional and company market share data.

Dataquest has organized the wafer fab equipment market into 11 major categories of front-end processing equipment. These categories, along with key subcategories, are shown in Table 1.

Table 1

Wafer Fab Equipment Categories

1. Lithography

   Contact/Proximity
   Projection Aligners
   Steppers
   Direct-Write E-Beam
   Maskmaking E-Beam
   Maskmaking Optical Laser
   X-Ray

2. Automatic Photoresist Processing Equipment

3. Etch and Clean

   Wet Process
   Dry Strip
   Dry Etch
   Ion Milling

4. Deposition

   Chemical Vapor Deposition
   Physical Vapor Deposition
   Silicon Epitaxy
   Metalorganic CVD
   Molecular Beam Epitaxy

5. Diffusion

6. Rapid Thermal Processing

(Continued)

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Table 1 (Continued)

Wafer Fab Equipment Categories

7. Ion Implantation

   Medium Current
   High Current
   High Voltage

8. Optical CD/Wafer Inspection

9. Other Process Control

10. Factory Automation

11. Other Equipment

Source: Dataquest
July 1989

Dataquest estimates the capital spending by the world's merchant and captive semiconductor manufacturers and publishes this estimate in this binder, behind the "Forecast" tab. We consider capital spending to consist of three components: spending for front-end, or wafer fab equipment; spending for back-end, or assembly and test equipment; and spending for property and plant. Thus, the total world market for the 11 categories of wafer fab equipment defined above should be equal to the total capital spending for front-end equipment by the world's semiconductor manufacturers.

Most of the equipment categories are self-explanatory; however, a few categories require further definition. The Other Process Control category represents a broad market that includes mask inspection and repair equipment, process monitoring equipment, surface analysis equipment, and analytical instrumentation. This market is a highly fragmented market with dozens of companies selling into a multitude of noncompetitive market niches.

Factory Automation includes CIM software for shop floor control, factory host computer systems, cell controllers and interface hardware, and wafer transport systems including automatic guided vehicles, robotics, and rail transport systems.

Other Equipment is a general, catch-all category that includes the other capital equipment used throughout the fab but not classified with the other nine major types of wafer processing equipment. Included in this segment are decontamination systems, wafer markers, gas analyzers, storage stations, and other types of equipment.

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Introduction to the Wafer Fab Equipment Data Base

CONVENTIONS

The data in the tables represent calendar year shipments, organized by company or by region. For companies with a different fiscal year, calendar year shipments have been estimated. Shipments do not include spare parts or service but do include retrofits and upgrades. Thus, for public companies, the sales reported here may be different from the sales reported in the annual reports. The compound annual growth rate (CAGR) is estimated over the years 1984 to 1988 for each major line item.

EXCHANGE RATES

Japanese-manufactured equipment sold in Japan is valued in dollars in the data base tables at the average exchange rate for each year, as shown below:

Yen/Dollar Exchange Rate

1984	1985	1986	1987	1988
237	238	167	144	130

It should be noted that Japanese equipment sold in Japan in 1986 reflects the high yen appreciation rate rather than a true increase in the total market.

EQUIPMENT COMPANIES

Table 2 presents a list of the equipment companies found in the data base tables by region of company ownership. The data base comprises a total of 81 U.S. equipment companies, 54 Japanese companies, and 30 European companies. These 165 companies account for virtually all of the world's wafer processing equipment for lithography, automatic photoresist processing, etch and clean, deposition, diffusion, rapid thermal processing, ion implantation, and optical CD/wafer inspection.

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Table 2

Equipment Companies

North American Companies	Japanese Companies	European Companies
AG Associates	Alcan Tech	Advanced Semiconductor Materials
Alameda Instruments	Amaya	Aixtron
American Semiconductor Equipment Technology	Anelva	ASM Lithography
Applied Materials	Canon	Balzers
Ateq	Chororin Engineering	Cambridge Instruments
Athens	Daiwa Semiconductor	Centrotherm
Automatic Cleaning Technology	Denko	Convac
Branson/IPC	Dainippon Screen	CVT
BTU/Bruce	Disco	E.T. Electrotech
CFM Technology	Eiko	Edwards High Vacuum
CHA Industries	Elionix	EEV
Circuits Processing Apparatus	Enya	Heidelberg Instruments
Crystal Specialties	Ergo Plasma Systems	Helmut Seier
CVC Products	Hitachi	HVE Europa
CVD Equipment	Hohkoh Sangyo	Isa Riber
Denton Vacuum	Japan Production Eng.	Karl Suss
Dexon	JEOL	Leybold-Heraeus
Drytek	Kaijo Denki	LPE
Eaton	Kokusai	Micro-Controle
Emcore	Koyo Lindberg	Pokorny
Epitaxy, Inc.	Kuwano Electric	Semco Engineering
Estek	Musashi	Sitesa
Focus Semiconductor	Nidek	Technics
FSI International	Nikon	Temescal
Gasonics	Nippon EMC	Thomas Schwonn
GCA	Nippon Sanso	VG Instruments
Gemini	Nissin High Voltage	Vickers Instrument
Genus	Olympus	Wellman Furnaces
Hampshire Instruments	Plasma Systems	Wild Leitz
Innotec	Ramco	Zeiss
Insystems	Ryokosha	
Integrated Air Systems	Samco	
Ion Tech	Sankyo Engineering	
	Seiden Sha	

(Continued)

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Table 2 (Continued)

Equipment Companies

North American Companies	Japanese Companies	European Companies
IVS Inc.	Seiko	
KLA	Shimada	
LAM Research	Sinko Seiki	
Kurt J. Lesker	SPC Electronics	
LFE	Sugai	
Machine Technology	Sumitomo	
March Instruments	Tazmo	
Materials Research	TEL/Lam	
Matrix	TEL/Thermco	
Micronix	TEL/Varian	
Nanometrics	Tokuda	
Nanosil	Tokyo Electron Ltd.	
National Electrostatics	Tokyo Ohka	
Novellus	Toshiba	
Optical Specialties, Inc.	Toyoko Chemical	
Pacific Western	Ulvac	
Peak Systems	Ulvac/BTU	
Perkin-Elmer	Ushio	
Plasma-Therm	Yawata	
Poly-Flow Engineering		
Process Products		
Process Technology		
Pure Aire Corp.		
Reichert-McBain		
S&K Products International		
Santa Clara Plastics		
SCI Manufacturing		
Semiconductor Systems, Inc.		
Semifab		
Semitherm		
Semitool		
Silicon Valley Group		
Siscan		
Solitec		
Spectrum CVD		
Spire		

(Continued)

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Table 2 (Continued)

Equipment Companies

North American Companies	Japanese Companies	European Companies
Sputtered Films		
Tamarack Scientific		
Tegal		
Tempress		
Thermco		
Tylan		
Ultratech		
Universal Plastics		
Varian		
Veeco		
Verteq		
Watkins-Johnson		

Source: Dataquest
July 1989

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Wafer Fab Equipment--Import/Export Data

This section of the equipment data base consists of two summary tables that provide information on the import/export markets for the worldwide wafer fab equipment market. In both Table 1 and Table 2, the worldwide fab equipment market total in millions of dollars is listed at the beginning of the table and followed by the subtotal for fab equipment. The subtotal fab equipment line item includes all of the front-end equipment categories for which detailed company analysis has been made and accounts for 85 percent of all front-end equipment for 1988. For some equipment categories (Ion Milling, Process Control, Factory Automation, and Other Equipment), detailed company analysis is not yet complete. For these categories, which account for the remaining 15 percent of wafer fab equipment, a top-down estimate has been made and included in Tables 1 and 2 so that worldwide fab equipment sales are consistent across all tables.

The subtotal fab equipment market includes all of the major wafer fab equipment categories and accounts for the majority of all import/export activity in the worldwide fab equipment market. Relatively little import/export activity exists for the remaining 15 percent of wafer fab equipment for which detailed company data are not yet complete. These equipment markets are largely supplied by domestic suppliers. Significant import/export analysis of the fab equipment market can be done, however, with the aid of the data in Tables 1 and 2.

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Wafer Fab Equipment--Import/Export Data

Table 1

Worldwide Wafer Fab Equipment Market
Import Data
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Fab Equipment Market	3,519.5	3,356.4	2,713.1	3,147.5	4,894.3	8.6%
Subtotal Fab Equip.*	2,812.2	2,739.5	2,228.2	2,600.1	4,162.3	10.3%
Subtotal Percent	79.9%	81.6%	82.1%	82.6%	85.0%	
United States						
U.S. Co. Sales	1,036.1	880.6	716.2	692.0	1,013.5	(0.5%)
Japanese Co. Sales	70.2	78.4	78.5	117.5	173.7	25.4%
European Co. Sales	80.0	85.2	87.4	106.5	143.3	15.7%
Total U.S. Market	1,186.3	1,044.2	882.1	916.0	1,330.5	2.9%
Japan						
U.S. Co. Sales	350.7	258.2	136.6	168.5	371.8	1.5%
Japanese Co. Sales	813.1	833.6	661.2	846.4	1,458.8	15.7%
European Co. Sales	26.5	36.9	37.9	38.1	48.5	16.3%
Total Japan Market	1,190.3	1,128.7	835.7	1,053.0	1,879.1	12.1%
Europe						
U.S. Co. Sales	219.7	257.9	212.1	238.5	315.8	9.5%
Japanese Co. Sales	19.0	28.3	40.5	51.9	72.3	39.7%
European Co. Sales	85.5	104.9	122.0	151.7	182.5	20.9%
Total Europe Market	324.2	391.1	374.6	442.1	570.6	15.2%
Rest of World (ROW)						
U.S. Co. Sales	76.3	135.8	89.3	110.3	223.1	30.8%
Japanese Co. Sales	22.7	26.2	33.9	60.1	132.1	55.3%
European Co. Sales	12.4	13.5	12.6	18.6	26.9	21.4%
Total ROW Market	111.4	175.5	135.8	189.0	382.1	36.1%
Worldwide						
U.S. Co. Sales	1,682.8	1,532.5	1,154.2	1,209.3	1,924.2	3.4%
Japanese Co. Sales	925.0	966.5	814.1	1,075.9	1,836.9	18.7%
European Co. Sales	204.4	240.5	259.9	314.9	401.2	18.4%
Subtotal Fab Equip.	2,812.2	2,739.5	2,228.2	2,600.1	4,162.3	10.3%

(Continued)

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Table 1 (Continued)

Worldwide Wafer Fab Equipment Market
Import Data
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Ion Milling						
All Companies	8.3	6.5	6.8	6.8	8.0	(0.9%)
Process Control						
All Companies	445.9	368.0	302.7	332.1	427.0	(1.1%)
Factory Automation						
All Companies	130.0	125.0	81.0	99.0	130.0	0
Other Equipment						
All Companies	123.1	117.4	94.4	109.5	167.0	7.9%
Total Fab Equipment	3,519.5	3,356.4	2,713.1	3,147.5	4,894.3	8.6%

*Subtotal Fab Equipment does not include Wet Process, Ion Milling, Process Control, Factory Automation, and Other Equipment categories, as detailed company data are not complete for these categories. Aggregate data for these categories are added to provide a consistent total for the worldwide wafer fab equipment market.

Source: Dataquest
July 1989
Ref: EXIMSHR

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Table 2

Worldwide Wafer Fab Equipment Market
Export Data
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
World Fab Equipment Market	3,519.5	3,356.4	2,713.1	3,147.5	4,894.3	8.6%
Subtotal Fab Equip.*	2,812.2	2,739.5	2,228.2	2,600.1	4,162.3	10.3%
Subtotal Percent	79.9%	81.6%	82.1%	82.6%	85.0%	
U.S. Equipment Companies						
Sales in U.S.	1,036.1	880.6	716.2	692.0	1,013.5	(0.5%)
Sales in Japan	350.7	258.2	136.6	168.5	371.8	1.5%
Sales in Europe	219.7	257.9	212.1	238.5	315.8	9.5%
Sales in ROW	76.3	135.8	89.3	110.3	223.1	30.8%
Total U.S. Cos.	1,682.8	1,532.5	1,154.2	1,209.3	1,924.2	3.4%
Japanese Equip. Cos.						
Sales in U.S.	70.2	78.4	78.5	117.5	173.7	25.4%
Sales in Japan	813.1	833.6	661.2	846.4	1,458.8	15.7%
Sales in Europe	19.0	28.3	40.5	51.9	72.3	39.7%
Sales in ROW	22.7	26.2	33.9	60.1	132.1	55.3%
Total Japanese Cos.	925.0	966.5	814.1	1,075.9	1,836.9	18.7%
European Equip. Companies						
Sales in U.S.	80.0	85.2	87.4	106.5	143.3	15.7%
Sales in Japan	26.5	36.9	37.9	38.1	48.5	16.3%
Sales in Europe	85.5	104.9	122.0	151.7	182.5	20.9%
Sales in ROW	12.4	13.5	12.6	18.6	26.9	21.4%
Total European Cos.	204.4	240.5	259.9	314.9	401.2	18.4%
Subtotal Fab Equip.	2,812.2	2,739.5	2,228.2	2,600.1	4,162.3	10.3%
Ion Milling						
All Companies	8.3	6.5	6.8	6.8	8.0	(0.9%)
Other Process Control						
All Companies	445.9	368.0	302.7	332.1	427.0	(1.1%)
Factory Automation						
All Companies	130.0	125.0	81.0	99.0	130.0	0

(Continued)

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Table 2 (Continued)

Worldwide Wafer Fab Equipment Market
Export Data
(Millions of Dollars)

	1984	1985	1986	1987	1988	CAGR 1984-1988
Other Equipment						
All Companies	123.1	117.4	94.4	109.5	167.0	7.9%
Total Fab Equip.	3,519.5	3,356.4	2,713.1	3,147.5	4,894.3	8.6%

*Subtotal Fab Equipment does not include Ion Milling, Other Process Control, Factory Automation, and Other Equipment categories as detailed company data is not complete for these categories. Aggregate data for these categories are added to provide a consistent total for the worldwide wafer fab equipment market.

Source: Dataquest
July 1989
Ref: EXIMSHR

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Wafer Fab Equipment--Company Rankings

This section of the wafer fab equipment data base presents the ranking of wafer fab equipment manufacturers by 1988 revenue, as shown in Table 1. Line 1 in the table shows the total worldwide wafer fab equipment market. Individual company data shown in the table represent 85 percent of the 1988 total wafer fab equipment market of approximately $4,894 million. The companies listed here represent virtually all worldwide industry sales in the key front-end equipment categories of lithography, automatic photoresist processing, etch and clean, deposition, diffusion, ion implantation, and CD/wafer inspection. The remaining 15 percent of the total worldwide wafer fab equipment includes other process control, factory automation, and other front-end equipment. Company sales for these categories are not included in the table.

Table 1 includes only company sales of front-end equipment; it does not include company sales of assembly and test equipment. For instance, back-end equipment sales by General Signal or ASM International are not included. Likewise, KLA's CD/wafer inspection equipment sales only are included; KLA's sales of mask inspection equipment are not.

The revenue reported in Table 1 is for the calendar year and includes system sales, upgrades, and retrofits, but it does not include service and spare parts. Thus, the revenue reported here will differ from each company's sales as reported in its financial statements.

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Wafer Fab Equipment--Company Rankings

Table 1

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
World Fab Equipment Market	3,519.5	3,356.4	2,713.1	3,147.5	4,894.3	
Nikon						1
Steppers	170.4	157.6	128.4	218.8	457.3	
CD/wafer inspection	10.5	7.4	8.7	13.3	29.1	
Total	180.9	165.0	137.1	232.1	486.4	
Applied Materials						2
Dry etch	69.0	69.6	74.0	102.0	196.7	
Silicon epitaxy	70.0	44.0	31.3	18.6	47.2	
APCVD	11.9	9.9	7.8	8.6	15.7	
PECVD	8.3	6.3	6.1	31.8	75.4	
LPCVD	0	0	0	0	0	
Ion implantation	0	0	4.4	10.0	24.9	
Total	159.2	129.8	123.6	171.0	359.9	
General Signal						3
GCA						
Steppers	202.8	114.2	74.6	47.4	104.0	
Resist process. equip.	25.5	15.0	12.3	7.0	5.5	
Dry etch	0	0.8	2.0	4.0	5.0	
Total	228.3	130.0	88.9	58.4	114.5	
Ultratech						
Steppers	63.0	50.7	38.9	40.6	73.0	
Drytek						
Dry etch	24.0	23.0	16.0	17.0	25.0	
Dry strip	3.0	3.0	2.0	1.0	1.2	
Total	27.0	26.0	18.0	18.0	26.2	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
General Signal (Continued)						
Semiconductor Systems Inc.						
Resist process. equip.	13.0	8.8	8.8	10.8	22.0	
Tempress						
Diffusion	0	6.0	2.0	0.5	4.3	
LPCVD	5.9	7.6	3.8	0	3.8	
APCVD	3.6	2.1	2.2	0	1.8	
Total Tempress	9.5	15.7	8.0	0.5	9.9	
Circuits Proc. Apparatus						
Sputtering	3.0	4.5	2.9	3.0	2.6	
Total General Signal	343.8	235.7	165.5	131.3	248.2	
Tokyo Electron Limited						4
Resist processing equip.	26.2	24.5	25.6	36.2	86.0	
Diffusion	47.2	60.0	49.0	56.3	88.0	
LPCVD	12.8	16.0	7.6	8.7	16.8	
Dry Etch	7.4	10.5	6.0	17.4	45.8	
Metalorganic CVD	2.3	2.3	3.0	2.9	1.7	
Rapid thermal processing	0.4	0.4	0.4	0	0.3	
Total	96.3	113.7	91.6	121.5	238.6	
Canon						5
Projection aligners	84.6	127.7	49.2	40.6	69.1	
Steppers	12.7	35.0	63.2	89.8	140.0	
Contact/proximity	50.0	30.3	15.4	11.1	8.7	
Resist processing equip.	0	0	0.5	1.0	3.8	
CD/Wafer inspection	2.0	1.3	1.4	2.0	3.0	
Total	149.3	194.3	129.7	144.5	224.6	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Varian Associates						6
Sputtering	52.1	57.1	56.7	48.3	61.3	
Ion implantation	95.4	101.5	33.7	40.5	69.1	
Molecular beam epitaxy	6.9	7.2	10.8	12.1	17.5	
Dry etch	15.0	8.0	4.0	0	0	
LPCVD	0	0	1.1	7.5	11.8	
Rapid thermal processing	0.6	0.4	0.4	0.9	0.4	
E-beam	2.9	0	0	0	0	
Total	172.9	174.2	106.7	109.3	160.1	
Eaton						7
Ion implantation	114.5	109.8	45.9	78.8	135.2	
Resist processing equip.	14.5	12.0	12.0	10.5	11.0	
Steppers	29.1	21.8	2.1	0	0	
Rapid thermal processing	1.5	1.4	0.7	0.2	0.4	
Total	159.6	145.0	60.7	89.5	146.6	
Perkin-Elmer						8
Projection aligners	151.2	138.4	121.8	88.0	90.0	
E-beam	47.5	64.8	42.4	36.6	39.8	
Steppers	21.8	22.2	27.0	25.2	5.0	
Dry etch	15.6	19.5	9.2	0	0	
Molecular beam epitaxy	2.7	6.0	7.2	5.0	2.8	
Sputtering	12.8	9.9	5.6	3.1	0.9	
CD/wafer inspection	0	0	0	0	2.9	
X-ray	0	0	0	0	0	
Total	251.6	260.8	213.2	157.9	141.4	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Anelva						9
Sputtering	27.0	30.8	21.8	42.9	68.3	
Dry etch	28.4	39.4	16.2	22.3	41.6	
Molecular beam epitaxy	2.5	6.3	7.2	9.7	15.8	
Evaporation	1.4	0.4	2.3	1.8	1.4	
LPCVD	0	0	0	0.7	2.3	
PECVD	0	0	0.6	1.0	0	
Total	59.3	76.9	48.1	78.4	129.4	
Hitachi						10
E-beam	7.4	11.0	11.2	22.1	13.1	
Steppers	13.6	17.9	8.2	33.3	49.2	
Dry etch	4.9	3.6	10.8	18.8	34.6	
Dry strip	0	0	0	0.7	4.6	
Ion implantation	3.4	4.2	3.2	3.8	9.6	
CD/wafer inspection	0	0	4.1	6.0	1.7	
APCVD	0.6	0.3	0.4	0	0.2	
Total	29.9	37.0	37.9	84.7	113.0	
Ulvac						11
Sputtering	18.2	22.6	25.4	34.0	48.7	
Evaporation	16.9	16.8	22.4	8.0	14.0	
Ion implantation	12.0	8.4	5.7	7.3	11.3	
Molecular beam epitaxy	3.4	4.2	7.8	7.6	9.2	
PECVD	2.7	2.9	3.0	2.8	4.4	
LPCVD	0	0	1.2	1.4	3.8	
Dry etch	4.9	4.7	3.9	5.7	8.3	
Metalorganic CVD	1.5	1.9	2.7	2.4	3.8	
Total	59.6	61.5	72.1	69.2	103.5	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Advanced Semiconductor Materials						12
Diffusion	12.5	17.9	16.6	18.5	22.7	
LPCVD	8.7	13.9	20.5	19.9	25.8	
PECVD	33.1	40.4	44.4	44.5	51.6	
Silicon epitaxy	0	0	0	0	3.1	
Total	54.3	72.2	81.5	82.9	103.2	
Dainippon Screen						13
Resist processing equip.	38.4	34.9	29.8	31.2	47.0	
Wet process	25.4	15.9	20.6	21.7	37.8	
Rapid thermal processing	1.3	1.9	1.8	1.0	1.2	
Total	65.1	52.7	52.2	53.9	86.0	
Lam Research						14
Dry Etch	28.0	34.0	26.0	32.0	65.0	
Silicon Epitaxy	30.9	19.4	11.4	14.8	19.0	
Total	58.9	53.4	37.4	46.8	84.0	
TEL/Varian						15
Ion implantation	27.4	36.9	10.2	25.2	76.6	
Thermco						16
Diffusion	42.6	45.1	27.6	34.9	60.0	
LPCVD	7.7	9.1	6.4	6.6	6.5	
Total	50.3	54.2	34.0	41.5	66.5	
ASM Lithography						17
Steppers	2.7	2.8	9.1	36.7	58.6	
E-beam	1.8	1.9	6.0	12.0	6.0	
Total	4.5	4.7	15.1	48.7	64.6	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Tegal						18
Dry etch	38.0	25.0	25.6	35.6	55.0	
Dry strip	8.0	3.0	2.0	2.4	2.0	
Total	46.0	28.0	27.6	38.0	57.0	
KLA Instruments						19
CD/Wafer Inspection	0	11.2	18.1	27.6	54.2	
Silicon Valley Group						20
Resist processing equip.	33.1	30.5	25.6	33.0	37.4	
Diffusion	0	0	0.2	1.1	4.0	
LPCVD	16.8	15.6	9.0	5.3	7.6	
Total	49.9	46.1	34.8	39.4	49.0	
BTU/Bruce						21
Diffusion	35.7	36.2	24.0	19.3	34.0	
LPCVD	4.0	6.7	5.6	7.9	14.5	
Total	39.7	42.9	29.6	27.2	48.5	
Genus						22
LPCVD	16.0	17.5	7.5	13.2	33.4	
Ion implantation	0	0	0	0	14.4	
Total	16.0	17.5	7.5	13.2	47.8	
Materials Research Corp.						23
Sputtering	34.8	37.8	21.9	23.1	34.0	
Dry etch	1.4	4.8	4.1	4.4	13.0	
Total	36.2	42.6	26.0	27.5	47.0	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
E.T. Electrotech						24
PECVD	6.4	13.6	15.3	13.3	20.3	
Dry etch	10.3	8.9	5.0	7.2	14.1	
Sputtering	5.5	8.7	5.3	6.0	9.0	
Dry strip	1.0	1.0	0	0	0	
Total	23.2	32.2	25.6	26.5	43.4	
Kokusai Electric						25
LPCVD	16.9	14.6	17.6	11.1	14.2	
Diffusion	25.3	17.3	13.8	19.2	20.3	
Dry etch	11.5	10.4	3.3	1.4	1.5	
Silicon epitaxy	6.3	5.0	2.1	1.5	4.2	
APCVD	1.5	0.7	0.7	0	0	
Rapid thermal processing	0.1	0.1	0	0	0	
Total	61.6	48.1	37.5	33.2	40.2	
JEOL						26
E-beam	20.3	22.4	41.7	48.9	36.1	
Watkins-Johnson						27
APCVD	4.8	5.9	8.1	16.0	36.0	
Nissin High Voltage						28
Ion Implantation	17.5	21.5	11.8	15.7	32.4	
Tokyo Ohka						29
Dry etch	8.9	7.6	7.2	7.1	10.0	
Dry strip	8.0	8.9	5.2	9.2	19.9	
Total	16.9	16.5	12.4	16.3	29.9	
FSI International						30
Wet process	23.2	28.4	22.4	19.2	24.1	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Sankyo Engineering						31
Wet process	5.2	5.3	7.4	8.1	23.8	
Novellus						32
PECVD	0	0	0	3.6	23.7	
ISA Riber						33
Molecular beam epitaxy	17.2	14.4	13.6	19.3	21.0	
Wild Leitz						34
CD/Wafer Inspection	8.7	9.1	8.3	11.1	20.2	
Machine Technology Inc.						35
Resist processing equip.	20.3	17.8	12.9	12.7	10.0	
Dry strip	0	0.3	2.0	2.7	4.5	
Sputtering	0	0	0.9	3.0	5.0	
Total	20.3	18.1	15.8	18.4	19.5	
Karl Suss						36
Contact/proximity	17.0	17.5	16.0	12.4	12.0	
X-ray	1.0	1.0	0	0	7.2	
Total	18.0	18.5	16.0	12.4	19.2	
Plasma-Therm						37
Dry etch	12.0	13.0	11.0	13.7	12.9	
PECVD	5.7	5.6	5.8	4.6	6.0	
Total	17.7	18.6	16.8	18.3	18.9	
Balzers						38
Sputtering	12.2	10.1	13.2	13.9	11.0	
Evaporation	9.0	10.4	5.0	2.9	2.9	
Ion Implantation	6.0	0	0	2.8	4.2	
Total	27.2	20.5	18.2	19.6	18.1	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Toshiba Machine						39
Silicon epitaxy	2.1	2.3	1.0	0.6	2.0	
E-beam	8.8	0	3.0	3.5	7.7	
APCVD	0	0	4.3	5.0	8.3	
Total	10.9	2.3	8.3	9.1	18.0	
Amaya						40
APCVD	13.7	10.9	6.0	5.5	17.5	
VG Instruments						41
Molecular Beam Epitaxy	8.2	13.5	19.4	15.0	16.5	
American Semiconductor Equipment Technologies						42
Steppers	10.2	8.1	11.6	11.3	16.0	
Tokuda						43
Dry etch	8.7	9.6	4.3	9.4	8.8	
Sputtering	5.1	5.0	3.3	11.1	7.0	
Total	13.8	14.6	7.6	20.5	15.8	
Cambridge Instruments						44
E-beam	11.7	11.9	14.5	10.0	13.0	
Metalorganic CVD	3.5	4.1	3.6	3.3	2.7	
Total	15.2	16.0	18.1	13.3	15.7	
Solitec						45
Resist processing equip.	4.5	5.0	6.5	6.2	7.5	
LPCVD	9.4	12.9	5.3	3.6	8.0	
Diffusion	0.6	0	0.3	0	0	
Total	14.5	17.9	12.1	9.8	15.5	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Semitool						46
Wet process	18.2	16.9	15.9	18.8	15.4	
Branson/IPC						47
Dry strip	17.0	14.3	10.2	7.8	15.0	
Dry etch	8.8	4.9	4.2	1.6	0	
Total	25.8	19.2	14.4	9.4	15.0	
Kaijo Denki						48
Wet Process	13.7	10.0	13.5	10.1	14.6	
Santa Clara Plastics						49
Wet process	25.0	26.0	20.0	16.0	14.6	
CVC Products						50
Sputtering	8.1	9.5	13.5	9.7	12.3	
Evaporation	0	0	0	0	1.6	
Total	8.1	9.5	13.5	9.7	13.9	
Convac						51
Resist processing equip.	3.0	3.8	6.4	10.9	13.8	
Plasma Systems						52
Dry strip	4.2	3.2	3.3	5.4	10.4	
Dry etch	1.5	1.5	1.7	1.9	3.2	
Total	5.7	4.7	5.0	7.3	13.6	
Enya Seisakusho						53
Wet process	10.8	8.8	9.6	6.2	7.6	
PECVD	5.1	4.2	1.6	1.9	4.2	
LPCVD	2.9	1.3	1.0	0.6	1.8	
Total	18.8	14.3	12.2	8.7	13.6	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Kuwano Electric						54
Wet process	2.1	2.7	3.9	6.3	13.4	
Koyo Lindberg						55
Diffusion	9.7	10.3	7.8	5.7	6.8	
LPCVD	1.7	1.9	2.2	2.0	4.5	
Rapid thermal processing	0.1	0.1	0.3	0.2	0.6	
APCVD	1.5	0.6	0.4	0.2	1.3	
Total	13.0	12.9	10.7	8.1	13.2	
Gasonics						56
Diffusion	4.5	5.3	6.1	7.5	9.0	
Dry strip	0	0	0.7	2.0	3.0	
Total	4.5	5.3	6.8	9.5	12.0	
Verteq						57
Wet process	6.0	5.9	8.3	6.5	11.8	
Leybold-Heraeus						58
Sputtering	3.9	8.8	9.6	15.0	10.8	
Evaporation	5.0	4.0	3.0	1.5	0.5	
Total	8.9	12.8	12.6	16.5	11.3	
Ateq						59
Maskmaking optical laser	0	0	0	1.6	11.2	
AG Associates						60
Rapid thermal processing	6.1	8.8	9.6	10.8	10.6	
Insystems						61
CD/wafer inspection	0	0	0	2.2	9.8	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Ramco						62
Dry strip	0	1.7	4.5	8.7	9.6	
S&K Products International						63
Wet process	5.6	6.6	6.9	8.5	9.4	
Alcan Tech						64
Dry strip	0	0	0.9	5.0	9.2	
Vickers Instruments						65
CD/wafer inspection	0	0	0	8.3	9.0	
Temescal						66
Evaporation	6.4	10.2	10.5	9.9	8.7	
Sputtering	1.8	2.1	1.3	0	0	
Total	8.2	12.3	11.8	9.9	8.7	
Universal Plastics						67
Wet process	0	0.1	1.6	3.7	8.5	
Spectrum CVD						68
LPCVD	0	0	0.5	2.3	8.0	
SCI Manufacturing						69
Wet process	0	0	0	4.8	8.0	
Matrix						70
Dry strip	0	0	2.1	5.2	7.2	
Emcore						71
Metalorganic CVD	0	0.1	2.3	5.1	7.0	

(Continued)

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Wafer Fab Equipment—Company Rankings

Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
CHA Industries						72
Evaporation	5.7	7.1	5.6	6.0	6.3	
Sputtering	0.3	1.0	0.7	0.3	0.7	
Total	6.0	8.1	6.3	6.3	7.0	
Semifab						73
Wet process	6.1	4.8	6.4	7.7	7.0	
Nidek						74
CD/wafer inspection	2.0	1.7	2.2	3.1	6.7	
Aixtron						75
Metalorganic CVD	0	0.5	1.7	4.9	6.7	
Peak Systems						76
Rapid thermal processing	0	0	0.7	3.4	6.6	
Japan Production Engineering						77
PECVD	5.5	5.9	6.0	4.5	6.5	
Nippon Sanso						78
Metalorganic CVD	2.3	3.6	4.6	4.9	6.5	
Sugai						79
Wet process	4.7	3.9	3.7	4.5	6.4	
IVS Incorporated						80
CD/wafer inspection	0	0	0.5	1.5	6.4	
Ulvac/BTU						81
Diffusion	0.2	0.5	0.4	1.7	5.3	
LPCVD	0	0	0	0.5	1.0	
Total	0.2	0.5	0.4	2.2	6.3	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Pacific Western Systems						82
PECVD	12.5	8.7	6.9	7.9	6.2	
APCVD	1.6	1.4	1.2	0.2	0	
LPCVD	0.3	0.4	0.5	0	0	
Diffusion	1.8	1.1	0.6	0	0	
Total	16.2	11.6	9.2	8.1	6.2	
Sumitomo Metal						83
Dry etch	0	0	2.4	5.6	6.2	
Dexon						84
Wet process	1.7	3.5	3.1	3.1	5.9	
Tazmo						85
Resist processing equip.	1.2	1.1	2.5	4.6	5.7	
Sitesa						86
Silicon epitaxy	0	0	0	0	4.5	
Rapid thermal processing	0.4	0.4	0.7	1.0	1.2	
Total	0.4	0.4	0.7	1.0	5.7	
Innotec						87
Sputtering	0.4	2.6	1.8	2.4	4.2	
Evaporation	0.3	0.3	0.2	0	1.0	
Total	0.7	2.9	2.0	2.4	5.2	
Denko						88
Diffusion	1.4	1.0	1.8	2.0	2.7	
LPCVD	0	1.3	2.7	2.1	2.3	
Total	1.4	2.3	4.5	4.1	5.0	

(Continued)

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Wafer Fab Equipment--Company Rankings

Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
SiScan Systems						89
CD/wafer inspection	0	0	1.9	3.0	4.9	
Optical Specialties						90
CD/wafer inspection	15.6	10.0	7.2	5.3	4.8	
Pokorny						91
Wet process	2.2	2.0	3.1	4.3	4.7	
LPE						92
Silicon epitaxy	0	0	0	0	4.5	
Tylan						93
Diffusion	5.5	4.0	2.5	2.0	2.5	
LPCVD	2.0	2.3	0.7	4.0	1.5	
Total	7.5	6.3	3.2	6.0	4.0	
Wellman Furnaces						94
Diffusion	1.5	1.4	1.5	2.0	3.0	
LPCVD	0	0	0	0	1.0	
Total	1.5	1.4	1.5	2.0	4.0	
Process Technology Ltd.						95
LPCVD	4.4	5.7	5.4	4.3	4.0	
Athens						96
Wet process	0	0	0	1.0	4.0	
Heidelberg Instruments						97
CD/wafer inspection	0	0	0	1.6	3.4	
Pure Aire Corporation						98
Wet process	2.2	1.8	1.8	2.4	2.8	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Crystal Specialties						99
Metalorganic CVD	1.2	1.8	2.7	2.6	2.7	
Focus Semiconductor						100
LPCVD	0	0	0	1.0	2.5	
Ryokosha						101
CD/wafer inspection	2.2	1.4	1.5	1.4	2.5	
Nanometrics						102
CD/wafer inspection	6.7	2.3	1.5	1.7	2.3	
Spire						103
Metalorganic CVD	0.8	3.0	3.3	1.3	2.1	
Integrated Air Systems						104
Wet process	6.0	5.0	4.0	3.0	2.0	
Nippon FMC						105
Metalorganic CVD	0.8	1.1	1.5	1.4	1.9	
Hampshire Instruments						106
X-ray	0	0	0	0	1.8	
Zeiss						107
CD/wafer inspection	0	0.9	2.4	1.8	1.8	
LFE						108
Dry strip	3.0	2.0	1.0	1.0	1.5	
Seiko						109
Molecular beam epitaxy	0	0.8	2.0	1.2	1.4	
Chemitronics						110
Wet process	0	0	0	0	1.4	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Estek						111
CD/wafer inspection	0	0.3	0.2	0.1	0.2	
Wet process	0	0	0	1.2	1.1	
Total	0	0.3	0.2	1.3	1.3	
Eiko						112
Molecular beam epitaxy	0.5	1.0	1.2	1.4	1.2	
Toyoko Chemical						113
Metalorganic CVD	0	0.7	1.0	0.7	1.2	
National Electrostatics						114
Ion implantation	1.1	2.1	3.9	1.8	1.2	
Samco						115
Metalorganic CVD	1.1	0.7	1.0	1.1	1.2	
CVT						116
Metalorganic CVD	0.5	0.7	0.4	1.1	1.2	
Kurt J. Lesker						117
Sputtering	0.9	0.8	0.8	0.8	0.8	
Evaporation	0.2	0.5	0.3	0.3	0.3	
Total	1.1	1.3	1.1	1.1	1.1	
CVD Equipment						118
Metalorganic CVD	1.2	1.5	0.6	1.2	1.0	
Helmut Seier						119
Diffusion	0.2	0.6	0.5	0.5	0.7	
LPCVD	0	0.3	0	0.3	0.3	
Total	0.2	0.9	0.5	0.8	1.0	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Centrotherm						120
Diffusion	0.2	0.2	0.2	0.5	1.0	
CFM Technology						121
Wet process	0	0	0	0	1.0	
Semitherm						122
Diffusion	0	0	0	0	0.5	
LPCVD	0	0	0	0	0.5	
Total	0	0	0	0	1.0	
Disco						123
Diffusion	0	0.3	0.7	1.5	1.0	
Semco Engineering						124
Metalorganic CVD	0	0	0	0.3	0.9	
Thomas Schwonn						125
Metalorganic CVD	1.0	0.9	0.3	0.7	0.8	
Sputtered Films						126
Sputtering	2.0	1.0	1.6	1.0	0.6	
Seiden						127
Metalorganic CVD	1.3	0.9	1.3	0.6	0.6	
Shimada						128
Silicon epitaxy	2.5	0.8	0.5	0	0	
Wet process	1.1	0.6	0.6	0.5	0.6	
Metalorganic CVD	0	0	0.3	0	0	
Total	3.6	1.4	1.4	0.5	0.6	
Ion Tech						129
Sputtering	0.5	0.8	0.7	0.7	0.5	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Daiwa Semiconductor						130
Metalorganic CVD	0	0	0.4	0.4	0.5	
Process Products						131
Rapid thermal processing	0	0.5	0.5	0.7	0.4	
Denton Vacuum						132
Sputtering	0	0.1	0.1	0.1	0.1	
Evaporation	0	0.1	0.2	0.2	0.2	
Total	0	0.2	0.3	0.3	0.3	
Elionix						133
Dry etch	0	0	0.2	0.3	0.3	
Nanosil						134
Rapid thermal processing	0	0	0	0.3	0.3	
Poly-Flow Engineering						135
Wet process	0.1	0.8	0.5	0.5	0.2	
Veeco						136
Resist processing equip.	3.8	4.2	2.9	0	0	
Ion implantation	11.0	9.0	0	0	0	
Total	14.8	13.2	2.9	0	0	
EEV						137
Metalorganic CVD	0	1.0	1.4	0.7	0	
Hohkoh Sangyo						138
Dry strip	0.4	1.1	0.5	0.6	0	
Micronix						139
X-ray	0.8	0.8	0.8	0	0	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Reichert-McBain						140
CD/wafer inspection	0	0	3.0	0.3	0	
Ergo Plasma Systems						141
Dry etch	0	0.8	0	0	0	
Ushio						142
Rapid thermal processing	0.3	0.3	0	0	0	

Source: Dataquest
July 1989

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Wafer Fab Equipment--Company Rankings

This section of the wafer fab equipment data base presents the ranking of wafer fab equipment manufacturers by 1988 revenue, as shown in Table 1. Line 1 in the table shows the total worldwide wafer fab equipment market. Individual company data shown in the table represent 85 percent of the 1988 total wafer fab equipment market of approximately $4,894 million. The companies listed here represent virtually all worldwide industry sales in the key front-end equipment categories of lithography, automatic photoresist processing, etch and clean, deposition, diffusion, ion implantation, and CD/wafer inspection. The remaining 15 percent of the total worldwide wafer fab equipment includes other process control, factory automation, and other front-end equipment. Company sales for these categories are not included in the table.

Table 1 includes only company sales of front-end equipment; it does not include company sales of assembly and test equipment. For instance, back-end equipment sales by General Signal or ASM International are not included. Likewise, KLA's CD/wafer inspection equipment sales only are included; KLA's sales of mask inspection equipment are not.

The revenue reported in Table 1 is for the calendar year and includes system sales, upgrades, and retrofits, but it does not include service and spare parts. Thus, the revenue reported here will differ from each company's sales as reported in its financial statements.

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Wafer Fab Equipment--Company Rankings

Table 1

Semiconductor Wafer Fab Equipment Companies Ranked by Worldwide Sales (Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
World Fab Equipment Market	3,519.5	3,356.4	2,713.1	3,147.5	4,894.3	
Nikon						1
Steppers	170.4	157.6	128.4	218.8	457.3	
CD/wafer inspection	10.5	7.4	8.7	13.3	29.1	
Total	180.9	165.0	137.1	232.1	486.4	
Applied Materials						2
Dry etch	69.0	69.6	74.0	102.0	196.7	
Silicon epitaxy	70.0	44.0	31.3	18.6	47.2	
APCVD	11.9	9.9	7.8	8.6	15.7	
PECVD	8.3	6.3	6.1	31.8	75.4	
LPCVD	0	0	0	0	0	
Ion implantation	0	0	4.4	10.0	24.9	
Total	159.2	129.8	123.6	171.0	359.9	
General Signal						3
GCA						
Steppers	202.8	114.2	74.6	47.4	104.0	
Resist process. equip.	25.5	15.0	12.3	7.0	5.5	
Dry etch	0	0.8	2.0	4.0	5.0	
Total	228.3	130.0	88.9	58.4	114.5	
Ultratech						
Steppers	63.0	50.7	38.9	40.6	73.0	
Drytek						
Dry etch	24.0	23.0	16.0	17.0	25.0	
Dry strip	3.0	3.0	2.0	1.0	1.2	
Total	27.0	26.0	18.0	18.0	26.2	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
General Signal (Continued)						
Semiconductor Systems Inc.						
Resist process. equip.	13.0	8.8	8.8	10.8	22.0	
Tempress						
Diffusion	0	6.0	2.0	0.5	4.3	
LPCVD	5.9	7.6	3.8	0	3.8	
APCVD	3.6	2.1	2.2	0	1.8	
Total Tempress	9.5	15.7	8.0	0.5	9.9	
Circuits Proc. Apparatus						
Sputtering	3.0	4.5	2.9	3.0	2.6	
Total General Signal	343.8	235.7	165.5	131.3	248.2	
Tokyo Electron Limited						4
Resist processing equip.	26.2	24.5	25.6	36.2	86.0	
Diffusion	47.2	60.0	49.0	56.3	88.0	
LPCVD	12.8	16.0	7.6	8.7	16.8	
Dry Etch	7.4	10.5	6.0	17.4	45.8	
Metalorganic CVD	2.3	2.3	3.0	2.9	1.7	
Rapid thermal processing	0.4	0.4	0.4	0	0.3	
Total	96.3	113.7	91.6	121.5	238.6	
Canon						5
Projection aligners	84.6	127.7	49.2	40.6	69.1	
Steppers	12.7	35.0	63.2	89.8	140.0	
Contact/proximity	50.0	30.3	15.4	11.1	8.7	
Resist processing equip.	0	0	0.5	1.0	3.8	
CD/Wafer inspection	2.0	1.3	1.4	2.0	3.0	
Total	149.3	194.3	129.7	144.5	224.6	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Varian Associates						6
Sputtering	52.1	57.1	56.7	48.3	61.3	
Ion implantation	95.4	101.5	33.7	40.5	69.1	
Molecular beam epitaxy	6.9	7.2	10.8	12.1	17.5	
Dry etch	15.0	8.0	4.0	0	0	
LPCVD	0	0	1.1	7.5	11.8	
Rapid thermal processing	0.6	0.4	0.4	0.9	0.4	
E-beam	2.9	0	0	0	0	
Total	172.9	174.2	106.7	109.3	160.1	
Eaton						7
Ion implantation	114.5	109.8	45.9	78.8	135.2	
Resist processing equip.	14.5	12.0	12.0	10.5	11.0	
Steppers	29.1	21.8	2.1	0	0	
Rapid thermal processing	1.5	1.4	0.7	0.2	0.4	
Total	159.6	145.0	60.7	89.5	146.6	
Perkin-Elmer						8
Projection aligners	151.2	138.4	121.8	88.0	90.0	
E-beam	47.5	64.8	42.4	36.6	39.8	
Steppers	21.8	22.2	27.0	25.2	5.0	
Dry etch	15.6	19.5	9.2	0	0	
Molecular beam epitaxy	2.7	6.0	7.2	5.0	2.8	
Sputtering	12.8	9.9	5.6	3.1	0.9	
CD/wafer inspection	0	0	0	0	2.9	
X-ray	0	0	0	0	0	
Total	251.6	260.8	213.2	157.9	141.4	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Anelva						9
Sputtering	27.0	30.8	21.8	42.9	68.3	
Dry etch	28.4	39.4	16.2	22.3	41.6	
Molecular beam epitaxy	2.5	6.3	7.2	9.7	15.8	
Evaporation	1.4	0.4	2.3	1.8	1.4	
LPCVD	0	0	0	0.7	2.3	
PECVD	0	0	0.6	1.0	0	
Total	59.3	76.9	48.1	78.4	129.4	
Hitachi						10
E-beam	7.4	11.0	11.2	22.1	13.1	
Steppers	13.6	17.9	8.2	33.3	49.2	
Dry etch	4.9	3.6	10.8	18.8	34.6	
Dry strip	0	0	0	0.7	4.6	
Ion implantation	3.4	4.2	3.2	3.8	9.6	
CD/wafer inspection	0	0	4.1	6.0	1.7	
APCVD	0.6	0.3	0.4	0	0.2	
Total	29.9	37.0	37.9	84.7	113.0	
Ulvac						11
Sputtering	18.2	22.6	25.4	34.0	48.7	
Evaporation	16.9	16.8	22.4	8.0	14.0	
Ion implantation	12.0	8.4	5.7	7.3	11.3	
Molecular beam epitaxy	3.4	4.2	7.8	7.6	9.2	
PECVD	2.7	2.9	3.0	2.8	4.4	
LPCVD	0	0	1.2	1.4	3.8	
Dry etch	4.9	4.7	3.9	5.7	8.3	
Metalorganic CVD	1.5	1.9	2.7	2.4	3.8	
Total	59.6	61.5	72.1	69.2	103.5	

(Continued)

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Wafer Fab Equipment--Company Rankings

Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Advanced Semiconductor Materials						12
Diffusion	12.5	17.9	16.6	18.5	22.7	
LPCVD	8.7	13.9	20.5	19.9	25.8	
PECVD	33.1	40.4	44.4	44.5	51.6	
Silicon epitaxy	0	0	0	0	3.1	
Total	54.3	72.2	81.5	82.9	103.2	
Dainippon Screen						13
Resist processing equip.	38.4	34.9	29.8	31.2	47.0	
Wet process	25.4	15.9	20.6	21.7	37.8	
Rapid thermal processing	1.3	1.9	1.8	1.0	1.2	
Total	65.1	52.7	52.2	53.9	86.0	
Lam Research						14
Dry Etch	28.0	34.0	26.0	32.0	65.0	
Silicon Epitaxy	30.9	19.4	11.4	14.8	19.0	
Total	58.9	53.4	37.4	46.8	84.0	
TEL/Varian						15
Ion implantation	27.4	36.9	10.2	25.2	76.6	
Thermco						16
Diffusion	42.6	45.1	27.6	34.9	60.0	
LPCVD	7.7	9.1	6.4	6.6	6.5	
Total	50.3	54.2	34.0	41.5	66.5	
ASM Lithography						17
Steppers	2.7	2.8	9.1	36.7	58.6	
E-beam	1.8	1.9	6.0	12.0	6.0	
Total	4.5	4.7	15.1	48.7	64.6	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Tegal						18
Dry etch	38.0	25.0	25.6	35.6	55.0	
Dry strip	8.0	3.0	2.0	2.4	2.0	
Total	46.0	28.0	27.6	38.0	57.0	
KLA Instruments						19
CD/Wafer Inspection	0	11.2	18.1	27.6	54.2	
Silicon Valley Group						20
Resist processing equip.	33.1	30.5	25.6	33.0	37.4	
Diffusion	0	0	0.2	1.1	4.0	
LPCVD	16.8	15.6	9.0	5.3	7.6	
Total	49.9	46.1	34.8	39.4	49.0	
BTU/Bruce						21
Diffusion	35.7	36.2	24.0	19.3	34.0	
LPCVD	4.0	6.7	5.6	7.9	14.5	
Total	39.7	42.9	29.6	27.2	48.5	
Genus						22
LPCVD	16.0	17.5	7.5	13.2	33.4	
Ion implantation	0	0	0	0	14.4	
Total	16.0	17.5	7.5	13.2	47.8	
Materials Research Corp.						23
Sputtering	34.8	37.8	21.9	23.1	34.0	
Dry etch	1.4	4.8	4.1	4.4	13.0	
Total	36.2	42.6	26.0	27.5	47.0	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
E.T. Electrotech						24
PECVD	6.4	13.6	15.3	13.3	20.3	
Dry etch	10.3	8.9	5.0	7.2	14.1	
Sputtering	5.5	8.7	5.3	6.0	9.0	
Dry strip	1.0	1.0	0	0	0	
Total	23.2	32.2	25.6	26.5	43.4	
Kokusai Electric						25
LPCVD	16.9	14.6	17.6	11.1	14.2	
Diffusion	25.3	17.3	13.8	19.2	20.3	
Dry etch	11.5	10.4	3.3	1.4	1.5	
Silicon epitaxy	6.3	5.0	2.1	1.5	4.2	
APCVD	1.5	0.7	0.7	0	0	
Rapid thermal processing	0.1	0.1	0	0	0	
Total	61.6	48.1	37.5	33.2	40.2	
JEOL						26
E-beam	20.3	22.4	41.7	48.9	36.1	
Watkins-Johnson						27
APCVD	4.8	5.9	8.1	16.0	36.0	
Nissin High Voltage						28
Ion Implantation	17.5	21.5	11.8	15.7	32.4	
Tokyo Ohka						29
Dry etch	8.9	7.6	7.2	7.1	10.0	
Dry strip	8.0	8.9	5.2	9.2	19.9	
Total	16.9	16.5	12.4	16.3	29.9	
FSI International						30
Wet process	23.2	28.4	22.4	19.2	24.1	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Sankyo Engineering						31
Wet process	5.2	5.3	7.4	8.1	23.8	
Novellus						32
PECVD	0	0	0	3.6	23.7	
ISA Riber						33
Molecular beam epitaxy	17.2	14.4	13.6	19.3	21.0	
Wild Leitz						34
CD/Wafer Inspection	8.7	9.1	8.3	11.1	20.2	
Machine Technology Inc.						35
Resist processing equip.	20.3	17.8	12.9	12.7	10.0	
Dry strip	0	0.3	2.0	2.7	4.5	
Sputtering	0	0	0.9	3.0	5.0	
Total	20.3	18.1	15.8	18.4	19.5	
Karl Suss						36
Contact/proximity	17.0	17.5	16.0	12.4	12.0	
X-ray	1.0	1.0	0	0	7.2	
Total	18.0	18.5	16.0	12.4	19.2	
Plasma-Therm						37
Dry etch	12.0	13.0	11.0	13.7	12.9	
PECVD	5.7	5.6	5.8	4.6	6.0	
Total	17.7	18.6	16.8	18.3	18.9	
Balzers						38
Sputtering	12.2	10.1	13.2	13.9	11.0	
Evaporation	9.0	10.4	5.0	2.9	2.9	
Ion Implantation	6.0	0	0	2.8	4.2	
Total	27.2	20.5	18.2	19.6	18.1	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Toshiba Machine						39
Silicon epitaxy	2.1	2.3	1.0	0.6	2.0	
E-beam	8.8	0	3.0	3.5	7.7	
APCVD	0	0	4.3	5.0	8.3	
Total	10.9	2.3	8.3	9.1	18.0	
Amaya						40
APCVD	13.7	10.9	6.0	5.5	17.5	
VG Instruments						41
Molecular Beam Epitaxy	8.2	13.5	19.4	15.0	16.5	
American Semiconductor Equipment Technologies						42
Steppers	10.2	8.1	11.6	11.3	16.0	
Tokuda						43
Dry etch	8.7	9.6	4.3	9.4	8.8	
Sputtering	5.1	5.0	3.3	11.1	7.0	
Total	13.8	14.6	7.6	20.5	15.8	
Cambridge Instruments						44
E-beam	11.7	11.9	14.5	10.0	13.0	
Metalorganic CVD	3.5	4.1	3.6	3.3	2.7	
Total	15.2	16.0	18.1	13.3	15.7	
Solitec						45
Resist processing equip.	4.5	5.0	6.5	6.2	7.5	
LPCVD	9.4	12.9	5.3	3.6	8.0	
Diffusion	0.6	0	0.3	0	0	
Total	14.5	17.9	12.1	9.8	15.5	

(Continued)

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Wafer Fab Equipment—Company Rankings

Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Semitool						46
Wet process	18.2	16.9	15.9	18.8	15.4	
Branson/IPC						47
Dry strip	17.0	14.3	10.2	7.8	15.0	
Dry etch	8.8	4.9	4.2	1.6	0	
Total	25.8	19.2	14.4	9.4	15.0	
Kaijo Denki						48
Wet Process	13.7	10.0	13.5	10.1	14.6	
Santa Clara Plastics						49
Wet process	25.0	26.0	20.0	16.0	14.6	
CVC Products						50
Sputtering	8.1	9.5	13.5	9.7	12.3	
Evaporation	0	0	0	0	1.6	
Total	8.1	9.5	13.5	9.7	13.9	
Convac						51
Resist processing equip.	3.0	3.8	6.4	10.9	13.8	
Plasma Systems						52
Dry strip	4.2	3.2	3.3	5.4	10.4	
Dry etch	1.5	1.5	1.7	1.9	3.2	
Total	5.7	4.7	5.0	7.3	13.6	
Enya Seisakusho						53
Wet process	10.8	8.8	9.6	6.2	7.6	
PECVD	5.1	4.2	1.6	1.9	4.2	
LPCVD	2.9	1.3	1.0	0.6	1.8	
Total	18.8	14.3	12.2	8.7	13.6	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Kuwano Electric						54
Wet process	2.1	2.7	3.9	6.3	13.4	
Koyo Lindberg						55
Diffusion	9.7	10.3	7.8	5.7	6.8	
LPCVD	1.7	1.9	2.2	2.0	4.5	
Rapid thermal processing	0.1	0.1	0.3	0.2	0.6	
APCVD	1.5	0.6	0.4	0.2	1.3	
Total	13.0	12.9	10.7	8.1	13.2	
Gasonics						56
Diffusion	4.5	5.3	6.1	7.5	9.0	
Dry strip	0	0	0.7	2.0	3.0	
Total	4.5	5.3	6.8	9.5	12.0	
Verteq						57
Wet process	6.0	5.9	8.3	6.5	11.8	
Leybold-Heraeus						58
Sputtering	3.9	8.8	9.6	15.0	10.8	
Evaporation	5.0	4.0	3.0	1.5	0.5	
Total	8.9	12.8	12.6	16.5	11.3	
Ateq						59
Maskmaking optical laser	0	0	0	1.6	11.2	
AG Associates						60
Rapid thermal processing	6.1	8.8	9.6	10.8	10.6	
Insystems						61
CD/wafer inspection	0	0	0	2.2	9.8	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Ramco						62
Dry strip	0	1.7	4.5	8.7	9.6	
S&K Products International						63
Wet process	5.6	6.6	6.9	8.5	9.4	
Alcan Tech						64
Dry strip	0	0	0.9	5.0	9.2	
Vickers Instruments						65
CD/wafer inspection	0	0	0	8.3	9.0	
Temescal						66
Evaporation	6.4	10.2	10.5	9.9	8.7	
Sputtering	1.8	2.1	1.3	0	0	
Total	8.2	12.3	11.8	9.9	8.7	
Universal Plastics						67
Wet process	0	0.1	1.6	3.7	8.5	
Spectrum CVD						68
LPCVD	0	0	0.5	2.3	8.0	
SCI Manufacturing						69
Wet process	0	0	0	4.8	8.0	
Matrix						70
Dry strip	0	0	2.1	5.2	7.2	
Emcore						71
Metalorganic CVD	0	0.1	2.3	5.1	7.0	

(Continued)

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Wafer Fab Equipment--Company Rankings

Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
CHA Industries						72
Evaporation	5.7	7.1	5.6	6.0	6.3	
Sputtering	0.3	1.0	0.7	0.3	0.7	
Total	6.0	8.1	6.3	6.3	7.0	
Semifab						73
Wet process	6.1	4.8	6.4	7.7	7.0	
Nidek						74
CD/wafer inspection	2.0	1.7	2.2	3.1	6.7	
Aixtron						75
Metalorganic CVD	0	0.5	1.7	4.9	6.7	
Peak Systems						76
Rapid thermal processing	0	0	0.7	3.4	6.6	
Japan Production Engineering						77
PECVD	5.5	5.9	6.0	4.5	6.5	
Nippon Sanso						78
Metalorganic CVD	2.3	3.6	4.6	4.9	6.5	
Sugai						79
Wet process	4.7	3.9	3.7	4.5	6.4	
IVS Incorporated						80
CD/wafer inspection	0	0	0.5	1.5	6.4	
Ulvac/BTU						81
Diffusion	0.2	0.5	0.4	1.7	5.3	
LPCVD	0	0	0	0.5	1.0	
Total	0.2	0.5	0.4	2.2	6.3	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Pacific Western Systems						82
PECVD	12.5	8.7	6.9	7.9	6.2	
APCVD	1.6	1.4	1.2	0.2	0	
LPCVD	0.3	0.4	0.5	0	0	
Diffusion	1.8	1.1	0.6	0	0	
Total	16.2	11.6	9.2	8.1	6.2	
Sumitomo Metal						83
Dry etch	0	0	2.4	5.6	6.2	
Dexon						84
Wet process	1.7	3.5	3.1	3.1	5.9	
Tazmo						85
Resist processing equip.	1.2	1.1	2.5	4.6	5.7	
Sitesa						86
Silicon epitaxy	0	0	0	0	4.5	
Rapid thermal processing	0.4	0.4	0.7	1.0	1.2	
Total	0.4	0.4	0.7	1.0	5.7	
Innotec						87
Sputtering	0.4	2.6	1.8	2.4	4.2	
Evaporation	0.3	0.3	0.2	0	1.0	
Total	0.7	2.9	2.0	2.4	5.2	
Denko						88
Diffusion	1.4	1.0	1.8	2.0	2.7	
LPCVD	0	1.3	2.7	2.1	2.3	
Total	1.4	2.3	4.5	4.1	5.0	

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
SiScan Systems						89
CD/wafer inspection	0	0	1.9	3.0	4.9	
Optical Specialties						90
CD/wafer inspection	15.6	10.0	7.2	5.3	4.8	
Pokorny						91
Wet process	2.2	2.0	3.1	4.3	4.7	
LPE						92
Silicon epitaxy	0	0	0	0	4.5	
Tylan						93
Diffusion	5.5	4.0	2.5	2.0	2.5	
LPCVD	2.0	2.3	0.7	4.0	1.5	
Total	7.5	6.3	3.2	6.0	4.0	
Wellman Furnaces						94
Diffusion	1.5	1.4	1.5	2.0	3.0	
LPCVD	0	0	0	0	1.0	
Total	1.5	1.4	1.5	2.0	4.0	
Process Technology Ltd.						95
LPCVD	4.4	5.7	5.4	4.3	4.0	
Athens						96
Wet process	0	0	0	1.0	4.0	
Heidelberg Instruments						97
CD/wafer inspection	0	0	0	1.6	3.4	
Pure Aire Corporation						98
Wet process	2.2	1.8	1.8	2.4	2.8	

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Crystal Specialties						99
Metalorganic CVD	1.2	1.8	2.7	2.6	2.7	
Focus Semiconductor						100
LPCVD	0	0	0	1.0	2.5	
Ryokosha						101
CD/wafer inspection	2.2	1.4	1.5	1.4	2.5	
Nanometrics						102
CD/wafer inspection	6.7	2.3	1.5	1.7	2.3	
Spire						103
Metalorganic CVD	0.8	3.0	3.3	1.3	2.1	
Integrated Air Systems						104
Wet process	6.0	5.0	4.0	3.0	2.0	
Nippon FMC						105
Metalorganic CVD	0.8	1.1	1.5	1.4	1.9	
Hampshire Instruments						106
X-ray	0	0	0	0	1.8	
Zeiss						107
CD/wafer inspection	0	0.9	2.4	1.8	1.8	
LFE						108
Dry strip	3.0	2.0	1.0	1.0	1.5	
Seiko						109
Molecular beam epitaxy	0	0.8	2.0	1.2	1.4	
Chemitronics						110
Wet process	0	0	0	0	1.4	

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Estek						111
CD/wafer inspection	0	0.3	0.2	0.1	0.2	
Wet process	0	0	0	1.2	1.1	
Total	0	0.3	0.2	1.3	1.3	
Eiko						112
Molecular beam epitaxy	0.5	1.0	1.2	1.4	1.2	
Toyoko Chemical						113
Metalorganic CVD	0	0.7	1.0	0.7	1.2	
National Electrostatics						114
Ion implantation	1.1	2.1	3.9	1.8	1.2	
Samco						115
Metalorganic CVD	1.1	0.7	1.0	1.1	1.2	
CVT						116
Metalorganic CVD	0.5	0.7	0.4	1.1	1.2	
Kurt J. Lesker						117
Sputtering	0.9	0.8	0.8	0.8	0.8	
Evaporation	0.2	0.5	0.3	0.3	0.3	
Total	1.1	1.3	1.1	1.1	1.1	
CVD Equipment						118
Metalorganic CVD	1.2	1.5	0.6	1.2	1.0	
Helmut Seier						119
Diffusion	0.2	0.6	0.5	0.5	0.7	
LPCVD	0	0.3	0	0.3	0.3	
Total	0.2	0.9	0.5	0.8	1.0	

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Centrotherm						120
Diffusion	0.2	0.2	0.2	0.5	1.0	
CFM Technology						121
Wet process	0	0	0	0	1.0	
Semitherm						122
Diffusion	0	0	0	0	0.5	
LPCVD	0	0	0	0	0.5	
Total	0	0	0	0	1.0	
Disco						123
Diffusion	0	0.3	0.7	1.5	1.0	
Semco Engineering						124
Metalorganic CVD	0	0	0	0.3	0.9	
Thomas Schwonn						125
Metalorganic CVD	1.0	0.9	0.3	0.7	0.8	
Sputtered Films						126
Sputtering	2.0	1.0	1.6	1.0	0.6	
Seiden						127
Metalorganic CVD	1.3	0.9	1.3	0.6	0.6	
Shimada						128
Silicon epitaxy	2.5	0.8	0.5	0	0	
Wet process	1.1	0.6	0.6	0.5	0.6	
Metalorganic CVD	0	0	0.3	0	0	
Total	3.6	1.4	1.4	0.5	0.6	
Ion Tech						129
Sputtering	0.5	0.8	0.7	0.7	0.5	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Daiwa Semiconductor						130
Metalorganic CVD	0	0	0.4	0.4	0.5	
Process Products						131
Rapid thermal processing	0	0.5	0.5	0.7	0.4	
Denton Vacuum						132
Sputtering	0	0.1	0.1	0.1	0.1	
Evaporation	0	0.1	0.2	0.2	0.2	
Total	0	0.2	0.3	0.3	0.3	
Elionix						133
Dry etch	0	0	0.2	0.3	0.3	
Nanosil						134
Rapid thermal processing	0	0	0	0.3	0.3	
Poly-Flow Engineering						135
Wet process	0.1	0.8	0.5	0.5	0.2	
Veeco						136
Resist processing equip.	3.8	4.2	2.9	0	0	
Ion implantation	11.0	9.0	0	0	0	
Total	14.8	13.2	2.9	0	0	
EEV						137
Metalorganic CVD	0	1.0	1.4	0.7	0	
Hohkoh Sangyo						138
Dry strip	0.4	1.1	0.5	0.6	0	
Micronix						139
X-ray	0.8	0.8	0.8	0	0	

(Continued)

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Table 1 (Continued)

Semiconductor Wafer Fab Equipment Companies
Ranked by Worldwide Sales
(Millions of Dollars)

	1984	1985	1986	1987	1988	1988 Rank
Reichert-McBain						140
CD/wafer inspection	0	0	3.0	0.3	0	
Ergo Plasma Systems						141
Dry etch	0	0.8	0	0	0	
Ushio						142
Rapid thermal processing	0.3	0.3	0	0	0	

Source: Dataquest
July 1989

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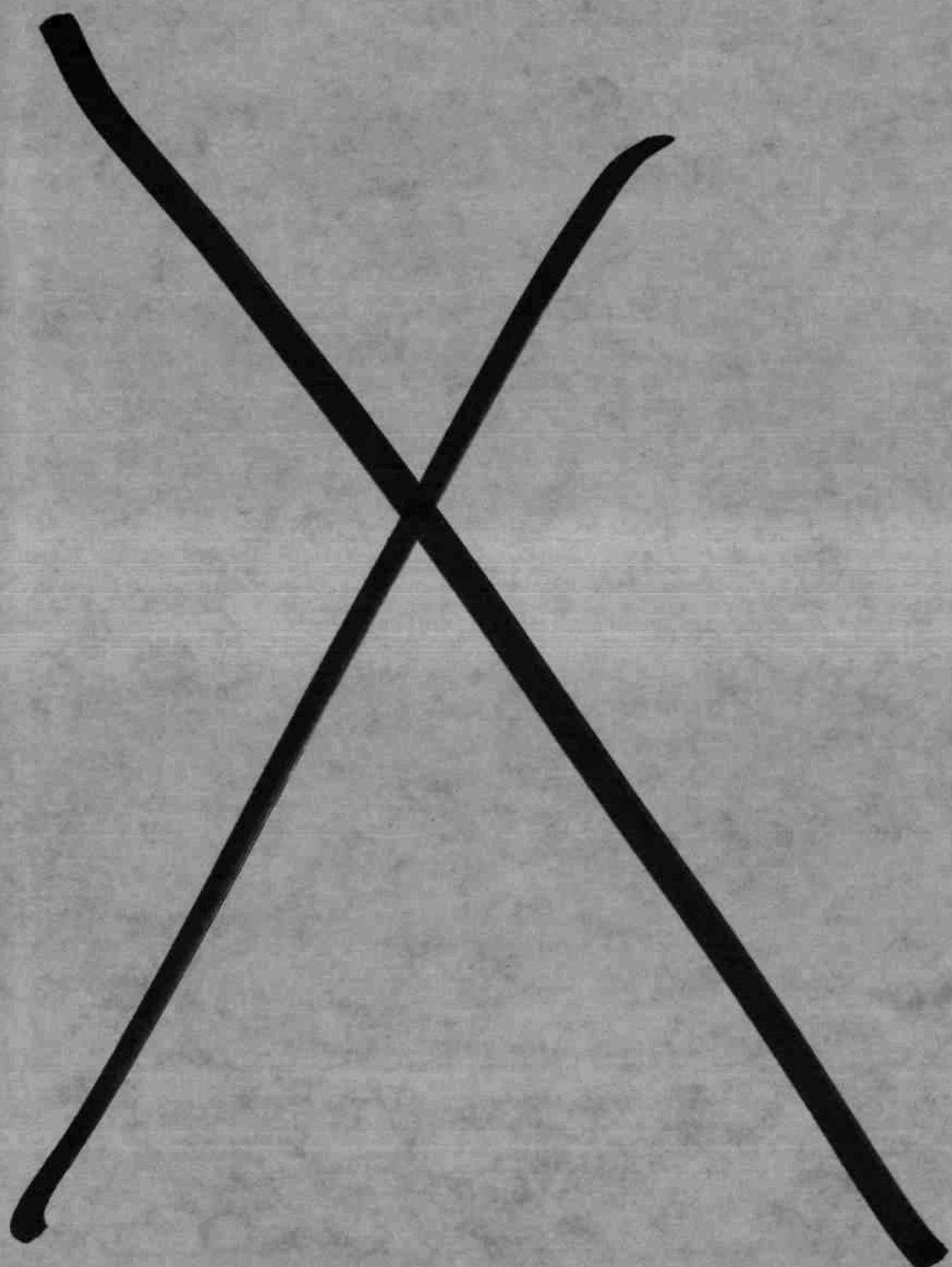

Lithography

The following is a list of the material in this section:

- Stepper Installed Base
- E-Beam Equipment

For additional information, please refer to the material behind the Lithography tab in your 1989 Newsletter binder.

Stepper Installed Base

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Stepper Installed Base

INTRODUCTION

Of all semiconductor capital equipment, wafer steppers tend to have the highest visibility, both within the semiconductor industry and outside. This attention is warranted by the fact that IC fabrication is driven by advances in stepper technology and, because of these advances, high-density, complex integrated circuits can be manufactured. While advances in other key fabrication technologies are also required to produce complex chips, steppers are the engine that pulls the train of wafer fabrication technology forward.

Steppers are often thought to be the bellwether of the semiconductor capital equipment industry; as go steppers, so go the fortunes of the rest of the industry. Industry observers are forever speculating on the outcome of the competitive battle between the stepper vendors, which takes on an international air as the two major stepper vendors view each other with a jaundiced eye across the Pacific.

In light of GCA's recent highly publicized financial problems, stepper discussions have been enlivened as questions of national priorities have arisen. Speculators are envisaging the flight of stepper technology to overseas vendors. Numerous articles discussing the plight of GCA and the stepper market have recently appeared in the nation's leading business publications, and certainly, the stepper market is discussed more than any other semiconductor capital equipment segment.

To aid our clients in interpreting these events, in this service section Dataquest will present the complete installed base of steppers by vendor and by region, from 1978, when the first stepper was shipped, to 1985. Dataquest believes that this is the most complete breakdown of the total installed stepper base yet published. This section will be updated annually.

Although the total stepper market value is given in dollars in one table, the rest of the data in the section deal solely with stepper unit sales. The average selling price of steppers, particularly for the different regions, is a difficult number to obtain, and Dataquest believes that the market can be more meaningfully discussed when comparisons between vendors are done on a unit basis.

WORLDWIDE STEPPER INSTALLED BASE

Table 1 shows worldwide sales for reduction and 1:1 steppers from 1978, the first year in which steppers were shipped, through 1985. Stepper revenue is shown in two parts: the first revenue line indicates revenue from the sale of units, and the second line includes field

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retrofits, upgrades, and associated revenue. Spare parts are not included, since these items generally are not included in the capital equipment budget.

Table 1

WORLDWIDE STEPPER SALES

	1978	1979	1980	1981	1982	1983	1984	1985	Total
Units	11	52	129	235	245	480	839	601	2,592
ASP ($K)	$477	$519	$558	$596	$543	$581	$616	$634	
Revenue ($M)*	$ 5	$ 27	$ 72	$140	$133	$279	$517	$381	
Revenue ($M)**	$ 5	$ 27	$ 74	$147	$140	$293	$552	$407	

*Revenue from sales of units only
**Includes revenue from upgrades and rebuilds

Source: Dataquest
August 1986

The total installed stepper base as of the end of 1985 was 2,592 units. However, 1,920 units or 74 percent of the world's stepper base was installed from 1983 through 1985, thus greatly increasing the world capacity for sub-2-micron devices. (Dataquest estimates that in 1985, 19 percent of wafer starts were sub-2-micron geometries; this is predicted to grow to 40 percent by 1990.) Figure 1 graphically shows the rapid increase in the worldwide installed base over the last three years.

Figures 2a through 2c show that, as expected, stepper sales closely track semiconductor device production and capital spending by the semiconductor manufacturers. Figure 2a shows the semiconductor recessions of 1981 through 1982 and 1985. In the mild recession of 1981/1982, total semiconductor production (merchant plus captive), capital spending, and stepper sales were almost flat. However, in the recent severe recession of 1985, when semiconductor production and capital spending fell off 15 percent and 16 percent, respectively, stepper unit sales went from 839 in 1984 to 601 in 1985, a drop of 28 percent, while revenue dropped from $552 million in 1984 to $407 million in 1985, a decrease of 26 percent.

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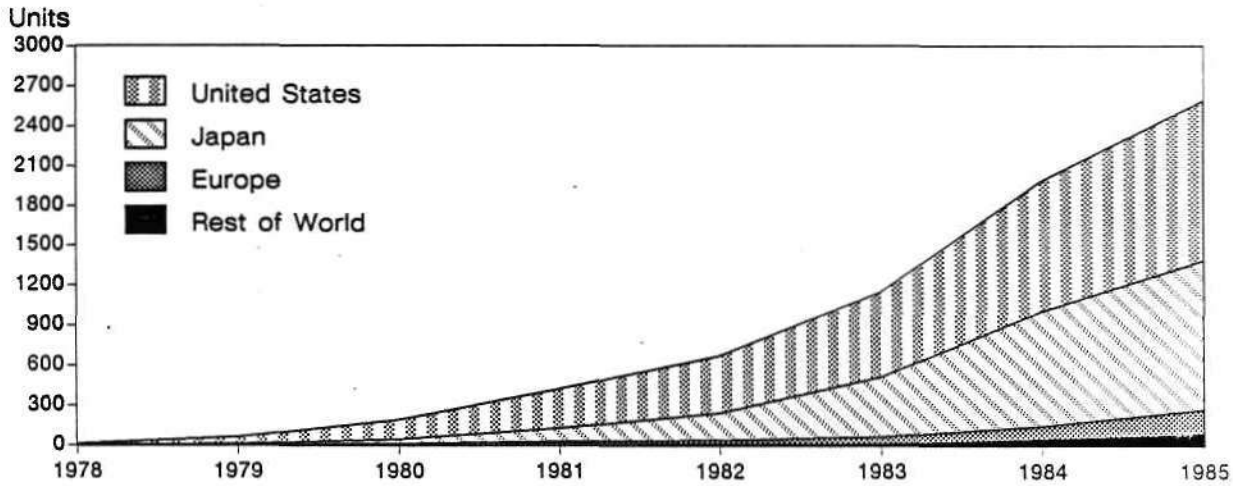
Stepper Installed Base

Figure 1

CUMULATIVE WORLDWIDE STEPPER INSTALLED BASE
1978-1985



Source: Dataquest
August 1986

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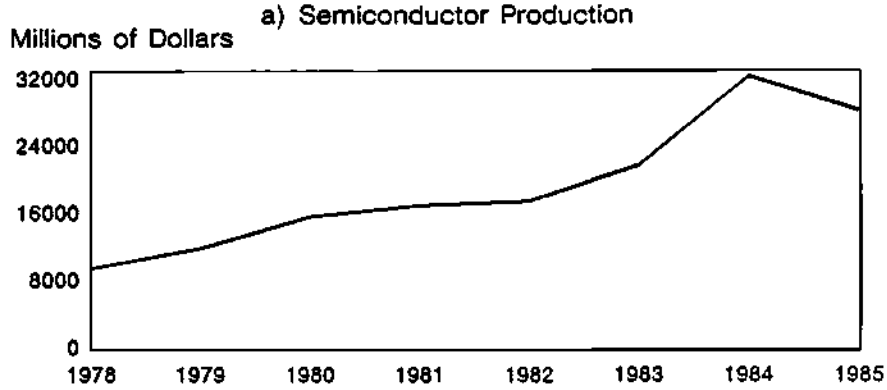
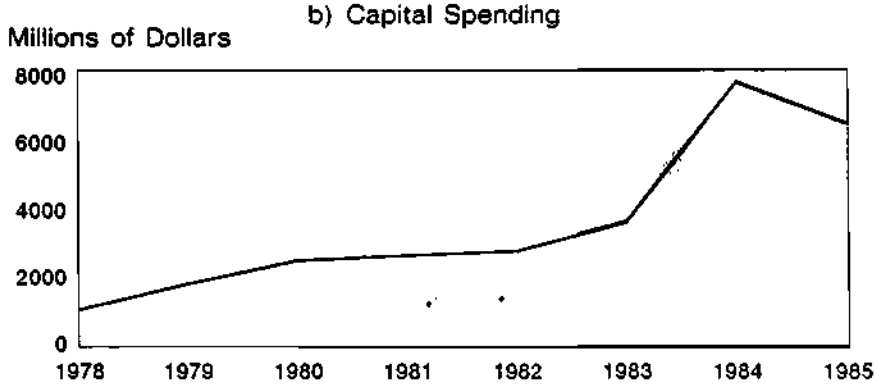
Figure 2

WORLDWIDE SEMICONDUCTOR PRODUCTION, CAPITAL SPENDING, AND STEPPER SALES 1978-1985

a) Semiconductor Production



b) Capital Spending



c) Stepper Sales

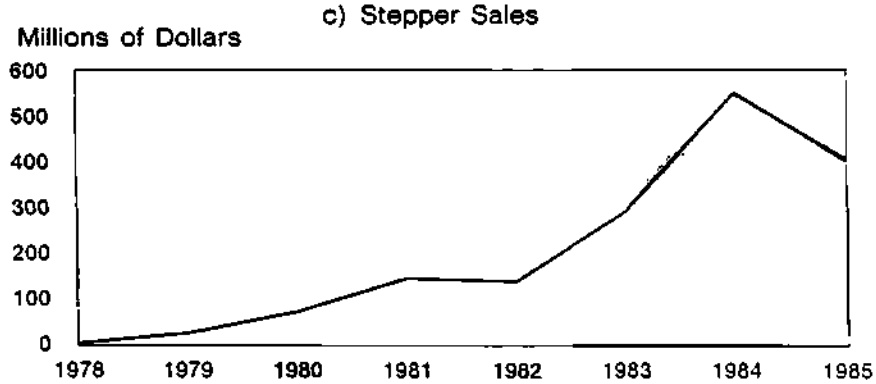


Fig 2

Source: Dataquest
August 1986

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Stepper Installed Base

Average selling prices (ASPs) of steppers took a dip in 1982 due to the semiconductor recession and the introduction of the lower-cost Ultratech 1:1 stepper. Although stepper prices are currently approaching $1 million including options, the 1985 ASP of $634,000 is considerably below this amount. This is due to the averaging in of the Ultratech stepper, regional discounting, and shipments in 1985 at 1984 booked prices. If the Ultratech stepper is removed, then the 1985 reduction stepper ASP is $661,000.

REGIONAL STEPPER INSTALLED BASE

Table 2 shows the regional distribution of the installed base of 2,592 steppers. Forty-six percent (1,205 units) of the installed base is in the United States, while 43 percent (1,111 units) is in Japan. Europe and the rest of the world (ROW) account for the remaining 11 percent (276 units). This is shown graphically in Figure 3.

Table 2

STEPPER INSTALLED BASE BY REGION
(Units)

Region	1978	1979	1980	1981	1982	1983	1984	1985	Total Units	Total %
United States	9	44	92	152	129	209	348	222	1,205	46%
Japan	1	4	32	64	106	243	408	253	1,111	43
Europe	1	4	5	19	9	17	47	79	181	7
Rest of World	0	0	0	0	1	11	36	47	95	4
Total	11	52	129	235	245	480	839	601	2,592	100%

Source: Dataquest
August 1986

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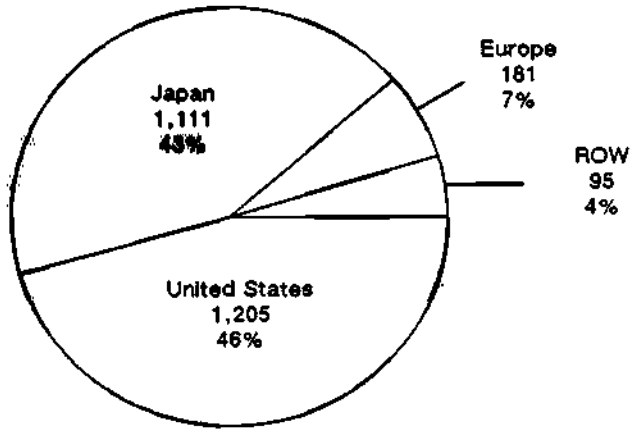
Stepper Installed Base

Figure 3

REGIONAL DISTRIBUTION OF STEPPER UNIT SALES
TOTAL INSTALLED BASE
1978-1985



Total Installed Base: 2,592 Steppers

Source: Dataquest
August 1986

Although presently the United States and Japan have nearly an equal installed base of steppers, the Japanese semiconductor manufacturers are actually adding steppers at a faster rate than the Americans. Figure 4 shows the yearly stepper unit sales to the United States and Japan; it is graphically apparent that the Japanese manufacturers have installed more steppers each year since 1983. From 1983 through 1985, Japanese manufacturers installed 904 steppers compared with the 779 purchased by the American manufacturers. Figure 5 shows that for 1985 stepper unit sales, 42 percent went to Japan while 37 percent were installed in the United States. Clearly, if this trend continues, and Dataquest believes that it will based on our capital equipment spending model, Japan should surpass the United States in installed steppers by early 1987.

Note also that for the 276 units installed in Europe and the ROW countries, 209 or 76 percent have been installed in the last two years. For 1985 alone, these areas accounted for 126 units or 21 percent of 1985 stepper sales. GCA and Ultratech, between them, shipped almost 100 units to Europe and the ROW in 1985. Thus, during the recession year of 1985, these positive areas helped to partially offset GCA's and Ultratech's falling shipments elsewhere.

Europe and the ROW have 11 percent of the worldwide installed stepper base, but accounted for 21 percent of 1985 unit sales. Clearly, the growing stepper market in these areas warrants closer attention by the stepper manufacturers.

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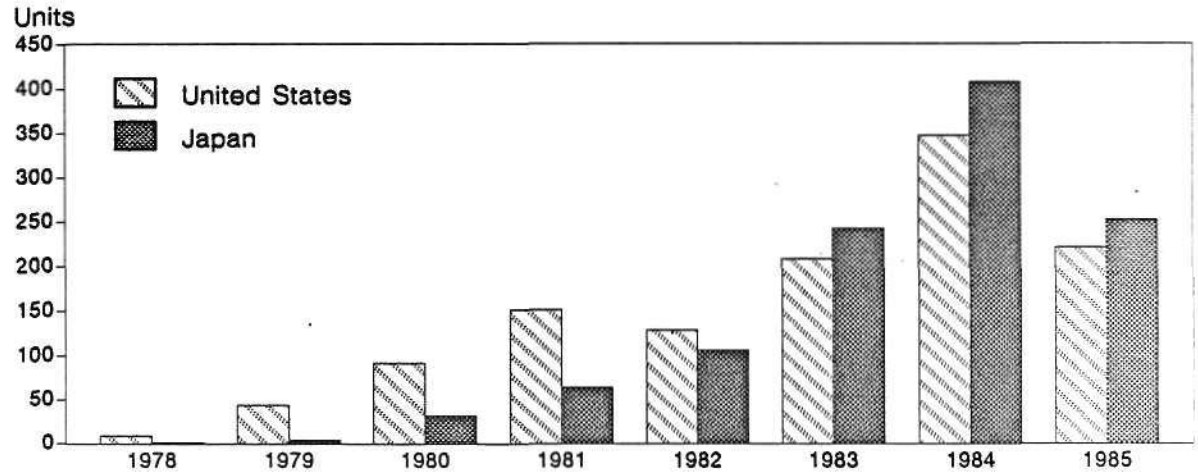
Stepper Installed Base

Figure 4

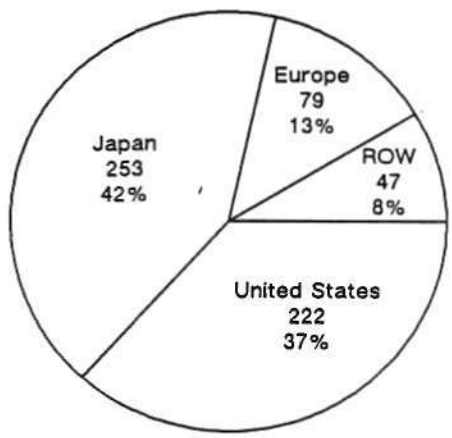
STEPPER UNIT SALES TO THE UNITED STATES AND JAPAN
1978-1985



Source: Dataquest
August 1986

Figure 5

REGIONAL DISTRIBUTION OF STEPPER UNIT SALES
1985



Total 1985 Sales: 601 Steppers

Source: Dataquest
August 1986

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Stepper Installed Base

WORLDWIDE INSTALLED BASE BY VENDOR

Table 3 shows the stepper manufacturers' yearly sales for the worldwide installed base of 2,592 units. GCA, with an installed base of 1,040 units, has a 40 percent share followed by Nikon with 668 units for a 26 percent share and Ultratech with 365 units and a 14 percent share. Together these three companies account for 80 percent of the worldwide installed base. Six other companies account for the remaining 20 percent. Figure 6 shows this graphically.

However, GCA's earlier dominance in the stepper market is giving way to rapidly oncoming Nikon. For instance, for the high-growth years of 1983 through 1985 when 1,920 steppers were shipped worldwide by all vendors, GCA shipped 632 units for a 33 percent market share, while Nikon shipped 600 units for a 31 percent share. Thus, for steppers shipped during the last three years, GCA and Nikon have essentially an equal share of the machines installed. However, for 1985 GCA shipped 168 units for a 28 percent share of the total 601 units shipped, while Nikon shipped 190 units for a 32 percent share.

Table 3

WORLDWIDE STEPPER UNIT SALES BY COMPANY

Company	1978	1979	1980	1981	1982	1983	1984	1985	Total Units	%/IB*
GCA	10	50	107	162	79	175	289	168	1,040	40%
Nikon	0	0	1	16	51	130	280	190	668	26
Ultratech	0	0	0	10	42	69	147	97	365	14
Eaton	0	0	3	10	11	33	43	32	132	5
TRE	0	0	13	18	27	24	15	10	107	4
Hitachi	0	1	4	12	13	25	21	25	101	4
PE	0	0	0	6	20	18	20	20	84	3
Canon	0	0	0	0	0	4	20	55	79	3
ASM	1	1	1	1	2	2	4	4	16	1
Total	11	52	129	235	245	480	839	601	2,592	100%

*Percent of installed base

Source: Dataquest
August 1986

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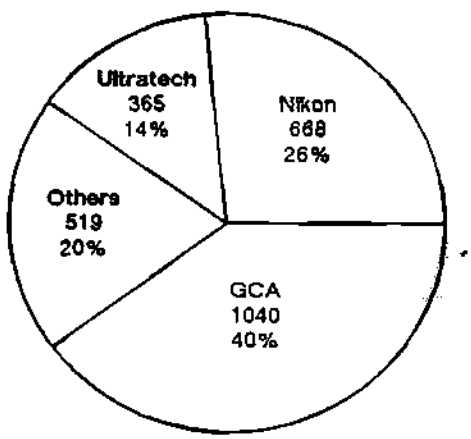
Stepper Installed Base

Figure 6

WORLDWIDE STEPPER UNIT SALES
BY COMPANY
1978-1985



Total Units: 2,592

Source: Dataquest
August 1986

Table 4 converts the unit shipment data in Table 3 to market share percentage. This table shows that GCA's market share has steadily eroded over the years to 28 percent in 1985, while Nikon's share has steadily risen to a 32 percent level in 1985. GCA and Nikon were neck and neck in 1984, but Nikon pulled ahead into the number one position in 1985.

While these two companies have been battling between themselves for dominance in the reduction stepper market, Canon has emerged as a serious threat to both. Table 3 indicates that Canon has an installed base of 79 units, with 55 units shipped in 1985. Canon has come from nowhere to capture 9 percent of the 1985 stepper market, and apparently is continuing its thrust into 1986; Canon may have as many as 120 units in the field as of August 1986.

Dataquest believes, however, that many of the Canon steppers in the field have not been paid for, as they are "evaluation" units. It is estimated that 50 percent or more of the units shipped in 1985 by Canon were evaluation units. Nevertheless, an incredible evaluation program of this magnitude can only indicate Canon's seriousness in obtaining a dominant market share. Every other stepper vendor had flat or decreased sales from 1984 to 1985. However, Canon's installed base almost tripled over this period, and most likely its evaluation program was a prime factor of this increase. (Note: Dataquest has assigned revenue to all of the Canon shipments and this revenue is included in Table 1; therefore, 1985 revenue may be overstated).

Stepper Installed Base

Table 4

WORLDWIDE STEPPER UNIT SALES
MARKET SHARE BY COMPANY

Company	1978	1979	1980	1981	1982	1983	1984	1985	%/IB*
GCA	91%	96%	83%	69%	32%	36%	34%	28%	40%
Nikon	-	-	1	7	21	27	33	32	26
Ultratech	-	-	-	4	17	14	18	16	14
Eaton	-	-	2	4	4	7	5	5	5
TRE	-	-	10	8	11	5	2	2	4
Hitachi	-	2	3	5	5	5	3	4	4
PE	-	-	-	3	8	4	2	3	3
Canon	-	-	-	-	-	1	2	9	3
ASM	9	2	1	1	1	-	-	1	1
Total	100%	100%	100%	100%	100%	100%	100%	100%	100%

*Percent of installed base
Note: Totals may not add due to rounding.

Source: Dataquest
August 1986

Table 4 indicates that Eaton, Perkin-Elmer, TRE (now American Semiconductor Equipment Technologies), ASM, and Hitachi are all struggling to maintain a few percent market share behind the leaders. Dataquest believes that most of the Hitachi steppers are internal to Hitachi. ASM Lithography is just beginning commercial marketing of the Philips stepper and has recently landed its first multiple-unit order.

REGIONAL INSTALLED BASE BY VENDOR

United States

Table 5 shows yearly stepper unit sales and market share by vendor for the United States. The total U.S. installed base is 1,205 units, of which GCA sold 567 units for a 47 percent share, followed by Ultratech with 301 units and a 25 percent share. Currently, TRE with 101 units and Nikon with 100 units share third place with 8 percent shares; however, we

expect that Nikon will be alone in third place by the end of 1986 as a result of its current marketing push in the United States. Figure 7 graphically shows the U.S. and the other regional market shares by vendor.

Table 5

STEPPER UNIT SALES AND MARKET SHARE BY VENDOR
UNITED STATES

	1978		1979		1980		1981		1982	
Company	Units	%	Units	%	Units	%	Units	%	Units	%
GCA	9	100%	44	100%	77	84%	113	74%	40	31%
Ultratech	0	-	0	-	0	-	10	7	41	32
TRE	0	-	0	-	12	13	18	12	23	18
Nikon	0	-	0	-	0	-	0	-	0	-
PE	0	-	0	-	0	-	4	3	17	13
Eaton	0	-	0	-	3	3	7	5	8	6
Canon	0	-	0	-	0	-	0	-	0	-
ASM	0	-	0	-	0	-	0	-	0	-
Hitachi	0	-	0	-	0	-	0	-	0	-
Total	9	100%	44	100%	92	100%	152	100%	129	100%

	1983		1984		1985		Total 1978-1985	
Company	Units	%	Units	%	Units	%	Units	%
GCA	93	44%	131	38%	60	27%	567	47%
Ultratech	64	31	124	36	62	28	301	25%
TRE	24	11	15	4	9	4	101	8%
Nikon	2	1	48	14	50	23	100	8%
PE	13	6	13	4	15	7	62	5%
Eaton	13	6	16	5	13	6	60	5%
Canon	0	-	0	-	10	5	10	1%
ASM	0	-	1	-	3	1	4	1%
Hitachi	0	-	0	-	0	-	0	-
Total	209	100%	348	100%	222	100%	1,205	100%

Note: Totals may not add due to rounding.

Source: Dataquest
August 1986

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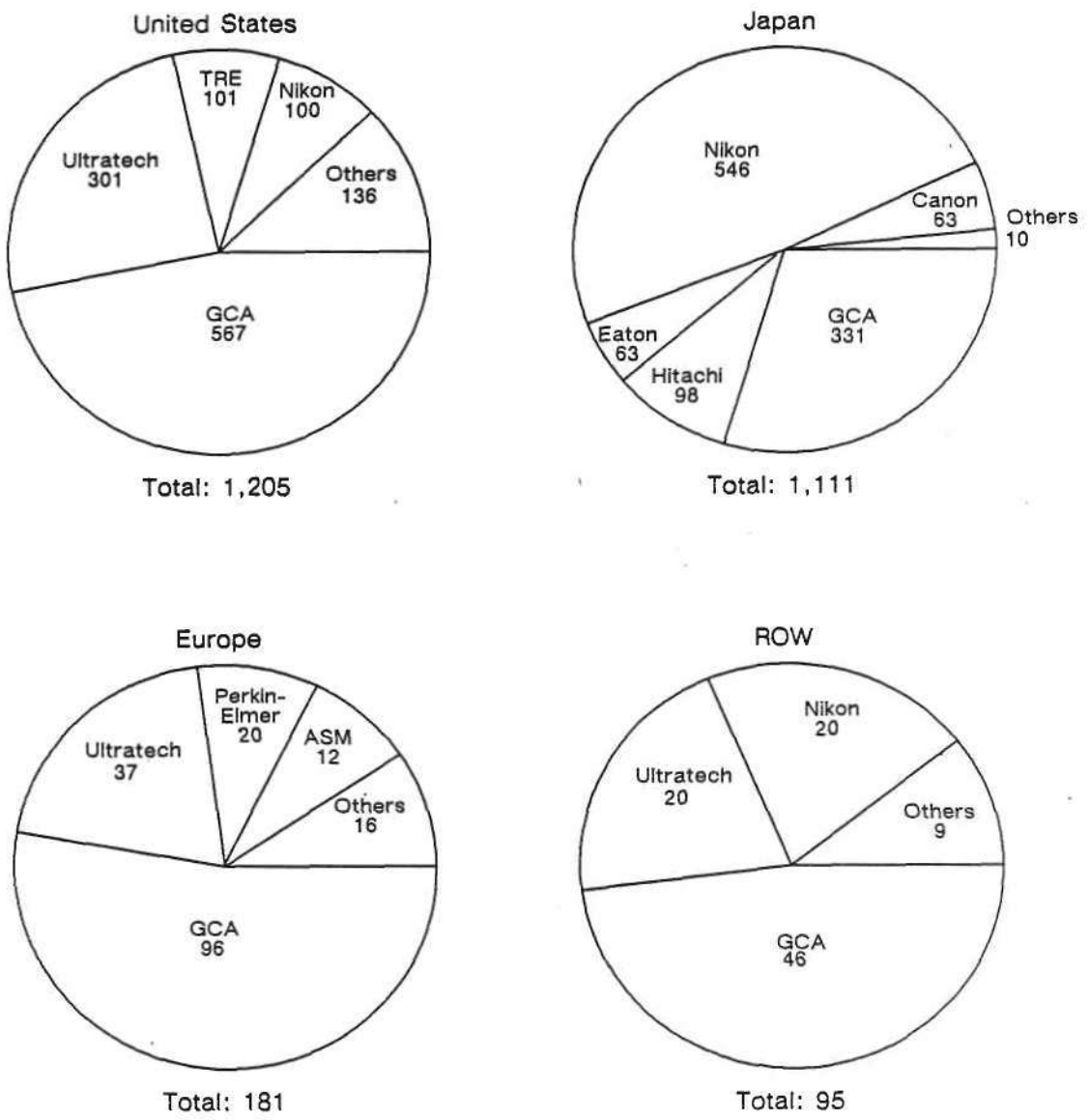
Stepper Installed Base

Figure 7

REGIONAL INSTALLED BASE BY COMPANY
1978-1985



Source: Dataquest
August 1986

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Stepper Installed Base

Although GCA holds almost half of the total U.S. installed base, its yearly market share has continuously declined over the years as indicated in Table 5. For instance, in 1980 its share of the U.S. market was 84 percent, which has eroded to a 27 percent share in 1985. Surprisingly, Ultratech was the 1985 market leader with 62 units for a 29 percent share. Nikon is rapidly increasing its U.S. penetration as it sold 50 units in 1985 for a 23 percent share of the U.S. market.

Together, GCA, Nikon, and Ultratech accounted for 634 units for 81 percent of the 779 steppers sold in the United States from 1983 through 1985. The other six vendors accounted for the remaining 19 percent.

Japan

Table 6 shows yearly stepper unit sales and market share by vendor for Japan. The total Japanese installed base is 1,111 units, of which Nikon has 546 units for a 49 percent share of its home market, followed by GCA with 331 units for a 30 percent share. Together, these two companies have a 79 percent share of the total installed base.

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Stepper Installed Base

Table 6

STEPPER UNIT SALES AND MARKET SHARE BY COMPANY
JAPAN

Company	1978 Units	1978 %	1979 Units	1979 %	1980 Units	1980 %	1981 Units	1981 %	1982 Units	1982 %
Nikon	0	-	0	-	1	3%	16	25%	51	48%
GCA	1	100%	3	75%	27	84	33	52	36	34
Hitachi	0	-	1	25	4	13	12	19	13	12
Canon	0	-	0	-	0	-	0	-	0	-
Eaton	0	-	0	-	0	-	3	5	3	3
Ultratech	0	-	0	-	0	-	0	-	1	1
PE	0	-	0	-	0	-	0	-	1	1
ASM	0	-	0	-	0	-	0	-	0	-
TRE	0	-	0	-	0	-	0	-	1	1
Total	1	100%	4	100%	32	100%	64	100%	106	100%

Company	1983 Units	1983 %	1984 Units	1984 %	1985 Units	1985 %	Total 1978-1985 Units	Total 1978-1985 %
Nikon	128	53%	222	54%	128	51%	546	49%
GCA	67	28	122	30	42	17	331	30
Hitachi	25	10	19	5	24	9	98	9
Canon	4	2	20	5	39	15	63	6
Eaton	15	6	25	6	17	7	63	6
Ultratech	3	1	0	-	3	1	7	1
PE	1	-	0	-	0	-	2	-
ASM	0	-	0	-	0	-	0	-
TRE	0	-	0	-	0	-	1	-
Total	243	100%	408	100%	253	100%	1,111	100%

Note: Totals may not add due to rounding.

Source: Dataquest
August 1986

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Stepper Installed Base

Again, the total installed base numbers mask the recent market dynamics; GCA, which once had more than a 50 percent share of the Japanese market, had only a 17 percent market share in 1985. During the period from 1983 through 1985, Nikon sold twice as many steppers (478) in Japan as GCA did (236). However, while Nikon and GCA had a combined market share of 84 percent of the Japanese market in 1984, they dropped to a combined share of 68 percent in 1985 due to the onslaught of Canon. Canon was able to gather a 15 percent share (even though many of the units have not yet been paid for), to almost equal GCA as the number two stepper supplier in Japan in 1985.

Together, the three Japanese vendors (Canon, Hitachi, Nikon) and GCA account for 93 percent of the installed base. Eaton, the only other American vendor with any presence in Japan, has a 6 percent share, due mainly to its large installed base at Oki Electric.

Finally, it should be noted that GCA and Nikon both have nearly 50 percent of their home markets in the United States and Japan, respectively.

Europe

European stepper sales and market shares are shown in Table 7. Of the total installed base of 181 units, GCA has sold 96 units for a 53 percent share, followed by Ultratech with 20 percent and Perkin-Elmer with 11 percent. Together, these three vendors account for 84 percent of the total installed base. Nikon and Canon have only recently begun marketing in Europe, so their installed bases are still low. Dataquest estimates that most of the ASM/Philips units are internal to Philips. TRE and Eaton have little presence in Europe, and Hitachi is not yet marketing its systems in Europe.

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Stepper Installed Base

Table 7

STEPPER UNIT SALES AND MARKET SHARE BY COMPANY
EUROPE

Company	1978 Units	1978 %	1979 Units	1979 %	1980 Units	1980 %	1981 Units	1981 %	1982 Units	1982 %
GCA	0	-	3	75%	3	60%	16	84%	3	33%
Ultratech	0	-	0	-	0	-	0	-	0	-
PE	0	-	0	-	0	-	2	11	2	22
ASM	1	100%	1	25	1	20	2	5	2	22
Canon	0	-	0	-	0	-	0	-	0	-
Eaton	0	-	0	-	0	-	0	-	0	-
TRE	0	-	0	-	1	20	0	-	2	22
Nikon	0	-	0	-	0	-	0	-	0	-
Hitachi	0	-	0	-	0	-	0	-	0	-
Total	1	100%	4	100%	5	100%	19	100%	9	100%

Company	1983 Units	1983 %	1984 Units	1984 %	1985 Units	1985 %	Total 1978-1985 Units	Total 1978-1985 %
GCA	7	41%	24	51%	40	51%	96	53%
Ultratech	2	12	13	28	22	28	37	20
PE	4	24	7	15	5	6	20	11
ASM	2	12	3	6	1	1	12	7
Canon	0	-	0	-	6	8	6	3
Eaton	2	12	0	-	2	3	4	2
TRE	0	-	0	-	1	1	4	2
Nikon	0	-	0	-	2	3	2	1
Hitachi	0	-	0	-	0	-	0	-
Total	17	100%	47	100%	79	100%	181	100%

Note: Totals may not add due to rounding.

Source: Dataquest
August 1986

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Rest of the World

Table 8 shows stepper sales and market share data for the ROW area. Of the total installed base of 95 steppers, GCA has 46 for a market share of 48 percent, followed by Nikon and Ultratech with 21 percent shares each. These three companies account for 90 percent of the total installed base; no other stepper manufacturer has any significant presence in ROW. Note also that 83 units of the installed base of 95 were installed in the last two years, and most were installed in Korea.

Table 8

STEPPER UNIT SALES AND MARKET SHARE BY COMPANY
REST OF WORLD

Company	1978 Units	1978 %	1979 Units	1979 %	1980 Units	1980 %	1981 Units	1981 %	1982 Units	1982 %
GCA	0	-	0	-	0	-	0	-	0	-
Nikon	0	-	0	-	0	-	0	-	0	-
Ultratech	0	-	0	-	0	-	0	-	0	-
Eaton	0	-	0	-	0	-	0	-	0	-
Hitachi	0	-	0	-	0	-	0	-	0	-
TRE	0	-	0	-	0	-	0	-	1	100%
ASM	0	-	0	-	0	-	0	-	0	-
Canon	0	-	0	-	0	-	0	-	0	-
PE	0	-	0	-	0	-	0	-	0	-
Total	0	-	0	-	0	-	0	-	1	100%

Company	1983 Units	1983 %	1984 Units	1984 %	1985 Units	1985 %	Total 1978-1985 Units	Total 1978-1985 %
GCA	8	73%	12	33%	26	55%	46	48%
Nikon	0	-	10	28	10	21	20	21
Ultratech	0	-	10	28	10	21	20	21
Eaton	3	27	2	6	0	-	5	5
Hitachi	0	-	2	6	1	2	3	3
TRE	0	-	0	-	0	-	1	1
ASM	0	-	0	-	0	-	0	-
Canon	0	-	0	-	0	-	0	-
PE	0	-	0	-	0	-	0	-
Total	11	100%	36	100%	47	100%	95	100%

Note: Totals may not add due to rounding.

Source: Dataquest
August 1986

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Stepper Installed Base

STEPPER UNIT SALES--GCA AND NIKON

The worldwide installed base of reduction steppers is 2,227 units (2,592 less the 365 Ultratech units). GCA and Nikon are the dominant players in the reduction stepper market as they have a combined total of 1,708 units for a worldwide market share of 76 percent. Table 9 provides a history of their stepper unit sales by year and by region. As the table shows, GCA has 55 percent of its installed base in the United States, 32 percent in Japan, with Europe and ROW accounting for the remaining 13 percent. Nikon has 82 percent of its steppers installed in Japan, but is striving toward an increasing base in the United States. Figure 8 graphically depicts GCA's and Nikon's regional market shares.

Table 9

STEPPER UNIT SALES
GCA AND NIKON

Region	1978	1979	1980	1981	1982	1983	1984	1985	Total Units	Total %
GCA										
U.S.	9	44	77	113	40	93	131	60	567	55%
Japan	1	3	27	33	36	67	122	42	331	32
Europe	0	3	3	16	3	7	24	40	96	9
ROW	0	0	0	0	0	8	12	26	46	4
Total	11	50	107	162	79	175	289	168	1,040	100%
Nikon										
U.S.	0	0	0	0	0	2	48	50	100	15%
Japan	0	0	1	16	51	128	222	128	546	82
Europe	0	0	0	0	0	0	0	2	2	-
ROW	0	0	0	0	0	0	10	10	20	3
Total	0	0	1	16	51	130	280	190	668	100%

Source: Dataquest
August 1986

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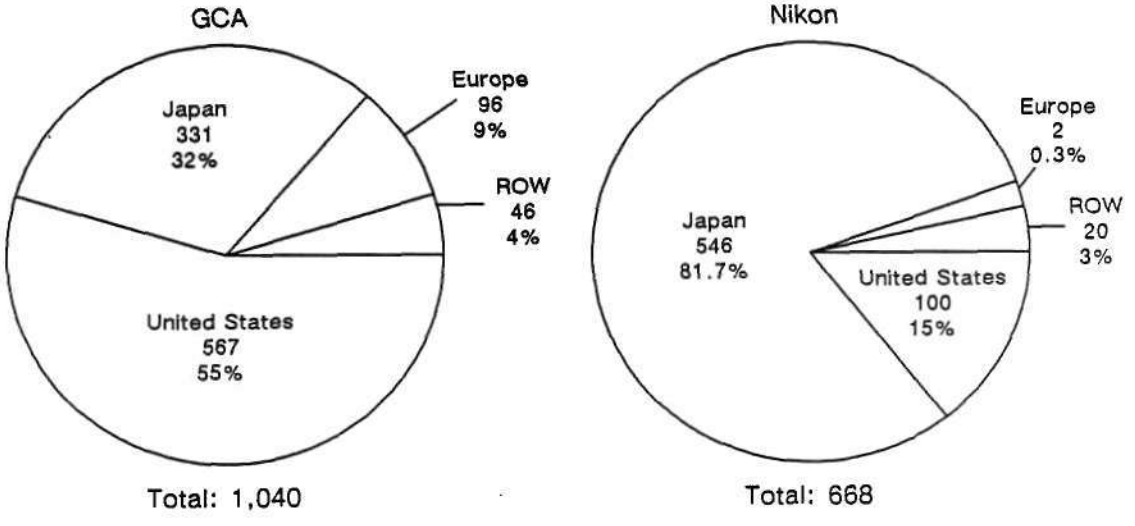
Stepper Installed Base

Figure 8

REGIONAL INSTALLED STEPPER BASE
GCA AND NIKON
1978-1985



Source: Dataquest
August 1986

In 1984, of the 289 steppers sold by GCA, 253 units were installed in Japan and the United States. However, in 1985, GCA's sales to these areas dropped to 102 units, a falloff of 60 percent of unit sales. Nikon's sales to these areas was 270 units in 1984, decreasing to 178 units in 1985, a falloff of only 34 percent. Nikon's sales in Japan decreased by 42 percent in 1985, and GCA's sales in the United States decreased by 54 percent. In contrast, GCA's sales in Japan decreased by 66 percent in 1985, while Nikon's sales in the United States were essentially flat from 1984 to 1985.

As Table 9 shows, GCA's sales to Europe and the ROW areas accounted for 66 units or 39 percent of 1985 unit sales, compared with only 11 percent of the 1984 total. It was the increased activity in these areas that partially offset the decline in GCA's sales in Japan and the United States, and helped to prevent an even greater slide in the company's total sales for 1985.

Stepper Installed Base

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E-Beam Equipment

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E-Beam Equipment

INTRODUCTION

This section provides an overview of E-beam equipment technology and an analysis of the E-beam equipment market. The discussion includes both direct write and maskmaking equipment.

E-beam direct write was predicted to be the lithography tool of the late 1980s and beyond as the IC industry continued to move to the smaller geometries that could not be handled by optical techniques. However, advances in optical and X-ray lithography and the low throughput and, consequently, high costs of E-beam lithography have prevented this from happening. DATAQUEST believes that E-beam lithography will not be used for high-volume manufacture of IC devices, but will find its major use in three market niches: fabrication of submicron gallium arsenide devices, low-volume application-specific IC (ASIC) production, and fast-turn prototyping.

E-beam direct write has been used in the production of low-volume, fast-turn ASIC devices for more than ten years at IBM. More recently, merchant ASIC companies, who also must manufacture low volumes of ICs with fast turnarounds, also are beginning to purchase direct write tools. Direct write provides a faster turnaround than optical lithography because the fabrication of masks is not necessary. Direct write can cost less per exposure than optical lithography for low volumes because the cost of the mask set is eliminated.

The device volume at which direct write costs less than optical lithography depends upon several factors. While it is not DATAQUEST's intent in this section to quantify the volume, one estimate has pegged the crossover point between optical and E-beam at 10 wafers per lot; other estimates range from 10,000 to 40,000 devices per lot.

The use of E-beam in the fabrication of gallium arsenide devices is another emerging market for direct write. In the past, direct write on gallium arsenide has been used either in research and development or by the system houses that fabricate military gallium arsenide devices. However, now the merchant gallium arsenide device manufacturers are beginning to install E-beam systems as well.

Another emerging application is fast-turnaround prototyping. With optical lithography, a mask set has to be fabricated before the customer can receive first silicon for his circuit design. Usually, a design will go through several iterations, and new masks have to be made each time. This adds to the developmental costs, and more importantly, extends the development time in critical situations. Direct write of the prototype design and its iterations shortens the development time and allows the customer quick access to working silicon parts and the opportunity to design silicon directly into his prototype systems.

E-Beam Equipment

DATAQUEST believes that the gallium arsenide, ASIC, and fast-turn prototyping market niches will have high growth rates over the next five years, with the gallium arsenide and ASIC areas having higher growth rates than the fast-turn prototyping. Accordingly, DATAQUEST expects the E-beam direct write equipment market to grow from $29.5 million in 1985 to $147 million in 1990. This represents a CAGR (compound annual growth rate) of 37.9 percent.

The E-beam maskmaking equipment market is expected to grow from $84.2 million in 1985 to $166 million in 1990. This represents a CAGR of 14.5 percent. DATAQUEST believes that from 1986 to 1990, 202 maskmaking systems with a market value of $626 million will be sold. It should be noted that this forecast does not take into account the possible impact of laser beam reticle making technology, which is just now being announced in the market.

COMPANIES WITH E-BEAM EQUIPMENT PROGRAMS

Back in the late 1960s and early 1970s, it was perceived that optical lithography would run out of steam below two microns. Consequently, many companies at this time began direct write E-beam programs in order to fill the anticipated need. In addition, it was apparent that optical pattern generators were becoming too slow for the rapidly increasing circuit complexities and, accordingly, commercial production-oriented E-beam pattern generators appeared in the late 1970s.

The years 1977 and 1978 saw a frenzy of activity for companies involved in E-beam development, as several companies introduced products during this time. Although the maskmaking equipment market has continued to grow since then, the direct write market has failed to live up to its earlier expectations.

This section gives a historical overview of E-beam direct write and maskmaking technology, the principal players involved in this technology, and the players who have become casualties. The idea is to provide an understanding of where E-beam technology has come from and where it stands today so that we can have a clearer idea of where it is going in the future. This section discusses 19 companies that are (or were) involved in substantial E-beam equipment build programs. These 19 companies are divided into three categories: 1) companies that build E-beam equipment solely for their own internal use, 2) companies that were developing E-beam equipment for the commercial market, but have since dropped out, and 3) companies that are actively participating in the commercial market. Table 1 lists the 19 companies to be discussed.

E-Beam Equipment

Table 1

COMPANIES WITH E-BEAM EQUIPMENT PROGRAMS

Internal Use Only	Companies Exited	Active Participants
AT&T	Control Data	Cambridge
Hewlett-Packard	GCA	Electron Vision
IBM	General Signal	Elionixs
Texas Instruments	Thomson-CSF	Hitachi
	Varian	JEOL
	Veeco	Perkin-Elmer
		Philips
		Toshiba
		Carl Zeiss (Jena)

Source: DATAQUEST
January 1986

Internal Use Only

Several companies have had very extensive programs for developing E-beam systems solely for their own internal use. Three such companies, Hewlett-Packard, IBM, and Texas Instruments, have not made their technology available to the commercial market, while AT&T has made available its earlier E-beam technology via licensing arrangements to Varian and Perkin-Elmer. There are a number of other companies and universities with their own in-house E-beam programs, but they will not be discussed separately here.

AT&T

In the early 1970s, Bell Laboratories developed an E-beam system specifically for maskmaking. This system, called the EBES (electron beam exposure system), uses a Gaussian round beam with raster scan writing and continuous stage motion. In the EBES writing method, the chip is divided into stripes that are 512 addresses wide. In the case of a 0.5-micron address, this would correspond to a stripe width of 256 microns. While the stage is continuously moving in the X direction, the electron beam is deflected in the Y direction in order to expose all 512 addresses along the scan line and all subsequent scan lines until the entire length of the stripe is exposed. (Refer to Figure 1.)

Figure 1

EBES WRITING STRATEGY

Source: DATAQUEST
January 1986

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E-Beam Equipment

After the first stripe of the first chip is exposed, the stage continues to move until the first stripes of all the chips on the wafer have been exposed. The second stripe is then written on all the chips and, similarly, the third and so on until the entire chip has been exposed.

By 1975, Bell had three E-beam machines in use. These were EBES I, a 10-MHz machine, and EBES II and EBES III, which were upgrades of EBES I and operated at a 20-MHz data rate. Also in 1975, Bell licensed its EBES technology to ETEC and Varian, both of whom subsequently shipped advanced commercial versions of the EBES system in the 1977/1978 time frame.

All three EBES machines were used for production maskmaking, but since have been retired. EBES II and III are now being used in research and development.

In 1978, Bell began to conceptualize a new generation machine, which resulted in EBES IV. This system uses a Gaussian round beam and a combination of vector and raster scanning. The electron beam is vector-scanned to the feature to be exposed. The feature is divided into microfeatures, which are then exposed with raster scan fill-in. The beam size can be as small as 1/8 micron and the address size can be as small as 1/64 micron.

Bell has intended EBES IV to be a multipurpose machine for use in an R&D environment for direct write, maskmaking R&D, E-beam resist R&D, and for use as a test bed to further Bell's E-beam technology. Bell has also built EBES V, which is similar to EBES IV. Bell has not disclosed details on the EBES IV/V, but it will be publishing some papers on this subject at the May 1986 IEEE meeting.

Hewlett-Packard

Hewlett-Packard (HP) revealed its E-beam system in 1981 at the IEEE Sixteenth Symposium on Electron, Ion, and Photon Beam Technology. HP's original intention was to develop a precision direct write E-beam system for production use, but later a requirement was added that it function as a maskmaking system as well.

Hewlett-Packard said that the E-beam project was its biggest R&D project ever; the equivalent of several person-centuries went into the program. By the end of the project, 65 engineers and scientists were working full time on the project with another 21 working part time. DATAQUEST mentions these comments by Hewlett-Packard to indicate the magnitude of E-beam development programs in general.

E-Beam Equipment

The machine is a step-and-repeat system that writes a 5mm x 5mm deflection field. It uses a modified raster scan and a Gaussian round beam with a spot size that originally was 0.5 micron, but since has been reduced to 0.25 micron. A zirconiated thermal field emission cathode is used to produce a very small bright source of electrons. The resulting high beam current of 600 nanoamperes for a 0.5-micron spot or 250 nanoamperes for a 0.25-micron spot allows a very fast writing rate of 300 MHz.

Hewlett-Packard currently has three of its E-beam systems in operation. Two of the machines are developmental machines in HP's Palo Alto facilities, and the third is being used in R&D at the Santa Rosa plant. HP also has a JEOL JBX-6AII, which it uses for direct write R&D applications. For production maskmaking, Hewlett-Packard has a Perkin-Elmer MEBES machine.

IBM

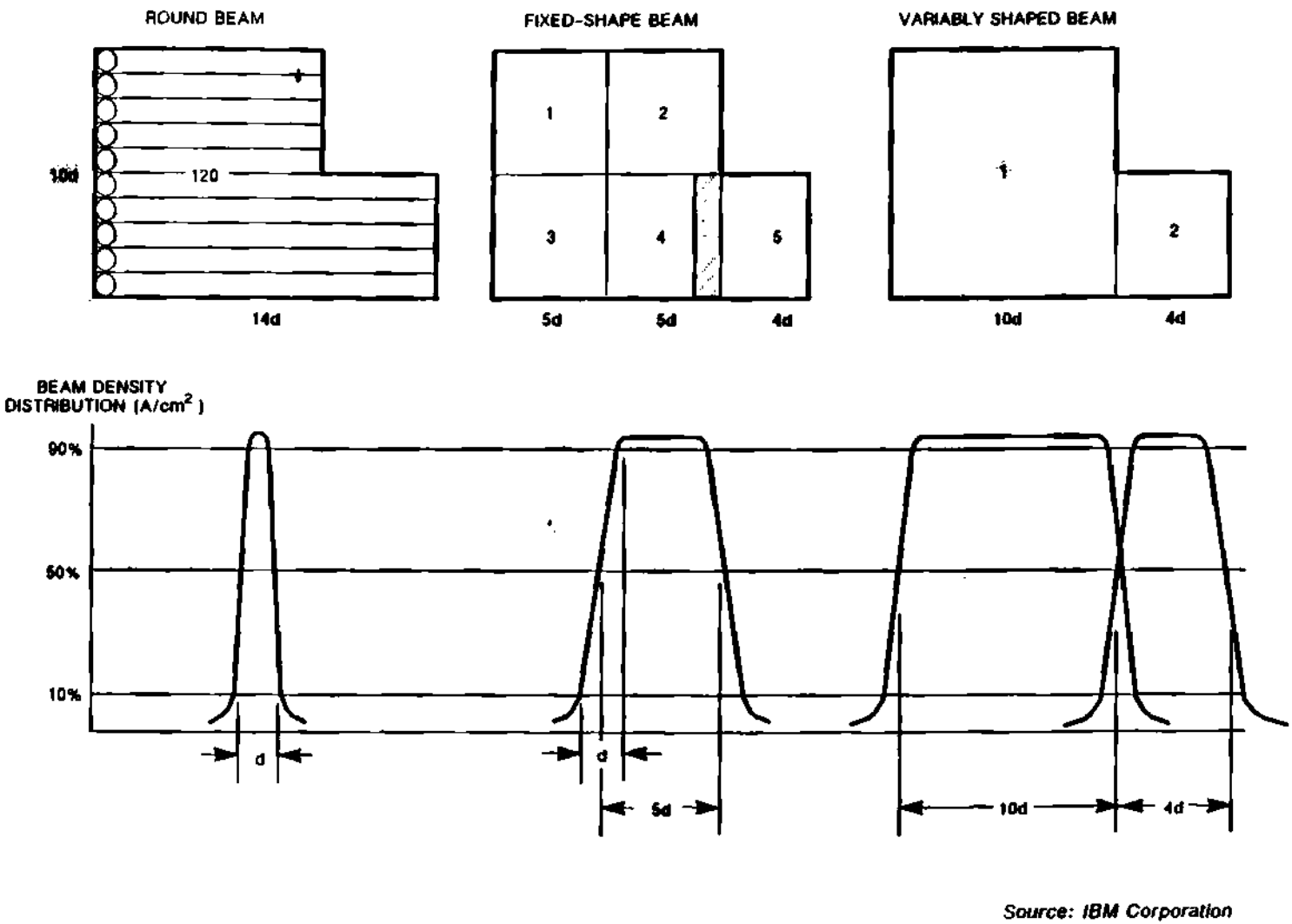
In 1968, an E-beam project was begun at IBM's East Fishkill Research Laboratory to explore the feasibility of a high-throughput, direct write system. The project was based on the need to obtain faster turnaround times on production gate arrays and the requirement for a lithography tool to fabricate one-micron geometries. The result of this project is the EL series of E-beam systems.

The initial activity resulted in the EL-1, which was not a modified scanning electron microscope (SEM) like most other contemporary systems, but was originally designed from the start as a lithography tool. It was the first scanning E-beam system designed specifically for production direct write of semiconductor devices on a manufacturing line. The EL-1 used a raster-scanned, fixed square beam to obtain a much higher throughput than systems using a Gaussian round beam. The 2.5-micron square beam, which was as big as the smallest geometry to be exposed, was equivalent to a 5 x 5 array of 0.5-micron Gaussian round beams and required only 1/25 of the exposure time. Figure 2 illustrates this point. A system using a round beam would need 120 exposures to expose the area shown in Figure 2, but would only require 5 exposures for a fixed square beam system. The EL-1 was a step-and-repeat system that exposed a maximum field size of 6.5mm x 6.5mm.

The EL-1 was used on IBM's QTAT (quick turnaround time) line to fabricate bipolar gate arrays as early as 1974. These devices were fabricated with optical and E-beam mix-and-match lithography, with the final three layers done on the EL-1. The EL-1 had 2,500 device part numbers in residence. Over one four-year period (1979 to 1982), the EL-1 exposed 352,000 wafers at throughputs of seven to ten wafers/hour, with a system availability of 90 to 95 percent. Ten EL-1s were eventually built and three systems are still in use on East Fishkill's QTAT line.

Figure 2

PATTERN GENERATION AND BEAM PROFILES



Source: IBM Corporation

E-Beam Equipment

The EL-2, the first E-beam system to use a variable shaped beam, further increased throughput over the fixed square beam EL-1. With a variable shaped beam, only two exposures are needed to write the area shown in Figure 2. Like the EL-1, the EL-2 beam was raster scanned over the deflection field. The EL-2, which became operational in 1977, was an interim machine that was developed primarily as a laboratory tool for advanced product and process development. Three EL-2s were built, but were eventually phased out when the EL-3 was developed. One EL-2 is currently being used at Rensselaer Polytechnic Institute for submicron development work.

Work on the EL-3 started in 1978, and it has since become the workhorse for E-beam lithography at IBM. Thirty systems have been built (or are being built) at a cost of about $3 million each. They are in use at IBM's semiconductor plants in the United States and France (IBM France has a line similar to East Fishkill's QTAT line) for applications ranging from 0.5-micron to 2.5-micron minimum geometries. Newly developed for the EL-3 was subfield vector writing. In this method, the deflection field is divided into subfields and the patterns within the subfields are written with vector scanning of the variable shaped beam. The beam is raster scanned from subfield to subfield and all subfields are visited regardless of whether the subfield contains a pattern or not. The EL-3 is used for both direct write and 1X and 10X maskmaking applications.

Of the 30 EL-3 machines, 5 are used for maskmaking and the rest are used for direct write development or production. In addition to the three EL-1s on the QTAT line, there are two EL-3s with another to be added. Besides custom logic production on the QTAT line, high-performance ROMs are personalized in one-third the time required for optical lithography. IBM has recently announced E-beam fabricated standard logic and memory array chips using 0.5-micron geometries.

Altogether, 43 EL-series machines have been built, with 40 still in use. At the end of 1984, 25 machines were in use and 15 more were added in 1985. Table 2 shows the progress of the EL-series. Since 1982 there have been further enhancements in the performance of the EL-3; however, IBM has not yet released the details of the current performance.

Table 2

PROGRESS OF IBM EL SERIES

	EL-1 1974	EL-2 1977	EL-3 1980	EL-3 1980	EL-3 1982
Minimum Feature Size	2.5um	1um	2um	1um	0.5um
Field Size (sq. mm.)	6.5mm	8mm	10mm	5mm	5mm
Overlay Accuracy	0.75um	0.4um	0.7um	0.4um	0.1um
Wafer Size	100mm	100mm	165mm	165mm	165mm
Maskmaking	No	No	Yes	Yes	Yes
Throughput (3-inch Wafers)					
2.5um Design	10	15	20-40	-	-
1.0um Design	-	5	-	10-20	-
0.5um Design	-	-	-	-	2-5

Source: IBM Corporation

Texas Instruments

Texas Instruments (TI) began working on E-beam development as early as 1965. By 1977, in-house maskmaking production on E-beam machines built by Texas Instruments was fairly routine, and direct write E-beam was being used in the laboratory. The EBM-2 (1976) was a step-and-repeat machine that exposed a 6.35mm x 6.35mm deflection field. It used a Gaussian round beam and could obtain one-micron minimum geometries. In late 1978, Texas Instruments reported that it was using E-beam to fabricate submicron MESFETS with 0.25-micron gate lengths. The process incorporated five E-beam levels. In 1981, TI reported that it would use direct write E-beam and optical lithography in mix-and-match production for a new 16-bit microprocessor designed for military applications. The device used 1.25-micron minimum features, but it would later be shrunk to 1-micron features. The EBM-5, which DATAQUEST believes is a variable-shaped beam vector scan system, was used to fabricate 16-bit microprocessors, I^2L circuits, and 4KSRAMs as early as 1981. Throughputs for the EBM-5 are estimated to be 20 to 45 wafers/hour for 2-micron lines and 10 to 20 wafers/hour for 1-micron geometries.

Texas Instruments has been very quiet about its developmental efforts in E-beam; it has been on the company's trade secret list for many years. Consequently, there has been almost no published information on the E-beam program. DATAQUEST estimates that Texas Instruments has built 16 E-beam machines, and that at least 10 of these machines are being used for maskmaking. DATAQUEST also believes that TI has de-emphasized

building its own E-beam machines, and in support of this, DATAQUEST notes that TI will soon take delivery of its first Perkin-Elmer MEBES III.

Texas Instruments has also developed and produces its own E-beam resists in-house.

Companies Exited

There are a number of companies that were developing E-beam machines for the commercial direct write and maskmaking market that have terminated their E-beam programs. These companies exited E-beam technology generally for one or more of the following reasons: 1) advances in optical and X-ray lithography, 2) the high cost of development, 3) the slow pace of development, and 4) lack of sales where a product was available. A discussion of these companies is included in order to give a complete perspective on the E-beam market.

Control Data Corporation

In the late 1960s, Control Data Corporation (CDC) began an E-beam development program that ultimately became the company's Micro Bit division. It was working on a "fly's eye"-type direct write system, similar to the Veeco machine, which was to become available in 1990. CDC was also working on an E-beam reticle generator, which was to be available in 1986 or 1987. In early 1984, CDC decided to sell the division because it no longer fit into the corporate strategy. Also, CDC could no longer afford the operation using internal funds, and was not successful in obtaining outside funds to keep it going.

A management group from the Micro Bit division performed a leveraged buy-out and set up operations as MultiBeam. MultiBeam completed an engineering model of a reticle generator using an E-beam column with dimensions of 3cm x 20cm. However, it was not successful in obtaining long-term funding to complete the program, and in July 1984, MultiBeam was dissolved and the entire 60-person staff was hired by Varian in an attempt to further its own direct write E-beam development program. It is interesting to note that since Varian has announced the shutdown of its E-beam program, the MultiBeam employees of Varian have left Varian to set up their own company, also to be called MultiBeam. As of January 1986, they are negotiating to purchase Varian's remaining maskmaking equipment and set up an independent mask shop.

GCA

GCA began working on development of an E-beam direct write system in 1976. The GCA machine's writing method was similar to the IBM EL-3 machine described above. The deflection field was divided into

subfields, and within each subfield a variable-shaped rectangular beam was used to write the pattern geometry. Within the subfield, the beam was vector scanned, while raster scanning was used to move from subfield to subfield. When the entire deflection field was written, the X-Y stage stepped to the next deflection field.

GCA abandoned its E-beam program in 1983, citing advances in optical and X-ray lithography and enormous development costs as the reasons. It is estimated that GCA had invested more than $25 million in the program.

General Signal

In 1980, General Signal entered the E-beam arena by investing in Electron Beam Microfabrication Corporation, but withdrew its funding in 1984. For further information see Electron Vision below.

Thomson-CSF

In the early 1970s, the Sescosem Division of Thomson-CSF also began an in-house E-beam program. Its efforts eventually culminated in a fourth-generation machine called the Fast Electron Beam Pattern Generator (FEPG), which was intended for both in-house use and for commercialization. E-beam equipment manufacture was eventually turned over to Cameca, which is the scientific instrumentation subsidiary of Thomson-CSF. In 1982, the commercialized machine was put on hold, although DATAQUEST believes that in-house E-beam R&D is still continuing.

The FEPG is a vector scan, variable-shaped beam system designed for both direct write and maskmaking applications. It uses a stripe writing method with continuous stage motion similar to the Bell EBES approach seen in Figure 1, except that within the stripe, vector scan is used instead of raster scan as in the EBES-type machines. The Bell method also uses a Gaussian round beam versus the variable-shaped beam of the FEPG. Minimum resolution is 1 micron and minimum address size is 0.4 micron. For a pattern covering 50 percent of a 3-inch wafer and 1-micron lines, throughput is 10 wafers/hour. Throughput for 5-inch wafers is approximately 5 wafers/hour.

DATAQUEST does not know how many machines were built for internal use, but estimates that only three to four were built by the Sescosem division and sold in the merchant market at a price of $2.2 million each. This was before the program was turned over to Cameca. Cameca had not sold any machines when the program was put on hold in 1982.

In January 1986, Thomson-CSF announced that it had exclusively licensed the FEPG technology to Cambridge Instruments.

E-Beam Equipment

Varian

Varian Extrion also obtained a license from Bell Labs to produce an E-beam machine based on the Bell EBES technology. Varian's first machine, an advanced version of the Bell machine, was the EBMG-20, a 20 MHz raster scan system with a Gaussian round beam with a spot size of 0.5 micron. It was very similar in concept to the Perkin-Elmer MEBES I, and used the same "stripe scan" method of writing the mask or reticle. The first EMBG-20 was delivered to Ultratech in 1978.

In 1980, Varian shipped the first 40-MHz Ee-BES-40, which was a faster version of the EBMG-20, and in 1982/1983 the VLS series was introduced. There were three versions: the VLS-20, the VLS-40, and the VLS-80 for 20-, 40-, and 80-MHz operation. All three systems used LaB_6 sources and used basically the same raster writing method as employed in the earlier machines, but had improved performance. All of the foregoing machines, with the exception described below, were primarily intended for maskmaking applications, although there may be a few installations where limited R&D direct write work is being done.

In August 1984, Varian shipped a VLS-20HC system to AMI-Austria. This was a modified, high-current system intended for both maskmaking and direct write of custom devices, although DATAQUEST believes that direct write has the higher machine priority. With the aid of direct write lithography, AMI-Austria is able to obtain four-week turnaround of 64K and 128K ROMs, from customer code approval to volume shipment of packaged parts. DATAQUEST believes that this was the first installation of an E-beam direct write system by a merchant ASIC manufacturer in Europe.

Table 3 lists Varian's total shipments from the initial delivery in 1978 through the closing of the Lithography Division in 1985. A total of only 16 machines were delivered, for a total revenue of $30 million over the life of the product.

Table 3

SHIPMENTS OF VARIAN E-BEAM MASKMAKING EQUIPMENT

	1978	1979	1980	1981	1982	1983	1984	1985	Total
Units	1	1	4	4	2	2	2	0	16
$M	$1.3	$1.8	$7.1	$8.0	$4.3	$4.6	$2.9	$ 0	$30

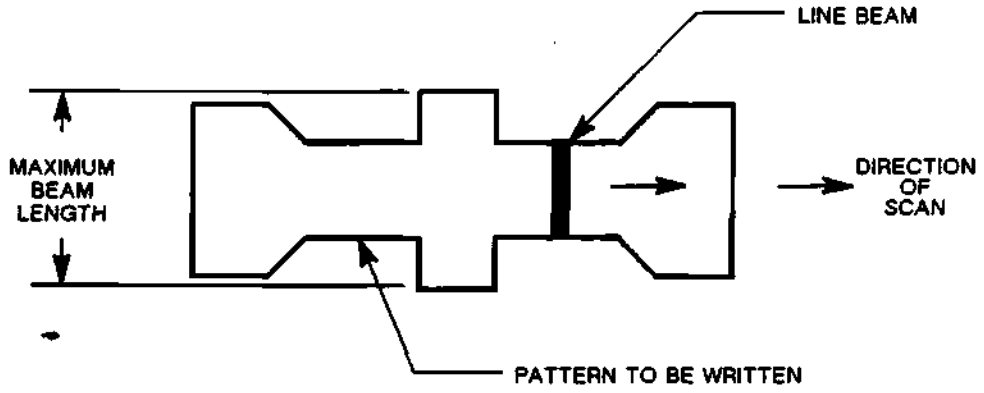
Source: DATAQUEST
January 1986

E-Beam Equipment

In 1980, Varian received a $4.5 million contract from the Air Force under Phase III of the VHSIC program to develop the major subsystems of an advanced E-beam direct write system for submicron lithography. The result of that program was the VLS-1000 machine, which used a unique writing method called the variable line scan. In this technique, the beam is a narrow line whose length and position are varied continuously. In Figure 3, the line beam starts at the left side of the pattern and is swept to the right with the beam length varying with the pattern height. The entire wafer is divided into 100-micron-square subfields, and within a subfield, the beam is vector scanned between shapes. The X-Y stage moves continuously in a serpentine movement to sequentially write all the subfields on the wafer.

Figure 3

VARIAN VLS-1000 LINE BEAM WRITING



Source: Varian

E-Beam Equipment

The VLS-1000 could write 0.5-micron minimum features and overlay accuracy was 0.15 micron. Throughput was 10 to 15 4-inch wafers/hour for geometries in the 0.75-micron range, and for applications with lower resolution requirements such as personalization of gate arrays, throughputs of 30 to 40 wafers/hour might be obtained.

Varian announced the $3 million VLS-1000 in 1982, with first deliveries to begin in 1983. However, because of delays in the program, machine availability was pushed into 1985. In an effort to beef up the program, in 1984 Varian acquired the entire 60-person staff of MultiBeam, Inc., and MultiBeam was subsequently dissolved. Varian still had not delivered a VLS-1000 system when it announced the closing of its Lithography Division in April 1985.

Varian's reasons for closing the Lithography Division, which included both the E-beam and X-ray product lines, were the delays and problems in the VLS-1000 program, the uncertain future of the X-ray market, and the advances made in optical lithography. Varian was also unable to penetrate the maskmaking market, and over the life of the product there were only 16 systems sold. The closing of the division left Varian with a $23 million pretax write-off. It is apparent that as with other companies, Varian's attempt to enter the E-beam market has proved to be a costly one.

As of December 1985, Varian was attempting to dispose of the division's technology and assets. Cambridge Instruments has been negotiating with Varian to acquire the X-ray technology. In December, a group of employees of the division, composed of members of the former MultiBeam staff, formed their own company to acquire various assets of Varian's E-beam unit. The new company, also called MultiBeam, is currently seeking financial backing. MultiBeam's intent is to initially set up an E-beam maskmaking shop and, as a longer-term goal, to develop equipment incorporating E-beam technology.

Veeco

In October 1979, Veeco announced the completion and initial testing of a laboratory model of an E-beam system based upon technology purchased from SRI. Research and development of the lab model and initial testing were done in cooperation with SRI at the SRI facility. The system used an SRI-patented lens (fly's eye lens), which split the electron beam into as many beams as there are die on the wafer. The individual beams, or beamlets, which could number in the hundreds, all write the die simultaneously on the wafer. Veeco's goal was to provide a commercial version of the machine that would have a throughput of 60 wafers/hour by late 1980.

E-Beam Equipment

The fly's eye concept had been researched since at least the early 1970s, but had some problems associated with it. They included a limited beam current in the individual beamlets, which would mean a tradeoff between resolution and throughput, and distortion, which would limit overlay accuracy. It is very difficult to fabricate the electron beam optics to provide an array of identical, controllable beamlets. GCA had also investigated this technology, but decided it was not a viable technique for production.

In November 1982, Veeco halted all work on the E-beam project. It said that progress was slower than expected and that the program would continue to require substantial investment. Also, return on investment would be over a longer term than was originally planned and considered advisable. It is estimated that Veeco had already invested $16 million to $18 million in the program when it was terminated.

Active Participants

There are nine companies providing E-beam direct write and maskmaking systems on the commercial market. Several of the companies are also major scanning electron microscope manufacturers (Cambridge, Hitachi, JEOL, and Philips), and it is this prior experience in E-beam that has led them into E-beam lithography. Several of the companies (Hitachi, Philips, and Toshiba) began their E-beam programs to satisfy internal needs, but eventually provided commercial systems. Note that the only significant U.S. supplier is Perkin-Elmer.

Cambridge Instruments

Cambridge Instruments, a British company, produced the world's first commercial scanning electron microscope in 1964. It began E-beam work in 1968 under a contract with the British government, and in 1972, it introduced its first commercial E-beam machine, the EBMF 1, which sold for $250,000. Cambridge's current line of E-beam machines includes the EBMF 2.5 ($1.25 million), the EBMF 6.5 ($1.5 million) and the EBMF 10.5 ($2 million). All of the machines use vector scanning of a Gaussian beam within the deflection field. Step and repeat of the stage is used to move to the next deflection field.

The EBMF 10.5 was introduced in 1984 and is the newest machine in the product line. It was also the first Cambridge machine specifically designed for production use (direct write and maskmaking); the previous machines were primarily for developmental work and low-volume prototyping. Altogether, Cambridge has an installed base of 62 E-beam systems, including 5 of the new EBMF 10.5 machines. Approximately

60 percent of the machines are used for direct write applications, 20 percent for maskmaking, and the remaining 20 percent for general-purpose use. Forty percent are installed in the United States, with most of the rest installed in Europe.

A primary application for the EBMF 6.5 has been direct write on gallium arsenide, with some geometries as small as 0.3 micron. An emerging commercial application is the use of direct write E-beam in the fabrication of ASICs, and both Fairchild in Milpitas and Array Logic in England have purchased EMBF 10.5s to fabricate gate arrays.

Array Logic intends to use E-beam direct write to address the quick-turn prototype and low-volume ASIC markets. Array Logic will provide customers with quick-turnaround ASIC prototype chips, which will allow customers to design silicon directly into their prototype systems. DATAQUEST believes that Array Logic is the first European merchant company to use E-beam direct write for fast-turn prototyping.

Electron Vision

Electron Beam Microfabrication Corporation (EBM) was formed in 1975 with the purchase of Radiant Energy Systems' E-beam technology. Radiant Energy Systems had been working on E-beam since 1969, and was developing an R&D prototype E-beam 1:1 projection system for the Naval Ocean Systems Center, San Diego, from the original Westinghouse patents. In 1980, EBM became an affiliate of General Signal. However, General Signal, the sole investor in EBM, withdrew its funding at the end of 1984. The founder of EBM purchased the E-beam technology from General Signal and formed Electron Vision in early 1985.

EBM delivered the final version of the E-beam 1:1 projection system started by Radiant to the Naval Ocean Systems Center in 1977. In 1978, EBM received a new contract to develop a second generation 1:1 projection system, which was subsequently shipped to the Naval Ocean Systems Center.

Recently, Electron Vision has sought funding to develop a production version of an E-beam 1:1 projection stepper that can do die-by-die alignment over the entire wafer. There would be no mechanical motion of either the wafer or the mask and, consequently, an X-Y stage would not be required. Alignment is accomplished by deflecting the electron beam to selectively illuminate each die site. Electron Vision says that it has demonstrated 0.5-micron resolution and 0.05-micron alignment accuracy and the system should be capable of 60 to 100 wafers/hour throughput. While other companies, including Philips and Toshiba, are developing full-field 1:1 E-beam projection systems, DATAQUEST does not know if they are working on E-beam steppers as well.

Radiant was also working on a scanning E-beam system, and had provided two systems to the Air Force and Honeywell. EBM further developed the system and provided an upgraded version to Burroughs in 1980. It was used in Burrough's bubble memory program, which has since been cancelled. The E-beam machine used a combination vector scan and high-speed raster scan writing method. It used a tungsten thermal field emission source to give a very high brightness so that optical photoresists could be used.

In 1980, EBM received a contract under Phase III of the VHSIC program to provide advancements in E-beam direct write technology based on EBM's scanning system with the high brightness source. EBM shipped this system, called the Waferwriter, to the Naval Ocean Systems Center in early 1985. The Navy will use the system to fabricate custom VLSI devices for the VHSIC program, to fabricate masks, and to manufacture limited quantities of obsolete ICs that are no longer available in the commercial market but still are being used in naval electronics.

Throughput of the Waferwriter is about four to five wafers/hour. EBM had introduced the Waferwriter to the commercial market at a price of $2.25 million, but had not sold any when General Signal withdrew its funding. Electron Vision will continue to market the product.

Altogether, EBM sold a total of six scanning and projection E-beam machines, including those provided by Radiant Systems.

Elionixs

Elionixs is a Japanese company that was spun out of JEOL in the late 1970s. Its principal product is a SEM-type, tabletop, direct write E-beam machine that uses a round beam with raster scanning. This is an inexpensive machine (about $200,000), designed to be a "starter" machine for companies that want to begin to investigate direct write E-beam on a small scale. It is also used for evaluation of E-beam resists. Elionixs' machines are not available in the United States. DATAQUEST does not have market estimates for them at this time.

Hitachi

In 1978, Hitachi announced the development of the EB52, a Gaussian round beam system that was used for laboratory direct write and maskmaking applications. This led to the EB55, which was announced in 1981. The EB55 was a 30-kV step-and-repeat machine with a variable-shaped rectangular beam. It had a 2.6-millimeters-square deflection field, which was further divided into subfields. The subfields were selected by magnetic deflection, and within each subfield the variable-shaped beam was vectorially scanned with electrostatic

deflection. Although capable of 0.5-micron minimum line widths and ±0.1-micron (3 sigma) overlay accuracy, the throughput was only about one wafer/hour. Thus, the EB55 was not practical for manufacturing applications.

Hitachi's current machine, the HL-600, is based on the EB55 and was developed to provide a higher-throughput machine that could be used for production maskmaking and direct write applications. The HL-600 operates in either a high-accuracy mode for maskmaking or a high-throughput mode for direct write. Table 4 lists some of the HL-600's specifications.

Table 4

HITACHI HL-600 SPECIFICATIONS

	High Accuracy	High Throughput
Minimum Line Width	0.5um/1um	0.5um/1um
Overlay Accuracy	0.1um	0.2um
Stitching Accuracy	0.1um	0.2um
Deflection Field	3.2mm square	6.5mm square
Address Increment	0.025um	0.05um
Throughput	3 masks/hour (5" mask)	10 wafers/hour (4" wafers)

Source: Hitachi

Hitachi uses the HL-600 internally and, in 1983, it was introduced to the commercial market in the United States and Japan. The average selling price is $2.5 million. To date, no machines have been sold in the United States. One possible drawback to its marketing success in the United States is that the HL-600 uses a Hitachi computer. DATAQUEST estimates that Hitachi has built 18 E-beam machines altogether, of which 13 are internal systems and 5 are installed outside of Hitachi. Of the 18 machines, we estimate that 9 are used for direct write and 9 are used in maskmaking.

Hitachi has recently announced a multiple E-beam column system for direct write and maskmaking. In this system, a single-pattern generator subsystem controls several E-beam columns simultaneously, thus boosting throughput. Each column can achieve a throughput of ten 4-inch wafers/hour or five 6-inch wafers/hour. Nominal feature size is 0.5 micron, but features as small as 0.2 micron can also be obtained. Overlay accuracy is 0.15 micron.

The E-beam system with two columns will start at $6 million, with each additional column costing $2.4 million. First deliveries are scheduled to start in October 1986.

JEOL

JEOL's E-beam experience goes all the way back to 1949 when it made available its first transmission electron microscope. JEOL commercialized Japan's first scanning electron microscope in 1966 and completed its first E-beam lithography machine in 1967. The current JBX-5 and JBX-6 series of E-beam equipment was preceded by the earlier JBX-2, -3, and -4 series.

Over the past several years, JEOL has had two parallel lines of E-beam lithography equipment. The JBX-5 series was first introduced in 1978. The latest model in the series, the fine-line JBX-5DII, was introduced in 1983 and is designed for basic research. It is a step-and-repeat system that uses a Gaussian round beam that can form a spot as small as 80 angstroms. The writing system is similar in concept to the Cambridge or Philips machines. Within the deflection field, the Gaussian beam is vector scanned to the geometric area to be written and then the beam is raster scanned to fill in the area. The JBX-5DII is automatically switchable between 25 kV and 50 kV. The 50 kV mode is used with the smaller spot size for producing Josephson and gallium arsenide devices, optoelectronics, and other devices with nanolithographic features. The 25 kV mode is used with a larger spot size with a higher-current density for producing devices with coarser geometries at higher throughputs.

There are more than 40 of the JBX-5 series installed. There are two in Europe, five in the United States, and the rest are in Japan. The U.S. machines are at the University of Michigan, Cornell University, Bell Labs (two), and Bell Communications (one). The average selling price of the JBX-5DII is $1.5 million.

JEOL also has the JBX-6 series, which was first introduced in 1977. The latest model in the series, the JBX-6AII, was introduced in 1982 and is designed for production direct write and maskmaking applications. The JBX-6AII is a step-and-repeat system similar to the IBM EL-3 described

earlier. It uses a variable-shaped rectangular beam to write subfields within the larger deflection field. However, the JEOL machine uses not only vector scan to write within the subfield, but also uses vector scan to move between subfields. The EL-3, on the other hand, raster scans between the subfields and visits each subfield in turn.

Of the 40 JBX-6 series machines sold since the series introduction in 1977, approximately 20 have been JBX-6AIIs, which have an average price of $2.5 million. To date, three JBX-6AII machines have been installed in the United States. One is at Hewlett-Packard, where it is being used in direct write R&D, and the other two are at Harris and Honeywell, where they are being used in the VHSIC program, also for direct write R&D. DATAQUEST believes that the other 37 machines are all installed in Japan for either direct write or maskmaking applications.

Table 5 lists some key specifications for the JBX-6AII and JBX-5DII. In addition, note that both machines utilize the DEC PDP 11/44 computer, which could enhance their marketability in the United States.

Table 5

SPECIFICATIONS OF JEOL E-BEAM MACHINES

	JBX-5DII	JBX-6AII
Accelerating Voltage	25kV/50kV	20kV
Beam Shape	Round	Variable rectangular
Beam Size	80A to 1um	12.5um max on a side, max area 65um^2
Writing Method	Step and repeat Vector scan with raster fill-in	Step and repeat Subfield vector scan
Deflection Field	1.5mm square (25Kv) 0.75mm square (50Kv)	2.5mm square
Stitching Accuracy	0.2um	0.1um
Overlay Accuracy	0.25um (3 sigma)	0.15um
Address Increment	0.025um	0.05um
Minimum Feature Size	----	0.5um
Substrate	3" wafer	5" wafer 6"x 6" plate
Throughput	-----	10 4" wafers/hour 10 5" plates/hour

Source: JEOL

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From an application point of view, the main difference between the two series is the minimum obtainable geometries. The JBX-6AII is a production machine used primarily for geometries down to about 0.5 micron, while the JBX-5DII is a research machine used for geometries down to about 0.02 micron. Both machines are used for direct write and maskmaking. Of the 80 JBX-5/6 series machines installed worldwide, 70 are installed in Japan. DATAQUEST estimates that for the Japanese installations, 70 percent are used for direct write and 30 percent for maskmaking. However, in some installations the same machine is used for both applications.

Perkin-Elmer

ETEC, located in Hayward, California, was formed in 1970 to provide modified scanning electron microscopes for laboratory E-beam use. The company's system, called the LEBES (laboratory electron beam exposure system), was introduced in 1973. In 1975, ETEC obtained a license from Bell Labs to use Bell's E-beam technology, and in 1977 ETEC shipped its first MEBES (manufacturing electron beam exposure system). The MEBES used the same writing technique described above for the Bell EBES, but was an advanced version of the Bell machine. In 1979, Perkin-Elmer acquired ETEC.

The MEBES III is the latest version in the series, which included the MEBES I, IA, IB, and II. First shipments for the MEBES III occurred in 1983. Table 6 shows the evolution of the series.

The MEBES series is specifically designed for maskmaking applications and is in use in maskmaking shops throughout the world. Virtually all of the MEBES machines are used for maskmaking, although there may be a few isolated, infrequent instances of direct write use. DATAQUEST estimates that Perkin-Elmer has shipped a total of 95 MEBES machines since the introduction in 1977 through 1985. Perkin-Elmer is clearly the world leader in installed base of maskmaking equipment.

Under the VHSIC program, Perkin-Elmer has developed the AEBLE-150 direct write E-beam machine. The AEBLE-150, which costs $3.5 million, is a vector scan, variable-shaped beam system using the stripe method of writing the wafer (Figure 1b). The writing method of the AEBLE 150 is similar to the Thomson-CSF FEBG whose E-beam technology was recently licensed to Cambridge Instruments. The beam shaper will produce rectangles and triangles with edge dimensions of 0.25 to 2.0 microns. The deflection field is two millimeters square and is divided into 60-micron subfields. Writing is done on the fly with a continuous stage motion. The first AEBLE-150 was accepted by the Army in February 1985; the next two units will be shipped in 1986 and will probably go to VHSIC contractors TRW and Motorola. European Silicon Structures, a start-up ASIC manufacturer, has also ordered an AEBLE-150 for delivery in 1986.

Table 6

EVOLUTION OF THE PERKIN-ELMER MEBES SERIES

	MEBES I	MEBES II	MEBES III
Data Rate	20 MHz	40 MHz	80 MHz
Beam Size	0.24-1.0um	0.24-1.1um	0.10-1.1um
Address Size	0.25um, 0.50um	0.20-1.1um	0.10-1.1um
Overlay Accuracy	±0.25um	±0.125um	±0.12um
Maximum Mask Size	5" x 5"	7" x 7"	7" x 7"
Loading System			
Capacity	2	10	10
Operation	Manual	Auto	Auto
Cathode Type	C-Th-W	LaB_6	LaB_6
Price ($M)	$1.3	$2.0	$2.7

Source: Perkin-Elmer
DATAQUEST
January 1986

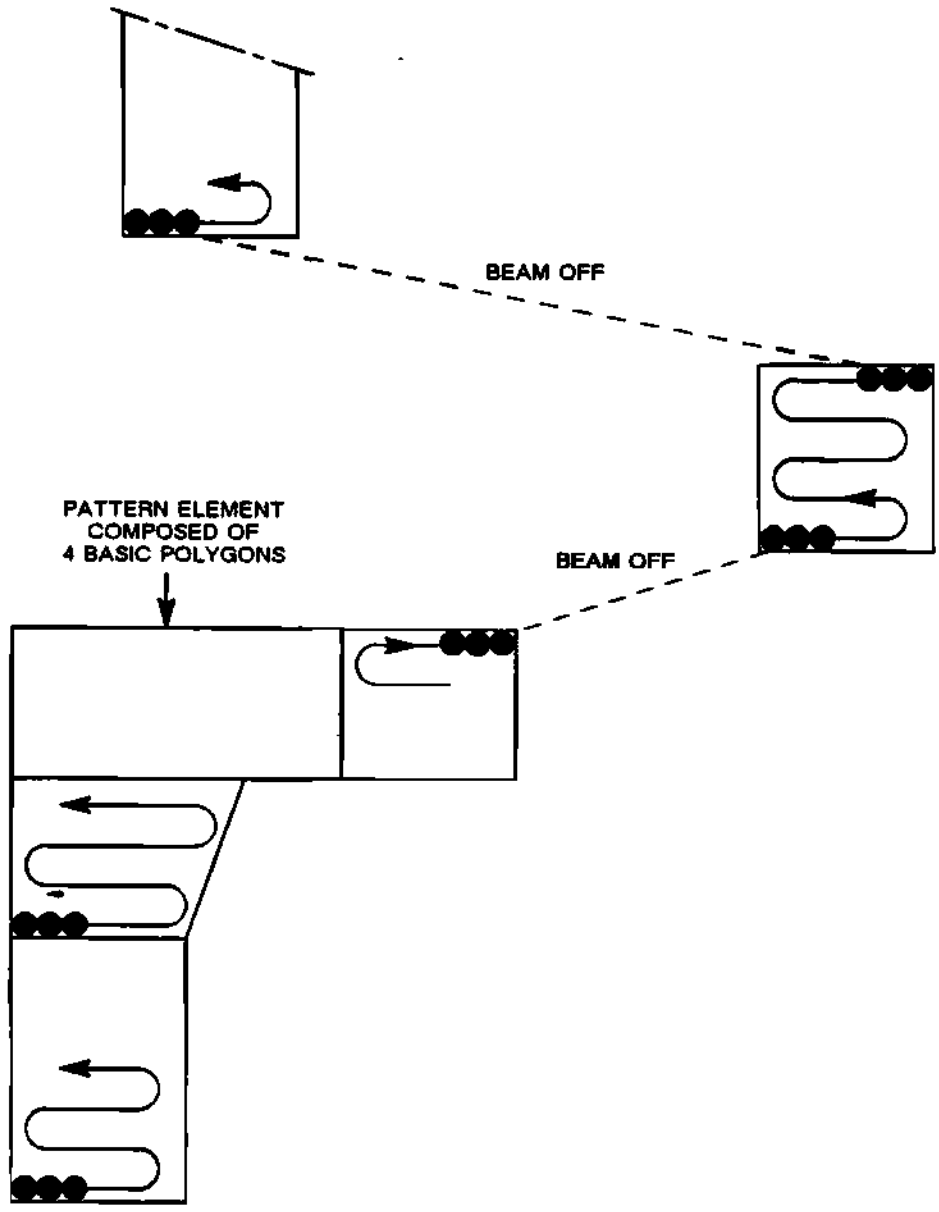
Philips

Philips has considerable experience in E-beam technology, since it has provided electron microscopes for the past 35 years. It was this experience that led the company to develop E-beam machines for in-house use. Its first commercial machine was the EBPG-3 Beamwriter, a third-generation system that was introduced in 1978 after ten years of development. The EBPG-3 was the first commercial vector scan machine and was designed for both direct write and maskmaking applications.

The Beamwriter uses a combination of vector and raster scanning. The beam is vectorially scanned to each pattern element to be written, but within each pattern element the beam is raster scanned with a Gaussian round spot (see Figure 4). The Beamwriter is programmed by describing the pattern element as a combination of rectangles, triangles, and trapezoids. The data to describe the area to be written are smaller than in a EBES-type raster scan system--only the corners of the boundaries need to be specified for each polygon. The Beamwriter steps the round beam at a maximum 10-MHz rate to fill in the polygons.

Figure 4

PHILIPS BEAMWRITER SCAN SYSTEM



Source: Philips

E-Beam Equipment

Philips introduced the EBPG-4 Beamwriter in May 1985, with first deliveries to begin in 1986. It is priced at $2 million, compared with an average selling price of $1.8 million for the EBPG-3. The EBPG-4 is fundamentally the same as the EBPG-3, but many of the items that were previously options are now standard on the new Beamwriter. Table 7 lists some of the EBPG-4 machine parameters.

Table 7

PHILIPS EBPG-4 BEAMWRITER SPECIFICATIONS

Substrate Size	125mm wafers 6"x 6" mask plates		
Writing Method	Vector scan with raster fill-in		
Scan Rate	Variable between 0.1 and 10 MHz		
Spot Size	Variable between 0.025 and 1um		
Deflection Field	1.6mm x 1.6mm 0.8mm x 0.8mm 0.4mm x 0.4mm		
Beam Energy	20 keV and 50 keV		
Minimum Line Width	Beam Energy	Field Size	Line Width
	20 keV	1.6mm x 1.6mm	0.3um
		0.8mm x 0.8mm	0.2um
		0.4mm x 0.4mm	0.15um
	50 keV	0.8mm x 0.8mm	0.15um
		0.4mm x 0.4mm	0.1um
Overlay Accuracy	0.1um for direct write (2 sigma)		

Source: Philips

Altogether, there are 11 EBPG-3s installed for direct write and maskmaking applications. Three of the 11 machines are in-house units at Philips' Central Research Laboratory. Recently installed commercial machines, as well as units on order but not yet delivered, are primarily for direct write on gallium arsenide wafers. For example, Alpha Industries, of Woburn, Massachusetts, will be using the EBPG-3 for production of gallium arsenide microwave ICs. The company will also use it for maskmaking.

Philips has also been working on an E-beam 1:1 projection system for many years. In its system, a chrome mask coated with cesium iqdide is illuminated by an UV source, which causes electrons to be emitted from the cesium iodide. The opaque areas of the mask block the electrons while the clear areas allow the electrons to pass through. Thus, the electron beam contains the image of the mask. The electrons are then accelerated by a 20-keV field and focused onto the wafer. Mask-to-wafer separation is 5 millimeters. The machine can expose features as small as 0.2 micron. The time required to align and expose a wafer is only about 30 seconds. However, because of overhead requirements, throughput is about 25 4-inch wafers/hour.

Advantages of this technology are: it is a simple and inexpensive machine that requires few precision parts and does not require an X-Y stage, machine control requires only a moderately priced microcomputer, and depth of focus is on the order of 100 microns compared with 5 microns for optical tools. A drawback to the technology is the effect of image distortion and wafer bow or warpage on registration, although Philips has demonstrated 0.1-micron registration in its labs. Currently, Philips has four working lab prototypes.

Toshiba

Toshiba, in conjunction with Japan's VLSI Project, developed E-beam technology that resulted in the EBM-105 machine. The EBM-105 was first offered commercially in 1978 at a price of $2 million. This system, using a Gaussian round beam with a minimum spot size of 0.2 micron, was a raster scan system similar to the Bell EBES approach shown in Figure 1. Like the Bell, Varian, and Perkin-Elmer machines, the EBM-105 scans a 256-micron-wide stripe in one direction, while the stage continuously advances in the orthogonal direction. The adjacent stripes are written until the entire substrate is written.

The EBM-105 could write 1.0-micron minimum lines. Toshiba later introduced the EBM-105R at a price of $1.3 million. It was basically the same machine, but was intended for reticle production only as it was limited to writing a 4.0-micron minimum line. Current Toshiba machines are the EB-130 and EB-140, which use the same writing technique but are upgraded machines.

Toshiba also reports that it has developed a direct write E-beam system for the in-house development of 4-Mbyte and 16-Mbyte DRAMs. This machine is a small-deflection, raster scan system, which operates at 50 keV to reduce proximity effects. Toshiba reports that there is no increase of radiation damage of the substrate at 50 keV over that at 20 keV. Toshiba is also investigating the use of double-exposure E-beam in the development of 64Mb DRAMs with design rules of 0.25 micron.

E-Beam Equipment

DATAQUEST estimates that Toshiba has built 16 E-beam machines for maskmaking, and that 3 are used internally and the remaining 13 machines are all external installations in Japan. In production maskmaking E-beam, Toshiba ranks third in Japan behind Perkin-Elmer and JEOL.

Carl Zeiss

It has been reported that Zeiss of Jena, East Germany, has been working on E-beam development in cooperation with the Soviet Union since the 1970s. The ZBA-10 was available as early as 1978, and ten of these systems were reportedly installed in Eastern Europe. This machine was followed by the ZBA-10/1 in 1980, which was a vector scanning machine using a programmable rectangular beam that was variable in one dimension only. The beam could be varied from 0.1 micron to 12 microns on a side. The ZBA-10/1 had four times the productivity of the ZBA-10 and could be used for both direct write and maskmaking.

The ZBA-20, introduced in 1982, used the same type of scan system as the ZBA-10/1, but provided a factor of ten improvement in productivity over the ZBA-10/1 because of a faster data transfer rate. Zeiss claimed that the ZBA-20 could write eight 3-inch wafers/hour with 256K DRAM complexity, and was capable of 0.2-micron resolution and 0.15-micron registration. It could also write 45-degree lines by using a patented process to electromagnetically rotate the E-beam by 45 degrees. The ZBA-20 can handle 6-inch wafers and 7-inch mask substrates. DATAQUEST includes this information for completeness, but have been unable to verify it.

VHSIC PROGRAM

The VHSIC program approach is to develop two generations of advanced, high-speed, high-performance silicon chips for digital signal processing. Phase I was begun in May 1981 to build the first generation of chips having minimum feature sizes of 1.25 micron. Phase II was begun in 1984 to develop second-generation submicron silicon chips with minimum features as small as 0.5 micron. Accordingly, one part of the VHSIC program was to develop an advanced E-beam lithography tool to do the submicron geometries. The major VHSIC support for E-beam lithography has been an Army contract with Hughes Research Labs and Perkin-Elmer to develop a machine capable of 0.5-micron line widths at throughput rates that are economically acceptable for chip production.

E-Beam Equipment

Varian Associates and Electron Beam Microfabrication (EBM) also received some funding from the VHSIC program to assist them in their own internal E-beam development efforts. It should be noted that the three companies were developing basically different E-beam systems: Perkin-Elmer was working on a variable-shaped beam system, Varian on a variable line scan system, and EBM on a Gaussian round beam system with a thermal field emitter.

Perkin-Elmer's prototype system, which has been commercialized as the AEBLE 150, has been factory accepted by the Army, but has not yet been delivered to Hughes. The first production AEBLE 150 systems will be delivered to Phase II VHSIC contractors in 1986. Varian, who received some funding from the Air Force to develop the VLS-1000, offered its system to the commercial market in 1984, but had not taken any orders for the system when it terminated its Lithography Division. EBM received assistance from the Navy to develop the Waferwriter. EBM did deliver a prototype machine to the Navy, but EBM's E-beam program never got off the ground as General Signal terminated its funding of EBM. Thus, Perkin-Elmer is the sole survivor of the VHSIC E-beam program that began in 1981.

In September 1985, the Army awarded a contract to GCA to develop an optical stepper capable of producing minimum feature sizes of 0.75 microns in silicon and gallium arsenide. The stepper, to be delivered in 1989, marks the first move into optical lithography for the VHSIC program. This change in emphasis results from the high cost and low throughputs of E-beam lithography and the continual advances that have been made in optical lithography. Initially, when the VHSIC program goals were defined, it was not foreseen that optical lithography could be used in submicron device fabrication. Today, with optical lithography in the lab approaching 0.5 micron, the role of E-beam in the VHSIC program remains uncertain.

MARKET ANALYSIS AND FORECAST

Table 8 shows the total worldwide installed base of E-beam systems through 1985 by manufacturer. This table includes the merchant manufacturers as well as the companies that manufacture only for their own internal use. Some companies, such as Hitachi, Philips, and Toshiba, build systems both for the commercial market and for their own internal needs. In many instances, particularly for E-beam machines manufactured by Cambridge, Hitachi, JEOL, and Philips, the systems are used for both direct write and maskmaking applications, and best estimates were made of their major use.

E-Beam Equipment

Table 8

TOTAL WORLDWIDE INSTALLED BASE BY MANUFACTURER
OF E-BEAM SYSTEMS THROUGH 1985
(Units)

	Maskmaking	Direct Write	Total
AT&T	4	1	5
Cambridge Instruments	19	43	62
Electron Beam Microfabrication*	-	6	6
Hewlett-Packard	-	3	3
Hitachi	9	9	18
IBM	5	35	40
JEOL	27	73	100
Perkin-Elmer	95	-	95
Philips	4	7	11
Texas Instruments	10	6	16
Toshiba	16	0	16
Varian	16	0	16
Carl Zeiss (Jena)	5	5	10
Others	5	10	15
	215	198	413

*Includes units built by Radiant Energy Systems

Source: DATAQUEST
January 1986

A total of 198 direct write and 215 maskmaking systems have been installed for a total installed E-beam base of 413. The "other" category includes such organizations as Hughes Research, Thomson-CSF, Cambridge University, and Japan's Nippon Telegraph and Telephone. JEOL is clearly the leader in direct write systems with 73, while Perkin-Elmer, with 95 MEBES installations, is the leader in maskmaking.

Table 9 shows E-beam shipments by units and dollars for the merchant equipment manufacturers from 1977 through 1985. The year 1977 marks the real emergence of the commercial market, as several commercial systems

(JEOL's JBX-6 series, Perkin-Elmer's MEBES, and Varian) first became available that year. This table includes only the systems sold on the commercial market and does not include systems built and used internally, nor the machines shipped prior to 1977. Hence, the difference in unit totals between Tables 8 and 9.

Table 9

E-BEAM SHIPMENTS BY MERCHANT EQUIPMENT COMPANIES

	1977	1978	1979	1980	1981	1982	1983	1984	1985	Total
Units										
Maskmaking	4	12	13	21	15	20	22	28	34	169
Direct Write	5	10	12	10	9	11	14	17	15	103
Total	9	22	25	31	24	31	36	45	49	272

Millions of Dollars	1977	1978	1979	1980	1981	1982	1983	1984	1985
Maskmaking	$ 6.1	$17.9	$19.5	$36.6	$28.2	$37.6	$45.8	$63.2	$ 84.2
Direct Write	5.0	11.6	14.6	13.3	11.6	16.2	22.0	29.8	29.5
Total	$11.1	$29.5	$34.1	$49.9	$39.8	$53.8	$67.8	$93.0	$113.7

Source: DATAQUEST
January 1986

Table 9 also includes maskmaking machines used in both R&D and production. When the R&D maskmaking machines are subtracted, and the noncommercial machines built internally for production maskmaking are added back in, the result is the number of E-beam machines used worldwide for production maskmaking. DATAQUEST has done this, and we have found that the unit shipments of production maskmaking machines between 1977 and 1985, whether internally or externally built, is almost identical to the yearly maskmaking unit shipment data shown in Table 9. Thus, this table can also be used to estimate the installed base of all E-beam machines used in production maskmaking from 1977 to 1985.

As Table 9 indicates, the worldwide installed base of production maskmaking machines is 169 units through 1985. Table 10 gives the regional breakdown of these units.

In terms of revenue, the total commercial E-beam market in 1985 totaled $113.7 million, of which maskmaking machines accounted for $84.2 million, or 74.1 percent, and direct write for $29.5 million, or 25.9 percent. Table 11 shows the E-beam sales for the six commercial manufacturers. Again, only external sales are included.

Table 10

TOTAL INSTALLED BASE OF PRODUCTION MASKMAKING MACHINES
INTERNALLY AND EXTERNALLY BUILT

	Units	Share
United States	78	46%
Japan	73	43
Europe	16	10
Rest of World	2	1
	169	100%

Source: DATAQUEST
January 1986

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E-Beam Equipment

Table 11

1985 WORLDWIDE E-BEAM MERCHANT EQUIPMENT MARKET SHARE
(Millions of Dollars)

	Maskmaking	Direct Write	Total
Cambridge	$ 3.9	$ 9.0	$ 12.9
Hitachi	5.0	2.5	7.5
JEOL	8.0	16.0	24.0
Perkin-Elmer	64.8	-	64.8
Philips	-	2.0	2.0
Toshiba	2.5	-	2.5
Total	$84.2	$29.5	$113.7

Source: DATAQUEST
January 1986

Table 12 shows combined direct write and maskmaking E-beam shipments for the commercial manufacturers by region for 1983 to 1985. It is apparent that Japan was a larger market than the United States in 1984 and 1985, and one may erroneously conclude that, at least based on market size, there is more E-beam activity in Japan than in the United States. The reason the market is larger is that there is no large internal E-beam installed base in Japan and most of the E-beam equipment is supplied by commercial vendors--mainly JEOL. DATAQUEST believes that no Japanese semiconductor manufacturer, except Hitachi with 13 internal machines, has any substantial number of internal machines. Even Toshiba, a commercial supplier, has only a few of its own machines. On the other hand, IBM and Texas Instruments have together 56 internal machines. DATAQUEST estimates that IBM built 15 EL-3s in 1985, which represents a loss to the 1985 U.S. direct commercial market of $45 million in 1985. This is equal to the total 1985 U.S. commercial market of $44.7 million. Actually, this is not a complete loss, as DATAQUEST believes that IBM buys the E-beam columns from a commercial E-beam vendor. Although Texas Instruments may be returning to the commercial market, the U.S. market will continue to be understated by the value of the IBM machines.

E-Beam Equipment

Table 12

TOTAL E-BEAM SHIPMENTS BY MERCHANT EQUIPMENT COMPANIES
By Region

	1983			1984			1985		
	Units	Millions of Dollars	Share	Units	Millions of Dollars	Share	Units	Millions of Dollars	Share
United States	13	$26.0	38.3%	15	$31.2	33.5%	18	$ 44.7	39.3%
Japan	12	22.4	33.0	20	45.0	48.4	23	53.2	46.8
Europe	10	16.9	24.9	9	14.3	15.4	7	13.1	11.5
Rest of World	1	2.5	3.7	1	2.5	2.7	1	2.7	2.4
	36	$67.8	100.0%	45	$93.0	100.0%	49	$113.7	100.0%

Note: Percent totals may not add due to rounding.

Source: DATAQUEST
January 1986

Market Forecast

Table 13 gives the forecast E-beam equipment sales for the merchant vendors for the years 1986 to 1990. The forecast includes both production and R&D E-beam systems. We estimate that a total of 202 maskmaking systems with a market value of $626 million will be sold over these five years, compared with 119 units with a market value of $259 million for the previous five years (1981-1985). For direct write, 154 units with a value of $426 million will be sold, compared with 66 units with a value of $80 million for the previous five years. DATAQUEST forecasts that the total E-beam market for the years 1986 to 1990 will exceed $1 billion as compared with $339 million for 1981 to 1985.

In 1984, E-beam direct write sales were $29.8 million for a 3 percent share of the total lithography market of $936 million. In 1990, DATAQUEST forecasts that direct write sales will be $147 million for an 8 percent share of the total lithography market of $1,827 million.

Because of the advances in optical and X-ray lithography and the high cost of E-beam lithography, DATAQUEST does not believe that E-beam direct write will ever reach the earlier expectations for this market. The 1986 to 1990 forecast assumes that E-beam direct write will find a market niche in three areas: gallium arsenide, application-specific devices, and quick-turnaround prototype devices. The growth in E-beam direct write is consequently dependent upon the growth in these three market niches.

E-Beam Equipment

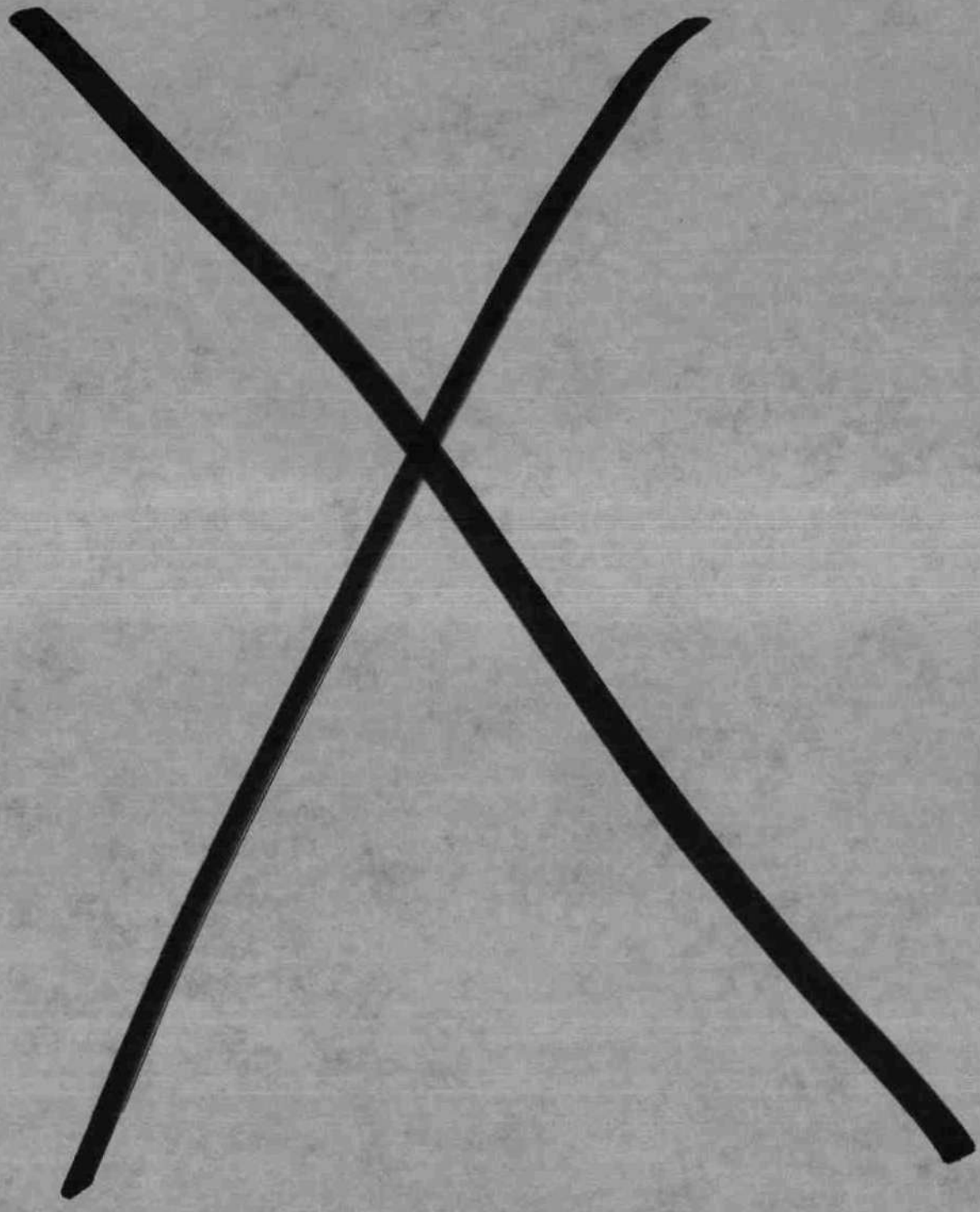
Table 13

FORECAST E-BEAM EQUIPMENT SALES BY MERCHANT COMPANIES

	Units						
	1986	1987	1988	1989	1990	Total 1986-1990	CAGR 1986-1990
Maskmaking	29	34	44	47	48	202	13.5%
Direct Write	19	23	29	37	46	154	24.7
	48	57	73	84	94	356	18.4%

	Millions of Dollars						
	1986	1987	1988	1989	1990	Total 1986-1990	CAGR 1986-1990
Maskmaking	$ 75	$ 96	$135	$154	$166	$ 626	22.0%
Direct Write	42	55	75	107	147	426	36.7
	$117	$151	$210	$261	$313	$1,052	27.9%

Source: DATAQUEST
January 1986



Etch/Clean

The following is a list of the material in this section:

- Dry Etch Processing

Dry Etch Processing

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Dry Etch Processing

SUMMARY

The semiconductor industry is rapidly approaching 1-micron and submicron lines in its quest for low-power, high-speed devices. Fine-line geometries demand changes in many wafer fabrication processes, and the etch process is no exception. In response to the demand, the industry is converting most of its etch processes from wet to dry etch. These dry etch processes can be subdivided into stripping, parallel-plate, which includes reactive ion etch (RIE), and ion-beam milling, which includes reactive ion-beam etching (RIBE).

We estimate that worldwide dry etch wafer processing equipment consumption was $406 million in 1985, down 2 percent from $414 million in 1984. Of this, $344 million was for parallel-plate applications, $45 million for barrels, and $17 million for ion-beam milling. We believe that worldwide consumption will drop 5 percent to $387 million in 1986 and then grow to $649 million in 1990, for a compound annual growth rate (CAGR) from 1985 through 1990 of 9.8 percent.

The wet process market for 1985 was $125 million, down 6.2 percent from $133 million in 1984. We estimate that it will decrease to $117 million in 1986 and then grow to $182 million in 1990, for a CAGR of 8 percent during that period. The percentage of layers that are wet etched will decrease from 58 percent in 1985 to 25 percent in 1990.

Dry etching is replacing wet etching because of the following advantages:

- Dry etching provides much better anisotropy (vertical etch profiles), which is required for small line dimensions.
- Dry etching obviates the handling and disposal of corrosive liquids, although care must be taken to protect the operator from hazardous gaseous by-products.
- Dry etch systems provide much better control of the etch process.
- Dry etch systems can do several steps in situ with one pump down, which reduces contamination that could be caused by several handling steps.

Production dry etching is being used successfully for most major semiconductor films. It has been used most widely in the past for silicon nitride and polysilicon films. Although a smaller portion of silicon dioxide layers are being dry etched, its production viability has been demonstrated and it is being more widely used. Aluminum etching has proven to be more formidable, especially where silicon and copper alloys are present, but it is still a production process for most semiconductor manufacturers.

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Dry Etch Processing

Many new processes that can only be done by dry etching are being developed. Some of these have already found their way into production semiconductor processing. One of these is the etching of multilevel photoresist for applications where severe topography reduces the resolution of photolithography. Another process is the etching of single-crystal silicon for the recessed local oxidation application, which decreases the cell area for new devices. Another is the deep trench isolation process in single-crystal silicon that provides isolation for n- and p-wells in CMOS devices. We are seeing the viability of dry etching in virtually every area of photoresist technology.

Because of the opportunities in this marketplace, the number of suppliers and new entrants has escalated. There are no less than 20 major competitors in this market today. Although most of those companies have grown rapidly, there have been considerable shifts in market share. We believe that the technology has not stabilized enough to predict long-term winners. There are emerging new technologies that could supplant current market leaders. Eventually, several niches will emerge to address different process requirements. Dominance in those niches will depend on machine excellence, product support, and process expertise.

WET CHEMICAL ETCHING

Traditionally, the most common method of etching a wafer patterned with photoresist is to submerge the wafer in a liquid chemical solution that attacks the exposed surface at a higher rate than the rate at which it attacks the photoresist. We estimate that 58 percent of mask layers are currently etched in wet chemical solutions.

Wet chemical etching has some very positive characteristics. The equipment used in the process is relatively inexpensive, and the process has very high selectivity (the difference in etch rates between the material in the layer that is being etched and the underlying layer).

Wet chemical etching also has some negative characteristics, however. It may be hazardous to personnel because of the potentially dangerous chemicals used in the solution. Furthermore, wet chemicals create a waste disposal problem. Another production problem can occur as the acids and bases in the solution are used up, causing the etch characteristics to change during the processing of a batch of wafers. This causes a lack of control in the etch process.

Dry Etch Processing

Wet chemical etching also has some serious technological limitations. It produces an isotropic etch (an etch that proceeds horizontally as well as vertically) that may lead to resist undercutting. In narrow lines, such as in VLSI, this can cause the line to etch laterally, thus erasing the line. It is also difficult to control the slope of the walls produced by the etch. Varying amounts of slope may be required in some applications in order to properly metallize in subsequent steps. These problems will become more critical as the industry approaches submicron lithography.

DRY ETCHING

Dry etch processing has production and technological advantages over wet chemical etching. Dry etching is safer because it requires fewer potentially dangerous chemicals in less volume, and because human operators are not directly exposed to the chemicals in the process. Furthermore, dry etching partially eliminates the waste disposal problem, and it reduces the problem of inconsistent etching associated with processing a batch of wafers in wet chemicals.

Among the technological advantages, dry etching allows some control over the slope of the etched sidewalls. Profiles can be varied from 60 to 90 degrees to fit the application, although such control is not a trivial matter. In wet etching, profiles are always concave because of the isotropy. Dry etching also provides the ability to etch multiple layers of several different materials in situ without undercutting the photoresist or degrading the profile. This feature can greatly reduce the contamination that would come from handling the wafer at each step.

Dry etching grew out of the vacuum industry. It uses an electrical discharge to partially ionize a gas (i.e., produce a gas plasma) in a vacuum chamber. Depending on the type of gas, reactive or inert, and the electrode configuration, the ions are used to chemically etch or sputter the material from the wafer surface. There are three generic categories of dry etching: stripping, parallel-plate etching, and ion-beam milling.

Strippers

Strippers are used for removing the photoresist from the wafer after the pattern has been etched or otherwise processed. The traditional method, which is still widely practiced, is to remove resist with wet chemicals. Strippers are becoming more popular because of the low cost and the elimination of personnel hazards caused by the dangerous chemicals. The most popular dry stripper is the barrel. However, because of some particularly tenacious resist residues, we have recently seen the emergence of single-wafer strippers.

Dry Etch Processing

Barrels

Barrels were first used for stripping resist. Their use was eventually extended to silicon nitride removal or patterning in cases where there were no requirements for anisotropy. These systems are simple in that they are manually loaded and use only a mechanical vacuum pump. Thus, their low cost ($20,000 to $60,000) and high throughput make them very cost effective.

The basic configuration is a cylindrical vacuum chamber with RF electrodes coupled to the outside. Wafer boats are loaded manually into the chamber (up to 100 wafers per load) and a low-pressure plasma (greater than 2 Torr or 2mm of Hg) isotropically etches the material from the substrate. The etch mechanism is that the chemically activated species in the gas form volatile gas by-products with the substrate, which are pumped out of the system. The electrical discharge imparts some anisotropy, but the profile is still mostly isotropic.

Single-Wafer Strippers

One of the most interesting new product areas in dry etch is that of single-wafer stripping. This technology is needed to minimize gate oxide damage and gate thickness loss and to increase stripping efficiency. Gate oxide damage occurs because, during stripping, the oxide is exposed to a plasma environment that contains high-energy ions and electrons, X-ray radiation, and sputtered contaminants from the processing chamber. Yield losses result from this oxide damage, since there is an attendant C-V shift and threshold voltage degradation. Although the results are not conclusive, one solution is to remove the wafer from this plasma environment by creating the plasma in an upstream chamber. In addition, by increasing the free radicals that impinge on the wafer, the etch efficiency is increased, which facilitates the removal of tenacious resist deposits such as result from high-current implantation.

Parallel-Plate

The parallel-plate application of plasma etching includes planar batch systems, single-wafer systems, and hexode systems. This technology was first developed at Texas Instruments (TI) in the late 1960s. The original TI configuration was a planar batch type and consisted of two electrodes with the upper electrode driven by an RF potential and the lower electrode grounded. The wafers were placed on the lower, circular electrode. This provided the first near-anisotropic etching in the industry.

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Dry Etch Processing

Since then, the parallel-plate technology has generated the types of systems mentioned above. The single-wafer version evolved from the original version by shrinking the chamber to hold one wafer only. The planar batch approach has also generated the reactive ion etch (RIE) configuration, in which the lower electrode, with the wafers, is RF powered. In another generation, the electrodes have been arranged in a vertical hexagonal structure (hexode) where the concentric inner electrode is RF driven. Finally, there are systems being built that power both electrodes, use magnetic enhancement of the plasma, employ multiple processing chambers, or use rotating electrodes.

Etch Mechanism

The basic mechanism in all these approaches is the creation between the electrodes of a plasma in a chemically reactive gas. Such a plasma develops a voltage drop (usually termed the sheath or dark space) from the plasma to the electrodes. The voltage drop imparts energy to the ions created in plasma and they impinge on the wafers, thus radiatively assisting the gas chemistry on the substrates. Each of the above approaches has its own set of constraints on the type of chemistries that can be achieved. Because of the sheath voltage, the parallel-plate method provides much more anisotropy than the barrel method. However, there can be considerable variation in the anisotropy, depending on which approach is used.

Plasma Etching

The term plasma etcher refers to the original approach with the cathode grounded. Such systems usually operate at greater than 1 Torr. They rely mostly on gas chemistry to achieve etching. The single-wafer versions of this approach can achieve very high etch rates (and thus, high wafer throughputs) at this pressure. However, the short mean free path of the gas molecules causes collisions in the dark space that detract from perfect anisotropy.

The largest installed base of etchers is of the plasma type. The early successes of Tegal and International Plasma Corporation (now Branson/IPC) were due to their single-wafer plasma systems. This technology reflects the tendency of semiconductor manufacturers to purchase single-wafer processing systems over batch systems when the process requirements can be met by either.

These systems were used primarily for polysilicon and nitride etching at geometries where the line loss due to some isotropy could be compensated for in the design. Since these early systems, the process technology has been refined so that there is much less line loss. One

method of reducing line loss is to adjust the pressure, gas mixture, and power so that a passive coating on the sidewall forms from the polymer created from resist by-products. This passive sidewall coating resists the ion flux and produces near anisotropic etching. Plasma reactors are now routinely used for oxide and aluminum etching. Lam Research Corporation and Varian's Zylin Division have had considerable success for single-wafer applications in oxide and aluminum, respectively.

Reactive Ion Etching

The term reactive ion etch (RIE) refers to the RF-driven-cathode approach. Such systems operate at lower pressures, usually 10 to 100 mTorr. They rely on the ion acceleration due to the large dark-space voltage to drive the chemistry. At these pressures, the etch rate is much lower than with the plasma method because there are only one-tenth to one-hundredth the gas densities. In addition, the electrode areas are such that the voltage drop at the cathode is much greater than in the planar method. Such systems are forced to operate in the batch mode to obtain adequate throughputs. However, the gas molecule mean free path at these pressures is much longer and results in much better anisotropy in general. The lower pressure also reduces the tendency for the chamber and chamber hardware to coat with organic polymers, which have plagued plasma reactors in the past.

Because the pressures are lower, more sophisticated pumping systems are needed, which increases the price over their planar counterparts. Although the systems are more expensive and operate in the batch mode, semiconductor manufacturers have purchased them for certain applications. They were first popularized for oxide etching. Anelva and Plasma Therm have had success in producing this type of system.

Hexode

The hexode is a special application of the RIE technology. The wafers are held vertically on a concentric, hexagonally shaped cathode within an outer bell jar. The symmetrical electrode configuration helps to achieve the uniformity within a batch of wafers that is needed for adequate yields. This approach allows maximum loading of wafers to obtain adequate throughputs with the characteristic low etch rates of the RIE approach. This is in contrast with planar electrode systems, which are constrained in wafer loading by the size of the electrode, which in turn causes reduced etch uniformity as the electrode becomes larger.

The hexode technology was invented at Bell Laboratories and subsequently licensed to Branson/IPC, LFE Corporation, Plasma Therm, and Technics. Although Applied Materials did not obtain a license, the creators of the hexode joined the company and refined the technology. Applied has been the most successful. Hexodes are used primarily for

oxide and aluminum etching. They are useful for more exotic processes such as aluminum with copper alloys, refractory metals and alloys, and single-crystal silicon. While there seems to be much process flexibility for process development, the wafer expense associated with the large wafer loading requires partial wafer loading during process experiments. This can impede development time and demonstrates one of the benefits of the single-wafer systems.

The early hexodes did not have a load lock. For aluminum etching, and etching in general, the subjection of the process chamber to atmospheric conditions after each run compromised the process. In addition, the hexode has been very difficult to automate with respect to loading wafers onto the cathode. LFE Corporation added a loadlock and automatic loading mechanism but had little success. Branson/IPC and Applied Materials introduced robotic handlers that loaded wafers onto the cathode, but these approaches did not receive acceptance from semiconductor manufacturers. In 1984, Applied Materials introduced a second-generation hexode with loadlock and automatic wafer handling. This product has received much better acceptance than the previous efforts.

Magnetron Etching

To obtain the anisotropy of the RIE method in a single-wafer system, the etch rates must be drastically increased to maintain the throughput. This can be done by increasing the ratio of ions to neutral gas molecules in the plasma. One approach is to magnetically enhance the plasma. The secondary electrons are confined to circular orbits by the magnetic field near the cathode, thus causing more ionizations. Such ionization ratios are two orders of magnitude greater than for normal plasmas. This greater ion flux provides the etch rates necessary for adequate throughputs in a single-wafer system.

Two vendors have introduced magnetically enhanced etchers: Materials Research Corporation (MRC) and Tokuda Seisakusho, Ltd. Both companies had early introductions of systems and followed up within three years with a new generation. MRC's approach is to use a quadrapole magnet above the chamber and a permanent magnet below the chamber, attempting to shape the field with these magnets to obtain maximum uniformity. Tokuda's approach is to sweep long bar magnets back and forth across the wafer from below and outside the chamber. The sweeping motion averages out the magnetic field for maximum uniformity. Tokuda also has a DI water rinse and dry station at the output of the exit loadlock.

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Triode

Another way to increase throughput in a single-wafer system is to increase the amount of power delivered to the electrodes. As the power is increased, the ionization ratio is also increased. However, the power density onto the wafer also increases. Such systems use sophisticated wafer cooling to protect the photoresist from becoming a hard epoxy under the increased flux. A particular application of this approach is the triode etcher, which has an upper, a lower, and an optional grounded middle electrode. Such a method provides a means of controlling the voltage on the cathode while pumping more power into the plasma.

These systems have achieved excellent process results with respect to selectivity, throughput, and anisotropy. There are three vendors with triode systems: Balzers, GCA Corporation, and Tegal. These systems are used for oxide, aluminum, refractory silicides, and silicon trench etching. They are used for polysilicon etching where the etch rate of the underlying oxide must be minimized.

All of the above approaches have their advantages and disadvantages with respect to uniformity, throughput, selectivity, anisotropy, price, and profile control. In addition, the engineering design can add or detract from the optimal use of the technologies. There is a perceived general desire in the industry to process one wafer at a time. However, it is not clear that the trade-offs will produce a better, cost-effective approach than the low-power, batch approach. The industry also desires the redundancy obtained by using several lower-priced, low-throughput systems instead of one high-priced, high-performance model. But it is not clear that a low-performance system can obtain the same quality etch that will be required on future VLSI devices.

We believe that future cost-effective approaches will be apparent in the ensuing high-growth market for dry etchers. For instance, in a typical 11-mask CMOS process, 4 mask steps require the high anisotropy of an RIE etcher, 5 steps could use plasma etchers, and 2 steps can be done by wet etching. Although the noncritical steps will decrease as devices become more complex, there will continue to be available niches for each of the technologies in the production of 256K DRAMs and beyond.

Ion Milling

Ion milling was pioneered as a production process for manufacturing bubble memories. Since then, it has become the dominant processing method for applications that contain chemically inert materials such as gold, chrome, and nickel-iron. These applications include bubble memory devices, maskmaking, and magnetic heads.

Dry Etch Processing

Unlike barrel and parallel-plate etching, ion milling uses physical ablation (sputtering) of the substrate as the etch mechanism. The gas plasma, which is usually inert, is produced remotely. The ions are extracted and accelerated toward the substrate by an electric field. This is done in a vacuum of about 0.1 mTorr. Since the gas is inert, the ions sputter each material roughly equally. Therefore, there is little selectivity over photoresist or the base material.

Since the pressure is low and the beam is collimated, ion milling can be used to etch lines well below 1 micrometer. In addition, the substrate can be oriented at an angle to the beam, which results in sloped wall profiles. Care must be taken to provide enough photoresist to survive the etch process (usually 1.5 times the etch depth). The photoresist is also subject to sideways erosion, which will transfer some slope into the wall profile.

The main disadvantages of the ion-milling process are the lack of selectivity and the low throughput. Since there is no chemical action, the etch rates are very low compared with wet or dry etching. The time to pump down the chamber to low vacuum also increased the process cycle time. For production processing of semiconductors, ion milling is not cost effective compared with other approaches.

To improve the etch rates, a reactive gas can be used instead of an inert one. This approach is called reactive ion-beam etching (RIBE). The chemical action provided by the gas (typically chlorine or fluorine with oxygen) helps to break surface bonds so that there is both a chemical and sputtering component to the etch rate. However, this action proceeds on all surface materials such that selectivity is not substantially improved. RIBE is still relegated to research and development efforts to improve these fundamental limitations.

We believe that ion milling will be used for very fine lines in inert materials. This could be a very fast growing, although small, niche. Gallium arsenide and GGG materials may fall into this market segment, and it remains to be seen whether applications can be served by the parallel-plate technology.

WET VERSUS DRY

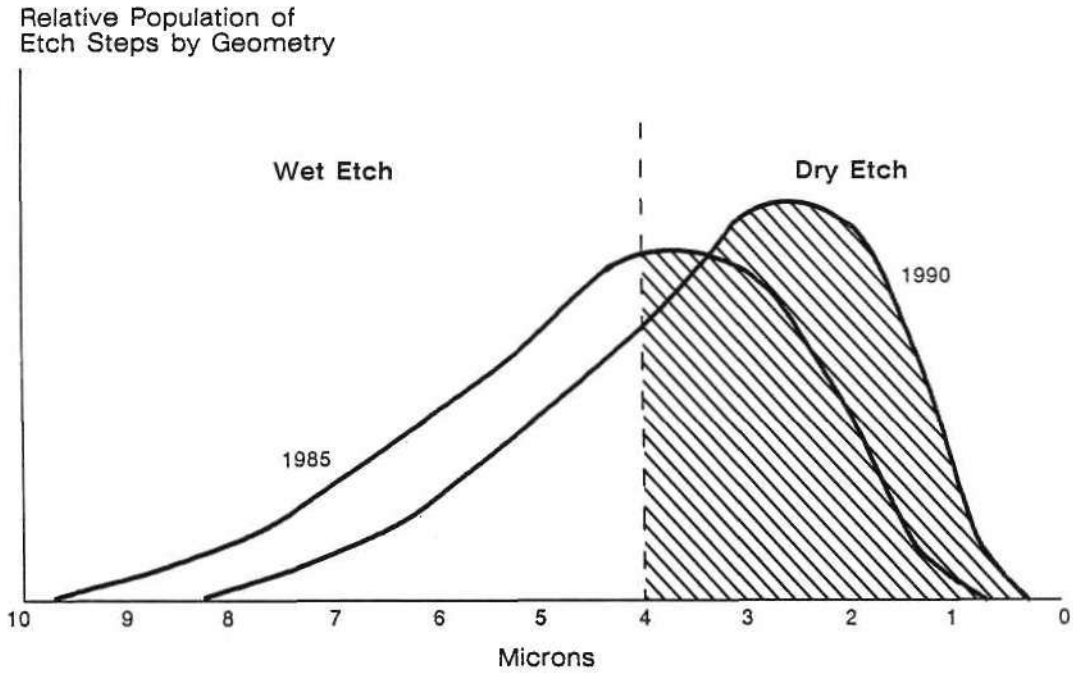
The movement away from wet etching in device fabrication has many impediments. It is still much more cost effective to perform wet chemistry on many of the devices manufactured today. The impact on yields for devices above 4 microns is not worth the considerable cost of implementing dry etching.

Dry Etch Processing

Figure 1 illustrates of the distribution of etch steps in the industry by line geometry for 1985 and 1990. Since it is more cost effective to wet etch geometries above 4 microns, the total number of layers done wet versus dry is still about 58 percent, which can be found by integrating the curve. However, in 1990, the percentage of layers that are wet etched will fall to about 25 percent.

Figure 1

ESTIMATED DISTRIBUTION OF PROCESS STEPS BY LINE GEOMETRY



Source: Dataquest
November 1986

Dry Etch Processing

For the newer devices being manufactured, the line geometries are much more critical. However, this still amounts to source and drain masks for MOS devices, emitters for bipolar devices, vias, and contact holes. Although the geometries are very small on these steps, device designers have resorted to double-layer interconnects and double-layer metallization to obviate the need for smaller geometries for those upper levels. This has retarded the application of dry etching for metals. It has even loosened the specifications on polysilicon so that less anisotropy is required, which allows the use of lower-performance dry etchers.

Since its inception, dry etch has grown significantly with respect to wet etch. As we show in Table 1, we believe that in the next five years there will continue to be growth of dry etch relative to wet etch. The viability of dry etch for interconnects and metal alloys was demonstrated in 1983. By 1985, dry etch had demonstrated its viability in virtually every etch process. The impact of yields for fine-line devices will more than justify the tenfold increase in cost per layer per device to implement dry etch.

Table 1

PERCENTAGE OF LAYERS BEING DRY ETCHED IN PRODUCTION

	1985	1990
Silicon Dioxide	25%	50%
Polysilicon	55%	80%
Silicon Nitride	65%	70%
Aluminum	20%	60%
Advanced Processes	80%	95%

Source: Dataquest
October 1986

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Dry Etch Processing

PROCESS APPLICATION

The market for dry etch breaks down as shown in Table 2. Although applications for silicon nitride and polysilicon have the lion's share of the levels etched, as we show in Table 1, the cost of the equipment is generally much lower. Since higher-priced equipment is needed to etch oxide, metals, and silicides, and since there will be more growth into those process steps, the highest dollar growth is expected for those applications.

Table 2

SYSTEM MARKET SHARE
BY PROCESS APPLICATION

	1985	1988
Silicon Dioxide	26%	26%
Polysilicon	14	9
Silicon Nitride	9	6
Aluminum	19	34
Advanced Processes	32	25
Total	100%	100%

Source: Dataquest
October 1986

TRENDS

Hexode

The hexode uses the RIE operation, which is positioned in the largest growth segment of the process applications--oxide, aluminum, and more advanced processes. The large wafer loading (24 four-inch wafers) provides good productivity, which is largely responsible for its success over planar batch-type systems. This success demonstrates the tendency for semiconductor manufacturers to select systems that maximize the wafers processed per dollar spent (which includes allocation of floor space).

The technology was taken to Applied Materials by its inventor, Dr. Dan Mayden, who further refined it. As mentioned before, it was also licensed by Bell Labs to Branson/IPC, LFE, Plasma-Therm, and Technics. Applied's lead has proven to be quite formidable. It became the leading producer of dry etchers in its first two years and now leads the parallel-plate market with about 23 percent market share. Although Branson/IPC, LFE, and Technics tried to improve on the original design, none have shown any appreciable success, and all have since stopped building hexodes. Plasma-Therm has delivered about 20 systems to captive semiconductor manufacturers on the East Coast.

Previous designs suffered from the lack of loadlocks and cassette-to-cassette operation. LFE implemented these on its system, but the design was not accepted by semiconductor manufacturers. Applied introduced a loadlocked, cassette-to-cassette system in 1984. This system was designed to reduce the particulate that is introduced during handling and to improve the problems associated with water vapor during aluminum etching. We believe that the vertical configuration, with its attendant high productivity, will continue to be popular for large-volume production of VLSI devices.

Single-Wafer versus Batch

There has been a lot of controversy concerning which is the most advantageous method of etching--batch or one wafer at a time. The most successful manufacturer of etchers has been Applied Materials, which sells a batch system. However, there have been several successful makers of single-wafer systems, both in the United States and Japan. Lam Research, in particular, has become second in worldwide market share, having introduced its system in 1982. In the last few years, the markets for single-wafer systems and batch systems have grown at the same rate. The market was split 50/50 in 1983 and, remarkably, it was still split 50/50 in 1985. Single-wafer systems have gained their market mostly in the etching of polysilicon and, to a lesser extent, silicon dioxide. The makers of each type are listed in Table 3.

One manufacturer, Drytek, has combined the single-wafer and batch methods by using a stack of single-wafer electrodes in a single chamber. Drytek has been very successful with this approach in polysilicon and oxide applications.

Dry Etch Processing

Table 3

MAKERS OF SINGLE-WAFER AND BATCH SYSTEMS

Single-Wafer Systems	Batch Systems
Balzers	Anelva
Branson/IPC	Applied Materials
CIT-Alcatel	Electrotech
Electrotech	Kokusai
GCA	Plasma-Therm
Lam Research	Tokuda
MRC	Ulvac
Perkin-Elmer	
Plasma Systems	
Plasma-Therm	
Ramco	
Tegal	
Tokyo Ohka	
Zylin	

Source: Dataquest
October 1986

It is evident from Table 3 that there are suitable applications for each approach. The dollar volumes of each category are equal. From Table 2, the highest growth areas are for silicon dioxide, aluminum, and advanced processes. These applications are generally believed to benefit from the RIE technology, which can best be done in the batch mode. However, there are techniques that can enhance the anisotropy of high-pressure systems and new advances that may allow RIE in a single-wafer mode, as mentioned earlier. In these new VLSI processes, end-point detection is very important in order not to etch into the underlayer. Some new applications can tolerate no more than 30 angstroms into the base layer. Such end-point detection favors the single-wafer system. This is because, in a single-wafer system, each wafer is monitored while in a batch system, either an average end point is derived by looking at the gas effluent or one wafer per batch is monitored.

We believe that both technologies will continue to grow for the next few years, each finding its most productive applications. The batch systems will develop very high throughputs, perhaps doubling single-wafer

systems' throughputs for smaller wafer sizes while maintaining process quality. Single-wafer systems will become highly automated with respect to end-point detection. Both will pay strict attention to particulate control, as contamination will become more important than shrinking line widths for device manufacturers. We believe that, as the technology matures, the single-wafer, RIE systems will begin to take market share away from batch systems.

Triode and Magnetically Enhanced Etching

The position that batch, RIE systems have held is due to being able to etch at low pressure with high throughputs. As described earlier, triode and magnetically enhanced etching allow low pressure in a single-wafer system with throughputs approaching those of hexode reactors. Once these incipient techniques are fully developed, they will compete directly with batch, RIE systems.

The triode, if it fulfills expectations, will occupy a position that competes both with plasma systems and RIE systems. However, the price of these systems is considerably higher than that of the plasma counterparts. For production, dedicated, low-cost systems will still provide higher productivity for less critical processes.

Magnetically enhanced etching has the advantage of etching at a much lower pressure than any of the techniques except ion-beam milling. As with the triode, there is no real differentiation with respect to plasma systems for less critical processes. In fact, plasma-type systems still maintain a throughput advantage over the low-pressure systems. Therefore, the importance will be where the low pressure becomes necessary--for the high-growth processes in very fine lines.

Trilevel Resist

The next few years will see device manufacturers concentrate on improving yields rather than reducing line geometries below 1 micron. One very important technique will be planarizing the severe topography with multilevel resist schemes. The ability to etch these levels will provide another market for dry etchers.

The trilevel resist process begins with the deposition of a thick film of polyimide or commercial photoresist on the base topography. Then a thin layer of Si_3N_4 or SiO_2 is deposited. In this case, the photoresist must be cured to withstand the deposition temperature of 200 degrees centigrade. An alternative to the high temperature would be

to spin on glass or use cold plasma deposition of SiO_2, which obviates the need for curing. Then a layer of working resist can be spun on the thin layer. After patterning and developing the working resist, the SiO_2 is dry etched. After etching, the SiO_2 can be used as a mask for etching the thick photoresist with an oxygen plasma. The polyimide then becomes an etch mask for the base layer.

The aspect ratio of these levels (ratio of etch depth to line width) can be as much as 4 to 1. The batch, RIE systems have a real advantage here. They do not necessarily etch organic polymer any better than high-pressure systems, but they are able to etch high aspect ratios much better. In addition, the layers can be 3 microns deep, which severely affects the throughputs of single-wafer systems.

MARKET DATA

History

We estimate that worldwide dry etch wafer processing equipment consumption was $406 million in 1985, a decrease of 2 percent from $414 million in 1984 (see Table 4). North American markets grew at a 27 percent CAGR from 1980 through 1985 but fell nearly 5 percent in 1985. It is interesting to note that while the worldwide market grew at a CAGR of 35 percent from 1980 ($90 million) through 1985 ($406 million), Japanese consumption grew at a 45 percent CAGR over the same period. The European CAGR of 44 percent reflects Europeans' growing awareness that they must accelerate spending to maintain a viable electronics community. The recent growth of the ROW markets reflects the concentrated efforts of large conglomerates in Korea and Taiwan to compete as semiconductor manufacturers. While ROW companies account for approximately 1 percent of semiconductor production, they consume nearly 5 percent of dry etch equipment.

For the worldwide market, Table 5 shows that the fastest-growing dry etch equipment is the parallel-plate type. This segment grew at 40 percent CAGR from 1980 through 1985. Barrel systems grew 8 percent from $30 million in 1980 to $45 million in 1985. Ion-milling equipment grew slightly after 1980 and fell in 1985 as it was affected by the severe semiconductor recession.

Dry Etch Processing

Table 4

ESTIMATED WORLDWIDE CONSUMPTION OF DRY ETCH EQUIPMENT
BY GEOGRAPHIC REGION
(Millions of Dollars)

	1980	1981	1982	1983	1984	1985
North America	$60	$ 77	$ 94	$123	$201	$194
Japan	25	40	69	103	174	162
Western Europe	5	8	12	21	27	31
Rest of World	0	0	0	2	12	19
Total	$90	$125	$175	$249	$414	$406
Growth		39%	40%	42%	66%	(2%)

Source: Dataquest
October 1986

Table 5

ESTIMATED WORLDWIDE CONSUMPTION OF DRY ETCH EQUIPMENT
BY TYPE
(Millions of Dollars)

	1980	1981	1982	1983	1984	1985
Barrels	$30	$ 29	$ 26	$ 29	$ 44	$ 45
Parallel-Plate	52	88	141	206	351	344
Ion-Milling	8	8	8	14	19	17
Total	$90	$125	$175	$249	$414	$406

Source: Dataquest
October 1986

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Dry Etch Processing

The dry etch market has grown since 1980 because of the performance of parallel-plate systems. In Table 6, we show that the North American stripping and ion-milling markets actually fell in sales, while the parallel-plate market grew at a 40 percent CAGR. This reflects the high productivity of the barrels and the low growth in applications for ion-milling systems. Parallel-plate applications are those that allow the production of line geometries below 2.5 microns, a region of prodigious growth.

Table 6

ESTIMATED NORTH AMERICAN CONSUMPTION OF DRY ETCH EQUIPMENT BY TYPE
(Millions of Dollars)

	1980	1981	1982	1983	1984	1985
Barrels	$20	$18	$14	$ 17	$ 19	$ 17
Parallel-Plate	32	52	74	99	173	170
Ion-Milling	8	7	6	7	9	7
Total	$60	$77	$94	$123	$201	$194
Growth		28%	22%	31%	63%	(3%)

Source: Dataquest
October 1986

In keeping with the aggressiveness of Japanese semiconductor manufacturers, Japanese consumption of parallel-plate equipment grew at 51 percent CAGR between 1980 and 1985 (see Table 7). Barrel systems grew at a 21 percent CAGR and ion-milling systems grew from very low levels to $6 million. These growth rates reflect both the lower installed base of Japanese manufacturers in 1980 and the commitment of those companies to gaining worldwide market share.

European distribution of dry etch equipment is shown in Table 8. Although the table shows a growth rate of 44 percent from 1980 through 1985, the market was too small for the growth to be meaningful. They are given as a comparison to the worldwide figures.

Table 7

ESTIMATED JAPANESE CONSUMPTION OF DRY ETCH EQUIPMENT
BY TYPE
(Millions of Dollars)

	1980	1981	1982	1983	1984	1985
Barrels	$ 8	$ 9	$ 9	$ 9	$ 19	$ 21
Parallel-Plate	17	30	58	89	149	135
Ion-Milling	0	1	2	5	6	6
Total	$25	$40	$69	$109	$174	$166
Growth		60%	72%	58%	69%	(7%)

Table 8

ESTIMATED EUROPEAN CONSUMPTION OF DRY ETCH EQUIPMENT
BY TYPE
(Millions of Dollars)

	1980	1981	1982	1983	1984	1985
Barrels	$2	$2	$ 3	$ 3	$ 5	$ 5
Parallel-Plate	3	6	9	16	19	23
Ion-Milling	0	0	0	2	3	3
Total	$5	$8	$12	$21	$27	$31
Growth		60%	50%	75%	29%	15%

Source: Dataquest
October 1986

The ROW market share estimates are listed in Table 9. This has been an important region in recent years. With the activity in Korea and Taiwan, some dry etch vendors have been able to survive the current recession by selling into the ROW region. With China's one billion people, there exists great potential for companies that have the distribution capabilities to market into the Pacific rim.

The market share estimates for strippers and parallel-plate systems are listed in Tables 10 and 11. As can be seen, the dominant suppliers in all three categories of dry etcher are concentrated in North America.

Dry Etch Processing

Table 9

ESTIMATED ROW CONSUMPTION OF DRY ETCH EQUIPMENT BY TYPE
(Millions of Dollars)

	1980	1981	1982	1983	1984	1985
Barrels	N/A	N/A	N/A	$0	$ 1	$ 2
Parallel-Plate	N/A	N/A	N/A	2	10	16
Ion-Milling	N/A	N/A	N/A	0	1	1
Total	N/A	N/A	N/A	$2	$12	$19
Growth		N/A	N/A	N/A	500%	58%

N/A = Not Available

Source: Dataquest
October 1986

Table 10

STRIPPER MARKET SHARE BY GEOGRAPHIC REGION
(Millions of Dollars)

Company	1984 Sales	1984 Share	1985 Sales	1985 Share
North America				
Branson/IPC	$ 7	37%	$ 9	53%
Tegal	6	32	4	24
Drytek	3	16	2	12
LFE	3	16	2	12
Total	$19	100%	$17	100%
Japan				
Plasma Systems	$ 8	42%	$11	52%
Tokyo Ohka	6	32	5	24
Branson/IPC	3	16	3	14
Yawata	2	10	2	10
Total	$19	100%	$21	100%
Europe				
Branson/IPC	$ 2	40%	$ 3	60%
Tegal	2	40	1	20
Electrotech	1	20	1	20
Total	$ 5	100%	$ 5	100%

Note: Columns may not add to totals due to rounding.

Source: Dataquest
October 1986

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Table 11

PARALLEL-PLATE MARKET SHARE BY GEOGRAPHIC REGION
(Millions of Dollars)

Company	1984 Sales	1984 Share	1985 Sales	1985 Share
North America				
Applied Materials	$ 45	26%	$ 44	26%
Tegal	30	17	25	15
Lam Research	23	13	25	15
Drytek	22	13	20	12
Plasma-Therm	12	7	20	12
Perkin-Elmer	12	7	15	9
Zylin	14	8	8	5
Electrotech	4	2	3	2
Anelva	3	2	4	2
Tokuda	3	2	3	2
Branson/IPC	4	2	2	1
Kokasai	1	1	1	1
Total	$173	100%	$170	100%
Japan				
Applied Materials	$ 26	17%	$ 26	19%
Anelva	32	21	32	24
Tokuda	18	12	20	15
Tokyo Ohka	23	15	18	13
Lam Research	11	7	11	8
Kokasai	14	9	8	6
Ulvac	10	7	8	6
Plasma Systems	6	4	5	4
Perkin-Elmer	3	2	3	2
Ramco	3	2	3	2
Electrotech	3	2	1	1
Total	$149	100%	$135	100%

Note: Columns may not add to totals due to rounding.

(Continued)

Table 11 (Continued)

PARALLEL-PLATE MARKET SHARE BY GEOGRAPHIC REGION
(Millions of Dollars)

Company	1984 Sales	1984 Share	1985 Sales	1985 Share
Europe				
Applied Materials	$ 4	21%	$ 5	22%
Electrotech	4	21	5	22
Plasma-Therm	2	11	4	17
Tegal	4	21	3	13
Lam Research	2	11	3	13
Branson	2	11	1	4
Drytek	1	5	1	4
Total	$ 19	100%	$ 23	100%
Rest of World				
Lam Research	$ 3	30%	$ 6	38%
Perkin-Elmer	3	30	3	19
Applied Materials	1	10	3	19
Drytek	1	10	2	13
Anelva	1	10	1	6
Plasma-Therm	0	0	1	6
Zylin	1	10	0	0
Total	$ 10	100%	$ 16	100%
Worldwide				
Applied Materials	$ 76	22%	$ 78	23%
Lam Research	39	11	45	13
Anelva	36	10	37	11
Tegal	34	10	28	8
Drytek	24	7	23	7
Tokuda	21	6	23	7
Plasma-Therm	14	4	25	7
Perkin-Elmer	18	5	21	6
Tokyo Ohka	23	7	18	5

Note: Columns may not add to totals due to rounding.

(Continued)

Table 11 (Continued)

PARALLEL-PLATE MARKET SHARE BY GEOGRAPHIC REGION
(Millions of Dollars)

Company	1984 Sales	1984 Share	1985 Sales	1985 Share
Worldwide (Continued)				
Kokasai	15	4	10	3
Electrotech	11	3	9	3
Zylin	15	4	8	2
Ulvac	10	3	8	2
Plasma Systems	6	2	5	1
Branson/IPC	6	2	3	1
Ramco	3	1	3	1
Total	$351	100%	$344	100%

Note: Columns may not add to totals due to rounding.

Source: Dataquest
October 1986

Most of these companies make a significant percentage of their sales in Japan. Almost all of the Japanese vendors' sales are made in Japan and Asia. Although most of the listed Japanese suppliers have North American operations or U.S. trading partners, none have shown appreciable sales in North America or Europe.

Forecast

We believe that capital spending in general, and for dry etch in particular, will settle down to lower growth rates for the rest of the decade. Dry etch revenue should fall 5 percent to $387 million in 1986 as the semiconductor industry adjusts to the excess capacity that currently exists (see Table 12). However, this estimate includes a dollar depreciation of 30 percent against the Japanese yen. If we adjust for the depreciation, the decrease in 1986 becomes 15 percent. The market for dry etch equipment should rise 9 percent in 1987 to $422 million. However, in 1987, we expect an additional dollar depreciation against the yen of 7 percent. If we adjust for the depreciation, the 1987 rise becomes 6 percent. Worldwide consumption should reach $649 million in 1990, representing a 10 percent CAGR from 1985 through 1990.

Dry Etch Processing

Table 12

FORECAST WORLDWIDE SALES OF DRY ETCH EQUIPMENT
BY TYPE
(Millions of Dollars)

	1986	1987	1990	CAGR 1986-1990
Stripping	$ 42	$ 45	$ 91	15%
Parallel-Plate	330	361	535	9%
Ion-Milling	15	16	23	7%
Total	$387	$422	$649	10%

Source: Dataquest
October 1986

Stripping should grow at a 15 percent CAGR to $91 million in 1990. This growth reflects the emerging market for single-wafer strippers. Ion-milling systems will grow at a 7 percent CAGR to $23 million in 1990.

Dry Etch Processing

Appendix A

DRY ETCH PRODUCTS

Company	Model/Series	Price Range	Comments
Barrels			
Branson/IPC	L2100	$30,000 to $40,000	
	L3100	$40,000	
Electrotech	PE508	N/A	
Psi Star	8200	$90,000	With pump; remote plasma
Tokyo Ohka	OPM-A Series	$100,000	Cassette to cassette
Plasma Systems	AEN, AH, AV	N/A	Several configurations
Single-Wafer Strippers, Remote Plasma			
Machine Technology	AfterGlo DPR	$110,000	
Matrix	N/A	$87,500	
Gasonics	Aura	$78,000	
Alcan Tech	MAS 800	$100,000	
Emergent Technologies	Phoenix NORD	$110,000	Pump included
Branson/IPC	L3200	$130,000	Without pump

(Continued)

Appendix A (Continued)

DRY ETCH PRODUCTS

Company	Model/Series	Price Range	Comments
Single-Wafer Strippers, Contact Plasma			
Plasma-Therm	Wafer/Strip	$95,000	Without pump
Tegal	Model 900e	$110,000	With pump
Plasma Systems (Semix)	PE 615	$125,000	With pump
Single-Wafer Plasma Systems			
Lam Research	600 Series	$250,000 to $365,000	
Varian/Zylin	Zylin 10 Zylin 100	$400,000 $500,000	Aluminum Aluminum, oxide, and poly
Drytek	Quad System	$395,000	4 chambers
Tegal	900 Series	$110,000 to $220,000	
Tokyo Ohka	OAPM-300	$100,000	
	OAPM-400	$200,000	Loadlocked
	OAPM-500	N/A	Loadlocked, 2 chambers
Plasma Systems	DES-A303	$180,000	Loadlocked
	PE-615	$116,000	
Ramco	RAM-400SE	$290,000	All processes except Al

(Continued)

Appendix A (Continued)

DRY ETCH PRODUCTS

Company	Model/Series	Price Range	Comments
Single-Wafer Plasma Systems (Continued)			
Plasma-Therm	X-160	N/A	Oxide
	P-360	N/A	Poly
	In-line	N/A	Aluminum
Perkin-Elmer	20000	$395,000	2 chambers
Electrotech	M4	N/A	RIE, triode options, multi chambers
Single-Wafer RIE Systems			
Tokuda	Hirrie 100	$500,000	Magnetron
Materials Research	Aries	$395,000	Magnetron
Balzers	SWE 654	$250,000	
GCA	WaferEtch 606	$400,000	Triode
Tegal	Model 1500e	$310,000 to $390,000	Triode
Anelva	4013	$450,000	4 chambers
Batch Systems			
Applied Materials	8100	$300,000 to $400,000	Hexode, no load-lock
	8300	$675,000	Hexode, cassette to cassette, loadlock

(Continued)

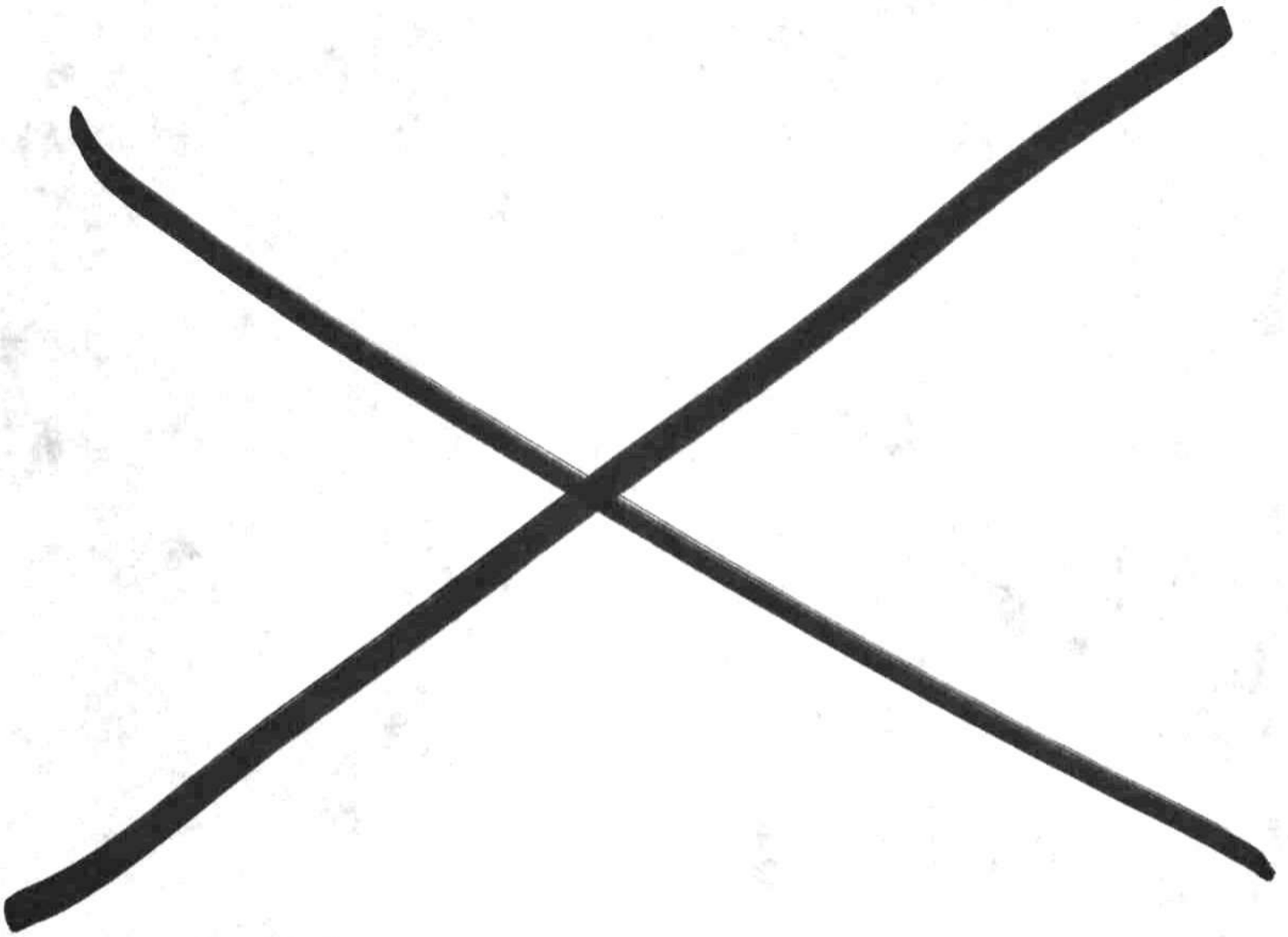
Appendix A (Continued)

DRY ETCH PRODUCTS

Company	Model/Series	Price Range	Comments
Batch Systems (Continued)			
Anelva	4000	N/A	
Plasma-Therm	Batch	N/A	24 wafers
Tokuda	555	$400,000	12 wafers
Electrotech	5200 Series	N/A	
Kokasai (Veeco)	DV-40	N/A	

N/A = Not Available

Source: Dataquest
October 1986



Deposition

The following is a list of the material in this section:

- CVD Technology
- CVD Companies

For additional information, please refer to the material behind the Deposition tab in your 1989 Newsletter binder.

CVD Technology

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CVD Technology

INTRODUCTION

Chemical vapor deposition (CVD) processing is one of the cornerstones of submicron fabrication technology. It is widely used through all aspects of semiconductor manufacturing ranging from traditional polysilicon and thermal nitride films to complex interlayer dielectrics, conductors, and passivation films. CVD has become one of the enabling technologies for ultralarge-scale integration (ULSI) products. Present lithography, dry etch, diffusion, and ion implantation equipment has developed to the extent where it will be able to support implementation of 0.5-micron processes in the early 1990s. However, the lack of optimized CVD equipment and multilevel interconnect processes creates the biggest bottleneck in submicron manufacturing; hence, substantial efforts are being directed toward the development of new CVD equipment and processes. Opportunities exist for equipment companies to develop new CVD solutions and capture a slice of the technology-intensive CVD market.

Multilevel interconnect technology drives the development of new CVD equipment and processes. As processes head toward the submicron regime, chip performance is controlled by multilevel interconnect technology limitations rather than active device technology. Dataquest believes that more than 50 percent of submicron process costs will be due to multilevel chip interconnection. Submicron application-specific integrated circuits (ASICs) with three and four levels of metal place an even greater emphasis on the development of production-worthy interconnect processes. Dynamic random-access memories (DRAMs), which primarily employed single-metal technology through the 1Mb generation, are expected to shift to double-metal technology for the 4Mb and 16Mb generations.

As processes move into the submicron regime, semiconductor manufacturers are adopting a systems approach to thin-film processing. Process and equipment development are becoming inextricably linked. In the past, equipment vendors focused on hardware development and semiconductor manufacturers developed the processes and debugged the equipment prior to production ramp-up, but times have changed. Spiraling costs of equipment and new processes, together with the need for rapid production ramp and minimum time to market, has led to new demands on the equipment industry. Today, semiconductor companies expect a complete systems solution from the equipment vendor that includes timely, economical implementation of equipment hardware and the process in production.

This section discusses current CVD equipment and technology trends in detail. The accompanying section profiles CVD equipment companies and their products. This service section is organized into the following major topics:

- CVD film and process requirements
- CVD equipment requirements
- Atmospheric pressure CVD (APCVD)
- Low-pressure CVD (LPCVD)

- Plasma-enhanced CVD (PECVD)
- Electron cyclotron resonance plasma CVD (ECR CVD)
- Integrated processing technology

A discussion of the current equipment, technology trends, and applications will be presented for each of these categories.

CVD FILM AND PROCESS REQUIREMENTS

Before plunging into a discussion of the main CVD equipment categories, it might be helpful to review the general film and process requirements for submicron CVD technology.

CVD films have four main applications: passivation, interlayer dielectrics, gate material, and interconnect metallization. Historically, the semiconductor industry has used CVD techniques for the first three applications and physical vapor deposition (PVD) techniques such as sputtering and evaporation for metallization. However, as PVD technology limits are reached, CVD techniques are being used for submicron ULSI interconnects as well. Although each application has its own specific requirements, the following general film and process attributes are needed:

- Film thickness uniformity—Film thickness has to be uniform across a wafer, from wafer to wafer and from lot to lot. Today's uniformity ranges from 1 to 2 percent, and Dataquest anticipates that films with uniformities of better than 1 percent will be required for submicron processing.
- Step coverage—Device topology and contact holes ideally should have 100 percent step coverage. This means that the film thickness on the vertical walls should be the same as on the horizontal surfaces.
- Pinholes—Pinholes must be minimized, as they can cause shorts and reliability hazards.
- Particles—Particles caused by the deposition process or equipment should be minimized and stringently controlled.
- Film stress—CVD films should have low compressive or tensile stress after deposition or annealing. The deposition process must be engineered to give the best stress characteristics.
- Planarization—In some cases, it may be desirable to achieve a planarized CVD film to enable better step coverage for subsequent film deposition.
- Adhesion—The film should adhere well to the substrate to prevent film lift-off.

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- Stoichiometry—Films should be stoichiometric. For instance, silicon nitride films deposited by PECVD contain relatively large amounts of hydrogen in addition to silicon and nitrogen. Hydrogen in nitride films is undesirable because subsequent processing steps can cause the hydrogen to evolve from the film, creating pinholes.

- Radiation damage—In the case of PECVD film deposition, the substrate is subjected to energetic ion and photon bombardment. Under certain conditions, this radiation can harm the device characteristics.

CVD EQUIPMENT REQUIREMENTS

Table 1 lists the film applications for various CVD equipment categories. It is unlikely that any one CVD technology will satisfy all semiconductor process needs; rather, different CVD technologies each will have applications for which they are best suited. Regardless of the technology used to deposit the CVD film, the equipment must have the following characteristics:

- Fully automated, cassette-to-cassette operation with self-monitoring and closed-loop controls
- Modular, flexible design with standardized components to enable varying applications
- Ability to interface with a factory automation system at the hardware and software level
- High throughput
- Low particulate generation that can be monitored and guaranteed by the equipment vendor
- High equipment reliability and guaranteed uptimes of 95 percent or more
- Limited scheduled downtime for preventive maintenance
- Small clean room footprint equipment design with through-the-wall installation
- Low power and utilities consumption
- Minimum load on the clean room air circulation system
- Efficient use of process gases
- Foolproof safety interlocks to enable safe operation

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CVD Technology

Table 1

Film Applications for Various CVD Equipment Categories

Application	Nontube APCVD	Tube HLPCVD	Tube VLPCVD	Nontube LPCVD	Tube HPECVD	Nontube PECVD	ECR CVD
Thermal Nitride		X	X				
Polysilicon		X	X				
Plasma Nitride					X	X	X
Undoped Oxide	X	X	X	X	X	X	X
Doped Oxide (PSG, BPSG)	X	X	X	X		X	
Tungsten Silicide				X			
Tungsten				X			
Aluminum				X			

Source: Dataquest
September 1989

ATMOSPHERIC PRESSURE CVD (APCVD)

APCVD films have been used since the early days of the semiconductor industry; historically, it is the oldest CVD technique still in use today. Recently, higher-quality LPCVD and PECVD films are beginning to displace APCVD films. Borophosphosilicate glass (BPSG) films remain as one of the last major APCVD applications.

Equipment Configuration

APCVD equipment consists of two general types. They are the continuous-belt, open reactor design such as Applied Materials' AMS 2100 and Watkins-Johnson's WJ-985 systems; and the closed-reactor batch design system such as Tempress' Pyrox and Hitachi's CVD 515A systems.

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Applications

1Mb DRAM manufacturers commonly use continuous-belt APCVD equipment to deposit BPSG as a smoothing reflow glass before metallization. APCVD BPSG films also are used as a reflow dielectric before first-level metal in double-metal ASIC and CMOS logic processes with minimum design rules of more than 1.2 microns.

APCVD equipment vendors are trying to extend their process ranges into submicron applications by offering incremental hardware and automation enhancements together with new process innovations. For example, efforts by vendors such as Watkins-Johnson are being conducted to develop thick, planarized intermetal oxides using organic, liquid source tetraethylorthosilicate (TEOS) materials.

In summary, APCVD reactors have the advantages of simplicity, low cost and high throughput. Disadvantages include relatively poorer step coverage and uniformity, higher temperature, and higher particle generation compared with LPCVD and PECVD films. For submicron processes, Dataquest expects APCVD applications to dwindle as higher-quality LPCVD and PECVD reactors emerge with the advantages of lower defects, lower temperatures, and better step coverage.

LOW-PRESSURE CHEMICAL VAPOR DEPOSITION (LPCVD)

For processes with design rules in the range of 1.2 to 2.0 microns, LPCVD has been the workhorse technology for polysilicon, thermal silicon nitride, interlayer dielectric oxides, tungsten, and silicide applications. LPCVD technology offers the advantages of higher-quality, higher-uniformity CVD films when compared with APCVD.

Equipment Configurations

LPCVD equipment can be divided into three broad design categories: horizontal tube reactors (HLPCVD), vertical tube reactors (VLPCVD), and nontube LPCVD reactors. Historically, HLPCVD reactor technology is the oldest of the three categories. It was developed in the mid-1970s to deposit polysilicon (poly) onto large batches of wafers. Such LPCVD tubes were designed to fit inside the bore of horizontal diffusion tube furnaces, which were in widespread use in the semiconductor industry at the time.

In contrast, vertical LPCVD tubes emerged recently as an evolution of vertical diffusion furnaces. In general, vertical LPCVD tubes have the advantages of better uniformity, smaller clean room footprint, and easier automation compared with horizontal tubes. For submicron processes, nontube LPCVD and PECVD reactors have the advantages of better uniformity, lower defects, and improved process control when compared with tube CVD equipment.

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CVD Technology

Horizontal LPCVD Tube Reactors

Developments in tube LPCVD processes are intimately related to developments in diffusion furnaces. Technology for horizontal LPCVD tube equipment has remained stable. Incremental advances have been made in the areas of wafer-handling automation, closed-loop pressure control, digital temperature control, and gas dispersion manifolds within the tube. The main advantage of the horizontal tube reactor is its ability to deposit uniform and conformal films economically onto large batches of wafers, typically 100 to 150 wafers per load.

Particle generation and uniformity for 6-inch and 8-inch processing are major problems for horizontal LPCVD tube applications. To compensate for reactant gas depletion and deposition nonuniformities toward the rear of the tube, the temperature profile is increased down the length of the tube. Because the horizontal LPCVD tube process is a "hot-wall" process, deposition occurs on heated surfaces other than the wafer, such as the walls of quartz tubes and the quartz wafer boat. Frequent cleaning of the quartz tube and boats is needed to minimize film flaking and wafer contamination inside the reactor. Particle generation is the single biggest problem with horizontal LPCVD tube reactors; thus, submicron processes are migrating away from horizontal LPCVD tube reactors toward nontube CVD reactors, which are easier to clean.

Vertical LPCVD Tube Reactors

Vertical LPCVD tube technology has evolved from vertical diffusion furnace technology. Advantages of vertical LPCVD tubes include the ability to handle large loads of 150mm and 200mm wafers, through-the-wall installation with zero clean room footprint, easier automation, better process uniformity, and lower defect generation. In contrast, conventional horizontal tube furnaces using cantilever loading cannot easily support larger size wafers and loads because of the added weight.

Nontube LPCVD Reactors

LPCVD tube technology has followed an evolutionary advancement path. In contrast, nontube (dedicated) LPCVD reactors have taken a revolutionary approach to fulfilling the needs of submicron manufacturing. Nontube LPCVD reactors are designed in two basic configurations—batch systems and single-wafer systems. The primary applications for nontube LPCVD reactors are doped and undoped oxide dielectrics and metal or silicide conductors. Single-wafer nontube LPCVD systems are gaining more applications compared with earlier batch nontube LPCVD systems due to their advantages of uniformity, flexibility, and compatibility with multichamber integrated processing systems. With the move to 8-inch wafers, advantages of single-wafer nontube LPCVD processing are more pronounced. Nontube LPCVD is used to deposit silicon nitride, silane-based silicon oxide, TEOS-based silicon oxide, polysilicon, tungsten, tungsten silicide, and other refractory metals.

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Silicon Nitride. LPCVD silicon nitride (also known as thermal nitride) is used primarily as an oxidation mask when growing the field oxide to separate the active device areas. LPCVD nitride is deposited at a high temperature (700°to 800°C) to provide a dense film as required for the field oxidation step. PECVD nitride is deposited at a lower temperature (less than 400°C), and because it is not as dense, it cannot be used for this application.

Silane–Based Oxide and TEOS–Based Oxide. LPCVD oxides are deposited at moderate temperatures of approximately 400°C. Because of the relatively low deposition temperature, LPCVD oxides are used over aluminum as an interlayer and passivation dielectric in multilevel interconnect processes.

Two major applications for undoped LPCVD oxides are spacer elements in lightly doped drain (LDD) CMOS devices and interlayer dielectrics in planarization applications. Doped LPCVD glasses such as PSG and BPSG are used as reflow glasses before first–level metal.

For submicron processes, liquid TEOS sources are preferred over gaseous silane sources. TEOS–based oxides can be deposited conformally at lower temperatures. This is desirable for submicron processes with tight thermal budgets. Moreover, liquid TEOS sources are less inflammable and less toxic compared with gaseous silane sources.

Polysilicon. LPCVD has been the predominant technique for the deposition of polysilicon as a gate material. The polysilicon film can be deposited undoped or doped in situ. For submicron applications, semiconductor manufacturers are examining the feasibility of in situ polysilicon deposition after gate oxide growth in an automated, vertical diffusion tube stack. The advantages of such an approach include better uniformity in vertical furnaces, lower gate oxide contamination due to vacuum transfer, and simplified processing.

Silicides, Tungsten, and Other CVD Conductors. CVD tungsten, tungsten silicide, and other refractory metals can be used as gate, contact barrier, plug, and interconnect materials in submicron processing. CVD techniques for these applications have the advantages of improved step coverage, self–aligned processes, and reliable, high–quality films.

- Silicides—Tungsten silicide is commonly used in combination with polysilicon as a polycide gate material. The polycide gate retains the advantages of the well–understood oxide–polysilicon interface while offering speed enhancements through lower gate resistance. Tungsten silicide films deposited in LPCVD reactors have been found to be very pure and dense with excellent step coverage. Genus is the pioneer in the development of dedicated batch LPCVD reactors for depositing tungsten silicide. Recently, many single–wafer dedicated LPCVD reactors for depositing tungsten silicide have emerged. Single–wafer reactor vendors claim advantages of better uniformity and process flexibility compared with batch LPCVD reactors.

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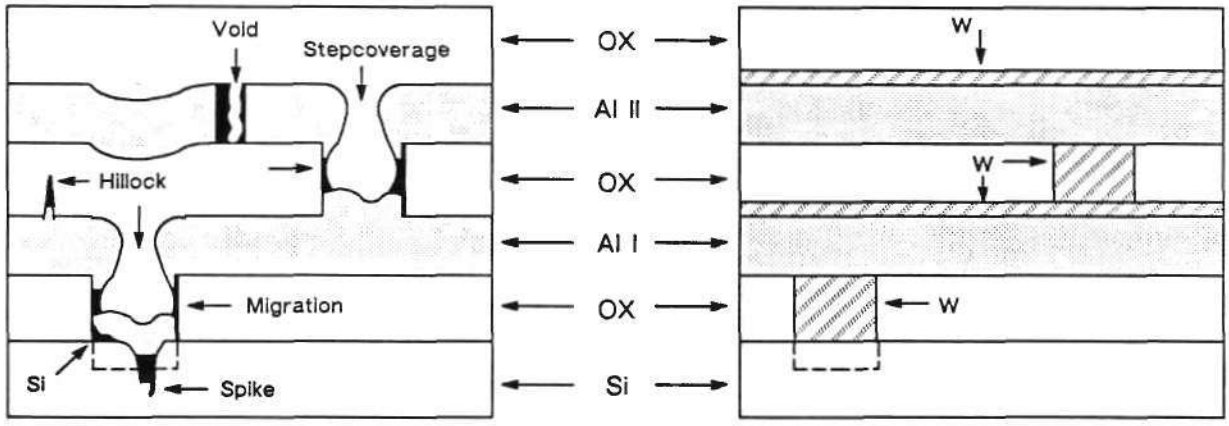
Titanium silicide is emerging as an alternative to tungsten silicide for gate and source–drain application. Titanium silicide can be formed as a self–aligned source, drain, and gate film (also known as a salicide) to reduce the resistances associated with submicron transistor operation. The salicide is formed by sputtering titanium onto the wafer after polysilicon gate etch. Subsequently, the wafer is annealed at 600°C in a rapid thermal processing environment to form the salicide on the source, drain, and gate areas. The unreacted titanium on the field areas is etched off in a selective wet–etch solution that does not attack the silicide. A final high–temperature rapid thermal anneal in the 850 to 900°C range yields a stable salicide film. Titanium salicide formed by this technique has a sheet resistance of less than one ohm per square, which is better than CVD tungsten silicide's sheet resistance of 2 to 5 ohms per square.

- Tungsten—CVD tungsten is being considered for use as a contact barrier, plug, and first–level interconnect material in advanced products such as 4Mb and 16Mb DRAM, and high–density ASICs. CVD tungsten has the benefits of excellent step coverage, immunity to electromigration failure, and higher current–carrying capability. Figure 1 illustrates the advantages of CVD tungsten as a barrier, plug, and interconnect material compared with conventional sputtered aluminum.

Figure 1

Advantage of CVD Tungsten over Sputtered Aluminum Interconnect Schemes



Problem of multilevel interconnection in half-micron devices (left) and uses of CVD (right)

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Source: Fujitsu Limited
Process Engineering Department

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CVD Technology

The disadvantages of CVD tungsten as an interconnect material include higher sheet resistance compared with aluminum, poor adhesion to oxide, high contact resistance, susceptibility to oxidation, and more complex processing. Steady progress is being made in solving these tungsten interconnect problems. Dataquest anticipates that CVD tungsten will be widely considered for contact barrier, plug, and first-level interconnect applications in submicron processes. For high-current density applications, CVD tungsten's advantages of superior step coverage and reliability outweigh the disadvantages of higher sheet resistance and more complex processing.

Tungsten can be deposited either as a blanket film or as a selective film. Blanket tungsten is being explored for current applications such as contact barriers, plugs, and first-level metal. The blanket tungsten film is deposited in batch or single-wafer dedicated LPCVD reactors. The chemistry involves hydrogen or silane reduction of tungsten hexafluoride. A glue layer of CVD tungsten silicide commonly is used to ensure good adhesion of the blanket tungsten film to the field oxide areas. Blanket tungsten can be easily dry etched using conventional reactive ion-etch techniques.

Selective tungsten is a potentially simple, self-aligned process to deposit tungsten on exposed silicon, polysilicon, and metal areas in multilevel interconnect integrated circuits. Selective tungsten does not deposit on field oxide areas and offers the advantages of good selectivity, uniformity, purity, step coverage, and density. Numerous problems such as excessive silicon consumption, junction leakage, encroachment, wormholes, and loss of selectivity remain to be solved before selective tungsten CVD can be implemented in production.

LPCVD selective tungsten is deposited in hot-wall dedicated batch reactors such as SVG/Anicon's system or in cold-wall dedicated batch reactors such as Genus' 8730 system. Currently, several cold-wall single-wafer reactors are being offered by companies such as BTU-Ulvac, Nanosil, Spectrum, and Varian.

Selective-tungsten CVD normally is deposited by a two-step reaction. First, a thin nucleation layer of selective tungsten is deposited on exposed silicon areas by silicon reduction of the source tungsten hexafluoride gas. This film has a self-limiting thickness of approximately 100 to 200 angstroms. Next, a hydrogen reduction reaction of tungsten hexafluoride is used to build up the selective tungsten film to the desired thickness. The main problems associated with the two-step selective CVD process include selectivity loss, lateral encroachment at the contact edge, tunnels from the junction into the substrate, and uneven nucleation due to residual oxide and surface contamination.

A new selective CVD tungsten process using silane reduction instead of hydrogen reduction recently has been proposed. The silane reduction process solves the problems of encroachment and silicon consumption that plagued the earlier hydrogen reduction reaction. But the remaining major problems of selectivity loss, tunnels, and uneven nucleation due to contamination still need to be resolved. The silane process shows promise as a viable production scheme for selective tungsten.

Selective tungsten also can be used as a cladding layer over aluminum interconnect lines. The cladding layer provides aluminum hillock suppression, electromigration resistance, and a selective nucleation site for subsequent tungsten via fills. The advantages of tungsten cladding on aluminum interconnects include increased reliability, self-alignment, and via etch stop barrier capability.

Aluminum CVD—Considerable efforts are being devoted toward the development of LPCVD aluminum processes. High-purity, conformal aluminum CVD films can be obtained with excellent step coverage and adhesion. Organic metal liquid CVD sources such as triisobutylaluminum (TIBA) are used. CVD aluminum problems such as roughness, nonspecularity, junction spiking, and TIBA source toxicity have to be solved before implementation in production. LPCVD techniques to deposit aluminum alloys incorporating copper and silicon still need development.

PLASMA-ENHANCED CHEMICAL VAPOR DEPOSITION (PECVD)

PECVD is a more recent deposition technique, which is displacing LPCVD for interlayer dielectric and passivation oxide/nitride applications. In PECVD reactors, radio frequency (RF) power is used to supply the energy to create a plasma and dissociate the reactant gases into highly reactive ions and radicals. These reactive species react at the wafer surface to deposit the film chemically. The main advantage of PECVD technology is its capability to deposit conformal, high-quality films at a low temperature of approximately 300°C. In particular, it was the low-temperature deposition of plasma nitride passivation films that caused PECVD to gain wide acceptance.

Equipment Configurations

Traditional PECVD systems either were batch reactors or horizontal tube reactors. These systems were used for plasma nitride and plasma oxide deposition for passivation and interlayer dielectric applications. Horizontal-tube PECVD systems are widely used to deposit oxide and nitride films. In turn, these films are widely used as interlayer and passivation dielectrics in processes with minimum design rules in the 1.0- to 1.6-micron range. Horizontal-tube PECVD systems have the advantages of high throughput, low cost, and compatibility with traditional tube processes. However, for submicron processing, horizontal-tube PECVD disadvantages include high particle counts resulting in frequent cleaning and lower uniformities for 150 and 200mm wafer processing.

Recently, several multichamber-process PECVD systems have emerged as potential solutions to the thorny interlayer dielectric problem in multilevel interconnect processes. Multichamber PECVD systems offer the advantages of flexibility, multilayer films, and in situ etchback planarization.

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CVD Technology

PECVD technology has moved from the traditional batch process technology to single-wafer process technology. In single-wafer process technology, the reactor can be either a true single-wafer reactor such as Applied Materials' PE 5000 system or a "semibatch" reactor with multiple localized plasma reaction zones such as Novellus' Concept One system. In both of these configurations, each wafer process station has its own gas shower head, plasma power supply, heating, and control unit. By confining the plasma to the region around the wafer, good film uniformity, plasma ionization efficiency, high deposition rates, and low particulate defects can be achieved. Many of these recent PECVD systems also incorporate an in situ plasma cleaning cycle between deposition cycles, thus enabling the reaction chamber to remain in a clean, particle-free condition at all times.

For interlayer dielectric planarization, multichamber PECVD systems can perform multiple sequences of deposition and etchback in situ without exposing the wafer to atmosphere. In such cases, one of the reactor chambers is configured to perform reactive ion etch or sputter etch to planarize the device topology steps. In planarization etchback applications, a minimum of three to four process chambers are needed to ensure viable throughputs. But such in situ planarization processes have the advantages of simplicity and low defects.

Applications

Dataquest estimates that silicon nitride accounts for 50 percent of the films deposited by PECVD, silane-based and TEOS-based silicon oxide accounts for 40 percent, and other applications such as amorphous silicon, polysilicon, silicides, and refractory metals together account for the remaining 10 percent.

Silicon Nitride

Because PECVD silicon nitride can be deposited at temperatures of less than 400°C with good moisture resistance, integrity, scratch resistance, and mobile ion-gettering ability, it is used widely as a passivation layer. PECVD nitride also is used in combination with PECVD or LPCVD oxide as an interlayer dielectric.

PECVD silicon nitride films deposited in traditional batch or horizontal tube reactors had a fairly high percentage of hydrogen trapped in the film. Although this was not of much consequence in passivation applications, it caused concern in the use of the film for other interlayer dielectric applications. Increased amounts of hydrogen in the film lower the film density and may also affect MOS device stability during subsequent high-temperature processing. Decreasing the deposition temperature increases the hydrogen content; therefore, most traditional tube PECVD and batch PECVD reactors are operated at 350 to 400°C although they can deposit nitride films at much lower temperatures.

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In contrast, modern single-wafer process PECVD systems have the capability of lowering the hydrogen level by manipulating the power and RF frequency independently. Many reactors have dual RF frequency operation in the KHz and MHz range to provide an additional degree of freedom in the process. PECVD systems that can manipulate a multitude of variable such as power, bias, RF frequency, gas chemistry, pressure, and upper/lower electrode power split provide flexibility in tailoring film properties. The ability to engineer film properties has led to the development of new passivation applications such as ultraviolet-transparent nitride for erasable programmable read-only memories (EPROMs), and low-stress nitride for plastic packaging.

Doped and Undoped PECVD Silicon Oxide

PECVD oxide is widely used as an interlayer dielectric between metal levels in multilevel interconnect processes. It has the advantages of low temperature, good conformality, and low defects for submicron applications. Other applications for PECVD oxides include LDD spacer oxides, BPSG reflow before first-level metal, planarization etchback layer, and stress-relief passivation oxide below nitride.

TEOS-based PECVD oxides have many advantages over traditional silane-based PECVD oxides, such as better conformality for submicron DRAM trench refill and interlayer dielectric planarization, higher-quality films, lower temperature, better safety, and simpler gas-delivery systems. TEOS oxides can be deposited as undoped films or doped films such as PSG and BPSG. BPSG TEOS films can be used as smoothing dielectrics before first-level metal because they can be reflowed at low temperatures of 850 to 900°C. Also, very thick as-deposited BPSG TEOS films can be used to fill and planarize steep topology between metal levels in submicron multilevel interconnect processes.

PECVD oxides often are used in combination with spin-on glasses to achieve a planarized interlayer dielectric between metal levels. In this application, PECVD oxides offer a conformal, low-temperature film over which spin-on glass can be easily coated and etched back for planarization.

ELECTRON CYCLOTRON RESONANCE (ECR) PLASMA CVD

As device geometries get smaller and dielectrics become thinner, semiconductor manufacturing equipment has to minimize process temperatures and energetic ion radiation damage on wafers. ECR technology is emerging as a promising method for depositing high-quality, low-temperature CVD films with minimal ion-radiation damage. Microwave power (2.45 GHz frequency) provides the plasma ionization energy in ECR CVD systems. Magnetic fields are superimposed on the plasma region to achieve circular electron motion for greater ionization energies. A magnetic field of 875 gausses is used to achieve resonance and high-plasma ionization efficiency with the 2.45 GHz microwave source.

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Table 2 contrasts the typical operating parameters for plasma CVD versus ECR CVD systems. ECR equipment has more stringent vacuum requirements due to its operation at lower pressures compared with plasma CVD equipment. Also, the wafer is located downstream from the plasma zone, thus isolating it from radiation damage. High-quality CVD films can be deposited at lower temperatures compared with plasma CVD films. Lower temperatures enable tight thermal budgets for high-performance submicron processes.

Table 2

Comparison of Operating Parameters for Plasma CVD and ECR CVD

Parameter	Plasma CVD	ECR CVD
Energy Source	RF	Microwave
Frequency	13.56 MHz	2.54 GHz
Pressure,	10-1,000 millitorr	0.01-1.0 millitorr
Ion Energy	100 electron volts	10 electron volts
Ion Density	10^6-10^8/cm^3	10^{10}-10^{12}/cm^3
Power	1,500-2,500 watts	200-500 watts
Temperature	25-50°C	300-400°C

Source: Dataquest
September 1989

Equipment Configuration

ECR equipment is available in two basic configurations--single-pole ECR and distributed multipole ECR.

Single-Pole ECR Configuration

Nippon Telegraph and Telephone Corporation (NTT) pioneered the single-pole ECR approach in Japan. Japanese equipment companies such as Anelva and Sumitomo Metals have licensed NTT's single pole ECR technology. Figure 2 illustrates NTT's ECR reactor concept. Japan leads the world in production implementation of ECR technology for submicron devices. In the United States, Lam Research will market an ECR CVD system in collaboration with its Japanese partner, Sumitomo Metals.

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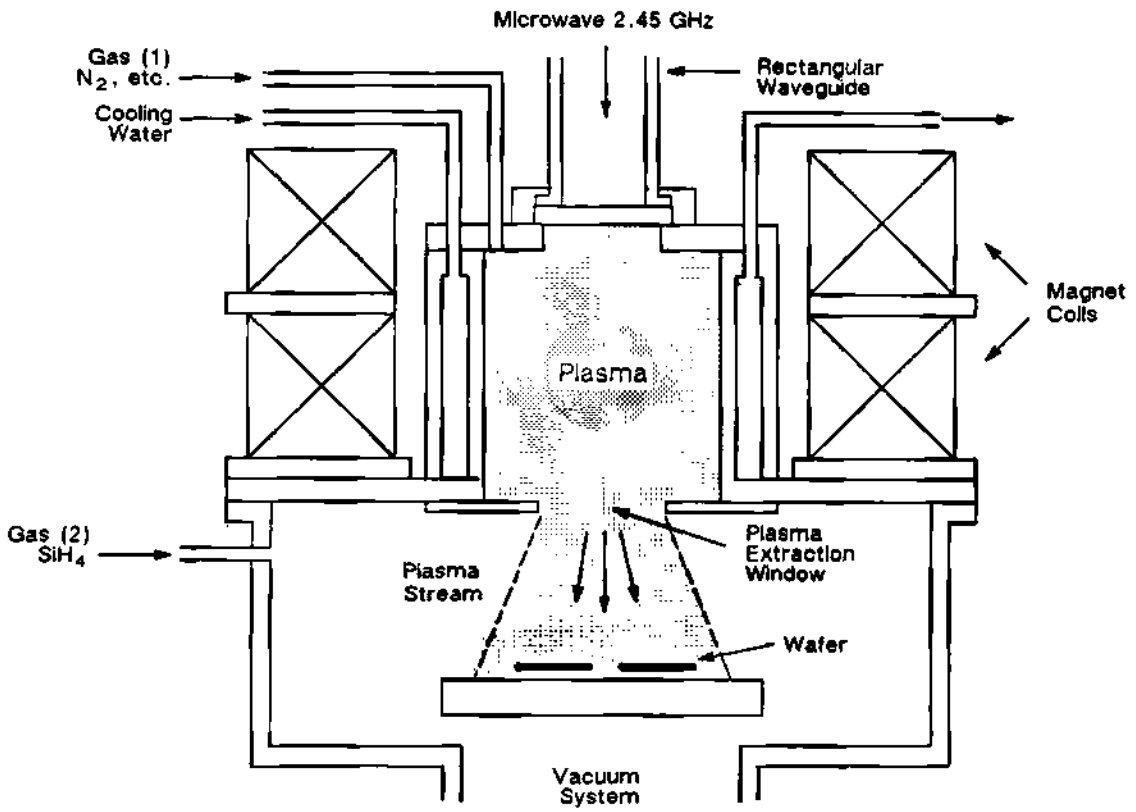
Figure 2

NTT's Single–Pole ECR Configuration



0004780-2

Source: NTT Japan

Multipolar ECR Configuration

The French National Research Organization, known as CNRS/CNET, pioneered the development of the multipolar, distributed ECR approach. Figure 3 illustrates the multipolar ECR concept. In this configuration, an array of microwave source antennas and permanent magnets are placed symmetrically around the edges of an octagonal reactor. The wafer is located at the center of the reactor chamber. Efficient plasma ionization is confined to the periphery of the reactor using the standard resonant combination of 2.45 GHz microwave energy with a 845–gauss magnetic field at each of the pole locations. Reactive ions with moderate energies drift toward the wafer at the center of the reactor, where they react with the reactant gas to deposit a high–quality CVD film. European equipment companies such as Alcatel and Electrotech have licensed the CRNS/CNET technology to develop commercial ECR CVD systems.

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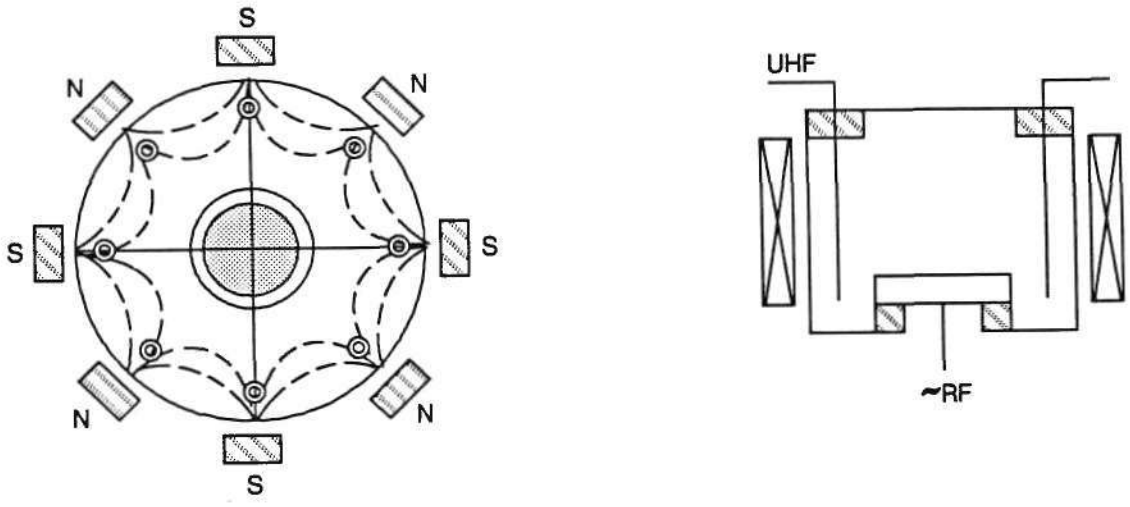
Figure 3

CNRS/CNET's Multipole ECR Configuration



0004780-3

Source: CNRS/CNET, France

Applications

ECR CVD films offer a promising range of submicron processing applications. ECR technology has the unique capability of depositing high-quality CVD films at low temperatures with minimal radiation damage. Hence, ECR technology is suited for low-temperature deposition of gate dielectrics, capacitor dielectrics, and planarized interlayer dielectrics.

Low-Temperature Gate and Capacitor Dielectrics

Advanced 4Mb and 16Mb DRAMs need high-quality gate and capacitor dielectrics with demanding material and electrical parameters. Current 1Mb DRAM processes use high-temperature (approximately 900°C) thermally grown gate, field, and capacitor oxides. Future submicron DRAM processes will emphasize low-temperature fabrication to achieve high performance. ECR CVD oxides, nitrides, and composite oxide/nitride dielectrics are being investigated for these applications. Organic liquid source materials such as TEOS can be used for these ECR CVD applications.

Interlayer Planarized Dielectrics

ECR CVD technology has the potential of in situ planarization during interlayer dielectric deposition. Furthermore, the low-temperature deposition process ensures the prevention of hillocks and intermetal shorts. A self-bias voltage on the wafer can be used to planarize device topology by simultaneous deposition and etchback using a 13.56 MHz RF frequency on the wafer stage. Thus, ECR CVD reactors offer an

integrated processing solution to the challenging problem of interlayer dielectric planarization. Disadvantages of ECR CVD for interlayer dielectrics include a relatively lower deposition rate and throughput, and also more complex process control due to many reaction variables.

INTEGRATED PROCESSING TECHNOLOGY

Multichamber CVD systems are the technology drivers in the trend toward integrated processing equipment. Integrated processing equipment offers the advantages of in situ multilayer film deposition and etching, lower defects, simplicity, flexibility, and progressive automation in semiconductor manufacturing. In the future, Dataquest expects flexible cluster tools (FCTs) to integrate areas such as CVD, sputter, etch, and rapid thermal processing around a central wafer-handling chamber. The emergence of industry standards for mechanical, wafer-handling, utilities, communications, and software interfaces will spur the acceptance of integrated processing cluster tools.

Equipment Configuration

Semiconductor manufacturers welcome the move to integrated processing. It enables them to configure flexible manufacturing systems using industry standard components from multiple-equipment vendors. A high degree of reliability and compatibility will be needed from different components of integrated processing systems. Any weak, incompatible link in the integrated process chain will make the entire system unusable and escalate operating costs tremendously. Open architecture and industry standards will lead to increased competition among equipment companies. Customer service and advanced process capabilities will be the differentiating factors in an otherwise standardized equipment environment.

Rigid multichamber tools (RMT) with a fixed number of process chambers are the precursors to FCTs with modular, expandable architecture. Figure 4 illustrates a generic rigid multichamber tool configuration. RMT systems have a fixed equipment configuration made up of three to four process chambers, each with its own vacuum pump. A loadlock chamber and a robotic transfer mechanism are used for staging and transferring wafers. Utilities such as power, cooling water, and gases are distributed to the individual process chambers through a central manifold. The computer and control functions are embedded in the main chamber. The process chambers are "dumb" and act as process-enabling slaves to the commands from the main computer.

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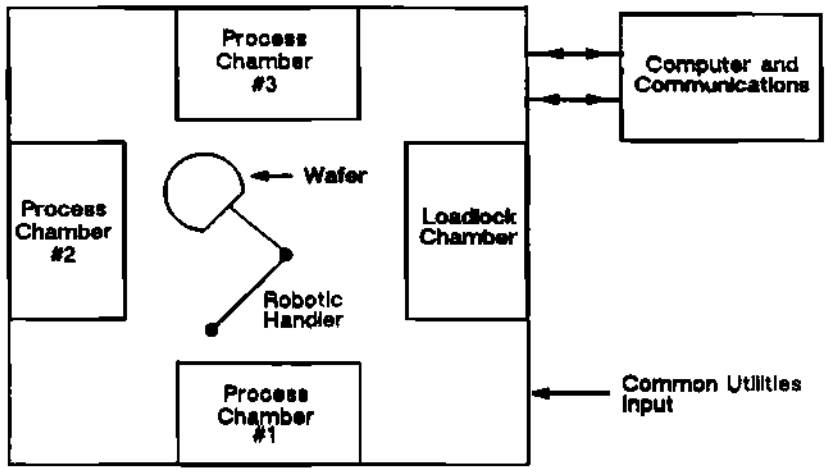
Figure 4

Schematic of a Rigid Multichamber Tool



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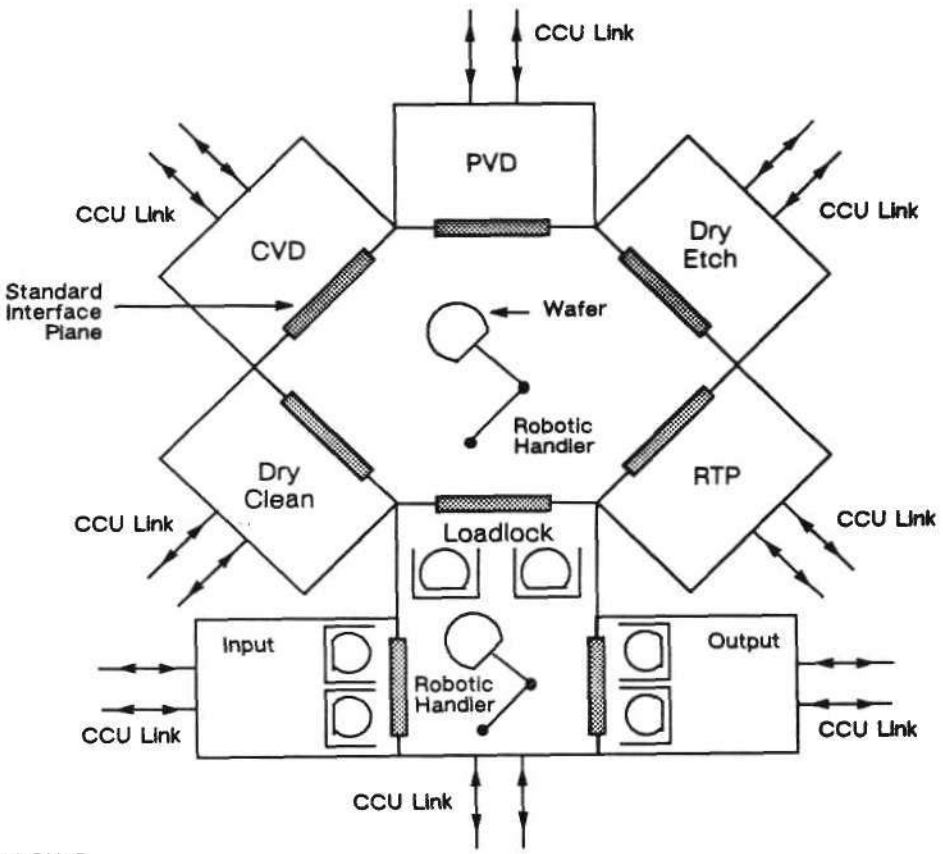
Source: Dataquest September 1989

In contrast, FCTs are highly modular and made up of detachable subsystems, each with its own computer, utilities, and communications abilities. Figure 5 shows a hypothetical flexible cluster tool. In general, the FCT system consists of a central, highly reliable automated wafer-handling platform equipped with a robot for transferring wafers between the input/output loadlock chamber and the process chamber module. The central wafer handling chamber has a series of standard wafer transfer interface ports to which the process module chambers or the input/output chambers may be bolted.

Ideally, each bolt-on process chamber is a "smart," fully functional reactor with its own vacuum pumps, utilities such as electricity and process gases, plasma power supply, gas distribution, computer, and communication units. The bolt-on process chamber should be capable of being unbolted and wheeled away for preventive maintenance and process development without interrupting the operation of the cluster mainframe tool. The bolt-on process chamber should be capable of being operated on a standalone basis for process development and qualification. The mainframe platform will have a supervisory computer, utilities, and communications systems for coordinating the process sequence through the bolted process modules.

Figure 5

Schematic of a Flexible Cluster Tool



Note: CCU link implies an interactive computer, communications, and utilities interface for each module.

Source: Dataquest September 1989

Table 3 lists the major worldwide companies that offer integrated processing equipment. Some of the systems are precursor RMT systems, which offer the traditional fixed multichamber configuration. Others are truly modular and can be classified as FCTs. A truly modular FCT system will allow the integration of several fabrication processes such as CVD, PVD, dry etch, rapid thermal processing (RTP), and dry clean onto the mainframe platform. The cluster tool will enable any arbitrary sequence of operations and random access to any of the process modules. Each of the process modules may be a single-wafer chamber or a multiwafer batch chamber.

Each of the modules attached to the central platform must be compatible with the overall system throughput, process sequence, film interface, and temperature cycles. For example, PVD chambers operate at substantially lower pressures when compared with CVD and etch chambers. Thus, the cluster configuration should be carefully optimized with regard to throughput, chamber type, and process flow for any given application. The process chamber has to deliver superior process results by itself and also in synergy with the other elements of the cluster tool.

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Table 3

Integrated Processing Equipment Companies and their Products

Company	Products	Dry Clean	CVD	PVD	Dry Etch	Dry Strip	RTP
Advantage Production Technology	SCR-2000	X					
Alcatel Comptech	GIR 820		X		X	X	
Anelva	ILC 1051	X		X			
	ILC 1551	X	X	X	X	X	
Applied Materials	PE 5000		X		X	X	
ASM International	Advance 600		X		X		
Balzers	Clusterline	X		X			
Branson/IPC	L3200				X	X	
BTU/Ulvac	ERA 1000		X				
Eaton	Radian	X		X			
Electrotech	Delta 200		X				
	Omega 200				X		
	Sigma 200	X		X			
General Signal (Drytek)	Quad				X	X	
Lam Research	Rainbow				X		
	ECR 3000		X		X		
Machine Technology Inc.	Sypherline	X		X			

(Continued)

Table 3 (Continued)

Integrated Processing Equipment Companies and their Products

Company	Products	Dry Clean	CVD	PVD	Dry Etch	Dry Strip	RTP
Materials Research Corporation	Eclipse	X		X			
	Aries				X		
Plasma Technology	AMR		X		X		
PlasmaTherm	Series 2800				X	X	
Rapro Technology	IPS 3000e		X				
Tegal	Series 2000				X	X	
Spectrum	Model 211		X				
Sumitomo Metals	ECR 3000		X		X		
Ulvac	MCH 9000	X		X			
	Stellar C2111	X	X	X	X		X
Varian	M2000	X		X			
	5103		X				
	RTP 8000						X

Notes: Dry clean module could be RF sputter etch or vapor clean.

Source: Dataquest
September 1989

Applications for Integrated Processing Technology

Numerous possible applications are emerging for integrated processing technology due to the versatility of the cluster tool concept. Dataquest believes that the RMTs available today are the precursors for tomorrow's highly integrated FCTs. The emergence of cluster tools and integrated process applications will be a

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barometer of automation trends in the semiconductor manufacturing business. The potential applications, described in the following paragraphs, are a sampling of many integrated processes that may emerge in the future.

Sandwich Oxide/Nitride Interlayer and Passivation Dielectrics

Integrated processing enables the in situ deposition of sandwich oxide/nitride dielectrics. These films combine the low stress and good interfacial properties of oxide films with the high integrity and passivation properties of nitride films. The multilayer films can be deposited by a combination of thermal and plasma processing using LPCVD, PECVD, and ECR CVD modules. Such combination films have applications as interlayer dielectrics and passivation layers in submicron processes.

Interlayer Dielectric Planarization

Cluster tools offer the possibility of an integrated process for interlayer dielectric deposition and planarization. In such applications, a combination of CVD and dry-etch chambers are configured around the central platform. The CVD system could be an APCVD, LPCVD, PECVD, or ECR CVD reactor. The dry-etch system could be operated in plasma, reactive ion etch (RIE), magnetically enhanced RIE, or ECR etch mode. A series of multiple depositions and etchbacks are performed with the appropriate processing sequence among different process chambers to achieve the desired degree of planarization. An optimum balance between the number of CVD and etch-process chambers is essential to ensure maximum system throughput.

Contact and Via Plug Conductor Planarization

Tungsten or other conductor plugs for contacts and vias can be fabricated in clustered integrated-process equipment. For blanket tungsten films, the plugs are obtained by etchback planarization using an appropriate combination of dry-clean, CVD, RTP, and dry-etch chambers. The dry-clean chamber is used for vapor phase thermal or plasma clean of contacts or vias prior to tungsten deposition. The CVD tungsten reactor can be either a batch or a single-wafer process. For blanket tungsten, etchback is carried out in a plasma or RIE chamber. Selective tungsten processes are simpler and do not need any etchback chambers. The RTP chamber may be used to anneal the tungsten plug and form a silicide in the contacts to lower the contact resistance.

Integrated processing is an enabling technology for selective tungsten, because it solves the main problem of selectivity loss due to contamination. By performing an in situ clean just prior to deposition, the selective tungsten process can occur on a clean surface without exposing the wafer to atmospheric contamination. A glue layer of tungsten silicide also can be deposited in one of the CVD process chambers before selective tungsten CVD.

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Self-Aligned Source-Drain-Gate Silicide or Refractory Metal

Self-aligned titanium silicide or cobalt silicide straps (also known as salicides) are used to reduce source, drain, and gate resistances in high-performance processes. Sensitivity to oxygen and moisture in the environment is one of the main problems associated with the silicide formation process. Integrated processing offers promise as a method for salicide formation. This process may use a combination of dry-clean, PVD, and RTP.

A dry-clean module using hydrogen fluoride (HF) vapors can be used to remove native oxide and condition the silicide formation areas; the source, drain, and gate areas. Next, the PVD module is used to sputter deposit a thin layer of titanium or cobalt. Finally, the wafer is annealed in the RTP chamber in a nitrogen environment to form the silicide in the active areas. By transferring the wafer from the PVD to the RTP chamber under vacuum, the titanium or cobalt film is preserved in a pure condition without oxygen or moisture absorption. After the wafers are removed from the cluster tool, they can undergo the standard wet etch for removing the unreacted titanium or cobalt from the field areas, leaving behind the salicide. A final RTP silicide anneal may be necessary after the wet etch to form the silicide fully and lower the sheet resistance to its final low value of 1 to 2 ohms per square.

Selective CVD tungsten on the source-drain-gate areas may be an alternative to the salicide technology. In the selective tungsten strap process, the process modules needed for the cluster tool are dry-clean, CVD, and RTP. After the dry-clean process using HF vapors, selective tungsten is deposited on the active device areas in the CVD chamber. Finally, an RTP anneal is performed in a inert argon environment to anneal the tungsten and form a thin base layer of silicide at the silicon interface in order to lower the contact resistance.

Multilayer Metallization Films for Reliable Interconnect Technology

Integrated cluster tools are an ideal method for depositing complex multilayer metal films for reliable interconnect technology. Such processes use a combination of dry-clean, PVD, CVD, and RTP modules. Sandwich interconnect films such as barrier/aluminum/refractory cap can be deposited using integrated process equipment.

The barrier metal can be a sputtered barrier such as titanium nitride (TiN) or titanium-tungsten (TiW) alloy. Sputtered barriers are deposited using a combination of dry clean and PVD modules. The dry-clean module uses a soft sputter etch or HF vapors to remove the native oxide. Frequently, a glue layer of titanium is sputtered in one PVD module before transferring the wafer to another PVD module for sputtering the barrier TiN or TiW film. TiN is sputtered in a reactive environment using a mixture of argon and nitrogen. Isolated, multichamber processing is essential to eliminate the effects of nitrogen cross-contamination between aluminum and TiN films. RTP annealing frequently is used between the barrier PVD and aluminum PVD to improve the barrier performance and contact resistance to silicon.

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Selective tungsten CVD plugs are an alternative to sputtered PVD barriers. In this case, the dry-clean and selective tungsten CVD may be followed by RTP anneal and aluminum PVD. Selective tungsten CVD barriers have the advantages of simplicity, good stepcoverage, and easy single-step aluminum interconnect etch. Dataquest anticipates that the availability of integrated cluster tools will expedite the adoption of selective CVD tungsten as a barrier and plug material.

Blanket and Selective Epi Growth and Annealing

High-performance CMOS, bipolar, and BiCMOS processes use epitaxial silicon (epi) extensively. Cost-effective epi films can be deposited in integrated-process equipment using multiple chambers to boost throughput without sacrificing epi quality. RTP modules can be attached to perform in situ anneal and epi dopant activation. New applications are emerging for the use of selective epi in high-density applications such as 16Mb and 64Mb DRAMs. Doped selective epi and polysilicon contact plugs are being explored as techniques to planarize submicron contacts prior to first-level metal.

Sequential Dry Etch of Multilayer Films

Multilayer conductor films such as barrier/aluminum/refractory cap and dielectric films such as oxide/nitride can be etched in multichamber dry-etch and dry-resist strip systems. Benefits of in situ sequential dry-etch and dry-resist strip without exposure to atmosphere include process simplicity, elimination of corrosive product species by immediate dry-resist strip, enhanced throughput, and lower costs.

Sequential etch of aluminum and the underlying TiN or TiW barrier is a common application for integrated dry etch and resist strip of multilayer conductor films. Chloride product residues that are left on the metal lines and the resist surface as a result of the aluminum etch can be stripped off in a dry-strip chamber prior to atmospheric exposure. Otherwise, chip corrosion and reliability hazards might result due to exposure of the wafer to atmosphere that contains moisture.

For interlayer dielectric and passivation films, multichamber dry etching is used to pattern composite oxide/nitride films. Integrated processing equipment allows the process engineer to use various combinations of plasma, RIE, triode, magnetic-enhanced RIE, and ECR etch modules to achieve optimum sidewall profiles for the device topology.

Integrated Gate Dielectric and Polycide Deposition

Integrated processing offers many advantages as gate dielectrics become thinner (less than 100 angstroms) in advanced products such as 4Mb DRAMs. Thin-gate dielectrics are extremely susceptible to contamination and defects if they are exposed to atmosphere for even short times. Electrical breakdown strength and device reliability suffer dramatically due to thin dielectric contamination and defects. Semiconductor manufacturers are investigating processes for in situ deposition of the gate dielectric, polysilicon, and refractory silicide gate.

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CVD Technology

High–quality submicron gate structures may be fabricated by combining dry–clean, RTP and CVD process modules into an integrated tool. Following a dry clean using organic cleaning agents and HF vapors, a high–quality gate dielectric is grown in the RTP module. Advanced 4Mb and 16Mb DRAMs may use composite oxide/nitride/oxide gate dielectrics for optimum interfacial and electrical characteristics. RTP processes have been developed that combine wet or dry oxidation with in situ ammonia anneals to nitridize the film. RTP modules also have the advantage of short process times to minimize exposure of the wafer to high temperatures.

Following the gate dielectric formation and anneal, polysilicon may be deposited and doped in situ in a CVD module. To reduce the sheet resistance of the gate material, a silicide capping film such as tungsten silicide can be deposited on the polysilicon in another CVD module. The composite polysilicon and silicide structure (also known as a polycide) combines the well–known oxide/poly interface with the low resistivity of the silicide material. After such an integrated gate dielectric and polycide process, the wafer is immediately ready for photolithographic patterning of the gate–level mask.

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CVD Companies

INTRODUCTION

This section describes the major chemical vapor deposition (CVD) equipment companies, their products, and applications for those products. In addition to this service section, more CVD information can be found in the accompanying service section entitled "CVD Technology," which describes the CVD process and equipment trends, and in the "Equipment Database" section of the Semiconductor Equipment and Materials binder, which contains detailed CVD equipment market information. Topical newsletters on CVD markets and technology are filed under the "Deposition" tab in the newsletters binder.

SUMMARY OF CVD EQUIPMENT COMPANIES, PRODUCT TECHNOLOGIES, AND APPLICATIONS

Table 1 shows the major worldwide CVD equipment companies and their product technologies, which can be classified into the following categories: nontube atmospheric CVD (APCVD), horizontal low-pressure tube CVD (HLPCVD), vertical low-pressure tube CVD (VLPCVD), nontube low-pressure CVD, horizontal plasma enhanced tube CVD (HPECVD), nontube plasma enhanced CVD, and nontube electron cyclotron resonance CVD (ECR CVD).

Table 2 summarizes the applications for products from major worldwide CVD equipment companies. Dataquest divides CVD equipment applications into the following major film categories: thermal nitride, polysilicon, plasma nitride, undoped oxide, doped oxide (PSG, BPSG), tungsten silicide, and tungsten. The choice of the appropriate tube or nontube CVD equipment technology depends on the film application, process flow, and temperature requirement.

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CVD Companies

Table 1

Major Worldwide CVD Equipment Companies and Their Technologies

U.S. Companies	Nontube APCVD	Tube HLPCVD	Tube VLPCVD	Nontube LPCVD	Tube HPECVD	Nontube PECVD	Nontube ECR CVD
Applied Materials	X			X		X	
BTU International		X	X				
BTU/Ulvac				X			
GSTC/Tempress	X	X	X		X		
Genus				X			
Lam Research							X
Novellus						X	
Pacific Western					X		
Plasma-Therm						X	
Process Technology		X					
Solitec		X					
Spectrum CVD				X			
SVG/Anicon				X			
SVG/Thermco		X	X				
Tylan		X					
Varian				X			
Watkins-Johnson	X						
Japanese Companies							
Amaya	X						
Anelva				X		X	
Enya		X					
Hitachi	X						
Japan Production						X	
Kokusai		X	X				
Koyo Lindberg		X	X				
Sumitomo Metals							X
Tokyo Electron		X	X				
Toshiba Machine	X						
Ulvac				X		X	
Ulvac/BTU		X	X				
European Companies							
ASM International		X		X	X	X	
E.T. Electrotech						X	
Plasma Technology						X	X
Wellman Furnaces		X					

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CVD Companies

Table 2

Applications for Products From Major Worldwide CVD Equipment Companies

U.S.Companies	Thermal Nitride	Poly Silicon	Plasma Nitride	Undoped Oxide	Doped Oxide (PSG,BPSG)	Tungsten Silicide	Tungsten
Applied Materials			X	X	X		X
BTU International	X	X		X	X		
BTU/Ulvac						X	X
GSTC/Tempress	X	X	X	X	X		
Genus						X	X
Lam Research			X	X			
Novellus			X	X	X		
Pacific Western			X	X			
Plasma-Therm			X	X			
Process Technology	X	X		X	X		
Solitec	X	X		X	X		
Spectrum CVD						X	X
SVG/Anicon				X	X	X	X
SVG/Thermco	X	X		X	X		
Tylan	X	X		X	X		
Varian						X	X
Watkins-Johnson				X	X		
Japanese Companies							
Amaya				X	X		
Anelva			X	X	X	X	X
Enya	X	X		X	X		
Hitachi				X	X		
Japan Production			X	X			
Kokusai	X	X		X	X		
Koyo Lindberg	X	X		X	X		
Sumitomo Metals			X	X			
Tokyo Electron	X	X		X	X		
Toshiba Machine				X	X		
Ulvac						X	X
Ulvac/BTU	X	X		X	X		
European Companies							
ASM International	X	X	X	X	X		
E.T. Electrotech			X	X	X		
Plasma Technology			X	X			
Wellman Furnaces	X	X		X	X		

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CVD Companies

PROFILES OF MAJOR CVD EQUIPMENT COMPANIES AND THEIR PRODUCTS

Profiles of major worldwide CVD equipment companies, product features, average selling price (ASP), and applications are presented here. The companies are grouped by the region in which the company's headquarters or parent offices are located. Even though the focus is on CVD products, a brief description of other product and industry segments relevant to company activities will be presented also. An understanding of these other competitive or complementary company technologies and products is essential to gaining insight into the company's strategy, its future direction, and its relation to the rest of the industry.

The reader is cautioned that the CVD product specifications and ASPs quoted in this section should be treated as nominal benchmark information. Actual product performance and ASP will depend on the application, equipment configuration, and production environment.

U.S. Companies

Applied Materials

Company Background. Applied Materials, Inc., (Applied) is the largest independent wafer-fabrication equipment company in the world. The company is publicly traded, and its corporate headquarters are located in Santa Clara, California. The company focuses on leading-edge semiconductor manufacturing equipment and process technology in order to maximize product life cycle while minimizing price competition and market downturn effects. Applied's products serve four broad wafer-fabrication equipment areas: CVD, dry etch, ion implant, and epi.

The company maintains a strong worldwide presence in its industry. It has production and development facilities in the United States, Japan, and the United Kingdom. Its sales and service centers are located throughout the world in major semiconductor manufacturing regions. The company operates in Japan through a wholly owned subsidiary known as Applied Materials Japan (AMJ). By establishing an early presence in Japan, Applied Materials has been successful in developing process solutions that meet the needs of the largest fabrication equipment market in the world: Japan. The AMJ subsidiary has allowed the company to build up a strong marketing presence in the rapidly growing Asia/Pacific Rim markets.

CVD Products and Applications. Table 3 shows Applied's major CVD products and applications. The AMS-2100 series CVD reactor was introduced in 1978 and found wide acceptance for undoped and doped atmospheric oxide deposition. The AMP-3300 plasma enhanced CVD reactor series also was introduced in 1978 for low-temperature oxide and nitride passivation applications. Applied is phasing out the AMS-2100 and the AMP-3300 products as it migrates its customers to the Precision 5000 (PE5000 CVD) system.

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CVD Companies

Table 3

Applied Materials: CVD Products and Applications

Product	Technology	Applications	ASP (K)	Comments
AMS-2100	Nontube APCVD	Undoped oxide Doped oxide	$ 540	Belt reactor, up to 200mm wafer size
AMP-3300	Nontube PECVD	Undoped oxide Plasma nitride	$ 350	Batch reactor, up to 125mm wafer size
PE-5000	Nontube PECVD	Undoped oxide Doped oxide	$1,000	Single-wafer reactor, up to 200mm wafer size
PE-5000	Nontube LPCVD	Tungsten	$ 960	Single-wafer reactor, up to 200mm wafer size

Source: Dataquest
November 1989

The PE5000 CVD system is Applied's flagship CVD product. It heralded the arrival of a new industry generation of CVD equipment with the following characteristics: single-wafer multichamber integrated processing, low-temperature PECVD technology, extensive automation, and modularity. The PE5000 CVD system is used to deposit conformal, low-temperature oxides (doped and undoped) and nitrides for interlayer dielectric (ILD) and passivation applications. The PE5000 dielectric CVD system is capable of in-situ planarization through sequential ILD deposition and etchback in separate chambers. Applied has recently introduced the PE5000 WCVD system for blanket tungsten deposition.

Applied Materials has emphasized low-particulates operation in the PE5000 series by limited wafer handling, movement below the wafer plane, and automatic plasma cleaning of the chamber between each wafer process cycle. The modular design of the PE5000 system provides easy expandability for either process options or throughput, with up to four independent bolt-on process chambers.

BTU International

Company Background. BTU International manufactures thermal processing equipment, automated wafer processing systems, and related process controls for the electronics industry. The company is publicly traded, and its corporate headquarters are located in North Billerica, Massachusetts. The company is structured into two divisions: The Bruce Systems Division focuses on wafer fabrication equipment, and the BTU Systems Division focuses on equipment for packaging, hybrid circuit manufacturing, and reflow solder applications.

CVD Companies

BTU has direct sales and customer support in locations throughout the United States, Europe, and the Asia/Pacific Rim regions. In Japan, the company's sales and services are conducted through a joint venture known as Ulvac-BTU Limited, located in Tsukuba, Japan. Ulvac-BTU manufactures diffusion and LPCVD tube systems for the Japanese fabrication equipment market using BTU components and technology. In 1989, BTU formed a U.S. joint venture known as BTU-Ulvac to market Ulvac's coldwall LPCVD tungsten reactor in the United States and Europe.

CVD Products and Applications. Table 4 lists BTU's CVD products, technology, and applications. BTU has four major tube families for diffusion and LPCVD film applications: BDF-4, BDF-41, System 2000, and the System 2100 series. The BDF-4 is a four-tube, manually loaded diffusion and LPCVD stack capable of handling wafer sizes up to 125mm. The BDF-41 is a four-tube automated stack capable of 150mm wafer processing. The System 2000 and the System 2100 are BTU's latest tube CVD products offering capability up to 200mm wafers. The System 2000 is a horizontal, automated tube stack, while the System 2100 is a vertical tube family with vacuum load-lock abilities.

Table 4

BTU International: CVD Products and Applications

Product	Technology	Applications	ASP	Comments
BDF-4	Horizontal tube LPCVD	Thermal nitride, polysilicon, undoped and doped oxide	$125K/tube	4-tube stack, manually loaded, up to 125mm wafer size
BDF-41	Horizontal tube LPCVD	Thermal nitride, polysilicon, undoped and doped oxide	$200K/tube	4-tube stack, automated up to 150mm wafer size
System 2000	Horizontal tube LPCVD	Thermal nitride, polysilicon, undoped and doped oxide	$250K/tube	4-tube stack, automated up to 200mm wafer size
System 2100	Vertical tube LPCVD	Thermal nitride, polysilicon, undoped and doped	$275K/tube	Vertical tube family, automated, up to 200mm wafer size
ERA-1000	Nontube LPCVD	Tungsten, tungsten silicide	$700K	Single-wafer, dual-chamber reactor, 200mm capability

Source: Dataquest
November 1989

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The ERA-1000 tungsten LPCVD reactor, developed by Ulvac in Japan, is offered by the BTU-Ulvac joint venture in the United States. It is a multichamber reactor, with each reactor having its own independent heater, pumps, gas supply lines, power supply, and controls. The ERA-1000 is targeted toward selective and blanket tungsten plug applications for contact and via filling in submicron multilevel interconnect processes.

General Signal ThinFilm Company (GSTC)

Company Background. The General Signal Corporation is a diversified, publicly held company that participates in industries such as semiconductor equipment, instrumentation and control, telecommunications, industrial automation, energy management, and rail transportation. GSTC is part of General Signal Corporation's Semiconductor Equipment Group (SEG). The SEG unit, headquartered in Andover, Massachusetts, is a major worldwide supplier of semiconductor capital equipment. The group's various operating units design, manufacture, and market a variety of semiconductor equipment including crystal-growing furnaces, wafer saws and polishers, diffusion/deposition equipment, photolithography equipment, plasma etch/strip equipment, wafer probers, and die bonders. The operating units within SEG are: Advanced Mechanization, Blue M, Drytek, Electroglas, GCA, GCA Tropel Division, GSTC, Kayex, Micro Automation, Ruckers and Kolls, Semiconductor Systems, and Ultratech Stepper.

The GSTC operating unit, located in Fremont, California, was created in June 1987 by combining several operations: Tempress, which makes diffusion and CVD equipment; Ionscan, which makes ion implantation uniformity and thin-film measuring equipment; Circuits Processing Apparatus, which makes sputtering equipment; and Ultratech Photolytics, which makes an excimer laser CVD system. The GSTC unit designs, manufactures, and markets diffusion, CVD, and thin-film deposition equipment for semiconductor manufacturing.

CVD Products and Applications. Table 5 lists GSTC's CVD products, technology, and applications. The Pyrox APCVD reactor was pioneered by Tempress for undoped and doped oxide applications. However, APCVD reactors are declining in use as semiconductor manufacturers migrate to LPCVD and PECVD reactors that produce higher-quality films. GSTC's Omega 5000 Series automated PECVD tube systems are targeted toward submicron, low-temperature oxide and nitride applications. The Enhanced Vertical Thermal Reactor (EVTR) family is targeted toward high-quality thermal oxides, poly, and thermal nitride applications. Both the Omega 5000 Series and the EVTR Series are capable of 200mm wafer processing.

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CVD Companies

Table 5

GSTC: CVD Products and Applications

Product	Technology	Applications	ASP	Comments
Pyrox	Nontube APCVD	Doped and undoped oxides	$200K	Batch, hotwall reactor
Omega 5000 Series	Horizontal tube PECVD	Undoped oxide, plasma nitride	$200K/tube	Automated stacks, up to 200mm wafer size
EVTR Series	Vertical tube LPCVD	Thermal nitride, polysilicon	$250K/tube	Automated handling, small footprint, up to 200mm wafer size

Source: Dataquest
November 1989

Genus

Company Background. Genus, Inc., designs, manufactures, markets, and services thin-film deposition and high-energy ion implantation systems for use in the fabrication of advanced integrated circuits. The company is publicly traded and is headquartered in Mountain View, California. Genus' CVD systems are widely used to deposit tungsten silicide and tungsten films in submicron processes. Genus has direct sales and service locations throughout the United States. Genus Europa Ltd., a wholly owned subsidiary of Genus located in Melbourn, England, serves the European market. In Japan, the company is represented by Innotech Corporation and C. Itoh Corporation. Genus is also actively marketing its products in the other growing Pacific Rim markets such as South Korea and Taiwan.

CVD Products, Technology, and Applications. Table 6 lists Genus' CVD products, technology, and applications. The 8700 series reactors are the flagship CVD products. The 8710 system is used for silicide deposition, and the 8720 system is used for blanket or selective tungsten deposition using silane or hydrogen chemistry. The 8700PC system is a single-wafer research system for advanced thin-film development.

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CVD Companies

Table 6

Genus: CVD Products and Applications

Product	Technology	Applications	ASP (K)	Comments
8710	Nontube LPCVD	Tungsten silicide	$650	Batch reactor, up to 200mm wafer size
8720	Nontube LPCVD	Blanket and Selective tungsten	$850	Batch reactor, silane or hydrogen process, up to 200mm wafer size
8700PC	Nontube LPCVD	Research tool	$200	Single-wafer reactor, 200mm capability, upgradable to production

Source: Dataquest
November 1989

Lam Research

Company Background. Lam Research designs, manufactures, and markets thin-film processing equipment used in wafer fabrication. The company is publicly traded and is headquartered in Fremont, California. The company's product offerings include a wide range of single-wafer dry etch systems, a family of silicon epitaxial systems, and electron cyclotron resonance (ECR) CVD systems in partnership with Sumitomo Metals of Japan. The company has sales and service locations throughout the major semiconductor manufacturing regions in the United States. Sumitomo Metals is the exclusive distributor of Lam Research's Rainbow dry etch systems in Japan. Lam Research earlier had an arrangement with Tokyo Electron Ltd. to manufacture and market its older AutoEtch series etch systems. This arrangement was terminated in 1987; TEL now markets its own dry etch systems based on enhancements to the AutoEtch design. Lam Research actively markets its systems in other Asia/Pacific region countries such as South Korea and Taiwan.

CVD Products and Applications. The ECR-3000 system developed by Sumitomo Metals will be marketed exclusively by Lam Research in the United States and Europe. The system, at an ASP of $1 million, is a single-wafer reactor with 200mm capability. It is targeted toward high-quality, low-temperature CVD dielectric applications. This system is capable of in-situ planarization through topology-dependent deposition and etchback technology. Dataquest believes that Lam Research may overcome the low-throughput limitations of ECR CVD planarization by offering multichamber equipment configuration. Lam Research also is developing its Integrity series CVD systems, which may be introduced in 1990.

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CVD Companies

Novellus

Company Background. Novellus Systems, Inc., manufactures advanced automated wafer-fabrication systems for semiconductor manufacturing and development. The company is publicly traded and is headquartered in San Jose, California. The company focuses on the CVD equipment market. It has expanded aggressively to provide worldwide customer service in all major semiconductor manufacturing regions. Novellus has exhibited spectacular growth due to the success of its pioneering Concept One CVD system design.

CVD Products and Applications. Novellus' flagship product is the Concept One CVD system that is targeted toward the demanding ILD and passivation dielectric market. The Concept One's ASP is $760,000. Novellus claims that its unique sequential-deposition batch system together with the localized plasma reaction zones results in exceptionally good throughput, uniformity, and film quality. Applications for the Concept One system include doped and undoped oxides and passivation plasma nitride films. Dataquest believes that Novellus is developing a tungsten CVD system that will compete in the interconnect film market.

Pacific Western Systems (PWS)

Company Background. PWS manufactures diffusion, CVD, tester, and mechanical prober systems for the semiconductor industry. The company is privately held and has headquarters in Mountain View, California. PWS claims to be small and flexible in order to serve the ever-changing needs of the semiconductor industry through custom-tailored equipment solutions. The company also markets equipment subsystems such as gas cabinets, plasma CVD tube retrofit kits, and computerized furnace control systems.

CVD Products and Applications. The company's model series 560 plasma enhanced CVD system is a low-temperature batch tube system (ASP/tube: $250,000) for depositing a broad range of films: nitride, doped and undoped oxide, poly, and amorphous silicon. The standard system consists of one or two tubes operating as independent units housed in a single frame.

Plasma-Therm

Company Background. Plasma-Therm manufactures plasma etch, deposition, and RF power supply components to the semiconductor industry. The company is publicly held and headquartered in Voorhees, New Jersey. The company's semiconductor fabrication equipment is used in research and production applications in the United States, Japan, South Korea, and Europe. The company maintains a growing number of strategically located application and service centers to serve all the major semiconductor manufacturing regions in the world.

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CVD Companies

CVD Products and Applications. Plasma-Therm's 700 Series deposition systems (ASP: $200,000) are designed for development and pilot-line applications. The SL-734 is a batch, load-locked reactor with 200mm wafer capability for in situ PECVD and RIE etchback planarization. The SL-770 is a batch, load-locked ECR reactor with 150mm wafer capability for low-temperature, low-damage etch and deposition applications.

Process Technology Ltd. (PTL)

Company Background. PTL is an independent privately held company headquartered in New Brunswick, Canada. PTL manufactures diffusion and LPCVD systems and components for the semiconductor industry. The PTL product line include gas panels, source cabinets, quartzware, and new or retrofitable diffusion/LPCVD tube systems.

CVD Products and Applications. PTL offers diffusion and LPCVD tube systems for applications such as thermally grown oxide, doped and undoped ILD oxides, doped and undoped polysilicon, silicon nitride, and tungsten. The company offers custom-designed new and retrofitable components and systems to upgrade or expand tube furnace stacks. Its products (ASP: $150,000/tube) can handle 2- through 6-inch wafer sizes.

Silicon Valley Group (SVG)

Company Background. SVG, Inc., is a major, publicly held company that manufactures wafer fabrication equipment. The company is headquartered in San Jose, California. Since beginning operations in 1977, the company has grown by expanding existing distribution channels and extending product lines through internal development and acquisitions. SVG's initial products were photoresist track systems and components. In 1986, SVG diversified into the CVD market by developing a vertical thermal reactor (VTR) and subsequently acquiring Anicon Inc, a nontube CVD reactor company. In December 1988, SVG further expanded its product offerings through the acquisition of Thermco Systems, a leading supplier of horizontal diffusion, oxidation, LPCVD, and factory automation systems. SVG is currently organized into two product divisions: the Track Systems Division, which focuses on photolithography equipment, and the Thermco Systems Division, which focuses on diffusion, oxidation, CVD, and factory automation equipment.

CVD Products and Applications. Table 7 shows SVG's major CVD products, technology, and applications.

CVD Companies

Table 7

SVG: CVD Products and Applications

Product	Technology	Applications	ASP	Comments
Anicon	Nontube LPCVD	Thermal nitride, poly, doped oxide, undoped oxide, tungsten	$570K	Batch, hotwall reactor, up to 150mm wafer size, automated wafer handling
VTR-6000	Vertical tube LPCVD	Thermal nitride, poly	$250K/tube	Small footprint, fully automated, up to 200mm wafer size
Series 5000	Horizontal tube LPCVD	Thermal nitride, poly, doped oxide, undoped oxide	$200K/tube	Horizontal tubes, automated, up to 150mm wafer size

Source: Dataquest
November 1989

Solitec

Company Background. Solitec, formerly known as Reid-Ashman, is located in Santa Clara, California. It is a publicly held company that manufactures a wide variety of wafer-fabrication and test equipment. Solitec's product lines include photoresist track systems, quartz and bell jar cleaning systems, UV exposure and mask alignment systems, diffusion and CVD tube equipment, and auxiliary test components. The diffusion and CVD products are designed, manufactured, and marketed by Advanced Crystal Sciences, Inc., a subsidiary of Solitec.

CVD Products and Applications. Solitec's Falcon IV tube product series (ASP: $150,000/tube) is a fully integrated automated system for diffusion and LPCVD processes. The system incorporates modular components and is designed to accommodate up to four tubes in the furnace stack. The system can handle wafer sizes up to 150mm and can be automated for production applications using cantilever or soft-land autoloaders. Applications for the Falcon IV products include thermally grown oxides, doped and undoped oxides, poly, nitride, and tungsten. ACS also offers furnace upgrade and expansion services.

Spectrum CVD

Company Background. Spectrum CVD is one of Motorola's New Enterprises companies to which Motorola provides financial backing and high-level executive management. The company is headquartered in Phoenix, Arizona. It focuses on

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developing CVD systems for advanced device processing applications. The company plans to leverage off Motorola's venture-capital support and synergy with other Motorola New Enterprises companies such as Tegal to offer advanced product, process, and service support to semiconductor manufacturers. Tegal focuses on advanced dry etch equipment technology, which complements Spectrum CVD's thin-film processes.

CVD Products and Applications. Spectrum CVD's flagship product is the Model 211 single-wafer system for applications such as tungsten silicide, blanket tungsten, and selective tungsten. The system's ASP is $530,000. It is an automated, coldwall system that can be operated in LPCVD or PECVD mode. The Model 211 can handle wafer sizes up to 200mm. Spectrum CVD also offers the Model 202 system, which is designed for thin-film research and development. The Model 202 system uses the same reactor chamber and radiant heater as the Model 211 system. This facilitates process transfer from development and pilot lines using the Model 202 to full-scale manufacturing lines using the Model 211.

Tystar Corporation

Company Background and Strategy. Tystar Corporation (Tystar), a privately-held company in Torrance, California, was formed in 1988 from the divestiture of Tylan Corporation's equipment business. It is headed by Dr. Klaus Schuegraf, who was previously Tylan Corporations' director of technology. The company manufactures diffusion tubes, CVD tubes, and nontube photochemical CVD reactors. The products are sold through manufacturer representatives throughout the world.

CVD Products and Applications. Tystar's LPCVD tube products (ASP: $150,000/tube) are capable of processing wafer sizes up to 200mm for films such as undoped and doped oxide, nitride, and poly. The PCVD-100 photochemical CVD reactor is capable of processing wafer sizes up to 200mm for low-temperature oxide/nitride dielectric applications.

Varian Associates

Company Background and Strategy. Varian Associates, Inc., a diversified high-technology company, produces systems and components for the worldwide communications, defense, scientific, medical, and industrial markets. It is a publicly held company headquartered in Palo Alto, California. Varian's Semiconductor Equipment Group (SEG) designs, manufactures, and markets ion implanters, sputtering systems, CVD systems, rapid thermal processing systems, and molecular beam epitaxy systems. The Varian-TEL joint venture assembles, markets, and services TEL's dry etch, vertical furnace, and photoresist track systems in the United States and Europe. Conversely, the TEL-Varian joint venture assembles, markets, and services Varian's ion implant systems in Japan.

CVD Products and Applications. The Varian-TEL joint venture markets the VCF 610 vertical tube LPCVD system in the United States and Europe. These systems are capable of 200mm wafer processing for applications such as poly and nitride films.

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Varian markets the 5100 series coldwall nontube LPCVD system for selective tungsten, blanket tungsten, and tungsten silicide film applications. It is highly modular and capable of being extended to 200mm wafer size processes. The Model 5101 is a single-chamber system; the Model 5103 is a three-chamber system with an ASP of $750,000.

Watkins-Johnson

Company Background. Watkins-Johnson is a diversified company producing components and systems for the defense and semiconductor industry sector. The company is publicly held and headquartered in Scotts Valley, California.

CVD Products and Applications. The WJ-900 series belt-type APCVD reactor is used for undoped and doped oxide (PSG, BPSG) applications. The system has an ASP of $580,000 and is capable of handling wafer sizes up to 200mm. New CVD applications are being developed for films such as silicon nitride, tungsten silicide, and polysilicon.

Japanese Companies

Amaya

Company Background. Amaya, a privately held company established in April 1963, is headquartered in Tokyo. The company manufactures and markets APCVD and PECVD systems.

CVD Products and Applications. Table 8 lists Amaya's CVD products and applications.

Table 8

Amaya: CVD Products and Applications

Product	Technology	Applications	ASP (K)	Comments
AMAX-200	APCVD	Undoped oxide, PSG, BPSG	$300	150mm wafer size capability, fully automated, batch reactor
AEC-2250	APCVD	Undoped oxide, PSG, BPSG	$400	Up to 150mm wafer size, continuous belt reactor
AMAX-600	PECVD	Undoped oxide, plasma nitride	$500	200mm wafer size capability, batch parallel-plate reactor.

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CVD Companies

Anelva

Company Background. Anelva (analysis, electronics, vacuum) is a major semiconductor equipment company that designs, manufactures, and markets thin-film processing systems for the semiconductor and electronics components business. The company was formed in 1967 as a joint venture between NEC and Varian Associates. Varian sold its share of the joint venture back to Anelva in 1977. The company is headquartered in Fuchu, Tokyo. Anelva categorizes its products in two main areas: thin-film production equipment including sputtering, evaporation, and CVD systems, and thin-film analysis equipment including gas analyzers, surface analyzers, vacuum pumps and components, pressure monitors, and sputtering materials.

CVD Products and Applications. Anelva's CVD products include the ILC-1051 and the ILC-1551 series single-wafer, multichamber systems. The ILC-1551, intended for R&D and small-volume production, is a three-chamber system with an ASP of $1 million. Possible process modules include aluminum and refractory barrier metal sputtering, refractory metal/silicide CVD, and ECR dielectric CVD. The ILC-1051, intended for production applications, is a four-chamber system (ASP: $1.5 million) that can be operated in series or in parallel for higher throughput. The ILC-1051 and the ILC-1551 have been designed with the same concept so that new process modules developed on the ILC-1551 can be easily transferred to volume production on the ILC-1051 platform.

Enya Seisakusho

This small privately held company is based in Tokyo. It offers products in the areas of wet process equipment and PECVD and LPCVD reactors.

Hitachi

Company Background. Hitachi is a major diversified conglomerate company with activities in many industrial areas including power systems and equipment, consumer electronics, electronic devices, computers, communications, industrial machinery, cable/wire, metals, and chemicals. Hitachi markets semiconductor manufacturing equipment through a wholly owned trading company known as Nissei Sangyo. The semiconductor equipment categories include virtually all aspects of semiconductor manufacturing including lithography, ion implant, etch, deposition, inspection, surface analysis, and clean-room modules.

CVD Products and Applications. Hitachi's model 415-A/515-A CVD reactors (ASP: $300,000) employ APCVD technology to deposit doped (PSG, BPSG) and undoped oxides. These reactors are batch, automated reactors that are capable of handling wafer sizes up to 200mm. Hitachi also markets an ECR deposition reactor for submicron applications.

Japan Production Engineering

This small privately held company is based in Tokyo. It offers nontube PECVD reactors for depositing low-temperature plasma oxides and nitrides.

CVD Companies

Kokusai Electric

Company Background. Kokusai Electric, founded in 1949, is a publicly held company headquartered in Tokyo. The company has organized its activities into four main divisions: communications equipment, data processing equipment, semiconductor manufacturing equipment, and electronic parts and components. The company's semiconductor manufacturing equipment includes the following major categories: single-crystal growth, epi growth, LPCVD, oxidation/diffusion furnaces, reactive ion etch systems, wafer resistivity mapping systems, and IC package automatic test handlers.

CVD Products and Applications. The company's DJ-600 series and DD-7000 series horizontal tube LPCVD systems are capable of handling wafer sizes up to 150mm. The DJ-600 has optional automation features, and the more advanced DD-7000 series offers complete automation and direct digital temperature control. ASPs for these tube systems are in the range of $200,000 to $250,000 per tube. Applications for these horizontal tube LPCVD systems include doped and undoped polysilicon, thermal nitride, and undoped and doped oxides (PSG, BPSG). The company's DJ-800V Vertex series vertical LPCVD tube systems have the features of full automation and 200mm capability for submicron processes.

Koyo Lindberg

Company Background. Koyo Lindberg was formed in 1967 as a joint venture between General Signal's Lindberg Division and Koyo Seiko in Japan. In 1981, Tempress (Japan) merged with Koyo Lindberg Limited. The company is publicly held and is headquartered in Tenri City, Nara. The company's product lines include industrial heat-treating furnaces, electronics industry conveyer furnaces, semiconductor manufacturing equipment, and die-sawing assembly equipment. Koyo Lindberg markets the following semiconductor manufacturing equipment in collaboration with General Signal: diffusion and LPCVD tubes, nontube CVD reactors, and rapid thermal processing systems.

CVD Products and Applications. Table 9 lists Koyo Lindberg's CVD products and applications.

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Table 9

Koyo Lindberg: CVD Products and Applications

Product	Technology	Applications	ASP	Comments
200 Series	LPCVD tube	Poly, thermal nitride, doped and undoped oxide	$150K/tube	Horizontal system, optional automation, up to 150mm wafer size
4000 Series	LPCVD tube	Poly, thermal nitride, doped and undoped oxide	$200K/tube	Horizontal system, fully automated, up to 200mm wafer size
VF2000 Series	LPCVD tube	Poly, thermal nitride, doped and undoped oxide	$200K/tube	Vertical system, manually loaded, up to 150mm wafer size
VF4000 Series	LPCVD tube	Poly, thermal nitride, doped and updoped oxide	$250K/tube	Vertical system, fully automated, up to 200mm wafer size
Pyrox	APCVD	Doped and undoped oxide	$225K	Batch reactor, up to 200mm wafer size, manually loaded

Source: Dataquest
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Sumitomo Metals

Company Background. Sumitomo Metals is a large, vertically integrated company engaged in steel production as well as finished products such as wheels, gears, forgings, castings, and truck components. The company is publicly held and headquartered in Tokyo. The company's research group focuses on development of advanced semiconductor manufacturing equipment.

CVD Products and Applications. Sumitomo Metals has developed electron cyclotron resonance (ECR) CVD and dry etch equipment for advanced semiconductor, magnetic media, and optical component coating applications. The ECR-110/210 series is targeted toward research applications, and the ECR-1000/2000 series is targeted toward submicron production applications. The production ECR equipment has single-wafer automated architecture with 150mm wafer-processing capability and an ASP of $1 million. Film applications include low-temperature oxide and nitride deposition.

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CVD Companies

Tokyo Electron Limited (TEL)

Company Background. TEL was established as a trading company in 1963. Since then, the company has augmented its trading activities with internally developed design, manufacturing, and marketing capability for a broad range of electronic products. The company is publicly held and headquartered in Fuchu, Tokyo. TEL participates in the following markets: semiconductor production equipment, measurement/analysis equipment, computer systems, and electronic components. TEL has adopted a global business strategy through joint ventures with leading worldwide companies.

CVD Products and Applications. Tube LPCVD products are offered by a wholly owned TEL subsidiary known as TEL-Sagami. The company offers both horizontal and vertical LPCVD tube furnaces. The HLPCVD systems have an ASP of $190,000; the VLPCVD systems have an ASP of $250,000. The furnaces are highly automated and possess 150mm wafer-processing capability. Applications for the tube LPCVD furnaces include doped and undoped polysilicon, thermal nitride, doped and undoped oxides. TEL also markets Varian's 5103 multichamber tungsten CVD system in Japan.

Toshiba Machine

Company Background. Toshiba Machine Company is part of the Toshiba Group, Japan. The company offers a wide variety of semiconductor manufacturing equipment and materials. Equipment categories offered include mask-making and e-beam lithography equipment, crystal growers, epitaxial reactors, diffusion tubes, dry etch, CVD, sputtering systems, test equipment, and assembly equipment. The company is headquartered in Tokyo.

CVD Products and Applications. The company offers the CVD-5M/CVD-6M batch APCVD systems. Applications include doped and undoped oxides. The tube CVD products are used for poly and nitride applications.

Ulvac

Company Background. Ulvac Corporation, headquartered in Tokyo, is a large, diversified company focused on vacuum technology and applications. The company designs, manufactures, and markets a broad range of vacuum-based thin-films processing equipment and materials. Equipment products include semiconductor manufacturing equipment such as CVD, sputtering, diffusion furnaces, ion implanters, dry etch, and molecular-beam epitaxy. The company distributes its semiconductor manufacturing equipment directly through wholly owned subsidiaries in the United States, Europe, and Asia/Pacific. Ulvac also participates in two joint ventures with BTU International. Ulvac/BTU, based in Japan, markets and services BTU diffusion, LPCVD, and factory-automation equipment in Japan. BTU/Ulvac, based in the United States, markets and services Ulvac's coldwall tungsten CVD system in the United States and Europe.

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CVD Products and Applications. Ulvac's ERA-1000 is a completely automated nontube LPCVD single-wafer reactor capable of 200mm wafer processing. The system has two independent process chambers that can be operated in series or in parallel. The system's ASP is $760,000. The main applications for the ERA-1000 system are selective tungsten, blanket tungsten, and tungsten silicide. Also, Ulvac recently introduced its MCH-9000 Series cluster equipment, which is capable of integrating sputtering and CVD modules.

European Companies

ASM International

Company Background. ASM International is a diversified, globalized semiconductor equipment company. It is publicly held and headquartered in Bilthoven, the Netherlands. The company participates in all the major semiconductor manufacturing regions of the world through independent subsidiaries: ASM America, ASM Japan, ASM Pacific Technology in Hong Kong. All the subsidiaries are publicly traded in their respective regional stock markets. ASM International has adopted a strategy of globalized design, manufacturing, marketing, and service for its products. ASM's core business is in the areas of diffusion, epi, CVD, and assembly equipment. It recently exited from the lithography equipment market by selling its part of the ASM Lithography/N.V. Philips joint-venture to N.V. Philips. ASM also exited from the ion implant equipment market by selling ASM Implant to Varian Associates.

CVD Products and Applications. Table 10 lists ASM International's CVD products and applications. It offers tube and nontube CVD products. The Advance 600 multichamber cluster tool is ASM's platform for future integrated processing technology using a combination of CVD, sputtering, and dry etch modules.

Table 10

ASM International: CVD Products and Applications

Product	Technology	Applications	ASP	Comments
DFS 200 Series	Horizontal tube LPCVD	Poly, nitride, doped/undoped oxide	$180K/tube	Fully automated, up to 150mm wafers
VMP-100 PRO Series	Vertical tube LPCVD	Poly, nitride	$250K/tube	Fully automated, up to 200mm wafers
Plasma III Series	Horizontal nontube PECVD	Doped/undoped oxide, nitride	$240K/tube	Fully automated, up to 150mm wafers
Advance 600 Series	Nontube PECVD Nontube PECVD Nontube LPCVD	Doped/undoped oxide, nitride aluminum	$900K	Cluster tool, up to four process modules, up to 200mm wafers

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CVD Companies

E.T. Electrotech

Company Background. Electrotech is a privately held semiconductor equipment company headquartered in Bristol, England, the United Kingdom. The company offers R&D, pilot-line, and production wafer-fabrication equipment in the following major process areas: plasma CVD, dry etch, and sputtering. Electrotech has direct sales, marketing, and service areas in all major semiconductor manufacturing regions in the United States, Japan, Europe, and the Asia/Pacific and Rest of World (ROW) areas.

CVD Products and Applications. Table 11 shows Electrotech's CVD products and applications. Electrotech's early CVD products emphasized batch PECVD reactor technology, evidenced by the ND6200 family of products. More recently, Electrotech has adopted the popular single-wafer, multichamber system for its CVD, dry etch, and PVD processes. Electrotech also has licensed the French CNRS/CNET Laboratory's multipolar ECR technology. It will offer a line of single-chamber ECR dry etch and CVD systems for development applications, which can be scaled up to production.

Table 11

E.T. Electrotech: CVD Products and Applications

Product	Technology	Applications	ASP	Comments
ND6200 Series	Nontube, batch PECVD	Doped/undoped oxide, nitride	$650K	Up to 200mm wafer, fully automated
Delta Series	Nontube, single-wafer, multi-chamber PECVD	Doped/undoped oxide, nitride	$850K	Up to 200mm wafer, fully automated, cluster tool
310PC	Nontube, single-wafer, PECVD system	R&D	$300K	Up to 200mm wafer, manual, flexible tool
MPM390	Nontube, single-wafer, ECR CVD	Undoped oxide, nitride	$400K	Up to 200mm wafer, R&D tool

Source: Dataquest
November 1989

Plasma Technology

Company Background. Plasma Technology is a privately held company headquartered in Bristol, England, the United Kingdom. The company manufactures plasma-based semiconductor fabrication equipment for R&D and pilot line applications. The company focuses on low-damage dry etch and PECVD equipment for advanced VLSI

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and compound semiconductor device fabrication. Plasma Technology markets and services its products through Microscience, Inc., in the United States and through Marubun Corporation in Japan. It uses representative agencies to market its products in the Asia/Pacific and ROW regions.

CVD Products and Applications. Plasma Technology's Plasmalab series system is used for R&D applications. The 8000 series PECVD system is designed for low-volume, pilot-line oxide and nitride applications. It is capable of handling wafer sizes up to 150mm in diameter. Plasma Technology also offers the 3000R series ECR CVD reactors for amorphous, polycrystalline, and epitaxial silicon deposition in an R&D or pilot-line environment.

Wellman Furnaces

Wellman Furnaces is a privately held company headquartered in West Midlands, England, the United Kingdom. The company offers tube LPCVD products for doped and undoped oxide applications. The four-stack tube furnaces are capable of 125mm wafer size processing and can be automated with a cantilever loading system. Other related products offered by the company include laminar flow cabinets, crystal zone refiners, diffusion furnaces, gas cabinets, and vacuum ovens.

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CVD Companies

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Chemical Vapor Deposition

INTRODUCTION

The fabrication of an IC device can be divided into three basic operations: films are deposited, the deposited films are patterned, and the film characteristics are altered. Significant advances have been made in the equipment and processes used to pattern the films in such areas as lithography and dry etching. Likewise, developments in the alteration of films, such as ion implantation, have kept pace with the developments in the patterning area. Today's lithography, dry etch, and ion implantation equipment is capable of fabricating the submicron geometries that will be required in the 1990s.

However, in the deposition area, which includes physical vapor deposition (PVD) and chemical vapor deposition (CVD), films are deposited today in much the same way that they have been for years. Whereas, in the past, deposited thin films accounted for only a few layers per finished wafer, today they make up at least half of the masking layers. Thus, thin-film deposition technology has become extremely important for today's devices. What advances have been made in deposition have been the result of attempts by the manufacturers to adapt their equipment to meet the needs of VLSI fabrication. Therefore, attention is now turning to this area as the limits of PVD metal deposition are reached and as the need increases for higher-quality dielectrics and for dielectrics with different properties. While we have the patterning technology to carry us into submicron devices, deposition technology has not kept pace, and, consequently, this is an area of substantial opportunity. This section focuses on this opportunity for developing new approaches and equipment in CVD deposition.

This section of the notebook discusses the current CVD technologies and trends in detail. Another section of the notebook has a similar discussion of PVD technologies. The discussion of CVD is organized into the following major topics:

- Atmospheric pressure CVD (APCVD)
- Low pressure CVD (LPCVD)
- Plasma enhanced CVD (PECVD)
- Photochemical vapor deposition (PCVD)
- Electron cyclotron resonance plasma CVD (ECR CVD)
- Trends in interconnection technology
- Trends in interlayer dielectrics
- Market summary and forecast

Chemical Vapor Deposition

For each of the five CVD technologies listed above there is a discussion of the current equipment available on the market and the equipment trends, the major applications for the technology and the application trends, and the worldwide market for that particular deposition technique. Because the development of CVD equipment is intimately involved with the film requirements of VLSI devices, the next two topics concern interconnection and dielectric trends, including the opportunities for CVD metallization in lieu of PVD deposition. The final topic is a market forecast for CVD equipment.

Before turning to the main discussion, it might be helpful to list the general requirements of VLSI films and the general equipment features that will be necessary in new equipment designs.

Film Requirements

CVD films have four main applications: passivation, interlayer dielectrics, gate interconnection, and metallization. Historically, the semiconductor industry has used CVD techniques for the first three applications and PVD techniques for metallization. However, as the limitations of PVD for metallization for VLSI devices are being reached, new CVD techniques are emerging for this application as well. Besides the new applications for CVD, the existing applications will require higher-quality films. While each of the applications has its own specific requirements, the following general film properties are needed.

- Film thickness uniformity--Film thickness has to be uniform across a wafer, from wafer to wafer, and from run to run. Today's uniformities range from 3 percent to 6 percent, and it is anticipated that 2 percent uniformity will be required. For instance, a 5 percent thickness uniformity coupled with a 5 percent etch uniformity could result in a total variation of 20 percent in etch time to clear all the wafers in a batch etcher. This would result in unacceptable overetching of the wafers in the batch that cleared earlier.

- Coating conformality--All steps and contact holes should be 100 percent conformally covered. This means that the film thickness on the vertical walls is the same as on the horizontal surfaces.

- Pinholes--Pinholes must be kept to a minimum, as they cause localized damage in the substrate beneath the pinhole.

- Particles--Particles caused either by the deposition process or by the equipment must be as low as possible and stringently controlled.

- Film stress--Films deposited with tensile stress may crack, and films deposited with too high a compressive stress may lift off. The deposition process must be chosen to give the proper stress characteristic. For instance, films deposited by PECVD techniques tend to be in compression while other techniques give films in tension.

- Planarization--It may be desirable in some cases to planarize the surface of films to provide for the conformal coverage of the subsequent film and to facilitate fine-line lithography.

- Adhesion--The film should adhere well to the substrate to prevent film lift-off.

- Stoichiometry--Films should be stoichiometric. For instance, silicon nitride films deposited by PECVD contain relatively large amounts of hydrogen in addition to silicon and nitrogen. Hydrogen is undesirable because subsequent processing steps can cause the hydrogen to evolve from the film, creating pinholes.

- Radiation damage--In the case of PECVD, as the film is deposited, it is subjected to ion and photon bombardment and under certain conditions this radiation can alter the device characteristics.

CVD Equipment Requirements

It is unlikely that any one CVD technology will satisfy all the applications and requirements for CVD films. More likely, APCVD, LPCVD, PECVD, and the other technologies will each have applications for which they are best suited. However, no matter what the technology used to deposit the film, the equipment designs must have the following characteristics:

- Fully automatic operation with self-monitoring and closed-loop control

- Cassette-to-cassette operation

- Ability to be interfaced to a factory automation system (both hardware and software compatibility)

- High throughput

- Low particulate contribution that can be measured and guaranteed by the manufacturer

- High reliability: mean time between failures (MTBF)--1,000 hours; mean time to repair (MTTR)--1 hour; mean time between assists (MTBA)--500 hours; mean time to assist (MTTA)--a few minutes
- Guaranteed uptime of 95 percent or greater
- Limited scheduled downtime for preventive maintenance
- Low use of floor space (footprint): some equipment is designed for through-the-wall installation to give a zero footprint. This may or may not be desirable, depending on the design of the fab
- Low power and utilities consumption
- Minimum load on the clean room HVAC system
- Efficient use of process gases
- Quick turnaround: a fairly recent need in the United States is for equipment to have the ability to process a wafer lot quickly but not necessarily to have a high capacity. This is particularly needed by the custom IC houses

ATMOSPHERIC PRESSURE CVD

Atmospheric pressure CVD (APCVD) films have been used since the early days of the semiconductor industry, and this method is, historically, the oldest of the CVD techniques in use today. The advantage of APCVD is its high throughput. However, as the LPCVD and PECVD technologies were developed, the use of APCVD declined because of the higher-quality films deposited by these newer processes. APCVD equipment is used today to deposit doped or undoped oxide films for final passivation and interlayer dielectric applications.

Equipment Configurations

In APCVD equipment, the chemical reaction between the reactant gases and the wafer surface is thermally drive. The deposition takes place on a heated wafer surface, typically in the range of 350 to 450 degrees C. Because the walls of the reactor are not heated, APCVD reactors are sometimes called "cold wall" reactors in contrast to LPCVD and PECVD "hot wall" reactors. Film deposition takes place at atmospheric pressures (760 torr), in contrast to the low-pressure (less than 1 torr) LPCVD and PECVD processes.

Chemical Vapor Deposition

APCVD equipment is of two general types: the continuous-belt, open-reactor design and the closed-reactor, batch design. Batch systems for oxide deposition were offered as early as 1968 by Applied Materials, which also introduced the industry's first continuous-belt reactor in 1973. In 1978, Applied introduced an upgraded belt version, the AMS 2100, which is still offered.

In both the Applied Materials AMS 2100 (Figure 1) and the Watkins-Johnson WJ-985 (Figure 2) systems, the wafers are transported on endless belts into a reactor that is open to the atmosphere. A nitrogen curtain at both the reactor entrance and exit isolates the deposition zone from the outside environment. The wafers are heated from beneath and move continuously through the deposition zone. In the AMS 2100 system (Figure 3), the film is continuously built up as the wafer moves through the deposition zone. The deposition rate is 1,100A per minute. In the WJ-985 reactor, the wafer moves continuously through the reactor, but film growth occurs only under the three sequential deposition heads, or gas injectors (Figure 4), so that the final film thickness is built up with three sequential depositions. Film grows under the deposition heads at a rate of 10,000A per minute. Throughput for belt systems is determined by wafer size and belt speed.

In contrast, the Tempress Pyrox 232 (Figure 5) is a batch system using a reactor chamber closed to the atmosphere and operating at a slightly negative pressure. The wafers are processed inside the chamber on a rotating, horizontal, circular susceptor heated from beneath. Figure 6 shows the susceptor of the Pyrox 232 with the chamber open. A disadvantage of batch systems is that they are manually loaded, since the design does not easily lend itself to automation. Throughput for batch systems is determined by susceptor diameter, wafer size, and the number of batches that can be processed per hour.

The Vapox 5000, manufactured by Pacific Western Systems, uses a different approach to the continuous-belt design. In this system, the wafers are loaded onto an 11 x 21-inch plate and the plate makes one or more passes under the same gas injector head. The deposition rate under the injector head is 1,200A per minute, so the final film thickness is determined by the speed of the plate under the head and by the number of passes. The Vapox 5000 was marketed for a while by Applied Materials, but Pacific Western now markets the product itself.

In addition to the four U.S. manufacturers just cited, two Japanese companies, Amaya Manufacturing and Hitachi, manufacture similar APCVD equipment. However, the Japanese equipment is not available in the United States. Table 1 lists the major worldwide APCVD manufacturers by reactor design.

Figure 1

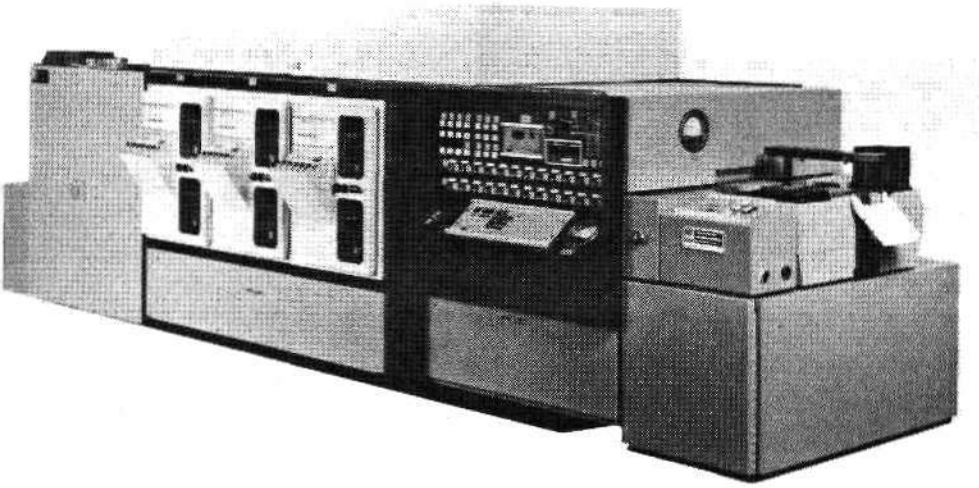
APPLIED MATERIALS AMS-2100 REACTOR

Source: Applied Materials

 © 1985 Dataquest Incorporated Sept. 26 ed.

Figure 2

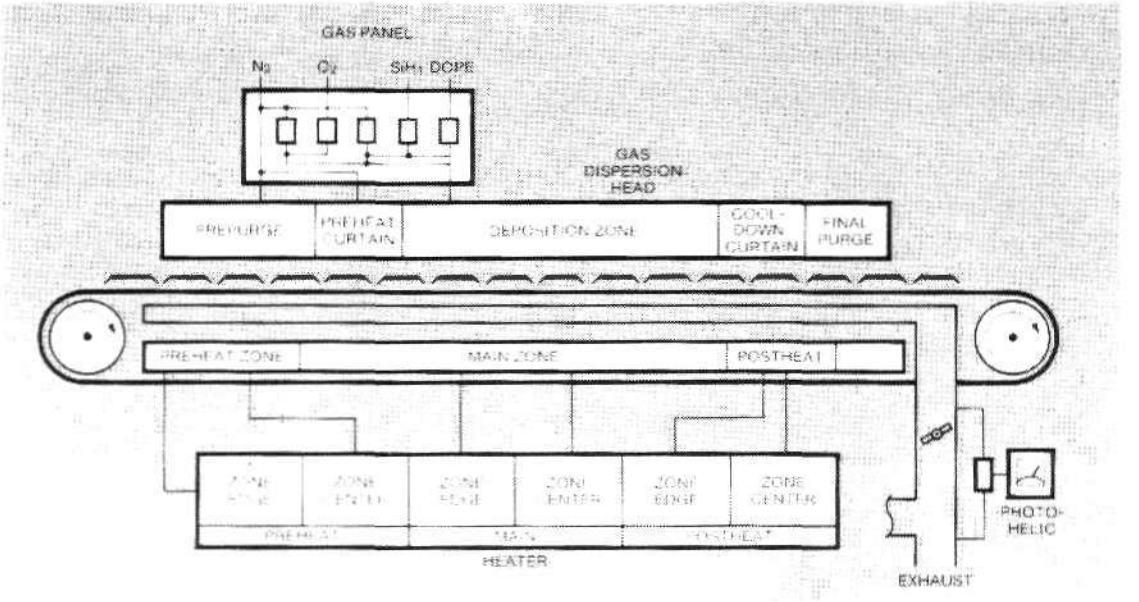
WATKINS-JOHNSON WJ-985 REACTOR



Source: Watkins-Johnson

Figure 3

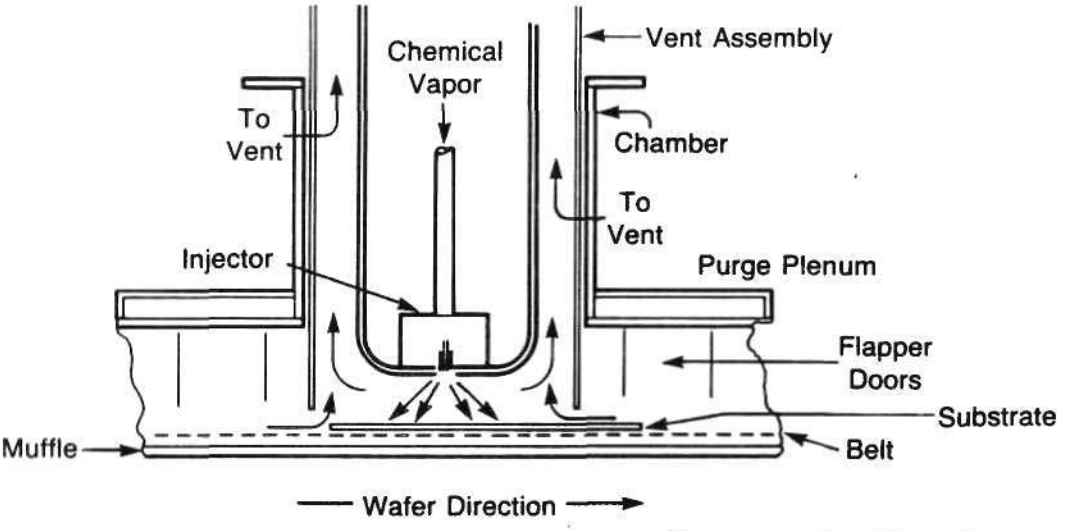
APPLIED MATERIALS AMS-2100 REACTOR DESIGN



Source: Applied Materials

Figure 4

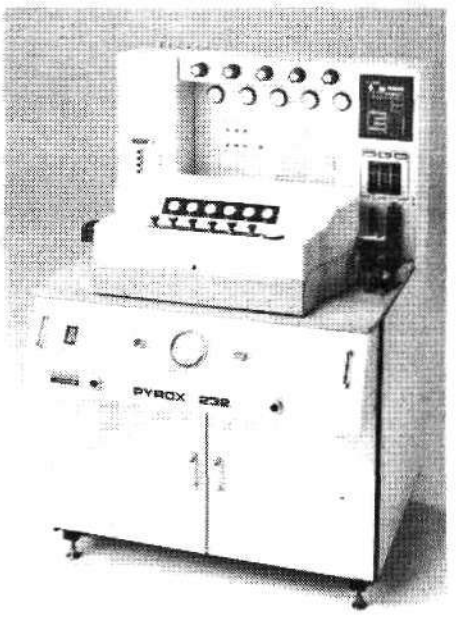
WATKINS-JOHNSON WJ-985 DEPOSITION HEAD



Source: Watkins-Johnson

Figure 5

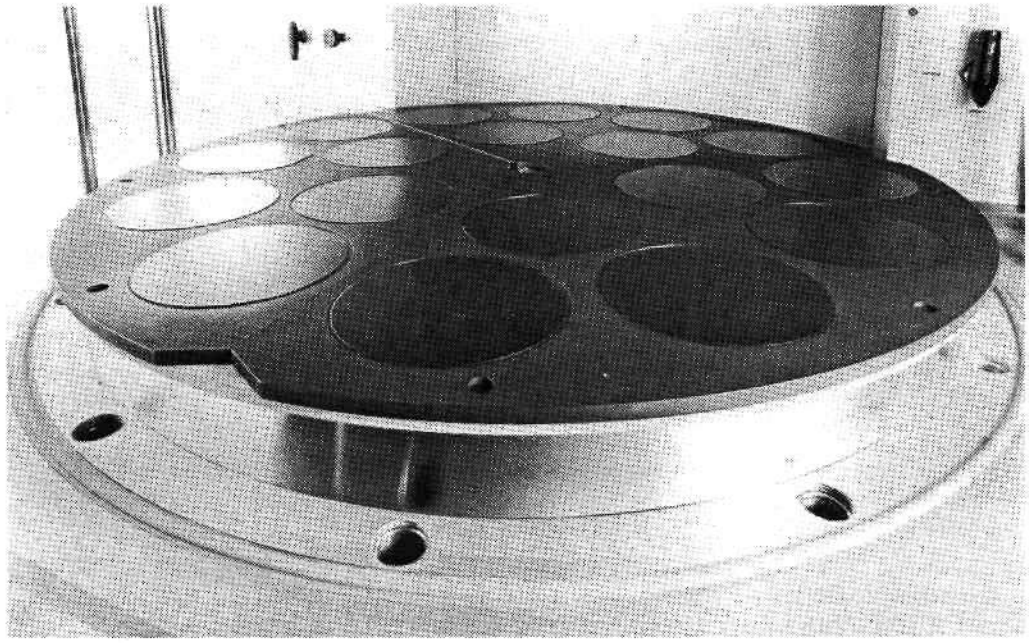
TEMPRESS PYROX 232 REACTOR



Source: Tempress

Figure 6

TEMPRESS PYROX 232 REACTOR CHAMBER



Source: Tempress

Table 1

WORLDWIDE APCVD EQUIPMENT MANUFACTURERS

Company	Model	Reactor Design	Price ($K)
United States			
Applied Materials	AMS 2100	Continuous Belt	$186
Pacific Western Systems	Vapox 5000	Modified Belt	$ 40
Tempress	Pyrox 232	Horizontal Susceptor	$160
Watkins-Johnson	WJ-985	Continuous Belt	$350
Japan			
Amaya Mfg. Works	-	Continuous Belt	$200
Hitachi	CVD 500	Horizontal Susceptor	$150

Source: DATAQUEST

Chemical Vapor Deposition

Atmospheric reactors have been used in the semiconductor industry for many years, but there has been relatively little technological change in the equipment during that time compared with other areas of wafer fabrication equipment such as lithography, dry etch, or ion implantation. For instance, the Applied Materials AMS 2100 has been in production since 1978. The Tempress Pyrox 232, the newest of the U.S. reactors, was introduced in 1982. In Japan, where APCVD plays a larger role in semiconductor manufacturing than in the United States, Hitachi, in early 1984, introduced its CVD 500. This reactor is a batch system similar to the Pyrox 232 but with automatic wafer load/unload capability.

Applications

APCVD reactors are used predominantly to deposit doped (PSG or BPSG) and undoped oxide films for either final passivation or for an interlayer dielectric. APCVD films are deposited at low temperatures and have low stress (hence, more resistance to cracking) and low pinhole counts. Throughput of APCVD reactors is high. For instance, throughputs of 90 to 108 wafers per hour are obtained for 100mm wafers. The main disadvantages of APCVD films have been the relatively poorer conformal step coverage, poorer uniformity, higher particulate count, and rougher surface compared with LPCVD and PECVD reactors. However, APCVD manufacturers are making improvements in these areas and they are now claiming that better step coverage, lower particulate count, and better uniformities are being obtained. Historically, it was the disadvantages of APCVD films that were primarily responsible for the shift from APCVD reactors to LPCVD and PECVD reactors for depositing low-temperature doped/undoped oxides and the consequent slowdown and stagnancy of the APCVD market.

Another factor that contributed to the lack of growth of the APCVD market was the development of PECVD technology for depositing silicon nitride at low enough temperatures so that it could be used as a passivation layer over aluminum. Previously, PSG (phosphosilicate glass) was used as a passivation layer, but because PSG is hygroscopic, it can cause aluminum corrosion problems in plastic packages.

Market Analysis

Worldwide market demand for APCVD equipment is shown in Table 2. Note that U.S. demand was flat from 1982 to 1983; it was also flat for several years before 1982. This stagnant market reflects the shift from PSG to silicon nitride for passivation and the shift from APCVD-doped/undoped oxides to LPCVD-doped/undoped oxides. U.S. demand increased in 1984 and DATAQUEST believes that this was due to the increasing interest in BPSG (borophosphosilicate glass) films for use as interlayer dielectrics. The BPSG application is discussed in more detail later in this section under TRENDS IN INTERLAYER DIELECTRICS.

The Japanese APCVD market is larger than the U.S. market and has been growing at respectable rates over the last several years, although the growth rates (shown in Table 3) have been less than the overall Japanese semiconductor equipment growth rates. For instance, Japanese spending on wafer fabrication equipment grew at a 74 percent rate in 1984 while the Japanese APCVD market grew at only a 23 percent rate. The larger Japanese APCVD market reflects their past tendency to use APCVD doped/undoped oxides more for passivation and interlayer dielectrics than U.S. manufacturers, who tend to use PECVD nitride for passivation and LPCVD oxides for interlayer dielectrics. It should be noted, however, that the Japanese appear to be using nitride passivation more and more.

Table 4 shows estimated 1984 market share data for the major APCVD manufacturers. Note that the belt reactors (Amaya, Applied Materials, Watkins-Johnson, and Pacific Western) accounted for 71 percent of sales. However, the new Hitachi CVD 500, a batch reactor, should increase its market share in 1985. The U.S. manufacturers have 59 percent ($19 M) of the world market, and of that share, approximately one-third is exported to Japan.

Table 2

WORLDWIDE APCVD EQUIPMENT MARKET DEMAND
(Millions of Dollars)

	1982		1983		1984	
	Sales	Share	Sales	Share	Sales	Share
United States	$ 8.6	38%	$ 8.8	34%	$11.1	34%
Japan	13.3	59	16.3	62	20.0	62
ROW	0.8	3	1.0	4	1.3	4
Total	$22.7	100%	$26.1	100%	$32.4	100%

Source: DATAQUEST

Table 3

WORLDWIDE APCVD EQUIPMENT MARKET GROWTH
(Millions of Dollars)

	1983		1984	
	Sales	Growth	Sales	Growth
United States	$ 8.8	2%	$11.1	26%
Japan	16.3	23%	20.0	23%
ROW	1.0	25%	1.3	30%
Total	$26.1	15%	$32.4	24%

Table 4

WORLDWIDE APCVD EQUIPMENT MARKET SHARE--1984
(Millions of Dollars)

Company	Sales	Share
Amaya	$10.0	31%
Tempress	6.0	19
Watkins-Johnson	6.0	19
Applied Materials	5.6	17
Hitachi	3.0	9
Pacific Western	1.4	4
Others	0.4	1
Total	$32.4	100%

Source: DATAQUEST

LOW PRESSURE CHEMICAL VAPOR DEPOSITION

Of the three CVD techniques, there is currently more activity in low pressure CVD (LPCVD) than in any other area. The reason for this is that the horizontal furnaces, which have been the workhorses for LPCVD films, are reaching the limits of their present designs and new approaches are required to meet the needs of VLSI fabrication. New designs are now being introduced into the marketplace and new companies are entering the LPCVD market with new approaches to the problem of repeatedly depositing a uniform, defect-free film.

Table 5 lists the major worldwide manufacturers of LPCVD equipment. Other manufacturers, not listed, provide custom LPCVD systems for special applications. In addition, there have been several recent start-ups including Focus Semiconductor, Novellus Systems, and Rome-Union. Because of the opportunities in this market, we could see more start-ups.

Table 5

WORLDWIDE LPCVD EQUIPMENT MANUFACTURERS

Company	Location	Design
Advanced Crystal Sciences	U.S.	Horizontal/Retrofit kits
Advanced Semiconductor Materials	U.S./Holland	Horizontal
Anicon	U.S.	Nontube
BTU Engineering	U.S.	Horizontal
Centrotherm	West Germany	Horizontal
Denko	Japan	Vertical
Genus	U.S.	Nontube
Kokusai Electric	Japan	Horizontal
Pacific Western	U.S.	Horizontal/Retrofit kits
Process Technology	Canada	Retrofit kits
Semy Engineering	France	Horizontal
Helmut Seier	Switzerland	Vertical
Tempress	U.S.	Horizontal/Vertical
Thermco	U.S.	Horizontal
TEL/Thermco	Japan	Horizontal
Tylan	U.S.	Horizontal
Wellman Furnaces	England	Horizontal
Koyo Lindberg	Japan	Horizontal/Vertical

Source: DATAQUEST

Chemical Vapor Deposition

Equipment Configurations

LPCVD equipment is of three designs: the horizontal tube reactor, the non-tube reactor, and the vertical tube reactor. Historically, the horizontal tube reactor is the oldest of the three techniques, developed in the mid-1970s to deposit polysilicon on large batches of wafers. It was designed to fit into the bore of horizontal tube diffusion furnaces, which were in widespread use in the semiconductor industry at the time. The development of horizontal tube LPCVD reactors paralleled the development of the parallel plate PECVD reactor. Non-tube LPCVD reactors are recent technologies, having only appeared in the last few years. Vertical tube LPCVD reactors are designed for use in vertical tube diffusion furnaces. While vertical tube furnaces are not a new idea, their use in the semiconductor industry is very recent and they are just now being introduced into the marketplace. Vertical tube LPCVD is the newest of all the CVD techniques commercially available.

In all of the three types of LPCVD reactors, the reaction is thermally driven, that is, the reactant gases chemically react on a heated wafer surface to form the film. The major factors that determine film growth and quality are wafer temperature, pressure, concentration of reactant gases, and the flow characteristics of the gases over the wafer surface. Flow characteristics are determined by the design of the reactor. Although some films can be deposited at relatively low temperatures, other films require much higher temperatures. For example, LPCVD deposition of silicon nitride requires temperatures in the range of 750 to 850 degrees C in order to drive the reaction. By contrast, in PECVD, the plasma dissociates the gases into highly reactive free radicals that react on the wafer surface to form the film. This reaction is relatively temperature insensitive so that nitride deposition can take place at temperatures of below 400 degrees C. Pressure in LPCVD reactors is generally maintained at between 250 to 1,000 mtorr.

Horizontal Tube Reactor

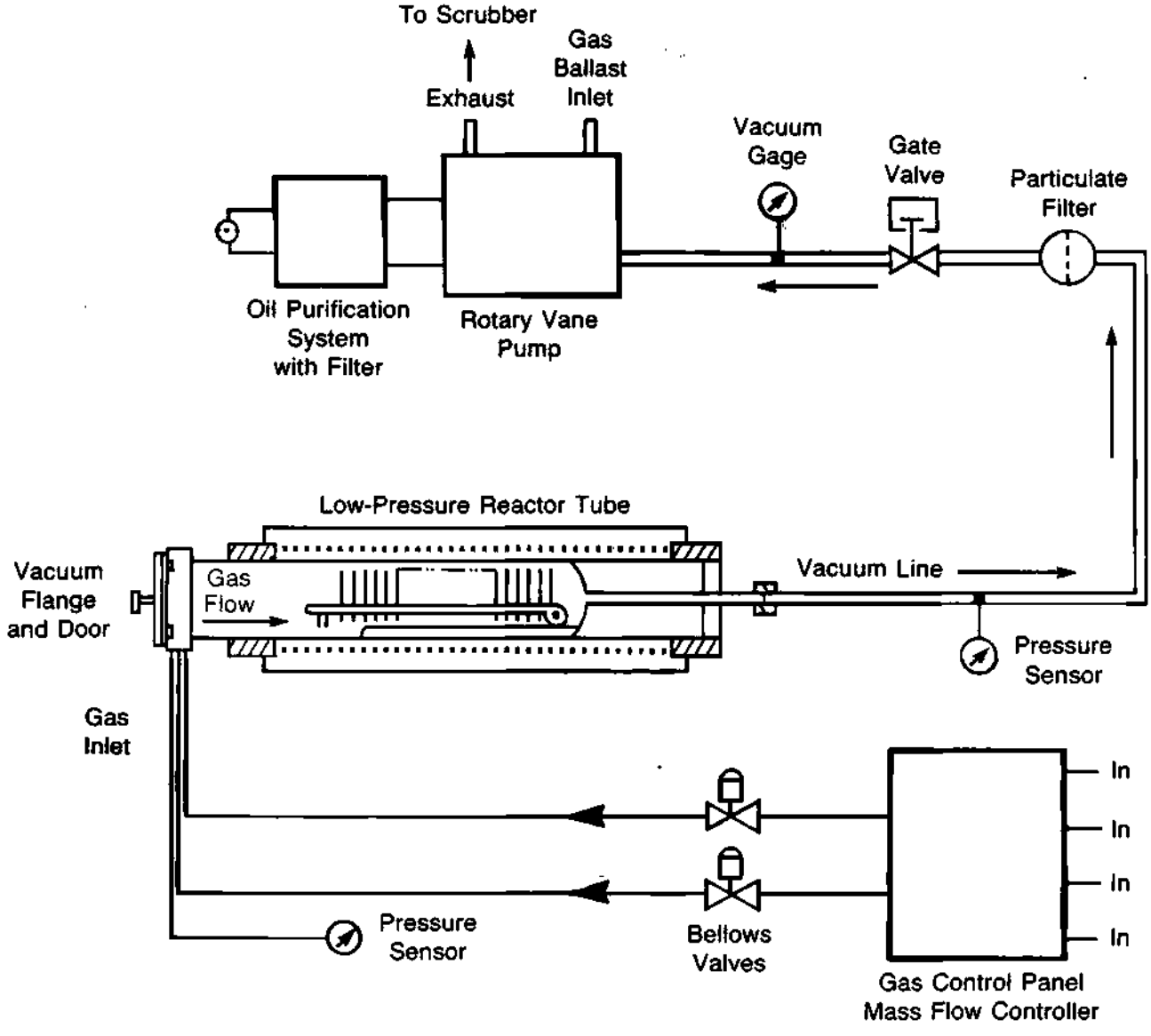
The main advantage of the horizontal tube reactor is its ability to economically deposit uniform and conformal films on large batches of wafers, typically 100 to 150 wafers per load.

Figure 7 shows a schematic of an LPCVD system. Basically, it consists of a quartz tube that is inserted into the bore of a diffusion furnace. The rear end of the tube is connected to the vacuum system and the front end is sealed with a vacuum flange and door. A quartz carrier, which is used to hold the wafers in a vertical position, is inserted into the tube. The wafers are heated by the diffusion furnace's three-zone resistance heater surrounding the quartz tube. Because the walls of the quartz tube heat up, this is also called a "hot wall" reactor.

Chemical Vapor Deposition

Figure 7

SCHEMATIC OF AN LPCVD SYSTEM



Source: Tylan Corporation

Process gases enter the tube through the sealed front door and diffuse toward the rear of the tube. As the gases suffer from depletion effects as they flow down the tube, the temperature profile increases down the length of the tube to offset the gas depletion effects and to maintain a uniform deposition rate. Because this is a thermally driven process, chemical reaction or film deposition will occur not only on the heated wafer surface but also on the walls of the quartz tube and any other heated surface in the tube, including the quartz wafer boat. Thus, a thick film will build up on the quartz walls and other surfaces after a series of deposition runs.

The film can flake off and cause particulate contamination on the wafers, so the quartz tube has to be periodically removed from the system for cleaning (typically every 10 to 20 runs). Also, the quartzware for holding the wafers has to be changed at even more frequent intervals. Another source of contamination is gas phase nucleation. Because of these sources of contamination, particulate control is the single biggest problem in horizontal tube reactors.

The LPCVD technique requires a furnace system capable of good temperature control similar to the diffusion technology requirements. When ordering several diffusion furnaces, a semiconductor manufacturer will specify for all of the tubes ordered how many will be dedicated to LPCVD and how many to diffusion or other processes. Typically, between 20 to 25 percent of all of the tubes ordered will be LPCVD tubes. These tubes would be divided up among the diffusion furnaces such that a four-stack furnace for LPCVD processes would typically have from two to four LPCVD tubes. It should be noted that developments in LPCVD processes are intimately connected with developments in diffusion furnaces, which are discussed in another section of the notebook in more detail. The following paragraphs discuss some of the major features and trends of today's horizontal tube LPCVD/diffusion furnace systems.

The boat load/unload station is provided either with horizontal or vertical laminar flow or a nitrogen purge to reduce particulates in the load area. The quartz wafer boats are manually placed on a quartz carrier, which is inserted into the process tube by an automatic loader. Each tube is processed independently and all process parameters such as temperature, profile, gas flows, process time, carrier insertion speed and position, and, in some cases, pressure are automatically controlled by a microprocessor. The operator need only load the wafer boats and initiate the process.

Furnaces are heavy power consumers and so, in order to reduce power consumption, distributed silicon controlled rectifier (SCR) firing has been introduced. Reactor pressure in an LPCVD tube will vary somewhat during the deposition cycle and from run to run. Because deposition rate varies with pressure, the result is that uniformity of the film suffers

from run to run. Pressure has not usually been controlled in tube reactors, but as the need for more uniform films increases, manufacturers are incorporating automatic, closed-looped pressure control in the system.

Withdrawing the quartz tube for periodic cleaning creates particulates in the clean room when the tube is withdrawn into the load/unload station. Newer designs have flangeless tubes that can be withdrawn through tne rear of the furnace directly into the chase area. An even better solution is to clean the tubes in situ with a plasma process; such a system was introduced by Benzing Technologies at Semicon West 1984. The Benzing system, priced at $98,000, uses a laser to guide the plasma electrodes into the furnace tube, where a plasma is struck with NH_3 gas. Benzing claims that total downtime per tube is one hour. If this is indeed the case, then this is a considerable improvement over the 8 or more hours previously required to do the job.

The quartz tubes are automatically loaded, but they previously rode on wheels, which created particulates, since they contacted the floor of the tube. To overcome the particulate problem, manufacturers have introduced soft-contact loading and cantilever loading. In soft-contact loading, the wafer boats are carried into the tube by an automatic loader without touching the walls of the tube and then gently lowered into position. The loader then withdraws from the tube before the process begins. Although this is a definite improvement over the previous method, the drawback to soft-contact loading is that the wafer boats still make contact with the tube at a few points, and during the deposition cycle, a minute bond is formed at the points of contact. When the boats are raised by the soft contact loader, the bond is broken and particulates are created.

In the cantilever approach, the boats are carried into the tube on quartz-sheathed ceramic supports (or a silicon carbide paddle for temperatures greater than the 1,150 degrees C encountered in diffusion processes). The cantilever remains in the tube during the deposition cycle and, because there is no contact with the walls of the tube, particulate formation is reduced even further.

Soft-contact loaders are mechanically more complex because they have the additional motion of raising and lowering the boats. Soft-contact loaders, because they withdraw from the tube, are more suitable for retrofit or for furnace designs that have a smaller-diameter quartz tube. Cantilever supports must be relatively massive to support the wafer load and, because they are positioned off the floor of the tube for good gas flow dynamics, larger-diameter tubes are required. New furnaces are being designed with larger tubes to accommodate cantilever loading. DATAQUEST believes that cantilevers will be the dominant approach in new equipment and soft-contact loading will be used for retrofit and in older furnace designs.

Another new feature is the three-axis elevator, which is installed at the load station to automatically position the wafer boats at any tube level and then place the boats on the cantilever or soft-contact loader. Previously, an operator had to manually transfer the wafers from the plastic cassettes to the quartz wafer boats and then manually place the boats on the elevator. However, manufacturers are now introducing fully automatic load/unload using robotics for cassette-to-cassette operation.

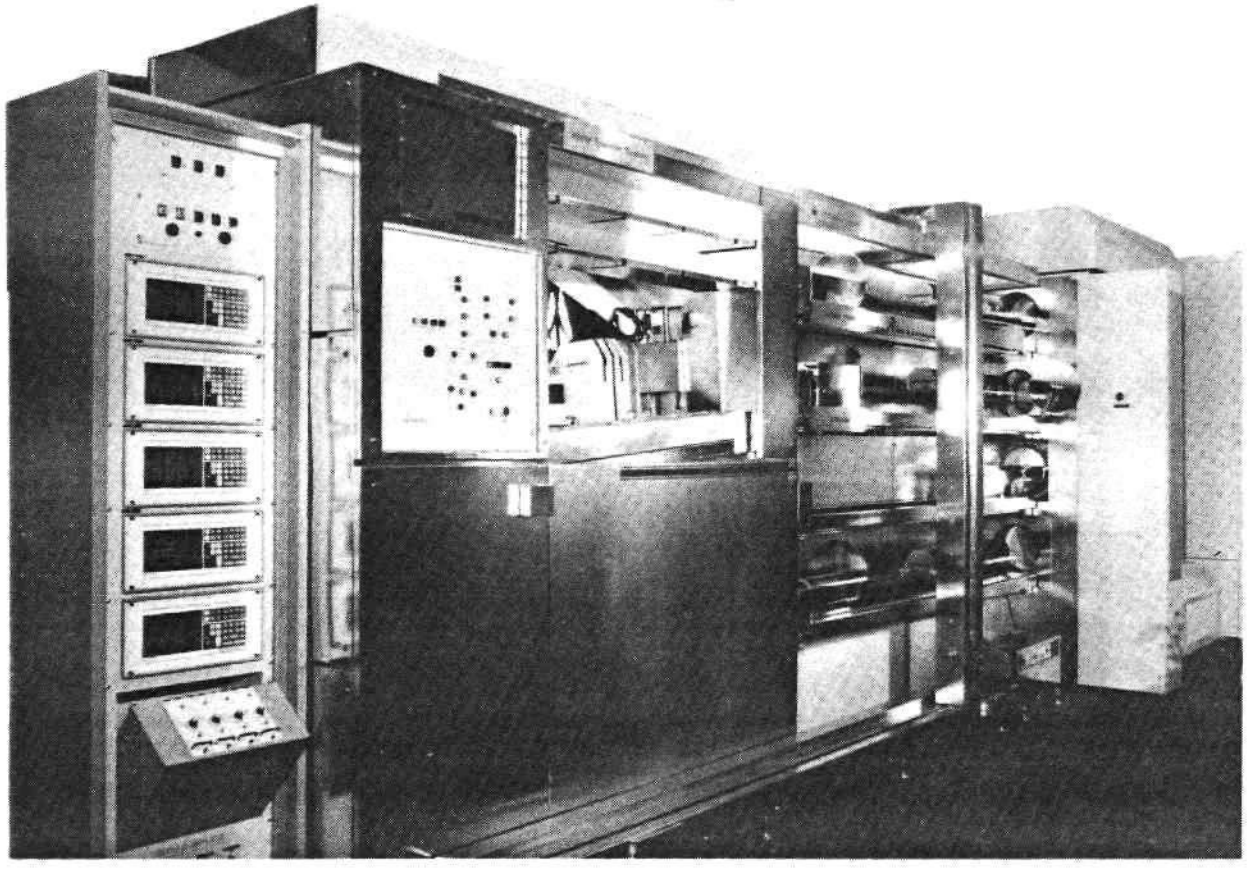
Figure 8 shows the cassette-to-cassette diffusion furnace manufactured by BTU Engineering Corp. Note the robot manufactured by Precision Robots, Inc. used for transferring the wafers between the plastic cassette and the quartz boats. BTU Engineering has been selling its diffusion furnaces for some time, but the LPCVD option has been available only since 1982. Most of the manufacturers listed in Table 5 provide both LPCVD systems and also LPCVD retrofit kits for use in their own or other manufacturers' furnaces. In addition, several non-furnace companies provide LPCVD retrofit kits for use in the leading manufacturers' diffusion furnaces. An LPCVD retrofit kit consists of the quartz tube with cantilever or soft-contact loader, a vacuum system, a gas system, and all the hardware and plumbing required. Until recently, Advanced Crystal Sciences only provided retrofit kits for LPCVD and diffusion. However, in late 1984, the company introduced its own four-stack furnace. First shipments will be in 1985. Pacific Western Systems (PWS) will provide LPCVD, PECVD, or diffusion retrofit kits for installation in any combination in a standard four-stack furnace. PWS can also provide its own furnace, which was introduced in 1984.

Process Technology Ltd., a new company based in New Brunswick, Canada, offers LPCVD retrofit kits for low-temperature oxide (LTO), polysilicon, silicon nitride, boron nitride, tetraethylorthosilicate (TEOS), selective tungsten, and BPSG (diborane process) and is developing a tungsten silicide process. The company also makes its own quartzware. First shipments were in 1983, and the company is growing rapidly, with most of its sales for the LTO process.

Diffusion furnaces appeared in the semiconductor industry in the early 1960s and the LPCVD capability was added in the late 1970s. Today's LPCVD/diffusion furnace technology has evolved from these early beginnings. It is obvious from the above discussion that this technology is still evolving as the horizontal tube manufacturers attempt to adapt their equipment to meet the demands of VLSI device fabrication.

Figure 8

AUTOMATED DIFFUSION FURNACE



Source: BTU Engineeering Corporation

A good example of this evolution is load/unload automation. We now have robotics to transfer wafers from cassettes to boats, elevator systems to transfer the boats to the loader, and cantilevers to automatically load the boats in the process tube. This complicated system is required because the original design of horizontal furnaces does not easily lend itself to automation. Completely automating a four-stack furnace is extremely expensive and represents a high percentage of the total cost of the system. In addition, horizontal furnaces have a large footprint and consume considerable amounts of power. Because of the inherent limitations in the designs of today's horizontal furnaces, new approaches and technologies are being taken for the deposition of LPCVD films.

Nontube Reactors

LPCVD horizontal tube technology has followed an evolutionary process. In contrast, Anicon and Genus have taken revolutionary approaches to LPCVD deposition. Anicon, incorporated in 1982, shipped its first reactor in late 1983. The Anicon system, shown in Figure 9, is designed around its unique reaction chamber, shown schematically in Figure 10. The reactor consists of an inner quartz chamber and an outer quartz bell jar. The incoming gases are injected through quartz gas injectors just above the wafers. The gases are mixed above the wafers, flow parallel to the wafer surfaces, and are then exhausted just below the wafers. Gas flow from injection to exhaust is less than 8 inches. Thus, each wafer receives the same gas concentration, unlike in a horizontal furnace, where wafers down the length of the tube receive different concentrations because of gas depletion. Because the gases have a short residence time in the chamber, particulate contamination due to gas phase nucleation is reduced.

The deposition chamber is an isothermal chamber such that the wafers, the inner chamber, and the outer chamber are all at the same temperature. Isothermal temperatures mean better film uniformities and more uniform grain size in films such as polysilicon. Because of the design of the isothermal chamber, Anicon will guarantee a particulate reduction of 50 percent over an LPCVD or APCVD process currently being used in the customer's facility.

Film deposition takes place only on the walls of the inner chamber and not on the walls of the outer bell jar. Therefore, only the inner chamber needs to be removed for periodic cleaning. The cycle time for cleaning is 30 minutes, in contrast to 8 hours or more for horizontal furnaces (although the in situ plasma cleaning system recently introduced by Benzing Technologies will reduce the cleaning time for horizontal furnaces).

Figure 9

ANICON LPCVD REACTOR

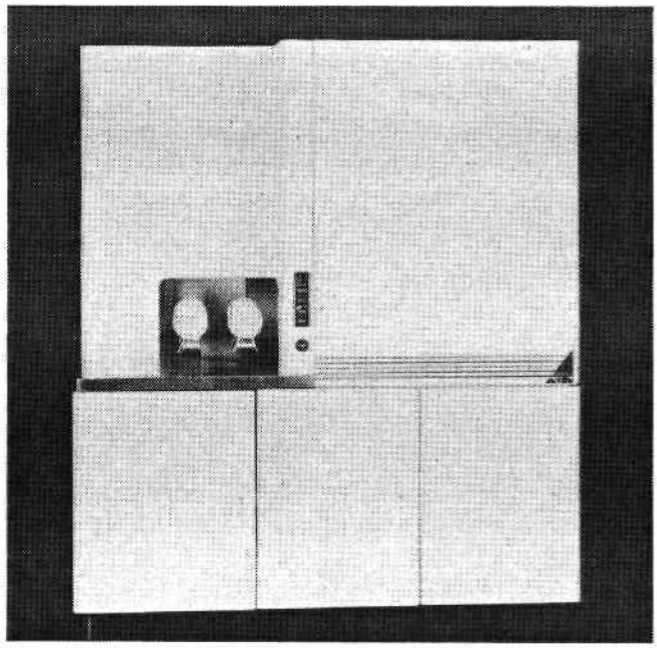
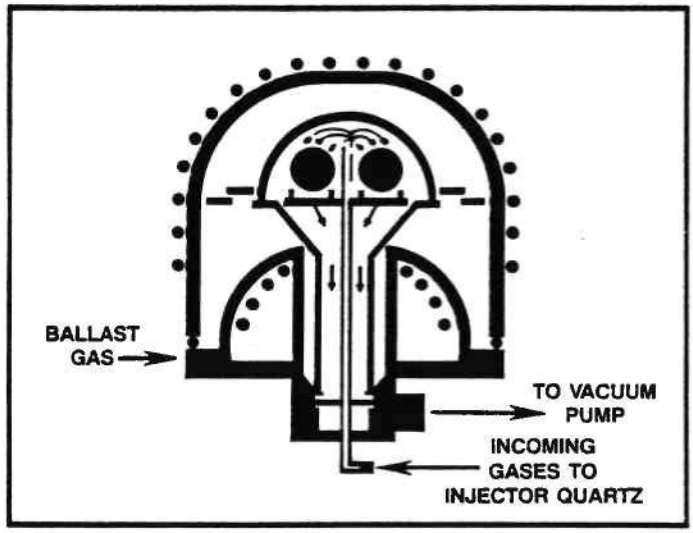


Figure 10

ANICON ISOTHERMAL CHAMBER DESIGN



Source: Anicon

During operation, the inner and outer chambers are automatically raised and two quartz boats containing 50 or 100 wafers, depending on the process, are automatically loaded onto a platform in the inner chamber. All process parameters, including chamber pressure, are automatically controlled. Anicon is currently working on cassette-to-cassette operation using a robot. The unit has a small footprint that can be reduced even further with a through-the-wall configuration. Power consumption in steady-state operation is 15 percent of a horizontal furnace.

Whereas, in a horizontal four-stack furnace, four independent LPCVD processes can be run at the same time, in the Anicon reactor, only one process can be run at a time. Even though the throughput may be higher when the downtime required for tube cleaning is considered, several reactors would be required to replace a horizontal furnace if dedicated processes are desired.

Genus, incorporated in late 1981, has focused on the refractory metal and refractory metal silicide markets. Genus' first product, the model 8301 LPCVD reactor for the deposition of tungsten silicide, was introduced in May 1983 and is shown in Figures 11 and 12. The 8301 is a fully automated cassette-to-cassette cold wall reactor. A robotic wafer handler transfers wafers from metal cassettes into the process chamber through a rectangular slot in the reaction chamber. The wafers are placed in a near vertical position on the face of a revolving turret that can hold up to eight wafers per batch. A uniform reactive gas atmosphere is created by feeding the process gases separately to eight mixing ports equally spaced around the circumference of the chamber. Uniformity of deposition is further enhanced by rotating the wafer turret at 1 rpm. The typical deposition rate is 500A to 1,000A per minute at temperatures in the range of 200 to 500 degrees C at a pressure of 300 mtorr. Throughput is typically 60 wafers per hour.

To prevent film buildup and the resulting particle contamination problems, the outer wall of the chamber is water cooled to near room temperature so that deposition will not take place on the "cold wall." The cold wall configuration also prevents gas phase reactions. The wafers are heated by a bank of quartz lamps located inside the turret housing. The reactor can run an in situ plasma clean step to remove films deposited on any of the inside chamber surfaces.

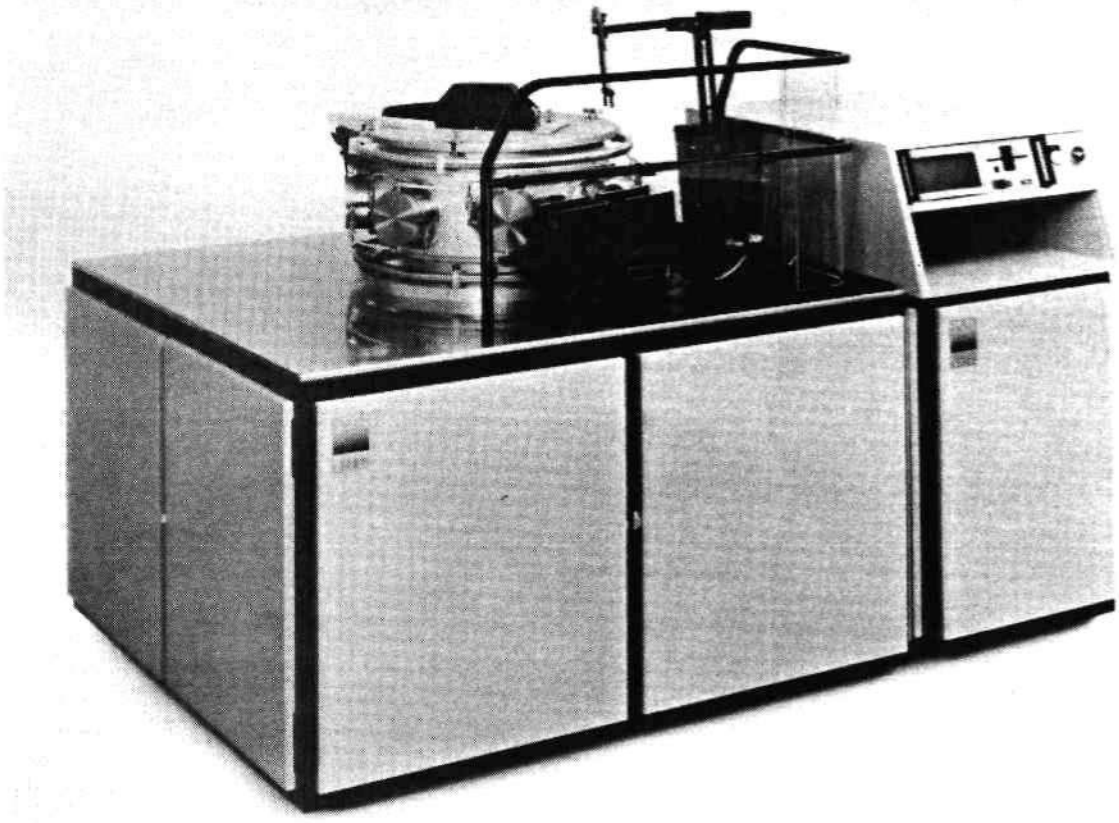
Genus also has available the model 8302 for depositing tungsten and tungsten silicide.

Focus Semiconductor Systems, founded in mid-1984, is developing a nontube reactor for the deposition of LTO, silicon nitride, and polysilicon with uniformities of 2 percent. The reactor will have cassette-to-cassette operation, a small footprint, and through-the-wall installation. First shipments are targeted for early 1986.

Chemical Vapor Deposition

Figure 11

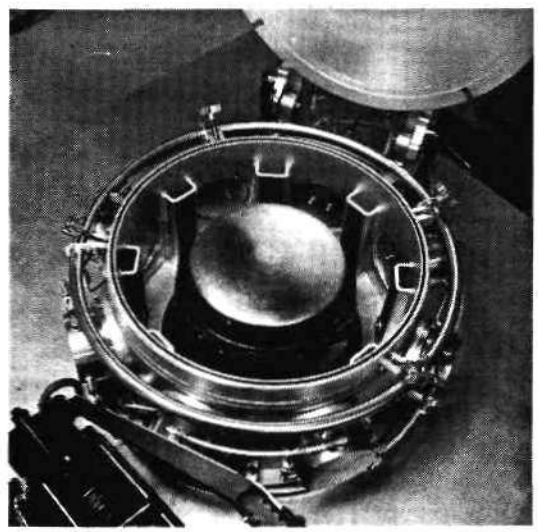
GENUS MODEL 8301



Source: Genus

Figure 12

GENUS 8301 REACTOR CHAMBER



Source: Genus

Vertical Tube Reactor

Another approach to overcoming the limitations of the horizontal furnace has resulted in the development of the vertical furnace. These products are either still under development or just now being introduced into the marketplace. The advantages of vertical furnaces include the ability to handle larger loads of 150mm wafers for today's requirements or 200mm or larger wafer sizes for future VLSI fabrication requirements. (However, it should be noted that larger wafer loads for large-diameter wafers may not be desirable because so many die are at risk should the process go awry.) In conventional horizontal furnaces using cantilever loading, larger wafers and loads pose problems because of the added weight that needs to be supported. In addition, the size of the furnace grows very large because of the larger tubes required and because of other scaling factors. It is unlikely that we will see four-stack horizontal furnaces for processing large wafers.

Vertical furnaces can be mounted in a through-the-wall configuration for a zero footprint in the clean room. They are much easier to automate and, because of efficient thermal design, they have better temperature recovery times and require about half the power of a horizontal furnace. The manufacturers are claiming better particulate control. However, a concern of this technology is that the wafers lie horizontally and, thus, present a larger surface to intercept the particulates that are generated.

A further significant advantage of vertical tube furnaces is that single-lot furnace operations can be done in a small area with a much faster turnaround time. This advantage should be of particular interest to the custom IC houses.

Tempress introduced its vertical furnace in May 1985, and it is interesting to note that it is the first of the horizontal furnace manufacturers to take a new approach. The model 2000, shown in Figure 13, features bottom-up loading to minimize heat loss during load/unload operations to enhance thermal recovery time. Wafers are loaded onto a vertical elevator that carries the wafers up into the quartz tube. Currently, both cassette-to-cassette operation and an LPCVD capability are under development.

Figure 13

TEMPRESS VERTICAL TUBE FURNACE

Source: Tempress

Helmut Seier, of Switzerland, also has a vertical furnace, which has been available in the United States for less than two years. Seier's furnace is top loaded and can handle 150 wafers per load for nitride, polysilicon, and TEOS processes. The wafers are placed with the active side down to minimize particulate contamination and are rotated about the vertical axis during deposition to enhance uniformity. Figure 14 shows two furnace modules served by an automatic loader between them. Denko, a Japanese company, has also recently introduced a vertical furnace. Koyo Lindberg, a joint venture between Koyo (Japan) and Lindberg, a unit of General Signal, manufactures a vertical furnace based on the vertical furnace design of Tempress, another General Signal unit. Koyo Lindberg also manufactures diffusion furnaces and LPCVD systems using some Tempress components and markets Tempress APCVD systems in Japan. Besides these companies, Silicon Valley Group has a vertical furnace under development.

Figure 14

HELMUT SEIER VERTICAL DIFFUSION FURNACE

Source: Disco-Seier

Chemical Vapor Deposition

Applications

LPCVD is used to deposit silicon nitride, high-temperature oxide, low-temperature oxide, polysilicon, TEOS, tungsten, tungsten silicide, and other films as well. The first four films made up 95 percent of the films deposited by LPCVD processes; some of the applications for these films are discussed below. The remaining films are just now beginning to be deposited as these films are required more and more in VLSI device fabrication.

Silicon Nitride

LPCVD silicon nitride is used primarily as an oxidation mask when growing the field oxide to separate the active device areas. LPCVD nitride is deposited at high temperatures (800 degrees C) to provide a dense film as required for the field oxidation step. Typical film thickness is 1,500A to 1,750A. PECVD nitride is deposited at lower temperatures (less than 400 degrees C), and because it is not as dense, it cannot be used for this application.

High-Temperature Oxide (HTO)

The main application for HTO, which is deposited at a temperature of 800 degrees C, has been its use as an etch mask for silicon nitride. At the very start of the wafer fabrication process, a thin layer of oxide (600A), called the stress-relief oxide, is grown on the bare silicon wafer. Then, a thin layer of high-temperature CVD silicon nitride is deposited as described above. Over this is deposited a 1,000A layer of HTO to be used as the nitride etch mask. After the nitride is etched, the field oxide is formed. However, this application for HTO is diminishing and is not now an important process, since the development of dry etch techniques has allowed the use of photoresists for the nitride etch mask.

Low-Temperature Oxide (LTO)

LTO is deposited at a temperature of 420 degrees C. Because of the low deposition temperature, one of the major uses of LTO films is as a passivation layer over aluminum. Interlayer dielectrics are another major use of LTO films. The LTO films can be deposited undoped or doped in situ with phosphorous or boron. Phosphorous-doped LTO, which is PSG, has been in widespread use as a passivation layer and as a reflow glass for interlayer dielectrics. BPSG, another reflow glass, results from both phosphorous and boron doping and is increasingly being used in wafer fabrication. Because of the importance of PSG and BPSG films, they are discussed in more detail later in this section under TRENDS IN INTERLAYER DIELECTRICS.

Chemical Vapor Deposition

Polysilicon

LPCVD has been the predominant technique for the deposition of polysilicon as a gate interconnect. The polysilicon film can be deposited undoped or doped in situ. If deposited undoped, it is later doped with $POCl_3$ in a diffusion furnace or doped with ion implantation.

During the deposition of polysilicon, gas depletion occurs down the LPCVD tube from inlet to exhaust. To compensate for this, the temperature profile is increased to provide a uniform deposition rate for all the wafers regardless of location. The temperature could be 620 degrees C on the inlet and 650 degrees C at the rear end of the tube. As average grain size and other polysilicon film properties vary with temperature, this 30-degree range causes undesirable changes in the film properties, particularly for VLSI devices. This has led to the development of a flat-temperature-profile polysilicon process in which the temperature of all the wafers is the same. To overcome gas depletion effects and maintain a uniform deposition rate, the reactant gas is injected at both ends of the tube. Although the equipment manufacturers offer both polysilicon processes, the semiconductor manufacturers are shifting toward the flat polysilicon process.

Table 6 lists some typical deposition parameters for LPCVD processes.

Table 6

TYPICAL DEPOSITION PARAMETERS FOR LPCVD FILMS DEPOSITED IN HORIZONTAL TUBE REACTORS

	Deposition Temperature (°C)	Deposition Rate (A/Min)	125mm Wafers per Load
Polysilicon	620-650	100	100
Polysilicon (Flat)	630	70-120	100
LTO	400-430	90-400	80-100
HTO	850-950	100	100
Silicon Nitride	750-850	40-60	150
TEOS	690-730	120-150	100
Tungsten	280-425	40-60	-

Source: DATAQUEST

Market Analysis

Table 7 shows the worldwide LPCVD equipment market demand by region for the last three years. Total 1984 worldwide sales totaled $141.5 million, of which, $75.3 million (53 percent) was sold in the United States, $47.5 million (34 percent) was sold in Japan, and $18.7 million (13 percent) was sold in the ROW region, which is mostly Europe. It is interesting to note that the percentage of LPCVD equipment sales in each region for 1984 parallels within a few points the percentage of worldwide semiconductor production in each region. For instance, in 1984, the United States accounted for 52 percent of worldwide semiconductor production, Japan accounted for 38 percent, and the ROW area produced 10 percent.

Table 7

WORLDWIDE LPCVD EQUIPMENT MARKET DEMAND
(Millions of Dollars)

	1982		1983		1984	
	Sales	Share	Sales	Share	Sales	Share
United States	$23.9	47%	$37.6	49%	$ 75.3	53%
Japan	19.7	39	28.9	38	47.5	34
ROW	7.0	14	9.9	13	18.7	13
Total	$50.6	100%	$76.4	100%	$141.5	100%

Source: DATAQUEST

Table 8 shows LPCVD equipment sales growth by region for the last two years. Note that 1984 growth was a hefty 85 percent worldwide and that U.S. growth was even higher at 100 percent. There are several reasons for this exceptional growth. The main reason was the increased capital spending by both the U.S. and Japanese semiconductor companies. U.S. companies doubled their capital expenditures from a 1983 level of $1,425 million to $2,916 million in 1984. The Japanese increased their spending from $1,902 to $3,278 million for a 72 percent increase for the same period.

Table 8

WORLDWIDE LPCVD EQUIPMENT MARKET GROWTH
(Millions of Dollars)

	1983		1984	
	Sales	Growth	Sales	Growth
United States	$37.6	57%	$ 75.3	100%
Japan	28.9	47%	47.5	64%
ROW	9.9	41%	18.7	89%
Total	$76.4	51%	$141.5	85%

Source: DATAQUEST

Another factor is the impact of the Genus tungsten/tungsten silicide LPCVD reactor. Before the advent of this reactor, these materials, mostly the silicides, were deposited by sputter deposition. The advent of the Genus reactor broadened the LPCVD market at the expense of the sputter market. Also, as LPCVD tungsten silicide became a reality, more design-ins occurred, thus further broadening the LPCVD market.

A third reason is the way LPCVD sales are reported by the equipment manufacturers. Most of the companies report the value of LPCVD tubes shipped, either for retrofits or installed in new furnace systems. The cost of the furnace is generally not included. Therefore, the actual value of the LPCVD market is somewhat understated. Anicon and Genus both manufacture non-tube LPCVD reactor systems and the total value of their systems is included in the 1984 LPCVD market demand. The systems shipped by these two companies accounted for $35.6 million, or 26 percent of the 1984 LPCVD market.

Table 9 ranks the leading LPCVD manufacturers by 1984 sales. Note that Thermco is ranked first, followed by Genus and Anicon. Also, the worldwide LPCVD market is dominated by U.S. companies. Of the $141.5 million in worldwide sales in 1984, the three Japanese companies--Kokusai, TEL/Thermco, and Koyo Lindberg--accounted for only $32.8 million, or 23 percent, and the latter two companies are actually joint ventures with U.S. firms.

Table 9

WORLDWIDE LPCVD EQUIPMENT MARKET SHARE--1984
(Millions of Dollars)

Company	Sales	Share
Thermco	$ 20.8	14.7%
Genus	18.0	12.7
Anicon	17.6	12.4
TEL/Thermco	15.0	10.6
Kokusai	14.5	10.2
ASM	13.4	9.5
ACS	12.0	8.5
Tylan	9.0	6.4
Bruce	7.0	5.0
Tempress	5.2	3.7
Process Technology	4.7	3.3
Koyo Lindberg	3.3	2.3
Others	1.0	0.7
Total	$141.5	100%

Source: DATAQUEST

PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION

Plasma enhanced CVD (PECVD) is the newest of the major CVD techniques. Although the parallel plate reactor was introduced in 1976, it was not until after the development of the horizontal tube reactor in 1979 that plasma deposition of films began to gain widespread use in IC production. The main advantage of PECVD is that it is a low-temperature process. Silicon nitride and silicon oxide, which make up the majority of films deposited by PECVD, are deposited at temperatures of less than 400 degrees C, and it was the low-temperature deposition of silicon nitride, in particular, that caused PECVD to gain rapid acceptance.

Before the development of PECVD, IC devices were typically passivated with a layer of PSG. Because PSG is hygroscopic, the absorbed moisture could react to form phosphoric acid, and this could cause potential aluminum corrosion problems when plastic packages were used. Silicon nitride, an effective moisture barrier, could not be used in lieu of PSG because the silicon nitride deposition process then available was a

high-temperature LPCVD process and the underlaying aluminum metallization layer could not withstand the high temperature. With the development of the low-temperature PECVD nitride process, the IC industry began to shift to that process for the final passivation, although PSG is still in widespread use as a passivation layer. Further, the use of nitride allowed the widespread use of plastic packaging.

Equipment Configurations

PECVD equipment is of two main types: the parallel plate design and the horizontal tube design. The parallel plate reactor was developed first, although the horizontal tube reactor is, today, the more dominant technology for production use. Regardless of type, in a PECVD reactor, RF power is used to supply the energy to create a plasma and dissociate the reactant gases into highly reactive products. The gas products then react at the wafer surface to form the film. Although plasma deposition can occur at low temperatures, the wafer is usually heated to 300 to 400 degrees C to improve the quality of the film. Deposition rates for PECVD processes are in the range of 200A to 400A per minute.

Tables 10 and 11 list the manufacturers of parallel plate and horizontal tube reactors.

Table 10

MAJOR PECVD EQUIPMENT MANUFACTURERS

Company	Model	Reactor Design	150mm Wafers per Load	ASP ($K)
Advanced Semiconductor Materials	-	Horizontal Tube	30	$400
Pacific Western Systems	560	Horizontal Tube	60	$400
Applied Materials	AMP3300	Parallel Plate	8	$182
E.T. Electrotech	ND6200	Parallel Plate	8	$400
Plasma-Therm	3011	Parallel Plate	10	$178

Source: DATAQUEST

Table 11

OTHER PECVD EQUIPMENT MANUFACTURERS

Company	Location	Reactor Design	Comments
Anelva	Japan	Parallel Plate	R&D use
Plasma-Electronic	West Germany	Parallel Plate	R&D use
Plasma-Technology	England	Parallel Plate	Benchtop unit
Semy Engineering	France	Horizontal Tube	Similar to Pacific Western Systems
Helmut Seier	Switzerland	Vertical Tube	8-inch wafer capacity
Technics	U.S.	Parallel Plate	Benchtop unit
Tokuda	Japan	Parallel Plate	Toshiba only
Ulvac	Japan	Parallel Plate	Cassette-to-cassette
SAMCO	Japan	Parallel Plate	R&D use

Source: DATAQUEST

Parallel Plate Reactor

In 1976, Applied Materials introduced the first commercially available plasma deposition system. The design of the system was based on the Reinberg reactor developed by Dr. A. R. Reinberg at Texas Instruments in the early 1970s. The current Applied Materials AMP 3300 design (see Figures 15 and 16) consists of two horizontal, circular, parallel plates or electrodes. Since the electrodes are 26 inches in diameter and only 2 inches apart (fixed), a uniform plasma is created between the electrodes. Wafers are placed on the lower electrode and heated from beneath to temperatures of up to 360 degrees C. The reactant gases are introduced at the center of the perforated upper electrode. The lower electrode is rotated to increase deposition uniformity. Films are deposited at pressures of 200 to 300 mtorr and with RF power frequencies that can be varied from 8kHz to 11kHz.

Plasma-Therm's model 3011 parallel plate reactor has two 27-inch-diameter electrodes, and the spacing between them can be varied within the confines of the reactor chamber. The reactant gases are not introduced at the center of the electrode but elsewhere in the chamber. Because of the design of the system, the lower electrode does not need to rotate. Plasma-Therm offers a choice of either a low-frequency or a 13.56MHz RF power generator. Plasma-Therm makes several other, smaller parallel plate systems for both production and R&D use.

Figure 15

APPLIED MATERIALS PARALLEL PLATE REACTOR

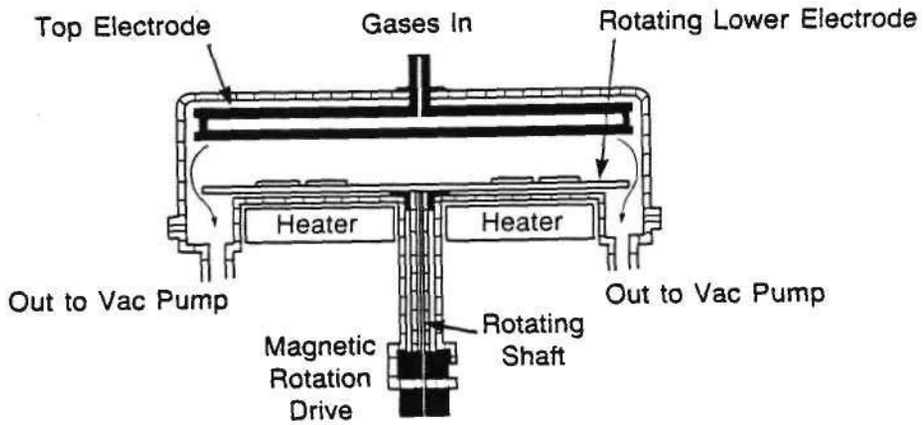
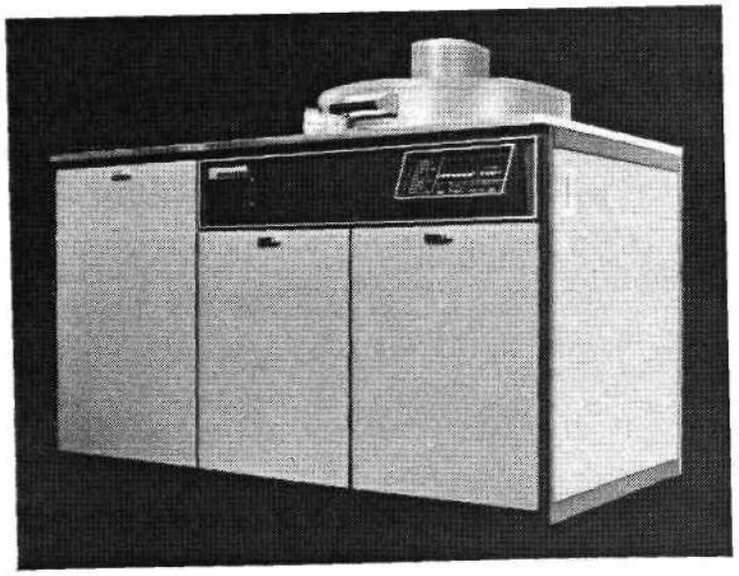


Figure 16

APPLIED MATERIALS AMP 3300



Source: Applied Materials

Both the Applied Materials and Plasma-Therm reactors are batch systems that have to be manually loaded/unloaded for each cycle. The reaction chamber has to be pumped down to the operating pressure after loading and then brought back up to atmospheric pressure for unloading. Also, after the wafers are loaded and the chamber lid is closed, time is required to bring the chamber back to operating temperature. Pump-down, venting, manual load/unload, and temperature recovery all require overhead time, which decreases the throughput of the machine.

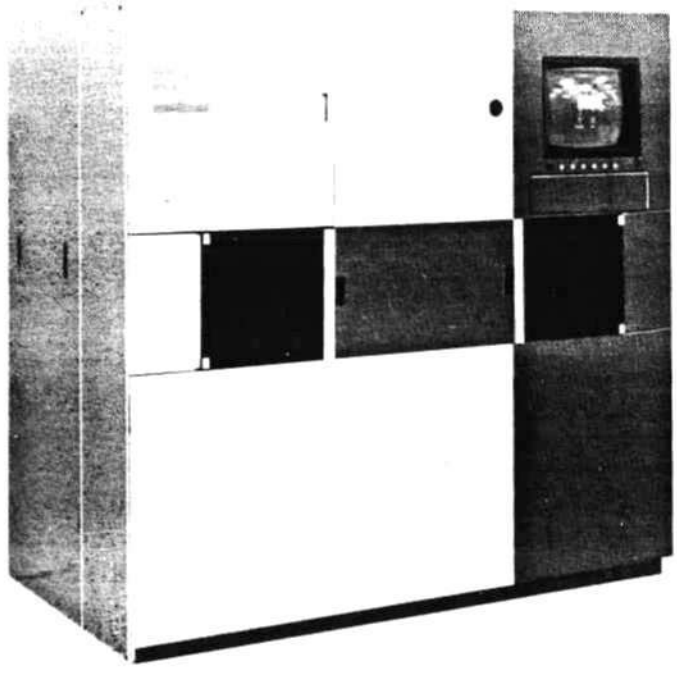
In contrast, the ND6200, manufactured by E.T. Electrotech, an English company, is a load-locked cassette-to-cassette batch system. In this type of system, the reaction chamber continuously stays near the operating pressure. While a batch of wafers is being processed, the load lock containing the next batch of wafers is pumped down to less than the chamber operating pressure. When the first batch has been processed and removed from the chamber, the next batch is transferred from the load lock into the chamber close to the operating pressure. Lengthy chamber pump-down time is not required and the batch begins processing almost immediately. The same sequence of operations occurs for the unload lock. The net effect is that overhead time is reduced and the throughput of the machine increases to 40 150mm wafers per hour. Another important advantage of load locks is that they act as a barrier to ambient contamination that might be carried into the process chamber. Further, in a load lock system, the chamber walls stay at a constant temperature, thus minimizing flaking of the deposited material from the chamber walls because of thermal expansion and contraction. The length of time between clean intervals is also extended.

Other manufacturers of parallel plate systems are shown in Table 11. Anelva currently provides a system for R&D use. However, it does have a cassette-to-cassette system under development. Tokuda, which is a subsidiary of Toshiba, has provided its systems only to Toshiba but will start marketing a system in the first half of 1985. The Ulvac model CPD-8148 is a unique parallel plate system, as it is a load-locked, in-line system with a rectangular discharge zone that is 380mm wide by 1,200mm long. Wafers are placed on trays and automatically move through the deposition zone facedown. Ulvac also has a small, circular parallel plate reactor for R&D use. The system is apparently designed for solar cells. At Semicon Osaka in June 1985, ULVAC introduced its MCP-1000 (Figure 17), which is a cassette-to-cassette, load-locked, parallel plate system very similar to E.T. Electrotech's model ND5200, which is the model that preceded the new ND6200 described above. SAMCO, a Japanese company, markets a line of small parallel plate systems for R&D use.

The main disadvantage of parallel plate reactors is their low throughput, and this led to the development of horizontal tube reactors.

Figure 17

ULVAC MCP-1000 CASSETTE-TO-CASSETTE REACTOR



Source: ULVAC

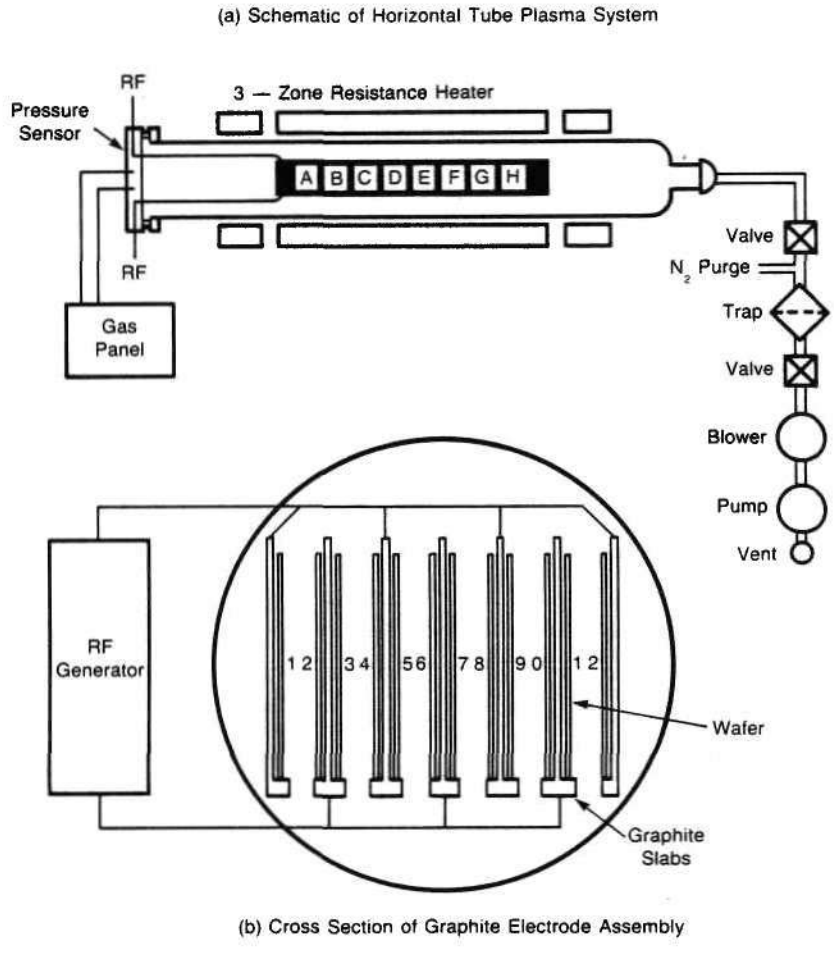
Horizontal Tube Reactors

In 1979, George Engle, of George Engle Co., conceived of an alternative design for a PECVD reactor that would use a standard quartz tube and fit into the bore of diffusion furnaces, which were in widespread use at the time. Engle developed the reactor in conjunction with Advanced Semiconductor Materials (ASM). Today, this so-called hot-wall type reactor (see Figure 18) consists of a 200mm furnace quartz tube (for 150mm wafers) into which is inserted a graphite electrode assembly. The electrode assembly consists of graphite slabs that are electrically isolated from each other. RF power is applied to the electrodes and alternate slabs are grounded so that a plasma is created in each space between the slabs. Wafers are placed on each side of the slab except on the outside. The slabs run the length of the tube. The reactant gases are introduced at the front of the tube and flow down the length of the tube. The quartz tube fits into the bore of a dedicated furnace, where zone-resistance heaters heat the wafers to the desired temperature. Because of these heaters, higher deposition temperatures can be obtained and films like polysilicon (620 to 650 degrees C) can be deposited.

The main advantage of horizontal tube reactors is the larger wafer load size and, hence, higher throughput. For instance, 84 to 96 125mm wafers can be processed at one time. Another advantage is that the wafers are processed in a vertical position and are less likely to intercept particulates.

Figure 18

SCHEMATIC OF A HORIZONTAL TUBE PLASMA SYSTEM



Source: ASM America

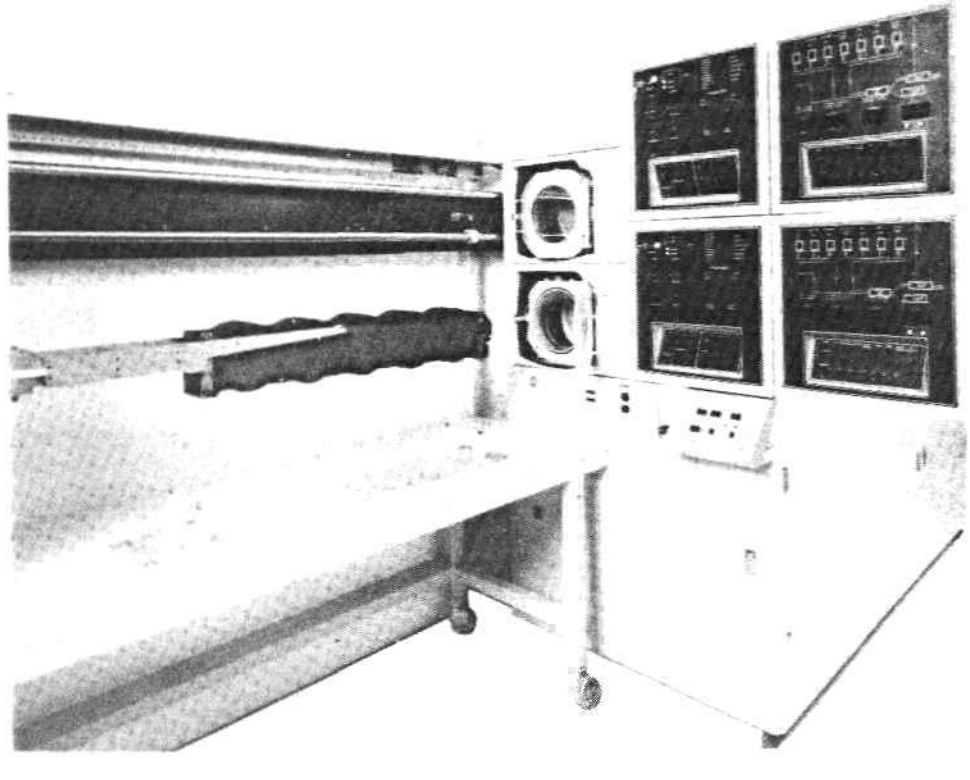
The graphite electrode assembly (boat) is withdrawn each cycle to load/unload the wafers, and because the boat rolls on wheels, particulates could be created. In an effort to reduce this source of contamination, soft-contact and cantilever loading have been developed as in LPCVD systems. ASM has a two-tube, 200mm reactor with a soft-contact loader that operates at an RF power frequency of 50kHz. ASM has another system that uses two 170mm quartz tubes operating at an RF power frequency of 450kHz, but this system will only handle up to 125mm wafers. Each tube in either the 170mm or 200mm reactor can be operated independently of the other so that two separate processes can be run at the same time.

The new Pacific Western Systems (PWS) model 560 reactor has 200mm independent process tubes and can be installed in the clean room in a through-the-wall configuration. Like the newer ASM reactor, the model 560 also has a lower RF power frequency that can be varied over the range of 25kHz to 125kHz. Figure 19 shows the model 560 with the cantilever loader holding the electrode assembly and configured for through-the-wall installation. Both the ASM and PWS reactors described here are dedicated quartz tube/furnace systems. However, PWS also markets a four-stack diffusion furnace in which LPCVD, PECVD, or diffusion tubes in any combination can be installed. The PECVD reactor tubes can also be installed in the field on a retrofit basis into other manufacturers' diffusion furnaces.

Semy Engineering, of France, is marketing a two-tube PECVD reactor that appears to be similar in design to PWS' systems.

Figure 19

PACIFIC WESTERN SYSTEMS MODEL 560



Source: Pacific Western Systems

Vertical Tube Reactor

Several companies are now introducing, or have under development, vertical tube diffusion furnaces. Although none of these furnaces currently have PECVD capability, it is expected that it will be added once the vertical furnaces gain acceptance in the marketplace. Helmut Seier, of Switzerland, introduced its vertical furnace less than two years ago and is now developing a PECVD capability. For more information on vertical furnaces see the discussion on LPCVD.

Applications

Silicon nitride accounts for 75 percent of the films deposited by PECVD, silicon oxide 20 percent, and other films such as polysilicon, amorphous silicon, oxynitride, and titanium silicide the remaining 5 percent. The following is a discussion of some of the applications of PECVD films. It should be noted that PECVD is a relatively new technique and not yet fully understood. As the knowledge of plasma processes increases, new materials will be deposited by PECVD and new applications will emerge.

Silicon Nitride

Because silicon nitride can be deposited at temperatures of less than 400 degrees C and has good scratch resistance, good moisture resistance, and good alkali-gettering capability, its major application is as a passivation, layer. Because of the widespread use of PECVD nitride passivation, this application alone accounts for the majority of films deposited by PECVD. Nitride is also used as an interlayer dielectric and in other applications that require a low-temperature nitride deposition. (LPCVD deposition of nitride is a high-temperature process.)

However, PECVD nitride films contain a fairly high percentage of hydrogen, and while this is generally not a problem when PECVD nitride is used as a passivation layer, it can be of concern when PECVD nitride is used in other applications. The inclusion of hydrogen affects the density of the film, and as the hydrogen content increases the density decreases. Increasing the deposition temperature decreases the hydrogen content, and this is the reason most PECVD nitride depositions take place near 400 degrees C, although nitride can be deposited at much lower temperatures. Another problem with a high hydrogen content is that the hydrogen will evolve from the nitride dielectric film during subsequent high-temperature processing steps and this may affect MOS device stability.

Another application for PECVD nitride is its use as a capping layer in gallium arsenide (GaAs) device fabrication. For GaAs devices, uniform dopant diffusion after implant occurs at a temperature of 850 degrees C. Because GaAs begins to decompose at 355 degrees C and dopant boil-off occurs at 500 degrees C, a capping seal is required to contain the constituents while the 850 degrees C anneal is occurring. PECVD nitride can be used for the capping layer, since it can be deposited at temperatures of below 355 degrees C. However, the hydrogen content must be kept low or the hydrogen will evolve from the film during the anneal step and pinholes would be created in the nitride cap, allowing substrate oxidation to occur at the pinhole sites. Typical PECVD nitride contains too much hydrogen for this application; however, Plasma-Therm has developed a PECVD nitride process with a low hydrogen content specifically for this application. Because of the low hydrogen content of the Plasma-Therm nitride film, it can also be used as an interlayer dielectric.

Silicon Dioxide

Although PECVD oxide is used as an interlayer dielectric, LPCVD is currently the primary method for depositing interlayer dielectrics in production. Trends indicate that the IC industry will shift more and more to BPSG, which is a doped oxide, for use as an interlayer dielectric in VLSI devices. Currently, the most developed BPSG process, is an APCVD process but both the LPCVD and PECVD manufacturers are also developing BPSG processes. However, should the PECVD BPSG process emerge as the dominant production technology, then the PECVD market will expand at the expense of the LPCVD market as the IC manufacturers shift to PECVD dielectrics in lieu of LPCVD dielectrics. BPSG is discussed in more detail later in this section under TRENDS IN INTERLAYER DIELECTRICS.

Silicon Oxynitride

It would be desirable to use a single film for both the passivation layer and as an interlayer dielectric for double-metal devices. Ideally, the film would have good step coverage, low dielectric constant, and good stress characteristics and would be a barrier to impurity diffusion. PECVD silicon nitride has good resistance to impurity diffusion and excellent step coverage but high stress characteristics and a high dielectric constant. PECVD oxide, on the other hand, has low stress characteristics and a low dielectric constant but poorer step coverage and more susceptibility to impurity diffusion. The search for a single material has led to PECVD oxynitride, which combines the best characteristics of both films while minimizing their drawbacks, with the result that it can be used both for passivation and as an interlayer dielectric. At present, this is not a major application.

Titanium Silicide

Currently, highly doped polysilicon is used for gate interconnects. However, the trend toward smaller VLSI geometries has dictated a need for gate interconnection materials with lower resistivities. The refractory metal silicides, $MoSi_2$, WSi_2, $TaSi_2$, and $TiSi_2$ have been considered as alternative materials. WSi_2 is now being used in the production of IC devices because there is a commercially available LPCVD reactor for WSi_2 deposition (from Genus). However, a PECVD process has been developed to allow the use of $TiSi_2$ as a gate interconnect in lieu of WSi_2. $TiSi_2$ has a lower resistivity and a lower anneal temperature than WSi_2. While it is not clear at this point which silicide (or silicides) will emerge as the dominant technique to be used in the fabrication of VLSI devices, it is apparent that one of the more important selection criteria will be the ease, reliability, and film quality of deposition in a production environment. Thus, while the new PECVD $TiSi_2$ process is not a major application today, its future role in VLSI fabrication is yet to be determined. More information on silicides is given later in this section under TRENDS IN INTERCONNECTION TECHNOLOGY.

Regarding the various PECVD equipment manufacturers, Advanced Semiconductor Materials has been aggressive among the horizontal tube manufacturers in developing new PECVD processes, and it has processes for nitride, oxide, polysilicon, amorphous silicon, oxynitride, and titanium silicide. ASM introduced its $TiSi_2$ process in mid-1984 but sold only a few tubes. However, the market for this process and other silicide processes as well will expand in the next few years. Among the parallel plate companies, Plasma-Therm has also pursued an aggressive process development program for specialty films.

While the other PECVD equipment manufacturers compete in the commodity silicon device market, Plasma-Therm has focused its activities on the specialty market for nitride and oxide films for GaAs and other III-V devices, and perhaps as much as 85 percent of its sales are directed to this market. Plasma-Therm dominates the GaAs market, having essentially no competition in this area. Although the market for GaAs devices is currently small in relation to the silicon device market, it is expected to grow at a faster rate than the silicon market over the next five years. Plasma-Therm, of all the PECVD equipment manufacturers, is best positioned to take advantage of this growth.

Plasma-Therm's low-throughput batch reactors are adequate for today's low-volume GaAs device market. However, because GaAs substrates are brittle, automatic wafer handling will be needed for tomorrow's higher-volume production. Up until now, Plasma-Therm has focused its efforts on the III-V niche market, but it is now beginning to address the

commodity silicon device market and compete with the other PECVD equipment companies in this market. The company recently introduced a line of plasma etch and strip equipment that has cassette-to-cassette operation, so it has the capability of upgrading its PECVD reactors for production use.

Market Analysis

Table 12 shows the worldwide PECVD equipment demand for the last three years. Total worldwide sales for 1984 were $71.3 million. Note that the U.S. demand is considerably higher than the Japanese demand for PECVD equipment. DATAQUEST believes that this reflects the Japanese tendency to use PSG more as a passivation layer instead of silicon nitride as is used in the United States. Since PSG is deposited by APCVD or LPCVD techniques, this accounts for the lower PECVD equipment demand in Japan. In addition, there is no major manufacturer of PECVD equipment in Japan; DATAQUEST believes that most of the PECVD equipment used in Japan is imported from U.S. manufacturers. This is supported by DATAQUEST's estimate that the Japanese market accounts for almost one-third of the leading U.S. PECVD equipment manufacturers' sales.

Table 12

WORLDWIDE PECVD EQUIPMENT MARKET DEMAND
(Millions of Dollars)

	1982		1983		1984	
	Sales	Share	Sales	Share	Sales	Share
United States	$17.0	54%	$22.3	50%	$36.8	51%
Japan	10.0	31	14.6	33	22.6	32
ROW	4.8	15	7.3	17	11.9	17
Total	$31.8	100%	$44.2	100%	$71.3	100%

Source: DATAQUEST

The ROW region, which is mostly Europe, has a relatively high demand in relation to its share of worldwide IC production, which for Europe in 1984 was 9 percent. DATAQUEST believes that this is because of the manufacturing presence of ASM in The Netherlands and E.T. Electrotech in England. Both ASM and E.T. Electrotech are European companies with operations in the United States. ASM America has manufacturing plants in the United States; Electrotech has a network of sales offices. In addition, there are several other European manufacturers of PECVD equipment, as listed in Table 11.

PECVD equipment market growth is shown in Table 13. In 1983, growth was higher in Japan than in the United States because of the higher rate of capital spending in Japan than in the United States. In 1984, U.S. and Japanese capital spending were nearly the same, and the higher growth for PECVD equipment in the United States reflects the tendency of the Japanese to use PSG more, as discussed above.

Table 14 lists the market share leaders. Note that the horizontal tube manufacturers, ASM and Pacific Western Systems, together had a 66 percent market share, with ASM alone accounting for 49 percent of the world market. The three parallel plate manufacturers, E.T. Electrotech, Applied Materials, and Plasma-Therm, had nearly equal shares and together accounted for 26 percent of the worldwide market. The other manufacturers in the United States, Japan, and Europe account for the remaining 8 percent share.

Table 13

WORLDWIDE PECVD EQUIPMENT MARKET GROWTH
(Millions of Dollars)

	1983		1984	
	Sales	Growth	Sales	Growth
United States	$22.3	31%	$36.8	65%
Japan	14.6	46%	22.6	55%
ROW	7.3	52%	11.9	63%
Total	$44.2	39%	$71.3	61%

Source: DATAQUEST

Table 14

WORLDWIDE PECVD EQUIPMENT MARKET SHARE--1984
(Millions of Dollars)

Company	Sales	Share
Advanced Semiconductor Materials	$34.7	49%
Pacific Western Systems	12.5	17
E.T. Electrotech	6.4	9
Applied Materials	6.2	9
Plasma-Therm	5.7	8
Others	5.8	8
Total	$71.3	100%

Source: DATAQUEST

PHOTOCHEMICAL VAPOR DEPOSITION

In an LPCVD system, the reactant gases are decomposed by thermal energy and film deposition occurs on a heated wafer in the range of 400 to 920 degrees C, depending on the deposited film. In a PECVD system, an RF-excited plasma is used to decompose the reactant gases, with deposition occurring at lower temperatures, in the range of 200 to 400 degrees C. In a photochemical vapor deposition reactor (photo-CVD or PCVD) ultraviolet light is the source of energy used to decompose the reactant gases. The main advantage of PCVD is the lower deposition temperatures, which are in the range of 50 to 200 degrees C. Films deposited by PCVD include silicon dioxide and silicon nitride.

The Photochemical Process

To deposit silicon nitride films, mercury vapor, silane, and ammonia are simultaneously introduced into the reaction chamber. A mercury arc lamp, separated from the reaction chamber by a quartz window, provides UV radiation at a wavelength of 253.7nm. The UV photons pass through the quartz window and elevate the mercury vapor atoms in the reaction chamber from the ground state to an excited state ($h\nu + Hg \longrightarrow Hg^*$).

The excited mercury atom then transfers its energy via collisions to the silane and ammonia gases in the reaction chamber, generating free radicals and reaction products, which eventually lead to the deposition of a silicon nitride film. For the deposition of silicon dioxide films, silane and nitrous oxide gases are used along with mercury vapor.

Film Characteristics

In PECVD system, the substrate is bombarded with high-energy charged particles, which can cause radiation damage to the substrate. In a PCVD system, since the energy of the UV photons is below the gas ionization energy, no charged particles are produced. Hence, another advantage of PCVD is that there is no radiation damage and the deposited film will not contain any trapped charged particles that could degrade device performance.

Heat from the mercury lamp causes only about a 5 degrees C rise in substrate temperature. This is in contrast to PECVD systems, in which plasma heating effects will raise the wafer temperature substantially. Thus, in a PCVD system, film deposition can take place at as low as 50 degrees C, although some substrate heating is desirable to promote better film adhesion.

PCVD silicon nitride and silicon dioxide films are conformal and have low pinhole counts. Pinholes are less likely to be produced in a photochemical process because of the low deposition temperature and because less particles are generated in the process.

Thermal expansion coefficients between the deposited film and substrate can be significantly different. Because of this difference, mechanical stresses can be induced in the film in a high-temperature deposition process as the film and wafer cool to room temperature. Because deposition in a PCVD system takes place at low temperatures, no mechanical stress is induced in the film.

A concern in PCVD is the inclusion of mercury in the deposited film. This may be undesirable in MOS devices because device performance may be degraded. Mercury levels on the order of 2×10^{16} atoms per cubic centimeter have been measured in deposited films. However, there is no evidence that this level of contamination will adversely affect MOS device performance. For III-V and other exotic substrate materials, the mercury inclusion does not seem to be a problem.

Applications

The primary application for PCVD is in the fabrication of semiconductor photodetectors and semiconductor diode lasers. Semiconductor photodetectors include infrared detectors, ultraviolet sensors, and visible sensors. These devices use III-V and other exotic material substrates, which decompose at low temperatures and which, therefore, require processing temperatures below 200 degrees C. The low-temperature PCVD process is used in the fabrication of photodetectors and diode lasers to deposit silicon dioxide and silicon nitride interlayer dielectric and passivation films.

Within this application, DATAQUEST believes that the major use of PCVD is in the fabrication of military infrared detectors using a mercury cadmium telluride (HgCdTe) substrate. Companies manufacturing infrared detectors include General Dynamics, Honeywell, Northrup, Raytheon, and Rockwell.

The low-temperature deposition of PCVD would be an advantage in MOS device fabrication particularly as advanced VLSI devices are developed. However, DATAQUEST does not believe that any PCVD systems are currently being used in this area because of the unavailability of production-oriented machines. Also, there may be some concern about the mercury contamination issue.

Equipment Configurations

The Tylan PVD-1000 is currently the only commercially available photochemical deposition system in the United States. It was originally developed by Tylan in 1980 in conjunction with Hughes Aircraft Co. for use in fabricating military infrared detector devices. The PVD-1000 is designed for low-volume R&D or pilot line use. It has twin reaction chambers, each of which can process up to five 100mm wafers. The film growth rate is 65A per minute for silicon nitride and 150A per minute for silicon dioxide. Figure 20 shows the Tylan system, which has an average selling price of about $130,000. To overcome the throughput limitations of the PVD-1000, Tylan is developing a system designed for high-volume production.

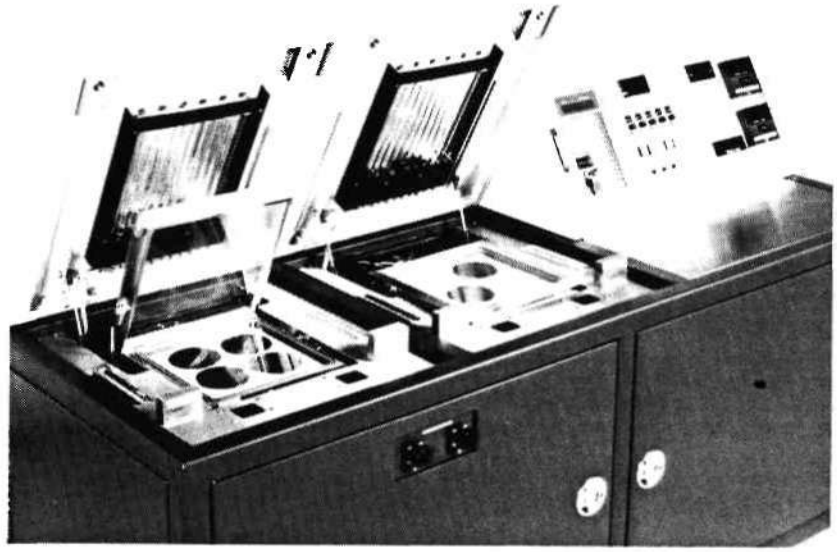
DATAQUEST estimates that Tylan sold 10 PVD-1000s in 1984 for sales of $1.3 million and that the total installed base of PVD-1000s is 30 to 35 units. In Japan, Nippon Tylan, a joint venture between Tylan and Peter Aoyama, manufactures the GS4500 and GS6000A PCVD systems. DATAQUEST estimates that Nippon Tylan has sold five of these systems to date. In addition, SAMCO, another Japanese company, introduced in September 1984 its PCVD system for $38,000. SAMCO has sold five of these systems to date.

In a general sense, PCVD equipment concerns include film growth rates, which are low compared with other deposition techniques. Since the growth rate is directly related to the photon flux density, the development of photon sources with higher-density fluxes is necessary if higher rates suitable for volume production are to be achieved. Higher productivity machines would broaden the PCVD market to include MOS fabrication.

Another area of equipment improvement would be the development of a PCVD system that would eliminate the inclusion of mercury in the deposited film and alleviate this concern.

Figure 20

TYLAN PVD-1000



Source: Tylan

ELECTRON CYCLOTRON RESONANCE PLASMA CVD

Anelva, of Japan, has recently announced the development of an electron cyclotron resonance (ECR) plasma CVD system in conjunction with Nippon Telegraph and Telephone Corporation (NTT). Anelva's design is based on NTT's ECR system, shown in Figure 21. Microwave power at 2.45 GHz is introduced into the plasma chamber through a rectangular waveguide and a quartz window. The magnet coils provide the circular electron motion and the resulting electron cyclotron frequency is made to coincide with the microwave frequency. This is the electron cyclotron resonance condition, which allows the plasma to effectively absorb the microwave energy at low gas pressures in the range of .01 to 1 mtorr. Thus, the plasma nas a high excitation efficiency and a highly activated plasma is easily obtained.

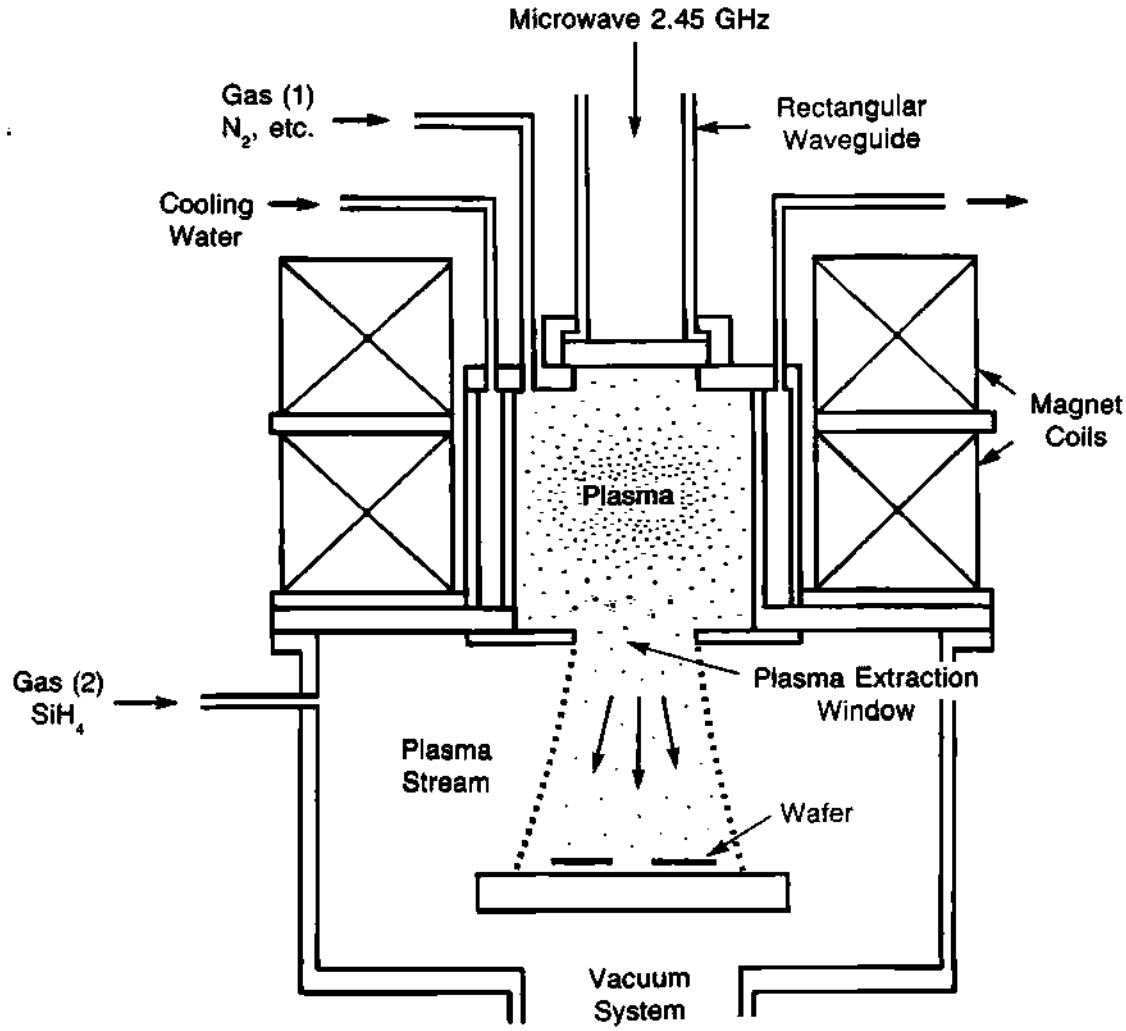
ECR CVD is used to deposit silicon nitride and silicon oxide. The advantage of this technique is that deposition occurs at room temperature, whereas, in conventional RF-excited PECVD, deposition normally occurs in the range of 200 to 400 degrees C. However, in the ECR system, the wafer still reaches temperatures in the range of 50 to 150 degrees C because of heating effects from the plasma. For nitride, deposition rates of 200A to 300A per minute are obtained. The nitride film is dense, of high quality, and, unlike nitride films deposited by PECVD, the amount of hydrogen in the film is quite low.

Deposition rates for oxide films are 200A to 400A per minute and are also of high quality. It is possible that the quality of ECR-plasma-deposited nitride and oxide films is comparable with that of nitride films deposited by high-temperature LPCVD and oxide films deposited by thermal oxidation.

The ECR system described here for IC production is still under development by Anelva. However, Anelva has provided ECR CVD deposition systems for silicon dioxide, silicon nitride, and amorphous silicon for use in thin-film displays and solar cells since 1983. In addition, Anelva introduced in Japan in 1984 an ECR reactive ion etch system (RIB-310), which will be available in the United States in 1985, so it is clear that Anelva has experience with this technology.

Figure 21

ECR PLASMA DEPOSITION SYSTEM



Source: S. Matsuo and M. Kiuchi "Low Temperature Deposition Apparatus Using An Electron Cyclotron Resonance Plasma" NTT, Japan

Chemical Vapor Deposition

TRENDS IN INTERCONNECTION TECHNOLOGY

Aluminum is widely used in IC device fabrication for making contacts and as an interconnection material. Likewise, highly doped polysilicon is widely used for making interconnections at the gate level. Both of these materials have several characteristics that have made them the dominant interconnection technologies used in today's device fabrication. However, as device geometries continue to shrink and device junctions continue to get shallower, these technologies will not be able to meet the challenge and new interconnection technologies will need to be used.

The Problem

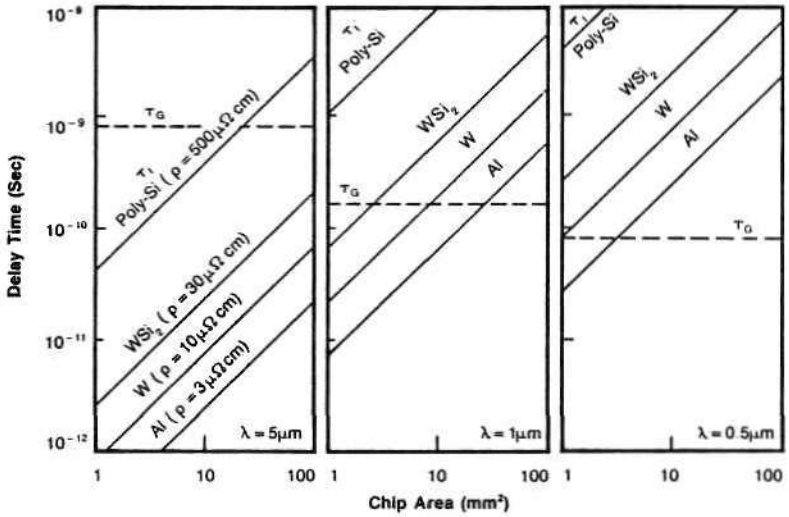
IC devices are scaled to obtain higher packing densities and higher device speeds. To obtain faster speeds, gate oxide thicknesses are reduced, channel lengths are decreased, and junction depths get shallower. The problem is that while scaling active elements improves performance, its effect on interconnections is the opposite. Because of scaling, interconnect lines become thinner and narrower and, in addition, get longer because of the larger die sizes used for advanced VLSI devices. The net effect of all these factors is to increase the interconnect resistance and, hence, the RC time delay of the circuit.

Figure 22 shows gate delay time ($_G$) and interconnect delay time ($_I$) as a function of chip area and minimum features size. It is apparent that as the minimum feature size shrinks, the gate delay and, hence, device speed increases. However, the figure also shows that the interconnect delay increases as the geometries get smaller and the devices get bigger. For 5um devices, interconnect delay is less than the gate delay for all but the largest chips. For 1um devices, interconnect delays are longer than the gate delay except for the small chips. Therefore, in order to obtain the faster speeds promised by scaling, lower-resistance materials and different interconnection methods had to be found. Table 15 lists the resistivity characteristics of some of the more important materials being considered.

Other problems associated with scaling include increased contact resistance as the contact area gets smaller, electromigration failures, which result from the increased current densities in the thinner and narrower aluminum interconnect lines, and contact failures resulting from shorted or leaky junctions. In addition, the greater aspect ratio of VLSI steps (aspect ratio is the step height divided by step width) strains the limits of metal deposition in step coverage.

Figure 22

INTERCONNECTION TIME DELAY VERSUS CHIP AREA FOR DIFFERENT MATERIALS AND MINIMUM FEATURE SIZES



Source: K.C. Saraswat and F. Mohammadi "Effect of Scaling of Interconnections of the Time Delay of VLSI Circuits" IEEE Transactions on Electron Devices, 1982

Table 15

PROPERTIES OF INTERCONNECTION MATERIALS

	Bulk Resistivity μΩ-CM	Thin-Film Resistivity μΩ-CM	Sinter Temperature (°C)
Polysilicon*	250.0	500	-
Aluminum	2.3	3	-
Molybdenum Silicide	21.6	40	1,000
Tantalum Silicide	8.5	35	1,000
Titanium Silicide	13.0	15	650
Tungsten Silicide	12.5	30	1,000
Tungsten	5.5	10	-
Molybdenum	5.0	10	-

*Heavily doped

Source: DATAQUEST
K. Saraswat and F. Mohammadi

Chemical Vapor Deposition

To overcome the limitations of today's interconnect methods, different materials that have the following general characteristics are required:

- Low resistivity
- Form low-resistance contacts
- Good electromigration resistance
- High temperature stability
- Form stable interfaces with silicon, oxide, and the final metallization
- Corrosion and oxidation resistance
- Good adhesion

From an IC fabrication point of view the materials should be:

- Easily and reliably deposited
- Capable of being dry etched
- Compatible with the IC fabrication process
- Easily implemented into the fabrication process

There are three areas in VLSI device interconnection that require these materials.

- Contacts
- Gate interconnects
- Metallization

Tnere are several candidate materials in each of these areas, but there is no one best material. Trade-offs will have to be made such that several may emerge as dominant technologies. Further, the choice of a material will result not only from an evaluation of its physical properties but also from consideration of problems associated with using it in a production environment. The material with the preferred physical properties may not be used if it cannot, for example, be reliably deposited and etched. Thus, new interconnection methods are intimately involved with process and equipment developments. The following sections discuss the three areas in more detail, including the deposition of the materials required in the new interconnection methods.

Chemical Vapor Deposition

Contacts

Aluminum, which is widely used as the contact metal to silicon junctions, has to be annealed after deposition at temperatures of between 400 and 500 degrees C. At these temperatures, the aluminum and silicon will interdiffuse and a leaky junction leading to contact failure may result. In addition, aluminum spikes can penetrate the junction to the underlying substrate and, thus, short out the junction. This problem has been alleviated by the use of an Al/1%Si alloy but for VLSI devices with shallow junctions on the order of 0.1um to 0.2um this solution is not satisfactory. Also, the contact resistance of aluminum on silicon is too high for VLSI devices, and a lower contact resistance is required, particularly, for contact dimensions of 1um or less.

To replace aluminum as a contact metal, refractory metals such as molybdenum, tungsten, titanium, tantalum, and tungsten/titanium have been considered. These metals act as contact barriers to prevent aluminum/silicon interdiffusion between the aluminum metallization layer and the underlying silicon junction. All have good contact resistance on silicon for submicron geometries with the exception of titanium, whose contact resistance is not satisfactory for contact dimensions below 1um.

The refractory metals are usually sputtered, with the exception of tungsten, which can also be deposited in a CVD reactor. In practice, a thin layer of the refractory metal (1,000A to 1,200A) is deposited prior to the normal aluminum metallization. Although many contact barrier materials are being considered, no clear choice has yet emerged. However, there are certain advantages to using CVD tungsten as a barrier metal. Sputtered refractory metals require added process steps while CVD tungsten can be implemented with minimal process change.

Deposition of LPCVD tungsten can be a selective process; the tungsten is selectively deposited on the silicon in the contact areas and not on the oxide dielectric. The process is selective because there is preferred nucleation on the silicon and because 200A to 400A of silicon are consumed in the process. However, if the wafers are not cleaned well prior to deposition, tungsten nucleation sites will form on the oxide dielectric. DATAQUEST believes that using tungsten as a barrier metal is still in the R&D and pilot production stage but that we may see some full production use by the end of 1985.

Most of the LPCVD equipment manufacturers advertise a selective tungsten process. The Genus reactor also deposits tungsten. However, it is a higher-temperature process intended for tungsten metallization and selective tungsten deposition will not occur at the higher temperatures.

Chemical Vapor Deposition

Gate Interconnect

Polysilicon has been the interconnection material of choice at the gate level because of its good step coverage, ease of deposition, and compatibility with the subsequent high-temperature processing steps. Also, polysilicon has excellent interface stability with both silicon and the gate oxide. However, even with highly doped polysilicon, the resistance for geometries below 2um becomes a limiting factor. Several different materials have been considered for reducing the gate interconnect resistance, including refractory metal silicides and refractory metals.

Of the silicides that have been studied, $TiSi_2$, $MoSi_2$, $TaSi_2$, and WSi_2 appear to be the most promising. When these materials are deposited on top of the polysilicon gate, the structure is called a polycide shunt. A typical polycide shunt would consist of 2,500A of a silicide on top of 2,000A of polysilicon. Use of a polycide will decrease the gate resistance by a factor of 10 over a typical polysilicon gate. Sheet resistances on the order of 2 ohms per square are obtained, in contrast with 20 ohms per square for a heavily doped polysilicon gate.

The polycide approach permits the continued use of polysilicon as a gate material and the retention of its many good qualities, such as the stable polysilicon/oxide interface. Silicides have properties that are compatible with standard IC processing. They can withstand the high temperature anneals and oxidation. They have good adhesion, good chemical resistance, and good dry etch properties. Table 16 summarizes some of the advantages and disadvantages of the silicides.

The main problem associated with silicides has been in the deposition area. Several physical vapor deposition techniques have been used to deposit silicides. These include sputter deposition from a composite target made of the silicide, cosputtering from two pure metal and silicon sources, and coevaporation from two e-beam sources. Sputter deposition from a composite target was first used to study $MoSi_2$ and WSi_2. However, the resulting silicide films contained contaminants, originating in the composite target, which degraded device performance. In addition, the stoichiometry of films sputtered from composite targets can be a problem. Cosputtered films have improved film purity but a significant amount of argon is incorporated in the film. Coevaporation of a metal and silicon from two e-beam sources also improves the film quality, but step coverage is poor.

Another problem associated with cosputtering and coevaporation is that the deposited films are not silicides but a mixture of the metal and silicon. Subsequent annealing at high temperature is required to form the silicide, but the silicide formation is accompanied by a volume change, which leads to high stress and possible cracks and adhesion

problems. The volume change also causes the resistivity of the film to increase. Silicides sputtered from composite targets also need to be annealed, not to form the silicide, which already exists, but to increase the grain size to lower the resistivity of the film. This recrystallization is also accompanied by an undesirable volume change.

Sputtering materials are also more expensive. For instance, it has been estimated that the composite target cost for sputtered WSi_2 is about $1.00 to $1.50 per wafer in contrast with $0.05 per wafer for the gases consumed in a CVD reactor.

Thus, physical vapor deposition of silicides suffers from limitations, which has been the driving force toward the development of CVD processes. As IC geometries shrink and aspect ratios get higher, the better step coverage and film quality of PECVD and LPCVD silicide processes will be an important factor in selecting the deposition technique.

Table 16

ADVANTAGES AND DISADVANTAGES OF REFRACTORY METAL SILICIDES

Advantages	Disadvantages
Low resistivity	Deposition not straightforward
Good process compatibility	Questionable mechanical integrity (stress, cracks, adhesion)
Good contacts to shallow junctions	
Can be dry etched	Void formation at Si/SiO_2 interface during oxidation if interface is not clean
Good electromigration resistance	

Source: K. C. Saraswat
Stanford University
Center for
Integrated Research

Chemical Vapor Deposition

The source materials for the CVD deposition of $MoSi_2$, WSi_2, $TiSi_2$ silicides are MoF_6, WF_6, $TiCl_4$. These materials are all liquids with sufficient vapor pressure at 25 degrees C to allow source flow to be controlled by a mass flow controller. The source materials for $TaSi_2$ are tantalum compounds, which must be heated to temperatures of greater than 100 degrees C to obtain sufficient vapor pressure to flow into the reactor. All the lines from the tantalum source to the reactor must be heated to the same temperature to prevent source condensation. Mass flow control is difficult at these temperatures, although the new heated mass flow controllers that have just become available may alleviate this problem. Thus, at least at present, $TaSi_2$ is more difficult to deposit than the other three silicides.

It is not clear at this point which of the silicides, if any, will become the dominant technology. While all of the four silicides discussed will reduce resistance, not all are equally easy to use and each has its own advantages and disadvantages. The choice of one silicide over another may depend not only on the film characteristics, but also on the deposition technique. For instance, the Japanese have used sputtered $MoSi_2$ in production for some time, even though that silicide does not have the best resistivity. The availability of an acceptable deposition process was most likely the major factor in their use of $MoSi_2$.

Tungsten silicide films have been deposited in LPCVD reactors and found to be very pure and dense and to have excellent conformal step coverage. The LPCVD-deposited films have a lower resistivity than PVD tungsten silicide films. The as-deposited amorphous films do not shrink with anneal as do the PVD tungsten silicide films.

DATAQUEST believes that tungsten silicide is currently the most widely used silicide in the United States, as there are several semiconductor manufacturers using it in production. Until recently, WSi_2 was the only silicide to be deposited with a CVD process, and this gave it a head start over the other silicides that were sputtered. Genus, the manufacturer that gave the LPCVD WSi_2 process its impetus with the introduction of a dedicated WSi_2 reactor, is currently the major supplier in this area, although the other CVD manufacturers are developing WSi_2 processes as well.

The Japanese have done development work in the PECVD deposition of $MoSi_2$ and ASM has recently developed a PECVD titanium silicide process. $TiSi_2$ films deposited by the ASM PECVD process exhibit both a lower resistivity and a lower anneal temperature than $TiSi_2$ sputtered films. Compared with WSi_2, $TiSi_2$ has a lower resistivity by a factor of 2 or 3. Also the anneal temperature for $TiSi_2$ is 650 degrees C, in contrast with 1,000 degrees C for WSi_2.

Chemical Vapor Deposition

A polycide gate is a silicide over polysilicon. In a pure silicide gate, the polysilicon is omitted and the refractory metal silicide is deposited directly on top of the gate oxide. However, this type of structure has problems with the stability of the silicide/oxide interface. For this reason, and because it is not yet clear what the advantages are of pure silicide gates over polycide gates, pure silicide gates have not received a lot of attention. However, with the recent developments in CVD tungsten silicide, this may change.

The use of polycides (or pure silicides) is probably only an interim solution to gate interconnects, since advanced VLSI devices place even more demanding requirements on reducing gate resistances. Titanium, molybdenum, and tungsten refractory metals have even lower resistivities than their silicides and are being considered as eventual replacements for the polycide structure. Whereas, a polycide structure results in a sheet resistance of 2 ohms per square, the refractory metals have sheet resistances in the range of 0.3 to 1 ohm per square for a 5,000A-thick film. In this type of interconnect 2,000A to 3,000A of the refractory metal are deposited directly on top of the polysilicon.

While the use of refractory metals for gate interconnects will reduce gate resistance, there are some process drawbacks. Refractory metals have poor corrosion resistance, poor adhesion after annealing, and poor oxidation characteristics. For instance, tungsten oxidizes at temperatures of above 450 degrees C and, thus, protective silicon oxide or nitride films are required. In addition, process temperatures for refractory metals must be kept below 600 degrees C because above that temperature, the metal will react with the underlying silicon to form a silicide, which results in a higher contact resistance.

Refractory metal technology is still in the R&D stage, and it is not yet clear what metal or metals will emerge as the technology of choice. However, one advantage of CVD tungsten is that it can be deposited selectively on the polysilicon gates without deposition on the adjacent oxide.

Another interconnect method that has been used is the self-aligned silicide (called salicide) structure. In this method, a silicide is deposited on top of the entire source/drain region and on top of the polysilicon gate as well. Contact is made to the silicide instead of directly to the source/drain. The purpose of the silicide over the entire source/drain area is to reduce the sheet resistance associated with shallow junctions. Sheet resistances of less than 5 ohms per square are obtained, in contrast with 20 to 100 ohms per square for a typical source/drain.

Chemical Vapor Deposition

The process steps for obtaining the salicide structure are shown in Figure 23. The reactive ion etch (RIE) step leaves an oxide space on the gate sidewall. A metal is deposited and thermally reacted with the underlying silicon to form a silicide. The metal on the sidewall remains unreacted and is removed by an etchant to isolate the gate from the source and drain. However, there are some processing problems because it is difficult to restrict silicide formation to the top of the gate and source/drain. Also, the silicidation process consumes the silicon in the shallow source/drain as shown in Figure 23(d).

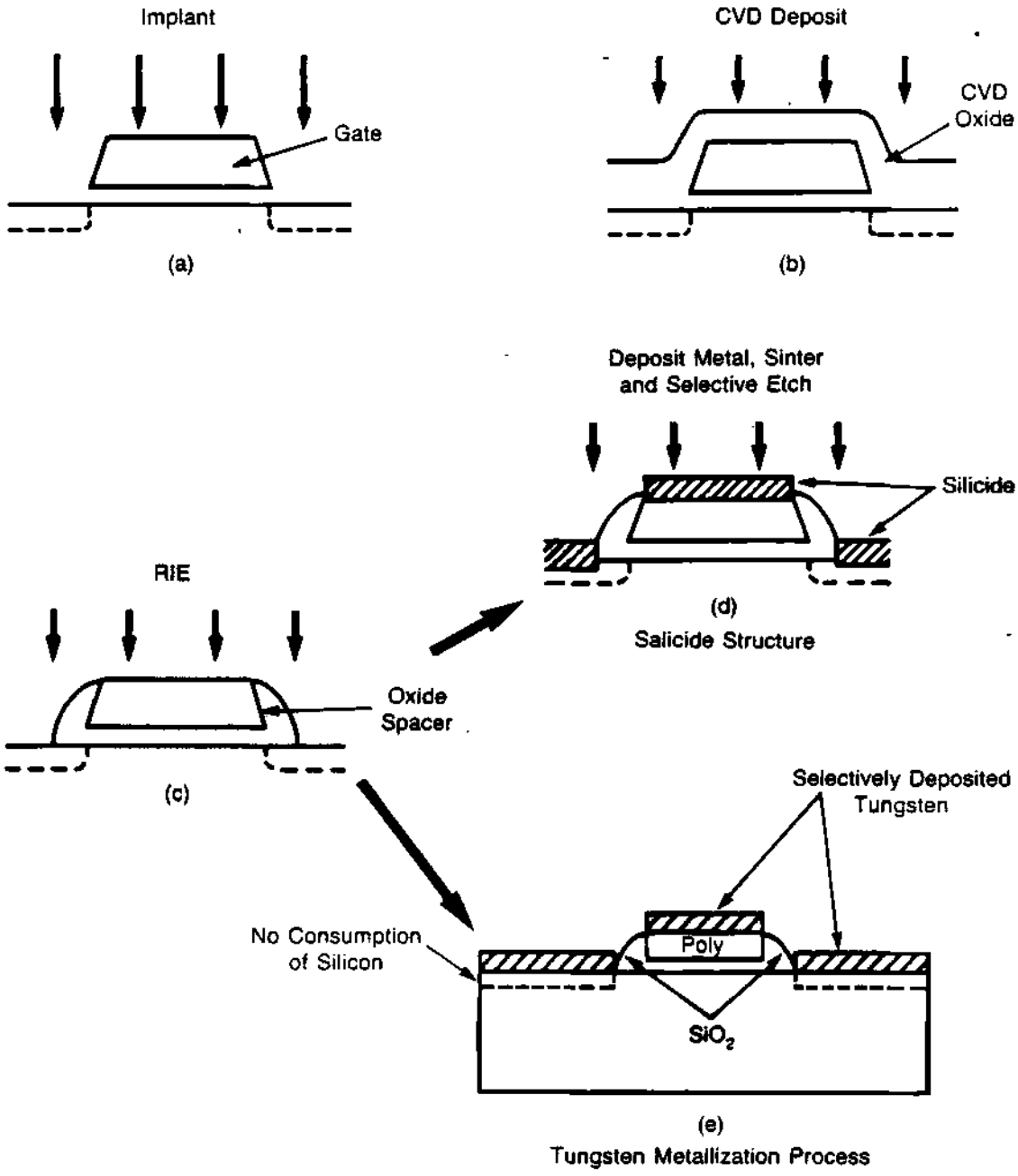
An alternative to using silicide is to use selectively deposited tungsten to form a self-aligned metallized structure. The process steps would be the same through the RIE step. CVD tungsten is selectively deposited on top of the source/drain/gate regions (Figure 23(e)), and because the process is selective, no tungsten will be deposited on the oxide spacer. Silicidation is not performed and no subsequent metal etch is required. The advantages of the metallized structure over the silicide structure are:

- It is a simple and straightforward process.
- No silicon is consumed from the shallow source/drain, since there is no silicidation.
- A contact barrier is formed.
- There is negligible contact resistance, particularly if tungsten is used for contact and metallization.

This metallized structure has application in future VLSI devices, since scaling demands minimum contact resistance.

Figure 23

SELF-ALIGNED SOURCE/DRAIN/GATE STRUCTURE



Source: J.Y. Chen and H. Vanderplas
"Contacts for VLSI"
Xerox, IC Laboratory
Palo Alto, CA

Metallization

Aluminum has several characteristics that have made it a widely used material for interconnection at the device level. These characteristics include ease of deposition and patterning, good bondability, low resistivity, good adhesion to silicon and oxide, and low cost. Three problems with using pure aluminum for metallization are the diffusion of silicon into the aluminum, which can cause junction leakage and shorting as discussed earlier, its lack of resistance to electromigration, and hillock growth.

Electromigration is the mass transport of aluminum along the interconnect line when the line is subject to a high current density. The current through an interconnect line is small in absolute terms but, because of the small cross-section in VLSI devices, current densities on the order of 1 million amperes per square centimeter can result. This can cause electromigration with the net result that voids in the film can form and an open circuit can occur in the interconnect line. As lines get narrower and aspect ratios increase, the metallization at steps and contacts becomes more susceptible to electromigration failure because of the nonuniformity of the deposited aluminum over the steps.

Hillock growth occurs when the aluminum is annealed at temperatures of between 400 to 500 degrees C. This results in a rough surface, which can cause shorts between levels in a multilevel structure. Film resistivity also increases after hillock growth.

Alloying pure aluminum with 1 to 2 percent silicon will alleviate the silicon diffusion problem, while adding copper (2 to 4 percent) will increase the electromigration resistance and reduce hillock growth. However, adding silicon and copper to aluminum increases the resistivity over that of pure aluminum, the added silicon makes bonding more difficult, and adding copper makes etching more difficult. In addition, hillock growth is not completely eliminated. Aluminum/copper films also are more susceptible to corrosion in the presence of chlorine. Because of the etch and corrosion problems of Al/Cu alloys, titanium, which can be dry etched, has been considered as a substitute for copper. An aluminum alloy with 0.1 to 0.2 percent titanium will give the same electromigration resistance as the 2 to 4 percent copper alloy.

Two metallization structures under consideration that use aluminum and titanium are shown in Figure 24. In Figure 24(a), the 10,000A metal film is a homogeneous alloy of Al/1%Si/2.4%Ti, and in Figure 24(b), the film is a layered structure of Al/1%Si and Ti. Compared with Al/Cu alloy films Al/Si/Ti homogeneous films have reduced hillock growth but higher resistivity. The layered structure results in a film with a smooth

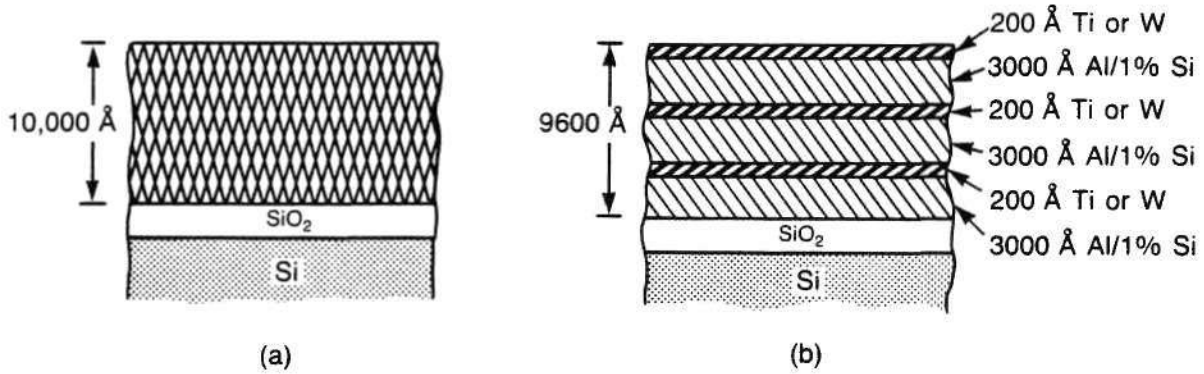
surface with an even further reduction of hillock density and a resistivity that is comparable with Al/Cu films. In both the homogeneous and layered films, silicon is still required because resistivity is increased without it.

Homogeneous alloys of Al/Ti/Si are sputtered. However, because of the very low percentage of titanium used in some films, it is difficult to control the final titanium composition in the deposited film. The layered film, besides having better film characteristics, can be easily deposited by cosputtering, which eliminates the problem of titanium composition in the deposited film.

As contacts and vias get smaller and more steeply sloped, conventionally sputter-deposited aluminum and its alloys become less suitable because of line thinning and nonconformal step coverage. While aluminum alloys will continue to be widely used in VLSI devices, it appears that, below lum geometries, refractory metals will have the edge at least for the first level of metallization. The refractory metal with the most promise for use in metallization is tungsten.

Figure 24

CROSS SECTION SCHEMATIC OF HOMOGENEOUS AND MULTILAYERED STRUCTURES



Source: K.C. Saraswat et. al. "Layered and Homogeneous Films of Aluminum/Silicon With Titanium Zirconium and Tungsten for Multi-Level Interconnects" Proceedings of the IEEE International Electron Devices Meeting 1984

The electromigration resistance for tungsten is about 1,000 times superior to aluminum alloys. The resistivity of tungsten is higher than an aluminum alloy. However, because of the thinning of the aluminum lines over the steps caused by sputter deposition, tungsten may, in practice, have a lower resistivity.

In contrast to aluminum alloys, tungsten metallization films can be deposited with LPCVD processes. Tungsten LPCVD films are conformal and can be deposited over steps and contacts with high aspect ratios with no thinning or degradation of step coverage. An advantage of CVD tungsten over PVD tungsten is that the as-deposited films do not have to be annealed.

A concern associated with LPCVD tungsten is the thin-film effect, which will increase resistivity for films less than 0.75um thick. Another is the adhesion to oxide, although Genus claims to have increased the adherence of films deposited with its tungsten process.

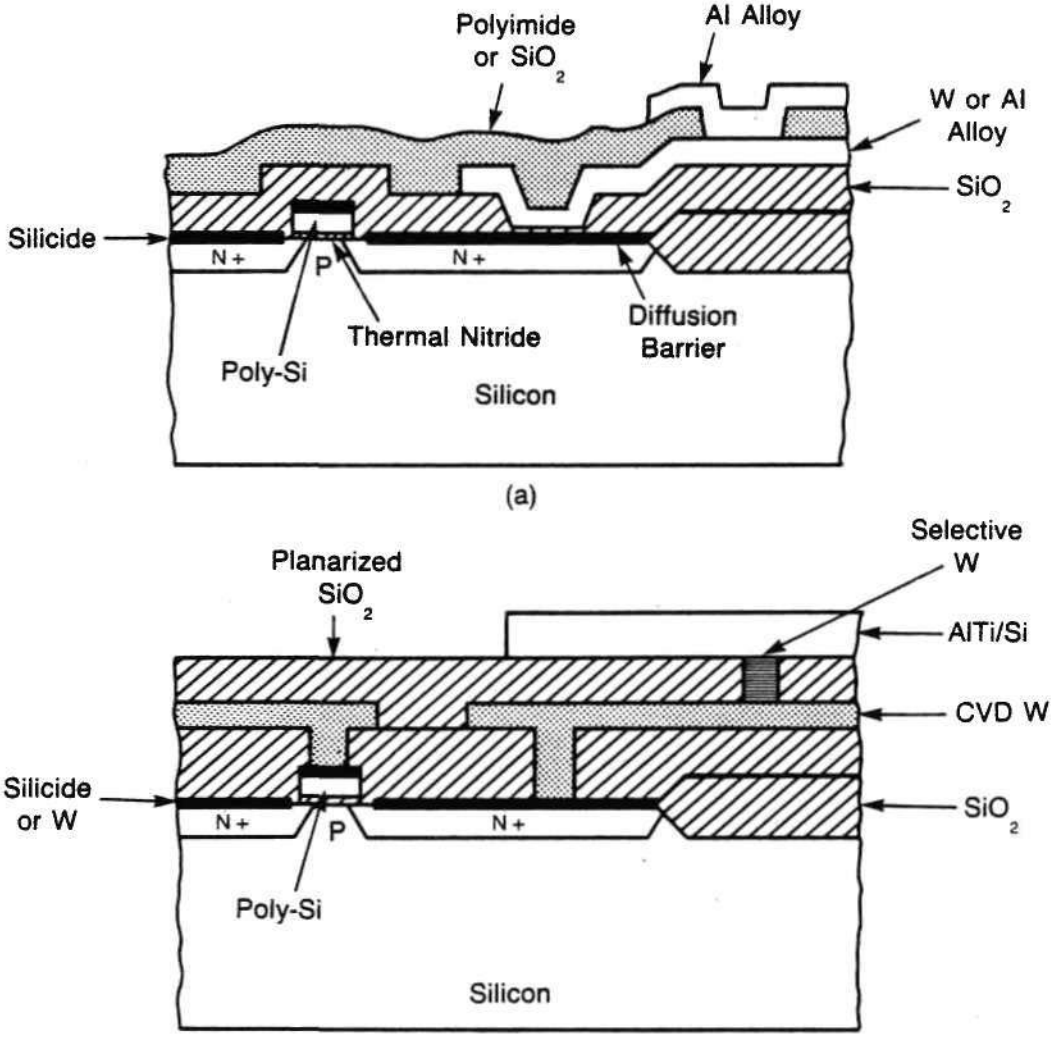
Hewlett-Packard is using two-level tungsten metallization in production of its 32-bit microprocessor family, which includes CPU, clock, RAM, memory controller, and I/O chips. The CPU chip contains 450,000 transistors and uses an NMOS process with minimum 1.5um line and 1.0um space design rules. Tungsten was chosen as the interconnect metal because of its low resistance and its superior electromigration resistance at the high current densities encountered in the circuit. The first level of metallization consists of 2.0um lines and 1.0um spaces of 4,000A of sputtered tungsten. The second layer consists of 5um lines and 3um spaces of 18,000A of CVD tungsten. CVD tungsten was chosen because of the thickness of the second layer and the high deposition rate of CVD. Hewlett-Packard developed its own CVD tungsten reactor because no commercial unit was available at the time.

Another interconnection method uses CVD-deposited tungsten for the first level of metallization with the second level being either the Al/Ti/Si alloy or the Al/Si and Ti layered structure. The aluminum metallization is sputtered onto a planarized dielectric. Again, as with contacts and gate interconnects, it is not clear what the dominant VLSI interconnection technology will be, although the final outcome will be heavily dependent on equipment and process developments.

Figure 25(a) shows a possible interconnection scheme for near-term VLSI devices. Note that the final metal layer is an Al/Si/Cu alloy and that a silicide is deposited over the source/drain regions. Figure 25(b) shows another scheme for future VLSI devices. The top metallization can be either the homogeneous or layer Al/Si/Ti film.

Figure 25

METALLIZATION SCHEMES FOR VLSI DEVICES



Source: K.C. Saraswat
Stanford University
Center for
Integrated Systems

Chemical Vapor Deposition

TRENDS IN INTERLAYER DIELECTRICS

No discussion of interconnection trends would be complete without considering the trends in the interlayer dielectrics used to separate the metallized layers, for the two are intimately related. Desirable qualities in an interlayer dielectric include the following:

- Good crack resistance
- Low compressive stress
- Low pinhole density
- Low defect density
- Conformal step coverage
- Low deposition and anneal temperatures
- Low dielectric constant
- Good barrier to impurity diffusion
- Good adhesion to the metal
- Planarized surface

Currently, interlayer dielectrics are low-temperature APCVD/LPCVD doped oxide (PSG/BPSG) and undoped oxide films or PECVD oxide or nitride films. PECVD films appear to have the advantages of lower pinhole and defect densities and a more conformal step coverage. They also have a better cracking resistance due to the better stress characteristics of PECVD films. Besides these films there is interest in two other CVD films: TEOS, which is a doped or undoped oxide, and silicon oxynitride, which is an SiNiO compound. Of the interlayer dielectrics, interest in BPSG has risen quite rapidly in the past year.

Non-CVD materials being considered for planarization include polymide, which is spun on, and bias-sputtered quartz, which is deposited by physical vapor deposition. Since these are non-CVD materials, however, they will not be discussed here.

Chemical Vapor Deposition

Borophosphosilicate Glass

There is rising interest in the semiconductor industry in using BPSG as a replacement for conventional PSG as an interlayer dielectric over oxide and polysilicon steps. BPSG has been extensively used at RCA in the manufacture of ICs since 1980 and, although not largely discussed in the literature, is more recently being used in production by some other semiconductor manufacturers as well. In addition, DATAQUEST believes that many IC manufacturers are investigating the BPSG process in their development labs. Further, CVD equipment manufacturers are reporting that shipments of equipment configured for the BPSG process are on the rise.

Because of the advantages of BPSG over PSG in VLSI processes, DATAQUEST believes that the semiconductor industry will shift more and more to BPSG as advanced VLSI products go into production.

Why BPSG

Conventional PSG containing 6 to 8 wt%P has been extensively used as an interlayer dielectric over steep oxide and polysilicon steps. When the as-deposited PSG film is heated to temperatures in the 1,000 to 1,100 degrees C range, the PSG flows to form tapered contours over the steep steps. Tapered contours are required to ensure proper film thickness of the subsequently deposited metal interconnect lines. Failure to provide tapered contours could result in line thinning and other anomalies that could degrade device performance.

After the initial flow at 1,000 to 1,100 degrees C, the PSG is patterned with photoresist and etched to form vias to the underlying polysilicon and contact areas. The vias have steep walls and sharp edges and, therefore, the PSG is heated a second time to 1,000 to 1,100 degrees C to allow the film to flow again to form vias with properly smoothed contours. This ensures proper metal coverage in the vias on the subsequent metallization step.

For some IC devices, the 1,000 to 1,100 degrees C temperature required to flow/reflow PSG is unacceptable because the unwanted dopant diffusion that occurs at these high temperatures will affect device performance. In general, the trend is toward lower processing temperatures, particularly in VLSI device applications, where device geometries continue to shrink and junction depths are 0.1um to 0.2um.

The flow/reflow temperature of PSG can be reduced somewhat by substantially increasing the phosphorous content of the film. For example, increasing the phosphorous content from, say, 6.5 percent to 9.5 percent will only reduce the flow/reflow temperature about

50 degrees C. Also, since phosphorous is hygroscopic and the resulting phosphoric acid that might be formed can corrode the aluminum, the higher phosphorous content has the disadvantage of causing potentially serious device reliability problems.

BPSG, on the other hand, has a significantly lower flow/reflow temperature. For instance, BPSG with a 5 wt%B and 4 wt%P (typical film) has a flow/reflow temperature of about 800 to 850 degrees C, or 200 to 250 degrees lower than a typical PSG film. This lower temperature is the driving force behind the shift from PSG to BPSG. Lower process temperatures offer a number of significant advantages, such as:

- Reduction of dopant diffusion that occurs during the flow/reflow steps
- Reduced wafer warpage
- Ability to fabricate radiation-hardened devices

Some phosphorous is still required in the film to provide an alkali-gathering capability. However, BPSG has an additional advantage of having a lower phosphorous content than PSG films. Note that the phosphorous content in a typical BPSG interlayer dielectric film is 4 wt%P, in contrast with 6 to 8 wt%P in a PSG film. Thus, potential corrosion effects are reduced with BPSG films. Even with the lower phosphorous content, BPSG films have been shown to be equal or better alkali getterers than PSG films. Photoresist adhesion to PSG films tends to be poor because of the water absorption of the hygroscopic PSG film. Another advantage of the lower phosphorous content in BPSG films is the improved photoresist adhesion to both BPSG and aluminum films.

Further, BPSG films have relatively low stress characteristics compared with PSG or LTO. PSG has considerably better stress characteristics than LTO and BPSG has even better characteristics than PSG. This means that much thicker and more crack-free BPSG films can be deposited than is possible with PSG or LTO. For example, an application where this would be an advantage would be the use of a thick BPSG passivation layer over a thick (greater than 2um) aluminum interconnect layer. In this application the BPSG is not flowed.

CVD Deposition of BPSG

RCA originally developed the BPSG process, and, as previously mentioned, it has been extensively used in production at RCA since 1980. RCA's BPSG process was developed on atmospheric CVD reactors, and deposition was accomplished by the simultaneous reaction of silane, diborane, and phosphine gases to form a borophosphosilicate glass. This

process using diborane has generally not been suitable for use in conventional tube-type LPCVD reactors because diborane dissociates very fast compared with silane or phosphine, with the result that severe diborane depletion occurs down the length of the tube and, hence, uniformity is poor.

As a consequence, the tube-type LPCVD manufacturers have developed a BPSG process using borontrichloride (BCl_3) instead of diborane. While this process overcomes the diborane depletion problem, there may be other problems to contend with. For instance, there is concern that chlorine trapped in the BPSG film could cause device corrosion problems. In addition, the newer BCl_3 process is not as well understood as the older diborane process.

Table 17 shows the BPSG process used by various APCVD and LPCVD equipment manufacturers. Anicon's reactor, a nontube type, is able to use the diborane process because of the vertical gas flow design. Process Technology also has a gas delivery system that allows the use of diborane in a horizontal LPCVD tube. DATAQUEST believes that there is other work underway to design a gas flow system for tube-type reactors that will overcome the diborane depletion problems encountered with conventional flow systems. This will enable the diborane process to be used in lieu of the BCl_3 process.

Table 17

BPSG PROCESS BY REACTOR TYPE

Company	BPSG Process	Process Gas	Reactor Type
APCVD			
Applied Materials	Yes	Diborane	Belt
Tempress	Yes	Diborane	Horizontal Susceptor
Watkins-Johnson	Yes	Diborane	Belt
LPCVD			
ACS	Yes	BCl_3	Tube
Anicon	Yes	Diborane	Nontube
Bruce	No	-	Tube
Process Technology	Yes	Diborane	Tube
Tempress	No	-	Tube
Thermco	Yes	BCl_3	Tube
Tylan	Yes	BCl_3	Tube

Source: DATAQUEST

Both APCVD and LPCVD equipment manufacturers say that interest in BPSG has been increasing in the last year, and they are reporting that shipments of BPSG-configured equipment are on the rise. In the case of APCVD equipment, approximately 75 percent of shipments are BPSG-configured. For LPCVD equipment, approximately 50 percent of shipments are configured for LTO applications, which include undoped oxide, PSG, and BPSG. Manufacturers report that within the LTO application, BPSG is increasing at the expense of PSG but has not yet reached the percentage that it has in APCVD equipment shipments.

Although recent shipments have been configured for BPSG, this does not necessarily mean that the reactors are being used in production. In the case of APCVD reactors, DATAQUEST believes that a good percentage of the BPSG-configured machines are actually being used in production. Semiconductor manufacturers are using APCVD reactors in production because the process was developed on them and, consequently, there is a greater understanding of the APCVD process. It is this interest in APCVD BPSG that was responsible for the modest growth in the 1984 U.S. market demand for APCVD reactors.

In the case of LPCVD reactors, DATAQUEST believes that few, if any, are being used for BPSG production, but that many semiconductor companies are working to develop a BPSG process in their R&D labs. BPSG can also be deposited in a PECVD reactor, and ASM is offering such a process using diborane.

Both the LPCVD and PECVD processes are new and not as fully characterized as the APCVD process. However, as they become more understood, they will be used more widely because of the advantages of LPCVD and PECVD over atmospheric processes.

TEOS

TEOS is an organic silicon compound that can be used in lieu of silane or dichlorosilane to produce high-quality silicon dioxide interlayer dielectrics. The advantages of TEOS oxide over typical LPCVD oxide include better electrical properties (higher breakdown voltage), better purity, higher density, lower pinhole density, and excellent step coverage. Because of its excellent step coverage, which is almost conformal, TEOS oxide does not need to be flowed like PSG or BPSG.

However, it may be desirable to flow TEOS oxide after the contact windows are formed to provide smooth edges, in which case, TEOS can be phosphorous or doron doped to reflow at temperatures of between 800 and 900 degrees C. An alternative method for making rounded contact edges is to control the edge profiles with a dry etch process. The dry etch method also applies to PSG and BPSG films discussed earlier.

The disadvantages of TEOS are that it is deposited at high temperatures (700 degrees C) and that LPCVD systems using TEOS require more maintenance because of the deposition of the by-products of the reaction.

To deposit TEOS oxide in an LPCVD reactor, TEOS, which is a liquid at room temperature, is contained in a stainless steel ampoule heated to between 30 and 65 degrees C. At these temperatures, TEOS has sufficient vapor pressure so that flow can be controlled by the reactor's mass flow controllers. TEOS oxide can be deposited undoped or doped in situ with phosphorous or boron. Because the addition of small amounts of phosphorous or boron provides a gettering capability, doped TEOS should be the preferred film.

For 2um to 3um devices, the flowed glasses, PSG and BPSG, are adequate. But for the 1um devices, there are penalties to using flowed glasses, and for these geometries, TEOS may be the preferred film for interlayer dielectrics. However, referring to the above discussion on BPSG, it is not clear at this time what film will be used, and there may be applications for both BPSG and TEOS in VLSI device fabrication. AT&T is currently using TEOS in production.

MARKET SUMMARY AND FORECAST

Tables 18 and 19 summarize the market data from the preceding sections on APCVD, LPCVD, and PECVD equipment. Table 18 shows the regional demand for each of the three CVD technologies. As can be seen, there are regional differences in the use of the CVD technologies. For example, 22 percent of the 1984 CVD equipment demand in Japan was for APCVD, while the corresponding share for APCVD in the United States was only 9 percent. On the other hand, Japanese PECVD demand was only 25 percent of total Japanese demand, which was the lowest of the regions. Both of these trends for APCVD and PECVD are in accordance with the earlier discussions of these technologies.

Table 19 presents the same data in another way. The APCVD equipment share of the total worldwide CVD equipment market steadily decreased from 22 percent in 1982 to 13 percent in 1984. LPCVD equipment share increased from 48 percent in 1982 to 58 percent in 1984. Earlier, in the discussion of LPCVD, it was mentioned that opportunities exist in this area. This trend lends further credence to that observation. In the case of PECVD equipment, its share remained flat at 29 percent to 30 percent during the last three years. Table 19 also shows that CVD equipment demand for all technologies in 1984 was very close to the actual semiconductor share by region. For example, in 1984, U.S. companies accounted for 52 percent of worldwide semiconductor production,

Japanese companies for 38 percent, and the ROW area for 10 percent. The CVD equipment demand for these regions in 1984 was 50 percent, 37 percent, and 13 percent, respectively.

Table 18

WORLDWIDE TOTAL CVD EQUIPMENT MARKET DEMAND BY REGION AND TECHNOLOGY
(Millions of Dollars)

	1982		1983		1984	
	Sales	Share	Sales	Share	Sales	Share
United States						
APCVD	$ 8.6	18%	$ 8.8	13%	$ 11.1	9%
LPCVD	23.9	48	37.6	55	75.3	61
PECVD	17.0	34	22.3	32	36.8	30
Total	$ 49.5	100%	$ 68.7	100%	$123.2	100%
Japan						
APCVD	$ 13.3	31%	$ 16.3	27%	$ 20.0	22%
LPCVD	19.7	46	28.9	48	47.5	53
PECVD	10.0	23	14.6	25	22.6	25
Total	$ 43.0	100%	$ 59.8	100%	$ 90.1	100%
ROW						
APCVD	$ 0.8	6%	$ 1.0	6%	$ 1.3	4%
LPCVD	7.0	56	9.9	54	18.7	59
PECVD	4.8	38	7.3	40	11.9	37
Total	$ 12.6	100%	$ 18.2	100%	$ 31.9	100%
Total CVD	$105.1		$146.7		$245.2	

Source: DATAQUEST

Table 19

WORLDWIDE TOTAL CVD EQUIPMENT MARKET DEMAND BY TECHNOLOGY AND REGION
(Millions of Dollars)

	1982		1983		1984	
	Sales	Share	Sales	Share	Sales	Share
Demand by Technology						
APCVD	$ 22.7	22%	$ 26.1	18%	$ 32.4	13%
LPCVD	50.6	48	76.4	52	141.5	58
PECVD	31.8	30	44.2	30	71.3	29
Total	$105.1	100%	$146.7	100%	$245.2	100%
Demand by Region						
United States	$ 49.5	47%	$ 68.7	47%	$123.2	50%
Japan	43.0	41	59.8	41	90.1	37
ROW	12.6	12	18.2	12	31.9	13
Total	$105.1	100%	$146.7	100%	$245.2	100%

Source: DATAQUEST

Figure 26 shows where the CVD equipment was manufactured in 1984. The United States clearly led the world in CVD technology, producing $175.8 M worth or 71.7 percent, of all the CVD equipment produced worldwide. Figure 27 shows where the U.S.-manufactured CVD equipment went. The United States consumed $120.6 million worth (68.6 percent), $39.0 million worth (22.2 percent) was exported to Japan, and $16.2 million worth (9.2 percent) was exported to the ROW areas. Thus, nearly one-third of the CVD equipment manufactured in the United States was exported in 1984. U.S. exports to Japan of $39 million represented 43 percent of the total 1984 Japanese CVD equipment demand of $90.1 million. CVD equipment, therefore, is one area where the United States is still strong in Japan.

Table 20 gives the forecast for CVD equipment from 1985 through 1989. APCVD equipment is expected to grow slowly at an 8.4 percent CAGR over the five years. DATAQUEST believes that while the APCVD market in the United States may have been temporarily boosted by interest in BPSG, there will be a shift to LPCVD or PECVD for BPSG once these processes become established. In Japan, where APCVD has played a larger role in IC manufacturing, there are indications that the Japanese are becoming more interested in PECVD processes to replace some of the APCVD processes. In 1984, APCVD equipment accounted for 13 percent of the total CVD equipment market; in 1989, the APCVD share is expected to be 8 percent.

Figure 26

1984 WORLDWIDE PRODUCTION OF TOTAL CVD EQUIPMENT BY REGION

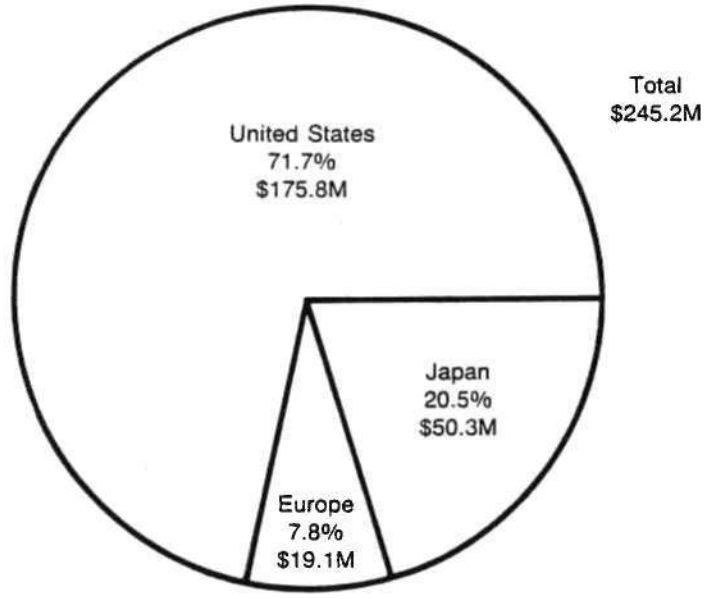
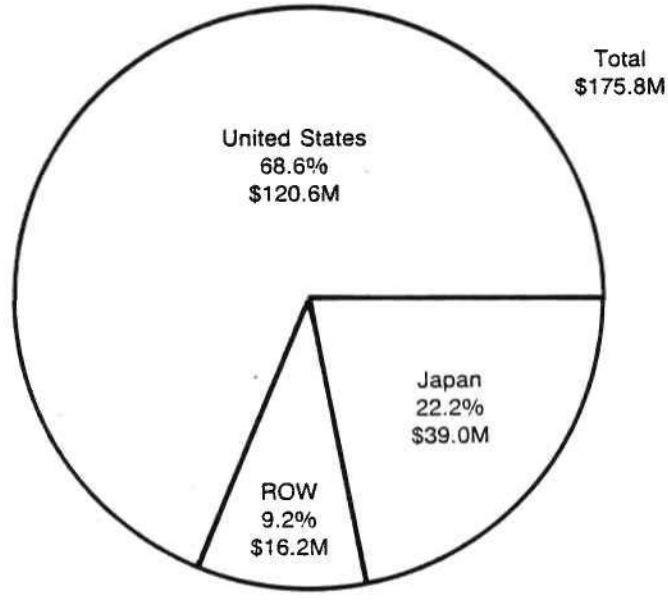


Figure 27

1984 CONSUMPTION OF U.S.-PRODUCED CVD EQUIPMENT BY REGION



Source: DATAQUEST

Table 20

WORLDWIDE CVD EQUIPMENT FORECAST

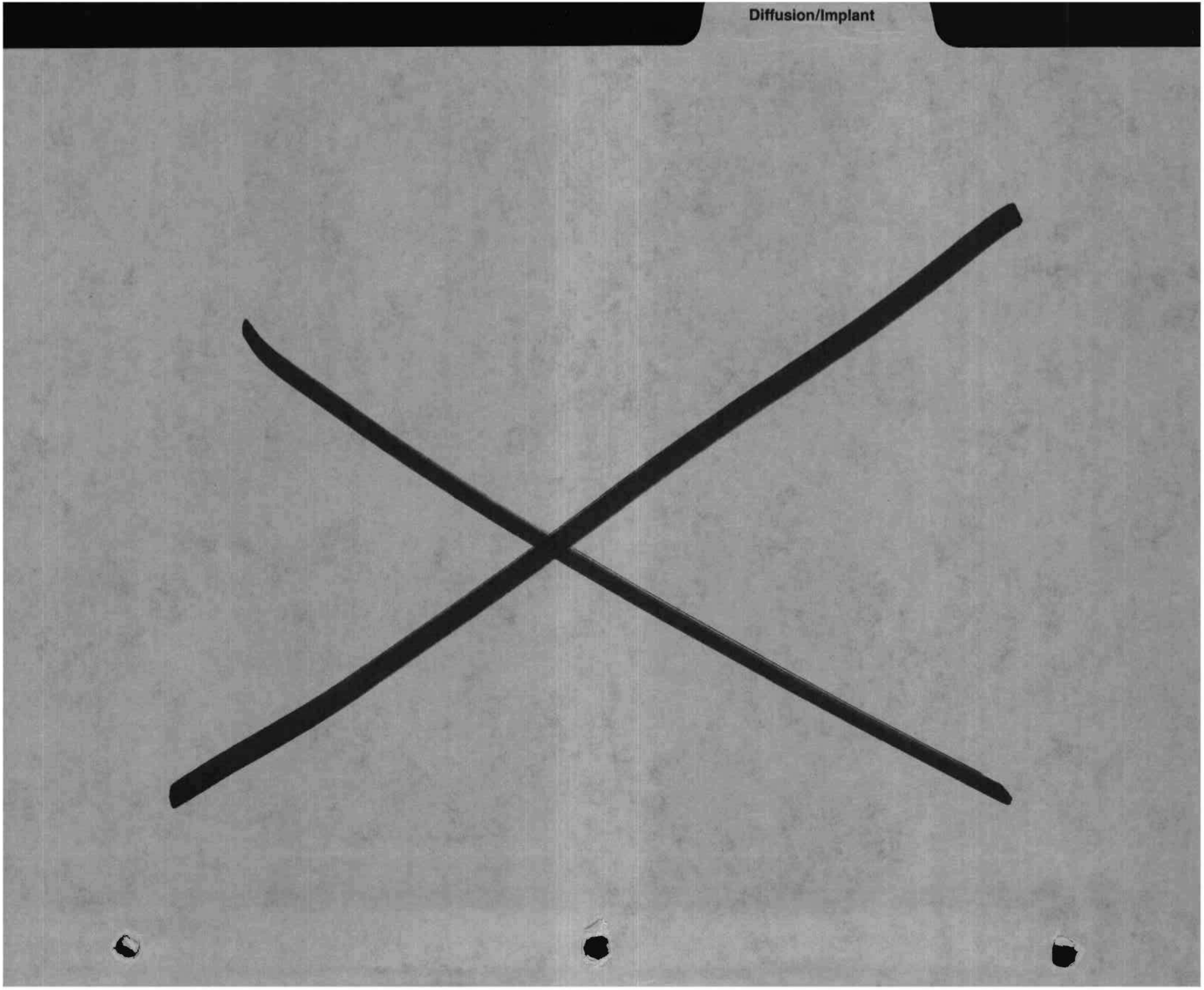
	1982	1983	1984	CAGR (1982-1984)	1985	1986	1987	1988	1989	CAGR (1985-1989)
APCVD	$ 22.7	$ 26.1	$ 32.4	19.5%	$ 29	$ 30	$ 34	$ 38	$ 40	8.4%
LPCVD	50.6	76.4	141.5	67.2%	135	148	207	279	306	22.7%
PECVD	31.8	44.2	71.3	49.7%	64	68	88	110	121	17.4%
Total	$105.1	$146.7	$245.2	52.8%	$228	$246	$329	$427	$467	19.6%

Source: DATAQUEST

The LPCVD market is expected to grow the fastest of the three technologies with a CAGR of 22.7 percent through 1989. The reasons for the interest in LPCVD have been discussed throughout this report, but basically, the reasons can be reduced to a need for different and higher-quality films for VLSI devices. These include interlayer dielectrics and interconnection films, and LPCVD techniques can provide the higher-quality films to meet these needs. Also, there is much interest in looking at alternative approaches to depositing LPCVD films in horizontal tube reactors, such as nontube reactors and vertical tube furnaces. In 1984, the LPCVD share of the CVD equipment market was 58 percent; in 1989, LPCVD equipment is expected to account for 66 percent of all CVD equipment sold.

The market for PECVD equipment is forecast to grow at a CAGR of 17.4 percent through 1989. PECVD, today, is used almost totally for the deposition of silicon nitride and silicon dioxide. While other film processes are being developed by the PECVD manufacturers, DATAQUEST believes that many of the newer films will be deposited by LPCVD techniques and that PECVD will continue to be used for essentially the same applications it is used for today, at least through 1989. The PECVD share of the CVD equipment market is expected to be 26 percent in 1989, 3 percent less than in 1984.

The growth rates expected for 1985 through 1989 are considerably less than the growth rates for 1982 through 1984. DATAQUEST believes that the exceptional growth rates in capital spending that were seen in 1982 through 1984 will not be repeated during the forecast period. For more information on capital spending, please refer to the "Capital Expenditures" section of the Industry Econometrics notebook.



Diffusion/Implant

The following is a list of the material in this section:

- Ion Implantation Equipment

Ion Implantation Equipment

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Ion Implantation Equipment

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Ion Implantation Equipment

OVERVIEW

Ion implantation has rapidly become one of the most important steps in the processing of semiconductor devices. This technology has arisen to satisfy the requirements for better control of device electrical characteristics and for better yields as device geometries have decreased to below 2 microns. For this report, Dataquest segments the ion implant market into three segments: medium-current implanters, high-current implanters, and high-voltage implanters.

In 1985, the market for medium-current implanters was $132 million. Of this, North American semiconductor manufacturers purchased $36 million, the Japanese purchased $72 million, Europeans purchased $16 million, and rest of world (ROW) companies purchased $8 million. Included in the sales for Japanese manufacturers are systems manufactured by TEL-Varian in Japan.

In 1985, the market for high-current implanters was $119 million. Of this, North American semiconductor manufacturers purchased $45 million, Japanese manufacturers purchased $49 million, European companies purchased $20 million, and ROW companies purchased $5 million. The sales numbers for Japanese manufacturers include sales by TEL-Varian and Sumitomo-Eaton.

The total worldwide consumption of medium- and high-current ion implanters in 1985 was $251 million, which represented a 19 percent decline from $309 million in 1984. Consumption in North America was $81 million, which was down 34 percent from $123 million in 1984. Consumption in Japan was $121 million, which was down 14 percent from $140 million in 1984. Consumption in Europe was $36 million, which was flat with 1984 consumption. Consumption in ROW countries was $13 million, which was 30 percent higher than 1983's $10 million.

The 1985 market share of the U.S.-based medium- and high-current system manufacturers accounted for 81 percent of the world market, roughly equal to 82 percent of the previous year. Japanese vendors had the rest of the world share. U.S. manufacturers lost share slightly in high-current markets and gained share slightly in medium-current markets.

Dataquest expects the worldwide medium- and high-current market to fall to $190 million in 1986. This represents a 24 percent decline from 1985. This decline will be the second year of negative growth for this equipment segment specifically and for capital spending in general. The ion implant segment has been hit particularly hard in this recession. Semiconductor manufacturers are burdened with greater than 50 percent overcapacity in several device segments. While in the past manufacturers were reluctant to implant several species on one implanter, preferring to

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dedicate implanters to processes, they have chosen to share implanters between processes and device types during this recession. Worldwide medium- and high-current implanter sales are expected to increase 32 percent in 1987 to $250 million.

TECHNOLOGY

Ion implantation is a method of introducing doping impurities into semiconductor materials. This technology has arisen in response to the need for precision and uniformity in both the amount of dopant and the doping geometries. Ion implantation is an alternative for diffusion doping, which is done in diffusion furnaces.

History

Ion implantation is an example of the application of an existing technology to semiconductor processing. The entrepreneurs who started this technology came out of various particle accelerator laboratories that were doing research in atomic physics at that time.

The first commercial ion implanter was produced by Accelerators, Incorporated (AI), in 1968. However, High Voltage Engineering, Inc. (HVE), had already established a five-year contract, beginning in 1965, with Corning Glass Company to provide ion implanters to Corning's Signetics subsidiary. During the late 1960s and early 1970s, commercial implanters were produced by HVE, Lintott Engineering, and Ortec.

Since its early formation, there have been considerable changes in the market structure. Table 1 gives a brief history of some of the significant events in this marketplace. In 1970, GCA acquired Ortec and, subsequently, abandoned the business in 1981. In 1971, some of the technologists at HVE left to form Extrion, which was subsequently bought by Varian in 1975. In 1978, some of the founders of Extrion left to form Nova with financial support from Cutler-Hammer. Eaton subsequently acquired Cutler-Hammer and has absorbed Nova under the Eaton logo. In 1980, Lintott was bought by Applied Materials. Applied Materials suspended production in 1983 in order to develop a new product for introduction in 1985. In 1980, Veeco bought AI. Throughout this period, several Japanese companies were developing their implant technology, and they now have a healthy share of the Japanese market.

Ion Implantation Equipment

Table 1

BRIEF CHRONOLOGY OF ION IMPLANTERS

1968	Accelerators, Incorporated (AI), was founded. It manufactured low-current postacceleration 80-400 KeV equipment.
1970	Ortec manufactured 200 KeV preacceleration equipment. Lintott (United Kingdom) used mass separator as a high-current ion implanter.
	GCA acquired the Ortec implanter operation.
1971	Extrion was founded by a group from High Voltage Engineering and funded by Glouchester Engineering. It manufactured low-current, 150, 200, and 400 KeV preacceleration equipment.
1974	Extrion manufactured a 100 KeV, dedicated implanter.
	Eltek was started by a group from AI to manufacture 100 KeV, dedicated implanters.
1975	Varian acquired Extrion.
	Cutler-Hammer acquired Eltek and made it part of Kasper.
	Extrion manufactured a medium-current, 200 KeV implanter.
	Extrion manufactured a high-current, 200 KeV implanter.
	Kasper manufactured a low-current, 200 KeV implanter.
1977	AI manufactured a medium-current preacceleration, 200 KeV implanter.
	Lintott manufactured a high-current, 200 KeV implanter.
1978	Nova was founded by a group from Extrion and funded by Cutler-Hammer. Eaton acquired Cutler-Hammer.
1980	Veeco acquired AI.
	Eaton/Nova manufactured a very high-current, 80 KeV implanter (pre-dep).

(Continued)

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Ion Implantation Equipment

Table 1 (Continued)

BRIEF CHRONOLOGY OF ION IMPLANTERS

1980	Applied Materials acquired Lintott and named the new company, Applied Implant Technology (AIT).
	Extrion manufactured a very high-current, 80 KeV implanter (pre-dep).
1981	Extrion manufactured a very high-current, 120 KeV implanter (pre-dep).
	AIT manufactured a very high-current, 120 KeV implanter (pre-dep).
	GCA discontinued manufacturing implanters.
1982	AIT discontinued manufacturing operations to place efforts on a next-generation product.
1983	Eaton/Nova manufactured a very high-current, 160 KeV implanter (pre-dep).
1984	Veeco introduced a very high-current, 120 KeV implanter (pre-dep).
1985	Applied Materials introduced its Precision Implant 9000 with capability for 30 milliamps of beam current.
1986	Eaton and Varian introduced their new-generation high-current systems with capability for 20 milliamps of beam current.

Source: Sini Systems
Dataquest
December 1986

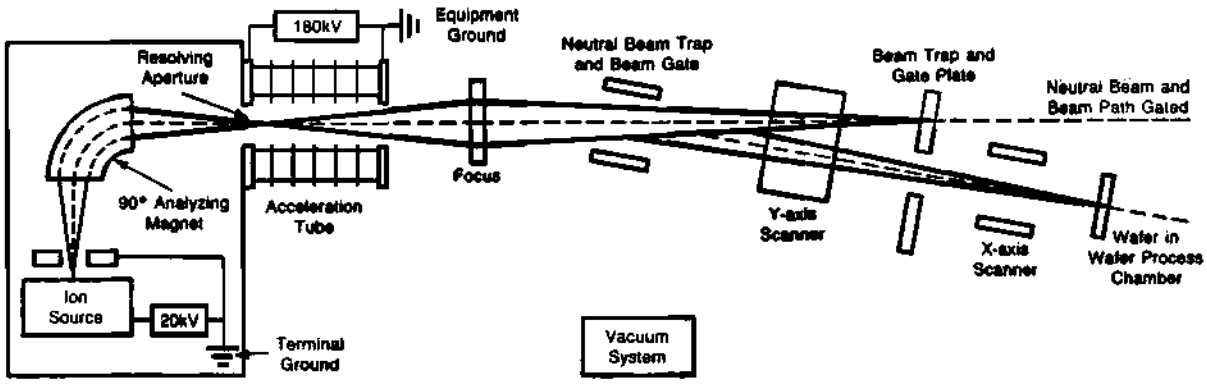
Machine Configuration

Figure 1 illustrates the basic configuration of an ion implanter. The basic elements are the source, the extractor, the analyzer magnet, the accelerator column, the scanning mechanism, the end station, and the monitoring instrumentation. In addition, implanters require a vacuum system to maintain a very high vacuum. The following section describes the basic operation. . . .

Ion Implantation Equipment

Figure 1

TYPICAL ION IMPLANTER CONFIGURATION



Source: Semiconductor Integrated Circuit Techniques
Fairchild Corporation

Theory of Operation

The physical theories involved in ion implantation include the creation of charged particles, the acceleration of those charged species (ions) through an electrostatic field, and the uniform distribution of those ions over the target (usually silicon or gallium arsenide wafers). In order to create an unimpeded beam, a very high vacuum is required. Most ion implanters have several vacuum pumps situated along the beam line to achieve vacuums of 10^{-5} Torr and lower.

The species of choice is produced in the source, extracted, and preaccelerated toward the analyzer magnet. Since a given process requires a specific species with a predetermined charge, the analyzer magnet current is set to choose this ion. The magnetic current, and thus the magnetic field, will cause the ion with the correct charge-to-mass ratio to traverse the magnet with the correct trajectory in order to emerge from the other end of the magnet. Ions with improper charge-to-mass ratios will have improper curvatures and, thus, will be lost on the walls of the magnet.

After emerging from the analyzer magnet, the ion beam is post-accelerated toward the wafer. Some configurations vary from system to system, such as the use of focusing plates, scanning plates, beam gates, and neutral beam traps. These will be discussed in the following sections.

Ion Implantation Equipment

The ion beam, which comprises ions with the proper charge and energy, is scanned across the wafer, implanting the ions into the substrate at the required depth. These ions become the dopant that will give the semiconductor device the proper electrical characteristics. However, the ions do not occupy crystal lattice sites immediately after implantation. They must be activated by the annealing of the wafer. Typical annealing is at 1000°C for 30 minutes. However, recent developments in equipment such as rapid thermal processors are allowing annealing to be done in approximately 10 seconds. Annealing also repairs the damage to the crystal lattice that was caused by the beam.

Sources

There are three types of sources used in ion implantation--solid, liquid, and gaseous. Dataquest estimates that approximately 67 percent of the installed implanters use a gas source. High-current implanters (which will be discussed later) almost exclusively use the solid type. Liquid sources are not used in any commercially available production ion implanter so they are not discussed here.

Solid Sources

The most widely used solid source is the Freeman Source. The basic mechanism is the sublimation of the solid dopant--which may be in the form of pellets, lumps, or pressed charges--into vapor. The sublimation takes place at pressures of 10^{-5} to 10^{-6} Torr and depends on the vapor pressure of the solid dopant. This vapor is passed over a tungsten filament at 3000°C to 4000°C to create a plasma discharge. The ions from the plasma are then electrostatically extracted into the beam line. Historically, all dopants except boron, which has a low vapor pressure, were available in solid form. Recently, boron has also become available in solid form.

The advantages of solid dopants are safety, purity, and beam stability. Since they are not under pressure, there is less potential for them to leak into the atmosphere. Also, since gases come in metal containers, any residual water vapor in these containers, when combined with the dopants, can eventually cause corrosion of the source and beam line components. Solid sources obviate this problem. In addition, the presence of water vapor in the gas bottles can cause variations in the beam current. This type of variation is not present with solid sources.

Gas Sources

The use of gas sources is the most widespread and the best understood. The most widely used gas source is the Penning Diode. In this application, gas is introduced into the source chamber where a tungsten filament creates a plasma discharge. The plasma ions are then extracted into the beam line. All dopants are available in gaseous form.

The problems with beam line corrosion and current stability can be reduced by careful choice of the gas vendor, since refilling procedures can introduce impurities and water vapor into the bottles. However, there is growing concern in the semiconductor industry about the handling of hazardous materials. Although great care is taken to minimize danger to personnel in the event of a gas leak, Dataquest believes that there will be a steady shift to the use of all solid sources.

Beam Line

The beam line can have various configurations. Starting with the extractor, the beam can be preaccelerated or not. The extractor can provide adequate acceleration prior to the analyzer magnet. If the beam is preaccelerated, it is not usually postaccelerated. After acceleration, the beam may go through vertical and horizontal focusing plates. In most cases, the analyzing magnet provides beam focusing.

The next component is the scanning plates that are used in beam scanning and hybrid scanning methods, which will be discussed later. The scanning plates may be electrostatic or electromagnetic. By varying the electrical power to these plates, the ion beam is scanned across the wafer, depositing the beam uniformly.

It is at the scanning plates that a neutral offset can be added to the beam. To create the offset, the vertical or horizontal scanning plates bend the ion beam so that neutral particles continue straight ahead and miss the wafer. Such an offset is required to trap the neutral (uncharged) particles from the beam. These particles are produced when an ion collides with a residual gas molecule. Such collisions occur quite often and can account for 1 percent of the total ions in the beam. The new particles formed as a result of collisions will have nearly full energy but no charge. Since these uncharged particles would not be affected by a scanning mechanism, they would cause a nonuniformity at the center of the wafer as the other 99 percent of the beam scans across the wafer. The nonuniformity could be 10 to 100 percent, depending on the type of scanning method used.

The beam then goes through a beam aperture. The aperture helps eliminate unwanted particles from impinging on the wafer. These particles could be created by collisions with air molecules or with the hardware in the beam line. The aperture also shields the wafer from unwanted magnetic and electrostatic fields.

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Scanning

We will discuss three types of beam scanning in this section; beam scanning (also known as x-y scan or electrostatic scan), hybrid scanning, and wafer scanning (also known as mechanical scan). Table 2 lists the types of scanning used in the major ion implanters in use today.

Table 2

SCANNING METHODS

Machine	Machine Type	Scan Type
AIT-IIIA	High	Hybrid
Nova NV-10 series	High	Wafer
Extrion 80-10	High	Hybrid
Extrion 120-10	High	Hybrid
Extrion 160-10	High	Hybrid
Extrion DF-3000	Medium	Beam
Extrion 350D	Medium	Beam
Eaton NV-3206	Medium	Beam
Applied Materials 9000	High	Wafer

Source: Solid State Technology
February 1985
Dataquest
December 1986

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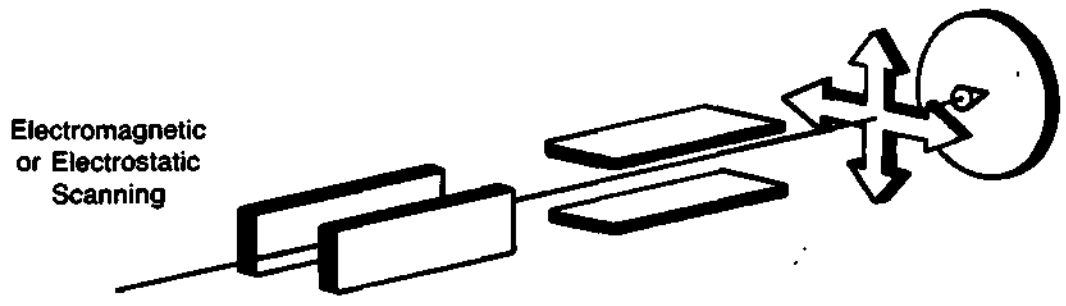
Beam Scanning

In the beam scan, the wafer is kept stationary and the beam is swept in vertical and horizontal planes by the electrostatic or electromagnet scanning plates, writing a single wafer at a time. This configuration is illustrated in Figure 2. Since the energy deposited on the wafer will heat the wafer, this approach is suitable for medium-current systems where wafer heating can be maintained to within acceptable levels. For high-current applications, in order to maintain photoresist on the wafer below critical temperatures (nominally 100°C), the beam energy must be spread over many wafers in a batch. For this reason, beam scanning is not used in high-current applications, and manufacturers have resorted to hybrid and mechanical scanning to spread the beam energy over the wafer in the batch.

Figure 2

BEAM SCANNING



Source: Yield Assurance Seminar
Prometrix Corporation 1984
Wayne O'Neill, Sini Systems

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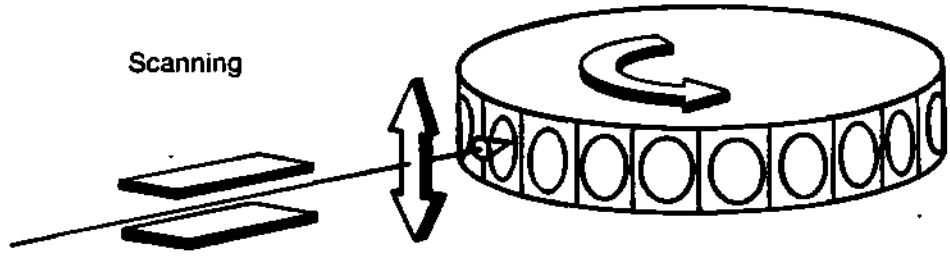
Hybrid Scanning

In hybrid scanning, the wafers are loaded onto a rotating drum or wheel. This is illustrated in Figure 3. The drum rotates rapidly moving the wafers across the beam path. As the drum or wheel rotates in one direction, the beam is scanned in the other, thus doping the whole wafer. Since the beam is scanned in both beam and hybrid scanning methods, neutrals will become a problem with respect to uniformity. It is for this reason that these two approaches use neutral beam traps as described above. Hybrid scanning enjoys the advantage of distributing the beam over a batch of wafers, thus allowing higher currents and energies to be used in implantation.

Figure 3

HYBRID SCANNING



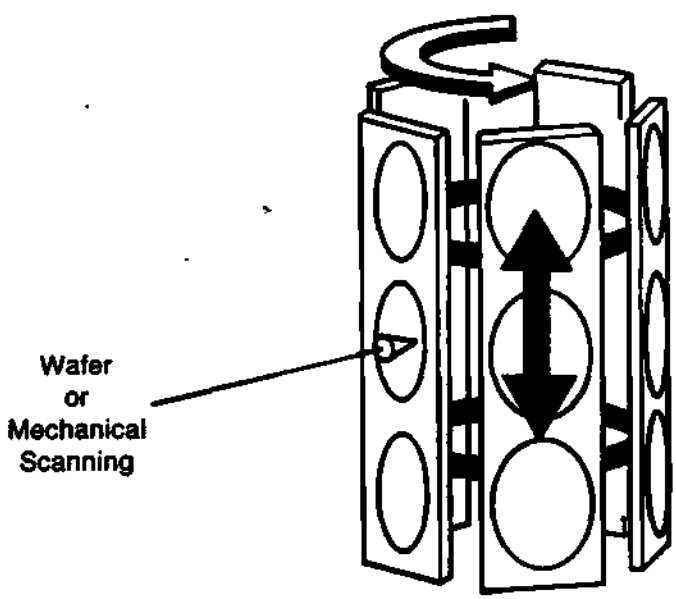
Source: Yield Assurance Seminar
Prometrix Corporation 1984
Wayne O'Neill, Sini Systems

Wafer Scanning

In wafer scanning, the wafers are also located on a rapidly spinning wheel or drum. This arrangement is illustrated in Figure 4. As the wheel or drum spins in one direction, it is also moved up and down to ensure that the entire wafer is covered with the beam. Since the beam is not scanned, this approach does not require the addition of a neutral beam trap. It also enjoys the advantage of distributing the beam over a batch of wafers, thus allowing higher currents and energies to be used in implantation.

Figure 4

WAFER SCANNING



Source: Yield Assurance Seminar
Prometrix Corporation 1984
Wayne O'Neill, Sini Systems

Monitoring and Control

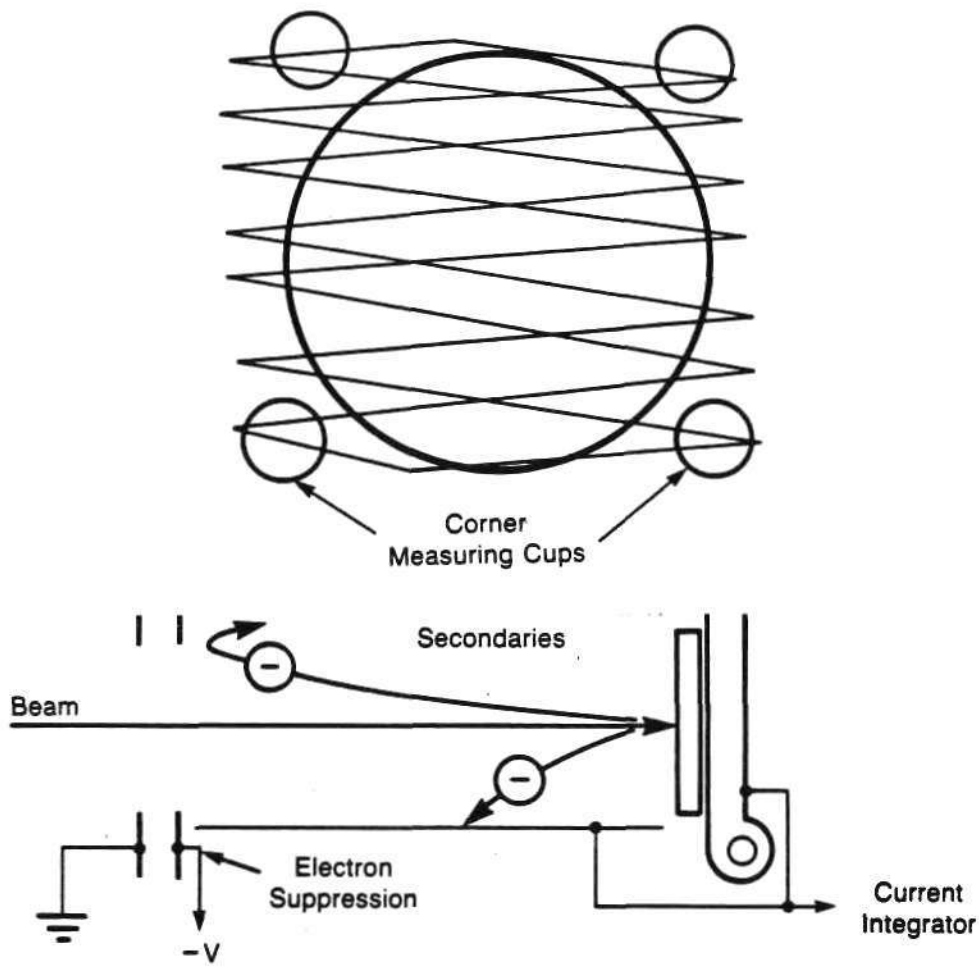
The uniformity of dose across the wafer is a critical factor in the monitoring and control of the beam. The method used for monitoring the beam is the faraday cup, a current-collecting electrode that is situated in various configurations in the beam, depending on the monitoring requirements.

Ion Implantation Equipment

In the electrostatic scan systems, faraday cups are placed to measure the amount of over-travel of the beam. This arrangement is illustrated in Figure 5. The amount of over-scan is critical for dose uniformity.

Figure 5

FARADAY CUP



Source: Yield Assurance Seminar
Prometrix Corporation 1984
Wayne O'Neill, Sini Systems

In hybrid and wafer scan systems, a slit in the carousel or wheel respectively allows the beam to fall on a faraday cup behind the carousel or wheel on each revolution. This gives a measure of the amount of current per revolution. In the wafer scan systems, this signal is used to index the wheel up or down. Such indexing is necessary to compensate for differing radial velocities from center to periphery across the wheel.

For wafers with insulating films, large surface charges can accumulate during implantation. These charges can damage devices on the wafer and can cause variations in the beam diameter, contributing to severe nonuniformities. To alleviate this effect, electron flooding, the injection of low-energy electrons near the wafer, is used to neutralize the build-up of positive charge on the wafer surface. Electron flooding must be done in such a way as to not affect the dosimetry.

PROCESS

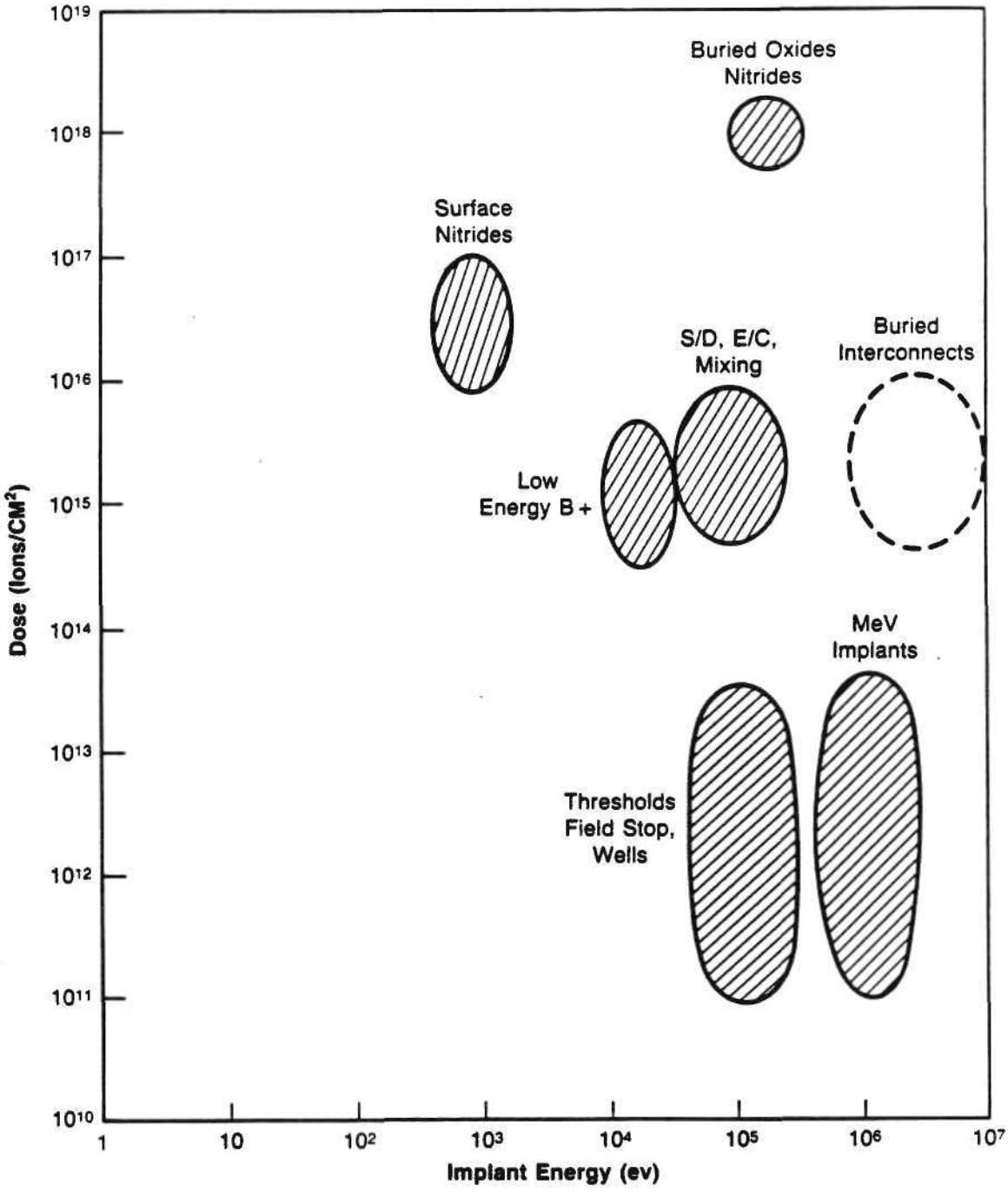
Ion implantation has grown as an alternative to diffusion. Diffusion is done in furnace tubes and consists of pre-deposition (pre-dep) and drive-in. In pre-dep, the dopant is deposited on the wafer surface. These pre-dep wafers are placed into the furnace for the drive-in process. At drive-in, the furnace temperature is raised to 1000 to 1200°C for one to two hours, depending on the required diffusion depth. Diffusion of the dopant occurs isotropically into the wafer, and will penetrate to regions beneath masked areas on the wafer. Because of this out-diffusion and the concomitant lack of control of junctions, the use of diffusion tubes for VLSI integrated circuit production is becoming inadequate. Ion implantation is preferred over diffusion because of better control of dopant distribution, superior uniformity, and better precision in controlling the actual dosage.

Since the advent of implantation for semiconductor manufacturing, processing has evolved along with system design. As different process requirements have unfolded, the current and voltage capability of implanters have changed to meet them. The success of MOS processing with its requirements for source/drain doping has been made feasible with the development of high-current implanters. Semiconductor manufacturers continue to find new implanter applications for their production processes. Figure 6 illustrates the regions of processing with respect to dose and energy.

Ion Implantation Equipment

Figure 6

PROCESS APPLICATIONS



Source: ASEE Seminar, 1985
Dipu Pramanic, Gould/AMI

Ion Implantation Equipment

Bipolar Processing

A typical bipolar device with the concomitant processes is shown in Figure 7. Since bipolar devices cannot be packed as densely as MOS devices, the line geometries are not as small. Therefore, junction dimensions are not as critical and the use of diffusion still prevails. However, the use of implant has accelerated in recent years and the number of implant steps has increased to an average of six per wafer.

Historically, ion implant energies were not adequate to penetrate to the depths required for bipolar processing. As line geometries and junction depths decreased, they became amenable to implantation, which has also increased the average number of implants per wafer.

Medium-current implanters can be used economically for doses of less than 10^{14} ions per cm^2. At higher doses, the throughput of the implanter becomes too low to be cost-effective. For this reason, emitters, collectors, and buried collectors were universally done in diffusion furnaces. With the advent of high-current implanters, these structures are routinely done by implantation.

Since high-current implanters are also capable of medium-current applications, their application reaches into regions held by medium-current systems (i.e., for bases, isolation, and resistors). This utility also applies to MOS processing, which helps to explain the greater growth in sales for high-current than for medium-current implanters.

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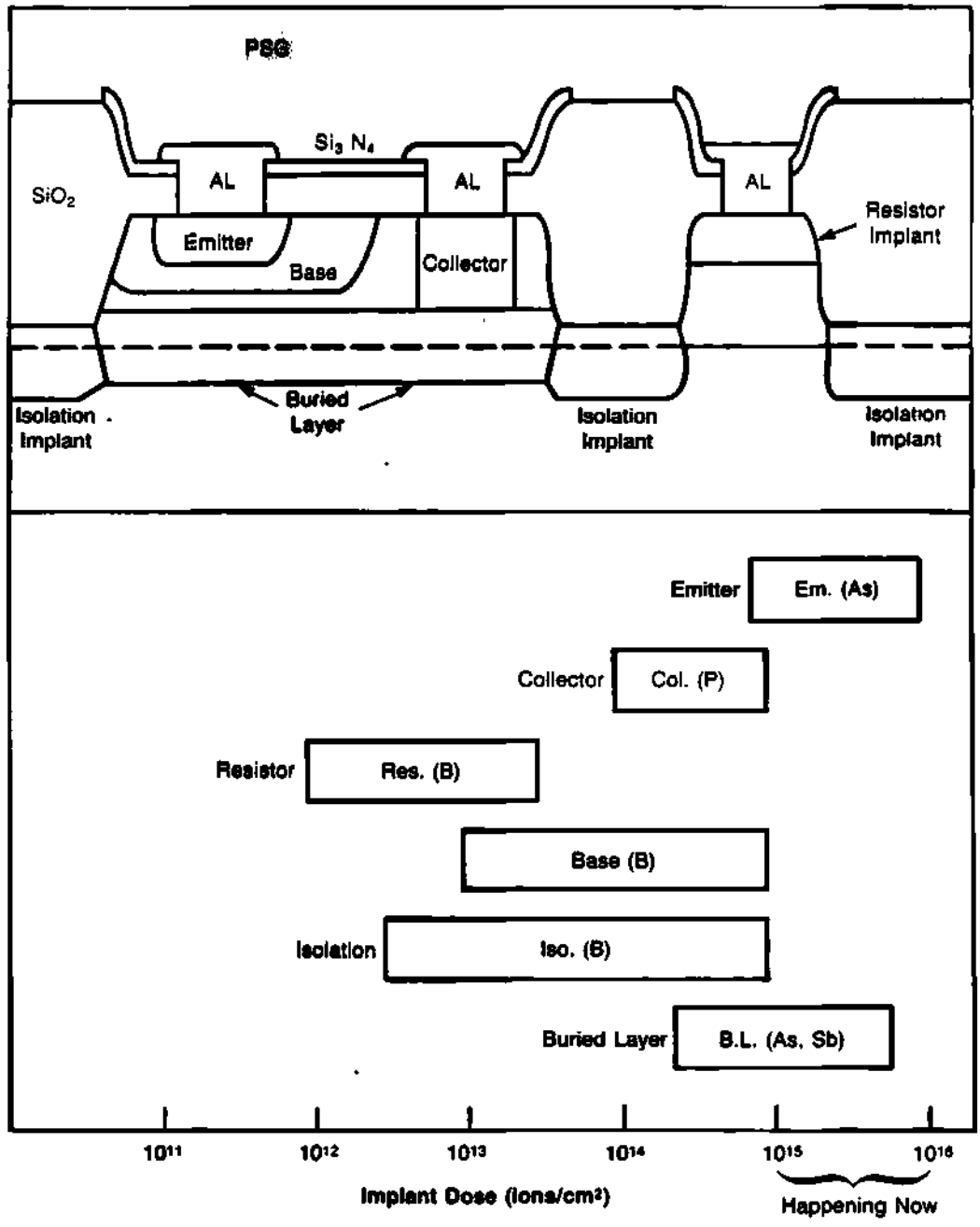
Figure 7

BIPOLAR PROCESSING



Source: Integrated Circuit Technologies for the 1980s, K.A. Pickar Signetics, February 1982

Implanted Resistors

Diffused resistors generally have poor tolerances and, since ion implantation controls impurities precisely, implants improve resistor tolerances. Ion implantation at low doses also may be used to create high-resistance, low-power resistors.

Phantom-Layer Deposition

Phantom-layer deposition is a backside implant that lowers high-starting resistivity and may be used to ensure good backside ohmic contact. It also eliminates the possibility that a manufacturer will create a diode on the backside of the silicon in the process of soldering the devices. This creation of a diode occurs because the material used in soldering is itself a dopant.

Buried-Layer Implant

Bipolar devices commonly use a buried layer, or highly doped layer, and then grow an epitaxial layer over it. The buried layer makes it possible to maintain a low-collector resistivity without degrading the breakdown voltage. The impurity types and profiles that are possible with ion implantation may help to reduce the auto-doping problem as well.

Base and Emitter Predepositions

Manufacturers use ion implantation to implant bases at 10^{13} ions/cm^2 to 10^{15} ions/cm^2 and emitters at 10^{15} ions/cm^2 to 10^{16} ions/cm^2 on critical-geometry bipolar devices.

Backside Gettering

Manufacturers typically implant Argon ions at 10^{13} ions/cm^2 to 10^{15} ions/cm^2 into the backside of the wafer. The damage caused to the lattice by the ions provide gettering sites for the capture of metallic impurities in the substrate. Such impurities degrade the devices and lower the probe yields on the wafer.

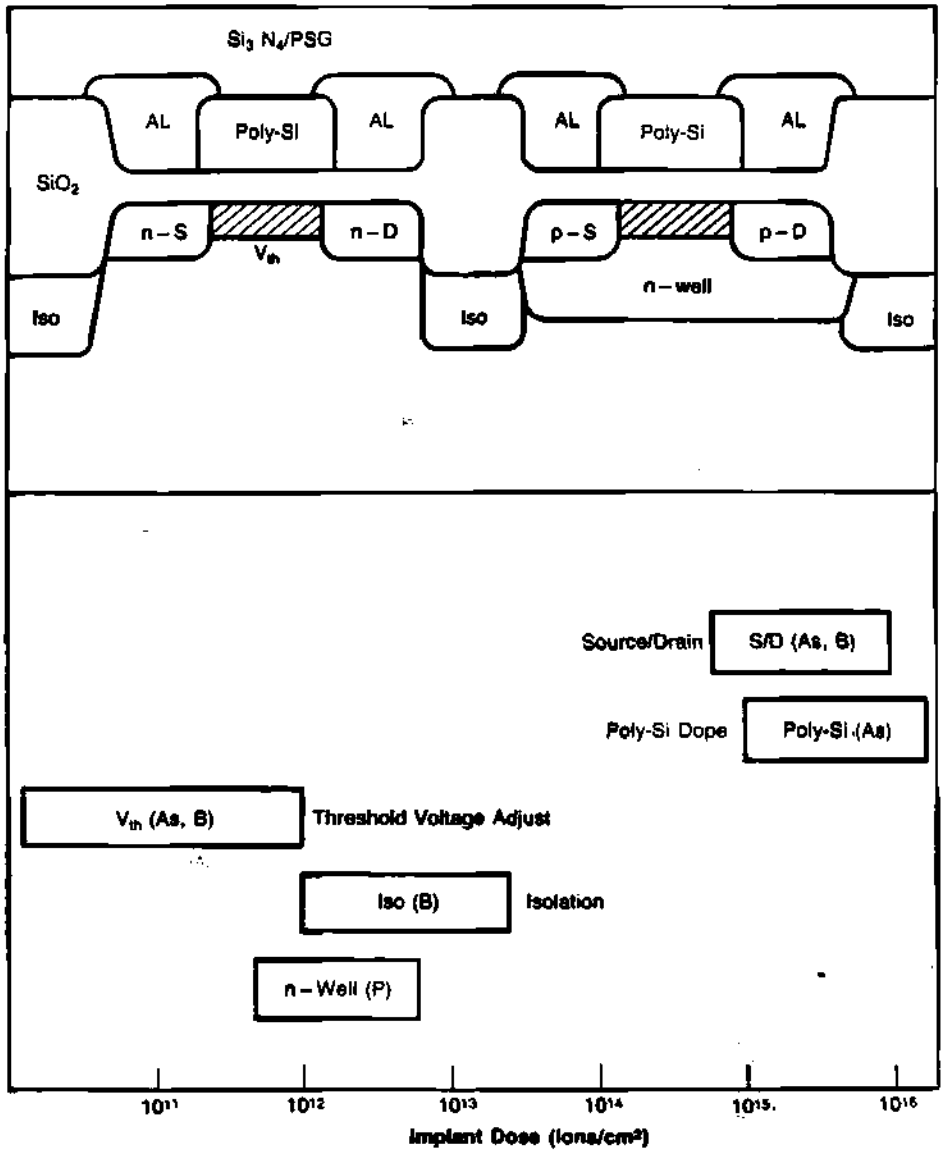
MOS Processing

Figure 8 shows a typical MOS device (in this case, CMOS) with the concomitant energy/dose regions. Originally, implant was used universally for the threshold adjust and also had some usage in N-well and isolation doping. With the increased packing densities for MOS devices, requirements for implant extended into the source/drain and polysilicon doping applications. These high-dose applications require higher currents and are largely responsible for the rapid growth of high-current implanters. The evolution of MOS technology has been made possible by the pacing developments in implant systems.

Ion Implantation Equipment

Figure 8

MOS PROCESSING



Source: Integrated Circuit Technologies for the 1980s, K.A. Pickar Signetics, February 1982

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MOS Threshold Adjustment

Short implants are used to control surface dopant concentrations and to adjust the threshold voltages of MOS devices. The more control a manufacturer has over the threshold of a device, the better the performance of the device. It is possible to have different thresholds for different transistors on the same chip. We observed one process that includes five threshold adjustments: two on the depletion device, two on the enhancement device, and one field threshold adjustment. Threshold adjustment was not possible before the advent of ion implantation.

Capacitor Implant

Some manufacturers apparently improve the performance of MOS devices by using an implant through the oxide of capacitors. The thinner the oxide, the larger the capacitance, and ion implantation helps the manufacturer achieve a high threshold and a high surface concentration.

Source and Drain Implant

Source and drain implant as a substitute for furnace predeposition on small-geometry, MOS devices is currently a very popular process. Manufacturers use 50 to 100 KeV energies at surface doses of 10^{15} ions/cm^2 to 10^{16} ions/cm^2.

P-Well in CMOS Devices

The P-well is implanted in N-type silicon to permit the fabrication of N-channel and P-channel devices on the same substrate. There are other variations on this application such as N-wells in P-type silicon and twin-tub implantations.

Emerging Applications

Semiconductor manufacturers are continually finding new applications for ion implantation. These new uses are first characterized in their labs and pilot lines and then transferred into production. The applications listed below are in various stages of acceptance in production processing.

ROM Programming

Vendors of application-specific ICs (ASICs) compete on the basis of delivery. For read-only memories, the codes are set early in the processing cycle by adjusting threshold voltage, formation of gates, or formation of through-hole contacts. Therefore, delivery time is limited to the total process cycle time, which is generally 6 to 10 weeks. With

ion implantation, the ROM can be fabricated through the first metallization step as a standard device. Then, using a high-voltage implanter, the threshold voltages can be adjusted by implanting through the active regions of the device.

Using this method, vendors can provide devices in one to two days after receiving the programming codes from the buyer. This method also has the advantage of providing a very high-yielding ROM process up to metallization, thereby decreasing costs.

Buried N-grid for Soft Error Reduction

Soft errors are created in memory cells when ionizing radiation forms electron-hole pairs in the silicon substrate, after which these pairs migrate to the storage area in the cell. This effect can be circumvented by the creation of a buried grid 1 to 2 microns below the memory device. The buried grid will trap any mobile ions that have been created in the substrate and conduct them away through a biased contact.

The grid is formed in two steps using a high-voltage ion implanter. First, boron is implanted at 2 MeV through an oxide mask. A second step, after the oxide mask is removed, requires the implantation of phosphorous at the same energy level to create a compensated N-grid below the enhanced P-grid. The fabrication of the active device continues after the formation of the buried grid.

Buried Layer (CMOS Latch-up)

Much research and development is being directed toward solving the problem of latch-up in modern CMOS circuits. Latch-up occurs when the N-well and P-well regions in a CMOS device are close enough to form an n-p-n-p device structure. With this structure, a voltage pulse in the substrate can switch on the device, as in a silicon-controlled rectifier (SCR), and effectively short the power supply to ground. This destroys the device.

This effect can be minimized by biasing the substrate at some negative potential that would block the voltage excursion or by building the device on a lightly doped epitaxial layer over a highly doped buried layer. Using high-voltage implantation, latch-up can be prevented with a buried layer without the need for building an epitaxial layer.

In this case, first the N-well is created by the implantation and drive-in of phosphorus. The oxide mask is then removed, and a buried layer is created by implanting boron into the substrate 1.5- to 3-microns below the N-well. This implantation is done at 1 to 4 MeV at a dose of about 10^{13} ion/cm^2. This method obviates the out-diffusion of the buried layer into the epitaxial layer that occurs with the epitaxial method, affording much better control of the junction.

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Retrograde Wells

In CMOS devices, a doped well, in which the dopant profile increases from a value on the surface to a peak value within the silicon, is called a retrograde well. This unique profile can provide a reduced susceptibility to latch-up. To achieve this profile, high-voltage implanters are used to deposit dopant at about 1.5 microns within the silicon surface. A typical implant would be boron at 1 MeV at a dose of 3×10^{12} ions/cm^2.

A marked advantage with this process is the reduced anneal time. The formation of a 2-micron deep well, with conventional pre-dep and drive-in, can require 40 hours of anneal at 1050° C. The anneal after high-voltage implantation requires only 30 minutes at the same temperature.

Annealing

Annealing accomplishes three purposes: it activates ions that have come to rest in silicon during ion implantation, it can drive-in dopant to the required depth for the formation of wells in MOS devices, and it heals defects or lattice damage caused by the ion implant process. Ions are activated when they occupy lattice sites and form bonds with the silicon atoms.

Furnace Annealing

The predominant method of activating the ions and healing the damaged regions is furnace annealing, which the industry discovered in 1972 nearly four years after the development of ion implantation. The method is not very precise, however, and can change the dopant profiles. Furnace annealing is also somewhat limited because it cannot correct the irreparable damage that is sometimes caused by high-dose ion implantation.

Pulse Annealing

To compensate for the limitations of furnace annealing, the industry is developing a new method of annealing called pulse annealing, which includes both laser and electron-beam annealing. Pulse annealing is designed to repair damage and activate ions in a more precise manner by striking the surface with some kind of energy pulse while avoiding thermal saturation.

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Laser annealing consists of using a laser to produce a short-duration, high concentration of energy on the surface of the silicon wafer. Light hits the surface of the wafer for such a short period of time that it heats only a very thin layer on the surface. The advantages of laser annealing are that it may offer improved control over defect annealing and better dimensional tolerance control.

Laser annealing has its limitations, however. For example, the absorption of the laser energy depends on the index of refraction of silicon and the degree of reflection from the silicon surface. In addition, some observers believe that it is necessary to use a thermal anneal that reaches temperatures of 600 to 700°C to repair lattice damage; thus, laser annealing may cause strain defects in the crystal lattice because of its small, intense heat spot. Dataquest is not aware of any equipment suppliers that are actively pursuing laser annealing at this time.

Some equipment manufacturers have turned to the development of electron-beam annealing systems because of the disadvantages of laser annealing. Electron-beam annealing uses electrons rather than light to heat the silicon, but it too has limitations. Some observers believe that the industry does not know enough about the nature of damage created by ion implantation and its effect on devices to allow development of a new annealing technique at this time. Dataquest does not believe that the problems with pulse annealing technology are well enough understood to assess its potential as a production process.

Rapid Thermal Processing (RTP)

Annealing can be done in a rapid thermal processor where typical anneal times can range from 10 to 100 seconds. During this process, a thermally isolated wafer is bathed in a radiation field until the temperature is stabilized for uniform dopant activation. Anneal temperatures range from 800 to 1200°C. Because of the low time at temperature, the junction does not have time to migrate appreciably.

Manufacturers of RTP equipment report excellent dopant profiles and lattice repair characteristics on their equipment. It would seem that as VLSI processing approaches 1-micron geometries, RTP will be required to ensure adequate junction tolerances. However, these systems are still being evaluated in laboratories and pilot lines and have not found large-scale use in production. Dataquest believes that this technology will become the preferred method for annealing VLSI devices within the next few years.

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MARKET ANALYSIS

The ion-implanter market may be segmented into three parts: medium-current implanters, high-current implanters, and a third segment, high-voltage implanters, which will not be included in the historic sales numbers in this report. We define these segments as follows: medium-current implanters have a beam current of less than two milliamps, although the current can be controlled down to 50 to 100 nanoamps; high-current machines have a beam current of greater than 2 milliamps; and high-voltage implanters have voltages greater than 200 KeV for singly charged ions. Although previous generations of high-current systems had capabilities of less than 15 milliamps, the latest generation has capability of from 20 to 30 milliamps. Table 3 presents Dataquest estimates of the world market for ion implanters since 1981.

Table 3

WORLDWIDE IMPLANTER SALES
(Millions of Dollars)

	1981	1982	1983	1984	1985	CAGR 1981-1985
North America						
Medium-Current	$36	$31	$38	$ 54	$ 36	
High-Current	14	24	34	69	45	
Total	$50	$55	$72	$123	$ 81	12.8%
Japan						
Medium-Current	$22	$27	$44	$ 67	$ 72	
High-Current	9	18	34	73	49	
Total	$31	$45	$78	$140	$121	40.6%

(Continued)

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Table 3 (Continued)

WORLDWIDE IMPLANTER SALES
(Millions of Dollars)

	1981	1982	1983	1984	1985	CAGR 1981-1985
Europe						
Medium-Current	$1	$3	$12	$21	$16	
High-Current	4	4	8	15	20	
Total	$5	$7	$20	$36	$36	63.8%
ROW						
Medium-Current	N/A	N/A	$1	$ 4	$ 8	
High-Current	N/A	N/A	3	6	5	
Total	N/A	N/A	$4	$10	$13	N/A
Total Medium-Current	$59	$ 61	$ 95	$146	$132	22.3%
Total High-Current	27	46	79	163	119	44.9%
Total Implanter	$86	$107	$174	$309	$251	30.7%

N/A = Not Available

Source: Dataquest
December 1986

Ion Implanter Markets

Table 3 illustrates some important evolutions in the implanter market. First, since worldwide semiconductor shipments have grown at a 12.8 percent compound annual growth rate (CAGR) since 1981, the implanter market has grown much faster than the semiconductor market. Second, high-current systems have grown much faster than medium-current systems. And third, other world markets have grown faster than North American markets.

Ion Implantation Equipment

Historic Implanter Market Growth

We would expect shipments of implanters to have grown much faster than the unit shipments of semiconductors, since the average number of applications per wafer has tripled in this same time period. However, several things have worked against this growth rate.

In the 1980 to 1985 period, the average yield at die probe increased from a world average of 45 percent to an average of 55 percent. This increase came about because of the concerted efforts of North American manufacturers to increase their yields in order to respond to the encroachment of Japanese chip vendors into worldwide markets. This increased yield would tend to raise the number of devices that could be processed per implanter.

In addition to probe yields, the productivity of implanters has grown phenomenally over this period. Although it is difficult to estimate the average productivity of implanters, since there are many different processes and types of systems, in 1980, typical throughputs were 150 wafers per hour for 10-second implants on medium-current systems. The same dose on a high-current system in 1985 could have yielded throughputs of over 300 wafers per hour. As we can see in Table 3, from 1981 unit shipments of high-current implanters have grown much faster than unit shipments of medium-current systems, and, since the average throughput has also increased, this would tend to raise the average number of devices processed per implanter.

Concomitant with throughput, the reliability and maintainability of implanters has increased. Both the throughput and reliability improvements are reflected in the steady increase in ASPs. In 1980, semiconductor manufacturers usually had a technician dedicated to an implanter. In many cases, this dedicated person was an engineer or had a Ph.D degree. Each system required continual tweeking, frequent restarts, and periodic maintenance. In addition, the procedure for changing species, energy, and dose was difficult. This situation has greatly improved since that time. For some systems, system start up is totally automatic. Changes in species, energy, and dose are also automatic. The operating system is now handled by a microprocessor so that a technician can handle the rudimentary tasks of routine production. Dataquest estimates that the average utilization of an implanter was about 10 percent in 1980 and increased to about 30 percent in 1985. We believe that this low utilization was responsible for the poor performance of this market with respect to other equipment markets during this recession. Dataquest's fabrication data base indicates that the average number of wafers processed on installed implant systems during 1985 was between 4,000 and 5,000 wafers per month.

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Ion Implantation Equipment

Installed Base

Table 4 gives Dataquest's estimates of installed ion implanters by region. As the table shows, North America has 48 percent of the operating implanters, Japan has 40 percent, Europe has 10 percent, and the ROW countries have 3 percent. However, in the last three years the percentage of ion implanter unit shipments was 24 percent for North America, 43 percent for Japan, 12 percent for Europe, and 4 percent for ROW. These percentages suggest that the largest capacity for modern, advanced implant processes exists outside of North America. This analysis is consistent with the large investment by Japanese and ROW firms in VLSI memory device capacity, and with the recent emphasis of European manufacturers on rebuilding their descending semiconductor industry.

Table 4

WORLDWIDE ION IMPLANTER INSTALLED BASE BY REGION

	Medium Current		High Current		Total	
	Units	Share	Units	Share	Units	Share
North America	565	49%	256	46%	820	48%
Japan	473	41	209	38	682	40
Europe	101	9	64	12	165	10
ROW	23	2	25	5	48	3
World Total	1,162	100%	554	100%	1,715	100%

Note: Columns may not add to totals due to rounding.

Source: Dataquest
December 1986

Ion Implantation Equipment

Implant Process Trends

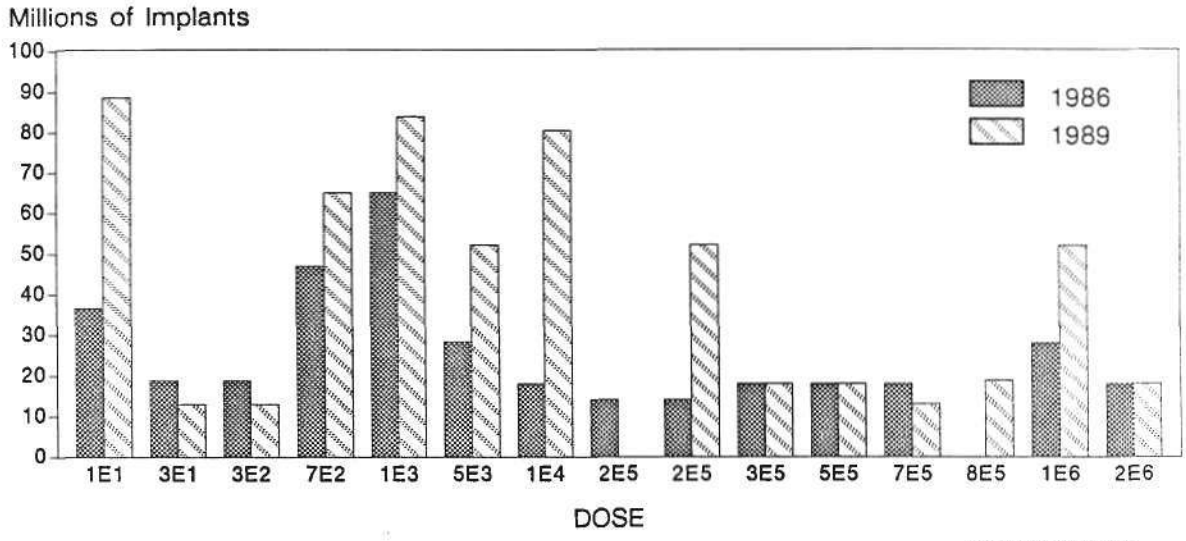
As discussed previously, high-current system sales grew much faster than medium-current systems between 1981 and 1985. It is clear from the foregoing discussion that the primary driving factor is throughput. As shown in Figure 8, recent years have seen more growth in applications for doses above 10^{14} ions/cm^2 than for below that level. Consider a throughput of 150 wafers per hour for a dose of 10^{14} ions/cm^2. A dose of 10^{16} ions/cm^2 would give a throughput of 1.5 wafers per hour on the same system. It seems ludicrous to consider the cost per wafer for 1.5 wafers per hour on a system costing $400 thousand to $600 thousand. Therefore, for modern semiconductor manufacturing, the development of high-current implanters was paramount.

However, as the demand for source/drain implants becomes satisfied, and as the device junction depths decrease, the growth of implants at doses greater than 10^{14} ions/cm^2 should slow relative to lower doses. Figure 9 shows our estimates of total implants by dopant concentration. The figure shows that there are many more low-dose implants than high-dose implants. (Note: We define low-dose implants as those for concentrations less than 10^{14} ions/cm^2.) This is consistent with our analysis of the installed base of implanters, where medium-current implanters outnumber high-current implanters 2.1:1. Figure 10 shows our estimates of total low- and high-dose implants for 1986 and 1989. The growth of low-dose implants is 64 percent, while the growth of high-dose implants is 45 percent.

From a cost-per-wafer standpoint, it is much more economical to process low doses on medium current implanters. This would imply that medium-current systems shipments would grow relative to high-current systems. However, we believe that this will not occur. It is prohibitive for a medium-current system to do high doses in a production environment because of throughput considerations. High-current systems can easily do low-dose applications, albeit while adding a higher than average incremental cost to the wafer processing cost. It will be more cost effective to spend incremental capital equipment dollars on high-current systems and then load those systems' excess capacity with low-dose implants. In this scenario, when the average low-dose load on the high-current system warrants a medium-current system, then the capital dollars would be allocated.

Figure 9

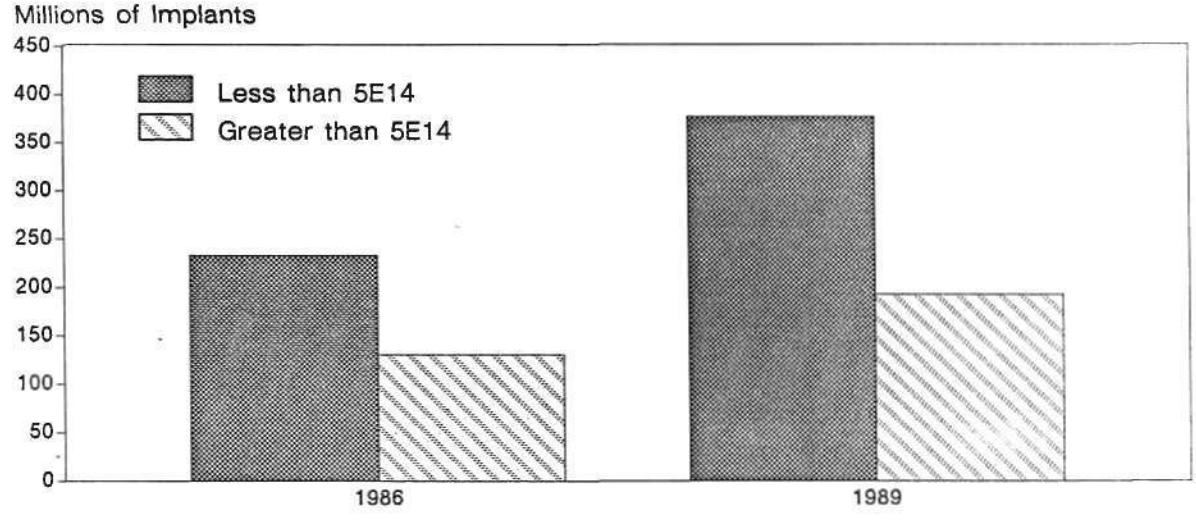
TOTAL IMPLANTS BY DOPANT CONCENTRATION



Source: Dataquest
December 1986

Figure 10

LOW- AND HIGH-DOSE IMPLANTS
1986 AND 1989



Source: Dataquest
December 1986

Ion Implantation Equipment

Market Forecast

Table 5 gives Dataquest's estimates of the markets for medium- and high-current implanters through 1989.

Dataquest expects implanter sales to continue to outpace sales of other front-end equipment as implanters replace diffusion furnaces in many of the existing process applications. Even so, the growth estimates in Table 5 are much lower than the historical sales for this equipment. This reflects the lower estimated growth of semiconductor manufacturers' capital spending for the years from 1984 through 1989. (This analysis was published in SEMS notebook, "Industry Econometrics," in the Capital Spending section.) We also expect that sales of high-current implanters will continue to grow with respect to medium-current systems.

Table 5

ESTIMATED ION IMPLANTER SALES
(Millions of Dollars)

System	1985	1986	1987	1988	1989	1990	CAGR 1985-1990
Medium-Current	$132	$85	$105	$130	$134	$150	2.6%
High-Current	119	105	145	192	182	208	11.8%
High-Voltage	5	10	15	20	34	52	59.7%
Total	$256	$200	$265	$342	$350	$410	9.9%
Growth		(22%)	32%	29%	2%	17%	

Source: Dataquest
December 1986

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New Product Markets

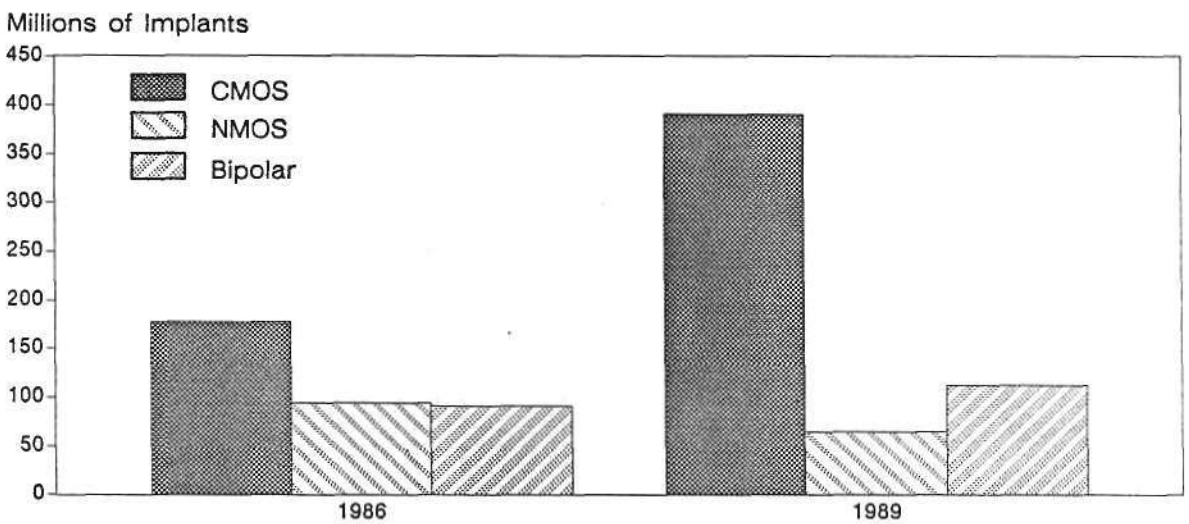
The relative growth of high-current implanters with respect to medium-current systems as shown in Table 5 is lower than historical growth. We believe that this will occur because of the growing opportunities for high-voltage and higher-current applications. Dataquest believes that there is an incipient market for systems that will target new process applications. These markets will be addressed by commercially available high-voltage implanters and by systems yet to be developed. These new product opportunities are reflected in the sales forecasted in Table 5, and they change the relative growth between the two categories.

The areas of opportunity for new products involve systems that are capable of much higher voltages and currents or are capable of higher currents with nominal voltages. These new applications are discussed in the Technology section of this report, and Dataquest believes that they represent opportunities for equipment manufacturers to penetrate or increase their shares of implanter markets.

Figure 11 shows our estimates of the number of implants as distributed by technology. It shows that the strongest growth area by far is for CMOS applications.

Figure 11

TOTAL IMPLANTS BY TECHNOLOGY
1986 AND 1989



Source: Dataquest
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One opportunity for manufacturers that this growth in CMOS processes provides is the application for high energies; energies of greater than 200KeV. For CMOS applications, these high-voltage systems can be used for the formation of CMOS wells, both conventional and retrograde. Applications also include the formation of buried layers for soft error reduction and for CMOS latch-up prevention. There is also a growing interest in late-process ROM programming. Because of the ion-current ratings on commercially available high-voltage (and hence, high-energy) systems, throughput considerations limit doses to less than 10^{13} ions/cm^2.

Table 6 lists commercial ion implantation systems that provide energies of 400 KeV or higher. In addition to these systems, Nissin and Ulvac build high-energy systems for the Japanese market. Nissin is marketed in North America by Mitsubishi International.

Table 6

COMMERCIAL HIGH-VOLTAGE IMPLANTERS

Manufacturer	Accelerator Type	Terminal Voltage(MeV)	Beam Current (particle·uA)
National Electrostatics	Tandem (MV-T30)	1.0	5 B^{+2}
	Single-End (MV-H20)	2.0	(20) (B^+) (40) (P^+)
General Ionex	Tandem (1500-25)	0.75	(20) (B^{+2}) (20) (P^{+2})
Extrion	Single-End (Extrion-400)	0.4	50 B^+ 100 P^+ 100 As^+
Veeco	Single-End (400MP)	0.4	58 B^+ 31 P^+
HVE Europa	Single-End	0.5	50 B^+ 75 P^+ 50 As^+
Eaton	Single-End (NV-1000)	0.8	300 B^+ 300 P^+

Source: Solid State Technology

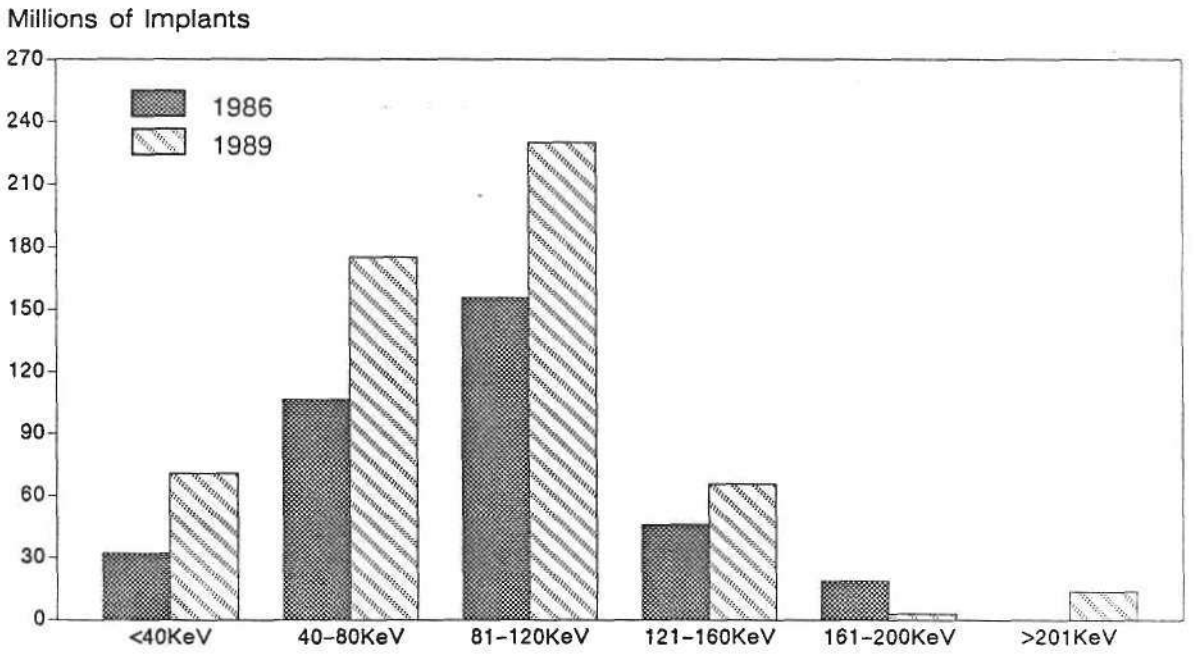
Ion Implantation Equipment

There could also be an opportunity for a very high-current system for implanting buried oxides. Such buried layers represent a replacement for silicon-on-saphire (SOS). Such layers are called silicon-on-insulator (SOI), and are used for radiation hardening and isolation. SOI systems would require voltages of 200 KeV and currents of greater than 100mA. They would also need to heat the wafer in situ to over 500°C in order to anneal the implant damage to the wafer substrate.

Figure 12 shows our estimates of total implants as distributed by ion energies. This figure assumes that 10 percent of the P- and N-wells will be done in the retrograde fashion in 1989. This conservative estimate yields nearly 20 million implants per year by the end of 1989.

Figure 12

TOTAL IMPLANTS BY ION ENERGY
1986 AND 1989



Source: Dataquest
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Market Share

Table 7 lists the major ion implanter manufacturers and Dataquest's estimates of their worldwide market shares in 1984 and 1985. Table 8 restates those shares as a percentage of the total market.

It is apparent that Eaton gained considerable share in 1985 at the expense of Varian, growing from 34 percent at $104 million in 1984 to 37 percent at $92 million in 1985, while Varian fell from 44 percent at $135 million to 40 percent at $100 million. The other competitors' worldwide market share remained relatively unchanged.

Table 7

ESTIMATED WORLDWIDE MARKET SHARE
(Millions of Dollars)

	Medium Current		High Current		Total	
Manufacturer	1984	1985	1984	1985	1984	1985
Varian	$80	$76	$55	$24	$135	$100
Eaton	$17	$20	$87	$72	$104	$ 92
Nissin	$16	$15	$12	$10	$ 28	$ 25
Ulvac	$16	$14	$ 4	$ 6	$ 20	$ 20
Veeco	$ 6	$ 2	$ 5	$ 7	$ 11	$ 9
Hitachi	$ 5	$ 5	N/A	N/A	$ 5	$ 5
Balzers	$ 6	0	N/A	N/A	$ 6	0

Source: Dataquest
December 1986

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Ion Implantation Equipment

Table 8

ESTIMATED WORLDWIDE MARKET SHARE
(Percentage)

Manufacturer	Medium Current 1984	Medium Current 1985	High Current 1984	High Current 1985	Total 1984	Total 1985
Varian	55%	58%	34%	20%	44%	40%
Eaton	12%	15%	53%	61%	34%	37%
Nissin	11%	11%	7%	8%	9%	10%
Ulvac	11%	11%	2%	5%	6%	8%
Veeco	4%	2%	3%	6%	4%	4%
Hitachi	3%	4%	N/A	N/A	2%	2%
Balzers	4%	0%	N/A	N/A	2%	0%

Source: Dataquest
December 1986

Table 9 shows Dataquest's estimates of installed base of ion implanters by company. This table shows that Varian has by far the most installed implanters worldwide, with 845 systems or 49 percent of the total. Eaton is second with 454 systems or 26 percent of the total. Although there are several potential threats to the leaders' position, the next seven companies contribute only 23 percent of the total implanters installed worldwide.

Table 9

ESTIMATED ION IMPLANTER INSTALLED BASE
BY COMPANY

	Medium Current		High Current		Total	
	Units	Share	Units	Share	Units	Share
Varian	674	58%	171	31%	845	49%
Eaton	161	14%	293	53%	454	26%
Ulvac	148	13%	11	2%	160	9%
Nissin	61	5%	37	7%	98	6%
Veeco	64	6%	13	2%	77	4%
Balzers	18	2%	8	2%	27	2%
Hitachi	21	2%	N/A	N/A	21	1%
App. Materials	N/A	N/A	21	4%	21	1%

Source: Dataquest
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Medium-Current Implanters

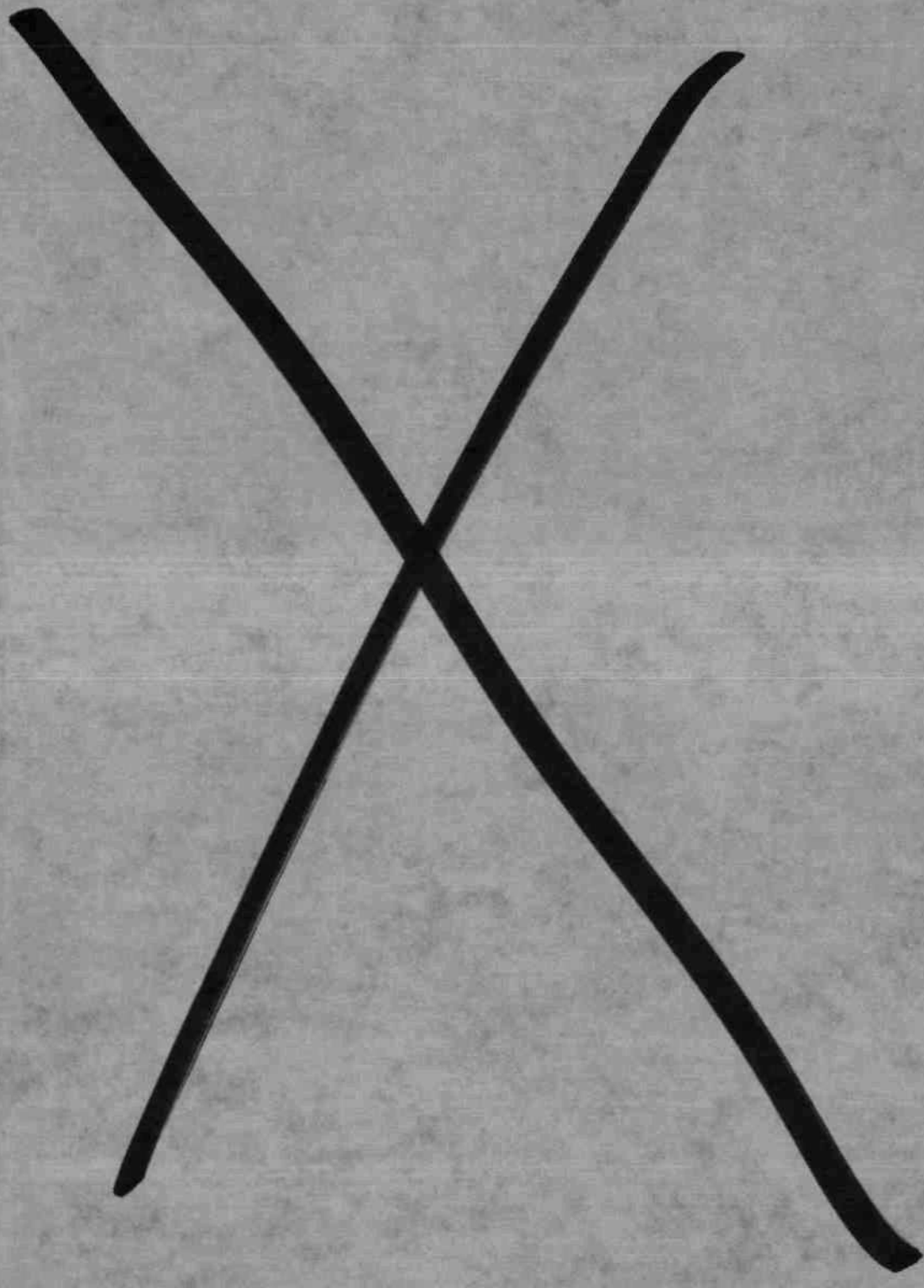
In medium-current implanters, Varian/Extrion has the leading market share and has maintained that position for many years. From 1980 to 1984, Eaton's sales of medium-current implanters had a 29.9 percent CAGR while Varian's sales grew 24.7 percent CAGR. In 1985, when the industry declined, Varian's share rose from 55 percent to 58 percent of the world, while Eaton's grew from 12 percent to 15 percent. While this relative growth is a tribute to the ingenuity of Eaton's implanter technologists, Varian quite clearly still has the dominant position. In 1985, Japanese vendors held their share.

From 1980 to 1984, Ulvac's sales of medium-current systems in Japan grew at 27.8 percent CAGR, while Varian's sales in Japan increased at 31.6 percent CAGR. Varian's trading partner in Japan is Tokyo Electron Laboratories (TEL). Varian and TEL formed a joint venture called TEL-Varian in 1982. Most all of Varian's medium current implanters are assembled by TEL-Varian in Japan. The quality and reputation of this company helps to maintain Varian's strength in Japan.

High-Current Implanters

In high-current implanters, Eaton has the leading market share and has maintained that position for many years. Its CAGR from 1980 to 1984 was 89.8 percent, while Varian's was 78.6 percent for the same period. In 1985, Eaton grew its share from 53 percent to 61 percent of the world total, while Varian lost share from 34 to 20 percent. Most of this loss occurred in Japan. Eaton quite clearly has the dominant worldwide position in this market and is maintaining it.

However, in Japan, Eaton had a lesser share than Varian through 1984. Dataquest believes that Eaton's slower penetration of the Japanese market was due to changing trading partners before it secured a foothold in this market. Eaton had three trading partners in five years. Kokasai began marketing Eaton's systems in 1979, then Eaton switched to Marubeni in 1981. To be successful, it is paramount that an equipment company form long-term relationships with its customers in Japan. Eaton has now had a successful joint venture with Sumitomo Corporation for three years, called Sumitomo-Eaton-Nova Corporation (SEN). SEN now assembles almost all of the Eaton-designed implanters sold in Japan, with Marubeni marketing these systems and brokering the overflow from Eaton's factory in the United States when SEN capacity is oversold. Eaton's position has improved considerably since the formation of SEN and it has 31 percent of that market. However, Varian still has a very strong position in that market, although it dropped from 49 percent to 31 percent in 1985. Ulvac and Nissin have grown their collective share from 16 to 33 percent of the total in 1985.



Process Control

The following is a list of the material in this section:

- CD and Wafer Inspection Equipment Companies

For additional information, please refer to the material behind the Process Control tab in your 1989 Newsletter binder.

CD and Wafer Inspection Equipment Companies

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CD and Wafer Inspection Equipment Companies

INTRODUCTION

This study discusses the products and strategies being pursued by manufacturers of critical dimension (CD) and wafer inspection equipment. For additional information on the CD and wafer inspection equipment segments, please refer to material filed behind the "Process Control" tabs in the SEMS Equipment and Materials binder and the SEMS Newsletter binder. Historical market information for optical CD, wafer inspection, and joint CD/inspection equipment is located in the SEMS Equipment Database in the Equipment and Materials binder.

OVERVIEW OF PRODUCT CATEGORIES

Critical dimension and wafer inspection systems represent segments within the larger equipment category that Dataquest defines as process control equipment. Process control is a broad category that includes equipment for mask and wafer inspection, film thickness measurement, linewidth and overlay measurement, surface particle analysis, resistivity mapping, and analytical quality control. This is a highly fragmented market with dozens of companies selling into many noncompetitive niches. In particular, CD and wafer inspection systems are used in the production environment to provide data, analysis, and feedback on equipment operation and the manufacturing process. The ability to acquire, measure, and analyze information in a timely manner becomes essential, as the semiconductor industry enters a new manufacturing phase in which attention is being focused on the automation of manufacturing processes. While total or "lights-out" factory automation in the semiconductor industry is still years away, automated CD and wafer inspection systems are fundamental components of manufacturing strategy today and will be necessary if lights-out automation is to be achieved.

Critical Dimension

A critical dimension of a semiconductor device refers to a line, element, or feature that must be manufactured and controlled to very tight specifications. In the design of advanced semiconductor devices, design tolerances of critical features are specified at 1/10 the size of the critical dimension. In the case of a 1.0-micron line geometry, that means that fabrication equipment, materials, and processing technology must reproducibly produce a feature that is 1.0 micron, with a deviation of plus or minus 0.1 micron, in order for the manufacturing process to be in control. CD measurement equipment must have very high precision, which means that repetitive measurements are reproducible within a very small range of deviation. The accuracy of a linewidth measurement system describes the nearness of a measurement to its accepted or true value, typically determined by comparison with in-house standards, usually a wafer that is known to be "good." A critical dimension can refer to the dimension of a linewidth in a device pattern at a given mask level, as well as to a measure of the allowable tolerance in the overlay of patterns from multiple mask levels. Typically, CD measurement systems available today perform both linewidth and overlay measurements.

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Over the last several years, the field of CD measurement has diversified into a multitude of technologies. Conventional CD tools have been based on white-light microscopy systems. Today, however, this equipment is enhanced with sophisticated image processing capabilities. In addition, laser-based measurement systems, confocal scanning laser microscopy, and coherence probe imaging technologies have been developed to perform submicron measurements. Scanning electron microscope (SEM) tools, traditionally relegated to the analytical lab, have been redesigned to meet the needs of submicron manufacturing in a production environment.

Wafer Inspection

Wafer inspection refers to the inspection of patterned wafers for process defects by visual and image-processing techniques. Traditionally, this equipment has been designed as a microscope station at which an operator visually inspects wafers under magnification for the presence of defects, which range from contaminating particles to defective circuit patterns. As wafer inspection tools have matured, additional features have been added, including automatic wafer handling, automatic and programmable stage movement, autoalignment, autofocus, and keypad data entry systems. In conventional wafer inspection systems today, almost everything but human vision is automated. Recently, a new generation of automatic wafer inspection stations was introduced. These sophisticated systems utilize holographic spatial frequency filtering technology and advanced image-processing techniques to perform automatic defect detection. In some instances, wafer inspection systems assist in defect classification as well.

Wafer inspection equipment discussed in this study focuses on systems that are used for the detection of process-related defects. In this category, Dataquest does not include standalone microscopes or the laser-based surface analyzers that are used to detect and measure particles, scratches, and deformities at the wafer surface.

Reticle Qualification

Reticle qualification systems are used during the setup and process qualification stage of lithographic processing. Typically, every time a reticle or mask is changed on a lithography tool, the reticle qualification procedure is performed to verify reticle quality and optimal lithographic equipment operation. Reticle qualification systems do not compete directly with the wafer inspection stations that are used for defect detection during the production process; thus, "ret qual" systems are considered a separate category from wafer inspection. This distinction becomes somewhat cloudy, because some systems are used in both wafer inspection and reticle qualification applications. Reticle qualification systems are discussed briefly in this study, because these systems perform a function that is complementary to wafer inspection.

Joint CD/Inspection Systems

Over the last several years, a new category of measurement and inspection equipment has emerged—systems that are designed for both CD measurement and inspection capability. Dataquest refers to this category of equipment as joint CD/inspection systems. In 1983, Optical Specialties, Inc., introduced the first system designed as a microscope-based inspection station with automatic CD measurement capability. An operator, however, was still required to perform defect detection and classification. In 1984, KLA Instruments introduced its 2020 system, a tool that combines automatic CD measurement with automatic inspection capability. For the first time, the subjective judgment of the operator was removed from the wafer inspection process.

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COMPANY ACTIVITIES

Table 1 contains a list of companies active in the CD and wafer inspection equipment markets. This list, organized by region of company ownership, summarizes company products by equipment category: optical and e-beam-based CD equipment, wafer inspection stations, reticle qualification systems, and joint CD/inspection systems. While not the primary focus of our analysis, the categories of e-beam-based CD equipment and reticle qualification systems are included in Table 1 and in the discussion of company activities, because they represent competitive, and, in some cases, complementary technologies and products. In addition to listing new product developments and announcements, Table 1 identifies four companies that are no longer active in these market segments.

In the following discussion of company activities and products, the measurement capability of CD equipment is discussed. The reader is cautioned that specifications of linewidth measurement capability for any model of equipment can vary, depending upon the type, thickness, and combination of semiconductor materials being measured, as well as whether the measurement is being performed in an R&D or a production environment. No attempt has been made to correlate and verify measurement conditions and specifications of the various models of CD measurement equipment discussed in this study.

Table 1

CD and Wafer Inspection Equipment Companies by Product Category

	CD Optical	CD e-Beam	Wafer Inspect	Reticle Qualification	Joint CD/Inspect
North American Companies					
Amray		X			
Angstrom Measurements		X			
Estek (Aeronca)			X		
Insystems			X		
ITP Inc.	X				
IVS Inc.	X		U/D		
KLA Instruments	X	X	X	X	X
Nanometrics	X	X	X		
Nanoquest, Ltd.*	X	X			
Orasis			U/D		
Opal Inc.		X			
Optical Specialties, Inc.	X		X		X
Reichert-McBain	X				
Perkin-Elmer	X				
SiSCAN Systems	X				
Waterloo Scientific	U/D				

(Continued)

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Table 1

CD and Wafer Inspection Equipment Companies by Product Category (Continued)

	CD Optical	CD e-Beam	Wafer Inspect	Reticle Qualification	Joint CD/Inspect
Japanese Companies					
ABT (Akashi Beam Technology)		X			
Canon			X		
Dainippon Screen	N/P				
Hitachi	X	X			
Holon		X			
JEOL		X			
Lasertec				X	
Nidek	X		X		
Nikon	X		X		
Olympus			X		
Ryokosha	X				
Sony				X	
European Companies					
Cambridge Instruments				X	
Heidelberg Instruments			U/D		
Micro-Controle	X		X		X
Wild Leitz	X		X		
Wild Leitz Instruments	X				
Zeiss			X		
Departures					
Contrex					X
Machine Intelligence					X
Optoscan	X				
Karl Suss			X		

Notes: N/P = New product announcement
U/D = Equipment currently under development
*Formedy Vickers Instruments

Source: Dataquest
October 1989

Prometrix, a manufacturer of linewidth measurement systems based on electrical probing techniques, is not listed in Table 1 because its equipment does not fall into any of the identified product categories. The company, however, is briefly discussed in the following section on U.S. companies.

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NORTH AMERICAN COMPANIES

Amray

Amray (Bedford, Massachusetts) manufactures the Amray 1500, a SEM-based CD measurement system. The Amray 1500, designed for in-process measurement operations, utilizes a field emission electron beam source. Throughput of the system is approximately 10 wafers per hour at five sites per wafer. The system, developed in the 1984 time frame, is currently priced at $550,000.

Angstrom Measurements

Angstrom Measurements (Sunnyvale, California) has developed and manufactured a low-voltage, e-beam-based metrology tool for the production environment known as the Scanline SEM CD Measurement System. Linewidth measurement capability is from 0.2 micron to 50 microns. The system incorporates pattern recognition, which provides a significant contribution to the system's wafer throughput of 15 to 20 wafers per hour at five sites per wafer. In addition, the company claims that the system has one-third the footprint of other SEM CD measurement systems. The price of the system (with lanthanum hexaboride source) is approximately $320,000. The first system was shipped in 1989.

In 1987 and 1988, Angstrom Measurements and Cambridge Instruments had a marketing agreement that Cambridge would represent the Scanline system in worldwide markets. In December 1988, the marketing agreement was terminated.

In mid-1989, it was announced that Nanometrics had signed a letter of intent to acquire a minority investment position in Angstrom Measurements. This relationship involves the exchange of some key technologies between the two companies. In addition, the companies are exploring the possible application of Nanometrics' proprietary field emission e-beam technology in the Angstrom Measurements' Scanline system. Nanometrics will distribute and provide support for the Scanline system in Japan through its wholly owned subsidiary, Nanometrics Japan, Ltd. Angstrom will market Scanline in the United States through its sales representatives.

Estek (Aeronca)

Estek, through its acquisition of Aeronca Electronics in late 1986, markets the AE-1000 automated wafer inspection system in the United States. Estek's AE-1000 system is manufactured by Canon of Japan and is the same as Canon's VIR-600 model. The AE-1000 can operate in 100 percent inspection or random sampling mode. Prior to inspection under the microscope, wafers are passed under a white-light source for visual inspection of gross defects and flaws in the wafer surface. Detection and classification of pattern defects are performed visually by an operator with the aid of a microscope station. The price of the AE-1000 is approximately $80,000. Aeronca Electronics began to market the Canon wafer inspection system in 1985. The Estek division responsible for Aeronca products is located in Charlotte, North Carolina.

In addition to marketing Canon's wafer inspection equipment, Estek manufactures a family of products for wafer surface inspection. These systems measure particulate contamination on both unpatterned and patterned wafers. Estek also manufactures rinser/dryer systems for semiconductor wet processing.

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Insystems

Insystems (San Jose, California) manufactures a fully automated, full-wafer, submicron defect detection system that utilizes holography and spatial frequency filtering technology. The Model 8600 was designed for in-process patterned wafer inspection and can inspect an entire wafer surface for defects in less than 30 minutes. This is in comparison with the several hours required for inspection by conventional optical- or SEM-based inspection tools. This reduction in measurement time is achieved because the Model 8600 relies on parallel optical processing rather than a serial analysis of the wafer on a die-by-die basis. Defect classification is still an operator-dependent task.

The Model 8600, with up to 200mm wafer capability, can detect submicron defects in high-density, repetitive areas in single- and multiple-process levels in photoresist, oxide, polysilicon, metal, and other films, such as nitride, PSG, and polyimide. The Model 8600 with robotic wafer handling capability is priced at $1.18 million. Insystems first introduced the system in March 1987 at SEMICON/Europa. The U.S. introduction was at SEMICON/West the following May. The Model 8600 was in beta site during 1986, and Insystems shipped its first two systems in fourth quarter 1987.

In May 1988, Insystems introduced an advanced data management software package for its Model 8600 system. The software package, known as FAB MANAGER, provides the capability for data capture, manipulation, and storage of up to 4,000 recorded wafer inspections. Wafer inspection data can be analyzed for repeating defects, for defects by process layers, and for defect patterns across the entire wafer map. The new software package is available to both new and existing Model 8600 customers at no additional cost.

At SEMICON/West in May 1989, Insystems introduced a defect review station, the Model 861. This station allows an operator to perform wafer defect classification as a function separate from the operation of the Model 8600. This translates to enhanced throughput because now the time-consuming task of operator defect classification can be performed essentially off-line. Defect data can be downloaded from the 8600 and stored locally on hard or floppy drive or the 861 can be linked with the 8600 through a local area network (LAN). In addition, the 861 defect review station is SMIF-compatible. The price of the 861 is $250,000 in the United States.

Insystems, founded in 1981, is a privately held company. Insystems' first product was the Model 8405 automatic photomask inspection system. The first unit, at a price of $800,000, was shipped to Motorola in April 1986. Insystems viewed the Model 8405 as an interim product in its technology development of wafer defect detection systems.

ITP Inc.

ITP Inc. (Sunnyvale, California) manufactures a product line of optical CD measurement equipment including the System 851, the System 85, and the System 891.

The System 851 is a video-based charge-coupled device (CCD) camera system with linewidth measurement capability down to 0.25 micron on certain features. System throughput is approximately 30 wafers per hour at five measurement sites per wafer. The System 851 is the successor of the System 85, ITP's first CD measurement system to combine a CCD camera and personal computer with the company's patented autofocus system. The System 851 is priced at approximately $60,000. The System 85, with 1.0-micron measurement capability, is priced at approximately $45,000.

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ITP is currently developing a new submicron measurement system, the System 891. The 891, like the System 851, has linewidth measurement capability down to 0.25 micron on certain features. In addition, the system incorporates pattern recognition capability, a high precision stage, and robotic wafer handling. The approximate price for the System 891 will be $200,000.

ITP has been a privately held company since its founding in 1968.

IVS Inc.

IVS Inc. (Concord, Massachusetts) manufactures a family of CD and registration alignment measurement equipment. The AccuVision products incorporate digital image processing and proprietary software algorithms with an optical microscope system to provide submicron measurement capability. The signal-to-noise ratio is improved by employing various digital enhancement techniques to remove random noise elements introduced by optical and electronic components.

IVS first introduced its AccuVision family of digital image processing tools in May 1986. The ACV-1 is a manual system for the R&D environment and small production lines. The AccuVision family of products also have included modular system upgrades of the ACV-1 with semiautomatic capability, known as the ACV-2 and ACV-3 systems. The ACV-4, first exhibited at SEMICON/West in 1987, was formally introduced at SEMICON/West in May 1989. This system is a fully automatic, cassette-to-cassette system for CD, registration, and contact hole measurements. It can measure linewidth geometries to 0.5 micron and below, with 0.025-micron repeatability (3 sigma). Typical wafer throughput for linewidth measurement is approximately 25 wafers per hour at five sites per wafer. A software package performs analysis of bottom and top contact measurements and determines if a contact is open or closed. Contact measurement capability is on the order of 0.8 micron with 45-nanometer repeatability and relies upon a proprietary autofocus mechanism that the company has developed. The price of the ACV-4 system is approximately $350,000, whereas the manual ACV-1 system is priced at $125,000.

In addition to its optical CD measurement systems, IVS is developing an automated wafer defect inspection system.

IVS, founded in 1980, began its operations as a manufacturer of digital image processors for scientific applications. The company began to shift its focus to the semiconductor wafer metrology market in 1984 and received its first round of venture funding in early 1985.

KLA Instruments

KLA Instruments (Santa Clara, California) is a major manufacturer of automated image analysis systems for the semiconductor industry. The company's Wafer Inspection Division (WISARD) was formed in 1983. In 1984, the company introduced the KLA 2020 Wafer Inspector, the industry's first fully automated wafer inspection system. Since that time, the company has developed a family of products for automatic CD measurement and wafer inspection (Table 2).

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Table 2

KLA Instruments' WISARD Division Products

Model Number	Year Introduced	Optical CD	Wafer Inspect	Joint CD/ Inspect	Analysis Stations	Software Packages
KLA 2020	1984			X		
DRG	1985				X	
KLAUT (KLA 2510)	1986				X	
KLA 2005	1987	X				
KLASS	1987					X
PWDA	1987					X
KLA 2028	1987		X			
KLA 2030	1987			X		
KLA 5000	1988	X				
KLA 2600	1988				X	
KLA 2029	1989		X			
KLA 2031	1989			X		
DSA	1989					X

Source: Dataquest
October 1989

Dedicated Wafer Inspection and Joint CD/Inspection Systems

The KLA 2020 is an in-process wafer inspection system that integrates CD, registration overlay, and area measurements with defect monitoring and macro inspection. Typical wafer throughput for the 2020 on CD measurement is on the order of 90 wafers per hour at five sites per wafer. The KLA 2020 performs a linewidth measurement in a 1.5-second time interval, which includes the time to move to a new position, the time for the system to settle and stop, and, finally, the time for the system to acquire the linewidth image. Measurements from the 2020 exhibit strong linear correlation with calibrating SEM tools down to 1.0 micron, with a three-nines to four-nines correlation coefficient. Customer applications, however, have included repeatable linewidth measurement down to 0.6 micron.

The KLA 2020 also has automatic defect inspection capability. After the wafer cassettes are loaded, inspection proceeds automatically under the direction of the system computer. The KLA 2020 has defect measurement sensitivity down to 0.5 micron in both repeating and random geometry inspection modes.

The first KLA 2020 system was shipped in early 1985. Today, the 2020 is priced at approximately $985,000 in the United States.

In September 1987, KLA introduced two new wafer inspection systems, the KLA 2028 and the KLA 2030. The KLA 2028 automatic wafer defect inspection system retains the same macro defect detection capability as the KLA 2020; however, the new 2028 is capable of micro defect detection at rates of speed approximately 4 times (for random geometry inspection) to 15 times (for repeating array inspection) faster than those of the KLA 2020. The KLA 2028, a dedicated defect inspection system, is priced at approximately $965,000 in the United States.

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The KLA 2030 automatic wafer defect inspection and metrology system combines the metrology capability of the KLA 2020 with the enhanced defect detection capability of the new 2028. Both systems have defect detection capability down to 0.4 micron. The price of the KLA 2030 is approximately $1.2 million in the United States. Current owners of the KLA 2020 can retrofit their systems to full 2030 performance capability at a cost of approximately $300,000. First shipments of the KLA 2028 and 2030 began in early 1988.

In May 1989, KLA introduced the KLA 2029 and KLA 2031 wafer inspection systems. These two systems provide improved defect detection capability in comparison with their predecessors, the 2028 and 2030 systems, respectively. In particular, the new systems are capable of detecting 0.35-micron defects on devices with 0.7-micron design rules, such as 4Mb DRAMs. The KLA 2029 is priced at $1.095 million; the 2031 is priced at $1.310 million. Shipments to customers are expected to commence in autumn 1989.

Optical CD Systems

Since early 1987, KLA has offered the KLA 2005, a metrology-only version of the 2020. This system, which has no defect inspection capability, has been targeted specifically at the lithography area of the fab. The 2005 is priced at approximately $700,000 in the United States. Several 2005 systems that were sold in 1987 were upgraded later to full 2020 systems. The price of the upgrade is approximately $300,000.

In March 1988, KLA Instruments introduced the KLA 5000, a coherence probe microscope system for CD measurement beyond the limit of conventional white-light optical systems. The coherence probe microscope utilizes a Linnick microscope, which is essentially a Michelson interferometer with the addition of two microscope objectives. The technique of coherence probe imaging (CPI) produces images by applying electronic algorithms to a particular set of interference images taken from the Linnick interference microscope. The coherence probe microscope system also provides three-dimensional detail of line geometry measurements. The KLA 5000 has a measurement resolution of 0.7 micron and wafer throughput is 40 to 45 wafers per hour at five sites per wafer. The system is priced at approximately $350,000 in the United States. As of mid-1989, several systems have been shipped to customers. KLA Instruments currently has a patent pending on the coherence probe microscope.

SEM CD Systems

In November 1986, KLA Instruments announced an agreement with Holon Co., Ltd., of Japan for KLA to be the exclusive distributor of Holon's SEM-based CD measurement system in the United States and Europe. This system, known as the KLA/Holon 2711, is a low-voltage, e-beam, submicron metrology system designed for automated CD and registration measurements. Dataquest believes that KLA is not doing much with this product at this time.

Analysis Stations

In May 1985, the company introduced an enhancement to the 2020, the Design Reference Generator (DRG). The DRG allows the 2020 to compare a processing level on the silicon wafer with the design database of the mask or reticle used to expose the wafer. This is an important application in the identification of repeating defects. The price of the DRG is approximately $380,000.

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In May 1986, KLA introduced a computer subsystem, the KLA Utility Terminal (KLAUT), which is used with the 2020 to collect, process, and format wafer inspection data into graphics displays for statistical analysis. This hardware system has since been renamed the KLA 2510 Analysis Station.

In May 1988, KLA introduced the KLA 2600 Defect Review Station. This station allows an operator to perform wafer defect classification as a function separate from the operation of KLA's automatic defect detection systems (the 20xx product family). This translates to enhanced throughput of the 20xx systems of approximately 33 percent, because now the time-consuming task of operator defect classification can be performed essentially off-line at the 2600 review station. The KLA 2600 consists of a microscope station, robotic wafer-handling system, and PC AT-compatible controller. The software of the 2600 interfaces with the KLA 2510, which downloads defect coordinates to the review station. After review and classification, the records are transferred back to the 2510 for comparative analysis.

Application Software Packages

In May 1987, KLA introduced the KLA Stepper Set-Up (KLASS), a software enhancement for the 20xx family of products. The KLASS software, which loads on the KLA 2510 (KLAUT), is an applications package for optimizing stepper setup parameters. The KLASS software can optimize the correct focus and exposure settings for a stepper in approximately 4 minutes and produces a picture of the stepper control screen on the KLA 2510 terminal in order to guide the operator in changing new focus and exposure settings. The KLASS software package is priced at $20,000.

The second software enhancement for the KLA 20xx product family was introduced in September 1987. The Product Wafer Defect Audit (PWDA) assists the user in identifying the cause of defects. It sells for approximately $30,000.

In May 1989, KLA introduced the Defect Source Analysis (DSA) software package, which provides a simple means of pinpointing a defect source in the process. This package is priced at approximately $50,000.

General Company Information

KLA Instruments was founded in 1976 and has been a publicly traded company since October 1980. Over the years, KLA has successfully developed a family of advanced inspection systems for use in various segments of the semiconductor industry. The company is structured into four operating divisions: RAPID, the Reticle and Photomask Inspection Division; WISARD, the Wafer Inspection Division; ATS, the Automated Test Systems Division, whose primary business is wafer prober systems; and KLASIC, a new division recently established to focus on supplying inspection systems to the printed circuit board industry.

Nanometrics

Nanometrics (Sunnyvale, California) manufactures optical and SEM-based linewidth measurement and inspection equipment for the semiconductor industry. The company's first optical CD measurement system, the Nanoline, was shipped in 1978, and total installations of Nanometrics' optical linewidth measurement systems number in excess of 1,000 units.

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Optical CD Measurement Systems

In 1986, Nanometrics introduced the Model 50, an optical CD measurement system that replaced its predecessors, the Nanoline V and VA. The Model 50 measurement technology is based on a narrow optical slit that is mechanically stepped across a magnified image of the wafer feature. The light passing through the slit is measured by a photomultiplier tube (PMT) to form a high-resolution reflectance profile. The profile is stored on the system computer and analyzed to determine the linewidth of the wafer feature. The primary changes between the Model 50 and the Nanoline V and VA included improved autofocus algorithms, faster measurement times, better system measurement linearity, and improved equipment uptime. The Model 50, like the Nanoline product family, is a manual measurement tool.

At SEMICON/West in 1988, Nanometrics introduced the Model 55 Submicron Optical CD Measurement System, a fully automated system that provides down to 0.7-micron linewidth measurement capability with 10-nanometer repeatability. The Model 55 is an automated version of the Model 50-2, which itself was recently upgraded with new optical components from the Model 50. Linewidth measurement throughput of the Model 55 is greater than 30 wafers per hour at five sites per wafer. The price of the Model 55 is approximately $100,000; the Model 50-2 is priced at $60,000.

SEM Measurement and Inspection Systems

In addition to optical linewidth measurement systems, Nanometrics manufactures a fully automated SEM for linewidth measurement and defect inspection. In May 1986, Nanometrics introduced the Model 100, a low-voltage, in-line SEM system. Shipments of the Model 100 began in fourth quarter 1986, at which time the system was priced at approximately $420,000. The Model 100 is the successor to Nanometrics' CWIKSCAN product line of scanning electron microscopes.

At SEMICON/West in May 1988, Nanometrics introduced its Nano 150Z SEM-based measurement and inspection system. The Nano 150Z is an extension from the Model 100 system that it replaces. The system has minimum linewidth measurement capability of approximately 0.3 micron and a throughput of six wafers per hour at five sites per wafer.

In addition to its metrology capabilities, the Nano 150Z can perform general inspection (i.e., step coverage, residual resist) and defect review. The Nano 150Z uses a patented field emission source to achieve superior image quality. As a SEM tool optimized for image quality, the Nano 150Z system can be used for detecting, identifying, and characterizing defects using nondestructive inspection techniques. The system also provides 0 to 60 degree tilt angle capability to optimize defect review and classification. Nanometrics suggests that the Nano 150Z is well suited, in particular, as a review station for such automatic defect detection system as KLA's 20xx family of products or Insystems' 8600 system. At SEMICON/West 1989, the company announced a new software release for the system with a multitude of features for improved operator ease-of-use and image processing. The price of the Nano 150Z is approximately $625,000. A manual version (no cassette-to-cassette wafer handling) of the Nano 150Z system, the 150Z-M, is available at a price of $525,000. Shipments of the Nano 150Z system began in 1989.

In mid-1989, it was announced that Nanometrics had signed a letter of intent to acquire a minority investment position in Angstrom Measurements. This relationship involves the exchange of some key technologies between the two companies. In addition, the companies are exploring the

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possible application of Nanometrics' proprietary field emission e-beam technology in the Angstrom Measurements' Scanline system. Nanometrics will distribute and provide support for the Scanline system in Japan through its wholly owned subsidiary, Nanometrics Japan, Ltd. Angstrom will market Scanline in the United States through its sales representatives.

Wafer Inspection Equipment

Nanometrics introduced the NanoStation 1 at SEMICON/West 1988. This product marks Nanometrics' entry into the wafer defect inspection equipment market. The NanoStation I is a dual-cassette system designed for inspection of 100mm, 125mm, and 150mm wafers. The system has many automated features, including robotic wafer handling. The system does require an operator to perform the defect detection and classification tasks. An optional feature is a computer image file that allows 2,500 images to be identified and stored with rapid retrieval for later defect review. The NanoStation 1 is priced at approximately $65,000. In 1989, several beta units were under evaluation by customers.

General Company Background

Nanometrics was founded in 1975 and has been a publicly traded company since late 1984. In addition to the company's optical and SEM-based measurement and inspection equipment, other Nanometrics' products include film thickness measurement equipment for the semiconductor industry and ultraviolet, visible, and infrared spectrophotometers for analytical applications. Nanometrics' majority-owned subsidiary, Loma Park Associates, manufactures a tooling system used in the production of multilayer printed circuit boards.

Nanoquest, Ltd.

In January 1989, Bio-Rad Laboratories (Hercules, California) acquired Vickers Instruments, the English-based manufacturer of optical and e-beam metrology equipment. (The acquisition also included the Canadian and U.S. operations of Vickers Instruments.) As part of the acquisition, Vickers Instruments (formerly part of Vickers Plc) has been renamed Nanoquest, Ltd.

Bio-Rad is a leader in life sciences research products, clinical diagnostics, and analytical instruments. The acquisition of Vickers Instruments provides Bio-Rad with an entry into the front-end semiconductor manufacturing environment with a well-established vendor.

Nanoquest manufactures the Quaestor CD-07A, a fully automatic, optical linewidth and overlay measurement system. This system has been designed specifically for the production environment, with major emphasis placed on fully automatic operation and reliable linewidth measurement in production operation. The CD-07A utilizes an image-shearing technique to measure linewidth geometries down to 0.7 micron. The system has a wafer throughput rate of 25 wafers per hour at five measurement sites per wafer. The CD-07A was introduced in 1986, and deliveries began in 1987. At SEMICON/West in May 1989, Nanoquest introduced 200mm capability and pick-and-place robotics for the Quaestor CD-07A. The price of the system with these enhancements is approximately $300,000.

Nanoquest also manufactures e-beam-based CD measurement systems. In May 1987, the company introduced the Nanolab SR Series at SEMICON/West. The Nanolab SR Series is an automatic, nondestructive, submicron CD and inspection system. The tool utilizes SEM technology

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and is designed to operate in the production environment. The wafer throughput rate is approximately 15 wafers per hour at five sites per wafer. The linewidth measurement range is from 0.1 micron to 10.0 microns. Inspection capability is based on visual observations made by an operator. The first shipment of the Nanolab SR was in late 1986. This system is priced at approximately $600,000.

Nanoquest also offers a sister tool to the Nanolab SR Series. This system, the Nanolab DL3206 SEM, is based on the same SEM technology as the Nanolab SR tool. The difference in the two systems is that the Nanolab DL3206 SEM is designed for use in process development and troubleshooting, such as in the early stages of setting up a production line. In contrast, the Nanolab SR Series is designed for in-line processing in a production environment. The price of the DL3206 system is approximately $350,000.

Manufacturing of the Quaestor system occurs at Nanoquest's headquarters in York, England. Nanoquest's U.S. office is located in Woburn, Massachusetts, while the Canadian office is located in Nepan, a suburb of Ottawa, Ontario. The Nepan office is where e-beam instrument design, development, and manufacturing take place.

Orasis

Orasis Corporation (Sunnyvale, California) recently has developed a proprietary 3-D imaging technology that it plans to combine with its submicron positioning technology in the development of a new high-speed advanced wafer defect detection system for patterned wafers. Details on the new system and its availability have not been released.

Since its inception in 1985, the company has specialized in the design, manufacture, and sale of precision motion systems for vacuum and nonvacuum applications with 1-micron and submicron resolution.

Opal Inc.

Opal Inc. (Billerica, Massachusetts) is a new entrant in the wafer metrology equipment market. Opal was established in December 1986 by Optrotech Ltd. and several other investors including Adler & Company and TA Associates, a large international venture capital firm. Optrotech, a manufacturer of inspection equipment for the printed circuit board industry, has a 31.5 percent interest in the $4.6 million investment, and the investor group led by TA Associates has a majority interest of 58 percent. The remaining investment was funded by Opal management.

Optrotech began development of an e-beam-based CD measurement system in late 1985, and established Opal Inc. as a separate business operation to finish product development and implement manufacturing, sales, and marketing operations. Opal Inc., in turn, established a wholly owned subsidiary, Opal Technologies Ltd. (Nes Ziona, Israel), that is conducting the research and development effort. The CD measurement system, known as Opal 702, was designed for automatic submicron metrology of wafers in the production environment. The throughput of the system is approximately 11 to 15 wafers per hour at five sites per wafer, although the company expects to increase this rate by using fully automatic e-beam pattern recognition. The price of the 702 system ranges between $600,000 and $800,000, depending on options. Opal shipped its first system to a customer in 1988.

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Optical Specialties, Inc.

Optical Specialties, Inc. (OSI; Fremont, California) manufactures a family of products for optical CD measurement and wafer inspection.

Wafer Inspection Stations

The company introduced its first wafer inspection stations in 1980. Since that time, OSI's wafer inspection products have included the single-cassette MV-7, the four-cassette MV-10, and the fully programmable MV-15 inspection stations. These tools ranged in price from $25,000 to $50,000. In 1986, OSI introduced the MV-360. The system featured a robotic wafer-handling system that was characterized by a very low contaminant count. The system was capable of handling 3-inch to 150mm wafers, and was priced at approximately $65,000. At SEMICON/West in May 1988, OSI introduced the MV-400, a dedicated wafer inspection station that replaced the MV-360 system. The major enhancement in the MV-400 is a new design of the automated wafer-handling system. The price of the MV-400 is approximately $85,000.

Optical CD Measurement Systems

OSI introduced its first linewidth measurement system, the VLS-I Video Linewidth System, in 1983. This optical tool provides linewidth measurement on wafers and photomasks and verifies pattern overlay registration on wafers. The VLS-I is priced at approximately $50,000.

At SEMICON/West in May 1988, OSI introduced the MV-500 system, the next-generation system of the VLS-I linewidth measurement tool. The MV-500 incorporates OSI's LaserLine technology, a solid-state infrared laser autofocus system for improving measurement precision. The MV-500 has 0.5-micron measurement capability in a production environment. The average selling price of the MV-500 with the LaserLine technology is approximately $100,000. The system with an automatic wafer handler is priced at $125,000.

In May 1989, OSI introduced its latest submicron measurement system, the OSI 2000. Like the MV-500, the OSI 2000 utilizes the LaserLine autofocus system and has 0.5-micron measurement capability. In addition, the system has been designed with Reichert optics, has 200mm wafer capability, and has a throughput level for CD measurement of 60 wafers per hour at five sites per wafer. The OSI 2000 is priced at approximately $400,000. The company expects the product to be available in fourth quarter 1989.

Joint CD/Inspection Stations

In late 1983, OSI began shipments of its first two systems that provide integrated wafer inspection and linewidth measurement capability. These tools, the MV-207 and the MV-215, combined the VLS-I linewidth measurement system with the MV-7 and MV-15 wafer inspection stations. The MV-207 and MV-215 were priced at $65,000 and $100,000, respectively.

The MV-PLUS wafer inspection and CD measurement station was introduced in 1984. This system provides fully automated measurement capability in addition to programmable wafer inspection. The MV-PLUS was priced at approximately $180,000. In May 1987, OSI announced an applications software package for the MV-PLUS, the Metrology Analysis Program I (MAP-I). This software package receives measurement data from OSI's MV-PLUS and uses it to optimize

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stepper/aligner operating parameters. In May 1988, OSI introduced the MV-PLUS LaserLine, which like the MV-500 incorporates OSI's solid-state infrared laser autofocus system. The MV-PLUS LaserLine is priced at approximately $185,000.

In May 1987, OSI announced the development of its new, fully automatic CD and defect inspection system. The system, first known as the Micropatterning Process Control System, has since been renamed the Inspectra 3000. This system has been designed with machine vision, robotics, and artificial intelligence in order to perform a variety of metrology and inspection tasks without operator intervention. The Inspectra 3000 uses pattern recognition and proprietary software algorithms for automated defect inspection and classification. The system is intended for use in the production environment as well as for the setup and qualification of new processes. The equipment can handle 100mm through 200mm wafers.

OSI received initial funding for this project through R&D Funding, a venture-funding arm of Prudential-Bache. In April 1989, OSI announced that it entered into a combined R&D and licensing agreement with PruTech R&D Partnership II and Toray Industries of Japan. This agreement will allow OSI to complete the development of the Inspectra 3000. The agreement calls for a joint engineering development by both Toray and OSI. Toray will make an initial payment for a technology license and will continue royalty payments based on the future sale of the final product. OSI also has contracted to build initial systems for product introduction in Japan. Marketing rights will be shared between OSI and Toray with Toray retaining exclusive distribution rights in Japan. Toray Industries is engaged in the manufacture and sale of textiles, plastics, and chemical products, in addition to having construction and electronic instrumentation divisions. Toray also supplies the semiconductor industry with a variety of electronic materials including e-beam resist.

General Company Background

OSI was founded in 1978 as an engineering consulting firm for the semiconductor industry and has been a publicly traded company since 1985. In December 1987, Cambridge Instruments agreed to acquire a 40 percent equity interest in OSI in exchange for the transfer of its Reichert-McBain division to OSI. The Microcheck and Polycheck products of Cambridge and Reichert-McBain are now incorporated into the OSI product line of measurement and inspection systems. The Microcheck and Polycheck products are focused on nonwafer fabrication applications such as magnetic head manufacturing and precision hybrid circuit metrology.

Reichert-McBain

As mentioned above, Cambridge Instruments agreed to acquire a 40 percent equity interest in OSI in exchange for the transfer of the Reichert-McBain division to OSI. As part of Cambridge Instruments, Reichert-McBain manufactured optical systems for manual and automated measurement of critical dimensions. The Reichert-McBain facility in Chatsworth, California, was responsible for design, development, and manufacture of the Microcheck and Polycheck products of Cambridge Instruments. These products are now incorporated into the OSI product line of measurement and inspection systems.

In 1986, the company introduced its Wafer MAP Automatic Optical Measurement System for linewidth and overlay measurement. This system, priced at approximately $150,000 to $180,000, was sold in 1986 through early 1987. Reichert-McBain also manufactured a system that was

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complementary to Wafer MAP, the MAP System II Intelligent Measuring System for line and edge measurement in nonsemiconductor industry applications. The price of the MAP product ranged from $80,000 to $120,000.

Reichert-McBain became part of the Cambridge Instruments' organization in May 1986 as part of the merger between Cambridge Instruments and Reichert-McBain, R. Jung GmbH (Heidelberg, West Germany), C. Reichert Optische Werke (Vienna, Austria), and Reichert Scientific Instruments (Buffalo, New York). In addition to products for the semiconductor industry, Reichert-McBain manufactures general application microscopes and industrial 3-D optical inspection stations.

Perkin-Elmer

Perkin-Elmer introduced the OMS 1 Overlay Measurement System at SEMICON/West in May 1987. This overlay system provides fast, precise overlay measurements that are used to optimize the performance of the company's Micralign and Micrastep lithography tools. At SEMICON/Europa 1989, the company exhibited the OMS 10, which incorporates a wafer-handling robot, a wafer prealigner, and dedicated electronics into the existing OMS 1 system. At SEMICON/West in May 1989, Perkin-Elmer exhibited the OMS 100, an ergonomic redesign of the OMS 10 system. In addition to the components of the OMS 10, the OMS 100 includes a new stage and a new computer. The ASP of the OMS 100 is approximately $275,000.

The announcement of Perkin-Elmer's plan to sell its semiconductor division has created some uncertainty regarding this product's future, as well as that of other semiconductor equipment manufactured by the company.

Prometrix

Prometrix (Santa Clara, California) manufactures a linewidth measurement system based on electrical probing techniques. The LithoMap EM-1 (successor to the LithoMap 20) provides extremely fast and accurate linewidth measurement capability. However, it is limited to conductive layers and requires special test wafers. The EM-1, priced at approximately $240,000, is targeted at process setup and qualification of lithography and etch processing. This system does not compete directly in the market with CD measurement equipment used in the production environment.

SiSCAN Systems

SiSCAN Systems (Campbell, California) manufactures a CD measurement and line profilometry system based on the technology of confocal scanning laser microscopy (CSLM). SiSCAN introduced the SiSCAN-IIA in May 1987. The SiSCAN-IIA, like its predecessor the SiSCAN-I, focuses on three-dimensional measurement of linewidths, contact areas, and layer registration. The SiSCAN II-A is designed to measure submicron circuit features in a Class 10 clean room environment. System enhancements include a smaller footprint, a new focus mechanism, and improvements in the speed of stage movements. In addition, the SiSCAN-IIA features an automatic robotic wafer-handling system. SiSCAN announced pattern recognition capability for the SiSCAN-IIA system in May 1988. Wafer throughput for the SiSCAN-IIA is greater than 20 wafers per hour at five sites per wafer, and linewidths can be measured down to 0.3 micron, with 0.005-micron repeatability. Dataquest believes that the first two units were shipped in fourth quarter 1987. The price of the SiSCAN-IIA is currently $350,000.

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The SiSCAN-IIM, priced at $270,000, is a manual version of the SiSCAN-IIA. Dataquest estimates that several systems were shipped in 1987 to both U.S. and European customers. The company's first product, the SiSCAN-I, was introduced in May 1986. It was priced at approximately $240,000.

SiSCAN initially offered its confocal systems with an argon ion laser source (488nm). In early 1988, SiSCAN shipped its first system with a helium cadmium (HeCd) laser source (325nm). As of mid-1989, all SiSCAN systems in the installed base are equipped with the HeCd sources. The shorter wavelength offers several advantages over 488nm illumination, including improved resolution and depth of focus. In addition, many photoresists have lower transmission profiles at shorter wavelengths and, thus, appear more opaque at 325nm than at 488nm. This means that interference effects will be attenuated significantly. Thus, the 325nm source reduces the amount of reflected and scattered light that makes linewidth measurement more difficult at 488nm.

SiSCAN is developing the technology for heavy-mass metrology. Heavy mass refers to sample substrates that are significantly heavier than wafers. Examples include masks, reticles, and erasable optical discs. The scanning mechanism for all SiSCAN tools consists of precise translation of the sample stage in a plane beneath a fixed laser beam and optical components. Heavy-mass metrology requires that existing x-y translation stages for wafers be adapted for heavier sample substrates.

SiSCAN Systems, through a marketing agreement with Shipley/Obelisk, also offers the Monolith workstation. SiSCAN first exhibited this product at SEMICON/West in May 1988. The Monolith workstation provides CD and overlay mapping capability and will plot out stepper correction values for focus and exposure settings. The system can communicate directly to a stepper through a SECS-II communication link. The Monolith workstation was originally developed at GCA, where it was used in conjunction with the GCA stepper to optimize focus and exposure settings. GCA sold the technology to Obelisk, which was later acquired by Shipley.

SiSCAN Systems was founded in 1982 and has received several rounds of venture funding.

Waterloo Scientific

Waterloo Scientific (Waterloo, Ontario) has been developing an automatic optical CD system based on confocal laser scanning microscopy. This system is known as the Model CD-II Critical Dimension Measurement System. A prototype system was first introduced in May 1987, and the company was in final development of the tool in first quarter 1989. Waterloo Scientific is a small, privately owned, Canadian firm. The company was formed in 1983. In addition to its laser scanning microscope products, the company also manufactures a scanning photoluminescence measurement system.

JAPANESE COMPANIES

ABT

ABT (Akashi Beam Technology; Tokyo, Japan) manufactures a family of transmission and scanning electron microscopes for analytical applications. At SEMICON/Japan 1988, ABT exhibited a new CD measurement system based on SEM technology. First announced at SEMICON/East in September 1988, the MEA-4000 is a low-voltage SEM system with measurement capability from 0.1 micron to 28.0 microns with 0.03 (3 sigma) reliability. The system has

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through-the-wall mounting and can handle 125mm, 150mm, and 200mm wafers. Throughput is greater than 15 wafers per hour at three measurement sites per wafer. In addition, the system has a simplified control panel as compared with its predecessor, the MEA-3500F, and other typical SEM systems. The price of the MEA-4000 is ¥120 million in Japan. Several systems were shipped to Japanese semiconductor manufacturers during 1988.

In addition to the MEA-4000, ABT manufactures the CC-CD system, a cassette-to-cassette SEM-based tool that was designed for linewidth measurement of integrated circuit patterns. The CC-CD system is priced at approximately $375,000 in the United States.

International Scientific Instruments (Milpitas, California) and ISI Korea, Inc., (Seoul, South Korea) are wholly owned subsidiaries of Akashi Beam Technology of Japan.

Canon

Canon (Tokyo, Japan) manufactures the VIR-600 Series of wafer inspection stations for the semiconductor industry. The VIR-600 can operate in 100 percent inspection or random sampling modes. Prior to inspection under the microscope, wafers are passed under a white-light source for visual inspection of gross defects and flaws in the wafer surface. Detection and classification of pattern defects are performed visually by an operator with the aid of a microscope station. Since 1985, Canon has had a marketing agreement with Aeronca (acquired by Estek in 1986) to supply the company with VIR-600 wafer inspection systems for marketing and sale in the United States.

Canon introduced a new model, the VIR-630, at SEMICON/Japan in December 1987. The new VIR-630 differs from the 600 in that the individual wafer transport time has been reduced by a factor of 3, down to approximately 3 seconds. The price of the VIR-630 is approximately ¥11 million in Japan. Sales to Japanese semiconductor manufacturers began in summer 1987. The VIR-600 system was first introduced in 1982. It is priced at approximately ¥8 million in Japan.

In addition to its wafer inspection stations, Canon manufactures a laser-based system that measures particulate contamination on the wafer surface. The model name of this tool is The Standard. This system does not compete directly in the same market segment as the other wafer inspection equipment discussed in this study.

Canon is a major manufacturer of semiconductor processing equipment including projection aligners, steppers, and contact/proximity aligners, as well as automatic photoresist processing equipment.

Dainippon Screen

Dainippon Screen (Kyoto, Japan) introduced an optical linewidth measurement system at SEMICON/Japan in December 1987. The system has a minimum linewidth measurement capability of 0.8 micron. At the time of introduction, the SLM 601 was still under development. Dataquest believes that system shipments began in 1989. Other Dainippon Screen products in the process control equipment category include automatic film thickness measurement systems and tools for trench depth measurement. The company also manufactures automatic photoresist processing equipment and wet processing systems.

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Hitachi

Two Hitachi equipment companies have several product offerings in the process control area, including optical and SEM-based CD measurement systems. In addition, Hitachi's equipment groups manufacture a wide variety of front-end processing equipment including e-beam lithography tools, steppers, etch equipment, ion implanters, CVD systems, and sputtering equipment.

Hitachi Electronics Engineering Co.

Hitachi Electronics Engineering Co., Ltd., (Hitachi Deco; Tokyo, Japan) manufactures the Lithography Accuracy Measuring Unit (LAMU) system for CD measurements. The LAMU-600 has nominal linewidth measurement of 0.8 micron, and 0.03-micron repeatability for overlay measurement. The LAMU-600, a production-oriented CD measurement system, is priced at ¥60 million in Japan. As yet, there has been no marketing of the LAMU-600 in the United States. This is because the LAMU-600 requires extensive software for interfacing with stepper and other lithography systems. At this time, Hitachi is still investigating the necessary software system capability that would be required to market the LAMU-600 effectively to the U.S. semiconductor industry.

In addition to the LAMU measurement system, Hitachi Electronics Engineering Co. manufactures the HILIS-200 and IS-1000 products, which are used to inspect the surface of wafers for particulate and defect contamination. Hitachi introduced the IS-1000 at SEMICON/Japan in December 1987. The IS-1000 is the newest generation of the company's HILIS-200 inspection system. Both of these tools utilize a highly sensitive detector to detect ultrafine foreign particles that adhere to the surface of a wafer. This is done by directing a laser beam over the wafer surface and detecting scattered light from the particles. The IS-1000 has a detection limit of 0.8 micron (first layer) to 2.0 microns (second or third layer, aluminum layer) on patterned wafers, compared with the HILIS-200 detection limit of 2.0 to 3.0 microns. The IS-1000 detection and measurement rate is on the order of 6 to 7 minutes per wafer, and, as such, the system has been designed for R&D, analytical, and process qualification operations. The HILIS-200 operates at twice the speed of the IS-1000, and is used extensively in the production environment. The HILIS-200 is priced at ¥50 million, while the new IS-1000 is approximately ¥90 million in Japan. Deliveries to Japanese customers began in first half 1988. Hitachi Electronics Engineering and FSI International of Chaska, Minnesota, announced an agreement in mid-1989 that FSI will market and distribute Hitachi's particle-counting systems in the eastern United States.

Hitachi's HILIS-200 and IS-1000 systems do not compete directly in the same market segment as the other wafer inspection equipment discussed in this study.

Hitachi Denshi

Hitachi Denshi (a different Hitachi equipment company from Hitachi Deco) manufactures the S-6000 Critical Dimension Measurement SEM system. This tool, priced at ¥90 million in Japan, was introduced in the 1984/1985 time frame. Since then, Hitachi Denshi has established itself as the leader in CD SEM tools with more than 90 percent of its systems currently being used in a production environment. Wafer throughput for the S-6000 is on the order of eight wafers per hour at five sites per wafer.

Hitachi introduced a new CD SEM measurement system, the S-7000, at SEMICON/Japan 1988. The S-7000 is a new and enhanced version of its popular S-6000 CD SEM. One new major

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design feature of the S-7000 is that it provides five-axis control (x, y, z, tilt, and rotation), whereas the S-6000 provides only x-y control. Measurement capability of the system is down to 0.1 micron with 0.02-micron measurement reliability. Wafer throughput is five wafers per hour at five measurement sites per wafer. The S-7000 can handle wafers of 100mm, 125mm, and 150mm diameter. Shipment of the S-7000, priced at ¥120 million in Japan, began in September 1988.

Holon

Holon (Tokyo, Japan) manufactures a low-voltage, e-beam, submicron metrology system designed for automated CD and registration measurements. The system's primary applications are in the characterization of process parameters in the initial stages of process development and in process control monitoring, as device volumes increase. This nondestructive measurement system can measure linewidths down to 0.1 micron, with a precision that is less than or equal to 0.05 micron (3 sigma) for automatic CD measurement. Wafer throughput is greater than 15 wafers per hour at five sites per wafer. The ESPA-11, first introduced in 1985, is priced at ¥90 million in Japan. This price includes an extended service warranty.

In November 1986, Holon and KLA Instruments announced an agreement by which KLA would have exclusive distribution rights to the ESPA-11 in the United States and Europe. KLA markets the ESPA-11 under the name KLA/Holon 2711. Holon was formed by several ex-JEOL engineers. NKK, the Japanese steel manufacturer, has a 20 percent equity position in the company.

JEOL

JEOL (Tokyo, Japan) manufactures a series of SEM systems. The JEPAS-1200 has been geared toward CD measurement in the production environment. Wafer throughput is on the order of 10 wafers per hour at five sites per wafer, and the system is priced at approximately $450,000 in the United States. In addition to manufacturing SEM microscope systems, JEOL is a major manufacturer of maskmaking and direct-write e-beam lithography equipment. JEOL's U.S. offices are in Peabody, Massachusetts.

Lasertec

Lasertec (Yokohama, Japan), formerly NJS Corporation, manufactures an automatic reticle qualification system known as the model 3WD36 Automatic Wafer Inspection System. This system was designed with high-resolution objective lenses and confocal laser optics, which allow wafers to be inspected for defects down to 0.5 micron. The high-speed inspection system converts the images of two adjacent dies to video signals that are compared with each other to detect the presence of defects. Defect coordinates, which are stored in the system computer, can be recalled by the operator for directing wafer stage movement during defect confirmation and classification. Dataquest believes that Lasertec shipped its first system in the latter half of 1987. The 3WD36 is priced at approximately ¥78 million in Japan.

In addition to its automatic wafer inspection system, Lasertec manufactures the 1LM11 Laser Scanning Microscope and the 2LM11 Color Laser Scanning Microscope, each with CD measurement capability. The 1LM11 Laser Scanning Microscope utilizes confocal optics to provide a high-quality image capable of 0.3-micron measurement. The 1LM11 is best suited for the R&D environment or the area of quality and process control applications, as the 1LM11 has no automatic wafer-handling capability.

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The 2LM11 Color Scanning Laser Microscope, also designed with confocal optics, utilizes beam output from both helium-neon and argon ion lasers to produce a real-time high-quality color image. The system, which includes a CD measurement system, has measurement capability of 0.3 micron and an optional optical beam-induced current (OBIC) display. An OBIC is produced when a light beam is focused on the surface of a p-n junction. When viewing the OBIC image, it is possible to observe real-time internal current flow by varying the TTL input signal. Applications for both the 1LM11 and 2LM11 systems outside the semiconductor industry include the study of metal surfaces, ceramics, polymers, synthetic textiles, and biological/biomedical specimens.

Lasertec's 3WD36, 1LM11, and 2LM11 products do not compete directly in the same market segment as the other wafer inspection and CD measurement equipment discussed in this study.

In addition to these products, Lasertec is also a major manufacturer of automatic mask/reticle inspection systems for the semiconductor industry.

Nidek

Although Nidek (Gamagori, Aichi, Japan) has been a significant supplier of wafer inspection equipment in Japan for a number of years, the company has only recently entered the arena of optical CD measurement systems. At SEMICON/Japan in November 1988, Nidek displayed two different versions of its CD-10 optical CD measurement system. The CD-10S is a standalone linewidth measurement tool, first introduced at SEMICON/Japan in 1987. The CD-10C system consists of the CD-10S plus Nidek's IM-9, a wafer handling system that employs belts in wafer transport. SEMICON/Japan 1988 was the first time the CD-10C was exhibited. The CD-10C system costs approximately ¥10 million; the CD-10S is priced at ¥5 million in Japan.

Nidek's product offerings in wafer inspection equipment include the IM-8A, the IM-8B, and its recently introduced IM-7 system. All three models are based on the traditional operator-dependent microscope station for the detection and classification of defects on patterned wafers. The IM-8A and IM-8B models include autofocus, automatic alignment, and automatic wafer handling. The difference between the 8A and 8B models is the configuration of input and output cassettes. The 8A and 8B are both priced at approximately ¥10 million. At SEMICON/Japan 1988, Nidek exhibited a new wafer inspection station, the IM-7. This system employs a robotic wafer handling system rather the belt-based transport system employed on the IM-8 systems. With the new robotic wafer handling system, the IM-7 provides better contamination control. The price of the IM-7 is approximately ¥10 million to ¥15 million, depending upon options.

In addition to wafer inspection systems and CD measurement tools, Nidek manufactures wafer-flatness measurement equipment.

Nikon

Nikon (Tokyo, Japan) manufactures both CD and wafer defect inspection stations for the semiconductor processing environment. Nikon's linewidth measurement systems have included the LAMPAS-M2 and -M3, as well as its newest system, the LAMPAS-HD. In the area of wafer inspection, Nikon manufactures a family of products: the Optistation 1, 1A, 2, 2A, and 3 systems.

Nikon's newest CD measurement system, the Incident-Light Micro-Pattern Analyzer LAMPAS-HD, was introduced in September 1987. As with its predecessors, the LAMPAS-M2 and -M3, the HD utilizes Nikon's patented scanning laser design for pattern-edge detection to

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determine CD and registration overlay measurements on wafers and masks. The linewidth is determined by scanning a precisely focused laser beam over the circuit pattern edges and then using a high-resolution laser interferometer to measure the distance between the edge detection pulses. The LAMPAS-HD, however, uses a helium-cadmium laser with a 325nm wavelength, rather than the helium-neon source (628nm) of the M2 and M3 systems. The shorter wavelength improves linewidth measurement capability. In addition, the laser spot size of the HD has been reduced from 1 micron x 5 micron of the M3 system to 0.4 micron x 0.4 micron, and the laser spot scan distance is 30 microns, rather than the 100-micron range of the M3.

The LAMPAS-HD system is a fully automated CD measurement tool and is capable of measuring linewidths down to 0.6 micron on silicon wafers with 1.0-micron-thick photoresist lines. Nikon cites linewidth measurement capability of 0.5 micron and repeatability specifications of less than 0.024 micron on chrome masks. Wafer throughput for the system is approximately 35 wafers per hour at five measurement sites per wafer. Shipment to Japanese customers began in October 1987. The price for the LAMPAS-HD in Japan is approximately ¥60 million. The price in the United States is approximately $500,000.

The LAMPAS-M3 was introduced in Japan in 1983. The LAMPAS-M3 minimum linewidth measurement capability has been specified at 0.8 micron on a hard chrome mask, with repeatability of 0.05 micron or better. Wafer throughput is greater than 30 wafers per hour at five sites per wafer. The price of the LAMPAS-M3 is approximately $165,000. The M3, first introduced in the United States in 1984, has not received wide acceptance in this region. Dataquest estimates that more than 80 percent of the LAMPAS-M3 installed base is in Japan.

The predecessor of the LAMPAS-M3 was the LAMPAS-M2 system. The LAMPAS-M2 was introduced in Japan at the end of 1978. The first system was shipped to a customer in Japan in 1979, and the last sale of this measurement system was in February 1984. Dataquest estimates that approximately 95 percent of the installed base of the LAMPAS-M2 is in Japan. The price of the LAMPAS-M2 was approximately $110,000.

In addition to its LAMPAS family of CD measurement systems, Nikon manufactures the Optistation line of wafer inspection stations. The Optistation 1 was introduced in 1982, the Optistation 2 in 1984, and the 2A in 1985. In 1987, Nikon introduced the Optistation 1A. The difference between the Optistation 1 and 2 series is that the Optistation 2 series of wafer inspection systems can be interfaced directly in-line with track and lithography equipment. Not all semiconductor manufacturers require this capability, so Nikon offers the Optistation 1 series, which does not have the interface feature. The Optistations 1 and 2 are 3-inch to 125mm compatible, while the models 1A and 2A are 100mm to 150mm compatible. The Optistation capabilities were expanded when SMIF compatibility was announced in May 1986.

The Optistation systems in the United States are typically configured as four-cassette systems with one-cassette input and three-cassette output for rework, accept, and reject. In Japan, the typical system configuration includes only accept and reject output cassettes, since Japanese manufacturers often do not perform rework on processed material. The Optistation 1 and 2 series of systems range in price from $50,000 to $80,000. While the Optistation is primarily a wafer defect inspection system, an optional linewidth measurement module is available at a cost of $35,000.

At SEMICON/West 1989, Nikon introduced the Optistation 3, its latest product offering in its family of wafer inspection stations. The major enhancement of the Optistation 3 is that it employs a linear robotic arm for wafer transport in order to provide improved contamination control over

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the belt transport system of its predecessor, the Optistation 2 series. The Optistation 3 is capable of handling wafers of 100 to 150mm diameter. Shipments of the Optistation 3 are expected to commence in the United States in autumn 1989. The price in the United States will be approximately $100,000 to $120,000. Shipments of the Optistation 3 systems in Japan began in first quarter 1989.

In addition to producing the LAMPAS measurement systems and Optistation inspection equipment, Nikon is a major manufacturer of wafer steppers and mask metrology tools for the semiconductor industry. Nikon Precision Incorporated (San Bruno, California) was formed in 1982 as a subsidiary of Nikon Corporation of Japan. Nikon Precision supports Nikon's sales, marketing, service, and technical support operations in North America for lithography, as well as mask and wafer metrology products. Nikon, Inc. (Garden City, New York) is responsible for sales, marketing, service, and technical support for Nikon's microscope-based products, such as the Optistation equipment. In addition to its internal lens manufacturing operations for its steppers, Nikon is a world leader in the production of high-quality optics for cameras, microscopes, medical, and scientific instrumentation.

Olympus

At SEMICON/West in May 1988, Olympus introduced its Cue 2000 Wafer Inspection Station. The Cue 2000 utilizes image recognition software and a user-defined defect library to perform operatorless defect inspection based on the automatic identification of 15 different defect types. Since the defect types are preprogrammed, the Cue 2000, can, in a sense, perform both automatic defect detection and classification. Olympus, a major Japanese manufacturer of optical components, undertook all system development for the Cue 2000 in the United States at its Precision Instrument Division in Lake Success, New York. Although Olympus has been a long-time supplier of standalone microscope products to the semiconductor industry, the Cue 2000 is the company's first systems-level offering for the semiconductor production environment. The Cue 2000, currently in beta site, is expected to be available by the end of 1989 and will be priced at approximately $150,000.

Ryokosha

Ryokosha (Tokyo, Japan) manufactures a video-based linewidth measurement system for the semiconductor industry. The MF-68 system consists of a telecomparator, video camera, and computer system with autofocus and variable threshold selection. The MF-68 has been manufactured for approximately 15 years and was jointly developed by Hitachi and Ryokosha. It began as a manual measurement tool and gradually has become more automated. The MF-68K, introduced in 1987, is the latest generation of the MF-68 systems, and it contains 100 programmable routines for linewidth measurement. The MF-68K is priced at approximately ¥10 million, while the MF-68 is priced at about ¥7 million. Essentially all of Ryokosha's sales of linewidth measurement systems have been in Japan only a small fraction of the company's installed base is in export markets.

Sony

Sony (Atsugi-City, Kanagawa, Japan) developed the ARQUS-20 Automatic Reticle Qualification System in 1979, and turned it into a commercial product in 1985. The ARQUS-20 utilizes a proprietary defect detection algorithm to perform a die-to-die comparison of the wafer

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image in order to detect the presence of defects. The defect specification on the ARQUS-20 is 0.8 micron at an 11-minute-per-square-centimeter scan rate. In 1988, Sony introduced the ARQUS-30, which has an improved defect detection sensitivity of 0.5 micron at the same scan rate as the ARQUS-20. Sony's ARQUS-20 is priced at approximately ¥80 million in Japan; the new ARQUS-30 is priced between ¥85 million and ¥90 million, depending upon options.

EUROPEAN COMPANIES

Cambridge Instruments

Cambridge Instruments (Cambridge, England) manufactures the Chipcheck, an optical system for image-to-database comparison of reticles, masks, and wafers. This process qualification system, introduced in 1984, automatically detects and classifies defects or deviations from the original CAD design and corresponding masks, reticles, or processed wafers. This image-to-data base comparative analysis is particularly useful for detecting repeating defects on multi-die reticles and can readily identify standard defects including rat bites, bridges, dirt, and pinholes. The tool primarily is used in mask and reticle inspection; however, Dataquest believes that several customers use the system for wafer inspection in addition to reticle qualification. In the wafer inspection mode, the Chipcheck system compares photoresist images on the silicon wafer directly with the original design data in the CAD database. The minimum defect detection limit is 0.35 micron for isolated defects and 0.5 micron for edge defects. The Chipcheck system is priced at approximately $750,000.

A metrology packet for the Chipcheck system is available for approximately $100,000. The micrometrology capability of the packet for critical dimensions provides measurement capability between 0.5 micron and 1 millimeter with 30 nanometer (3 sigma) repeatability at the smaller geometries. The macrometrology capability provides positional repeatability of 0.15 micron (3 sigma) for distances up to 100 millimeters. At SEMICON/West in May 1989, Cambridge introduced the Quanticheck DBM 1000 (Data Base Metrology System) which combines Chipcheck database inspection and metrology system with Cambridge's Quantimet image analysis system and Reichert Polyvar optics.

In addition to the Chipcheck system, Cambridge Instruments also has been involved in the marketing of an automated e-beam comparator dedicated to submicron linewidth measurement. This system, known as the Scanline, has been developed and manufactured by Angstrom Measurements. Through a marketing agreement between the two companies, Cambridge Instruments had worldwide marketing rights to this system. In December 1988, the marketing agreement was terminated.

Cambridge Instruments was founded in 1881 by Horace Darwin, youngest son of the famous naturalist, Charles Darwin. In May 1986, the Cambridge Instruments organization merged with R. Jung GmbH (Heidelberg, West Germany), C. Reichert Optische Werke (Vienna, Austria), Reichert Scientific Instruments (formerly American Optical Company and Spencer Lens Company, located in Buffalo, New York), and Reichert-McBain. In December 1987, Cambridge Instruments agreed to acquire a 40 percent equity interest in Optical Specialties, Inc., in exchange for the transfer of the Reichert-McBain division to OSI. The Microcheck and Polycheck products of Reichert-McBain are now incorporated into the OSI product line of measurement and inspection systems.

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Cambridge Instruments' semiconductor products include optical microscopes, database metrology and inspection systems, scanning electron microscopes, direct-write e-beam lithography equipment, MOCVD reactors, and single-crystal pullers. Three other major markets for the company are scientific instruments, ophthalmic and medical instruments, and components for industrial process control and automation.

In July 1989, it was announced that Cambridge Instruments and Wild Leitz had agreed to a merger of their two organizations. Although there is some overlap between the optical measurement and inspection instruments of the two corporations, it is believed that the combination of the two companies will create a firm better positioned to compete with the other major manufacturers of optical products, such as Nikon and Olympus of Japan and Carl Zeiss of West Germany. The new company will be called Leica Plc. The merger still must be approved by regulatory authorities in the United Kingdom and Cambridge Instruments shareholders.

Heidelberg Instruments

In January 1989, Wild Leitz acquired Heidelberg Instruments' laser scanning technology and linewidth measurement equipment business and established a new wholly owned subsidiary, Wild Leitz Instruments. (For more information on this company's activities and products, please refer to the section entitled, "Wild Leitz Instruments.") After the acquisition, Heidelberg Instruments still remains as a separate company. It is involved in the development of an automatic wafer inspection system for the semiconductor industry. In addition, the company has developed a laser tomography system for ophthalmic applications. Heidelberg Instruments (located in Heidelberg, West Germany) was formed in 1984 by five researchers from Heidelberg University and four industrial partners.

Micro-Controle

At SEMICON/Europa in March 1989, Micro-Controle (Evry, France) introduced its new Automatic Linewidth and Registration Measurement (ALARM) system and its new Imaging Defect Inspection System (IDIS). Historically, the company's business activities have been focused on precision positioning devices such as micrometers and air-bearing tables. In 1982, Micro-Controle decided to diversify into the semiconductor industry. The ALARM and IDIS products represent Micro-Controle's entry into the front-end semiconductor equipment market.

The ALARM is an optical CD measurement tool with minimum linewidth measurement capability down to 0.5-micron, 10-nm (3 sigma) precision for thick film patterns. System throughput for linewidth measurement is reported to be 60 wafers per hour at five sites per wafer, two measurements per site. This is significantly faster than the standard 25 wafers per hour for most other optical CD systems. The company believes that its fast and accurate stage contributes to this impressive throughput rate.

The IDIS wafer inspection system uses image processing and software algorithms to detect wafer defects on a die-to-die basis. The company hopes to introduce die-to-date base inspection capability by the end of 1989. The IDIS system can be purchased as a separate system or as part of the ALARM. The ALARM is priced between $550,000 and $650,000, while the IDIS is priced at $300,000. A joint CD/inspection version of the ALARM and IDIS systems is priced at approximately $900,000. System shipments began in March 1989 to European customers, while U.S. customers expect delivery later in the year.

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Wild Leitz

Wild Leitz (Wetzlar, West Germany) manufactures microscopes and measurement and inspection systems for front-end and assembly operations within the semiconductor industry. The company's CD measurement systems employed in the front-end production environment are the MPV-CD 2, LTS-M-CD, and the LIS-M-CD systems. The MPV-CD 2 is a standalone optical CD tool priced at approximately $95,000. It was introduced in the late 1970s. The LTS-M-CD, introduced in 1984, is a single-cassette system that incorporates the MPV-CD 2 system, pattern recognition, and an IBM PC system with the automatic wafer-handling capability of the Leitz Transport System (LTS). The LTS-M-CD is priced at approximately $250,000. The LIS-M-CD is similar to the LTS-M-CD, but is a four-cassette rather than a single-cassette system. The LIS-M-CD is priced at $270,000.

Wild Leitz introduced its four-cassette wafer inspection station, the Leitz Inspection Station (LIS) in 1982. This inspection station is priced at approximately $110,000. The company also offers a one-cassette version of the LIS wafer inspection system known as the LTS. This system is priced at $90,000. In May 1989, Wild Leitz introduced the MIS Measurement and Inspection Station. The MIS system is the next-generation development of the LIS wafer inspection station. In addition to a new microscope and improved optics, the MIS system represents Wild Leitz's first offering with 200mm wafer capability in the wafer inspection product area. The price of the MIS system in the United States is approximately $200,000. The first system was shipped to a semiconductor manufacturer in Europe in November 1988.

In addition to its CD and wafer inspection equipment, Wild Leitz manufactures the MPV-SP 2, a film thickness measurement system; the MVG Automatic, a mask comparator system used for image overlay and CD measurements; and a scanning acoustic microscope system with applications in materials research, failure analysis, and device development. Wild Leitz is also a major supplier of optical microscopes and components to OEMs.

Leitz IMS Company (Billerica, Massachusetts) was formed as a partnership between Wild Leitz of West Germany and Image Micro Systems, Inc., of the United States. The LMS-2000 Laser Metrology System, focused on mask metrology applications, provides CDs and pattern-dimensional integrity data with nanometer accuracy and repeatability over an 8 x 8-square-inch area. The LMS-2000 can support the output of several e-beam mask generating systems. Shipments of the LMS-2000 system began in 1987. Today, the tool is priced at approximately $1.25 million.

The name of the company, Wild Leitz, reflects its two parent corporations: Wild Heerbrugg of Switzerland and Ernst Leitz Wetzlar GmbH of West Germany. In the late 1970s, the Leitz family sold a minority interest, and later a majority share, of the Leitz business to Wild. Today, Wild Leitz represents a large conglomerate of business activities centered on optical imaging systems. Major business operations include microelectronics, medical and microscopic diagnostics, and industrial metrology technology.

Wild Leitz Instruments

In January 1989, Wild Leitz acquired Heidelberg Instruments' laser scanning technology and linewidth measurement equipment business and established a new wholly owned subsidiary, Wild Leitz Instruments (Heidelberg, West Germany). Wild Leitz, formerly an investor in Heidelberg

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Instruments, stated that the new company will be concerned exclusively with laser scanning technology and will focus on applications in semiconductor technology, as well as in life and material sciences.

The optical CD metrology system now manufactured by Wild Leitz Instruments is the Line Profile Measurement (LPM) system. The LPM is a confocal laser scanning microscope designed for fully automatic linewidth measurement and line profilometry. The system is designed with telecentric optics that allows a laser beam to be scanned over the wafer surface, which is held fixed in the x-y plane. The LPM measures linewidths down to 0.3 micron, with 0.005-micron repeatability. One of the advantages of confocal scanning laser microscopy is the ability to measure the vertical profile of a circuit feature. The LPM can measure lineheight down to 0.05 micron, with 0.005-micron repeatability. Typical wafer throughput is on the order of 20 to 25 wafers per hour at five sites per wafer.

The LPM was first introduced at SEMICON/Europa in March 1987, and the first system was shipped to a European semiconductor manufacturer in May of that year. The price of the LPM system is approximately $340,000.

At SEMICON/Europa in March 1989, Wild Leitz Instruments introduced a new dual-laser confocal metrology system, the LPM Tandem. This 200mm-compatible system utilizes both an argon ion laser (488nm) and a helium cadmium laser (325nm). The helium cadmium (325nm) source is optimized for linewidth measurements and profiles, whereas the argon source is optimized for overlay measurements. The price of the LPM Tandem is approximately $870,000. The first system was shipped in early 1989.

Zeiss

Zeiss (Oberkochen, West Germany) manufactures the Wafer Inspection Station (WIS). The WIS was introduced in March 1985 at SEMICON/Europa as a basic manual inspection station. Enhancements to the WIS system include a motorized stage, new microscope design, automatic wafer handling and vacuum transport, and computer-controlled operation. In addition, a film thickness measurement option for the WIS was introduced at SEMICON/East in September 1987. The price of the WIS is approximately $100,000. Manufacture of the WIS system occurs at Zeiss facilities in Gottingen and Oberkochen, West Germany.

DEPARTURES

Contrex

Contrex spent six years developing a submicron automated measurement and wafer inspection system, the Wafervision 3000. This system, priced at approximately $600,000 to $800,000, was expected to compete with the KLA 2020. Contrex ceased operations in 1986, after being unable to secure additional funding.

Machine Intelligence

Machine Intelligence undertook preliminary development of an automated CD and wafer inspection station. The company closed its facilities in 1987 after being unable to obtain sufficient venture funding for further product design and development. Technology developed by Machine

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Intelligence for bank note inspection was sold to a European currency-printing equipment manufacturer when the corporation was dissolved.

Optoscan

Optoscan, founded in 1983, spent four years in the development of a laser-based linewidth and overlay measurement system, the model 2010. This system, priced at approximately $240,000, utilized a 325nm laser source and was expected to achieve 0.5-micron measurement capability. General Signal acquired Optoscan in 1985 and closed the subsidiary in 1987, after an unsuccessful effort to market the 2010 system.

Karl Suss

Although Karl Suss (Munich, West Germany) has not officially announced its departure from the wafer inspection equipment market, the company is no longer actively marketing its IP-125 wafer inspection station. The IP-125 wafer inspection system was sold between 1982 and 1984 in Europe and was priced at approximately $40,000.

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CD and Wafer Inspection Equipment Markets

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CD and Wafer Inspection Equipment Markets

SUMMARY

In today's semiconductor industry, line geometries are shrinking, while device complexity, processing steps, wafer size, and mask levels continue to increase. In response to demands for faster measurements with greater resolution, new generations of tools are being developed to meet the requirements of advanced device fabrication. Measurement and inspection equipment is currently undergoing a transition from operator-intensive tools to automated, machine-intensive systems, as the semiconductor industry attempts to overcome the limitations of the human operator.

This study is Dataquest's market analysis of the critical dimension (CD) and wafer inspection equipment markets. In particular, the study focuses on three categories of equipment: optical CD tools, which include automated linewidth and overlay measurement equipment; wafer inspection stations that are used for detecting process-related defects; and joint CD/inspection systems that combine CD measurement capability with wafer inspection. All three types of equipment are based on microscope stations that, in the past, have relied upon operators to perform measurement and inspection tasks. These equipment markets have undergone significant changes in the last few years, as new systems for fully automated measurement and inspection operations have been introduced.

In 1987, the world market for CD and wafer inspection equipment was $94.0 million, of which $39.5 million (42.1 percent) was for optical CD measurement equipment, $24.5 million (26.1 percent) for wafer inspection stations, and $29.9 million (31.8 percent) for systems that combine both measurement and inspection capabilities on the same tool. Table 1 presents the worldwide markets for optical CD equipment, wafer inspection stations, and joint CD/inspection systems for 1982 through 1987.

All three market segments exhibited moderate to healthy dollar growth in 1986 and 1987. The emerging market segment of joint CD/inspection systems has been dominated by the presence of KLA Instruments and its 2020 system, priced at close to $1 million. This system has received attention not only for its price tag, but for its fully automated measurement and inspection capabilities as well. Semiconductor manufacturers in the United States, Japan, and Europe are exploring the applications and economics of these costly joint CD/inspection systems. In the meantime, other equipment companies are developing and introducing new products for this emerging market segment.

Growth, however, in the market segments of optical CD equipment and wafer inspection stations seems contrary to the mood and general business climate of the semiconductor equipment industry during the recession years. In part, the growth in these markets during 1986 and 1987 can be attributed to yen appreciation in Japan, in particular, in the wafer inspection equipment category. However, a far more significant factor affecting all regions of the world has been the increase in the average selling price (ASP) of equipment over the last several years. This is because new measurement and inspection technologies have been developed to keep pace with the shrinking geometries of integrated circuits. New technology advancements typically carry a higher price tag. Thus, it is no surprise that dollar growth in 1986 and 1987 is directly attributable to those companies offering advanced technology products with improved automation capability for submicron measurement and inspection.

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CD and Wafer Inspection Equipment Markets

Table 1

Worldwide Markets for CD and Wafer Inspection Equipment, 1982–1987
(Millions of Dollars)

	1982	1983	1984	1985	1986	1987	CAGR 1982-1987
Optical CD Equipment	$13.4	$22.5	$32.6	$20.1	$28.7	$39.5	24.1%
Wafer Inspection Stations	11.4	16.7	27.1	20.5	21.8	24.5	16.5%
Joint CD/Inspection Systems	0.0	0.7	3.1	13.9	20.3	29.9	155.6%*
Total	$24.9	$40.0	$62.8	$54.4	$70.7	$94.0	30.5%
Growth		54%	72%	(21%)	30%	33%	

Note: Numbers may not add to totals shown due to rounding.
*CAGR for joint CD/inspection systems is taken from 1983 through 1987.

Source: Dataquest
March 1988

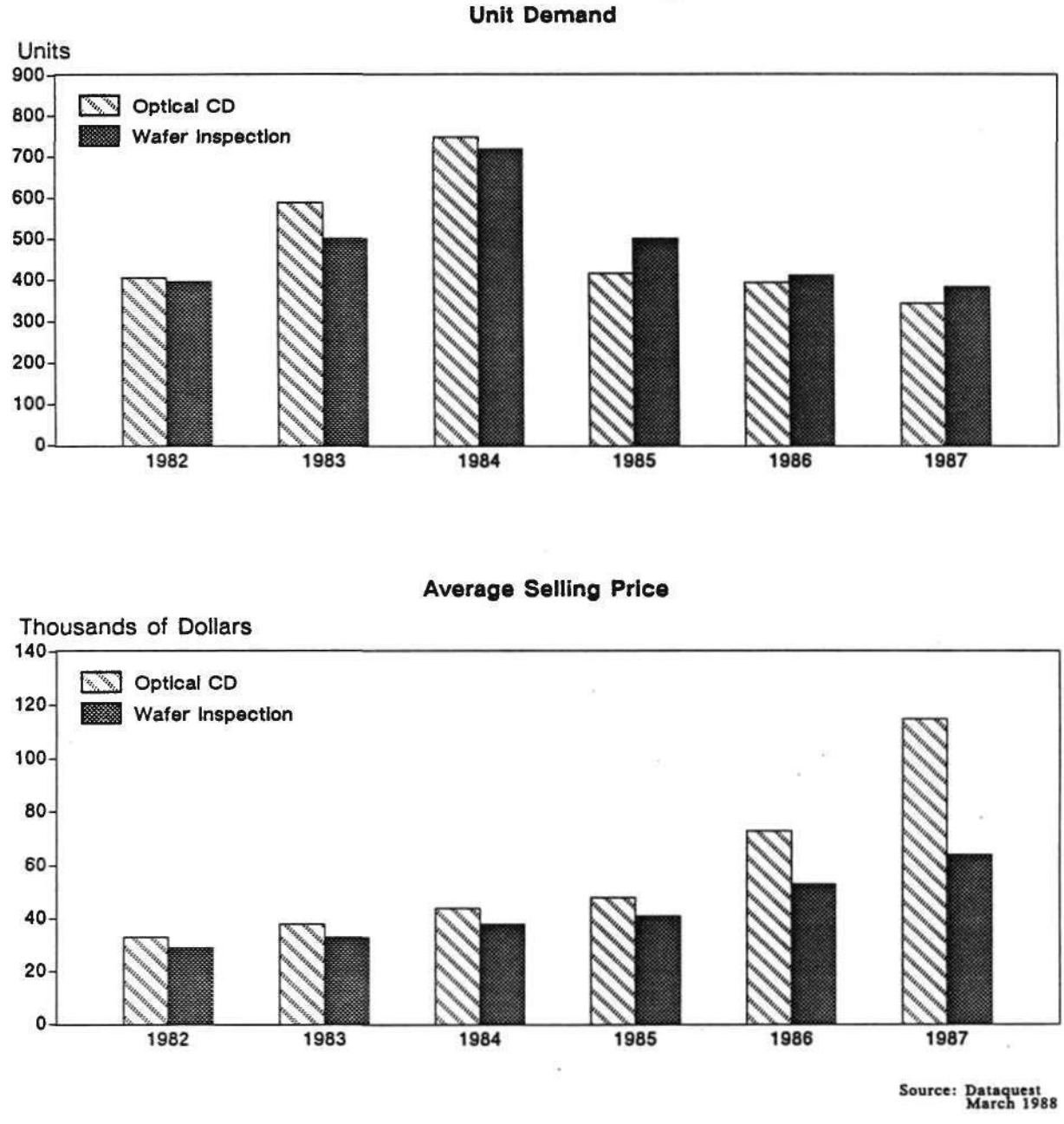
Figure 1 presents a six-year trend in unit demand and ASP for optical CD equipment and wafer inspection stations. As shown in Figure 1, the ASP of optical CD measurement and wafer inspection stations has risen appreciably, while unit demand for both categories of equipment has continued to fall during the last three recession years.

The substantial decline in unit demand for optical CD and wafer inspection equipment in 1985 was clearly a result of the excess capacity within the semiconductor industry. The need for new process control tools—linewidth measurement and wafer inspection equipment, in particular—is tied strongly to the current production level within the fab. With capacity utilization running at 62 percent in 1985, and little or no new technological developments in optical CD and wafer inspection stations, semiconductor manufacturers slashed spending in these equipment categories. Most equipment manufacturers of optical CD and wafer inspection systems continued to experience a decline in unit demand during 1986 and 1987. The growing portion within each market segment was represented by those systems that provided submicron measurement capability and improved equipment automation features.

CD and Wafer Inspection Equipment Markets

Figure 1

Optical CD Equipment and Wafer Inspection Stations Worldwide Unit Demand and ASP, 1982–1987



Source: Dataquest March 1988

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CD and Wafer Inspection Equipment Markets

OVERVIEW

Critical dimension and wafer inspection systems represent segments within the larger equipment category that Dataquest defines as process control equipment. Process control is a broad category that includes equipment for mask and wafer inspection, film thickness measurement, linewidth and overlay measurement, resistivity mapping, process monitoring, surface analysis, and analytical quality control. This is a highly fragmented market with dozens of companies selling into many noncompetitive niches. Dataquest has chosen to focus on CD and wafer inspection systems, because these tools are used in the production environment to provide data, analysis, and feedback on equipment operation and the manufacturing process. The ability to acquire, measure, and analyze information in a timely manner becomes essential, as the semiconductor industry enters a new manufacturing phase in which attention is being focused on the automation of manufacturing processes. While total or "lights-out" factory automation in the semiconductor industry is still years away, automated CD and wafer inspection systems are fundamental components of manufacturing strategy today and will be necessary if lights-out automation is to be achieved.

Critical Dimension

A critical dimension of a semiconductor device refers to a line, element, or feature that must be manufactured and controlled to very tight specifications. In the design of advanced semiconductor devices, design tolerances of critical features are specified at 1/10 the size of the critical dimension. In the case of a 1.0-micron line geometry, that means that fabrication equipment, materials, and processing technology must reproducibly produce a feature that is 1.0 micron, with a deviation of plus or minus 0.1 micron, in order for the manufacturing process to be in control. CD measurement equipment must have very high precision, which means that repetitive measurements are reproducible within a very small range of deviation. The accuracy of a linewidth measurement system describes the nearness of a measurement to its accepted or true value, typically determined by comparison with in-house standards, usually a wafer that is known to be "good." A critical dimension can refer to the dimension of a linewidth in a device pattern at a given mask level, as well as to a measure of the allowable tolerance in the overlay of patterns from multiple mask levels. Typically, CD measurement systems available today perform both linewidth and overlay measurements.

Over the last several years, the field of CD measurement has diversified into a multitude of technologies. Conventional CD tools have been based on white-light microscopy systems. Today, however, this equipment is enhanced with fluorescent measurement capability and image-processing systems. In addition, laser-based measurement systems, confocal scanning laser microscopy, and coherence probe imaging technologies have been developed to perform submicron measurements. Scanning electron microscope (SEM) tools, traditionally relegated to the analytical lab, have been redesigned to meet the needs of submicron manufacturing in a production environment.

CD and Wafer Inspection Equipment Markets

Wafer Inspection

Wafer inspection refers to the inspection of patterned wafers for process defects by visual and image-processing techniques. Traditionally, this equipment has been designed as a microscope station at which an operator visually inspects wafers under magnification for the presence of defects, which range from contaminating particles to defective circuit patterns. As wafer inspection tools have matured, additional features have been added, including automatic wafer handling, automatic and programmable stage movement, autoalignment, autofocus, and keypad data entry systems. In conventional wafer inspection systems today, almost everything but human vision is automated. Recently, a new generation of automatic wafer inspection stations was introduced. These sophisticated systems utilize holographic spatial frequency filtering technology and advanced image-processing techniques to perform automatic defect detection. In some instances, wafer inspection systems assist in defect classification as well.

Wafer inspection equipment discussed in this study focuses on systems that are used for the detection of process-related defects. Market analysis of this equipment segment does not include standalone microscopes or the laser-based surface analyzers that are used to detect and measure particles, scratches, and deformities at the wafer surface.

Reticle Qualification

Reticle qualification systems are used during the setup and process qualification stage of lithographic processing. Typically, every time a reticle or mask is changed on a lithography tool, the reticle qualification procedure is performed to verify reticle quality and optimal lithographic equipment operation. Reticle qualification systems do not compete directly with the wafer inspection stations that are used for defect detection during the production process; thus, "ret qual" systems are considered a separate category from wafer inspection. This distinction becomes somewhat cloudy, because some systems, such as KLA Instruments' 2020 system, are used in both wafer inspection and reticle qualification applications. Reticle qualification systems are discussed briefly in this study, because these systems perform a function that is complementary to wafer inspection.

Joint CD/Inspection Systems

Over the last several years, a new category of measurement and inspection equipment has emerged—systems that are designed for both CD measurement and inspection capability. Dataquest refers to this category of equipment as joint CD/inspection systems. In 1983, Optical Specialties, Inc., introduced the first system designed as a microscope-based inspection station with automatic CD measurement capability. An operator, however, was still required to perform defect detection and classification. In 1984, KLA Instruments introduced its 2020 system, a tool that combines automatic CD measurement with automatic inspection capability. For the first time, the subjective judgement of the operator was removed from the wafer inspection process. The KLA 2020 has received attention, not only on the basis of its

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advanced technology and automated performance, but also because of its price tag, currently $895,000. The KLA 2020 heralded the beginning of a new era in advanced measurement and image-processing technology for the semiconductor industry. The purchase of joint CD/inspection systems now represents a substantial capital investment for semiconductor manufacturers and a significant growth opportunity for equipment manufacturers. In the last year alone, Dataquest noted that several companies were developing new products in this equipment category, and we expect more to follow in the years to come.

For more information on the different measurement technologies of CD and wafer inspection systems, please refer to the service section, "CD and Wafer Inspection Equipment—Technology and Trends."

COMPANY ACTIVITIES

Table 2 contains a list of companies active in the CD and wafer inspection equipment markets. This list, organized by region in which company headquarters are based, summarizes company products by equipment category: optical and e-beam-based CD equipment, wafer inspection stations, reticle qualification systems, and joint CD/inspection systems. While not the primary focus of our market analysis, the categories of e-beam-based CD equipment and reticle qualification systems are included in Table 2 and in the discussion of company activities, because they represent competitive, and, in some cases, complementary technologies and products. In addition to listing new product developments and announcements, Table 2 identifies four companies that are no longer active in these market segments.

In the following discussion of company activities and products, the measurement capability of CD equipment is discussed. The reader is cautioned that specifications of linewidth measurement capability for any model of equipment can vary, depending upon the type, thickness, and combination of semiconductor materials being measured, as well as whether the measurement is being performed in an R&D or a production environment. No attempt has been made to correlate and verify measurement conditions and specifications of the various models of CD measurement equipment discussed in this study.

Prometrix, a manufacturer of linewidth measurement systems based on electrical probing techniques, is not listed in Table 2 because its equipment does not fall into any of the identified product categories. The company, however, is briefly discussed in the following section on U.S. companies.

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CD and Wafer Inspection Equipment Markets

Table 2

CD and Wafer Inspection Equipment Companies by Product Category

	CD Optical	CD e-Beam	Wafer Inspect	Reticle Qualification	Joint CD/Inspect
U.S. Companies					
Amray		X			
Estek (Aeronca)			X		
Insystems			X		
ITP Incorporated	X				
IVS Inc.	X		U/D		
KLA Instruments	X, N/P	X	X	X	X
Nanometrics	X	X			
Opal Inc.		N/P			U/D
Optical Specialties, Inc.	X		X		X
Reichert-McBain*	X				
SiSCAN Systems	X				
Waterloo Scientific	N/P				
Japanese Companies					
ABT (Akashi Beam Technology)		X			
Canon			X		
Dainippon Screen	N/P				
Hitachi	X	X			
Holon		X			
JEOL		X			
Lasertec				X	
Nidek	N/P		X		
Nikon	X		X		
Ryokosha	X				
Sony				X	
European Companies					
Bio-Rad Lasersharp Ltd.	X				
Cambridge Instruments	X	X		X	
Heidelberg Instruments	X		U/D		
Vickers Instruments	X	X			
Wild Leitz	X		X		
Zeiss			X		

(Continued)

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Table 2 (Continued)

CD and Wafer Inspection Equipment Companies by Product Category

	CD Optical	CD e-Beam	Wafer Inspect	Reticle Qualification	Joint CD/Inspect
Departures					
Contrex					X
Machine Intelligence					X
Optoscan	X				
Karl Suss			X		

N/P = New product announcement
U/D = Equipment currently under development
*Acquisition by Optical Specialties Inc. from Cambridge Instruments announced in December 1987

Source: Dataquest
March 1988

U.S. Companies

Amray

Amray (Bedford, Massachusetts) manufactures the Amray 1500, a SEM-based CD measurement system. The Amray 1500 was designed for in-process measurement operations. The system has a throughput of approximately six wafers per hour at five measurement sites per wafer. The Amray 1500 is approximately four years old and is priced at $350,000.

Estek (Aeronca)

Estek, through its acquisition of Aeronca Electronics in late 1986, markets the AE-1000 automated wafer inspection system in the United States. Estek's AE-1000 system is manufactured by Canon of Japan and is the same as Canon's VIR-600 model. The AE-1000 can operate in 100 percent inspection or random sampling mode. Prior to inspection under the microscope, wafers are passed under a white-light source for visual inspection of gross defects and flaws in the wafer surface. The price of the AE-1000 is approximately $80,000, though price increases are expected due to the high rate of yen appreciation. Aeronca Electronics began to market the Canon wafer inspection system approximately three years ago. The Estek division responsible for Aeronca products is located in Charlotte, North Carolina.

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CD and Wafer Inspection Equipment Markets

Insystems

Insystems (San Jose, California) manufactures a fully automated, full-wafer, submicron defect detection system that utilizes holography and spatial frequency filtering technology. The Model 8600 was designed for in-process patterned wafer inspection and can inspect an entire wafer surface for defects in less than 30 minutes. This is in comparison with the several hours required for inspection by conventional optical- or SEM-based inspection tools. This reduction in measurement time is achieved because the Model 8600 relies on parallel optical processing rather than a serial analysis of the wafer on a die-by-die basis. Defect classification is still an operator-dependent task.

The Model 8600, with up to 150mm wafer capability, can detect submicron defects in high-density, repetitive areas in single- and multiple-process levels in photoresist, oxide, polysilicon, metal, and other films, such as nitride, PSG, and polyimide. The Model 8600 is priced at $1.065 million. Insystems first introduced the system in March 1987 at SEMICON/Europa. The U.S. introduction was at SEMICON/West the following May. The Model 8600 was in beta site during 1986, and Insystems shipped its first two systems in fourth quarter 1987.

Insystems, founded in 1981, is a privately held company. Insystem's first product was the Model 8405 automatic photomask inspection system. The first unit, at a price of $800,000, was shipped to Motorola in April 1986. Insystems views the Model 8405 as an interim product and plans to focus on wafer inspection as its primary market.

ITP Incorporated

ITP Incorporated (Sunnyvale, California) manufactures a product line of optical CD measurement equipment including the System 85, Auto CD 88, and System 802. The System 85 is a video-based charge-coupled device (CCD) camera system capable of measuring lines and contacts smaller than 0.5 micron with 2 percent precision. This was ITP's first CD measurement system to combine a CCD camera and personal computer with the company's patented autofocus system. The System 85 is priced at approximately $45,000 to $50,000. The company's Auto CD 88 system, like its predecessor the Auto CD 87, combines the capability of the System 85 with wafer flat and feature location enhancements as well as robotic wafer-handling capability. The Auto CD 88 is priced at $75,000. ITP has been using CCD cameras in its CD measurement systems for approximately three years. ITP also manufactures the System 802 CD measurement system. This tool, also designed with autofocus, is approximately four years old and is priced at $130,000. ITP has been a privately held company since its founding in 1968.

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IVS Inc.

IVS Inc. (Concord, Massachusetts) manufactures a family of CD and registration alignment measurement equipment. The AccuVision products incorporate digital image processing and proprietary software algorithms with an optical microscope system to provide submicron measurement capability. The signal-to-noise ratio is improved by employing various digital enhancement techniques to remove random noise elements introduced by optical and electronic components.

IVS first introduced its AccuVision family of digital image-processing tools in May 1986. The AccuVision family currently includes the ACV-1, ACV-2, ACV-3, and ACV-4, which range in price from $80,000 to $300,000. The AccuVision systems are modular in hardware and software design, and each member of the AccuVision systems can be upgraded to the next system level, without price penalty. The ACV-4, introduced in May 1987, is a fully automatic, cassette-to-cassette system. It can measure linewidth geometries down to 0.3 micron, with .005-micron repeatability. Typical wafer throughput is on the order of 30 wafers per hour at five sites per wafer.

In addition to linewidth and registration alignment measurement and image enhancement routines, IVS provides a Digital Compare software package that can be used to highlight the presence of defects. To implement this function, the operator identifies a given area of the wafer as a "golden" image. Then the system, with its pattern recognition algorithms, performs a comparison analysis of selected portions of the wafer with the "golden" image. The difference between the two digitized signals is presented on a color monitor—areas in red represent what is present on the wafer but should not be, while areas in green identify what is missing on the wafer but should be there.

IVS is developing an automated wafer defect inspection system. The company plans to introduce this system in 1988.

IVS, founded in 1980, began its operations as a manufacturer of digital image processors for scientific applications. The company began to shift its focus to the semiconductor wafer metrology market in 1984 and received its first round of venture funding in early 1985.

KLA Instruments

KLA Instruments (Santa Clara, California) is a major manufacturer of automated image analysis systems for the semiconductor industry. The company's Wafer Inspection Division (WISARD) was formed in 1983; in 1984, it introduced the KLA 2020 Wafer Inspector, the industry's first fully automated wafer inspection system. The KLA 2020 is an in-process wafer inspection system that integrates CD, registration overlay, and area measurements with defect monitoring and macro inspection. The price of the system is $895,000.

Typical wafer throughput for the 2020 on CD measurement is on the order of 90 wafers per hour at five sites per wafer. The KLA 2020 performs a linewidth measurement in a 1.5-second time interval, which includes the time to move to a new position, the time for the system to settle and stop, and, finally, the time for the system to acquire the linewidth image. KLA states that measurements from the 2020 exhibit strong linear correlation with calibrating SEM tools down to 1.0 micron, with a three-nines to four-nines correlation coefficient. Customer applications, however, have included repeatable linewidth measurement down to 0.6 micron.

The KLA 2020 also has automatic defect inspection capability. After the wafer cassettes are loaded, inspection proceeds automatically under the direction of the system computer. The KLA 2020 has defect measurement sensitivity down to 0.5 micron in both repeating and random geometry inspection modes.

The first KLA 2020 system was shipped in early 1985. Dataquest estimates that, at the end of 1987, there were approximately 62 KLA 2020s in the installed base, with about 80 percent of the units in the production environment and 20 percent in R&D facilities. Of those tools used in the production environment, approximately 65 percent are used for defect inspection, while the remaining 35 percent are used for metrology measurements in the lithography area.

In May 1985, the company introduced a major enhancement to the 2020, the Design Reference Generator (DRG). The DRG allows the 2020 to compare a processing level on the silicon wafer with the design data base of the mask or reticle used to expose the wafer. This is an important application in the identification of repeating defects. The price of the DRG is approximately $350,000.

In May 1986, KLA introduced a computer subsystem, the KLA Utility Terminal (KLAUT), which is used with the 2020 to collect, process, and format wafer inspection data into graphics displays for statistical analysis.

In May 1987, KLA introduced the KLA Stepper Set-Up (KLASS), a software enhancement for the 2020. The KLASS software, which loads on the KLAUT, is an applications package for optimizing stepper setup parameters. The KLASS software can optimize the correct focus and exposure settings for a stepper in approximately 4 minutes and produces a picture of the stepper control screen on the KLAUT terminal in order to guide the operator in changing new focus and exposure settings. The KLASS software package is priced at $20,000. The second software enhancement for the KLA 2020 was introduced in September 1987. The Product Wafer Detect Audit (PWDA) assists the user in identifying the cause of defects. It sells for approximately $30,000.

Since early 1987, KLA has offered the KLA 2005, a metrology-only version of the 2020. This system, which has no defect inspection capability, has been targeted specifically at the lithography area of the fab. The 2005 is priced at approximately $700,000, which includes a KLAUT computer and the KLASS software applications package. Several 2005 systems that were sold in 1987 were upgraded later to full 2020 systems. The price of the upgrade is approximately $300,000.

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CD and Wafer Inspection Equipment Markets

In September 1987, KLA introduced two new wafer inspection systems, the KLA 2028 and the KLA 2030. The KLA 2028 automatic wafer defect inspection system retains the same macro defect detection capability as the KLA 2020; however, the new 2028 is capable of micro defect detection at rates of speed approximately 4 times (for random geometry inspection) to 15 times (for repeating array inspection) faster than those of the KLA 2020. The KLA 2028, a dedicated defect inspection system, is priced at $895,000. The KLA 2030 Automatic Wafer Defect Inspection and Metrology system combines the metrology capability of the KLA 2020 with the enhanced defect detection capability of the new 2028. The price of the KLA 2030 is $1.095 million. Current owners of the KLA 2020 can retrofit their systems to full 2030 performance capability at a cost of approximately $300,000. For customers with 2020 systems on order, backlog conversion to the 2028 will be performed at no charge, and conversion to the 2030 will be priced at $200,000. First shipments of the KLA 2028 and 2030 are expected in March 1988.

KLA Instruments is developing a coherence probe microscope system for CD measurement beyond the limit of conventional white-light optical systems. The coherence probe microscope utilizes a Linnick microscope, which is essentially a Michelson interferometer with the addition of two microscope objectives. The technique of coherence probe imaging (CPI) produces images by applying electronic algorithms to a particular set of interference images taken from the Linnick interference microscope. The coherence probe microscope system also provides three-dimensional detail of line geometry measurements. This system, known as the KLA 5000, has a measurement resolution of 0.7 micron and wafer throughput is 40 to 45 wafers per hour at five sites per wafer. The system is priced at approximately $380,000. In March 1988, KLA introduced the KLA 5000 at SEMICON/Europa in Zurich, Switzerland, and presented preliminary results of the KLA 5000's operations at the SPIE meeting in Santa Clara, California. KLA Instruments currently has a patent pending on the coherence probe microscope.

In addition to the manufacture of optical CD/inspection systems, KLA distributes the KLA/Holon 2711, a low-voltage, e-beam, submicron metrology system designed for automated CD and registration measurements. Its primary applications are in the characterization of process parameters in the initial stages of process development and in process control monitoring as device volumes increase. Wafer throughput is greater than 15 wafers per hour at five sites per wafer, and the system can handle 100mm through 200mm wafers. This nondestructive measurement system can measure linewidths down to 0.1 micron, with a precision less than or equal to 0.05 micron (3 sigma) for automatic CD measurement. The price of the 2711, depending on options, is less than $500,000. The KLA/Holon 2711 is the first product to be introduced under an agreement announced in November 1986 by KLA and Holon Co., Ltd., of Japan. KLA is the exclusive distributor of the 2711 in the United States and Europe.

KLA Instruments was founded in 1976 and has been a publicly traded company since October 1980. Over the years, KLA has successfully developed a family of advanced inspection systems for use in various segments of the semiconductor industry. The company is structured into three operating divisions: the Reticle and Photomask Inspection Division (RAPID), the Wafer Inspection Division (WISARD), and the

Automated Test Systems Division (ATS). A new division recently was established to focus on supplying inspection systems to the printed circuit board industry; first deliveries are scheduled for 1988.

Nanometrics

Nanometrics (Sunnyvale, California) manufactures optical linewidth measurement equipment for the semiconductor industry. Its first Nanoline system was shipped in 1978, and total installations of Nanometrics' optical linewidth measurement systems number on the order of 1,000 units. The Model 50, introduced in 1986, replaced its predecessors, the Nanoline V and VA.

The Model 50 measurement technology is based on a narrow optical slit that is mechanically stepped across a magnified image of the wafer feature. The light passing through the slit is measured by a photomultiplier tube (PMT) to form a high-resolution reflectance profile. The profile is stored on the system computer and analyzed to determine the linewidth of the wafer feature. The primary changes between the Model 50 and the Nanoline V and VA include improved autofocus algorithms, faster measurement times, better system measurement linearity, and improved equipment uptime. The linewidth measurement capability of the Model 50 is approximately 0.7 to 0.8 micron in a production environment. The price of this system is about $45,000.

The Model 50 optical linewidth measurement system, like its predecessors in the Nanoline family of equipment, does not have wafer-handling capability. Recently, however, Nanometrics developed the NanoStation-1, which is an optional wafer-loading station for the Model 50. This option now transforms the Model 50 into a fully automatic linewidth measurement system, with wafer throughput on the order of 25 wafers per hour at five sites per wafer. The price of the Model 50 with the NanoStation-1 is $80,000 to $85,000. This wafer handling option for the Model 50 was introduced at the end of 1987.

In 1986, Nanometrics introduced the Model 51 Fluorescence Submicron Linewidth Measurement System. The Model 51 uses the same technology (i.e., a scanning PMT) as the Model 50; however, the system optics were designed for fluorescence linewidth measurement. Fluorescence-based systems provide high-quality images, because the fluorescence signal is generated by the material itself and, as such, is completely incoherent. While this incoherent signal is weak, an important advantage is that it does not produce the ringing or interference effect evident in coherent source systems. Images show a very high contrast, since the fluorescing photoresist features appear against a black (nonfluorescing) substrate background. Nanometrics claims linewidth measurement capability on the Model 51 down to 0.4 micron in the fluorescence measurement mode. Several units of the Model 51 were shipped in 1987. The price is approximately $45,000.

Nanometrics is developing the Model 400 Linewidth and Registration Measurement Station. This fully automated, cassette-to-cassette tool provides both bright field and fluorescence measurement capability for CD and overlay registration measurement. The Model 400 is based on a different technology from that of the Nanoline and Models 50/51

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systems. While the Nanoline and Models 50/51 systems utilize a photomultiplier scanning slit detection system, the Model 400 incorporates a proprietary CCD camera developed by Nanometrics. The CCD camera is particularly well suited for collecting the weak signals associated with fluorescence measurements. Nanometrics displayed a post-engineering prototype system of the Model 400 at the SEMICON/West show in May 1987. The price of the Model 400 is expected to be on the order of $150,000. Shipments are expected to begin in 1988.

In addition to optical linewidth measurement systems, Nanometrics manufactures a fully automated SEM system for linewidth measurement and defect inspection. The Model 100 was designed as an in-line SEM system, with minimum linewidth measurement of 200 angstroms. Wafer throughput is currently about 12 wafers per hour at five sites per wafer; however, the company expects throughput to be increased to approximately 20 wafers per hour, with certain system modifications. The Model 100 was introduced in May 1986, and shipments began in fourth quarter 1986. It is priced at approximately $420,000. The Model 100 is the successor to Nanometrics' CWIKSCAN product line of scanning electron microscopes.

Nanometrics was founded in 1975 and has been a publicly traded company since late 1984. Nanometrics has a wholly owned subsidiary, Nanometrics Japan Ltd., located in Narita, Japan. In addition to the company's optical and SEM-based linewidth measurement systems, other Nanometrics' products include film thickness measurement equipment for the semiconductor industry and ultraviolet, visible, and infrared spectrophotometers for analytical applications. Nanometrics also markets a molecular beam epitaxy system, the model EV100, manufactured by Eiko Engineering of Japan. Nanometrics' majority-owned subsidiary, Loma Park Associates, manufactures a tooling system used in the production of multilayer printed circuit boards.

Opal Inc.

Opal Inc. (Billerica, Massachusetts) is a new entrant in the wafer metrology and inspection systems market. Opal was established in December 1986 by Optrotech Ltd. and several other investors including Adler & Company and TA Associates, a large international venture capital firm. Optrotech, a manufacturer of inspection equipment for the printed circuit board industry, has a 31.5 percent interest in the $4.6 million investment, while the investor group led by TA Associates has a majority interest of 58 percent. The remaining investment was funded by Opal management.

Optrotech began development of an e-beam-based CD system in late 1985, and established Opal Inc. as a separate business operation to finish product development and implement manufacturing, sales, and marketing operations. Opal Inc., in turn, established a wholly owned subsidiary, Opal Technologies Ltd. (Nes Ziona, Israel), that will conduct the research and development effort. The CD measurement system, known as Opal 702, was designed for automatic submicron metrology of wafers in the production environment; however, the company plans to incorporate wafer inspection capability on the system as well. The company claims that the 702 exhibits an impressive throughput rate that is comparable with the rate of most optical-based systems: 30 wafers per hour at five sites per wafer. In March 1988, Opal presented preliminary information on the metrology operations of the Opal 702 system at the SPIE meeting in Santa Clara, California.

Optical Specialties, Inc.

Optical Specialties, Inc. (OSI; Fremont, California) manufactures a family of products for CD measurement and wafer inspection. The company introduced its first wafer inspection stations in 1980. Since that time, OSI's wafer inspection products have included the single-cassette MV-7, the four-cassette MV-10, and the fully programmable MV-15 inspection stations. These tools have ranged in price from $25,000 to $50,000. In 1986, OSI introduced the MV-360. The system features a robotic wafer-handling system that is characterized by a very low contaminant count, as verified by VLSI Standards, a contamination analysis firm in the Silicon Valley. The MV-360 can handle 3-inch to 150mm wafers and is priced at approximately $65,000.

OSI introduced its first linewidth measurement system, the VLS-I Video Linewidth System in 1983. This optical tool provides linewidth measurement on wafers and photomasks and verifies pattern overlay registration on wafers. Equipment specifications quote 0.5-micron minimum measurement capability. The VLS-I is priced at $47,000.

In late 1983, OSI began shipments of its first two systems that provide integrated wafer inspection and linewidth measurement capability. These tools, the MV-207 and the MV-215, combine the VLS-I linewidth measurement system with the MV-7 and MV-15 wafer inspection stations. The MV-207 and MV-215 are priced at $65,000 and $100,000, respectively. The MV-PLUS wafer inspection and CD measurement station was introduced in 1984. This system provides fully automated measurement capability in addition to programmable wafer inspection and is priced at approximately $180,000. In May 1987, OSI announced an applications software package for the MV-PLUS, the Metrology Analysis Program I (MAP-I). This software package receives measurement data from OSI's MV-PLUS and uses it to optimize stepper/aligner operating parameters. The MV-360CD, introduced in May 1987, supplements the wafer inspection station of the MV-360 with CD measurement capability. The price of the MV-360CD is approximately $120,000.

In May 1987, OSI announced its new, fully automatic CD and defect inspection system, the Micropatterning Process Control System. The new system is designed to perform a variety of tasks without operator intervention. The tool automatically receives wafers from robotic material-handling equipment, reads the wafer's identification code (via an alphanumeric optical character reader), creates a wafer pattern array map, performs macroscopic defect inspection and classification, reads the photo mask layer identifier (optical character verification), measures registration and linewidths, detects and classifies microscopic defects, and displays macro or micro images and test data. The OSI system uses pattern recognition and proprietary software algorithms for defect inspection and classification. The Micropatterning Process Control System was designed for use in the production environment as well as for the setup and qualification of new processes. The equipment can handle 100mm through 200mm wafers. The system is expected to go into beta site during the first part of 1988. The system's target selling price will be approximately $500,000. OSI has received funding for this project through R&D Funding, a venture-funding arm of Prudential-Bache.

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CD and Wafer Inspection Equipment Markets

In December 1987, Cambridge Instruments agreed to acquire a 40 percent equity interest in Optical Specialties, Inc., in exchange for the transfer of its Reichert–McBain division to OSI. The Microcheck, Polycheck, and Polycheck VLSI products of Cambridge and Reichert–McBain will now be incorporated into the OSI product line of CD and wafer inspection systems for the semiconductor industry.

OSI was founded in 1978 as an engineering consulting firm for the semiconductor industry and has been a publicly traded company since 1985.

Prometrix

Prometrix (Santa Clara, California) manufactures a linewidth measurement system based on electrical probing techniques. The LithoMap EM–1 (successor to the LithoMap 20) provides extremely fast and accurate linewidth measurement capability. However, it is limited to conductive layers and requires special test wafers. The EM–1, priced at approximately $210,000, is targeted at process setup and qualification of lithography and etch processing. This system does not compete directly in the market with CD measurement equipment used in the production environment.

Reichert–McBain

Reichert–McBain (Chatsworth, California), part of the Cambridge Instruments' organization until December 1987, manufactures optical systems for manual and automated measurement of CDs. In 1986, the company introduced its Wafer MAP Automatic Optical Measurement System for linewidth and overlay measurement. This system, priced at approximately $150,000 to $180,000, was sold in 1986 through early 1987. The product is no longer available, having been replaced by Cambridge Instruments' new Polycheck VLSI system for wafer metrology and inspection. Reichert–McBain also manufactured a system that is complementary to Wafer MAP, the MAP System II Intelligent Measuring System for line and edge measurement in nonsemiconductor industry applications. The price of the MAP product ranged from $80,000 to $120,000. Dataquest estimates that there are approximately 70 systems of the MAP family of products in the installed base, of which one–third are Wafer MAP systems for the semiconductor industry.

The Reichert–McBain facility in Chatsworth, California, is responsible for design, development, and manufacture of the Microcheck, Polycheck, and Polycheck VLSI products of Cambridge Instruments. (See the Cambridge Instruments entry under the section of this service section entitled "European Companies" for more information on these systems.) In addition to its semiconductor products, Reichert–McBain manufactures general application microscopes and industrial 3–D optical inspection stations. In December 1987, Cambridge Instruments agreed to acquire a 40 percent equity interest in Optical Specialties, Inc., in exchange for the transfer of the Reichert–McBain division to OSI. The Microcheck, Polycheck, and Polycheck VLSI products will now be incorporated into the OSI product line of CD and wafer inspection systems for the semiconductor industry. Reichert–McBain became part of the Cambridge Instruments' organization in May 1986 as part of the merger between Cambridge Instruments and Reichert–McBain, R. Jung GmbH (Heidelberg, West Germany), C. Reichert Optische Werke (Vienna, Austria), and Reichert Scientific Instruments (Buffalo, New York).

CD and Wafer Inspection Equipment Markets

SiSCAN Systems

SiSCAN Systems (Campbell, California) manufactures a CD measurement and line profilometry system based on the technology of confocal scanning laser microscopy (CSLM). SiSCAN introduced the SiSCAN–IIA in May 1987. The SiSCAN–IIA, like its predecessor the SiSCAN–I, focuses on three–dimensional measurement of linewidths, contact areas, and layer registration. The SiSCAN II–A is designed to measure submicron circuit features in a Class 10 clean room environment. System enhancements include a smaller footprint, a new focus mechanism, and improvements in the speed of stage movements. In addition, the SiSCAN–IIA features an automatic robotic wafer–handling system. Wafer throughput is greater than 20 wafers per hour at five sites per wafer, and linewidths can be measured down to 0.3 micron, with 0.005–micron repeatability. The price of the SiSCAN–IIA is $350,000. Dataquest believes that the first two units were shipped in fourth quarter 1987. Enhanced computer capability and pattern recognition for the SiSCAN–IIA will be available in summer 1988, and the company will retrofit existing systems for a modest price.

The SiSCAN–IIM, priced at $270,000, is the manual version of the SiSCAN–IIA. Dataquest estimates that a total of four to five systems were shipped in 1987 to both U.S. and European customers. The company's first product, the SiSCAN–I, was introduced in May 1986. It is priced at approximately $240,000. Dataquest estimates that at the end of 1987, SiSCAN had a total installed base on the order of 18 systems.

All SiSCAN confocal scanning laser systems, to date, have utilized an argon ion laser (488nm wavelength) as the illumination source. The company now offers a helium cadmium laser that emits light at 325nm. The shorter wavelength offers several advantages over 488nm illumination, including improved resolution and depth of focus. In addition, many photoresists have lower transmission profiles at shorter wavelengths and, thus, appear more opaque at 325nm than at 488nm. This means that interference effects will be attenuated significantly. Thus, the 325nm source reduces the amount of reflected and scattered light that makes linewidth measurement more difficult at 488nm. SiSCAN Systems expects to ship its first system with a 325nm laser source in early 1988.

SiSCAN is developing the technology for heavy–mass metrology. Heavy mass refers to sample substrates that are significantly heavier than wafers. Examples include masks, reticles, and erasable optical discs. The scanning mechanism for all SiSCAN tools consists of precise translation of the sample stage in a plane beneath a fixed laser beam and optical components. Heavy–mass metrology requires that existing x–y translation stages for wafers be adapted for heavier sample substrates.

SiSCAN Systems was founded in 1982 and has received a total of $10 million in venture funding.

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Waterloo Scientific

Waterloo Scientific (Waterloo, Ontario) manufactures an automatic CD measurement system based on confocal laser scanning microscopy. The system (WSI-1000CD) is priced at approximately $300,000, which includes robotic material-handling capability. A prototype system was first introduced in May 1987, and Dataquest expects deliveries to begin in 1988.

Waterloo Scientific is a small, privately owned, Canadian firm. The company was formed in 1983. Its main products are laser scanning microscopes. In addition to its automatic CD measurement tool, Waterloo Scientific has a second laser scanning microscope system, the WSI 100, which features optical beam induced current (OBIC) measurement for semiconductor material and device characterization. An OBIC signal is produced when a light beam is focused on the surface of a p-n junction. When viewing the OBIC image, it is possible to observe real-time internal current flow by varying the TTL input signal.

Japanese Companies

ABT

ABT (Akashi Beam Technology; Tokyo, Japan) manufactures a family of transmission and scanning electron microscopes for analytical applications. The CC-CD system, in particular, is a cassette-to-cassette SEM-based tool that was designed for linewidth measurement of integrated circuit patterns. The CC-CD system is priced at $375,000. International Scientific Instruments (Milpitas, California) and ISI Korea, Inc., (Seoul, Korea) are wholly owned subsidiaries of Akashi Beam Technology of Japan.

Canon

Canon (Tokyo, Japan) manufactures the VIR-600 Series of wafer inspection stations for the semiconductor industry. The VIR-600 can operate in 100 percent inspection or random sampling modes. Prior to inspection under the microscope, wafers are passed under a white-light source for visual inspection of gross defects and flaws in the wafer surface. For approximately the last three years, Canon has had a marketing agreement with Aeronca (acquired by Estek in 1986) to supply the company with VIR-600 wafer inspection systems for marketing and sale in the United States.

Canon introduced a new model, the VIR-630, at SEMICON/Japan in December 1987. The new VIR-630 differs from the 600 in that the individual wafer transport time has been reduced by a factor of 3, down to approximately 3 seconds. The price of the VIR-630 is approximately ¥11 million ($76,000), and sales to Japanese semiconductor manufacturers began in summer 1987. The VIR-600 system was first introduced in 1982. It is currently priced at approximately ¥8 million ($55,000) in Japan.

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CD and Wafer Inspection Equipment Markets

In addition to its wafer inspection stations, Canon manufactures a laser-based system that measures particulate contamination on the wafer surface. The model name of this tool is The Standard. This system does not compete directly in the same market segment as the other wafer inspection equipment discussed in this study.

Canon is a major manufacturer of semiconductor processing equipment including projection aligners, steppers, and contact/proximity aligners, as well as automatic photoresist processing equipment.

Dainippon Screen

Dainippon Screen (Kyoto, Japan) introduced an optical linewidth measurement system at SEMICON/Japan in December 1987. The SLM 601, which is still under development, has a minimum linewidth measurement capability of 0.8 micron. Automatic wafer handling will be a future option. Deliveries of the SLM 601 are expected to begin in April 1988. Dainippon Screen also manufactures automatic film thickness measurement systems and tools for trench depth measurement.

Hitachi

Hitachi Deco (Hitachi Electronics Engineering Co., Ltd.; Tokyo, Japan) manufactures the Lithography Accuracy Measuring Unit (LAMU) system for CD measurements. The LAMU-600 has nominal linewidth measurement of 0.8 micron, and 0.03-micron repeatability for overlay measurement. The LAMU-600, a production-oriented CD measurement system, is priced at ¥43 million ($300,000) in Japan. As yet, there has been no marketing of the LAMU-600 in the United States. This is because the LAMU-600 requires extensive software for interfacing with stepper and other lithography systems. At this time, Hitachi is still investigating the necessary software system capability that would be required to market the LAMU-600 effectively to the U.S. semiconductor industry.

In addition to the LAMU measurement system, Hitachi Deco manufactures the HILIS-200 and IS-1000 products, which are used to inspect the surface of wafers for particulate and defect contamination. Hitachi Deco introduced the IS-1000 at SEMICON/Japan in December 1987. The IS-1000 is the newest generation of the company's HILIS-200 inspection system. Both of these tools utilize a highly sensitive detector to detect ultrafine foreign particles that adhere to the surface of a wafer. This is done by directing a laser beam over the wafer surface and detecting scattered light from the particles. The IS-1000 has a detection limit of 0.8 micron (first layer) to 2.0 microns (second or third layer, aluminum layer) on patterned wafers, compared with the HILIS-200 detection limit of 2.0 to 3.0 microns. The IS-1000 detection and measurement rate is on the order of 6 to 7 minutes per wafer, and, as such, the system has been designed for R&D, analytical, and process qualification operations. The HILIS-200 operates at twice the speed of the IS-1000, and is used extensively in the production environment. The HILIS-200 is priced at ¥50 million ($350,000), while the new IS-1000 is approximately ¥90 million ($625,000). Deliveries to Japanese customers are expected to begin in April 1988.

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Hitachi's HILIS–200 and IS–1000 systems do not compete directly in the same market segment as the other wafer inspection equipment discussed in this study.

Hitachi Denshi (a different Hitachi equipment company from Hitachi Deco) manufactures the S–6000 Critical Dimension Measurement SEM system. This tool, priced at ¥90 million ($625,000), is three years old. In that time, Hitach Denshi has established itself as the leader in CD SEM tools with over 90 percent of its systems currently being used in a production environment. Wafer throughput for the S–6000 is on the order of eight wafers per hour at five sites per wafer. Dataquest estimates that more than 100 S–6000 systems are in the installed base, of which Japanese customers represent more than 80 percent of shipments.

Holon

Holon (Tokyo, Japan) manufactures a low–voltage, e–beam, submicron metrology system designed for automated CD and registration measurements. The system's primary applications are in the characterization of process parameters in the initial stages of process development and in process control monitoring, as device volumes increase. This nondestructive measurement system can measure linewidths down to 0.1 micron, with a precision that is less than or equal to 0.05 micron (3 sigma) for automatic CD measurement. Wafer throughput is greater than 15 wafers per hour at five sites per wafer. The ESPA–11, first introduced approximately two–and–a–half years ago, is priced at ¥90 million ($625,000) in Japan. This price includes an extended service warranty.

In November 1986, Holon and KLA Instruments announced an agreement by which KLA would have exclusive distribution rights to the ESPA–11 in the United States and Europe. KLA markets the ESPA–11 under the name KLA/Holon 2711. Dataquest believes that Holon has shipped several systems to KLA Instruments in the United States and two systems to Japanese semiconductor manufacturers. Holon was formed by several ex–JEOL engineers. NKK, the Japanese steel manufacturer, has a 20 percent equity position in the company.

JEOL

JEOL (Tokyo, Japan) manufactures a series of SEM systems. The JEPAS–1200 has been geared toward CD measurement in the production environment. Wafer throughput is on the order of 10 wafers per hour at five sites per wafer, and the system is priced at approximately $450,000. In addition to manufacturing SEM microscope systems, JEOL is a major manufacturer of maskmaking and direct–write e–beam lithography equipment. JEOL's U.S. offices are in Peabody, Massachusetts.

Lasertec

Lasertec (Yokohama, Japan), formerly NJS Corporation, manufactures an automatic reticle qualification system known as the model 3WD36 Automatic Wafer Inspection System. This system was designed with high–resolution objective lenses and confocal laser optics, which allow wafers to be inspected for defects down to 0.5 micron. The

high-speed inspection system converts the images of two adjacent dies to video signals that are compared with each other to detect the presence of defects. Defect coordinates, which are stored in the system computer, can be recalled by the operator for directing wafer stage movement during defect confirmation and classification. Dataquest believes that Lasertec shipped its first system in the latter half of 1987. The 3WD36 is priced at approximately ¥78 million ($540,000) in Japan.

In addition to its automatic wafer inspection system, Lasertec manufactures the 1LM11 Laser Scanning Microscope and the 2LM11 Color Laser Scanning Microscope, each with CD measurement capability. The 1LM11 Laser Scanning Microscope utilizes confocal optics to provide a high-quality image capable of 0.3-micron measurement. The 1LM11 is best suited for the R&D environment or the area of quality and process control applications, as the 1LM11 has no automatic wafer-handling capability.

The 2LM11 Color Scanning Laser Microscope, also designed with confocal optics, utilizes beam output from both helium-neon and argon ion lasers to produce a real-time high-quality color image. The system, which includes a CD measurement system, has measurement capability of 0.3 micron and an optional OBIC display. An (OBIC) is produced when a light beam is focused on the surface of a p-n junction. When viewing the OBIC image, it is possible to observe real-time internal current flow by varying the TTL input signal. Applications for both the 1LM11 and 2LM11 systems outside the semiconductor industry include the study of metal surfaces, ceramics, polymers, synthetic textiles, and biological/biomedical specimens.

Lasertec's 3WD36, 1LM11, and 2LM11 products do not compete directly in the same market segment as the other wafer inspection and CD measurement equipment discussed in this study.

In addition to these products, Lasertec is also a major manufacturer of automatic mask/reticle inspection systems for the semiconductor industry.

Nidek

Nidek (Gamagori, Aichi, Japan) manufactures four models of wafer inspection equipment: the IM-8A, IM-8B, IM-6, and IM-9. All four models are based on the traditional operator-dependent microscope station for the detection and classification of defects on patterned wafers. The IM-8A and IM-8B models include autofocus, automatic alignment, and automatic wafer handling. The difference between the 8A and 8B models is the configuration of input and output cassettes. The 8A and 8B are both priced at ¥8 million (approximately $55,000). The IM-6 and IM-9 were new systems for Nidek in 1987 and are priced at ¥2.5 million ($18,000) and ¥6.0 million ($42,000), respectively. Nidek competes with Canon and Nikon in Japan's wafer inspection market.

At SEMICON/Japan in December 1987, Nidek introduced a new optical linewidth measurement system that marks the company's entry into this equipment category. The model CD-10 is priced at approximately ¥5 million ($35,000). Deliveries will begin in 1988. In addition to wafer inspection systems and CD measurement tools, Nidek manufactures wafer-flatness measurement equipment.

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CD and Wafer Inspection Equipment Markets

Nikon

Nikon (Nippon Kogaku K.K.; Tokyo, Japan) manufactures both CD and wafer defect inspection stations for the semiconductor processing environment. Nikon's linewidth measurement systems include the LAMPAS–M2, –M3, and –HD systems, and the company manufactures a line of wafer defect inspection stations, the Optistation 1, 1A, 2, and 2A systems.

The Incident–Light Micro–Pattern Analyzer LAMPAS–M3 was introduced in Japan in 1983. It utilizes Nikon's patented scanning laser design for pattern–edge detection to determine CD and registration overlay measurements on wafers and masks. The linewidth is determined by scanning a precisely focused laser beam over the circuit pattern edges and then using a high–resolution laser interferometer to measure the distance between the edge detection pulses. The M3 has been designed with a helium–neon laser (628nm) as its source, with a laser spot size of 1 micron x 5 microns and a laser spot scan distance of 100 microns.

The LAMPAS–M3 minimum linewidth measurement capability has been specified at 0.8 micron on a hard chrome mask, with repeatability of 0.05 micron or better. Wafer throughput is greater than 30 wafers per hour at five sites per wafer. The price of the LAMPAS–M3 is approximately $165,000. The M3 was first introduced in the United States in 1984 but has not received wide acceptance. Dataquest estimates that more than 80 percent of the LAMPAS–M3 installations, to date, were in Japan.

The predecessor of the LAMPAS–M3 was the LAMPAS–M2 system. The LAMPAS–M2 was introduced in Japan at the end of 1978. The first system was shipped to a customer in Japan in 1979, and the last sale of this measurement system was in February 1984. Dataquest estimates that approximately 70 units were shipped, with about 95 percent of these units going to Japanese customers. The price of the LAMPAS–M2 was approximately $110,000.

Nikon's newest CD measurement system, the LAMPAS–HD, was introduced in September 1987. As with the other LAMPAS tools, the HD employs a laser–based edge detection method; however, the HD utilizes a helium–cadmium laser with a 325nm wavelength, which improves linewidth measurement capability. In addition, the laser spot size has been reduced to 0.4 micron x 0.4 micron, and the laser spot scan distance is 30 microns, rather than the 100–micron range of the M3.

The LAMPAS–HD system is a fully automated CD measurement tool and is capable of measuring linewidths down to 0.6 micron on silicon wafers with 1.0–micron–thick photoresist lines. Nikon cites linewidth measurement capability of 0.5 micron and repeatability specifications of less than 0.024 micron on chrome masks. While wafer throughput specifications are not yet available, the HD is expected to demonstrate the same wafer throughput as the M3, or faster. Shipment to Japanese customers began in October 1987. The price for the LAMPAS–HD in Japan is approximately ¥60 million. The price in the United States has not yet been fixed but is expected to be less than $500,000.

In addition to its LAMPAS family of CD measurement systems, Nikon manufactures the Optistation line of wafer inspection stations. The Optistation 1 was introduced in 1982, the Optistation 2 in 1984, and the 2A in 1985. In 1987, Nikon introduced the Optistation 1A. The difference between the Optistation 1 and 2 series is that the Optistation 2 series of wafer inspection systems can be interfaced directly in-line with track and lithography equipment. Not all semiconductor manufacturers require this capability, so Nikon offers the Optistation 1 series, which does not have the interface feature. The Optistations 1 and 2 are 3-inch- to 125mm compatible, while the models 1A and 2A are 100mm to 150mm compatible. The Optistation systems in the United States are typically configured as four-cassette systems with one-cassette input and three-cassette output for rework, accept, and reject. In Japan, the typical system configuration includes only accept and reject output cassettes, since Japanese manufacturers often do not perform rework on processed material. The Optistation capabilities were expanded when SMIF compatibility was announced in May 1986. The Optistation systems range in price from $50,000 to $70,000. While the Optistation is primarily a wafer defect inspection system, an optional linewidth measurement module is available at a cost of $35,000.

In addition to producing LAMPAS and Optistation wafer measurement and inspection equipment, Nikon is a major manufacturer of wafer steppers and mask metrology tools for the semiconductor industry. Nikon Precision Incorporated (San Bruno, California) was formed in 1982 as a subsidiary of Nippon Kogaku K.K. of Japan in order to support Nikon's sales, marketing, service, and technical support operations in North America. Nikon is a world leader in the production of high-quality optics for cameras, microscopes, medical, and scientific instrumentation.

Ryokosha

Ryokosha (Tokyo, Japan) manufactures a video-based linewidth measurement system for the semiconductor industry. The MF-68 system consists of a telecomparator, video camera, and computer system with autofocus and variable threshold selection. The MF-68 has been manufactured for approximately 15 years and was jointly developed by Hitachi and Ryokosha. It began as a manual measurement tool and gradually has become more automated. The MF-68K, approximately one year old, is the latest generation of the MF-68 systems, and it contains 100 programmable routines for linewidth measurement. The MF-68K is priced at approximately ¥10 million ($70,000), while the MF-68 is priced at about ¥7 million ($49,000). Essentially all of Ryokosha's sales of linewidth measurement systems have been in Japan; only a small fraction of the company's installed base is in export markets.

Sony

Sony (Atsugi-City, Kanagawa, Japan) developed the ARQUS-20 Automatic Reticle Qualification System in 1979. The ARQUS-20 utilizes a proprietary defect detection algorithm to perform a die-to-die comparison of the wafer image in order to detect the presence of defects. The defect specification on the ARQUS-20 is 0.8 micron at an 11-minute-per-square-centimeter scanning rate. Sony's ARQUS-20 is priced at approximately ¥80 million ($560,000) in Japan. The ARQUS-20 became a commercial product in 1985 and is represented by Marubeni. Dataquest believes that only two systems have been shipped to date, both to Sony's Kokubu semiconductor manufacturing plant on Kyushu.

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CD and Wafer Inspection Equipment Markets

European Companies

Bio-Rad Lasersharp Ltd.

Bio-Rad Lasersharp Ltd., (Abingdon, Oxfordshire, England) manufactures a scanning laser microscope system, the SOM 150. The imaging modes of the SOM include optical beam induced current, confocal, and differential phase contrast (DPC). An optional CD/linewidth measurement package is also available. Major applications for this system include material characterization and preproduction qualification in semiconductor processing. The system was first introduced in Europe in early 1986 and made its U.S. debut at SEMICON/East in September 1986. The system, which does not include automated wafer handling, is priced at $95,000. Dataquest believes that approximately 12 to 14 units are in the installed base worldwide. The company was formed by Bio-Rad Laboratories when it acquired the manufacturing and marketing rights to the Lasersharp scanning laser microscope from IBT Dubilier.

While the Bio-Rad Lasersharp tool does not compete directly with other commercial confocal microscope measurement systems discussed in this study, the company is mentioned because of possible future development of a system for the semiconductor production environment.

Cambridge Instruments

Cambridge Instruments (Cambridge, England) manufactures a family of products for the wafer metrology and inspection market. These include optical CD and defect inspection systems, a SEM-based system for CD measurement, and an optical system for image-to-data base comparison of reticles, masks, and wafers.

Cambridge offers three different systems for optical CD measurement: the Microcheck 1, the Polycheck, and the Polycheck VLSI. The Microcheck 1 and Polycheck systems were introduced at SEMICON/West in May 1987. The Microcheck 1, priced at $60,000, is a manual system that employs fully automatic measurement of CDs and overlay. The Microcheck 1 is well suited for R&D and pilot-line manufacturing. The Polycheck system provides CD measurement capability down to 0.5 micron, macro measurements of large dimensions, and additional defect inspection capabilities. The Polycheck is priced at $115,000. Both the Microcheck 1 and Polycheck systems were designed for use in cross-industry applications including the measurement of CDs in magnetic head manufacturing and other computer peripheral operations. Dataquest believes that all deliveries of Microcheck 1 and Polycheck systems through the end of 1987 have gone to nonsemiconductor manufacturing operations.

The Polycheck VLSI, introduced in September 1987, was designed as a fully automatic CD measurement and inspection station for the semiconductor production environment. The tool features a four-cassette robotic wafer-handling system with up to 200mm wafer capability. Wafer inspection is accomplished through the use of preprogrammed inspection sequences, and an operator performs defect detection and classification operations. Typical measurement repeatability is approximately

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0.008 micron (1 sigma), and measurement capability is down to 0.5 micron. The Polycheck VLSI is an enhanced version of the basic Polycheck system, which, in turn, was based on the Wafer MAP product of Reichert–McBain. The price of the Polycheck VLSI is on the order of $200,000. Dataquest believes that deliveries will begin in first quarter 1988.

Reichert–McBain, part of the Cambridge Instruments' organization until December 1987, is responsible for design, development, and manufacture of the Microcheck, Polycheck, and Polycheck VLSI products. In December 1987, Cambridge Instruments agreed to acquire a 40 percent equity interest in OSI in exchange for the transfer of the Reichert–McBain division to OSI. The Microcheck, Polycheck, and Polycheck VLSI products will now be incorporated into the OSI product line of CD and wafer inspection systems for the semiconductor industry.

The Scanline system from Cambridge Instruments is an automated e–beam comparator dedicated to submicron linewidth measurement. While this system is based on SEM technology, the Scanline design has been optimized for CD measurement, rather than for imaging. The system has minimum feature–size measurement down to 0.1 micron, with repeatability of 30 to 50 angstroms. Wafer throughput is at a minimum of 12 wafers per hour at five sites per wafer. Wafer–size capability ranges from 2–inches to 150mm, with an option available for 200mm wafers. The system is priced at approximately $300,000 with pattern recognition capability. The Scanline is currently under final development, and Dataquest believes that deliveries will begin in 1988.

The Chipcheck system from Cambridge is an image–to–data base comparator for reticles, masks, and wafers, and is used in process qualification operations. The system, introduced in 1984, automatically detects and classifies defects or deviations from the original CAD design and corresponding masks, reticles, or processed wafers. This image–to–data base comparative analysis is particularly useful for detecting repeating defects on multi–die reticles and can readily identify standard defects including rat bites, bridges, dirt, and pinholes. The tool primarily is used in mask and reticle inspection; however, Dataquest believes that several customers use the system for wafer inspection as well. In the wafer inspection mode, the Chipcheck system compares photoresist images on the silicon wafer directly with the original design data in the CAD data base. The minimum defect detection limit is 0.5 micron. The Chipcheck system is priced at approximately $750,000, and Dataquest estimates that there were approximately 15 systems in the installed base at the end of 1987. CD measurement capability is available as an option.

Cambridge Instruments was founded in 1881 by Horace Darwin, youngest son of the famous naturalist, Charles Darwin. In May 1986, the Cambridge Instruments organization merged with R. Jung GmbH (Heidelberg, West Germany), C. Reichert Optische Werke (Vienna, Austria), Reichert Scientific Instruments (formerly American Optical Company and Spencer Lens Company, located in Buffalo, New York), and Reichert–McBain. Today, Cambridge Instruments' semiconductor products include optical and e–beam metrology equipment, CAD data base and wafer inspection systems, scanning electron microscopes, direct–write e–beam lithography equipment, MOCVD reactors, epitaxial reactors, and single–crystal pullers. Three other major markets for the company are scientific instruments, ophthalmic and medical instruments, and components for industrial process control and automation.

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Heidelberg Instruments

Heidelberg Instruments (Heidelberg, West Germany) manufactures the Line Profile Measurement (LPM) system. The LPM is a confocal laser scanning microscope designed for fully automatic linewidth measurement and line profilometry. The system is designed with telecentric optics that allows a laser beam to be scanned over the wafer surface, which is held fixed in the x–y plane. The LPM measures linewidths down to 0.3 micron, with .005–micron repeatability. One of the advantages of confocal scanning laser microscopy is the ability to measure the vertical profile of a circuit feature. The LPM can measure lineheight down to 0.05 micron, with .005–micron repeatability. Typical wafer throughput is on the order of 20 to 25 wafers per hour at five sites per wafer.

The LPM was first introduced at SEMICON/Europa in March 1987, and the first system was shipped to Siemens in late May. Dataquest estimates that a total of five systems was shipped in 1987, with systems going to both European and U.S. semiconductor manufacturers. The price of the LPM in Europe is DM 550,000, while the price in the United States is approximately $340,000.

Heidelberg Instruments is developing an automatic defect inspection system for the wafer inspection market. The system will be designed with die–to–die and die–to–data base inspection modes. The company plans to introduce the system in fourth quarter 1988.

Heidelberg Instruments was formed in 1984 by five researchers from Heidelberg University and four industrial partners. Investors in Heidelberg Instruments include Wild Leitz, a West German manufacturer of wafer and mask metrology and inspection equipment for the semiconductor industry. Other products from Heidelberg Instruments include laser scanning microscope systems for biological, chemical, and medical applications.

Vickers Instruments

Vickers Instruments (York, England) manufactures the Quaestor CD–07A, a fully automatic, optical linewidth and overlay measurement system. This system has been designed specifically for the production environment, with major emphasis placed on fully automatic operation and reliable linewidth measurement in production operation. The CD–07A utilizes an image–shearing technique to measure linewidth geometries down to 0.7 micron. The system has a wafer throughput rate of 25 wafers per hour at five measurement sites per wafer. The CD–07A was introduced in 1986, and deliveries began in 1987. Dataquest estimates that more than 35 systems were shipped in 1987 to semiconductor manufacturers in the United States, Europe, and Japan. The price of the Quaestor CD–07A is approximately $230,000.

Vickers Instruments also manufactures e–beam–based CD measurement systems. In May 1987, Vickers introduced the Nanolab SR Series at SEMICON/West. The Nanolab SR Series is an automatic, nondestructive, submicron CD and inspection system. The

tool utilizes SEM technology and is designed to operate in the production environment. The wafer throughput rate is greater than 15 wafers per hour at five sites per wafer. The linewidth measurement range is from 0.1 micron to 10.0 microns. Inspection capability is based on visual observations made by an operator. The first shipment of the Nanolab SR was in late 1986, and Dataquest estimates that the installed base of systems was approximately 15 systems at the end of 1987. This system is priced at $500,000.

Vickers also offers a sister tool to the Nanolab SR Series. This system, the Nanolab DL3206 SEM, is based on the same SEM technology as the Nanolab SR tool. The difference in the two systems is that the Nanolab DL3206 SEM is designed for use in process development and troubleshooting, such as in the early stages of setting up a production line. In contrast, the Nanolab SR Series is designed for in-line processing in a production environment. The price of the DL3206 system is $280,000.

Vickers Instruments is an operating business unit of Vickers plc. Manufacturing of the Quaestor system occurs at the company's headquarters in York, England. The U.S. corporate office is located in Woburn, Massachusetts, while the Canadian office is located in Nepan, a suburb of Ottawa, Ontario. The Nepan office is where e-beam instrument design, development, and manufacturing takes place. Vickers Instruments is represented by Union Optical in Japan. Vickers plc, Vickers Instruments' parent company, is a multinational corporation with diverse interests that range from marine engineering, infant medical-care systems, and the Rolls-Royce automobile operations.

Wild Leitz

Wild Leitz (Wetzlar, West Germany) manufactures microscopes and measurement and inspection systems for front-end and assembly operations within the semiconductor industry. The company's CD measurement systems employed in the production environment are the MPV-CD 2 and the LTS-M systems. The MPV-CD 2 is a standalone optical CD tool priced at approximately $70,000. It was introduced in the late 1970s. The LTS-M, introduced in 1984, incorporates the MPV-CD 2 system, pattern recognition, and an IBM PC system with the automatic wafer-handling capability of the Leitz Transport System (LTS). The LTS-M is priced at approximately $175,000. Wild Leitz introduced its four-cassette wafer inspection station, the Leitz Inspection Station (LIS) in 1982. This inspection station ranges in price from $50,000 to $100,000. The company also offers a one-cassette version of the LIS wafer inspection system known as the LTS.

In addition to its CD and wafer inspection equipment, Wild Leitz manufactures the MPV-SP 2, a film thickness measurement system; the MVG Automatic, a mask comparator system used for image overlay and CD measurements; and a scanning acoustic microscope system with applications in materials research, failure analysis, and device development. Wild Leitz is also a major supplier of optical microscopes and components to OEMs.

Leitz IMS Company (Billerica, Massachusetts) was formed as a partnership between Wild Leitz of West Germany and Image Micro Systems, Inc., of the United States. The LMS-2000 Laser Metrology System provides CDs and pattern-dimensional integrity data

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with nanometer accuracy and repeatability over an 8 x 8-square-inch area. The LMS-2000 can support the output of several e-beam mask generating systems. Shipments of the LMS-2000 system began in 1987. The price of the tool is approximately $1 million.

The name of the company, Wild Leitz, reflects its two parent corporations: Wild Heerbrugg of Switzerland and Ernst Leitz Wetzlar GmbH of West Germany. In the late 1970s, the Leitz family sold a minority interest, and later a majority share, of the Leitz business to Wild. Today, Wild Leitz represents a large conglomerate of business activities centered on optical imaging systems. Major business operations include microelectronics, medical and microscopic diagnostics, and industrial metrology technology. A fourth group in Wild Leitz is involved in providing venture funding for new companies including Heidelberg Instruments, a manufacturer of confocal scanning laser microscopy systems for the semiconductor industry.

Zeiss

Zeiss (Oberkochen, West Germany) manufactures the Wafer Inspection Station (WIS). The WIS was introduced in March 1985 at SEMICON/Europa as a basic manual inspection station. Enhancements to the WIS system include a motorized stage, new microscope design, automatic wafer handling and vacuum transport, and computer-controlled operation. In addition, a film thickness measurement option for the WIS was introduced at SEMICON/East in September 1987. The price of the WIS is approximately $110,000 but will vary, depending upon options. Manufacture of the WIS system occurs at Zeiss facilities in Gottingen and Oberkochen, West Germany. Shipments of the WIS system, to date, have been to European and Canadian semiconductor manufacturing companies.

Departures

Contrex

Contrex spent six years in the development of a submicron automated measurement and wafer inspection system, the Wafervision 3000. This system, priced at approximately $600,000 to $800,000, was expected to compete with the KLA 2020. Contrex ceased operations in 1986, after being unable to secure additional funding.

Machine Intelligence

Machine Intelligence undertook preliminary development of an automated CD and wafer inspection station. The company closed its facilities in 1987, after being unable to obtain sufficient venture funding for further product design and development. Technology developed by Machine Intelligence for bank note inspection was sold to a European currency-printing equipment manufacturer when the corporation was dissolved.

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Optoscan

Optoscan, founded in 1983, spent four years in the development of a laser-based linewidth and overlay measurement system, the model 2010. This system, priced at approximately $240,000, utilized a 325nm laser source and was expected to achieve 0.5-micron measurement capability. General Signal acquired Optoscan in 1985 and closed the subsidiary in 1987, after an unsuccessful effort to market the 2010 system.

Karl Suss

While Karl Suss (Munich, West Germany) has not officially announced its departure from the wafer inspection equipment market, the company is no longer actively marketing its IP-125 wafer inspection station. The IP-125 wafer inspection system was sold between 1982 and 1984 in Europe and was priced at approximately $40,000.

MARKET ANALYSIS

The following sections of our study present historical market information and analysis for optical CD equipment, wafer inspection stations, and joint CD/inspection systems from 1982 through 1987. This information includes worldwide market estimates by company, unit demand, and ASP trends as well as a discussion of the market leaders by region for each of the three market segments. Models of equipment in each segment are identified by vendor and ASP. (ASPs reflect 1987 prices across all regions of the world, unless otherwise noted. The yen/dollar exchange rate in 1987 was 144.) In addition to these three equipment segments, the e-beam-based CD equipment and reticle qualification systems are discussed briefly with regard to their competitive impact. The forecast of optical CD equipment, wafer inspection stations, and joint CD/inspection systems is contained in the final section of this study.

Optical CD Equipment Market

World Market

In 1987, the worldwide market for optical CD equipment was $39.5 million, up 38 percent from the 1986 level of $28.7 million. Table 3 presents historical worldwide sales for companies participating in this market segment from 1982 through 1987.

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CD and Wafer Inspection Equipment Markets

Table 3

Worldwide Optical CD Equipment Market, 1982–1987
(Millions of Dollars)

Company	1982	1983	1984	1985	1986	1987	1987 % Share
Heidelberg Instruments	0	0	0	0	0	$ 1.6	4.0%
Hitachi	0	0	0	0	$ 4.1	6.0	15.2
IVS, Inc.	0	0	0	0	0.5	1.5	3.8
Nanometrics	$ 4.0	$ 7.0	$ 6.7	$ 2.3	1.5	1.7	4.3
Nikon	1.9	2.4	4.7	3.0	2.3	5.2	13.2
Optical Specialties, Inc.	0	1.9	4.7	3.1	2.2	1.3	3.3
Reichert-McBain	0	0	0	0	3.0	0.3	0.8
Ryokosha	1.1	1.6	2.2	1.4	1.5	1.4	3.5
SiSCAN Systems	0	0	0	0	1.9	3.0	7.6
Vickers Instruments	0	0	0	0	0	8.3	21.0
Wild Leitz	1.6	2.8	4.4	4.4	4.8	3.6	9.1
Others	4.8	6.8	9.9	5.9	6.9	5.6	14.2
Total	$13.4	$22.5	$32.6	$20.1	$28.7	$39.5	100.0%
Growth		68%	45%	(38%)	43%	38%	

Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
March 1988

Vickers Instruments of the United Kingdom ranked first in market share of the optical CD equipment market, with the successful introduction of its new automatic CD measurement system, the Quaestor CD–07A. Hitachi, with its LAMU measurement system, and Nikon, with its LAMPAS tools, ranked second and third, respectively, in the world market. Together, these three companies had a combined share of 49.4 percent. In addition, the new confocal scanning laser microscopy systems of Heidelberg Instruments and SiSCAN Systems captured a combined share of 11.6 percent of the 1987 market. All five companies have introduced new systems within the last two years, and Dataquest believes that their success in the marketplace reflects new technology implementations and advanced automation capability. The prices of the CD measurement systems of these five companies range from $230,000 to $420,000, substantially higher than $115,000, the ASP across all equipment models in this market segment in 1987.

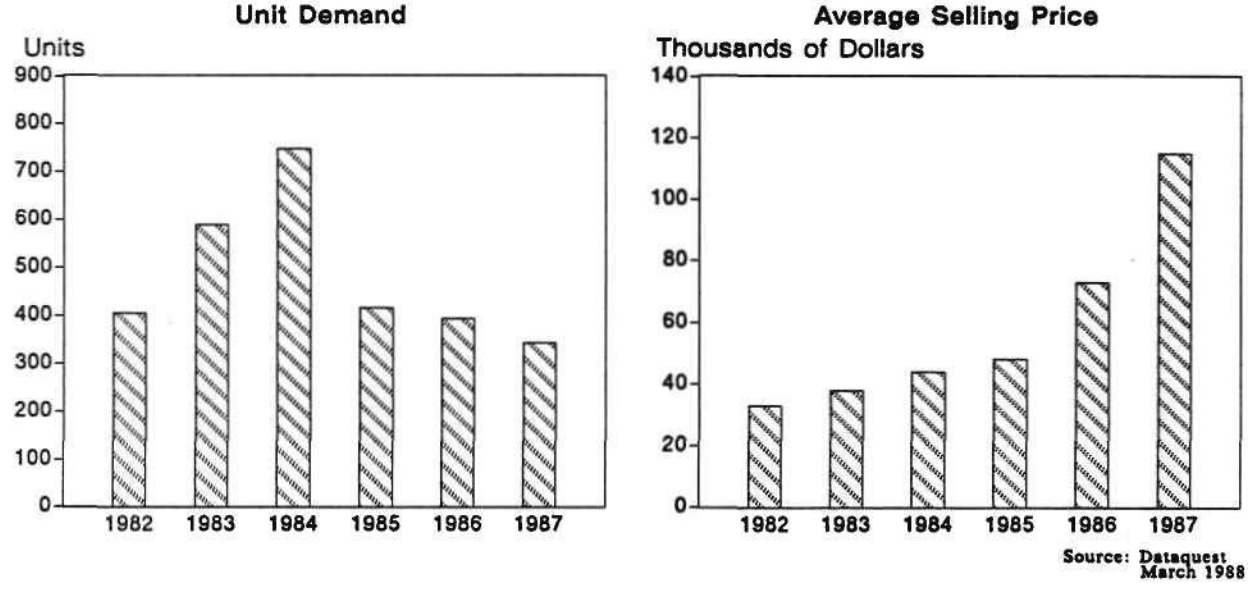
CD and Wafer Inspection Equipment Markets

In 1982, the market leaders in the CD equipment market consisted of Nanometrics, Nikon, and Wild Leitz. Dataquest estimates that these companies had a combined share of 56.0 percent of the $13.4 million market. In 1984, the boom year for the semiconductor equipment industry, market leaders in the CD equipment market were Nanometrics, Nikon, OSI, and Wild Leitz. These companies had combined sales of $20.5 million, or 62.9 percent of the 1984 market. Interestingly enough, Nikon has managed to maintain its market share of approximately 13 percent from 1982 through 1987. In addition, it was the only company among the 1982 and 1984 market leaders that was still ranked among the top three in 1987.

With the advent of new technologies and increased equipment automation, the ASP of optical CD equipment has risen considerably over the last five years. Figure 2 presents a summary of the worldwide unit demand and ASP of optical CD equipment from 1982 through 1987. As illustrated in Figure 2, the ASP of optical CD equipment has increased by a factor of 3.5 between 1982 and 1987, from approximately $33,000 to almost $115,000. At the same time, unit demand for CD measurement systems has declined every year for the last three years, and, in 1987, it stood at only 85 percent of its 1982 level.

Figure 2

Optical CD Equipment
Worldwide Unit Demand and ASP, 1982–1987



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CD and Wafer Inspection Equipment Markets

Regional Markets

Table 4 presents the historical optical CD equipment market by regional consumption. In 1987, the United States and Japan had approximately equal share of the world optical CD equipment market, with 37.7 percent and 37.5 percent, respectively. European sales of optical CD equipment were 17.2 percent of the world market in 1987, while the ROW represented 7.6 percent.

Table 4

Optical CD Equipment
Regional Markets, 1982–1987
(Millions of Dollars)

Region	1982	1983	1984	1985	1986	1987	CAGR 1982-1987
United States	$ 6.2	$11.0	$16.6	$ 7.8	$11.3	$14.9	19.2%
Japan	4.8	7.3	10.4	6.7	10.5	14.8	25.3%
Europe	1.9	3.0	3.7	3.4	4.1	6.8	29.1%
ROW	0.6	1.2	1.8	2.2	2.7	3.0	38.0%
Total	$13.4	$22.5	$32.6	$20.1	$28.7	$39.5	24.1%
Growth		68%	45%	(38%)	43%	38%	

Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
March 1988

Many of the market leaders that emerged in 1987 are relatively new participants in the optical CD equipment market. Growth in the regional markets during 1987 is directly attributable to those new companies offering advanced technology products with improved automation capability.

In the United States, the top three participants in the optical CD equipment market in 1987 were Vickers Instruments, SiSCAN Systems, and IVS, Inc. Together, these three companies represented 57.7 percent, or $8.6 million, of the 1987 optical CD equipment market in the United States. Both SiSCAN Systems and IVS, Inc., sold their first systems in 1986, while Vickers started shipments in 1987. Wild Leitz, Nanometrics, and OSI were next in the ranking in this market segment in 1987 and had a combined share of approximately 23.5 percent. In 1984, Nanometrics and OSI were the major suppliers of optical CD measurement equipment to the U.S. semiconductor industry and had a combined share of 49.4 percent of the $16.6 million market. On a unit basis, Nanometrics and OSI have dominated the U.S. market over the past six years.

In Japan, Hitachi and Nikon ranked first and second, respectively, in a market of $14.8 million in 1987. These two manufacturers had a combined market share of 71.0 percent. Ryokosha is the next largest supplier of optical CD equipment to the Japanese semiconductor industry, with 9.5 percent share of the 1987 market.

In Europe, the top three participants in 1987 were Vickers Instruments, Wild Leitz, and Heidelberg Instruments, with a combined share of 75.0 percent of the $6.8 million market. While Vickers Instruments and Heidelberg Instruments experienced their first sales in this market segment during 1987, Wild Leitz has been a major supplier of optical linewidth measurement and inspection systems since the early 1980s.

In 1987, no clear leader emerged in the $3.0 million optical CD equipment market in the ROW region.

Equipment Models and Average Selling Prices

Table 5 presents a summary of optical CD measurement equipment by manufacturer, model name, and ASP.

Table 5

Optical CD Equipment
Equipment Models and ASPs

Company	Model	ASP
Bio-Rad Lasersharp Ltd.	SOM 150	$ 95,000
Cambridge Instruments	Microcheck 1	$ 60,000
Dainippon Screen	SLM 601	N/A
Heidelberg Instruments	LPM	$340,000
Hitachi	LAMU-600	$300,000
ITP, Inc.	AUTO CD 88	$ 75,000
	System 802	$130,000
IVS, Inc.	Accuvision-1 (ACV-1)	$ 80,000
	ACV-2	$140,000
	ACV-3	$220,000
	ACV-4	$300,000
KLA Instruments	KLA 2005	$700,000
	KLA 5000	$380,000
Nanometrics	Model 50	$ 45,000
	Model 51	$ 45,000
	Model 400	$150,000
Nidek	CD-10	$ 35,000
Nikon	LAMPAS-M3	$165,000
	LAMPAS-HD	$420,000*
Optical Specialties, Inc.	VLS-I	$ 47,000

(Continued)

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Table 5 (Continued)

Optical CD Equipment
Equipment Models and ASPs

Company	Model	ASP
Reichert-McBain	Wafer MAP	$165,000
Ryokosha	MF-68	$ 49,000
	MF-68K	$ 70,000
SiSCAN Systems	SiSCAN-I	$240,000
	SiSCAN-II M	$270,000
	SiSCAN-II A	$350,000
Vickers Instruments	Quaestor CD-07A	$230,000
Waterloo Scientific	WSI-1000CD	$300,000
Wild Leitz	MPV-CD 2	$ 70,000
	LTS-M	$175,000

N/A = Not Available
*Reflects price in Japan; at time of publication, price had not yet been fixed in the United States.

Source: Dataquest
March 1988

SEM-Based CD Systems

SEM-based CD systems provide better measurement resolution and depth of focus, compared with their optical counterparts. These systems, with measurement capability down to 0.1 micron, are already being used for linewidth and overlay measurement in R&D and pilot line operations. Many of the SEM manufacturers have perceived this as a growing market opportunity and are currently redesigning and retrofitting their existing SEM tools for operation in the production environment. So far, this has encompassed the addition of CD measurement software packages from optical-based systems, automatic wafer handling, and load locks to increase wafer throughput. The systems being designed specifically for IC metrology are low-voltage SEMs because of the concern about damage to the wafer at higher levels of electron irradiation. Compared with optical tools, the SEM CD tools still have relatively low throughput, on the order of 8 to 15 wafers per hour at five measurement sites per wafer. The slow throughput rate and the general lack of user-friendly controls are two factors that have impeded the acceptance of many SEM systems in the production environment.

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CD and Wafer Inspection Equipment Markets

Table 6 identifies several companies currently providing SEM-based CD measurement systems. The table includes equipment model names and ASPs. Hitachi, with its S-6000 system, has established a leadership position in Japan, where semiconductor manufacturers have embraced SEM CD systems for submicron measurement.

Table 6

SEM-Based CD Systems
Equipment Models and ASPs

Company	Model	ASP
ABT (Akashi Beam Technology)	CC-CD	$375,000
Amray	Model 1500	$350,000
Cambridge Instruments	Scanline	$300,000
Hitachi	S-6000	$625,000
JEOL	JEPAS-1200	$450,000
KLA Instruments*	KLA/Holon 2711	$500,000
Nanometrics	Model 100	$420,000
Opal Inc.	Opal 702	N/A
Vickers Instruments	Nanolab SR Series	$500,000
	DL3206 SEM	$280,000

N/A = Not Available

*Holon's equivalent system, model ESPA-11, is priced at ¥90 million in Japan.

Source: Dataquest
March 1988

CD Measurement Equipment—An Evaluation of Four Factors

With a plethora of competing technologies to choose from, semiconductor manufacturers are faced with evaluating and differentiating CD measurement systems on the basis of the following four important factors:

- Measurement capability
- Wafer throughput
- Cost of the equipment
- Level of equipment automation

Measurement Capability

Measurement capability is an essential issue, as manufacturers advance into the processing and measurement range of 1.25– to 0.75–micron geometries. This is the range at which traditional white–light CD measurement systems begin to "run out of steam." New technologies and techniques, such as confocal scanning laser microscopy, fluorescence measurement capability, enhanced video imaging processing, and coherence probe imaging tools, are being designed to compete with the traditional white–light measurement systems for measuring line geometries in the submicron range. SEM–based CD measurement systems provide an additional alternative to the variety of optical techniques that are available or are being developed today.

Wafer Throughput

In the production environment, equipment throughput must meet or exceed a rate that will accommodate the flow of material through the processing line. Optical CD measurement equipment typically has a throughput on the order of 25 to 30 wafers per hour at five linewidth measurements per wafer. In comparison, wafer throughput for e–beam–based systems is on the order of 8 to 15 wafers per hour at five sites per wafer. This is slower than the optical systems because, during the SEM CD measurement process, the wafer must be in a vacuum environment. Manufacturers have added load locks to improve throughput on the SEM CD tools. A significant exception for CD equipment throughput is KLA Instruments' 2020 system. This system has a throughput of approximately 90 wafers per hour at five linewidth measurement sites per wafer.

Cost of the Equipment

In 1987, optical CD measurement systems ranged in price from $50,000 for a traditional white–light microscopy tool to almost $900,000 for a joint CD/inspection system like the KLA 2020. SEM CD systems ranged in price from $300,000 to $600,000. This enormous breadth in the range of prices, coupled with varying measurement capability and throughput, has further complicated the purchasing issues and priorities for semiconductor manufacturers.

Equipment Automation

The fourth major factor in the evaluation of CD measurement systems is the level of equipment automation. All systems today provide some form of automated wafer handling in addition to automatic measurement algorithms. Some types of equipment, however, still require some additional amount of operator assistance and interaction beyond normal setup procedures. This reliance on an operator is considered unacceptable by many semiconductor manufacturers who want fully automated equipment performance. Dataquest believes that Vickers Instruments, in particular, was able to capture 21.0 percent of the world optical CD equipment market in 1987 because its Quaestor CD–07A system provides reliable automated performance in the production environment.

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CD and Wafer Inspection Equipment Markets

In addition to the automation of physical operations, semiconductor manufacturers also are very interested in measurement systems that can analyze the collected data for the optimization of equipment setup parameters. In particular, several systems have been developed for optimizing the performance of lithography equipment. KLA Instruments offers a software enhancement for the 2020 system, known as the KLA Stepper Set-Up, or KLASS. The KLASS software is an applications package for optimizing stepper setup parameters, including focus and exposure settings. In May 1987, OSI announced an applications software package known as the Metrology Analysis Program I (MAP-I). This software package receives measurement data from OSI's MV-PLUS and uses it to optimize stepper/aligner operating parameters. Perkin Elmer introduced the OMS 1 Overlay Measurement System at SEMICON/West in May 1987. This system provides fast, precise overlay measurements that are used to optimize the performance of the company's Micralign and Micrastep lithography tools. Dataquest expects analysis packages to be developed eventually in order to provide measurement, analysis, and feedback to equipment in a single closed-loop operation.

Wafer Inspection Equipment Market

World Market

In 1987, the worldwide market for wafer inspection stations was $24.5 million, up 13 percent from the 1986 level of $21.8 million. Table 7 presents historical worldwide sales for companies participating in this market segment from 1982 through 1987.

Table 7

Worldwide Wafer Inspection Stations Market, 1982-1987
(Millions of Dollars)

Company	1982	1983	1984	1985	1986	1987	1987 % Share
Canon	$ 0.8	$ 1.3	$ 2.0	$ 1.3	$ 1.4	$ 2.0	8.2%
Estek (Aeronca)	0	0	0	0.3	0.2	0.1	0.4
Insystems	0	0	0	0	0	2.1	8.7
Nidek	1.3	1.7	2.0	1.7	2.2	3.1	12.6
Nikon	1.3	3.2	5.8	4.4	6.4	8.1	33.0
Optical Specialties, Inc.	5.3	4.2	7.8	4.2	2.8	1.7	6.9
Karl Suss	0.1	0.2	0.2	0	0	0	0
Wild Leitz	0.6	2.3	4.3	4.7	3.5	2.8	11.4
Zeiss	0	0	0	0.9	2.4	1.8	7.3
Others	2.0	3.8	5.0	3.0	2.9	2.8	11.4
Total	$11.4	$16.7	$27.1	$20.5	$21.8	$24.5	100.0%
Growth		47%	62%	(25%)	7%	13%	

Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
March 1988

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CD and Wafer Inspection Equipment Markets

Nikon, with its Optistation systems, had the largest share of the 1987 worldwide wafer inspection market with 33.0 percent of the $24.5 million market. Nidek, Wild Leitz, and Canon together had an additional 32.2 percent. All four companies manufacture microscope-based inspection stations that rely on operators to detect and classify defects on the wafer surface. Insystems, with its new system based on holographic, spatial frequency filtering technology, captured 8.7 percent of the world market with sales of $2.1 million in 1987. This system provides fully automatic detection of an entire wafer in less than 30 minutes. While the traditional microscope inspection stations are priced at approximately $60,000 to $70,000, the automatic wafer inspection system from Insystems is $1 million.

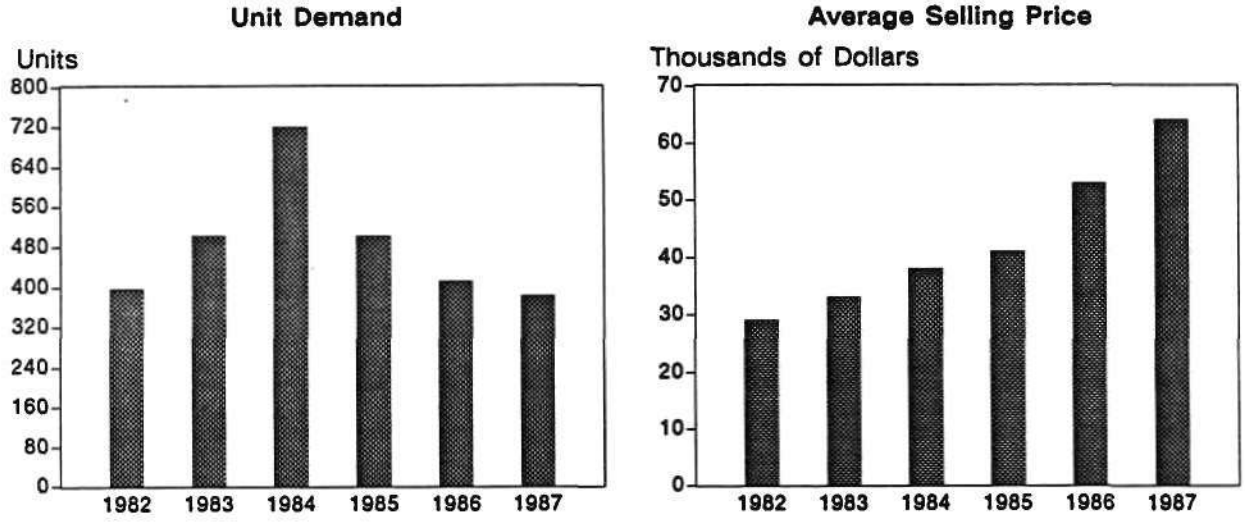
In contrast with 1987, the 1982 market was dominated by OSI, which had 46.5 percent share of the $11.4 million market. In 1984, the market leaders in wafer inspection equipment were OSI, Nikon, and Wild Leitz. These companies had combined sales of $17.9 million, or 66.1 percent, of the 1984 market. As in the optical CD equipment market, Nikon has maintained its presence as a market leader from 1982 through 1987.

Figure 3 presents a summary of the worldwide unit demand and ASP of wafer inspection stations. As with optical CD measurement equipment, worldwide unit demand for wafer inspection stations declined in 1985, 1986, and 1987. At the same time, the price of the equipment has been increasing from an average of $29,000 in 1982 to $64,000 in 1987. The increase in the ASP of wafer inspection stations has been more gradual than the ASP of optical CD equipment over the same time frame. This is because the technology of defect detection has remained virtually unchanged over this time period. An operator is still responsible for visually scanning a magnified image of the wafer surface to detect the presence of defects. As wafer inspection stations have matured, system enhancements have been directed toward automatic wafer handling, automatic and programmable stage movement, autoalignment, autofocus, and keypad data entry systems. Recently, a new generation of wafer inspection stations was introduced. These systems perform automatic defect detection and, in some instances, assist in defect classification as well. The technological advances of Insystems' holographic, spatial frequency filtering system and KLA's new 2028 automatic inspection station are reflected in price tags in the neighborhood of $1 million.

CD and Wafer Inspection Equipment Markets

Figure 3

Wafer Inspection Stations
Worldwide Unit Demand and ASP, 1982–1987



Source: Dataquest March 1988

Regional Markets

Table 8 presents the historical wafer inspection equipment market by regional consumption. In 1987, Japan had the major share, with 42.7 percent of the $24.5 million world market. The United States ranked second, with 31.0 percent, while Europe represented 14.7 percent, and ROW had approximately 11.6 percent. Japan's major share of the wafer inspection market in 1986 and 1987, for the most part, is due to yen appreciation during those years. However, Dataquest believes that, since 1985, Japan also has purchased more wafer inspection stations on a unit basis than has the United States. This correlates with the general trend that Japan has purchased more wafer steppers on a cumulative basis than has the United States over the last three years.

In the United States, the top three participants in the wafer inspection market in 1987 were Nikon, OSI, and Wild Leitz. Together, they represented 61.8 percent of the $7.6 million market in 1987. These three companies have been the major suppliers of wafer inspection stations to the United States since 1983. In 1982, OSI dominated the U.S. market with more than 80 percent of the $6.1 million market.

In Japan, Nikon, Nidek, and Canon are the major suppliers of wafer inspection equipment. In 1987, they had a combined share of almost 82.9 percent of the $10.5 million market. These three companies have consistently represented in excess of 80 percent of the Japanese wafer inspection market since 1982.

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Table 8

Wafer Inspection Stations
Regional Markets, 1982–1987
(Millions of Dollars)

Region	1982	1983	1984	1985	1986	1987	CAGR 1982-1987
United States	$ 6.1	$ 8.5	$14.2	$ 7.8	$ 7.5	$ 7.6	4.5%
Japan	4.0	6.0	9.1	7.2	8.6	10.5	21.3%
Europe	1.1	2.0	3.2	4.0	3.8	3.6	26.8%
ROW	0.2	0.3	0.6	1.5	1.9	2.9	70.7%
Total	$11.4	$16.7	$27.1	$20.5	$21.8	$24.5	16.5%
Growth		47%	62%	(25%)	7%	13%	

Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
March 1988

In Europe, the top three participants were Wild Leitz, Zeiss, and Nikon, with a combined share of 88.9 percent of the $3.6 million market in 1987. For Nikon, 1987 was the first year of sales in Europe, while Zeiss began to sell wafer inspection stations in Europe in 1985. Historically, Wild Leitz has been the market leader in wafer inspection in Europe since 1983.

In ROW, Nidek and Nikon were the major suppliers of wafer inspection stations, with a combined share of 55.2 percent of the $2.9 million market in 1987.

Equipment Models and Average Selling Prices

Table 9 presents a summary of wafer inspection stations by manufacturer, model name, and ASP.

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Table 9

Wafer Inspection Stations
Equipment Models and ASPs

Company	Model	ASP
Estek (Aeronca)	AE-1000	$ 80,000
Canon	VIR-600	$ 55,000
	VIR-630	$ 76,000
Heidelberg Instruments	Under development	N/A
Insystems	Model 8600	$1,065,000
IVS Inc.	Under development	N/A
KLA Instruments	KLA 2028	$ 895,000
Nidek	IM-8A/-8B	$ 55,000
Nikon	Optistation 1	$ 50,000
	Optistation 1A	$ 55,000
	Optistation 2	$ 60,000
	Optistation 2A	$ 70,000
Optical Specialties, Inc.	MV-7	$ 25,000
	MV-10	$ 35,000
	MV-15	$ 50,000
	MV-360	$ 65,000
Wild Leitz	LTS	$ 60,000
	LIS	$ 75,000
Zeiss	WIS	$ 120,000

Source: Dataquest
March 1988

Reticle Qualification Systems

Reticle qualification systems represent a category of equipment that is used during the setup and process qualification stages of wafer fabrication. These systems do not compete directly with wafer inspection stations that are used to monitor wafers for the presence of defects in a production environment. There is, however, some overlap in product applications, because some equipment, such as KLA Instruments' family of 2020 systems, is used in both wafer inspection and reticle qualification applications. (Note that the majority of KLA's sales of reticle qualification systems are the KLA 200 Series products, manufactured by the company's RAPID division.) Table 10 identifies several manufacturers of reticle qualification systems by equipment model names and ASPs.

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Table 10

Reticle Qualification Systems
Equipment Models and ASPs

Company	Model	ASP
Cambridge Instruments	Chipcheck	$ 750,000
Lasertec	3WD36	$ 540,000
KLA Instruments	KLA 2020	$ 895,000
	KLA 2028	$ 895,000
	KLA 2030	$1,095,000
	KLA 200 Series	$ 670,000-
		$ 950,000
Sony	ARQUS-20	$ 560,000

Source: Dataquest
March 1988

Joint CD/Inspection Systems

World Market

In 1987, KLA Instruments had 92.3 percent share of the world market of $29.9 million for joint CD/inspection equipment. This category of equipment has been dominated strongly by KLA Instruments since it started to ship its 2020 system in 1985. OSI was the first equipment company to combine linewidth and overlay measurement capability with wafer inspection when it introduced its MV-207 and MV-215 systems in 1983. These tools combined the company's popular MV-7 and MV-15 microscope-based inspection stations with the CD measurement capability of its VLS-I system. While the MV-207 and MV-215 perform linewidth and overlay measurement in an automatic mode, an operator is still required to perform defect detection and classification. In 1984, KLA Instruments introduced the 2020 system, a tool that combines automatic CD measurement with automatic inspection capability. For the first time, the subjective judgement of the operator was removed from the wafer inspection process. OSI is developing a fully automated measurement and inspection system that will also free the operator from visual defect inspection. The company plans to market the system in 1988, and Dataquest expects other introductions in the joint CD/inspection equipment category to occur this year. Table 11 presents historical worldwide sales for the two companies that participated in this market segment from 1982 through 1987.

Figure 4 presents a summary of the worldwide unit demand and ASP of joint CD/inspection systems from 1982 through 1987. Over the last several years, the ASP of joint CD/inspection systems has skyrocketed, while unit demand has remained relatively constant. The increasing ASP of joint CD/inspection systems reflects the acceptance of KLA's 2020 system in the marketplace. The 2020 is priced at $895,000, which is substantially higher than the $77,000 ASP of joint CD/inspection systems in 1983.

CD and Wafer Inspection Equipment Markets

Table 11

Worldwide Joint CD/Inspection Systems Market, 1982–1987
(Millions of Dollars)

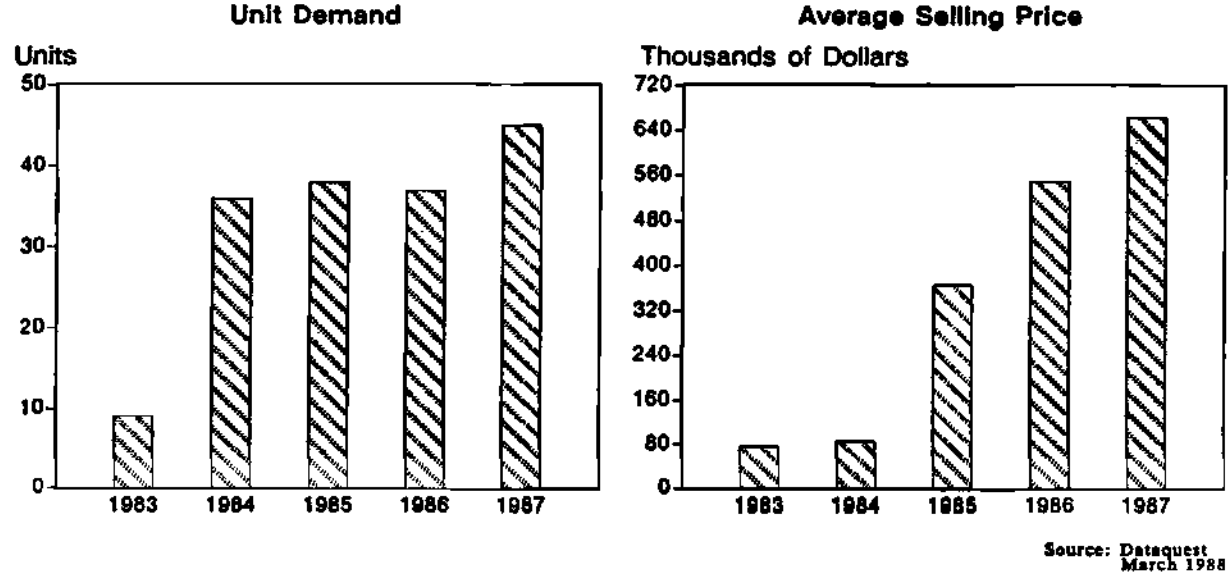
Company	1982	1983	1984	1985	1986	1987	1987 % Share
KLA Instruments	0	0	0	$11.2	$18.1	$27.6	92.3%
Optical Specialties, Inc.	0	$0.7	$3.1	2.7	2.2	2.3	7.7
Total	0	$0.7	$3.1	$13.9	$20.3	$29.9	100.0%
Growth			343%	348%	32%	30%	

Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
March 1988

Figure 4

Joint CD/Inspection Systems
Worldwide Unit Demand and ASP, 1983–1987



Source: Dataquest
March 1988

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CD and Wafer Inspection Equipment Markets

Regional Markets

Table 12 presents the historical joint CD/inspection systems market by regional consumption. In 1987, the United States represented 45.8 percent of the $29.9 million market. Japan ranked second with 38.5 percent, while Europe ranked third with 12.4 percent. Semiconductor manufacturers in the ROW countries have not as yet purchased significant amounts of equipment in this category. On a dollar basis, KLA Instruments dominates the market in the United States, Japan, and Europe. On a unit basis, however, OSI has shipped almost twice as many systems as KLA Instruments from 1983 through 1987.

Table 12

Joint CD/Inspection Systems
Regional Markets, 1982–1987
(Millions of Dollars)

Region	1982	1983	1984	1985	1986	1987	CAGR 1983-1987
United States	0	$0.6	$2.7	$ 8.3	$10.5	$13.7	119%
Japan	0	0	0.1	3.8	7.2	11.5	N/A
Europe	0	0.1	0.3	1.6	2.6	3.7	147%
ROW	0	0	0	0.2	0	1.0	N/A
Total	0	$0.7	$3.1	$13.9	$20.3	$29.9	156%
Growth			343%	348%	32%	30%	

Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
March 1988

Equipment Models and Average Selling Prices

Table 13 presents a summary of joint CD/inspection systems by manufacturer, model name, and ASP. All products identified in Table 13 are optical-based systems, except for Opal's new SEM-based metrology tool, the 702. The company plans to incorporate wafer inspection capability on this system in the future.

Table 13

Joint CD/Inspection Systems
Equipment Models and ASPs

Company	Model	ASP
Cambridge Instruments*	Polycheck	$ 115,000
	Polycheck VLSI	$ 200,000
KLA Instruments	KLA 2020	$ 895,000
	KLA 2030	$1,095,000
Opal Inc.	Opal 702	N/A
Optical Specialties, Inc.	MV-207	$ 65,000
	MV-215	$ 100,000
	MV-PLUS	$ 180,000
	MV-360CD	$ 120,000
	Micropatterning Process Control System	$ 500,000

N/A = Not Available
*Polycheck and Polycheck VLSI products transferred to Optical Specialties, Inc., as part of December 1987 acquisition of Reichert-McBain.

Source: Dataquest
March 1988

Optical CD, Wafer Inspection, and Joint CD/Inspection Equipment Market

World Market

The three categories of optical CD equipment, wafer inspection stations, and joint CD/inspection systems are closely related, because they represent process control equipment used directly in the production environment. In the case of the joint CD/inspection systems, applications and functionality overlap with those of equipment in the other two categories. Therefore, companies participating in one market segment are well placed to develop systems in one or both of the other categories. For example, Heidelberg Instruments and IVS Inc., both optical CD equipment manufacturers, are developing wafer inspection stations, while KLA Instruments, a major manufacturer of joint CD/inspection equipment, now offers systems that perform only automatic wafer inspection (the KLA 2028) or automatic linewidth and overlay measurements (the KLA 2005 and the new KLA 5000 system). Some manufacturers, such as Nikon and Wild Leitz, are already major participants in two segments, or, in the case of OSI, the

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company offers equipment in all three categories. Finally, several companies, such as KLA Instruments, Nanometrics, Hitachi, and Vickers Instruments, offer e-beam-based as well as optical CD measurement equipment in order to provide linewidth measurement capability that encompasses the entire range of submicron processing.

Table 14 presents historical worldwide sales for companies participating in the optical CD, wafer inspection, and joint CD/inspection equipment markets from 1982 through 1987. Dataquest believes that Table 14 provides an interesting perspective of company and product developments and indicates those companies that are well positioned for future market growth.

Table 14

Worldwide Market Share
Optical CD Equipment, Wafer Inspection Stations, and Joint CD/Inspection Systems, 1982-1987
(Millions of Dollars)

Company	1982	1983	1984	1985	1986	1987	1987 % Share
Canon	$ 0.8	$ 1.3	$ 2.0	$ 1.3	$ 1.4	$ 2.0	2.1%
Estek (Aeronca)	0	0	0	0.3	0.2	0.1	0.1
Heidelberg Instruments	0	0	0	0	0	1.6	1.7
Hitachi	0	0	0	0	4.1	6.0	6.4
Insystems	0	0	0	0	0	2.1	2.3
IVS, Inc.	0	0	0	0	0.5	1.5	1.6
KLA Instruments	0	0	0	11.2	18.1	27.6	29.4
Nanometrics	4.0	7.0	6.7	2.3	1.5	1.7	1.8
Nidek	1.3	1.7	2.0	1.7	2.2	3.1	3.3
Nikon	3.2	5.6	10.5	7.4	8.7	13.3	14.2
Optical Specialties, Inc.	5.3	6.8	15.6	10.0	7.2	5.3	5.6
Reichert-McBain	0	0	0	0	3.0	0.3	0.3
Ryokosha	1.1	1.6	2.2	1.4	1.5	1.4	1.5
SiSCAN Systems	0	0	0	0	1.9	3.0	3.2
Karl Suss	0.1	0.2	0.2	0	0	0	0
Vickers Instruments	0	0	0	0	0	8.3	8.8
Wild Leitz	2.2	5.1	8.7	9.1	8.3	6.4	6.8
Zeiss	0	0	0	0.9	2.4	1.8	1.9
Others	6.9	10.7	14.9	8.8	9.7	8.4	9.0
Total	$24.9	$40.0	$62.8	$54.4	$70.7	$94.0	100.0%
Growth		61%	57%	(13%)	30%	33%	

Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
March 1988

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CD and Wafer Inspection Equipment Markets

In 1987, the three leaders in the combined market of optical CD, wafer inspection, and joint CD/inspection systems were KLA Instruments, Nikon, and Vickers Instruments. They had a combined market share of 52.4 percent of the $94.0 million market. These three players, each headquartered in a different region of the world, have strength and breadth in a variety of areas. KLA Instruments, of the United States, is very strong in the joint CD/inspection systems market and recently introduced systems for automatic wafer inspection as well as automatic optical and e-beam CD measurement. In addition, KLA is the world's largest supplier of mask inspection systems to the semiconductor industry. Nikon, of Japan, has had a strong and consistent presence in the optical CD and wafer inspection equipment markets since the early 1980s and is also a major manufacturer of wafer steppers. Vickers Instruments, of the United Kingdom, ranked first in market share in the world optical CD equipment category in 1987. In addition to offering optical CD, Vickers offers a SEM-based CD measurement system for the semiconductor production environment.

While KLA Instruments, Nikon, and Vickers performed well in 1987, an additional 15 equipment companies competed for approximately 38.6 percent of the $94.0 million market. As new technologies and products are developed and new companies enter the marketplace, the optical CD, wafer inspection, and joint CD/inspection equipment markets will continue to be highly competitive segments within the semiconductor equipment industry.

Regional Markets

Table 15 presents the historical market for optical CD, wafer inspection, and joint CD/inspection systems by regional consumption. In 1987, Japan and the United States accounted for almost equal share of the $94.0 million market, with 39.3 percent and 38.5 percent, respectively. Europe ranked third with 14.9 percent, while the ROW represented 7.3 percent of the world market.

Table 15

Regional Markets
Optical CD Equipment, Wafer Inspection Stations, and Joint CD/Inspection Systems, 1982-1987
(Millions of Dollars)

Region	1982	1983	1984	1985	1986	1987	CAGR 1983-1987
United States	$12.3	$20.1	$33.5	$23.9	$29.3	$36.2	24.1%
Japan	8.8	13.4	19.8	17.5	26.2	36.9	33.2%
Europe	3.0	5.0	7.0	9.1	10.6	14.0	36.1%
ROW	0.8	1.5	2.4	3.9	4.6	6.9	53.9%
Total	$24.9	$40.0	$62.8	$54.4	$70.7	$94.0	30.5%
Growth		61%	57%	(13%)	30%	33%	

Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
March 1988

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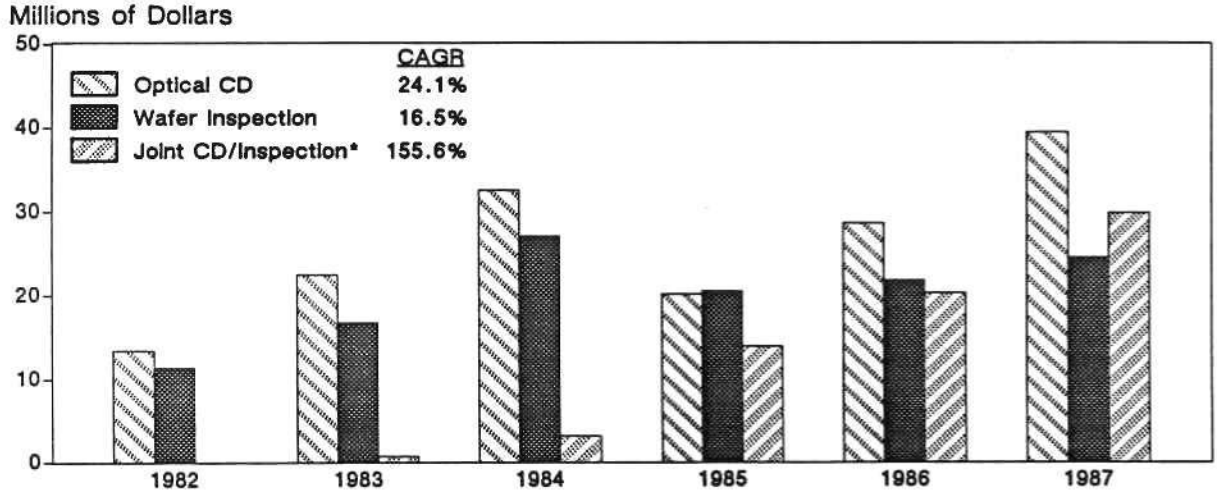
CD and Wafer Inspection Equipment Markets

Figure 5 presents a summary of the worldwide markets for optical CD equipment, wafer inspection stations, and joint CD/inspection systems for 1982 through 1987 (see Table 1 for tabulated data). As illustrated in Figure 5, the compound annual growth rate (CAGR) for the optical CD equipment and wafer inspection markets were 24.1 percent and 16.5 percent, respectively. The newly emerging market segment of joint CD/inspection equipment enjoyed a healthy 155.6 percent CAGR between 1983 and 1987. Overall, the combined market segments grew from $24.9 million in 1982 to $94.0 million in 1987 at a CAGR of 30.5 percent.

Figure 5

Worldwide Optical CD Equipment, Wafer Inspection Stations, and Joint CD/Inspection Systems Market, 1982–1987 (Millions of Dollars)



*CAGR for Joint CD/Inspection systems is from 1983 through 1987.

Source: Dataquest March 1988

FORECAST

Table 16 presents Dataquest's forecast for the markets of optical CD equipment, wafer inspection stations, and joint CD/inspection systems from 1988 through 1992. Sales of optical CD equipment, wafer inspection stations, and joint CD/inspection systems are expected to reach $325 million in 1992. In particular, the emerging market for joint CD/inspection systems is anticipated to experience strong growth at a CAGR of 32.5 percent, reflecting a trend in the industry for multiple functionality and integrated applications on a single piece of capital equipment.

CD and Wafer Inspection Equipment Markets

Table 16

Forecast
Optical CD Equipment, Wafer Inspection Stations, and Joint CD/Inspection Systems, 1988–1992
(Millions of Dollars)

	Actual 1987	1988	1989	1990	1991	1992	CAGR 1987-1992
Optical CD Equipment	$39.5	$ 53	$ 61	$ 77	$ 99	$127	26.3%
Wafer Inspection Stations	24.5	36	41	50	62	76	25.4%
Joint CD/Inspection Systems	29.9	42	51	67	90	122	32.5%
Total	$94.0	$131	$153	$194	$251	$325	28.2%
Growth		39%	17%	27%	29%	29%	

Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
March 1988

The optical CD equipment market is forecast to grow at a 26.3 percent CAGR. This will be driven by the acceptance of new technologies for submicron measurement. At this time, however, no measurement technology has emerged as a clear leader. Over the next several years, SEM-based CD tools for the production environment will also emerge as significant competition for optical systems in the submicron measurement range.

Wafer inspection stations are expected to experience growth of 25.4 percent, or sales of $76 million in 1992. Within the category of wafer inspection stations, Dataquest expects most of the growth to come from advanced image-processing systems that rely on software algorithms or technology-based defect detection. In many cases, this capability, combined with critical dimension measurement, will be available in a joint CD/inspection system.

Market growth in each of the three equipment categories will be driven by the need for automated measurement and inspection tools for the sub-1.5-micron production environment, since sub-1.5-micron processing represents the major thrust in new fab capacity and IC production over the next five years. In a recent analysis, Dataquest concluded that 20 percent of silicon square inches consumed in the United States in 1992 will be used in sub-1.0-micron production, while an additional 37 percent of silicon will be used in production of devices with geometries greater than 1.0 micron but less than 1.5 microns. (These percentages of silicon square inches for sub-1.5-micron processing translate to 49 percent of silicon wafer starts.) While this analysis considers

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semiconductor production only in the United States, we believe that the figure of 57 percent of silicon square inches for sub–1.5–micron processing will be indicative of semiconductor processing in all regions of the world.

Dataquest believes that market growth for optical CD equipment, wafer inspection stations, and joint CD/inspection systems will be the result of equipment that incorporates the following:

- New technology implementations for submicron measurement
- Advanced image–processing algorithms for defect detection and classification
- Fully automated equipment operation for the production environment

These three factors will contribute to a continuing trend toward higher ASPs for equipment in the future, since equipment with increasing levels of sophistication carries a correspondingly higher price tag. In general, semiconductor manufacturers would prefer to minimize the amount of measurement and inspection of wafers during the fabrication process, since each additional task lengthens the cycle time and may, in itself, expose the wafer to additional contamination. CD measurement and wafer inspection systems, however, will not disappear altogether, since these tools provide vital information for monitoring process control in the production environment. While a reduction in measurement and inspection operations may impact overall unit demand, Dataquest expects the CD measurement and wafer inspection equipment markets to continue to experience healthy growth in the years to come.

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Equipment Communications

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Equipment Communications

SUMMARY

To maintain a competitive edge in manufacturing technology, major semiconductor manufacturers worldwide are adopting a strategy for automation of fabrication facilities in the 1980s. Processing and test equipment, workstation terminals, robots, and material transfer systems are being linked together through a communications network to support integrated manufacturing on the shop floor. Sophisticated software packages to control and coordinate the manufacturing environment are being developed in order to provide semiconductor manufacturers with timely access to the flow of information that characterizes the fabrication sequence of today's advanced devices.

The financial and strategic incentives for implementing computer integrated manufacturing (CIM) in the semiconductor industry have been the subject of numerous symposia and publications. The central goals of automation include efficient WIP (work in progress) monitoring of wafers through the processing sequence, increased equipment utilization through efficient line balancing, process recipe management, as well as access to and analysis of data to optimize process control in real time. In addition, the removal of the operator from the processing environment results in yield enhancement through reduced particulates. Semiconductor manufacturers must choose from a variety of criteria to evaluate the payback analysis most appropriate for automation of their facilities.

Protocol Specifications

Regardless of the CIM software package being employed, whether it is the result of an in-house development effort or a commercially available product, a successful automation effort requires a communications protocol for the network in order to establish the electronic guidelines for communication between the various computing devices on the shop floor. A communications protocol helps to ensure operational consistency and compatibility among the equipment-level, cell-level, and factory host computers operating in the network environment. In the semiconductor industry, SEMI (Semiconductor Equipment and Materials Institute) has proposed and developed SECS (SEMI Equipment Communications Standard) as a communications protocol for semiconductor manufacturing. Semiconductor equipment manufacturers are responsible for implementing the SECS protocol on their equipment to enable equipment/host communications within the fab.

Several semiconductor manufacturers such as Intel, Texas Instruments, and Thomson Components-Mostek Corporation, have already established minimum protocol specifications. DATAQUEST believes that equipment manufacturers that can satisfy the needs of IC manufacturers will gain a

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strategic market advantage in providing equipment to the semiconductor industry. Equipment manufacturers have the opportunity to participate in the formative stages of automation in the semiconductor industry, and in the process, to establish firm relationships with the automation leaders.

Equipment/Host Communications

The SECS protocol supports a hierarchical topology of computing devices in the semiconductor manufacturing environment. A host computer (for example, a VAX computer from Digital Equipment Corporation) is located at the top of this network topology and communicates with node or cell-level computers at an intermediate level. The node computers (for example, MicroVAX computers), in turn, communicate directly with a given set of processing equipment or robots that has been grouped together in a manufacturing cell. The equipment within a cell typically has similar processing functions and responsibilities, and as such exists as a distinct area of manufacturing activity. Semiconductor manufacturers have chosen a cell-by-cell approach to equipment automation in their facilities by automating one processing area at a time, such as a diffusion cell or photobay, and adding automation capabilities to new cells as time and resources allow.

As an example of an actual installation, Figure 1 illustrates the configuration of processing equipment, robotics, and computers in a fully automated diffusion furnace cell. Thomson Components-Mostek Corporation has chosen the Consilium COMETS package, including the PAM (Process Automation Management) module, for computer integrated manufacturing at its Carrollton, Texas, facility. An operator is responsible for inputting the appropriate lot identification (ID) at a workstation terminal in the fab. The host receives the ID number of the lot awaiting diffusion, and communicates the information to the cell-level controller and Veeco-dedicated MicroVAX, which in turn communicate with the robots and AGVs (automatic guided vehicles) that are responsible for material movement within the cell. The appropriate process recipe is downloaded from the node (cell-level) computer to the diffusion furnace, and the process is initiated automatically. All of the relevant processing status information and results are communicated to the node computer and the host system via the SECS II protocol, a subset of the SECS protocol that specifies a detailed message set for semiconductor manufacturing.

The purpose of this study is to evaluate and quantify the current status of SECS implementation by equipment manufacturers. The other equipment issues related to automation that will be discussed include the development of equipment-specific interfaces to link equipment to a given CIM software system, and the level of operator interactions with the processing equipment in a fabrication environment. The study also

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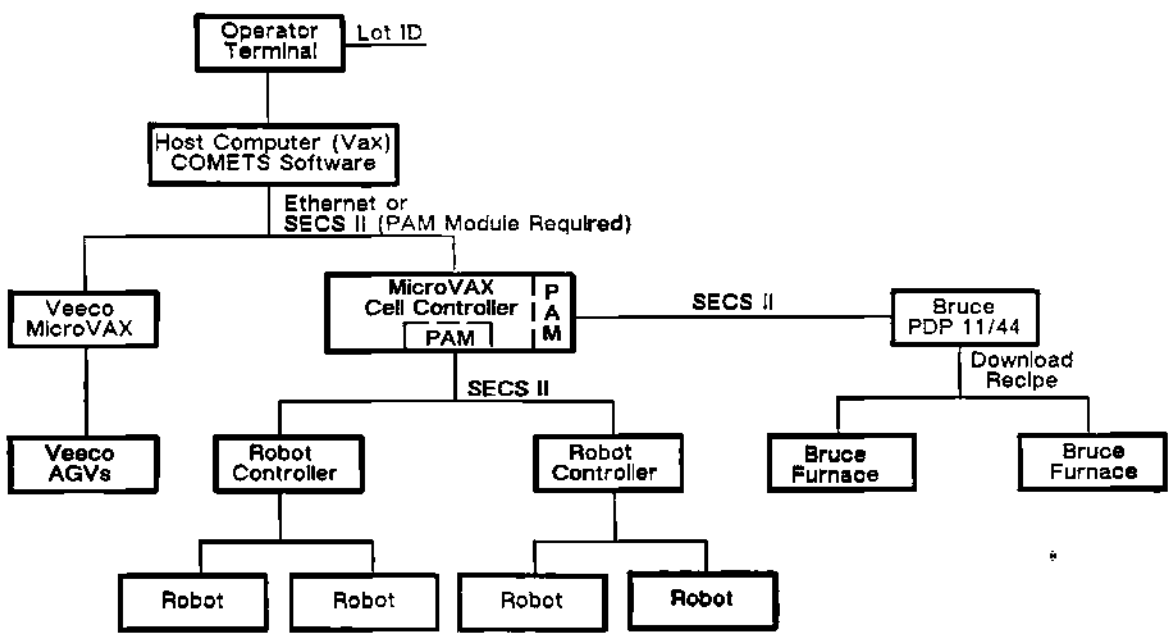
presents an overview of the SECS protocol, the communications standard MAP (General Motors' Manufacturing Automation Protocol), and MAP's potential impact on the semiconductor industry. Appendix A provides general background information on the concepts and terminology used to describe communications networks; particular emphasis is placed on those network components supported by the SECS and MAP protocols.

Figure 1

FULLY AUTOMATED DIFFUSION FURNACE CELL



Source: Thomson Components-Mostek Corp.
DATAQUEST
February 1986

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Equipment Communications

THE SECS PROTOCOL

In response to a growing concern to establish a communications protocol specifically focused on manufacturing in the semiconductor environment, the Semiconductor Equipment and Materials Institute (SEMI), through its Communications Subcommittee, proposed and developed an equipment communications protocol known in the industry as SECS. SECS is designed to provide communication capabilities between computers in semiconductor processing equipment and upstream node or host computers. In its simplest implementation, process recipe information can be downloaded from a host system to the equipment, and the equipment in turn can communicate process and equipment status information as well as collected data to the host system. Equipment-level communication (also referred to as Level 1 or cell-level communication) is the first step in a bottoms-up approach to integrated factory automation.

The SECS protocol is divided into two parts, known as SECS I and SECS II. The SECS I protocol, which addresses the electrical specifications and data link protocol between computers, was not designed to be specific to the semiconductor industry. The SECS II document, however, defines the general message set for transactions in a semiconductor processing environment, and as such, deal with units and concepts familiar to the industry, such as wafers, boats, and process recipes.

SECS I

The SECS I document was first published in SEMI Standards in 1980 and deals with the specifics of the electrical interface for connections between computers and the data link protocol (also known as the access method), which is responsible for establishing and governing the direction of communications between computers. (The electrical interface, RS-232, and the access method specified in the SECS protocol are discussed in Appendix A.) The SECS I document also defines the basic format for the message header, a 10-byte section of the message block that contains information used to ease the task of decoding transaction details.

SECS II

The SECS II document (first published in 1982) defines the message and data structures for the actual transactions between computers and processing equipment. The message set that has been chosen for the SECS protocol is meant to represent the typical activities required for IC manufacturing. Some number of custom messages may be required for

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equipment-specific applications. For a more thorough understanding of the protocol, the reader is encouraged to consult the SEMI document itself, or to participate in a tutorial short course on SECS such as that available from GW Associates, Mountain View, California.

Message Structure

A standard SECS message consists of a specified number of blocks of information. Multiblock messages are allowed by the SECS protocol and may contain up to 32,767 blocks for a total of 7.99 Mbytes of information in a single message. Each block includes a length byte, the message header (10 bytes), the text itself (0 to 244 bytes), and a checksum (2 bytes). The header (defined in SECS I) has a fixed format with bytes specified for the device ID (message source or destination can be designated), stream and function codes (identifies type of message to be sent), block number (specifies which block is being sent in a multiblock sequence), and system bytes (used for internal bookkeeping by the message source computer). The length and checksum bytes are used to validate successful message transmission between the source and destination.

Data Structure

The general topic of the message text is identified by the stream and function codes designated in the header. The message text within any given block of a multiblock message is structured as a series of data items. Each data item contains information that specifies the format of the data (ASCII, integer, floating point, etc.), the length of the data (in bytes), and the actual data itself. The protocol currently identifies 14 types of data format, and the choice of format is left to the user's discretion. A "list" data item may also be used to designate a series of data items in the message text. In a list data item, the length field specifies the number of data items contained in the list rather than the length in bytes of the list. In addition, list items can be embedded within other list items. Where appropriate, the protocol specifies the data and list structure of the different stream/function codes.

Message Set

The SECS II protocol classifies the different types of messages into eleven streams or general message types. Streams 1 through 11 are specifically defined in the protocol, while stream 0 is not used, and streams 12 through 63 are reserved for future use. Stream 64 through 127 are available for user-defined message topics.

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Within each stream, there are a number of function codes that identify the associated subtopics of each stream. The same function code can have different meanings in the different streams, but function 0 is always defined as the abort message within that stream. For each stream, functions 1 through 63 are reserved for the specified messages of the SECS II protocol and its future updates. Functions 64 through 255 are available for user-defined functions, which are also known as custom messages. The number of functions currently defined in the protocol varies from stream to stream, and new function codes will continue to be specified as the protocol matures. However, within every stream, when a conversation is undertaken between equipment and host, the query message always has an odd function value, and the response always has an even function message; together they constitute a transaction. In some streams, only the odd function codes are used because, due to the type of message, no response is required. The associated even function code for those types of messages are not used.

Stream Definitions of the SECS II Message Set - The eleven streams that have been defined in the SECS II protocol are found in Table 1, along with a brief description of the general message category. The number of specified functions within each stream is also identified. Aborts (function 0, or F0) are present in every stream and are included in the number of functions in Table 1.

Problems with the SECS Protocol

Several issues have been raised with regard to problems in the SECS protocol. Some of the concerns focus on SECS I issues and include speed of data transmission, as well as problems with "message flooding." Ambiguity in the SECS II message set and choice of data format have also been mentioned by equipment manufacturers. These points will be discussed in the following paragraphs.

SECS I Problems

The SECS I protocol specifies an RS-232 connection between equipment and host systems with a typical data transmission rate of 9,600 baud (characters per second). This is considered by many as too slow for effective shop floor communications between a large number of processing stations and a host system. Since some types of metrology and process/test equipment acquire large amounts of data, the SECS I protocol is not well suited for massive data transfers because of its limited speed. For those applications, some level of preliminary data reduction and analysis would be required before data are sent to an upstream host system. The SECS protocol also specifies a point-to-point topology, which many manufacturers consider cumbersome because of the requirement for discrete wiring and channels of communication for every communications device on the shop floor.

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Table 1

SECS II STREAM DEFINITIONS

Number	Stream Name and Definition	Specified Functions (#)
1	**Equipment Status** Allows host to monitor equipment status including current operating mode, depletion of consumables, and transfer status of material ports	11 (5 transactions, 1 abort)
2	**Equipment Control and Diagnostics** Messages deal with control operations of equipment from the host, includes remote operations and equipment self-diagnostics and calibration	29 (14 transactions, 1 abort)
3	**Material Status** Used to communicate material-in-process and time-to-completion information to the host	11 (5 transactions, 1 abort)
4	**Material Control** Used for automatic transfer of material between equipment	9 (8 odd functions, no responses specified, 1 abort)
5	**Exception Reporting** Communicates alarms generated by equipment in response to changing conditions detected by the equipment	7 (3 transactions, 1 abort)
6	**Data Collection** Covers the needs of in-process measurements and equipment monitoring	11 (5 transactions, 1 abort)
7	**Process Program Management** Used to manage and transfer equipment-specific process programs	35 (17 transactions, 1 abort)

(Continued)

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Table 1 (Continued)

SECS II STREAM DEFINITIONS

Number	Stream Name and Definition	Specified Functions (#)
8	**Control Program Transfer** Provides method for loading equipment-specific boot and executive programs	5 (2 transactions, 1 abort)
9	**System Errors** Allows for equipment to inform host that received message block cannot be handled, or that time-out on transaction has occurred	8 (7 odd functions, no responses specified, 1 abort)
10	**Terminal Services** Used to pass text messages between equipment operator terminals and the host	6 (5 odd functions, no responses specified, 1 abort)
11	**Host File Services** Provides limited access to host file system	13 (5 transactions, 2 odd functions with no responses, 1 abort)

Source: 1985 SEMI Standards Volume II, E5-85

In the SECS Communication Handbook, published by GW Associates (1985), two situations are identified in which the SECS protocol does not adequately deal with message flooding of the communications link. In the first example, a piece of equipment, designated as the master, may flood the host with alarm messages and, since the host system as the slave always yields to the master, the host system may be unable to send a message to the equipment to shut itself off. Some SECS implementations have added the capability for the host to send a reverse interrupt, which would temporarily shift the master designation from the equipment to the host system.

In the second example of message flooding, the host may inadvertently flood a piece of equipment that lacks sufficient buffer with a heavy flow of messages. If the equipment is too busy to receive additional messages, there is nothing in the protocol that would allow the equipment

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to send a wait-acknowledge response to the host system. The only alternatives available to the equipment result in what appears to be a transmission failure on the part of the equipment. These two examples of message flooding illustrate some insufficiencies of the SECS I protocol that could cause problems in some applications.

SECS II Problems

Semiconductor equipment manufacturers have expressed concerns that the SECS II message set of the protocol is too ambiguous. Several equipment vendors have indicated that it is not clear which stream/function code should be chosen for certain transactions. In addition, many manufacturers feel that the data format (binary, ASCII, floating point, etc.) for given messages should be specified, and not left as an arbitrary decision. The protocol currently provides 14 options for the data format. This level of discretion for the choice of data format can be a problem when an equipment manufacturer is trying to meet the particular specifications of different semiconductor manufacturers. These matters should be taken up with the SEMI Communications Subcommittee, which is responsible for the development and modifications of the SECS protocol as it matures.

THE MAP PROTOCOL

In the early 1980s, General Motors adopted a strategy of automation for its facilities to allow them to compete more effectively against the Japanese automotive industry. General Motors realized that a multivendor approach to automation would require a widely accepted, nonproprietary communication protocol for shop floor communications. The Manufacturing Automation Protocol (MAP) was developed by General Motors in 1982 in response to the need for such a standardized protocol for its manufacturing environment, and MAP has since gained acceptance as an evolving communications standard for general factory automation.

Specifically, MAP is a seven-layer, broadband, token-bus based communication protocol. The seven layers of MAP are based on the International Standards Organization's (ISO) Open Systems Interconnection (OSI) model for network communications. Broadband transmission, specified by the protocol, provides high-speed communications along multiple channels in the single transmission line of the bus network. The bus topology (the physical arrangement of computers within the network) specifies that the communications devices are linked to a single cable throughout the factory floor. Token passing is a type of access method that determines which computer within the network gets to transmit at any given time. The nature of token passing eliminates any possibility for more than one computer to talk along the same channel at the same time. (Broadband transmission, token passing and the bus topology are described in more detail in Appendix A.)

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Equipment Communications

MAP incorporates nationally and internationally accepted standards developed by the National Bureau of Standards (NBS), the Institute of Electrical and Electronic Engineers (IEEE), the International Standards Organization (ISO), and the American National Standards Institute (ANSI). Much interest has been focused on the MAP protocol because it has managed to gain a sizable backing from many large companies in the United States and the international community within a relatively short period of time. Many credit the influence of General Motors for accelerating what is typically a glacial rate for protocol and standards development.

In network communications, there are two separate issues: applications, which are concerned with the preprogrammed functioning of computers, and communications, which provide a method by which computers can talk to one another. The OSI model separates out the applications from communications, and it is the structural details of the latter that are divided into the seven layers of the model. Table 2 illustrates the structure and defines the functions of the seven-layer model.

A block of information transmitted through the MAP network increases in size as it is transferred from the application program down through the communications levels from layer 7 to layer 1. At each level, the appropriate message header information is added to the message block in order to facilitate the subsequent transfer of information to the next level. After the data have been encoded at layer 1 and physically transferred to the next communications device, the information is transferred back up through the layers of the protocol to layer 7 and the application program. The message header information specific to each given layer is stripped off as the block of information passes through that level. In this sense, the system is hierarchical, with each layer providing communication-related services to the layer immediately adjacent to itself. This "nesting of protocols" allows the application to be separate from the communications functions. The effect is that the microcomputer, controller, processing equipment, or robot on the factory floor is responsible only for performing its task, not for communicating its results through the layers of the communication network.

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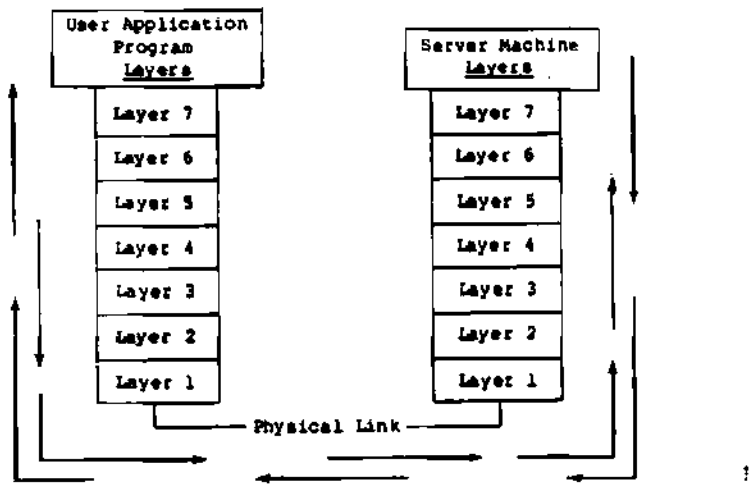
Table 2

THE SEVEN LAYERS OF MAP



Layer 1: **The Physical Layer**
This layer deals with most of the hardware questions involved in networking, such as the actual medium that will be used and the rates at which data will be sent.

Layer 2: **The Data Link Layer**
This layer concerns the composition of the actual "frames" of data that are sent out on the network, as well as the protocols for getting those transmissions onto the network.

Layer 3: **The Network Layer**
This layer sets up the procedure for communications between different networks.

Layer 4: **The Transport Layer**
This layer makes sure a message reaches its destination. It is responsible for assembling a message into frames, then reassembling the frames upon arrival and sending back an acknowledgement.

Layer 5: **The Session Layer**
At this layer, connections are established between stations and logical names are mapped onto physical addresses.

Layer 6: **The Presentation Layer**
This layer converts the message into a form that can be used by the receiving device.

Layer 7: **The Application Layer**
This layer brings network services, such as electronic mail, to the end user.

Source: Intel Corporation
DATAQUEST
April 1986

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Equipment Communications

A useful communications analogy to the OSI reference model is that of sending a letter through the postal system. When a letter (essentially a message or a block of data) is written and mailed, it must go through a series of intermediate steps before it is received at its final destination. The letter is placed in a mailbox, it is collected by a postal carrier, taken to the local post office, collated, sent on to a central post office, and collated once more for final destination. It is then transported (in some sense, analogous to the physical link) by truck, rail, air, or by ship to the receiving central post office. The letter goes through the appropriate sort mechanism, is sent off to the receiving local post office, sorted again, and delivered to the final destination. The communication sequence is independent of the contents of the letter that was written. In an analogous fashion, the seven layers of the OSI reference model facilitate communications in a factory network, but their operations are independent of the contents of the message that is being transmitted.

MAP Users Group

The MAP protocol has been aggressively promoted by General Motors as a viable standard for factory communications between equipment and computers supplied by multiple vendors. Many manufacturers have endorsed the protocol, including Boeing, Ford, General Electric, and Westinghouse. In addition, more than 350 companies have joined a MAP Users Group to promote industry-wide understanding of the protocol and provide a forum for discussion of MAP issues as the protocol matures. The MAP Users Group was established in February 1984 by General Motors with the assistance of such firms as DuPont, Eastman Kodak, and McDonnell Douglas. The Society of Manufacturing Engineers (SME) is responsible for coordinating the administrative activities of the MAP Users Group.

Boeing, in addition to supporting MAP, has developed TOP (Technical Office Protocol), which applies the same seven-layer architecture to office automation that MAP applies to manufacturing on the factory floor. A MAP/TOP Steering Committee is looking at integration of these two protocols that would allow transfer of data between management and manufacturing applications.

The MAP standard has been endorsed by many computer-based system suppliers as well. The list includes Allen-Bradley, Concord Data Systems, Digital Equipment Corporation, Hewlett-Packard, IBM, and Texas Instruments. In the semiconductor industry, Motorola, Intel, Industrial Networking Inc. (a joint venture between General Electric and Ungermann-Bass Inc.), and Concord Data Systems (in conjunction with Gould/AMI Semiconductor) have been very active in the production of chip and board-level products for the MAP standard.

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International Activity

The MAP protocol has also generated interest from European and Japanese manufacturers. In Europe, MAP's counterpart is known as the European Communications Network for Manufacturing Automation (CNMA), a project of the ESPRIT research and development program sponsored by the European community. CNMA also plans to establish protocol capabilities for automated manufacturing and to evaluate and test them in practical applications. Siemens recently joined the CNMA, and will also continue to support MAP activities worldwide. The U.S. MAP Users Group has held discussions with Siemens concerning the compatibility of the MAP standards with the direction of communications development by the CNMA. MAP is also being evaluated in Japan. General Motors delivered a major presentation on the MAP protocol to Japanese manufacturers in the summer of 1985, and one GM official recently commented that he expects Japanese manufacturers to develop MAP products within the next year.

Testing of the MAP Protocol

One of the major obstacles to overcome in the acceptance of the MAP protocol as a de facto standard for manufacturing communications lies in the area of testing. Not only do individual products need to be tested for compliance to the multilayered MAP standard, but the successful interoperability between products from multiple vendors must be established. As with any emerging standard, vendor interpretation of the MAP specifications may still differ, which means that systems can be built that conform to the standard, but may not work with other "standard" products.

A demonstration at last November's Autofact '85 (a factory automation trade show held annually in Detroit) included an exhibit of products from 23 vendors tied together by a MAP system. The demonstration was sponsored by General Motors and Boeing, and vendors participating in the demonstration included Allen-Bradley, AT&T, Concord Data Systems, Digital Equipment Corporation, Gould, Hewlett-Packard, Honeywell, IBM, Industrial Networking Inc. (INI), Intel, Motorola, NCR, Northern Telecom, and Siemens. While the demonstration was hailed as an important step toward successful MAP implementation, it was considered by many as still a far cry from an actual installation of the communications protocol in a manufacturing and assembly line plant.

Work to develop MAP test equipment is under way at several locations, including General Motors, NBS, and the International Technology Institute (ITI), a nonprofit organization in Ann Arbor, Michigan. In September of 1985, the ITI became the first organization to introduce an independent conformance testing service for MAP products. General Motors is

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developing test facilities for MAP products in Canada, England, France, Germany, and Japan. Proposals have also been made for consortiums funded by multiple vendors and users of the MAP protocol to support the development of MAP testing tools. Many, however, concede that current test systems cannot check out MAP adequately for all operating situations that may be encountered in a real network, and that significant tasks lie ahead to determine how to test equipment for MAP compatibility and interoperability in a black-box test environment.

Problems with the MAP Protocol

In addition to a lack of test equipment and procedures for the MAP protocol, several other areas must be addressed before widespread implementation of the standard can be achieved. These include the specification of standards at the upper levels of MAP, development of low-cost interfaces to the network, and development of gateways to allow communication between MAP and non-MAP networks.

The MAP protocol is still in the development stage. Standards have been specified at the lower levels of the seven-layer model; however, standard specification at the upper levels has not been completed. The IEEE 802.4 standard, which is familiar to most people following MAP development, is employed only at layers 1 and 2, the physical and data link levels. General Motors officials claim that all of the standards should be in place by the end of 1988.

A network interface connects a node or network station to the broadband backbone of the MAP network. Between an equipment controller and the network itself, there will always be a "box," the network interface. It provides conversion of the node's protocol to the protocol used by the network and controls when the node can transmit. The interface could be, for example, a modem or an intelligent card. Currently, the costs for node/network interfaces are still high, and the lack of low-cost interfaces impedes the development of MAP-based communications networks. The continuing development of chip and board-level products to interpret the different levels of MAP will replace existing software programs and reduce costs for network interfaces.

A gateway provides interconnect capability from a MAP-based network to another digital communications system. It not only serves as the interface between two networks, but also provides protocol conversion between the two communications systems. Many facilities have local area networks such as DECNet or Ethernet in place. These systems would still be able to communicate with a MAP-based system through the gateway. For example, a group of CAD stations might communicate through an Ethernet

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system. When it comes time to send data to a host system, one computer in the cluster would be responsible for sending the information through a transfer device, or gateway, into the larger MAP network. Implementation of the MAP protocol in a semiconductor manufacturing environment might well employ a gateway to provide protocol conversion between SECS used at the lower levels of the communications network and a MAP-based system operating at the upper levels.

Finally, perhaps MAP's biggest problem is that the protocol is not simple, and thus there is a large degree of confusion as to how to design MAP-compatible products and how to implement a MAP-based communications network. Education will need to continue at all levels to ensure that MAP will continue to gain acceptance as a general communications protocol for factory automation.

SECS AND MAP IN THE SEMICONDUCTOR INDUSTRY

There has been some discussion that SECS might eventually be replaced by MAP as the communications protocol for semiconductor automated facilities. Some manufacturers have expressed doubt whether SECS has sufficient capability to provide the requirements of interactive communications in a large communications network. These manufacturers' complaints include that SECS is too slow, that it is based on only one standard (RS-232), and that it requires a point-to-point configuration that has logistic and economic disadvantages when the automation environment grows beyond a certain size. The question has been raised whether MAP may be a suitable substitute for SECS or if complementary components of the two protocols might be brought together for implementation in the semiconductor industry. Table 3 summarizes the advantages of these two protocols that would provide complementary functions in possible future applications in the semiconductor manufacturing environment.

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Table 3

MAP AND SECS COMPARISON

MAP	SECS
Based on ISO/OSI model, which allows different types of network interconnections; uses ISO, NBS, and IEEE standards, all large standards organizations	Has an existing organization (SEMI) that focuses on specific semiconductor industry needs
Designed for general manufacturing environment; has the backing of large organizations	Has a good message set, specifically designed for semiconductor manufacturing environments
Thousands of man-hours have been invested; many MAP-related products have been developed	Many working implementations of the protocol exist
A real network (broadband, token-passing bus), not just a point-to-point configuration	

Source: DATAQUEST
May 1986

SEMI's Communications Subcommittee established the Network Implementation Task Force (NITF) in 1985 to develop network standards for the semiconductor industry. In particular, the NITF has decided to evaluate the potential for implementing the MAP protocol in a semiconductor manufacturing environment. Figure 2 illustrates the point-to-point arrangement of computers and equipment specified by the SECS protocol, and presents for comparison the topology that DATAQUEST expects will be employed in a SECS/MAP environment. This scenario retains the SECS protocol for communications between equipment and cell-level and node-level computers. Upper-level communications between host and node computers would follow the MAP specifications for a broadband, token-bus network that would provide high-speed communications along the multichannel transmission line of the bus. The SECS II message set would be maintained throughout the network environment because of its specificity to semiconductor manufacturing. MAP's message set is currently free-form in design and does not focus on the specific message needs of any given industry.

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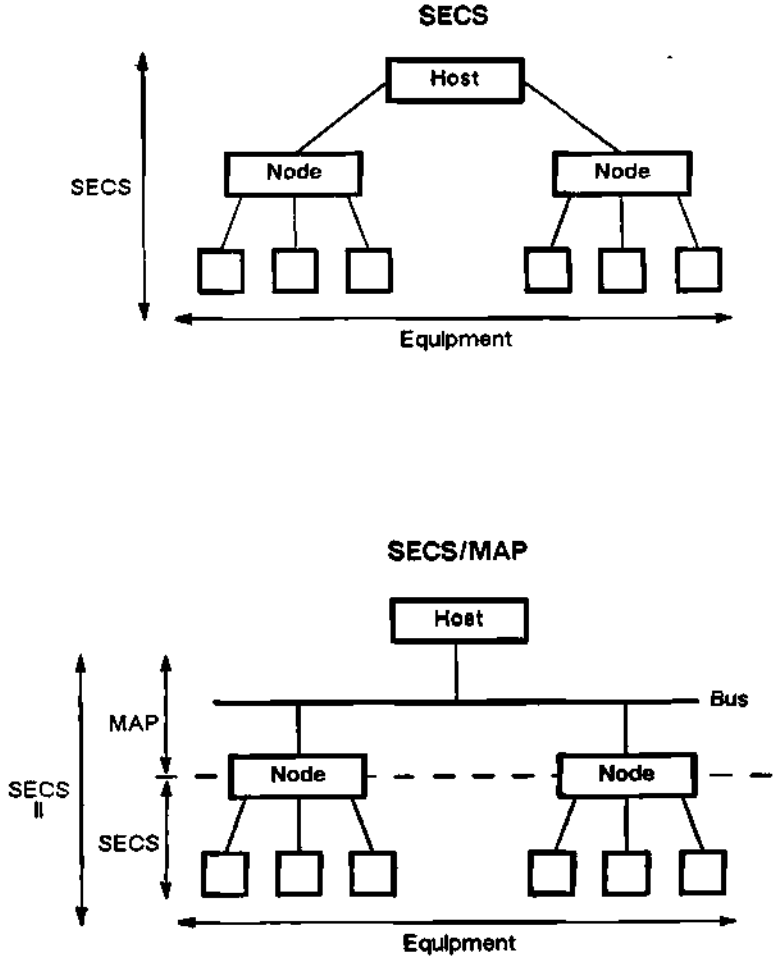
Equipment Communications

CIM manufacturers, such as Consilium and PROMIS Systems (a wholly owned subsidiary of I.P. Sharp), would be responsible for providing gateways between the MAP and SECS protocols. The gateway would likely reside at the level of the node computer to act as a translator between communications on the bus network of MAP and the point-to-point topology of semiconductor processing equipment that communicates with SECS. Equipment manufacturers most likely will not be responsible for linking their equipment directly to the MAP token-bus network, but will continue protocol implementation as specified in the SEMI SECS document.

Figure 2

SECS AND SECS/MAP TOPOLOGIES



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May 1986

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However, equipment vendors cannot afford to entirely ignore the design and development of the MAP protocol and its associated chip and board-level products. The lack of understanding and education in automation issues, including protocol development, can result in substantial confusion, misdirected activities, and misspent resources for all concerned in the automation effort. MAP is a particularly complex and involved protocol, and DATAQUEST strongly encourages equipment manufacturers to either start now or continue current efforts in monitoring MAP development.

VENDOR IMPLEMENTATION OF THE SECS PROTOCOL

Equipment Survey Overview

DATAQUEST recently conducted a survey of semiconductor equipment manufacturers in order to evaluate the level of vendor commitment to the SECS protocol. Twenty-six equipment manufacturers representing eight general types of front-end processing equipment participated in the study in which a total of 42 models of equipment were discussed. The eight categories of front-end processing equipment include chemical vapor deposition (CVD) reactors, diffusion furnaces (including annealers) epitaxial reactors, dry etch equipment, ion implanters, lithography, sputtering, and automatic photoresist processing (track) equipment. The 26 survey participants combined represented 50 percent overall market share of the 1984 worldwide semiconductor front-end processing equipment market. The combined market share of survey participants in each equipment category is presented in Table 4. For example, the five lithography companies surveyed represented 75 percent of the 1984 lithography market.

Table 4

SURVEY PARTICIPANTS' 1984 WORLDWIDE MARKET SHARE
BY EQUIPMENT CATEGORY

Equipment Category	Participants' Sum Market Share
CVD	14%
Diffusion/Anneal	55%
Dry Etch	62%
Epitaxy	58%
Ion Implantation	79%
Lithography	75%
Sputtering	54%
Track	61%

Source: DATAQUEST
May 1986

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Equipment Communications

Discussions with equipment vendors were undertaken with the condition that information provided would not be reported by company; instead the information would be used to establish an industry perspective on equipment-level implementation of the SECS protocol and related automation issues. Participants in the study are identified in Table 5. The number beneath each equipment category indicates the number of equipment models that were discussed in the survey. In some instances, several models of equipment from the same vendor have been included. Vendor responses were for existing equipment models that are considered to be the most advanced, as well as for next-generation equipment currently under development.

Table 5

EQUIPMENT SURVEY PARTICIPANTS

	CVD	Diffusion/ Anneal	Dry Etch	Epitaxy	Ion Implant	Lithography	Sputtering	Track
Models of Equipment	4	6	9	3	3	6	4	7
Companies								
Advanced Crystal Sciences, Inc.		X						
ASM America		X						
Anicon Incorporated	X							
Applied Materials, Inc.			X	X	X			
BTU Engineering Corporation		X						
Drytek Inc.			X					
Eaton Corporation					X	X		X
GCA Corporation			X			X		X
Gemini Research				X				
Genus Incorporated	X							
Lam Research Corporation			X					X
Machine Technology, Inc.							X	
Materials Research Corporation			X					
Nikon Precision, Inc.						X		
Perkin-Elmer			X			X	X	
Semiconductor Systems, Incorporated								X
Silicon Valley Group, Inc.	X							X
Solitec, Inc.								X
Tegal Corporation			X					
Temescal							X	
Thermco Systems, Inc.		X						
Tylan Corporation		X						
Ultratech Stepper						X		
Varian Associates	X	X			X		X	
Veeco Instruments Inc.								X
Zylin Corporation			X					

Note: In some cases, more than one model of equipment from the same vendor has been included in a given equipment category.

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SECS II Implementation by Equipment Vendors

Of the 42 equipment models that were surveyed, 39 models have SECS capability. Of those 39 equipment models, 28 models already have an existing SECS protocol implementation, while 11 models have their SECS implementation currently under development such that a software release will be available in 1986. Table 6 summarizes the vendor response on SECS implementation by equipment category.

Table 6

IMPLEMENTATION OF THE SECS PROTOCOL

Equipment Category	Yes	UD	No
CVD	2	2	0
Diffusion/Anneal	5	1	0
Dry Etch	6	3	0
Epitaxy	1	1	1
Ion Implantation	2	1	0
Lithography	3	2	1
Sputtering	3	1	0
Track	6	0	1
Total	28	11	3
Percent Response	67%	26%	7%

Source: DATAQUEST
April 1986

In order to quantify the level of vendor implementation of the SECS protocol, equipment manufacturers were requested to provide specific information on their SECS II message set, in particular the total number of SECS II messages and the number of messages per stream, whether specified or custom. Message detail was provided by equipment manufacturers for 27 of the 39 models of equipment. Transactions between equipment and host typically consist of a query and a response, each of which has a different function code designation in a given stream. Survey respondents were requested to include the total number of stream/function codes (messages) that the equipment is responsible for sending to or receiving from a host system. Custom messages are included in the message count. Vendors were also requested to indicate whether they had chosen to include any of the abort transactions (function 0) provided in each stream.

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Total Message Count

The SECS II protocol provides a general message set for transactions between processing equipment and a host computer system in an automated semiconductor fabrication environment. However, as one equipment vendor was quick to point out, "No two people do SECS the same way." Therefore, while the SECS protocol does provide a standardized structure for communications, a great deal of variety exists in the interpretation and number of messages a vendor has chosen to specify for his equipment.

Each point in Figure 3 represents the total number of SECS II messages from a particular model of equipment (total 27 models of equipment). For example, the three models of lithography equipment have message sets consisting of 31, 36, and 37 function codes, respectively. The number of messages in Figure 3 represents those function codes (both specified and custom) that equipment vendors have implemented in the eleven standard streams of the protocol. (Two vendors have developed messages for custom streams; these messages are not included in Figure 3.) Not only is there a wide range in the number of messages between the various categories (18 to 214), but also within a given equipment category. (Sputtering equipment, epitaxial, and CVD reactors have been classified in a general deposition equipment category in this figure to maintain equipment vendor anonymity.)

The average number of total messages implemented by equipment vendors in Figure 3 is 38 (excluding the one diffusion entry of 214 messages). The absolute number of messages implemented by a given equipment manufacturer does not necessarily reflect the level of protocol software sophistication for the equipment. It is possible that some equipment manufacturers have chosen to implement a very efficient, compact message set while others have included a large number of special-function custom messages to enhance the protocol's capabilities.

What is most important is not the absolute number of messages that have been chosen but rather that the implemented message set includes all of the necessary functional components of the protocol such as recipe management (uploading and downloading), process and equipment status, and alarm information. Two factors--specific message code implementation and functionality of the message set--could well be represented by a unique set of stream/function codes, which, if detailed in the exact same manner by all equipment manufacturers, would ensure a standardized implementation across the board for all types of equipment. However, in reality vendor interpretation and implementation of the SECS II messages can vary considerably, and yet still meet the necessary requirements for functionality of the message set.

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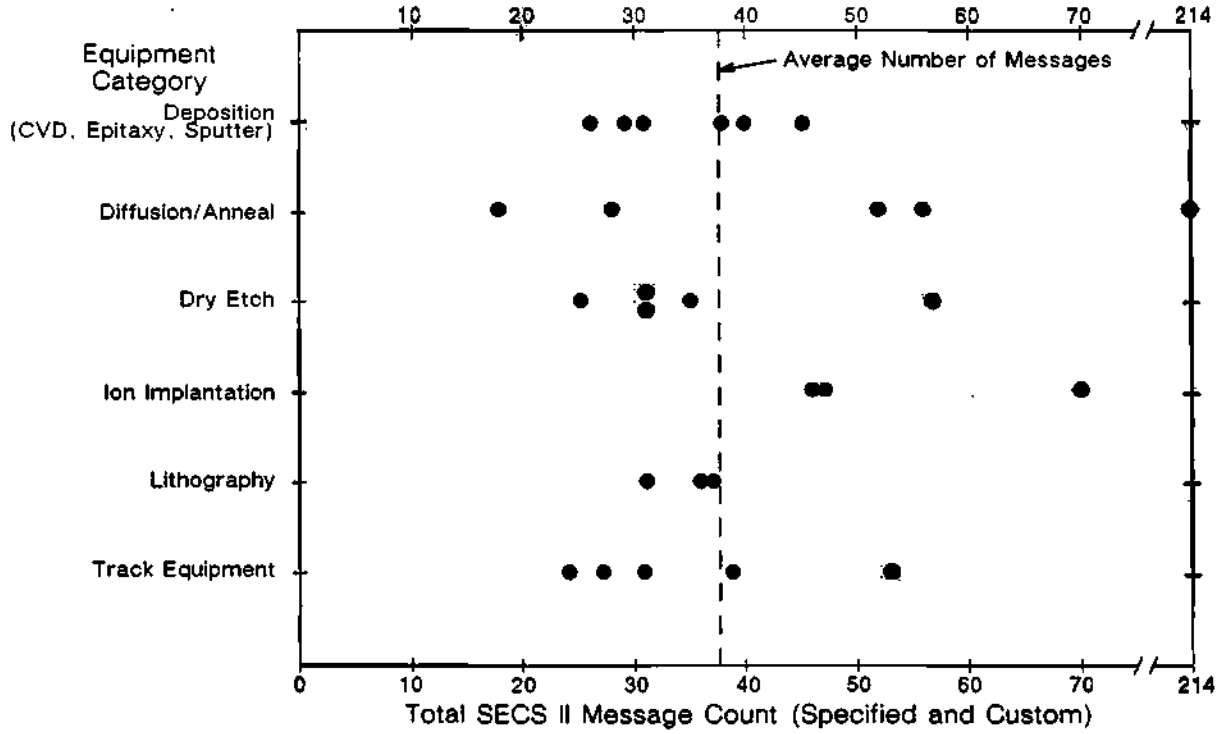
Figure 3

TOTAL SECS II MESSAGE COUNT--SPECIFIED AND CUSTOM
BY EQUIPMENT CATEGORY



Source: DATAQUEST
MAY 1986

Upon the completion of their SECS protocol, equipment manufacturers must be able to provide semiconductor manufacturers with a document that contains details of their SECS II message set. Semiconductor manufacturers such as Intel, Texas Instruments (TI), and Thomson Components-Mostek Corporation (TCMC), have taken the first step in equipment-level automation and have provided equipment manufacturers with minimum SECS II message set requirements. These manufacturers feel that their minimum message sets include the essential functionality of the SECS II protocol. In addition, they are attempting to ensure standardization throughout their own facilities by providing clear guidelines to the equipment industry. Other semiconductor manufacturers have chosen to specify the broad functional components of the protocol,

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which they feel are necessary for equipment/host communication in an automated facility. The details of the protocol implementation are left to their equipment vendors and the CIM manufacturer responsible for coordinating their automation efforts.

Specified Message Count

Figure 4 compares the number of protocol-specified messages implemented by equipment manufacturers with the number of messages specified by Intel and Texas Instruments in their minimum SECS message sets. The information in Figure 4 is essentially the same as that contained in Figure 3, except that custom messages have been removed from the total message count for 14 of the 27 equipment models that include these equipment manufacturer-defined functions. On the basis of specified message count, the average number of messages implemented for the 27 equipment models is 34.

Intel's SECS II specification identifies 42 messages from 7 different streams as the minimum set necessary for implementation on process and analytical equipment. Only 6 equipment models of the 27 represented in Figure 4 can meet Intel specifications based on specified message count alone. Similar to Intel, TI also has a set of specifications that defines a minimum set of messages for equipment vendor implementation. In TI's case, 51 messages in 9 streams have been identified. Only 3 of the 27 equipment models in Figure 4 have more than 51 specified messages in their SECS II message set. In addition, only 14 of the 27 survey respondents that provided detailed information on their SECS II message sets included any abort messages in their protocol implementation. Both Intel and Texas Instruments require the abort message for every stream in which messages have been specified. On the basis of the information presented in Figure 4, the majority of equipment manufacturers will have to make substantial additions to their present message sets in order to satisfy Intel and Texas Instruments requirements.

Intel and Texas Instruments recognize that minimum SECS II requirements from semiconductor manufacturers should be focused on specific categories of equipment rather than on a general message set for all wafer processing equipment. Both manufacturers are willing to negotiate their minimum message set requirements with equipment vendors since in some cases, the messages may not be appropriate for a given type of equipment. However, these semiconductor manufacturers will not negotiate when an equipment vendor has chosen to implement his own custom messages when existing messages in the protocol would have sufficed. The generic minimum message subsets from Intel and TI are meant as a guideline for equipment protocol development to ensure that equipment purchased for Intel and TI facilities has sufficient communications capability to operate in an automated environment. Clearly, if Intel's and Texas Instruments' message sets are indicative of the minimum requirements for general SECS II implementation in the industry, the

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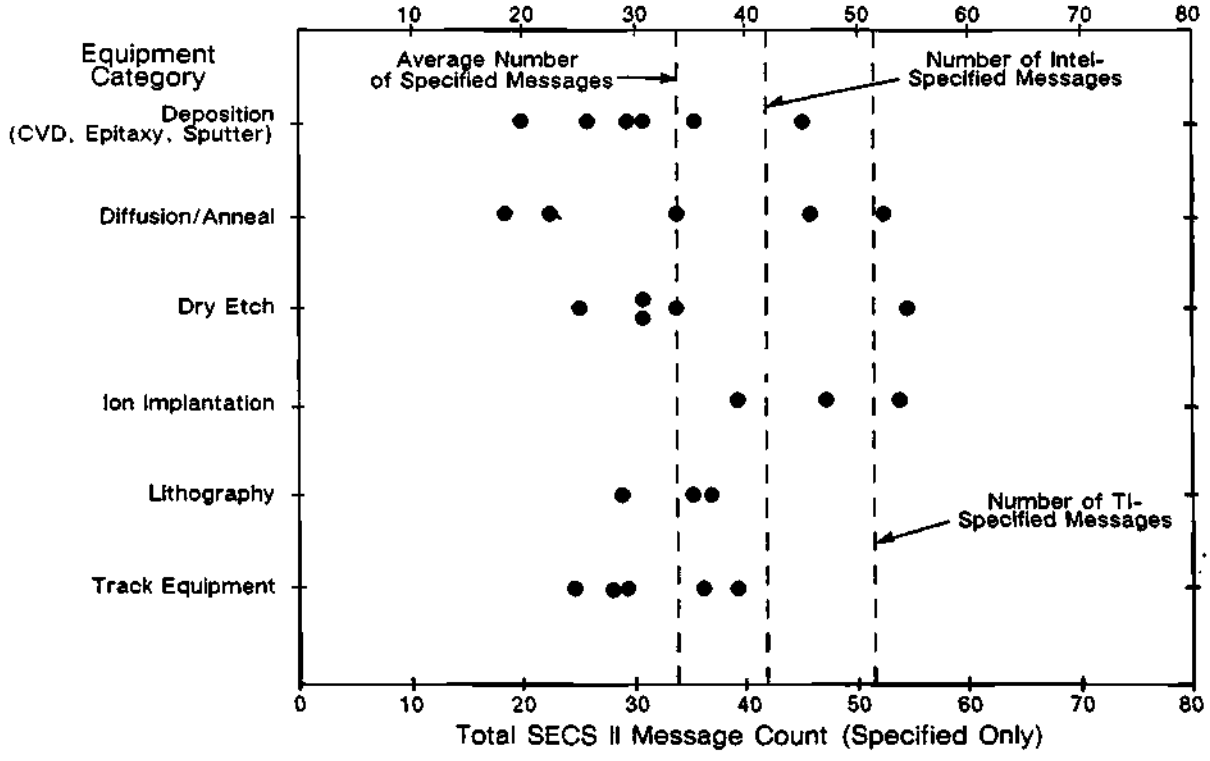
majority of equipment vendors face major customization of their SECS protocol at some stage when a semiconductor manufacturer decides to automate its facilities. DATAQUEST believes that this is an extremely important finding to come out of this survey.

Figure 4

TOTAL SECS II MESSAGE COUNT--SPECIFIED ONLY
BY EQUIPMENT CATEGORY



Source: DATAQUEST
MAY 1986

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Message Count per Stream

Table 7 contains information on the average number and range of function codes implemented per stream for the 27 equipment models represented in Figure 3. Equipment manufacturers choose the set of messages that they feel are most appropriate for implementation on their equipment. The first column in Table 7 indicates the number of equipment models for which any messages (whether specified or custom) have been implemented from the 11 streams. The second column identifies the total number of function codes per stream that have been specified to date in the SECS II protocol document (from Table 1). The average and range in the number of function codes that equipment manufacturers have chosen to implement is presented in columns three and four of Table 7.

Table 7

FUNCTION CODE COUNTS PER STREAM

	Equipment Models with Function Codes in the Stream	Total Number of Function Codes Specified in Protocol	Average Number of Function Codes Implemented	Range in Number of Function Codes
Stream 1				
Specified	27	11	4	2-9
Custom	6	0	3	1-7
Stream 2				
Specified	27	29	7	2-20
Custom	8	0	7	1-34
Stream 3				
Specified	7	11	2	1-5
Custom	4	0	5	1-8
Stream 4				
Specified	7	9	6	1-9
Custom	6	0	12	2-36
Stream 5				
Specified	25	7	3	1-6
Custom	3	0	3	1-6
Stream 6				
Specified	16	11	4	1-10
Custom	4	0	3	1-10

(Continued)

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Table 7 (Continued)

FUNCTION CODE COUNTS PER STREAM

	Equipment Models with Function Codes in the Stream	Total Number of Function Codes Specified in Protocol	Average Number of Function Codes Implemented	Range in Number of Function Codes
Stream 7				
Specified	25	35	8	4-15
Custom	5	0	16	1-54
Stream 8				
Specified	0	5	0	0
Custom	1	0	30	30
Stream 9				
Specified	27	8	6	1-8
Custom	2	0	2	1-3
Stream 10				
Specified	10	6	3	1-5*
Custom	0	0	0	0
Stream 11				
Specified	1	13	5	5
Custom	0	0	0	0

*Note: One manufacturer has chosen to include an additional 7 specified function codes in Stream 10 that have yet to be accepted by the SEMI Communications Subcommittee for incorporation into the SECS II message set. With the inclusion of those additional 7 responses, the average number of messages specified in Stream 10 is 4, with a range of 1 to 11.

Source: DATAQUEST
May 1986

Specific stream/function message detail is regarded by many equipment manufacturers as proprietary information, so only the number of function codes implemented are included in Table 7. The SECS protocol provides equipment vendors with the option of implementing custom streams (S64-S127) as well as custom function codes (F64-F255). Two of the 27 message sets that were received by DATAQUEST in the survey include custom streams and 14 of the 27 message sets contain custom function codes. Table 7 does not contain custom stream information, only those function code counts for the 11 specified streams of the SECS II protocol.

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In Table 7, the streams that show the largest degree of protocol activity are Streams 1 (Equipment Status), 2 (Equipment Control and Diagnostics), 5 (Exception Reporting), 7 (Process Program Management), and 9 (System Errors). At this time, only 7 equipment models in the survey have specified functions implemented in Stream 4, which defines messages associated with material control and provides for equipment/robotic interactions. No equipment models include specified functions from Stream 8, which is responsible for loading equipment-specific boot and executive programs. (For some models and types of equipment, this type of application is not possible.)

Again, it is instructive to compare equipment vendor activity in a given stream with the specifications that Intel and Texas Instruments have defined as a minimum message set for SECS II protocol implementation. Table 8 compares the average number of specified function codes per stream implemented by equipment vendors (from Table 7) with the number of messages in the 10 streams that Intel and TI recommend for a minimum message set. Both Intel and TI require that the abort transaction (F0) be included in every stream in which messages have been specified, therefore, these messages are accounted for in Table 8. As mentioned previously, of the equipment vendors that provided protocol information to DATAQUEST, only 14 of 27 responses have chosen to include any abort transactions in their protocol implementation.

Table 8

FUNCTION CODE COUNTS PER STREAM FOR VENDOR IMPLEMENTATION, INTEL, AND TI REQUIREMENTS

	Equipment Models with Function Codes in the Stream	Total Number of Function Codes Specified in Protocol	Average Number of Function Codes Implemented	Intel Number of Function Codes Specified	TI Number of Function Codes Specified
Stream 1					
Specified	27	11	4	3	7
Stream 2					
Specified	27	29	7	11	7
Stream 3					
Specified	7	11	2	4	7

(Continued)

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Table 8 (Continued)

FUNCTION CODE COUNTS PER STREAM FOR
VENDOR IMPLEMENTATION, INTEL, AND TI REQUIREMENTS

	Equipment Models with Function Codes in the Stream	Total Number of Function Codes Specified in Protocol	Average Number of Function Codes Implemented	Intel Number of Function Codes Specified	TI Number of Function Codes Specified
Stream 4 Specified	7	9	6	*	9
Stream 5 Specified	25	7	3	7	3
Stream 6 Specified	16	11	4	3	5
Stream 7 Specified	25	35	8	*	5
Stream 8 Specified	0	5	0	5	*
Stream 9 Specified	27	8	6	8	5
Stream 10 Specified	10	6	3	5	3
Stream 11 Specified	1	13	5	*	*

*No specifications at this time.

Source: Intel Corporation
Texas Instruments
DATAQUEST
May 1986

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While the specific function codes that Intel and Texas Instruments have identified in their minimum subsets are not compared directly with the vendors' choice of messages, it is only in Streams 1 and 6 that equipment vendors have exceeded the number of minimum messages specified by Intel, and in Streams 2, 5, 6, 9, and 10 that equipment vendors have equaled or exceeded the message count specified by Texas Instruments.

Table 8 also illustrates the degree of variability between the message sets of the two semiconductor manufacturers. In the case of Stream 8, Intel specifies that all five function codes be implemented, when applicable, while Texas Instruments has chosen not to include any messages from Stream 8. On the other hand, Texas Instruments has identified messages from Streams 3, 4, and 7, where Intel has no specifications at this time. If an equipment manufacturer chose to comply with the number of messages that would satisfy both Intel and TI specifications (based on the overlap of the stream/function message set between TI and Intel), a total of 73 specified messages from the SECS II protocol would be required. Not a single equipment model of the 27 that provided detailed protocol information in the DATAQUEST survey can meet both Intel and TI's minimum message set specifications on the basis of message count alone.

As mentioned previously, both TI and Intel recognize that protocol message requirements really should be directed toward specific equipment categories, and both are willing to negotiate with equipment manufacturers over messages that are not necessarily appropriate for a given type of processing equipment. However, for a fully automated manufacturing facility, semiconductor manufacturers probably will require equipment communications capability to exceed those specifications already identified by Intel and Texas Instruments.

Additional Specifications

Up to this point, discussion in this analysis has centered only on the number of function codes that have been specified in each stream. For a more accurate comparison of protocol specifications between equipment and semiconductor manufacturers, the actual function code numbers used to identify the messages and the data structure also must be identified. The data structure includes the data element name, the format, and the length (in bytes) of the data. The SECS II protocol does provide data element names but data format, of which there are 14 options in the protocol, and data length are variable. Therefore, even if semiconductor and equipment manufacturers specify the identical stream/function codes, it is still possible that the message sets are not entirely compatible due to differences in the data format and length. Equipment and semiconductor manufacturers must come to a common consensus for data structure as well as protocol specifications in order to achieve some level of standardization in equipment communication throughout the industry.

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Custom Messages

The SECS protocol provides equipment vendors with the option of implementing custom streams (S64-S127) and custom function codes (F64-F255). The SEMI Communications Subcommittee recognizes that there will be user needs beyond the specific definitions given in the protocol because of equipment-specific applications. In addition, the protocol reserves stream and function codes for future messages that will be adopted by the Communications Subcommittee as the protocol matures. One vendor that supplied protocol information to DATAQUEST included an additional 7 messages in Stream 10 that as yet have not been adopted by the committee. Two of the 27 message sets in the survey include custom streams and 14 of the 27 message sets contain custom function codes. Table 9 summarizes custom message implementation by equipment category for the 27 message sets.

Table 9

CUSTOM MESSAGE IMPLEMENTATION BY EQUIPMENT CATEGORY

Category	Yes	No
CVD	1	2
Diffusion/Anneal	3	2
Dry Etch	3	2
Epitaxy	1	0
Ion Implantation	2	1
Lithography	2	1
Sputtering	0	2
Track	2	3
Total	14	13

Source: DATAQUEST
April 1986

From Table 9, it is clear that equipment manufacturers are implementing custom messages in all categories of front-end processing equipment (except sputtering, for which only a limited sampling size was available). While custom messages provide extended communication capability for equipment-specific applications, their presence also demands that semiconductor manufacturers and equipment vendors have a

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clear, consistent understanding of the interpretation of these messages. Some semiconductor manufacturers will not accept processing equipment utilizing a custom message set without conducting substantial negotiations. In particular, TI and Intel will not accept custom messages when specified messages within the SECS II message set would have sufficed. In addition, the development of an equipment-specific interface by a CIM manufacturer requires additional time, resources, and cost for those equipment models that implement a large custom message set. Thus, equipment manufacturers that choose to include custom messages in their protocol should carefully evaluate semiconductor and CIM manufacturer response to their message set in order to avoid unnecessary costs or delays in protocol acceptance and interface development required before the equipment can be integrated into an automated environment.

Testing of the SECS Protocol

It is very important that an equipment vendor's implementation of the SECS protocol is tested, not only to ensure compliance with protocol specifications, but also to provide semiconductor manufacturers with the appropriate support documentation for the equipment. Several products are available that allow a semiconductor equipment manufacturer to test the implementation of his protocol. These systems include a SECS Protocol Emulator available from Texas Instruments, and SECSIM, a SECS Simulator from GW Associates. Both systems provide host and equipment emulation, and can send valid or invalid messages to monitor host/equipment responses. Both systems are PC-based for flexibility and low cost, and allow field engineers to provide trouble-shooting capability at the time of equipment installation within the communications network. Equipment protocol testing with CIM manufacturers is also possible with a CIM-based SECS emulator package or through a telephone hookup. CIM manufacturers encourage equipment manufacturers to have the proper dial-out and dial-in modems available at their facilities for the initial testing phase of their SECS protocol.

In addition, some equipment manufacturers have chosen to develop host emulator software packages. For example, Silicon Valley Group (SVG) provides an IBM XT-compatible software package for communication and protocol testing of its Host Computer Interface Unit, which is a local controller that coordinates operations and process control for SVG's track equipment. The software package allows semiconductor manufacturers to install and test the communication capabilities of the track equipment without requiring a fully operational host system in the fab.

The surveyed equipment vendors that have implemented or are currently developing the SECS protocol for their equipment were asked to identify the companies with whom they have tested their protocol. These companies

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include the major CIM manufacturers such as Consilium, Hewlett-Packard, PROMIS Systems, and Sentry/Schlumberger. (Note: Hewlett-Packard and Sentry/Schlumberger have recently chosen to exit the computer-integrated manufacturing market. HP is still active in the custom software market in Japan and the Far East, but chose not to fund major software rewrites for its CIM systems operational in Europe and the United States. Sentry/Schlumberger was not able to successfully commercially market their system.) Responses from equipment vendors also included testing of the protocol at beta sites with semiconductor manufacturers, as well as with a SECS emulator and with an in-house testing program.

Typically, a test of a SECS protocol implementation would include a direct or remote hookup to a host (or host-emulator) system that is capable of generating and responding to the basic message transmission and reception. Table 10 summarizes the vendor responses for testing of SECS protocol implementation. For the 39 equipment models in the survey for which a SECS protocol has been implemented or is being developed, some type of protocol testing program has been undertaken for 27 models of equipment. In several cases, multiple responses were given for a single equipment model and are included in Table 10.

Table 10

SECS PROTOCOL TEST PARTNERS

Test Source	Responses	Percent Responses
Consilium	14	30%
I.P. Sharp	9	19
Hewlett-Packard	6	13
Sentry/Schlumberger	2	4
Beta Site Test	11	23
In-House Test	3	6
SECS Emulator	2	4
Total	47	99%

Source: DATAQUEST
April 1986

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Equipment Communications

EQUIPMENT-SPECIFIC INTERFACES

CIM manufacturers are responsible for the development of software equipment interfaces that allow a vendor's equipment to communicate with other computers linked by the factory automation network. The equipment-specific interface is dependent on the equipment vendor's interpretation of the SECS protocol. If the protocol changes, then the equipment interface must also change to reflect the software update. When an equipment manufacturer has to customize his SECS protocol for different semiconductor manufacturers, any equipment interfaces that have been developed by CIM manufacturers for that equipment model will also have to be modified. While the SECS II message sets can vary considerably from vendor to vendor, there is no fundamental problem in developing an equipment interface as long as the functional components of the protocol are present, such as recipe management, process and equipment status, and alarm information. However, the time and cost for equipment interface development could be reduced if vendor implementation of the protocol were not so diverse. The choice for interface development by a CIM manufacturer is driven by semiconductor customer needs.

Table 11 summarizes the total number of different types of equipment interfaces, by equipment category, that have been developed by Consilium, Hewlett-Packard, and PROMIS Systems. These three companies are the major CIM manufacturers that currently supply or have supplied software systems to the semiconductor industry. For every model of equipment, even within the same general category such as diffusion equipment, a unique interface must be developed by each of the different CIM manufacturers. The interface acts as an interpreter between the equipment and a given CIM software system to ensure that the host understands the set of equipment messages (both specified and custom) that are generated.

In several cases, equipment interfaces for the same model of equipment have been developed by the different CIM manufacturers. Table 11 includes multiple counting when several CIM manufacturers have developed an interface for the same model of equipment. Table 11 does not contain the total number of equipment interfaces that are operating on equipment in the installed base; rather, the numbers reflect only the number of different equipment models for which an interface has been developed. The number of interfaces currently under development for other models of equipment are indicated in parentheses. Metrology tools, parametric testers, and AGVs (automatic guided vehicles for material transport) have been included in Table 11.

The number of equipment interfaces presented in Table 11 focuses on equipment supplied by U.S. manufacturers. Hewlett-Packard has also developed equipment interfaces for more than 20 models of equipment for Japanese customers across the full spectrum of front-end processing equipment.

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Table 11

EQUIPMENT-SPECIFIC INTERFACES
BY EQUIPMENT CATEGORY

Equipment Category	Number of Interfaces
Diffusion	9 (1)
Dry Etch	1 (2)
Epitaxy	1 (1)
Ion Implantation	3 (2)
Lithography	0 (2)
Sputtering	1
Wafer Clean Station	1
Metrology	17
Parametric	2
AGV	2 (1)
Total	37 (9)

Note: Numbers in parentheses indicate the number of interfaces currently under development in a given equipment category.

Source: DATAQUEST
April 1986

Cameo Systems and CTX International offer equipment interfaces that focus on metrology and test equipment. Isitec Corporation offers equipment interfaces for wafer fabrication equipment, metrology tools, test, and assembly equipment for which no SECS protocol has been developed. Many semiconductor manufacturers have chosen to implement automation in their facilities in the front-end test and measurement areas first because of the data-intensive nature of the equipment. Short-term payback is achieved through efficient data collection, reduction, analysis, and archiving, which can be greatly simplified with the installation and implementation of a CIM automation package.

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OPERATOR INTERFACE

While the previous discussion has focused on the protocol issues of equipment automation, it is also important to evaluate what level of operator interface and interaction is still required for equipment operation in today's version of an automated manufacturing environment. As part of the survey, equipment manufacturers were asked to identify the current level of operator interactions with processing equipment in three areas: operator input capability at the equipment, process parameter setup once the recipe has been received, and process initiation.

Operator Input Capability at the Equipment

Lot tracking is an important component of an integrated manufacturing system. DATAQUEST asked equipment vendors to indicate whether their equipment currently can accept the input of a lot identification number from an operator at the equipment. In an automated facility, there are several scenarios for entering the lot ID number into the host system and for subsequent verification of lot arrival and departure from the various processing stages. These include bar code readers as well as direct operator input at a keyboard that is part of processing equipment or at a workstation within the manufacturing cell. In addition, there is still the alternative of the traditional lot traveler that accompanies each lot through the processing sequence.

Several semiconductor manufacturers have indicated that they would like to see processing equipment capable of transferring lot ID information to the host system for verification rather than have the full burden fall on the host system to inform the equipment which lot should be arriving next for processing. This verification of lot ID at the equipment before and after processing would minimize potentially costly mistakes that might arise during the early stages of implementing a CIM system on the shop floor.

Table 12 summarizes the vendor responses categorized into four areas: equipment can accept lot ID from operator input and host download (via a SECS link); equipment can accept ID from host download only; equipment can accept ID from operator only; and equipment has no lot ID input capability. In the survey, for 18 of 42 equipment models, the equipment can receive lot ID input from the operator as well as from the host system, while an additional 21 models of equipment surveyed can receive lot ID information only from a host system. In one survey response, the equipment can accept a lot ID only from operator input at the equipment, and for two models of equipment, there is no access to the lot identification.

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Table 12

LOT ID INPUT AT THE EQUIPMENT

Equipment Category	Operator Input/ Host Download	Host Download	Operator Input	No Input
CVD	1	3	0	0
Diffusion/Anneal	3	3	0	0
Dry Etch	2	7	0	0
Epitaxy	1	1	0	1
Ion Implantation	3	0	0	0
Lithography	4	1	1	0
Sputtering	2	2	0	0
Track	2	4	0	1
Total	18	21	1	2
Percent Responses	43%	50%	2%	5%

Source: DATAQUEST
April 1986

The methods of current operator input include keyboard and terminal that are part of the equipment (16 equipment models), alphanumeric touch screen (2 equipment models), and a light pen at an alphanumeric screen on the equipment (1 equipment model). In three cases, survey respondents indicated that bar code readers were being considered for next-generation equipment.

Less than half of the equipment models that were surveyed have the capability for operator input of a lot ID. This means that for some equipment that might be installed in an island of automation on the factory floor, some method of alternative lot ID verification would need to be established. In the absence of operators, advanced automated manufacturing fabs will include material logging systems such as automatic bar code readers directly at the equipment or at adjacent workstations under robotic control. As an interim measure in the transition to a "peopleless" fab, operator workstations and terminals throughout the fab may be logical points for material logging. DATAQUEST believes that processing equipment that provides operator input capability directly at the equipment offers semiconductor manufacturers a flexible alternative for lot ID verification. Processing equipment that provides such features and thus eases the transition to automation will receive special attention from semiconductor manufacturers.

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Parameter Setup

An important and necessary step in an automated processing environment is the ability of equipment to accept a recipe download from the host system, to institute an automatic parameter setup, and to initiate the processing sequence. Table 13 addresses the issue of parameter setup that occurs after a recipe download or operator input has been received by the equipment, and includes setting and verifying parameters such as temperature, pressure set points, and alignment settings. Of the 42 models of equipment surveyed, 39 have the capability of accepting a recipe download via the SECS protocol. For the other 3 equipment models for which no SECS protocol has yet been developed, the only methods for current recipe input are either through direct operator input at the equipment, or by operator selection from a menu of recipes stored at the equipment.

Equipment manufacturers were asked to indicate whether their equipment initiates automatic parameter setup prior to process initiation or whether operator interaction with the equipment is necessary once the recipe has been received by the equipment. Some vendors responded that parameter setup responsibility is divided between operator and equipment, as noted in Table 13. In the survey, 35 of 42 equipment models can implement parameter setup with no operator interactions. DATAQUEST believes that fully automatic parameter setup is an essential component of equipment operation in an automated fab.

Table 13

PARAMETER SETUP

Equipment Category	Equipment	Operator	Equipment/ Operator
CVD	4	0	0
Diffusion/Anneal	6	0	0
Dry Etch	9	0	0
Epitaxy	2	1	0
Ion Implantation	1	1	1
Lithography	4	1	1
Sputter	3	0	1
Track	6	1	0
Total	35	4	3
Percent Responses	83%	10%	7%

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Process Initiation

One final area of operator interaction with the equipment is in the area of process initiation. Vendors were asked to indicate whether the equipment or an upstream host system can initiate the process or whether an operator is required to "push the start button." As shown in Table 14, vendor responses indicate that there is essentially a 50-50 mix with regard to process initiation responsibility.

DATAQUEST believes that the current level of operator interaction with equipment must be reduced further in order to provide processing capability in a fully automated environment. Equipment that can operate solely on the basis of equipment/host transactions will be judged as that most suitable for operation in an automated facility. While manufacturers are making the transition to a "peopleless" processing environment, equipment that can accept a lot ID input from an operator provides a useful alternative for lot ID verification with host expectations. Semiconductor manufacturers are evaluating processing equipment today on the basis of such criteria as present and future automation strategies are being developed in the industry. DATAQUEST encourages equipment manufacturers to continue to focus on these issues as well as on increased equipment reliability, for which the level of operator interactions and assists also must be minimized in order to achieve manufacturing goals in an automated semiconductor fabrication facility.

Table 14

PROCESS INITIATION

Equipment Category	Equipment	Operator	Not Available
CVD	3	0	1
Diffusion/Anneal	4	2	0
Dry Etch	6	3	0
Epitaxy	1	2	0
Ion Implantation	1	2	0
Lithography	0	6	0
Sputtering	2	2	0
Track	5	2	0
Total	22	19	1
Percent Responses	52%	45%	3%

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Equipment Communications

DATAQUEST ANALYSIS

DATAQUEST believes that equipment-host communications is a critical component in the automated manufacturing environment. Our current evaluation of this topic concludes that:

- The SECS protocol has been accepted as the industry standard for communications.
- While MAP may have a future in the semiconductor industry, it will not replace SECS at the equipment level.
- The opportunity exists for equipment manufacturers to gain a strategic market advantage with active participation in SECS protocol development.
- Equipment protocol implementation should not be a proprietary issue.
- DATAQUEST strongly encourages IC manufacturers to establish a clear consensus on SECS protocol specifications.

The SECS protocol clearly has been established as the standard for communications in the U.S. semiconductor industry. European and Japanese semiconductor manufacturers are also adopting the protocol in their facilities. To assist in the distribution of information on the protocol, the SEMI Communications Subcommittee has made presentations in Japan and the SECS protocol document has recently been translated into Japanese. Japanese equipment and computer manufacturers are contributing to protocol modifications and development through JEIDA (the Japan Electronic Industry Development Association) in order to achieve standardization of the SECS protocol.

The majority of semiconductor manufacturers involved in advanced device fabrication now require SECS compatibility for new equipment purchases. However, many offer little else for guidance. Equipment vendors have commented that most semiconductor manufacturers do not seem to know what they want with regard to automation or in the specifications of a SECS II message set. Many equipment vendors are thus faced with the prospect of developing a SECS protocol that will require special customization when the equipment is finally installed in an automated environment at a given semiconductor manufacturer's facility.

Clearly, there is a need for semiconductor and equipment manufacturers to establish a common framework for protocol implementation in order to remove the confusion surrounding the protocol and lower the software development costs of manufacturers. DATAQUEST believes that

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semiconductor manufacturers involved in the automation effort need to take the first step and establish a clear consensus on what they feel is necessary for SECS protocol implementation by equipment manufacturers.

It has been suggested that a SECS Users Group for IC manufacturers be organized as a forum for identifying protocol and automation needs from a manufacturing perspective. In particular, the SECS Users Group would identify protocol specifications for specific equipment categories. Equipment manufacturers would participate in the SECS Users Group and provide their current protocol documentation as an aid in evaluating the status of protocol implementation. Some equipment manufacturers, however, regard their protocol implementation as confidential information. Semiconductor processing equipment should not be competing on the basis of protocol implementation but rather on equipment design and special features.

CIM manufacturer involvement with a SECS Users Group is also very important because the development and implementation of a CIM software package is the critical link between the equipment and the manufacturing elements of the fab. The time and cost for linking equipment to a CIM system in a semiconductor fab would be reduced considerably if the implementation of a SECS protocol offered a standardized procedure for interactive communications.

DATAQUEST believes that equipment manufacturers that actively participate in the development of the SECS protocol and the formulation of protocol specifications for their specific equipment categories will gain a strategic market advantage in providing equipment to the semiconductor industry. Equipment manufacturers have the opportunity to participate in the formative stages of automation in the semiconductor industry, and in the process can establish firm relationships with the automation leaders. Semiconductor manufacturers that are not yet active in the automation arena will evaluate future equipment purchases not only on equipment performance, but also on equipment manufacturers' proven automation experience and protocol acceptance.

The potential for incorporating the MAP protocol into the automation networks of semiconductor manufacturing facilities is still under evaluation. SECS, however, is the protocol that manufacturers are specifying today. DATAQUEST believes that the SECS protocol, in one form or another, will survive the transition to any MAP-based system in the future. Regardless of which protocol is employed, the need for better communication between equipment, semiconductor, and CIM manufacturers mirrors the automation goal itself: to develop reliable, interactive communications between the various components in an integrated, automated, manufacturing environment.

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APPENDIX A

THE NETWORK ENVIRONMENT: AN OVERVIEW

Introduction

The focus of the development of a computer integrated manufacturing (CIM) environment is to tie together all sources of information and production on the shop floor. The infrastructure that describes such a system is a communication network, typically a local area network that provides reliable, medium-to-high speed, interactive communications between various computing devices and processing equipment. A local area network, by definition, is located within a limited geographical area, typically within a single building or adjacent facilities.

Network Components

A communications network can be characterized by several different components, including the physical medium used for data transmission, the type of data transmission employed, the configuration or topology of the network, and, finally, the data link (or access method) by which communication devices gain use of the network's physical medium. The communications protocol is an important component in ensuring operational consistency and compatibility among the variety of computers and equipment operating in a network environment. The following sections review the network components that are supported by the SECS and MAP protocols.

Physical Medium/Data Transmission

In the SECS protocol, electrical connections between equipment and computers utilize the international standard known in the United States as EIA RS-232-C (or, more simply, RS-232) for connector and voltage levels. RS-232 is a mature standard and the familiar 25-pin, "D"-shaped connector can be found on almost every type of computer today. While RS-232 uses the 25-pin connector, the SECS protocol specifies bit serial data transmission along only a single wire (plus a ground); one wire is used for transmission in one direction and a second wire for the reverse direction. The SECS protocol, therefore, uses only a total of three signal wires (plus frame ground) for transmitting data and only one flow of information is allowed at any one time (half-duplex transmission).

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Equipment Communications

SECS I also specifies that equipment will provide power on two additional pins for external line-drivers for the purpose of extending the cable length. The RS-232 connector also has several additional pins that are useful for testing purposes but are not specified by the SECS protocol. Since some computer systems may require that these pins be active, appropriate signals will have to be locally generated by the equipment for those systems.

In the SECS protocol, the data transmission rate is limited to 9,600, 4,800, 2,400, 1,200, 300 or 150 baud (characters per second), with a high-speed option of 19,200 baud also available with modification. The preferred data transfer rate of 9,600 baud is considered sufficient for most equipment-to-host communications; however, speed can be a problem when data-intensive measuring equipment communicates with a host system. For that reason, some level of data reduction is usually required before uploading information to the host, so as not to "tie up" the lines for too long a period of time.

The MAP protocol specifies broadband coaxial cable as the physical medium for the network. Broadband coaxial cable is a shared medium that consists of multiple independent channels. Broadband transmission uses CATV technology (Community Antenna TeleVision, more commonly known as CAble TeleVision), which is characterized by a wide bandwidth that uses frequency division multiplexing to establish multiple channels. It has a high data bandwidth, typically 400 MHz, with 5 to 10 MHz per channel. Broadband coaxial cable can also support a closed circuit television system and voice telephone in addition to providing the physical communications medium for digital transmission in a local area network. One additional advantage of broadband coaxial cable is that it can be installed over distances of up to 10 kilometers; longer distances can be achieved with the installation of repeaters. Its primary disadvantages are the cost and complexity of installation. Broadband coaxial cable is very cumbersome to work with and, in addition, each tap to the network requires a modem.

Since baseband transmission is often mentioned in context with broadband, it is useful to understand the difference between these two types of transmission that are used in an automated factory environment. Baseband transmission (not supported by MAP or SECS) specifically employs bit serial digital transmission in which a variety of coding techniques are used that rely on time division multiplexing. When each communications device transmits on a baseband system, it makes use of the entire bandwidth of the channel, typically 5 MHz. Baseband coaxial cable technology is well understood. It is a low-cost, easy-to-install cable. However, its disadvantages are that it is a single channel system and can only be applied over a limited distance on the order of 3 kilometers.

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Equipment Communications

Topology

A network topology or configuration is the geometric arrangement of computing devices, or nodes, and the physical media links that make up the network. A node may be defined as a communication system connection point, and is typically represented by either a controller or a computer. The network configurations that will be discussed here include the point-to-point hierarchical structure, as well as the ring and bus network topologies. Figure A-1 shows schematic representations of the three general types of geometrical configurations that have been implemented in automated network environments.

The SECS standard supports a point-to-point configuration or topology in which a single communication line links two stations that each have the capability to initiate a conversation. The point-to-point configuration may be extended into a more complex topology known as the tree or hierarchical configuration. In the hierarchical configuration, a host system is resident at the uppermost level, with an intermediate level of communication devices (node computers) installed between the host and the equipment-level computer systems. The tree configuration is a particularly useful topology for SECS as the SECS message header contains information that indicates the direction of information flow (i.e., "up" or "down" the tree).

The ring topology, while not used in the semiconductor industry, can be found in other communication networks. In the simple ring configuration illustrated in Figure A-1, each communication node is connected to exactly two other nodes. Data that travels through the ring must go through each station in its path between the original source and final destination of the message. The simplicity of the design provides that no routing decisions must be made; however, the system has predictable timing delays because of the geometrical arrangement. One major disadvantage of the ring configuration is that a failure in any one device on the ring can have a global effect on the system unless relay shunts are provided around each device. The SECS and MAP protocols do not support the ring topology.

In the bus configuration, each node in the system is connected to a central transmission line. The transmission line or bus is passive so that in the event that a node communications device fails, the bus still remains operative. However, because of the arrangement of a bus configuration, specific protocols must be established to deal with which communications device has the control of the network at any given time. The MAP protocol employs a bus topology.

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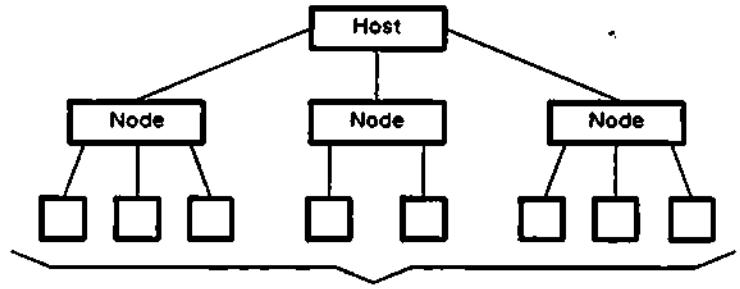
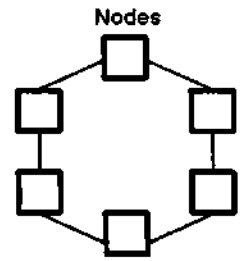
Figure A-1

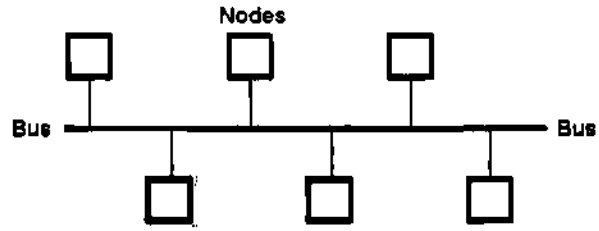
SCHEMATIC REPRESENTATIONS OF NETWORK TOPOLOGIES



Point-to-Point Topology
(Hierarchical)



Ring Topology



Bus Topology

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Access Method

The access method by which a communication device obtains use of a network's physical medium is part of the the overall data link control of a given communications protocol. The data link establishes the direction of transmission, verifies proper data link status, and resolves contention when more than one device attempts to transmit at the same time.

The data link protocol in SECS I is the procedure used by the serial line to establish the direction of communication between the equipment and a host computer. As mentioned previously, transmission between host and equipment under the SECS protocol is half-duplex, so that essentially only one party is allowed to talk at any one time. When both ends of the line attempt to communicate at the same time, it results in a line contention or a "collision." Collisions are resolved in the SECS protocol by the specification of one station as the master and the other end of the link as the slave. In the event of a collision, the slave postpones transmission and yields to the master. The SECS I protocol also provides a series of timeouts and retries that are used to correct communication errors.

In a semiconductor processing environment, the equipment typically is designated as the master and the node or host computer as the slave. This initially may seem contrary to the hierarchical topology that is supported by the SECS protocol, but since the equipment computer usually has limited storage capability for messages, it must be allowed to send any messages it has before receiving new requests for information from the host system.

Polling can be described as a controlled media access method. It requires a master/slave relationship among the communication nodes in the system. The master computer typically controls the link and initiates all communications within the system. All other devices on the network, designated as slaves, respond only when polled by the master for information.

Token passing is a shared media access method. In this type of configuration, the "token" or special message is passed around the network in a prescribed manner. The station that holds the token is given exclusive but temporary control of the network to transmit information. All other stations in the network can only listen when the token is not in their possession. Ring and bus topologies typically employ a token passing access method. The MAP protocol, in particular, utilizes token passing as the access method in its bus network.

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The carrier sense multiple access/collision detection (CSMA/CD) access method can be simply described as a system in which a station listens before talking and listens while talking. It is important that before transmitting information, each communications device first listens to the network to see if the media is occupied or idle. When access has been gained to the physical media and transmission has begun, each device also listens for a collision--someone else in the network trying to gain access to the system. If a collision occurs, each station backs off the network for a prescribed and unique period of time in order to prevent another collision. Ethernet, a local area network developed by Xerox, utilizes the CSMA/CD access method.

Both the polling and token passing access methods avoid the issue of contention by their very design. The CSMA/CD access method is similar to that specified in the SECS protocol since both have mechanisms to deal with line contention. However, the difference between these two methods is that in the SECS protocol, contention is resolved by the slave yielding to the master, while in CSMA/CD, both stations back off the network for a prescribed and unique period of time in order to prevent another collision.

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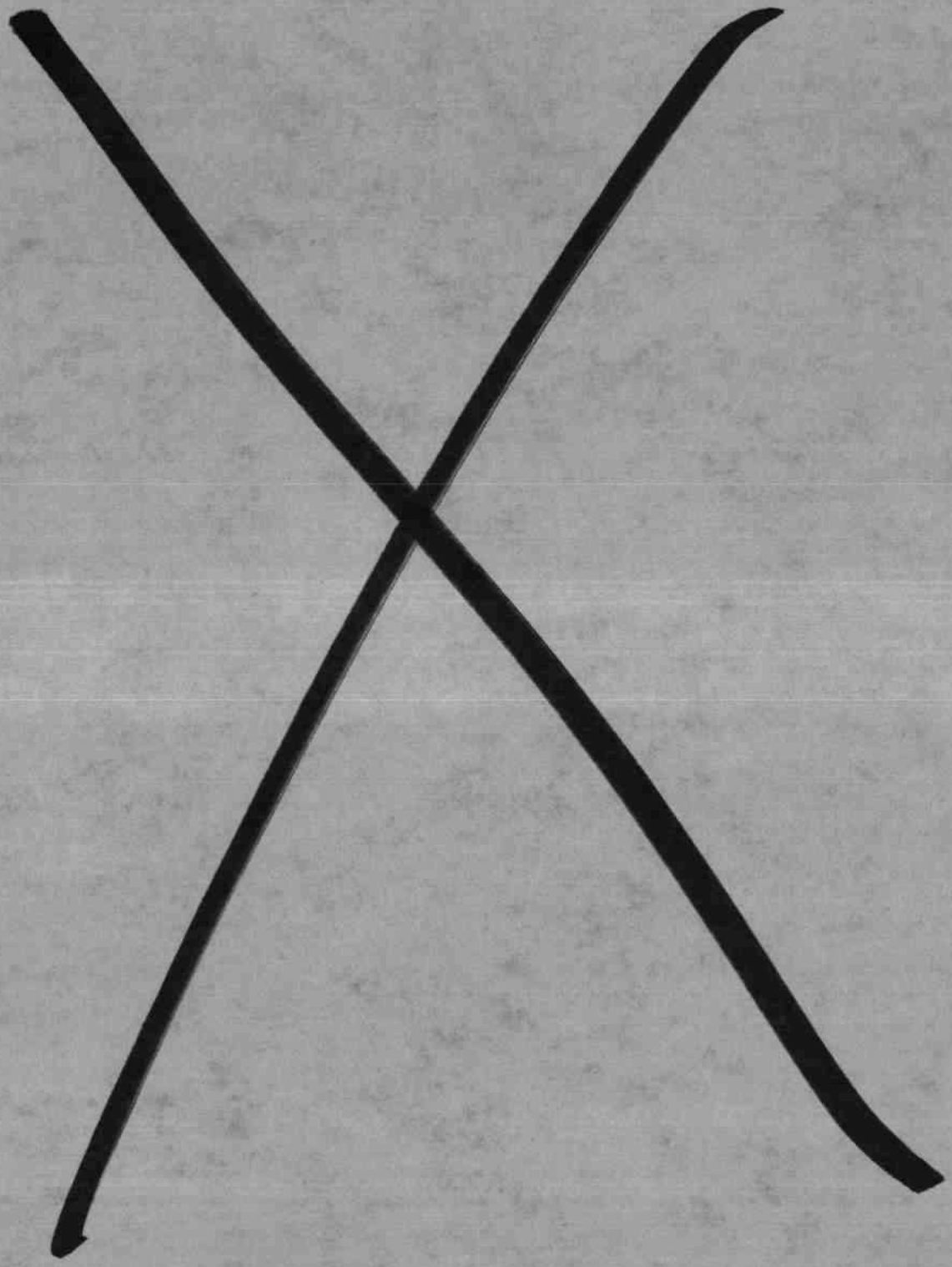
Process Control

The following is a list of the material in this section:

- CDE and Wafer Inspection Equipment Markets



Semiconductor Materials

The following is a list of the material in this section:

- Silicon History
- Silicon Technology
- Silicon Data Base
- Silicon Forecast
- Silicon and Epitaxial Wafer Companies
- Semiconductor Gases--Products and Applications
- Semiconductor Gas Companies
- Photoresist

For additional information, please refer to the material behind the Semiconductor Materials tab in your Newsletter binder.

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Silicon History

INTRODUCTION

Since the invention of the transistor at Bell Labs in 1949 by William Shockley, Walter Brattain, and John Bardeen, it has been understood that device performance is intimately affected by the substrate material. During the early 1950s, the first devices were produced on germanium. Between then and now, many other materials have been used for semiconductor processing. Gallium arsenide (GaAs) offers the advantages of speed and ability to withstand high processing temperatures. Silicon-on-sapphire (SOS) offers the advantage of high speed. Gallium-gandolium-garnet (GGG) has become the preferred material for bubble memory applications. However, in spite of all this, the preferred material for semiconductor processing today is still silicon.

SILICON VERSUS GERMANIUM

In the early years of semiconductor device manufacturing technology, silicon was hard to process but had better operating characteristics above 50 degrees Centigrade (C) than germanium. However, germanium was readily available in a pure form and easy to work. Germanium became the accepted production material in the rapidly growing semiconductor market of the 1950s. The mesa transistor, grown on germanium and developed at Texas Instruments in 1957, was by far the most widely used semiconductor device. It was made possible by William Pfann's discovery of a method for alloying impurities into the substrate, thus making batch processing possible.

In 1960, Jean Hoerni of Fairchild succeeded in developing the planar process on silicon. This process was the first move away from semiconductor manufacture using alloyed junctions common with germanium as a substrate to the use of diffused junctions. In the planar process, impurities were masked by the oxide layer and diffused under high temperature into the substrate where the oxide had been removed. This process both passivated the silicon after processing and allowed metal interconnections to be built up on the insulating oxide surface. Since germanium developed thermal problems above operating temperatures of 50 degrees C, silicon's temperature characteristics became a winning advantage. Furthermore, germanium oxide did not provide a good barrier to diffusion, and silicon oxide did. Consequently, the development of planar processing was the death knell for germanium.

In spite of silicon's advantages when used with planar processing, widespread use of silicon was retarded for a time by germanium's price advantage. Germanium mesa transistors were high on the learning curve, and the availability of polished silicon wafers was low. From 1959 to 1960, germanium devices dropped from an average selling price (ASP) of $1.96 to 57 cents. During the same period, silicon transistors dropped

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from an ASP of $14.00 to $1.46. The relative price drop of silicon was greater as production volumes increased, and silicon came up the learning curve. However, regardless of their superior performance, silicon devices were still more costly than germanium. In 1963, General Electric's development of inexpensive plastic packaging for silicon transistors, coupled with the dissemination of planar processing methods, provided the final push to bring silicon transistor ASPs down to a competitive level with germanium. Silicon ASPs dropped from $1.45 in 1964 to 86 cents in 1965, and the total market for silicon devices surpassed that of germanium.

PRODUCTION

Polycrystalline Silicon Production

Silicon, unlike germanium, is not a naturally occurring element. Pure silicon is produced chemically in the form of polycrystalline silicon (polysilicon), so-called because the silicon produced is in the form of many small crystals. The polysilicon is then reprocessed into large, single-crystal ingots from which silicon wafers are sliced for use by the semiconductor industry.

During the 1950s, a variety of poly production processes were under development. Bell Labs made polysilicon through a process of hydrogen reduction of silicon tetrachloride on a resistively heated tantalum rod.

Siemens developed a method for depositing polysilicon on silicon through the hydrogen reduction of trichlorosilane gas on a resistively heated silicon rod. Siemens chose to license its poly production process rather than enter the business; it had arrangements with Dow Corning, Merck Chemical, Monsanto, Montecassini, Shin-Etsu, Wacker, and Westinghouse. Today, most suppliers use the Siemens process.

Texas Instruments (TI) developed a process through the hydrogen reduction of silicon tetrabromide and later went on to use trichlorosilane. In 1957, TI built a poly production facility that used trichlorosilane; it has been manufacturing the bulk of the silicon used in its semiconductor production ever since.

Poly production processes were also under development at ITT Standard Laboratories in London, at Mallinckrodt, at Trancoa (a subsidiary of Transitron), and at Union Carbide. Union Carbide began supplying TI with high-grade trichlorosilane for poly production in 1954 and has remained a major supplier of semiconductor grade gases to date. In 1956, Union Carbide built a small poly plant in Parma, Ohio. It did not expand, however, and the Parma plant was shut down in 1963.

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Silicon History

While a number of poly production processes were under development, it was unclear which would become the process of choice and which suppliers were to become major forces in the market. In 1956, Du Pont was the only U.S. company selling polysilicon for single-crystal semiconductor silicon production. The company went into production at its Brevard, North Carolina, plant in 1957. Du Pont's zinc reduction process required extra steps to obtain the purity required, and production costs were higher than for the Siemens process. However, most of the suppliers at that time used Du Pont's process.

In 1958, Merck Chemical obtained a license from Siemens and built a poly plant in Danville, Connecticut, with piping and base plates made of silver or silver-lined materials. Coming from a background in the pharmaceuticals business, Merck focused on cleanliness and high purity. Merck and Du Pont were the leading suppliers of polysilicon during the late 1950s.

Dow Corning built its first poly plant in 1960, using the Siemens process; riding on the strong growth of the market in the early 1960s, the company successfully expanded operations. In 1963, Dow cut its poly prices by 10 to 25 percent. At that time, Du Pont announced that it was discontinuing its silicon business, citing excess silicon production capacity in the industry as a major factor. Merck, hampered by high production costs relative to other suppliers and by a marketing focus that was still primarily directed to the pharmaceuticals business rather than the semiconductor business, closed its poly operations in 1965. Dow Corning became the leading poly supplier. In 1979, Dow's poly plant in Hemlock, Michigan, was converted into a subsidiary, Hemlock Semiconductor Corporation.

Meanwhile, in Germany, Wacker obtained the Siemens license in 1956 and built a pilot production plant in Burghausen, West Germany. By 1959, Wacker had a poly production plant and was selling worldwide. In less than 10 years, Wacker became the second largest supplier after Dow Corning in poly production and was second to Monsanto in silicon wafer production. The company bought Monosilicon, Inc., from Alloys Unlimited for U.S.-based poly production. After 10 years of operation, Wacker closed this plant in 1977 and built a new poly facility in Portland, Oregon.

In 1974, Applied Materials and Fairchild formed a joint venture to build a poly plant for Fairchild's internal silicon production. This company, which was called Great Western Silicon, used the Siemens process. The plant was completed in 1978, with a 100-ton capacity. It was subsequently sold to General Electric in 1980, after expanding to a 150-ton capacity. General Electric sold Great Western to Nippon Kokan in 1985.

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Silicon History

Motorola had built a poly production plant with a capacity of 10 tons to augment its in-house wafer production. This plant was later expanded to a capacity of 30 tons. In 1969, the company built a second poly plant.

Silicon Wafer Production

As with polysilicon production, widespread research and development efforts at a variety of companies produced the technological developments necessary for production of single-crystal silicon.

Two major processes for the conversion of polysilicon into single-crystal silicon were developed. They are the float zone (Fz) and the Czolchralski (Cz) techniques. Fz was developed in 1949 at Bell Labs by Gordon Teal and John Little for use with germanium. Bell licensed this technology to Merck, Monsanto, Montecassini, SEH, and others. Siemens also developed an Fz process. Mr. Teal later developed a silicon wafer puller based on the Czolchralski technique while he was at Texas Instruments.

During the early years of the industry, many semiconductor manufacturers were producing single-crystal silicon in-house from poly produced by the previously mentioned manufacturers. In 1960, Motorola began production of high-quality silicon wafers. It also developed an epitaxial reactor with features that were to be used in other designs throughout the world.

Delco (a subsidiary of General Motors) started silicon operations in 1961 and was in full production by 1964. Delco had the first automated wafer-pulling operation in 1975.

The first merchant silicon wafer production company on record was Knapic Electro Physics, started by Dean Knapic of Shockley in 1957. Knapic was in production until 1963. During the 1960s, there were an estimated 35 companies producing silicon wafers.

When Merck Chemical entered the silicon business in 1958, it licensed both the Siemens poly and Fz processes. The company manufactured its own poly and converted it into single-crystal silicon, which sold for $1,000 a kilogram. Until Merck left the market in 1965, as discussed previously, it was a major supplier of Fz and Cz single-crystal silicon wafers, as well as wafers with epitaxial layers.

Monsanto was making Fz silicon wafers at the end of the 1950s. In the early 1960s, Monsanto had set up a Cz silicon manufacturing operation at its research center in Saint Peters, Missouri.

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Silicon History

In addition to supplying poly, Dow Corning produced Fz wafers. In 1967, Dow formed a joint venture with SEH of Japan for production of Czolchralski-grown wafers, which Dow sold in the United States. Dow soon left the FZ market, confining its wafer business to the Japanese-made Cz wafers. The joint venture with SEH was dissolved in 1979, and, as mentioned, Dow's poly plant in Hemlock, Michigan, was converted into a subsidiary, Hemlock Semiconductor Corporation. After the dissolution of the venture, SEH continued to sell both Fz and Cz wafers to the U.S. market. In the 1980s, the company's subsidiary, SEH America, built a large wafer production facility in Washington State.

In 1960, Robert Lorenzini of Rheem Semiconductor, a spinoff from Fairchild, made the first production-scale Cz crystal puller. Lorenzini went on to found Siltec in 1968. The company came out with the first 3-inch crystal puller at a time when the majority of wafer production was of 3/4- to 2-inch wafers. The company also developed the first automatic diameter control and became the third or fourth leading supplier of wafers. It has since fallen to seventh in the world among merchant wafer suppliers. To this day, Siltec is a supplier of wafer-pulling equipment.

In the mid-1970s, Montecassini and Edison in Italy merged to form Montedison. The Montedison venture was designed to revive Montecassini's dormant silicon business. It formed a company called Smiel, which was sold to the West German company Dynamit Nobel in 1980. Dynamit Nobel has since become the eighth leading supplier of poly and the sixth leading supplier of wafers among the merchant silicon suppliers.

In the 1960s, there were approximately 35 suppliers of polished wafers worldwide. Many dropped out of the business, or were sold to other companies during that time period. One such company was California-based Galamar, which started producing wafers in 1959 and was sold to Applied Materials in 1963. Other companies include General Instrument, Grace Chemical, Monosilicon, Pacific Semiconductor, Silcoa, and Sylvania. Although many semiconductor manufacturers had attempted to produce their own wafers in-house, many also abandoned these efforts during the 1960s, choosing to purchase wafers from merchant silicon suppliers. AT&T (Western Electric), Delco, Fairchild, IBM, Motorola, and TI are the only semiconductor manufacturers that retain internal wafer production today.

The first major shakeout occurred during the 1960s. In 1963, when Dow cut poly prices by 10 to 25 percent, it cut its polished-wafer prices by 40 percent. In the late 1960s and early 1970s, pricing in the silicon wafer business was tentative and often dependent on negotiation of specific contracts.

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In 1975, the second major shakeout occurred when Wacker published a concrete price list for polished wafers. Wacker's wafers were cheaper by a large margin, and this lowering of price was to have an immediate impact on the structure of the silicon manufacturing industry. All of the wafer suppliers were to respond by cutting prices, beginning a volatile pricing environment in which margins were strained. Majority supplier Monsanto lost market share and retaliated by further cutting prices below those of Wacker. The prolonged price war was a contributing factor in the dissolution of companies such as Galamar and in the withdrawal of General Instrument from the market.

INDUSTRY EXPANSION AND CONTRACTION

As the semiconductor industry hit a period of dramatic growth in the late 1970s, most of the major silicon suppliers laid plans to add capacity beginning in 1980. Silicon suppliers had been operating at capacity during the 1978-1980 semiconductor industry peak, and many suppliers planned expansion programs that would have doubled their capacities. Many of these expansions were postponed as the two-year recession of 1981/1982 dragged on.

The year 1982 was virtually flat for silicon suppliers. Silicon production decreased to 50 to 60 percent of capacity. By mid-1983, production had again increased, reaching 65 percent of capacity as the upturn began to be felt by the silicon suppliers. Revenues increased by approximately 15 percent in 1983 and by 40 percent in 1984.

During 1983, production was at 75 to 80 percent of capacity. Lead times, which are normally about 6 weeks, had stretched out to 12 to 14 weeks. For the first time in four years, there was an industry-wide price increase of approximately 10 percent for all silicon products. In this environment, suppliers began adding capacity at a breakneck pace. (Further discussion of capacity increases as they affect the current market climate are presented in the Markets section.)

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Silicon Technology

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INTRODUCTION

Silicon is the second most abundant element in the earth's crust. It occurs in the form of oxides, or silicates such as silica (sand). In the 1950s, silicon was considered to be one of several materials with semiconductor potential. With the development of planar processing in 1960, polysilicon price reductions, and inexpensive plastic silicon transistor packaging, silicon took the market from germanium as the basic element for the manufacture of semiconductor devices.

Silicon has an easily produced natural oxide that acts as an effective diffusion mask and dielectric layer in the planar processing method devised to build electronic circuits by Jean Hoerni of Fairchild. Silicon oxide mask layers are effectively etched with hydrofluoric acid to form patterns for selective introduction of impurities into the substrate silicon as the device is built up layer by layer.

In the periodic table of elements, silicon falls in Group IV-A, along with carbon, germanium, tin, and lead. In its chemical structure and physical characteristics, silicon falls between metals, which are electrical conductors, and nonmetals or insulators. Hence its designation as a "semiconductor" material. All of the elements in Group IV-A are structured with atoms that have four valence electrons in their outer shells. A positive charge in the nucleus of the atom is balanced by the four negative charges of the electrons in the outer shell, and therefore the atom is in a neutral, nonconductive electrical state.

The crystal structure of silicon is such that the four valence electrons of each atom are shared with adjacent atoms, forming covalent bonds that hold the atoms together in their crystal structure (see Figure 1).

It is this particular crystal lattice structure that provides silicon with its semiconductor properties. While in its pure elemental state, silicon is relatively inert; its crystal structure can be selectively chemically manipulated to form areas with active electrical characteristics.

The process of chemical manipulation of silicon is called "doping." Doping consists of replacing a silicon atom in a specified area of the crystal with atoms of an element that has either three or five valence electrons. If a silicon atom is replaced with an atom that has three valence electrons, such as antimony, an electron deficiency is created (see Figure 2). This deficiency is called a "hole." With its missing electron, the hole provides a potential well in the material that neighboring electrons can move into, thus allowing for a flow of electrical current. Silicon doped in this way, such that the majority current carriers are "holes" (or the absence of electrons), is called a P-type semiconductor material.

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Figure 1

SILICON CRYSTAL LATTICE
(TWO-DIMENSIONAL)

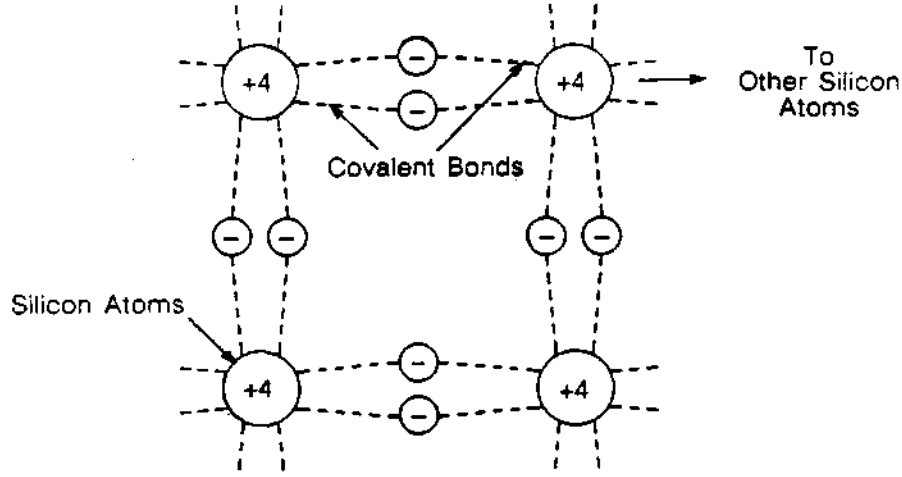
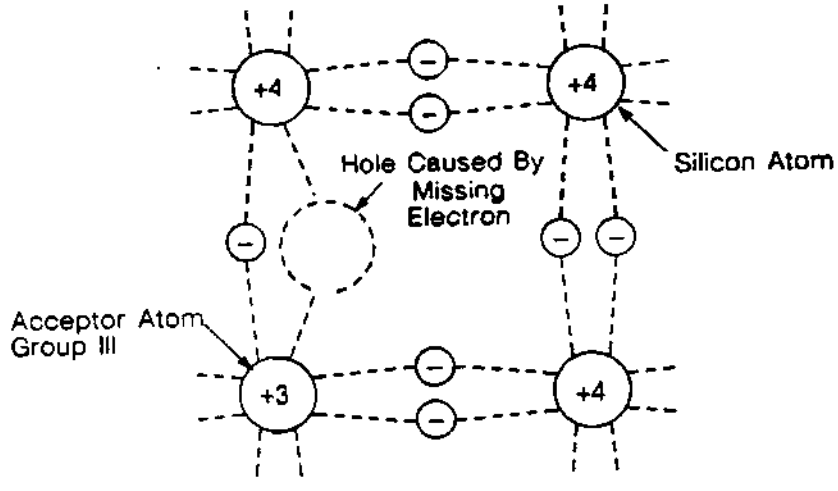


Figure 2

SILICON CRYSTAL LATTICE
ACCEPTOR ATOM OR "HOLE"



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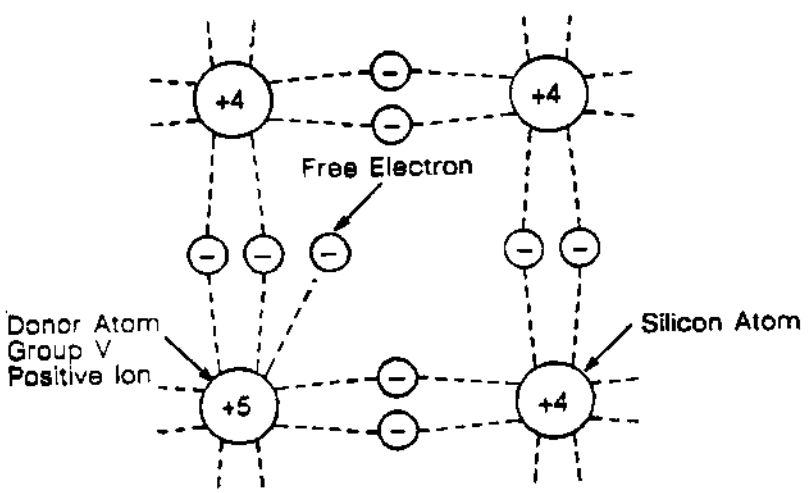
If the silicon lattice is doped with an atom that has five valence electrons, such as phosphorus, this atom is said to be a "donor." It has an extra electron in the lattice that is available for the flow of electrical current (see Figure 3). The oversupply of electrons provides the majority carrier of electronic current, and the silicon is then called N-type material.

Figure 3

SILICON CRYSTAL LATTICE
DONOR ATOM



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Silicon Technology

POLYCRYSTALLINE SILICON

Pure silicon can be obtained through several processes. The Siemens process, developed in 1953, is based on the hydrogen reduction of $SiCl_4$ on a hot silicon rod. Other processes involve the reduction of $SiCl_3$ (trichlorosilane) in a hot quartz tube, and a reduction using $SiBr_4$ as the starting material. The Siemens process is the most widely used today for the production of semiconductor-grade polycrystalline (poly) silicon. These processes form a purified poly, so-called because the silicon produced is in the form of many small crystals.

SINGLE-CRYSTAL SILICON

Poly requires further processing to obtain the single-crystal ingots that are then sliced into wafers for semiconductor production. The two methods in use today for production of single-crystal silicon ingots from poly base material are Floatzone (Fz), and Czochralski (Cz).

Floatzone Crystal Production

Floatzone crystals are grown on a bar of polycrystalline silicon that is suspended vertically inside a furnace chamber filled with an inert gas. A seed crystal of the desired orientation is placed in contact with the lower end of the bar, and is heat-fused to the poly starting material. Fz furnaces employ radio frequency (RF) heating, supplied by movable coils that surround the bar. (See Figure 4.)

The RF heating coils melt a narrow horizontal zone, beginning at the lower end of the poly bar. This melted zone "floats" on the solid silicon on both sides of it; hence the name "floatzone." The RF heating element is then slowly moved upward along the length of the bar, melting the poly rod. As the zone of heating continues along the poly rod, the melted silicon cools and crystallizes into a single ingot matching the orientation of the seed crystal.

In Fz processing, dopants in gaseous form are added to the furnace chamber continuously throughout the melt and recrystallization cycle. Consequently, the uniformity of dopant levels in the resulting crystal ingot have historically been more uniform than those in crystals formed with the Cz process. Recently, however, Cz process technology has developed methods to reduce the dopant uniformity problem.

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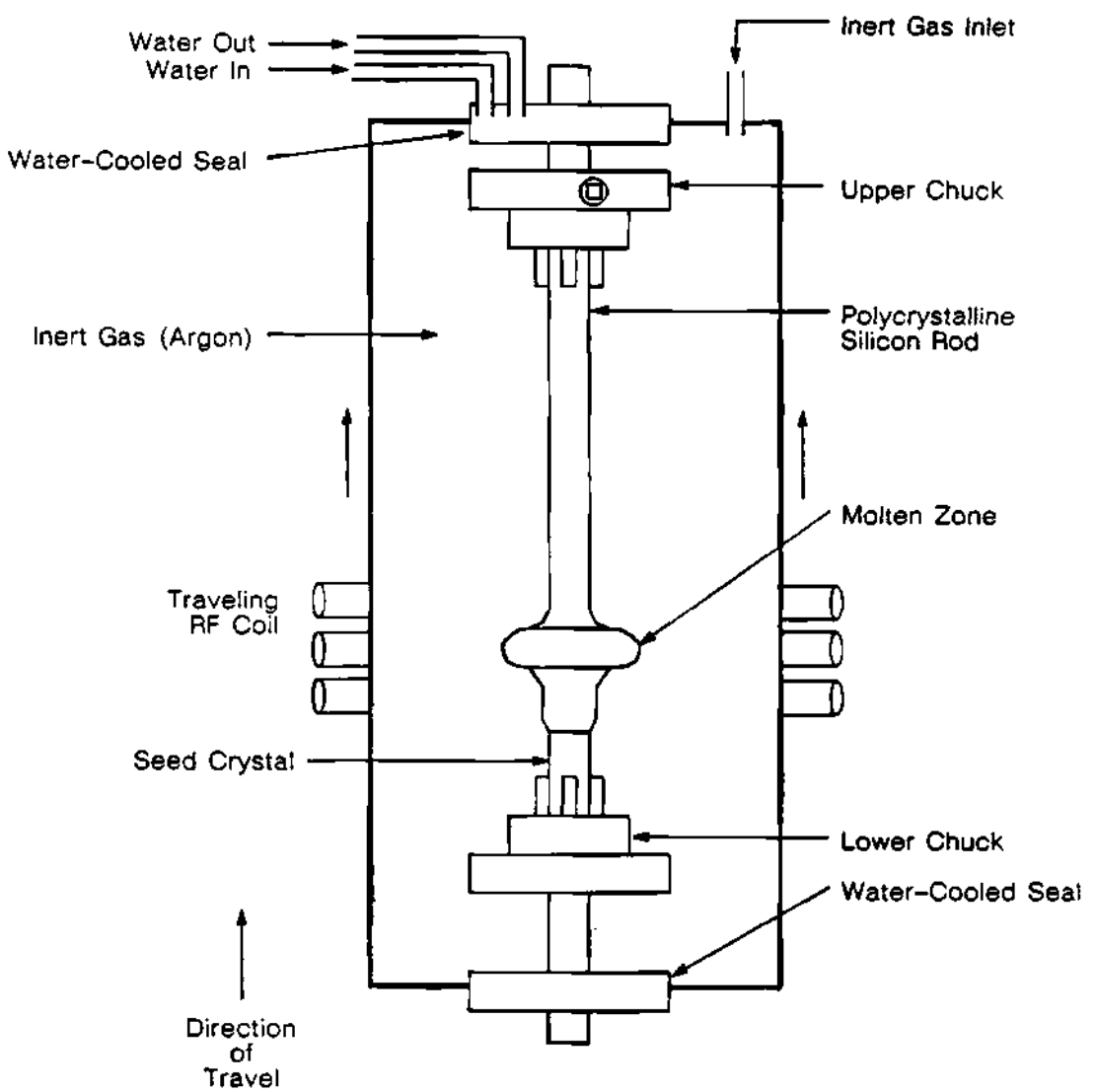
Figure 4

FLOATZONE CRYSTAL-GROWING FURNACE



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Historically, an advantage to the Fz process has been that because no crucible is used, oxygen contamination of the crystallizing silicon is reduced. In the Cz process, oxygen contamination results from the diffusion of oxygen out of the crucible in which the silicon starting material is placed.

Fz crystals have also traditionally been the choice for production of single-crystal silicon with resistivity ratings higher than 30 ohms per centimeter. Fz crystals may still be the choice for producing silicon wafers used in production of discrete devices, where material defect requirements are not as strict as for higher-density ICs.

A disadvantage of silicon production using the Fz technique is its higher cost relative to Cz silicon. This is because the starting material must be in the form of polysilicon rods for Fz processing. Further, as the silicon crystal grows, it is suspended by the seed crystal. The system tends to be mechanically unstable, and is sensitive to vibration. Vibration can cause slippage within the crystal structure due to the plastic nature of the cooling silicon ingot.

Because Fz starting material must be in the form of a bar, it is difficult to produce large-diameter crystals. As the semiconductor industry's demand for large-diameter crystals continues to be a major market factor, the economics of Fz crystal production have caused advances in production technology to lag those of Cz processing technology.

Czochralski Crystal Growing

Cz-grown silicon is the type most widely used in today's semiconductor industry, accounting for an estimated 90 percent of semiconductor-grade silicon.

In this process, poly is melted in a crucible placed inside a furnace. A specified quantity of poly, called a "charge," and the desired dopants, are placed in a quartz crucible. The size of the charge (and the size of the crucible itself) is determined by the diameter of the crystal to be grown. The crucible is placed in the sealed furnace chamber (see Figure 5) and the chamber filled with an inert gas such as argon. The poly is then melted by means of resistance heating.

A silicon seed crystal of the desired crystallographic orientation is suspended on a rotating chuck and lowered into the melted poly. The temperature of the furnace is gradually lowered until it reaches the solidification point of the silicon. The poly melt crystallizes at the solid/liquid interface of the seed crystal and the melt, and as the chuck is then slowly raised out of the melt, a single-crystal ingot that replicates the orientation of the seed crystal is formed.

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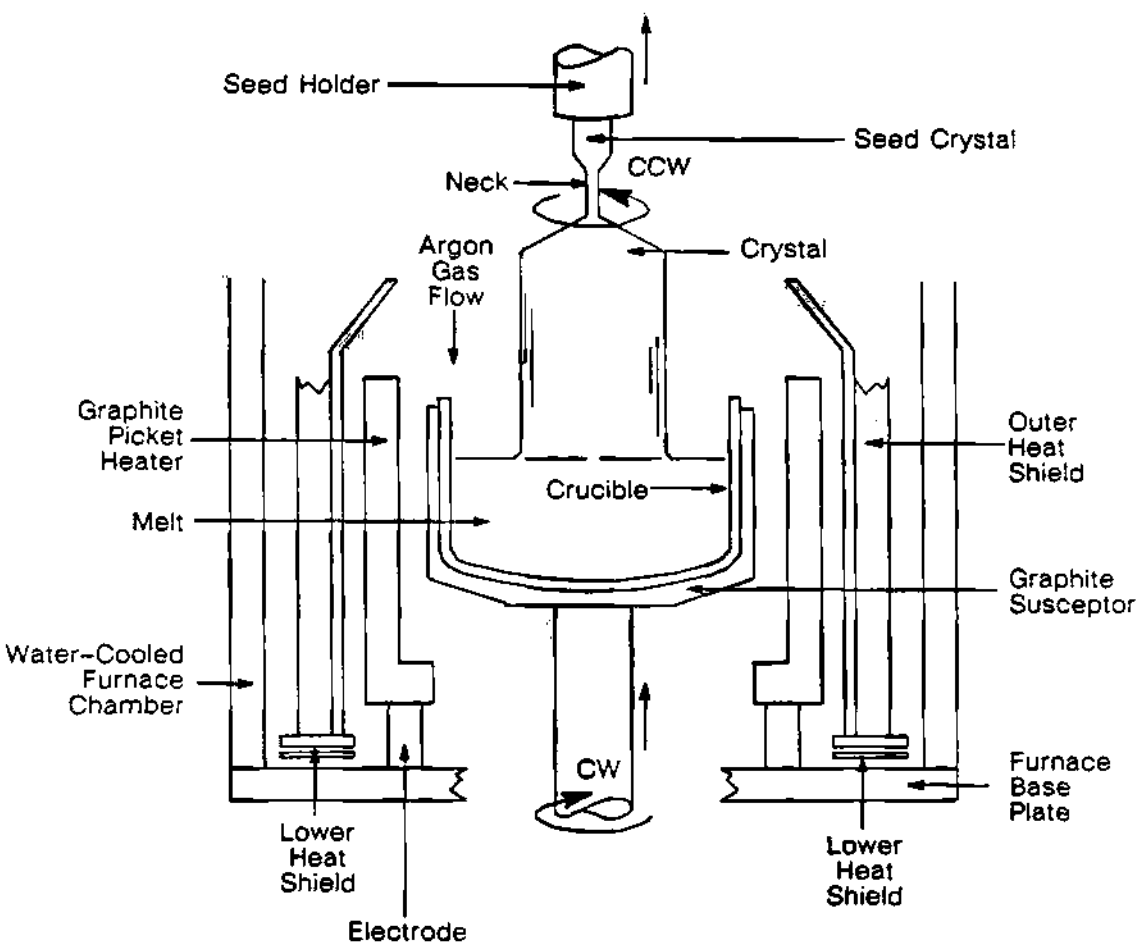
Figure 5

CZOCHRALSKI CRYSTAL-GROWING FURNACE



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The diameter of the crystal is determined by the temperature and the rate of speed at which the chuck is pulled from the melt. During the initial stage of crystal formation, an operator controls the rate of pull. When the desired diameter is reached, an automatic diameter control system, originally developed by Siltec, is activated, and monitors and controls the rate of pull for the rest of the operation.

The chuck and the crucible are rotated in opposite directions as the crystal is drawn out of the melt, providing a mixing of the melt to assure the greatest degree of uniformity in the dopant concentration throughout the length of the silicon ingot.

The Cz process offers a number of advantages over Fz crystal production. Large-diameter crystals can be formed. The Cz method allows crystals to be heavily doped, and is more economic since both poly and recycled croppings from the ends of ingots that have been sliced into wafers can be used in the melt.

The disadvantages include the variation in the resistivity profile of the silicon along the length and width of the crystal (resulting in variation across the resulting wafer), and contamination by oxygen and carbon. The variation in the resistivity profile is a result of the dopant not being incorporated into the solid crystal in the same concentration as it exists in the melt.

A processing advance called continuous-liquid silicon feed (CLF) provides a method of introducing fresh liquid silicon material into the melt during the crystal-pulling process, and provides more control of dopant levels in the finished ingot.

Oxygen contamination of the single-crystal ingot arises from the diffusion of oxygen out of the quartz crucible and into the melt. Convection currents resulting from the mixing movement of the crucible direct the oxygen into the solid/liquid interface. The convection currents within the melt are illustrated in Figure 6. Control of oxygen impurities has been improved under experimental conditions with a technique whereby a transverse magnetic field is applied to the melt during the crystal-growing process. This magnetic field dampens the convection currents produced in the melt, as shown in Figure 7, and thereby reduces the incorporation of oxygen into the area where the silicon is crystallizing. Magnetic dampening of convection currents also appears to control the development of microdefects associated with crystal striations formed during the solidification.

Carbon contamination of the ingot results from carbon impurities produced by the graphite susceptor surrounding the crucible (see Figure 5). Graphite is a form of carbon.

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Figure 6

THERMAL CONVECTION CURRENTS
IN CZOCHRALSKI FURNACE

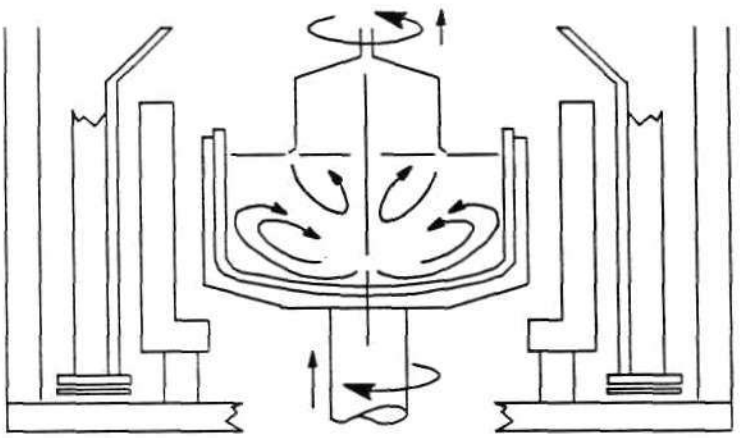
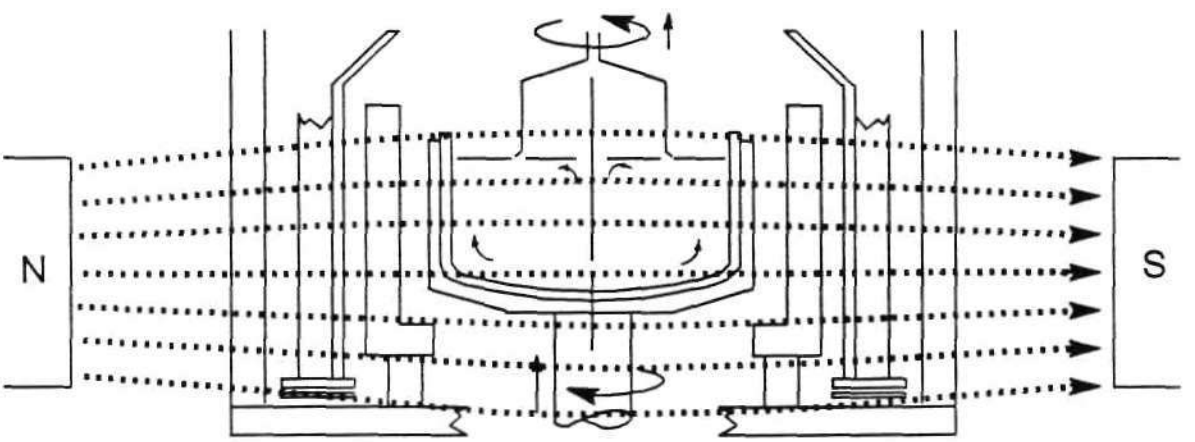


Figure 7

MAGNETIC DAMPENING



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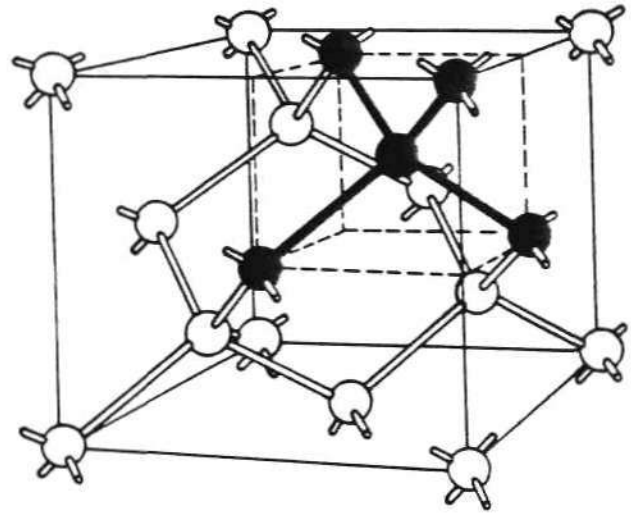
Crystal Orientation

The crystallographic cell is the smallest unit of a silicon crystal. Crystal orientation is determined in reference to the planes of this face-centered cell (see Figure 8). The majority of semiconductor devices are fabricated on silicon with 111 and 100 crystal orientations. There are subtle yet significant differences in physical parameters and consequent device performance characteristics, depending upon the particular crystal plane at which the wafers have been sliced from the ingot.

Figure 8

SILICON CRYSTAL FACE-CENTERED CELL



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For example, given identical diffusion conditions, the diffusion of impurities will vary between wafers with 111 and wafers with 100 crystal orientations. Orientation also affects the placement of the individual die on the wafer, as the wafer can be cut more cleanly relative to certain crystalline planes. The placement of the primary flat (a flat area on one edge of the wafer that is ground along the length of the original ingot after production), usually indicates optimum scribe direction. Crystal orientation also affects the deposition of epitaxial layers and the reduction of surface state charge in MOS devices.

Wafer Production

After production, the single-crystal silicon ingot is ground to a uniform diameter, and a primary orientation flat is ground along the length of the ingot to indicate crystal orientation.

Once ground, the ingot is sliced into wafers. The most common slicing method is by inside-diameter diamond sawing. Wafer flatness is becoming increasingly critical in maintaining photolithographic tolerances as wafer diameters continue to increase. Wafer flatness is a peak-to-valley measurement across the surface of the wafer. Typical flatness specifications require a peak-to-valley variation of not more than 1 micron per inch across the surface of the wafer.

Wafer flatness is a function of the movement of the blade during sawing. The more control in blade movement across the surface of the wafer, the flatter the resulting wafer and the less surface damage. Inside-diameter sawing employs a ring-shaped blade, as shown in Figure 9, with the diamond cutting surface on the inside. A tension is placed on the outside diameter of the saw blade assembly, which reduces lateral blade movement during the cut and as the blade withdraws back across the sliced surface before it proceeds to the next cut.

Once sliced, wafers undergo edge-rounding and lapping operations. Edge-rounding practices include mechanical rounding, followed by a chemical etch to relieve stresses on the crystal structure produced during the mechanical processing. The edge-profiling process removes material laden with microcracks that cause the wafers to be highly fracture-prone. Direct automatic cassette-to-cassette equipment has been developed for transfer of the wafers from manufacturers' shipping containers to processing cassettes to further reduce edge chipping.

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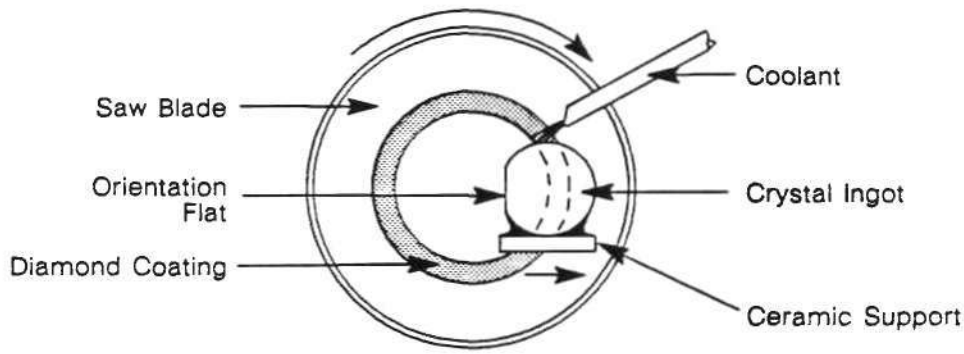
Figure 9

INNER-DIAMETER WAFER SAW



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Lapping operations involve a free-abrasive, double-sided machining process that mechanically reduces the physical disuniformities resulting from slicing. Silicon carbide and alumina abrasive powders remove up to 2 microns of silicon per wafer side in a planetary-motion carrier that moves the wafers between opposed, rotating metal lapping plates.

Lapping is followed by a chemical etch to obtain the mirrorlike surface of the finished wafer. An acid or caustic etching medium is employed to remove approximately 1 micron per side, ridding the wafer of surface microcracks that can propagate farther into the wafer.

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Silicon Database

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Silicon Database

INTRODUCTION

Dataquest's Semiconductor Equipment and Materials Service (SEMS) tracks the silicon wafer industry by examining the merchant silicon and epitaxial wafer market, captive silicon production, wafer pricing trends, and silicon square inch consumption. The market data for silicon and epitaxial wafers are collectively known as the SEMS Silicon Database and is organized into the following sections:

- Definitions and conventions
- Merchant silicon and epitaxial wafer suppliers
  - List of companies
  - World sales, 1985 through 1989
  - World share, 1985 through 1989
  - Company ranking
  - Wafer sales by regionally owned companies, 1985 through 1989
  - Market share by regionally owned companies, 1985 through 1989
- 1989 Regional silicon and epitaxial wafer markets
  - United States
  - Japan
  - Europe
  - Rest of World
  - World
- Wafer pricing
  - 1989 regional average selling prices of silicon and epitaxial wafers by wafer size
  - Silicon and epitaxial wafers—weighted average selling prices by region, 1985 through 1989
- Million-square-inch market
  - Merchant silicon and epitaxial wafers, 1985 through 1989
  - Captive silicon production, 1985 through 1989

The information in this document is focused on the silicon and epitaxial wafer markets. For additional information on the silicon and epitaxial wafer industry, please refer to the "Silicon History," "Silicon Technology," "Silicon and Epitaxial Wafers," and "Silicon Forecast" sections located behind the "Semiconductor Materials" tab in this binder, as well as the newsletters behind the "Semiconductor Materials" tab in the SEMS newsletter binder.

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DEFINITIONS AND CONVENTIONS

The calendar year sales of merchant silicon and epitaxial wafer suppliers are estimated in US dollars and converted to millions of square inches using an average selling price for each region. Currency appreciation over the last several years affects the dollar value of wafer sales of Japanese and West German companies. Dataquest uses average exchange rates supplied by the International Monetary Fund (IMF) to convert from local currency to US dollars. The average exchange rates for the Japanese yen and West German deutsche mark for 1985 through 1989 are shown in Table 1.

Please note the convention that the regional designation "United States" includes Canadian semiconductor manufacturing activities.

Silicon Products

The merchant silicon wafer market is categorized into two product segments: silicon wafers and silicon epitaxial wafers. (Silicon wafers grown by both Czochralski and float zone methods are included.) In the silicon database, Dataquest does not include sales of polysilicon, single-crystal silicon ingots (unless noted), silicon materials used in solar applications, or compound semiconductor material substrates such as gallium arsenide.

Silicon Producers

Companies that produce silicon and epitaxial wafers are defined as either merchant silicon companies or captive silicon producers. Merchant silicon companies are suppliers such as Shin-Etsu Handotai (SEH) of Japan and Wacker of West Germany.

Silicon also is produced to a lesser extent by both merchant and captive semiconductor manufacturers. These semiconductor manufacturers collectively are referred to as captive silicon producers because they grow single-crystal silicon to produce wafers for their own internal consumption. Captive producers with significant internal silicon production include AT&T, IBM, Motorola, and Texas Instruments in the United States, Hitachi in Japan, and to a lesser extent, Philips in Europe.

Table 1

Japanese and West German Exchange Rates

	1985	1986	1987	1988	1989
Yen/Dollar	238	167	144	128	139
Deutsche Mark/Dollar	2.94	2.17	1.80	1.78	-

Source: IMF

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Merchant or Captive?

Some captive silicon producers have sold small amounts of materials on the merchant silicon market. These producers have sold wafers in order to ensure that internal production methods continue to produce material of competitive quality and cost. Dataquest estimates that merchant sales for these companies historically have represented a small percentage of their total captive silicon production, and thus these companies are identified as captive rather than merchant silicon producers.

Dataquest identifies Toshiba Ceramics, a subsidiary of Toshiba Corporation, as a merchant silicon company even though a substantial amount of its silicon production is consumed by its semiconductor parent. However, because Toshiba Ceramics is actively marketing its material on the merchant market, Toshiba Ceramics is considered a merchant rather than a captive silicon producer. Toshiba Corporation is considered a customer of Toshiba Ceramics.

MERCHANT SILICON AND EPITAXIAL WAFER SUPPLIERS

Table 2 contains a list of merchant silicon manufacturers that were active in the world market in 1988. This list, organized by region of corporate ownership, summarizes whether a company offers silicon and/or epitaxial wafers.

Merchant Wafer Sales, 1985-1989

Table 3 presents worldwide merchant silicon and epitaxial wafer company sales for the years 1985 through 1989. Table 4 summarizes company world market share during this same time period. The regional market detail for 1989 is presented later in this report.

The same nine merchant wafer companies have dominated the silicon and epitaxial wafer market from 1985 through 1989. Table 5 presents the worldwide wafer sales of these nine companies according to their 1989 rankings.

Table 6 presents the combined sales of silicon and epitaxial wafers by regionally owned merchant companies in the four regions of the world. Regional ownership is defined as the region where a wafer company's corporate parent is headquartered. For example, in Table 6, the sales of Shin-Etsu Handotai's US subsidiary, SEH America, are included in Japanese company sales in the United States. Similarly, the sales of Wacker Siltronic, the US affiliate of Europe-based Wacker Chemitronic, are included in European company sales in the United States. Table 7 represents the revenue information from Table 6 translated into percent shares.

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Table 2

World Merchant Silicon and Epitaxial Companies

	Silicon Wafers	Epitaxial Wafers
US Companies		
Crysteco, Inc.	X	
Epitaxy, Inc.		X
General Instrument		
Power Semiconductor Division		X
M/A-COM Semiconductor Products		X
Pensilco	X	
Recticon	X	
Spire Corporation		X
Virginia Semiconductor	X	
Japanese Companies		
Kawasaki Steel		
—NBK Corporation	X	X
Komatsu Electronic Metals	X	X
Mitsubishi Metal		
—Japan Silicon	X	X
—Siltec Corporation	X	X
Nittetsu Denshi	X	X
Osaka Titanium Company		
—Cincinnati Semiconductor		X
—Osaka Titanium Company	X	X
—U.S. Semiconductor		X
Shin-Etsu Handotai	X	X
Showa Denko	X	X
Toshiba Ceramics	X	X
European Companies		
Huels AG		
—DNS Electronic Materials	X	X
—MEMC	X	X
Okmetic	X	
Siltronix SA	X	
Topsil Semiconductor Materials A/S	X	
Wacker	X	X
ROW Companies		
South Korea		
Korsil	X	
Lucky Advanced Materials, Inc.	X	
Taiwan		
Hermes Epitaxy		X
Sino-America	X	
Tatung Company	X	

Source: Dataquest (August 1990)

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Table 3

Merchant Silicon and Epitaxial Wafer Suppliers
Company Ranking
(Millions of Dollars)

Worldwide Wafer Sales	1985	1986	1987	1988	1989	1989 Ranking
Shin-Etsu Handotai	298.9	408.0	452.1	567.3	645.3	1
Huels AG	-	-	-	-	358.5	2
Osaka Titanium Company[1]	132.3	197.6	235.5	281.6	317.4	3
Mitsubishi Metal Corp.[2]	123.2	195.0	241.3	300.2	303.4	4
Komatsu Electronic Metals	113.8	168.5	197.3	256.9	254.2	5
Wacker	160.4	162.1	166.5	193.0	214.4	6
Toshiba Ceramics	35.1	61.0	78.9	94.5	112.0	7
Cincinnati Milacron[3]	42.1	37.9	34.0	30.2	-	
DNS Electronic Materials[3]	43.0	53.0	63.0	74.5	-	
Monsanto[3]	137.0	154.0	185.0	254.0	-	
Others	82.0	79.9	71.7	118.3	141.2	
Total	1,167.8	1,517.0	1,725.3	2,170.5	2,346.4	

[1]Includes US Semiconductor sales, 1987 and 1988; Cincinnati Semiconductor 1989
[2]Includes Siltec sales (1987 and 1988)
[3]Acquired by other wafer manufacturers
Source: Dataquest (August 1990)

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Table 4

Merchant Silicon and Epitaxial Wafer Sales by Regionally Owned Companies, 1985-1989 (Percent Share)

	1985	1986	1987	1988	1989
United States					
US Companies	58.9%	55.3%	46.0%	44.1%	7.3%
Japanese Companies	19.4	24.5	33.2	35.4	46.0
European Companies	21.7	20.2	20.8	20.2	46.6
ROW Companies	0	0	0	0.3	0.1
Total	100.0%	100.0%	100.0%	100.0%	100.0%
Japan					
US Companies	1.4%	1.4%	2.2%	3.0%	0
Japanese Companies	97.7	98.0	96.9	96.1	95.7
European Companies	0.9	0.6	0.9	0.9	4.2
ROW Companies	0	0	0	0	0
Total	100.0%	100.0%	100.0%	100.0%	100.0%
Europe					
US Companies	14.3%	14.3%	17.0%	20.9%	0.8%
Japanese Companies	8.5	13.8	19.7	18.1	19.0
European Companies	77.1	71.8	63.2	61.1	80.2
ROW Companies	0	0	0	0	0
Total	100.0%	100.0%	100.0%	100.0%	100.0%
Rest of World					
US Companies	29.0%	34.6%	29.7%	26.4%	4.4%
Japanese Companies	11.3	13.5	15.0	11.2	13.7
European Companies	58.6	49.7	45.0	33.2	56.0
ROW Companies	1.1	2.2%	10.2	29.1	26.0
Total	100.0%	100.0%	100.0%	100.0%	100.0%
World					
US Companies	21.4%	16.6%	14.6%	14.7%	2.1%
Japanese Companies	60.2	68.4	70.9	70.7	71.2
European Companies	18.3	14.9	14.0	12.9	25.2
ROW Companies	0	0.1	0.5	1.7	1.4
Total	100.0%	100.0%	100.0%	100.0%	100.0%

Note: Monsanto Electronic Materials Company acquired by Huels AG of West Germany and Cincinnati Milacron of the United States acquired by Osaka Titanium Company of Japan
Source: Dataquest (August 1990)

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Table 5

World Silicon and Epitaxial Wafer Market, 1989
(Millions of Dollars)

Company	Silicon Wafers Sales	Epitaxial Wafers Share	Total Sales	Share	Sales	Share
US-Based Companies						
Crysteco	11.6	0.6%	0	0	11.6	0.5%
Epitaxy, Inc.	0	0	9.6	1.7%	9.6	0.4
Recticon	7.0	0.4	0	0	7.0	0.3
UniSil Corp.	8.5	0.5	0	0	8.5	0.4
Other US Companies	5.7	0.3	6.2	1.1	11.9	0.5
Total	32.8	1.8%	15.8	2.8%	48.6	2.1%
Japan-Based Companies						
Kawasaki Steel, NBK Corp.	6.8	0.4%	1.2	0.2%	8.0	0.3%
Komatsu Electronic Metals	200.8	11.2	53.4	9.5	254.2	10.8
Mitsubishi Metal Corp.	216.4	12.1	87.0	15.5	303.4	12.9
Japan Silicon	172.4	-	82.0	-	254.4	-
Siltec	44.0	-	5.0	-	49.0	-
Osaka Titanium Company*	247.6	13.9	69.8	12.4	317.4	13.5
Shin-Etsu Handotai	461.0	25.8	184.3	32.9	645.3	27.5
Toshiba Ceramics	78.5	4.4	33.5	6.0	112.0	4.8
Other Japanese Companies	31.3	1.8	0	0	31.3	1.3
Total	1,242.4	69.6%	429.2	76.5%	1,671.6	71.2%
Europe-Based Companies						
Huels AG	287.1	16.1%	71.4	12.7%	358.5	15.3%
Topsil Semiconductor Materials A/S	13.1	0.7	0	0	13.1	0.6
Wacker	171.5	9.6	42.9	7.6	214.4	9.1
Other European Companies	6.4	0.4	0	0	6.4	0.3
Total	478.1	26.8%	114.3	20.4%	592.4	25.2%
ROW-Based Companies						
Korsil	15.0	0.8%	0	0	15.0	0.6%
Lucky Advanced Materials, Inc.	14.5	0.8	0	0	14.5	0.6
Other ROW Companies	2.8	0.2	1.5	0.3%	4.3	0.2
Total	32.3	1.8%	1.5	0.3%	33.8	1.4%
Total Sales—Worldwide	1,785.6	100.0%	560.8	100.0%	2,346.4	100.0%

*Includes US Semiconductor and Cincinnati Semiconductor sales
Source: Dataquest (August 1990)

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Table 6

1989 Regional Average Selling Prices of Silicon and Epitaxial Wafers by Wafer Size

Wafer Diameter Wafer Area (Square Inches)	3-inch 7.07	100mm 12.17	125mm 19.02	150mm 27.39	200mm 48.70
Per Wafer ($/Wafer)					
CZ Polished Wafers					
North America	6.35	9.64	17.44	30.49	120.48
Europe	7.81	11.26	18.47	31.88	123.06
ROW	6.50	10.00	17.82	29.12	-
Japan	10.88	12.17	24.49	42.37	131.03
Japan* (¥/Wafer)	1,513	1,692	3,405	5,889	18,214
Epitaxial Wafers					
North America	24.39	31.64	50.46	80.03	-
Europe	24.39	34.92	57.12	87.98	-
ROW	20.79	34.08	52.69	86.44	-
Japan	35.60	46.67	71.70	114.88	-
Japan* (¥/Wafer)	4,949	6,487	9,966	15,968	-
Per Square Inch ($/SI)					
CZ Polished Wafers					
North America	0.898	0.792	0.917	1.113	2.474
Europe	1.11	0.93	0.97	1.16	2.53
ROW	0.92	0.82	0.94	1.06	-
Japan	1.54	1.00	1.29	1.55	2.69
Japan* (¥/Wafer)	214	139	179	215	374
Epitaxial Wafers					
North America	3.45	2.60	2.65	2.92	-
Europe	3.45	2.87	3.00	3.21	-
ROW	2.94	2.80	2.77	3.16	-
Japan	5.04	3.83	3.77	4.19	-
Japan* (¥/Wafer)	700	533	524	583	-

*¥139 = US$1
Source: Dataquest (August 1990)

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Table 7

Silicon and Epitaxial Wafers
Weighted Average Selling Price by Region, 1985-1989
(Dollars per Square Inch)

	1985	1986	1987	1988	1989
Silicon Wafers					
United States	0.96	0.88	0.85	0.87	0.80
Europe	0.89	1.03	1.00	1.02	1.04
ROW	0.93	0.86	0.92	0.93	0.94
Japan	0.98	1.33	1.45	1.59	1.37
Japan (¥/SI)	233	221	209	204	190
Epitaxial Wafers					
United States	2.93	2.86	2.67	2.80	2.70
Europe	2.89	2.86	2.92	2.95	3.01
ROW	2.90	2.90	2.85	2.70	2.85
Japan	2.61	3.29	3.68	4.30	4.29
Japan (¥/SI)	620	549	530	551	550

Source: Dataquest (August 1990)

1989 REGIONAL MERCHANT SILICON AND EPITAXIAL WAFER MARKETS

This section presents Dataquest's estimates of worldwide silicon and epitaxial wafer shipments by the merchant silicon companies in 1989. Our estimates of company sales include wafers sold directly to semiconductor manufacturers and those sold to epitaxial silicon wafer houses that do not grow all of their own substrate material. The potential problem of double-counting million square inches that arises from sales to epi houses is corrected in our final analysis of total million-square-inch consumption by the semiconductor industry. The company market shares that we publish, however, reflect sales to both sets of customers: semiconductor manufacturers and epitaxial silicon wafer companies.

WAFER PRICING

Table 6 presents the 1989 average selling prices (ASPs) for merchant silicon and epitaxial wafers in the United States, Japan, Europe, and ROW, on a per-wafer basis and per-square-inch basis for 3-inch through 200mm wafers. (Japanese wafer prices are reported in yen as well as dollars.) The silicon wafer prices reflect the ASP for polished CZ wafers. Epitaxial wafer prices can vary considerably, depending upon the level of custom specifications and the thickness of the epitaxial layer required. The regional ASPs presented in Table 6 reflect a broad distribution in product specifications for each wafer size.

The regional ASP per square inch of silicon and epitaxial wafers is dependent upon the wafer size mix in the different regions of the world. Table 7 presents a five-year perspective of the regional ASPs per square inch for both silicon and epitaxial wafers, weighted by the wafer size

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distribution. It also should be noted that the weighted silicon wafer ASP in Table 7 reflects several different types of wafers sold by merchant silicon companies including test, polished CZ, and float zone wafers.

MILLION-SQUARE-INCH MARKET

The following section presents 1985 through 1989 MSI estimates for the merchant silicon and epitaxial wafer market. Internal production of silicon by captive silicon producers is estimated.

Merchant Silicon Companies

The merchant silicon and epitaxial wafer market, as measured in MSI, is determined for each of the four regions of the world by dividing merchant silicon company sales in a given region by the regional average selling price per square inch. Table 8 contains the million-square-inch market of merchant silicon and epitaxial wafers based on this procedure. Please note that the 1989 merchant silicon revenue in ROW included some sales of ingots by Monsanto to its Korean joint venture, Korsil. The silicon MSI estimate for ROW in Table 8 has been modified to reflect these transactions.

Table 8

Merchant Silicon and Epitaxial Wafer Market by Region, 1985-1989
(Million Square Inches)

	1985	1986	1987	1988	1989
Merchant Silicon Wafers					
United States	281	296	325	364	435
Japan	515	548	565	661	796
Europe	134	138	155	174	194
Rest of World	41	62	75	95	123
Total	972	1,044	1,120	1,294	1,547
Merchant Epitaxial Wafers					
United States	25	29	35	45	54
Japan	49	65	71	75	76
Europe	6	9	12	15	18
Rest of World	2	2	3	4	5
Total	82	104	120	139	152
Total Merchant Wafers					
United States	307	324	360	409	489
Japan	564	613	636	736	872
Europe	140	147	166	189	211
Rest of World	43	64	78	98	127
Total	1,054	1,148	1,240	1,432	1,699

Source: Dataquest (August 1990)

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In the United States, several small epitaxial houses do not grow all of their own silicon substrate material, but rather purchase their wafers from other merchant silicon companies. For this reason, it is necessary to correct the square inches of silicon derived from sales of silicon wafers in the United States for the amount of silicon substrate sold to epitaxial silicon companies. Dataquest estimates that this corresponds to approximately 11 to 13 MSI per year from 1985 through 1989. The US silicon million-square-inch estimates presented in Table 8 include this corrective factor.

Captive Silicon Production

In 1989, six semiconductor manufacturers grew single-crystal silicon to produce wafers for internal consumption. Four of these were US companies, including AT&T, IBM, Motorola, and Texas Instruments. Hitachi in Japan, through its subsidiary, Hitachi Ohme Denshi, perform captive silicon production. Table 9 contains Dataquest's estimates of the silicon produced by these semiconductor manufacturers in the years 1985 through 1989. No distinction is made between silicon and epitaxial wafers in the MSI estimates for the captive silicon producers.

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Table 9

Captive Silicon Production 1985-1989
(Million Square Inches)

	1985	1986	1987	1988	1989
Total Captive Silicon Production					
AT&T	15	15	17	18	18
Delco Electronics	3	1	0	0	0
Fairchild	3	0	0	0	0
Hitachi	18	18	18	18	18
IBM	18	18	18	20	12
Motorola	15	15	15	18	18
Philips	6	5	2	2	2
Texas Instruments	45	46	45	54	58
Total—Worldwide	123	118	115	130	126
Regional Consumption of Captive Silicon Production					
United States					
AT&T	15	15	17	18	18
Delco Electronics	3	1	0	0	0
Fairchild	3	0	0	0	0
IBM	18	18	18	20	12
Motorola	15	15	15	18	18
Texas Instruments	37	32	25	31	34
Total—United States	91	81	75	87	82
Japan					
Hitachi	18	18	18	18	18
Texas Instruments	6	11	16	18	19
Total—Japan	24	29	34	36	37
Europe					
Philips	6	5	2	2	2
Texas Instruments	2	3	4	5	5
Total—Europe	8	8	6	7	7

Source: Dataquest (August 1990)

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Silicon Forecast

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Silicon Forecast

SILICON CONSUMPTION

Tables 1 and 2 present the historical and forecast consumption of silicon in million square inches (MSI) by region.

The market for silicon and other fabrication materials is dependent on the level of semiconductor device production in the different regions of the world. Tables 3 and 4 present the historical (1985 through 1989) and forecast (1989 through 1994) production revenue for captive and merchant semiconductor manufacturers by region of production. The silicon forecast in Table 2 is tied to the device production forecast presented in Table 4.

Table 1

Historical Silicon Consumption by Region, 1985-1989
(Million Square Inches)

	1985	1986	1987	1988	1989	CAGR 1985-1989
United States	398	405	435	496	571	9.4%
Growth	(43.7%)	1.9%	7.3%	13.6%	14.9%	
Japan	588	642	670	772	909	11.5%
Growth	(11.0%)	9.1%	4.4%	15.2%	17.6%	
Europe	148	155	172	196	218	10.1%
Growth	(7.5%)	4.6%	10.9%	14.0%	11.2%	
Rest of World	43	64	78	98	127	31.2%
Growth	(15.7%)	47.9%	22.0%	26.8%	29.4%	
World	1,177	1,266	1,355	1,562	1,825	11.6%
Growth	(25.5%)	7.5%	7.0%	15.2%	16.7%	

Source: Dataquest (August 1990)

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Table 2

Forecast Silicon Consumption by Region, 1989-1994
(Million Square Inches)

	1989	1990	1991	1992	1993	1994	CAGR 1989-1994
United States	571	578	647	757	929	924	10.1%
Growth	14.9%	1.8%	11.9%	17.0%	22.8%	(0.5%)	
Japan	909	985	1,029	1,151	1,368	1,345	8.2%
Growth	17.6%	8.5%	4.5%	11.8%	18.8%	(1.7%)	
Europe	218	253	311	385	483	505	18.2%
Growth	11.2%	15.7%	23.3%	23.7%	25.2%	4.6%	
Rest of World	127	181	217	255	301	315	19.8%
Growth	29.4%	42.4%	19.5%	17.6%	18.1%	4.6%	
World	1,825	1,997	2,204	2,548	3,081	3,089	11.1%
Growth	16.7%	9.6%	10.4%	15.6%	20.9%	0.3%	

Source: Dataquest (August 1990)

Table 3

Historical Semiconductor Production by Region, 1985-1989
(Millions of Dollars)

	1985	1986	1987	1988	1989	CAGR 1985-1989
United States	12,654	14,456	16,711	20,171	21,880	14.7%
Growth	(18.9%)	14.2%	15.6%	20.7%	8.5%	
Japan	10,651	14,686	19,004	26,693	29,061	28.5%
Growth	(11.3%)	37.9%	29.4%	40.5%	8.9%	
Europe	3,403	3,831	4,671	5,789	6,439	17.3%
Growth	(0.9%)	12.6%	21.9%	23.9%	11.2%	
Rest of World	406	756	1,088	1,868	2,522	57.9%
Growth	(16.3%)	86.2%	43.9%	71.7%	35.0%	
World	27,114	33,729	41,474	54,521	59,902	21.9%
Growth	(13.4%)	24.4%	23.0%	31.5%	9.9%	

Source: Dataquest (August 1990)

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Table 4

Forecast Semiconductor Production by Region, 1989-1994
(Millions of Dollars)

	1989	1990	1991	1992	1993	1994	CAGR 1989-1994
United States	21,880	21,156	24,391	30,256	40,114	43,103	14.5%
Growth	8.5%	(3.3%)	15.3%	24.0%	32.6%	7.5%	
Japan	29,061	28,374	31,144	36,919	47,811	51,243	12.0%
Growth	8.9%	(2.4%)	9.8%	18.5%	29.5%	7.2%	
Europe	6,439	7,526	9,651	12,595	16,876	18,881	24.0%
Growth	11.2%	16.9%	28.2%	30.5%	34.0%	11.9%	
Rest of World	2,522	3,125	4,220	5,359	7,028	8,158	26.5%
Growth	35.0%	23.9%	35.0%	27.0%	31.1%	16.1%	
World	59,902	60,181	69,406	85,129	111,829	121,385	15.2%
Growth	9.9%	0.5%	15.3%	22.7%	31.4%	8.5%	

Source: Dataquest (August 1990)

WAFER SIZE DISTRIBUTION

The changing mix of wafer size is an indicator of the penetration of leading-edge equipment and new fab capacity. The estimated percentage of consumption of silicon MSI by wafer size for 1985 through 1993 is presented in Table 5. This information reflects Dataquest's estimate of wafer size consumption for semiconductor production in the United States. For convenience, the information in Table 5 has also been translated into percentage of wafer starts and is presented as such in Table 6.

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Table 5

Estimated Worldwide Square-Inch Distribution by Wafer Size, 1985-1994
(Percent Million Square Inches)

Size	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994
2-Inch	0.9%	0.8%	0.6%	0.5%	0.3%	0.2%	0.2%	0.2%	0.1%	0
3-Inch	7.2	6.0	3.5	3.1	3.3	3.0	2.6	2.1	1.5	0.5%
100mm	42.9	35.4	30.0	28.4	26.5	24.3	22.6	20.7	18.7	14.4
125mm	38.3	41.9	45.0	42.9	39.8	36.9	34.0	31.4	28.8	27.4
150mm	10.7	15.8	20.5	24.3	28.2	31.6	34.8	37.9	41.0	47.1
200mm	0	0	3	8	1.9	3.9	5.9	7.8	9.8	10.6
Total	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%
Total MSI	1,177	1,266	1,355	1,562	1,823	2,001	2,209	2,554	3,087	2,913

Source: Dataquest (August 1990)

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Table 6

Estimated Worldwide Wafer Start Distribution by Wafer Size, 1985-1994
(Wafer Starts—Millions)

Size	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994
2-Inch	3.4	3.4	2.5	2.5	1.5	1.5	1.4	1.2	0.9	0.5
3-Inch	12.0	10.8	6.8	6.8	8.6	8.6	8.1	7.5	6.7	4.4
100mm	41.5	36.8	33.5	36.4	39.7	40.0	41.0	43.4	47.5	42.6
125mm	23.7	27.9	32.1	35.3	38.2	38.8	39.5	42.1	46.8	42.9
150mm	4.6	7.3	10.2	13.9	18.8	23.1	28.0	35.3	46.2	50.0
200mm	0	0	0.1	0.3	0.7	1.6	2.7	4.1	6.2	7.4
Total Wafers (Millions)	85.2	86.2	85.1	95.1	107.5	113.7	120.7	133.7	154.3	147.7
Average Wafer Diameter (Inches)	4.2	4.3	4.5	4.6	4.6	4.7	4.8	4.9	5.0	5.0

Source: Dataquest (August 1990)

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Silicon and Epitaxial Wafer Companies

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Silicon and Epitaxial Wafer Companies

INTRODUCTION

This study presents an overview of merchant silicon and epitaxial wafer companies, including a discussion of company products, market focus, and manufacturing activities. Please refer to the sections entitled "Silicon Database" and "Silicon Forecast" located behind the Semiconductor Materials tab in this binder for information on the silicon and epitaxial wafer markets including wafer pricing, company market share, captive silicon production, and regional silicon consumption—both historical and forecast.

SILICON SUPPLIERS

Merchant Silicon Companies

Companies that produce silicon and epitaxial wafers are defined as either merchant silicon companies or captive silicon producers. Merchant silicon companies include suppliers such as Shin-Etsu Handotai (SEH) of Japan and Wacker of West Germany. These companies and other merchant wafer suppliers will be discussed in later sections.

Captive Silicon Producers

Silicon also is produced to a lesser extent by both merchant and captive semiconductor manufacturers. These semiconductor manufacturers collectively are referred to as captive silicon producers because they grow single-crystal silicon to produce wafers for their own internal consumption. Captive producers with significant internal silicon production include AT&T, IBM, Motorola, and Texas Instruments in the United States, Hitachi in Japan, and to a lesser extent, Philips in Europe.

Semiconductor manufacturers with captive silicon production tend to be established, vertically integrated companies. In the early years of the semiconductor industry, the high cost of silicon provided sufficient economic justification for some semiconductor manufacturers to develop this internal capability. Today, however, high-quality, low-cost silicon wafers are readily available from a number of merchant silicon companies. In response to such competitive factors, some semiconductor manufacturers have shut down their silicon operations. Fairchild closed its silicon wafer plant in Healdsburg, California, in June 1985, and later sold its silicon production equipment to Pentagood Training, Ltd., a Hong Kong firm, for $3.5 million. This equipment, in turn, was sold to the People's Republic of China. Delco, another semiconductor manufacturer with internal silicon production, discontinued its captive silicon operations in the spring of 1986. Although Motorola continues to produce single-crystal silicon, the company closed its 100-metric-ton polysilicon plant in the fall of 1986. At the end of 1988, Texas Instruments announced that it would end polysilicon production at its Sherman, Texas, facility, but would continue its captive single-crystal silicon operations.

Merchant or Captive?

Some captive silicon producers, such as Motorola and Fairchild (when it was actively producing silicon), have sold small amounts of material on the merchant silicon market. Such

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captive silicon producers have sold wafers in order to ensure that internal production methods continue to produce material of competitive quality and cost. Dataquest estimates that merchant sales for these companies historically have represented a small percentage of their total captive silicon production, and thus Dataquest identifies these companies as captive rather than merchant silicon producers.

Dataquest identifies Toshiba Ceramics, a subsidiary of Toshiba Corporation, as a merchant silicon company although a substantial amount of its silicon production is consumed by its semiconductor parent. However, because Toshiba Ceramics is actively marketing its material on the merchant market, Dataquest considers Toshiba Ceramics to be a merchant rather than a captive silicon producer. Toshiba Corporation is considered to be a customer of Toshiba Ceramics.

SILICON AND EPITAXIAL WAFER PRODUCTS

Dataquest categorizes the merchant silicon wafer market into two product segments: silicon wafers and silicon epitaxial wafers. (Silicon wafers grown by both Czochralski and float-zone methods are included.) In addition to single-crystal silicon ingots and wafers, several merchant silicon companies produce polysilicon. Information regarding poly plant locations and capacities for these companies is included in the merchant silicon company profiles.

Silicon Wafers

In the early days of the semiconductor industry, silicon was considered to be one of several materials with semiconductor potential. With the development of planar processing in 1960, polysilicon price reductions, and inexpensive plastic packaging for silicon transistors, silicon took the market from germanium as the basic element used to manufacture semiconductor devices. Please refer to the "Silicon History" and "Silicon Technology" sections behind the Semiconductor Materials tab in this binder for reference information regarding the history of silicon manufacturing in the United States, and the technology of single-crystal growth and wafer production.

Epitaxial Wafers

Epitaxial processing produces a layer of single-crystal material that has the same crystallographic orientation as the underlying substrate. It is possible to design the epitaxial layer to meet well-defined chemical, physical, and electrical specifications. The epitaxial layer of material is produced by a chemical vapor phase deposition reaction upon a polished substrate, which also has been manufactured to tightly controlled specifications. The substrate of the epi wafer may be doped uniformly or may include buried layers (isolated regions of heavy doping diffused in a lightly doped substrate). Uniformly doped substrates are used typically in CMOS applications while buried layers are used in bipolar device structures.

CMOS Epi

An area where epitaxy has become important is in CMOS device fabrication. CMOS circuits are especially vulnerable to a condition known as latch-up. In CMOS construction, n-type and p-type wells are in sufficiently close proximity to create parasitic n-p-n-p (silicon-controlled rectifier type) switching structures. Latch-up occurs when such parasitic devices turn on due to a transient condition such as forward biasing produced by a voltage spike. In latch-up, the CMOS

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device presents a near short-circuit condition across the power supply. The adverse effects of this can range from the interruption of further circuit operation until the condition is removed to physical destruction of the chip. With CMOS design rules in the 1-micron regime and gate oxide thicknesses approaching 100 angstroms, latch-up becomes more of a problem. High-resistivity epi layers on low-resistivity substrates are now used as a technique for latch-up hardening (prevention).

WORLDWIDE MERCHANT SILICON AND EPITAXIAL WAFER COMPANIES

Table 1 contains a list of active merchant silicon and epitaxial wafer companies. Organized by region of corporate ownership, the table summarizes whether a company offers silicon and/or epitaxial wafers. The manufacturing activities of these companies are summarized in the following sections. Silicon wafer companies in Brazil and India (not listed in Table 1) are discussed in the section entitled "ROW-Based Silicon Companies." In addition, companies that have closed their silicon wafer operations in the last several years are briefly discussed; the companies are Gensil and Silicon Services of the United States and Rhone-Siltec of France.

Table 1

Worldwide Merchant Silicon and Epitaxial Wafer Companies

Company	Silicon Wafers	Epitaxial Wafers
U.S. Companies		
Crysteco, Inc.	X	
Epitaxy, Inc.		X
General Instrument Power Semiconductor Division		X
M/A-COM Semiconductor Products		X
Pensilco	X	
Recticon	X	
Spire Corporation		X
Virginia Semiconductor	X	
Japanese Companies		
Kawasaki Steel —NBK Corporation	X	X
Komatsu Electronic Metals	X	X
Mitsubishi Metal —Japan Silicon	X	X
—Siltec Corporation	X	X
Nittetsu Denshi	X	X
Osaka Titanium Company	X	X
—Cincinnati Semiconductor		X
—U.S. Semiconductor		X

(Continued)

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Table 1 (Continued)

Worldwide Merchant Silicon and Epitaxial Wafer Companies

Company	Silicon Wafers	Epitaxial Wafers
Japanese Companies (Continued)		
Shin-Etsu Handotai	X	X
Showa Denko	X	X
Toshiba Ceramics	X	X
European Companies		
Huels AG		
—MEMC Electronic Materials*	X	X
Okmetic	X	
Siltronix SA	X	
Topsil Semiconductor Materials A/S	X	
Wacker	X	X
ROW Companies		
South Korea		
Korsil	X	
Lucky Advanced Materials, Inc.	X	
Taiwan		
Hermes Epitaxy		X
Sino-America	X	
Tatung Company	X	
Departures		
Gensil	X	
Silicon Services		X
Rhone-Siltec	X	

*MEMC Electronic Materials includes the former silicon operations of DNS Electronic Materials and Monsanto Electronic Materials Company.

Source: Dataquest
January 1990

UNITED STATES SILICON COMPANIES

Crysteco, Inc.

Crysteco, Inc., of Wilmington, Ohio, supplies silicon wafers to the semiconductor industry. The company specializes in supplying arsenic-doped silicon material. All material grown is Czochralski silicon, though Dataquest believes that Crysteco provides some slice and polish services for float-zone ingots. In addition to selling wafers, the company sells a small amount of single-crystal silicon ingots.

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Epitaxy, Inc.

Epitaxy, Inc., is an epitaxial wafer company in Santa Clara, California; the company was established in 1972. Epitaxy, Inc., does not grow any substrate material, but rather purchases it from other merchant silicon manufacturers. Like several other small custom epi houses, it is pursuing niche market applications and has opted not to compete in the CMOS epi wafer market.

General Instrument—Power Semiconductor Division

The Power Semiconductor Division of General Instrument (Westbury, New York) manufactures epitaxial wafers. Most of its epi wafers are used in-house, but a small number is sold on the merchant market. Major applications for its epitaxial wafers include microwave and radio frequency (RF) discrete devices.

M/A COM Semiconductor Products

M/A-COM Semiconductor Products (Burlington, Massachusetts) produces epitaxial silicon wafers for the semiconductor industry. It offers epi wafers from 3 inches to 125mm in diameter. These wafers are used primarily in discrete device applications, with a small amount used in CMOS processing as well.

In 1985, M/A-COM produced 50 percent of its silicon substrate material and purchased 50 percent from other companies. In 1986, however, M/A-COM decided to curtail its single-crystal growth operations. The company now obtains all of its silicon substrate requirements from other merchant silicon companies.

Pensilco

Pensilco is a small silicon wafer manufacturer in Bradford, Pennsylvania. It specializes in small-diameter wafers, which range from 1 inch to 100mm in diameter. It provides customized silicon wafers, especially for zener diode fabrication. The company started its silicon operations in 1958 under the name of Allegheny Electronics; the Pensilco name was adopted in 1976.

Recticon

Recticon is a small silicon wafer company in Pottstown, Pennsylvania. Rockwell International sold Recticon to Walker International in the first quarter of 1986. (Walker plans to use the acquisition to move out of its traditional business, photo processing.) Recticon has established a niche business supplying very thin and smaller-size wafers, but currently can produce wafers from 1 inch to 125mm in diameter. In addition, the company specializes in growing single-crystal silicon with unusual crystal orientations. Recticon has attracted interest from semiconductor R&D groups that want to use silicon wafers with unusual orientations as substrates for gallium arsenide-on-silicon processing.

Spire Corporation

Spire Corporation (Bedford, Massachusetts) supplies epitaxial silicon wafers to the semiconductor industry. Spire provides 2-inch, 3-inch, and 100mm epi wafers and focuses on meeting custom epitaxial specifications for microwave devices and discretes. The company has chosen not

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to pursue the MOS epitaxial wafer market. In addition to silicon epitaxial wafers, Spire supplies compound semiconductor epitaxial wafers and silicon-on-insulator (SOI) wafers. The company first began its efforts in SOI in 1985. In the fall of 1988, Texas Instruments signed an agreement with Spire that enables Spire to market SOI wafers produced by TI. Spire also manufactures MOCVD equipment.

Virginia Semiconductor

Virginia Semiconductor, a small silicon wafer manufacturer in Fredericksburg, Virginia, specializes in small-diameter wafers (from 1 to 3 inches) and offers very thin wafers of three-mil (0.003-inch) thickness. Founded in 1978, Virginia Semiconductor started production of float-zone and Czochralski single-crystal ingots in June 1979.

JAPANESE SILICON COMPANIES

Kawasaki Steel, NBK Corporation

NBK Corporation (Santa Clara, California) is a small silicon wafer manufacturer located in the Silicon Valley. In the third quarter of 1985, NBK was purchased by Kawasaki Steel for $9.4 million. The acquisition was part of the Japanese steelmaker's strategy for diversification into electronic materials. Kawasaki Steel invested $8.3 million in NBK in 1986 to upgrade to 150mm wafer capability and improve silicon wafer quality control with a Class 10 clean room environment; as a result, an incremental amount of capacity was added on the order of 10 to 15 percent. In 1986, the company started sampling silicon wafers in Japan.

In February 1989, damage from an accidental fire at the NBK facility in Santa Clara resulted in a loss of crystal-growing capacity. Prior to the fire, plans to upgrade the existing NBK facility had begun. Instead, NBK is building a new wafer facility with the assistance of a two-phase investment that totals $55 million from its corporate parent, Kawasaki Steel. Construction at the new 59,000-square-foot facility, located near the original wafer plant, began in July 1989. The facility is expected to produce 1.8 million prime wafers and 500,000 epitaxial wafers per year when it ramps up and will be capable of producing both 6-inch and 8-inch wafers. Production at the new facility is expected to begin in September 1990. Since the fire, NBK has reestablished crystal-growing capability to meet current customers' wafer requirements.

Komatsu Electronic Metals Co., Ltd.

Komatsu Electronic Metals is a major Japanese supplier of silicon and epitaxial wafers. Komatsu Electronic Metals was incorporated in 1960 as an affiliate of Komatsu, Ltd., the Japanese construction equipment manufacturer.

Table 2 contains the locations and plant activities of Komatsu's silicon facilities. (Please note that in Table 2, the Polysilicon heading refers to the location of a polysilicon plant. The Single-Crystal Ingots heading refers to the growth of silicon ingots at a given location. The Wafers heading refers to epitaxial wafer processing when present, in addition to the slicing, lapping, and polishing activities associated with wafer preparation.)

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Table 2

Komatsu Electronic Metals Silicon Plant Locations

Location	Polysilicon	Single-Crystal Ingots	Wafers
Head Office and Plant Hiratsuka City, Kanagawa Prefecture	X	X	X
Nagasaki Plant Omura City, Nagasaki Prefecture		X	X
Kyushu Komatsu Electric Co., Ltd. Kiyotake City, Miyazaki Prefecture			X

Source: Dataquest January 1990

Komatsu's Hiratsuka facility produces polysilicon, single-crystal silicon, and some wafers. The Kyushu Komatsu plant in Miyazaki produces most of the company's polished wafers. Komatsu's Nagasaki plant was opened in 1985 and initially produced epitaxial wafers. In 1989, Komatsu expanded its Nagasaki facility for the growth of single-crystal silicon ingots. Additional facilities at the Nagasaki plant for slicing and polishing are expected to be added during the next several years. A new clean room and additional capacity also will be added to the epitaxial wafer operations at the Nagasaki plant. Eventually, the Nagasaki facility will replace the Hiratsuka plant as Komatsu's main production site.

Komatsu supplies both Czochralski and float-zone material to the semiconductor industry. It ranks as one of the three major float-zone suppliers in the world (Shin-Etsu Handotai and Wacker are the others).

Komatsu both produces polysilicon for its own needs and purchases it from the merchant market to supplement its supply. Its polysilicon capacity is approximately 100 metric tons. Komatsu manufactures polysilicon by a proprietary method that employs monosilane gas. This method, known as the Komatsu method, uses crude silica as a source of silane gas that is refined to high purity, then decomposed into very high-purity polycrystalline silicon material. Union Carbide Corporation is the only polysilicon producer in the world that has licensed the Komatsu method. In addition to its internal usage of silane in polysilicon production, Komatsu Electronic Metals is also a major supplier of high-purity silane to the semiconductor industry for processing applications such as epitaxy and chemical vapor deposition (CVD).

Mitsubishi Metal Corporation

Mitsubishi Metal Corporation is a multibillion dollar, multinational corporation headquartered in Tokyo. (Mitsubishi Metal and Mitsubishi Electric Corporation, the semiconductor manufacturer, both are members of the same industrial group, the Mitsubishi Group.) Mitsubishi Metal Corporation has two subsidiaries that are silicon wafer manufacturers: Japan Silicon (also known as JASIL or Nippon Silicon) and Siltec Corporation, which was acquired in 1986. In addition to silicon wafers, Mitsubishi Metal is a major supplier of gallium arsenide wafers to the semiconductor industry.

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Japan Silicon

Japan Silicon is a major Japanese supplier of silicon and epitaxial wafers. A brief history of the company's name is as follows: Japan Electronic, part of Mitsubishi Metal, merged with Chisso Denshi to form a silicon operation called Toyo Silicon (Toyo means Asia in Japanese). In the early 1980s, Toyo Silicon's name was changed to Japan Silicon, which is often shortened to JASIL.

Table 3 gives the location of Japan Silicon's manufacturing facilities and plant activities. Both the Ikuno and Noda facilities have single-crystal silicon operations and wafer production. The Noda Plant produces 3-inch to 200mm wafers, whereas the Ikuno Plant produces 125mm and 150mm wafers. Yamagata Silicon in Yonezawa obtains ingots of single-crystal silicon from its sister plants and produces 100mm to 150mm wafers. Dataquest believes that Japan Silicon recently expanded its Yonezawa facility for the production of 200mm wafers. Epitaxial wafer activity takes place at the Noda Plant.

Japan Silicon obtains most of its polysilicon materials from Hi-Silicon Co., Ltd. (also known as Kojundo Silicon), located in Yokkaichi City, Mie Prefecture. Hi-Silicon was formed in 1967 as a joint venture between Mitsubishi Metal and Osaka Titanium Company (OTC). Through this joint venture, Japan Silicon and OTC have been entitled to equal amounts of polysilicon capacity at the Hi-Silicon facility, which has a total capacity of 1,080 metric tons. In October 1987, Osaka Titanium announced that it had sold its 50 percent position in Hi-Silicon to Mitsubishi Metal for an undisclosed sum. In addition to its interest in Hi-Silicon, Mitsubishi Metal Corporation has a 12.25 percent equity position in Dow Corning's polysilicon subsidiary, Hemlock Semiconductor.

Table 3

Japan Silicon Plant Locations

Location	Polysilicon	Single-Crystal Ingots	Wafers
Ikuno Plant Asaki District, Hyogo Prefecture		X	X
Noda Plant Noda City, Chiba Prefecture		X	X
Yamagata Silicon Yonezawa City, Yamagata Prefecture			X
Hi-Silicon Yokkaichi City, Mie Prefecture	X		

Source: Dataquest
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Siltec Corporation

Siltec Corporation (Menlo Park, California) consists of two business units: Siltec Silicon, a merchant silicon wafer supplier; and Cybeq Systems, a manufacturer of production, transport, and test equipment used in silicon production operations. The company was founded in 1969 by Robert Lorenzini, a recognized pioneer in the field of crystal growing.

In September 1986, Siltec Corporation agreed to an acquisition by Mitsubishi Metal Corporation of Japan for approximately $33 million. The acquisition included both Siltec Silicon and Cybeq Systems. The acquisition was financed 60 percent by Mitsubishi Metal, 30 percent by Mitsubishi Mining and Cement, and 10 percent by Mitsubishi Corporation.

Siltec began operations in Salem, Oregon, in October 1982. In mid-1985, Siltec's California silicon production facilities were relocated and consolidated in Salem from operations in Menlo Park and Mountain View. In November 1987, Siltec announced a 60 percent phased expansion and modernization program for the Salem facility. The $30 million modernization program was completed in 1988. In February 1988, the company announced its decision to construct an epitaxial wafer facility adjacent to the Salem wafer plant. The new epi facility came on-line in summer 1989. Prior to the completion of its new epi facility in Oregon, Siltec supplied epitaxial wafers through a manufacturing and technology agreement with Japan Silicon, Siltec's sister company in Japan.

In the mid-1980s, Siltec expanded its activities overseas through joint venture and technology licensing strategies. In 1984, Siltec entered into an agreement with Rhone-Poulenc of France to manufacture silicon wafers in France for distribution to semiconductor manufacturers in Western Europe. The joint venture, Rhone-Siltec, began pilot production in September 1985 at a facility near Mantes-la-Jolie (100 kilometers west of Paris). Rhone-Siltec, with a capacity of 20 MSI, focused on wafer slicing, polishing, and lapping operations. In the fourth quarter of 1987, the company closed its facility after three years of operation because the company was unprofitable.

In October 1985, Siltec announced the licensing of its silicon technology to Lucky Advanced Materials, Inc. (LAMI), of South Korea, an affiliate of the Lucky-Goldstar group. Lucky Advanced Materials agreed to pay Siltec $4 million plus royalties for the technology. The LAMI silicon facility, located in Gumi, began production in February 1987. The LAMI plant has both single-crystal silicon growth and wafer production operations.

Nittetsu Denshi

Nittetsu Denshi is a new company supplying the semiconductor industry with silicon and epitaxial wafers. The company was established as a wholly owned subsidiary of Nippon Steel in June 1985. (Note: Nittetsu Denshi is also referred to as NSC Electron Corporation; NSC stands for Nippon Steel Corporation and denshi refers to electronics.) The silicon wafer facility is in Hikari City, Yamaguchi Prefecture. Sampling of CZ polished wafers began in the fall of 1986, with production wafers available in April 1987. Nittetsu Denshi is focusing on 125mm and 150mm wafers. Epitaxial wafer sampling commenced in the latter half of 1987.

Nippon Steel, Nittetsu Denshi's parent, is one of several Japanese steel manufacturers diversifying from its traditional sunset industry, steel, into the sunrise industries, such as electronic materials. In addition to financial backing, the steelmaker provides its new venture with a strong background in support technologies for silicon manufacturing, such as molten materials processing, crystal growth control, and precision measurement.

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Osaka Titanium Company

Osaka Titanium Company (OTC) is a major Japanese supplier of silicon and epitaxial wafers. OTC is part of the Osaka Titanium Group along with Kyushu Electronic Metals Co. OTC is a fully integrated producer of silicon from trichlorosilane (source material for polysilicon) to the finished wafer. Table 4 shows the locations and activities of silicon facilities within the Osaka Titanium Group, including U.S. Semiconductor, and the company's most recent acquisition, Cincinnati Semiconductor (formerly Cincinnati Milacron's epitaxial wafer division). Not shown in Table 4 is OTC Semiconductor Corporation, the company's North American sales and service organization, located in Fremont, California.

In Japan, OTC produces both silicon (Czochralski and float-zone) and epitaxial wafers. OTC started research on silicon for semiconductor applications in 1957 and built its first polysilicon facility in 1960. In 1984, OTC completed a new poly facility in Amagasaki (approximate capacity of 720 metric tons per year).

Until recently, OTC also had access to polysilicon capacity at Hi-Silicon located in Yokkaichi City, Mie Prefecture. Hi-Silicon (also known as Kojundo Silicon) was established in 1967 as a joint venture between Mitsubishi Metal and Osaka Titanium Company in which both companies shared equally in the 1,080-metric-ton capacity of the Hi-Silicon plant. In October 1987, Osaka Titanium announced that it had sold its 50 percent position in Hi-Silicon to Mitsubishi Metal for an undisclosed sum.

Kyushu Electronic Metal Co., Ltd., was established in 1973, with OTC and Sumitomo Metal Industries as the major stockholders. All of OTC's wafers are produced at the Kyushu Electronic Metal facilities in the Saga Prefecture. Kyushu Electronic Metal's first wafer facility was built in 1975; its newest silicon plant, in Imari City, was completed in 1984. The Imari Plant has the capability of manufacturing 125mm, 150mm, 200mm, as well as 250mm wafers.

Table 4

Osaka Titanium Group Silicon Plant Locations

Location	Polysilicon	Single-Crystal Ingots	Wafers
Osaka Titanium Company			
Head Office and Plant			
Amagasaki, Hyogo Prefecture	X	X	
Kyushu Electronic Metal Co., Ltd.			
Head Office and Plant			
Kishima District, Saga Prefecture		X	X
Imari Plant			
Imari City, Saga Prefecture			X
Cincinnati Semiconductor			
Maineville, Ohio		X	X
U.S. Semiconductor			
Fremont, California			X

Source: Dataquest January 1990

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Asia/Pacific Activities

In 1988, OTC and Tatung, a Taiwanese-based manufacturer of silicon ingots and wafers, reached an agreement for OTC to supply equipment and technology to Tatung in exchange for OTC using Tatung's silicon facilities as a foundry for local wafer production. Initial production is targeted at semiconductor manufacturers in Asia/Pacific. Eventually, OTC may sell wafers produced by the Tatung foundry in other regional markets such as the United States and Japan.

Cincinnati Semiconductor

In December 1988, OTC announced that it was negotiating to purchase the semiconductor materials division of Cincinnati Milacron, one of the largest suppliers of epitaxial wafers in the United States. (In February 1988, the corporate office of Cincinnati Milacron announced a reorganization strategy that included plans to sell its epi wafer division in addition to restructuring its machine-tools and robot operations.) The acquisition by OTC was finalized in March 1989 and the semiconductor materials division of Cincinnati Milacron was renamed Cincinnati Semiconductor. OTC is expected to invest approximately $30 million in upgrading and expanding the Maineville, Ohio, manufacturing facility.

Historically, the majority of Cincinnati Milacron's epitaxial wafer production has been for discrete device applications, with a small percentage dedicated to CMOS epi wafers. In the past, the company has built its own epitaxial reactors, which have not been for sale on the commercial epitaxial reactor market.

U.S. Semiconductor

U.S. Semiconductor (Fremont, California) manufactures epitaxial wafers for MOS and discrete device applications. The company, founded in 1984, was privately held until its acquisition by OTC in December 1986. U.S. Semiconductor supplies the semiconductor industry with 3-inch through 150mm epi wafers. The company expanded its epitaxial wafer capacity at the Fremont facility in 1987/1988 time frame. U.S. Semiconductor and OTC Semiconductor, the company's North American sales and service organization, share the same facilities in Fremont.

Shin-Etsu Handotai

Shin-Etsu Handotai (also known as SEH) is the largest silicon and epitaxial wafer company in the world. The company was formed as a joint venture between Shin-Etsu Chemical and Dow Corning in 1967. In 1979, Shin-Etsu Chemical acquired full ownership of Shin-Etsu Handotai. Shin-Etsu Handotai's subsidiaries and affiliates include SEH America, SEH Europe, and SEH Malaysia. SEH's world headquarters are in Tokyo, and its R&D centers are in Isobe, Japan and Vancouver, Washington. In addition to silicon products, SEH manufactures gallium arsenide and gallium phosphide through a joint venture with Furukawa Mining known as Iwaki Handotai. Table 5 summarizes Shin-Etsu Handotai's silicon plant locations and activities.

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Table 5

Shin-Etsu Handotai Silicon Plant Locations

Location	Polysilicon	Single-Crystal Ingots	Wafers
Isobe Plant			
Annaka City, Gunma Prefecture	X	X	X
Nagano Plant			X
Naoetsu Plant			
Jyoetsu City, Niigata Prefecture	X		X
Saigata Plant			
Kubiki Town, Niigata Prefecture		X	
Shirakawa Plant			
Nishishirakawa, Fukushima Prefecture		X	X
Takefu Plant			
Takefu District, Fukui Prefecture		X	
Kuala Lumpur, Malaysia			X
Vancouver, Washington, United States		X	X
Livingston, Scotland, United Kingdom		X	X

Source: Dataquest
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Like several of the major silicon merchant companies, Shin-Etsu Handotai's silicon manufacturing is vertically integrated, from polysilicon to polished wafers. Polysilicon facilities are at the Naoetsu factory (part of Shin-Etsu Chemical) and the Isobe factory. Polysilicon capacity is approximately 150 metric tons per year. Shin-Etsu Handotai also has a 24.5 percent equity position in Hemlock Semiconductor, the Dow Corning polysilicon subsidiary, and obtains additional polysilicon from other vendors to supplement its needs.

Shin-Etsu Handotai is a major manufacturer of both Czochralski and float-zone material. Float-zone ingots are grown at the Isobe and Saigata facilities; Czochralski ingots at Isobe, Shirakawa, and Takefu, as well as Vancouver, Washington, and Livingston, Scotland. Shin-Etsu Handotai produces epitaxial wafers at the Isobe and Shirakawa factories in Japan, and overseas at Vancouver and Livingston. In 1988, SEH America completed an expansion of its epitaxial manufacturing capacity at the Vancouver facility. In 1988, SEH also expanded slice and polish capacity at its subsidiary in Livingston, Scotland. In third quarter 1989, SEH announced that it will be building a new facility at its silicon operations in Livingston for the production of silicon wafers used in IC device fabrication. Existing wafer production at Livingston has been focused on transistor and other discrete device applications.

Showa Denko

Showa Denko (along with Nittetsu Denshi) is one of the new entrants in the Japanese silicon market. The company began actively sampling its wafers in the third quarter of 1986.

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In addition to its silicon wafer operations, Showa Denko provides a broad mix of electronic materials to semiconductor manufacturers, including compound semiconductor materials (gallium arsenide, gallium phosphide, and indium phosphide) and high-purity specialty gases (such as silane, hydrogen chloride, boron trichloride, nitrogen trifluoride, and fluorocarbon etchants).

Showa Denko manufactures silicon at its Chichibu City facility in Saitama Prefecture. (Single-crystal ingots of gallium arsenide are also produced at this facility.) Showa Denko manufactures both Czochralski and magnetic Czochralski (MCZ) material. The company obtained its MCZ technology from Sony Corporation, a pioneer in this field. The MCZ growth method has received attention the last few years because of its ability to provide very high purity material with tight oxygen control.

Showa Denko has more than a decade of experience in compound semiconductor material manufacturing and an existing distribution network in electronic materials, factors that Showa Denko hopes will provide a competitive advantage.

Toshiba Ceramics

Toshiba Ceramics supplies both silicon and epitaxial wafers to the semiconductor industry. Dataquest understands that a significant majority of Toshiba Ceramics' wafer sales are to its semiconductor parent, Toshiba Corporation. However, Dataquest still considers Toshiba Ceramics to be a merchant silicon company because it has active marketing and sales of wafers to the merchant market in addition to supplying its semiconductor parent.

Toshiba Ceramics has a silicon manufacturing facility (Oguni Plant) in the Nishiokitama District, Yamagata Prefecture. Activities at this facility include the growth of Czochralski single-crystal silicon ingots and wafer production. Toshiba Ceramics has a joint venture with the polysilicon manufacturer, Tokuyama Soda, known as Tokuyama Ceramics (Tokuyama, Yamaguchi Prefecture). This facility produces both silicon and epitaxial wafers. In addition, Toshiba Ceramics manufactures a diverse product mix for the semiconductor industry, including ceramic materials and quartz, graphite, and silicon carbide products. Table 6 shows Toshiba Ceramics' silicon plant locations and activities.

Table 6

Toshiba Ceramics Silicon Plant Locations

Location	Polysilicon	Single-Crystal Ingots	Wafers
Oguni Plant Nishiokitama District, Yamagata Prefecture		X	X
Tokuyama Ceramics Tokuyama, Yamaguchi Prefecture			X

Source: Dataquest January 1990

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EUROPEAN SILICON COMPANIES

Huels AG

Huels AG, a diversified chemical company based in Marl, West Germany, first ventured into the silicon wafer industry in May 1987, when it was announced that its parent corporation, Veba AG of West Germany, would acquire the silicon and photoresist operations of Dynamit Nobel AG. The acquisition, part of the divestiture of Dynamit Nobel's chemical and plastics operations, included Dynamit Nobel Silicon's facilities in Merano and Novara, Italy, and Research Triangle Park, North Carolina, as well as a New Jersey-based photoresist company, Dynamit Nobel Microelectronics (formerly Petrarch Systems). The Huels division of Veba AG took over operating responsibility for the newly named operation, DNS Electronic Materials. Acquisitions and name changes are not new to DNS. Prior to DNS becoming a wholly owned subsidiary of Dynamit Nobel AG in October 1980, the company had been known as Smiel and was owned by Montedison.

In November 1988, the groundwork was laid for a second key acquisition when it was announced that Monsanto Company had signed a letter of intent concerning the sale of its silicon operations, Monsanto Electronic Materials Company, to Huels. In April 1989, Huels completed the acquisition and subsequently consolidated operations of the former Monsanto subsidiary with DNS Electronic Materials. In two short years, Huels AG went from being a virtual unknown in the market to become one of the world's largest silicon wafer suppliers. Huels' consolidated silicon operations today operate under the name of MEMC Electronic Materials. Table 7 presents a summary of the silicon plant locations and activities of MEMC Electronic Materials. The company's corporate headquarters is in St. Peters, Missouri.

Table 7

MEMC Electronic Materials Silicon Plant Locations

Location	Country	Polysilicon	Single-Crystal Ingots	Wafers	Technical Center
Merano	Italy	X	X		
Novara	Italy			X	
St. Peters, Missouri	United States		X	X	X
Spartanburg, South Carolina	United States		X	X	
Kuala Lumpur	Malaysia			X	
Utsonomiya, Tochigi	Japan			X	X

Note: The future relationship between MEMC Electronic Materials and Komil, the South Korean joint venture between Monsanto Company and Dongbu Industrial Company, is expected to be resolved in early 1990.

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Two former DNS silicon facilities are part of the new MEMC Electronic Materials organization. The Merano facility includes a polysilicon plant with approximately 700-metric-ton capacity. (This plant was expanded from 450 to 700 metric tons per year at the end of 1985.) In addition, both Czochralski and float-zone ingots are grown at the Merano facility. European wafer operations are located in Novara, where both silicon and epitaxial wafers are produced.

Four facilities, formerly part of the Monsanto silicon operations, are now part of the MEMC Electronic Materials organization. Both the St. Peters plant and the newer Spartanburg facility grow single-crystal silicon ingots and produce wafers; epitaxial wafer production is done in St. Peters. (The St. Peters facility was also the site of Monsanto's 210-metric-ton capacity polysilicon plant, which was closed in 1987.) The Malaysian wafer facility in Kuala Lumpur and the Japanese facility in Utsonomiya obtain single-crystal silicon and etched wafers from the St. Peters and Spartanburg plants to produce polished wafers for their respective local markets.

Closures

As a result of the consolidation of DNS Electronic Materials and the Monsanto silicon operations, two wafer facilities were closed in the summer of 1989: the Monsanto wafer operation in Milton Keynes, England, and the DNS facility in Research Triangle Park, North Carolina. The Milton Keynes facility became operational in 1986 and was part of Monsanto's strategy to penetrate overseas markets more effectively. Like the Monsanto facilities in Japan and Malaysia, the Milton Keynes facility obtained single-crystal silicon and etched wafers from the St. Peters and Spartanburg plants to produce polished wafers for its local market.

The DNS facility in Research Triangle Park was originally a joint venture between Dynamit Nobel Silicon and W.R. Grace. The two companies formed Dynamit Nobel Grace Silicon in late 1984 to produce silicon wafers, polysilicon, and single-crystal ingots at a new facility in North Carolina. They invested $35 million initially in the Research Triangle Park plant, which was opened in May 1985; this facility began wafer production in January 1986. In March 1986, DNS bought out the one-third interest held by Grace for approximately $10 million. The company announced, in May 1988, its plan to double the production capacity of the North Carolina plant. Expansion plans at that time had included a new building for epitaxial wafer manufacturing.

In addition to the closure of the two wafer facilities, the activities of the DNS Electronic Materials technical center, formerly in Sunnyvale, California, were consolidated with the technical center in St. Peters, Missouri.

South Korean Activities

In the mid-1980s, Monsanto Company formed a 50-50 joint venture for silicon wafer manufacturing with Dongbu Industrial Company of South Korea. The Korsil plant became operational in 1986 and is located in Gumi, adjacent to the country's developing semiconductor industry. (Please note that Korsil's silicon wafer sales are listed separately from Monsanto's sales in the section entitled "Silicon Database.")

As part of the original joint venture agreement, Dongbu has the option to buy Monsanto's 50 percent share in Korsil in the event that Monsanto's silicon operations were to be acquired. In light of the Huels acquisition, the current relationship between Dongbu and MEMC Electronic Materials is uncertain. Dongbu may choose to negotiate a new joint venture agreement with MEMC and Huels, seek another joint venture partner, or acquire the remaining 50 percent share in

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Korsil and keep it as a wholly owned subsidiary. A key issue in Dongbu's eventual decision will be concerned with obtaining a source of single-crystal silicon ingots, as the Korsil operation currently does not have crystal-pulling capability. The future status of Korsil is expected to be resolved in early 1990.

Okmetic

Okmetic is a new silicon wafer company in Espoo, Finland. The company was founded in 1985 by Outokumpu and Nokia. Outokumpu is a diversified company that specializes in metallurgy, mining, industrial equipment manufacturing, and electronics, while Nokia has several divisions that specialize in electronics, cables, machinery, metal products, engineering, chemicals, and plastics. Okmetic's silicon manufacturing capability is based on a joint research and development program between Helsinki University of Technology and Okmetic's founders. Okmetic started silicon wafer production in 1987 and currently offers polished CZ wafers from 3-inch through 150mm in diameter.

Siltronix SA

Siltronix SA is small silicon wafer company located in Geneva, Switzerland. The privately held company was established in 1970. Dataquest believes that Siltronix focuses its sales and marketing efforts on the European market.

Topsil Semiconductor Materials A/S

Topsil is a merchant silicon manufacturer in Frederikssund, Denmark. Topsil produces its own polysilicon, grows float-zone single-crystal ingots, and manufactures wafers. The company pioneered the neutron transmutation doping (NTD) technique in 1974. This technique transforms silicon atoms into phosphorus by exposing a wafer to a flux of thermal neutrons. Although the technique can form only phosphorus-doped materials, its advantage is that it can provide an extremely uniform distribution of phosphorus, thus producing wafers with well-defined resistivity profiles.

Wacker

Wacker is a major supplier of silicon and epitaxial wafers to the semiconductor industry. Wacker is the name used in this study to refer to the collective silicon operations of Wacker Chemie GmbH of West Germany, which is owned equally by Hoechst AG and Dr. Alexander Wacker Familliengesellschaft GmbH. Wacker Chemie first started its research into high-purity silicon materials in 1953 and established Wacker Chemitronic at Burghausen, West Germany, in 1968. Wacker Siltronic, established in 1978, is a U.S. subsidiary of Wacker Chemie and an affiliate of Wacker Chemitronic. Wacker's silicon plant locations and activities are shown in Table 8.

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Table 8

Wacker Silicon Plant Locations

Location	Polysilicon	Single-Crystal Ingots	Wafers
Wacker Chemitronic			
Burghausen, West Germany	X	X	X
Wasserburg, West Germany			X
Wacker Siltronic			
Portland, Oregon		X	X

Source: Dataquest January 1990

Wacker's Burghausen facility has a polysilicon capacity of approximately 3,200 metric tons per year. In addition, extensive single-crystal growth operations, both Czochralski and float-zone, and wafer production, silicon and epitaxial, occur at Burghausen. Wacker is a recognized leader in the field of float-zone silicon material. In the summer of 1988, Wacker acquired Fairchild's facility in Wasserburg, West Germany. The plant in Wasserburg is used primarily for polishing and epitaxial processing of 150mm and 200mm wafers. Dataquest believes that wafer production at Wasserburg began in 1989. In addition to producing semiconductor substrate materials—silicon and gallium arsenide—Wacker Chemitronic established a subsidiary, Heliotronic GmbH, in 1977, to research and manufacture solar-grade silicon. Wacker Chemitronic is also a major manufacturer of chlorosilanes and ultrapure hydrogen chloride.

In the United States, Wacker Siltronic produces silicon single-crystal ingots and wafers at its Portland, Oregon, facility. Wacker Chemicals East Asia, established in Tokyo in 1982, serves as a marketing and sales arm for Wacker Chemie in Japan and the Pacific Rim.

REST OF WORLD SILICON COMPANIES

Dataquest has identified five ROW silicon companies—two in South Korea and three in Taiwan—that represent a growing domestic supplier base in the newly industrialized countries of the Pacific Rim. This section of our study briefly examines the activities of these five merchant silicon companies. In addition, silicon wafer activities in Brazil and India are discussed.

South Korea

Korsil

Korsil Company, Ltd., was formed in the mid-1980s as a 50-50 joint venture between Monsanto Company and Dongbu Industrial Company. The Korsil plant became operational in 1986 and is located in Gumi, adjacent to the country's developing semiconductor industry. As part of the original joint venture agreement, Dongbu has the option to buy Monsanto's 50 percent share in Korsil in the event that Monsanto's silicon operations were to be acquired. In light of the Huels acquisition of the Monsanto silicon operations in early 1989, the current status of Korsil is uncertain. Dongbu may choose to negotiate a new joint venture agreement with the new Huels

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silicon organization, seek another joint venture partner, or acquire the remaining 50 percent share in Korsil and keep it as a wholly owned subsidiary. A key issue in Dongbu's eventual decision concerns obtaining a source of single-crystal silicon ingots, as the Korsil operation currently does not have crystal-pulling capability. The future status of Korsil is expected to be resolved in early 1990.

Lucky Advanced Materials, Inc.

In October 1985, Siltec announced the licensing of its silicon technology to LAMI, of South Korea. Lucky Advanced Materials agreed to pay Siltec $4 million plus royalties for the technology. The LAMI silicon facility, located in Gumi, began production in February 1987. The LAMI plant has both single-crystal silicon growth and wafer production operations.

Taiwan

Three silicon wafer companies are located in Taiwan—Hermes Epitaxy, Sino-America, and Tatung Company. Hermes Epitaxy produces epitaxial wafers, while Sino-America produces single-crystal ingots and CZ wafers. Both companies have wafer facilities in Hsinchu. Tatung Company is a large, diversified electronics firm; its silicon manufacturing facility is located in Taipei. In 1988, Osaka Titanium Company and Tatung reached an agreement for OTC to supply equipment and technology to Tatung in exchange for OTC using Tatung's silicon facilities as a foundry for local wafer production. Initial production is targeted at semiconductor manufacturers in the Asia/Pacific region. Eventually, OTC may sell wafers produced by the Tatung foundry in other regional markets such as the United States and Japan.

Others

Brazil

Heliodinamica of Sao Paolo, Brazil, began production of silicon wafers for semiconductor device fabrication in 1988. The solar energy company originally manufactured silicon wafers for photovoltaic applications but now has expanded its capability to service the Brazilian microelectronics industry. The crystal growth and wafer technology employed by Heliodinamica was developed in Brazil.

India

Metkem Silicon, Ltd., in Mettur, India, manufactures polysilicon and has plans to produce silicon wafers for semiconductor device fabrication. Another plan for polysilicon production in India was dropped by the government in late 1987. The national silicon factory project, which was planned to have a capacity of 200 metric tons per year, was being developed in conjunction with Hemlock Semiconductor, a major U.S. polysilicon manufacturer.

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DEPARTURES

Gensil

Until it ceased operations in September 1987, Gensil was a small silicon wafer company located in Garland, Texas. It manufactured silicon wafers to custom specifications for discrete device applications (such as zener diodes, which require tight resistivity profiles) and provided silicon substrate suitable for epitaxial deposition. Gensil was closed by its corporate parent, General Semiconductor Industries, a Tempe, Arizona, semiconductor device company that manufactures discrete devices such as diodes and switching and power transistors. Gensil provided silicon wafers from 1 inch to 100mm in diameter.

Silicon Services

Silicon Services (Santa Clara, California) was a small, epitaxial wafer supplier in the Silicon Valley. (Dataquest believes that the company closed its operations in 1986.) Its primary product was epitaxial wafers for power transistors; other application markets included epitaxial wafers for bipolar processing and a small amount of CMOS. Silicon Services did not grow its own substrate material. Instead, it purchased from other merchant silicon companies or obtained the material directly from its customers (as in the case of bipolar applications where the customer had already prepared a buried layer, followed by ion implantation). Silicon Services supplied epitaxial wafers between 2 inches and 125mm.

Rhone-Siltec

In 1984, Siltec Corporation entered into an agreement with Rhone-Poulenc of France, one of the world's largest chemical companies, to manufacture silicon wafers in France for distribution to semiconductor manufacturers in Western Europe. The joint venture, Rhone-Siltec, began pilot production in September 1985 at a facility near Mantes-la-Jolie (100 kilometers west of Paris). Rhone-Siltec, with a capacity of 20 MSI, focused on wafer-slicing, polishing, and lapping operations. In the fourth quarter of 1987, the company closed its facility after three years of operation because the company was unprofitable.

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Semiconductor Gases—Products and Applications

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Semiconductor Gases
Products and Applications

INTRODUCTION

In the semiconductor industry, process gases represent one category of consumable materials that are used throughout the fabrication of semiconductor devices, from the growing of single silicon crystals, through the many steps of wafer fabrication, to the final stages of assembly and packaging.

This study presents an overview of the semiconductor gas industry. It discusses the different gas product categories, gas applications in semiconductor fabrication, gas production, and distribution networks. An appendix on unit conversion factors for volumes and weights commonly used to describe semiconductor gases is included. Please refer to the study, "Semiconductor Gas Companies," located behind the Semiconductor Materials tab in this binder for information on the companies that participate in this segment of the electronic materials industry.

PRODUCT CATEGORIES

Gases used in the semiconductor industry are divided into two general categories: bulk gases and specialty gases.

Bulk gases include nitrogen, oxygen, hydrogen, and argon. The designation of "bulk" typically refers to a discrete delivery of a large volume of a given gas by truck transport. These gases usually are delivered via tanker trucks as cryogenic liquids because of the efficiency of transportation and storage prior to the vaporization stage at the semiconductor manufacturer's facility. In some cases, when a semiconductor manufacturer has insufficient volume demand or uneven patterns of usage, bulk gases are transported via tube trailers in a gaseous, rather than liquid, state. Nitrogen gas provided through direct pipeline delivery, as well as customer on-site nitrogen generation plants, is also considered as part of the bulk gas category, even though the supply of nitrogen, in this sense, cannot be classified as discrete.

There are a large number of gases (more than 35) that can be classified as specialty gases. For that reason, a further segmentation of this category is necessary and is based on the chemical reactivity and functionality of the various specialty gases. Dataquest segments the specialty gas market into six categories: silicon-precursor gases, dopants, etchant gases, reactant gases, atmospheric/purge cylinder gases, and others. Specialty gases are used in comparatively smaller volumes than the bulk gases and, thus, are delivered in high-pressure cylinders.

Table 1 contains a comprehensive list of the bulk and specialty gases that are used in semiconductor manufacturing. Note that nitrogen and other atmospheric gases appear in one of the specialty gas categories as well as under the bulk gas designation. The distinction in this case is that these gases are supplied in gas cylinders rather than in discrete deliveries of large volumes of bulk liquid. These cylinders of gas are used in general device manufacturing when small volumes of gas are required in areas of the fab not generally accessible to the house supply lines. In addition, atmospheric/purge gases in cylinders are used for purging certain processing systems and equipment in cases when a semiconductor manufacturer is concerned about possible back-contamination of the house lines of nitrogen and argon.

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Table 1

Bulk and Specialty Gases Used in Semiconductor Manufacturing

I. Bulk Gases

Nitrogen, N_2	Hydrogen, H_2
Oxygen, O_2	Argon, Ar

II. Specialty Gases

A. Silicon-Precursor Gases

Silane, SiH_4	Dichlorosilane, SiH_2Cl_2
Trichlorosilane, $SiHCl_3$	Silicon Tetrachloride, $SiCl_4$

B. Dopant Gases

Arsine, AsH_3	Boron Trifluoride, BF_3
Phosphine, PH_3	Phosphorous Pentafluoride, PF_5
Diborane, B_2H_6	

C. Etchant Gases

Carbon Tetrafluoride, CF_4	(Halocarbon-14)
Fluoroform, CHF_3	(Halocarbon-23)
Hexafluoroethane, C_2F_6	(Halocarbon-116)
Dichlorodifluoromethane, CCl_2F_2	(Halocarbon-12)
Bromotrifluoromethane, $CBrF_3$	(Halocarbon-13B1)
Chlorotrifluoromethane, $CClF_3$	(Halocarbon-13)
Chloropentafluoroethane, C_2ClF_5	(Halocarbon-115)
Methyl Fluoride, CH_3F	(Halocarbon-41)
Trichlorofluoromethane, CCl_3F	(Halocarbon-11)
Perfluoropropane, C_3F_8	
Boron Trichloride, BCl_3	
Chlorine, Cl_2	
Carbon Tetrachloride, CCl_4	
Silicon Tetrafluoride, SiF_4	
Sulphur Hexafluoride, SF_6	
Nitrogen Trifluoride, NF_3	
Others	

D. Reactant Gases

Ammonia, NH_3	Nitrous Oxide, N_2O
Hydrogen Chloride, HCl	Carbon Dioxide, CO_2

E. Atmospheric/Purge Cylinder Gases

Nitrogen, N_2	Oxygen, O_2
Hydrogen, H_2	Argon, Ar
Helium, He	

F. Other Gases

Tungsten Hexafluoride, WF_6	Germane, GeH_4
Others	

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APPLICATIONS

Bulk Gases

Nitrogen

Nitrogen is the most widely used gas in the semiconductor industry, in both wafer fabrication as well as assembly operations. Its consumption by volume represents approximately 95 percent of all bulk gases used in semiconductor manufacturing. Its primary application is in providing an inert atmosphere for the various wafer processing systems such as epitaxial reactors, chemical vapor deposition (CVD) reactors, and diffusion furnaces. Nitrogen is used as a transportation medium in some wafer processing equipment. In addition, it is used as an inert environment during the exposure of negative photoresist in lithography because of the necessity to minimize competitive oxygen side reactions that can lead to film thickness losses. Nitrogen is also used to maintain the integrity of various pieces of processing equipment, such as furnace banks, even while they are not in direct production use. In some facilities, certain clean stations are equipped with constant flows of nitrogen to maintain ultraclean conditions. Many other pieces of equipment in a fab use nitrogen, including blow guns, pneumatic-actuated valves, spin rinse dryers, dessicators, and cryo pumps used for condensing contaminants in vacuum systems. Because of the emphasis on the use of high-purity materials in the semiconductor industry, nitrogen purity is typically "five nines" (99.999 percent) to "six nines" purity.

Hydrogen

Hydrogen is most commonly used as an ambient environment for the growth of epitaxial layers. It is also used as a carrier gas during diffusion processes to provide a reducing environment in such reactions as the conversion of boron trichloride to atomic boron.

Hydrogen is used with oxygen in oxidation processes to form water vapor at oxidation temperatures in what is called a wet-ox (wet oxidation) process. Typically, silicon and oxygen react directly to form silicon dioxide, but the formation of thicker oxide layers requires prohibitive amounts of production time. When silicon reacts with water vapor to produce silicon dioxide and hydrogen, the oxide layer forms at an increased rate due to the relatively fast diffusion of a hydroxyl species. Hydrogen that has been included in the silicon dioxide film is driven off by subsequent heating steps such as diffusion, and densification of the oxide occurs.

Hydrogen consumption represents a few percent by volume of the bulk gases used in the semiconductor industry.

Oxygen

Oxygen has the capability to form oxides with all elements except inert gases. In wafer fabrication, it is used to form dielectric and passivation layers of silicon dioxide (SiO_2) on silicon substrates (MOS devices, in particular). It is also used as a component in certain halocarbon plasma etch mixtures such as carbon tetrafluoride (CF_4) and oxygen for the etching of silicon dioxide and silicon nitride layers. Its usage represents 1 percent or less by volume of the bulk gases consumed by the semiconductor industry.

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Argon

Argon is used by the semiconductor industry primarily as an inert environment for the growth of single-crystal silicon and also has applications in sputtering and ion implantation. There is currently a trend toward increased usage of argon in the annealing process for thin gate oxides because of the truly "inert" nonreactive nature of the gas. Argon costs more than nitrogen, which has been the traditional choice for an inert environment in this process. However, the extra expense at such a late stage of fabrication is considered minimal compared with potential device failure, and hence lower yields, caused by chemical contamination during the annealing process.

Argon consumption represents 1 percent or less of the total volume of bulk gases consumed by the semiconductor industry; consumption is split between usage in single silicon crystal growth and fabrication processing.

Specialty Gases

Silicon-Precursor Gases

The silicon-precursor gases such as silane, dichlorosilane, trichlorosilane, and silicon tetrachloride are used in epitaxial and CVD processes to deposit layers of silicon or silicon compounds (i.e., silicon dioxide, silicon nitride) onto silicon substrates. Silane, in particular, is used in plasma-enhanced CVD (PECVD) for the deposition of amorphous and polysilicon layers. Dichlorosilane is also a primary source for the deposition of polysilicon.

Silicon epitaxial layers are formed in reactions based on mechanisms of thermal decomposition or reduction by hydrogen, depending on the silicon-precursor reactant gas. Each of the silicon-precursor gases has epitaxial processing advantages and disadvantages, which include the processing temperature range, degree of autodoping, and growth rates. Silane is a pure gaseous source, while silicon trichloride and silicon tetrachloride are both corrosive liquids at room temperature and pressure. Dichlorosilane is in a gaseous state at a pressure of 0.5 atmosphere.

A layer of silicon dioxide is formed when silane and oxygen react together in an oxidation process. The other silicon-precursor gases form oxide layers when they undergo hydrolysis (reaction with water) in a moist atmosphere.

Oxidation

$$SiH_4 + O_2 \longrightarrow SiO_2 + 2H_2$$

Hydrolysis

$$SiH_2Cl_2 + 2H_2O \longrightarrow SiO_2 + 2HCl + 2H_2$$

$$SiHCl_3 + 2H_2O \longrightarrow SiO_2 + 3HCl + H_2$$

$$SiCl_4 + 2H_20 \longrightarrow SiO_2 + 4HCl$$

Silane and dichlorosilane both react with ammonia to form passivation layers of silicon nitride.

$$3SiH_4 + 4NH_3 \longrightarrow Si_3N_4 + 12H_2$$

$$3SiH_2Cl_2 + 4NH_3 \longrightarrow Si_3N_4 + 6HCl + 6H_2$$

As mentioned previously, each of the silicon-precursor gases has processing advantages and disadvantages. The safety issue is particularly important with regard to silane as it is a pyrophoric gas, which means that it will burn upon exposure to air. Silicon tetrachloride ("siltet") on the other

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hand, while corrosive, is not classified as toxic nor does it ignite in air. However, it does require the highest operating temperature of all the silicon-precursor gases for epitaxial deposition. In addition, unlike silane, siltet can cause pattern shifts in epitaxial layers due to the formation of chlorine radicals.

The chemical characteristics of dichlorosilane and trichlorosilane fall between those of silane and silicon tetrachloride. Both operate in an intermediate temperature range between silane and siltet. While toxic and corrosive, neither one is considered pyrophoric. In addition, both can cause some degree of pattern shift in epitaxial deposition.

Dopant Gases

Dopant gases are used as a source of controllable impurities within semiconductor devices. A known concentration and type of impurity (n or p) is introduced into specific regions to modify local electrical properties of the medium. Specifically, an element contributes either an excess hole (p dopant) or electron (n dopant) to the local structure of the crystal lattice, which in turn alters the conductivity of the material. For silicon, the p and n dopants are found in Groups III and V, respectively, of the periodic table. Dopants are available in liquid, solid, and gaseous states. The common gaseous n dopants are arsine and phosphine, while the common gaseous p dopant is diborane. Dopants are utilized in epitaxial deposition, diffusion, and ion implantation.

(Note: In addition to diborane, boron trichloride can be used as a p-dopant source material. This gas is also used in the chemical vapor deposition of borophosphosilicate glass (BPSG). For purposes of classification, however, Dataquest classifies boron trichloride as an etchant gas, because its usage in semiconductor manufacturing is predominately in the area of metal etch.)

In diffusion processes, the dopant gas, which is frequently mixed with nitrogen or hydrogen, is introduced into a high-temperature oven and is incorporated into the substrate by a diffusional mechanism. A dopant concentration gradient in the substrate material is established and the depth of diffusion is controlled by process time and temperature.

The common carrier gases for dopants in diffusion processes are nitrogen and hydrogen, as mentioned previously, although argon and helium are also used. Arsine and phosphine may be supplied to a semiconductor manufacturer as pure gases or as premixed dilutions with these carrier gases. Arsine and phosphine premixed with silane are also available. As diborane is extremely unstable in its pure form, and decomposes at a rate of 0.5 percent per day at room temperature, it is always supplied to semiconductor manufacturers diluted with other gases; typically, 15.0 percent diborane in nitrogen, hydrogen, argon, or helium.

Arsine, phosphine, and diborane gases are all highly poisonous materials. Arsine has a disagreeable garlic-like odor, and inhalation of as little as 0.5 parts per million is considered to be dangerous. Phosphine has an unpleasant odor of decaying fish and will react violently in the presence of an oxygen environment. Diborane is described as having a repulsive, sickly sweet odor and is spontaneously flammable in air above a temperature of 40°C. However, in the presence of certain contaminants, the ignition of diborane/air mixtures may occur at or even below room temperature. For these reasons and other safety issues, primary manufacturing of these gases is limited to only a handful of companies.

Ion implantation, and more recently neutron transmutation, offer a substantial amount of processing control over diffusion. In ion implantation, the dopant atoms are ionized and accelerated to high energies. The ion beam is directed and focused onto the wafer and the high-energy

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ions penetrate the surface. Ion implantation offers a great deal of process control because ion current and implant time can both be measured, and thus the number (dosage) of dopant ions incorporated into the material as well as the concentration profile can be determined. In ion implantation, room temperature processing minimizes dopant migration in the substrate, particularly beneath critical gate structures. Because the dopant profile can be controlled, smaller line geometries can be achieved. In addition to arsine and phosphine, boron trifluoride and phosphorous pentafluoride are also used as dopant source gases in ion implantation.

One disadvantage to ion implantation compared with diffusion is that as the dopant ions collide with the wafer, a significant amount of damage can occur to the crystal lattice. Most of this damage, however, can be later repaired in subsequent annealing steps.

There is an increasing trend away from diffusion and toward ion implantation as a doping procedure for the small-geometry devices because of the greater degree of process control. This trend is having some impact on the gas industry since the diffusion process consumes large amounts of nitrogen in addition to the dopant source gases. However, it is unlikely that diffusion will completely disappear in the future, but rather, will likely remain a standard technique for introducing dopant materials in the larger-geometry devices.

Neutron transmutation doping (NTD) is a relatively new technique for n-type doping that primarily has been limited to high-power applications. In this process, silicon wafers are placed in a nuclear reactor and a stream of thermal neutrons is passed through them. Some of the silicon atoms in the lattice are altered to phosphorous through a nuclear mechanism. While the technique can only form phosphorous-doped materials, it has its advantages in that it can provide an extremely uniform distribution of phosphorous in silicon. In addition, no external source of dopant material is required, as the silicon provides its own. One disadvantage, however, is that access to a nuclear reactor is required. Currently this technique is still quite limited in its applications and production capability. However, it may prove to be a viable alternative for doping semiconductor devices at some future time.

Etchant Gases

A wide variety of gases, primarily halocarbons, are used in etching processes. The choice of gases is strongly dependent on the ability of a given mixture of gases to selectively etch one film in the presence of another with a sufficient degree of profile control. The advantages of plasma etch over wet etching techniques include the ability to generate anisotropic (i.e., sharp-walled) as well as isotropic (curved-walled) profiles. In addition, loss of photoresist adhesion is minimized in plasma compared with wet etch. Also, because the etching materials are gases, smaller quantities of reagents are used and thus smaller amounts of waste chemicals are generated.

From a conceptual point of view, plasma etch is a fairly simple process. A highly reactive gaseous species is generated that reacts with the wafer surface to produce a volatile etch product. For most semiconductor materials and metals, the plasma is used as a source of halogen atoms to generate volatile halide etch products. The etching of organic films is best achieved when the plasma provides a source of oxygen atoms to form volatile products such as carbon monoxide (CO).

It is difficult to establish a quantitative relationship to describe the consumption of halocarbon gases in the plasma etch process, since the physical and chemical mechanisms that determine plasma etch efficiency are still not fully understood. For that reason, plasma etch has been

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described as more of an art than a science, and most process engineers exercise a great deal of freedom in establishing their own unique plasma etch gas mixtures.

Carbon tetrafluoride (CF_4) is probably the most commonly used plasma etch gas. It is an odorless, colorless gas that is stable and nontoxic. It is capable of etching silicon in both its pure gaseous form and when mixed with oxygen. It is also known as tetrafluoromethane, halocarbon-14, or Freon-14. (Freon is a registered trademark of Dupont.) Fluoroform (CHF_3, trifluoromethane, halocarbon-23) and hexafluoroethane (C_2F_6, halocarbon-116) are also used in large quantities.

(Note: In second quarter 1988, DuPont, a major primary manufacturer of carbon tetrafluoride and other fluorocarbon gases, announced its intention to phase out production of its fully halogenated chlorofluorocarbon gases. These materials have been linked to the depletion of the earth's ozone layer. This decision would affect five gases commonly used in semiconductor etch processing: CCl_3F, CCl_2F_2, $CClF_3$, C_2ClF_5, and $CBrF_3$. A firm timetable on the phaseout of these gases has not yet been established. The widely used etchant gases—CF_4, CHF_3, and C_2F_6—are not affected by this decision.)

Please refer to Table 1 for a comprehensive list of etchant gases. The following sections provide examples of the gases that specifically are used to etch silicon and polysilicon, silicon dioxide and nitride, silicides, metals, and photoresist.

Etching of Silicon and Polysilicon. For any given plasma etch mixture, it is very important to be able to selectively etch one film in the presence of another. Selectivity for isotropic etching of silicon and polysilicon in the presence of oxide is very high when using the fluorine-source plasmas (such as CF_4/O_2, SiF_4, SF_6, and NF_3). Typically, anisotropic profiles are difficult to achieve when using fluorine sources however, a high degree of anisotropy can be obtained with plasmas that produce chlorine and bromine atoms (Cl_2, Cl_2/C_2F_6, $CClF_3$, C_2F_6, Br_2, and $CBrF_3$).

It is believed that the underlying mechanism for achieving such anisotropic profiles may be the physical ion bombardment of the surface. Isotropic profiles are easier to obtain when etching silicon and polysilicon with fluorine sources, and are believed to be due to chemical etching by fluorine atoms.

Etching of Silicon Dioxide and Nitride. The gases that are used to etch silicon dioxide and nitride in the presence of silicon include CF_4/H_2, CHF_3, and C_2F_6. It has been established empirically that high degrees of selectivity for etching oxide and nitride layers are achieved by the addition of fluorine scavengers such as methane, ethylene, and hydrogen, thereby establishing a fluorine-deficient chemical environment. The underlying chemistry is not clearly understood, and the fine-tuning of feed gases to the plasma discharge is still empirical in nature.

Etching of Silicides. Silicides of titanium (Ti), tantalum (Ta), molybdenum (Mo), and tungsten (W) are commonly etched with a mixture of CF_4 and O_2. Highly volatile silicon tetrafluoride (SiF_4) is produced, as well as moderately volatile metal fluorides. Isotropic as well as anisotropic profiles have been reported. Dataquest expects this area of plasma etch to continue to receive attention with the increasing trend toward CVD-tungsten silicide applications in MOS devices.

Etching of Metals. In etching metal layers, it is critical that water vapor and oxygen be excluded from the plasma reactor (or possibly scavenged) because of the formation of native metal

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oxides at the surface. Chlorocarbon and fluorocarbon gases are typically used to etch metal films rather than pure halogens because of their ability to reduce the native oxides chemically. Nitrogen trifluoride (NF_3) is helpful in increasing selectivity over silicon dioxide films.

Aluminum and chromium do not form volatile metal fluorides, and therefore, etching of these metals is best carried out in plasmas that generate chlorine atoms. Boron trichloride (BCl_3) and silicon tetrachloride ($SiCl_4$) form radicals that react with the native metal oxide. Once the native oxide has been removed, aluminum may be etched spontaneously in a pure chlorine environment. Both anisotropic and isotropic etches can be achieved depending upon the amount of molecular chlorine in the plasma mixture. In addition to their etchant capabilities, both boron trichloride and silicon tetrachloride are efficient scavengers of oxygen and moisture.

Etching of Photoresist. Photoresist and organic films are often stripped by plasma systems that generate atomic oxygen. Rare gases and CF_4 are added to stabilize the discharge and enhance the reactivity of the organic material. The discharge produces such etch products as carbon monoxide, carbon dioxide, and water. If the plasma is rich in atomic oxygen, high selectivities over silicon dioxide, silicon nitride, and metals can be achieved.

Reactant Gases

Reactant gases include ammonia, hydrogen chloride, nitrous oxide, and carbon dioxide. Ammonia is typically used with either silane or dichlorosilane to produce silicon nitride layers in chemical vapor deposition. Silicon nitride films are used as passivation layers or interlayer dielectrics in semiconductor devices. Ammonia is a corrosive, alkaline gas that is considered toxic. It is generally regarded as nonflammable and has a distinctive pungent odor.

Hydrogen chloride is used to polish and etch wafers prior to deposition steps by removing defects on the wafer surface due to mechanical polishing and handling of the wafer. A significant development in thermal oxidation has been the use of hydrogen chloride in combination with oxygen. Hydrogen chloride is particularly effective in gettering mobile sodium ions and other impurities in the wafer, which in turn helps minimize leakage in the MOS gate threshold voltage. Hydrogen chloride is a colorless, corrosive, nonflammable, acidic gas that has a repulsive odor. Because of its corrosive nature, special attention must be focused to maintain the purity of the gas. In particular, contamination can result from the interaction between hydrogen chloride and the walls of gas cylinders.

Nitrous oxide and carbon dioxide are both used as sources of oxygen in silicon oxide films formed in chemical vapor deposition processes. Nitrous oxide is available as a liquefied gas. It has a sweet odor and is generally used as an anesthetic. It is commonly known as "laughing gas." However, nitrous oxide becomes a strong oxidizing agent at temperatures greater than 300°C. Carbon dioxide is a colorless, odorless, noncombustible gas.

Atmospheric/Purge Cylinder Gases

As mentioned previously, nitrogen and other atmospheric gases are supplied to semiconductor manufacturers in cylinders as well as in discrete deliveries of bulk liquids. They are classified under the specialty gas designation because they represent cylinder deliveries. Atmospheric/purge gases in cylinders are used for purging certain processing systems and equipment in cases when a semiconductor manufacturer is concerned about possible back-contamination of the house lines.

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In addition, some processes, such as sputtering, require only small amounts of gas and thus single-cylinder usage of argon is more economical. In the case of sputtering, the process is run under vacuum conditions and argon ions are accelerated in an electric field. Through physical bombardment, the argon ions knock molecules off the surface of a solid target. The ejected material from the target is deposited onto the surface of a wafer, in addition to the walls of the sputtering chamber. Typically, a cylinder of argon can last for three months or more in a sputtering system before it requires replacement.

Other Specialty Gases

In this specialty gas category can be found such gases as tungsten hexafluoride and germane. Germane, GeH_4, is used in epitaxial chemical vapor deposition for the manufacturing of LEDs. Germane must be used with great caution as it is a hemolytic gas and thus has the ability to dissolve red blood cells.

Tungsten hexafluoride, WF_6, is used as a source of tungsten for the deposition of tungsten silicide as an alternative interconnect material in VLSI devices. The deposition of refractory metal silicides is an area that is receiving increased attention as semiconductor manufacturers design IC devices with higher packing densities and higher device speeds. The problem is that while scaling improves overall device performance, a reduction in device geometries also results in a corresponding reduction of the thickness of interconnect lines. In addition, the larger die sizes used in VLSI devices typically require longer interconnect lines. This combination of thinner and longer interconnect lines results in an increase in the interconnect resistivity and hence in the RC time delay of the circuit.

Tungsten silicide, as well as other refractory metal silicides based on molybdenum, tantalum, and titanium, have been developed as interconnect materials for VLSI devices because they exhibit considerably reduced resistivities. When these refractory metal silicides are deposited at the gate level on a layer of doped polysilicon, the resulting structure is called a "polycide" shunt. The polycide structure has the advantage of the reduced resistivity of the refractory metal silicide and yet retains the good performance characteristics of polysilicon, such as the stable polysilicon/oxide interface.

The techniques of deposition of refractory metal silicides include sputtering, coevaporation, and chemical vapor deposition. The source materials for molybdenum, titanium, and tungsten are molybdenum hexafluoride, titanium tetrachloride, and tungsten hexafluoride, respectively. These materials are all liquids at 25 °C that have sufficient vapor pressure to allow for source flow to be controlled with a mass flow controller. Tungsten hexafluoride, in particular, is a yellow liquid at room temperature. In its gaseous state, it forms a white mist of hydrogen fluorine gas in moist air. In an inert environment, tungsten hexafluoride is a colorless, odorless gas.

Dataquest believes that tungsten silicide is the most widely used refractory metal silicide in the United States. Genus, a CVD equipment company, was the first to develop a dedicated tungsten silicide reactor for chemical vapor deposition, and the success of the Genus reactor has done much to stimulate interest in tungsten hexafluoride as a source material.

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PRODUCTION AND DISTRIBUTION

Bulk Gas Manufacturing

Nitrogen, Oxygen, and Argon

Nitrogen, oxygen, and argon are obtained directly from the air by a technique of cryogenic air separation and distillation. Essentially, the process entails cooling air close to its liquefaction point and then utilizing the physical difference in volatilities of components of air to distill and separate them. Table 2 contains a list of the fixed components of air by percent composition, as well as the variable components. The fixed components are numbered (in parentheses) in decreasing order of volatility. Those gases in the same volatility range will become impurities of one another. Therefore, helium and neon will sometimes be found in nitrogen, but not in oxygen or argon. Similarly, krypton and xenon will always occur in oxygen, but not in argon or nitrogen. The extent to which any components become impurities in the others is dependent on the separation capacity of the distillation system.

Table 2

Components of the Atmosphere

Gas	Order of Volatility	Symbol	Concentration-Dry Basis Volume %	ppm
Fixed				
Nitrogen	(3)	N_2	78.084	
Oxygen	(5)	O_2	20.9476	
Argon	(4)	Ar	0.934	
Neon	(2)	Ne		18.18
Helium	(1)	He		5.24
Krypton	(6)	Kr		1.14
Xenon	(7)	Xe		0.087
Variable				
Carbon Dioxide		CO_2		300 to 400
Nitrous Oxide		N_2O		0.5
Nitrogen Dioxide		NO_2		0 to 0.02
Water		H_2O	1.25*	
Hydrogen		H_2		0.5 Typ
Carbon Monoxide		CO		1 Typ
Methane		CH_4		2 Typ
Ethane		C_2H_6		0.1 Typ
Other Hydrocarbons		C_xH_y		0.1 Typ

*At 70°F and 50 percent relative humidity

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It is interesting to note that the level of the variable components of the air may differ, depending on the geographical location of a given air separation plant because of the local levels of smog and humidity. Additional purification of the bulk gases is necessary in areas that have substandard air quality.

Once the different components of air have been separated, the cryogenic liquids are transported to a customer's site from the gas company's air separation facility in specially equipped tank trucks. Upon arrival at a semiconductor facility, the liquid is transferred to cryogenic storage tanks located "on the pad," close to the vaporization equipment. The transportation and storage advantages associated with cryogenic liquids are clearly demonstrated by the fact that a single volume of liquid nitrogen upon vaporization translates to an equivalent of approximately 750 volumes of nitrogen gas.

In some cases, when a semiconductor manufacturer has insufficient volume demand or uneven patterns of usage, bulk gases are transported via tube trailers in a gaseous, rather than liquid, state. Other alternative delivery modes for nitrogen include multicustomer nitrogen gas pipeline networks, as well as on-site nitrogen generation facilities at a semiconductor manufacturing location. In most situations, it is not economical to produce any gas other than nitrogen on-site because of insufficient volume demand. The alternative modes of nitrogen delivery are discussed in detail in a later section.

Hydrogen

Hydrogen is obtained in the industrial processes of thermal cracking or steam reforming of hydrocarbons (i.e., natural gas) or in the reduction of water by carbon. Hydrogen, like the bulk gases generated through air separation, is delivered to semiconductor manufacturers as a cryogenic liquid in a tanker truck, or when appropriate, in a gaseous state via tube trailer.

Nitrogen Delivery Systems

There are three different modes of delivering high-purity nitrogen to a semiconductor fabrication facility: an on-site air separation plant, a single-customer or multicustomer pipeline network, and merchant deliveries of liquid nitrogen. For the purpose of this study, only multicustomer pipeline systems are considered under the pipeline category. Single-customer pipelines are considered delivery extensions of dedicated merchant air separation facilities, and thus in some ways are analogous to customer on-site facilities. Each of the three delivery modes has economic and logistical advantages and disadvantages which will be reviewed in the following sections. In particular, such issues as the amount of nitrogen required, the location of the fabrication facility, and the existing infrastructure must be considered in each case.

On-Site Nitrogen Generation Plants

Semiconductor manufacturers consider an on-site nitrogen generation facility when sufficiently large volumes of nitrogen are required for a given fabrication facility. This occurs when a new facility with large nitrogen consumption requirements comes on-line, or when the consumption of nitrogen has grown beyond the point of economic justification for merchant delivery of liquid nitrogen. Because the consumption rate of nitrogen is substantially larger than that of the other bulk gases, often it is the only gas that is economical for a semiconductor manufacturer to produce on-site. There are exceptions to this practice, however. For example, a Texas Instruments

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facility in Texas is supplied via a single-customer pipeline network with high-purity nitrogen, oxygen, argon, and hydrogen generated at a nearby plant operated by Liquid Air.

Typically, the gas company responsible for installation of the plant retains ownership and supervises its operation. There are several reasons why this is the case. First, a semiconductor manufacturer has other more pressing demands for capital expenditure than a nitrogen generation plant. In addition, personnel at a fabrication facility are usually not knowledgeable about gas production or maintenance of such a facility. Finally, if it becomes necessary to expand nitrogen capacity, existing plant equipment will have to be removed and a larger facility installed in its place, because smaller plants cannot be directly upgraded.

The charge to a semiconductor manufacturer for on-site generation of nitrogen usually includes a regular fixed fee that covers the equipment and facility, the cost of maintaining the plant, as well as the gas itself. The customer typically pays the power costs for the generation of nitrogen this can vary considerably, depending on the source of electricity. For example, in the United States, the energy costs in the Pacific Northwest are significantly lower than in other areas of the country because of an abundant source of cheap hydroelectric power. In the Silicon Valley of northern California, however, the cost of power makes the overall cost of a customer on-site generation plant prohibitive when compared with existing pipeline networks and liquid bulk deliveries.

There are several factors that influence the choice for on-site nitrogen generation, but foremost is the wafer production level, and thus nitrogen consumption rate, of a fabrication facility. However, nitrogen consumption in a fab depends on more than just a large level of wafer starts, because a certain amount of nitrogen is always required to maintain the processing equipment and environment even when wafer production levels drop. If production levels at a given facility decrease, the reduction in nitrogen will not drop at a rate proportional to wafer starts because of the amount of gas that is needed to maintain the integrity of the processing environment.

Two issues that can affect a lower break-even point for the conversion to an on-site facility from merchant gas delivery include the location of the fabrication facility and the condition of the existing infrastructure. If a semiconductor fab is located in an area that is quite a distance from a merchant source of liquid nitrogen, the additional costs for transporting bulk liquids may become prohibitive when compared with the alternative of on-site nitrogen generation. In addition, if the existing infrastructure (communications and transportation network) is poor, regular and reliable delivery of bulk liquid nitrogen may not be possible, and again, on-site nitrogen generation may be the only alternative.

Several on-site plants at semiconductor fabrication locations have been identified in countries in the Rest of World (ROW) region these include Israel, Malaysia, and South Korea. In these cases, the infrastructure that would allow for merchant delivery of liquid nitrogen is poor. At the semiconductor facility in Israel, hydrogen and oxygen as well as nitrogen are produced on-site. This is unusual because hydrogen and oxygen are required in much smaller volumes than nitrogen in the semiconductor processing environment. Hydrogen, oxygen, and argon are rarely produced on-site in Europe, Japan, and the United States because the existing infrastructure is sufficient to make bulk delivery economically viable.

One disadvantage to on-site nitrogen production that should be mentioned is that regardless of the amount of nitrogen produced at the facility, the fixed fee payments are unaffected. In an economic downturn, such as the semiconductor industry endured during the years 1985 through 1987, those fees can become an economic liability for facilities that are required to significantly cut back or shut down production lines.

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Dataquest estimates that there are approximately 40 to 50 semiconductor fab locations in the United States that have on-site nitrogen generation facilities. The major gas companies that provide on-site nitrogen generation facilities in the United States include Air Products, Airco, Liquid Air, and the Linde division of Union Carbide.

On-site nitrogen generation facilities are also found at approximately 30 Japanese semiconductor facilities. The companies that supply the on-site nitrogen generation plants in Japan include Daido Sanso, Nippon Sanso, Osaka Sanso, and Teisan.

In the European gas market, several on-site nitrogen generation facilities have been identified in the United Kingdom gas suppliers for these sites include Air Products and BOC (British Oxygen Company). In addition, Dataquest is aware that there are a number of on-site nitrogen generation plants at semiconductor facilities in France and West Germany. Gas suppliers at these facilities include L'Air Liquide and Linde AG.

Pipeline Delivery of Nitrogen

Gaseous nitrogen is supplied to semiconductor facilities via single-customer and multicustomer pipeline networks. For the purpose of this study, only multicustomer pipeline systems are considered under the pipeline designation. Single-customer pipelines are considered delivery extensions of dedicated merchant air separation facilities and thus are analogous to customer on-site facilities.

At this time, there are only three multicustomer pipeline systems (all located in the United States) that supply semiconductor manufacturers with nitrogen. Although single-customer pipelines exist in Europe as well as Japan, there are currently no multicustomer pipeline networks in those regions. In Japan, in particular, it is not uncommon for a semiconductor manufacturer to have nitrogen piped to the facility from a neighboring chemical or steel plant that has excess nitrogen capacity. The nitrogen obtained from such sources must undergo significant purification processes prior to its use in device manufacturing.

The following discussion of multicustomer pipeline networks focuses on the two Air Products pipelines located in the Silicon Valley and Chandler, Arizona, and the Linde pipeline, located in San Jose, California.

The driving force for establishing a multicustomer pipeline system is the strategic location of a network that has the ability to serve an expanding geographical region of semiconductor production activity. Air Products established its first pipeline system in 1971, located in the Silicon Valley. Over the years, the low-carbon steel pipeline has been expanded to a system that is 25 miles long, including a recent 3-mile extension that is made of electropolished stainless steel. The pipeline network supplies high-purity gaseous nitrogen to approximately 32 semiconductor manufacturers in the Silicon Valley, from Mountain View to San Jose, with the recent 3-mile extension into Milpitas. A second Air Products pipeline, also low-carbon steel, was established in Chandler, Arizona, in the late 1970s. It is approximately 25 miles long and serves more than 10 semiconductor manufacturers in the area.

The Linde division of Union Carbide brought a high-purity nitrogen pipeline system on-line in early 1985. It is a two-mile long stainless steel system that serves the International Business Park in San Jose. There are currently several semiconductor manufacturers that are being supplied with nitrogen from the Linde pipeline network. Linde chose a stainless steel pipeline system rather than low carbon steel because of its ability to provide an ultrahigh-purity, low-contaminant environment for gaseous nitrogen delivery.

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Merchant Liquid Nitrogen Delivery

Liquid nitrogen is delivered via tanker trucks to cryogenic holding tanks located on the pad at semiconductor manufacturing facilities. This is the only option available for nitrogen supply when a semiconductor manufacturer is not strategically located to take advantage of a multicustomer pipeline system, or if the account is of insufficient size to warrant on-site nitrogen generation. The overwhelming advantage for shipping discrete amounts of bulk liquid rather than gaseous nitrogen is that a single volume of liquid corresponds to an equivalent of 750 volumes of gas after vaporization. Vaporizers are installed on the pad by the gas supplier for on-site conversion from liquid to gas as needed.

The pricing system for merchant delivery of liquid nitrogen can vary considerably depending on the size of the account and the distance of the fab facility from vendor-owned air-separation plants. The basic cost of bulk liquid nitrogen delivery includes the power costs to liquefy and separate out the nitrogen, transportation costs (based on round-trip mileage) to move a discrete volume of liquid by tanker truck to a fabrication facility, as well as a hook-up charge. In addition, there is typically an escalation clause built into the contracts for liquid nitrogen delivery that increases the price of nitrogen as time goes on. (For example, in the United States, pricing for bulk liquids can in some cases follow the Producer Price Index for Industrial Commodities set by the Bureau of Labor Statistics.) However, as the account grows, appropriate reductions in price are also considered.

The price of liquid nitrogen includes the nitrogen itself, delivery of the bulk liquid, as well as the leasing fee for vaporization equipment and storage tanks. Because of very aggressive pricing practices within the gas industry for semiconductor manufacturer accounts, the pricing distribution for liquid nitrogen will continue to span a wide range of values in the future.

The merchant liquid nitrogen delivery prices can be higher overall than either pipeline delivery or on-site generation, even when power costs are included. One reason is that some of the power cost for air liquefaction and separation can be recovered through heat exchange equipment when the liquid is vaporized to a gas. The gas company is responsible for the operation of customer on-site facilities, as well as their own plants, and thus can pass the savings in power costs directly on to the semiconductor manufacturer through prices for on-site nitrogen and pipeline-delivered nitrogen. However, with liquid nitrogen delivery, the semiconductor manufacturer is paying for a liquid supply of nitrogen, and thus the price up front does not reflect any eventual recovery of power charges that may be generated through vaporization.

Specialty Gas Manufacturing and Distribution

More than 35 specialty gases are used in semiconductor manufacturing. Although the majority of specialty gas companies essentially supply the entire range of gases, it is interesting to note that no one company has complete manufacturing capability. Therefore, in the specialty gas industry, it is necessary that companies sell products among themselves. It is therefore possible for a gas manufactured by one company to be purchased, remixed, filtered, and repackaged by another company, and in some cases exchange hands a second time, before finally being sold to a semiconductor manufacturer. For that reason, a clear and sharp distinction must be made between primary manufacturers and final gas suppliers when evaluating the semiconductor specialty gas market because of possible double- and triple-counting of products through the distribution chain. As mentioned, many of the specialty gases are remixed to provide different dilution mixtures with

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gases such as nitrogen, argon, hydrogen, or helium. This remixing can also be a source of confusion when following the distribution network of gases produced by primary manufacturers to their final semiconductor manufacturing destination.

Figure 1 presents a schematic of different possible distribution networks for specialty gases from a primary manufacturer to a final destination at a semiconductor manufacturing facility. An interesting example of the complexity of the semiconductor specialty gas distribution network is illustrated by Solkatronic Chemicals. Solkatronic Chemicals, through its acquisition of Synthatron in 1987, is a primary manufacturer of arsine in the United States. In addition to its direct sales to semiconductor manufacturers, Solkatronic may supply one or more gas companies in the United States with the dopant gas. Typically, these gas companies would refilter and repackage the material and sell the product directly to a semiconductor manufacturer. However, they may also sell some amount of the gas to yet another gas company, possibly to a joint venture partner, or to their overseas gas operations. In addition to its activities in the United States, Solkatronic Chemicals supplies dopant gases directly to foreign gas companies, which in turn supply their domestic semiconductor manufacturing customers. In Japan, the nature of the distribution network for specialty gases is more complex than in Europe or the United States. The distribution chain from primary manufacturer to the end user—the semiconductor manufacturer—can involve as many as five or more different transactions for the same molecules of gas.

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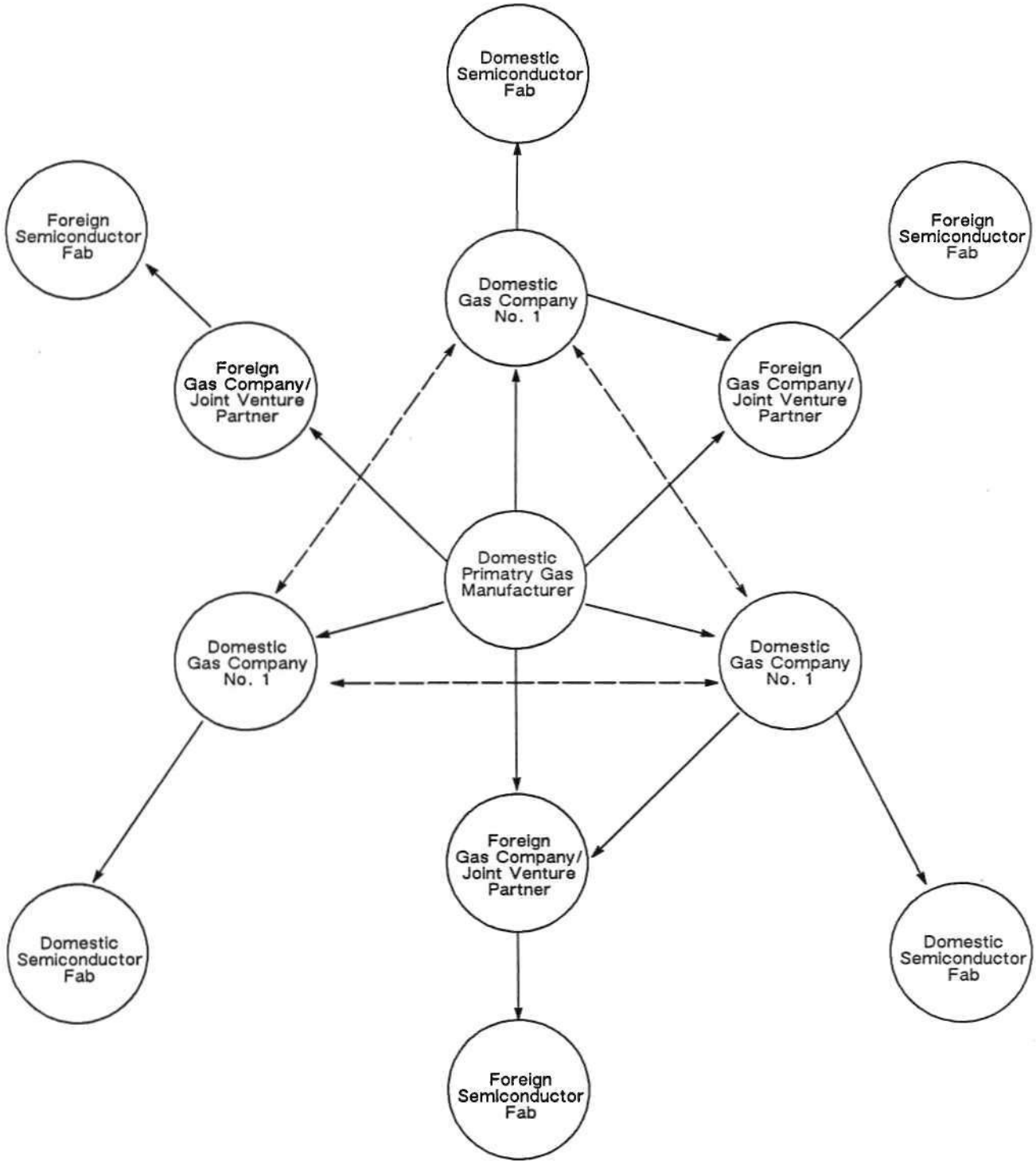
Figure 1

Possible Distribution Networks for Specialty Gases from Point of Manufacturing to Point of Use



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APPENDIX - UNIT CONVERSION FACTORS—TEMPERATURE, VOLUME, AND WEIGHT

Gas, by its very nature, is available in a variety of different volumes and quantities depending on the temperature and pressure of the system. The associated nomenclature used to describe a given amount of gas is likewise as varied. The following section presents a summary of the different units of temperature, pressure, volume, and weight that are commonly used in the gas industry, as well as a set of conversion factors between the different units.

Any amount or quantity of gas has a temperature and pressure dependence that in its simplest form is governed by the Ideal Gas Law, PV=nRT. This law states that the pressure of any gas, P (measured in atmospheres), multiplied by its volume, V (liters), is equal to the product of the number of moles of the gas, n, the temperature of the system, T (in kelvins), and the universal gas constant, R. One convenient way to remember the appropriate factors is that one mole of gas at one atmosphere pressure at 0°C (273 K) will occupy 22.4 liters.

STP is the designation that is used to indicate standard temperature and pressure by definition, one atmosphere, 0°C (273 K). The more common specification is that of NTP, which stands for normal temperature and pressure, and corresponds to one atmosphere, 70°F. One atmosphere of pressure can also be defined in units of pounds per square inch; specifically, one atmosphere of pressure is equal to 14.7 psi. An alternative designation is gauge pressure, or psig (pounds per square inch gauge), which does not include ambient pressure conditions. Finally, psia (pounds per square inch absolute) is the sum of gauge pressure as well as the atmospheric pressure, typically 14.7 psi.

Common units for volume include liters, cubic feet (cf), and cubic meters (cm, not to be confused with centimeters). In some cases, cubic feet will be specifically identified as standard cubic feet (scf), which defines the temperature and pressure values at NTP. However, while "scf" may not be directly stated, generally it is assumed that NTP conditions hold unless otherwise specified. Large quantities of gas are usually described in units of hundred cubic feet (hcf), billion cubic feet (Bcf), or hundred cubic meters (hcm); this last designation is pronounced "hook-ems."

The units of kilograms, pounds, and tons are also used to designate a given quantity of gas under normal temperature and pressure. The definition of a ton, and thus the conversion factor from tons to pounds, takes on a different value in the United States compared with Europe and Japan. In the United States, one ton is equal to 2,000 pounds. In Europe and Japan, the designation of metric tons is assumed, in which case one metric ton is equal to 2,204 pounds (1,000 kg). Table 3 contains a summary of temperature, volume, and weight conversion factors.

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Table 3

Unit Conversion Factors—Temperature, Volume, and Weight

Temperature
- Fahrenheit (°F) = 1.8 * °C + 32
- Celsius (°C) = (5/9) * (°F-32)
- Kelvin (K) = °C + 273

Volume
- 1 liter = 1,000 cubic centimeters
- 1 cubic foot = 28.32 liters
- 1 cubic meter = 35.31 cubic feet = 1,000 liters
- 1 hcm = 100 cubic meters = 3,531 cubic feet
- 100 Bcf = 28.32 million hcm (million hundred cubic meters)

Weight
- 1 kg = 2.204 pounds
- 1 ton = 1,000 pounds
- 1 metric ton = 1,000 kg = 2,204 pounds

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Semiconductor Gas Companies

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Semiconductor Gas Companies

INTRODUCTION

In the semiconductor industry, process gases represent one category of consumable materials that are used throughout the fabrication of semiconductor devices—from the growing of single silicon crystals through the many steps of wafer fabrication to the final stages of assembly and packaging. Gases used in the semiconductor industry are divided into two general categories: bulk gases and specialty gases. This service section presents a discussion of the major suppliers of bulk and specialty gases. Please refer to the "Semiconductor Gases—Products and Applications" section located behind the Semiconductor Materials tab in this binder for information on products, applications, manufacturing, and distribution networks for semiconductor gases.

DEFINITIONS

An important part of any analysis of the semiconductor gas industry is a clear understanding of the definitions that are used to describe product categories and the customer base.

Gas Categories

As mentioned previously, semiconductor gases generally are divided into two categories—bulk and specialty. The bulk semiconductor gases are nitrogen, oxygen, hydrogen, and argon. The designation "bulk" typically refers to a discrete delivery of a large volume of gas by truck transport. These gases typically are delivered as cryogenic liquids because of the efficiency of transportation and storage prior to the vaporization stage at the semiconductor manufacturer's facility. Nitrogen gas provided through direct pipeline delivery, as well as customer on-site nitrogen generation plants, is also considered as part of the bulk gas category, although the supply of nitrogen, in this sense, cannot be classified as discrete.

A large number of gases (more than 35) are classified as semiconductor specialty gases. For this reason, a further segmentation of this category is necessary and is based on the chemical reactivity and functionality of the various specialty gases. Dataquest segments the specialty gas market into six categories: silicon-precursor gases, dopants, etchant gases, reactant gases, atmospheric/purge cylinder gases, and others. Specialty gases are used in comparatively smaller volumes than the bulk gases and thus are delivered in high-pressure cylinders.

Semiconductor Industry Customer Base

For most gas companies, the semiconductor industry represents part of a loosely defined category of "electronics" customers. Because the designation of electronics is ambiguous, Dataquest defines the customer base for semiconductor bulk and specialty gases to include the following:

- Semiconductor manufacturers (both merchant and captive)
- Research cooperatives, government labs, and university semiconductor programs
- Polysilicon, silicon, and gallium arsenide (GaAs) operations

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Dataquest's market estimates reflect direct sales of bulk and specialty gases to this customer community by merchant gas companies. Sales of gases between gas companies are excluded because of the problems that arise from the double- and possibly triple-counting of gas molecules along the distribution chain. In addition, revenue from gas-handling equipment sales and from those gases sold to semiconductor equipment companies is excluded. Gases that are used in nonsemiconductor industry segments such as fiber optics, solar applications, or the printed circuit board industry also are not included in our analysis.

SUPPLIERS VERSUS PRIMARY MANUFACTURERS

In the specialty gas market, an important distinction is made between suppliers and primary manufacturers. A primary manufacturer is defined as a company with basic production capability for a specific material. A representative example is Du Pont, which is a primary manufacturer of Freon gases. Suppliers are companies that are involved in remarketing a material to other suppliers or to the end user. Typically, a supplier will purchase material in bulk from a primary manufacturer and repackage it for the semiconductor market.

No single industrial gas company is a primary manufacturer of the entire spectrum of electronic gases. Because of the range of gases and the small volumes used in the industry, it is not economical for each company to have its own production capability. However, several of the major companies are primary manufacturers of a family of gases such as Union Carbide's silicon precursors. Primary companies often have agreements to supply other industrial gas companies with the products in which they are primary.

SEMICONDUCTOR GAS COMPANIES

Five companies and their associated operations (see Table 1) dominate the world's semiconductor gas industry. These major semiconductor gas suppliers have a good-to-strong presence in the four major semiconductor production regions of the world: Japan, the United States, Europe, and the Pacific Rim. This presence is achieved through overseas operations, equity investment positions in foreign gas companies, or technical and marketing agreements.

For the major gas suppliers, the semiconductor gas market represents only a small portion of a company's total gas business activities. Some of the nonsemiconductor gas applications that represent far larger market opportunities include nitrogen for frozen food processing, oxygen for steel processing, and hydrogen for fuel cells in the rocket and aerospace industries. However, the semiconductor industry represents probably the most rigorous demands on gas suppliers with regard to providing high-purity materials and delivery systems. Therefore, success in the semiconductor gas industry promotes a gas supplier's presence at the cutting edge of gas technology.

The semiconductor bulk gas industry is characterized by long-term contracts between vendor and customer because of the support equipment required at the customer's site for the on-site storage of bulk gases. Typically, one bulk gas supplier supports each fab facility, and that company often will receive the initial gas contract before construction even begins on a new fab. In contrast, the specialty gas industry is characterized by spot purchases. Consequently, multiple specialty gas vendors per fab is the norm rather than the exception.

Specialty gas suppliers are unique when compared with other electronic materials suppliers that sell products to the semiconductor industry. What makes this market different is that no single specialty gas company has primary manufacturing capability for all of the specialty gases that it

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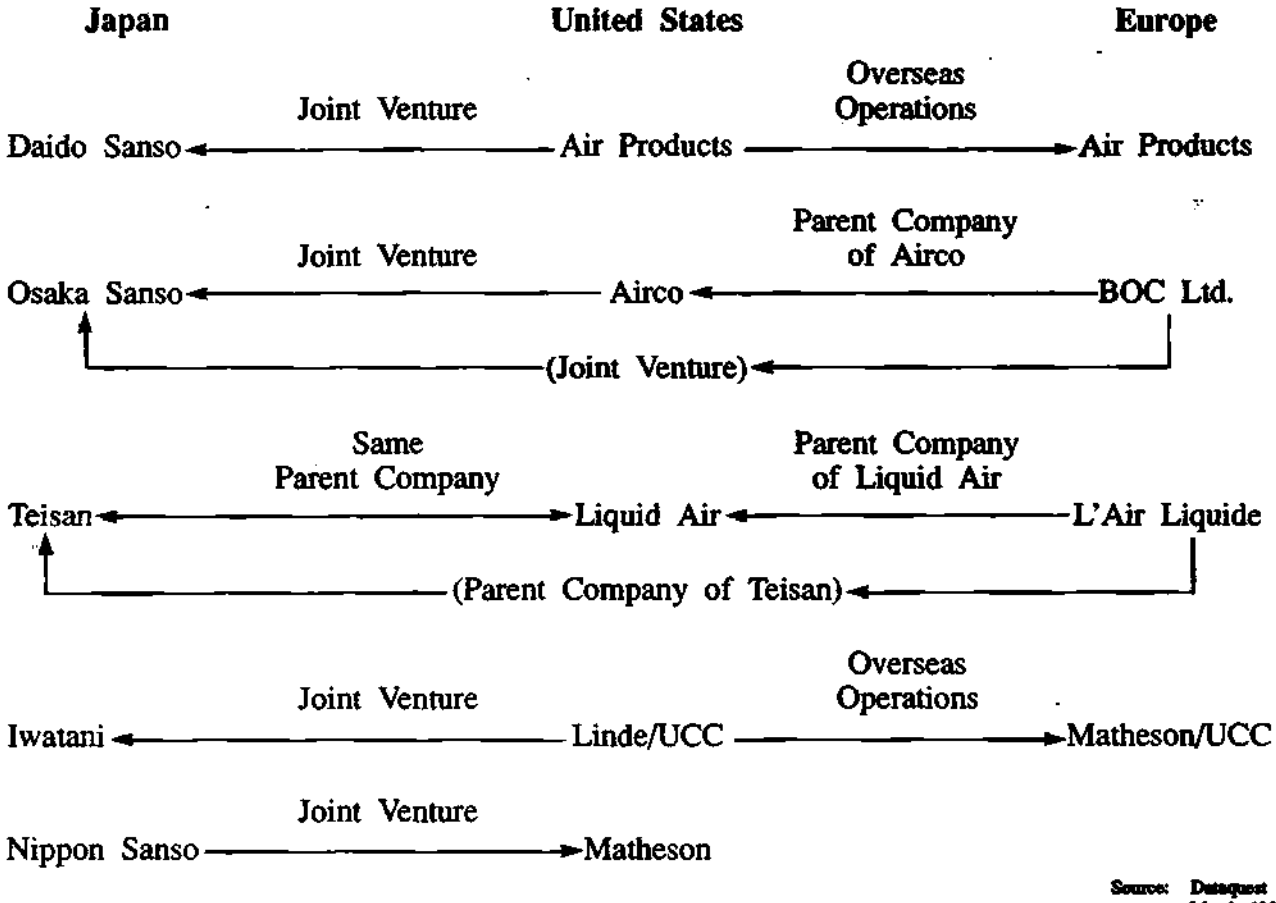
Table 1

Gas Company Interrelationships



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provides to the industry. Thus, a specialty gas company typically must buy some of its products from a primary manufacturer that, in some cases, may be a competitor.

Because these companies are the major suppliers of bulk and specialty gases to the worldwide semiconductor industry, a more detailed discussion of each company's activities is presented in the following subsections.

COMPANIES

Air Products

Air Products is a major supplier of industrial gases to the world semiconductor industry. The company's worldwide headquarters are located in Allentown, Pennsylvania; its European headquarters are located in Walton on Thames, Surrey, England. The company's primary markets are the United States and Europe. Its participation in the Pacific Rim industrial gas market has been through joint ventures with local companies.

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Air Products is especially strong in the U.S. and U.K. atmospheric bulk markets. An important aspect of this strength is the company's two multicustomer high-purity nitrogen pipelines in the United States. In addition, the company has implemented a program to provide very high purity liquid product to the North American and European markets. Air Products also is well positioned in the liquid hydrogen market. It has several liquid hydrogen plants in the United States and one plant in continental Europe.

Air Products is a prominent supplier of specialty gases. The company has a well-developed distribution network. The foundation of the network is the regional production facility, where specialty gases are transfilled and stocked. Service and technical support are provided from these facilities. Another notable strength of the company is its primary manufacturing capability of fluorinated products including CF_4, SF_6, NF_3, and WF_6. The company operates one of the largest direct fluorination plants in the world.

Ever since the semiconductor industry's inception, Air Products has aggressively targeted the industry's bulk gas requirements. As a result, the company has a very strong market share of bulk gas products in the United States. Moreover, the company continues to develop innovative marketing strategies, most recently with the introduction of the point-of-use agreement. This arrangement calls for Air Products to take over responsibility for the safety, analysis, piping and monitoring systems, and ultimately the supply of all gas products to the point of use. In the first agreement of this sort, Air Products and Motorola entered into a 10-year contract that covers every aspect of the supply and use of industrial and specialty gases at Motorola's semiconductor facility in Mesa, Arizona.

In the Far East, Air Products has expanded through a series of joint ventures. In Japan, the company has an equity position in a medium-size gas supplier, Daido Sanso. In Korea, Air Products serves the semiconductor industry through its joint venture with Korea Industrial Gases; in Taiwan, it has allied itself with San Fu Chemical; in Hong Kong and China, with Chun Wang Industrial Gases; in Thailand, with Bangkok Industrial Gases; and in Malaysia, with Super Oxygen.

In addition, Air Products has diversified beyond the traditional industrial gas business. In 1984, it purchased a silicon wafer reclaim business. In 1986, the company purchased J.C. Schumacher, a San Diego-based manufacturer of liquid organic source silicon and dopant materials. It has also taken a 30 percent interest in Epichem, a British manufacturer of organometallic precursors. Air Products has since transferred this technology to the United States and is manufacturing organometallic precursors in Hometown, Pennsylvania.

BOC Ltd.

BOC is a major supplier of industrial gases to the world semiconductor industry. The company's worldwide headquarters are located in Windlesham, Surrey, England. The company participates in the U.S. market through a wholly owned subsidiary, Airco, which is headquartered in Murray Hill, New Jersey. Its participation in the Pacific Rim industrial gas market has been through joint ventures with local companies in Korea, Taiwan, Singapore, and Malaysia.

BOC's bulk gas presence is strong in the U.S. and U.K. markets. The company has a very strong distribution network in both regions. In addition to the standard products, the company markets a high-purity line of bulk gas products. BOC also has actively participated in and marketed the ultraclean technology approach to industrial gas handling that was pioneered by

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Professor Tadahiro Ohmi at Tohoku University.

Within its specialty gas business, BOC has placed particular emphasis on its semiconductor gases. It has a very strong distributor network and regional transfill facilities through which it markets a broad line of semiconductor gases. Furthermore, the company has made significant capital expenditure in semiconductor specialty gas facilities located in North Carolina and West Germany. In Europe, BOC recently brought on-line a new facility for purifying hydrogen chloride.

Airco, the U.S. subsidiary of BOC, has led BOC Ltd. in executing a strategy that places strong emphasis on the development and production of electronic specialty gases. In the fourth quarter of 1987, Airco acquired the Materials Science Division of Genus, which produces high-purity tungsten hexafluoride used in LPCVD processing. In 1989, the company completed the construction of a specialty gas facility in Research Triangle Park, North Carolina. This complex is dedicated to the research, development, and production of high-purity specialty gases for the semiconductor industry.

The BOC Group owns 50 percent of Osaka Sanso, BOC's venture partner in Japan. Osaka Sanso is a medium-size supplier of bulk gases and a small supplier of specialty gases to the Japanese semiconductor industry. However, this association has provided BOC access to the technical developments in the Japanese market, as is made evident by BOC's close relationship with Tohoku University.

BOC also has aggressively expanded its operations in the Far East. In 1988, BOC concluded a joint venture with Wusong Chemical Works, an industrial gases manufacturer located in Shanghai, China. The new company is called Shanghai BOC. BOC's contribution to the venture includes the construction of a 110 ton-per-day liquefier that produces high-purity nitrogen and oxygen and an entire specialty gases plant.

BOC also supplies semiconductor manufacturers in Pacific Rim countries through a group of joint ventures and subsidiaries. Hong Kong Oxygen is a joint venture between BOC and L'Air Liquide in Hong Kong. KBOC is a joint venture in South Korea; Lienhwa is a joint venture in Taiwan; Malayan Oxygen is a subsidiary in Malaysia; and Thai Industrial Gases is a subsidiary in Thailand.

L'Air Liquide

L'Air Liquide is a major supplier of industrial gases to the European semiconductor industry and to other regional markets through its subsidiaries. The company's worldwide headquarters are located in Paris, France. Liquid Air, 94 percent owned by L'Air Liquide of France, is the North American affiliate and is headquartered in Walnut Creek, California; Teisan is a wholly owned subsidiary of L'Air Liquide in Japan (L'Air Liquide expanded into Japan in 1911). Alphagaz is the specialty gas division of L'Air Liquide and Liquid Air Corporation.

L'Air Liquide is a major supplier of bulk gases to the continental European and Japanese semiconductor industries through its subsidiary, Teisan. Teisan also is a primary supplier of liquid hydrogen. In continental Europe, L'Air Liquide has a strong position in liquid hydrogen with the completion of a 10-tons-per-day plant in France. In the United States, the company is building its presence in the semiconductor bulk gas market.

L'Air Liquide's specialty gas business mirrors its bulk gas business in terms of regional strengths. The Alphagaz division has a large market share in continental Europe and is building its

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business in the North American market. In Japan, Teisan is a prominent supplier of specialty gases to the semiconductor industry. It has aggressively pursued the monosilane market and is one of the few primary manufacturers of arsine.

In Europe, L'Air Liquide has established a primary source of arsine through a joint agreement between L'Air Liquide and Les Mines de Salsignes, a mining company located in Salsignes in southern France. In the joint agreement, L'Air Liquide provides process technology for high-purity arsine manufacturing, while Les Mines has built and is responsible for running the plant. The facility came on-line in the summer of 1987. L'Air Liquide has an exclusive marketing agreement with Les Mines for the arsine gas.

In 1988, Comurhex Inc., a subsidiary of Pechiney Group company, and L'Air Liquide signed an agreement for the joint development, production, and marketing of fluorine gases. As a result, Comurhex produces tungsten hexafluoride at its Pierrelatte plant in southern France, and L'Air Liquide markets the product worldwide through its Alphagaz division.

Denki Kagaku Kogyo (Denka), L'Air Liquide, and Teisan have jointly established a $10 million silane plant in Omi, Niigata prefecture. The company is named Denal Silane Co., Ltd. The facility, completed in January 1989, has the capacity to produce several hundred tons per year of silane. Denka owns 51 percent of the joint venture and is in charge of production. L'Air Liquide and Teisan together own 49 percent of the joint venture and are responsible for product sales, Teisan in Japan and L'Air Liquide outside of Japan.

L'Air Liquide also supplies semiconductor manufacturers in Pacific Rim countries. Hong Kong Oxygen is a joint venture between BOC and L'Air Liquide. L'Air Liquide also has a joint venture in South Korea called Daesung Sanso and a joint venture in Taiwan called Liquid Air Far East.

Nippon Sanso

Nippon Sanso is the largest supplier of bulk and specialty gases in Japan and a major supplier in the Pacific Rim countries. The company is a primary manufacturer of specialty gases, including phosphine and diborane. The company also is the largest supplier of MOCVD equipment in Japan.

The U.S. operations of Matheson were acquired in 1983 as a joint venture between Nippon Sanso of Japan and Amerigas of the United States. Matheson's European operations were acquired at the same time by Union Carbide Corporation. In 1989, Nippon Sanso acquired the 50 percent of Matheson's U.S. operations that was owned by Amerigas. Matheson supplies specialty gases to semiconductor manufacturers in the United States and Rest of World (ROW).

Nippon Sanso has a strong distribution network for both bulk and specialty products in the Japanese market. Matheson's U.S. operations provide primary manufacturing capability for many semiconductor gases, including phosphine and diborane.

In 1988, Nippon Sanso announced that the company is investing $4 million in Industrial Oxygen Inc., Malaysia's second largest gas producer. Nippon Sanso will take the leading role in management, provide technology, and invest in future production facilities. That same year, Nippon Sanso and Linde AG of Wiesbaden, West Germany, agreed to a joint technology exchange that involved the exchange of engineers and technology to improve the production, analysis, and safe handling of silane, arsine, and phosphine gases.

In 1990, Nippon Sanso purchased Semi-gas Systems of San Jose, California. Semi-gas manufactures high-purity gas distribution and control systems. The acquisition fits Nippon Sanso's strategy of being a major supplier of specialty gases and equipment to semiconductor manufacturers and complements its earlier purchase of Matheson Gases' U.S. operations.

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Union Carbide

Union Carbide's Linde division is a major supplier of bulk and specialty gases to the world semiconductor industry. The worldwide corporate headquarters for the company are located in Danbury, Connecticut.

The company's major strengths are in primary manufacturing capability for bulk industrial gases, silicon precursor gases (i.e., silane), and dopant gases (i.e., arsine and phosphine). On a regional basis, Linde's strengths are in the European and U.S. markets. The company has participated in the Far East market by pursuing joint ventures in Japan and South Korea.

Linde has an extensive history in silicon chemistry. The company's Sistersville, West Virginia, plant has been manufacturing chlorosilanes since the late 1950s. In addition, the company completed a full-scale merchant silane plant in Moses Lake, Washington, in 1984. This plant produces high-purity silane, most of which is used as feedstock for the 2,400-metric-tons-per-year polysilicon plant.

Linde acquired Phoenix Research of Costa Mesa, California, a primary manufacturer of dopants, in 1984. This acquisition made Union Carbide one of four companies in the world with primary manufacturing capability for arsine. Production was moved to a new semiconductor facility in Kingman, Arizona, early in 1990. This facility also provides filling and mixing capability for other semiconductor gases.

Linde has continued to make capital investments in the bulk gases portion of its business. In 1985, the company completed a high-purity pipeline to deliver gaseous nitrogen to semiconductor customers in the "Silicon Valley" area south of San Francisco, California. Linde also supplies gases and manages the gas equipment at Sematech.

In Europe, the company's specialty gas operations are headquartered in Paris; the bulk gas operations are headquartered in Geneva. Union Carbide acquired the European operations of Matheson Specialty Gases in 1985. That same year, the company signed a joint venture with Enichem of Italy to market, distribute, and produce industrial and specialty gases in Italy.

In Japan, Union Carbide established a joint venture with Iwatani Industrial Gases to produce helium, hydrogen, argon, nitrogen, and specialty gases for the Japanese markets. Union Carbide currently has a 5 percent stake with option to buy up to 20 percent. The agreement involves an exchange of technology and personnel between Iwatani and Linde.

In South Korea, Union Carbide further extended its participation in the growing Far East market through a new venture called Union Gas Company. The company operates several plants and specialty gas facilities.

OTHER COMPANY ACTIVITIES

Table 2 identifies a wide range of companies actively involved in the primary manufacture or supply of bulk and specialty gases to the worldwide semiconductor industry.

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Table 2

Primary Manufacturers and Suppliers of Semiconductor Gases

Region	Company Activities
United States	
Airco (BOC)	Major supplier of bulk and specialty gases to the U.S. semiconductor industry; wholly owned subsidiary of BOC Ltd. of the United Kingdom. In the fourth quarter of 1987, Airco acquired the Materials Science Division of Genus, which produces high-purity tungsten hexafluoride used in LPCVD processing (see BOC profile).
Air Products	A leading worldwide manufacturer of bulk and specialty gases for semiconductor applications. The world headquarters are located in Allentown, Pennsylvania (see profile).
Alphagaz	Specialty gas division of L'Air Liquide and Liquid Air. Please refer to the L'Air Liquide profile in this section for more details on Alphagaz activities.
American Cyanamid	Primary manufacturer of semiconductor-grade phosphine; no direct sales to semiconductor manufacturers. In mid-1988, the company announced the availability of production volumes of tertiarybutylarsine (TBA), a liquid replacement for arsine gas and tertiarybutylphosphine, a liquid replacement for phosphine. The company also supplies trimethylgallium (TMG) and trimethylaluminum (TMA) for MOCVD processes. These semiconductor materials are produced at the company's Welland plant in Niagara Falls, Ontario.
Amerigas	A primary manufacturer of bulk gas with a regional emphasis in the southern and western United States, Amerigas acquired a 50 percent position in Matheson's U.S. operations in 1983 through a joint venture with Nippon Sanso of Japan. In 1989, Amerigas sold its investment in Matheson to Nippon Sanso, giving Nippon Sanso 100 percent control of Matheson's U.S. operations.
Bandgap Technology	A subsidiary of AMAX and a primary manufacturer of organometallic precursors and high-purity tungsten hexafluoride, Bandgap also has III-V epitaxial growth capability. It markets its products directly to the semiconductor industry. Its facilities are located in Broomfield, Colorado.
Callery Chemical	Callery Chemical is a primary manufacturer of diborane gas and has no direct sales to semiconductor manufacturers.

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Table 2 (Continued)

Primary Manufacturers and Suppliers of Semiconductor Gases

Region	Company Activities
United States (Continued)	
Du Pont	A primary manufacturer of carbon tetrafluoride and other fluorocarbon gases; no direct sales to semiconductor manufacturers. In the second quarter of 1988, Du Pont announced its intention to phase out production of its fully halogenated chlorofluorocarbon gases; these materials have been linked to depletion of the earth's ozone layer. The decision would affect five gases commonly used in plasma etch processing: $CFCl_3$, CF_2Cl_2, CF_3Cl, C_2F_5Cl and CF_3Br. The most widely used etch gases—CF_4, CHF_3, and C_2F_6—are not affected by this decision. In September 1988, Du Pont announced an agreement with Lam Research, a major supplier of plasma etch equipment, to exchange process technology on etchant gases.
Kerr-McGee	Kerr-McGee is a primary manufacturer of boron trichloride and has no direct sales to semiconductor manufacturers.
Liquid Air	Major supplier of bulk gases to the U.S. semiconductor industry; currently building specialty gases business. Liquid Air is 94 percent owned by L'Air Liquide of France. (Please refer to the L'Air Liquide profile in this section for more details on Liquid Air's activities.)
Liquid Carbonic	Small supplier of specialty gases to the U.S. semiconductor industry. Company headquarters are in Chicago, Illinois.
Matheson	Supplier of specialty gases to semiconductor manufacturers in the United States and ROW. U.S. operations of Matheson acquired in 1983 as a joint venture between Nippon Sanso of Japan and Amerigas of the United States; Nippon Sanso acquired the remaining portion of the joint venture in 1989. The European operations were acquired by Union Carbide in 1983. Please refer to the Nippon Sanso profile in this section for more information.
MG Industries/Scientific Gases	Small supplier of gases to the U.S. semiconductor industry. MG Industries is a U.S. subsidiary of Messer Griesheim of West Germany (part of the Hoechst AG corporation).

(Continued)

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Table 2 (Continued)

Primary Manufacturers and Suppliers of Semiconductor Gases

Region	Company Activities
Japan (Continued)	
Scott Specialty Gases	A supplier of specialty gases to the U.S. semiconductor industry. The company is not a primary manufacturer of specialty gas, but it has entered the market by investing in cylinder transfill facilities and a strong distribution network. Scott acquired Scientific Gas Products in 1987.
Solkatronic Chemicals	Solkatronic acquired Synthatron, a small U.S. primary manufacturer of specialty gases in 1987. Solkatronic is one of four manufacturers in the world with primary arsine manufacturing capability and is also primary in phosphine, silicon precursor gases, chlorine, and hydrogen selenide. The company does not supply gases directly to semiconductor manufacturers but rather sells its products to other gas companies. Solkatronic Chemicals is owned by Kali-Chemie AG of West Germany.
Union Carbide	Linde division of Union Carbide is a major supplier of bulk and specialty gases to the world semiconductor industry (see profile).
Voltaix	Voltaix is a small start-up company in North Branch, New Jersey, and primary manufacturer of digermane, diborane, trimethylboron, and germane. It also supplies custom fills of silane, disilane, boron trifluoride, and boron trichloride. Its strategy is to provide custom fills and packaging for semiconductor manufacturers.
Japan	
Asahi Glass	Asahi Glass is a member of the Mitsubishi group and Japan's largest comprehensive glass manufacturer; it has a very strong fluorine and fluorinated chemical production capability, and it is a primary manufacturer of tungsten hexafluoride, carbon tetrafluoride, and other fluorocarbon gases. Electronic materials make up only 3 percent of the company's total sales.

(Continued)

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Table 2 (Continued)

Primary Manufacturers and Suppliers of Semiconductor Gases

Region	Company Activities
Japan (Continued)	
Central Glass	The third-largest sheet glass manufacturer in Japan; chemicals constitute approximately 25 percent of its overall sales. The company places emphasis on fluorinated electronic materials and is a primary manufacturer of tungsten hexafluoride and nitrogen trifluoride.
Daido Sanso	Major Japanese producer and supplier of bulk gases to the semiconductor industry. The company is a distributor but not a primary producer of a wide range of specialty gases. Air Products of the United States has an estimated 15 percent equity position in Daido Sanso. In addition to semiconductor gases, Daido Sanso also manufactures a VCE/CBE system for epitaxial processing. (Please refer to the Air Products profile in this section for more details on Daido Sanso's activities.)
Daikin Industries	Major manufacturer of air conditioners and primary manufacturer of carbon tetrafluoride. The company has diversified into fluorine chemicals, pioneering fluorine and fluorinated products for the semiconductor industry. Chemical products account for about 16 percent of sales. In addition to semiconductor gases, Daikin manufactures fluorine-based photoresist for maskmaking and X-ray lithography applications.
Denal Silane	Founded in 1988 as a joint venture between L'Air Liquide, Teisan, and Denki Kagaku Kogyo, a large industrial chemical company. The partners have built a large silane plant in Omi, Japan, with an estimated capacity of 100 tons per year. The production will provide a source of monosilane for the venture partners' merchant and captive requirements.
Iwatani	Trading company that specializes in industrial gases; noted for powerful end-user sales network. In 1985, Iwatani formed a joint venture with Union Carbide to produce and/or market helium, hydrogen, argon, nitrogen, and electronic specialty gases. Union Carbide has a 5 percent stake in Iwatani now with an option to buy up to 20 percent. It is not a significant primary producer of any semiconductor products except hydrogen; however, the company's extensive distribution network makes it an important vendor in the semiconductor market.

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Table 2 (Continued)

Primary Manufacturers and Suppliers of Semiconductor Gases

Region	Company Activities
Japan (Continued)	
Kanto Denka	Kanto Denka is a medium-size chemical manufacturer that places emphasis on fluorine-based chemicals in its R&D expenditure. It's a primary manufacturer of tungsten hexafluoride, fluorocarbon gases, nitrogen trifluoride, and sulphur hexafluoride.
Komatsu Electronic Metals	Primary manufacturer of silane; estimated capacity is 300 tons per year. Much of the silane production is used in captive operations. The company supplies monosilane to the semiconductor industry through the resale of product to Nihon Sanso and Tomoe Shokai.
Osaka Sanso	Fourth largest manufacturer of bulk gases in Japan. BOC of the United Kingdom entered into a joint venture with company in 1982; BOC has an estimated 50 percent stake. Osaka Sanso is an important supplier of bulk gases to the semiconductor industry. Primarily a reseller of specialty gases, the company has a strong distribution network and markets directly to semiconductor end users.
Mitsui Toatsu	A large diversified chemical manufacturer that belongs to the Mitsui group and is the third largest chemical manufacturer in Japan. Its Electronic Materials group is a primary supplier of a range of silicon-based chemicals (mono, disilane, SiF^4, and others). In addition, the company manufactures NF^3, HCl, NH^3, Cl^2 and other semiconductor grade gases. In the domestic Japanese market, Mitsui Toatsu uses distributors and brokers to sell to semiconductor manufacturers.
Nippon Sanso	A leading worldwide manufacturer of bulk and specialty gases for semiconductor applications. The world headquarters are located in Tokyo (see profile).
Seitetsu Kagaku	Chemical manufacturer affiliated with Sumitomo Chemicals; primary manufacturer of nitrous oxide, silicone tetrachloride, and ammonia. Changed company name to Sumitomo Seika Chemicals in October 1989 to clarify affiliation and improve operations. Specialty gases make up 21 percent of corporate revenue.

(Continued)

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Table 2 (Continued)

Primary Manufacturers and Suppliers of Semiconductor Gases

Region	Company Activities
Japan (Continued)	
Shin-Etsu Chemical	Primary manufacturer of dichlorosilane and disilane; no direct sales to semiconductor manufacturers. Shin-Etsu Chemical is the parent corporation of Shin-Etsu Handotai, the world's largest merchant silicon supplier. Electronic materials make up 35 percent of total sales.
Showa Denko	Belongs to the the Fuyo group. Company is the fourth largest integrated chemical manufacturer. Primary manufacturer of N_2O, Cl_2, NF_3, HCl, BCl_3, CF_4, and NH_3. The company expanded its direct sales force through the acquisition of its distributor in 1986.
Taiyo Sanso	Major industrial bulk gas producer: oxygen, nitrogen, and argon. Company completed a diborane plant in 1987 at its Atsugi facility with a capacity of 100kg per year. Strong distribution network for bulk and specialty gases. Enjoys high market share in gas purification systems for semiconductor facilities. Signed marketing agreement with Union Carbide for the development of the North American purifier market.
Teisan	Leading producer of industrial gases such as oxygen, nitrogen, and argon; member of the L'Air Liquide group (see profile); active in exchange of technology with French parent company, but operates independently; strong in equipment, including air separators and cryogenic equipment. Teisan is developing specialty gases for the semiconductor industry and is a primary supplier of SiH^4 through participation in Denal Silane joint venture. It has a strong distribution network for bulk and specialty gases.
Toagosei Chemical Industry	Medium-size chemical company in the Mitsui group. It focuses on the specialty chemicals market, including high-purity chemicals for the semiconductor industry and high-purity gases and is strong in chlorine-based products.
Toyo Sanso	Medium-size manufacturer of bulk industrial gases such as oxygen, nitrogen, and argon. This Mitsubishi group member has only a small participation in specialty gases and resells high-purity oxygen and silane.

(Continued)

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Table 2 (Continued)

Primary Manufacturers and Suppliers of Semiconductor Gases

Region	Company Activities
Japan (Continued)	
Ube Industries	Primary manufacturer of high-purity boron trichloride and large diversified chemical supplier. The company does not market directly to end users.
Europe	
AGA	AGA is a large industrial company headquartered in Sweden; approximately 50 percent of its revenue is generated from its industrial gas operations. Until recently, AGA's main focus in the semiconductor industry was bulk gas products in continental Europe. In 1987, AGA initiated a program of cooperation with Nippon Sanso, a Japanese gas company. Consequently, AGA is developing its high-purity bulk and specialty gas businesses with particular emphasis on semiconductor applications.
BOC Ltd.	A leading worldwide manufacturer of bulk and specialty gases for semiconductor applications. Airco is BOC's wholly owned U.S. subsidiary (see profile).
Comurhex	Comurhex, a company of the Paris-based Pechiney Group, is a primary manufacturer of tungsten hexafluoride at its Pierrelatte plant in southern France. The company has an agreement with L'Air Liquide (see profile) to market the product through L'Air Liquide's Alphagaz Division.
Epichem	Epichem is a small company based in the United Kingdom that produces high-purity organometallic compounds. Air Products has an equity stake in the company, has licensed the technology, and is producing material in the United States.
Kali-Chemie	Kali-Chemie is a West Germany-based company that supplies high-purity gases, gas mixtures, and chemicals to the semiconductor industry through a group of affiliates. These affiliates include Intermar in the Netherlands, Solkatronic Chemicals in the United States, and Soltronic in West Germany.
L'Air Liquide	A leading worldwide manufacturer of bulk and specialty gases for semiconductor applications. World headquarters are located in Paris, France (see profile).

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Table 2 (Continued)

Primary Manufacturers and Suppliers of Semiconductor Gases

Region	Company Activities
Europe (Continued)	
Linde AG	Linde AG is primarily a supplier of bulk gases; the company is headquartered in West Germany and should not be confused with the Linde Division of Union Carbide. In addition to bulk gases, Linde AG also manufactures purification equipment for bulk gases and currently is working with Nippon Sanso on the transfer of specialty gas technology. Its primary semiconductor activity is in Western Europe.
Messer Griesheim	Messer Griesheim is primarily a manufacturer of specialty gases. It packages and markets a full range of semiconductor specialty gases and is also a small player in the bulk gas market in West Germany. At the Special Gas Works in Duisburg, West Germany, the company operates its own purifying systems for many products. This center is equipped for producing, filling, mixing, and analyzing semiconductor gases. The company works closely with Hoechst on a wide range of R&D activities.
Asia/Pacific	
Bangkok Industrial Gases	Air Products joint venture in Thailand
Chronar Corporation	Joint venture in China
Chung Wang Industrial Gas	Air Products joint venture in Hong Kong and China
Daesung Sanso	L'Air Liquide joint venture in Korea
KBOC	BOC joint venture in Korea
Hong Kong Oxygen	Joint venture between L'Air Liquide and BOC in Hong Kong
Industrial Oxygen, Inc.	Nippon Sanso investment joint venture in Malaysia
Korean Industrial Gases	Air Products joint venture in Korea
Lienhwa	BOC joint venture in Taiwan
Malayan Oxygen	BOC subsidiary in Malaysia
San Fu Chemical	Air Products joint venture in Taiwan
Super Oxygen	Air Products joint venture in Malaysia

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Table 2 (Continued)

Primary Manufacturers and Suppliers of Semiconductor Gases

Region	Company Activities
Asia/Pacific (Continued)	
Thai Industrial Gases	BOC subsidiary in Thailand
Union Gas Company	Union Carbide subsidiary in South Korea
Shanghai BOC	The company is a 50/50 joint venture between Wusong Chemical Works and the BOC Group. Wusong provides the site at Shanghai; BOC provides 110 tons per day of liquefier for oxygen, nitrogen, and argon. BOC will also provide special gas technology for semiconductor technology.

Source: Dataquest March 1990

SEMICONDUCTOR GAS INDUSTRY BY REGION

There are notable differences among the regional gas markets. This section will address those differences from a semiconductor manufacturing perspective.

North America

The bulk industrial gas business in North America is dominated by a few large vertically integrated gas suppliers. These companies are Airco, Air Products, Linde, and Liquid Air.

Each company participates in all major areas in North America where semiconductor manufacturing is concentrated. However, because of the geographical size of the market, regional strengths among the suppliers are evident. These strengths are based largely on the location of bulk gas plants and the resultant economies associated with distribution of liquid product.

Liquid product accounts for 85 percent by volume of the product sold to semiconductor manufacturers in North America. Product is shipped by tanker truck and is stored in cryogenic tanks. The cost to truck liquid product is high which limits the service area of any given plant to a radius that is served in a cost-effective manner by a tanker truck.

In two areas with a high density of semiconductor manufacturers, gas suppliers have installed nitrogen pipelines to serve semiconductor facilities. Air Products in San Jose, California, and Phoenix, Arizona, and Linde in San Jose supply customers with low-cost gaseous product by pipeline. A pipeline is a very cost-competitive distribution system, provided that there is a high concentration of users that can share the expense of laying the pipe.

On-sites play a very small part in the distribution of bulk products to semiconductor facilities. It is difficult to justify the expense of an on-site gas plant, even with the volume of gas used by the largest fabs.

Another factor impacting the supply of bulk gas products to the semiconductor manufacturers is purity. The semiconductor industry is requiring industrial gas vendors to supply higher-purity

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products. Gas suppliers in North America responded by manufacturing high-purity product at the plant and providing stringent quality control throughout the delivery system. Quality control includes high-purity tanks and piping systems at the fab. The North American market has not accepted purifier technology to the extent that semiconductor manufacturers have in Japan.

The specialty gas business in North America is very different from the bulk gas business. The supply of electronic specialty gases is fragmented, with many suppliers participating in different niches within the market. Moreover, the supplier usually is not the primary manufacturer. Primary manufacturers typically are major chemical companies or one of the large industrial gas companies.

Chemical companies such as Du Pont do not directly market their gases. They sell large volumes to specialty gas vendors, which purify and package the product for semiconductor manufacturers. The chemical companies do not involve themselves in packaging the volumes required by semiconductor end users, nor have they invested in equipment required to purify and analyze these gases. Therefore, the intermediaries that consist of the specialty gas departments of major industrial gas suppliers and many smaller niche companies play an important role in adding value to semiconductor grades of specialty gases by purifying, packaging, and analyzing these products. They in turn market the gases directly to semiconductor manufacturers.

Japan

The Japanese bulk gas market is distinguished by three features. First, the market is dominated by one supplier, Nippon Sanso. Consequently, many of the other suppliers (i.e., Daido Sanso, Iwatani, Osaka Sanso, and Teisan) have allied themselves with foreign gas vendors in order to strengthen themselves against the formidable market penetration of Nippon Sanso. This tactic is evident in the large number of joint ventures and technology exchanges between Japanese and foreign gas companies.

The second distinguishing feature of the Japanese bulk market is the large number of on-site and single-site pipeline installations. This arrangement is a result of the close proximity of semiconductor manufacturers to large steel and chemical manufacturers that own and operate their own gas plants. A steel or chemical manufacturer becomes the gas vendor simply by installing a gas pipeline and selling excess capacity from its own plant.

The third distinguishing feature of the bulk gas market is the large installed base of purifiers. Instead of purchasing high-purity product, semiconductor manufacturers purchase purification equipment and purify the low-purity product at their fabs.

In the Japanese specialty gas market, as in North America, large chemical companies typically are the primary manufacturers of electronic gases. However, the Japanese chemical manufacturers take an active role in packaging the material, whereas in the other major markets the chemical companies sell electronic gases in large volumes to the gas vendors, which purify, package, and analyze the product.

In Japan, the marketing of specialty gases is complicated by a highly convoluted distribution network. Often, three or four intermediates lie between the primary manufacturer of the product and the end user. These intermediates may or may not be industrial gas companies. The final company in this chain is commonly referred to as the "gate keeper." The gate keeper is the company that has the established relationship with the end user; in many cases, this relationship is product specific. The responsibility of the gate keeper is to supervise the supply of that specialty gas (or gases). The gate keeper is selected directly by the customer, usually because of a

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longstanding relationship. Often, people employed by the gate-keeper company are retired employees of the customer company. The closest comparison to a gate keeper in the West is an external purchasing department.

Europe

The European industrial gas market has been impacted by two historical events. First, countries that have had strong industrial histories have built strong domestic gas industries and, in the United Kingdom, West Germany, and France, the primary domestic supplier has grown into an international supplier. As a result, the regional strengths of the European suppliers are largely defined by national borders.

In the northern bulk gas market, the United Kingdom is dominated by BOC. West Germany and Austria are dominated by Linde AG and Messer Griesheim. The Scandinavia countries are supplied by AGA. In the Southern European market, France is dominated by L'Air Liquide. Italy is supplied by several small domestic companies. Other European countries historically have not had the industrial mass to support a locally based company.

The second historical influence on this market was World War II. The destruction to the industrial infrastructure provided an opportunity for two American companies, Air Products and Union Carbide, to enter the market. It was the historical anomaly of World War II and the resultant destruction of the European bulk gas industry that opened a window for the American companies. This opportunity would not have existed otherwise.

From a technical standpoint, European gas suppliers have followed rather than led gas technology trends within the semiconductor application. This fact does not reflect on their technical capabilities but is more appropriately correlated to the historically small base of semiconductor manufacturers in Europe.

Far East

The Far East is undergoing a strong expansion of its industrial sector, and semiconductor technology is often the foundation of these countries' industrial policies. The Far East market is best defined as being in its development phase. The sophistication of local suppliers matches the growing prominence of semiconductor manufacturing in this region. The industrial gas technology is being largely transferred through joint ventures or wholly owned subsidiaries of the five major industrial gas companies in the world.

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Photoresist

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Photoresist

INTRODUCTION

This section discusses the fundamentals of photoresist processing and describes how photoresist materials contribute to that process. Photoresist chemicals and the chemicals associated with photoresist are described from a functional point of view; that is, they are described by the results that they accomplish rather than by their chemical structures.

PHOTORESIST OVERVIEW

Photoresist serves to define regions of the silicon substrate in which either material is selectively removed or impurities are added.

The photoresist process itself involves many steps. These include the following:

- Wafer Prime—Normally, a primer is applied to the silicon wafer as a first step. This primer improves the adhesion of the photoresist to the wafer.
- Photoresist coat and edge bead removal—A measured amount of photoresist is applied to the wafer and spun off. Toward the end of this cycle, a solvent is applied to the wafer to remove the buildup of material around the wafer circumference.
- Softbake—Heat is applied to the photoresist to drive out solvents and turn the photoresist from a liquid to a solid.
- Expose—Light is applied selectively to the photoresist through a patterned mask.
- Develop and Rinse—A liquid developer is applied to the resist to wash away areas of the resist as defined during exposure. Rinse is usually conducted with deionized water and serves to remove any traces of developer.
- Hardbake—The resist again is exposed to heat to further harden it so that it can withstand later processing steps.

Wafer Prime

Wafer prime is accomplished with materials, such as HMDS, that promote adhesion of photoresist to the silicon substrate. In the last few years, vapor prime has largely replaced liquid prime. Both types of prime use the same materials, but vapor prime is favored because it gives a more uniform result. Coincidentally, it also reduces the gallons of primer chemical consumed in photoresist processing by about 80 percent.

Photoresist Coat

During photoresist coat, resist is applied to the wafer and then spun off by rapid rotation of the wafer around its center. The thickness of the remaining resist layer is determined by the viscosity of the resist and the spin speed. The resulting resist layer is usually between 1.0 and 2.0 microns thick.

It is important to note that well over 99 percent of the resist applied to the wafer is spun off in the coating process. This amount can be calculated by observing that roughly 2/3 milliliter of resist

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is applied per inch of wafer diameter. On a 6-inch wafer, the resulting resist layer would be about 230 microns thick if none of the resist were spun off. If only 1.5 microns of resist remain, then more than 99 percent of the resist has been spun off.

During the last several years, the manufacturers of wafer track equipment have been striving to reduce the amount of photoresist that must be applied to the wafer. In North America, photoresist volume dispensed per wafer has been declining by 7 percent a year, assuming that the wafer size is constant.

Softbake

The softbake step is simply a heating process that results in evaporation of solvents in the resist. The solvents are evaporated to achieve two results: to avoid retention of solvent in the resist film, which would interfere in the exposure of the polymer, and to increase adhesion of the resist to the wafer surface.

Expose

For years, semiconductor manufacturers have used optical resists that are exposed with a light source in the visible spectrum. As the linewidths in semiconductor processing have shrunk, use of light with shorter and shorter wavelengths has become necessary. In 1989, the first significant numbers of steppers were shipped using a light source in the the ultraviolet range of the spectrum (I-line). Observers believe that ultraviolet light may have to be abandoned in the future in favor of deep UV, and eventually, soft X-rays. For reference, the following are the wavelengths of interest:

- G-line—436 nanometers (visible spectrum)
- I-line—365 nanometers (ultraviolet)
- Excimer laser—248 nanometers (krypton fluoride, deep UV)
- X-ray—1 nanometer, typically

G-line and I-line energy can be obtained from a mercury vapor ultraviolet lamp if suitable filters are used to exclude unwanted wavelengths. Krypton fluoride excimer lasers are used for the 248nm wavelength, and various sources (including synchrotron rings) are being considered for X-ray exposure tools.

Electron beams (e-beams) also are used to expose photoresist. In this process, the beam is swept across the photoresist much in the same way that a beam is swept across a TV set. Exposure times for this technique tend to be lengthy; for this reason, e-beam exposure tools are favored for prototype production rather than volume production. The advantage of an e-beam for prototype production is that no mask is required because the beam itself can be turned on and off to pattern the resist.

E-beams are used also in maskmaking. Today, most of the world's masks are produced using e-beam equipment.

A key consideration is that the method used to expose the resist determines the chemistry of the resist used. Generally, the same resist will not function at G-line, I-line, excimer, and X-ray wavelengths and will not be useful under e-beam exposure. For this reason, resists now are described functionally by the type of exposure for which they are designed to be sensitive as well as whether they are positive or negative.

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Currently, the linewidths used in semiconductor processing are shrinking at a rate of about 12 percent a year. The cutting-edge plants being built are typically designed to work at 0.8-micron wavelengths. As these linewidths shrink, it is possible to estimate the timing in which new photoresists will be required. Table 1 gives the technology, resolution, and approximate lifetime in the market for the various exposure wavelengths and techniques.

Wafer steppers are the current exposure tools of choice in the semiconductor industry. The linewidth a wafer stepper can accomplish in production is a function of the lens numerical aperture (NA) and the wavelength of light for which the lens is designed. Table 2 lists a number of lenses and the production resolution each is expected to achieve. This resolution is computed by the following formula:

$$\text{Resolution} = (0.8 \times \text{wavelength})/\text{NA}$$

Table 2 indicates that increasing the numerical aperture is as effective in lowering the linewidth as choosing a shorter wavelength of light. Unfortunately, increasing the numerical aperture reduces the depth of focus. A reduced depth of focus requires that the surface of the wafer be planarized to a high degree. Although attempts at planarization are under way, it is not clear at this time how successful these attempts will be.

Depth of focus is inversely proportional to the square of numerical aperture, so increasing numerical aperture reduces the depth of focus rapidly. The formula is as follows:

$$\text{Depth of focus} = (0.5 \times \text{wavelength})/(\text{NA})^{*}2$$

Table 1

Linewidth Timing
(12 Percent Per Year Shrink)

Technology	Resolution	Life
G-Line	0.8 micron	1978—2000
I-Line	0.7 micron	1989—2000+
Excimer	0.4 micron	1993—2000+
X-ray	0.1 micron	1995—2010
E-beam	0.1 micron	198X—2007

Source: Dataquest (August 1990)

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Table 2

Stepper Lenses
(All 5x)

Company	Numerical Aperture	Resolution
Nikon	0.55 G-line	0.63 micron
Nikon	0.45 I-line	0.65 micron
Canon	0.48 G-line	0.73 micron
Canon	0.45 G-line	0.78 micron
GCA	0.42 I-line	0.70 micron
Hitachi	0.40 I-line	0.73 micron

Source: Dataquest (August 1990)

Develop and Rinse

During the develop and rinse steps the soluble parts of the resist are washed away, leaving the resist pattern on the silicon. The developer chemistry must, of course, be compatible with the resist chemistry in order for this process to occur. Therefore, most resist suppliers also supply the developers that are intended for use with their resists.

Developers tend to be hazardous chemicals. Currently, OSHA restrictions are forcing the semiconductor industry to seek less hazardous developers. The resist suppliers are responding to this challenge by reformulating their resists and developers.

Hardbake

Hardbake is the second bake step in the photomasking procedure. Like softbake, its purpose is to evaporate the solvent in the photoresist in order to increase adhesion of the resist to the silicon surface. Hardbake occurs either after develop or after develop inspect.

Other Issues

Surface preparation and coating often make use of a surface primer such as HMDS. Good adhesion of resist to the surface prevents undercutting. Typically, the resist is spun onto the wafer and then over 99 percent is lost as it is spun off by centrifugal force. The film thickness is determined by both spin speed and viscosity (solids content) of the resist. After spinning, the resist is softbaked to remove solvents. This processing step is critical because it very definitely affects the subsequent development of the resists. Semiconductor process engineers often will hold a run of wafers prior to spin until an aligner is free. This allows them to spin, softbake, and move the wafer to exposure with little time delay. The short time delay ensures that the resist is exposed before its characteristics have a chance to alter.

The absorption during exposure and development is a function of wavelength and the amount and type of dye (if any) that has been added to the resist. It is subject to optical effects such as diffraction, scattering, and standing waves. These effects depend on the reflectivity of the

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underlying semiconductor material and may vary considerably depending on the step of the process the wafer has reached. The removal of exposed resist (or unexposed, in the case of negative resist) is accomplished during development carried out by either immersion, puddling, or spray puddling. Recently, there has been a marked trend to metal-ion-free developers because these offer less contamination of the underlying semiconductor material and improved device yields.

After development, the resist undergoes a post-bake treatment that increases its resistance to etching and may include deep UV as well as thermal stabilization. This step is most important if the wafer is to undergo subsequent dry etching or ion implantation during which the resist itself is used as a mask.

Etching and resist removal are both accomplished with wet and dry etching methods. The etchants and etching conditions depend on the layer of the semiconductor device that is being etched. Dry etch is becoming increasingly popular and may someday replace wet etch. Stripping (or resist removal) is also tending toward dry processing. The stripping requirements often depend on the post-bake treatment.

For all photoresist processing, broad process latitude is the name of the game. Semiconductor manufacturers demand consistent results, although operating conditions may vary.

Post-Photoresist Processing

After the resist has been applied and developed, it is then used to mask an etch or impurity deposition process, which is applied to the underlying silicon substrate. The resist must undergo many steps in this subsequent processing, and each of these steps makes different demands on the resist.

Etch steps include oxide removal, polysilicon removal, silicon removal, and metal removal. Each of these etch steps requires a different chemical; in practice, many of these steps can be accomplished through either wet or dry etch. Again, the demands on the resist vary according to the type of etch and whether the etch step is wet or dry. In particular, dry etch often removes the photoresist (although at a slower rate) as well as the material that is being etched. Process engineers seek a resist with a high differential etch rate so that the underlying substrate is completely etched before the resist is removed.

Impurity addition often is done with ion implantation. In this technique, ions of the desired material are accelerated through an electric field of several thousand volts to bombard both the resist and the underlying semiconductor material. The resist serves to trap the ions and keep them from hitting the substrate in areas where no impurity is desired. Unfortunately, this action tends to further harden the resist and make it difficult to strip.

High-dose implants harden the resist to an unacceptable degree. In this case, process engineers often add a silicon nitride layer to the silicon substrate. This nitride layer is patterned using the resist, which, in turn, is used to mask the high-dose implant.

Today, wafers may undergo 12 to 20 or more maskmaking steps. Each of these steps is likely to require somewhat different characteristics of the resist, for the reasons discussed in the previous paragraphs. At the same time, semiconductor manufacturers like to use the same resist for all mask layers, wherever possible. Therefore, significant testing and characterization are necessary to determine whether or not a resist will withstand all these different environments. Often, characterization of a new resist will take a year. For this reason, a new entrant to the market would not achieve significant sales penetration for at least a year.

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Performance factors that might be checked during resist characterization include resolution, contrast, contact hole cleanout, critical dimension control, control of resist over steps in the substrate, etch selectivity, adhesion, compatible developers, filtration, process-induced particles, coating uniformity, strippability, implant protection, thermal stability, shelf life, exposure latitude, and viscosity.

Strippers are used to dissolve the patterned resist after the pattern has been transferred to the substrate. Usually, a cleaning step is used after stripping to remove residual contaminants. Cleaners are usually a mixture of sulphuric acid and other chemicals. A trend is emerging toward the use of dry strip of photoresist, and this trend could impact stripper consumption.

PHOTORESIST CLASSIFICATION

Photoresists are described functionally by whether they are positive or negative and by the exposure method or wavelength to which they respond. Positive resists are those in which the resist remaining after development is the resist that was not exposed to light. Negative resists are those in which the resist remaining after development is the resist that was exposed to the light. Figure 1 illustrates the difference between positive and negative photoresist.

Historically, negative resists were used before positive resists. As the linewidths on semiconductor wafers became smaller, it became necessary to develop a new resist technology. It just happened that these new resists were positive rather than negative. Today, positive resist is thought to be synonymous with fine-line processing, although no real technical reason for this belief exists.

Negative Photoresists

The conventional negative resists that have been around for a decade or more utilize a cyclized rubber matrix with bis-aralyzides sensitizers. Xylene is generally used as the solvent in the resist. These resists are useful in the 3- to 5-micron range and above, and they are reliable and consistent with broad processing conditions. They are inexpensive ($90 to $100 per gallon) but are difficult to handle and can have some unpleasant side effects.

New negative resists have been developed to handle resolutions at 1 micron and below. Some of these resists have nothing in common with the older resists from a chemical point of view. Image reversal is another process that is being considered. This technique is claimed to enhance the contrast of the resist. Aqueous developers have been developed as a less hazardous alternative to developers currently in use.

Positive Photoresists

Today's popular positive resists typically use a novolac resin matrix together with a sensitizer and a cellulose acetate (toxic) solvent. The bulk of this product is sold for 1- to 3-micron resolution processing. New products are being developed with submicron resolution; these also contain a toxic solvent. It is claimed that these products are consistent with broad processing conditions down to the 0.6- to 0.7-micron range. These resists are relatively expensive ($350 to $450 per gallon). Some suppliers of emerging resists claim to have shown resolutions down to 0.5 micron using G- and I-line exposure, but there is some concern as to whether these linewidths can be controlled on a production line.

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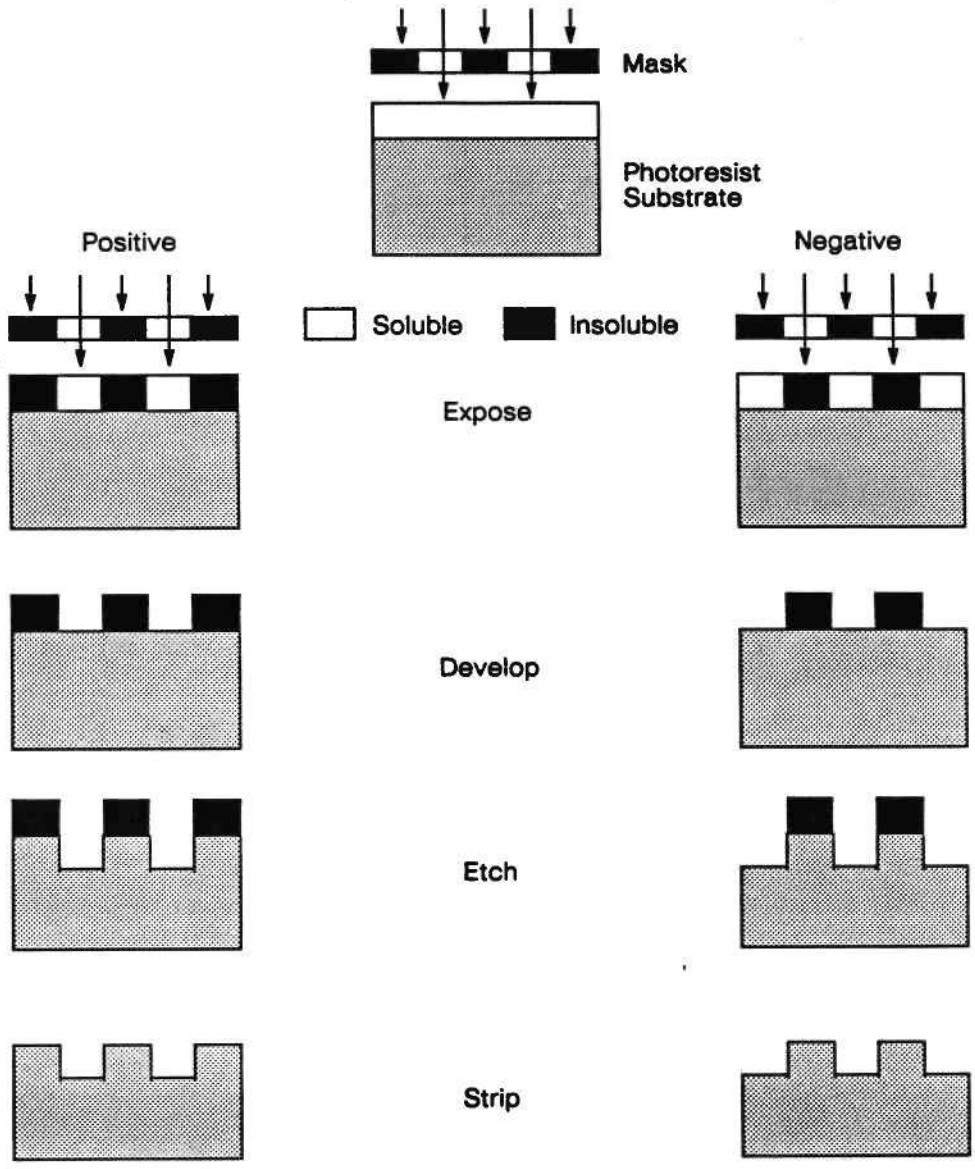
Figure 1

Mechanisms of Positive- and Negative-Working Photoresist



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Deep UV

Deep UV resists are under development. These will probably need to abandon the novolac resin matrix because this material is virtually opaque at the shorter UV wavelengths. Chemical amplification is being considered as a way of increasing sensitivity that might eliminate the need to find a substitute for novolac. The search for a new resist is being coordinated with excimer laser stepper (and SVG Lithography's Microscan aligner) developments.

E-beam

Electron beam resists are slow acting. They are used for limited production of semiconductor prototype parts and for maskmaking.

Other Issues

The photoresist business is characterized by an almost Byzantine complexity. Processes interact and are extremely sensitive, and everything that happens seems to depend on everything else. Dataquest likens photoresist processing to sailing a clipper ship: A clipper ship can cross the ocean almost as rapidly as a steamship, but the clipper ship demands much more attention from its crew because the technology is barely adequate for the task to be performed. Photoresist processing is similarly marginal. The marginal adequacy of photoresist processing can be appreciated by observing that semiconductor users are considering making 0.7-micron lines in resist that is more than 1 micron thick using light that has a wavelength of only 365 nanometers (I-line).

Photoresist processing is highly dependent on process equipment and operating conditions. A deep understanding and effective use of the technology is needed if the desired end results are to be accomplished. This means that the photoresist supplier must also supply a high level of technical service to ensure that the product is properly applied.

SUMMARY

The primary chemicals used in photoresist processing include primers, the resist itself, edge bead removers, developers, and strippers. Deionized water and various post-stripper cleaners also are used.

The resist itself can be further described in a functional manner by whether it is positive or negative and by the type of exposure it is designed for: G-line, I-line, excimer, X-ray, or e-beam.

Resist characterization is a difficult, lengthy process and limits the rate at which a supplier can generate new business. Qualifying a new resist at a semiconductor plant often takes a year. No overriding reason exists for a semiconductor manufacturer to initiate this qualification process unless the current supplier is not meeting service or technical needs. Semiconductor manufacturers are reluctant to change resist suppliers. One of the individuals interviewed for this study said, "Asking a process engineer to change to a new resist is like asking him to change all his blood for new blood. He will do this only in a dire emergency."

Future growth is expected to come from new, high-performance resists. The conversion to excimer resist may provide some opportunities for market penetration, as semiconductor companies will be required to characterize and implement a new resist chemistry whether they want to

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or not. The resist supplier will be able to ensure proper application of a new resist technology only by working closely with equipment suppliers which means working with photoresist processing equipment suppliers as well as exposure tool suppliers. The photoresist processing suppliers control the way the resist is handled, and the exposure tool suppliers control the way the resist is exposed. Both phases of the process are critically important. Exposure tool suppliers often recommend a brand of resist for use with their specific tools, and sometimes they guarantee results only with the specified resist. Obviously, this kind of endorsement can have significant market impact. Today, approximately 75 percent of the exposure tools shipped are built in Japan.

A worldwide marketing position is essential. Currently, 33 percent of the world's resist dollar consumption is in North America, 48 percent is in Japan, 11 percent is in Europe, and the remaining 8 percent is in the Rest of World (ROW) region.

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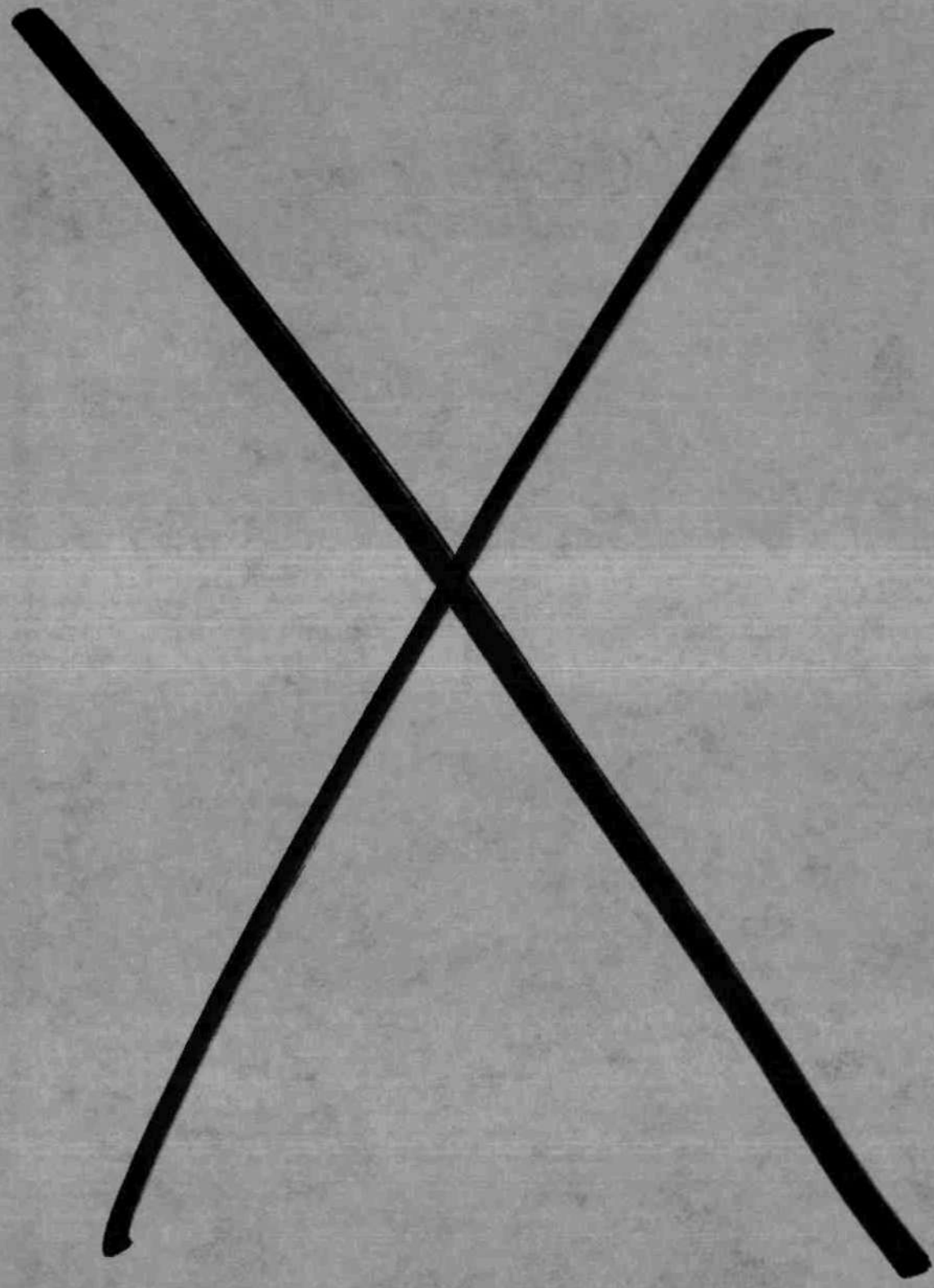

Industry & Technology Trends

The following is a list of the material in this section:

- Submicron Device Technology Trends

For additional information, please refer to the material behind the Industry and Technology Trends tab in your 1989 Newsletter binder.

Submicron Device Technology Trends

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Submicron Device Technology Trends

INTRODUCTION

In this section, we will highlight important trends in semiconductor device technology and circuits that are driving forces in the submicron regime. Every year, the International Electron Devices Meeting (IEDM) and the International Solid-State Circuits Conference (ISSCC) together provide a barometer of developments in semiconductor technology and devices. These two events provide information on important technologies being pursued by major IC manufacturers worldwide. In the context of these conferences, Dataquest will summarize key technology trends from the perspective of the semiconductor equipment and materials companies. These technology trends directly translate into requirements that have to be satisfied by the next generation of semiconductor manufacturing equipment and materials.

This year's IEDM, held in December 1988 and ISSCC held in February 1989 emphasized the continuing trend toward more complex process technologies and ultralarge scale integration (ULSI) products. CMOS technology continues to be the mainstream workhorse for high-density memory and logic products. With its advantages of high packing density and low power consumption, CMOS technology has enabled the realization of such ULSI memory products as 16Mb DRAMs, 4Mb SRAMs, and logic products such as application-specific integrated circuits (ASICs) with gate counts in excess of 100,000.

In their pursuit of high-yield, high-reliability products, semiconductor manufacturers have developed many approaches to solving the problems associated with ever-shrinking silicon area and cost per memory or logic bit. The development costs and risks associated with these major programs entail huge expenditures and a long-term commitment to submicron manufacturing. In order to ensure their participation in shortened market windows framed by rapid technological evolution, the major semiconductor companies are pursuing several alternative processing schemes at the same time. For example, DRAM manufacturers are exploring both stacked and trench capacitor cells for the 4Mb/16Mb generation. The availability of steppers with submicron photolithographic capabilities, together with other advanced front-end deposition and etch equipment, enable these complex process technologies to be realized in production.

Beyond 4Mb DRAMs and 1Mb SRAMs, Dataquest believes that the delays associated with long interconnect lines will become the performance-limiting factor. ASIC products will drive interconnect technology because of the nature of their random logic and routing requirements. There is a trend toward "system-on-a-chip" architectures for high-performance standard and ASIC products. New process technologies such as BiCMOS combine the high-density and high-yield attributes of CMOS technology with the high-performance attributes of bipolar technology.

A symbiotic relationship is evolving between advances in memory and logic process technologies. Memory products such as DRAMs and SRAMs push transistor performance, device-packing density, and high-volume manufacturing. Such memory processes are amenable to "hardwired automation," which helps the manufacturer move quickly down

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the cost/volume production curve. In contrast, ASIC and standard logic products push design automation, multilevel interconnect technology, and low-volume, flexible manufacturing systems.

In the first part of this section, we will discuss the trends in new memory and logic product technology presented at ISSCC Conference. The second part of this section discusses the associated device and process technologies presented at the IEDM.

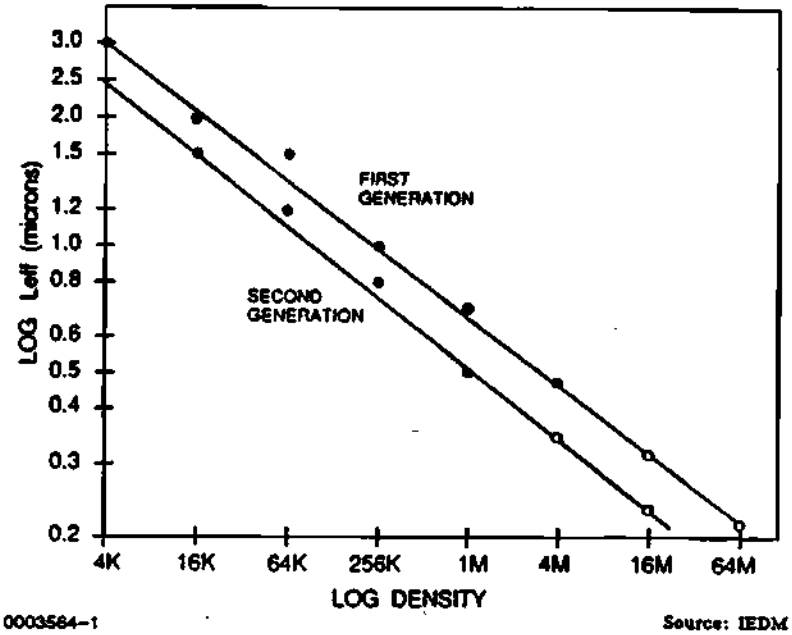
TRENDS IN MEMORY AND LOGIC PRODUCT TECHNOLOGY

This year's ISSCC gave a preview of many submicron memory, logic, and ASIC products. Memory products continue to advance in performance and density. Figures 1 and 2 illustrate the advances in SRAM density and access times. Figure 3 shows the key process technologies used for successive generations of SRAMs. Memory technology continues to drive device-level innovations at the silicon level. Effective channel lengths are approaching 0.5 micron for 1Mb SRAMs and 4Mb DRAMs based on advanced CMOS technology.

DRAM memory cell structures have become three-dimensional as manufacturers strive to reduce cell size by using trench capacitors or stacked capacitors. The objectives of continually reducing the cost per bit coupled with shrinking the area per bit have kept DRAMs at the head of the technology race. SRAMs are positioned next to DRAMs as technology drivers because of their emphasis on speed and their similarity to logic products.

Figure 1

SRAM Density Trends



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Submicron Device Technology Trends

Figure 2

SRAM Speed Trends

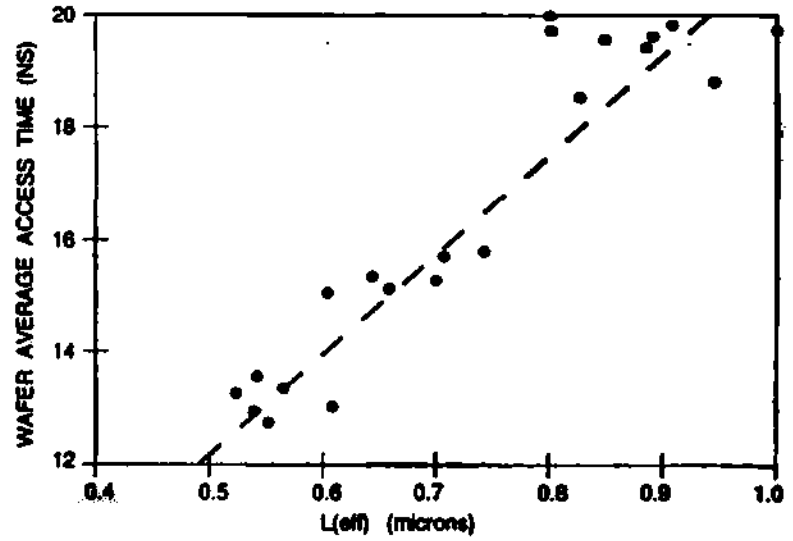

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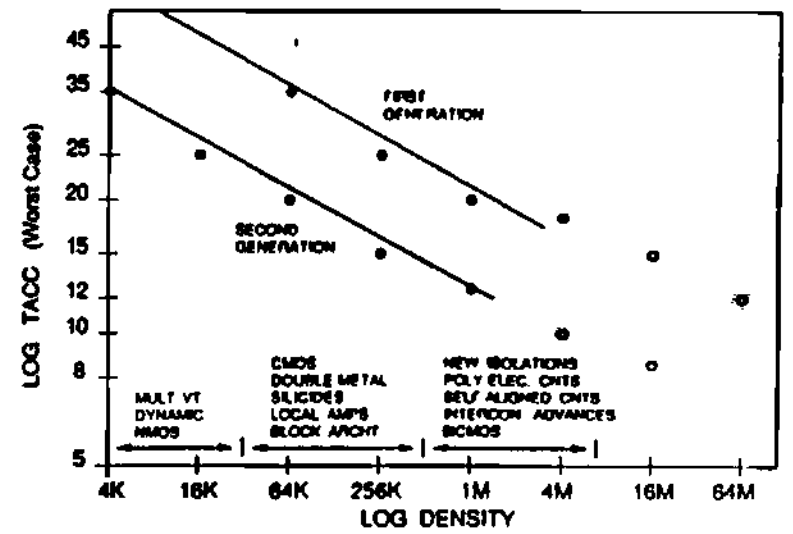
Figure 3

SRAM Technology Trends



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Submicron Device Technology Trends

Logic and ASIC products continue to drive design automation, interconnect technology, multiproduct flexible manufacturing, and high-speed testing. Also, new process technologies such as BiCMOS are used by SRAM, logic, and ASIC products, which need high performance and high packing density.

There is an emerging divergence in technology needs for memory and logic products. Three-dimensional capacitor cell structures are specific to DRAMs only and are not needed for SRAM and logic process technologies. Conversely, gate arrays and other ASIC products benefit immensely from triple-level metal technology and BiCMOS processes.

High-Speed SRAMs

At ISSCC, a variety of SRAMs ranging from 1Mb CMOS SRAMs to ECL/BiCMOS SRAMs with on-chip gate arrays for "smart" applications were presented. Speed is the main design objective for these submicron SRAMs.

Table 1 gives a summary of the design features for a variety of SRAMs presented at ISSCC. It is evident that all of these products are designed with submicron channel lengths and multiple layers of poly and metal. BiCMOS is a popular technology of choice for high-performance SRAMs because of its potent combination of high-density CMOS with the high-drive capability of the bipolar drivers. Texas Instruments and Toshiba have favored BiCMOS technology for their 1Mb SRAMs, while Hitachi has adopted pure CMOS technology for its 1Mb SRAM. Sony has adopted a pure CMOS technology for its experimental 4Mb SRAM.

Table 1

Key Features of SRAMs Presented at ISSCC

Company	SRAM Density	Technology	Minimum Design Rule (um)	I/O Level	Poly Layers	Metal Layers	Address Access Time (ns)	Cell Size (um^2)	Chip Size (mm^2)
Hitachi	16K	BiCMOS	0.5	ECL	2	2	3.5	28.6	9.7
Hitachi	36K	Bipolar	0.8	ECL	1	4	2.0	N/A	N/A
IBM	128K	CMOS	1.2	ECL	1	3	6.5	235.0	56.3
Hitachi	512K	BiCMOS	0.8	ECL	3	1	5.0	54.0	N/A
Hitachi	1Mb	CMOS	0.5	TTL	3	2	9.0	21.0	54.6
TI	1Mb	BiCMOS	0.8	ECL	1	2	8.0	77.5	120.0
Toshiba	1Mb	BiCMOS	0.8	ECL	2	2	8.0	49.8	107.0
Sony	4Mb	CMOS	0.5	TTL	2	2	25.0	21.1	130.0

N/A = Not Available

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Dynamic RAMs

Since last year's ISSCC, 16Mb DRAMs have gone from experimental chips to first-production prototypes. The DRAMs at this year's conference appear to be based on more conservative design rules than those shown last year. Mitsubishi, NEC, and Toshiba presented their 16Mb DRAMs. Table 2 gives a summary of the features of these 16Mb DRAMs. These chips were fabricated with 0.5- to 0.6-micron minimum design rules. Most Japanese companies also appear to favor extensions of the stacked capacitor cell for the 16Mb DRAM generation rather than adopt the more intricate trench capacitor scheme. Toshiba uses a combination stacked trench capacitor cell for its 16Mb DRAM. To ensure device reliability at 0.5-micron channel lengths, most manufacturers are using an internal 3.3V memory core power supply. On-chip voltage conversion is used to reduce the voltage from the external standard of 5V.

Table 2

Key Features of 16Mb DRAMs Presented at ISSCC

Company	Technology	Minimum Design (um)	Metal Layers	Cell Type	Cell Size (um^2)	Chip Size (mm^2)	Access Time (ns)	V_{CC} (volt)
Mitsubishi	CMOS	0.50	2	Stacked	4.8	134.8	60	3.3
NEC	CMOS	0.55	2	Stacked	4.1	130.4	55	5.0
Toshiba	CMOS	0.60	2	Stacked, trench	4.8	136.9	45	5.0

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Memory cell sizes range from 4.0 to 4.8 square microns, and the chip sizes are in the range of 130 to 135 mm^2. Access times for these 16Mb DRAMs are reported to be 45 to 60ns. The use of double-metal interconnect schemes is standard for all these 16Mb DRAMs.

A Novel Approach—200Mb Wafer Scale Memory

In a joint technology project, Anamartic Ltd. (United Kingdom) and Fujitsu (Japan) reported a revolutionary 200Mb wafer scale DRAM. Each wafer consists of an array of chips, each with a 1Mb DRAM core and additional control logic known as the configurational logic (CONLOG). Each CONLOG is connected to its four neighbors by signal lines that form logic networks on the wafer. An external controller transmits

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commands to each CONLOG element to set up links between chips and configure a continuous data path known as SPIRAL (see Figure 4). Upon completion of wafer processing, the SPIRAL data path is configured by external control software that tests and links the chips into a single, spiral-shaped data flow path. Figure 5 illustrates the interconnection of 1Mb DRAM chips on the wafer using software. No additional processing or hardwiring on the wafer is required to achieve the SPIRAL connection. The memory capacity is maximized through the use of partially defective chips in conjunction with a small EPROM within the wafer package. This EPROM defines the defective DRAM locations to be masked off.

The DRAM core and CONLOG circuit are designed using a standard 1Mb DRAM, 1.3-micron process. Table 3 shows the key technology features of the 200Mb wafer scale memory. The process uses double poly/single polycide/single aluminum technology. The CONLOG wiring layer is implemented in the polycide aluminum layers; thus, no additional processing is required to connect the DRAMs. The memory cell is a 3-D, stacked capacitor cell.

The 1Mb chip size is 13.65mm x 4.4mm including the common signal lines. This is about 20 percent larger than the standard 1Mb DRAM size. A 6-inch wafer will have 202 of these 1Mb chips, creating a potentially astounding 200Mb wafer-level memory component. The wafer is directly mounted on a printed circuit board along with associated signal chips and the EPROM chip. Figure 6 shows a photo of the 200Mb DRAM memory mounted on a printed circuit board.

Figure 4

Example of 200Mb Wafer Data Flow SPIRAL Chain

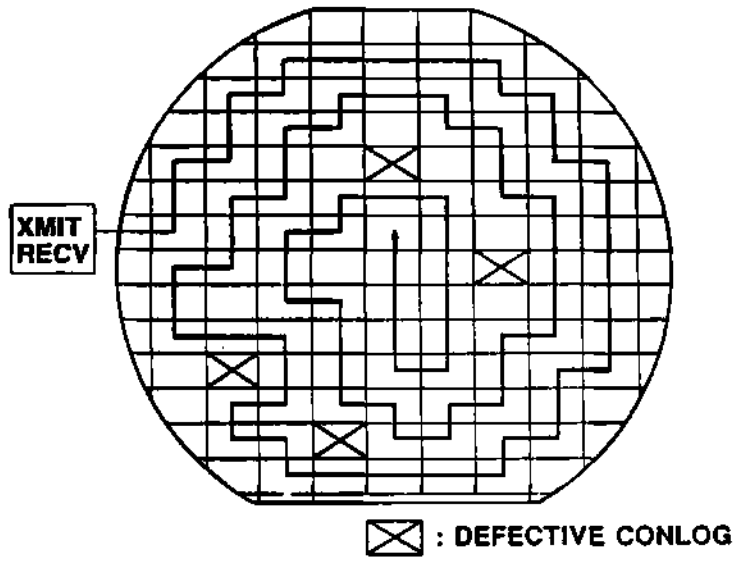

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Figure 5

Software Interconnection of 1Mb DRAM Chips on Wafer to Form 200Mb Wafer Scale DRAM

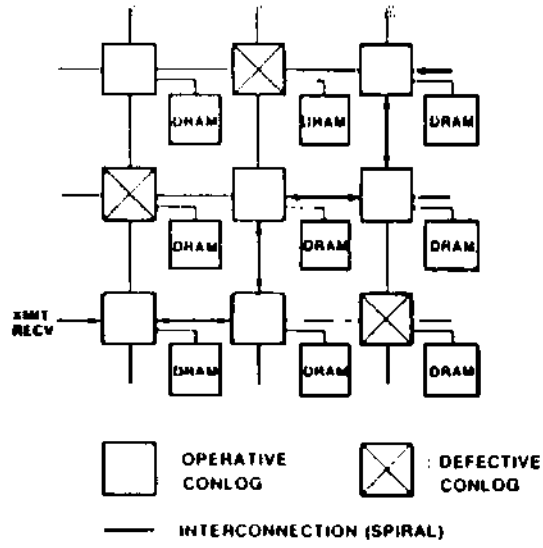

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Table 3

Key Features of 200Mb Wafer Scale Memory Presented at ISSCC

Process Technology	Double poly/single polycide/ single aluminum
Minimum Design Rule	1.3-micron n-well CMOS
Chip Size	13.65 x 4.40mm^2
DRAM Cell Size	21.8 mm^2
CONLOG Wiring Layer	Single polycide/single aluminum

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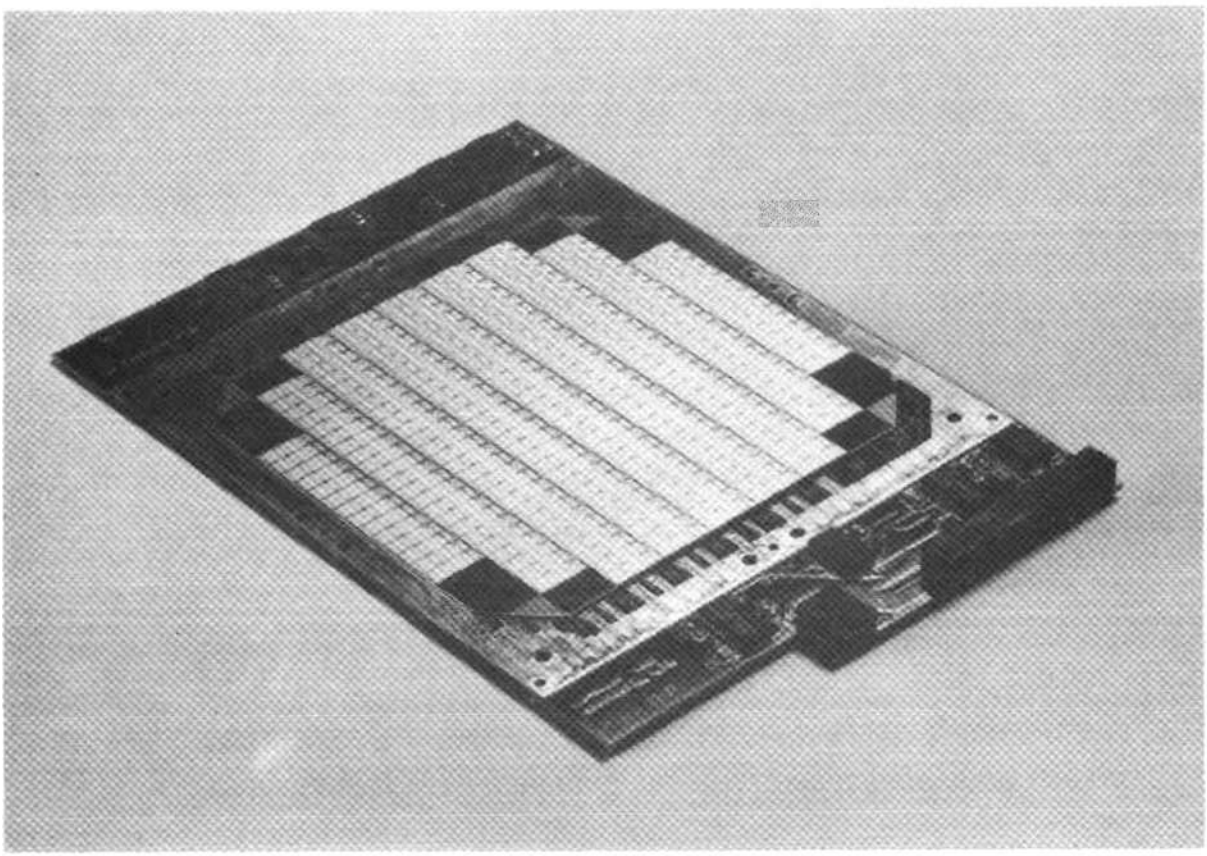
Figure 6

200Mb Wafer Scale DRAM Memory Mounted Directly on Printed Circuit Board



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Source: ISSCC

This wafer scale memory component represents a radical departure from the trends of shrinking device dimensions and increasing chip dimensions. By combining the advantages of a relatively mature 1Mb DRAM process technology with innovative logic design circuitry, Anamartic and Fujitsu have achieved wafer scale memory integration. Packaging costs and board space in systems are significantly reduced by this approach. Whether or not this technology is economically competitive in large-scale manufacturing remains to be seen.

Microprocessors

Microprocessors continue to become bigger and faster. CPUs with transistor counts of 440,000 and peak performance of 50 million instructions per second were presented at this year's ISSCC. Package complexity and pin count continue to increase proportionately. These CPU chips are now challenging mainframe computers in cost and

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performance. There is a continuing trend toward CMOS technology and RISC architecture. CPU designers are eagerly looking at submicron, low-power CMOS and BiCMOS technologies in their efforts toward developing single-chip ULSI logic systems.

Table 4 compares the average microprocessor's performance enhancements between 1987 and 1989 as presented at ISSCC. It is obvious that significant advances have been made in performance, density, and innovative architectures. Microprocessor technology continues to lag behind minimum memory design rules. Current microprocessor designs are using 1.2- to 1.4-micron CMOS technology, as compared with submicron DRAM memory features. However, CPU technology leads DRAM technology in its utilization of multiple levels of interconnect and polycide technology.

Table 4

Microprocessor Performance Comparison
1987-1989

	1987	1989
No. of Transistors	150,000	283,000
Frequency	16 MHz	32 MHz
Peak Execution Rate	13 mips	29 mips
Sustained Execution Rate	6 mips	18 mips
Cache Memory	1 kB	1.6 kB
Die Size	86 mm^2	144 mm^2
Technology	CMOS	CMOS
Minimum Design Rule	1.6 microns	1.4 microns
No. of Pins in Package	134 pins	236 pins

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April 1989

Gate Arrays

Gate arrays continue to dominate as the mainstream technology for ASICs. Gate densities continue to rise, with several companies reporting gate array sizes of more than 100,000. The choice of technology depends on the application. BiCMOS and ECL are used for high-performance ASICs, while CMOS is used for high gate count, large-volume commodity applications. Minimum design rules have entered the submicron regime with dimensions of 0.6- to 0.8-micron being reported. Channelless architectures with sea-of-gates implementation are the technology of choice for highly complex products.

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There is a trend toward using three or more levels of interconnect to achieve flexible routing and maximum gate utilization. Chip sizes continue to grow, with chips as large as 14.5 x 13mm^2 being reported. Table 5 shows the main features of gate array products described at ISSCC.

Table 5

Key Features of Submicron Gate Arrays Presented at ISSCC

Company	Array Size (Gate Count)	Technology	Min. Design Rule (um)	Metal Layers	Gate Delay (ps)	Chip Size (mm^2)
NTT	57,000	BiCMOS	0.80	2	450	102.2
Hitachi	130,000	CMOS	0.80	3	350	210.3
Mitsubishi	67,000	CMOS	0.80	2	405	42.0
Fujitsu	50,000	ECL	0.35	5	100	64.0
Mitsubishi	209,000	ECL	0.60	3	110	188.5

Source: ISSCC Proceedings (February 1989)
Dataquest
April 1989

TRENDS IN NEW DEVICE TECHNOLOGIES

As device geometries enter the submicron regime, entirely new and more complex technologies are being developed to overcome the numerous problems associated with shrinking dimensions and tighter process margins. As chip density and size increase, yield levels will drop. By switching to larger 6- and 8-inch wafers, device manufacturers will be able to achieve higher revenue per wafer. This trend toward more complex processes and 8-inch wafer sizes implies a very close coupling between the performance of the manufacturing equipment, materials, and devices.

The following processes highlight significant submicron device technologies and the associated equipment and material needs to produce submicron products.

Texas Instruments' 0.5-Micron Process

Texas Instruments (TI) reported that its new 0.5-micron CMOS process with 120-angstrom gate oxide yields a 20 percent speed improvement at 3.3V, compared with its 0.8-micron process with 200-angstrom gate oxide at 5V. N+ and P+ poly gates are used to ensure surface/channel operation and to minimize leakage. In order to reduce gate resistance and source drain series resistance, TI has developed a self-aligned titanium silicide scheme for gate/source drain strapping. The effective channel lengths for the n-channel and p-channel transistor are about 0.4 micron.

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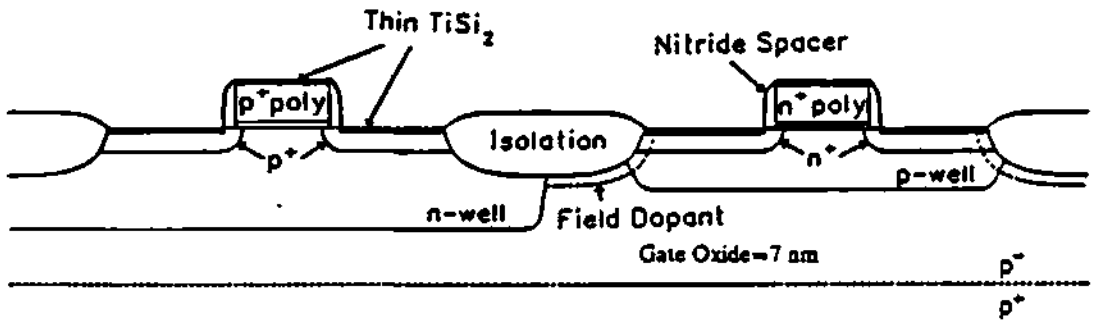
IBM's 0.25–Micron Process

Using its 0.25–micron process, IBM reported a 1.7X improvement in speed over its 0.5–micron process. IBM used a reduced operating voltage in the 2.2 to 2.5V range to improve device reliability. N+ and P+ doped poly was used to avoid buried channel operation while minimizing short–channel effects. The N+ and P+ poly are doped simultaneously with the masked N+ and P+ source drain implants. Again, self–aligned titanium silicide was used on gate and source drain to minimize active area resistances. The gate oxide thickness was 70 angstroms. Figure 7 shows the highlights of IBM's process.

Figure 7

Device Structure for IBM's 0.25–Micron Process



Source: IEDM

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Toshiba's Surrounding Gate Transistor (SGT) Submicron Process

Toshiba presented a novel submicron transistor structure for future ULSI devices. In this technology, the source, drain and gate are arranged vertically along the sidewalls of a vertical pillar island of silicon that is formed by a conventional silicon groove etch process. A 20nm gate oxide is grown on the sidewalls of the pillar, after which the gate N+ polysilicon is deposited and etched off everywhere except on the sidewalls of the pillar where it forms the gate electrode.

By using these vertical transistors, the area of typical CMOS circuits can be reduced to 50 percent of the area for conventional planar CMOS circuits. Toshiba reports that this technology has excellent transistor control characteristics and reliability. Figure 8 shows a schematic of the Toshiba SGT structure.

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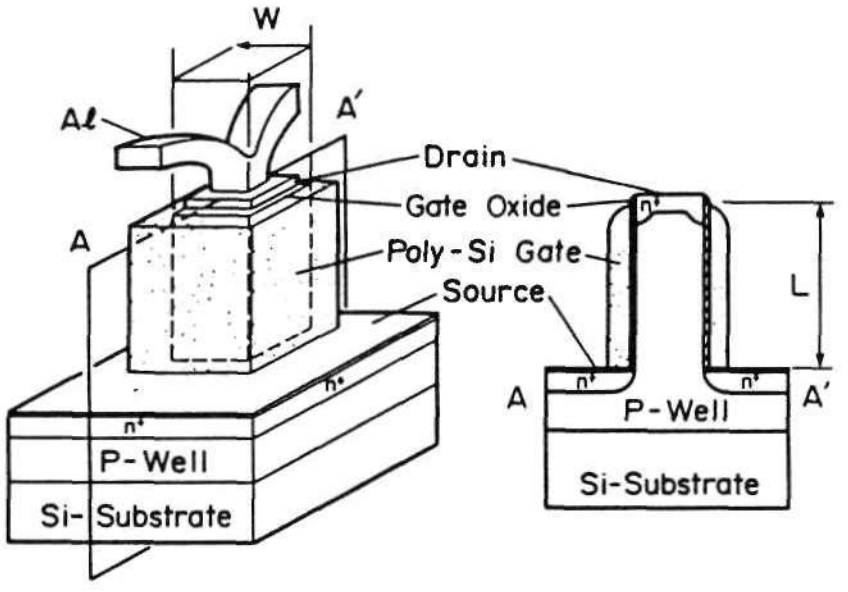
Figure 8

Toshiba's SGT Submicron Process Structure



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Source: IEDM

NEC'S Submicron Tungsten Gate Process

NEC has developed a submicron tungsten gate technology using a high-quality selective epi process. This technology gives a 30 percent improvement in transistor gain compared with conventional poly gate processes. The tungsten gate film was deposited by magnetron sputtering using a very high-quality target. Epi was selectively grown in a reduced pressure (30 torr) epi reactor at 900°C using SiH_2Cl_2-H_2-HCl gas chemistry. This epi film suppresses the short-channel effects in submicron MOSFET devices by reducing the channel depth. Figure 9 shows the main fabrication process steps for this technology.

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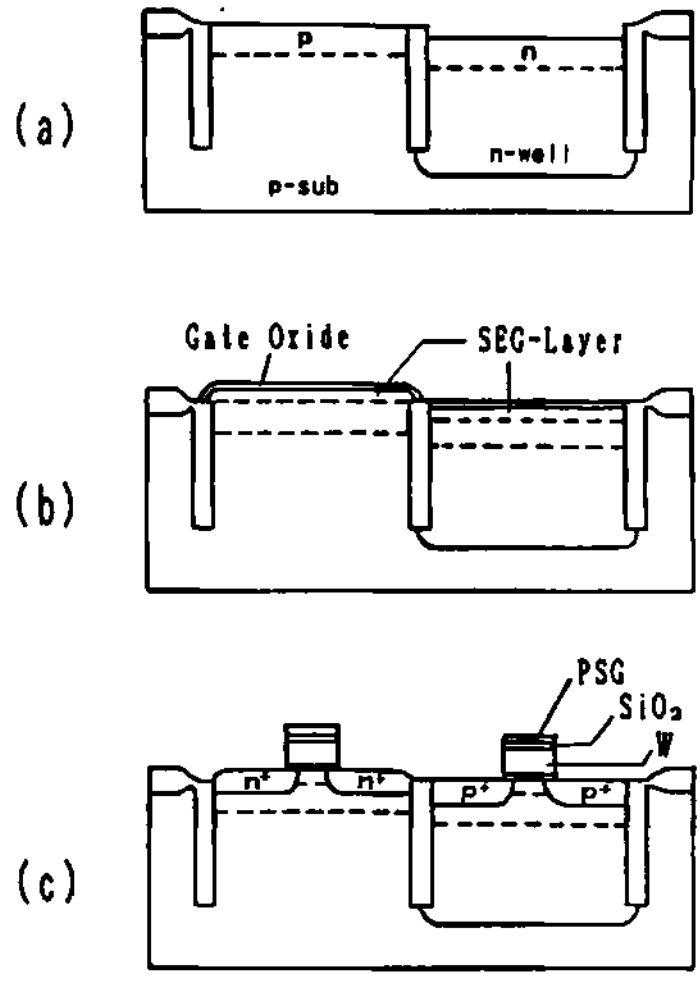
Figure 9

Process Flow for NEC's Submicron Tungsten Gate Technology



(a) Isolation region and punch-through prevention layer formation.
(b) Selective epi-layer growth and gate oxidation.
(c) Tungsten gate electrode definition and source/drain formation.

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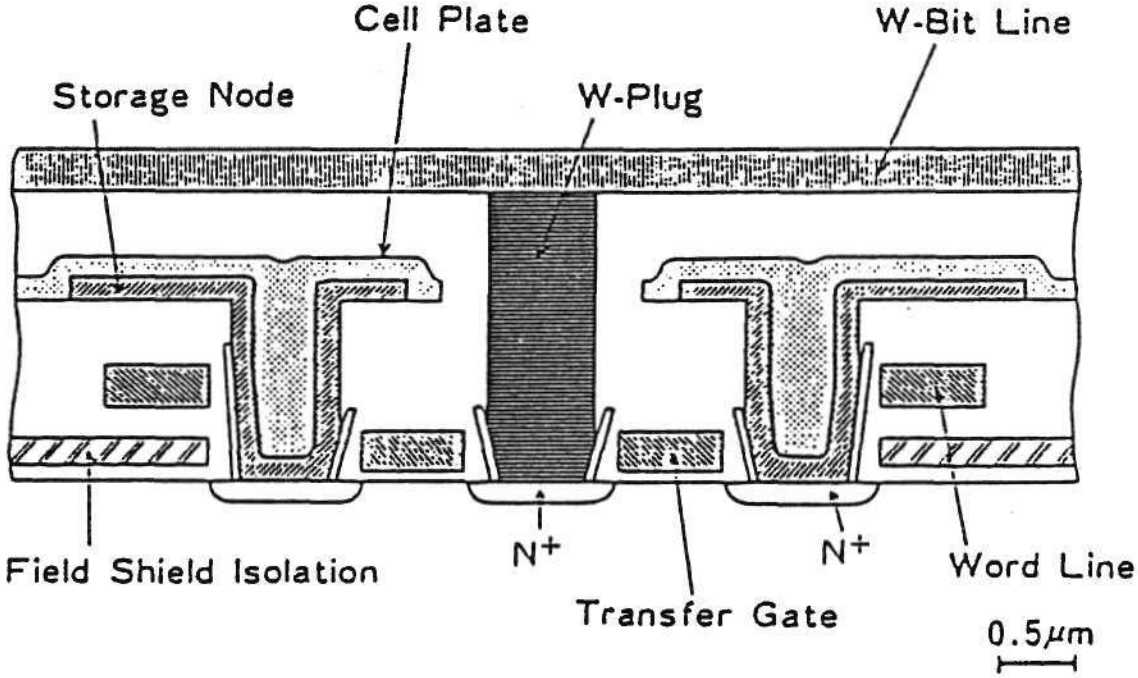
Mitsubishi's Fully Planarized 0.5–Micron Process

Mitsubishi used a "field–shield" isolation technology in conjunction with selective tungsten on the source drain regions for its 0.5–micron 16Mb DRAM process. The field–shield isolation is a three–layer structure consisting of a thin thermal oxide (field shield gate oxide), doped polysilicon (field shield gate plate), and a CVD oxide deposited on the polysilicon plate. The isolation region is implanted with boron to prevent turn–on of the field transistor channel. This isolation technique is completely free of the lateral encroachment that constrains conventional LOCOS isolation scaling.

The selective tungsten deposition reduces the source drain parasitic resistance and enables full planarization of the T–shaped stacked capacitor cell. The tungsten process uses SiH_4/WF_6 chemistry in a coldwall reactor at 300°C. Tungsten plugs were used to fill up contacts to the source drain regions. This creates a fully planarized structure. Figure 10 shows a schematic of the T–shaped stacked capacitor cell and the fully planarized topology.

Figure 10

Schematic of Mitsubishi's Fully Planarized 0.5–Micron Process



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TRENDS IN ISOLATION TECHNOLOGY

Trench Isolation

Trench isolation is very commonly used in submicron device technologies. For 4Mb and 16Mb DRAMs, the use of reactive ion-etched (RIE) trenches is popular. The main concern with the trench etch process is damage to the silicon lattice structure and consequent leakage and device degradation. This is of special importance to DRAM trench capacitors, which have charge leakage problems at the interface between the silicon trench sidewalls and the capacitor dielectric. Another concern with trench etching is the removal of the organic polymer film deposited on the sidewalls of the trenches during the RIE process. Unless these residual films are completely removed, leakage and device reliability problems can occur.

Shallow and deep trenches can be used for different purposes in this process. The shallow trench is refilled with a conformal CVD oxide and etched back for a planarized isolation structure. In contrast, the deep trenches are used for the DRAM capacitor. After the trench is etched, an appropriate wet clean is used to remove the polymer film residue. This may be followed by the growth of a "sacrificial oxide," which removes the damaged silicon layers. The high-quality capacitor dielectric is then grown along the sidewalls of the trench. Composite oxide-nitride-oxide (ONO) films grown thermally are commonly used. The ONO film combines the good qualities of the well-known silicon/oxide interface with the high dielectric strength of the thermal nitride film. Frequently, the ONO film is grown by an in-situ process of oxidation-nitridation-oxidation using rapid thermal processing equipment.

A conformal CVD oxide is crucial to refilling and planarization of the trench surface. The use of low-temperature tetra-ethyl-ortho-silicate (TEOS) undoped or doped CVD oxides enables a conformal trench fill. Boron-doped TEOS oxides are used to dope the sidewalls of the trench. This prevents trench sidewall inversion and parasitic leakage that would otherwise degrade DRAM memory retention characteristics. Figure 11 indicates a cross-section of the trench capacitor structure used in IBM's 4Mb DRAM process.

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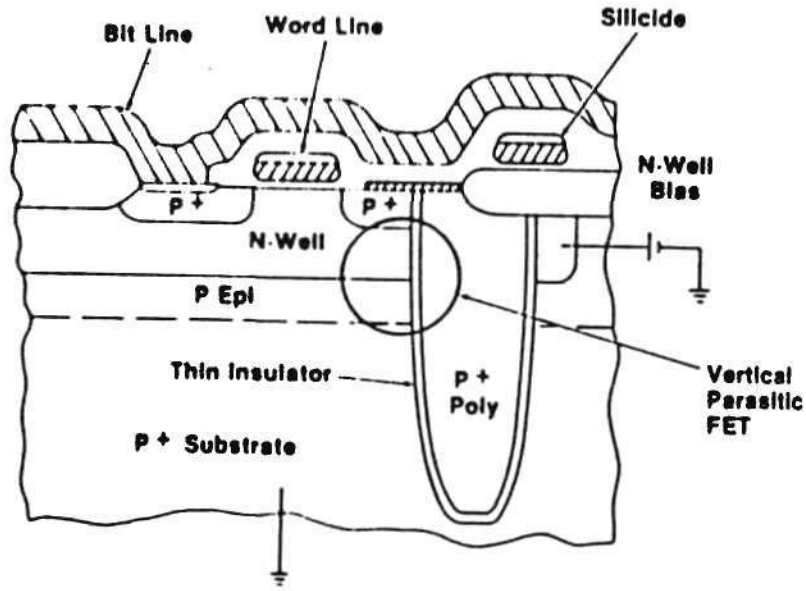
Figure 11

Cross Section of IBM's 4Mb DRAM Trench Capacitor Structure



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Source: IEDM

Mitsubishi's BIPS Technology

An alternative isolation technique reported by Mitsubishi is called buried insulator between source/drain/polysilicon (BIPS) technology. In this process, isolation is achieved by refilling a CVD oxide in field openings etched between source/drain/poly patterns. Subsequently, the surface is planarized by using double photoresist etchback. Mitsubishi concludes that 0.5-micron isolation can be achieved by this process without any field leakage or narrow channel effects.

Sony's APPL Technology

In Sony's advanced polysilicon pad LOCOS (APPL) process for 0.5-micron isolation, a thin layer (about 500 angstroms) of poly is sandwiched between the conventional LOCOS pad oxide and silicon nitride film. This variation of the standard LOCOS process inhibits lateral diffusion of oxygen, thereby restricting the lateral encroachment to less than 0.1 micron.

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TRENDS IN MULTILEVEL INTERCONNECT TECHNOLOGY

As minimum device geometries reduce to 0.5 micron and below, diffusion resistances and interconnect line resistances arrest the speed enhancements gained by submicron transistor dimensions. This will dictate the use of silicides and refractory metals at the source drain/gate level to reduce local interconnect resistance, while multiple levels of aluminum or tungsten will be used as global interconnects.

Local Interconnects

The use of self-aligned titanium silicide for reducing source drain/gate resistances is gaining popularity for submicron CMOS technology. However, the selective titanium silicide formation reaction is very sensitive to environmental conditions in the process. For example, the silicide process is adversely affected by the presence of oxygen in the environment. Also, long silicide reaction times in conventional furnaces can lead to oxygen incorporation and dopant diffusion within the silicide. This will increase the silicide resistance and degrade the device performance. To overcome this problem, semiconductor manufacturers are using rapid thermal processing (RTP) equipment for the silicide formation and anneal. The use of RTP also enables in-situ silicide anneal and formation of a titanium nitride barrier on top of the silicide. The titanium nitride barrier prevents aluminum interactions with shallow junctions in silicon. Such RTP-based silicide processes can reduce the diffusion and gate resistances by an order of magnitude to about 1 ohm/square.

As an alternative to titanium silicide, Mitsubishi used selective CVD tungsten to reduce the resistance of the source drain regions. The tungsten is deposited selectively on active areas using a process involving silane reduction of tungsten hexafluoride (WF_6). Mitsubishi has successfully fabricated 16Mb DRAM cells with this technology.

Tungsten can also be used as a gate material to replace doped polysilicon or poly/silicide composite gates. The advantages of tungsten as a gate material for submicron VLSI are its very low resistance and compatibility with VLSI processing. Recent reports from NEC Research Laboratories have solved some of the earlier problems associated with sputtered tungsten gates, such as reaction with gate oxides, oxidation of the tungsten during postprocessing, and mobile ion contamination from the tungsten sputtering targets.

Global Interconnects

Because of its low resistance and proven compatibility with submicron VLSI processing, aluminum will continue to be the material of choice for multilevel wiring. However, there will be variations in the composition of the aluminum alloy film and the technique by which the film is deposited. There also is an increase in the use of multilayered films involving sandwiches of barrier materials such as TiN and TiW with aluminum. These barrier films improve the reliability of the interconnect lines and the contacts to silicon.

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As contact sizes shrink below 1 micron, the step coverage of sputtered aluminum on the sidewalls of these steep aspect ratio contacts is very poor. Selective and blanket CVD tungsten is being explored for use as plugs to fill up the contacts and vias. CVD aluminum is being developed as an alternative to CVD tungsten for contact plugs in an attempt to replace conventional sputtered aluminum. CVD aluminum has the advantages of good step coverage and the ability to fill contacts and deposit interconnect films in the same reactor.

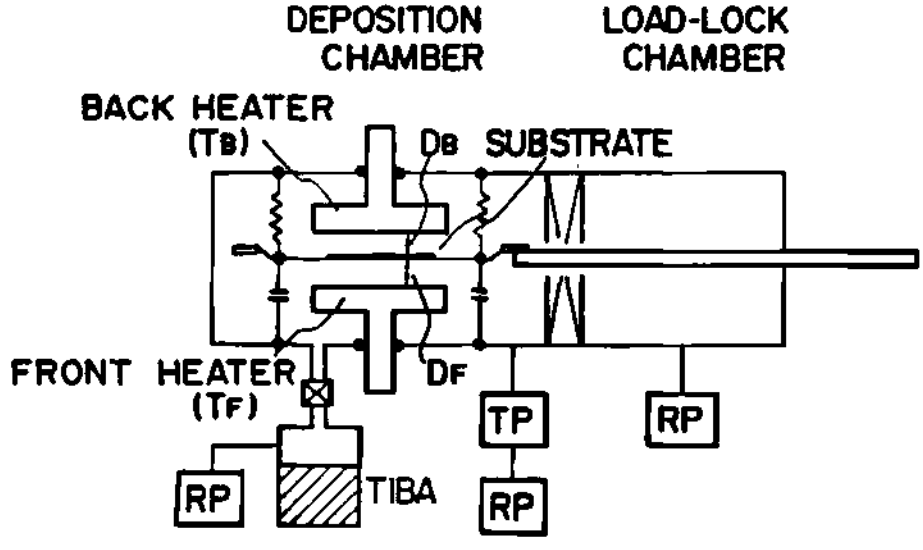
Future 0.5-micron multilevel interconnect technologies also will require full planarization between metal levels to enable good metal step coverage and patterning abilities.

Selective Plugs in Contacts and Vias

Nippon Telephone and Telegraph (NTT) LSI Laboratories reported selective CVD growth of aluminum using a newly developed double-wall CVD reactor. This system uses a process involving thermal decomposition of tri-isobutyl aluminum (TIBA). The wafer is placed between two heaters with different temperatures. In contrast to the earlier conventional aluminum cold-wall CVD reactors, which deposited very rough films, the new NTT reactor with its load-locked double-wall scheme gives very smooth aluminum films. The CVD process is highly selective and deposits only on silicon, metals, and silicides. It does not deposit on oxides. This feature is highly desirable for integration into a conventional double-metal CMOS process. NTT has demonstrated the process by fabricating 0.4-micron-diameter contact chains with reproducibly low resistance. Figure 12 shows a schematic of the NTT CVD reactor.

Figure 12

NTT's Selective Aluminum CVD Reactor



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Intel has developed a novel method of filling 1.5-micron contact holes using selective electroless metal deposition (SEMD). The process is based on the electroless deposition of palladium or nickel selectively in contacts plated with cobalt silicide ($CoSi_2$) or titanium silicide ($TiSi_2$). The deposition does not occur on dielectric films such as boro-phospho-silicate-glass (BPSG). A selective electroless contact plug technique such as this is compatible with normal CMOS processes.

Advances in Aluminum Alloy Interconnect Materials

Work is in progress on a broad array of alternatives to copper as an alloy element in conventional aluminum/silicon/copper metallization schemes. Al/Si/Cu alloys have serious problems in submicron interconnect applications. Some of these problems include linewidth reduction because of lateral erosion during dry etching and corrosion of metal lines because of copper chloride residues after dry etching and wet cleaning.

Hitachi Research Laboratories has developed a new sputtered aluminum-silicon-palladium alloy to replace Al/Si/Cu alloys. The masking and etching capabilities of 0.8-micron-wide Al/Si/Pd lines are demonstrably better than Al/Si/Cu lines. The long-term reliability of this new alloy apparently is significantly better than Al/Si/Cu interconnect materials.

Fujitsu Laboratories has developed in-situ carbon-doped aluminum metallization using a plasma CVD reactor. The in-situ doping of the aluminum film with carbon suppresses the growth of aluminum hillocks and spikes, which can cause metal-to-metal shorts between aluminum layers in the integrated circuit. The aluminum films were deposited by magnetron-enhanced plasma CVD in a parallel plate reactor with a pair of rectangular bar magnets. The source gas is trimethyl aluminum (TMA). The mean time to failure is an order of magnitude higher for these carbon-doped films compared with pure aluminum films. Fujitsu claims that these films will be useful for submicron interconnections and contacts.

Tungsten Interconnect Technology

Tungsten is receiving a great deal of attention as a material suitable for a variety of applications in submicron process technology. Several of the important applications are discussed herein.

Gate and Selective Local Interconnect

Gate and selective local interconnect applications of tungsten reduce gate and source drain resistances in submicron MOSFET operation. Cornell University and Stanford University report that this approach will increase packing density of submicron devices by making the source drain contact through the local tungsten interconnect extending over the field area. Packing densities are increased by eliminating the conventional design rule margins for contact misalignment and shape relative to the edge of the source drain. Figure 13 illustrates this processing sequence.

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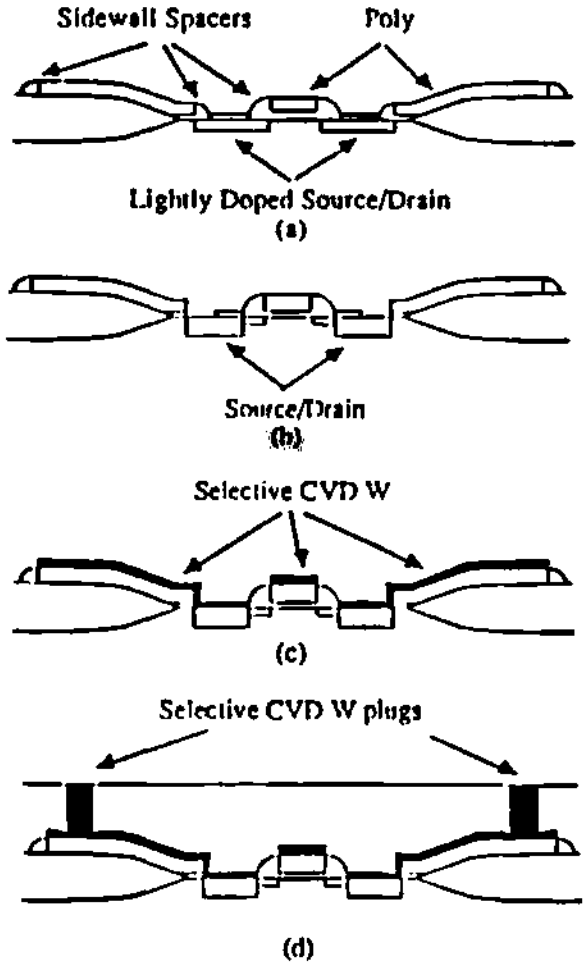
Figure 13

Processing Sequence of Selective CVD W Local Interconnect Technology



Cross-sectional view after (a) sidewall spacer formation, (b) selective removal of sidewall spacer of local interconnect and source/drain formation, (c) selective CVD W deposition, and (d) selective CVD W plug filling

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Contact and Via Tungsten Plugs

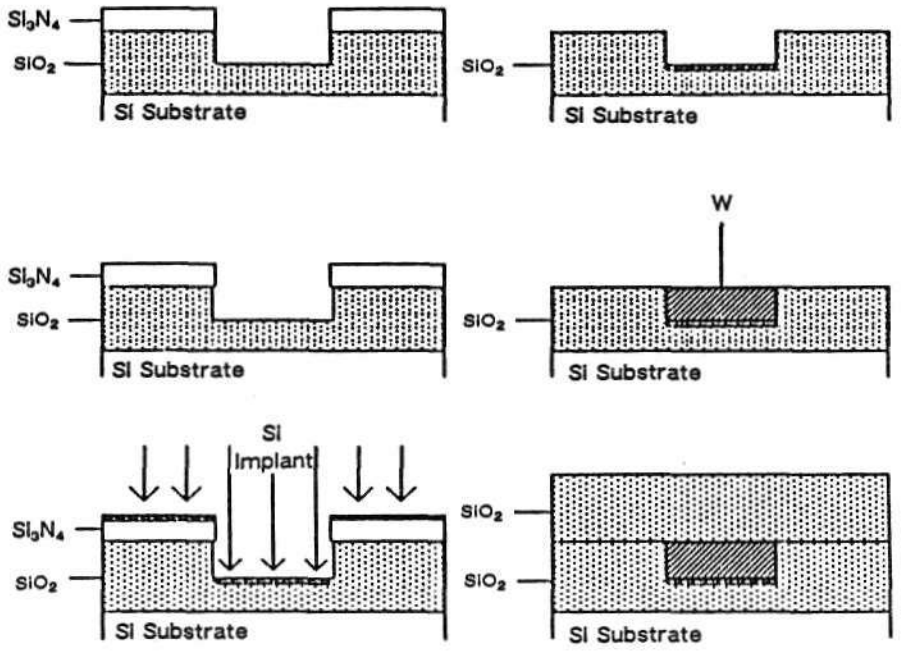
Work continues on developing tungsten CVD processes to solve the step-coverage problem in submicron vias and contacts. In order for these plug processes to be effective, it is necessary to achieve perfect planarization before every metal layer.

Multilevel Tungsten Global Interconnect

Cornell University has demonstrated the feasibility of an inherently planar multilayer tungsten interconnect process, which potentially solves some of the major interconnect problems in submicron VLSI circuits. This technology is based on implanting silicon in oxide channels that are later selectively filled with tungsten. The process has been extended to three levels of interconnect tungsten. The technology requires a fully planarized surface before the interconnect channels are etched into the oxide. After the first tungsten layer is selectively deposited, the succeeding topology is inherently planar by virtue of the process. This process has the advantage of allowing tight metal design rules by allowing self-aligned stacked contacts and vias. Cornell has demonstrated a 2-micron metal pitch at all levels. This tungsten-based interconnect scheme is more reliable than aluminum metallization. Figure 14 shows the sequence for the planar tungsten process.

Figure 14

Cornell University's Planar Tungsten Interconnect Technology



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DRAM CELL TECHNOLOGY TRENDS FOR 16Mb AND 64Mb DRAMs

As DRAM density reaches the 16Mb/64Mb level, the cell area needs to be reduced below 1.5 square microns in order for yield, die size, and package size to be economical. This goal directly translates into the use of even more complex process technology, aggressive lithography, and innovations in the cell architecture. In the following sections, we will analyze the key technological features of various DRAM cells and fabrication processes being explored by major DRAM manufacturers for their 16 Mb/64 Mb product generations.

IBM'S "SEOT" Technology for 64Mb DRAMs

IBM has demonstrated a new three-dimensional buried-trench (BT) memory cell suitable for DRAMs of 64Mb and beyond. The process uses a novel self-aligned epitaxy over trench (SEOT) technology, which allows the fabrication of the cell horizontal access transistor in bulk material grown epitaxially over the trench capacitor. The contact between the access transistor and the BT capacitor is a vertical, self-aligned connection to the trench. The process is based on an n-well CMOS epi technology.

The crucial step in this SEOT technology is the high quality epi material grown over the silicon trench capacitor. Figure 15 shows the key processing steps in the SEOT technology. The selective epi reactor must provide exceedingly good uniformity both across the wafer and from wafer to wafer within the lot. IBM used a conventional reduced-pressure barrel reactor. Epi films were grown at 900°C at a pressure of 40 torr using $SiCl_4$ and H_2 chemistry.

IBM has demonstrated a working DRAM cell with this process. The cell size is 7.8 square microns using 0.85-micron average design rules. With the advent of improved lithography processes, isolation, and self-aligned contacts, IBM expects this technology to be used in 64Mb DRAMs and beyond.

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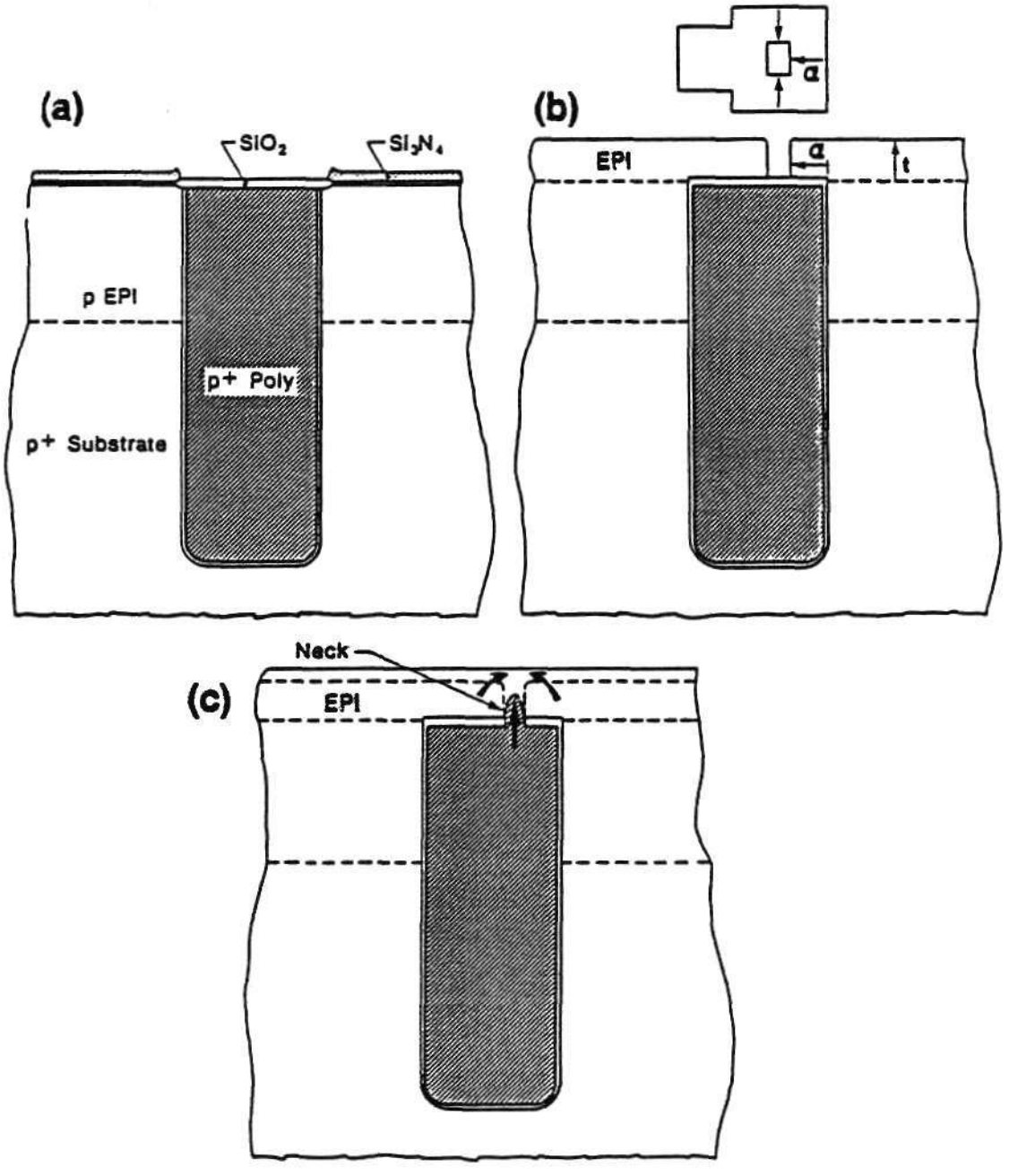
Figure 15

Key Process Steps of IBM's SEOT Technology for 16Mb/64Mb DRAMs



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Fujitsu's 3–D Stacked Capacitor Cell for 16Mb and 64Mb DRAMs

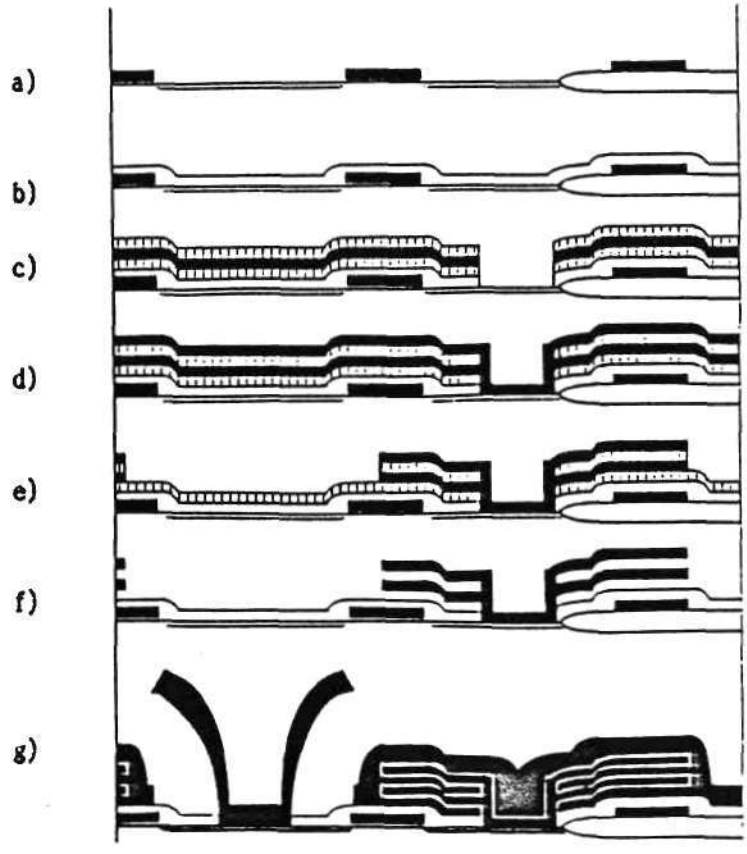
Fujitsu has developed a second-generation 3–D stacked capacitor cell for 16Mb DRAMs and beyond. Its new cell has two new significant features, as follows:

- It uses multiple "fin" horizontal storage capacitors.
- The bit–access lines are dilineated before the fin storage capacitor, thus enabling larger storage capacitance and easier patterning and contact hole formation.

Figure 16 shows a schematic of the fin structure and the fabrication sequence. Fujitsu has fabricated cells with two different design rules to demonstrate the viability of this technology. The cell areas are 1.8 square microns and 0.9 square microns with minimum design rules of 0.3 micron and 0.2 micron, respectively. The feasibility of 0.2–micron DRAM design rules has been verified using e–beam lithography.

Figure 16

Fujitsu's Stacked Capacitor Process Flow for 16Mb/64Mb DRAMs



a) transister formation
b) SiN deposition
c) SiO_2, polysilicon, SiO_2 deposition and contact hole formation
d) polysilicon deposition
e) storage electrode patterning
f) SiO_2 removal by HF solution
g) capacitor film growth, polysilicon deposition, cell plate and bit line formation.

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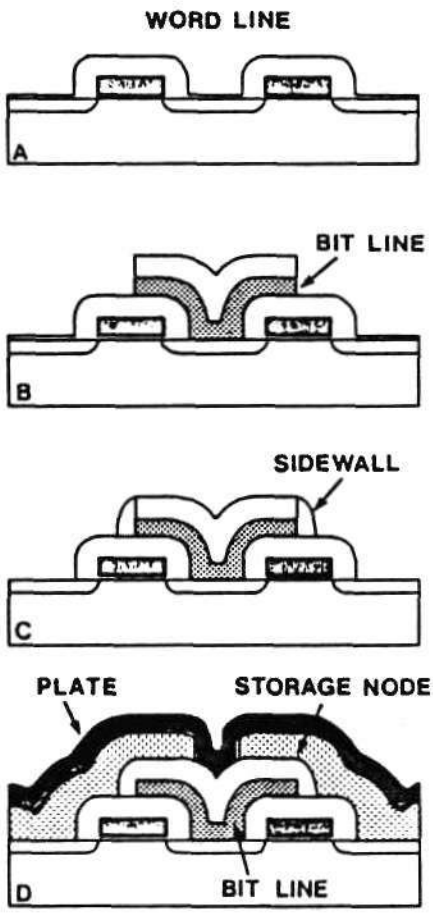
Hitachi's "DASH" Stacked Capacitor DRAM Cell for 16Mb DRAMs

Hitachi has reported a diagonal active stacked capacitor (DASH) cell for use in 16Mb DRAMs. One of the main disadvantages of the conventional stacked capacitor cell is that the bit access line must be connected to the memory cell transistor's drain through a window in the capacitor plate electrode. This results in problems of alignment tolerance between the capacitor plate and the bitline contact. Also, the capacitance margin is lower because of the reduced plate area. These problems can be solved by placing the storage capacitor over the bit access line and placing the active area diagonal to both the word access line and the bit access line.

Figure 17 shows the process flow for Hitachi's DASH process. Using design rules of 0.5 micron, Hitachi achieved a cell size of 3.36 square microns using a triple poly/single polycide/double metal technology. A 50-angstrom composite oxide-nitride thermal dielectric was used as the capacitor material.

Figure 17

Process Flow for Hitachi's DASH Process for 16Mb DRAMs



(A) Transfer gate formation,
(B) Bit-line formation,
(C) Bit-line isolation by sidewall SiO_2,
(D) Capacitor formation by storage node and plate.

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Toshiba's Stacked Capacitor Cell for 16Mb and 64Mb DRAMs

Toshiba has modified the conventional stacked capacitor cell process to allow for the increased capacitances needed for 16Mb/64Mb DRAM cell operation. In the conventional process, the bit access line contact is formed before the deposition of the lower plate capacitor. Toshiba increased the effective area of the capacitor by opening the bit access line contact window through the lower plate polysilicon. By doing this, Toshiba was able to achieve 30 percent more cell capacitance area for the same cell size.

As a variation of this technique, Toshiba was able to extend the technology to 64Mb DRAM cell requirements by etching the bit access line contact window 1 micron deep into the substrate silicon. This effectively increased the lower plate's area even more, thus increasing cell capacitance.

Toshiba used a 90-angstrom composite oxide-nitride material for the capacitor dielectric. Experimental 4Mb DRAMs have been fabricated with a cell size of 4.9 x 2.3 square microns using this new process. Figure 18 compares the process flow for the conventional stacked capacitor, the newly developed stacked capacitor, and the ultimate groove-etched stacked capacitor schemes.

In summary, we see that DRAM manufacturers are adopting a wide array of process technologies for submicron 16Mb/64Mb product generations. The availability of manufacturing equipment and materials capable of economically fabricating these complex structures in large-volume production is a prerequisite for future product generations.

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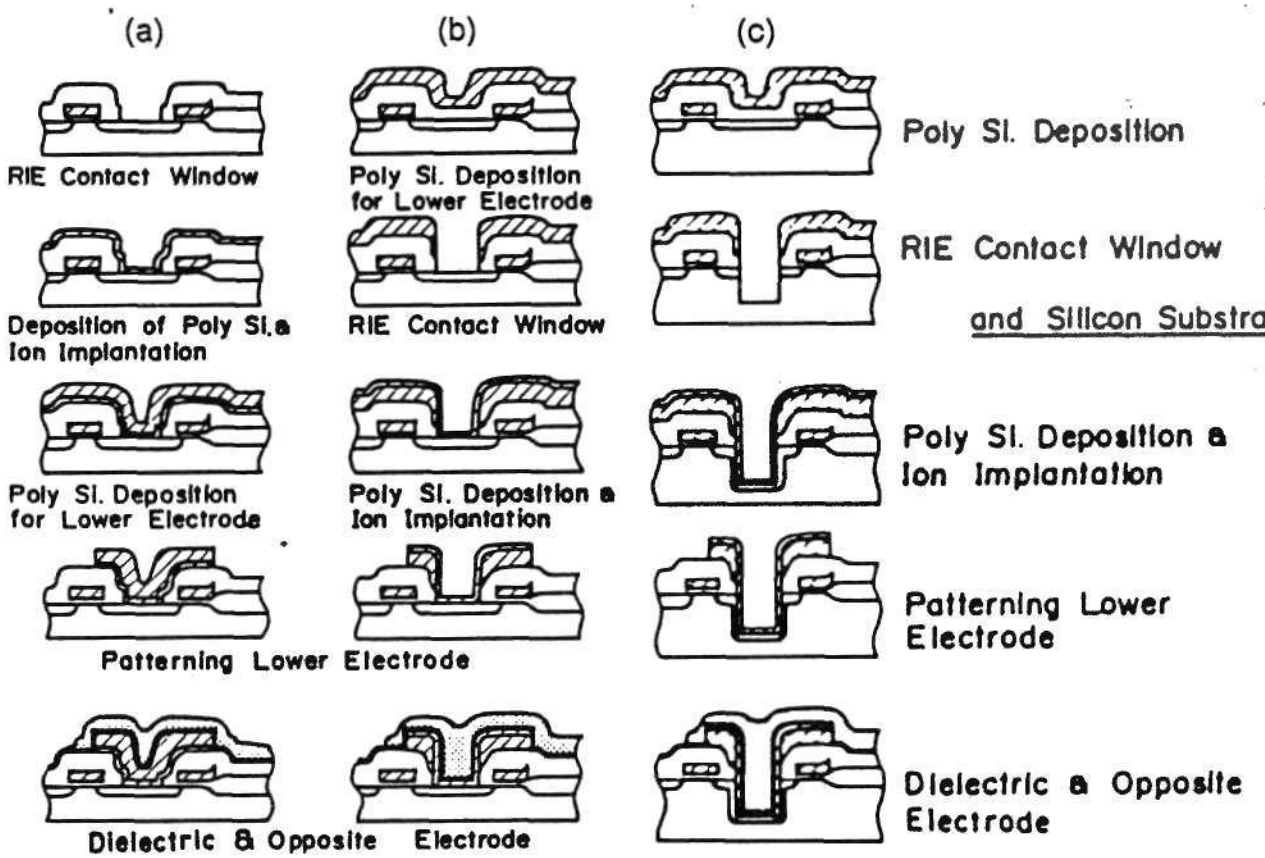
Figure 18

Process Sequence for Toshiba's Stacked Capacitor Technology for 16Mb/64Mb DRAMs



(a) Conventional STC

(b) Newly developed STC (Type I)

(c) Far evolutional STC (Type II)

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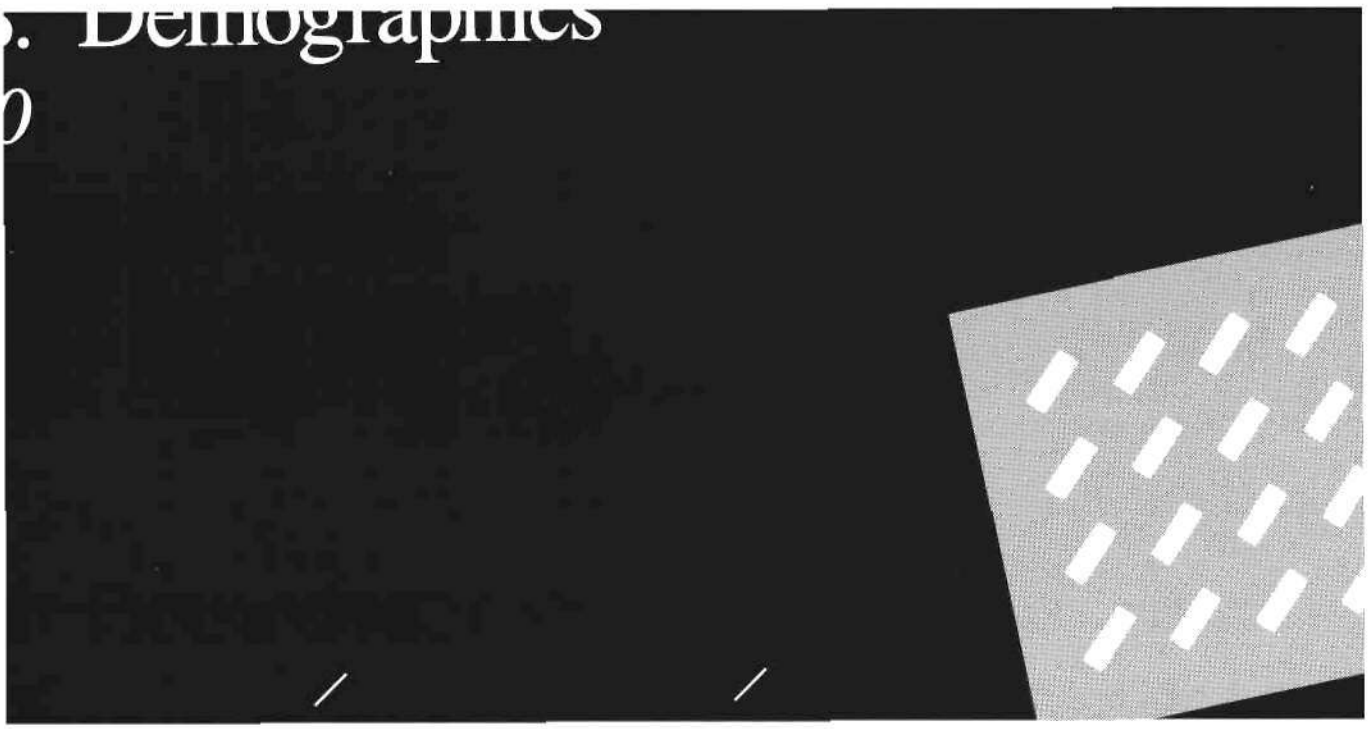
Demographics



U.S. Demographics

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Demographic Terms

CAGR (compound annual growth rate). Calculated using the formula:

$$CAGR = \left(\frac{\text{Value in year 1+n}}{\text{Value in year 1}}\right)^{\left(\frac{1}{n}\right)} - 1$$

civilian population. Resident population of the United States that does not include resident or overseas armed forces, merchant marines, or citizens living outside the United States.

corporation. A self-perpetuating body set up as a business entity separate from its owners. This means that ownership is separate from management and incurs limited liability.

desktop. Defined in Dataquest's desktop analyses as a potential location for a desktop information device.

elementary grades. Elementary grades are classified through the school district. If the district covers kindergarten through eighth grade, then up through eighth grade is considered elementary. If the district covers only through sixth grade, then only through sixth grade is considered elementary.

enterprise. An aggregation of establishments that have common ownership. This definition includes a parent company plus all of its subsidiaries and branches, as well as single establishments that have no financial links with other establishments.

establishment. A single physical location where business activity is conducted, whether or not there are any financial links to other units. Establishments include independently owned and operated businesses as well as the headquarters, subsidiaries, and branches of larger firms.

family. A group of two or more persons residing together who are related by birth, marriage, or adoption.

household. A housing unit intended as separate living quarters. A household includes all persons, either related or unrelated, living in the unit.

householder. The person in whose name the housing unit is owned or rented. The term is never applied to either husbands or wives in married-couple families, but relates only to persons in families maintained by either men or women without a spouse.

information worker. An individual who is or will be a user of an automated desktop information device.

median income. Indicates the value that divides the income distribution into two equal parts, one part having values above the median and the other having values below the median.

nonfamily. A group of two or more persons residing together who are unrelated.

occupational tenure. The cumulative number of years a person works in his or her current occupation, regardless of the number of employers, interruptions in employment, or times spent in other occupations.

other four-year colleges. A school that places its primary emphasis on undergraduate education. A four-year college can offer doctorate and professional degrees, but its graduate programs will not be as extensive as those of a university.

participation rates. Represents the proportion of the population that is in the labor force.

partnership. An association of two or more persons to carry on as co-owners of a business. Partners may be individuals, corporations, estates, trusts, or other partnerships and may be actively or passively involved in business operations.

secondary grades. Secondary grades are classified like elementary grades, by district. If the district covers eighth through twelfth grades, then grades eight through twelve are considered secondary. Likewise, if the district covers grades nine through twelve, then only nine through twelve are considered secondary.

sole proprietorship. A business that is fully owned and managed by a single individual.

total population. Includes all citizens, armed forces personnel, and merchant marines of the United States living at home or abroad.

two-year colleges. A school that offers an associate degree, but not a baccalaureate degree. Two-year colleges are also called junior colleges.

university. A school that places its primary emphasis on graduate and professional education. Universities offer doctoral studies in numerous fields and support at least two professional programs.

vocational school. A school that offers a certification in a specialized profession but does not offer classes applicable toward an associate or baccalaureate degree.

Education and Government Environments

The evolution of demographic changes in the United States has profoundly affected American society. One significant factor that has caused major shifts in school enrollment is the alteration in the fertility rate of women.

- The continuing effects of the baby boom (1946-1964) have caused enrollment at the elementary and secondary levels to:
  - Increase—1950s and 1960s
  - Decrease—1970s and early 1980s
  - Increase—Mid-1980s to late 1980s
- Higher education (postsecondary) enrollment has also been affected. Enrollment has:
  - Increased—Mid-1960s and 1970s
  - Peaked—Mid-1980s
  - Increased—Late 1980s
- Changes in the enrollment of elementary and secondary schools reflect shifts in school-age population. As women started having more children in the early 1980s, the school-age population began to increase.
- Enrollment in grades kindergarten through 8 will continue to increase well into the 1990s. However, enrollment in grades 9 through 12 is expected to decline through 1990, then begin to increase through 1997.
- Although enrollment in elementary and secondary schools was decreasing in the 1970s, the number of teachers in public elementary and secondary schools increased. Part of the increase can be attributed to a greater number of teachers required to implement special and bilingual education programs and smaller class-size policies. The number of teachers declined in the late 1970s and early 1980s. After 1983, the number of classroom teachers reached an all-time high of 2.3 million in 1987. This number is expected to reach 2.6 million by 1997.
- Although school-age population contributes to the enrollment of higher education institutions, the younger population is no longer the sole source of enrollment.
- The traditional college-age population is between 18 and 24 years old. This group declined from 30.4 million in 1981, to 27.4 million in 1987. This decline is expected to continue throughout most of the 1990s, reaching 24.0 million in 1997.
- There are several factors influencing changes in enrollment. Some of these factors are:
  - Economic conditions
  - Political and administrative decisions
  - Perceived value of a degree
  - Intrinsic value of higher education
  - College costs
- Although the traditional college-age population is declining, higher education enrollment will be supplemented by the increasing entrance of women, part-time, and older students.
- Preparing students for their post-education work experience is critical. As the required skill level to perform basic job tasks escalates, the demand on the education system to provide a solid foundation to meet these requirements is heightened.
- The 1990s will be a time for the education system and the workplace to join together and take action to keep the skill level of the work force in step with the rapid changes in technology and skill requirements.

In This Section

Tables E-1 through E-9 and G-1, and Figure 1 provide a general overview of education and government statistics. Areas covered in this section are number of schools, enrollment, expenditures, and government employment.

Table E-1. Number of U.S. Schools, Student Enrollment, and Instructional Staff

	Schools	Percent	Student Enrollment (Thousands)	Percent	Instructional Staff (Thousands)	Percent
Elementary						
Public	59,311	52.8	28,818	49.1	1,336	38.8
Private	15,303	13.6	4,097	7.0	256	7.4
Secondary						
Public	20,758	18.5	11,505	19.6	1,003	29.1
Private	2,438	2.2	1,175	2.0	96	2.8
K-12						
Public	2,179	NA	NA	NA	NA	NA
Private	4,949	NA	NA	NA	NA	NA
Other						
Public	1,000	NA	NA	NA	NA	NA
Private	2,926	NA	NA	NA	NA	NA
Subtotal	108,864	96.9	45,595	77.7	2,691	78.1
Higher Education						
Public	1,549	1.4	10,188	17.4	534	15.5
Private	1,908	1.7	2,899	4.9	221	6.4
Subtotal	3,457	3.1	13,087	22.3	755	21.9
Total	112,321	100.0	58,682	100.0	3,446	100.0

Note: Instructional staff for elementary and secondary education represents teachers exclusively.
Others includes special schools, vocational schools, and adult education schools.
Columns may not add to totals shown because of rounding.
NA = Not available

Source: Market Data Retrieval
U.S. Department of Education,
National Center for Education Statistics

Table E-2. Public School Systems and Student Enrollment by Enrollment-Size Class, 1988-1989

Enrollment Size (Students)	Number of Systems	Percent	Enrollment (Thousands)	Percent
0	195	1.3	NA	0
1 to 299	3,984	25.9	526	1.3
300 to 599	2,266	14.7	1,010	2.5
600 to 999	1,813	11.8	1,454	3.6
1,000 to 2,499	3,529	23.0	5,860	14.5
2,500 to 4,999	1,907	12.4	6,748	16.7
5,000 to 9,999	924	6.0	6,546	16.2
10,000 to 24,999	473	3.1	7,112	17.6
25,000 or more	177	1.2	11,233	27.7
Size Not Reported	108	0.7	NA	0
Total	15,376	100.0	40,489	100.0

Note: Enrollments and numbers of schools should be regarded as approximations only.
These totals differ from those in other tables because this table represents data reported by school districts rather than by states.
Columns may not add to totals shown because of rounding.
NA = Not available

Source: U.S. Department of Education, National Center for Education Statistics

Table E-3. Student Enrollment at U.S. Colleges and Universities, 1985-1995

	Total Enrollment	Four-Year Institutions	Two-Year Institutions	Percent Change
Actual				
1985	12,247	7,716	4,531	0
Estimated				
1986	12,397	7,753	4,644	1.2
1987	12,544	7,816	4,728	1.2
Projected				
1988	12,557	7,878	4,679	0.1
1989	12,570	7,857	4,713	0.1
1990	12,585	7,862	4,723	0.1
1991	12,529	7,831	4,698	(0.2)
1992	12,408	7,756	4,652	(1.3)
1993	12,300	7,679	4,621	(2.3)
1994	12,201	7,605	4,596	(2.6)
1995	12,151	7,563	4,588	(2.1)

Source: U.S. Department of Education, National Center for Education Statistics

Table E-4. Student Enrollment in Grades Kindergarten through 8 and 9 through 12 in Public and Private Elementary and Secondary Schools, 1985-1995 (Thousands of Students)

	Total Public and Private			Public			Private		
Year	K-12	K-8	9-12	K-12	K-8	9-12	K-12	K-8	9-12
Actual									
1987	45,547	32,101	13,446	40,200	27,983	12,217	5,347	4,118	1,229
Projected									
1988	45,522	32,475	13,047	40,280	28,439	11,841	5,242	4,036	1,206
1989	45,609	32,904	12,705	40,337	28,807	11,530	5,272	4,097	1,175
1990	46,092	33,542	12,550	40,752	29,366	11,386	5,340	4,176	1,164
1991	46,718	34,031	12,687	41,306	29,794	11,512	5,412	4,237	1,175
1992	47,366	34,470	12,896	41,879	30,178	11,701	5,487	4,292	1,195
1993	48,000	34,792	13,208	42,444	30,460	11,984	5,556	4,332	1,224
1994	48,635	34,980	13,655	43,014	30,624	12,390	5,621	4,356	1,265
1995	49,112	35,110	14,002	43,442	30,738	12,704	5,670	4,372	1,298

Source: U.S. Department of Education, National Center for Education Statistics

Table E-5. Institutions of Higher Education by Control and Student Enrollment, 1987

Student Enrollment	All Institutions		Universities		Other Four-Year Colleges		Two-Year Colleges	
	Number	Enrollment (Thousands)	Number	Enrollment (Thousands)	Number	Enrollment (Thousands)	Number	Enrollment (Thousands)
Public Institutions								
Less than 200	7	1	0	0	1	0	6	1
200 to 499	40	15	0	0	11	4	29	11
500 to 999	131	100	0	0	29	23	102	76
1,000 to 2,499	415	713	0	0	107	189	308	524
2,500 to 4,999	319	1,137	1	5	103	376	215	756
5,000 to 9,999	316	2,208	7	59	134	930	175	1,220
10,000 to 19,999	220	2,998	30	452	91	1,222	99	1,325
20,000 to 29,999	73	1,741	34	832	18	430	21	479
30,000 or More	28	1,063	22	841	2	71	4	150
Subtotal	1,549	9,976	94	2,189	496	3,245	959	4,542
Private Institutions								
Less than 200	400	41	0	0	283	29	117	12
200 to 499	395	133	0	0	235	79	160	54
500 to 999	393	284	0	0	307	224	86	60
1,000 to 2,499	463	716	0	0	423	654	40	62
2,500 to 4,999	148	509	6	25	139	473	3	11
5,000 to 9,999	68	465	24	183	43	275	1	7
10,000 to 19,999	33	424	24	313	7	82	2	29
20,000 to 29,999	5	125	5	125	0	0	0	0
30,000 or More	3	95	3	95	0	0	0	0
Subtotal	1,908	2,792	62	741	1,437	1,816	409	235
Public and Private Institutions								
Less than 200	407	42	0	0	284	29	123	13
200 to 499	435	148	0	0	246	83	189	65
500 to 999	524	384	0	0	336	248	188	137
1,000 to 2,499	878	1,429	0	0	530	843	348	586
2,500 to 4,999	467	1,646	7	30	242	849	218	766
5,000 to 9,999	384	2,673	31	242	177	1,204	176	1,227
10,000 to 19,999	253	3,422	54	764	98	1,304	101	1,354
20,000 to 29,999	78	1,866	39	957	18	430	21	479
30,000 or More	31	1,158	25	937	2	71	4	150
Total	3,457	12,768	156	2,930	1,933	5,061	1,368	4,777

Source: U.S. Department of Education, National Center for Education Statistics

Table E-6. Expenditures of U.S. Schools, 1986 (Millions of Dollars)

Type of School	Expenditures	Percent
Public Elementary and Secondary		
Instruction	89,559	61.1
Support Services	51,905	35.4
Noninstruction	5,125	3.5
Total, Elementary and Secondary	146,589	100.0
Higher Education		
Public Institutions		
Instruction	21,881	34.6
Research	5,705	9.0
Public Service	2,516	4.0
Academic Support	4,694	7.4
Student Services	2,922	4.6
Institutional Support	5,667	9.0
Operation and Maintenance	5,177	8.2
Scholarships and Fellowships	1,576	2.5
Others	13,057	20.7
Subtotal	63,195	100.0
Private Institutions		
Instruction	9,151	26.6
Research	2,732	8.0
Public Service	604	1.8
Academic Support	1,974	5.7
Student Services	1,641	4.8
Institutional Support	3,684	10.7
Operation and Maintenance	2,428	7.1
Scholarships and Fellowships	2,584	7.5
Others	9,543	27.8
Subtotal	34,341	100.0
Total, Higher Education	97,536	
Total	244,125	

Source: U.S. Department of Education, National Center for Education Statistics

Table E-7. Ratio of Students to Microcomputers in Public Schools

Grade Level	School Year 1985-86*	1986-87*	1987-88	1988-89	1989-90
Elementary	55.3	43.7	36.8	32.4	28.0
Junior High	41.6	32.9	27.6	23.8	22.0
Senior High	37.9	31.1	26.3	22.8	20.5
Total	45.5	36.5	30.8	26.9	24.1

Note: Total represents all public schools including K-12, but excluding schools of special education. Data are preliminary.
Source: Market Data Retrieval
*Data collection was limited to those schools with a microcomputer.

Table E-8. Installed Base of Microcomputers in Public Elementary and Secondary Schools by Manufacturer and School Year

	School Year				
Manufacturer	1985-86	1986-87	1987-88	1988-89	1989-90
Apple	460,900	632,900	783,400	930,600	1,072,000
Tandy-Radio Shack	139,000	155,800	171,900	178,200	183,000
Commodore	116,300	130,900	140,400	141,600	138,000
IBM	42,100	68,200	108,900	147,700	189,000
Others	84,300	94,100	107,600	124,900	125,000
Total	842,600	1,081,900	1,312,200	1,523,000	1,707,000

Source: Market Data Retrieval

Table E-9. Microcomputers for Student Instruction in Elementary and Secondary Schools, 1986-1988

	Number of Schools				Percent with Microcomputers			
Year	All	Elementary	Junior High	Senior High	All	Elementary	Junior High	Senior High
1986	80.5	50.7	9.7	15.1	95.6	94.9	98.5	98.7
1987	80.6	50.9	9.7	15.0	96.4	96.0	98.6	99.0
1988	80.8	51.0	9.8	15.0	97.1	96.8	98.8	99.1

Source: Market Data Retrieval

Figure 1. Installed Base of Microcomputers in School for School Year, 1989-1990

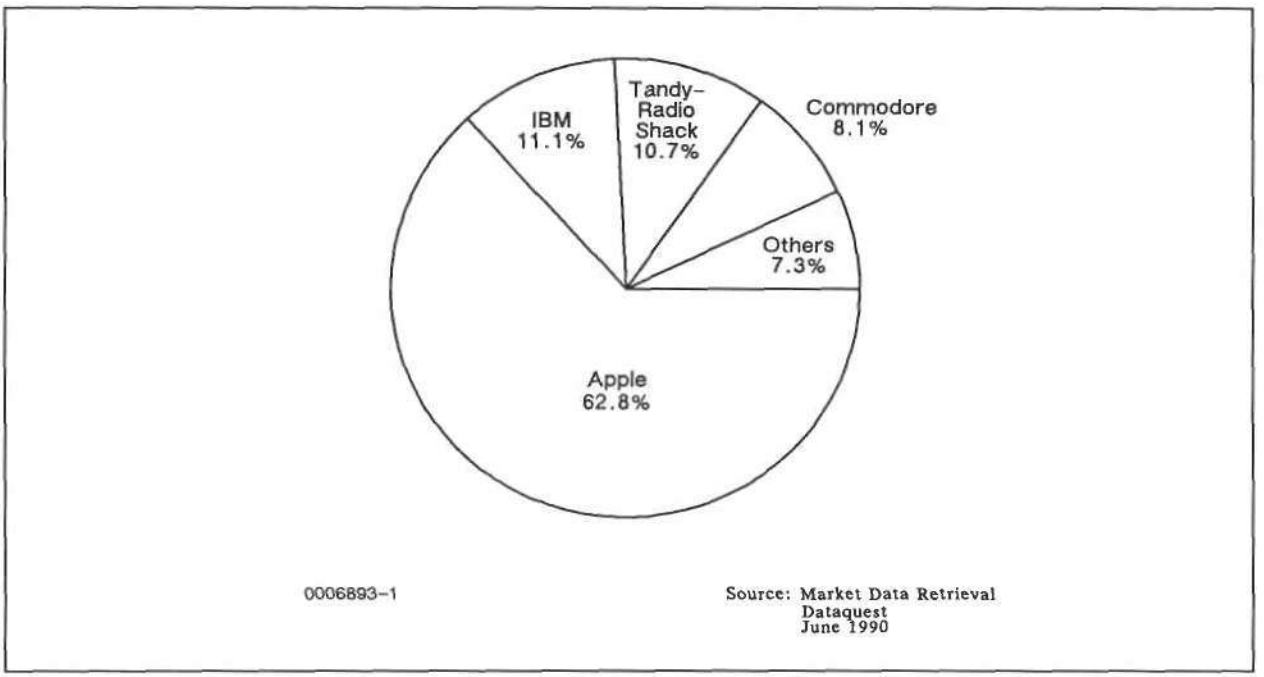


Table G-1. Federal, State, and Local Government Employment by Industry Sector, 1988

SIC Category	Employees
Construction	188,500
Manufacturing	126,039
Transportation and Public Utilities	480,541
Retail Trade	80,655
Services	8,503,458
Hospitals	1,253,829
Social Services	285,018
Amusement and Recreation	138,445
Educational	5,525,277
Elementary and Secondary	5,087,240
Colleges and Universities	1,250,769
Public Administration	6,098,305
U.S. Postal Service	834,673
Total	16,312,171

Source: U.S. Department of Labor, Bureau of Labor Statistics

Households and Population

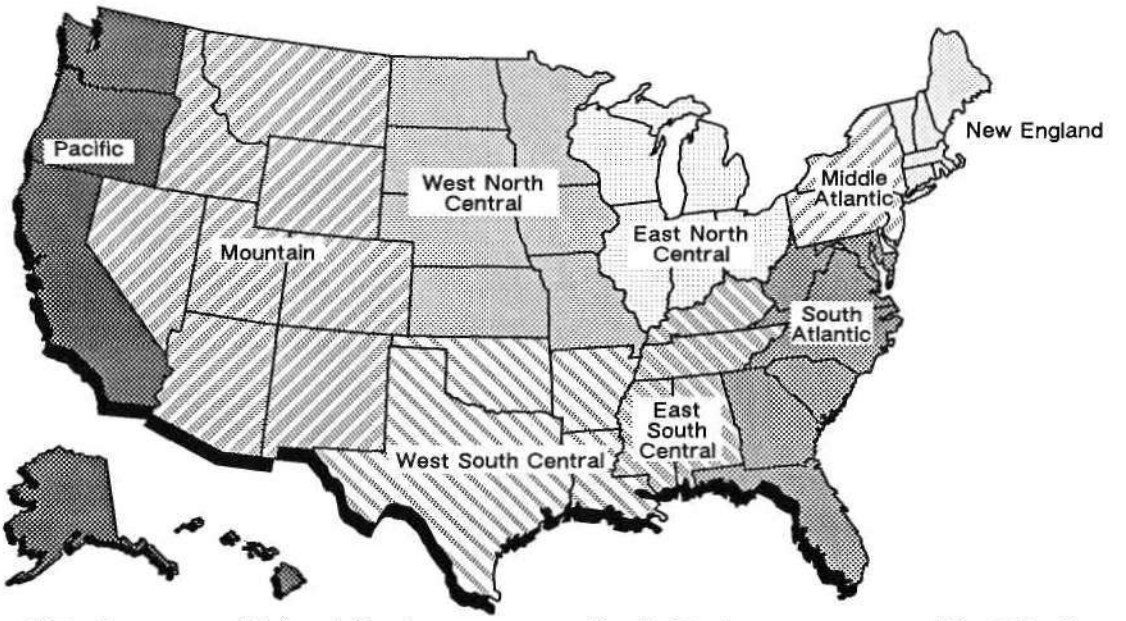
The phrase "traditional nuclear family" is rapidly becoming a sociological term describing the past in American society. As the new decade begins, the movement away from the two-parent, one-income family with children shall continue. This transition time will give rise to an increase in nonfamily, single-parent households, and dual-income marriages without children.

- The percentage of households composed of a married couple with children in the home is 26 percent, down from 31 percent in 1980.
- The fastest growing household classification is people living with nonrelatives. Although the number of households of this type has increased, it accounts for only 5 percent of total households.
- The overall number of households has grown steadily for decades. In 1910, there were 20.3 million households, increasing in number to 92.8 million in 1989.
- In 1989, 16.5 percent of all family households were maintained by women without a husband present, compared with 9.2 percent in 1950. Two contributing factors to this increase are:
  - A greater number of women participating in the work force
  - A higher incidence of divorce than ever before
- The median age for first marriages is getting older. In the late 1980s, the median age for women getting married for the first time was 23.6 and 26.0 for men. These ages compare with the 1950s, when the median age for first marriages was 20.1 and 22.5 for women and men, respectively. The rise in median age for first marriages will have implications on initial and lifetime fertility rates and marriage dissolution. Those couples who are older at the time of their first marriage have fewer children born and a lower incidence of divorce.
- Almost one-fourth of family households with children are maintained by a single parent.
- Nearly 9 out of 11 children living with a single parent are with their mothers. Unfortunately, many women in this circumstance have lower than average incomes. Subsequently, children raised in poverty are at higher risk of low educational attainment, more frequent crime involvement, and out-of-wedlock childbearing.
- The current social patterns in childbearing point to the continuation of small family units as the norm for the nineties.
- Five states have grown by at least 10 percent since 1985. These increases are significantly higher than the national rate of 4 percent. The five states are:
  - Nevada—18 percent
  - Arizona—12 percent
  - Florida and New Hampshire—11 percent
  - California—10 percent (Overall growth in California—2.7 million—accounted for more than one-fourth of the entire nation's growth since 1985.)
- Rebounding from a slight decline in the early 1980s, the East North Central States (such as Michigan and Ohio) experienced population increases in the second half of the decade.
- West Virginia, Kentucky, Mississippi, and the District of Columbia all experienced either slow growth or population declines in the mid-1980s to late 1980s.

In This Section

Figures 2, 3, and 4, and Tables H-1 through H-4 and P-1 through P-8 provide a detailed overview of the U.S. population and household demographics.

Figure 2. U.S. Census Regions and Divisions



Northeast Region

New England Division
- Maine
- New Hampshire
- Vermont
- Massachusetts
- Rhode Island
- Connecticut

Middle Atlantic Division
- New York
- New Jersey
- Pennsylvania

Midwest Region

East North Central Division
- Ohio
- Indiana
- Illinois
- Michigan
- Wisconsin

West North Central Division
- Minnesota
- Iowa
- Missouri
- North Dakota
- South Dakota
- Nebraska
- Kansas

South Region

South Atlantic Division
- Delaware
- Maryland
- District of Columbia
- Virginia
- West Virginia
- North Carolina
- South Carolina
- Georgia
- Florida

East South Central Division
- Kentucky
- Tennessee
- Alabama
- Mississippi

West South Central Division
- Arkansas
- Louisiana
- Oklahoma
- Texas

West Region

Mountain Division
- Montana
- Idaho
- Wyoming
- Colorado
- New Mexico
- Arizona
- Utah
- Nevada

Pacific Division
- Washington
- Oregon
- California
- Alaska
- Hawaii

0006893-2

Source: U.S. Department of Commerce
Bureau of the Census
Dataquest
June 1990

Table H-1. Number of U.S. Households and Average Household Size

							Estimated	
Year	1985	1986	1987	1988	1989	1990	1995	2000
Households (Millions)	86.8	88.4	89.5	91.1	92.8	94.2	100.3	105.9
CAGR (%)	1.6	1.8	1.2	1.8	1.9	1.7	1.3	1.2
Persons per Household	2.69	2.67	2.66	2.64	2.62	2.60	NA	2.48

NA = Not available

Source: U.S. Department of Commerce, Bureau of the Census

Table H-2. Income Distribution of U.S. Households, 1988

Income	Households (Thousands)	Percent
Less than $5,000	5,737	6.2
$5,000 to $9,999	10,006	10.8
$10,000 to $14,999	9,516	10.3
$15,000 to $19,999	9,126	9.8
$20,000 to $24,999	8,184	8.8
$25,000 to $29,999	7,891	8.5
$30,000 to $34,999	6,984	7.5
$35,000 to $39,999	6,414	6.9
$40,000 to $49,999	9,638	10.4
$50,000 to $74,999	12,455	13.4
$75,000 or More	6,877	7.4
Total	92,828	100.0
Median Income	$27,225	
Mean Income	$34,017	

Source: U.S. Department of Commerce, Bureau of the Census

Table H-3. Average U.S. Household Size

Type of Household	Persons per Household 1986	1987	1988	1989
All Households	2.67	2.66	2.64	2.62
Family Households[1]	3.28	3.22	3.21	3.16
Married Couple Households	3.32	3.27	3.25	3.23
Male Householder, No Wife	2.94	2.88	2.92	2.75
Female Householder, No Husband	3.11	3.09	3.08	2.95
Nonfamily Households[2]	1.21	1.22	1.22	NA
Male Householder	1.33	1.34	1.33	NA
Female Householder	1.13	1.13	1.13	NA

[1] Family households consist of people related to the householder by birth, marriage, or adoption.
[2] Nonfamily households consist of a person living alone or a householder living with people unrelated by birth, marriage, or adoption.
NA = Not available

Source: U.S. Department of Commerce, Bureau of the Census

Table H-4. U.S. Households by Region (Thousands of Households)

Region	1988 Households	Percent	1989 Households	Percent	CAGR
Northeast	19,137	21.0	19,158	20.6	0.11
Midwest	22,402	24.6	22,719	24.5	1.42
South	31,048	34.1	31,962	34.4	2.94
West	18,480	20.3	19,078	20.5	3.24
Total	91,067	100.0	92,917	100.0	2.03

Note: Columns may not add to totals shown because of rounding.

Source: U.S. Department of Commerce, Bureau of the Census

Table P-1. Population of the United States, 1987-2000 (Thousands of People)

	Actual			Estimated			
	1987	1988	1989	1991	1994	1997	2000
Population	244,425	246,048	248,241	252,502	258,338	263,543	268,266
CAGR (%)	1.39	0.66	0.89	0.85	0.76	0.67	0.59

Source: U.S. Department of Commerce, Bureau of the Census
Datapest
June 1990

Table P-2. Distribution of U.S. Population by Age (Percent)

	Actual	Estimated			
Age	1989	1991	1994	1997	2000
Less than 10 Years	14.7	14.6	14.2	13.7	13.0
10-19 Years	14.0	13.7	13.9	14.2	14.3
20-29 Years	16.4	15.7	14.4	13.5	13.2
30-44 Years	23.7	24.6	24.7	24.4	23.6
45-64 Years	18.7	18.7	19.9	21.2	22.9
65 Years and Over	12.5	12.7	12.9	13.0	13.0
	100.0	100.0	100.0	100.0	100.0

Source: U.S. Department of Commerce, Bureau of the Census

Figure 3. Actual and Estimated Distribution of U.S. Population by Age

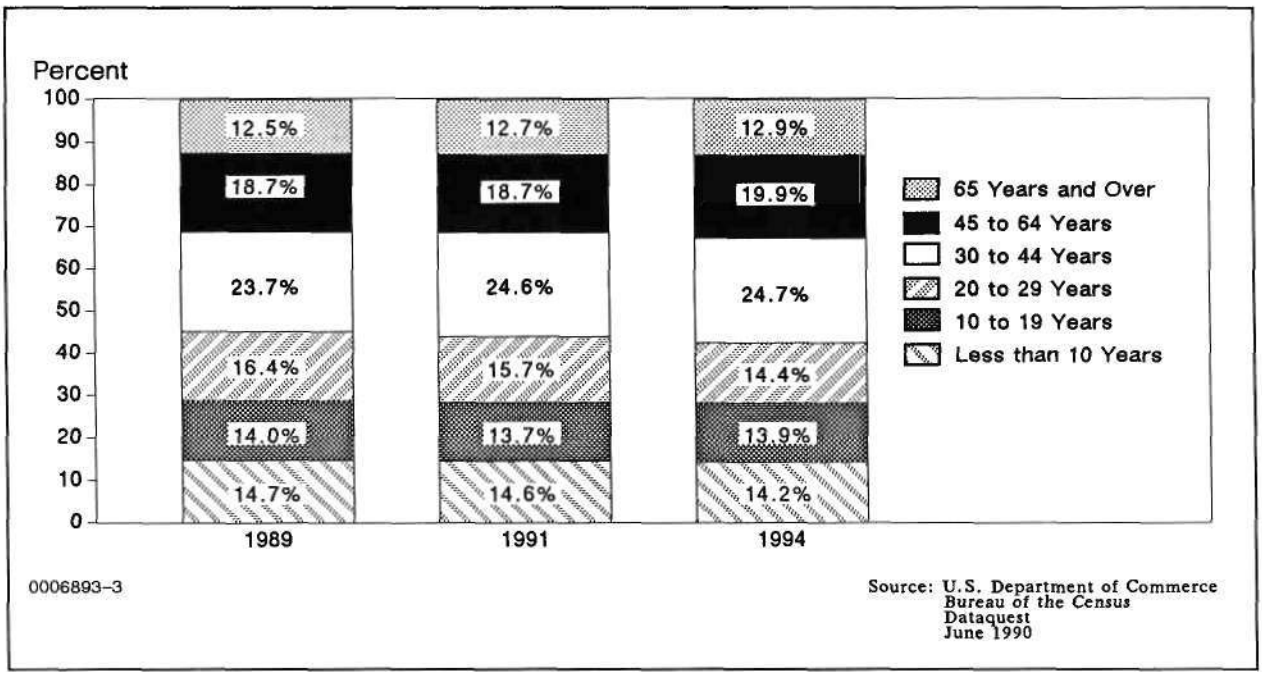


Table P-3. Top 50 Metropolitan Statistical Areas, 1988

Rank	Name	Population (Thousands)
1	New York - Northern New Jersey - Long Island, NY - NJ - CT	18,120,200
2	Los Angeles - Anaheim - Riverside, CA	13,769,700
3	Chicago - Gary - Lake County, IL - IN - WI	8,180,900
4	San Francisco - Oakland - San Jose, CA	6,041,800
5	Philadelphia - Wilmington - Trenton, PA - NJ - DE - MD	5,963,300
6	Detroit - Ann Arbor, MI	4,620,200
7	Boston - Lawrence - Salem, MA - NH	4,109,900
8	Dallas - Fort Worth, TX	3,766,100
9	Washington, DC - MD - VA	3,734,200
10	Houston - Galveston - Brazoria, TX	3,641,500
11	Miami - Fort Lauderdale, FL	3,000,500
12	Cleveland - Akron - Lorain, OH	2,769,000
13	Atlanta, GA	2,736,600
14	St. Louis, Mo - IL	2,466,700
15	Seattle - Tacoma, WA	2,420,800
16	Minneapolis - St. Paul, MN - WI	2,387,500
17	San Diego, CA	2,370,400
18	Baltimore, MD	2,342,500
19	Pittsburgh - Beaver Valley, PA	2,284,100
20	Phoenix, AZ	2,029,500
21	Tampa - St. Petersburg - Clearwater, FL	1,995,100
22	Denver - Boulder, CO	1,858,000
23	Cincinnati - Hamilton, OH - KY - IN	1,728,500
24	Kansas City, MO - KS	1,575,400
25	Milwaukee - Racine, WI	1,571,700
26	Portland - Vancouver, OR - WA	1,414,200
27	Sacramento, CA	1,385,200
28	Norfolk - Virginia Beach - Newport News, VA	1,380,200
29	Columbus, OH	1,344,300
30	San Antonio, TX	1,323,200
31	New Orleans, LA	1,306,900
32	Indianapolis, IN	1,236,600
33	Buffalo - Niagara Falls, NY	1,175,600
34	Providence - Pawtucket - Fall River, RI - MA	1,125,400
35	Charlotte - Gastonia - Rock Hill, NC	1,112,000
36	Hartford - New Britain - Middletown, CT	1,067,600
37	Salt Lake City - Ogden, UT	1,065,000
38	Rochester, NY	980,100
39	Memphis, TN - AR - MS	979,300
40	Nashville, TN	971,800
41	Orlando, FL	971,200
42	Louisville, KY	967,000
43	Oklahoma City, OK	963,800
44	Dayton - Springfield, OH	948,000
45	Greensboro - Winston-Salem - High Point, NC	924,700
46	Birmingham, AL	923,400
47	Jacksonville, FL	898,100
48	Albany - Schenectady - Troy, NY	850,800
49	Richmond - Petersburg, VA	844,300
50	Honolulu, HI	838,500

Source: U.S. Department of Commerce, Bureau of the Census

Table P-4. 100 Largest U.S. Cities, 1988

Rank	City	Population (Thousands)
1	New York, NY	7,353
2	Los Angeles, CA	3,353
3	Chicago, IL	2,978
4	Houston, TX	1,698
5	Philadelphia, PA	1,647
6	San Diego, CA	1,070
7	Detroit, MI	1,036
8	Dallas, TX	987
9	San Antonio, TX	941
10	Phoenix, AZ	924
11	Baltimore, MD	751
12	San Jose, CA	738
13	San Francisco, CA	732
14	Indianapolis, IN	727
15	Memphis, TN	645
16	Jacksonville, FL	635
17	Washington, D.C.	617
18	Milwaukee, WI	599
19	Boston, MA	578
20	Columbus, OH	570
21	New Orleans, LA	532
22	Cleveland, OH	521
23	El Paso, TX	511
24	Seattle, WA	502
25	Denver, CO	492
26	Nashville-Davidson, TN	481
27	Austin, TX	465
28	Kansas City, MO	439
29	Oklahoma City, OK	434
30	Fort Worth, TX	427
31	Atlanta, GA	420
32	Portland, OR	418
33	Long Beach, CA	415
34	St. Louis, MO	404
35	Tucson, AZ	386
36	Albuquerque, NM	378
37	Honolulu, HI	376
38	Pittsburgh, PA	375
39	Miami, FL	371
40	Cincinnati, OH	370
41	Tulsa, OK	368
42	Charlotte, NC	368
43	Virginia Beach, VA	365
44	Oakland, CA	357
45	Omaha, NE	353
46	Minneapolis, MN	345
47	Toledo, OH	341
48	Sacramento, CA	338
49	Newark, NJ	314
50	Buffalo, NY	314
51	Fresno, CA	307

(Continued)

Table P-4 (Continued). 100 Largest U.S. Cities, 1988

Rank	City	Population (Thousands)
52	Wichita, KS	295
53	Norfolk, VA	286
54	Colorado Springs, CO	283
55	Louisville, KY	282
56	Tampa, FL	282
57	Mesa, AZ	280
58	Birmingham, AL	277
59	Corpus Christi, TX	261
60	St. Paul, MN	259
61	Arlington, TX	257
62	Anaheim, CA	245
63	Santa Ana, CA	240
64	St. Petersburg, FL	235
65	Baton Rouge, LA	235
66	Rochester, NY	230
67	Lexington-Fayette, KY	226
68	Akron, OH	222
69	Aurora, CO	219
70	Anchorage, AK	218
71	Shreveport, LA	218
72	Jersey City, NJ	218
73	Richmond, VA	213
74	Riverside, CA	211
75	Las Vegas, NV	211
76	Mobile, AL	209
77	Jackson, MS	201
78	Montgomery, AL	194
79	Des Moines, IA	193
80	Stockton, CA	191
81	Lubbock, TX	188
82	Lincoln, NE	188
83	Huntington Beach, CA	187
84	Raleigh, NC	187
85	Grand Rapids, MI	185
86	Yonkers, NY	183
87	Greensboro, NC	182
88	Garland, TX	180
89	Little Rock, AR	180
90	Fort Wayne, IN	180
91	Madison, WI	178
92	Dayton, OH	178
93	Columbus, GA	178
94	Knoxville, TN	172
95	Spokane, WA	171
96	Fremont, CA	166
97	Amarillo, TX	166
98	Tacoma, WA	164
99	Chattanooga, TN	163
100	Hialeah, FL	162

Source: U.S. Department of Commerce, Bureau of the Census

Table P-5. Summary of U.S. Civilian Population By Labor Force Status, 1989

	Population (Thousands)
Civilian Noninstitutional Population Under 16 Years	57,038
Civilian Noninstitutional Population 16 Years and Over	
Civilian Labor Force	
Employed	
Nonagricultural Industries	
Wage and Salary Workers	
Private Household Workers	1,112
Government	17,637
Others	87,568
Self-Employed Workers	8,692
Unpaid Family Workers	282
Subtotal	115,291
Agricultural	
Wage and Salary Workers	1,682
Self-Employed Workers	1,417
Unpaid Family Workers	132
Subtotal	3,231
Total	118,523
Unemployed	6,594
Total	125,117
Not in Labor Force	
Keeping House	27,252
Going to School	7,454
Unable to Work	3,487
Other Reasons	24,966
Subtotal	63,158
Total	188,275
Institutionalized Population	2,928
Civilian Population	248,241

Note: Civilian population figure does not include armed forces or institutionalized population under 16 years. Noninstitutional population under 16 years as of July 1, 1988.

Source: U.S. Department of Labor, Bureau of Labor Statistics

Table P-6. U.S. Census Regions and Divisions

Northeast Region	Midwest Region	South Region	West Region
New England Division	East North Central Division	South Atlantic Division	Mountain Division
Maine	Ohio	Delaware	Montana
New Hampshire	Indiana	Maryland	Idaho
Vermont	Illinois	District of Columbia	Wyoming
Massachusetts	Michigan	Virginia	Colorado
Rhode Island	Wisconsin	West Virginia	New Mexico
Connecticut		North Carolina	Arizona
		Maryland	Utah
		Georgia	Nevada
		Florida	
Middle Atlantic Division	West North Central Division	East South Central Division	Pacific Division
New York	Minnesota	Kentucky	Washington
New Jersey	Iowa	Tennessee	Oregon
Pennsylvania	Missouri	Alabama	California
	North Dakota	Mississippi	Alaska
	South Dakota		Hawaii
	Nebraska	West South Central Division	
	Kansas	Arkansas	
		Louisiana	
		Oklahoma	
		Texas	

Source: U.S. Department of Commerce, Bureau of the Census

Figure 4. Distribution of U.S. Population by Census Divisions

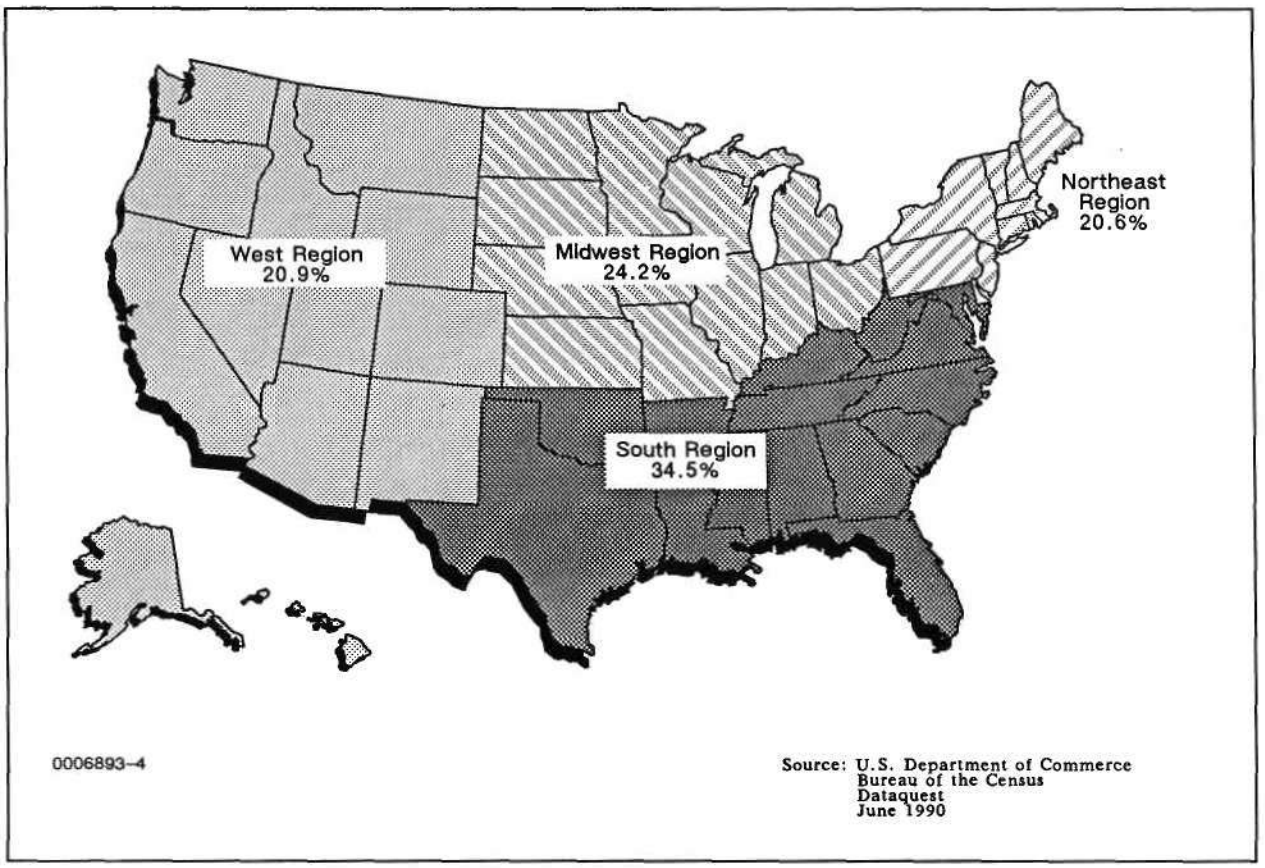


Table P-7. U.S. Population by Region and Division (Thousands)

	1989	Percent	1990	Percent
Northeast Region				
New England Division	13,047	5.3	12,733	5.1
Middle Atlantic Division	37,726	15.2	35,690	14.3
Subtotal	50,773	20.5	48,423	19.4
Midwest Region				
East North Central Division	42,298	17.0	42,372	17.0
West North Central Division	17,851	7.2	17,894	7.2
Subtotal	60,149	24.2	60,266	24.2
South Region				
South Atlantic Division	43,115	17.4	43,144	17.3
East South Central Division	15,406	6.2	16,121	6.5
West South Central Division	27,002	10.9	28,328	11.4
Subtotal	85,523	34.5	87,593	35.1
West Region				
Mountain Division	13,513	5.4	15,404	6.2
Pacific Division	38,283	15.4	37,516	15.1
Subtotal	51,796	20.9	52,920	21.2
Total	248,241	100.0	249,202	100.0

Note: Columns may not add to totals shown because of rounding.

Source: U.S. Department of Commerce, Bureau of the Census
Dataquest
June 1990

Table P-8. U.S. Population by Census Regions, Divisions, and States

Region	Population (Thousands)	Percent
Northeast Region		
New England Division		
Maine	1,222	0.5
New Hampshire	1,107	0.4
Vermont	567	0.2
Massachusetts	5,913	2.4
Rhode Island	998	0.4
Connecticut	3,239	1.3
Subtotal	13,046	5.3
Middle Atlantic Division		
New York	17,950	7.2
New Jersey	7,736	3.1
Pennsylvania	12,040	4.9
Subtotal	37,726	15.2
Midwest Region		
East North Central Division		
Ohio	10,907	4.4
Indiana	5,593	2.3
Illinois	11,658	4.7
Michigan	9,273	3.7
Wisconsin	4,867	2.0
Subtotal	42,298	17.0
West North Central Division		
Minnesota	4,353	1.8
Iowa	2,840	1.1
Missouri	5,159	2.1
North Dakota	660	0.3
South Dakota	715	0.3
Nebraska	1,611	0.6
Kansas	2,513	1.0
Subtotal	17,851	7.2

(Continued)

Table P-8 (Continued). U.S. Population by Census Regions, Divisions, and States

Region	Population (Thousands)	Percent
South Region		
South Atlantic Division		
Delaware	673	0.3
Maryland	4,694	1.9
District of Columbia	604	0.2
Virginia	6,098	2.5
West Virginia	1,857	0.7
North Carolina	6,571	2.6
South Carolina	3,512	1.4
Georgia	6,436	2.6
Florida	12,671	5.1
Subtotal	43,116	17.4
East South Central Division		
Kentucky	3,727	1.5
Tennessee	4,940	2.0
Alabama	4,118	1.7
Mississippi	2,621	1.1
Subtotal	15,406	6.2
West South Central Division		
Arkansas	2,406	1.0
Louisiana	4,382	1.8
Oklahoma	3,224	1.3
Texas	16,991	6.8
Subtotal	27,003	10.9
West Region		
Mountain Division		
Montana	806	0.3
Idaho	1,014	0.4
Wyoming	475	0.2
Colorado	3,317	1.3
New Mexico	1,528	0.6
Arizona	3,556	1.4
Utah	1,707	0.7
Nevada	1,111	0.4
Subtotal	13,514	5.4

(Continued)

Table P-8 (Continued). U.S. Population by Census Regions, Divisions, and States

Region	Population (Thousands)	Percent
West Region (Continued)		
Pacific Division		
Washington	4,761	1.9
Oregon	2,820	1.1
California	29,063	11.7
Alaska	527	0.2
Hawaii	1,112	0.4
Subtotal	38,283	15.4
Total	248,241	100.0

Note: Includes armed forces residing in each state. Columns may not add to totals shown because of rounding.

Source: U.S. Department of Commerce, Bureau of the Census
Dataquest
June 1990

Business

The business sector of the U.S. economy is faced with responding to a multitude of high-impact trends occurring simultaneously in our society. The production orientation of American business is transforming into a service-providing framework. As the structure of business is rebuilt, a new set of challenges await businesses in the nineties.

- Over the next decade, service-producing industries are projected to reach 79.0 percent of all nonfarm wage and salary jobs, compared with 75.9 percent in 1988.
- Employment within the services segment of service-producing industries will account for nearly one-half of all new jobs added over the next 10 years.
- In health and business services alone, employment is expected to reach 18 million by the year 2000. The fastest growing business service industry will be computer services. The business starts of computer-related services have been increasing at an accelerating level.
- The installation of automatic processing equipment in industries such as food production and automotive has raised productivity levels while reducing employment.
- Increased demand for printed material has augmented growth in both employment in this field and the establishment of new small firms. Printing and publishing is one of the few manufacturing sectors where growth has increased to accommodate these new opportunities.
- Strong migration to western states such as Nevada, Arizona, and California has spawned opportunities. The market for opening new businesses in response to this population movement is widening.
- The results of The Dun & Bradstreet Corporation's Dun's 5000 Survey show that 40.9 percent of the companies surveyed expect to increase capital spending in 1990 over their 1989 level. This is a positive economic development in light of rising interest rates.
- Capital equipment expenditures, within the information industry sector, are less dependent on interest rates because of the pace of technological change. The average life-cycle of a computer is shorter than that of a turbine, tractor, or desk.
- There is a strong correlation between the size of the company and plans to increase capital spending. Over half of the companies with greater than 10,000 employees plan to increase capital equipment expenditures. Only 31.7 percent of the companies with less than 20 employees plan to spend more.
- The implementation of technologically advanced equipment in the workplace will foster a continued need for businesses to train and retrain existing employees.

In This Section

Tables B-1 through B-5 and Figures 5 through 7 provide a detailed overview of the overall composition of U.S. business.

Table B-1. Distribution of U.S. Establishments by Detailed Industry Sector and Employment-Size Class, 1990

Industry Sector	Number of Establishments by Employment-Size Class								Percent of Total
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total	
Agriculture, Forestry, Fisheries									
Agricultural Production	206,669	7,775	4,473	1,154	743	52	19	220,885	2.5
Agricultural Services	85,386	6,648	2,965	704	360	19	5	96,087	1.1
Forestry	3,213	274	159	47	48	10	1	3,752	0
Fishing, Hunting, and Trapping	2,315	174	103	29	6	0	0	2,627	0
Subtotal	297,583	14,871	7,700	1,934	1,157	81	25	323,351	3.7
Percent	92.0	4.6	2.4	0.6	0.4	0	0	100.0	
Mining									
Oil and Gas Extraction	29,653	4,176	2,852	876	587	58	45	38,247	0.4
Other Mining	8,180	1997	1756	579	675	91	47	13,325	0.2
Subtotal	37,833	6,173	4,608	1,455	1,262	149	92	51,572	0.6
Percent	73.4	12.0	8.9	2.8	2.4	0.3	0.2	100.0	
Contract Construction									
General Contractors and Builders	271,208	20,894	11,356	2,900	1,458	58	27	307,901	3.5
Heavy Construction Contractors	30,870	6,306	5,114	1,946	1,197	60	39	45,532	0.5
Special Trade Contractors	432,107	42,268	24,537	6,060	2,563	54	16	507,605	5.8
Subtotal	734,185	69,468	41,007	10,906	5,218	172	82	861,038	9.9
Percent	85.3	8.1	4.8	1.3	0.6	0	0	100.0	
Manufacturing									
Food and Kindred Products	15,565	4,852	5,142	2,888	3,704	488	238	32,877	0.4
Tobacco Manufactures	97	29	28	32	63	10	16	275	0
Textile Mill Products	5,805	1,612	1,894	1,127	1,743	309	112	12,602	0.1
Apparel and Other Textile Products	16,668	4,061	4,438	2,613	3,028	261	52	31,121	0.4
Lumber and Wood Products	30,805	5,713	4,693	1,946	1,527	84	30	44,798	0.5

(Continued)

Table B-1 (Continued). Distribution of U.S. Establishments by Detailed Industry Sector and Employment-Size Class, 1990

Industry Sector	Number of Establishments by Employment-Size Class								
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total	Percent of Total
Manufacturing (Continued)									
Furniture and Fixtures	11,041	2,599	2,353	1,179	1,239	129	41	18,581	0.2
Paper and Allied Products	2,708	1,326	1,958	1,327	1,891	169	112	9,491	0.1
Printing and Publishing	76,496	12,146	8,673	3,463	2,791	260	167	103,996	1.2
Chemicals and Allied Products	10,881	3,780	3,810	1,916	2,086	335	258	23,066	0.3
Petroleum and Coal Products	2,167	621	611	265	343	60	58	4,125	0
Rubber and Miscellaneous Plastics Products	7,861	2,812	3,555	2,238	2,283	160	74	18,983	0.2
Leather and Leather Products	2,336	455	469	278	377	39	12	3,966	0
Stone, Clay, and Glass Products	14,065	3,781	3,411	1,353	1,262	145	54	24,071	0.3
Primary Metal Industries	4,497	1,834	2,158	1,226	1,586	215	137	11,653	0.1
Fabricated Metal Products	24,325	8,292	8,718	4,086	3,361	219	141	49,142	0.6
Machinery, except Electrical	52,140	13,206	10,872	4,311	3,829	466	319	85,143	1.0
Electric and Electronic Equipment	14,118	4,269	4,754	2,647	3,677	612	430	30,507	0.3
Transportation Equipment	10,623	2,461	2,414	1,321	1,976	349	439	19,583	0.2
Instruments and Related Products	10,972	2,943	2,794	1,418	1,683	255	209	20,274	0.2
Miscellaneous Manufacturing Industries	27,242	4,079	3,187	1,276	966	80	29	36,859	0.4
Subtotal	340,412	80,871	75,932	36,910	39,415	4,645	2,928	581,113	6.7
Percent	58.6	13.9	13.1	6.4	6.8	0.8	0.5	100.0	
Transportation, Communications, Utilities									
Railroad Transportation	1,653	409	415	208	364	73	69	3,191	
Local and Interurban Passenger Transportation	13,677	3,902	3,991	1,530	905	72	36	24,113	0.3
Trucking and Warehousing	111,081	17,206	13,570	4,542	2,737	199	89	149,424	1.7
Water Transportation	8,778	1,177	940	300	265	20	12	11,492	0.1
Transportation by Air	10,293	1,864	1,803	808	642	78	88	15,576	0.2
Pipe Lines, except Natural Gas	497	182	163	58	41	3	0	944	0
Transportation Services	39,418	5,854	2,794	741	495	42	20	49,364	0.6

(Continued)

Table B-1 (Continued). Distribution of U.S. Establishments by Detailed Industry Sector and Employment-Size Class, 1990

Industry Sector	Number of Establishments by Employment-Size Class								Percent of Total
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total	
Transportation, Communications, Utilities (Continued)									
Communication									
Telephone	5,644	2,139	1,837	880	951	168	209	11,828	0.1
Telegraph	857	134	57	19	31	1	4	1,103	0
Broadcasting	4,347	3,608	3,049	835	521	16	15	12,391	0.1
Others	6,416	1,416	1,229	425	475	39	18	10,018	0.1
Electric, Gas, and Sanitary Services	19,632	4,557	4,386	2,189	1,799	259	175	32,997	0.4
Subtotal	222,293	42,448	34,234	12,535	9,226	970	735	322,441	3.7
Percent	68.9	13.2	10.6	3.9	2.9	0.3	0.2	100.0	
Wholesale Trade									
Durable Goods	333,253	56,051	31,782	7,364	3,438	169	110	432,167	5.0
Nondurable Goods	188,211	29,225	18,292	5,480	3,282	209	75	244,774	2.8
Subtotal	521,464	85,276	50,074	12,844	6,720	378	185	676,941	7.8
Percent	77.0	12.6	7.4	1.9	1.0	0.1	0	100.0	
Retail Trade									
Building Materials and Garden Supplies	99,721	11,764	5,653	1,440	526	11	4	119,119	1.4
General Merchandise Stores									
Department Stores	3,453	1,644	2,769	3,458	7,784	285	90	19,483	0.2
Others	29,702	3,505	1,813	873	592	41	9	36,535	0.4
Food Stores									
Grocery Stores	136,435	17,557	15,628	9,472	5,823	86	42	185,043	2.1
Others	57,540	6,348	2,603	377	126	9	0	67,003	0.8
Automotive Dealers and Service Stations									
New and Used Car Dealers	13,516	8,129	13,818	6,547	1,711	0	3	43,724	0.5

(Continued)

Table B-1 (Continued). Distribution of U.S. Establishments by Detailed Industry Sector and Employment-Size Class, 1990

Industry Sector	Number of Establishments by Employment-Size Class								
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total	Percent of Total
Retail Trade (Continued)									
Used Car Dealers	31,583	858	204	25	5	0	0	32,675	0.4
Auto and Home Supply	52,347	5,677	1,445	137	68	3	3	59,680	0.7
Gasoline Service Stations	96,454	7,443	1,505	409	207	1	1	106,020	1.2
Others	22,572	2,287	720	103	24	0	0	25,706	0.3
Apparel and Accessory Stores	172,455	15,417	4,406	879	545	42	24	193,768	2.2
Furniture and Home Furnishings Stores									
Household Appliances Stores	20,657	1,484	690	96	38	0	1	22,966	0.3
Radio, TV, and Music Stores	29,380	1,570	522	125	71	7	0	31,675	0.4
Others	124,489	11,150	3,891	582	264	13	6	140,395	1.6
Eating and Drinking Places	260,440	76,014	74,413	22,087	3,798	109	46	436,907	5.0
Miscellaneous Retail									
Drug Stores	36,831	11,931	5,743	652	189	13	8	55,367	0.6
Liquor Stores	38,043	2,040	411	39	7	1	1	40,542	0.5
Used Merchandise Stores	46,388	720	409	77	32	0	1	47,627	0.5
Miscellaneous Shopping Goods	310,257	14,202	4,400	1,006	351	24	17	330,257	3.8
Nonstore Retailers	64,950	3,812	2,170	731	474	41	34	72,212	0.8
Others	180,890	5,172	2,009	365	137	11	2	188,586	2.2
Subtotal	1,828,103	208,724	145,222	49,480	22,772	697	292	2,255,290	25.9
Percent	81.1	9.3	6.4	2.2	1.0	0	0	100.0	
Finance, Insurance, Real Estate									
Banking	45,860	27,441	16,259	4,626	2,831	316	326	97,659	1.1
Credit Agencies, Except Banks	29,997	4,379	2,706	825	655	73	36	38,671	0.4
Securities, Commodities Brokers, and Services	23,305	4,075	3,485	1,229	814	80	90	33,078	0.4
Insurance Carriers	12,423	4,555	5,142	2,280	2,537	411	406	27,754	0.3
Insurance Agents, Brokers and Services	120,529	9,292	5,658	1,668	991	95	35	138,268	1.6

(Continued)

Table B-1 (Continued). Distribution of U.S. Establishments by Detailed Industry Sector and Employment-Size Class, 1990

Industry Sector	Number of Establishments by Employment-Size Class								
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total	Percent of Total
Finance, Insurance, Real Estate (Continued)									
Real Estate	313,425	27,955	16,421	3,814	1,771	72	29	363,487	4.2
Holding and Other Investment Offices	28,915	2,197	1,359	531	381	60	36	33,479	0.4
Subtotal	574,454	79,894	51,030	14,973	9,980	1,107	958	732,396	8.4
Percent	78.4	10.9	7.0	2.0	1.4	0.2	0.1	100.0	
Services									
Hotels and Other Lodging Places	55,361	7,981	7,430	3,729	3,802	306	136	78,745	0.9
Personal Services									
Laundry, Cleaning, Garment Services	70,370	4,942	2,337	824	476	6	2	78,957	0.9
Photographic Studios	18,947	472	139	38	28	5	1	19,630	0.2
Beauty and Barber Shops	152,746	6,405	1,220	102	16	0	0	160,489	1.8
Shoe Repair, Hat Cleaning	8,280	40	6	1	0	0	0	8,327	0.1
Funeral Services	19,532	1,245	315	38	16	0	0	21,146	0.2
Miscellaneous Personal Services	34,981	1,175	542	154	107	9	4	36,972	0.4
Business Services									
Advertising	26,517	3,210	1,634	498	307	30	15	32,211	0.4
Credit Collection and Reporting	5,414	1,361	994	266	130	6	6	8,177	0.1
Mailing, Reproduction, Stenography	15,728	1,682	1,155	363	268	9	1	19,206	0.2
Services to Buildings	40,825	6,710	4,303	1,513	1,529	143	82	55,105	0.6
News Syndicates	586	122	114	35	30	5	0	892	0
Personnel Supply Services	17,721	3,148	1,651	679	939	110	73	24,321	0.3
Computer and Data Processing Services	41,041	6,224	4,405	1,678	1,471	153	114	55,086	0.6
Miscellaneous Business Services	195,790	14,234	8,529	2,873	2,461	210	82	224,179	2.6
Auto Repair, Services, Garages									
Auto Rental, without Drivers	18,372	2,267	1,396	419	227	9	7	22,697	0.3
Auto Parking	2,258	378	319	103	74	4	1	3,137	0

(Continued)

Table B-1 (Continued). Distribution of U.S. Establishments by Detailed Industry Sector and Employment-Size Class, 1990

Industry Sector	Number of Establishments by Employment-Size Class								Percent of Total
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total	
Services (Continued)									
Auto Repair Shops	193,843	8,757	2,181	218	85	6	3	205,093	2.4
Auto Services, except Repair	23,053	1,926	1,055	104	28	2	2	26,170	0.3
Miscellaneous Repair Services	170,398	5,903	2,670	602	311	13	8	179,905	2.1
Motion Pictures	34,961	3,145	1,387	334	219	16	9	40,071	0.5
Amusement and Recreation Services	71,427	10,648	8,263	2,663	1,231	57	63	94,352	1.1
Health Services									
Offices of Physicians	169,628	15,109	6,702	1,329	685	51	41	193,545	2.2
Offices of Dentists	89,783	5,023	943	93	16	0	0	95,858	1.1
Offices of Osteopathic Physicians	5,849	309	87	5	1	1	0	6,252	0.1
Offices of Other Health Practitioners	50,951	1,585	468	107	76	2	0	53,189	0.6
Nursing and Personal Care Facilities	2,649	1,283	3,870	6,416	5,817	97	40	20,172	0.2
Hospitals	1,075	613	1,087	1,555	4,384	1,588	1,899	12,201	0.1
Medical and Dental Laboratories	14,340	1,694	1,024	321	230	17	13	17,639	0.2
Outpatient Care Facilities	3,801	1,728	1,645	627	322	13	18	8,154	0.1
Other Health and Allied Services	4,457	1,831	1,838	844	807	52	17	9,846	0.1
Legal Services	112,716	10,193	6,039	1,722	1,038	91	10	131,809	1.5
Educational Services									
Elementary and Secondary Schools	14,700	12,431	38,378	23,086	9,175	592	296	98,658	1.1
Colleges and Universities	570	346	563	360	1,034	249	335	3,457	0
Libraries and Information Centers	16,467	1,104	914	310	162	18	6	18,981	0.2
Correspondence and Vocational Schools	3,049	791	849	388	238	15	7	5,337	0.1
Other Schools and Educational Services	10,741	1,885	1,757	793	1,030	167	72	16,445	0.2
Social Services	89,954	16,785	10,750	3,333	2,133	115	41	123,111	1.4
Museums, Botanical, Zoological Gardens	3,998	573	550	200	145	9	4	5,479	0.1

(Continued)

Table B-1 (Continued). Distribution of U.S. Establishments by Detailed Industry Sector and Employment-Size Class, 1990

Industry Sector	Number of Establishments by Employment-Size Class								
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total	Percent of Total
Services (Continued)									
Membership Organizations	186,483	16,667	11,025	3,420	1,720	130	52	219,497	2.5
Miscellaneous Services	212,405	26,299	16,960	5,466	4,375	470	395	266,370	3.1
Subtotal	2,211,767	208,224	157,494	67,609	47,143	4,776	3,855	2,700,868	31.0
Percent	81.9	7.7	5.8	2.5	1.7	0.2	0.1	100.0	
Total	6,768,094	795,949	567,301	208,646	142,893	12,975	9,152	8,505,010	97.6
Percent	79.6	9.4	6.7	2.5	1.7	0.2	0.1	100.0	
Other Government									
Federal								42,047	0.5
Military								13,462	0.2
State								52,656	0.6
Local								99,893	1.1
Subtotal								208,058	2.4
Percent								100.0	
Total								8,713,068	100.0
Percent								100.0	

Note: Columns may not add to totals shown due to rounding.

Source: Dun's Marketing Services
Dataquest
June 1990

Figure 5. Percent Distribution of Business Establishments by Industry Sector

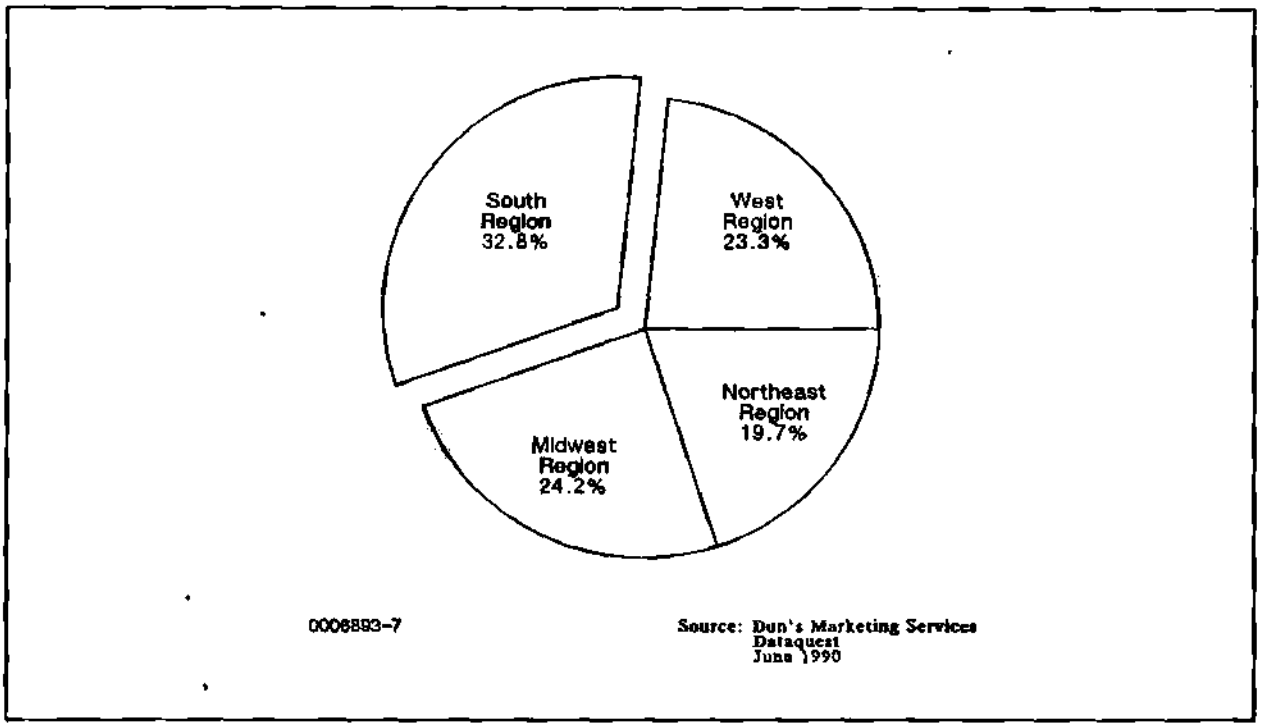


Table B-2. Distribution of U.S. Establishments by State and Employment-Size Class

Census Regions and Divisions	Number of Establishments by Employment-Size Class							
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total
Northeast Region								
New England Division								
Maine	34,147	4,115	2,835	1,016	637	64	43	42,857
New Hampshire	31,334	4,130	2,981	1,031	740	79	36	40,331
Vermont	20,046	2,335	1,619	543	299	16	12	24,870
Massachusetts	147,121	21,047	15,540	5,834	4,569	482	354	194,947
Rhode Island	24,794	3,514	2,431	920	616	79	42	32,396
Connecticut	111,443	13,918	9,887	3,336	2,376	233	175	141,368
Subtotal	368,885	49,059	35,293	12,680	9,237	953	662	476,769
Middle Atlantic Division								
New York	460,645	57,846	40,904	14,966	10,801	1,086	855	587,103
New Jersey	192,813	27,712	20,645	7,480	5,795	543	417	255,405
Pennsylvania	278,179	35,217	25,121	10,075	7,414	796	469	357,271
Subtotal	931,637	120,775	86,670	32,521	24,010	2,425	1,741	1,199,779
Midwest Region								
East North Central Division								
Ohio	238,075	31,741	24,151	9,245	6,662	603	451	310,927
Indiana	120,415	15,789	11,526	4,431	3,278	287	197	155,923
Illinois	335,450	38,554	29,319	11,037	8,050	770	507	423,687
Michigan	208,395	27,432	19,871	7,220	4,882	373	342	268,515
Wisconsin	125,275	15,196	11,153	4,198	3,026	272	191	159,311
Subtotal	1,027,610	128,712	96,020	36,131	25,898	2,305	1,688	1,318,363

(Continued)

Table B-2 (Continued). Distribution of U.S. Establishments by State and Employment-Size Class

Census Regions and Divisions	Number of Establishments by Employment-Size Class							
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total
West North Central Division								
Minnesota	139,330	14,598	10,223	4,180	2,955	253	175	171,714
Iowa	141,791	9,503	6,878	2,463	1,589	140	101	162,465
Missouri	130,109	15,178	11,181	4,078	2,917	284	192	163,939
North Dakota	25,450	2,363	1,472	527	289	20	13	30,134
South Dakota	30,675	2,527	1,739	630	368	18	17	35,974
Nebraska	57,557	5,429	3,927	1,388	873	91	45	69,310
Kansas	87,412	8,536	5,761	2,054	1,322	110	76	105,271
Subtotal	612,324	58,134	41,181	15,320	10,313	916	619	738,807
South Region								
South Atlantic Division								
Delaware	15,310	2,161	1,520	568	431	58	44	20,092
Maryland	100,460	15,460	10,773	3,996	2,728	243	177	133,837
District of Columbia	20,578	3,331	2,541	962	717	108	125	28,362
Virginia	147,099	18,422	12,724	4,832	3,486	361	277	187,201
West Virginia	39,585	4,444	3,362	1,104	732	81	53	49,361
North Carolina	153,380	18,936	13,583	5,318	4,007	411	255	195,890
South Carolina	74,752	8,982	6,272	2,522	1,936	232	132	94,828
Georgia	143,907	19,688	13,461	5,438	3,800	383	247	186,924
Florida	308,145	39,942	26,388	10,067	6,581	530	354	392,007
Subtotal	1,003,216	131,366	90,624	34,807	24,418	2,407	1,664	1,288,502
East South Central Division								
Kentucky	84,731	9,245	6,955	2,692	1,702	174	104	105,603
Tennessee	108,148	14,103	9,859	3,681	2,738	298	179	139,006
Alabama	81,663	10,225	7,559	2,915	2,148	254	128	104,892
Mississippi	60,539	6,396	4,445	1,827	1,287	162	61	74,717
Subtotal	335,081	39,969	28,818	11,115	7,875	888	472	424,218

(Continued)

Table B-2 (Continued). Distribution of U.S. Establishments by State and Employment-Size Class

Census Regions and Divisions	Number of Establishments by Employment-Size Class							
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total
West South Central Division								
Arkansas	65,053	6,094	4,227	1,625	1,189	125	74	78,387
Louisiana	94,255	11,336	8,370	3,023	1,890	178	116	119,168
Oklahoma	97,605	9,446	6,585	2,368	1,408	114	78	117,604
Texas	652,001	53,912	36,213	13,395	9,214	796	648	766,179
Subtotal	908,914	80,788	55,395	20,411	13,701	1,213	916	1,081,338
West Region								
Mountain Division								
Montana	36,726	3,098	2,103	585	319	25	11	42,867
Idaho	37,383	3,427	2,261	723	386	52	31	44,263
Wyoming	22,284	1,865	1,348	443	250	12	8	26,210
Colorado	127,495	12,601	9,018	3,119	1,941	160	138	154,472
New Mexico	43,628	4,712	3,241	1,078	660	59	29	53,407
Arizona	115,191	12,474	8,473	2,986	1,935	166	108	141,333
Utah	42,021	4,890	3,322	1,296	858	69	63	52,519
Nevada	29,232	3,624	2,460	834	602	65	86	36,903
Subtotal	453,960	46,691	32,226	11,064	6,951	608	474	551,974
Pacific Division								
Washington	144,554	15,348	10,572	3,765	2,202	172	143	176,756
Oregon	98,859	9,954	7,092	2,328	1,439	140	71	119,883
California	877,279	94,360	66,445	24,198	15,722	1,309	1,063	1,080,376
Alaska	15,674	1,566	998	323	253	21	13	18,848
Hawaii	22,419	3,225	2,272	813	583	52	33	29,397
Subtotal	1,158,785	124,453	87,379	31,427	20,199	1,694	1,323	1,425,260
Total	6,800,419	779,946	553,605	205,475	142,601	13,408	9,557	8,505,010

Note: Columns may not add to totals shown because of rounding.

Source: Dun's Marketing Services
Dataquest
June 1990

Figure 6. Distribution of Business Establishments by Census Divisions

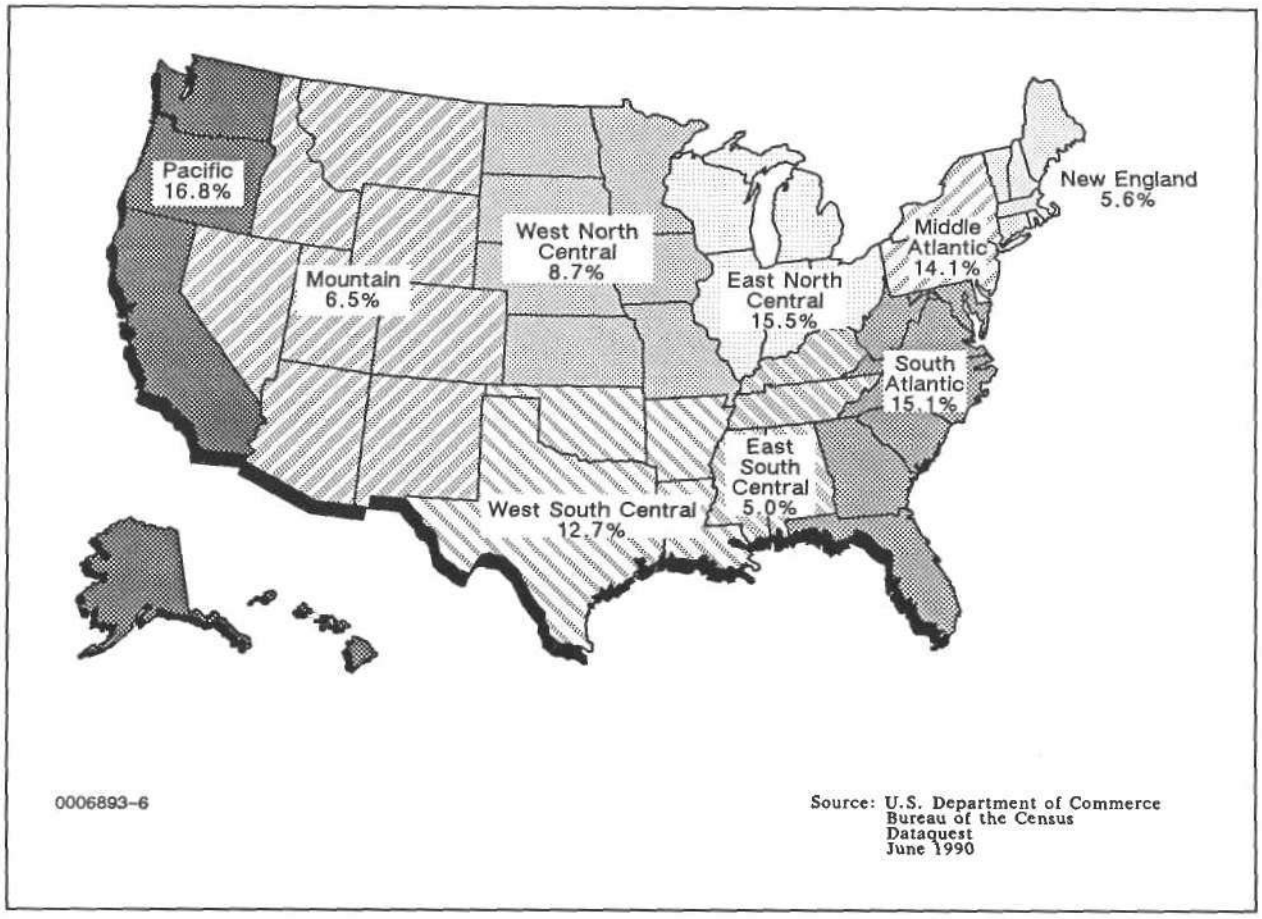


Table B-3. Establishment Data by Census Region, 1990

Census Regions and Divisions	Total	Percent of Total
Northeast Region		
New England Division	476,769	5.6
Middle Atlantic Division	1,199,779	14.1
Midwest Region		
East North Central Division	1,318,363	15.5
West North Central Division	738,807	8.7
South Region		
South Atlantic Division	1,288,502	15.1
East South Central Division	424,218	5.0
West South Central Division	1,081,338	12.7
West Region		
Mountain Division	551,974	6.5
Pacific Division	1,425,260	16.8
Total	8,505,010	100.0

Source: Dun's Marketing Services
Dataquest
June 1990

Figure 7. Distribution of Establishments by Census Region

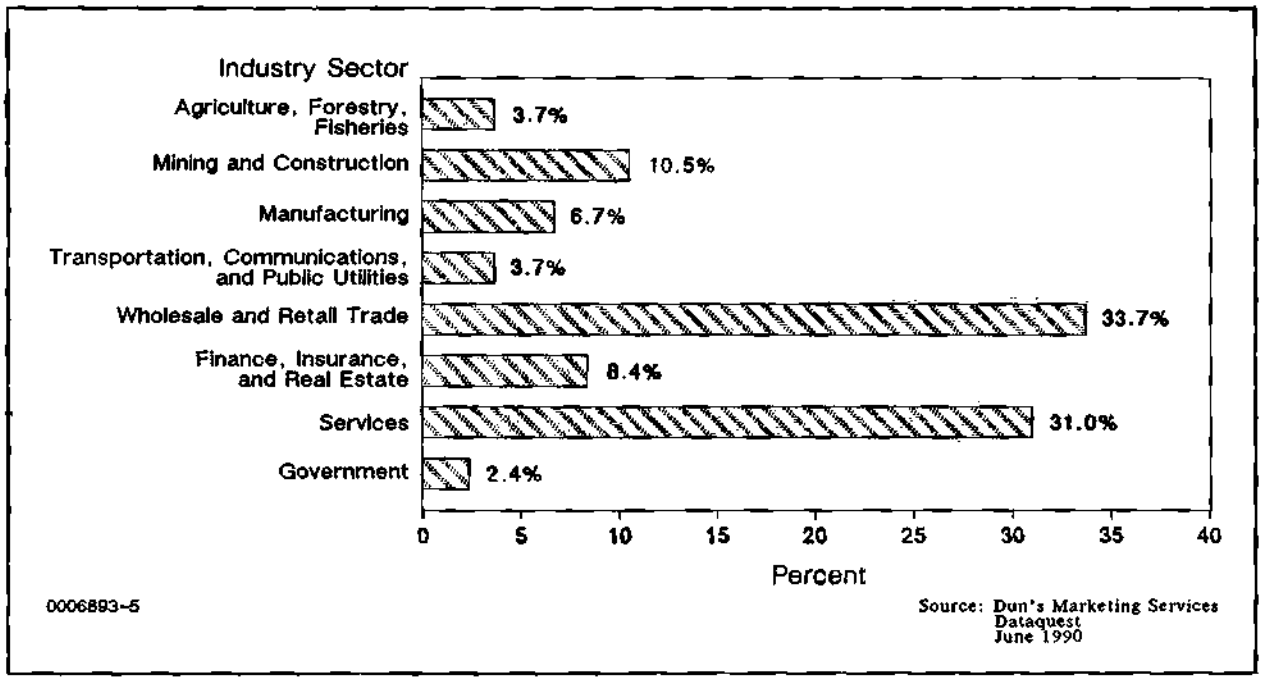


Table B-4. Distribution of Establishments by Sales Volume and Industry Sector

Industry	Number of Establishments by Sales Volume							
	0-99.9m	100-499.9m	500-999.9m	1-4.9mm	5-9.9mm	10-49.9mm	50mm+	Total
Agriculture, Forestry, and Fisheries	90,637	196,803	17,744	13,071	1,382	1,036	184	320,857
Percent of Subtotal	28.2	61.3	5.5	4.1	0.4	0.3	0.1	100.0
Mining	8,099	24,356	7,252	8,039	1,268	1,439	721	51,175
Percent of Subtotal	15.8	47.6	14.2	15.7	2.5	2.8	1.4	100.0
Construction	224,862	416,314	88,551	100,809	13,219	9,247	1,382	854,385
Percent of Subtotal	26.3	48.7	10.4	11.8	1.5	1.1	0.2	100.0
Manufacturing	94,813	225,669	73,437	119,700	26,078	27,327	9,598	576,622
Percent of Subtotal	16.4	39.1	12.7	20.8	4.5	4.7	1.7	100.0
Transportation, Public Utilities, and Communication	67,962	129,025	47,825	55,656	8,818	7,679	2,982	319,947
Percent of Subtotal	21.2	40.3	14.9	17.4	2.8	2.4	0.9	100.0
Wholesale Trade	49,593	280,769	111,150	165,290	32,468	27,291	5,151	671,712
Percent of Subtotal	7.4	41.8	16.5	24.6	4.8	4.1	0.8	100.0
Retail Trade	519,621	1,272,072	221,955	176,104	21,962	22,532	3,620	2,237,865
Percent of Subtotal	23.2	56.8	9.9	7.9	1.0	1.0	0.2	100.0
Banking	4,780	15,596	11,157	36,922	11,435	12,095	4,920	96,904
Percent of Subtotal	4.9	16.1	11.5	38.1	11.8	12.5	5.1	100.0
Finance, Insurance, and Real Estate	139,113	330,992	68,650	63,482	10,711	12,126	4,760	629,833
Percent of Subtotal	22.1	52.6	10.9	10.1	1.7	1.9	0.8	100.0
Services	1,083,624	1,240,714	186,449	187,216	22,137	19,822	5,749	2,745,711
Percent of Subtotal	39.5	45.2	6.8	6.8	0.8	0.7	0.2	100.0
Total	2,283,103	4,132,309	834,170	926,289	149,478	140,593	39,067	8,505,010
Percent of Total	26.8	48.6	9.8	10.9	1.8	1.7	0.5	100.0

Note: Columns may not add to totals shown because of rounding.
m = Thousands
mm = Millions

Source: Dun's Marketing Services
Dataquest
June 1990

Table B-5. Primary Mainframe Installation Sites of IBM/PCM* by Vertical Market

Vertical Market	Total	IBM	Amdahl	Others
Natural Resources/Construction	223	207	14	2
Process Manufacturing	1,073	1,034	15	24
Discrete Manufacturing	1,467	1,404	26	37
Transportation	203	185	9	9
Communications	119	111	7	1
Utilities	223	212	9	2
Wholesale Trade	572	546	11	15
Retail Trade	444	419	7	18
Finance	821	788	21	12
Insurance	727	694	16	17
Real Estate	68	63	1	4
Health Care	407	397	7	3
Hotels and Lodging	18	17	0	1
Business Services	1,339	1,219	68	52
Other Services	484	459	12	13
Education	707	677	11	19
Government	783	677	67	39
Others	61	59	1	1
Total	9,739	9,168	302	269

*Plug-compatible mainframe

Source: Dataquest
June 1990

Work Force

Labor force opportunities in the 1990s will be challenged by industry employment trends, technological change, worker displacement, and education and training needs for workers. Technology and changes in business practices are two factors, in particular, that will play a key role in the ability to achieve and maintain job stability in this new decade.

- Three of the nine major occupational groups are expected to grow more rapidly than the average for total employment over the next 10 years—executive, administrative, and managerial; professional specialty; and technicians and related support. In addition to being the fastest growing groups, these fields also require the highest level of educational attainment to fulfill job requirements.
- An exception to the growth pattern of the top three occupational categories lies in the service workers. Although this category is projected to grow faster than average, it has relatively few workers with college degrees and a rather high incidence of workers with less than a high-school education.
- Occupations within the professional specialty category growing most in this growth segment are:
  - Engineers
  - Computer specialists
  - Lawyers
  - Health-diagnosing and treatment occupations
  - Teachers (except college and university)
- Technological changes and advancements have been key in furthering the demand for several occupations, including engineers and computer specialists.
- The service occupations group will add more than 4 million jobs by the year 2000, an increase of 23 percent. This category will add more new jobs than any other major occupational group.
- Technological innovation and use of office automation will encourage a slowing trend in the growth in the administrative support occupations. However, this technological movement will affect certain occupations positively, such as computer operators.
- Very low employment growth is expected in agriculture, forestry, and fishing. An increase of less than 100,000 jobs is projected through the year 2000.
- A negative result of declining industries is worker displacement. Some of these workers may be reemployed in their same occupation in a growing industry or retrained for a similar position in the declining industry. However, those workers displaced because of technological change, regardless of whether they are in growing or declining industries, will have a more difficult time finding reemployment.

In This Section

Tables W-1 through W-7 and Figures 8 through 11 highlight the work force by job classification, white-collar segmentation, and employment growth by industry.

Table W-1. Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1988 Number of Workers	1988 Percent of Total	1989 Number of Workers	1989 Percent of Total	1988-1989 Percent Change
Managerial and Professional Specialty	29,190	25.39	30,398	25.91	4.1
Executive, Administrative, and Managerial	14,216	12.37	14,848	12.65	4.4
Officials and Administrators, Public Administration	472	0.41	519	0.44	10.0
Financial Managers	502	0.44	472	0.40	(6.0)
Personnel and Labor Relations Managers	130	0.11	128	0.11	(1.5)
Purchasing Managers	99	0.09	110	0.09	11.1
Managers, Marketing, Advertising, and PR	482	0.42	514	0.44	6.6
Administrators, Education and Related Fields	562	0.49	585	0.50	4.1
Managers, Medicine and Health	163	0.14	188	0.16	15.3
Managers, Properties and Real Estate	433	0.38	451	0.38	4.2
Management-Related Occupations	3,772	3.28	3,908	3.33	3.6
Accountants and Auditors	1,329	1.16	1,416	1.21	6.5
Underwriters and Other Financial Officers	741	0.64	103	0.09	(86.1)
Management Analysts	199	0.17	183	0.16	(8.0)
Personnel, Training, Labor Relations	390	0.34	426	0.36	9.2
Buyers, Wholesale and Retail Except Farm Production	233	0.20	214	0.18	(8.2)
Construction Inspectors	60	0.05	61	0.05	1.7
Inspectors and Compliance Officers, Except Construction	194	0.17	196	0.17	1.0
Others (Includes Other Financial Officers)	626	0.54	1309	1.12	109.1
Executive, Administrative, and Managerial NEC	7601	6.61	7973	6.79	4.9
Professional Specialty	14,974	13.02	15,550	13.25	3.8
Architects	143	0.12	157	0.13	9.8
Engineers	1,805	1.57	1,823	1.55	1.0
Aerospace	115	0.10	112	0.10	(2.6)
Chemical	65	0.06	67	0.06	3.1
Civil	218	0.19	249	0.21	14.2
Electrical and Electronic	573	0.50	571	0.49	(0.3)

(Continued)

Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1988 Number of Workers	1988 Percent of Total	1989 Number of Workers	1989 Percent of Total	1988-1989 Percent Change
Industrial	221	0.19	199	0.17	(10.0)
Mechanical	297	0.26	310	0.26	4.4
Engineers NEC	316	0.27	315	0.27	(0.3)
Mathematical and Computer Scientists	732	0.64	853	0.73	16.5
Computer Systems Analysts and Scientists	479	0.42	566	0.48	18.2
Operations and Systems Researchers and Analyst	210	0.18	239	0.20	13.8
Mathematical and Computer Scientists NEC	43	0.04	48	0.04	11.6
Natural Scientists	395	0.34	413	0.35	4.6
Chemists, except Biochemists	125	0.11	122	0.10	(2.4)
Biological and Life Scientists	75	0.07	77	0.07	2.7
Natural Scientists NEC	195	0.17	214	0.18	9.7
Health Diagnosing Occupations	818	0.71	854	0.73	4.4
Physicians	541	0.47	548	0.47	1.3
Dentists	152	0.13	170	0.14	11.8
Health Diagnosing Occupations NEC	125	0.11	136	0.12	8.8
Health Assessment and Treating Occupations	2,154	1.87	2,242	1.91	4.1
Registered nurses	1,559	1.36	1,599	1.36	2.6
Pharmacists	168	0.15	174	0.15	3.6
Dietitians	74	0.06	83	0.07	12.2
Therapists	298	0.26	324	0.28	8.7
Inhalation	65	0.06	63	0.05	(3.1)
Physical	82	0.07	90	0.08	9.8
Speech	66	0.06	63	0.05	(4.5)
Others	85	0.07	108	0.09	27.1
Health Assessment and Treating Occupations NEC	140	0.12	62	0.05	(55.7)
Teachers, College and University	700	0.61	709	0.60	1.3
Teachers, except College and University	3,773	3.28	3,936	3.35	4.3
Prekindergarten and Kindergarten	393	0.34	431	0.37	9.7

(Continued)

Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1988 Number of Workers	1988 Percent of Total	1989 Number of Workers	1989 Percent of Total	1988-1989 Percent Change
Elementary School	1,424	1.24	1,489	1.27	4.6
Secondary School	1,187	1.03	1,220	1.04	2.8
Special Education	246	0.21	257	0.22	4.5
Teachers, NEC	524	0.46	539	0.46	2.9
Counselors, Educational and Vocational	206	0.18	214	0.18	3.9
Librarians, Archivists and Curators	219	0.19	212	0.18	(3.2)
Librarians	196	0.17	188	0.16	(4.1)
Librarians, Archivists and Curators NEC	23	0.02	24	0.02	4.3
Social Scientists and Urban Planners	343	0.30	374	0.32	9.0
Economists	116	0.10	122	0.10	5.2
Psychologists	196	0.17	210	0.18	7.1
Social Scientists and Urban Planners NEC	31	0.03	42	0.04	35.5
Social, Recreation, and Religious Workers	1,052	0.92	1,043	0.89	(0.9)
Social Workers	537	0.47	527	0.45	(1.9)
Recreation Workers	92	0.08	101	0.09	9.8
Clergy	348	0.30	336	0.29	(3.4)
Religious Workers NEC	75	0.07	79	0.07	5.3
Lawyers and Judges	757	0.66	774	0.66	2.2
Lawyers	724	0.63	741	0.63	2.3
Lawyers and Judges NEC	33	0.03	33	0.03	0
Writers, Artists, Entertainers, Athletes	1,855	1.61	1,921	1.64	3.6
Authors	82	0.07	82	0.07	0
Technical Writers	58	0.05	65	0.06	12.1
Designers	510	0.44	534	0.46	4.7
Musicians and Composers	151	0.13	170	0.14	12.6
Actors and Directors	100	0.09	96	0.08	(4.0)
Painters, Sculptors, Craft Artists and Artist Printmakers	215	0.19	229	0.20	6.5
Photographers	117	0.10	112	0.10	(4.3)

(Continued)

Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1988 Number of Workers	1988 Percent of Total	1989 Number of Workers	1989 Percent of Total	1988-1989 Percent Change
Editors and Reporters	260	0.23	253	0.22	(2.7)
Public Relations Specialists	151	0.13	159	0.14	5.3
Announcers	52	0.05	51	0.04	(1.9)
Athletes	73	0.06	74	0.06	1.4
Writers, Artists, Entertainers, Athletes NEC	86	0.07	96	0.08	11.6
Other Professional Specialty	22	0.02	25	0.02	13.6
Technical, Sales, and Administrative Support	35,532	30.91	36,127	30.79	1.7
Technicians and Related Support	3,521	3.06	3,645	3.11	3.5
Health Technologists and Technicians	1,226	1.07	1,276	1.09	4.1
Clinical Laboratory Technologists and Technicians	272	0.24	308	0.26	13.2
Dental Hygienists	78	0.07	80	0.07	2.6
Radiologic Technicians	133	0.12	124	0.11	(6.8)
Licensed Practical Nurses	423	0.37	414	0.35	(2.1)
Health Technicians and Related Support NEC	320	0.28	350	0.30	9.4
Engineering and Related Technologists and Technicians	930	0.81	937	0.80	0.8
Electrical and Electronic Technicians	322	0.28	326	0.28	1.2
Drafting Occupations	290	0.25	296	0.25	2.1
Surveying and Mapping Technicians	78	0.07	70	0.06	(10.3)
Engineering and Related Technologists and Technicians NEC	240	0.21	245	0.21	2.1
Science Technicians	216	0.19	217	0.18	0.5
Biological Technicians	55	0.05	59	0.05	7.3
Chemical Technicians	81	0.07	74	0.06	(8.6)
Science Technicians NEC	80	0.07	84	0.07	5.0
Technicians, except Health, Engineering, and Science	1,149	1.00	1,216	1.04	5.8
Airplane Pilots and Navigators	88	0.08	109	0.09	23.9
Computer Programmers	570	0.50	561	0.48	(1.6)
Legal Assistants	203	0.18	210	0.18	3.4
Technicians, except Health, Engineering, and Science	288	0.25	336	0.29	16.7

(Continued)

Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1988 Number of Workers	1988 Percent of Total	1989 Number of Workers	1989 Percent of Total	1988-1989 Percent Change
Sales Occupations	13,747	11.96	14,065	11.99	2.3
Supervisors and Proprietors	3,658	3.18	3,828	3.26	4.6
Sales Representatives, Finance and Business Service	2,410	2.10	2,371	2.02	(1.6)
Insurance Sales	545	0.47	535	0.46	(1.8)
Real Estate Sales	792	0.69	772	0.66	(2.5)
Securities and Financial Services Sales	319	0.28	302	0.26	(5.3)
Advertising and Related Sales	168	0.15	156	0.13	(7.1)
Sales Occupations, Other Business Services	585	0.51	607	0.52	3.8
Sales Representatives, Commodities, except Retail	1,551	1.35	1,612	1.37	3.9
Sales Workers, Retail and Personal Services	6,068	5.28	6,186	5.27	1.9
Sales Workers, Motor Vehicles and Boats	294	0.26	300	0.26	2.0
Sales Workers, Apparel	462	0.40	449	0.38	(2.8)
Sales Workers, Shoes	112	0.10	107	0.09	(4.5)
Sales Workers, Furniture and Home Furnishings	166	0.14	152	0.13	(8.4)
Sales Workers, Radio, Television, Hi-Fi, and Appliances	180	0.16	203	0.17	12.8
Sales Workers, Hardware, and Building Supplies	198	0.17	206	0.18	4.0
Sales Workers, Parts	169	0.15	160	0.14	(5.3)
Sales Workers, Other Commodities	1,537	1.34	1,522	1.30	(1.0)
Sales Counter Clerks	189	0.16	190	0.16	0.5
Cashiers	2,337	2.03	2,473	2.11	5.8
Street and Door-to-Door Sales Workers	318	0.28	323	0.28	1.6
News Vendors	108	0.09	101	0.09	(6.5)
Sales-Related Occupations	59	0.05	68	0.06	15.3
Administrative Support, Including Clerical	18,264	15.89	18,416	15.69	0.8
Supervisors	764	0.66	736	0.63	(3.7)
General Office	458	0.40	446	0.38	(2.6)
Financial Records Processing	91	0.08	82	0.07	(9.9)

(Continued)

Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1988 Number of Workers	1988 Percent of Total	1989 Number of Workers	1989 Percent of Total	1988-1989 Percent Change
Supervisors, Distributing, Scheduling, and Adjusting	165	0.14	169	0.14	2.4
Supervisors NEC	50	0.04	39	0.03	(22.0)
Computer Equipment Operators	869	0.76	876	0.75	0.8
Computer Operators	865	0.75	870	0.74	0.6
Computer Equipment Operators NEC	4	0	6	0.01	50.0
Secretaries, Stenographers, and Typists	4,876	4.24	4,788	4.08	(1.8)
Secretaries	4,030	3.51	4,010	3.42	(0.5)
Stenographers	48	0.04	47	0.04	(2.1)
Typists	798	0.69	731	0.62	(8.4)
Information Clerks	1,479	1.29	1,451	1.24	(1.9)
Interviewers	163	0.14	183	0.16	12.3
Hotel Clerks	103	0.09	89	0.08	(13.6)
Transportation Ticket and Reservation Agents	114	0.10	112	0.10	(1.8)
Receptionists	848	0.74	815	0.69	(3.9)
Information Clerks NEC	251	0.22	252	0.21	0.4
Records Processing Occupations, Except Financial	827	0.72	851	0.73	2.9
Order Clerks	197	0.17	199	0.17	1.0
Personnel Clerks, except Payroll and Timekeeping	65	0.06	77	0.07	18.5
Library Clerks	143	0.12	144	0.12	0.7
File Clerks	271	0.24	284	0.24	4.8
Records Clerks	132	0.11	116	0.10	(12.1)
Records Processing Occupations, except Financial	19	0.02	31	0.03	63.2
Financial Records Processing	2,414	2.10	2,394	2.04	(0.8)
Bookkeepers, Accounting, and Auditing Clerks	1,970	1.71	1,926	1.64	(2.2)
Payroll and Timekeeping Clerks	173	0.15	177	0.15	2.3
Billing Clerks	157	0.14	159	0.14	1.3
Cost and Rate Clerks	75	0.07	83	0.07	10.7
Financial Records Processing NEC	39	0.03	49	0.04	25.6

(Continued)

Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1988 Number of Workers	1988 Percent of Total	1989 Number of Workers	1989 Percent of Total	1988-1989 Percent Change
Duplicating, Mail, and Other Office Machine Operators	68	0.06	65	0.06	(4.4)
Communications Equipment Operators	218	0.19	210	0.18	(3.7)
Telephone Operators	210	0.18	201	0.17	(4.3)
Communications Equipment Operators NEC	8	0.01	9	0.01	12.5
Mail and Message Distributing Occupations	936	0.81	952	0.81	1.7
Postal Clerks, except Mail Carriers	313	0.27	313	0.27	0
Mail Carriers, Postal Service	320	0.28	327	0.28	2.2
Mail Clerks, except Postal Service	163	0.14	179	0.15	9.8
Messengers	141	0.12	133	0.11	(5.7)
Material Recording, Scheduling, and Distributing	1,681	1.46	1,745	1.49	3.8
Dispatchers	171	0.15	189	0.16	10.5
Production Coordinators	192	0.17	196	0.17	2.1
Traffic, Shipping and Receiving Clerks	521	0.45	550	0.47	5.6
Stock and Inventory Clerks	559	0.49	561	0.48	0.4
Weighers, Measurers, and Checkers	72	0.06	76	0.06	5.6
Expediters	95	0.08	96	0.08	1.1
Material Clerks NEC	71	0.06	77	0.07	8.5
Adjusters and Investigators	949	0.83	1,079	0.92	13.7
Insurance Adjusters, Examiners, and Investigators	287	0.25	325	0.28	13.2
Investigators and Adjusters, except Insurance	466	0.41	546	0.47	17.2
Eligibility Clerks, Social Welfare	65	0.06	72	0.06	10.8
Bill and Account Collectors	130	0.11	136	0.12	4.6
Miscellaneous Administrative Support	3,183	2.77	3,269	2.79	2.7
General Office Clerks	833	0.72	810	0.69	(2.8)
Bank Tellers	478	0.42	503	0.43	5.2
Data Entry Keyers	362	0.31	414	0.35	14.4
Statistical Clerks	85	0.07	86	0.07	1.2

(Continued)

Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1988 Number of Workers	1988 Percent of Total	1989 Number of Workers	1989 Percent of Total	1988-1989 Percent Change
Teachers' Aides	423	0.37	440	0.37	4.0
Miscellaneous Administrative Support NEC	1002	0.87	1,016	0.87	1.4
Service Occupations	15,332	13.34	15,556	13.26	1.5
Private Household	909	0.79	872	0.74	(4.1)
Child Care Workers	378	0.33	358	0.31	(5.3)
Cleaners and Servants	476	0.41	464	0.40	(2.5)
Private Household NEC	55	0.05	50	0.04	(9.1)
Protective Service	1,944	1.69	1,960	1.67	0.8
Supervisors, Protective Services	174	0.15	169	0.14	(2.9)
Supervisors, Police and Detectives	93	0.08	83	0.07	(10.8)
Supervisors, Protective Services NEC	81	0.07	86	0.07	6.2
Firefighting and Fire Prevention	218	0.19	208	0.18	(4.6)
Firefighting Occupations	195	0.17	188	0.16	(3.6)
Firefighting and Fire Prevention NEC	23	0.02	20	0.02	(13.0)
Police and Detectives	755	0.66	803	0.68	6.4
Police and Detectives, Public Service	427	0.37	461	0.39	8.0
Sheriffs, Bailiffs, and Other Law Enforcement Officers	111	0.10	112	0.10	0.9
Correctional Institution Officers	217	0.19	230	0.20	6.0
Guards	796	0.69	781	0.67	(1.9)
Guards and Police, except Public Service	675	0.59	658	0.56	(2.5)
Guards, NEC	121	0.11	123	0.10	1.7
Service Occupations, except Private Household, Protective Service	12,479	10.85	12,724	10.84	2.0
Food Preparation and Service Occupations	5,182	4.51	5,351	4.56	3.3
Supervisors	325	0.28	356	0.30	9.5
Bartenders	324	0.28	322	0.27	(0.6)
Waiters and Waitresses	1,363	1.19	1,389	1.18	1.9
Cooks, except Short Order	1,634	1.42	1,713	1.46	4.8

(Continued)

Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1988 Number of Workers	1988 Percent of Total	1989 Number of Workers	1989 Percent of Total	1988-1989 Percent Change
Short-Order Cooks	95	0.08	91	0.08	(4.2)
Food Counter, Fountain, and Related Occupations	325	0.28	354	0.30	8.9
Kitchen Workers, Food Preparation	132	0.11	126	0.11	(4.5)
Waiters' and Waitresses' Assistants	339	0.29	352	0.30	3.8
Miscellaneous Food Preparation	645	0.56	648	0.55	0.5
Health Service Occupations	1,977	1.72	2,042	1.74	3.3
Dental Assistants	165	0.14	187	0.16	13.3
Health Aides, except Nursing	407	0.35	416	0.35	2.2
Nursing Aides, Orderlies, and Attendants	1,404	1.22	1,439	1.23	2.5
Cleaning and Building Service Occupations	2,994	2.60	2,997	2.55	0.1
Supervisors	159	0.14	154	0.13	(3.1)
Maids and Housemen	644	0.56	646	0.55	0.3
Janitors and Cleaners	2,133	1.86	2,148	1.83	0.7
Cleaning and Building Service Occupations, NEC	58	0.05	49	0.04	(15.5)
Personal Service Occupations	2,327	2.02	2,333	1.99	0.3
Barbers	94	0.08	81	0.07	(13.8)
Hairdressers and Cosmetologists	769	0.67	736	0.63	(4.3)
Attendants, Amusement and Recreation Facilities	130	0.11	133	0.11	2.3
Public Transportation Attendants	77	0.07	86	0.07	11.7
Welfare Service Aides	92	0.08	95	0.08	3.3
Child Care Workers	853	0.74	861	0.73	0.9
Personal Service Occupations, NEC	312	0.27	341	0.29	9.3
Precision Production, Craft and Repair	13,664	11.88	13,818	11.78	1.1
Mechanics and Repairers	4,454	3.87	4,550	3.88	2.2
Supervisors	256	0.22	285	0.24	11.3
Mechanics and Repairers, except Supervisors	4,198	3.65	4,265	3.63	1.6

(Continued)

Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1988 Number of Workers	1988 Percent of Total	1989 Number of Workers	1989 Percent of Total	1988-1989 Percent Change
Vehicle and Mobile Equipment Mechanics and Repairers	1,811	1.58	1,793	1.53	(1.0)
Automobile Mechanics	879	0.76	880	0.75	0.1
Bus, Truck, and Stationery Engine Mechanics	325	0.28	320	0.27	(1.5)
Aircraft Engine Mechanics	131	0.11	122	0.10	(6.9)
Small-Engine Repairers	70	0.06	65	0.06	(7.1)
Automobile Body and Related Repairers	194	0.17	191	0.16	(1.5)
Heavy Equipment Mechanics	159	0.14	160	0.14	0.6
Vehicle and Mobile Equipment	53	0.05	55	0.05	3.8
Industrial Machinery Repairers	547	0.48	539	0.46	(1.5)
Electrical and Electronic Equipment Repairers	677	0.59	680	0.58	0.4
Electronic Repairers, Communications and Industrial Equipment	165	0.14	165	0.14	0
Data Processing Equipment Repairers	140	0.12	152	0.13	8.6
Telephone Line Installers and Repairers	61	0.05	54	0.05	(11.5)
Telephone Installers and Repairers	202	0.18	193	0.16	(4.5)
Electronic and Electronic Equipment NEC	109	0.09	116	0.10	6.4
Heating, Air Conditioning, and Refrigeration Mechanics	262	0.23	279	0.24	6.5
Miscellaneous Mechanics and Repairers	874	0.76	948	0.81	8.5
Office Machine Repairers	60	0.05	67	0.06	11.7
Millwrights	96	0.08	101	0.09	5.2
Miscellaneous Mechanics NEC	718	0.62	780	0.66	8.6
Mechanics and Repairers, NEC	27	0.02	26	0.02	(3.7)
Construction Trades	5,098	4.43	5,142	4.38	0.9
Supervisors	617	0.54	662	0.56	7.3
Construction Trades, except Supervisors	4,481	3.90	4,479	3.82	0
Brickmasons and Stonemasons	202	0.18	219	0.19	8.4
Carpet Installers	108	0.09	109	0.09	0.9
Carpenters	1,427	1.24	1,369	1.17	(4.1)

(Continued)

Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1988 Number of Workers	1988 Percent of Total	1989 Number of Workers	1989 Percent of Total	1988-1989 Percent Change
Drywall Installers	149	0.13	155	0.13	4.0
Electricians	701	0.61	702	0.60	0.1
Electrical Power Installers and Repairers	101	0.09	104	0.09	3.0
Painters, Construction, and Maintenance	525	0.46	543	0.46	3.4
Plumbers, Pipefitters, and Steamfitters	494	0.43	456	0.39	(7.7)
Concrete and Terrazzo Finishers	85	0.07	77	0.07	(9.4)
Insulation Workers	54	0.05	64	0.05	18.5
Roofers	156	0.14	178	0.15	14.1
Structural Metal Workers	48	0.04	63	0.05	31.3
Construction Trade NEC	431	0.37	440	0.37	2.1
Extractive Occupations	144	0.13	138	0.12	(4.2)
Precision Production Occupations	3,968	3.45	3,988	3.40	0.5
Supervisors	1,361	1.18	1,353	1.15	(0.6)
Precision Metalworking	896	0.78	911	0.78	1.7
Tool and Die Makers	145	0.13	148	0.13	2.1
Machinists	497	0.43	479	0.41	(3.6)
Sheet-Metal Workers	126	0.11	141	0.12	11.9
Precision Metalworking, NEC	128	0.11	143	0.12	11.7
Precision Woodworking Occupations	106	0.09	95	0.08	(10.4)
Cabinet Makers and Bench Carpenters	66	0.06	56	0.05	(15.2)
Precision Woodworking, NEC	40	0.03	39	0.03	(2.5)
Precision Textile, Apparel, Furnishings Machine Workers	296	0.26	277	0.24	(6.4)
Dressmakers	126	0.11	117	0.10	(7.1)
Upholsterers	84	0.07	71	0.06	(15.5)
Precision Textile, NEC	86	0.07	89	0.08	3.5
Precision Workers, Assorted Materials	529	0.46	565	0.48	6.8
Optical Goods Workers	60	0.05	80	0.07	33.3

(Continued)

Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1988 Number of Workers	1988 Percent of Total	1989 Number of Workers	1989 Percent of Total	1988-1989 Percent Change
Dental Laboratory and Medical Appliance Technicians	49	0.04	51	0.04	4.1
Electrical and Electronic Equipment Assemblers	305	0.27	316	0.27	3.6
Precision Workers Assorted NEC	115	0.10	118	0.10	2.6
Precision Food Production Occupations	418	0.36	414	0.35	(1.0)
Butchers and Meat Cutters	258	0.22	266	0.23	3.1
Bakers	126	0.11	113	0.10	(10.3)
Precision Food Production NEC	34	0.03	35	0.03	2.9
Precision Inspectors, Testers, and Related Workers	126	0.11	125	0.11	(0.8)
Inspectors, Testers and Graders	113	0.10	113	0.10	0
Precision Inspectors, NEC	13	0.01	12	0.01	(7.7)
Plant and System Operators	236	0.21	249	0.21	5.5
Stationary Engineers	103	0.09	109	0.09	5.8
Plant and System Operators NEC	133	0.12	140	0.12	5.3
Operators, Fabricators, and Laborers	17,814	15.49	18,022	15.36	1.2
Machine Operators, Assemblers, and Inspectors	8,117	7.06	8,248	7.03	1.6
Machine Operators and Tenders, except Precision	5,362	4.66	5,381	4.59	0.4
Metalworking and Plastic Working Machine Operators	465	0.40	470	0.40	1.1
Lathe and Turning Machine Operators	63	0.05	55	0.05	(12.7)
Punching and Stamping Press Machine Operators	123	0.11	120	0.10	(2.4)
Grinding, Abrading, Buffing, and Polishing Machine Operators	141	0.12	143	0.12	1.4
Metalworking and Plastic Operators NEC	138	0.12	152	0.13	10.1
Metal and Plastic Processing Machine Operators	170	0.15	160	0.14	(5.9)
Molding and Casing Machine Operators	102	0.09	97	0.08	(4.9)
Metal and Plastic Processing, NEC	68	0.06	63	0.05	(7.4)
Woodworking Machine Operators	159	0.14	165	0.14	3.8
Sawing Machine Operators	105	0.09	96	0.08	(8.6)
Other Woodworking, NEC	54	0.05	69	0.06	27.8

(Continued)

Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1988 Number of Workers	1988 Percent of Total	1989 Number of Workers	1989 Percent of Total	1988-1989 Percent Change
Printing Machine Operators	505	0.44	474	0.40	(6.1)
Printing Machine Operators	339	0.29	324	0.28	(4.4)
Typesetters and Compositors	67	0.06	66	0.06	(1.5)
Printing Machine Operators, NEC	99	0.09	84	0.07	(15.2)
Textile, Apparel, and Furnishings Machine Operators	1,355	1.18	1,356	1.16	0.1
Winding and Twisting Machine Operators	76	0.07	77	0.07	1.3
Textile Sewing Machine Operators	749	0.65	757	0.65	1.1
Pressing Machine Operators	146	0.13	134	0.11	(8.2)
Laundering and Dry Cleaning Machine Operator	222	0.19	220	0.19	(0.9)
Textile, Apparel, and Furnishings, NEC	162	0.14	168	0.14	3.7
Machine Operators, Assorted Materials	2,680	2.33	2,736	2.33	2.1
Packaging and Filling Machine Operators	414	0.36	442	0.38	6.8
Mixing and Blending Machine Operators	102	0.09	110	0.09	7.8
Separating, Filtering, and Clarifying Machine Operators	56	0.05	62	0.05	10.7
Painting and Paint Spraying Machine Operator	200	0.17	186	0.16	(7.0)
Furnace, Kiln, and Oven Operators, except Food	102	0.09	96	0.08	(5.9)
Slicing and Cutting Machine Operators	215	0.19	219	0.19	1.9
Photographic Process Machine Operators	98	0.09	91	0.08	(7.1)
Machine Operators, Assorted Materials, NEC	1493	1.30	1530	1.30	2.5
Other Machine Operators and Tenders	28	0.02	20	0.02	(28.6)
Fabricators, Assemblers, and Hand-Working Occupations	1,906	1.66	2,011	1.71	5.5
Welders and Cutters	555	0.48	612	0.52	10.3
Assemblers	1,141	0.99	1,177	1.00	3.2
Fabricators, Assemblers, NEC	210	0.18	222	0.19	5.7
Production Inspectors, Testers, Samplers, and Weighers	849	0.74	856	0.73	0.8
Production Inspectors, Checkers, and Examiners	683	0.59	688	0.59	0.7
Production Testers	63	0.05	60	0.05	(4.8)

(Continued)

Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1988 Number of Workers	1988 Percent of Total	1989 Number of Workers	1989 Percent of Total	1988-1989 Percent Change
Graders and Sorters, except Agricultural	96	0.08	102	0.09	6.3
Production Inspectors, NEC	7	0.01	6	0.01	(14.3)
Transportation and Material-Moving Occupations	4,831	4.20	4,886	4.16	1.1
Motor Vehicle Operators	3,592	3.12	3,602	3.07	0.3
Truck Drivers, Heavy	1,826	1.59	1,850	1.58	1.3
Truck Drivers, Light	782	0.68	766	0.65	(2.0)
Drivers-Sales Workers	201	0.17	192	0.16	(4.5)
Bus Drivers	450	0.39	440	0.37	(2.2)
Taxi-Cab Drivers and Chauffeurs	218	0.19	220	0.19	0.9
Motor Vehicle Operators, NEC	115	0.10	134	0.11	16.5
Transportation Occupations, except Motor Vehicle	195	0.17	177	0.15	(9.2)
Rail Transportation Occupations	137	0.12	129	0.11	(5.8)
Locomotive Operating Occupations	51	0.04	0	0	(100.0)
Rail NEC	86	0.07	129	0.11	50.0
Water Transportation Occupations	58	0.05	0	0	(100.0)
Material Moving Equipment Operators	1,043	0.91	1,107	0.94	6.1
Operating Engineers	210	0.18	220	0.19	4.8
Crane and Tower Operators	88	0.08	99	0.08	12.5
Excavating and Loading Machine Operators	108	0.09	128	0.11	18.5
Grader, Dozer, and Scraper Operators	92	0.08	98	0.08	6.5
Industrial Truck and Tractor Equipment Operators	431	0.37	452	0.39	4.9
Material Moving, NEC	114	0.10	110	0.09	(3.5)
Handlers, Equipment Cleaners, Helpers and Laborers	4,866	4.23	4,888	4.17	0.5
Helpers, Construction and Extractive Occupations	156	0.14	133	0.11	(14.7)
Helpers, Construction Trades	141	0.12	123	0.10	(12.8)
Helpers, NEC	15	0.01	10	0.01	(33.3)
Construction Laborers	799	0.69	755	0.64	(5.5)
Production Helpers	64	0.06	82	0.07	28.1

(Continued)

Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1988 Number of Workers	1988 Percent of Total	1989 Number of Workers	1989 Percent of Total	1988-1989 Percent Change
Freight, Stock, and Material Handlers	1,756	1.53	1,743	1.49	(0.7)
Stock Handlers and Baggers	891	0.77	900	0.77	1.0
Machine Feeders and Offbearers	110	0.10	91	0.08	(17.3)
Freight, Stock, Material, NEC	755	0.66	752	0.64	(0.4)
Garage and Service Station Related Occupations	246	0.21	230	0.20	(6.5)
Vehicle Washers and Equipment Cleaners	253	0.22	281	0.24	11.1
Hand Packers and Packagers	298	0.26	327	0.28	9.7
Laborers, except Construction	1,248	1.09	1,288	1.10	3.2
Handlers, Equipment Cleaners, Helpers, and Laborers	46	0.04	49	0.04	6.5
Farming, Forestry, and Fishing	3,437	2.99	3,421	2.92	(0.5)
Farm Operators and Managers	1,286	1.12	1,269	1.08	(1.3)
Farmers	1,154	1.00	1,118	0.95	(3.1)
Farm Managers	133	0.12	150	0.13	12.8
Other Agricultural and Related Occupations	1,978	1.72	1,976	1.68	(0.1)
Farm Occupations, except Managerial	1,020	0.89	964	0.82	(5.5)
Farm Workers	949	0.83	893	0.76	(5.9)
Farm Occupations, NEC	71	0.06	71	0.06	0
Related Agricultural Occupations	958	0.83	1,012	0.86	5.6
Supervisors	76	0.07	73	0.06	(3.9)
Groundskeepers and Gardeners, except Farmers	765	0.67	816	0.70	6.7
Animal Caretakers, except Farmers	101	0.09	104	0.09	3.0
Related Agriculture Occupations, NEC	16	0.01	19	0.02	18.8
Forestry and Logging Occupations	117	0.10	118	0.10	0.9
Timber Cutting and Logging	84	0.07	82	0.07	(2.4)
Forestry and Logging, NEC	33	0.03	36	0.03	9.1
Fishers, Hunters, and Trappers	56	0.05	59	0.05	5.4
Total	114,969	100.00	117,342	100.00	2.1

Note: Columns may not add to totals shown because of rounding.
NEC = Not elsewhere classified

Source: U.S. Department of Labor, Bureau of Labor Statistics

Table W-2. Distribution of U.S. Work Force by Major Occupational Category (Thousands of Workers)

Occupational Classification	Actual			Estimated		
	1988	1989	1991	1994	1997	2000
Executive, Administrative, and Managerial	14,216	14,848	15,302	15,982	16,663	17,344
Professional Specialty	14,974	15,550	16,099	16,922	17,745	18,568
Technicians and Related Support	3,521	3,645	3,825	4,094	4,364	4,634
Sales Occupations	13,747	14,065	14,497	15,145	15,793	16,441
Administrative Support, Including Clerical	18,264	18,416	18,780	19,327	19,873	20,419
Private Household	909	872	871	868	866	864
Protective Service	1,944	1,960	2,037	2,152	2,268	2,383
Service, except Private Household and Protective	12,479	12,724	13,192	13,895	14,597	15,299
Precision Production, Craft, and Repair	13,664	13,818	14,036	14,363	14,690	15,017
Operators, Fabricators, and Laborers	17,814	18,022	18,026	18,033	18,039	18,046
Farming, Forestry, and Fishing	3,437	3,422	3,394	3,354	3,313	3,272
Total	114,969	117,342	120,059	124,135	128,211	132,287

Source: U.S. Department of Labor, Bureau of Labor Statistics Dataquest June 1990

Figure 8. Actual and Estimated Number of Employed U.S. Civilian Workers

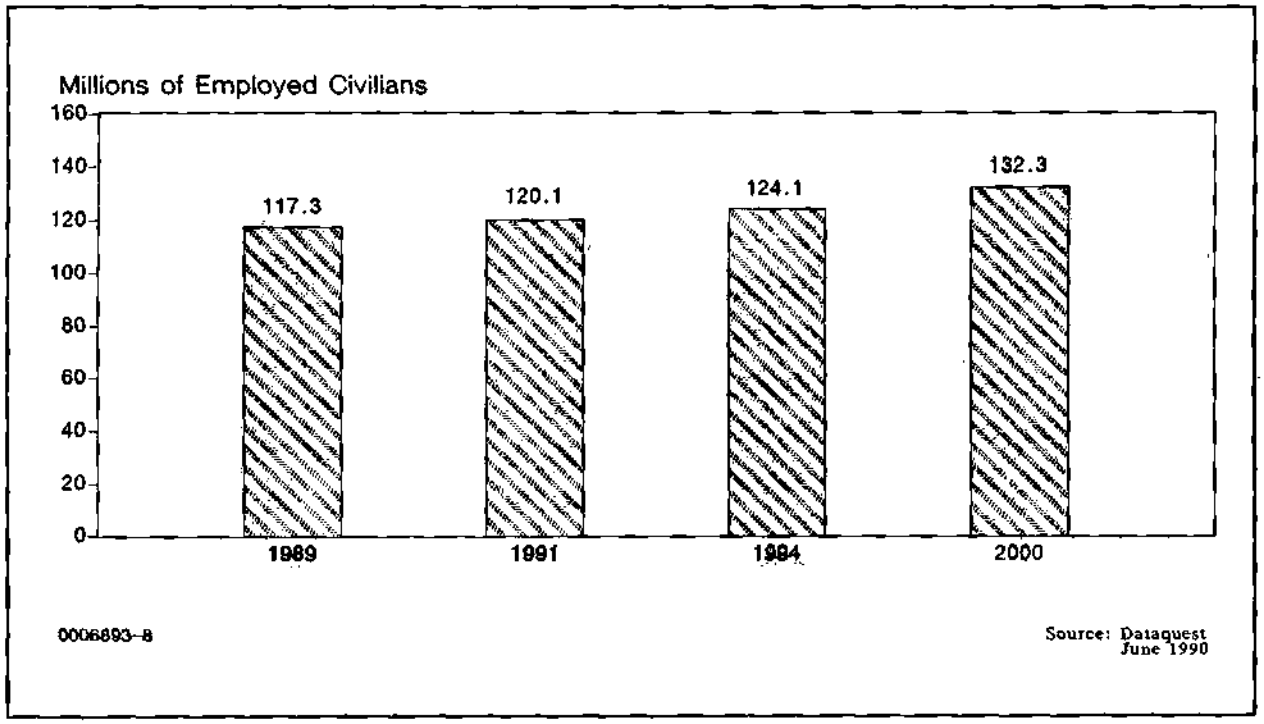


Table W-3. Employment Growth by Industry for 1988 and 1989
Annual Estimates through 2000 (Thousands of Workers)

	Actual		Estimated			
Industry	1988	1989	1991	1994	1997	2000
Agriculture	3,169	3,199	3,195	3,187	3,180	3,173
Mining	753	719	718	717	715	714
Construction	7,603	7,680	7,838	8,075	8,312	8,549
Manufacturing	21,320	21,652	21,626	21,590	21,555	21,523
Transportation and Public Utilities	8,064	8,094	8,203	8,367	8,531	8,695
Wholesale and Retail Trade	23,664	24,229	24,824	25,717	26,611	27,504
Finance	7,921	7,989	8,168	8,436	8,705	8,974
Services	37,043	38,227	39,871	42,334	44,794	47,251
Private Household	1,163	1,108	1,106	1,103	1,100	1,098
Public Administration	5,432	5,553	5,616	5,712	5,808	5,904
Total	114,969	117,342	120,059	124,135	128,211	132,287

Source: U.S. Department of Labor, Bureau of Labor Statistics
Dataquest
June 1990

Figure 9. Actual and Estimated Employment Growth by Industry, 1989-2000

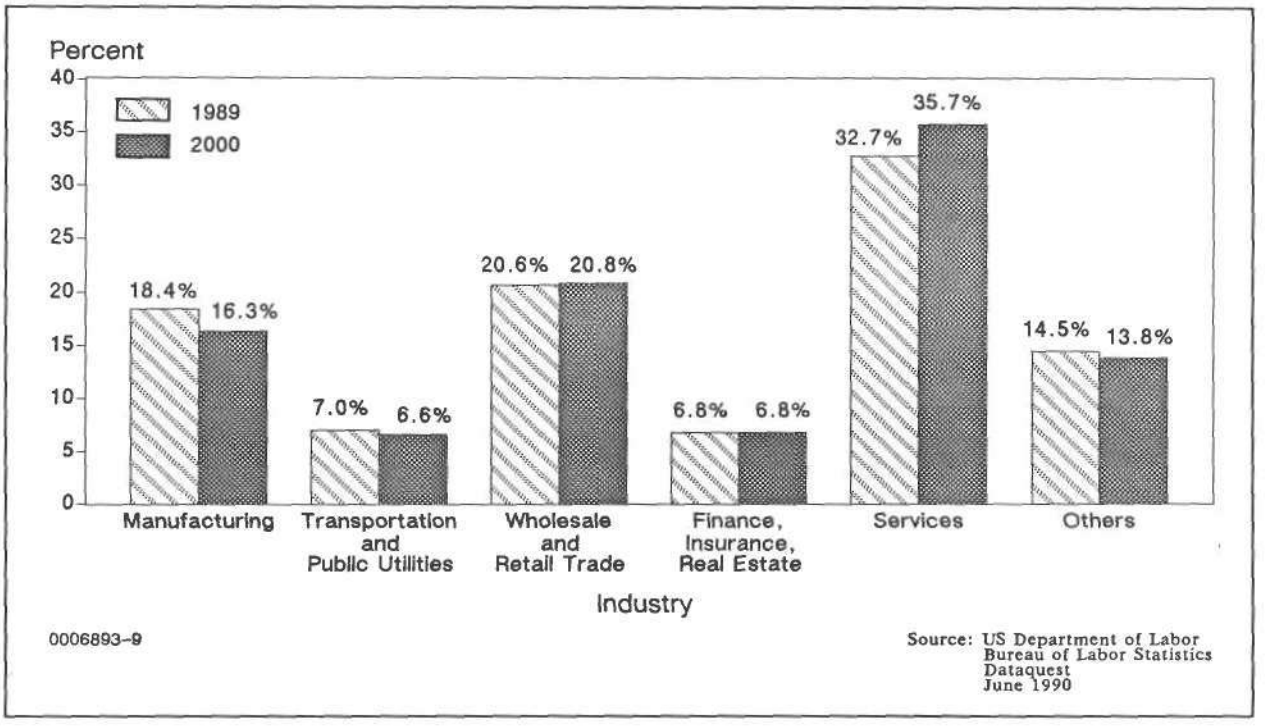


Table W-4. Estimated U.S. White-Collar Workers by Job Classification

Job Function	1988 Total White-Collar Workers (Millions)	1988 Percent Total Work Force	1989 Total White-Collar Workers (Millions)	1989 Percent Total Work Force	1994 Total White-Collar Workers (Millions)	1994 Percent Total Work Force
Executive, Administrative, and Managerial	14.2	12.4	14.8	12.6	16.0	12.9
Professional Specialty	15.0	13.0	15.6	13.3	16.9	13.6
Technicians and Related Occupations	3.5	3.0	3.6	3.1	4.1	3.3
Sales Workers	13.7	11.9	14.1	12.0	15.2	12.2
Administrative Support (Including Clerical)	18.3	15.9	18.4	15.7	19.3	15.5
Total White Collar	64.7	56.2	66.5	56.7	71.5	57.5
Total Work Force	114.9	100.0	117.3	100.0	124.2	100.0

Source: U.S. Department of Labor, Bureau of Labor Statistics
Dataquest
June 1990

Figure 10. 1989 White-Collar Workers by Job Classification as a Percentage of Total Work Force

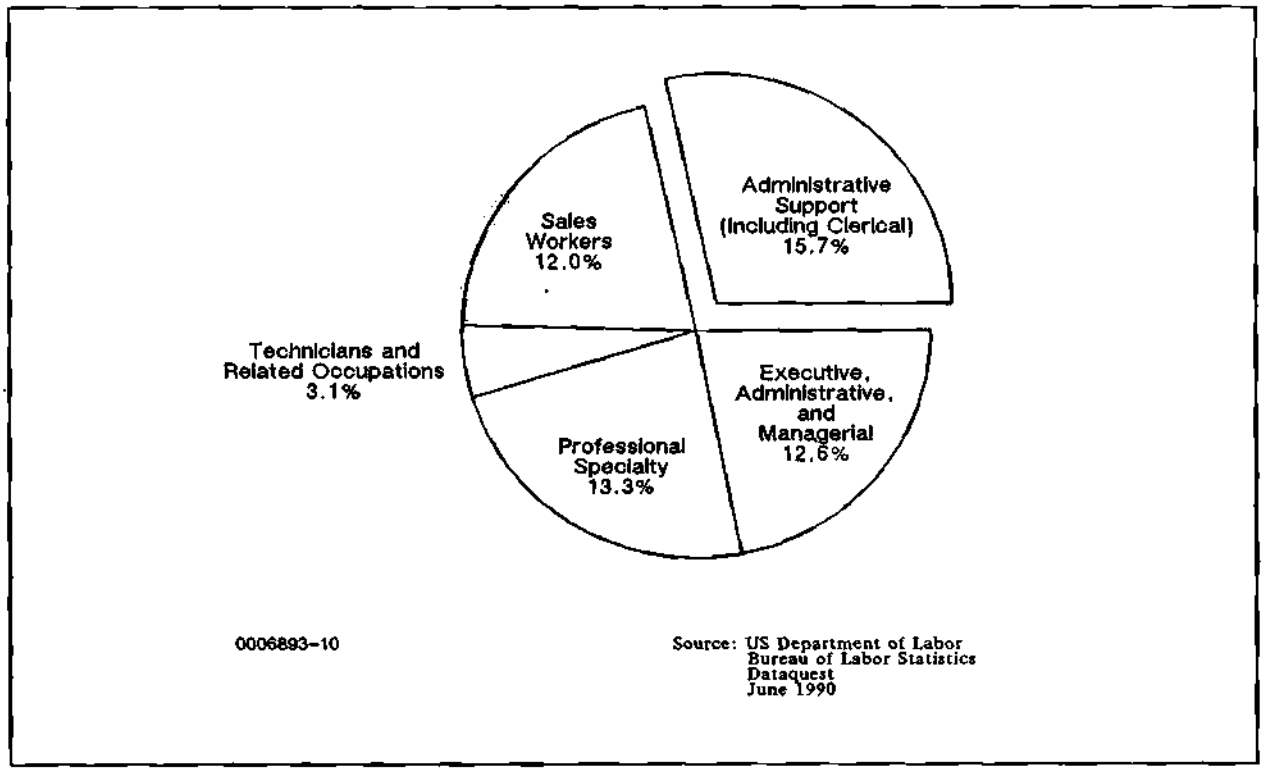


Table W-5. Estimated U.S. White-Collar Workers by Industry Sector

Industry Sector	1988 Total White-Collar Workers (Millions)	1988 Percent Total White Collar	1989 Total White-Collar Workers (Millions)	1989 Percent Total White Collar	1994 Total White-Collar Workers (Millions)	1994 Percent Total White Collar
Services	24.4	37.7	25.4	38.2	29.3	41.0
Wholesale and Retail Trade	14.8	22.9	15.1	22.7	16.0	22.4
Manufacturing	8.1	12.5	8.3	12.5	7.9	11.0
Finance, Insurance, and Real Estate	7.3	11.3	7.4	11.1	8.0	11.2
Transportation, Communication, and Utilities	4.1	6.3	4.2	6.3	4.2	5.9
Others*	6.0	9.3	6.1	9.2	6.1	8.5
Total White Collar	64.7	100.0	66.5	100.0	71.5	100.0

*Includes agriculture, mining, construction, and public administration.

Source: U.S. Department of Labor, Bureau of Labor Statistics
Dataquest
June 1990

Table W-6. Estimated U.S. White-Collar Workers as a Percent of Total Work Force by Industry Sector

Industry Sector	1988 Total Work Force (Millions)	1988 Percent White Collar	1989 Total Work Force (Millions)	1989 Percent White Collar	1994 Total Work Force (Millions)	1994 Percent White Collar
Services	37.0	65.6	38.2	66.6	42.3	69.1
Wholesale and Retail Trade	23.7	65.8	24.2	62.2	25.7	62.1
Manufacturing	21.3	38.0	21.6	38.2	21.6	36.6
Finance, Insurance, and Real Estate	7.9	92.9	8.0	93.2	8.4	94.7
Transportation, Communication, and Utilities	8.1	50.8	8.1	51.9	8.4	50.9
Others*	16.9	35.8	17.2	35.0	17.7	33.8
Total Work Force	114.9	56.3	117.3	56.7	124.1	57.6

*Includes agriculture, mining, construction, and public administration; average of all four industries.

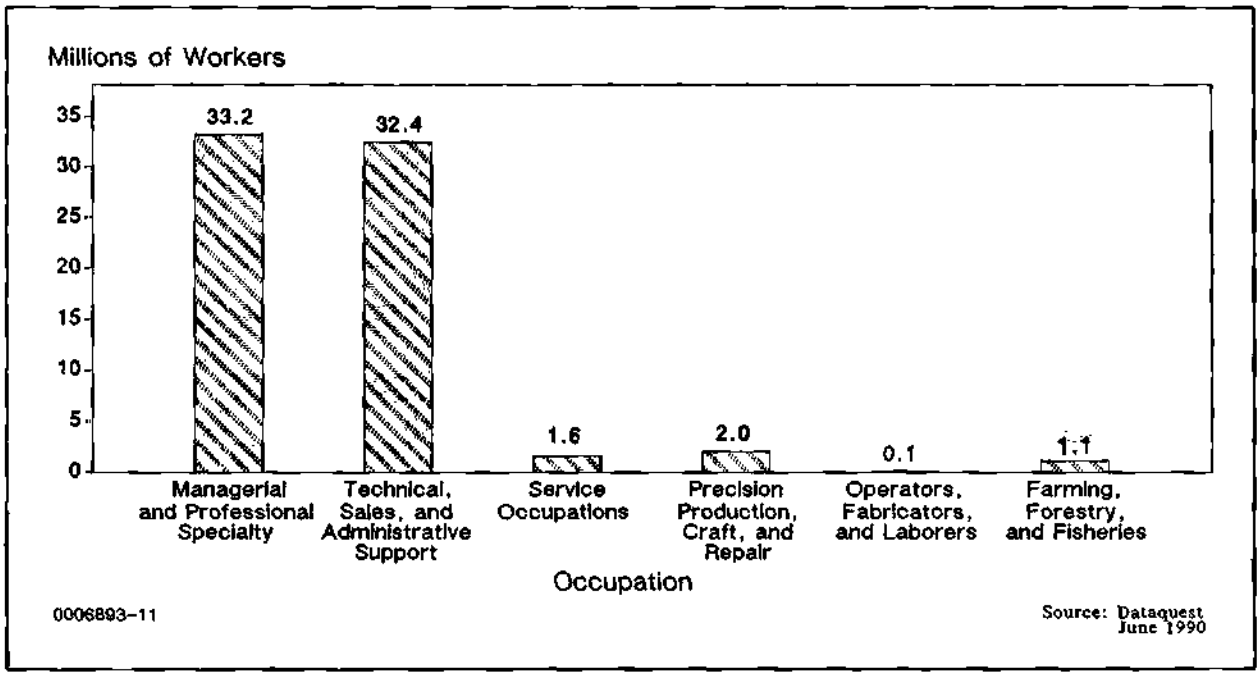
Source: U.S. Department of Labor, Bureau of Labor Statistics
Datapoint
June 1990

Table W-7. Number of Desktops by Job Classification (Thousands)

Occupational Classification	1989	1990	Estimated 1992	1994	1996
Managerial and Professional Specialty	33,179	33,747	34,885	36,022	37,160
Technical, Sales, and Administrative Support	32,394	32,827	33,694	34,561	35,428
Service Occupations	1,620	1,648	1,703	1,758	1,814
Precision Production, Craft, and Repair	2,044	2,058	2,085	2,113	2,141
Operators, Fabricators, and Laborers	114	117	123	130	136
Farming, Forestry, and Fishing	1,092	1,088	1,081	1,074	1,067
Total	70,443	71,485	73,571	75,658	77,746

Source: Dataquest
June 1990

Figure 11. Number of Desktops by Major Occupational Category, 1989



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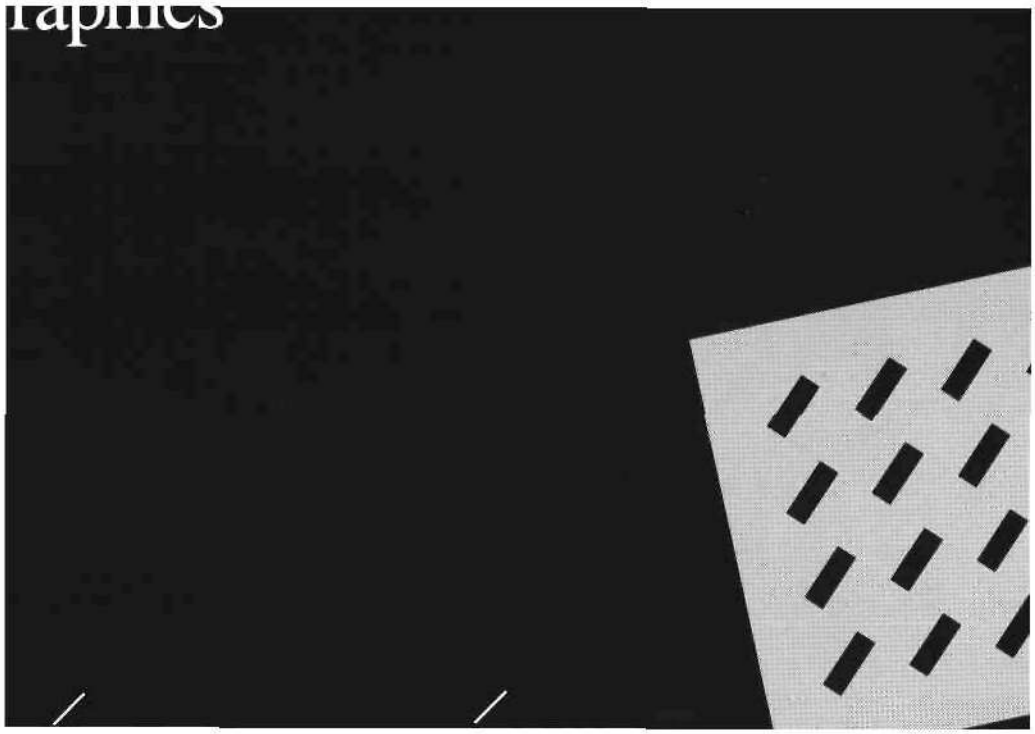

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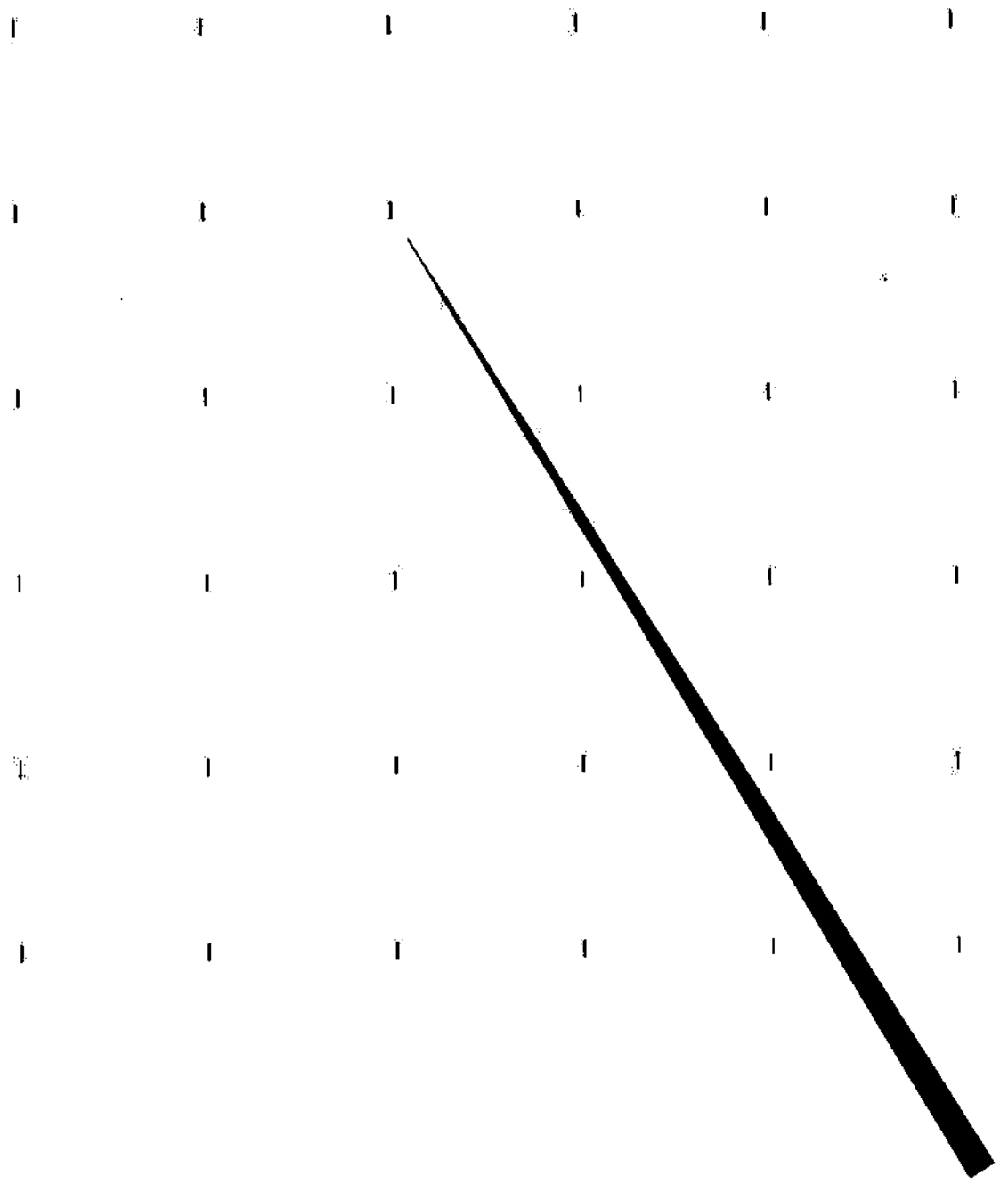

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Demographic Terms

desktop. Defined in Dataquest's desktop analyses as a potential location for a desktop information device.

information worker. An individual who is or will be a user of an automated desktop information device.

establishment. A single physical location where business activity is conducted, whether or not there are any financial links to other units. Establishments include independently owned and operated businesses as well as the headquarters, subsidiaries, and branches of larger firms.

enterprise. An aggregation of establishments that have common ownership. This definition includes a parent company plus all of its subsidiaries and branches, as well as single establishments that have no financial links with other establishments.

sole proprietorship. A business that is fully owned and managed by a single individual.

partnership. An association of two or more persons to carry on as co-owners of a business. Partners may be individuals, corporations, estates, trusts, or other partnerships and may be actively or passively involved in business operations.

corporation. A self-perpetuating body set up as a business entity separate from its owners. This means that ownership is separate from management and incurs limited liability.

household. A housing unit intended as separate living quarters. A household includes all persons, either related or unrelated, living in the unit.

householder. The person in whose name the housing unit is owned or rented. The term is never applied to either husbands or wives in married-couple families, but relates only to persons in families maintained by either men or women without a spouse.

family. A group of two or more persons residing together who are related by birth, marriage, or adoption.

nonfamily. A group of two or more persons residing together who are unrelated.

elementary grades. Elementary grades are classified through the school district. If the district covers kindergarten through eighth grade, then up through eighth grade is considered elementary. If the district covers only through sixth grade, then only through sixth grade is considered elementary.

secondary grades. Secondary grades are classified like elementary grades, by district. If the district covers eighth through twelfth grades, then grades eight through twelve are considered secondary. Likewise, if the district covers grades nine through twelve, then only nine through twelve are considered secondary.

university. A school that places its primary emphasis on graduate and professional education. Universities offer doctoral studies in numerous fields and support at least two professional programs.

other four-year colleges. A school that places its primary emphasis on undergraduate education. A four-year college can offer doctorate and professional degrees, but its graduate programs will not be as extensive as those of a university.

two-year colleges. A school that offers an associate degree, but not a baccalaureate degree. Two-year colleges are also called junior colleges.

vocational school. A school that offers a certification in a specialized profession but does not offer classes applicable toward an associate or baccalaureate degree.

total population. Includes all citizens, armed forces personnel, and merchant marines of the United States living at home or abroad.

civilian population. Resident population of the United States that does not include resident or overseas armed forces, merchant marines, or citizens living outside the United States.

participation rates. Represents the proportion of the population that is in the labor force.

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occupational tenure. The cumulative number of years a person works in his or her current occupation, regardless of the number of employers, interruptions in employment, or times spent in other occupations.

median income. Indicates the value that divides the income distribution into two equal parts, one part having values above the median and the other having values below the median.

CAGR (compound annual growth rate). Calculated using the formula:

$$\text{CAGR} = \left(\frac{\text{Value in year 1+n}}{\text{Value in year 1}}\right)^{\left(\frac{1}{n}\right)} - 1$$

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Education and Government Environments

The United States places a high value on education. During the 1987-1988 school year, in a country of 243 million people, approximately 65 million Americans were involved, directly or indirectly, in providing or receiving formal education.

- Apple Computer has a dominant position in the public elementary and secondary school market. Apple leads the way with a 61 percent market share, followed by Radio Shack, a distant second with an 11.7 percent share.

- While the installed base growth rate for both Commodore and Radio Shack have tapered off significantly from the 1987-1988 to the 1988-1989 school year (1.0 and 3.7, respectively), IBM's presence in the elementary and secondary school markets has surged. IBM's installed base of microcomputers has grown 35 percent from the 1987-1988 school year (107,600 units) to 147,700 units for 1988-1989.

- Enrollment in elementary schools is increasing steadily as the mini baby boom trend continues. This upward trend, which contrasts sharply with the period of decline between 1971 and 1984, is expected to continue for a number of years.

- Secondary school enrollment will not benefit from the new wave of students in the elementary levels until the early 1990s. Starting then, increases in enrollment in grades 9 through 12 will be maintained for several years.

- College enrollment has reached a record level, although the "college-age" population has declined. According to the Center of Education Statistics, the number of college-age students (those between the ages of 18 and 24) peaked in 1981 and then started to decline. Total enrollment, however, has remained at a relatively high level. The increased number of older students, especially women, attending college, and a high rate of enrollment by recent high school graduates, helps maintain total enrollment numbers.

- In 1986, 75 percent of the population 25 years old and older had completed high school and 19 percent had completed 4 years of college. This increase is significant when compared with statistics from 10 years ago, when 62 percent had completed high school and 14 percent had completed 4 years of college.

(Continued)

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Education and Government Environments

- Educational attainment has a direct impact on the dynamics of the work force. The greater the amount of time and money invested in education and training, the more likely an individual is to remain in a particular occupation. Occupational tenure, defined as the cumulative number of years a person works in his or her current occupation regardless of number of employers, interruptions in employment, or time spent in other occupations, directly relates to the number of years of college.
- The degree of unemployment cyclical movement generally is smaller for individuals with more education.

In This Section

Tables E-1 through E-8 and G-1, and Figure 1 provide a general overview of education and government statistics. Areas covered in this section are number of schools, enrollment, expenditures, and government employment.

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Table E-1. Number of U.S. Schools, Student Enrollment, and Instructional Staff, 1987–1988

	Schools	Percent	Student Enrollment (Thousands)	Percent	Instructional Staff (Thousands)	Percent
Elementary						
Public	50,878	47.4%	19,617	34.5%	1,024	36.9%
Private	14,726	13.7	3,008	5.3	152	5.5
Secondary						
Public	23,377	21.8	19,961	35.1	807	29.1
Private	2,397	2.2	1,795	3.2	72	2.6
K-12						
Public	2,945	N/A	N/A	N/A	N/A	N/A
Private	4,334	N/A	N/A	N/A	N/A	N/A
Other						
Public	4,000	N/A	N/A	N/A	N/A	N/A
Private	1,242	N/A	N/A	N/A	N/A	N/A
Subtotal	103,899	96.8%	44,381	78.0%	2,055	74.0%
Higher Education						
Public	1,533	1.4%	9,706	17.1%	508	18.3%
Private	1,873	1.7	2,838	5.0	214	7.7
Subtotal	3,406	3.2%	12,544	22.0%	722	26.0%
Total	107,305	100.0%	56,925	100.0%	2,777	100.0%

Note: Instructional staff for elementary and secondary education represents teachers exclusively.
Other includes special schools; vocational schools; and adult education schools.
Columns may not add to totals shown because of rounding.
N/A = Not Available

Source: Market Data Retrieval

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Table E-2. Public School Systems and Student Enrollment by Enrollment-Size Class, 1986–1987

Enrollment Size	Number of Systems	Percent	Enrollment (Thousands)	Percent
1 to 299	4,071	25.9%	522	1.3%
300 to 599	2,257	14.4	987	2.5
600 to 999	1,754	11.2	1,371	3.5
1,000 to 2,499	3,504	22.3	5,691	14.7
2,500 to 4,999	1,823	11.6	6,363	16.4
5,000 to 9,999	915	5.8	6,382	16.5
10,000 to 24,999	447	2.8	6,606	17.1
25,000 or More	173	1.1	10,821	27.9
Size not reported	769	4.9	N/A	0
Total	15,713	100.0%	38,743	100.0%

Note: Enrollments and numbers of schools should be regarded as approximations only. These totals differ from those in other tables bcause this table represents data reported by school districts rather than by states.
Columns may not add to totals shown because of rounding.
N/A = Not Available

Source: U.S. Department of Education, National Center for Education Statistics

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Table E-3. Student Enrollment at U.S. Colleges and Universities, 1983 to 1993

	Total Enrollment	Four-Year Institutions	Two-Year Institutions	Percent Change
Actual				
1983	12,464	7,741	4,723	
1984	12,242	7,711	4,531	(1.8%)
1985	12,247	7,716	4,531	0
Estimated				
1986	12,398	7,754	4,644	1.2%
1987	12,544	7,816	4,728	1.2%
Projected				
1988	12,560	7,881	4,679	0.1%
1989	12,570	7,857	4,713	0.1%
1990	12,585	7,862	4,723	0.1%
1991	12,529	7,831	4,698	(1.2%)
1992	12,408	7,756	4,652	(2.1%)
1993	12,300	7,679	4,621	(2.3%)

Source: U.S. Department of Education, National Center for Education Statistics

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Table E-4. Student Enrollment from Kindergarten through 12th Grade for Regular Day Schools, 1985-1993 (Thousands of Students)

	Total Public and Private			Public			Private		
	K-12	K-8	9-12	K-12	K-8	9-12	K-12	K-8	9-12
Actual									
1985	44,509	30,649	13,860	39,509	27,049	12,460	5,000	3,600	1,400
1986	44,938	31,104	13,834	39,838	27,404	12,434	5,100	3,700	1,400
1987	45,547	32,101	13,446	40,200	27,983	12,217	5,347	4,118	1,229
Projected									
1988	45,522	32,475	13,047	40,280	28,439	11,841	5,242	4,036	1,206
1989	45,609	32,904	12,705	40,337	28,807	11,530	5,272	4,097	1,175
1990	46,092	33,542	12,550	40,752	29,366	11,386	5,340	4,176	1,164
1991	46,718	34,031	12,687	41,306	29,794	11,512	5,412	4,237	1,175
1992	47,366	34,470	12,896	41,879	30,178	11,701	5,487	4,292	1,195
1993	48,000	34,792	13,208	42,444	30,460	11,984	5,556	4,332	1,224

Source: National Center for Education Statistics

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Table E-5. Institutions of Higher Education by Control and Student Enrollment, 1985

Student Enrollment	All Institutions Number	All Institutions Enrollment (Thousands)	Universities Number	Universities Enrollment (Thousands)	Other Four-Year Colleges Number	Other Four-Year Colleges Enrollment (Thousands)	Two-Year Colleges Number	Two-Year Colleges Enrollment (Thousands)
Public Institutions								
Less than 200	3	1	0	0	0	0	3	1
200 to 499	35	13	0	0	9	3	26	10
500 to 999	125	94	0	0	29	23	96	72
1,000 to 2,499	404	684	0	0	93	166	311	518
2,500 to 4,999	329	1,183	1	5	107	395	221	784
5,000 to 9,999	293	2,055	7	59	125	866	161	1,131
10,000 to 19,999	211	2,879	33	496	90	1,200	88	1,183
20,000 to 29,999	66	1,571	31	753	15	352	20	466
30,000 or More	27	999	22	829	2	65	3	105
Subtotal	1,493	9,479	94	2,142	470	3,070	929	4,270
Private Institutions								
Less than 200	327	37	0	0	256	28	71	8
200 to 499	361	125	0	0	226	78	135	46
500 to 999	416	300	0	0	319	233	97	67
1,000 to 2,499	444	679	0	0	396	609	48	70
2,500 to 4,999	147	506	5	20	134	457	8	29
5,000 to 9,999	72	481	25	184	44	279	3	18
10,000 to 19,999	32	398	24	306	8	92	0	0
20,000 to 29,999	6	144	5	121	0	0	1	23
30,000 or More	3	98	3	98	0	0	0	0
Subtotal	1,808	2,768	62	729	1,383	1,776	363	261
Public and Private Institutions								
Less than 200	330	37	0	0	256	28	74	9
200 to 499	396	138	0	0	235	82	161	56
500 to 999	541	394	0	0	348	256	193	139
1,000 to 2,499	848	1,363	0	0	489	774	359	588
2,500 to 4,999	476	1,690	6	25	241	852	229	813
5,000 to 9,999	365	2,537	32	243	169	1,145	164	1,149
10,000 to 19,999	243	3,277	57	802	98	1,291	88	1,183
20,000 to 29,999	72	1,715	36	873	15	352	21	489
30,000 or More	30	1,096	25	927	2	65	3	105
Total	3,301	12,247	156	2,870	1,853	4,845	1,292	4,531

Source: National Center for Education Statistics

Table E-6. Expenditures of U.S. Schools, 1986 (Millions of Dollars)

Type of School	Expenditures	Percent
Public Elementary and Secondary		
Instruction	$ 89,559	61.1%
Support Services	51,905	35.4
Noninstruction	5,125	3.5
Total, Elementary and Secondary	$146,589	100.0%
Higher Education		
Public Institutions		
Instruction	$ 21,881	34.6%
Research	5,705	9.0
Public Service	2,516	4.0
Academic Support	4,694	7.4
Student Services	2,922	4.6
Institutional Support	5,667	9.0
Operation and Maintenance	5,177	8.2
Scholarships and Fellowships	1,576	2.5
Other	13,057	20.7
Subtotal	$ 63,195	100.0%
Private Institutions		
Instruction	$ 9,151	26.6%
Research	2,732	8.0
Public Service	604	1.8
Academic Support	1,974	5.7
Student Services	1,641	4.8
Institutional Support	3,684	10.7
Operation and Maintenance	2,428	7.1
Scholarships and Fellowships	2,584	7.5
Other	9,543	27.8
Subtotal	$ 34,341	100.0%
Total, Higher Education	$ 97,536	
Total	$244,125	

Source: National Center for Education Statistics

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Table E-7. Ratio of Students to Microcomputers in Public Schools

Grade Level	School Year 1983-84*	1984-85*	1985-86*	1986-87*	1987-88	1988-89
Elementary	112.4	79.3	55.3	43.7	36.8	32.4
Junior High	92.3	61.2	41.6	32.9	27.6	23.8
Senior High	76.6	51.5	37.9	31.1	26.3	22.8
	92.3	63.5	45.5	36.5	30.8	26.9

Note: Total represents all public schools including K-12, but excluding schools of special education. Data are preliminary.
*Data collection was limited to those schools with a microcomputer.

Source: Market Data Retrieval

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Table E-8. Installed Base of Microcomputers in Public Elementary and Secondary Schools by Manufacturer and School Year

Manufacturer	School Year 1983-84	1984-85	1985-86	1986-87	1987-88	1988-89
Apple	160,500	290,000	460,900	632,900	783,400	930,600
Radio Shack	68,200	112,000	139,000	155,800	171,900	178,200
Commodore	49,500	86,400	116,300	130,900	140,400	141,600
IBM	8,000	19,800	42,100	68,200	108,900	147,700
Other	38,000	61,800	84,300	94,100	107,600	124,900
Total	324,200	570,000	842,600	1,081,900	1,312,200	1,523,000

Source: Market Data Retrieval

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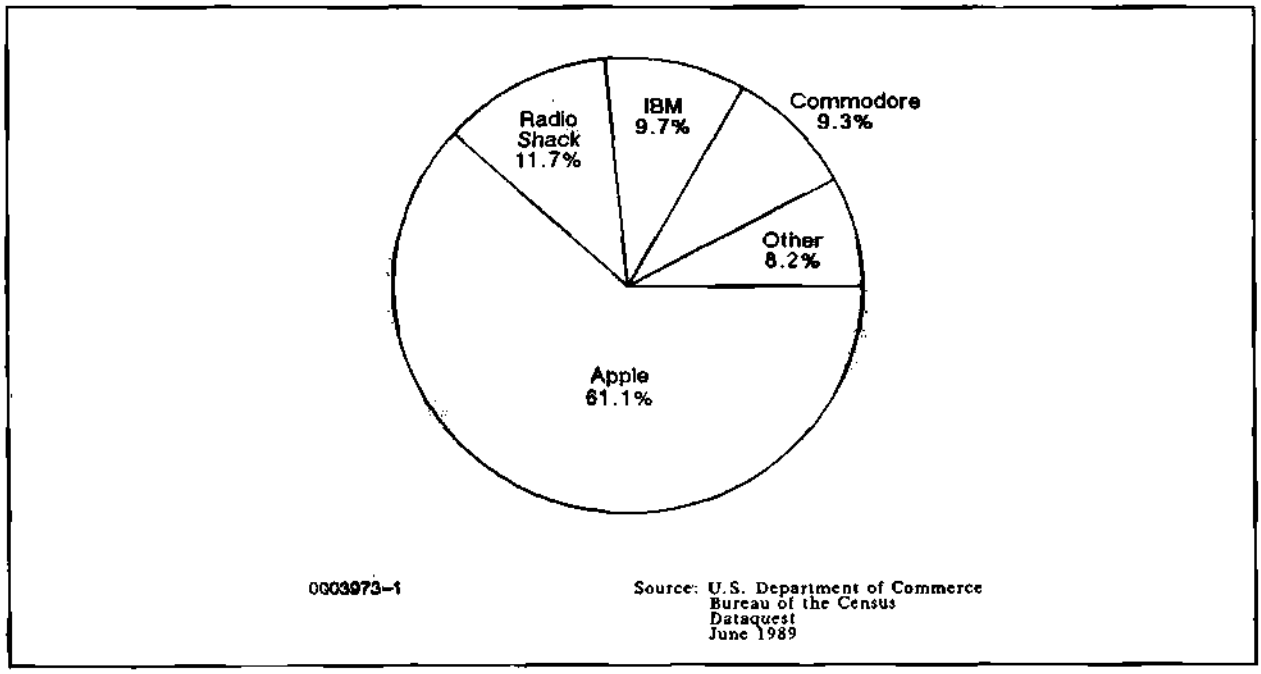

Figure 1. Installed Base of Microcomponents in School for School Year, 1988–1989

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Table G-1. Federal, State, and Local Government Employment by Industry Sector, 1987

SIC Category	Employees
Construction	185,960
Manufacturing	124,122
Transportation and Public Utilities	472,862
Retail Trade	79,915
Services	8,284,643
Hospitals	1,232,349
Social Services	273,218
Amusement and Recreation	134,970
Educational	5,376,420
Elementary and Secondary	4,964,208
Colleges and Universities	1,226,117
Public Administration	5,948,638
U.S. Postal Service	814,625
Total	15,910,765

Source: U.S. Department of Labor, Bureau of Labor Statistics

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Households and Population

The American family has endured challenges caused by a myriad of socioeconomic changes. Major alterations in household composition, financial demands of single-income families, and populations shifts from one geographic region to another are but a few of the changes to be considered when evaluating the complexity of the American market of the eighties.

- An increasing number of children under the age of 18 are likely to live in a household with only one parent. Of even greater significance is the fact that the marital status of these single parents is greatly different from those of a generation ago. In 1960, a single parent was likely to be widowed or separated. Today, 38.3 percent of single parents are divorced, with a noteworthy 30.5 percent never having been married.

- Women traditionally have lower occupational tenure than men. This lower occupational tenure may be attributed to the fact that many women interrupt their careers for family responsibilities. In addition, women continue to be underrepresented in higher paying positions in managerial, professional, and craft areas.

- Florida is the fourth most populous state, moving past Pennsylvania in state rankings.

- By the year 2010, the U.S. population is expected to increase by approximately 36 million persons. Three states, California, Texas, and Florida, will account for more than one-half of the increase in total population.

- Spurred on by increases in population in the states of Michigan and Ohio, the Midwest is showing moderate growth for the first time in this decade.

- Approximately one-half of the U.S. population lives in metropolitan areas of one million or more.

- The Midwest has been affected dramatically by the slow, but significant decline in the farm population. Approximately one-half of the nation's farms are located in the Midwest. Only 2 percent of the U.S. population live on farms, compared with 30 percent in 1920.

(Continued)

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Households and Population

- The median age of the farm population is 37.0 years, well above the median for nonfarm residents at 31.6 years.

In This Section

Figures 2, 3 and 4, and Tables H-1 through H-4 and P-1 through P-8 provide a detailed overview of the U.S. population and household demographics.

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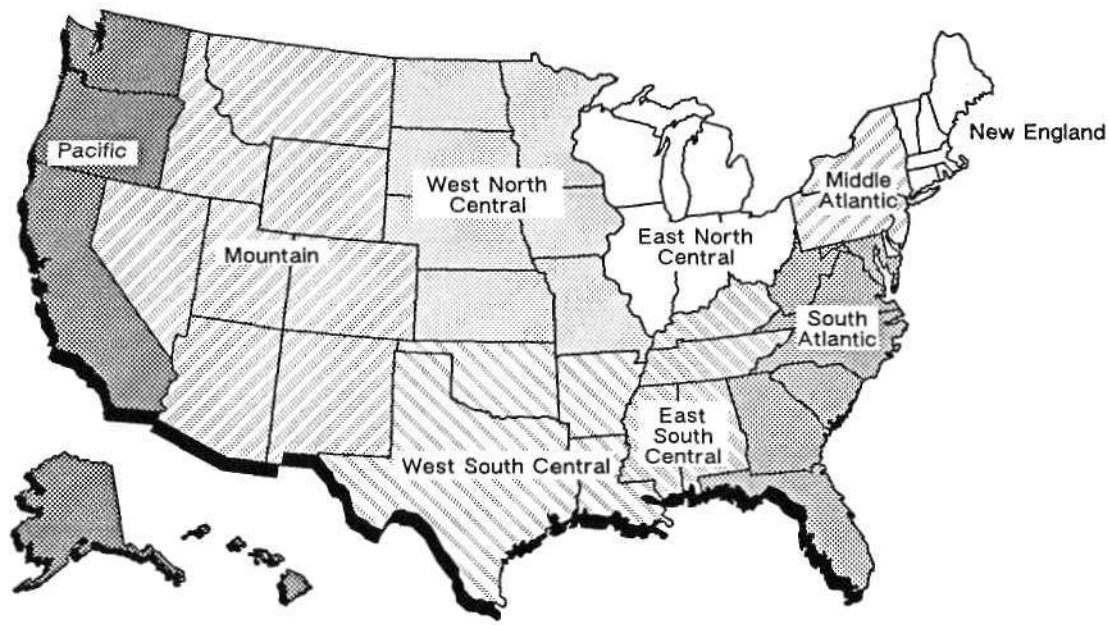

Northeast Region

New England Division
- Maine
- New Hampshire
- Vermont
- Massachusetts
- Rhode Island
- Connecticut

Middle Atlantic Division
- New York
- New Jersey
- Pennsylvania

Midwest Region

East North Central Division
- Ohio
- Indiana
- Illinois
- Michigan
- Wisconsin

West North Central Division
- Minnesota
- Iowa
- Missouri
- North Dakota
- South Dakota
- Nebraska
- Kansas

South Region

South Atlantic Division
- Delaware
- Maryland
- District of Columbia
- Virginia
- West Virginia
- North Carolina
- South Carolina
- Georgia
- Florida

East South Central Division
- Kentucky
- Tennessee
- Alabama
- Mississippi

West South Central Division
- Arkansas
- Louisiana
- Oklahoma
- Texas

West Region

Mountain Division
- Montana
- Idaho
- Wyoming
- Colorado
- New Mexico
- Arizona
- Utah
- Nevada

Pacific Division
- Washington
- Oregon
- California
- Alaska
- Hawaii

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Source: U.S. Department of Commerce
Bureau of the Census
Dataquest
June 1989

Figure 2. U.S. Census Regions and Divisions

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Table H-1. Number of U.S. Households and Average Household Size

	1983	1984	1985	1986	1987	1988	Est. 1990	Est. 1995
Households (Millions)	83.9	85.4	86.8	88.4	89.5	91.1	94.2	100.3
CAGR	N/A	1.8%	1.6%	1.8%	1.2%	1.8%	1.7%	1.3%
Persons per Household	2.73	2.71	2.69	2.67	2.66	2.64	2.60	N/A

N/A = Not Available

Source: U.S. Department of Commerce, Bureau of the Census

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Table H-2. Income Distribution of U.S. Households, 1987

Income	Households (Thousands)	Percent
Less than $5,000	6,271	6.9%
$ 5,000 to $9,999	10,446	11.5
$10,000 to $14,999	9,658	10.6
$15,000 to $19,999	9,136	10.0
$20,000 to $24,999	8,406	9.2
$25,000 to $29,999	7,647	8.4
$30,000 to $34,999	7,017	7.7
$35,000 to $39,999	6,198	6.8
$40,000 to $49,999	9,479	10.4
$50,000 to $74,999	11,109	12.2
$75,000 or More	5,700	6.3
Total	91,067	100.0%
Median Income	$25,986	
Mean Income	$32,144	

Source: U.S. Department of Commerce, Bureau of the Census

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Table H-3. Average U.S. Household Size

Type of Household	Persons per Household 1984	1986	1987	1988
All Households	2.71	2.67	2.66	2.64
Family Households*	3.28	3.28	3.22	3.21
Married Couple Households	3.32	3.32	3.27	3.25
Male Householder, No Wife	2.97	2.94	2.88	2.92
Female Householder, No Husband	3.11	3.11	3.09	3.08
Nonfamily Households**	1.21	1.21	1.22	1.22
Male Householder	1.33	1.33	1.34	1.33
Female Householder	1.12	1.13	1.13	1.13

*Family households consist of people related to the householder by birth, marriage, or adoption.
**Nonfamily households consist of a person living alone or a householder living with people unrelated by birth, marriage, or adoption.

Source: U.S. Department of Commerce, Bureau of the Census

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Table H-4. U.S. Households by Region (Thousands of Households)

Region	1987 Households	Percent	1988 Households	Percent	CAGR
Northeast	18,873	21.1%	19,137	21.0%	1.40%
Midwest	21,973	24.6	22,402	24.6	1.95%
South	30,620	34.2	31,048	34.1	1.40%
West	18,014	20.1	18,480	20.3	2.59%
Total	89,480	100.0%	91,067	100.0%	1.77%

Source: U.S. Department of Commerce, Bureau of the Census

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Table P-1. Population of the United States, 1980–2000 (Thousands of People)

	1980	1985	Actual 1986	1987	1988	1990	Estimated 1995	2000
Population	227,704	238,631	241,077	244,425	246,329	250,410	260,138	268,266
CAGR	N/A	0.94%	1.03%	1.39%	0.78%	0.82%	0.77%	0.62%

N/A = Not Available

Source: U.S. Department of Commerce, Bureau of the Census

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Table P-2. Distribution of U.S. Population by Age

Age	Actual 1988	Estimated 1990	1991	1993	2000
Less than 9 Years	14.7%	14.7%	14.6%	14.4%	13.0%
9-17 Years	14.2	13.8	13.7	13.8	14.3
18-24 Years	7.9	7.5	7.4	7.1	6.6
25-44 Years	32.2	32.7	32.8	32.3	30.2
45-64 Years	18.7	18.7	18.8	19.5	22.9
65 Years and Over	12.3	12.6	12.7	12.9	13.0
	100.0%	100.0%	100.0%	100.0%	100.0%

Source: U.S. Department of Commerce, Bureau of the Census

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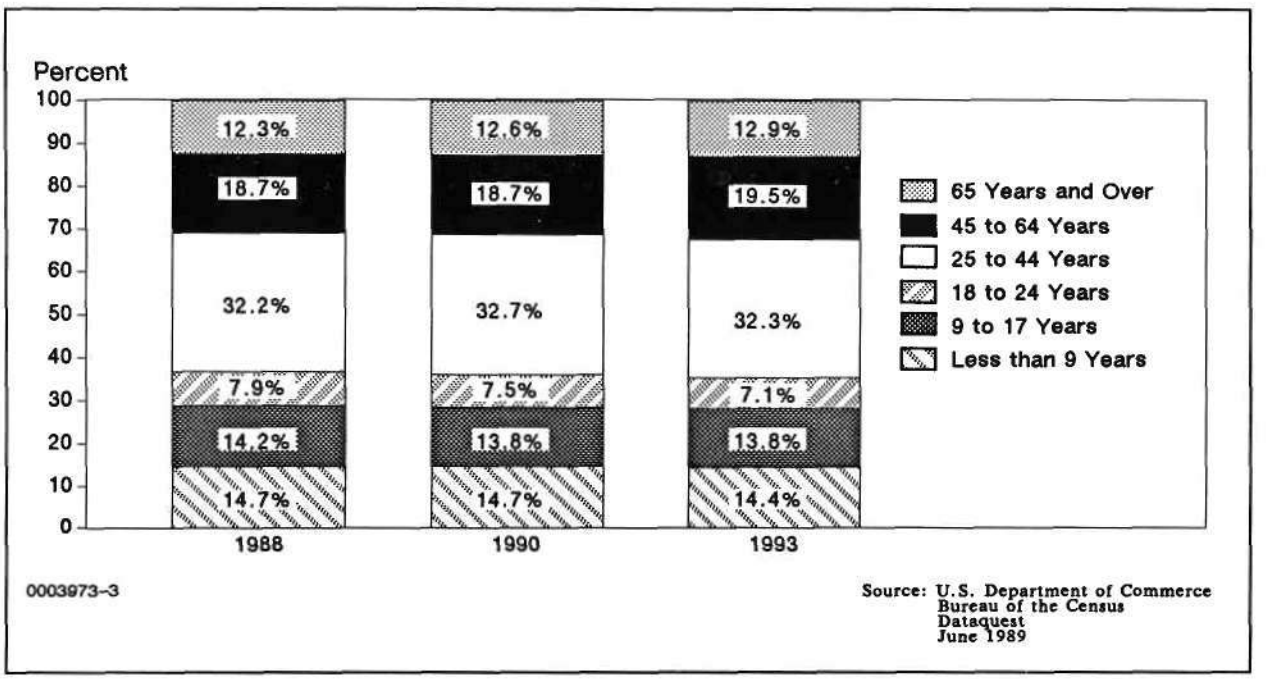

Figure 3. Distribution of U.S. Population by Age

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Table P-3. Top 50 Metropolitan Statistical Areas, 1987

Rank	Name	Population (Thousands)
1	New York - Northern New Jersey - Long Island, NY - NJ - CT	18,053,800
2	Los Angeles - Anaheim - Riverside, CA	13,470,900
3	Chicago - Gary - Lake County, IL - IN - WI	8,146,900
4	San Francisco - Oakland - San Jose, CA	5,953,100
5	Philadelphia - Wilmington - Trenton, PA - NJ - DE - MD	5,890,600
6	Detroit - Ann Arbor, MI	4,629,400
7	Boston - Lawrence - Salem, MA - NH	4,092,900
8	Dallas - Fort Worth, TX	3,724,900
9	Washington, DC - MD - VA	3,646,000
10	Houston - Galveston - Brazoria, TX	3,626,300
11	Miami - Fort Lauderdale, FL	2,954,100
12	Cleveland - Akron - Lorain, OH	2,766,900
13	Atlanta, GA	2,656,800
14	St. Louis, Mo - IL	2,458,100
15	Seattle - Tacoma, WA	2,340,600
16	Minneapolis - St. Paul, MN - WI	2,335,600
17	Baltimore, MD	2,302,900
18	Pittsburgh - Beaver Valley, PA	2,296,400
19	San Diego, CA	2,285,900
20	Tampa - St. Petersburg - Clearwater, FL	1,965,100
21	Phoenix, AZ	1,959,600
22	Denver - Boulder, CO	1,861,300
23	Cincinnati - Hamilton, OH - KY - IN	1,714,600
24	Milwaukee - Racine, WI	1,562,100
25	Kansas City, MO - Kansas City, KS	1,546,400
26	Portland - Vancouver, OR - WA	1,383,400
27	Norfolk - Virginia Beach - Newport News, VA	1,346,100
28	Sacramento, CA	1,336,500
29	New Orleans, LA	1,321,000
30	Columbus, OH	1,320,100
31	San Antonio, TX	1,306,700
32	Indianapolis, IN	1,228,600
33	Buffalo - Niagara Falls, NY	1,174,500
34	Providence - Pawtucket - Fall River, RI - MA	1,117,700
35	Charlotte - Gastonia - Rock Hill, NC	1,091,000
36	Hartford - New Britain - Middletown, CT	1,057,500
37	Salt Lake City - Ogden, UT	1,054,500
38	Rochester, NY	979,100
39	Oklahoma City, OK	975,000
40	Memphis, TN - AR - MS	971,900
41	Louisville, KY - IN	966,500
42	Nashville, TN	956,200
43	Dayton - Springfield, OH	938,800
44	Orlando, FL	934,700
45	Birmingham, AL	916,900
46	Greensboro - Winston-Salem - High Point, NC	915,700
47	Jacksonville, FL	878,200
48	Albany - Schenectady - Troy, NY	846,400
49	Honolulu, HI	830,600
50	Richmond - Petersburg, VA	825,300

Source: U.S. Department of Commerce, Bureau of the Census

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Table P-4. 100 Largest U.S. Cities, 1986

Rank	City	Population (Thousands)
1	New York, NY	7,263
2	Los Angeles, CA	3,259
3	Chicago, IL	3,010
4	Houston, TX	1,729
5	Philadelphia, PA	1,643
6	Detroit, MI	1,086
7	San Diego, CA	1,015
8	Dallas, TX	1,004
9	San Antonio, TX	914
10	Phoenix, AZ	894
11	Baltimore, MD	753
12	San Francisco, CA	749
13	Indianapolis, IN	720
14	San Jose, CA	712
15	Memphis, TN	653
16	Washington, DC	626
17	Jacksonville, FL	610
18	Milwaukee, WI	605
19	Boston, MA	574
20	Columbus, OH	566
21	New Orleans, LA	554
22	Cleveland, OH	536
23	Denver, CO	505
24	El Paso, TX	492
25	Seattle, WA	486
26	Nashville-Davidson, TN	474
27	Austin, TX	467
28	Oklahoma City, OK	446
29	Kansas City, MO	441
30	Fort Worth, TX	430
31	St. Louis, MO	426
32	Atlanta, GA	422
33	Long Beach, CA	396
34	Portland, OR	388
35	Pittsburgh, PA	388
36	Miami, FL	374
37	Tulsa, OK	374
38	Honolulu, HI	372
39	Cincinnati, OH	370
40	Albuquerque, NM	367
41	Tucson, AZ	359
42	Oakland, CA	357
43	Minneapolis, MN	357
44	Charlotte, NC	352
45	Omaha, NE	349
46	Toledo, OH	341
47	Virginia Beach, VA	333
48	Buffalo, NY	325
49	Sacramento, CA	324
50	Newark, NJ	316

(Continued)

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Table P-4 (Continued). 100 Largest U.S. Cities, 1986

Rank	City	Population (Thousands)
51	Wichita, KS	289
52	Louisville, KY	286
53	Fresno, CA	285
54	Tampa, FL	278
55	Birmingham, AL	278
56	Norfolk, VA	275
57	Colorado Springs, CO	273
58	Corpus Christi, TX	264
59	St. Paul, MN	264
60	Mesa, AZ	251
61	Arlington, TX	250
62	Baton Rouge, LA	241
63	Anaheim, CA	241
64	St. Petersburg, FL	239
65	Santa Ana, CA	237
66	Rochester, NY	236
67	Anchorage, AK	235
68	Akron, OH	222
69	Shreveport, LA	220
70	Jersey City, NJ	219
71	Aurora, CO	218
72	Richmond, VA	218
73	Lexington-Fayette, KY	213
74	Jackson, MS	208
75	Mobile, AL	203
76	Riverside, CA	197
77	Montgomery, AL	194
78	Des Moines, IA	192
79	Las Vegas, NV	192
80	Grand Rapids, MI	186
81	Lubbock, TX	186
82	Yonkers, NY	186
83	Huntington Beach, CA	184
84	Stockton, CA	183
85	Lincoln, NE	183
86	Little Rock, AR	181
87	Raleigh, NC	180
88	Columbus, GA	180
89	Dayton, OH	179
90	Greensboro, NC	177
91	Garland, TX	176
92	Madison, WI	176
93	Knoxville, TN	173
94	Fort Wayne, IN	173
95	Spokane, WA	173
96	Amarillo, TX	166
97	Huntsville, LA	163
98	Chattanooga, TN	162
99	Kansas City, KS	162
100	Hialeah, FL	162

Source: U.S. Department of Commerce, Bureau of the Census

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Table P-5. Summary of U.S. Civilian Population by Labor Force Status, 1988

	Population (Thousands)
Civilian Noninstitutional Population Under 16 Years	56,846
Civilian Noninstitutional Population 16 Years and Over	
Civilian Labor Force	
Employed	
Nonagricultural Industries	
Wage and Salary Workers	
Private Household Workers	1,153
Government	17,114
Other	84,754
Self-Employed Workers	8,519
Unpaid Family Workers	260
Subtotal	111,800
Agricultural	
Wage and Salary Workers	1,621
Self-Employed Workers	1,398
Unpaid Family Workers	150
Subtotal	3,169
Total	114,969
Unemployed	6,701
Total	121,670
Not in Labor Force	
Keeping House	28,036
Going to School	7,565
Unable to Work	3,194
Other Reasons	24,149
Subtotal	62,944
Total	184,614
Institutionalized Population	2,843
Civilian Population	244,303

Note: Civilian population figure does not include armed forces or institutionalized population under 16 years.

Source: U.S. Department of Labor, Bureau of Labor Statistics

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Table P-6. U.S. Census Regions and Divisions

Northeast Region	Midwest Region	South Region	West Region
New England Division	East North Central Division	South Atlantic Division	Mountain Division
Maine	Ohio	Delaware	Montana
New Hampshire	Indiana	Maryland	Idaho
Vermont	Illinois	District of Columbia	Wyoming
Massachusetts	Michigan	Virginia	Colorado
Rhode Island	Wisconsin	West Virginia	New Mexico
Connecticut		North Carolina	Arizona
	West North Central Division	South Carolina	Utah
Middle Atlantic Division	Minnesota	Georgia	Nevada
New York	Iowa	Florida	
New Jersey	Missouri		Pacific Division
Pennsylvania	North Dakota	East South Central Division	Washington
	South Dakota	Kentucky	Oregon
	Nebraska	Tennessee	California
	Kansas	Alabama	Alaska
		Mississippi	Hawaii
		West South Central Division	
		Arkansas	
		Louisiana	
		Oklahoma	
		Texas	

Source: U.S. Department of Commerce, Bureau of the Census

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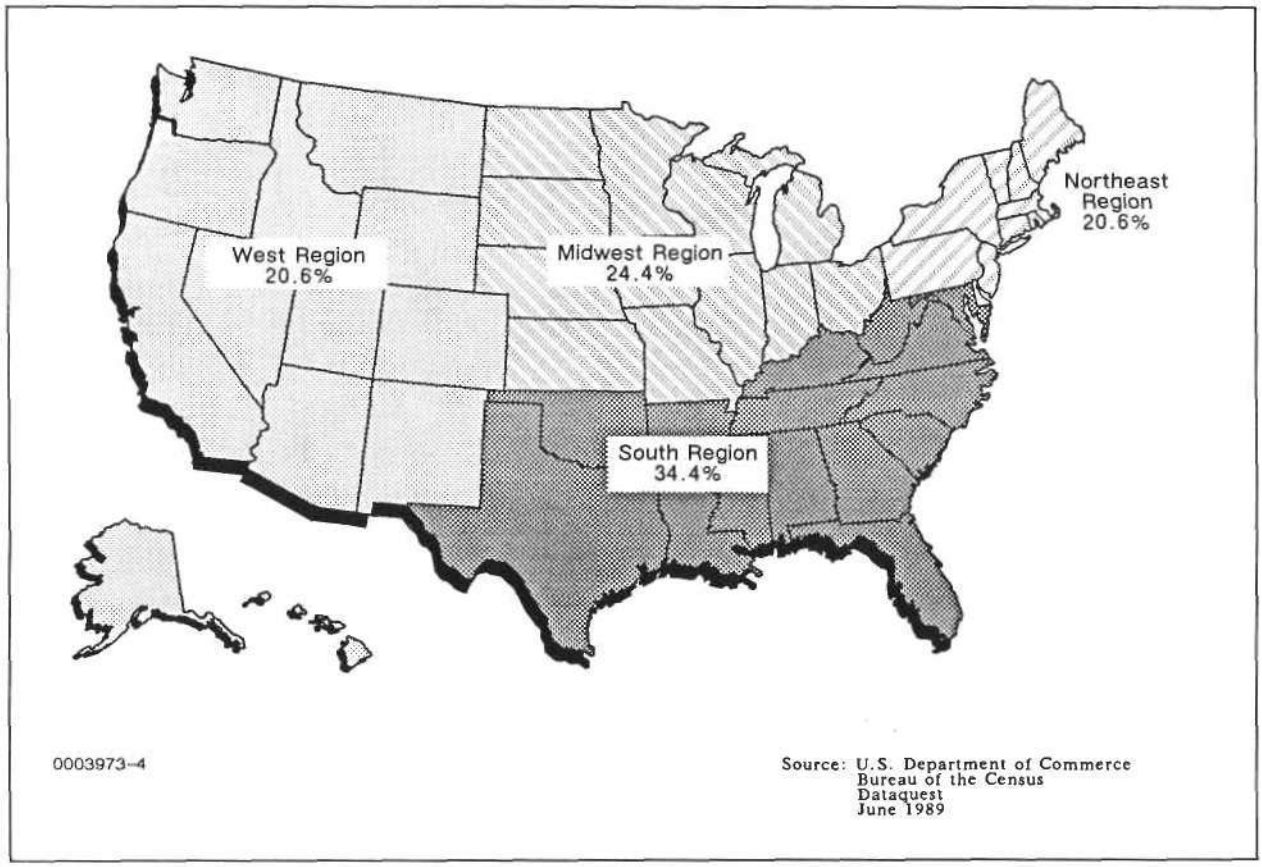

Figure 4. Distribution of U.S. Population by Census Divisions

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Table P-7. U.S. Population by Region and Division (Thousands)

	1988	Percent	1990	Percent
Northeast Region				
New England Division	12,991	5.3%	12,733	5.1%
Middle Atlantic Division	37,711	15.3	35,690	14.3
Subtotal	50,702	20.6%	48,423	19.4%
Midwest Region				
East North Central Division	42,209	17.1%	42,372	17.0%
West North Central Division	17,797	7.2	17,894	7.2
Subtotal	60,005	24.4%	60,266	24.2%
South Region				
South Atlantic Division	42,516	17.3%	43,144	17.3%
East South Central Division	15,377	6.2	16,121	6.5
West South Central Division	26,942	10.9	28,328	11.4
Subtotal	84,835	34.4%	87,593	35.1%
West Region				
Mountain Division	13,356	5.4%	15,404	6.2%
Pacific Division	37,430	15.2	37,516	15.1
Subtotal	50,787	20.6%	52,920	21.2%
Total	246,329	100.0%	249,202	100.0%

Note: Columns may not add to totals shown because of rounding.

Source: U.S. Department of Commerce, Bureau of the Census

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Table P-8. U.S. Population by Census Regions, Divisions, and States

Northeast Region	Population (Thousands)	Percent
New England Division		
Maine	1,208	0.5%
New Hampshire	1,087	0.4
Vermont	558	0.2
Massachusetts	5,902	2.4
Rhode Island	995	0.4
Connecticut	3,240	1.3
Subtotal	12,991	5.3%
Middle Atlantic Division		
New York	17,948	7.3%
New Jersey	7,738	3.1
Pennsylvania	12,027	4.9
Subtotal	37,714	15.3%
Midwest Region		
East North Central Division		
Ohio	10,879	4.4%
Indiana	5,568	2.3
Illinois	11,640	4.7
Michigan	9,260	3.8
Wisconsin	4,866	2.0
Subtotal	42,213	17.1%
West North Central Division		
Minnesota	4,316	1.8%
Iowa	2,840	1.2
Missouri	5,152	2.1
North Dakota	668	0.3
South Dakota	715	0.3
Nebraska	1,606	0.7
Kansas	2,501	1.0
Subtotal	17,798	7.2%

(Continued)

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Table P-8 (Continued). U.S. Population by Census Regions, Divisions, and States

South Region	Population (Thousands)	Percent
South Atlantic Division		
Delaware	661	0.3%
Maryland	4,632	1.9
District of Columbia	618	0.3
Virginia	6,028	2.4
West Virginia	1,880	0.8
North Carolina	6,503	2.6
South Carolina	3,478	1.4
Georgia	6,356	2.6
Florida	12,362	5.0
Subtotal	42,520	17.3%
East South Central Division		
Kentucky	3,735	1.5%
Tennessee	4,886	2.0
Alabama	4,111	1.7
Mississippi	2,626	1.1
Subtotal	15,358	6.2%
West South Central Division		
Arkansas	2,400	1.0%
Louisiana	4,418	1.8
Oklahoma	3,249	1.3
Texas	16,878	6.9
Subtotal	26,945	10.9%
West Region		
Mountain Division		
Montana	807	0.3%
Idaho	1,005	0.4
Wyoming	480	0.2
Colorado	3,308	1.3
New Mexico	1,510	0.6
Arizona	3,497	1.4
Utah	1,694	0.7
Nevada	1,056	0.4
Subtotal	13,357	5.4%

(Continued)

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Table P-8 (Continued). U.S. Population by Census Regions, Divisions, and States

West Region	Population (Thousands)	Percent
Pacific Division		
Washington	4,658	1.9%
Oregon	2,773	1.1
California	28,376	11.5
Alaska	525	0.2
Hawaii	1,100	0.4
Subtotal	37,433	15.2%
Total	246,329	100.0%

Note: Includes Armed Forces residing in each state.
Columns may not add to totals shown because of rounding.

Source: U.S. Department of Commerce, Bureau of the Census

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Business

The overall composition of U.S. businesses is relatively stable. Noteworthy changes in the types of businesses existing today are in the farm and services sectors. While the number of farms has been steadily declining, the number of new service-type businesses has been increasing.

- The overall number of business establishments has increased from 7.7 million in 1988 to nearly 8.0 million in 1989.
- The largest percentage of business establishments (77 percent) have less than 10 employees.
- Twenty-five percent of business establishments with $10 million or more in sales have 250 or more employees.
- Wholesale and retail trade accounts for 33 percent of all business establishments.
- According to a Dun & Bradstreet survey, the majority of companies allocate less than 10 percent of their capital spending budgets for computers and telecommunications. However, the survey also indicated that a greater number of companies are allocating between 11 and 50 percent of their budgets for computers and telecommunications equipment in 1989 as compared with 1988.
- The total number of available desktops (see Demographic Terms for definition) for 1989 is 69.8 million, and is expected to reach 73.4 million by 1993.
- The 1989 installed base of desktop information devices is approximately 36 million for a 51 percent market penetration. Dataquest estimates that the market penetration of desktop information devices will reach 64 percent by 1993.

In This Section

Tables B-1 through B-5 and Figures 5 through 9 provide a detailed overview of the overall composition of U.S. businesses.

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Table B-1. Distribution of U.S. Establishments by Detailed Industry Sector and Employment-Size Class, 1989

Industry Sector	Number of Establishments by Employment-Size Class								Percent of Total
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total	
Agriculture, Forestry, Fisheries									
Agricultural Production	187,077	10,282	5,739	1,534	1,049	77	23	205,780	2.6%
Agricultural Services	79,113	7,815	3,409	817	415	27	3	91,600	1.1
Forestry	2,656	304	179	52	55	7	3	3,256	0
Fishing, Hunting, and Trapping	2,178	179	122	38	10	0	0	2,527	0
Subtotal	271,024	18,580	9,450	2,441	1,529	111	28	303,163	3.8%
Percent	89.4%	6.1%	3.1%	0.8%	0.5%	0	0	100.0%	
Mining									
Oil and Gas Extraction	30,533	4,312	2,952	908	627	73	59	39,464	0.5%
Other Mining	7,701	1,834	1,578	531	613	88	50	12,395	0.2
Subtotal	38,234	6,146	4,530	1,439	1,240	161	109	51,859	0.7%
Percent	73.7%	11.9%	8.7%	2.8%	2.4%	0.3%	0.2%	100.0%	0
Contract Construction									
General Contractors and Builders	253,625	22,374	12,038	3,173	1,497	58	29	292,794	3.7%
Heavy Construction Contractors	30,283	6,335	5,141	1,842	1,173	62	37	44,873	0.6
Special Trade Contractors	388,318	44,195	25,541	6,342	2,617	62	15	467,090	5.9
Subtotal	672,226	72,904	42,720	11,357	5,287	182	81	804,757	10.1%
Percent	83.5%	9.1%	5.3%	1.4%	0.7%	0	0	100.0%	
Manufacturing									
Food and Kindred Products	14,111	4,830	5,085	2,907	3,695	459	206	31,293	0.4%
Tobacco Manufacturers	86	33	24	27	64	6	18	258	0
Textile Mill Products	5,495	1,558	1,899	1,124	1,728	294	97	12,195	0.2
Apparel and Other Textile Products	16,263	4,271	4,784	2,772	3,078	269	52	31,489	0.4
Lumber and Wood Products	25,855	6,044	4,862	2,067	1,607	75	36	40,546	0.5
Furniture and Fixtures	9,783	2,560	2,357	1,200	1,274	136	48	17,358	0.2
Paper and Allied Products	2,503	1,337	1,915	1,296	1,818	177	110	9,156	0.1
Printing and Publishing	67,141	13,340	9,424	3,704	2,968	270	179	97,026	1.2
Chemicals and Allied Products	10,416	3,600	3,628	1,864	1,897	317	231	21,953	0.3
Petroleum and Coal Products	1,853	578	590	250	310	51	54	3,686	0
Rubber and Miscellaneous Plastics Products	7,277	2,739	3,501	2,170	2,164	158	75	18,084	0.2
Leather and Leather Products	2,289	462	512	304	413	34	13	4,027	0.1
Stone, Clay, and Glass Products	10,995	3,374	3,093	1,213	1,148	122	48	19,993	0.3
Primary Metal Industries	4,034	1,767	2,132	1,151	1,583	209	146	11,022	0.1

(Continued)

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Table B-1 (Continued). Distribution of U.S. Establishments by Detailed Industry Sector and Employment-Size Class, 1989

Industry Sector	Number of Establishments by Employment-Size Class								Percent of Total
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total	
Manufacturing (Continued)									
Fabricated Metal Products	23,125	8,503	8,865	4,064	3,396	217	134	48,304	0.6%
Machinery, except Electrical	48,224	13,391	10,900	4,245	3,810	464	311	81,345	1.0
Electric and Electronic Equipment	13,450	4,544	4,878	2,705	3,780	599	478	30,434	0.4
Transportation Equipment	8,873	2,323	2,299	1,224	1,791	325	418	17,253	0.2
Instruments and Related Products	9,535	2,778	2,703	1,260	1,460	213	144	18,093	0.2
Miscellaneous Manufacturing Industries	29,038	5,104	3,768	1,544	1,190	91	33	40,768	0.5
Subtotal	310,346	83,136	77,219	37,091	39,174	4,486	2,831	554,283	7.0%
Percent	56.0%	15.0%	13.9%	6.7%	7.1%	0.8%	0.5%	100.0%	
Transportation, Communications, Utilities									
Railroad Transportation	1,440	373	350	191	317	75	61	2,807	
Local and Interurban Passenger Transportation	12,053	3,312	3,497	1,321	830	69	33	21,115	0.3%
Trucking and Warehousing	96,008	17,117	13,302	4,319	2,605	196	100	133,647	1.7
Water Transportation	8,105	1,286	1,020	338	275	16	13	11,053	0.1
Transportation by Air	9,466	1,821	1,737	783	540	69	90	14,506	0.2
Pipe Lines, except Natural Gas	412	185	147	59	32	3	0	838	0
Transportation Services	36,591	6,310	2,905	791	514	43	23	47,177	0.6
Communication									
Telephone	4,166	1,519	1,440	666	743	137	166	8,837	0.1
Telegraph	529	71	30	13	25	4	4	676	0
Broadcasting	3,975	3,430	2,853	798	486	16	12	11,570	0.1
Other	6,672	1,395	1,187	432	393	30	24	10,133	0.1
Electric, Gas, and Sanitary Services	15,680	4,433	4,288	1,929	1,720	261	191	28,502	0.4
Subtotal	195,097	41,252	32,756	11,640	8,480	919	717	290,861	3.7%
Percent	67.1%	14.2%	11.3%	4.0%	2.9%	0.3%	0.2%	100.0%	
Wholesale Trade									
Durable Goods	316,141	59,290	33,094	7,593	3,496	165	115	419,894	5.3%
Nondurable Goods	180,092	30,361	18,946	5,578	3,291	207	84	238,559	3.0
Subtotal	496,233	89,651	52,040	13,171	6,787	372	199	658,453	8.3%
Percent	75.4%	13.6%	7.9%	2.0%	1.0%	0.1%	0	100.0%	
Retail Trade									
Building Materials and Garden Supplies	91,063	12,170	5,762	1,413	512	12	8	110,940	1.4%
General Merchandise Stores									
Department Stores	2,960	1,458	2,488	3,137	7,043	266	83	17,435	0.2
Other	28,959	3,147	1,789	928	656	37	9	35,525	0.4

(Continued)

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Table B-1 (Continued). Distribution of U.S. Establishments by Detailed Industry Sector and Employment-Size Class, 1989

Industry Sector	Number of Establishments by Employment-Size Class								Percent of Total
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total	
Retail Trade (Continued)									
Food Stores									
Grocery Stores	121,907	15,442	13,875	7,832	4,535	87	32	163,710	2.1%
Other	53,464	6,749	2,650	354	112	10	0	63,339	0.8
Automotive Dealers and Service Stations									
New and Used Car Dealers	10,428	7,970	13,251	6,264	1,654	3	3	39,573	0.5
Used Car Dealers	29,698	980	239	41	6	0	0	30,964	0.4
Auto and Home Supply	46,158	6,163	1,383	155	70	7	1	53,937	0.7
Gasoline Service Stations	91,028	8,001	1,615	404	225	1	1	101,275	1.3
Other	21,843	2,549	789	129	30	0	0	25,340	0.3
Apparel and Accessory Stores	154,442	14,942	4,381	903	504	47	25	175,244	2.2
Furniture and Home Furnishings Stores									
Household Appliances Stores	21,103	1,995	861	132	47	4	5	24,147	0.3
Radio, TV, and Music Stores	28,074	2,110	692	137	77	8	1	31,099	0.4
Other	106,142	10,047	3,354	516	207	13	8	120,287	1.5
Eating and Drinking Places	230,733	70,995	67,502	19,675	3,538	119	43	392,605	4.9
Miscellaneous Retail									
Drug Stores	35,074	10,959	5,105	570	156	9	5	51,878	0.7
Liquor Stores	36,687	2,281	413	55	12	0	1	39,449	0.5
Used Merchandise Stores	44,468	1,618	733	175	49	0	2	47,045	0.6
Miscellaneous Shopping Goods	251,899	15,983	4,867	1,149	379	29	21	274,327	3.4
Nonstore Retailers	39,778	4,638	2,556	862	612	48	33	48,527	0.6
Other	104,438	9,099	3,395	587	249	14	6	117,788	1.5
Subtotal	1,550,346	209,296	137,700	45,418	20,673	714	287	1,964,434	24.7%
Percent	78.9%	10.7%	7.0%	2.3%	1.1%	0	0	100.0%	
Finance, Insurance, Real Estate									
Banking	26,167	17,968	10,943	3,043	1,836	231	248	60,436	0.8%
Credit Agencies, except Banks	44,084	11,002	6,692	2,102	1,575	148	70	65,673	0.8
Securities, Commodities Brokers, and Services	19,429	3,984	3,500	1,258	851	77	100	29,199	0.4
Insurance Carriers	17,303	5,148	5,384	2,393	2,713	437	431	33,809	0.4
Insurance Agents, Brokers and Services	93,732	9,700	5,624	1,541	990	89	30	111,706	1.4
Real Estate	281,427	28,002	16,100	3,780	1,838	84	39	331,270	4.2
Combined Real Estate, Insurance, etc.	5,337	710	502	152	94	15	3	6,813	0.1
Holding and Other Investment Offices	24,692	1,924	1,086	405	321	61	39	28,528	0.4
Subtotal	512,171	78,438	49,831	14,674	10,218	1,142	960	667,434	8.4%
Percent	76.7%	11.8%	7.5%	2.2%	1.5%	0.2%	0.1%	100.0%	

(Continued)

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Table B-1 (Continued). Distribution of U.S. Establishments by Detailed Industry Sector and Employment-Size Class, 1989

Industry Sector	Number of Establishments by Employment-Size Class								Percent of Total
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total	
Services									
Hotels and Other Lodging Places	51,250	7,371	6,762	3,508	3,517	276	115	72,799	0.9%
Personal Services									
Laundry, Cleaning, Garment Services	65,402	5,266	2,581	889	479	5	6	74,628	0.9
Photographic Studios	15,898	601	183	46	35	4	1	16,768	0.2
Beauty and Barber Shops	134,216	7,136	1,353	112	15	0	0	142,832	1.8
Shoe Repair, Hat Cleaning	7,449	49	7	0	1	0	0	7,506	0.1
Funeral Services	18,476	1,293	327	38	13	0	0	20,147	0.3
Miscellaneous Personal Services	26,849	3,206	1,560	354	179	15	7	32,170	0.4
Business Services									
Advertising	23,441	3,619	1,873	541	339	34	22	29,869	0.4
Credit Collection and Reporting	4,430	1,486	1,077	277	142	8	3	7,423	0.1
Mailing, Reproduction, Stenography	13,228	1,949	1,336	419	307	13	1	17,253	0.2
Services to Buildings	33,805	6,170	4,062	1,435	1,435	145	79	47,131	0.6
News Syndicates	479	89	89	32	28	4	2	723	0
Personnel Supply Services	15,686	2,679	1,433	567	794	108	71	21,338	0.3
Computer and Data Processing Service	34,947	7,152	4,768	1,863	1,568	177	118	50,593	0.6
Miscellaneous Business Services	279,567	30,933	19,058	6,347	5,553	591	413	342,462	4.3
Auto Repair, Services, Garages									
Auto Rental, without Drivers	16,811	2,290	1,396	394	195	7	7	21,100	0.3
Auto Parking	2,233	400	307	81	64	4	0	3,089	0
Auto Repair Shops	166,994	10,360	2,529	277	90	4	5	180,259	2.3
Auto Services, except Repair	18,986	2,199	1,188	121	28	3	4	22,529	0.3
Miscellaneous Repair Services	147,184	6,805	3,048	681	320	16	11	158,065	2.0
Motion Pictures	17,549	2,644	1,333	342	231	19	14	22,132	0.3
Amusement and Recreation Services	59,360	10,380	8,124	2,557	1,273	68	73	81,835	1.0
Health Services									
Offices of Physicians	148,531	13,385	4,839	842	418	17	13	168,045	2.1
Offices of Dentists	85,401	4,810	848	73	19	0	0	91,151	1.1
Offices of Osteopathic Physicians	5,750	341	61	8	4	0	1	6,165	0.1
Offices of Other Health Practitioners	42,532	1,460	430	111	117	3	2	44,655	0.6
Nursing and Personal Care Facilities	2,627	1,209	3,662	6,025	5,522	89	38	19,172	0.2
Hospitals	916	500	938	1,422	4,200	1,492	1,792	11,260	0.1
Medical and Dental Laboratories	10,948	1,839	1,107	349	229	16	12	14,500	0.2
Outpatient Care Facilities	8,133	3,622	3,159	1,149	741	42	51	16,897	0.2
Other Health and Allied Services	3,394	1,249	1,212	597	583	35	18	7,088	0.1
Legal Services	111,418	10,483	6,078	1,752	1,225	84	13	131,053	1.6

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Table B-1 (Continued). Distribution of U.S. Establishments by Detailed Industry Sector and Employment-Size Class, 1989

Industry Sector	Number of Establishments by Employment-Size Class								Percent of Total
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total	
Services (Continued)									
Educational Services									
Elementary and Secondary Schools								103,899	
Colleges and Universities								3,406	0
Libraries and Information Centers	15,090	504	658	293	195	22	10	16,772	0.2%
Correspondence and Vocational Schools	126	27	8	10	5	0	0	176	0
Other Schools and Educational Services	13,033	3,216	3,735	1,952	2,677	374	164	25,151	0.3
Social Services	81,062	17,595	11,643	3,837	2,612	151	67	116,967	1.5
Museums, Botanical, Zoological Gardens	2,169	455	438	148	114	4	0	3,328	0
Membership Organizations	133,848	19,500	13,279	4,190	2,159	176	88	173,240	2.2
Miscellaneous Services	105,048	17,811	11,045	3,453	2,526	230	186	140,299	1.8
Subtotal	1,924,266	212,083	127,534	47,092	39,952	4,236	3,407	2,465,875	30.9%
Percent	78.0%	9.8%	6.9%	2.3%	1.7%	0.2%	0.2%	100.0%	
Total	5,969,943	811,486	533,780	184,323	133,340	12,323	8,619	7,761,119	97.4%
Percent	76.9%	10.5%	6.9%	2.4%	1.7%	0.2%	0.1%	100.0%	
Other Government									
Federal								42,020	0.5%
Military								13,462	0.2
State								51,615	0.6
Local								99,175	1.2
Subtotal								206,272	2.6%
Percent								100.0%	
Total								7,967,391	100.0%
Percent								100.0%	

Note: Columns may not add to totals shown because of rounding.

Source: Dun's Marketing Services
Dataquest
June 1989

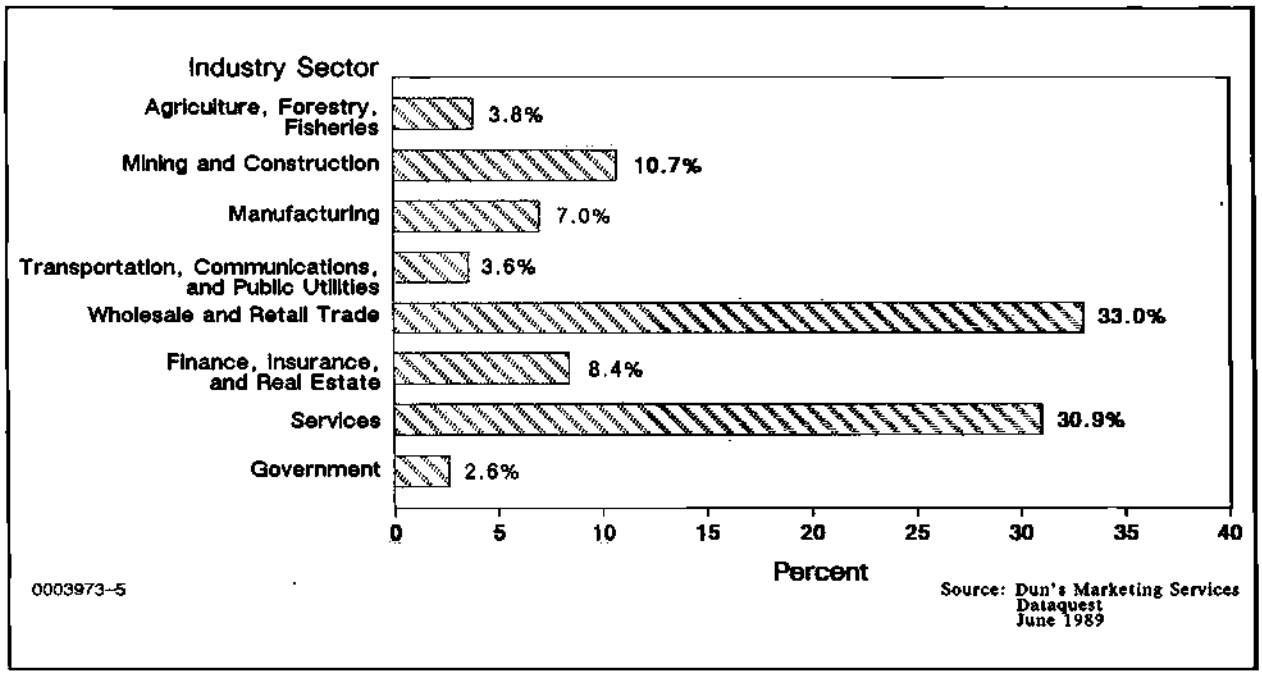

Figure 5. Percent Distribution of Business Establishments by Industry Sector

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Table B-2. *Distribution of* U.S. Establishments by State and Employment-Size Class

Census Regions and Divisions	Number of Establishments by Employment-Size Class							
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total
Northwest Region								
New England Division								
Maine	27,505	3,818	2,612	936	632	65	43	35,611
New Hampshire	24,965	3,889	2,826	958	755	88	42	33,523
Vermont	16,333	2,130	1,467	476	321	18	16	20,761
Massachusetts	135,704	21,948	16,320	5,957	4,836	513	395	185,674
Rhode Island	22,430	3,485	2,444	895	639	73	44	30,010
Connecticut	80,872	12,055	8,600	2,973	2,326	250	183	107,260
Subtotal	307,809	47,325	34,269	12,195	9,509	1,007	724	412,839
Middle Atlantic Division								
New York	420,452	58,916	41,318	14,420	10,760	1,098	891	547,854
New Jersey	182,155	28,420	20,465	7,326	5,754	550	445	245,114
Pennsylvania	263,932	36,314	25,073	9,812	7,535	826	508	343,999
Subtotal	866,538	123,649	86,856	31,558	24,049	2,474	1,844	1,136,967
Midwest Region								
East North Central Division								
Ohio	228,367	33,379	24,199	8,916	6,588	638	485	302,573
Indiana	117,471	16,223	11,738	4,255	3,316	306	215	153,523
Illinois	265,594	38,874	28,858	10,804	8,304	804	552	353,790
Michigan	202,622	29,355	20,891	7,414	5,000	414	359	266,054
Wisconsin	115,940	15,761	11,192	4,142	3,089	265	200	150,589
Subtotal	929,993	133,592	96,878	35,531	26,298	2,426	1,810	1,226,530
West North Central Division								
Minnesota	125,664	15,739	10,883	4,348	3,155	261	208	160,258
Iowa	104,220	11,127	7,550	2,698	1,823	165	107	127,691
Missouri	126,871	16,301	11,682	4,023	3,026	316	209	162,428
North Dakota	22,943	2,771	1,563	546	326	21	17	28,187
South Dakota	26,767	2,993	1,916	642	440	23	27	32,806
Nebraska	53,735	6,306	4,176	1,490	953	101	55	66,815
Kansas	80,517	9,971	6,511	2,231	1,422	121	86	100,859
Subtotal	540,716	65,208	44,280	15,979	11,145	1,007	709	679,044

(Continued)

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Table B-2 (Continued). Distribution of U.S. Establishments by State and Employment-Size Class

Census Regions and Divisions	Number of Establishments by Employment-Size Class							
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total
South Region								
South Atlantic Divison								
Delaware	14,352	2,196	1,484	527	427	60	37	19,083
Maryland	93,829	15,489	10,771	3,987	2,757	232	186	127,250
District of Columbia	18,157	3,794	2,908	1,044	819	130	157	27,009
Virginia	111,378	17,762	12,281	4,558	3,329	329	263	149,900
West Virginia	34,090	4,440	3,182	1,056	707	84	55	43,614
North Carolina	132,066	18,824	13,273	4,938	4,039	426	257	173,823
South Carolina	64,098	8,800	6,105	2,394	1,899	247	130	83,673
Georgia	134,049	19,635	13,403	5,166	3,756	368	232	176,608
Florida	298,988	42,456	27,686	10,220	6,864	546	370	387,131
Subtotal	307,241	40,404	28,144	10,305	7,803	938	490	395,324
East South Central Division								
Kentucky	82,570	9,403	6,740	2,502	1,679	184	105	103,185
Tennessee	96,093	13,932	9,442	3,427	2,630	328	184	126,036
Alabama	74,732	10,314	7,461	2,672	2,150	250	127	97,706
Mississippi	53,846	6,755	4,501	1,704	1,342	175	73	68,397
Subtotal	307,241	40,404	28,144	10,305	7,803	938	490	395,324
West South Central Division								
Arkansas	57,373	6,388	4,306	1,560	1,246	119	80	71,072
Louisiana	91,487	11,992	8,498	2,832	1,857	184	119	116,970
Oklahoma	92,256	10,520	6,893	2,375	1,505	128	92	113,769
Texas	541,684	74,785	49,558	17,646	12,227	1,071	844	697,815
Subtotal	782,800	103,686	69,255	24,413	16,834	1,503	1,134	999,626
West Region								
Mountain Division								
Montana	36,545	3,566	2,147	615	361	32	13	43,278
Idaho	34,354	3,918	2,343	807	472	58	41	41,993
Wyoming	21,239	2,220	1,415	456	291	23	12	25,656
Colorado	129,722	17,043	11,987	4,074	2,733	226	190	165,976
New Mexico	40,735	5,580	3,580	1,186	722	73	45	51,921
Arizona	110,534	17,501	12,115	4,201	2,810	251	171	147,583
Utah	38,691	5,257	3,546	1,283	854	76	77	49,784
Nevada	27,903	4,164	2,825	966	650	79	93	36,679
Subtotal	439,723	59,249	39,957	13,589	8,894	817	642	562,870

(Continued)

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Table B-2 (Continued). Distribution of U.S. Establishments by State and Employment-Size Class

Census Regions and Divisions	Number of Establishments by Employment-Size Class							
	0-9	10-19	20-49	50-99	100-499	500-999	1,000+	Total
Pacific Division								
Washington	138,530	17,283	11,884	4,230	2,446	219	179	174,771
Oregon	90,844	11,325	7,790	2,606	1,658	152	85	114,459
California	618,943	96,524	66,689	24,181	15,743	1,346	1,102	824,528
Alaska	14,949	1,716	998	312	246	24	15	18,260
Hawaii	21,012	3,241	2,105	805	553	57	36	27,810
Subtotal	884,277	130,090	89,466	32,134	20,646	1,798	1,417	1,159,828
Total	5,960,105	836,599	580,199	209,594	149,773	14,392	10,458	7,761,120

Note: Columns may not add to totals shown because of rounding.

Source: Dun's Marketing Services
Dataquest
June 1989

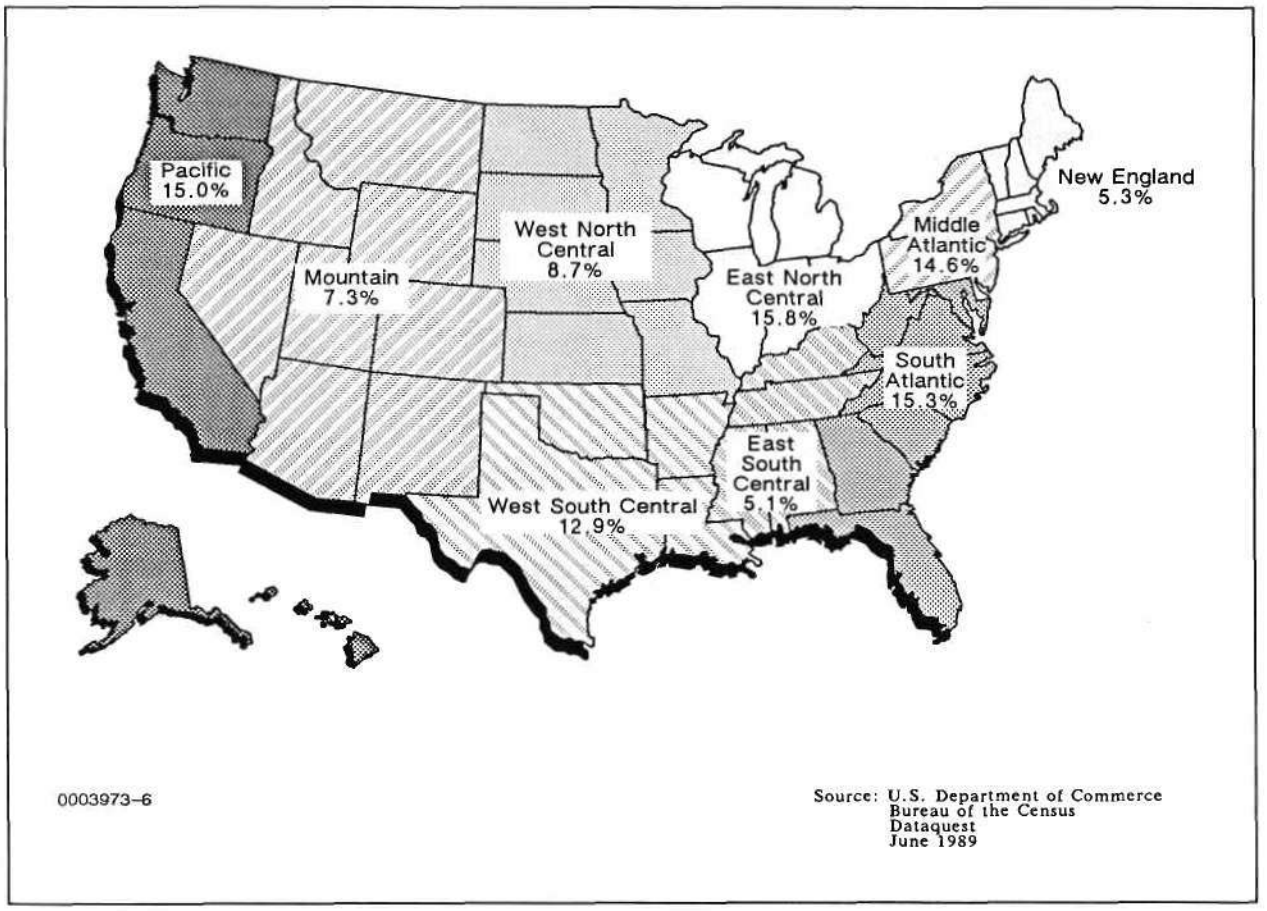

Figure 6. Distribution of Business Establishments by Census Divisions

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Table B-3. Establishment Data by Census Region, 1989

Census Regions and Divisions	Total	Percent of Total
Northwest Region		
New England Division	412,839	5.3%
Middle Atlantic Division	1,136,967	14.6
Midwest Region		
East North Central Division	1,226,530	15.8
West North Central Division	679,044	8.7
South Region		
South Atlantic Division	1,188,091	15.3
East South Central Division	395,324	5.1
West South Central Division	999,626	12.9
West Region		
Mountain Division	562,870	7.3
Pacific Division	1,159,828	14.9
Total	7,761,119	100.0%

Source: Dun's Martketing Services

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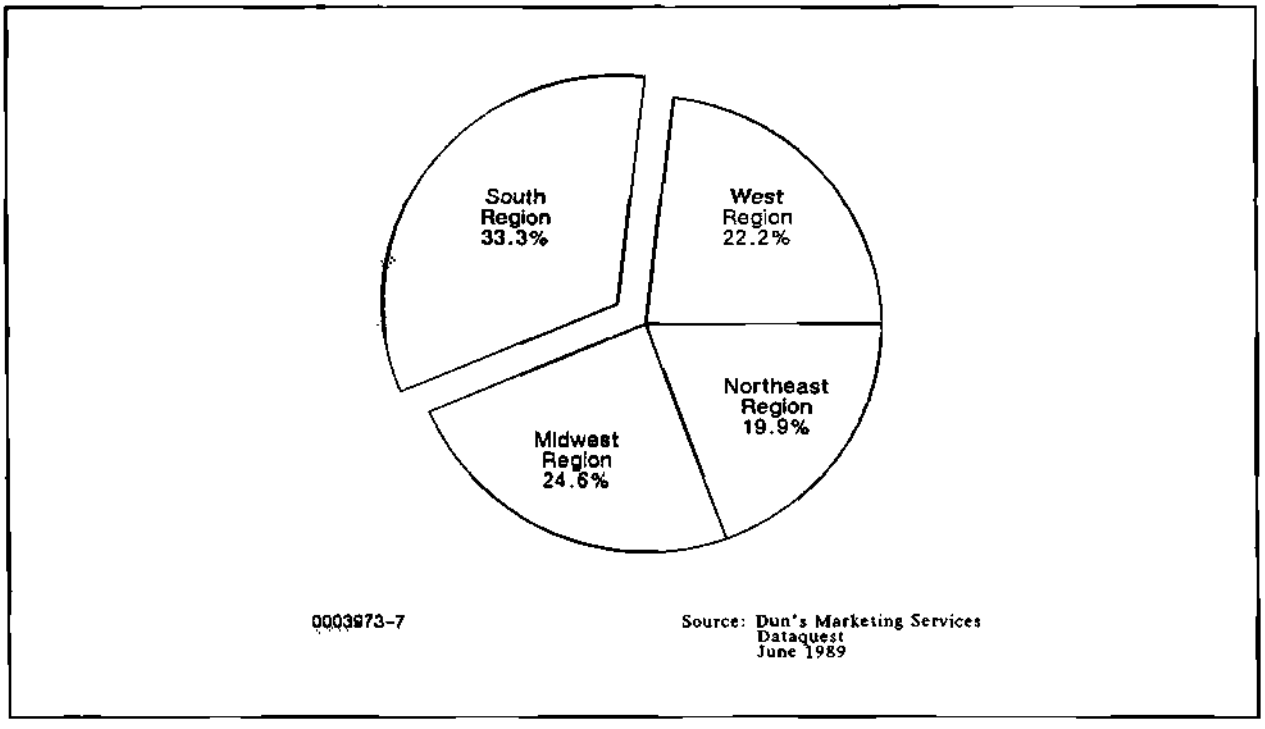

Figure 7. Distribution of Establishments by Census Regions

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Table B-4. Distribution of Establishments by Sales Volume and Industry Sector

Industry	Number of Establishments by Sales Volume							
	0-99.9m	100-499.9m	500-999.9m	1-4.9mm	5-9.9mm	10-49.9mm	50mm+	Total
Agriculture, Forestry, and Fisheries	71,476	172,066	36,408	19,455	2,039	1,289	288	302,961
Percent of Subtotal	23.6%	56.8%	12.0%	6.4%	0.7%	0.4%	0.1%	100.0%
Mining	3,661	17,049	14,669	12,821	1,276	1,755	596	51,826
Percent of Subtotal	7.1%	32.9%	28.3%	24.7%	2.5%	3.4%	1.1%	100.0%
Construction	201,507	373,163	92,830	110,646	14,486	10,164	1,425	804,222
Percent of Subtotal	25.1%	46.4%	11.5%	13.8%	1.8%	1.3%	0.2%	100.0%
Manufacturing	80,264	201,422	76,813	135,414	27,610	27,813	8,039	557,374
Percent of Subtotal	14.4%	36.1%	13.8%	24.3%	5.0%	5.0%	1.4%	100.0%
Transportation, Public Utilities, and Communication	54,732	105,301	30,427	41,742	7,906	6,950	2,569	249,627
Percent of Subtotal	21.9%	42.2%	12.2%	16.7%	3.2%	2.8%	1.0%	100.0%
Wholesale Trade	47,303	190,473	133,276	211,988	38,060	31,507	5,407	658,014
Percent of Subtotal	7.2%	28.9%	20.3%	32.2%	5.8%	4.8%	0.8%	100.0%
Retail Trade	428,840	1,017,583	260,358	207,069	24,342	22,822	3,295	1,964,308
Percent of Subtotal	21.8%	51.8%	13.3%	10.5%	1.2%	1.2%	0.2%	100.0%
Banking	1,585	4,269	4,586	23,883	9,391	10,629	6,052	60,395
Percent of Subtotal	2.6%	7.1%	7.6%	39.5%	15.5%	17.6%	10.0%	100.0%
Finance, Insurance, and Real Estate	149,616	206,206	72,842	108,572	24,612	31,032	13,712	606,591
Percent of Subtotal	24.7%	34.0%	12.0%	17.9%	4.1%	5.1%	2.3%	100.0%
Services	968,036	1,034,887	213,583	220,305	31,421	29,972	7,597	2,505,801
Percent of Subtotal	38.6%	41.3%	8.5%	8.8%	1.3%	1.2%	0.3%	100.0%
Total	2,007,019	3,322,418	935,791	1,091,896	181,141	173,934	48,919	7,761,119
Percent of Subtotal	25.9%	42.8%	12.1%	14.1%	2.3%	2.2%	0.6%	100.0%

Note: Columns may not add to totals shown because of rounding.

Source: Dun's Marketing Services
Dataquest
June 1989

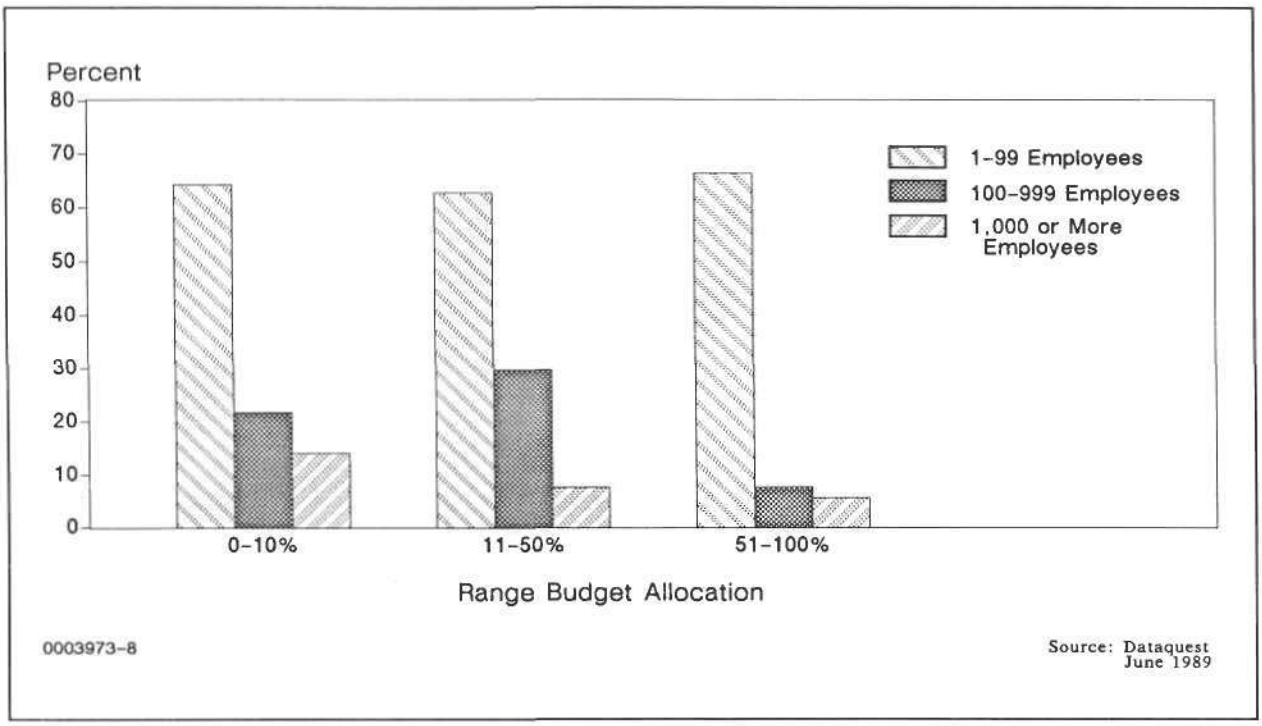

Figure 8. Percent Budget Allocation for Computers and Telecommunications Equipment by Size of Company

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Table B-5. Actual and Estimated Penetration of Desktop Information Devices in U.S. Business (Millions of Devices)

	1988	1989	1990	1991	1992	1993
Number of Desktops* in U.S. Business (Millions)	68.8	69.8	70.7	71.6	72.5	73.4
Installed Base of Desktop Devices (Millions)						
Display Terminals	15.2	16.4	17.2	17.6	17.8	17.5
Graphics Terminals	0.6	0.8	0.9	1.1	1.2	1.3
Office Personal Computers	15.8	18.5	21.1	23.7	26.1	28.4
Total Desktop Devices	31.6	35.7	39.2	42.4	45.1	47.2
Percent Penetration	45.9%	51.1%	55.4%	59.2%	62.2%	64.3%
Remaining Available Desktops (Millions)	37.2	34.1	31.5	29.2	27.4	26.2

*A desktop is defined as a potential location for a desktop information processing device.

Source: Dataquest June 1989

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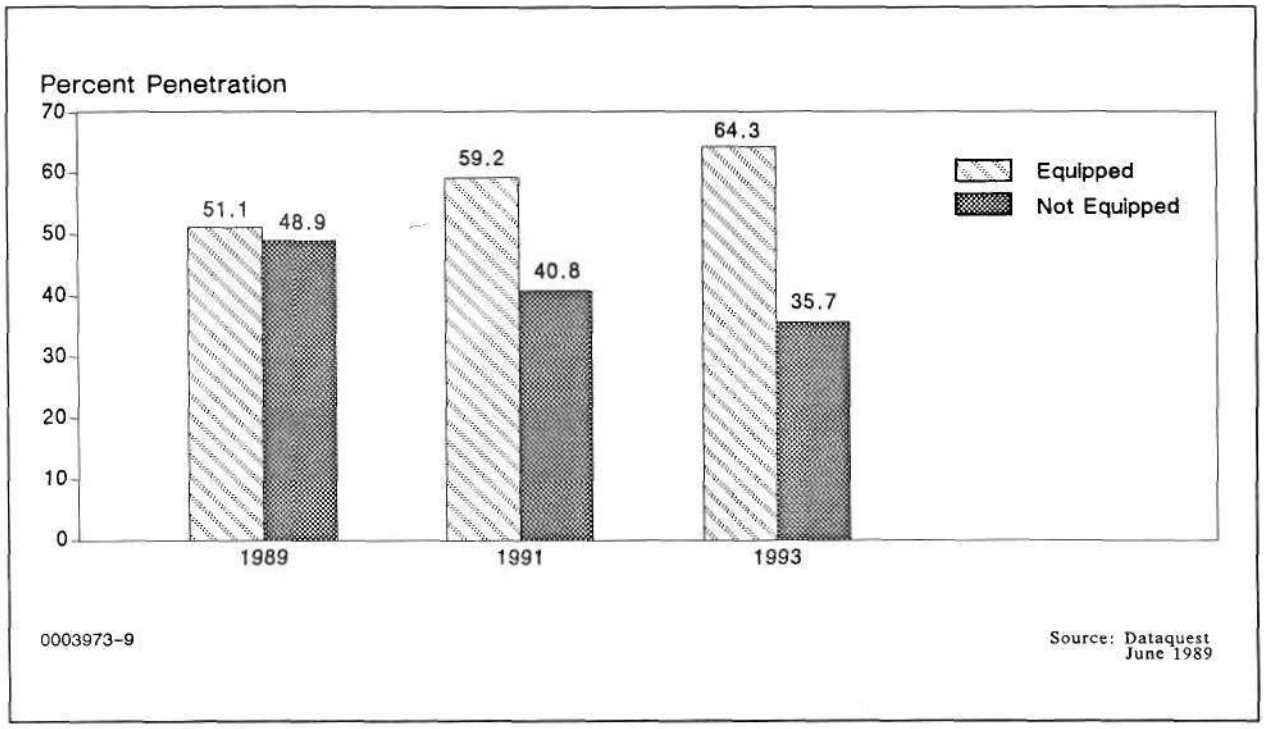

Figure 9. Penetration of Desktop Information Devices in U.S. Businesses

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Work Force

Parallel to changes in the home, today's work force also is in a major state of transformation. The influx of women and minorities into professional and managerial positions, albeit slow, is changing the complexion of the U.S. labor force.

- As women attain higher levels of education and are compelled by financial demands to work, the gap between male and female work participation is narrowing. Approximately 68 percent of married women and 80 percent of single women currently are participating in the labor force.
- In 1987, more than one-half of mothers with toddlers were in the labor force, exemplifying the magnitude of socioeconomic change occurring in the United States.
- The outgrowth of women's changing role in the work force has brought additional demands on corporations. Additional worker benefits such as child care, flexitime, and broad-range health plans are being instituted to accommodate two-career couples and single-parent families.
- Occupational tenure directly corresponds with age. The average occupational tenure for workers in the 16-24 age group is 1.9 years, while those 70 years and older have 21.9 years of tenure.
- Recently emerging job classifications, such as computer programmers, have a low occupational tenure primarily because of the large proportion of young people working in these occupations.
- Small companies (those with fewer than 19 employees) will provide about 32 percent of the new jobs in 1990 according to the 1989 Dun's 5000 Employment Outlook Survey (a Dun & Bradstreet survey). Conversely, companies with 10,000 or more employees are expected to contribute only 10 percent.
- The service sector will account for 68 percent of expected growth, while goods-producing industries will contribute about 28 percent of new jobs.

(Continued)

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Work Force

- Currently, there are approximately 69 million information workers. By 1993, Dataquest estimates that nearly 73 million will be users or potential users of automated desktop information devices.

In This Section

Tables W-1 through W-7 and Figures 10 through 13 highlight the work force by job classification, white collar segmentation, and employment growth by industry.

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Table W-1. Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1987 Number of Workers	1987 Percent of Total	1988 Number of Workers	1988 Percent of Total	1987-1988 Percent Change
Managerial and Professional Specialty	27,742	24.67%	29,190	25.39%	5.2%
Executive, Administrative, and Managerial	13,316	11.84	14,216	12.37	6.8%
Officials and Administrators, Public Administration	474	0.42	472	0.41	(0.4%)
Financial Managers	462	0.41	502	0.44	8.7%
Personnel and Labor Relations Managers	127	0.11	130	0.11	2.4%
Purchasing Managers	100	0.09	99	0.09	(1.0%)
Managers, Marketing, Advertising, and PR	444	0.39	482	0.42	8.6%
Administrators, Education and Related Fields	516	0.46	562	0.49	8.9%
Managers, Medicine and Health	154	0.14	163	0.14	5.8%
Managers, Properties and Real Estate	397	0.35	433	0.38	9.1%
Management-Related Occupations	3,577	3.18	3,772	3.28	5.5%
Accountants and Auditors	1,255	1.12	1,329	1.16	5.9%
Underwriters and Other Financial Officers	728	0.65	741	0.64	1.8%
Management Analysts	178	0.16	199	0.17	11.8%
Personnel, Training, Labor Relations	381	0.34	390	0.34	2.4%
Buyers, Wholesale and Retail except Farm Production	231	0.21	233	0.20	0.9%
Construction Inspectors	60	0.05	60	0.05	0
Inspectors and Compliance Officers, except Construction	183	0.16	194	0.17	6.0%
Other	561	0.50	626	0.50	11.6%
Executive, Administrative, and Managerial NEC	7,065	6.28	7,601	6.61	7.6%
Professional Specialty	14,426	12.83	14,974	13.02	3.8%
Architects	135	0.12	143	0.12	5.9%
Engineers	1,731	1.54	1,805	1.57	4.3%
Aerospace	104	0.09	115	0.10	10.6%
Chemical	63	0.06	65	0.06	3.2%
Civil	210	0.19	218	0.19	3.8%
Electrical and Electronic	545	0.48	573	0.50	5.1%
Industrial	221	0.20	221	0.19	0
Mechanical	277	0.25	297	0.26	7.2%
Engineers NEC	311	0.28	316	0.27	1.6%
Mathematical and Computer Scientists	685	0.61	732	0.64	6.9%
Computer Systems Analysts and Scientists	447	0.40	479	0.42	7.2%
Operations and Systems Researchers and Analysts	197	0.18	210	0.18	6.6%
Mathematical and Computer Scientists NEC	41	0.04	43	0.04	4.9%
Natural Scientists	388	0.35	395	0.34	1.8%
Chemists, except Biochemists	120	0.11	125	0.11	4.2%
Biological and Life Scientists	71	0.06	75	0.07	5.6%
Natural Scientists NEC	197	0.18	195	0.17	(1.0%)

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Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1987 Number of Workers	1987 Percent of Total	1988 Number of Workers	1988 Percent of Total	1987-1988 Percent Change
Health Diagnosing Occupations	793	0.71	818	0.71	3.2%
Physicians	514	0.45	541	0.47	5.3%
Dentists	160	0.14	152	0.13	(5.0%)
Health Diagnosing Occupations NEC	119	0.11	125	0.11	5.0%
Health Assessment and Treating Occupations	2,148	1.91	2,154	1.87	0.3%
Registered Nurses	1,588	1.41	1,559	1.36	(1.8%)
Pharmacists	153	0.14	168	0.15	9.8%
Dietitians	63	0.06	74	0.06	17.5%
Therapists	285	0.25	298	0.26	4.6%
Inhalation	60	0.05	65	0.06	8.3%
Physical	75	0.07	82	0.07	9.3%
Speech	73	0.06	66	0.06	(9.6%)
Other	77	0.07	85	0.07	10.4%
Health Assessment and Treating Occupations NEC	136	0.12	140	0.12	2.9%
Teachers, College and University	661	0.59	700	0.61	5.9%
Teachers, except College and University	3,587	3.19	3,773	3.28	5.2%
Prekindergarten and Kindergarten	389	0.35	393	0.34	1.0%
Elementary School	1,329	1.18	1,424	1.24	7.1%
Secondary School	1,172	1.04	1,187	1.03	1.3%
Special Education	216	0.19	246	0.21	13.9%
Teachers, NEC	480	0.43	524	0.46	9.2%
Counselors, Educational and Vocational	191	0.17	206	0.18	7.9%
Librarians, Archivists and Curators	219	0.19	219	0.19	0
Librarians	196	0.17	196	0.17	0
Librarians, Archivists and Curators NEC	23	0.02	23	0.02	0
Social Scientists and Urban Planners	316	0.28	343	0.30	8.5%
Economists	113	0.10	116	0.10	2.7%
Psychologists	171	0.15	196	0.17	14.6%
Social Scientists and Urban Planners NEC	32	0.03	31	0.03	(3.1%)
Social, Recreation, and Religious Workers	980	0.87	1,052	0.92	7.3%
Social Workers	507	0.45	537	0 47	5.9%
Recreation Workers	81	0.07	92	0.08	13.6%
Clergy	312	0.28	348	0.30	11.5%
Religious Workers NEC	82	0.07	75	0.07	(8.5%)
Lawyers and Judges	707	0.63	757	0.66	7.1%
Lawyers	672	0.60	724	0.63	7.7%
Lawyers and Judges NEC	35	0.03	33	0.03	(5.7%)
Writers, Artists, Entertainers, Athletes	1,858	1.65	1,855	1.61	(0.2%)
Authors	85	0.08	82	0.07	(3.5%)
Technical Writers	51	0.05	58	0.05	13.7%
Designers	531	0.47	510	0.44	(4.0%)

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Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1987 Number of Workers	1987 Percent of Total	1988 Number of Workers	1988 Percent of Total	1987-1988 Percent Change
Musicians and Composers	169	0.15	151	0.13	(10.7%)
Actors and Directors	88	0.08	100	0.09	13.6%
Painters, Sculptors, Craft Artists and Artist Printmakers	191	0.17	215	0.19	12.6%
Photographers	126	0.11	117	0.10	(7.1%)
Editors and Reporters	267	0.24	260	0.23	(2.6%)
Public Relations Specialists	142	0.13	151	0.13	6.3%
Announcers	59	0.05	52	0.05	(11.9%)
Athletes	69	0.06	73	0.06	5.8%
Writers, Artists, Entertainers, Athletes NEC	80	0.07	86	0.07	7.5%
Other Professional Specialty	27	0.02	22	0.02	(18.5%)
Technical, Sales, and Administrative Support	35,082	31.20	35,532	30.91	1.3%
Technicians and Related Support	3,346	2.98	3,521	3.06	5.2%
Health Technologists and Technicians	1,142	1.02	1,226	1.07	7.4%
Clinical Laboratory Technologists and Technicians	259	0.23	272	0.24	5.0%
Dental Hygienists	74	0.07	78	0.07	5.4%
Radiologic Technicians	127	0.11	133	0.12	4.7%
Licensed Practical Nurses	406	0.36	423	0.37	4.2%
Health Technicians and Related Support NEC	276	0.25	320	0.28	15.9%
Engineering and Related Technologists and Technicians	896	0.80	930	0.81	3.8%
Electrical and Electronic Technicians	305	0.27	322	0.28	5.6%
Drafting Occupations	283	0.25	290	0.25	2.5%
Surveying and Mapping Technicians	81	0.07	78	0.07	(3.7%)
Engineering and Related Technologists and Technicians NEC	227	0.20	240	0.21	5.7%
Science Technicians	204	0.18	216	0.19	5.9%
Biological Technicians	59	0.05	55	0.05	(6.8%)
Chemical Technicians	73	0.06	81	0.07	11.0%
Science Technicians NEC	72	0.06	80	0.07	11.1%
Technicians, except Health, Engineering, and Science	1,104	0.98	1,149	1.00	4.1%
Airplane Pilots and Navigators	78	0.07	88	0.08	12.8%
Computer Programmers	527	0.47	570	0.50	8.2%
Legal Assistants	189	0.17	203	0.18	7.4%
Technicians, except Health, Engineering, and Science NEC	310	0.28	288	0.25	(7.1%)
Sales Occupations	13,480	11.99	13,747	11.96	2.0%
Supervisors and Proprietors	3,572	3.18	3,658	3.18	2.4%
Sales Representatives, Finance and Business Services	2,330	2.07	2,410	2.10	3.4%
Insurance Sales	544	0.48	545	0.47	0.2%
Real Estate Sales	778	0.69	792	0.69	1.8%
Securities and Financial Services Sales	319	0.28	319	0.28	0
Advertising and Related Sales	148	0.13	168	0.15	13.5%
Sales Occupations, other Business Services	542	0.48	585	0.51	7.9%

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Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1987 Number of Workers	1987 Percent of Total	1988 Number of Workers	1988 Percent of Total	1987-1988 Percent Change
Sales Representatives, Commodities, except Retail	1,544	1.37	1,551	1.35	0.5%
Sales Workers, Retail and Personal Services	5,973	5.31	6,068	5.28	1.6%
Sales Workers, Motor Vehicles and Boats	304	0.27	294	0.26	(3.3%)
Sales Workers, Apparel	450	0.40	462	0.40	2.7%
Sales Workers, Shoes	120	0.11	112	0.10	(6.7%)
Sales Workers, Furniture and Home Furnishings	167	0.15	166	0.14	(0.6%)
Sales Workers, Radio, Television, Hi-Fi, and Appliances	187	0.17	180	0.16	(3.7%)
Sales Workers, Hardware, and Building Supplies	209	0.19	198	0.17	(5.3%)
Sales Workers, Parts	157	0.14	169	0.15	7.6%
Sales Workers, Other Commodities	1,514	1.35	1,537	1.34	1.5%
Sales Counter Clerks	174	0.15	189	0.16	8.6%
Cashiers	2,286	2.03	2,337	2.03	2.2%
Street and Door-to-Door Sales Workers	303	0.27	318	0.28	5.0%
News Vendors	100	0.09	108	0.09	8.0%
Sales-Related Occupations	60	0.05	59	0.05	(1.7%)
Administrative Support, Including Clerical	18,256	16.24	18,264	15.89	0
Supervisors	723	0.64	764	0.66	5.7%
General Office	439	0.39	458	0.40	4.3%
Financial Records Processing	79	0.07	91	0.08	15.2%
Supervisors, Distributing, Scheduling, and Adjusting	159	0.14	165	0.14	3.8%
Supervisors NEC	46	0.04	50	0.04	8.7%
Computer Equipment Operators	914	0.81	869	0.76	(4.9%)
Computer Operators	911	0.81	865	0.75	(5.0%)
Computer Equipment Operators NEC	3	0.00	4	0.00	33.3%
Secretaries, Stenographers, and Typists	5,004	4.45	4,876	4.24	(2.6%)
Secretaries	4,107	3.65	4,030	3.51	(1.9%)
Stenographers	54	0.05	48	0.04	(11.1%)
Typists	843	0.75	798	0.69	(5.3%)
Information Clerks	1,371	1.22	1,479	1.29	7.9%
Interviewers	157	0.14	163	0.14	3.8%
Hotel Clerks	90	0.08	103	0.09	14.4%
Transportation Ticket and Reservation Agents	111	0.10	114	0.10	2.7%
Receptionists	766	0.68	848	0.74	10.7%
Information Clerks NEC	247	0.22	251	0.22	1.6%
Records Processing Occupations, except Financial	844	0.75	827	0.72	(2.0%)
Order Clerks	189	0.17	197	0.17	4.2%
Personnel Clerks, except Payroll and Timekeeping	70	0.06	65	0.06	(7.1%)
Library Clerks	146	0.13	143	0.12	(2.1%)
File Clerks	281	0.25	271	0.24	(3.6%)
Records Clerks	135	0.12	132	0.11	(2.2%)
Records Processing Occupations, except Financial	23	0.02	19	0.02	(17.4%)

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Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1987 Number of Workers	1987 Percent of Total	1988 Number of Workers	1988 Percent of Total	1987-1988 Percent Change
Financial Records Processing	2,469	2.20	2,414	2.10	(2.2%)
Bookkeepers, Accounting, and Auditing Clerks	2,004	1.78	1,970	1.71	(1.7%)
Payroll and Timekeeping Clerks	177	0.16	173	0.15	(2.3%)
Billing Clerks	171	0.15	157	0.14	(8.2%)
Cost and Rate Clerks	84	0.07	75	0.07	(10.7%)
Financial Records Processing NEC	33	0.03	39	0.03	18.2%
Duplicating, Mail, and Other Office Machine Operators	69	0.06	68	0.06	(1.4%)
Communications Equipment Operators	225	0.20	218	0.19	(3.1%)
Telephone Operators	218	0.19	210	0.18	(3.7%)
Communications Equipment Operators NEC	7	0.01	8	0.01	14.3%
Mail and Message Distributing Occupations	961	0.85	936	0.81	(2.6%)
Postal Clerks, except Mail Carriers	315	0.28	313	0.27	(0.6%)
Mail Carriers, Postal Service	321	0.29	320	0.28	(0.3%)
Mail Clerks, except Postal Service	172	0.15	163	0.14	(5.2%)
Messengers	153	0.14	141	0.12	(7.8%)
Material Recording, Scheduling, and Distributing	1,709	1.52	1,681	1.46	(1.6%)
Dispatchers	197	0.18	171	0.15	(13.2%)
Production Coordinators	192	0.17	192	0.17	0
Traffic, Shipping and Receiving Clerks	483	0.43	521	0.45	7.9%
Stock and Inventory Clerks	580	0.52	559	0.49	(3.6%)
Weighers, Measurers, and Checkers	72	0.06	72	0.06	0
Expediters	109	0.10	95	0.08	(12.8%)
Material Clerks NEC	76	0.07	71	0.06	(6.6%)
Adjusters and Investigators	897	0.80	949	0.83	5.8%
Insurance Adjusters, Examiners, and Investigators	257	0.23	287	0.25	11.7%
Investigators and Adjusters, except Insurance	442	0.39	466	0.41	5.4%
Eligibility Clerks, Social Welfare	67	0.06	65	0.06	(3.0%)
Bill and Account Collectors	131	0.12	130	0.11	(0.8%)
Miscellaneous Administrative Support	3,071	2.73	3,183	2.77	3.6%
General Office Clerks	803	0.71	833	0.72	3.7%
Bank Tellers	467	0.42	478	0.42	2.4%
Data Entry Keyers	361	0.32	362	0.31	0.3%
Statistical Clerks	98	0.09	85	0.07	(13.3%)
Teachers' Aides	390	0.35	423	0.37	8.5%
Miscellaneous Administrative Support NEC	952	0.85	1,002	0.87	5.3%
Service Occupations	15,054	13.39	15,332	13.34	1.8%
Private Household	934	0.83	909	0.79	(2.7%)
Child Care Workers	405	0.36	378	0.33	(6.7%)
Cleaners and Servants	472	0.42	476	0.41	0.8%
Private Household NEC	57	0.05	55	0.05	(3.5%)

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Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1987 Number of Workers	1987 Percent of Total	1988 Number of Workers	1988 Percent of Total	1987-1988 Percent Change
Protective Service	1,907	1.70	1,944	1.69	1.9%
Supervisors, Protective Services	161	0.14	174	0.15	8.1%
Supervisors, Police and Detectives	83	0.07	93	0.08	12.0%
Supervisors, Protective Services NEC	78	0.07	81	0.07	3.8%
Firefighting and Fire Prevention	221	0.20	218	0.19	(1.4%)
Firefighting Occupations	204	0.18	195	0.17	(4.4%)
Firefighting and Fire Prevention NEC	17	0.02	23	0.02	35.3%
Police and Detectives	717	0.64	755	0.66	5.3%
Police and Detectives, Public Service	438	0.39	427	0.37	(2.5%)
Sheriffs, Bailiffs, and Other Law Enforcement Officers	104	0.09	111	0.10	6.7%
Correctional Institution Officers	175	0.16	217	0.19	24.0%
Guards	809	0.72	796	0.69	(1.6%)
Guards and Police, except Public Service	689	0.61	675	0.59	(2.0%)
Guards, NEC	120	0.11	121	0.11	0.8%
Service Occupations, except Private Household, Protective	12,213	10.86	12,479	10.85	2.2%
Food Preparation and Service Occupations	5,204	4.63	5,182	4.51	(0.4%)
Supervisors	301	0.27	325	0.28	8.0%
Bartenders	326	0.29	324	0.28	(0.6%)
Waiters and Waitresses	1,383	1.23	1,363	1.19	(1.4%)
Cooks, except Short Order	1,627	1.45	1,634	1.42	0.4%
Short-Order Cooks	93	0.08	95	0.08	2.2%
Food Counter, Fountain, and Related Occupations	359	0.32	325	0.28	(9.5%)
Kitchen Workers, Food Preparation	130	0.12	132	0.11	1.5%
Waiters' and Waitresses' Assistants	325	0.29	339	0.29	4.3%
Miscellaneous Food Preparation	660	0.59	645	0.56	(2.3%)
Health Service Occupations	1,873	1.67	1,977	1.72	5.6%
Dental Assistants	169	0.15	165	0.14	(2.4%)
Health Aides, except Nursing	380	0.34	407	0.35	7.1%
Nursing Aides, Orderlies, and Attendants	1,324	1.18	1,404	1.22	6.0%
Cleaning and Building Service Occupations	2,886	2.57	2,994	2.60	3.7%
Supervisors	161	0.14	159	0.14	(1.2%)
Maids and Housemen	602	0.54	644	0.56	7.0%
Janitors and Cleaners	2,059	1.83	2,133	1.86	3.6%
Cleaning and Building Service Occupations, NEC	64	0.06	58	0.05	(9.4%)
Personal Service Occupations	2,249	2.00	2,327	2.02	3.5%
Barbers	90	0.08	94	0.08	4.4%
Hairdressers and Cosmetologists	743	0.66	769	0.67	3.5%
Attendants, Amusement and Recreation Facilities	128	0.11	130	0.11	1.6%
Public Transportation Attendants	76	0.07	77	0.07	1.3%

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Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1987 Number of Workers	1987 Percent of Total	1988 Number of Workers	1988 Percent of Total	1987-1988 Percent Change
Welfare Service Aides	104	0.09	92	0.08	(11.5%)
Child Care Workers	827	0.74	853	0.74	3.1%
Personal Service Occupations, NEC	281	0.25	312	0.27	11.0%
Precision Production, Craft, and Repair	13,568	12.07	13,664	11.88	0.7%
Mechanics and Repairers	4,445	3.95	4,454	3.87	0.2%
Supervisors	259	0.23	256	0.22	(1.2%)
Mechanics and Repairers, except Supervisors	4,186	3.72	4,198	3.65	0.3%
Vehicle and Mobile Equipment Mechanics and Repairers	1,779	1.58	1,811	1.58	1.8%
Automobile Mechanics	871	0.77	879	0.76	0.9%
Bus, Truck, and Stationary Engine Mechanics	329	0.29	325	0.28	(1.2%)
Aircraft Engine Mechanics	117	0.10	131	0.11	12.0%
Small-Engine Repairers	70	0.06	70	0.06	0
Automobile Body and Related Repairers	184	0.16	194	0.17	5.4%
Heavy Equipment Mechanics	157	0.14	159	0.14	1.3%
Vehicle and Mobile Equipment	51	0.05	53	0.05	3.9%
Industrial Machinery Repairers	542	0.48	547	0.48	0.9%
Electrical and Electronic Equipment Repairers	685	0.61	677	0.59	(1.2%)
Electronic Repairers, Communications and Industrial Equipment	171	0.15	165	0.14	(3.5%)
Data Processing Equipment Repairers	134	0.12	140	0.12	4.5%
Telephone Line Installers and Repairers	57	0.05	61	0.05	7.0%
Telephone Installers and Repairers	215	0.19	202	0.18	(6.0%)
Electrical and Electronic Equipment NEC	108	0.10	109	0.09	0.9%
Heating, Air Conditioning, and Refrigeration Mechanics	264	0.23	262	0.23	(0.8%)
Miscellaneous Mechanics and Repairers	880	0.78	874	0.76	(0.7%)
Office Machine Repairers	64	0.06	60	0.05	(6.3%)
Millwrights	96	0.09	96	0.08	0
Miscellaneous Mechanics NEC	720	0.64	718	0.62	(0.3%)
Mechanics and Repairers, NEC	36	0.03	27	0.02	(25.0%)
Construction Trades	5,011	4.46	5,098	4.43	1.7%
Supervisors	630	0.56	617	0.54	(2.1%)
Construction Trades, except Supervisors	4,382	3.90	4,481	3.90	2.3%
Brickmasons and Stonemasons	193	0.17	202	0.18	4.7%
Carpet Installers	100	0.09	108	0.09	8.0%
Carpenters	1,388	1.23	1,427	1.24	2.8%
Drywall Installers	148	0.13	149	0.13	0.7%
Electricians	650	0.58	701	0.61	7.8%
Electrical Power Installers and Repairers	111	0.10	101	0.09	(9.0%)
Painters, Construction, and Maintenance	525	0.47	525	0.46	0
Plumbers, Pipefitters, and Steamfitters	491	0.44	494	0.43	0.6%
Concrete and Terrazzo Finishers	75	0.07	85	0.07	13.3%

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Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1987 Number of Workers	1987 Percent of Total	1988 Number of Workers	1988 Percent of Total	1987-1988 Percent Change
Insulation Workers	53	0.05	54	0.05	1.9%
Roofers	171	0.15	156	0.14	(8.8%)
Structural Metal Workers	58	0.05	48	0.04	(17.2%)
Construction Trade NEC	419	0.37	431	0.37	2.9%
Extractive Occupations	161	0.14	144	0.13	(10.6%)
Precision Production Occupations	3,951	3.51	3,968	3.45	0.4%
Supervisors	1,317	1.17	1,361	1.18	3.3%
Precision Metalworking	891	0.79	896	0.78	0.6%
Tool and Die Makers	144	0.13	145	0.13	0.7%
Machinists	483	0.43	497	0.43	2.9%
Sheet-Metal Workers	127	0.11	126	0.11	(0.8%)
Precision Metalworking, NEC	137	0.12	128	0.11	(6.6%)
Precision Woodworking Occupations	102	0.09	106	0.09	3.9%
Cabinet Makers and Bench Carpenters	56	0.05	66	0.06	17.9%
Precision Woodworking, NEC	46	0.04	40	0.03	(13.0%)
Precision Textile, Apparel, Furnishings Machine Workers	299	0.27	296	0.26	(1.0%)
Dressmakers	121	0.11	126	0.11	4.1%
Upholsterers	87	0.08	84	0.07	(3.4%)
Precision Textile, NEC	91	0.08	86	0.07	(5.5%)
Precision Workers, Assorted Materials	536	0.48	529	0.46	(1.3%)
Optical Goods Workers	50	0.04	60	0.05	20.0%
Dental Laboratory and Medical Appliance Technicians	60	0.05	49	0.04	(18.3%)
Electrical and Electronic Equipment Assemblers	325	0.29	305	0.27	(6.2%)
Precision Workers Assorted NEC	101	0.09	115	0.10	13.9%
Precision Food Production Occupations	438	0.39	418	0.36	(4.6%)
Butchers and Meat Cutters	271	0.24	258	0.22	(4.8%)
Bakers	123	0.11	126	0.11	2.4%
Precision Food Production NEC	44	0.04	34	0.03	(22.7%)
Precision Inspectors, Testers, and Related Workers	116	0.10	126	0.11	8.6%
Inspectors, Testers and Graders	103	0.09	113	0.10	9.7%
Precision Inspectors, NEC	13	0.01	13	0.01	0
Plant and System Operators	252	0.22	236	0.21	(6.3%)
Stationary Engineers	108	0.10	103	0.09	(4.6%)
Plant and System Operators NEC	144	0.13	133	0.12	(7.6%)
Operators, Fabricators, and Laborers	17,486	15.55	17,814	15.49	1.9%
Machine Operators, Assemblers, and Inspectors	7,994	7.11	8,117	7.06	1.5%
Machine Operators and Tenders, except Precision	5,257	4.68	5,362	4.66	2.0%
Metalworking and Plastic Working Machine Operators	472	0.42	465	0.40	(1.5%)
Lathe and Turning Machine Operators	60	0.05	63	0.05	5.0%
Punching and Stamping Press Machine Operators	145	0.13	123	0.11	(15.2%)

(Continued)

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Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1987 Number of Workers	1987 Percent of Total	1988 Number of Workers	1988 Percent of Total	1987-1988 Percent Change
Grinding, Abrading, Buffing, and Polishing Machine Operators	144	0.13	141	0.12	(2.1%)
Metalworking and Plastic Operators NEC	123	0.11	138	0.12	12.2%
Metal and Plastic Processing Machine Operators	157	0.14	170	0.15	8.3%
Molding and Casing Machine Operators	96	0.09	102	0.09	6.3%
Metal and Plastic Processing, NEC	61	0.05	68	0.06	11.5%
Woodworking Machine Operators	153	0.14	159	0.14	3.9%
Sawing Machine Operators	100	0.09	105	0.09	5.0%
Other Woodworking, NEC	53	0.05	54	0.05	1.9%
Printing Machine Operators	476	0.42	505	0.44	6.1%
Printing Machine Operators	321	0.29	339	0.29	5.6%
Typesetters and Compositors	76	0.07	67	0.06	(11.8%)
Printing Machine Operators, NEC	79	0.07	99	0.09	25.3%
Textile, Apparel, and Furnishings Machine Operators	1,334	1.19	1,355	1.18	1.6%
Winding and Twisting Machine Operators	80	0.07	76	0.07	(5.0%)
Textile Sewing Machine Operators	755	0.67	749	0.65	(0.8%)
Pressing Machine Operators	138	0.12	146	0.13	5.8%
Laundering and Dry Cleaning Machine Operators	195	0.17	222	0.19	13.8%
Textile, Apparel, and Furnishings, NEC	166	0.15	162	0.14	(2.4%)
Machine Operators, Assorted Materials	2,634	2.34	2,680	2.33	1.7%
Packaging and Filling Machine Operators	403	0.36	414	0.36	2.7%
Mixing and blending Machine Operators	96	0.09	102	0.09	6.3%
Separating, Filtering, and Clarifying Machine Operators	53	0.05	56	0.05	5.7%
Painting and Paint Spraying Machine Operators	185	0.16	200	0.17	8.1%
Furnace, Kiln, and Oven Operators, except Food	95	0.08	102	0.09	7.4%
Slicing and Cutting Machine Operators	218	0.19	215	0.19	(1.4%)
Photographic Process Machine Operators	100	0.09	98	0.09	(2.0%)
Machine Operators, Assorted Materials, NEC	1,484	1.32	1,493	1.30	0.6%
Other Machine Operators and Tenders	31	0.03	28	0.02	(9.7%)
Fabricators, Assemblers, and Hand-Working Occupations	1,877	1.67	1,906	1.66	1.5%
Welders and Cutters	558	0.50	555	0.48	(0.5%)
Assemblers	1,105	0.98	1,141	0.99	3.3%
Fabricators, Assemblers, NEC	214	0.19	210	0.18	(1.9%)
Production Inspectors, Testers, Samplers, and Weighers	861	0.77	849	0.74	(1.4%)
Production Inspectors, Checkers, and Examiners	694	0.62	683	0.59	(1.6%)
Production Testers	60	0.05	63	0.05	5.0%
Graders and Sorters, except Agricultural	96	0.09	96	0.08	0
Production Inspectors, NEC	11	0.01	7	0.01	(36.4%)
Transportation and Material-Moving Occupations	4,712	4.19	4,831	4.20	2.5%
Motor Vehicle Operators	3,489	3.10	3,592	3.12	3.0%
Truck Drivers, Heavy	1,822	1.62	1,826	1.59	0.2%

(Continued)

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Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1987 Number of Workers	1987 Percent of Total	1988 Number of Workers	1988 Percent of Total	1987-1988 Percent Change
Truck Drivers, Light	721	0.64	782	0.68	8.5%
Drivers-Sales Workers	226	0.20	201	0.17	(11.1%)
Bus Drivers	419	0.37	450	0.39	7.4%
Taxi-Cab Drivers and Chauffeurs	194	0.17	218	0.19	12.4%
Motor Vehicle Operators, NEC	107	0.10	115	0.10	7.5%
Transportation Occupations, except Motor Vehicle	194	0.17	195	0.17	0.5%
Rail Transportation Occupations	136	0.12	137	0.12	0.7%
Locomotive Operating Occupations	53	0.05	51	0.04	(3.8%)
Rail NEC	83	0.07	86	0.07	3.6%
Water Transportation Occupations	58	0.05	58	0.05	0
Material-Moving Equipment Operators	1,029	0.92	1,043	0.91	1.4%
Operating Engineers	184	0.16	210	0.18	14.1%
Crane and Tower Operators	81	0.07	88	0.08	8.6%
Excavating and Loading Machine Operators	115	0.10	108	0.09	(6.1%)
Grader, Dozer, and Scraper Operators	92	0.08	92	0.08	0
Industrial Truck and Tractor Equipment Operators	428	0.38	431	0.37	0.7%
Material Moving, NEC	129	0.11	114	0.10	(11.6%)
Handlers, Equipment Cleaners, Helpers, and Laborers	4,779	4.25	4,866	4.23	1.8%
Helpers, Construction and Extractive Occupations	170	0.15	156	0.14	(8.2%)
Helpers, Construction Trades	156	0.14	141	0.12	(9.6%)
Helpers, NEC	14	0.01	15	0.01	7.1%
Construction Laborers	766	0.68	799	0.69	4.3%
Production Helpers	71	0.06	64	0.06	(9.9%)
Freight, Stock, and Material Handlers	1,696	1.51	1,756	1.53	3.5%
Stock Handlers and Baggers	873	0.78	891	0.77	2.1%
Machine Feeders and Offbearers	94	0.08	110	0.10	17.0%
Freight, Stock, Material, NEC	729	0.65	755	0.66	3.6%
Garage and Service Station Related Occupations	257	0.23	246	0.21	(4.3%)
Vehicle Washers and Equipment Cleaners	214	0.19	253	0.22	18.2%
Hand Packers and Packagers	306	0.27	298	0.26	(2.6%)
Laborers, Except Construction	1,251	1.11	1,248	1.09	(0.2%)
Handlers, Equipment Cleaners, Helpers, and Laborers	48	0.04	46	0.04	(4.2%)
Farming, Forestry, and Fishing	3,507	3.12	3,437	2.99	(2.0%)
Farm Operators and Managers	1,317	1.17	1,286	1.12	(2.4%)
Farmers	1,173	1.04	1,154	1.00	(1.6%)
Farm Managers	144	0.13	133	0.12	(7.6%)
Other Agricultural and Related Occupations	2,013	1.79	1,978	1.72	(1.7%)
Farm Occupations, except Managerial	1,035	0.92	1,020	0.89	(1.4%)
Farm Workers	968	0.86	949	0.83	(2.0%)
Farm Occupations, NEC	67	0.06	71	0.06	6.0%

(Continued)

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Table W-1 (Continued). Distribution of U.S. Work Force by Detailed Occupational Category (Thousands of Workers)

Occupational Category	1987 Number of Workers	1987 Percent of Total	1988 Number of Workers	1988 Percent of Total	1987-1988 Percent Change
Related Agricultural Occupations	978	0.87	958	0.83%	(2.0%)
Supervisors	72	0.06	76	0.07	5.6%
Groundskeepers and Gardeners, except Farmers	803	0.71	765	0.67	(4.7%)
Animal Caretakers, except Farmers	90	0.08	101	0.09	12.2%
Related Agricultural Occupations, NEC	13	0.01	16	0.01	23.1%
Forestry and Logging Occupations	104	0.09	117	0.10	12.5%
Timber Cutting and Logging	72	0.06	84	0.07	16.7%
Forestry and Logging, NEC	32	0.03	33	0.03	3.1%
Fishers, Hunters, and Trappers	73	0.06	56	0.05	(23.3%)
Total	112,439	100.00%	114,969	100.0	2.3%

NEC = Not Elsewhere Classified

Source: U.S. Department of Labor, Bureau of Labor Statistics

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Table W-2. Distribution of U.S. Work Force by Major Occupational Category (Thousands of Workers)

Occupational Category	Actual 1986	1987	1988	Estimated 1991	1993	1995	2000
Executive, Administrative, and Managerial	12,642	13,316	14,216	14,730	15,072	15,415	16,270
Professional Specialty	13,911	14,426	14,974	15,647	16,096	16,545	17,667
Technicians and Related Support	3,364	3,346	3,521	3,803	3,991	4,179	4,649
Sales Occupations	13,245	13,480	13,747	14,602	15,171	15,741	17,166
Administrative Support, Including Clerical	17,745	18,256	18,264	18,640	18,891	19,141	19,768
Private Household	981	934	909	704	567	430	88
Protective Service	1,787	1,907	1,944	2,051	2,122	2,193	2,371
Service, except Private Household and Protective	11,913	12,213	12,479	13,311	13,866	14,421	15,808
Precision Production, Craft, and Repair	13,405	13,568	13,664	14,001	14,226	14,451	15,014
Operators, Fabricators, and Laborers	17,160	17,486	17,814	17,762	17,728	17,693	17,606
Farming, Forestry, and Fishing	3,444	3,507	3,437	3,399	3,374	3,349	3,286
Total	109,597	112,439	114,969	118,650	121,104	123,558	129,693

Source: U.S. Department of Labor,
Bureau of Labor Statistics
Dataquest
June 1989

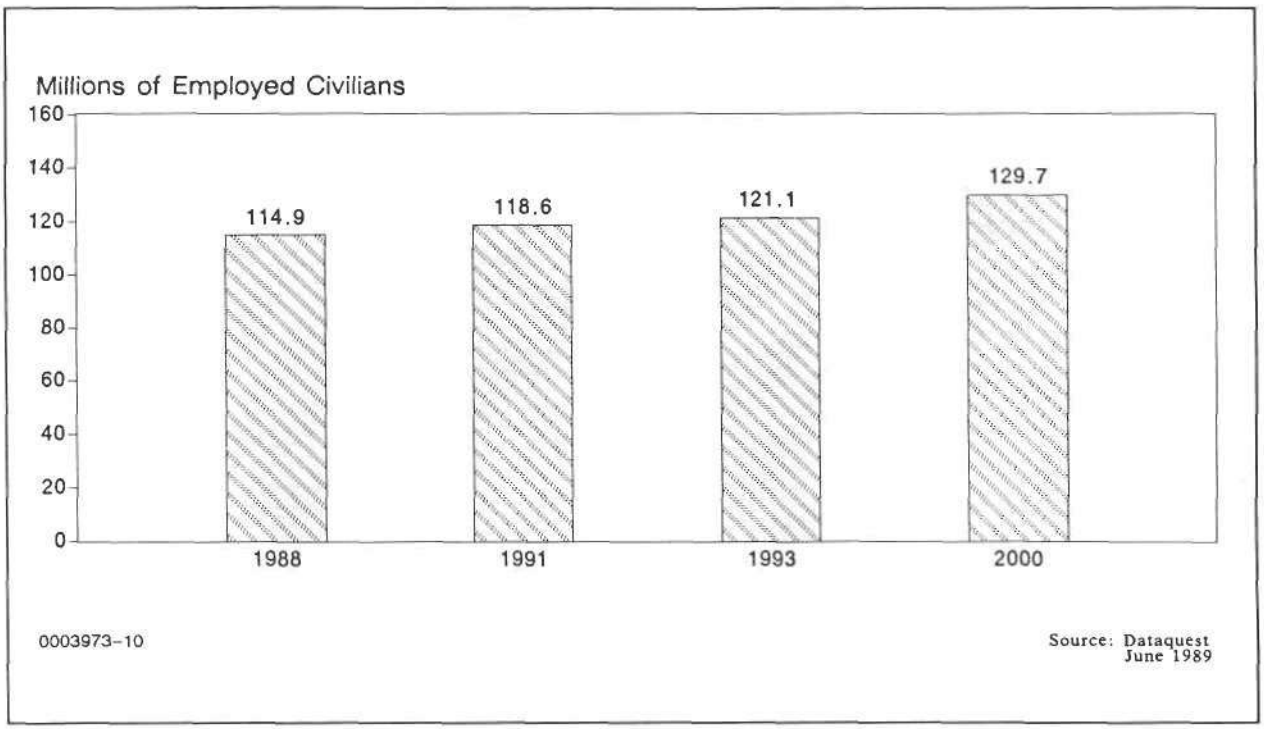

Figure 10. Number of Employed U.S. Civilian Workers

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Table W-3. Employment Growth by Industry for 1987 and 1988 Annual Estimates through 2000 (Thousands of Workers)

Industry	Actual 1987	Actual 1988	Estimated 1990	Estimated 1993	Estimated 1995	Estimated 2000
Agriculture	3,208	3,169	3,338	3,593	3,751	4,116
Mining	818	753	776	811	827	852
Construction	7,456	7,603	7,822	8,150	8,366	8,895
Manufacturing	20,935	21,320	21,326	21,331	21,342	21,396
Transportation and Public Utilities	7,880	8,064	8,101	8,154	8,194	8,310
Wholesale and Retail Trade	23,392	23,664	24,256	25,144	25,715	27,083
Finance	7,763	7,921	8,073	8,301	8,452	8,829
Services	35,743	37,043	38,275	40,128	41,387	44,586
Private Household	1,241	1,163	1,180	1,205	1,215	1,218
Public Administration	5,271	5,432	5,456	5,492	5,524	5,626
Total	112,439	114,969	117,423	121,104	123,558	129,693

Source: U.S. Department of Labor, Bureau of Labor Statistics
Dataquest
June 1989

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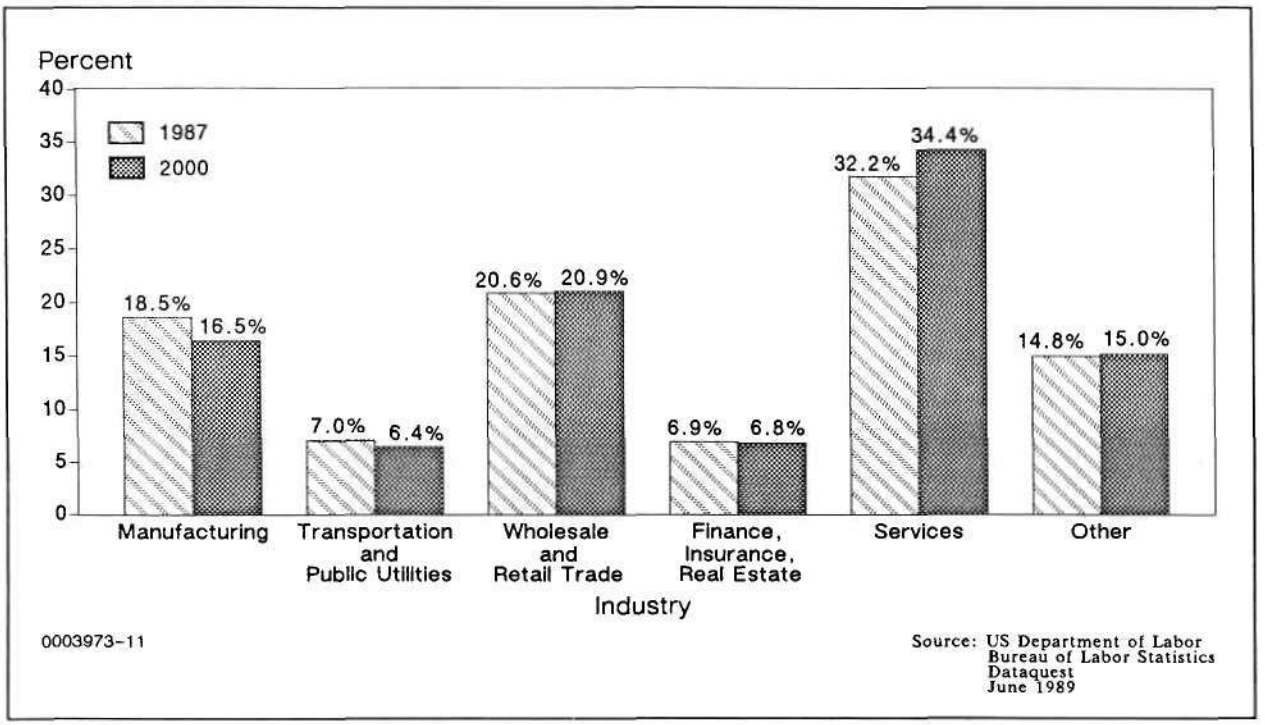

Figure 11. Employment Growth by Industry, 1988–2000

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Table W-4. Estimated U.S. White-Collar Workers by Job Classification

Job Function	1987 Total White-Collar Workers (Millions)	1987 Percent Total Work Force	1988 Total White-Collar Workers (Millions)	1988 Percent Total Work Force	1993 Total White-Collar Workers (Millions)	1993 Percent Total Work Force
Executive, Administrative, and Managerial	13.3	11.8%	14.2	12.4%	15.1	12.5%
Professional Specialty	14.4	12.8	15.0	13.0	16.1	13.3
Technicians and Related Occupations	3.3	2.9	3.5	3.0	3.9	3.3
Sales Workers	13.5	12.0	13.7	11.9	15.2	12.6
Administrative Support (Including Clerical)	18.3	16.3	18.3	15.9	18.9	15.6
Total White Collar	62.8	55.9%	64.7	56.2%	69.2	57.3%
Total Work Force	112.4	100.0%	114.9	100.0%	121.1	100.0%

Source: U.S. Department of Labor, Bureau of Labor Statistics
Dataquest
June 1989

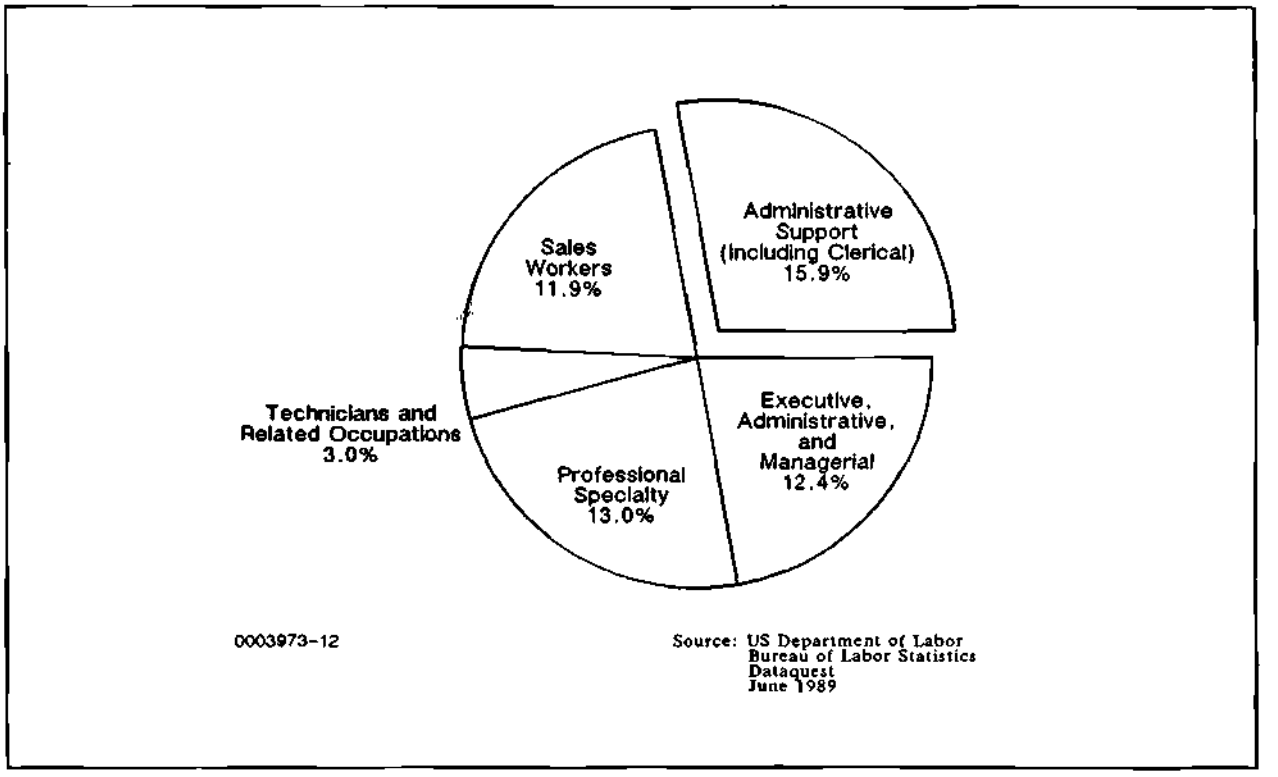

Figure 12. 1988 White-Collar Workers by Job Classification as a Percentage of Total Work Force

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Table W-5. Estimated U.S. White-Collar Workers by Industry Sector

Industry Sector	1987 White-Collar Workers (Millions)	1987 Percent Total White Collar	1988 White-Collar Workers (Millions)	1988 Percent Total White Collar	1993 White-Collar Workers (Millions)	1993 Percent Total White Collar
Services	23.4	37.3%	24.4	37.7%	27.6	39.9%
Wholesale and Retail Trade	14.5	23.1	14.8	22.9	15.8	22.8
Manufacturing	7.9	12.5	8.1	12.5	7.9	11.4
Finance, Insurance, and Real Estate	7.2	11.5	7.3	11.3	7.8	11.3
Transportation, Communication, and Utilities	4.0	6.4	4.1	6.3	4.0	5.8
Other*	5.8	9.2	6.0	9.3	6.1	8.8
Total White Collar	62.8	100.0%	64.7	100.0%	69.2	100.0

*Includes agriculture, mining, construction, and public administration.

Source: U.S. Department of Labor, Bureau of Labor Statistics
Dataquest
June 1989

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Table W-6. Estimated U.S. White-Collar Workers as a Percent of Total Work Force by Industry Sector

Industry Sector	1987 Total Work Force (Millions)	1987 Percent White Collar	1988 Total Work Force (Millions)	1988 Percent White Collar	1993 Total Work Force (Millions)	1993 Percent White Collar
Services	35.7	65.6%	37.0	65.6%	40.0	68.9%
Wholesale and Retail Trade	23.4	62.0	23.7	65.8	25.2	62.9
Manufacturing	20.9	37.6	21.3	38.0	21.3	37.1
Finance, Insurance, and Real Estate	7.8	92.9	7.9	92.9	8.3	93.8
Transportation, Communications, and Utilities	7.9	51.1	8.1	50.8	8.2	49.3
Others*	16.7	34.5	16.9	35.8	18.1	34.9
Total White Collar	112.4	55.9%	114.9	56.3%	121.1	57.2%

*Includes agriculture, mining, construction, and public administration.

Source: U.S. Department of Labor, Bureau of Labor Statistics
Dataquest
June 1989

Table W-7. Number of Desktops by Job Classification (Thousands)

Occupational Classification	1988	1989	Estimated 1991	1993	1995
Managerial and Professional Specialty	32,080	32,512	33,375	34,239	34,678
Technical, Sales, and Administrative Support	31,948	32,377	33,236	34,095	34,116
Service Occupations	1,569	1,601	1,665	1,728	978
Precision Production, Craft, and Repair	1,999	2,017	2,053	2,089	3,637
Operators, Fabricators, and Laborers	147	148	150	153	127
Farming, Forestry, and Fishing	1,107	1,107	1,106	1,105	1,295
Total	68,850	69,762	71,585	73,409	74,831

Source: Dataquest June 1989

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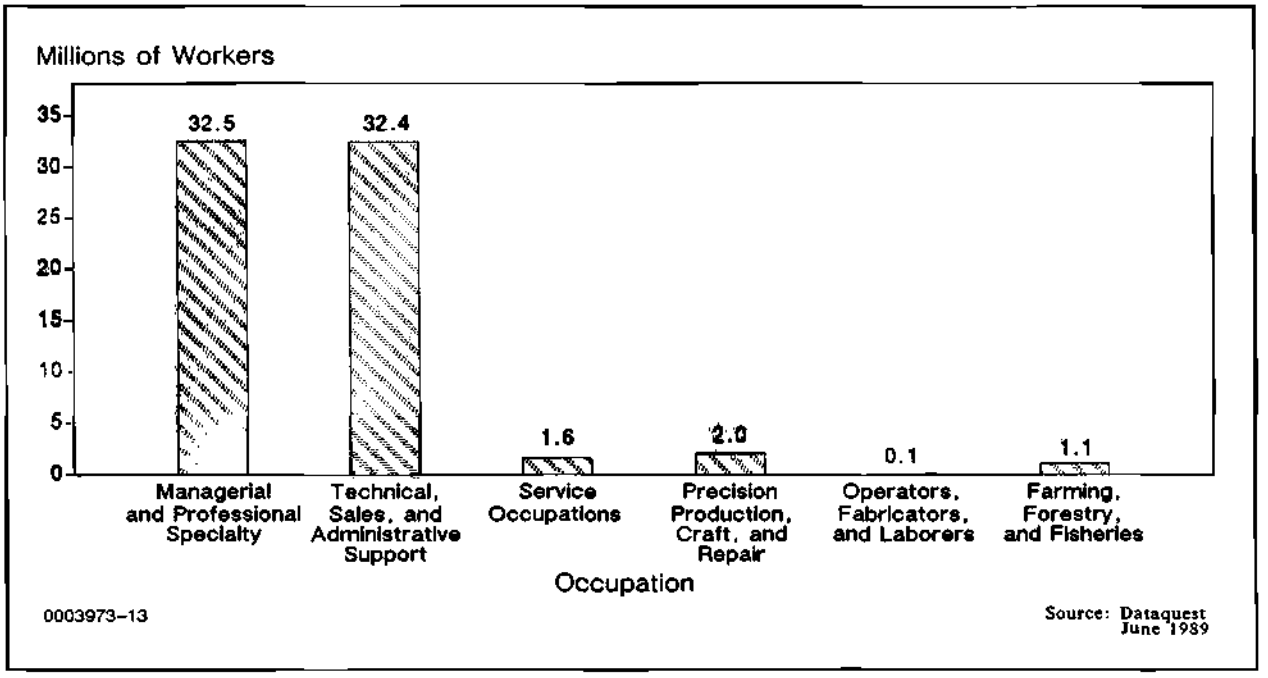

Figure 13. Number of Desktops by Major Occupational Category

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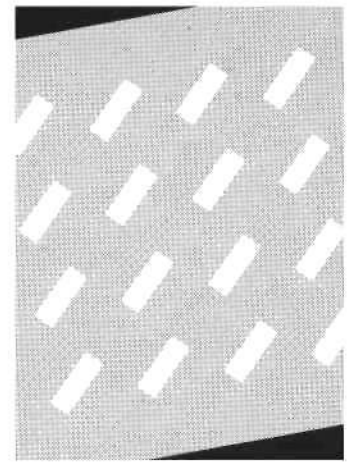

Economic Outlook Update
1988–1990

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Preface

This report is an update to the *Economic Outlook 1988-1989* that was published by Dataquest in early 1988. As such, many references and definitions in this report assume the reader will use it as a continuation of the data and projections in the previous report.

Highlights contained in this report are:

- Real U.S. GNP growth will continue at an average 3.4 percent annualized rate through the first quarter of 1989 then will slow through the last three quarters of that year. Overall 1989 real GNP will be 2.8 percent greater than the record for 1988. A recession is forecast in the first two quarters of 1990, followed by a sharp rebound led by consumer spending and private investment in the second half of the year.
- The rate of U.S. domestic spending on capital equipment and production capacity improvement that saw double-digit growth in the first half of 1988 will gradually slow until reaching negative growth in the fourth quarter of 1989. Investment spending will continue to decrease in early 1990, particularly in the second quarter. Improvement will follow in the second half.
- The U.S. trade deficit will show steady improvement toward a negative $50 billion annualized level by mid-1990, when higher interest rates and a stronger dollar will begin to attenuate the rate of progress.
- The U.S. federal budget deficit will be largely unaffected by the national elections and existing Gramm-Rudman legislation. New federal programs in 1990 will be funded by additional consumption taxes, changes in personal income tax ceilings, reductions in some personal tax credits and federally mandated shifts in some worker-related program funding to corporations.

Introduction

The last years of the 1980s are an exciting time. Political and economic events are unfolding in the United States and throughout the world in a vast interactive network. The influence of these economic developments is significant in our daily lives, in the prospects for business endeavors, and from the perspective of strategic national interests. The international influence of nations is based on their relative economic strengths, and long-term economic changes are resulting in unmistakable geographical shifts of power.

During autumn of 1988, we will see developments on many issues important to the nations listed below, that may cause reverberations in the economic outlooks of other nations:

United States

In the United States, Americans are wrestling with massive deficits in the federal budget and in international trade. Both problems will be treated with platitudes in the upcoming national elections due to the political realities of playing for votes and avoiding special-interest sensitivities. However, after the election, both issues will affect greatly the programs of the new president and his administration's performance rating.

Canada

Political debate is reaching a climax in Canada and the United States on the pending free trade agreement between the two countries. The Liberal opposition to Prime Minister Mulroney has threatened to delay action until Mr. Mulroney calls parliamentary elections, which in effect is a national referendum on free trade.

Japan

What country is the world's biggest donor of foreign aid, the second-largest contributor to the United Nations, and has the world's third-largest defense budget? Answer: Japan, with a $10 billion budget for foreign aid in 1988, pushing past the United States' $9.2 billion program. The Japanese are just beginning to formulate the manner and direction in which they will exercise their new economic power and wealth.

U.S.S.R.

The fascinating cultural and political experiments by Mikhail Gorbachev in attempt to rejuvenate the Soviet economy, coupled with the warming of U.S.-Soviet relations, have already resulted in benefits to U.S. electronics companies through a relaxation of U.S. technology export regulations.

Iran and Iraq

Iran and Iraq appear to be approaching a cease-fire that, if realized, will directly affect crude oil production and prices as the two countries boost output to help recover from the destruction and $300 billion expense of their eight-year war.

EEC

The 12-country European Economic Community (EEC) is proceeding steadily toward its target of standardizing internal financial regulations and eliminating *internal* trade restrictions by 1992. There are growing indications that the Europeans will implement strong protectionist measures to favor European "national champion" computer and telecommunications companies in the form of import quotas, bidding restrictions on government contracts, and minimum local content requirements on hardware.

In effect, they may replace national trade barriers with one large trade barrier around the entire community.

Taiwan and the Peoples' Republic of China

Taiwan and the Peoples' Republic of China are quickly warming to the possibilities of increased cooperation in bilateral trade, investment, and travel. China has raw materials, cheap labor, and is starved for foreign capital, while Taiwan needs to reduce manufacturing costs and continue to expand into new markets.

How will these events affect the electronics industry? What new opportunities will emerge? What are the best strategies to anticipate these changes? For U.S. multinational companies, the answers are based in part on expectations for the outlook for the U.S. economy through 1990.

United States International Trade

U.S. exports continue to surge ahead in the third quarter of 1988, at a pace 30 percent greater than the same period to date in 1987. U.S. industry's export record in 1987 was itself the largest one-year increase this decade: an 11 percent increase over 1986. The bulk of U.S. export volume is in chemicals, auto parts and subassemblies, industrial machinery (including computers and associated hardware) and raw materials. Many of these exporting industries were forced to restructure and upgrade production processes earlier in the decade in order to stay competitive when the dollar's value was peaking. The dollar's three-year (1985-1988) slide has since been accompanied by an acceleration of international sales.

Exporting companies began to feel the effects of the cheaper dollar in mid-1985, as the dollar began to decline and significant international orders followed shortly thereafter. This key relationship between dollar exchange rates and export sales is illustrated in Figures 1 and 2. Dollar exchange rates reached bottom in early 1988 and have shown a recent tendency to creep upward. Dataquest expects the index of dollar exchange rates against trade-weighted currencies will remain close to current levels through 1989, before mid-1990 increases bring the dollar back up to 1986 levels.

Where are U.S. exports going? Figure 3 ranks geographical markets in descending order by aggregate merchandise export value from January through May this year, compared with the same period last year. Western Europe alone accounts for more than $7 billion of the $30 billion export increase so far in 1988. When U.S. exports to Canada and Japan are included, these three market areas constitute 62 percent of the export trade, and 52 percent of the 1988 year-to-date increase. Percentage increases in export values through May of 1988 compared with the same period in 1987 are graphed in Figure 4.

It is worth noting in the midst of this success that most of the 1988 improvement in U.S. international trade has come in established markets, such as Western Europe, that are growing at slower rates than Pacific Rim economies. U.S. companies still focus their export strategies largely toward Europe, and think of Asian countries primarily in terms of defensive marketing strategies. U.S. exporters must quickly recognize that the Pacific Rim is a top priority market equal in value to the U.S. export trade with Western Europe, and will be twice the value of U.S.-European trade before the turn of the century.

U.S. import activity for 1988 to date is compared with the same period in 1987 in Figure 5, reflecting some percentage shifts toward new sources of imports from Asia and South America.

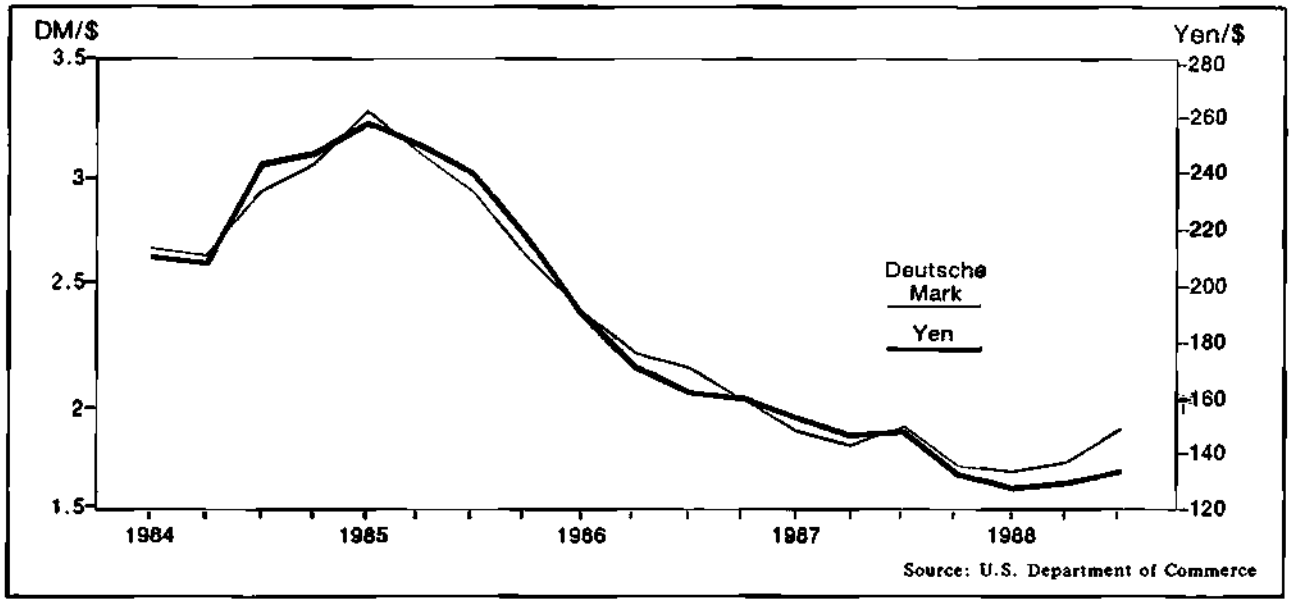

Figure 1. Dollar Exchange Rates (Quarterly Averages) 1984-1988

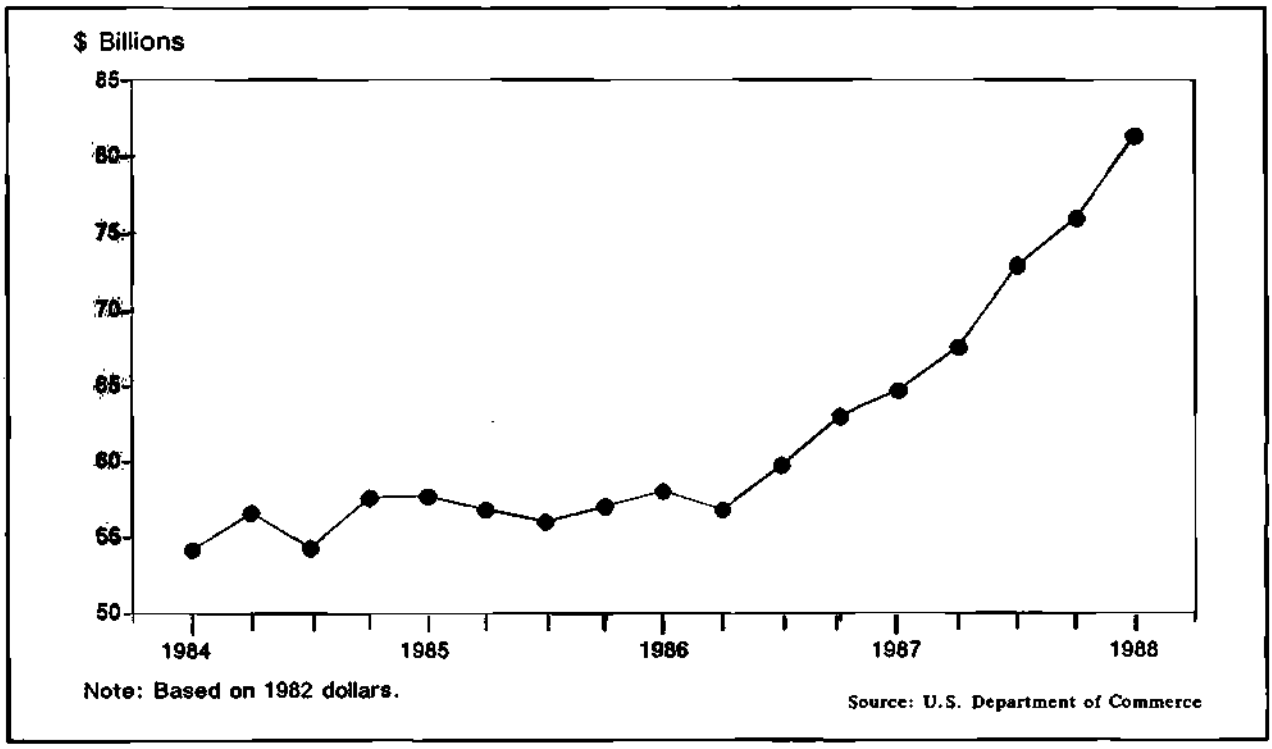

Figure 2. U.S. Merchandise Exports (Quarterly) 1984-1988

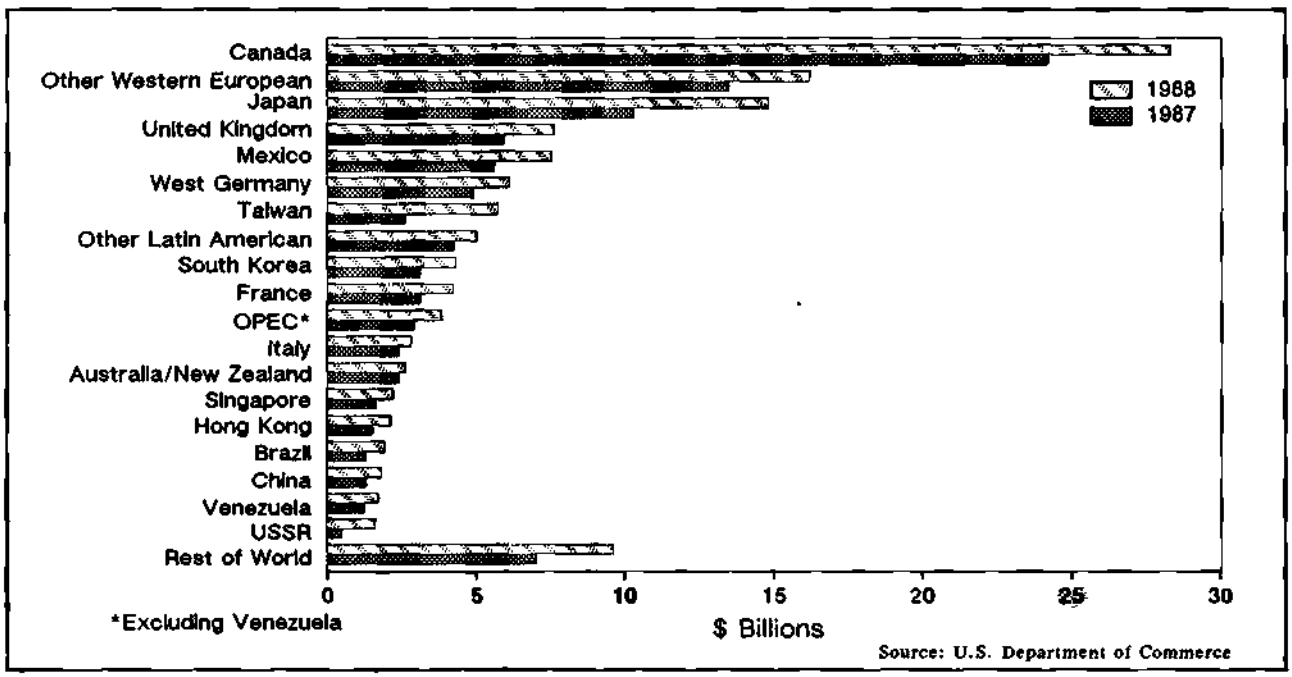

Figure 3. Comparison of U.S. Export Markets, January-May 1988 versus January-May 1987 (Bilions of Dollars)

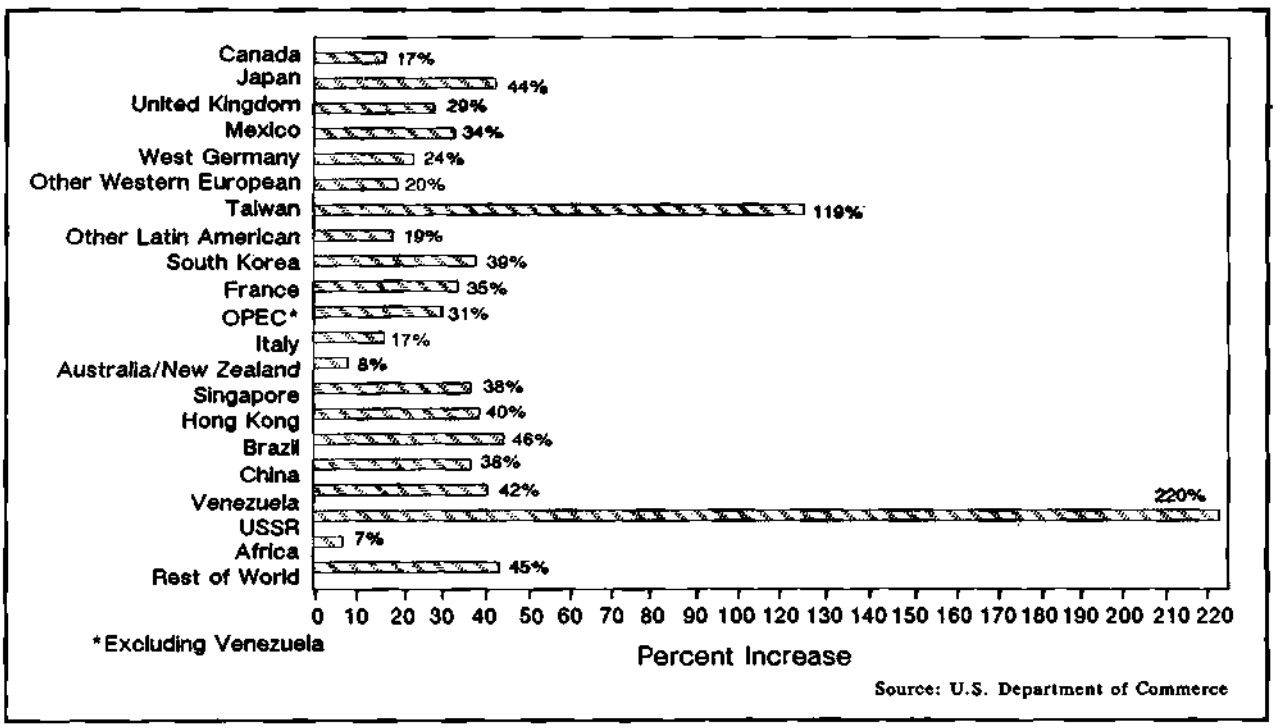

Figure 4. U.S. Merchandise Exports—Percentage Increases January-May 1988 versus January-May 1987

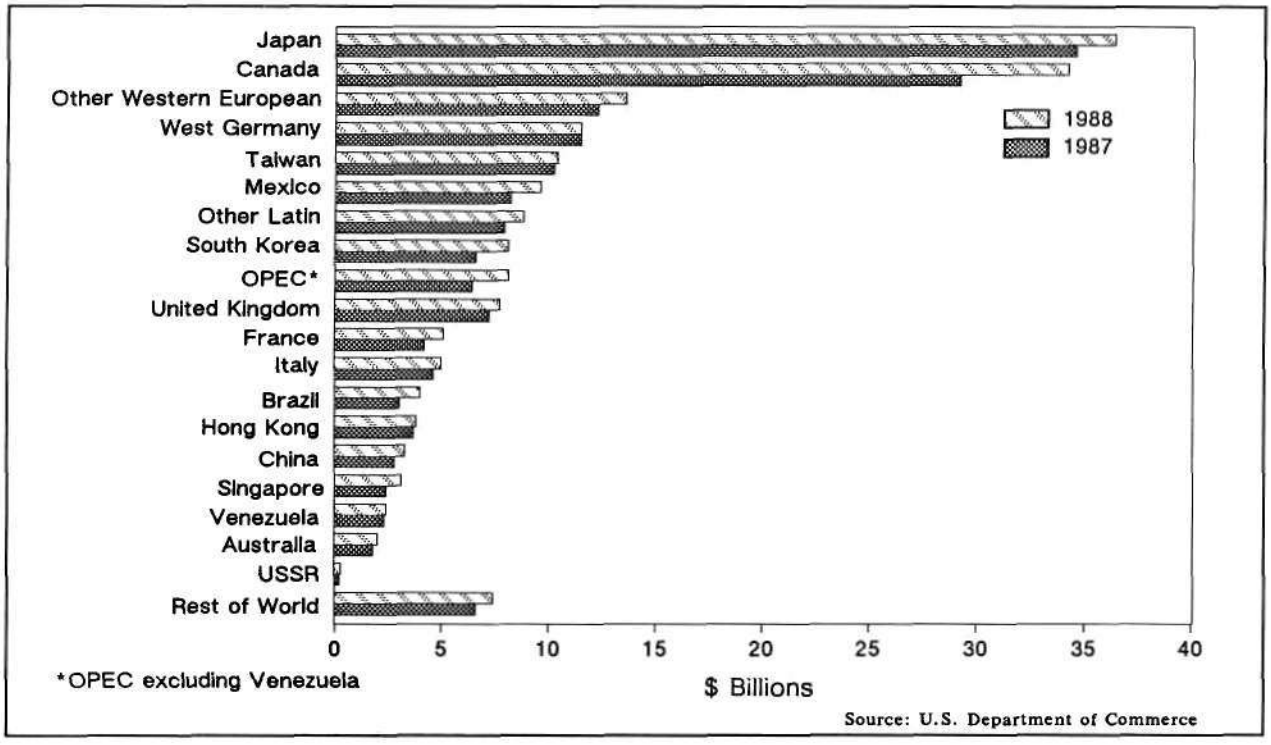

Figure 5. Comparison of U.S. Import Activity, January-May 1988 versus January-May 1987 (Bilions of Dollars)

What about the specific markets for electronics goods? Figure 6 ranks the top twelve national markets for three basic categories of American electronic products: computers, semiconductors, and telecommunications equipment. Canada, the United Kingdom, and Japan remain the top three markets in a pattern and product mix very similar to that of 1987. Figures 7 and 8 compare 1988 and 1987 electronics import and export activity through April of each year. In general, computer equipment shows the largest absolute increase: $1.9 billion in exports so far this year compared with the same period in 1987, a 36 percent increase. Telecommunications equipment accounted for the largest rise with an increase in export value of 40 percent.

Imports of foreign goods into the U.S. have slackened slightly, as importers have struggled to remain price-competitive in the face of weak dollar exchange rates. A significant part of this process has been a growing shift toward less-expensive imports from newly industrializing countries, particularly the Republic of Korea, Brazil, Singapore, and China. The American consumer's passion for imports has not diminished; it has been transferred to other, cheaper, sources of supply.

Figure 9 demonstrates the continuing close linkage between U.S. consumption, measured by final sales to domestic purchasers, and the value of imported goods into the United States. Final sales is an accurate measure of domestic demand in that it includes import sales and excludes unsold inventory and exports. Dataquest forecasts diminishing annual rates of increase in final sales, measured quarterly, through the remainder of 1988 and into early 1990. These and other projections are contained in Table 1. Along with a forecast of continued export strength, a corresponding decrease in the U.S. international trade deficit is projected, lowering it to an annualized $50 billion level by the middle of 1990. Figure 10 shows the history and Dataquest forecast of total merchandise trade on a quarterly basis through 1990.

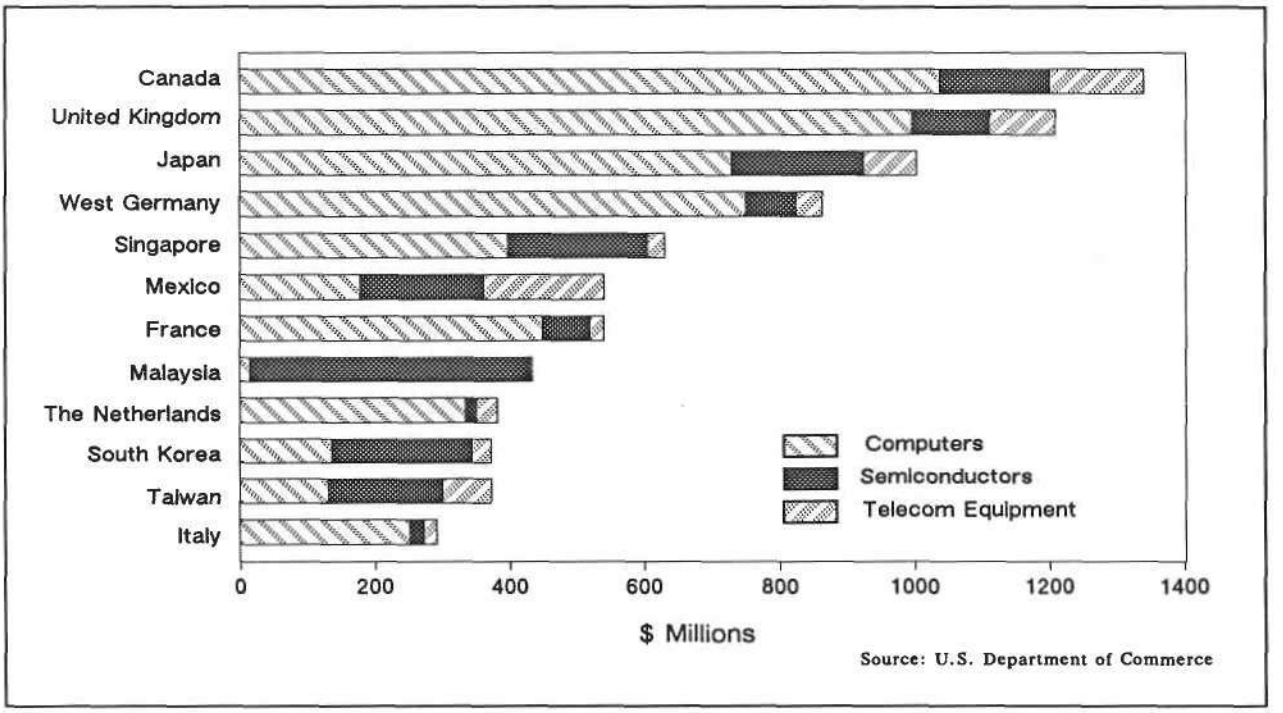

Figure 6. U.S. Electronics Exports—January-April 1988, Top Twelve Markets

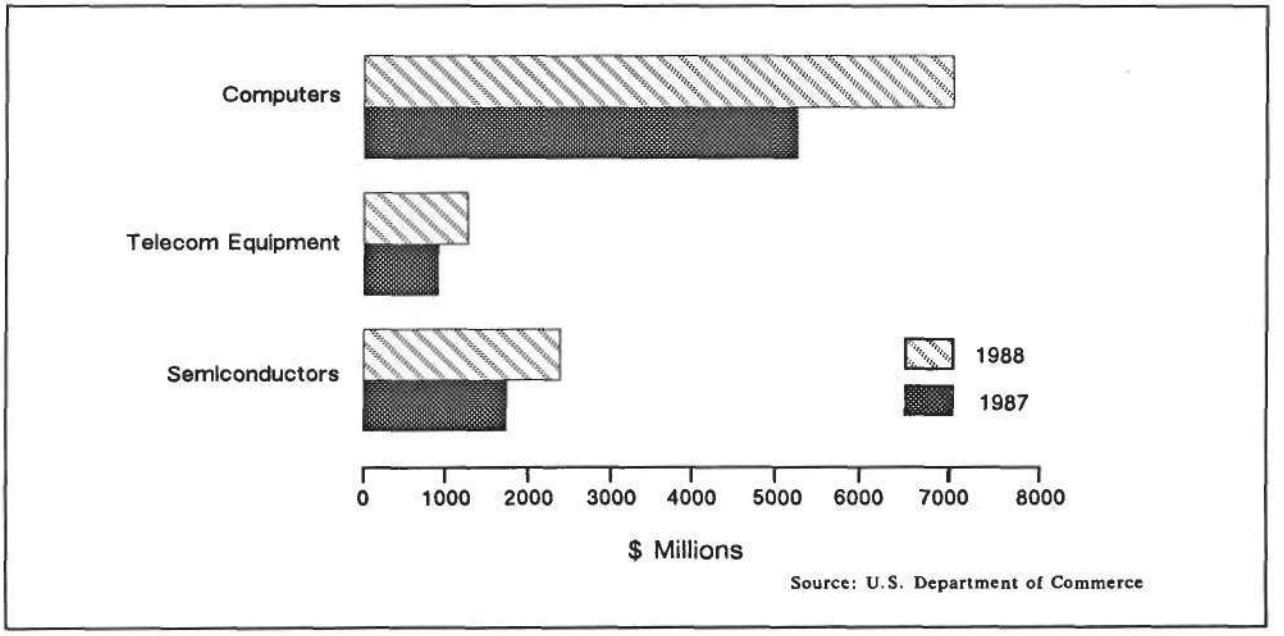

Figure 7. U.S. Electronics Exports January-April 1988 versus January-April 1987

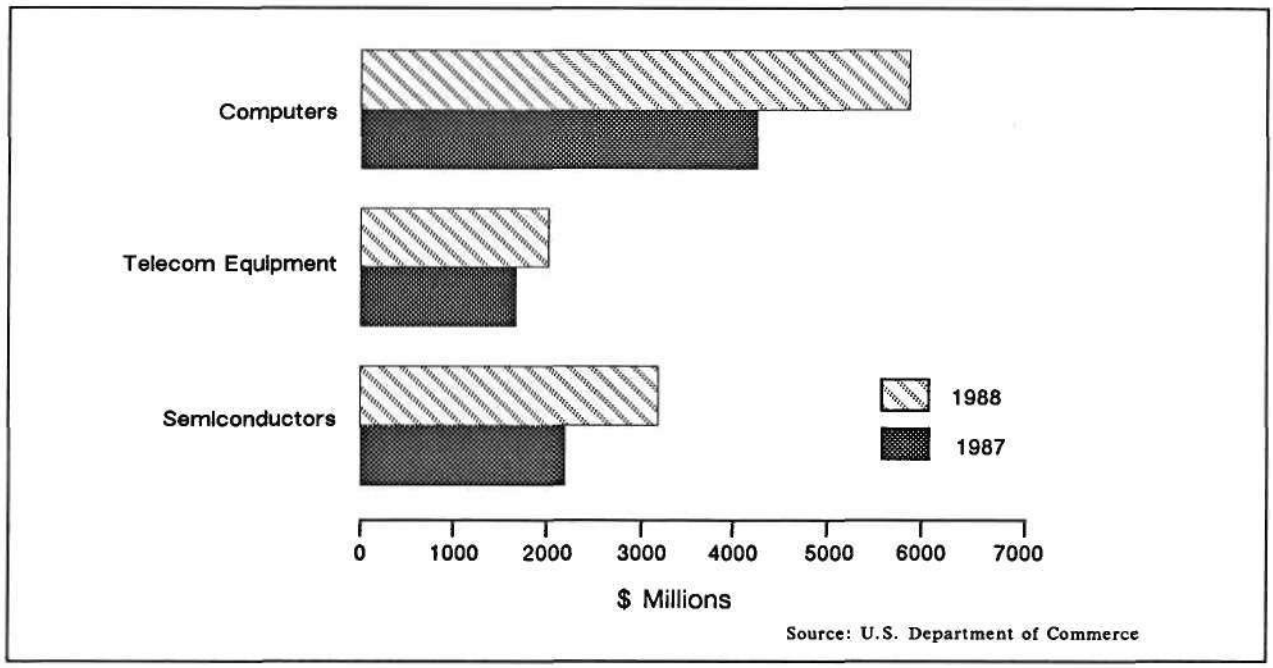

Figure 8. U.S. Electronics Imports January-April 1988 versus January-April 1987

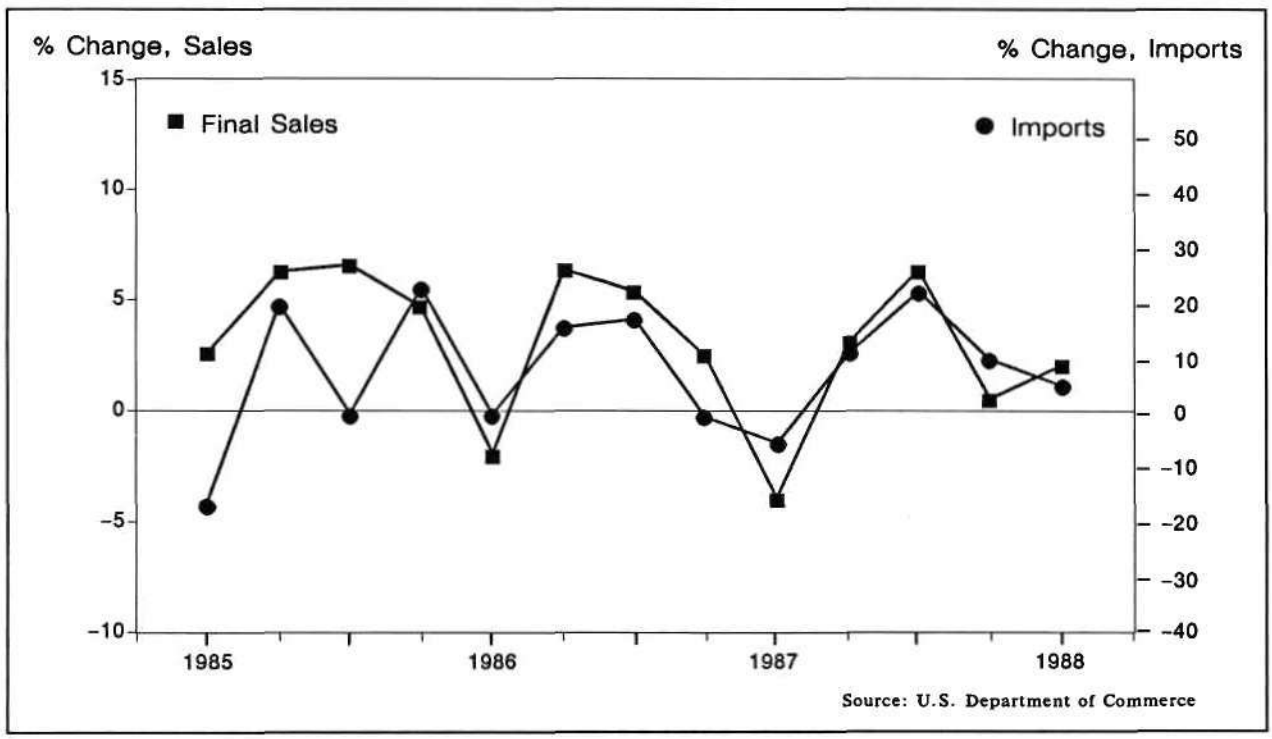

Figure 9. Final Sales to Domestic Purchasers versus Imports (Quarter-to-Quarter Changes) 1985-1988

Table 1. Dataquest Economic Forecast, 1988-1990

	1988 Q1	1988 Q2	1988 Q3	1988 Q4	Average 1988	1989 Q1	1989 Q2	1989 Q3	1989 Q4	Average 1989	1990 Q1	1990 Q2	1990 Q3	1990 Q4	Average 1990
Real GNP, SAAR	$3,956	$3,988	$4,015	$4,049	$4,002	$4,084	$4,110	$4,127	$4,134	$4,114	$4,109	$4,092	$4,132	$4,185	$4,129
% Change, Year Ago	4.8%	4.3%	3.9%	3.2%		2.4%	3.0%	2.8%	2.1%		0.6%	(0.4%)	0.1%	1.2%	
% Change, Annual Rate	3.4%	3.3%	2.6%	3.4%		3.4%	2.7%	1.7%	0.7%		(2.4%)	(1.6%)	3.9%	5.1%	
Consumer Spending	2,560	2,576	2,591	2,612	2,585	2,630	2,643	2,651	2,656	2,645	2,641	2,638	2,668	2,703	2,663
% Change, Year Ago	2.8%	2.4%	1.8%	3.2%		2.1%	2.7%	2.3%	1.7%		0.5%	(0.1%)	0.6%	1.7%	
% Change, Annual Rate	4.5%	2.5%	2.3%	3.3%		2.7%	2.1%	1.2%	0.7%		(2.1%)	(0.3%)	4.4%	5.0%	
Fixed Investment	473	489	501	512	494	520	526	529	527	525	518	503	505	514	510
% Change, Year Ago	13.2%	12.5%	8.2%	10.2%		9.8%	7.6%	5.7%	2.8%		(0.3%)	(4.5%)	(4.6%)	(2.3%)	
% Change, Annual Rate	7.6%	16.0%	9.7%	9.7%		5.8%	5.3%	2.1%	(2.0%)		(6.2%)	(11.3%)	1.5%	7.7%	
Equipment Investment	349	362	372	384	367	392	399	402	400	398	392	377	379	388	384
% Change, Year Ago	17.6%	15.3%	11.2%	15.3%		12.1%	10.3%	8.1%	4.3%		0.1%	(5.5%)	(5.7%)	(3.0%)	
% Change, Annual Rate	21.6%	14.8%	12.2%	12.8%		8.4%	7.5%	3.2%	(2.0%)		(7.3%)	(14.5%)	2.1%	10.1%	
Residential Investment	190	191	190	189	190	190	190	191	191	190	189	190	195	204	194
Government Purchases	776	777	792	796	785	799	802	810	812	806	806	808	815	820	812
% Change, Year Ago	0.5%	0.6%	1.2%	0.4%		2.9%	3.1%	2.3%	2.0%		0.9%	0.8%	0.5%	1.0%	
% Change, Annual Rate	(7.9%)	0.4%	8.0%	1.8%		1.5%	1.4%	4.4%	0.8%		(3.1%)	1.1%	3.3%	2.8%	
Net Exports	(109)	(90)	(96)	(93)	(97)	(88)	(83)	(77)	(67)	(79)	(55)	(48)	(48)	(51)	(50)
Inventory Change	66	45	37	33	45	33	32	23	15	26	10	1	(3)	(5)	1
Final Sales to Domestic Purchasers	3,975	4,019	4,049	4,077	4,030	4,093	4,101	4,117	4,132	4,111	4,136	4,157	4,196	4,235	4,181
% Change, Year Ago	3.0%	3.3%	2.5%	3.1%		3.0%	2.0%	1.7%	1.3%		1.1%	1.4%	1.9%	2.5%	
% Change, Annual Rate	1.9%	4.5%	3.0%	2.9%		1.6%	0.8%	1.5%	1.5%		0.4%	2.1%	3.8%	3.7%	
Dollar Exchange Rate Index	147	149	150	149	149	146	143	140	140	142	144	148	152	156	150
% Change, Year Ago	(0.3%)	1.8%	0.5%	0.4%		(0.7%)	(4.0%)	(6.7%)	(6.0%)		(1.4%)	3.5%	8.6%	11.4%	
% Change, Annual Rate	0.1%	5.4%	2.7%	(2.7%)		(8.1%)	(8.2%)	(8.4%)	0.0		11.4	11.1%	10.8%	10.5%	
Unemployment Rate	5.7%	5.4%	5.3%	5.2%	5.4%	5.4%	5.5%	5.7%	6.0%	5.7%	6.6%	7.4%	7.4%	7.3%	
Interest Rates															
3-Month T-Bills	5.7%	6.2%	6.9%	7.0%	6.5%	7.2%	7.9%	8.4%	8.9%	8.1%	8.6%	8.1%	7.7%	7.3%	7.9%
30-Year T-Bonds	8.6%	9.1%	9.2%	9.6%	9.1%	10.2%	10.6%	10.9%	10.1%	10.4%	9.3%	9.0%	8.8%	9.0%	9.0%
Savings Rate	4.7%	4.4%	4.3%	4.3%	4.4%	4.4%	4.6%	4.7%	4.3%	4.6%	4.4%	4.5%	4.4%	4.2%	4.4

Note: Values shown are billions of 1982 dollars and are seasonally adjusted annual rates.

Source: U.S. Department of Commerce
Dun & Bradstreet
Dataquest
September 1988

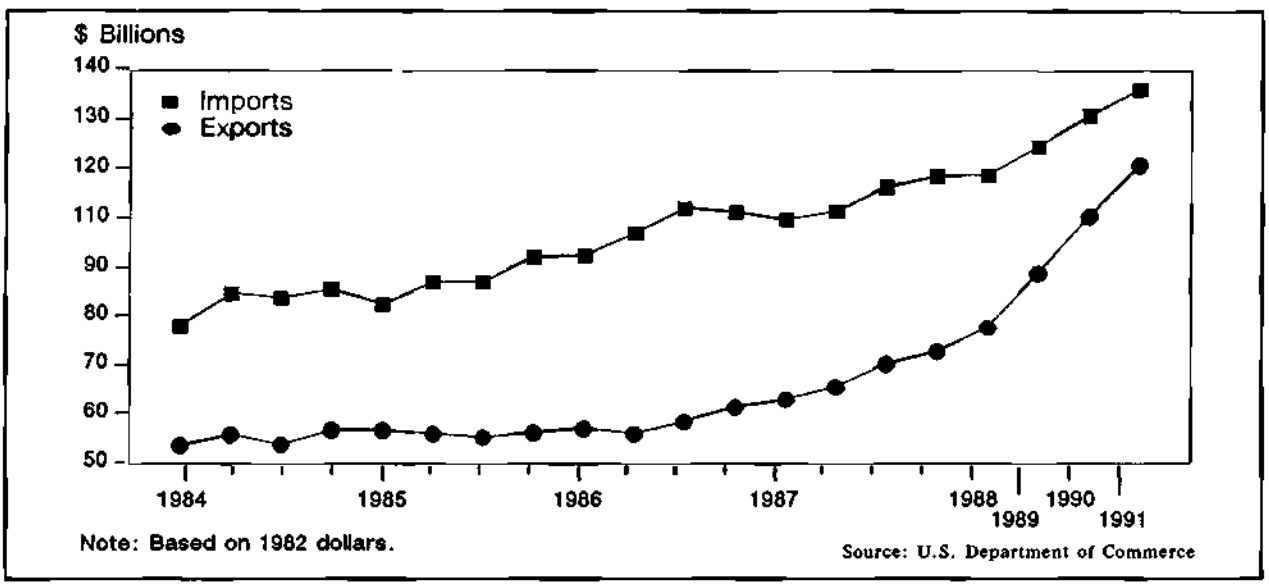

Figure 10. U.S. Merchandise Trade, Quarterly 1984-1990

The status of U.S. trade from February through May 1988 is shown in Figure 11. The predominant roles of Japan and Canada in the current U.S. trade position can be seen clearly, as can the broad distribution of the U.S. deficit across many markets. The fruitful relationship between the United States and Canada offers the United States more near-term possibilities for improved trade activity than does the U.S.-Japan trade relationship. This potential improvement centers on the pending free-trade agreement now being debated in both national legislatures. Seventy-five percent of the $140 billion value of goods passing between the two countries is currently duty free, while the remainder is subject to Canadian duties averaging 9.9 percent and U.S. duties of 3.3 percent. The agreement will remove all tariffs and many nontariff barriers to bilateral trade over 10 years, establishing rules for trade in services, investments, hydroelectric and petroleum energy, and government procurement activity. Studies by the two governments have concluded that this stimulus to direct trade ultimately could add as much as 10.0 percent to the Canadian GNP and 1.0 percent to that of the United States. Congress likely will approve the measure by September, but Liberal and New Democratic opposition leaders in the Canadian Parliament may force national elections this fall as a trade referendum. Canadian objections to final approval relate to the regulation of subsidies, procedures for settlement of disputes, and deep Canadian concern about dilution of their cultural and economic sovereignty by their southern partner.

More than 24 percent of U.S. exports go to Canada, while 17 percent of imports into the U.S. come from Canada, but in 1987 the net difference was a U.S. trade deficit of $12 billion. By comparison, 11 percent of U.S. exports are shipped to Japan, and 21 percent of U.S. imports are Japanese goods. U.S. exports to Japan are accelerating much faster than imports, 44 percent from January through May 1988 compared with the same period in 1987. However, the United States has a huge gap to bridge against the higher aggregate value of imported Japanese goods into the U.S., which rose only 5 percent.

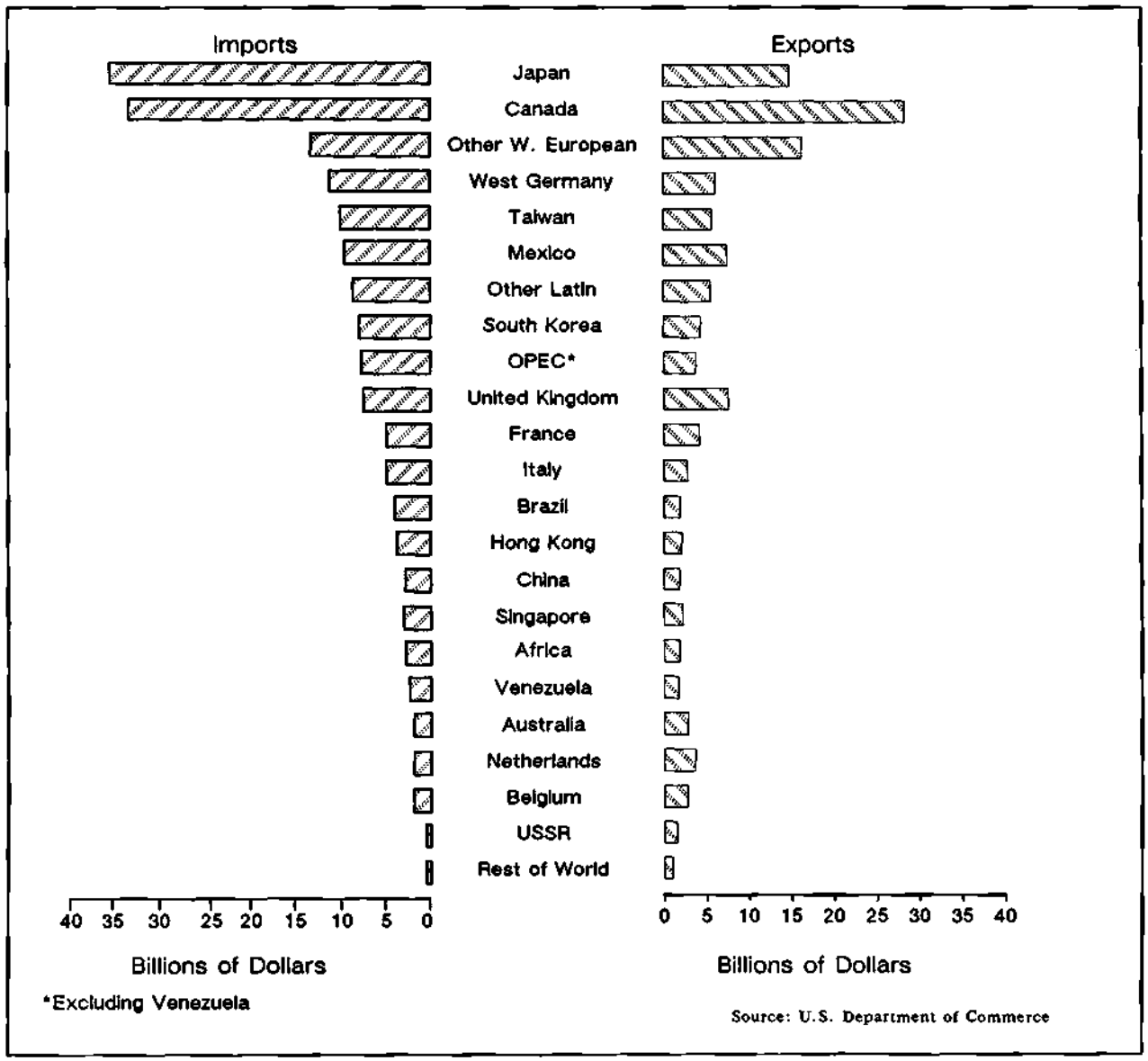

Figure 11. U.S. Merchandise Trade—January-May 1988 (Dollars in Billions)

U.S. Domestic Economic Outlook—downturn In The First Half Of 1990

The Dataquest outlook is for continued strong economic growth through the first three quarters of 1989. Robust exportation and domestic capital spending, coupled with healthy employment growth and a moderating level of consumer spending on imports, all translate into an optimistic economic forecast, particularly for sales of electronic goods and equipment.

There are, of course, many potentially destabilizing factors. When demand for skilled workers exceeds supply and limitations on production capacity are reached, manufacturers must train new workers and invest in additional plant and equipment. To the extent that these additional costs are not reflected directly in additional

production, they are inflationary. A continuing deficit at the federal level itself creates inflationary pressures and affects consumer and business confidence. Any increases in the discount rate by the Federal Reserve Board in attempts to keep economic growth and inflation rates within reasonable limits are followed closely by increases in general interest rates. As interest rates in the United States increase, thedollar.becomes more attractive and its exchange value against other currencies rises. Ultimately, a stronger dollar makes imported goods less expensive and U.S. goods more costly in foreign markets, tending to reverse U.S. trade gains.

Aside from catastrophic external events, the onset and magnitude of a general economic downturn are caused by the *coincident* rise of many of these separate factors to significant levels. Dataquest believes that the likelihood of a downturn is increasingly probable by late 1989, as outlined in the introduction to this report and in Table 1. Dataquest anticipates that the most likely scenario involves 1989 increases in interest rates by the Federal Reserve Board, coupled with plans for higher taxes and continued government spending. Declines in consumer sentiment and spending will result in a more pessimistic mood in the business community and subsequent capital spending cuts from the fourth quarter of 1989 through the second quarter of 1990.

The negative GNP growth is forecast to last only two quarters, with a maximum quarterly decrease of 2.4 percent. However, the equipment investment component of the economy is hypersensitive to interest rates and demand and will have a longer cycle of decline, consisting of three consecutive negative growth quarters. The Dataquest forecast shows equipment investment declining to negative 14.5 percent annualized growth in the second quarter of 1990 before beginning recovery in the third quarter. Purchases of computers, peripherals, and telecommunications equipment represent about 45.0 percent of U.S. equipment investment spending, and while they are more resistant to recession than many capital items, they will still be affected adversely by an economic slowdown.

As discussed in the *Economic Outlook 1988-1989*, Dataquest sees little prospect for significant improvement in the U.S. federal budget deficit through 1990, regardless of who become the new occupants of the White House and congress. In an election year, no one in Washington expects to gain any votes with tough talk about the deficit. After the election, there will be strong bipartisan interest to increase spending in a number of domestic areas that have seen lean times over the last eight years, such as health care, drug enforcement, environmental issues, and construction. The most likely budget scenario through 1989-1990 is one in which new program increases are balanced by raising personal income tax ceilings, elimination of some existing personal tax credits, increasing consumption taxes on tobacco, alcohol and gasoline, and modifying the corporate tax structure. Some programs that might otherwise have been federally funded, such as child care and worker retraining, will be shifted to corporate shoulders.

Dataquest projects federal deficits of $166 billion in 1988, $160 billion in 1989, and $145 billion in 1990, measured in current dollar terms. Figure 12 shows the 1976 to 1987 federal budget history, and projects the budget picture through 1990.

While Dataquest sees no perceptible slowdown in federal spending for computers, peripherals, and telecommunications equipment in civilian programs, the outlook is not good for the military budget. There is growing congressional sentiment for cuts of as much as 20 percent in the Pentagon's current annual spending level of $300 billion. Dataquest projects that the military's budget will be held to no real growth over the next two to three years. Our recommendation to related industries is to diversify into more commercial applications where possible, and into international markets where opportunities present themselves.

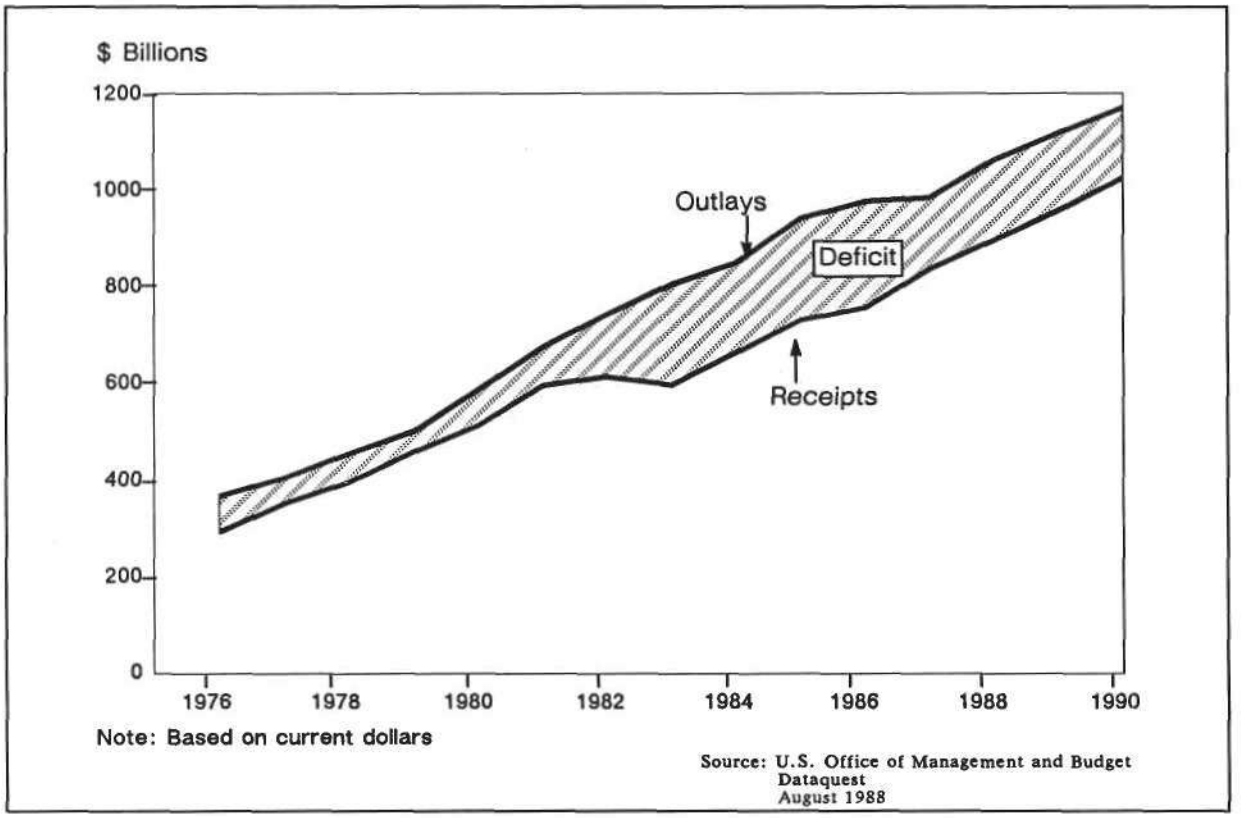

Figure 12. Federal Budget Receipts and Outlays—1976-1990

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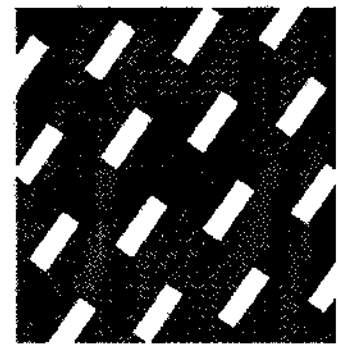

Economic Outlook 1988–1989

Dataquest
a company of
The Dun & Bradstreet Corporation

Published by Dataquest Incorporated

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April 1988

Executive Preface

Why You Should Take an Hour to Read This Report

We are entering an era of global markets. The electronics industry is a primary force in the creation of this era, and this is the same industry that stands to profit the most from it. Successful businesspeople in this era will add two new skills to the traditional set:

- They will understand the appropriate uses of technology in their field.
- They will anticipate opportunities and competitive moves on an international basis.

Every business and every individual will be influenced by global economic events, willingly or not. Some effects will be more obvious or dynamic than others. Regardless of whether the decision is where to design system software or where to open the next sales office, an understanding of economic factors is fundamental to the specific business skills needed for success.

This report is written for Dataquest clients. About 60 percent of the material concerns the United States, and 40 percent relates to major U.S. trading partners and markets. The report summarizes events leading to the current position of the United States in the world economy. For the future, economic trends and forces are described that will directly affect both global and domestic markets for electronics industry products in 1988-1989.

The most significant forecasts in this document are as follows:

- United States real economic growth in 1988 will be similar to 1987 at 2.8 percent; but 1989 will be slower, particularly in the second half. Consumer and government spending will continue to weaken, but export trade growth will compensate for a large part of these declines.
- 1989 federal tax increases and congressional legislation will have little real effect in reducing the federal budget deficit.
- Structural shifts in the United States economy will tend to stabilize wage and employment rates. The largest contribution to inflation in the United States will come in the form of consumer spending for imported goods.
- The focus of international trade for the United States will sharpen on the Pacific region, which accounts for 60 percent of its trade deficit and only 20 percent of its export markets.
- The most positive domestic prospects for 1988-1989 among major U.S. trading partners belong to Japan, Canada, the United Kingdom, and Italy.

Much of the macroeconomic data presented in this report is used by Dataquest analysts to put together specific industry market forecasts. As informed Dataquest clients, your understanding of this material will enhance the information value of every Dataquest service.

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Introduction

As the end of the 1980s approaches, a new economic era is dawning. Global markets are becoming a reality, with electronics, steel, and automotive products leading the way and providing new opportunities on an unprecedented scale. Yet these developments are also making the economic relationships between nations, industries, and markets increasingly complex. As a result, there is a rapidly growing need for accurate insights and sources of information to improve marketing, planning, and decision-making within the electronic industry.

Change is rarely painless, since it requires doing things differently from the way they were done in the past. In particular, the structural economic changes of the 1980s are increasingly forcing analysts and managers to focus their research more on current conditions, since historical trends have become less meaningful. Evidence of this can be clearly seen in the daily newspapers. The most closely watched indicators of economic activity today are the dollar exchange rates, interest rates, international stock and commodity markets, and consumer spending and sentiment. The one characteristic these variables all share is their short-term volatility.

Given this constantly changing environment, one way to achieve a clearer U.S. perspective is to focus on the realities of the marketplace as viewed by the actual participants—businesspeople in large and small companies across the country. Dun & Bradstreet, Dataquest's parent company, makes important contributions toward understanding current trends with its quarterly surveys of business expectations.

For example, D&B post-stock market crash surveys of sales expectations for 1988 showed levels of optimism equal to the high levels of 1985 through 1987. In another D&B post-crash survey of corporate buyers, roughly 75 percent of the respondents said that their capital spending plans were not affected by the October stock market slump. A third year-end survey of 1,500 plant managers showed an immediate but small reduction in 1988 production plans.

In formulating Dataquest forecasts, we utilize many of the D&B business surveys. The perceptions of Main Street are substantially more important than those of Wall Street. Given the insights provided in part by these survey results, our economic forecast for 1988 of 2.8 percent growth expected in the inflation-adjusted gross national product (GNP) reflects a pace of activity that is similar to 1987. Looking further ahead, we expect U.S. economic growth in 1989 to be about 2.2 percent, with the first half of the year showing more strength than the second half.

Growth in 1988 will be driven by significantly different factors from those of recent years. A brief overview of these factors and the circumstances leading to their emergence is presented in the next section. For reference, key economic statistics appear later in this document.

The 1980s in Review

To a great degree, the economic events of 1987 represent the culmination of a number of trends that have been developing throughout this decade.

Inflation was undoubtedly the most dominant issue in terms of shaping the U.S. economy in the early 1980s. Oil prices and high wages forced double-digit increases in the consumer price index in the beginning of the decade, reflecting problems created in the late 1970s. High real and nominal interest rates were exacerbated by a large dose of Federal Reserve tightening, which sharply limited the supply of loanable funds in the economy. The recessions in 1980 and 1982 were the price that was paid to end this wage-price spiral.

During the early 1980s, three key events occurred that played major roles in shaping today's economic environment:

- First, President Reagan's massive individual tax cuts took effect. The average tax rate on taxable personal income fell from 13.2 percent in 1981 to 11.1 percent in 1984. With only a minor slowdown in federal

spending, the federal budget deficit, which had been almost nil in 1979, exploded to 5.2 percent of GNP in 1983 and now hovers in the 3.4 percent range.

- Second, the pattern of financial deregulation that started in the late 1970s began to influence money and equity markets in significant ways. New financial institutions and instruments began to offer individuals and firms a wide range of competitive investment choices.
- Third, technology began to have a profound impact on business information processing and communication during this period. Through the application of information technology, financial institutions expanded through the scope and sophistication of their analyses to interpret and evaluate vast amounts of macroeconomic and microeconomic data. Stock markets began to react in unison to global economic events. The more aggressive businesses began to apply technology to sharpen their control of "mission-critical" sales, manufacturing, and customer service activities.

The tax cuts served as the starting gun that set the U.S. economic expansion off and running. America rapidly emerged as the engine of economic growth for the industrialized world. The United States, with its relatively high interest rates, strong domestic markets, and sophisticated financial infrastructure, became a magnet for foreign investors. As a result, the dollar exchange rate soared and prices of imported goods in the United States fell.

In response, U.S. consumers flexed their increased disposable income muscles, courtesy of the Reagan tax cuts, and voraciously bought these low-priced imported goods. Unfortunately, this was not what was intended. The tax cuts were designed to stimulate the U.S. economy by increasing disposable income and, hence, demand for *domestically* produced goods. However, consumers found better value in imports, and the dollars flowed both into the U.S. economy and abroad. At the same time, savings as a percentage of disposable income fell from 7.5 percent in 1981 to about 3.6 percent in 1987, due to new and convenient ways to borrow. By comparison, the Japanese savings rate is 17.5 percent, and most Europeans average about 14.0 percent.

In capital markets, savings must necessarily match investment. Given the shortage of domestic savings and an excess demand for capital by both consumers and government, foreign capital filled the void. In September 1985, this instability was formally recognized by the finance ministers of the G-7 industrialized countries (Canada, Germany, the United Kingdom, France, Italy, Japan, and the United States), and efforts were initiated to systematically devalue the dollar.

The goals of the devaluation were to discourage U.S. consumption of imports by raising imported prices, and to make U.S.-produced goods more competitive abroad.

This devaluation has succeeded in stimulating U.S. exports. In terms of volume, the U.S. trade deficit has started to improve slightly, but a turnaround has yet to occur in terms of current dollars, because import price increases have compensated for the decline in demand. Meanwhile, U.S. export prices have been flat, indicating that current export markets are both highly competitive and somewhat weak. U.S. exports on a constant-dollar basis increased 17.5 percent in 1987, while imports were up only 3.1 percent. Which U.S. industries led the export surge? Many of the same ones that had suffered earlier—textiles, paper, and agricultural products. Others are also the most visible beneficiaries of American productivity and quality improvements—metals, chemicals, aircraft, machinery, instruments, and computer equipment.

However, the earlier import wave has left the United States in 1988 in the position of a debtor nation after 50 years of creditor status. American assets owned by foreigners exceed the value of foreign assets owned by Americans.

Other factors make a shift in the U.S. balance of trade an uphill battle. For example, goods from newly industrialized countries (NICs), such

as Taiwan and South Korea, are increasingly being substituted for other import sources, such as Japan. The dollar has fallen relatively little against the currencies of many of these countries. In other cases, such as Mexico, the dollar has appreciated. As a result, NIC products are still a bargain when priced in dollars. So, while the mix of trading partners has changed, the U.S. trade deficit has not yet been substantially reduced. The Japanese have held onto a major piece of the action by setting up plants in Taiwan and Singapore, for example, and by building their products with low-cost components from these countries.

In recognition of this shift in manufacturing sources, the United States has increased pressure on NICs to revalue their currencies. However, NIC revaluations constitute a two-edged sword. Although imports would indeed become more costly in the United States, many of the current international sources of inexpensive goods and labor would also be eliminated. The result would be increased inflationary pressures on the U.S. economy.

To summarize, the 1980s to date have been characterized by consumption-driven growth of the U.S. GNP. Though trade improvements contributed to final demand early in the decade, by 1983 the swelling trade deficit began to have a negative impact on U.S. economic growth, an impact that was overshadowed only by the exuberant levels of consumer spending. Nevertheless, the current expansion is now 64 months old and continuing, the second longest expansion in the post-war period.

Figure 1 shows the shift in factors that contribute to U.S. economic growth. This illustration clearly shows that growth in the mid-1980s was exceptional, despite the tremendous drag from the trade deficit. The Dun & Bradstreet forecast for 1988-1989 has real GNP growing annually at a lower rate compared with the initial phases of the current expansion. Consumption growth also is expected to be lower in the years ahead, but will remain on par with growth in the '60s and '70s. Meanwhile, contributions to GNP from improvements in trade will help to offset a large part of this reduction in consumer-spending growth.

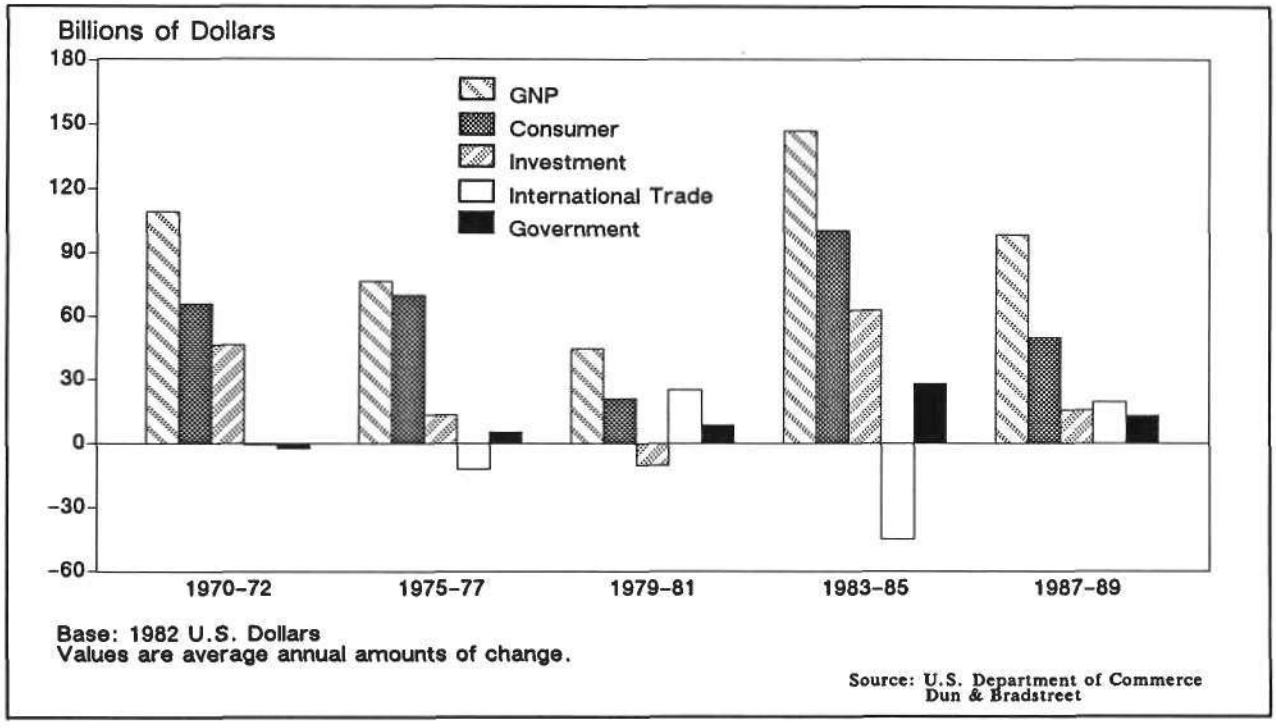

Figure 1. Components of U.S. Real GNP Growth

Key Factors in the U.S. Economy of the 1990s

The key issues for the future are the trade and federal budget deficits, and the steps that will be taken to reduce them. Reducing the federal deficit will, in the long run, reduce U.S. demand for capital, thereby relieving upward pressure on interest rates. However, for the near term, measures to reduce the federal deficit will hurt industries and individuals directly dependent upon the federal government.

Cutting the trade deficit will be more difficult. Basically, the deficit can be reduced by increasing exports or decreasing imports, with export growth having far more beneficial side effects. Currently, 90 percent of all American manufacturers concentrate exclusively on the domestic market. To enlarge their horizons and expand exports, of course, it is essential for U.S. manufacturers to develop export markets. Overseas market development requires development of the fundamental skills, with an international accent:

- Thorough market research
- Products designed with the features to appeal to those markets
- Professional sales and service organizations
- The capability of delivering those products on time at the right price

U.S. manufacturers can hope to be the beneficiaries of any further erosion of the dollar's value, or they can pursue a more aggressive strategy of improving their industrial productivity, and so reduce unit costs.

Productivity gains require that capital spending must increase, and that other input costs, such as labor and scrapped material, must decrease as a percentage of the total. Federal policies must be put into place to stimulate investment and induce individuals to save rather than to spend. This is crucial if the United States is to increase domestic sources of investment funds. In addition, some of this reduced consumption would inevitably lower the volume of imported goods, further helping the trade deficit. The forecast is for very modest increases in personal savings rates, from a 1987 level of 3.7 percent of disposable income to about 4.0 percent in 1988-1989.

To the extent that U.S. domestic spending is curtailed, many production-oriented businesses must find growth opportunities outside the United States. There are many emerging opportunities in Asia, Europe, and the Americas, but U.S. companies will have to adapt their products and sales strategies to compete effectively outside the familiar domestic arena.

Demographic shifts will also occur in the '90s as they have in each decade in the postwar period. Household formation will slacken as baby-boomers reach their thirties and forties. The demand for starter housing will ebb, being replaced by a market for step-up homes. Dual income households will increasingly dominate spending trends, especially for upscale consumer items and time-saving services.

Capital investments in manufacturing automation will continue to be extended and upgraded. The shakeout of firms that have not chosen—or cannot afford—to improve productivity and quality by modernizing will continue in a bigger way. Dispersal and subcontracting of production, where smaller firms produce components for larger firms, will increase. Thus, the current trend in which new small businesses provide much of the employment growth will continue.

Dataquest's View of the U.S. Economy

In recent years, most economic analysts have compiled rather poor records in forecasting important economic developments. All a good economist can do is to assimilate as much information as possible, and interpret it with the maximum amount of skill. However, the major structural changes occurring in the U.S. economy in conjunction with international events

make it difficult to foresee major developments and dangerous to rely too much on historical patterns. Dataquest expects the U.S. economy to continue its evolution in ways that bear little resemblance to the past. Hence, analyses of historical relationships are of limited value.

Under these conditions, information directly from business decision makers and major participants in the economic system is especially valuable. It is important to grasp how business people perceive the environment and to recognize how the status of their order books directly affects their business plans.

For example, a Dun's 5000 survey at the end of 1987 asked businesses whether the October decline in the stock market and the subsequent turmoil in the capital markets affected their 1988 capital spending plans. Capital spending is a good proxy for the general health of the economy. Firms invest when they wish to increase capacity or enhance productivity, and both situations require confidence in future economic conditions.

About 75 percent of the respondents said their capital spending plans for 1988 were not affected by the October 1987 crash. The remaining respondents were unsure or said their spending plans were negatively impacted. The responses were uniform across most industries and firm sizes. The two exceptions were among the smallest firms (1 to 19 employees) and among construction companies, for reasons one might expect. Small firms typically pull back during periods of uncertainty to avoid risking their limited financial resources, and construction firms routinely turn pessimistic when interest rates appear to be heading upward. Both types of companies are the most flexible about spending plans and become conservative during periods of economic uncertainty.

The quarterly Dun & Bradstreet Business Expectations survey (See Figure 2), querying about 1,400 business people, asked executives

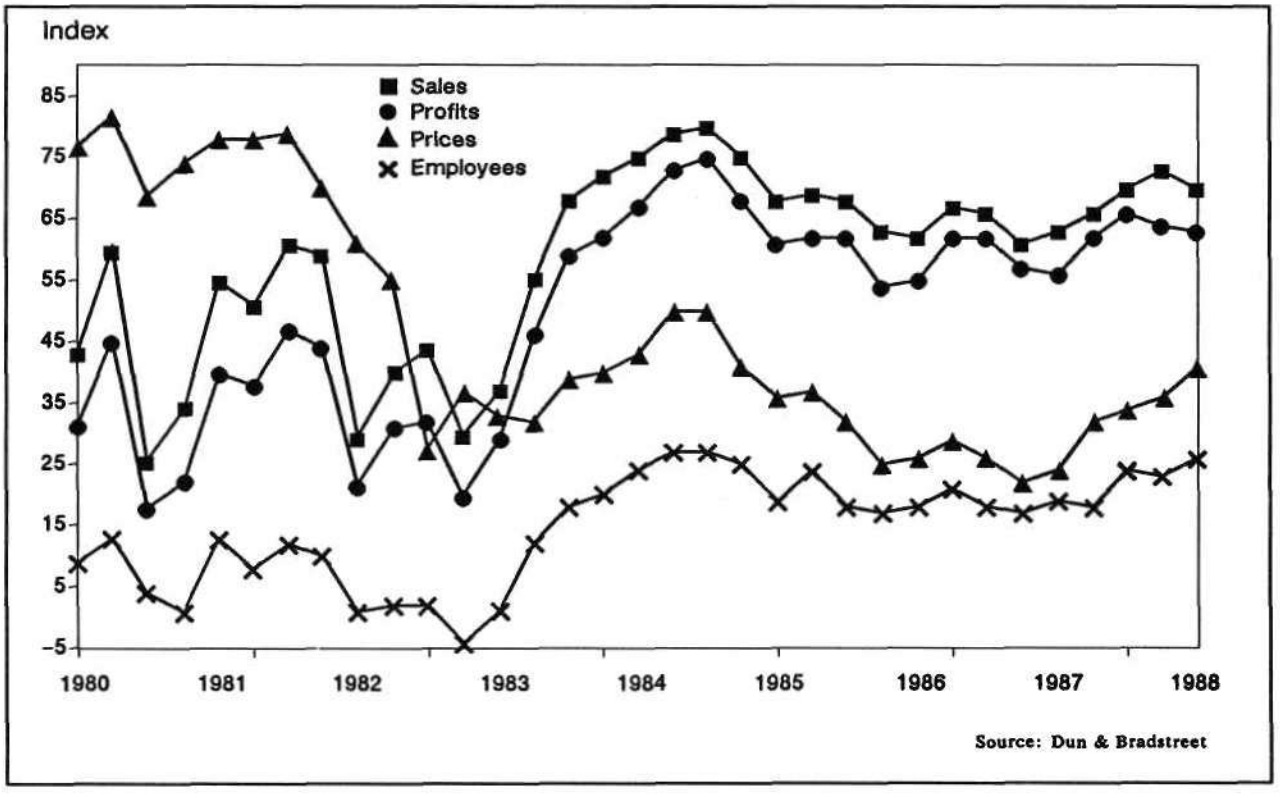

Figure 2. Dun & Bradstreet Business Expectations Survey

about their outlook for their businesses in the first quarter of 1988. The results showed that the outlook for sales and profits was down only slightly compared with their expectations for the fourth quarter of 1987, measured prior to the crash. What is more remarkable is that hiring plans for the first quarter of 1988 actually increased compared with plans in the fourth quarter of 1987.

The survey also showed an increase in the number of executives anticipating price increases in the beginning of 1988. Several inferences may be made from this. First, prices usually increase during periods of economic strength, not weakness, so comparatively few of the respondents expect a recession soon. Second, these anticipated price increases could be related to expectations of a continued decline in the dollar or concerns over an expansionary trend in monetary policy, both of which could increase inflation down the road. Lastly, given the recent rise in prices of many imported goods, some firms will seek to exploit this reduced competition by raising their own prices.

Dun & Bradstreet's statistical series on business starts and failures are two other key sources of insight into U.S. economic trends. Regional and industry breakdowns provide information on the business environment that is not easily available from other sources.

Business starts through November 1987 decreased 7.6 percent compared with the same period in 1986. Despite this decline, the overall level remains high, given that the current economic expansion is more than five years old. Stronger regions include the Northeast and the Pacific Coast, both of which have been strong for some time. The Midwest, with its large industrial sector, is benefiting from the surge in exports and is an emerging area of strength.

D&B data on business failures shows that the growth in bankruptcies, which had continued unabated for eight years, finally leveled off in 1987. Similar to business starts, the decrease in failures occurred in all industry sectors except agriculture and services. The increase in agriculture failures was related to tax law changes and the introduction of Chapter 12 reorganization for farmers, giving them the opportunity to reorganize rather than liquidate. Business failures in the service sector of the economy reflect the entrepreneurial quality of growth in the past few years. Overall, we conclude that the business sector is healthy and optimistic about prospects for 1988. We now will examine the factors that have shaped this outlook.

Factors Affecting the Economic Environment in 1988-1989

As noted earlier, the outlook for 1988 is for continued moderate growth of 2.8 percent. However, this growth will come more from improvements in trade and capital spending than from consumers. Consumer spending will be as weak this year as it was in 1987, while government spending growth will be impeded somewhat by Gramm-Rudman-Hollings expenditure cuts.

Nineteen eighty-nine growth will be a bit weaker than 1988, with the first half of 1989 stronger than the second half. Trade gains will be waning and higher interest rates will inhibit capital purchases later in the year. Consumer and government spending will remain weak. While 1989 will not be a recessionary year, the absence of any sparkling growth sectors will hold GNP expansion to about 2.2 percent in 1989.

Figure 3 shows the quarterly pattern of growth during 1986-1987. Two measures of growth are illustrated: real GNP and real final sales to domestic purchasers. Real GNP is the total of all goods and services produced in the economy. GNP includes items produced but not sold in this country. In contrast, final sales to domestic purchasers excludes unsold inventory and exports to foreign markets, while including imported goods in the total.

While GNP measures all economic activity, final sales to domestic purchasers measures only the portion of GNP that is actually spent within the

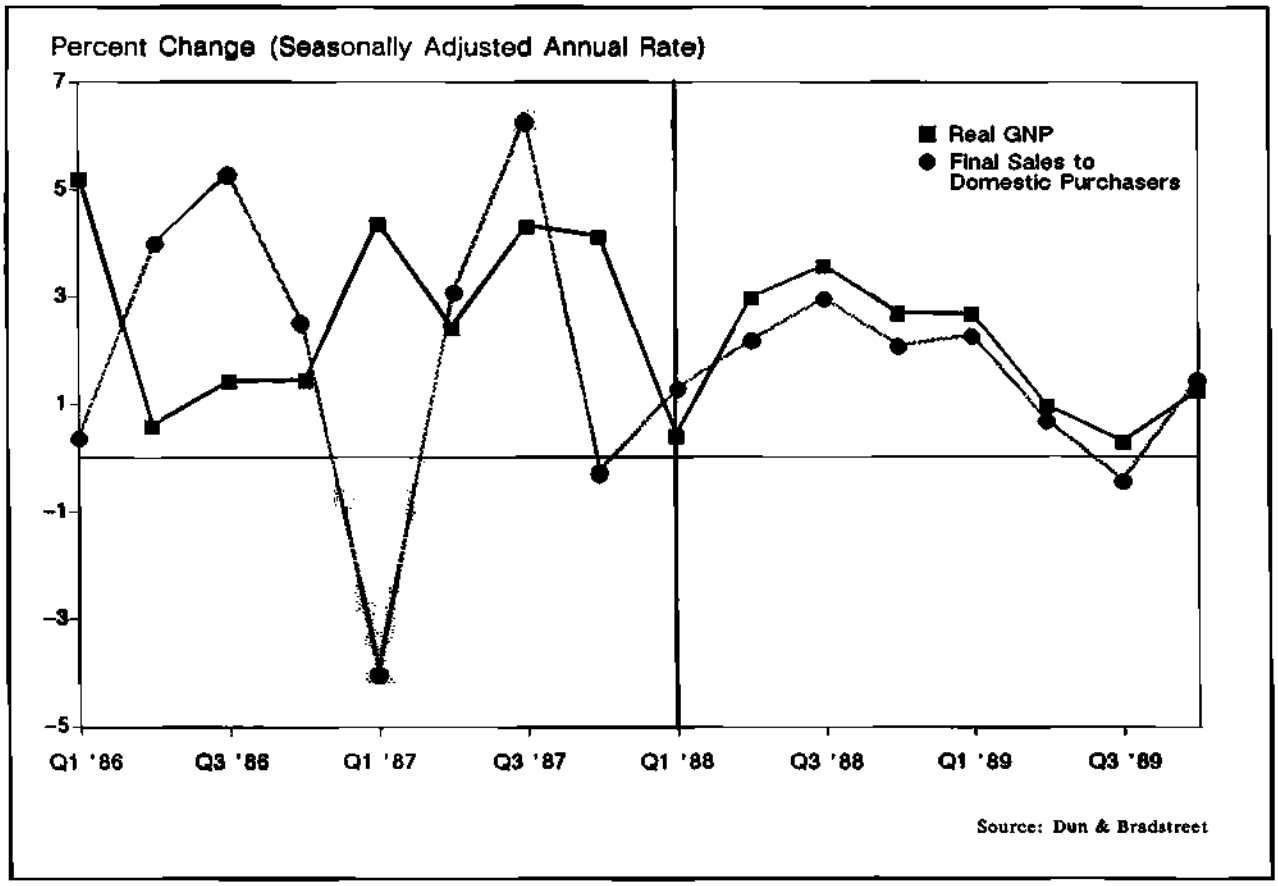

Figure 3. Forecast of U.S. Economic Growth (Seasonally Adjusted)

United States. The higher final sales measure in 1986 indicates that GNP was reduced by a degradation of the real trade balance. That is, the volume of imports into the United States exceeded the volume of exports.

The wide discrepancies between the two measures in several quarters are caused by massive inventory swings, particularly for consumer electronics, apparel, and automobiles, toward the end of 1987. When a car is built but not sold, it counts as part of GNP but not as part of final sales. The carmakers' incentive programs in the third quarters of 1986 and 1987 increased car purchases and, hence, final sales. But these cars were built earlier in each year, particularly in the first quarters, adding to GNP at that time. The important fact is that both measures of output should be used to properly gauge the direction of the economy.

The Trade Deficit and the Dollar

The trade deficit and the dollar will be among the most closely watched indicators in the next two years. Since last year's stock market plunge, the trade-weighted value of the dollar has fallen by an additional 10 percent, in addition to the more than 40 percent it had already dropped from its peak in March 1985. The dollar value now is about the same as in the fourth quarter of 1980. This stimulated export sales of price-sensitive U.S. goods and commodities, such as chemicals, lumber, and pharmaceuticals, then broadened into more durable goods and equipment.

It is important to remember that what happens in the United States as a result of a lower dollar occurs in reverse in the countries against whose currencies the dollar falls. A lower dollar means

eventual improvements in the U.S. trade balance, but leads to trade deterioration abroad. In addition, a lower dollar leads to increases in domestic inflation and interest rates. Countries whose currencies have appreciated against the dollar experience deflationary effects from cheaper imports. These countries can also reduce their interest rates because of the lower inflation.

Typically, these inflation and interest rate hikes that follow a drop in the dollar take place only after a period of several months to two years. In other words, the aftershocks of recent falls in the dollar will probably occur after the 1988 election.

In the meantime, the Federal Reserve System can either support the dollar or fix interest rates at some antirecessionary level. These objectives are contradictory because interest rates are used as a tool to attract foreign funds into this country, ultimately affecting the dollar exchange rates. Immediately after the stock market crash, the Federal Reserve Board allowed the dollar to drop, preferring to encourage lower interest rates to ward off adverse effects of the crash. In pursuing this policy, bank reserves were increased to make certain that the stock market crash did not result in a liquidity crunch.

Because of the dichotomous monetary policy goals of the Federal Reserve Board, Dataquest assumes the Fed will walk a tightrope, trying its best to avoid a recession while also attempting to achieve stable dollar exchange rates. As a result, the best the Fed can do is to achieve partial success on both fronts. Interest rates will slowly edge upward, while the dollar will continue to decline, albeit at a much slower pace, bottoming out in the second half of 1989.

This policy can succeed only with international support and coordination. If other countries such as Japan or West Germany reduce their interest rates, this also reduces upward pressure on U.S. interest rates. This eases the Fed's balancing act. Such economic stimulation from abroad can help solve the U.S. trade imbalance by increasing worldwide demand. The key point, however, is that U.S. producers *must* capture the lion's share of any new demand. The current U.S. share of world markets is about 13 percent. To eliminate the U.S. trade deficit solely by increasing exports would require this share to double. Some U.S. import restrictions would seem to be inevitable.

On the import side, the dollar's 50 percent drop over the last three years will eventually channel U.S. demand away from imports and toward domestic goods as the price advantages of U.S. producers become more pronounced. Figure 4 illustrates a forecast of 7.9 percent and 8.6 percent increases in the average prices of imported goods in 1988 and 1989, stemming from continued erosion in dollar exchange rates. Government policies that encourage increased levels of saving and investment can go far to reduce import demand.

Clearly, many economic and political events have to occur to achieve improvements in the U.S. balance of trade. However, U.S. businesses must take upon themselves the responsibility for changes to their own internal cultures and attitudes in order to be successful internationally. Attention and effort must be directed toward selling a higher percentage of U.S. production abroad rather than domestically, even in circumstances when demand in the U.S. market is strong. American industry would do well to follow the example of U.S. computer and semiconductor manufacturers, and seek ways to pool commercial R&D resources in cooperative efforts to perfect manufacturing technology and regain a competitive edge.

The free trade agreement signed January 2 by President Reagan and Prime Minister Mulroney is intended to gradually phase out all trade barriers and investment restrictions between the United States and Canada, the world's largest trading relationship. The agreement is currently being converted to legislation for review and ratification by Congress and the Canadian Parliament. Although some industries and regions on both sides of the border will have to make adjustments, the agreement has a 10-year implementation period for that purpose. The net result will be significant bilateral market development, particularly for Canadian lumber and apparel and U.S. investors.

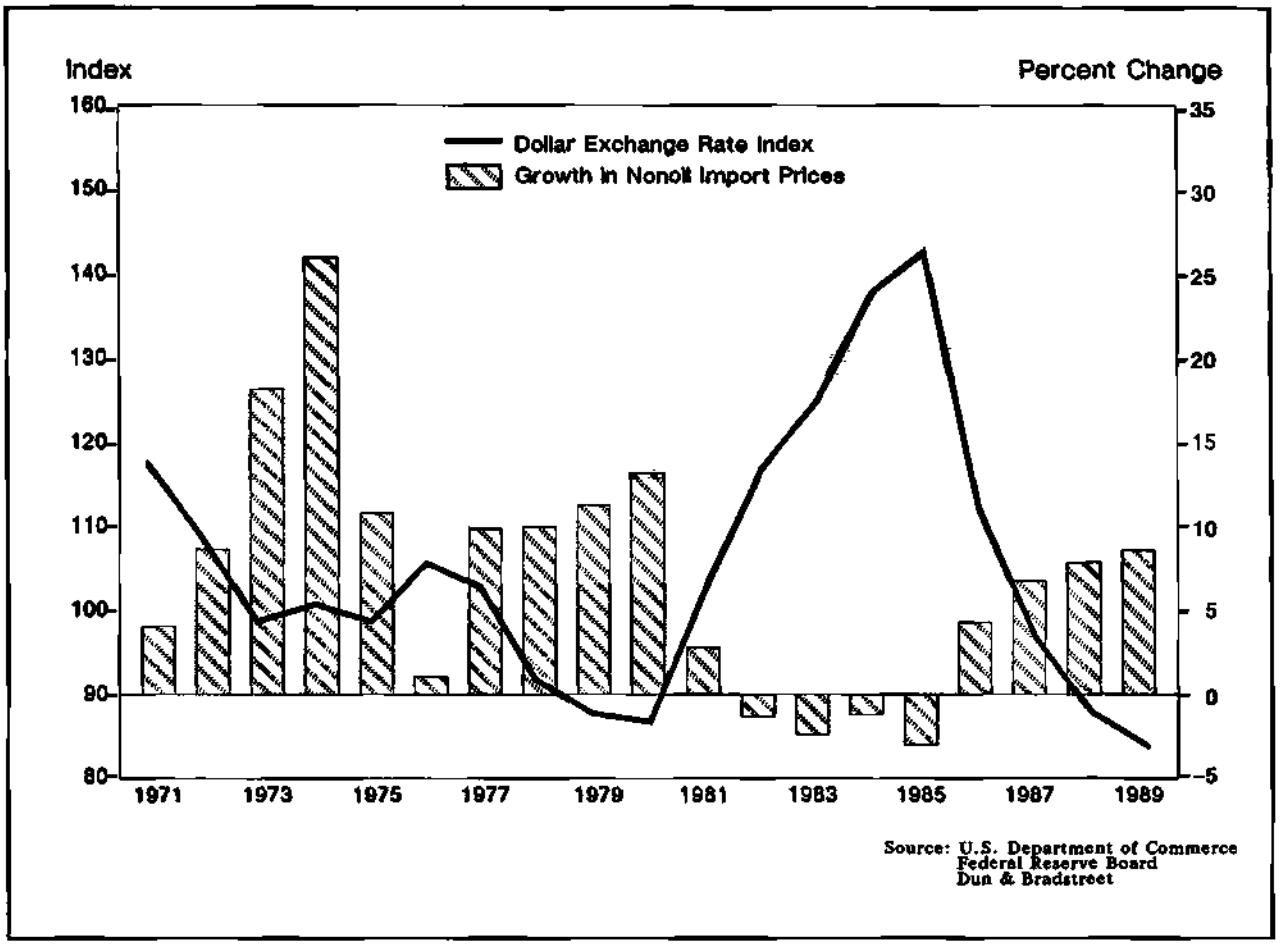

Figure 4. Imported Inflation and the Dollar

It is interesting to speculate on the free trade agreement and the prospect for an eventual North American common market encompassing Canada, the U.S., and Mexico. Figure 5 shows the 1987 U.S. balance of trade with Canada and Mexico. The elimination of import tariffs on goods traveling between the three countries would most directly benefit Canada and Mexico, which ship 80 percent and 75 percent of their respective exports to the United States. By comparison, the United States sells 25 percent of its exports to its bordering neighbors. The primary benefits to the United States would be freer commercial investment opportunities, a favorable climate for development of lower-cost manufacturing operations close to home, and preferential pricing on Canadian and Mexican petroleum.

Interest Rates, Bonds, and the Stock Market

The large federal deficit has created a global market of considerable size in U.S. Treasury securities, a market which recently has more movement and effect on monetary policy than the Federal Reserve Board. Government bond rates rose beyond 10 percent in early October, responding to a booming global economy, and helped to trigger the stock market meltdown. Bond prices dipped and then recovered immediately after the crash, as the Federal Reserve's flood of liquidity pushed interest rates down again.

While the long-term relationship between bonds and stocks is tenuous, the two instruments currently interact closely. As money flows from

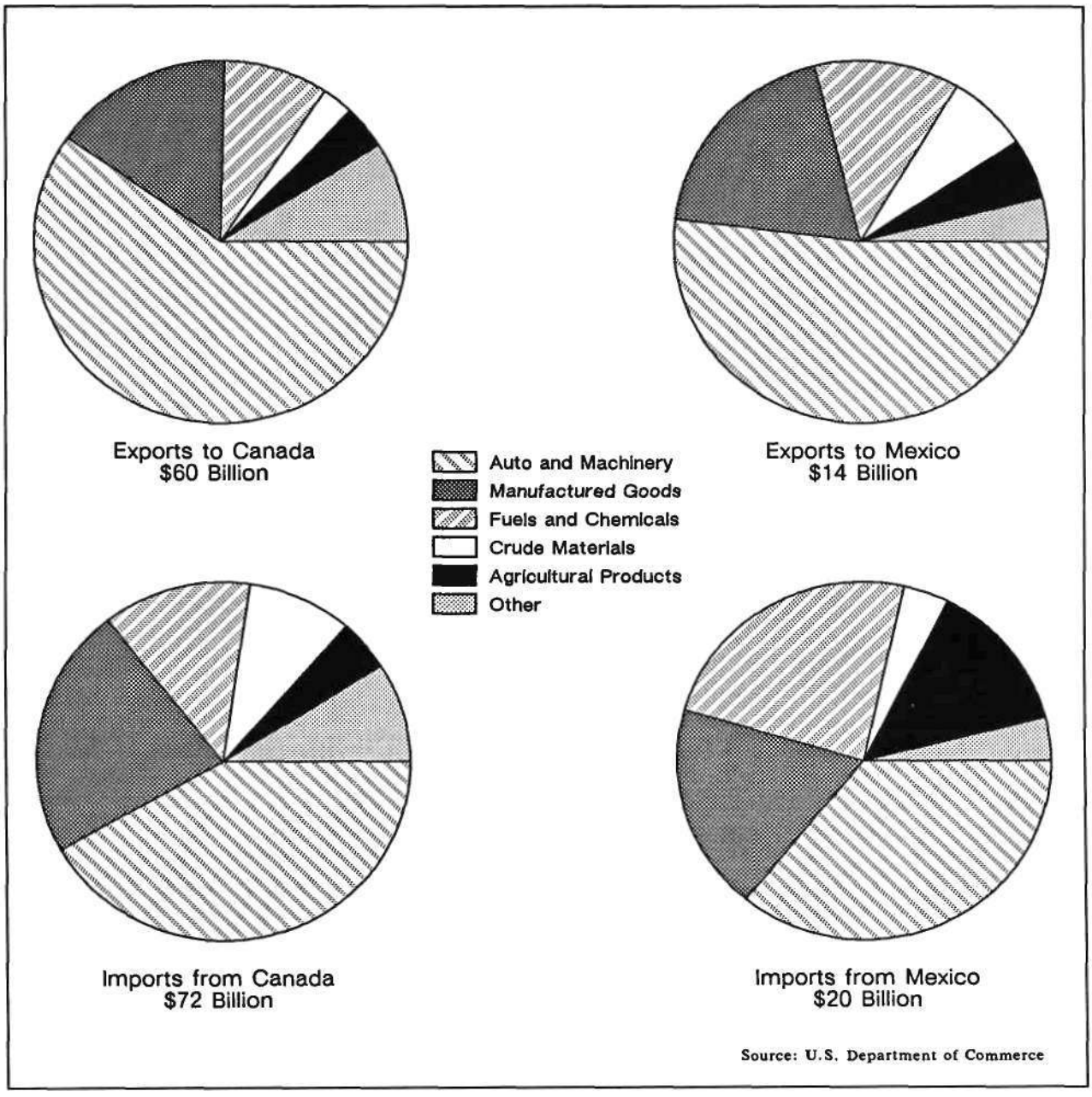

Figure 5. U.S. Merchandise Trade with Canada and Mexico—1987

stock markets into bonds, the price of stocks fall, raising the price of bonds and lowering bond yields, i.e., interest rates. Psychological factors play a big role in this relationship, too. If negative expectations about the economy form, then downward expectations about interest rates and stock prices follow, and the demand for bonds increases.

Thus, the bond market also serves as a handy economic buffer. When the total market value of the U.S. stock market fell by about $1 trillion from an original total of $3 trillion in last year's fourth quarter, the value of bonds increased about $700 billion, representing a 10 percent gain on a $7 trillion base. This may help explain why businesses and consumers

remained relatively calm in the weeks after the crash.

Expectations for continued declines in the dollar and a subsequent increase in inflation suggest interest rates will rise over the next two years. Long-term bonds, which currently yield just over 9.0 percent, should yield between 9.5 and 10.0 percent by the end of the year, and between 10.0 and 10.5 percent by the end of 1989. Risk factors that might increase rates beyond these ranges include higher inflation rates or a rebound in the stock market, which could drain liquidity from bonds. About the only source of downward pressure on interest rates is a recession or "growth pause" in final demand, reducing the demand for loanable funds.

The Federal Sector: The 1988 Election and the Budget Deficit

Given the lagging consequences of actions taken in 1986 and 1987, the direction of the economy in 1989 depends very little on who occupies the White House and Congress, especially considering the start-up period of several months required before a new administration can begin to implement its own policies.

Gramm-Rudman-Hollings restrictions on federal spending will also hinder the implementation of new policy initiatives. The distribution of the Gramm-Rudman-Hollings cuts, or of any avoidance measures, may vary depending on the party or person in power. However, any cuts will probably net out to elaborate accounting maneuvers rather than real spending reductions.

The Gramm-Rudman-Hollings budget cuts will also mean little to the macroeconomy, and very little to capital markets. The recently passed legislation calls for $30 billion in deficit reduction in fiscal 1988, and an additional $46 billion in fiscal 1989. With these cuts, the federal deficit is still likely to exceed $170 billion in 1988 and $150 billion in 1989, compared with $149 billion in fiscal 1987. The deficit reductions mean even less compared with the $2.4 trillion cumulative federal budget debt. Figure 6 illustrates the enormous bulge since 1981 in federal deficit spending.

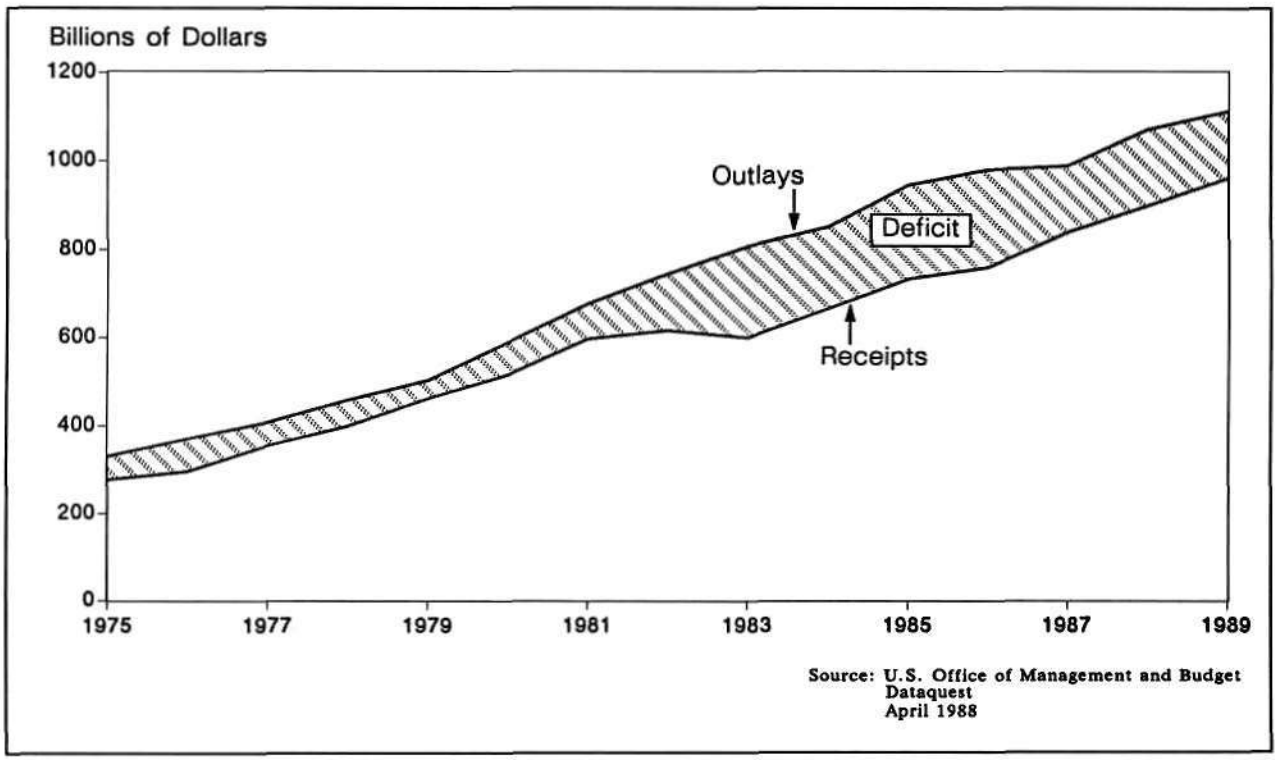

Figure 6. Federal Budget Receipts and Outlays—1975 to 1989

Since a portion of these cuts merely transfers the demand for capital from the government to the private sector, the cuts will have little impact on reducing the U.S. demand for capital and, hence, little impact on interest rates. For example, private acquisition of federal assets to be sold in the deficit reduction plan requires private financing, merely replacing federal debt with individual or corporate debt.

Difficult budget decisions have been postponed to the future. Eventually, elected officials will have to address out of balance national entitlement programs such as Medicare and Social Security that consume 9.5 percent of the GNP.

Thus, any economic fallout from the federal sector will probably be psychological. Until the 1988 presidential election is decided, and the winner's policies become clear, there will be a cloud of uncertainty surrounding the outlook for the economy. To the degree any leading presidential candidates propose a peculiar or uncertain economic or political agenda, this uncertainty may add a downbeat note to the economy.

The Consumer

In the measurement of U.S. GNP, consumer spending accounts for about two-thirds of the total. The economic realities of the late 1980s are affecting three primary factors that have a direct impact on the consumer—personal income, debt, and psychology.

The first and most obvious factor is household income. The best measure of this is *real disposable income*, which necessarily takes inflation and taxes into account. When the second part of the 1986 tax reform act's tax cut took effect on January 1, 1988, tax liabilities of individuals were reduced by about 4 percent. Offsetting a large part of this increase was a substantial increase in social security tax payments. On balance, tax payments will be reduced in 1988, but because of the change in the Oval Office in 1989, taxes can be expected to increase thereafter.

Also affecting disposable income, of course, are wage rates. Slight increases in compensation are expected over the next two years because of gradually tightening labor markets in some regions and industry sectors. In addition, inflation is expected to rise slightly in 1988-1989, offsetting much of the buying power of these gains. Therefore, real disposable income is expected to remain largely unchanged from 1987.

Another factor that affects the consumer is *debt*. Consumer debt-to-disposable-income ratios are currently high, but can be explained in part by the increased use of credit cards over the past five years. The use of credit cards is a convenience rather than a debt purchase if the credit card bill is paid off in full each month. However, as far as the credit accounts are concerned, debt is debt, even though consumers may not regard it as such.

The explosion of home equity loans and adjustable rate mortgages have in the past provided consumers with reduced interest rates for debt payments of all types. However, this debt involves flexible rather than fixed interest rates, and so ties debt payments more closely to current interest rates. Thus, if interest rates increase, more current income would be required to pay off old debt, reducing consumption growth.

The net effect of consumer debt on expenditures remains a complex issue. Compounding the problem of analysis is the third factor affecting consumption decisions: *consumer psychology*. What is certain is that consumers are less likely to incur debts if they have doubts about their future prosperity.

If consumers fear a recession is coming, they will withhold spending in favor of increasing savings as a hedge against bad times. Because the economy is in a period of notable transition, there is a great deal of uncertainty. The University of Michigan conducts regular surveys of consumer attitudes, and the results provide some insight into spending plans. Figure 7 shows historical values for consumer sentiment and spending, with projections for 1988 and 1989. The survey's consumer sentiment index took a large dip immediately after the October crash,

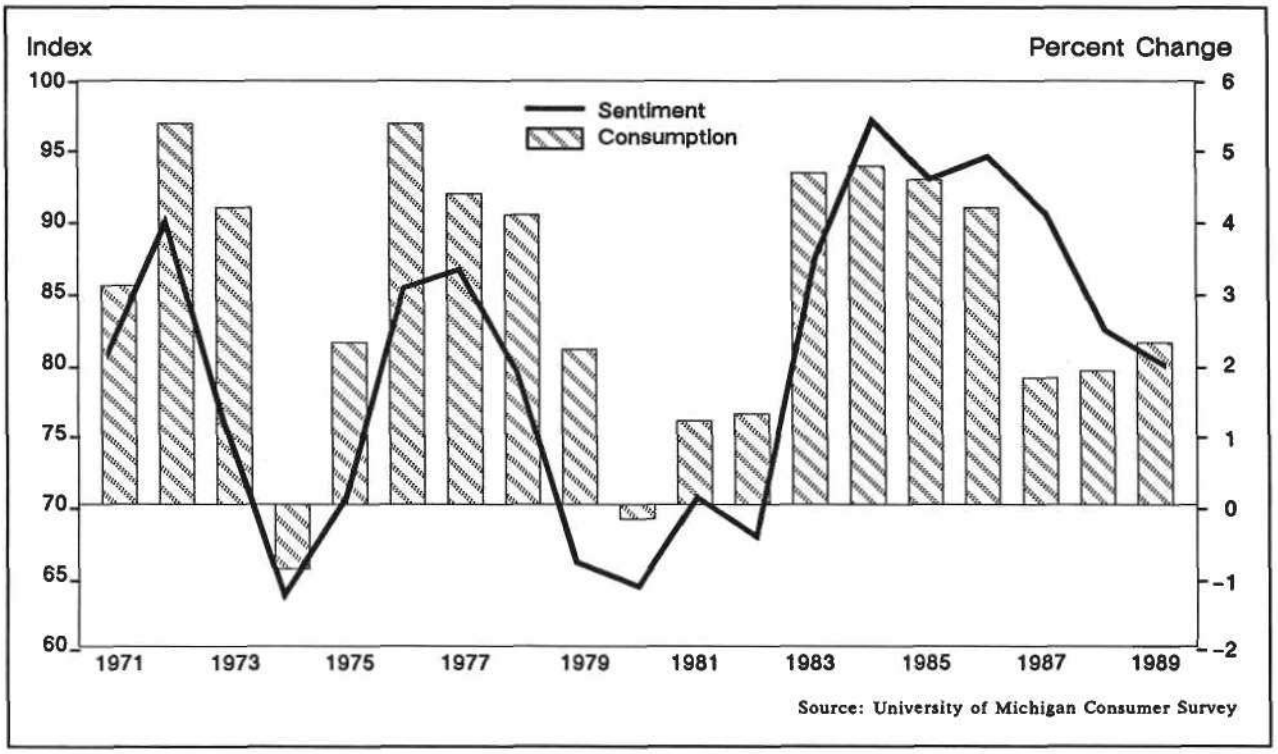

Figure 7. U.S. Consumer Sentiment and Consumption

stabilized in November, and then rose modestly in December. The resiliency evident in consumer sentiment makes it likely that changes would occur only after sustained stress or sustained improvement in the general economy.

The outlook for consumer spending is weak, but not weak enough to cause a recession. While GNP is expected to grow 2.8 percent in 1988, consumption is anticipated to grow only 2.0 percent. Dataquest views this as a favorable trend for two reasons:

- Roughly 21 percent of U.S. *merchandise imports* in 1987 were consumer goods, and another 21 percent were automobiles and auto parts. Therefore, a cutback in consumer spending would clearly help reduce the U.S. trade deficit.
- Because income must be either spent or saved, a reduction in consumer spending means an increase in savings, which flow back into capital investments in plant and equipment. Capital investments will be necessary to expand production capacity for export.

Consumer spending reductions will help hold prices and inflation down, and will restrict further excesses in the level of American personal debt.

The Household Balance Sheet

An analysis of consumer spending requires a brief examination of the health of the consumer. A look at the balance sheet of households—total assets and liabilities—can provide insight into the longer-term trends of consumer behavior.

This is especially important today because much has been written about the so-called "wealth effects" of the stock market decline killing off personal spending. Scant empirical evidence is available to support the view that wealth effects

are important, and there are many arguments against this type of forecast:

- If wealth effects indeed exist, there would have been a surge in spending when the stock market was on the way up during the first nine months of last year. Consumption expenditures were flat during this period.
- The period in which wealth effects are measured is likely to be quite long. It is doubtful that individuals would make consumption decisions on potentially fleeting paper profits.
- Only 20 percent of individuals own stock. Many of these individuals are either long-term investors who ignore short-term fluctuations, or simply are well enough off to withstand the stock market's bearish intervals.
- Much of the lost wealth in the value of stocks was made up by the gains in the bond markets.

These arguments imply that the long-term health of the consumer is dependent on all of the net assets of the household, not just on income flows. As a result, it is necessary to look at all sources of household wealth and all liabilities supported by this wealth.

Using an accountant's point of view, the ratio of household liabilities to assets has generally been stable at around 20 to 24 percent since 1960. In 1986, this ratio reached a 24 percent cyclical peak. Increases in mortgage and installment debt exceeded increases in wealth, including stocks. And in 1986, economists were forecasting a mild consumer retrenchment for 1987, which in fact occurred.

In 1987, the household liability/asset ratio dropped to 22 percent, signaling an increase in the long-term solvency of the consumer. The most pessimistic projections of lost wealth in the fourth quarter from the stock market crash would raise the liability/asset ratio from 22 percent back to the 1986 level of 24 percent.

Two conclusions can be reached from this analysis. First, based on calculations from the aggregate household balance sheet, 1988 and 1989 will see a continuation of weak spending growth, much like 1987. Second, the economy, at this time, can survive mild consumer retrenchments and still avoid a recession.

Inflation and Unemployment

Near-term inflation will be the resultant combination of three forces: oil prices, wage rates, and import prices.

Oil prices should decrease relative to the general inflation rate in 1988. This is due to OPEC's failure to reduce its overall production quotas below 17.5 million barrels per day, the lack of success in controlling unofficial discounting by OPEC members, widespread non-OPEC third-world production increases, and very small increases in worldwide demand. OPEC oil prices should average $17 per barrel in 1988, and rise gradually to about $18 per barrel by the end of 1989.

In the labor market, it would appear that the currently low unemployment rate would suggest future labor shortages if the economy expands any further, causing large future increases in wages. However, outside the Northeast, this simply is not so. With the unemployment rate at 5.8 percent, there is still room for further expansion without generating wage pressures. Since the last time the unemployment rate fell this low was in 1979, the average age of the labor force has increased. With this maturation, fewer people are changing jobs, and this job stability is reflected in the unemployment rate.

The gradual shift in the U.S. economy from manufacturing toward service industries and the trimming of corporate payrolls have reduced many potential downside effects. In addition, the focus of labor contracts has shifted from wage increases to job stability. Average annual wage increases in negotiated labor contracts are running between 2 and 3 percent. Also, new entrepreneurial activity is responsible for many new jobs in smaller businesses, which generally pay less than their large business counterparts and offer fewer direct employee benefits. Therefore, unemployment and inflation rate

comparisons with the past are not necessarily valid. We see the unemployment rate bottoming out at 5.6 percent by the end of 1988 and rising from 5.8 percent to 6.0 percent in 1989.

A major source of inflation comes from abroad. With a decreasing dollar value, foreign goods cost more. To the extent that U.S. markets see higher prices for foreign goods, U.S. competitors may also choose to raise their prices. Imports other than oil represent about 10.0 percent of GNP, so if prices for these goods increase by 8.0 percent, and if prices of substitute domestic goods increase by about 6.0 percent, this can add about one percentage point to current inflation rates. Overall, Dataquest expects inflation rates to rise through 1988 to the 4.5 to 5.0 percent range, until peaking at about 5.4 percent in mid-1989.

Capital Spending

The projected growth in capital spending is an important factor in our forecast of 2.8 percent real GNP growth for 1988 and 2.2 percent in 1989. Although the outlook for purchases of plant and equipment is influenced by many of the same considerations as consumer spending, two additional factors will make this sector a major source of growth. First, U.S. production facilities are currently running at an average 82.0 percent of capacity. The export boom, if sustained, will strain industrial capacity in many export-oriented industries and thus force expansion. Second, corporate profits in 1987 were quite strong, providing funds for investment in 1988. Much of this investment will go into equipment rather than construction because of the shorter payback period.

The pivot point in this forecast concerns interest rates. Since firms usually plan major capital expenditures many months in advance, it is unlikely that any minor uptick in interest rates would adversely affect corporate spending in 1988. The recent Dun's 5000 Survey on 1988 capital expenditure plans confirms this. In 1989, investment expenditures for larger firms would still be interest-rate insensitive up to a point. In other words, larger businesses generally pay more attention to the sales prospects for their products than to interest rates when planning their capital spending.

Financial Industries

With the declines in the stock markets, the financial sector is one of the weakest in the economy. The banking industry must deal with a weak portfolio, including large amounts of nonperforming third world debt, plus weak loans in the agricultural, energy, and real estate sectors. Higher interest rates can exacerbate these problems by raising the cost of obtaining new funds. The good news for bankers is that they are not working for Wall Street brokerage houses, which instituted 10 percent personnel cutbacks after meteoric expansion over the past several years. At the same time, many of these same firms express commitments to continue purchases of communications and data processing equipment in 1988, in order to retain their competitive position.

The risk of a potential banking crisis appears to have passed. However, because of the general economic sluggishness ahead, any turnaround will be slow. While government regulatory agencies appear to consider most bank and brokerage house problems under control, the situation remains precarious.

One additional factor to consider in this sector may come from repeal of regulatory restrictions preventing banks, brokers, and insurance companies from engaging in each other's activities. With new markets open to these institutions, an expansion followed by a shakeout of the new megabanks will occur. The end result may be a stronger industry, but the route to this end is likely to be painful.

Tables 1 and 2 contain key statistics concerning the U.S. economic outlook and GNP components.

Table 1. U.S. Economic Outlook (Billions of U.S. Dollars)

	1987	1988				1989			
		Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Nominal GNP	$4,486	$4,641	$4,723	$4,818	$4,904	$4,989	$5,060	$5,123	$5,197
% Change SAAR	7.2%	3.8%	7.2%	8.3%	7.4%	7.1%	5.8%	5.1%	5.9%
% Change Year Ago	5.9%	6.0%	6.2%	6.5%	6.7%	7.5%	7.1%	6.3%	6.0%
Real GNP	$3,820	$3,880	$3,909	$3,944	$3,970	$3,997	$4,006	$4,009	$4,022
% Change SAAR	3.6%	0.5%	3.0%	3.6%	2.7%	2.7%	1.0%	0.3%	1.3%
% Change Year Ago	2.8%	2.9%	3.0%	2.8%	2.4%	3.0%	2.5%	1.7%	1.3%
GNP Deflator	117.5	119.6	120.8	122.2	123.5	124.8	126.3	127.8	129.2
% Change SAAR	3.5%	3.2%	4.1%	4.5%	4.5%	4.3%	4.8%	4.7%	4.6%
% Change Year Ago	3.0%	3.0%	3.2%	3.6%	4.1%	4.4%	4.5%	4.6%	4.6%
Industrial Production	129.8	134.0	134.6	135.8	136.9	137.8	138.6	139.1	139.5
% Change SAAR	5.0%	3.0%	2.0%	3.6%	3.2%	2.8%	2.1%	1.6%	1.2%
% Change Year Ago	3.6%	5.6%	5.0%	3.7%	3.0%	2.9%	2.9%	2.4%	1.9%
Capacity Utilization (%)	81.0%	83.1%	83.6%	83.6%	83.7%	83.7%	83.4%	83.0%	82.7%
Unemployment Rate (%)	6.1%	5.8%	5.8%	5.7%	5.6%	5.8%	5.9%	6.0%	6.0%
Number Employed (M)	102.1	103.2	103.7	104.9	106.6	106.8	105.9	104.0	104.4
% Change Year Ago	2.5%	2.1%	2.0%	2.5%	3.2%	3.5%	2.1%	(0.9%)	(2.1%)
Real Final Sales	$3,785	$3,827	$3,848	$3,877	$3,897	$3,920	$3,927	$3,923	$3,938
% Change SAAR		1.3%	2.2%	3.0%	2.1%	2.3%	0.7%	(0.4%)	1.5%

Notes: Nominal GNP = GNP measured in current dollars
Real GNP = GNP measured in constant dollars from 1982 base year
SAAR = Seasonally adjusted annual rate
Industrial Production = Base 100 in 1977.

Source: Dun & Bradstreet

Table 2. U.S. GNP Components (SAAR*, 1982 Billions of U.S. Dollars)

	1987	1988				1989			
		Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Consumer Spending	$2,495	$2,514	$2,531	$2,556	$2,569	$2,586	$2,596	$2,608	$2,611
Nonresidential Fixed Invest	447	467	473	481	490	502	507	509	506
Residential Fixed Invest	196	195	197	196	196	193	189	185	185
Government Purchases	773	784	781	789	796	792	788	796	800
Inventory Change	42	29	24	20	16	11	14	0	4
Net Foreign Trade	(134)	(109)	(97)	(98)	(97)	(87)	(88)	(89)	(84)
GNP	$3,819	$3,880	$3,909	$3,944	$3,970	$3,997	$4,006	$4,009	$4,022

*Seasonally adjusted annual rate

Source: Dun & Bradstreet

Conclusion—the U.S. Economy

The next two years are expected to be about as strong as 1987, but the economy will rely on different sources to achieve similar levels of growth.

On the downside, there are several realistic scenarios in which a recession could develop as early as this summer. Such possibilities include a massive divestment of dollars by foreign investors, a drop in consumer confidence, or a jump in oil prices from extraordinary military developments in the Persian Gulf.

Positive risks include larger-than-expected export gains or increased international coordination to reduce interest rates, which could bring about a capital spending and housing boom.

In any event, careful planning will be required to keep pace with the evolving economy. The nature and location of markets for all firms will be changing in the next two years. Profitability will depend on the ability to exploit these changes to their fullest advantage.

1988-1989 Outlook for Major U.S. Trading Partners

Figure 8 shows the volume and composition of U.S. international transactions in goods and services during 1987, illustrating the large share attributable to imported consumer goods (15.5 percent), even excluding automobiles. The bar graphs in Figures 9 and 10 rank U.S. trading partners in descending order by value of imported goods into the United States. Three conclusions are particularly worth noting:

- Japan accounts for 36 percent of the 1987 U.S. merchandise trade deficit, and the NICs of the Pacific region account for a rapidly growing 23 percent.

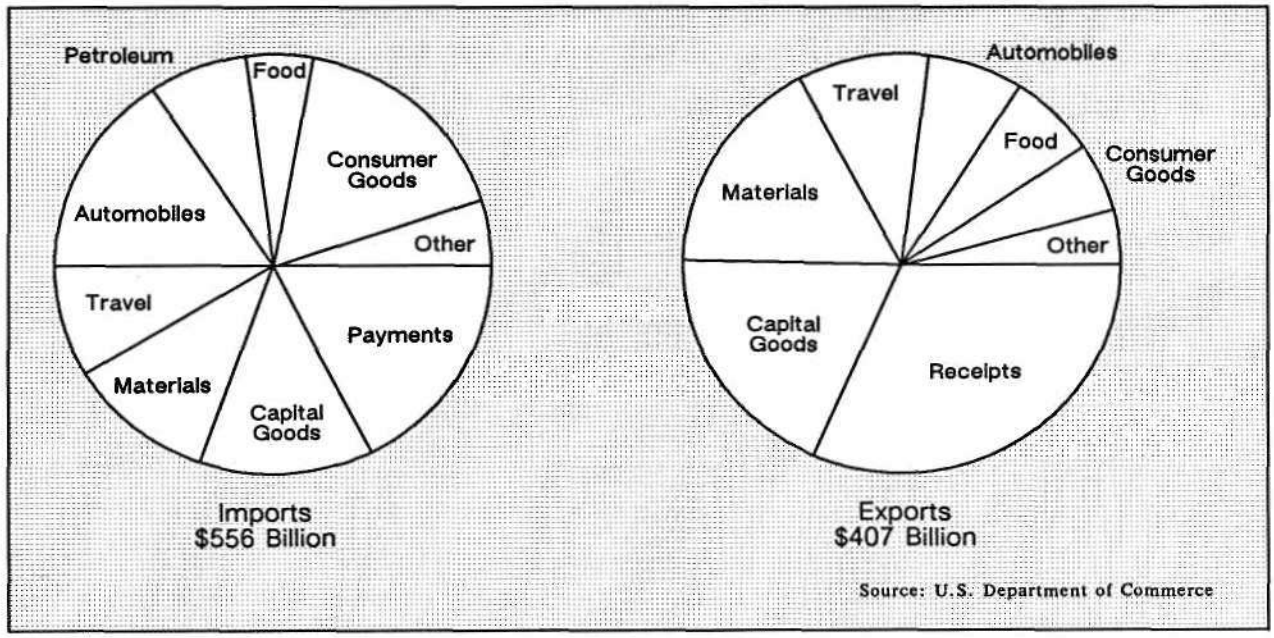

Figure 8. U.S. International Transactions—1987 ($ Billions)

- The negative aspect of the 1987 U.S. trade results, while weighted so heavily by Pacific area countries, still permeates almost all U.S. trading relationships. In scanning the list, the reader will note that the U.S. balance is negative until reaching the nineteenth area, Australia and New Zealand.
- The first- and third-ranking country-markets for U.S. exports are its bordering neighbors, Canada and New Mexico. Many of the U.S. exports to these countries are related to automotive and electronic assembly operations, the products of which are reimported into the United States.

Japan

As international markets shift toward new equilibrium points, the Japanese are reshaping their economy with increased emphasis on domestic demand as the primary driving force, and less dependence on exports. The years of 20 percent-plus export growth in the 1960s and early 1970s, which made Japan the world's largest creditor nation, are dampening to a steady 3.50 percent. Meanwhile, total domestic demand grew at 4.00 percent rates in 1986 and 1987, and is expected to continue at this rate through 1988 before slowing to 3.25 percent in 1989. This is in comparison with a healthy 3.50 percent to 3.00 percent real GNP growth in 1988 and 1989. The primary components of domestic spending are as follows:

- Sharp spending increases in 1987 by central and local governments on airport and railway construction projects, telecommunications facilities, conference centers, highways, and electric power generation and distribution networks will continue through 1988-1989. The U.S. government is seeking rights for American companies to bid on parts of the $17 billion construction and expansion program.
- Corporate capital spending plans for 1988 are moderate overall. Sizable spending in industries closely related to domestic markets, such as construction, banking, insurance, and food, will be counterbalanced by decreases in the shipbuilding, steel, mining, and automobile industries.

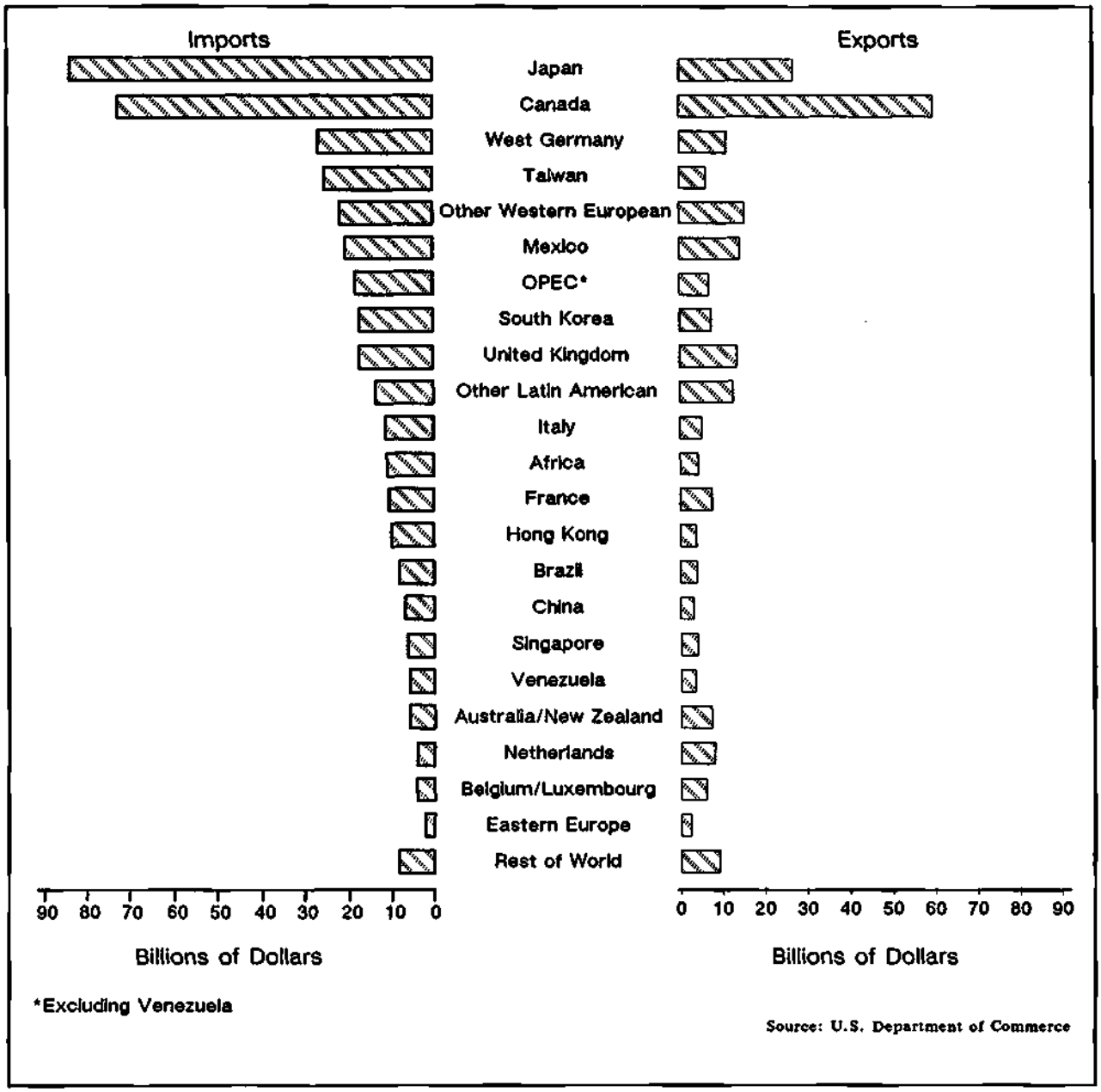

Figure 9. U.S. Merchandise Trade—1987 ($ Value, Billions)

- Modest wage increases, stable consumer prices, and historically low interest rates combined to spur Japanese consumption 3.75 percent in 1987. Consumer spending will continue to increase 5.00 percent per year through 1988-1989, primarily for housing and household goods, automobiles, and travel. To date, the benefits of yen appreciation on imported goods have been retained as profits within the complex multilayered Japanese distribution network, and have not been passed through to the ultimate consumer.

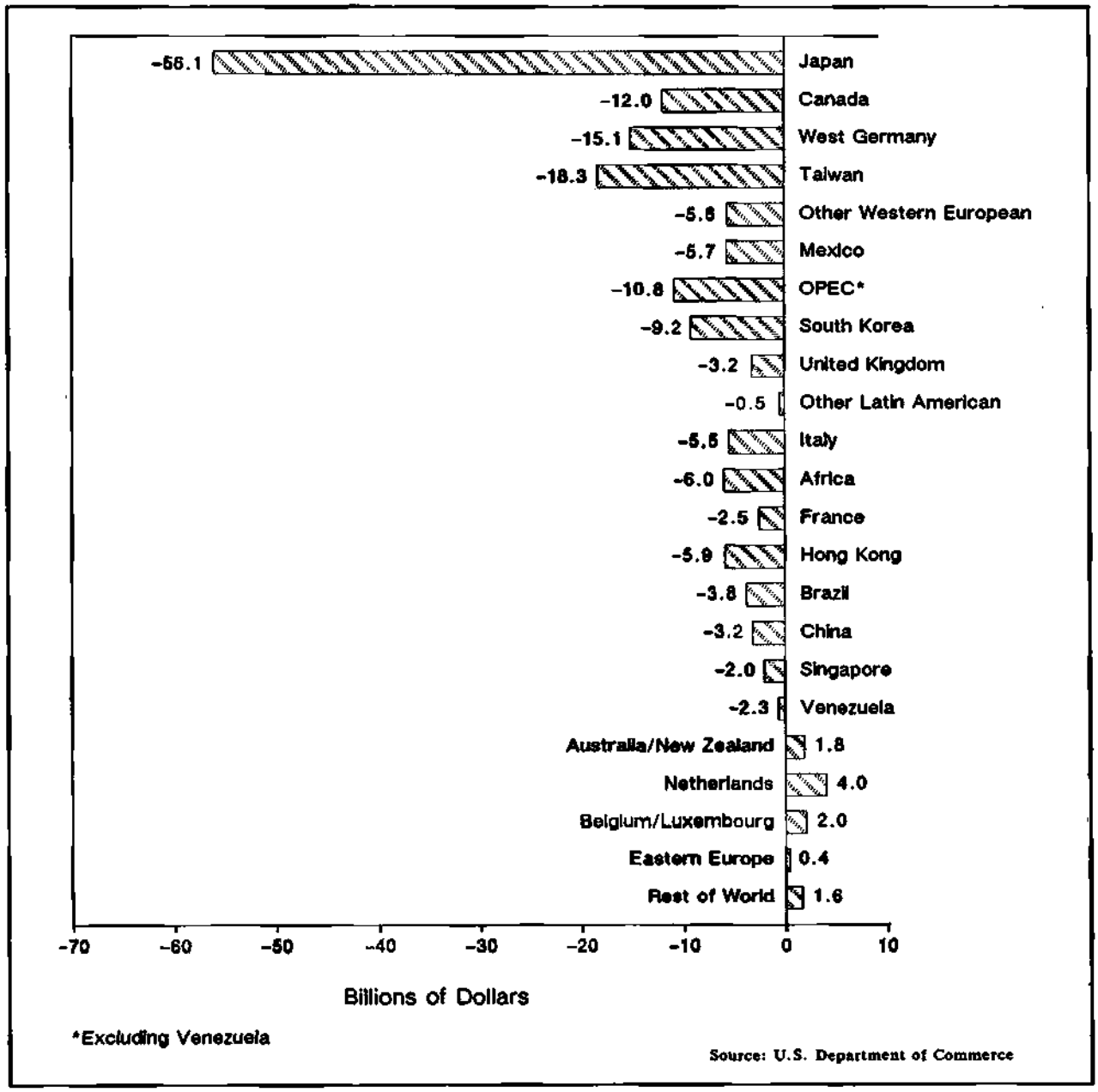

Figure 10. U.S. Merchandise Balance of Trade—1987 ($ Value, Billions)

As developing countries emulate the Japanese industrial success model, and the strong yen is a major factor in international trade balances, the Japanese face a number of pressing domestic issues.

The Japanese baby-boom generation of 1947 through 1949 numbers 10 million, about 20.0 percent greater in size than the generations just before and after. These workers, hired in the mid-1960s period of rapid expansion, are now competing for a limited number of promotions. Japan's rigid labor market still regards job-hopping as disloyalty, and pay systems are based heavily on seniority. The national unemployment rate has been steady at 2.8 percent.

Consequently, there is growing corporate pressure on the over-50 generation to take early retirements. By 2010, the ratio of adults over 65 to working adults will exceed 0.4 and put increasing stress on government and family health care budgets.

Japanese agricultural import restrictions and controls have kept domestic food prices at much higher levels than in many other countries. The most prominent example is rice, which is regarded as a strategic national resource and supported at a price four times the U.S. price. The magnitude of all agricultural subsidies is such that they would add 1 percent to the Japanese GNP if redirected.

Japan's post-war development has concentrated a disproportionate share of political, industrial, and financial power in the Kanto region surrounding Tokyo. Tokyo's population now strains the limits of municipal services. The Kansai region to the west, with its major cities of Kyoto, Osaka, and Kobe, has thus been eclipsed economically. Indeed, foreign companies seeking entry to Japanese markets would do well to investigate the more receptive Kansai.

Service industry employment now accounts for 60 percent of the total work force, as the Japanese domestic economy tracks the global trend. However, large portions of the work force remain in export-oriented manufacturing and subsidized agriculture, and are more vulnerable to fluctuations in foreign exchange rates, trade restrictions, and government budget constraints.

Japanese manufacturers have opened many foreign production subsidiaries, to move closer to ultimate markets and cope with exchange rates and trade barriers. This trend is accelerating, particularly regarding U.S. locations. Public concerns and debates about "exporting jobs" continue, as in the United States. As a perspective, Dataquest estimates the cumulative Japanese overseas manufacturing investment at $23.6 billion at year-end 1987, compared with an estimated U.S. figure of $110 billion.

West Germany

West Germany, another beneficiary of the U.S. import shopping spree, has experienced a decrease to zero real growth in exports of goods and services in the last two years. Germany was able to sustain a significant positive trade balance with the United States through the mid-1980s, second only to that of Japan. The effective appreciation of the deutsche mark has hindered exports of machinery and automobiles, slowing industrial production and creating some upward pressure on unemployment figures. The German economy in 1987 was generally weak and erratic across many sectors, but was rescued from a chill by a notable rise in consumer spending during the second half of the year.

Dataquest expects West German exports to show a modest recovery to 1.0 percent real growth in 1988 and 1989, accompanied by a 3.5 percent per year rise in the value of imported goods. The result will be a contraction of the German foreign trade balance by about negative 1.0 percent annually. More attention will be focused on sales efforts in European and newly industrialized world markets for German exports, where the deutsche mark has appreciated less than against the dollar. In the battle to retain its competitive export position, Dataquest also expects German industry to be a leader in making substantial investments in shop floor control systems, factory networks, and design automation.

The Germans have done the best job among major industrial countries in managing central government budgets, averaging less than a 1.4 percent annual deficit since 1980. Domestic demand will grow at about 2.0 percent per year. Family disposable income will grow at 3.5 percent, and consumer spending is projected to increase at 4.0 percent per year, with imported goods getting a considerable share. Automobiles, electronics, and household goods will be high on German shopping lists. Given the above, GNP is expected to grow at 1.3 percent per year. In addition to recent and pending tax reform legislation, these projections are based on assumptions of continued low rates of inflation, interest, and wage increases.

France

The French economy is a vessel with her sails luffed in the wind. Real GDP growth was 1.5 percent in 1987, and Dataquest projects the same 1.5 percent growth in 1988, before slowing further to 1.3 percent in 1989. French GDP growth has ranked as the lowest of the major Western European economies since 1983. The rate of unemployment is currently the highest in Western Europe, at 10.8 percent of the French labor force. Inflation and average annual wage increases were both a little more than 3.0 percent in 1987.

In a time of shifting international trade balances, France's $2 billion trade deficit in 1986 slid to a negative $10 billion in 1987, or 1.3 percent of GDP, and will continue in this direction by about a negative $1 billion per year through 1989. The problem is not as much the increasing value of imports, as it is the flat export growth rate. Between 1969 and 1974, the value of French exports grew an average of 13.4 percent per year, second only to the 14.9 percent annual growth in Japanese exports. However, a large proportion of French exports went to oil-exporting and developing countries, both sensitive to dollar exchange rates and growing more slowly than the average. As the franc appreciated against the dollar in the early 1980s, the price competitiveness of French exports declined. Finally, the total value of exports slipped below the value of imports in 1982.

The government began to take stringent measures to improve the economic picture in early 1986 by deregulating many sectors of the economy, and by privatizing a number of large state-owned companies. The privatization process has been successful in liberalizing and stimulating some industries, though the program is far from complete. Whether it will be continued depends upon the socialist-conservative composition of the government after the May 1988 election, and the market value of companies under consideration.

Private and corporate disposable incomes will improve when the government reduces income and corporate tax rates by 3.0 percent and 4.0 percent, respectively, in 1988. French value-added tax rates will be reduced progressively through 1992, to align with the internal European community. Corporate investment and private consumption spending should show modest increases as a result. Over time, the value-added tax reductions could add 0.5 percent per year to French GDP growth.

Generally, the French have been slower than the Germans and quicker than the English to make investments in manufacturing automation, and have been slow to adapt their products and distribution organizations to match changing market demands. Both domestic and international market share have been lost, and it is unlikely that near-term reversals in the trade deficit trend will occur. U.S. computer companies now control more than 60 percent of the French market, with only a 24 percent share going to French companies.

Domestically, the government has moved to improve employment figures by offering retraining, tax, and various subsidy incentives to new employers, including foreign firms. In view of the labor market and prospects for moderate wage increases through 1990, U.S. firms should seize the opportunity to open new offices and production facilities in France.

Italy

The Italian economy is a dramatic play of extremes. With 2.8 percent GDP growth in 1987, Italy pulled past Britain and France to rank as the fourth largest capitalist economy, behind the United States, Japan, and West Germany. The fastest annual growth rate over the last decade among major European countries has generated much talk of an Italian economic miracle. Inflation has dropped to 5.0 percent, down from 21.0 percent in 1980. Thousands of new small businesses have sprung from the fertile ground of a high household savings rate, 23.0 percent of disposable income, and plenty of individual entrepreneurial drive. Dispersion of production to networks of these small businesses is common, enabling the smaller subcontractors to contribute substantial added value to the finished products of big firms.

But beneath the gleam of GDP growth lie economic fault lines. As in the United States, the two largest problems are the balance of trade and the government budget deficit.

The Italian international trade balance, which popped into a surplus condition in 1986, dropped back to the deficit side in 1987. Imports of manufactured goods, energy, and food shot up 6.3 percent, occupying an increasing share of the domestic market. At the same time, Italian exports were weak, declining 1.0 percent in aggregate value shipped. Domestic demand will grow in 1988 and 1989 at a faster rate than GDP because imports will continue to outpace exports and detract from the total GDP figure. Unemployment seems destined to climb from the 1987 level of 10.8 percent to 11.5 percent within the next two years.

A disproportionate share of Italian exports are low-technology manufactured goods. For example, 14 percent of the 1987 total was clothing and textiles, which will become increasingly vulnerable to future competition from newly developing countries. In the high-technology sector, Olivetti is the largest Italian data processing equipment company and tenth largest worldwide, but is the only Italian company within the industry's top 100 firms. Funds for high-technology investment within the economy are limited, and R&D spending is half that of other major industrial economies, as a percentage of GDP. Much of the effective progress in technology advancement has come through acquisitions and strategic partnerships with foreign firms. Higher relative unit labor costs and slow productivity growth in the 1980s continue to hamper the competitive position of manufacturers. Given the foregoing, Dataquest projects that the Italian trade deficit will continue to widen through 1988 and 1989, due to heavy import traffic and only modest export growth.

In the United States, where credit cards are quite common, many consumers know firsthand how difficult it can be to recover from a large accumulated debt. Monthly payments to reduce the debt and cover interest must be squeezed from cash that otherwise would go to normal monthly activities. The debt to income ratio determines the degree of constraint in selecting options. On a national scale, Americans can easily see the problems posed by the U.S. budget deficit.

By comparison, Italy has a GDP one-sixth the size of the U.S. GNP, but had a 1987 budget deficit two-thirds the size of the U.S. deficit. The accumulated Italian government debt is equal to 93 percent of the annual GDP. By another measure, the debt is equivalent to $628 billion, or one-fourth the size of the huge U.S. public debt.

The tightly regulated Italian financial system, which severely restricts competition for financial assets, has thus far enabled government securities to sell very well in the domestic economy. However, as a member of the EEC, Italy must bring its banking and financial systems into accord with the other nations by 1992. The pending liberalization of capital flows means the government must ultimately increase the yield on its securities and come to grips with the deficit size. The most realistic hope for progress lies in a series of reductions in government spending. For fiscal 1988, a series of budget cutbacks and increases in direct taxes are expected to compress the Italian deficit to 12 percent of the GDP.

United Kingdom

The United Kingdom can boast the highest average rate of real GNP/GDP growth (3.6 percent) over the last three years among the major industrialized countries. This has been fueled chiefly by very strong private consumption and healthy exports. Industrial employment, which had dropped 25.0 percent in the United Kingdom since 1979, finally rose slightly in 1987 in conjunction with the growth in industrial output. Previous declines in manufacturing jobs have been partially countered by employment growth in the services sector since 1982. Total unemployment, which had risen to a 1986 peak of 11.6 percent of the work force, dropped below 10.0 percent by the end of 1987.

The above factors have enabled the British government to do an outstanding job of budget management in the 1980s, turning in a revenue-expense performance against plan second only to the record of the German government. Government spending will decrease slightly as a percentage of GDP in 1988, as will the small government budget deficit. The strength of the economy has also translated to good tax revenues, and the prospects are excellent for more supply-side incentives in the form of 1988 tax rate reductions.

Real GDP is forecast to increase by 2.8 percent in 1988, slowing to 1.8 percent in 1989. Economic growth will be led by continued expansion of consumer spending, in anticipation of tax cuts, moderate 3.5 percent to 4.0 percent inflation rates and further small decreases in the unemployment rate. Good order backlogs have caused business sentiment to remain very bullish regarding domestic markets, and many companies expect to make substantial investments in equipment and real estate to increase manufacturing capacity.

The primary drag on future economic growth will be from a deterioration in the United Kingdom's international competitive position, and decreasing demand from the United States, which in recent years has taken 14.0 to 16.0 percent of the United Kingdom's exports. A strong pound, declining North Sea oil production and recent weakening world oil prices will contribute negatively to the trade deficit in the near term. Exports are expected to show real growth of 2.0 percent in 1988, declining to 1.5 percent in 1989. A 4.0 to 4.5 percent growth in the value of imports will result in a growth in negative trade balance of approximately 0.8 percent of GDP per year.

Canada

Nineteen eighty-seven brought more good economic news for the United States' largest trading partner. The Canadian economy continued very robust growth in 1987, chalking up a real 3.6 percent increase. A glance at the table at the end of this section, which contains the 1983 through 1989 GNP/GDP growth, shows the Canadian average of 3.7 percent to be the highest average growth rate among the seven countries.

Fuel for the 1988-1989 economic engine will be provided by strong domestic investment in capital equipment and plant construction. Exports will continue to grow at 3.5 percent in 1988, with 78 percent of Canadian merchandise exports going into the United States. The Canada-U.S. free trade agreement, signed last year and officially taking effect in 1989, will begin having a substantial positive impact in 1988 in anticipation of the phased elimination of all tariffs and most other constraints on trade and investments. Canada's international trade balance is positive, with Can$125 billion in merchandise leaving the country and Can$114 coming in during 1987. U.S. manufacturers supply fully 70 percent of Canada's import purchases. Of the incoming goods from the U.S. in 1987, about 36 percent was automobiles and parts, 14 percent was industrial machinery and equipment, and 9 percent was communications and electronics equipment.

The Canadian economy is based around forestry, automobile manufacturing, petroleum, and mining. While smaller by comparison, the dynamic Canadian electronics industry is a major U.S. export market and a worldwide supplier of sophisticated products for telecommunications, geophysical exploration, natural resource processing and refining, and defense electronics. Many of the leading Canadian electronics companies are subsidiaries of U.S. or British firms, but there are an increasing number of examples in the opposite direction, such as Northern Telecom and Mitel Corporation.

With the exception of oil-related industries, Canadian manufacturers will continue to make heavy investments in capital equipment to sustain their growth, and U.S. exporters will continue to have the lion's share of that market. Many Canadian companies are actively seeking joint-venture manufacturing or sales partnerships with U.S. companies, and probably constitute the best learning opportunity for U.S. companies looking to expand into international markets.

Nineteen eighty-eight will see the lowering and restructuring of Canadian corporate and personal tax rates, as part of the government's long-range tax reform program. The general plan includes the probability of a national sales tax in 1990, replacing the current sales tax on manufacturers. If the government can keep spending relatively controlled, the federal budget deficit should improve to the range of 2.4 to 3.0 percent of GDP in 1988 and 1989.

As always, the big swing factor affecting prospects for Canadian economic growth is the health of U.S. markets. The good news/bad news about having such a good customer for exports on your southern border is that the United States accounts for so much of Canada's international business. Since a great part of the Canadian export industry centers on automobiles and lumber, it is especially sensitive to levels of U.S. consumer spending and residential construction. When the North American economies are moving along well, the Canadians generally do very well. Historically, the effects of slowdowns also tend to be more pronounced on Canada, and the economy underperforms that of the United States. Most current indications are cause for optimism, however, and the prospects for business activity in Canada remain good.

Newly Industrializing Countries

Figure 11 charts the 1987 gross domestic product data for five newly industrializing countries. Each country has its unique problems and unique strategies for long-range industrial success. The role of import-export trade in relation to total GDP should be especially noted. The most prominent trade example is Singapore, where import and export trade volumes were $37 billion in 1987, while GDP was $17 billion.

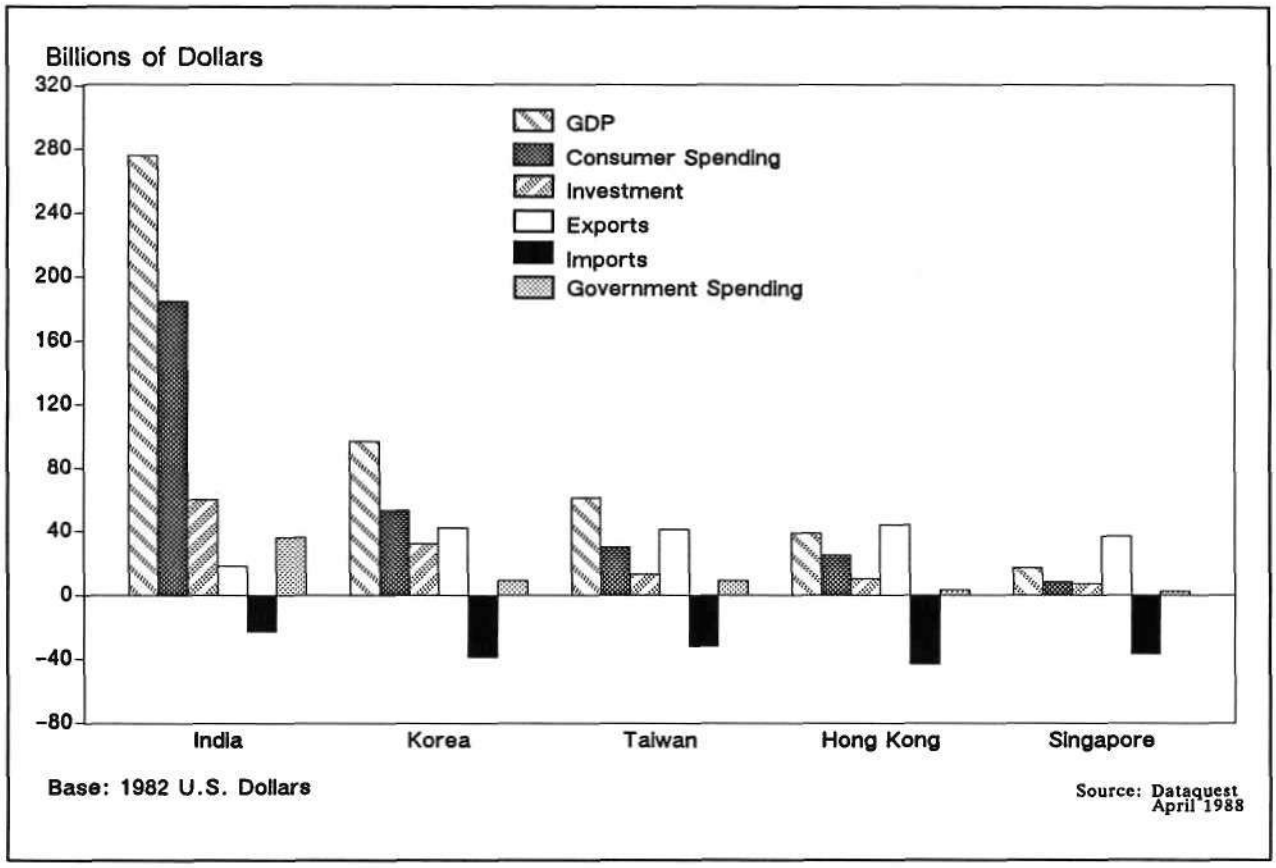

Figure 11. Newly Industrializing Countries' Components of 1987 GDP

Asian NICs continue to take advantage of the manufacturing opportunities and export markets opened by a weak dollar and strong yen. The countries of choice for United States and Japanese manufacturing investment have grown beyond the basic industry stage in many sectors, and have begun to successfully challenge for international market share. In particular, Taiwan and South Korea posted record levels of exports to the United States in 1987, ranking fourth and eighth on the list of U.S. suppliers. The most striking aspect in this can be seen in Figure 10, where the 1987 $18.3 billion U.S. trade deficit with Taiwan is second only to Japan, and has increased $3.6 billion over 1986. The U.S.-Korea deficit at $9.2 billion is half the Taiwan deficit size, but is growing at a faster rate. The pending U.S. removal of Taiwan, Korea, Hong Kong, and Singapore from the U.S. Generalized System of Preferences recognizes the U.S. status as 40 to 50 percent of their export markets, the relative restriction of their own domestic markets, and the consequent contribution to the U.S. trade deficit.

Korea, along with Taiwan, has been the major beneficiary of the yen's appreciation against the U.S. dollar, the Korean won, and the Taiwanese dollar. Trade surpluses, a drop in oil prices, and lower international interest rates have enabled the Korean government to halt foreign borrowing and begin to repay existing debts. Real GDP growth in 1987 was 12.5 percent, repeating 1986. Korean industry has been heavily dependent on imported Japanese capital equipment to continue manufacturing expansion, and this has been the source of a growing trade deficit with Japan, as well as an added stimulus in the Korean competitive attitude toward Japan. In efforts to reduce the trade deficit with Japan and the surplus in U.S. trade, the Korean government is pressuring manufacturers to shift part of their export sales efforts to Japan and away from the United States. Real GDP growth is expected to continue at a 9.0 percent rate through 1988-1989.

Taiwan has a far more decentralized industrial base than Korea, and as a percent of GDP, spends one-third less overall than the Koreans on fixed investments and capital equipment. The Taiwanese rate of growth in industrial production is, not surprisingly, 85 percent of the Korean rate, and is more concentrated in textiles and other light manufactured products, which are more vulnerable to foreign trade legislation. In programs to assist the capitalization and expansion of Taiwanese industry, the government is sponsoring centralized industrial parks and technology research institutions, with some notable successes. The administration of these programs is very active in promoting strategic alliances with Taiwanese and foreign companies for joint R&D, manufacturing, and East Asian market development.

Singapore is a recognized base for multinational manufacturing, and electronics and is becoming the central theme in the economy. More than 180 foreign companies have now established plants in the city-state, responding to a series of generous government incentives. In an aggressive move to accelerate this process, the Singaporean government will cover 74 percent of the construction costs for a $40 million wafer-fabrication plant to be built this year, in conjunction with National Semiconductor and Sierra Semiconductor, who have 9 and 17 percent shares, respectively.

Hong Kong, like Singapore, is a reexporting economy. A record 14.8 percent GDP growth in 1987 followed 11.0 percent the previous year, and is expected to continue at 9.0 percent through 1989. Textiles and apparel make up more than 40.0 percent of Hong Kong's exports and the bulk of shipments to the United States. Exports to the United States were up by 14.0 percent, while the Hong Kong-U.S. trade surplus increased by $119 million, or 2.0 percent. Strong domestic demand and increased trade with China will be major contributors to 1988 growth.

Hong Kong exporters have benefited from the Hong Kong dollar's stability against the U.S. dollar since 1985, in comparison with the Korean and Taiwanese currencies, which have appreciated 15 percent and 30 percent, respectively. The domestic economy has not suffered unduly, primarily because 45 percent of Hong Kong's consumer goods and food comes from the People's Republic of China

(PRC), and the Chinese reminbi has dropped 20 percent in value relative to the dollar. A revaluation of the Hong Kong dollar in the near term is unlikely.

India's 1987 4 percent growth in real GDP will continue through 1988 and 1989. International trade runs a $5 billion per year deficit. The government's past constraints on competition have effectively protected most of the domestic market, but the lack of stimulation has produced little technological innovation. This is beginning to change. The government has begun loosening restrictions on imports of systems, peripherals, and components. Efforts to encourage hardware assembly, especially software development in joint partnerships with foreign companies, have seen some modest successes. Indians believe that the most promising opportunities lie in matching their large pool of technically trained, English-speaking manpower with the worldwide demand for software. If the weighty Indian bureaucracy and start-up productivity levels can be overcome, Indian software technology will become a world force.

The reference statistics in Table 3 comprise GNP/GDP growth rates for the United States and its trading partners that were discussed in this document.

Table 3. Reference Statistics
(Percentage Changes from Previous Period, SAAR*)

	1983	1984	1985	1986	1987	1988	1989
Growth of Real GNP/GDP							
United States	3.6	6.8	3.0	2.9	2.8	2.8	2.2
Japan	3.2	5.1	4.7	2.4	3.5	3.5	3.0
West Germany	1.9	3.3	2.0	2.5	1.5	1.3	1.3
France	0.7	1.4	1.7	2.0	1.5	1.5	1.3
United Kingdom	3.3	2.7	3.6	3.3	3.8	2.8	1.8
Italy	0.5	3.5	2.7	2.7	2.8	2.0	1.8
Canada	3.2	6.3	4.3	3.3	3.6	2.8	2.3
Growth of Private Consumption							
United States	4.6	4.8	4.6	4.2	1.9	2.0	2.3
Japan	3.2	2.7	2.6	2.7	3.3	3.3	3.0
West Germany	1.7	1.5	1.8	4.3	2.5	2.8	2.3
France	0.9	1.0	2.4	3.3	1.8	1.5	1.0
United Kingdom	4.0	2.1	3.7	5.8	4.5	3.3	2.3
Italy	0.4	2.2	2.7	3.2	4.5	2.5	2.0
Canada	3.4	4.3	5.2	3.9	4.0	2.3	2.3
Growth of Government Consumption							
United States	1.1	4.4	7.3	3.8	1.8	1.9	0.8
Japan	2.9	2.8	2.0	6.6	(0.3)	2.5	3.0
West Germany	0.2	2.4	2.1	2.3	2.0	1.8	1.5
France	2.1	1.1	3.2	2.7	2.5	2.0	1.8
United Kingdom	1.9	0.8	(0.1)	0.9	0.5	1.0	1.0
Italy	2.8	2.0	3.5	3.0	2.8	2.5	1.8
Canada	1.4	1.5	2.7	1.0	2.0	1.8	1.0

(Continued)

Table 3. Reference Statistics
(Percentage Changes from Previous Period, SAAR*) (Continued)

	1983	1984	1985	1986	1987	1988	1989
Growth of Gross Fixed Investment							
United States	8.2	16.8	5.5	1.8	0.5	4.8	3.0
Japan	(0.3)	4.9	5.6	6.6	8.5	4.8	3.1
West Germany	3.1	0.8	0.1	3.1	1.0	1.5	1.0
France	(3.6)	(2.3)	1.1	3.1	3.0	2.5	2.3
United Kingdom	5.2	8.2	3.1	0.3	4.8	5.8	3.5
Italy	(1.6)	4.4	3.3	1.2	2.8	2.5	1.3
Canada	(0.7)	1.6	8.1	5.1	8.0	3.0	2.3
Growth of Real Exports							
United States	(3.8)	6.8	(1.7)	3.3	12.0	14.3	9.3
Japan	4.2	17.5	5.3	(4.8)	2.0	3.0	3.5
West Germany	(0.5)	9.0	7.2	(0.1)	0.0	1.0	1.0
France	3.7	7.1	2.1	(0.7)	(0.8)	2.5	2.5
United Kingdom	2.0	7.0	5.7	3.1	5.5	2.0	1.5
Italy	2.3	7.6	4.0	3.1	(1.0)	3.5	3.0
Canada	6.4	18.8	6.0	4.7	3.8	3.5	3.3
Growth of Real Imports							
United States	9.6	23.9	3.9	10.5	5.0	1.3	2.3
Japan	(5.1)	11.1	(0.1)	3.6	6.3	7.5	4.8
West Germany	0.6	5.3	4.7	3.5	3.3	3.5	3.5
France	(2.7)	2.8	4.7	6.9	4.8	3.0	3.0
United Kingdom	5.8	9.8	2.8	6.2	5.8	4.5	4.0
Italy	(1.6)	11.3	5.3	5.1	6.3	4.8	4.3
Canada	9.0	16.6	8.3	7.2	4.5	3.5	3.0

*Seasonally adjusted annual rate

Source: Dataquest
April 1988

Glossary

balance of payments. A double-entry accounting of the value of all exchanges and transfers of goods, services, capital loans, investments, and gold and international reserves between the public and private sectors of a given country and the rest of the world over a given time, usually one year. Balance of payments is divided into three accounts—current, capital, and the reserve and gold account.

balance of trade. The difference between the value of a country's exports and imports of *tangible goods* over a given period, usually one year.

balance on current account. See **current account.**

capacity utilization. The ratio of actual production output to potential production output, with existing plant, workers, and equipment.

capital account. Balance of payments category for the inward and outward flow of investment capital.

capital goods. All goods used for the *production* of other goods and services. See also **consumer goods.**

consumer. An individual who buys goods and services for personal use, rather than for manufacturing, processing, or resale.

consumer goods. Products used directly to satisfy human needs or wants, such as food and clothing. The distinction between consumer and capital goods lies in how products are *used* rather than in the products themselves.

consumer price indices (CPI). Monthly measures by the U.S. Bureau of Labor Statistics of the average retail prices of products commonly bought by households, compared with the average prices of a selected base year.

consumption. Expenditures for durable goods, nondurable goods, and services.

current account. Balance of payments category for **goods and services.** The difference between total exports and imports of goods and services is the **balance on current account.**

disposable income. An individual's income remaining after any payments to government (taxes, fines), and thus available for either spending or saving.

durable goods. Items that yield their services over an extended period of time, generally three years or more. Durables are often divided into the categories of *producer durables* (e.g., metals, machinery, equipment), and *consumer durables* (e.g., automobiles, appliances).

external debt. The total sum of a country's public and private debt owed to foreigners.

federal debt, federal deficit. See **public debt, public deficit.**

fixed investment. Assets for production of goods or services that cannot be quickly converted into money without disrupting operations, such as plant and equipment.

goods. Tangible items of trade, such as automobiles or shoes. Merchandise.

gross domestic product (GDP). The total market value of all goods and services produced each year within the domestic borders of a nation.

gross national product (GNP). GNP equals GDP plus the net of income accrued by domestic residents from investments abroad minus income earned in the domestic market by foreigners abroad.

gross national product deflator. A revision in the calculation of GNP derived by adjusting each component of GNP for price changes, then summing each into a weighted total. The result thus measures both changes in prices and shifts in consumption patterns.

industrial production index. A monthly measure of the quantity of U.S. output in mining, manufacturing, and utilities industries compared with a base year and seasonally adjusted.

inflation. A sustained increase in the average level of all prices.

internal debt. The total sum of a country's public and private debt owed to citizens of the same country.

investment. Expenditures for capital goods.

invisibles. Items of foreign trade that are intangible, such as banking, insurance, tourism, and transportation. Unlike visibles, such items are not recognized by customs and until recently were not reported in trade statistics.

nominal GDP/GNP. GDP/GNP valued in prices prevailing at the time of measurement. Year-to-year changes then reflect differences in both quantities and market prices.

nondurable goods. Items that yield their services over a short period of time, generally less than three years. Examples are food, clothing, paper, chemicals, petroleum, rubber.

private. Relating to individuals and businesses, rather than government.

producer price indices (PPI). Monthly measures by the U.S. Bureau of Labor Statistics of the prices of 2,800 representative commodities compared with those prices of a given base year.

public. Relating to local, state, or national governments.

public debt. The sum of debts outstanding of local, state, and national governments in a given country. Debt of the national government alone is the *national public debt* or *national debt*. In effect, the public debt is a measure of the extent to which government expenditures are financed by borrowing rather than taxation.

public deficit. Circumstance where government outlays for goods and services exceed receipts for a fiscal year.

real GDP/GNP. GDP/GNP valued in *constant* prices prevailing in a reference base year—1982 in this publication. Year-to-year changes thus reflect changes only in *quantities* produced.

recession. A broad downward movement of the economy over an extended time. Generally defined for the U.S. as two successive quarterly decreases in U.S. GNP.

seasonal variation. A regularly recurring pattern of change in economic activity owing to factors such as periodic climate changes, holidays, and vacations. Seasonal variations are commonly adjusted for in the analysis of data to clarify overall trends.

services. Intangible items of trade, such as education, transportation, banking, legal and medical care.

terms of trade. The ratio of the average price of a country's exports to the average price of its imports.

visibles or visible goods. Tangible items of foreign trade.

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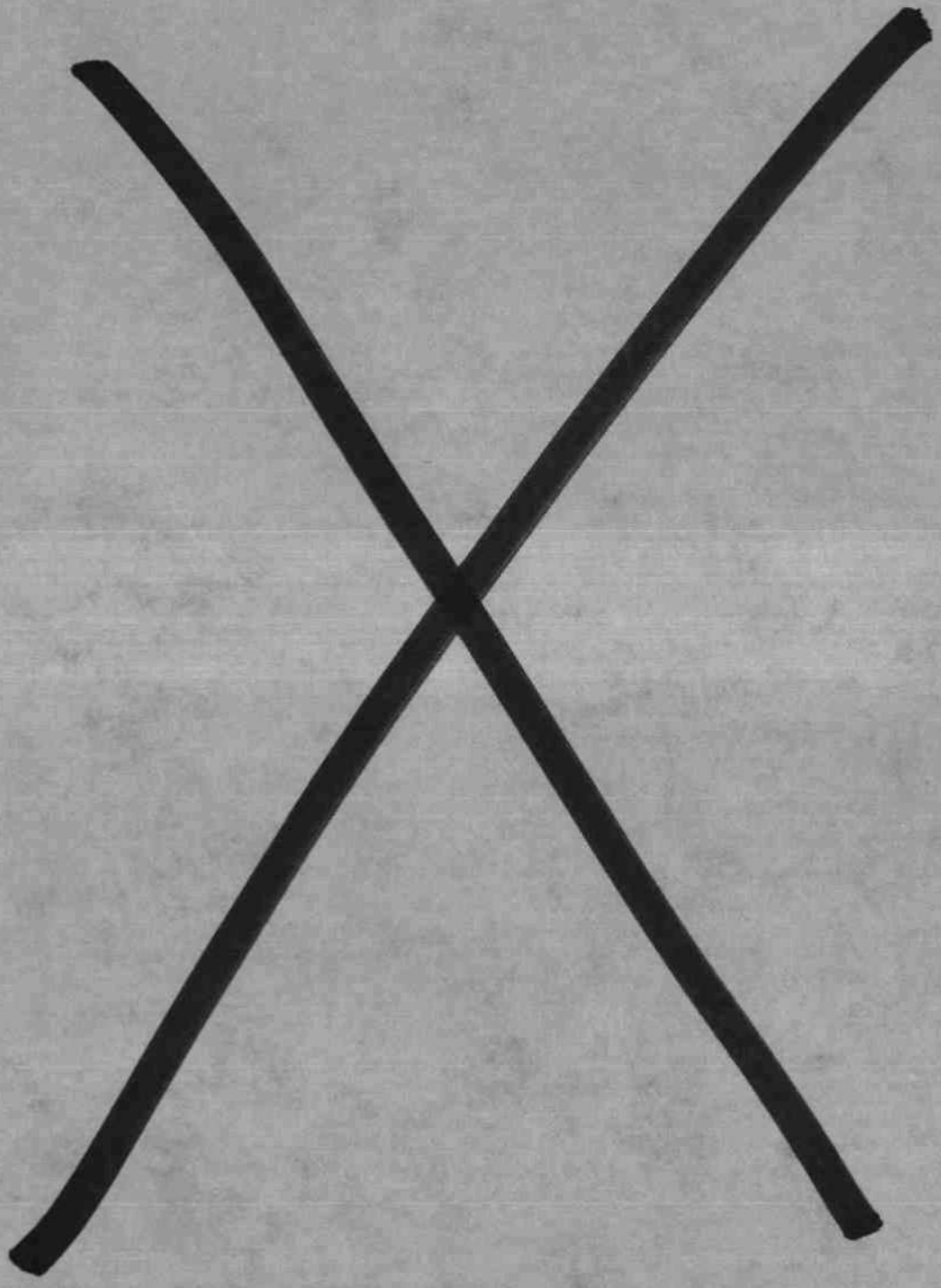

Capital Spending

The following is a list of the material in this section:

- Capital Spending by Company: U.S. Merchants
- Capital Spending by Company: Japan
- Capital Spending Forecast

For additional information, please refer to the material behind the Capital Spending tab in your 1989 Newsletter binder.

Capital Spending by Company: U.S. Merchants

NORTH AMERICAN CAPITAL SPENDING

Dataquest surveys the major North American merchant semiconductor manufacturers twice a year to track their capital spending plans. Table 1 provides a summary of the history of worldwide capital spending by North American merchants from 1985 to 1989 and an estimate of their capital spending plans for 1990. Table 2 presents U.S. merchants' capital-spending-to-revenue ratios and the U.S. merchant semiconductor industry average capital-spending-to-revenue ratio for the 1985 to 1989 time frame.

Table 1

U.S. Company Capital Spending
(Millions of Dollars)

Company	1985	1986	1987	1988	1989	1990	Percent Change 1989-1990
AMD	243	102	138	133	159	200	26%
Analog Devices	62	37	49	51	50	46	(8%)
AT&T	NA	NA	180	198	150	100	(33%)
General Electric	81	50	45	NA	NA	NA	NA
General Instrument	12	8	12	20	20	NA	NA
Harris	52	37	30	65	68	79	17%
IDT	25	18	18	37	57	41	(28%)
Intel	214	155	302	405	359	510	42%
LSI Logic	40	61	139	101	115	75	(35%)
Micron Technology	32	11	14	120	199	90	(55%)
Motorola	330	250	350	430	540	615	14%
National Semiconductor	319	223	120	220	200	200	0
Texas Instruments	281	217	231	388	641	780	22%
Vitelic	NA	NA	NA	8	36	47	31%
VLSI Technology	26	28	50	70	50	45	(10%)
Others	348	248	298	499	474	504	6%
Total	2,065	1,445	1,976	2,746	3,117	3,331	7%
Percent Change	(34%)	(30%)	37%	39%	14%	7%	

NA = Not available

Source: Dataquest May 1990

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Table 2

U.S. Merchant Capital Spending as a Percentage of Revenue

Company	1985	1986	1987	1988	1989
AMD	31%	12%	14%	12%	15%
Analog Devices	28%	15%	17%	14%	14%
AT&T	NA	NA	22%	23%	17%
General Electric	16%	10%	9%	NA	NA
General Instrument	6%	4%	8%	12%	NA
Harris	21%	19%	13%	9%	8%
IDT	48%	25%	19%	21%	27%
Intel	21%	16%	20%	17%	15%
LSI Logic	29%	31%	53%	27%	21%
Micron Technology	90%	18%	12%	36%	50%
Motorola	18%	12%	14%	14%	16%
National Semiconductor	23%	16%	8%	13%	12%
Texas Instruments	16%	12%	11%	14%	23%
Vitelic	NA	NA	NA	20%	49%
VLSI Technology	34%	25%	29%	32%	17%
U.S. Merchant Industry Average	21%	12%	15%	17%	18%

NA = Not available

Source: Dataquest May 1990

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Capital Spending by Company: U.S. Merchants

INTRODUCTION

This service section will report the results of Dataquest's latest survey of capital spending plans by U.S. merchant semiconductor companies. Knowledge of capital spending plans is useful to semiconductor manufacturers because it is an essential element of any competitive and capacity analysis. Knowledge of current spending plans of manufacturers can help semiconductor equipment manufacturers to identify sales leads and direct existing resources to the best markets.

NORTH AMERICAN COMPANY CAPITAL SPENDING

Dataquest surveys the major North American semiconductor manufacturers several times a year to track their capital spending plans. Table 1 provides a summary of the history of capital spending in North America by company and the change in spending from 1988 to 1989.

Table 1

U.S. Capital Spending of Selected Semiconductor Manufacturers

Company	1981	1982	1983	1984	1985	1986	1987	1988	1989	Percent Change 1988-1989
AMD	$ 58	$ 67	$ 121	$ 308	$ 243	$ 102	$ 138	$ 133	$ 150	13%
Analog Devices	16	19	24	58	62	37	49	51	62	21%
AT&T							180	198	222	12%
General Electric			64	107	81	50	45			
General Instrument				9	12	8	12	20	20	0
Harris	45	35	31	47	52	37	30	65	65	0
IDT			2	4	25	18	18	37	59	60%
Intel	157	138	146	388	214	155	302	450	470	4%
LSI Logic		6	30	82	40	71	135	100	100	0
Thomson-Mostek	98	47	78	123						
MMI	20	25								
Micron Technology		5	29	58	32	11	14	120	105	(13%)
Motorola	184	160	174	412	330	250	350	430	490	14%
National	245	238	245	495	319	223	120	220	220	0
Texas Instruments	145	140	232	472	281	217	231	392	492	26%
Vitelic								8	36	350%
VLSI Technology				26	26	28	50	70	40	(43%)
Others	265	251	324	551	348	238	302	452	496	10%
Total	$1,233	$1,131	$1,499	$3,139	$2,065	$1,445	$1,976	$2,746	$3,027	10%

Source: Dataquest June 1989

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Capital Spending by Company: U.S. Merchants

Continuing the trend that began in 1987, most U.S. companies are planning to increase their capital spending in 1989, although at a slower rate than in 1988. Intel, Motorola, and Texas Instruments each will spend more than $400 million on property, plant, and equipment.

Individual company capital spending/revenue ratios for the period 1981 through 1988 are given in Table 2.

Table 2

U.S. Capital Spending of Selected Semiconductor Manufacturers as a Percent of Revenue

Company	1981	1982	1983	1984	1985	1986	1987	1988
AMD	21%	20%	19%	27%	31%	12%	14%	12%
Analog Devices	18%	18%	17%	27%	28%	15%	17%	14%
AT&T							22%	23%
General Electric	0	0	13%	17%	16%	10%	9%	0
General Instrument		0	0	3%	6%	4%	8%	12%
Harris	27%	22%	18%	18%	21%	19%	13%	9%
IDT		0	23%	13%	48%	25%	19%	21%
Intel	30%	22%	19%	32%	21%	16%	20%	19%
LSI Logic		98%	94%	98%	29%	37%	52%	27%
Thomson-Mostek	47%	21%	25%	33%	35%	6%		
Micron Technology		103%	119%	49%	90%	18%	12%	31%
Motorola	15%	13%	11%	18%	18%	12%	14%	14%
National	20%	21%	18%	26%	23%	16%	8%	13%
Texas Instruments	11%	11%	14%	19%	16%	12%	11%	14%
Vitelic								20%
VLSI Technology				38%	34%	25%	29%	32%
Others	13%	13%	15%	19%	13%	8%	8%	11%
Total	16%	14%	16%	23%	19%	11%	13%	15%

Source: Dataquest
June 1989

Advanced Micro Devices (AMD)

From 1983, we have included Monolithic Memories' revenue and capital expenditure with AMD's. Monolithic Memories recently merged with AMD.

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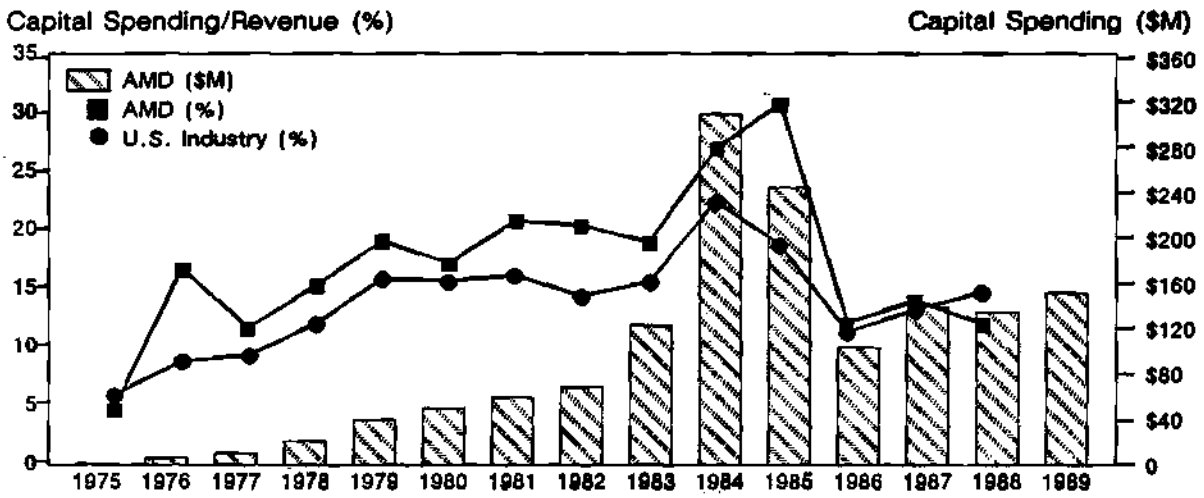
Capital Spending by Company: U.S. Merchants

AMD's capital spending-to-revenue ratio generally has exceeded the industry's average (see Figure 1). In 1989, however, AMD's capital spending-to-revenue ratio fell below the U.S. industry average. AMD plans to spend $150 million in 1989, up 13 percent from its spending level of 1988. AMD's submicron R&D facility in Sunnyvale, California, is under construction and expected to come on-line in the first quarter of 1990. This facility will be one of the first in the United States to utilize some of the advanced clean room concepts developed by Dr. Ohmi of Tohoku University of Japan.

Figure 1

AMD Capital Spending



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Source: Dataquest June 1989

AMD also plans to add more equipment to Fab 15 in Austin, Texas, and to close Fab 12 in San Antonio, Texas.

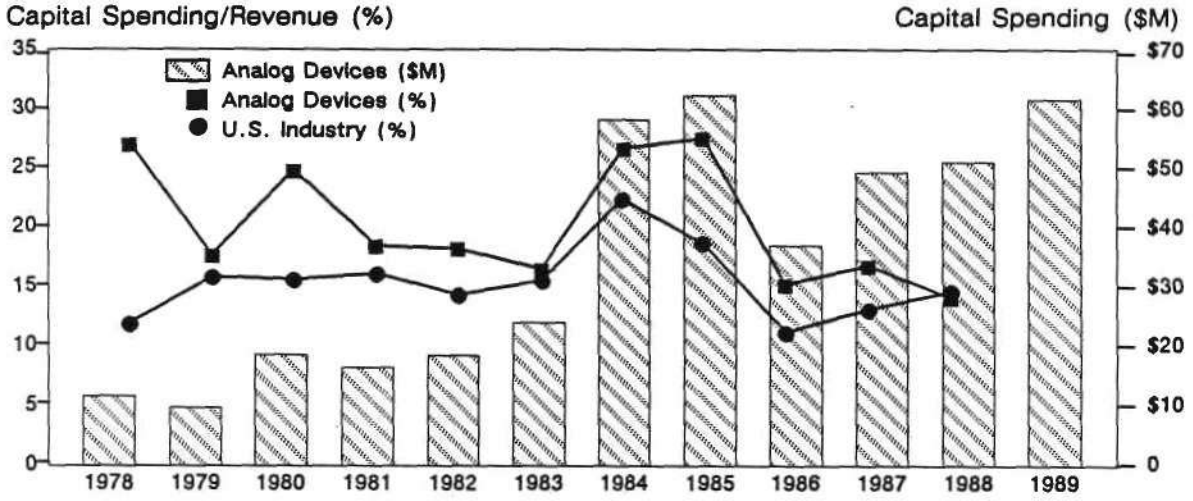
At the beginning of 1989, AMD announced plans to sell its assembly facility in Manila, the Philippines, to Amkor Electronics. Amkor will contract with AMD to provide assembly operations at the Manila facility for three years. This arrangement will allow AMD to concentrate on bringing up its new state-of-the-art assembly facility in Bangkok, Thailand.

Analog Devices

Analog Devices' capital spending-to-revenue ratio had always been above the industry's average (see Figure 2). However, in 1988, its ratio was slightly below the U.S. industry average. We estimate that its capital spending in 1989 will increase 21 percent, to $62 million.

Figure 2

Analog Devices Capital Spending



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Source: Dataquest June 1989

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Capital Spending by Company: U.S. Merchants

The focus of Analog's 1989 spending will be to upgrade its older facilities and to increase its capability in test, CAD/CAM, and factory control.

General Electric

All of General Electric's semiconductor facilities, except for its Research Triangle Park, North Carolina facilities, have been purchased by Harris Semiconductor. We will no longer track General Electric's capital spending as a separate item.

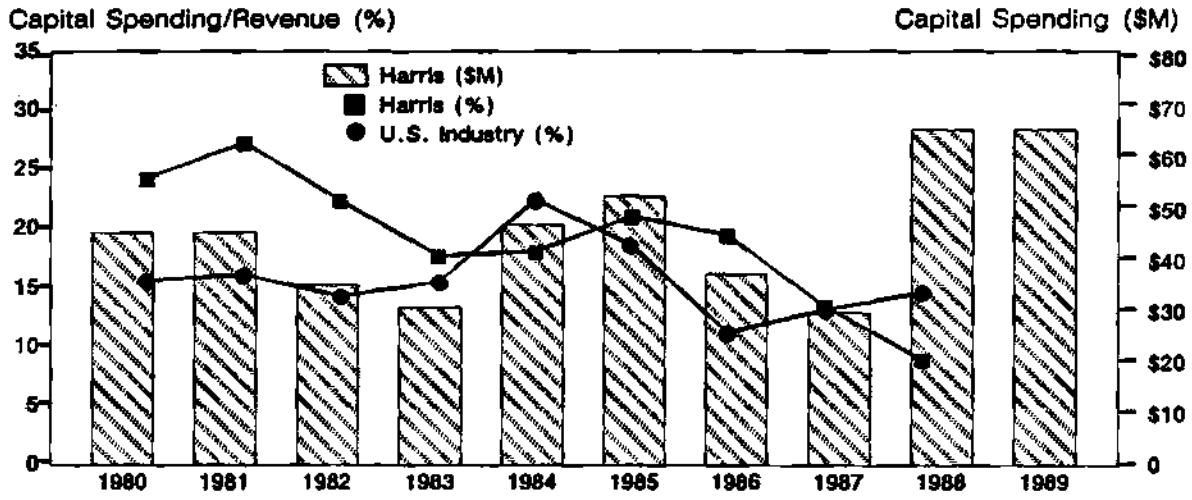
Harris Semiconductor

In 1988, Harris Semiconductor acquired the major parts of General Electric's semiconductor operations. These operations include the semiconductor operations of both RCA and Intersil. Data for 1988 and 1989 reflect the combined capital spending for Intersil, RCA, General Electric, and Harris. Harris' data before 1988 has not been restated to reflect the acquisition.

With the exception of 1984, Harris' capital spending ratio has been above that of the industry (see Figure 3). In 1988 it fell below the industry average, reflecting partly the weak spending by General Electric before the sale of its semiconductor operations. Harris' major goal in 1989 will be to integrate the various units from its acquisition into its ongoing operations. We therefore do not expect Harris to increase its spending this year.

Figure 3

Harris Capital Spending



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Source: Dataquest June 1989

Integrated Device Technology (IDT)

IDT's capital spending ratio generally has been above the industry's average (see Figure 4). In 1988, its ratio stood at 21 percent, which is significantly above the industry's average of 15 percent.

IDT's capital spending in 1989 will be $59 million, up 60 percent from its 1988 level of $37 million. In March of this year, IDT broke ground for its 135,000-square-foot facility in San Jose, California. This new facility will house a 150mm, Class 1 fab, which, according to IDT, will be capable of producing devices with line geometries of 0.5 micron. Dataquest estimates that this facility's capacity will be 20,000 wafers per month. The company hopes to see first silicon by mid-1989.

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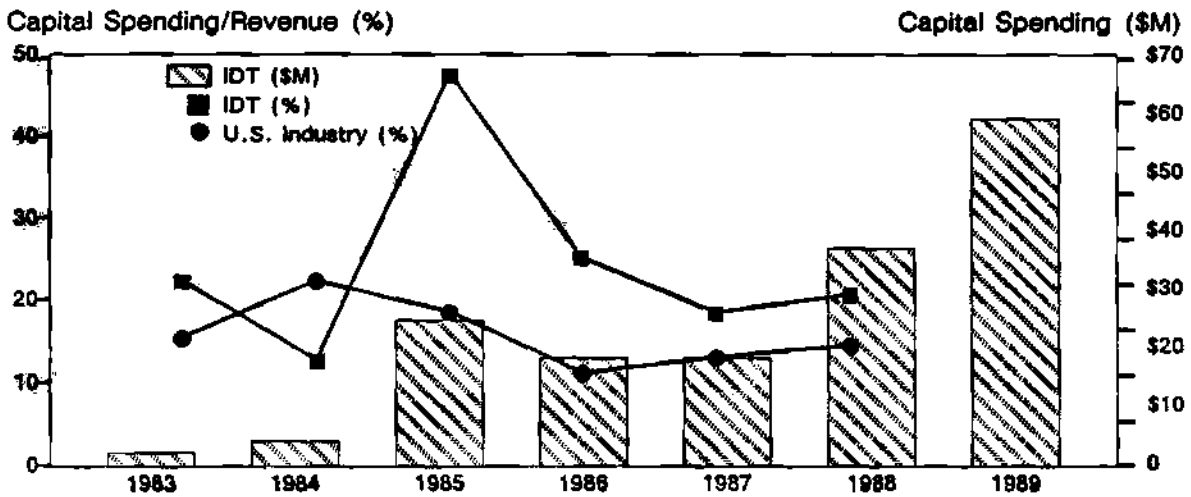
In 1988, IDT acquired a 100,000-square-foot test-and-assembly facility in Penang, Malaysia, to which it already has transferred a significant portion of its test activities. The company will continue to make expenditures to enhance and equip its Penang facility in 1989.

Figure 4

IDT Capital Spending



0004404-4

Source: Dataquest June 1989

Intel

Every year since 1975, Intel's capital spending-to-revenue ratio has exceeded the industry average (see Figure 5). In 1987, Intel's capital spending-to-revenue ratio was more than 20 percent, and in 1988 it was 19 percent.

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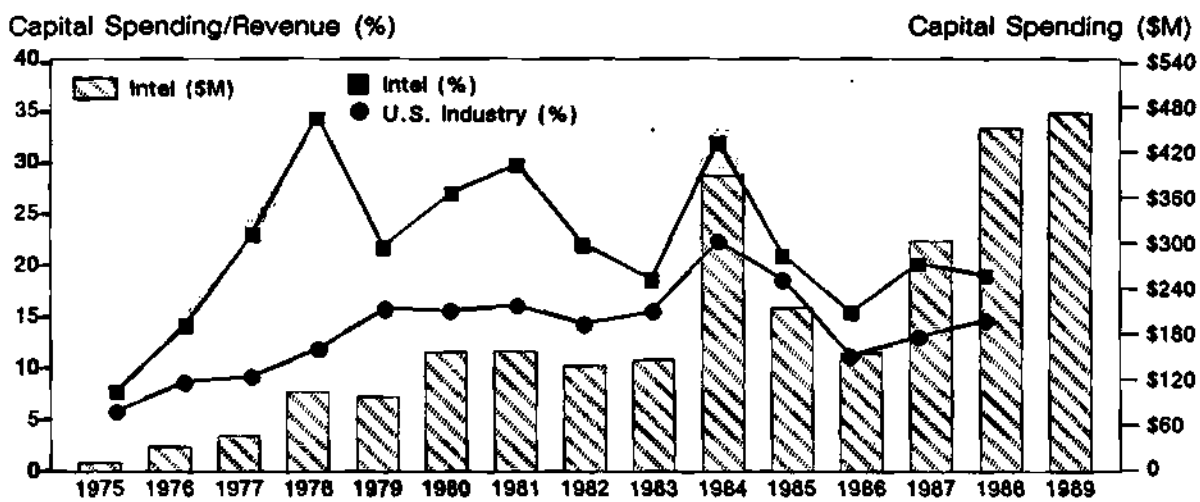
Capital Spending by Company: U.S. Merchants

Intel's capital spending in 1989 will increase only slightly; about 4 percent, to $470 million. Intel hopes to have its new R&D facility, D–2 in Santa Clara, California, completed and producing silicon by the end of this year. D–2 incorporates some of the latest clean room technology from Dr. Ohmi of Tohoku University. D–2 will be set up to run in three phases of centers of technology, as follows:

- Optimizing current standards of production
- Working on the next generation of process
- Beyond the next generation

Figure 5

Intel Capital Spending



0004404-5

Source: Dataquest June 1989

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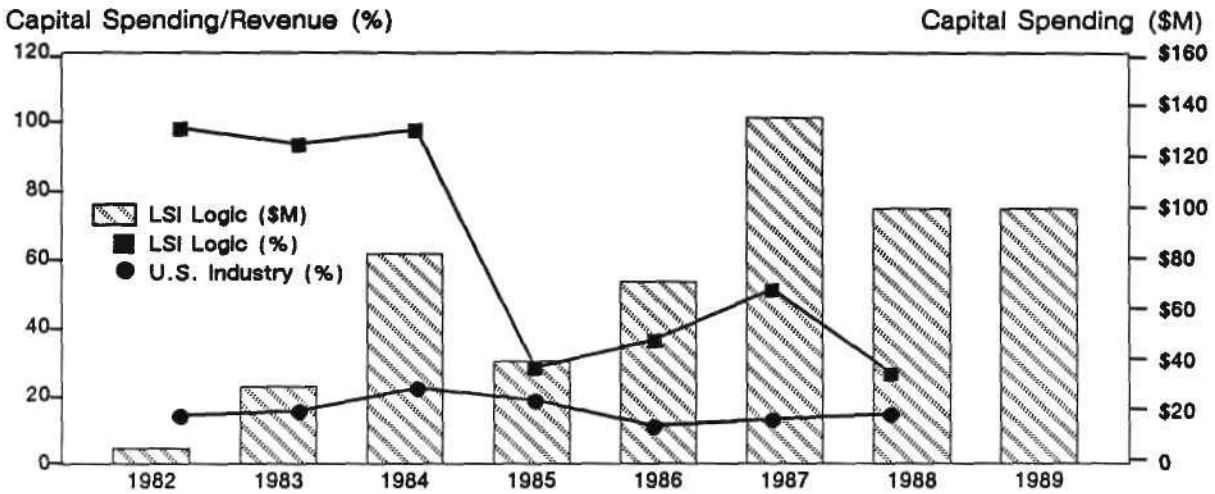
Capital Spending by Company: U.S. Merchants

LSI Logic

LSI Logic, which was incorporated in 1980, has had a very high capital spending ratio, because it put in fabs and equipment before its revenue stream became very large (see Figure 6).

Figure 6

LSI Logic Capital Spending



0004404-6

Source: Dataquest June 1989

In 1984, the focus of LSI's spending was on the establishment of its Santa Clara fab. In 1986, LSI began to convert from 4-inch wafers to 5-inch wafers and also began construction of Nihon Semiconductor in Japan. Its Nihon Semiconductor facility was completed in 1987 and in 1988, its new test and assembly facility in Braunshweig, West Germany, was completed. Also in 1988, LSI brought up its new fab in Sidcup, England, and a metallization line at Nihon Semiconductor.

Capital Spending by Company: U.S. Merchants

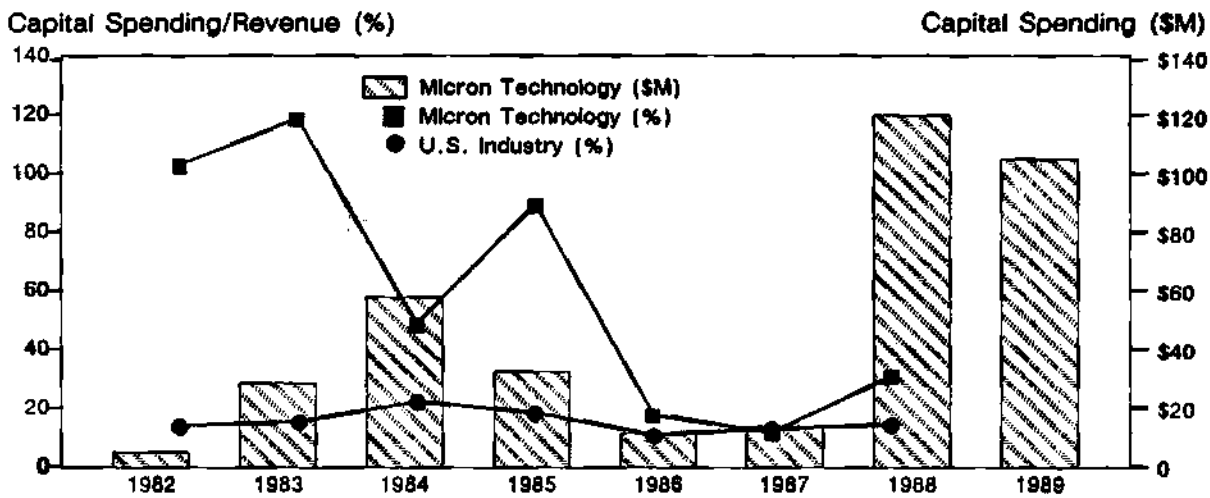
LSI recently announced that it will build a facility in Milpitas, California. This new facility will be the home of LSI's corporate headquarters, administrative facilities, research and development center, and 0.5-micron wafer fab. Groundbreaking for this new facility could occur by the end of 1989. Total expenditure for this facility through 1993 is estimated by LSI to be in the neighborhood of $300 million to $500 million.

Micron Technology

Micron Technology's capital spending ratio has been above the industry average every year since 1982. From 1982 to 1985, its capital spending ratio has ranged from 50 percent of revenue to a high of 120 percent of revenue in 1982 (see Figure 7). Prior to 1985, these high ratios were due to its building capacity as a start-up (Micron was incorporated in 1978). Its high spending ratio in 1985 was due to the downturn in revenue associated with the semiconductor industry's recession, especially in the DRAM market.

Figure 7

Micron Technology Capital Spending



0004404-7

Source: Dataquest June 1989

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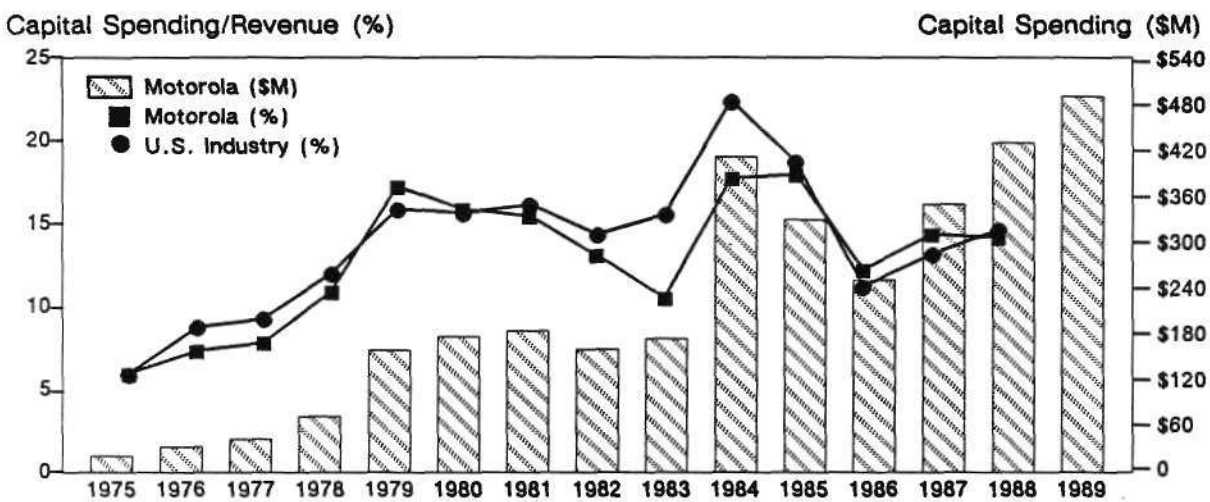
In 1988 and 1989, Micron responded to DRAM shortages by increasing its capital spending to more than $100 million. Micron's new DRAM facility, Fab 3, began production in the first half of 1989, approximately one year from ground-breaking. When the facility is fully ramped (approximately 18 months after first silicon) its capacity will be 18,000 150mm wafers per month. Eventually, Micron plans to run 4Mb and 16Mb DRAMs in Fab 3.

Motorola

Since 1984, Motorola's capital spending-to-revenue ratio has been very close to the industry average (see Figure 8).

Figure 8

Motorola Capital Spending



0004404-8

Source: Dataquest June 1989

Capital Spending by Company: U.S. Merchants

Dataquest estimates that Motorola's current capital spending for calendar 1989 will be up 14 percent from 1988 (from $430 million in 1988 to $490 million in 1989). This forecast does not include expenditure for its joint venture with Toshiba.

Motorola plans to build a $250-million submicron fab (MOS 11) on its 150-acre site in Oak Hill, Texas, which is just south of Austin, Texas. This new fab will produce 4Mb DRAMs with 0.8-micron minimum line geometries with both CMOS and BiCMOS. Motorola also plans to fabricate MPUs at MOS-11 eventually.

Motorola's 35,000-square-foot submicron R&D facility will come on-line in the first quarter of 1990. Motorola plans to spend $100 million for the facility and its equipment by the time the facility goes into production.

Motorola also plans to continue to invest in equipping MOS 11, its new 1Mb-DRAM fab in Phoenix, Arizona.

National Semiconductor

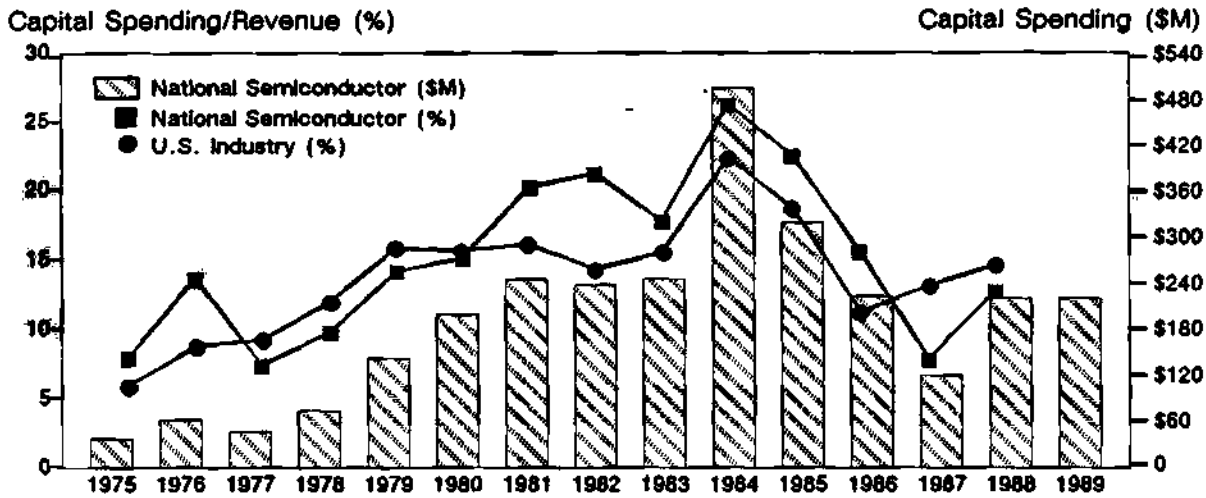
National Semiconductor's capital spending-to-revenue ratio has been below the industry average for the last two years (see Figure 9).

Dataquest estimates that National Semiconductor's capital spending in 1989 will be the same as in 1988: $220 million. Spending will be directed to bringing National's new 15,000-wafer-per-month, 150mm, BiCMOS facility on-line by the first quarter of 1990. National also is putting in a new line at its Arlington, Texas, facility.

Capital Spending by Company: U.S. Merchants

Figure 9

National Semiconductor Capital Spending



0004404-9

Source: Dataquest June 1989

Texas Instruments

Texas Instruments' capital spending–to–revenue ratio has been below the industry average since 1981, except for 1986 (see Figure 10).

Texas Instruments already has begun construction of its 200mm, pilot 4Mb–DRAM line in Dallas, Texas. The Company also has announced plans to build a $250–million fab in Avezzano, Italy. This fab will probably run 150mm wafers at 0.8 micron. Texas Instruments hopes to begin pilot production in 1990 and volume production by 1991.

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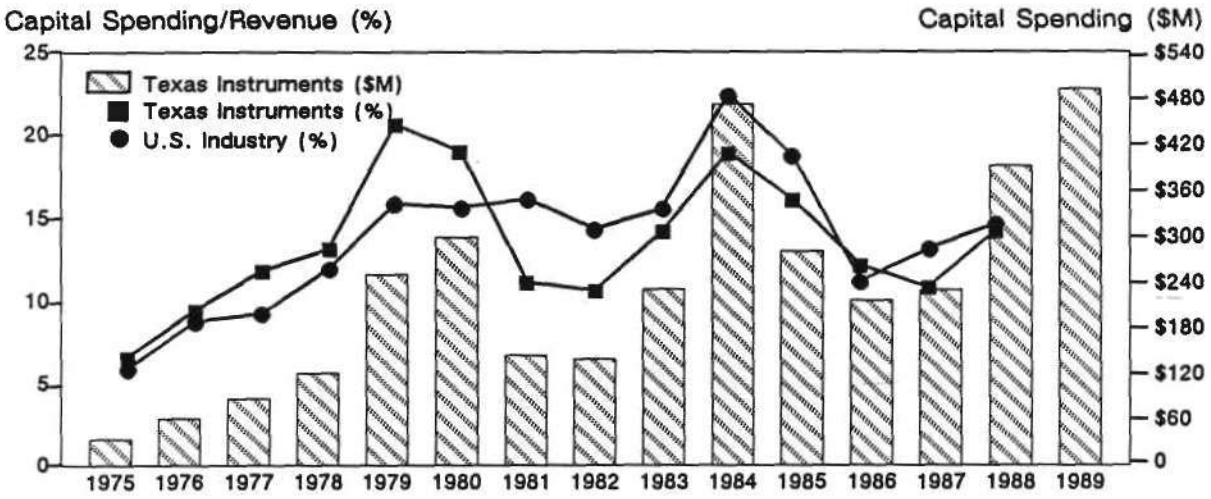
Capital Spending by Company: U.S. Merchants

Figure 10

Texas Instruments Capital Spending



0004404-10

Source: Dataquest June 1989

Texas Instruments recently announced that it will be building a 4Mb DRAM fab in Taiwan as part of a joint venture with Acer. When this fab is completed, Texas Instruments will join Motorola as one of the only two companies in the world with fabrication facilities in Japan, the United States, Europe, and in the Asia–Pacific region.

Vitelic

Vitelic spent 20 percent of its revenue on capital spending in 1988. It plans to spend $36 million in 1989. Vitelic is currently building a fab in Taiwan, at a cost of approximately $80 million. The plant will run 150mm wafers with 0.90–micron capability and will come on–line in 1990.

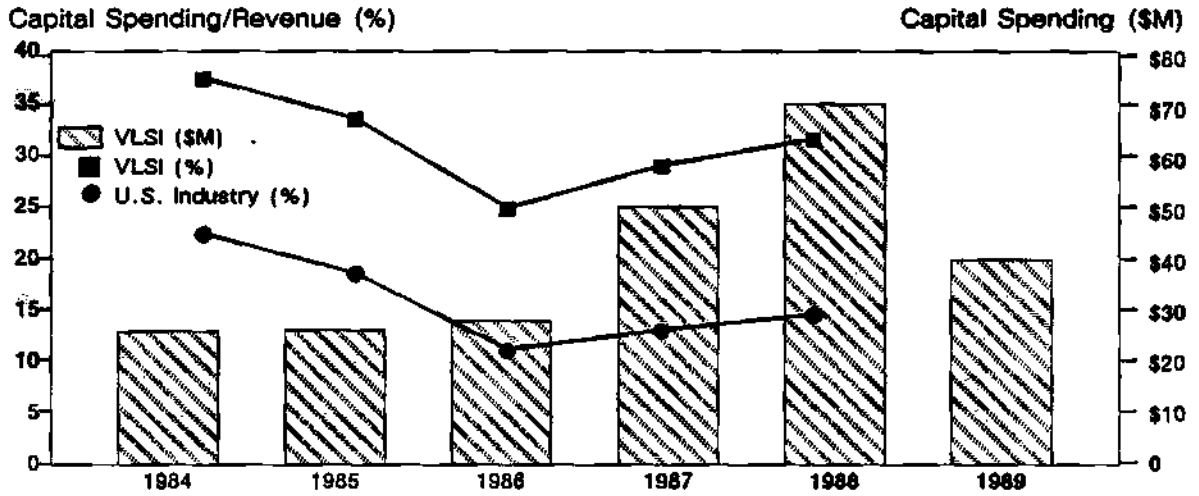
Capital Spending by Company: U.S. Merchants

VLSI Technology

In 1988, VLSI Technology spent 32 percent of its 1988 revenue on property, plant and equipment in 1988 and brought up a new fab in San Antonio, Texas (see Figure 11). This new fab, which is now operational, will run 10,000 150mm wafers per month at 1.2 micron. Now that the San Antonio fab is complete, VLSI will decrease its capital expenditure in 1989 by 43 percent, to $40 million.

Figure 11

VLSI Technology Capital Spending



0004404-11

Source: Dataquest June 1989

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Capital Spending by Company: U.S. Merchants

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Capital Spending by Company: Japan

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Capital Spending by Company: Japan

INTRODUCTION

This service section will report the results of Dataquest's latest survey of capital spending plans by Japanese semiconductor companies. Knowledge of capital spending plans is useful to semiconductor manufacturers because it is an essential element of any competitive or capacity analysis. Knowledge of semiconductor manufacturers' current spending plans can help semiconductor equipment manufacturers identify sales leads and direct existing resources to the best markets.

JAPANESE COMPANY CAPITAL SPENDING

Dataquest surveys the major Japanese semiconductor manufacturers several times a year to track their capital spending plans. Table 1 provides a summary of the history of capital spending by Japanese semiconductor manufacturers in yen and the percent change in their spending from 1988 to 1989. Most of the analysis in this service section is given in yen. This is because statements of change in current dollars overstate the growth of Japanese capital spending because of Japanese currency appreciation. Table 2 provides Japanese capital spending data in U.S. dollars.

Continuing the trend that began in 1987, most Japanese companies are planning to increase their capital spending, although at a slower rate than in 1988. Toshiba will spend more than any other company in the world except Samsung and Goldstar, each of which will spend approximately as much as Toshiba. In 1989, Toshiba plans to spend ¥80 billion ($615 million); Hitachi and NEC each plan to spend ¥70 billion ($538 million); and Fujitsu and Matsushita each plan to spend ¥60 billion ($462 million). These five companies account for 34 percent ($1.8 billion) of total Japanese capital spending of $5.4 billion. Individual company capital spending/revenue ratios for 1976 through 1988 are given in Table 3.

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Table 1

Japanese Company Capital Spending
(Billions of Yen)

Company	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	Percent Change 1988-1989
Fuji Electric	N/M	N/M	N/M	N/M	¥ 4	¥ 6	¥ 12	¥ 12	¥ 5	¥ 3	¥ 5	¥ 7	40%
Fujitsu	¥10	¥14	¥ 25	¥ 32	35	53	115	72	16	20	60	60	0
Hitachi	9	13	21	33	36	62	120	92	22	30	65	70	8%
Matsushita	4	9	20	19	9	21	110	60	25	22	50	60	20%
Mitsubishi	4	9	8	13	20	31	65	62	20	15	40	50	25%
NEC	14	23	30	38	42	58	129	123	30	30	55	70	27%
Nihon Semiconductor	0	0	0	0	0	0	0	0	5	15	3	5	67%
New Japan Radio Corp.	N/M	N/M	N/M	N/M	2	2	4	5	5	2	5	7	40%
NMB	N/M	N/M	N/M	N/M	N/M	N/M	14	14	5	10	10	40	300%
OKI	2	3	12	12	11	11	26	26	10	25	37	40	8%
Rohm	N/M	N/M	N/M	N/M	2	3	6	9	8	12	10	15	50%
Sanken Electric	N/M	N/M	N/M	N/M	2	3	6	6	4	5	10	12	20%
Sanyo	1	4	8	12	10	12	32	47	18	25	29	35	21%
Sharp	2	8	9	10	8	16	26	36	22	20	35	45	29%
Shindengen	N/M	N/M	N/M	N/M	1	1	3	3	1	1	2	3	50%
Seiko Epson	N/M	N/M	N/M	N/M	5	9	18	8	5	6	7	7	0
Sony	N/M	N/M	N/M	N/M	5	9	14	36	16	16	35	45	29%
Toshiba	5	8	11	16	28	86	136	123	65	60	80	80	0
Others	0	0	0	0	9	16	34	32	13	20	45	55	22%
Total	¥51	¥91	¥144	¥185	¥229	¥399	¥870	¥766	¥295	¥337	¥583	¥706	21%
Percent Change	21%	79%	58%	29%	24%	74%	118%	(12%)	(61%)	14%	73%	21%	

N/M = Not Meaningful

Source: Dataquest August 1989

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Capital Spending by Company: Japan

Table 2

Japanese Company Capital Spending
(Millions of Dollars)

Company	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	Percent Change 1988-1989
Fuji Electric	0	0	0	0	$ 16	$ 26	$ 51	$ 50	$ 30	$ 21	$ 38	$ 54	40%
Fujitsu	$ 49	$ 63	$111	$145	141	226	485	303	96	139	462	462	0
Hitachi	44	59	93	149	145	264	506	387	132	208	500	538	8%
Matsushita	19	41	89	86	36	89	464	252	150	153	385	462	20%
Mitsubishi	19	41	36	59	80	132	274	261	120	104	308	385	25%
NEC	68	104	133	172	169	247	544	517	180	208	423	538	27%
New Japan Radio Corp.	0	0	0	0	8	9	17	21	30	17	38	54	40%
NMB	0	0	0	0	0	-0	59	59	30	69	77	308	300%
OKI	10	14	53	54	44	47	110	109	60	174	285	308	8%
Rohm	0	0	0	0	8	13	25	38	48	83	77	115	50%
Sanken Electric	0	0	0	0	8	13	25	25	24	35	77	92	20%
Sanyo	7	18	36	54	40	51	135	197	108	174	223	269	21%
Sharp	7	36	38	43	32	68	110	151	132	139	269	346	29%
Shindengen	0	0	0	0	4	-4	13	13	6	7	15	23	50%
Seiko Epson	0	0	0	0	20	38	76	34	30	42	54	54	0
Sony	0	0	0	0	20	38	59	151	96	111	269	346	29%
Toshiba	24	36	49	72	113	366	574	517	389	417	615	615	0
Others	0	0	0	0	36	68	143	134	78	139	346	423	22%
Total	$247	$411	$638	$834	$921	$1,698	$3,671	$3,219	$1,766	$2,345	$4,485	$5,431	21%
Percent Change	57%	66%	55%	31%	10%	84%	116%	(12%)	(45%)	33%	91%	21%	
Exchange Rate (Yen per US$1)	206	221	225	221	249	235	237	238	167	144	130	130	

N/M = Not Meaningful

Source: Dataquest
August 1989

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Capital Spending by Company: Japan

Table 3

Japanese Company Capital Spending as a Percentage of Revenue

Company	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988
Fuji Electric	N/M	N/M	N/M	N/M	16%	21%	29%	32%	15%	8%	14%
Fujitsu	39%	31%	40%	39%	30%	34%	41%	30%	7%	8%	20%
Hitachi	10%	13%	15%	18%	16%	21%	25%	23%	6%	8%	14%
Matsushita	8%	17%	28%	18%	8%	15%	50%	28%	13%	10%	20%
Mitsubishi	13%	21%	14%	18%	24%	26%	28%	39%	11%	7%	14%
NEC	13%	17%	17%	17%	16%	17%	24%	26%	7%	6%	9%
New Japan Radio Corp.	N/M	N/M	N/M	N/M	N/M	N/M	N/M	N/M	33%	11%	21%
OKI	N/M	N/M	N/M	55%	34%	20%	30%	36%	14%	27%	30%
Rohm	N/M	N/M	N/M	N/M	8%	8%	10%	15%	12%	16%	12%
Sanken Electric	N/M	N/M	N/M	N/M	9%	12%	16%	16%	11%	12%	20%
Sanyo	6%	12%	19%	24%	17%	15%	30%	43%	18%	20%	21%
Sharp	N/M	N/M	N/M	27%	17%	24%	33%	46%	30%	24%	26%
Seiko Epson	N/M	N/M	N/M	N/M	N/M	N/M	66%	36%	18%	17%	17%
Sony	N/M	N/M	N/M	N/M	N/M	30%	35%	60%	21%	19%	29%
Toshiba	6%	8%	8%	9%	16%	37%	37%	35%	17%	14%	14%
Japanese Industry Average	10%	14%	17%	16%	17%	22%	32%	32%	12%	13%	18%

N/M = Not Meaningful

Source: Dataquest
August 1989

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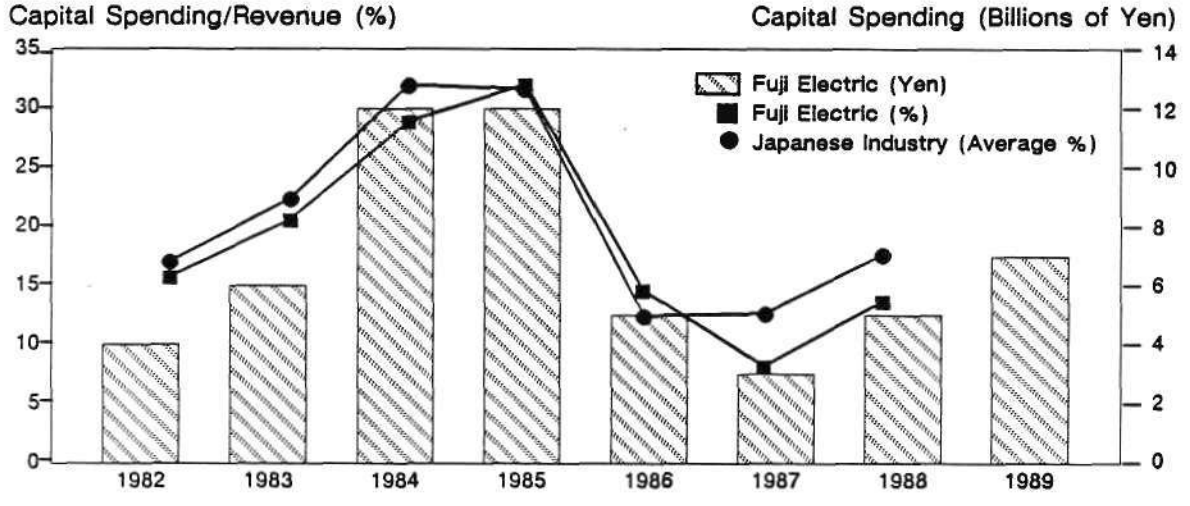
Fuji Electric

Fuji Electric's ratio of capital spending was below the Japanese company average in both 1987 and 1988 (see Figure 1). Fuji plans to increase its spending from 5 billion yen in 1988 to 7 billion yen in 1989 (from $38 million to $54 million). This is an increase of 40 percent over 1987.

Figure 1

Fuji
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-1

Source: Dataquest August 1989

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Capital Spending by Company: Japan

Fujitsu

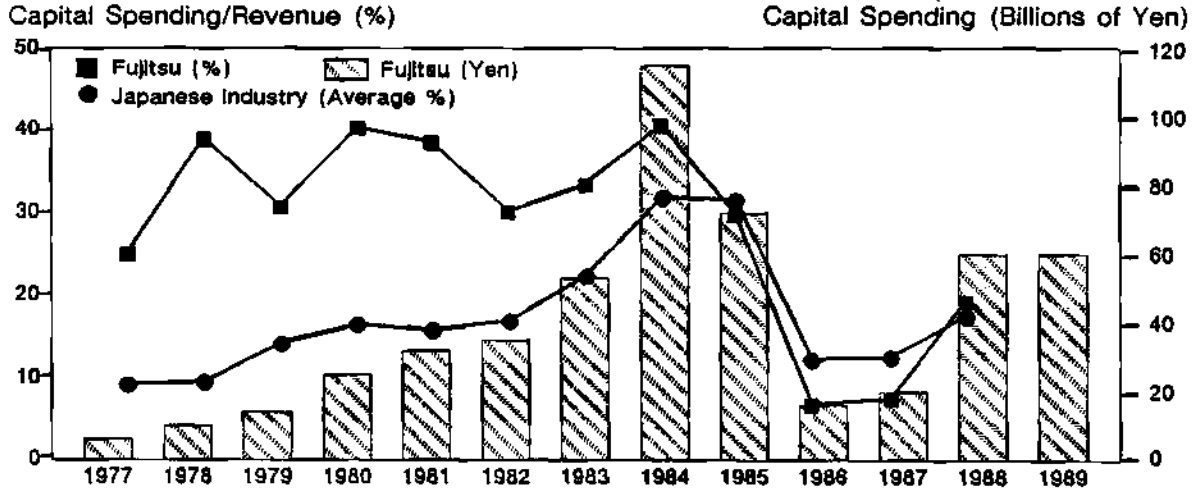
In 1986, Fujitsu's ratio of capital spending to revenue was 7 percent compared with the Japanese company average of 12 percent (see Figure 2). In 1987, Fujitsu's ratio was 8 percent; the Japanese industry's average was 13 percent. In 1988, however, Fujitsu's ratio of capital spending to revenue was 20 percent; the Japanese industry's average was 18 percent.

Fujitsu plans to keep its capital spending on par with its 1988 spending of ¥60 billion ($462 million). Fujitsu is committed to an ambitious expansion program. This year, it completed two new fabs in Gresham, Oregon, in the United States. One of these fabs is an ASIC facility, capable of running 28,000 1.5-micron 125mm wafers per month. The other fab in Gresham is a 150mm line capable of running 15,000 1.2-micron 1Mb DRAMs per month. Fujitsu plans to begin pilot production on this line in the summer of 1989.

Fujitsu announced plans for a 1Mb and a 4Mb DRAM and also an ASIC facility in Newton Aycliffe in the United Kingdom. The Company also announced that it plans to build a 4Mb DRAM production line at its Mie, Japan, plant. Dataquest believes that Fujitsu also may soon have a 200mm 4Mb DRAM facility in Izawa-gun, Iwate, in Japan.

Figure 2

Fujitsu
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-2

Source: Dataquest August 1989

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Capital Spending by Company: Japan

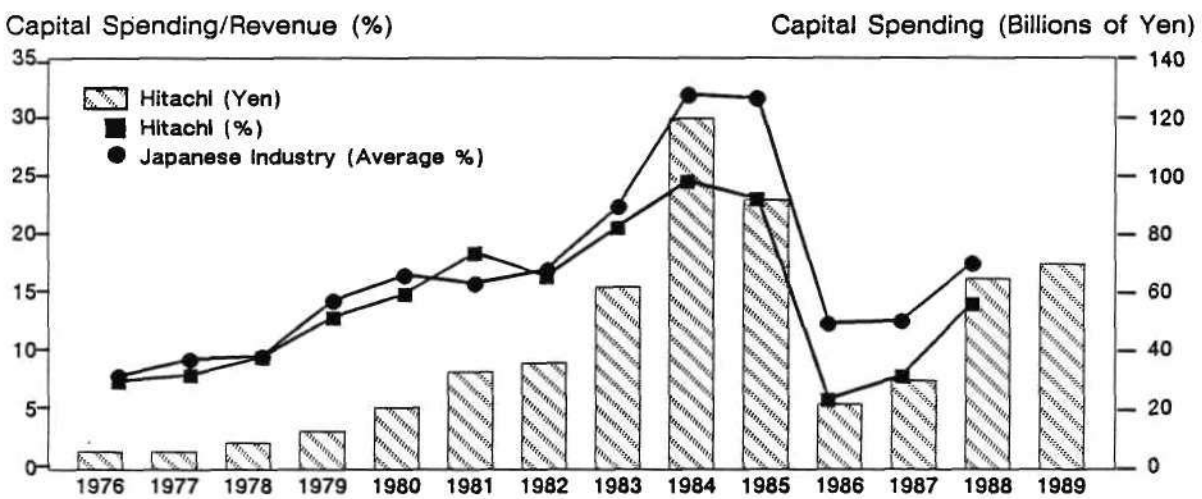
Hitachi

Hitachi's capital spending/revenue ratio has been less than the industry's average since the early 1980s (see Figure 3). We expect Hitachi to increase its capital spending by 8 percent in 1989, from ¥65 billion in 1988 to ¥70 billion in 1989 (from $500 million to $538 million).

Hitachi also is involved in an ambitious expansion program. Hitachi's new 150mm SRAM facility in Irving, Texas, in the United States began production in May of 1989. Dataquest believes that Hitachi may also begin running 200mm wafers for 4Mb DRAMs at its Kodaira-shi, Tokyo, facility in 1990; Hitachi reportedly will open another 4Mb-DRAM facility at Kanakoma-gun, Yamanashi, in Japan, also in 1990, but one that will produce 150mm wafers.

Figure 3

Hitachi
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-3

Source: Dataquest August 1989

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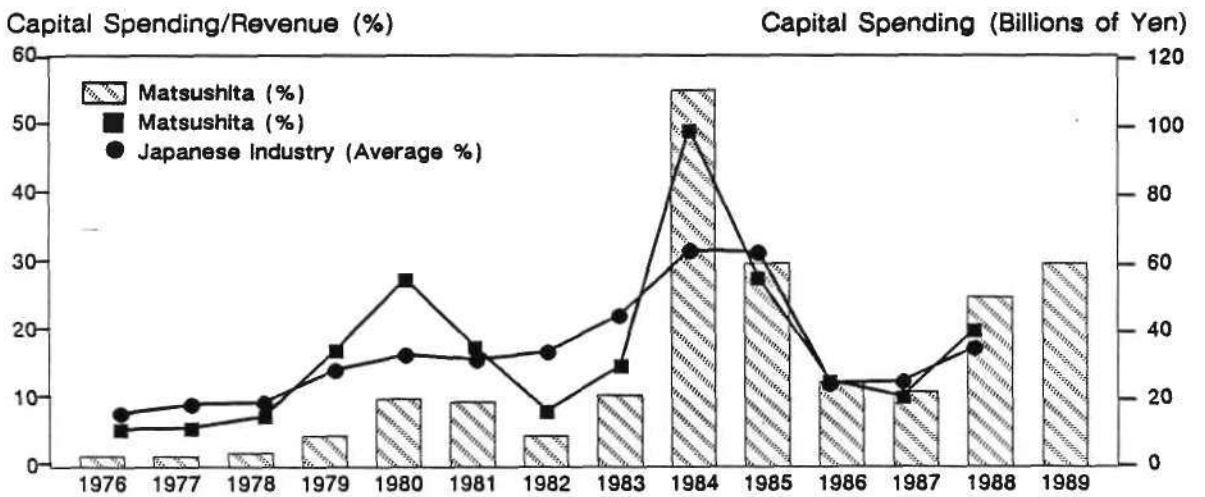
Capital Spending by Company: Japan

Matsushita

Matsushita's ratio of capital spending to revenue has been very close to the Japanese industry's average since 1985 (see Figure 4). In 1988, Matsushita spent ¥50 billion ($385 million) on capital spending. We expect Matsushita's capital spending to increase by approximately 20 percent this year, to ¥60 billion ($462 million). The company plans to install a 4Mb DRAM line at its Uozu, Japan, facility. Matsushita also plans to expand its prototype line at its Semiconductor Research Center in Kadoma-shi, Japan.

Figure 4

Matsushita
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-4

Source: Dataquest August 1989

Capital Spending by Company: Japan

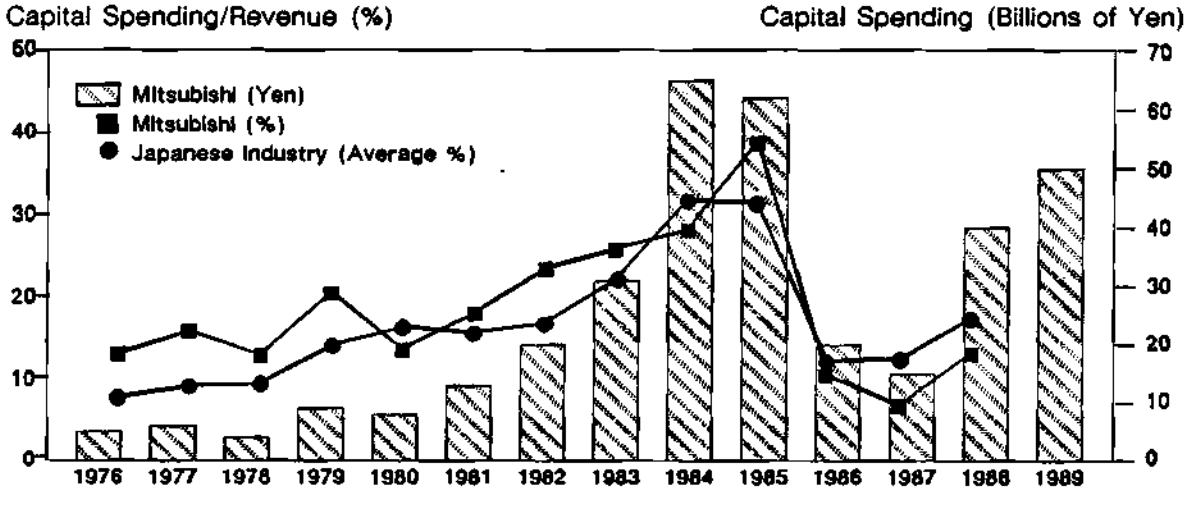
Mitsubishi

In 1987, Mitsubishi's ratio of capital spending to revenue was 7 percent, while the average for the Japanese industry was 13 percent (see Figure 5). In 1988, Mitsubishi increased its capital spending from ¥15 billion in 1987 to ¥40 billion in 1988. Its ratio of capital spending to revenue rose to 14 percent; the Japanese industry's average in 1988 was 18 percent. Dataquest expects Mitsubishi's capital spending to increase 25 percent in 1989, from ¥40 billion ($308 million) in 1988 to ¥50 billion ($385 million) in 1989.

Mitsubishi had planned to began ASIC production at its Durham, North Carolina, facility in the United States in the early part of 1989. The Company, however, recently announced that it will start producing 1Mb DRAMs at this facility instead of ASICs. Mitsubishi also is building a 4Mb DRAM prototype line at its Saijo, Japan, facility. This prototype line is expected to be operational in 1990.

Figure 5

Mitsubishi
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-5

Source: Dataquest August 1989

Capital Spending by Company: Japan

NEC

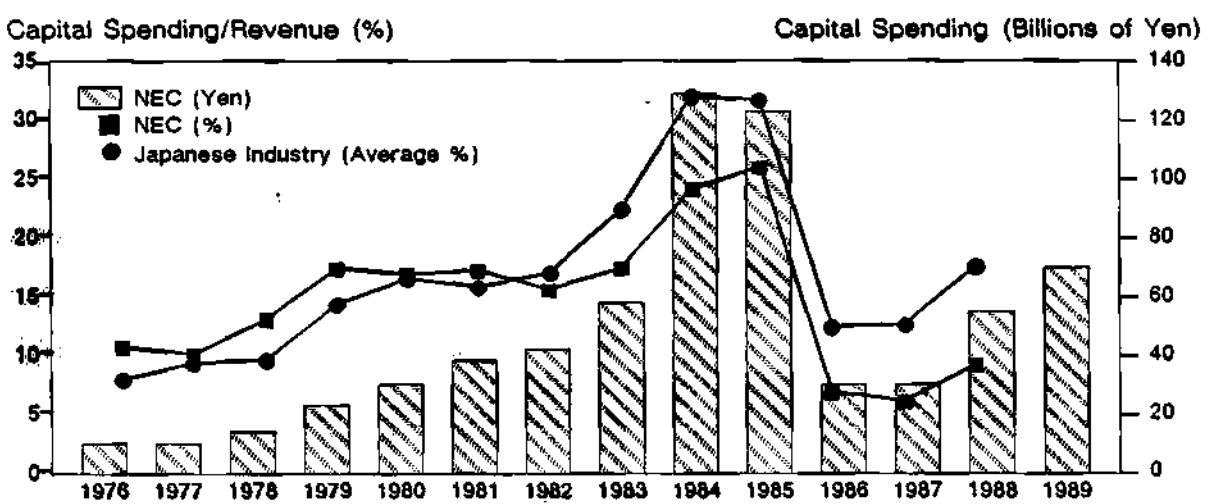
NEC's capital spending/revenue ratio has been significantly below the Japanese industry's average since 1983 (see Figure 6). In 1987, NEC's capital spending-to-revenue ratio was just 6 percent, with the Japanese industry average at 13 percent. In 1988, NEC's capital spending-to-revenue ratio was approximately one-half the Japanese industry's average (9 percent versus 18 percent).

NEC's capital spending totaled ¥55 billion ($423 million) in 1988; by the end of 1989, NEC's capital spending is expected to increase by 27 percent to ¥70 billion ($538 million).

NEC reportedly plans to complete its 16Mb prototype DRAM line at its Sagamahara, Japan, facility and begin production there by the end of this year. These prototypes may be run on 200mm wafers. NEC also expects to complete its 4Mb DRAM facility in Yamaguchi, Japan, this year. The Company reportedly plans to follow up its DRAM fab in Yamaguchi with one in Hiroshima, Japan, in 1990.

Figure 6

NEC
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-6

Source: Dataquest August 1989

Capital Spending by Company: Japan

NMB Semiconductor

NMB plans to increase its capital spending substantially this year; from ¥10 billion to ¥40 billion (from $77 million to $308 million). This represents an increase of more than 300 percent. Most of this increase will be for the construction of a 4Mb DRAM fab, which the Company plans to have completed by March 1990.

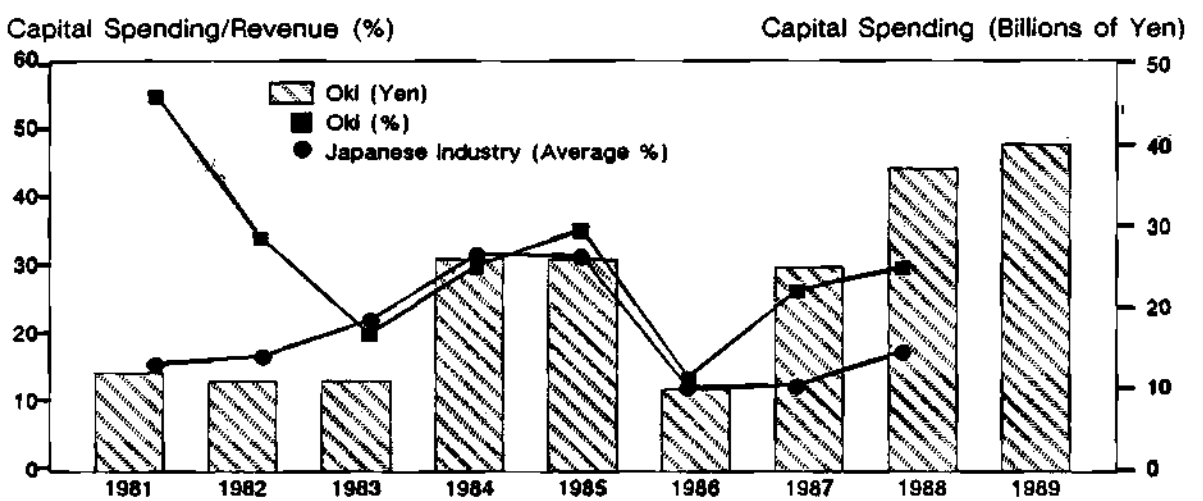
Oki

Oki's ratio of capital spending to revenue was substantially above the Japanese industry average in both 1987 and 1988 (see Figure 7). In 1988, Oki's ratio exceeded 30 percent, more than any other Japanese semiconductor company. However, Oki plans to increase its spending by only 8 percent in 1989, from ¥37 billion to ¥40 billion (from $285 million to $308 million).

A major part of Oki's recent investments was for its 4Mb DRAM plant at Miyagi, Japan. Oki plans to begin production at this plant in the second half of 1989.

Figure 7

Oki
Capital Spending/Revenue versus Industry Average
and Total Capital Spending



0004587-7

Source: Dataquest August 1989

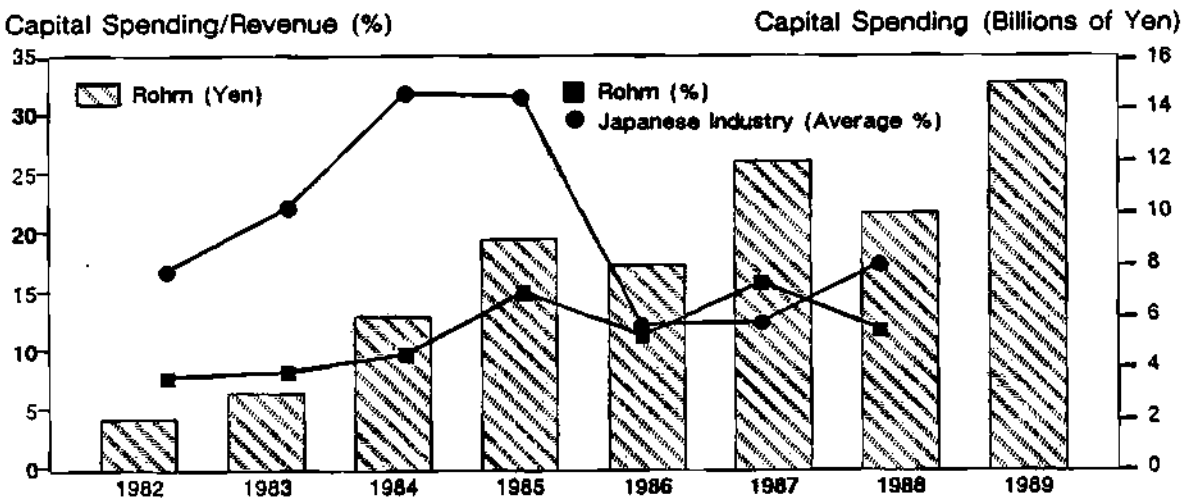
Capital Spending by Company: Japan

Rohm

In 1987, Rohm's ratio of capital spending to revenue was 16 percent and the Japanese industry's average was 13 percent (see Figure 8). However, in 1988, Rohm's level of capital spending fell 17 percent, causing its ratio to fall below the industry's average. Dataquest expects Rohm to increase its capital spending by 50 percent in 1989, from ¥10 billion ($77 million) to ¥15 billion ($115 million).

Figure 8

Rohm
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-8

Source: Dataquest August 1989

Capital Spending by Company: Japan

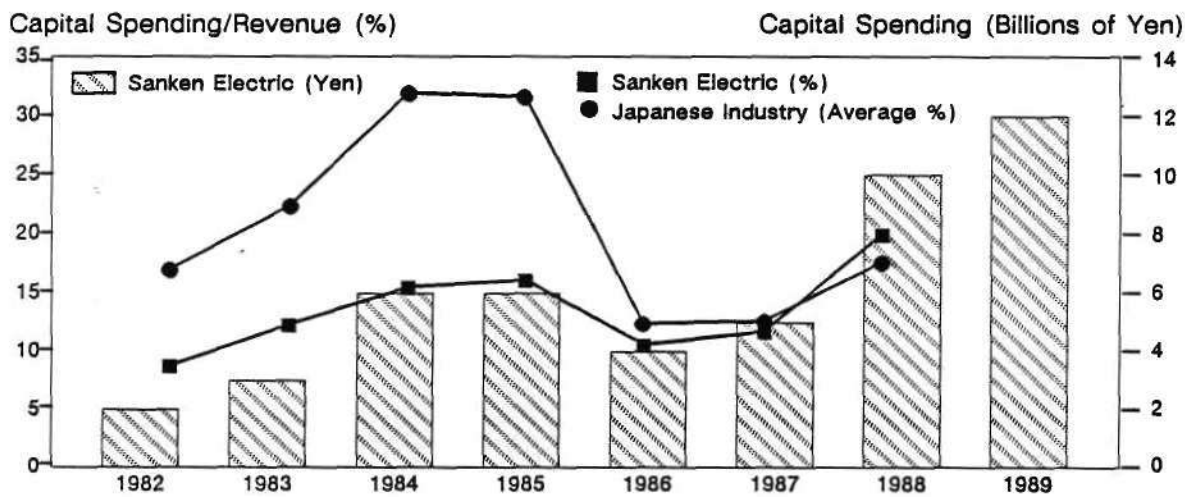
Sanken Electric

Sanken's ratio of capital spending to revenue was close to the Japanese industry average in 1986, 1987, and 1988. Before 1986, however, its ratio was significantly below the industry's average (see Figure 9).

In 1988, Sanken completed its new fab at Yamagata, Japan. The Company's current plans include building two new assembly plants, one at Ishikawa, Japan, and another at Kashima, Japan. Sanken's capital spending will increase 20 percent in 1989, from ¥10 billion ($77 million) in 1988 to ¥12 billion yen in 1989 ($92 million) in 1989.

Figure 9

Sanken Electric
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-9

Source: Dataquest August 1989

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Capital Spending by Company: Japan

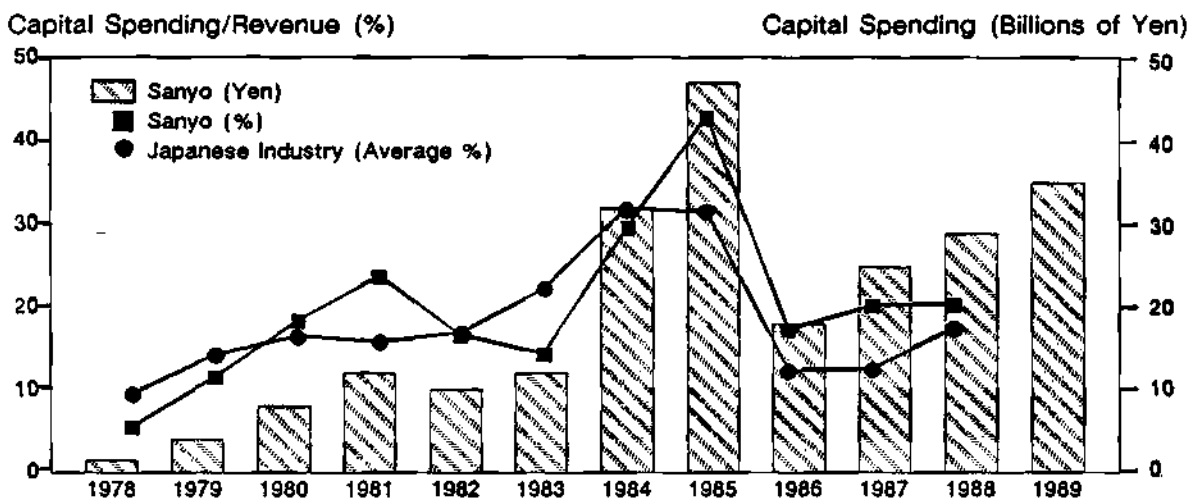
Sanyo

Sanyo's capital spending/revenue ratio has been significantly above the industry's average since 1985 (see Figure 10). Sanyo's capital spending will reach ¥35 billion ($269 million) in 1989, an increase of 21 percent over its 1988 level.

Sanyo started 1Mb production this year at its new plant at Niigata, Japan. Currently, the company is building an ultralarge-scale integrated (ULSI) laboratory for research on 16Mb and 64Mb DRAMs.

Figure 10

Sanyo
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-10

Source: Dataquest August 1989

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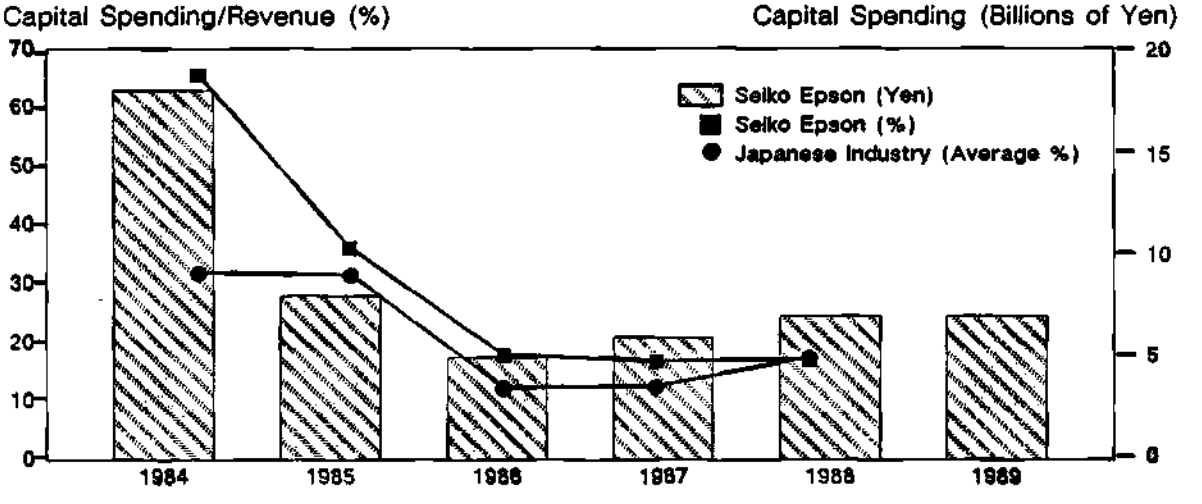
Capital Spending by Company: Japan

Seiko Epson

In 1988, Seiko Epson's ratio of capital spending to revenue was the same as the Japanese industry's average (see Figure 11). The Company's capital-spending level has been flat since 1987, basically hovering around the ¥7 billion ($54 million) level. Dataquest anticipates that Seiko will maintain its spending at this level.

Figure 11

Seiko Epson
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-11

Source: Dataquest August 1989

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Capital Spending by Company: Japan

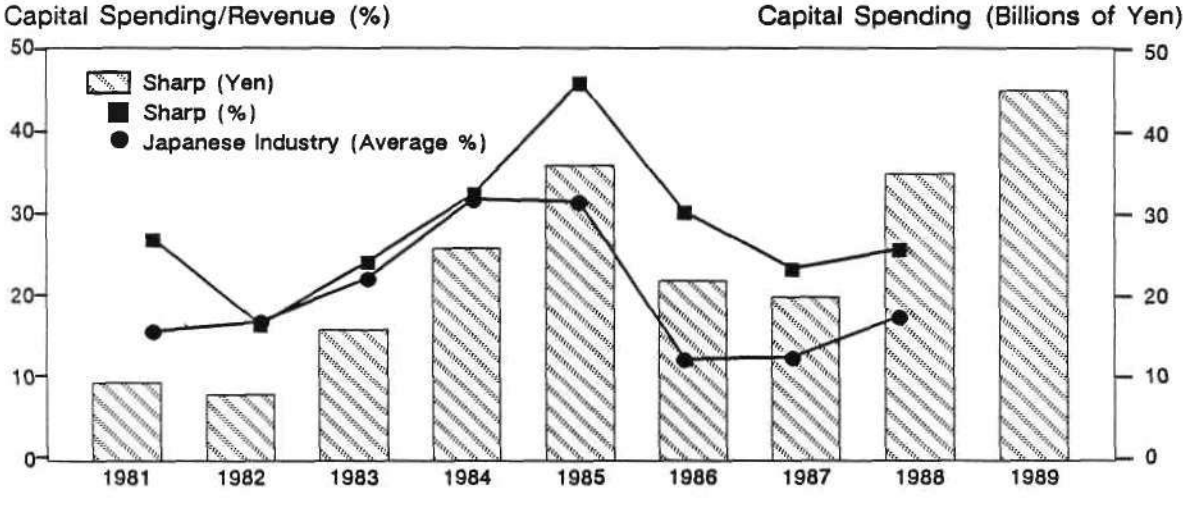
Sharp

Sharp's ratio of capital spending to revenue has been significantly above the Japanese industry's average since 1985 (see Figure 12). Dataquest expects Sharp to increase its capital spending by 29 percent in 1989, from ¥35 billion ($269 million) in 1988 to ¥45 billion ($346 million) in 1989.

In 1988, Sharp began construction of a ¥25 billion ($200 million) 1Mb DRAM plant at its existing facility in Fukuyama in Hiroshima Prefecture, Japan. This new fab will have a computer-intregrated manufacturing (CIM) system developed by Sharp's U.S. subsidiary, Sharp Microelectronics Technology. Dataquest also has heard reports that Sharp will resurrect a fab that was begun as a joint venture by RCA and Sharp. This fab will be located in Camus, Washington, in the United States.

Figure 12

Sharp
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-12

Source: Dataquest August 1989

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Capital Spending by Company: Japan

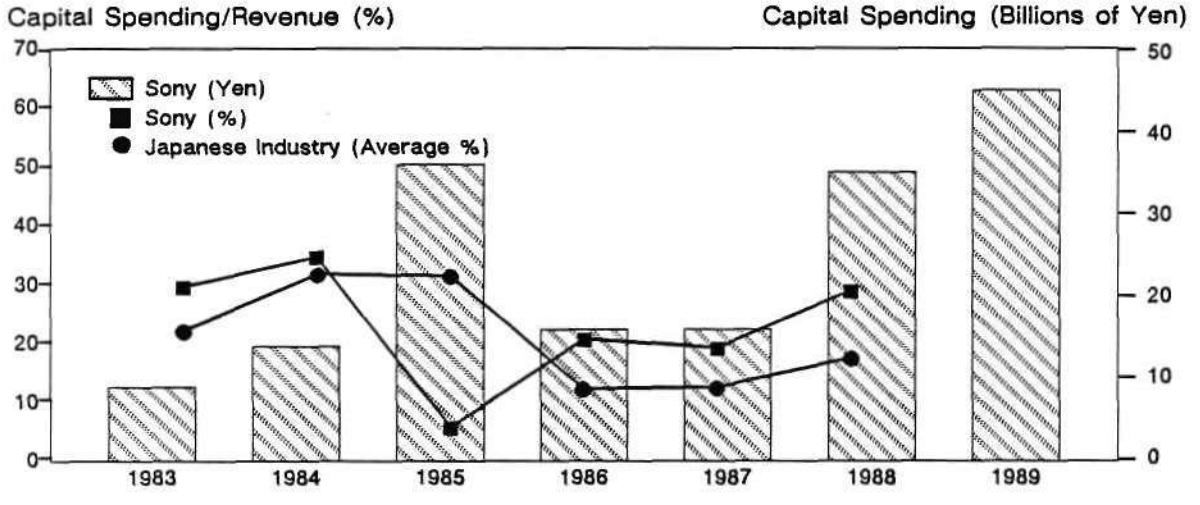
Sony

Sony's ratio of capital spending to revenue has been above the Japanese industry's average since 1985 (see Figure 13). Dataquest believes that Sony will increase its capital spending by 29 percent in 1989, from ¥35 billion ($269 million) to ¥45 billion ($346 million).

Sony will be the first Japanese semiconductor facility to construct a front-end facility in Thailand. This new plant will be located in Bangkadi Industrial Park, outside of Bangkok. Sony expects to begin production at this facility in October 1990. Initial devices fabricated at this facility primarily will be bipolar devices for compact disc (CD) players. Sony also is building a new facility for megabit SRAMs in Nagasaki, Japan. This fab will cost approximately ¥35 billion ($270 million).

Figure 13

Sony
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-13

Source: Dataquest August 1989

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Capital Spending by Company: Japan

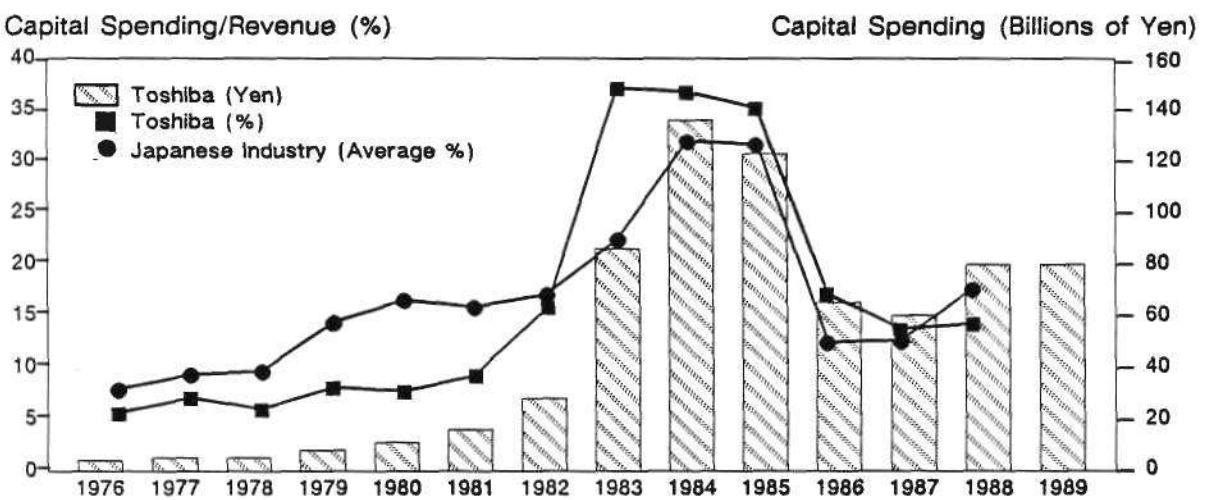
Toshiba

Toshiba's ratio of capital spending to revenue had been slightly above the Japanese industry's average until 1988, when it dipped below the industry's average (see Figure 14). Dataquest expects Toshiba 1989 capital spending to remain at last year's level of ¥80 billion ($615 million). Only two other merchant semiconductor companies in the world (Samsung and Goldstar) will match this level of spending in 1989.

Dataquest expects Toshiba to begin construction of a 4Mb-DRAM fab at its Ohita plant this year. The Company plans to spend ¥70 billion ($260 million) on this fab, which also will include a 16Mb DRAM prototype line.

Figure 14

Toshiba
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-14

Source: Dataquest August 1989

Capital Spending by Company

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Capital Spending by Company

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Capital Spending by Company

SUMMARY

This service section will report the results of Dataquest's latest survey of capital spending plans by Japanese and United States semiconductor companies. Knowledge of capital spending plans is useful to semiconductor manufacturers because it is an essential element of any competitive analysis or capacity analysis. Knowledge of current spending plans of manufacturers can help semiconductor equipment manufacturers to identify sales leads and to direct existing resources to the best markets.

NORTH AMERICAN COMPANY CAPITAL SPENDING

Dataquest surveys the major North American semiconductor manufacturers several times a year to track their capital spending plans. We have noted a strengthening of optimism as this year has progressed. Table 1 provides a summary of the history of capital spending in the United States by company and the change in spending from 1987 to 1988.

In 1985, capacity utilization for all U.S. companies fell to an all-time low of 51 percent. In 1988, capacity utilization will rise to 88 percent. Capacity utilization for leading-edge devices is even higher, and, in some cases, demand exceeds supply. Due to these increasing rates of utilization, the percent of capital spending devoted to property and plant is the highest since 1985 (see Figure 1).

Continuing the trend which began in 1987, most U.S. companies are planning to increase their capital spending. Intel, Motorola, and Texas Instruments will each spend more than $400 million on property, plant, and equipment. Micron Technology will increase is spending by more than 700 percent as it adds a new fab to its manufacturing inventory.

Individual U.S. company capital spending-to-revenue ratios for the period 1975 through 1987 are given in Table 2.

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Capital Spending by Company

Table 1

U.S. Company Capital Spending
(Millions of Dollars)

Company	1980	1981	1982	1983	1984
Advanced Micro Devices	$ 49	$ 58	$ 67	$ 121	$ 308
Analog Devices	19	16	19	24	58
Fairchild	83	140	156	125	195
General Electric	N/A	N/A	N/A	64	107
General Instruments	N/A	N/A	N/A	N/A	9
Harris	45	45	35	31	47
IDT	N/A	N/A	N/A	2	4
Intel	156	157	138	146	388
LSI Logic	N/A	N/A	6	30	82
Thomson-Mostek	85	98	47	78	123
Monolithic Memories	6	20	25	N/A	N/A
Micron Technology	N/A	N/A	5	29	58
Motorola	177	184	160	174	412
National Semiconductor	199	245	238	245	495
Texas Instruments	300	145	140	232	472
Others	312	265	251	324	577
Total	$1,347	$1,233	$1,131	$1,499	$3,139

(Continued)

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Capital Spending by Company

Table 1 (Continued)

U.S. Company Capital Spending
(Millions of Dollars)

Company	1985	1986	1987	1988	Percent Change 1987-88
Advanced Micro Devices	$ 243	$ 102	$ 138	$ 180	30%
Analog Devices	62	37	50	50	(1%)
Fairchild	135	135	N/A	N/A	N/A
General Electric	81	50	45	50	11%
General Instrument	12	8	12	20	67%
Harris	52	37	30	30	0
IDT	25	18	18	37	103%
Intel	214	155	302	450	49%
LSI Logic	40	71	135	60	(56%)
Thomson-Mostek	N/A	N/A	N/A	N/A	N/A
Monolithic Memories	N/A	N/A	N/A	N/A	N/A
Micron Technology	32	11	14	120	769%
Motorola	330	250	350	430	23%
National Semiconductor	319	223	157	200	27%
Texas Instruments	281	217	231	410	77%
Others	374	266	352	530	51%
Total	$2,065	$1,445	$1,834	$2,566	40%

*Columns may not add to totals shown because of rounding.

N/A = Not Applicable

Source: Dataquest
August 1988

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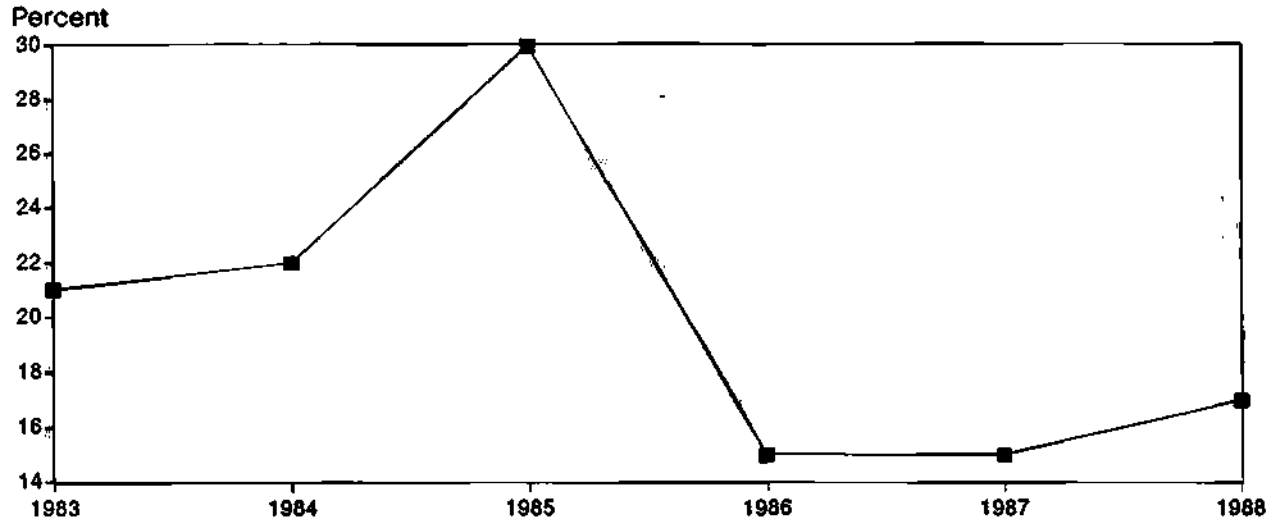
Capital Spending by Company

Figure 1

U.S. Property and Plant Capital Spending as a Percent of Total Capital Spending



Source: Dataquest August 1988

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Capital Spending by Company

Table 2

U.S. Company Capital Spending as a Percent of Revenue

Company	1980	1981	1982	1983	1984	1985	1986	1987
AMD	17.2%	20.8%	20.4%	19.0%	27.1%	30.9%	12.1%	13.6%
Analog Devices	24.9%	18.5%	18.3%	16.6%	26.7%	27.6%	15.3%	18.4%
Fairchild	14.7%	30.3%	38.0%	27.5%	29.3%	27.4%	N/A	N/A
General Electric	N/A	N/A	N/A	13.0%	17.0%	16.0%	9.6%	7.9%
General Instrument	N/A	N/A	N/A	N/A	3.1%	5.5%	3.4%	4.4%
Harris	24.3%	27.3%	22.4%	17.8%	18.2%	21.1%	20.0%	13.4%
IDT	N/A	N/A	N/A	22.5%	12.9%	8.0%	25.3%	18.6%
Intel	27.1%	29.9%	22.1%	18.8%	32.3%	21.0%	15.6%	20.1%
LSI Logic	N/A	N/A	98.3%	93.7%	97.9%	28.5%	36.6%	51.9%
Thomson-Mostek	25.8%	46.7%	21.4%	24.8%	33.2%	35.5%	6.5%	N/A
Micron Technology	N/A	N/A	103.5%	119.0%	49.4%	90.1%	18.0%	12.0%
Monolithic Memories	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Motorola	15.9%	15.5%	13.1%	10.6%	17.8%	18.0%	12.3%	14.3%
National Semi	15.2%	20.3%	21.3%	17.9%	26.4%	22.5%	16.4%	11.0%
Texas Instruments	19.0%	11.2%	10.7%	14.2%	19.0%	16.1%	11.9%	10.9%
Total	16.7%	17.7%	15.6%	16.1%	22.9%	19.7%	14.2%	12.9%

N/A = Not Applicable

Source: Dataquest
August 1988

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Capital Spending by Company

Advanced Micro Devices (AMD)

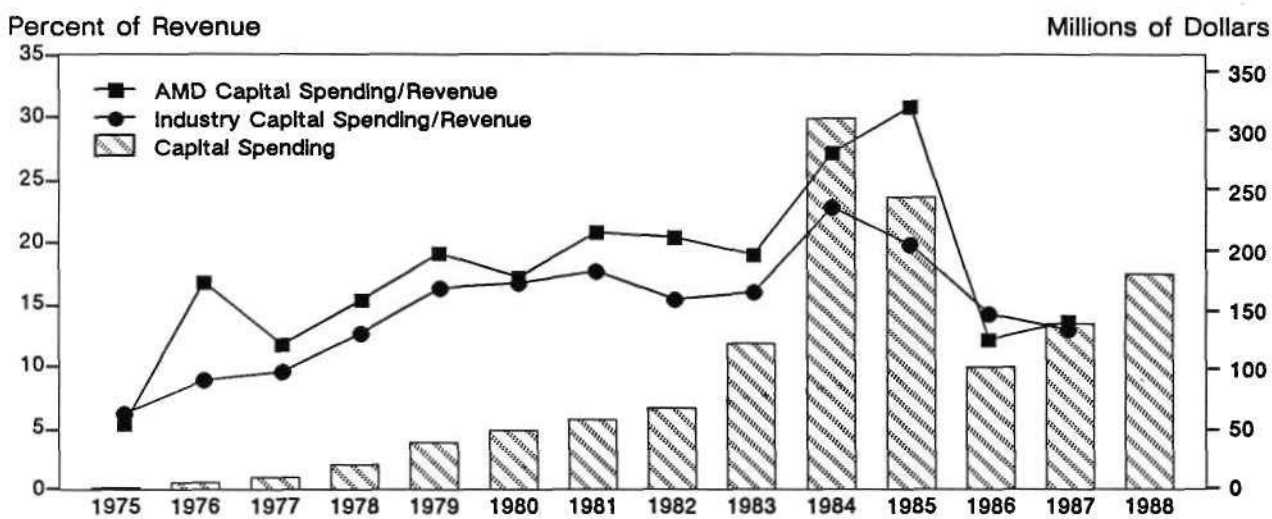
We have included Monolithic Memories' (which recently merged with AMD) revenue and capital expenditures with AMD's back to 1983.

AMD's capital spending–to–revenue ratio has generally exceeded the industry's average (see Figure 2). In 1987, AMD spent $138 million, or 13.6 percent of its revenue, on capital spending. AMD plans to spend $180 million in 1988, up 30 percent from its 1987 spending level. Dataquest estimates that approximately 90 percent of 1988's spending will be for equipment and the remaining 10 percent will be for property and plant. AMD will focus its spending on equipment to increase and enhance yields, throughput, and reliability.

In October of this year, AMD will break ground for its new submicron R&D facility in Santa Clara.

Figure 2

AMD versus Industry Average Capital Spending/Revenue



Source: Dataquest August 1988

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Capital Spending by Company

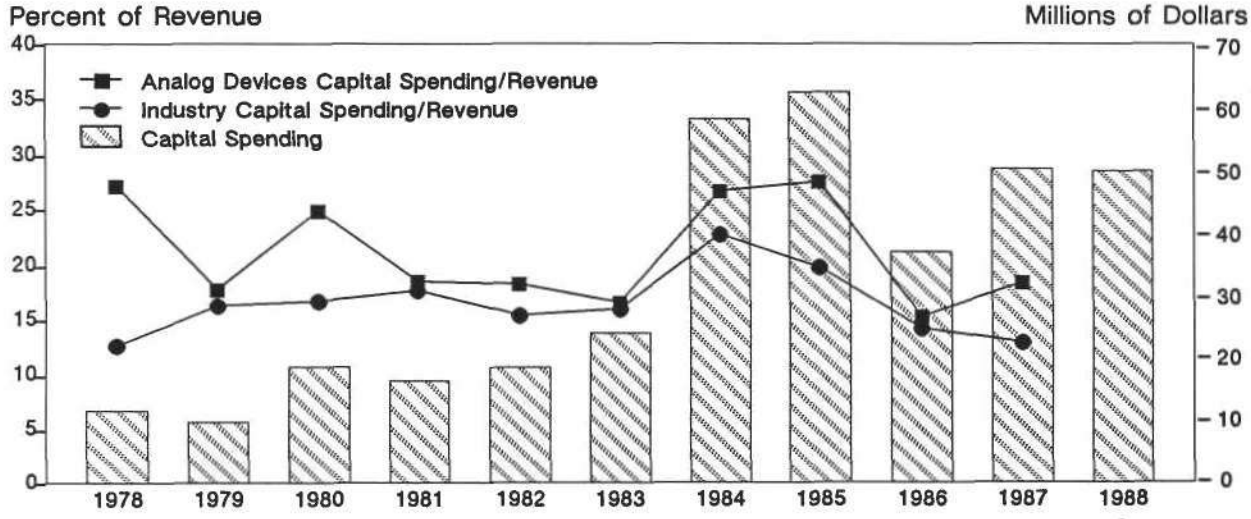
Analog Devices

Analog Devices' capital spending-to-revenue ratio has always been above the industry's average (see Figure 3). Indeed, in 1987 its ratio of 18.4 percent exceeded the industry's average by 4.2 percentage points. We estimate that its capital spending in 1988 will be at the same level as it was in 1987: $50 million.

Completion of Analog's new engineering and R&D facility in Wilmington, Delaware, has been postponed and no new date has been set. The focus of Analog's spending will continue to be the expansion of back-end capacity, especially at its Manila facility.

Figure 3

Analog Devices versus Industry Average Capital Spending/Revenue



Source: Dataquest
August 1988

Capital Spending by Company

General Electric (GE)

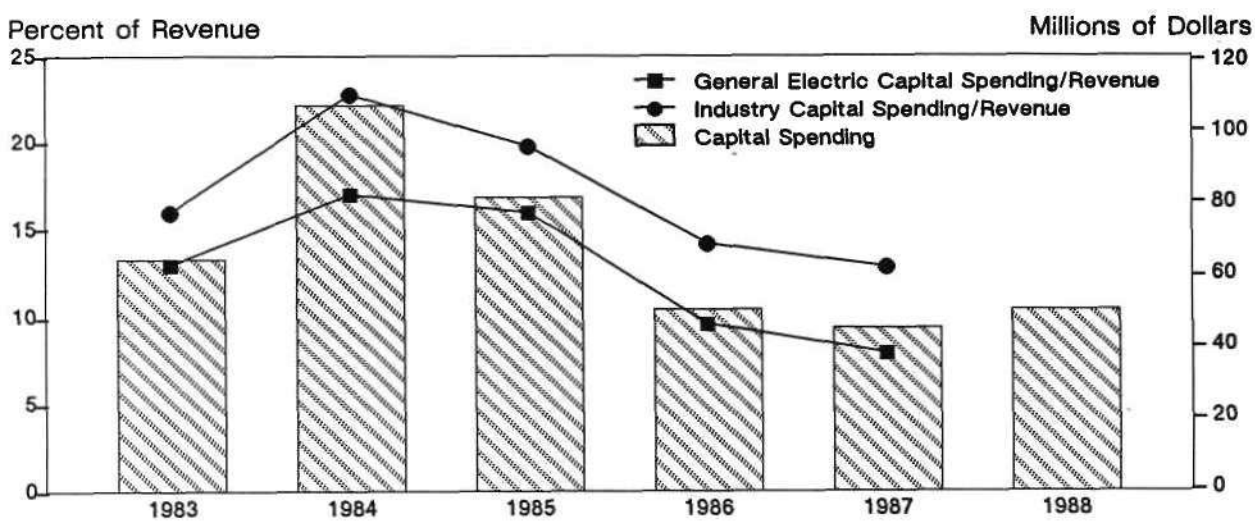
GE's capital spending (which includes that of the recently acquired RCA as well as Intersil) as a percent of revenue has generally been below the industry's average (see Figure 4). In 1987, GE's capital spending-to-revenue ratio stood at 7.9 percent compared with the industry average of 13.2 percent.

General Electric's combined capital spending reached its peak in 1984 at $107 million. Its level in 1987 was about $45 million, less than one-half its 1984 level. We estimate that GE's 1987 spending level will rise only slightly to $50 million. We believe that it is possible that GE will sell some of its RCA operations.

GE will increase capacity on its 1.5-micron ASIC line at Findley, Pennsylvania. Another focus of GE's spending will be its Mt. Top, Ohio, facility for power IC's.

Figure 4

General Electric versus Industry Average Capital Spending/Revenue



Source: Dataquest August 1988

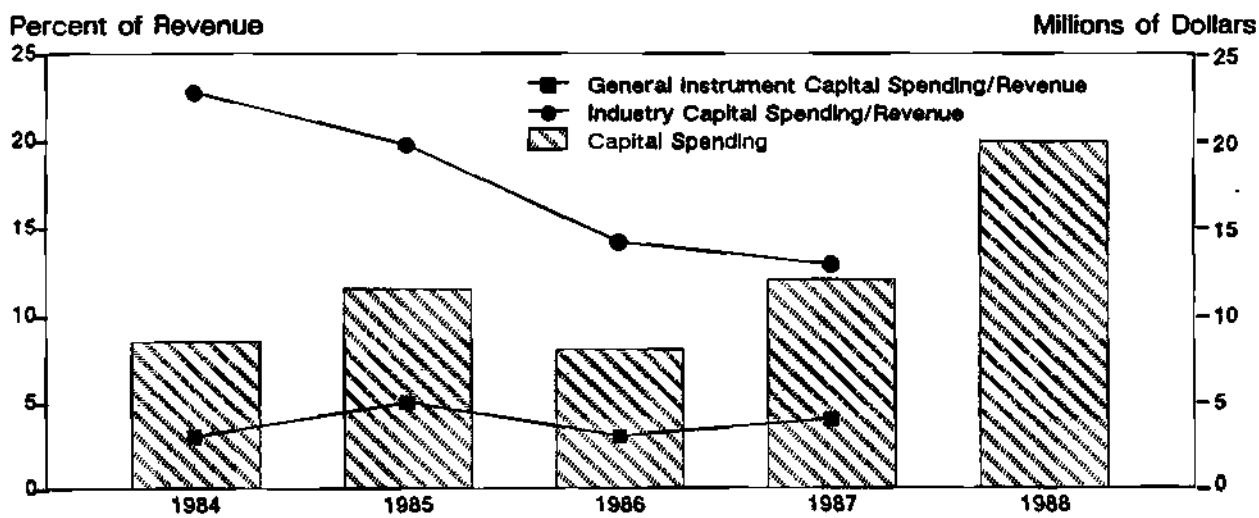
Capital Spending by Company

General Instruments

General Instruments' ratio of capital spending–to–revenue has always been several points below the industry's average (see Figure 5). General Instruments will spend $20 million this year, up 67 percent from its level of $12 million in 1987. General Instruments reports that it increased its capacity by 20 percent in 1987 through mechanization of its test and assembly operations. Most of its spending since 1984 has been for its front–end facility in Taiwan. Its focus in the future will be on mechanization of its fab in Taiwan.

Figure 5

General Instrument versus Industry Average Capital Spending/Revenue



Source: Dataquest August 1988

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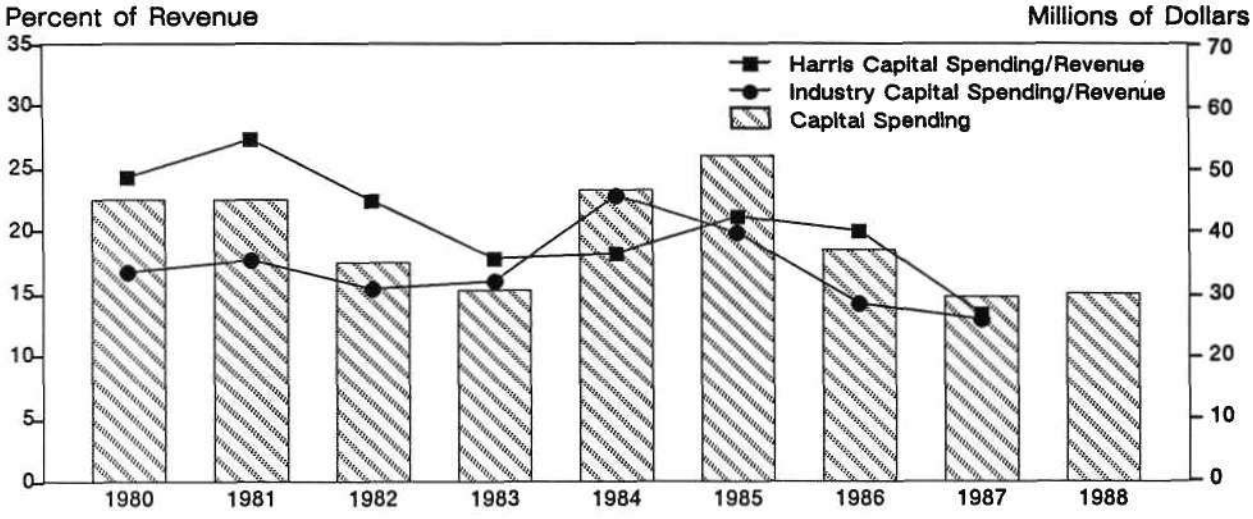
Capital Spending by Company

Harris

With the exception of 1983 and 1984, Harris' capital spending–to–revenue ratio has been above that of the industry (see Figure 6). We estimate that Harris spent $30 million in 1988, approximately what it spent in 1987. The focus of this spending will be a new wafer facility, to upgrade and expand existing facilities, and to expand its R&D facilities. Those fabs receiving upgrades include the Custom Integrated Circuits division in Melbourne, Florida, which makes 1–micron, radiation–hardened CMOS devices for the Strategic Defense Initiative (SDI) program, and also the Semiconductor Products division, also in Melbourne.

Figure 6

Harris versus Industry Average Capital Spending/Revenue



Source: Dataquest August 1988

Capital Spending by Company

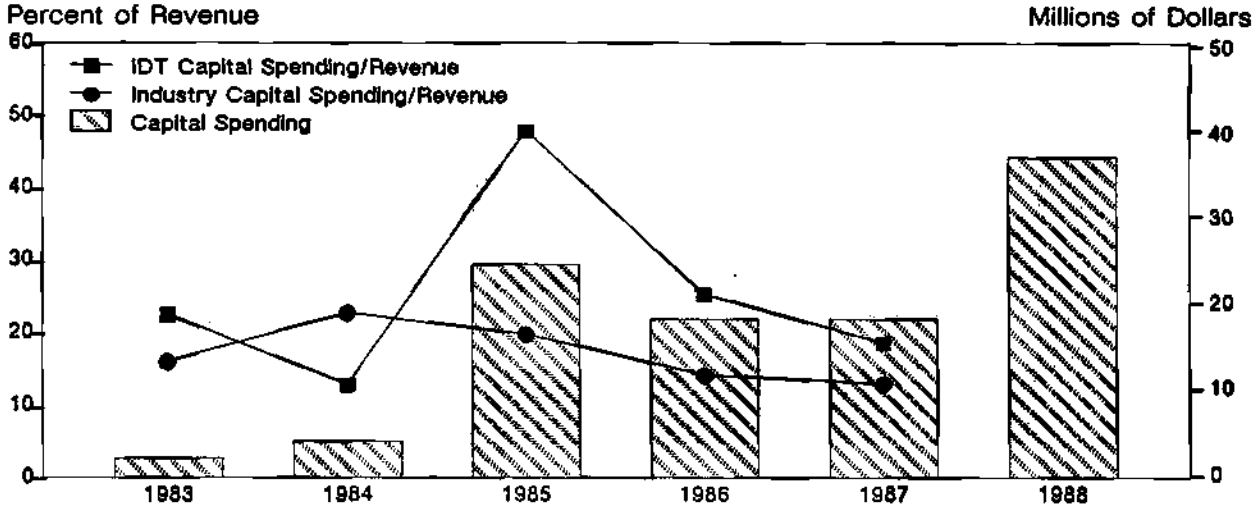
Integrated Device Technology (IDT)

IDT's capital spending-to-revenue ratio has generally been above the industry's average (see Figure 7). In 1987 its ratio stood at more than 18 percent.

IDT's 1988 capital spending will be $37 million, up 103 percent over its 1987 level of $18 million. IDT will be buying equipment, such as steppers, to increase capacity at its Salinas, California, fab. Testers for its Penang, Malaysia, test facility will be another focus of IDT's spending. IDT hopes to have its new R&D facility in Santa Clara, California, completed by the end of this year or by the first quarter of 1989.

Figure 7

IDT versus Industry Average Capital Spending/Revenue



Source: Dataquest August 1988

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Capital Spending by Company

Intel

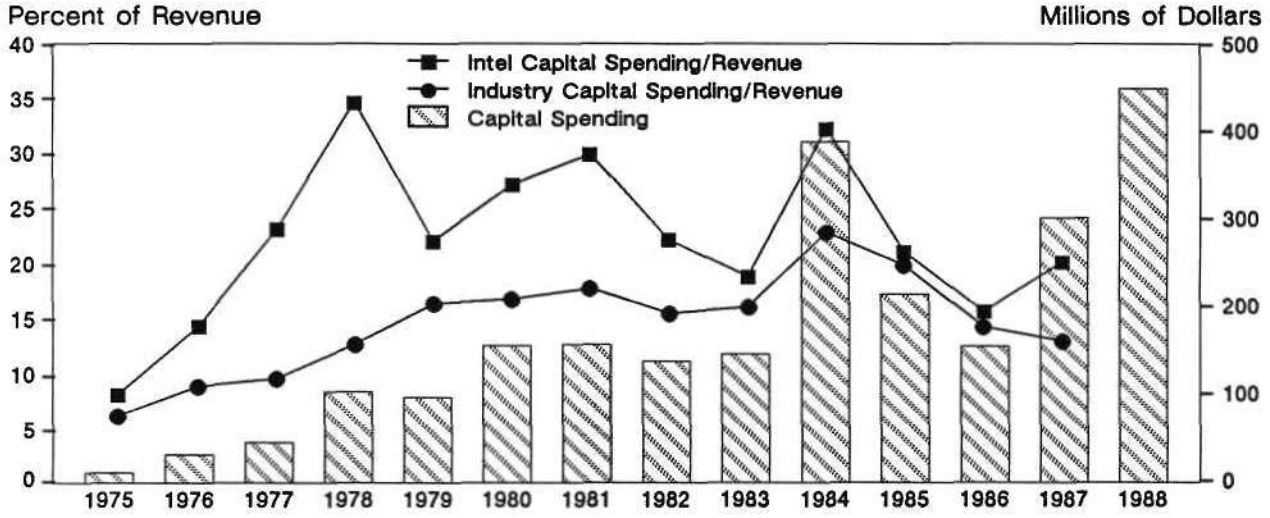
Every year since 1975 (with the exception of 1985) Intel's capital spending–to–revenue ratio has exceeded the industry average (see Figure 8). In 1987, Intel's capital spending–to–revenue ratio was more than 20 percent.

Intel's capital spending will be higher than any other merchant semiconductor vendor in the United States in 1988. Intel's capital spending in 1987 increased by 93 percent to $302 million. We estimate that in 1988 Intel will increase its capital spending by 50 percent to $450 million. The main focus of its spending will be upgrading Fab 7, completing Fab 9.1, and putting in Fab 9.2 in Albuquerque, New Mexico. Fab 9.2 will run either high–end logic or EPROMs.

Fab 7 at Albuquerque is currently Intel's largest fab, accounting for 25 percent of Intel's silicon output. Fab 9, however, when complete, will be twice the size of Fab 7. When all four modules in Fab 9 are complete, Intel estimates that its total capital expenditures will be approximately $650 million.

Figure 8

Intel versus Industry Average Capital Spending/Revenue



Source: Dataquest August 1988

Capital Spending by Company

Intel recently announced that it plans to construct an advanced manufacturing development facility in Santa Clara, California. Intel plans to spend $95 million on this facility, which it claims will be one of the most advanced development sites in the world. The facility will be 200,000 square feet and will be dedicated to the development of submicron manufacturing processes focused on non-volatile memory devices and microcontrollers. It is scheduled for completion in April 1989. The facility will have 35,000 square feet of Class I clean room.

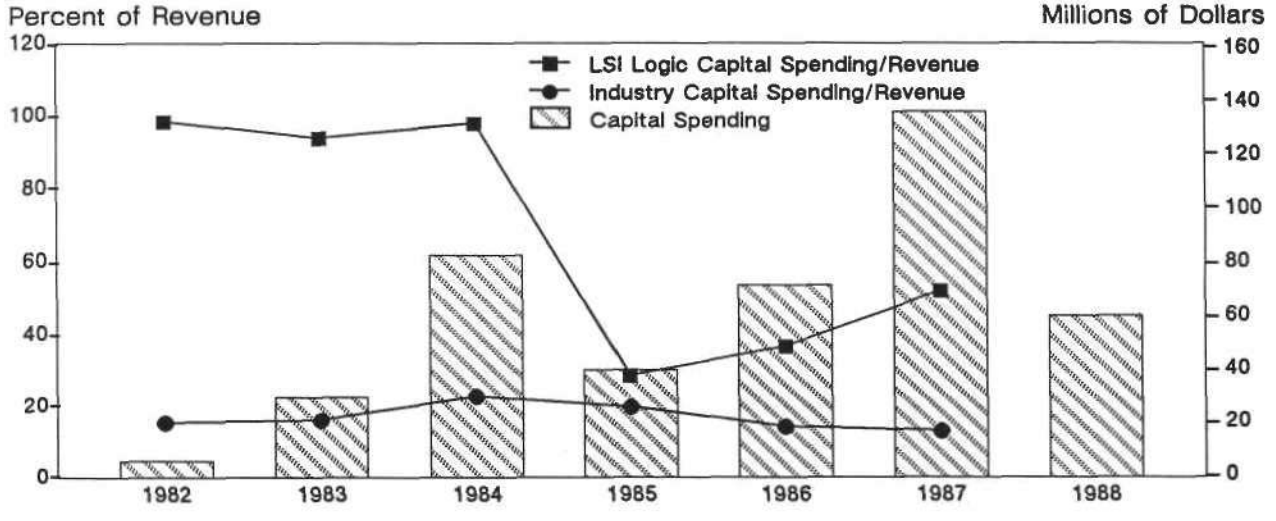
Intel is going ahead with its plans to double its equipment utilization, and we expect it to invest significantly in automation to achieve this goal.

LSI Logic

LSI Logic, which was incorporated in 1980, has had a very high capital spending-to-revenue ratio as it put in fabs and equipment before its revenue stream became very large. In 1987, LSI's capital-to-revenue ratio was 51.9 percent (see Figure 9).

Figure 9

LSI Logic versus Industry Average Capital Spending/Revenue



Source: Dataquest August 1988

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Capital Spending by Company

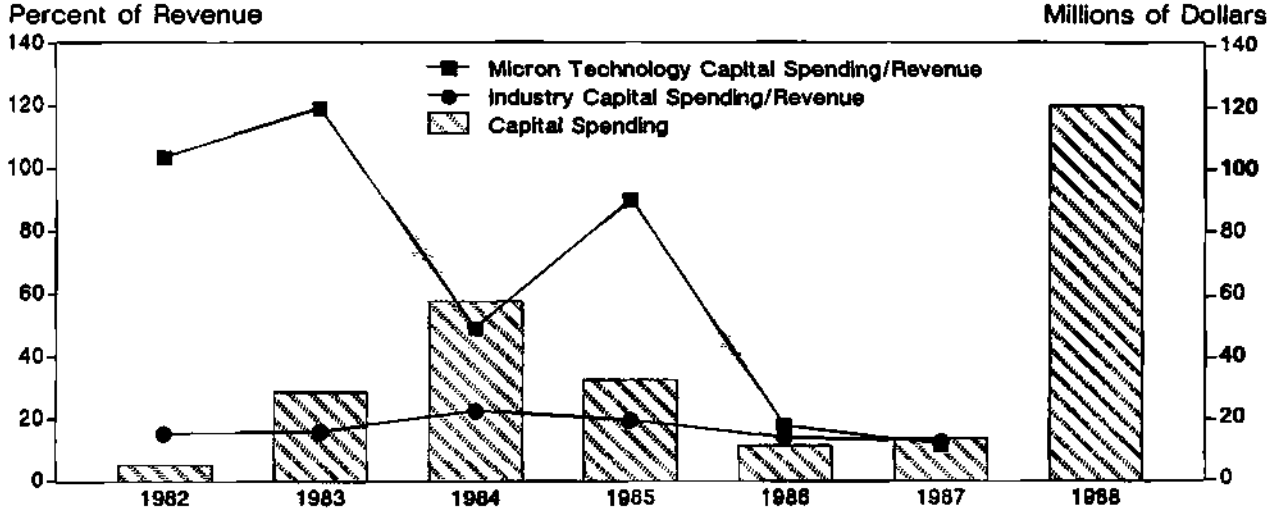
In 1984, the focus of LSI's spending was the establishment of its Santa Clara fab. In 1986 LSI began to convert from 4-inch wafers to 5-inch wafers and also began construction of Nihon Semiconductor in Japan. Nineteen eighty-seven saw the completion of its Nihon Semiconductor facility and the beginning of work on its new facility in Braunshweig, West Germany, which is expected to be completed in 1988. Because its new fabs are either completed or almost complete, we expect LSI's spending will decline 56 percent this year, from $135 million in 1987 to $60 million in 1988.

Micron Technology

Micron Technology's capital spending-to-revenue ratio has been above the industry's average every year since 1982. In the period 1982 to 1985 its capital spending-to-revenue ratio ranged from a low of 50 percent of revenue to a high of 120 percent of revenue in 1982 (see Figure 10). Prior to 1985, these high ratios were due to its building capacity as a start-up (Micron was incorporated in 1978). Its spending ratio in 1985 was due to the downturn in revenue associated with the semiconductor industry's recession, especially in the DRAM market. In 1987, Micron's capital spending-to-revenue ratio was below the industry average.

Figure 10

Micron Technology versus Industry Average
Capital Spending/Revenue



Source: Dataquest
August 1988

Capital Spending by Company

In 1988, however, Micron is responding to the current DRAM shortage by increasing its capital spending by 769 percent, from $14 million in 1987 to $120 million in 1988. Micron will be spending approximately $100 million to build and equip its new 100,000-square-foot fab. Micron hopes to have this fab in production by the first quarter of 1989. This fab will have a 150mm line with a 20,000-wafer start-per-month capacity. Micron is also spending approximately $13 million on new equipment to upgrade its current fabs.

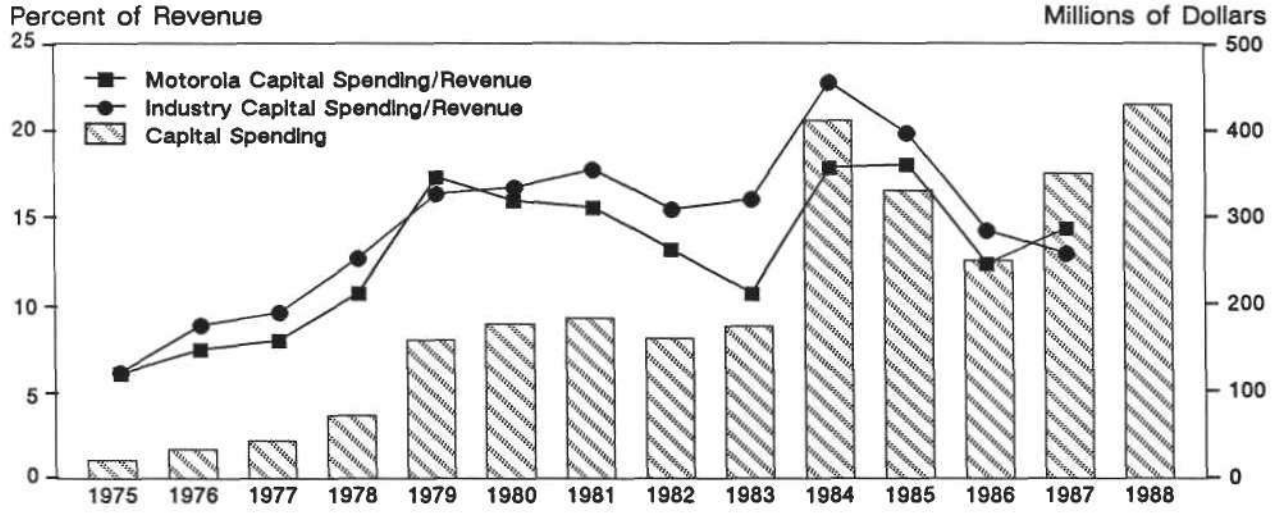
Motorola

Motorola's capital spending-to-revenue ratio in 1987, 14.3 percent, exceeded the industry's average for the first time since 1980 (see Figure 11).

Dataquest estimates that Motorola's capital spending for calendar 1988 will be up 23 percent, from $350 million in 1987 to $430 million in 1988. This does not include expenditures for its joint venture with Toshiba.

Figure 11

Motorola versus Industry Average Capital Spending/Revenue



Source: Dataquest August 1988

Capital Spending by Company

Motorola's reentry into DRAM manufacture, with facilities in the United States and Europe, will be accomplished using a 1.2-micron CMOS architecture developed in a joint venture with Toshiba. Motorola is transferring the process from Japan to its MOS-6 fab in Mesa, Arizona, and its MOS-9 in East Kilbride, Scotland. MOS-6 will be in pilot production by the end of the year. MOS-6 will have a 150mm line that will be capable, eventually, of submicron processing. According to rumors, a new fab, MOS-12, will manufacture 4Mb DRAMs in Austin, Texas, in the 1990s.

Motorola plans to have pilot production underway at its new commodity factory in Seremban, Malaysia, by the end of the year. An assembly facility already exists at this site. This new fab will be a fully integrated manufacturing facility from front end to final test, and will manufacture power transistors.

Also, Motorola recently purchased seven acres of land in Hong Kong to build a facility to house its various Hong Kong operations. These operations include its Asian-Pacific headquarters, a design center, and an assembly/test facility. The size of this new building will be 300,000 square feet. Dataquest estimates that Motorola will spend $50 million to equip this facility.

National Semiconductor

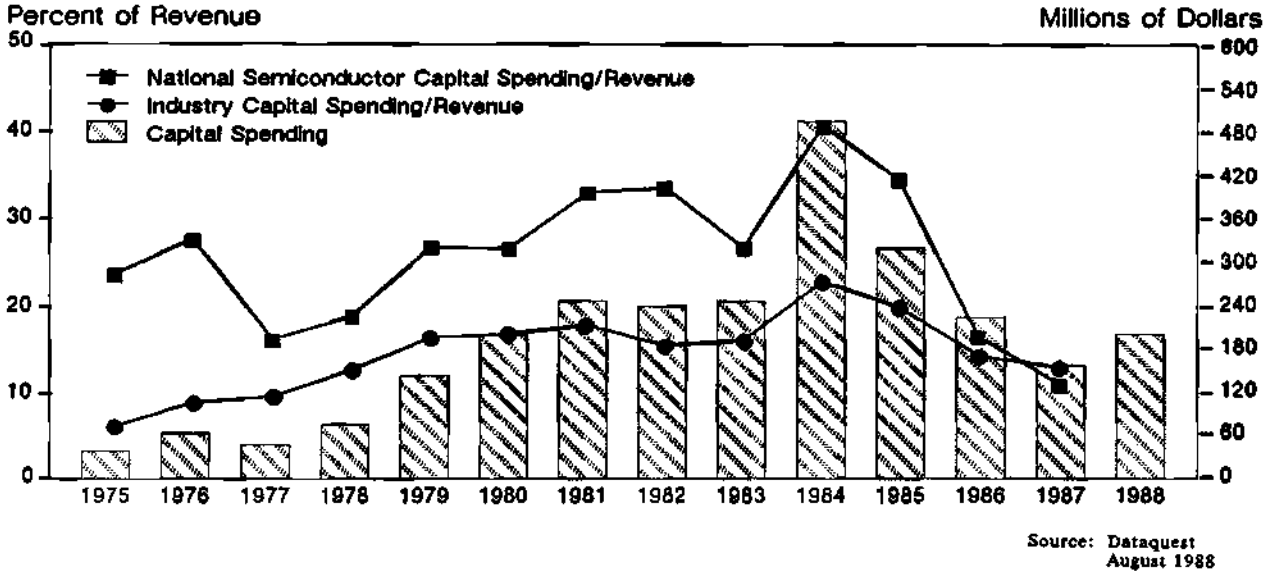
National Semiconductor's capital spending-to-revenue ratio stood at 26 percent in 1984 when National was building its Arlington, Texas, facility. Since then, it has fallen. In 1987, it was 11 percent of revenue (see Figure 12).

Dataquest estimates that National will increase its capital spending by 27 percent in 1988, from $157 million in 1987 to $200 million in 1988. National will be directing its spending to adding capacity at Puyallup, Washington; Arlington, Texas; and at Salt Lake City, Utah.

Capital Spending by Company

Figure 12

National Semiconductor versus Industry Average Capital Spending/Revenue



Source: Dataquest August 1988

Philips–Signetics

Dataquest estimates that Signetics will increase its capital spending by 32 percent in 1988, from $95 million in 1987 to $125 million in 1988. The focus of this spending will be equipping its new fab (Fab 23) in Albuquerque, New Mexico, as well as Fabs 22 and 21, also in Albuquerque. Fab 23 is a 150mm, CMOS line that is capable of manufacturing 1.0–micron devices. It will have 30,000 square feet of clean room and eventually have a wafer–start capacity of 30,000 wafers per month.

Capital Spending by Company

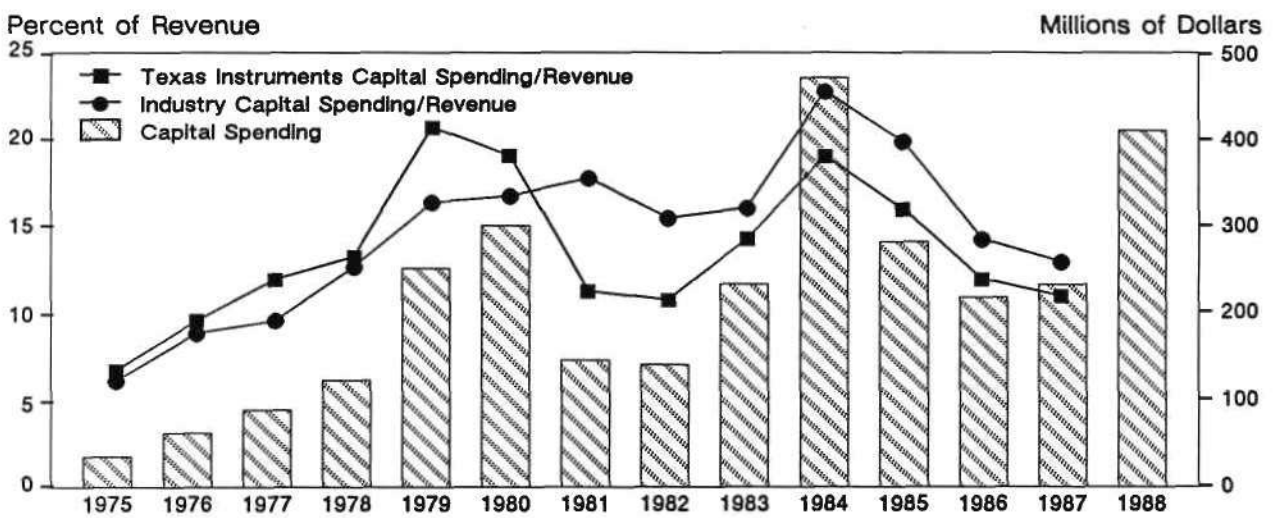
Texas Instruments

Texas Instruments' capital spending-to-revenue ratio has been below the industry's average since 1981. In 1987, Texas Instruments' ratio stood at 10.9 percent, significantly below the industry's average (see Figure 13). However, Dataquest estimates that Texas Instruments will increase its capital spending by 79 percent in 1988, from $231 million in 1987 to $410 million in 1988. A significant amount of this increase will be to increase DRAM capacity, both in Texas and in Japan.

Texas Instruments plans to begin sampling 4Mb DRAMs in 1988 and begin pilot production at Miho, Japan, in 1989. Texas Instruments is currently ramping up volume production of 1Mb DRAMs at its DMOS IV facility in Dallas, Texas. In addition to advanced logic and DRAM capacity, Texas Instruments is also expanding its assembly operations in the Baguio City Export Zone, the Philippines. Reportedly, the company will spend up to $34.5 million in Baguio City to add the assembly of quad flat packs as well as to increase production of plastic leaded chip carriers.

Figure 13

Texas Instruments versus Industry Average Capital Spending/Revenue



Source: Dataquest August 1988

Capital Spending by Company

JAPANESE COMPANY CAPITAL SPENDING

Japanese company capital spending will increase 41 percent to ¥476 billion in calendar year 1988, after a 14 percent increase in 1987. Toshiba, Hitachi, and NEC alone will account for 35 percent of total Japanese capital spending. Fujitsu plans to double its spending from ¥20 billion to ¥40 billion in 1988 (see Tables 3 & 4). Capital spending as a percent of revenue is shown in Table 5.

Table 3

Japanese Calendar Year Capital Spending
(Billions of Yen)

Company	1980	1981	1982	1983	1984	1985	1986	1987	1988	Percent Change 1987-88
Fuji Electric	0	0	¥ 4	¥ 6	¥ 12	¥ 12	¥ 5	¥ 3	¥ 5	67%
Fujitsu	¥ 25	¥ 32	35	53	115	72	16	20	40	100%
Hitachi	21	33	36	62	120	92	22	30	55	83%
Nihon Semi	0	0	0	0	0	0	5	15	3	(80%)
Matsushita	20	19	9	21	110	60	25	22	30	36%
Mitsubishi	8	13	20	31	65	62	20	15	25	67%
NEC	30	38	42	58	129	123	30	30	50	67%
NJRC	N/A	N/A	2	2	4	5	5	2	5	108%
NMB	0	0	0	0	14	14	5	10	10	0
Oki Electric	12	12	11	11	26	26	10	25	37	48%
Rohm	0	0	2	3	6	9	8	12	10	(17%)
Sanken Electric	0	0	2	3	6	6	4	5	10	100%
Sanyo Electric	8	12	10	12	32	47	18	25	29	16%
Sharp	9	10	8	16	26	36	22	20	26	30%
Shindengen	0	0	1	1	3	3	1	1	2	100%
Seiko Epson	0	0	5	9	18	8	5	6	7	17%
Sony	0	0	5	9	14	36	16	16	32	100%
Toshiba	11	16	28	86	136	123	65	60	60	0
Other	0	0	9	16	34	32	13	20	40	100%
Total	¥144	¥185	¥229	¥399	¥870	¥766	¥295	¥337	¥476	41%

*Columns may not add to totals shown because of rounding.

N/A = Not Available

Source: Dataquest
August 1988

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Capital Spending by Company

Table 4

Japanese Calendar Year Capital Spending
(Millions of Dollars)

Company	1980	1981	1982	1983	1984	1985	1986	1987	1988	Percent Change 1987-88
Fuji Electric	0	0	$ 16	$ 26	$ 51	$ 50	$ 30	$ 21	$ 38	85%
Fujitsu	$111	$145	141	226	485	303	96	139	308	122%
Hitachi	93	149	145	264	506	387	132	208	423	103%
Japan Semi	0	0	0	0	0	0	30	104	23	(78%)
Matsushita	89	86	36	89	464	252	150	153	231	51%
Mitsubishi	36	59	80	132	274	261	120	104	192	85%
NEC	133	172	169	247	544	517	180	208	385	85%
NJRC	0	0	8	9	17	21	30	17	38	131%
NMB	0	0	0	0	59	59	30	69	77	11%
Oki Electric	53	54	44	47	110	109	60	174	285	64%
Rohm	0	0	8	13	25	38	48	83	77	(8%)
Sanken Electric	0	0	8	13	25	25	24	35	77	122%
Sanyo Electric	36	54	40	51	135	197	108	174	223	29%
Sharp	38	43	32	68	110	151	132	139	200	44%
Shindengen	0	0	4	4	13	13	6	7	15	122%
Seiko Epson	0	0	20	38	76	34	30	42	54	29%
Sony	0	0	20	38	59	151	96	111	246	122%
Toshiba	49	72	113	366	574	517	389	417	462	11%
Other	0	0	36	68	143	134	78	139	308	122%
Total	$638	$834	$921	$1,698	$3,671	$3,219	$1,766	$2,345	$3,662	56%

*Columns may not add to totals shown because of rounding.

Source: Dataquest
August 1988

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Capital Spending by Company

Table 5

Japanese Company Capital Spending as a Percent of Revenue

Company	1980	1981	1982	1983	1984	1985	1986	1987
Fuji Electric	N/A	N/A	16%	21%	29%	32%	15%	8%
Fujitsu	40%	39%	30%	34%	41%	30%	7%	7%
Hitachi	15%	18%	16%	21%	25%	23%	6%	7%
Japan Semi	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Matsushita	28%	18%	8%	15%	50%	28%	12%	10%
Mitsubishi	14%	18%	24%	26%	28%	39%	11%	7%
NEC	17%	17%	16%	17%	24%	26%	7%	7%
NJRC	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
NMB	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Oki Electric	N/A	55%	34%	20%	30%	36%	14%	27%
Rohm	N/A	N/A	8%	8%	10%	15%	13%	17%
Sanken Electronics	N/A	N/A	9%	12%	16%	16%	11%	12%
Sanyo Electric	19%	24%	17%	15%	30%	43%	18%	22%
Sharp	N/A	27%	17%	24%	33%	46%	30%	23%
Seiko Epson	N/A	N/A	N/A	N/A	66%	36%	18%	20%
Sony	N/A	N/A	N/A	30%	35%	60%	21%	20%
Toshiba	8%	9%	16%	37%	37%	35%	175%	14%
Others	N/A	N/A	6%	9%	30%	31%	14%	20%
Total	17%	16%	17%	22%	32%	32%	12%	13%

N/A = Not Applicable

Source: Dataquest
August 1988

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Capital Spending by Company

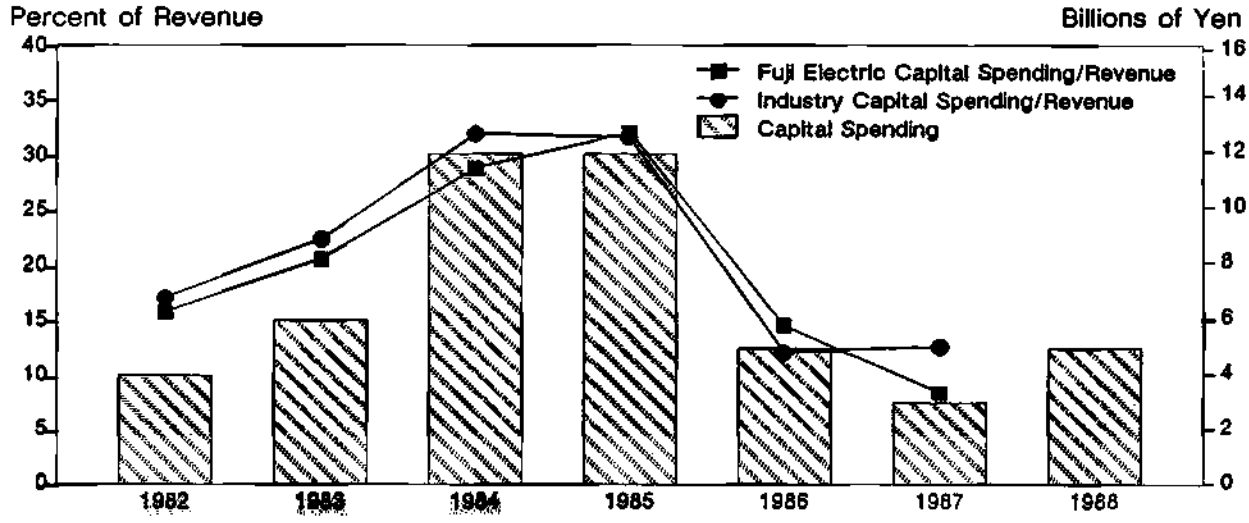
As a further, and final, note to the discussion above regarding the size of Japanese and U.S. industries, Dataquest notes that not one of the top five Japanese semiconductor manufacturers (NEC, Toshiba, Hitachi, Fujitsu, or Mitsubishi) will have capital expenditures at a level anywhere near those they attained in 1984. By contrast, two of the five U.S. manufacturer (Intel and Motorola) will exceed 1984's levels, and Texas Instruments will come very close to attaining its 1984 level of capital spending.

Fuji Electric

Fuji Electric's capital spending–to–revenue ratio has generally paralleled that of the Japanese industry (see Figure 14). Dataquest expects Fuji Electric to increase its capital spending by 67 percent to ¥5 billion in 1988, up from ¥3 billion in 1987.

Figure 14

Fuji Electric versus Industry Average Capital Spending/Revenue



Source: Dataquest August 1988

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Capital Spending by Company

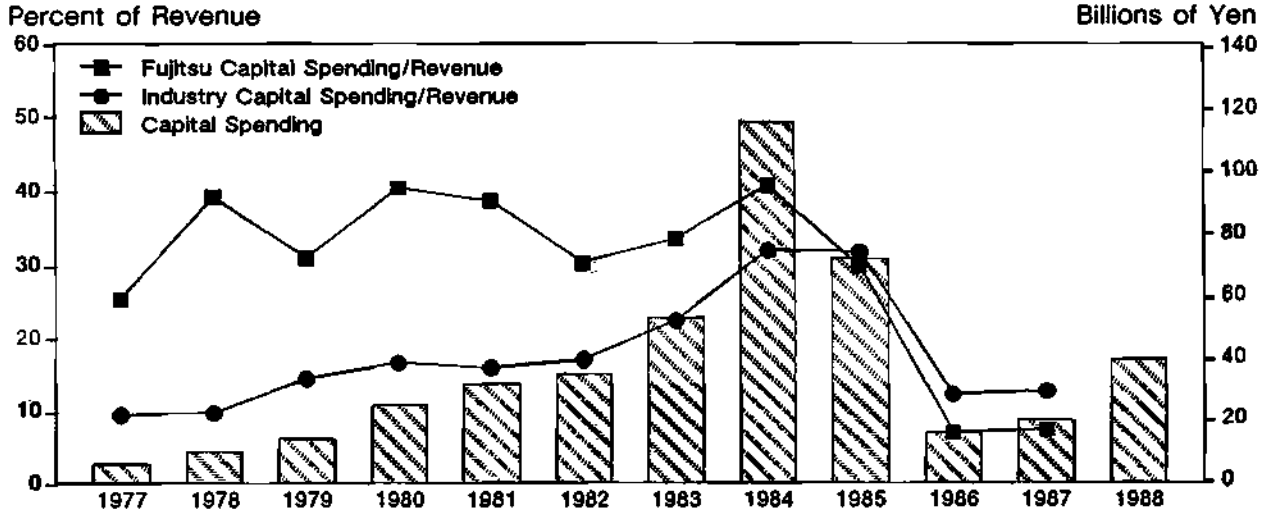
Fujitsu

Until 1984, Fujitsu's capital spending–to–revenue ratio exceeded the average for the Japanese industry. However, since 1985 it has been below the industry average (see Figure 15). Dataquest estimates that Fujitsu will increase its capital spending in 1988 by 100 percent, from ¥20 billion in 1987 to ¥40 billion in 1988.

Fujitsu will spend 25 percent of its capital budget, or ¥10 billion, to build and equip its new ASIC fab in Gresham, Oregon. This will be a 125mm line, capable of producing devices with line geometries of 1.5 microns. Fujitsu reportedly plans eventually to hire 350 employees for this new fab. Fujitsu also plans an extensive refurbishing of its Aizu fab, and an ASIC pilot line at its Miyagi fab.

Figure 15

Fujitsu versus Industry Average Capital Spending/Revenue



Source: Dataquest August 1988

Capital Spending by Company

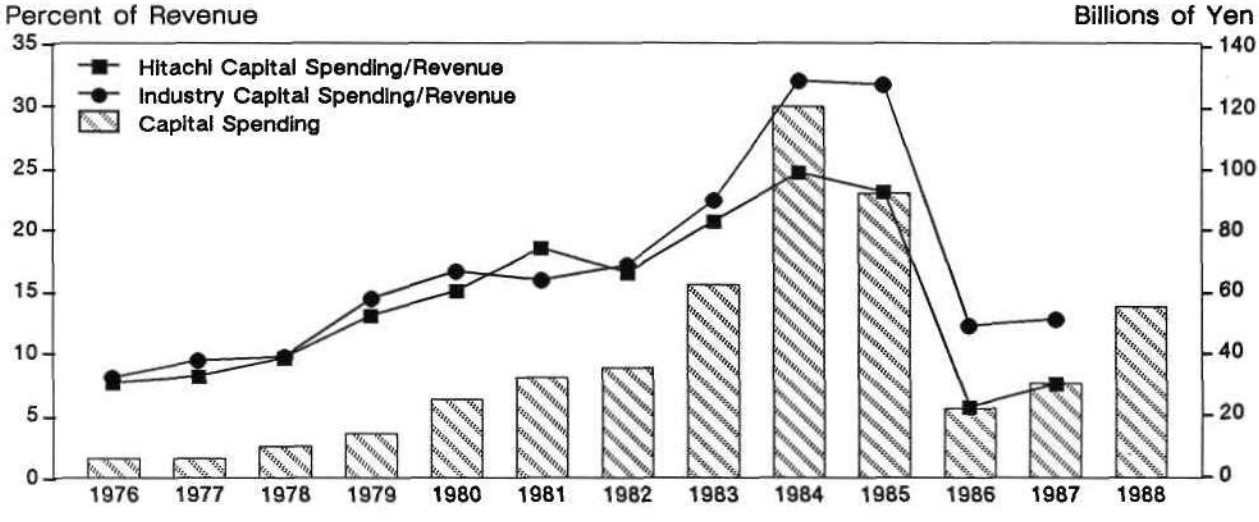
Hitachi

Hitachi's capital spending–to–revenue ratio has generally been below the Japanese industry's average. Generally, its movements have paralleled those of the industry average (see Figure 16). Dataquest expects that Hitachi will increase its capital spending by 83 percent in 1988, from ¥30 billion in 1987 to ¥55 billion in 1988.

Hitachi's major investment in 1988 is the construction of its new fab in Irving, Texas. When completed, this new fab will cost 10.4 to ¥12.5 billion and will be a class 10 facility with 40,000 square feet of clean room. Hitachi hopes to begin pilot production of 1.3–micron 256K SRAMs by the fall of 1989. In January of this year, Hitachi began a new 150mm memory line at the Naka Works facility.

Figure 16

Hitachi versus Industry Average
Capital Spending/Revenue



Source: Dataquest
August 1988

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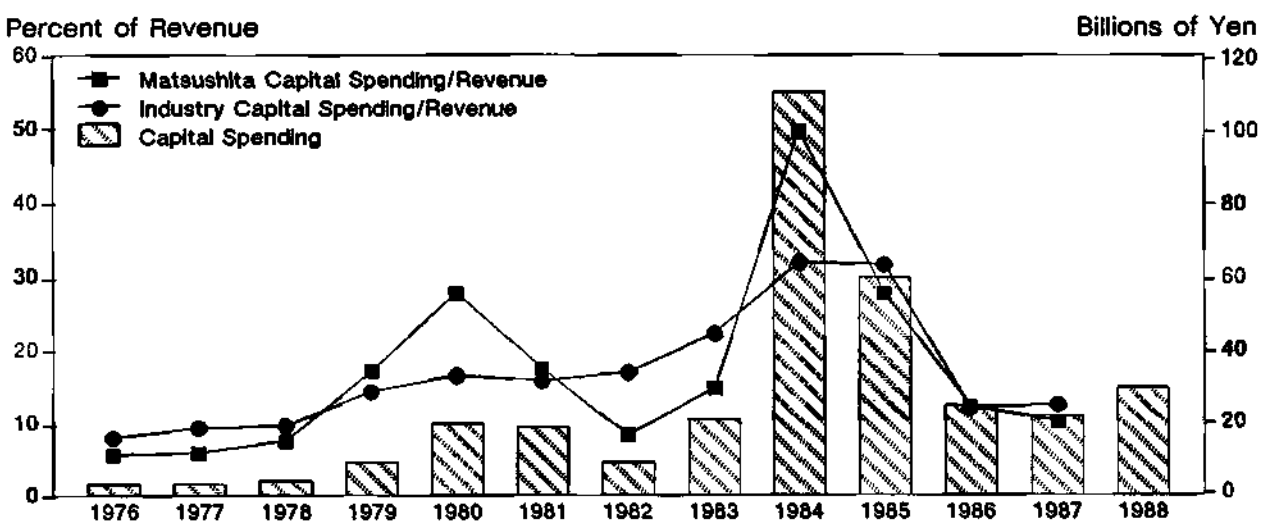
Capital Spending by Company

Matsushita Electric

Matsushita's capital spending–to–revenue ratio substantially exceeded the Japanese industry's average in 1984. Since 1984, however, its capital spending–to–revenue ratio has been quite close to the industry average (see Figure 17). Dataquest expects that Matsushita will increase its capital spending by 67 percent in 1988, from ¥22 billion in 1987 to ¥30 billion in 1988. The main focus of its expenditures will be the construction of a memory line at its Uozu fab.

Figure 17

Matsushita versus Industry Average Capital Spending/Revenue



Source: Dataquest August 1988

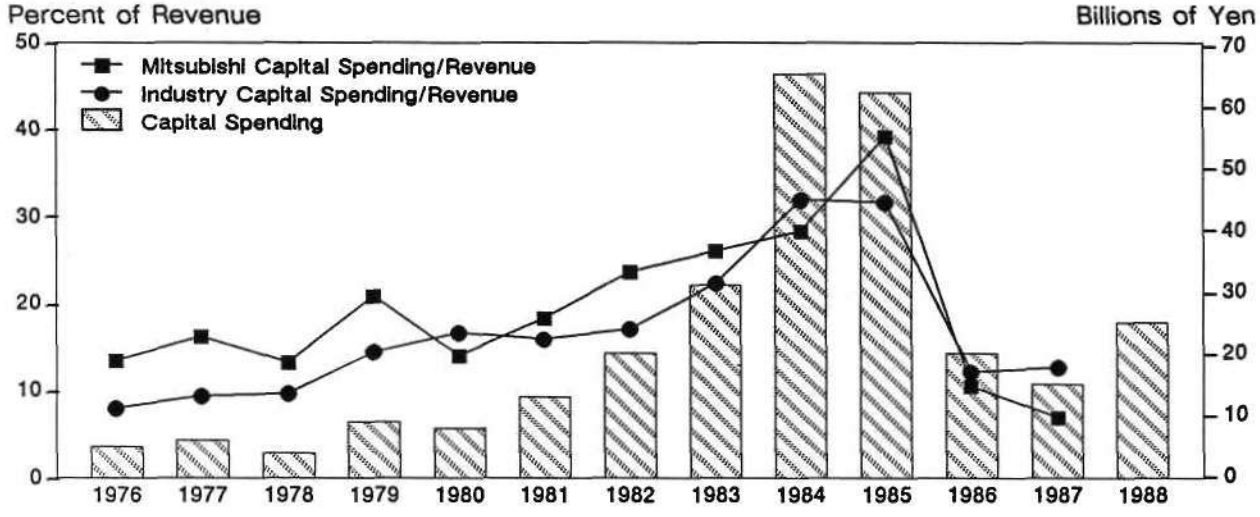
Capital Spending by Company

Mitsubishi Electric

Mitsubishi's capital spending-to-revenue ratio peaked in 1985. Since then, it has continued to decline (see Figure 18). Dataquest expects, however, that Mitsubishi will increase its capital spending by 67 percent in 1988, from ¥15 billion in 1987 to ¥25 billion in 1988. The main focus of Mitsubishi's expenditures will be to increase microprocessor capacity at its Kochi fab.

Figure 18

Mitsubishi versus Industry Average Capital Spending/Revenue



Source: Dataquest
August 1988

Capital Spending by Company

NEC

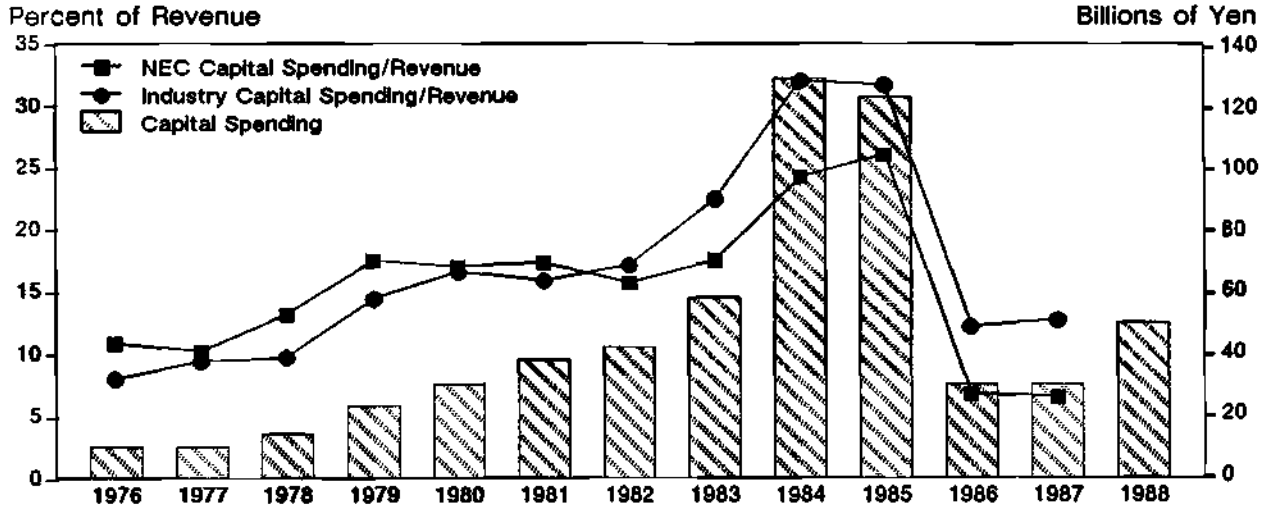
NEC's capital spending-to-revenue ratio has generally been lower than the average for the Japanese industry, and has tended to move in parallel with the industry's average (see Figure 19). Dataquest expects that NEC will increase its capital spending by 67 percent in 1988, from ¥30 billion to ¥50 billion.

In June of this year, NEC completed a 150mm, 15,000-wafer-start capacity line at NEC Kyushu. Devices produced on this new line include 16- and 32-bit microprocessors, and high-density ASICs. Also in June, NEC started production of 1Mb DRAMs at its Yamaguchi facility. This new line has a capacity of 20,000 150mm wafers per month.

NEC also plans to invest an additional ¥4 billion at its Kansai facility; ¥2.5 billion at its Yamagata facility; ¥3 billion at its facility in Scotland; and ¥2 billion to expand capacity at its Roseville, California, fab.

Figure 19

NEC versus Industry Average Capital Spending/Revenue



Source: Dataquest August 1988

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Capital Spending by Company

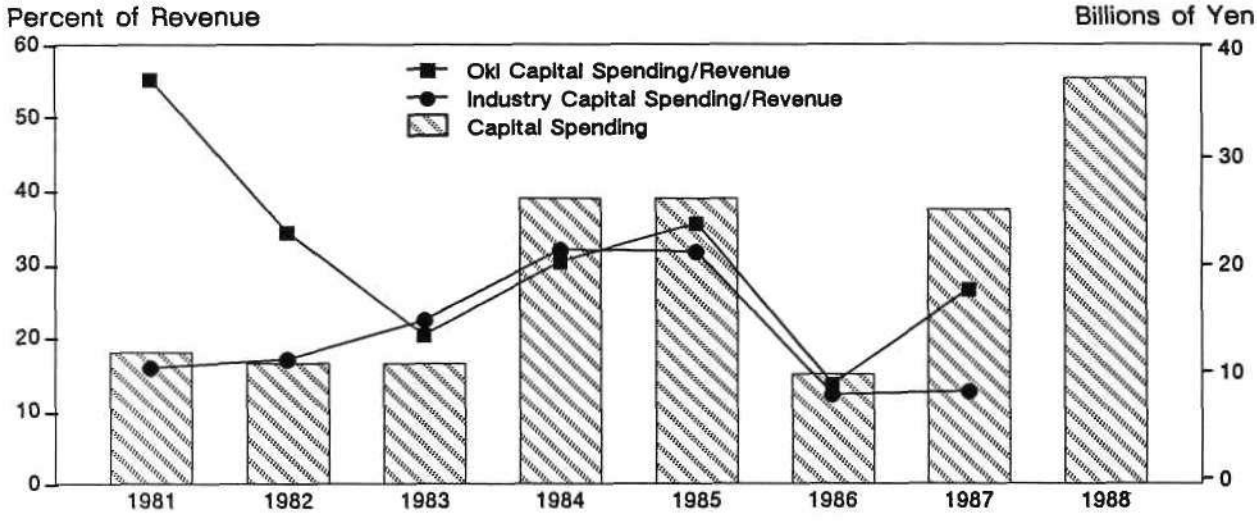
Oki Electric

Until 1987, Oki's capital spending-to-revenue ratio generally equaled the industry's average for Japan. In 1987, Oki's capital spending levels approached its 1984 and 1985 levels. Dataquest expects that Oki will exceed its 1984 level in 1988 (see Figure 20).

Dataquest expects Oki to increase its capital spending in 1988 by 48 percent, from ¥25 billion in 1987 to ¥37 billion in 1988. The main focus of this spending will be for its new facility at Miyagi, which it hopes will begin operations in the early part of 1989. Oki is also in the process of upgrading its lines at its Miyazake facility. Dataquest does not expect Oki to build a fab in the United States until at least 1990.

Figure 20

Oki Electric versus Industry Average Capital Spending/Revenue



Source: Dataquest
August 1988

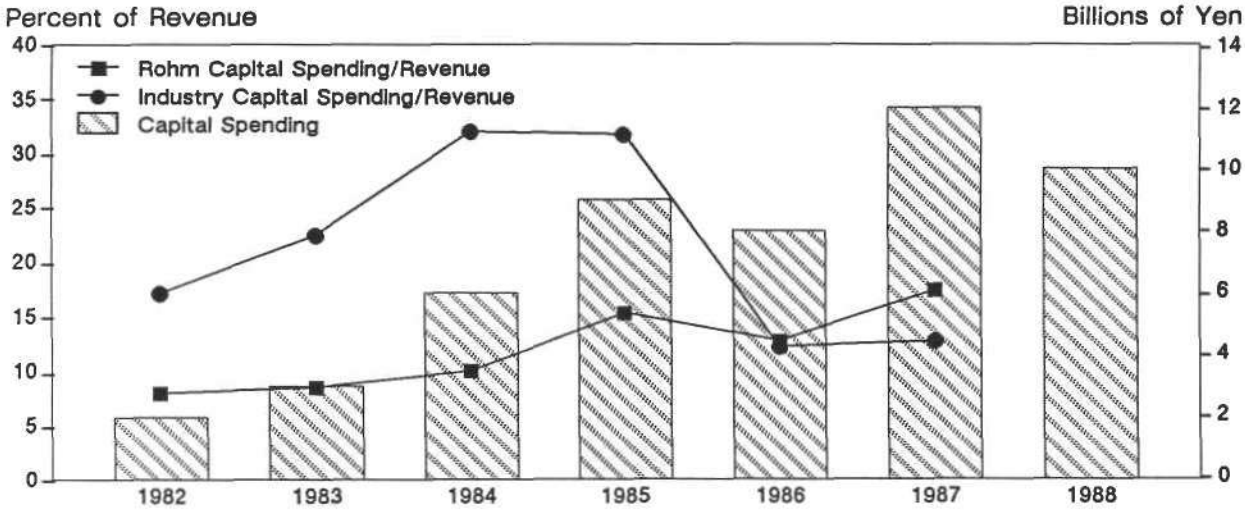
Capital Spending by Company

Rohm

Rohm's capital spending–to–revenue ratio exceeded the industry's average in 1986. Since then, Rohm's capital spending–to–revenue ratio has grown, as, generally, has Rohm's absolute level of spending (see Figure 21). Dataquest expects, however, that Rohm's level of spending will fall off slightly (17 percent) in 1988 to ¥10 billion from ¥12 billion in 1987.

Figure 21

Rohm versus Industry Average Capital Spending/Revenue



Source: Dataquest August 1988

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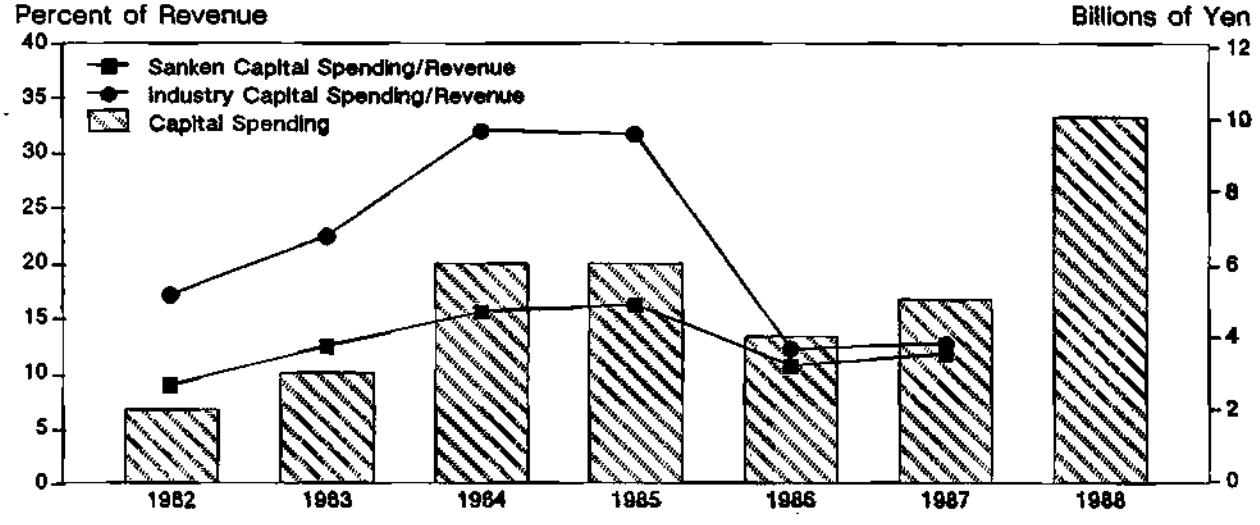
Capital Spending by Company

Sanken Electric

Sanken Electric's capital spending was substantially below the Japanese industry average until 1986 (see Figure 22). In 1986 and 1987, Sanken's ratio of capital spending to revenue was quite close to the industry's average. Dataquest expects that Sanken Electric will double its capital spending in 1988, from ¥5 billion in 1987 to ¥10 billion in 1988.

Figure 22

Sanken Electric versus Industry Average
Capital Spending/Revenue



Source: Dataquest
August 1988

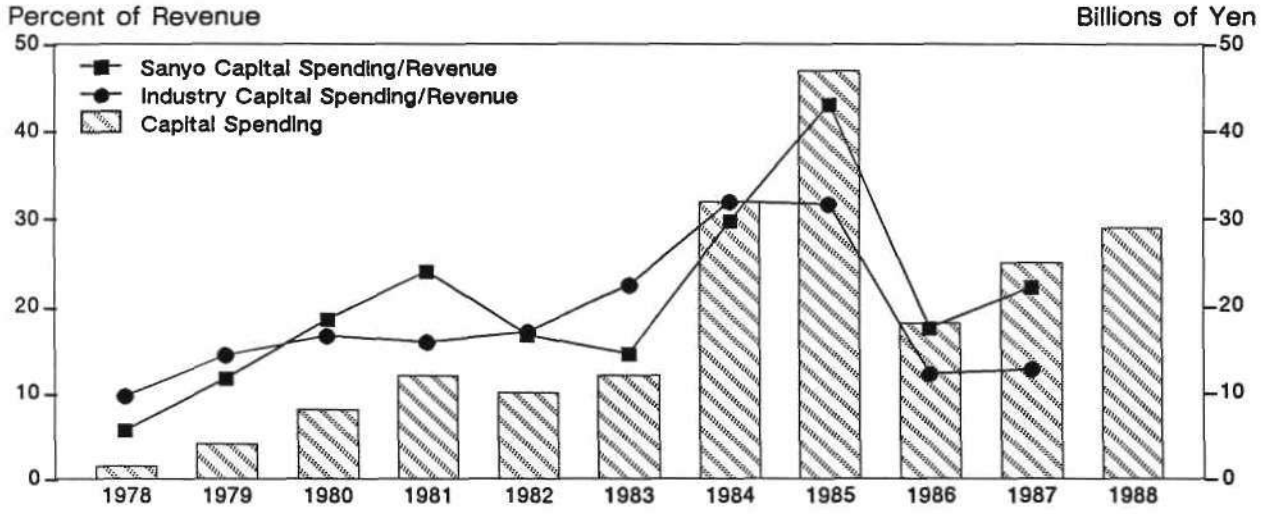
Capital Spending by Company

Sanyo Electric

Sanyo Electric's capital spending–to–revenue ratio has exceeded the Japanese industry's average since 1986 (see Figure 23). Dataquest expects that Sanyo will increase its spending this year to ¥29 billion, up 16 percent from 1987. The goal of Sanyo's spending will be to increase its ASIC capacity by investing ¥10 billion at its Niigata facility to construct a third clean room.

Figure 23

Sanyo Electric versus Industry Average Capital Spending/Revenue



Source: Dataquest
August 1988

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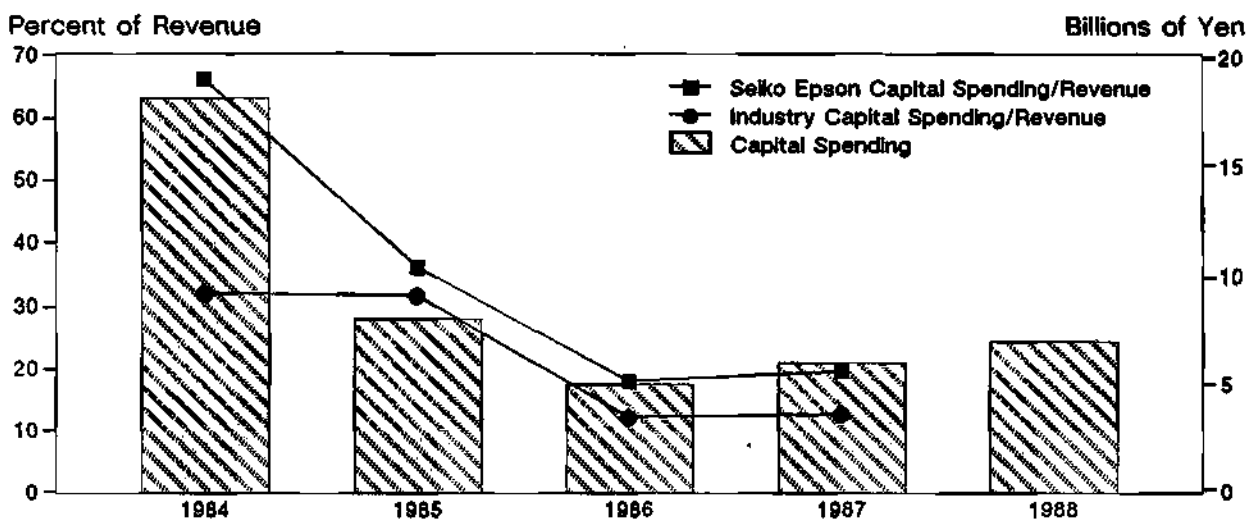
Capital Spending by Company

Seiko Epson

Seiko Epson's capital spending-to-revenue ratio has been above the industry's average since 1984 (see Figure 24). Dataquest expects that Seiko Epson will increase its capital spending by 17 percent in 1988, from ¥6 billion in 1987 to ¥7 billion in 1988.

Figure 24

Seiko Epson versus Industry Average
Capital Spending/Revenue



Source: Dataquest
August 1988

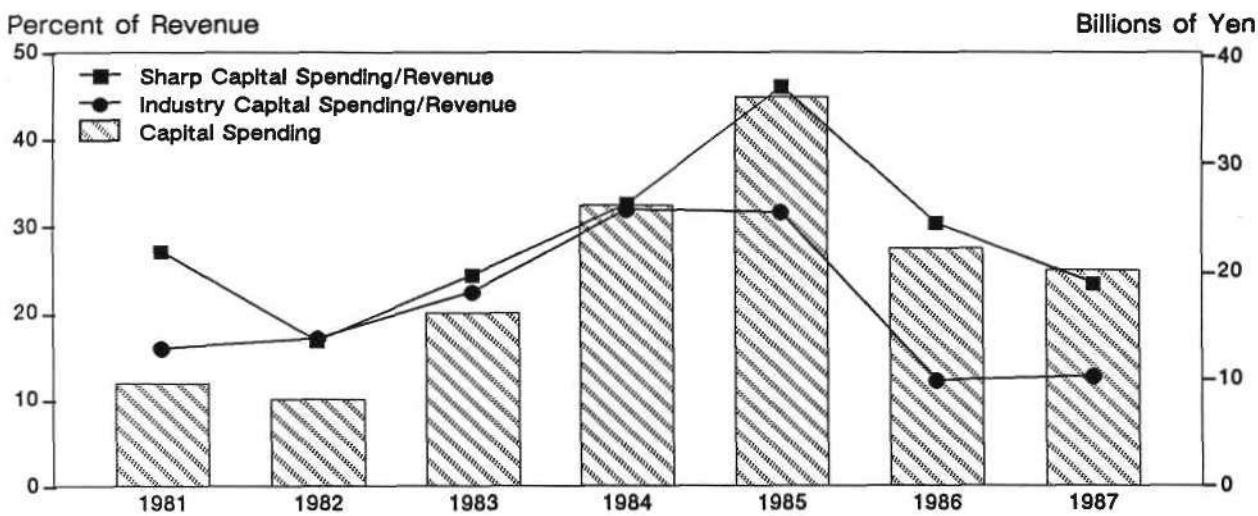
Capital Spending by Company

Sharp

Sharp's capital spending–to–revenue ratio has exceeded the Japanese industry's average since 1982. Since 1985, it has exceeded the industry's average substantially (see Figure 25). Dataquest believes that Sharp will increase its capital spending by 30 percent, from ¥20 billion in 1987 to ¥26 billion in 1988. The main focus of this spending will be the construction of its second fab at Fukuyama, which is scheduled to begin production of 1Mb and 4Mb DRAMs in the summer of 1989.

Figure 25

Sharp versus Industry Average
Capital Spending/Revenue



Source: Dataquest
August 1988

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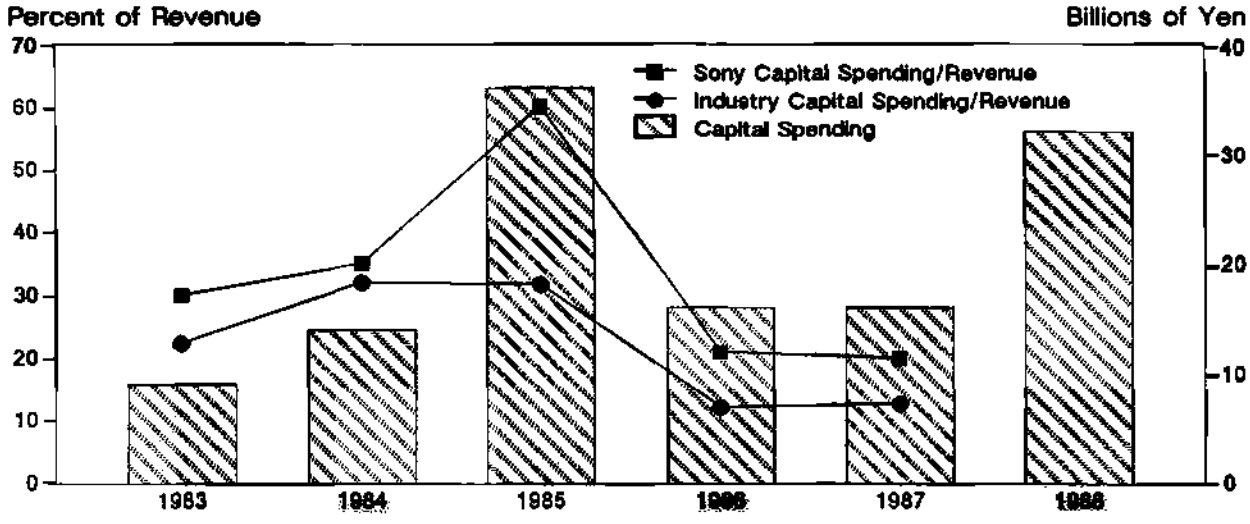
Capital Spending by Company

Sony

Sony's capital spending–to–revenue ratio has exceeded the Japanese industry's average since 1983 (see Figure 26). Dataquest expects Sony to increase its capital spending by 100 percent, from ¥16 billion in 1987 to ¥32 billion in 1988. The focus of this spending is to remodel its Nagasaki fab (which it acquired from Fairchild), increase capacity at its Kokubu facility for analog ICs, and for CCD production at its Atsugi fab.

Figure 26

Sony versus Industry Average
Capital Spending/Revenue



Source: Dataquest
August 1988

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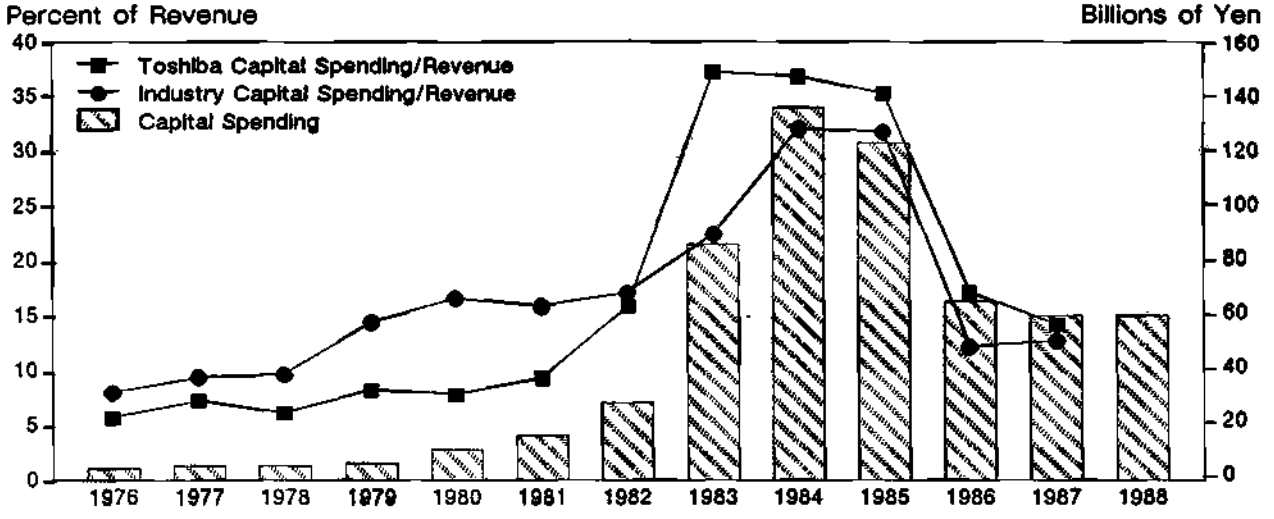
Capital Spending by Company

Toshiba

Toshiba's capital spending-to-revenue ratio has moved in tandem with the Japanese industry's average, and has exceeded the average since 1983 (see Figure 27). Toshiba's capital spending is the largest of any of the Japanese companies. Dataquest expects that Toshiba will spend ¥60 billion in 1988, approximately the same amount as 1987. In addition to equipment upgrades, Toshiba will add a new 150mm line at its Oita facility, which began operation in October of 1987. Toshiba also plans to add a logic line at its Iwate facility and a BICMOS line at its Kita-Kyushu facility.

Figure 27

Toshiba versus Industry Average
Capital Spending/Revenue



Source: Dataquest
August 1988

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Capital Spending by Company

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Capital Spending by Company: Japan

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Capital Spending by Company: Japan

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Capital Spending by Company: Japan

INTRODUCTION

This service section will report the results of Dataquest's latest survey of capital spending plans by Japanese semiconductor companies. Knowledge of capital spending plans is useful to semiconductor manufacturers because it is an essential element of any competitive or capacity analysis. Knowledge of semiconductor manufacturers' current spending plans can help semiconductor equipment manufacturers identify sales leads and direct existing resources to the best markets.

JAPANESE COMPANY CAPITAL SPENDING

Dataquest surveys the major Japanese semiconductor manufacturers several times a year to track their capital spending plans. Table 1 provides a summary of the history of capital spending by Japanese semiconductor manufacturers in yen and the percent change in their spending from 1988 to 1989. Most of the analysis in this service section is given in yen. This is because statements of change in current dollars overstate the growth of Japanese capital spending because of Japanese currency appreciation. Table 2 provides Japanese capital spending data in U.S. dollars.

Continuing the trend that began in 1987, most Japanese companies are planning to increase their capital spending, although at a slower rate than in 1988. Toshiba will spend more than any other company in the world except Samsung and Goldstar, each of which will spend approximately as much as Toshiba. In 1989, Toshiba plans to spend ¥80 billion ($615 million); Hitachi and NEC each plan to spend ¥70 billion ($538 million); and Fujitsu and Matsushita each plan to spend ¥60 billion ($462 million). These five companies account for 34 percent ($1.8 billion) of total Japanese capital spending of $5.4 billion. Individual company capital spending/revenue ratios for 1976 through 1988 are given in Table 3.

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Table 1

Japanese Company Capital Spending
(Billions of Yen)

Company	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	Percent Change 1988-1989
Fuji Electric	N/M	N/M	N/M	N/M	¥ 4	¥ 6	¥ 12	¥ 12	¥ 5	¥ 3	¥ 5	¥ 7	40%
Fujitsu	¥10	¥14	¥ 25	¥ 32	35	53	115	72	16	20	60	60	0
Hitachi	9	13	21	33	36	62	120	92	22	30	65	70	8%
Matsushita	4	9	20	19	9	21	110	60	25	22	50	60	20%
Mitsubishi	4	9	8	13	20	31	65	62	20	15	40	50	25%
NEC	14	23	30	38	42	58	129	123	30	30	55	70	27%
Nihon Semiconductor	0	0	0	0	0	0	0	0	5	15	3	5	67%
New Japan Radio Corp.	N/M	N/M	N/M	N/M	2	2	4	5	5	2	5	7	40%
NMB	N/M	N/M	N/M	N/M	N/M	N/M	14	14	5	10	10	40	300%
OKI	2	3	12	12	11	11	26	26	10	25	37	40	8%
Rohm	N/M	N/M	N/M	N/M	2	3	6	9	8	12	10	15	50%
Sanken Electric	N/M	N/M	N/M	N/M	2	3	6	6	4	5	10	12	20%
Sanyo	1	4	8	12	10	12	32	47	18	25	29	35	21%
Sharp	2	8	9	10	8	16	26	36	22	20	35	45	29%
Shindengen	N/M	N/M	N/M	N/M	1	1	3	3	1	1	2	3	50%
Seiko Epson	N/M	N/M	N/M	N/M	5	9	18	8	5	6	7	7	0
Sony	N/M	N/M	N/M	N/M	5	9	14	36	16	16	35	45	29%
Toshiba	5	8	11	16	28	86	136	123	65	60	80	80	0
Others	0	0	0	0	9	16	34	32	13	20	45	55	22%
Total	¥51	¥91	¥144	¥185	¥229	¥399	¥870	¥766	¥295	¥337	¥503	¥706	21%
Percent Change	21%	79%	58%	29%	24%	74%	118%	(12%)	(61%)	14%	73%	21%	

N/M = Not Meaningful

Source: Dataquest
August 1989

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Capital Spending by Company: Japan

Table 2

Japanese Company Capital Spending
(Millions of Dollars)

Company	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	Percent Change 1988-1989
Fuji Electric	0	0	0	0	$ 16	$ 26	$ 51	$ 50	$ 30	$ 21	$ 38	$ 54	40%
Fujitsu	$ 49	$ 63	$111	$145	141	226	485	303	96	139	462	462	0
Hitachi	44	59	93	149	145	264	506	387	132	208	500	538	8%
Matsushita	19	41	89	86	36	89	464	252	150	152	385	462	20%
Mitsubishi	19	41	36	59	80	132	274	261	120	104	308	385	25%
NEC	68	104	133	172	169	247	544	517	180	208	423	538	27%
New Japan Radio Corp.	0	0	0	0	8	9	17	21	30	17	38	54	40%
NMB	0	0	0	0	0	0	59	59	30	69	77	308	300%
OKI	10	14	53	54	44	47	110	109	60	174	285	308	8%
Rohm	0	0	0	0	8	13	25	38	45	83	77	115	50%
Sanken Electric	0	0	0	0	8	13	25	25	24	35	77	92	20%
Sanyo	7	18	36	54	40	51	135	197	108	174	223	269	21%
Sharp	7	36	38	43	32	68	110	151	132	139	269	346	29%
Shinmengen	0	0	0	0	4	-4	13	13	6	7	15	23	50%
Seiko Epson	0	0	0	0	20	38	76	34	30	42	54	54	0
Sony	0	0	0	0	20	38	59	151	96	111	269	346	29%
Toshiba	24	36	49	72	113	366	574	517	389	417	615	615	0
Others	0	0	0	0	36	68	143	134	78	139	346	423	22%
Total	$247	$411	$638	$834	$921	$1,698	$3,671	$3,219	$1,766	$2,345	$4,485	$5,431	21%
Percent Change	57%	66%	55%	31%	10%	84%	116%	(12%)	(45%)	33%	91%	21%	
Exchange Rate (Yen per US$1)	206	221	225	221	249	235	237	238	167	144	130	130	

N/M = Not Meaningful

Source: Dataquest
August 1989

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Capital Spending by Company: Japan

Table 3

Japanese Company Capital Spending as a Percentage of Revenue

Company	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988
Fuji Electric	N/M	N/M	N/M	N/M	16%	21%	29%	32%	15%	8%	14%
Fujitsu	39%	31%	40%	39%	30%	34%	41%	30%	7%	8%	20%
Hitachi	10%	13%	15%	18%	16%	21%	25%	23%	6%	8%	14%
Matsushita	8%	17%	28%	18%	8%	15%	50%	28%	13%	10%	20%
Mitsubishi	13%	21%	14%	18%	24%	26%	28%	39%	11%	7%	14%
NEC	13%	17%	17%	17%	16%	17%	24%	26%	7%	6%	9%
New Japan Radio Corp.	N/M	N/M	N/M	N/M	N/M	N/M	N/M	N/M	33%	11%	21%
OKI	N/M	N/M	N/M	55%	34%	20%	30%	36%	14%	27%	30%
Rohm	N/M	N/M	N/M	N/M	8%	8%	10%	15%	12%	16%	12%
Sanken Electric	N/M	N/M	N/M	N/M	9%	12%	16%	16%	11%	12%	20%
Sanyo	6%	12%	19%	24%	17%	15%	30%	43%	18%	20%	21%
Sharp	N/M	N/M	N/M	27%	17%	24%	33%	46%	30%	24%	26%
Seiko Epson	N/M	N/M	N/M	N/M	N/M	N/M	66%	36%	18%	17%	17%
Sony	N/M	N/M	N/M	N/M	N/M	30%	35%	60%	21%	19%	29%
Toshiba	6%	8%	8%	9%	16%	37%	37%	35%	17%	14%	14%
Japanese Industry Average	10%	14%	17%	16%	17%	22%	32%	32%	12%	13%	18%

N/M = Not Meaningful

Source: Dataquest
August 1989

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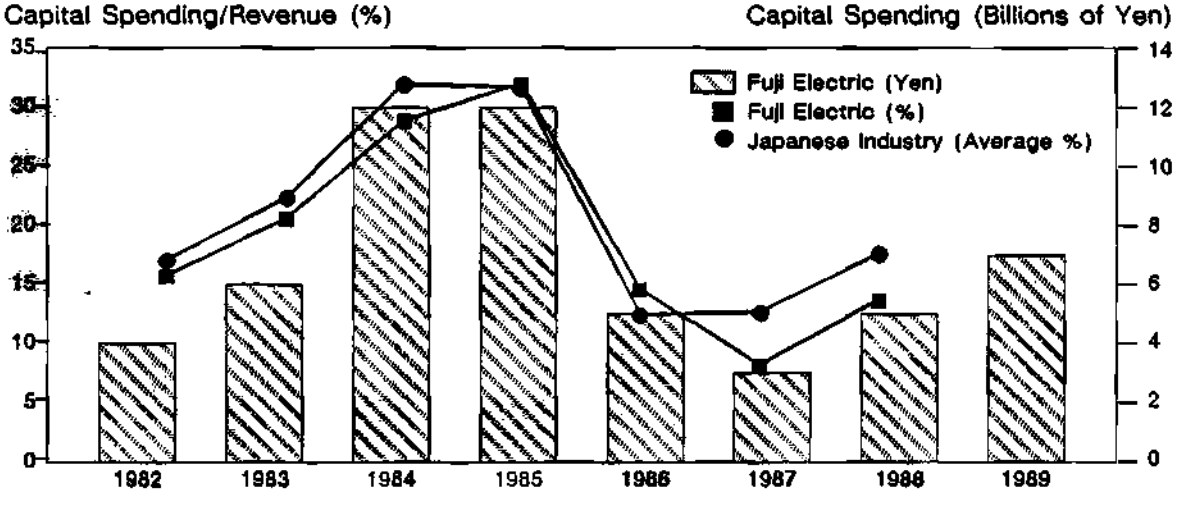
Capital Spending by Company: Japan

Fuji Electric

Fuji Electric's ratio of capital spending was below the Japanese company average in both 1987 and 1988 (see Figure 1). Fuji plans to increase its spending from 5 billion yen in 1988 to 7 billion yen in 1989 (from $38 million to $54 million). This is an increase of 40 percent over 1987.

Figure 1

Fuji
Capital Spending/Revenue versus Industry Average and Total Capital Spending



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Source: Dataquest August 1989

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Capital Spending by Company: Japan

Fujitsu

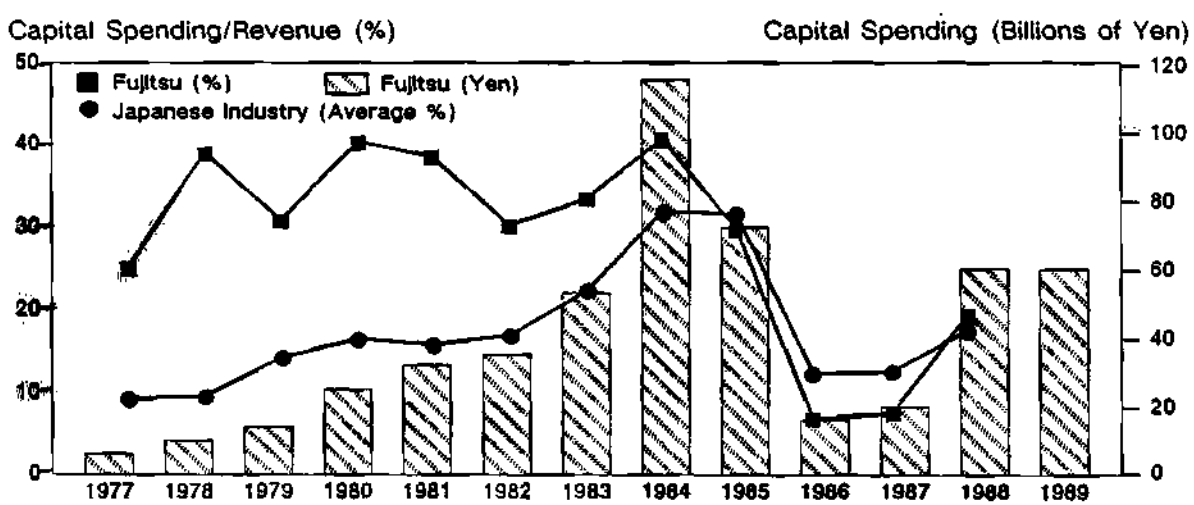
In 1986, Fujitsu's ratio of capital spending to revenue was 7 percent compared with the Japanese company average of 12 percent (see Figure 2). In 1987, Fujitsu's ratio was 8 percent; the Japanese industry's average was 13 percent. In 1988, however, Fujitsu's ratio of capital spending to revenue was 20 percent; the Japanese industry's average was 18 percent.

Fujitsu plans to keep its capital spending on par with its 1988 spending of ¥60 billion ($462 million). Fujitsu is committed to an ambitious expansion program. This year, it completed two new fabs in Gresham, Oregon, in the United States. One of these fabs is an ASIC facility, capable of running 28,000 1.5-micron 125mm wafers per month. The other fab in Gresham is a 150mm line capable of running 15,000 1.2-micron 1Mb DRAMs per month. Fujitsu plans to begin pilot production on this line in the summer of 1989.

Fujitsu announced plans for a 1Mb and a 4Mb DRAM and also an ASIC facility in Newton Aycliffe in the United Kingdom. The Company also announced that it plans to build a 4Mb DRAM production line at its Mie, Japan, plant. Dataquest believes that Fujitsu also may soon have a 200mm 4Mb DRAM facility in Izawa-gun, Iwate, in Japan.

Figure 2

Fujitsu
Capital Spending/Revenue versus Industry Average and Total Capital Spending



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Source: Dataquest August 1989

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Capital Spending by Company: Japan

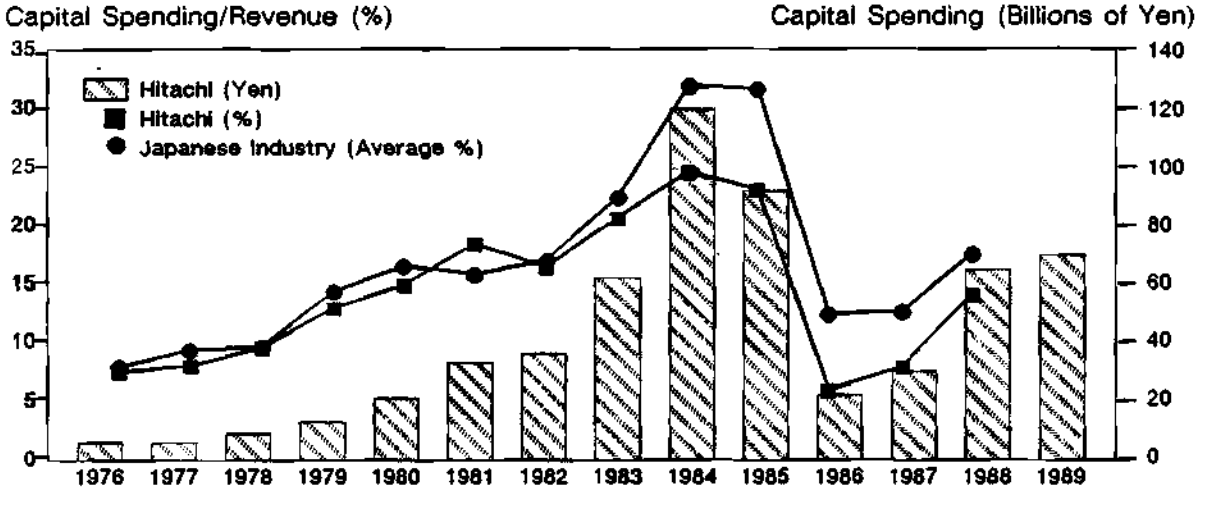
Hitachi

Hitachi's capital spending/revenue ratio has been less than the industry's average since the early 1980s (see Figure 3). We expect Hitachi to increase its capital spending by 8 percent in 1989, from ¥65 billion in 1988 to ¥70 billion in 1989 (from $500 million to $538 million).

Hitachi also is involved in an ambitious expansion program. Hitachi's new 150mm SRAM facility in Irving, Texas, in the United States began production in May of 1989. Dataquest believes that Hitachi may also begin running 200mm wafers for 4Mb DRAMs at its Kodaira-shi, Tokyo, facility in 1990; Hitachi reportedly will open another 4Mb-DRAM facility at Kanakoma-gun, Yamanashi, in Japan, also in 1990, but one that will produce 150mm wafers.

Figure 3

Hitachi
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-3

Source: Dataquest August 1989

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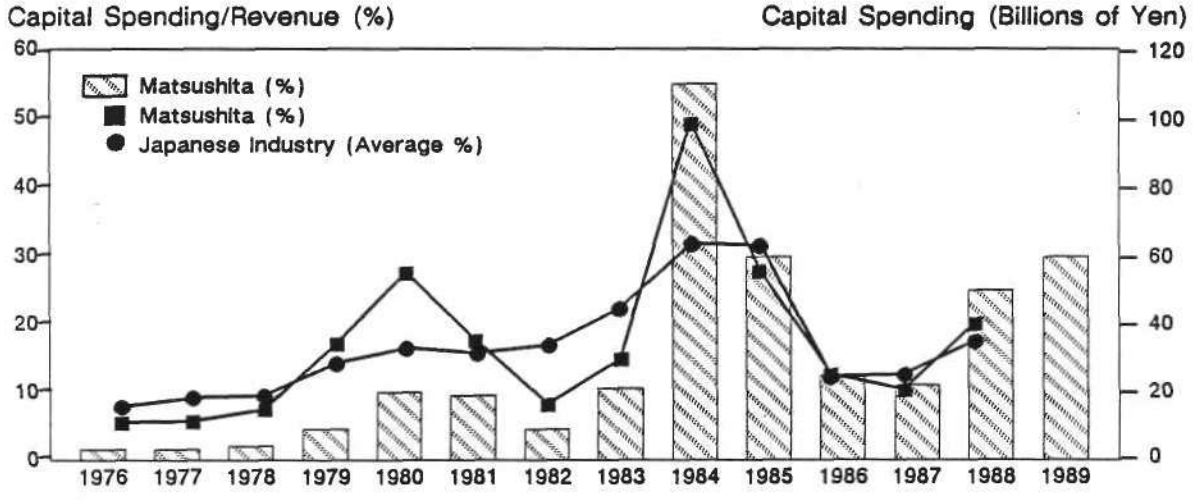
Capital Spending by Company: Japan

Matsushita

Matsushita's ratio of capital spending to revenue has been very close to the Japanese industry's average since 1985 (see Figure 4). In 1988, Matsushita spent ¥50 billion ($385 million) on capital spending. We expect Matsushita's capital spending to increase by approximately 20 percent this year, to ¥60 billion ($462 million). The company plans to install a 4Mb DRAM line at its Uozu, Japan, facility. Matsushita also plans to expand its prototype line at its Semiconductor Research Center in Kadoma-shi, Japan.

Figure 4

Matsushita
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-4

Source: Dataquest August 1989

Capital Spending by Company: Japan

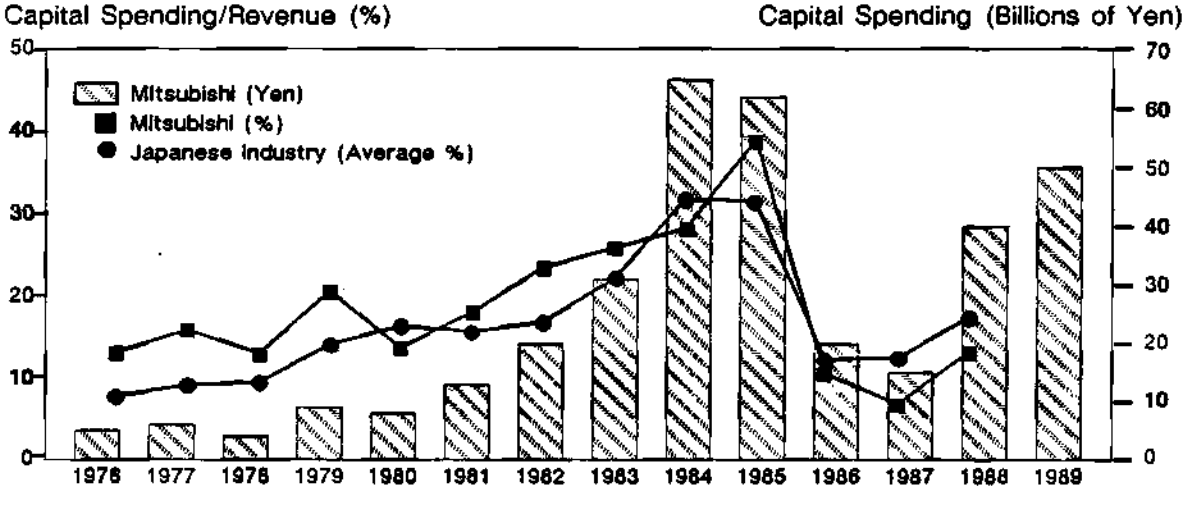
Mitsubishi

In 1987, Mitsubishi's ratio of capital spending to revenue was 7 percent, while the average for the Japanese industry was 13 percent (see Figure 5). In 1988, Mitsubishi increased its capital spending from ¥15 billion in 1987 to ¥40 billion in 1988. Its ratio of capital spending to revenue rose to 14 percent; the Japanese industry's average in 1988 was 18 percent. Dataquest expects Mitsubishi's capital spending to increase 25 percent in 1989, from ¥40 billion ($308 million) in 1988 to ¥50 billion ($385 million) in 1989.

Mitsubishi had planned to began ASIC production at its Durham, North Carolina, facility in the United States in the early part of 1989. The Company, however, recently announced that it will start producing 1Mb DRAMs at this facility instead of ASICs. Mitsubishi also is building a 4Mb DRAM prototype line at its Saijo, Japan, facility. This prototype line is expected to be operational in 1990.

Figure 5

Mitsubishi
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-5

Source: Dataquest August 1989

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Capital Spending by Company: Japan

NEC

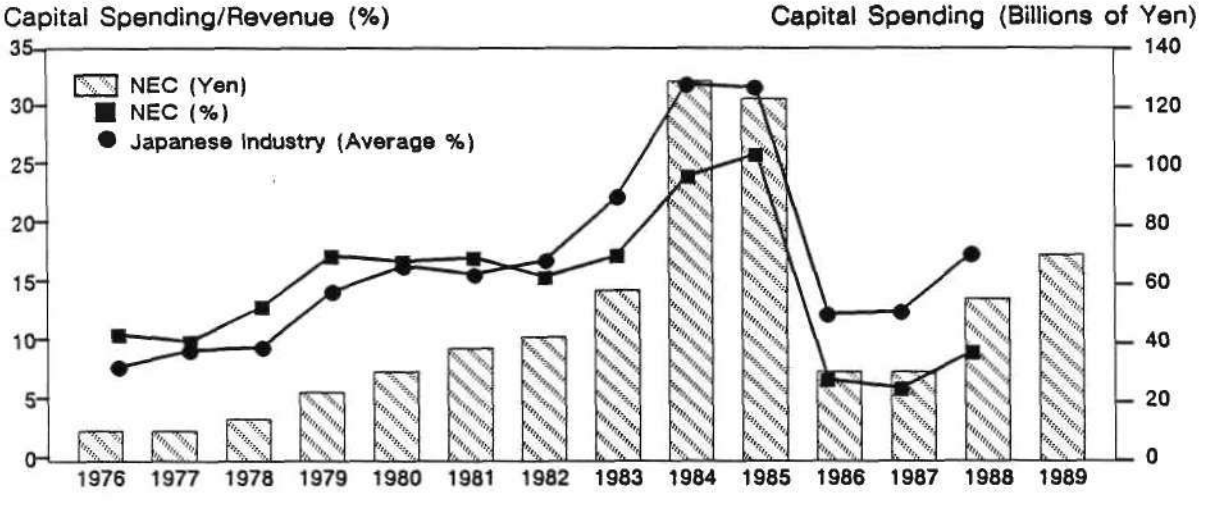
NEC's capital spending/revenue ratio has been significantly below the Japanese industry's average since 1983 (see Figure 6). In 1987, NEC's capital spending–to–revenue ratio was just 6 percent, with the Japanese industry average at 13 percent. In 1988, NEC's capital spending–to–revenue ratio was approximately one–half the Japanese industry's average (9 percent versus 18 percent).

NEC's capital spending totaled ¥55 billion ($423 million) in 1988; by the end of 1989, NEC's capital spending is expected to increase by 27 percent to ¥70 billion ($538 million).

NEC reportedly plans to complete its 16Mb prototype DRAM line at its Sagamahara, Japan, facility and begin production there by the end of this year. These prototypes may be run on 200mm wafers. NEC also expects to complete its 4Mb DRAM facility in Yamaguchi, Japan, this year. The Company reportedly plans to follow up its DRAM fab in Yamaguchi with one in Hiroshima, Japan, in 1990.

Figure 6

NEC
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587–6

Source: Dataquest August 1989

Capital Spending by Company: Japan

NMB Semiconductor

NMB plans to increase its capital spending substantially this year; from ¥10 billion to ¥40 billion (from $77 million to $308 million). This represents an increase of more than 300 percent. Most of this increase will be for the construction of a 4Mb DRAM fab, which the Company plans to have completed by March 1990.

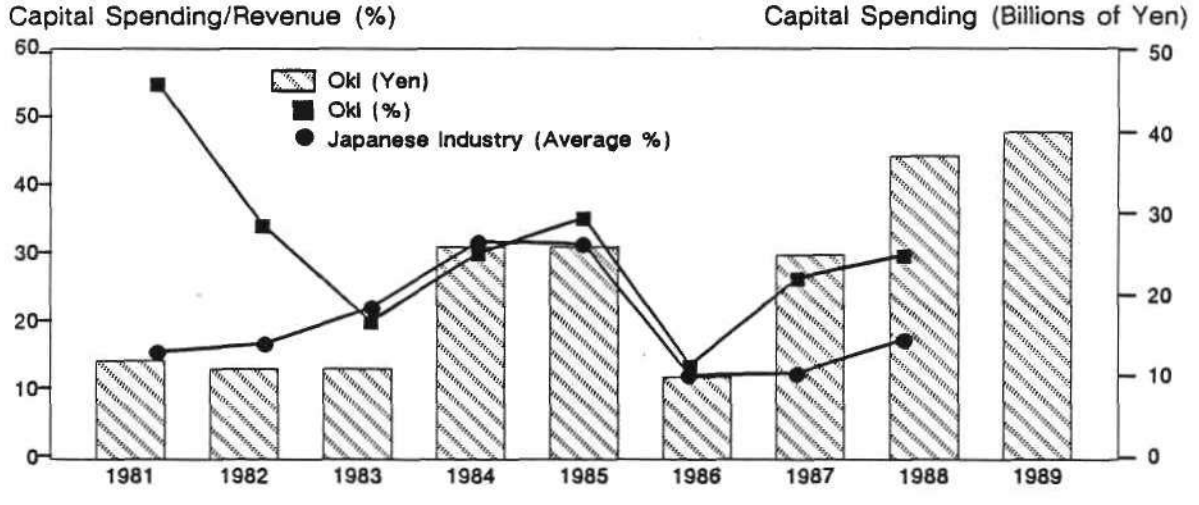
Oki

Oki's ratio of capital spending to revenue was substantially above the Japanese industry average in both 1987 and 1988 (see Figure 7). In 1988, Oki's ratio exceeded 30 percent, more than any other Japanese semiconductor company. However, Oki plans to increase its spending by only 8 percent in 1989, from ¥37 billion to ¥40 billion (from $285 million to $308 million).

A major part of Oki's recent investments was for its 4Mb DRAM plant at Miyagi, Japan. Oki plans to begin production at this plant in the second half of 1989.

Figure 7

Oki
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-7

Source: Dataquest August 1989

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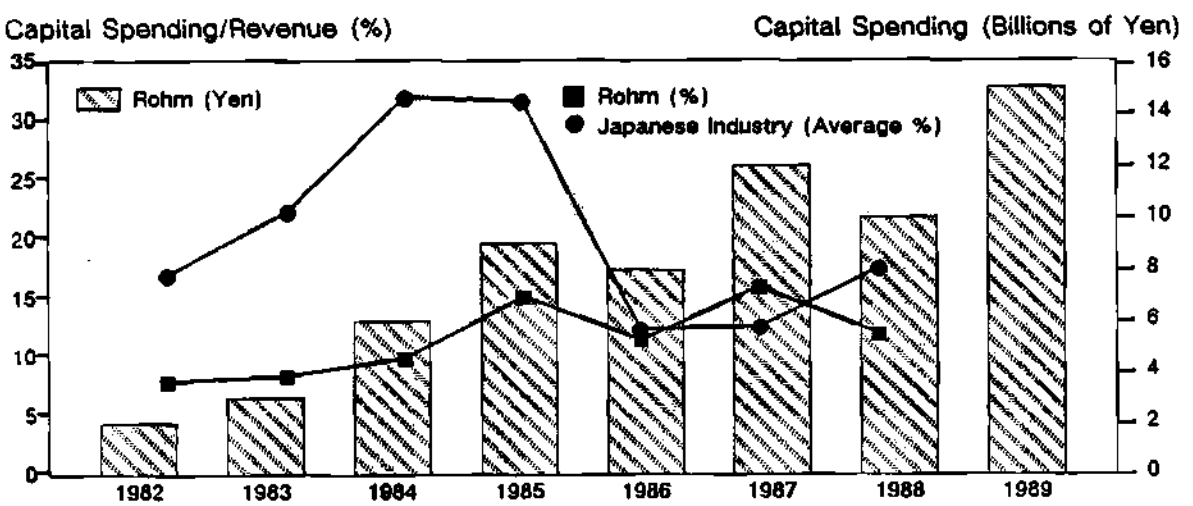
Capital Spending by Company: Japan

Rohm

In 1987, Rohm's ratio of capital spending to revenue was 16 percent and the Japanese industry's average was 13 percent (see Figure 8). However, in 1988, Rohm's level of capital spending fell 17 percent, causing its ratio to fall below the industry's average. Dataquest expects Rohm to increase its capital spending by 50 percent in 1989, from ¥10 billion ($77 million) to ¥15 billion ($115 million).

Figure 8

Rohm
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-8

Source: Dataquest August 1989

Capital Spending by Company: Japan

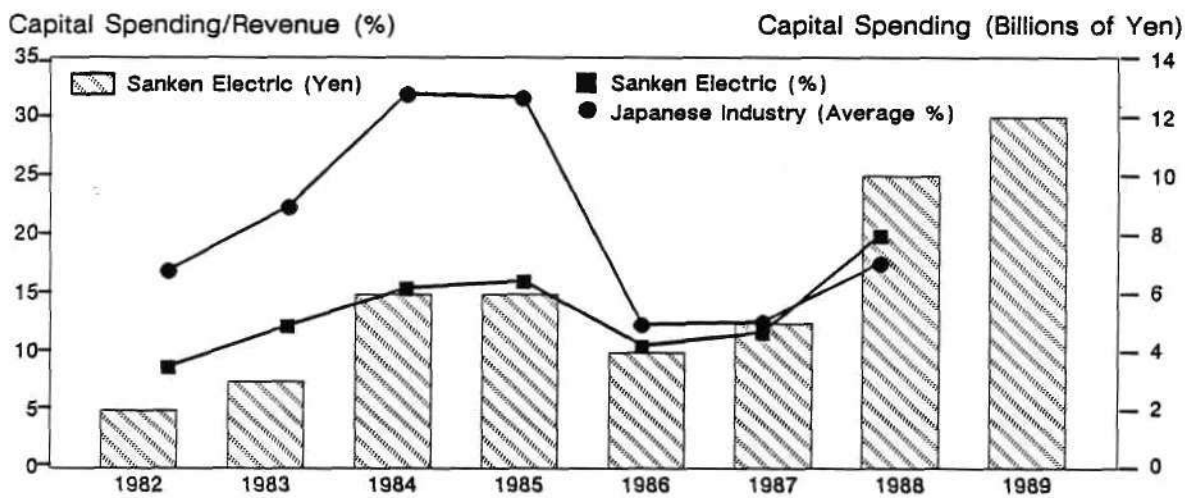
Sanken Electric

Sanken's ratio of capital spending to revenue was close to the Japanese industry average in 1986, 1987, and 1988. Before 1986, however, its ratio was significantly below the industry's average (see Figure 9).

In 1988, Sanken completed its new fab at Yamagata, Japan. The Company's current plans include building two new assembly plants, one at Ishikawa, Japan, and another at Kashima, Japan. Sanken's capital spending will increase 20 percent in 1989, from ¥10 billion ($77 million) in 1988 to ¥12 billion yen in 1989 ($92 million) in 1989.

Figure 9

Sanken Electric
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-9

Source: Dataquest August 1989

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Capital Spending by Company: Japan

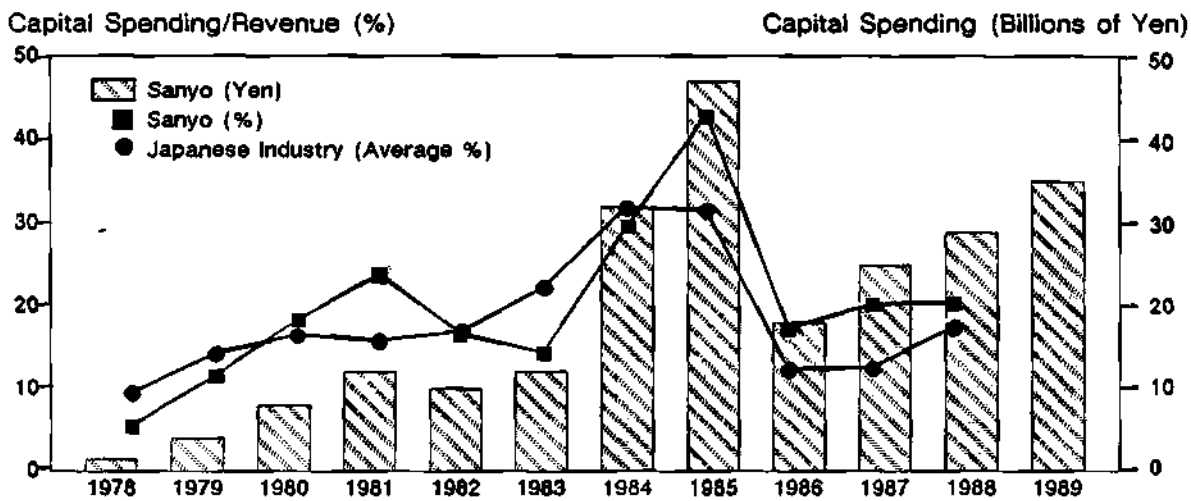
Sanyo

Sanyo's capital spending/revenue ratio has been significantly above the industry's average since 1985 (see Figure 10). Sanyo's capital spending will reach ¥35 billion ($269 million) in 1989, an increase of 21 percent over its 1988 level.

Sanyo started 1Mb production this year at its new plant at Niigata, Japan. Currently, the company is building an ultralarge-scale integrated (ULSI) laboratory for research on 16Mb and 64Mb DRAMs.

Figure 10

Sanyo
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-10

Source: Dataquest August 1989

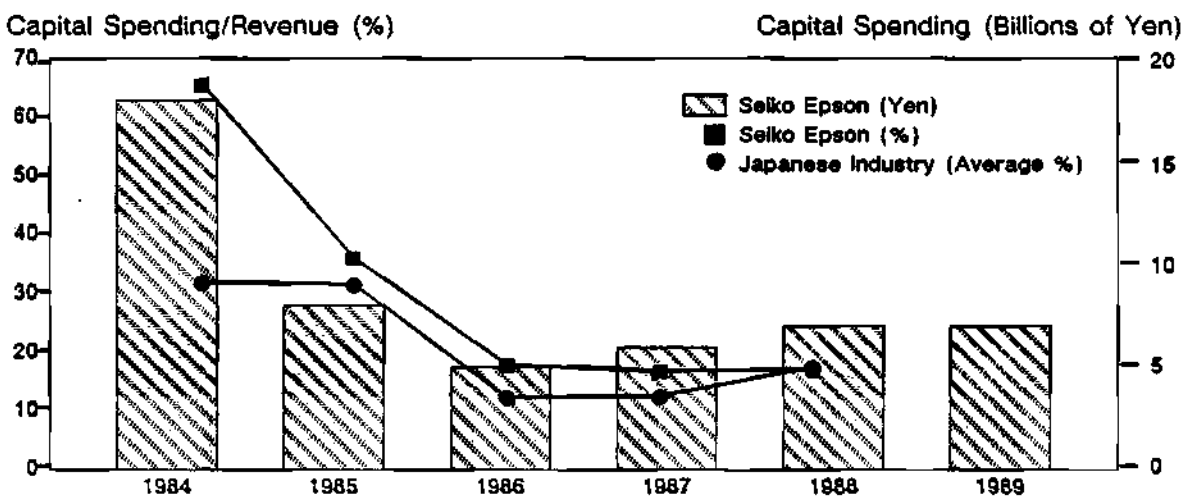
Capital Spending by Company: Japan

Seiko Epson

In 1988, Seiko Epson's ratio of capital spending to revenue was the same as the Japanese industry's average (see Figure 11). The Company's capital-spending level has been flat since 1987, basically hovering around the ¥7 billion ($54 million) level. Dataquest anticipates that Seiko will maintain its spending at this level.

Figure 11

Seiko Epson
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-11

Source: Dataquest August 1989

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Capital Spending by Company: Japan

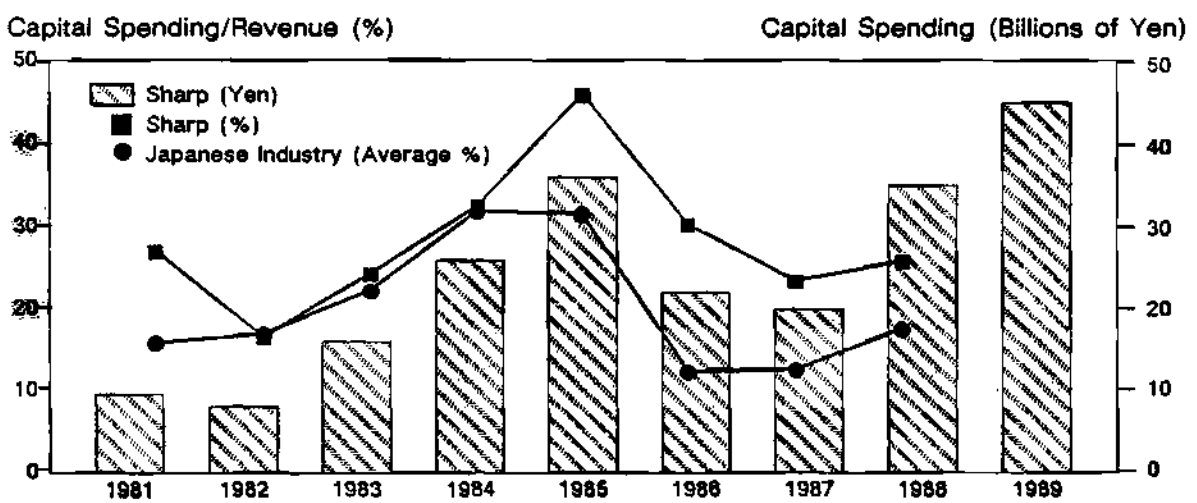
Sharp

Sharp's ratio of capital spending to revenue has been significantly above the Japanese industry's average since 1985 (see Figure 12). Dataquest expects Sharp to increase its capital spending by 29 percent in 1989, from ¥35 billion ($269 million) in 1988 to ¥45 billion ($346 million) in 1989.

In 1988, Sharp began construction of a ¥25 billion ($200 million) 1Mb DRAM plant at its existing facility in Fukuyama in Hiroshima Prefecture, Japan. This new fab will have a computer-intregrated manufacturing (CIM) system developed by Sharp's U.S. subsidiary, Sharp Microelectronics Technology. Dataquest also has heard reports that Sharp will resurrect a fab that was begun as a joint venture by RCA and Sharp. This fab will be located in Camus, Washington, in the United States.

Figure 12

Sharp
Capital Spending/Revenue versus Industry Average
and Total Capital Spending



0004587-12

Source: Dataquest August 1989

Capital Spending by Company: Japan

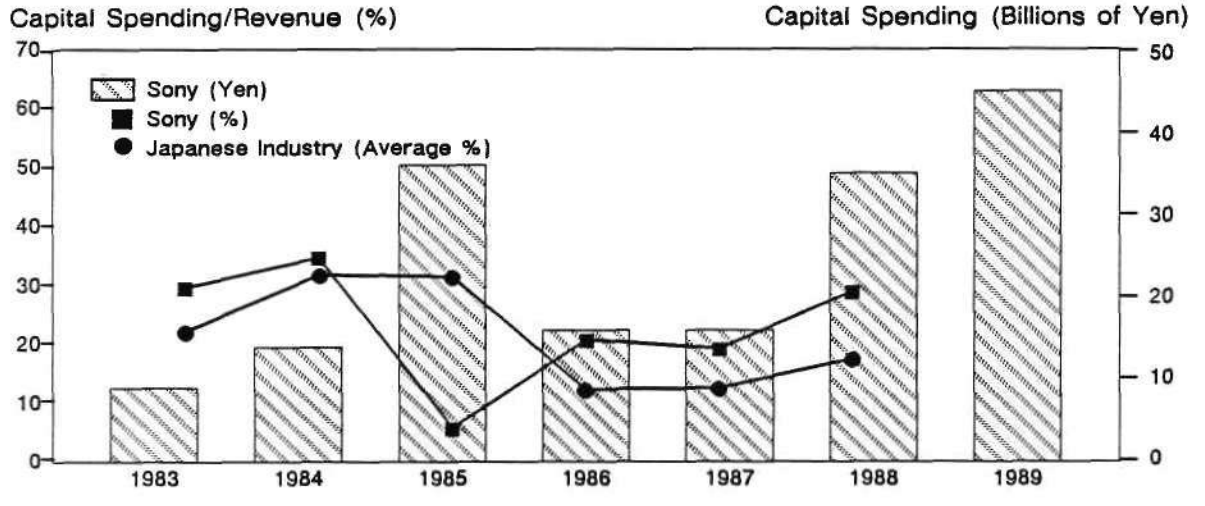
Sony

Sony's ratio of capital spending to revenue has been above the Japanese industry's average since 1985 (see Figure 13). Dataquest believes that Sony will increase its capital spending by 29 percent in 1989, from ¥35 billion ($269 million) to ¥45 billion ($346 million).

Sony will be the first Japanese semiconductor facility to construct a front-end facility in Thailand. This new plant will be located in Bangkadi Industrial Park, outside of Bangkok. Sony expects to begin production at this facility in October 1990. Initial devices fabricated at this facility primarily will be bipolar devices for compact disc (CD) players. Sony also is building a new facility for megabit SRAMs in Nagasaki, Japan. This fab will cost approximately ¥35 billion ($270 million).

Figure 13

Sony
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-13

Source: Dataquest August 1989

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Capital Spending by Company: Japan

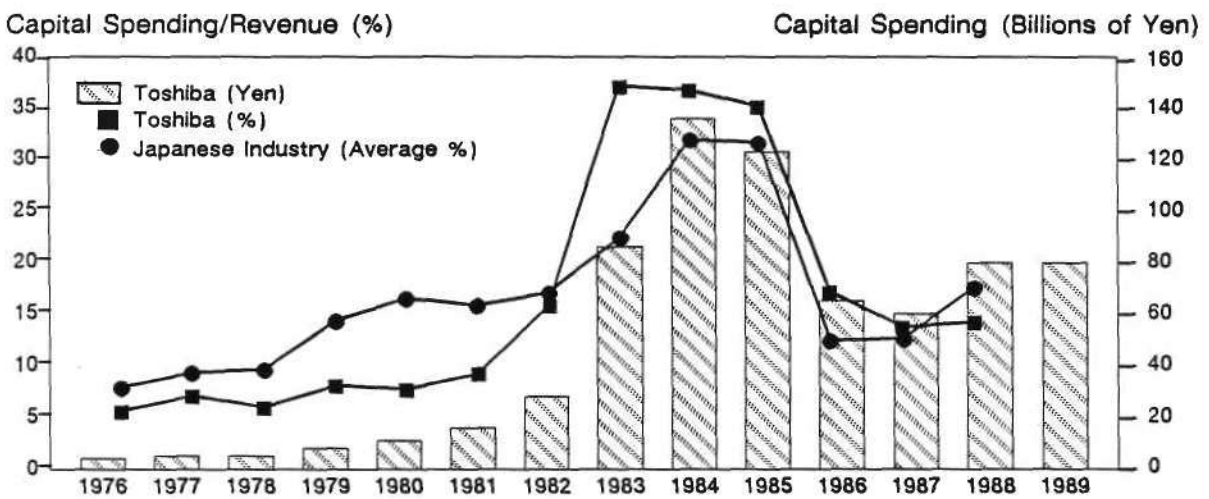
Toshiba

Toshiba's ratio of capital spending to revenue had been slightly above the Japanese industry's average until 1988, when it dipped below the industry's average (see Figure 14). Dataquest expects Toshiba 1989 capital spending to remain at last year's level of ¥80 billion ($615 million). Only two other merchant semiconductor companies in the world (Samsung and Goldstar) will match this level of spending in 1989.

Dataquest expects Toshiba to begin construction of a 4Mb-DRAM fab at its Ohita plant this year. The Company plans to spend ¥70 billion ($260 million) on this fab, which also will include a 16Mb DRAM prototype line.

Figure 14

Toshiba
Capital Spending/Revenue versus Industry Average and Total Capital Spending



0004587-14

Source: Dataquest August 1989

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Capital Spending Forecast

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Capital Spending Forecast

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Capital Spending Forecast

INTRODUCTION

Knowledge of semiconductor manufacturers' aggregate capital spending plans is important for strategic and tactical planning, both in the semiconductor industry itself and in the semiconductor equipment industry. Accurate capital spending forecasts help equipment vendors deploy their capital and manufacturing resources in order to have their products in the right markets at the right time.

This section will provide a forecast of capital spending, including captives, for the 1989 to 1993 period.

METHODOLOGY

To forecast capital spending, Dataquest uses an econometric model in which capital spending is a function of regional companies' revenue and capacity utilization. Using this model, we have obtained a regression coefficient of more than 90 percent.

A feature of our capital spending analysis is that we report capital spending in two different ways. The first is by regional semiconductor companies. The regional company capital spending report consists of worldwide semiconductor capital spending by captive companies and by companies in the Asia/Pacific region, Europe, Japan, and the United States.

The second way in which we report capital spending is by geographic region. Company capital spending information is allocated to the regions of the world in which those expenditures occur. For example, regional European capital spending includes all capital spending by Asia/Pacific, European, Japanese, U.S., and captive semiconductor companies in Europe, and excludes all spending by European companies on facilities outside of Europe.

Associated with regional capital spending will be a history and forecast of regional production. Regional production, which is different from regional consumption, is an estimate of the final market value of devices fabricated within that region. A device is classified as produced within a region if it is fabricated within that region, even though it may be tested, assembled, and shipped from another region. Thus, for example, regional European production will include all production by Asia/Pacific, European, Japanese, U.S., and captive companies in Europe, and will exclude all production by European companies outside of Europe. For a more complete discussion of production and consumption by region, readers should refer to the service section entitled "Production," located behind the "Industry Issues" tab in this binder.

THE FORECAST

Our new capital spending and revenue forecast for companies is shown in Table 1. Our new regional capital spending and production forecast is shown in Table 2.

Table 1

Capital Spending and Revenue by Companies

Capital Spending by Region	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	CAGR 1988-1993
North America	$3,139	$2,065	$1,445	$1,976	$ 2,746	$ 3,027	$ 2,866	$ 3,555	$ 4,671	$ 6,205	18%
Japan	3,771	3,233	1,760	2,343	4,485	5,431	4,996	7,061	9,753	13,273	24%
Europe	763	689	759	814	788	952	959	1,169	1,550	2,126	22%
ROW	434	507	363	453	952	1,747	1,763	2,163	2,380	2,838	24%
Captive	731	805	801	849	1,076	1,217	1,343	1,447	1,708	2,050	14%
Total	$8,838	$7,299	$5,129	$6,435	$10,046	$12,373	$11,927	$15,395	$20,063	$26,492	21%
Percent Change	106.4%	(17.4%)	(29.7%)	25.5%	56.1%	23.2%	(3.6%)	29.1%	30.3%	32.0%	
Production by Region											
North America	$13,948	$11,051	$12,809	$14,931	$18,686	$21,439	$20,953	$24,018	$29,194	$ 38,070	15%
Japan	11,456	10,144	14,160	18,476	25,397	29,124	28,468	32,666	39,805	52,060	15%
Europe	3,183	2,851	3,443	4,200	4,988	5,751	5,795	6,874	8,661	11,680	19%
ROW	238	295	422	671	1,414	1,890	2,674	3,901	5,375	7,550	40%
Captive	2,501	2,773	2,894	3,227	3,662	4,465	5,074	5,515	6,098	7,557	16%
Total	$31,326	$27,114	$33,728	$41,505	$54,148	$62,669	$62,964	$72,975	$89,132	$116,917	17%
Percent Change	44.5%	(13.4%)	24.4%	23.1%	30.5%	15.7%	0.5%	15.9%	22.1%	31.2%	

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest July 1989

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Table 2

Capital Spending and Production by Regions

Capital Spending by Region	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	CAGR 1988-1993
North America	$3,661	$2,629	$2,082	$2,594	$ 3,435	$ 3,826	$ 3,839	$ 4,619	$ 6,002	$ 7,863	18%
Japan	3,900	3,336	1,845	2,432	4,568	5,488	4,972	6,915	9,439	12,864	23%
Europe	816	800	765	875	1,025	1,250	1,307	1,684	2,231	2,920	23%
ROW	461	534	437	534	1,019	1,809	1,810	2,177	2,391	2,845	23%
Total	$8,838	$7,299	$5,129	$6,435	$10,046	$12,373	$11,927	$15,395	$20,063	$26,492	21%
Percent Change	106.4%	(17.4%)	(29.7%)	25.5%	56.1%	23.2%	(3.6%)	29.1%	30.3%	32.0%	
Production by Region											
North America	$15,596	$12,654	$14,456	$16,711	$20,289	$23,271	$23,418	$26,382	$32,108	$ 42,024	16%
Japan	12,007	10,651	14,686	18,958	25,903	29,632	28,492	32,537	39,270	51,536	15%
Europe	3,373	3,403	3,831	4,749	6,088	7,371	7,845	9,637	11,894	15,366	20%
ROW	349	406	756	1,088	1,868	2,395	3,208	4,419	5,860	7,992	34%
Total	$31,326	$27,114	$33,728	$41,505	$54,148	$62,669	$62,964	$72,975	$89,132	$116,917	17%
Percent Change	44.5%	(13.4%)	24.4%	23.1%	30.5%	15.7%	0.5%	15.9%	22.1%	31.2%	

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest July 1989

SEMS Semiconductor Manufacturing
0004541
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Capital Spending Forecast

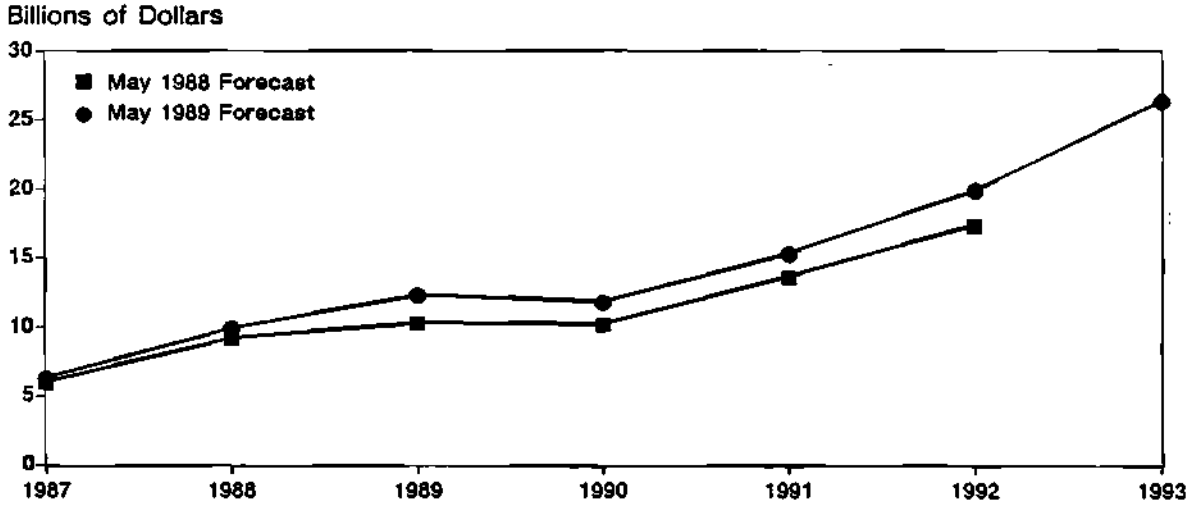
Metaphors of youthful expansion are no longer appropriate for the United States economy, the world economy, or the semiconductor industry. Although the industry continues to grow, many semiconductor manufacturers express concern about how long it can last. Dataquest believes that a downturn, or period of flat growth, for the semiconductor industry could begin by the end of 1989. Consequently, our capital spending forecast looks for less growth in 1989 than in 1988; we also are forecasting a downturn in capital spending of 3.6 percent in 1990. We believe, however, that the downturn in capital spending will not be severe, and that it will be brief.

Before 1990 is over, we expect recovery to be on its way. Overall, we expect capital spending to grow at a compound annual growth rate (CAGR) of 21 percent between 1988 and 1993.

Figure 1 compares our forecast of one year ago with our current forecast. Our forecast for 1988 undershot the mark by 7 percent—we forecast $9.3 billion and it was actually $10.0 billion. The main reason we were off was that the semiconductor industry had a slightly stronger 1988 than we had anticipated. Using our May, 1988 capital spending to revenue ratio (18.9 percent) against actual production in 1988, our forecast error is less than 2 percent; i.e., 0.189 x $54.1 billion = $10.2 billion.

Figure 1

Capital Spending Forecast Comparison



0004541-1

Source: Dataquest July 1989

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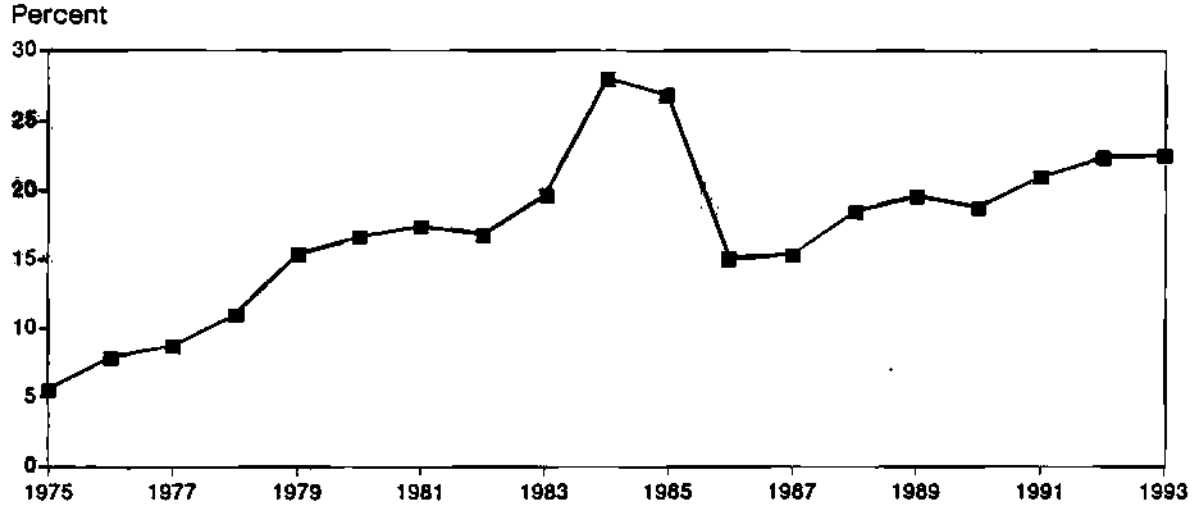
Capital Spending Forecast

Our forecast for 1989 through 1991 is similar to our previous forecast. The slope of the two forecast lines and the ratios of capital spending to revenue are basically equal. Of course, the current forecast is higher in dollars because the base year of the forecast (1988) is higher than we anticipated one year ago. Revenue and production (our independent variables) also are higher, and, therefore, our forecast is higher. The pattern of growth and the underlying dynamics of capital spending are the same as in last year's forecast and in this year's until 1992.

Readers, however, probably already will have noticed that Figure 1 shows that the slope of this year's forecast from 1991 to 1992 is higher than in our previous forecast. This represents a change in what we believe to be the underlying dynamics of capital spending in the future. We believe that the ratio of capital spending to revenue will increase in the future (see Figure 2) from 18 percent in 1988 to 23 percent in 1993. We believe that capital productivity will cease to climb in the near future and will actually decline, albeit slightly, thus causing the increase in this ratio.

Figure 2

Capital Spending as a Percentage of Revenue



Increasing device complexity and ever-smaller geometries are the reasons behind the forecast slowdown and decline in capital productivity. Not only are the devices harder to make, but equipment and fabs also are more expensive. SEMS will be publishing a more in-depth discussion of capital productivity later this year.

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Capital Spending Forecast

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Capital Spending Forecast

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Capital Spending Forecast

INTRODUCTION

Knowledge of aggregate capital spending plans of semiconductor manufacturers is important for strategic and tactical planning, both in the semiconductor industry itself and in the semiconductor equipment industry. Accurate forecasts of capital spending help equipment vendors to deploy their capital and manufacturing resources in order to have their products in the right markets at the right time.

This section provides a forecast of capital spending, including captives, for the period 1988 to 1992, as well as historical figures from 1980 to 1987. It also includes a discussion of the forces that drive capital spending, especially pertaining to the competitive relationship between the Japanese and U.S. semiconductor industries.

Methodology

To forecast capital spending, Dataquest uses an econometric model in which capital spending is a function of regional companies' revenue and capacity utilization. Using this model, we have obtained a regression coefficient of more than 90 percent.

A new feature of our capital spending analysis is that we will report capital spending by regional companies and also by geographical areas. The regional companies' report will consist of worldwide semiconductor merchant capital spending and semiconductor merchant revenue by Asia-Pacific, European, Japanese, and U.S. companies. We will also report capital spending and production for the captive manufacturers.

Spending by region will include capital spending within a given geographical area by all companies, including captives. Thus, for example, regional European capital spending will include all capital spending by Asia-Pacific, European, Japanese, U.S., and captive companies in Europe. It will exclude all spending by European companies on facilities outside of Europe.

Associated with regional capital spending will be a history and forecast of regional production. Regional production, which is different from regional consumption, is an estimate of the final market value of devices fabricated within a given region. A device is classified as produced within a region if it is fabricated within that region, even though it may be tested and assembled in, and shipped from, another region. Thus, for example, regional European production will include all production by Asia-Pacific, European, Japanese, U.S., and captive companies in Europe, and will exclude all production by European companies outside of Europe. For a more complete discussion of production and consumption by region, refer to the section entitled "Production" in this binder.

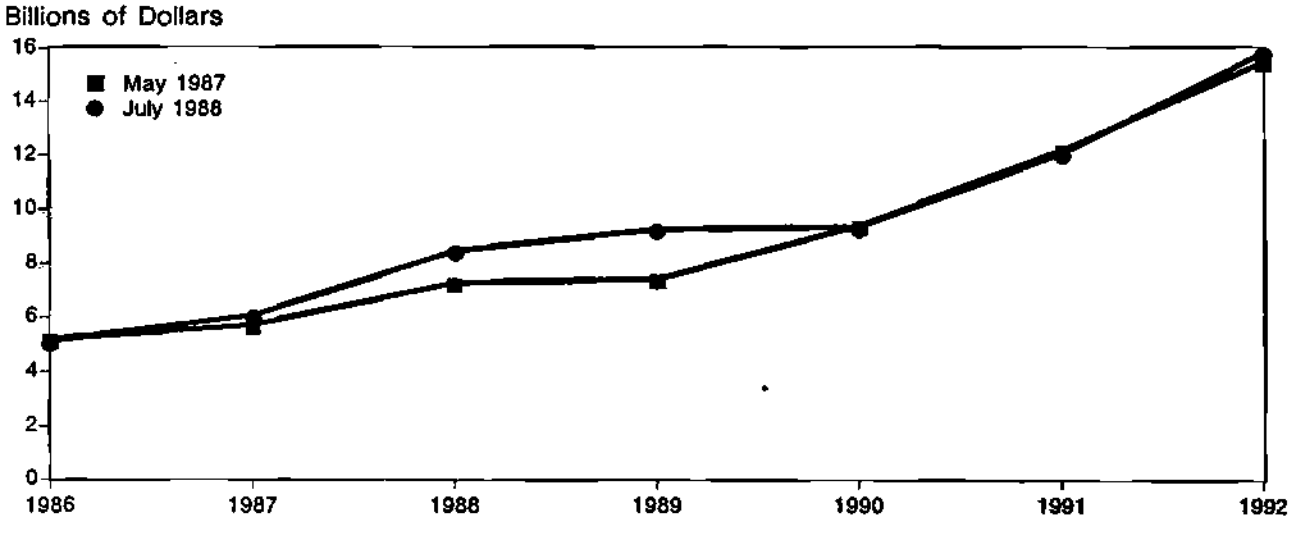
Capital Spending Forecast

SUMMARY

Figure 1 compares our forecast of one year ago with our current forecast. Our May 1987 forecast was 6 percent less buoyant than the industry actually turned out to be. We called $5.9 billion, and it came out to be $6.1 billion. However, our last year's forecast used a yen/$ exchange rate of 154 yen to the dollar. The actual rate turned out to be 140. Factoring in this exchange rate difference, our forecast was only 3 percent shy of the mark—fairly close, even without considering the exchange rate appreciation between Europe and the United States.

Figure 1

Forecast Comparison



Source: Dataquest
August 1988

Our forecast for 1988 through 1990 is quite different from our forecast of a year ago. This is because the economic recession and consequent slowdown in the semiconductor industry, which we thought would occur in the latter part of this year and early 1989, has not happened. We now believe that the slowdown will occur in the latter part of 1989, and have therefore pushed back the slowdown in capital spending growth to reflect the continually surprising (and welcome) vigor of the U.S. economy. Our long-term view of capital spending, however, has not changed (as also can be seen from Figure 1). After the recession, we believe that the growth in capital spending will be as we have been saying—vigorous.

Our new capital spending and revenue forecast for companies is shown in Table 1. Our new regional capital spending and production forecast is shown in Table 2.

Capital Spending Forecast

Table 1

Capital Spending and Revenue by Regional Companies (Billions of Yen, Millions of Dollars)

	1980	1981	1982	1983	1984	1985	1986
Japanese Revenue (Yen)	¥ 837	¥ 1,162	¥ 1,336	¥ 1,794	¥ 2,706	¥ 2,404	¥ 2,389
Percent Change	36%	39%	15%	34%	51%	(11%)	(1%)
Capital Spending (Yen)	¥ 142	¥ 185	¥ 229	¥ 415	¥ 894	¥ 769	¥ 294
Percent Change	56%	30%	24%	81%	115%	(14%)	(62%)
Capital Spending/ Revenue	17%	16%	17%	23%	33%	32%	12%
Japanese Revenue	$ 3,726	$ 5,252	$ 5,375	$ 7,633	$11,419	$10,100	$14,305
Percent Change	34%	41%	2%	42%	50%	(12%)	42%
Capital Spending	$ 632	$ 834	$ 921	$ 1,768	$ 3,771	$ 3,233	$ 1,760
Percent Change	54%	32%	10%	92%	113%	(14%)	(46%)
Capital Spending/ Revenue	17%	16%	17%	23%	33%	32%	12%
North American Revenue	$ 8,572	$ 7,628	$ 7,859	$ 9,628	$13,903	$11,003	$11,697
Percent Change	27%	(11%)	3%	23%	44%	(21%)	6%
Capital Spending	$ 1,347	$ 1,233	$ 1,131	$ 1,434	$ 3,039	$ 2,072	$ 1,480
Percent Change	26%	(8%)	(8%)	29%	109%	(32%)	(24%)
Capital Spending/ Revenue	16%	16%	14%	15%	22%	19%	14%
European Revenue	$ 1,785	$ 1,903	$ 1,929	$ 2,230	$ 3,173	$ 2,839	$ 3,455
Percent Change	16%	7%	1%	16%	42%	(11%)	22%
Capital Spending	$ 365	$ 390	$ 370	$ 408	$ 763	$ 789	$ 759
Percent Change	55%	7%	(5%)	10%	87%	(10%)	10%
Capital Spending/ Revenue	20%	20%	19%	18%	24%	24%	22%

(Continued)

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Capital Spending Forecast

Table 1 (Continued)

Capital Spending and Revenue
by Regional Companies
(Billions of Yen, Millions of Dollars)

	1980	1981	1982	1983	1984	1985	1986
Asia Pacific							
Revenue	$ 35	$ 45	$ 98	$ 175	$ 237	$ 294	$ 425
Percent Change	40%	29%	118%	79%	35%	24%	45%
Capital Spending	$ 10	$ 20	$ 45	$ 126	$ 434	$ 439	$ 273
Percent Change	233%	100%	125%	180%	245%	1%	(38%)
Capital Spending/ Revenue	29%	44%	46%	72%	183%	149%	64%
Captive Revenue	N/A	$ 1,675	$ 1,841	$ 2,016	$ 2,501	$ 2,773	$ 2,894
Percent Change	N/A	N/A	10%	10%	24%	11%	4%
Capital Spending	$ 0	$ 414	$ 432	$ 482	$ 731	$ 805	$ 801
Percent Change	N/A	N/A	4%	12%	52%	10%	0%
Capital Spending/ Revenue	N/A	20%	18%	17%	25%	24%	20%
North America	$ 1,347	$ 1,233	$ 1,131	$ 1,454	$ 3,039	$ 2,072	$ 1,480
Japan	$ 632	$ 834	$ 921	$ 1,768	$ 3,771	$ 3,233	$ 1,760
Europe	$ 365	$ 390	$ 370	$ 408	$ 763	$ 689	$ 759
Asia-Pacific	$ 10	$ 20	$ 45	$ 126	$ 434	$ 439	$ 273
Captive	0	$ 414	$ 432	$ 482	$ 731	$ 805	$ 801
Total Worldwide Capital Spending	$ 2,355	$ 2,891	$ 2,899	$ 4,238	$ 8,738	$ 7,238	$ 5,173
Percent Change	36.7%	22.8%	0.3%	46.2%	106.2%	(17.2%)	(28.5%)
North America	$ 8,572	$ 7,628	$ 7,859	$ 9,628	$13,903	$11,003	$11,697
Japan	$ 3,726	$ 5,252	$ 5,375	$ 7,633	$11,419	$10,100	$14,305
Europe	$ 1,785	$ 1,903	$ 1,929	$ 2,230	$ 3,173	$ 2,839	$ 3,455
Asia-Pacific	$ 35	$ 45	$ 98	$ 175	$ 237	$ 294	$ 425
Captive	0	$ 1,675	$ 1,841	$ 2,016	$ 2,501	$ 2,773	$ 2,894
Total Worldwide Production Revenue	$14,118	$16,503	$17,102	$21,682	$31,233	$27,009	$32,776
Percent Change	27.0%	16.9%	3.6%	26.8%	44.1%	(13.5%)	21.4%

(Continued)

Capital Spending Forecast

Table 1 (Continued)

Capital Spending and Revenue
by Regional Companies
(Billions of Yen, Millions of Dollars)

	1987	1988	1989	1990	1991	1992	CAGR (1987-1992)
Japanese Revenue (Yen)	¥ 2,583	¥ 2,933	¥ 3,240	¥ 3,158	¥ 3,561	¥ 4,221	10%
Percent Change	8%	14%	10%	(3%)	13%	19%	
Capital Spending (Yen)	¥ 337	¥ 476	¥ 509	¥ 504	¥ 681	¥ 919	22%
Percent Change	15%	41%	7%	(1%)	35%	35%	
Capital Spending/ Revenue	13%	16%	16%	16%	19%	22%	
Japanese Revenue	$17,938	$22,560	$24,927	$24,290	$27,392	$32,468	13%
Percent Change	25%	26%	10%	(3%)	13%	19%	
Capital Spending	$ 2,340	$ 3,662	$ 3,918	$ 3,879	$ 5,236	$ 7,069	25%
Percent Change	33%	56%	7%	(1%)	35%	35%	
Capital Spending/ Revenue	13%	16%	16%	16%	19%	22%	
North American Revenue	$13,890	$17,084	$17,938	$17,669	$20,780	$24,992	12%
Percent Change	19%	23%	5%	(2%)	18%	20%	
Capital Spending	$ 1,834	$ 2,566	$ 2,752	$ 2,477	$ 3,155	$ 4,294	19%
Percent Change	16%	40%	7%	(10%)	27%	36%	
Capital Spending/ Revenue	13%	15%	15%	14%	15%	17%	
European Revenue	$ 4,015	$ 4,761	$ 5,452	$ 5,639	$ 6,443	$ 8,249	15%
Percent Change	16%	19%	15%	3%	14%	28%	
Capital Spending	$ 724	$ 730	$ 861	$ 973	$ 1,245	$ 1,432	15%
Percent Change	(5%)	1%	18%	13%	28%	15%	
Capital Spending/ Revenue	18%	15%	16%	17%	19%	17%	

(Continued)

Capital Spending Forecast

Table 1 (Continued)

Capital Spending and Revenue
by Regional Companies
(Billions of Yen, Millions of Dollars)

	1987	1988	1989	1990	1991	1992	CAGR (1987-1992)
Asia Pacific							
Revenue	$ 656	$ 938	$ 1,247	$ 1,434	$ 2,079	$ 3,160	37%
Percent Change	54%	43%	33%	15%	45%	52%	
Capital Spending	$ 355	$ 451	$ 541	$ 730	$ 949	$ 1,139	26%
Percent Change	30%	27%	20%	35%	30%	20%	
Capital Spending/ Revenue	54%	48%	43%	51%	46%	36%	
Captive Revenue	$ 3,357	$ 3,779	$ 4,522	$ 5,215	$ 6,072	$ 7,071	16%
Percent Change	16%	13%	20%	15%	16%	16%	
Capital Spending	$ 883	$ 1,110	$ 1,232	$ 1,380	$ 1,594	$ 1,980	18%
Percent Change	10%	26%	11%	12%	15%	24%	
Capital Spending/ Revenue	20%	20%	16%	16%	15%	16%	
North America	$ 1,834	$ 2,566	$ 2,752	$ 2,477	$ 3,155	$ 4,294	19%
Japan	$ 2,340	$ 3,662	$ 3,918	$ 3,879	$ 5,236	$ 7,069	25%
Europe	$ 724	$ 730	$ 861	$ 973	$ 1,245	$ 1,432	15%
Asia-Pacific	$ 355	$ 451	$ 541	$ 730	$ 949	$ 1,139	26%
Captive	883	$ 1,110	$ 1,232	$ 1,380	$ 1,594	$ 1,980	18%
Total Worldwide Capital Spending	$ 6,136	$ 8,518	$ 9,304	$ 9,438	$12,179	$15,914	21%
Percent Change	18.6%	38.8%	9.2%	1.4%	29.0%	30.7%	
North America	$13,890	$17,084	$17,938	$17,669	$20,780	$24,992	12%
Japan	$17,938	$22,560	$24,927	$24,290	$27,392	$32,468	13%
Europe	$ 4,015	$ 4,761	$ 5,452	$ 5,639	$ 6,443	$ 8,249	15%
Asia-Pacific	$ 656	$ 938	$ 1,247	$ 1,434	$ 2,079	$ 3,160	37%
Captive	$ 3,357	$ 3,779	$ 4,522	$ 5,215	$ 6,072	$ 7,071	16%
Total Worldwide Production Revenue	$39,855	$49,122	$54,086	$54,247	$62,767	$75,939	14%
Percent Change	21.6%	23.3%	10.1%	0.3%	15.7%	21.0%	

N/A = Not Available
Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
August 1988

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Capital Spending Forecast

Table 2

Capital Spending and Production
by Regions

	1980	1981	1982	1983	1984	1985	1986
Japanese Production (Yen)	¥ 837	¥ 1,182	¥ 1,414	¥ 1,893	¥ 2,837	¥ 2,524	¥ 2,477
Percent Change	36%	41%	20%	34%	50%	(11%)	(2%)
Capital Spending (Yen)	¥ 142	¥ 189	¥ 242	¥ 433	¥ 924	¥ 794	¥ 310
Percent Change	54%	33%	28%	79%	113%	(14%)	(61%)
Capital Spending/ Production	17%	16%	17%	23%	33%	31%	13%
Japanese Production	$ 3,726	$ 5,341	$ 5,688	$ 8,055	$11,970	$10,606	$14,832
Percent Change	34%	43%	6%	42%	49%	(11%)	40%
Capital Spending	$ 632	$ 856	$ 975	$ 1,841	$ 3,897	$ 3,336	$ 1,856
Percent Change	52%	35%	14%	89%	112%	(14%)	(44%)
Capital Spending/ Production	17%	16%	17%	23%	33%	31%	13%
North American Production	$ 8,576	$ 8,971	$ 9,017	$10,012	$15,551	$12,607	$13,343
Percent Change	25%	5%	1%	21%	43%	(19%)	6%
Capital Spending	$ 1,365	$ 1,582	$ 1,449	$ 1,804	$ 3,569	$ 2,635	$ 2,184
Percent Change	26%	16%	(8%)	24%	98%	(26%)	(17%)
Capital Spending/ Production	16%	18%	16%	17%	23%	21%	16%
European Production	$ 1,781	$ 2,145	$ 2,299	$ 2,539	$ 3,474	$ 3,402	$ 4,057
Percent Change	24%	20%	7%	10%	37%	(2%)	19%
Capital Spending	$ 347	$ 433	$ 430	$ 466	$ 838	$ 803	$ 834
Percent Change	57%	25%	(1%)	$ 1,058	80%	(4%)	4%
Capital Spending/ Production	19%	20%	19%	$ 871	24%	24%	21%

(Continued)

Capital Spending Forecast

Table 2 (Continued)

Capital Spending and Production by Regions

	1980	1981	1982	1983	1984	1985	1986
Asia Pacific							
Production	$ 35	$ 45	$ 98	$ 175	$ 237	$ 394	$ 545
Percent Change	40%	29%	118%	79%	35%	66%	38%
Capital Spending	$ 10	$ 20	$ 45	$ 126	$ 434	$ 463	$ 299
Percent Change	233%	100%	125%	180%	245%	7%	(35%)
Capital Spending/ Production	29%	44%	46%	72%	183%	118%	55%
North America	$ 1,365	$ 1,582	$ 1,449	$ 1,804	$ 3,569	$ 2,635	$ 2,184
Japan	$ 632	$ 856	$ 975	$ 1,841	$ 3,897	$ 3,336	$ 1,856
Europe	$ 347	$ 433	$ 430	$ 466	$ 838	$ 803	$ 834
Asia-Pacific	$ 10	$ 20	$ 45	$ 126	$ 434	$ 463	$ 299
Total Worldwide Capital Spending	$ 2,355	$ 2,891	$ 2,899	$ 4,238	$ 8,738	$ 7,238	$ 5,173
Percent Change	36.4%	22.8%	0.3%	46.2%	106.2%	(17.2%)	(28.5%)
North America	$ 8,576	$ 8,971	$ 9,017	$10,912	$15,551	$12,607	$13,343
Japan	$ 3,726	$ 5,341	$ 5,688	$ 8,055	$11,970	$10,606	$14,832
Europe	$ 1,781	$ 2,145	$ 2,299	$ 2,539	$ 3,474	$ 3,402	$ 4,057
Asia-Pacific	$ 35	$ 45	$ 98	$ 175	$ 237	$ 394	$ 545
Total Worldwide Production Revenue	$14,118	$16,503	$17,102	$21,681	$31,232	$27,009	$32,776
Percent Change	27.0%	16.9%	3.6%	26.8%	44.1%	(13.5%)	21.4%

(Continued)

Capital Spending Forecast

Table 2 (Continued)

Capital Spending and Production by Regions

	1987	1988	1989	1990	1991	1992	CAGR (1987-1992)
Japanese Production (Yen)	¥ 2,665	¥ 3,026	¥ 3,324	¥ 3,179	¥ 3,571	¥ 4,230	10%
Percent Change	8%	14%	10%	(4%)	12%	18%	
Capital Spending (Yen)	¥ 351	¥ 493	¥ 526	¥ 509	¥ 681	¥ 917	21%
Percent Change	13%	40%	7%	(3%)	34%	35%	
Capital Spending/ Production	13%	16%	16%	16%	19%	22%	
Japanese Production	$18,504	$23,274	$25,565	$24,454	$27,471	$32,538	12%
Percent Change	25%	26%	10%	(4%)	12%	18%	
Capital Spending	$ 2,440	$ 3,796	$ 4,044	$ 3,919	$ 5,238	$ 7,056	24%
Percent Change	31%	56%	7%	(3%)	34%	35%	
Capital Spending/ Production	13%	16%	16%	16%	19%	22%	
North American Production	$15,791	$19,219	$20,858	$21,914	$25,939	$31,136	15%
Percent Change	18%	22%	9%	5%	18%	20%	
Capital Spending	$ 2,473	$ 3,332	$ 3,654	$ 3,729	$ 4,640	$ 6,056	20%
Percent Change	13%	35%	10%	2%	24%	31%	
Capital Spending/ Production	16%	17%	18%	17%	18%	19%	
European Production	$ 4,765	$ 5,553	$ 6,299	$ 6,446	$ 7,253	$ 9,078	14%
Percent Change	17%	17%	13%	2%	13%	25%	
Capital Spending	$ 843	$ 923	$ 1,061	$ 1,135	$ 1,402	$ 1,706	15%
Percent Change	1%	9%	15%	7%	23%	22%	
Capital Spending/ Production	18%	17%	17%	18%	19%	19%	

(Continued)

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Capital Spending Forecast

Table 2 (Continued)

Capital Spending and Production by Regions

	1987	1988	1989	1990	1991	1992	CAGR (1987-1992)
Asia Pacific							
Production	$ 796	$ 1,076	$ 1,364	$ 1,433	$ 2,104	$ 3,188	32%
Percent Change	46%	35%	27%	5%	47%	51%	
Capital Spending	$ 380	$ 468	$ 545	$ 655	$ 900	$ 1,096	24%
Percent Change	27%	23%	16%	20%	37%	22%	
Capital Spending/ Production	48%	44%	40%	46%	43%	34%	
North America	$ 2,473	$ 3,332	$ 3,654	$ 3,729	$ 4,640	$ 6,054	20%
Japan	$ 2,440	$ 3,796	$ 4,044	$ 3,919	$ 5,238	$ 7,056	24%
Europe	$ 843	$ 923	$ 1,061	$ 1,135	$ 1,402	$ 1,706	15%
Asia-Pacific	$ 380	$ 468	$ 545	$ 655	$ 900	$ 1,096	24%
Total Worldwide Capital Spending	$ 6,136	$ 8,518	$ 9,304	$ 9,438	$12,179	$15,914	21%
Percent Change	18.6%	38.8%	9.2%	1.4%	29.0%	30.7%	
North America	$15,791	$19,219	$20,858	$21,914	$24,939	$31,136	15%
Japan	$18,504	$23,274	$25,565	$24,454	$27,471	$32,538	12%
Europe	$ 4,765	$ 5,553	$ 6,299	$ 6,446	$ 7,253	$ 9,078	14%
Asia-Pacific	$ 796	$ 1,076	$ 1,364	$ 1,433	$ 2,104	$ 3,188	32%
Total Worldwide Production Revenue	$39,855	$49,122	$54,086	$54,247	$62,767	$75,939	14%
Percent Change	21.6%	23.3%	10.1%	0.3%	15.7%	21.0%	

N/A = Not Available
Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
August 1988

Capital Spending Forecast

1988

Buoyed by a generally expanding economy and growing end-use markets, semiconductor production has continued to expand. For this reason, we believe that the 1988 spending level will be approximately equal to that of 1984 ($8.8 billion in 1984 versus $8.5 billion in 1988). Because of the continuing high demand for devices, capacity utilization is now at about 80 percent industry-wide. Capacity utilization rates for devices with smaller geometries, however, are generally more than 80 percent; in some cases, such as DRAMs and 32-bit microprocessors, demand exceeds available supply. Semiconductor manufacturers, though spending for more capacity, will remain cautious; they prefer to increase equipment availability and to increase yields before adding capacity. Dataquest does not, therefore, expect 1988 growth to be anywhere near the 1984 level.

Capital spending will be driven not only by increases in the level of demand, but also by the continuing need for equipment upgrades. The goals of equipment upgrades are both technological and economic: Upgrades are technologically necessary in order to manufacture increasingly complex devices with ever smaller geometries. They are economically necessary in order to increase equipment productivity in an increasingly fierce competitive environment.

We expect Japanese companies to increase capital spending by 56 percent in dollars over 1987. However, measured in yen, the spending increase will not be quite so abrupt (41 percent). Measured in yen or in dollars, this is healthy and welcome growth.

This year, U.S. companies will increase their spending by 40 percent over 1987. Spending by Asia-Pacific companies will reach $451 million in 1988, a 27 percent growth over 1987. Spending by captives will also see a healthy increase in 1988. We expect captive capital spending to grow to $1.1 billion, an increase of 26 percent.

Spending by European companies will be relatively weak in 1988, rising only 1 percent to $730 million. This relative flat spending has two causes. The first is that European companies like Philips and Siemens had strong spending plans that they carried through in spite of the recent downturn. These spending programs are now complete and the facilities they generated (Philips at Einhoven, The Netherlands, and Siemens at Regensburg, West Germany), are now going into volume production. Consequently, we can expect both Philips and Siemens to moderate their spending plans somewhat. The second reason for the slowdown is the recent merger of SGS and Thomson into SGS/Thomson. This new world-class manufacturer is now taking time to step back, examine, restructure, and rationalize its operations.

Beyond 1988

In 1989, we expect to see a slowdown in the growth of semiconductor production and, consequently, in the growth of capital spending. This is because we expect the U.S. economy (and therefore the end markets that semiconductors serve) to undergo a slight recession in the latter part of 1989.

Capital Spending Forecast

Growth in production and capital spending should therefore be much stronger in the first half of 1989 than in the second half. We expect to see some decline in both production and capital spending in the second half of 1989. We foresee that semiconductor production will grow 10 percent on an annual basis in 1989 and capital spending will grow 9 percent on an annual basis.

The negative growth rate in the second half of 1989 will likely continue into the first half of 1990. However, growth should resume in the second half of 1990. As a result of a continuing decline in the first half of 1990, followed by the beginnings of a recovery will be that, for 1990, both production and capital spending will be flat on an annual basis.

After 1990, however, we expect a resumption of vigorous growth. Overall, for the period 1987 to 1992, capital spending will grow at a compound annual growth rate (CAGR) of 21 percent. Spending in this period will be led by the Japanese companies that, by 1992, will be spending more than $7 billion on capital equipment.

Spending worldwide after 1990 will be driven by the need for equipment upgrades that will be necessary for new generations of devices, and for the added capacity that will be necessary for a growing world economy. Capital spending will also be driven by the need for companies to replenish the capital stock that they brought on-stream in 1984.

The need to replenish 1984's and 1985's capital stock is especially important for Japanese companies, which more than doubled their installed base between 1983 and 1986. Consequently, 1984's and 1985's capital stock will represent a very large part of Japanese companies' installed base, and a large part of their spending will be dedicated to replacing it. Spending in dollars by Japanese companies between 1987 and 1992 will grow at a CAGR of 25 percent in dollars. In yen, the growth rate will be somewhat lower—22 percent.

By 1992, U.S. merchant spending will be $4.2 billion. The growth rate of U.S. company spending will be at a CAGR of 19 percent from 1987–1992.

Capital spending by European companies between 1987 and 1992 will grow the least of any other region, with a CAGR of 15 percent. However, after 1988, spending growth in Europe will resume at an above average rate. Spending by European companies will equal $1.4 billion in 1992.

Capital spending by Asia–Pacific companies continues to grow faster than spending by any other region companies in the world. Their CAGR for 1987 to 1992 is forecast at 26 percent. In 1987, spending by Asia–Pacific companies was 62 percent that of European companies. By 1992, we expect this figure to rise to 80 percent of the European level.

Capital Spending Forecast

Captive semiconductor manufacturers include such companies as AT&T, Delco, IBM, and others. A captive manufacturer is distinguished from a merchant manufacturer in that a captive produces semiconductors for its own internal use. Captive manufacturers do not sell their devices on the merchant market.

These manufacturers are a major market for semiconductor equipment. Generally, their capital spending is more stable than that of merchant manufacturers. The stability is because captives produce for internal consumption rather than for the volatile merchant market.

Spending by captives between 1987 and 1992 will grow at a CAGR (18 percent) that is less than the industry average. However, it is important to note that we expect the growth rate of capital spending for captives to increase over what is has been in the recent past. For the 1981 to 1987 period, the CAGR of captive capital spending was only 13 percent. Captives want their own capacity for times of shortages, so that they are not dependent on only one manufacturing region for a timely supply of devices.

Captives have manufacturing facilities in Japan, the United States, and Europe. Captive activity in Europe, where both AT&T and IBM are building major facilities, is especially strong this year. AT&T began assembly and test in its new Madrid, Spain, plant in May of 1988, and expects to be in full-scale production by mid-1989. IBM is building the world's largest 200mm line at its Sindelfingen, West Germany, facility.

JAPAN AND THE UNITED STATES: NO WINNER IN SIGHT

Measured in dollars, Japan will increase its 1988 capital spending at a much faster rate than U.S. merchant companies (56 percent versus 40 percent). For the 1987 to 1992 forecast period, the story is similar: a CAGR of 25 percent for Japanese companies versus 19 percent for U.S. merchant companies. In 1992, Japanese company capital spending will stand at more than $7 billion, while the U.S. merchants will spend a mere $4.3 billion. Measured in dollars, it appears that the Japanese merchant semiconductor industry will tower over that of the United States merchants. If capital spending by the U.S. captives is added to that of the U.S. merchants, we estimate that Japanese company capital spending in 1992 will still be 13 percent greater than the combined U.S. merchants and captives ($7.1 billion versus $6.3 billion).

However, measured in local currencies, (i.e., measuring growth rates and installed bases in yen for Japanese companies and dollars for U.S. merchant companies), the story is quite different. In 1988, Japanese companies will increase their spending by 41 percent in yen, as opposed to 40 percent for U.S. merchant companies—essentially the same percentage growth. Japanese capital spending in 1988 will likely be 55 percent of Japanese capital spending in 1984. U.S. merchant capital spending in 1988 will be 84 percent of U.S. merchant capital spending in 1984.

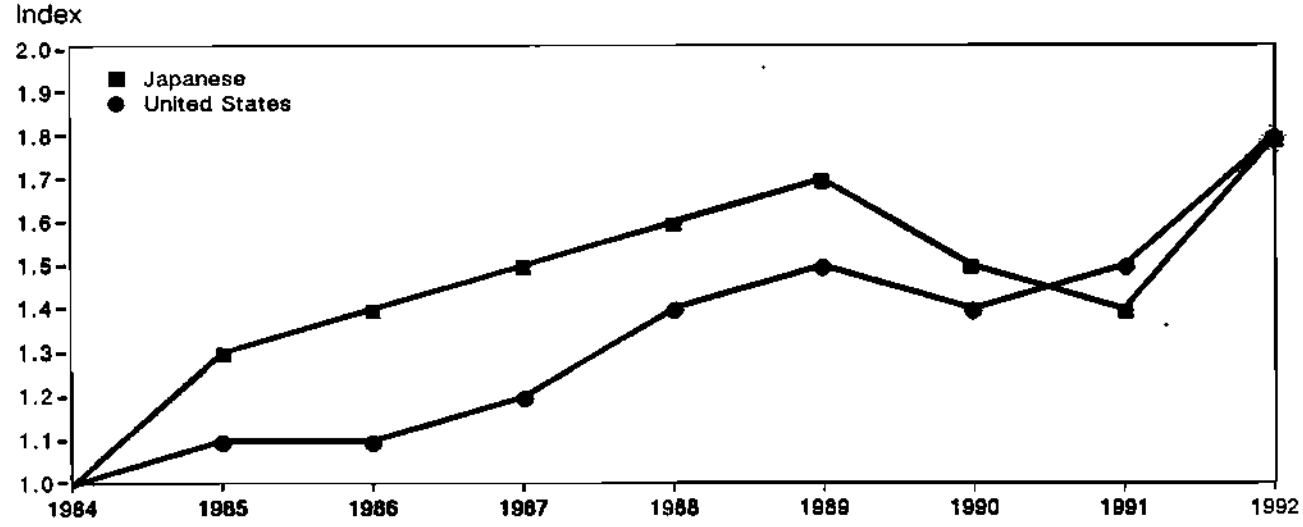
Capital Spending Forecast

An even more telling comparison is for the period 1984 to 1992. 1984 was the peak year for capital spending for both Japanese and U.S. merchant companies. In our forecast horizon, 1992 is the peak year. The growth rate of capital spending for Japanese companies from 1984 to 1992 is 1 percent in yen. That of U.S. merchant companies is 4 percent in dollars.

Figure 2 shows the growth of Japanese and U.S. merchant companies' installed base of property, plants, and equipment. The growth of each industry's installed base is indexed to 1984 (the year that the Japanese industry achieved parity with the U.S. merchant industry). If, in 1984, the installed base of each industry was essentially the same size, then, in 1985, the Japanese installed base surpassed that of the U.S. merchants by a large margin. However, in 1990, when a substantial amount of the Japanese company installed base from 1984 will be retired, the installed base of U.S. merchant companies will likely surpass that of Japanese companies. By 1992, we expect the size of the installed base of Japanese companies and U.S. merchant companies to be about equal. If the installed base of the U.S. captives is added to that of the U.S. merchants, then, measured in local currencies, the combined U.S. installed base is substantially larger than the installed base of the Japanese industry.

Figure 2

Japanese and U.S. Installed Base



Source: Dataquest
August 1988

Capital Spending Forecast

PRODUCTION AND CAPITAL SPENDING

Production is one of the basic forces that shape capital spending, which is a derived demand. If the semiconductor end users do not have a strong demand for their products, then the demand for semiconductors, and consequently for capital equipment, will be weak. While we expect that the long-term growth of semiconductor production will remain vigorous, it will not be quite as vigorous as before.

From 1975 to 1981, semiconductor production grew at a 25 percent CAGR. For the 1982 to 1986 period, this growth rate slowed to 18 percent. Dataquest now expects semiconductor production to grow even more slowly, at a 15 percent rate, from 1986 to 1992. This new, lower, long-term growth rate is due to the absence of a new "hula-hoop," such as the PC, to drive the industry as it did from 1982 to 1984. It is also due to the success of the industry. Since semiconductors are now found throughout the economy, they therefore will be increasingly influenced by the secular trends of the economy.

Another reason for the slowdown in the CAGR of capital spending is that of increasing productivity of capital. Capital productivity is the amount of revenue that is generated with a given installed base of property, plant, and equipment (PPE). Historically, this is a ratio that has declined. We believe, however, that capital productivity has begun to rise (see Figure 3). There are several reasons for this. Computer-integrated manufacturing (CIM) will allow manufacturers to schedule many different product mixes and maintain line balance while increasing equipment utilization. We estimate that equipment utilization is in the neighborhood of 40 percent presently. We expect that manufacturers will increase their yields because automation will remove people from clean rooms and because of lower particulate from semiconductor equipment and materials.

Figure 4 shows the effects of increasing capital productivity. Until 1985, the percentage change in capital spending exceeded that of the percentage change of production in every year but one. From 1985 to 1992, we expect the percentage change in capital spending to exceed that of production only twice, and by much less substantial margins than in the previous period.

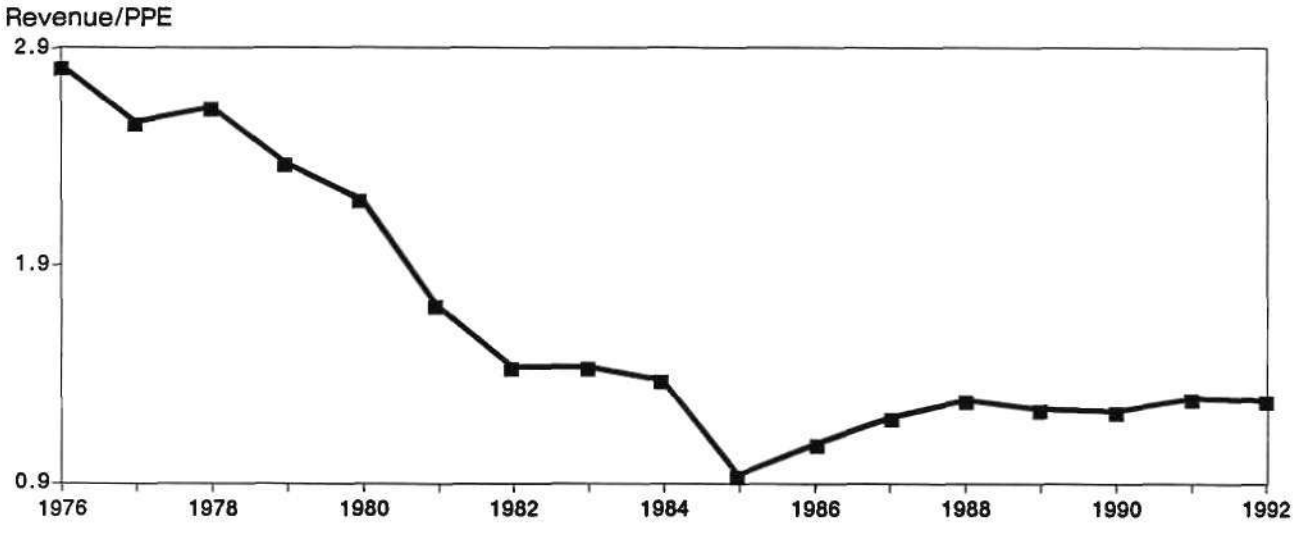
Thus, although we are in the midst of a boom, growth in capital spending will be slower than it has been in the past. It will also be steadier because the semiconductor industry itself is becoming more mature, which results in a less uneven growth. Therefore, capacity additions will be better planned than in the past.

Dataquest consequently does not expect skyrocketing capital spending growth such as that which occurred in 1984. We also do not expect the devastating descents that occurred in 1985 and 1986. The peaks may not be as high, but the ride will be smoother and more sustainable.

Capital Spending Forecast

Figure 3

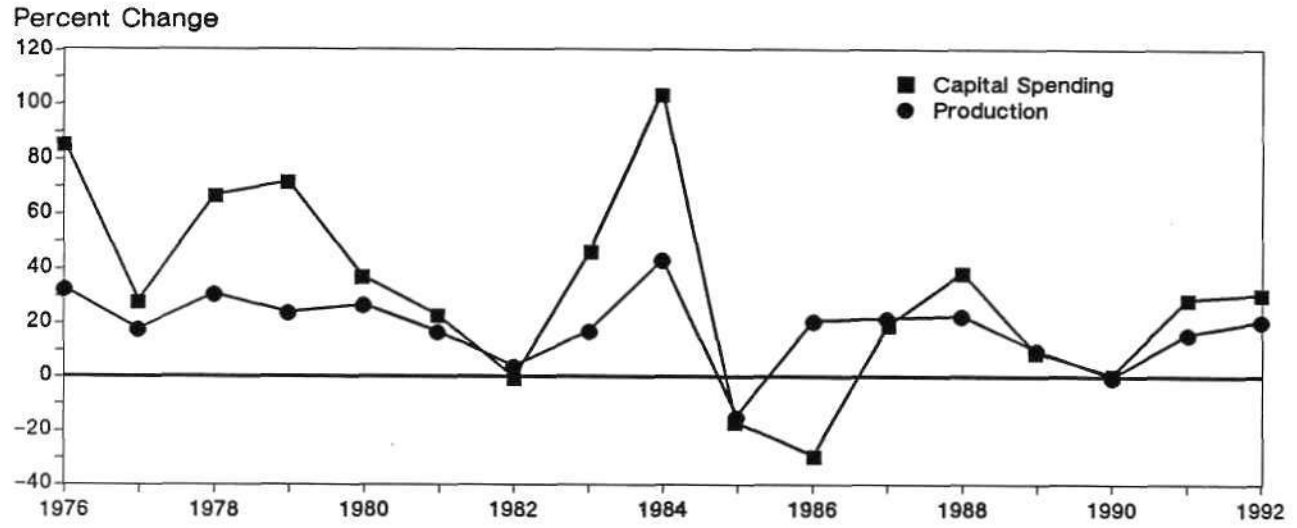
The Productivity of Capital



Source: Dataquest
August 1988

Figure 4

Percent Change in Capital Spending Production



Source: Dataquest
August 1988

Capital Spending

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Capital Spending

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Capital Spending

INTRODUCTION

Aggregate capital spending plans of semiconductor manufacturers are vital information for strategic and tactical planning in the semiconductor equipment industry. Knowledge of manufacturers' current spending plans can help in identifying sales leads and directing existing resources to the best markets. Accurate forecasts of capital spending help equipment vendors deploy their capital and manufacturing resources in order to have their products in the right markets at the right time.

This section provides the results of Dataquest's latest survey of the major merchant manufacturers regarding their planned spending in 1987. This section also provides a regional forecast of capital spending, including captives, for 1987 through 1992.

METHODOLOGY

To forecast capital spending, Dataquest uses an econometric model in which capital spending is a function of regional production. Using this model, we have obtained a regression coefficient of more than 90 percent. Production is a measure of regional front-end activity.

Regional production, which is different from regional consumption, is an estimate of the final market value of devices fabricated within a region. A device is classified as produced within a region if it is fabricated within that region, even though it may be tested, assembled and shipped from another region. (For a more complete discussion of production and consumption by region, the reader should refer to the service section entitled "Production" in this binder.)

SUMMARY

1986: Market Crash

Figure 1 summarizes the 1986 market for capital spending. On a worldwide basis, capital spending declined 27 percent from 1985's level of $7.2 billion. However, not all regions experienced declines in 1986. European capital spending grew 12 percent in 1986, from $600 million in 1985 to $670 million in 1986. ROW spending grew at a very healthy rate of 25 percent, from $220 million in 1985 to $275 million in 1986. Unfortunately, these two markets represented only 18 percent of the worldwide market for capital spending.

Spending by merchants in North America declined a full 28 percent, from $2.1 billion in 1985 to $1.6 billion in 1986. Captive capital spending was flat from 1985 to 1986 at $1.0 billion. However, it was in Japan that capital spending fell the most. Measured in dollars, the decline in Japan was severe—47 percent, from $3.2 billion in 1985 to $1.8 billion in 1986. Measured in yen, the decline was a cliff—63 percent from 1985 to 1986.

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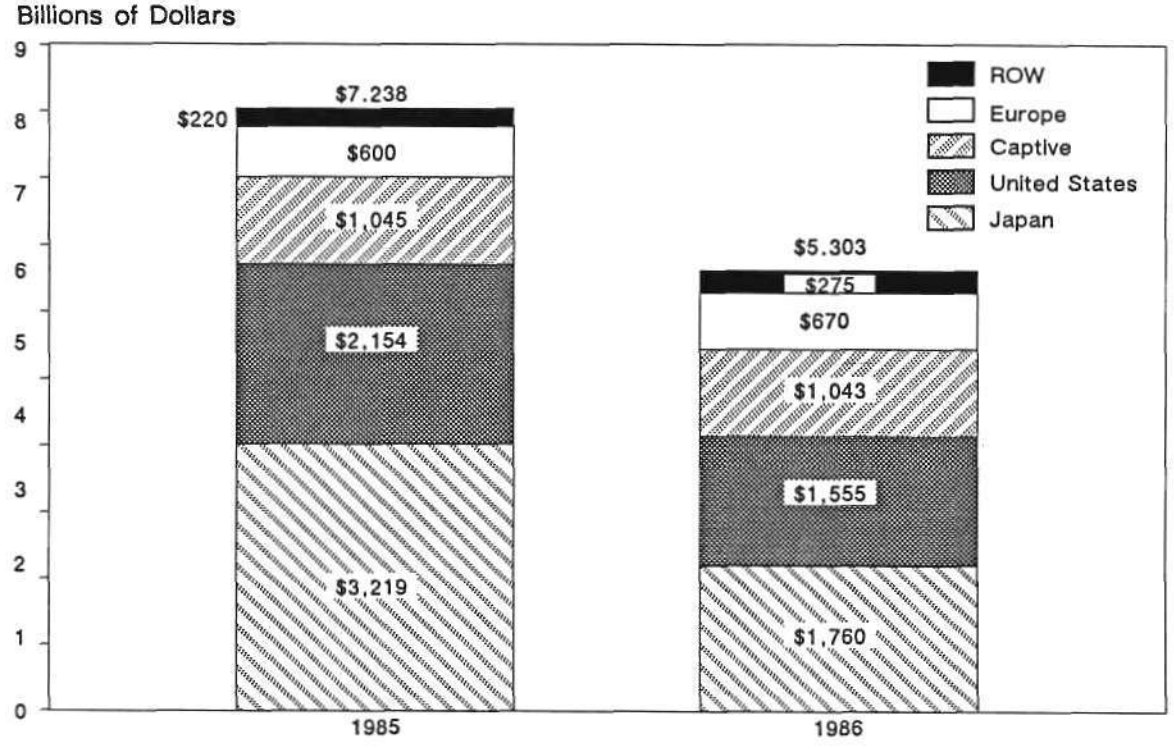
Capital Spending

Figure 1

Market Crash
Capital Spending
1985–1986



Source: Dataquest
December 1987

1987: The Recovery

In Dataquest's opinion, 1987 was a year of recovery. We anticipate that spending for the year will be up 10 percent worldwide. Capital spending in Japan, however, for the year as a whole will decline 4 percent, from $1.8 billion in 1986 to $1.7 billion in 1987. Measured in yen, the decline for the year as a whole will be 12 percent. However, our analysts in Japan report that orders in Japan have increased in the last months of 1987. We therefore look forward to an increase in the 1988 Japanese market of 26 percent in both yen and dollars. (Our dollar estimates for Japanese spending are based on a 1987 average exchange rate of 154 yen to the dollar. We do not forecast exchange rates, although the yen will probably be lower next year.)

Capital Spending

Table 1 presents a regional breakdown of capital spending in 1986 and 1987.

Table 1

1987 Regional Capital Spending

Region	1986	1987	Percent Change
Captives	$1,043	$1,104	6.0%
European	670	823	23.0%
Japan	1,760	1,683	(4.0%)
North America	1,555	1,908	23.0%
ROW	275	406	48.0%
Total	$5,303	$5,924	11.7%

Source: Dataquest
December 1987

1988: Before and After the October 1987 Crash

After the October 1987 stock market crash, Dataquest surveyed major semiconductor manufacturers to determine what effects the crash would have on the semiconductor industry. There has been as yet no sign of a decrease in orders as a result of the crash, and capital spending plans are reported as unaffected. Indeed, some companies, such as Intel, have reported that their capital spending plans have increased. We continue to forecast growth in capital spending. However, with the possibility of greater economic instability looming, we are less certain about the immediate future than we were before the crash.

Dun & Bradstreet has lowered its projections for the U.S economic growth in 1988, from 3.3 percent to 2.5 percent. As we have already noted, some potential exists for generally slower economic growth in 1988 to slow down the growth of the semiconductor industry and, hence, capital spending in 1988. This need not be bad news.

In the past, semiconductor companies have swung the equipment companies around in "boom to bust" scenarios; the impending slowdown could ameliorate this volatility. We anticipate less of a mismatch between supply and demand for semiconductors; orders, though perhaps slower than they would have been, will remain real. There will be less "overheating," both in the general economy and in the semiconductor industry. With less overheating, there will be less of a likelihood of sliding into a recession, which can only be good news for an equipment industry just climbing out of the last industry recession.

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Capital Spending

Because of this uncertainty surrounding 1988, we are publishing two forecasts for 1988: an optimistic forecast generated on assumptions made prior to October 1987, and a downside 1988 forecast generated on assumptions made after October 1987. It should be noted that both forecasts foresee growth in 1988.

Both the optimistic and downside forecasts for 1988 are shown in Tables 2 and 3.

We will be watching events very closely in the general economy and in the semiconductor industry to see if the October crash will have any implications beyond 1988. If our downside scenario unfolds, we will revise our 1989 and beyond projections. However, because both manufacturers and end-user markets report no signs of a downturn, we will stay with our optimistic forecast for now.

Table 2

Two Views of Production in 1988

	Optimistic Outlook	Downside Outlook
U.S. Production	$18,057	$17,139
% Change (1986-1987)	21%	15%
Japanese Production	22,147	20,934
% Change (1986-1987)	23%	16%
European Production	5,729	5,340
% Change (1986-1987)	27%	18%
ROW Production	1,592	1,510
% Change (1986-1987)	66%	57%
Captive Production	7,199	6,730
% Change (1986-1987)	18%	11%
Worldwide Production	$54,723	$51,652
% Change (1986-1987)	23%	16%

Source: Dataquest
December 1987

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Capital Spending

Table 3

Two Views of Capital Spending in 1988

	Optimistic Outlook	Downside Outlook
U.S. Capital Spending	$ 2,650	$ 2,279
% Change (1986-1987)	39%	19%
Japan Capital Spending	2,119	2,119
% Change (1986-1987)	26%	26%
Europe Capital Spending	1,037	892
% Change (1986-1987)	26%	8%
ROW Capital Spending	606	606
% Change (1986-1987)	49%	49%
Captives Capital Spending	1,309	1,225
% Change (1986-1987)	18%	11%
Worldwide Capital Spending	$ 7,722	$ 7,121
% Change (1986-1987)	30%	20%

Source: Dataquest
December 1987

1989 and Beyond

If the economy grows as we had originally projected in 1988 (3.3 percent), we expect to see a pause in capital spending growth in 1989. This expectation is due to our belief that semiconductor consumption will be flat in 1989, reflecting a general flatness in the economy.

After 1989, however, we expect renewed growth both in semiconductor production and in capital spending (see Table 4). Japanese capital spending after 1989 will be very strong because of Japan's need to replace the large volume of equipment brought on-stream in 1984 and 1986 (see SEMS newsletter, 1987-14, "Capital Spending Forecast: Slower but Steadier Growth," for a detailed analysis of the underlying causes of the strong capital spending in Japan after 1989).

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Capital Spending

Table 4

Estimated Capital Spending and Production

	1983	1984	1985	1986	1987
Japan Production	$7,928	$11,952	$10,689	$15,031	$18,069
Percent Change	42%	51%	(11%)	41%	20%
Capital Spending	$1,698	$ 3,671	$ 3,219	$ 1,760	$ 1,682
Percent Change	84%	116%	(12%)	(45%)	(4%)
Capital Spending/ Production	21%	31%	30%	12%	9%
North America Production	$9,419	$13,925	$10,964	$11,857	$14,870
Percent Change	24%	48%	(21%)	8%	25%
Capital Spending	$1,557	$ 3,272	$ 2,154	$1,555	$1,908
Percent Change	31%	110%	(34%)	(28%)	23%
Capital Spending/ Production	16%	23%	20%	13%	13%
European Production	$2,144	$ 2,972	$ 2,759	$ 3,498	$ 4,519
Percent Change	10%	39%	(7%)	27%	29%
Capital Spending	$ 350	$ 630	$ 600	$ 670	$ 823
Percent Change	11%	80%	(5%)	12%	23%
Capital Spending/ Production	16%	21%	22%	19%	18%
ROW Production	$ 174	$ 238	$ 411	$ 623	$ 961
Percent Change	78%	36%	73%	52%	54%
Capital Spending	$ 91	$ 201	$ 220	$ 275	$ 406
Percent Change	102%	121%	10%	25%	48%
Capital Spending/ Production	52%	84%	54%	44%	42%
Captive	$3,577	$ 4,377	$ 4,875	$ 5,422	$ 6,088
Percent Change	12%	22%	11%	11%	12%
Capital Spending	$ 542	$ 965	$ 1,045	$ 1,043	$ 1,104
Percent Change	8%	78%	8%	0%	6%
Capital Spending/ Production	17%	25%	24%	20%	20%

(Continued)

Capital Spending

Table 4 (Continued)

Estimated Capital Spending and Production

	1983	1984	1985	1986	1987
North America	$1,452	$3,051	$2,154	$1,555	$1,908
Japan	1,698	3,671	3,219	1,760	1,682
Europe	350	630	600	670	823
ROW	91	201	220	275	406
Captive	542	965	1,045	1,043	1,104
Worldwide Capital Spending	$4,238	$8,738	$7,238	$5,303	$5,924
Percent Change	42.8%	106.2%	(17.2%)	(26.7%)	11.7%
North America	$ 9,419	$13,925	$10,964	$11,857	$14,870
Japan	7,928	11,952	10,689	15,031	18,069
Europe	2,144	2,972	2,759	3,498	4,519
ROW	174	238	411	623	961
Captive	$ 3,577	$ 4,377	$ 4,875	$ 5,422	$ 6,088
Worldwide Production	$23,242	$33,464	$29,698	$36,431	$44,508
Percent Change	25.9%	44.0%	(11.3%)	22.7%	22.2%
Capital Spending/ Production	18.2%	26.1%	24.4%	14.6%	13.3%

(Continued)

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Capital Spending

Table 4 (Continued)

Estimated Capital Spending and Production

	1988	1989	1990	1991	1992	CAGR (1987-1992)
Japan Production	$22,147	$21,343	$23,582	$26,583	$30,688	11%
Percent Change	23%	(4%)	10%	13%	15%	
Capital Spending	$ 2,119	$ 2,437	$ 3,655	$ 5,118	$ 6,912	33%
Percent Change	26%	15%	50%	40%	35%	
Capital Spending/ Production	10%	11%	16%	19%	23%	
North America Production	$18,057	$18,222	$20,926	$24,053	$28,292	14%
Percent Change	21%	1%	15%	15%	18%	
Capital Spending	$ 2,650	$ 2,498	$ 2,918	$ 3,482	$ 4,326	18%
Percent Change	39%	(6%)	17%	19%	24%	
Capital Spending/ Production	15%	14%	14%	14%	15%	
European Production	$ 5,729	$ 5,727	$ 6,591	$ 8,079	$10,232	18%
Percent Change	27%	0%	15%	23%	27%	
Capital Spending	$ 1,037	$ 1,063	$ 1,220	$ 1,468	$ 1,829	17%
Percent Change	26%	3%	15%	20%	25%	
Capital Spending/ Production	18%	19%	19%	18%	18%	
ROW Production	$ 1,592	$ 2,047	$ 2,692	$ 4,413	$ 6,566	47%
Percent Change	66%	29%	32%	64%	49%	
Capital Spending	$ 606	$ 648	$ 810	$ 969	$ 1,135	23%
Percent Change	49%	7%	25%	20%	17%	
Capital Spending/ Production	38%	32%	30%	22%	17%	
Captive	$ 7,199	$ 7,992	$ 9,074	$10,361	$11,999	15%
Percent Change	18%	11%	14%	14%	16%	
Capital Spending	$ 1,309	$ 1,244	$ 1,294	$ 1,527	$ 1,920	12%
Percent Change	19%	(5%)	4%	18%	26%	
Capital Spending/ Production	20%	16%	16%	15%	16%	

(Continued)

Capital Spending

Table 4 (Continued)

Estimated Capital Spending and Production

	1988	1989	1990	1991	1992	CAGR (1987-1992)
North America	$2,650	$2,498	$2,918	$ 3,482	$ 4,326	18%
Japan	2,119	2,437	3,655	5,118	6,912	33%
Europe	1,037	1,063	1,220	1,468	1,829	17%
ROW	606	648	810	969	1,135	23%
Captive	1,309	1,244	1,294	1,527	1,920	12%
Worldwide Capital Spending	$7,722	$7,889	$9,897	$12,564	$16,122	22%
Percent Change	30.4%	2.2%	25.4%	26.9%	28.3%	
North America	$18,057	$18,222	$20,926	$24,053	$28,292	14%
Japan	22,147	21,343	23,582	26,583	30,688	11%
Europe	5,729	5,727	6,591	8,079	10,232	18%
ROW	1,592	2,047	2,692	4,413	6,566	47%
Captive	7,199	7,992	9,074	10,361	11,999	15%
Worldwide Production	$54,723	$55,332	$62,865	$73,488	$87,778	15%
Percent Change	23.0%	1.1%	13.6%	16.9%	19.4%	
Capital Spending/ Production	14.1%	14.3%	15.7%	17.1%	18.4%	

Source: Dataquest
December 1987

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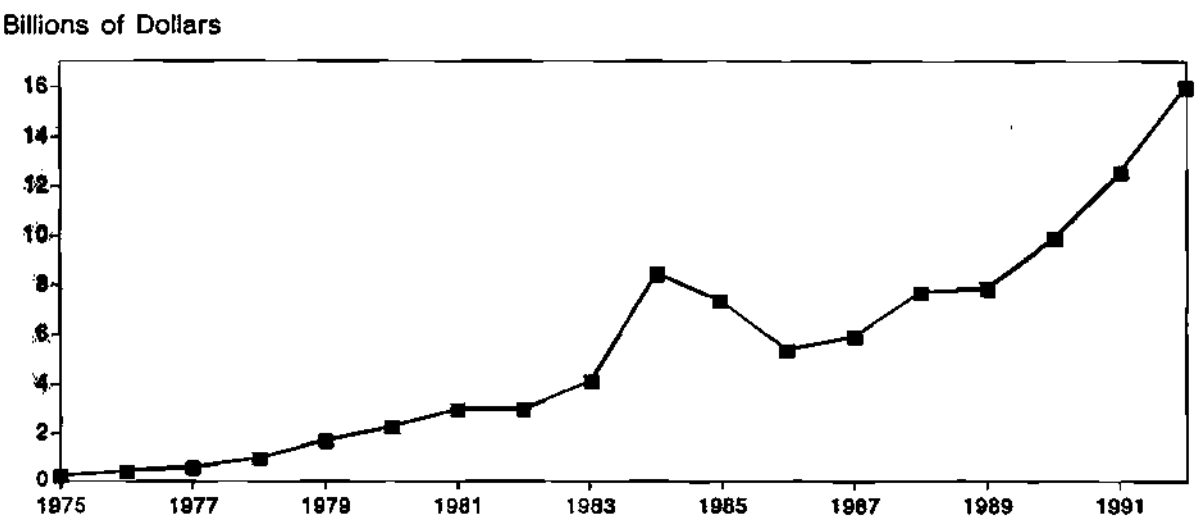
Capital Spending

An examination of Figure 2, which shows the growth of capital spending from 1975 through 1992, suggests that 1986 is a logical point from which to view long-term compound annual growth rates (CAGRs). Table 5 compares CAGRs of both capital spending and production. Capital spending grew at a slower rate from 1980 through 1986 compared with 1975 through 1986.

Figure 2

Estimated Worldwide Capital Spending



Source: Dataquest December 1987

Capital Spending

Table 5

Production and Capital Spending (CAGRs)

	CAGR 1975-1986	CAGR 1980-1986
Worldwide Capital Spending	32%	14%
Worldwide Production	21%	17%

Source: Dataquest
December 1987

PRODUCTION AND CAPITAL SPENDING

We believe that the industry will not exceed its 1984 spending level until 1990. This interval represents a very long valley between peaks and is due to the maturity of the semiconductor industry and to the increasing productivity of capital.

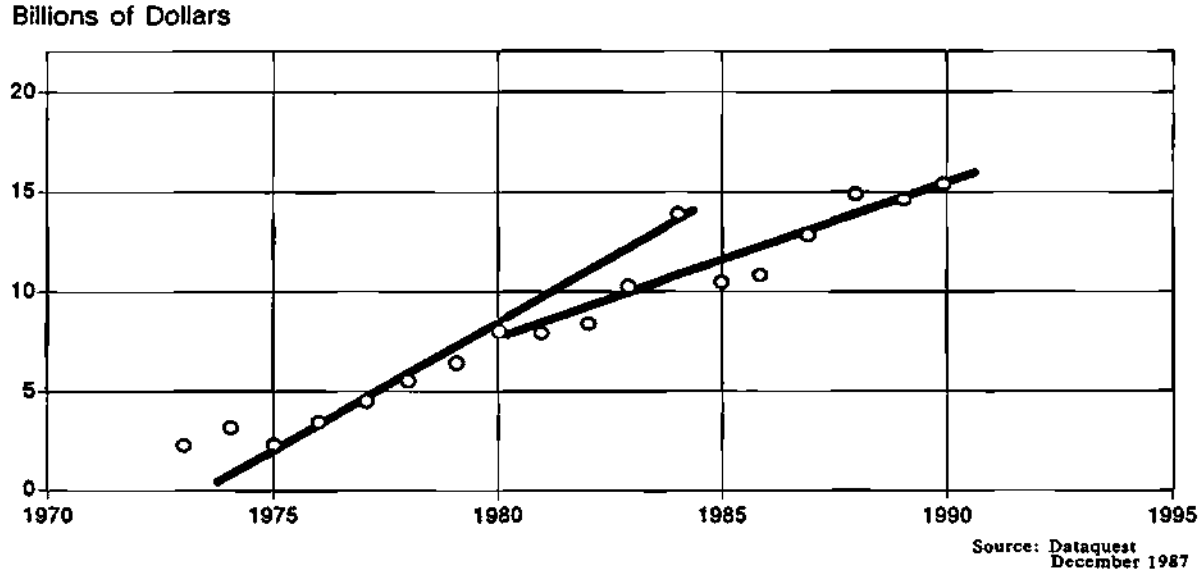
Production is one of the basic forces that shape capital spending, and capital spending is a derived demand. If the end users of semiconductors do not have a strong demand for their products, then there will be a weak demand for semiconductors and, consequently, for capital equipment. Although we expect production to grow by 23 percent in 1987 and 1988 (under our optimistic scenario), we believe that the long-term growth of the semiconductor industry has slowed.

Historically, semiconductor production has grown at an 18 percent CAGR. Dataquest now expects semiconductor consumption to grow at a slower rate of 13 to 15 percent (see Figure 3). This new, lower, long-term growth rate is due to the absence of a new "hoola-hoop" such as the PC, to drive the industry as it did from 1982 through 1984. This growth rate is also due to the success of the industry. Semiconductors are now found throughout the economy; they therefore will increasingly be influenced by the secular trends of the economy.

Capital Spending

Figure 3

Estimated North American Semiconductor Consumption



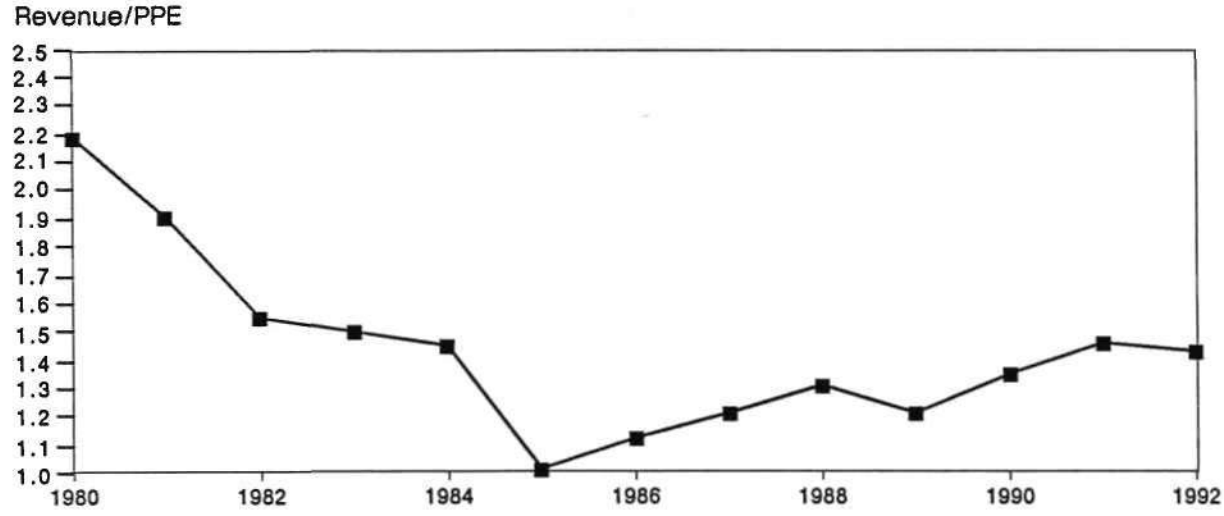
The second reason for the slowdown in the capital spending CAGR is that of increasing productivity of capital. Capital productivity is the amount of revenue that is generated with a given installed base of property, plant, and equipment (PPE). Historically, this ratio has declined (see Figure 4). However, we believe for several reasons that capital productivity has begun to rise. Computer integrated manufacturing (CIM) will allow manufacturers to schedule many different product mixes and maintain line balance while increasing equipment utilization. We estimate that equipment utilization is presently in the neighborhood of 40 percent. We also anticipate that manufacturers will increase their yields. Yields will increase because automation will remove people from clean rooms. Yields will also increase because of lower particulate from semiconductor equipment and materials.

Figure 5 shows the effects of both the slowdown of semiconductor production and of increasing capital productivity. For the first period, from 1975 through 1986, worldwide capital spending grew at a CAGR of 32 percent, and worldwide semiconductor production, including captives, grew at a CAGR of 21 percent. From 1980 through 1986, however, the CAGRs of both capital spending and production had fallen, but the CAGR of capital spending was below that of production. We expect this trend to continue. There will be growth, but it will be slower than it has been in the past.

Capital Spending

Figure 4

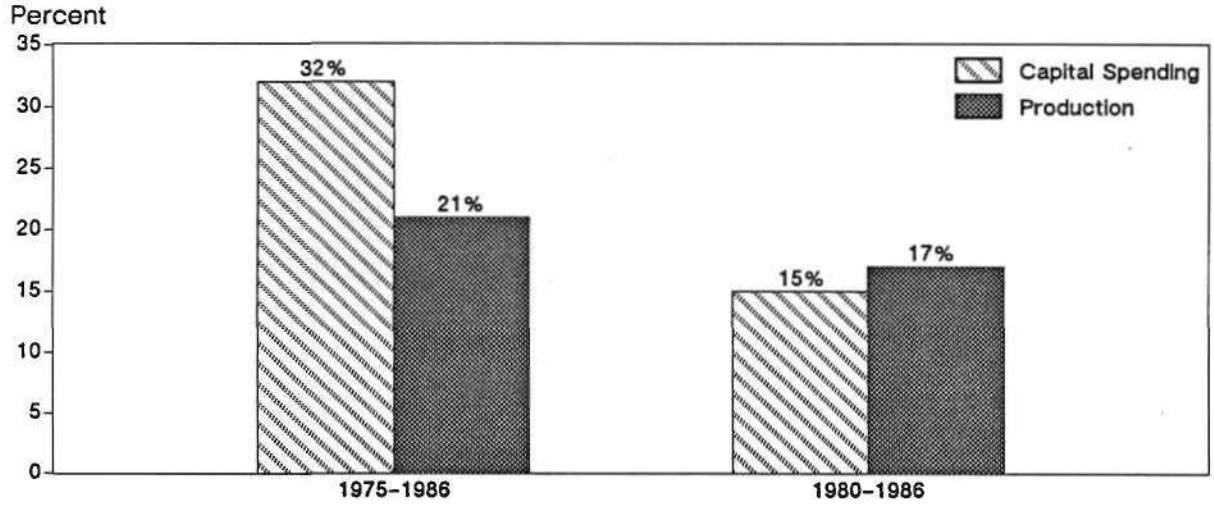
Estimated Revenue/PPE
Worldwide Installed Base



Source: Dataquest
December 1987

Figure 5

Declining CAGR
Capital Spending versus Production



Source: Dataquest
December 1987

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Capital Spending

EUROPE AND ROW

European capital spending and ROW capital spending were welcome bright spots in an otherwise gloomy 1986 capital spending picture. Spending in Europe increased 12 percent, from $600 million in 1985 to $670 million in 1986. The rest of the world (ROW) also increased its capital spending, from $220 million in 1985 to $275 million in 1986, an increase of 25 percent.

European companies and their governments have stated that they are committed to expanding their roles in the semiconductor industry. European capital spending is expected to reach $1.8 billion by 1992, growing at a CAGR of 18 percent between 1986 and 1992.

We also anticipate that the European governments will continue to offer various incentives for semiconductor manufacturers to locate in their countries. In addition to tax incentives, low-interest loans for capital equipment purchases could be offered.

ROW capital spending is expected to grow at a CAGR of 27 percent between 1986 and 1992, reaching $1.1 billion by 1992. This is a remarkable growth rate and certainly represents a real opportunity for capital equipment manufacturers.

CAPTIVES

Captive semiconductor manufacturers include such companies as IBM, AT&T, Delco, Honeywell, and others. The difference between a captive manufacturer and a merchant manufacturer is that a captive produces semiconductors for its own internal use. Captive manufacturers do not sell their devices on the merchant market.

Captive manufacturers are a major market for semiconductor equipment. Captives, as a percent of North American merchant capital spending, has varied from as low as 32 percent to as high as 56 percent in recent years. Generally, captive capital spending is more stable than capital spending by merchant manufacturers. Captives are more stable because they produce for internal consumption rather than for a volatile merchant market.

We believe that captive capital spending was basically flat in 1986. We expect spending by the captives to increase 6 percent in 1987 and to grow to $1.9 billion in 1992.

NORTH AMERICAN MERCHANT CAPITAL SPENDING

Dataquest surveys the major North American semiconductor manufacturers several times a year to track their capital spending plans. We have noted a strengthening of optimism as the year has progressed. This optimism has not waned since the October crash.

Capital Spending

The results of our survey indicate an increase of capital spending in North America of 10 percent, from $1,555 million in 1986 to $1,908 million in 1987. Tables 6 and 7 provide a summary of the history of capital spending in North America by company and the change in spending from 1986 to 1987.

Table 6

North American Capital Spending
1975–1987

Company	1975	1976	1977	1978	1979	1980	1981
	Domestic Company Spending						
AMD	$ 1	$ 6	$ 10	$ 20	$ 39	$ 49	$ 58
Analog Devices	2	4	7	12	10	19	16
Fairchild	20	36	15	23	58	83	140
General Electric							
General Instruments							
Harris						45	45
IDT							
Intel	11	32	46	104	97	156	157
LSI Logic							
Thomson-Mostek	3	10	24	19	42	85	98
MMI					4	6	20
Motorola	21	33	43	72	159	177	184
Micron Technology							
National Semiconductor	17	26	31	51	84	116	105
Philips-Signetics	4	10	19				
Texas Instruments	35	62	88	122	251	300	145
Others	56	94	105	177	329	312	265
Subtotal	$170	$312	$388	$599	$1,073	$1,347	$1,233
	Non-U.S.-Owned Company Spending in United States						
NEC							
Philips-Signetics				$ 40	$ 50	$ 90	$ 115
Siemens							
Thomson-Mostek							
Subtotal				$ 40	$ 50	$ 90	$ 115
Total	$170	$312	$388	$639	$1,123	$1,437	$1,348
Percent Change		84%	24%	65%	76%	28%	(6%)

(Continued)

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Capital Spending

Table 6 (Continued)

North American Capital Spending
1975–1987

Company	1982	1983	1984	1985	1986	1987
	Domestic Company Spending					
AMD	$ 67	$ 111	$ 237	$ 172	$ 55	$ 111
Analog Devices	19	24	58	62	37	49
Fairchild	156	125	195	135	135	45
General Electric		64	107	81	50	50
General Instruments			9	12	8	12
Harris	35	25	41	58	45	29
IDT		2	4	25	18	18
Intel	138	146	388	214	155	300
LSI Logic	6	30	82	40	71	135
Thomson-Mostek	47	78	123			
MMI	25	25	52	49		
Motorola	160	174	412	330	250	338
Micron Technology	5	29	58	32	11	14
National Semiconductor	82	120	300	184	88	112
Philips-Signetics						
Texas Instruments	140	232	472	281	213	240
Others	252	314	602	391	319	331
Subtotal	$1,131	$1,499	$3,139	$2,065	$1,456	$1,783
	Non-U.S.-Owned Company Spending in United States					
NEC					$ 10	$ 12
Philips-Signetics	$ 55	$ 58	$ 133	$ 50	$ 60	90
Siemens					$ 20	$ 15
Thomson-Mostek				$ 39	$ 9	$ 8
Subtotal	$ 55	$ 58	$ 133	$ 89	$ 99	$ 125
Total	$1,186	$1,557	$3,272	$2,154	$1,555	$1,908
Percent Change	(12%)	31%	110%	(34%)	(28%)	23%

Source: Dataquest
December 1987

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Capital Spending

Table 7

Percent Change in U.S. Capital Spending
1986 and 1987

Company	1986	1987	Percent Change
AMD	$ 55	$ 111	101%
Analog Devices	37	49	33%
Fairchild	135	45	(67%)
General Instruments	8	12	50%
General Electric	50	50	0
Harris	45	29	(36%)
IDT	18	18	0
Intel	155	300	94%
LSI Logic	71	135	90%
Micron Technology	11	14	22%
Motorola	250	338	35%
National Semiconductor	88	112	28%
NEC	10	12	20%
Philips-Signetics	60	90	50%
Siemens	20	15	(25%)
Texas Instruments	213	240	13%
Thomson-Mostek	9	8	(11%)
Others	319	331	4%
Total	$1,555	$1,908	23%

Source: Dataquest
December 1987

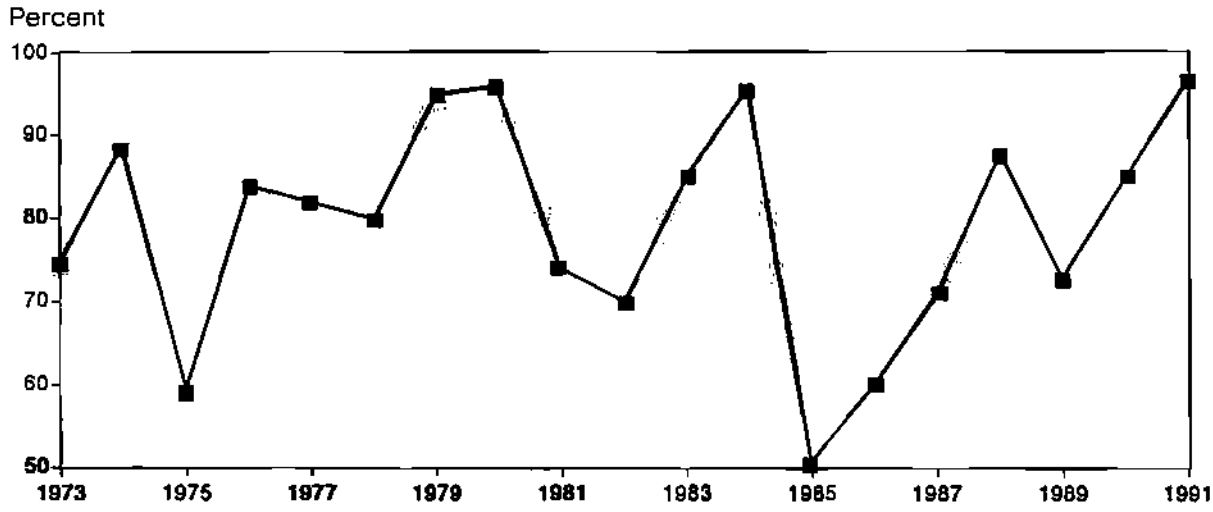
In 1985, capacity utilization in North America fell to an all-time low of 51 percent. However, it rose to 60 percent in 1986, and we expect it to rise to 71 percent in 1987 (see Figure 6). Due to these relatively low rates of utilization, we do not expect to see new fab activity to be at a very high rate. Our survey results indicate that only 12 percent, or $229 million of the $1,908 million to be spent in 1987, will be for new property and plant. Approximately 88 percent, or $1,679 million, will be spent on front-end and test and assembly equipment in 1987.

Spending in 1988 (under our optimistic scenario) will grow by 34 percent over 1987's level to $2,650 million. For 1989, we expect capital spending to fall back by 6 percent to $2,498 million. After 1989, we expect three years of solid growth.

Capital Spending

Figure 6

North America Capacity Utilization



Source: Dataquest
December 1987

Expenditures by Companies

In contrast to 1986, according to our survey, most companies operating in North America planned to increase their capital spending in 1987. AMD reported that it might increase its spending by more than 100 percent, and Intel planned to increase its spending by 93 percent. Siemens probably planned to decrease its spending in 1987. Motorola planned to spend $338 million in 1987, more than any other company in North America. We estimate that both Texas Instruments and Intel spent more than $200 million in 1987.

Individual company capital spending for the period 1975 through 1987 is given in Table 6.

In addition to discussing capital spending plans for each of the major U.S. merchants, we show semiconductor capital spending as a percent of company semiconductor revenue. On the same graph, for comparative purposes, we also show the North American industry-wide ratio.

Advanced Micro Devices (AMD)

Discussion of AMD's capital spending does not yet include spending done or planned by Monolithic Memories, which recently merged with AMD.

Capital Spending

The capital-spending-to-revenue ratio of AMD has generally exceeded the industry average every year since 1975 (see Figure 7). Until 1986, it rose every year but three. The ratio rose from approximately 5 percent in 1975 to about 28 percent in 1985. However, in 1986, AMD's capital spending ratio fell along with the industry average, even falling below the industry average.

In terms of absolute dollars, AMD's capital expenditures increased each year until the 1985 downturn. In 1986, AMD's expenditures were their lowest since 1980. We estimate that AMD increased its 1987 spending by 117 percent, to $137.5 million, in order to increase capacity.

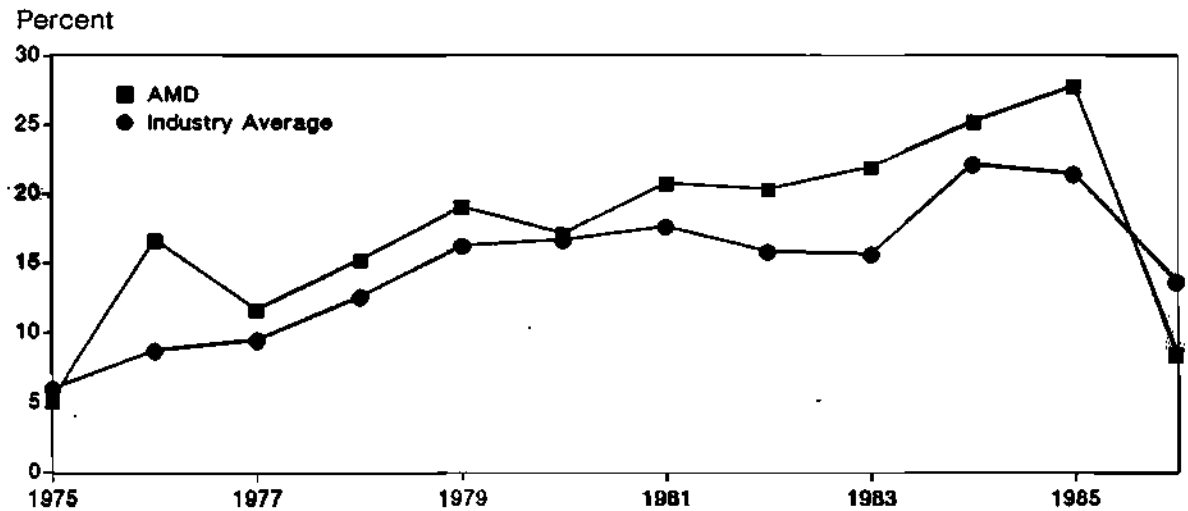
The focus of this spending was on equipment; no more than 5 percent was for new property or plant. Most of AMD's spending on plant and property was for its Bankok, Thailand, test and assembly facility.

We expect AMD to continue to revamp or close its older lines. Fab 5 in Austin, for example, is now closed. Fab 10 in Austin is also closed and may be refurbished to 8-inch capability, perhaps by 1988.

We believe that, in order for AMD to increase its capacity, etchers, steppers, and testers were high on its 1987 shopping list.

Figure 7

AMD versus Industry Average
Capital Spending/Production



Source: Dataquest December 1987

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Capital Spending

Analog Devices

Analog Devices' capital-spending-to-production ratio has always been above the industry average (see Figure 8). Indeed, in 1984 and 1985, its ratio exceeded the industry's average by 4.5 and 6.1 percentage points, respectively. The company's capital spending rose from $19 million in 1980 to a high of $62 million in 1985. We estimate its 1987 capital spending to be $49 million, up 32 percent from 1986's level of $37 million.

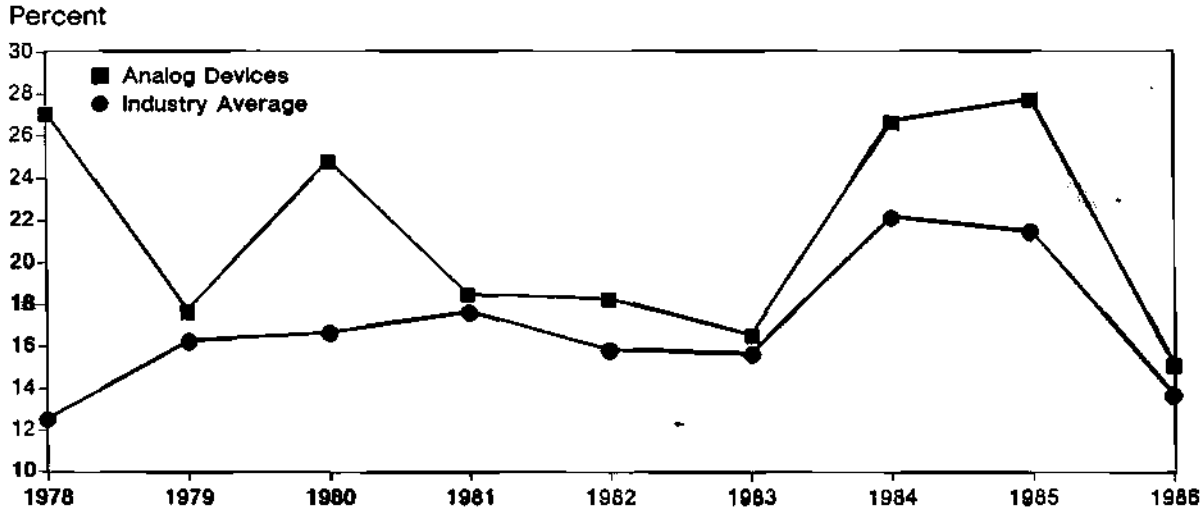
Analog's new 4-inch line in Wilmington, Massachusetts, is now making and shipping Word Slice digital signal processing products with a 1.5-micron CMOS process. This line is capable of being upgraded to 6-inch. At the same facility, Analog also began running products utilizing a BIMOS technology in 1986. In 1987, also at Wilmington, Analog was looking forward to running a bipolar line.

Analog's 4-inch CMOS line in Limerick, Ireland, is now in production.

Analog postponed completion of its new engineering and R&D facility in Wilmington, Delaware, for at least two quarters. Future spending plans for Analog include expanding back-end capacity.

Figure 8

Analog Devices versus Industry Average Capital Spending/Production



Source: Dataquest December 1987

Capital Spending

General Electric

General Electric's capital spending (which includes that of the recently acquired RCA as well as Intersil) as a percent of production has generally been below the industry average and has generally moved in parallel with the industry (see Figure 9).

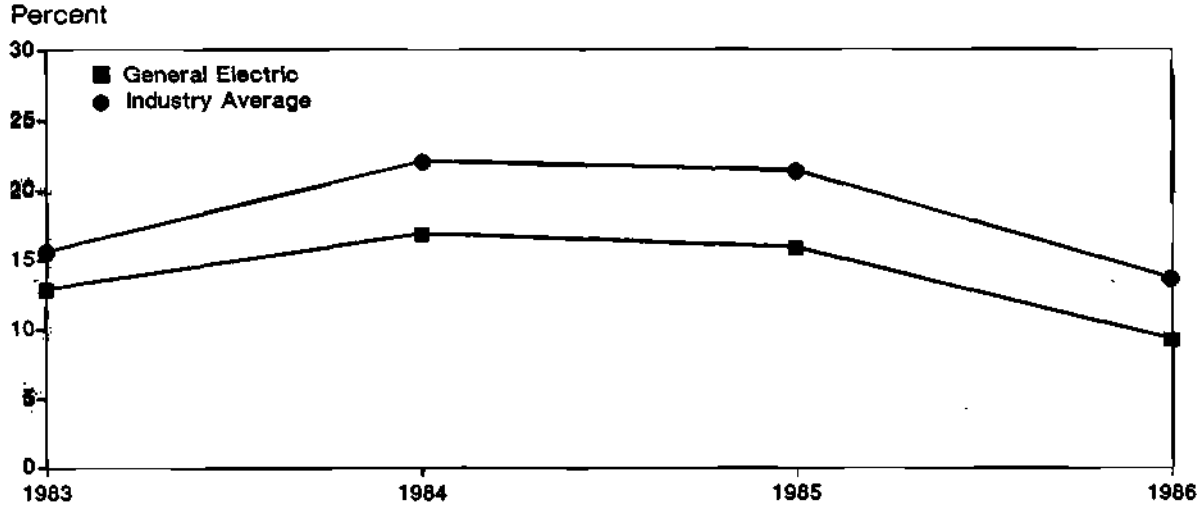
General Electric's combined capital spending reached its peak in 1984 at $107 million. Its level in 1986 was about $50 million, about one-half its 1984 level. We estimate that General Electric's 1987 spending level again reached $50 million, as the company continues to absorb RCA's semiconductor division. We believe that it is possible that General Electric will sell some of its RCA operations.

Most of General Electric's capital spending was directed toward equipment, with particular emphasis on 1.25-micron processing and test equipment.

1986 saw General Electric bring its 1.25-micron facility in Research Triangle Park, North Carolina, into production. Currently, its production line is running 4-inch wafers, but the company plans to run 5-inch wafers eventually.

Figure 9

General Electric versus Industry Average
Capital Spending/Production



Source: Dataquest
December 1987

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Capital Spending

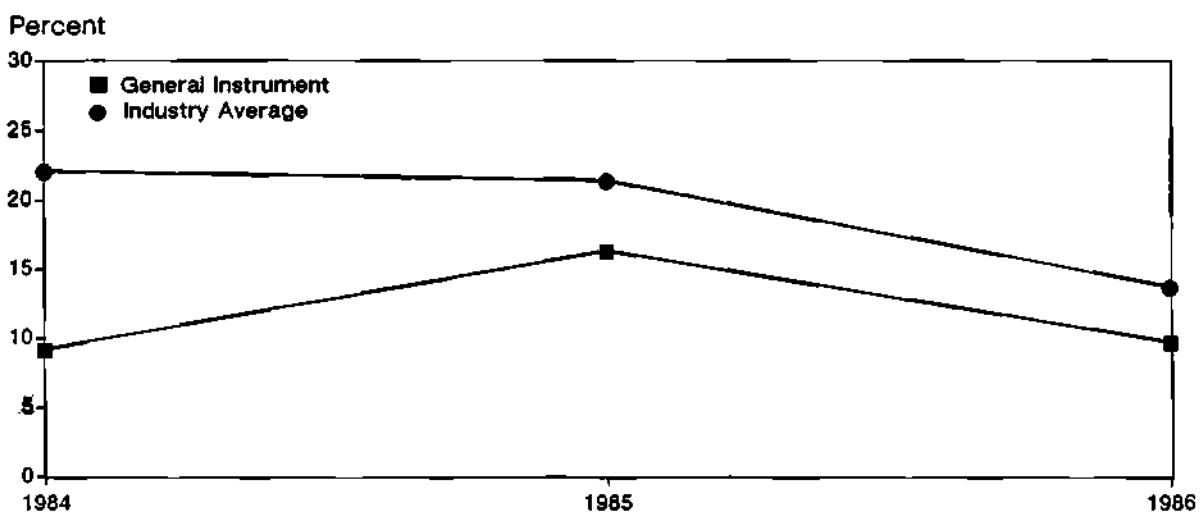
General Instruments

General Instruments' spending ratio has been below the industry average since 1984. It was less than half the industry average in 1984, rose to 16 percent in 1985, and then fell back to 9 percent in 1986 (see Figure 10).

General Instruments reports that it increased its capacity by 20 percent in 1987 through mechanization of its test and assembly operations. Most of its spending since 1984 has been for its front-end facility in Taiwan. The focus of its future plans will be on the mechanization of its fab in Taiwan.

Figure 10

General Instruments versus Industry Average
Capital Spending/Production



Source: Dataquest
December 1987

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Capital Spending

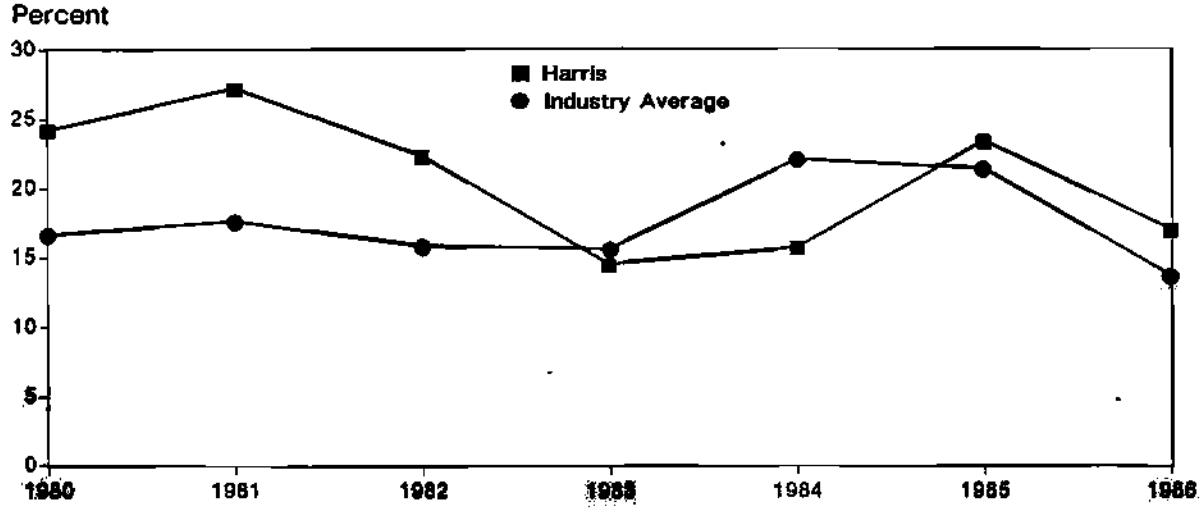
Harris

With the exception of 1983 and 1984, Harris' capital spending ratio has been above that of the industry (see Figure 11). In 1986, we estimate that Harris spent $40 million. Most of this spending was directed toward its new CMOS 5-inch facility, which is claimed to have a Class I clean room. We estimate that the company's 1987 spending declined to $30 million and was directed toward facilitizing and upgrading its existing fabs. Those fabs receiving upgrades include the Melbourne, Florida, Custom Integrated Circuits Division, which makes 1-micron, radiation-hardened CMOS devices for the Strategic Defense Initiative (SDI) program and the Semiconductor Products Division, also in Melbourne.

We believe that analog test equipment was also a focus of the company's spending.

Figure 11

Harris versus Industry Average Capital Spending/Production



Source: Dataquest December 1987

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Capital Spending

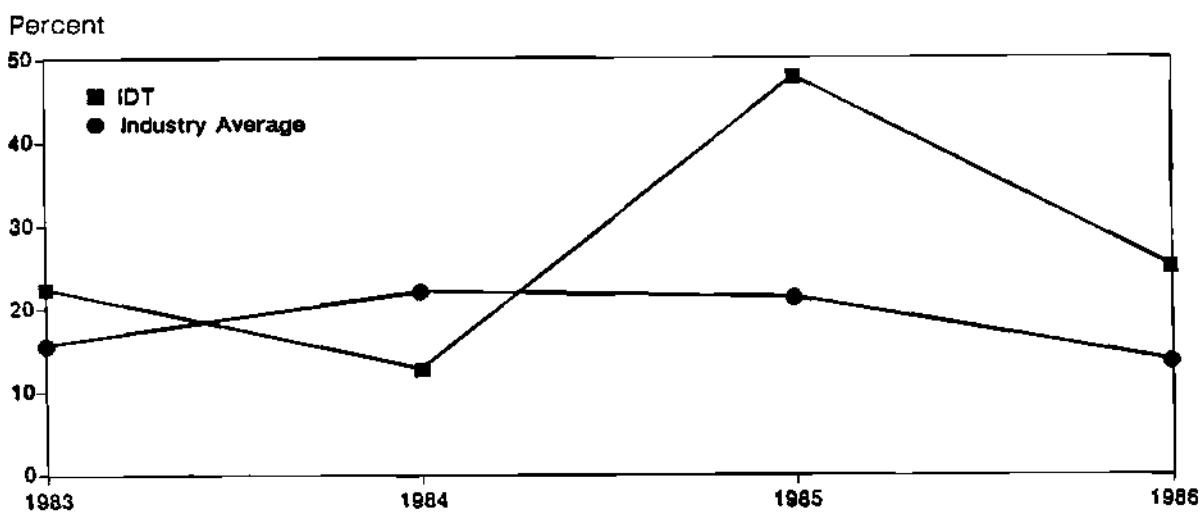
Integrated Device Technology (IDT)

IDT's capital spending ratio has generally been above the industry's average, as the company first opened its Santa Clara fab and, in 1985, its new Salinas fab (see Figure 12).

IDT is making improvements on both of its lines. Its spending plans for 1987 included new steppers and other front-end equipment to expand capacity at its 1-micron CMOS Salinas facility. IDT also planned to expand capacity in its 1.2-CMOS Santa Clara fab. New testers were also a focus of 1987 spending activity.

Figure 12

IDT versus Industry Average
Capital Spending/Production



Source: Dataquest December 1987

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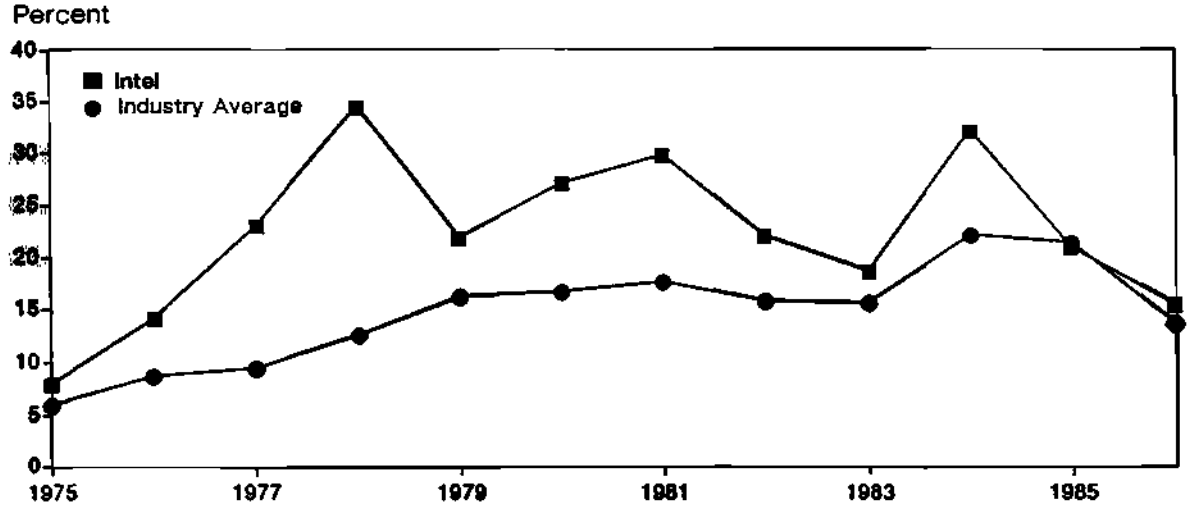
Capital Spending

Intel

Every year since 1975 (with the exception of 1985) Intel's capital-spending-to-revenue ratio has exceeded the industry average (see Figure 13).

Figure 13

Intel versus Industry Average Capital Spending/Production



Source: Dataquest December 1987

Intel's capital spending declined in 1985 and 1986, from $388 million in 1984 to $150 million in 1986. We estimate that the company's spending in 1987 increased by 93 percent, to $300 million. Intel increased its capital spending by such a large amount because of the improving economic climate and also because of its plans to expand capacity for its 80386 microprocessor.

Intel plans to bring its first module in Fab 9 in Albuquerque, New Mexico, on-line in early 1988. Fab 9 will have four production modules when fully operational. Its first module will run its 80386 microprocessor on 6-inch wafers that will feature 1-micron line geometries.

Intel recently announced that it plans to construct an advanced manufacturing development facility in Santa Clara, California. The company plans to spend $95 million on this facility, which it claims will be one of the most advanced development sites in the world. The facility will be 200,000 square feet and will be dedicated to the development of submicron manufacturing processes focused on nonvolatile memory devices and microcontrollers. It is scheduled for completion in April 1989. The facility will have 35,000 square feet of Class I clean room.

Capital Spending

Intel is going ahead with its plans to double its equipment utilization, and we expect it to invest significantly in automation to achieve this goal. We also believe that testers will be another focus of Intel's capital spending.

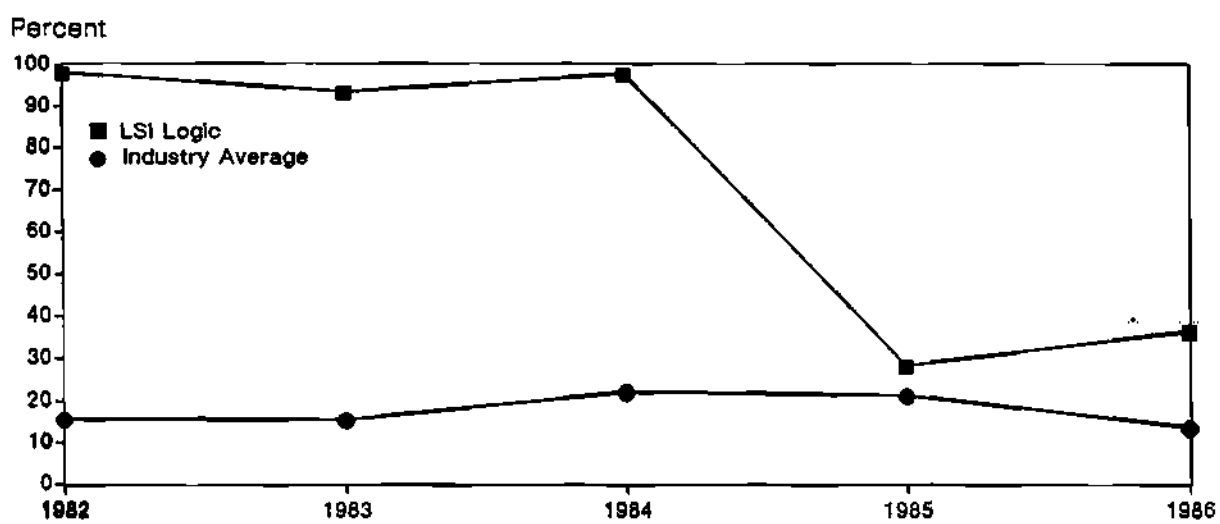
LSI Logic

LSI Logic, which was incorporated in 1980, has had a very high capital spending ratio, as it established fabs and installed equipment before its revenue stream became very large (see Figure 14). In 1985 and 1986, when their revenue had become substantial, LSI was still spending more than 30 percent of its revenue on capital spending.

In 1984, the focus of LSI's spending was on the establishment of its Santa Clara fab. In 1986, LSI began conversion from 4-inch wafers to 5-inch wafers and also began construction of Nihon Semiconductor in Japan. The year 1987 saw the completion of LSI's Nihon Semiconductor facility and the beginning of work on its new Braunshweig, West Germany, facility, which is expected to be completed in 1988.

Figure 14

LSI Logic versus Industry Average Capital Spending/Production



Source: Dataquest December 1987

Capital Spending

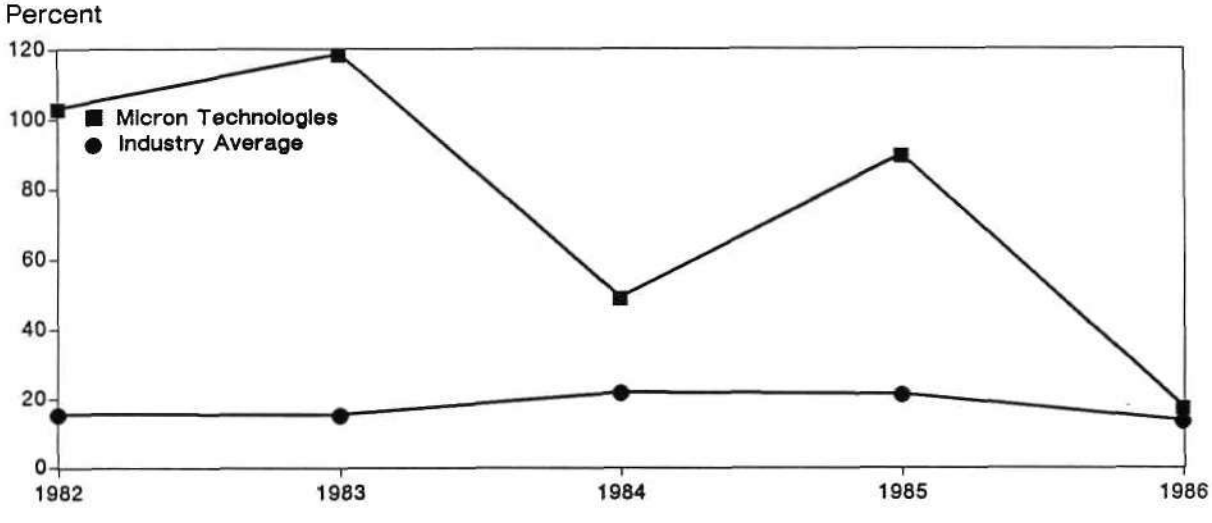
Micron Technology

Micron Technology's capital spending ratio has been above the industry average every year since 1982. For the period 1982 to 1985, the company's capital spending ratio has ranged from 50 percent of revenue to a high of 120 percent of revenue in 1982. Prior to 1985, these high ratios were due to the company's building capacity as a start-up (Micron was incorporated in 1978). Micron's spending ratio in 1985 was due to the downturn in revenue associated with the semiconductor industry's recession, especially in the DRAM market (see Figure 15).

Micron is currently remodeling its two fabs in Boise, Idaho, into one fab. This remodeling is expected to be completed in the first quarter of 1988. Micron is looking forward to expanding its capacity by 20 percent in 1988.

Figure 15

Micron Technology versus Industry Average Capital Spending/Production



Source: Dataquest December 1987

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Capital Spending

Motorola

Motorola's capital-spending-to-revenue ratio has been below that of the industry average since 1980 (see Figure 16).

We estimate that Motorola's capital spending for calendar 1987 was up 31 percent from 1986, from $250 million in 1986 to $338 million in 1987. At least 90 percent of the company's 1987 spending was for equipment.

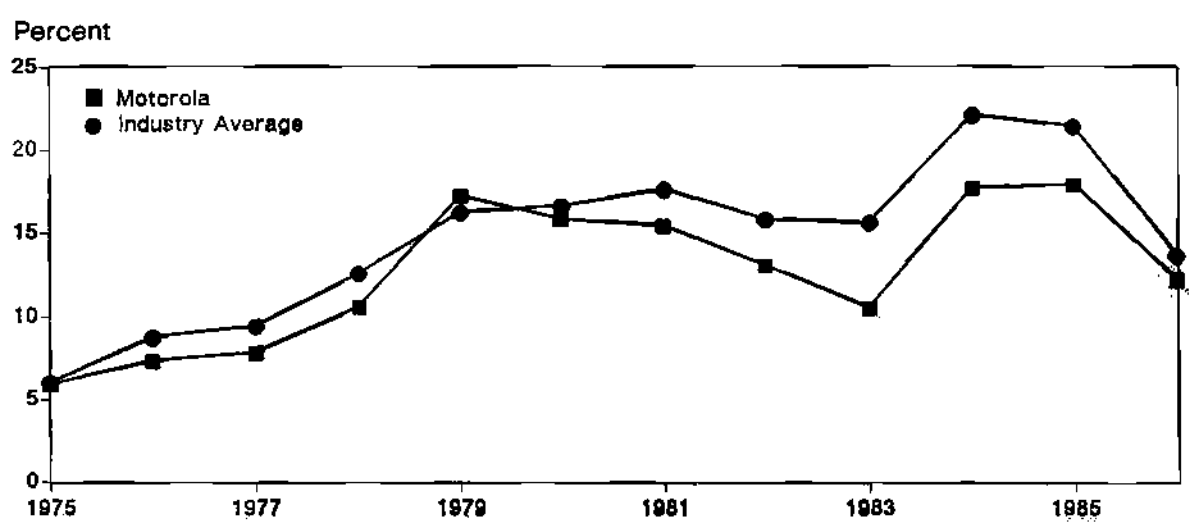
A large part of Motorola's spending in 1986 was for converting all of its domestic MOS fabs to CMOS. Motorola's new fab in East Kilbride, Scotland, began production in 1987. This facility, which Motorola calls "one of the finest in the world," will feature automatic wafer handling, 6-inch lines, and 1-micron geometries.

In addition to East Kilbride, a large part of Motorola's spending in 1986 was for the expansion of its test facilities in Guadalahara, Mexico; Korea; and Kuala Lampur. The year 1986 also saw Motorola making a major addition to its final test and assembly facility in Japan and starting construction on a new facility in Munich, West Germany, for final test of ASICs and digital ICs.

Motorola's 1987 spending was mainly for upgrading existing facilities, especially its Izumi City, Japan, facility.

Figure 16

Motorola versus Industry Average
Capital Spending/Production



Source: Dataquest December 1987

Capital Spending

Motorola recently announced that it will resume DRAM manufacturing at facilities in the United States and Europe in 1988. The company will use a 1.2-micron CMOS architecture developed in a joint venture with Toshiba. Motorola which halted DRAM manufacturing two years ago, will transfer the process from Japan to its MOS-6 fab in Mesa, Arizona; MOS-8 in Austin, Texas; and MOS-9 in East Kilbride, Scotland. A new fab, MOS-12, is planned for Austin for additional DRAM production, and production of 4-megabit DRAMs is scheduled for 1990.

We also expect Motorola to add to its assembly capability in Hong Kong and Korea. Our estimates for Motorola's 1987 capital spending do not include its joint-manufacturing venture with Toshiba.

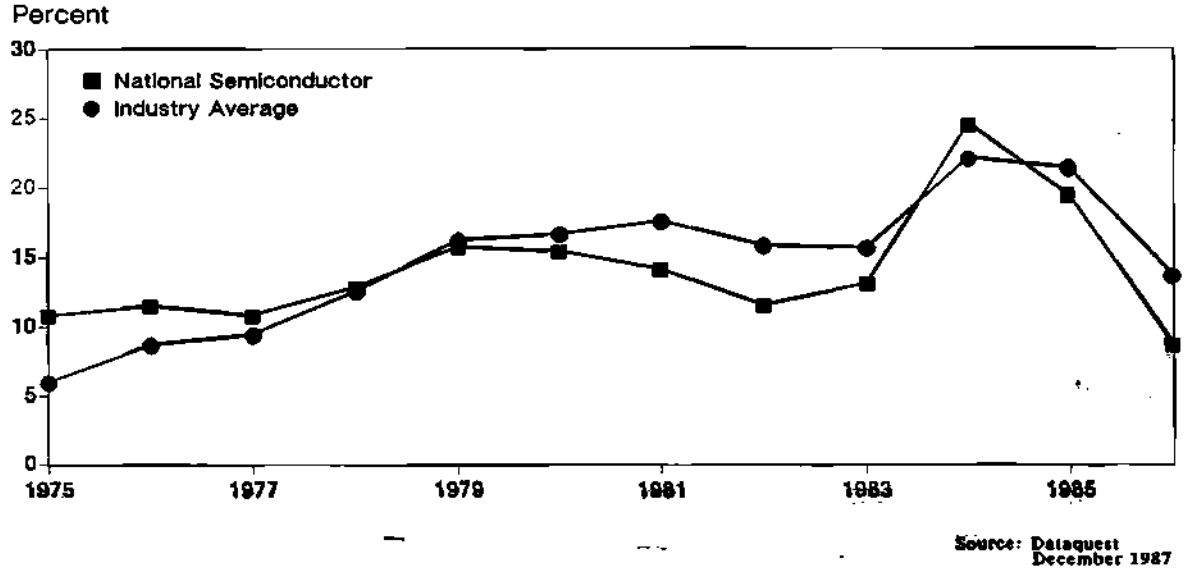
The strategic goals that Motorola hopes to achieve with its capital spending are to expand its CMOS capability, expand its TAB and surface-mount capability, and support its focus factories. (Focus factories are lines or modules within a fab that are dedicated to specific product types or product lines. These factories allow for better predictability of process, improved cycle time, and better delivery.)

National Semiconductor

National Semiconductor's capital-spending-to-revenue ratio, though not coincident with the industry average, has generally paralleled it (see Figure 17). The company's ratio reached its highest level in 1984, at 23 percent, and has fallen since then, reaching 12 percent in 1986.

Figure 17

National Semiconductor versus Industry Average Capital Spending/Production



Capital Spending

Dataquest estimates that National's calendar 1986 capital spending was down 52 percent, from $184 million to $88 million. We anticipate that National's capital spending increased 27 percent in 1987, to $112 million (not including Fairchild's 1987 capital spending), National Semiconductor 1987 efforts were directed toward facilitizing its Arlington, Texas, fab.

Before the acquisition of Fairchild by National Semiconductor, Fairchild had planned to spend $45 million, one–third of its previous year's spending.

NEC

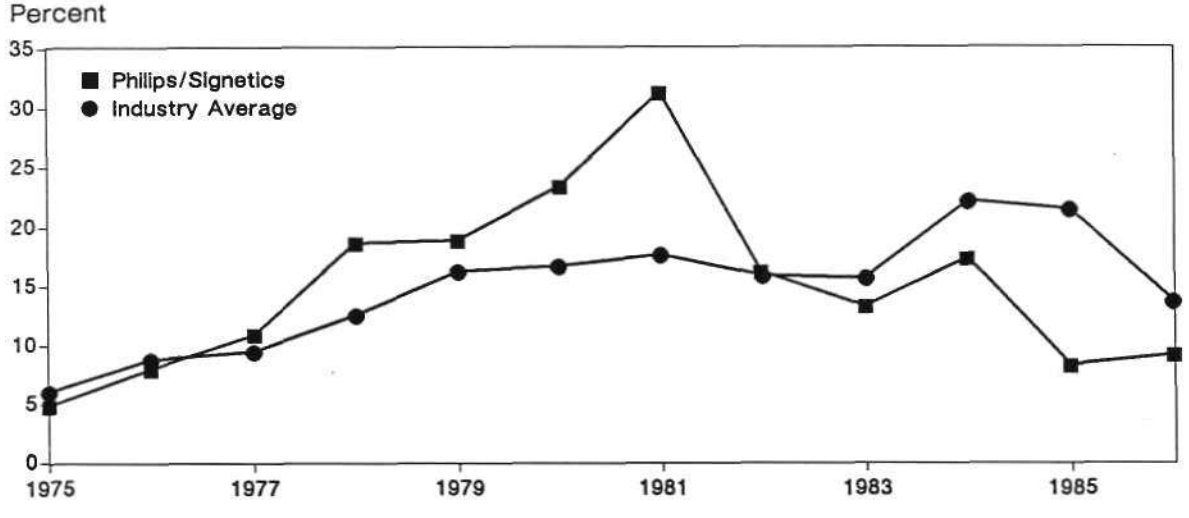
We estimate that NEC spent $10 million in North America in 1986, primarily for test and assembly equipment. We believe that this amount increased in 1987 to $12 million, as NEC expanded capacity at its Roseville, California, fab. Spending in 1987 was for lithographic equipment and for test and assembly equipment. Spending in 1988 will be for more capacity, test and assembly, and upgrading the cleanliness of clean rooms.

Philips–Signetics

Signetics' capital–spending–to–revenue ratio, until 1982, had tended to be above that of the industry average (see Figure 18). However, since 1983, the company's ratio has been below the industry average.

Figure 18

Philips/Signetics versus Industry Average
Capital Spending/Production



Source: Dataquest
December 1987

Capital Spending

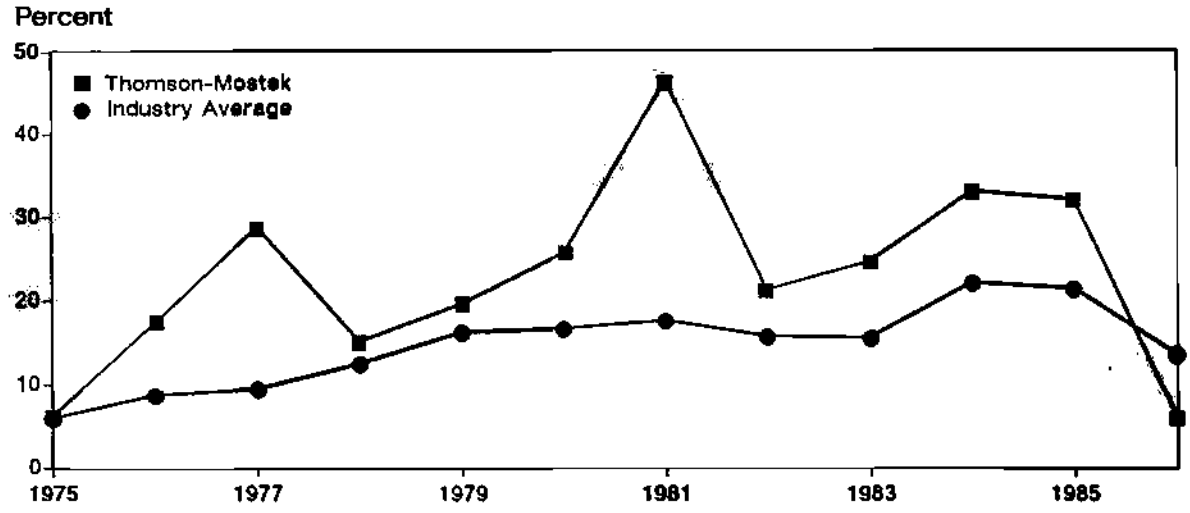
Signetics spent approximately $60 million on capital spending in 1986, up 20 percent from 1985's level of $50 million. We estimate that the company's spending increased 67 percent in 1987, to $100 million. The focus of its 1987 spending is to bring Fab 23 in Albuquerque, New Mexico, on-line in 1988. This new fab will run 6-inch CMOS, 1-micron wafers. We believe that SMD was another focus of capital spending for Philips-Signetics in 1987.

SGS/Thomson (Formerly Thomson/Mostek)

SGS/Thomson's capital-spending-to-production ratio fell in 1986 after Mostek's acquisition from United Technologies by Thomson Semiconductor (see Figure 19). We estimate that SGS/Thomson spent $8 million in 1987 for rounding out capacity at its Carrolton, Texas, facility. This spending was for equipment upgrades and CAD tools. The 6-inch line in Carrolton is scheduled to be in production by the second half of 1988.

Figure 19

SGS/Thomson versus Industry Average
Capital Spending/Production



Source: Dataquest
December 1987

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Siemens

We estimate that Siemens spent $15 million in North America in 1987 to equip its fab in Santa Clara, California. Siemens purchased this facility in 1986 from Hyundai. This facility is now producing power MOS devices for the automobile industry. Siemens will begin work on adding a new semicustom line at its Santa Clara facility in the latter part of 1988.

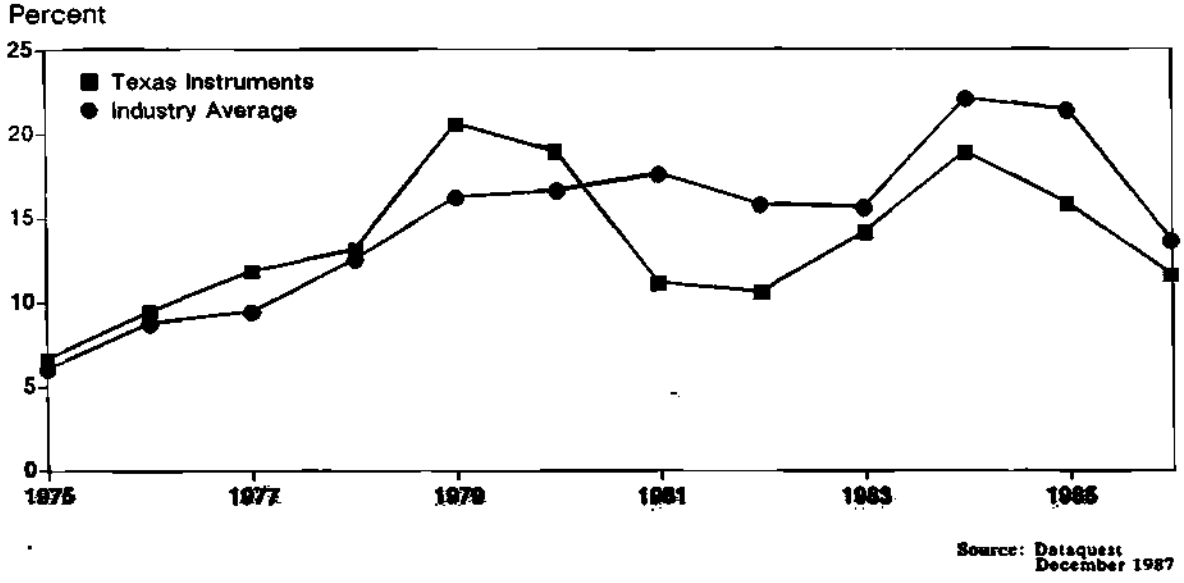
Texas Instruments

Texas Instruments capital-spending-to-revenue ratio has been below the industry's average since 1981 (see Figure 20).

We estimate that the company's semiconductor capital spending in 1986 was $213 million, down 24 percent from 1985. For 1987, we estimate that Texas Instruments' capital spending increased slightly to $240 million. We believe that the company will be spending for equipment to manufacture new gate arrays and 1-megabit DRAMs, especially as it shifts production from its Miho, Japan, fab to its Dallas, Texas, fab. Other areas of spending for Texas Instruments in 1987 include small outline packaging and test equipment.

Figure 20

Texas Instruments versus Industry Average Capital Spending/Production



Source: Dataquest December 1987

Capital Spending

JAPANESE 1986 CAPITAL SPENDING

Japan's capital expenditures fell by 62 percent in yen in calendar 1986, from 766 billion yen in 1985 to 294 billion yen in 1986. We estimate that capital spending decreased in 1987 by 12 percent in yen, to 259 billion yen. Expressed in dollars, the decline in 1886 was 45 percent, from $3.219 million in 1985 to $1.760 thousand in 1986. In 1987, the decline in dollars was only 4.5 percent, to $1.682 thousand.

Expressed as a percent of production, capital spending reached a high in 1984 and 1985 of more than 30 percent of production. The capital-spending-to-production ratio fell to less than 12 percent in 1986 and we expect this ratio to be 9 percent for 1987 (see Table 8).

Table 8

Estimated Japanese Company Capital Spending by Calendar and Fiscal Years (Billions of Yen, Millions of Dollars)

Year	FY Capital Spending	FY Percent Change	CY Capital Spending	CY Percent Change	CY Production
1975			¥ 15		¥ 251
1976			¥ 34	120.2%	¥ 423
1977			¥ 42	23.5%	¥ 468
1978	¥ 59		¥ 51	21.2%	¥ 533
1979	¥103	76.1%	¥ 91	78.8%	¥ 609
1980	¥162	56.5%	¥ 144	57.7%	¥ 846
1981	¥195	20.5%	¥ 185	28.6%	¥1,162
1982	¥279	43.6%	¥ 229	24.1%	¥1,390
1983	¥459	64.4%	¥ 399	74.2%	¥1,863
1984	¥966	110.4%	¥ 870	118.0%	¥2,833
1985	¥688	(28.8%)	¥ 766	(12.0%)	¥2,544
1986	¥354	(48.6%)	¥ 294	(61.6%)	¥2,510
1987	¥346	(2.1%)	¥ 259	(11.9%)	¥2,783
1988		3.9%	¥ 326	26.0%	¥3,411
1989			¥ 375	15.0%	¥3,287
1990			¥ 563	50.0%	¥3,632
1991			¥ 788	40.0%	¥4,094
1992			¥1,048	33.0%	¥4,726

(Continued)

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Capital Spending

Table 8 (Continued)

Estimated Japanese Capital Spending by Calendar and Fiscal Years
(Billions of Yen, Millions of Dollars)

Year	FY Capital Spending/ Production	CY Yen/US$)	CY Capital Spending (US$)	CY Percent Change (US$)
1975	6.2%	¥297	$ 52	
1976	8.0%	¥296	$ 115	120.9%
1977	9.0%	¥269	$ 156	35.9%
1978	9.5%	¥210	$ 242	55.2%
1979	14.9%	¥219	$ 416	71.4%
1980	17.0%	¥227	$ 632	52.1%
1981	15.9%	¥221	$ 834	31.9%
1982	16.5%	¥249	$ 921	10.5%
1983	21.4%	¥235	$1,698	84.3%
1984	30.7%	¥237	$3,671	116.2%
1985	30.1%	¥238	$3,219	(12.3%)
1986	11.7%	¥167	$1,760	(45.3%)
1987	9.3%	¥154	$1,682	(4.5%)
1988	9.6%	¥154	$2,119	26.0%
1989	11.4%	¥154	$2,437	15.0%
1990	15.5%	¥154	$3,655	50.0%
1991	19.3%	¥154	$5,118	40.0%
1992	22.2%	¥154	$6,807	

Source: Dataquest
December 1987

These changes in Japanese capital spending are due to major shocks that have hit the Japanese economy in general and the semiconductor industry in particular.

These fundamental changes affecting the Japanese semiconductor industry are as follows:

- MITI production quotas due to trade friction with Japan's leading trading partners, including the United States and Europe
- Sharply reduced profits and even some layoffs
- The yen shock, which has raised production costs by more than 50 percent within the last year

Capital Spending

We expect Japanese capital spending to recover somewhat in 1988, increasing 26 percent, from $1.69 billion in 1987 to $2.1 billion in 1988. After 1988, we expect Japanese capital spending to increase at a rate much faster than the worldwide average, as the $6.9 billion of capital put on-stream in the 1984 to 1985 time frame will be nearing the end of its productive life and will have to be replaced. Equipment purchased during the 1984–1985 period will represent more than 50 percent of the Japanese installed base through the remainder of this decade.

As a consequence of the aging of a significant part of the Japanese installed base, we anticipate that Japanese capital spending will increase 15 percent in 1989 when the worldwide market for capital goods will be flat; we also estimate that 1990 and 1991 Japanese capital spending will increase by 50 percent and 40 percent, respectively.

Japanese Company Spending

As shown in Tables 9 and 10, the combined spending of individual Japanese semiconductor makers has dropped sharply since 1984. Of the top nine semiconductor manufacturers, NEC and Hitachi have registered declines in capital spending greater than 60 percent from 1984 to 1987. Matsushita and Fujitsu had declines of more than 70 percent for the same period.

However, our analysts in Japan report strong order activity by Japanese semiconductor companies. For example, NEC has recently announced that it will start full production of 1Mb DRAMs at its Yamaguchi facility. Toshiba has now started production on its recently completed 6-inch line in Ohita.

Table 9

Japanese Company Capital Spending
Merchant Calendar Year
(Millions of U.S. Dollar)

Company	1976	1977	1978	1979	1980	1981
Fuji Electric	0	0	0	0	0	0
Fujitsu	$ 3	$ 22	$ 48	$ 64	$110	$145
Hitachi	20	22	43	59	93	149
Japan Semiconductor	0	0	0	0	0	0
Matsushita	10	11	19	41	88	86
Mitsubishi	17	22	19	41	35	59
NEC	34	37	67	105	132	172
NJRC	0	0	0	0	0	0
NMB	0	0	0	0	0	0
Oki	10	15	10	14	53	54
Rohm	0	0	0	0	0	0
Sanken Electric	0	0	0	0	0	0

(Continued)

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Table 9 (Continued)

Japanese Company Capital Spending
Merchant Calendar Year
(Millions of U.S. Dollar)

Company	1976	1977	1978	1979	1980	1981
Sanyo	7	7	7	18	35	54
Sharp	0	0	7	37	37	43
Shindengen	0	0	0	0	0	0
Seiko Epson	0	0	0	0	0	0
Sony	0	0	0	0	0	0
Toshiba	14	19	24	37	48	72
Others	0	0	0	0	0	0
Total	$115	$156	$242	$416	$632	$834

Company	1982	1983	1984	1985	1986	1987
Fuji Electric	$ 16	$ 26	$ 51	$ 50	$ 30	$ 32
Fujitsu	141	226	485	303	96	130
Hitachi	145	264	506	387	132	162
Japan Semiconductor	0	0	0	0	30	0
Matsushita	36	89	464	252	150	117
Mitsubishi	80	132	274	261	120	65
NEC	169	247	544	517	180	195
NJRC	8	9	17	21	30	19
NMB	0	0	59	59	0	19
Oki	44	47	110	109	60	97
Rohn	8	13	25	38	48	65
Sanken Electric	8	40	51	25	24	19
Sanyo	40	51	135	197	108	130
Sharp	32	68	110	151	132	65
Shindengen	4	4	13	13	18	6
Seiko Epson	20	38	76	34	30	32
Sony	20	38	59	151	96	104
Toshiba	113	366	574	517	389	325
Others	36	68	143	134	90	97
Total	$921	$1,698	$3,671	$3,219	$1,760	$1,682

Source: Dataquest
December 1987

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Capital Spending

Table 10

Japanese Company Capital Spending
Calendar Year Japanese Capital Expenditures
(Billions of Yen)

Company	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987
Fuji Electric	0	0	0	0	0	0	4	6	12	12	5	5
Fujitsu	1	6	10	14	25	32	35	53	115	72	16	20
Hitachi	6	6	9	13	21	33	36	62	120	92	22	25
Japan Semiconductor	0	0	0	0	0	0	0	0	0	0	5	0
Matsushita	3	3	4	9	20	19	9	21	110	60	25	18
Mitsubishi	5	6	4	9	8	13	20	31	65	62	20	10
NEC	10	10	14	23	30	38	42	58	129	123	30	30
NJRC							2	2	4	5	5	3
NMB	0	0	0	0	0	0	0	0	14	14	0	3
Oki	3	4	2	3	12	12	11	11	26	26	10	15
Rohm	0	0	0	0	0	0	2	3	6	9	8	10
Sanken Electric	0	0	0	0	0	0	2	3	6	6	4	3
Sanyo	2	2	1	4	8	12	10	12	32	47	18	20
Sharp	0	0	2	8	9	10	8	16	26	36	22	10
Shindengen	0	0	0	0	0	0	1	1	3	3	3	1
Seiko Epson	0	0	0	0	0	0	5	9	18	8	5	5
Sony	0	0	0	0	0	0	5	9	14	36	16	16
Toshiba	4	5	5	8	11	16	28	86	136	123	65	50
Others	0	0	0	0	0	0	9	16	34	32	15	15
Total	34	42	51	91	144	185	229	399	870	766	294	259
Percent Change	-	24%	21%	79%	58%	29%	24%	74%	118%	(12%)	(62%)	(12%)

Source: Dataquest
December 1987

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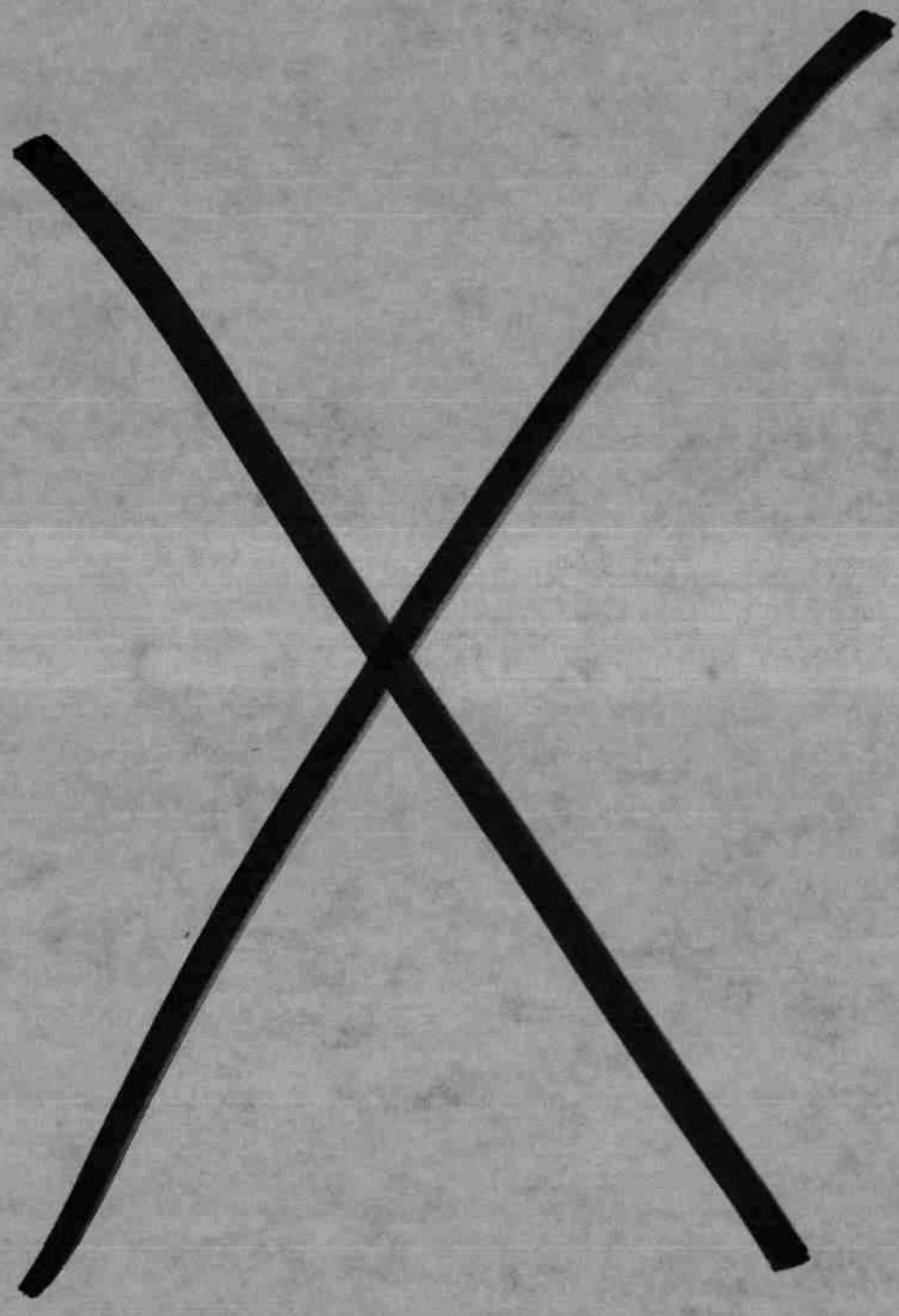

R&D

The following is a list of the material in this section:

- U.S. Merchant and Captive Semiconductor Manufacturers' R&D Expenditure

For additional information, please refer to the material behind the R&D tab in your Newsletter binder.

U.S. Merchant and Captive Semiconductor Manufacturers' R&D Expenditure

Semiconductor research and development (R&D) is vital for the continued development of new products, applications, and processes. Very few industries are able to match the semiconductor industry's record for R&D expenditure as a percentage of revenue. In the semiconductor industry, R&D expenditure is the seed corn from which the future emerges.

Table 1 and Figure 1 show U.S. merchant and captive semiconductor manufacturers' R&D expenditure from 1981 through 1989. Please note that these estimates differ from our previously published estimates in that we have now included an estimate for the "Others" category and for the captives. R&D expenditure has increased each year. The compound annual growth rate (CAGR) of R&D expenditure from 1981 to 1989 is 16 percent.

Table 2 and Figure 2 show U.S. merchant and captive semiconductor manufacturers' R&D expenditure as a percentage of semiconductor revenue.

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Table 1

U.S. Merchant and Captive Semiconductor R&D Expenditure (Millions of Dollars)

	1981	1982	1983	1984	1985	1986	1987	1988	1989	CAGR 1981-1989
Merchant Companies										
Advanced Micro Devices	42	63	106	169	207	223	248	208	202	
Altera	N/M	N/M	0	1	3	3	4	6	9	
Analog Devices	8	11	15	21	27	33	56	56	71	
California Micro Devices	N/M	N/M	0	1	1	1	2	3	3	
Chips & Technologies	N/M	N/M	N/M	N/M	2	4	12	28	39	
Cypress	N/M	N/M	2	5	5	10	19	34	48	
Harris	16	20	22	44	37	36	37	45	65	
IDT	N/M	1	2	5	11	14	18	26	38	
IMP	N/M	N/M	3	3	3	2	7	8	12	
Intel	109	122	132	163	175	178	234	318	365	
LSI Logic	N/M	2	4	12	14	22	29	37	42	
Linear Technology	N/M	2	3	2	2	3	4	5	7	
Micron Technology	N/M	2	1	4	5	4	7	12	27	
Motorola	116	128	155	176	192	199	207	225	289	
National Semiconductor	83	89	114	158	187	190	213	255	250	
SEEQ	N/M	N/M	5	6	6	7	8	9	9	
Siliconix	6	8	9	12	15	16	17	17	19	
Silicon Systems	N/M	1	2	3	5	8	9	12	15	
Texas Instruments	119	128	163	195	214	256	270	292	327	
VLSI Technology	N/M	3	8	14	20	23	31	38	46	
Xicor	N/M	N/M	5	8	11	9	8	11	13	
ZyMOS	N/M	N/M	4	5	4	4	5	7	9	
Others	293	341	340	380	459	641	624	614	615	
Total Merchant	793	921	1,097	1,386	1,605	1,886	2,067	2,265	2,520	16%
Percent Change	13	16	19	26	16	17	10	10	11	
Captive Companies	225	280	302	324	526	557	582	627	706	15%
Percent Change		24	8	7	63	6	4	8	13	
Total Merchant and Captive	1,018	1,201	1,399	1,710	2,131	2,443	2,649	2,892	3,226	16%
Percent Change		18	16	22	24	14	8	10	12	

N/M = Not Meaningful

Source: Dataquest April 1990

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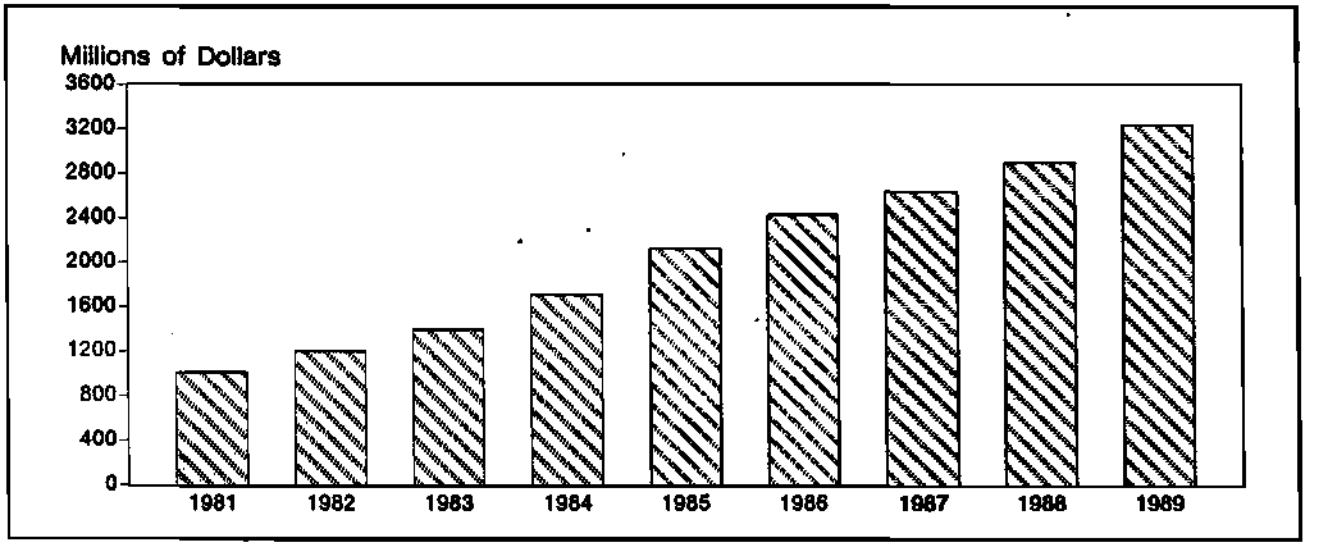
Figure 1

U.S. Merchant and Captive Semiconductor Manufacturers' R&D Spending (Millions of Dollars)



0006718-1

Source: Dataquest
April 1990

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Table 2

U.S. Merchant and Captive Semiconductor R&D Expenditure as a Percentage of Semiconductor Revenue

	1981	1982	1983	1984	1985	1986	1987	1988	1989
Merchant Companies									
Advanced Micro Devices	15	19	17	15	26	27	25	19	19
Altera	N/M	N/M	N/M	467	70	28	20	15	16
Analog Devices	9	11	10	10	12	14	19	15	20
California Micro Devices	N/M	N/M	7	8	8	8	8	11	11
Chips & Technologies	N/M	N/M	N/M	N/M	N/M	11	10	18	16
Cypress	N/M	N/M	N/M	123	29	21	24	25	24
Harris	10	13	13	17	15	13	14	14	8
IDT	N/M	45	23	15	21	19	18	15	18
IMP	N/M	N/M	20	10	11	7	16	17	22
Intel	21	20	17	14	17	18	16	14	15
LSI Logic	N/M	38	14	14	10	11	11	10	8
Linear Technology	N/M	N/M	63	14	13	10	8	9	9
Micron Technology	N/M	40	4	3	15	6	6	4	7
Motorola	10	11	9	8	10	10	8	7	9
National Semiconductor	7	8	8	8	13	13	14	15	15
SEEQ	N/M	N/M	54	11	20	21	15	15	17
Siliconix	11	13	13	12	14	14	15	13	15
Silicon Systems	N/M	N/M	7	5	10	10	11	9	14
Texas Instruments	9	10	10	8	12	14	13	11	12
VLSI Technology	N/M	16	24	20	25	21	18	17	16
Xicor	N/M	N/M	34	21	34	21	13	12	14
ZyMOS	N/M	N/M	43	22	24	23	19	25	24
Others	N/M	N/M	11	10	15	15	14	12	13
Total Merchant	10	12	11	10	15	15	14	12	13
Captive Companies	13	15	15	13	19	19	18	17	17
Total Merchant and Captive	11	12	12	10	15	15	15	13	14

N/M = Not Meaningful

Source: Dataquest April 1990

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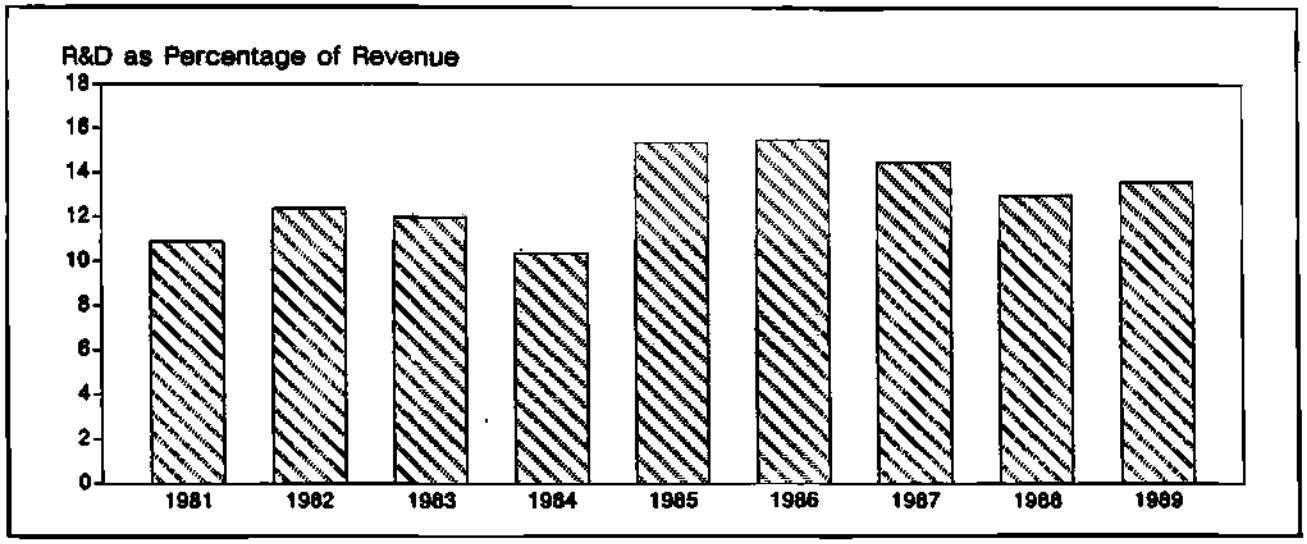
Figure 2

U.S. Merchant and Captive Semiconductor Manufacturers' R&D Spending as a Percentage of Revenue



0006718-2

Source: Dataquest
April 1990

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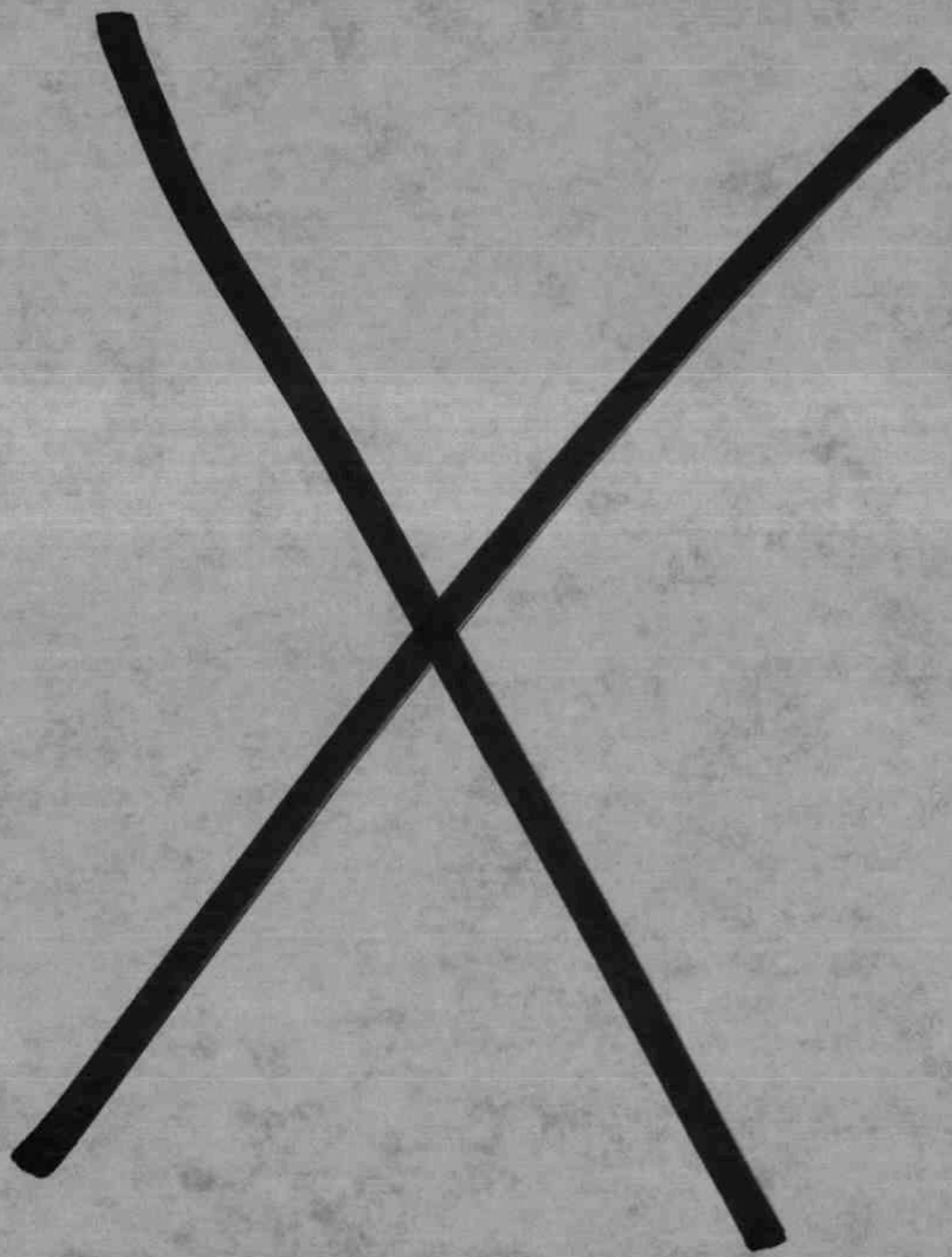

Worldwide Fabs

The following is a list of the material in this section:

- Definitions - Worldwide Fab Database
- North American Fab Data Base
- European Fab Database
- Japanese Fab Data Base
- Asia/Pacific and Rest of World Fab Database
- Future Fab Activity--North America
- Future Fab Activity--Japan
- Future Fab Activity--Europe
- Future Fab Activity--Asia/Pacific

For additional information, please refer to the material behind the Worldwide Fabs in your 1989 Newsletter binder.

All Semiconductor Front-End Fab Lines Excluding R&D
(Includes New Fabs Going into Production During 1990)

Company	Country or Territory	City or District	Fab Name	Products Produced	Process Technology	Min. Line Width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. in. Start Capacity (4 wks.)	Clean Room (square feet)	Clean Room Class	Origin of Owner	Mer., Cap., Res.
ADVANCE DEVICES TECH.	TAIWAN	HSINCHU	N/A	DIS OPTO	BIP MOS	0.00	0	0	0	0	0	TAIWAN	M
AMALGAMATED WIRELESS	AUSTRALIA	SYDNEY	N/A	ASIC	CMOS	1.50	6	0	0	0	0	AUST./ENGL.	M
AMPI	TAIWAN	HSINCHU	N/A	PWR ICs	N/A	0.00	4	8000	97389	0	0	TAIWAN	M
BEIJING NO.2	CHINA	BEIJING	N/A	INTERFACE IC	BIP TTL	5.00	3	0	0	0	0	CHINA	C
BEIJING NO.3	CHINA	BEIJING	N/A	LOG TRANS LIN MEM WATCH	CMOS MOS	5.00	3	15000	105975	0	0	CHINA	C
BEIJING NO.5	CHINA	BEIJING	N/A	OP AMP LOG PWR TRAN	N/A	5.00	3	0	0	0	0	CHINA	C
BEIJING NO.878	CHINA	BEIJING	N/A	DIS	N/A	5.00	3	0	0	0	0	CHINA	C
BEIJING TUBE FACTORY	CHINA	BEIJING	N/A	DIS	N/A	5.00	4	0	0	0	0	CHINA	C
BEL	INDIA	BANGALORE	N/A	DIS	N/A	4.00	4	0	0	0	0	INDIA	M
CHARTERED S/C	SINGAPORE	N/A	N/A	ASIC	CMOS	1.20	6	5000	136907	0	0	SING./U.S.	M
CONTINENTAL DEVICES	INDIA	DELHI	N/A	DIS DIODE TRAN PWR SCR	N/A	0.00	3	0	0	0	0	INDIA	M
DAEWOO	KOREA	SEOUL	GURO	CUSTOM AUTOMOTIVE AUDIO	BIP	0.00	4	9000	109563	0	0	KOREA	M
DAEWOO	KOREA	SEOUL	GURO	TELECOM MPR CUSTOM	CMOS	0.00	4	9000	109563	0	0	KOREA	M
DONG GUANG PLANT	CHINA	BEIJING	N/A	LOG MPU	BIP TTL	5.00	3	0	0	0	0	CHINA	C

Continued

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All Semiconductor Front–End Fab Lines Excluding R&D (Continued)
(Includes New Fabs Going into Production During 1990)

Company	Country or Territory	City or District	Fab Name	Products Produced	Process Technology	Min. Line Width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. in. Start Capacity (4 wks.)	Clean Room (square feet)	Clean Room Class	Origin of Owner	Mer., Cap., Res.
ELCAP	HONG KONG	TAI PO	N/A	MEM MPU LOG LIN	MOS	0.00	3	90000	635850	0	0	HONG KONG	M
ELECT. COMPONENTS INDIA	INDIA	HYDERABAD	N/A	DIS CONSUMER ICs	BIP	0.00	3	0	0	0	0	INDIA	M
FINE MICROELECT.	TAIWAN	HSINCHU	N/A	OPTO TRAN	N/A	0.00	3	0	0	0	0	TAIWAN	M
FUCHOU	CHINA	FUCHOU	N/A	N/A	N/A	5.00	3	0	0	0	0	CHINA	M
GENERAL INSTRUMENT	TAIWAN	N/A	N/A	PWR DIS	BIP	0.00	3	12000	84780	0	0	U.S.	M
GOLDSTAR	KOREA	ANYANG	N/A	MPU ASIC 64K SRAM	CMOS	0.00	5	10000	190175	0	0	KOREA/U.S.	M
GOLDSTAR	KOREA	GUMI	PLANT 1	LIN	BIP	0.00	4	25000	304341	0	0	KOREA/U.S.	M
GOLDSTAR	KOREA	GUMI	PLANT 2	64K SRAM MPU ARRAYS	CMOS MOS	0.00	5	15000	285262	0	0	KOREA/U.S.	M
GOLDSTAR	KOREA	WOOMYUN	N/A	LOG LIN DIS CONSUMER	BIP	0.00	5	3000	57052	0	0	KOREA/U.S.	M
GOLDSTAR	KOREA	WOOMYUN	N/A	256K DRAM 1Mb PROTO	CMOS HITACHI	1.20	6	18000	492866	0	0	KOREA/U.S.	M
GOVERNMENT OF IRAQ	IRAQ	N/A	N/A	N/A	N/A	0.00	0	0	0	0	0	IRAQ	C
HARBIN FACTORY	CHINA	HARBIN	N/A	TRAN	N/A	5.00	3	0	0	0	0	CHINA	C
HUA KO ELECTRONICS	HONG KONG	TAI PO	N/A	MEM MPU LOG LIN	MOS	0.00	4	4500	54781	0	0	HONG KONG	M
HUALON MICROELECT.	TAIWAN	HSINCHU	FAB 1	SRAM DRAM POLY2 M2	CMOS	1.50	5	30000	570524	0	0	TAIWAN	M

Continued

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All Semiconductor Front-End Fab Lines Excluding R&D (Continued)
(Includes New Fabs Going into Production During 1990)

Company	Country or Territory	City or District	Fab Name	Products Produced	Process Technology	Min. Line Width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. in. Start Capacity (4 wks.)	Clean Room (square feet)	Clean Room Class	Origin of Owner	Mer., Cap., Res.
HUALON MICROELECT.	TAIWAN	HSINCHU	FAB 2	MEM TELECOM SRAM	CMOS	0.00	6	30000	821444	0	0	TAIWAN	M
HYUNDAI	KOREA	ICHON	S/C 1	16K SRAM EPROM	CMOS MOS	1.50	5	15000	285262	0	0	KOREA	M
HYUNDAI	KOREA	ICHON	S/C 2	256K 1Mb DRAM 256K SRAM	CMOS TI	1.20	6	25000	684536	0	0	KOREA	M
HYUNDAI	KOREA	ICHON	S/C 3	1Mb DRAM 64K 256K SRAM	CMOS	0.80	5	8000	152140	0	0	KOREA	M
HYUNDAI	KOREA	ICHON	S/C 4	1Mb DRAM 4Mb PROTO SRAM	CMOS	1.00	6	20000	547629	0	0	KOREA	M
INDIAN TELEPHONE	INDIA	BANGALORE	N/A	ARRAYS TELECOM	CMOS VLSI	1.50	5	0	0	0	0	INDIA	C
INDIAN TELEPHONE	INDIA	BANGALORE	N/A	DIS	BIP	0.00	3	0	0	0	0	INDIA	C
INTEL	ISRAEL	JERUSALUM	FAB 8	386 MPU 286 MPU	CMOS	1.50	6	21000	575011	24000	10	U.S.	M
JINAN NO.1	CHINA	JINAN	N/A	LOG OP AMP	N/A	5.00	3	0	0	0	0	CHINA	C
JINAN NO.2	CHINA	JINAN	N/A	1K SRAM 4K DRAM	MOS	5.00	3	0	0	0	0	CHINA	C
KOREA ELECTRONICS	KOREA	GUMI	N/A	DIS LIN OPTO	BIP	0.00	4	20000	243473	0	0	KOREA	M
KUO HWA	TAIWAN	N/A	N/A	N/A	N/A	0.00	5	10000	190175	0	0	TAIWAN	M
LIAONING FACTORY	CHINA	JINZHOU	N/A	TRAN	N/A	5.00	3	0	0	0	0	CHINA	C

Continued

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All Semiconductor Front-End Fab Lines Excluding R&D (Continued)
(Includes New Fabs Going into Production During 1990)

Company	Country or Territory	City or District	Fab Name	Products Produced	Process Technology	Min. Line Width	Wef. Size	Wafer Start Capacity (4 wks.)	Sq. in. Start Capacity (4 wks.)	Clean Room (square feet)	Clean Room Class	Origin of Owner	Mer., Cap., Res.
MIN MACHINERY INDUSTRY	CHINA	N/A	N/A	LOG PWR TRAN	MOS GE	5.00	3	0	0	0	0	CHINA/U.S.	C
MOTOROLA	MALAYSIA	SEREMBAN	N/A	PWR TRAN DIS SST	N/A	0.00	6	0	0	6000	0	U.S.	M
NATIONAL S/C	ISRAEL	HA-EMEK	N/A	32-bit MPU	CMOS	1.20	6	6400	175241	20000	10	U.S.	M
NATIONAL S/C	MALAYSIA	PENANG	N/A	LOG	N/A	0.00	4	0	0	0	0	U.S.	M
PHOTRONICS	TAIWAN	N/A	N/A	OPTO	N/A	0.00	0	0	0	0	0	TAIWAN	M
QIANMEN S/C FACTORY	CHINA	BEIJING	N/A	DIG WATCH IC	N/A	5.00	3	0	0	0	0	CHINA	C
QUASEL	TAIWAN	N/A	N/A	MEM	MOS	0.00	4	0	0	0	0	TAIWAN	M
RAMAX	AUSTRALIA	MELBOURNE	N/A	FERRAM	CMOS GaAs	0.00	0	0	0	0	0	AUST./U.S.	M
RCL S/C	HONG KONG	N/A	N/A	MEM MPU LOG LIN TRAN	CMOS	0.00	4	4000	48695	0	0	HONG KONG	M
RECTRON	TAIWAN	TAIPEI	NO. 1	DIS	N/A	0.00	2	90000	282600	0	0	TAIWAN	M
ROHM	KOREA	SEOUL	N/A	DIS OPTO	N/A	0.00	0	0	0	0	0	JPN.	M
S. AFRICAN MICROELECT.	SOUTH AFRICA	PRETORIA	N/A	A/D D/A TELECOM	BIP	5.00	3	0	0	0	0	SOUTH AFRICA	M
S. AFRICAN MICROELECT.	SOUTH AFRICA	PRETORIA	N/A	A/D D/A TELECOM	CMOS	3.00	4	0	0	0	0	SOUTH AFRICA	M
SAMMI	KOREA	N/A	N/A	LASER DIODE	GaAs	0.00	2	0	0	0	0	KOREA	M
SAMSUNG	KOREA	BUCHON	N/A	LIN	BIP	0.00	4	25000	304341	0	0	KOREA	M
SAMSUNG	KOREA	BUCHON	N/A	MPU LOG ASIC PWR MOSFET	CMOS MOS	2.00	5	20000	380350	0	0	KOREA	M
SAMSUNG	KOREA	KIHEUNG	FAB 1	64K DRAM SRAM EEPROM ASIC	MOS	2.00	4	35000	426078	0	0	KOREA	M

Continued

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All Semiconductor Front-End Fab Lines Excluding R&D (Continued)
(Includes New Fabs Going into Production During 1990)

Company	Country or Territory	City or District	Fab Name	Products Produced	Process Technology	Min. Line Width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. in. Start Capacity (4 wks.)	Clean Room (square feet)	Clean Room Class	Origin of Owner	Mer., Cap., Res.
SAMSUNG	KOREA	KIHEUNG	FAB 2	256K DRAM 256K EPROM SRAM	MOS	1.50	6	35000	958351	0	0	KOREA	M
SAMSUNG	KOREA	KIHEUNG	FAB 3	1Mb DRAM 4Mb SAMPLE	CMOS	1.00	6	30000	821444	0	0	KOREA	M
SAMSUNG	KOREA	KIHEUNG	FAB 4	1Mb DRAM 4Mb DEVELOP SRAM	CMOS	0.80	6	30000	821444	0	0	KOREA	M
SGS-THOMSON	SINGAPORE	ANG MO KIO	N/A	PWR TRAN LIN	BIP MOS	0.00	5	25000	475437	14000	10	ITALY	M
SHANGHAI NO.5	CHINA	SHANGHAI	N/A	8080 MPU LOG MEM LIN DIS	CMOS	5.00	3	10000	70650	0	0	CHINA	C
SHANGHAI NO.8331	CHINA	SHANGHAI	N/A	OP AMP PWR TRAN	BIP TTL	5.00	3	0	0	0	0	CHINA	C
SHANGHAI PHILIPS NO.7	CHINA	SHANGHAI	N/A	OP AMP PWR TRAN DIS	BIP TTL	5.00	3	20000	141300	0	0	CHINA/NETH.	M
SID MICROELECT.	BRAZIL	CONTAGEM	N/A	LIN PWR TRAN SST PWR ICs	BIP	30.00	3	0	0	15000	100	BRAZIL/JPN.	M
SID MICROELECT.	BRAZIL	CONTAGEM	N/A	PWR ICs	CMOS	2.00	4	0	0	15000	0	BRAZIL	M
SPIC ELECTRONICS	INDIA	MADRAS	N/A	PHOTO VOLTAIC DIS	N/A	3.00	3	0	0	0	0	INDIA	M
SYNTEK	TAIWAN	N/A	N/A	N/A	N/A	0.00	0	0	0	0	0	N/A	M

Continued

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All Semiconductor Front-End Fab Lines Excluding R&D (Continued)
(Includes New Fabs Going into Production During 1990)

Company	Country or Territory	City or District	Fab Name	Products Produced	Process Technology	Min. Line Width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. in. Start Capacity (4 wks.)	Clean Room (square feet)	Clean Room Class	Origin of Owner	Mer., Cap., Res.
TIAN GUANG FACTORY	CHINA	SHAOXING	N/A	LOG	BIP ECL TTL	5.00	4	14000	170431	0	0	CHINA	C
TIANJIN NO.1	CHINA	TIANJIN	N/A	AUDIO IC	CMOS FUJI	5.00	3	0	0	0	0	CHINA/JPN.	C
TSMC	TAIWAN	HSINCHU	FAB 1	LOG ASIC SRAM ROM DRAM	MOS CMOS	1.50	6	10000	273815	7637	10	TAIWAN	M
TSMC	TAIWAN	HSINCHU	FAB 2-A	SRAM ROM DRAM LOG CUSTOM	CMOS	1.20	6	20000	547629	40000	1	TAIWAN	M
UNITED MICROELECT.	TAIWAN	HSINCHU	FAB 1	MCU LIN 64K SRAM CUSTOM	CMOS MOS M2	1.25	4	50000	608683	0	0	TAIWAN	M
UNITED MICROELECT.	TAIWAN	HSINCHU	FAB 2	MCU TELECOM SRAM CUSTOM	CMOS MOS M2	1.00	6	30000	821444	45000	0	TAIWAN	M
WINBOND	TAIWAN	HSINCHU	FAB 1	ASIC MPR TELECOM SRAM ROM	CMOS MOS ERSO	1.50	5	15000	285262	0	10	TAIWAN	M
WUXI FACTORY	CHINA	WUXI	N/A	TRAN DIODES LIN LOG MEM	MOS TOSHIBA	5.00	4	15000	182605	0	0	CHINA/JPN.	M
YANHE RADIO FACTORY	CHINA	XIAN	N/A	LIN LOG	N/A	5.00	3	0	0	0	0	CHINA	C

Source: Dataquest January 1990

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North American Fab Database
Fab Activity Planned or Initiated to Begin Production During 1990 and Beyond

Company	City	St.	Fab Name	Products	Process Technology	Fab Type	Target Date Prod. Begins	Min. Line-width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. In. Start Capacity (4 wks.)	Clean Room (Square feet)
** Production Begins 1990												
AMCC	SAN DIEGO	CA	N/A	ARRAYS CBIC	BIP	F		1.00	6	8000	219052	15000
AMD	SUNNYVALE	CA	R&D CTR	N/A	N/A	P	08/01/90	0.80	6	6800	186194	35000
AMD	AUSTIN	TX	FAB 10	FULL VLF LITHO AREA	N/A	F	12/01/90	0.80	6	10000	273815	0
AT&T	ORLANDO	FL	OR2	256K 1Mb SRAM	CMOS MITSUBISHI	NF	11/01/90	0.80	6	22400	613345	25000
BROOKTREE	PORTLAND	OR	N/A	HIGH SPEED A/D D/A GRAPH.	BIP	R	02/01/90	0.00	0	0	0	0
DALLAS S/C	DALLAS	TX	FAB 2	SRAM CCD	CMOS	F	04/01/90	1.00	6	12000	328577	20000
HARRIS S/C	MOUNTAINTOP	PA	N/A	ASIC PWR ICs AUTOMOTIVE	BICMOS CMOS	F	02/01/90	0.00	6	8500	232742	0
HP	CORVALLIS	OR	N/A	ASIC MPR DSP	N/A	NF	11/01/90	0.00	6	15000	410722	20000
IBM	HOPEWELL JUNCTION	NY	ASTC/MEM	MEM PROCESS VERIFICATION	CMOS	P	02/01/90	0.80	8	10000	486205	20000
IBM	HOPEWELL JUNCTION	NY	ASTC/LOG	LOG PROCESS VERIFICATION	BIP CMOS	P	02/01/90	0.80	8	10000	486205	20000
IBM	HOPEWELL JUNCTION	NY	ASTC/R&D	16Mb 64Mb DRAM	BICMOS BIP CMOS	R	02/01/90	0.60	8	10000	486205	20000
IBM	ESSEX JUNCTION	VT	BLDG 973	1Mb 4Mb DRAM	CMOS	F	03/01/90	0.80	8	20000	972409	40000
IBM	ESSEX JUNCTION	VT	BLDG 973	4Mb DRAM	CMOS M2	F	11/01/90	0.80	8	20000	972409	40000
IDT	SANTA CLARA	CA	FAB 3	PROCESS DEVELOP	BICMOS CMOS	F	03/01/90	0.50	6	18000	492866	0
INTEL	RIO RANCHO	NM	FAB 9.2	386 486 MPU EPROM	CMOS	F	11/01/90	1.00	6	13600	372388	25000

(Continued)

SEMS Semiconductor Manufacturing 0006655

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North American Fab Database
Fab Activity Planned or Initiated to Begin Production During 1990 and Beyond (Continued)

Company	City	St.	Fab Name	Products	Process Technology	Fab Type	Target Date Prod. Begins	Min. Line-width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. In. Start Capacity (4 wks.)	Clean Room (Square Feet)
INTL. MICROCIRC.	MILPITAS	CA	N/A	ARRAYS	CMOS	Q		1.50	0	0	0	12000
LINEAR TECHNOLOGY	MILPITAS	CA	FAB 2	LIN	BIP CMOS	F	10/01/90	2.00	5	6400	121712	6000
MAXIM INTEGRATED PROD.	SUNNYVALE	CA	N/A	OP AMPS A/D D/A	CMOS	P	06/01/90	3.00	4	4000	48695	13500
MICRON TECHNOLOGY	BOISE	ID	FAB 3	SAMPLE 4Mb DRAM 16Mb DEV.	CMOS IBM	P	04/01/90	0.80	6	20000	547629	0
MITSUBISHI	DURHAM	NC	N/A	1Mb DRAM ARRAYS MCU	CMOS	F	06/01/90	1.00	6	8500	232742	0
MOTOROLA	SCHAUMBERG	IL	N/A	SMARTPOWER	BIP	P	02/01/90	5.00	4	10000	121737	10000
NATIONAL S/C	ARLINGTON	TX	CMOS 2	N/A	CMOS	F	02/01/90	1.20	6	18000	492866	25000
NATIONAL S/C	PUYALLUP	WA	N/A	1Mb SRAM ARRAYS PLD	BICMOS BIP ECL	F	01/01/90	0.80	6	12000	328577	40000
NATL. SECURITY ADMIN.	FORT MEADE	MD	N/A	MIL STD	N/A	P	12/01/90	0.80	6	5000	136907	0
OKI	TUALATIN	OR	N/A	ARRAYS 256K SRAM 4Mb DRAM	CMOS	PAT	06/01/90	1.00	6	16000	438103	15000
PARADIGM TECH.	SAN JOSE	CA	N/A	256K 1Mb SRAM 4 TR.	CMOS M2 POLY 2	P	03/01/90	1.00	5	2500	47544	4000
PERFORMANCE S/C	SUNNYVALE	CA	FAB 2	SRAM MPU ASIC	BICMOS CMOS	P	11/01/90	0.80	6	7000	191670	0
RAMTRON	COLORADO SPRINGS	CO	N/A	FERRAM 4Mb DRAM DEV.	CMOS M2	P	12/01/90	1.00	6	2700	73930	11500
RAYTHEON	MOUNTAIN VIEW	CA	N/A	N/A	BIP ECL	Q		1.00	4	6400	77911	12000
ROHM	SUNNYVALE	CA	PILOT	LIN ARRAYS	BIP EPI	F	04/01/90	0.00	4	17000	206952	14000
SHARP MICROELECT.	CAMUS	WA	N/A	256K 1Mb SRAM FIFO DSP	N/A	DRAT	08/01/90	0.00	0	0	0	0

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North American Fab Database
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Company	City	St.	Fab Name	Products	Process Technology	Fab Type	Target Date Prod. Begins	Min. Line-width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. In. Start Capacity (4 wks.)	Clean Room (Square Feet)
SIGNETICS	ALBUQUERQUE	NM	FAB 24	N/A	N/A	F		1.00	6	8000	219052	15000
U.C. SANTA BARBARA	SANTA BARBARA	CA	N/A	N/A	GaAs	R		0.00	0	0	0	0
VLSI TECHNOLOGY	SAN ANTONIO	TX	MODULE B	ARRAYS CBIC SRAM MPU E2	CMOS M3	F	06/01/90	0.80	6	6400	175241	7000
WESTERN DIGITAL	COSTA MESA	CA	DVLPMNT	CUSTOM	CMOS M2	F	09/01/90	1.25	6	6400	175241	12000
ZILOG	NAMPA	ID	MOD 3	N/A	N/A	F		1.00	6	8000	219052	12000
** Production Begins 1991												
CYPRESS S/C TEXAS INC.	ROUNDROCK	TX	FAB 3	N/A	CMOS	F		0.70	6	8000	219052	0
DIGITAL EQUIPMENT	SAN JOSE	CA	N/A	N/A	N/A	P		0.80	6	3200	87621	10000
GENESIS MICROCHIP	MARKHAM, ONTARIO	CN	N/A	PLD ARRAYS CBIC CUSTOM	CMOS M2	F	11/01/91	1.00	6	8000	219052	12000
HARRIS S/C	MELBOURNE	FL	N/A	N/A	N/A	F	11/01/91	0.00	6	0	0	0
IBM	SAN JOSE	CA	N/A	N/A	N/A	R		0.80	8	9000	437584	25000
IBM	HOPEWELL JUNCTION	NY	ASDC/ALF	64Mb DRAM	SOR LITHO.	R	06/01/91	0.50	8	0	0	0
IDT	SALINAS	CA	FAB 4	SRAM LOG DSP FIFO	CMOS	F		0.70	6	10800	295720	14000
MOTOROLA	CHANDLER	AZ	BP-6	ECL 50K ARRAYS	ECL BIP BICMOS	F	05/01/91	1.00	6	20000	547629	25000
MOTOROLA	CHANDLER	AZ	BP-6	ARRAYS CBIC	BIP BICMOS ECL	R	02/01/91	0.80	0	0	0	0
MOTOROLA	OAK HILL	TX	MOS-11	4Mb DRAM MCU MPU RISC	CMOS TOSH18A	F	05/01/91	0.80	6	17000	465485	35000
NEC	ROSEVILLE	CA	PHASE 2	4Mb DRAM	CMOS	FAT	08/01/91	0.70	8	16000	777927	70000
RICOH	SAN JOSE	CA	N/A	N/A	N/A	R		1.00	6	9600	262862	15000
SAMSUNG S/C	N/A	CA	N/A	DRAM SRAM FIFO PLD	CMOS	F	02/01/91	0.00	6	30000	821444	45000

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Company	City	St.	Fab Name	Products	Process Technology	Fab Type	Target Date Prod. Begins	Min. Line-width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. In. Start Capacity (4 wks.)	Clean Room (Square Feet)
SGS-THOMSON	SCOTTSDALE	AZ	N/A	1Mb EPROM	CMOS	F	02/01/91	1.00	6	12000	328577	22000
SHARP MICROELECT.	CAMUS	WA	N/A	1Mb SRAM FIFO ROM DSP	N/A	F	11/01/91	1.00	6	9600	262862	20000
SIGNETICS	OREM	UT	FAB 18	N/A	BIP	F	11/01/91	1.00	6	12000	328577	20000
SONY	SAN ANTONIO	TX	FAB 12	1Mb SRAM	CMOS BICMOS	F	03/01/91	0.80	6	12800	350483	17500
TI	DALLAS	TX	CMOS 5.1	4Mb DRAM	CMOS	F	06/01/91	0.80	8	16000	777927	25000
U.C. DAVIS	DAVIS	CA	N/A	N/A	N/A	R		0.00	0	0	0	15000
UNITED Si STRUCTURES	N/A	N/A	N/A	CBIC ARRAYS CUSTOM	N/A	P		0.00	0	0	0	0
VLSI TECHNOLOGY	SAN ANTONIO	TX	MODULE C	ARRAYS CBIC SRAM MPU E2	CMOS M3	F	09/01/91	0.80	6	6400	175241	7000
** Production Begins 1992												
ACTEL	N/A	N/A	N/A	PROGRAMABLE ARRAYS	CMOS	F		0.00	0	0	0	0
EXAR	FREMONT	CA	N/A	LIN DSP MPU	CMOS	F		1.00	6	0	0	0
INTEL	RIO RANCHO	NM	FAB 9.3	586 MPU EPROM	CMOS	F		0.80	6	24000	657155	25000
LSI LOGIC	MILPITAS	CA	N/A	ASIC	BICMOS	R		0.50	0	0	0	0
MITSUBISHI	DURHAM	NC	N/A	16Mb DRAM	N/A	F	11/02/92	0.60	8	14000	680687	0
NATIONAL S/C	ARLINGTON	TX	CMOS 3	N/A	CMOS	F		0.80	6	14400	394293	25000
NMB S/C	N/A	N/A	N/A	4Mb DRAM	CMOS	OF		0.80	0	0	0	0
OKI	TUALATIN	OR	N/A	ARRAYS	N/A	Q		0.00	0	0	0	0
SIERRA S/C	SAN JOSE	CA	N/A	N/A	N/A	F		0.80	6	0	0	0
TOSHIBA	WEST COAST	N/A	N/A	4Mb DRAM RISC MPU ASIC	CMOS	F		0.80	6	17000	465485	40000

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North American Fab Database
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Company	City	St.	Fab Name	Products	Process Technology	Fab Type	Target Date Prod. Begins	Min. Line-width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. In. Start Capacity (4 wks.)	Clean Room (Square Feet)
VLSI TECHNOLOGY	SAN ANTONIO	TX	MODULE D	ARRAYS CBIC SRAM MPU E2	CMOS M3	F	11/01/92	0.60	6	6400	175241	7000
** Production Begins 1993												
HP	CORVALLIS	OR	N/A	ASIC	N/A	F		0.00	6	0	0	20000
INTEL	ALOHA	OR	FAB 10	586 MPU	CMOS	F		0.00	8	21250	1033185	35000
MICRON TECHNOLOGY	N/A	N/A	FAB 4	4Mb DRAM	CMOS	F	02/01/93	0.80	0	0	0	0
TI	DALLAS	TX	MMST	ASIC	CMOS	P		0.50	6	800	21905	0
TI	DALLAS	TX	DMOS 5.2	16Mb DRAM	CMOS	F		0.00	8	16000	777927	25000
** Production Begins 1994												
AMD	AUSTIN	TX	FAB 25	N/A	N/A	F		0.35	8	15000	729307	0
CYPRESS S/C TEXAS INC.	ROUNDROCK	TX	FAB 4	N/A	CMOS	F		0.55	6	8000	219052	0
INTEL	RIO RANCHO	NM	FAB 9.4	N/A	CMOS	F		0.70	8	17000	826548	25000
LSI LOGIC	MILPITAS	CA	N/A	ASIC	BICMOS	F		0.50	0	0	0	0
MOTOROLA	OAK HILL	TX	N/A	16Mb DRAM	N/A	F	06/01/94	0.60	8	15000	729307	0
NEC	HILLSBORO	OR	PHASE 3	16Mb DRAM	CMOS	FAT		0.60	8	16000	777927	90000
OKI	TUALATIN	OR	N/A	ASIC DRAM	N/A	F		0.00	8	15000	729307	0
** Production Begins 1995												
CRYSTAL S/C	AUSTIN	TX	N/A	LIN A/D D/A	MOS	F		1.20	0	0	0	0
MAXIM INTEGRATED PROD.	SUNNYVALE	CA	N/A	OP AMPS A/D D/A	BIP CMOS	P		2.00	0	0	0	0
** Production Begins 1996												
SONY	SAN ANTONIO	TX	N/A	SRAM	CMOS	F		0.60	8	0	0	0

N/A = Not Available

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Company	Prefect.	Plant Name	Fab Name	Products	Process Technology	Fab Type	Target Date Prod. Begins	Min. Line-width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. In. Start Capacity (4 wks.)	Clean Room (Square Feet)
** Production Begins 1990												
FUJI ELECTRIC	NAGANO	MATSUMOTO	N/A	DIODE PWR TRAN PWR MOSFET	MOS	FAT		2.00	5	20000	380350	0
FUJI ELECTRIC	TOYAMA	MAIN OFFICE	N/A	DIODE	N/A	PAT		0.00	4	10000	121737	0
FUJITSU	FUKUSHIMA	WAKAMATSU	NO. 3	ARRAYS CBIC 32-bit MCU	CMOS	F	06/01/90	0.70	6	30000	821444	113000
FUJITSU	IWATE	IWATE	NO. 4	4Mb DRAM 1Mb SRAM ASIC	CMOS MOS P3	F	10/01/90	0.80	8	25000	1215512	0
FUJITSU	MIE	MIE	PROCESS LAB	BASIC RSCH.	N/A	R	05/01/90	0.00	0	0	0	0
HAMAMATSU PHOTONICS	SHIZUOKA	HAMAKITA R&D	N/A	OPTO	N/A	R	03/01/90	0.00	0	0	0	0
HITACHI	TOKYO	MUSASHI WORKS	N/A	4Mb DRAM 16Mb PROTO MCU	CMOS	P	09/01/90	0.80	8	8000	388964	0
HITACHI	YAMANASHI	KOFU WORKS	IMASUWA	4Mb DRAM 16Mb PROTO SRAM	CMOS	F	04/01/90	0.60	6	25000	684536	0
HITACHI	YAMANASHI	KOFU WORKS	IMASUWA	16Mb DRAM	N/A	P	07/01/90	0.50	8	8000	388964	0
HONDA	TOCHIGI	CENTRAL RSCH.	N/A	ENGINE CONTROL SENSORS	GaAs	P	03/01/90	0.00	3	0	0	0
IBM	SHIGA	N/A	N/A	1Mb 4Mb DRAM SRAM ASIC	N/A	F	04/01/90	0.80	8	20000	972409	40000
MATSUSHITA	TOYAMA	UOZU	FAB C-2	4Mb DRAM 256K SRAM	CMOS	F	05/01/90	0.80	6	20000	547629	0

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Company	Prefect.	Plant Name	Fab Name	Products	Process Technology	Fab Type	Target Date Prod. Begins	Min. Line-width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. In. Start Capacity (4 wks.)	Clean Room (Square Feet)
NEC	HIROSHIMA	CHUGOKU	PHASE 1	4Mb DRAM SRAM MPU 4Mb ROM	CMOS BICMOS	FAT	05/01/90	0.80	6	27000	739299	38754
NEC	KANAGAWA	SAGAMIHARA	BLDG G FLR2	16Mb DRAM	CMOS	PAT	02/01/90	0.55	8	5000	243102	20000
NIPPON DENSO	AICHI	KODA WORKS	BLDG. 2	MCU	MOS	F	12/01/90	0.00	6	10000	273815	0
NIPPON PRECISION CIRC.	TOCHIGI	SHIOBARA	N/A	A/D D/A DSP LOG ASSP	CMOS	P	02/01/90	0.80	6	20000	547629	21530
NIPPON SILICON	N/A	N/A	N/A	16Mb DRAM	N/A	R	09/01/90	0.60	0	0	0	0
NMB S/C	CHIBA	N/A	M3	4Mb DRAM	CMOS	OF	10/01/90	0.80	6	20000	547629	0
OKI	MIYAGI	MIYAGI OKI	N/A	4Mb DRAM VRAM 1Mb SRAM	CMOS	F	02/01/90	0.80	6	20000	547629	0
RICOH	OSAKA	N/A	N/A	ARRAYS	CMOS	NF		1.00	6	10000	273815	0
SANYO	GIFU	ULSI RSCH.	N/A	16Mb DRAM 64Mb LATER	CMOS	R	02/01/90	0.60	0	0	0	0
SANYO	GIFU	VLSI DIV.	N/A	256K SRAM 4Mb 8Mb ROM	N/A	F	04/01/90	0.80	0	0	0	0
SHARP	HIROSHIMA	FUKUYAMA	BLDG 2 #2	4Mb DRAM 16Mb ROM ASIC	CMOS	F	09/01/90	0.80	6	24000	657155	0
SHINDENGEN	YAMAGATA	HIGASHINE DIV.	BLDG 3	CUSTOM	CMOS MOS	F		0.00	5	10000	190175	0
SUMITOMO METAL MINING	OITA	N/A	N/A	N/A	N/A	P	10/01/90	0.00	5	3000	57052	5000
TOHOKU S/C	MIYAGI	SENDAI	PHASE 2	DRAM SRAM MPU	CMOS	F	11/01/90	0.80	6	15000	410722	42000

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Company	Prefect.	Plant Name	Fab Name	Products	Process Technology	Fab Type	Target Date Prod. Begins	Min. Line-width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. In. Start Capacity (4 wks.)	Clean Room (Square Feet)
TOSHIBA	OITA	OITA BLDG #4	#1	4Mb DRAM	CMOS	F	12/01/90	0.80	6	30000	821444	40000
TOYOTA	AICHI	CENTRAL LAB	N/A	MCU PWR ICs CUSTOM	CMOS BIP	PAT	03/01/90	2.00	5	500	9509	0
YAMAHA	KAGOSHIMA	KAGOSHIMA	N/A	ROM CBIC ASSP	CMOS	NF	08/01/90	1.00	6	14000	383340	0
** Production Begins 1991												
ASAHI MICRO SYSTEMS	MIYAZAKI	N/A	N/A	ASIC LIN A/D D/A ASSP	CMOS HITACHI	F		0.00	6	0	0	0
FUJI ELECTRIC	NAGANO	MATSUMOTO	N/A	N/A	N/A	RAT		0.00	0	0	0	0
FUJI ELECTRIC	YAMANASHI	YAMANASHI	N/A	LOG	CMOS	F		0.00	6	0	0	0
FUJITSU	MIE	MIE	NO. 4	16Mb DRAM 1Mb SRAM	N/A	P	11/01/91	0.60	8	10000	486205	0
FUJITSU	YAMANASHI	YAMANASHI ELECT	N/A	FET LIN OPTO	GaAs	F		0.00	4	0	0	0
FUJITSU/ISUZU	N/A	N/A	N/A	AUTOMOTIVE ICs	N/A	R		0.00	0	0	0	0
HITACHI	GUNMA	TAKASAKI WORKS	N/A	256K SRAM 4Mb DRAM MCU	CMOS	F	02/01/91	0.80	0	0	0	0
HITACHI MAXELL	IBARAGI	N/A	N/A	CHIP SETS	N/A	R	06/01/91	0.00	0	0	0	0
INTL. RECTIFIER	AKITA	AKITA	N/A	DIS	N/A	FAT		0.00	0	0	0	0
JPN. ATOM. ENRGY. RSCH.	N/A	N/A	N/A	SOR LITHO.	SOR LITHO.	R	08/01/91	0.00	0	0	0	0
KAWASAKI STEEL	TOCHIGI	PHASE 1	N/A	256K SRAM CBIC ARRAYS	CMOS NTT	NP	09/01/91	0.80	6	10000	273815	0
MATSUSHITA	OSAKA	S/C RSCH. CTR.	PROTOTYPE	16Mb DRAM 64-bit MPU	CMOS	P	02/01/91	0.60	0	0	0	0

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MITSUBISHI	EHIME	SAIJO A	N/A	4Mb DRAM	CMOS	FAT	02/01/91	0.80	6	20000	547629	60000
MITSUBISHI	HYOGO	KITAITAMI WORKS	N/A	N/A	N/A	F		0.00	4	0	0	0
MOTOROLA	FUKUSHIMA	AIZU WORKS	N/A	CONSUMER ICs	N/A	R	01/01/91	0.00	0	0	0	0
NEC	KUMAMOTO	KYUSHU	FAB 8	4Mb DRAM RISC MPU ARRAYS	CMOS BICMOS	F	11/01/91	0.80	8	20000	972409	40000
NIPPON STEEL	KANAGAWA	ELECT. LAB	N/A	ASIC	N/A	DP	09/01/91	0.80	0	0	0	0
OKI	MIYAGI	N/A	N/A	N/A	N/A	R	12/01/91	0.00	0	0	0	0
OKI	MIYAZAKI	MIYAZAKI OKI	M3	4Mb DRAM	CMOS	F	02/01/91	0.80	6	0	0	0
SANYO	NIIGATA	NIIGATA SANYO	BLDG 3 #4	16-BIT MCU DSP	CMOS	F		1.00	6	18000	492866	0
SEIKO-EPSON	YAMAGATA	TOHOKU EPSON	N/A	ARRAYS CBIC 1Mb SRAM	CMOS	MF	05/01/91	0.80	6	20000	547629	0
SONY	KANAGAWA	ATSUGI	N/A	MEM LIN OPTO DIS	GaAs CMOS	P		0.00	0	0	0	0
SONY	NAGASAKI	SONY NAGASAKI	3G	1Mb SRAM	N/A	F		0.80	0	40000	0	0
TI	IBARAGI	N/A	N/A	16Mb 64Mb DRAM HDTV ICs	N/A	R	06/01/91	0.50	0	0	0	0
TOSHIBA	IWATE	IWATE TOSHIBA	BLDG 3	ARRAYS CBIC	CMOS BICMOS	P	04/01/91	0.70	6	10000	273815	0
TOSHIBA	MIE	N/A	PHASE 1	4Mb DRAM SAMPLE 16Mb	CMOS	F	08/01/91	0.70	0	25000	0	40000
TOSHIBA	OITA	OITA BLDG #3	C-4 #2	4Mb DRAM	CMOS	F	03/01/91	0.80	6	15000	410722	0
TOSHIBA	OITA	OITA BLDG #4	#2	4Mb DRAM SAMPLE 16Mb	BICMOS CMOS	F		0.60	8	20000	972409	40000

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TOSHIBA	SHIGA	N/A	N/A	N/A	N/A	R	02/01/91	0.00	0	0	0	0
** Production Begins 1992												
KYOCERA	KYOTO	N/A	N/A	N/A	N/A	R	04/01/92	0.00	0	0	0	0
MITSUBISHI	KUMAMOTO	KUMAMOTO WORKS	D	ARRAYS CBIC ASSP MCU	N/A	F		0.00	0	0	0	0
MOTOROLA	MIYAGI	SENDAI	MOS-10	4Mb DRAM MPU CUSTOM	CMOS	F	04/01/92	0.80	6	25000	684536	25000
NEC	HIROSHIMA	CHUGOKU	PHASE 2	4Mb DRAM EPROM	CMOS	F	06/01/92	0.80	8	22000	1069650	0
NEW JAPAN RADIO	KUMAMOTO	KYUSHU	N/A	CUSTOM CONSUMER LOG	CMOS	F		1.00	6	20000	547629	0
NIHON S/C	IBARAGI	N/A	PHASE 2	ARRAYS CBIC RISC MPU	N/A	F	03/01/92	0.80	8	20000	972409	0
NKK	TOKYO	N/A	N/A	4Mb DRAM	N/A	P	03/01/92	0.80	6	3000	82144	0
NMB S/C	CHIBA	N/A	M4	4Mb DRAM SAMPLE 16Mb	BICMOS CMOS	OF		0.60	0	20000	0	0
SANYO	NIIGATA	NIIGATA SANYO	BLDG 3 #5	4Mb DRAM	CMOS	F	06/01/92	0.80	6	20000	547629	0
SONY	KAGOSHIMA	SONY KOKUBU	#5	LOG MEM MPU LIN DIS OPTO	BIP CMOS MOS	FAT		0.80	6	0	0	0
TDK/SILICON SYSTEMS	IBARAGI	N/A	N/A	ASIC MPR LOG A/D D/A	CMOS BIP	P		0.00	0	0	0	0
TI/KOBE STEEL	HYOGO	N/A	N/A	LOG ASIC	CMOS	F	06/01/92	0.80	0	0	0	0
TOSHIBA	MIE	N/A	PHASE 2	16Mb DRAM	CMOS	F		0.50	8	20000	972409	40000
TOSHIBA	OITA	OITA BLDG #4	#3	4Mb 16Mb DRAM	CMOS	F		0.80	8	20000	972409	40000

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Company	Prefect.	Plant Name	Fab Name	Products	Process Technology	Fab Type	Target Date Prod. Begins	Min. Line-width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. In. Start Capacity (4 wks.)	Clean Room (Square Feet)
** Production Begins 1993												
MITSUBISHI	EHIME	SAIJO D	N/A	16Mb DRAM	N/A	F		0.60	8	20000	972409	0
SEIKO-EPSON	NAGANO	FUJIMI	BLDG E	SRAM ARRAYS	CMOS	MFAT		0.00	0	0	0	0
SGS THOMPSON	N/A	N/A	N/A	DRAM	N/A	F		0.00	0	0	0	0
TOSHIBA	OITA	OITA BLDG #4	#4	16Mb DRAM	BICMOS CMOS	F		0.60	8	20000	972409	40000
** Production Begins 1994												
NEC	HIROSHIMA	CHUGOKU	PHASE 3	16Mb DRAM MPU EPROM	CMOS	F		0.60	8	22000	1069650	0
NKK	KANAGAWA	KEIHIN	PHASE 1	4Mb DRAM	N/A	F		0.80	6	0	0	0
TOSHIBA	MIE	N/A	PHASE 3	16Mb DRAM	CMOS	F		0.60	8	20000	972409	40000
** Production Begins 1995												
KAWASAKI STEEL	TOCHIGI	PHASE 2	N/A	SRAM DRAM ARRAYS	CMOS NTT	F		0.00	6	15000	410722	0
NEC	HIROSHIMA	CHUGOKU	PHASE 4	16Mb DRAM MPU EPROM	CMOS	F		0.60	8	22000	1069650	0
** Production Begins 1996												
TOSHIBA	MIE	N/A	PHASE 4	16Mb DRAM	CMOS	F		0.50	8	20000	972409	40000
** Production Begins 1997												
NKK	KANAGAWA	KEIHIN	PHASE 2	4Mb 16Mb DRAM	N/A	F		0.60	8	0	0	0

(Continued)

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Japanese Fab Database
Fab Activity Planned or Initiated to Begin Production During 1990 and Beyond (Continued)

Company	Prefect.	Plant Name	Fab Name	Products	Process Technology	Fab Type	Target Date Prod. Begins	Min. Line-width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. In. Start Capacity (4 wks.)	Clean Room (Square Feet)
** Production Begins 1999												
KAWASAKI STEEL	TOCHIGI	PHASE 3	N/A	16Mb DRAM SRAM ARRAYS	CMOS NTT	F		0.00	6	15000	410722	0
** Production Begins 2000												
NKK	KANAGAWA	KEIHIN	PHASE 3	16Mb DRAM	N/A	F		0.60	8	0	0	0

N/A = Not Available

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European Fab Database
Fab Activity Planned or Initiated to Begin Production During 1990 and Beyond

Company	City	Country	Fab Name	Products	Process Technology	Fab Type	Target Date Prod. Begins	Min. Line-width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. In. Start Capacity (4 wks.)	Clean Room (Square Feet)
** Production Begins 1990												
DIGITAL EQUIPMENT	QUEENSFERRY	SCOT.	N/A	DRAM	CMOS	P		1.00	6	3000	82144	28000
FUJITSU	NEWTON AYCLIFFE	ENGL.	N/A	ASIC	CMOS	F	12/01/90	1.00	6	25000	684536	0
TI	AVEZZANO	ITALY	PHASE 1	4Mb DRAM	CMOS	F	12/01/90	0.80	6	30000	821444	30000
TI	FREISING	W. GER.	N/A	LOG	CMOS	P	02/01/90	0.80	6	3000	82144	0
** Production Begins 1991												
ANALOG DEVICES	LIMERICK	EIRE.	N/A	LIN AD/DA TELECOM	BIP BICMOS	F	02/01/91	1.25	6	20000	547629	0
IBM	SINDELFINGEN	W. GER.	N/A	4Mb DRAM	CMOS	F	02/01/91	0.80	8	30000	1458614	45000
ITT	FREIBURG	W. GER.	N/A	DSP	CMOS	F		0.80	6	0	0	0
MOTOROLA	EAST KILBRIDE	SCOT.	MOS-12	4Mb DRAM	CMOS TOSHIBA	F		0.00	6	0	0	25000
NEC	LIVINGSTON	SCOT.	N/A	4Mb DRAM	CMOS	F	02/01/91	0.00	6	10000	273815	0
SAMSUNG	N/A	W. GER.	N/A	N/A	N/A	F		0.00	6	0	0	0
SGS-THOMSON	AGRATE	ITALY	VLSI LAB	N/A	N/A	R		0.00	0	0	0	0
TOSHIBA	BRAUNSCHWEIG	W. GER.	N/A	DRAM SRAM	CMOS	FAT		0.00	6	0	0	0
** Production Begins 1992												
ATMEL	N/A	NETH.	N/A	EPROM EEPROM	CMOS	P	12/01/92	0.60	8	5000	243102	0
FUJITSU	NEWTON AYCLIFFE	ENGL.	N/A	1Mb 4Mb DRAM	CMOS	F		1.00	6	45000	1232166	0
HITACHI	LANDSHUT	W. GER.	N/A	4Mb DRAM 256K 1Mb SRAM	N/A	F	05/01/92	0.80	6	16000	438103	0
MITSUBISHI	ALSDORF	W. GER.	N/A	4Mb DRAM MCU MPU ARRAYS	CMOS	F	03/01/92	0.80	6	22000	602392	25000
SONY	N/A	SCOT.	N/A	1Mb SRAM	CMOS	F		0.00	0	0	0	0
TI	AVEZZANO	ITALY	PHASE 2	16Mb DRAM	CMOS	F	02/01/92	0.60	8	20000	972409	30000

(Continued)

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European Fab Database
Fab Activity Planned or Initiated to Begin Production During 1990 and Beyond (Continued)

Company	City	Country	Fab Name	Products	Process Technology	Fab Type	Target Date Prod. Begins	Min. Line-width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. In. Start Capacity (4 wks.)	Clean Room (Square Feet)
** Production Begins 1993												
HITACHI	N/A	FRANCE	N/A	N/A	N/A	R		0.00	0	0	0	0
INTEL	LEIXLIP, KILDARE	EIRE.	FAB 11	N/A	N/A	F		0.00	6	0	0	35000
** Production Begins 1994												
FUJITSU	NEWTON AYCLIFFE	ENGL.	N/A	4Mb DRAM	CMOS	F		0.80	8	30000	1458614	0
MITSUBISHI	ALSDORF	W. GER.	N/A	4Mb DRAM MCU MPU ARRAYS	CMOS	F		0.80	8	18000	875168	25000

N/A = Not Available

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Asia/Pacific and Rest of World Fab Database
Fab Activity Planned or Initiated to Begin Production During 1990 and Beyond

Company	City or District	Country or Territory	Fab Name	Products	Process Technology	Fab Type	Target Date Prod. Begins	Min. Line-width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. In. Start Capacity (4 wks.)	Clean Room (Square Feet)
** Production Begins 1990												
HUALON MICROELECT.	HSINCHU	TAIWAN	FAB 2	MEM TELECOM SRAM	CMOS	F	05/01/90	0.00	6	30000	821444	0
HYUNDAI	ICHON	S. KOREA	S/C 4	1Mb DRAM 4Mb PROTO SRAM	CMOS	F	06/01/90	1.00	6	20000	547629	0
HYUNDAI	ICHON	S. KOREA	S/C 5	16Mb DRAM DEVELOP	BICMOS CMOS	R	03/01/90	0.60	0	0	0	0
INDIAN TELEPHONE	BANGALORE	INDIA	N/A	ARRAYS TELECON	CMOS VLSI	QAT	11/01/90	1.50	5	0	0	0
MOTOROLA	SEREMBAN	MALAYSIA	N/A	PWR TRAN DIS SST	N/A	FAT	02/01/90	0.00	6	8000	219052	6000
RAMAX	MELBOURNE	AUSTRALIA	N/A	FERRAM	CMOS GaAs	F		0.00	0	0	0	0
SAMSUNG	KIHEUNG	S. KOREA	FAB 4	4Mb DRAM SRAM ROM ASIC	CMOS	FAT	03/01/90	0.80	6	30000	821444	0
SID MICROELECT.	CONTAGEM	BRAZIL	N/A	PWR ICs	CMOS	F		2.00	4	13000	158258	15000
TSMC	HSINCHU	TAIWAN	FAB 2-A	SRAM ROM DRAM LOG CUSTOM	CMOS	OFAT	02/01/90	1.20	6	20000	547629	40000
** Production Begins 1991												
FORMOSA PLASTICS	N/A	TAIWAN	N/A	EPROM ROM	N/A	F		0.00	0	0	0	0
GOLDSTAR	CHONGJU	S. KOREA	PHASE 1	1Mb DRAM 256K SRAM	CMOS HITACHI	F	02/01/91	1.00	6	45000	1232166	0
HANILL	SIHEUNG	S. KOREA	N/A	N/A	GaAs	P	06/01/91	0.00	2	0	0	0
HYUNDAI	ICHON	S. KOREA	S/C 5	4Mb DRAM 16Mb PROTO	BICMOS CMOS	F	03/01/91	0.80	6	20000	547629	0

(Continued)

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Asia/Pacific and Rest of World Fab Database
Fab Activity Planned or Initiated to Begin Production During 1990 and Beyond (Continued)

Company	City or District	Country or Territory	Fab Name	Products	Process Technology	Fab Type	Target Date Prod. Begins	Min. Line-width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. In. Start Capacity (4 wks.)	Clean Room (Square Feet)
INTEL	PENANG	MALAYSIA	N/A	N/A	N/A	F		0.00	0	0	0	15000
MOSEL	HSINCHU	TAIWAN	FAB 1	256K SRAM	CMOS M3	F	04/01/91	1.00	6	10000	273815	10000
MOTOROLA	TIANJIN	CHINA	N/A	LOG DIS	BIP MOS	F	03/01/91	0.00	6	10000	273815	0
SAMSUNG	KIHEUNG	S. KOREA	FAB 5	4Mb DRAM	N/A	F	07/01/91	0.70	8	20000	972409	0
SAMSUNG	KIHEUNG	S. KOREA	N/A	N/A	GaAs GIGABIT	F	06/01/91	0.00	0	0	0	0
SHINDENGEN	N/A	THAILAND	N/A	TRAN DIODES	N/A	F	08/01/91	0.00	0	0	0	0
TI/ACER	HSINCHU	TAIWAN	FAB 1	1Mb DRAM	CMOS	FAT	06/01/91	1.00	6	30000	821444	30000
VITELIC	HSINCHU	TAIWAN	MODULE 1	DRAM SRAM	CMOS OKI	F	10/01/91	0.00	6	10000	273815	22000
WINBOND	HSINCHU	TAIWAN	FAB 2	SRAM ASIC	CMOS M2	F	03/01/91	1.20	6	30000	821444	0
WUXI FACTORY	WUXI	CHINA	N/A	16K SRAM 64K DRAM	MOS TOSHIBA	F	02/01/91	3.00	5	25000	475437	0
** Production Begins 1992												
TSMC	HSINCHU	TAIWAN	FAB 2-B	SRAM ROM DRAM LOG CUSTOM	CMOS	OF	02/01/92	1.00	6	20000	547629	40000
XICOR	N/A	ISRAEL	N/A	EPROM	CMOS	F		0.80	6	0	0	0
** Production Begins 1993												
GOLDSTAR	CHONGJU	S. KOREA	PHASE 2	4Mb DRAM 1Mb SRAM	CMOS	F		0.80	6	45000	1232166	0
SAMSUNG	KIHEUNG	S. KOREA	FAB 6	4Mb 16Mb DRAM	N/A	F	06/01/93	0.60	8	20000	972409	0
** Production Begins 1994												
MOSEL	HSINCHU	TAIWAN	FAB 2	1Mb SRAM	N/A	F		0.80	0	10000	0	10000

(Continued)

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Asia/Pacific and Rest of World Fab Database
Fab Activity Planned or Initiated to Begin Production During 1990 and Beyond (Continued)

Company	City or District	Country or Territory	Fab Name	Products	Process Technology	Fab Type	Target Date Prod. Begins	Min. Line-width	Waf. Size	Wafer Start Capacity (4 wks.)	Sq. In. Start Capacity (4 wks.)	Clean Room (Square Feet)
VITELIC	HSINCHU	TAIWAN	MODULE 2	DRAM SRAM	N/A	F		0.00	0	10000	0	22000
** Production Begins 1995												
ERSO	HSINCHU	TAIWAN	N/A	16Mb DRAM	N/A	R		0.00	6	1000	27381	0
SAMSUNG	KIHEUNG	S. KOREA	FAB 7	16Mb DRAM SAMPLE 64Mb	N/A	F		0.50	8	20000	972409	0
TI/ACER	HSINCHU	TAIWAN	FAB 2	4Mb 16Mb DRAM	CMOS	F		0.80	8	0	0	30000
** Production Begins 1996												
GOLDSTAR	CHONGJU	S. KOREA	PHASE 3	16Mb DRAM 4Mb SRAM	CMOS	F		0.60	8	45000	2187921	0
** Production Begins 1997												
SAMSUNG	KIHEUNG	S. KOREA	FAB 8	64Mb DRAM	N/A	F		0.35	8	0	0	0

N/A = Not Available

Source: Dataquest
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Definitions—Worldwide Fab Database

OVERVIEW

The definitions in this section apply to all of the regional fab database tables that follow it. These regional fab databases are updated on an ongoing basis with information generated by surveys, fab tours, research, industry sources, and the scanning of more than 30 periodicals related to the semiconductor industry. These tables include both silicon-based and compound semiconductor-based fab lines, but exclude semiconductor-related research and development (R&D) facilities. Our definitions for the types of fab lines in the following lists are as follows:

- A *Fab Line* is a processing line in a clean room that is equipped to do all front-end wafer processing. Occasionally there are two different wafer sizes or two separate product-specific fab lines in a single clean room. This clean room will be documented as two fab lines if the equipment is dedicated to each wafer size or product line. There can be many fab lines at one location.
- *Front-End* wafer processing is defined as all steps involved with semiconductor processing, beginning with the polished wafer and ending at the die probe stage.
- A *Production-Based Fab Line* is designed and used for medium- to high-volume semiconductor production.
  - Wafer-start capacity per four weeks at silicon-based production lines is usually not less than 10,000 wafers in the Asia/Pacific region and Japan and not less than 5,000 wafers in Europe and the United States
- A *Quick-Turn Line* personalizes gate arrays with the final metal interconnect.
  - These lines perform the last three to five mask levels of the front-end process
  - The base wafers come from another fab line
- A *Pilot and/or Prototype Line* is one of the following:
  - A fab line that performs process development and prototype production for the transition from R&D to volume production
  - A small fab line (usually owned by companies in niche markets) that operates at intended low volumes
  - A fab line intended for volume production that has begun initial production shipments and operates at less than one-third of its ultimate capacity

DEFINITIONS OF TABLE COLUMNS

The *Plant Name* column (used for Japan only) contains the name given to a plant location by the owner and/or company. The plant name may be the subsidiary name given by the parent company. In many cases, the plant name is not the same as the city or the prefecture in which the plant is located. Many fab lines can exist at one plant location.

The *Fab Name* column contains the internal and/or external name given to the fab line by the owner and/or company. Fab names are used to identify the individual fab lines at or within a plant location.

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The *Products Produced* column contains product information for seven product categories. The information in this column can be very detailed depending on the information's availability. The nomenclature used within the seven product groups of the fab database is as follows, with definitions where warranted:

- Analog
  - LIN—Linear/analog devices
  - A/D D/A—Analog-to-digital, digital-to-analog converters
  - AUTOMOTIVE—Dedicated to automobile applications
  - CODEC—Coder/decoder
  - INTERFACE—Interface IC
  - MESFET (GaAs)—Metal Schottky field-effect transistor
  - MODFET (GaAs)
  - MDIODE (GaAs)—Microwave diode
  - MFET (GaAs)—Microwave field-effect transistor
  - MODEM—Modulator/demodulator
  - MMIC—Monolithic microwave IC
  - OP AMP—Operational amplifier
  - PWR IC—Power IC
  - REG—Voltage regulator
  - SMART PWR—Smart power
  - SWITCHES—Switching device
  - TELECOM—Telecommunications chips
- Memory
  - MEM—Memory
  - RAM—Random-access memory
  - DRAM—Dynamic RAM
  - SRAM 4 TR.—Static RAM uses a 4-transistor cell design
  - SRAM 6 TR.—Static RAM uses a 6-transistor cell design
  - VRAM—Video RAM
  - ROM—Read-only memory
  - PROM—Programmable ROM
  - EPROM—Ultraviolet erasable PROM
  - EEPROM or E2—Electrically erasable PROM
  - FERRAM—Ferroelectric RAM
  - NVMEM—Nonvolatile memory (ROM, PROM, EPROM, EEPROM, FERRAM)
  - FIFO—First-in, first-out memory
  - SPMEM—Other specialty memory (dual port, shift-register, color look-up, etc.)
- Micrologic
  - ASSP—Application-specific standard product
  - BIT—Bit slice (subset of MPU functions)
  - DSP—Digital signal processor

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- MCU—Microcontroller unit
- MPR—Microperipheral
- MPRCOM—MPR digital communications (ISDN, LAN, UART, modem)
- MPU—Microprocessor unit
- LISP—32-bit list instruction set processor for AI applications
- RISC—Reduced-instruction-set computation 32-bit MPU

• Standard logic

- LOG—Standard logic

• ASIC logic

- ASIC—Application-specific IC
- ARRAYS—Gate arrays
- CBIC—Cell-based IC
- CUSTOM—Full-custom IC (single user)
- PLD—Programmable logic device

• Discrete

- DIS—Discrete
- DIODE
- FET—Field-effect transistor
- GTO—Gate turn-off thyristor
- HEMT (GaAs)—High-electron-mobility transistor
- MOSFET—MOS-based field-effect transistor
- PWR TRAN—Power transistor
- RECTIFIER
- RF—Radio frequency
- SCR—Schottky rectifier
- SENSORS
- SST—Small-signal transistor
- THYRISTOR
- TRAN—Transistor
- ZENER DIODE

• Optoelectronic

- OPTO—Optoelectronic
- CCD—Charge-coupled device (imaging)
- COUPLERS—Photocouplers
- IED—Infrared-emitting diode
- IMAGE SENSOR
- LASER (GaP)—Semiconductor laser or laser IC
- LED—Light-emitting diode
- PDIODE—Photo diode
- PTRAN—Photo transistor

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- SAW—Surface acoustic wave device
- SIT IMAGE SENSOR—Static induction transistor image sensor

The *Process Technology* column lists four major types of technologies. This column also lists a few uncommon technologies along with information on levels of metal, type of well, and logic structure, when available. Definitions of the nomenclature used in the *Process Technology* column are as follows:

- MOS (silicon-based)
  - CMOS—Complementary metal-oxide semiconductor
  - MOS—n-channel metal-oxide semiconductor (NMOS) and p-channel metal-oxide semiconductor (PMOS) (More than 90 percent of the MOS fabs use n-channel MOS.)
  - M1—Single-level metal
  - M2—Double-level metal
  - M3—Triple-level metal
  - N-WELL
  - P-WELL
  - POLY1—Single-level polysilicon
  - POLY2—Double-level polysilicon
  - POLY3—Triple-level polysilicon
- BiCMOS (silicon-based)
  - BICMOS—Bipolar and CMOS combined on a chip
  - BIMOS—Bipolar and MOS combined on a chip
  - ECL I/O—ECL input/output
  - TTL I/O—TTL input/output
- Bipolar (silicon-based)
  - BIP—Bipolar
  - ECL—Emitter-coupled logic
  - TTL—Transistor-transistor logic
  - STTL—Schottky TTL
- Gallium arsenide and other compound semiconductor materials
  - GaAs—Gallium arsenide
  - GaAlAs—Gallium aluminum arsenide
  - GaAs on Si—Gallium arsenide on silicon
  - GaP—Gallium phosphide
  - HgCdTe—Mercuric cadmium telluride
  - InAs—Indium arsenide
  - InP—Indium phosphide
  - InSb—Indium antimony
  - LiNbO3—Lithium niobate
  - SOS—Silicon on sapphire

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The number in the *Minimum Linewidth* column represents the minimum linewidth at the critical mask layers as drawn. This number is stated in microns and is defined in Dataquest's fab survey as being available in production volumes.

The *Wafer Size* column represents the wafer diameter expressed colloquially in inches. However, for wafers greater than 3 inches in diameter the colloquial expression is inaccurate. When calculating square inches, the following approximations are used:

Stated Diameter	Approximate Diameter
4 inches (100mm)	3.938 inches
5 inches (125mm)	4.922 inches
6 inches (150mm)	5.906 inches
8 inches (200mm)	7.87 inches

Wafer-Start Capacity is defined in the fab survey as the equipment-limited wafer-start capacity per four-week period. Start capacity is not limited by current staffing or the number of shifts operating; it is limited only by the installed equipment in the fab and the complexity of the process it runs. Start capacity in square inches is calculated using the approximate diameter and the wafer-start capacity.

The *Clean Room Class* column represents the level of cleanliness in the cleanest part of the clean room. This area represents the true environment to which the wafer is exposed.

The *Origin of Owner* column represents the country where the parent company is headquartered.

The *Merchant, Captive, Research* column categorizes each fab line on the tables as one of these three types. A fourth category, universities, is not on this list because all universities are considered R&D locations, which are not included in the following tables. In several instances, one company possesses both captive and merchant fab lines. Definitions of the various categories are as follows:

- A *Merchant* fab line is a fab line that produces devices that end up available on the merchant market.
- A *Captive* fab line does not sell any of its devices on the merchant market. All production is consumed by the owner of the fab line.
- A *Research* center is a facility that does not fit into the merchant, captive, or university definitions. A research center operates as a consortium or co-op, operates as a private lab, or is owned and operated by a government agency for the purpose of R&D and/or production.

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European Semiconductor Manufacturing

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European Fab Database
All Semiconductor Front-End Fab Lines Excluding R&D
(Includes New Fabs Going into Production during 1989)

Company	City	Country	Fab Name	Products Produced	Process Technology	Minimum Line-Width (drawn)	Wafer Size (inches)	Start Capacity, Square Inches (per four weeks)	Wafer Start Capacity (per four weeks)	Clean Room (square feet)	Clean Room Class	Origin of Owner	Mer., Cap., Res.
ABB-IXYS	JARFALLA	SWEDEN	N/A	MEM DIS OPTO	BIP CMOS	0.00	0	0	0	6000	0	U.S.	M
ABB-IXYS	LAMPERTHEIM	WEST GERMANY	N/A	DIS	BIP	15.00	3	113040	16000	0	100	U.S.	M
ACRIAN	BRIDGEND	WALES	N/A	MICROWAVE	BIP	0.00	0	0	0	0	0	U.S.	M
AMS	UNTERPREMSTATTN	AUSTRIA	N/A	ARRAYS CBIC CUSTOM	CMOS	0.00	0	0	0	0	0	AUSTRIA	M
ANALOG DEVICES	LIMERICK	EIRE	N/A	LIN AD/DA TELECOM	BIP BiCMOS	2.00	4	121737	10000	10000	10	U.S.	M
ANSALDO TRASPORTI	GENOA	ITALY	LINITA	PWR DIS	BIP	5.00	4	121737	10000	0	100	ITALY	
ASCOM FAVAG	BEVAIX	SWITZERLAND	N/A	ARRAYS CUSTOM	BIP	5.00	4	12174	1000	0	100	SWITZERLAND	M
ASIC	OOSTERGEN	NETHERLANDS	N/A	ARRAYS	BIP CMOS	2.00	6	0	0	0	0	NETHERLANDS	M
AT&T MICRO-ELECTRONICA	MADRID	SPAIN	N/A	CbIC CUSTOM	CMOS M2	1.25	6	383340	14000	25000	1	SPAIN/U.S.	M
BMMR BROWN	LIVINGSTON	SCOTLAND	N/A	LIN CUSTOM	BIP CMOS	0.00	0	0	0	0	0	U.S.	M
BMCS	DORTMUND	WEST GERMANY	N/A	LIN CUSTOM	CMOS	3.00	4	40695	4000	0	10	N/A	M
BS2	AIX-EN-PROVENCE	FRANCE	N/A	CBIC ARRAYS CUSTOM	CMOS M2	2.00	5	0	0	0	0	FRANCE	M
BURGSIL ELECTRONIC	ECHING	WEST GERMANY	N/A	LOG MPU MCU ARRAYS CUST	CMOS	3.00	4	292168	24000	3000	100	WEST GERMANY	M
FAVAG	BEVAIX	SWITZERLAND	N/A	CUSTOM	N/A	0.00	0	0	0	0	0	SWITZERLAND	M
GOULD-AMI-WEST-ALPINE	GRAZ	AUSTRIA	N/A	N/A	MOS	0.00	0	0	0	28000	0	WEST GERMANY/ JAPAN	M
HPT	BRUGG	SWITZERLAND	N/A	CONSUMER ICs	MOS	0.00	3	0	0	15000	0	SWITZERLAND	M
HUGHES MICRO-ELECTRONICS	GLENROTHES	SCOTLAND	N/A	ARRAYS CBIC EPROM CUSTOM	CMOS MOS	3.00	4	77911	6400	28000	100	U.S.	M
IBM	CORBEIL-ESSONNES	FRANCE	N/A	ARRAYS LIN CUSTOM	BIP	2.00	5	760699	40000	50000	0	U.S.	C
IBM	CORBEIL-ESSONNES	FRANCE	N/A	288K DRAM, 64K SRAM	CMOS MOS	1.00	5	475437	25000	25000	0	U.S.	C
IBM	CORBEIL-ESSONNES	FRANCE	N/A	1Mb DRAM	CMOS	0.00	8	340163	7000	0	0	U.S.	C
IBM	BOEBLINGEN	WEST GERMANY	N/A	PWR DIS HYBRID	BIP	0.00	0	0	0	0	0	U.S.	C
IBM	HANNOVER	WEST GERMANY	N/A	DIS	BIP	0.00	0	0	0	0	0	U.S.	C
IBM	SINDELFINGEN	WEST GERMANY	N/A	ARRAYS	BIP	2.00	5	285262	15000	20000	0	U.S.	C
IBM	SINDELFINGEN	WEST GERMANY	N/A	1Mb, 4Mb DRAM	CMOS	1.00	8	972409	20000	45000	0	U.S.	C
IBM	SINDELFINGEN	WEST GERMANY	N/A	288K DRAM, SRAM DSP MPU	MOS	1.50	5	475437	25000	20000	0	U.S.	C
IBM	SINDELFINGEN	WEST GERMANY	N/A	CUSTOM	BIP	1.50	5	285262	15000	20000	0	U.S.	C
INSTITUTE SCIENCE & TECH.	TRENTO	ITALY	N/A	CCD	CMOS	0.00	0	0	0	0	0	ITALY	R
INTERNATIONAL RECTIFIER	BORGARA TORINES	ITALY	N/A	DIS	N/A	0.00	0	0	0	13000	0	U.S.	M
INTERNATIONAL RECTIFIER	BORGARA TORINES	ITALY	N/A	DIS	N/A	0.00	0	0	0	0	0	U.S.	M
ISKRA	TRBOVLJE	YUGOSLAVIA	N/A	DIS	BIP	0.00	0	0	0	0	0	YUGOSLAVIA	M
ISOLON	HARTLEPOOL	ENGLAND	N/A	OPTO	GaAs	0.00	0	0	0	0	0	ENGLAND	M
ITALTEL	ROME	ITALY	N/A	N/A	GaAs	0.00	0	0	0	0	0	ITALY	M
ITT	FREIBURG	WEST GERMANY	N/A	PWR TRAN DIS	BIP MOS	5.00	4	511294	42000	0	1000	WEST GERMANY	M
ITT	FREIBURG	WEST GERMANY	N/A	DSP NMOS CUSTOM	CMOS MOS	1.20	5	408876	21500	0	10	WEST GERMANY	M
ITT	FREIBURG	WEST GERMANY	N/A	DIS CUSTOM	BIP	5.00	4	200865	16500	0	10	FRANCE	M
LSI LOGIC	FOOTSCRAY	ENGLAND	PHASE 1	ARRAYS CBIC LIN MPU	CMOS BICMOS	1.20	6	68454	2500	13000	10	U.S.	M

(Continued)

European Fab Database (Continued)
All Semiconductor Front-End Fab Lines Excluding R&D
(Includes New Fabs Going into Production during 1989)

Company	City	Country	Fab Name	Products Produced	Process Technology	Minimum Line-Width (drawn)	Wafer Size (inches)	Start Capacity, Square Inches (per four weeks)	Wafer Start Capacity (per four weeks)	Clean Room (square feet)	Clean Room Class	Origin of Owner	Mer., Cap., Res.
LSI LOGIC	BRAUNSCHWEIG	WEST GERMANY	N/A	ARRAYS	MOS	0.00	6	0	0	0	0	U.S.	M
LUCAS	SUTTON COLDFIELD	ENGLAND	N/A	PWR DIS	GaAs	0.00	0	0	0	54000	0	ENGLAND	M
MARCONI ELECTRONIC	LINCOLN	ENGLAND	N/A	LIN MPU ARRAYS SRAM CUST	CMOS MOS	1.50	4	158258	13000	12000	10	ENGLAND	M
MATRA-HARRIS	NANTES	FRANCE	N/A	256K SRAM MCP ARRAYS LIN	CMOS MOS M2	1.00	5	171157	9000	0	10	FRANCE/U.S.	M
MATRA-HARRIS	NANTES	FRANCE	N/A	LIN	BIP MOS	0.00	0	0	0	0	0	FRANCE	M
MICROELECTRONIC-MARIN	MARIN	SWITZERLAND	N/A	CUSTOM	N/A	0.00	0	0	0	0	0	SWITZERLAND	M
MICROELECTRONIC-MARIN	MARIN	SWITZERLAND	N/A	ARRAYS LIN CUSTOM	CMOS	3.00	4	121737	10000	0	10	SWITZERLAND	M
MICRONAS	ESPOO	FINLAND	N/A	LIN CMIC CUSTOM	BICMOS CMOS	2.50	4	24347	2000	0	10	FINLAND	C
MIETEC	OUDENAARDE	BELGIUM	N/A	ASIC	BIMOS CMOS MOS	2.40	4	674238	55305	0	10	BELGIUM	M
MIETEC	OUDENAARDE	BELGIUM	N/A	CUSTOM	MOS	0.00	0	0	0	0	0	BELGIUM	M
MISTRAL	SERMONETA	ITALY	N/A	DIS	N/A	0.00	0	0	0	0	0	ITALY	M
MITEL	NEWPORT	WALES	N/A	LIN OPTO CUSTOM	BIP	0.00	0	0	0	20000	0	WALES	M
MITEL	NEWPORT	WALES	N/A	CUSTOM	N/A	0.00	0	0	0	0	0	ENGLAND	M
MOTOROLA	TOULOUSE	FRANCE	BIP PWR	PWR TRAN	BIP	10.00	5	228210	12000	8700	100	U.S.	M
MOTOROLA	TOULOUSE	FRANCE	BP-4	TELECOM OP AMP REG AUTO	BIP	2.00	4	0	0	22000	100	U.S.	M
MOTOROLA	TOULOUSE	FRANCE	N/A	DIS	BIP	0.00	4	0	0	5800	0	U.S.	M
MOTOROLA	EAST KILBRIDE	SCOTLAND	MOS-3	MCU MEM LOG	CMOS MOS M3	3.00	4	0	0	25600	100	U.S.	M
MOTOROLA	EAST KILBRIDE	SCOTLAND	MOS-4	MCU MEM LOG	CMOS MOS	2.00	5	0	0	0	0	U.S.	M
MOTOROLA	EAST KILBRIDE	SCOTLAND	MOS-9	SRAM, 1MB DRAM 68040 MPU	CMOS TOSHIBA	1.00	6	0	0	34000	10	U.S.	M
MOTOROLA	EAST KILBRIDE	SCOTLAND	N/A	FET AMPS LKD MMIC	GaAs	0.00	0	0	0	0	0	U.S.	M
MULLARD	SOUTHAMPTON	ENGLAND	N/A	N/A	BIP MOS	0.00	0	0	0	0	0	ENGLAND	M
MULLARD	STOCKPORT	ENGLAND	N/A	DIS	N/A	0.00	0	0	0	0	0	ENGLAND	M
NATIONAL SEMICONDUCTOR	GREENOCK	SCOTLAND	BIP 4	LOG	BIP	5.00	4	486946	40000	10000	100	U.S.	M
NATIONAL SEMICONDUCTOR	GREENOCK	SCOTLAND	LOGIC	LOG	N/A	0.00	5	0	0	15000	0	U.S.	M
NATIONAL SEMICONDUCTOR	GREENOCK	SCOTLAND	UK 6"	LOG CUSTOM ARRAYS	BIP	1.50	6	191670	7000	10000	10	U.S.	M
NEC	LIVINGSTON	SCOTLAND	N/A	1MB DRAM SAMPLE 4MB	CMOS	1.20	6	328577	12000	39000	1	JAPAN	M
NEWMARKET MICROSYSTEMS	NEWMARKET	ENGLAND	N/A	LIN DIS	BIP	0.00	0	0	0	0	0	ENGLAND	M
PHILIPS	STOCKPORT	ENGLAND	PWR LABS	DIS	MOS	4.00	4	97389	8000	0	10	NETHERLANDS	M
PHILIPS	NIJMEGEN	NETHERLANDS	N/A	LIN	BIP	0.00	0	0	0	20000	0	NETHERLANDS	M
PHILIPS	NIJMEGEN	NETHERLANDS	N/A	1MB SRAM DEVELOPMENT	CMOS	0.70	6	479175	17500	0	0	NETHERLANDS	M
PHILIPS	NIJMEGEN	NETHERLANDS	N/A	N/A	CMOS	0.00	0	0	0	0	0	NETHERLANDS	M
PHILIPS	NIJMEGEN	NETHERLANDS	N/A	N/A	CMOS	0.00	0	0	0	0	0	NETHERLANDS	M
PHILIPS	NIJMEGEN	NETHERLANDS	N/A	PWR DIS	BIP	0.00	0	0	0	0	0	NETHERLANDS	M
PHILIPS	NIJMEGEN	NETHERLANDS	N/A	DIS	BIP	0.00	0	0	0	0	0	NETHERLANDS	M
PHILIPS	STADSKANAAL	NETHERLANDS	N/A	OPTO CUSTOM	GaAs MOS	0.00	0	0	0	0	0	NETHERLANDS	M

(Continued)

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European Fab Database (Continued)
All Semiconductor Front-End Fab Lines Excluding R&D
(Includes New Fabs Going into Production during 1989)

Company	City	Country	Fab Name	Products Produced	Process Technology	Minimum Line-Width (drawn)	Wafer Size (inches)	Start Capacity, Square Inches (per four weeks)	Wafer Start Capacity (per four weeks)	Clean Room (square feet)	Clean Room Class	Origin of Owner	Mer., Cap., Res.
PHILIPS	STADSKANAAL	NETHERLANDS	N/A	DIS OPTO	N/A	0.00	0	0	0	0	0	NETHERLANDS	M
PHILIPS	HAMBURG	WEST GERMANY	DISCRETE	DIS	BIP	7.00	3	141300	20000	0	100	NETHERLANDS	M
PHILIPS	HAMBURG	WEST GERMANY	N/A	1Mb DRAM	CMOS	1.20	0	0	0	0	0	NETHERLANDS	M
PHILIPS NATIONAL LABS	EINDHOVEN	NETHERLANDS	N/A	4Mb, 16Mb DRAM DEVELOPMENT	CMOS MOS	0.80	4	77911	6400	0	0	NETHERLANDS	R
PHILIPS/PASE&EC	ZURICH	SWITZERLAND	N/A	LOG MCU CUSTOM	CMOS	2.00	4	170431	14000	5000	10	NETHERLANDS	M
Piher	GRANOLLERS	SPAIN	N/A	DIS LIN	BIP	0.00	0	0	0	11000	0	SPAIN	M
PLESSEY SEMICONDUCTORS	OLDHAM	ENGLAND	CDI BIP	ARRAYS LIN CUSTOM	BIP	1.50	4	304341	25000	0	100	ENGLAND	M
PLESSEY SEMICONDUCTORS	OLDHAM	ENGLAND	N/A	CUSTOM	BIP MOS	0.00	0	0	0	26000	0	ENGLAND	M
PLESSEY SEMICONDUCTORS	OLDHAM	ENGLAND	N/A	LIN CUSTOM	BIP BICMOS	0.00	0	0	0	0	0	ENGLAND	M
PLESSEY SEMICONDUCTORS	PLYMPTON	ENGLAND	N/A	N/A	MOS	0.00	0	0	0	0	0	ENGLAND	M
PLESSEY SEMICONDUCTORS	ROBOROUGH	ENGLAND	N/A	ARRAYS CUSTOM BIT WAFIC	CMOS M2 MIL STD	1.40	6	164209	6000	0	10	ENGLAND	M
PLESSEY SEMICONDUCTORS	ROBOROUGH	ENGLAND	N/A	LIN LOG	MOS	2.00	4	24347	2000	0	100	ENGLAND	M
PLESSEY SEMICONDUCTORS	SWINDON	ENGLAND	N/A	DIODES DIS LIN	BIP	0.00	0	0	0	29000	0	ENGLAND	M
PLESSEY SEMICONDUCTORS	SWINDON	ENGLAND	N/A	LIN	BIP	0.00	0	0	0	0	0	ENGLAND	M
QUBOS	CAMBRIDGE	ENGLAND	N/A	ARRAYS	N/A	1.50	4	36521	3000	0	10	ENGLAND	M
RACAL	READING	ENGLAND	N/A	N/A	MOS	0.00	0	0	0	0	0	ENGLAND	M
RIFA	KALMAR	SWEDEN	N/A	PWR DIS	BIP	0.00	0	0	0	92000	0	SWEDEN	M
RIFA	KISTA	SWEDEN	N/A	N/A	BIP MOS	0.00	0	0	0	0	0	SWEDEN	M
ROBERT BOSCH	REUTLINGEN	WEST GERMANY	R&W/FAM	LIN DIS CUSTOM	BIP CMOS BICMOS	3.00	4	243473	20000	0	100	WEST GERMANY	C
RTC (PHILIPS)	CAEN	FRANCE	N/A	DIS LIN OPTO	GaAs	0.00	0	0	0	0	0	FRANCE	M
SGAGATE MICROELECTRONICS	LIVINGSTON	SCOTLAND	N/A	LIN	BIP	6.00	4	54781	4500	0	100	U.S.	C
SMEFAB	GLENROTHES	SCOTLAND	N/A	LIN DIS OPTO	BIP CMOS MOS	4.00	4	24347	2000	0	10	SCOTLAND	M
SEMITRON	CHICKLADE	ENGLAND	N/A	DIS	BIP	0.00	0	0	0	0	0	WEST GERMANY	M
SEMITRON	NURNBERG	WEST GERMANY	N/A	DIS	BIP	0.00	0	0	0	0	0	WEST GERMANY	M
SGS-THOMSON	AIX-EN-PROVENCE	FRANCE	N/A	DIS	N/A	0.00	3	0	0	0	0	ITALY	M
SGS-THOMSON	AIX-EN-PROVENCE	FRANCE	N/A	DIS	N/A	0.00	4	0	0	0	0	ITALY	M
SGS-THOMSON	GRENOBLE	FRANCE	N/A	LIN PWR IC CUSTOM	BIP CMOS	2.00	4	255647	21000	0	10	ITALY	M
SGS-THOMSON	MASSY	FRANCE	N/A	N/A	GaAs	0.00	0	0	0	0	0	ITALY	M
SGS-THOMSON	RENNES	FRANCE	N/A	LIN	BIP	5.00	5	228210	12000	0	10	ITALY	M
SGS-THOMSON	ROUSSET	FRANCE	MOD 4	MPU LIN	CMOS MOS	2.00	4	267820	22000	0	10	ITALY	M
SGS-THOMSON	ROUSSET	FRANCE	MOD 5	NVMEM MPU	CMOS MOS	1.50	5	304200	16000	0	1	ITALY	M
SGS-THOMSON	SAINT EGREVE	FRANCE	N/A	LIN CUSTOM	BIP	0.00	4	0	0	0	0	ITALY	M
SGS-THOMSON	TOURS	FRANCE	MESA	DIS	N/A	5.00	3	494550	78000	0	100	ITALY	M
SGS-THOMSON	TOURS	FRANCE	PLANAR	DIS	N/A	5.00	4	243473	20000	0	100	ITALY	M
SGS-THOMSON	AGRATE	ITALY	MMD	LIN	BIP BICMOS	4.00	5	304280	16000	22000	10	ITALY	M
SGS-THOMSON	AGRATE	ITALY	N/A	64K 256K 1Mb EPROM	CMOS	1.20	6	273815	10000	22000	0	ITALY	M
SGS-THOMSON	CATANIA	ITALY	N/A	DIS	N/A	3.00	5	646594	34000	0	100	ITALY	M

(Continued)

European Fab Database (Continued)
All Semiconductor Front-End Fab Lines Excluding R&D
(Includes New Fabs Going into Production during 1989)

Company	City	Country	Fab Name	Products Produced	Process Technology	Minimum Line-Width (drawn)	Wafer Size (inches)	Start Capacity, Square Inches (per four weeks)	Wafer Start Capacity (per four weeks)	Clean Room (square feet)	Clean Room Class	Origin of Owner	Ner., Cap., Reg.
SGS-THOMSON	CATANIA	ITALY	N/A	LOG LIN CUSTOM	CMOS	1.00	4	255647	21000	0	100	ITALY	M
SGS-THOMSON/[illegible]	NEWPORT	WALES	FZ1	SRAM LIN MPU DRAM MOS DSP	CMOS MOS	0.00	4	244471	20000	0	1	ITALY	M
SIEMENS	VILLACH	AUSTRIA	N/A	256K DRAM	MOS	1.20	0	0	0	0	0	WEST GERMANY	M
SIEMENS	VILLACH	AUSTRIA	N/A	64K DRAM LIN	MOS	2.00	4	0	0	0	0	WEST GERMANY	M
SIEMENS	CRICKLADE	ENGLAND	N/A	DIS	N/A	0.00	0	0	0	0	0	WEST GERMANY	M
SIEMENS	MUNICH	WEST GERMANY	N/A	ASIC CUSTOM LIN	BIP	0.00	0	0	0	0	0	WEST GERMANY	M
SIEMENS	MUNICH	WEST GERMANY	N/A	4Mb DRAM PROTO	CMOS	0.00	0	0	0	0	0	WEST GERMANY	M
SIEMENS	MUNICH	WEST GERMANY	N/A	ASIC CUSTOM	CMOS MOS	0.00	0	0	0	0	0	WEST GERMANY	M
SIEMENS	MUNICH	WEST GERMANY	N/A	N/A	BIP	0.00	0	0	0	0	0	WEST GERMANY	M
SIEMENS	REGENSBURG	WEST GERMANY	MEGA FAC	1Mb DRAM 4Mb DEVELOP	CMOS TOSHIBA	1.00	6	547629	20000	0	0	WEST GERMANY	M
SIEMENS	REGENSBURG	WEST GERMANY	N/A	DIS OPTO	N/A	0.00	0	0	0	0	0	WEST GERMANY	M
SILICONIX	SWANSEA	WALES	N/A	DIS	MOS	0.00	0	0	0	0	0	U.S.	M
STANDARD ELECTRICA	CASCAIS	PORTUGAL	N/A	DIS	N/A	0.00	0	0	0	0	0	PORTUGAL	M
STC SEMICONDUCTORS	SIDCUP, KENT	ENGLAND	N/A	ARRAYS LIN DRAM SRAM COST	BICMOS CMOS MOS BIP	2.00	4	36521	3000	0	10	ENGLAND/U.S.	M
TAG	ZURICH	SWITZERLAND	N/A	DIS	N/A	0.00	0	0	0	0	0	SWITZERLAND	M
TELEFUNKEN ELECTRONIC	HEILBRONN	WEST GERMANY	N/A	CUSTOM LIN DIS MCU	BIP MOS BICMOS CMOS	1.00	4	243473	20000	0	1	WEST GERMANY	M
TELEFUNKEN ELECTRONIC	HEILBRONN	WEST GERMANY	N/A	OPTO HIGH FREQUENCY	BIP	1.00	3	35325	5000	0	0	WEST GERMANY	M
TELEFUNKEN ELECTRONIC	HEILBRONN	WEST GERMANY	N/A	OPTO	GaAs	1.00	2	9420	3000	0	0	WEST GERMANY	M
TEXET	NICE	FRANCE	N/A	DIS	N/A	0.00	0	0	0	25000	0	FRANCE	M
TI	BEDFORD	ENGLAND	PWR FAB	PWR DIS	BIP	0.00	4	243473	20000	2500	100	U.S.	M
TI	FREISING	WEST GERMANY	N/A	LOG LIN	BIP	0.00	5	285262	15000	13000	100	U.S.	M
VAISALA	VANTAA	FINLAND	N/A	LIN	CMOS	5.00	3	1413	200	0	100	FINLAND	M
VEB CARL ZEISS JENA	N/A	EAST GERMANY	N/A	256K DRAM	CMOS	1.50	0	0	0	0	0	EAST GERMANY	R
VEB CARL ZEISS JENA	N/A	EAST GERMANY	N/A	N/A	N/A	1.00	4	0	0	0	0	EAST GERMANY	R
WESTCODE SEMICONDUCTOR	CHIPPENHAM	ENGLAND	N/A	DIS	N/A	0.00	0	0	0	0	0	ENGLAND	C
Total								15078892	951885	862600			

N/A = Not Available

Source: Dataquest
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Japanese Fab Data Base

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Japanese Fab Data Base

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Japanese Fab Data Base

OVERVIEW

Table 1 lists information on the fab lines in Japan. This information was generated by a three-month joint research project launched during 1988 between Dataquest's San Jose and Tokyo offices and by follow-up research that was completed recently.

The table presented here includes 181 production-based fab lines, 47 pilot lines, and 1 quick-turn fab. Fifteen of these fab lines will begin production during 1989. The table includes both silicon-based and compound semiconductor-based fab lines, but excludes semiconductor-related R&D facilities. Our definitions for the types of fab lines in the Japanese Fab Data Base are as follows:

- A Fab Line is defined as an individual clean room that is equipped to do all front-end wafer processing, except that occasionally two different wafer sizes or two separate product-specific fab lines operate in the same clean room. This clean room will be documented as two fab lines if the equipment is dedicated to each wafer size or product line. There can be many fab lines at one location.

- Front-End wafer processing is defined as all steps involved with semiconductor processing, beginning with the polished wafer and ending at the die probe stage.

- A Production-Based Fab Line is designed and used for medium- to high-volume semiconductor production.

  - Wafer start capacity per four weeks at silicon-based fab lines is usually not less than 10,000 wafers in Japan and 5,000 wafers in the United States.

  - The majority of these silicon-based fab lines in Japan have wafer capacities between 15,000 and 35,000 wafers per four weeks, whereas the U.S. counterparts have capacities between 5,000 and 25,000 wafers per four weeks.

- A Quick-Turn Fab Line personalizes gate arrays with the final metal interconnect.

  - These fab lines do the last three to five mask levels.

  - The base wafers come from another fab line.

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Japanese Fab Data Base

- A Pilot and/or Prototype Line is one of the following:
  - A small silicon-based fab line that operates at intended low volumes (i.e., start capacity in Japan is less than 15,000 wafers per four-week period and in most cases is usually less than 10,000, whereas the clear majority of U.S. pilot line volumes are less than 5,000 wafers per four-week period).
  - A fab line intended for volume production that has begun initial production shipments and operates at less than one-third of its ultimate capacity.
- A R&D and/or Trial Production Facility is not intended to produce devices that will be sold in the merchant market.
  - The range of research can be very specific or very diverse.
  - These facilities can be publicly owned, privately owned, or located at universities.
  - Some facilities may, on limited occasions, run very small lots to be sold to military contractors or for special projects.

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Table 1

Japanese Fab Data Base
All Semiconductor Front-End Fab Lines Excluding R&D

Company	Prefecture	City	Plant Name	Fab Name	Products Produced	Process Technology	Minimum Line Width (Drawn)	Wafer Size (Inches)	Start Capacity, Square Inches (per Four Weeks)	Wafer Start Capacity (per Four Weeks)	Clean Room (Square Feet)	Clean Room Class	Origin of Owner
CANON	KANAGAWA	HIRATSUKA-SHI	R&D CENTER	N/A	AMORPHOUS IMAGE SENSORS	GaAs	0.00	3	-	-	-	-	JAPAN
CANON	SHIGA	NAGAHAMA-SHI	NAGAHAMA WORKS	N/A	AMORPHOUS IMAGE SENSORS	GaAs	0.00	3	-	-	-	-	JAPAN
CANON DENSHI	SAITAMA	CHICHIBU-SHI	N/A	N/A	CCD	MOS	3.00	5	95087	5000	-	-	JAPAN
CLARION	FUKUSHIMA	KORIYAMA-SHI	S/C LAB	N/A	SAW CONVOLVER CUSTOM	N/A	0.00	4	60868	5000	-	-	JAPAN
FUJI ELECTRIC	NAGANO	MATSUMOTO-SHI	MATSUMOTO PLANT	N/A	LOG	CMOS MOS	2.00	5	380350	20000	-	100	JAPAN
FUJI ELECTRIC	NAGANO	MATSUMOTO-SHI	MATSUMOTO PLANT	N/A	DIODE PWR TRAN PWR MOSFET	MOS	4.00	4	243473	20000	-	-	JAPAN
FUJI ELECTRIC	NAGANO	MATSUMOTO-SHI	MATSUMOTO PLANT	N/A	DIS PWR MOSFET	MOS	3.00	4	73042	6000	-	-	JAPAN
FUJI ELECTRIC	NAGANO	MATSUMOTO-SHI	MATSUMOTO PLANT	N/A	LOG	CMOS	2.00	5	228210	12000	-	-	JAPAN
FUJI XEROX	MIE	SUZUKA-SHI	SUZUKA FUJI/XER	N/A	PWR ICs IMAGE SENSOR LOG	CMOS	3.00	5	57052	3000	-	-	JAPAN
FUJITSU	FUKUSHIMA	AIZU WAKAMATSU-SHI	AIZU F	VLSI 1	DIS A/D D/A	BIP	2.00	5	570524	30000	-	-	JAPAN
FUJITSU	FUKUSHIMA	AIZU WAKAMATSU-SHI	AIZU F	VLSI 2	256K DRAM SRAM EPROM MPU	MOS CMOS	1.50	5	760699	40000	-	-	JAPAN
FUJITSU	FUKUSHIMA	AIZU WAKAMATSU-SHI	AIZU F	VLSI 3	1Mb DRAM SRAM ROM	CMOS MOS	1.00	6	547629	20000	-	10	JAPAN
FUJITSU	FUKUSHIMA	AIZU WAKAMATSU-SHI	WAKAMATSU F	NO. 1	ARRAYS LOG	CMOS	1.50	5	722664	38000	-	-	JAPAN
FUJITSU	FUKUSHIMA	AIZU WAKAMATSU-SHI	WAKAMATSU F	NO. 2	ARRAYS LOG	CMOS	1.20	6	438103	16000	-	-	JAPAN
FUJITSU	FUKUSHIMA	AIZU WAKAMATSU-SHI	WAKAMATSU F	NO. 3	1Mb DRAM ASIC	CMOS	0.00	6	410722	15000	-	-	JAPAN
FUJITSU	GIFU	MINOKAMO-SHI	FUJITSU VLSI	MINOKAMO F	PROTOTYPE ICs	CMOS	1.00	6	136907	5000	-	10	JAPAN
FUJITSU	IWATE	IZAWA-GUN	IWATE F	NO. 1	ARRAYS	BIP	2.00	4	365210	30000	-	-	JAPAN
FUJITSU	IWATE	IZAWA-GUN	IWATE F	NO. 2	ROM EPROM	MOS	1.50	5	608559	32000	-	-	JAPAN
FUJITSU	IWATE	IZAWA-GUN	IWATE F	NO. 3	256K 1Mb DRAM SRAM ROM	CMOS MOS POLY3	1.00	6	821444	30000	-	-	JAPAN
FUJITSU	KANAGAWA	KAWASAKI-SHI	N/A	N/A	3D ICs JOSEPHSON JUNCTION	N/A	0.00	5	285262	15000	-	-	JAPAN
FUJITSU	MIE	KUWANA-GUN	MIE F	NO. 1	ARRAYS	CMOS MOS	1.00	6	273815	10000	-	10	JAPAN
FUJITSU	MIE	KUWANA-GUN	MIE F	NO. 2	LOG ARRAYS 4Mb DRAM PROTO	MOS CMOS	0.80	6	273815	10000	-	-	JAPAN
FUJITSU	MIE	KUWANA-GUN	MIE F	NO. 3	4Mb DRAM	CMOS	0.80	8	340343	7000	-	-	JAPAN
FUJITSU	MIYAGI	SHIBATA-GUN	MIYAGI	N/A	ASIC	CMOS	1.20	6	-	-	-	-	JAPAN
FUJITSU	YAMANASHI	NAKAKOMA-GUN	YAMANASHI ELECT	N/A	FET LIN OPTO	GaAs	0.00	3	-	-	-	-	JAPAN
HAMAMATSU PHOTONICS	SHIZUOKA	HAMAMATSU-SHI	N/A	N/A	OPTO	N/A	0.00	3	105975	15000	-	-	JAPAN
HITACHI	CHIBA	MOBARA-SHI	MOBARA WORKS	D1	256K DRAM	MOS CMOS	1.50	5	570524	30000	60000	-	JAPAN

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Table 1 (Continued)

Japanese Fab Data Base
All Semiconductor Front-End Fab Lines Excluding R&D

Company	Prefecture	City	Plant Name	Fab Name	Products Produced	Process Technology	Minimum Line Width (Drawn)	Wafer Size (Inches)	Start Capacity, Square Inches (per Four Weeks)	Wafer Start Capacity (per Four Weeks)	Clean Room (Square Feet)	Clean Room Class	Origin of Owner
HITACHI	CHIBA	MOBARA-SHI	MOBARA WORKS	D2	256K 1Mb DRAM	CMOS NOS	1.20	5	570524	30000	60000	-	JAPAN
HITACHI	CHIBA	MOBARA-SHI	MOBARA WORKS	D3	1Mb DRAM SAMPLE 4Mb	CMOS M2 N-WELL	0.80	6	821444	30000	60000	-	JAPAN
HITACHI	GUNMA	TAKASAKI-SHI	TAKASAKI WORKS	KOMORO	OPTICAL LASERS TELECOM	CMOS	1.50	5	285262	15000	20000	-	JAPAN
HITACHI	GUNMA	TAKASAKI-SHI	TAKASAKI WORKS	N/A	LIN EPROM PWR MOSFET SRAM	BIP NOS CMOS	2.00	5	380350	20000	-	-	JAPAN
HITACHI	HOKKAIDO	CHITOSE-SHI	HOKKAI S/C	CHITOSE F	64K 256K SRAM	CMOS	1.00	6	410722	15000	20000	-	JAPAN
HITACHI	IBARAGI	HITACHI-SHI	HITACHI WORKS	N/A	PWR GTO THYRISTORS	BIP STTL	4.00	5	380350	20000	-	-	JAPAN
HITACHI	IBARAGI	KATSUTA-SHI	NAKA WORKS	N/A	1Mb DRAM SAMPLE 4Mb	CMOS	1.00	6	547629	20000	20000	-	JAPAN
HITACHI	IBARAGI	KATSUTA-SHI	NAKA WORKS	N/A	1Mb DRAM 1Mb SRAM	CMOS	1.00	6	246433	9000	-	-	JAPAN
HITACHI	TOKYO	KODAIRA-SHI	MUSASHI WORKS	DDC	N/A	BIP	2.00	4	182605	15000	-	-	JAPAN
HITACHI	TOKYO	KODAIRA-SHI	MUSASHI WORKS	N/A	N/A	MOS	1.50	4	243473	20000	-	-	JAPAN
HITACHI	TOKYO	KODAIRA-SHI	MUSASHI WORKS	N/A	N/A	N/A	2.00	5	570524	30000	-	-	JAPAN
HITACHI	TOKYO	KODAIRA-SHI	MUSASHI WORKS	R&D	PROTO MPU &RAM DRAM ARRAY	CMOS	1.30	6	410722	15000	82352	-	JAPAN
HITACHI	TOKYO	KODAIRA-SHI	MUSASHI WORKS	R&D	PROTO MPU ASIC MEM	CMOS	1.20	5	285262	15000	-	10	JAPAN
HITACHI	YAMANASHI	NAKAKOMA-GUN	KOFU WORKS	LSI	N/A	MOS	3.00	4	365210	30000	-	-	JAPAN
HITACHI	YAMANASHI	NAKAKOMA-GUN	KOFU WORKS	NO. K4-2	1Mb DRAM	CMOS	1.00	6	547629	20000	-	-	JAPAN
HITACHI	YAMANASHI	NAKAKOMA-GUN	KOFU WORKS	NO. K2-1	N/A	N/A	2.00	4	182605	15000	-	-	JAPAN
HITACHI	YAMANASHI	NAKAKOMA-GUN	KOFU WORKS	NO. K2-2	N/A	MOS	2.00	5	380350	20000	-	-	JAPAN
HITACHI	YAMANASHI	NAKAKOMA-GUN	KOFU WORKS	NO. K3	64K SRAM	MOS	1.50	5	285262	15000	43006	-	JAPAN
HITACHI	YAMANASHI	NAKAKOMA-GUN	KOFU WORKS	NO. K4-1	MEM MPU LOG	MOS	2.00	5	380350	20000	-	-	JAPAN
HITACHI	YAMANASHI	NAKAKOMA-GUN	KOFU WORKS	NO. K4-3	16K 64K SRAM MPU	CMOS NOS	1.20	6	547629	20000	-	100	JAPAN
IBM	SHIGA	YASU-GUN	S/C RSRCH CTR	N/A	1Mb 4Mb DRAM	CMOS	0.00	8	388964	8000	-	-	U.S.
IBM	SHIGA	YASU-GUN	YASU WORKS	N/A	256K 1Mb DRAM 386 MPU ROM	MOS CMOS	1.00	5	570524	30000	50000	-	U.S.
INTERNATIONAL RECTIFIER	KANAGAWA	HATANO-SHI	HQ PLANT	N/A	MOSFET DIODE RECTIFIER	BIP	0.80	3	141300	20000	-	-	U.S.
INATSU	TOKYO	HACHIOJI-SHI	HACHIOJI BLDG	N/A	N/A	CMOS	1.50	5	114105	6000	-	-	JAPAN
JVC	KANAGAWA	YOKOHAMA-SHI	CENTRAL LAB	N/A	1K ARRAYS DSP CUSTOM	CMOS	3.00	3	63585	9000	-	-	JAPAN
KODAK	KANAGAWA	YOKOHAMA-SHI	MIDORI-KU	N/A	N/A	N/A	0.00	3	98910	14000	-	-	U.S.
KODENSHI	KYOTO-FU	UJI-SHI	N/A	PLANT 3	DIS P_DIODE P_TRAN	GaAs GaP	0.00	0	-	-	-	-	JAPAN
KYOTO SEMICONDUCTOR	KYOTO-FU	KYOTO-SHI	N/A	N/A	LED P_TRAN IMAGE SENSOR	GaAs GaP	0.00	0	-	-	-	10000	JAPAN
MATSUSHITA	KAGOSHIMA	HIOKI-GUN	KAGOSHIMA P	N/A	OPTO S/C LASERS LED	GaP MOS	0.00	0	-	-	-	10000	JAPAN

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Table 1 (Continued)

Japanese Fab Data Base
All Semiconductor Front-End Fab Lines Excluding R&D

Company	Prefecture	City	Plant Name	Fab Name	Products Produced	Process Technology	Minimum Line Width (Drawn)	Wafer Size (Inches)	Start Capacity, Square Inches (per Four Weeks)	Wafer Start Capacity (per Four Weeks)	Clean Room (Square Feet)	Clean Room Class	Origin of Owner
MATSUSHITA	KYOTO-FU	KYOTO-SHI	NAGAOKA F	IC	MEM MPU ARRAYS CBIC	MOS	2.00	4	182605	15000	-	1000	JAPAN
MATSUSHITA	KYOTO-FU	KYOTO-SHI	NAGAOKA F	LSI	LOG	CMOS	2.00	4	182605	15000	-	-	JAPAN
MATSUSHITA	KYOTO-FU	KYOTO-SHI	NAGAOKA F	N/A	TTL LOG PWR TRAN CUSTOM	BIP	3.00	4	243473	20000	-	10000	JAPAN
MATSUSHITA	KYOTO-FU	KYOTO-SHI	NAGAOKA F	N/A	CCD	MOS	2.00	4	97389	8000	-	1000	JAPAN
MATSUSHITA	KYOTO-FU	KYOTO-SHI	NAGAOKA F	VLSI	CCD FET	MOS	1.50	4	121737	10000	-	-	JAPAN
MATSUSHITA	KYOTO-FU	KYOTO-SHI	TOYO DENPA LTD.	N/A	PWR TRAN	MOS	0.00	5	342315	18000	-	-	JAPAN
MATSUSHITA	NIIGATA	ARAI-SHI	ARAI F	FAB B-3	64K DRAM SRAM MPU	MOS	2.00	5	855706	45000	-	-	JAPAN
MATSUSHITA	NIIGATA	ARAI-SHI	ARAI F	FAB C-1	MPU	MOS	1.50	4	182605	15000	-	-	JAPAN
MATSUSHITA	NIIGATA	ARAI-SHI	ARAI F	FAB C-2	256K DRAM SRAM MPU	MOS	1.50	5	665612	35000	-	100	JAPAN
MATSUSHITA	NIIGATA	ARAI-SHI	ARAI F	FAB D	LOG LIN CCD	BIP	3.00	5	380350	20000	-	100	JAPAN
MATSUSHITA	NIIGATA	ARAI-SHI	ARAI F	FAB D	N/A	MOS	1.50	5	380350	20000	-	-	JAPAN
MATSUSHITA	TOCHIGI	UTSUNOMIYA-SHI	APPLICA-TIONS LB	N/A	BST VARIABLE CAPAC. DIODE	MOS	0.00	3	56520	8000	-	-	JAPAN
MATSUSHITA	TOYAMA	UOZU-SHI	UOZU F	FAB A-1	16-BIT MPU ARRAYS CCD	CMOS	2.00	5	285262	15000	-	100	JAPAN
MATSUSHITA	TOYAMA	UOZU-SHI	UOZU F	FAB A-2	MPU	MOS	1.50	5	285262	15000	-	-	JAPAN
MATSUSHITA	TOYAMA	UOZU-SHI	UOZU F	FAB B	256K 1Mb DRAM	CMOS	1.00	6	547629	20000	-	10	JAPAN
MATSUSHITA	TOYAMA	UOZU-SHI	UOZU F	FAB C-1	1Mb DRAM SAMPLE 4Mb	CMOS	1.00	6	547629	20000	-	10	JAPAN
MEIDENSHA	SHIZUOKA	NAMAZU-SHI	N/A	N/A	GTO THYRISTOR	N/A	0.00	5	133122	7000	-	-	JAPAN
MITSUBISHI	EHIME	SAIJO-SHI	SAIJO B	N/A	256K 1Mb DRAM	CMOS	1.20	5	665612	35000	-	-	JAPAN
MITSUBISHI	EHIME	SAIJO-SHI	SAIJO C	N/A	256K 1Mb DRAM SAMPLE 4Mb	CMOS	0.80	6	821464	30000	43060	10	JAPAN
MITSUBISHI	FUKUOKA	FUKUOKA-SHI	FUKUOKA F	NO. 1	PWR TRN DIODE	BIP	4.00	4	486946	40000	-	-	JAPAN
MITSUBISHI	FUKUOKA	FUKUOKA-SHI	FUKUOKA F	NO. 2	LOG LIN A/D D/A	BIP	3.00	4	304341	25000	-	-	JAPAN
MITSUBISHI	HYOGO	ITAMI-SHI	KITAITAMI WORKS	N/A	ARRAYS OPTO LASER	CMOS MOS	2.00	5	532489	28000	7000	10	JAPAN
MITSUBISHI	HYOGO	ITAMI-SHI	KITAITAMI WORKS	N/A	FET OPTO	GaAs	0.00	3	-	-	-	-	JAPAN
MITSUBISHI	KOCHI	KAMI-GUN	KOCHI FACTORY	N/A	8-BIT 16-BIT MCU 1Mb DRAM	CMOS	1.00	6	273815	10000	-	10	JAPAN
MITSUBISHI	KOCHI	KAMI-GUN	KOCHI FACTORY	N/A	1Mb DRAM SAMPLE 1Mb SRAM	CMOS	1.00	6	328577	12000	-	-	JAPAN
MITSUBISHI	KOCHI	KAMI-GUN	KOCHI FACTORY	QUICK-TURN	ASIC	CMOS	1.30	6	136907	5000	-	-	JAPAN
MITSUBISHI	KUMAMOTO	KIKUCHI-GUN	KUMAMOTO WORKS	B-1F	EPROM	CMOS	1.50	5	570524	30000	-	-	JAPAN
MITSUBISHI	KUMAMOTO	KIKUCHI-GUN	KUMAMOTO WORKS	B-2F	ARRAYS	CMOS	2.00	4	511294	42000	-	-	JAPAN
MITSUBISHI	KUMAMOTO	KIKUCHI-GUN	KUMAMOTO WORKS	C-1F	EPROM	CMOS	1.50	5	475437	25000	-	-	JAPAN
MITSUBISHI	KUMAMOTO	KIKUCHI-GUN	KUMAMOTO WORKS	C-2F	256K SRAM 1Mb DRM	MOS CMOS	1.20	5	475437	25000	-	-	JAPAN
MITSUMI	KANAGAWA	ATSUGI-SHI	ATSUGI PLANT	N/A	LOG DIS	BIP	0.00	4	365210	30000	-	100	JAPAN

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Table 1 (Continued)

Japanese Fab Data Base
All Semiconductor Front-End Fab Lines Excluding R&D

Company	Prefecture	City	Plant Name	Fab Name	Products Produced	Process Technology	Minimum Line Width (Drawn)	Wafer Size (inches)	Start Capacity, Square Inches (per Four Weeks)	Wafer Start Capacity (per Four Weeks)	Clean Room (Square Feet)	Clean Room Class	Origin of Owner
MORIRICA	KANAGAWA	N/A	HEAD-QUARTER P	N/A	OPTO	GaP	0.80	0	-	-	-	-	JAPAN
MOTOROLA	FUKUSHIMA	YAMA-GUN	AIZU WORKS	MOS 7	CBIC MCU SRAM ROM PWR ICs	CMOS NOS M1	2.00	4	304341	25000	25000	100	U.S.
MOTOROLA	FUKUSHIMA	YAMA-GUN	AIZU WORKS	N/A	LOG	BIP	3.00	4	365210	30000	-	-	U.S.
NEC	KAGOSHIMA	IZUMI-SHI	KAGOSHIMA	N/A	LIN TELECOM LASER	BIP GaAs SI	0.78	4	51129	4200	-	-	JAPAN
NEC	KANAGAWA	KAWASAKI-SHI	TAMAGAWA WORKS	N/A	CCD IMAGE SENSOR LASER	GaAs	0.80	3	-	-	-	-	JAPAN
NEC	KANAGAWA	KAWASAKI-SHI	TAMAGAWA WORKS	N/A	256K DRAM	MOS	1.40	5	380350	20000	-	-	JAPAN
NEC	KANAGAWA	SAGAMIHARA-SHI	SAGAMIHARA	BLDG B FLR1	ARRAYS CBIC	MOS	2.00	5	532489	28000	-	-	JAPAN
NEC	KANAGAWA	SAGAMIHARA-SHI	SAGAMIHARA	BLDG B FLR2	ARRAYS CBIC SRAM EPROM	CMOS	1.25	5	380350	20000	-	-	JAPAN
NEC	KANAGAWA	SAGAMIHARA-SHI	SAGAMIHARA	BLDG G FLR1	4Mb DRAM ASIC	CMOS	0.80	8	656376	13500	-	-	JAPAN
NEC	KUMAMOTO	KUMAMOTO-SHI	KYUSHU	FAB 3	CCD	MOS	3.00	4	730419	60000	96005	-	JAPAN
NEC	KUMAMOTO	KUMAMOTO-SHI	KYUSHU	FAB 4	256K DRAM	MOS POLY2	1.40	5	760699	40000	60000	100	JAPAN
NEC	KUMAMOTO	KUMAMOTO-SHI	KYUSHU	FAB 6	256K 1Mb DRAM MPU ARRAYS	MOS POLY2	1.00	6	1232166	45000	50000	100	JAPAN
NEC	KUMAMOTO	KUMAMOTO-SHI	KYUSHU	FAB 7	ASIC 32-BIT MPU 1Mb DRAM	CMOS NOS	1.00	6	958351	35000	30000	10	JAPAN
NEC	SHIGA	RITTO-SHI	KANSAI LTD	NO. 1	PWR TRAN DIS CCD	BIP	4.00	4	182605	15000	-	1000	JAPAN
NEC	SHIGA	OTSU-SHI	KANSAI LTD	NO. 2	LIN CCD	BIP	3.00	4	243473	20000	-	1000	JAPAN
NEC	SHIGA	OTSU-SHI	KANSAI LTD	NO. 3	ARRAYS SRAM 8-BIT MPU	CMOS NOS	2.00	4	243473	20000	-	-	JAPAN
NEC	SHIGA	OTSU-SHI	KANSAI LTD	NO. 4	ARRAYS MPU 64K SRAM DRAM	CMOS	1.50	6	950351	35000	-	100	JAPAN
NEC	SHIGA	YOKAICHI-SHI	KANSAI LTD	YOKAICHI P	ZENER DIODE	BIP	5.00	4	243473	20000	-	1000	JAPAN
NEC	YAMAGATA	TSURUOKA-SHI	YAMAGATA LTD	TSURUOKA N	LOG LIN DIS	BIP	3.00	4	243473	20000	-	-	JAPAN
NEC	YAMAGATA	TSURUOKA-SHI	YAMAGATA LTD	TSURUOKA N	64K SRAM	MOS	2.00	4	243473	20000	-	-	JAPAN
NEC	YAMAGATA	TSURUOKA-SHI	YAMAGATA LTD	TSURUOKA W	LOG LIN	BIP	2.00	5	760699	40000	-	-	JAPAN
NEC	YAMAGUCHI	ASA-GUN	YAMAGUCHI LTD	PHASE 1	256K 1Mb DRAM SRAM MPU	CMOS NOS	1.00	6	547629	20000	-	10	JAPAN
NEC	YAMAGUCHI	ASA-GUN	YAMAGUCHI LTD	PHASE 2	4Mb DRAM 1Mb SRAM MPU	CMOS	0.80	6	547629	20000	24760	10	JAPAN
NEC	YAMANASHI	OTSUKI-SHI	OTSUKI WORKS	N/A	OPTO LED	N/A	2.00	5	570524	30000	-	100	JAPAN
NEW JAPAN RADIO	SAITAMA	KAMIFUKUOKA-SHI	KAWAGOE WORKS	N/A	OP AMP A/D D/A REG	BIP	0.80	5	323297	17000	-	1000	JAPAN
NEW JAPAN RADIO	SAITAMA	KAMIFUKUOKA-SHI	KAWAGOE WORKS	N/A	LED H_FET H_DIODE	GaAs GaAlAs	1.50	3	19782	2000	-	-	JAPAN
NEW JAPAN RADIO	SAITAMA	KAMIFUKUOKA-SHI	KAWAGOE WORKS	N/A	A/D D/A LOG CUSTOM OPTO	CMOS	2.00	5	380350	20000	-	-	JAPAN
NIHON SEMICONDUCTOR	IBARAGI	TUKUBAKITA-GUN	N/A	N/A	ARRAYS CBIC	CMOS	1.50	6	369650	13500	-	1	JAPAN/ U.S.
NIPPON DENSO	AICHI	KARIYA-SHI	HQ PLANT	N/A	DIODE LOG CUSTOM MCU	BIP MOS	3.00	4	243473	20000	-	-	JAPAN
NIPPON DENSO	AICHI	KARIYA-SHI	KODA WORKS	BLDG. 1	LOG CUSTOM MCU OPTO	MOS	1.50	5	38035	2000	-	-	JAPAN

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Table 1 (Continued)

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NIPPON PRECISION CIRCUITS	TOCHIGI	NASU-GUN	N/A	N/A	LOG LIN	CMOS	0.00	6	191670	7000	21530	-	JAPAN
NIPPON PRECISION CIRCUITS	TOCHIGI	NASU-GUN	N/A	N/A	LOG LIN A/D D/A	CMOS	2.00	5	247227	13000	32295	1000	JAPAN
NISSAN	KANAGAWA	YOKOSUKA-SHI	CENTRAL RSCH.	N/A	MCU CUSTOM	CMOS	2.00	5	9509	500	16140	10	JAPAN
NMB SEMICONDUCTOR	CHIBA	TATEYAMA-SHI	N/A	FAB 1	256K DRAM 64K SRAM	CMOS	1.20	5	380350	20000	43000	1	JAPAN
NMB SEMICONDUCTOR	CHIBA	TATEYAMA-SHI	N/A	FAB 2	1MD DRAM SRAM SAMPLE 4MD	CMOS M1	1.00	6	273815	10000	43000	1	JAPAN
OKI	MIYAGI	KUROKAWA-GUN	MIYAGI OKI	N/A	ARRAY 1MD DRAM SAMPLE 4MD	CMOS	1.00	6	547629	20000	-	10	JAPAN
OKI	MIYAZAKI	MIYAZAKI-GUN	MIYAZAKI OKI	M1	256K DRAM SRAM ARRAYS MPU	CMOS	1.50	5	950874	50000	-	100	JAPAN
OKI	MIYAZAKI	MIYAZAKI-GUN	MIYAZAKI OKI	M2	256K 1MD DRAM EEPROM	CMOS	1.30	5	570524	30000	30142	10	JAPAN
OLYMPUS	NAGANO	KANIIMA-GUN	TATSUNO NOARS	N/A	SIT IMAGE SENSOR	CMOS	3.00	5	95087	5000	-	-	JAPAN
ONKYO TATEISHI	SHIGA	KOUGA-GUN	MINAKUCHI P	N/A	OPTO IMAGE SENSOR	BIP GaP	3.00	4	12174	1000	14218	-	JAPAN
ONKYO TATEISHI	SHIGA	KOUGA-GUN	MINAKUCHI P	N/A	OPTO IMAGE SENSOR	BIP GaP	8.00	4	243473	20000	49734	-	JAPAN
ORIGIN ELECTRONICS	TOCHIGI	OHYAMA-SHI	N/A	N/A	TRAN DIODE DIS	BIP	0.80	4	206952	17000	-	-	JAPAN
PIONEER VIDEO CORP.	YAMANASHI	KOFU-SHI	N/A	N/A	ARRAYS LOG SAW CCD	CMOS	3.00	5	152140	8000	-	-	JAPAN
RICOH	OSAKA	IKEDA-SHI	N/A	N/A	ARRAYS ROM PLD LOG	BICMOS CMOS MOS	2.00	4	182605	15000	15286	100	JAPAN
RICOH	OSAKA	IKEDA-SHI	N/A	N/A	256K ROM ARRAYS CBIC	CMOS MOS	1.30	6	191670	7000	-	100	JAPAN
ROHM	FUKUOKA	YUKUHASHI-SHI	N/A	N/A	TRAN DIS	BIP	0.00	4	243473	20000	-	-	JAPAN
ROHM	FUKUOKA	YUKUHASHI-SHI	N/A	N/A	PWR ICs MPU MODEM	BIP	3.00	4	243473	20000	-	-	JAPAN
ROHM	KYOTO-FU	KYOTO-SHI	LSI RESEARCH	N/A	256K SRAM	CMOS	1.20	6	410722	15000	27000	-	JAPAN
ROHM	KYOTO-FU	KYOTO-SHI	MAIN OFFICE P	N/A	MPU LASER MODEM TRAN LED	BIP GaAs	0.00	4	304341	25000	-	-	JAPAN
ROHM	OKAYAMA	IHARA-SHI	SHINKO ELECTRIC	N/A	TRAN DIODE	BIP	0.00	3	162495	23000	-	1000	JAPAN
SANKEN	SAITAMA	NIIZA-SHI	HQ PLANT	N/A	PWR TRAN DIODE LED	N/A	0.00	3	105975	15000	-	1000	JAPAN
SANKEN	SAITAMA	NIIZA-SHI	S/C TECH. CTR.	N/A	PWR TRAN DIODE LED	N/A	0.00	5	114105	6000	-	-	JAPAN
SANKEN	YAMAGATA	HIGASHINE-SHI	YAMAGATA SANKEN	N/A	PWR TRAN DIODE LED	N/A	0.00	5	190175	10000	-	1000	JAPAN
SANSHA	OKAYAMA	KATSUTA-GUN	OKAYAMA F	N/A	PWR TRAN PWR DIODE	BIP	0.00	5	285262	15000	-	-	JAPAN

(Continued)

Table 1 (Continued)

Japanese Fab Data Base
All Semiconductor Front-End Fab Lines Excluding R&D

Company	Prefecture	City	Plant Name	Fab Name	Products Produced	Process Technology	Minimum Line Width (Drawn)	Wafer Size (Inches)	Start Capacity, Square Inches (per Four Weeks)	Wafer Start Capacity (per Four Weeks)	Clean Room (Square Feet)	Clean Room Class	Origin of Owner
SANYO	GIFU	ANPACHI-GUN	VLSI DIVISION	BUILDING F	CCD SRAM ARRAYS CBIC	CMOS	2.00	4	304341	25000	-	100	JAPAN
SANYO	GIFU	ANPACHI-GUN	VLSI DIVISION	BUILDING G	CCD ARRAY CBIC	CMOS	1.50	5	285262	15000	-	10	JAPAN
SANYO	GUNMA	OURA-GUN	S/C DIVISION	N/A	TRAN DIODE	N/A	4.00	4	486946	40000	53825	1000	JAPAN
SANYO	GUNMA	OURA-GUN	S/C DIVISION	N/A	N/A	BIP	2.00	4	365210	30000	69972	10	JAPAN
SANYO	GUNMA	OURA-GUN	S/C DIVISION	N/A	N/A	MOS	2.00	4	304341	25000	-	-	JAPAN
SANYO	NIIGATA	OJIYA-SHI	NIIGATA SANYO	BLDG 1	64K 256K DRAM 8-BIT MPU	CMOS	1.20	5	570524	30000	75355	10	JAPAN
SANYO	NIIGATA	OJIYA-SHI	NIIGATA SANYO	BLDG 2 BIP	LIN	BIP	2.00	5	475437	25000	37678	1000	JAPAN
SANYO	NIIGATA	OJIYA-SHI	NIIGATA SANYO	BLDG 2 CMOS	ASIC FLD 1Mb DRAM	BICMOS CMOS	1.00	6	438103	16000	-	-	JAPAN
SANYO	TOTTORI	TOTTORI-SHI	TOTTORI SANYO	N/A	LASER LED	GaAs GaP	5.00	3	141300	20000	32295	1000	JAPAN
SEIKO EPSON	NAGANO	SUWA-GUN	FUJIMI PLANT	A WING	ASIC 64K 256K SRAM EPROM	CMOS	1.50	5	532489	28000	-	100	JAPAN
SEIKO EPSON	NAGANO	SUWA-GUN	FUJIMI PLANT	B WING	ARRAYS CBIC SRAM EEPROM	CMOS MOS	2.00	4	486946	40000	-	100	JAPAN
SEIKO EPSON	NAGANO	SUWA-GUN	FUJIMI PLANT	BLDG C	SRAM ARRAYS	CMOS	2.00	5	380350	20000	-	-	JAPAN
SEIKO EPSON	NAGANO	SUWA-GUN	FUJIMI PLANT	BLDG D	ARRAYS CBIC 256K SRAM	CMOS	1.20	6	547629	20000	-	10	JAPAN
SEIKO INSTRUMENT	CHIBA	MATSUDO-SHI	TARATSUKA F	BLDG B	TELECOM	CMOS	2.00	5	190175	10000	-	-	JAPAN
SEIKO INSTRUMENT	CHIBA	MATSUDO-SHI	TARATSUKA F	N/A	SRAM ARRAYS CBIC EEPROM	CMOS	1.25	6	82144	3000	-	10	JAPAN
SHARP	HIROSHIMA	FUKUYAMA-SHI	FUKUYAMA PLANT	BLDG 1	1Mb DRAM SRAM ARRAYS ROM	MOS	1.80	5	665612	35000	37678	10	JAPAN
SHARP	HIROSHIMA	FUKUYAMA-SHI	FUKUYAMA PLANT	BLDG 2	1Mb DRAM 16Mb ROM CCD	CMOS	0.80	6	547629	20000	-	1	JAPAN
SHARP	NARA	KITAKATSURAGI-GUN	SHINJO PLANT	N/A	P_DIODE P_TRAN COUPLERS	N/A	0.00	4	304341	25000	-	-	JAPAN
SHARP	NARA	TENRI-SHI	IC TECH. CTR.	N/A	ARRAYS	CMOS	0.80	6	136907	5000	-	10	JAPAN
SHARP	NARA	TENRI-SHI	TENRI PLANT	NO. 1	LOG MEM LIN	BIP	3.00	4	243473	20000	-	-	JAPAN
SHARP	NARA	TENRI-SHI	TENRI PLANT	NO. 2	DRAM ROM	CMOS MOS	2.00	4	243473	20000	-	-	JAPAN
SHARP	NARA	TENRI-SHI	TENRI PLANT	NO. 3	ARRAYS CBIC	CMOS MOS BIP	1.50	4	243473	20000	-	-	JAPAN
SHARP	NARA	TENRI-SHI	TENRI PLANT	NO. 4	N/A	MOS	1.50	5	190175	10000	-	-	JAPAN
SHARP	NARA	YAMATOKORIYAMA-SHI	NARA PLANT	N/A	LASER LED OPTO	GaAs	0.00	3	155430	22000	-	-	JAPAN
SHINDENGEN	AKITA	HONJO-SHI	AKITA DIV.	BLDG 1	DIODE THYRISTOR VARISTOR	BIP	0.00	4	243473	20000	-	-	JAPAN
SHINDENGEN	AKITA	HONJO-SHI	AKITA DIV.	BLDG 2	DIODE VARISTOR THYRISTOR	BIP	0.00	5	570524	30000	19377	-	JAPAN
SHINDENGEN	SAITAMA	HANNO-SHI	N/A	N/A	DIS LIN	BIP	0.00	4	121737	10000	-	1000	JAPAN
SHINDENGEN	SAITAMA	HANNO-SHI	N/A	N/A	PWR MOSFET LIN LOG	MOS BIP	2.00	5	418304	22000	20023	100	JAPAN

(Continued)

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Table 1 (Continued)

Japanese Fab Data Base
All Semiconductor Front-End Fab Lines Excluding R&D

Company	Prefecture	City	Plant Name	Fab Name	Products Produced	Process Technology	Minimum Line Width (Drawn)	Wafer Size (Inches)	Start Capacity, Square Inches (per Four Weeks)	Wafer Start Capacity (per Four Weeks)	Clean Room (Square Feet)	Clean Room Class	Origin of Owner
SHINDENGEN	YAMAGATA	HIGASHINE-SHI	HIGASHINE DIV.	BLDG 1	TRAN DIODE	N/A	8.00	4	182605	15000	-	1000	JAPAN
SHINDENGEN	YAMAGATA	HIGASHINE-SHI	HIGASHINE DIV.	BLDG 2 DIS.	TRAN DIODE LIN	BIP	0.00	5	570524	30000	27311	-	JAPAN
SHINDENGEN	YAMAGATA	HIGASHINE-SHI	HIGASHINE DIV.	BLDG 2 MOS	CUSTOM	CMOS MOS	2.00	5	475437	25000	27311	-	JAPAN
SHOWA DENKO	TOKYO	TOKYO	N/A	N/A	N/A	GaAs	0.00	0	-	-	-	-	JAPAN
SONY	KAGOSHIMA	KOKUBU-SHI	SONY KOKUBU	NO. 1	DIS	N/A	4.00	4	182605	15000	-	-	JAPAN
SONY	KAGOSHIMA	KOKUBU-SHI	SONY KOKUBU	NO. 2	DIS	N/A	3.00	4	182605	15000	-	-	JAPAN
SONY	KAGOSHIMA	KOKUBU-SHI	SONY KOKUBU	NO. 3	LIN A/D D/A	BIP	2.00	4	304341	25000	-	-	JAPAN
SONY	KAGOSHIMA	KOKUBU-SHI	SONY KOKUBU	NO. 4	SRAM MPU CCD	CMOS MOS	1.30	5	570524	38000	-	10	JAPAN
SONY	KAGOSHIMA	KOKUBU-SHI	SONY KOKUBU	CCD	CCD	MOS	1.50	4	243473	20000	-	-	JAPAN
SONY	KANAGAWA	ATSUGI-SHI	ATSUGI PLANT	N/A	FET LASER CCD	GaAs	0.00	3	-	-	-	-	JAPAN
SONY	KANAGAWA	ATSUGI-SHI	ATSUGI PLANT	N/A	ROM 2.4MB VRAM 4Mb SRAM	CMOS	1.20	6	328577	12000	-	100	JAPAN
SONY	KANAGAWA	ATSUGI-SHI	ATSUGI PLANT	N/A	LIN	BIP	2.00	4	292168	24000	-	-	JAPAN
SONY	NAGASAKI	ISAHAYA-SHI	SONY NAGASAKI	N/A	1Mb SRAM CCD	CMOS	1.00	6	547629	20000	25080	10	JAPAN
STANLEY	KANAGAWA	HADANO-SHI	STANLEY ELECT.	N/A	LASER LED	N/A	0.00	4	121737	10000	-	-	JAPAN
STANLEY	YAMAGATA	TSURUOKA-SHI	TSURUOKA WORKS	N/A	LED	N/A	0.00	3	84780	12000	-	-	JAPAN
SUMITOMO METAL INDUSTRIES	OSAKA	OSAKA-SHI	OSAKA WORKS	N/A	LED P_DIODE	GaAs	0.00	3	7065	1000	-	-	JAPAN
TI	IBARAGI	INASHIKI-GUN	MINO PLANT	MINO 4	64K DRAM VRAM CCD	MOS	2.00	4	243473	20000	20080	100	U.S.
TI	IBARAGI	INASHIKI-GUN	MINO PLANT	MINO 5	256K DRAM	MOS	1.50	5	380350	20000	25000	1	U.S.
TI	IBARAGI	INASHIKI-GUN	MINO PLANT	MINO 6.1	256K 1Mb DRAM 256K SRAM	BICMOS CMOS MOS	1.00	6	650310	23750	30800	1	U.S.
TI	IBARAGI	INASHIKI-GUN	MINO PLANT	MINO 6.2	SRAM 1Mb DRAM SAMPLE 4MB	CMOS BICMOS	0.80	6	657155	24000	38000	1	U.S.
TI	OITA	ITSUMI-GUN	HIJI PLANT	BLDG 1	LOG LIN ARRAYS	BIP	3.00	4	608683	50000	-	-	U.S.
TI	OITA	ITSUMI-GUN	HIJI PLANT	BLDG 2	ARRAYS LISP MPU LIN	BICMOS CMOS	1.20	6	547629	20000	-	-	U.S.
TI	OITA	ITSUMI-GUN	HIJI PLANT	N/A	4Mb DRAM	CMOS	0.80	8	340343	7000	26912	-	U.S.
TI	SAITAMA	HATOGAYA-SHI	HATOGAYA PLANT	N/A	MCU DSP CBIC ARRAYS	CMOS MOS	2.00	5	285262	15000	-	100	U.S.
TI	SAITAMA	HATOGAYA-SHI	HATOGAYA PLANT	N/A	N/A	MOS	3.00	5	532489	28000	-	-	U.S.
TI	SAITAMA	HATOGAYA-SHI	HATOGAYA PLANT	N/A	N/A	BIP	3.00	4	219126	18000	-	-	U.S.
TOHOKU SEMICONDUCTOR	MIYAGI	IZUMI-SHI	SENDAI FACTORY	N/A	1Mb DRAM 256K SRAM MPU	CMOS	1.00	6	410722	15000	42000	10	JAPAN/ U.S.
TOKIN	MIYAGI	SENDAI-SHI	SENDAI WORKS	N/A	POWER SIT	BIP	0.00	3	70650	10000	-	-	JAPAN
TOKO	SAITAMA	IRUMA-GUN	SAITAMA PLANT	N/A	A/D D/A TELECOM DIODE	BIP	3.50	4	243473	20000	-	-	JAPAN
TOKO	SAITAMA	IRUMA-GUN	SAITAMA PLANT	N/A	N/A	MOS	3.00	4	182605	15000	-	-	JAPAN

(Continued)

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Table 1 (Continued)

Japanese Fab Data Base
All Semiconductor Front-End Fab Lines Excluding R&D

Company	Prefecture	City	Plant Name	Fab Name	Products Produced	Process Technology	Minimum Line Width (Drawn)	Wafer Size (Inches)	Start Capacity, Square Inches (per Four Weeks)	Wafer Start Capacity (per Four Weeks)	Clean Room (Square Feet)	Clean Room Class	Origin of Owner
TOSHIBA	CHIBA	KIMITSU-SHI	KIMITSU PLANT	PHASE 1	DIODE RECTIFIER THYRISTOR	BIP	0.00	4	243473	20000	-	-	JAPAN
TOSHIBA	CHIBA	KIMITSU-SHI	KIMITSU PLANT	PHASE 2	DIODE RECTIFIER THYRISTOR	BIP	0.00	5	342315	18000	-	-	JAPAN
TOSHIBA	FUKUOKA	KITAKYUSHU-SHI	KITAKYUSHU P	KUBIC 1	LASER LED	GaAs	2.00	3	176625	25000	17226	-	JAPAN
TOSHIBA	FUKUOKA	KITAKYUSHU-SHI	KITAKYUSHU P	KUBIC 2	ASIC OPTO LOG	BICMOS BIP	2.00	5	570524	30000	21530	100	JAPAN
TOSHIBA	FUKUOKA	KITAKYUSHU-SHI	KITAKYUSHU P	N/A	LIN	BIP	3.00	5	570524	30000	43060	-	JAPAN
TOSHIBA	FUKUOKA	NAKAMA-SHI	NIPPO INDUST.	NAKAMA P	LED P DIODE IMAGE SENSOR	N/A	0.00	4	365210	30000	-	-	JAPAN
TOSHIBA	HYOGO	HIMEJI-SHI	HIMEJI PLANT	N/A	TRAN DIODE	BIP	2.00	5	1407293	74000	-	-	JAPAN
TOSHIBA	HYOGO	HIMEJI-SHI	HIMEJI PLANT	N/A	TRAN DIODE	BIP	3.00	4	365210	30000	-	-	JAPAN
TOSHIBA	IWATE	KITAKAMI-SHI	IWATE TOSHIBA	PHASE 1	ARRAYS CBIC MPU CUSTOM	CMOS	1.50	5	380350	20000	-	100	JAPAN
TOSHIBA	IWATE	KITAKAMI-SHI	IWATE TOSHIBA	PHASE 2	4Mb ROM	CMOS	1.50	6	410722	15000	62437	100	JAPAN
TOSHIBA	IWATE	KITAKAMI-SHI	IWATE TOSHIBA	PHASE 2	ARRAYS CCD	CMOS	1.50	5	380350	20000	-	-	JAPAN
TOSHIBA	IWATE	KITAKAMI-SHI	IWATE TOSHIBA	PHASE 3	ASIC	CMOS	0.00	6	905732	36000	-	-	JAPAN
TOSHIBA	KANAGAWA	KAWASAKI-SHI	TAMAGAWA PLANT	N/A	1Mb DRAM SAMPLE 4Mb	CMOS	0.00	6	273815	10000	-	-	JAPAN
TOSHIBA	KANAGAWA	KAWASAKI-SHI	TAMAGAWA PLANT	N/A	LOG	BIP	2.00	5	285262	15000	-	-	JAPAN
TOSHIBA	OITA	OITA-SHI	OITA BLDG #1	LSI 1	MPU LOG 64K DRAM	MOS	2.00	4	243473	20000	-	-	JAPAN
TOSHIBA	OITA	OITA-SHI	OITA BLDG #1	LSI 2	MPU LOG ROM EPROM	CMOS MOS	1.50	5	855786	45000	-	-	JAPAN
TOSHIBA	OITA	OITA-SHI	OITA BLDG #2	C-1	256K 1Mb DRAM	CMOS MOS	1.00	5	570524	30000	-	100	JAPAN
TOSHIBA	OITA	OITA-SHI	OITA BLDG #2	C-2	256K 1Mb DRAM	CMOS	1.00	5	570524	30000	-	-	JAPAN
TOSHIBA	OITA	OITA-SHI	OITA BLDG #3	C-3 NO. 1	1Mb DRAM	CMOS	1.00	6	303340	14000	-	-	JAPAN
TOSHIBA	OITA	OITA-SHI	OITA BLDG #3	C-3 NO. 2	1Mb DRAM	CMOS	1.00	6	410722	15000	-	-	JAPAN
TOSHIBA	OITA	OITA-SHI	OITA BLDG #4	C-4 NO. 1	4Mb DRAM	CMOS	0.00	6	410722	15000	-	-	JAPAN
TOYO	KANAGAWA	YAMATO-SHI	TECHNICAL LAB	N/A	STATIC INDUCT. THYRISTOR	N/A	0.00	5	95087	5000	-	10	JAPAN
TOYOTA	AICHI	TOYOTA-SHI	CENTRAL LAB	N/A	MCU PWR ICs CUSTOM	CMOS	2.00	5	9509	500	-	100	JAPAN
UNISON	HYOGO	ITAMI-SHI	ITAMI PLANT	N/A	ZENER DIODE REG ARRAYS	BIP	0.00	5	285262	15000	-	-	JAPAN
YAMAHA	KAGOSHIMA	AIRA-GUN	KAGOSHIMA PLANT	N/A	LIN ROM CBIC	CMOS MOS	2.00	5	266245	14000	-	-	JAPAN
YAMAHA	KAGOSHIMA	AIRA-GUN	KAGOSHIMA PLANT	N/A	ROM CBIC ASSP	CMOS	1.20	5	665612	35000	-	10	JAPAN
YAMAHA	SHIZUOKA	HAMAMATSU-SHI	TOYOOKA WORKS	EE DEV CTR	CBIC LOG	CMOS	0.80	6	164289	6000	-	10	JAPAN
YAMAHA	SHIZUOKA	HAMAMATSU-SHI	TOYOOKA WORKS	N/A	CBIC LOG	CMOS	1.50	4	121737	10000	-	-	JAPAN
YOKOGAWA HOKUSHIN	TOKYO	MUSASHINO-SHI	N/A	N/A	CUSTOM	BIP	0.00	4	206952	17000	32295	-	JAPAN
YOKOGAWA INT	NAGANO	KITAINA-SHI	N/A	N/A	TRAN DIODE OPTO	N/A	0.00	4	34086	2800	-	-	JAPAN

N/A = Not Available

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Japanese Fab Data Base

DEFINITIONS OF TABLE COLUMNS

The Plant Name column contains the name given to a plant location by the owner and/or company. In many cases, the plant name is not the same as the city or the prefecture in which the plant is located.

The Fab Name column contains the internal and/or external name given to the fab line by the owner and/or company. Fab names are used to identify the individual fab lines at or within a plant location.

The Products Produced column contains product information for eight product categories. The information in this column can be very detailed depending on the information's availability. The nomenclature used within the eight product groups of the fab data base is as follows, with definitions where warranted:

- Analog
  - LIN—Linear/analog devices
  - A/D D/A—Analog-to-digital, digital-to-analog converters
  - AUTOMOTIVE—Dedicated to automobile applications
  - CODEC—Coder/decoder
  - INTERFACE—Interface IC
  - MESFET (GaAs)—Metal Schottky field-effect transistor
  - MODFET (GaAs)
  - M_DIODE (GaAs)—Microwave diode
  - M_FET (GaAs)—Microwave field-effect transistor
  - MODEM—Modulator/demodulator
  - MMIC—Monolithic microwave IC
  - OP AMP—Operational amplifier
  - REG—Voltage regulator
  - SWITCHES—Switching device
  - TELECOM—Telecommunications chips
- Memory
  - MEM—Memory
  - RAM—Random access memory
  - DRAM—Dynamic RAM
  - SRAM 4 TR.—Static RAM uses a 4-transistor cell design
  - SRAM 6 TR.—Static RAM uses a 6-transistor cell design
  - VRAM—Video RAM

- ROM—Read-only memory
- PROM—Programmable ROM
- EPROM—Ultraviolet erasable PROM
- EEPROM or E2—Electrically erasable PROM
- FERRAM—Ferroelectric RAM
- NVMEM—Nonvolatile memory (ROM, PROM, EPROM, EEPROM, FERRAM)
- FIFO—First-in, first-out memory
- SPMEM—Other specialty memory (dual port, color look-up, etc.)

• Micrologic

- ASSP—Application-specific standard product
- BIT—Bit slice (subset of MPU functions)
- DSP—Digital signal processor
- MCU—Microcontroller unit
- MPR—Microperipheral
- MPRCOM—MPR digital communications (ISDN, LAN, UART, modem)
- MPU—Microprocessor unit
- LISP—32-bit list instruction set processor for AI applications
- RISC—Reduced-instruction-set computation 32-bit MPU

• Standard logic

- LOG—Standard logic

• ASIC logic

- ASIC—Application-specific IC
- ARRAYS—Gate arrays
- CBIC—Cell-based IC

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Japanese Fab Data Base

- CUSTOM—Full-custom IC (single-user)
- PLD—Programmable logic device

- Discrete
  - DIS—Discrete
  - DIODE
  - FET—Field-effect transistor
  - GTO—Gate turn-off thyristor
  - HEMT (GaAs)—High-electron-mobility transistor
  - MOSFET—MOS-based field-effect transistor
  - PWR TRAN—Power transistor
  - RECTIFIER
  - RF—Radio frequency
  - SCR—Schottky rectifier
  - SENSORS
  - SST—Small-signal transistor
  - THYRISTOR
  - TRAN—Transistor
  - ZENER DIODE
- Optoelectronic
  - OPTO—Optoelectronic
  - CCD—Charge-coupled device (imaging)
  - COUPLERS—Photocouplers
  - IED—Infrared-emitting diode
  - IMAGE SENSOR

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- LASER (GaP)—Semiconductor laser or laser IC
- LED—Light-emitting diode
- P_DIODE—Photo diode
- P_TRAN—Photo transistor
- SAW—Surface acoustic wave device
- SIT IMAGE SENSOR—Static induction transistor image sensor

• Power IC

- PWR IC—Power IC
- SMART PWR—Smart power

The Process Technology column lists four major types of technologies. This column also lists a few uncommon technologies along with information on levels of metal, type of well, and logic structure, when available. Definitions of the nomenclature used in the Process Technology column are as follows:

• MOS (silicon-based)

- CMOS—Complementary metal-oxide semiconductor
- MOS—n-channel metal oxide semiconductor (NMOS) and p-channel metal oxide semiconductor (PMOS) (More than 90 percent of the MOS fabs use n-channel MOS.)
- M1—Single-level metal
- M2—Double-level metal
- M3—Triple-level metal
- N-WELL
- P-WELL
- POLY1—Single-level polysilicon
- POLY2—Double-level polysilicon
- POLY3—Triple-level polysilicon

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Japanese Fab Data Base

- BiCMOS (silicon-based)
  - BICMOS—Bipolar and CMOS combined on a chip
  - BIMOS—Bipolar and MOS combined on a chip
  - ECL I/O—ECL input/output
  - TTL I/O—TTL input/output
- Bipolar (silicon-based)
  - BIP—Bipolar
  - ECL—Emitter-coupled logic
  - TTL—Transistor-transistor logic
  - STTL—Schottky TTL
- Gallium arsenide and other compound semiconductor materials
  - GaAs—Gallium arsenide
  - GaAlAs—Gallium aluminum arsenide
  - GaAs on Si—Gallium arsenide on silicon
  - GaP—Gallium phosphide
  - HgCdTe—Mercuric cadmium telluride
  - InAs—Indium arsenide
  - InP—Indium phosphide
  - InSb—Indium antimony
  - LiNbO3—Lithium niobate
  - SOS—Silicon on sapphire

The number in the Minimum Line Width column represents the minimum line width at the critical mask layer as drawn. This number is stated in microns and is defined in Dataquest's fab survey as being available in production volumes.

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Japanese Fab Data Base

The Wafer Size column represents the wafer diameter expressed in inches. However, when the wafer diameter is larger than 3 inches and we are calculating square inches, the wafer diameter is defined in millimeters, as shown below:

Diameter	True Diameter
4 inches	100mm
5 inches	125mm
6 inches	150mm
8 inches	200mm

Wafer Start Capacity is defined in the fab survey as the equipment-limited wafer start capacity per four-week period. Start capacity is not limited by current staffing or the number of shifts operating; it is limited only by the installed equipment in the fab. Start capacity in square inches is calculated using the wafer size and the wafer start capacity.

The Clean Room Class column represents the level of cleanliness in the cleanest part of the clean room. This area represents the true environment to which the wafer is exposed.

The Origin of Owner column represents the origin of the owner and/or company.

SUPPLEMENTAL INFORMATION

Additional information and aggregate analysis based on the fab data base may be obtained by clients who use their inquiry privileges. dBASE III PLUS allows Dataquest to sort, count, list information, or run equations based on numerous fields and conditions. Inquiries to the Japanese Fab Data Base can produce lists that include or can be sorted by the columns in Table 1 or any of the following fields:

- Foundry supplier
- Facility type (see code definitions in Table 2)
- Year production began or had last upgrade
- Status of year production began or last upgrade (see status nomenclature in Table 3)

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Japanese Fab Data Base

Table 2

Code Definitions
Fab Field

Letter Code	Definition	Comments
F	Fab	Front-end processing; wafer start-up to die probe
P	Pilot line	Initial production or intended low volume
C	Quick-turn fab, personalizes gate arrays	Final mask layers only; base wafers from other location
R	Semiconductor research facility	Very small lot runs and R&D
A	Assembly	Back-end processing, sawing, and packaging
T	Test	Back-end processing; final device test
N	Nondedicated foundry service available	Excess capacity
O	Dedicated foundry supplier	Manufactures only customer designs
H	Headquarters	
UH	Foundry user headquarters address and company information	
U	Foundry user company name	All other information is on foundry supplier
K	Closed fab	
D	Design center	

Source: Dataquest
April 1989

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Table 3

Nomenclature and Definitions
Status Field

Nomenclature	Definition
NEW SHELL/CLEAN ROOM	Brand new from the ground up (green field)
NEW CLEAN ROOM	Building complete and ready for clean room installation
READY FOR EQUIPMENT	Clean room complete and ready for equipment installation
CLEAN ROOM EXPANSION	Increase of total square footage for an existing clean room
EQUIPMENT EXPANSION	Installation of additional equipment to an existing clean room
EXPANSION	Increase in total clean room square footage and installed equipment
CLEAN ROOM UPGRADE	Improved cleanliness, design, DI water, and/or vibration isolation
EQUIPMENT UPGRADE	Conversion to larger wafer size and/or finer line widths; equipment replacement, retrofit, and/or refurbishment
UPGRADE	Clean room and equipment upgrade
RERAMP FROM SHUTDOWN	Brought back into production from a shutdown

Source: Dataquest
April 1989

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Production

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Production

INTRODUCTION

Semiconductor production is the key economic activity that drives the market for capital spending and materials expenditures. Production refers to devices produced. On a worldwide basis, production and consumption of semiconductor devices are equal. However, on a regional basis they are not, because some of what is produced in one region is exported for consumption in another region.

Knowledge of production as opposed to consumption is important to equipment and materials vendors. Production is useful in understanding markets for semiconductor equipment and materials, where these markets are, and how they might grow. Production, and how it moves from one region to another, is also important to semiconductor manufacturers for competitive analysis and for planning manufacturing strategy.

In this service section, we will look at production by major regions of the world, identify major trends affecting production, and forecast the growth of production by region in the next five years. Regional consumption and production are defined as follows:

- Regional consumption--The final sales value of all devices consumed within one of the four major regions of North America, Japan, Europe, or ROW.

- Regional production--The final sales value of all devices fabricated within a region, even if the fabrication is owned by a nondomestic company. For example, we count as North American those production devices fabricated by NEC in North America. The value added by subsequent test and assembly, even if it occurs in another region, is assumed to be part of the production of that region where the fabrication occurred.

MERCHANT PRODUCTION AND MARKET SHARE

The worldwide production of merchant companies whose corporate headquarters are in North America (North American companies) is equal to their sales revenue. North American merchant companies have fabs not only in North America, but also in Asia and in Europe. Similarly, worldwide production of companies whose corporate headquarters are in Japan, Europe, or ROW (Japanese, European, or ROW companies) is equal to their sales revenue. Japanese, European or ROW merchant companies may also have fabs outside their geographic regions. Since worldwide merchant production is equal to merchant sales revenue, looking at shares of production is another way of looking at worldwide merchant market share.

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Production

Throughout most of the 1970s, North American merchant companies had a worldwide market share of production of over 60 percent (see Table 1 and Figure 1). During this same period, European companies had a worldwide share that hovered in the mid-teens and Japanese companies had about 25 percent of worldwide production. ROW companies were at that time but a footnote to market share tables.

Table 1

ESTIMATED WORLDWIDE MERCHANT MARKET SHARE

	1970	1971	1972	1973	1974	1975	1976	1977
North America	57%	61%	60%	59%	62%	64%	61%	61%
Japan	27%	22%	24%	26%	21%	19%	25%	25%
Europe	16%	17%	15%	14%	16%	16%	15%	14%
ROW	0	0	0	0	1%	0	0	0

	1978	1979	1980	1981	1982	1983	1984	1985
North America	55%	61%	61%	51%	51%	49%	48%	45%
Japan	28%	25%	26%	35%	35%	39%	40%	42%
Europe	16%	14%	13%	13%	13%	11%	11%	12%
ROW	0	0	0	0	1%	1%	1%	2%

	1986	1987	1988	1989	1990	1991
North America	39%	40%	40%	40%	40%	40%
Japan	47%	47%	47%	46%	46%	45%
Europe	11%	12%	12%	12%	12%	13%
ROW	2%	2%	2%	2%	2%	2%

Source: Dataquest
May 1987

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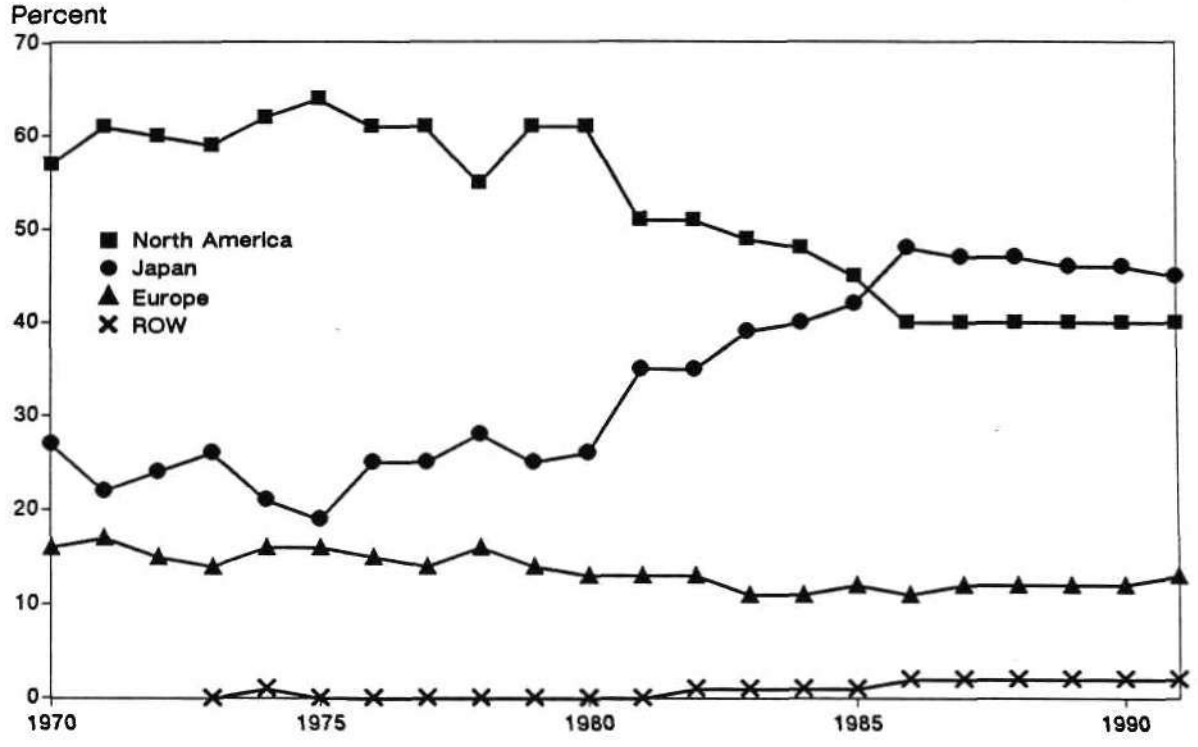
Production

Figure 1

ESTIMATED COMPANY SHARE OF WORLD MERCHANT MARKET



Source: Dataquest
February 1987

However, beginning in the early 1980s, all of this began to change. The most dramatic change was the swift ascent of Japanese companies and the corresponding breathtaking descent of North American merchant companies. Most of this movement took place in commodity memory devices where a combination of successful high volume production and price competition more or less drove North American merchant companies from the field. From 1978 to 1982, North American merchant companies' market share fell approximately 10 percent. During this same period, the value of the dollar versus the yen rose about 18 percent from 210 yen/dollar to 249 yen/dollar. Average sales

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prices as measured in dollars made Japanese products more attractive and, along with commodity manufacturing skill, helped lift Japanese share and depress North American share.

It should be noted, however, that if captives are added to North American market share numbers, the story is different. Although Japanese companies still gain share, the bottom line is that North American merchants plus North American captives still have significantly more worldwide share than do Japanese companies. In 1986, we estimate that total North American merchants plus North American captives had a 48 percent share of the total worldwide merchant and captive market. We do not expect these total share relationships to change in the next five years (see Table 2).

Table 2

ESTIMATED WORLDWIDE MERCHANT AND CAPTIVE MARKET SHARE

	1981	1982	1983	1984	1985
North America	59%	59%	57%	55%	54%
Merchant	43%	43%	42%	42%	39%
Captive	16%	16%	15%	12%	15%
Japan	30%	29%	33%	35%	35%
Europe	11%	11%	10%	10%	10%
ROW	0	1%	1%	1%	1%

	1986	1987	1988	1989	1990	1991
North America	48%	48%	48%	49%	49%	49%
Merchant	34%	35%	35%	34%	34%	35%
Captive	13%	13%	13%	14%	15%	14%
Japan	41%	41%	41%	40%	39%	38%
Europe	10%	10%	10%	10%	10%	11%
ROW	1%	1%	2%	2%	2%	2%

Source: Dataquest
May 1987

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Production

The early 1980s also saw the re-emergence of European companies as major players on the worldwide semiconductor scene. European companies and their governments began to recognize the strategic importance of semiconductors. An example of European government commitment to the semiconductor industry is the ESPRIT program to support research and development in information technology. Another example is the EURIKA research coordinating agency to coordinate development of advanced technologies. Thomson Semiconductor's acquisition of Mostek is another example of renewed European commitment to the industry. Siemens, Phillips/Signetics, and SGS have also demonstrated renewed commitment to the industry by engaging in production outside of Europe.

The early 1980's also saw ROW companies lay the groundwork for their emergence from the footnotes of worldwide market share tables.

In 1985, North American merchant companies' market share stood at 45 percent and Japanese companies' share stood at 42 percent. One year later, in 1986, their respective shares were 39 and 47 percent. The main reason for this stunning reversal was the surging strength of the yen versus the dollar. In 1985, the yen stood at 238 to the dollar; in 1986, it had grown to 167 to the dollar--a gain of 30 percent. The yen's strength had the net effect of increasing the dollar value of yen-based production.

Yen appreciation is responsible for the recent surge in the valuation of devices produced in Japan, and therefore the leap upward of Japanese market share. However, in the long run it will have a negative effect on demand. There are two reasons for this. One is that consumer electronics, as well as other semiconductor end-use items, will find price competition much tougher because of the stronger yen. This will lessen demand for Japanese end-use products that are heavy users of Japanese-produced semiconductors. A recent example of this process is General Electric's decision to begin domestic volume production of television sets after Matsushita had tried to increase prices for the sets it manufactures for General Electric.

Yen appreciation will also cut margins for Japanese semiconductor manufacturers. With reduced margins, it will be more difficult for Japanese manufacturers to compete on commodity prices; it will also accelerate their movement into higher-margined markets such as microdevices and ASICs. These markets, it should be noted, are areas where North American manufacturers can expect to have more strength and competitive resiliency than in the commodity markets.

Trade friction, renewed commitment on the part of European manufacturers and their governments, and the emergence of Hong Kong, Korea, Singapore, and Taiwan as centers of commodity production will combine to limit the growth of Japanese company market share in the next five years. Nevertheless, Dataquest expects Japanese companies to maintain their premier position in the merchant market.

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REGIONAL CONSUMPTION AND MARKET SHARE

The relationship between the value of devices consumed within a region and the value of devices produced by merchant companies headquartered within that region has varied. In North America, for example, the value of devices consumed in North America rose from a 38.0 percent share in 1978 to 47.0 percent in 1983 (slightly less than the value of dollar appreciation for that period--see Table 3). In the same period, the value of devices produced worldwide by North American merchant companies (their total worldwide share from Table 1) in North America plunged from a more than 55.0 percent share to a 49.0 percent share (see Table 1). Devices produced by North American merchant companies were losing their appeal to their North American consumers. At the same time, Japanese company sales into the North American merchant market rose from 4.4 to 12.6 percent in 1983 (see Figure 2).

While regional consumption and market share in North America diverged rather sharply from 1978 to 1983, Japanese share of worldwide merchant consumption and Japanese market share of the worldwide merchant market moved upward in unison (see Figures 3 through 5). Devices consumed in Japan tended to be produced in Japan by Japanese companies.

In Europe, consumption and market share also moved together, but the direction from late 1970s until 1985 was down. However, due to Europe's renewed commitment to electronics in general, and semiconductors in particular, we believe that the share of both the devices consumed in Europe and also those produced in Europe will rise.

Table 3

ESTIMATED REGIONAL CONSUMPTION

	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980
North America	42%	41%	44%	41%	42%	41%	39%	40%	38%	40%	42%
Japan	29%	27%	27%	25%	24%	23%	28%	25%	27%	25%	24%
Europe	27%	30%	26%	30%	29%	31%	27%	28%	26%	27%	26%
ROW	1%	2%	3%	4%	4%	5%	6%	7%	7%	7%	7%

	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991
North America	44%	46%	47%	46%	39%	33%	32%	33%	31%	30%	29%
Japan	29%	27%	29%	31%	35%	40%	40%	39%	39%	41%	41%
Europe	21%	21%	17%	17%	19%	18%	17%	17%	18%	17%	18%
ROW	7%	7%	8%	8%	8%	9%	11%	12%	12%	12%	12%

Source: Dataquest
May 1987

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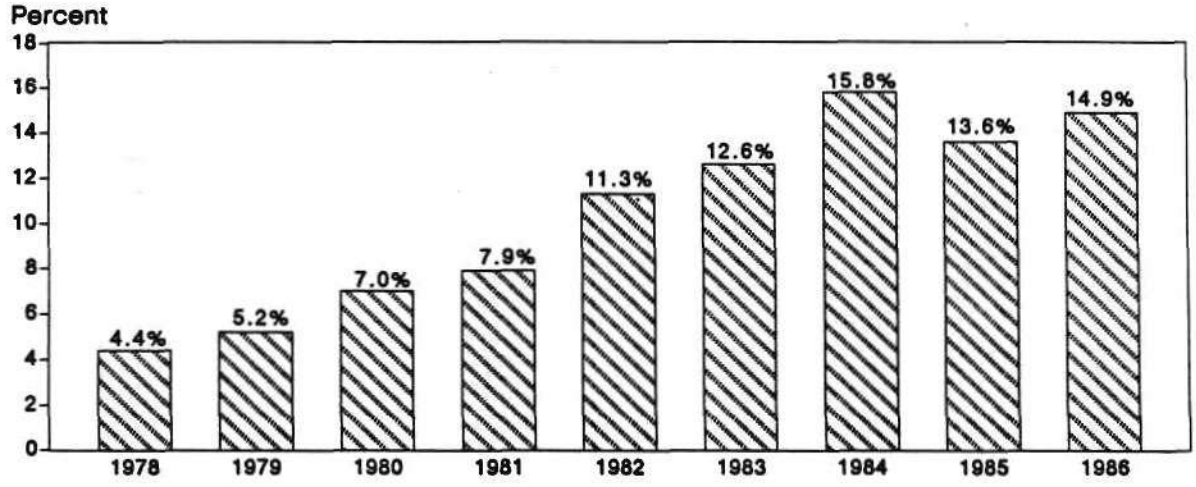
Figure 2

JAPANESE SHARE OF THE NORTH AMERICAN SEMICONDUCTOR MARKET



Source: Dataquest
April 1987

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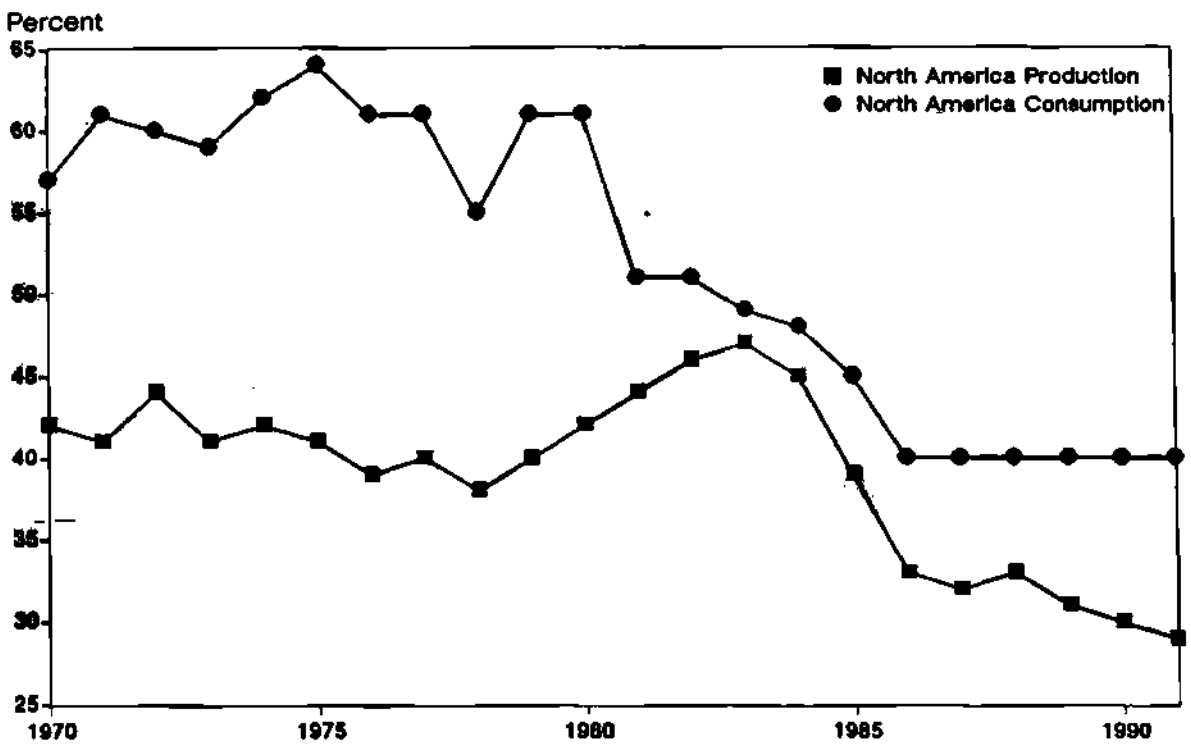
Figure 3

REGIONAL CONSUMPTION VERSUS REGIONAL MARKET SHARE



Source: Dataquest February 1987

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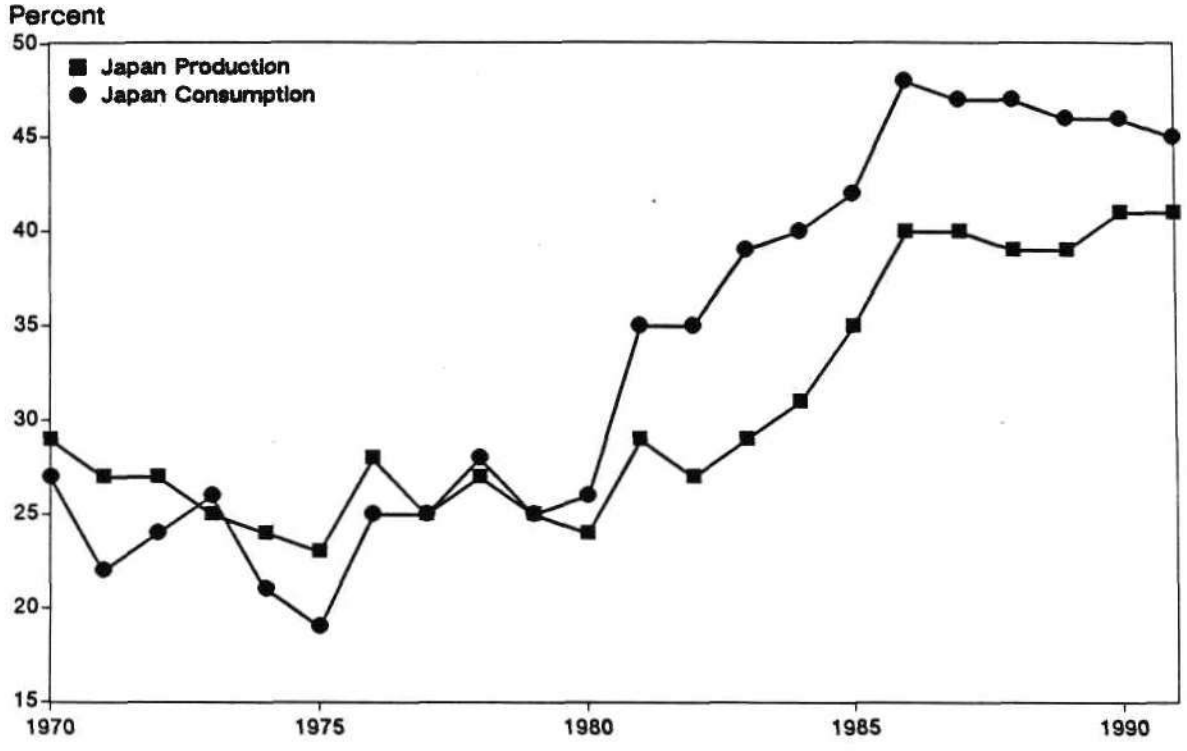
Figure 4

REGIONAL CONSUMPTION VERSUS REGIONAL MARKET SHARE



Source: Dataquest
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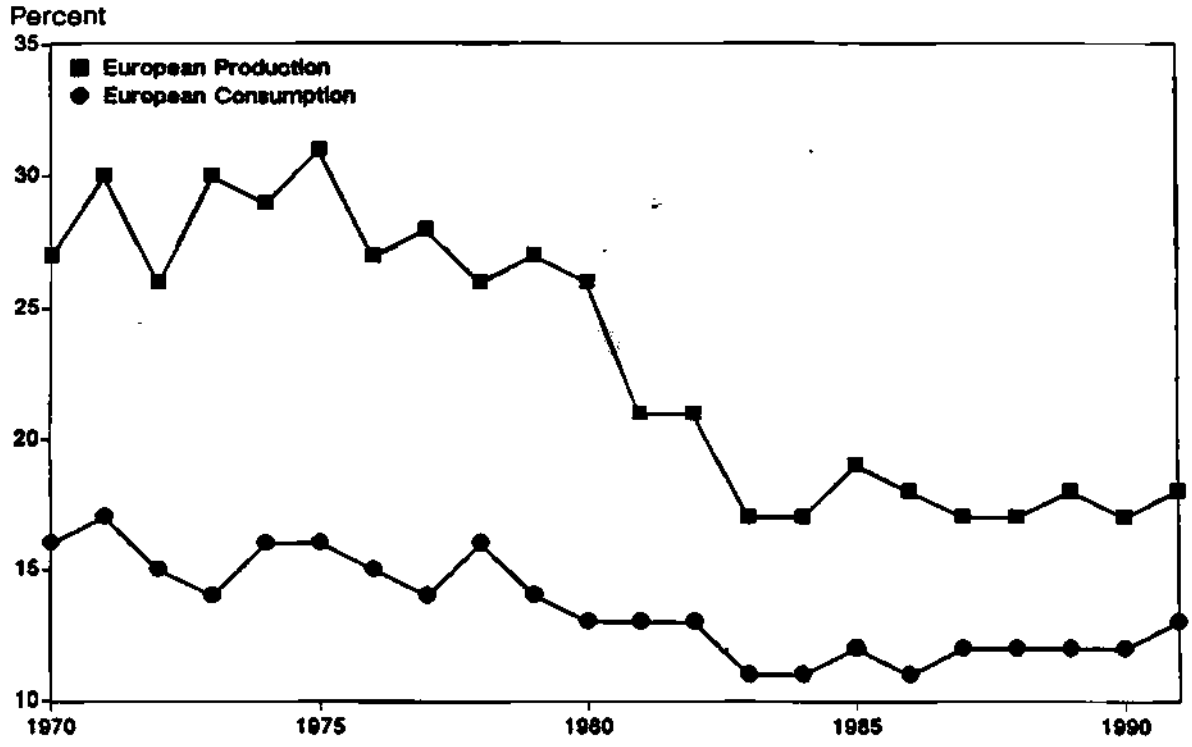
Figure 5

REGIONAL CONSUMPTION VERSUS REGIONAL MARKET SHARE



Source: Dataquest February 1987

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Production

PRODUCTION BY REGION

While worldwide market share will probably change little in the next five years (barring currency fluctuations), the value of devices produced in the each of the major regions of the world will see some changes. Production in North America will grow from 39 percent of the worldwide total in 1986 to 40 percent in 1991 (see Table 4 and Figure 6). This growth in share is due almost entirely to the movement of international manufacturers into North America. For example, we expect production by Japanese-based manufacturers in North America to grow from $118 million in 1986 to $753 million in 1991, a compound annual growth rate (CAGR) of 45 percent. In this same period of time we expect European-based companies to also increase their presence in North America. We expect production in North America by European-based companies to rise from $773 million in 1986 to $1671 million by 1991, a CAGR of 16 percent. Table 5 lists those Japanese and European companies that we believe will be producing devices in North America by 1991.

Table 4

ESTIMATED PRODUCTION BY REGION

	1977	1978	1979	1980	1981	1982	1983	1984
North America	55%	52%	57%	58%	49%	49%	46%	46%
Japan	25%	28%	25%	26%	35%	37%	40%	41%
Europe	20%	19%	18%	16%	15%	14%	12%	12%
ROW	0	0	0	0	0	1%	1%	1%

	1985	1986	1987	1988	1989	1990	1991
North America	42%	38%	38%	38%	39%	39%	39%
Japan	43%	49%	48%	48%	47%	46%	46%
Europe	13%	11%	12%	12%	12%	12%	13%
ROW	2%	2%	2%	2%	2%	2%	2%

Source: Dataquest
May 1987

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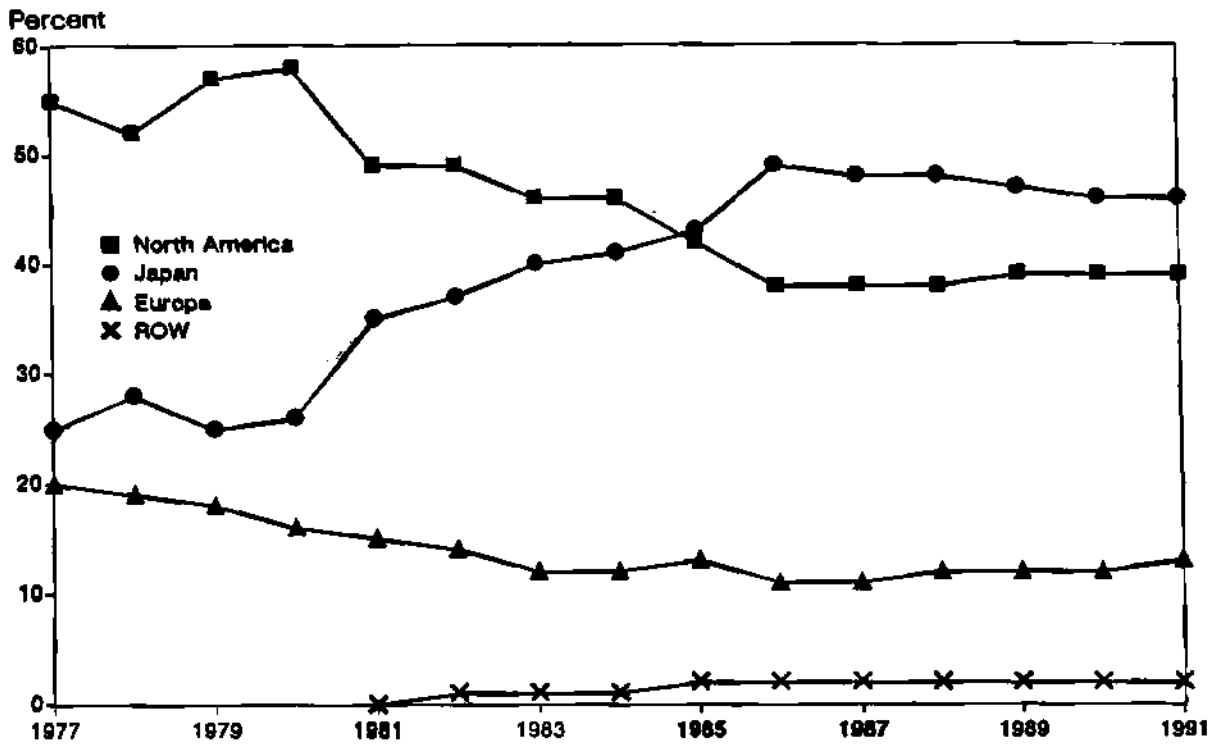
Production

Figure 6

PRODUCTION BY REGION



Source: Dataquest
February 1987

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Table 5

JAPANESE AND EUROPEAN COMPANIES IN NORTH AMERICA BY 1991

Company	Operation Date
Japan	
Exar	In Operation
Exel	In Operation
Hitachi	1988
NEC	In Operation
Oki	1988
Sharp	1989
Europe	
Philips/Signetics	In Operation
Thomson/Mostek	In Operation
SGS	1988
Siemens	In Operation

Source: Dataquest
May 1987

We also expect North American merchant companies to increase their presence in Europe and Japan. (See Table 6 for a listing of North American companies with overseas fabs.) Additionally, Japanese companies will increase their manufacturing in Europe and North America; and European-based companies will increase their presence in ROW countries and in North America (see Table 7 through 10). This movement of nondomestic-based companies into other regions is motivated by the desire of manufacturers to be close to their markets, to avoid trade friction, and to lower the risk of currency fluctuations.

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Table 6

NORTH AMERICAN MANUFACTURERS
WITH FABS IN EUROPE

Company	City	Country
Analog Devices	Basingstoke	Scotland
Analog Devices	Limerick	Ireland
Analog Devices	Limerick	Ireland
AT&T JV W/Telefonica	Madrid	Spain
Fairchild	Wasserburg	West Germany
General Instruments	Glenrothes	Scotland
Hughes Microelectronics	Glenrothes	Scotland
IBM	Boeblingen	West Germany
IBM	Corbell-Essones	France
IBM	Hannover	West Germany
IBM	Sindelfingen	West Germany
Intel	Tel Aviv	Israel
ITT	Freiburg	West Germany
LSI Logic	Braunschweig	West Germany
Motorola	East Kilbride	Scotland
Motorola	East Kilbride	Scotland
Motorola	Toulouse	France
National Semiconductor	Greenock	Scotland
National Semiconductor	Midgel Haenek	Israel
Siliconix	Swansea	Wales
Texas Instruments	Bedford	England
Texas Instruments	Freising	West Germany
Texas Instruments	Villeneuve-Loub	France

Source: Dataquest
May 1987

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Table 7

ESTIMATED PRODUCTION IN NORTH AMERICA BY REGIONAL COMPANIES
(Millions of Dollars)

	1977	1978	1979	1980	1981	1982	1983	1984
Total Production	$ 3,779	$ 4,667	$ 6,261	$ 8,030	$ 7,267	$ 7,421	$ 9,097	$13,352
Growth Rate		23.5%	34.2%	28.3%	(9.5%)	2.1%	22.6%	46.8%
North American	$ 3,779	$ 4,453	$ 5,996	$ 7,646	$ 6,901	$ 7,081	$ 8,661	$12,548
Japanese	0	0	0	0	0	0	0	$ 39
European	0	$ 214	$ 265	$ 384	$ 366	$ 340	$ 436	$ 765
ROW	0	0	0	0	0	0	0	0

	1985	1986	1987	1988	1989	1990	1991	CAGR 1986-1991
Total Production	$10,349	$11,553	$13,796	$16,682	$16,798	$19,596	$23,617	15.4%
Growth Rate	(22.5%)	11.6%	19.4%	20.9%	0.7%	16.7%	20.5%	
North American	$ 9,660	$10,635	$12,672	$15,292	$15,135	$17,686	$21,078	14.7%
Japanese	$ 56	$ 118	$ 126	$ 226	$ 398	$ 654	$ 753	44.8%
European	$ 613	$ 800	$ 969	$ 1,105	$ 1,215	$ 1,374	$ 1,675	15.9%
ROW	0	0	$ 29	$ 59	$ 50	$ 83	$ 111	N/M

N/M = Not Meaningful

Source: Dataquest
May 1987

Table 8

ESTIMATED PRODUCTION IN JAPAN BY REGIONAL COMPANIES
(Millions of Dollars)

	1977	1978	1979	1980	1981	1982	1983	1984
Total Production	$ 1,679	$ 2,540	$ 2,741	$ 3,676	$ 5,252	$ 5,590	$ 7,893	$11,872
Growth Rate	0	51.3%	7.9%	34.1%	42.9%	6.4%	41.2%	50.4%
North American	0	0	0	0	0	$215	$310	$455
Japanese	$ 1,679	$ 2,540	$ 2,741	$ 3,676	$ 5,252	$ 5,375	$ 7,583	$11,417
European	0	0	0	0	0	0	0	0
ROW	0	0	0	0	0	0	0	0

	1985	1986	1987	1988	1989	1990	1991	CAGR 1986-1991
Total Production	$10,499	$14,846	$17,301	$20,964	$20,309	$23,002	$27,329	13.0%
Growth Rate	(11.6%)	41.4%	16.5%	21.2%	(3.2%)	13.3%	18.8%	
North American	$ 411	$ 482	$ 592	$ 836	$ 899	$ 1,069	$ 1,288	27.1%
Japanese	$10,088	$14,364	$16,709	$20,128	$19,410	$21,933	$26,042	12.6%
European	0	0	0	0	0	0	0	N/M
ROW	0	0	0	0	0	0	0	N/M

N/M = Not Meaningful

Source: Dataquest
May 1987

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Production

Table 9

ESTIMATED PRODUCTION IN EUROPE BY REGIONAL COMPANIES
(Millions of Dollars)

	1977	1978	1979	1980	1981	1982	1983	1984
Total Production	$1,380	$1,728	$1,948	$2,171	$2,237	$2,122	$2,411	$3,424
Growth Rate	0	25.2%	12.7%	11.4%	3.0%	(5.1%)	13.6%	42.0%
North American	$ 400	$ 500	$ 700	$ 800	$ 700	$ 533	$ 632	$1,006
Japanese	0	0	0	0	0	0	0	0
European	$ 980	$1,228	$1,248	$1,371	$1,537	$1,589	$1,779	$2,418
ROW	0	0	0	0	0	0	0	0

	1985	1986	1987	1988	1989	1990	1991	CAGR 1986-1991
Total Production	$3,132	$3,448	$4,077	$5,124	$5,112	$5,989	$7,778	17.7%
Growth Rate	(8.5%)	10.1%	18.2%	25.7%	(1.3%)	17.0%	29.9%	N/M
North American	$991	$922	$1,014	$1,216	$1,274	$1,441	$1,843	14.9%
Japanese	0	0	$ 33	$ 64	$ 93	$ 100	$ 134	N/M
European	$2,141	$2,526	$3,030	$3,844	$3,744	$4,448	$5,801	18.1%
ROW	0	0	0	0	0	0	0	N/M

N/M = Not Meaningful

Source: Dataquest
May 1987

Table 10

ESTIMATED PRODUCTION IN ROW BY REGIONAL COMPANIES

	1977	1978	1979	1980	1981	1982	1983	1984
Total Production	$ 14	$ 18	$ 25	$ 35	$ 45	$ 98	$ 174	$238
Growth Rate	0	28.6%	38.9%	40.0%	28.6%	117.8%	78.0%	36.5%
North American	0	0	0	0	0	0	0	0
Japanese	0	0	0	0	0	0	0	0
European	0	0	0	0	0	0	0	0
ROW	$ 14	$ 18	$ 25	$ 35	$ 45	$ 98	$ 174	$238

	1985	1986	1987	1988	1989	1990	1991	CAGR 1986-1991
Total Production	$411	$623	$716	$878	$946	$1,088	$1,328	16.3%
Growth Rate	72.7%	51.6%	14.9%	22.6%	7.7%	15.1%	22.0%	
North American	0	0	0	0	0	0	0	N/M
Japanese	0	0	0	0	0	0	0	N/M
European	$100	$120	$140	$150	$170	$ 180	$ 200	10.8%
ROW	$311	$503	$576	$728	$776	$ 908	$1,128	17.5%

N/M = Not Meaningful

Source: Dataquest
May 1987

Production

CONCLUSIONS

Change is constant. Ten years ago, 40 percent of semiconductor devices were consumed in North America. North American merchant companies produced 55 percent of all merchant devices worldwide. Now all that has changed and a new leader has emerged. Because of the movement of the electronics end-use industry to Japan and to the Pacific Rim countries, more devices are consumed in Japan than in any other region. More devices are also produced in Japan, and Japanese companies have the largest market share of the merchant market.

But the fruit of leadership is less sweet (and profitable) than imagined; and forces are already in motion that will challenge Japanese leadership. The rise of the yen will hinder Japanese competitiveness and squeeze the profitability of Japanese companies. The threat of trade barriers will probably be constant. Other regions of the world, such as Korea, Taiwan, Hong Kong, and Singapore, will continue to rise from relative obscurity to challenge the leadership of Japan, North America, and Europe.

The globalization of manufacturing is a dominant trend in semiconductors today. Discerning what is a Japanese company, a North American company, or a European company will be increasingly difficult. North American companies in Japan have adapted to local culture and learned Japanese manufacturing techniques, and Japanese and European companies have adapted to North American techniques. The semiconductor industry will continue to become more global, to move closer to its markets, and to diversify to avoid currency fluctuations.

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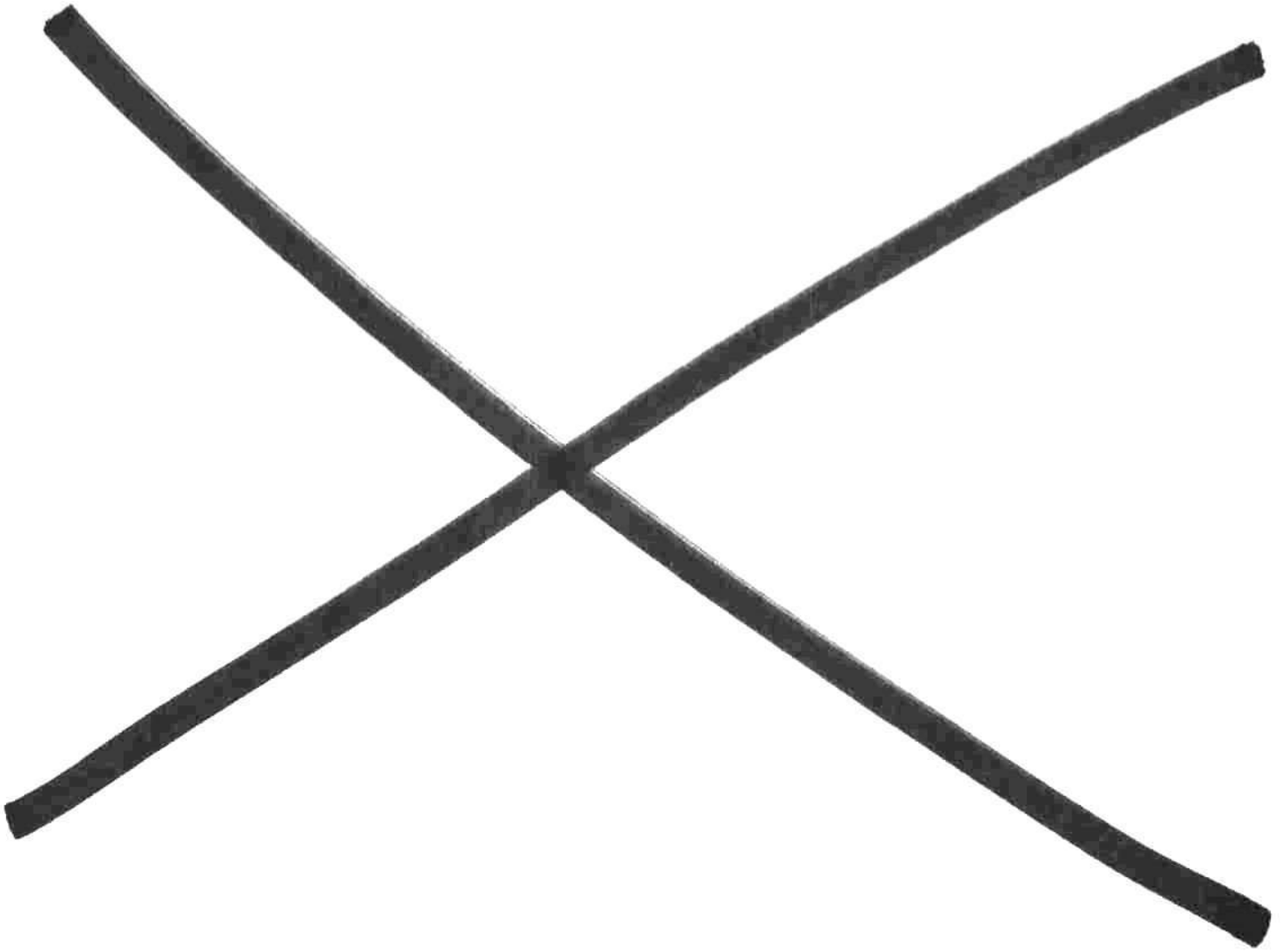


Capacity Utilization Forecast

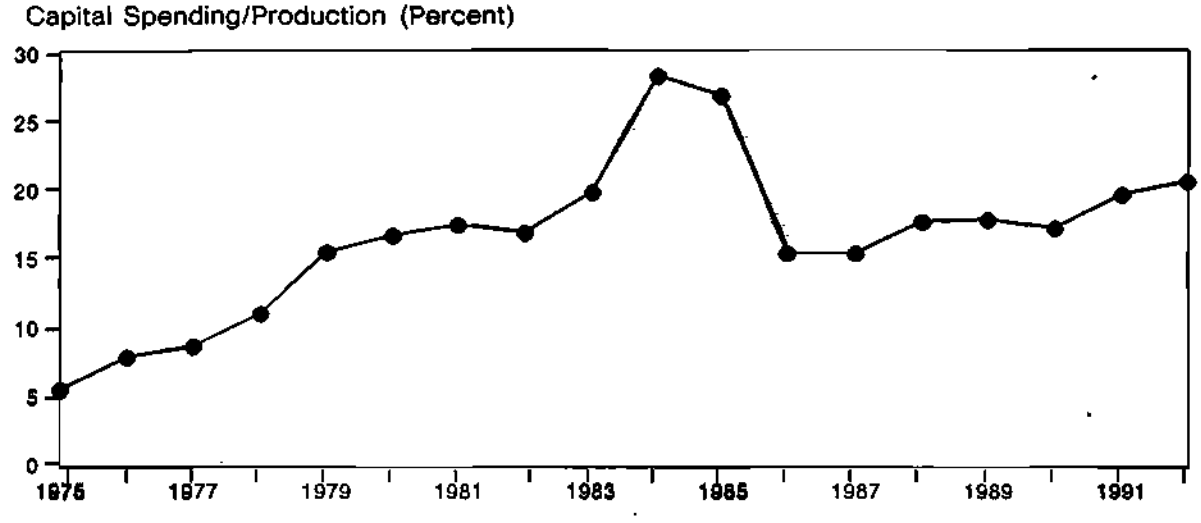
In all regions, capacity utilization reached a maximum of more than 90 percent in 1984. However, in 1985, capacity utilization fell to slightly more than 50 percent in the United States and, in 1986, it fell to 60 percent in Japan. Since that time, capacity utilization has risen in all regions of the world, reaching what we believe to be its peak in 1988. We expect capacity utilization to dip slightly over the next two years because of a slowdown in production growth. This is because, although the dollar value of worldwide semiconductor production grew 33 percent in 1988, we expect this growth rate to be less than 3 percent in 1990. After 1990, however, we anticipate that production will increase to its traditional double-digit rate, and capacity utilization will increase modestly to the 80 percent range.

One of the main features of this forecast, the reader will note, is that we expect capacity utilization to be much more stable than it has been in the past. This increased stability is due in part to improvements in factory management such as computer-integrated manufacturing (CIM) and just-in-time (JIT) manufacturing, which involves close partnering between semiconductor manufacturers and their customers.

Dataquest also believes that this increased stability of capacity utilization is due to the maturation of the industry itself. Since 1985, manufacturers have become much more conservative in the manner in which they add capacity. As can be seen from Figure 2, capital spending as a percentage of production jumped to abnormal levels in 1984 and 1985. Since 1985, this ratio has returned to historic levels.

Figure 2

Capital Spending as a Percentage of Production



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Capacity Utilization Forecast

Coincident with this decline in capital spending as a percentage of worldwide production has been a decline in the percentage of capital dollars devoted to property and plants. Historically, semiconductor manufacturers have spent about 20 percent of their capital dollars for property and plants. After 1985, however, this percentage declined to 15 to 17 percent.

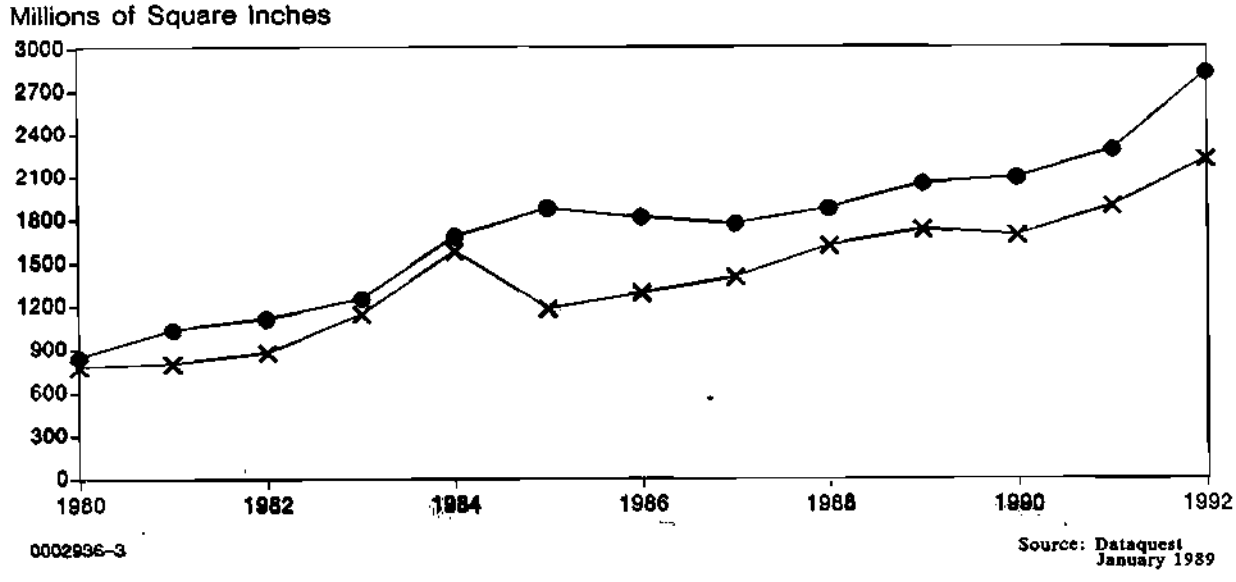
Thus, since 1985, manufacturers have decreased the percentage of their revenue devoted to capital spending and have also decreased the percentage of capital dollars devoted to new additions of property and plants. Capacity additions have thus come about more through upgrades and additions of equipment rather than through new plants. The net effect has been that capacity has been added in a more controlled and incremental fashion.

CAPACITY FORECAST

Silicon capacity, measured in square inches, increased steadily until 1985 (see Figure 3). However, in 1986 and again in 1987, capacity actually declined slightly. This decline in capacity was caused by two factors, the first of which was the 1985 recession, which allowed the industry to close down many older fabs and, as discussed above, caused manufacturers to adopt a more conservative capital spending stance.

Figure 3

Worldwide Starts and Capacity (in Square Inches)



Capacity Utilization Forecast

A second reason for the decline in worldwide capacity was the introduction of many new products and processes, which had the effect of decreasing equipment productivity; requirements for finer linewidths, automatic wafer handling and process control, and strict cleanliness all added up to much higher average selling prices (ASPs) for equipment. These higher prices more than offset any gains in equipment throughput, and, therefore, equipment productivity (which is the throughput per dollar value of property, plant, and equipment) declined. (See the sections elsewhere in this binder entitled "Manufacturing Productivity: An Overview" and "Manufacturing Productivity Forecast" for a more thorough discussion of the behavior of equipment productivity.)

Pushed by a 51 percent increase in capital spending and turnaround in equipment productivity, manufacturing capacity resumed its upward thrust in 1988. Except for a slowdown in 1989, we expect increases in equipment productivity and capital spending to continue to fuel increases in capacity. By 1992, capacity and starts should rise to approximately 2.7 billion and 2.2 billion square inches, respectively.

Capacity Analysis

The following is a list of the material in this section:

- North American Capacity Utilization

For additional information, please refer to the material behind the Capacity Analysis in your Newsletter binder.

North American Capacity Utilization

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North American Capacity Utilization

INTRODUCTION

Capacity utilization directly affects semiconductor ASPs, semiconductor lead times, and capital spending for semiconductor manufacturing equipment. Capacity utilization itself is a direct indicator of where the industry is in the business cycle: When capacity utilization is high, the semiconductor and equipment industries are expanding; when utilization is low, semiconductor and equipment manufacturers are generally experiencing hard times.

Industry-wide capacity utilization is currently the highest it has been since 1984. Capacity utilization is especially high for devices with line geometries less than or equal to 2.0 microns. It is also quite high for microdevices (microprocessors, microperipherals, and microcontrollers), standard logic devices, memory devices, and analog devices. ASPs and lead times for these products are increasing.

The following information has been generated by our second annual survey of North American semiconductor manufacturers. The fab data base is maintained by an annual survey and is updated on an ongoing basis with information generated by component group research, fab tours, industry sources, and the scanning of more than 30 periodicals related to the semiconductor industry.

Analysis in this section covers only pilot and production fab lines. It excludes R&D lines and quick-turn fabs. Also, any category of analysis that has fewer than three fabs has been excluded from tabular and graphical analysis in order to preserve the confidentiality of the fab.

The capacity utilization analysis that follows refers to the usage of wafer start capacity. The rates that are given refer to the last quarter of 1987. Since that time, utilization rates have risen slightly. Dataquest expects utilization to remain high until the middle of 1989, when added capacity and a leveling of demand will ease capacity pressures somewhat.

CAPACITY UTILIZATION BY LINEWIDTH AND WAFER SIZE

Capacity utilization at the end of 1987 was the highest (87 percent) for fabs that produced devices with line geometries in the 1.5- to 2.0- micron range (see Figure 1 and Table 1). For fabs that produced devices with line geometries between 1.0 and 1.5 microns, the utilization rate was 84 percent. Facilities producing submicron devices had capacity utilization rates approaching 80 percent. Because of these high utilization rates, Dataquest expects most of the new fabs built in the future to be for devices with line geometries at or less than 1.5 microns; many of these will be submicron facilities. Facilities that produced devices with line geometries greater than 2.5 microns had utilization rates that were much lower than the average—68 percent for 2.5 to 3.0 microns, 67 percent for 3.0 microns or greater.

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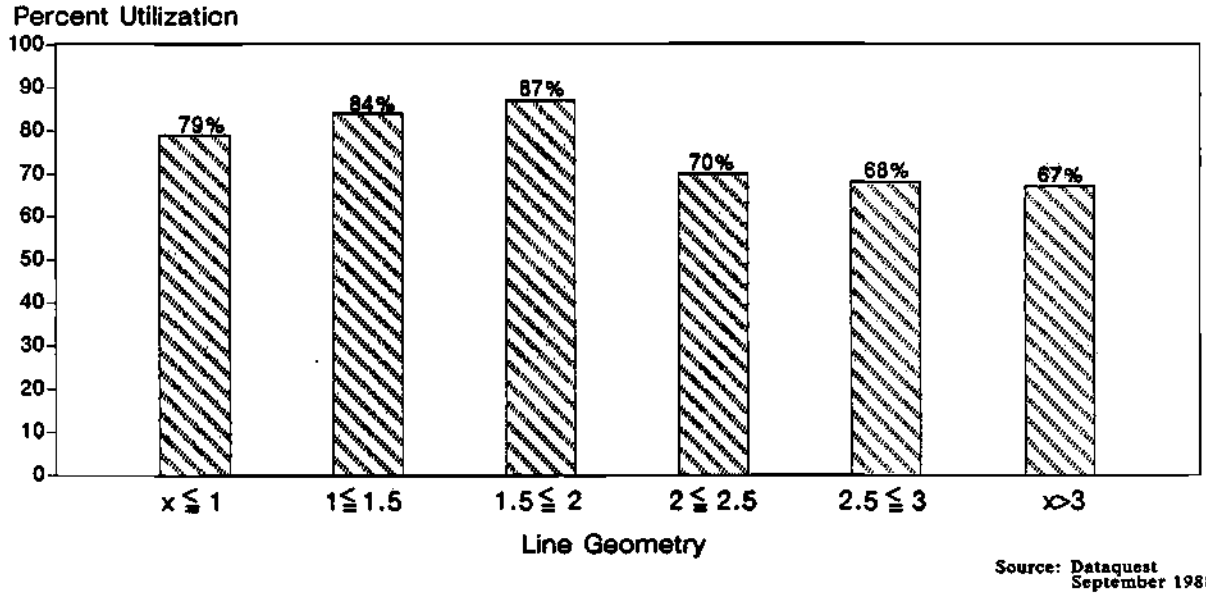
North American Capacity Utilization

Figure 1

Capacity Utilization by Line Geometry, Q4 1987



Source: Dataquest September 1988

Table 1

Capacity Utilization by Line Geometry, Q4 1987

Minimum Line Geometry	Percent Utilization
x<=1	79%
1<x<=1.5	84%
1.5<x<=2	87%
2<x<=2.5	70%
2.5<x<=3	68%
x>3	67%

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North American Capacity Utilization

Capacity utilization by wafer size was the highest for 125mm and 150mm wafers, more than 80 percent. Capacity utilization for 100mm wafers was less than 80 percent (see Figure 2 and Table 2).

Figure 2

Capacity Utilization by Wafer Size, Q4 1987

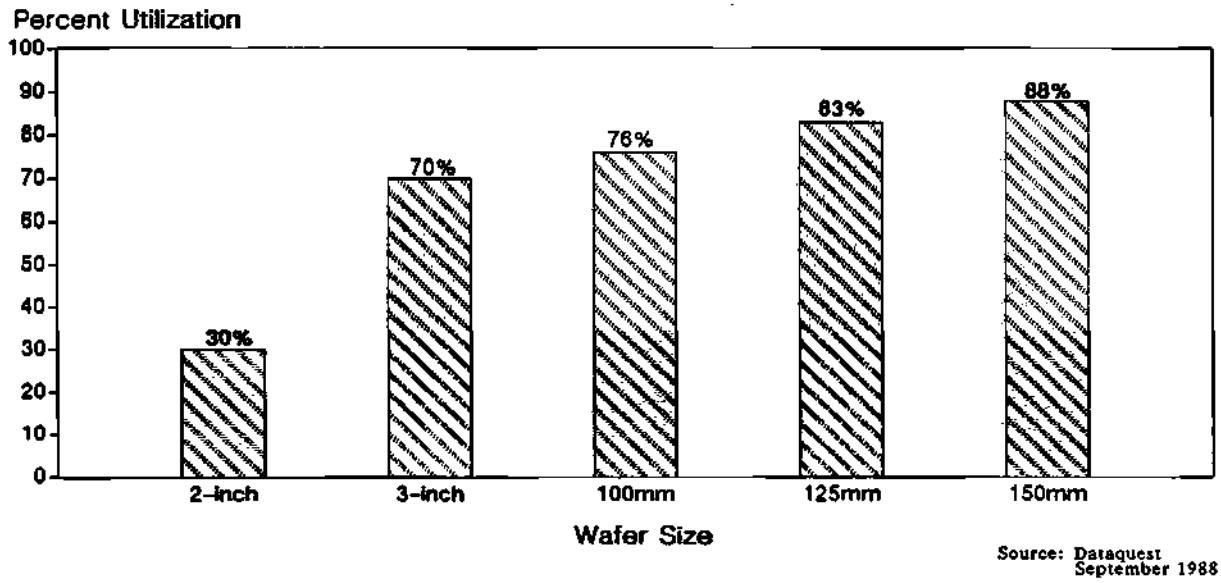

Table 2

Capacity Utilization by Wafer Size

Wafer Size	Percent Utilization
2-Inch	30%
3-Inch	70%
100mm	76%
125mm	83%
150mm	88%

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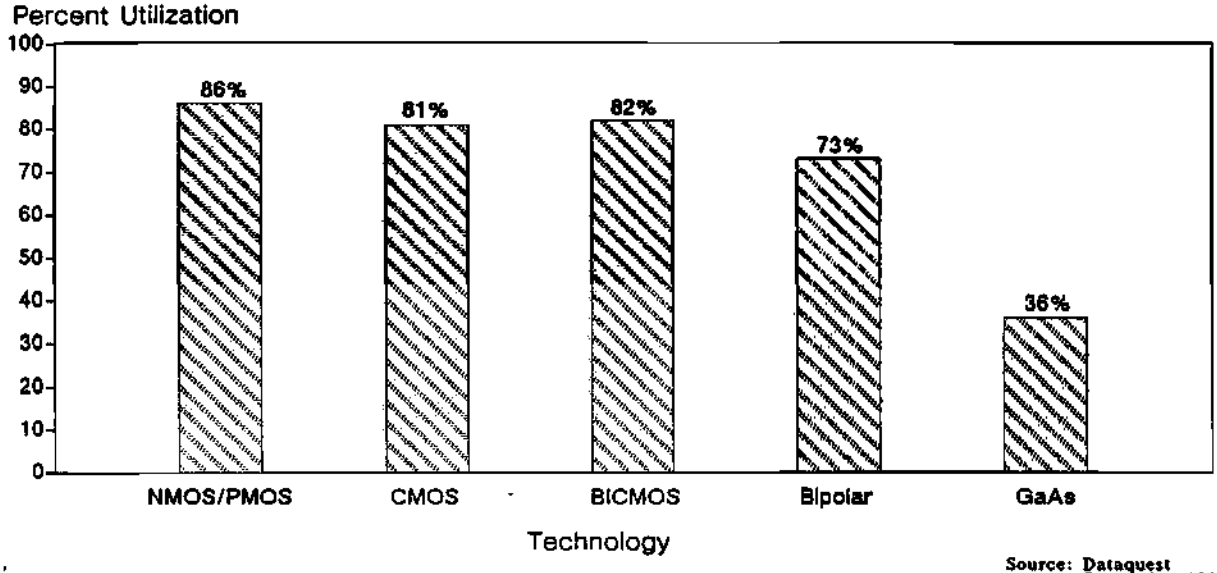
North American Capacity Utilization

CAPACITY UTILIZATION BY TECHNOLOGY AND LINEWIDTH

CMOS, NMOS/PMOS, and BiCMOS utilization were at or above 80 percent. Bipolar utilization rates were slightly more than 70 percent (see Figure 3 and Table 3).

Figure 3

Capacity Utilization by Technology, Q4 1987



Source: Dataquest
September 1988

Table 3

Capacity Utilization by Technology

Technology	Percent Utilization
NMOS/PMOS	86%
CMOS	81%
BiCMOS	82%
Bipolar	73%
GaAs	36%

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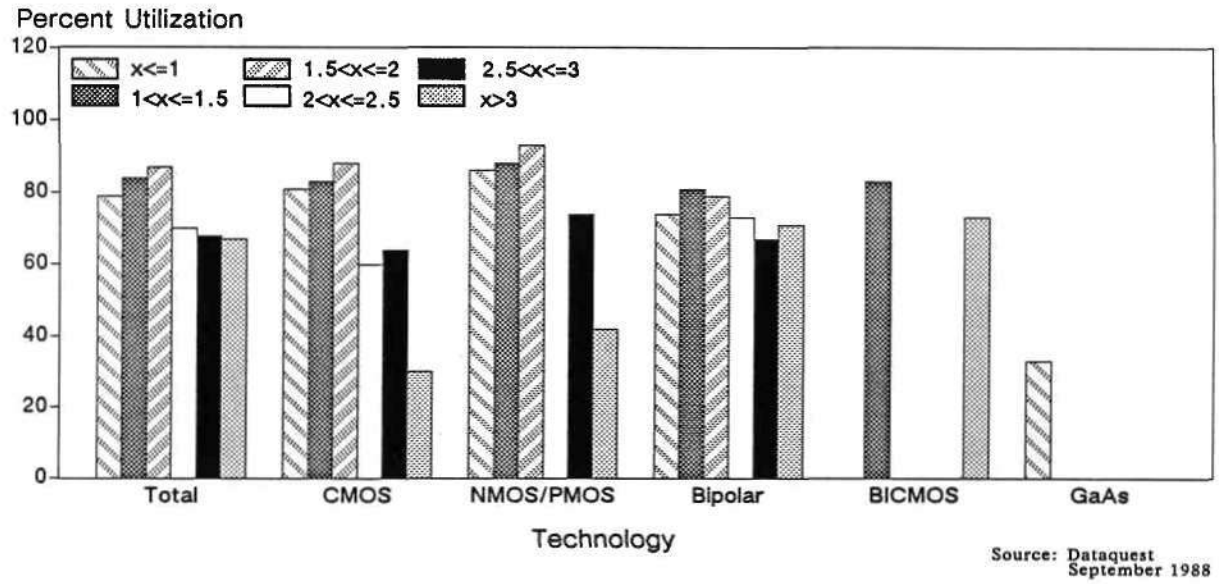
North American Capacity Utilization

CMOS capacity utilization is more than 80 percent for several devices with line geometries of less than 2.0 microns (see Figure 4 and Table 4). Bipolar capacity utilization is more than 80 percent only for devices with line geometries greater than 1.0 and less than 1.5 microns. NMOS/PMOS has a utilization rate of more than 80 percent for devices with line geometries less than or equal to 2.5 microns. Several categories of BiCMOS devices had too few fabs to be able to report capacity utilization by line geometries. However, BiCMOS devices with line geometries greater than 1.0 and less than 1.5 microns had a capacity utilization rate of 83 percent. Gallium arsenide and other III/V compound devices are still operating at low capacity utilization levels.

Figure 4

Capacity Utilization by Technology and Geometry, Q4 1987



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North American Capacity Utilization

Table 4

Capacity Utilization by Technology and Geometry

Minimum Line Geometry	Percent Utilization	CMOS	NMOS/PMOS	Bipolar	BiCMOS	GaAs
X<=1	79%	81%	86%	74%	N/A	33%
1<X<=1.5	84%	83%	88%	81%	83%	N/A
1.5<X<=2	87%	88%	93%	79%	N/A	N/A
2<X<=2.5	70%	60%	N/A	73%	N/A	N/A
2.5<X<=3	68%	64%	74%	67%	N/A	N/A
X>3	67%	30%	43%	71%	73%	N/A

N/A = Not Applicable

Source Dataquest
September 1988

CAPACITY UTILIZATION BY PRODUCT AND LINEWIDTH

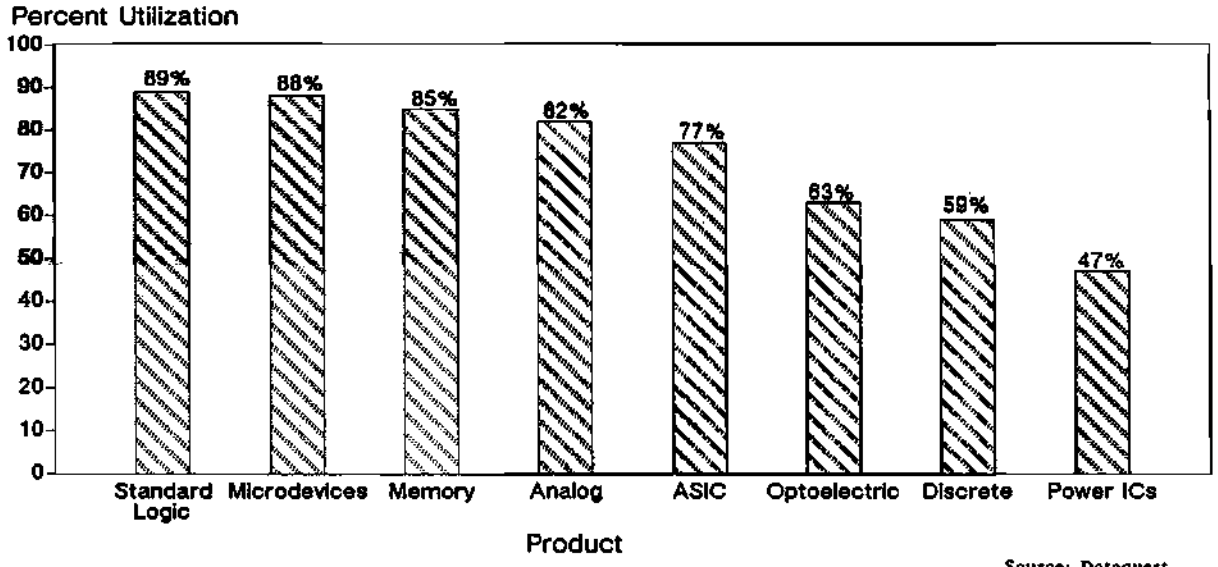
Dataquest's North American fab data base tracks wafer starts by the following product categories: analog, ASICs, discretes, memory devices, microdevices, optoelectric devices, power ICs, and standard logic. Capacity utilization rates exceeded 80 percent for standard logic devices and microdevices, memory devices, and analog devices (see Figure 5 and Table 5).

ASIC devices had capacity utilization rates near or exceeding 83 percent for devices with line geometries greater than 2.0 microns, but less than or equal to 2.0 microns (see Figure 6 and Table 6). Utilization rates for microdevices were very high indeed: near or exceeding the 90 percent level for line geometries less than 2.0 microns. The utilization rate for memory devices was at or exceeded 80 percent for all categories of line geometries less than or equal to 2.0 microns. Capacity utilization exceeded 90 percent for standard logic for geometries less than or equal to 1.5 microns, and, at the other end of the scale, for geometries greater than 3.0 microns. Capacity utilization of analog devices was the highest, 93 percent, for line geometries greater than 1.5 microns, but less than or equal to 2.0 microns. Capacity utilization for discrete devices was 93 percent for line geometry categories between 1.5 and 2.0 microns. Capacity utilization for power ICs is, generally, not high. Capacity utilization for optoelectric devices is high for the larger geometries.

North American Capacity Utilization

Figure 5

Capacity Utilization by Product, Q4 1987



Source: Dataquest
September 1988

Table 5

Capacity Utilization by Product

Product	Percent Utilization
Standard Logic	89%
Microdevices	88%
Memory	85%
Analog	82%
ASIC	77%
Optoelectric	63%
Discrete	59%
Power ICs	47%

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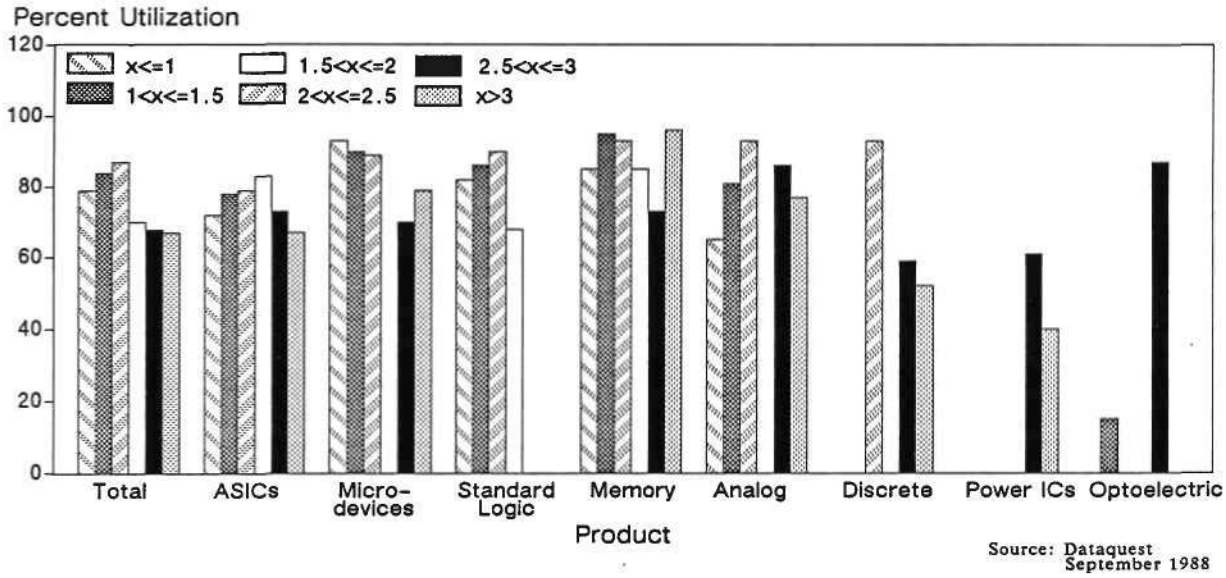
North American Capacity Utilization

Figure 6

Capacity Utilization by Product by Geometry, Q4 1987



Source: Dataquest
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Table 6

Capacity Utilization by Product by Geometry

Minimum Line Geometry	Total	ASIC	Micro Devices	Memory	Standard Logic	Analog	Discrete	Power IC	Opto-Electronic
X<=1	79%	72%	93%	82%	85%	65%	N/A	N/A	N/A
1<X<=1.5	84%	78%	90%	86%	95%	81%	N/A	N/A	15%
1.5<X<=2	87%	79%	89%	90%	93%	93%	93%	N/A	N/A
2<X<=2.5	70%	83%	N/A	68%	85%	N/A	N/A	N/A	N/A
2.5<X<=3	68%	73%	70%	N/A	73%	86%	59%	61%	87%
X>3	67%	67%	79%	N/A	96%	77%	52%	40%	N/A

N/A = Not Applicable

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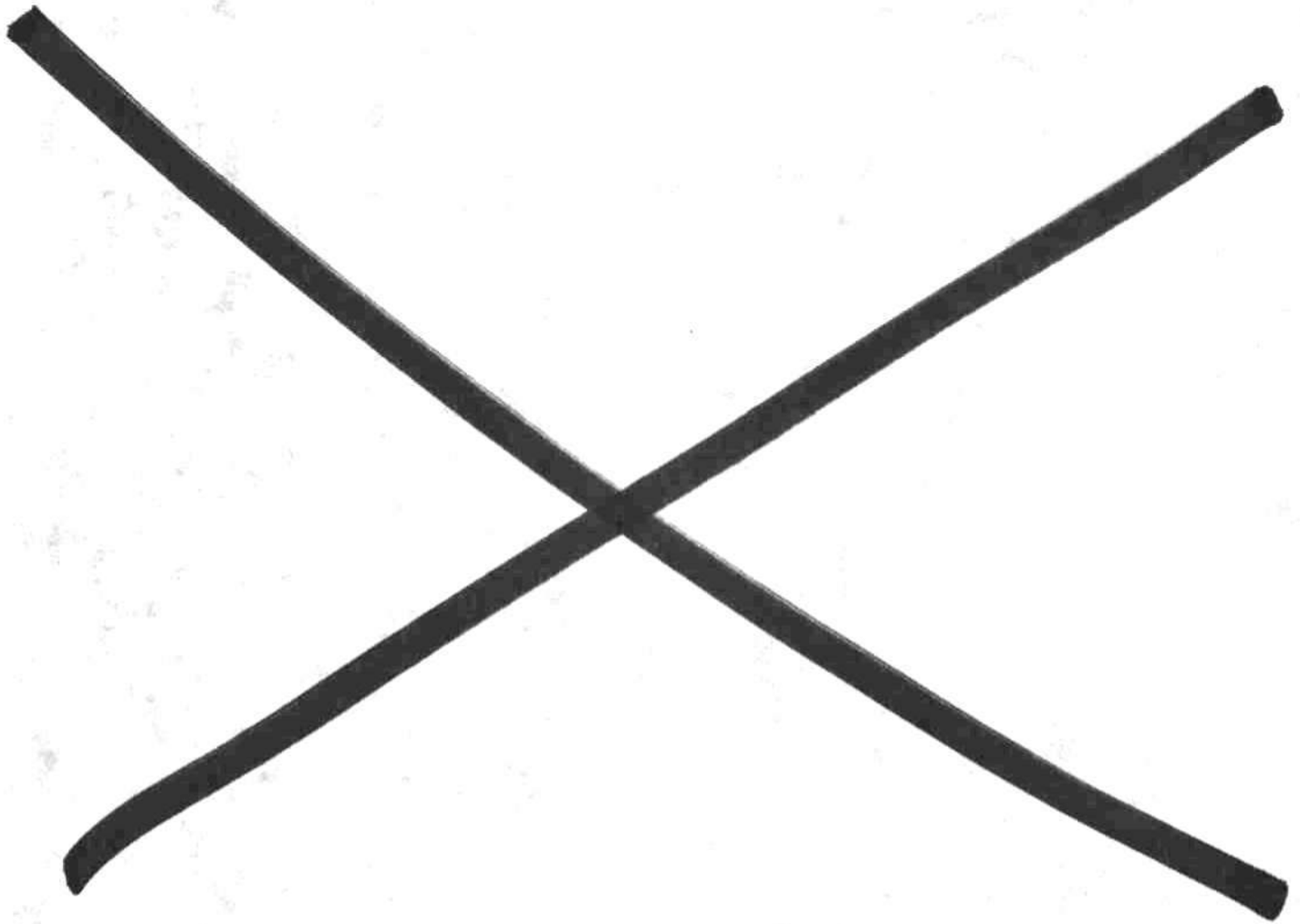

Manufacturing Productivity

The following is a list of the material in this section:

- Manufacturing Productivity: An Overview
- Manufacturing Productivity Forecast
- VLSI Device Fabrication: The 256K DRAM
- Prototype CMOS Model
- The Emerging Fab

Manufacturing Productivity: An Overview

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Manufacturing Productivity: An Overview

INTRODUCTION

Manufacturing productivity in the semiconductor industry has become a competitive weapon in the struggle for dominance of our increasingly global industry. This overview will examine the forces that are driving the evolution of capital productivity, equipment productivity, and process productivity. Understanding these forces is a vital requirement not only for semiconductor manufacturers but also for their equipment and materials vendors who, in the final analysis, are in partnership with semiconductor manufacturers to implement any successful productivity strategy.

CAPITAL PRODUCTIVITY

Productivity is usually defined as a measure of output per unit of input. In this case, we want to examine how much revenue (output) a unit of capital equipment (input) can generate. This is best measured by the ratio of revenue to the installed base of property, plant, and equipment (PPE).

The ratio of revenue to PPE for the different regions of the world from 1976 through 1987 is shown in Figure 1. Capital productivity has behaved similarly in all 1985 regions of the world, falling until 1985. Since 1985, it has had a tendency to rise. This rise in capital productivity is due to the increase in process productivity and equipment productivity. The relationship between capital productivity, process productivity, and equipment productivity can be expressed as follows:

$$P(C) = P(P) \times P(E)$$

where:

P(C) = capital productivity = revenue/PPE
P(P) = process productivity = revenue/(square inches)
P(E) = equipment productivity = (square inches of silicon)/PPE

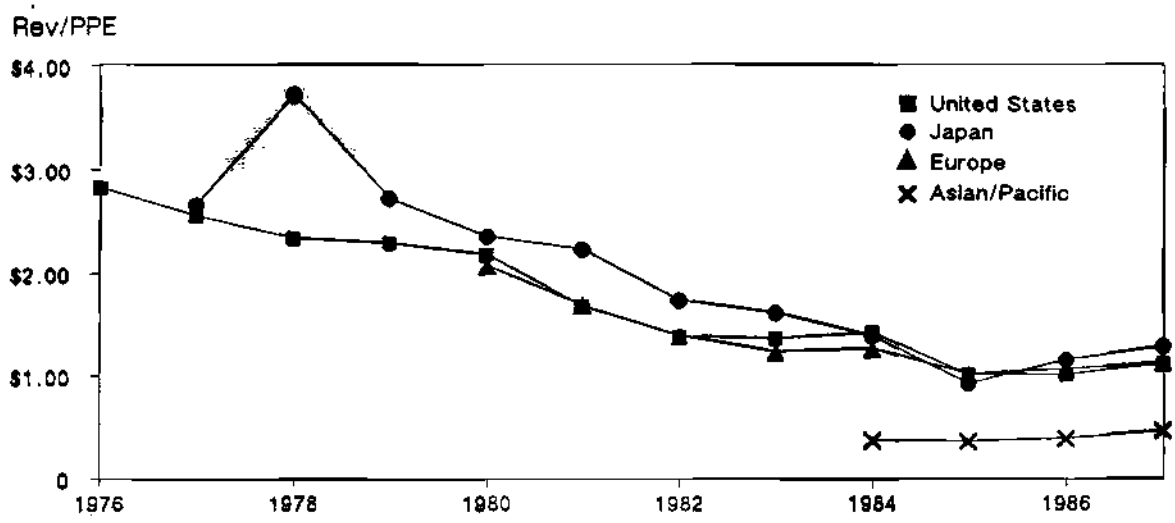
and therefore:

P(P) x P(E) = (revenue)/(square inches) x (square inches)/PPE
= (revenue)/PPE
= P(C)

In other words, capital productivity depends on how much silicon the equipment can produce (square inches of silicon per PPE) and on how much that silicon is worth (revenue per square inch).

Figure 1

Worldwide Revenue/PPE



EQUIPMENT PRODUCTIVITY

Equipment productivity is measured in square inches of silicon per dollar of PPE. Equipment productivity can be divided into three factors: reliability, utilization, and throughput. For example:

$$P(E) = R \times U \times T$$

where:

R = reliability
U = utilization
T = throughput per dollar PPE

Reliability

Equipment reliability is measured by four parameters in the following formula:

$$R = 1-(MTTR/MTBR + MTTA/MTBA)$$

where:

MTBF = mean time between failure
MTTR = mean time to repair
MTBA = mean time between assists
MTTA = mean time to assist

For example, if MTBF = 300 hours, MTTR = 10 hours, MTBA = 4 hours, MTTA = 5 minutes, then R = 0.88.

Reliability is becoming increasingly important for in-line processing. As reliability increases, there is less need for redundancy; for example, with increased reliability, a company may be able to operate with one etcher instead of the two needed previously to ensure continuous production.

Semiconductor manufacturers now are putting incentives and/or penalties for minimum levels of reliability into their purchase contracts. Semiconductor equipment manufacturers, on the other hand, are now offering service contracts that, for a premium, offer 95 percent reliability. Reliability is and will continue to be an important element in the competition between equipment vendors. Because of this, some equipment vendors have reorganized and are maintaining large field service groups as separate P&L centers.

Dataquest estimates that reliability is currently in the 85 percent range and will rise to 98 percent by the year 2000, even though the equipment is becoming more and more complex. As an illustration of the importance of reliability, consider the following example. Assume that there are five pieces of equipment with a reliability rating of 90 percent. For the five machines working together, their combined reliability is 90 percent to the fifth power, i.e., (0.9) x (0.9) x (0.9) x (0.9) x (0.9) = 0.59, or 59 percent. If the reliability of the individual pieces of equipment can be increased to 0.95, then the overall reliability of the five machines working together is raised to 77 percent.

Reliability is important also because it affects equipment utilization. When a piece of equipment is down, queues form upstream from the downed equipment, and equipment downstream stands idle. Line balance, which is so important for the efficient manufacture of complex product mixes, is upset. Not only is time lost on the downed piece of equipment, but utilization increases cycle time, and, as the wafers wait in ever-lengthening queues, their chances of getting hit by particulate contamination increases. Thus, yield decreases.

Utilization

Utilization refers to the use of equipment once it is available for use. The average equipment utilization for North American semiconductor companies has risen recently and is now in the neighborhood of 50 percent. In other words, equipment sits idle almost 50 percent of the time. This is primarily a function of inefficiencies in the production process caused by having to plan large mixes of products with many process steps for many different customers. Additionally, as discussed above, there are inefficiencies in utilization caused by reliability problems. It should be noted that in Japan, dedicated plants obtain a higher utilization than that of their U.S. counterparts because the Japanese plants have less process/product variation.

Dataquest believes that equipment utilization will increase as a result of computer-aided manufacturing (CAM) and automation systems that will enable manufacturers to balance and optimize their product mixes. Utilization also will increase as semiconductor manufacturers demand more reliability and quality from their equipment and materials vendors.

We believe that utilization is the biggest area of opportunity for semiconductor manufacturers to improve equipment productivity. We believe this because average equipment reliability is already high (85 percent), and we expect throughput per dollar of PPE to continue to be low because of high equipment costs. This leaves utilization as the equipment productivity variable with the most potential.

Throughput

Wafer throughput, the equipment's wafer-handling capacity, is measured in square inches of silicon per year per dollar of PPE. For those processes that have changed from batch to single-wafer processes, there has been a loss in wafer-handling capability. This is because batch-wafer handling has had a higher throughput than single-wafer handling, and a change from batch to single wafer represents a lessening of throughput. Although batch systems have had a higher wafer-handling capability, we now believe that the wafer-handling capability for the two types of processes are at approximate parity. We do not, therefore, expect that the migration from batch- to single-wafer handling will cause any further decrease in wafer-handling capability.

Process wafer-handling capability has increased only slightly. For single-wafer processing, it has increased as wafer size has increased. For those processes that have always been single-wafer dependent, this trend has increased throughput. Historically, the effects of the trend from batch to single wafer and the trend to higher wafer sizes have almost canceled each other out, although Dataquest believes that the net effect has been a slight increase in wafer-handling capability over the last 10 years. Although the wafer-handling ability of equipment has increased only slightly over the last 10 years, however, the price of equipment has not been so shy. It has increased dramatically over the years, with the result that throughput, measured in square inches per dollar of PPE, has fallen.

In the future, we believe that the industry's march into submicron reaches will work against increasing wafer-handling capability. This is because fabrication operations (e.g., alignment) in the submicron range take more time as the geometries become ever smaller. On the other hand, continued movement into larger wafer sizes will have an overall effect of increasing throughput, measured in square inches.

Regional Equipment Productivity

Historical equipment productivity by region is shown in Figure 2. Figure 3 illustrates Japanese equipment productivity measured in square inches per yen value of PPE, in order to eliminate distortions caused by exchange rate variations. Process productivity had a tendency to fall until 1985. Since 1985, equipment productivity has shown a slight tendency to rise.

Figure 2

Worldwide Regional Equipment Productivity

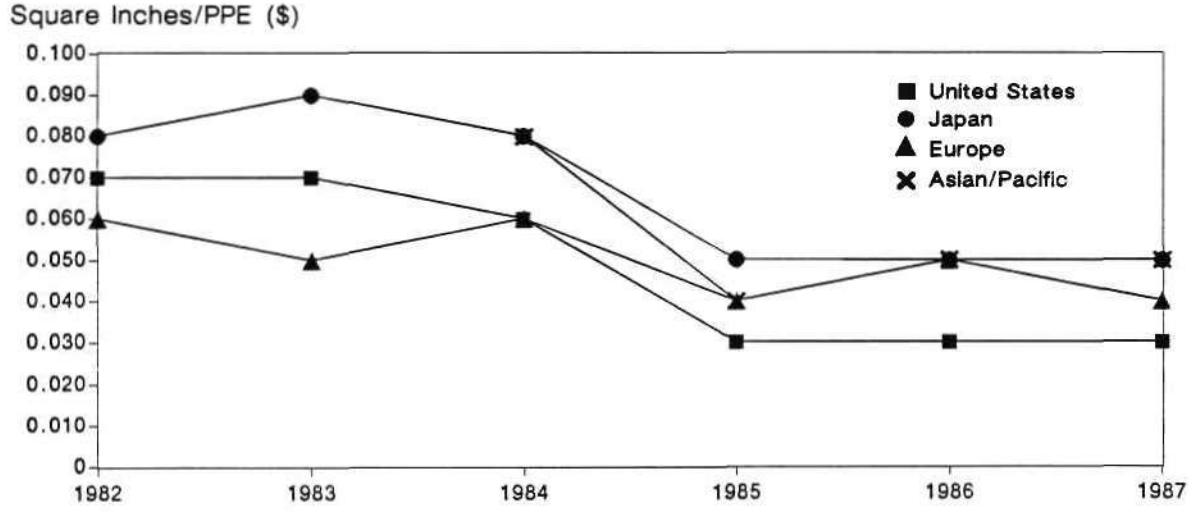
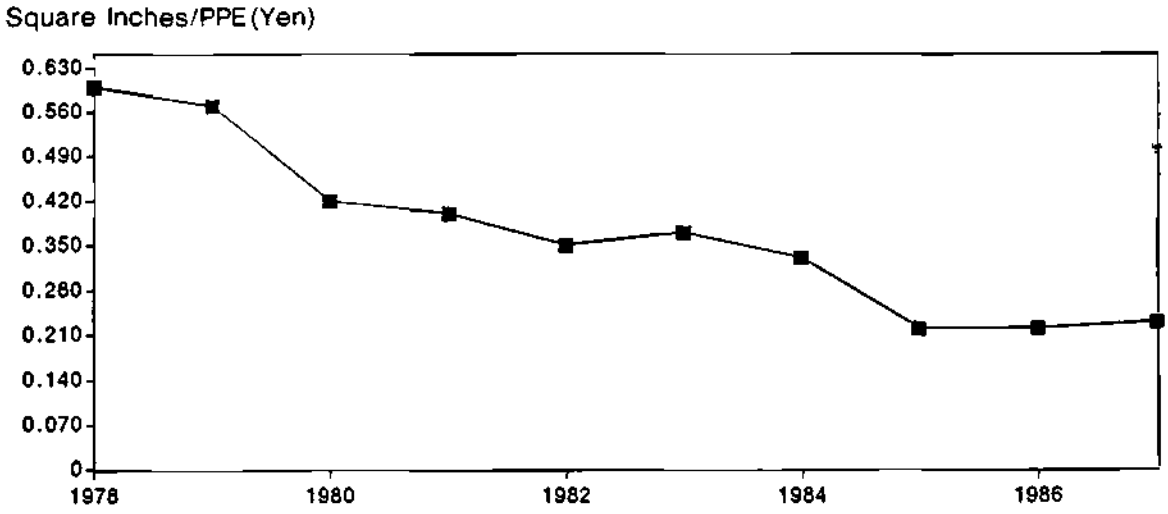


Figure 3

Japanese Equipment Productivity



PROCESS PRODUCTIVITY

Process productivity is defined as revenue per square inch of silicon. It is a measure of the revenue generated by silicon input. Revenue per square inch of silicon is a function of the average selling price (ASP), changes in inventory induced by the business cycle, manufacturing yields, and die size.

Given any amount of silicon in square inches, revenue is a direct function of ASPs. Revenue will tend to increase as ASPs increase, and conversely. ASPs will increase over the long term, both because of the increasing value of devices and because of the generally higher costs associated with manufacture. In the short term, however, ASPs tend to rise and fall with the waves of the business cycle. In a downturn, when capacity exceeds supply, ASPs tend to decrease. In an upturn, when capacity is constrained relative to demand, ASPs tend to rise.

Business cycle effects are not limited to ASPs. The ups and downs of the business cycle also affect the square inches carried in inventory and, thus, the revenue per square inch. During an expansion, work in process and pipeline inventory tend to expand, which in turn causes an increase in silicon consumption without a proportional increase in revenue. Conversely, when unit sales of devices slow down or decline, revenue is generated from work in process and from contraction of the pipeline without a corresponding increase in square inches purchased.

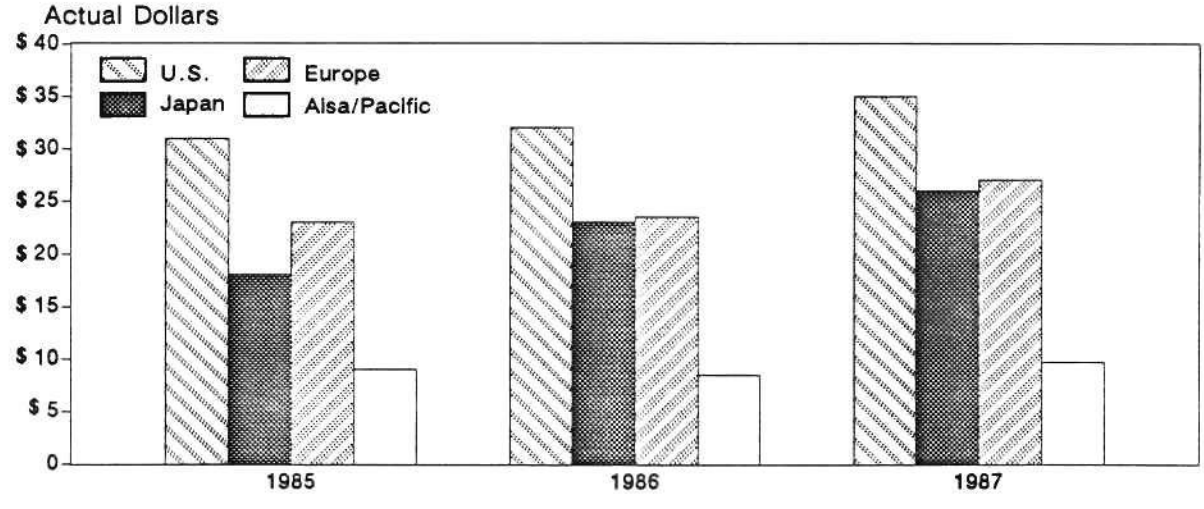
The business cycle also affects process productivity in another way--through yields. During an expansion, new equipment, new processes, and new labor personnel are brought into the production process. Because they are at the beginning of their learning curves, all of these factors tend to decrease yields.

Yields are affected positively by decreases in particulate contamination. Particulate contamination caused by human beings has been the focus of much study in the recent past; because of this attention, it is no longer the main source of contamination. Particulates housed in the equipment are now thought to be a major source of contamination. Trace impurities in process chemicals also have been identified recently by Dr. Tadahiro Ohmi as major sources of yield loss. Dataquest believes that as the problems of equipment-induced contamination and trace impurities in process chemicals are solved, yields will increase. Advances in automation that will further eliminate human contact from wafer processing will continue to increase yields also.

Process productivity is inversely proportional to die size. That is, as die size increases, process productivity decreases. This is because increasing the die size not only decreases the number of die per square inch but also decreases the yields. The larger the die are, the bigger will be the probability for killer defects. Nevertheless, Dataquest believes that process productivity has tended to increase since 1985 (see Figure 4).

Figure 4

Revenue per Square Inch by Region



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Manufacturing Productivity Forecast

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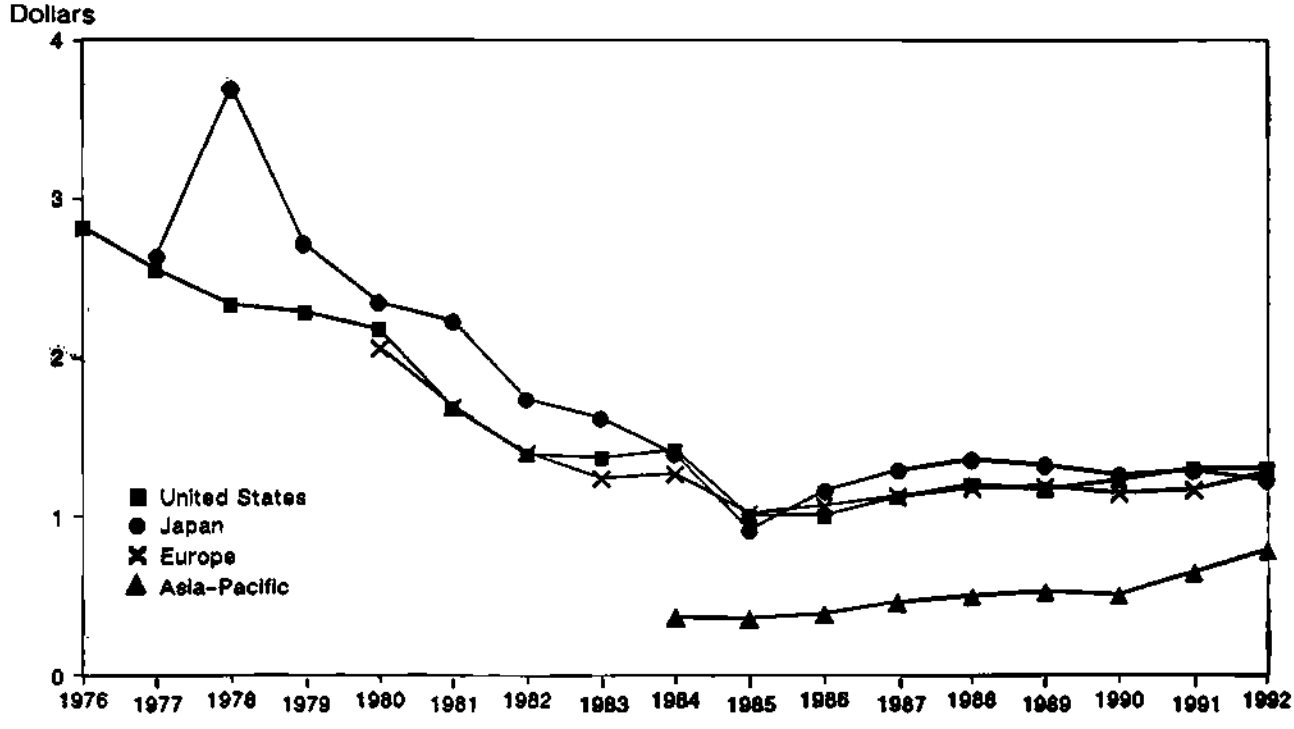
Manufacturing Productivity Forecast

CAPITAL PRODUCTIVITY

Dataquest's forecast for capital productivity is shown in Figure 1 and Table 1. Figure 1 shows dollar revenue per dollar value of property, plant, and equipment (PPE). Prior to 1985, for all regions except the Asia-Pacific region, revenue per PPE had declined. In 1985, it bottomed out at approximately $1.00 of revenue per dollar value of PPE. Our forecast indicates that this ratio will grow to approximately $1.30 by 1992 for both the European and U.S. regions. Figure 2 shows Japanese revenue per PPE measured in yen, which will increase from ¥0.87 per PPE in 1986 to ¥1.22 by 1992. Capital productivity of the Asia-Pacific region will grow faster than that of any other region. Our projections indicate that revenue per PPE will rise from $0.36 in 1985 (approximately one-third that of the other regions of the world) to $0.79 by 1992 (more than one-half that of the other regions of the world).

Figure 1

Revenue/PPE by Region



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Manufacturing Productivity Forecast

Table 1

Revenue/PPE

Region	1976	1977	1978	1979	1980	1981	1982	1983	1984
United States	$2.83	$2.56	$2.34	$2.29	$2.18	$1.68	$1.39	$1.27	$1.42
Japan	N/A	$2.67	$2.72	$2.72	$2.35	$2.23	$1.74	$1.62	$1.39
Europe	N/A	N/A	N/A	N/A	$2.07	$1.69	$1.40	$1.24	$1.27
Asia-Pacific	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	$0.37

Region	1985	1986	1987	1988	1989	1990	1991	1992	CAGR 1987-1992
United States	$1.01	$1.01	$1.12	$1.20	$1.17	$1.23	$1.30	$1.30	3%
Japan	$0.92	$1.16	$1.29	$1.36	$1.32	$1.26	$1.29	$1.23	(1%)
Europe	$1.02	$1.07	$1.13	$1.18	$1.19	$1.15	$1.17	$1.28	3%
Asia-Pacific	$0.36	$0.39	$0.46	$0.50	$0.53	$0.51	$0.65	$0.79	12%

N/A = Not Available

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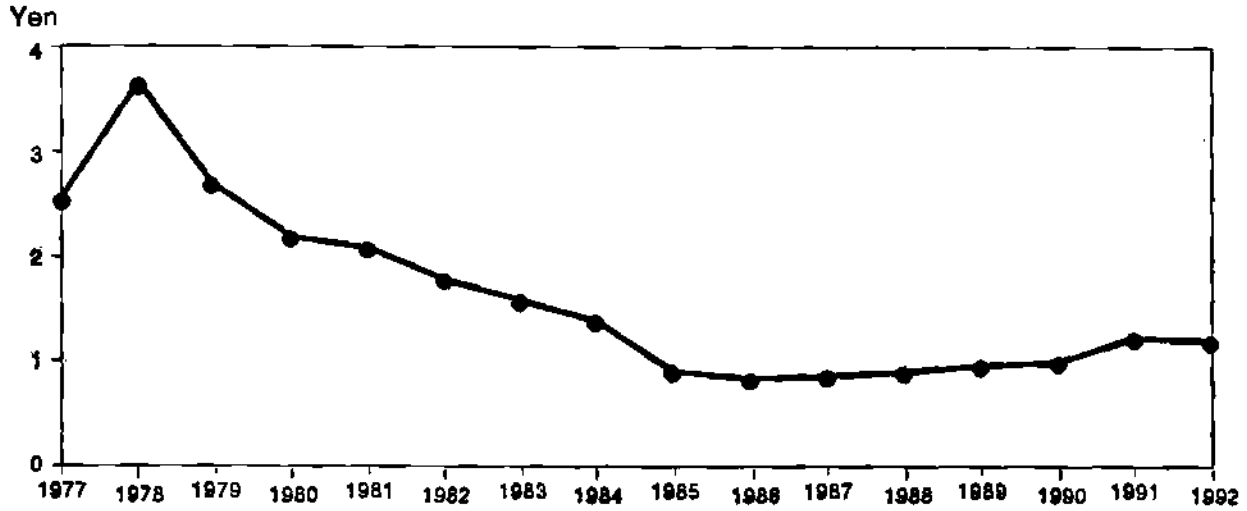
Figure 2

Japanese Revenue/PPE



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Manufacturing Productivity Forecast

Capital productivity will continue to rise because of continuing improvements in both equipment productivity and process productivity. Analysis of the upward dynamics of capital productivity is given in the service section entitled "Manufacturing Productivity: An Overview."

EQUIPMENT PRODUCTIVITY

Dataquest's unit of measure for equipment productivity is square inches of silicon per value of PPE. Historical and forecast values, measured in square inches per dollar value or PPE, are shown in Figure 3 and Table 2. Equipment productivity, measured in local currencies, has risen since 1985 in both Europe and Japan (see Figures 4 and 5).

Figure 3

Regional Equipment Productivity
Square Inches/PPE
(Dollars)

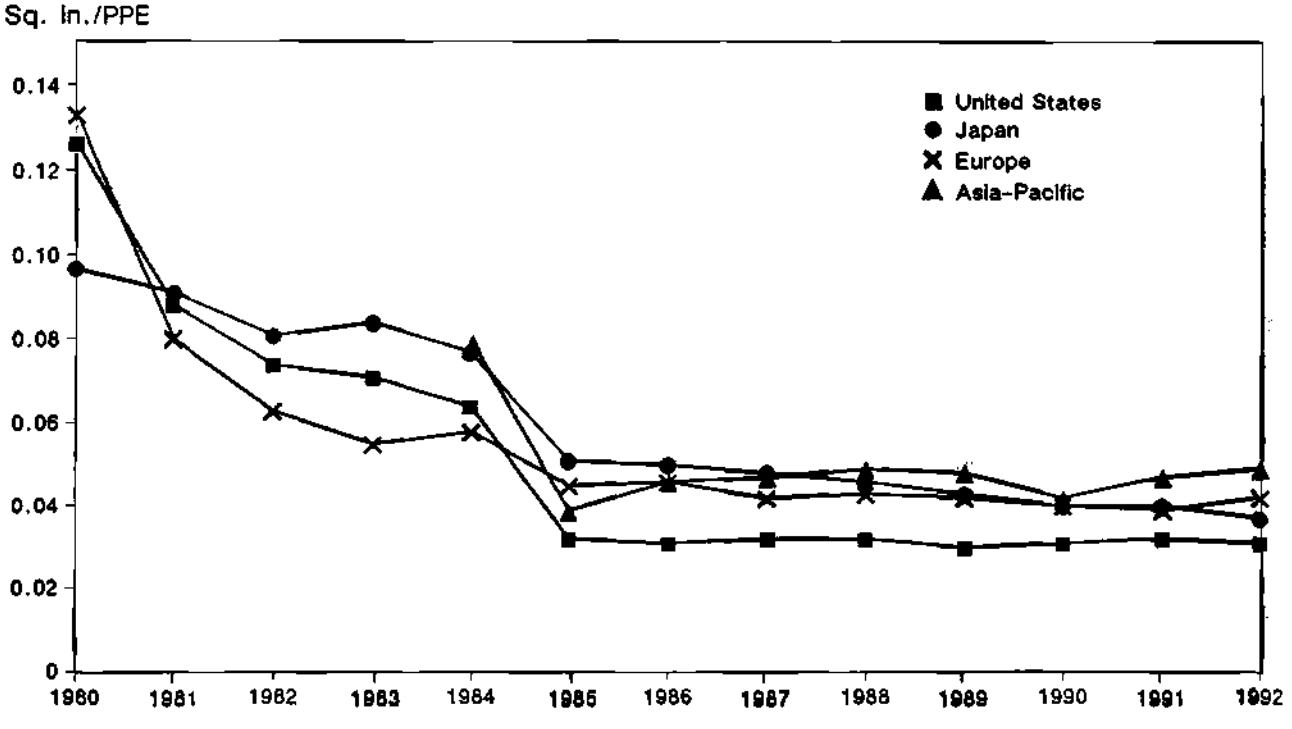

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Table 2

Square Inches/PPE

Regional Square Inches/PPE (Dollars)

Region	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	CAGR 1987-1992
United States	$0.13	$0.09	$0.07	$0.07	$0.06	$0.03	$0.03	$0.03	$0.03	$0.03	$0.03	$0.03	$0.03	0
Japan	$0.10	$0.09	$0.08	$0.09	$0.08	$0.05	$0.05	$0.05	$0.05	$0.04	$0.04	$0.04	$0.04	(5%)
Europe	$0.13	$0.08	$0.06	$0.05	$0.06	$0.04	$0.05	$0.04	$0.04	$0.04	$0.04	$0.04	$0.04	0
Rest of World	N/A	N/A	N/A	N/A	$0.08	$0.04	$0.05	$0.05	$0.05	$0.05	$0.04	$0.05	$0.05	1%

European Square Inches/PPE (European Currency Units--ECUs)

	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	CAGR 1987-1992
Europe	ECU 0.14	ECU 0.08	ECU 0.05	ECU 0.04	ECU 0.04	ECU 0.03	ECU 0.03	ECU 0.03	ECU 0.03	ECU 0.03	ECU 0.03	ECU 0.03	ECU 0.03	5%

Japanese Square Inches/PPE (Yen)

	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	CAGR 1987-1992
Japan	¥0.42	¥0.40	¥0.35	¥0.37	¥0.33	¥0.22	¥0.22	¥0.23	¥0.24	¥0.25	¥0.26	¥0.30	¥0.28	5%

N/A = Not Available

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Figure 4

Japanese Equipment Productivity
Square Inches/PPE
(Yen)

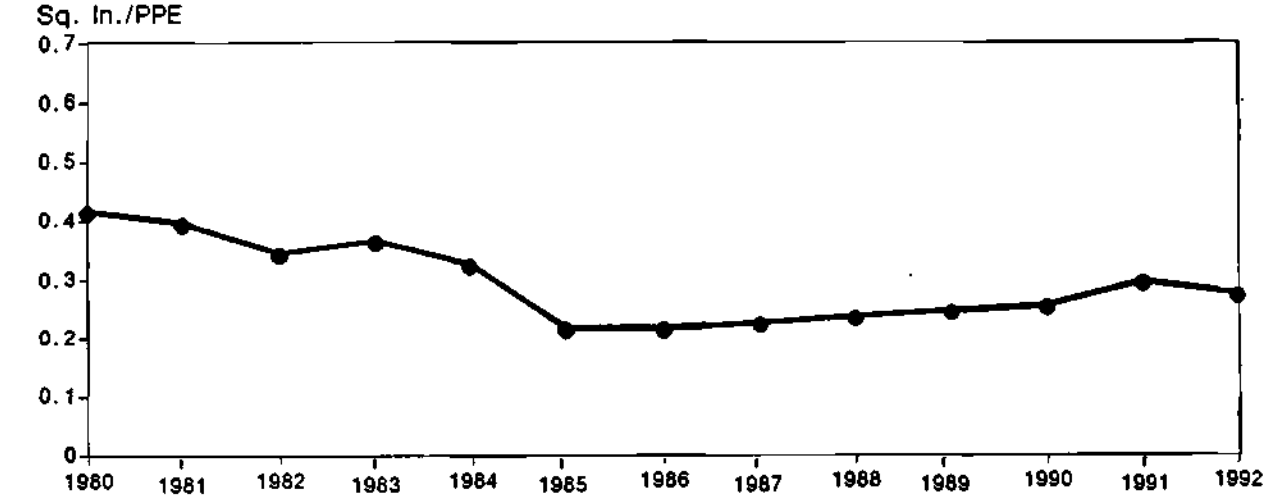

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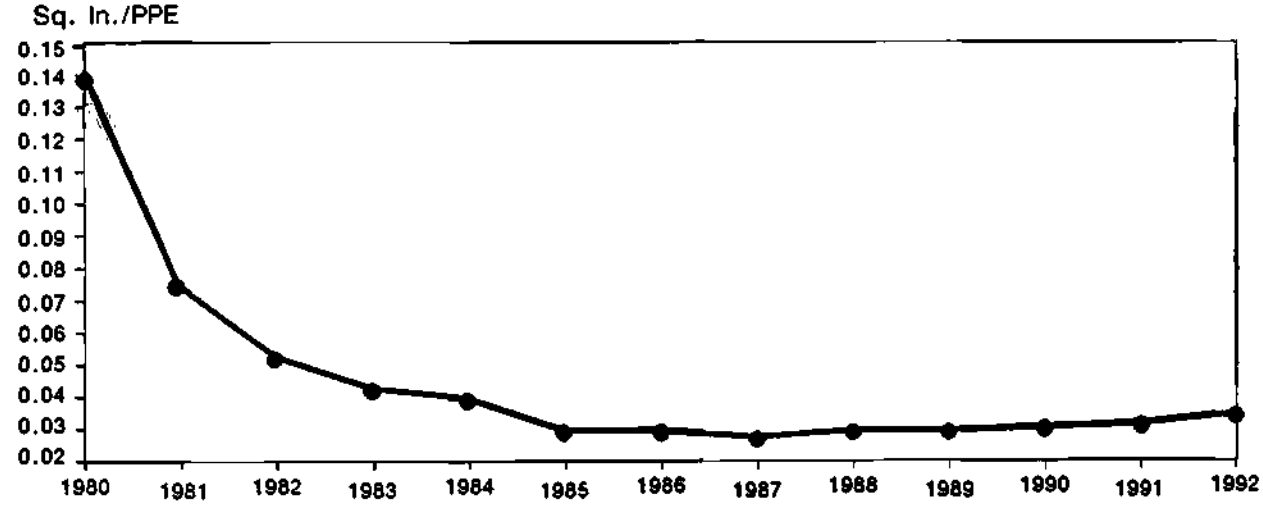
Figure 5

European Equipment Productivity
Square Inches/PPE
(ECU)



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However, the United States has experienced no increase in equipment productivity since 1985 (as shown in Figure 3 and Table 2). We believe that this difference between the United States and Japan and Europe is due to two reasons. First, the level of automation in both Europe and Japan is higher than in the United States. Second, the product mix in the United States is more varied; therefore, it is much more difficult to maintain utilization in the United States (see "Manufacturing Productivity: An Overview" for an analysis of the underlying dynamics of equipment productivity).

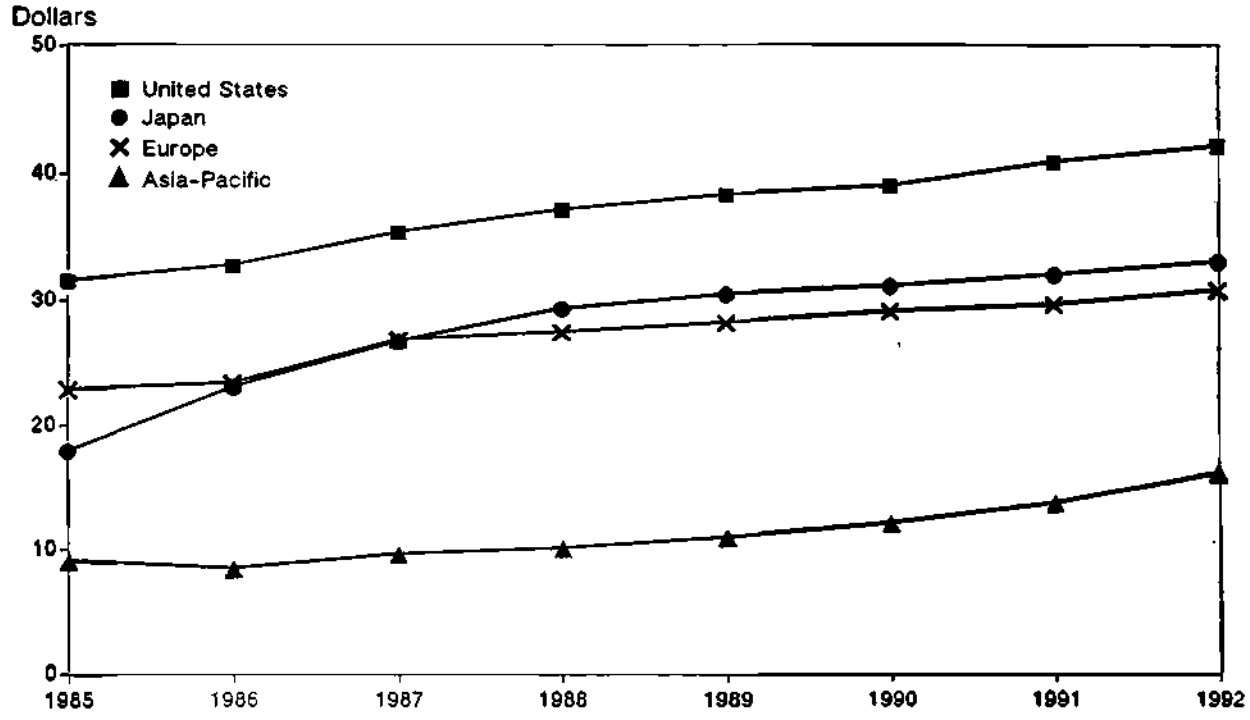
Equipment productivity in the Asia-Pacific region also has shown a slight tendency to rise. This is because of increases in throughput due to larger wafers now being processed in the area. We also expect engineers and managers in this area to continue their progress up the learning curve and thus improve both reliability and utilization.

PROCESS PRODUCTIVITY

Process productivity (revenue per square inch) is a function of average die size, average selling price, and yields (see "Manufacturing Productivity: An Overview" for an analysis of the underlying dynamics of process productivity). Dataquest's forecast for process productivity, in Figure 6, shows Europe and Japan to be approximately equal. However, U.S. process productivity is expected to be higher because of the higher average selling prices of U.S. devices. We expect process productivity to rise because of increases in average selling prices and yield improvements brought about through continued advancement in contamination control technologies, equipment improvement (such as integrated vacuum systems), and CIM.

Figure 6

Revenue/Square Inch by Region



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VLSI Device Fabrication--The 256K DRAM

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VLSI Device Fabrication--The 256K DRAM

INTRODUCTION

In this report, Dataquest will discuss the manufacture of the 256K dynamic random access memory (DRAM). This section will remain in our notebook as new products, such as the 1-Mbit DRAM, are introduced into semiconductor production. As such, some of the discussion may seem somewhat out-of-date. However, with this section, our clients will be able to follow the progress of semiconductor process technology as it evolves ever further into very large scale integration (VLSI) and beyond.

As the semiconductor industry charges through the 1980s, "VLSI" has become one of the most ill-defined terms in the electronic jargon. It means different things to different people. To those involved with VHSIC (very high speed integrated circuits), it means feature sizes of 1.25 microns or less. To others, it means more than 100,000 transistors per chip. To most people, it means something that "we can't quite make yet, but we're working on it."

The fact is that all of the above are true. The purpose of this chapter is to show the technological directions in MOS VLSI, particularly as they apply to the manufacture of 256K dynamic RAMs (dynamic read-write random access memories). We hope that this information will provide readers with an understanding of the manufacturing implications of VLSI, or at least aid them in formulating their own definitions.

Equipment plays a much bigger part in today's technology than it did in the past. In fact, many would claim that the equipment is the technology, for without it, VLSI circuits could not be built. As such, the selection of the "right" equipment is more important now than ever before, and with more advanced equipment hitting the marketplace every day, the concept of "right" is changing daily! This chapter will discuss these technological changes and how they influence the processing. But before we get into the details of wafer processing, we need to understand which MOS technology we are talking about and which feature sizes are significant.

N-CHANNEL TECHNOLOGY

The "old workhorse" in dynamic RAM technology is the double-layer polysilicon, oxide-isolated, N-channel silicon gate process. This basic process is widely sourced in the industry. It is a six-etched-mask process and is reasonably well characterized and understood. However, today's N-channel technology bears little resemblance to what it was at its inception. The process sequence is virtually the same for 64K and 256K RAMs, and if one were to draw a process schematic, yesterday's 64K RAM and today's 256K would look quite similar. But there the similarity ends. One of the differences that is most apparent is that in going from the 64K to the 256K, IC manufacturers have crammed four times the memory into only two times the space or less. Through the process of scaling, there has been a rapid trend toward smaller dimensions over the past years. The 3- and 4-micron polywidths of last year are now

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2 microns, and heading toward 1.25 microns. Implementation of these scaled devices is due to better processing equipment; not only have the dimensions shrunk, but the tolerances have as well. This means that today's 256K RAM is even more finely tuned than the 64K.

Design Challenges

One of the design challenges in N-channel technology is the sense amplifier, which, as most product engineers on RAM manufacturing lines realize, is really a linear circuit cleverly disguised as a digital one. The one-transistor, one-capacitor cell is still the backbone of RAM design. However, because of scaling, the size of the capacitor has been shrunk down to 50 femtofarads (5×10^{-14} farads), which when charged to 5 volts gives 250 femtocoulombs. This is the charge of about 1.6 million electrons. Needless to say, leakage currents have to be incredibly small to hold this charge between refreshes. This capacitor is discharged into the bit line, and therefore the voltage across the bit line is related to the ratio of bit-line-to-cell capacitance. Reasonable designs still only have the actual voltage sensed at the sense amplifier at the 100-millivolt level. To sense this small voltage reliably, threshold voltages must be tightly controlled. Capacitances of the cell and bit line, as well as parasitic capacitances, must be similarly constrained. This puts a squeeze on the process tolerance limits, since designers want to make things smaller and smaller.

All of the scaling and processing are directed toward:

- Reducing the bit-line capacitance
- Reducing the cell size
- Increasing the cell capacitance
- Reducing the propagation delay
- Improving or at least maintaining soft error sensitivity
- Reducing the defect density

All the processing techniques that will be discussed will relate to the achievement of one or more of these goals. Everything is directed toward more process control (i.e., tighter limits), lower defect density, and, as we shall see, lower temperature processing.

Some of the typical parameters for a 256K RAM compared with 64K technology include:

	64K	256K
Gate Oxide	400 nm	250 nm
Junction Depth	0.5 m	0.25 m
Channel Length (drawn)	3.0 m	2.0 m
Diffusion Pitch	6.0 m	5.0 m
Poly Pitch	5.5 m	4.0 m
Metal Pitch	8.0 m	6.0+ m

The trend toward smaller critical dimensions is clearly evident.

CMOS Versus NMOS

Before discussing processing in detail, we should mention CMOS. All of the current 256K designs in production are NMOS rather than CMOS, which is supposedly the technology of preference for VLSI. CMOS offers many advantages for VLSI, most notably its low-power consumption. However, for memories (more specifically, dynamic memories), CMOS memory cells presently take up too much space. The one transistor plus one capacitor cell of NMOS is hard to beat for space. We expect increasing use of CMOS in the chips' peripheral logic--decoders, buffers, and assorted on-chip logic for "smart" memories. Stacked transistors may change this, but their widespread use is years away. The basic technology is still N-channel for dynamic memories.

MANUFACTURING TECHNOLOGY

In this section we will discuss the various areas of wafer fabrication technology, current processing trends, and the various options to implement the technology. We will include discussions of the impact of automation and robotics as applicable. We will analyze both sides of the competing technology implementations and itemize their impacts on the 256K RAM goals. Since the technology is so intertwined with the equipment, we also intend to look objectively at the equipment alternatives and at their economic and technological limitations.

Dielectric Films

Dielectric films fall into two broad classifications: active (gate dielectrics) and passive (dielectric films used purely as "insulation" or isolation). These dielectrics, whether grown or deposited by a chemical vapor deposition process, have received much attention over the years because they can be the source of high defect densities on the chip if they are not handled properly.

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Gate Dielectrics

Gate dielectrics in particular have received tremendous scrutiny. The gate dielectric (silicon dioxide in most cases) has become much thinner over the years. Previous gates were 1,000 Angstroms thick (100 nm); typical VLSI thicknesses are currently 250 Angstroms. As these films get thinner, defect densities become more and more important. The majority of these films are grown in either oxygen or steam ambient in a diffusion furnace. Today's digitally controlled diffusion furnaces allow complete selection of load and unload speeds, gas ambients, temperature, and temperature profile, as well as autologging of all furnace parameters as part of the "archives" of a particular batch of wafers. These furnaces have had direct digital control for several years, but have only recently achieved the reliability level necessary for VLSI. (When furnace manufacturers rushed into the digital age and abandoned their analog control systems, many problems developed with the cross-coupling of noise from the power control circuitry into the digital master control circuits.) These problems have been solved in today's equipment.

Another major innovation in the last two years has been improvement in loading and unloading of wafers into the furnace. Previously, the wafers were pushed and pulled from the furnace by quartz rods that engaged the wafer carriers (boats). The boats dragged along the bottom of the quartz furnace tubes and generated a shower of particles inside the furnace tubes. As oxides became thinner, these particles drastically increased the defect densities. Various attempts to eliminate the sliding of quartz on quartz were tried. Boats were given little wheels or rollers. Other designs tried shields to deflect the shower of particles. Finally, a cantilevered, soft-landing system was developed which loads the wafers down the tube and only at the end of the push are the wafers gently lowered to the tube surface. This technique has greatly improved yields, and virtually all furnace systems for VLSI devices now offer this design as an option.

Ionic contamination of the gate dielectric and the breakdown voltage strength of the oxide are critical factors in fabrication of 256K RAM devices. As the dielectrics get thinner, the electric field for a fixed voltage (the universal 5 volts) increases rapidly. To reduce the ionics, the use of hydrogen chloride (HCl) to "clean" the oxide is virtually universal. It is, however, highly controversial. HCl can be used in three ways. First, it can be used as a cleaning agent for furnace tubes. The furnace is heated to a temperature of 1,100 degrees C and steam and HCl are introduced into the tube. After awhile, the HCl is turned off and the tube is allowed to "steam out" for a few hours. This lowers the ionic contamination in the tube and results in excellent impurity control in the furnaces. This is probably the most uncontroversial aspect of HCl.

The second use of HCl is for precleaning the wafers prior to oxidation. The wafers are brought up to the oxidizing temperature in a mixture of oxygen and HCl. The HCl is then turned off and the oxidation cycle starts. This has been shown to produce films of excellent dielectric quality without any serious side effects.

The third and most controversial use of HCl is its introduction during the oxidation process. While this seems to give the "cleanest" oxide films, it can have some serious side effects. The incorporation of chlorine into the film is a cumulative process. The

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chlorine migrates to the silicon-silicon dioxide interface. This goes on throughout the processing since many of the dopants ($POCl_3$) and gases (SiH_2Cl_2) used for LPCVD (low-pressure chemical vapor deposition) also contain chlorine. It has been shown that large chlorine accumulations can actually delaminate the oxide from the silicon or cause threshold voltage shifts. Customers who require radiation hard devices (for military systems or satellite applications) have found that use of HCl during oxidation causes instabilities when exposed to radiation. The proper amount of HCl must be determined that will provide clean films, without causing any side effects. Device manufacturers are now backing away from both HCl and chlorine-based compounds that have the same action. More and more users are eliminating HCl during the oxidation process and using it only for wafer precleaning or tube cleaning.

Not all the activity in the active dielectric area is directed toward low-defect density. Increasing the cell capacitance has some immediate paybacks. More capacitance in the same area can be obtained by thinning the gate dielectric (which has its limits) or by increasing the dielectric constant of the gate dielectric. This is where silicon oxynitride comes in. Silicon nitride has a dielectric constant that is 50 percent greater than that of silicon dioxide. The direct growth of silicon nitride on silicon causes some undesirable properties that reduce device speed and threshold voltage control. The preferred technique is to grow a thin film of silicon dioxide and then convert the film to an oxynitride in the presence of ammonia gas at elevated temperature. These films are stable, and while they do not get the full 50 percent boost in dielectric constant, they get most of the advantage without any of the disadvantages. Although there are no 256K devices on the market today with oxynitride storage capacitors, Dataquest believes that the next wave of devices will implement this technology in an effort to reduce die size and still maintain performance and reliability.

One processing technique that has not achieved the initial success that was originally anticipated is high-pressure oxidation. In this technique, the wafers are placed in a special high-pressure chamber and oxidized under a steam ambient of 10 to 20 atmospheres. This greatly increases the oxidation rate, which means that at a given temperature, one can grow oxides more quickly. Therefore, one can grow the same oxide in the same time at lower temperature. This provides better diffusion control and less damage to the wafer caused by oxidation at high temperatures. Yet few systems have been sold, and the application of this technology has been very slow. Many fab managers are concerned about potential safety problems, although Dataquest believes that the units are exceptionally safe. Their one disadvantage is that because of expense and time considerations, the wafer loads must be quite large (several hundred wafers). Some managers do not want to process that many wafers at one time. Another reason that this process is not widely used is that the units themselves occupy a great deal of floor space and manufacturers are reluctant to redesign the units to fit into smaller areas.

Passive Insulators

The two major functions of passive insulators are topside chip passivation and insulation between the polysilicon and the metallization (or between two metal layers). For topside passivation, the standby has been chemically vapor-deposited silicon dioxide doped with phosphorus (phosphosilicate glass or PSG). The glass is doped to a level of

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3 to 5 percent phosphorus (by weight). However, due to the hygroscopic nature of PSG and the use of plastic packaging to lower package cost, silicon nitride deposited by a low-temperature plasma reaction has become the preferred topside passivation material. Whereas the action of PSG was to entrap mobile ionic contamination in the glass, the action of nitride is that of an ionic barrier. It is also free of any moisture sensitivity problems. The skill is to put the film down with a low enough internal stress to keep the film from delaminating. Dataquest expects nitride to continue to be the preferred topside protection material in the near future.

The choice of insulator to separate metal from poly or metal from metal is less clear cut. The insulator to separate poly from metal in the N-channel technology has been PSG, but with a much higher doping level (7 to 8 percent P). The reason for the higher phosphorus content was to allow the glass to reflow at high temperatures, smoothing out step contours and making metal coverage over poly steps easier. This has worked well, but is not without its problems. A process engineer has the choice of high phosphorus content and low reflow temperature or low content and high temperature. High phosphorus content means that the films are very moisture sensitive, and resist adhesion is a problem. Thus, in an effort to reduce process temperatures, one could create a photoresist masking problem. Etching of contacts through PSG is also difficult. Finally, most PSG is deposited in atmospheric CVD (chemical vapor deposition) systems, which causes particle problems. Therefore, PSG is falling out of grace for VLSI devices.

In the last few years, many contenders have come forward to displace or attempt to displace PSG. One serious contender is BPSG (borophosphosilicate glass). BPSG will reflow at lower temperatures and there is some etch sensitivity improvement. However, the particulate problem still exists, and while better than PSG, it does not seem to have many advantages over its rivals.

Plasma-assisted oxide deposition is becoming popular in that the films as-grown show good step coverage and do not need reflow. The films etch well both wet and dry. Its chief disadvantages are that film stress must be carefully controlled or the film will delaminate, and that the equipment is relatively expensive. Since step coverage is quite good and the deposition occurs at low temperatures, this material has gained wide acceptance as the insulator between two metal layers.

Plasma nitride falls into the same category as plasma oxide. Its chief disadvantage is the higher dielectric constant, which increases the capacitance between metal and poly or metal and metal. Therefore, polyimide (a long-chain polymeric material) is a possibility for an interlayer dielectric. It is self-planarizing and covers steps extremely well. It is a bit difficult to etch, however, and control of its properties has been a problem in the past. Military applications have not accepted it, and we expect that this material will be a long time proving itself. If the problems with the material properties and the reliability of the devices can be improved, this could become the dominant choice.

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The current first choice for poly-to-metal isolation appears to be TEOS (tetraethylorthosilicate) glass. This is easy to apply to the wafer at relatively low temperatures (650 degrees C), has excellent step coverage, and because there is no phosphorus in it, it is easy to coat with resist and etch. It is also inexpensive. The predominant trend is TEOS for the poly-to-metal dielectric, and plasma oxide or polyimide for metal-to-metal isolation.

All of the preceding techniques are fairly conventional as far as the equipment or technology is concerned. One new technique is photochemical deposition of silicon dioxide or silicon nitride. The action is initiated by an intense ultraviolet discharge in the presence of either silane and nitrous oxide or silane and ammonia. This will produce an oxide or nitride film at 50 to 250 degrees C. However, there must be some mercury vapor present. Mercury's side effects on the process are not well characterized. It does produce reasonable films, however. Film stress is minimal as long as no further high temperature steps are used, but since die attach occurs at 380 degrees C, the low temperature advantages of the process become quickly lost. It may be used in a few unusual applications, but it is not likely to displace the more conventional means of CVD.

Doping Technology

There have been major changes in this area during the last few years. All the control afforded by direct digital control of diffusion furnaces has had a minimal impact on the continued use of "conventional" diffusion sources for VLSI. Even with better temperature and gas system control, the uniformity of liquid or gaseous diffusion sources has not been up to the level required for VLSI and the 256K RAM, with the possible exception of the doping of the polysilicon layer to lower sheet resistance. In addition, the toxicity of many of the dopant sources involved has convinced many that there are much better ways to go. Since cleanliness and control are the watchwords in this business, conventional doping sources are for the most part being left behind. One major improvement has been the development of solid source phosphorus using a technology similar to that of boron nitride. This seems to give good results, but since the majority of all VLSI source-drain diffusions are done with arsenic, solid phosphorous sources will find its use limited to poly doping. This technology is highly desirable for poly doping since there is no residual chlorine and the process does not use or evolve hydrogen, which can enhance the diffusion of phosphorus through the gate dielectric with disastrous consequences.

Ion Implantation

The preferred method of doping is ion implantation, with larger and larger currents becoming available. Since current is a direct measure of throughput, theoretically the higher the current the more wafers can be processed in a given time. But high current, particularly with heavy ions such as arsenic, can lead to substrate damage. This residual damage is difficult to eliminate, and causes leakage currents in the device. Since fairly small stored charges in the memory are involved, leakage is a critical factor. To control this requires not only the proper amount of substrate cooling during implant, but also proper post-implant annealing. Beam currents of 10 milliamperes are readily achievable today and reliable dose monitoring up to 10^{17} ions/cm^2 is available.

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The present thrust in ion implantation is the reduction of floor area. Machines used for this task have tended to be extremely large in the past. With the rise in the cost of clean space, the implanter is a conspicuous target for size reduction. The instrumentation on today's implanters is quite accurate, and wafer uniformities and dose repeatability of 0.5 percent seems to be the state of the art.

There are a few methods in current use that are totally dependent on the use of an implanter to set the source and drain junctions. Lightly doped drains are quite popular in the 2-um region. This technique places an n-region between the channel and the more heavily doped source and drain region to reduce the electric field at the edges of the channel. This reduces the short channel effects on the electron mobility and lowers parasitic capacitances. Many devices currently in the 256K RAM marketplace use multiple device thresholds, in which there are not only enhancement and depletion devices, but devices with different thresholds. It is common to have peripheral circuitry with thresholds targeted to provide TTL level compatibility, and internal circuits, such as the RAM core, with much lower threshold voltages to boost device speed. All of these thresholds are adjusted via ion implants.

Annealing

Traditionally, all implanted devices were returned to the diffusion furnace for anneal and activation of the implants. Even if "conventional" diffusion sources were not employed, there was still a market for the diffusion furnace. While we expect that there will always be a few diffusion tubes for oxidation and CVD applications, the hot wall furnace tube is being challenged by a technique called RIA or rapid isothermal annealing. The wafers are introduced to a small purged chamber a wafer at a time, and then rapidly heated to the desired temperature by either direct resistance heating of a susceptor or by infrared heating with quartz halogen lamps. While there is some discussion regarding the annealing of high-dose implant damage, this technique appears to be clean and repeatable, allowing implant activation with minimal junction movement. It also shows promise for wafer alloy and silicide formation. It has a very low sample chamber volume, which permits a very controlled environment and a high-gas velocity. In addition, its cost is low and it requires minimal floor space. Dataquest believes that this will emerge as a beneficial (both economically and technologically) piece of equipment in the years to come.

Although it is possible to do the same rapid annealing with an electron beam (e-beam) or a laser, these techniques have found minimal utility and appear impractical. E-beams require high vacuum which translates into high cost, potential contamination problems, and troublesome mechanisms required to automate them. Lasers, while not requiring a vacuum, have selective absorption resulting in uneven wafer temperatures. While there may be a few novel techniques that could use laser heating, quartz halogen lamps as used in RIA have far fewer problems. Dataquest believes that RIA will become standard practice for VLSI.

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Epitaxy

At the introduction of MOS circuitry, one of the chief benefits of MOS technology was its simplicity of processing. It required a minimal number of masking steps and could be made on bulk silicon. Over the years, the processing of MOS devices has become more complex. Until now, it has retained its freedom from epitaxy. As the circuit elements become smaller and smaller, the device requirements become more stringent. Some companies, such as Texas Instruments (TI), believe that many of the shortcomings in ROM technology can be overcome by epitaxy. TI currently mass produces its 64K device with epitaxial technology. According to TI, the advantages are:

- Higher minority carrier lifetimes in the epi layer for better refresh characteristics (TI claims improvements in refresh interval of 10 to 15 times.)
- Improved oxide defect density
- A backplane formed by the higher conductivity substrate which minimizes spurious coupling of sensitive circuitry
- Substrate that acts as a minority carrier sink due to its poor minority carrier lifetime

These claims are valid, but there is a question of whether the gains of epitaxy outweigh the problems and extra costs involved.

To answer this question, one must look at today's epi technology to see if these layers can be produced economically. The radiantly heated epi reactor is radically different from the horizontal RF-heated reactors of the past. The newer reactors are cylindrical with the wafers mounted vertically. Radiant energy from quartz-halogen lamps provides the required heating. These reactors produce films of exceptionally high quality, with very low slip and internal stress. Since the epi films required for 256K technology are relatively thin (1 micron), deposition time is quite quick, and therefore, outdiffusion from the substrate is minimal.

In addition to the radiant reactor, significant improvements are being made in RF-heated reactors. Since the wafers are heated conductively through the susceptor upon which they sit, the somewhat uneven heating causes a higher degree of slip in the epi layer than in the radiant method. While this is acceptable for linear and discrete devices, it cannot be tolerated for MOS. Therefore, improvements are focused on reducing slip. It remains to be seen whether equipment vendors can overcome this obstacle.

MOS manufacturers have scrupulously avoided epi; for the most part they do not trust it. Unless manufacturers have considerable expertise in epi (e.g., TI), it is not likely a technology that they will embrace. Also, minor surface defects that would have no effect on bipolar devices could be critical to MOS.

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Even if these technical and attitude problems can be overcome, there is a question of whether epi can be made economical for VLSI. From bipolar technology, we have learned that epi is an expensive technology. Even in high volume it can add $3 (yielded) to the wafer cost. This adds a lot to the selling price of a 256K device, which uses a large die. Second, epi is a tricky process that requires a great deal of specialized hands-on engineering to keep it running smoothly. Third, epi reduces yield. An example of this can be seen in the triple-diffused processes for VLSI as opposed to epi processes. The triple-diffused processes yield much better.

An alternative to the deposition of epi layers by semiconductor manufacturers is for them to buy wafers with an epi layer already deposited. Since there are no patterns under the epi as there are in bipolar, it is possible to buy stock epi wafers. Standards have not yet been defined; we believe that they must be or epi will always be a special process with different thicknesses and resistivities for each manufacturer, and the economies of scale will not be reached. If epi is to take hold in the 256K area, the purchase of epi silicon will be a reasonable alternative for most MOS manufacturers. (Note: Applied Materials, Anicon, and Gemini have announced new epitaxy systems for production of epitaxial films for CMOS devices.)

Metallization and Polysilicon

Basic polysilicon technology has not changed much over the last few years. Low-pressure chemical vapor deposition is the standard means of poly deposition today. For the most part, poly is deposited undoped and later doped with phosphorus to a sheet resistance of 10 to 20 ohms per square. Some attempts have been made to produce depositions with doped poly (all in one), but these systems have proved temperamental. The addition of phosphorus in the deposition process tends to cause heterogeneous nucleation which grows spikes or outcroppings in the poly films. Since the goal is for lower defect density, this is counterproductive.

Polysilicon is a material that is well suited to IC manufacturing. The push to VLSI has put pressure on polysilicon's most serious weakness: sheet resistivity. For films 0.35 to 0.45 microns thick, resistivities below 10 ohms per square are a real problem. Doping the film more does not change the resistance, and can cause etching problems along with increased potential for phosphorus penetration of the gate. The sheet resistance of the poly causes propagation delay problems; it would be highly desirable to reduce the sheet resistance to less than 5 ohms per square. The material must be refractory or quasi-refractory since it must be stable under the high temperature processing steps that follow poly deposition. One possible choice would be refractory metals such as tungsten, tantalum, titanium, or molybdenum. These metals can take the heat of the processing (as long as the oxygen level in the ambient is low) and are relatively easy to pattern. Their chief disadvantage is their difference in work function from silicon, which requires major changes in device processing. They also must be carefully deposited, or some interface stability problems can result.

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A better choice would be the deposition of silicides, such as titanium silicide, tantalum silicide, molybdenum silicide, or tungsten silicide. These materials can be sputtered or chemically vapor deposited directly on the gate oxide, and yield films of excellent stability. Their chief disadvantage is that they are difficult to etch.

Both of the above techniques require some substantial redirections in processing. To minimize these changes, the easiest choice to implement is the so-called polycide shunt. The polysilicon is topped with a layer of refractory metal, then the metal and poly are heated to a high temperature and reacted to form a silicide coating on top of the poly. The work function and stability of polysilicon at the polysilicon dioxide interface are retained while obtaining the low sheet resistance desired. There are many ways to pattern the film, and depending on the manufacturer's choice, the silicide can be formed either before or after the composite film is patterned. Regardless of the method used, polycides and silicides are needed for this technology. We expect polycides to be used until better etch techniques are developed for silicides.

Silicides have another important use in VLSI circuits. In 64K RAMs with junction depths of 0.5 micron, it is still possible to reliably contact the junctions with aluminum-silicon metallization and not alloy through the junction. With the 256K RAM's 0.25-micron junction depths, this is no longer possible and the contacts must be silicided prior to metallizing.

One of the most commonly used silicides is platinum silicide. It is easy to form and is stable. Platinum is sputtered into the contact windows and reacted with the silicon at elevated temperature to form the silicide. Excess platinum is removed and the wafers are now ready for metallization. Titanium must be deposited first to act as a barrier metal. This is usually done in the same sputtering system that is used to deposit the aluminum films, so that the two sputterings can be done sequentially without breaking vacuum.

The choice of which aluminum alloy to use for metallization is quite important. With aluminum linewidths down in the 3-micron range and going lower, current density climbs rapidly. The addition of copper to the aluminum film retards electromigration at high current densities. The choice of copper content is a hotly-debated subject, however, particularly among those who have to etch these aluminum-copper films. Even though sputtered films are highly homogeneous on average, plasma etching of films shows a large amount of microsegregation, which makes these films difficult to etch. A concentration of 2 to 3 percent copper seems reasonably easy to etch and still provides the necessary electromigration resistance.

The metal films are deposited in much the same way as they have been since 1975. What has changed is the level of automation used to produce the films. Today's most popular systems are fully automated cassette-to-cassette systems. The wafers are sputtered in a vertical position to reduce contamination and lower defect density. Sputtering takes place at very high rates to maximize throughput. Manufacturers and users have both belatedly realized that precise control over deposition ambient is essential to the control of etching, and as a result, most systems come with residual gas analyzers to monitor system performance.

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Most of today's 256K designs are single-layer metal. To reduce the die sizes down to more economical levels it is clear that they can't push too much, at least in the short term, on the feature sizes. The current design rules are aggressive enough for the next round or so. Dual-layer metal can help, and although it costs two extra masking steps (the via contact and the second metal), it can make a tremendous difference in die size. The smallest 256K RAM is 46 mm^2 with single metal. NEC's device with dual-layer metal is 34 mm^2. That is a major size decrease and one that will pay off handsomely in yield. Although most of the current first round offerings in 256K RAMs are single-layer metal, economic pressure will force the participants to dual metal for the next generation.

Photolithography

A battle is continuing between stepped projection mask aligners (steppers) and scanning projection mask aligners to win space on the manufacturing floor. To sort out the superiority claims, it is necessary to understand the fundamental limitations of each piece of equipment. If one were to define the technological capabilities of any semiconductor manufacturing line, the first item to be evaluated would be the photolithography area in both the equipment and the photoresist process.

Contact/Proximity/Projection

Traditionally, wafers were processed with 1X photomasks. The wafer was held either in vacuum contact with the photomask or in near-contact (proximity). These techniques, along with the proper choice of resist, can result in the ultimate in resolution. The trade-off is defect density. If a particle on a wafer is crushed against the mask, it not only ruins that location on the wafer, but also damages the photomask and hence all subsequent wafer exposures. Promixity alignment is a natural progression, but it too has its problems. The wafer-to-mask gap is usually 10 to 20 microns. Setting this gap precisely presents many problems, and some large particles can still damage the mask. Proximity aligners have been used successfully on gate array devices with relatively low component densities. However, for dense devices such as the 64K and 256K RAM, the defect density cannot be reduced below 5 to 6 defects per square inch which is borderline for economy on the 64K, and unsatisfactory on the 256K devices. The mid-seventies saw a swing to the scanning projection aligner in which the mask and wafer never came in contact. The image of the photomask was projected on the wafer—a technique that would seem to solve the defect problem handily. The problem became resolution and size control of the image across the wafer.

Steppers

The introduction of the stepper in 1978 seemed to solve these problems by stepping a small field reticle (typically a 10X version of the circuit) across the wafer. Runout and resolution were impressive, and defect density (4 defects/square inch) was very low. This appeared to be a good solution, except that steppers had a very low throughput, which clouded the economic picture.

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The steppers of 1984 as used in 256K technology, bear little relation to the initial steppers. The optics have been greatly improved, as have the light sources. "Writing" speeds are much higher, boosting the throughput of the devices. In addition, steppers can now handle 6-inch (150 mm) wafers, and very importantly, steppers occupy much less floor space than before. Many semiconductor manufacturers require die-by-die alignment on large devices such as the 256K, as well as accurate prealignment of the wafer. Typical throughputs today for a stepper are 65 100-mm wafers per hour or 55 125-mm wafers per hour. This number is somewhat misleading since setup time is not included; i.e., focusing on the reticle and exposure setup. It can take up to 40 minutes to change reticles manually and set up on the new reticle. For a multiple product line such as a custom VLSI facility, throughput can be cut in half by set-up time. Stepper manufacturers have introduced reticle changers with only modest success. The intention was to have a library of reticles stored in the machine and change them automatically, saving handling and time. The fact is that none of them really work very well and the time saved is not significant. The RAM manufacturers have "solved" the problem by dedicating a single stepper to a single mask layer. Thus, for a 6-mask process one would need at least six steppers. This is a rather expensive solution but it does solve the problem, assuming that all of the steppers have been calibrated or "matched" to work with each other. Today's steppers have a registration error of +/-0.5 microns or less, which is generally sufficient for today's technology.

The stepper has become the standard tool for 256K production, and stepper manufacturers are working on improved lens systems. Lenses come in three sizes: 10X, 5X, and 1X. The 10X lens gives the best resolution but the lowest throughput, since more steps are required to cover the wafer. At the other end, the 1X lens has maximum throughput, but suffers on resolution. The 5X is a reasonable compromise. In fact, 1-micron resolution is available on select 5X lenses today. With changes in lens design and the use of shorter wavelengths, we expect steppers to be able to eventually handle linewidths down to 0.7 to 0.8 micron, and thus be the equipment of choice for micron and sub-micron work.

Scanning Projection Aligners

Meanwhile, scanning projection manufacturers have not stood by and watched their market share dwindle. Initially, their strategy was throughput, and when steppers also improved throughput, the key words became "mix and match" (i.e., the use of steppers for critical layers and scanners for noncritical layers). This strategy did not work well, particularly for VLSI devices such as the 256K RAM, since getting two diverse pieces of equipment functioning well together was very difficult. Equipment vendors then attempted better resolution which was a real disadvantage for projection manufacturers. Now, at least two vendors (Perkin-Elmer and Canon) have all-reflective optical scanners capable of 150-mm wafers and 2-micron resolution in production. In addition, they claim throughputs at close to 100 wafers per hour and a cost that is 60 to 90 percent of stepper cost. The reflective system lends itself to shorter wavelengths than the refractive optical systems of steppers. However, they still provide inadequate resolution for the 256K RAM. Scanners are good for custom VLSI of 2-micron minimum linewidth and very large die sizes such as in wafer scale integration where die sizes require multiple reticles on a stepper. The stepper represents the only economical

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choice for machines with some technological mileage left to go. Even if the resolution could be pushed below two microns (and it probably can), the scanner still suffers from a poorer overlay alignment accuracy that the die-by-die stepper can easily beat.

Optical Resolution

One way of improving resolution is to shorten the wavelength. The light source for most optical equipment in today's semiconductor factories is the mercury arc lamp. The optical spectrum of a mercury arc lamp contains several distinct lines. In scanners, the full spectrum of the lamp is presented to the resist or one of the spectral lines can be chosen and a more monochromatic illumination used. Typically, these systems have focused on the near-UV spectrum (350-450 nm), primarily because of the low absorption of UV light by the optics and their high inefficiency at lower wavelengths.

With the improvements in stepper lenses and the use of all-reflective scanners, systems can now be built that go to deep UV (250 to 300 nm). This will improve the resolution, but the cost of all materials in the optical path, including the photomask or reticle, will increase dramatically. Very high purity quartz is required, and ozone production at these wavelengths due to interaction with oxygen molecules is a problem. There are some deep-UV systems on the market, but they have not lived up to expectations. We believe that the near-UV range will continue as long as refractive optical systems are in use. If deep UV does become widely used, it will be in the scanning projection area where the economic penalty for deep UV is not as severe.

E-Beam Technology

There are also some non-optical lithography methods on the horizon that could play an important role in VLSI/256K production. Electron beam technology is the mainstay of mask manufacturing for VLSI circuits. Direct writing on the wafer has been promised, and it now appears that it will be available soon. Electron Beam Corporation (EBC), Perkin-Elmer, and Varian have announced systems that claim to have a 0.75-micron resolution. The problem is a throughput of about 20 wafers per hour. At that rate, it is hard to conceive of a manufacturing line producing 25,000 wafers per period with e-beams! One must also be careful when talking about e-beam throughput to quote both feature size and wafer size. If the throughput problem could be solved, the systems will require an overlay accuracy of 0.1 micron and that will be difficult to achieve on a production basis. Optical lithography will reach a limit at the 0.7-0.8 micron range so e-beam would seem to have an open field.

X-Ray Technology

X-ray technology is also looming on the horizon. Micronix Corp. introduced the first commercial x-ray exposure system in 1983, with a specified 0.5-micron resolution and a registration accuracy of 0.1 micron. Because of the short wavelength of x-rays, resolution should be quite good. Energy scattering within the resist is negligible and dust would be transparent to x-rays. Current work is centered on the improvement of the x-ray target and the masking technique.

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Masks are quite complicated. They are constructed from 3-micron-thick mylar with a good overcoating that has been patterned by an electron beam exposed photoresist. Micronix has developed a 6-um boron nitride membrane with a gold absorber. Currently the exposure systems are contact or proximity type, which is bound to increase defect density. There is also some question about radiation damage to the devices, which could prove detrimental for MOS. The problems of operator safety around x-rays also pose a problem, whether real or imagined. Since VHSIC (very high scale integrated circuits) contractors have chosen x-ray as the choice for 0.5-um linewidths, it has an excellent chance to be the dominant technology in the 1990s.

Ion Beam Technology

The first commercial introduction of an ion beam exposure system occurred in 1983. Resolution should be no problem with a beam size of 0.1 micron. Many within the Defense Department see this as the ultimate technology. There are two types of ion beam technology:

- Focused Ion Beam (FIB)--Similar to e-beam only using an ion source. As with e-beam, it will be difficult to get 0.1 micron registration.

- Masked Ion-Beam Lithography (MIBL)--Uses a "hard" mask similar to x-ray system, but the mask does not have to be in contact with the resist.

These technologies are more complicated than e-beam technology and suffer from the same problems. We do not expect to see ion beam systems in use before 1990. We expect that their introduction into manufacturing will be through mask repair.

Photoresist Technology

In the previous section, photolithography was discussed from an equipment point of view, with the photoresist "going along for the ride." The fact is that the photoresist and the exposure systems are tightly linked. While it is possible although not desirable to make up for the deficiencies of an exposure system with photoresist, it is seldom if ever possible to offset a photoresist weakness with equipment. With a few exceptions, all the VLSI technology today is produced with positive resist. Through techniques of quality control and improvements in polymer chemistry, today's resists are cleaner and more predictable than ever.

Multilayer Resist Schemes

The majority of VLSI/256K production is handled with single layers of resist for dimensions above 2 microns. Problems arise where step heights of 0.5 micron or greater are encountered. As the layers build up on top of one another, the step heights mount and depth of focus for fine line becomes a problem. The resist must be planarized so that the image, or at least the initial image, is formed on a virtually flat surface. This is where multilayer resists come into play. There are three popular schemes.

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The first is the single-resist, dual-level process. In this process, a normal resist layer of 1.5 microns is spread across the wafer. Resist as-spun tends to be self-planarizing, and as a result, the surface is virtually flat. The wafer is then flood-exposed nonselectively to UV light after baking. Next, a thin layer of the same resist is spread on top of the existing layer to a thickness of 0.8 micron. It is into this thinner top pattern that the resist image is formed. The top resist is developed after exposure, and as it develops, the blanket-exposed resist underneath is developed away with the top resist acting as the etch mask. This has advantages over single resist, but the developer does undercut the top pattern somewhat. To overcome these problems, reactive ion etch (RIE) can be used, but it relies on the differential etch rate of polymerized vs. nonpolymerized resist.

A second scheme is the dual-resist, dual-layer. This technique is the same as the one above except that a different resist is used as the topmost resist (dual-resist system). The advantage here is that the top resist can be sensitized to x-ray or e-beam, whereas the bottom resist is a straight optical resist. This technique has the advantage that the selective etch rate in RIE can be biased to the user's advantage. It is a practical scheme for thickness/height (aspect) ratios greater than 1:1.

The third scheme is the tri-level resist. This technique is similar to dual-resist, dual-layer, but between the two resists is an interposed layer of plasma-deposited oxide or sputtered metal. The topmost resist is used to define a pattern in the interposed layer, then that layer acts as a mask for the RIE of the bottom resist layer. This provides the ultimate in linewidth fidelity since the RIE is chosen for a near zero etch rate on the interposed layer.

The majority of all 2+ micron work is done with a single layer of resist purely for economic reasons. For dimensions between 1.5 and 2 microns, dual-resist, dual-layer is preferred. For dimensions of 1.5 microns or less with good dimensional control, tri-level becomes essential. As 256K technology goes below 2 microns, we foresee that tri-level will become the dominant technology.

While not strictly a photoresist, anti-reflective coatings (ARCs) are gaining in popularity for VLSI work. These coatings are spun onto the wafer prior to the photoresist application. The ARC gets exposed and developed concurrently with the photoresist, and manufacturers claim a 95 percent reduction in reflected light in the near-UV. While this sounds as if it should improve linewidth control, particularly over steps, it generates a few problems of its own. ARC's exposure sensitivity is a strong function of bake temperature. If this can be controlled, it will become a valuable addition to the process.

For electron beam or x-ray technology, different resists must be used. These resists are available in both positive and negative varieties. COP and OEBR-100 are the most popular negative e-beam resists, and PBS and PMMA the most popular positive e-beam resists. These are available in different formulations and it is possible to fine-tune the resist to the particular application. COP and PMMA also make good x-ray resists.

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A key element in resist processing is the level of automation. The track/spindle system is the most popular today and consists of the following steps:

- Wafer scrubber to remove foreign particles, followed by a dehydration bake
- Application of an adhesion promoter such as HMDS (hexamethydisilizane) (This is often done off-line in a separate oven with an HMDS ambient, and some manufacturers have introduced in-line HMDS modules as part of their systems.)
- The resist application
- Soft bake using infrared conduction (so-called hot plate bake) or microwave baking

Infrared is inexpensive, but it heats the resist from the outside in and the temperature is highly dependent on the reflectivity of the underlying substrate to IR. Thus for a given bake oven setting, oxides will bake at a different temperature than metals. Since this can dramatically affect the exposure sensitivity and resultant line width, IR is less than desirable. Hot plate bake is also a step backward, since that is how wafers were originally baked when photoresist technology was in its infancy. Here, the resist warms from the inside out and is not reflectivity sensitive. Integrating this into track processing systems has insured the viability of this technology. Microwave heating is another inside-out heating method and gives good results. The equipment is expensive, however, and many people are concerned about leakage of microwave radiation.

After resist processing, the wafers are ready for exposure. Many systems are now being interfaced directly to the aligners. This reduces handling and improves defect density. It also allows for control over wait times between coat and expose. Following exposure, the wafers are developed and here, automation has not helped too much. Spray developers have notoriously poor temperature control, and therefore linewidth control suffers. About one half of all developing is still done in carefully temperature controlled baths with filtered developer. Robot handlers are being used to automate this batch process and achieve better control. Hard bake still takes place in the convection oven as it has for many years. It is a very cost-effective production step.

Processing today with its high current implanters and plasma etch equipment needs resist that can hold up to temperatures in the 200 to 250 degrees area. There are some specific resists made for high temperatures, but these are expensive compared to "normal resists." One technique for hardening resist uses a brief $CF_4/0_2$ plasma to create a hardened skin around the resist so that it will not flow at elevated temperatures. Another technique uses deep-UV hardening of the resist after developing. This can be implemented in track processing, and several manufacturers produce equipment for automatic deep-UV exposure. This equipment can also be used for the UV flood in multi-layer resist schemes.

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The removal of the photoresist, or resist stripping, hasn't changed very much over the last decade. Plasma resist stripping in an oxygen plasma is widely used, but is generally not sufficient in itself to remove all residues. Scanning ion microprobing of plasma-stripped surfaces shows metal residues, largely tin. These are not desirable, so most people finish off plasma-stripping with a wet clean in sulfuric/ peroxide (Caro's etch), sulfuric/ammonium persulfate, or fuming nitric acid. The fuming nitric acid, a strip popular outside the United States, can be used after metal mask, as can some improved non-phenolic room temperature strippers. Removing resist after plasma etch or ion implant is a real problem since the resist is firmly attached to the wafer. Multiple stripping procedures are usually required to remove the resist. In the setup of a manufacturing facility, allowances must be made to accommodate these special resist strip procedures in order to remove this heavily polymerized resist.

Etching Technology

With the advent of plasma etching, many people expected wet processing to be phased out. However, it has been 10 to 12 years since the development of plasma processing, and wet processing is still used for 60 percent of all processing etching and cleaning. Fabs today may need less DI (deionized) water than they did in the past, but they still use DI water. There are some very good reasons why wet processing will not relinquish its hold.

Among them is initial wafer cleaning. This is to remove any residues from the wafer polishing and lapping procedures, and is used prior to the initial oxidation of the wafers. While most wafer suppliers deliver a product that is suitably clean, many wafer fab people adopt a pragmatic attitude about cleaning. They know theoretically that it is not always necessary but they prefer a little "insurance." These cleans are fairly elaborate and consist of mixed acid cleans, DI rinses, 10:1 Hydrofluoric acid dips, and other processing as needed. Diffusion engineers tend to be dogmatic about these cleans, and once established, it is almost impossible to eliminate them; thus, they are not likely to disappear. These cleans have been automated with mixed success in prediffusion cleaners (PDCs). This removes most of the operator involvement, but because the wafers are sprayed with a hot acid mixture, it is difficult to determine the exact temperature due to the cooling effect of the spray action. However, even with this uncertainty, it is far less time-consuming than the old hot bath method. Some have used the hot baths with a walking-beam cassette handler to automate the process.

Another use for wet processing is in wafer cleaning prediffusion. The same argument for initial wafer cleaning applies here, but the argument is even stronger. This is an "insurance clean" so that there are no residues left on the wafer from the resist processing operation. Automation is the same as discussed above.

Wet processing is also used for general oxide etching. Plasma oxide etching is quite effective, but expensive. Not all layers in the process require the tight control of feature sizes that is provided by plasma oxide etching. Therefore, wet etching, which is 10 percent of the cost of dry etching, will continue to be used.

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Resist stripping was discussed in the Photoresist section; we expect wet processing to continue to survive here as both necessary and cost-effective processing. This, too, can be automated either by the walking-beam processing or in a PDC. The walking-beam system has much better temperature control. One advantage to the PDC is the smaller footprint of the equipment.

There are still some manufacturers who prefer wet etching of metal. Wet etching of metal down to a 6-micron pitch is feasible on a production basis with the right equipment. Manually submerging the wafers in a temperature-controlled bath does not give very good results, but if the proper equipment is used to automate the process, it can be an extremely low-cost operation. Etching below 6-micron pitch is very difficult, and most people prefer to use plasma etch. Of all the wet etching techniques, Dataquest predicts that this will be the first one to disappear.

Plasma Etching

Plasma, or dry etching, has established its place in VLSI technology. There are three distinct types of plasma etching:

- Barrel or cylinder plasma etch
- Parallel plate plasma etch
- Reactive ion etch

In order to understand the impact of each, we need to understand their limitations.

Barrel or Cylinder Etching. Barrel or cylinder etching was the original form of plasma etching. The wafers are stacked along the axis of a cylinder and a plasma is formed in the cylinder. There was some initial concern about radiation damage within the plasma, so the technique was modified to place the wafers in the field-free region of a Faraday cage. This way, the plasma did not contact the wafers. The reactive species formed by the plasma drifted through the mesh openings in the cage, and etching took place. The major problems with this technology were poor etch selectivity, radial etch sensitivity (the outer perimeter of the wafer etched faster than the center), and batch volume sensitivity (the more wafers, the lower the etch rate). For the tight linewidth controls needed for VLSI/256K devices, the barrel reactor is virtually useless. it still has some major uses, however, where dimensional control is virtually unimportant, such as nitride stripping after selective oxidation, etching of nitride for bonding pad openings, and the removal of photoresist.

Parallel Plate Etching. In parallel plate plasma etching, the wafers are placed in the plasma formed between two parallel electrodes. Here the etch selectivity can be increased and the etching is more uniform. This is widely used for etching aluminum, for hardening of resist as discussed earlier, and for removal of silicon precipitates after aluminum-silicon etching.

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A particular type of parallel plate system is the single-wafer-at-a-time system, typified by Tegal. The wafers are cassette unloaded one at a time into a chamber, which is then evacuated and the plasma process initiated. Etch rate is much faster (up to 1 micron per minute) but the power density is also high. For aluminum etching, because of the power density being higher, radiation damage can be a problem. Drytek has a variation on this in which multiple parallel plate reactors are formed inside a vacuum chamber. This way, the power can be lowered, reducing damage and etch rate, but still maintaining throughput. One chief advantage to the wafer-at-a-time system is that wafer size is relatively unimportant and 150 mm wafers are readily accommodated.

Reactive Ion Etching. Reactive ion etch is the logical extension of parallel plate etching. When electrode spacing becomes narrower, not only do the reactive species do the etching, but there is a high degree of physical and chemical sputtering. This produces a highly anisotropic etch and a high degree of etch selectivity. Since this is of paramount interest in VLSI work, the remainder of the discussion of etching will focus on RIE and its variants.

RIE is used for poly etch, oxide etch, nitride etch, and metal etch, as well as for the "developing" of photoresist. It has had a major impact on the semiconductor industry, and together with today's photolithographic advances has made the present technology manufacturable. The most popular configuration is the hexagonal cathode or hexode. This technique was originally invented at Bell Labs and is produced commercially by such companies as LFE, Plasmatherm, Branson/IPC, Technics, and Applied Materials. The idea is relatively simple.

The wafers are mounted on a hexagonal cathode surrounded by a cylindrical anode, usually a "bell-jar" of a vacuum system. The anode-to-cathode area is about 2:1. The batch configuration allows the power density to be kept low, preventing damage to both the photoresist and the wafers. Etch rates are relatively low, but batch size is large, leading to a reasonable throughput. Etch selectivity is quite good, particularly for resist with an oxide mask (e.g., tri-level) where selectivity is 30:1. Aluminum etches at about 1,000 Angstroms per minute, while poly and oxide etch at 600 and 450 Angstroms/minute respectively. Uniformity varies from 5 to 10 percent depending on the material etched, an acceptable number for today's work.

Automation has concentrated on the loading of the cathodes. Initially, wafers were loaded manually, then cassette-to-cassette loading evolved. The cassette loaders only loaded the cathode plates with wafers, and the cathode plates still had to be manually affixed to the cathode structure. At SEMICON West 1983, robot loaders were demonstrated. While these solve the automation of the process, they do not address all the problems. In all the systems mentioned so far, the wafers and the etch chamber are exposed to air for each load/unload cycle. What is needed is an isolation airlock system that keeps the chamber under vacuum at all times. This is particularly critical for aluminum etching using chlorine chemistries, since the $AlCl_3$ formed in this reaction is extremely hygroscopic. Each time the system opens to air, vacuum performance is degraded. LFE has recently introduced a hexode system with airlocks and a cassette-to-cassette loader. It entails extremely complex mechanisms operating in a

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vacuum, but if it works well, it will solve most of the problems. Currently, hexode systems have 150-mm wafer capability. A typical load of 100-mm wafers is 24 wafers, dropping to 18 at 125 mm and 150 mm. Most of the hardware must be outside the clean room walls, for today's hexode systems are relatively large.

The latest developments in RIE are magnetron etching and triode etching. The physics involved in magnetron etching is similar to magnetron sputtering. A magnetic field is employed to confine the electrons in the discharge and thereby increase the plasma density. This will allow high etch rate at low power. Magnetron etching also takes place at a vacuum that is much lower than straight RIE. While RIE has difficulty handling oxide etch rates greater than 500 Angstroms per minute, magnetron etching is an order of magnitude faster. Uniformity is competitive with straight RIE. The advantage is throughput. An order of magnitude is worth a good deal, particularly in the reduction of floor space for a given productivity. All of the magnetron etching is still unproven in production, but it appears to be a viable technology. Since it is faster and more compact than the hexode system, Dataquest believes that magnetron etching will become a competitive technology for high-volume production. For custom VLSI operations, this parallel plate RIE system is extremely cost-effective and requires a minimal amount of floor space.

The triode system uses high power to obtain high etch rates, as opposed to the magnetron which uses a magnetic field. It must therefore remove the excess heat from the wafer with sophisticated wafer cooling techniques. It does have high throughputs in a single-wafer configuration, and operates at low pressure. GCA has recently introduced a triode system; this system is under evaluation by a number of semiconductor manufacturers.

Plasma Process. Plasma chemistry plays an important role in VLSI production. The proper choice of gases makes the difference between a process that is merely workable and a manufacturable process. To review all of the etch chemistries involved is beyond the scope of this report. Materials Research Corporation (MRC) has made a collection of etch characterization data available in library form on a floppy diskette which is very helpful, even if only to narrow down the choices for the "plasma soup." There seem to be as many formulations for etch gases as there are plasma etch specialists. Submicron linewidths are easily achieved, and the etch anisotropy has become so good that processes have now been implemented that slightly slope the edges for better metal coverage.

Materials Required

As mentioned earlier, control of defect levels has been the focus of all VLSI/256K processing. Since the yield is largely determined by the photomasking yield (i.e., process-induced defects caused by masking defects), efforts have been concentrated on reducing defect density during the lithographic process. Similarly, diffusion-induced defects (oxide inclusions, diffusion stresses, ion implant damage) have also come under close scrutiny. Memory manufacture, particularly in the case of the 256K RAM, is

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extremely sensitive to leakage currents. These are caused by metallic precipitates at defect sites in the silicon. Process engineers have concentrated on reduced metallic contamination and the minimization of process-induced defects. VLSI has brought manufacturing to the point where the silicon that was being used turns out to be far less than adequate. In fact, it can be argued that silicon is one of the fundamental limitations in VLSI technology.

Silicon vendors have concentrated on improving bulk minority carrier lifetime values. These lifetime figures are an indicator of the defect density in the silicon. On the whole, most vendors have made some major improvements over the years. The fact is that on the average, the values are acceptable. However, on the microscale, minority carrier lifetime varies from wafer to wafer, and more importantly, across the wafer, the concept of microhomogeneity is becoming more and more important as transistor sizes shrink and transistor densities climb. It has also been shown that oxygen precipitates can have a beneficial effect on wafers since internal gettering (the profiling of substrate impurities) is possible. The problem is that very few vendors are capable of tight oxygen control, and the interaction of high oxygen wafers with certain process schemes can be disastrous. Specifications for silicon wafers for VLSI is not a simple matter.

The microscale is not the only problem area. At each point in the history of silicon technology, the upward change in wafer diameters brings about a discovery of the old problems. As the wafers are cut and polished, stresses build up in the wafers and these must be removed. Larger diameters mean larger problems. Wafer flatness is extremely critical. Lapping and polishing are more critical with 125-mm wafers. The jump from 100-mm to 125-mm has caused numerous problems to the silicon vendors, and the situation with 150-mm is even more critical. Silicon sawing and polishing may need some new technology to make 150-mm wafers that are acceptable for VLSI. Pilot production is one thing; mass production at the level necessary for the 256K memory business is another.

Improvements are also required in the doping and specialty gases used in semiconductor device manufacture, as well as in the liquid chemicals and solvents. Incoming gas cylinders are causing some problems. The existence of minute particulates, which heretofore were always filtered out, is being questioned. Liquid chemicals are also under scrutiny. For the past ten years, MOS-grade chemicals have been available to the industry. However, many of the acids reportedly start out the same and are selectively bottled depending on assay. Microfiltration of the acids and solvents used in the process are becoming a necessity. More suppliers are now improving their products, and end users are conducting in-plant assays in addition to the factory assays. Liquids are carefully checked for particulate densities and then filtered at the point of use. With VLSI, the risks of contamination are too great to take chances. The development of filtration media that can stand up to the harsh chemicals used in semiconductor processing still has a long way to go, but improvements are being made. Today's chemicals cannot be blindly accepted, and we believe that every major IC manufacturer must have at least the rudiments of an analytical lab to qualify incoming chemicals.

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Facilities Requirements

Changes in the makeup of production equipment have made some major changes in the requirements for an efficient manufacturing facility for VLSI devices. With stringent requirements on purity and cleanliness, many of the old clean room concepts have had to be rethought. Important changes have appeared in several areas.

Among them is a change in high-purity gas piping. At one time, copper pipe was used for nitrogen and oxygen. Hydrogen and specialty gases were handled in stainless steal pipes. Now, the entire facility is plumbed with stainless steel, with all welded joints. In-line moisture monitors are standard equipment. Gas lines are routinely checked with a gas chromatograph to insure purity levels. Because of the problems encountered with HCl gas lines and moisture, solid-welded PTFE lines are now being installed.

Because of the use of steppers and the overall requirement for fine linewidths, floor vibration is a major problem. Facility siting requirements preclude heavy vehicle traffic close to the building. Special foundations, isolated from the vibrations of the air handling equipment, must be employed.

Floor space is a precious commodity, and only the items that are absolutely essential in the clean space are allowed. Through-the-wall mounting is becoming a standard practice. Maintenance access is outside of the clean room, so that maintenance personnel can perform most of the service without entering the clean space.

Improvement of the air quality level is a very controversial issue. Most facilities today have a Class 100 room for VLSI work with Class 10 workstations. Several facilities are Class 10 throughout. Cleaning up the air to a Class 10 level and then putting people in this environment makes little sense, yet that is common practice. Some more adventuresome clean room designers led by the magnetic disk manufacturing industry, are returning to the glove box, one of the original ways of providing clean environments. Only the wafers and the important equipment are in the Class 10 environment; the people are outside. With in-line processing systems and robotic handlers, this is an achievable goal. A major benefit of this approach is the cost savings in air filtration. The volume occupied by the equipment is a small percentage of the total floor area. We believe that within five years, this will be the standard practice for all new facilities.

Robotics, as mentioned above, is essential to a "people-free" clean room environment. Robots have been used for loading and unloading in the diffusion, plasma etch, and wet etch areas. Automatic pattern recognition systems are improving, and autoalignment of wafers is common, at least with a minimum of human intervention.

Deionized water is the most widely used chemical in the semiconductor industry. The requirements for DI water have been reduced, due to dry etching, as far as quantity is concerned. The quality requirement has increased, however. The need for 18 megohm/cm water has not changed, but the emphasis has shifted to particles, colloids,

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and organics, all of which do not affect the resistivity. In-line organic monitors are becoming standard equipment. The production of DI water is a major expense in both capital and overhead for a semiconductor area. Ultrafiltration combined with electrodialysis (EDR) and reverse osmosis (RO) can produce very high-purity water at very low cost. This is then followed by a conventional demineralizing chain and the sterilization and filtration processes. Point-of-use filtration of the water down to the 0.2-micron level is now common practice in VLSI facilities.

With respect to facility design, mass production for the 256K RAM market uses the "individual bay" layout, in which each bay has its own air handling system to provide temperature and humidity control as required. Custom houses still seem to prefer the larger room, which has its merits for small numbers of wafers and low operator densities. Chemicals are either piped to the point of use, or bottles (having had their outsides cleaned) are passed through the walls into the room. Because of the cost of conditioning air, the air is reused up to the 75 percent level. This requires odor control systems using activated charcoal to keep the air cosmetically acceptable to personnel. Many facilities have constant monitoring of the internal air to detect low levels of toxic fumes or explosive gases. In the event of fire or gas leak, special dampers are activated that can rapidly clear the air of smoke or toxic fumes. Return air ducts can either be in the sidewalls or the floor. The floor return is better for laminarity, but has its problems if chemicals are spilled. A simple solvent spill can force the evacuation of the entire area if solvents flow into the return air ducts. Ionization of the air, as done by the photomask manufacturers, is used to reduce particles stirred up by personnel movement. With all the facility requirements necessitated by having humans in the clean space, it is easy to see why glove-box access is so attractive.

Waste treatment is a major concern to both the manufacturers and local governments. In today's modern facilities, the zero-effluent has become the popular design process. In this scheme, only water and certain easily neutralized chemicals go down the drains. This wastewater is treated and neutralized to an acceptable pH and ionic content, and then reused within the facility for sanitary applications and single-pass cooling. In many cases, the water that is eventually discharged into the drains is purer (at least ionically) than the water that comes from the mains. Acids such as HF are contained in special tanks and removed for off-site disposal. Thus, zero-effluent really means only that the waste is not discharged on-site. It is still there, however. Some companies precipitate out the fluorides as a sludge, but this, too, must be buried. There are fewer sites every year that can handle this waste. A serious problem concerns the wastes from dry etching. Exhaust gases are particularly toxic and must be well scrubbed. In addition, the contaminated silicone pump oils must be disposed of. Since these are contaminated by HF, PH_3, and arsenic, among other chemicals, their disposal poses some nasty problems. Waste disposal for a modern semiconductor facility has improved, but it still has some major problems.

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ECONOMIC ISSUES

The technology required to build 256K RAMs is very expensive. Not only are the semiconductor manufacturers attempting the manufacture of fine-line VLSI devices, but these devices are grouped together on a large die area. Thus they need not only fine lines and the tight tolerances that go with them, but also big chips, a combination that conjures up some undesirable possibilities.

In order to test the economics of 256K RAM manufacturing, we look at some optimum yields, that is, yields that are pretty far along the learning curve. We then model the cost to produce such a device and make comparisons against forecast market prices. The yield model employed for this analysis is approximated by Bose-Einstein statistics. The yield, Y (%), is given by the following relation:

$$Y(\%) = (1 + D_0A)^{-N}$$

where:

D_0 = average defect density and is a function of feature size
A = active chip area
N = number of critical masking steps

This yield is sometimes called the photomasking limited yield. It assumes that the yield is totally controlled by the defects created by the photomasking process, and that factors such as parasitic leakage, design flaws and sensitivities, and general design margins do not impact the yield. As might be expected, this is seldom the case, but the photomasking yield does represent the maximum attainable yield, and as such, is useful for best case economic projections. To arrive at the dice per wafer yield, Y(DPW), the Y(%) is multiplied by a factor that relates to the maximum number of whole dice per wafer. This is arrived at by removing an annulus from the outer perimeter of the wafer that has an incremental width that is the square root of the die area, A. Thus the yield in dice per wafer is given by:

$$Y\ (DPW) = Y\ (\%)\ \ 3.14\ (r - (A)^{.5})^2\ /A$$

where r = radius of the wafer.

In order to arrive at the manufacturing cost, we have made some assumptions of "typical" costs for certain manufacturing items. These are:

- Wafer Cost--Based on current 100-mm wafer costs, some 125-mm typical costs, and extrapolated 150-mm wafer costs. The wafer cost is different for the single- and dual-layer metal processes, which reflects the costs of the extra process steps involved. We used typical costs for wafer volumes of 10,000 to 15,000 wafers per four-week period.

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- Wafer Sort Cost--Based on a current average estimate of $60 per hour and the fact that one can sort four 100-mm wafers per hour. Because of the extra area involved on larger wafers, the sort time is longer; consequently, the sort cost is higher.

- Assembly Cost--The value used is based on a 16-bin plastic DIP. Organizations of the memory that would be X4 or X8 would require more expensive packaging.

- Burn-in--Costing includes a 16-hour burn-in (dynamic) as typical for most memory manufacture.

It is clear that die size reduction improves manufacturing economy. In the technical discussion of dual-layer metal technology, it was mentioned that this process could and is being used to reduce die size.

Even though the process complexity and wafer cost have been substantially increased, the overall reduction in die area improves the economics of the situation and shows a major cost reduction.

In our analysis of cost reduction, we did a sensitivity analysis by perturbing one cost-determining item, and calculated the impact on manufacturing cost. The results of this analysis are shown in Table 1. In order to see how these apply to future dice, we performed the calculation for "shrunk" dice that we expect to be shipped by late 1984.

As shown in Table 1, die area and defect density have the biggest impact. From our analysis, all of the attendant problems of VLSI can be solved; then the best opportunity that manufacturers will have will be with dual-layer metal.

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Table 1

MANUFACTURING COST SENSITIVITY ANALYSIS

Single-Layer Metal

Adjusted Variable	Cost Reduction 100 mm	125 mm	150 mm
Reduce Defect Density 10%	(9.4%)	(8.8%)	(8.3%)
Reduce Die Area 10%	(17.3%)	(16.1%)	(15.1%)
Reduce Wafer Cost 10%	(6.6%)	(6.0%)	(5.3%)
Increase Assembly Yield 5%	(5.1%)	(4.9%)	(4.7%)

Dual-Layer Metal

Adjusted Variable	Cost Reduction 100 mm	125 mm	150 mm
Reduce Defect Density 10%	(7.7%)	(7.1%)	(6.8%)
Reduce Die Area 10%	(14.7%)	(13.2%)	(12.8%)
Reduce Wafer Cost 10%	(6.2%)	(5.4%)	(5.2%)
Increase Assembly Yield 5%	(4.7%)	(4.3%)	(4.4%)

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Prototype CMOS Model

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Prototype CMOS Model

OVERVIEW

This service section deals with the design and manufacturing cost analysis of a facility dedicated to the prototype production of custom ICs. These ICs incorporate a 1.25-micron CMOS process having a double layer of metal for interconnection. These ICs are capable of extremely high gate densities (more than 2,000 gates per chip) with subnanosecond gate delays. The treatment mainly applies to a small facility, the so-called pilot line, where initial investment in processing equipment is kept to a minimum. In such a facility, the skill and intelligence of the technical people is more important than their wafer fabrication productivity.

The model is based on 500 wafers out during a four-week period. In addition, information is presented for a more productive operation of 1,000 wafers per period.

The emphasis on fast turnaround time (10 to 15 working days) leads to low labor productivity and extremely low capital equipment productivity, even though equipment costs are minimized. As a result, wafer costs are $538 per 100mm wafer. Such a wafer would have to be priced at more than $1,100 if such a facility were to supply wafer processing services on the open market. These prices are well in excess of the current market prices of $250 to $350 for a 100mm CMOS wafer. These higher costs are solely due to the investment in capital equipment and the relatively low volume of wafers produced. At 1,000 wafers per period, the costs of production are much improved and, in fact, are almost equal to the cost of procuring a wafer from a foundry.

We believe that the high manufacturing costs associated with such a line can be justified in two ways:

- Fast turnaround (two weeks) can be achieved running several different products on the line. While this level of turnaround is available on high-volume lines, it is only available on single products. The setup and mask-changeover considerations preclude this type of product flexibility on a high-volume production line.

- Such a low-volume production line allows for the retention of proprietary design with a relatively small capital investment. Although the wafer cost is high, the retention of proprietary design and the value added at the system level warrant the higher manufacturing cost.

Many engineering managers feel that once a team of engineers and technicians is assigned to a project, money is expended at a more or less constant rate until the project is completed. This rate of spending is often called the "burn" rate; a term analogous to a rocket that, once

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fired, burns fuel at a constant rate. Since even a small IC design project with one engineer and a few technicians might "burn" money at the rate of $100,000 per year, it could be argued that a 10-week schedule saves at least $20,000. This savings equals the total cost of two lots of 10 wafers each. In addition, having a product ready 10 weeks earlier might lead to other benefits such as increased market share.

It can also be argued that fast turnaround time can be achieved on a conventional manufacturing line by using the "hot-lot" technique. In this method, a portion of the wafers are processed without having to wait in the work-in-process inventory. This argument is valid until an emergency--such as high yield loss--occurs. At such a time, the economics of the situation demand that all resources of the line be applied to returning the line to full production. Any hot-lot runs are delayed for the duration of the emergency. Since emergencies occur frequently on most lines, the availability of this hot-lot service is unpredictable.

Most likely, any custom circuits intended for high-volume production that are developed on this line will be produced in another fab, and for this reason, the processes must be compatible. This is possible because in the last few years, major developments have taken place in the areas of semiconductor materials, chemicals, and gases, and in wafer processing equipment used in the industry. This, together with the availability of accurate computer simulation tools for semiconductor processes and devices, makes it possible for a small-scale wafer fabrication area to approach the type of process control formerly obtainable only on large manufacturing lines.

Clearly, a system house has a strong motivation to set up an IC fabrication facility as a means of implementing proprietary designs into silicon rapidly and with complete control. Alternatively, this need may be filled by small, efficient companies dedicated to the production of custom ICs.

Why CMOS?

It is widely recognized that many future designs are going to be implemented in silicon with CMOS technologies. Some of the reasons are:

- A CMOS gate dissipates power only during the transition from one state to the other and has negligible power dissipation during standby conditions. Thus, for a given package power dissipation and average gate delay, the maximum number of gates that can be integrated on a chip is orders of magnitude larger for CMOS circuits than for either bipolar or MOS circuits of any other technology.

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- The propagation delay for a CMOS gate is only slightly longer than for an NMOS gate. For a 1.25-micron gate length, subnanosecond gate delays are readily attainable.

- The CMOS inverter has a high degree of built-in noise immunity, since the output voltage swings completely from one supply voltage to the other.

- CMOS circuits are easy to design in comparison with other circuit forms.

For our analysis, we chose a double layer of metal for interconnections because of VLSI design considerations. The biggest challenge in complex VLSI designs is not so much the ability to place a very large number of gates on a chip, but the ability to interconnect them without errors and with a short design cycle. Industries and universities are very busy developing tools for automatic layout of the interconnections. It is generally recognized that more than one level of high-conductivity metal is going to be needed to make computer layout possible, while keeping the density of gates on the VLSI chip comparable with that of a completely manual layout with single-layer metal.

PRODUCTIVITY CONSIDERATIONS

Organization

As mentioned, the pilot line is intended to use state-of-the-art technologies to produce a small quantity of wafers with a fast turnaround time; it is not intended to be a laboratory dedicated to developing process technologies. Once the individual pieces that are part of the process flow have been installed and characterized and a complete process flow has been defined and specified in detail, the line has to run with the same general organization and discipline as a normal (high-volume) production line.

The division of labor and level of experience required for the people in the organization are different. The division of labor in the wafer fab area is different because operators are cross-trained on several pieces of equipment. This allows them to hand-carry a batch of wafers through several sequential process steps, eliminating any inventory delay. In some companies, these individuals might be called model makers to distinguish them from more conventional fab operators. A higher level of experience generally is required for most workers in the organization. This arises from the fact that the relatively small number of individuals in the pilot line must have the aggregate experience of the staff of a much larger production line if they are to be technologically competitive. A typical organization chart is shown in Figure 1.

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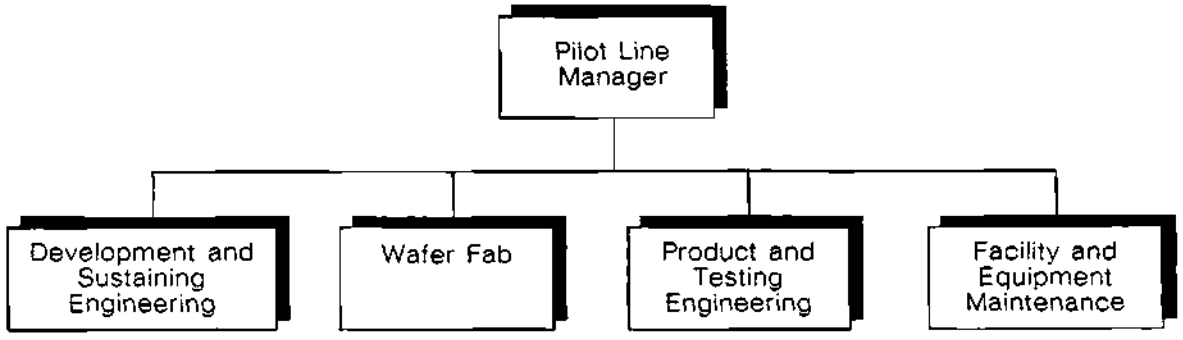
Figure 1

ORGANIZATION CHART



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The development and sustaining engineering group comprises the engineers who will develop and install the technologies, train the operators to run the various process steps, and be responsible for the quality of the material produced and the correct use and maintenance of all equipment. Each engineer will have responsibility for more than one process technology and must be very familiar with the equipment used and all the steps of the process. Because of the broad range of responsibilities of the job, he or she must be familiar with the physics of semiconductor devices and have experience in both semiconductor R&D and production environments.

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The wafer fab group comprises all the equipment operators. It is directed by one supervisor who is responsible for scheduling the movements of the material and for the line throughput. To enhance turnaround time, the operators (or model makers) must be able to perform several related steps. For example, a diffusion operator will run all the diffusion, LPCVD deposition, and ion implantation operations, together with wafer cleaning and resist stripping operations. An etching operator will be able to use any etching machine, perform all the inspections to check resist pattern quality before committing the wafer to etching, and check the agreement of the critical dimensions with the specifications. A masking operator will be able to prepare the wafers for exposure, run the photolithography equipment, and do all the post-processing operations and inspections. He or she must also know how to clean and inspect masks and reticles. Having all operators capable of doing all the processing steps is ideal for reducing turnaround time because it reduces and eliminates problems. However, it is impractical because of the long time required for training, and it is dangerous because of the lack of doublechecking. Nevertheless, one or two operators of this kind (senior model makers) are invaluable for processing batches of wafers that have priority over the other batches.

The size of the product engineering and testing group depends on how much the customer is going to test the circuits. Even if all testing at the wafer level and debugging of the circuits is done by the customer, the pilot line needs product engineers who use specifically designed test patterns to constantly monitor the stability of the device parameters and the defect level of the wafers. These product engineers can be much more effective if they are also responsible for at least limited device testing, and if they have good communications skills and a good understanding of both processing and circuit design.

Fast turnaround requires that most equipment perform properly most of the time. Responsive and professional maintenance of the facility infrastructures and processing equipment is key to this goal. Preventive maintenance should be done at specified times, even if the process engineers think that it is unnecessary. Whenever possible, maintenance contracts that cover preventive and emergency equipment care should be negotiated at the time of purchase. The availability of such contracts usually directly determines the reliability level of the equipment.

Staffing

Our estimate of the staffing required for a 500-wafer-per-period operation of this kind is shown in Table 1.

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Table 1

STAFFING REQUIREMENTS

Classification	Number Required	Estimated Wage Rate per Period*
Direct		
Wafer Fab Operators (model makers)	10	$2,000
Indirect		
Line Manager	1	$5,000
Wafer Fab Supervisor	2	$3,400
Allocated		
Development and Sustaining Engineers	5	$4,000
Product and Testing Engineers	3	$3,500
Facility and Equipment Maintenance Technicians	6	$2,500

*Period equals four weeks

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Number of Shifts

For most operations, the presence of process engineers is essential. Consequently, the number of shifts cannot exceed two--for example, a large shift from 7:00 a.m. to 3.30 p.m. and a reduced-staff shift from 2:00 p.m. to 10:30 p.m. This small second shift can complete time-consuming operations that take longer than eight hours, such as high-dose implants and long diffusions. It can also tolerate reduced engineering support.

The only exception is in the masking area. There, a full staff of experienced operators and a sustaining engineer should operate on two shifts because of the limited throughput of the wafer stepper equipment.

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Equipment Selection Criteria

For easy transfer of the technology to a production line, the pilot line equipment should be compatible with production-type equipment. The decision whether to use an R&D or a production version of the equipment requires a good knowledge of, and familiarity with, the process in question and a detailed study of all the factors that might affect the duplication of the operation. Such a decision should be made by the development engineer under the guidance of the line manager. Some money can be saved by not requiring many of the equipment options needed by inexperienced and untrained operators, but any automation that saves labor and enhances duplication and safety should be included. The level of automation has been chosen to be below that required on a high-volume manufacturing line. High levels of automation are only consistent with the manufacture of a single product or several products each of which is a minor variant of the other. To provide the flexibility needed for the prototype line and to reduce the capital investment required, automation has only been included where it is absolutely necessary for the achievement of the required results.

Maximum Output

To achieve the desired line width and the registration accuracy required to produce large, complex chips, it is necessary that the required photolithography be implemented with a 5X stepper. The output of the fabrication line has been set at 500 wafers per four-week period. Because of the time required to change reticles, the effective throughput of a typical 5X stepper is only 20 exposures per hour. With a 5 percent rework rate and a 10-mask photo process, this translates to an effective output of 1.90 wafers per hour. As mentioned before, because of limitations in the photo area, it is necessary to run the steppers in two shifts. This would give an effective utilization of 15 hours per day and a resulting output of 28.5 wafers per day. Since there are only 20 working days in the period, it is possible to get by with one stepper to achieve an output of 500 wafers. With one stepper and an output of 500 wafers per period, this would give an effective utilization of the stepper of 87.7 percent. This should allow sufficient time for maintenance.

Although additional space has been provided in the layout for some duplicate equipment, the equipment specified in the equipment list is the minimum required to achieve the output of 500 wafers per period.

Because of the high degree of control required for positional accuracy of the patterns and the control of critical dimensions, the 5X reticles must be generated with an e-beam pattern generator.

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FAB LAYOUT AND FACILITY REQUIREMENTS

Introduction

This section describes the main process flow used for producing two-layer metal CMOS circuits, lists the needed equipment, shows an example of equipment layout in the clean room area, and describes the facility requirements in terms of electric power, gases, and DI water.

Laying out the fab area for a pilot line is a very challenging task. It is a compromise between various and often contradictory needs. The requirements are to:

- Ensure a smooth flow of wafers through the steps of the main process used in the fab
- Allocate space and equipment for new technology developments in such a way that this activity will not interfere with standard production
- Simplify the layout of process piping, air and exhaust ducting, and power distribution for ease of maintenance and cost reduction during construction
- Facilitate equipment maintenance, so that it will not disturb adjacent equipment
- Ensure the highest achievable level of cleanliness, particularly in the masking and deposition areas
- Minimize wherever possible the contact between the wafer-fab personnel and the wafers

Process Flow

The silicon-gate CMOS process has stabilized over the years, and, in keeping with the trend toward smaller dimensions and the reduction/ elimination of latch-up sensitivity, the CMOS process employed in this fab uses an epitaxial substrate and a twin-well technology. With this process, it is possible to tailor the electrical characteristics of both the p- and n-channel transistors independently and without trade-off. Most of the major silicon suppliers now supply wafers with epitaxial layers as desired, and it is presumed that this pilot line will procure the wafers with the required epitaxial layer already grown. For these volumes, one can expect to pay $55 per raw wafer.

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In addition, the process employs a polycide gate to lower the sheet resistance of the gate. This allows for more interconnect flexibility in the CAD process and provides for efficient high-speed ROM structures to be implemented on-chip. Because of the large chip area and the high density of both metal 1 and metal 2, planarization of the surface is employed to minimize surface topography, thus improving yield and reliability.

The minimum number of masking steps for this process is 10. For gate lengths of 2 microns or greater, an additional field implant mask is employed to raise the n-channel field thresholds. However, for 1.25-micron circuits, the surface doping requirements necessary to minimize short channel effects are sufficient to provide the necessary field thresholds for 5-volt operation. A typical process flow is shown in Table 2.

The mechanical yield is shown in Table 3. Typical survival yields for this type of pilot line are given, and, because of the complexity of the planarization process and the parametric yield, both of these quantities have been factored into the mechanical yield.

Equipment List and Utilization

The equipment necessary for performing all the process steps is given in the appendix at the end of this section, with prices, delivery times, and manufacturers listed. We have also added a list of equipment for a testing area that is not part of the clean room area.

For a more accurate prediction of equipment utilization, one has to know the wafer mechanical yield at every step. Since the throughput limits occur in the masking area, we have assumed that the sorting of good and bad wafers occurs at incoming inspection in the masking area, not at each processing step. The assumed wafer mechanical yield is shown in Table 3. Equipment utilization (in terms of hours of use for a final production of 500 wafers per period) as a percentage of the total time the equipment is available to the operators is given in Table 4, along with the time spent by the operator using the equipment. These numbers are used for predicting the number of operators needed in the processing area and their assignments in the three areas of specialization--diffusion (including ion implantation and thin-film deposition), etching, and masking.

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Table 2

TWO-LAYER METAL CMOS PROCESS FLOW OUTLINE

Process Step
Initial Oxidation
Masking Nitride Deposition
P-Well Mask--Defines areas where n-channel transistors are built
Boron (P) Implant
P-Well Drive-In/Oxidation
Etch Oxynitride
Strip Nitride
Phosphorus Implant--Self-aligned n-well I^2
N-Well Drive-In
Strip Oxide
Reoxidation
Masking Nitride Deposition
Active Area Mask--Defines all active device areas
Field Oxidation
Gate Oxidation
BF_2 Implant--Adjusts p- and n-channel thresholds
Doped Poly Deposition
Silicide Sputter
Silicide Alloy (Rapid Thermal Anneal)
Gate Mask/Polycide Etch--Defines gate electrodes
Reoxidation
N^+ Mask/Deep UV Cure (DUV)
Arsenic Implant--Establishes source/drain regions of n-channel
P^+ Mask/DUV
Boron Implant--Establishes source/drain regions of p-channel
Rapid Thermal Anneal--Activates implants
BPSG Deposition--To achieve maximum reflow at minimum temperature
Rapid Thermal Anneal Reflow
Contact Mask
Platinum Deposition

(Continued)

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Table 2 (Continued)

TWO-LAYER METAL CMOS PROCESS FLOW OUTLINE

Process Step

Pt/Si Sinter (Rapid Thermal Anneal)--Pt/Si to form silicide in source/ drain contacts
Excess Platinum Strip
Barrier Metal + Aluminum-Silicon Deposition (First Metal)
First Metal Mask
Plasma CVD Oxide Planarization--Oxide etch with oxide/resist selectivity ratio = 1

Redeposit Plasma CVD Oxide
Via Mask--Establishes the areas of contact between the two layers of metal
Second Metal Deposition
Second Metal Mask
Alloy
Dielectric Deposition--For scratch protection
Pad Mask

Table 3

WAFER MECHANICAL YIELD

Step	Yield	Cumulative Yield	Number of Wafer Starts
			707
P-Well Mask	98.0%	98.0%	693
Active Area Mask	98.0%	96.0%	679
Gate Mask	96.0%	92.2%	652
N^+ Mask	99.0%	91.3%	645
P^+ Mask	99.0%	90.4%	639
Contact Mask	96.0%	86.8%	613
First Metal Mask	96.0%	83.3%	589
Planarization	95.0%	79.1%	559
Via	98.0%	77.5%	548
Second Metal Mask	96.0%	74.4%	526
Pad Mask	99.0%	73.7%	521
Parametric Yield	96.0%	70.7%	500

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Table 4

EQUIPMENT UTILIZATION AND OPERATOR TIME PER EQUIPMENT AREA
(500 Wafers Out per Four-Week Period)

Equipment	Use (Hours)	Number of Shifts	Utilization	Operator Time per Period (Hours)
Diffusion Area				
Wet Processing				
#1	36.87	2	13.2%	12.93
#2	73.18	1	52.3%	28.33
#3	26.30	1	18.8%	9.02
#4	78.48	2	28.3%	31.62
Furnace				
#1	144.13	2	51.5%	17.65
#2	98.29	2	35.1%	3.88
#3	44.84	1	32.0%	5.90
#4	21.25	1	15.2%	14.87
#5	25.20	1	18.0%	8.82
#6	12.28	1	8.8%	3.07
#7	12.62	1	9.0%	3.53
LPCVD				
Poly	8.97	1	6.4%	3.73
Nitride	20.70	1	15.8%	8.64
Oxide/BPSG	33.47	1	23.9%	8.37
Plasma Oxide	21.10	1	24.0%	5.30
Metal Deposit	40.70	1	29.1%	24.40
Implanter	178.30	2	63.7%	30.80
RTA	35.85	1	24.0%	7.17
Total Diffusion Operator Time				228.03
Etching Area				
Nitride Etcher	44.22	1	31.6%	29.46
Poly Etcher	41.18	1	29.4%	38.95
Oxide Etcher	130.00	2	46.4%	130.00
Metal Etcher	59.09	1	42.2%	59.09
Asher	55.42	1	39.6%	19.95
Total Etching Operator Time				277.45

(Continued)

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Table 4 (Continued)

EQUIPMENT UTILIZATION AND OPERATOR TIME PER EQUIPMENT AREA
(500 Wafers Out per Four-Week Period)

Equipment	Use (Hours)	Number of Shifts	Utilization	Operator Time per Period (Hours)
Masking Area				
Wafer Stepper	263.10	2	87.7%	263.10
Photoresist Equipment	464.50	2	25.0%	371.80
Total Masking Operator Time				634.90
Total Operator Time				1,140.38

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Clean Room Layout

A typical layout for the equipment in the wafer fab area is shown in Figure 2. We can identify three distinct areas:

- A photolithography area, with the process line for the wafer stepper; as shown, the process lines can easily accommodate four steppers; the photolithography area is isolated from the rest of the clean room and uses a dedicated air conditioning system
- An etching and metal deposition area, which requires a high degree of cleanliness but a less stringent climate control than the masking area
- A diffusion, thin-film deposition, and ion implantation area

Service aisles are provided behind lithography and etching process lines for locating all the "dirty" equipment (pumps, power generators, canisters containing liquids, and specialty-gas cylinders), the gas and liquid pipes, and the electrical wiring. This approach allows most of the maintenance work to be done outside the clean areas; the resulting reduction of traffic makes it easier to keep the clean areas particle free.

The overall wafer fab area comprises 5,400 square feet. The service aisle area measures about 1,300 square feet, leaving a net effective clean area of 4,100 square feet.

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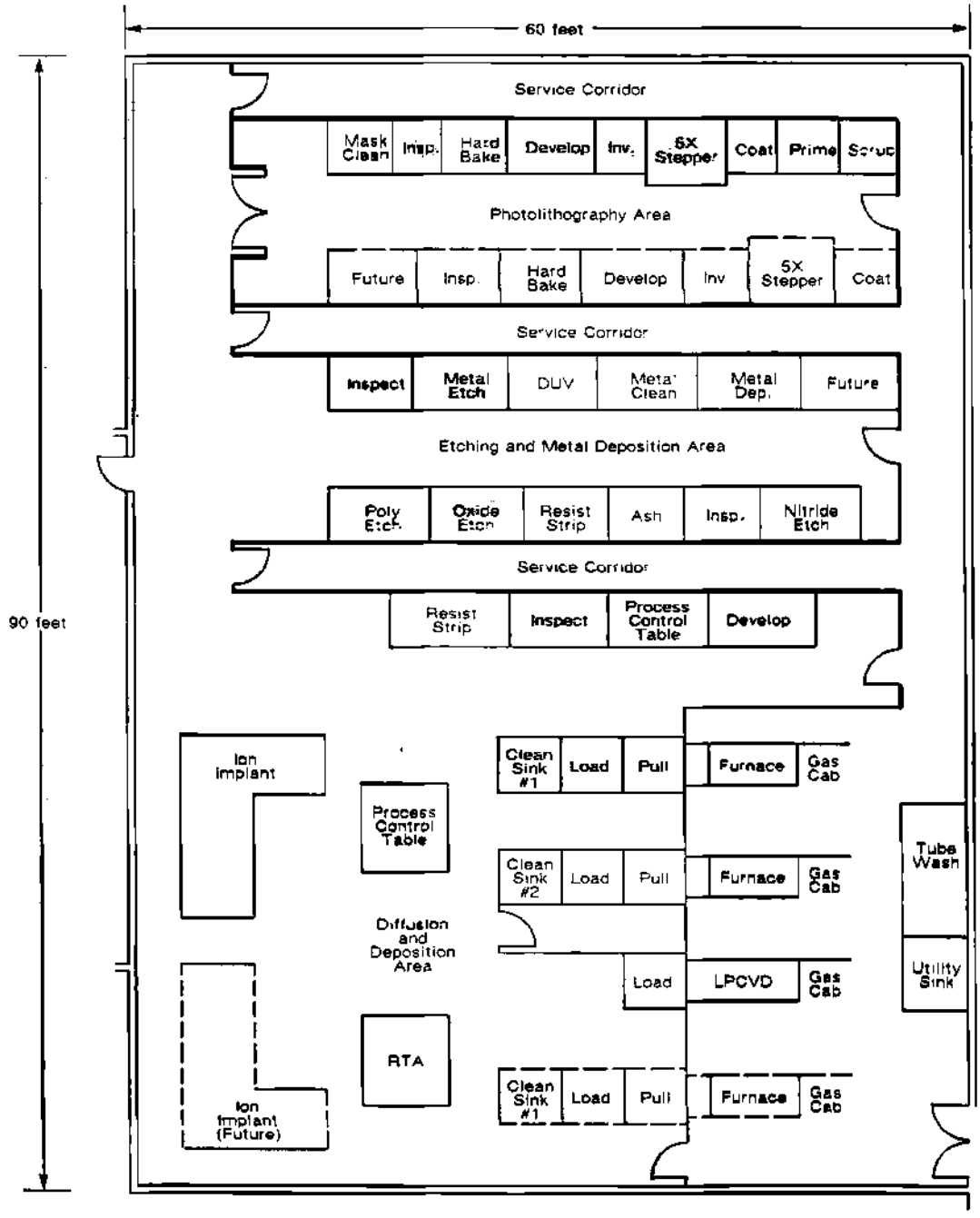
Prototype CMOS Model

Figure 2

LAYOUT FOR CMOS WAFER FAB AREA



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Prototype CMOS Model

Facility Requirements

The major systems and requirements for the wafer fab area are listed in Table 5. A range of costs for material and installation is given, reflecting differences in the requirements and materials used.

Table 5

FACILITIES IMPROVEMENTS FOR WAFER FABRICATION AREA
(Thousands of Dollars)

System	Requirements	Cost Range	Average
Fab Construction	5,400 ft^2	$520-$ 750	$ 650
DI Water System	10-20 gallons per minute of makeup	125- 200	180
Air Conditioning (With Cooling System and Tower)	100-125 tons	180- 250	200
Chemical Storage		20- 25	22
Electrical		150- 200	175
Total		$995-$1,425	$1,227

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Prototype CMOS Model

WAFER COST ANALYSIS

Assumptions

The assumptions described in the previous sections are:

- Technology
  - Two-layer metal CMOS
  - All masking layers done on the stepper
  - Epitaxial substrate
  - Dry etching
  - 100mm-diameter silicon wafers
- Production
  - One fully staffed shift in diffusion and etching areas
  - Small second shift in diffusion area
  - Two fully staffed shifts in the masking area
  - 500 finished wafers out per four-week period
- Cumulative fab yield of 70.7 percent

Fixed Costs

Tooling

The costs of reticles and masks used for wafer production are not included in the wafer cost analysis. These costs are very high, ranging from $2,000 to $10,000 for reticles and masks. These costs are normally included in circuit design costs. The cost depends on whether the designs are for custom or semicustom reticles or masks.

Facilities

We assume that the building is rented as a shell at $1.20 per square foot per period. The total space rented comprises 12,000 square feet (5,400 square feet for wafer fab and 6,600 square feet for office, test, and service areas). Facility design is contracted to an outside engineering firm and all facilities and services are supplied from scratch.

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Prototype CMOS Model

Table 5 shows that the average cost of construction of the prototype fab and the fab support systems is $1,227,000. In addition, the construction cost for the 6,600 square feet of office, test, and service areas is estimated at $40 per square foot, for a total cost of $264,000. Thus, total cost of improvements to the rented building is $1,227,000 plus $264,000, or $1,491,000. Note that the fab construction cost in this model is depreciated over a 10-year period in contrast to the more rapid 5-year depreciation typical of high-volume production fabs.

Equipment

As listed in the appendix to this section, equipment costs are as follows (in thousands of dollars):

Diffusion area equipment	$1,546.8	31.3%
Deposition/implantation equipment	1,244.3	25.2%
Etching equipment	772.8	15.6%
Photomasking equipment	1,092.5	22.1%
In-process test equipment	289.0	5.8%
Total cost for fabrication equipment	$4,945.4	100.0%

Variable Costs

Table 6 shows the personnel requirements, wage rates, and labor costs for direct, indirect, and allocated personnel. Total labor costs for the four-week period are $96,650. For 500 wafers out per period this corresponds to labor costs of $193.30 per wafer.

Table 7 shows the complete wafer costs analysis. The total cost of the wafer is $537.67.

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Prototype CMOS Model

Table 6

LABOR COSTS

Personnel	Number	Wage Rate per Period	Personnel Cost per Period	25 Percent Fringe Benefit	Total Personnel Cost
Direct					
Wafer Fab Operators	10	$2,000	$20,000	$5,000	$25,000
Indirect					
Line Manager	1	$5,000	$ 5,000		
Wafer Fab Supervisor	2	$3,400	6,800		
Total Indirect			$11,800	$2,950	$14,750
Allocated					
Development and Sustaining Engineers	5	$4,000	$20,000		
Product and Testing Engineers	3	$3,500	10,500		
Facility and Equipment Maintenance Technicians	6	$2,500	15,000		
Total Allocated			$45,500	$11,400	$56,900
Total Labor Cost					$96,650

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Prototype CMOS Model

Table 7

WAFER COST ANALYSIS
(500 Wafers Out per Four-Week Period)

Fixed Costs per Calendar Month		
Rent (12,000 square feet at $1.20 per square foot)	$ 14,400	
Sewage and Water Maintenance	2,000	
Electrical Power	22,000	
Gas	900	
Depreciation		
Fab construction (120 months); $1,227,000	10,125	
All other construction, including office, test area, and fab support systems (120 months); $264,000	2,200	
Fab equipment, excluding test equipment (60 months); $4,945,400	82,423	
Total per Calendar Month	$134,048	
Total per Four-Week Period	$123,737	
Total Fixed Cost per Wafer	$247.47	46.0%
Variable Cost per Wafer		
Direct Materials		
Wafer (yielded cost)	$ 77.80	
Chemicals	8.50	
Miscellaneous Materials	2.90	
Gases	5.20	
DI Water	2.50	
Subtotal	$ 96.90	
Labor		
Direct	$ 50.00	
Indirect	29.50	
Allocated	113.80	
Subtotal	$193.30	
Total Variable Cost per Wafer	$290.20	54.0%
Total Cost per Wafer	$537.67	100.0%

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INCREASING PRODUCTIVITY

Introduction

The productivity of our pilot line in terms of wafers per operator and per square foot of fab area is quite small compared with the results achieved, for instance, in NMOS DRAM production lines. There are several reasons for this:

- We want reasonably fast turnaround time and so, for this reason, the equipment utilization is low and the batch size small.
- Our CMOS process is more complicated than that of a conventional NMOS process.
- We have limited the investment in very expensive equipment (e.g., steppers) and created throughput bottlenecks.

A look at Table 4 shows that much expensive equipment (occupying costly floor space) is greatly underutilized. Productivity can be raised by duplicating the equipment that has a high degree of utilization. This has the additional benefit of avoiding a complete paralysis of the line in case a heavily utilized piece of equipment is not operational.

In this section, we modify our plan to increase wafer output from 500 wafers per period to 1,000 wafers per period. Substantial cost savings result.

Duplication of Equipment

The line throughput can be doubled by adding one wafer stepper, used on two shifts. Utilization of the wafer steppers remains at 85 percent, which is very high, but assumes a wafer throughput of only 15 wafers per hour. Expected improvements in existing equipment (automatic alignment and automatic reticle exchange) and the introduction of completely new models is expected to increase the equipment throughput by at least a factor of two, thus reducing the equipment utilization to levels more acceptable for a fast turnaround time.

Wafer Cost Analysis for Increased Line Throughput

For increased throughput, these cost figures are going to change:

- Fab equipment depreciation
- Labor

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No other costs will change significantly. To double the output, another implanter, a 5X stepper, and resist coat/develop equipment are needed. This requires an additional capital investment of $1,520,000, which adds $23,385 to the depreciation per period. The direct labor costs will decrease from $50 per wafer to $37.50 (15 operators).

Table 8 compares the total wafer cost for 1,000 wafers per period with the cost for 500 wafers.

Table 8

COST PER WAFER FOR DIFFERENT THROUGHPUTS

	500 Wafers per Period		1,000 Wafers per Period	
	Cost	Percent	Cost	Percent
Fixed Cost	$247.47	46.0%	$149.12	42.0%
Direct Materials	96.90	18.0	96.90	27.3
Fab Labor				
Direct	50.00		37.50	
Indirect	29.50		14.75	
Allocated	113.80		56.90	
Total Labor	$193.30	36.0	$109.15	30.7
Total Cost per Wafer	$537.67	100.0%	$355.17	100.0%

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APPENDIX

EQUIPMENT LIST FOR CMOS WAFER FAB AREA

Item	Unit Cost ($K)	Number Required	Total Cost ($K)	Delivery (Weeks)	Manufacturers
Diffusion Area Equipment					
Furnaces (4 tubes/stack, w/digital control and cantilever loaders)	$45.0	8 tubes	$ 360.0	26	Tylan, Thermco, BTU
LPCVD System (auto)	$80.0	3 tubes	240.0	26	ACS, ASM, Tylan
Plasma Oxide System		1 tube	300.0	26	PWS, ACS, Tylan
Chemical Sink (6 feet with rinser/ dryer)	$22.0	2	44.0	12-20	IAS, Santa Clara Plastics
Rapid Thermal Annealer		1	150.0	30	AG, Varian, Eaton
Process Monitoring Equipment					
Step Height Meas. System	$12.0	1	12.0	6-12	Sloan, Tencor, Siltec
4-Point Probe	$ 3.5	3	10.5	4-8	Signatone, Veeco
UV Lamp	$ 1.0	3	3.0	4	
CV Plotter	$11.0	1	11.0	6	MDC
Probe Station	$18.0	1	18.0	6-12	Micromanipulator, R&K, Signatone
Thin-Film Meas. Equipment	$30.0	1	30.0	16-20	Nanometrics
Curve Tracer	$10.0	1	10.0	12-16	Tektronix
Angle LAP Equipment	$ 4.5	1	4.5	6-8	Philtek
Microscope	$ 5.0	1	5.0	4-8	Lietz, Nikon, Olympus
Interferometer	$ 4.0	1	4.0	4-8	Lietz
Camera	$ 1.0	1	1.0	4-8	Polaroid
Maintenance Equipment					
Tube Washer	$12.0	1	12.0	8-10	IAS, Santa Clara Plastics
Utility Sink (8 feet)	$10.0	1	10.0	12-20	
Miscellaneous Equipment (gas system, gas cabinets, acid storage, quartzware, TC and temp. meas. systems, tables, chairs)			120.0		
Subtotal			$1,345.0		
Shipping and Taxes (15%)			201.8		
Total for Diffusion Area Equipment			$1,546.8		

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APPENDIX (Continued)

EQUIPMENT LIST FOR CMOS WAFER FAB AREA

Item	Unit Cost ($K)	Number Required	Total Cost ($K)	Delivery (Weeks)	Manufacturers
Deposition and Implant Equipment					
Ion Implanter (medium current, 200kV)	$500.0	1	$ 500.0	20-30	Eaton, Varian
Metal Sputtering System w/Multiple Sources	$520.0	1	520.0	20-30	Varian, MRC
Chemical Sink (6 feet with rinser/ dryer)	$ 22.0	1	22.0	12-20	IAS, Santa Clara Plastics
Wafer Scrubber	$ 20.0	1	20.0	8-12	MTI, Ultratech, Solitec
Leak Detector	$ 8.0	1	8.0	8-12	Veeco, Varian
Miscellaneous Equipment (Dewar flasks, gas systems, tables, chairs)			12.0		
Subtotal			$1,082.0		
Shipping and Taxes (15%)			162.3		
Total for Deposition and Implant Equipment			$1,244.3		

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APPENDIX (Continued)

EQUIPMENT LIST FOR CMOS WAFER FAB AREA

Item	Unit Cost ($K)	Number Required	Total Cost ($K)	Delivery (Weeks)	Manufacturers
Etching Equipment					
Nitride Etcher (planar)	$120.0	1	$120.0	20-25	Drytek, Tegal
Polysilicon Etcher (planar)	$120.0	1	120.0	18-26	PlasmaTherm, Tegal, LAM Drytek
Oxide Etcher (planar)	$150.0	1	150.0	18-26	Tegal, PlasmaTherm, LAM Drytek
DUV Resist Stabilizer	$ 25.0	1	25.0	15-20	Fusion, OAI, HTG
Metal Etcher (planar)	$150.0	1	150.0	20-26	Tegal
Asher (barrel)	$ 20.0	1	20.0	12-16	Branson IPC, Tegal
Resist Strip Sink	$ 22.0	1	22.0	12-20	IAS, Santa Clara Plastics
Chemical Sink (6 feet with rinser/ dryer)	$ 22.0	1	22.0	12-20	IAS, Santa Clara Plastics
Microscope	$ 4.0	2	8.0	4-8	Leitz, Olympus
Miscellaneous Equipment (gas systems, gas cabinets, wafer storage cabinets, tables, chairs)			35.0		
Subtotal			$672.0		
Shipping and Taxes (15%)			100.8		
Total for Etching Equipment			$772.8		

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APPENDIX (Continued)

EQUIPMENT LIST FOR CMOS WAFER FAB AREA

Item	Unit Cost ($K)	Number Required	Total Cost ($K)	Delivery (Weeks)	Manufacturers
Masking Equipment					
Wafer Stepper (5X)	$750.0	1	$ 750.0	25-35	Nikon, ASM, Canon
Wafer Scrubber	$ 20.0	1	20.0	8-10	Solitec, Eaton
Single-Track Resist Spinner	$ 45.0	1	45.0	20-25	Solitec, MTI
HMDS Vacuum Oven	$ 20.0	1	20.0	15	YES, IMTEK
Resist Develop Station	$ 35.0	1	35.0	15-20	IAS, Santa Clara Plastics
Hard-Bake Oven	$ 5.0	2	10.0	10	Lab-line Instr., Blue-M, Thelco
Mask Cleaner	$ 8.0	1	8.0	16	Ultratech, MTI
Line-Width Meas. System	$ 40.0	1	40.0	26	Nanometrics, ITP
High-Quality Microscope and Camera	$ 16.0	1	16.0	6-8	Leitz, Zeiss, Reichert
Inspection Microscope	$ 4.0	3	12.0	6-8	Leitz, Nikon, Olympus
Wafer Flatness Tester	$ 20.0	1	20.0	3	Tropel
Particle Counter	$ 7.0	1	7.0		Royco
Temp./Humidity Monitor	$ 1.0	1	1.0		
Miscellaneous Equipment (solvent, acid storage cabinets, mask, wafer storage cabinets, specialty sink)			15.0		
Subtotal			$ 950.0		
Shipping and Taxes (15%)			142.5		
Total for Masking Equipment			$1,092.5		

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APPENDIX (Continued)

EQUIPMENT LIST FOR CMOS WAFER FAB AREA

Item	Unit Cost ($K)	Number Required	Total Cost ($K)	Delivery (Weeks)	Manufacturers
In-Process Test Equipment					
Automatic Prober	$ 27	1	$ 27.0		Pacific Western, Electroglass
Parametric Tester	$ 85	1	85.0		Keithley, HP, PWS
Curve Tracer	$ 5	1	5.0		Tektronix
Oscilloscope	$ 5	1	5.0		Tektronix
Digital Voltmeter	$ 1	2	2.0		Fluke, HP
Frequency Counter	$ 2	1	2.0		HP
Signal Generator	$ 2	2	4.0		HP
SEM (4-inch stage)	$120	1	120.0		Cambridge, Hitachi
Manual Prober	$ 11	1	11.0		Rucker & Kolls
Miscellaneous Equipment (power supplies, ammeters, L-C meter, tables, chairs)			10.0		
Subtotal			$271.0		
Tax (6.5%)			18.0		
Total for In-Process Test Equipment			$289.0		

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The Emerging Fab

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The Emerging Fab

INTRODUCTION

The semiconductor industry is characterized by rapid and constant innovations and improvements. These changes scan a broad spectrum from new products and markets to new design techniques, new process technologies, more productive manufacturing equipment, and more efficient manufacturing. As a result, semiconductor devices have become pervasive, the marketplace has expanded, and the price and cost for a given function have continued their vigorous decline.

This service section describes an ultramodern production facility that utilizes the latest process technology, process equipment, and clean room technology. The output of this fab is 14,000, 150mm wafers per four-week period. An eleven mask, 1.5μm CMOS process is used. The fab output and costs are assumed for only one large-volume product, such as an SRAM, to be in production. The costs, yields, and efficiency of operation are typical of those attainable at present. Wafer probe, test, assembly, and marketing of the packaged devices are not included in this model, as this hypothetical factory is dedicated to high-volume wafer fab operation.

PROCESS TECHNOLOGY

CMOS technology has emerged as a versatile and pervasive technology for the next decade. Although CMOS is quite an old technology, CMOS has reached a major new significance when examined in the context of the present technical capability, market needs, and manufacturing viability of the semiconductor industry. The reasons for its new prominence are as follows:

- Semiconductor components for equipment that can be used in offices and homes and are transportable have created enormous new markets. Power dissipation of components has become a design specification.

- Bipolar and NMOS VLSI components have reached such a high degree of integration that they are limited in their degree of integration or speed by the amount of thermal dissipation permitted in conventional semiconductor packages. CMOS technology does not have these limitations and thus can offer both a higher performance and a higher degree of integration than either bipolar or NMOS technology, while still permitting the use of industry-standard packages.

- With the smaller sizes and improved methods of minimizing latch-up, the area penalty of CMOS versus NMOS has disappeared below 2μm dimensions.

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- CMOS requires a complex process, with 10 to 13 masks versus 7 to 8 masks in earlier NMOS. But the modern NMOS process has become more complex too, as integration and performance needs have resulted in adding extra processing steps to NMOS.

- Modern processing equipment, with its emphasis on automation and cassette-to-cassette transfer, has eliminated much individual wafer handling; thus, the penalty associated with a longer and more complex process has been reduced. It is possible to expect and get 90 percent mechanical fab yield for complex CMOS processes by using modern automated production facilities.

- CMOS circuits have higher noise margins. This attribute significantly impacts the design costs, which is a major consideration for VLSI devices. Not only are the design costs reduced, but the probe yields for high-complexity devices performing to specifications are higher in CMOS than in NMOS.

The combination of these parameters has brought CMOS technology to the center stage. Most new designs are being committed to CMOS technology. There is, however, no single CMOS process, and a large number of variations of CMOS process are being practiced. These variations include:

- N-well CMOS
- P-well CMOS
- N-well with epitaxy
- P-well with epitaxy
- Twin well with epitaxy

Interconnect technologies also have several possibilities, including:

- Single poly, or polycide and single metal
- Single poly, or polycide and double metal
- Double poly/polycide and single metal
- Double poly/polycide and double metal

Of these possibilities, the CMOS process described in this report has the following features:

- Twin well with epitaxy
- One poly, one polycide, and one level of metal

The process flow, which is described later in this section is a representative process flow applicable to a variety of applications. A fairly accurate cost model can be formulated to draw conclusions about this and other variations of the CMOS process.

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The Emerging Fab

The major trend in the industry is toward smaller feature sizes. Most new designs are at 2μ m geometries. Present manufacturing equipment, however, will support 1.5μ m. In view of this, the major design rules assumed for the purpose of this discussion, are as follows:

- Gate oxide 25nm
- Junction depth 0.25μ m
- Channel length (drawn) 1.5μ m
- Diffusion pitch 5μ m
- Poly/polycide pitch 3.5μ m
- Metal pitch 5μ m

WAFER SIZE

The facility described in this discussion uses 150mm silicon wafers with epitaxial film grown by the silicon vendor. With the advent of small-geometry CMOS, the market for wafers with epitaxy will grow. All major silicon vendors have plans to enter the epitaxial wafer market; thus epitaxial wafer prices are expected to drop significantly in the next few years.

The 150mm wafers will be the preferred wafer size for the next five years, and production plants now under construction will utilize these wafers. Equipment to process 150mm wafers is now available with superior wafer-handling mechanisms, high reliability, and process automation.

MANUFACTURING FACILITY/CLEAN ROOM

With the dawn of the VLSI era, stringent requirements for the control of submicron particle contamination, temperature, and humidity have been placed on the design of manufacturing facilities, manufacturing personnel, processing equipment, and manufacturing material. To profitably manufacture sub-2-micron VLSI devices, the manufacturer needs a world-class, paperless facility with filtration down to 0.1-micron particle size in the process area; a minimum number of suitably attired and trained personnel; processing equipment that does not contaminate personnel or silicon wafers; and multiple-filtered DI water, chemicals, photoresist, and process gases.

Since clean room floor space is at a premium, the question of maintaining 100 percent HEPA ceiling and Class 10 environment versus local Class 10 zones is debatable. In our opinion, until the Standard

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Mechanical InterFace (SMIF) concept is fully developed and proven to provide a true human isolation of wafers in a sealed and controlled ambient during entire wafer processing, the best alternate is a paperless, Class 10, 100 percent HEPA ceiling with automated equipment and a low density of process personnel that is well-trained in clean room practices. Because of the high cost of Class 10 clean room space and the cost pressures on IC products, we believe that within the next two to three years, SMIF technology will be employed in a facility of this type. For dimensions in the 1-micron range and below, it is essential that the process personnel and the wafers be totally isolated.

With modern, automated, cassette-to-cassette processing equipment, clean room occupancy is substantially reduced. Most of the equipment is installed through the wall, and the clean room area requirement for this equipment is significantly decreased. Furthermore, because of these advancements, the total heat load and air-handling requirements inside the clean room are substantially reduced and are most conveniently handled by individual clean room bays/tunnels. Each bay has its own temperature and humidity controls.

The clean room ceiling is 100 percent covered with HEPA filters operating at an air velocity of 90 feet per minute. HEPA filter efficiency is 99.999 percent down to 0.1μm particle size to minimize the particle density to less than 10 particles per cubic foot. Sidewall return air ducts are used to provide vertical laminar flow with an exit velocity not exceeding 700 feet per minute. Air ionization grids are installed throughout the process area and clean room entrances to achieve the high efficiency of air filtration and to reduce the electrostatic adhesion of particles to wafers, cassettes, and cassette boxes. Recovery time after disturbance is 6 seconds in workstation areas and 10 seconds in the aisle area. Laminar flow is adjusted and controlled aerodynamically at each piece of process equipment to provide maximum laminar isolation and cleanliness between wafer and worker.

The temperature control is 68 $\pm$ 0.5^{o}F in the photoresist area and 68 $\pm$ 1^{o}F in other areas. The control of humidity is expecially critical in the photoresist area from the application of the adhesion promoter (HMDS) up to and including the developing of the printed image. The relative humidity should be kept at 40 $\pm$ 2 percent in this critical area. For the rest of the wafer fab area, the humidity can be at 40 $\pm$ 5 percent. The vibration specification in the photo area is less than 10 microns floor displacement over a frequency range of up to 40Hz.

With the increase in microprocessor-controlled equipment in the wafer fab area, care must be taken to avoid the introduction of electrical noise into the control circuitry. Most equipment manufacturers now

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provide equipment with a separate mains supply for the low-current and high-current portions of the equipment. It is highly advisable to supply the low-current control circuitry with isolated ground, regulated AC power. This will remove transients and protect the equipment from brownout conditions.

MATERIAL QUALITY AND HANDLING

All the gases, chemicals, and related materials are piped through high-purity stainless steel or teflon piping with welded joints. Multiple filters with 0.1-micron point-of-use filters, in-line moisture analyzers, and gas chromatographs are used to ensure purity and low particulates in the gas, chemicals, and water supply. Toxic gas monitors, dampers to rapidly clear the air of smoke or toxic fumes, sprinklers, and emergency doors are installed throughout the facility. Double-walled containers, chemical neutralization, and exhaust scrubbers are installed to maintain a zero- effluent facility.

The advent of dry etching has reduced both the DI water consumption and the usage of wet chemicals within the fab area. However, these chemicals have been replaced by gases. The exhaust gases from the etch equipment must be adequately scrubbed to reduce toxic effluents. This shifts the burden from chemical neutralization to scrubbing. It is essential for the protection of both the personnel and equipment that the exhaust fans used to carry away the toxic fumes be supplied with power that is backed up with an emergency generator. This will allow the continuous exhausting of toxic fumes during an interruption of mains power.

PERSONNEL PRACTICES

The clean room is restricted to the absolute minimum number of personnel and, as much as possible, clean room needs are serviced from the outside. Chemicals are transferred through the chase walls, and clean room conditions, including gases and liquids, are automatically monitored. With through-the-wall equipment installation, the majority of equipment services and maintenance is provided in the chase area.

Procedures are developed to provide maximum isolation between personnel and the wafers. In areas where personnel and wafers must come in close contact, aerodynamics is engineered in a manner to direct the flow of particles away from the wafers and toward the personnel. Ultra-low-particulate, full-coverage clean room gowns are used. Movements within the clean room are minimized, and the number of personnel in each work area is controlled. Training in clean room practices is continuously provided and regularly monitored.

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PROCESS AND PROCESS EQUIPMENT CLEANLINESS

Process equipment can be a source of particulate contamination. In addition to normal process control, contamination deposited on a clean wafer, when cycled through the total equipment process, needs to be continuously monitored and the process equipment must be cleaned if the particulate specifications are not met. All portions of the equipment, where particle generation is likely, need to be thoroughly vented.

The entire manufacturing process is tracked using an on-line manufacturing tracking system without any paper run-sheets or process instructions. To enhance the instant visibility and to identify the next process step, plastic placards are used. Video terminals are installed throughout the fab area to provide process instructions and other information. All the printers associated with the equipment are placed in the chase area. All the process control equipment (thickness monitors, resistivity monitors, and CV and CD measurement equipment) are directly linked with the host computer to gather in-process data.

PRODUCT EXPOSURE TIMES

Despite all the steps that have been taken to reduce and eliminate the particulates from the process, the longer the wafers are exposed in the process area, the more contaminants they accumulate. Thus the probe yields are reduced. This fact has driven the need for reduced cycle times and quick turnaround times for normal production.

In order to achieve this, process equipment uptime is vigorously managed. Computerized material and work in process (WIP) management, computer-aided processing, process feedback and control, and around-the-clock manufacturing seven days a week are all necessary to achieve production goals.

OPERATIONAL STRATEGY--RESOURCE SELECTION

People and Their Skill Levels

This operation is distinguished from the conventional resource selection in various aspects. Equipment processing is significantly more sophisticated and automated; therefore, the asset utilization factor and

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hence the equipment uptime requirement is high, and the degree of cleanliness required is significantly higher. The criteria for the manpower resource are:

- High skill level
  - Preferably a four-year college degree (not necessarily an E.E. degree) or a two-year junior college program in IC technology
  - Expertise in equipment operation and first order maintenance
  - Expertise in process and quality control
  - Expertise in unsupervised material flow with the aid of a computerized system
- Small in number

Fab technologists who qualify for this facility will have a minimum of six months of exhaustive training in the above areas through:

- The equipment vendor's training/demonstration centers
- Organized classroom/on-the-job process training
- Operational efficiency training

This will be followed by a formal certification of the technologists through the written certification test, as well as through periodic on-the-job audits.

MANUFACTURING EQUIPMENT

During the last five years there have been major changes made in the way that wafer fabrication areas are both built and equipped. These changes, while they have dramatically increased the minimum cost to enter the business, have also had an equally dramatic effect on circuit density and the reduction of defect density. As a result, a substantially reduced cost per function has been attained.

Equipment plays the central role in this revolution. It has become the technology. If the equipment to implement a new process in a cost-effective manner does not exist, that process will not be used. The new equipment has several common characteristics, which have become a must. The key to success is selection of the right equipment, even when both the definition and the choice changes frequently.

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With the modern equipment, the clean room area requirement has been dramatically reduced. Changes include smaller footprint and through-the-wall installation, wafer handling done cassette-to-cassette or by robots, and microprocessor-controlled process execution. Process control and recipe downloading have become standard. Specifications on uptime, meantime to failure, meantime to repair, process control, reproducibility, contamination control, and safety have improved manifolds. The integration of many process steps has also become viable, thus reducing the inventory points, cycle time, and manpower requirements while improving throughput and yields. With the advent of on-line inventory management, process tracking, and recipe downloading, a truly paperless wafer fab is now possible.

The major process steps and the corresponding equipment selection are briefly described in the following discussion.

Photolithography

The photolithography area has undergone one of the most dramatic changes. Today's alignment machines step the image of a defect-free reticle enclosed in a pellicle, over a wafer. Each step is automatically aligned, thus ensuring alignment and registration accuracies that were impossible heretofore. In the most advanced versions, it is possible to couple photoresist coat, bake, align, expose, develop, and inspection processes in a single integrated system, with the only human intervention at cassette loading, unloading, and the optical inspection station. Since controlling elapsed time between coat, bake, expose, and develop is critical, dimension control has greatly improved.

For the purposes of the production facility described here, both 5X and 1X steppers can be used. However, our model uses 1X steppers integrated with photoresist coater and developer, together with an automatic inspection station. Single-layer positive photoresist is used throughout the process. Two steppers continuously feed the exposed and developed wafers to the automatic inspection station, where a technologist inspects them for defects and dimensional control.

Etching

All etching steps are performed using cassette-to-cassette, single-wafer-at-a-time, plasma or RIE/plasma equipment. Poly, polycide, oxide, and metal etches are accomplished using RIE/plasma machines, and a controlled slope is achieved at all of these steps. Nitride etch is similarly etched although the requirement for a controlled slope is not necessary or desirable.

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Photoresist removal is done by plasma ashing. Prior to furnace operations such as oxidations, anneals, and LPCVD operations, a wet cleaning operation is done in an automatic, cassette-to-cassette wet station. Noncritical etches, such as oxide strips, are also done in these automated wet stations.

Diffusion Operation

Horizontal diffusion furnaces are used for oxidation, diffusion, anneals, alloy and LPCVD doped/undoped LTO, doped/undoped polysilicon, and masking nitride. Polycide is formed by sputter deposition of silicide (tungsten or titanium silicide) on doped polysilicon. All the furnaces are integrated with automatic, cassette-to-cassette prediffusion-clean wet stations and wafer transfer mechanisms, which transfer wafers from teflon boats to the quartz boats used in the diffusion furnaces. Noncontact cantilevers and elevators minimize the particulate generation. The furnace process recipe is downloaded from a secured computer to minimize operator errors and to maintain full tracking of wafer processing conditions. Process control on the processed wafers is also done using cassette-to-cassette systems.

Implant activations, silicide alloys, and glass reflows are performed using cassette-to-cassette rapid thermal annealing to maintain the control on junction depths and the reproducibility of polycide sheet resistance.

No gas or liquid source dopants are used in the furnace operations. The dopings are done using cassette-to-cassette ion-implanters. These implanters are located in the chase areas with only their end stations located in the Class 10 areas.

FACILITY/CLEAN ROOM LAYOUT

Figure 1 shows the wafer fab area layout, which is capable of 500 wafers-a-day out, working 24 hours a day. The total area is 10,028 square feet, with 4,460 square feet for the Class 10 clean room (976 square feet for clean room corridors), 5,064 square feet for chases, and 504 square feet for the change room. All the equipment is placed to follow the process flow and thus reduce the inventory points and personnel traffic.

The total facility is located in a 50,000-square foot building. A summary of the facility is provided in Tables 1 and 2. Various considerations for this facility were discussed in the previous section.

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Figure 1

WAFER FAB LAYOUT

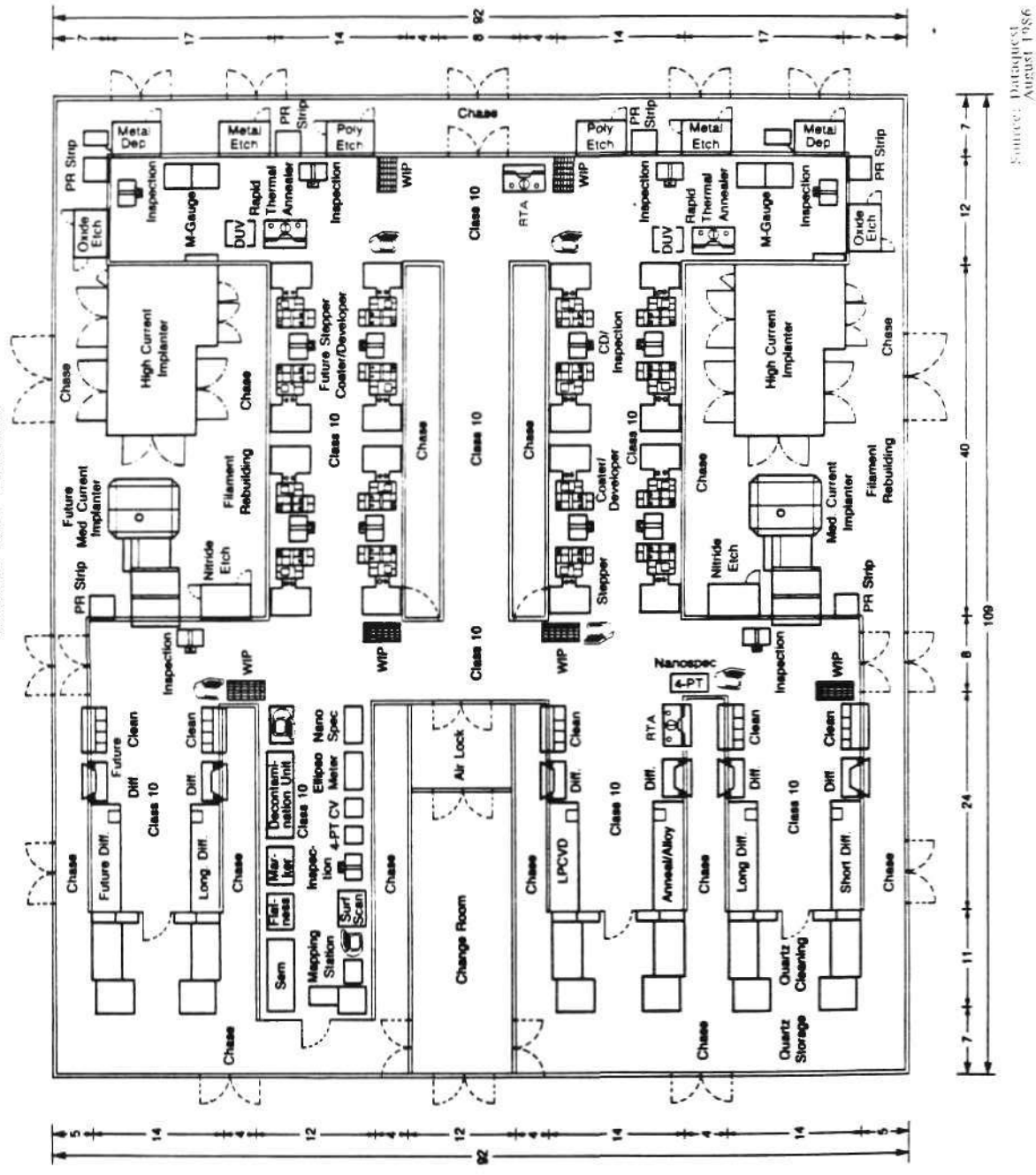

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Table 1

SUMMARY OF MANUFACTURING AREAS
(In Square Feet)

Wafer Fab	
Diffusion	1,008
Photo	1,120
Etch	936
Process Control	420
Clean Room Aisle	976
Chase	5,064
Locker/Change Room	504
Total Wafer Fab	10,028
Office/Aisles	12,000
Personnel Services	
Lobby	500
Security	100
Restrooms	1,500
Copy Room	200
Conference Rooms	800
Data Processing	800
Library	300
Document Control	300
Lunch Room	3,000
Training	500
Total Personnel Services	8,000
Support	
Store	2,500
Hazardous Chemical Store	1,000
Chemical Mix	300
Maintenance	1,500
QC/QA	500
Electrical	500
Mechanical/DI Pad	7,500
Miscellaneous/Future	6,172
Total Support	19,972
Gross Area	50,000

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Table 2

SUMMARY OF MANUFACTURING FACILITY REQUIREMENTS

Clean Room	
Temperature	68 ± 1° F
Relative Humidity	40 ± 2% for photoresist area, otherwise 40 ± 5%
Floor Vibration	10 microns maximum
Particle Count (0.1μ m)	10 per cubic foot maximum
Recovery Time	6-10 seconds
Chases Particle Count (0.5μ m)	100-1,000 per cubic foot
Electrical Hook-Up	2,000 KVA with isolated clean power for control circuitry
DI Water	
DI Water Production Capability	70 GPM
DI Water Storage	25,000 gallons
Bulk Gas Tank	
Nitrogen	15,000 gallons
Hydrogen	2,000 gallons
Oxygen	2,000 gallons
Argon	2,000 gallons
HVAC	
Air Conditioning	500 tons
Exhaust	100,000 CFM
Chilled Water	150 GPM at 60-70°F
Waste Treatment	
Solvent Storage Tank	1,000 gallons
Acid Neutralization	3 x 500 gallons
Sewer Water	100 GPM

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OPERATIONAL STRATEGY--PRODUCTIVITY CONSIDERATIONS

Asset Utilization

State-of-the-art equipment and Class 10 clean room assets are the most expensive elements of wafer manufacturing. Hence, the utilization factor of these assets, as determined by the work schedules and uptime, is an important feature of the present-day wafer fab.

The operation discussed here involves an around-the-clock, 7-day-a-week, 360-day-a-year work schedule, with no weekend or general module shutdown (except for a 5-day period and for item-by-item preventive maintenance). Therefore, there is minimum equipment downtime due to the "shut down--start up" syndrome. Equipment uptime is also improved by expert handling and through proper maintenance with user/vendor collaboration.

The around-the-clock operation can be organized in various ways. In this model, it is accomplished using two shifts a day of 12 hours each, and a split week alternating a 4-day week with a 3-day week. Four groups of people provide full 7-day coverage as illustrated in Table 3. Production is done by skilled and trained fab technologists.

The features that make this model work well are as follows:

- The fab technologists are highly qualified and cross-trained.
- The equipment is highly automated.
- Real-time, computer-based communications are utilized.

Table 3

WAFER FAB SHIFT SCHEDULE

	1st Week							2nd Week						
	M	T	W	T	F	S	S	M	T	W	T	F	S	S
6 a.m.-6 p.m.	Group I				Group III			Group I			Group III			
6 p.m.-6 a.m.	Group II				Group IV			Group II			Group IV			

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CYCLE TIME

Return on assets cannot be maximized without proper management of cycle time. A short cycle time minimizes the inventory costs, yield losses, special handling and expediting costs to meet customer needs, and obsolete inventories. It improves the output predictability and fast reaction to opportunities and customer needs. These assets lead to increased profitability, increased market share, satisfied customers, and better return on assets.

This model emphasizes reducing the active WIP, minimizing the inventory points, and reducing the dwell time per inventory point in order to achieve a short cycle time. Photo steps (coat, bake, align, expose, develop, and bake) are integrated as well as the diffusion steps (pre-clean, wafer transfer, and furnace loading) in order to reduce the inventory points and the inventory dwell times. Material flow is improved by the use of computerized production control and WIP balance. Continuous manufacturing operation around the clock improves the time utilization and minimizes the equipment requalification on each start-up that would occur after weekend shut-down.

An analysis of wafer fab cycle time for an 11-mask CMOS process is shown in Table 4. (The cycle time is reduced to two weeks by reducing the inventory points, and the average dwell time per inventory point is reduced by using an integrated and automated manufacturing facility.) The calculations are based on the following assumptions:

- Additional inventory points in the conventional line are needed due to separate coat, develop, and diffusion clean steps in photo and diffusion areas.
- This model fab obtains better material flow due to computerized production control; thus, WIP balance, automation, high equipment uptime, and fab technologist concept are achieved.
- A 7-day, 24-hour operation is assumed in a leading-edge line as compared to a 5-day, 24-hour operation in a conventional line.
- Net process time and inventory dwell times are improved due to equipment integration, less rework, and higher equipment throughput.

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Table 4

CYCLE TIME ANALYSIS FOR 11-MASK CMOS PROCESS

		Conventional Line	Leading-Edge Line
A.	Net Process Time (Hours)	250.00	200.00
B.	Number of Inventory Points	110.00	65.00
C.	Number of Process Blocks	35.00	35.00
D.	Average Dwell Time per Inventory Point (Hours)	1.00	0.50
E.	Average Time per Block Transfer (Hours)	2.00	2.00
F.	Total Dead Time (BxD) + (CxE) (Hours)	180.00	102.50
G.	Material Flow Efficiency	0.70	0.90
H.	Percent Utilization of Weekly Time	0.71	1.00
I.	Cycle Time (A+F)/(GxH) (Weeks)	5.15	2.00

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COMPUTER-AIDED PRODUCTION MANAGEMENT

Computer management of total wafer fab has become essential to high productivity in a modern facility. A large measure of a semiconductor company's competitive advantage comes from the efficient use of its manufacturing systems. Until recently, planning, execution, data collection, data analysis, process control, and WIP management have been largely manual or, at best, semiautomatic. Preventive actions have been difficult to plan, and incipient problems have had to become catastrophic before they became visible.

In the new fabrication line, this has changed. The new lines have computerized the deployment of personnel, material, and equipment; WIP management and adjustments to changing dynamics of the production floor; status monitoring of equipment and facility; and recipe downloading and process control. Real-time availability of data permit expedited problem diagnostics and therefore the solution to those problems. Yield improvements are achieved at a faster rate. Cycle times are dramatically reduced and the slope of the learning curve is enhanced.

Dataquest believes that the computerization of the following functions are most desirable in the emerging fab:

- Centralization of data and their update in real time
- WIP management, line balancing, and yield computations

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- Cost collecting systems
- Yield analyses, lot histories, and statistical analyses
- Process documentation and process control
- Lot scheduling to meet fab out schedules and automatic lot status logging
- Maintenance scheduling, spare parts, uptime history, and downtime causes
- Downloading of process recipes
- Equipment monitoring for performance and quality of operation
- Monitoring of all facility functions
- Quality, productivity, and efficiency monitoring
- Flags on all out-of-specification conditions

The hardware and the software necessary to handle most of these functions are available today. Although a lack of standardization and various incompatibilities between various systems and equipments still exist, vigorous third-party software houses that supply application programs have emerged. Standardization in equipment interface has also begun to emerge. While there are still some substantive issues to be resolved regarding equipment interfaces and standardization, work is under way at present to resolve these incompatibilities. Dataquest believes that most if not all of these issues will be resolved in 1987.

PROCESS FLOW

The rapid reduction in the feature sizes has required the use of low-resistivity gate materials and shallow junctions. N^+ poly is still the best-characterized and most understood gate material. Silicidation of the top of poly gates (polycide) provides a well-controlled, low-resistivity gate material. Barrier metal is required before interconnect aluminum-silicon alloy is deposited to avoid spiking through shallow junctions.

With the reduction in design rules, latch-up susceptibility in the conventional bulk CMOS has also increased. With smaller geometries, latch-up is effectively minimized by the use of epitaxial substrate. Twin-well CMOS process is preferred with the use of epitaxial substrate

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to optimize and balance the performance of n-channel and p-channel devices. Two layers of low-resistivity conductors are utilized for a variety of CMOS applications in order to achieve higher performance and packing densities.

With these considerations, a double poly (polycide gate), single-metal, twin-well CMOS process flow is described in Table 5; the major process steps are summarized in Table 6.

The epi material used for the process is assumed to be purchased from silicon vendors; therefore, no equipment related to epi growth is shown. The conventional oxide isolation technique is used for this process until the trench isolation technique is perfected. The surface doping requirements to avoid the short channel effects are such that for 5V CMOS devices, no field implants are needed for sub-2-micron geometries. Following the gate oxidation, a single low-energy BF_2 implant is used to adjust both n- and p-channel threshold voltages.

This 11-mask process is suitable for a variety of applications, such as SRAM microprocessors. Certain products may need modifications in the process flow to meet the specific device and topological requirements of the specific product. Although the process requires 11 photomasking steps, it requires 12 resist coating steps. To remove oxide, poly, and nitride from the back of the wafer, a layer of resist is spun on the front of the wafer to protect the devices during backside etch. This resist layer does not need to be either exposed or developed.

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Table 5

DOUBLE POLY (POLYCIDE GATE), SINGLE METAL,
TWIN-WELL CMOS PROCESS FLOW

Process Step

Pad Oxide
Masking Nitride
P-well Photo--Defines P-well
Etch Nitride
Boron Implant--P-well implant

Photoresist Strip
Diffusion Pre-Clean
P-well Drive-in/Oxidation
Etch Oxynitride
Strip Nitride

Phosphorous Implant--Self-aligned N-well I^2
Diffusion Pre-Clean
N-well Drive-in
Strip Oxide
Pad Oxide

Masking Nitride
Active Area Photo--Defines all active devices
Etch Nitride
Photoresist Strip
Diffusion Pre-Clean

Field Oxidation
Etch Oxynitride
Strip Nitride
Etch Pad Oxide
Gate Oxidation

BF_2 Implant--Adjust both N- and P-channel device thresholds
Pre-Poly Clean
Doped Poly I Deposition
Silicide Sputter
Silicide Alloy

(Continued)

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Table 5 (Continued)

DOUBLE POLY (POLYCIDE GATE), SINGLE METAL,
TWIN-WELL CMOS PROCESS FLOW

Process Step

Gate Photo--Defines all gates
Etch Polycide
Photoresist Strip
Diffusion Pre-Clean
Source/Drain Oxidation--Re-oxidize source/drain

N^+ Photo/DUV--Defines N^+ regions; DUV = deep UV curing of resist to improve resist survivability during plasma/RIE etching
Arsenic Implant--N^+ implant (high dose)
Photoresist Strip
P^+ Photo/DUV--Defines P^+ regions

BF_2 Implant--p^+ Implant (High Dose)
Photoresist Strip
Diffusion Pre-Clean
Rapid Thermal Anneal--Activate N^+/P^+ Areas
Diffusion Pre-Clean

LTO Deposition
Poly Contact Photo--Defines poly-to-poly and poly-to-diffusion contact
Pre-Poly Clean
Poly II Deposition
Poly II Photo--Defines second Poly

Poly II Etch
Photoresist Strip
Poly II Implant Photo--Defines low resistivity Poly II areas
Phosphorous Implant
Photoresist Strip

Diffusion Pre-Clean
Rapid Thermal Anneal--Activate Poly II implant
LTO Deposition
Rapid Thermal Anneal--Reflows LTO over poly II steps
Contact Photo--Define all contacts with sloped sidewalls for reliable metal step coverage

(Continued)

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Table 5 (Continued)

DOUBLE POLY (POLYCIDE GATE), SINGLE METAL,
TWIN-WELL CMOS PROCESS FLOW

Process Step
Oxide Etch
Photoresist Strip
Surface Oxide Etch
Barrier Layer + Metal Deposition--Barrier metal and aluminum-silicon alloy are sequentially deposited
Metal Photo/DUV--Defines metal
Metal Etch
Photoresist Strip
Pre-Alloy Clean
Alloy
Pre-Passivation Rinse
Passivation Deposition
Passivation Photo--Scratch protection mask
Passivation Etch
Photoresist Re-Coat
Back-Side Etch
Photoresist Strip
Parametric Mapping--Parametric Screening
Final QC/Ship to Wafer Sort

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Table 6

PROCESS SUMMARY

Process Steps/Photoresist Strips

1. Well	2. Active	3. Gate
4. N^+	5. P^+	6. Poly cont.
7. Poly II	8. Poly II I^2	9. Contact
10. Metal	11. Passivation	12. Back etch

Nitride Plasma Etch

1. Pre-well	2. Post-well	3. Pre-field
4. Post field		

Poly/Polycide RIE/Plasma Etch

1. Gate polycide	2. Poly II	3. Back-etch

Oxide RIE/Plasma Etch

1. Poly contact	2. Contact	3. Surface oxide

Metal RIE/Plasma Etch

1. Metal + barrier layer

Medium Implants

1. P-well	2. N-well	3. VT adjust
4. Poly II		

High Dose Implants

1. N^+	2. P^+

Metal Deposition

1. Silicide	2. Barrier + Al alloy

(Continued)

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Table 6 (Continued)

PROCESS SUMMARY

Short Diffusion

1. Well pad oxidation	2. P-well oxidation	3. Field pad oxidation
4. Gate oxidation	5. S/D oxidation	

Anneal/Alloy

1. Metal alloy

Long Diffusion

1. Well drive-in	2. Field drive-in

LPCVD

1. Well nitride	2. Field nitride	3. Poly I
4. Poly II	5. Interpoly LTO	6. Pre-metal LTO
7. Passivation		

Rapid Thermal Anneal

1. Silicide alloy	2. S/D Activation	3. Poly I^2 activation
4. LTO reflow		

Wet Etch

1. Oxynitride I	2. Well oxidation	3. Oxynitride II
4. Field pad oxidation	5. Passivation etch	6. Back etch

Diffusion Pre-Clean

1. P-well oxidation	2. Well drive-in	3. Field oxidation
4. Poly I	5. S/D oxidation	6. S/D anneal
7. Interpoly LTO	8. Poly II	9. Pre-metal LTO

Pre-Deposition Clean

1. Pre-barrier + Al-alloy	2. Pre-passivation

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EQUIPMENT CAPACITY ANALYSIS

The daily wafer out capacity of the key manufacturing equipment depends on the process complexity. Major process steps for the double poly, single metal process described are summarized in Table 6. Based on this process and the intrinsic data for the process equipment (i.e., wafer pass per hour, uptime, daily production availability, rework rate, and mechanical yield), the daily wafer out capacity for the key equipment shown in Table 7 is based on around-the-clock equipment utilization.

Equipment, clean room, and chase requirements for the equipment needed to do 500 wafers out per day, 14,000 wafers out per period, is calculated in Table 8. Equipment utilization based on these calculations is also included in Table 8.

As noted from these calculations, about $20 million worth of equipment is needed for this facility. One stepper is dedicated per masking layer. Additional steppers will be needed if a more complex process is required for some applications. Enough room is provided in the manufacturing facility layout to accommodate up to 16 steppers, plus one additional furnace bank and an implanter. The cost analysis presented in this report will be affected slightly by the additional equipment required for a more complex process. A list of equipment needed, including the potential vendors and typical lead times, is presented in the appendix at the end of this section.

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Table 7

CAPACITY ANALYSIS FOR 100 PERCENT EQUIPMENT UTILIZATION

Equipment	Wafers/ Hour	Uptime	Available Hours/Day	Rework Rate	Turns/ Wafer	Mechanical Yield	Wafers Out Per Day*
Coat/Develop	45	0.90	20	0.05	12	1.000	64
Stepper (1X)	30	0.90	20	0.05	11	1.000	47
Auto Inspect/CD Measurement	40	0.95	20	0.02	15	0.990	49
Resist Strip	60	0.95	20	0.05	12	1.000	90
Nitride/Poly Etch	60	0.90	20	0.03	7	0.995	149
Oxide Etch	60	0.90	20	0.03	3	0.995	349
Metal Etch	30	0.80	18	0.03	1	0.995	417
Implant (Medium)	150	0.90	18	0.00	4	0.995	604
Implant (High)	45	0.90	15	0.00	2	0.995	302
Metal Deposition	60	0.90	18	0,02	2	0.995	474
Short Diffusion (4 Tubes)	30	0.95	18	0.00	1	1.000	513
Anneal/Alloy/Short Diffusion (4 Tubes)	60	0.95	18	0.00	1	1.000	1,026
Long Diffusion (8 Tubes)	15	0.90	20	0.00	1	1.000	270
LPCVD (4 Tubes)	60	0.90	20	0.02	2	0.990	524
Rapid Thermal Anneal	60	0.90	18	0.02	4	1.000	238
Diffusion Clean/Wet Etch and Pre-deposition Clean	100	0.95	18	0.02	17	0.995	98
Parametric Mapping	30	0.95	20	0.05	1	0.950	514
Net Cumulative Fab Yield						0.899	

*Wafers out per day = (Wafers/hour x available hours/day x uptime x (1 - rework rate) x mechanical yield) ÷ turns/wafer

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Table 8

MANUFACTURING EQUIPMENT COST/CAPACITY ANALYSIS
FOR 500 WAFERS OUT/DAY

Equipment	Wafer/ Day/Unit	$K/ Unit	Clean Room Sq. Ft./ Unit	Equipt Chase Sq. Ft./ Unit	Number Needed	Equipment Utilization	Total K$	Total Clean Room Sq. Ft.	Total Equipt Chase Sq. Ft.
Coat/Develop	64	150	16	6	11	0.71	1,650	176	66
Stepper (1X)	47	500	16	6	11	0.97	5,500	176	66
Auto Inspect/CD	49	145	12	0	13	0.78	1,885	156	0
Resist Strip	90	60	10	40	6	0.93	360	60	240
Nitride/Poly Etch	149	150	25	50	4	0.84	600	100	200
Oxide Etch	349	200	25	50	2	0.96	400	50	100
Metal Etch	417	400	25	50	2	0.60	800	50	100
Implant (Medium)	604	600	40	200	1	0.83	600	40	200
Implant (High)	302	1,250	40	400	2	0.83	2,500	80	800
Metal Deposition	474	500	30	60	2	0.53	1,000	60	120
Short Diffusion (4 Tubes)	513	260	70	70	1	0.97	260	70	70
Anneal/Alloy (4 Tubes)	1,026	260	70	70	1	0.49	260	70	70
Long Diffusion (8 Tubes)	270	260	70	70	2	0.93	520	140	140
LPCVD (4 Tubes)	524	400	70	70	1	0.95	400	70	70
Rapid Thermal Anneal	238	150	20	10	3	0.79	450	60	30
Diffusion Clean/ Wet Etch	104	180	30	40	5	0.96	900	150	200
Miscellaneous	500	1,750	2,972	2,602	1	1.00	1,795	2,952	2,592
							19,880	4,460	5,064

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WAFER THROUGHPUT YIELD

With the use of automated equipment, equipment integration, and increased emphasis on equipment reliability, the wafer throughput yield has increased continually over the years, in terms of both mechanical yield and parametric yield. For the process described before, the wafer throughput yield for various photomasking blocks is projected in Table 9. (The corresponding mechanical yield for various equipment is shown in Table 7.)

Table 9

MECHANICAL WAFER YIELD

Step	Yield
Well Photo	0.997
Active Photo	0.995
Gate Photo	0.993
N^+ Photo	0.997
P^+ Photo	0.997
Poly Contact Photo	0.995
Poly II Photo	0.993
Poly II I^2 Photo	0.997
Contact Photo	0.993
Metal Photo	0.993
Passivation Photo	0.997
Parametric Mapping	0.950
Overall Throughput Yield	0.900

Source: Dataquest
August 1986

STAFFING REQUIREMENTS/ORGANIZATION

The total staffing requirement for the facility described here is shown in Table 10. This plant will require 124 people, of which 76 are direct labor responsible for wafer manufacture. The other 48 people are indirect labor associated with management, engineering, quality control, and general administration. The organization of manpower is depicted in Figure 2.

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Table 10

STAFFING REQUIREMENT

Category	Number	Annual Salary/Person ($K)	Total Salary Per Period ($K)
Direct			
Lead Technician	4	32	$ 9.85
Fab Technician	60	24	110.77
Material Handler	4	18	5.54
Maintenance	8	29	17.85
Total Direct Labor	76		$144.00
Indirect			
Wafer Fab			
Operations Manager	1	60	$ 4.62
Engineers	5	43	16.54
MIS Engineers	2	43	6.62
Secretary	1	18	1.38
Subtotal	9		$ 29.16
QC/QA			
Manager	1	54	$ 4.15
QC/QA Engineers	2	43	6.62
Technicians	4	24	7.38
Trainers	2	27	4.15
Document Control	1	18	1.38
Secretary	1	18	1.38
Subtotal	11		$ 25.08

(Continued)

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Table 10 (Continued)

STAFFING REQUIREMENT

Category	Number	Annual Salary/Person ($K)	Total Salary Per Period ($K)
Production/Material/Facility			
Manager	1	54	$ 4.15
Production Planners	2	24	3.69
Purchasers	2	43	6.62
Shipping/Receiving/Store	2	18	2.77
Facility Engineers	2	43	6.62
Technicians	4	24	7.38
Safety	1	43	3.31
Security Manager	1	54	4.15
Guards	4	18	5.54
Secretary	1	18	1.38
Receptionist	1	18	1.38
Subtotal	21		$ 47.00
General Administration			
Plant Manager	1	100	$ 7.69
Controller	1	54	4.15
Financial Analyst	1	43	3.31
Personnel Manager	1	54	4.15
Personnel Assistant	1	43	3.31
Executive Secretary	1	27	2.08
Secretary	1	18	1.38
Subtotal	7		$ 26.08
Total Indirect Labor	48		$127.32
Total Staffing	124		$271.32

Notes:

1. Annual salaries are for 1986-1987.
2. Staffing level is based on four alternate work pattern manufacturing groups.

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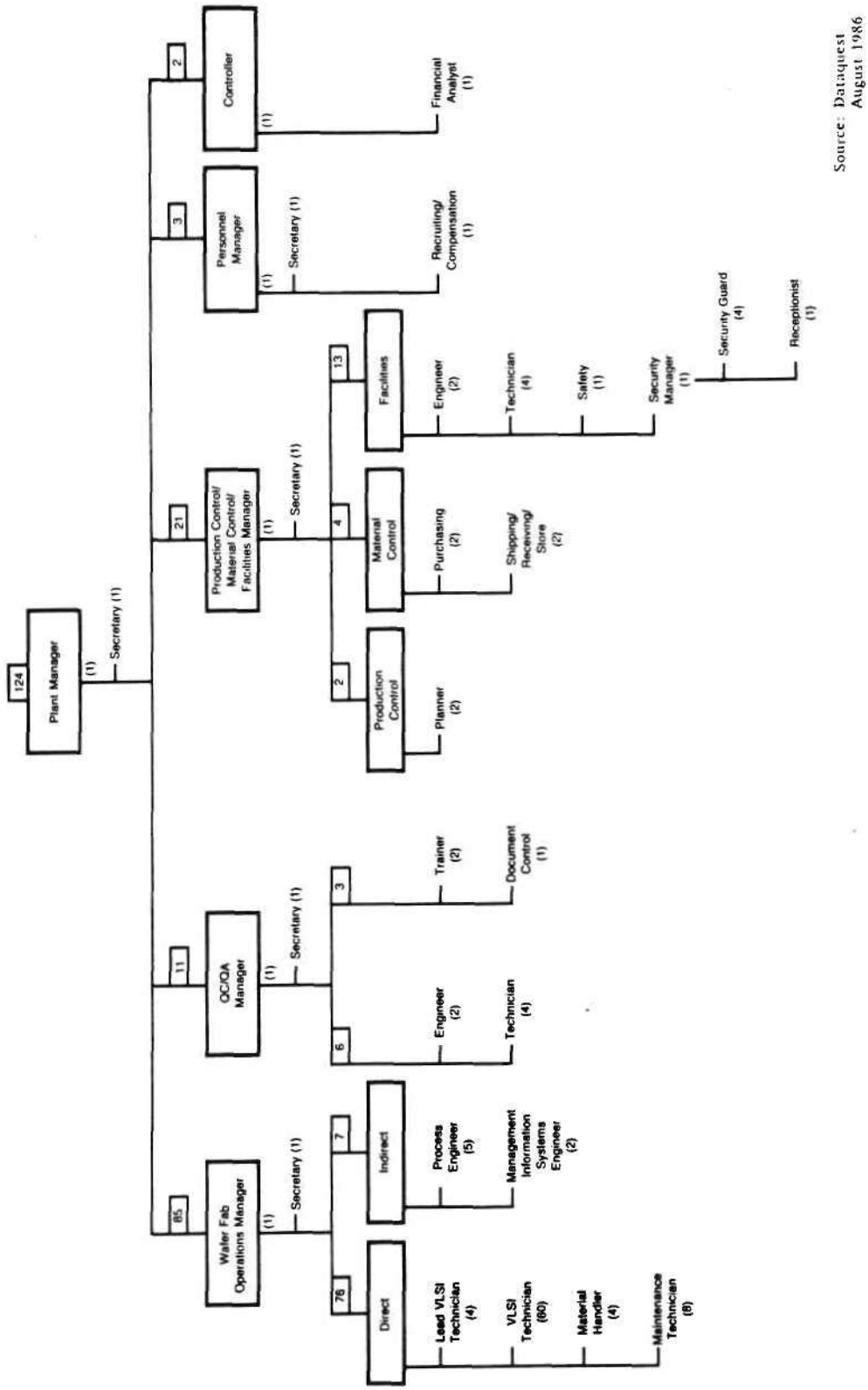
Figure 2

ORGANIZATION CHART



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With this staffing, the average wafer out per direct labor is 46 per week in this facility. This is possible with around-the-clock facility utilization, high throughput, automated equipment and computer controlled WIP, and production management.

COST ANALYSIS

The manufacturing costs per 150mm wafer are analyzed in Tables 11 and 12. Table 11 itemizes various cost assumptions. The building is depreciated over 25 years, and the equipment and clean room are depreciated over 5 years. Electricity cost is assumed at $0.06 per KWH. Since the wear-out of reticles is minimal, their costs are not included in this model nor is the original cost of procurement of the reticles.

With these and other assumptions, as outlined in Table 11, the total manufacturing cost per 150mm wafer in this facility is about $173, of which about $101 are variable costs like materials and labor, and the other $72 are fixed costs such as indirect labor, utilities, and depreciation. The wafer cost in this model is less than the cost in the model we published in 1985. The difference in cost is due mainly to two factors: the decrease in price in epitaxial wafers ($50 versus $60) and the cost increase due to the higher equipment cost and associated maintenance and spare parts. The net effect has been as $5 reduction in wafer cost for the current model.

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Table 11

ITEMIZED COST ELEMENTS

Item	
Wafers Finished/Period	14,000
Mechanical Yield	0.9
Wafer Starts/Period	15,556
Average Wafer Movement Per Period	14,778
Active WIP Wafers	7,389
Cost per Wafer Start (Epi wafer)	$50
Chemical Cost/Wafer	$10
Process Gas Cost/Wafer	$10
DI Water Usage (GPM)	50
DI Water Cost/1,000 Gallons	$6
Operating Supplies/Wafer	$10
Electricity Requirement (KW)	1,500
Electric Rate/KWH	$0.06
Sewage Water (1,000 gallons/day)	144
Sewage Water Cost/1,000 gallons	$1
Gas/Vacuum/Air (Cost/Wafer)	$1
Fab Area (Clean Room+Chase) ($ft.^2$)	10,028
Building ($ft.^2$)	50,000
Building Cost (at $100/$ft.^2$)	$5,000,000
Fab Area Cost (at $400/$ft.^2$)	$4,011,200
Equipment Costs (15% added for freight, installation, & taxes)	$22,862,000
Equipment maintenance and spares (at 1% of cost per period)	$228,620
Building Insurance (at 1%/year of value) per period	$3,846
Equipment Insurance (at 2%/year of value) per period	$35,172
Inventory Insurance (at $1/active WIP wafer)	$7,389
Property Tax (at 1.2%/year of building) per period	$4,615

Notes:

1. Building depreciation at 25 years straight line
2. Equipment and clean room depreciation at 5 years straight line
3. Clean room counted as equipment for maintenance and insurance purposes

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Table 12

WAFER COST ANALYSIS

	Cost/Period ($K)	Cost/Wafer Out ($)
Variable Costs		
Material		
Wafers	$ 778	
Chemicals	148	
Process Gases	148	
DI Water	12	
Supplies	148	
Subtotal	$1,234	$ 88.14
Direct Labor		
Salary	$ 144	
Fringe Benefits (25%)	36	
Subtotal	$ 180	$ 12.86
Total Variable Cost	$1,414	$101.00
Fixed Manufacturing Overhead		
Indirect Labor Salary		
Wafer Fab	$ 29	
QC/QA	25	
Production/Material/Facility	47	
General Administration	26	
Total Indirect Labor Salary	127	
Fringe Benefit (25%)	32	
Travel & Other Expenses (8% of Salary)	10	
Subtotal	$ 169	$ 12.05
Electricity	$ 60	$ 4.32
Water/Sewage	$ 4	$ 0.29
Gas/Vacuum/Air	$ 15	$ 1.06

(Continued)

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Table 12 (Continued)

WAFER COST ANALYSIS

	Cost/Period ($K)	Cost/Wafer Out ($)
Insurance and Tax		
Building Insurance	$ 4	
Equipment Insurance	35	
Inventory Insurance	7	
Property Tax	5	
Subtotal	$ 51	$ 3.64
External Services/Maintenance		
External Services (Waste Disposal, etc.)	$ 50	
Maintenance	229	
Subtotal	$ 279	$ 19.93
Depreciation		
Building (25 years)	$ 15	
Clean Room and Equipment (5 years)	413	
Subtotal	$ 428	$ 30.57
Total Fixed Manufacturing Overhead	$1,006	$ 71.86
Total Wafer Cost	$2,420	$172.86

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Appendix A

LIST OF EQUIPMENT

Equipment	Vendor	Unit Cost ($K)	Lead Time (Weeks)	Number Needed	Total Cost ($K)
Wafer Fab					
Coat/Develop	MTI, SSI, SVG, Solitec, GCA	$ 150	20-25	11	$ 1,650
Stepper (1x)	Ultratech	500	36-40	11	5,500
Auto Inspection/CD	OSI, Nikon, Leitz, Matrix	145	20-25	13	1,885
Resist Strip	IPC, Drytek, Matrix, Tegal	60	20-25	6	360
Nitride Etch	LAM, Tegal, Drytek, AMT	150	20-25	2	300
Polycide Etch	LAM, Tegal, Drytek, AMT	150	20-25	2	300
Oxide Etch	LAM, Tegal, Drytek, AMT	200	20-25	2	400
Metal Etch	Zylin, ET, Tegal, AMT	400	20-25	2	800
Acid Processor	FSI, Fluorocarbon, Semi-Tool	180	25-30	5	900
Medium Dose Implanter	Eaton, Varian, Veeco	600	36-40	1	600
High Dose Implanter	Eaton, Veeco, Varian	1,250	36-40	2	2,500
Metal Deposition	Varian, ET, MRC	500	25-30	2	1,000
Diffusion Furnace (4 Tube/Stack)	Tylan, BTU, Thermco	260	36-40	4	1,040
LPCVD (4 Tubes)	ACS, Anicon, Thermco, Tempress	400	36-40	1	400
Rapid Thermal Anneal	AG, Varian, Eaton, Peak	150	20-25	3	450
Subtotal					$18,085
Process Control and Maintenance					
Vacuum Bake Oven	VWR, Fisher, Blue-M	$ 5	15-20	5	$ 25
Microscope	Nikon, Leitz, Olympus	15	20-25	5	75
Wafer Transfer System	MGI, Procronics, Quartz Int.	15	20-25	5	75
DUV Illuminator	Fusion System, OAI, HTG	25	20-25	2	50
Thickness Measurement	Nanometrics	50	20-25	2	100
Ellipsometer	Rudolph, Gaertner	50	20-25	1	50
Four-Point Probe	Veeco, ASM, Magne-Tron, Eaton	25	15-20	2	50
Spreading Resistance	SSM	125	25-30	1	125
CV Plotter	MDC, PAR, MSI	30	20-25	1	30
Metal Thickness Measurement	Tencor	15	20-25	2	30
Surface Particle Monitor	Tencor, Hamamatsu, Aeronca	65	25-30	1	65
Wafer Flatness Analyzer	ADE, GCA, Prometrix, Siltec	30	25-30	1	30
Surface Profiler	Tencor, Sloan, Siltec	15	20-25	1	15
Decontamination System	Atcor	25	20-25	1	25
Wafer Marker	LIS, ADE	25	25-29	1	25
Mapping Station	Keithley, Hewlett-Packard	150	25-30	1	150
Wafer Prober	Electroglas/Xynetics, PWS, Teledyne	25	25-30	2	50
Curve Tracer	Tektronix	15	20-25	2	30
Meters, Power Supplies	HP, Fluke, Keithley	10	15-20	3	30
SEM	Cambridge, Amray, ISI	150	25-30	1	150
Micro-Probe	Kevex, EP&F	50	25-30	1	50
CIM Package	Consilium, IP Sharp	250	25-30	1	250
Gas Analyzer	Balzers, Inficon, Edwards	15	15-20	1	15
Leak Detector	Veeco, Edwards, Varian	25	15-20	2	50
Particle Monitor	Climet, Hiac/Royco	15	15-20	1	15
Air Flow Meter	Alnor, Kurz	5	15-20	1	5
Tube Cleaning Station	IAS, Polyflow	15	20-25	1	15
Bead Blast	Various	5	15-20	2	10
Sputter Part Cleaning	Various	10	15-20	1	10
Strobe, Exposure Meter	Various	5	15-20	1	5
Gas Cabinets	Semi-Gas, Vari-Flow	5	15-20	5	25
Quartz Storage	IAS, Various	5	15-20	2	10
Mask Storage	Various	25	15-20	2	50
Vib. Free Table	Newport, Kinetic Systems, TMC	3	15-20	10	30
Clean Room Temperature	Various	25	15-20	1	25
Maintenance Tools	Various	50	15-20	1	50
Subtotal					$ 1,795
Grand Total					$19,880

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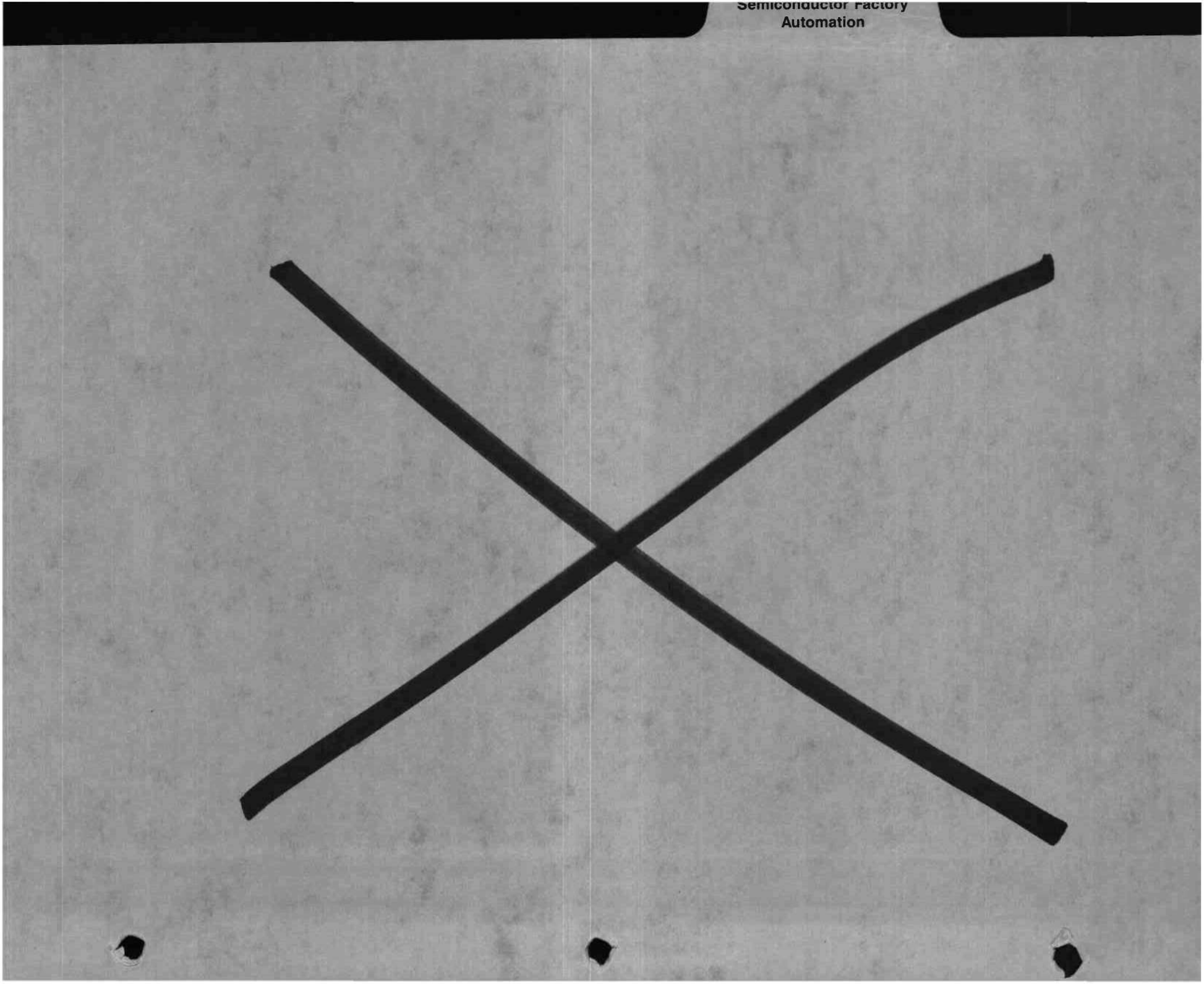

Semiconductor Manufacturing Automation

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- Equipment Communication

Equipment Communications

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Equipment Communications

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Equipment Communications

SUMMARY

To maintain a competitive edge in manufacturing technology, major semiconductor manufacturers worldwide are adopting a strategy for automation of fabrication facilities in the 1980s. Processing and test equipment, workstation terminals, robots, and material transfer systems are being linked together through a communications network to support integrated manufacturing on the shop floor. Sophisticated software packages to control and coordinate the manufacturing environment are being developed in order to provide semiconductor manufacturers with timely access to the flow of information that characterizes the fabrication sequence of today's advanced devices.

The financial and strategic incentives for implementing computer integrated manufacturing (CIM) in the semiconductor industry have been the subject of numerous symposia and publications. The central goals of automation include efficient WIP (work in progress) monitoring of wafers through the processing sequence, increased equipment utilization through efficient line balancing, process recipe management, as well as access to and analysis of data to optimize process control in real time. In addition, the removal of the operator from the processing environment results in yield enhancement through reduced particulates. Semiconductor manufacturers must choose from a variety of criteria to evaluate the payback analysis most appropriate for automation of their facilities.

Protocol Specifications

Regardless of the CIM software package being employed, whether it is the result of an in-house development effort or a commercially available product, a successful automation effort requires a communications protocol for the network in order to establish the electronic guidelines for communication between the various computing devices on the shop floor. A communications protocol helps to ensure operational consistency and compatibility among the equipment-level, cell-level, and factory host computers operating in the network environment. In the semiconductor industry, SEMI (Semiconductor Equipment and Materials Institute) has proposed and developed SECS (SEMI Equipment Communications Standard) as a communications protocol for semiconductor manufacturing. Semiconductor equipment manufacturers are responsible for implementing the SECS protocol on their equipment to enable equipment/host communications within the fab.

Several semiconductor manufacturers such as Intel, Texas Instruments, and Thomson Components-Mostek Corporation, have already established minimum protocol specifications. DATAQUEST believes that equipment manufacturers that can satisfy the needs of IC manufacturers will gain a

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strategic market advantage in providing equipment to the semiconductor industry. Equipment manufacturers have the opportunity to participate in the formative stages of automation in the semiconductor industry, and in the process, to establish firm relationships with the automation leaders.

Equipment/Host Communications

The SECS protocol supports a hierarchical topology of computing devices in the semiconductor manufacturing environment. A host computer (for example, a VAX computer from Digital Equipment Corporation) is located at the top of this network topology and communicates with node or cell-level computers at an intermediate level. The node computers (for example, MicroVAX computers), in turn, communicate directly with a given set of processing equipment or robots that has been grouped together in a manufacturing cell. The equipment within a cell typically has similar processing functions and responsibilities, and as such exists as a distinct area of manufacturing activity. Semiconductor manufacturers have chosen a cell-by-cell approach to equipment automation in their facilities by automating one processing area at a time, such as a diffusion cell or photobay, and adding automation capabilities to new cells as time and resources allow.

As an example of an actual installation, Figure 1 illustrates the configuration of processing equipment, robotics, and computers in a fully automated diffusion furnace cell. Thomson Components-Mostek Corporation has chosen the Consilium COMETS package, including the PAM (Process Automation Management) module, for computer integrated manufacturing at its Carrollton, Texas, facility. An operator is responsible for inputting the appropriate lot identification (ID) at a workstation terminal in the fab. The host receives the ID number of the lot awaiting diffusion, and communicates the information to the cell-level controller and Veeco-dedicated MicroVAX, which in turn communicate with the robots and AGVs (automatic guided vehicles) that are responsible for material movement within the cell. The appropriate process recipe is downloaded from the node (cell-level) computer to the diffusion furnace, and the process is initiated automatically. All of the relevant processing status information and results are communicated to the node computer and the host system via the SECS II protocol, a subset of the SECS protocol that specifies a detailed message set for semiconductor manufacturing.

The purpose of this study is to evaluate and quantify the current status of SECS implementation by equipment manufacturers. The other equipment issues related to automation that will be discussed include the development of equipment-specific interfaces to link equipment to a given CIM software system, and the level of operator interactions with the processing equipment in a fabrication environment. The study also

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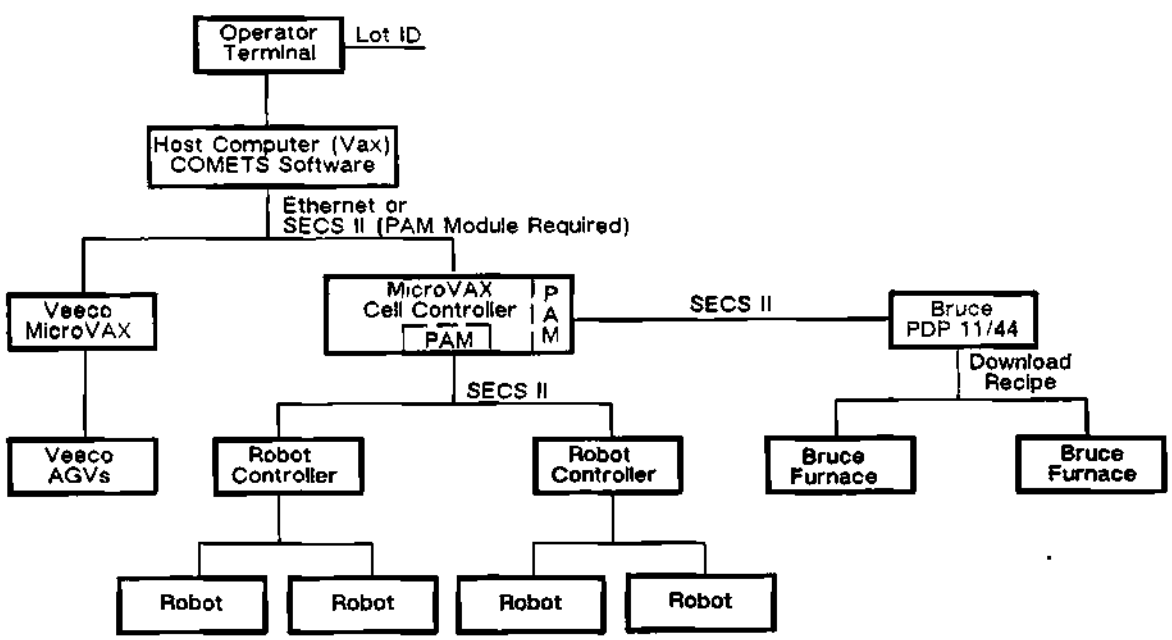
presents an overview of the SECS protocol, the communications standard MAP (General Motors' Manufacturing Automation Protocol), and MAP's potential impact on the semiconductor industry. Appendix A provides general background information on the concepts and terminology used to describe communications networks; particular emphasis is placed on those network components supported by the SECS and MAP protocols.

Figure 1

FULLY AUTOMATED DIFFUSION FURNACE CELL



Source: Thomson Components-Mostek Corp.
DATAQUEST
February 1986

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Equipment Communications

THE SECS PROTOCOL

In response to a growing concern to establish a communications protocol specifically focused on manufacturing in the semiconductor environment, the Semiconductor Equipment and Materials Institute (SEMI), through its Communications Subcommittee, proposed and developed an equipment communications protocol known in the industry as SECS. SECS is designed to provide communication capabilities between computers in semiconductor processing equipment and upstream node or host computers. In its simplest implementation, process recipe information can be downloaded from a host system to the equipment, and the equipment in turn can communicate process and equipment status information as well as collected data to the host system. Equipment-level communication (also referred to as Level 1 or cell-level communication) is the first step in a bottoms-up approach to integrated factory automation.

The SECS protocol is divided into two parts, known as SECS I and SECS II. The SECS I protocol, which addresses the electrical specifications and data link protocol between computers, was not designed to be specific to the semiconductor industry. The SECS II document, however, defines the general message set for transactions in a semiconductor processing environment, and as such, deal with units and concepts familiar to the industry, such as wafers, boats, and process recipes.

SECS I

The SECS I document was first published in SEMI Standards in 1980 and deals with the specifics of the electrical interface for connections between computers and the data link protocol (also known as the access method), which is responsible for establishing and governing the direction of communications between computers. (The electrical interface, RS-232, and the access method specified in the SECS protocol are discussed in Appendix A.) The SECS I document also defines the basic format for the message header, a 10-byte section of the message block that contains information used to ease the task of decoding transaction details.

SECS II

The SECS II document (first published in 1982) defines the message and data structures for the actual transactions between computers and processing equipment. The message set that has been chosen for the SECS protocol is meant to represent the typical activities required for IC manufacturing. Some number of custom messages may be required for

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equipment-specific applications. For a more thorough understanding of the protocol, the reader is encouraged to consult the SEMI document itself, or to participate in a tutorial short course on SECS such as that available from GW Associates, Mountain View, California.

Message Structure

A standard SECS message consists of a specified number of blocks of information. Multiblock messages are allowed by the SECS protocol and may contain up to 32,767 blocks for a total of 7.99 Mbytes of information in a single message. Each block includes a length byte, the message header (10 bytes), the text itself (0 to 244 bytes), and a checksum (2 bytes). The header (defined in SECS I) has a fixed format with bytes specified for the device ID (message source or destination can be designated), stream and function codes (identifies type of message to be sent), block number (specifies which block is being sent in a multiblock sequence), and system bytes (used for internal bookkeeping by the message source computer). The length and checksum bytes are used to validate successful message transmission between the source and destination.

Data Structure

The general topic of the message text is identified by the stream and function codes designated in the header. The message text within any given block of a multiblock message is structured as a series of data items. Each data item contains information that specifies the format of the data (ASCII, integer, floating point, etc.), the length of the data (in bytes), and the actual data itself. The protocol currently identifies 14 types of data format, and the choice of format is left to the user's discretion. A "list" data item may also be used to designate a series of data items in the message text. In a list data item, the length field specifies the number of data items contained in the list rather than the length in bytes of the list. In addition, list items can be embedded within other list items. Where appropriate, the protocol specifies the data and list structure of the different stream/function codes.

Message Set

The SECS II protocol classifies the different types of messages into eleven streams or general message types. Streams 1 through 11 are specifically defined in the protocol, while stream 0 is not used, and streams 12 through 63 are reserved for future use. Stream 64 through 127 are available for user-defined message topics.

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Within each stream, there are a number of function codes that identify the associated subtopics of each stream. The same function code can have different meanings in the different streams, but function 0 is always defined as the abort message within that stream. For each stream, functions 1 through 63 are reserved for the specified messages of the SECS II protocol and its future updates. Functions 64 through 255 are available for user-defined functions, which are also known as custom messages. The number of functions currently defined in the protocol varies from stream to stream, and new function codes will continue to be specified as the protocol matures. However, within every stream, when a conversation is undertaken between equipment and host, the query message always has an odd function value, and the response always has an even function message; together they constitute a transaction. In some streams, only the odd function codes are used because, due to the type of message, no response is required. The associated even function code for those types of messages are not used.

Stream Definitions of the SECS II Message Set - The eleven streams that have been defined in the SECS II protocol are found in Table 1, along with a brief description of the general message category. The number of specified functions within each stream is also identified. Aborts (function 0, or F0) are present in every stream and are included in the number of functions in Table 1.

Problems with the SECS Protocol

Several issues have been raised with regard to problems in the SECS protocol. Some of the concerns focus on SECS I issues and include speed of data transmission, as well as problems with "message flooding." Ambiguity in the SECS II message set and choice of data format have also been mentioned by equipment manufacturers. These points will be discussed in the following paragraphs.

SECS I Problems

The SECS I protocol specifies an RS-232 connection between equipment and host systems with a typical data transmission rate of 9,600 baud (characters per second). This is considered by many as too slow for effective shop floor communications between a large number of processing stations and a host system. Since some types of metrology and process/test equipment acquire large amounts of data, the SECS I protocol is not well suited for massive data transfers because of its limited speed. For those applications, some level of preliminary data reduction and analysis would be required before data are sent to an upstream host system. The SECS protocol also specifies a point-to-point topology, which many manufacturers consider cumbersome because of the requirement for discrete wiring and channels of communication for every communications device on the shop floor.

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Equipment Communications

Table 1

SECS II STREAM DEFINITIONS

Number	Stream Name and Definition	Specified Functions (#)
1	**Equipment Status** Allows host to monitor equipment status including current operating mode, depletion of consumables, and transfer status of material ports	11 (5 transactions, 1 abort)
2	**Equipment Control and Diagnostics** Messages deal with control operations of equipment from the host, includes remote operations and equipment self-diagnostics and calibration	29 (14 transactions, 1 abort)
3	**Material Status** Used to communicate material-in-process and time-to-completion information to the host	11 (5 transactions, 1 abort)
4	**Material Control** Used for automatic transfer of material between equipment	9 (8 odd functions, no responses specified, 1 abort)
5	**Exception Reporting** Communicates alarms generated by equipment in response to changing conditions detected by the equipment	7 (3 transactions, 1 abort)
6	**Data Collection** Covers the needs of in-process measurements and equipment monitoring	11 (5 transactions, 1 abort)
7	**Process Program Management** Used to manage and transfer equipment-specific process programs	35 (17 transactions, 1 abort)

(Continued)

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Table 1 (Continued)

SECS II STREAM DEFINITIONS

Number	Stream Name and Definition	Specified Functions (#)
8	**Control Program Transfer** Provides method for loading equipment-specific boot and executive programs	5 (2 transactions, 1 abort)
9	**System Errors** Allows for equipment to inform host that received message block cannot be handled, or that time-out on transaction has occurred	8 (7 odd functions, no responses specified, 1 abort)
10	**Terminal Services** Used to pass text messages between equipment operator terminals and the host	6 (5 odd functions, no responses specified, 1 abort)
11	**Host File Services** Provides limited access to host file system	13 (5 transactions, 2 odd functions with no responses, 1 abort)

Source: 1985 SEMI Standards Volume II, E5-85

In the SECS Communication Handbook, published by GW Associates (1985), two situations are identified in which the SECS protocol does not adequately deal with message flooding of the communications link. In the first example, a piece of equipment, designated as the master, may flood the host with alarm messages and, since the host system as the slave always yields to the master, the host system may be unable to send a message to the equipment to shut itself off. Some SECS implementations have added the capability for the host to send a reverse interrupt, which would temporarily shift the master designation from the equipment to the host system.

In the second example of message flooding, the host may inadvertently flood a piece of equipment that lacks sufficient buffer with a heavy flow of messages. If the equipment is too busy to receive additional messages, there is nothing in the protocol that would allow the equipment

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to send a wait-acknowledge response to the host system. The only alternatives available to the equipment result in what appears to be a transmission failure on the part of the equipment. These two examples of message flooding illustrate some insufficiencies of the SECS I protocol that could cause problems in some applications.

SECS II Problems

Semiconductor equipment manufacturers have expressed concerns that the SECS II message set of the protocol is too ambiguous. Several equipment vendors have indicated that it is not clear which stream/function code should be chosen for certain transactions. In addition, many manufacturers feel that the data format (binary, ASCII, floating point, etc.) for given messages should be specified, and not left as an arbitrary decision. The protocol currently provides 14 options for the data format. This level of discretion for the choice of data format can be a problem when an equipment manufacturer is trying to meet the particular specifications of different semiconductor manufacturers. These matters should be taken up with the SEMI Communications Subcommittee, which is responsible for the development and modifications of the SECS protocol as it matures.

THE MAP PROTOCOL

In the early 1980s, General Motors adopted a strategy of automation for its facilities to allow them to compete more effectively against the Japanese automotive industry. General Motors realized that a multivendor approach to automation would require a widely accepted, nonproprietary communication protocol for shop floor communications. The Manufacturing Automation Protocol (MAP) was developed by General Motors in 1982 in response to the need for such a standardized protocol for its manufacturing environment, and MAP has since gained acceptance as an evolving communications standard for general factory automation.

Specifically, MAP is a seven-layer, broadband, token-bus based communication protocol. The seven layers of MAP are based on the International Standards Organization's (ISO) Open Systems Interconnection (OSI) model for network communications. Broadband transmission, specified by the protocol, provides high-speed communications along multiple channels in the single transmission line of the bus network. The bus topology (the physical arrangement of computers within the network) specifies that the communications devices are linked to a single cable throughout the factory floor. Token passing is a type of access method that determines which computer within the network gets to transmit at any given time. The nature of token passing eliminates any possibility for more than one computer to talk along the same channel at the same time. (Broadband transmission, token passing and the bus topology are described in more detail in Appendix A.)

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Equipment Communications

MAP incorporates nationally and internationally accepted standards developed by the National Bureau of Standards (NBS), the Institute of Electrical and Electronic Engineers (IEEE), the International Standards Organization (ISO), and the American National Standards Institute (ANSI). Much interest has been focused on the MAP protocol because it has managed to gain a sizable backing from many large companies in the United States and the international community within a relatively short period of time. Many credit the influence of General Motors for accelerating what is typically a glacial rate for protocol and standards development.

In network communications, there are two separate issues: applications, which are concerned with the preprogrammed functioning of computers, and communications, which provide a method by which computers can talk to one another. The OSI model separates out the applications from communications, and it is the structural details of the latter that are divided into the seven layers of the model. Table 2 illustrates the structure and defines the functions of the seven-layer model.

A block of information transmitted through the MAP network increases in size as it is transferred from the application program down through the communications levels from layer 7 to layer 1. At each level, the appropriate message header information is added to the message block in order to facilitate the subsequent transfer of information to the next level. After the data have been encoded at layer 1 and physically transferred to the next communications device, the information is transferred back up through the layers of the protocol to layer 7 and the application program. The message header information specific to each given layer is stripped off as the block of information passes through that level. In this sense, the system is hierarchical, with each layer providing communication-related services to the layer immediately adjacent to itself. This "nesting of protocols" allows the application to be separate from the communications functions. The effect is that the microcomputer, controller, processing equipment, or robot on the factory floor is responsible only for performing its task, not for communicating its results through the layers of the communication network.

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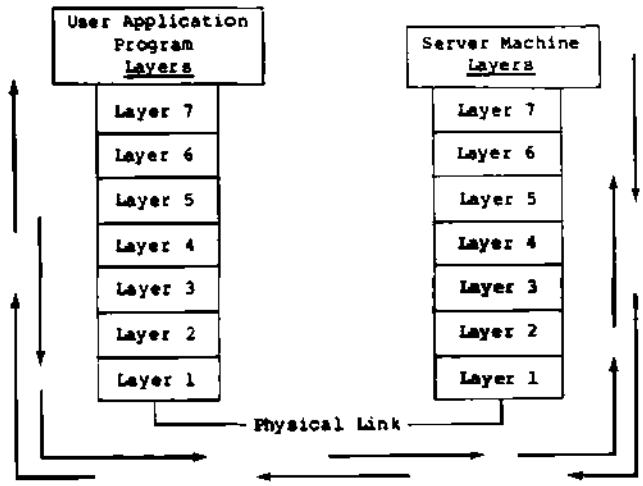
Table 2

THE SEVEN LAYERS OF MAP



Layer 1: **The Physical Layer**
This layer deals with most of the hardware questions involved in networking, such as the actual medium that will be used and the rates at which data will be sent.

Layer 2: **The Data Link Layer**
This layer concerns the composition of the actual "frames" of data that are sent out on the network, as well as the protocols for getting those transmissions onto the network.

Layer 3: **The Network Layer**
This layer sets up the procedure for communications between different networks.

Layer 4: **The Transport Layer**
This layer makes sure a message reaches its destination. It is responsible for assembling a message into frames, then reassembling the frames upon arrival and sending back an acknowledgement.

Layer 5: **The Session Layer**
At this layer, connections are established between stations and logical names are mapped onto physical addresses.

Layer 6: **The Presentation Layer**
This layer converts the message into a form that can be used by the receiving device.

Layer 7: **The Application Layer**
This layer brings network services, such as electronic mail, to the end user.

Source: Intel Corporation
DATAQUEST
April 1986

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Equipment Communications

A useful communications analogy to the OSI reference model is that of sending a letter through the postal system. When a letter (essentially a message or a block of data) is written and mailed, it must go through a series of intermediate steps before it is received at its final destination. The letter is placed in a mailbox, it is collected by a postal carrier, taken to the local post office, collated, sent on to a central post office, and collated once more for final destination. It is then transported (in some sense, analogous to the physical link) by truck, rail, air, or by ship to the receiving central post office. The letter goes through the appropriate sort mechanism, is sent off to the receiving local post office, sorted again, and delivered to the final destination. The communication sequence is independent of the contents of the letter that was written. In an analogous fashion, the seven layers of the OSI reference model facilitate communications in a factory network, but their operations are independent of the contents of the message that is being transmitted.

MAP Users Group

The MAP protocol has been aggressively promoted by General Motors as a viable standard for factory communications between equipment and computers supplied by multiple vendors. Many manufacturers have endorsed the protocol, including Boeing, Ford, General Electric, and Westinghouse. In addition, more than 350 companies have joined a MAP Users Group to promote industry-wide understanding of the protocol and provide a forum for discussion of MAP issues as the protocol matures. The MAP Users Group was established in February 1984 by General Motors with the assistance of such firms as DuPont, Eastman Kodak, and McDonnell Douglas. The Society of Manufacturing Engineers (SME) is responsible for coordinating the administrative activities of the MAP Users Group.

Boeing, in addition to supporting MAP, has developed TOP (Technical Office Protocol), which applies the same seven-layer architecture to office automation that MAP applies to manufacturing on the factory floor. A MAP/TOP Steering Committee is looking at integration of these two protocols that would allow transfer of data between management and manufacturing applications.

The MAP standard has been endorsed by many computer-based system suppliers as well. The list includes Allen-Bradley, Concord Data Systems, Digital Equipment Corporation, Hewlett-Packard, IBM, and Texas Instruments. In the semiconductor industry, Motorola, Intel, Industrial Networking Inc. (a joint venture between General Electric and Ungermann-Bass Inc.), and Concord Data Systems (in conjunction with Gould/AMI Semiconductor) have been very active in the production of chip and board-level products for the MAP standard.

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International Activity

The MAP protocol has also generated interest from European and Japanese manufacturers. In Europe, MAP's counterpart is known as the European Communications Network for Manufacturing Automation (CNMA), a project of the ESPRIT research and development program sponsored by the European community. CNMA also plans to establish protocol capabilities for automated manufacturing and to evaluate and test them in practical applications. Siemens recently joined the CNMA, and will also continue to support MAP activities worldwide. The U.S. MAP Users Group has held discussions with Siemens concerning the compatibility of the MAP standards with the direction of communications development by the CNMA. MAP is also being evaluated in Japan. General Motors delivered a major presentation on the MAP protocol to Japanese manufacturers in the summer of 1985, and one GM official recently commented that he expects Japanese manufacturers to develop MAP products within the next year.

Testing of the MAP Protocol

One of the major obstacles to overcome in the acceptance of the MAP protocol as a de facto standard for manufacturing communications lies in the area of testing. Not only do individual products need to be tested for compliance to the multilayered MAP standard, but the successful interoperability between products from multiple vendors must be established. As with any emerging standard, vendor interpretation of the MAP specifications may still differ, which means that systems can be built that conform to the standard, but may not work with other "standard" products.

A demonstration at last November's Autofact '85 (a factory automation trade show held annually in Detroit) included an exhibit of products from 23 vendors tied together by a MAP system. The demonstration was sponsored by General Motors and Boeing, and vendors participating in the demonstration included Allen-Bradley, AT&T, Concord Data Systems, Digital Equipment Corporation, Gould, Hewlett-Packard, Honeywell, IBM, Industrial Networking Inc. (INI), Intel, Motorola, NCR, Northern Telecom, and Siemens. While the demonstration was hailed as an important step toward successful MAP implementation, it was considered by many as still a far cry from an actual installation of the communications protocol in a manufacturing and assembly line plant.

Work to develop MAP test equipment is under way at several locations, including General Motors, NBS, and the International Technology Institute (ITI), a nonprofit organization in Ann Arbor, Michigan. In September of 1985, the ITI became the first organization to introduce an independent conformance testing service for MAP products. General Motors is

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developing test facilities for MAP products in Canada, England, France, Germany, and Japan. Proposals have also been made for consortiums funded by multiple vendors and users of the MAP protocol to support the development of MAP testing tools. Many, however, concede that current test systems cannot check out MAP adequately for all operating situations that may be encountered in a real network, and that significant tasks lie ahead to determine how to test equipment for MAP compatibility and interoperability in a black-box test environment.

Problems with the MAP Protocol

In addition to a lack of test equipment and procedures for the MAP protocol, several other areas must be addressed before widespread implementation of the standard can be achieved. These include the specification of standards at the upper levels of MAP, development of low-cost interfaces to the network, and development of gateways to allow communication between MAP and non-MAP networks.

The MAP protocol is still in the development stage. Standards have been specified at the lower levels of the seven-layer model; however, standard specification at the upper levels has not been completed. The IEEE 802.4 standard, which is familiar to most people following MAP development, is employed only at layers 1 and 2, the physical and data link levels. General Motors officials claim that all of the standards should be in place by the end of 1988.

A network interface connects a node or network station to the broadband backbone of the MAP network. Between an equipment controller and the network itself, there will always be a "box," the network interface. It provides conversion of the node's protocol to the protocol used by the network and controls when the node can transmit. The interface could be, for example, a modem or an intelligent card. Currently, the costs for node/network interfaces are still high, and the lack of low-cost interfaces impedes the development of MAP-based communications networks. The continuing development of chip and board-level products to interpret the different levels of MAP will replace existing software programs and reduce costs for network interfaces.

A gateway provides interconnect capability from a MAP-based network to another digital communications system. It not only serves as the interface between two networks, but also provides protocol conversion between the two communications systems. Many facilities have local area networks such as DECNet or Ethernet in place. These systems would still be able to communicate with a MAP-based system through the gateway. For example, a group of CAD stations might communicate through an Ethernet

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system. When it comes time to send data to a host system, one computer in the cluster would be responsible for sending the information through a transfer device, or gateway, into the larger MAP network. Implementation of the MAP protocol in a semiconductor manufacturing environment might well employ a gateway to provide protocol conversion between SECS used at the lower levels of the communications network and a MAP-based system operating at the upper levels.

Finally, perhaps MAP's biggest problem is that the protocol is not simple, and thus there is a large degree of confusion as to how to design MAP-compatible products and how to implement a MAP-based communications network. Education will need to continue at all levels to ensure that MAP will continue to gain acceptance as a general communications protocol for factory automation.

SECS AND MAP IN THE SEMICONDUCTOR INDUSTRY

There has been some discussion that SECS might eventually be replaced by MAP as the communications protocol for semiconductor automated facilities. Some manufacturers have expressed doubt whether SECS has sufficient capability to provide the requirements of interactive communications in a large communications network. These manufacturers' complaints include that SECS is too slow, that it is based on only one standard (RS-232), and that it requires a point-to-point configuration that has logistic and economic disadvantages when the automation environment grows beyond a certain size. The question has been raised whether MAP may be a suitable substitute for SECS or if complementary components of the two protocols might be brought together for implementation in the semiconductor industry. Table 3 summarizes the advantages of these two protocols that would provide complementary functions in possible future applications in the semiconductor manufacturing environment.

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Table 3

MAP AND SECS COMPARISON

MAP	SECS
Based on ISO/OSI model, which allows different types of network interconnections; uses ISO, NBS, and IEEE standards, all large standards organizations	Has an existing organization (SEMI) that focuses on specific semiconductor industry needs
Designed for general manufacturing environment; has the backing of large organizations	Has a good message set, specifically designed for semiconductor manufacturing environments
Thousands of man-hours have been invested; many MAP-related products have been developed	Many working implementations of the protocol exist
A real network (broadband, token-passing bus), not just a point-to-point configuration	

Source: DATAQUEST
May 1986

SEMI's Communications Subcommittee established the Network Implementation Task Force (NITF) in 1985 to develop network standards for the semiconductor industry. In particular, the NITF has decided to evaluate the potential for implementing the MAP protocol in a semiconductor manufacturing environment. Figure 2 illustrates the point-to-point arrangement of computers and equipment specified by the SECS protocol, and presents for comparison the topology that DATAQUEST expects will be employed in a SECS/MAP environment. This scenario retains the SECS protocol for communications between equipment and cell-level and node-level computers. Upper-level communications between host and node computers would follow the MAP specifications for a broadband, token-bus network that would provide high-speed communications along the multichannel transmission line of the bus. The SECS II message set would be maintained throughout the network environment because of its specificity to semiconductor manufacturing. MAP's message set is currently free-form in design and does not focus on the specific message needs of any given industry.

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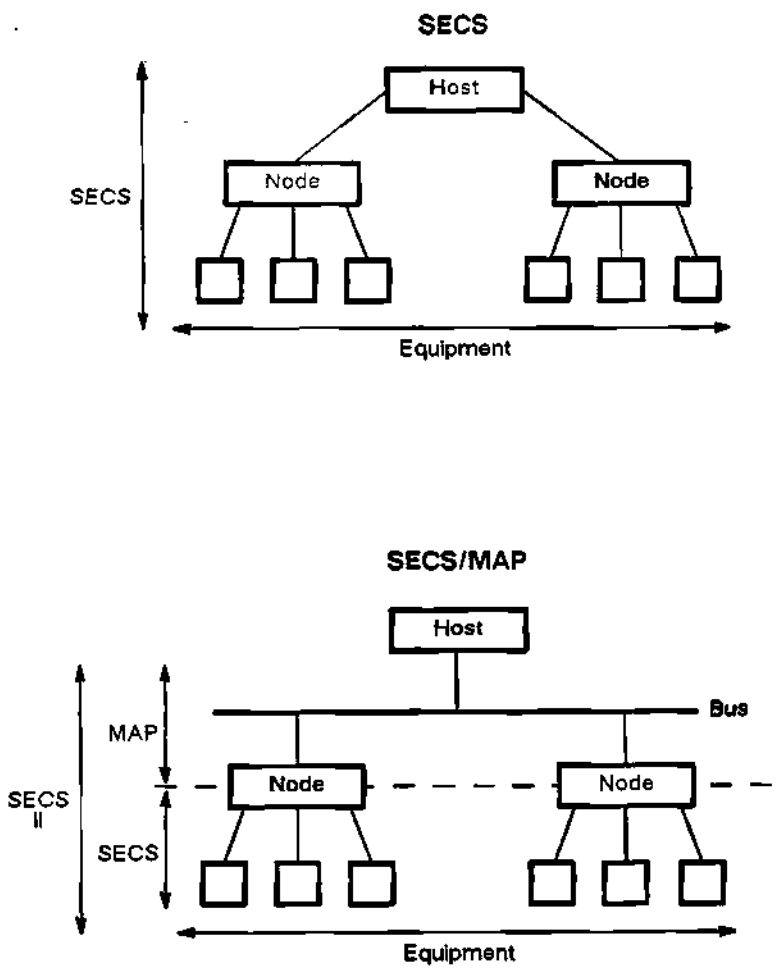
CIM manufacturers, such as Consilium and PROMIS Systems (a wholly owned subsidiary of I.P. Sharp), would be responsible for providing gateways between the MAP and SECS protocols. The gateway would likely reside at the level of the node computer to act as a translator between communications on the bus network of MAP and the point-to-point topology of semiconductor processing equipment that communicates with SECS. Equipment manufacturers most likely will not be responsible for linking their equipment directly to the MAP token-bus network, but will continue protocol implementation as specified in the SEMI SECS document.

Figure 2

SECS AND SECS/MAP TOPOLOGIES



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May 1986

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However, equipment vendors cannot afford to entirely ignore the design and development of the MAP protocol and its associated chip and board-level products. The lack of understanding and education in automation issues, including protocol development, can result in substantial confusion, misdirected activities, and misspent resources for all concerned in the automation effort. MAP is a particularly complex and involved protocol, and DATAQUEST strongly encourages equipment manufacturers to either start now or continue current efforts in monitoring MAP development.

VENDOR IMPLEMENTATION OF THE SECS PROTOCOL

Equipment Survey Overview

DATAQUEST recently conducted a survey of semiconductor equipment manufacturers in order to evaluate the level of vendor commitment to the SECS protocol. Twenty-six equipment manufacturers representing eight general types of front-end processing equipment participated in the study in which a total of 42 models of equipment were discussed. The eight categories of front-end processing equipment include chemical vapor deposition (CVD) reactors, diffusion furnaces (including annealers) epitaxial reactors, dry etch equipment, ion implanters, lithography, sputtering, and automatic photoresist processing (track) equipment. The 26 survey participants combined represented 50 percent overall market share of the 1984 worldwide semiconductor front-end processing equipment market. The combined market share of survey participants in each equipment category is presented in Table 4. For example, the five lithography companies surveyed represented 75 percent of the 1984 lithography market.

Table 4

SURVEY PARTICIPANTS' 1984 WORLDWIDE MARKET SHARE BY EQUIPMENT CATEGORY

Equipment Category	Participants' Sum Market Share
CVD	14%
Diffusion/Anneal	55%
Dry Etch	62%
Epitaxy	58%
Ion Implantation	79%
Lithography	75%
Sputtering	54%
Track	61%

Source: DATAQUEST May 1986

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Equipment Communications

Discussions with equipment vendors were undertaken with the condition that information provided would not be reported by company; instead the information would be used to establish an industry perspective on equipment-level implementation of the SECS protocol and related automation issues. Participants in the study are identified in Table 5. The number beneath each equipment category indicates the number of equipment models that were discussed in the survey. In some instances, several models of equipment from the same vendor have been included. Vendor responses were for existing equipment models that are considered to be the most advanced, as well as for next-generation equipment currently under development.

Table 5

EQUIPMENT SURVEY PARTICIPANTS

	CVD	Diffusion/ Anneal	Dry Etch	Epitaxy	Ion Implant	Lithography	Sputtering	Track
Models of Equipment	4	6	9	3	3	6	4	7
Companies								
Advanced Crystal Sciences, Inc.		X						
ASM America		X						
Anicon Incorporated	X							
Applied Materials, Inc.			X	X	X			
BTU Engineering Corporation		X						
Drytek Inc.			X					
Eaton Corporation					X	X		X
GCA Corporation			X			X		X
Gemini Research				X				
Genus Incorporated	X							
Lam Research Corporation			X					X
Machine Technology, Inc.							X	
Materials Research Corporation			X			X		
Nikon Precision, Inc.						X	X	
Perkin-Elmer			X					
Semiconductor Systems, Incorporated								X
Silicon Valley Group, Inc.	X							X
Solitec, Inc.								X
Tegal Corporation			X					
Temescal							X	
Thermco Systems, Inc.		X						
Tylan Corporation		X						
Ultratech Stepper						X		
Varian Associates	X	X			X		X	
Veeco Instruments Inc.								X
Zylin Corporation			X					

Note: In some cases, more than one model of equipment from the same vendor has been included in a given equipment category.

Source: DATAQUEST
April 1986

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SECS II Implementation by Equipment Vendors

Of the 42 equipment models that were surveyed, 39 models have SECS capability. Of those 39 equipment models, 28 models already have an existing SECS protocol implementation, while 11 models have their SECS implementation currently under development such that a software release will be available in 1986. Table 6 summarizes the vendor response on SECS implementation by equipment category.

Table 6

IMPLEMENTATION OF THE SECS PROTOCOL

Equipment Category	Yes	UD	No
CVD	2	2	0
Diffusion/Anneal	5	1	0
Dry Etch	6	3	0
Epitaxy	1	1	1
Ion Implantation	2	1	0
Lithography	3	2	1
Sputtering	3	1	0
Track	6	0	1
Total	28	11	3
Percent Response	67%	26%	7%

Source: DATAQUEST
April 1986

In order to quantify the level of vendor implementation of the SECS protocol, equipment manufacturers were requested to provide specific information on their SECS II message set, in particular the total number of SECS II messages and the number of messages per stream, whether specified or custom. Message detail was provided by equipment manufacturers for 27 of the 39 models of equipment. Transactions between equipment and host typically consist of a query and a response, each of which has a different function code designation in a given stream. Survey respondents were requested to include the total number of stream/function codes (messages) that the equipment is responsible for sending to or receiving from a host system. Custom messages are included in the message count. Vendors were also requested to indicate whether they had chosen to include any of the abort transactions (function 0) provided in each stream.

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Total Message Count

The SECS II protocol provides a general message set for transactions between processing equipment and a host computer system in an automated semiconductor fabrication environment. However, as one equipment vendor was quick to point out, "No two people do SECS the same way." Therefore, while the SECS protocol does provide a standardized structure for communications, a great deal of variety exists in the interpretation and number of messages a vendor has chosen to specify for his equipment.

Each point in Figure 3 represents the total number of SECS II messages from a particular model of equipment (total 27 models of equipment). For example, the three models of lithography equipment have message sets consisting of 31, 36, and 37 function codes, respectively. The number of messages in Figure 3 represents those function codes (both specified and custom) that equipment vendors have implemented in the eleven standard streams of the protocol. (Two vendors have developed messages for custom streams; these messages are not included in Figure 3.) Not only is there a wide range in the number of messages between the various categories (18 to 214), but also within a given equipment category. (Sputtering equipment, epitaxial, and CVD reactors have been classified in a general deposition equipment category in this figure to maintain equipment vendor anonymity.)

The average number of total messages implemented by equipment vendors in Figure 3 is 38 (excluding the one diffusion entry of 214 messages). The absolute number of messages implemented by a given equipment manufacturer does not necessarily reflect the level of protocol software sophistication for the equipment. It is possible that some equipment manufacturers have chosen to implement a very efficient, compact message set while others have included a large number of special-function custom messages to enhance the protocol's capabilities.

What is most important is not the absolute number of messages that have been chosen but rather that the implemented message set includes all of the necessary functional components of the protocol such as recipe management (uploading and downloading), process and equipment status, and alarm information. Two factors--specific message code implementation and functionality of the message set--could well be represented by a unique set of stream/function codes, which, if detailed in the exact same manner by all equipment manufacturers, would ensure a standardized implementation across the board for all types of equipment. However, in reality vendor interpretation and implementation of the SECS II messages can vary considerably, and yet still meet the necessary requirements for functionality of the message set.

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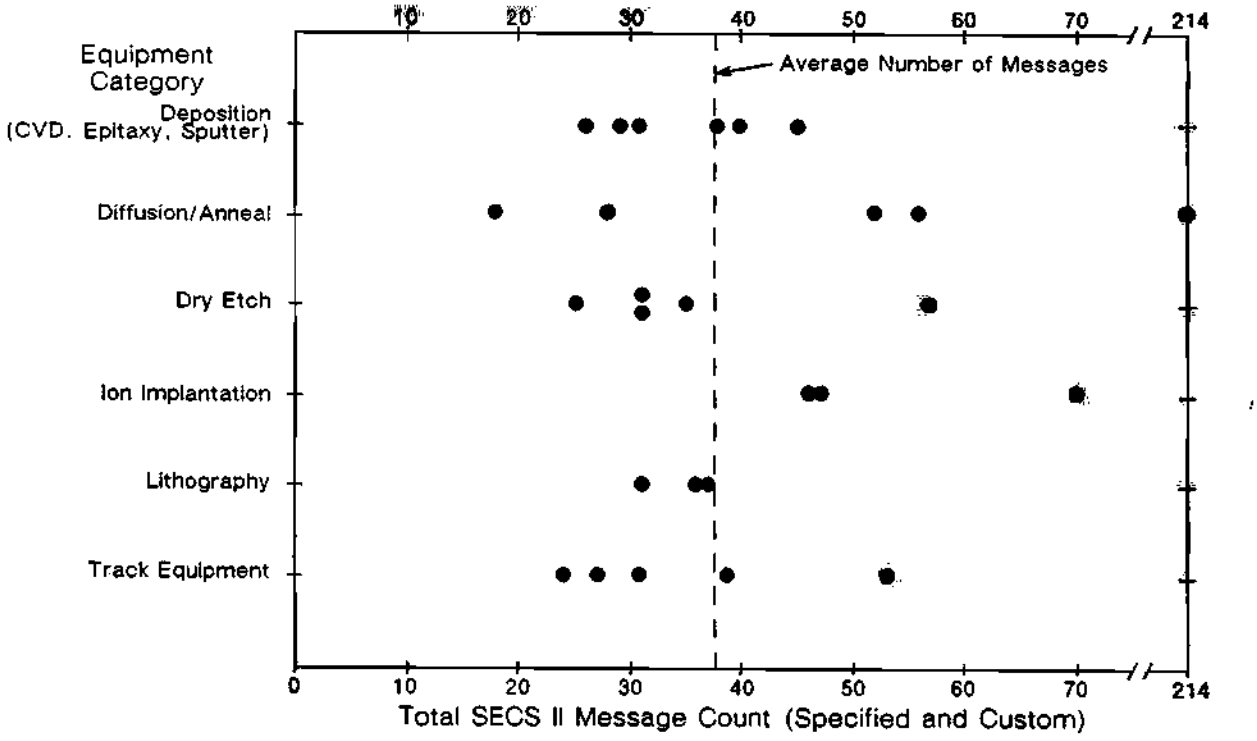
Figure 3

TOTAL SECS II MESSAGE COUNT--SPECIFIED AND CUSTOM
BY EQUIPMENT CATEGORY



Source: DATAQUEST
MAY 1986

Upon the completion of their SECS protocol, equipment manufacturers must be able to provide semiconductor manufacturers with a document that contains details of their SECS II message set. Semiconductor manufacturers such as Intel, Texas Instruments (TI), and Thomson Components-Mostek Corporation (TCMC), have taken the first step in equipment-level automation and have provided equipment manufacturers with minimum SECS II message set requirements. These manufacturers feel that their minimum message sets include the essential functionality of the SECS II protocol. In addition, they are attempting to ensure standardization throughout their own facilities by providing clear guidelines to the equipment industry. Other semiconductor manufacturers have chosen to specify the broad functional components of the protocol,

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which they feel are necessary for equipment/host communication in an automated facility. The details of the protocol implementation are left to their equipment vendors and the CIM manufacturer responsible for coordinating their automation efforts.

Specified Message Count

Figure 4 compares the number of protocol-specified messages implemented by equipment manufacturers with the number of messages specified by Intel and Texas Instruments in their minimum SECS message sets. The information in Figure 4 is essentially the same as that contained in Figure 3, except that custom messages have been removed from the total message count for 14 of the 27 equipment models that include these equipment manufacturer-defined functions. On the basis of specified message count, the average number of messages implemented for the 27 equipment models is 34.

Intel's SECS II specification identifies 42 messages from 7 different streams as the minimum set necessary for implementation on process and analytical equipment. Only 6 equipment models of the 27 represented in Figure 4 can meet Intel specifications based on specified message count alone. Similar to Intel, TI also has a set of specifications that defines a minimum set of messages for equipment vendor implementation. In TI's case, 51 messages in 9 streams have been identified. Only 3 of the 27 equipment models in Figure 4 have more than 51 specified messages in their SECS II message set. In addition, only 14 of the 27 survey respondents that provided detailed information on their SECS II message sets included any abort messages in their protocol implementation. Both Intel and Texas Instruments require the abort message for every stream in which messages have been specified. On the basis of the information presented in Figure 4, the majority of equipment manufacturers will have to make substantial additions to their present message sets in order to satisfy Intel and Texas Instruments requirements.

Intel and Texas Instruments recognize that minimum SECS II requirements from semiconductor manufacturers should be focused on specific categories of equipment rather than on a general message set for all wafer processing equipment. Both manufacturers are willing to negotiate their minimum message set requirements with equipment vendors since in some cases, the messages may not be appropriate for a given type of equipment. However, these semiconductor manufacturers will not negotiate when an equipment vendor has chosen to implement his own custom messages when existing messages in the protocol would have sufficed. The generic minimum message subsets from Intel and TI are meant as a guideline for equipment protocol development to ensure that equipment purchased for Intel and TI facilities has sufficient communications capability to operate in an automated environment. Clearly, if Intel's and Texas Instruments' message sets are indicative of the minimum requirements for general SECS II implementation in the industry, the

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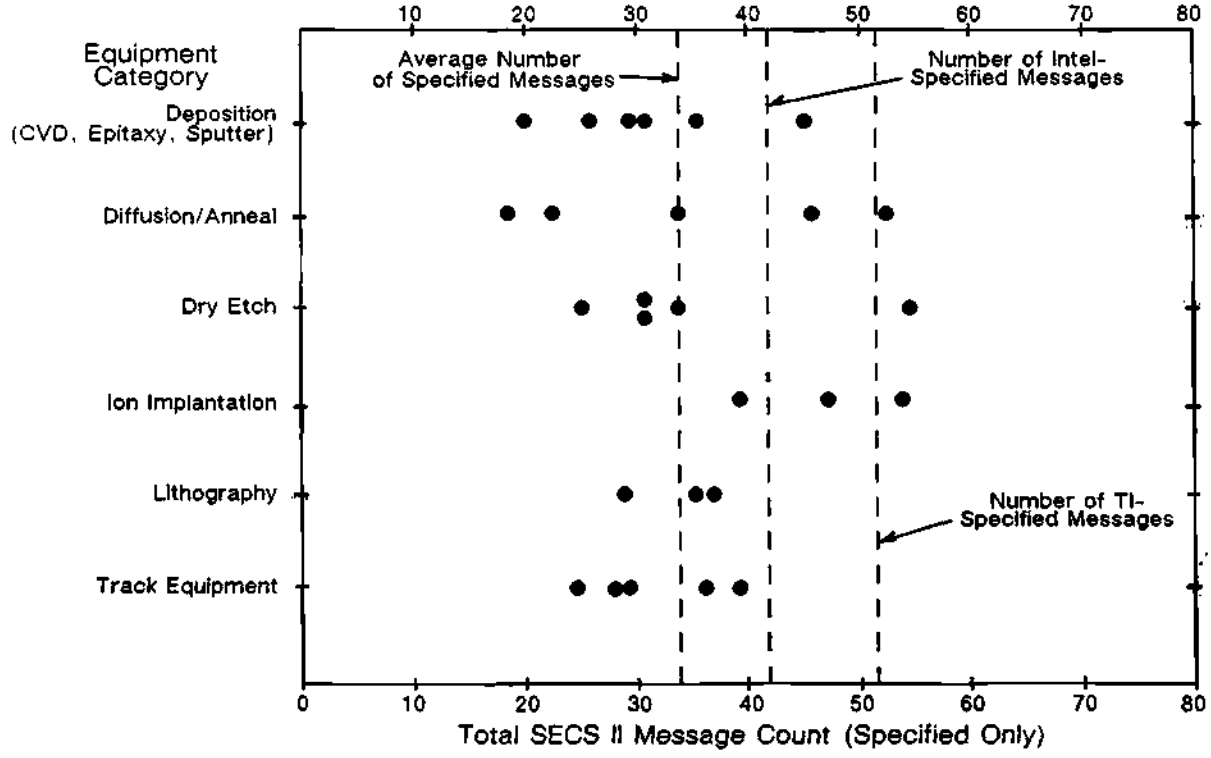
majority of equipment vendors face major customization of their SECS protocol at some stage when a semiconductor manufacturer decides to automate its facilities. DATAQUEST believes that this is an extremely important finding to come out of this survey.

Figure 4

TOTAL SECS II MESSAGE COUNT--SPECIFIED ONLY
BY EQUIPMENT CATEGORY



Source: DATAQUEST
MAY 1986

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Message Count per Stream

Table 7 contains information on the average number and range of function codes implemented per stream for the 27 equipment models represented in Figure 3. Equipment manufacturers choose the set of messages that they feel are most appropriate for implementation on their equipment. The first column in Table 7 indicates the number of equipment models for which any messages (whether specified or custom) have been implemented from the 11 streams. The second column identifies the total number of function codes per stream that have been specified to date in the SECS II protocol document (from Table 1). The average and range in the number of function codes that equipment manufacturers have chosen to implement is presented in columns three and four of Table 7.

Table 7

FUNCTION CODE COUNTS PER STREAM

	Equipment Models with Function Codes in the Stream	Total Number of Function Codes Specified in Protocol	Average Number of Function Codes Implemented	Range in Number of Function Codes
Stream 1				
Specified	27	11	4	2-9
Custom	6	0	3	1-7
Stream 2				
Specified	27	29	7	2-20
Custom	8	0	7	1-34
Stream 3				
Specified	7	11	2	1-5
Custom	4	0	5	1-8
Stream 4				
Specified	7	9	6	1-9
Custom	6	0	12	2-36
Stream 5				
Specified	25	7	3	1-6
Custom	3	0	3	1-6
Stream 6				
Specified	16	11	4	1-10
Custom	4	0	3	1-10

(Continued)

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Table 7 (Continued)

FUNCTION CODE COUNTS PER STREAM

	Equipment Models with Function Codes in the Stream	Total Number of Function Codes Specified in Protocol	Average Number of Function Codes Implemented	Range in Number of Function Codes
Stream 7				
Specified	25	35	8	4-15
Custom	5	0	16	1-54
Stream 8				
Specified	0	5	0	0
Custom	1	0	30	30
Stream 9				
Specified	27	8	6	1-8
Custom	2	0	2	1-3
Stream 10				
Specified	10	6	3	1-5*
Custom	0	0	0	0
Stream 11				
Specified	1	13	5	5
Custom	0	0	0	0

*Note: One manufacturer has chosen to include an additional 7 specified function codes in Stream 10 that have yet to be accepted by the SEMI Communications Subcommittee for incorporation into the SECS II message set. With the inclusion of those additional 7 responses, the average number of messages specified in Stream 10 is 4, with a range of 1 to 11.

Source: DATAQUEST
May 1986

Specific stream/function message detail is regarded by many equipment manufacturers as proprietary information, so only the number of function codes implemented are included in Table 7. The SECS protocol provides equipment vendors with the option of implementing custom streams (S64-S127) as well as custom function codes (F64-F255). Two of the 27 message sets that were received by DATAQUEST in the survey include custom streams and 14 of the 27 message sets contain custom function codes. Table 7 does not contain custom stream information, only those function code counts for the 11 specified streams of the SECS II protocol.

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In Table 7, the streams that show the largest degree of protocol activity are Streams 1 (Equipment Status), 2 (Equipment Control and Diagnostics), 5 (Exception Reporting), 7 (Process Program Management), and 9 (System Errors). At this time, only 7 equipment models in the survey have specified functions implemented in Stream 4, which defines messages associated with material control and provides for equipment/robotic interactions. No equipment models include specified functions from Stream 8, which is responsible for loading equipment-specific boot and executive programs. (For some models and types of equipment, this type of application is not possible.)

Again, it is instructive to compare equipment vendor activity in a given stream with the specifications that Intel and Texas Instruments have defined as a minimum message set for SECS II protocol implementation. Table 8 compares the average number of specified function codes per stream implemented by equipment vendors (from Table 7) with the number of messages in the 10 streams that Intel and TI recommend for a minimum message set. Both Intel and TI require that the abort transaction (F0) be included in every stream in which messages have been specified, therefore, these messages are accounted for in Table 8. As mentioned previously, of the equipment vendors that provided protocol information to DATAQUEST, only 14 of 27 responses have chosen to include any abort transactions in their protocol implementation.

Table 8

FUNCTION CODE COUNTS PER STREAM FOR VENDOR IMPLEMENTATION, INTEL, AND TI REQUIREMENTS

	Equipment Models with Function Codes in the Stream	Total Number of Function Codes Specified in Protocol	Average Number of Function Codes Implemented	Intel Number of Function Codes Specified	TI Number of Function Codes Specified
Stream 1 Specified	27	11	4	3	7
Stream 2 Specified	27	29	7	11	7
Stream 3 Specified	7	11	2	4	7

(Continued)

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Table 8 (Continued)

FUNCTION CODE COUNTS PER STREAM FOR
VENDOR IMPLEMENTATION, INTEL, AND TI REQUIREMENTS

	Equipment Models with Function Codes in the Stream	Total Number of Function Codes Specified in Protocol	Average Number of Function Codes Implemented	Intel Number of Function Codes Specified	TI Number of Function Codes Specified
Stream 4 Specified	7	9	6	*	9
Stream 5 Specified	25	7	3	7	3
Stream 6 Specified	16	11	4	3	5
Stream 7 Specified	25	35	8	*	5
Stream 8 Specified	0	5	0	5	*
Stream 9 Specified	27	8	6	8	5
Stream 10 Specified	10	6	3	5	3
Stream 11 Specified	1	13	5	*	*

*No specifications at this time.

Source: Intel Corporation
Texas Instruments
DATAQUEST
May 1986

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While the specific function codes that Intel and Texas Instruments have identified in their minimum subsets are not compared directly with the vendors' choice of messages, it is only in Streams 1 and 6 that equipment vendors have exceeded the number of minimum messages specified by Intel, and in Streams 2, 5, 6, 9, and 10 that equipment vendors have equaled or exceeded the message count specified by Texas Instruments.

Table 8 also illustrates the degree of variability between the message sets of the two semiconductor manufacturers. In the case of Stream 8, Intel specifies that all five function codes be implemented, when applicable, while Texas Instruments has chosen not to include any messages from Stream 8. On the other hand, Texas Instruments has identified messages from Streams 3, 4, and 7, where Intel has no specifications at this time. If an equipment manufacturer chose to comply with the number of messages that would satisfy both Intel and TI specifications (based on the overlap of the stream/function message set between TI and Intel), a total of 73 specified messages from the SECS II protocol would be required. Not a single equipment model of the 27 that provided detailed protocol information in the DATAQUEST survey can meet both Intel and TI's minimum message set specifications on the basis of message count alone.

As mentioned previously, both TI and Intel recognize that protocol message requirements really should be directed toward specific equipment categories, and both are willing to negotiate with equipment manufacturers over messages that are not necessarily appropriate for a given type of processing equipment. However, for a fully automated manufacturing facility, semiconductor manufacturers probably will require equipment communications capability to exceed those specifications already identified by Intel and Texas Instruments.

Additional Specifications

Up to this point, discussion in this analysis has centered only on the number of function codes that have been specified in each stream. For a more accurate comparison of protocol specifications between equipment and semiconductor manufacturers, the actual function code numbers used to identify the messages and the data structure also must be identified. The data structure includes the data element name, the format, and the length (in bytes) of the data. The SECS II protocol does provide data element names but data format, of which there are 14 options in the protocol, and data length are variable. Therefore, even if semiconductor and equipment manufacturers specify the identical stream/function codes, it is still possible that the message sets are not entirely compatible due to differences in the data format and length. Equipment and semiconductor manufacturers must come to a common consensus for data structure as well as protocol specifications in order to achieve some level of standardization in equipment communication throughout the industry.

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Custom Messages

The SECS protocol provides equipment vendors with the option of implementing custom streams (S64-S127) and custom function codes (F64-F255). The SEMI Communications Subcommittee recognizes that there will be user needs beyond the specific definitions given in the protocol because of equipment-specific applications. In addition, the protocol reserves stream and function codes for future messages that will be adopted by the Communications Subcommittee as the protocol matures. One vendor that supplied protocol information to DATAQUEST included an additional 7 messages in Stream 10 that as yet have not been adopted by the committee. Two of the 27 message sets in the survey include custom streams and 14 of the 27 message sets contain custom function codes. Table 9 summarizes custom message implementation by equipment category for the 27 message sets.

Table 9

CUSTOM MESSAGE IMPLEMENTATION BY EQUIPMENT CATEGORY

Category	Yes	No
CVD	1	2
Diffusion/Anneal	3	2
Dry Etch	3	2
Epitaxy	1	0
Ion Implantation	2	1
Lithography	2	1
Sputtering	0	2
Track	2	3
Total	14	13

Source: DATAQUEST
April 1986

From Table 9, it is clear that equipment manufacturers are implementing custom messages in all categories of front-end processing equipment (except sputtering, for which only a limited sampling size was available). While custom messages provide extended communication capability for equipment-specific applications, their presence also demands that semiconductor manufacturers and equipment vendors have a

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clear, consistent understanding of the interpretation of these messages. Some semiconductor manufacturers will not accept processing equipment utilizing a custom message set without conducting substantial negotiations. In particular, TI and Intel will not accept custom messages when specified messages within the SECS II message set would have sufficed. In addition, the development of an equipment-specific interface by a CIM manufacturer requires additional time, resources, and cost for those equipment models that implement a large custom message set. Thus, equipment manufacturers that choose to include custom messages in their protocol should carefully evaluate semiconductor and CIM manufacturer response to their message set in order to avoid unnecessary costs or delays in protocol acceptance and interface development required before the equipment can be integrated into an automated environment.

Testing of the SECS Protocol

It is very important that an equipment vendor's implementation of the SECS protocol is tested, not only to ensure compliance with protocol specifications, but also to provide semiconductor manufacturers with the appropriate support documentation for the equipment. Several products are available that allow a semiconductor equipment manufacturer to test the implementation of his protocol. These systems include a SECS Protocol Emulator available from Texas Instruments, and SECSIM, a SECS Simulator from GW Associates. Both systems provide host and equipment emulation, and can send valid or invalid messages to monitor host/equipment responses. Both systems are PC-based for flexibility and low cost, and allow field engineers to provide trouble-shooting capability at the time of equipment installation within the communications network. Equipment protocol testing with CIM manufacturers is also possible with a CIM-based SECS emulator package or through a telephone hookup. CIM manufacturers encourage equipment manufacturers to have the proper dial-out and dial-in modems available at their facilities for the initial testing phase of their SECS protocol.

In addition, some equipment manufacturers have chosen to develop host emulator software packages. For example, Silicon Valley Group (SVG) provides an IBM XT-compatible software package for communication and protocol testing of its Host Computer Interface Unit, which is a local controller that coordinates operations and process control for SVG's track equipment. The software package allows semiconductor manufacturers to install and test the communication capabilities of the track equipment without requiring a fully operational host system in the fab.

The surveyed equipment vendors that have implemented or are currently developing the SECS protocol for their equipment were asked to identify the companies with whom they have tested their protocol. These companies

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include the major CIM manufacturers such as Consilium, Hewlett-Packard, PROMIS Systems, and Sentry/Schlumberger. (Note: Hewlett-Packard and Sentry/Schlumberger have recently chosen to exit the computer-integrated manufacturing market. HP is still active in the custom software market in Japan and the Far East, but chose not to fund major software rewrites for its CIM systems operational in Europe and the United States. Sentry/Schlumberger was not able to successfully commercially market their system.) Responses from equipment vendors also included testing of the protocol at beta sites with semiconductor manufacturers, as well as with a SECS emulator and with an in-house testing program.

Typically, a test of a SECS protocol implementation would include a direct or remote hookup to a host (or host-emulator) system that is capable of generating and responding to the basic message transmission and reception. Table 10 summarizes the vendor responses for testing of SECS protocol implementation. For the 39 equipment models in the survey for which a SECS protocol has been implemented or is being developed, some type of protocol testing program has been undertaken for 27 models of equipment. In several cases, multiple responses were given for a single equipment model and are included in Table 10.

Table 10

SECS PROTOCOL TEST PARTNERS

Test Source	Responses	Percent Responses
Consilium	14	30%
I.P. Sharp	9	19
Hewlett-Packard	6	13
Sentry/Schlumberger	2	4
Beta Site Test	11	23
In-House Test	3	6
SECS Emulator	2	4
Total	47	99%

Source: DATAQUEST
April 1986

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Equipment Communications

EQUIPMENT-SPECIFIC INTERFACES

CIM manufacturers are responsible for the development of software equipment interfaces that allow a vendor's equipment to communicate with other computers linked by the factory automation network. The equipment-specific interface is dependent on the equipment vendor's interpretation of the SECS protocol. If the protocol changes, then the equipment interface must also change to reflect the software update. When an equipment manufacturer has to customize his SECS protocol for different semiconductor manufacturers, any equipment interfaces that have been developed by CIM manufacturers for that equipment model will also have to be modified. While the SECS II message sets can vary considerably from vendor to vendor, there is no fundamental problem in developing an equipment interface as long as the functional components of the protocol are present, such as recipe management, process and equipment status, and alarm information. However, the time and cost for equipment interface development could be reduced if vendor implementation of the protocol were not so diverse. The choice for interface development by a CIM manufacturer is driven by semiconductor customer needs.

Table 11 summarizes the total number of different types of equipment interfaces, by equipment category, that have been developed by Consilium, Hewlett-Packard, and PROMIS Systems. These three companies are the major CIM manufacturers that currently supply or have supplied software systems to the semiconductor industry. For every model of equipment, even within the same general category such as diffusion equipment, a unique interface must be developed by each of the different CIM manufacturers. The interface acts as an interpreter between the equipment and a given CIM software system to ensure that the host understands the set of equipment messages (both specified and custom) that are generated.

In several cases, equipment interfaces for the same model of equipment have been developed by the different CIM manufacturers. Table 11 includes multiple counting when several CIM manufacturers have developed an interface for the same model of equipment. Table 11 does not contain the total number of equipment interfaces that are operating on equipment in the installed base; rather, the numbers reflect only the number of different equipment models for which an interface has been developed. The number of interfaces currently under development for other models of equipment are indicated in parentheses. Metrology tools, parametric testers, and AGVs (automatic guided vehicles for material transport) have been included in Table 11.

The number of equipment interfaces presented in Table 11 focuses on equipment supplied by U.S. manufacturers. Hewlett-Packard has also developed equipment interfaces for more than 20 models of equipment for Japanese customers across the full spectrum of front-end processing equipment.

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Table 11

EQUIPMENT-SPECIFIC INTERFACES
BY EQUIPMENT CATEGORY

Equipment Category	Number of Interfaces	
Diffusion	9	(1)
Dry Etch	1	(2)
Epitaxy	1	(1)
Ion Implantation	3	(2)
Lithography	0	(2)
Sputtering	1	
Wafer Clean Station	1	
Metrology	17	
Parametric	2	
AGV	2	(1)
Total	37	(9)

Note: Numbers in parentheses indicate the number of interfaces currently under development in a given equipment category.

Source: DATAQUEST
April 1986

Cameo Systems and CTX International offer equipment interfaces that focus on metrology and test equipment. Isitec Corporation offers equipment interfaces for wafer fabrication equipment, metrology tools, test, and assembly equipment for which no SECS protocol has been developed. Many semiconductor manufacturers have chosen to implement automation in their facilities in the front-end test and measurement areas first because of the data-intensive nature of the equipment. Short-term payback is achieved through efficient data collection, reduction, analysis, and archiving, which can be greatly simplified with the installation and implementation of a CIM automation package.

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OPERATOR INTERFACE

While the previous discussion has focused on the protocol issues of equipment automation, it is also important to evaluate what level of operator interface and interaction is still required for equipment operation in today's version of an automated manufacturing environment. As part of the survey, equipment manufacturers were asked to identify the current level of operator interactions with processing equipment in three areas: operator input capability at the equipment, process parameter setup once the recipe has been received, and process initiation.

Operator Input Capability at the Equipment

Lot tracking is an important component of an integrated manufacturing system. DATAQUEST asked equipment vendors to indicate whether their equipment currently can accept the input of a lot identification number from an operator at the equipment. In an automated facility, there are several scenarios for entering the lot ID number into the host system and for subsequent verification of lot arrival and departure from the various processing stages. These include bar code readers as well as direct operator input at a keyboard that is part of processing equipment or at a workstation within the manufacturing cell. In addition, there is still the alternative of the traditional lot traveler that accompanies each lot through the processing sequence.

Several semiconductor manufacturers have indicated that they would like to see processing equipment capable of transferring lot ID information to the host system for verification rather than have the full burden fall on the host system to inform the equipment which lot should be arriving next for processing. This verification of lot ID at the equipment before and after processing would minimize potentially costly mistakes that might arise during the early stages of implementing a CIM system on the shop floor.

Table 12 summarizes the vendor responses categorized into four areas: equipment can accept lot ID from operator input and host download (via a SECS link); equipment can accept ID from host download only; equipment can accept ID from operator only; and equipment has no lot ID input capability. In the survey, for 18 of 42 equipment models, the equipment can receive lot ID input from the operator as well as from the host system, while an additional 21 models of equipment surveyed can receive lot ID information only from a host system. In one survey response, the equipment can accept a lot ID only from operator input at the equipment, and for two models of equipment, there is no access to the lot identification.

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Table 12

LOT ID INPUT AT THE EQUIPMENT

Equipment Category	Operator Input/ Host Download	Host Download	Operator Input	No Input
CVD	1	3	0	0
Diffusion/Anneal	3	3	0	0
Dry Etch	2	7	0	0
Epitaxy	1	1	0	1
Ion Implantation	3	0	0	0
Lithography	4	1	1	0
Sputtering	2	2	0	0
Track	2	4	0	1
Total	18	21	1	2
Percent Responses	43%	50%	2%	5%

Source: DATAQUEST
April 1986

The methods of current operator input include keyboard and terminal that are part of the equipment (16 equipment models), alphanumeric touch screen (2 equipment models), and a light pen at an alphanumeric screen on the equipment (1 equipment model). In three cases, survey respondents indicated that bar code readers were being considered for next-generation equipment.

Less than half of the equipment models that were surveyed have the capability for operator input of a lot ID. This means that for some equipment that might be installed in an island of automation on the factory floor, some method of alternative lot ID verification would need to be established. In the absence of operators, advanced automated manufacturing fabs will include material logging systems such as automatic bar code readers directly at the equipment or at adjacent workstations under robotic control. As an interim measure in the transition to a "peopleless" fab, operator workstations and terminals throughout the fab may be logical points for material logging. DATAQUEST believes that processing equipment that provides operator input capability directly at the equipment offers semiconductor manufacturers a flexible alternative for lot ID verification. Processing equipment that provides such features and thus eases the transition to automation will receive special attention from semiconductor manufacturers.

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Parameter Setup

An important and necessary step in an automated processing environment is the ability of equipment to accept a recipe download from the host system, to institute an automatic parameter setup, and to initiate the processing sequence. Table 13 addresses the issue of parameter setup that occurs after a recipe download or operator input has been received by the equipment, and includes setting and verifying parameters such as temperature, pressure set points, and alignment settings. Of the 42 models of equipment surveyed, 39 have the capability of accepting a recipe download via the SECS protocol. For the other 3 equipment models for which no SECS protocol has yet been developed, the only methods for current recipe input are either through direct operator input at the equipment, or by operator selection from a menu of recipes stored at the equipment.

Equipment manufacturers were asked to indicate whether their equipment initiates automatic parameter setup prior to process initiation or whether operator interaction with the equipment is necessary once the recipe has been received by the equipment. Some vendors responded that parameter setup responsibility is divided between operator and equipment, as noted in Table 13. In the survey, 35 of 42 equipment models can implement parameter setup with no operator interactions. DATAQUEST believes that fully automatic parameter setup is an essential component of equipment operation in an automated fab.

Table 13

PARAMETER SETUP

Equipment Category	Equipment	Operator	Equipment/ Operator
CVD	4	0	0
Diffusion/Anneal	6	0	0
Dry Etch	9	0	0
Epitaxy	2	1	0
Ion Implantation	1	1	1
Lithography	4	1	1
Sputter	3	0	1
Track	6	1	0
Total	35	4	3
Percent Responses	83%	10%	7%

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Process Initiation

One final area of operator interaction with the equipment is in the area of process initiation. Vendors were asked to indicate whether the equipment or an upstream host system can initiate the process or whether an operator is required to "push the start button." As shown in Table 14, vendor responses indicate that there is essentially a 50-50 mix with regard to process initiation responsibility.

DATAQUEST believes that the current level of operator interaction with equipment must be reduced further in order to provide processing capability in a fully automated environment. Equipment that can operate solely on the basis of equipment/host transactions will be judged as that most suitable for operation in an automated facility. While manufacturers are making the transition to a "peopleless" processing environment, equipment that can accept a lot ID input from an operator provides a useful alternative for lot ID verification with host expectations. Semiconductor manufacturers are evaluating processing equipment today on the basis of such criteria as present and future automation strategies are being developed in the industry. DATAQUEST encourages equipment manufacturers to continue to focus on these issues as well as on increased equipment reliability, for which the level of operator interactions and assists also must be minimized in order to achieve manufacturing goals in an automated semiconductor fabrication facility.

Table 14

PROCESS INITIATION

Equipment Category	Equipment	Operator	Not Available
CVD	3	0	1
Diffusion/Anneal	4	2	0
Dry Etch	6	3	0
Epitaxy	1	2	0
Ion Implantation	1	2	0
Lithography	0	6	0
Sputtering	2	2	0
Track	5	2	0
Total	22	19	1
Percent Responses	52%	45%	3%

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Equipment Communications

DATAQUEST ANALYSIS

DATAQUEST believes that equipment-host communications is a critical component in the automated manufacturing environment. Our current evaluation of this topic concludes that:

- The SECS protocol has been accepted as the industry standard for communications.
- While MAP may have a future in the semiconductor industry, it will not replace SECS at the equipment level.
- The opportunity exists for equipment manufacturers to gain a strategic market advantage with active participation in SECS protocol development.
- Equipment protocol implementation should not be a proprietary issue.
- DATAQUEST strongly encourages IC manufacturers to establish a clear consensus on SECS protocol specifications.

The SECS protocol clearly has been established as the standard for communications in the U.S. semiconductor industry. European and Japanese semiconductor manufacturers are also adopting the protocol in their facilities. To assist in the distribution of information on the protocol, the SEMI Communications Subcommittee has made presentations in Japan and the SECS protocol document has recently been translated into Japanese. Japanese equipment and computer manufacturers are contributing to protocol modifications and development through JEIDA (the Japan Electronic Industry Development Association) in order to achieve standardization of the SECS protocol.

The majority of semiconductor manufacturers involved in advanced device fabrication now require SECS compatibility for new equipment purchases. However, many offer little else for guidance. Equipment vendors have commented that most semiconductor manufacturers do not seem to know what they want with regard to automation or in the specifications of a SECS II message set. Many equipment vendors are thus faced with the prospect of developing a SECS protocol that will require special customization when the equipment is finally installed in an automated environment at a given semiconductor manufacturer's facility.

Clearly, there is a need for semiconductor and equipment manufacturers to establish a common framework for protocol implementation in order to remove the confusion surrounding the protocol and lower the software development costs of manufacturers. DATAQUEST believes that

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semiconductor manufacturers involved in the automation effort need to take the first step and establish a clear consensus on what they feel is necessary for SECS protocol implementation by equipment manufacturers.

It has been suggested that a SECS Users Group for IC manufacturers be organized as a forum for identifying protocol and automation needs from a manufacturing perspective. In particular, the SECS Users Group would identify protocol specifications for specific equipment categories. Equipment manufacturers would participate in the SECS Users Group and provide their current protocol documentation as an aid in evaluating the status of protocol implementation. Some equipment manufacturers, however, regard their protocol implementation as confidential information. Semiconductor processing equipment should not be competing on the basis of protocol implementation but rather on equipment design and special features.

CIM manufacturer involvement with a SECS Users Group is also very important because the development and implementation of a CIM software package is the critical link between the equipment and the manufacturing elements of the fab. The time and cost for linking equipment to a CIM system in a semiconductor fab would be reduced considerably if the implementation of a SECS protocol offered a standardized procedure for interactive communications.

DATAQUEST believes that equipment manufacturers that actively participate in the development of the SECS protocol and the formulation of protocol specifications for their specific equipment categories will gain a strategic market advantage in providing equipment to the semiconductor industry. Equipment manufacturers have the opportunity to participate in the formative stages of automation in the semiconductor industry, and in the process can establish firm relationships with the automation leaders. Semiconductor manufacturers that are not yet active in the automation arena will evaluate future equipment purchases not only on equipment performance, but also on equipment manufacturers' proven automation experience and protocol acceptance.

The potential for incorporating the MAP protocol into the automation networks of semiconductor manufacturing facilities is still under evaluation. SECS, however, is the protocol that manufacturers are specifying today. DATAQUEST believes that the SECS protocol, in one form or another, will survive the transition to any MAP-based system in the future. Regardless of which protocol is employed, the need for better communication between equipment, semiconductor, and CIM manufacturers mirrors the automation goal itself: to develop reliable, interactive communications between the various components in an integrated, automated, manufacturing environment.

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APPENDIX A

THE NETWORK ENVIRONMENT: AN OVERVIEW

Introduction

The focus of the development of a computer integrated manufacturing (CIM) environment is to tie together all sources of information and production on the shop floor. The infrastructure that describes such a system is a communication network, typically a local area network that provides reliable, medium-to-high speed, interactive communications between various computing devices and processing equipment. A local area network, by definition, is located within a limited geographical area, typically within a single building or adjacent facilities.

Network Components

A communications network can be characterized by several different components, including the physical medium used for data transmission, the type of data transmission employed, the configuration or topology of the network, and, finally, the data link (or access method) by which communication devices gain use of the network's physical medium. The communications protocol is an important component in ensuring operational consistency and compatibility among the variety of computers and equipment operating in a network environment. The following sections review the network components that are supported by the SECS and MAP protocols.

Physical Medium/Data Transmission

In the SECS protocol, electrical connections between equipment and computers utilize the international standard known in the United States as EIA RS-232-C (or, more simply, RS-232) for connector and voltage levels. RS-232 is a mature standard and the familiar 25-pin, "D"-shaped connector can be found on almost every type of computer today. While RS-232 uses the 25-pin connector, the SECS protocol specifies bit serial data transmission along only a single wire (plus a ground); one wire is used for transmission in one direction and a second wire for the reverse direction. The SECS protocol, therefore, uses only a total of three signal wires (plus frame ground) for transmitting data and only one flow of information is allowed at any one time (half-duplex transmission).

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Equipment Communications

SECS I also specifies that equipment will provide power on two additional pins for external line-drivers for the purpose of extending the cable length. The RS-232 connector also has several additional pins that are useful for testing purposes but are not specified by the SECS protocol. Since some computer systems may require that these pins be active, appropriate signals will have to be locally generated by the equipment for those systems.

In the SECS protocol, the data transmission rate is limited to 9,600, 4,800, 2,400, 1,200, 300 or 150 baud (characters per second), with a high-speed option of 19,200 baud also available with modification. The preferred data transfer rate of 9,600 baud is considered sufficient for most equipment-to-host communications; however, speed can be a problem when data-intensive measuring equipment communicates with a host system. For that reason, some level of data reduction is usually required before uploading information to the host, so as not to "tie up" the lines for too long a period of time.

The MAP protocol specifies broadband coaxial cable as the physical medium for the network. Broadband coaxial cable is a shared medium that consists of multiple independent channels. Broadband transmission uses CATV technology (Community Antenna TeleVision, more commonly known as CAble TeleVision), which is characterized by a wide bandwidth that uses frequency division multiplexing to establish multiple channels. It has a high data bandwidth, typically 400 MHz, with 5 to 10 MHz per channel. Broadband coaxial cable can also support a closed circuit television system and voice telephone in addition to providing the physical communications medium for digital transmission in a local area network. One additional advantage of broadband coaxial cable is that it can be installed over distances of up to 10 kilometers; longer distances can be achieved with the installation of repeaters. Its primary disadvantages are the cost and complexity of installation. Broadband coaxial cable is very cumbersome to work with and, in addition, each tap to the network requires a modem.

Since baseband transmission is often mentioned in context with broadband, it is useful to understand the difference between these two types of transmission that are used in an automated factory environment. Baseband transmission (not supported by MAP or SECS) specifically employs bit serial digital transmission in which a variety of coding techniques are used that rely on time division multiplexing. When each communications device transmits on a baseband system, it makes use of the entire bandwidth of the channel, typically 5 MHz. Baseband coaxial cable technology is well understood. It is a low-cost, easy-to-install cable. However, its disadvantages are that it is a single channel system and can only be applied over a limited distance on the order of 3 kilometers.

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Equipment Communications

Topology

A network topology or configuration is the geometric arrangement of computing devices, or nodes, and the physical media links that make up the network. A node may be defined as a communication system connection point, and is typically represented by either a controller or a computer. The network configurations that will be discussed here include the point-to-point hierarchical structure, as well as the ring and bus network topologies. Figure A-1 shows schematic representations of the three general types of geometrical configurations that have been implemented in automated network environments.

The SECS standard supports a point-to-point configuration or topology in which a single communication line links two stations that each have the capability to initiate a conversation. The point-to-point configuration may be extended into a more complex topology known as the tree or hierarchical configuration. In the hierarchical configuration, a host system is resident at the uppermost level, with an intermediate level of communication devices (node computers) installed between the host and the equipment-level computer systems. The tree configuration is a particularly useful topology for SECS as the SECS message header contains information that indicates the direction of information flow (i.e., "up" or "down" the tree).

The ring topology, while not used in the semiconductor industry, can be found in other communication networks. In the simple ring configuration illustrated in Figure A-1, each communication node is connected to exactly two other nodes. Data that travels through the ring must go through each station in its path between the original source and final destination of the message. The simplicity of the design provides that no routing decisions must be made; however, the system has predictable timing delays because of the geometrical arrangement. One major disadvantage of the ring configuration is that a failure in any one device on the ring can have a global effect on the system unless relay shunts are provided around each device. The SECS and MAP protocols do not support the ring topology.

In the bus configuration, each node in the system is connected to a central transmission line. The transmission line or bus is passive so that in the event that a node communications device fails, the bus still remains operative. However, because of the arrangement of a bus configuration, specific protocols must be established to deal with which communications device has the control of the network at any given time. The MAP protocol employs a bus topology.

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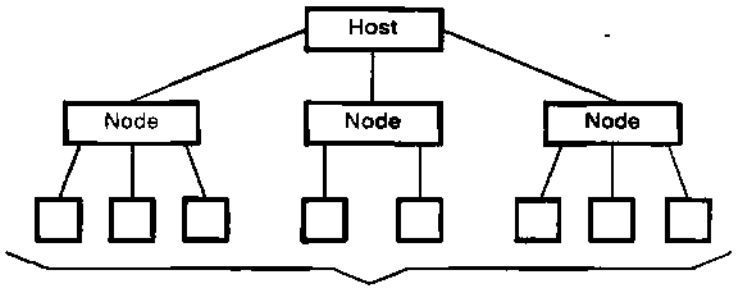
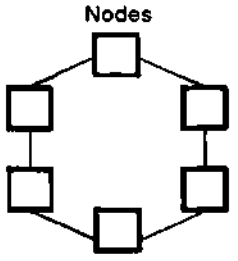
Figure A-1

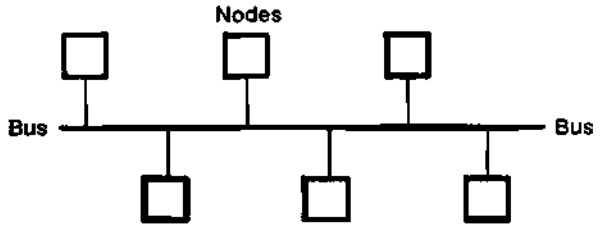
SCHEMATIC REPRESENTATIONS OF NETWORK TOPOLOGIES



Point-to-Point Topology (Hierarchical)



Ring Topology



Bus Topology

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Access Method

The access method by which a communication device obtains use of a network's physical medium is part of the the overall data link control of a given communications protocol. The data link establishes the direction of transmission, verifies proper data link status, and resolves contention when more than one device attempts to transmit at the same time.

The data link protocol in SECS I is the procedure used by the serial line to establish the direction of communication between the equipment and a host computer. As mentioned previously, transmission between host and equipment under the SECS protocol is half-duplex, so that essentially only one party is allowed to talk at any one time. When both ends of the line attempt to communicate at the same time, it results in a line contention or a "collision." Collisions are resolved in the SECS protocol by the specification of one station as the master and the other end of the link as the slave. In the event of a collision, the slave postpones transmission and yields to the master. The SECS I protocol also provides a series of timeouts and retries that are used to correct communication errors.

In a semiconductor processing environment, the equipment typically is designated as the master and the node or host computer as the slave. This initially may seem contrary to the hierarchical topology that is supported by the SECS protocol, but since the equipment computer usually has limited storage capability for messages, it must be allowed to send any messages it has before receiving new requests for information from the host system.

Polling can be described as a controlled media access method. It requires a master/slave relationship among the communication nodes in the system. The master computer typically controls the link and initiates all communications within the system. All other devices on the network, designated as slaves, respond only when polled by the master for information.

Token passing is a shared media access method. In this type of configuration, the "token" or special message is passed around the network in a prescribed manner. The station that holds the token is given exclusive but temporary control of the network to transmit information. All other stations in the network can only listen when the token is not in their possession. Ring and bus topologies typically employ a token passing access method. The MAP protocol, in particular, utilizes token passing as the access method in its bus network.

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The carrier sense multiple access/collision detection (CSMA/CD) access method can be simply described as a system in which a station listens before talking and listens while talking. It is important that before transmitting information, each communications device first listens to the network to see if the media is occupied or idle. When access has been gained to the physical media and transmission has begun, each device also listens for a collision--someone else in the network trying to gain access to the system. If a collision occurs, each station backs off the network for a prescribed and unique period of time in order to prevent another collision. Ethernet, a local area network developed by Xerox, utilizes the CSMA/CD access method.

Both the polling and token passing access methods avoid the issue of contention by their very design. The CSMA/CD access method is similar to that specified in the SECS protocol since both have mechanisms to deal with line contention. However, the difference between these two methods is that in the SECS protocol, contention is resolved by the slave yielding to the master, while in CSMA/CD, both stations back off the network for a prescribed and unique period of time in order to prevent another collision.

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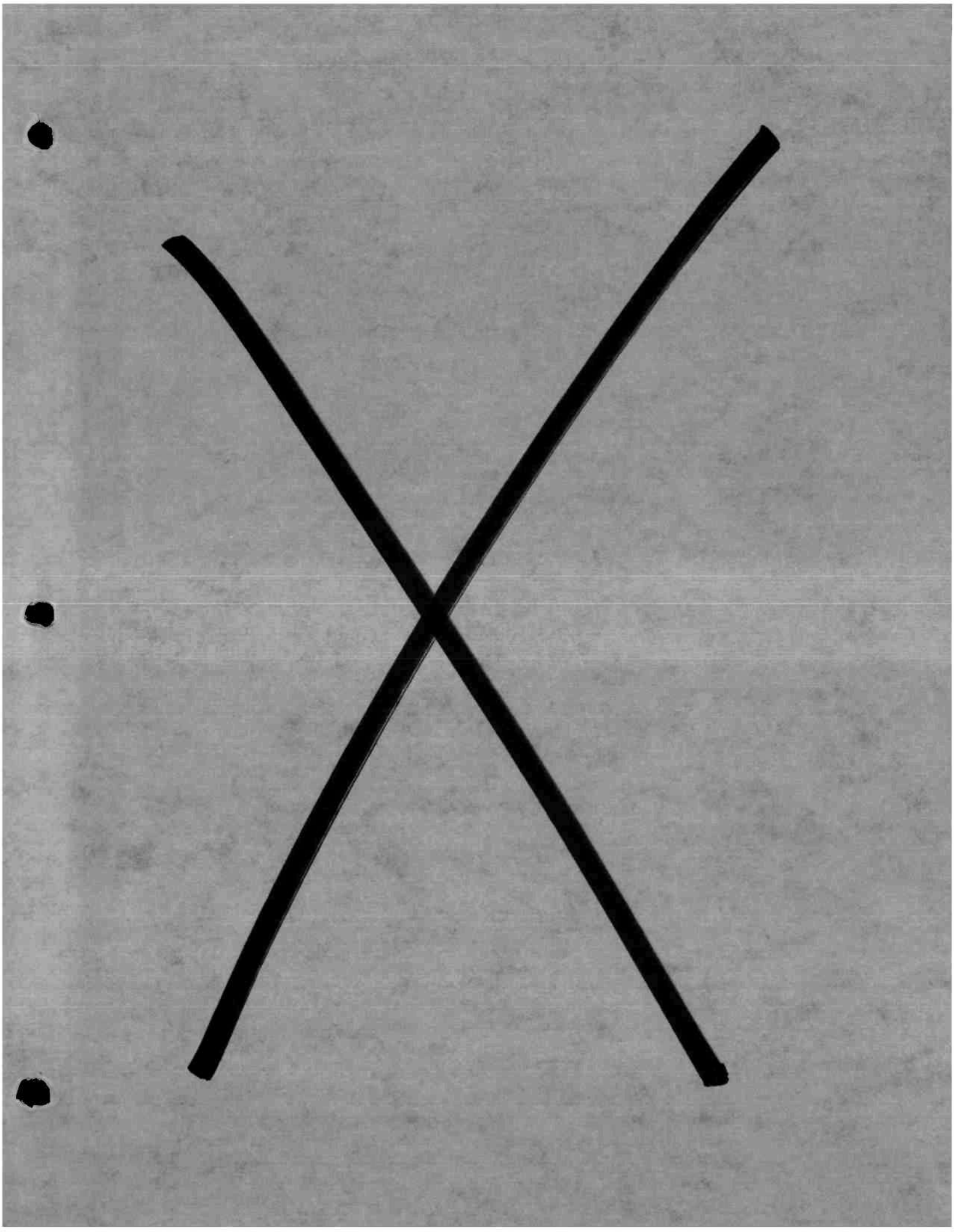

Industry Issues

The following is a list of the material in this section:

- Line Geometries of Silicon Wafers

For additional information, please refer to the material behind the Industry Issues in your Newsletter binder.

Line Geometries of Silicon Wafers

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Line Geometries of Silicon Wafers

INTRODUCTION

The term "line geometries" refers to the minimum geometries of semiconductor devices. Dataquest obtains information on the distribution of the production of line geometries in both wafers and square inches through empirical methods—chiefly through our U.S. fab data base survey. In our survey, we define line geometries as the minimum feature size of a device as drawn, since actual production geometries can vary greatly.

Line geometries are the feature sizes that semiconductor equipment manufacturers must use as parameters in configuring and designing their equipment. The trend is for line geometries to become smaller, which places ever greater demands on equipment and materials manufacturers. These additional demands include registration, overlay, CD measurement, and increasingly stringent cleanliness standards.

CURRENT DISTRIBUTION OF LINE GEOMETRIES

As recently as 1984, 70 percent of silicon wafer starts were of geometries greater than or equal to 2.5 microns (see Figure 1 and Table 1). In 1987, however, these wafer starts accounted for only slightly more than 36 percent of all wafer starts (see Figure 2). In addition to new sub–2.5 micron fabs coming on line, there are two other major reasons for this shift:

- Most of the fabs that were closed in the downturn of 1985 and 1986 had geometries greater than 3 microns.
- Many fabs that were categorized in the 2.5– to 3–micron range have since improved their process and now produce at smaller geometries.

In 1987, wafer starts for sub–2 micron geometries accounted for more than 36 percent of all wafer starts, approximately equal to the number of wafers with geometries greater than or equal to 2.5 microns. Wafer starts with geometries greater than or equal to 2 microns and less than 2.5 microns accounted for almost 27 percent of all wafers. Submicron wafer starts were negligible, accounting for slightly less than 1.0 percent.

The distribution of line geometries in 1987 by square inches (see Figure 3) differs somewhat from the wafer start distribution of line geometries. This is because the smaller geometries typically are processed on larger wafers than are the larger geometries. Consequently, geometries greater than or equal to 2.5 microns represented only 30 percent of the square–inch starts in 1987, yet represented 36 percent of 1987's wafer starts.

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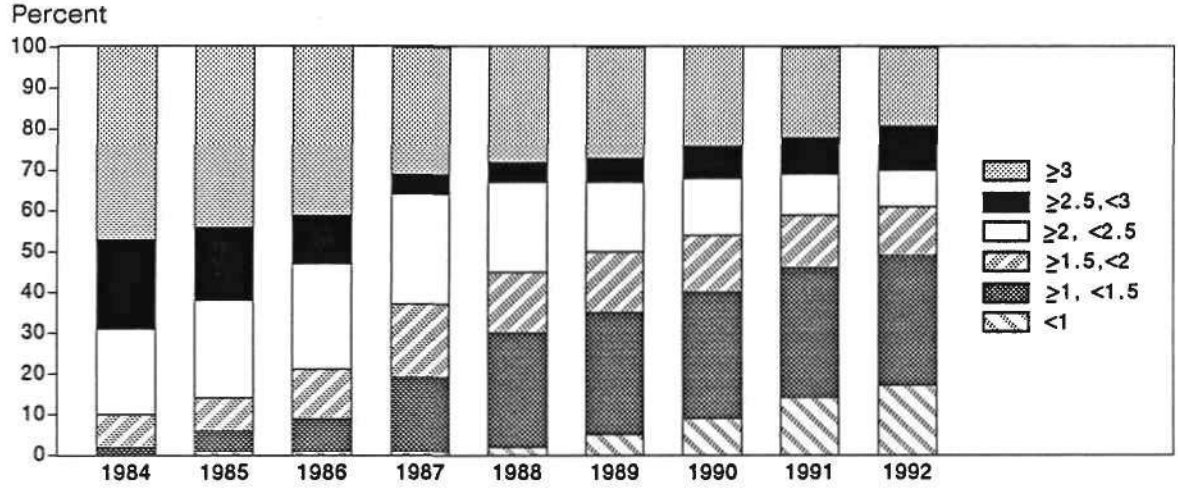
Line Geometries of Silicon Wafers

Figure 1

Distribution of Silicon Wafer Starts
by Line Geometries



Note: Totals may not add to 100 due to rounding.

Source: Dataquest
February 1988

Table 1

Distribution of Wafer Starts by Line Geometries

Minimum Line Geometry	1984	1985	1986	1987	1988	1989	1990	1991	1992
<1 Micron	0	1%	1%	1%	2%	5%	9%	14%	17%
≥1 Micron and <1.5 Microns	2%	5	8	18	28	30	31	32	32
≥1.5 Microns and <2 Microns	8	8	12	18	15	15	14	13	12
≥2 Microns and <2.5 Microns	21	24	26	27	22	17	14	10	9
≥2.5 Microns and <3 Microns	22	18	12	5	5	6	8	9	11
≥3 Microns	48	45	42	31	29	27	26	22	19
Total	100%	100%	100%	100%	100%	100%	100%	100%	100%

Note: Columns may not add to totals shown because of rounding.

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Line Geometries of Silicon Wafers

Figure 2

1987 Starts by Line Geometry

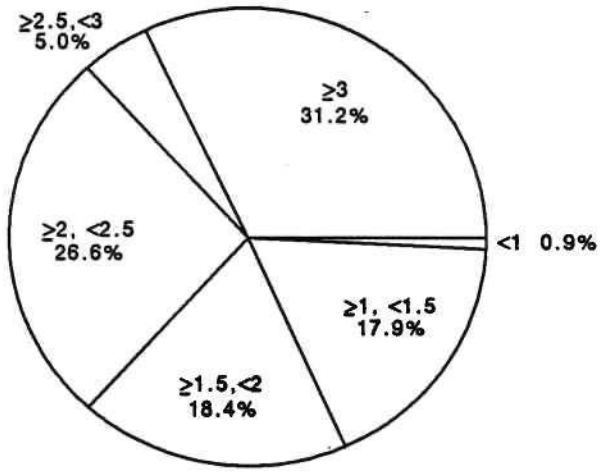

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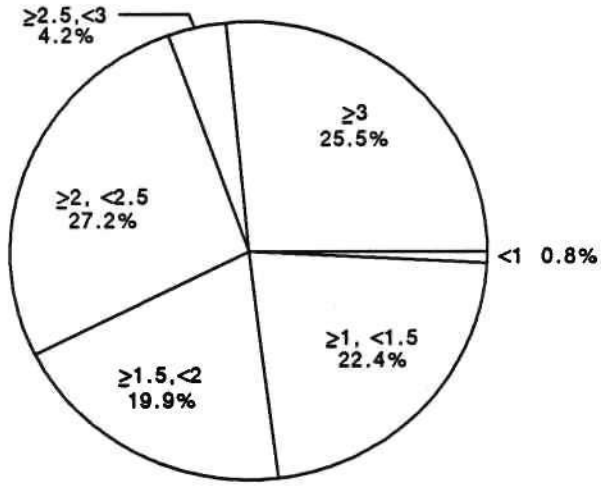
Figure 3

Distribution of Square Inches by Line Geometry 1987



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Line Geometries of Silicon Wafers

CAPACITY UTILIZATION BY LINE GEOMETRIES

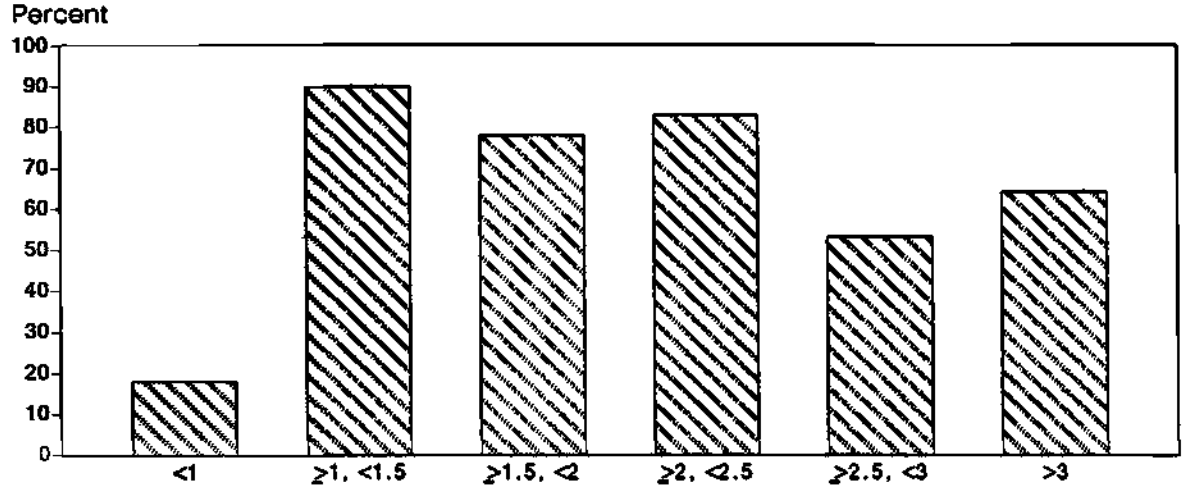
Figure 4 shows Dataquest estimates for silicon wafer capacity utilization by line geometries for the final quarter of 1987. Wafers with geometries of less than 1.5 microns but greater than or equal to 1.0 micron have the highest utilization rate—90 percent. A 90 percent utilization rate is a rate at which shortages occur; it implies tight supply and some shortages. At this utilization level, manufacturers will rush to buy equipment to increase capacity.

Utilization rates for wafers with geometries between 1.5 microns and 2.5 microns are also high—approximately 80 percent. Utilization rates for wafers with geometries equal to or greater than 2.5 microns are not very high, and, in general, we do not expect high demand for equipment to produce devices in this range.

The utilization rate for silicon wafers with geometries of less than 1 micron is very low—only 18 percent. The reason for this low rate is that these lines are just beginning their ramp-up phase. We expect the utilization rates to rise slowly because of the difficulty in developing and characterizing the process for submicron production.

Figure 4

Silicon Wafer Start Capacity Utilization
by Line Geometries
Q4 1987



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Line Geometries of Silicon Wafers

SUBMICRON SHIFT IN NEW FABS

High utilization rates are magnets that attract additional capacity. Additional capacity can be added either through upgrades of existing facilities or through building new fabs.

Dataquest has tabulated the capacity for all planned or announced new fabs between now and 1991. Table 2 shows the distribution of new wafer capacity from 1988 to 1991 by line geometries.

We expect that 80 percent of the new fabs built in the United States in 1988 will be capable of sub–1.5 micron production. By 1991, most new fabs will be capable of producing wafers with geometries of less than one micron.

Table 2

Distribution of New Wafer Capacity by Line Geometry for Planned or Announced New Fabs 1988–1991

Minimum Line Geometry	1988	1989	1990	1991
<1 Micron	1%	9%	42%	78%
≥1 Micron and <1.5 Microns	80%	61%	49%	22%
≥1.5 Micron and <2 Microns	20%	31%	10%	0

Source: Dataquest February 1988

FORECAST OF LINE GEOMETRIES

Based on the new fabs that will be coming on–line and on the Dataquest IC consumption forecast, Dataquest has forecast the distribution of silicon wafer starts by line geometries through 1992 (see Figure 1 and Table 1). Wafer starts with geometries of less than 1.5 microns, which in 1987 accounted for slightly less than 20 percent of total silicon wafer starts, will account for almost 50 percent of total starts by 1992. Submicron wafer starts will account for 17 percent of all starts in 1992. The share of wafers with geometries greater than or equal to 3 microns will decline from 31 percent in 1987 to 19 percent in 1992. The growth of such devices such as smart power and mixed signal devices will cause the proportion of devices with geometries of greater than or equal to 3 microns to decline and, after 1988, will cause the proportion of devices with geometries less than 3 but greater than 2.5 microns to increase.

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Line Geometries of Silicon Wafers

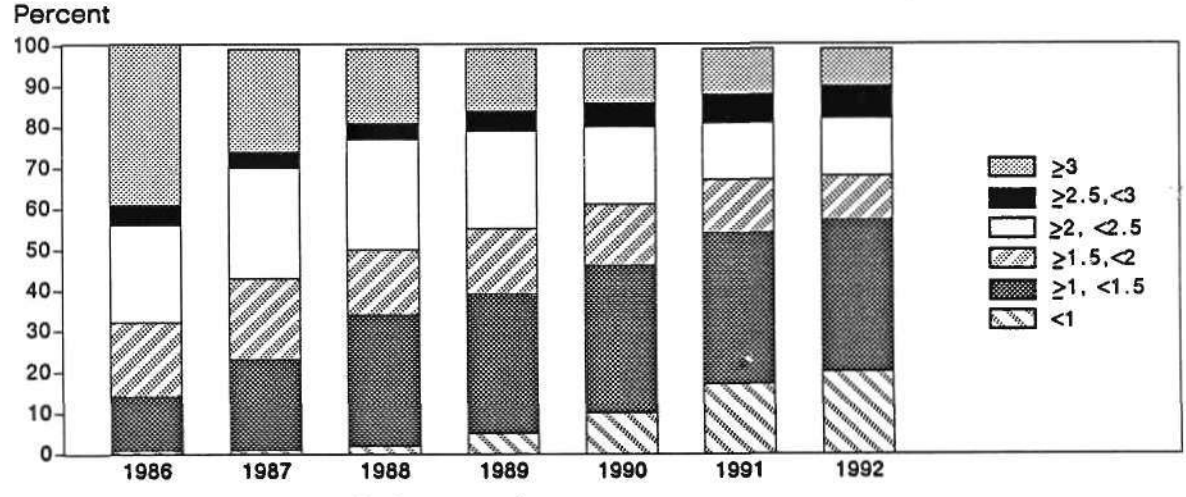
Wafer starts with geometries of less than 2.5 microns and greater than or equal to 1.5 microns will decline in proportion to the total. This trend will result from upgrades as manufacturers move from, for example, producing 2–micron devices to devices with sub–1.5–micron geometries.

In addition to wafer starts, Dataquest has forecast the square inches of silicon consumption by line geometry (see Figure 5 and Table 3). Square inches of silicon is especially important to silicon manufacturers and to other materials suppliers as a surrogate for material consumption. The distribution of square inches by line geometries is similar to that of wafer starts by geometries. However, because devices with smaller geometries tend to be produced on larger wafers and devices with larger geometries tend to be produced on smaller wafers, the proportion of square inches devoted to sub–1.5–micron production is slightly larger, while the proportion devoted to greater than or equal to 2.5 microns is smaller.

Sub–1.5 starts in 1987 accounted for less than 25 percent of all square inches of silicon processed in the United States. We believe that by 1992, it will account for more than 50 percent of all the square inches processed. Greater than or equal to 2.5–micron devices accounted for 25 percent of all square–inch starts in the United States in 1987. We believe that this share will decline to 9 percent by 1992.

Figure 5

Distribution of Square Inches of Silicon
by Line Geometries



Note: Totals may not add to 100 due to rounding.

Source: Dataquest
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Line Geometries of Silicon Wafers

Table 3

Distribution of Square Inches of Silicon by Line Geometries

Minimum Line Geometry	1986	1987	1988	1989	1990	1991	1992
<1 Micron	1%	1%	2%	5%	10%	17%	20%
≥1 Micron and <1.5 Microns	13	22	32	34	36	37	37
≥1.5 Microns and <2 Microns	18	20	16	16	15	13	11
≥2 Microns and <2.5 Microns	24	27	27	24	19	14	14
≥2.5 Microns and <3 Microns	5	4	4	5	6	7	8
≥3 Microns	40	25	18	15	13	11	9
Total	100%	100%	100%	100%	100%	100%	100%

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
February 1988

DATAQUEST CONCLUSIONS

Most of the new fabs built in the next five years will be capable of sub-1.5-micron production. Furthermore, 20 percent of the square inches of silicon processed in 1992 will be on wafers with submicron geometries. While submicron production will place difficult performance, measurement, and cleanliness demands on equipment and materials manufacturers, we believe that these demands will not only provide opportunities, but will also be the proving ground for tomorrow's market leaders.

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Semiconductor Equipment and Materials Service Semiconductor Manufacturing

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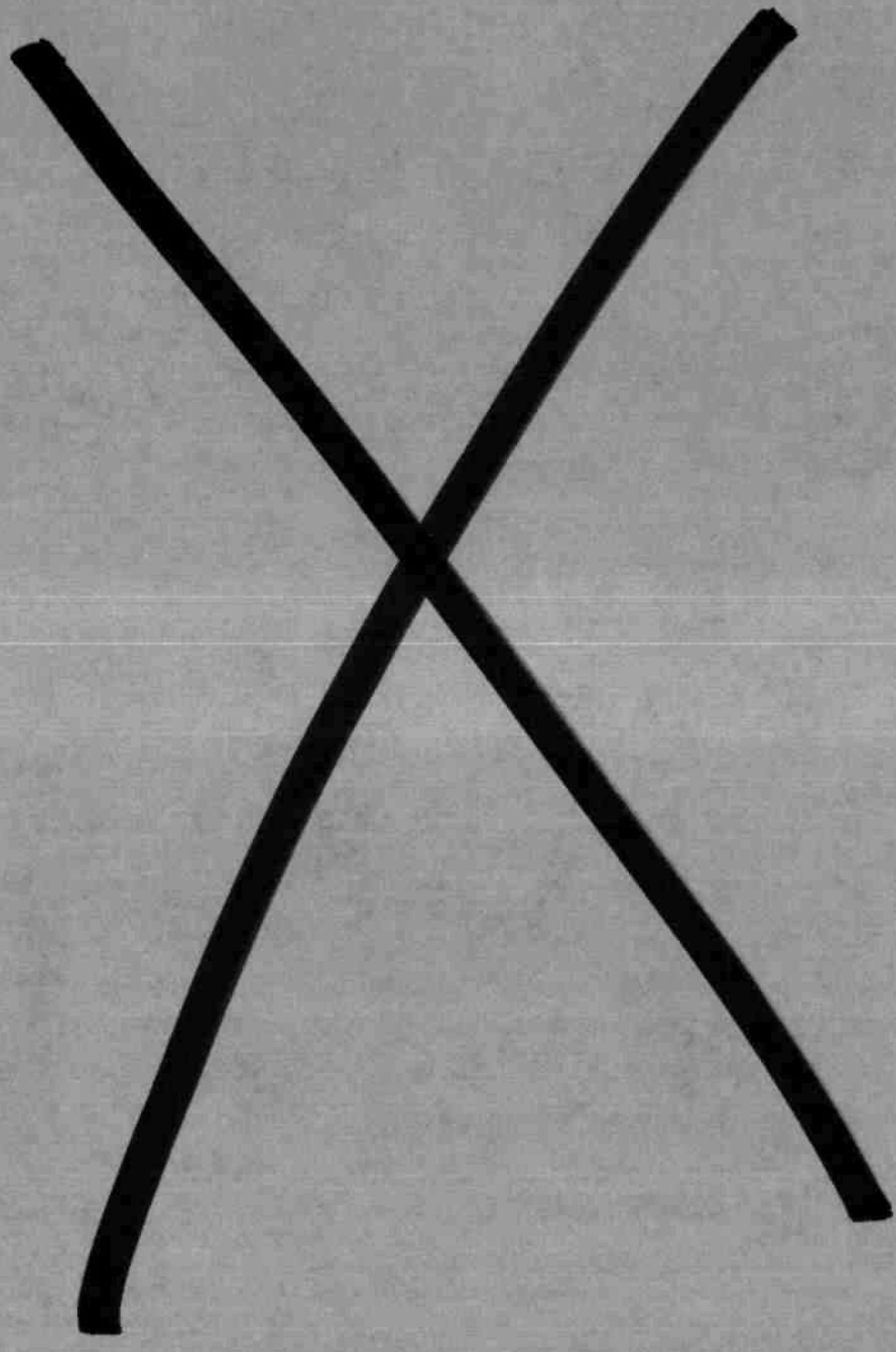

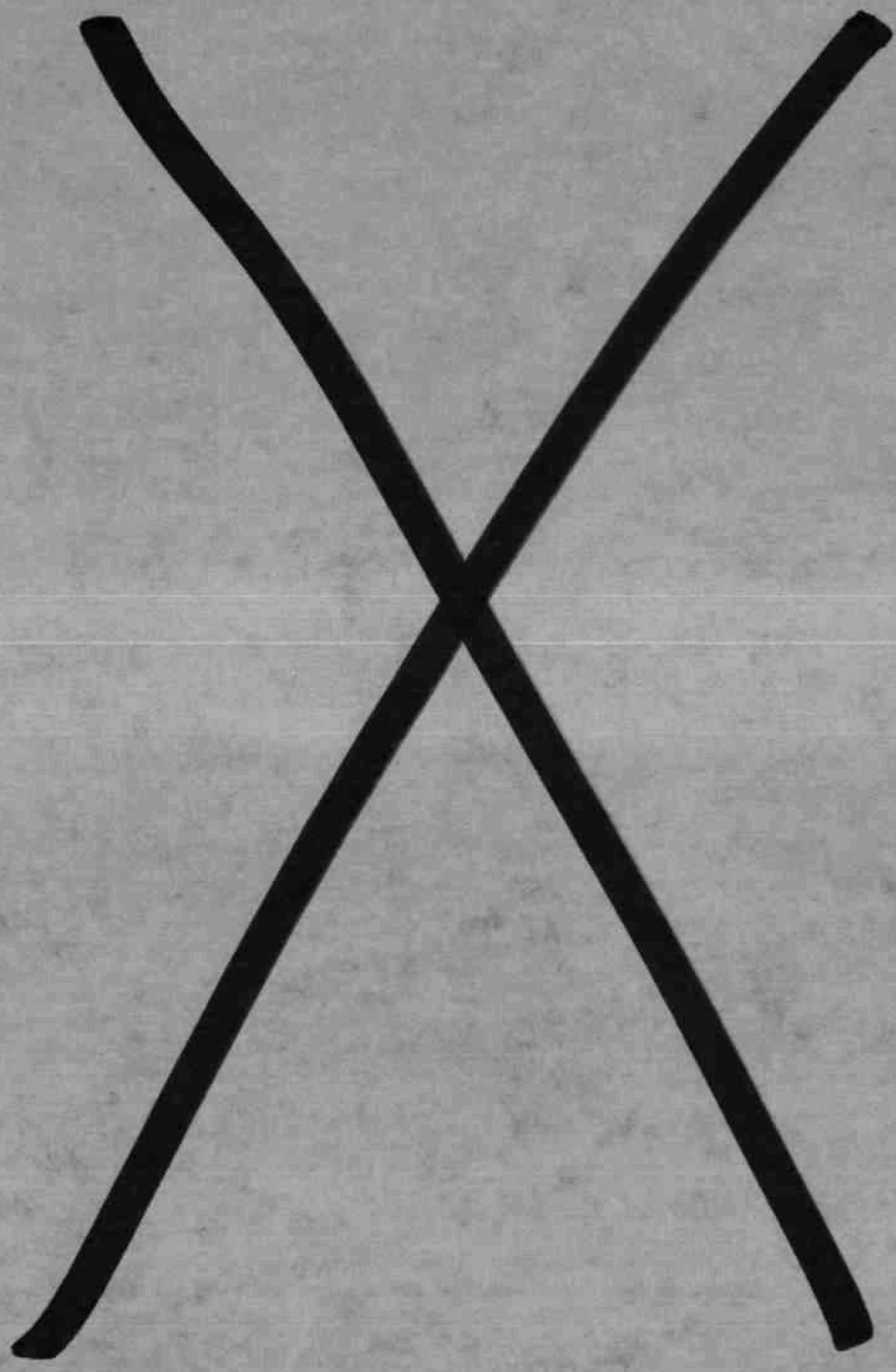

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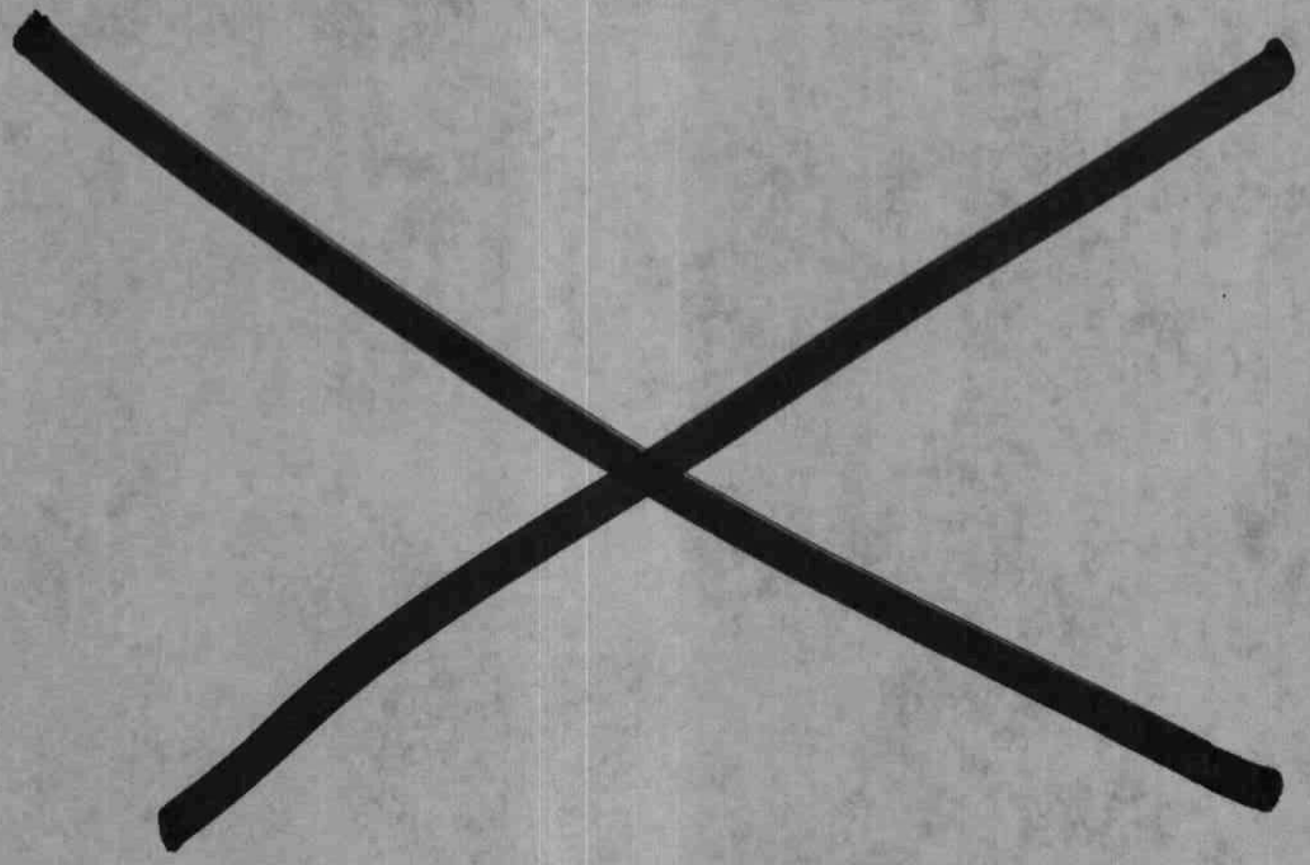

Business Conditions

The following is a list of the material in this section:

- U.S. Demographics

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