Semiconductor Equipment and Materials Service 1987–1988 Newsletters and Bulletins

Dataquest

a company of The Dun & Bradstreet Corporation

1290 Ridder Park Drive
San Jose, California 95131-2398
(408) 437-8000
Telex: 171973
Fax: (408) 437-0292

Sales/Service offices:

UNITED KINGDOM
Dataquest UK Limited
13th Floor, Centrepoint
103 New Oxford Street
London WC1A 1DD
England
01-379-6257
Telex: 266195
Fax: 01-240-3653

FRANCE
Dataquest SARL
Tour Gallieni 2
36, avenue Gallieni
93175 Bagnolet Cedex
France
(1)48 97 31 00
Telex: 233 263
Fax: (1)48 97 34 00

GERMANY
Dataquest GmbH
Rosenkavalierplatz 17
D-8000 Munich 81
West Germany
(089)91 10 64
Telex: 5218070
Fax: (089)91 21 89

JAPAN
Dataquest Japan, Ltd.
Taiyo Ginza Building/2nd Floor
7-14-16 Ginza, Chuo-ku
Tokyo 104 Japan
(03)546-3191
Telex: 32768
Fax: (03)546-3198

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Strategic ISSUES

A Special Report from Dataquest.

January 1988

Manufacturing: Global Struggle in a Changed Environment

By David C. Penning and John W. Wilson

An industrial miracle is starting to revive America's sickly factories. Although the health of U.S. manufacturers has been the target of much editorial and political concern, their competitiveness actually is rising rapidly. Dataquest believes that U.S. corporate strategists can no longer assume the superiority of offshore manufacturing facilities and sources. Manufacturing for export to the United States may no longer be a successful basis for economic development plans. The stage is set for global competition in which U.S. factories must once again be respected as worthy contenders—but only if U.S. managers take full advantage of their strengthening position.

HOPEFUL OMENS

There is clear evidence of improvement in national productivity statistics. Prudential-Bache economists Edward Yardeni and Deborah Johnson pointed out in a recent study that the productivity of U.S. manufacturing, which lagged badly in the 1970s, has grown at a compound annual rate of 4.8 percent since 1982.

More impressive still is the performance of the durable goods sector, which recorded annual gains averaging 7.1 percent in output per man-hour. Mr. Yardeni and Ms. Johnson cited the corporate restructurings, tougher labor settlements, and tighter inventory controls that have rippled through corporate America in the last few years as sources of the advance in factory productivity.

On top of this, the plummeting dollar has wiped out the advantages conferred on Japanese and European manufacturers during the first half of the decade, when the dollar seemed to be headed for the moon. Japan, with its incredible industrial flexibility, has been able to cut costs substantially on a wide range of products since the yen started its climb in 1985. But many European companies have been forced to raise their dollar prices by 20 percent or more, and the Japanese will have to follow suit as the dollar continues to decline. Dataquest believes that companies now must plan for a world in which the dollar is worth only ¥120 and DM 1.55.

DO LABOR COSTS MATTER?

Rounding out the changes are advances in product design and manufacturing automation, which together have drastically reduced the direct labor content in many products. In many cases, direct labor now accounts for no more than 5 percent to 15 percent of total production costs, suggesting that labor cost differentials have become unimportant for some products.

That is what Tandy Corporation discovered when it took a close look at the cost of producing its Color Computer 3 in South Korea. Tandy decided to move the product to a plant in Fort Worth, Texas, because currency changes, Korean inflation, and higher freight and duty costs made it 7 percent cheaper to manufacture in Texas. "The direct labor component is so small," says Ed Juge, director of market planning for Tandy, "that it doesn't enter into the picture."

David C. Penning is director of Dataquest's Manufacturing Automation Service. A graduate of Yale University and the Harvard Graduate School of Business, Mr. Penning has worked in manufacturing management at DuPont, Hewlett-Packard, and Honeywell. John W. Wilson is Vice President for Business and Technology Analysis at Dataquest and editor of Strategic Issues.

Case Study #1

IBM's Manufacturing Strategy

By David C. Penning

International Business Machines Corporation is a leading vendor of manufacturing automation systems. But, unlike the shoemaker whose children went barefoot, IBM is also recognized as a pioneering user of new manufacturing concepts in its own facilities. It has established at least three "showcase" facilities in the last few years: the Lexington, Kentucky, typewriter plant; the Charlotte, North Carolina, printer facility; and the Austin, Texas, personal computer factory.

All must be regarded as leading examples of world-class manufacturing. At Lexington, for example, IBM spent $350 million to renovate and equip a facility that can take a typewriter from receiving dock to shipping dock in 16 hours. Dataquest identifies these key components of IBM's manufacturing strategy as exemplified by these new plants:

- The primary manufacturing goal is to develop factories geared for high-volume production at competitive cost levels. A key strategy supporting this goal is the concept of close working communications between designers and production engineers. Design trade-offs such as processes, materials, tolerances, and sourcing are influenced by manufacturing considerations as well as design objectives.
- A second strategic goal is to emphasize design of products for manufacturing in an automated environment. For example, variations are kept as low as possible by:
  - Reducing the number of parts required for the assembled product
  - Eliminating fasteners
  - Designing symmetrical parts so that orientation problems in assembly are reduced
- A third element of IBM's strategy is to limit the number of models and to minimize engineering change orders. When customized variations are essential, they are moved out of the production area and into the distribution chain. Product design changes are delayed until several can be introduced simultaneously in a new model.
- Finally, inventories are kept low by scheduling shipments of components so that a constant flow for each product line is achieved. This just-in-time (JIT) approach encourages close relations with suppliers and keeps work-in-process inventories low. The number of suppliers serving a plant is reduced dramatically—in the case of Lexington, from 640 to about 30. JIT, IBM believes, also fosters zero-defect quality goals for both suppliers and workers at successive steps in the production process.

NO MORE EXCUSES

All of this has done no more than clear away the most obvious excuses for the shockingly bad performance of many U.S. industries, including the electronics industry, in international competition. While exports have started to rise again, imports have not slowed. Foreign manufacturers, reluctant to give up hard-won positions in the U.S. market, have been slow to pass along the impact of the falling dollar by raising prices. Further, the high perceived value of many imported goods suggests that U.S. consumers will be willing to pay higher prices for them. Clearly, relying on currency changes alone to restore competitiveness will not work.

Similarly, the efforts to restructure companies and to cut labor costs, inventories, and overhead are necessary but not sufficient steps toward full international competitiveness. Even the progress on reducing direct labor content is, by itself, not the answer to a very complex problem.

Manufacturing has been neglected for so long in the U.S., both in terms of investment and of corporate culture and strategy, that it will take almost a revolution to restore its rightful position. For much of the post-World War II period, U.S. companies have taken their manufacturing operations for granted. The way to the executive suite has not been via manufacturing but through marketing or finance. Few talented people have chosen careers in the manufacturing industries, and fewer still have opted for the factory floor. The result is that top executives in the United States seldom have either technical education or production experience.

RETHINKING STRATEGIES

Now that the worst of the inefficiencies have been scoured from American industry, the time has come for a hard look at manufacturing strategies in light of some new realities. Spurred by the urgings of a few academics and consultants, as well as by the example and threat posed by Japanese competitors, some companies have already started rethinking their approach to manufacturing.

Computer and other electronics equipment vendors are in the forefront of this move. They accounted for almost half of the 84 plants and companies singled out by consultant Richard J. Schonberger for an honor roll of efficiency in his 1986 book, *World Class Manufacturing: The Lessons of Simplicity Applied*.

European and Asian companies are also engaged in a dramatic response to the realignment of currencies and other global trends in manufacturing. In contrast to U.S. companies, which raced to establish manufacturing outposts around the world when the dollar soared, Japanese and European companies have tended to concentrate their manufacturing resources at home and to serve foreign markets with exports. That is beginning to change. At the same time, companies in every geographical region are continuing to press for increased automation, but with subtle strategic differences. Dataquest sees the following developments:

- Western Europe is investing heavily in new manufacturing equipment and technologies in order to lower costs. An important part of this investment is for factory networks, information systems, and shop floor controls that will allow better integration of information flows in the factory and across functional organizations.

- Japan is focusing less on factory floor automation, where it leads the world, and more on design automation as product innovation becomes the key to continued market growth. Factories are being built outside Japan to offset the stronger yen and the prospect of trade barriers in key markets. Thus, global communication and control systems are becoming more important as companies struggle to coordinate their increasingly dispersed worldwide operations.

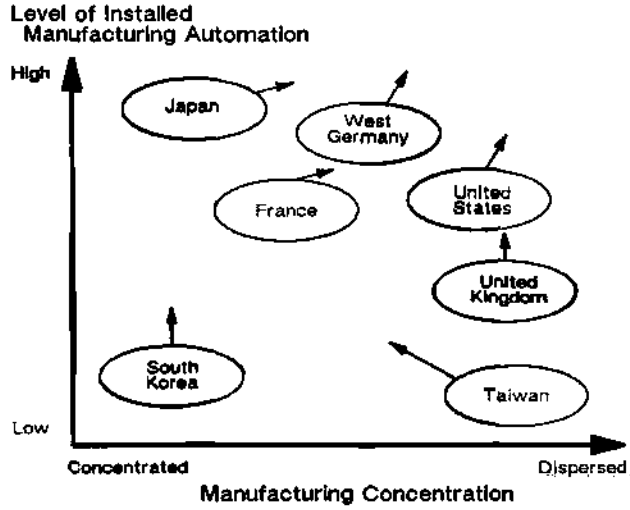
- North America is making product quality the primary manufacturing goal, both to reduce total costs by cutting rework and service and to recover lost market share through improved customer relationships. While some companies continue to invest in automation equipment to lower costs and increase flexibility, few are buying the systems required to integrate their factories. The new political emphasis on preserving domestic manufacturing and technology resources is only beginning to foster a turn from offshore dispersal of production.

- Developing countries, especially in Asia, are starting to focus on product development and on building local niche markets in response to the changing global environment. No longer able to count on using low-cost labor as a winning strategy, they are just beginning to invest in manufacturing automation. In many Asian countries, particularly Taiwan, highly fragmented industries are starting to integrate by sector as the need for world-scale production becomes apparent.

GOING FOR WORLD CLASS

Dataquest believes that while companies in every region have distinctive problems and priorities, (see Figure 1) all must be guided by a few basic manufacturing strategies that flow from new trade and currency realities, new technology, and new management approaches.

Figure 1
Global Strategies in Manufacturing



Source: Dataquest January 1988

Case Study #2

Making Terminals in Roseville

By John W. Wilson

When a manufacturing strategy is tightly linked to marketing, design, and quality objectives, the results can be surprising. In the case of the Hewlett-Packard Company's alphanumeric terminals business, a rethinking of strategies created one of the world's lowest-cost assembly facilities—in the pastureland of California's Central Valley.

Never known for slugging it out in commodity markets, Hewlett-Packard startled the display terminals industry last August when it announced a line of low-priced terminals for the highly competitive Digital Equipment Corporation, IBM 3270, and general-purpose ASCII markets as well as for its own computer systems. HP's prices start at $375, which Greg Blatnik, director of Dataquest's Display Terminal Industry Service, calls the lowest list price for a basic alphanumeric terminal. The move puts HP in direct competition with the factories of Taiwan and South Korea, which produced about half the 2.6 million terminals sold in the United States in 1987.

HP faced two alternatives, explains Larry D. Mitchell, general manager of HP's Roseville Terminals Division. Like other large systems companies, HP was seeing some competitive inroads into its terminals business. But even if it were able to get rid of the clones, HP could not achieve enough volume to reach competitive cost levels. If HP continued supplying terminals only for its own computer systems, it would end up relying increasingly on offshore suppliers.

The other option, which HP adopted about two years ago, was to go aggressively after new markets to achieve competitive production volumes. But that decision in turn required a new approach to manufacturing.

Mr. Mitchell and Max Davis, manufacturing manager, led an effort to make manufacturing strategy fit the new objective. According to Mr. Davis, an important first step was to "wipe the slate clean" in both product design and manufacturing processes. By pushing the manufacturing engineers and designers to work together, HP made sure that factors such as component costs and manufacturability were given top priority from the beginning. Component counts were cut in half, and vendors were pulled into the cost-trimming process early.

HP departed from its usual process of designing the ideal parts and paying high prices to get them. Explains Mr. Davis, "It was an iterative process to first find out what was available at the lowest price; then, if we couldn't use that, we'd ramp up a notch." Altogether, about half the eventual cost savings in the new line of terminals came from design changes, Mr. Davis reckons.

Other savings came from a 75 percent reduction in assembly labor, a move to just-in-time delivery of components, and other manufacturing efficiencies. Dataquest estimates that one eight-hour shift of about 20 workers at the computer-guided Roseville operation can assemble, test, and ship between 300 and 400 terminals. (The Roseville plant is presently operating with two shifts daily.)

One reason for this high output is the care HP took in designing the manufacturing process. For example, the time usually required to handle material was slashed by employing new equipment to move components and present them to the assemblers. The use of bar coding to log incoming materials and to track work in process saved operator time as well.

It is still too early to judge the success of HP's dramatic bid to compete as a manufacturer of high-volume, low-cost products. But HP appears to have demonstrated that a carefully crafted strategy can at least put U.S.-based manufacturers back in a ball game that appeared to be lost.

It should be clear by now that corporate strategists can no longer ignore the need to restore the world trading system to something approaching balance. The huge U.S. trade deficit has generated protectionist talk and legislation that threatens to repeat the disastrous trade wars of the 1930s. Dataquest believes that the political climate alone is likely to make offshore manufacturing less attractive for many U.S. companies and to force exporting companies both to disperse production targeted at offshore markets and to focus more on their own domestic markets.

As global competition intensifies, North American companies will once again be under severe pressure to match the efficiencies of Asian and European manufacturers. That will not be easy, but the path at least is clear. In the last few years, academics and consultants have agreed on the basic structure of what several of them call "world-class manufacturing."

Although definitions vary, this ideal is usually drawn in part from the obvious successes of just-in-time (JIT) inventory policies and other Japanese manufacturing strategies. It is also based on the teachings of Americans such as Joseph Harrington, who spelled out the essentials of computer-integrated manufacturing (CIM) as early as 1973, and W. Edwards Deming and J.M. Juran, who have been preaching the importance of quality for decades. But management fads and technology alone do not equate to world-class manufacturing.

Seven Big Steps

Dataquest has identified seven steps that should be considered by any company seeking a world-class manufacturing strategy:

- Identify a single, overriding mission that guides all underlying manufacturing, marketing, and organizational decisions
- Coordinate planning and implementation for all phases of production, from product and process development to distribution and service
- Integrate information flows among office, product development, production, and delivery systems
- Simplify everything—product designs, production processes, inventories, and management layers
- Stress quality—not just on the factory floor but as an integral part of every job
- Recognize the needs of employees for security, motivation, and training
- Create long-term, mutually supportive relationships with suppliers and customers

THE AGE OF FLEXIBILITY

These guidelines, illustrated in part by the case studies that accompany this report, will be increasingly important as the industrial world moves away from the era of high-volume, focused production to the Age of Flexibility. As James C. Abegglen and George Stalk Jr. point out in *Kaisha: The Japanese Corporation*, many Japanese companies are already shifting away from the highly focused product strategies they used to penetrate Western markets. Faced with currency and trade barriers as well as increasing competition from their developing neighbors in Asia, the *kaisha* are seeking higher-value niches and increasing product variety.

Western companies that try to respond to Japanese competition by diversifying product offerings often run into trouble when their costs or quality get out of line. But companies that react by cutting their product lines "are risking decreased competitiveness and relevance in their markets," Abegglen and Stalk warn. Now every company engaged in global competition must be able to produce a wide variety of products in relatively low volumes without sacrificing manufacturing efficiency or product quality.

Information systems that connect and integrate all the elements that make up a manufacturing enterprise are crucial to flexible manufacturing. Balancing the flows of raw material and production processes in a multiproduct plant cannot be done on the back of an envelope. Yet, Dataquest estimates that U.S. companies are spending only 5 percent of their automation dollars on systems linking their design and production equipment and trying to integrate them. That compares to 16 percent of the total in Asia and fully 30 percent in Europe.

TIME TO WAKE UP

Difficult as it may be for American manufacturers to change their information strategies, that is just one step on the road to world-class manufacturing. What is required, says Mr. Schonberger, is "continual and rapid improvement" in every area of manufacturing management: quality, costs, lead times, customer service, labor relations, and plant organization. The list is a long one, and the evidence is that relatively few

companies have begun to tackle it. Recent issues of *Science* and *Physics Today*, both prestigious scientific journals, carried articles critical of American shortcomings in manufacturing. Thomas G. Gunn, director of manufacturing consulting for Arthur Young & Co., writes disparagingly of U.S. manufacturers in his book *Manufacturing for Competitive Advantage: Becoming a World Class Manufacturer*. "The managements of these companies are paralyzed," Mr. Gunn says, "either unable or unwilling to act."

That paralysis will lead to death if managers do not heed the warnings. Restructuring and the fall of the dollar have provided U.S. manufacturers with a great opportunity to forestall that fate and reclaim their former position of world leadership. They must now put to work the new technologies and techniques that are at their disposal and make manufacturing excellence part of a unified strategy for world competition. They may not get another chance.

Case Study #3

Intel's Manufacturing Strategy

By John W. Wilson

If any industry can be said to be the keystone to American industrial competitiveness, it is the semiconductor industry. According to some pessimists, chipmaking is an endangered art in the United States and needs heavy government intervention. In fact, however, U.S. semiconductor companies have made enormous strides in the efficiency with which they run their manufacturing operations.

Intel Corporation offers a good example of the progress that has been achieved. In the two years since the company decided to upgrade its manufacturing performance, Intel has improved the utilization of its production equipment by 100 percent and dramatically increased the percentage yield of good devices from every wafer start. These advances have enabled the Santa Clara, California, company to about double the capacity of its factories while shutting down several obsolete facilities, according to Craig Barrett, head of manufacturing for Intel. Intel's strategy incorporates three basic elements for achieving a world-class manufacturing operation: increased plant efficiency, enhanced equipment utilization, and higher manufacturing yields.

- Plant efficiency was improved by closing three older plants and operating the remaining eight wafer fabrication and assembly facilities on extended work weeks. Plants now are designed to run 24 hours per day, 6 or 7 days per week. Intel gave frontline operators responsibility for tasks such as material movements and minor equipment repairs; it also installed computer controls to monitor inventories and work in process.
- Equipment utilization was further enhanced by revamping vendor relationships. Instead of trying to characterize new equipment on a production line, Intel now sets aside clean rooms for that purpose and encourages vendors to take on more of that responsibility. Through a new "key supplier" program, Intel tries to deal with a few important vendors almost as if they were part of the same company.
- Manufacturing yields were raised in part by stressing statistical process control techniques and insisting that technology development engineers consider manufacturability as a design goal. Defect density, a crucial determinant of yields in semiconductor production, was reduced both by using traditional efforts to clean up the manufacturing environment and by employing new computer technology to model and improve the manufacturing process.

The upshot of these efforts, according to Mr. Barrett, has been to make domestic semiconductor manufacturing fully competitive again. With direct labor costs driven below 10 percent as a contributor to product cost, he argues, "the only reason to go offshore (for manufacturing) now would be to satisfy a local market requirement."

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Research *Newsletter*

CAPITAL SPENDING PLANS LOOK STRONG FOR 1988

SUMMARY

The stock market plunge of October 19, 1987, caused most economists to lower their projections for economic growth in 1988. But a survey conducted after the crash by The Dun & Bradstreet Corporation, Dataquest's corporate parent, indicates that most U.S. companies are not cutting back their spending plans for new capital equipment and facilities. Instead, three quarters of the companies surveyed expect to maintain or increase capital spending in 1988. Together with Dataquest surveys of client companies and a recent U.S. Commerce Department forecast of capital spending intentions, the Dun & Bradstreet survey buttresses the view that 1988 will be a strong growth year for those high-technology markets that are closely linked to the capital investments of Corporate America.

SURVEY RESULTS

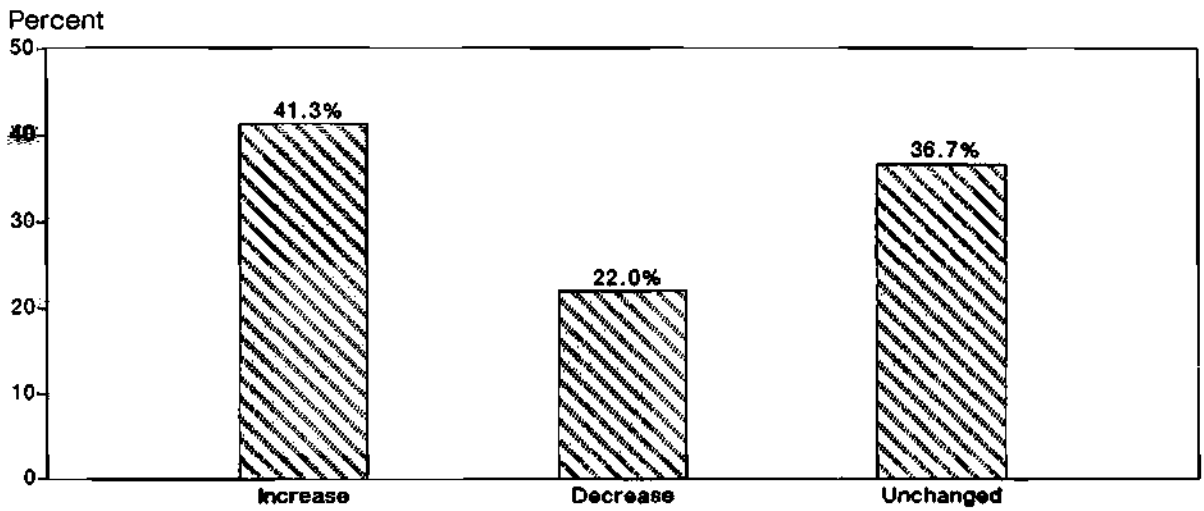
Dun & Bradstreet's Dun's 5000 survey is based on a sample of companies that is statistically representative of the distribution of companies by size in the U.S. economy. Of the companies surveyed, only 22 percent indicated they plan to decrease their capital spending in 1988 from 1987 levels, a solid 36.7 percent expect no change, and 41.3 percent are planning capital spending increases (Figure 1). These gains reflect the continuation of a trend that began last year, according to Joseph W. Duncan, Dun & Bradstreet's corporate economist. Mr. Duncan pointed out that almost 25.0 percent of the companies surveyed spent more than they had planned in 1987, while only 17.2 percent saw their spending come in lower than expected (Figure 2).

Only 8.4 percent of the Dun's 5000 respondents said the decline in stock prices would have a negative impact on their capital spending. But nearly 16 percent of small companies—those with fewer than 20 workers—said the crash would crimp their plans (Figure 3). And, looking at spending intentions by size of firm shows a far more bullish mood among large companies than is reflected in the small-business sector (Figure 4). Because of their need to carefully manage financial resources, explained Mr. Duncan, "small companies are more likely to reduce spending during periods of uncertainty."

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 437-8000, Telex 171973, Fax (408) 437-0292

Figure 1

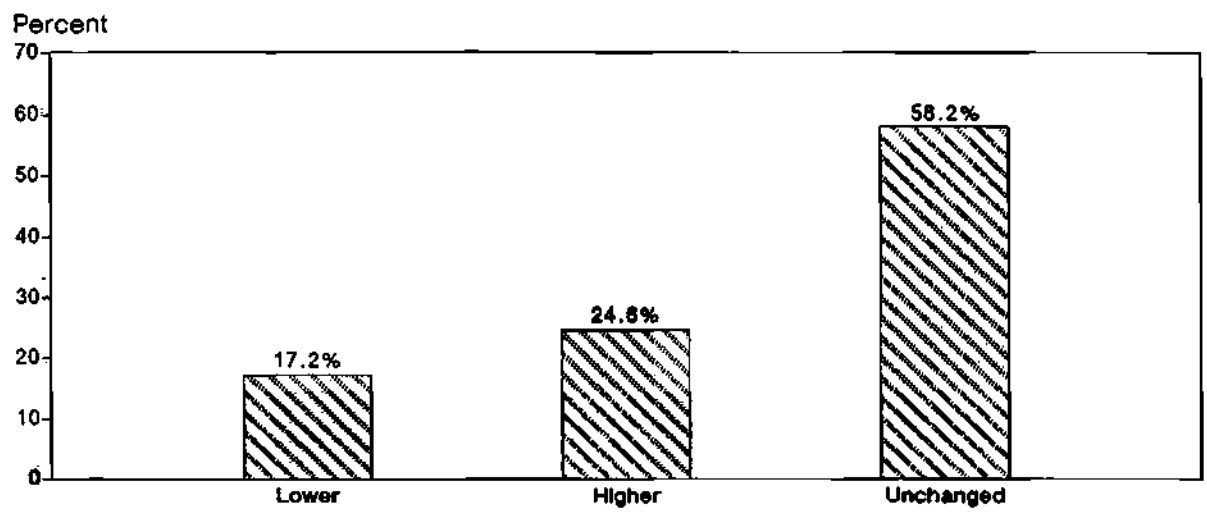
Capital Spending Plans
1988 versus 1987



Source: Dun & Bradstreet

Figure 2

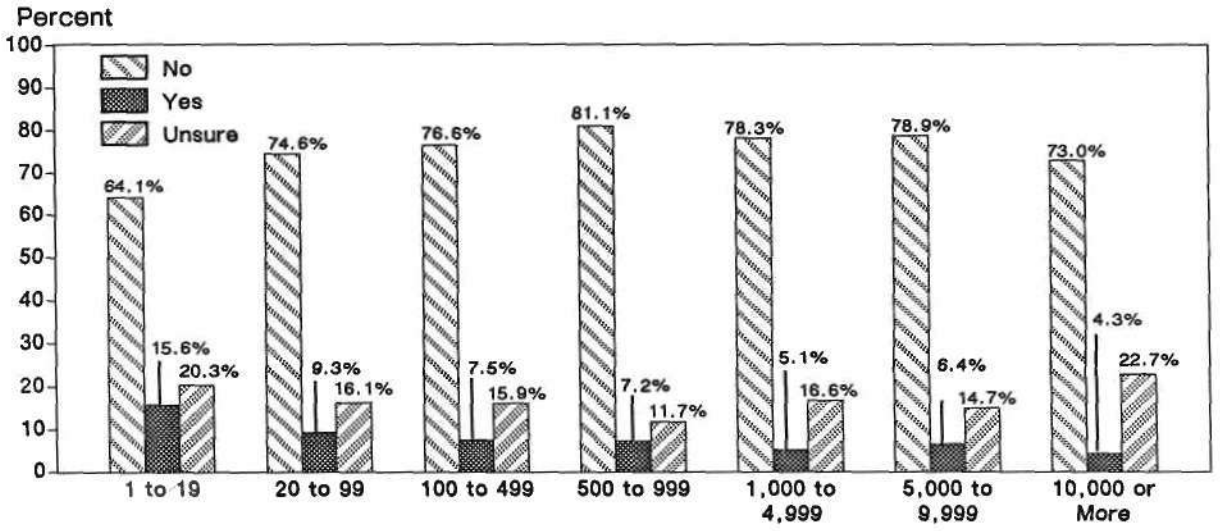
1987 Capital Spending
Actual versus Planned



Source: Dun & Bradstreet

Figure 3

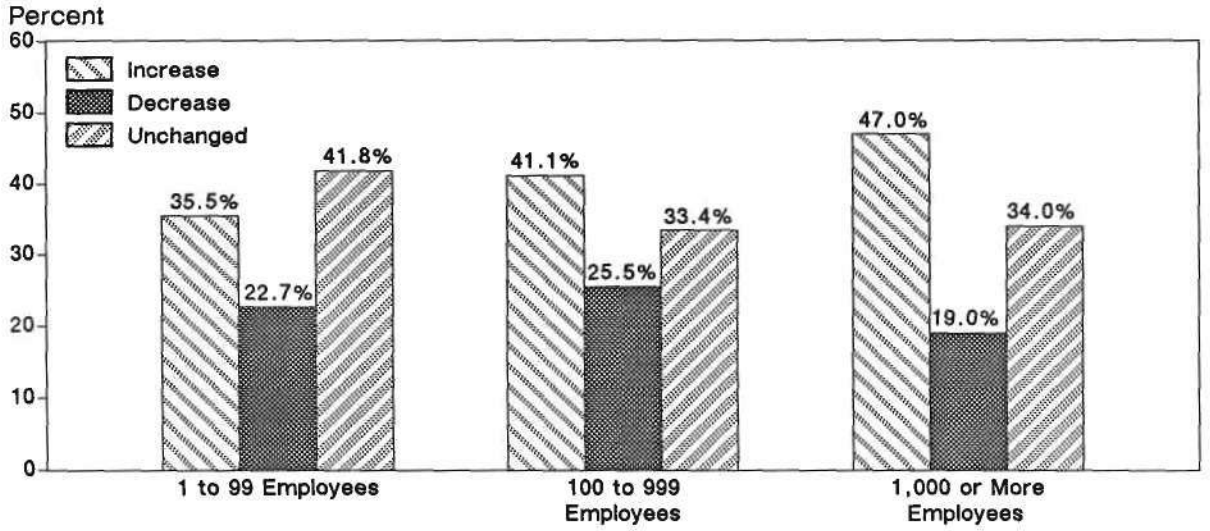
Will Stock Market Crash Have Negative Impact on Spending? (By Company Size)



Source: Dun & Bradstreet

Figure 4

Capital Spending Plans 1988 versus 1987 by Company Size

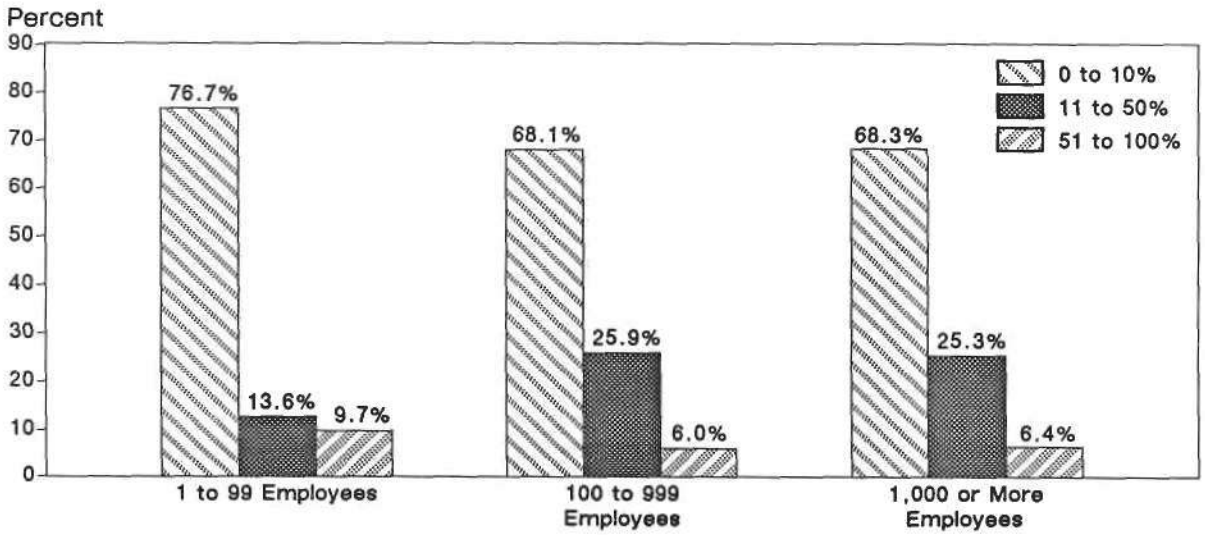


Source: Dun & Bradstreet Dataquest January 1988

Small companies are a hard sell for another reason: According to the survey, they allocate less of their capital budgets to computers and telecommunications equipment than larger firms (Figure 5).

Figure 5

Budget Allocation for Computers and Telecommunications Equipment by Company Size

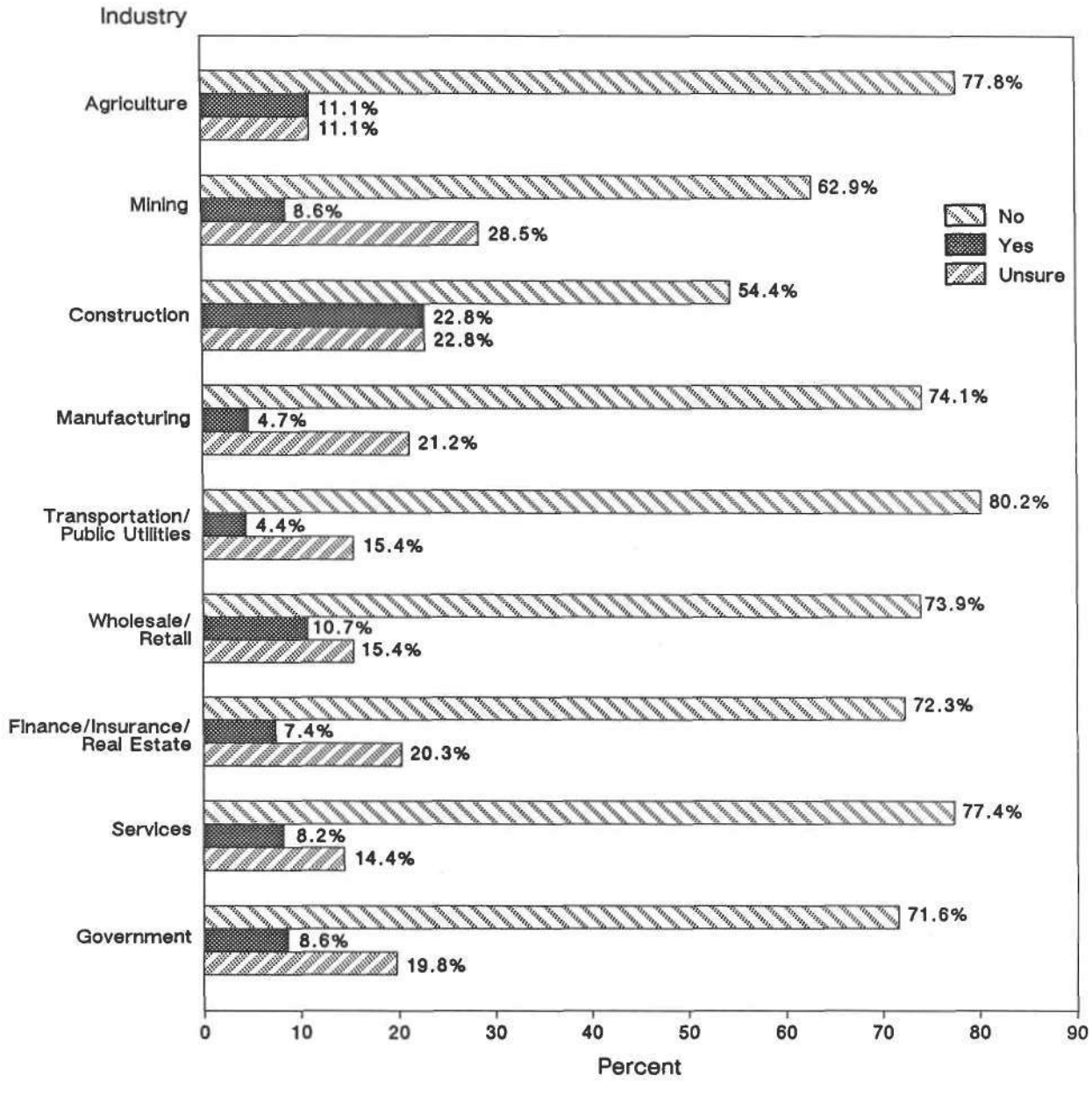


Source: Dun & Bradstreet
Dataquest
January 1988

The survey turned up few disparities in spending intentions among industry sectors. Construction companies, which were more likely than other companies to cut capital budgets in 1987, felt the largest impact from the stock crash (Figure 6). On the other hand, plans for increased spending in 1988 were fairly uniform across industries (Figure 7). While 41.3 percent of the manufacturers surveyed plan to increase spending, even more service companies, transportation companies, and utilities also expect higher capital outlays. But there are marked sectoral differences in the share of capital spending budgets devoted to information systems. Computers loom largest in the plans of financial, real estate, and insurance companies. Almost all the construction, mining and agricultural firms devote 10 percent or less of their capital budgets to computers and telecommunications equipment (Figure 8).

Figure 6

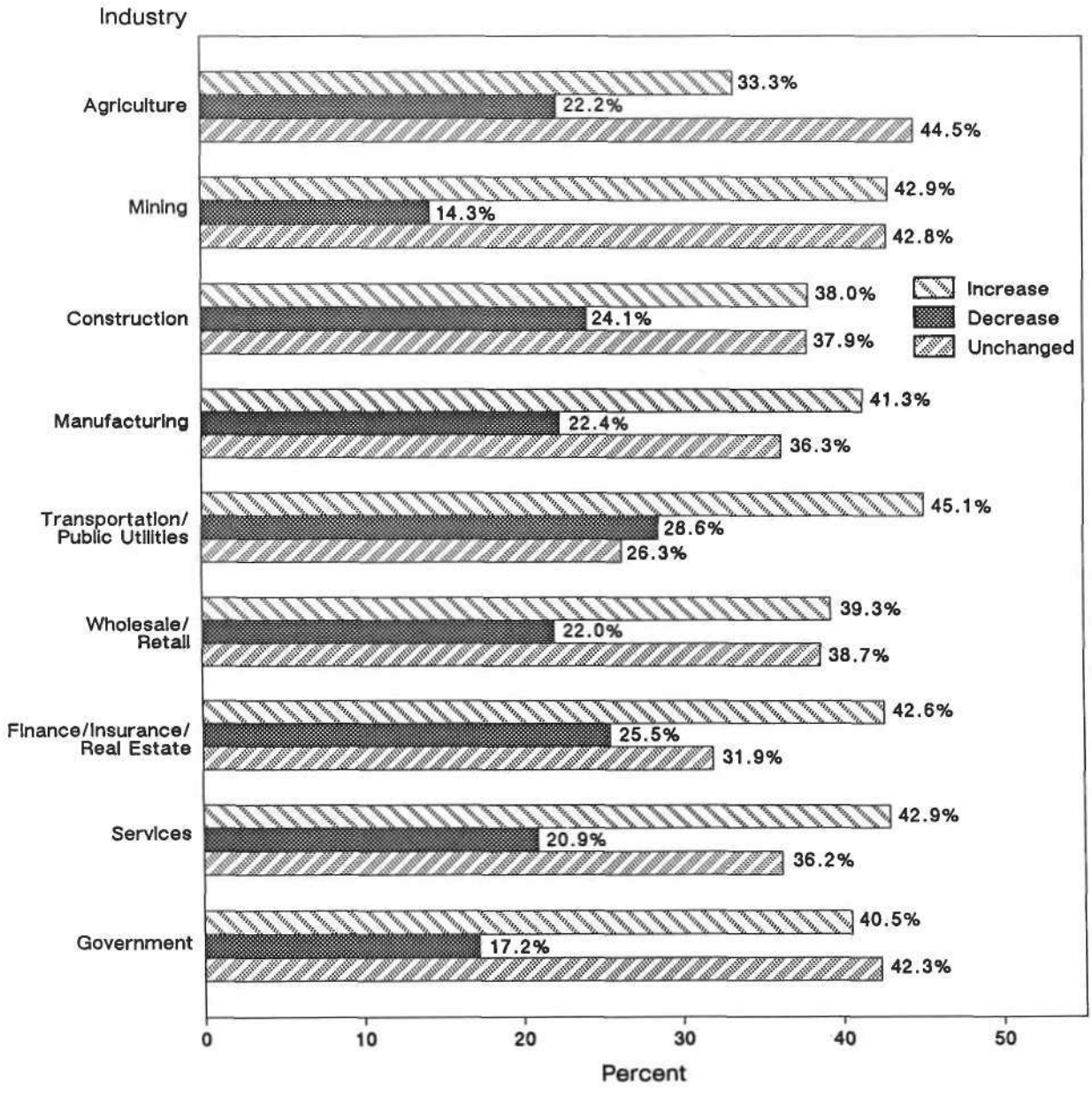
Will Stock Market Crash Have Negative Impact on Spending by Industry?



Source: Dun & Bradstreet

Figure 7

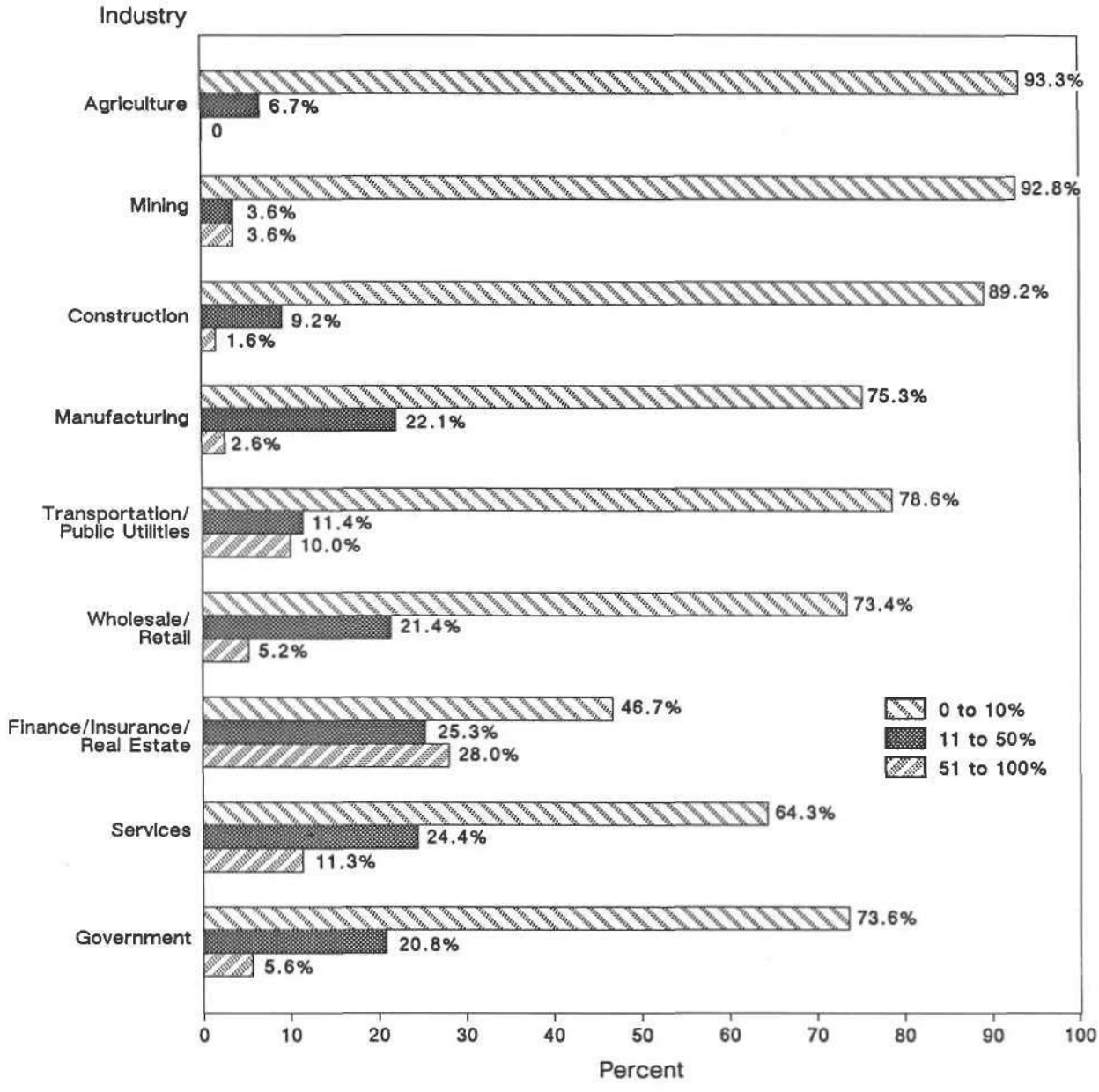
Capital Spending Plans
1988 versus 1987
by Industry



Source: Dun & Bradstreet
Dataquest
January 1988

Figure 8

Budget Allocation for Computers and Telecommunications Equipment by Industry



Source: Dun & Bradstreet
Dataquest
January 1988

OTHER INDICATORS

The Dun's 5000 survey is only the latest in a series of indicators pointing toward strong U.S. demand for capital equipment this year. The Commerce Department reported in mid-December that U.S. companies are planning to increase capital spending by 7.3 percent in 1988. That is more than three times the estimated 2.3 percent rise in 1987. According to the Commerce Department survey, manufacturers will lead the way with an 8.6 percent increase in capital spending.

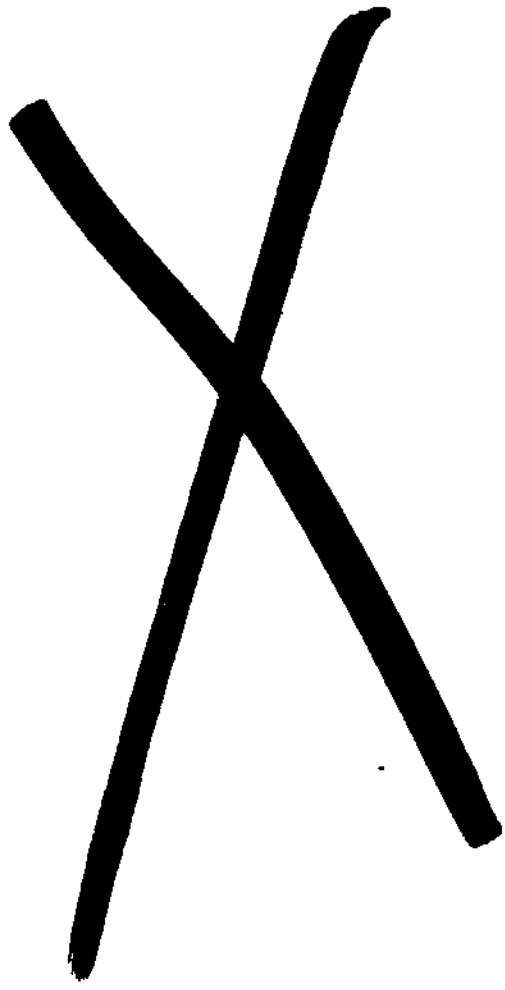
Dataquest's survey of chief financial officers, reported to clients in late November, also predicted that buyers of electronics equipment would ignore the market crash. Another important indicator of strength came in December, when Dataquest's Personal Computer Industry Service surveyed four major personal computer retailers, representing more than 1,500 U.S. outlets. The chains reported that December sales were up 20 to 25 percent over December of 1986, and their growth expectations for the first quarter of 1988 ranged from 12 to 28 percent.

DATAQUEST CONCLUSIONS

It is clear that manufacturing industries in the United States are booming and that the market crash has had little or no immediate impact on their prospects. Although domestic spending has slowed from the strong growth pace of the last few years, the sharp decline of the dollar has vastly improved export prospects for many industries. Capacity utilization, at 82 percent in November, is tighter than it has been in almost a decade. Manufacturers' profits are strong—up 19 percent from the second quarter to the third quarter of 1987—and are expected to keep improving. As a result, companies across a wide range of industry sectors are committing to long-postponed expansion and modernization projects. The Dun's 5000 survey shows that service companies are also gearing up for capital projects.

Dataquest believes that vendors positioned to take advantage of an upsurge in capital spending will prosper in 1988. The cloud of uncertainty that was created by the market crash has been all but dispelled. Dangers still lurk in the potential for higher interest rates if the dollar resumes its free-fall or if inflation heats up. And, a delayed consumer reaction to the woes of Wall Street is still possible. But the combination of a healthy capital spending climate and a presidential election means that for most Dataquest clients, 1988 should be a year to remember.

John W. Wilson
Bernadette Joseph
Dataquest Corporate Research



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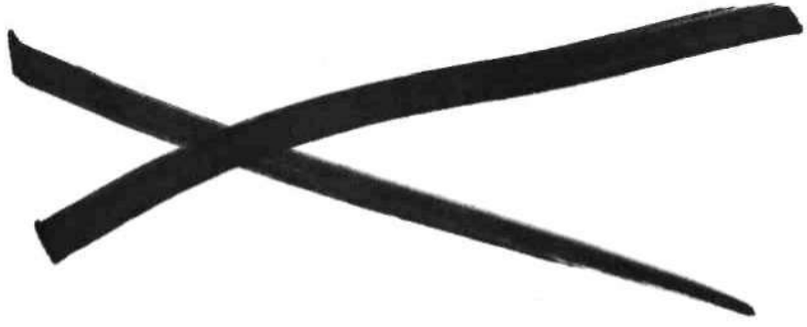

1987–1988 SEMS Newsletter Index

The 1987-1988 SEMS Newsletter Index is a quick reference guide to the SEMS newsletters. It is structured as follows:

- Titles are organized by both subject and company.
  - The first part is a company list, e.g., LSI Logic.
  - The second part is a subject list, e.g., Memory.
- The newsletter month and year follow each title listing in the index. Refer to the month tab to locate a specific newsletter.

This index is updated quarterly.

1987–1988 SEMS Newsletter Index

Company	Newsletter	Date
ADVANCED MICRO DEVICES		
	Capital Spending in North America: Survey Results Point to Lift-Off in 1987	Jan. 87
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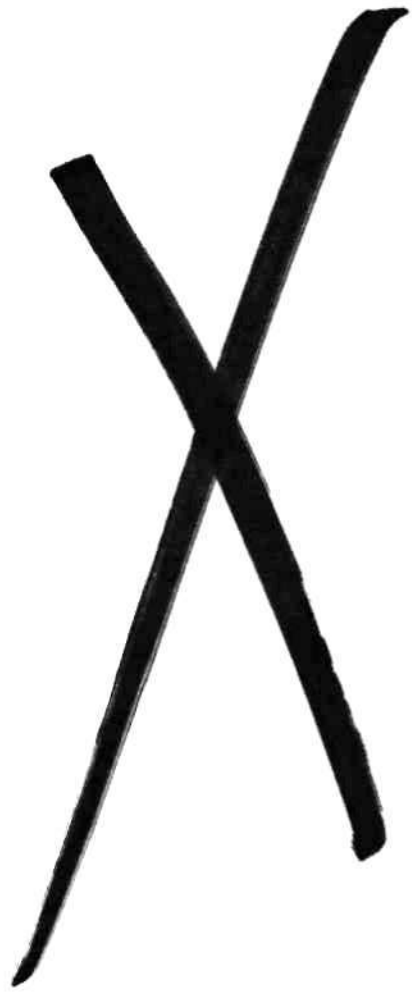


January Newsletters

The following is a list of newsletters found in this section:

Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987–1988 Newsletters: January 1988–1

HOW TO INCREASE SEMICONDUCTOR MARKET SHARE: INCREASE THE INSTALLED BASE

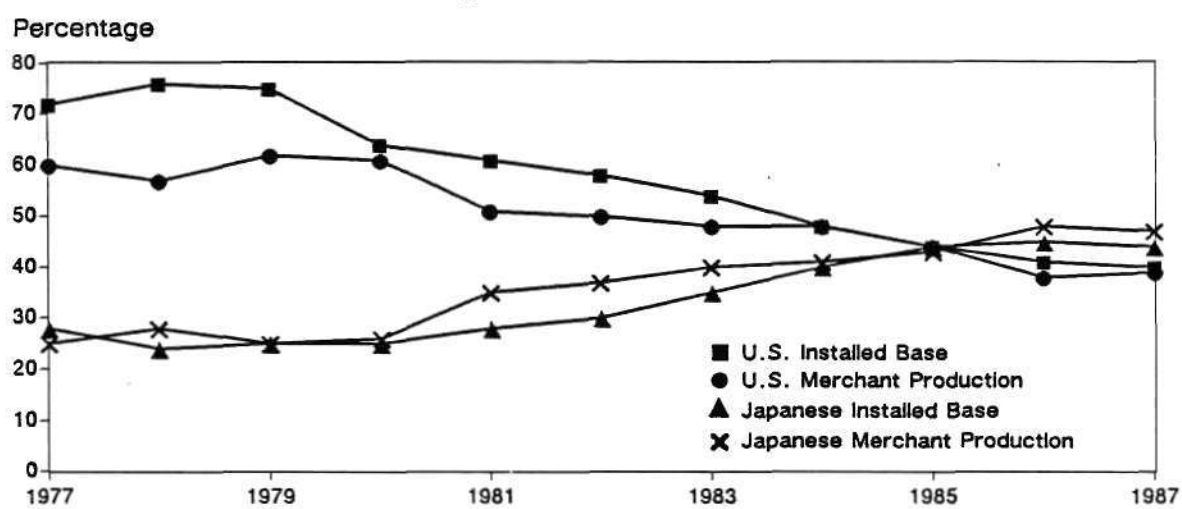
SUMMARY

A country's market share depends on the size of its installed base. A company's market share depends on how wisely it uses what it has. There is a direct correlation between a region's capital spending, installed base, and market share. Put very simply, as the installed base goes, so does market share. Figure 1 shows market share and share of worldwide productive capacity for both the United States and Japan. Productive capacity is measured in dollars worth of property, plant, and equipment (PPE).

The relationship between the size of the installed base and market share holds true on an individual company level also, although other variables such as product differentiation, process complexity, and clean room practices may increase or decrease the efficiency of a company's PPE.

Figure 1

Worldwide Share of PPE and Market Share
Japan and the United States



Source: Dataquest
January 1988

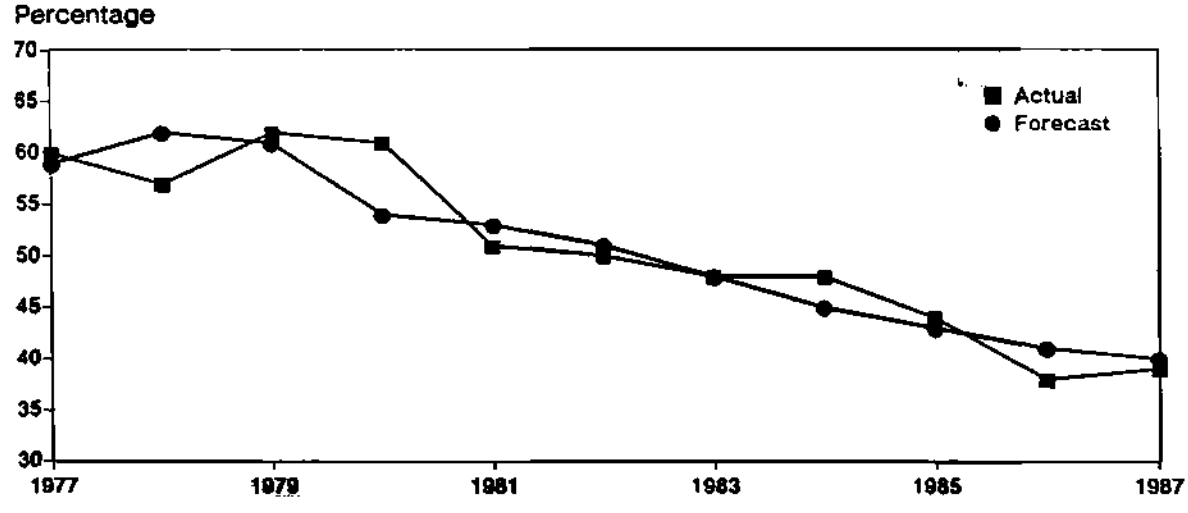
REGIONAL INSTALLED BASE

A region's installed base of PPE is the bone and sinew upon which the muscle of market share must be developed. Japanese merchant companies started out the decade of the '80s with a market share that was less than one-half of their U.S. counterparts' share: 25 percent versus 64 percent in 1980. However, from 1977 to 1987, Japan's installed base grew at a compound annual growth rate (CAGR) of 35 percent, while the installed base of U.S. manufacturers grew at a lower rate of 22 percent. The result of this differential growth was that, by 1985, the productive capacity of Japanese companies matched that of the U.S. merchants. By 1987, Japanese and U.S. market shares were 44 percent and 40 percent, respectively. Market share growth springs from an increased share of worldwide PPE.

The correlation between share of PPE and market share is quite high. Figure 2 shows the comparison between the forecast historical regional market share, using share of installed base as the independent variable and actual regional historical market share. Using this relationship and our capital spending forecast, we have forecast the market share of the major regions of the world. (See the SEMS service section, "Production," May 1987, in the Industry Econometrics binder. Figure 3 shows our forecast of the market share of ROW companies from 1988 through 1992. Pulled by a quickly growing installed base, we expect the ROW's market share to shoot up from 2.5 percent in 1987 to almost 9.0 percent in 1992.

Figure 2

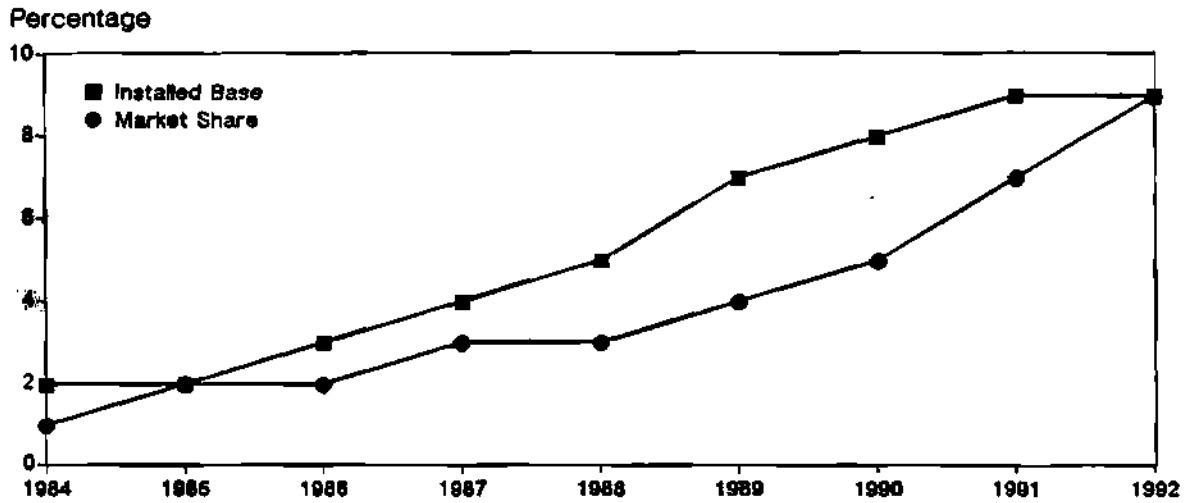
Actual and Forecast U.S. Historical Market Share



Source: Dataquest January 1988

Figure 3

Installed Base and Market Share for ROW



Source: Dataquest
January 1988

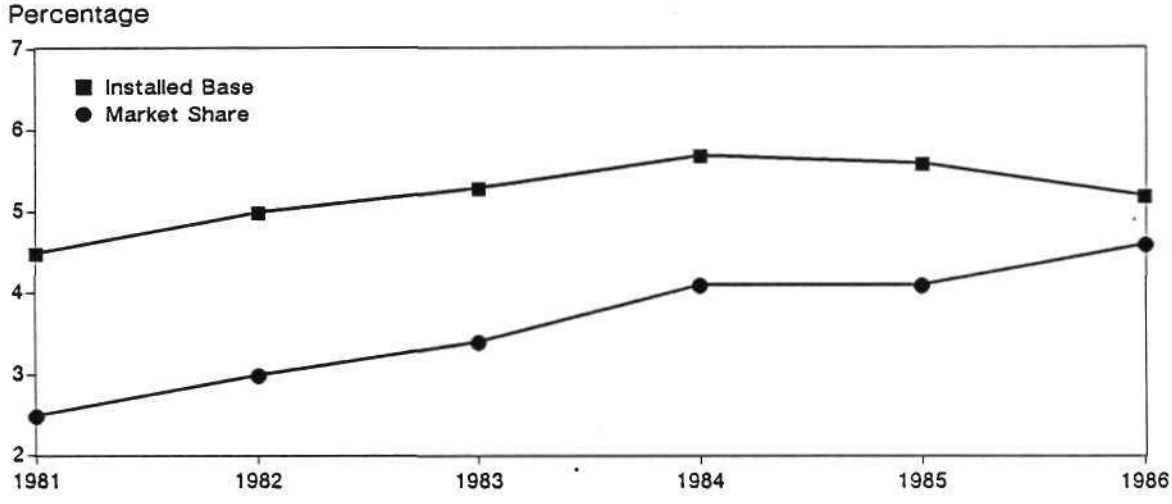
COMPANY MARKET SHARE AND INSTALLED BASE

Figures 4 through 16 show our estimates of worldwide market share and share of worldwide productive capacity for major U.S. and Japanese merchants. In general, company market share and share of PPE move in the same direction. The Japanese companies' market share and share of productive capacity have moved up, while those of U.S. companies have tended to move down.

However, the relationship between market share and PPE on a company level is not one to one. Because of product differentiation, market niche strategies, and effective application of manufacturing science on the fab floor, companies do vary in how efficiently they use their PPE. Several companies have been able to maintain market shares that are higher than their share of the world's PPE. For example, Hitachi, Motorola, National Semiconductor, NEC, Philips/Signetics in the United States, and Texas Instruments, have rather consistently outperformed their productive capacities. Intel, while its market share has not exceeded its share of PPE, has been able to increase its market share, even as its share of PPE has declined.

Figure 4

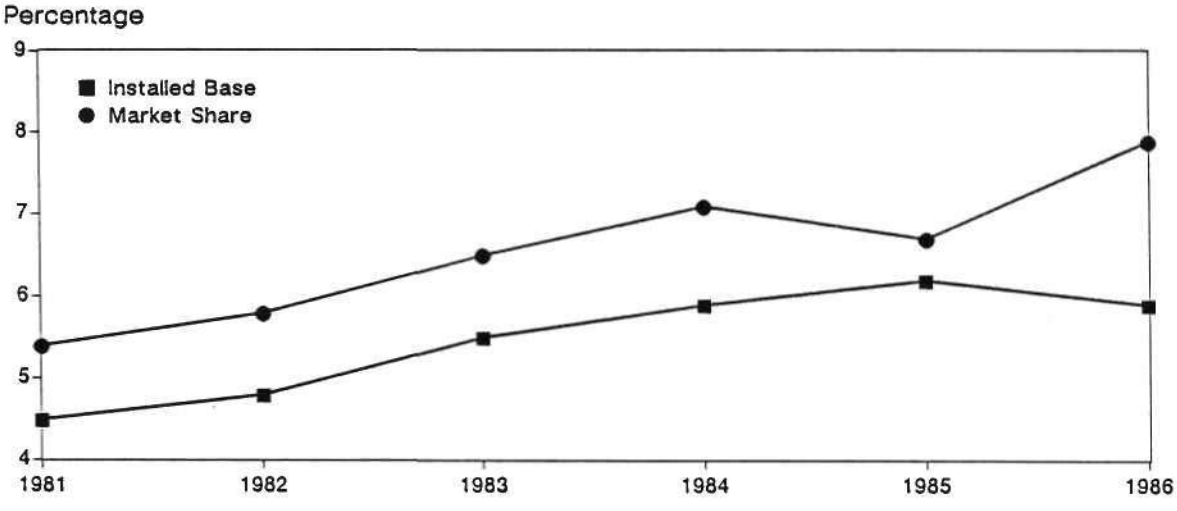
Fujitsu Installed Base versus Worldwide Market Share



Source: Dataquest
January 1988

Figure 5

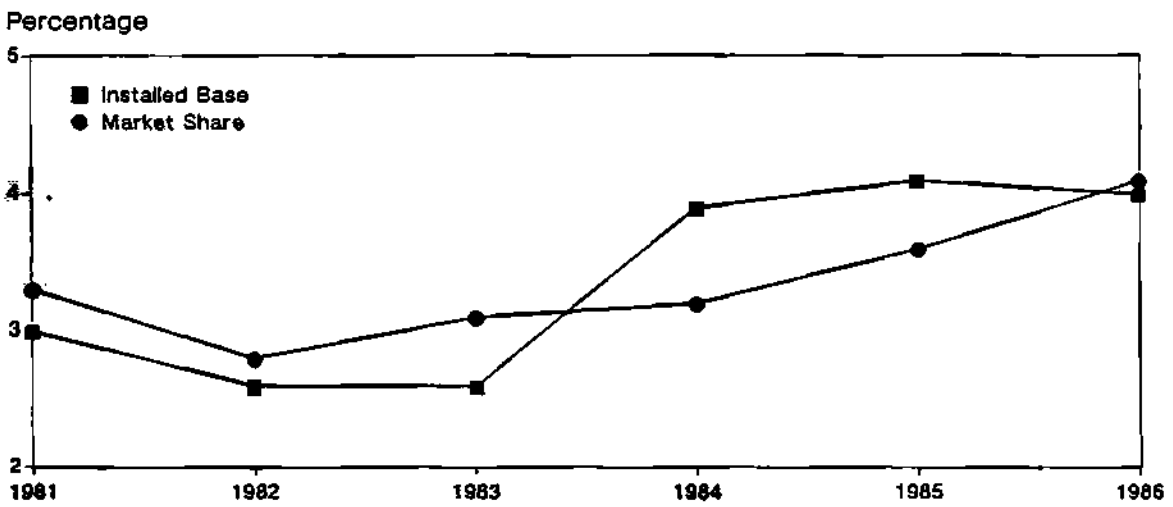
Hitachi Installed Base versus Worldwide Market Share



Source: Dataquest
January 1988

Figure 6

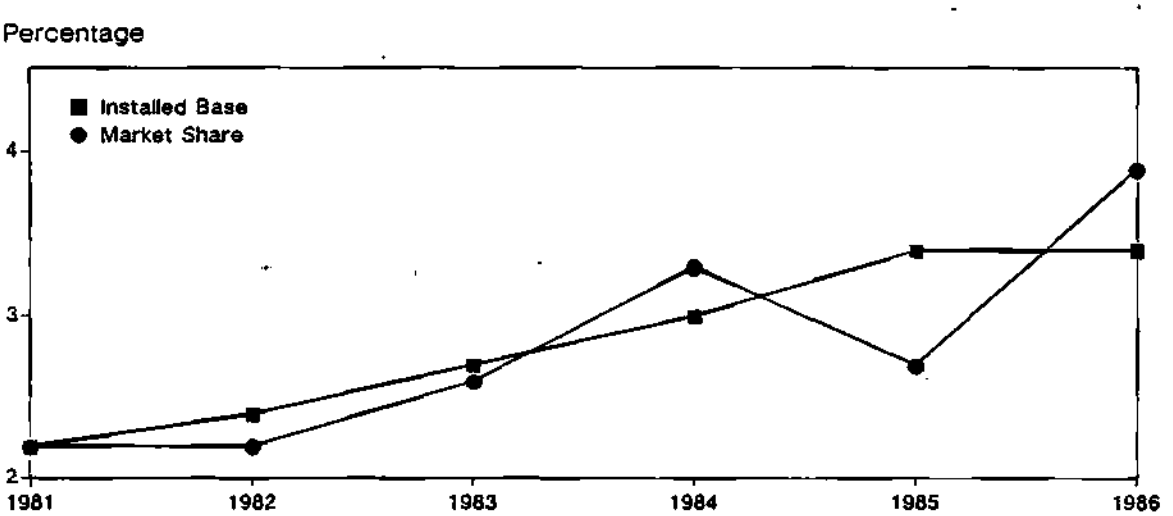
Matsushita Installed Base versus Worldwide Market Share



Source: Dataquest
January 1988

Figure 7

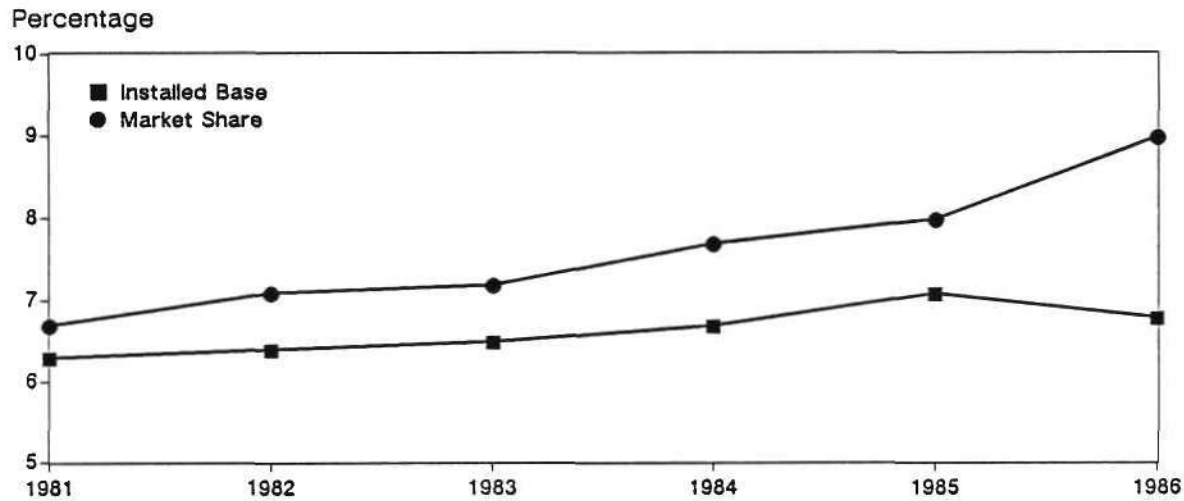
Mitsubishi Installed Base versus Worldwide Market Share



Source: Dataquest
January 1988

Figure 8

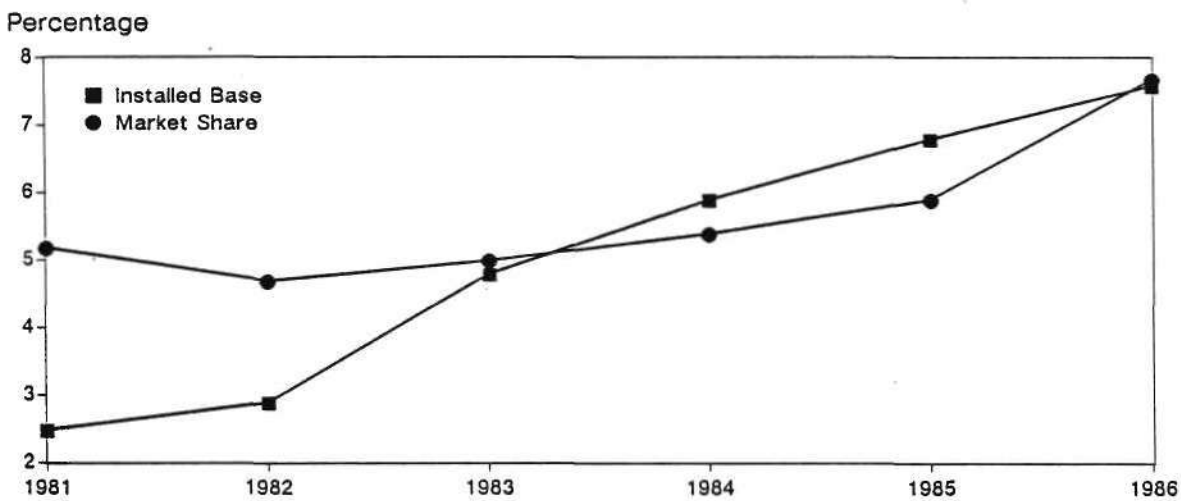
NEC Installed Base versus Worldwide Market Share



Source: Dataquest
January 1988

Figure 9

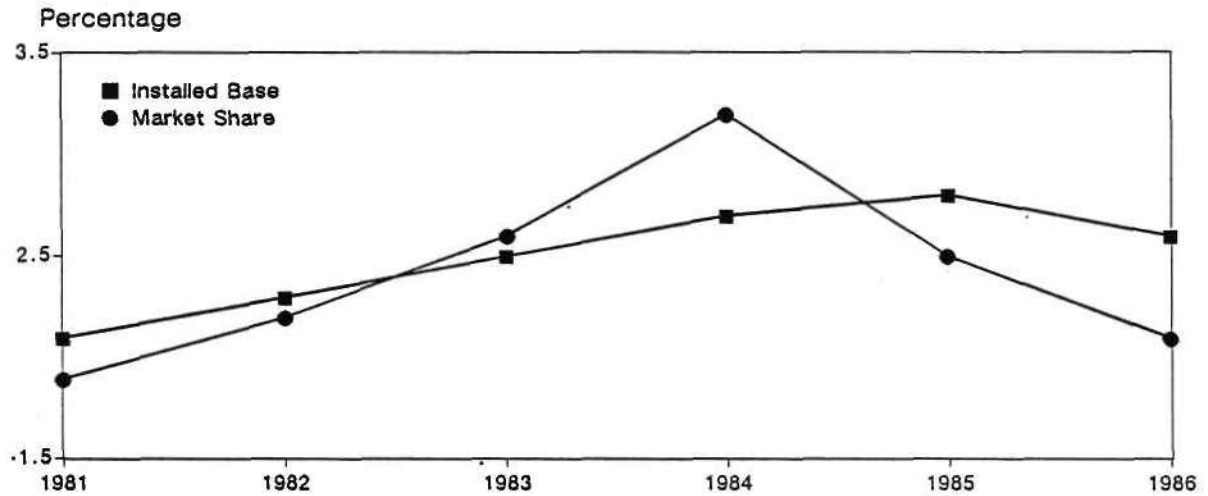
Toshiba Installed Base versus Worldwide Market Share



Source: Dataquest
January 1988

Figure 10

AMD Installed Base versus Worldwide Market Share

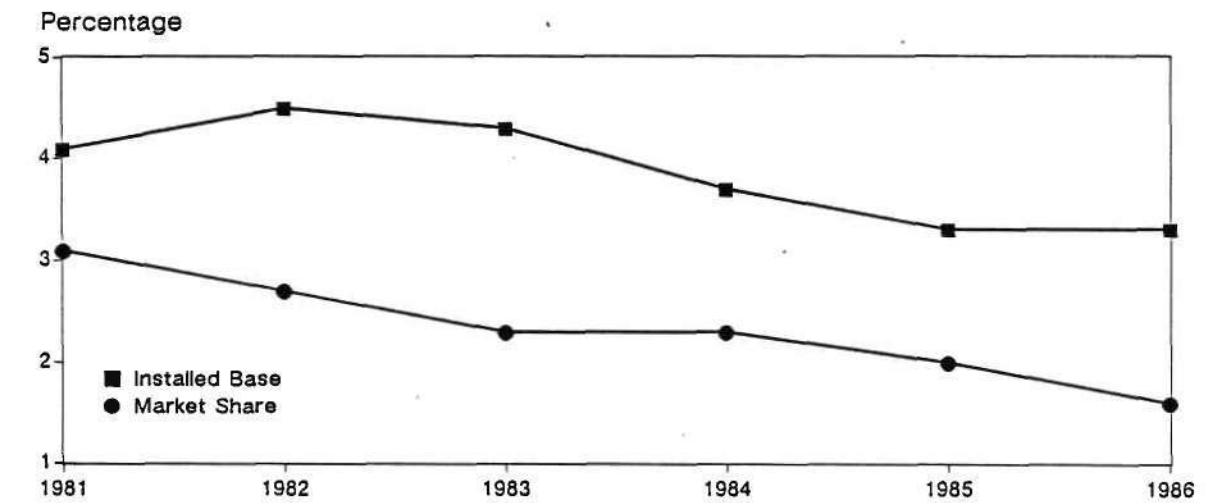


*Does not include PPE and market share for MMI

Source: Dataquest
January 1988

Figure 11

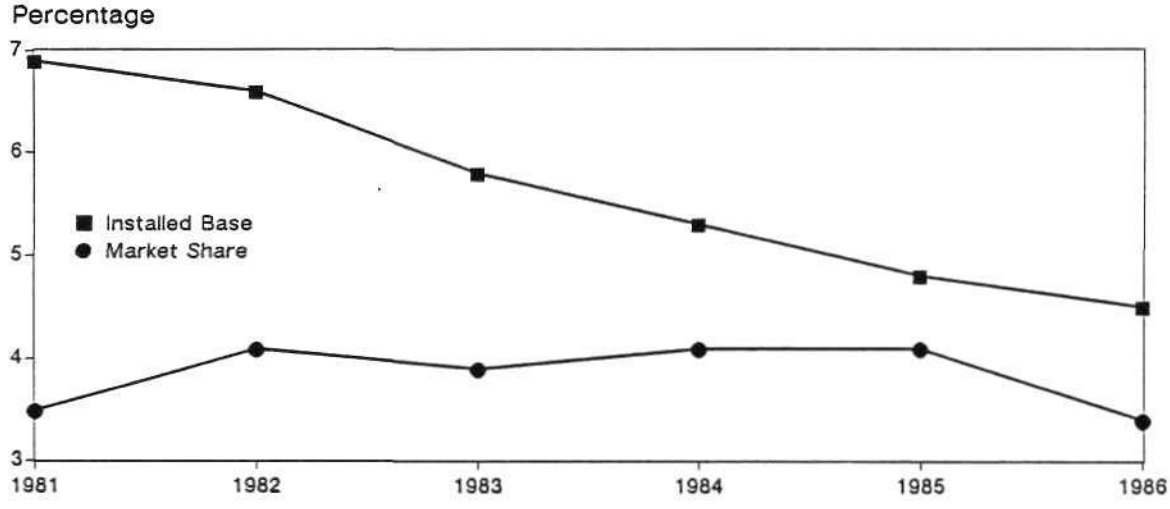
Fairchild Installed Base versus Worldwide Market Share



Source: Dataquest
January 1988

Figure 12

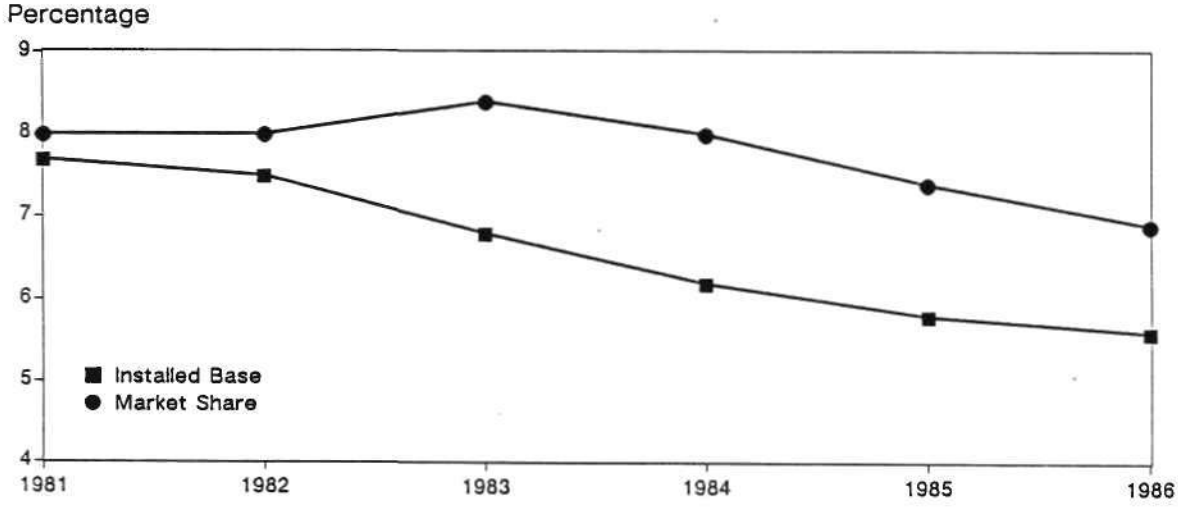
Intel Installed Base versus Worldwide Market Share



Source: Dataquest
January 1988

Figure 13

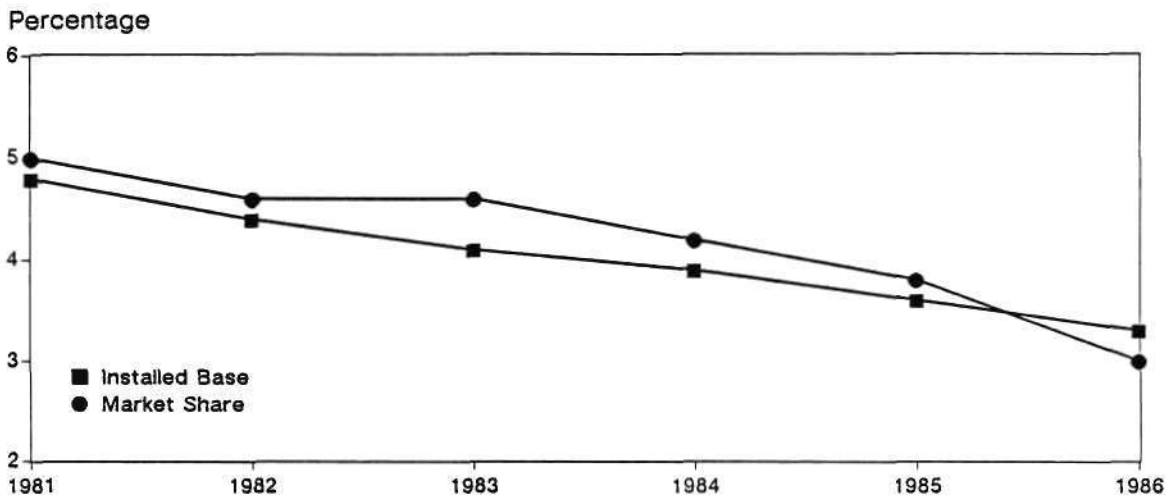
Motorola Installed Base versus Worldwide Market Share



Source: Dataquest
January 1988

Figure 14

National Semiconductor Installed Base versus Worldwide Market Share*

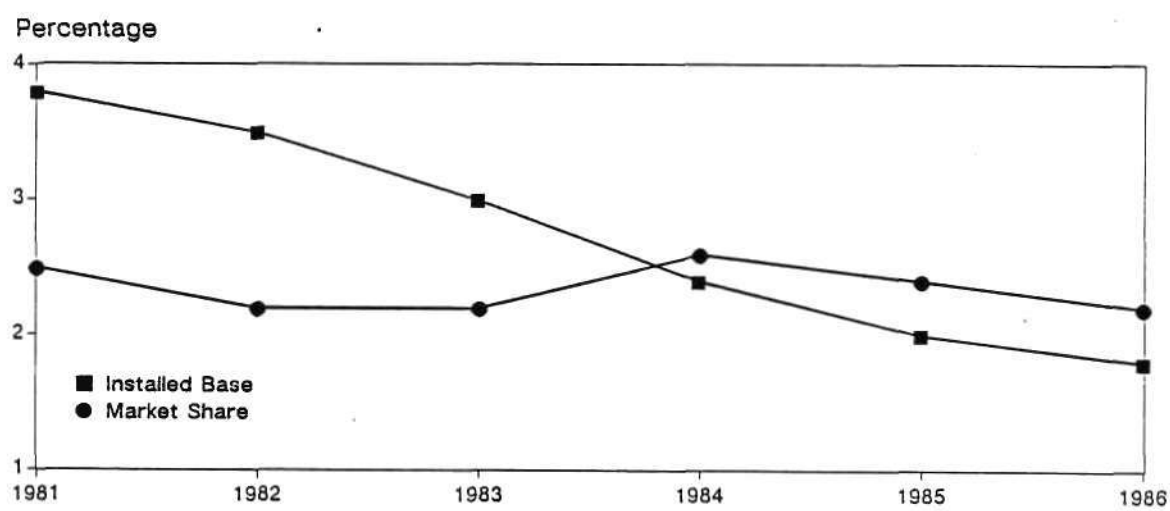


*Installed base and market share do not include Fairchild.

Source: Dataquest January 1988

Figure 15

Philips/Signetics Installed Base versus Worldwide Market Share*

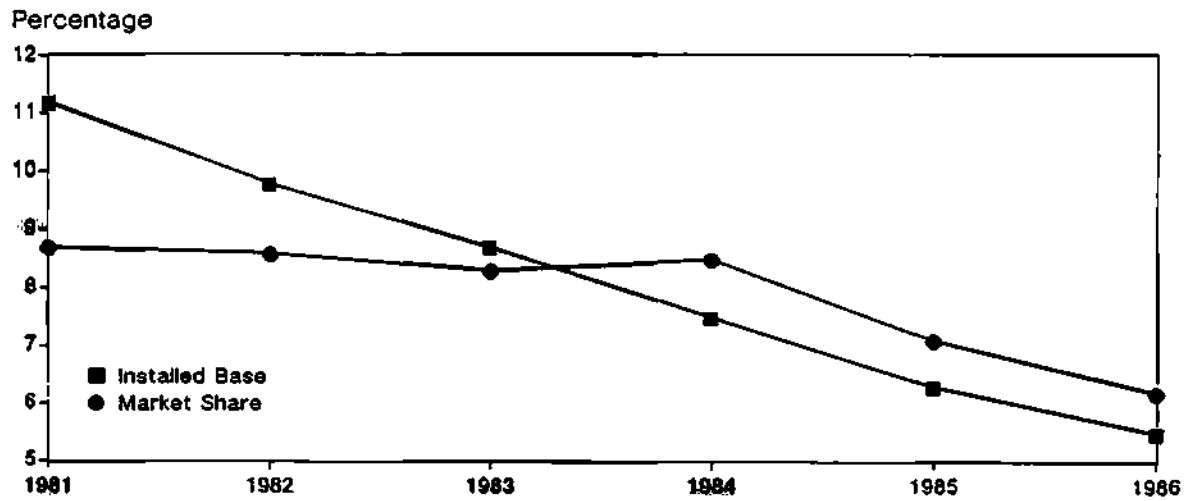


*Refers to installed base and worldwide market share of U.S. facilities only.

Source: Dataquest January 1988

Figure 16

Texas Instruments Installed Base versus Worldwide Market Share



Source: Dataquest
January 1988

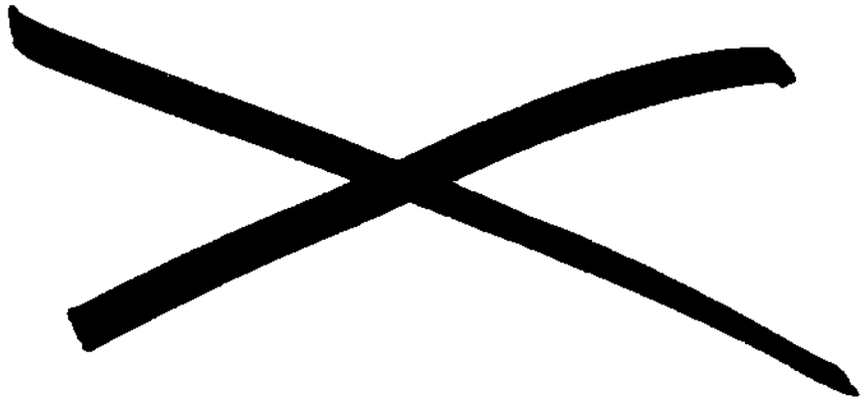
CONCLUSIONS

On a regional basis, size of market share is determined mainly by a region's share of the worldwide productive base. Regional market share follows from a commitment to investment. Government policy that seeks to maintain or nourish its domestic industry as a major player on the world market can do so by fostering an environment favorable to capital formation.

A company's market share is also, to a large extent, determined by its commitment to investment—its share of the world's productive assets—though, as previously noted, other variables also play a part. Government policy can be helpful on this level also. It can encourage basic R&D from which new products flow. An example of this is the next-generation computer project in Japan. It can also encourage manufacturing science, which will increase the efficiency of how manufacturing resources are used. Sematech, for example, is attempting such a project in the United States.

A large installed base is the foundation of a healthy industry. Governments can provide a nourishing and favorable environment for the formation of productive assets and their efficient use. Individual companies, however, have to provide the vision to use their productive resources wisely. Those companies that have unique products and can use their PPE efficiently will gain market share when they expand their share of installed base.

George Burns



February Newsletters

The following is a list of newsletters found in this section:

Dataquest
a company of
The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987–1988 Newsletters February
1988–5

SECS UPDATE: SEMICONDUCTOR MANUFACTURERS GET INVOLVED

On February 2, 1988, the SECS Implementation Task Force (SITF) presented its first public report on its past work and future plans for reducing disparity among end–user requirements and equipment manufacturers' implementations of the SEMI Equipment Communications Standard (SECS protocol). The SITF has specifically targeted the following three projects:

- Generic SECS II guidelines for semiconductor processing equipment
- SECS II guidelines for 18 specific equipment categories
- An education program for the equipment and end–user communities

Dataquest believes that this joint program among seven major semiconductor companies represents a significant level of cooperation and commitment in the end–user community. In addition, the successful adoption of SITF recommendations will minimize the number of dollars and hours currently invested in equipment communications programs. Equipment communications represents one of the essential cornerstones upon which factory automation programs are built. Dataquest believes that the guidelines being developed today by the SITF warrant the attention of our clients in all segments of the semiconductor industry.

A REVIEW OF SECS

SECS was proposed and developed by the Semiconductor Equipment and Materials Institute (SEMI) as a communications protocol for the semiconductor manufacturing environment. SECS is designed to provide communications capabilities between computers in semiconductor processing equipment and upstream node or host computers.

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 437-8000, Telex 171973, Fax (408) 437-0292

One part of the SECS protocol, known as SECS II, specifies a general message set for all communications and transactions. As Dataquest's Semiconductor Equipment and Materials Service (SEMS) reported in May 1986, a majority of front-end processing equipment today is SECS II-compatible. However, a great deal of variety exists in the interpretation and number of messages that equipment manufacturers have chosen to specify for their equipment. This is because most semiconductor manufacturers, while requiring SECS compatibility, have provided little, if any, direction and few guidelines for their equipment vendors.

In a sense, the SECS protocol provides the tools for building a communications environment in the fab, just as a hammer, nails, and two-by-fours are required for building a house. A set of tools, however, can be used to build a shack or a chateau, depending upon the blueprints and the building code. While every semiconductor manufacturer will have its own blueprints for factory automation, the SITF believes that the industry needs a uniform building code—in essence, an industry-recommended practice for building the communications environment between processing equipment and cell-level or host-level computers in the fab.

FROM A CONVERSATION AT LUNCH . . .

The seeds for a SECS implementation task force literally were planted during a conversation at lunch among several equipment and semiconductor manufacturers attending a February 1986 SEMI technical symposium on effective manufacturing implementation of the SECS protocol. Disgruntled equipment manufacturers raised the often-heard complaints that semiconductor manufacturers were not telling their vendors what they wanted; if they did know what they wanted, then every semiconductor manufacturer wanted something different. Equipment vendor resources were being strained to the limit while equipment companies were trying to meet the vague and varied requirements of their customers.

In response to the grumbles at that February luncheon, several semiconductor manufacturers joined together to establish a SECS Users Committee. The SECS Users Committee, as part of the SEMI Communications Committee, has grown substantially from the handful of founding member companies. Working plans were developed in February 1987 for a smaller task force to focus specifically on guidelines for SECS implementation, and the SITF member companies held their first meeting two months later.

WHO IS SITTING AT THE TABLE?

The SITF member companies are as follows:

- AT&T
- IBM
- Intel
- Motorola
- National Semiconductor
- Siemens
- Texas Instruments

As part of the committee bylaws, membership is limited to just seven companies, and a member company can be removed if its representative misses more than two meetings in a row. In addition, the designated representatives from a given company are limited to only a handful of individuals in order that the SITF can move rapidly while maintaining continuity in the development of SECS guidelines. Representatives from member companies have been meeting for two-day sessions every six weeks since the first meeting in April 1987. Beginning in March 1988, the SITF will meet for three-day sessions every eight weeks. Each member company has been responsible for developing specific aspects of the SECS implementation guidelines, such as material handling, recipe management, and equipment terminal communications. Dataquest believes that this effort represents a substantial commitment of manpower and resources from the SITF member companies.

While the core membership of the SITF is closed, the committee strongly welcomes input from a variety of different groups, including the SEMI Communications Committee, the SEMI SECS Users Committee (including the Cell Task Force and Material Movement Task Force), and the equipment vendor community directly. In general, the philosophy of the SITF is to stay lean through limited membership, meet frequently, achieve group consensus, and interact with other task forces, primarily through the SEMI organization.

SITF TARGETS

The SITF has focused on three specific projects: a set of generic SECS II guidelines for semiconductor processing equipment, a subset of SECS II messages for specific types of processing equipment, and a program of education for the equipment vendor and end-user communities. The general SITF process for the development of both generic and equipment-specific models includes the following steps:

- Analyze equipment capability
- Establish group consensus among SITF member companies
- Develop scenario to support equipment capability
- Extract SECS II message subset
- Develop factory operations script
- Undergo industry review
- Update and revision by the SITF
- Publish guidelines through SEMI
- Present education program

The SITF has taken a position that its primary objective is to choose SECS II messages that already exist within the protocol. However, there will be situations in which custom messages are developed as substitutes for awkward or inefficient transactions of existing message sets.

Generic Equipment Model

The first SITF project was the design of a generic equipment model for equipment communications in the semiconductor processing environment. An important part of that development was an analysis of the fundamental elements of equipment functionality and capability necessary for equipment communications. These elements include the following:

- Abort operations
- Alarm management
- Data collection
- Equipment terminal communications
- Equipment initialization
- Local/remote operations
- Material transfer
- WIP tracking
- Recipe management
- Remote commands
- Error tracking

From that analysis, the SITF has chosen a subset of SECS II messages deemed essential for basic equipment communications. The generic equipment model also includes a factory operations script that outlines how a generic type of equipment and a cell–level controller will interact in the processing environment.

The SITF generic equipment model will be published by SEMI in the March/April 1988 time frame and can be obtained by contacting SEMI headquarters in Mountain View, California.

Specific Equipment Model

In addition to formulating generic SECS guidelines for processing equipment, the SITF has undertaken the development of SECS guidelines for specific types of processing equipment. The generic equipment model is used as a framework, but the specific equipment model also includes items that are specific to a given type of equipment. Twenty–four types of equipment in eighteen categories have been targeted. The equipment categories, listed alphabetically, are as follows:

- Automatic guided vehicles*
- Coater/developer
- Die attach
- Diffusion*
- Dry etch
- Epitaxy
- Functional test
- Ion implantation*
- Metrology equipment
- Parametric test
- Plastic encapsulation/mold
- Probe
- Sputter
- Stepper*
- Trim and form
- Wafer saw
- Wave solder
- Wire bonder*

The five equipment categories marked by an asterisk represent those categories of equipment that will receive initial priority in SECS guidelines development. The SITF plans to release the specific equipment models for all categories of equipment between April and August 1988. Like the generic equipment model, this information will be available through SEMI.

Vendor/End–User Education

The SITF recognizes that a technical education program for equipment and semiconductor manufacturers is essential for the successful adoption of SITF SECS guidelines. Committee members readily acknowledge that if no one ever understands the project, all their work will have been for naught. The SITF plans to hold two formal educational programs in May (during SEMICON/West) and September.

HOW WILL SITF HELP?

Equipment Vendors

Several important benefits of the SITF guidelines for equipment manufacturers are as follows:

- For equipment companies with minimal resources to dedicate to SECS protocol implementation for new or existing equipment, the SITF guidelines provide a generic SECS II framework. In one possible scenario to control costs in software development, an equipment manufacturer might decide to charge extra for custom SECS implementation beyond the SITF SECS guidelines.

- For equipment manufacturers that have already dedicated substantial resources to SECS protocol implementation, there is the possibility of working closely with the SITF in the development of SECS guidelines for specific equipment models.

- Certainly, the ability to meet the generic equipment communications requirements of AT&T, IBM, Intel, Motorola, National Semiconductor, Siemens, and Texas Instruments is strong incentive alone for equipment manufacturers to carefully consider adopting the SITF guidelines.

- Finally, other major U.S. semiconductor manufacturers may choose to reference the SITF guidelines in future purchase requirements.

Some legal constraints will not allow a semiconductor manufacturer to require an equipment company to meet SITF SECS guidelines absolutely. This is part of the reason that the SITF is very careful to point out that its work represents only guidelines for the vendor community, not hard and fast requirements. The SITF believes, however, that even 20 percent to 30 percent commonality among SECS II specifications would reduce the work load significantly for both equipment and semiconductor manufacturers in the development and interpretation of SECS protocol implementations.

End Users

For semiconductor manufacturers, one of the major benefits of SITF SECS guidelines is that many companies will not have to devote limited resources to the development of internal SECS specifications. They can, in a sense, ride on the shoulders of the semiconductor giants that are SITF member companies. With the adoption of certain minimum SECS specifications, the manufacturers' task of evaluating every equipment company's SECS implementation will also be reduced substantially.

SITF SECS guidelines will impact not only in-house automation programs, but internal equipment development groups as well. In addition, it will be vital that SITF SECS guidelines be raised as a priority within semiconductor companies' purchasing departments, since, oftentimes, product technology (i.e., 0.5-micron processing capability) wins out over manufacturing technology such as factory automation programs.

Sematech

It is too early to tell what position Sematech will take regarding the adoption of SITF SECS guidelines. It is interesting to note, however, that all SITF member companies, with the exception of Siemens, are members of Sematech as well. In addition, Dataquest is aware that the SITF recently made a presentation to Sematech during an automation and robotics workshop. Because of the resources and commitment that SITF member companies have already invested in this project, Dataquest does not expect Sematech to reinvent the wheel but, instead, to follow the equipment communications guidelines, as outlined by the SITF.

WILL SECS GUIDELINES WORK?

Ultimately, the question arises, will SITF guidelines really work? Dataquest believes that the answer to this question hinges upon the success of the technical education programs planned for May and September. Semiconductor and equipment manufacturers alike will have to be convinced that they will receive some fundamental benefit by adopting the SITF SECS guidelines. The other critical factor that will determine the success of this program is whether semiconductor manufacturers actually establish a communications network between processing equipment and host computers within their fabs. Semiconductor manufacturers must use SECS, not just ask for it. Only then will equipment manufacturers have the evidence that they need to justify additional software and engineering resources to their management.

It has been the burden of the SITF member companies to develop generic SECS guidelines for the industry. For the success of this program, these same companies may also have to be the first to report on the success of their own in-house programs in equipment communications. While the SITF may not answer everyone's questions regarding SECS, Dataquest believes that this committee has taken a bold first step in consolidating the efforts of developing effective equipment communications within the semiconductor industry.

Peggy Marie Wood

Dataquest
a company of The Dun & Bradstreet Corporation

Research *Bulletin*

SEMS Code: 1987–1988 Newsletters/Bulletins
1988–4

U.S. IC PRODUCERS HEADING SUBMICRON

Recent analysis of Dataquest's U.S. fab data base reveals that wafers with small line geometries account for a large part of U.S. production. We believe that U.S. production will move vigorously into the submicron range by 1992.

WAFER STARTS AND CAPACITY UTILIZATION BY LINE GEOMETRY

Wafer starts for sub–2–micron geometries accounted for more than 36 percent of all wafers in 1987, approximately equal to the number of wafers with geometries greater than or equal to 2.5 microns (see Figure 1).

Capacity utilization rates for geometries <1.5 microns and ≥1.0 microns are at 90 percent (see Figure 2). The utilization rate, however, for silicon wafers with geometries of <1 micron is very low—only 18 percent. This is because these lines are at the very beginning of their ramp–up phase. We expect these utilization rates to rise as the submicron process becomes better understood.

SUBMICRON SHIFT

Analysis of new fab capacity from Dataquest's fab data base reveals that the industry plans to respond to today's tight capacity in small geometries, as shown in Table 1.

Table 1

New Wafer Capacity Distribution
1988–1991

Line Geometry	1988	1989	1990	1991
<1	0	9%	42%	78%
≥1, <1.5	80%	61%	49%	22%
≥1.5, <2	20%	31%	10%	0

Source: Dataquest
February 1988

Based on the new fabs that will be coming on–line and on the Dataquest IC consumption forecast, we predict that almost 60 percent of the square inches of silicon consumed in 1992 will be for sub–1.5–micron production (see Figure 3).

George Burns

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 437-8000, Telex 171973, Fax (408) 437-0292

Figure 1

1987 Starts by Line Geometry

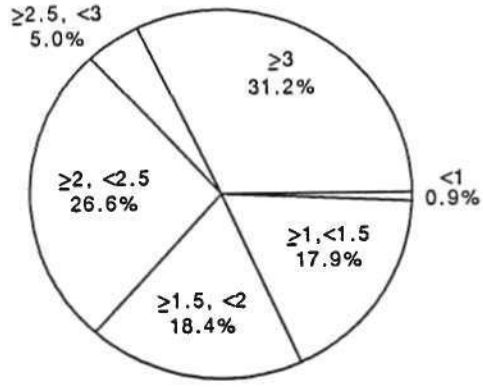


Figure 2

1987 Wafer Capacity Utilization by Line Geometry

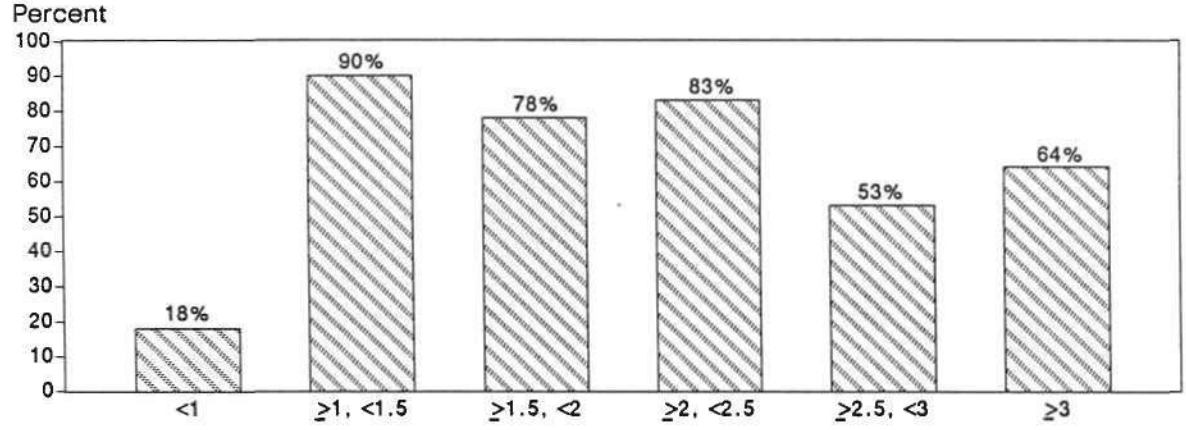
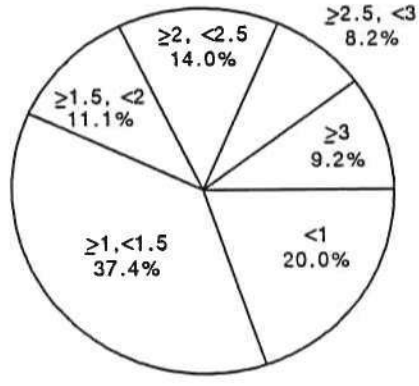


Figure 3

1992 U.S. Silicon Consumption
(In Square Inches by Line Geometry)



Source: Dataquest
February 1988

Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: Newsletters 1987–1988
1988–3

SEMICON/JAPAN 1987 EQUIPMENT HIGHLIGHTS

The 11th annual SEMICON/Japan trade show, specializing in semiconductor process equipment and materials, was held December 2 through 4 in Tokyo. This industry trade show was the largest of the seven SEMICON shows sponsored in 1987 by the Semiconductor Equipment and Materials Institute (SEMI). SEMICON/Japan had nearly 50,000 attendees, with SEMICON/West 1987 coming in second with 45,000. SEMICON/Japan is also the most important trade show for the Japanese semiconductor equipment and materials industry.

The general mood at the show was upbeat and optimistic as the signs were clear that the equipment and materials industry has finally emerged from its slump. Many new products were introduced and many new companies exhibited for the first time. Dataquest believes that SEMICON/Japan 1987 marked a turning point in the worldwide equipment and materials industry. We believe, as this newsletter will indicate, that the Japanese equipment industry has matured and is now ready to flex its muscles in the world arena to provide more unwanted competition for the American and European equipment vendors.

Each year, Dataquest attends the show and reports on significant new equipment introductions and product enhancements. This year, Dataquest concentrated on Japanese wafer fab equipment vendors in order to report on the status and development of the Japanese equipment industry. This newsletter presents the results of the survey.

INTRODUCTION

SEMICON/Japan has become more and more dominated by Japanese equipment and materials companies over the last six years. As shown in Table 1, there were 232 Japanese exhibitors in 1982 and 542 in 1987, an increase of 134 percent. Of the 542 exhibitors, 100 companies were exhibiting for the first time. In contrast, U.S. exhibitors numbered 204 in 1982, increasing only 34 percent to 274 in 1987. In addition, the number of Japanese exhibitors increased by 35 from 1986 to 1987, while the number of U.S. exhibitors declined by 17. Clearly, the Japanese equipment and materials industry is growing at a very rapid pace, while U.S. company presence in Japan is declining.

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 437-8000, Telex 171973, Fax (408) 437-0292

Table 1

SEMICON/Japan Exhibitors by Country
(1982–1987)

Country	1982	1983	1984	1985	1986	1987
Japan	232	327	413	468	507	542
United States	204	289	288	282	291	274
United Kingdom	11	15	19	19	22	21
West Germany	12	14	20	13	14	11
Other	16	30	28	25	34	27
Total	475	675	768	807	868	875

Source: SEMI

The ambience at SEMICON/Japan is also changing in accordance with the increasing strength of the Japanese equipment and materials industry. SEMICON/Japan 1987 was very much a Japanese equipment and materials exposition that could be likened to a large SEMICON/Osaka, the regional Japanese show held midyear and attended only by Japanese companies and personnel.

A few years ago at SEMICON/Japan, almost all displays and most brochures were in English, with an abundance of American and European marketing people striding the exhibition halls, and with little problem having discussions in English at just about any booth. It was almost like SEMICON/West transported to Tokyo, but with a Japanese flavor. This year, however, things were very different at SEMICON/Japan: almost every display and brochure was in Japanese, few Westerners were wandering about, and it was very difficult to have conversations in English, even at the booths of major Japanese equipment companies.

An examination of exhibition booth size is also illuminating. As the Japanese companies continue to grow, so does the size of their booths. At the same time, the booth size of American companies has decreased. Today, the large exhibition booths are occupied by Japanese companies rather than their previous tenants, the American companies.

The implications of the above discussion are more than cosmetic: the increasing number of Japanese equipment and materials companies coupled with their advances in equipment and materials technology mean that the Japanese companies will continue to increase their share of the world market. Table 2 shows 1982 and 1986 worldwide market share data for regional companies participating in key front-end equipment segments (lithography, etch, deposition, diffusion, and ion implantation). The data show that, while European companies are holding their own, U.S. equipment companies are losing worldwide market share to the Japanese companies.

Table 2

Worldwide Wafer Fab Equipment Market Shares

	1982	1986
U.S. Companies	62%	55%
Japanese Companies	29%	35%
European Companies	9%	10%

Source: Dataquest
February 1988

In Japan, the situation is very similar. As Table 3 shows, Japanese equipment companies are increasingly dominating their home market, whereas U.S. companies continue to lose market share in Japan. The loss has not been gradual for the American companies; as recently as 1984, they still had a 30 percent market share, but their share decreased to 23 percent in 1985 and 18 percent in 1986. Data for 1987 has not been completely compiled, but Dataquest believes that U.S. companies' market share in Japan will be even less than in 1986.

Table 3

Wafer Fab Equipment Market Shares in Japan

	1982	1986
Japanese Companies	67%	78%
U.S. Companies	30%	18%
European Companies	3%	4%

Source: Dataquest
February 1988

In the past, Japan has been a viable market for U.S. equipment vendors, but we believe that future opportunities for U.S. vendors in Japan will continue to dwindle. Unless a U.S. company already has a very strong presence in Japan, or an exceptional leading-edge product, it should forego the Japanese market and employ its scarce resources to develop the European and Rest of World (ROW) markets.

The huge buildup in installed capital equipment by the Japanese semiconductor manufacturers from 1983 through 1985 directly benefited the Japanese equipment industry. As a result of that technology development and growth, Japanese equipment companies now are positioned to begin a strategy to capture a majority share of the

world equipment market. The assault has already begun, as Japanese equipment companies are now expanding into their export markets. American companies are not only losing market share in Japan, but, along with the European equipment companies, face increasing competition in their home markets and in the other export markets as well.

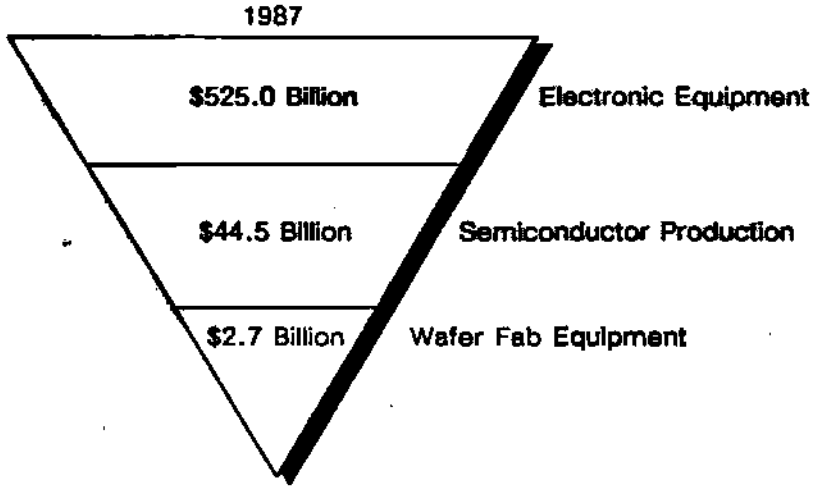
ADVANCED EQUIPMENT TECHNOLOGY

The most significant observation made at the show was that the Japanese equipment companies are beginning to aggressively develop equipment technologies that they consider key to the future manufacturing success of IC devices. These same technologies are being only minimally pursued by American and European equipment companies. If these future equipment technologies prove to be vital, then the Japanese equipment companies will be well positioned to dominate the world market when the market emerges.

An important implication of advanced equipment technology is that wafer fab equipment is at the bottom of the electronic industry "food chain" (see Figure 1). Advanced manufacturing equipment drives advanced semiconductor manufacturing techniques, which drive advanced IC devices, resulting in advanced electronic equipment, including computers and military electronics. Thus, leadership in the relatively small $2.7 billion front-end equipment industry is a gateway to leadership in the $525 billion worldwide electronic equipment market.

Figure 1

Worldwide Electronic Industry Food Chain



Source: Dataquest February 1988

Dataquest has identified several such areas of advanced technology that are being pursued by the Japanese equipment companies: photo CVD, excimer lasers, ion beam technology, large substrate processing equipment, vertical diffusion furnaces, and electron cyclotron resonance (ECR) etch and deposition equipment. Substantially more Japanese equipment companies are participating in each of these areas than are their American or European counterparts. Following is a discussion of these advanced technology areas.

Photo CVD

In chemical vapor deposition (CVD), a source of energy is needed to decompose the reactant gases in order for film deposition to occur. In LPCVD, thermal energy is used; in PECVD, the source of energy is an RF-excited plasma; and in photo CVD, ultraviolet light is used to decompose the reactant gases. The main advantage of photo CVD is the lower deposition temperature, which can be as low as room temperature. Such low deposition temperatures are required in some III-V devices.

Four Japanese companies, Nippon Tylan, Samco, Semiconductor Energy Laboratories, and Tokyo Electron Limited, offer photo CVD equipment. The market for photo CVD equipment is currently very small, and the future of this technology is uncertain. Only one U.S. company (Tytan, formerly Tylan) manufactures this type of equipment, and Dataquest is not aware of any European companies that offer it.

Excimer Lasers

Excimer lasers are key to the development of optical lithography. Wafer steppers using excimer laser sources will be the next lithography tool after i-line steppers and will extend optical lithography to 0.5 micron and, perhaps, lower. At SEMICON/Japan, four companies were offering excimer lasers: Hamamatsu, Mitsubishi, Nissin Electric, and Shibuya. Shibuya, which also makes laser marking equipment, manufactures its excimer laser under license from Questek, an American company. Other Japanese companies offering excimer lasers are Komatsu and NEC.

Ion Beam Technology

In the area of ion beam technology, Mitsubishi Electric is marketing an ion cluster beam system, the M-ICB, for the deposition of thin films. The M-ICB can be supplied with one to four ion sources and can accept 200mm wafers. Nissin Electric also offers an ion cluster beam system, the ICB-2G and, in addition, offers several ion vapor deposition systems, ranging from the IVD2/10 (2kV, 10mA) to the IVD40/100 (40kV, 100mA).

Seiko, expanding upon its focused ion beam mask repair technology, has introduced the SMI8100, a focused ion beam system designed for IC development work. The SMI8100 can modify passivated metal traces on IC devices in the wafer, chip, or open package configuration to help reduce IC development time. Other companies active in ion beam technology include Elionix, which manufactures ion beam and ion shower equipment, and JEOL, which manufactures focused ion beam equipment.

JEOL has concentrated its efforts on equipment for research in focused ion beam lithography, ion implantation, and other areas, and has not marketed a focused ion beam system for mask repair. However, JEOL has sold many focused ion beam systems, and easily has the market lead for nonmask repair focused ion beam systems. Also, almost all of JEOL's customers for the focused ion beam system are in Japan. Because there are very few commercial focused ion beam systems in the United States and Europe for doing research in lithography and ion implantation, the Japanese semiconductor companies may be in the lead for this advanced semiconductor manufacturing technology.

Large Substrate Processing Equipment

Large substrate, or liquid crystal display (LCD), processing equipment is a new branch of capital equipment specifically designed for manufacturing large substrates. Equipment of this nature is just beginning to appear on the market, and Canon and Nikon, in the past year or so, have introduced lithography equipment to align and image the large substrates. At SEMICON/Japan there were several equipment introductions in this area, some of which are described below.

Nippon Seiko introduced the LZ-340, an optical pattern generator specifically designed to make the large masks required to image LCDs. It is priced at approximately $1.5 million. In the etch area, Plasma Systems and Tokuda offer systems for the dry processing (dry etch and dry strip) of LCDs. In the deposition area, Tokuda offers sputtering and plasma deposition systems for LCDs; ASM Japan, Denko, and Koyo Lindberg offer vertical furnaces for LPCVD thin film deposition.

This emerging equipment technology in Japan should be compared with the situation in the United States and Europe. Two American companies (American Semiconductor Equipment Technologies and MRS) offer large substrate lithography equipment, but Dataquest does not know of any other semiconductor capital equipment company outside of Japan offering etch or deposition equipment for large substrates.

Vertical Furnaces

SEMICON/Japan 1987 was the coming-out party for the Japanese manufacturers of vertical diffusion and LPCVD furnaces. This year there were eight Japanese manufacturers but only one American manufacturer, Silicon Valley Group (SVG), exhibiting products in this area. The Japanese furnace manufacturers firmly believe that, although horizontal furnaces continue to dominate the marketplace, in two to three years wafer fabs will use only vertical furnaces. They cite as advantages higher-quality, critical gate oxides because of the minimization of oxygen draw-in, ease of automation, better contamination control, and better uniformity of LPCVD films, in comparison with horizontal furnaces.

In contrast, in the United States, there are only three manufacturers of vertical furnaces, Semitherm, SVG, and Tempress. Interest in this technology on the part of the U.S. semiconductor manufacturers is lackluster, although it seems to be increasing. Clearly, the Japanese will be well positioned to meet the market demands in Japan as well as to provide competition for the American equipment vendors when the U.S. market emerges.

The following paragraphs give a brief description of the products offered by the eight Japanese vertical furnace manufacturers.

ASM Japan

ASM Japan introduced two vertical furnaces: the VMP-100 for LPCVD and the VDF-100 for diffusion processes. Prices of the furnaces are ¥35 million to ¥50 million depending on the model. Dataquest believes that the furnaces can accommodate up to 100 wafers per load. They were developed and manufactured by ASM Japan, which also introduced a vertical furnace for LPCVD on large substrates.

Dainippon Screen (DNS)

DNS also exhibited a vertical furnace for diffusion and LPCVD processes. It can process up to 100 125mm or 150mm wafers. Currently, the furnace must be manually loaded; robotic transfer will be added in the future.

Denko Systems

Denko began its involvement with vertical furnaces about five years ago. Today, Denko has the Erectus series of vertical systems available for use in production: a single-tube system for diffusion (¥35 million) or LPCVD (¥45 million), a dual-tube system for diffusion or LPCVD (¥50 million to ¥60 million), and a multiple-tube system with a common robotic transfer system that loads and unloads all the tubes. All of the production systems accommodate up to 100 150mm wafers per load with the exception of the single-tube system, which accommodates 200mm wafers. Denko also provides diffusion and LPCVD vertical systems for R&D use that will accept 25 150mm wafers per load.

Denko also has a vertical diffusion and LPCVD furnace for large substrates. It can handle 50 350mm substrates.

In addition to vertical furnaces, Denko sells horizontal furnaces, an area in which the company has been participating for 15 years.

Disco

Disco, which began shipping vertical furnaces three years ago, exhibited a multiple-tube system with a common robotic handler. The system can be configured with one to eight vertical tubes with a single handler, with four tubes being the most common. The price of a four-tube system is ¥150 million.

The vertical tubes are for diffusion (DWD1000) or LPCVD (DWL1000) processes. The DWD1000 accepts up to 125 150mm wafers, and the DWL1000 accepts 100 150mm wafers for LPCVD films (except that for LTO films, 50 125mm wafers are processed).

Koyo Lindberg

Koyo Lindberg's vertical furnaces are designed and manufactured in Japan but were originally based upon the design of General Signal's Tempress vertical furnace.

Koyo Lindberg offers the VF-2000 Series, a manually loaded system for either diffusion or LPCVD processes. This system, which was first introduced three years ago, is currently priced at ¥20 million. Two years ago, Koyo Lindberg introduced the VF-4000 Series for production use. This system is automatically loaded, and it is for either diffusion or LPCVD processes. It is priced at ¥30 million. The VF-4000 can accom- modate 200 150mm wafers per load. Several VF-4000s can be used together with a common robotic loader that runs on a track and uses a work-in-process station to store cassettes. The cassettes are then transferred to the individual VF-4000 stations.

Koyo Lindberg also has introduced a vertical furnace for large substrates. It can handle a load of 20 300mm substrates.

Kokusai Electric

Kokusai introduced improved versions of the DJ-800V vertical furnace called the DJ-802V for LPCVD (¥55 million) and the DD-802V for diffusion (¥44 million). Improvements included better control, wafer handling, and communications systems, and other changes to make the system more production-worthy. At present, the vertical reactor can accommodate 120 150mm wafers and up to 165 in the future. For LPCVD films, from 50 to 100 wafers are processed, depending on the film.

TEL/Thermco

TEL/Thermco exhibited its vertical furnace for LPCVD, the VCF-6105, which was designed and built in Japan. It can accommodate 125 150mm wafers, but for a silicon nitride film the process load is 100 wafers. Five cassettes of wafers can be transferred to a horizontal wafer boat, which is then rotated to a vertical position for processing. The method of wafer transfer from the cassettes to the wafer boat can be either single wafer or mass transfer.

Ulvac-BTU

Ulvac-BTU introduced its vertical furnace, which was also designed and built in Japan. Dataquest believes that the cassettes of wafers are placed in a closed evacuated area before the wafers are transferred to the wafer boat.

ECR Equipment

Electron cyclotron resonance technology uses microwave power to generate a plasma that can be used for either etch or CVD of silicon oxide and silicon nitride. Advantages of ECR technology include no radiation damage in the case of etch, and low-temperature deposition of very high-quality films in the case of CVD. Japanese semiconductor manufacturers see ECR etch and deposition equipment as important for advanced manufacturing of semiconductor devices. Within the last year, interest in this advanced technology has picked up rapidly, particularly among the Japanese and European equipment vendors.

The first ECR equipment was developed by NTT and commercialized by Anelva in 1983 under license from NTT. This year at SEMICON/Japan, there was literally an explosion of Japanese companies marketing ECR etch and deposition equipment, as 10 equipment companies offered products in this area. Dataquest believes that most of

the Japanese companies are manufacturing the ECR equipment under license from NTT. It is interesting to note that NTT, while giving Anelva the initial lead in ECR, is now promoting intense competition in the marketplace via its licensing policy.

Table 4 lists the 10 companies, along with the model and price where known. Note that 2 of the 10 companies, Japan Steel Works and Sumitomo Metal Industries, are new entrants into the wafer fab equipment market. Both of these are examples of Japanese companies in declining industries that are now turning to high-tech industries for their future growth. Also, Tokki, a factory automation equipment maker, has entered the market with NTT-licensed equipment.

ECR activity in the United States has been minimal to date, as there is no U.S. equipment vendor manufacturing U.S.-designed ECR equipment; however, VEECO has announced the development of a proprietary ECR source. Other activity involves Materials Research Corporation, which recently signed an agreement with NTT to produce ECR equipment under license from NTT, and Lam Research, which has an agreement with Sumitomo Metal Industries to market its ECR equipment in the United States. Two other small U.S. companies, Applied Science and Technology and Microscience, also have some activity in ECR.

Table 4

Japanese Companies Offering ECR Equipment

Company	Model	Price (Millions of Yen)	Process		
			Etch	CVD	Sputter
Anelva	N/A	N/A	X	X	
Ashida	ATM-800	¥ 33		X	
Elionix	EIS-150B	¥ 39	X		
Hitachi	M-206A	¥120	X		
Japan Steel Works	RE-601	¥100	X		
Shimadzu	SLEC-200	¥ 65		X	
Sumitomo Metal Industries	EC-300	N/A		X	
	EC-3000	N/A		X	
	ER-2000	N/A	X		
	ES-200	N/A			X
Tokki	ECV-251	¥ 50		X	
Tokyo Ohka	TSME-5300	¥120	X		
Ulvac	RIEX-8000	N/A	N/A	N/A	N/A

N/A = Not Available

Source: Dataquest
February 1988

In Europe, two companies offer ECR systems. Electrotech, a U.K. company, markets a system that is the result of a joint development program between Electrotech and two research organizations in France: the Centre National D'Etudes des Telecommunication (CNET) and the Centre National de la Recherche Scientifique (CNRS). Plasma Technology, another U.K. company, also offers ECR etch and deposition systems.

NEW PRODUCT INTRODUCTIONS—TODAY'S FRONT-END TECHNOLOGY

In addition to the equipment introduced for advanced semiconductor manufacturing technology described above, numerous significant new products were introduced by the Japanese equipment vendors in all segments of today's front-end equipment. Discussed below are key product introductions in the closely related segments of lithography, automatic photoresist processing equipment, and wafer inspection equipment. Also discussed is rapid thermal processing (RTP) equipment.

Although key product introductions occurred in other areas, such as etch, deposition, and ion implantation, they are not discussed here; for information on the products in these areas, please contact Dataquest's SEMS staff in San Jose.

Lithography

In optical reduction steppers, product introductions were mainly in the area of i-line lenses to push resolution limits down to 0.6 micron. Hitachi and Sumitomo GCA introduced new i-line lenses, and Nikon is rumored to be developing one. On the other hand, Canon believes that i-line lenses will not be necessary and that the submicron path will be with high numerical aperture (NA), g-line lenses and excimer laser steppers.

Perhaps the most significant introduction in lithography was the Nikon excimer laser stepper. Now, three companies—Canon, GCA, and Nikon—are developing excimer laser steppers and are vying for position in this advanced lithography technique.

Canon

Canon introduced a new lens for the FPA-1550 MII stepper, a 0.48-NA, g-line lens with a resolution of 0.7 micron. On display at the booth were scanning electron microscope (SEM) photos showing 0.55-micron lines and spaces resolved with this lens. The lens will be available in the spring of 1988.

GCA

Although GCA is an American company, it is discussed here because the new S-2142i lens used in the new Model 8570i DSW Wafer Stepper is made in Japan by a Japanese optical company. The S-2142i is a 5X i-line lens with an NA of 0.42, a field size of 21.2mm in diameter, and a resolution of 0.6 to 0.7 micron. On display at the booth were SEM photos showing 0.5-micron resolution. The S-2142i lens will be available in the second half of 1988.

Hitachi

Hitachi displayed its new LD-5010i stepper, which uses a new 5X i-line lens. The LD-5010 has an overlay specification of 0.15 micron (3 sigma) and a 10-reticle automatic reticle changer. The new lens, which is made by Hitachi, has an NA of 0.40, a field size of 21.2mm in diameter, and a resolution of 0.6 micron. Hitachi offers two g-line lenses: one made by Zeiss, and the other a 0.38-NA lens made by Hitachi.

Nikon

Nikon announced, via a video tape, its 1505EX Excimer Laser Stepper. The 1505EX uses a krypton fluoride laser and a 0.40-NA lens that has a resolution of 0.35 micron and a field size of 15mm x 15mm. The 1505EX will be available for delivery in the spring of 1988 and will cost ¥300 million.

Nikon is also offering the SX-5 X-ray Stepper, which uses a rotating target as the source of X rays. The SX-5 has a resolution of 0.5 micron and uses field-by-field alignment to obtain an overlay accuracy of 0.15 micron (3 sigma). The system can handle 150mm wafers with the exposure area varying from 11mm x 11mm to 29mm x 29mm. X-ray power is 0.5 mW/cm^2. Nikon introduced the SX-5 a year ago, but Dataquest does not believe that any systems have yet been shipped. Price of the SX-5 is ¥250 million.

No new lenses were announced by Nikon for its NSR g-line series steppers; however, we believe that Nikon is developing a 5X production, i-line lens to be introduced in the near future.

Sumitomo Heavy Industries

Sumitomo Heavy Industries announced its Aurora compact synchrotron orbital radiation (SOR) ring for use in X-ray lithography. The Aurora ring is 3.0 meters in outside diameter, 2.2 meters high, and has a 1.0-meter orbital diameter, the smallest in the world. Its compactness was made possible by the development of a new resonance injection method employing a superconducting magnet. The injector is of race-track design and has an energy of 150 MeV. The energy of the storage ring is 650 MeV; stored beam current is 300mA.

Sumitomo began development of the ring in 1984. The prototype machine is under construction and undergoing various tests; beam tests will begin in the spring of 1988. Operation of the ring, which will initially have three beam lines but eventually will be expandable to 16 ports, is scheduled for the spring of 1989. Price of the Aurora will be about $15 million.

Interestingly, Sumitomo Heavy Industries seems to be very qualified to undertake the development of an SOR ring. It has 17 years of experience in accelerator research and 10 to 15 years of experience in superconducting motors. Sumitomo also has under way a development project for the X-ray stepper to be used with the ring, which it will develop itself, rather than work with a lithography company.

Sumitomo does not see lithography as the only application for SOR; other applications include medical research and analysis of macromolecular structures.

Automatic Photoresist Processing Equipment

Four Japanese companies demonstrated automatic photoresist processing equipment at SEMICON/Japan 1987: Canon, Dainippon Screen, Tazmo, and TEL. System enhancements and new equipment introductions focused on tighter contamination control, smaller equipment footprint, and new systems for spin-on-glass applications and CCD manufacturing.

Canon

Canon demonstrated several configurations of its production-viable vertical track system, the CDS 650. This equipment was first introduced as a development model at SEMICON/Japan in 1986. The CDS 650 utilizes a mechanical pick-and-place wafer handler in lieu of belts for wafer movement. The wafer handler is centrally located between various processing modules (i.e., spin coater, HMDS, and development units) and a series of four vertically stacked plates. The company claims tighter contamination control and a substantially reduced footprint with the new vertical design. As yet, Canon has made no deliveries of the CDS 650. Demonstrations at Japanese semiconductor manufacturers' facilities will commence in first quarter 1988. The price of the system is expected to be on the order of ¥10 million to ¥20 million.

Dainippon Screen

Dainippon Screen introduced a new system, the Model 629, to its family of automatic photoresist processing equipment. Rather than belts or o-rings, the new system employs a pick-and-place wafer transport mechanism. The 629 was designed, in particular, for the 4-Mbit and 16-Mbit DRAM processing environment because of the enhanced contamination control achieved through this type of wafer-handling mechanism. The system is also equipped with an IC smart card reader that simplifies the input of processing specifications, such as spin parameters and oven recipes, by storing that information directly on a smart card. The Model 629 is priced between ¥25 million and ¥60 million, depending on options. Dainippon Screen expects to begin shipments to Japanese semiconductor manufacturers in February 1988.

Tazmo

Tazmo introduced a new spin-on-glass system, the TR 6132-UD. This tool has been designed for the U.S. market as a result of feedback from customers in that region. One significant new feature is the reduced footprint achieved by designing a U-turn in the wafer path configuration. In addition, the system's display panel has been made more flexible for the R&D-oriented environment of spin-on-glass processing in the United States. In contrast to the United States, spin-on-glass processing systems in Japan are considered production tools. As such, the display panel on previous Tazmo machines had been designed at a location below waist level, since minimal access to the panel is required in a production environment. The price of Tazmo's new TR 6132-UD is approximately $150,000 in the United States, although the final price will vary, depending upon customer options and final configurations. First shipments to a U.S. semiconductor manufacturer will occur in March 1988.

TEL

At SEMICON/Japan 1987, TEL announced a new track system specifically for CCD manufacturing. The CCD On-Chip Coater system dispenses photoresist through a temperature-controlled nozzle onto a wafer also maintained in a temperature-controlled environment. The price of the CCD On-Chip Coater system is ¥40 million. Dataquest believes that TEL has already sold several systems in Japan.

Future Opportunities?

To date, the Japanese track companies have had minimal penetration of the U.S. market, a region that represents a strategic growth opportunity. To address this issue, Dainippon Screen opened an office in Santa Ana, California, in October 1987. The new operation is known as Dainippon Screen Engineering of America Inc. Tazmo is represented by Semix in the United States. Semix's first sales of Tazmo's track equipment were in 1986.

Two more Japanese companies may enter the automatic photoresist processing equipment market in 1988. Hitachi Tokyo Electronics (formerly Hitachi Ohme) currently manufactures the PM1400 Coat Develop System for in-house processing applications at Hitachi's semiconductor facilities. In a similar vein, Toshiba Machine manufactures the APF-5000 and APF-6000 track systems for Toshiba's semiconductor operations. Both Toshiba Machine and Hitachi Tokyo Electronics are considering bringing these products to the commercial market during 1988.

Rapid Thermal Processing

The use of rapid thermal processing (RTP) systems in production applications has not been widely accepted in Japan. Semiconductor manufacturers, with their extensive experience in traditional diffusion processing, have been slow to adopt the new rapid thermal processing techniques. The primary focus in RTP technology is on improving temperature uniformity across the wafer surface and on developing closed-loop temperature-monitoring systems. When these factors have been improved to meet the demands of the production environment, Dataquest expects the rapid thermal processing market to experience significant growth.

Japanese manufacturers of RTP equipment include Dainippon Screen, Koyo Lindberg, M. Setek, and TEL/Thermco (no equipment exhibited this year). Kokusai and Ulvac are reportedly developing systems, while Ushio supplies high-intensity lamp sources for rapid thermal processing equipment. Three companies—AG Associates (through Canon, its representative in Japan), Dainippon Screen, and M. Setek—introduced new systems at SEMICON/Japan.

Canon/AG Associates

AG Associates, represented by Canon at SEMICON/Japan, announced the introduction of the Heatpulse 4100. The Heatpulse 4100 was designed as a production tool and utilizes ultrahigh efficiency filters in the reaction chamber to create a Class 10 environment. The system also incorporates a new wafer-handling robot in the design in order to minimize contamination. Primary applications for the 4100 include rapid

thermal oxidation and nitridization, and reflow of BPSG. The Heatpulse 4100 was manufactured by AG Associates at Canon's request, based on input from several Japanese semiconductor manufacturers. The Heatpulse 4100 is priced at approximately ¥50 million, and deliveries to Japanese customers are scheduled to begin in March 1988.

Dainippon Screen

Dainippon Screen introduced a new model of its rapid thermal processing equipment at SEMICON/Japan 1987. The difference between the new 614A and Dainippon Screen's model 613 system is a new control system for monitoring wafer temperature in the reaction chamber. The 614A provides closed-loop monitoring for temperature control in addition to the open-loop monitoring available on the 613. Closed-loop monitoring is a direct technique for monitoring the temperature of processed wafers, while open-loop monitoring is an indirect technique that uses a test wafer for temperature calibration of actual wafers being processed. The model 614A is priced at ¥40 million. Primary applications for this system include rapid thermal oxidation for deposition of oxide layers of less than 100-angstrom thickness.

M. Setek

M. Setek introduced its high-pressure annealing equipment, the HPA-10A. This system was designed for the formation of silicon oxide and silicon nitride, PSG/BPSG reflow, and silicide-annealing processes under high-pressure, low-temperature, and short time-duration conditions. The lamp configuration consists of a series of 24 halogen lamps, and the system can operate at pressures of up to 10 atmospheres. The HPA-10A is priced at ¥35 million. Deliveries are expected to begin in 1988. M. Setek offered a manual version of this system in 1987.

Wafer Inspection

Japanese equipment companies dominate their home market in the categories of wafer defect inspection systems and critical dimension measurement equipment. In the area of traditional microscope-based wafer inspection stations, Canon, Nidek, and Nikon are the three companies with significant market presence. Lasertec, with its new model 3WD36 Automatic Wafer Inspection Station, and Sony, with the ARQUS-20 system, offer advanced high-speed reticle qualification systems based on a die-to-die comparison of the wafer pattern. In optical critical dimension (CD) measurement systems, major suppliers Hitachi and Nikon vie for leadership, while Ryokosha is a smaller participant in this equipment category. Two new entrants announced optical CD measurement systems at SEMICON/Japan 1987: Dainippon Screen (already active in automatic film thickness measurement) and Nidek (one of the three major participants in wafer inspection in Japan).

As line geometries shrink past the resolution limits of traditional white-light measurement equipment, semiconductor manufacturers are faced with several technological choices for critical dimension measurement systems. While European and U.S. semiconductor manufacturers are exploring the capability of the newly developed confocal scanning laser microscope systems, Japanese manufacturers have embraced in-process scanning electron microscope (SEM) tools for linewidth measurements in the submicron range. Many of the Japanese semiconductor companies believe that the

technique of confocal scanning laser microscopy is not fully qualified for the production environment; therefore, manufacturers have chosen to jump directly to e-beam-based measurement systems. Hitachi, with its model S-6000, is the leader in Japan for providing in-process SEM for CD measurement. Other Japanese manufacturers of e-beam-based CD measurement systems include ABT (Akashi Beam Technology), JEOL, and newcomer Holon.

Canon

Canon introduced a new model of the VIR 600 Series wafer inspection systems. The new product, the VIR 630, differs from the 600 in that the individual wafer transport time has been reduced by a factor of 3, down to approximately 3 seconds. The price of the VIR 630 is ¥11 million, and the first sales began in summer 1987. The VIR 600 system was first introduced in 1982.

Dainippon Screen

Dainippon Screen introduced an optical-based linewidth measurement system at SEMICON/Japan 1987. The SLM 601, which has minimum linewidth measurement capability of 0.8 micron, is still under development. Future options will include automatic wafer handling. Deliveries of the SLM 601 are expected to begin in April 1988. Dainippon Screen also manufactures automatic film thickness measurement systems and tools for trench depth measurement.

Hitachi

Hitachi Deco (Hitachi Electronics Engineering Co., Ltd.) manufactures the LAMU (Lithography Accuracy Measuring Unit) system for critical dimension measurements. The LAMU-600 has nominal linewidth resolution of 0.8-micron and 0.03-micron repeatability for overlay measurement. The LAMU-600, a production-oriented CD measurement system, is priced at ¥43 million. As yet, the LAMU-600 is not marketed in the United States. This is because the LAMU-600 requires extensive software for interfacing with stepper and other lithography systems. At this time, Hitachi is still investigating the software system capability that would be necessary to effectively market the LAMU-600 to U.S. semiconductor manufacturers.

At SEMICON/Japan, Hitachi Deco introduced the IS-1000, the newest generation of its HILIS-200 patterned wafer inspection system. Both of these systems use highly sensitive detectors to detect ultrafine foreign particles that adhere to the surface of a wafer. This is done by directing a laser beam over the wafer surface and detecting scattered light from the particles. The IS-1000 has a detection limit of 0.8 micron (first layer) to 2.0 microns (second or third layer, aluminum layer) on patterned wafers, compared with the HILIS-200 detection limit of 2.0 to 3.0 microns. The IS-1000 detection and measurement rate is on the order of six to seven minutes per wafer, and, as such, the system was designed for R&D, analytical, and process qualification operations. The HILIS-200 operates at twice the speed of the IS-1000, and is used extensively in the production environment. The HILIS-200 is priced at ¥50 million, while the new IS-1000 is approximately ¥90 million. Deliveries to Japanese customers are expected to begin in April 1988.

Hitachi Denshi (a different Hitachi equipment company from Hitachi Deco) manufactures the S-6000 Critical Dimension Measurement SEM system. This tool, priced at ¥90 million, is three years old. In that time, it has established itself as the leader in CD SEM tools for the production environment. Dataquest estimates that there are more than 100 of these systems in the installed base.

Lasertec

Lasertec introduced its Model 3WD36 Automatic Wafer Inspection System at SEMICON/Japan. This reticle qualification tool, priced at ¥75 million to ¥80 million, was designed with high-resolution objective lenses and confocal laser optics that allow wafers to be inspected for defects down to 0.5 micron. The high-speed inspection system converts the images of two adjacent dies to video signals that are compared with each other to detect the presence of defects. Defect coordinates, which are stored in the system computer, can be recalled by the operator for directing wafer stage movement during defect confirmation and classification. Dataquest believes that Lasertec shipped its first system in the latter half of 1987.

The Lasertec 3WD36 system competes with Sony's ARQUS-20 Automatic Reticle Qualification System. This tool, developed by Sony in 1979, became a commercial product in 1985. The ARQUS-20 utilizes a proprietary defect detection algorithm to perform a die-to-die comparison on the wafer image in order to detect the presence of defects. The minimum defect specification on the ARQUS-20 is 0.5 micron at 5.5 minutes per square centimeter. Sony's ARQUS-20 is priced at ¥80 million.

Nidek

Nidek manufactures four models of wafer inspection equipment: the IM-8A, IM-8B, IM-6, and IM-9. All four models are based on the traditional operator-dependent microscope station for defect detection and classification. The difference between Nidek's 8A and 8B models is the configuration of input and output cassettes. The 8A and 8B are both priced at approximately ¥8 million. The IM-6 and IM-9 were new systems for Nidek in 1987 and are priced at ¥2.5 million and ¥6.0 million, respectively. Nidek competes with Nikon and Canon in Japan's wafer inspection market.

At SEMICON/Japan, Nidek introduced a new optical-based linewidth measurement system, which heralds its entry into this equipment category. The model CD10 is priced at ¥5 million. Deliveries begin in 1988.

Nikon

Nikon's newest CD measurement system, the LAMPAS-HD, was shown at SEMICON/Japan. First introduced at SEMICON/East in September 1987, the LAMPAS-HD system is a fully automated CD measurement tool and is capable of measuring linewidths down to 0.6 micron on silicon wafers with 1.0-micron photoresist lines. Nikon cites linewidth pattern resolution of 0.5 micron and repeatability specifications of less than 0.024 micron on chrome masks. As with the other LAMPAS tools, the HD employs a laser-based edge detection method. However, the HD utilizes a helium-cadmium laser with a wavelength of 325 nanometers, which improves linewidth measurement capability. While wafer throughput specifications are not yet available, the HD is expected to demonstrate the same wafer throughput as the LAMPAS M3, or faster. The HD is priced at ¥60 million. Shipments to Japanese customers began in October 1987.

In addition to its LAMPAS family of CD measurement systems, Nikon manufactures the Optistation line of wafer inspection stations. The Optistation 1 was first introduced in 1982, the Optistation 2 in 1984, and the 2A in 1985. In 1987, Nikon introduced the Optistation 1A. The difference between the Optistation 1 and 2 series is that the Optistation 2 series of wafer inspection systems can be interfaced directly in line with track and lithography equipment. Not all semiconductor manufacturers require this capability, so Nikon offers the Optistation 1 series that does not have the interface feature. The Optistation models 1 and 2 are 3–inch to 125mm compatible, whereas the models 1A and 2A are 100mm to 150mm compatible. The Optistation 2A is priced at ¥9 million; the new 1A is priced at ¥8 million.

New Linewidth Measurement Standard Announced

Although new equipment enhancements and announcements receive most of the attention at SEMICON/Japan, at the most recent show, a significant announcement was made in the area of metrology standards. VLSI Standards introduced the semiconductor industry's first calibration standard for in–process linewidth measurement. The new calibration standard provides accurate measurement capability for all optical linewidth measurement equipment that is based on reflected light microscopy. Calibration of linewidth measurement equipment for in–process wafer measurements is a very complex process because of the combination and variety of film materials and thicknesses that exist in the production of semiconductor devices. The new standard from VLSI Standards was designed for linewidth measurement of any thin film material (less than 400 angstroms in thickness). For the first time, a calibration standard exists that will allow process engineers a method for evaluating and comparing the capability of different optical linewidth measurement equipment. VLSI Standards, represented in Japan by TEL, developed the new standard in a joint program with the National Bureau of Standards.

Joseph Grenier
Kaz Hayashi
Peggy Marie Wood

Dataquest

Conference Schedule

1988

Semiconductor Users/Semiconductor Application Markets	February 22–23	Westin St. Francis Hotel San Francisco, California
Computer Products	March 1	Hotel Inter-Continental New York City, New York
	March 4	Back Bay Hilton Boston, Massachusetts
	March 7	Santa Clara Doubletree Inn Santa Clara, California
Copying and Duplicating	March 7–9	The Pointe at Squaw Peak Phoenix, Arizona
Imaging Supplies	March 9–10	The Pointe at Squaw Peak Phoenix, Arizona
Telecommunications	March 21–23	Hyatt Regency Monterey Monterey, California
Electronic Printer	April 5–7	Hyatt Regency Monterey Monterey, California
Imaging Supplies	April 7–8	Hyatt Regency Monterey Monterey, California
Japanese Semiconductor	April 11–12	Century Hyatt Hotel Tokyo, Japan
Computer Storage	April 18–20	Santa Clara Marriott Santa Clara, California
Color Conference	May 2–3	Hyatt Regency Cambridge Cambridge, Massachusetts
European Semiconductor	June 8–10	Gleneagles Hotel Auchterarder, Scotland
Display Terminals/Graphics and Imaging	June 13–15	Hyatt Regency Monterey Monterey, California
Electronic Publishing	June 16–17	Silverado Country Club Napa, California
European Copying and Duplicating	June 29–July 1	Bristol Hotel Kempinski Berlin, West Germany
Financial Services	August 28–30	Silverado Country Club Napa, California
Western European Printer	September 7–9	Hilton International Wien Vienna, Austria
Manufacturing Automation/CAD/CAM	September 12–15	Hyatt Regency Monterey Monterey, California
Personal Computer	September 21–23	Silverado Country Club Napa, California

(Continued)

Information Systems	September 30–October 7	Tokyo American Club Tokyo, Japan
Technical Computer	October 5–7	San Diego Princess San Diego, California
Semiconductor	October 17–19	San Diego Princess San Diego, California
European Telecommunications	October 19–21	Hilton International Brussels Brussels, Belgium
Office Equipment Dealer/ Electronic Typewriter	November 2–4	Hyatt Regency Cambridge Cambridge, Massachusetts
Asian Semiconductor and and Electronics Technology	November 7–8	Seoul, Korea
Industrial Automation	November 30–December 2	Palace Hotel Madrid, Spain

Dataquest
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Research Newsletter

SEMS Code: 1987–1988 Newsletters: February 1988–2

SEMATECH GOES TO AUSTIN—WHAT'S NEXT?

SUMMARY

During the month of January, Sematech made two key announcements concerning what it plans to produce and where it plans to produce it. The details of these announcements are are follows:

- On January 6, Sematech's board of directors unanimously approved Austin, Texas, as the site for the first U.S. semiconductor manufacturing consortium. In so doing, the board ended months of intense speculation concerning Sematech's intended location.

- On January 26, Sematech announced its manufacturing demonstration vehicles (MDVs). The devices that Sematech has chosen to produce, high-density DRAMs and fast SRAMs, are based on processes being donated by member corporations AT&T and IBM.

This newsletter, produced jointly by Dataquest's Semiconductor Industry Service (SIS) and Semiconductor Equipment and Materials Service (SEMS), looks at the following issues that have arisen in the wake of these recent Sematech announcements:

- The significance of the Austin site as an infrastructure serving the goals of the Sematech program

- The manufacturing choices now confronting Sematech as it undertakes its charter to restore the U.S. semiconductor industry to world class manufacturing competitiveness

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 437-8000, Telex 171973, Fax (408) 437-0292

SITE SELECTION CRITERIA

The responsibility for choosing a Sematech location fell to a site selection committee headed by Sanford L. Kane, vice president of industry operations for IBM's General Technology Division. In a document sent to participants in the site proposal process, Mr. Kane's committee outlined the site selection criteria. The stated criteria included the following:

- A 100,000– to 200,000–square–foot facility, preferably with existing clean room capability, that could be occupied by the fourth quarter of 1987
- At least 30 to 35 acres of property to accommodate a future facility
- Proximity to universities with which the site could maintain a "proposed ongoing relationship"
- Support from state and local governments in the form of financial and other incentives
- A quality of life for Sematech personnel that would take into account the cost and availability of housing, traffic congestion, and climate

WHY AUSTIN?

At first glance, Austin, Texas, seems to be overshadowed by some of its competitors in key criterion areas:

Funding

The University of Texas, Austin, pledged $50 million to purchase and retrofit a facility formerly owned by Data General. With the addition of other incentives offered by the university and state and local governments, the total funding offered by Texas came to an estimated $68 million. In comparison, Massachusetts had proposed a financial package valued at nearly $400 million, with Arizona, California, and New York offering financial incentives in the neighborhood of $100 million or more.

Facilities

While the former Data General building that will serve as Sematech's manufacturing facility meets the site selection requirements for immediate and expandable space, it lacks one significant feature: a clean room. Acceptance of the Massachusetts bid, on the other hand, would have given Sematech immediate access to the Massachusetts Microelectronics Center, located in Westboro, which is situated on 36 acres of land and includes an IC fab facility. The Arizona bid would have given Sematech the headquarters and wafer fab sites formerly belonging to SGS, with rent subsidized by bond money.

University Research Relationships

The close working relationship that Sematech will have with the University of Texas, Austin, is already evident from the fact that the university itself is funding Sematech's fab requirements. In addition, the university is allowing Sematech access to its Cray supercomputer and will build a permanent headquarters for the consortium at its Balcones Research Center.

Other site proposals, however, included highly attractive associations with university research programs. Arizona offered support valued at nearly $160 million from its state university system. New York's proposal would have given Sematech a complex of facilities at the Rensselaer Polytechnic Institute, making available its Centers for Integrated Electronics and Industrial Innovation. Also participating would have been the Rochester Institute of Technology, the semiconductor laboratory of Cornell University, Massachusetts Institute of Technology, and Carnegie Mellon Institute.

INFRASTRUCTURE WINS

With its choice of Austin, Texas, the Sematech site selection committee believes that it has chosen an infrastructure that will further the consortium's goal. As expressed by Sematech Board Chairman Charlie Sporck, that goal is to "ensure the domestic semiconductor industry's future competitiveness." Although some of the components of this infrastructure may not shine as brightly as those offered by competing states, Austin certainly touches all the bases: strong ties with a major university program, proximity to the Microelectronics and Computer Corporation (MCC), an aggressive program aimed at retrofitting the Data General facility for wafer processing by the end of this year, a centralized location, and an environment that is increasingly attracting technology industries.

However effectively other site proposals addressed these same infrastructure elements, the Austin site adds two others that make it unique:

- The close involvement of government at local, state, and federal levels
- The presence of leading-edge semiconductor manufacturing capacity

For an organization that clearly sees its mission in the context of a nationwide initiative to restore the United States to the front ranks of world class manufacturing, these elements could very well have tipped the scales in Austin's favor. A closer look at these elements follows.

Government Partnering

Texas politicians at the state and local levels are being credited with a masterful performance in putting together the Austin site proposal. When faced with the obvious disadvantage of a facility that lacked a clean room, Texas officials responded with a thorough and demanding clean room construction schedule. Then, they built a model clean room at the Data General site through the cooperation of a consultant and donations from equipment suppliers.

The support shown for Sematech at the state and local levels in Texas was mirrored at the federal level by the efforts of U.S. Representative J.J. Pickle, a senior member of the House Ways and Means Committee, and House Speaker James Wright. Sematech leaders have cited the efforts of these two Texas politicians in the saving of Sematech's $100 million federal grant from budget cutting.

Some of the losing states in the site selection contest have suggested that the choice of Austin may be as much a tribute to political clout as to the intrinsic advantages of the site itself. The fact remains, however, that in order to be successful, Sematech will depend on a partnering relationship with government. Texas has clearly demonstrated its intention, at all political levels, to support the Sematech program.

Where the Manufacturers Are

Dataquest's Semiconductor Equipment and Materials Service (SEMS) maintains a detailed data base on semiconductor manufacturers in North America. Much of the information that follows has been derived from the surveys and research that support the fab data base. A top-level view of the SEMS data base suggests that, from the standpoint of the regional dispersion of semiconductor manufacturing capacity, locating Sematech in the central region of North America makes sense. Looking at the wafer fab locations of the 10 largest U.S.-owned semiconductor manufacturers, most of whom are participating in Sematech, a regional profile appears in Table 1.

Table 1

Regional Dispersion of Semiconductor Fab Sites Among the Ten Major Sematech Participants

Company	Western	Central	Eastern
AMD	X	X	
AT&T			X
GE	X		X
Harris			X
HP	X	X	
IBM			X
Intel	X	X	
Motorola		X	
National	X	X	X
TI	X	X	X
Total	5	6	5

Note: The above table does not represent the actual number of facilities that a company has in a geographic region, but whether or not it has some manufacturing presence there.

Source: Dataquest
February 1988

Quoting Charlie Sporck, Sematech's "product" is "...manufacturing knowledge. This cannot be expressed as a single deliverable product, process, statement, or strategy." Because of Sematech's charter to further production-worthy semiconductor processes, locating in a state with a high-volume, leading-edge manufacturing base makes sense. Moreover, in terms of current, equipment-limited, semiconductor manufacturing capacity, Texas leads all other North American states.

Texas: Home of Leading Edge Capacity

Although California boasts the largest number of production-based fab lines currently operating in North America (97 of 255 locations), the fab lines in California have approximately half of the average start capacity of their Texas counterparts. In addition, 38 percent of today's 150mm and 200mm wafer capacity is in Texas.

This suggests that if someone wants to develop a start-up and a process technology, California is the place to go. If, however, a company wants to bring up volume production, it should be aware that a large portion is outside California—and most is in Texas. This difference in infrastructure of this activity is not lost on semiconductor manufacturers, as is evident in recent moves to Texas by VLSI Technology and Cypress Semiconductor. In fact, California has seen almost every major semiconductor company move its manufacturing eastward, as new capacity was required. Looking ahead, Dataquest believes that while California will continue to support more wafer fab lines during the 1990s, Texas is expected to have the highest capacity in North America.

WHAT NEXT FOR SEMATECH?

With its manufacturing site selected, Sematech is now faced with rolling up its sleeves and producing. Since the announcement of its formation in early 1987, the member companies of Sematech have held ongoing workshops to hammer out the consortium's objectives. Among the issues that have been settled are the following:

- Sematech will manufacture both DRAMs and fast SRAMs. Member company IBM will donate its 0.8-micron, 4Mb DRAM process to Sematech, while AT&T will contribute its 0.7-micron, 64K fast SRAM process based on the six-transistor cell.
- The processes are CMOS based.
- Sematech will begin its fab operations by early 1989.
- Sematech will be using equipment geared for high-volume production, but on a smaller manufacturing scale.
- Working devices produced by Sematech will be destroyed rather than sold. This will keep Sematech focused on the manufacturing demonstration vehicles (MDVs) that it is developing, rather than on making shipment commitments.

PRODUCING 16Mb SRAMS/64Mb DRAMS

In predicting just what type of MDVs Sematech will deliver, two points are important to note. The first is that, at present, 256K SRAMs (four-transistor cell) and 1Mb DRAMs, utilizing 1.0- to 1.2-micron processes, are the current technology drivers. The second is that, in 1989, Sematech will start out with 0.8- and 0.7-micron technologies that will be six months to one year ahead of the merchant semiconductor market. Dataquest is assuming that Sematech is serious about its avowed goal of achieving world class semiconductor manufacturing leadership within five years. Based on this assumption, Dataquest believes that by early 1994, Sematech expects to deliver the equivalent of a 16Mb SRAM (four-transistor cell) and 64Mb DRAM to its members, using a 0.35-micron CMOS process.

If Sematech is able to hit this assumed target, it could give its members a lead of one to one and one-half years ahead of the rest of the merchant semiconductor industry's predicted introductions of these devices. Dataquest does not expect the merchant semiconductor industry to be reasonably comfortable with 0.8-micron processes until 1990, and even then, these processes are not expected to be mainstream. Excluding the possible impact of Sematech, the merchant semiconductor industry is not expected to become equally comfortable with 0.5-micron processes until 1993, and with 0.35-micron processes until 1996.

SRAM/DRAM Pros and Cons

With Sematech's choice of both SRAMs and DRAMs as the MDVs, the pros and cons of both MDV choices are listed below.

DRAMs—The Pros

- IBM has contributed a 4Mb DRAM, plus all the manufacturing and engineering support that is necessary for a rapid and efficient technology transfer.
- IBM's DRAM uses a modular process architecture, which allows the construction of SRAMs or logic chips with only minor changes to the process sequence.
- DRAMs are proven as complex technology drivers.
- DRAMs are very high-volume products.
- DRAMs are conducive to very large wafer sizes.
- Some merchant semiconductor DRAM-technology expertise still remains in North America.

DRAMs—The Cons

- Limited DRAM capacity is left in North America.
- Possible limitations of technology transfer arise from IBM's proprietary photoresist technologies.

Fast SRAMs—The Pros

- AT&T has contributed a 64K SRAM using a six-transistor cell design.
- AT&T's SRAM is built with a process technology designed for making circuits such as logic chips, microprocessors, and ASICs.
- More fast SRAM expertise in North America is available to Sematech for the development and execution of the technology.
- AT&T's SRAM process sequence is shorter than IBM's DRAM process sequence and will, therefore, produce working silicon demonstration units first.

Fast SRAMs—The Cons

- Fast SRAMs do not drive the largest wafer sizes for the following two reasons:
  - The uniformity of the process across the wafer is critical to achieving uniform yields of the fastest SRAMs. Since one wafer can yield various classes of SRAMs, these uniformity issues are better addressed on smaller wafers. As wafer sizes get larger, process uniformity across the wafer is degraded.
  - The fast SRAM market is not a high-volume market and, therefore, is not conducive to the largest wafer sizes.

When looking at these issues, the best product for Sematech appears to be the DRAM. The DRAM is a high-volume, large-wafer technology driver, and some good on-shore expertise is available. With the additional selection of fast SRAMs, Sematech is working to meet the diversified needs of its 13 member companies. Sematech appears to have made the most logical choices concerning the types of devices it will develop and deliver.

WAFER SIZE

A number of important manufacturing decisions still face Sematech. Probably the most important near-term decision Sematech must make is whether to run 125mm, 150mm, or 200mm wafers initially. Sematech must also plan which wafer size it will use to deliver products to its member companies.

The processes offered to Sematech by AT&T and IBM are based on 125mm wafers. While there is a mixed bag of issues regarding wafer size, one thing is obvious: Sematech cannot expect to deliver a leading-edge process based on 125mm wafers when 150mm and 200mm wafers will, respectively, be the mainstream and leading-edge wafer sizes in 1994.

Wafer Size Pros and Cons

The following are the pros and cons that Sematech must resolve regarding the wafer size that it will begin with and the wafer size it will eventually deliver its MDVs on.

The Pros of 125mm Wafers

- 125mm wafers would allow for the quickest start with established 0.7– and 0.8–micron processes.
- Sematech could immediately begin to smooth out its fab operations with a well–understood wafer size.
- The industry as a whole is far along the learning curve with 125mm wafers.

The Cons of 125mm Wafers

- 125mm wafers are too small to be competitive in the 1994 time frame.
- Starting with this size will add one or possibly two necessary jumps in wafer size for Sematech during the next five years.

The Pros of 150mm Wafers

- The product could be delivered in 1994, at which time 150mm wafers will be mainstream.
- The industry has gained a fairly good understanding of 150mm wafer technology.

The Cons of 150mm Wafers

- No 150mm wafer processes have been offered to Sematech.
- If a 150mm wafer process is delivered in 1994, some companies (certainly IBM) will have to bear the expense and risk of bringing the process up to a 200mm process. At that time, there will be approximately 20 to 25 large 200mm fabs in North America.

The Pros of 200mm Wafers

- IBM could offer its 200mm process soon.
- This size would be difficult to start out with but could offer the most reward in 1994.
- It is easier to downsize from 200mm wafers to 150mm wafers than it is to jump up from 150mm to 200mm wafers.

The Cons of 200mm Wafers.

- No 200mm wafer processes are currently offered to Sematech.
- The 200mm wafer size would be a difficult size to start with in 1989.

- Some companies will not have 200mm wafer processes and will, therefore, have to downsize the process to 150mm, thereby adding cost and time.

- Some semiconductor equipment is not yet ready for 200mm wafer processing.

CONCLUSIONS

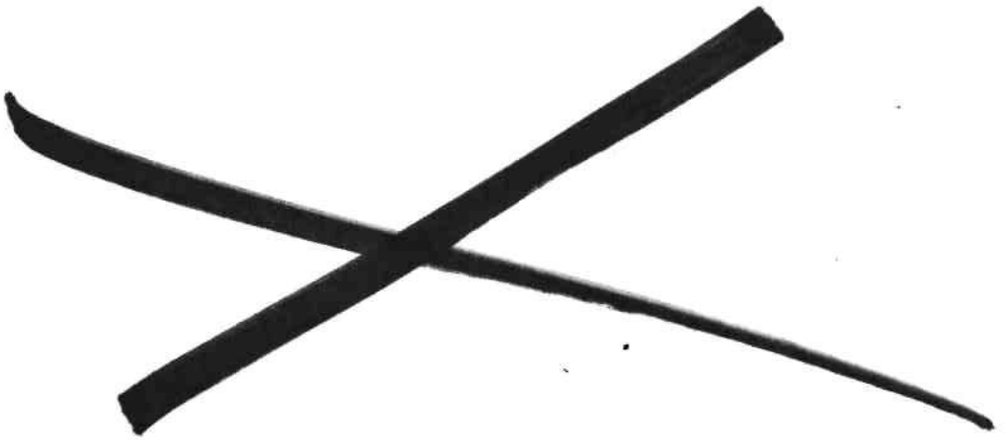
With a facility and products selected, a new sense of urgency now accompanies the manufacturing decisions facing Sematech. Based on the information concerning wafer size, the most likely scenario for Sematech could be any one of the following three:

- Starting out with the established 125mm wafer processes and enlist the help of IBM to make one jump up to 200mm wafers

- Starting out with 150mm wafers during 1989 and shift to 200mm wafers by 1991

- Starting out with 200mm wafers during 1989, assuming that IBM offers its 200mm wafer process and that the process is mature enough to be delivered

Mark T. Reagan
Michael J. Boss



March Newsletters

The following is a list of newsletters found in this section:

- SEMICON/Europa: A Slow Show For A Year Of Slow European Equipment Sales
  1988 - #11
- SPIE 1988: A Report on Advances in Spatial Metrology
  1988 - #9
- General Signal Acquires GCA-GCA is Back in Business
  1988 - #8
- SPIE 1988 A Report on Advances in Excimer Laser Lithography
  1988 - #7
- A Sampling of Sub-1.5-Micron Devices
  1988 - #6

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Research *Newsletter*

SEMS Code: 1987–1988 Newsletters: March
1988–11

SEMICON EUROPA: A SLOW SHOW FOR A YEAR OF SLOW EUROPEAN EQUIPMENT SALES

INTRODUCTION

The fourteenth SEMICON/Europa Exhibition was held at the Zuspa Convention Centre in Zurich, Switzerland, March 1 through to March 3. This show, organized by the Semiconductor Equipment and Materials Institute (SEMI), is the first of several equipment expositions sponsored by SEMI throughout the world this year.

SEMICON/Europa 1988 came and went amid whispers of a lackluster year in European equipment sales. The late, but intense, snow storm in Germany and Switzerland delayed many visitors to the show, and it appeared to Dataquest analysts that the exhibition was effectively over by noon on Thursday, even though the official closing was at 4:00 p.m. While SEMI logged approximately 6,800 attendees—8 percent more than last year's 6,300—it was a disappointing exposition compared to the frenetic activities of the 1983 and 1984 shows. About 50 percent of the stand space was taken by U.S. companies. Although European companies were well represented, their presence was somewhat down from previous years largely as a result of mergers and acquisitions.

In this newsletter, we will report on various front-end equipment and materials segments and on the mood in Europe in general.

SILICON EPITAXY

Both the epitaxial equipment and silicon epitaxy markets are driven by advances in MOS device processing. The pervasiveness of epitaxy in bipolar processes cannot prevent the decline of epitaxial equipment sales as MOS devices gain in performance and replace bipolar applications. In 1984 and 1985, silicon manufacturers added capacity in anticipation of the movement of epi processes into MOS production, and in particular, 1Mb DRAM manufacturing. This movement did not occur, however, and worldwide epitaxial equipment sales fell from $112 million in 1984 to $49 million in 1986 and have only risen to approximately $50 million in 1987.

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398 / (408) 437-8000 / Telex 171973 / Fax (408) 437-0292

The outlook for 1988, however, appears to be sanguine. Orders for epi reactors are up, but more significantly, MOS-epi wafer demand is beginning to outpace supply. SEH, Monsanto, Wacker, OTC, and DNS are pursuing aggressive epi wafer strategies worldwide and in Europe. They are not, however, using the new MOS-epi products introduced recently—namely, Applied's 7010 and LAM/Gemini's Tetron I. The lion's share of MOS-epi wafer production is produced on Applied's 7800 series reactors.

Silicon manufacturers will continue to be cautious, carefully keeping supply in tune with demand. Monsanto, for example, has recently purchased capacity from AT&T rather than adding reactors to its plant in St. Peters, Missouri. High-volume system purchases continue to await the movement of epi into DRAM products. Until now, epi wafers have been going into high-performance, CMOS logic and, in Japan, into CCDs.

ETCH

We saw the same cadre of dry-etch systems at SEMICON/Europa as were introduced within the last few years, but with some absences and some new products. Most significantly, the Japanese manufacturers did not show systems.

Leybold AG

Degussa purchased Leybold-Heraeus last year and provided funds for an aggressive attack on the equipment market. Leybold introduced a single-wafer, multichamber reactive ion etcher (RIE) system this year.

The Series 3000 Etcher, can be configured with 1 to 4 chambers. It can be configured uniquely for high-pressure operation for oxide and nitride or as an RIE for aluminum and aluminum alloys. The multichamber operation makes it suitable for low-pressure, low-etch rate processing and for multistep recipes. It can be configured for wafer sizes up to 200mm. The price is about $600,000 for two chambers. So far, two beta sites have been installed.

CIT/Alcatel

CIT/Alcatel introduced a two-chamber version of its CIT series reactors two years ago. Each chamber and handling system can be operated independently of the others. Approximately 30 of these systems have been installed so far. At this year's show, CIT/Alcatel introduced a microwave version of the CIT 260. The system uses technology licensed from CNET, a french agency (also licensed by Electrotech), that employs a network of alternating magnetic poles and microwave antennas around the periphery of a single wafer electrode. The system price is $750,000. Three systems have been installed to date.

CVD

Several companies have introduced new CVD systems in the last three years. Of these companies, Applied Materials has been very successful, shipping 30 systems into dielectric applications in eight months in 1987. Varian has also been successful with its

Model 5101, shipping systems into R&D and pilot applications for refractory metals. The new systems from Novellus and Focus have been very slow getting started. However, Focus has improved its temperature control and has shipped several systems since November. Novellus has moved slightly faster and had shipped about 10 systems by the SEMICON showing of the system.

Spectrum CVD, which had pulled its system off the market soon after introduction, reintroduced the system at SEMICON. The system is now a single-wafer, single-chamber configuration in lieu of a multichamber configuration. Spectrum claims typical throughputs of 30 wafers per hour (wph) for WSi_2 and 15 wph for selective tungsten. Of course, like all refractory-CVD vendors, Spectrum claims to have a "production-worthy" selective tungsten process. The price of the system is $600,000.

DIFFUSION AND PVD

Several companies introduced new diffusion or PVD systems—or modified their existing systems.

MTI

MTI introduced the SypherLine sputtering system, which it claims provides step coverage, film uniformity, and fine grain size that exceeds results of any other system on the market today. The system is available in two through-the-wall configurations: Class 10 and Class 100. The Class 10 system provides minimal clean room penetration and has a cassette/cassette load/unload capability. Each system includes an RF sputter etch module, a sputter deposition module, a cassette lock, and a transfer chamber.

The SypherLine "sputtering . . . plus" process features sideways deposition onto the wafer and an 8-1/2-inch diameter standard target independent of wafer size. The SypherLine can produce 2,500 wafers per target at a throughput of 45+ wafers per hour.

MTI reports that the SypherLine is now being used to fabricate 4Mb DRAM devices.

Varian

Varian introduced the M2000, an isolated-chamber sputtering system. The M2000 integrates free-standing and interchangeable modules. Each self-contained module has independent systems for vacuum, wafer handling, and process control. Modules are interconnected by a central wafer-handling system that is designed for high reliability and exceptional contamination control.

The M2000 is configured with modules for automated cassette-to-cassette wafer loading, central wafer handling, sputter deposition, and RF sputter etch. Process sequences can be tailored to provide optimum processing conditions for different devices. The M2000 can be used for either R&D or for production, and is designed for easy field upgradability and expansion to meet new process requirements.

Process modules can be easily disconnected and wheeled off-line for maintenance while the other modules continue to process wafers. The system is capable of handling gallium arsenide wafers.

Varian plans to introduce future process modules for CVD, RTP, and etch.

E.T. Electrotech

E.T. Electrotech introduced its Plasmafab ND 6210 PECVD system. The 6210 can be used for the deposition of oxide, nitride, doped oxide, and oxynitride. The 6210 offers increased process stability and features a TEOS (tetra–ethyl–ortho–silicate) liquid source for a more planarized film surface. It has a throughput of 25 wafers per hour and can be purchased in a beltless model.

Tempress

General Signal's Thinfilm Company introduced the Omega 5000 PECVD from Tempress. The new system is the result of a joint effort from Tempress and the University Twenty (Enschede, The Netherlands). The new system was developed for the deposition of silicon nitride layers. The Omega 5000 can be used in combination with other diffusion and/or LPCVD processes in the same four–stack furnace. The system is designed for low contamination. The features that have been incorporated into the Omega to achieve low particulates include a rounded scavenger, an RF coil connector at the back of the tube, and a newly redesigned boat. Additionally, the gas system is laid out vertically and is constructed of electro–polished piping with orbital welds.

MASKMAKING

We believe that one of the most significant events at SEMICON this year was the joint announcement by GCA and Ateq of a strategic alliance. Ateq will market and support GCA's photo–repeaters in the United States to U.S. mask shops. GCA will market Ateq's Core 2000 in Europe. GCA will terminate the laser pattern generator introduced two years ago. In addition, GCA and Ateq will cooperate on product and process development.

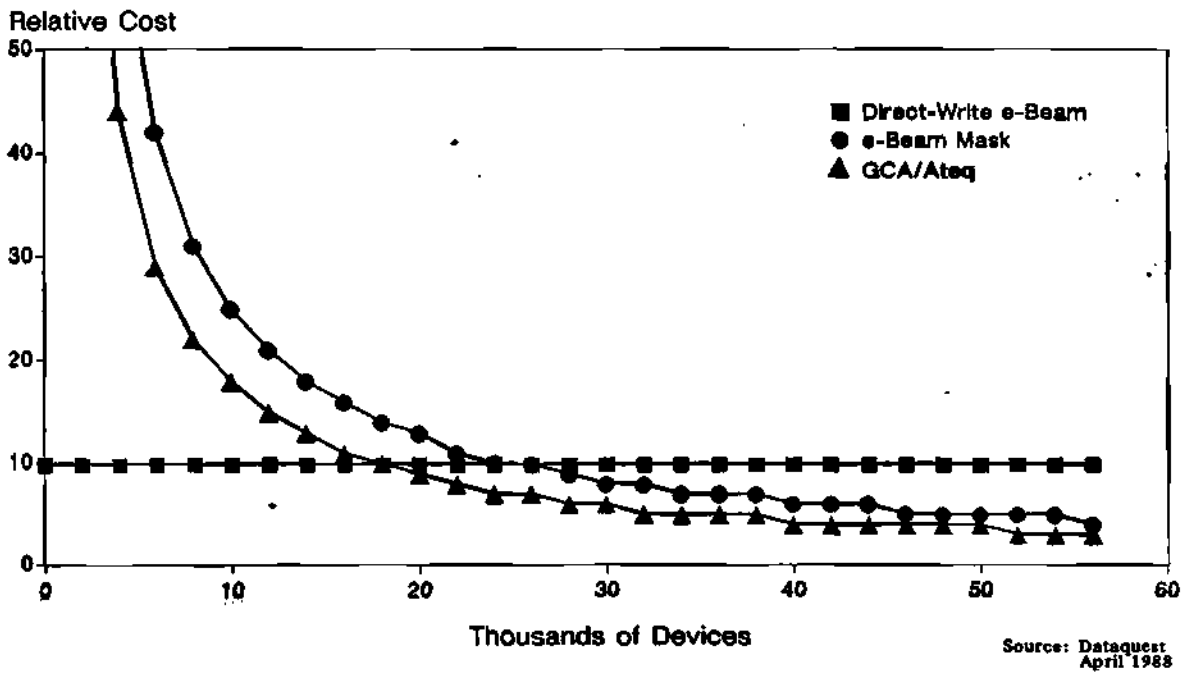
By bundling their products, the companies hope to give semiconductor manufacturers an alternative to direct–write e–beam and to give mask shops a low–cost, quick–turn alternative to e–beam.

Direct Write

Figure 1 represents an analysis of mask versus direct–write cost as a function of the number of devices produced. While the point at which both costs are equal can vary greatly depending on system price, mask cost, and device complexity, the graph shows that lowering the mask cost makes the semiconductor manufacturer much less likely to use direct write. The GCA/Ateq agreement proposes to provide a quick turn alternative to direct–write e–beam.

Figure 1

Pattern Replication Cost
Direct Write Versus Maskmaking



The companies claim that designs with geometries of 1.2 micron and greater can be transferred to reticles directly by the Core 2000 and then be produced on a stepper faster than with direct write. For geometries of less than 1.2 micron, reticles can be made by creating a 5x master on the Core 2000, using the GCA repeater to make a 5x or 1x reticle, then stepping the device on silicon, all of which is still faster than using direct-write e-beam.

Maskmaking Shops

If the procedure mentioned in the previous paragraph works, it could provide low-cost capacity in mask shops, be they merchant or captive, for ASICs or for standard products. The issue inevitably will be one of quality. The GCA/Ateq alliance has a long way to go before it demonstrates that this technology can produce masks and (ultimately) devices with the same yields that the e-beam technology has labored so long to enjoy.

The ability of GCA/Ateq to gain experience will be severely limited by the excess mask capacity that currently exists; mask shops do not need more capacity, low cost or otherwise. The development of silicon compilers and simulation software has greatly reduced the amount of prototyping that was necessary in ASIC manufacturing a few years ago. This advance has effectively doubled the mask capacity with little change in the installed base of e-beam systems.

We believe that GCA/Ateq will certainly achieve sales into a niche of quick-turn ASIC products. However, the potential for GCA/ATEQ to penetrate into high-performance applications and into commodity production does exist and is enhanced because of this alliance.

TRACK EQUIPMENT

Convac and MTI introduced new systems at SEMICON/Europa and Eaton announced new enhancements to its system.

Convac

Convac introduced the Module Series 6000 photoresist processing equipment. This system features a Class 1 local environment and is fully compatible with the SMIF concept. The Series 6000 has eliminated belt- and air-driven wafer transfer mechanisms by using four frog-leg pick-and-place wafer handlers. These frog-leg transfer mechanisms give the 6000 the ability to transfer wafers to any station within the module or to an adjoining module. The company claims that the frog-leg pick-and-place transfer mechanism is cleaner than the belt- or air-transfer method.

Another new feature of the 6000 is that the hot plates are stacked one atop the other, five high. Vapor prime stations are also stacked one atop the other. The company chose this configuration in order to reduce space requirements. Each module can be operated as a standalone module or integrated with other modules.

MTI

MTI introduced FlexiFab, a network of independent, single-process modules. Each self-contained module performs a complete process step. Each module has its own electronics, handling system, and facilities connections. Since the modules are linked only by communications and power to a master controller, the modules can be configured in a variety of ways to fit individual process needs. Each module is capable of both wet and dry process. The mean-time-between-failure of each module is estimated to be 900 hours.

Eaton

Eaton added some new features to its existing Spin-on-Glass System, the 6020XL. These new features include a new teflon tub, a full-coverage nozzle rinse, and a tub rinse.

Eaton also showed its complete Point and Go Operator Interface Model 6010XL for the first time. This system has a menu-driven touchscreen with capabilities in all major European languages. The 6010XL is retrofittable to all 6000XL systems.

STEPPERS

Although all of the major stepper companies were present at SEMICON/Europa, only GCA and Perkin–Elmer announced new products.

GCA

GCA introduced the 200mm ALS Waferstep wafer stepper for sub–micron production. The ALS 200 is intended primarily for 4– to 16–Mb production. The system has improved stage precision, registration, and overlay. It offers tightly controlled machine–to–machine matching. The system can be equipped with either i–line or g–line optical systems. Lenses for the ALS Series are available from either GCA Tropel Division or Carl Zeiss Inc. The system can be configured with the GCA Environmental Chamber Model 8860. The system features a dark field alignment system and is usable in a 100 percent die–by–die operation or with flexible die sampling routines. The ALS 200 features a 0.15–micron registration and a 0.25–micron overlay and has an average selling price of $1.2 million to $1.4 million, depending on the type of lens used. GCA claims that the system has a 95 percent uptime.

Perkin–Elmer

Perkin–Elmer introduced the OMS 1 overlay measurement system at SEMICON/ Europa. The new system can monitor overlay, suggest correction coefficients, and perform overlay measurement at many sites on production wafers. Software is available for overlay correction for both the Micralign 600 HT and Micrastep stepper.

EUROPEAN MOOD

Dataquest's Malcolm Penn reported at SEMI's Tuesday morning press conference that in 1987, the European semiconductor industry experienced a 14 percent growth rate in U.S. dollars (to $6,355 million), which equates to about 9 percent in local currency. The United Kingdom showed the most dynamic growth in Europe and now accounts for 37 percent of all European wafer fabrication manufacturing capability.

With the fabrication industry entering what might be described as a fairly "mature" phase compared with the volatility of earlier years, growth is expected to settle into the range of 10 to 12 percent CAGR, while the outlook for 1990 considered to be good.

Equipment vendors at the show are experiencing lackluster sales in Europe while Japan and the ROW markets have been heating up. Equipment and materials vendors expect European equipment sales to be flat or, at best, up only slightly in 1988.

In the last two years, Europe has provided equipment vendors with a growing market while the United States and Japan were in severe slumps. European governmental monies have been disseminated into European semiconductor manufacturers—most notably Philips, Siemens, and Thomson—as Europe has attempted to regain its lost position in electronics. It is time for European manufacturers to demonstrate the wisdom of their strategies as they fill this new capacity with new production.

George Burns
Kathleen Killian
Robert McGeary

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Research *Newsletter*

SEMS Code: 1987–1988 Newsletters: March 1988–9

SPIE 1988: A REPORT ON ADVANCES IN SPATIAL METROLOGY

INTRODUCTION

SPIE (Society of Photo–Optical Instrumentation Engineers) held its 1988 Santa Clara Symposium on Microlithography from February 28 through March 4 in Santa Clara, California. This annual event is an important international conference on advances in lithography, including optical, electron–beam, X–ray, and ion–beam technologies; in IC metrology, inspection, and process control; and in resist technology and processing. During the week–long conference, 141 regular papers were presented, along with another 56 papers presented during poster sessions. There were an estimated 1,500 attendees this year, compared with 1,300 in 1987 and 1,100 in 1986. Approximately 30 percent of this year's attendees came from outside of the United States.

In the area of IC metrology, inspection, and process control, a total of 49 papers were presented, including 31 regular papers and 18 poster session presentations. A diverse range of topics was discussed, including SEM metrology, imaging, and applications; current and emerging technologies in submicron optical metrology; overlay and registration; automated wafer inspection; and process control and automation of lithographic processes.

Spatial metrology, in particular, combines linewidth measurement with three–dimensional line profilometry. Because of the importance of spatial metrology in future IC manufacturing, this newsletter focuses on the presentations at SPIE that addressed the three technologies providing this capability today: scanning electron microscopy (SEM), confocal scanning laser microscopy (CSLM), and coherence probe imaging. This newsletter concludes with a look into a future technology development in spatial metrology—atomic force microscopy.

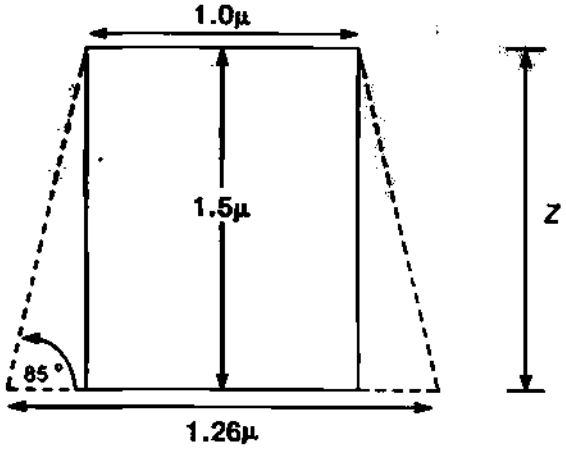
Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398 / (408) 437-8000 / Telex 171973 / Fax (408) 437-0292

SPATIAL METROLOGY—LINEWIDTH MEASUREMENT AND PROFILOMETRY COMBINED

As semiconductor manufacturers continue to shrink line geometries, the slope of the side walls becomes increasingly important in linewidth measurement. Few linewidth measurement systems today, however, are capable of capturing the entire line profile to establish and correlate linewidth measurement with the actual shape of the line. How much can the slope of the side wall affect a linewidth measurement? A simple geometric example shown in Figure 1 illustrates that for a 1.5–micron–thick line, an 85–degree slope of the side wall can result in a bottom–layer measurement of 1.26 microns, 25 percent larger than a 1.0–micron top–layer measurement. This difference in linewidth between top and bottom becomes more enhanced as line geometries are reduced to submicron dimensions and wafer topographies become more pronounced. Thus, spatial metrology—line profilometry combined with linewidth measurement—is essential for submicron metrology.

Figure 1

Example of Linewidth Variation



Source: Dataquest March 1988

SEM Metrology

Prior to the development of the new optical techniques of confocal scanning laser microscopy and coherence probe imaging, SEM systems were the tool of choice to generate three–dimensional images of line profiles. Although once relegated strictly to the analytical lab, many SEM systems today have been redesigned to meet the needs of nondestructive submicron measurement in a production environment. These systems, however, are typically characterized by low throughput, complicated operations that require a skilled operator, and sensitivity to environmental factors such as stray magnetic fields and vibrations.

At the SPIE symposium this year, Opal Technologies (Nes Ziona, Israel) discussed a new low-voltage SEM tool for spatial metrology, the Opal 702. This system has been specifically developed for fully automated in-process e-beam metrology applications. It provides simultaneous measurement of the top, middle, and bottom of submicron features, and requires no operator intervention during measurement operations. The Opal 702 system combines low accelerating voltage—which reduces substrate damage—with extremely low electron dose in order to reduce charging effects. Additional design features provide the system with immunity against environmental interferences such as electromagnetic fields and vibrations.

Opal Technologies claims that the 702 exhibits an impressive throughput rate that is comparable to most optical-based systems: 30 wafers per hour at 5 sites per wafer, 20 wafers per hour at 12 sites per wafer, or 10 wafers per hour at 40 sites per wafer. This rate is achieved through a special mechanical design that provides multiwafer processing capability through parallel operations. In comparison, other SEM linewidth measurement systems designed for the production environment typically have a throughput rate on the order of 8 to 15 wafers per hour at 5 sites per wafer.

Confocal Scanning Laser Microscopy (CSLM)

At this year's SPIE symposium, six papers were presented that discussed various applications of CSLM. In comparison, only one paper on CSLM was presented at the 1987 symposium, and none was presented in 1986. There has been significant interest in CSLM systems because they provide superior image resolution and depth discrimination compared with traditional white-light microscopy techniques. In addition, because of a characteristic narrow depth of focus, line profile information may also be obtained with this technique.

One of the important areas of development in confocal scanning laser microscopy is the application of short-wavelength laser sources. This topic was discussed by both Heidelberg Instruments and SiSCAN Systems at this year's symposium. Although both companies initially developed their CSLM systems with 488nm laser sources, they are now investigating UV sources. Shorter-wavelength sources offer several advantages over 488nm illumination, including improved resolution and depth of focus. In addition, most photoresists have higher absorption profiles at shorter wavelengths and, thus, appear more opaque; this means that interference effects will be attenuated significantly.

SiSCAN Systems

SiSCAN Systems reported on measurement performance of a CSLM system utilizing a 325nm helium cadmium laser. In addition to improved resolution of 0.2 micron, the company also reported that 325nm data, obtained using two common optical photoresists, is less sensitive to substrate conditions than 488nm data. Dataquest believes that SiSCAN will ship its first system with a 325nm laser source in early 1988.

Heidelberg Instruments

Heidelberg Instruments discussed three different measurement modes for its CSLM system: normal contrast, quasi-incoherent confocal contrast, and ultraviolet confocal contrast. Quasi-incoherent confocal contrast is a new technique for Heidelberg Instruments and provides good contrast for measurement of top layers of transparent films. The ultraviolet confocal contrast technique uses a 355nm source in order to increase photoresist absorption and minimize the interference effects previously mentioned.

In addition, Heidelberg Instruments presented some technical details of its beam–scanning CSLM system. In contrast to SiSCAN, Heidelberg's system relies upon a beam–scanning rather than object–scanning mechanism. In Heidelberg's design, telecentric optics are used to scan the beam over a fixed wafer sample; while in SiSCAN's system, the laser beam is held in a fixed position and the wafer sample is moved beneath the beam in a raster pattern. Heidelberg Instruments believes that beam scanning has substantial benefits over object scanning, in particular, for extending CSLM applications to defect detection. The company is currently developing an automatic defect inspection system that incorporates its CSLM technology. It plans to introduce the system in fourth quarter 1988.

Other CSLM Topics

Several other topics on CSLM were discussed, including:

- A comparison of measurement accuracy for a CSLM system, a low–voltage SEM, and a bright field microscope measurement system (E. Leitz, GE Micro–electronics Center)
  - The major advantages of CSLM over other systems include high contrast and shallow depth of focus, which increase lateral resolution.
- A confocal imaging system that generates a complete image of the sample in real time by scanning multiple spots across the sample (This is achieved by illuminating several thousand pinholes in a rotating disk above the sample surface.) (Stanford University)
  - This technique is contrasted with conventional confocal systems, which scan a single spot of light over the sample or move the sample under a beam, in a raster pattern, to build up an image pixel by pixel.
- Differential and confocal differential phase contrast in scanning optical microscopy (Philips Research Laboratories)
- CSLM as a nondestructive alternative to SEM cross–sectional measurements in the metrology of oxide isolation structures (Philips Research Laboratories/Signetics Corporation)

These topics, combined with the work of Heidelberg Instruments and SiSCAN Systems, demonstrate that there is significant interest in technology development in the area of CSLM.

Coherence Probe Imaging

At the 1987 SPIE symposium, KLA Instruments first reported on coherence probe imaging, a new technology it was developing for submicron metrology. This year, the company discussed its new product, the KLA 5000 Coherence Probe Metrology System. This is the first system to utilize coherence probe imaging for spatial metrology. (Coherence is a property of light that describes the correlation between the amplitude and phase of light at any one point compared with another.)

In this technique, three–dimensional images are produced by calculating the degree of coherence between corresponding pixels in the object and reference image planes of a Linnik interferometer. Linewidth measurement algorithms generate independent

measurements of the top, bottom, and height of the line profile. Similar to CSLM, the system has a very narrow depth of focus, such that all the parts of the image that are out of focus appear dark while those in focus appear bright. KLA believes that several advantages of coherence probe imaging over CSLM include better z-axis resolution and the ability to use broadband illumination to eliminate unwanted interference effects caused by laser sources.

Measurement resolution of the KLA 5000 is currently quoted at 0.7 micron, although the company anticipates that this will be extended to smaller geometries in the future. Wafer throughput is 40 to 45 wafers per hour at five measurement sites per wafer. This is slower than the KLA 2020 and 2005 at 80 to 90 wafers per hour, but approximately 40 to 60 percent faster than most other optical-based linewidth measurement systems.

The KLA 5000 is currently in beta site, and the company expects shipments to begin in late summer. The system, priced at approximately $380,000, has been developed and will be manufactured by KLA Israel, a wholly owned subsidiary. KLA Instruments is the only company that offers a metrology system based on coherence probe imaging and has applied for patents on its technology.

THE FUTURE

Atomic Force Microscopy

IBM's T.J. Watson Research Center presented a paper on the subject of spatial metrology with an atomic force microscope. (This was the only invited paper of the 49 presented during the two-day session on IC metrology, inspection, and process control.) Atomic force microscopy is based on the technology of scanning tunneling microscopy, for which IBM Zurich researchers were awarded the 1986 Nobel Prize in Physics. Although scanning tunneling microscopy can look only at conducting and semiconducting surfaces, researchers at IBM are modifying this technique to look at surfaces of nonconducting materials such as photoresist.

In atomic force microscopy, the tip of a needle is translated across a sample at a height of approximately 100 angstroms above the surface. According to IBM researchers, it is possible to map out a surface of constant Van der Waal force that, to first order approximation, corresponds to the topography of the surface. Atomic force microscopy provides a nondestructive measurement technique with 50-angstrom resolution. Unlike optical metrology, resolution for an atomic force microscope is not governed by the wavelength of light but, rather, by the size of the needle tip. By using a needle tip made of iron, it is also possible to map out surfaces of constant magnetic forces; this technique has applications in the measurement of thin-film magnetic heads.

To date, IBM has designed and built an atomic force microscope system on an optical bench. The company, however, is evaluating future plans for design of an 8-inch-wafer system. Atomic force microscopy is still in the very early stages of development, and has several experimental and theoretical hurdles to overcome before it can be applied in a semiconductor production environment. Dataquest believes, however, that atomic force microscopy with 50-angstrom resolution may well be one of the most important measurement technologies for semiconductor processing in the next decade and the next century.

Peggy Marie Wood

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Research *Bulletin*

SEMS Code: 1987-1988 Newsletters: March 1988-8

GENERAL SIGNAL ACQUIRES GCA—GCA IS BACK IN BUSINESS

GCA announced on March 14 that it had entered into an agreement with General Signal whereby GCA would become a wholly owned subsidiary of General Signal. This acquisition has created a new force in the equipment industry, injected new life into GCA, and will be synergistic for both General Signal and GCA. As a result, GCA—which has been faltering in the marketplace, not because of its well-respected technology but because of the uncertainty of its future—is suddenly infused with credibility and back on the street as a viable competitor.

FINANCIAL

The years 1985 to 1987 were traumatic for GCA; everyone is familiar with the company's financial woes during this time, so there is no need to rehash them here. Perhaps nothing indicates GCA's problems over this time more than the shrinkage in its facilities. GCA's 1984 10-K report listed 15 major facilities totaling 1,220,000 square feet; by the end of 1986, this area had shrunk to 5 facilities and 544,000 square feet (which is still a lot of space for an $80 million company).

Table 1 shows the performance of GCA and General Signal over the 1984 through 1987 time period. Almost all of GCA's sales represent semiconductor equipment sales into the semiconductor industry. General Signal's Semiconductor Equipment Group, one of the company's six operating groups, accounted for only about 13 percent, or $200 million, of its 1987 sales.

Table 1

Financial Performance of GCA and General Signal
(Thousands of Dollars)

	1984	1985	1986	1987
GCA				
Net Sales	$ 240,097	$ 156,484	$ 123,147	$ 80,280
Income (Loss) from Operations	$ 33,099	($ 94,240)	($ 31,696)	($ 56,409)
Net Income (Loss)	$ 28,569	($ 145,472)	($ 24,290)	($ 9,452)
General Signal				
Net Sales	$1,787,000	$1,801,000	$1,583,000	$1,603,000
Net Income	$ 109,000	$ 49,000	$ 75,000	$ 69,000

Source: Dataquest March 1988

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 437-8000, Telex 171973, Fax (408) 437-0292

SEMICONDUCTOR EQUIPMENT

GCA's main products for the semiconductor industry include wafer steppers, photoresist processing (track) equipment, and reactive ion etchers. Three of the operating units within General Signal's Semiconductor Equipment Group—Drytek, Semiconductor Systems Inc. (SSI), and Ultratech Stepper—compete with GCA in these equipment segments. In addition, GCA manufactures maskmaking equipment (optical pattern generators and photorepeaters) and optical components through its Tropel division.

Lithography

In terms of the final 1987 worldwide installed base for all wafer stepper manufacturers, the rankings were GCA (1,216 steppers), Nikon (1,105), and Ultratech (490). The announced General Signal/GCA (GS/GCA) combination now will be in first place with 1,696 steppers. In terms of current sales, however, the GS/GCA combination is a distant second to Nikon. In 1987, Nikon shipped 230 steppers, while GS/GCA shipped 125. When Canon and Hitachi are also considered, the Japanese are still very much entrenched as the leading stepper manufacturers. In steppers, the main issue for GS/GCA will be in defining a long-term strategic plan that encompasses both 1X and 5X technologies.

General Signal will now have access to GCA's Tropel division. Tropel originally made the lenses for Ultratech, but for competitive reasons, Ultratech had to seek an alternative lens source. Tropel also has strength in interferometry, which is very important in lithography. The financial backing of General Signal in the GS/GCA combination also has implications for optical pattern generation, which may enjoy a resurgence due to the progress recently noted in this area.

Photoresist Processing Equipment

SSI's 1987 sales in track equipment were $11 million, while GCA's sales were $7 million. The combined GS/GCA sales of $18 million should be compared with the leading U.S. manufacturer of track equipment, Silicon Valley Group, whose 1987 track sales were $33 million. Since most of the emphasis of the acquisition has been focused on lithography, the ramifications of the acquisition on track equipment have not yet been fully explored. There are, however, some interesting geographical points. SSI, for instance, has not done well in Europe, an area where GCA has been strong.

Reactive Ion Etch Equipment

Drytek's 1987 sales of dry etch equipment were $17.0 million, while GCA's sales of its new reactive ion etcher were minimal at $3.5 million. These sales should be compared with the worldwide leader of reactive ion etch equipment, Applied Materials, which had 1987 sales for this equipment of approximately $90.0 million.

Because there is considerable overlap of applications between GCA and Drytek, they cannot be allowed to compete against each other for very long. We believe that there will be an advantage in pitting the lower-priced GCA etcher against Lam and Tegal. The higher-priced Drytek system can incorporate GCA's triode technology and compete against Applied Material's hexode etcher. This system could eventually be used in the integrated vacuum technology that IBM seeks.

Joseph Grenier
Robert McGeary
Peggy Wood

Dataquest
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Research Newsletter

SEMS Code: 1987–1988 Newsletters: March
1988–7

SPIE 1988
A REPORT ON ADVANCES IN EXCIMER LASER LITHOGRAPHY

SPIE (Society of Photo–Optical Instrumentation Engineers) held its 1988 Santa Clara Symposium on Microlithography from February 28 through March 4 in Santa Clara, California. This annual event is an important international conference on advances in lithography, including optical, electron–beam, X–ray, and ion–beam technologies; in IC metrology, inspection, and process control; and in resist technology and processing.

Over the week–long conference, 141 papers were given, along with another 56 papers given via poster sessions. There were an estimated 1,500 attendees, compared with 1,300 in 1987 and 1,100 in 1986; approximately 30 percent of this year's attendees were from outside the United States.

In the lithography area, 75 papers were presented; 13 of these papers concerned the use of excimer lasers in lithography. Because of the importance of excimer lasers in future IC manufacturing, this newsletter will focus on the advances in this technology as presented in the 13 papers.

EXCIMER LASER LITHOGRAPHY

Before jumping into the results of the 1988 symposium, it is beneficial to discuss a little of the history of excimer laser lithography as presented at earlier symposiums.

Previous Symposiums

The first paper on excimer laser steppers presented at the SPIE Santa Clara Symposium on Microlithography was in 1983 by K. Jain of IBM, who described the first results of IBM's work in this area. The next paper on the subject was presented at the 1986 Symposium by V. Pol of AT&T. He described a modified GCA stepper with a 248nm krypton fluoride (KrF) laser that was able to obtain a practical resolution of 0.5 micron and a resolution of 0.4 micron in the laboratory. In 1986, only one other paper on excimer lasers was presented; it described the use of excimer lasers to etch diamond and diamond–like films.

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398 / (408) 437-8000 / Telex 171973 / Fax (408) 437-0292

At the 1987 symposium, a half-day session devoted to the subject of excimer laser lithography included the presentation of seven papers. D. Markle of Ultratech talked about the problems and potential of deep UV lithography, and K. Jain of IBM gave an overview of current developments in excimer laser lithography. AT&T described the work it was doing in defining the characteristics of an excimer laser suitable for lithography. GCA, Matsushita, and Nikon described, in separate papers, various aspects of the KrF excimer laser stepper that each has under development; they unanimously concluded that 0.5-micron resolutions could be obtained. Besides these six papers in the lithography area, General Electric discussed the use of excimer lasers to etch polymers.

In summary, the feeling after the 1987 session was that optical lithography would probably get down to 0.5 micron, and that the advances in excimer laser lithography had pushed out, once again, the advent of X-ray lithography.

1988 Symposium

As Table 1 shows, a lot of worldwide development activity is occurring in excimer laser lithography. This activity was reflected at this year's symposium, where an entire day was devoted to this subject. Thirteen papers in four sessions were presented on various aspects of excimer laser lithography, five of which were by companies listed in Table 1. (Although IBM is the source for Table 1, it is not included in the table even though it is investigating excimer laser lithography. IBM did, however, give two papers on this subject throughout the day.) The following sections describe the salient points of the various papers.

GCA

GCA described its KrF excimer laser steppers. One system was shipped to IBM, Federal Systems Division, in Manassas, Virginia, as part of a VHSIC contract; it was accepted in September 1987. The stepper uses a Tropel 10-1435 lens with a 10X reduction ratio, a 14mm diameter field size, and a numerical aperature (N.A.) of 0.35 (hence, the 10-1435 designation). Total depth of focus was 1 micron. GCA showed SEM photos of very nicely resolved 0.35-micron lines/0.7-micron spaces and 0.5-micron lines/space in an IBM resist.

GCA shipped a second system to IBM, where it is now undergoing acceptance tests. This stepper has a Tropel 5-2035 lens, a 5X, 20mm diameter, 0.35 N.A. lens. Both of the Tropel lenses are made with fused quartz.

Focus dependence upon temperature is -4.6 micron/C°. To compensate for this, the GCA excimer laser stepper incorporates an atmospheric compensation system (ACS) that monitors the lens temperature, ambient temperature, relative humidity, and barometric pressure. Output of the ACS goes to the stepper autofocus system to maintain long-term focus stability.

Matsushita

Matsushita's Semiconductor Research Center described its KrF stepper. The system uses a 5X, 21.2mm diameter, 0.36 N.A. quartz lens, with a total physical length of 675.5mm. A new compact KrF laser has been developed that can deliver up to 84 millijoules (mj) of energy per pulse. At 40mj, pulse energy stability is ±5 percent. Spectral bandwidth is 0.007nm with a ±0.001nm stability. Typical pulse rate is 200 pulses per second. Gas exchange in the laser is continuous, and switching lifetime is 3×10^9 pulses.

Matsushita concluded that KrF excimer laser lithography with single-layer resist has been confirmed as an effective tool for the fabrication of 0.5-micron devices such as 16Mb DRAMs. However, advances still need to be made in excimer lasers and stepper alignment systems.

Rutherford Appleton Laboratory

Rutherford is a U.K. government-funded lab investigating excimer laser lithography with 1X Wynne-Dyson optics. Rutherford is funding its own work in this area, although there has been some cooperation with Ultratech Stepper. (A piece of history: Dyson, an Englishman, designed a lens back in the late 1950s that was later improved by Wynne, another Englishman. Hershel, an American, further improved the Wynne-Dyson lens; this is the Wynne-Dyson-Hershel lens currently used in the Ultratech 1X stepper.)

There are two approaches to the excimer laser/lens system. One approach is to use a narrow-band excimer laser source (bandwidth of 0.001 percent) and construct the lens from a single material such as quartz; this is the approach taken by GCA, Nikon, and others (see Table 1). Alternatively, a wide-band laser (bandwidth of 0.1 percent) can be used with a lens constructed from materials of different refractive indices in order to provide chromatic correction; this is the approach taken by Rutherford, Toshiba, and Ultratech.

Rutherford described the results of its lens, which is fabricated from quartz and lithium fluoride. It also touched on other applications of excimer lasers in the semiconductor industry such as micromachining and laser-assisted chemical processing.

Admon Science

Admon Science is a Japanese venture business founded in 1986; the major shareholder is Mitsui. Admon described its narrow-band KrF laser and monochromatic lens. The compact laser has a bandwidth of 0.003nm with 17mj pulse energy. The lens has a 0.36 N.A. and a 15mm x 15mm field size. The laser/lens combination has a resolution of 0.4 micron when the laser bandwidth is set to 0.007nm. Admon provided the laser and lens to Matsushita for the work reported above.

Nippon Telegraph and Telephone (NTT)

NTT's LSI Laboratories described the effects of coherence of the laser source on the patterning characteristics. NTT used a 5X lens with a 0.42 N.A. and a 10mm x 10mm field size. The KrF laser bandwidth was narrowed by inserting etalons in the laser cavity such that bandwidth could be varied from 0.003nm to 0.007nm; coherence was also varied. With a bandwidth of 0.003nm, NTT was able to obtain a resolution of 0.3-micron lines and spaces.

Lambda Physik and Lumonics

Lambda Physik and Lumonics described, in separate papers, the development work they are doing in the area of excimer lasers for use in lithography. Requirements for such a laser include narrow bandwidth, center wavelength stability, wavelength tunability, and stabilized energy output.

Lambda Physik's laser has a bandwidth of 0.0032nm, peak wavelength stability of 0.00032nm, and a stabilized output power of 2 to 3 watts. Average stabilized pulse energy is 10 to 15mj. Lambda Physik also gave some maintenance specifications—for a 200Hz pulse rate and 50 percent duty cycle, optics maintenance is 1×10^8 pulses; major overhaul is required at 5×10^8 pulses.

Lumonics estimated that 2,000 excimer lasers were probably installed by 1986, but that industrial applications are just now emerging. Lumonics contrasted the industrial requirements for excimer lasers with the much more stringent requirements for lithography. It has taken its Index 200 conventional excimer laser, and, by adding external control and stabilization circuits, converted it to the Index 300 excimer laser for lithography. Typical performance specifications for the Index 300 are 2-watt average power, 10mj pulse energy, 200Hz pulse repetition rate, 0.003nm bandwidth, and wavelength stability of 0.001nm.

GCA/Tropel and Leitz-IMS

GCA/Tropel and Leitz-IMS described, in separate papers, bench-top excimer laser imaging systems for R&D applications. The idea is to provide inexpensive systems for the investigation of excimer laser lithography and resist development.

The GCA system occupies 2 square feet of space without the customer-supplied source, which can be either an excimer laser or a mercury arc lamp. The system features a stable platform with interchangeable lenses and manual focus control. The first lens to be offered is a 20X, small-field, 248nm lens whose N.A. can be continuously varied from 0.1 to 0.6. At the 0.6 N.A., the field size is 0.7mm diameter. Resolution of 0.2 micron has been obtained with the lens. The system, which looks like a big microscope, can handle 150mm wafers. The first system will be shipped to the University of California, Berkeley. Cost of the system, without the source, is $90,000.

Leitz-IMS described a similar system with interchangeable 15X and 36X lenses that can obtain 0.2-micron resolution. Leitz-IMS cited the following applications of excimer laser lithography: direct resist imaging with single-pulse ablation, latent exposure imaging, multilayer processing, alignment mark ablation, and customization of ICs. Leitz-IMS's system is priced at $200,000 with the excimer laser, and $120,000 without the source.

Other Papers In Excimer Laser Lithography

Perkin-Elmer discussed exposure dose control strategies for excimer lasers in lithography. This is a significant issue when using pulsed excimer lasers since they often exhibit relatively large and variable pulse-to-pulse output. Integration of many laser shots is generally required to obtain the required precision in total exposure energy at the wafer. However, laser pulse energies can be sufficiently high so that the minimum number of pulses required per exposure is determined by the exposure precision requirements rather than the total energy demands.

The Massachusetts Institute of Technology's Lincoln Laboratory discussed its work in patterning 0.13–micron lines and spaces in several thin–film materials with an argon fluoride (193nm) excimer laser. Materials included diamond–like carbon (dry develop) films and PMMA (wet develop) films. MIT noted that, as recently as one year ago, it was not thought possible to obtain 0.13–micron resolution with optical lithography.

IBM's T.J.Watson Research Center gave a paper on the effects of 248nm excimer laser radiation on chromium mask damage. IBM found chromium damage on the masks at relatively low energy levels.

Excimer Laser Maskmaking

IBM Germany described its work in using excimer lasers in the maskmaking process. In 1982, IBM equipped a GCA 3600 pattern generator with a 308nm excimer laser to expose the photoresist in a "flash–on–the–fly" mode with only one 13ns pulse per flash. The system has been in use for almost four years with a very high reliability. IBM said that it has been used to generate more than 700 reticles, which translates to about 250 X 10^6 flashes over the four–year period. In 1985, 134 reticles were manufactured, with 50 X 10^6 flashes. Some advanced reticles that were manufactured include one that required 4.5 X 10^6 flashes that took 42 hours to make, another required 4.2 X 10^6 flashes and took 14 hours, and a third required 2.5 X 10^6 flashes and 23 hours.

DATAQUEST CONCLUSIONS

Many speakers noted the recent increase in activity in excimer laser lithography. At last year's symposium, as noted above, the feeling was that optical lithography would probably extend to 0.5 micron. This year, the opinion was that optical lithography would definitely be used for 0.5–micron work, and that a high probability of extension to 0.35 micron exists. In fact, some were of the opinion that 0.35–micron resolution would be definitely obtainable in production. In spite of the development effort that still must be undertaken in the areas of excimer laser sources, lens, alignment, and possible mask damage, the industry (at least the optical people) are very bullish on optical lithography. One only needs to look at the rapid progress that has been made in the last year or so to feel optimistic about the progress yet to come.

Joe Grenier

Table 1

Survey of Reported Developments in Excimer Laser Lithography

Company	λ	N.A.	nX	Field Size (mm)	Resolution (mm)	Alignment Precision (±mm)	Lens Type	Lens Optics	Laser Δλ(nm)	Line Narrowing by
AT&T	248nm	0.2-0.38	5	14.5-20ϕ	0.52	0.25 (2σ)	Mono	Quartz	0.005	Etalon
GCA	248nm	0.35	5	20ϕ	0.57	0.3 (3σ)	Mono	Quartz	-	Dispersive Elements
Matsushita	248nm	0.37	5	15 x 15	0.55	0.3 (3σ)	Mono	Quartz	0.005	Etalon
Toshiba	248nm	0.37	10	5 x 5	0.54	0.2 (3σ)	Achro	Q+CaF_2	0.4	-
Nikon	248nm	0.4	5	15 x 15	0.5	0.15 (3σ)	Mono	Quartz	-	-
Canon	248nm	0.35	5	5ϕ	0.57	-	Mono	Quartz	0.4	-
Mitsubishi	248nm	0.37	10	5 x 5	-	-	Achro	-	0.4	-
Sony	248nm	0.35	5	4 x 4	0.57	-	Mono	Quartz	0.002	-
Mitsui	248nm	0.3-0.4	-	21.2ϕ	0.5	-	Mono	Quartz	0.007	Etalon
NTT	248nm	0.42	5	10 x 10		-	Mono	-	0.007	-
Rutherford	248nm	0.3	1	60	0.5	-	Achro	Q+LiF	0.003	-

Source: IBM Corporation

Dataquest
a company of The Dun & Bradstreet Corporation

Research *Newsletter*

SEMS Code: 1987–1988 Newsletters: March 1988–6

A SAMPLING OF SUB–1.5–MICRON DEVICES

INTRODUCTION

For the past year and a half, the Semiconductor Equipment and Materials Service (SEMS) has been maintaining a log of public announcements of semiconductor devices that are fabricated with 1.5–micron or lower geometries. The log is not the result of an exhaustive literature search but, rather, a serendipitous recording of information when one happened across it. The intent of this newsletter is to present this sampling to our clients to indicate the range of sub–1.5–micron products presently on the market. The date at the end of each entry is the date on which the information was noted.

This month, SEMS is publishing "The North American Fab Data Base," which contains information on 400 semiconductor fabs. The information includes, for most of the fabs, the minimum line geometries being produced at each fab. In addition, SEMS recently published a newsletter, "U.S. IC Producers Heading Submicron" (SEMS Code: 1988–4), which analyzes wafer starts and capacity utilization by line geometry in the United States. This newsletter, together with these other two publications, provides good insight into sub–1.5–micron production in the United States today.

MICROPROCESSOR, MICROCONTROLLER, AND PERIPHERAL PRODUCTS

- Motorola will introduce its new line of reduced–instruction–set computer (RISC) microprocessors in the second quarter. The processor unit is a three–circuit set containing a primary processor and two cache memory management units (MMUs). The RISC set is manufactured in 1.5–micron HCMOS. (2/22/88)

- Trident Microsystems is sampling its first product, a video graphics array (VGA) fabricated in 1.5–micron CMOS under a foundry arrangement with Toshiba. (2/1/88)

- Hitachi will sample the Gmicro–200, a 32–bit microprocessor based on the TRON (the real operating nucleus) real–time operating system, in the second quarter, with production scheduled for the third quarter. It is designed with 1–micron CMOS design rules, with a double–metal process. It measures 14mm x 14mm and contains 730,000 transistors. (1/25/88)

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398 / (408) 437-8000 / Telex 171973 / Fax (408) 437-0292

- Advanced Micro Devices is sampling its 17-mips (millions of instructions per second), 32-bit RISC microprocessor. Called the Am29000, it is fabricated in 1.2-micron CMOS at the Austin, Texas, facility. (11/23/87)

- United Technologies has introduced an MMU, the UT1750, fabricated in 1.5-micron CMOS. (11/23/87)

- Motorola is designing a 1-micron successor to its 68HC11 controller. The new controller will be shipped in 1989. (11/23/87)

- National Semiconductor is sampling its new 32532 32-bit microprocessor. It is fabricated in 1.25-micron, double-metal, silicon-gate CMOS and has 370,000 transistors. (11/2/87)

- LSI Logic's affiliate, G-2 Inc., is shipping the GC201 graphics controller fabricated in 1.5-micron HCMOS design. (10/12/87)

- LSI Logic has qualified its two-device microprocessor set for 1750A military applications. The device set consists of the L64500 CPU and the L64550 MMU peripheral. They are fabricated in 1.5-micron HCMOS. (10/12/87)

- Mitsubishi will sample four models of a new 16-bit, single-chip microcontroller, as of December 1, 1987. The Melps family will be fabricated in 1.3-micron design rules. Chip size is 5.55mm x 7.50mm, and each chip contains 220,000 transistors. (10/5/87)

- LSI Logic's affiliate, G-2 Inc., will offer an AT-compatible chip set that runs at 16 MHz. The set consists of three devices: the GC101, which is a systems controller, peripheral controller, and memory controller; and two buffer devices, both called the GC102, which have address and data functions. The chip set is fabricated with a 1.5-micron HCMOS process. G-2 also plans a three-device, AT chip set that will run at 12.5 MHz and will be fabricated with the same 1.5-micron HCMOS process. (9/21/87)

- Texas Instruments will release a cache tag MMU designed for the 68030 microprocessor. The BICMOS device will use a 2.0-micron bipolar Impact process and a 1.5-micron CMOS process. (9/14/87)

- AT&T has unveiled a second-generation, floating-point digital signal processor. The new DSP32C will be fabricated in 0.9-micron, double-metal CMOS and will be available in the second quarter of 1988. (7/27/87)

- Motorola's new 68030 microprocessor will be fabricated in single-layer metal, with a silicide process. It will be done originally according to 1.3-micron design rules, with a shrink to 1.2 microns. (7/27/87)

- Fujitsu, Bipolar Integrated Technology, and Cypress are licensing Sun's SPARC microprocessor technology. Fujitsu's SPARC processor is using a 20,000-gate, 1.5-micron CMOS gate array. Cypress will implement the SPARC architecture in a CMOS chip set, using Cypress' 0.8-micron, double-metal CMOS process. (7/13/87)

- Texas Instruments is introducing a family of bus interface devices, the SN74BCT, which are its first circuits using a combined bipolar/CMOS process. The process combines TI's 2.0-micron Impact process with a 1.5-micron CMOS process. (6/22/87)

- Motorola expects to sample an LAPD controller. Designed primarily for ISDN applications, the MC68606 will be fabricated with a 1.5-micron HCMOS process. (6/1/87)

- Hewlett-Packard will build the Weitek 2264-65 floating-point chip set. HP will license the technology to fabricate the chip set in 1.2-micron CMOS at HP's Corvallis, Oregon, facility. Weitek maintains a foundry agreement with VLSI Technology, which produces the chip with a 1.5-micron process. (5/18/87)

- Advanced Micro Devices will produce an integrated data protocol for ISDN use. It will be fabricated with a 1.2-micron, double-metal CMOS process. (4/13/87)

- NEC will sample, next June, the V70 32-bit microprocessor fabricated in 1.5-micron CMOS and incorporating 385,000 transistors. (4/13/87)

- National's 32532 32-bit microprocessor is fabricated with a 1.5-micron, double-metal, silicon-gate CMOS process. It incorporates 370,000 transistors. (4/6/87)

- Fujitsu and Hitachi samples of the jointly developed 32-bit microprocessor for TRON will be available by the end of 1988 or early 1989. Fabricated in 1.3-micron CMOS with 700,000 transistors, it is called the F32-200 by Fujitsu and the H32-200 by Hitachi. Ultimately, a 1-micron process will be used. (4/6/87)

- Texas Instruments is developing a third-generation digital signal processor, the TMS320C30. It is fabricated with a 1-micron CMOS technology developed in TI's DRAM program. (3/30/87)

- Motorola will sample, in early 1988, an ISDN controller designed with a 1.2-micron, double-metal, HCMOS process used with its other ISDN devices. (3/16/87)

- Intel's 80386 microprocessor and 80387 floating-point units are fabricated with a 1.5-micron CMOS III process. (2/16/87)

- Analog Devices has introduced two sets of IEEE floating-point multipliers and arithmetic logic units. The ADSP-3211/ADSP-3201 and the ADSP-3221/ ADSP-3202 sets are fabricated in 1.5-micron design rules. Pin-compatible upgrades for the new parts, using 1-micron design rules, are slated for the first half of 1987. (1/12/87)

- AT&T is introducing its latest-generation 32-bit microprocessor, the WE 32200, fabricated in 1-micron CMOS. The 32200 has 230,000 transistors. AT&T also introduced the 32201 MMU, which has 400,000 transistors and is fabricated with the same 1-micron process. The 32206 math accumulator unit has 233,000 transistors. (12/8/86)

- Inmos is introducing a 20-MHz version of its Transputer T800 fabricated with a 1.5-micron CMOS process. (12/1/86)

- Performance Semiconductor's 1750 16-bit military microprocessor is fabricated in submicron technology to allow 200,000 transistors on a die that measures less than 0.25 inch on a side. (12/1/86)

- LSI Logic is introducing a series of DSP products drawn with 1.5-micron CMOS design rules. Products include a 32-bit floating-point unit and a multiplier accumulator. (11/24/86)

- LSI Logic is using 1.5-micron CMOS design rules on its L64500 16-bit microprocessor. (11/10/87)

- Weitek has designed a family of floating-point microprocessors. The Accel family, which consists of three CMOS processors, the 8000, 8032, and 8064, is fabricated with a 1.5-micron, N-well, double-metal CMOS process. (10/27/86)

- Hitachi has announced a 1.3-micron CMOS 32-bit microprocessor called the H32. Chip size is 10.4mm x 12mm. (10/13/86)

- Motorola's MC68030 is an enhanced version of the 68020 32-bit microprocessor. It will be fabricated in a 1.5-micron, single-layer metal HCMOS with a silicide process. Sampling will be in the second quarter of 1987. Die size will be 400 mils on a side, compared with 320 mils on a side for the 68020. When in production, Motorola will shrink the 68030 to 1.2-microns and 380 mils. (9/22/86)

- Motorola will introduce an enhanced floating-point coprocessor designed with a 1.5-micron HCMOS process and measuring 287 mils on a side. (9/22/86)

- Intersil has introduced a 16 x 16 CMOS multiplier accumulator designed with 1.5-micron geometries. (9/22/86)

- Motorola's new 25-MHz, 32-bit microprocessor, the MC68020, is fabricated in 1.5-micron HCMOS using a single-layer metal and polycide process. (7/28/86)

- WaferScale is sampling the WS59032D, a 20-MHz version of its 32-bit microprogrammable CMOS bit-slice processor. It is fabricated in 1.2-micron CMOS. (7/28/86)

- Hitachi will introduce, in 1987, a proprietary 32-bit microprocessor. It will be done with 1.3-micron design rules and will incorporate more than 300,000 transistors. (6/30/86)

- Intel announced its graphics coprocessor, the 82786, which is fabricated with a 1.5-micron CHMOS III process. (5/19/86)

- AT&T is planning on a third-generation, 32-bit microprocessor, the 20-MHz WE32200, which will be fabricated with 1-micron design rules. (5/19/86)

- Integrated Device Technology will introduce, this fall, two generations of floating-point chip sets, the 72064/65 and the 72265/65 sets, that will be fabricated with IDT's 1.2-micron process. (5/12/86)

MEMORY PRODUCTS

- National has introduced a 256K BICMOS SRAM, with ECL I/O, called the NM5100. The device is fabricated with the BICMOS III process, which is a 1-micron, 16-mask, twin-well, double-poly, double-metal process. It measures 213 x 386 mils, and will be fabricated at the Puyallup, Washington, bipolar facility. (2/22/88)

- Alliance Semiconductor is sampling a family of 64K CMOS SRAMs fabricated with a 1.2-micron technology. (2/1/88)

- Excel Microelectronics is shipping a 1.5-micron 64K CMOS reprogrammable PROM, called the XL46HC64 Speedprom. It is the first of a new line of memories from Excel. (2/1/88)

- IBM has donated its memory recipe for the 4Mb DRAM to Sematech. The chips are 0.5 inch x 0.25 inch and are fabricated with 0.7-micron design rules. AT&T's contribution to Sematech is a 64K SRAM fabricated with a 0.7-micron, double-metal CMOS technology. (2/1/88)

- Texas Instruments is shipping a 1Kx9 FIFO memory, the SN7ACT7202, fabricated with a 1-micron process. (12/21/87)

- NEC is sampling the uPD42601, a 1-micron CMOS silicon file. The device, which uses the same technology and has the same pinout as NEC's 1Mb DRAM, is designed to replace hard disks and to eliminate the need for a backup disk in personal computers and other computers. (12/14/87)

- Toshiba is sampling a 4Mb DRAM fabricated with a 0.9-micron, twin-tub, single-aluminum, triple-poly CMOS process with trenches. The die measures 111 square mils and will be shipped in a 400-mil DIP. In the first quarter of 1988, Toshiba will sample a version fabricated with a 0.8-micron process that will give a die size of 97.4 square mils for shipment in 350-mil SOJ packages. In the first quarter of 1989, it will sample a second-generation part fabricated in 0.7-micron CMOS for a die size of 81 square mils. The part will be packaged in a 300-mil DIP or SOJ and will be available in volume in the third quarter of 1989. (11/23/87)

- Texas Instruments will sample its 4Mb DRAM. The device will be fabricated at its Miho, Japan, facility, with a 1-micron, double-metal CMOS process utilizing trench capacitors for both the transistor and capacitor. (9/14/87)

- Intel has available a 35ns 64K SRAM, the M51C98, which is fabricated with Intel's 1-micron, double-poly CHMOS-IV process. (6/22/87)

- AMD/Sony's first products will be SRAMs fabricated with a 1.2-micron CMOS process. AMD currently has a 1.4-micron CMOS process for its 64K and 256K SRAMs. (6/1/87)

- Fujitsu has available a fast 64K SRAM (25 to 35ns), which is fabricated in a 1.3-micron, double-metal, double-poly, polycide gate CMOS process. (5/87)

- Hitachi has available a 12ns 64K ECL I/O SRAM, the HM10490CG-12, fabricated in 1.3-micron BICMOS. (4/20/87)

- Cypress Semiconductor is shipping a 16Kx8 reprogrammable power-switched PROM, the CY7C251, fabricated with a 1.2-micron, floating-gate, CMOS process. (4/13/87)

- Thomson Components-Mostek is offering the MK41H80, a 16K cache tag SRAM fabricated with a 1.2-micron, double-metal CMOS process. (3/2/87)

- VLSI Technology is offering a 1K SRAM, the VT7C122, with 1.5-micron design rules. (3/2/87)

- Oki's 1Mb DRAM is designed with a 1.2-micron CMOS process. (2/23/87)

- Motorola's fast 16K and 64K SRAMs are fabricated with a 1.5-micron, double-metal, double-poly CMOS process. (12/15/86)

- Intel will try to qualify for VHSIC parts. This requires that the 51C98 64K CMOS SRAM be shrunk to 1.1 microns. (11/10/86)

- VLSI Technology is producing 16K SRAMs with 1.5-micron design rules. SRAMs with 1.2-micron rules will be produced in 1987. (10/27/86)

- Cypress has introduced a CMOS EPROM, which is a version of Monolithic Memories' 22V10, called the PALC22V10. It will be manufactured under license from MMI with 1.2-micron design rules. (10/13/86)

- Fujitsu has developed a 16K ECL RAM with a 10ns access time, making it the fastest of its kind in the world. The product is designed with 1-micron rules and scheduled for mass production in January 1987. (10/86)

- Motorola will release its fast 256K SRAM that uses 1.2-micron design rules. (9/15/86)

- RCA is offering EPROMs with 1.2-micron design rules. (9/5/86)

- Toshiba's new UV EPROM is designed with 1.2-micron rules with a 200-angstrom gate oxide. The cell size is 50 square microns, compared with a 20-square-micron stacked design. (9/4/86)

- Saratoga Semiconductor's 16K and 64K ECL SRAMs and 64K TTL SRAMs are fabricated with 1.5-micron design rules. Saratoga will produce 256K devices with 1.2-micron rules within a year. (8/18/86)

- Integrated Device Technology has introduced two parallel I/O FIFOs with 35ns access times. The IDT7201 is a 512 x 9 FIFO, and the IDT7207 is a 1,024 x 9 FIFO. The parts are fabricated with a 1.2-micron CMOS process. (7/28/86)

- Performance Semiconductor is sampling a 64K SRAM, the P4C188, which is based on a submicron CMOS design. The device, which has speeds down to 20ns, is a six-transistor design that incorporates more than 400,000 transistors. Metal pitch is 2.75 microns, and the chip has an effective channel length of 0.8 micron. (5/26/86)

- Cypress Semiconductor's 4K 14ns CMOS SRAM, the CY7C150, is fabricated with a channel length of 0.8 micron. Its 25ns 4K SRAM is designed with 1.2-micron rules. (5/26/86)

ASIC AND LOGIC PRODUCTS

- Toshiba America has introduced a series of gate arrays using a 1.0-micron CMOS process that cuts gate delays by up to 35 percent. The TC120G Series, which offers typical gate delays of 400ps, has a range of 37,392 to 129,042 raw gates in a channel-less (sea-of-gates) architecture. The new series is compatible with Toshiba's channel-less TC110G Series, which is fabricated with a 1.5-micron CMOS process and offers gate delays of 600ps. The TC110G Series ranges in complexity from 3,400 to 129,042 raw gates. (2/26/88)

- Applied Micro Circuits and Plessey Semiconductor have signed an agreement to jointly develop a family of high-performance ECL gate arrays. The arrays will have up to 14,000 gates and will be produced initially at Plessey's Swindon, England, facility, using Plessey's new 1-micron, triple-metal HEI bipolar process. (2/22/88)

- National is taking designs for a nine-member 1.5-micron CMOS gate array family that has densities of up to 14,892 gates. The SCX6B00 family has effective channel lengths of 1.1 microns. National is also in the process of migrating its 2-micron standard cell library to a 1-micron process. (2/8/88)

- United Technologies Microelectronics Center has introduced its UTD-R family of radiation-hardened gate arrays with up to 11,000 equivalent NANDs. They are fabricated with a 1.5-micron CMOS process. Included are the UT1553 multiprotocol bus controller remote terminal, the UT1553B bus controller remote terminal interface, and the UT1553M version with monitor function. (1/18/88)

- Yamaha has obtained a license to manufacture and sell gate arrays based on Integrated Logic System's technology, which consists of a family of six 1.5-micron arrays ranging from 3,000 to 40,000 gates. Usable number of gates ranges from 1,500 to 20,000. (12/14/87)

- Motorola has introduced a series of 1-micron CMOS gate arrays fabricated in triple metal. The family consists of 10 parts ranging from 6,000 to 104,832 gates. (11/23/87)

- LSI Logic is offering a family of gate arrays, with 50,000 to 100,000 usable gates, fabricated with a 0.7-micron channel length with a 1.0-micron HCMOS process. The LCA100C has 236,880 total gates and has three layers of metal. (10/26/87)

- Mitsubishi Electronics America's semiconductor division has introduced two families of 1.3-micron CMOS gate arrays. The M6003X series has up to 47,000 gates, and the M6002X series has up to 2,400 gates. (10/19/87)

- Xilinix's XC2064 1,200-gate, programmable gate array and the XC2018 programmable gate array are both fabricated with a 1.2-micron process. (10/12/87)

- Raytheon is offering a family of VHSIC phase two-compatible gate arrays fabricated with a 1.25-micron CMOS process. The RAY1.25VG family consists of devices with 5,670 to 20,440 gates. (10/5/87)

- Fujitsu's AV series of CMOS gate arrays has densities of up to 8,000 gates, and densities of up to 12,000 gates are expected with 1.5-micron design rules. (8/31/87)

- LSI Logic has filled in its low-end, channel-free gate array (sea-of-gates) offering by introducing the LMA9000 Micro Array series and the LMb6000 Micro bASIC series gate array. Both series are fabricated with a 1.5-micron, double-metal HCMOS process. Densities range from 700 to 10,000 gates. LSI Logic introduced its channel-free architecture in 1985. (8/17/87)

- VLSI Technology is offering the VGT10 and VGT100 families of gate arrays fabricated, respectively, with 2-micron and 1-micron CMOS processes. The chips will be second-sourced by GE/RCA. (7/27/87)

- Fujitsu, Bipolar Integrated Technology, and Cypress are licensing Sun Microsystems' SPARC microprocessor technology. Fujitsu's SPARC processor will use a 20,000-gate, 1.5-micron CMOS gate array. Cypress will implement the SPARC architecture in a CMOS chip set using Cypress' 0.8-micron, double-metal CMOS process. (7/13/87)

- Texas Instruments has introduced its first bipolar gate array, an 8K ECL device using a 1.5-micron process derived from TI's Impact process. The TGE8000 gate array family will be fabricated in Houston, Texas. TI has also recently introduced a 1.2-micron CMOS gate array family. (7/6/87)

- Honeywell has produced working prototypes of a VHSIC implementation of the navy's AN UYS-2 standard signal processor. The three custom circuits included in the processor are a FIFO buffer, floating-point multiplier, and register arithmetic logic unit. Circuit complexities range from 17,500 to 32,000 equivalent gates fabricated with a 1.25-micron VHSIC bipolar process. Volume production is to take place at Honeywell's Colorado Springs, Colorado, facility. (6/29/87)

- Texas Instruments has introduced a family of bipolar PLA devices fabricated with a 1.5-micron Impact X process. The devices use trench isolation and have a 1.0-micron epitaxial layer. (6/29/87)

- Honeywell's Solid State Division will sell, under license from ETA Systems (a subsidiary of Control Data) a 20,000-gate array that was designed for the ETA-10 supercomputer. The device is fabricated with Honeywell's 1.25-micron CMOS VHSIC process. (5/25/87)

- Texas Instruments is beta-testing a series of quick-turn gate arrays fabricated with a 1.2-micron CMOS process. The TGC100 series has a range of 3,200 to 8,890 gates, and the TGC500 series has from 3,000 to 16,000 gates. The devices are the initial entries in a planned 1-micron CMOS gate array and standard cell library designed for TI's EPIC process. (5/11/87)

- Fujitsu has introduced a library of gate arrays, the UHB series, which has versions available with up to 12,734 gates. The devices are fabricated with a 1.5-micron, double-metal CMOS process. (3/9/87)

- Thomson Components–Mostek has had available, since 1986, 1.2–micron gate arrays with up to 10,000 gates and expects first silicon this month on a 20,000 sea–of–gates array with up to 57,000 usable gates. The sea–of–gates device will be fabricated with an HCMOS III process. (3/9/87)

- Texas Instruments will introduce 1–micron gate arrays and standard cells to be fabricated with TI's proprietary EPIC CMOS process at the Dallas, Texas, and Miho, Japan, facilities. TI will also introduce a new 1–micron bipolar ECL gate array library with up to 10,000 gates. The library will be fabricated with TI's latest bipolar technology, called TIPSA. (2/16/87)

- Toshiba is offering the TC19G channeled gate array family that has from 3,200 to 10,000 gates and the TC110G sea–of–gates family that has from 2,100 to 50,000 gates. Both families are fabricated with a 1.5–micron, double–metal CMOS process. (1/19/87)

- Plessey has developed a family of ECL gate arrays. The initial set consists of three arrays with 1,000, 2,900, and 4,500 gates. They are fabricated with a 1.5–micron bipolar process using three levels of metal. (1/12/87)

- Thomson Components–Mostek has converted its 2– and 3–micron gate array libraries to a 1.2–micron series called the TSGC. The TSGC series will be available in densities from 1,000 to 10,000 gates. (12/8/86)

- National will second–source Chips & Technologies devices at its Arlington, Texas, facility. Semicustom parts will be done with a 2–micron process, while full–custom parts will be done with a 1.5–micron process. The agreement calls for production of current and future logic lines, using National's gate array, standard cell, and custom tools. (11/3/86)

- VLSI Technology has introduced the VGT100 series of 1.5–micron CMOS gate arrays. The series has a range of 12,000 raw gates (9,000 usable) to 67,000 raw gates (50,000 usable). (10/13/86)

- Intel will offer 1.5–micron, double–metal CMOS gate arrays, originally developed by IBM. Intel also has had available cell–based designs fabricated with a 1.5–micron, single–metal CMOS process; this cell–based library has been enhanced with a 1.5–micron, double–metal process. (10/6/86)

- Texas Instruments will introduce a 1–micron CMOS gate array family in the first half of 1987, and will also introduce in 1987 a 1–micron standard cell line. Until now, TI has second–sourced 2– and 3–micron designs from Fujitsu at its Miho, Japan, facility. (9/22/86)

- RCA's standard cells are fabricated with a 1.2–micron channel length CMOS process. (9/5/86)

- VLSI Technology (VTC) is offering a 1–micron standard cell library, VL5000, that has 20,000 equivalent gate complexity. The devices are fabricated with VTC's double–metal CMOS II process. (9/4/86)

- Plessey is planning a 1–micron CMOS MEGACELL with up to 100,000 gates. (9/1/86)

- General Electric is making 1.25-micron CMOS custom ICs at its Research Triangle Park, North Carolina, facility. (8/15/96)

- General Electric, Siemens, and Toshiba will have a 1.5-micron CMOS ASIC process. The 1.5-micron cell libraries are scheduled for late 1986, while the 1.2-micron process is scheduled for 1987 or 1988. (8/11/86)

- United Technologies Microelectronics Center has introduced a 1.5-micron CMOS gate array family with 11,000 usable gates. The family is aimed at the military and aerospace markets. (8/11/86)

- NEC has a 1.5-micron CMOS standard cell family that includes 130 mega-cells. Densities of up to 17,000 gates can be achieved. (7/86)

- Hitachi will produce Fairchild's FACT logic line with a 1.3-micron, double-metal, P-well CMOS process. (7/7/86)

- RCA's Advanced CMOS Logic (ACL) parts are fabricated with a 1.5-micron channel length and an N-well process. (7/14/86)

- Thomson Components-Mostek is producing 2- and 3-micron, double-metal HCMOS gate arrays and standard cells with densities of up to 4,000 gates with the 3-micron process and up to 10,000 gates with the 2-micron process. The company is migrating these parts to a 1.2-micron process. (6/30/86)

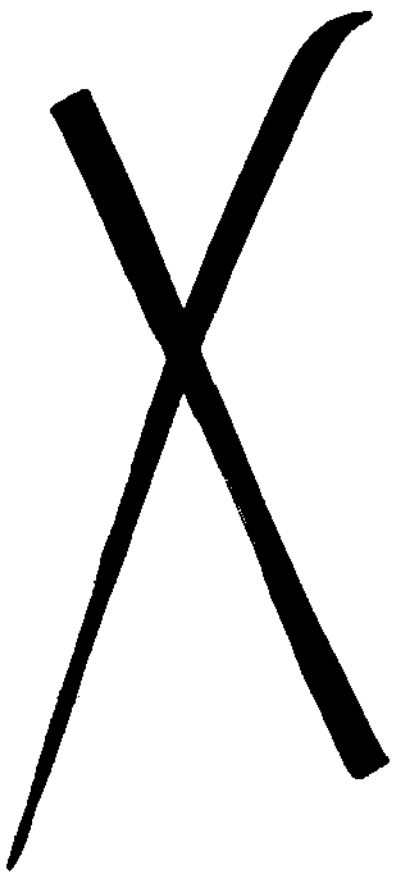
DISCRETE PRODUCTS

- Motorola has introduced a series of three low-noise NPN bipolar small-signal transistors, the MRF951 series. The parts are fabricated with 1.2-micron design rules, with silicon nitride passivation and gold metallization. Average selling price is $1.30. (2/22/88)

LINEAR PRODUCTS

- Datel has available the ADC-207 7-bit flash converter fabricated with General Electric's 1.2-micron AVLSI process. (9/29/86)

Joseph Grenier



April Newsletters

The following is a list of newsletters found in this section:

- Emerging Superconductor Applications:
  Visions and Market Realities
  1988 - #12

- 1988 IEEE Solid-State Circuits Council:
  From Density to Performance
  1988 - #10

Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987–1988 Newsletters: April 1988–12

EMERGING SUPERCONDUCTOR APPLICATIONS: VISIONS AND MARKET REALITIES

INTRODUCTION

Since IBM Zurich's discovery of high–temperature (Tc) superconductors in 1986, scientists and the media have hyped the prospects of superconductivity. New fuel has been added by Japan's recent breakthrough in bismuth–strontium ceramic oxides and its new national R&D projects. Although much work remains to be done, Dataquest believes that we will see superconductivity used in the following electronic applications by the early 1990s:

- Superconducting quantum interference devices (SQUID) in magnetic field detection equipment and magnetic sensors
- Infrared detectors and sensors for military and aerospace systems
- Electromagnetic interference (EMI) shielding for data security in military and industrial computer systems
- Magnetic separation machines for producing superconducting R&D materials
- High magnetic–field instrumentation and testing machines for research
- Prototype high–speed analog/digital converters, digital signal processors (DSPs), and CMOS/superconductor hybrid circuits using miniature cryogenic packages
- Prototype interconnection for workstations and mainframes
- Small prototype batteries for military and industrial data storage systems

Our forecast is based on presentations made at the recent International Superconductor Applications Conference in Los Angeles, where leading scientists announced key breakthroughs and outlined emerging applications. These presentations are summarized in this newsletter.

Although prospects look bright, we see formidable technical and nontechnical barriers facing superconductivity. Thus far, attention has focused primarily on technical breakthroughs, while little discussion has been given to the critical issues of patent rights, useful applications, product design, manufacturability, marketing, and distribution. To address these key issues, Dataquest is introducing an Emerging Semiconductor Technology Service this year.

EMERGING SEMICONDUCTOR APPLICATIONS—A JAPANESE VIEW

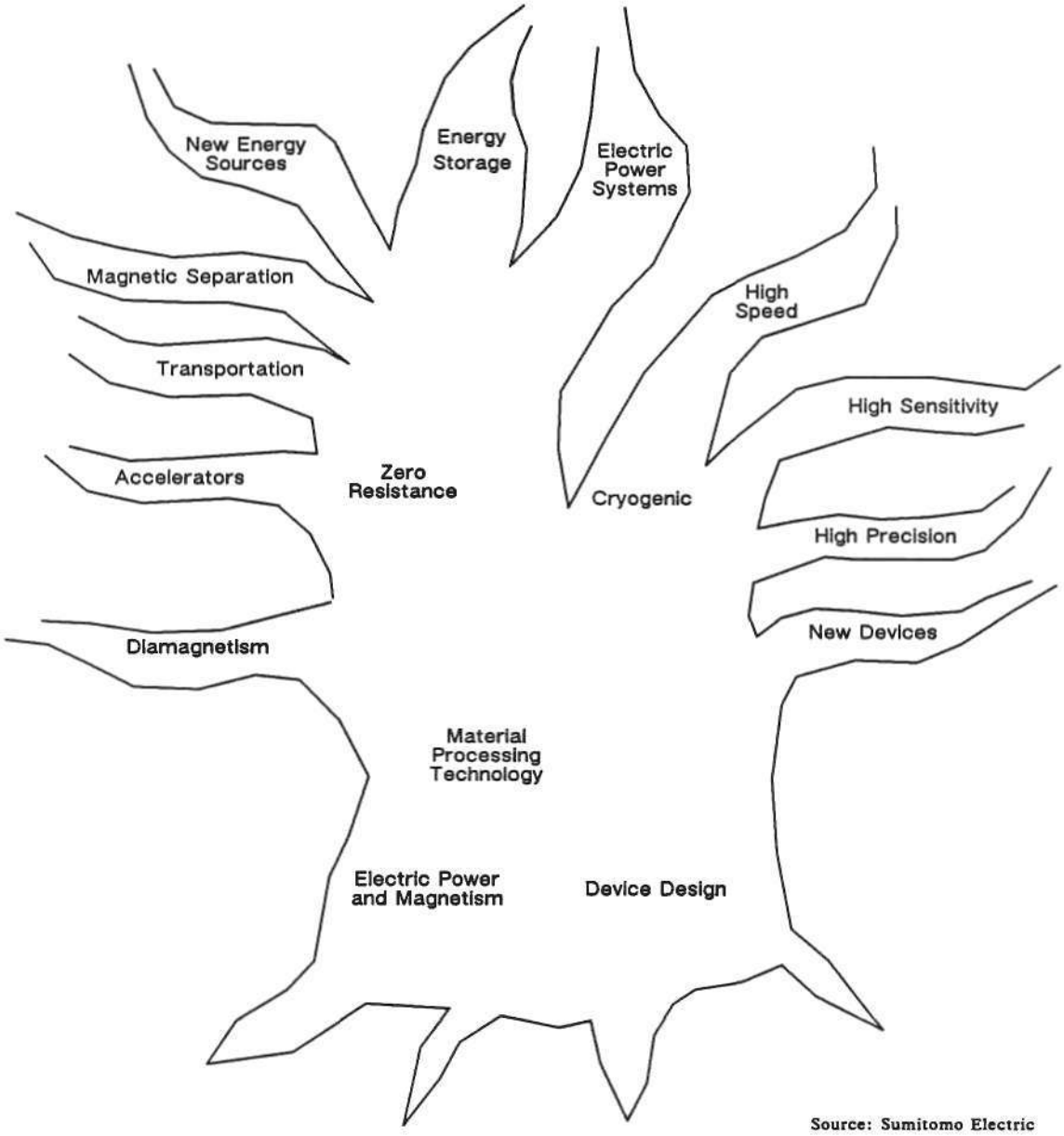
The National Bureau of Standards (NBS) exhibited a superconductor "technology tree" developed by Sumitomo Electric, which recently filed more than 200 patents in the field. As shown in Figure 1, Sumitomo envisions the following applications:

- Diamagnetism—magnetic shielding, actuators, and bearings
- New devices—superconducting transistors, Josephson junctions, and SQUIDs
- High precision—voltage standards and fundamental physical measurements
- High sensitivity—SQUID machines (heart and brain flux meters and geomagnetism), low-noise microwave devices, infrared sensors, and radiation sensors
- High speed—computers, analog/digital converters, wide-range signal treatment
- Energy storage—pulsed power supply and load-leveling
- Electric power systems—transmission cables and generators
- New energy sources—plasma confinement for nuclear fusion and power generation
- High magnetic-field instruments—magnetic resonance image (MRI) machines and electron microscopes
- Magnetic separation—ore separation, coal desulfurization, waste processing, and pollution countermeasures
- Transportation—magnetic levitation trains and magnetically propelled ships
- Accelerators—superconducting supercolliders, linear accelerators, and accelerators for medical applications

Sumitomo Electric has dedicated a large staff of researchers to explore these various applications. However, we believe that most of these applications will not take off for at least 10 to 15 years. JSIS will provide more information on electronics applications in our upcoming special report on Japanese superconductor research activities.

Figure 1

Emerging Superconductor Applications



Source: Sumitomo Electric

JAPANESE BREAKTHROUGH IN NEW BISMUTH OXIDES

On January 22, the National Research Institute of Metals (NRIM) in Tsukuba reported a new ceramic oxide that becomes superconducting at minus 243 degrees Celsius, about 50 degrees warmer than Paul Chu's discovery last February at the University of Houston. The new oxide consists of bismuth, strontium, calcium, copper, and oxygen (BiSrCaCuO). U.S. and European laboratories have confirmed the discovery.

Professor Shoji Tanaka of Tokyo University explained that the new bismuth material has a lower melting point (890 degrees Celsius for undoped material and 740 to 860 degrees for doped material versus 900 degrees for yttrium–lanthanum compounds), making energy requirements lower for manufacturing. The material, which is very stable, has low resistance at 120K and zero resistance at 95K. Moreover, about 50 to 80 percent of the sample material showed the Meissner (levitation) effect, indicating superconductivity. Professor Tanaka expects to see new bismuth–based superconductor breakthroughs at least once a year, although Arthur W. Sleight of DuPont is not optimistic about these materials because they are highly anisotropic (different orientations in different planes) like mica.

Robert J. Cava of AT&T Bell Laboratories explained that the new bismuth–strontium material was discovered after Tokyo University researchers noticed a new trend emerging: Faster progress was being made with barium, bismuth, and strontium oxides than intermetallic (niobiumtin) or the newer yttrium–lanthanum–copper oxides. His advice to the audience: "Watch the trend lines." Bell Labs observes that bismuth is an unusual material that forms superconducting arrays in sheets, which still has scientists puzzled. Bismuth–based superconductors have a relatively high critical temperature of 85K to 110K, so understanding this array structure is crucial for achieving higher temperatures.

U.S. SUPERCONDUCTOR TECHNOLOGY TRANSFER EFFORTS

Since President Reagan's speech on superconductors last year, U.S. national laboratories have organized technology transfer programs to expedite the flow of basic superconductor research to U.S. companies. The NBS provided an overview of superconductor research at leading U.S. federal laboratories:

- Ames—a high Tc update newsletter, rare earth separation and purification, metals development and fabrication, and wire fabrication
- Argonne—basic property studies, ceramic processing, and conductor development
- Brookhaven—neutron scattering, synchrotron light source; multifilamentary conductor fabrication; and power transmission test facility
- Fermi—magnetic applications
- Idaho National Engineering Laboratory—high Tc coatings on metal, and military applications
- Lawrence–Berkeley—thin–film processing, fabrication, devices, synthesis, and characterization

- Lawrence–Livermore—theory and demand studies, materials preparation (powders, sputtering), and physical measurements

- Los Alamos—basic research, bulk and thin–film synthesis shielding, applications for Department of Defense, Department of Energy, and industry

- Oak Ridge—single crystal synthesis and ceramic processing, thin–film preparation of single crystal films, high–current conductors, and characterization and analysis

- Pacific Northwest—synthesis of monolithics, films, and fibers; materials desirability studies; and utility transmission and distribution applications

- Sandia—synthesis of thin films and bulk processing, device development (passive, active, infrared electrical devices), and funding studies

For more information, contact:

- Eugene Stark, Chairman, Federal Laboratory Consortium
  Phone: (505) 667–1234
  Karl Stauhammer, Shock Consolidation
  Phone: (505) 667–2067
  Los Alamos National Laboratory MS H–811
  Los Alamos, NM 87545

- Gregory Besio, Director
  Superconductivity Applications Information Office
  Argonne National Laboratory, Building 207/TTC
  9700 S. Cass Avenue
  Argonne, IL 60439
  Phone: (312) 972–7928

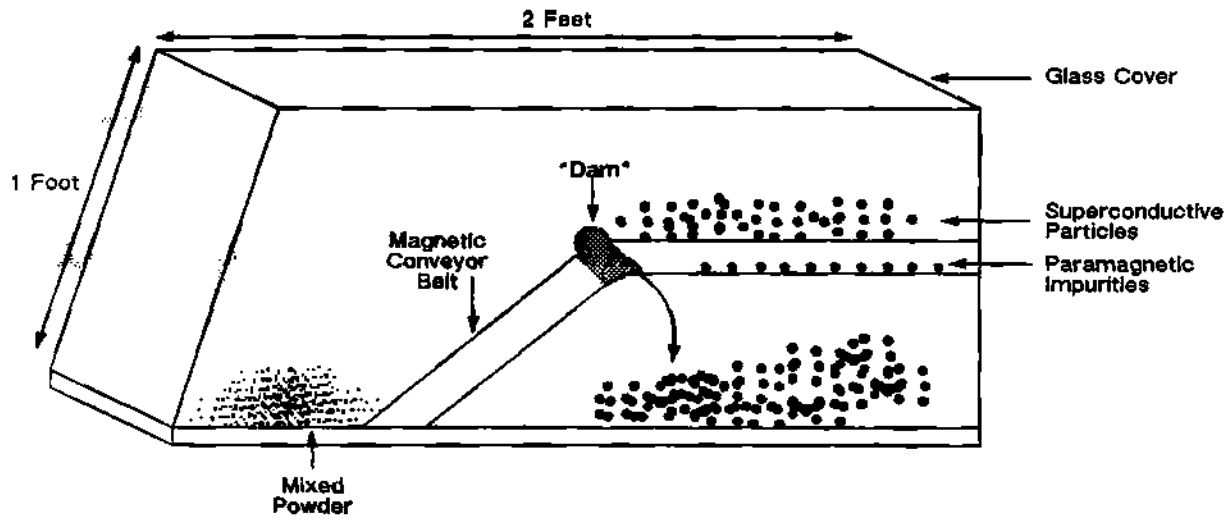
- Mark Alper, Assistant Division Head
  Center for Thin Film Applications
  Lawrence Berkeley Laboratory/Materials
  and Chemical Sciences Division
  1 Cyclotron Road, Bldg. 62, Room 203
  Berkeley, CA 94720
  Phone: (415) 486–6062

REFINING SUPERCONDUCTOR POWDERS

Richard E. Stephens, senior staff scientist at General Atomics, described a new method for separating superconducting oxide powders from normal grains. As shown in Figure 2, powder mixtures are conveyed up a tilted surface by a rotating magnet behind the surface. Superconducting particles are carried to the upper compartment, while normal grains fall to the trough and paramagnetic impurities are eliminated by a small "dam." Using this technique, very pure superconducting powders can be produced. This continuous magnetic separation technique can be used for volume powder separation and enhancement. In the future, large–scale machines, parallel machines, and magnetic screens could be developed for manufacturing lines.

Figure 2

General Atomics' Superconducting Powder Separation Machine



Source: General Atomics

A NEW CERAMIC MELTING PROCESS

Mr. Cava of Bell Labs explained that high Tc superconductors (more than 90K) require ceramic materials that are stable, easy to prepare, stress–resistant, and capable of being made into wires. The weakness of ceramics is their poor superconductivity at the boundaries between the ceramic grains due to holes and loops. To solve this problem, Bell Labs is developing a melting process that produces polycrystalline bulk with better grain quality (thus better superconductivity) than traditional sintering processes.

PRODUCING SUPERCONDUCTORS BY CONTROLLED EXPLOSIONS

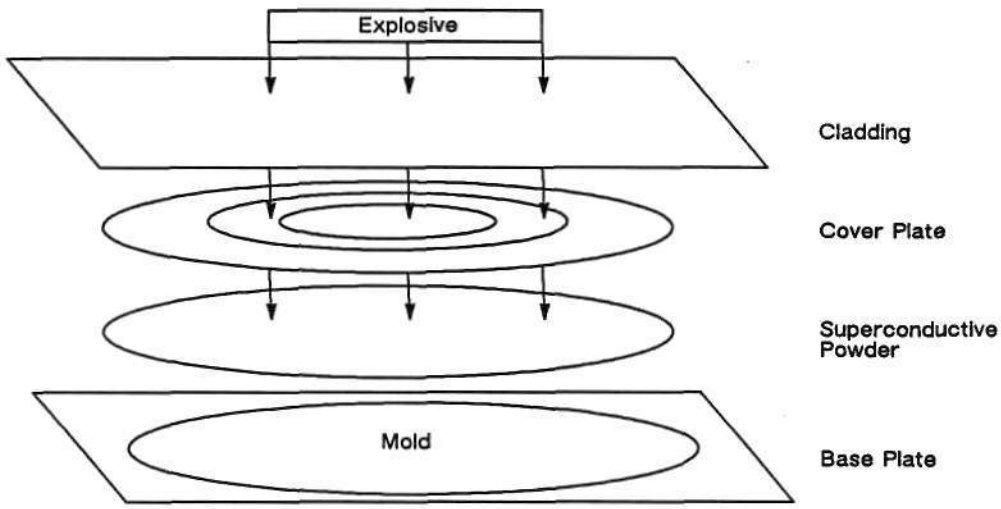
Lawrence E. Murr, cofounder of Monolithic Superconductors, described a new technique that employs controlled explosions to produce monolithic superconductor materials, which can be machined, milled, drilled, or polished into products. As shown in Figure 3, a detonation compresses the superconductive powder into a mold pattern designed on a base plate. The superconductive powder can be mixed in different proportions with other materials, not just ceramics. Using this method, superconducting circuits can be pressed into solid bars for electrical transmission or electronic circuitry, as shown in Figure 4. Potential niche markets include:

- "Bus bars" (interconnection) between simple systems on printed circuit boards
- Switching devices (e.g., Josephson junctions)

- Lightweight, high-density storage rings for airborne power systems, satellites, and transportation systems
- Solar-powered batteries for laptop computers and consumer products (replacement for lithium batteries)

Figure 3

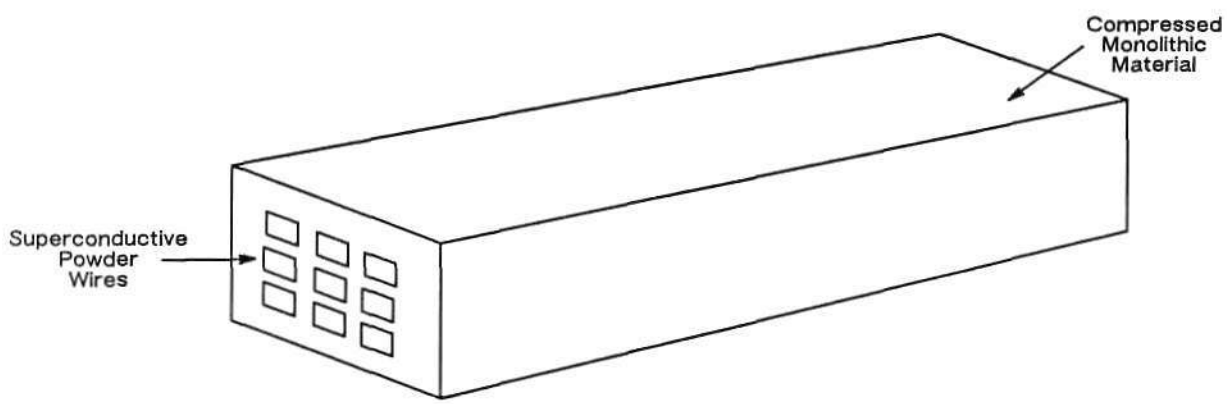
Monolithic Superconductors' Controlled Explosion Method



Source: Monolithic Superconductors
Dataquest
April 1988

Figure 4

Monolithic Superconductors' Superconducting Transmission Liner



Source: Monolithic Superconductors
Dataquest
April 1988

ELECTROMAGNETIC SHIELDING FOR ELECTRONIC EQUIPMENT

Jack Reilly of Electro-Kinetic Systems described the growing need for electromagnetic shielding in computer systems because of stricter government regulations, more sensitive components, and concern over data security. EMI can be reduced by using low-pass filters (for conducted EMI) and changes in electronic design, mechanical design, and metallized cabinets (for radiated EMI). Many shielding methods can be used: conductive coatings, wire sprays, vacuum meters, ion plating, electroless plating, and conductive composites.

Mr. Reilly observes that current shielding methods are inadequate if EMI is increased by 10 to 20 decibels. Electro-Kinetic Systems is developing superconductive composites in plastic coatings that offer more efficient shielding. Potential applications include:

- Superconducting surfaces—potential use in PCB interconnection and computer cabinet shielding
- Hyperconductive plastics—simple doping by halogens offers greater stability than copper; possible synergy with superconductors

As shown in Table 1, superconductive coatings are only one application. Superconductive molded parts, gaskets, and adhesives can also be developed for electronic systems in a variety of areas. Mr. Reilly observes a growing industry trend toward more source shielding and gasketing to reduce EMI. Dataquest believes that, as government and industry concern over EMI increase, we will see commercial use of superconductive parts.

Table 1

Potential Superconductive Components in Electronic Systems to Reduce EMI

Application	Coatings	Molded Parts	Gaskets	Adhesives
Large Shielding	X		X	X
Photomagnetic		X	X	X
Secure Communications	X	X	X	X
Electromagnetic Pipes	X		X	
Millimeter Waves	X	X	X	

Source: Electro-Kinetic Systems
Dataquest
April 1988

SUPERCONDUCTING DEVICE OPPORTUNITIES

Theodore Van Duzer, professor in the Electrical Engineering and Computer Science Department at the University of California/Berkeley, described several prototype superconducting devices:

- A flash-type analog-to-digital converter
- A quasi-one-junction SQUID with a 20-GHz sampling and 4MHz-sine wave capability
- A fully parallel A/D converter with 15 to 16 comparators
- A one-junction SQUID with a 5-GHz analog bandwidth for 4-bit processing
- A multiple-input SQUID

During the question-and-answer session, Professor Van Duzer explained that UC Berkeley uses niobium for the ground plane and liquid helium coolants, like IBM. He believes that 50-GHz sampling capability will be needed for faster circuits. Moreover, he believes that superconductors may be effective for portable signal processors, but not mainframes.

SUPERCONDUCTOR PACKAGING TRENDS

Dr. Dudley Chance of IBM's Watson Research Center explained potential uses of high Tc superconductors in computer packaging. Although copper is easier to use, superconducting multilayer interconnection would allow higher chip densities and lower power consumption. However, there are significant materials and process challenges, including:

- High processing-temperature requirements
- Thermal expansion of the superconductor material
- Reaction with other oxides
- Grain boundary layers (which reduce conductivity)
- Anisotropy (different plane orientations of the materials)

IBM sintered a 94 percent dense yttrium-barium-copper-oxide (YBaCuO) material and encountered cracking, uneven granular composition (intergranular phases) and distortions (twinning patterns). Dr. Chance recommends testing superconductive packaging performance with CMOS devices before using Josephson junctions.

A MINIATURE SUPERCONDUCTOR REFRIGERATOR

William A. Little, professor at Stanford University and founder of MMR Technology, described an integrated cryogenic chip package for superconducting devices using micro-miniature refrigerators. MMR Technology employs the Joule-Thomson refrigeration method, which was developed more than 100 years ago, to cool high-pressure gases to low temperatures (30K). The refrigerator is scaled down to chip size (1.0cm x 0.5cm) and covered by a bonded glass plate. Currently, the process involves five steps: glass and photoresist, sandblasting, etching, sawing, and packaging. MMR uses a step-and-repeat process to manufacture 0.4-inch-diameter refrigerators that are diced and bonded. Professor Little explained that photolithography can be used to develop a variety of chip-size refrigerators for superconducting devices. MMR's miniature refrigerators can be cooled down to 80K in 1.5 to 15.0 seconds using a hydrocarbon-nitrogen gas mixture. Potential uses include:

- Miniature refrigerators for telescopes and microscopes
- Built-in refrigerators for IC wafer probes
- Cryogenic chip carriers

MMR Technology has introduced a cryogenic chip carrier called Cryopack (Model 0288) that allows CMOS and superconductor devices to be integrated onto the same chip. Using this coolant, the operation speed of an 80386 would be two to five times faster. The 2 x 1/2-inch cryogenic package can be plugged into a printed circuit board and hooked up to a gas line. Nitrogen gas costs run about $0.50 per hour. Dataquest believes that this coolant could be useful for high-performance ECL, CMOS, and GaAs circuits since very small refrigerators could be developed.

MAKING SUPERCONDUCTING WIRES

Dr. George W. McKinney III discussed the efforts of his start-up company, American Superconductor, to develop superconducting wire. Currently, there are four wire manufacturing methods:

- Ceramics—redrawn tubing or coated filamentary wire
- Bulk forming—monolithic materials compressed using controlled explosions (e.g., Monolithic Superconductors)
- Thick films—superconducting material layered onto substrates or printed circuit boards
- Metal precursors—1-2-3 superconductive compounds and composites

American Superconductor is using the metal precursor approach developed by Massachusetts Institute of Technology in 1987, which involves melting yttrium, barium, and copper into a wire, then oxidizing and annealing the ceramic material. To date, the company has superconductor samples that are large, dense (99 percent), and strong. The advantages of these precursors are threefold:

- Good manufacturability in a metal state
- Direct synthesis of dense, homogeneous oxides
- Direct synthesis of microcomposites (flexible with silver added)

American Superconductor has received $4.5 million in venture capital to fund research on new alloy compositions and determine optimum processing conditions. The company plans to produce limited samples by mid-1988 and a demonstration unit by 1992.

SUPERCONDUCTIVE RESEARCH INSTRUMENTS

Barry Lindgren, president of Quantum Design in San Diego, discussed his company's success in selling superconductive instruments for research purposes. Established in 1981, Quantum's sales leapt from $360,000 in 1984 to $1.3 million in 1986, and the company anticipates $4.0 million in revenue in 1988. Quantum sells four types of instruments:

- Magnetic field detectors (passive)—for low-frequency geophysical exploration, magnetic anomaly detection, corrosion processes (with MIT), and biomagnetism (potentially a big market)
- Sample magnetometry—for rock magnetometers, magnetic resonance imaging (more than 1,000 units sold), low-frequency nuclear magnetic resonance, AC susceptibility research, and susceptometers (in the future)
- Particle detectors—for monopoles and gravity wave research
- Superconducting electronics—thin films for devices and interconnection

Quantum's magnetometer (Magnetic Property Measurement System), which measures differences in temperature and current fields, integrates a SQUID and temperature controls. Sales surged in 1987 because of the sudden increase in superconductor research, especially in the United States (31 units) and Japan (26 units). Its first unit was purchased by Ames Laboratory to measure thin-film deposition.

TWO VENTURE CAPITALIST VIEWS OF SUPERCONDUCTIVITY

Dr. McKinney, general partner of American Research and Development (in addition to his responsibilities at American Superconductor), explained that advanced materials require high investment costs ($75 million to $100 million) and long market-penetration cycles for design-in and field testing. He emphasized that start-ups must seek novel,

high–leverage applications, where superconductors are only a small part of the total solution. American Research and Development has invested in two superconductor start–up companies, as follows:

- Ceramics Process Systems, which raised $2.5 million from MIT, Paine–Webber, and Venture Founders in 1984, is headed by MIT professors and Kent Bowen and Eric Berringer. The company is emphasizing long–term development and cross–training of its polymers and ceramics researchers. The company has a pilot plant and raised $40 million in 1987 for a new production facility.

- American Superconductor, which raised $4.5 million to produce high Tc wires and cables, has six researchers (all Ph.D.s) and four professors on its advisory board.

John Shoch, president of Conductus, Inc., a superconducting thin–film start–up, emphasized that venture capitalists must develop a new investment style to leverage this high–risk/high–reward technology. Patience will be required because of the expected length of the development cycle. Start–ups need to focus on four goals: a patented proprietary technology, a clearly identified market, high prices, and a complete management team. There are two realistic start–up models:

- Hypres, which went against conventional thinking by narrowing IBM's broad focus, provides oscilloscopes that meet market needs because they are movable and fit through doors.

- Conductus, which is focusing on new breakthroughs with wide potential applications in emerging systems, not existing systems, raised $6 million in 15 minutes without a business plan because the principals have worked with superconductors for many years.

During the discussion, Mr. Shoch mentioned several market opportunities: bulk applications (substrates, wires, and cables) and electronic applications (interconnection, high–speed digital and analog devices, sensors, and detectors). Both gentlemen emphasized the importance of owning patent rights. However, they believe that, unlike ICs, fundamental patent monopolies are unlikely. Mr. Shoch believes that there are market opportunities in three areas:

- New materials breakthroughs—process–driven

- New user demands (e.g., data security)—product–driven

- New applications for existing superconductor technologies

Despite the optimism, Dataquest believes that superconductivity will test the long–term commitment of U.S. venture capitalists. Unless early start–ups are able to market samples quickly, venture capital interest will subside. Nevertheless, we believe that many market opportunities exist for companies with long–term staying power (more than five years).

DATAQUEST ANALYSIS

The first International Superconductor Applications Conference offered a respite from the technical superconductor conferences being held worldwide. Although Dataquest believes that widespread superconductor applications will not emerge until the late 1990s, we expect sample production of magnetic sensors and detectors, magnetic field detection equipment, and testing equipment within several years. Prototype A/D converters, hybrid CMOS/superconductor chips, and interconnection will be introduced about the same time. Dataquest understands that superconductivity is a much richer phenomenon than transistors; physicists mention more than 40 physical properties, such as thermal gradients, zero resistance, and antimagnetic properties. Each property promises a variety of new applications.

To be prepared, we recommend that companies implement the following policies:

- Attendance at major new materials and superconductor conferences in Europe, Japan, and the United States
- A few dedicated superconductor researchers to identify potential applications that would leverage corporate strengths
- Participation in technology transfer programs at national laboratories and universities
- Creation of semiautonomous superconductor start-up companies jointly financed with venture capital to test market potential products related to the company's main product lines

Over the next 20 years, Dataquest believes that superconductivity will have a major impact on existing electronics technologies because of its strategic importance as a new materials industry. Governments in Japan, Europe, and North America realize the importance of this technology and have established a variety of national R&D projects. Although superconductor markets will not take off, at earliest, until the mid-1990s, we believe waiting for the market is a sure recipe for disaster. Companies must plan now to take advantage of this emerging technology.

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Peggy Wood
Sheridan Tatsuno

Dataquest
A company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987–1988 Newsletters: April
1988–10

1988 IEEE SOLID–STATE CIRCUITS COUNCIL: FROM DENSITY TO PERFORMANCE

The Institute of Electrical and Electronic Engineers (IEEE) sponsored the IEEE Solid–State Circuits Council (ISSCC) at the San Francisco Hilton Hotel from February 17 through February 19. This newsletter analyzes that conference with respect to new trends that may emerge in future fabrication of semiconductor devices.

SEMS newsletter number 1987–4 entitled "1987 IEEE Solid–State Circuits Council: New Technology Perspective," on ISSCC 1987 concentrated on the DRAM papers and their implications. This year, we find that the future of manufacturing can be found only by looking at the broad spectrum of devices and technologies presented.

PRESENTATION OF PAPERS

This year, 97 papers were presented at the conference as opposed to 116 papers last year. Our initial analysis of these papers is by regional and technical distributions.

Regional Distribution

Table 1 gives the segmentation of the papers by the region in which the research was done. For instance, IBM/Corbeil is listed as being European. Each region is segmented by company or organizational type (i.e., merchant, captive, or institution).

Table 1 shows that 54 percent of the papers were from North America. Last year's figure was 43 percent. Japan presented 33 percent of the papers, falling from 44 percent, while Europe presented 14 percent, increasing from 13 percent. The split by type of company remained relatively constant. We believe that the change in percentages does not reflect a shift in R&D activity, since only one more paper was presented by North American companies this year than last year. We believe that the sharp decrease in the number of Japanese papers, from 51 in 1987 to 32 in 1988, reflects the whirlwind shift in worldwide economic conditions since last year.

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398 / (408) 437-8000 / Telex 171973 / Fax (408) 437-0292

Table 1

Papers by Company Type Segmentation (By Numbers and Percentage)

Region	Merchant		Captive		Institution		Total
North America	23	46%	17	33%	11	21%	51
Japan	27	84	2	6	3	10	32
Europe	12	86	0	0	2	14	14
Total	62	65%	19	20%	16	15%	97

Source: ISSCC

Product Group

The breakdown of papers according to device segment is represented in Table 2. The table breaks down each region's papers into five major device types. The memory category was the largest single segment, comprising 26 percent of the papers. The "other" category consisted of several types, including processors, logic, GaAs, and sense amps.

Table 2

Papers by Product Type Segmentation (By Numbers and Percentage)

Region	Memory		Microprocessor		Custom		Analog		Other	
North America	12	48%	5	83%	2	40%	6	43%	26	55%
Japan	11	44	1	17	2	40	4	29	14	30
Europe	2	8	0	0	1	20	4	29	7	15
Total	25	100%	6	100%	5	100%	14	100%	47	100%

Source: ISSCC

Referring to Table 2, the memory segment represented 26 percent of the papers this year compared with 25 percent last year. In light of the lower Japanese representation, this shows that North American companies have stepped up their activities in memories. Presentations by North American companies constituted 24 percent by category as opposed to 14 percent last year.

The largest change from last year was in the microprocessor segment. Last year, this category represented 15 percent of the papers, while this year it was at 6 percent. The lack of Japanese papers in this segment, one compared to six last year, seems to suggest that the Japanese (and the Europeans) have relinquished this area to the Americans. We find this hard to believe.

Technology Group

Table 3 shows the segmentation according to technology. This table reflects and corroborates the consensus that CMOS technology is taking over the IC business.

Table 3

Segmentation by Technology
(Number of Papers)

Region	CMOS	BICMOS	Bipolar	GaAs	Other
North America	36	3	4	3	6
Japan	19	3	4	1	4
Europe	11	0	0	0	3
Total	66	6	8	4	13

Source: ISSCC

Referring to Table 3, 68 percent of the papers were in the CMOS category, 6 percent in BICMOS, 8 percent in bipolar, 4 percent in gallium arsenide, and 13 percent in other technologies (such as HEMT, Josephson junctions, etc.). The high percentage of CMOS activity seems to indicate an overwhelming confidence that clever designers, manufacturers, and equipment and materials vendors will make it possible to push this technology toward unimaginable performance.

Even as our industry pursues this goal, the boundaries between the technologies blur. BICMOS devices now hold the promise of low power and even higher performance, with the added advantage of versatility in their ability to interface. Last year, there were four BICMOS papers, three from Japanese companies and one from North America. This year, six papers were presented, three from North America and three from Japan.

TECHNOLOGY ANALYSIS

Last year's newsletter concentrated on memories and the implications on how readily they could be manufactured; this year we will look more generally at all of the product areas. The momentum of decreasing densities has been suspended as the industry waits for the rest of the devices to catch up with memories. We found that emphasis was on device performance and speed at this year's conference.

DRAM Analysis

Table 4 gives the specifications for this year's DRAM papers. We have excluded the paper from IBM entitled "An 11ns, 8Kx18 CMOS Static RAM" since it is a static RAM.

Table 4

DRAM Specifications

Company	Device	Epitaxy	Geometry (Microns)	Area Mils^2
Texas Instruments	1Mb DRAM	N/A	1.0	132
Mitsubishi	1Mb DRAM	N/A	N/A	N/A
IBM	512K DRAM	Yes	1.3	121
Siemens	4Mb DRAM	N/A	0.9	142
Matsushita	16Mb DRAM	N/A	0.5	145
Toshiba	16Mb DRAM	Yes	0.7	325
JIT	16Mb DRAM	N/A	0.6	142
Matsushita	1Mb DRAM	N/A	0.7	134
Averages			0.8	163

Company	Trench	Cell Area Microns^2	Oxide Thickness (Angstroms)	Access Speed (ns)
Texas Instruments	Yes	21.3	N/A	14
Mitsubishi	N/A	N/A	N/A	N/A
IBM	N/A	75.2	235	20
Siemens	Yes	10.6	200	60
Matsushita	Yes	3.3	100	65
Toshiba	Yes	6.1	N/A	10
JIT	Yes	4.16	N/A	60
Matsushita	Yes	41.6	180	14
Averages		23.2	178	35

N/A = Not Available

Source: ISSCC

Comparing the Table 4 numbers with last year's specifications, we see a routine improvement of 39 percent in average DRAM density, from 5.0Mb to 6.9Mb. The average design rules also evolve from 0.9 micron to 0.8 micron. However, in cell area, oxide thickness, and speed, we see the emphasis being placed on performance and reliability. For instance, the average oxide thickness actually increases from 148 angstroms to 178 angstroms. The cell area increases from an already large 97 square mils to a whopping 129 square mils (if we exclude Toshiba's enormous 325-square mils chip). Finally, the access speeds of the devices improve by more than 86 percent, increasing from 65ns to 35ns.

Table 5 compares DRAM specifications for 1987 and 1988. We can see from this comparison that the emphasis was on design rather than brute-force cell shrinkage. Even though trench capacitors were used in six of the eight DRAM papers, their use did not shrink the chip size. We found that two papers were identified as using epitaxy (we suspect that they were used in many others), but that these devices were of the fastest.

We believe that this exemplifies a tendency that reestablishes itself at each generation of technology--that chip manufacturers are driven to put more performance on each chip rather than to make the chips smaller. In other words, performance is the first priority, die size is the second.

Table 5

Comparison of DRAM Specifications (1987 versus 1988)

Attribute	1987	1988
Cell Area (Square Microns)	14	23
Minimum Geometry (Microns)	0.9	0.8
Die Size (Square Mils)	97	129
Access Speed (Nanoseconds)	65	35
Oxide Thickness (Angstroms)	148	179
Density (Megabits)	5	6.9

Source: ISSCC

Device Summary

We have extracted the averages of all device categories and displayed them in Table 6 for easy comparisons.

As we can see from Table 6, the design rules actually remained the same in 1988 as in 1987, at 1.5 microns. Design played an important role since the die size decreased in general but increased for the memory categories. Chip access speeds improved from 55ns to 35ns. While this does not in itself signify the toppling of DRAMs from their position as the manufacturing "technology driver," it lends credence to the arguments proffered by Dr. Billy Crowder, who gave this year's keynote address, which is the subject of the next section.

Table 6

Device Specifications
(1987 versus 1988)

Type	Geometry (Microns)	Area ($Mils^2$)	Oxide Thickness (Angstroms)	Access Speed (ns)
1987 Average	1.5	98	281	55
DRAM	0.9	97	148	65
Memory	1.2	78	192	63
Microprocessor	1.5	149	283	78
Analog	2.2	34	N/A	4
ASIC	1.4	122	N/A	9
Other	1.5	113	575	16
1988 Average	1.5	88	222	35
DRAM	0.8	129	179	35
Memory	1.1	109	231	37
Microprocessor	1.4	120	N/A	N/A
Analog	2.5	29	N/A	N/A
ASIC	1.7	88	205	1
Logic	1.4	102	180	22
Other	1.7	61	250	N/A

N/A = Not Applicable

Source: Dataquest
April 1988

KEYNOTE ADDRESS

One of the highlights of this year's session was the keynote address presented by Dr. Crowder of IBM, Yorktown Heights. His speech was entitled "Manufacturing . . . a New Science . . . and the Design Engineer." The speech embodied concepts that could very well determine which semiconductor companies will become the eventual winners in the race for market dominance.

The theme of the speech can be summarized as follows: The kind of production that will hone a semiconductor company's manufacturing prowess, enabling it to best cope with tomorrow's new technology, has shifted from DRAM production to the quick-turn, market-responsive ASIC device production. Dr. Crowder began the speech by drawing attention to the importance of the designer in the manufacturing of ICs. He said that, since the manufacturer has become the key to the success of the designed die, it is incumbent upon the designer to participate in the manufacturing process. The importance of ASIC devices is that they become a common driver between the manufacturing engineer and the designer.

Dr. Crowder offered the following definition: Manufacturing science is identifying, understanding, and describing the principles that must be used in repetitive manufacturing. He said that it is generally understood that manufacturing technology is the technology driver. This is because it allows the manufacturer to pay for the R&D costs associated with the development of advanced devices. Until now, it has been the DRAM that has provided the vehicle between technology and the market. But DRAMs, which are high-volume commodity devices, neglect many necessary manufacturing techniques. For instance, production scheduling software, in-line inspection techniques, and sophisticated testing are not cost-effective or are simply deemphasized in the manufacturing of commodity devices. It does not follow that a good manufacturer of DRAMs will be a good manufacturer of many low-volume products.

The marketplace is now changing and becoming more sophisticated. Advanced designs and applications are now driving the market. ASICs, then, will drive manufacturing. Dr. Crowder gave as an example from his IBM experience that the 4Mb DRAM was designed to complement ASICs.

The factors that favor ASICs as a manufacturing driver are as follows:

- Time-to-market requirements
- The coupling between chip architecture and applications
- The need for responsive manufacturing systems

These issues inextricably link the designer to the manufacturing process. Dr. Crowder went on to say that the infusion of manufacturing knowledge into the product and process design will be facilitated by the development of three key software tools: integrated computer-aided design, computer-aided manufacturing, and computer-aided test.

Dr. Crowder said that future manufacturing will include designing for manufacturability, introduction of more science and technology into manufacturing, bottom-up factory automation, and plant/enterprise integration (computer-integrated manufacturing). These are the same manufacturing components that will be required by successful ASIC manufacturers.

We have summarized some interesting points in Dr. Crowder's speech below:

- X-ray—X-ray mask processes are very complicated and degrade yields. X-ray systems will not be used in ASICs.
- Inspection—Inspection use in device fabrication will evolve as follows:

	1987	1996
Scanning Electron Microscopy	30%	45%
Optical Inspection	50%	10%
Laser Scanning Microscopy	5%	20%
Scanning Tunneling Microscopy	1%	15%

- Metallization—Metallization will approach 50 percent of processing cost for two reasons: Metal levels are increasing, and the need for planarization will increase the number of steps.

- Yield—The use of redundancy in RAMs tends to cause unreliability in ASICs. This is because, in metallization, not all faults cause defects. There is an inverse correlation between yield and field failures. Redundancy tends to permit poor yields on the silicon area while optimizing device yields with fusing alternatives. This also illustrates why DRAM manufacturers may not be successful with ASIC technology. Dr. Crowder said that manufacturers must learn yield improvement in the ASIC environment now.

Dr. Crowder concluded with a discussion of the design engineer. He said that the design engineer owns the design for manufacturing, participates in the manufacturing yields, and owns the design for testing.

DATAQUEST CONCLUSIONS

We could see some interesting trends developing at this year's ISSCC. Our newsletter subtitle, "From Density to Performance," and our conjecture that design is rising in prominence, has been borne out by analysis of the papers presented.

Manufacturing Implications

We have seen the industry accept, in one year, the fact that optical lithography will be able to produce 0.5–micron design rules in production with certainty, and will probably be able to go as low as 0.35–micron design rules. With this, attention has turned toward other matters, bringing the rest of manufacturing along.

Epitaxy versus High–Voltage Implantation

We saw the further emergence of epitaxy in CMOS processing. Although epitaxy reduces latch–up as line geometries grow smaller, it has a more profound effect on device performance. This year's concentration on performance leads us to believe that epitaxy will be used in the very next technology evolution, moving from microprocessors and high–performance CMOS logic to DRAMs. The new epitaxial reactors appear to be up to the task.

Since epitaxy reduces latch–up, what will be the fate of high–voltage implantation (HVI)? The retrograde well, with its concomitant latch–up protection, has been touted as the high–volume vehicle for high–energy applications. With epitaxy, will HVI be needed? There are two considerations that indicate that HVI will be used.

- First, from a cost–per–wafer standpoint, HVI has epitaxy beat. Since adequate performance may be obtained by clever design and die shrinkage, HVI may be used in some cases instead of epitaxy for latch–up protection.

- Second, even with epitaxy, the thickness of the epitaxial layer is important from both cost and performance considerations. Autodoping of the epitaxial layer during deposition requires that the layer be thicker than necessary. We believe that HVI of wells and buried layers after the epitaxial layer has been formed, along with rapid thermal annealing, will allow thinner layers to be grown, thereby improving cost and performance. Again, HVI will be used.

Trenches

We saw that trenches have become solidly established in the CMOS-device manufacturer's repertoire. Trench applications offer opportunities for equipment manufacturers in etching and deposition. For the new, low-pressure etching techniques, such as load-locked RIE, magnetron, or triode systems, we expect copious activity. We also expect to see significant new process applications movement in the newer, planar deposition systems as they target the polysilicon deposition market that has been held for so long by the tube type systems.

Metallization

The importance of ASIC manufacturing will increase the opportunities for aluminum and refractory metals and silicide deposition. As Dr. Crowder predicted, metallization costs will become 50 percent of the cost of fabricating a die. We observed an increase in the use of refractory metal this year. The metal of choice was tungsten, both in silicide form and as a pure interconnect.

Inspection

The use of inspection for critical defect measurement and for particulate detection has different importance in commodity and ASIC manufacturing. The Japanese companies, leaders in DRAM manufacturing, choose to inspect as little as possible. Inspection is a process step that injects defects into the process. It is better to establish a process window and then keep the process within this window.

As Dr. Crowder said, the manufacturing of many products in one plant, albeit in low volumes, will require more sophisticated test and inspection routines. A process window cannot be established when the process changes for each device that enters a piece of equipment. Because of the emphasis on performance, and hence, applications, we believe that semiconductor manufacturers will aggressively purchase the new inspection systems introduced within the last few years.

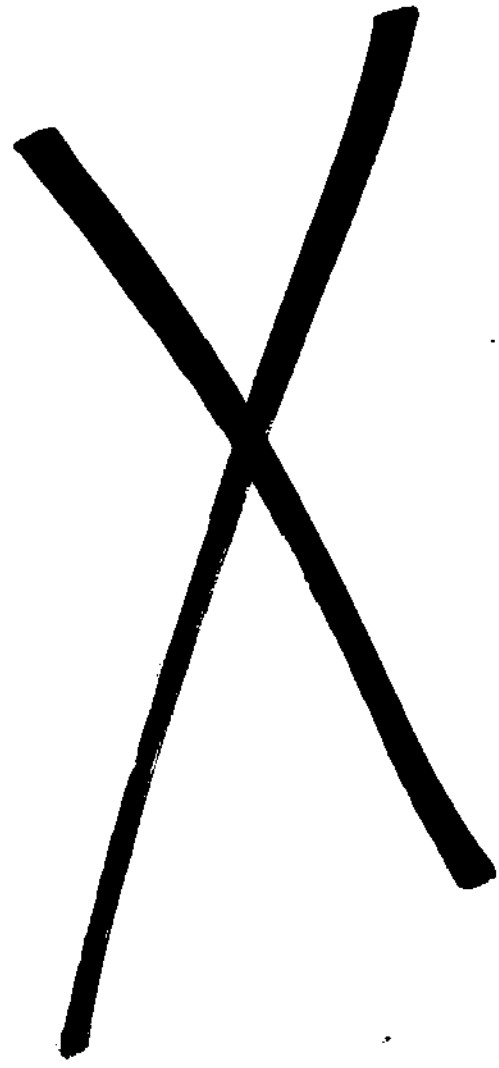
Density to Performance . . . and Back Again

We remember the evolution to smaller line geometries that occurred not so long ago as we approached 2-micron design rules. Many forecasters predicted that our polysilicon and silicon wafer capacities would be excessive. They believed that die sizes would shrink and silicon use would not increase as fast as silicon supply. This caused silicon suppliers to stop capacity buildup, which, in turn, caused a severe undercapacity situation in the latter half of the 1970s.

What actually happened was that semiconductor manufacturers used the newfound silicon area to build more performance into their chips not to decrease chip sizes. They did this because the market demanded it. It is now no surprise that the same trends appear after the recent evolution in DRAM technology.

We offer the conjecture that this play will always occur between density and performance, between standard products and ASICs, between design and manufacturing. Our industry will use each new manufacturing technology to bring more performance into the marketplace, and, in turn, use the standardization of these applications to develop new manufacturing technologies. It appears that the cycle has swung in favor of applications for now.

Robert McGeary



May Newsletters

The following is a list of newsletters found in this section:

Dataquest
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Research Newsletter

SEMS Code: Newsletters: 1987–1988: May 1988–16

WAFER FAB UPDATE— A TOUR OF THE NEW NORTH AMERICAN LEADING–EDGE FABS

SUMMARY

As part of the research that supports our North American fab data base, Dataquest conducts an annual survey of all the wafer fabs in North America. In conjunction with our survey, Dataquest has had the opportunity to tour some of the most advanced wafer fabs in North America. The results from this research include information on future semiconductor manufacturing trends and information on the announced, initiated, and forecast fab lines that will go into production during 1988 and into the 1990s. This information is reported in this newsletter.

PROFILE/TRENDS

Fifteen production and pilot–based silicon fabs will go into production this year, 19 will go into production in 1989, and 21 more are expected to come on–line in 1990. In addition to the production and pilot–based lines already mentioned, 20 other gallium arsenide, R&D, and quick–turn ASIC fabs should also come on–line during those three years. Dataquest also knows of 17 more fab lines that are planned to go into production after 1990.

Details of all the known future fabs in North America are listed in Table 1 and definitions to the column called status are listed in Table 2. For definitions of the fab type field, please see Table 3.

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398 / (408) 437-8000 / Telex 171973 / Fax (408) 437-0292

Table 1

North American Fab Data Base Fab Activity Planned or Initiated to Begin Production During 1988 and Beyond

Company	City	St.	Fab Name	Status	Target Date Prod. Began	Wafer Size	Clean Room Sq. Feet	Drawn Line-width	Process Technology	Products to Be Produced	Start Capacity per Month	Fab Type
1988												
AT&T BELL LABS	MCCUNGIE	PA	R&D	NEW SHELL/ CLEAN ROOM	/ /	4	20000	1.25	CMOS	LOG ASIC	9600	R
ELECTRONIC DECISIONS INC.	URBANA	IL	N/A	NEW CLEAN ROOM	07/01/88	3	2400	0.70	GaAs	MONOLITHIC ICs HYBRID	300	P
EXAR	SUNNYVALE	CA	TELMOS	UPGRADE	04/01/88	4	12000	3.00	BIP	LINEAR ARRAYS	13000	P
GAIN ELECTRONICS	SOMERVILLE	NJ	N/A	NEW SHELL/ CLEAN ROOM	03/01/88	3	9000	1.00	GaAs	LOG 4K SRAM ARRAYS CUSTOM	800	OFAT
GE SOLID STATE INTERSIL	SANTA CLARA	CA	SCOTT 3	NEW CLEAN ROOM	02/01/88	5	0	0.80	CMOS	N/A	0	P
GIGABIT LOGIC	NEWBURY PARK	CA	N/A	EQUIPMENT EXPANSION	01/20/88	3	6000	1.50	GaAs	CBIC 4K SRAM ROM CUSTOM	2000	NPAT
HONEYWELL MICRO-SWITCH	RICHARDSON	TX	N/A	NEW CLEAN ROOM	07/01/88	0	4000	2.00	BIP	HALL SENSORS	5600	P
HUGHES	MALIBU	CA	NEW R&D	NEW SHELL/ CLEAN ROOM	12/01/88	3	9000	0.20	GaAs	FET MMIC DIGITAL ICs	0	R
IBM	ESSEX JUNCTION	VT	ALPHA	N/A	02/01/88	8	25000	1.00	Si GATE MOS	1Mb DRAM	12000	P
IBM	ESSEX JUNCTION	VT	N/A	N/A	/ /	0	30000	1.00	CMOS	1Mb DRAM	0	P
ICI ARRAY TECHNOLOGY	SAN JOSE	CA	N/A	NEW CLEAN ROOM	03/01/88	0	0	0.00	N/A	ARRAYS	0	RAT
INTEL	RIO RANCHO	NM	FAB 9.1	NEW CLEAN ROOM	05/01/88	6	25000	1.00	CMOS	MIL STD 64K SRAM 386 MPU	15000	NP
LOCKHEED	SUNNYVALE	CA	113	NEW CLEAN ROOM	09/01/88	5	3000	1.50	CMOS	ASIC MIL STD RAD-HARD	640	P
MASS. MICRO-ELECTRONICS CENTER	WESTBOROUGH	MA	N/A	NEW SHELL/ CLEAN ROOM	12/01/88	5	12700	1.00	CMOS	N/A	0	R
MCDONNELL DOUGLAS	HUNTINGTON BEACH	CA	DVLPMNT	NEW CLEAN ROOM	03/01/88	3	4000	1.00	GaAs	MPU LOG ASIC DIS	0	P
MOTOROLA	MESA	AZ	MOS-6	UPGRADE	12/01/88	6	36000	1.00	CMOS TOSHIBA M2	1Mb DRAM SRAM	33600	F
NATIONAL SECURITY ADMINISTRATION	FORT MEADE	MD	N/A	NEW SHELL/ CLEAN ROOM	/ /	6	0	1.00	BIP CMOS MOS	CUSTOM MIL STD	0	P
NATIONAL SEMI-CONDUCTOR	SANTA CLARA	CA	BLDG E	READY FOR EQUIPMENT	12/01/88	6	10000	1.00	BIP CMOS MOS BICMOS	ALL R&D FUNCTIONS	4000	P
NATIONAL/FAIRCHILD	PUYALLUP	WA	N/A	EQUIPMENT EXPANSION	01/01/88	5	10000	1.00	BICMOS M2 ECL I/O	64K 256K FASTSRAM 4 TR.	3150	P
RAYTHEON	WALTHAM	MA	N/A	NEW SHELL/ CLEAN ROOM	/ /	3	11000	0.00	GaAs	MMIC	400	NP
SANDIA NATIONAL LABS	ALBUQUERQUE	NM	RHIC-II	NEW SHELL/ CLEAN ROOM	02/01/88	6	15000	0.90	CMOS	RAD-HARD MPU SRAM ASIC	320	RAT
SEMATECH	AUSTIN	TX	N/A	NEW CLEAN ROOM	12/01/88	6	15000	0.80	CMOS	1Mb DRAM 64K SRAM (6 TR.)	6400	R
SGS-THOMSON MICROELECTRONICS	CARROLLTON	TX	FAB 6	EXPANSION UP-GRADE	07/01/88	6	30000	1.20	CMOS M2	64K SRAM 50K ARRAYS CBIC	14400	NPAT
SIGNETICS	ALBUQUERQUE	NM	FAB 23	NEW CLEAN ROOM	08/01/88	6	27000	1.25	CMOS	256K 1Mb EPROM 8-bit MCU	5600	F
TI	DALLAS	TX	DMOS 4.2	NEW CLEAN ROOM	06/01/88	6	30000	1.00	CMOS BICMOS	1Mb DRAM 256K SRAM	23750	F
VLSI TECHNOLOGY	SAN ANTONIO	TX	MODULE A	NEW SHELL/ CLEAN ROOM	10/01/88	6	10000	1.25	CMOS M3	ARRAYS CBIC SRAM MPU E2	6800	F

(Continued)

Table 1 (Continued)

North American Fab Data Base Fab Activity Planned or Initiated to Begin Production During 1988 and Beyond

Company	City	St.	Fab Name	Status	Target Date Prod. Began	Wafer Size	Clean Room Sq. Feet	Drawn Line-width	Process Technology	Products to Be Produced	Start Capacity per Month	Fab Type
1989												
BALL AEROSPACE	BOULDER	CO	N/A	NEW CLEAN ROOM	/ /	0	0	1.20	N/A	N/A	0	F
DIGITAL EQUIPMENT	HUDSON	MA	PILOT	NEW CLEAN ROOM	04/01/89	6	14000	1.50	CMOS	MPU MCU MPR CBIC CUSTOM	1600	P
FUJITSU	GRESHAM	OR	N/A	NEW SHELL/ CLEAN ROOM	03/01/89	5	35000	1.50	BIP ECL CMOS	ARRAYS 30K-100K	28000	F
GENESIS MICRO-CHIP INC.	MARKHAM, ONTARIO	CN	N/A	NEW SHELL/ CLEAN ROOM	05/01/89	6	20000	1.50	CMOS M2	PLD ARRAYS CBIC CUSTOM	8000	F
HITACHI	IRVING	TX	N/A	NEW CLEAN ROOM	05/01/89	6	40000	1.30	CMOS	1Mb DRAM 256K SRAM ASIC	16000	F
IBM	ESSEX JUNCTION	VT	N/A	N/A	/ /	0	30000	1.00	CMOS	1Mb DRAM	0	F
IBM	ESSEX JUNCTION	VT	N/A	N/A	/ /	0	30000	1.00	CMOS	1Mb DRAM	0	F
IBM	HOPEWELL JUNCTION	NY	ASTC	NEW SHELL/ CLEAN ROOM	05/01/89	8	60000	0.80	CMOS	4Mb DRAM 1Mb SRAM	32000	P
INTEL	RIO RANCHO	NM	FAB 9.2	NEW CLEAN ROOM	11/01/89	6	25000	1.00	CMOS	N/A	15000	P
INTEL	SANTA CLARA	CA	D2	NEW SHELL/ CLEAN ROOM	09/01/89	6	35000	0.80	CMOS	EPROM MPU TECH. DEV.	12000	F
MICRON TECHNOLOGY	BOISE	ID	FAB 3	NEW SHELL/ CLEAN ROOM	02/01/89	6	35000	1.00	CMOS	1Mb DRAM 256K SRAM VRAM	14400	P
MITSUBISHI	DURHAM	NC	N/A	NEW SHELL/ CLEAN ROOM	04/01/89	6	7000	1.20	CMOS	CBIC ARRAYS CUSTOM	5600	CAT
MOTOROLA	MESA	AZ	BP-5	NEW CLEAN ROOM	/ /	6	25000	1.00	BIP BICMOS	ADVANCED BIP	16000	F
NCR	COLORADO SPRINGS	CO	FAB 2	NEW CLEAN ROOM	02/01/89	5	11000	1.20	CMOS	MPU LOG ASIC MEM	6400	FAT
NORTHRUP	LOS ANGELES	CA	N/A	N/A	/ /	0	0	0.00	N/A	N/A	0	R
RAMTRON	COLORADO SPRINGS	CO	N/A	NEW SHELL/ CLEAN ROOM	03/01/89	4	0	2.00	GaAs CMOS M2	FERRAM FERRO ELECTRIC RAM	0	C
RAYTHEON MICRO-ELECTRONICS CTR.	ANDOVER	MA	GaAs	NEW SHELL/ CLEAN ROOM	01/15/89	3	0	0.50	GaAs	N/A	800	F
RICOH	SAN JOSE	CA	N/A	NEW SHELL/ CLEAN ROOM	10/01/89	6	20000	1.00	N/A	N/A	9600	F
SGS-THOMSON MICROELECTRONICS	SCOTTSDALE	AZ	N/A	READY FOR EQUIPMENT	12/01/89	6	22000	0.80	CMOS	N/A	12000	F
SIMTEK	COLORADO SPRINGS	CO	N/A	NEW SHELL/ CLEAN ROOM	02/01/89	6	2000	1.00	CMOS	ADV. MEM EEPROM	800	P
TOSHIBA	PORTLAND	OR	N/A	NEW SHELL/ CLEAN ROOM	/ /	6	25000	1.00	N/A	N/A	12000	F
UNIVERSITY OF WASHINGTON	SEATTLE	WA	N/A	N/A	/ /	0	0	0.00	N/A	N/A	0	R
WESTERN DIGITAL	COSTA MESA	CA	DVLPMNT	NEW SHELL/ CLEAN ROOM	/ /	5	12000	1.25	CMOS M2	CUSTOM	6400	F
WESTINGHOUSE	CHURCHILL	PA	R&D CTR.	NEW SHELL/ CLEAN ROOM	03/01/89	0	0	0.00	GaAs	REDUNDENT INTERCONNECT	0	P
XICOR	MILPITAS	CA	PHASE 2	NEW CLEAN ROOM	02/01/89	6	25000	0.80	CMOS M2 POLY3	1Mb 4Mb EEPROM	12000	P

(Continued)

Table 1 (Continued)

North American Fab Data Base Fab Activity Planned or Initiated to Begin Production During 1988 and Beyond

Company	City	St.	Fab Name	Status	Target Date Prod. Began	Wafer Size	Clean Room Sq. Feet	Drawn Line-width	Process Technology	Products to Be Produced	Start Capacity per Month	Fab Type
1990												
AMCC	SAN DIEGO	CA	N/A	NEW CLEAN ROOM	/ /	6	15000	1.00	BIP	ARRAYS CBIC	8000	F
AMD	SUNNYVALE	CA	R&D CTR	N/A	/ /	0	35000	0.80	N/A	N/A	0	R
AT&T	ORLANDO	FL	OR2	NEW CLEAN ROOM	03/01/90	6	35000	1.20	CMOS	MEM	22400	F
CRYSTAL SEMI-CONDUCTOR	AUSTIN	TX	N/A	NEW SHELL/ CLEAN ROOM	/ /	0	0	1.20	MOS	LIN A/D D/A	0	F
DALLAS SEMI-CONDUCTOR	DALLAS	TX	FAB 2	N/A	04/01/88	6	20000	1.00	CMOS	SRAM CCD	12000	F
IBM	ESSEX JUNCTION	VT	N/A	N/A	/ /	0	30000	0.80	CMOS	4Mb DRAM	0	F
IBM	SAN JOSE	CA	N/A	NEW SHELL/ CLEAN ROOM	/ /	8	25000	0.80	N/A	N/A	12000	F
IDT	SANTA CLARA	CA	N/A	NEW SHELL/ CLEAN ROOM	/ /	0	0	0.70	CMOS	PROCESS DEVELOPMENT	0	P
LINEAR TECHNOLOGY CORP.	MILPITAS	CA	FAB 2	NEW CLEAN ROOM	01/01/90	5	7500	2.00	BIP CMOS	LIN	6400	F
MAXIM INTEGRATED PRODUCTS	SUNNYVALE	CA	N/A	NEW CLEAN ROOM	02/01/90	0	0	2.00	BIP CMOS	OP AMPS A/D D/A	0	P
MOTOROLA	AUSTIN	TX	MOS 12	NEW SHELL/ CLEAN ROOM	/ /	6	35000	0.80	CMOS TOSHIBA	4Mb DRAM	24000	F
MOTOROLA	SCHAUMBERG	IL	N/A	NEW CLEAN ROOM	/ /	0	10000	5.00	BIP	SMARTPOWER	0	P
NATIONAL SEMICONDUCTOR	ARLINGTON	TX	CMOS 2	NEW CLEAN ROOM	09/01/90	6	25000	1.00	CMOS	N/A	18000	F
NEC	ROSEVILLE	CA	PHASE 2	NEW SHELL/ CLEAN ROOM	03/01/90	8	70000	0.70	CMOS	4Mb DRAM	16000	FAT
RAYTHEON	MOUNTAIN VIEW	CA	N/A	NEW CLEAN ROOM	/ /	6	12000	1.00	N/A	N/A	6400	F
SAN JOSE STATE UNIVERSITY	SAN JOSE	CA	N/A	N/A	/ /	0	0	0.00	N/A	N/A	0	R
SHARP	CAMUS	WA	N/A	NEW CLEAN ROOM	/ /	6	20000	1.00	MOS	N/A	9600	F
SIERRA SEMI-CONDUCTOR	SAN JOSE	CA	N/A	READY FOR EQUIPMENT	/ /	6	0	0.80	N/A	N/A	0	F
SIGNETICS	ALBUQUERQUE	NM	FAB 24	NEW CLEAN ROOM	/ /	6	27000	1.00	N/A	N/A	8000	F
TI	DALLAS	TX	N/A	N/A	02/01/90	6	30000	0.70	CMOS	4Mb DRAM	20000	F
TI	DALLAS	TX	N/A	N/A	11/01/90	8	25000	0.70	N/A	N/A	16000	F
U.C. SANTA BARBARA	SANTA BARBARA	CA	N/A	NEW SHELL/ CLEAN ROOM	/ /	0	0	0.00	GaAs	N/A	0	R
VLSI TECHNOLOGY	SAN ANTONIO	TX	MODULE B	NEW CLEAN ROOM	06/01/90	6	10000	1.00	CMOS M3	ARRAYS CBIC SRAM MPU E2	6800	F
ZILOG	NAMPA	ID	MOD 3	NEW SHELL/ CLEAN ROOM	/ /	6	12000	1.00	N/A	N/A	8000	F

(Continued)

Table 1 (Continued)

North American Fab Data Base Fab Activity Planned or Initiated to Begin Production During 1988 and Beyond

Company	City	St.	Fab Name	Status	Target Date Prod. Began	Wafer Size	Clean Room Sq. Feet	Drawn Line-width	Process Technology	Products to Be Produced	Start Capacity per Month	Fab Type
1991												
CYPRESS SEMICONDUCTOR TEXAS INC.	ROUNDROCK	TX	FAB 3	NEW SHELL/ CLEAN ROOM	/ /	6	0	0.70	CMOS	N/A	8000	F
DIGITAL EQUIPMENT	SAN JOSE	CA	N/A	NEW SHELL/ CLEAN ROOM	/ /	6	10000	0.80	N/A	N/A	3200	P
IDT	SALINAS	CA	FAB 4	NEW SHELL/ CLEAN ROOM	/ /	6	24000	0.70	CMOS	SRAM LOG DSP FIFO	10800	F
INTEL	RIO RANCHO	NM	FAB 9.3	NEW CLEAN ROOM	/ /	6	25000	0.80	CMOS	N/A	24000	F
INTEL	SANTA CLARA	CA	N/A	NEW SHELL/ CLEAN ROOM	/ /	6	12000	0.80	CMOS	ARRAY BASE WAFERS	8000	NP
NATIONAL/FAIRCHILD	PUYALLUP	WA		NEW CLEAN ROOM	11/01/91	6	0	0.80	BICMOS	SRAM	0	F
OKI	SILICON VALLEY	CA	N/A	NEW SHELL/ CLEAN ROOM	04/01/91	6	15000	1.00	CMOS	ARRAYS	8000	C
SIGNETICS	OREM	UT	N/A	NEW SHELL/ CLEAN ROOM	/ /	6	20000	1.00	BIP	N/A	12000	F
VLSI TECHNOLOGY	SAN ANTONIO	TX	MODULE C	NEW CLEAN ROOM	09/01/91	6	10000	1.00	CMOS M3	ARRAYS CBIC SRAM MPU E2	6800	F
1992												
EXAR	FREMONT	CA	N/A	NEW SHELL/ CLEAN ROOM	/ /	6	0	1.00	CMOS	LIN DSP MPU	0	F
INTEL	RIO RANCHO	NM	FAB 9.4	NEW CLEAN ROOM	/ /	8	25000	0.70	CMOS	N/A	20000	F
TI	DALLAS	TX	N/A	N/A	01/01/92	8	25000	0.70	N/A	N/A	16000	F
VLSI TECHNOLOGY	SAN ANTONIO	TX	MODULE D	NEW CLEAN ROOM	11/01/92	6	10000	1.00	CMOS M3	ARRAYS CBIC SRAM MPU E2	6800	F
1993												
NATIONAL SEMICONDUCTOR	ARLINGTON	TX	CMOS 3	NEW CLEAN ROOM	/ /	8	25000	0.70	CMOS	N/A	14400	F
1994												
CYPRESS SEMICONDUCTOR TEXAS INC.	ROUNDROCK	TX	FAB 4	NEW SHELL/ CLEAN ROOM	/ /	6	0	0.55	CMOS	N/A	8000	F
NEC	HILLSBORO	OR	PHASE 3	NEW SHELL/ CLEAN ROOM	/ /	8	90000	0.50	CMOS	16Mb DRAM	16000	FAT

Source: Dataquest
May 1988

Table 2

Nomenclature and Definitions
Status Field

Nomenclature	Definition
NEW SHELL/CLEAN ROOM	Brand new from the ground up (green field)
NEW CLEAN ROOM	The building is complete and ready for clean room installation
READY FOR EQUIPMENT	The clean room is complete and ready for equipment installation
CLEAN ROOM EXPANSION	Increase of total square footage for an existing clean room
EQUIPMENT EXPANSION	The installation of additional equipment to an existing clean room
EXPANSION	An increase in total clean room square footage and installed equipment
CLEAN ROOM UPGRADE	Improved cleanliness, design, DI water, and/or vibration isolation
EQUIPMENT UPGRADE	Conversion to larger wafer size and/or finer linewidths; equipment replacement, retrofit, and/or refurbishment
UPGRADE	Clean room upgrade and equipment upgrade
RERAMP FROM SHUTDOWN	Brought back into production from a shutdown

Source: Dataquest
May 1988

Table 3

Code Definitions
Fab Type Field

Letter Code	Definition	Comments
F	Fab	Front-end processing; wafer start-up to die probe
P	Pilot line	Initial production or intended low volume
C	Quick-turn fab, personalizes gate arrays	Final mask layers only; base wafers from other location
R	Semiconductor research facility	Very small lot runs and R&D
A	Assembly	Back-end processing, sawing, and packaging
T	Test	Back-end processing; final device test
N	Nondedicated foundry service available	Excess capacity
O	Dedicated foundry supplier	Only manufactures customer designs
H	Headquarters	
UH	Foundry user headquarters address and company information	
U	Foundry user company name	All other information is on foundry supplier
K	Closed fab	
D	Design center	

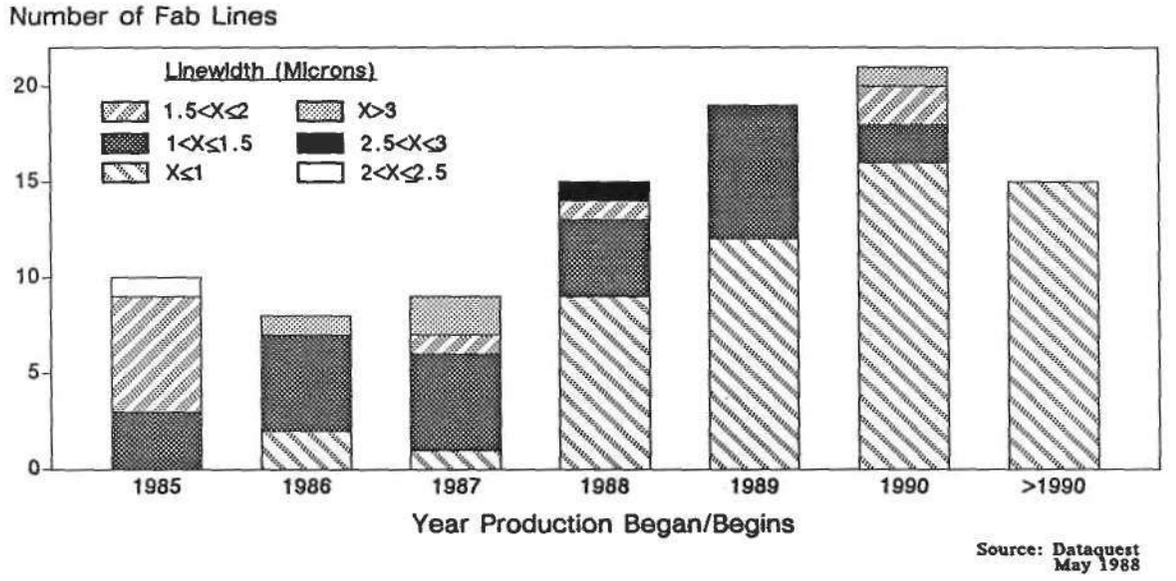
Source: Dataquest
May 1988

Of all the new fab lines that will come on–line during 1988 and beyond, 75 percent will be CMOS, and almost all of them will have drawn linewidths below 1.6 microns. Of these future fabs, 73 percent will be running 6–inch wafers and only 18 percent will be running 8–inch wafers. Some new 5–inch wafer fabs are still on the way, which will represent 9 percent of these future fab lines.

Figure 1 summarizes the number of fabs by linewidth that have come on–line since 1985 and the fabs that are expected to come on–line in the future. Virtually all of the new wafer fabs are sub–1.6 micron facilities. The exceptions to this trend are in the linear and power IC fab lines that will be installed. By 1990, a clear majority of the wafer fabs that go into production will do so on leading–edge processes at less than 1.1 microns. Please refer to Table 4 for Dataquest's forecast of drawn line widths for typical production, leading–edge production, and R&D.

Figure 1

New Silicon Pilot and Fab Lines
Actual, Announced, and Forecast



Source: Dataquest
May 1988

Table 4

Drawn Linewidths

	1988	1991	1994
Typical Production	1.5-2 micron	1-1.5 micron	0.8-1.2 micron
Leading Edge	1-1.4 micron	0.7-0.8 micron	0.5-0.6 micron
R&D	0.8 micron	0.5-0.6 micron	0.35-0.4 micron

Source: Dataquest
May 1988

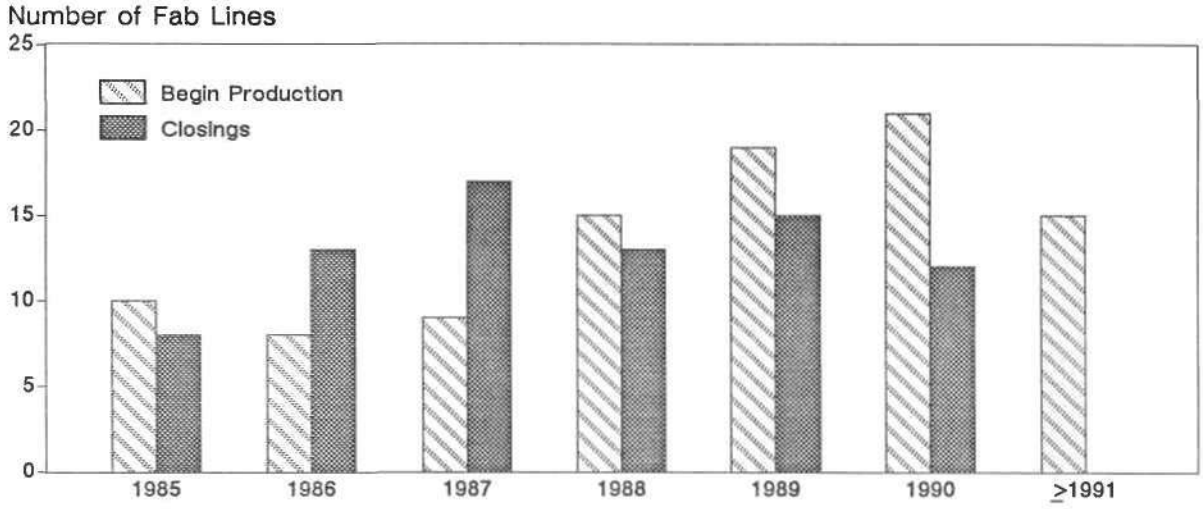
Figure 2 summarizes the number of fab lines that have or will open versus the number that have or will close. Figure 3 depicts the net effect of the new fab lines coming on-line and the older fab lines being shut down. During 1985, 10 fab lines came on-stream even though the industry was flat on its back from the worst recession it has ever seen. Some of these fab lines were brought up because it was too late to put them on hold, and some were brought up in response to technology-driven demand for devices in the 1.5- to 2-micron range. A few companies were still limited in terms of capacity for 1.5- to 2-micron devices. Most of the overcapacity that the industry experienced came from the 3- to 5-micron range. During 1986 and 1987, a majority of the fab lines that came up, did so in response to new demand in the 1.5-micron range, while most of the fab lines that shut down were in the 3- to 5-micron range. So far this year, seven fabs have been shut down, and six more will be shutting down in the second half. Overall capacity utilization has climbed to 83 percent for North America. In the 1.1- to 2-micron range for microdevices and standard logic, capacity utilization is between 88 percent and 95 percent and very tight.

Net installation of new fabs will be positive this year, and is expected to stay positive through 1990. This trend will be both capacity and technology driven. It is important to note that, in terms of square inches, the old fabs that are shutting down have much less capacity than the new ones coming on-line. This is due not only to the larger wafer sizes produced in the new fabs but also to the fact that, based on the installed fabs, the average start capacity tends to increase as the wafer size increases—with the exception of quick-turn ASIC fabs.

Dataquest is forecasting that 15 fab lines will shut down during 1989 and that 12 more will be shut down during 1990. This forecast is based on the fact that there are still 8 2-inch and 34 3-inch silicon fab lines in North America. Those companies that still consume large volumes of 2- and 3-inch wafers are getting pressure from the silicon suppliers to convert to larger wafer sizes because production of the smaller wafers is not economical. Dataquest expects most of the 2- and 3-inch fabs to shut down during the next two years, along with some 4-inch fabs.

Figure 2

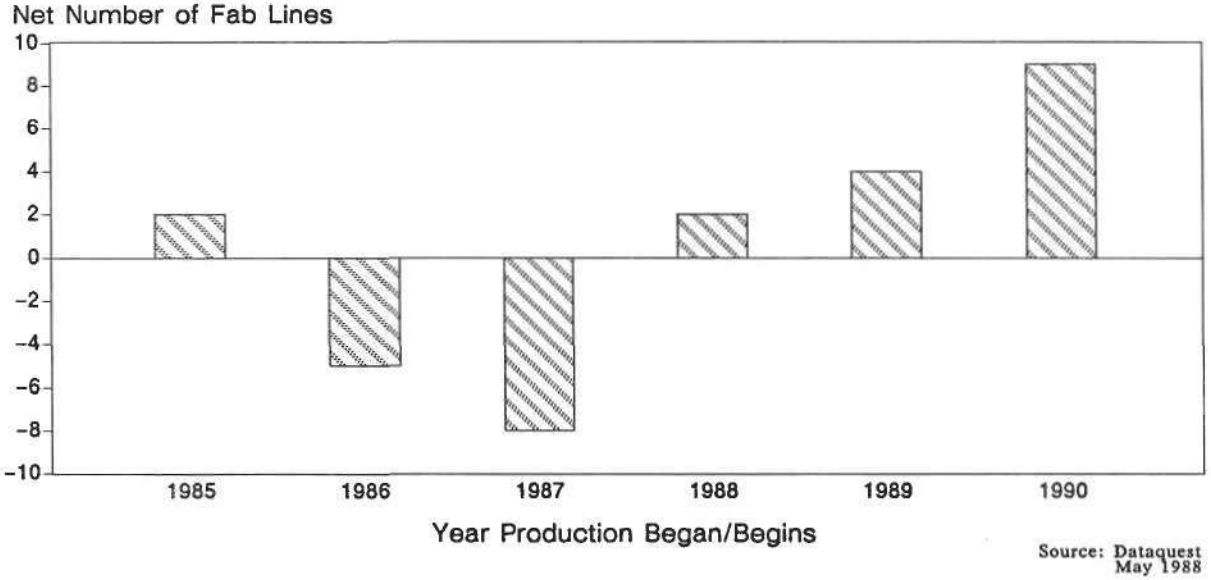
Silicon Pilots and Fab Lines



Source: Dataquest
May 1988

Figure 3

Silicon Pilot and Fab Lines



Source: Dataquest
May 1988

Production of semiconductors on 8-inch wafers has just started and has a very long way to go. The first 8-inch wafer fab in the world went out of R&D and ramped up toward production levels during the fourth quarter of 1987 at IBM Essex Junction, Vermont. A second 8-inch facility at Essex Junction recently qualified to ramp up. Both fabs are producing 1Mb DRAMs. Dataquest expects that no more than 12 8-inch fabs will be installed worldwide by the end of 1990. Six of these fabs will be in North America, four in Japan, and two in Germany. The majority of these facilities will be owned by IBM. Dataquest estimates that 8-inch wafers will represent only 4.6 percent of the total silicon square inches used worldwide during 1991.

DATAQUEST'S TOUR OF ADVANCED WAFER FABS

Dataquest recently took a tour of leading-edge wafer fabs that are coming on-line this year. Some common ideas were apparent in terms of fab design, cleanliness, and equipment ordering.

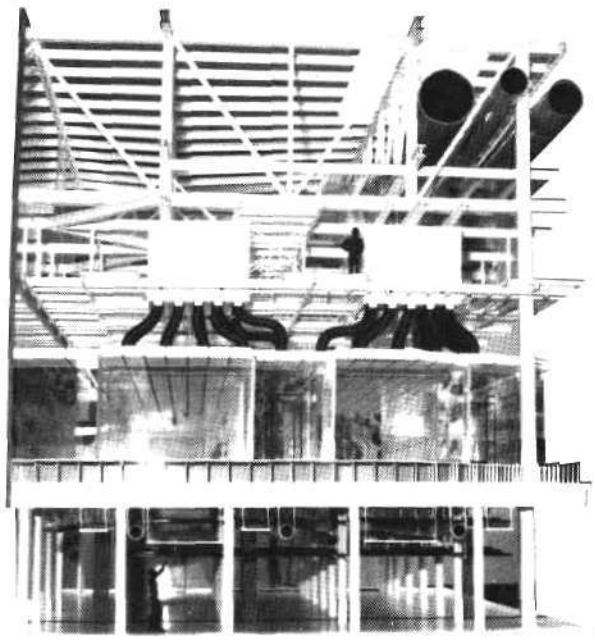
Basic Construction

Most of today's leading-edge fabs are constructed with three levels: the chase area in the basement, the clean room on the second level, and the HVAC system on the third level. (Please refer to Figure 4.) All of these facilities are designed for full vertical laminar flow (VLF), and most are built to meet the H6 occupancy code (building code for facilities that handle hazardous and/or combustible gases, chemicals, and waste). The clean room is supported by a concrete waffle slab that allows the air to pass through it into the basement. The concrete slab is about 30 inches thick and is supported by concrete piles that go through the slab on grade (basement floor), preferably into bedrock. These piles are fully isolated from the vibration of the shell of the building and the slab on grade. This design results in a clean-room floor that is isolated from the vibrations of the building, fans, pumps, and footsteps that are being generated above, below, and around it. The waffle slab is covered by a floor of perforated white tiles that look the same as the tiles seen in a computer room. The vibration levels of these waffle slabs range from 0.01 micron to 0.025 micron between 0Hz and 50Hz. All of these fabs claim to be class 5 or less at 0.3 microns (no more than 5 particles larger than 0.3 microns per cubic foot of air). These facilities change the air in the clean room every 10 seconds or less.

Companies are requiring that the fab be "built clean," since they are now filtering particles that are smaller than some bacteria. They are training the construction crews that build these fabs to understand the impact they have on the fab's success. The construction crews are required to clean up after themselves constantly as they work.

Figure 4

Model of Intel's Fab D2 Santa Clara



Source: Intel Corporation

Vibration Levels

Vibration levels are becoming very critical and semiconductor manufacturers are now taking many sources of vibration into consideration. One manufacturer has isolated the large fans (which handle the air exchange) from the shell as well as from the fab floor as an extra precaution. The fans are mounted with the axles in a vertical position instead of a horizontal position to further reduce vibrations. Temperature control systems are sound dampened to reduce vibrations caused by noise. Consideration is given to the site location: how close do the commercial and military jets get to the fab, and how close is the nearest quarry, railroad track, and freeway.

Flexibility and Incremental Capacity Growth

If only two words could be used to describe the new leading-edge fabs, the words would be flexible and incremental. These fabs are flexible because they have been set up to allow hookups to any gas, chemical, and power source at all areas of the fab floor. Walls in these clean rooms are movable and non-loadbearing. These designed-in features will allow the owners to completely reconfigure the layout of the fab floor when needed in the future.

These new fabs are incremental because clean room expansion can be done in phases within one shell, and equipment can be installed into the clean room incrementally. In North America, clean room shells are currently in place for 25 future wafer fabs. Since it usually takes one year to go through the building permit, planning, and design processes, and an additional year to actually construct a facility, having a shell in place can save up to two years in the time it takes to activate a wafer fab. These shells can be equipped with a clean room/HVAC system, DI water, gas/chemical-handling systems, and equipment in one year, and then begin qualifying the equipment. Examples of these types of facilities include Intel's fab 9, Signetics' fab 23, TI's DMOS IV, and VLSI Technology's San Antonio fab. All of these facilities have room for between two and four clean rooms.

Most of the companies studied during Dataquest's tour are ordering equipment in two to five incremental segments over time, as opposed to ordering all the equipment for the fab floor in one large order. This is a safer and more stable approach for both the equipment vendor and the equipment user.

FAB MANAGER COMMENTS

While a lot of effort is going into designing and constructing clean rooms that are ultra clean and vibration resistant, managers of most of these leading-edge facilities think they are spending too much time and money on the design, construction, and maintenance of clean rooms. Their thinking is that what really matters is the cleanliness of the environment that the wafer passes through. What these managers would like to be able to do is start putting the clean room into the equipment, not put the equipment into the clean room. These managers want to maintain wafer integrity with little or no clean room space required. Some of these semiconductor manufacturers are developing their systems to achieve this goal, while others are looking at the SMIF system or a derivative of it.

DATAQUEST CONCLUSIONS

Dataquest believes that the industry will ultimately evolve away from clean rooms as we know them today. The industry will move toward the concept of supporting little or no clean room space. This concept is, however, a long way off. For now and into the early 1990s, Dataquest's conclusions are:

- 8-inch production is in its infancy, and Dataquest expects large-scale movement into 8-inch production not to occur until some time after 1991.
- The vast majority of fabs that go into production will be sub-1.6 micron, 6-inch, CMOS lines.
- Most new clean rooms will use the three-level full VLF design and will be class 5 or better at 0.3 microns.
- Fab shells will be built for incremental clean room additions.
- Clean rooms will be filled with incremental equipment orders.

Mark T. Reagan

Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987–1988 Newsletters: May 1988–15

JAPANESE EPITAXY MARKET DEMAND REMAINS FLAT

SUMMARY

Metalorganic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) equipment is used to fabricate optoelectronic, microwave, and advanced digital devices using gallium arsenide (GaAs) and other Group III–V and II–VI compound materials. Since 1983, the Japanese market for MOCVD and MBE equipment has grown at a 4.8 percent compound annual growth rate (CAGR). Despite the market downturn in 1987, Dataquest expects moderate growth over the next three years for a variety of reasons:

- The Japanese optoelectronic device market is expected to grow at a 9.9 percent CAGR (yen value) from 1987 to 1990 because of demand for optoelectronic switching chips, compact disk lasers, and optical fiber communications emitters and receivers.
- Japan Broadcasting Corporation's (NHK's) direct satellite broadcasting this year will boost sales of satellite antennas using high electron mobility transistors (HEMT), but volumes will be limited.
- Advanced work on ultrafast GaAs–based digital devices for supercomputers is accelerating, but the market is still small.

We expect MOCVD and MBE equipment to move gradually from R&D centers to full production lines in Japan over the next few years. Major users, such as Rohm and Sony, are already using this equipment on their production lines.

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398 / (408) 437-8000 / Telex 171973 / Fax (408) 437-0292

TECHNOLOGY OVERVIEW

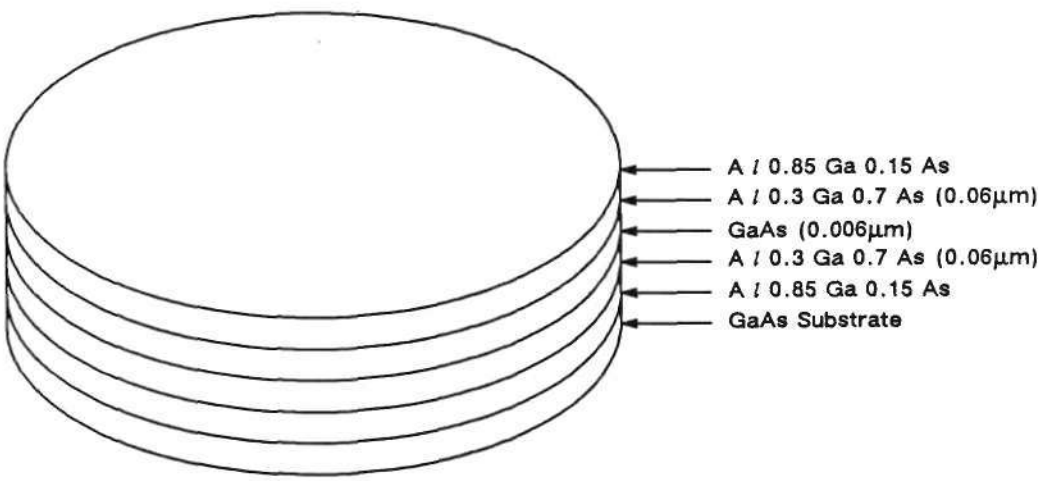
MOCVD, MBE, and metalorganic MBE (MOMBE) are methods for depositing epitaxial films used in the fabrication of optoelectronic, microwave, and digital devices. Metals and compound semiconductor films from the II–VI, IV–VI, IV, and III–V groups of "The Periodic Table of Elements" are most commonly used. MOCVD, MBE, and, more recently, MOMBE have attracted favorable industry response because of the following features:

- Highly accurate control of thin–film thickness
- Capability of developing superlattices and heterostructure devices
- Excellent growth uniformity over large wafer areas

The three methods involve depositing from one to many epitaxial layers onto bare compound semiconductor wafers. Figure 1 shows a typical substrate with epitaxial layers for a quantum–well laser device. Figure 2 shows the structure of a HEMT. MOCVD, MBE, and MOMBE are superior to conventional liquid–phase epitaxy (LPE) and other silicon epitaxy systems, which cannot be used to produce quantum–well laser and HEMT devices.

Figure 1

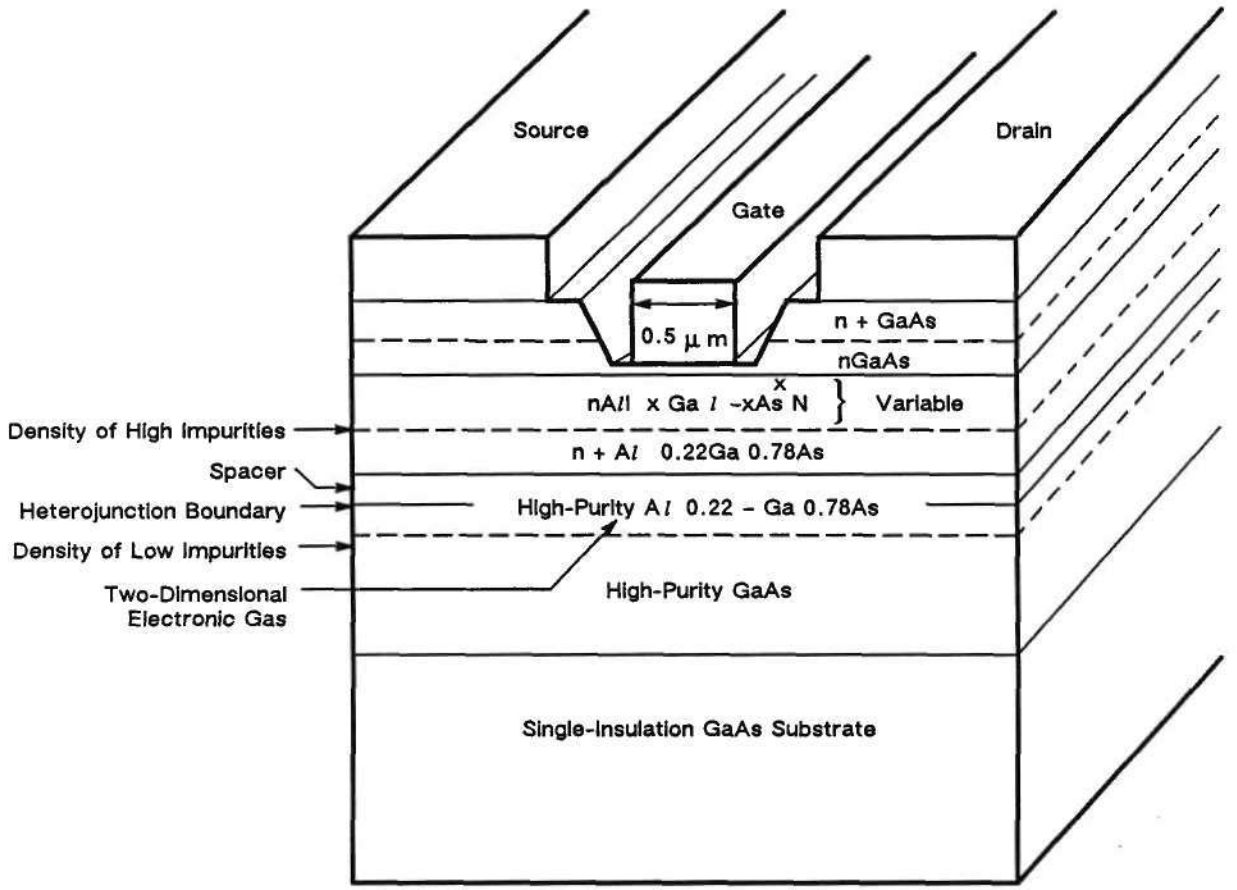
Quantum–Well Laser Structure



Source: Dataquest
May 1988

Figure 2

0.5–Micron–Gate HEMT



Source: Dempa Shimbun
Dataquest
May 1988

Molecular Beam Epitaxy

MBE is an ultrahigh-vacuum evaporation technique used to deposit epitaxial layers of metals, semiconductors, and compound semiconductors. Table 1 lists several materials that are deposited via MBE. The following is a list of optoelectronic and advanced devices fabricated using MBE:

- Microwave/digital
  - Diodes
    - IMPATT
    - Varactor
    - Mixer
  - Field-effect transistors (FETs)
    - Low noise/power
    - High electron mobility transistor (HEMT)
    - Heterojunction bipolar transistor (HBT)
    - Hot electron/ballistic transistor
    - Permeable base transistor
    - Metal base transistor
    - Heterojunction insulated-gate transistor (HIGFET)
    - Semiconductor-insulator-semiconductor transistor
- Optoelectronic
  - Diodes
    - Light-emitting diode (LED)
    - Avalanche photodiode detector
  - Lasers
    - Single heterojunction
    - Double heterojunction
    - Multiple quantum well
    - Distributed feedback
    - Graded index, separate confinement heterojunction (GRINSCH)

- Integrated circuits
  - High electron mobility transistor 4K SRAM

In MBE, film deposition occurs in growth chambers in which a beam of molecules is aimed at a heated substrate. The molecular beam source is a Knudsen cell, which is a crucible surrounded by an oven. As the oven heats up, the solid material vaporizes into molecules that are directed toward the heated wafer. Epitaxial growth rate on the wafer surface is controlled by wafer temperature and molecular beam flux. The relatively slow growth rate (1 micron per hour) allows precise control of film thickness, doping profile, and abrupt film interfaces. Separate sources are required for each material. A typical MBE system has up to eight sources, each controlled by a shutter mechanism.

Major Japanese MBE vendors are Anelva, Hitachi, ISR, Ulvac, Seiko Electronics, and Ulvac-HI. Foreign vendors include Varian and VG Semicon.

Metalorganic Chemical Vapor Deposition

MOCVD is a vapor-phase technique most commonly used to deposit Group III-V compound semiconductor epitaxial films onto III-V wafer substrates. Typical epitaxial films include compound semiconductors such as GaAs, aluminum GaAs (AlGaAs), indium phosphide (InP), and indium gallium arsenide phosphide (InGaAsP). Substrates include GaAs and indium arsenide (InAs) wafers. MOCVD can also be used to grow Group II-VI compounds such as mercuric cadmium telluride (HgCdTe). Most films and devices listed in Tables 1 and 2 for MBE can also be fabricated by MOCVD, but MOCVD is used primarily for III-V films and devices. Common reactants used in III-V epitaxy are shown in Table 2.

Table 1

Metals and Compound Semiconductor Films Deposited via MBE

Metal	Semiconductors
Aluminum	Group II-VI
Tungsten	CdTe, CdS, ZnTe, ZnSe, HgCdTe
Molybdenum	Group IV-VI
Gold	PbTe, PbSe, PbSnTe, PbSnSe
Platinum	Group IV
Titanium	Si, Ge, SiGe
Cobalt silicide	Group III-V
Nickel silicide	GaAs, AlGaAs, GaP, AlAs, GaAsP, GaSb, GaSbAs, InP, InGaAs, InSb, InAs, InGaP, InAlAs, InGaAsP, InGaAlAs

Source: Varian
Dataquest
May 1988

Table 2

Common Reactants Used in Group III–V MOCVD Epitaxy

Group III Sources	Group V Sources
Gallium Sources	**Arsenic Sources**
Trimethylgallium (TMGa)	Arsine
Triethylgallium (TEGa)	Trimethlarsenic
Triisobutylgallium	Triethylarsenic
Aluminum Sources	**Phosphorus Sources**
Trimethylaluminum (TMAl)	Phosphine
Triethylaluminum (TEAl)	
Dimethylaluminum	
Indium Sources	
Trimethylindium (TMIn)	
Triethylindium (TEIn)	
Dimethylethylindium	
Diethylmethylindium	

n-Type Dopant Sources	p-Type Dopant Sources
Silane	Dimethylzinc
Disilane	Diethylzinc
Trimethylsilane	Bis (cyclopentadienyl) magnesium
Hexamethyldesilane	Bis (methylcyclopentadienyl) magnesium
Hydrogen selenide	Diethylberyllium
Tetraethyltin	Dimethylcadmium

Source: Solid State Technology
Dataquest
May 1988

MOCVD systems are classified as R&D and production systems, depending on their wafer throughput. Low-throughput MOCVD systems are used as alternatives to MBE for advanced-compound semiconductor device R&D. Higher-throughput MOCVD systems are used to fabricate optoelectronic devices. MOCVD systems reportedly are capable of processing up to 200,000 LEDs or 500,000 semiconductor lasers per day.

Major Japanese MOCVD vendors are Nippon EMC, Nippon Sanso, Samco International, TEL Sagami, Ulvac, and others. Foreign companies include Crystal Specialties Inc. (CSI) and Fuji Cambridge.

Metalorganic Molecular Beam Epitaxy

Recently, MOMBE, a new silicon growth technology that combines both MOCVD and MBE technologies was developed. Table 3 compares the relative merits of MOMBE with those of MBE and MOCVD. MOCVD and MBE vendors are currently involved in joint development of MOMBE.

Table 3

Comparison of Epitaxial Growth Technologies

	MBE	MOCVD	MOMBE
Growth Speed	1.10 A/sec	1.333 A/sec	1.0 A/sec
Growth Temperature			
Gallium Arsenide	450-800°C	500-850°C	550-750°C
Silicon	400-900°C	N/A	N/A
Selected Epitaxial	Available	Available	Available
Wafer Surface Inspection Technology	Available	Not available	Available

N/A = Not Available

Source: Dataquest
May 1988

COMMERCIAL DEVICE APPLICATIONS

MOCVD and MBE are strategic technologies because of their use in fabricating advanced optoelectronic, microwave, and digital components. Optoelectronic devices include LEDs, solar cells, photodetectors, and solid-state lasers. Advanced microwave and digital devices include diodes, hot electron transistors (HETs), field-effect transistors (FETs), HEMTs, and heterojunction bipolar transistors (HBTs).

Optoelectronic devices are used as light emitters and detectors in fiber-optic communications systems, military infrared imaging systems and night-vision systems, consumer electronics such as compact disc players, and optoelectronic switching chips.

Microwave and digital device applications include electronic warfare equipment, commercial satellite earth stations, electronic test equipment used for measuring high-frequency signals, and advanced supercomputers. High-lattice mismatched heteroepitaxy (H2M), which is produced by layering GaAs on silicon wafers, may be used for supercomputer devices in the near future.

Recently, consumer use of HEMT increased sharply since NHK began 24-hour broadcasting using a direct broadcasting satellite (DBS). Major HEMT makers plan to increase production toward the end of 1988. Fujitsu, the developer of HEMT, is increasing production for consumer use, while NEC is boosting production by four to five times. Mitsubishi and Sony are also entering the market.

Table 4 shows the main applications for MOCVD and MBE, by company. Dataquest observes that major semiconductor users, such as Fujitsu, Matsushita, Mitsubishi, and Oki Electric, are using MOCVD for a variety of GaAs HEMTs, ICs, and LEDs. Eight device makers already have introduced MBE equipment.

Table 4

Main Applications of MOCVD and MBE by Company

Company	Technology MOCVD	Technology MBE	Main Application
Fujitsu	X	X	HEMT
Furukawa Denko	X		Laser diode
Hamamatsu Photonics	X		GaAs LED, AlGaAs LED
Kyocera	X		LED
Matsushita	X	X	GaAs IC
Mitsubishi	X	X	Photo device
Mitsubishi Metal	X		GaAs Epitaxial wafer
NTT	X	X	FET
Oki	X	X	GaAs IC power FET, LCD
Rohm		X	Laser diode (LD)
Sharp	X	X	LD
Sony	X		LD
Toshiba	X	X	LED, LD

Source: Dataquest
May 1988

EQUIPMENT MARKET ESTIMATES

The Japanese markets for MOCVD and MBE equipment have grown modestly during the last five years. As shown in Table 5, both markets grew until 1986, but MOCVD sales dropped 14.6 percent in yen value during 1987 because of a 1.2 percent drop in overall optoelectronic device sales and a 4.6 percent decline in discretes sales. MBE sales grew by 6.8 percent in 1987. Dataquest observes the following other major shifts in these equipment markets:

- The Japanese share of the domestic MOCVD and MBE markets jumped from 38.3 percent (in value) in 1983 to 62.9 percent in 1987.
- The Japanese MOCVD market grew at a 13.8 percent CAGR (in value) during the last five years, while foreign MOCVD market share jumped from 0 in 1983 to 10.3 percent in 1987.
- In contrast, foreign share of the larger but slower-growing MBE market declined from 83.4 percent in 1983 to 49.3 percent in 1987.
- Although the MBE market is growing slowly (6.8 percent CAGR), the Japanese MBE share grew at a phenomenal 44.0 percent CAGR (in value) from 1983 to 1987.
- Japanese vendors did not export any MOCVD or MBE equipment during the five-year period.

Table 5

Estimated Japanese MOCVD and MBE Equipment Shipments (Number of Units and Millions of Yen)

	1983		1984		1985		1986		1987		CAGR 1983-1987	
	Units	Value	Units	Value	Units	Value	Units	Value	Units	Value	Units	Value
Domestic												
MOCVD												
Japanese	23	¥1,270	37	¥2,190	43	¥2,470	40	¥2,350	33	¥1,910	9.4%	10.7%
Imported	0	0	0	0	2	150	2	145	3	220	0	0
MOCVD Total	23	¥1,270	37	¥2,190	45	¥2,620	42	¥2,495	36	¥2,130	11.9%	13.8%
MBE												
Japanese	7	¥ 600	12	¥1,400	22	¥2,680	18	¥2,840	18	¥2,380	26.6%	41.1%
Imported	18	3,010	18	3,010	7	1,200	9	1,550	14	2,310	3.9%	(6.4%)
MBE Total	25	¥3,610	30	¥4,410	29	¥3,880	27	¥4,390	32	¥4,690	6.4%	(6.8%)
Total	48	¥4,880	67	¥6,600	74	¥6,500	69	¥6,885	68	¥6,820	8.3%	8.7%
Exchange Rate (¥ per US$1)	240		237		250		167		144			

Source: Dataquest
May 1988

Dataquest believes that Japanese vendors are making tremendous strides in MBE technology and sales because of the growing optoelectronics shipments, which nearly doubled from ¥95.1 billion ($404 million) in 1983 to ¥134.5 billion ($805 million) in 1986.

However, as shown in Table 6, Dataquest forecasts moderate consumption of optoelectronic and discrete devices through 1991, which will slow MOCVD and MBE sales.

Table 6

Estimated Japanese Optoelectronic and Discrete Markets
(Billions of Yen)

	1987	1988	1989	1990	CAGR 1987-1990
Discrete	¥343.3	¥392.4	¥385.8	¥414.4	6.5%
Optoelectronic	118.7	143.0	140.2	157.9	9.9%
Total	¥462.0	¥535.4	¥526.0	¥572.3	7.4%
Billions of Dollars*	$3.2	$3.8	$3.7	$4.0	7.6%

*Exchange rate: ¥144 = $1.

Source: Dataquest
May 1988

THE MOCVD MARKET

As shown in Table 7, Japanese equipment makers totally dominated the MOCVD market until 1985, when foreign makers entered the market. Japanese vendors' shares then declined to 89.7 percent in 1987. Despite their revenue growth, Nippon EMC and TEL Sagami lost market share. Third-ranking Samco International fell to sixth place. However, the top two makers in 1983—Nippon Sanso and TEL Sagami—increased their combined share from 51.1 percent (in value) in 1983 to 58.6 percent in 1987, while Ulvac's share jumped to 18.3 percent. Newcomers Crystal Specialties Inc. and Ulvac collectively more than doubled their share from 15.7 percent to 36.2 percent during the same period.

Dataquest observes the following trends among the major players:

- Nippon EMC is a spinoff of TEL Sagami, whose engineers developed Nippon EMC's MOCVD technology. The company's sales grew at a moderate 7.5 percent CAGR between 1983 and 1987, and the company had 9.4 percent market share in 1987.

- Nippon Sanso is the top maker in the MOCVD business. After developing its equipment with Professor Masayoshi Umeno of Nagoya Industrial University in 1982, Nippon Sanso increased its market share from 19.7 percent in 1983 to 32.9 percent in 1987. Nippon Sanso's strength is threefold: its sales of R&D equipment; its total-system approach to integrating gases, materials, and equipment; and its manufacturing equipment sales through Spire.

- Samco International has developed MOCVD equipment for R&D purposes and has targeted university and corporate research centers. Its market share has dropped from 15.7 percent in 1983 to 8.4 percent in 1987 due to the faster growth of production MOCVD shipments.

- Ulvac is becoming a major player in the MOCVD market, with its shipments soaring from ¥50 million ($208,000) in 1983 to ¥350 million ($2.4 million) in 1987. The company specializes in thin-film growth technology and is developing MOMBE technology.

- TEL Sagami (formerly TEL Thermco) held a 19.7 percent share of the Japanese MOCVD market in 1987 and is leveraging its CVD technology into the MOCVD field. Its sales division, which is located in the GaAs division, has been active, but TEL Sagami's MOCVD shipments have increased in value at only a 1.2 percent CAGR since 1983.

- Fuji Cambridge, a joint venture between Fuji Electric and Cambridge Instruments, entered the market in 1985 when it successfully installed its equipment at Mitsubishi. However, it has had limited success; in 1987, the company sold no systems in Japan.

- Crystal Specialties Inc. (CSI) revenue has grown rapidly, capturing a 10.3 percent share of the market in 1987, because of Sumisho Electronic Systems, CSI's Japanese sales agent.

- Other MOCVD vendors include Seidensha Electronics, Shimazu Company, SPC Electronics, Toyoko Kagaku Ltd., and Yamato Semiconductor Equipment.

Table 7

Estimated MOCVD Shipments in Japan (Units and Millions of Yen)

	1983		1984		1985		1986		1987		CAGR (Value)
	Units	Value	Units	Value	Units	Value	Units	Value	Units	Value	1983-1987
Domestic Company											
Nippon EMC	3	¥ 150	4	¥ 200	5	¥ 250	5	¥ 250	4	¥ 200	7.5%
Nippon Sanso	3	250	7	550	12	850	11	770	10	700	29.4%
Samco International	4	200	5	250	4	160	4	160	4	160	(5.4%)
TEL Sagami	8	400	9	540	9	540	7	500	6	420	1.2%
Ulvac	1	50	7	350	9	450	9	450	7	350	62.7%
Others	4	220	5	300	4	220	4	220	2	80	(22.3%)
Total	23	¥1,270	37	¥2,190	43	¥2,470	40	¥2,350	33	¥1,910	10.7%
Non-Japanese Company											
CSI	0	0	0	0	1	80	1	80	3	220	0
Fuji Cambridge	0	0	0	0	1	70	1	65	0	0	0
Total	0	0	0	0	2	¥ 150	2	¥ 145	3	¥ 220	0
MOCVD Total	23	¥1,270	37	¥2,190	45	¥2,620	42	¥2,495	36	¥2,130	13.8%
Exchange Rate (¥ per US$1)	240		237		250		167		144		

Source: Dataquest
May 1988

THE MBE MARKET

As shown in Table 8, shipments of MBE equipment have grown at a 6.8 percent CAGR since 1983. While imports have dropped, Japanese vendors' combined share has jumped from 16.6 percent in 1983 to 50.7 percent in 1987. Leading players are Anelva, VG Semicon (distributor is Marubun), Varian (distributor is Tokyo Electron Ltd.), and Ulvac, respectively. The following is a summary of three Japanese vendors' activities:

- Anelva developed its MBE equipment, using its thin-film growth technology, which offers much higher value-added results and resolution than its MOCVD technology. Anelva is the leader with 29.9 percent of the market in 1987.
- Hitachi has tested its MBE equipment for internal use but has not sold any equipment yet.
- Seiko Electronic developed its MBE equipment for in-house compound semiconductor R&D and entered the market in 1985. The company had only 3.4 percent market share in 1987, so it is strengthening its sales support.
- Other Japanese vendors include Echo Engineering and Japan Vitec.

Table 8

Estimated MBE Shipments in Japan
(Units and Millions of Yen)

	1983		1984		1985		1986		1987		CAGR (Value)
	Units	Value	Units	Value	Units	Value	Units	Value	Units	Value	1983-1987
Domestic Company											
Anelva	3	¥ 300	5	¥ 600	12	¥1,500	8	¥1,200	10	¥1,400	47.0%
Hitachi	0	0	0	0	0	0	0	0	0	0	0
Seiko Electronic	0	0	0	0	1	180	2	340	1	180	0
Ulvac	4	300	7	800	9	1,000	8	1,300	7	800	27.8%
Ulvac-HI	0	0	0	0	0	0	0	0	0	0	0
Total	7	¥ 600	12	¥1,400	22	¥2,680	18	¥2,840	18	¥2,380	41.1%
Non-Japanese Company											
ISR	10	¥1,600	10	¥1,600	2	¥ 320	3	¥ 460	3	¥ 460	(26.8%)
Varian	3	540	3	540	1	180	2	350	5	850	12.0%
VG Semicon	5	870	5	870	4	700	4	740	6	1,000	3.5%
Total	18	¥3,010	18	¥3,010	7	¥1,200	9	¥1,550	14	¥2,310	(6.4%)
MBE Total	25	¥3,610	30	¥4,410	29	¥3,880	27	¥4,390	32	¥4,690	6.8%

Source: Dataquest
May 1988

DATAQUEST CONCLUSIONS

Dataquest anticipates moderate growth in the MOCVD and MBE equipment markets because of the increasing use of optoelectronic, microwave, and ultrafast digital devices. Our conclusions are based on the following observations:

- Existing equipment is used mostly for R&D, but Japanese makers are introducing MOCVD and MBE equipment on production lines. For example, Sony recently introduced an MOCVD machine, and Rohm has purchased an MBE machine.

- MOMBE equipment is being developed and eventually will be introduced on production lines.

- MOCVD and MBE are being introduced on production lines because of their use in H2M for GaAs–based optoelectronic ICs (OEICs).

Despite the short–term slowdown in MOCVD and MBE sales, we believe that these new applications will lead to moderate shipment growth and attract new equipment makers to this field.

Joe Grenier
Kaz Hayashi
Sheridan Tatsuno

Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987–1988 Newsletters: May 1988–14

CD AND WAFER INSPECTION EQUIPMENT MARKETS: AN INDUSTRY OVERVIEW

INTRODUCTION

Dataquest recently completed an analysis of the worldwide critical dimension (CD) and wafer inspection equipment markets. This analysis focused on three specific categories of equipment: optical CD tools, which include automated linewidth and overlay measurement equipment; wafer inspection stations that are used for detecting process-related defects; and joint CD/inspection systems that combine CD measurement capability with wafer inspection. All three types of equipment are based on microscope stations that, in the past, have relied upon operators to perform measurement and inspection tasks. In today's semiconductor industry, line geometries are shrinking, while device complexity, processing steps, wafer size, and mask levels continue to increase. These equipment markets have undergone significant changes in the last few years, as new systems for fully automated measurement and inspection operations have been introduced to meet the needs of future device fabrication.

This newsletter provides an overview of the CD and wafer inspection equipment categories, companies, and world markets. For a more complete discussion of this topic, please refer to the "CD and Wafer Inspection Equipment Markets" service section in the SEMS Markets and Technology binder.

MARKET SUMMARY

In 1987, the world market for CD and wafer inspection equipment was $94.0 million, of which $39.5 million (42.1 percent) was for optical CD equipment, $24.5 million (26.1 percent) for wafer inspection stations, and $29.9 million (31.8 percent) for systems that combine both measurement and inspection capabilities on the same tool. Table 1 presents the worldwide markets for optical CD equipment, wafer inspection stations, and joint CD/inspection systems for 1982 through 1987.

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398 / (408) 437-8000 / Telex 171973 / Fax (408) 437-0292

Table 1

Worldwide Markets for CD and Wafer Inspection Equipment, 1982–1987 (Millions of Dollars)

	1982	1983	1984	1985	1986	1987	CAGR 1982-1987
Optical CD Equipment	$13.4	$22.5	$32.6	$20.1	$28.7	$39.5	24.1%
Wafer Inspection Stations	11.4	16.7	27.1	20.5	21.8	24.5	16.5%
Joint CD/Inspection Systems	0.0	0.7	3.1	13.9	20.3	29.9	155.6%*
Total	$24.9	$40.0	$62.8	$54.4	$70.7	$94.0	30.5%
Growth		54%	72%	(21%)	30%	33%	

Note: Numbers may not add to totals shown due to rounding.
*CAGR for joint CD/inspection systems is taken from 1983 through 1987.

Source: Dataquest
May 1988

All three market segments exhibited moderate to healthy dollar growth in 1986 and 1987. The emerging market segment of joint CD/inspection systems has been dominated by the presence of KLA Instruments and its 2020 system, priced at close to $1 million. This system has received attention not only for its price tag, but for its fully automated measurement and defect detection capabilities as well. Semiconductor manufacturers in the United States, Japan, and Europe are exploring the applications and economics of these costly joint CD/inspection systems. In the meantime, other equipment companies are developing and introducing new products for this emerging market segment.

Growth, however, in the market segments of optical CD equipment and wafer inspection stations seems contrary to the mood and general business climate of the semiconductor equipment industry during the recession years. In part, the growth in these markets during 1986 and 1987 can be attributed to currency appreciation, in particular in the wafer inspection equipment category. However, a far more significant factor affecting all regions of the world has been the increase in the average selling price (ASP) of equipment over the last several years. This is because new measurement and inspection technologies have been developed to keep pace with the shrinking geometries of integrated circuits. Thus, it is no surprise that dollar growth in 1986 and 1987 is directly attributable to those companies offering advanced technology products with improved automation capability for submicron measurement and inspection.

COMPANY ACTIVITIES

Table 2 contains a list of companies active in the CD and wafer inspection equipment markets. This list, organized by region in which company headquarters are based, summarizes company products by equipment category: optical and e-beam-based CD equipment, wafer inspection stations, reticle qualification systems (used during setup and process qualification of lithography equipment when a mask or reticle is changed), and joint CD/inspection systems. While not the primary focus of our market analysis, the categories of e-beam-based CD equipment and reticle qualification systems are included in Table 2 because they represent competitive, and in some cases, complementary technologies and products. In addition to listing new product developments and announcements, Table 2 identifies four companies that are no longer active in these market segments.

Table 2

CD and Wafer Inspection Equipment Companies by Product Category

	CD Optical	CD e-Beam	Wafer Inspect	Reticle Qualification	Joint CD/Inspect
U.S. Companies					
Amray		X			
Estek (Aeronca)			X		
Insystems			X		
ITP Incorporated	X				
IVS Inc.	X		U/D		
KLA Instruments	X, N/P	X	X	X	X
Nanometrics	X	X			
Opal Inc.		N/P			U/D
Optical Specialties, Inc.	X		X		X
Reichert-McBain*	X				
SiSCAN Systems	X				
Waterloo Scientific	N/P				
Japanese Companies					
ABT (Akashi Beam Technology)		X			
Canon			X		
Dainippon Screen	N/P				
Hitachi	X	X			
Holon		X			
JEOL		X			
Lasertec				X	
Nidek	N/P		X		
Nikon	X		X		
Ryokosha	X				
Sony				X	

(Continued)

Table 2 (Continued)

CD and Wafer Inspection Equipment Companies
by Product Category

	CD Optical	CD e-Beam	Wafer Inspect	Reticle Qualification	Joint CD/Inspect
European Companies					
Bio-Rad Lasersharp Ltd.	X				
Cambridge Instruments	X	X		X	
Heidelberg Instruments	X		U/D		
Vickers Instruments	X	X			
Wild Leitz	X		X		
Zeiss			X		
Departures					
Contrex					X
Machine Intelligence					X
Optoscan	X				
Karl Suss			X		

N/P = New product announcement
U/D = Equipment currently under development
*Acquisition by Optical Specialties, Inc., from Cambridge Instruments announced in December 1987

Source: Dataquest
May 1988

(Note: Prometrix, a manufacturer of linewidth measurement systems based on electrical probing techniques, is not listed in Table 2 because its equipment does not fall into any of the identified product categories.)

OPTICAL CRITICAL DIMENSION EQUIPMENT

A critical dimension of a semiconductor device refers to a line, element, or feature that must be manufactured and controlled to very tight specifications. A CD can refer to the dimension of a linewidth in a device pattern at a given mask level, as well as to a measure of the allowable tolerance in the overlay of patterns from multiple mask levels. Typically, CD measurement systems available today perform both linewidth and overlay measurements.

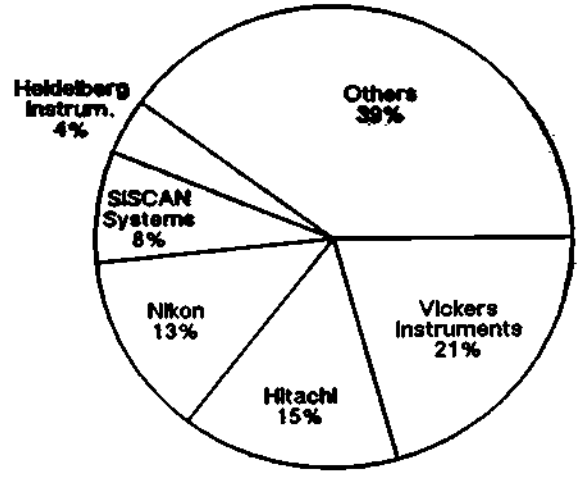
Over the last several years, the field of CD measurement has become diversified into a multitude of technologies in response to the need for submicron measurement capability. Conventional CD tools have been based on white-light microscopy systems. Today, however, this equipment is enhanced with fluorescent measurement capability and image-processing systems. In addition, laser-based measurement systems, confocal scanning laser microscopy, and coherence probe imaging technologies have been developed to perform submicron measurements. Scanning electron microscope (SEM) tools, traditionally relegated to the analytical lab, have been redesigned to meet the needs of submicron manufacturing in a production environment and are now beginning to emerge as alternatives to optical-based systems in the fab.

Market Summary

In 1987, the worldwide market for optical CD equipment was $39.5 million, up 38 percent from the 1986 level of $28.7 million. Figure 1 summarizes the world market share for the top five companies within this equipment segment in 1987.

Figure 1

1987 Optical CD Equipment Company Market Share



$39.5 Million

Source: Dataquest May 1988

Vickers Instruments of the United Kingdom ranked first in the optical CD equipment market, with the successful introduction of its new automatic CD measurement system, the Quaestor CD–07A. Hitachi, with its LAMU measurement system and Nikon, with its LAMPAS tools, ranked second and third, respectively, in the world market. Together these three companies had a combined share of 49 percent. In addition, the new confocal scanning laser microscopy systems of Heidelberg Instruments and SiSCAN Systems captured a combined share of 12 percent of the 1987 market. All five companies have introduced new systems within the last two years, and Dataquest believes that their success in the marketplace reflects new technology implementations and advanced automation capability. The prices of the CD measurement systems of these five companies range from $230,000 to $420,000, substantially higher than $115,000, the ASP across all equipment models in this market segment in 1987.

WAFER INSPECTION STATIONS

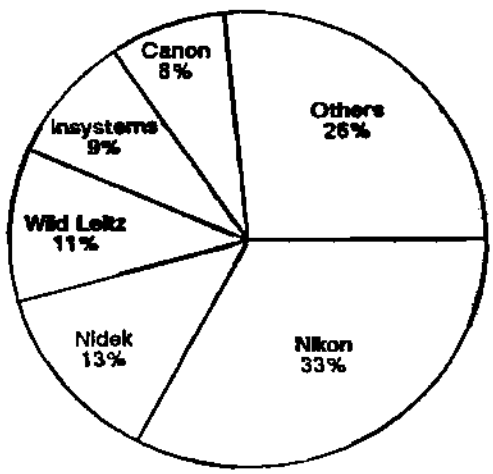
Wafer inspection refers to the inspection of patterned wafers for process defects by visual and image–processing techniques. Traditionally, this equipment has been designed as a microscope station at which an operator visually inspects wafers under magnification for the presence of defects, which range from contaminating particles to defective circuit patterns. As wafer inspection tools have matured, additional features have been added, including automatic wafer handling, automatic and programmable stage movement, autoalignment, autofocus, and keypad data entry systems. In conventional wafer inspection systems today, almost everything but human vision is automated. Recently, a new generation of automatic wafer inspection stations was introduced. These sophisticated systems utilize holographic spatial frequency filtering technology and advanced image–processing techniques to perform automatic defect detection. In some instances, wafer inspection systems assist in defect classification as well.

Market Summary

In 1987, the worldwide market for wafer inspection stations was $24.5 million, up 13 percent from the 1986 level of $21.8 million. Figure 2 summarizes world market share for the top five companies within this equipment segment in 1987.

Figure 2

1987 Wafer Inspection Company Market Shares



$24.5 Million

Source: Dataquest
May 1988

Nikon, with its Optistation systems, had the largest share of the 1987 worldwide wafer inspection market, with 33 percent of the $24.5 million market. Nidek, Wild Leitz, and Canon together had an additional 32 percent. All four companies manufacture microscope-based inspection stations that rely on operators to detect and classify defects on the wafer surface. Insystems, with its new system based on holographic, spatial frequency filtering technology, captured 9 percent of the world market with sales of $2.1 million in 1987. This system provides fully automatic detection of an entire wafer in less than 30 minutes. While the traditional microscope inspection stations are priced at approximately $60,000 to $70,000, the automatic wafer inspection system from Insystems is $1 million.

JOINT CD/INSPECTION SYSTEMS

Over the last several years, a new category of measurement and inspection equipment has emerged—systems that are designed for both CD measurement and inspection capability. Dataquest refers to this category of equipment as joint CD/inspection systems. In 1983, Optical Specialties, Inc., introduced the first system designed as a microscope-based inspection station with automatic CD measurement capability. An operator, however, was still required to perform defect detection and classification. In 1984, KLA Instruments introduced its 2020 system, a tool that combines automatic CD measurement with automatic defect detection capability. For the first time, the subjective judgement of the operator was removed from the wafer inspection process. The KLA 2020 heralded the beginning of a new era in advanced measurement and image-processing technologies for the semiconductor industry.

Market Summary

In 1987, KLA Instruments had a 92.3 percent share of the world market of $29.9 million for joint CD/inspection equipment. This category of equipment has been dominated strongly by KLA Instruments since it started to ship its 2020 system in 1985. Over the last several years, the ASP of joint CD/inspection systems has skyrocketed, while unit demand has remained relatively constant. The increasing ASP of joint CD/inspection systems reflects the acceptance of KLA's 2020 system in the marketplace. The 2020 is priced at $895,000, which is substantially higher than the $77,000 ASP of joint CD/inspection systems in 1983.

FORECAST

Table 3 presents Dataquest's forecast for the markets of optical CD equipment, wafer inspection stations, and joint CD/inspection systems from 1988 through 1992. Sales of optical CD equipment, wafer inspection stations, and joint CD/inspection systems are expected to reach $325 million in 1992. In particular, the emerging market for joint CD/inspection systems is anticipated to experience strong growth at a CAGR of 32.5 percent, reflecting a trend in the industry for multiple functionality and integrated applications on a single piece of capital equipment.

Table 3

Forecast
Optical CD Equipment, Wafer Inspection Stations, and Joint/CD Inspection Systems, 1987–1992
(Millions of Dollars)

	Actual 1987	1988	1989	1990	1991	1992	CAGR 1987-1992
Optical CD Equipment	$39.5	$ 53	$ 61	$ 77	$ 99	$127	26.3%
Wafer Inspection Stations	24.5	36	41	50	62	76	25.4%
Joint CD/Inspection Systems	29.9	42	51	67	90	122	32.5%
Total	$94.0	$131	$153	$194	$251	$325	28.2%
Growth		39%	17%	27%	29%	29%	

Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
May 1988

The optical CD equipment market is forecast to grow at a 26.3 percent CAGR. This will be driven by the acceptance of new technologies for submicron measurement. At this time, however, no measurement technology has emerged as a clear leader. Over the next several years, SEM–based CD tools for the production environment will also emerge as significant competition for optical systems in the submicron measurement range.

Wafer inspection stations are expected to experience growth of 25.4 percent, or sales of $76 million, in 1992. Dataquest expects most of the growth within the category of wafer inspection stations to come from advanced image–processing systems that rely on software algorithms or innovative technology–based defect detection. In many cases, this capability, combined with critical dimension measurement, will be available in a joint CD/inspection system.

Manufacturing automation programs in the semiconductor industry will also be an important factor fueling growth in these equipment segments. CD and wafer inspection equipment is used in the production environment to provide data, analysis, and feedback on equipment operation and the manufacturing process. The ability to acquire, measure, and analyze information in a timely manner becomes essential as the semiconductor industry enters a new manufacturing phase in which attention is being focused on the automation of the manufacturing processes. While total or "lights–out" factory automation in the semiconductor industry is still years away, automated CD and wafer inspection systems are fundamental components of manufacturing strategy today and will be necessary if lights–out automation is to be achieved in the future.

Peggy Marie Wood

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Research *Bulletin*

SEMS Code: 1987–1988 Newsletters: May 1988–13

CAPITAL SPENDING IN UNITED STATES AND JAPAN BOUNDS FORWARD

CAPITAL SPENDING SURVEY RESULTS

Dataquest surveys the major semiconductor companies in Japan and the United States twice a year to determine their capital spending plans. The results of the first survey are in: Spending by Japanese companies will be up by 44 percent in yen and 52 percent in dollars. Spending by United States companies will increase by 46 percent. (See Tables 1 and 2.) The higher percentage increase in yen is due to the continued appreciation of the yen relative to the dollar. Mitsubishi will have the largest percentage growth in yen (157 percent) followed by NEC (67 percent). However, in absolute terms, Toshiba is by far the biggest spender in Japan at $615 million, followed by NEC with $385 million.

Table 1

Change in Worldwide Japanese Company Capital Spending
(Billions of Yen; Millions of Dollars)

Company	1987	1988	Percent Change	1987	1988	Percent Change
Fujitsu	¥ 20	¥ 32	60%	$ 139	$ 246	77%
Hitachi	30	50	67%	208	385	85%
Matsushita	22	27	23%	153	208	36%
Mitsubishi	7	18	157%	49	138	185%
NEC	30	50	67%	208	385	85%
Oki	25	37	48%	174	285	64%
Sanyo	25	29	16%	174	223	28%
Sharp	20	26	30%	139	200	44%
Toshiba	60	80	33%	417	615	48%
Others	72	98	36%	498	758	52%
Total	¥311	¥447	44%	$2,158	$3,442	52%
Exchange Rate (Yen per US$1)				144	130	

Source: Dataquest May 1988

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 437-8000, Telex 171973, Fax (408) 437-0292

Table 2

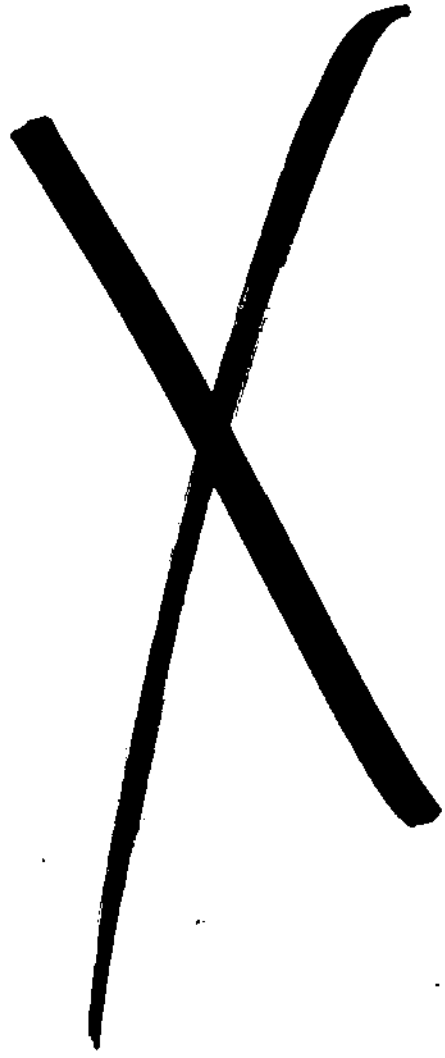
U.S. Capital Spending
(Millions of Dollars)

Company	1987	1988	Percent Change
AMD	$ 138	$ 175	27%
Analog Devices	50	50	0
Fairchild	45	-	-
General Electric	45	50	11%
General Instrument	12	20	67%
Harris	30	30	0
IDT	18	37	103%
Intel	302	400	32%
LSI Logic	135	60	(56%)
Micron Technology	14	120	769%
Motorola	350	450	29%
National Semiconductor	112	180	60%
Sematech	-	140	-
Texas Instruments	231	360	56%
Others	352	476	35%
Total	$1,834	$2,548	39%

Source: Dataquest
May 1988

For United States companies, the largest percentage change will be registered by Micron Technology (769 percent) as the company increases its spending from $14 million to $120 million in order to construct a new DRAM facility in Boise. Motorola will spend more than any other company in the United States in 1988 ($450 million), followed by Intel ($400 million) and Texas Instruments ($360 million).

George Burns



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Research Newsletter

SEMS Code: 1987–1988 Newsletters: June
1988–19
0000477

ELECTRONICS INDUSTRY FORECAST: FROM END–USE EQUIPMENT TO CAPITAL SPENDING

SUMMARY

Probably one of the most frequent questions we are asked at Dataquest is "What is driving the semiconductor recovery, and how long will it last?" We have published several newsletters and other material that address various aspects of this question, which our clients have received. The purpose of this newsletter is to compile information that has already been published and present, in one newsletter, a very concise summary of the electronics industry as we see it for the next five years. Our intent is to provide a reference document to be used for high–level forecasts.

The newsletter presents top–level forecasts of the electronic equipment industry, the semiconductor production required to meet the electronic equipment demand, and the capital spending required by the semiconductor manufacturers to meet semiconductor demand.

ELECTRONIC EQUIPMENT

The electronics industry has gained clout as a major driving force behind the worldwide economy. Few are aware that in 1988 $770 billion worth of electronic equipment will be produced, creating direct demand for a $49 billion semiconductor market.

The electronics industry, made up of six major markets, will grow more than 12 percent this year. Figure 1 reflects the major factors behind that growth—the data processing and consumer markets. In the United States, Japan, and the Far Eastern countries, these two markets comprise the bulk of electronic equipment production. Major growth areas within these markets are personal computers, workstations, terminals, televisions, VCRs, and compact disk players. All of these areas have two points in common: high pervasiveness, meaning high semiconductor content, and high volume. All of the previously mentioned products are tied to individual use; that makes for a very large total available market.

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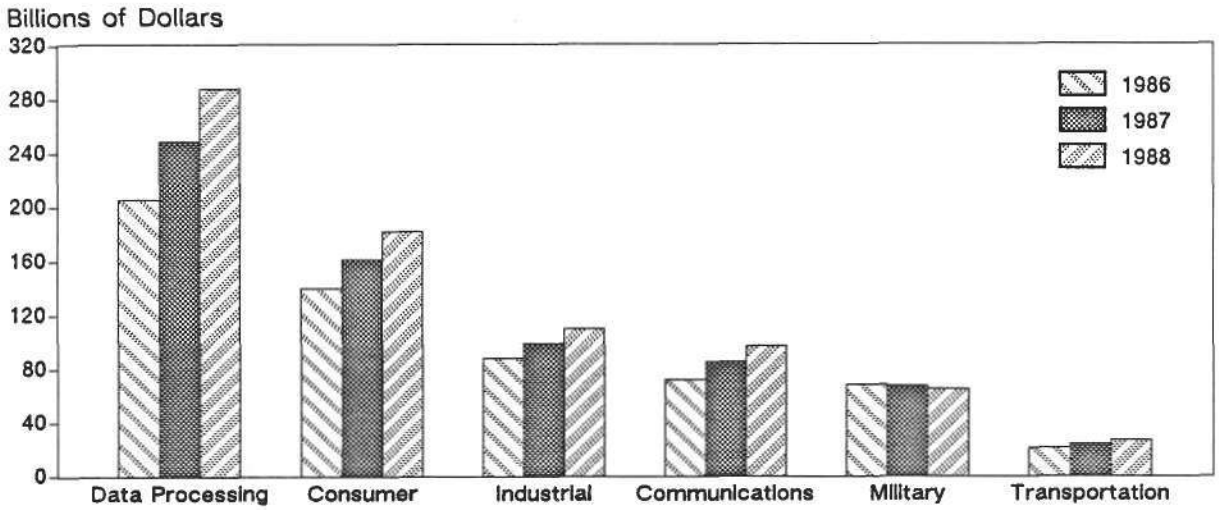
Figure 1

Worldwide Electronic Equipment Market by Electronics Segment



Source: Dataquest June 1988

Table 1 shows Dataquest's estimates for worldwide electronic equipment market. Solid state technology now affects all of us; our appliances, entertainment, transportation, telephones, and productivity tools rely on semiconductors. The commoditization of electronics and the semiconductor industry may ultimately create a more stable marketplace. Market demand is broad based, and marketing and manufacturing strategies are assessed across an international marketplace. Closer ties between users and vendors create implications for more stable growth. We believe that there will be less dramatic swings in the semiconductor industry, which will be largely due to a changing worldwide electronics industry.

Table 1

Worldwide Electronic Equipment Semiconductor Production and Capital Spending (Billions of Dollars)

	1986	1987	1988	1989	1990	1991	1992	CAGR 1986-1992
Electronic Equipment Market	$595.0	$685.0	$769.0	$819.0	$843.0	$968.0	$997.0	9.0%
Semiconductor Production	32.8	39.9	49.1	54.1	54.2	62.8	75.9	15.0%
Capital Spending	5.3	6.0	8.3	9.0	9.1	11.8	15.4	19.5%

Source: Dataquest June 1988

SEMICONDUCTOR PRODUCTION

Electronic equipment demand drives semiconductor production. Figure 2 shows the semiconductor consumption by electronic equipment segment. Here we see that the data processing and consumer electronics markets alone will consume almost $30 billion worth of chips in 1988; this represents more than 60 percent of all the chips produced in 1988. Table 1 shows Dataquest's latest estimates of worldwide semiconductor production by all producers, including captive and merchant.

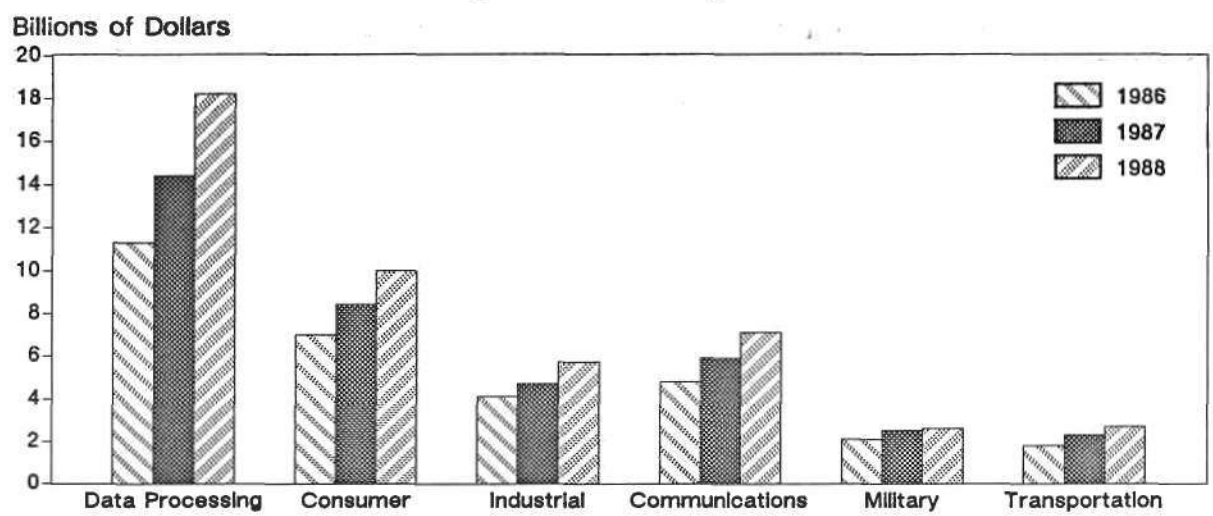
Semiconductor production in 1988 will increase by 23 percent over 1987 levels, which were up 22 percent over 1986 levels. The bookings momentum and the shortages in leading-edge semiconductor products suggest that strength in shipments should continue through the first half of 1989. Growth in 1989 should be 10 percent, followed by a flat 1990.

In spite of memory chip shortages, the short-term outlook is very strong because of the increasing demand for high-end microprocessors and ASIC devices that are consumed in the production of data processing equipment. Overall capacity utilization is estimated to be 82 percent by the end of 1988, up from 78 percent in 1987. Capacity is tight for the leading-edge products, with capacity utilization in excess of 90 percent for the finer-line geometries in the 1.5-micron range.

As new plants are brought on stream, capacity utilization for high-integration devices should ease a bit later this year. High-end microprocessors should soon cease to be supply limited, but microprocessor demand in 1988 is constrained by memory shortages. Although we expect DRAM demand to exceed supply in 1988, we expect supply to catch up in 1989 as a result of increased capacity and improved yields for 1Mb DRAMs, putting downward pressure on prices.

Figure 2

Worldwide Semiconductor Consumption by Electronics Segment

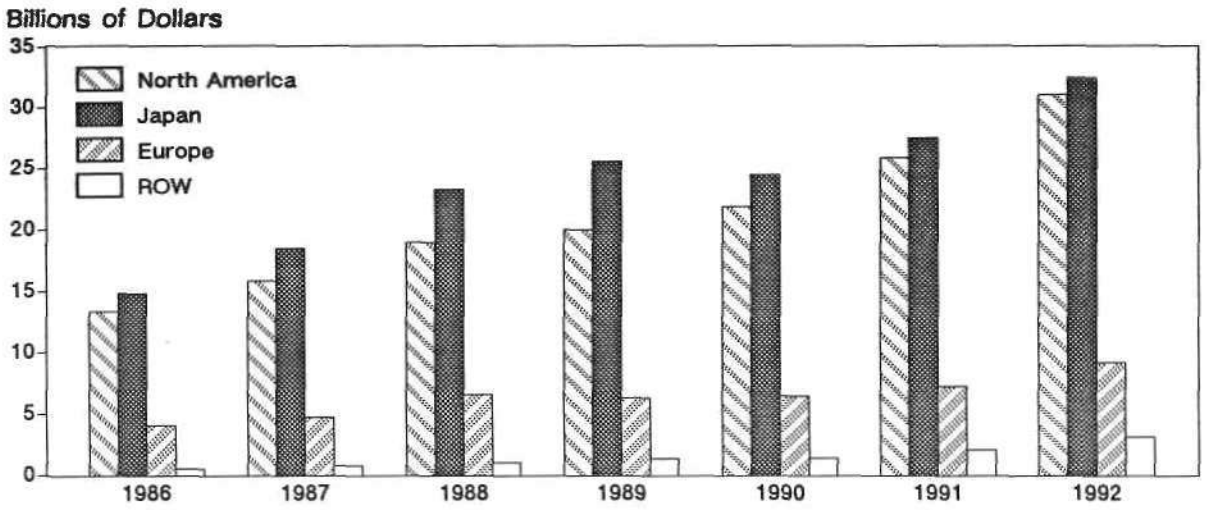


Source: Dataquest June 1988

Figure 3 shows the regional production of semiconductors, which includes production by all companies in the region, regardless of country location of headquarters. Table 2 shows the shift in regional production from 1984 through 1992. Here we see that for North America, in spite of the increase of Japanese and European fabs in the United States, its share of worldwide semiconductor production will only be about 41 percent by 1992.

Figure 3

Worldwide Semiconductor Production by Region



Source: Dataquest June 1988

Table 2

Worldwide Semiconductor Production by Region

	1984	1992
North America	49.8%	40.9%
Japan	38.3	42.8
Europe/ROW	11.9	16.3
Total	100.0%	100.0%

Source: Dataquest June 1988

CAPITAL SPENDING

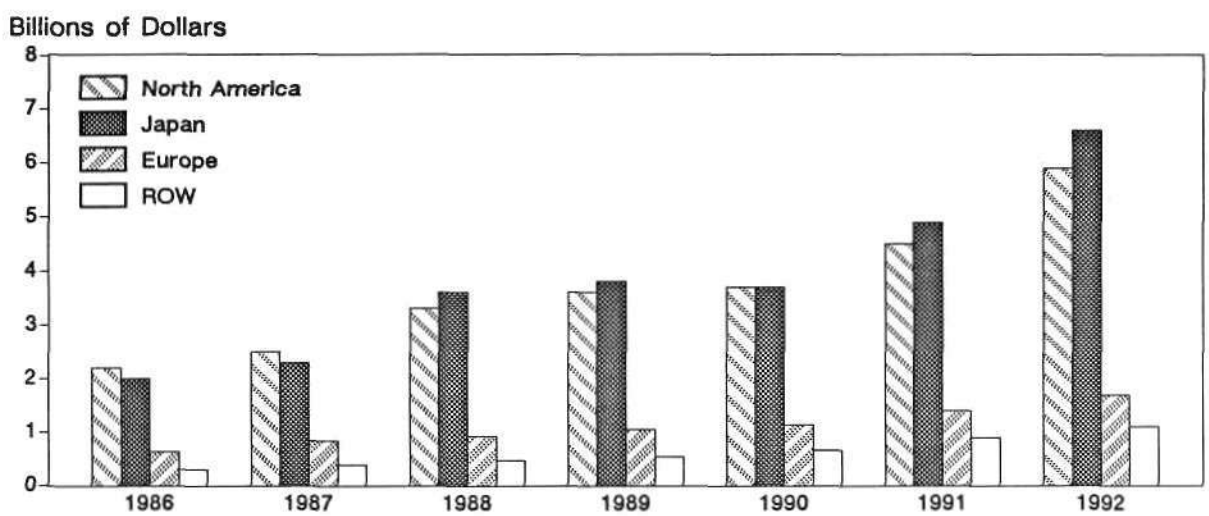
Table 1 also shows the capital spending that must be made by the world's semiconductor producers in order to meet the projected semiconductor demand. Capital spending will be driven by the need for increased capacity and upgrades, especially for leading-edge devices. Capital spending will also be fueled by competitive pressures as many manufacturers locate front-end facilities offshore to be close to their markets and to protect themselves from the double nemesis of trade friction and currency fluctuations.

Capital spending, like the electronics end markets that it eventually serves, will grow at a much more steady rate than in the past. Semiconductor manufacturers, although spending for more capacity, will remain cautious; they prefer to increase equipment availability and to increase yields before adding capacity. Consequently, although Dataquest does not anticipate the skyrocketing growth that occurred in 1984, we also do not anticipate the devastating descents that occurred in the 1985 to 1986 time frame. The peaks may not be as high, but the ride will be smoother and more sustainable.

Figure 4 shows the capital outlays by region that must be made to support the semiconductor output of those regions. Again, these projections represent spending by all companies in the region, regardless of the company nationality. We expect spending by all companies in Japan (including U.S. merchants and IBM) to increase at a CAGR of 24 percent. The reason for this high growth in Japan is the fairly low starting base, especially in terms of yen. Spending in yen by Japanese companies, U.S. companies, and IBM in Japan actually fell 65 percent from 1984 to 1987—from ¥924 billion in 1984 to ¥325 billion in 1987.

Figure 4

Worldwide Capital Spending by Region



Source: Dataquest June 1988

We also expect spending by all companies in the Asia–Pacific region to grow at a CAGR of 24 percent. This growth rate will be driven by Asia–Pacific companies' commitment to become world–class manufacturers and by new fab construction by European and North American companies.

Spending in North America will grow at a healthy 19 percent CAGR, and will be almost $6 billion in 1992. This spending will be fueled by new fabs and upgrades for leading–edge devices, especially DRAMs and microprocessors. Dataquest also anticipates a strong surge of spending by Japanese companies in the United States, as several Japanese companies either have already initiated new fab construction or are soon planning to begin.

Europe will experience the slowest growth rate—only 15 percent. The relatively slow rate in Europe is due to the recent completion of major expansions by Philips and Siemens and to the rationalization of existing facilities by SGS–Thomson. Captives will play a major role in Europe: AT&T will complete its new fab in Spain in 1989, and IBM will begin production on the largest 200mm fab in the world at Singlefingen, West Germany, also in 1989.

Capital spending, like the electronics industry it serves, will be more stable than it has been in the past. It will also be more international—and more competitive. Equipment vendors will have to serve markets that are culturally different from their home offices and compete with new competitors on their home turf. Capital spending may grow at a more stable rate than in the past, but competition will be as fierce as ever.

DATAQUEST CONCLUSIONS

The forecast presented here for the electronics industry—from end–use markets through capital spending—shows a consistent picture of healthy and sustainable growth rates. Furthermore, worldwide markets, increased dialog, just–in–time inventory control, and more realistic capacity planning are beginning to pay off for the electronics industry. The good growth rates, combined with a more mature business point of view, signify that the electronics industry is emerging from the vertigo of youth and should rationally grow to a $1 trillion level by 1992. That is, indeed, good news.

Joseph Borgia
George Burns
Joe Grenier
Anthea Stratigos

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Research Newsletter

SEMS Code: 1987–1988 Newsletters: June
1988–18
0000438

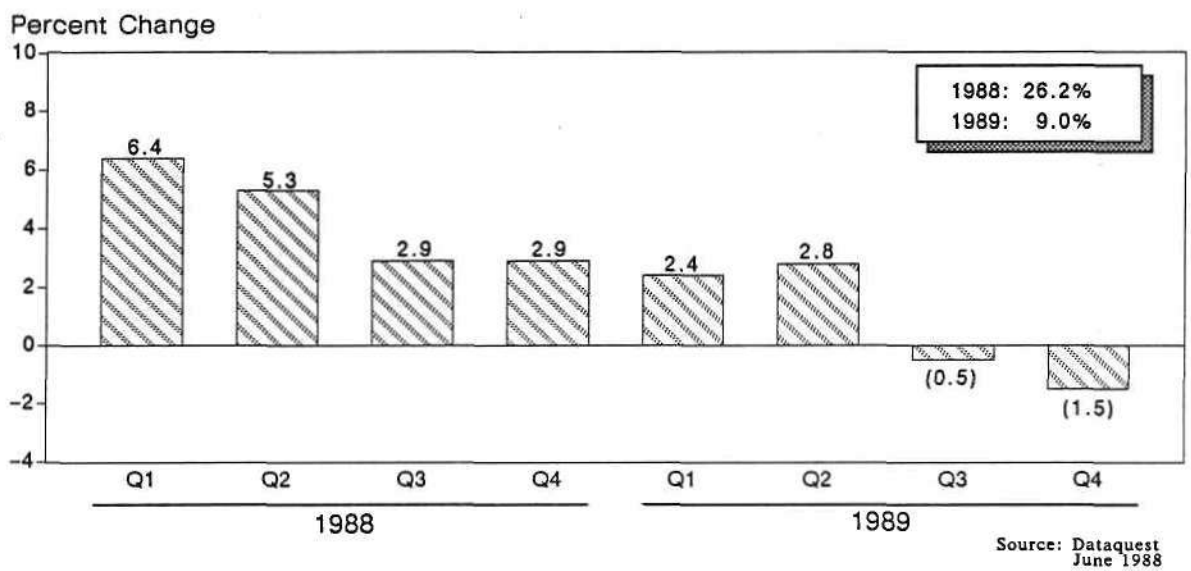
SEMICONDUCTOR RECOVERY GATHERS MOMENTUM

SUMMARY

The recovery in the worldwide semiconductor market should be stronger in 1988, as the Japanese and European markets continue to recover following the lead of the North American and Rest of World markets. Dataquest forecasts that the worldwide semiconductor market will grow 26 percent in 1988, stacked on top of the 23 percent growth in 1987. The bookings momentum and the shortages in leading-edge products suggest that the strength in shipments should continue through the first half of 1989. The Dataquest world semiconductor forecast is summarized in Figure 1 and Tables 1 and 2.

Figure 1

World Semiconductor Forecast



Source: Dataquest
June 1988

Table 1

Estimated World Semiconductor Market
(Billions of U.S. Dollars)

	1987	1988	1989	1990	1991	1992	CAGR 1987-1992
North America	11.9	14.7	15.6	15.2	18.0	22.3	13.5%
Japan	14.3	18.2	19.9	18.8	21.1	25.4	12.1%
Europe	6.4	7.6	8.1	8.3	9.2	10.4	10.3%
Rest of World	3.9	5.5	6.6	7.1	8.9	11.4	23.6%
Total World	36.5	46.0	50.2	49.4	57.2	69.5	13.8%

Table 2

Estimated World Semiconductor Market
(Percent Change, U.S. Dollars)

	1987	1988	1989	1990	1991	1992
North America	19%	24%	6%	(2%)	18%	24%
Japan	21%	27%	9%	(5%)	12%	21%
Europe	16%	20%	6%	2%	10%	13%
Rest of World	67%	39%	22%	7%	26%	28%
Total World	23%	26%	9%	(2%)	16%	22%

Source: Dataquest
June 1988

The short-term outlook is very strong, in spite of shortages in memory chips and increasing demand for high-end microprocessors and ASIC devices consumed in the production of data processing equipment. Overall capacity utilization is estimated to be 82 percent by the end of 1988, up from 78 percent in 1987. Capacity is tight for the leading-edge products, with capacity utilization in excess of 90 percent for the finer geometries in the 1.5-micron range. Capital spending is expected to rise 40 percent in 1988 in both the United States and Japan.

As new plants are brought on stream, capacity utilization for high-integration devices should ease a bit later this year. High-end microprocessors should soon cease to be supply limited, but microprocessor demand in 1988 is constrained by memory shortages. Although we expect demand to exceed supply for DRAMs in 1988, we expect supply to catch up in 1989 as a result of increased capacity and improved yields for 1Mb DRAMs, putting downward pressure on prices.

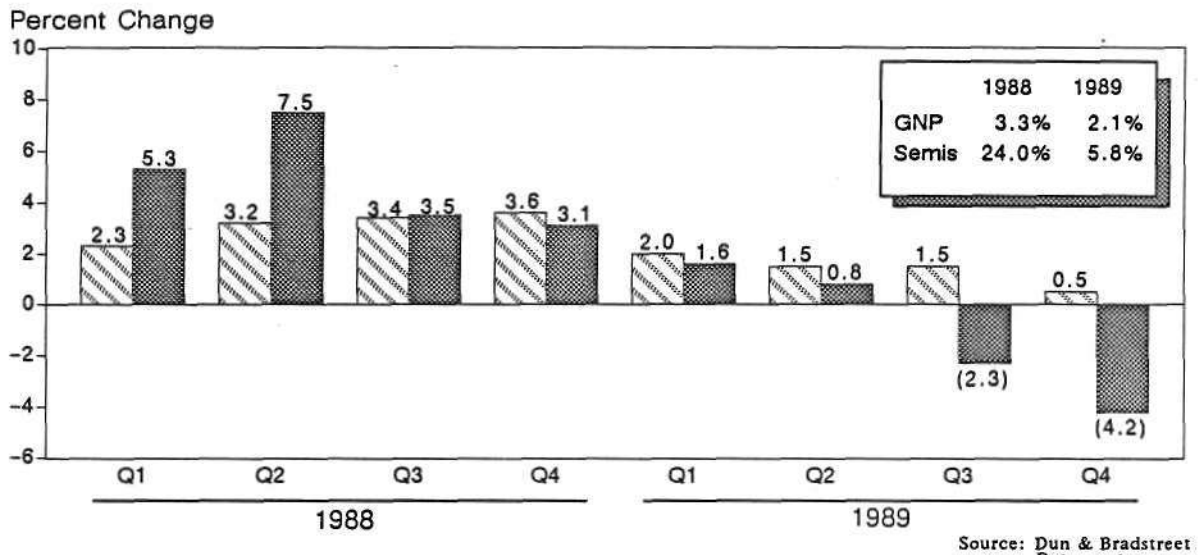
NORTH AMERICAN SEMICONDUCTOR MARKET

In the North American Semiconductor market, the strength in bookings continued in the first quarter of 1988 as confirmed by the SIA reports of robust book-to-bill ratios in the 1.15 to 1.17 range. The bookings and billings levels are now in striking range of beating the records set in 1984. The broad-based strength in data processing equipment production is driving the semiconductor demand, and demand for PCs, technical computers, and business computers continues to be strong. The resulting shortages in memory chips and high-end micros have put upward pressure on prices. Supporting the health of the industry, Dataquest's Semiconductor Application Markets (SAM) service surveys suggest that end-user inventories of semiconductors are below their target levels. Dataquest projects that the North American semiconductor market will grow 24 percent in 1988.

A mild chip recession is anticipated by mid-1989, coincident with a mild recession in the U.S. economy (see Figure 2). As the growth in U.S. real GNP slows from 3.3 percent in 1988 to 2.1 percent in 1989, worldwide electronic equipment production is expected to slow down. In particular, U.S. computer and data processing equipment production is expected to slow down from a 10.0 percent pace in 1988 to an 8.0 percent pace in 1989 and a 6.0 percent pace in 1990 (see Figure 3).

Figure 2

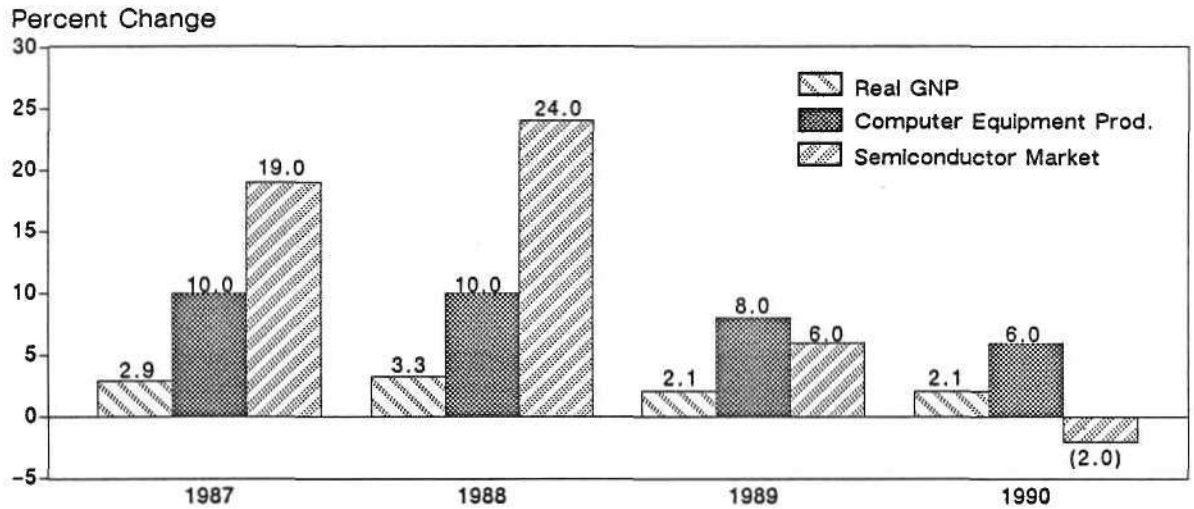
U.S. Economy versus Semiconductors



Source: Dun & Bradstreet
Dataquest
June 1988

Figure 3

U.S. Economy versus Equipment versus Semiconductors



Source: Dun & Bradstreet
Dataquest
June 1988

The chip recession is signaled by a virtually flat semiconductor market forecast for the second quarter of 1989 in North America. This should be followed by four to five quarters of mild contraction spanning the second half of 1989 and the first half of 1990, resulting in an annual growth of 5.8 percent in 1989 and a decline of 2.2 percent in 1990 in the North American semiconductor market.

The stagger chart shown in Table 3 compares our current forecast to our prior forecasts. A significant change from our prior forecast is the timing of the next chip recession. Some of the strength in 1988 is now anticipated to spill over into early 1989 because of the memory shortage. The mild downturn is now projected to span second half of 1989 and first half of 1990.

Table 3

North American Semiconductor Market
Stagger Chart
(Percent Change, U.S. Dollars)

Forecast Date	1987	1988	1989	1990
October 1986	12%	30%	(5%)	11%
January 1987	13%	23%	(5%)	11%
April 1987	15%	22%	(0%)	12%
July 1987	18%	22%	(1%)	12%
October 1987	21%	20%	(2%)	13%
January 1988		21%	(1%)	14%
April 1988		24%	6%	(2%)

Source: Dataquest
June 1988

The North American product detail forecasts are shown in Tables 4 and 5. MOS memory is the fastest growing product area in the North American market, growing 49.0 percent in 1988. MOS logic (including ASICs) and MOS microcomponents are also strong, growing 32.0 percent and 29.0 percent, respectively. The long-term forecast is for a robust 13.5 percent compound annual growth rate (CAGR) from 1987 through 1992 for the North American semiconductor market. MOS memory leads with 20.4 percent CAGR, followed by MOS logic with 17.0 percent CAGR and MOS microcomponents with 14.4 percent CAGR. High-end microprocessors and denser memories push up the average selling price of these high-integration devices. The replacement of discrete devices and standard logic by ASICs transfers value from board real-estate and wire traces to ICs. Bipolar memory is a declining market because the proportion of TTL PROMs getting replaced by MOS EPROMs and EEPROMs outpaces the growth in the high-speed ECL RAM market. Linear (analog) ICs are strong, with 11.2 percent CAGR due to fast-growing segments such as linear arrays and telecom ICs.

Table 4

Estimated Semiconductor Shipments to North America by Quarter (Millions of Dollars)

	1987	Q1/88	Q2/88	Q3/88	Q4/88	1988	Percent Change 1987-1988
Total Semiconductor	$11,869	$3,395	$3,651	$3,779	$3,895	$14,720	24.0%
Total IC	9,991	2,908	3,140	3,264	3,370	12,682	26.9%
Bipolar Digital	2,072	510	561	590	608	2,269	9.5%
Memory	279	65	72	76	84	297	6.5%
Logic	1,793	445	489	514	524	1,972	10.0%
MOS Digital	6,128	1,928	2,086	2,171	2,239	8,424	37.5%
Memory	2,347	815	862	892	916	3,485	48.5%
Micro	1,817	533	584	609	623	2,349	29.3%
Logic	1,964	580	640	670	700	2,590	31.9%
Linear	1,791	470	493	503	523	1,989	11.1%
Discrete	1,442	377	396	396	404	1,573	9.1%
Optoelectronic	436	110	115	119	121	465	6.7%

	1988	Q1/89	Q2/89	Q3/89	Q4/89	1989	Percent Change 1988-1989
Total Semiconductor	$14,720	$3,956	$3,988	$3,898	$3,734	$15,576	5.8%
Total IC	12,682	3,424	3,453	3,377	3,240	13,494	6.4%
Bipolar Digital	2,269	616	617	587	555	2,375	4.7%
Memory	297	82	77	72	70	301	1.3%
Logic	1,972	534	540	515	485	2,074	5.2%
MOS Digital	8,424	2,275	2,303	2,273	2,187	9,038	7.3%
Memory	3,485	941	950	935	895	3,721	6.8%
Micro	2,349	632	633	623	612	2,500	6.4%
Logic	2,590	702	720	715	680	2,817	8.8%
Linear	1,989	533	533	517	498	2,081	4.6%
Discrete	1,573	408	409	397	373	1,587	0.9%
Optoelectronic	465	124	126	124	121	495	6.5%

Source: Dataquest June 1988

Table 5

Estimated Semiconductor Shipments to North America
by Year
(Millions of U.S. Dollars)

	1987	1988	1989	1990	1991	1992	CAGR 1987-1992
Total Semiconductor	$11,869	$14,720	$15,576	$15,236	$17,993	$22,355	13.5%
Total IC	9,991	12,682	13,494	13,079	15,655	19,762	14.6%
Bipolar							
Digital	2,072	2,269	2,375	2,245	2,528	2,924	7.1%
Memory	279	297	301	291	275	265	(1.0%)
Logic	1,793	1,972	2,074	1,954	2,253	2,659	8.2%
MOS Digital	6,128	8,424	9,038	8,664	10,582	13,794	17.6%
Memory	2,347	3,485	3,721	3,499	4,287	5,936	20.4%
Micro	1,817	2,349	2,500	2,375	2,890	3,558	14.4%
Logic	1,964	2,590	2,817	2,790	3,405	4,300	17.0%
Linear	1,791	1,989	2,081	2,170	2,545	3,044	11.2%
Discrete	1,442	1,573	1,587	1,642	1,753	1,904	5.7%
Optoelectronic	436	465	495	515	585	689	9.6%

Source: Dataquest
June 1988

WORLDWIDE SEMICONDUCTOR MARKET

The Japanese semiconductor market experienced slow growth of only 4 percent in 1987 measured in yen, although the yen appreciation translated this to 21 percent growth measured in U.S. dollars. The Japanese market is now projected to recover in 1988 to 15 percent growth measured in yen. At a constant exchange rate of 130 yen to the U.S. dollar, compared with the 1987 rate of 144 yen, this translates to 27 percent growth measured in U.S. dollars. Despite the slowdown in consumer electronics production in Japan for export to the United States due to the yen appreciation, semiconductor consumption in Japan is shifting more and more into the telecom and data processing application markets. Electronic equipment production in Japan is expected to grow 7 percent in 1988.

Real GDP growth in Japan is expected to slow from 3 percent in 1988 and 1989 to 2 percent in 1990. A slow third quarter in 1989 signals the chip recession in Japan. This should be followed by three to four quarters of mild decline, resulting in an annual growth of 9 percent in 1989 and a mild decline of 4 percent in 1990 in the Japanese semiconductor market.

The European semiconductor market declined 1 percent in 1987, measured in local currency, though this translates to 16 percent growth when measured in U.S. dollars. The European market is now projected to recover to 12 percent growth in 1988, measured in local currency. At a constant exchange rate of 117 European Basket Currency Units, compared with the 1987 rate of 125 Units, this translates to 20 percent growth measured in U.S. dollars. Though European electronic equipment production continues to stagnate with only 5 percent growth expected in 1988, semiconductor demand is spurred by growth in selected areas such as PCs, workstations, and telephones. In addition to the production increase of such U.S. computer companies as Digital Equipment, Hewlett-Packard, and IBM, some Japanese electronics manufacturers are opening facilities in Europe to be closer to the markets they serve. The long-term projection is for continued modest growth in the European semiconductor market with the usual summer doldrums. The outlook is for 6 percent growth in 1989, slowing to 2 percent growth in 1990.

The Rest of World (ROW) semiconductor market, including the Asia/Pacific region (Korea, Taiwan, Singapore, Hong Kong, China) boomed in 1987, growing a whopping 67 percent. We expect this growth to "moderate" to 39 percent in 1988 in this fastest-growing region of the world. While the 1987 growth came from relocation of electronic equipment production by U.S. companies, this trend has slowed considerably. However, Japanese electronics manufacturers are now reported to be relocating plants to Asia/Pacific, sustaining growth in the region. As the U.S. economy slows, the growth in the ROW semiconductor market should flatten during the second half of 1989. The long-term outlook is for growth slowing to 22 percent in 1989 and 7 percent in 1990 in the ROW semiconductor market. As we move into the 1990s, semiconductor consumption in the ROW region should be sustained more and more by electronic equipment produced for local consumption in potentially vast markets such as China. Dataquest estimates that the ROW semiconductor market will surpass the European market in size by 1992, accounting for more than 16 percent of worldwide semiconductor consumption (see Figure 4).

The Worldwide semiconductor shipment forecasts are shown in Tables 6 and 7. The relative product trends are similar to the North American market. MOS memory leads the pack with 42.0 percent growth in 1988, followed by MOS logic growing 33.0 percent and MOS microcomponents growing 28.0 percent. Linear (analog) ICs and optoelectronic devices will grow 20.0 percent, faster than the North American pace, with Japanese and ROW markets contributing to the growth. The long-term outlook is for a strong 13.8 percent CAGR for the world semiconductor market from 1987 through 1992. MOS memory leads with 17.7 percent CAGR, followed by MOS logic with 17.3 percent CAGR, MOS microcomponents with 14.3 percent CAGR, and linear with 13.3 percent CAGR. Optoelectronics will grow at 11.7 percent CAGR because of fast-growing segments such as laser devices used in compact discs (CDs), charge-coupled device (CCD) sensors used in imaging, and fiber-optic couplers used in telecommunications.

In summary, Dataquest forecasts the world semiconductor market to grow 26.0 percent in 1988, measured in U.S. dollars. Due to the cyclical downturn caused by slowing demand and capacity buildup, growth should decelerate to 9.0 percent in 1989, followed by a mild 1.5 percent decline in 1990. The industry should then enter the recovery cycle, topping 22.0 percent growth by 1992.

George Burns
Joseph Borgia

Figure 4

Semiconductor Markets:
The Emergence of Rest of World

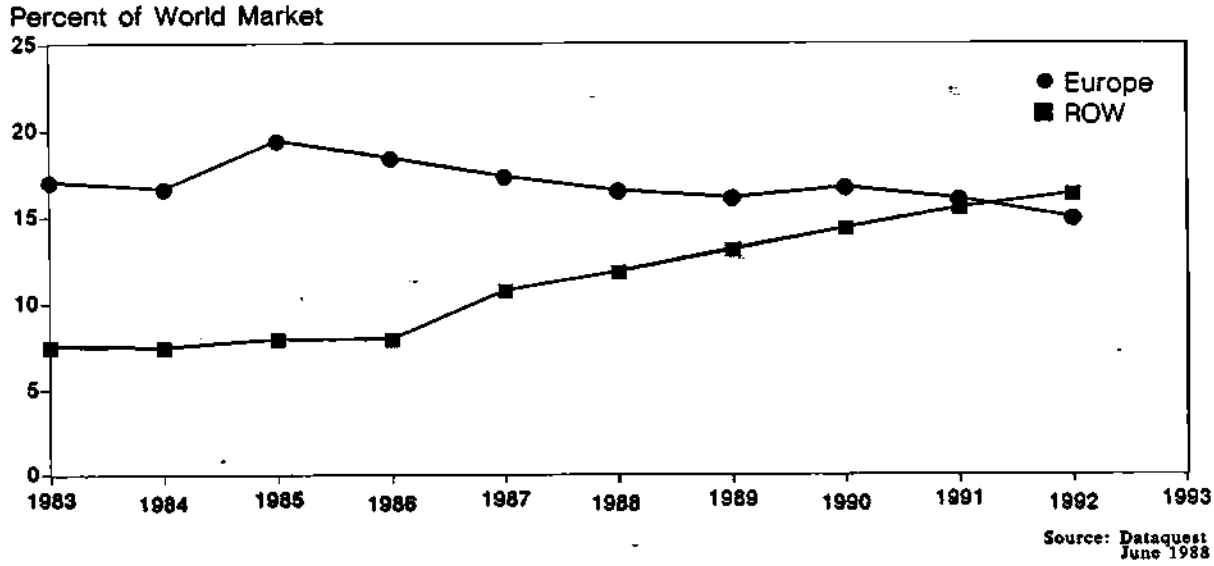


Table 6

Estimated Worldwide Semiconductor Shipments
(Millions of U.S. Dollars)

	1987	Q1/88	Q2/88	Q3/88	Q4/88	1988	Percent Change 1988
Total Semiconductor	$36,498	$10,831	$11,404	$11,736	$12,077	$46,048	26.2%
Total IC	28,668	8,602	9,098	9,399	9,707	36,806	28.4%
Bipolar Digital	4,672	1,263	1,364	1,424	1,480	5,531	18.4%
Memory	565	143	153	158	167	621	9.9%
Logic	4,107	1,120	1,211	1,266	1,313	4,910	19.6%
MOS Digital	16,788	5,285	5,580	5,783	5,973	22,621	34.7%
Memory	6,019	1,999	2,099	2,184	2,246	8,528	41.7%
Micro	4,819	1,435	1,531	1,579	1,609	6,154	27.7%
Logic	5,950	1,851	1,950	2,020	2,118	7,939	33.4%
Linear	7,208	2,054	2,154	2,192	2,254	8,654	20.1%
Discrete	6,112	1,734	1,797	1,814	1,840	7,185	17.6%
Optoelectronic	1,718	495	509	523	530	2,057	19.7%
Exchange Rate Yen/$	144	130	130	130	130	130	(9.7%)
European Basket/$	125	117	117	117	117	117	(6.4%)

	1988	Q1/89	Q2/89	Q3/89	Q4/89	1989	Percent Change 1989
Total Semiconductor	$46,048	$12,368	$12,713	$12,649	$12,464	$50,194	9.0%
Total IC	36,806	9,960	10,241	10,181	10,019	40,401	9.8%
Bipolar Digital	5,531	1,506	1,526	1,469	1,400	5,901	6.7%
Memory	621	165	164	156	151	636	2.4%
Logic	4,910	1,341	1,362	1,313	1,249	5,265	7.2%
MOS Digital	22,621	6,139	6,332	6,339	6,263	25,073	10.8%
Memory	8,528	2,332	2,421	2,425	2,405	9,583	12.4%
Micro	6,154	1,643	1,697	1,704	1,699	6,743	9.6%
Logic	7,939	2,164	2,214	2,210	2,159	8,747	10.2%
Linear	8,654	2,315	2,383	2,373	2,356	9,427	8.9%
Discrete	7,185	1,864	1,911	1,907	1,891	7,573	5.4%
Optoelectronic	2,057	544	561	561	554	2,220	7.9%
Exchange Rate Yen/$	130	130	130	130	130	130	0
European Basket/$	117	117	117	117	117	117	0

Source: Dataquest
June 1988

Table 7

Estimated Worldwide Semiconductor Shipments
(Millions of U.S. Dollars)

	1987	1988	1989	1990	1991	1992	CAGR 1987-1992
Total Semiconductor	$36,498	$46,048	$50,194	$49,446	$57,152	$69,533	13.8%
Total IC	28,668	36,806	40,401	39,572	46,253	57,203	14.8%
Bipolar Digital	4,672	5,531	5,901	5,731	6,492	7,572	10.1%
Memory	565	621	636	613	578	534	(1.1%)
Logic	4,107	4,910	5,265	5,118	5,914	7,038	11.4%
MOS Digital	16,788	22,621	25,073	24,291	28,621	36,179	16.6%
Memory	6,019	8,528	9,583	8,967	10,327	13,608	17.7%
Micro	4,819	6,154	6,743	6,603	7,742	9,382	14.3%
Logic	5,950	7,939	8,747	8,721	10,552	13,189	17.3%
Linear	7,208	8,654	9,427	9,550	11,140	13,452	13.3%
Discrete	6,112	7,185	7,573	7,613	8,339	9,341	8.9%
Optoelectronic	1,718	2,057	2,220	2,261	2,560	2,989	11.7%
Exchange Rate Yen/$	144	130	130	130	130	130	
European Basket/$	125	117	117	117	117	117	

Source: Dataquest
June 1988

Dataquest
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The Dun & Bradstreet Corporation

Research *Bulletin*

SEMS Code: 1987–1988 Newsletters: June
1988–17
0000439

PRIME TIME FOR CAPITAL SPENDING

Capital spending by merchant and captive semiconductor manufacturers will increase by a healthy 39 percent in 1988 (see Tables 1 and 2). Table 1 shows worldwide capital spending by North American, Japanese, European, Rest of World (ROW), and captive semiconductor companies. Table 2 shows spending in each world region by all merchant and captive companies, regardless of their company headquarters location.

Although growth will be quite strong in 1988, we expect the rate of increase to slow significantly in 1989 and again in 1990. It still will remain positive, however. This slowdown in capital spending will be the result of slowdowns in the U.S. and world economies and a coincident slowdown in the growth rate of such semiconductor end–use markets as data processing. Nonetheless, our outlook for the next five years is basically positive. We expect healthy growth to revive in both 1991 and 1992 at rates near or above 30 percent. For the period from 1987 through 1992, we expect a compound annual growth rate (CAGR) of 21 percent.

Capital spending will be driven by the need for increased capacity and upgrades, especially for leading–edge devices. Capital spending also will be fueled by competitive pressures as many manufacturers locate front–end facilities offshore in order both to be close to their markets and to protect themselves from the double nemesis of trade friction and currency fluctuations.

Capital spending will grow at a much steadier rate than in the past. Semiconductor manufacturers, though spending for more capacity, will remain cautious; they prefer to increase equipment availability and yields before adding capacity. Consequently, while Dataquest does not expect skyrocketing growth such as occurred in 1984, we also do not expect the devastating descents that occurred in 1985/1986. The peaks may not be as high, but the ride will be smoother and more sustainable.

We expect spending by all companies in Japan (including U.S. merchants and IBM) to increase at a CAGR of 24 percent. The reason for this high growth is the fairly low starting base, especially if looked at in yen. We also expect spending by all regional companies in the ROW region to grow at a CAGR of 24 percent. This growth rate will be driven by Asia–Pacific companies' commitment to grow as world–class manufacturers and by the new fab construction of European and North American companies in the ROW region.

Spending in the North American region will grow at a healthy 19 percent CAGR, to almost $6 billion in 1992. This growth will be fueled by new fabs and upgrades for leading–edge devices, especially DRAMs and microprocessors. Dataquest also expects a

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strong surge of spending by Japanese companies in the United States; several Japanese companies have either already initiated new fab construction or are planning to soon. The European region will experience the slowest growth rate, only 15 percent. This relatively slow growth is due to the recent completion of major expansions by Philips and Siemens, and to the rationalization of existing facilities by SGS-Thomson. Captives will play a major role in Europe: AT&T will complete its new fab in Spain in 1989, and IBM will begin production on the largest 200mm fab in the world at Sindelfingen, West Germany, also in 1989.

George Burns

Table 1

Worldwide Capital Spending by Regional Companies

	1984	1985	1986	1987	1988
North America	$3,039	$2,072	$1,580	$1,834	$2,548
Japan	3,771	3,233	1,899	2,158	3,442
Europe	763	689	759	724	730
ROW	434	439	273	355	451
Captive	731	805	801	883	1,110
Worldwide Capital Spending	$8,738	$7,238	$5,313	$5,954	$8,281
Percent Change	106.2%	(17.2%)	(26.6%)	12.1%	39.1%

	1989	1990	1991	1992	CAGR (1987-1992)
North America	$2,675	$2,405	$ 3,064	$ 4,167	18%
Japan	3,683	3,643	4,918	6,639	25%
Europe	861	973	1,245	1,432	15%
ROW	541	730	949	1,139	26%
Captive	1,232	1,380	1,594	1,980	18%
Worldwide Capital Spending	$8,993	$9,131	$11,770	$15,357	21%
Percent Change	8.6%	1.5%	28.9%	30.5%	

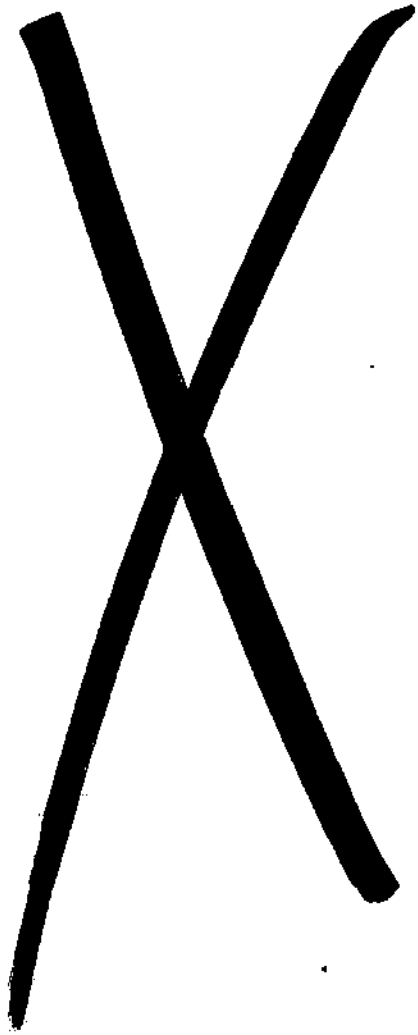
Table 2

Regional Capital Spending Including Captives (Millions of Dollars)

	1984	1985	1986	1987	1988
North America	$3,569	$2,635	$2,186	$2,472	$3,314
Japan	3,897	3,336	1,994	2,260	3,578
Europe	838	803	834	842	920
ROW	434	463	299	380	468
Worldwide Capital Spending	$8,738	$7,238	$5,313	$5,954	$8,281
Percent Change	106.2%	(17.2%)	(26.6%)	12.1%	39.1%

	1989	1990	1991	1992	CAGR (1987-1992)
North America	$3,583	$3,659	$ 4,548	$ 5,927	19%
Japan	3,810	3,689	4,929	6,640	24%
Europe	1,055	1,128	1,392	1,694	15%
ROW	545	655	900	1,096	24%
Worldwide Capital Spending	$8,993	$9,131	$11,770	$15,357	21%
Percent Change	8.6%	1.5%	28.9%	30.5%	

Source: Dataquest June 1988



Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987–1988 Newsletters: July
1988–23
0000921

A SAMPLING OF SUB–1.5–MICRON DEVICES MARCH THROUGH JUNE 1988

INTRODUCTION

This newsletter lists the new commercial products with line geometries of 1.5 microns or below that were announced from March through June 1988. For the most part, the products are either being sampled or in production. (Although the list is not the result of a thorough literature search, Dataquest believes that it represents a fair cross section of the sub–1.5–micron products introduced during the four–month period.) The intent of this newsletter is to provide our clients with a barometer of the changes occurring in fabrication technology and an idea of the types of leading–edge products entering production.

Table 1 summarizes the new product introductions by linewidth. (A product family, such as an ASIC family is considered a single product.) Of the 71 new products listed in this newsletter, 37 percent are (or will be) fabricated with 1.5–micron linewidths, while 63 percent are fabricated with 1.3–micron linewidths or less. Twenty–one of the new products (or 29 percent) are fabricated with 1.1–micron or lower linewidths, and 11 percent are fabricated with submicron geometries.

Table 1

New Products by Linewidth (Microns)

Family	1.5	1.3 to 1.2	1.1 to 1.0	Submicron	Total
Microprocessor Products	13	8	5	1	27
Memory Products	8	9	2	4	23
ASIC and Logic Products	5	7	6	3	21
Total	26	24	13	8	71
Total (Share)	37%	34%	18%	11%	100%

Source: Dataquest July 1988

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Table 2 lists the 21 products that have linewidths of 1.1 microns or lower and the companies that will manufacture the products.

The Semiconductor Equipment and Materials Service plans to publish this newsletter at periodic intervals; Tables 1 and 2 will serve as a benchmark by which progress in industry linewidths can be measured in our future newsletters.

Table 2

1.0–Micron and Submicron Devices

Company	Linewidth (Microns)	Device Type
Microprocessors		
Analog Devices	1.0	DSP
Cypress	0.8	Integer unit
LSI Logic	0.9 (eff.)	RISC MPU
Texas Instruments	1.0	Microsequencer
Texas Instruments	1.0	DSP
Texas Instruments	1.0	Floating-point processor
Memory		
Atmel	1.0	256K EPROM
Fujitsu	0.8	4-Mbit DRAM
Hitachi	0.8	4-Mbit DRAM
Hitachi	0.8	1-Mbit SRAM
Samsung	0.8	4-Mbit DRAM
Samsung	1.0	1-Mbit DRAM
ASIC and Logic		
Applied Micro Circuits/Plessey	0.6	ECL gate array
Cypress	0.8	EPLD
Fujitsu	0.5	HEMT logic IC
IBM	1.0	Mixed gate array/std. logic IC
Intel	1.0	EPLD
Lattice Semiconductor	1.1	General array logic
Raytheon	1.0	CMOS gate array
Sony	1.0	ECL logic
Texas Instruments	1.0	CMOS gate array

Source: Dataquest
July 1988

MICROPROCESSOR, MICROCONTROLLER, AND PERIPHERAL PRODUCTS

- Cypress Semiconductor has introduced the integer unit of its CY7C600 SPARC chip set. The CY7C601 IU operates at 33 MHz and is built with a 0.8-micron, double-metal CMOS process. (6/27/88)

- Intel has announced that 16-MHz samples of its new 16-bit 80386SX MPU with a 32-bit internal architecture have been shipped. The device is fabricated with a 1.5-micron CMOS process at Intel's Fab 3 in Livermore, California. Volume production is scheduled for the fourth quarter. (6/20/88)

- Weitek is sampling the 3167, a math coprocessor for computers based on the Intel 80386 32-bit MPU. The 3167 is a single-chip version of Weitek's 1167 math coprocessor, which was implemented in a three-device set. The 3167 is available in 20-MHz or 25-MHz versions and is fabricated with a 1.5-micron Hewlett-Packard CMOS process. (6/20/88)

- Texas Instruments has announced its SN74ACT8818 16-bit microsequencer that can support a 50ns system cycle. The device is fabricated with a 1-micron CMOS process. TI says that it is the fastest microsequencer yet available. (6/20/88)

- Motorola has announced a 33-MHz version of the 68030; the new version is fabricated with a 1.2-micron CMOS process. Motorola will begin sampling the device in August from its Austin, Texas, facility. (6/6/88)

- Acer Laboratories, the U.S. design arm of Taiwan-based Acer Inc., is entering the IBM PS/2-compatible marketplace with an eight-device, core-logic chip set for the Model 30 and 25 computers. Called the PC86 chip set, one of the chips (the M1201 system controller) is fabricated with a 1.5-micron CMOS process; the other seven chips are done with a 2-micron CMOS process. The chip set will be available in production volumes in July, and will be fabricated in the company's foundries in the United States, Japan, and Europe. (5/30/88)

- V.M. Technology, a start-up company based in Tokyo, will sample a 32-bit microprocessor called the VM8600S in September. The device is designed with a 1.2-micron, double-metal CMOS process. Volume production is scheduled for 1989. (5/2/88)

- Oki has available the 699210, a DSP with 22-bit floating-point capability. The device is fabricated with a 1.5-micron CMOS process. (4/25/88)

- VLSI Technology is offering a 32-bit RISC microprocessor that was designed in conjunction with Acorn Computers of the United Kingdom. The VL86C010 MPU, as well as the MPU's peripheral chips, the VL86C110 memory controller, VL86C310 video controller, and VL86C410 I/O controller, are presently fabricated with a 2-micron CMOS process. VLSI is in the process of scaling the MPU to a 1.5-micron process. (4/18/88)

- NEC is sampling the V33, a 16-MHz hard-wired version of its 16-bit V-series microprocessor. The V33 eliminates the microcode that has been the subject of a three-year copyright suit with Intel. The V33 is fabricated with a 1.2-micron CMOS process. Volume production is scheduled for the third quarter of 1988. (4/18/88)

- Texas Instruments will sample a third-generation DSP chip, the TMS320C30, in the second quarter; production is scheduled for 1989. The device will be fabricated with a 1-micron CMOS process. TI also announced that it is working on a fourth-generation chip, the TMS320C40, which will be a submicron version. It will be introduced in the first half of 1989. (4/18/88)

- Intel introduced two new 32-bit microprocessors for embedded control applications, the new 80960 family with a CPU based on RISC techniques, and the 80376, a stripped-down version of the 80386 CISC microprocessor. The 80960 family is based on a RISC-like core of about 250,000 transistors surrounded by another 100,000 transistors in peripheral circuitry. It is fabricated with a 1.5-micron CMOS process. The family currently consists of three devices, but future versions will be added for event-controlled applications, such as a 32-bit automotive controller. (4/11/88)

- Austek Microsystems is sampling a 25-MHz cache controller, the A38152-25 Microcache, for use with 25-MHZ 80386 designs. The device includes 120,000 transistors and is fabricated with a 1.5-micron CMOS process. (4/11/88)

- Fujitsu will sample a 25-MHz second-generation version of the Sun SPARC 32-bit RISC microprocessor in July; volume production is scheduled for September. The new version, called the S-25, is fabricated with Fujitsu's 1.2-micron, double-metal CMOS standard-cell library and is an upgrade of the initial 16-MHz version introduced in the summer of 1987 in a gate array configuration. A faster 1-micron version is planned for the middle of 1989. (4/4/88)

- Analog Devices has added the ADSP2101 and ADSP2102 DSP chips to its 16-bit ADSP2100 family. The 2101/2102 chips offer 12.5 and 10 mips, respectively; the 2101 is an all-RAM version, while the 2102 provides mask ROM for high-volume signal processing applications. The chips are fabricated with a 1-micron CMOS process. Sampling is expected in the fourth quarter of 1988, with volume production scheduled for the first half of 1989. (4/4/88)

- Advanced Micro Devices has introduced a 64-bit floating-point processor that incorporates Digital Equipment, IBM, and IEEE floating-point standards on a single chip. First sampling is expected in May, with production scheduled for the fourth quarter of 1988. The 10-mflop Am29C327 has 250,000 transistors and is fabricated with a 1.2-micron CMOS process at AMD's Austin, Texas, facility. (3/28/88)

- Motorola has announced two new floating-point DSPs, the DSP96001 and DSP96002. The chips can perform at 13.33 mips, which Motorola claims sets a new record for single-chip general-purpose DSPs. They will be fabricated with Motorola's 1.2-micron, double-metal HCMOS process. The 96001 will be sampled in December with production scheduled for the second quarter of 1989. The 96002 will be sampled in 1989. (3/28/88)

- LSI Logic's G-2 affiliate has introduced a second round of new products for the start-up venture. The GC100 is an IBM PS/2 Model 30 or XT-compatible device that, on a single chip, integrates the functions of the Intel 8237A DMA controller, 8254 interval timer, 8255 peripheral interface, 8288 bus controller, and the 8284 clock generator. G-2 is also offering a three-chip set to implement an 80386-based AT that comprises the GC132 CPU and memory controller and the GC131 peripheral controller. In addition, G-2 is offering the GC205 VGA, jointly developed by LSI Logic and Video Seven.

  All of these products are fabricated with a 1.5-micron process at LSI Logic's facility in Milpitas, California and at the Nihon Semiconductor facility at Scuba, Japan, which LSI Logic built in partnership with Kawasaki. The process will migrate to 1.2 microns at the end of 1988. (3/28/88)

- Texas Instruments is sampling a 64-bit floating-point processor designed for use with the 32-bit SPARC RISC microprocessor. The device, called the SN74ACT8847, is fabricated with TI's 1-micron EPIC CMOS process and can perform 33 mflops. (3/21/88)

- At the heart of Unisys' new 2200/400 midrange computer is a microprocessor chip set expressly designed for the 2200/400. The 6-device chip set, the Micro 1100, consists of an arithmetic logic unit, an address generator unit, a decode/control unit, a cache/interface unit, an extended instruction set unit, and a multiply/divide unit. The Micro 1100 chip set is fabricated at Unisys' facility in Rancho Bernardo, California, using a 1.5-micron, double-metal, single-poly, n-well CMOS process. Unisys will shrink the design to 1.2-micron design rules. (3/21/88)

- Weitek has announced two new single-chip, 64-bit, floating-point processors, each operating at a peak rate of 20 mflops. The WTL3164 chip is intended for cost-sensitive applications and is expected to be used in graphics applications and as a coprocessor for CISC and emerging RISC CPUs. The WTL3364 will be used in applications demanding the highest throughput. The two devices are being built by Hewlett-Packard at its Corvallis, Oregon, facility using a 1.25-micron, double-metal, single-poly process; a 1-micron process is planned for volume production. Sampling will take place in July, with production scheduled for October. (3/14/88)

- VLSI Design Associates has introduced a PS/2-compatible color palette. The VDA-176 includes a 256 x 18 RAM color look-up table with triple 6-bit D-A converters. It is produced by Ricoh with a 1.5-micron, double-metal CMOS process. It will be sampled in April. (3/14/88)

- By midsummer, LSI Logic will sample, a 25-MHz cell-based RISC microprocessor that implements Sun Microsystem's SPARC architecture. The 15-mips chip will be fabricated with a CMOS process with a 0.9-micron effective (not drawn) gate length. (3/21/88)

- Intel is sampling a serial communications device, the 82526, for automobiles and other motorized vehicles. The device is designed to prioritize and distribute signals in an automotive system, and to replace electrical harness wiring with a single twisted-pair or coaxial cable. The 82526 is fabricated with a 1.5-micron CMOS process. (3/7/88)

- General Electric's Undersea Systems Department (USD) has demonstrated a 32-bit CPU that operates at 40 MHz, almost twice as fast as commercial devices. The custom CPU chip uses an extension of RISC architecture, and was developed by GE using its 1.25-micron VHSIC-like CMOS process. The CPU is one of two chips being developed by USD as part of its High-Speed CMOS Microprocessor Program. (3/88)

MEMORY PRODUCTS

- Tables 3 and 4 were compiled from an article that discussed fast CMOS 256K and 1-Mbit EPROMs that are either in production, being sampled, or will be released in the near future. Devices with geometries greater than 1.5 micron are included for completeness. (6/27/88)

Table 3

Fast 256K EPROMs

Company	256K Device	Speed	Geometry	Price
Atmel	AT27HC256	55ns	1.5 micron	$52
Catalyst Semiconductor	CAT27HC256	55ns	-	-
Hitachi	HN27C256HG	70ns	1.3 micron	$ 7
AMD	Am27C256	90ns	1.35 micron	$30
Texas Instruments	TMS27C256-120	120ns	1.7 micron	$11
Intel	27C256-120	120ns	1.5 micron	$17
Mitsubishi	M5M27C256	120ns	2.0 microns	-
SGS-Thomson Microelectronics	-	200ns	2.0 microns	$ 5

Table 4

Fast 1-Mbit EPROMs

Company	1-Mbit Device	Speed	Geometry	Price
Hitachi	HN27C1024HG	85ns	-	-
Atmel	-	90ns	1.2 micron	-
SGS-Thomson Microelectronics	-	20ns	1.2 micron	-
AMD	Am27C010	150ns	1.35 micron	$55
Texas Instruments	TMS27C210	150ns	1.7 micron	-
Mitsubishi	M5M27C100K	150ns	1.5 micron	-
Fujitsu	MBM27C1001	200ns	1.5 micron	-
	MBM27C1024	200ns	1.5 micron	-
	MBM27C1028	200ns	1.5 micron	-

Source: Dataquest
July 1988

- Hitachi is sampling its 1-Mbit SRAM, the HM628128. Unlike the Inova 1-Mbit SRAM, which uses a modular approach, Hitachi's device is a true monolithic design. It is organized as 128Kx8 and available with speeds down to 70ns. It is the first device from Hitachi that uses a 0.8-micron CMOS process. Hitachi traditionally has used the SRAM as a process driver, and the 1-Mbit SRAM is being built with the same process that will be used for its 4-Mbit DRAM. Volume production is scheduled to begin in the first quarter of 1989. The Hitachi spokesperson said that its 4-Mbit SRAM, the process driver for 16-Mbit DRAMs, will be built with a 0.5-micron design rule. (6/27/8)

- Toshiba has introduced two new products: a fast 256K flash EEPROM with access times down to 170ns, and a fast 256K EPROM with access times down to 70ns.

  The TC58257AP/AF EEPROM has a 4.49mm x 4.96mm die size and is fabricated with 1.2-micron design rules. Sample shipments will start in June with mass production scheduled to begin in September. The TC57H256D EPROM has a 4.49mm x 4.88mm die size and is fabricated with 1.5-micron design rules. Sample shipments will begin in August, and volume production is scheduled to begin in the fourth quarter of 1988. Both the EEPROM and EPROM devices use NMOS for the memory cell and CMOS for the peripheral circuits. The EPROM device uses a polycide structure to obtain more than a 40 percent gain in access time over a conventional polysilicon approach. (6/17/88)

- Inova Microelectronics Corporation has announced the first commercially available monolithic 1-Mbit SRAM, the S128K8. The 70ns S128K8 chip measures 1.338 inches x 0.370 inches and contains 20 64K SRAM prime die of which 16 are ultimately connected, via wafer-scale integration, to obtain a 1-Mbit SRAM. Yield for such a large chip is assured with the 25 percent 64K die redundancy. Inova has been sampling the chip since January, and fabrication on 150mm wafers is being done by Sharp in Japan.

  The chip is manufactured as follows. The individual 64K die are fabricated on the wafer with a normal 1.2-micron, double-metal, double-poly CMOS process. In the 20-die array, the functional 64K die are determined after first metal at the probe stage; the nonfunctional die are disconnected at this point by lasing fuse links. A universal second metal layer, which is the wafer-scale integration, is then added to fully interconnect the chip.

  Nikon 5X steppers are used for the lithography. Note that for all but the second layer of metal, normal die imaging can be used, as there is no electrical connection between the prime die, and individual (or multiple) prime die are well within the Nikon field size. For the second metal, however, reticle images must be butted since the second metal layer covers the entire chip and the Nikon field is not large enough to handle the entire chip in one exposure. Butting of second metal has not been a problem since the pitch is not tight and any mismatches between butts will not cause a problem. (6/13/88)

- Ramtron and the Intermetall subsidiary of ITT Semiconductors are teaming up to develop high-volume manufacturing of nonvolatile memories based upon Ramtron's ferroelectronic technology and ITT's 1.5-micron CMOS process. Ramtron believes that it can develop a nonvolatile memory that offers the speed and ease of use of SRAMs, the density and potential low cost of DRAMs, and the nonvolatility of EPROMs.

  The device is made by sputtering a thin ferroelectric film of ceramic lead-zirconate-titanate on a CMOS substrate. The thin film is sandwiched between two metal electrodes to form a digital memory capacitor, which is built above the existing semiconductor circuity. The process subsequently will be scaled down to 1.2 microns. Ramtron and ITT plan to develop an advanced submicron ferroelectronic IC technology in 1989. (6/6/88)

- Fujitsu and Hitachi are sampling their 4-Mbit DRAMs to selected customers. Both companies use a 0.8-micron process. (5/30/88)

- Samsung's 1-Mbit DRAM is manufactured with a 1.0-micron CMOS process. Its 4-Mbit DRAM will be made with 0.8-micron linewidths. The cell size of the 1-Mbit DRAM is 27.00 square microns; that of the 4-Mbit DRAM is 10.25 square microns.

  Samsung's 256K SRAM, the KM62256, is organized as 32Kx8 and is available with speeds down to 100ns. It is fabricated with a 1.2-micron CMOS process. (5/30/88)

- Advanced Micro Devices has extended its CMOS EPROM line with a new 1-Mbit device and a series of faster 256K devices. The 1-Mbit device, the Am27C010, is organized as 128Kx8 and is available in speeds ranging from 150ns to 300ns. The Am27C256 256K device is organized as 32Kx8 and is available in speeds ranging from 90ns to 150ns. The 1-Mbit and 256K devices are fabricated with a 1.3-micron process and are being shipped. (5/23/88)

- Atmel has introduced a 70ns 256K EEPROM that is fabricated with a 1-micron, double-metal CMOS process. The device, which is called the AT28HC256, is produced at a Japanese facility. (5/16/88)

- Intel has introduced a new family of 64K and 256K flash memories designed for embedded applications. The 27F64 and 27F256 devices are fabricated with Intel's 1.5-micron ETOX flash memory process, which uses a single-transistor cell that stores its charge on a floating gate, with programming through hot electron injection. (4/11/88)

- Next month Intel will begin shipping a 64K SRAM that has been upgraded from commercial to VHSIC qualification. The 16Kx4 part, designated the MV51C98, is the first to be qualified as part of a million-dollar, year-long Intel program to provide VHSIC parts. The MV51C98 is fabricated with 1.25-micron design rules. (3/28/88)

- Micron has introduced a fast 256K SRAM in versions down to 25ns access times. The part, designated the MT5C2561C, is fabricated with a CMOS double-metal process. (3/14/88)

ASIC AND LOGIC PRODUCTS

- Lattice Semiconductor is shipping 12ns versions of its general array logic (GAL) devices. The GAL16V8A-12 and GAL20V8A-12 are double-metal conversions of the company's original 16V8 and 20V8 single metal devices. The new devices are fabricated with a 1.1-micron process co-developed by Lattice and Seiko-Epson; the devices are built in Japan by Seiko-Epson. (6/27/88)

- General Electric has available a gate array family using continuous gate (sea-of-gates) technology with complexities of up to 50,000 gates and with up to 75 percent gate utilization. Effective gate length (not drawn) is 1.2 microns. This family is an alternate source to VLSI Technology gate arrays. (6/27/88)

- Matsushita is offering a two-day turnaround time for some of its 1.2-micron CMOS gate arrays. The MN59000 series, with gate delay times of 0.6ns, is being offered in four versions with complexities ranging from 2,000 to 10,000 gates. Normally, customization of gate arrays is done with two metal layers and four masks. Matsushita has shortened the turnaround time by prewiring the first layer of metal and incorporating the customer's specification in the second metal layer. Thus, only one mask is required. The disadvantages of this technique are that the die size is 60 to 100 percent larger and the cost is twice as much as for a conventional gate array. However, customers can easily migrate from this technology to Matsushita's conventional 1.2-micron CMOS gate array technology. (6/27/88)

- S-MOS Systems, a Seiko Epson venture, is offering several families of CMOS gate arrays. The families all have complexities of up to 38,550 gates, but their speeds differ. The SLA8000 family uses a 1.2-micron process to obtain 800ps delays, the SLA7000 family has a 1.5-micron process for 1.0ns delays, and the SLA6000 has 2-micron features for 1.8ns speeds. Also available is the SSC1000 CMOS standard-cell family with complexities of 16,000 gates that use a 1.8-micron process resulting in 1.4ns speeds. The chips are fabricated at Seiko Epson's Japanese facility. (6/27/88)

- IBM's Essex Junction facility in Vermont is building mixed gate array/standard-cell ICs as the core chip sets for the Models B10 and B20 of the company's new Application Systems/400 computers, which were introduced in early June. The devices are fabricated with a 1-micron, double-metal CMOS process. IBM's spokesperson said that the use of mixed gate array/standard-cell technology on a single chip is the first commercial application of this ASIC technology. (6/27/88)

- Intel's 5AC312 EPLD device with 50-MHz performance is now available. The chip is fabricated with Intel's 1.0-micron CHMOS EPROM process. (6/20/88)

- Applied Micro Circuits and Plessey have announced the first of a family of high-performance ECL gate arrays based upon Plessey's HE1 process. HE1 has a 0.6-micron emitter, trench isolation, triple metal, and 5-micron metal pitch. The first devices in the ELA 80000 family have 1,500, 8,000, and 16,000 gates (originally, a maximum of 14,000 gates was planned). Production

is occurring at Plessey's Swindon facility in England. In the future, Plessey will use its HE2 submicron process, which has a 3.5–micron metal pitch, to provide gate arrays with more than 30,000 gates. (6/13/88)

- Motorola uses triple–layer metal in its high–density CMOS gate arrays to obtain more than 75 percent gate utilization and small die sizes. For instance, the 105,000 gate array measures 486 mils on a side, while the 8,000 gate array measures 180 mils on a side. Typical gate delays are 250ps. (6/6/88)

- AT&T Microelectronics is sampling its first bipolar gate array, the 6,000–gate ATE6000; 1,000– and 3,000–gate devices will be available in the third quarter of 1988. The bipolar arrays are fabricated with a 1.5–micron, triple–metal, scaled–oxide isolated process. (6/6/88)

- NCR has added a family of 1.5–micron analog standard cells to its ASIC library. They allow analog functions to be combined with digital cells. The new analog cells are compatible with NCR's 1.5– and 2–micron CMOS digital libraries. (5/30/88)

- Sony has introduced a series of 24 ECL logic devices that can achieve speeds up to 4 GHz. The devices are fabricated with Sony's 1–micron ECL 3 process. (5/9/88)

- International Microelectronic Products (IMP) has announced a family of analog and digital CMOS cell libraries that allow designers to mix technologies on the same chip. The 1.2–micron digital library is available now, while the 1.2–micron analog process will be available in the fourth quarter of 1988. (5/9/88)

- NEC has introduced the uPD65000 series, its newest family of channeled CMOS gate arrays, which range from 2,000 to 45,000 gates. NEC is now sampling arrays of up to 24,000 gates fabricated with a 1.2–micron, double–metal process; later this year, two additional family members of 2,000 gates and 45,000 gates will be fabricated with a triple–metal process. (4/11/88)

- Evans & Sutherland Computer Corporation is developing a supercomputer around a half–dozen full–custom 100,000 gate chips. The devices are fabricated with a 1.25–micron CMOS VHSIC process at the VTC foundry of Control Data Corp's Federal Systems Division at Bloomington, Minnesota. The product is scheduled for delivery later this year. (4/11/88)

- NCR's Microelectronics division has introduced a family of high–speed cells for use in its VS1500 library. They are intended to replace previous cells with the same function. The VS1500 library, which is currently in the customer prototype stage, is fabricated with a 1.5–micron, double–metal, CMOS process. (4/11/88)

- Texas Instruments has released the first of three products in its TGC100 series of 1–micron CMOS gate arrays for general availability nearly a year after beginning its beta testing. The devices, with densities ranging from 3,200 to 8,896 gates have a 500ps delay, and are fabricated with TI's double–metal, silicon–gate EPIC process. (4/11/88)

- Raytheon's Mountain View, California, Semiconductor Division has a channeled gate array family ranging from 5,670 to 20,440 gates. Typical design utilization should be about 80 percent. The family is fabricated with a 1-micron CMOS technology at Raytheon's VHSIC-quality fab. (3/31/88)

- Hewlett-Packard has quietly entered the merchant ASIC market, offering selected customers a standard-cell library with programmable logic, RAM, and ROM cells. The library is fabricated with a 1.25-micron CMOS process at HP's Corvallis, Oregon, facility; it will soon migrate to a 1-micron process. (3/21/88)

- VLSI Technology will begin taking designs in April for a new family of channelless-architecture, 1.5-micron, double-metal CMOS gate arrays with 560ps delay. The VGT200 family, which is a more highly integrated version of the VGT100 family, ranges from 700 to 65,000 usable gates. VLSI is also planning to have a 1-micron, triple-metal family called the VGT300 and based on the VGT200 family; it is scheduled to be introduced by the end of 1988. The VGT300 series will have up to 200,000 usable gates. (3/21/88)

- Cypress Semiconductor is shipping a 50-MHz EPLD for programmable-state machine applications. The device, called the CY7C330-50PC, is fabricated with a 0.8-micron, double-metal CMOS process. (3/28/88)

- Fujitsu Laboratories has developed a 0.5-micron HEMT multibit data register that it claims is the first use of HEMT digital IC technology in a computer system. The 2.4mm x 2.4mm chip contains 3,335 HEMTs arrayed in 1,137 gates. At room temperature, the chip has a 490ps delay between arrival of the clock signal and data output. (3/88)

OTHER

- Bell Northern Research (BNR), the research arm of Northern Telecom, has developed an advanced monolithic optoelectronic transmitter that combines laser technology and microelectronics on a single IC. This new chip could have a major impact on the home and office by providing efficient, high-speed transmission of voice, data, and images over a single optic fiber. A BNR spokesperson says that this is the world's first optoelectronics transmitter with both of its light-reflecting mirrors fabricated entirely by semiconductor processing. The chip is fabricated on gallium arsenide with a 1-micron process. (5/16/88)

- Fujitsu has announced the FHX04/05 series of HEMT devices for satellite broadcasting systems. The devices are fabricated on gallium arsenide with a 0.25-micron gate length. E-beam lithography is used for fabricating the gates. The gate itself is a multilayer structure consisting of a tungsten silicide gate contact overlaid with a gold plating. Volume production of 50,000 units per month is scheduled to start in June. (5/9/88)

Joe Grenier

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Research *Bulletin*

SEMS Code: 1987–1988 Newsletters: July
1988–22
0000818

SILICON VALLEY GROUP ACQUIRES THERMCO—TWO INDUSTRY LEADERS UNITE

A new competitive force in the semiconductor equipment industry was formed on July 12. Silicon Valley Group (SVG) and Allegheny International announced that they have signed a letter of intent for SVG to acquire Thermco Systems, a subsidiary of Allegheny. This acquisition reflects an on-going trend toward consolidation within a maturing semiconductor equipment industry as well as a continuation of SVG's strategy to grow its business and diversify its product line by acquisition. Thermco is a world leader in horizontal-tube furnace technology. This, combined with SVG's vertical-tube furnaces and its Anicon line of LPCVD reactors, provides SVG with an important new avenue of opportunity to become a major world supplier in furnace technology, and augments SVG's present position as a world leader in photoresist processing equipment.

As shown in Table 1, SVG's acquisition of Thermco would more than double its sales of wafer fab equipment to the semiconductor industry. Based on combined sales in 1986, the SVG/Thermco organization would have placed eighth in Dataquest's ranking of semiconductor equipment companies by worldwide front-end equipment sales. SVG/Thermco now offers the following products: photoresist processing (track) equipment, horizontal and vertical tube diffusion and LPCVD furnaces, the Anicon LPCVD reactor, and high-pressure oxidation furnaces. While all the 1987 data are not yet in, Dataquest expects that SVG/Thermco will rank among or near the top ten wafer fab equipment suppliers in 1987.

Table 1

SVG and Thermco Equipment Sales
(Millions of Dollars)

	1986	1987
Silicon Valley Group		
Track Equipment	$25.6	$33.0
Vertical Thermal Reactor	0.3	2.3
Anicon LPCVD Reactor	8.8	4.7
Total	$34.7	$40.0
Thermco Systems		
Horizontal Diffusion Furnaces	$32.5	$41.0
Horizontal-Tube LPCVD Equipment	7.5	7.8
Total	$40.0	$48.8
Combined Sales	$74.7	$88.8

Source: Dataquest
July 1988

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STRATEGY FOR GROWTH

Over the years, SVG's main product offering for the semiconductor industry has been focused on track equipment. SVG is the largest U.S. manufacturer of track equipment and is a worldwide leader in this area. However, as part of a strategy to grow its business, SVG diversified its product line in February 1986 with the introduction of the Vertical Thermal Reactor (VTR) system for diffusion and LPCVD processes. To further the company's expansion program, SVG entered into an agreement with AG Associates in March 1986 to acquire this manufacturer of rapid thermal processing equipment; however, merger discussions were terminated in June 1986.

The subsequent acquisition of Anicon in February 1987 provided SVG with additional process technology and personnel in the fast-paced arena of LPCVD. SVG has been quietly building a strong cadre of CVD experts in order to position itself to take advantage of the high growth opportunities in the CVD market.

One of the important aspects of the Thermco acquisition is that SVG now can offer customers both horizontal and vertical thermal processing equipment. The horizontal-tube furnace has been the workhorse of the semiconductor industry since its inception, and, consequently, there is a huge installed base of furnaces. The new vertical furnaces, however, are seen as an alternative thermal technology, and future fabs will most likely use a combination of horizontal and vertical furnaces. Although more than ten manufacturers already have introduced vertical furnaces (mostly in Japan), SVG/Thermco is very well positioned to fight for the leadership in the horizontal and vertical furnace market.

THERMCO ON THE BLOCK

Allegheny International announced its intention of selling Thermco in 1987. This is part of the Pennsylvania-based corporation's program of divesting units unrelated to its consumer durables business, which includes small household appliances, electric blankets, outdoor furniture, and barbecue grills. Allegheny signed a non-binding agreement to sell the furnace manufacturer to its chief competitor, BTU Engineering, in April 1988. Less than two months later, however, the plan was abandoned in response to objections from the Department of Justice because of potential antitrust violations.

DATAQUEST CONCLUSIONS

Dataquest considers SVG's acquisition of Thermco to be an excellent opportunity for both corporations. SVG acquires the technology, equipment, personnel, and customer installed base of one of the world's major suppliers of horizontal-tube furnace equipment. Thermco, in turn, has been matched with a new parent corporation that complements its existing product line with little redundancy. It is also an excellent example of a synergistic consolidation that will benefit the U.S. semiconductor equipment industry and strengthen the industry against foreign competition. Terms of the Thermco acquisition have not been disclosed, but Dataquest understands that the proposed transaction would involve a cash purchase.

Peggy Marie Wood
Joseph Grenier

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Research *Bulletin*

SEMS Code: 1987–1988 Newsletters: July
1988–21
0000815

EUROPEAN SILICON STRUCTURES
QUICK–TURN PROTOTYPING WITH DIRECT–WRITE e–BEAM LITHOGRAPHY

Direct–write e–beam lithography has been relegated to a niche market because of the advances in optical lithography. That niche market is actually two markets: direct–write e–beam for fine–line (nanolithography) applications that cannot be met by optical lithography and direct–write e–beam for quick–turn prototyping and small–volume ASIC devices. Because masks are not required, turnaround times are lessened and costs are reduced for low volumes. Thus, the maskless feature of e–beam is the most important factor, rather than the geometries of ASIC devices, which are well within the limits of optical lithography.

This bulletin reports on European Silicon Structures (ES2), a start–up company whose strategy is centered on the use of direct–write e–beam lithography to produce ASIC devices. With an eye toward the future of e–beam lithography, Dataquest believes that ES2's e–beam activities warrant our clients' attention.

THE COMPANY

ES2 was founded in 1985 specifically to provide quick–turn prototyping and low–volume ASIC devices. ES2 can provide 2–micron prototype devices with a four–week turnaround; this should be compared with the industry average of a 10– to 12–week turnaround for 2–micron standard cells. The main reason for this shorter turnaround time is the use of direct–write e–beam lithography instead of conventional optical lithography, which requires the fabrication of photomasks.

ES2 is using Perkin–Elmer AEBLE–150 e–beam systems to fabricate devices with 2–micron geometries and plans to migrate to a 1–micron process. The AEBLE–150 has the capability of writing 0.5–micron lines, so the scaling down can be done easily with the AEBLE–150.

United Silicon Structures (US2), a subsidiary of ES2 located in San Jose, California, was founded in September 1987. US2 will set up a foundry relationship with a company in the United States, but the name of the company has not yet been disclosed. Designs from the United States are currently sent to ES2's fab in Rousset, France, for fabrication, but this adds two weeks to the turnaround time.

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THE PROCESS

In Europe, device fabrication is done at ES2's $40 million Rousset Technology Centre, a Class-10 and below, 125mm wafer facility. The fab is designed for quick turnaround of low volumes in the range of 10 to 10,000 devices. For high volumes, ES2 has an agreement with Philips, whereby Philips will provide high-volume production from its five manufacturing locations in the United States, Europe, and the Far East.

Two AEBLE-150s are operating at Rousset; a third will be installed by the end of the year. US2 also has an AEBLE-150, which is undergoing refurbishing at Perkin-Elmer; it will be installed at a yet undisclosed facility in the United States.

ES2 started fabrication in 1987, using the Philips 2-micron CMOS process. By the end of September 1988, ES2 will have fully qualified a 1.5-micron process and will start production of 1.5-micron ASICs by fall. ES2 expects to implement a 1.2-micron process by the first quarter of 1989 and a 1.0-micron process by the third quarter of 1989. The Philips CMOS process uses epitaxial wafers and is a double-metal, 13-mask level, n-well process. All 13 levels are done on the AEBLE-150.

ES2 has noted no significant yield difference between optical (mask) lithography and direct-write e-beam lithography for 2-micron geometries, but it has noted a yield improvement with e-beam for 1.5-micron geometries. A throughput of 6 to 12 layers per hour is being obtained on the AEBLE-150, depending upon device complexity.

Direct-write e-beam lithography allows not only fast turnaround, but also the fabrication of several devices on the same wafer. Since a typical quick-turn prototype order is initially for 10 devices, and as device yields are good, several customer designs can be fabricated simultaneously on a 125mm wafer. ES2 fabricates four, and sometimes six, different designs on the same wafer, depending on die size and number of parts required. Thus, the cost of manufacturing each customer's design is minimized. Note that the different designs on the wafer can have different die sizes.

In addition, ES2, working closely with several universities, has fabricated a wafer with 28 different designs on it. This wafer, called the fast-turnaround multiproject wafer, allows undergraduates in their final year to design, fabricate, and test ICs. Because of the fast turnaround, it allows them to go through the design cycle realistically more than once.

For electrical test and probe, ES2 has two schemes. There are nine test die located on the wafer; electrical test is performed on these die between metal 1 and metal 2. After metal 2, only a rough device die sort (3-pin probe) is performed for high pin count and low-volume devices; full probe is not done. All device die, good and bad, are then assembled and packaged. Die sort then takes place at final electrical test. The objectives of this technique are faster turnaround and lower cost, since probe cards do not need to be made for each of the designs. For low pin count and high-volume devices, full probe on the device die is done, according to the conventional procedure, and only the good die are assembled and tested.

Joseph Grenier

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Research *Newsletter*

SEMS Code: 1987–1988 Newsletters: July
1988–20
0000705

SEMICON/WEST 1988 EQUIPMENT SURVEY

The SEMICON/West Equipment and Materials Exposition is held annually in San Mateo, California. This industry trade show is sponsored by the Semiconductor Equipment and Materials Institute (SEMI) and is a yearly milestone for the semiconductor equipment and materials vendors. Each year, Dataquest surveys the wafer fabrication equipment vendors and reports on significant new products and enhancements introduced at the show. The results of the survey are published in this annual newsletter.

INTRODUCTION

This year's show was reminiscent of SEMICON/West 1983. At that time, the industry was recovering from a deep recession, and the vendors' enthusiasm was as strong as the healthy and rising bookings of the recovery. This year's show is the result of a healthy and sustainable expansion, not like SEMICON/West 1984, at which artificially inflated demand for capital equipment brought process engineers out in droves—and in one short year's time, brought on the worst downturn the equipment industry has ever experienced.

Nor was this year's show like last year's, where there was a preponderance of "tire kickers," with no real budgets behind them. This was an orderly crowd with genuine interest in buying equipment with value rather than equipment for capacity's sake. There was no doubt that the recovery had arrived.

However, unlike the recovery of 1983/1984 when all equipment vendors participated in the boom, not all equipment companies have participated equally in the boom. This was one of Dataquest's themes at its annual SEMICON/West Seminar, held in conjunction with the show. Those companies that had best managed their businesses during the recession by better product planning, market planning, and control of expenses, are now being rewarded with higher market shares. New market leaders are emerging from this recovery and are replacing some of the previous market leaders. This recovery is more sustainable than previous recoveries; it and its new set of market leaders may represent a new and more mature phase in the development of the semiconductor equipment industry.

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SEMI's official attendance count was 47,288 attendees this year, compared with 45,089 last year. This does not include the approximately 15,000 attendees from exhibitor companies who freely roamed the show as they networked and performed their own "market research." The conspicuous comment that characterized this year's attendees was that their "quality" was very high; that is, these attendees looked like they wanted to buy something, and, in many cases, did buy something.

Dataquest was also particularly interested in Japanese company participation in this year's show. In recent years, Japanese equipment companies have dominated their home market and have also begun to increase their shares in the United States and Europe. As shown in Table 1, the number of Japanese companies at SEMICON/West is quite extensive. For a complete description of new product introductions by Japanese companies, please read the appropriate equipment sections throughout this newsletter.

Table 1

Japanese Companies at SEMICON/West

	Equipment Type			
Company	Front-End	Assembly	Test	Inspection
Ando Electric			X	
Anelva	X			
Canon	X			
Dainippon Screen	X			X
Disco Abrasive		X		
Holon/KLA				X
Horiba				X
Japan LSI/Kamatsu-Gosho		X		
JEOL, U.S.A.	X			X
Mitsui Contek				X
MTC/Okura	X			
NEC America		X		
Nikon Precision		X		
NSA Hitachi Scientific				X
Olympus				X
Shinkawa		X		
Sumitomo Heavy Industries	X			
TEL/Sagani/Varian	X			
TEL/Kyushu/Varian	X			
Tokoyo Seinitsu			X	
Tylan/Tokuda	X			
Ulvac North America	X	-	-	-
Total	10	5	2	7

Source: Dataquest
July 1988

Another salient feature of this year's exposition were the many new product introductions and product enhancements. While many of these new products were truly "new" systems, most of the improvements were invisible to the casual observer. These invisible new product enhancements involved innovations at the operations level that dealt with cleanliness, operator friendliness, process management, reliability, ease of maintenance, and productivity. It appeared that the R&D investment of the last few years is entering a refinement phase, as semiconductor manufacturers become serious about using the new technologies in production.

Because of space considerations, we can give only a brief overview of the products and technologies. For further information, please contact the manufacturers directly. By referring to previous years' SEMICON/West newsletters, the direction in technological trends and in product development can be seen very clearly.

LITHOGRAPHY

The key stepper developments were in new lenses and improvements in various aspects of registration, much as they were last year. This is to be expected, as lens resolutions continue to increase, the stepper manufacturers have to improve the registration of their machines in order to take full advantage of the resolution gains.

Perhaps nothing better depicts the relationship between resolution and registration than an example that ASM Lithography uses in one of its application notes. ASM compares theoretical die size for a 256K SRAM for three processes: a 1.25um minimum linewidth with 0.45um registration, a shrink to 1um with 0.45um registration, and a shrink to 1um with 0.25um registration. The resulting die sizes are 94 mm^2, 77 mm^2, and 42 mm^2 respectively. Obviously, smaller die size means higher yields, lower product cost, and lower capital equipment expenditures. Improvements in resolution tend to grab all the limelight, but clearly, improvements in registration are just as important.

Not much was said about excimer laser steppers at the show. Last year, it seemed that excimer laser steppers would be used for 0.5-micron lithography, but this year there was talk by some stepper manufacturers of pushing conventional optical lithography to reach this level. Neither was there much activity in X-ray lithography, as the advances in conventional and excimer laser optical lithography have slowed down developments in the X-ray area.

Activity in e-beam was limited to high-resolution, direct-write lithography, as several companies introduced enhancements to their fine-line e-beam systems to better address the nanolithography market. There were no significant developments in the areas of maskmaking e-beam or "low-resolution" direct-write e-beam.

The most significant lithography product expected at SEMICON/West this year was Perkin-Elmer's step-and-scan aligner, since it had been widely rumored for some time prior to the show that Perkin-Elmer would finally introduce it. This did not happen, and Perkin-Elmer has been very quiet and reticent to discuss the program.

In summary, the scene in lithography was subdued, as there was little activity in X-ray, and improvements in e-beam were confined to a very small niche market. In optical steppers, there were the usual new lenses and registration improvements (this is not to minimize the importance or the technical and manufacturing challenges involved in these advancements). This lower-than-usual level of new product activity in lithography was in contrast to the heightened level of activity now taking place in deposition equipment.

Steppers

Like last year, the key developments in the stepper area were in lenses and enhancements to existing steppers to improve their performance. In lenses, four companies, American Semiconductor Equipment Technologies (ASET), ASM Lithography, GCA, and Perkin-Elmer (PE), were pushing i-line lenses. ASET and ASM use the same Zeiss 0.40 numerical aperture (NA) i-line lens, GCA's i-liner has a NA of 0.35, and Perkin-Elmer is developing a 0.42 NA i-line lens. There are, however, i-line lenses being developed that have NAs above 0.42.

The Japanese stepper manufacturers, Canon and Nikon, have not been so aggressive in marketing i-line technology. Canon, which has not yet marketed an i-liner, continued its evolution of g-line lenses with the introduction of a new 0.48 NA g-line lens. Nikon is developing an advanced i-line lens, but has not released any information on it.

ASM marketed a new metrology package for its stepper. ASET, Canon, GCA, and Ultratech all introduced improvements in their steppers, resulting in new stepper model numbers for these four companies.

American Semiconductor Equipment Technologies

ASET introduced a new stepper in its 900 SLR Series, the 958 i-line stepper, which incorporates the Zeiss 10-78-58 i-line lens. The 10-78-58 5X lens has an NA of 0.40, a 21.1mm-diameter field size, and a working resolution of 0.7 micron. The 958 is priced at $1.3 million, and first deliveries occurred in January 1988. ASET recently announced that it had received an order from Integrated Device Technologies for eight 958 steppers. Dataquest believes that in the future, ASET will introduce a 0.48 NA i-line lens.

In addition to the features described above, the 958 SLR incorporates various other improvements: a new reticle-masking blade assembly, an improved i-line illumination system that gives better spectral purity, a new air-bearing stage with magnetic compensation, a bright field/dark field microscope with automatic switching, and a new magnification control system.

ASET has also added another g-line wafer stepper in its SLR Series, the 961 SLR, which incorporates a Zeiss 10-78-61 5X g-line lens. This lens has a numerical aperture of 0.43, a 21.2mm-diameter field, and a working resolution of 0.81 micron. Altogether ASET now offers seven steppers—four g-line steppers and three i-line steppers—all of which use Zeiss lenses. Please see last year's newsletter, "SEMICON/West 1987 Equipment Survey," SEMS Code: 1987-15, for a listing of the five previously offered steppers.

ASET has also augmented its 600 Series Image Repeaters (photorepeaters), which are used in the manufacture of 1X full-field masks, with the addition of a fourth model, the 648 Image Repeater. The 648 incorporates a Zeiss 10-78-48 10X i-line lens with a 13mm-diameter field and 0.7-micron resolution. With a stepping repeatability of 0.1 micron (3 sigma), the 648 can make high-precision, submicron 1X masks by optically stepping the 10X die image instead of writing the entire 1X mask on an e-beam system, which can take three or four hours of expensive e-beam time. A key feature of the new image repeaters is the new metrology package that allows perfect grid matching. The 600 Series Image Repeaters range in price from $830,000 to $900,000; the first system will be delivered shortly.

ASM Lithography

ASM exhibited the PAS 2500/40, which it first introduced at last year's SEMICON/West. The PAS 2500/40 uses a Zeiss 10-78-58 i-line lens with an NA of 0.40 and a resolution of 0.7 micron over a 20mm-diameter field size. Depth of focus at 0.7 micron resolution is 2.2 microns on average. The PAS 2500/40 is priced at $1.3 million.

ASM showed the performance of the 10-78-58 lens for sub-0.7-micron geometries and displayed scanning electron microscope (SEM) photographs with resolutions down to 0.5 micron. The performance of advanced i-line lenses coupled with the excellent overlay accuracy of the PAS 2500/40 stepper (99.7 percent of measurements less than 0.15 micron, global alignment) leads ASM to believe that optical lithography (nonexcimer laser) will eventually reach 0.5 micron and that excimer laser-based steppers will not be needed until 0.35 micron.

ASM also has a new metrology software package for its steppers that facilitates the measurement and matching of overlay performance between the various steppers on the production line.

Further, ASM introduced an enhanced version of the 2500/10 called the 2500/15. The 2500/15 has dual input and output cassettes and a 450-watt illuminator instead of the 350 watts used for the 2500/10. In addition, a dedicated microprocessor for stage motion and a faster software algorithm have reduced alignment overhead time by 40 percent.

The price of the 2500/15 is $1,125,000, compared with $975,000 for the 2500/10. A 2500/10 can be purchased and then later upgraded in the field to a 2500/15 if desired.

Canon

Canon introduced an improved version of its FPA-1550 Mark II stepper that incorporates a new high-speed reticle changer and a new higher-speed wafer-handling system. These two improvements can be either ordered as options on new factory systems or retrofitted in the field.

The new reticle changer can accommodate 10 reticles, each in its own dust-free cassette, and can change reticles in 17 seconds. Other features include dual pellicle capability, a bar code reader, and an optional reticle inspection system. Canon also discussed using automatic guided vehicles for reticle movements in the fab area.

The new backside-contact-only wafer-handling system replaces the belt transfer system previously used on the Mark II stepper. Features of the new pick-and-place system include an X, Y, and theta wafer prealignment stage, optical detectors for wafer centering, and flat/notch detection by CCD devices. The new system is two to three times faster than the belt system and contributes only three particles greater than 0.5 micron per pass on a 150mm wafer.

Canon also announced the FPA-1550 Mark III stepper, which incorporates as standard equipment the new high-speed reticle changer, the new pick-and-place wafer-handling system, and the new UL-11 lens. The UL-11 lens has switch-selectable numerical apertures of 0.48 and 0.43. Previously, Canon had offered a similar variable aperture lens of 0.43 and 0.35 numerical aperture for the FPA-1550MII. The UL-11 is a 5X, g-line lens with a 21.2mm-diameter field and a distortion of less than 0.08 micron. At the 0.48 NA setting, it has a production resolution of 0.7 micron, with a 1.5-micron depth of focus at 0.7-micron lines and spaces.

Other features of the Mark III stepper are 200mm wafer capability, an optional high-speed reticle changer that can accommodate 14 reticles, and an off-axis alignment system in addition to the dark field and light field alignment systems. FPA-1550 MIIIs will be available in Japan starting the second half of 1988, and in the United States, the first quarter of 1989.

Canon is also developing a new g-line lens, the UL-X, which will have a NA of 0.45, a resolution of 0.75 micron, and a 20mm-square field size. It will be available in early 1989.

GCA

GCA introduced its advanced lithography system, the ALS Waferstep 200. This system can handle 200mm wafers and has a more reliable stage than GCA's Model 8500 stepper. The ALS Waferstep 200 uses the company's Maximus 2000 light source that can be operated either in a continuous illumination mode or in the flash mode to provide greater intensity, and hence, a shorter exposure time. The lens used is the Tropel 2235i, the same that was offered on the Model 8500 stepper. This 5X i-line lens has a NA of 0.35, a 22mm-diameter field, and a resolution of 0.7 to 0.8 micron with depth of focus of 2 microns. The ALS 200 can also use g-line lenses, although the bridge and column are different than the 8500.

Registration is 0.2 micron (3 sigma) in the local alignment mode using the through-the-lens dark field alignment system and 0.3 micron (3 sigma) in the global alignment mode. The company's SMART SET metrology package has been improved and made standard on the ALS 200. This software package includes metrology, self diagnostics, data monitoring, and wafer history software. It is also used to facilitate the measurement and matching of registration between production steppers.

In addition to the 2235i, Tropel has under development an i-line lens with a NA of 0.45. Dataquest believes that even higher numerical aperture i-line lenses are being developed by GCA.

First shipments of the ALS Waferstep 200 occurred in the third quarter of 1987.

Nikon

Nikon did not introduce any new lenses or significant enhancements to its stepper line this year. Instead, the company chose to focus on new equipment offerings in the areas of wafer, photomask, and reticle metrology and inspection. More will be said about these new products later in the "Process Control" section of this newsletter.

Concerning other developments, however, Nikon officially changed its company name from Nippon Kogaku K.K. to Nikon Corporation as of April 1, 1988. Also as of April 1, Nikon established a new organization in Europe called Nikon Precision Europe (NPE) GmbH, located in Dusseldorf, West Germany. This new organization will be responsible for the marketing, sales, and service of all of Nikon's semiconductor products in the Western European countries. Nikon plans staff and equipment additions in Europe to increase its capability for demonstration, training, and application engineering. Engineering staff will also be added to augment its present capabilities for stepper installation and maintenance.

Previously, there was a small staff of Nikon people in Dusseldorf to support the company's semiconductor products in Europe. The establishment of a separate organization there to better address the European market is parallel to Nikon's organization in the United States, Nikon Precision Inc. (NPI). As a point of reference of the extent of service support currently available in the United States, NPI offers an Uptime Guarantee service agreement whereby it guarantees 93 percent uptime for steppers. The agreement also provides a two-hour response time, optional six- or seven-day coverage, and the optional assignment of a NPI field service engineer on-site.

Perkin-Elmer

Perkin-Elmer did not introduce any new lenses or significant enhancements to its Micrastep line of steppers. PE did, however, announce it is developing a new i-line lens called the I-42, which should be available at the beginning of 1989. This lens, which will be manufactured by PE, has an NA of 0.42, a 27mm-diameter field (17mm square), and a depth of focus of $\pm$0.75 micron at a resolution of 0.6 micron. PE has not yet specified the production resolution of the lens, but it will be less than 0.8 micron.

Ultratech

Ultratech introduced the Model 1500 stepper, which is an improved version of the Model 1100. Improvements include a new digital alignment system, which provides a better alignment signal for difficult metal layers; a new magnification compensation system that uses a thermal chuck to heat wafers to compensate for magnification changes; and an improved system for isolating wafers from vibration sources.

Ultratech also introduced two-row capability for 1X reticles. Previously, Ultratech steppers could only access one row of 1X fields on a reticle. Now, two rows of fields can be accessed on the same reticle, and switching time from any one field to any other field in the two rows takes only about five seconds. Each row in the reticle can have from three to seven different fields, depending on field size. For instance, for a field size

of 15mm X 15mm, five fields can be placed in one row. The advantages of two-row reticles include a reduction in cost and the capability of placing multiple die layers on the same reticle. Thus, it is possible to completely personalize a gate array with one 1X reticle.

The 1500 uses the 4035 variable aperture lens that Ultratech introduced last year. Also, all of the above enhancements can be retrofitted to field steppers. Price of the 1500 is $1.2 million, and deliveries are expected to begin in the latter half of 1988.

Concerning future developments, Ultratech believes that its stepper can reach sub-0.5-micron resolutions with the deep UV output from conventional mercury sources; Ultratech is, however, keeping a close eye on developments in excimer laser sources.

X-Ray Lithography

Activity in X-ray lithography was minimal this year; no equipment was exhibited, and only three companies had anything to say about this technology. Notably absent from the show were Cosy-Microtec, a West German company developing a compact SOR source for X-ray lithography; and Hampshire Instruments, an X-ray stepper manufacturer that last year introduced its first product, the XRL 5000 stepper.

Cosy-Microtec had exhibited a mock-up of its compact SOR source at the Leybold-Heraeus booth for the last two years at SEMICON/West, but this year there was no one available to even discuss the product. Subsequent to SEMICON/West, Dataquest has learned that the Cosy-Microtec project has been disabled. Perhaps this lack of activity reflects the recent advances in optical lithography; these developments have the effect of moving out the market window for X-ray lithography.

Canon

Canon had a single display panel showing a 4:1 reduction X-ray exposure system that uses an SOR source and a stepper in which the wafer is held in a vertical position. Interposed between the SOR source and stepper is an X-ray mirror optics system that holds the reticle in a vertical position and provides the 4:1 exposure reduction. Canon has targeted this system for 1993.

Canon also had a display panel showing its lithography expectations. The 4Mb DRAM is expected to be built with g-line steppers in 1988, the 16Mb DRAM is expected to be built with excimer laser steppers in 1991, and X-ray steppers are expected to be used to build the 64Mb and 256Mb DRAMs in 1994 and 1998, respectively.

Karl Suss

Karl Suss had an excellent video describing the West German cooperative X-ray program and Karl Suss's involvement in it. The program began in 1979 and now is using five dedicated beam lines on the big West Berlin synchrotron orbital radiation ring, BESSY, for the study of X-ray lithography. Karl Suss has provided two prototype X-ray steppers to the cooperative, and these steppers have been in use at BESSY since 1984. In 1987, Suss installed at BESSY its new XRS-200 X-ray stepper, which was introduced at last year's SEMICON/West show.

BESSY has been used to manufacture devices in which the critical layers are exposed by X-ray lithography. AEG-Telefunken has fabricated a silicon tetrode with 0.6- to 1-micron gate lengths, with a 90 percent yield for the 1-micron device. IHT Aachen, in conjunction with the Fraunhofer Institute (the steering organization for the cooperative), has fabricated 0.3-micron gate length silicon MOSFETs, and Siemens has fabricated 0.25- to 0.5-micron gate length gallium arsenide MESFETs.

The cooperative has extensively studied X-ray maskmaking, and currently, silicon carbide with tungsten absorber and silicon with gold absorber appear to be the most promising technologies. Mask distortions are approaching 0.1 micron, and no major technical hurdles are foreseen for continued improvement. Masks with features as small as 0.25 micron have been written using a three-level resist; working masks have been made from the masters by X-ray replication using a single-level resist. The video mentioned that the most important aspect of X-ray maskmaking technology will probably be mask defect detection and repair. Using the Suss prototype X-ray stepper, wafer-to-wafer alignment accuracy of 37nm (one sigma) has been obtained.

Suss also introduced the LSX-10 plasma point source for use with the XRS-200 stepper. This is a low-intensity source of X-rays that can be used for R&D studies of photoresists, maskmaking, and X-ray process. The effective X-ray intensity of the LSX-10 is 0.1 to 0.5 mJ/cm^2/pulse; this translates into a 10-minute or less exposure time (in contrast, exposure time using the Cosy compact SOR source would be about a second). The emission wavelength of the LSX-10 source is 0.7 to 1.2 nanometers.

Sumitomo Heavy Industries

Sumitomo introduced to the United States its Aurora compact synchrotron orbital radiation (SOR) X-ray source at SEMICON/West. The Aurora was first introduced last December at SEMICON/Japan, and was described in SEMS newsletter number 1988-3, "SEMICON/Japan 1987 Equipment Highlights." Please refer to that newsletter for more information on the Aurora.

E-Beam Lithography

This year, activity was pretty much restricted to direct-write rather than maskmaking e-beam, and even in direct-write, developments were concentrated in the high-resolution area. Production applications of high-resolution e-beam lithography include gallium arsenide devices, quantum well devices, FETs, and X-ray mask fabrication. The minimum feature sizes in these applications are dropping from 0.25 micron to less than 0.1 micron (quantum well devices require 200 angstrom lithography). Accordingly, e-beam manufacturers are improving their fine-line systems to be able to do nanolithography, which is less than 0.1 micron with sufficient production throughput. (Note: (0.1 micron = 100 nanometers = 1,000 angstroms).

Thus, the direct-write market actually consists of two niche markets; the "low-resolution" direct-write market typified by the Perkin-Elmer AEBLE-150 and JEOL JBX-6AIII and the high-resolution market typified by the nanolithography systems. These two application segments have always coexisted in the e-beam market, but now seem to be dividing into two very distinct markets as the equipment becomes more specialized to meet the requirements of low- and high-resolution e-beam lithography.

The e-beam manufacturers are not fundamentally rebuilding their tools to do nanolithography, but are essentially improving the performance by increasing the signal-to-noise (S/N) ratio of the tools and better characterizing the existing machines. Ways of increasing the S/N ratio include higher accelerating voltages, better signal-processing software, and sources that provide more electron current.

ASM Lithography

ASM Lithography markets the EBPG-4 Beamwriter e-beam system manufactured by Philips in Holland. At SEMICON/West this year, ASM introduced the new Philips EBPG-4HR, which is a high-resolution version of the EBPG-4 specifically intended for nanolithography. The EBPG-4HR has a maximum scan field of 800 microns, a 12nm beam spot size, and a minimum beam deflection step of 5nm. In contrast, the EBPG-4 has a maximum scan field of 1,600 microns, a 25nm spot size, and a 25nm step size. The price of the EBPG-4HR is $2.4 million; first shipments will be made in the United States this year.

Cambridge Instruments

Cambridge is also improving its EBMF 10.5 e-beam system for nanolithography. The EBMF 10.5 accelerating voltage has been increased to 40kV, and improved software has been added for better S/N ratios.

JEOL

JEOL has introduced some new enhancements to increase the throughput of its JBX-5DII high-resolution e-beam direct-write lithography system. New is a thermal field emission source (TFE) that provides a current density of 1,000 amps/cm^2 at a 25kV accelerating voltage, compared with a previous current density of around 10 amps/cm^2. Also, the data rate for the JBX-5DII has been upped from 2 MHz to 6 MHz. The faster JBX-5DII configured with the new source is called the JBX-5DII (TFE) and is priced at about $2.5 million, compared with $2.0 million for the standard JBX-5DII system. First deliveries for the JBX-5DII (TFE) are scheduled for 1989.

For data editing, JEOL has introduced a verification software package, that runs offline on a VAX workstation. The software package takes the JEOL-formatted data tape (after data conversion from the pattern generator or GDS-2 format) and converts the data into the actual physical patterns to be written on the wafer. An operator can view the patterns on a color monitor and can edit the data as required. The software package is presently available only for the JBX-5DII series.

For the JBX-6AIII, a fairly recent enhancement is the BX-SPA63 Shot Partition Accelerator (SPA) software/hardware package. The SPA is used for the real-time partitioning of large feature patterns (trapezoids, rectangles, triangles, up to 2.5mm X 2.5mm), into smaller 12.5-micron by 12.5-micron patterns. Previously, the partitioning was done at the data preparation stage and was included on the input tape to the JBX-6AIII. Now, however, the data tape includes only the large features; the partitioning is done in real time at the JBX-6AIII. Advantages of this include more efficient use of the data memory and data transfer time.

Perkin-Elmer

Perkin-Elmer did not introduce any new enhancements to either the MEBES III maskmaking e-beam system or the AEBLE-150 direct-write e-beam system.

Concerning the AEBLE-150, PE has received additional orders from Raytheon (for writing gallium arsenide wafers) and Thomson in France. PE has two AEBLE-150s operating at European Silicon Structures (ES2) at Rousset, France. ES2 is using the AEBLE-150s to do quick-turn prototyping and small volume lots (less than 5,000 chips). ES2 has been fabricating full-custom chips with a 2-micron, double-metal, 13-mask level, CMOS process on 125mm wafers, but is now in the qualification stage for a 1.5-micron process. All layers are written with the AEBLE-150.

ES2's normal procedure is to write four designs per wafer; it has written as many as 28 different devices on a single wafer. Turnaround time for full-custom, quick-turn prototypes is four weeks.

AUTOMATIC PHOTORESIST PROCESSING EQUIPMENT

Silicon Valley Group and Solitec exhibited new systems at the show this year that highlight advances in contamination control and process control monitoring. In addition, Dataquest notes that three Japanese track manufacturers—Canon, Dainippon Screen, and TEL—are now actively marketing their track systems in the United States.

Silicon Valley Group

Silicon Valley Group (SVG) introduced its new beltless track system, the SVG-8800 ATS (Arm Transport System). The 8800 ATS incorporates an advanced wafer transport system as a standard feature into SVG's 8600 Series of track process modules. The ATS can be utilized between any two of the processing modules in the 8800 ATS Series; modules include coater, developer, scrubber, hot plate, vapor prime, vacuum bake, multiple hot plate, SOG coater, U-turns, and stepper/aligner interfaces. Reduced contamination was an important priority in the design of the 8800 ATS Series. The mechanical/electronic housing of the arm system, as well as the moving arm itself, are enclosed and can be exhausted so that any particles generated by internal moving parts can be removed before wafer contamination could occur. In addition, all of the moving mechanisms of the arm system are below the wafer plane. Prices can range from $80,000 for a simple coat module up to $300,000 for the full coat/expose/develop system. Although the 8800 ATS system was introduced at SEMICON/West in May, SVG first started demonstrating the system for customers at the beginning of 1988. To date, multiple systems have been shipped to customers in the United States.

Solitec

Solitec exhibited its Series 10000 track system that includes real-time process monitoring systems for film thickness measurement and develop end-point detection. The Series 10000 is a 200mm-compatible system and entirely modular in design.

Standard components include the Autocoat coating module, the Optimist development module, and two process control monitors: the Autoscan and the Optiscan. The Autoscan monitor has been designed for in-line measurement of photoresist thickness, while the Optiscan is targeted at develop end-point detection. Solitec believes that in-line process control is an effective strategy for tracking process variations in real time so that if any problems arise, they can be identified and corrected promptly. Both process control monitors rely on optical measurement techniques. The Autoscan and Optiscan were first introduced at the end of 1987 and are available on other Solitec track systems in addition to the Series 10000. Solitec began shipping the Series 10000 in March 1988.

Japanese Track Companies Look to the United States

This year marked the emergence of Japanese track manufacturers—Canon, Dainippon Screen, and TEL—at SEMICON/West. To date, these companies have had minimal penetration of the U.S. market with their track products. However, Japanese equipment companies have recognized that they must place increased emphasis on markets outside of Japan as a part of any long-term strategy for growth. Dataquest believes visibility at U.S. trade shows like SEMICON/West, along with U.S.-based marketing, sales, and service offices represents a new Japanese competitive aspect within the U.S. track equipment market. (Note: Tazmo, a Japanese manufacturer of track and spin-on-glass systems, has been represented by Semix in the United States since 1984.)

Canon

While Canon had a prototype of its CDS-650 Coater/Developer system at last year's show, this year the company displayed the full system. Canon's initial marketing focus for this product in the United States is to market it in conjunction with its stepper.

Dainippon Screen

Dainippon Screen (DNS) displayed information on its D-Spin 629 track equipment and photoresist asher (PAS 812), in addition to exhibiting its spin etcher (for wet etch processing) and film thickness measurement systems. As part of its effort to increase penetration of the U.S. market, DNS opened an office in Santa Ana, California, last October, and signed an agreement earlier this year with Prism Technologies for Prism to market DNS track equipment on the West Coast.

TEL

TEL displayed its photoresist coater/developer system, the Clean Track Mark II, in the Varian booth. Through a recent marketing agreement, Varian is now the exclusive distributor of TEL's track equipment in the United States, the United Kingdom, and Europe.

ETCH AND CLEAN

Wet Process Stations

Wet process stations are undergoing rapid technological changes as the semiconductor industry marches off to ever smaller geometries, and thus ever smaller defect–causing particles. Because of these demands, it is imperative that wet chemicals not only must start out pure, but they must also maintain their purity during use. Chemical usage must be done in a safe manner, and, after use, chemicals must be disposed in an environmentally safe manner. To meet these needs, wet chemical process systems have responded in a variety of ways, all of which were shown at this year's SEMICON/West.

Some wet system manufacturers are monitoring and maintaining low particulate levels in their chemicals. Others are recirculating their chemicals or developing less costly and safer processes that are also environmentally safer. Finally, most wet system manufacturers have embraced robotics to transfer wafers within wet process stations.

Athens Corporation

Although Athens did not have a booth at SEMICON/West it is in the process of introducing two new products, as well as an upgrade to another product, the Piranha Piranha system. The first new product is the Towel Vapor Dryer, which, Athens claims, cleans wafers without adding contaminants. The Towel consists of a vaporizer unit in the drying chemical that repurifies and reuses the condensate. A second unit, the regeneration module, removes water and further repurifies and regenerates the drying chemical. It operates independently of the dryer and can be scaled to provide both cost and/or space flexibility. Athens also claims that waste and disposal costs are eliminated due to its regeneration process.

The average selling price for the Towel system is $100,000. The Towel features a safe, no–flashpoint vapor drying process. The dry rate for this process is the same as for IPA, but Athens claims that it is safer than IPA because of the no–flashpoint chemical used. The system also has a closed–loop purification distribution network capable of delivering clean chemical automatically to multiple dryers from a single regeneration unit. The Towel system can be integrated into conventional wet benches. First shipment was scheduled for June.

The second new product Athens has developed is an HF Reprocessor. Acid repurification in this product is based on ion exchange coupled with filtration. Application of the product tool is for interfacing with any tube or quartz cleaner; a similar HF system is planned for wafer cleaning. Average price of the HF is $275,000; it is scheduled to ship this month.

Athens also has introduced the second generation of its Piranha Piranha wafer cleaning system. With this upgrade, the system now has less than 5 ppb for particles greater than or equal to 1 micron in size, less than 10 ppb for particles greater than or equal to 0.5 micron in size, and less than 200 ppb for trace elements. MTBF is 500 hours; MTTR is less than 4 hours; MTBA is 168 hours. Output is greater than or equal to 0.6 liter per minute, which Athens hopes to increase to 0.7 to 0.8 liter per minute.

Average selling price for the Piranha Piranha system is $375,000. Athens reports that shipments of this system to new customers began in the second quarter of this year.

Dexon

Dexon showed the Omega 110 robot in its wet station system. The Omega 110 is capable of operating in a Class 10 environment and features an expansion movement rather than a flex movement in order to use less space.

FSI International

FSI officially released three new wet-bench products at SEMICON/West: the EXCALIBUR Gas Processing System, the FSI Vapor Dryer, and the Mercury Acid Processing System.

FSI has been market testing its EXCALIBUR Gas Processing System previous to SEMICON/West, and officially introduced it at this year's show. The EXCALIBUR uses anhydrous HF and water vapor to remove native oxide for a particle-free surface. Process applications for the EXCALIBUR include presilicide clean, pregate clean, polysilicon deglaze, preepitaxial clean, preinitial oxidation clean, BPSG and other doped oxide deglaze, and controlled etch back. FSI claims that the EXCALIBUR adds less than five 0.5-micron particles per 150mm wafer.

FSI also introduced the FSI Vapor Dryer. The FSI Vapor Dryer has a unique tank-within-a-tank design. This design enables the unit to keep the isopropyl alcohol much purer than conventional systems do. FSI claims that the unit has extremely low particle levels and leaves a residue-free surface. The system also uses remote heat as a safety feature.

Additionally, FSI introduced the MERCURY Acid Processing System. The MERCURY represents FSI's new generation of acid processors. It was specifically designed to be both cost efficient and space efficient to allow for the needs of ASIC manufacturers. The MERCURY is an automated system with high reliability, featuring an improved rotating union, turntable, and bowl design.

Typical cleaning or treatment applications for the system include: prefurnace, pre-CVD, postash, pre-MOCVD, premetal, preimplant, and pre-epi. Additional applications include photoresist stripping and oxide and deglaze etches.

Polyflow Engineering Inc.

Polyflow showed its Accuetcher Automatic Spray Processing System. The average selling price of the Accuetcher is $75,000.

Polyflow claims that its Accuetcher, which uses choline, provides superior particle counts to RCA clean processes. Polyflow also claims that the waste chemical from its system presents no disposal problems and can be disposed of without treatment.

The Accuetcher has a high flow rate of 3 gallons per minute and its rinser/dryer can operate at variable speed and with bidirectional rotation. Polyflow claims to have shipped six units to date.

Pure Air Corporation

Pure Air showed the Cosmo System 5 wet station system. The System 5 features a back-load Cosmo II robot and can integrate up to 67 stations. An internal programming feature as an option allows the changing of processing parameters as required. Each station has its own timer/controller for each process. Processes available include etch/stripping, plating, cleaning, ultrasonics, spin rinse/dry, and degreasing. The average selling price of the System 5 is $105,000.

Santa Clara Plastics

Santa Clara Plastics introduced its Model 8400 Robotic Wet Process System. This system is a fully automatic, fully software-supported SECS II-compatible robotic transfer system that has been designed to accommodate a wide range of processes. The 8400 can operate in Class 10 environments and can handle any of the wet chemistry immersion processes. The system features an automatic chemical dispenser that will shut the tank down, drain it, cool it, and flush it, and then fill and heat the tank. It also has automatic diagnostics that can exercise a valve or relay in order to diagnose a problem.

SCI Manufacturing

SCI Manufacturing introduced three new wet station products. The first is the SCI 4505 Robotic Wet Process Station. The 4505 can be configured by process engineering personnel to perform any sequence of wet process operations without operator intervention. The 4505 uses SCI's TRANSort Optimization Software (TRANSOS). TRANSOS allows process engineers to define multiple operational recipes that allow the same station to perform several different functions. Any recipe can be initiated at any time, and several different recipes can be active at the same time. TRANSOS allows up to 10 product carriers to operate simultaneously. The 4504 is SECS II compatible.

SCI also introduced the SCI 3400 Chemical Pumping System. This system provides continuous monitoring and automated delivery of high-purity process liquids. It is used for automated controlled delivery of process chemicals to liquid process equipment. Systems range from standalone pump stations to integrated systems.

Additionally, SCI introduced the SCI 4650 Intelligent Gas Cabinet. This cabinet provides for intelligent containment and control for high-purity toxic gases. The cabinet provides a high-purity manifold, automated operation, and continuous safety monitoring. It can be used as a completely standalone cabinet or integrated into a larger system. The system provides automated purge cycles, safety interlocks, and user customization capabilities.

Semifab

Semifab showed its AT 6000 system. The 6000 is designed for Class 10 clean rooms and incorporates megasonic cleaning. The system can handle multiple processes simultaneously, and can accommodate automatic chemical fill. All system electronics are housed in a separate cabinet that can be situated in a remote location in relation to process cabinetry.

Semitool, Incorporated

Semitool introduced the Auto Cell, which it claims is the industry's first single-wafer processor to perform an RCA clean. The unit is fully automated and is capable of handling both 150mm and 200mm wafers.

Semitool also showed an automated etch station as a new member of its Spray Acid Tool family. The automated etch station features a small footprint and has unicabinet construction. It includes an input WIP station, a PUMA robotic wafer handler, a spin/rinse/dry station, a process chamber, and an output WIP station. The etch station can also be rear-accessed for easy service.

Verteq

Verteq introduced the Sunburst cleaning system, which is a megasonic system for removing submicron particles. The Sunburst has no moving parts, a small footprint, and uses 50 percent fewer chemicals than Verteq's nonmegasonic System.1600 rinser/dryer. Selling price for the Sunburst is $8,500—or $12,000 with automation.

DRY ETCH AND STRIP

Technology is rapidly advancing in this processing category. Several approaches, each vying for share of a number of processing segments, are being implemented by several different companies. In this section, we will focus on dry etching and dry stripping.

Dry Etch

This equipment category is one of the richest for technical evolution. Three inventions are competing for acceptance as the "single-wafer" solution to anisotropic etching. This is happening in an environment where Applied Materials continues to carve out increasing market share year after year with its batch (hexode) systems. But single-wafer evangelists are undaunted as electron-cyclotron-resonance (ECR), triode, and magnetically enhanced etching continue to advance.

ECR

Nippon Telephone and Telegraph (NTT) Laboratories developed ECR for both deposition and etch in 1978. This technology has been licensed by several companies including Sumitomo Heavy Metal in Japan and, in the United States, by Materials Research Corp. Recently, Lam Research Corporation (LRC) formed an alliance with Sumitomo to market the Japanese system in this country.

In 1986, CNET (Centre National D'Etudes Des Telecommunications) and CNRS (Centre National de la Recherche Scientifique), both French governmental research agencies, developed a unique method of achieving the ECR effect. Their technology employs eight microwave antennas located in the horizontal plane on the periphery of a large electrode. Located at each of these antennae are alternating positive and negative magnetic poles. This configuration creates eight electromagnetic cusps near the electrode periphery where the ECR conditions exist. These cusps become the source of an intense plasma, several orders of magnitude greater than conventional plasmas. The wafer, which resides in the center of the electrode, can be electrically biased to achieve different etch parameters. This technology decouples the plasma from the wafer surface, allowing a degree of freedom that is not available with contact plasmas. The technology has been licensed to Electrotech and CIT/Alcatel.

Triode

In 1983, GCA Corporation (now General Signal/GCA) introduced the Model 606 Dry Etcher. It uses the triode configuration. Since then, Tegal has introduced its version of the triode, the Model 1500. These products will be described under the appropriate company headings below.

This technology essentially decouples the wafer from the plasma by creating another current path through the plasma that bypasses the wafer. The effect is to "pump-up" the ionization ratio (and also the number of reactive neutrals) without increasing the voltage on the wafer. This allows high etch rates at low pressures, the conditions that favor anisotropic etching in single-wafer chambers.

GCA and Tegal each approach the technology slightly differently. GCA uses a third electrode that sits at ground potential with respect to the plasma and is located between the upper and lower electrodes. The power is pumped into the plasma above the grounded electrode, isolating the plasma from the wafer that sits on the bottom electrode. High densities of reactive neutrals are formed and drift through the grounded electrode to the wafer surface. The wafer is then biased with a low-energy RF voltage in order to create a low-energy plasma that will achieve the etch conditions necessary for the process.

Tegal does not employ a third electrode, but rather, uses the grounded walls of the chamber as the grounded current path. The power is pumped into the upper electrode and the wafer on the lower electrode is biased with RF voltage.

Magnetically Enhanced Etching

Two companies have previously attempted this technology, MRC and Tokuda. They used static magnetic fields, which gave them problems with etch uniformities. Recently, a rotating magnetic field has been used as advocated by IBM Corporation in its technical literature. This technology has been further developed and refined independently by Anelva and Applied Materials.

The technology uses four electromagnets configured evenly around a single-wafer chamber. The phase of the AC power to these magnets can be offset to create a rotating magnetic field between the magnetic poles (i.e., within the chamber). During an etch process, the wafer will see the time integral of the magnetic field, creating extremely uniform etch conditions. The plasma is not decoupled from the wafer, but current voltage conditions can be varied somewhat by varying the voltage to the magnetic field. The magnetic field creates an extremely intense plasma enabling high etch rates at low pressures with low substrate bias.

Dry Etch Companies

Applied Materials

Applied introduced its Precision Etch 5000 (PE-5000) magnetically enhanced plasma etcher. This system uses the same configuration as the Precision Deposition 5000 that can house two to four chambers around a central vacuum chamber. The system uses the magnetic enhancement principle described above. The basic system was first employed in the deposition system as a planarization etch chamber in a multistep deposition process.

The PE-5000 has been configured as a standalone etcher and targets single-crystal silicon, primarily deep trench etching, as its first application. Prices for the system range from $800,000 (two chambers) to $1.3 million (four chambers).

This system's configuration illustrates the advanced nature of Applied's integrated vacuum processing development (see the "Integrated Vacuum Processing" section of this newsletter). This single-wafer, multichamber configuration is being used in production in CVD, and now, with the PE-5000, in dry etching.

CIT/Alcatel

CIT/Alcatel has licensed the microwave technology from CNET described earlier. The company has incorporated it into its RCE 160. This is a two-chamber system that can be configured with several processing sequences (using RIE, planar plasma, and ECR). The system price ranges from $800,000 to $1 million depending on configuration. There are three systems in beta testing in France, Germany, and Japan.

Electrotech

Electrotech has also licensed the microwave technology from CNET and offers R&D versions of the technology in its MPM 390. The technique has not been incorporated into the production model but will be available for delivery in October 1988. The first applications will be for single-crystal silicon and GaAs.

Plasma-Therm

Plasma-Therm introduced its version of a multichamber system, its Model 2130. It is capable of housing three chambers; this combines the advantages of batch throughput with single-wafer control. The system price is $550,000.

Tegal

Tegal showed its new oxide etcher, Model 1530. The system is load-locked and employs a single frequency, 13.5 MHz. The price is $350,000.

Dry Stripping

Photoresist stripping equipment has been a very "low-tech" processing area for many years. It is routinely done by wet dunking or by plasma in very simple barrel reactors. Since the increase in the use of high-current implantation for CMOS source/drains and reactive ion etching (RIE) for very large scale integration (VLSI), semiconductor manufacturers have had problems with very tenacious resist residues. This is because the high energy of the above processes bakes the resist, rendering it very resistant to removal.

To solve this problem, single-wafer strippers have been developed. These have been reported in previous years' SEMICON/West newsletters. Process development for these systems has centered on trying to reduce the C-V shifts and the threshold voltage reduction that results from the residual ionic contaminants that remain embedded in the substrate after the resist removal. While many of the companies selling these systems claim that they have solved the problem, there has not been an avalanche of orders for this technology. It may be that the semiconductor manufacturers are not quite convinced. There were two new innovations in the single-wafer stripper area this year.

Branson/IPC

Branson's introduced a single-chamber system, the Model L-3300, priced at $90,000 (including pump). This system operates at 13.56 MHz and is automatically loaded. It uses an remote oxygen plasma as the reactive species. The resist removal rate is 1.0 to 2.0 microns per minute depending on the process. This would yield a throughput of approximately 30 wafers per hour for a 1-micron resist.

General Signal/Drytek

Drytek introduced its single-wafer stripper at last year's show. This year, the company introduced a version whereby the stripper has been integrated into its quad system. This is important because it gives a semiconductor manufacturer the ability to strip without leaving the vacuum environment. This application will find immediate

usage after RIE etching because of the tenacity of the resist residue, and after aluminum etching because of the potential for corrosion if subjected to atmosphere. It is General Signal's first foray into integrated vacuum processing (IVP) technology. (See the "Integrated Vacuum Processing" section of this newsletter.) With its various operating companies and divisions, General Signal has the processing expertise and the equipment configuration (Drytek) to be a significant player in this area.

DIFFUSION AND TUBE CVD

This section of the SEMICON/West newsletter contains new product and feature information for horizontal and vertical tube diffusion furnaces. It also discusses the associated low-pressure CVD (LPCVD) processes and the horizontal tube plasma-enhanced CVD (PECVD) equipment.

Horizontal Tube Systems

New equipment activity in this area was very slow this year, with only one new piece of equipment exhibited in the diffusion/LPCVD area and one in the PECVD area. Dataquest noted some new activity in the robotic area and some new retrofit and feature options being offered.

ASM America

ASM had no new equipment introductions in the horizontal tube area; however, the company exhibited a Class 10 clean room robot model TT4000SC by Seiko. This robot was attached to a ASM model SF-50 small-footprint, single-tube PECVD system. This robot can be added to systems in the field for $150,000. The price for the CVD system and robot together is $375,000. Cleanliness for this robot is Class 10 at 0.11 micron using a Hitachi laser system for particle measurement. The CVD system and robot can process 100mm, 125mm, 150mm, and 200mm wafers. ASM claims to have more than one of these systems/robots in production on 200mm wafers and a total of six installed in the United States. The systems in production on 200mm wafers are depositing Si_3N_4 films 1,612 angstroms thick with uniformity of ±2.8 percent.

BTU Engineering

BTU offered no new equipment in this area. It did, however, offer two new options that can be added to new equipment or as a retrofit into installed BTU systems. One option/retrofit is called the Cross Flow System and the other is called the Fast Cool Core.

The Cross Flow System is designed to provide higher-quality LTO, PSG, and BPSG interlayer dielectric films in a horizontal tube LPCVD system. Instead of introducing the gases from one end of the tube, the gases are introduced evenly from beneath the boat using load-end injectors. The reacted gases are exhausted perpendicular to the axis of the wafer load. This method ensures one pass of unreacted gas over the entire load. This price of this option/retrofit is $140,000 per tube. An increased deposition rate of 150 to 300 angstroms is achieved with a full wafer load. Film uniformities average ±3 percent across the wafer, from wafer to wafer, and run to run. Particulate level within the process chamber is reduced due to the elimination of wafer exposure to by-products of the reacted gases.

The Fast Cool Core is designed to provide rapid cooling of furnace loads in a controlled atmosphere. Two concentric quartz tubes create a double-walled tube. This tube has an air space between the walls and a manifold at each end to supply and remove the cooling air. The price of this option/retrofit is $30,000 per tube. It offers rapid cooling in controlled and uncontrolled modes (up to 25°C per minute). Wafer motion is not necessary during cooldown, thus reducing particulate generation.

Pacific Western Systems (PWS)

Pacific Western introduced a new zero-stress nitride process for its Model 560-PC horizontal tube PECVD system. Like the Applied Materials and Novellus CVD systems to be discussed later, the 560-PC uses two power supplies in order to control the stress of the deposited nitride film. In the PWS system, however, the zero-stress nitride film is made by depositing alternating compressive and tensile layers of nitride; the stress and proportional thickness of the alternating layers determine the overall stress outcome of the film.

Price of the 560-PC configured for zero-stress nitride is $480,000, including the personal computer and cantilever loading system.

Tempress

Tempress has now appended its APCVD and LPCVD offerings with the new OMEGA-5000 series PECVD horizontal tube system. The 5000 is available now, though so far, no units have been shipped. The cost per PECVD tube is $250,000, and the system can be supplied in single-tube through four-stack configurations. This system has been developed for the deposition of silicon nitride layers using SiH_4, NH_3, and N_2 as the process gases. The deposition rate is 300 angstroms per minute with the film thickness typically falling between 500 and 15,000 angstroms. The 5000 can also be set up with a mixture of PECVD, LPCVD, and/or diffusion tubes. The cost per LPCVD tube ranges from $100,000 to $250,000, while the cost per diffusion tube ranges from $40,000 to $200,000. Load size ranges between between 20 and 68 wafers, with three tube lengths available. Tube diameters are available to process 100mm, 125mm, 150mm, and 200mm wafers. This system is equipped with a Class 10 laminar flow load station and can be purchased with a Wollman loading robot. Tube level controls can be linked up with local or host computers via SECS I and SECS II protocol. This system is equipped with a Class 10-compatible flat panel touch screen display for real-time system status information.

Thermco

The Automation Compatible Furnace Module (ACFM) is Thermco's robotic compatible diffusion and LPCVD system. The system has been built to very tight tolerances and the frame of the furnace has been reinforced. Precision quartz and element positioning reduce the need to recalibrate the robot after each tube change due to tube position variance. The thermocouples go in one way to reduce the need for recalibration after replacement, and adjustable feet eliminate the need for Johnson bars and shims when positioning the furnace on the fab floor. The costs are $250,000 per LPCVD tube and $200,000 per diffusion tube. This system can process 150mm or 200mm wafers. The first shipment will be made to Intel during August.

Vertical Tube Systems

Although, the two vertical processors described below have been previously introduced to the marketplace, they are included in this newsletter because worldwide semiconductor manufacturers are beginning to show more interest in this technology, and we believe that our clients should be aware of what is happening in this area.

Besides the two companies listed below, there is another U.S. vertical furnace manufacturer, Tempress. However, it did not exhibit any products, and it is not clear what the future of the Tempress vertical processor is going to be. In addition to the three U.S. vertical processor vendors, there are now eight Japanese vendors offering vertical processors, although none of the Japanese products were exhibited at the show. Please refer to SEMS newsletter number 1988-3, "SEMICON/Japan 1987 Equipment Highlights," for a description of the Japanese vertical processors.

Semitherm

Semitherm exhibited its Advantage 801A vertical thermal processor. In this system, the wafers are placed on a stationary quartz pedestal and then the cylindrical quartz process chamber, previously in the up position, is lowered over the pedestal and sealed against a base plate. The sealed process chamber allows either vacuum or controlled atmosphere processing. After the quartz process chamber is lowered, the outer bell jar and heating element are lowered over the process chamber. After processing, the concentric outer bell jar and quartz process chamber are independently raised; this is what Semitherm calls the double-lift system.

Wafers are processed in quartz boats that hold them in a vertical position; the boats can accommodate either 25 or 50 wafers depending on wafer spacing, which can be either the standard 3/16 inch or 3/32 inch. Two boats can be loaded, one above the other, on two horizontal stationary quartz pedestals. Thus, process load size can range from 50 to 100 wafers, depending upon the number of boats used and the slot spacing. The uniform temperature zone is a volume 14 inches in height by 9 inches in diameter, sufficient to accommodate two quartz boats of 150mm wafers. Semitherm has also said that wafers can be "coin stacked"; that is, processed in the horizontal position.

Currently, the quartz boats must be manually placed on the quartz pedestal; Semitherm will, however, automate the system.

For thin-gate oxides in the range of 50 to 250 angstroms, typical performance is better than 2 percent. Polysilicon and nitride processes are also available, and typical performance for a polysilicon film with a 50-wafer load is 2 to 3 percent.

Silicon Valley Group (SVG)

SVG exhibited the SVG-6000 Series Vertical Tube Reactor. This system accommodates up to nine cassettes of 150mm wafers, six cassettes of product wafers, and three cassettes of test or filler wafers in a Class 10 staging area. A pattern of product, test, or filler wafers can be programmed. A single-wafer backside handling system transfers the wafers from the cassettes to a vertical quartz tower (boat)

in the staging area while another batch of wafers is being processed in a second quartz tower in the vertical reaction chamber. Whereas in the Semitherm vertical processor the process chamber is lowered over the stationary wafers, in the SVG system the quartz tower is raised into a stationary process chamber. Also, in the SVG system, the wafers are placed horizontally in the quartz tower.

Load size (150mm product wafers) is 150 wafers for diffusion/oxidation processes and 100 to 150 wafers for LPCVD processes. For 200mm wafers, four cassettes of product wafers and one of test or filler wafers can be accommodated.

For thin-gate oxides in the range of 50 to 200 angstroms, guaranteed performance is a range of ±3 angstroms within a wafer, wafer-to-wafer, and run-to-run; typical performance is ±6 angstroms. For gate oxide films, the quartz boat is inserted and withdrawn in a nitrogen environment. LPCVD processes available include silicon nitride, flat temperature polysilicon, and liquid-source TEOS oxide films. Guaranteed polysilicon film uniformities on 150mm wafers are ±2 percent within a wafer, ±3 percent wafer-to-wafer, and ±2 percent run-to-run.

SVG guarantees 10,000 wafer transfers without an operator assist, and typical handling system cleanliness is 0.01 particle/cm^2 larger than 0.3 micron. SVG also will guarantee, for the polysilicon process, a 50 percent reduction in particle densities over conventional horizontal furnaces or any other vertical reactor.

Prices range from about $120,000 for a basic anneal system to $250,000 for a fully loaded TEOS LPCVD system. SVG has approximately 30 systems in the field.

Chemical Vapor Deposition

This year, most of the advances in nontube, or dedicated, CVD equipment were made in the area of process development rather than in new equipment introductions. The reason for the lack of new equipment introductions is simply that the key equipment in this area has only been introduced in the last year or two and is just now beginning to be installed for production use. Significant equipment introductions included the Genus 8700 series, the Plaser 8701, and the Varian 5103. All of these new models are primarily for the deposition of selective tungsten and tungsten silicide.

In the process area, progress continues to be made in interlayer dielectrics, planarization, and CVD selective tungsten. Progress in this area is extremely important, as it is the key to the multilevel metalization that will be required in advanced devices. Perhaps nothing better puts into perspective the subject of chip interconnection, which includes interlayer dielectrics, planarization, selective tungsten, and metallization, than IBM's recent statement that for its multilevel chips more than half of the cost of manufacturing the wafer occurs in chip interconnection.

Passivation films are also receiving attention as both Applied Materials and Novellus introduced stress-controlled nitride films, and previously in the newsletter, we mentioned that Pacific Western has also introduced a zero-stress nitride film.

Two of the systems, the Applied Materials Precision 5000 and the Varian 5103, are multiple independent-chamber systems, and thus, are capable of doing integrated vacuum processing. Here we see CVD systems migrating toward integrated vacuum processing; this is one approach. On the other hand, companies making sputtering equipment are also introducing multiple-chamber systems in their bids toward integrated vacuum systems. Varian's new M2000 is a multiple-chamber sputtering system. Thus, Varian is going at integrated vacuum systems from both directions.

Applied Materials

Applied announced two new processes for its Precision 5000 CVD system that was introduced at last year's SEMICON/West.

One of the new processes is an improved silicon nitride film for device passivation. Traditional difficulties with nitride passivation films include high nitrogen content, which can cause accelerated aging in short-channel MOS devices; high compressive stress, which can cause voids in the underlying aluminum layer; and low UV transmission, which prevents nitride from being used as a passivation film in EPROM devices. The Precision 5000 can deposit a low hydrogen content film, can vary deposition parameters to select the film stress desired, and can deposit a film that is fully transparent to UV light, thus allowing its use in passivating EPROM devices.

The other new process is a plasma-enhanced deposition of BPSG using TEOS and silane sources. Usually, BPSG films are deposited by atmospheric pressure or low-pressure chemical vapor deposition, which, Applied claims, are relatively porous and hygroscopic. Also, the maximum boron content of these conventional films is limited, which puts a limit on the lower glass flow temperature. Applied's plasma BPSG process provides a denser film that is stable at high dopant concentrations, and thus, has reduced flow temperatures. Applied also said that BPSG films deposited from a TEOS source have better as-deposited step coverage and better slope after reflow than conventional BPSG films.

CVC Products

CVC announced at the show that it had just signed an agreement to market the Plasmox 1 and Plasmox 2 PECVD systems, manufactured by Plasmos GmbH of West Germany, in North and South America.

These systems are pancake-type reactors for the deposition of oxide, nitride, amorphous silicon, and oxynitride films, and are primarily intended for R&D and pilot line use. The Plasmox 1 is a manually loaded system that can process three 100mm wafers, while the Plasmox 2 can be either manually loaded or provided with the option of cassette-to-cassette with SMIF boxes. Wafers in both systems can be processed with the active side either up or down. Gas flow is laminar across the susceptor.

Plasmox 1 is priced at $200,000; Plasmox 2 is priced at $300,000. There are no systems yet installed in the United States.

E.T. Electrotech

Electrotech exhibited the ND6210 plasma-enhanced CVD system, which was first introduced at SEMICON/Europe in March. The ND6210 is an improved version of the ND6200 PECVD system and offers an optional continuous deposition process for either oxide or nitride films (previously, only oxide was offered in a continuous process) and an optional TEOS process, in addition to a silane oxide process. TEOS films can be deposited at 300°C temperatures. Other enhancements include an improved chamber and a longer time between chamber clean, which essentially has doubled the throughput for nitride films on 150mm wafers.

The ND6210 costs $550,000. CVD systems currently being built are ND6210 models.

Electrotech is developing a single-wafer, multiple-chamber PECVD system based on its Omega 2 technology, which may be introduced at SEMICON/East this September. Like Applied Materials' Precision 5000, Electrotech's new system will provide interlayer dielectric planarization with etchback, do a chamber clean after every wafer, and have the capability of attaching up to four process chambers.

This system will also be Electrotech's entry into the area of multivacuum processing, as the process chambers can be either CVD, reactive ion etch, ECR etch, sputtering, or rapid thermal processing (RTP). Note that Electrotech is already well positioned technically for multivacuum systems, as it already has systems on the market to do all of the required processes (in separate equipment) except RTP, which is currently under development.

Focus Semiconductor

Focus did not introduce any new enhancements to its F1000 system, but did indicate the in-situ capability of the F1000 for multistep processes. An example of such a process to provide a special planarized dielectric is a three-step deposition sequence consisting of a 2,500-angstrom LTO first layer; followed by a 1.4-micron BPSG layer; followed by a 2,000-angstrom, 11 percent PSG third layer; and finally, a 20-minute reflow in nitrogen at 850°C. All steps were in-situ, and the final result was a completely planarized film.

Focus also announced that it has entered into a distributor agreement with Nissin Electric to market the F1000 in Japan.

Genus

Genus exhibited the 8700 series cold-wall CVD reactor. This is a continuous-feed batch reactor that processes six wafers at a time. Dual input cassettes are individually loadlocked; while the 8700 is processing wafers from one cassette, the other cassette in its loadlock is being pumped down. Wafers are continuously transferred one at a time from the cassette into the process chamber; as a wafer completes its process, it is transferred back into the cassette and another wafer immediately takes its place.

The 8700 series is available in three models. The 8710, which was introduced at last year's SEMICON/West, is for deposition of tungsten silicide; the new 8720 is primarily for the deposition of selective and blanket tungsten but can also deposit tungsten silicide; and the new 8700PC can deposit all three films.

The 8710 and 8720 systems have six wafer chucks in the reaction chamber. The 8700PC is specifically intended for R&D applications and has only a single chuck, but it can be upgraded in the field to either a 8710 or 8720 system. The idea is to provide a lower-cost R&D and development tool for the development of a process and then be able to transfer the process directly to the production line using the same piece of equipment. Using the same tool for process development and production minimizes the time to transfer a process into production.

The 8710 and 8720 systems are priced between $825,000 and $900,000; the 8700PC is priced at $630,000.

Lam Research

Lam has an agreement to market Sumitomo Metal Industries' line of ECR equipment in North America and Europe, and accordingly, it exhibited Sumitomo Metal's EC-3000 bias ECR CVD system.

The EC-3000 is a single-wafer, cassette-to-cassette system. It is designed to deposit an in-situ planarized layer of oxide for interlayer dielectrics. In normal ECR CVD, 2.45-GHz microwave power combined with a magnetic field is used to generate the plasma for conformal deposition of oxide. In bias ECR, additional 13.56-MHz power is applied to the wafer and argon is introduced so that simultaneous plasma deposition and argon sputter etch occurs; the result is a planarized oxide layer. Sumitomo Metal has said that the EC-3000 can planarize 0.5-micron features with 3:1 aspect ratios.

Deposition rate is 2,500 to 3,000 angstroms per minute during planarization. Deposition temperature is typically less than 100°C, and ion energies are about 20eV. Throughput for a 1-micron film is about 15 to 18 wafers per hour. Currently, the EC-3000 has only a single chamber; in the future a second chamber will be added to increase the throughput.

Price of the EC-3000 is $1.1 million to $1.2 million.

Novellus

Novellus exhibited the Concept One PECVD system, which it had exhibited last year. New developments include a process to control stress and hydrogen content in the deposition of silicon nitride films by varying RF bias. This is accomplished by applying low-frequency 450-kHz power to the wafer susceptor while simultaneously applying 13.56-MHz power to the upper electrode. Stress and hydrogen content of the film can be controlled by varying the split of high- and low-frequency power between the upper and lower electrodes.

Novellus also has developed a low-temperature (400°C) plasma TEOS process. The Concept One, however, does not use heated bubblers, but instead, pumps the liquid TEOS source directly to the reaction chamber, where the TEOS is evaporated into a gas distribution box, which is at the same pressure as the reaction chamber. Hence, no heating of the TEOS source is required. Up to three different liquid sources can be used, and combinations of the sources can be mixed in a mixing unit before being pumped to the chamber. For instance, a liquid source could be used to dope the TEOS film with phosphorous to improve step coverage.

Plaser

Plaser, a company founded in 1983, introduced its first product in the area of deposition equipment, the 8701 selective tungsten deposition system. The 8701 is essentially identical to the company's first product, the 8600 system for the dry etching of gallium arsenide; only the active chemistry in each is different.

Both systems utilize Plaser's proprietary molecular beam process (MBP) for either the etching of gallium arsenide or the selective deposition of tungsten. Conventional CVD takes place at relatively high pressures; MBP deposition takes place at lower pressures (10^{-5} to 10^{-4} torr), where the reactant gas flow is in the molecular beam flow region. The same reactive gases are used in the 8701 as in conventional CVD. Plaser, however, claims that the MBP reaction is more efficient, and that the quality of the MBP tungsten film is superior to a conventional CVD tungsten film.

The 8701 is a cassette-to-cassette multichamber system that can accommodate from one to five individually pumped reaction chambers arranged around a central wafer handler. Input and output cassettes are loadlocked, and wafers are transferred, one at a time, from the input cassette to the central wafer handler where the wafer is transferred to one of the five process chambers. The chambers can be used for different process steps such as wafer clean, preheat, etch, or deposition. Selective tungsten deposition rate is 1,000 angstroms per minute; uniformity is ±5 percent on a 150mm wafer.

A single-chamber 8701 is priced at $400,000; a five-chamber system is $1 million. First shipments are expected to occur at the end of 1988.

Spectrum CVD

Spectrum exhibited the Model 211 through-the-wall production system, which is designed for CVD deposition of blanket and selective tungsten and tungsten silicides. Previously, the 211 used a three-wafer loadlock; now, however, the 211 uses the same wafer-handling system as that used on the Tegal 1500 etcher. Wafers are transferred one at a time from the input wafer cassette to a single-wafer loadlock, where they are then transferred into the reaction chamber. On the output side, there is also a single-wafer loadlock feeding the output cassette.

Wafers are transferred through the system active side down. In the single-wafer, cold-wall reaction chamber, which has a volume of less than one liter, the wafer is positioned active side down against the underside of a quartz plate. Radiant heaters heat the wafer through the quartz window and the backside of the wafer. Process gases are introduced below the wafer, and deposition occurs on wafers with the active side down. Spectrum says that advantages of this type of chamber include the prevention of backside

deposition; a short reactive gas flow path, which minimizes gas depletion effects; and the assistance of gravity in preventing particle-induced contamination from occurring on the wafer. An RF plasma can also established in the chamber for the purposes of chamber cleaning or wafer pretreatment.

Spectrum has developed a silane reduction process for selective and blanket tungsten films. Typical deposition rates for silane-reduced selective tungsten films are in the range of 2,000 to 6,000 angstroms per minute, depending upon deposition parameters.

Dataquest believes that shipment of the first Model 211 is imminent. Spectrum has shipped several of the Model 202 manual systems, which are intended for R&D applications.

Varian

Varian exhibited the Model 5103 single-wafer production CVD system that was first introduced at SEMICON/Japan last December. The 5103, designed for deposition of blanket and selective tungsten and tungsten silicide films, was a joint development project between Varian and TEL/Varian. The 5103 will be built both in Japan and in the United States.

The 5103 consists of three independent, vacuum-isolated, cold-wall chambers arranged in the horizontal plane around a pumped-down central wafer handler. Input and output cassettes are placed in loadlocks, and a transfer arm moves the wafers from the input cassette, one at a time, to a three-wafer storage buffer. Another transfer arm in the central wafer handler moves each wafer from the three-wafer buffer into any one of the three process chambers. After processing, the wafers are transferred back to the three-wafer buffer, and thence, into the output cassette in the output loadlock. Wafer transfer is done active side down.

Processes include silane-reduced deposition of selective and blanket tungsten films, and deposition rates of 10,000 angstroms per minute have been obtained for selective tungsten. Either low-temperature silane-reduced or high-temperature dichlorosilane-reduced tungsten silicide films can be deposited.

Dataquest believes that the process chambers on the 5103 and the M2000 are interchangeable. Thus, the 5103 is capable of multichamber vacuum processing and could be used for a deposition process sequence such as selective tungsten followed by aluminum sputter.

The 5103 is priced at $1.1 million to $1.5 million and first shipments will occur in October.

Watkins-Johnson (WJ)

WJ's advancements this year were in the processing area. For the APCVD deposition of oxide and PSG, WJ is now using disilane (Si_2H_6) instead of silane. Advantages of disilane include safety and improved step coverage at lower deposition temperatures. Oddly enough, disilane is more pyrophoric than silane. Whereas the autoignition concentration of silane in air is about 2 percent, for disilane it is ten times less than this. For a gas leak with silane, the concentration would build up to the

autoignition point, and then an explosion would occur. For disilane, this would not occur, as the gas would start burning almost right away.

WJ also has a new APCVD process that deposits a BSG interlayer dielectric film that is almost completely planarized. The film is deposited in a thick layer (1.6 microns), is planarized as deposited, and requires no flow at elevated temperatures after deposition as do PSG and BPSG films. BSG films have excellent step coverage, very smooth surfaces, and excellent void-filling characteristics. Use of BSG as an interlayer dielectric is a new application; concerns raised about it include moisture problems and boron's efficacy as a getterer.

BSG deposition temperature is around 360°C, and for a 1.6-micron film, throughput is about 60 wafers per hour on WJ-999 double-wide APCVD reactor. Because of the three-head design of the WJ APCVD systems, the first 1,500 angstroms of the film can be deposited at temperatures as low as 250°C to suppress hillocks. Deposition at the other two heads would be done at higher temperatures for more optimum step coverage and deposition rate.

PHYSICAL VAPOR DEPOSITION

The physical vapor deposition (PVD) equipment segment includes sputtering and evaporation technologies. This year at SEMICON/West, it became clear that companies are pursuing two different strategies in the development of next-generation PVD equipment. While one group of companies is focusing on traditional PVD system technology, a second group is developing integrated vacuum processing systems that will eventually provide a variety of vacuum process capabilities on a single system, such as sputter, CVD, etch, and RTP. In this portion of our newsletter, we will discuss new equipment introductions and enhancements from Anelva, CHA Industries, Eaton, Gryphon Products, Temescal, and Varian.

Anelva

Anelva did not exhibit any equipment this year, but did introduce to the U.S. market the ILC-1051 and ILC-1551 single-wafer, in-line multichamber systems that it first introduced last December at SEMICON/Japan.

Whereas other manufacturers are just now introducing their first individually pumped, vacuum-isolated multichamber sputtering systems, the ILC-1051 is a second-generation system, following Anelva's first product in this area, the ILC-1015 sputtering system. Among other differences, the ILC-1015 used belts for wafer transfer, while the ILC-1551 uses pick-and-place-type transfer.

The ILC-1051 employs four individually pumped, vacuum-isolated chambers arrayed in a horizontal plane around the perimeter of a central wafer-handling chamber (Anelva calls it a separation chamber). The central wafer-handling chamber is pumped down and isolated from the input wafer cassettes via a loadlock that can accommodate 50 wafers. Wafers are transferred with the active side down, and the wafers are processed in a vertical position.

The ILC-1051 can be used either in series for multistep processing or in parallel for higher throughput. A typical serial, multistep sputtering process would be the deposition of a titanium nitride (TiN) barrier layer followed by aluminum deposition. For this type of process, RF etch would occur in the first chamber, followed by the sputtering of titanium, nitridization of the titanium, and the sputtering of aluminum in the other three chambers.

For the deposition of aluminum or aluminum alloys in the parallel processing configuration, throughput is 50 wafers per hour for a 1-micron film at a deposition rate of 1.2 microns per minute.

The ILC-1551 is a single-wafer, multiprocess system with three chambers arrayed horizontally around a central wafer-handling chamber. Process chambers that can be used include aluminum sputtering, metal CVD, and ECR deposition of a silicon dioxide interlayer dielectric. A typical multiprocess sequence might be RF etch, followed by selective tungsten to fill the contacts, followed by sputtered aluminum. The ILC-1551 is intended for R&D and small volume production. The ILC-1051 and ILC-1551 have both been designed with the same concept so that new processes developed on the ILC-1551 can be used in volume production on the ILC-1051.

Both the ILC-1051 and ILC-1551 are priced in the range of $1.8 billion to $2.0 million. Dataquest believes that as of June, no systems had been shipped.

CHA Industries

CHA Industries' Mark 40 evaporation system is designed for silicon or gallium arsenide applications. It accepts planetary fixtures or a single lift-off dome, and can be used with up to three electron beam guns as well as with thermal evaporation, sputtering, ion beam, magnetron, and diode sources. The system can be supplied with a source isolation chamber, which allows for loading and unloading substrates while the deposition sources are maintained under vacuum, thus reducing the possibility of source contamination. The reverse process can also be implemented by putting the substrates under vacuum while performing emergency repairs, such as changing the gun filament, in the source chamber. The first shipment will be made in August for GaAs lift-off applications. The price of the Mark 40 is $200,000.

Eaton

Eaton announced that it is developing an advanced single-wafer sputtering system called the Radian.

The Radian employs up to five individually pumped, vacuum-isolated chambers arrayed in a horizontal plane around the perimeter of a central wafer-handling or staging chamber. The staging chamber contains a pick-and-place wafer handler that is used to randomly transfer wafers from the loadlock onto each of the five wafer platens; the platens, one for each chamber, are then rotated 90 degrees to hold the wafer vertically for processing.

Wafer transfer from input wafer cassettes (up to four) to the loadlock is accomplished by a Puma robot that transfers the wafers into a 25-wafer input stack in the loadlock. Transfer is done one at a time by the robot, which is the same type as that used on Eaton's NV-20A implanter. The loadlock is then pumped down to 10^{-7} torr, and the batch of 25 wafers is radiantly heated to 400°C for wafer preheating and outgassing. The wafers are then transferred one at a time by the staging chamber pick-and-place arm, from the input stack onto the five platens in the pumped-down staging chamber.

After processing, the wafers are transferred into a 25-wafer output stack located in a second loadlock. After backfilling of the loadlock, the Puma robot transfers the wafers from the output stack back into one of the four wafer cassettes.

Other features of the Radian include 200mm wafer capability, 10^{-8} torr base pressures, deposition temperatures of up to 550°C, programmable RF bias, and maintaining the central wafer handler at sputtering temperature. For heating the wafer, heat transfer between the wafer and platen is accomplished by argon gas. The chambers can be used either in series for multistep processes or in parallel for higher throughput. For example, a typical multistep metal process might be an RF etch, followed by the sputter deposition of a titanium/tungsten (Ti/W) barrier layer, followed by sputtered aluminum. One module would be for RF etch and two each for the Ti/W and aluminum layers. Throughput would be determined by the throughput of the RF etch module.

The Radian is Eaton's entry into the area of multiprocessing vacuum systems that are just now beginning to emerge in the marketplace. When configured for multiprocessing, one or more of the sputtering chambers will be replaced by RIE, CVD, or RTP modules. Integrated vacuum processing will be discussed in more detail later in this newsletter.

Gryphon Products

Gryphon's Reliance is a derivative of the Horizon, a system that was shown at last year's show. The Reliance uses three sputtering targets in a batch processing chamber. Gryphon designed this system for metal layering, planarization, reactive sputtering, and codeposition. One system has been shipped to Inmos. Throughput is claimed to be 60 150mm wafers per hour depositing 1-micron aluminum alloy. The Reliance has a guaranteed uptime of better than 85 percent. The price of the system is $850,000.

Temescal

Temescal introduced the FCE-2500 evaporator, which is primarily designed for GaAs lift-off processes. This system comes with a source isolation loadlock and a touch-screen control panel that uses a Motorola 68000 MPU, and can be mounted through the wall. The control system can be interfaced through a SECS-II link to a host computer. Substrate fixturing options include a 90-degree angle of incidence, flat, or high-speed planetaries. The system can be equipped with single or multipocket electron beam sources or can be set up with resistance sources. Typical process time for 1 micron of aluminum deposition is less than 10 minutes. Two-inch, three-inch, or 100mm wafers can be processed in the FCE-2500. The price is $300,000.

Varian

Varian made its domestic introduction of the M2000 single-wafer sputtering system that was first introduced to the world at SEMICON/Japan last December.

The M2000, which was exhibited at the show, is a loadlocked system that accommodates three cassettes, each in its own separate, independent loadlock. After pumpdown of the loadlock, the wafers are transferred horizontally one at a time from the cassettes to the central wafer handler via a pick-and-place arm. The wafers are then transferred to one of up to five separate process chambers, where they are processed in a vertical position. The process chambers, which can be for either sputter or RF etch processes, are arrayed in a horizontal plane around the pumped-down central wafer handler. The chambers are individually pumped and vacuum isolated from each other.

The M2000 is a truly modular system—each module is a freestanding unit that is mounted on casters so the chambers can be easily added, removed, or exchanged. Because of the system's modularity, a process chamber can be shut down for maintenance or cleaning while the other chambers continue processing wafers. Thus, the entire system does not have to be shut down, and throughput of the system will only be decreased by the throughput of the shut-down module. The wafer-load module, which includes the three independent loadlocks, can handle 200mm wafers and is the same as the end station used on Varian's new Extrion 1000 ion implanter.

Price of the M2000 will range from $1 million to $2 million depending upon options, although the price of the system configured with one RF etch module and three sputtering modules is $1.4 million. As of June, Varian has booked seven orders for the M2000; the first system is expected to be shipped at the end of July.

The M2000 is currently targeted at multistep metal processes (for example, Ti/W followed by aluminum), but it is also Varian's entry into the multiprocessing vacuum systems that are just beginning to emerge in the marketplace. When configured for multiprocessing, one or more of the sputter modules can be replaced with rapid thermal processing or CVD modules. Integrated vacuum processing is discussed in more detail in the next section of this newsletter.

Integrated Vacuum Processing

Dataquest believes that integrated vacuum processing systems represent a significant trend in equipment development for advanced semiconductor manufacturing. These systems, potentially incorporating etch, sputter, CVD, and RTP processing modules all within the same piece of equipment, may offer several important advantages and alternatives over traditional single-process systems.

As semiconductor device fabrication becomes more and more advanced, the associated cost of the clean room manufacturing environment has risen accordingly. Integrated vacuum processing systems may provide one avenue for reducing this cost by providing a clean room environment within the machine. The general design of the new multichamber vacuum systems has focused on isolated chambers, each with its own

pump. These multiple chambers are arranged around a central wafer-handling mechanism, which is pumped down and isolated from the input wafer cassettes' loadlocks. These factors together help to eliminate cross-contamination between the various processing chambers.

Another important advantage of an integrated vacuum system is their ability to perform sequential processing steps within the same system. This removes the necessity of exposing the wafers to contaminating reactive species, such as water vapor and air, by eliminating wafer transport between different pieces of equipment for some types of processes.

One issue that has not been resolved is whether integrated vacuum processing systems will achieve higher throughput than single-process systems. The answer cannot be readily ascertained because of the complexity of these systems. This, however, will be one of the factors that will be closely examined as semiconductor manufacturers evaluate future equipment requirements.

Company Activities

There are a number of companies in the area of integrated vacuum processing, many of which are discussed in this newsletter. Table 2 identifies the companies that are well-positioned to pursue this new equipment opportunity by incorporating their existing and future technology developments in an integrated system. Dataquest expects this list of companies to grow as integrated vacuum processing emerges as a mainstream technology for advanced device fabrication.

Table 2

Integrated Vacuum Processing
Multichamber Capability

Company	PVD	CVD	Etch	RTP
Anelva	X		X	
Applied Materials		X	X	
Eaton	X			X
E.T. Electrotech	X	X	X	
General Signal	X	X	X	
LAM/Sumitomo		X	X	
MRC/NTT	X	X	X	
Spectrum CVD/Tegal		X	X	
Ulvac	X	X	X	
Varian	X	X	X	X

Source: Dataquest
July 1988

SILICON EPITAXY

We are seeing an awakening of the epitaxy market after a long, long slumber. Because of the lower growth of bipolar devices with respect to CMOS, and because of the reluctance of semiconductor manufacturers to use epitaxy for commodity CMOS fabrication, epitaxial silicon capacity has been excessive. It has taken two successive years of growth in semiconductor sales to take the excesses out of the supply. During this time, there has been increased usage of epitaxy in CMOS for high-performance devices. The utilization of silicon suppliers' epitaxial capacity appears to be near 100 percent.

We have not seen a movement of semiconductor manufacturers into commodity use of epitaxy for CMOS (i.e., for DRAMs). We believe that manufacturers will employ either epitaxy or high-voltage implantation or both to solve the problems associated with latch-up on the 4Mb era of products. Silicon suppliers have been slowly adding capacity for this inevitability.

However, neither semiconductor manufacturers nor silicon suppliers have invested in the production use of the new epitaxial reactors that have been recently developed for use in CMOS applications; namely, Applied's Model 7010 and Lam/Gemini's Tetron I. These systems have yet to prove that they can deliver the cost and quality improvements necessary for commodity production of CMOS integrated circuits. Applied's Model 7800 series remains the choice for high-quality thin films and Lam's Gemini II and recently, Gemini III, are purchased for most thick-film applications.

ASM Epitaxy

ASM Epitaxy introduced its Epsilon I in its booth this year, although it did not show the actual system. This is the much-awaited-for, single-wafer epitaxial system that had been under development in an R&D partnership called Epsilon (now ASM Epitaxy).

The system uses tungsten-halogen lamps configured at 90 degrees to each other above and below the wafer and rotates the wafer platen. It eliminates the cleaning and qualification cycle that must be performed on the 7010 and Tetron I by doing an HCl etch after every wafer. The price of the system ranges from $600,000 to $900,000 depending on options and spares. ASM has shipped three systems to date.

The specification on this system reflects the control and uniformity of the single-wafer approach. The company presented its specifications at the ASTM 5th International Silicon Symposium on February 4, 1988. We have summarized these and other specifications in Table 3.

This paper merely presents an existence proof of the potential film quality of the single-wafer approach. The measurement methods for the three sets of column data in Table 3 are not necessarily consistent, but are shown here for a relative comparison. While the process specification looks very good with respect to the batch approach, it is not a trivial matter to translate 40 years of production batch processes to single-wafer systems.

Table 3

Comparison of Epitaxial Systems Specifications

Specification	Epsilon I	Tetron I	7010
Thickness Uniformity	0.4 to 1.5%	3.0 to 5.0%	3.0 to 5.0%
Resistivity Uniformity	1.5 to 4.0%	Approx. 8.0%	Approx. 10.0%
Typical Intrinsics	500 ohm·cm	500 ohm·cm	500 ohm·cm

Source: Dataquest
July 1988

The throughput of the Epsilon I will pose a problem that will counterbalance the perceived process benefits. The gross throughput for a 10-micron epitaxial film is 6 wafers per hour (150mm wafers) compared with 21 wafers per hour on Applied's 7010 and 40 wafers per hour on Lam's Tetron I. After cleaning, reliability, preventative maintenance, and operational costs are considered, the cost per wafer on the Epsilon I should be approximately 1.5 to 2.5 times the cost of the batch approach. For a single-chamber system, we expect this approach to be relegated to a "high-performance" niche. However, this technique seems to have a natural potential evolution into a more productive, multichamber configuration. Who will do it? Dataquest wonders.

MOLECULAR BEAM EPITAXY/METALORGANIC CVD

The primary interest during the last year in the area of molecular beam epitaxy (MBE) and metalorganic CVD (MOCVD) has been the development of multiwafer systems to achieve higher throughput in the epitaxial growth of compound semiconductor materials. Equipment has also emerged for the deposition of the new high-temperature superconducting materials.

Three companies introduced new systems or presented major enhancements to existing equipment at the show this year: Emcore, ISA Riber, and Spire. While VG Instruments, a major supplier of MBE equipment, had no introductions or enhancements to announce at the show, the company is active in supplying MBE equipment for high-temperature superconductor applications; three systems have been shipped to Japan in the last year.

Emcore

Emcore introduced its VS/1000 MBE Source Panel. The VS/1000 is used in conjunction with conventional MBE systems to provide vapor source capability for metalorganic MBE (MOMBE), chemical beam epitaxy, and gas source MBE equipment. Typical MBE systems rely upon elemental solid sources for III-V epitaxial processing. With the VS/1000, vapor sources such as arsine, phosphine, and gas-phase organometallics can be introduced in a controlled fashion, with residual source material processed through a toxic gas scrubbing module. Advantages of vapor source materials

over solid sources include the elimination of equipment downtime and contamination associated with replenishing solid sources, as well as the elimination of certain types of defects associated with solid source contaminants. The VS/1000 is compatible with existing MBE systems from major manufacturers, such as Perkin-Elmer and Varian. The price of the VS/1000 can range from $175,000 to $350,000, depending upon configuration. Several systems have been shipped.

ISA Riber

ISA Riber announced its new system, the Riber MBE 48, an MBE system dedicated to III-V device production. The major feature of the system is that it is a multiwafer system, handling either four 3-inch or seven 2-inch wafers at a time. The price of the system is approximately $1.5 million to $1.8 million depending upon options. The first system will be delivered in early 1989 to Picogiga, a French manufacturer of III-V epitaxial wafers. The Riber MBE 48 was part of a joint development program between the two French companies and was designed to Picogiga's specifications.

ISA Riber also displayed information regarding its Supra 32 system. The Supra 32 (formerly known as the EVA 32) is designed for the growth and characterization of thin-film superconducting materials. (Supra is short for supraconducteur, the French word for superconductor.) Approximately half a dozen systems have already been shipped, and an additional half dozen are currently being converted from normal evaporator system design to one that is compatible with the rare earth metal oxides currently under investigation. The price of the Supra 32 is approximately $1.0 million. Because this system is primarily for the research environment, manufacturers may wish to add optional analytical surface analysis tools to the system in order to fully characterize the superconducting materials under investigation. These surface analysis tools, such as Auger and SIMS systems, can add as much as an additional $1.0 million to the price of the Supra 32.

Spire

Spire displayed information regarding its new SPI-MO CVD 500XT Advanced MOCVD Reactor. This system, designed for both reduced and low-pressure operation, is the latest from Spire in advanced MOCVD systems for the epitaxial growth of III-V materials. The 500XT can load and process single wafers, up to five 2-inch, or up to three 3-inch wafers at a time. The price of the 500XT is approximately $350,000, and the first system has been shipped to the University of Washington for development of high-efficiency GaAs solar cells.

RAPID THERMAL PROCESSING (RTP)

RTP vendors introduced several new models designed for specific environments. AG Associates introduced a production model in a through-the-wall configuration, as did Peak Systems and Varian. Peak and Varian also introduced models designed specifically for nonproduction environments. Eaton addressed itself to the needs of a specific process by introducing a titanium silicide retrofit kit for its ROA 4000.

At the same time, RTP vendors moved to address industry-wide trends such as larger wafer sizes and finer-line geometries. AG Associates introduced a 200mm system, and all vendors continued to improve those features that contribute to lower PWPs.

AG Associates

AG Associates introduced the Heatpulse 4100. The 4100 is a production model that can operate in either a through-the-wall configuration or a standalone configuration. The average selling price of the 4100 is approximately $275,000

The new system has a redesigned wafer handler with a three-axis flexible robot from Genmark Robot and has no elevators or belts. The robot arm can work in two planes simultaneously and has its own internal vacuum system that sucks out any particulates that may be generated by the robot's moving parts.

The 4100 is capable of handling 200mm wafers by changing the process chamber. It also comes equipped with its own ULPA filter. The company says that the 4100 can perform slip-free processing up to 1,250 degrees for oxide and nitride growth.

During service from the chaise area, the 4100 can be isolated from the clean room by a plexiglass partition that comes down between the handler area and the clean room. AG claims that the 4100 will generate only 0.0016 particles (0.5 micron) per square centimeter per wafer pass.

The 4100 also comes with a separate Emissivity and Temperature Calibrator cart, which AG claims gives a more accurate temperature reading than temperature readings done with a pyrometer.

AG says that it has already shipped 15 units of the 4100, including some to Japan.

AG also showed its vacuum oven option for the 4100. The vacuum oven has a gold-coated process chamber and a cylindrical quartz tube to withstand vacuum pressures.

Eaton

Eaton added a titanium silicide retrofit kit for its ROA 400. This kit purges the chamber with either an inert gas or nitrogen so that oxidation of the wafer does not occur. This allows the 400 to grow titanium silicide films without using a vacuum system and, Eaton claims, at a higher throughput than a vacuum system.

Peak Systems, Inc.

Peak Systems introduced two new RTP series, the ALP 5000 and 8000 Series. The ALP 5000 Series is a scaled-down version of Peak's ALP 6000 RTP systems. The 5000 and the 5500 are specifically designed for small footprints and low-productivity requirements such as are found in pilot lines, R&D lines, ASIC, and gallium arsenide lines. The 5000 Series has only a single wafer handler. The ALP 5500 has a low-pressure chamber for vacuum processing.

The 8000 Series employs the same core technology as the 6000 Series, but has the added features of flush mounting, stainless steel panels, and rear serviceability, with a clean room footprint of less than one square foot. It also has a self-contained ULPA filter. Pressure transducers and variable speed drives are employed to create an environmental balance that eliminates the pressure differential between the processing system and the clean room. Additionally, the 8000 is equipped with dual wafer handlers.

The 8000 incorporates full SECS implementation in both hardware and software and can be operated from either a local cell controller or a factory-wide control system. The 8000 Series is compatible with Asyst-SMIF wafer isolation and robotic-handling systems.

Varian

Varian introduced the RTP 8000 RD, which is specifically designed for development and pilot production work. Its average selling price is approximately $150,000. The new system offers the advanced processing features of the fully automated model and is 100 percent process compatible with that machine. It can be upgraded for fully automated production when high throughput is needed. The company expects shipments to begin by midsummer.

ION IMPLANT

Most of the implant vendors at SEMICON/West either introduced or showed for the first time 200mm-capable systems. Two vendors (ASM and Eaton) showed serial implanters. All of the systems featured increased use of robotics, and many systems claimed to be fully automated. User friendly (fail-safe) controls were also featured by several vendors.

Applied Materials

Applied introduced the 9200, which is designed specifically to handle 200mm wafers. The 9200 is a fully automated system, and its average selling price is approximately $1.8 million to $2.2 million.

The 9200 can handle 100, 125, and 150mm wafers, in addition to 200mm wafers. Conversion can be made with a larger wheel and wafer-handling size kit.

Applied also added an enhancement, called the Autobeam system, of its Light Touch automation package. The Autobeam allows a process engineer to create recipes and then identify them by simple code numbers. The Autobeam is fully compatible with factory automation requirements such as links to host computers via an SECS-II interface and robotic handling of cassettes.

Applied states that it has booked and shipped two systems to date.

ASM Lithography

ASM Lithography showed its ASM 220 medium-current ion implanter, which was introduced at last year's SEMICON/West. The 220 is a serial processing implanter that was designed for wafers from 125mm to 200mm. The 220 uses a parallel beam to eliminate shadowing.

All processing takes place in high vacuum to eliminate particulates from pump and vent operations, and all moving parts are below the wafer plane. The 220 features a PWP of 0.05 particles per square centimeter.

The 220 is capable of any tilt angle and has a throughput of 86 wafers per hour for 200mm wafers. Throughput for wafers smaller than 200mm is greater than 200 wafers per hour. Each component's operational hours and maintenance hours are logged and monitored by software.

ASM reports that it shipped its first system in the first quarter of this year.

Eaton

Eaton introduced the NV 6200A medium-current implanter. The NV 6200A features a new control system with one-button operation and auto-tune beam adjustment. The NV 6200A is a 200mm serial processing implanter; its average selling price is approximately $750,000.

The new control system will bring up the system under process recipe control and can change recipes with host control. An interlock system prevents any inadvertent misprocessing that might occur when an operator pushes the wrong button.

Eaton claims that the NV 6200 A has a MTBF of 200 hours and a MTTR of 2 hours.

Although Eaton's soon-to-be-introduced high-current implanter, the NV 20 A, was not shown at SEMICON/West, the company reports that it already has four orders for the 20 A and plans to ship four units this year.

Genus

Genus showed it Model IX-1500 system. The average selling price of the 1500 is approximately $2 million. The 1500 has an energy range of 40 keV to 3 MeV. The end station has an ultraclean robotic wafer handler and process chamber that is designed for 76 200mm wafers. The robotic arm is intelligent and can locate and compensate for the wafer's center of gravity. Wafers are handled in vacuum and transferred from cassette to a clamp-free, water-cooled disk. The disk has a variable angle of incidence.

Genus claims that the 1500 has an MTBF of 200 to 300 hours and a PWP of 0.05 particles per square centimeter. It is fully automated with auto-setup, failure prediction, diagnostics, and SECS II compatibility. Genus says that, to date, it has shipped two systems.

NEC

NEC introduced the MV – T31. The T31 boosts current by 2x over the MV – T30 and has a new end station with a clampless, mechanically scanned, water–cooled spinning disk. The implant angle is variable.

NEC also showed the MV – T60. The T60 is an automated 2MV tandem–based production system that is capable of providing ion beam beyond 8 MeV. NEC has added a new end station that it claims has a higher throughput, has no breakage, and is much cleaner than its previous end station.

Varian

Varian introduced the Extrion 1000, a high–current ion implanter for submicron devices. Varian designed the new implanter to appeal to both volume and ASIC manufacturers. The system can handle VLSI requirements for thin–gate oxides; ASIC requirements for fast parameter changes; as well as a broad range of implants for BICMOS processing. Features include improved uptime, advanced automation, real–time process control, and intelligent wafer handling.

The Extrion 1000 has been in development since 1984 and has a selling price of approximately $2.5 million. Varian expects its first shipments in early 1989. It has reportedly already booked an offshore order.

The 1000 is a fully automated system that is compatible with robot–guided vehicles in a fully automatic fab. The system can be operated by SECS II computer interface or touch–screen control. The system also has a second color touch–screen monitor that allows fully automated diagnostics from behind the clean room wall.

The implanter control system is based on distributed 68000–based modules. Each module is self diagnostic and subservient to a master module that continually queries its function–specific subordinates to predict and detect problems or failures.

The 1000 is a batch processing system with three individual vacuum–load elevators that handle one cassette each, thus minimizing load time, enhancing particulate control, and maintaining high throughput. The 1000's pick–and–place arm is equipped with a tactile sense and contacts each wafer on the backside only. The pick–and–place arm also has the ability to center and orient the wafer during transport.

The 1000 is capable of handling 200mm wafers. No mechanical motion occurs above the wafers, and wafers are handled without sliding, thus preventing particle generation. Damaged wafers are detected by laser sensors, which prevent the damaged wafers from being loaded onto the disk. Varian claims that its new platen will remove heat from implanted wafers four times faster than previous platens.

The 1000 is automatically set up, self–tested, and self–corrected. All critical parameters are monitored and automatically adjusted during operation. Dose accuracy is monitored and scan rate is adjusted in real time; real–time wafer temperature and wafer charging are also monitored and controlled constantly.

The 1000 has an energy range of 2 to 200 keV and a standard beam current range from microamperes up to 27 mA.

PROCESS CONTROL

Process control systems represent a broad category of equipment that is used to measure, inspect, and monitor the status and trends of processes in semiconductor device fabrication. In this year's review of SEMICON/West, Dataquest reports on a diversity of new products and enhancements in the areas of critical dimension (CD) measurement, wafer inspection, defect review, particle detection, film thickness measurement, and mask metrology and inspection. Companies showing products in this area are discussed below.

Inspex

Inspex introduced the EX100/200 Microscope Revisiting Station, a classification station for its EX3000 patterned wafer inspection system. The EX3000, introduced at last year's SEMICON/West, provides both count and size distribution of particles on patterned wafers. With the EX100/200 station, an operator can perform classification tasks as a function separate from the operation of the EX3000. The EX100 is a manual system priced at $70,000, while the EX200 includes automatic wafer handling and is priced at $95,000. First shipments will begin in the July time frame to U.S. customers.

Insystems

Insystems introduced an advanced data management software package for its Model 8600 holographic patterned wafer defect inspection system. The software package, known as FAB MANAGER, provides the capability for data capture, manipulation, and storage of up to 4,000 recorded wafer inspections. Wafer inspection data can be analyzed for repeating defects, for defects by process layers, and for defect patterns across the entire wafer map. FAB MANAGER software can be networked to other systems via a SECS-II link. The new software package is available to both new and existing Model 8600 customers at no additional cost.

In addition to its new software release, Insystems recently announced that it has received a new round of funding of $3 million. The latest funding brings the total capitalization from private sources to more than $12 million.

IVS, Inc.

IVS introduced a new software package for its Accuvision family of critical dimension (CD) measurement systems. The new software performs analysis of bottom and top contact measurements and determines whether a contact is open or closed. Contact measurement capability is on the order of 0.8 micron with 30-nanometer repeatability and relies upon a proprietary autofocus mechanism that the company has developed.

IVS currently offers the ACV-1 and ACV-4 systems, which perform linewidth, overlay, and now, contact measurements. The ACV-1 is a manual system priced at approximately $100,000, while the ACV-4 includes automated wafer handling and is priced at approximately $300,000. Wafer throughput for linewidth measurement on the ACV-4 is on the order of 25 to 30 wafers per hour at five sites per wafer. Measurement capability is specified at 0.5 micron with 30-nanometer repeatability.

KLA Instruments

At this year's show, KLA Instruments introduced the KLA-2600 Defect Review Station. This station allows an operator to perform wafer defect classification as a function separate from the operation of KLA's automatic defect detection systems (the KLA-2020, -2028, and -2030 systems). This translates to enhanced throughput of the 2020/2028/2030 systems of approximately 33 percent, because now the time-consuming task of operator defect classification can be performed essentially off-line at the 2600 review station. The KLA-2600 consists of a microscope station, robotic wafer-handling system, and PC AT-compatible controller. The software of the 2600 interfaces with the KLAUT computer (KLA-2500), which downloads defect coordinates to the review station. After review and classification, the records are transferred back to the KLAUT for comparative analysis. The base price of the KLA-2600 is approximately $120,000, compared with the $1.0 million price tag of KLA's automatic defect detection systems. The company has received orders for the 2600, and shipments are expected to commence in the August time frame.

The KLA-5000 Coherence Probe Imaging System system had its West Coast debut at SEMICON/West this year. First introduced at SEMICON/Europa in March, the KLA-5000 is an optical-based system that performs automatic linewidth and overlay measurements. With the technique of coherence probe imaging, three-dimensional metrology information is obtained from independent measurements of the top, bottom, and height of line profiles. Measurement resolution is currently quoted at 0.7 micron, although the company anticipates that this will be extended to smaller geometries in the future. Wafer throughput is 40 to 45 wafers per hour at five measurement sites per wafer. The KLA-5000 is priced at $395,000 in Europe (includes 12-month warranty) and $350,000 in the United States (3-month warranty). Several orders have been received, and shipments are expected to commence in the August time frame. The system is being manufactured at KLA's facility in Israel.

In addition to its products in wafer metrology and inspection, KLA Instruments also introduced a new system for mask and reticle inspection, the KLA-239HR. The advanced photomask and reticle inspection tool is capable of both die-to-die and die-to-database inspection of linewidths down to 0.5 micron with defect sensitivity as low as 0.25 micron. The system is priced at approximately $1.2 million in the United States and deliveries are expected to begin in fourth quarter 1988. In addition to the KLA-239HR, KLA displayed the KLA-259 Automatic Resist Image Inspection System. This system uses special reusable photoresist-coated quartz wafers in the reticle qualification process, which eliminates the need for etching of metal-coated glass wafers. The KLA-259 is priced at $895,000, and deliveries are scheduled to begin at the end of the year.

Nanometrics

Nanometrics introduced six new products at SEMICON/West this year: three film thickness measurement systems, an optical-based CD measurement system, a SEM-based CD measurement tool, and the company's first optical defect inspection station.

In the area of film thickness measurement, Nanometrics introduced three new models in its family of NanoSpec/AFT Automated Film Thickness Systems: the Models 210 VT, 212 VT, and 215. The Model 215, priced at less than $100,000, is a fully automated system with autofocus, automated wafer handling, automatic positioning, automatic flat finding, and automatic measurement. It has film thickness measurement precision of a few angstroms for photoresist and thick oxide films in the range of 500 angstroms to 30,000 angstroms. The new VT option for the Model 210 and 212 NanoSpec/AFT systems is specifically targeted at thin-film measurement applications in the range of 20 to 450 angstroms. (The Model 210 system is a manual system, the 212 includes automated wafer-handling capability.) The 210 VT is priced at $57,000, and the 212 VT is approximately $80,000. Shipments of the 210 VT and 212 VT systems have commenced. As of SEMICON/West, no orders had been received for the Model 215 system.

The Model 55 Submicron Optical CD Measurement System is a fully automated system that provides 0.7-micron linewidth measurement capability with 10-nanometer repeatability. Linewidth measurement throughput is approximately 40 wafers per hour at five sites per wafer. The Model 55 is an automated version of the Model 50-2, which itself was recently upgraded with new optical components from the Model 50. The price of the Model 55 is $99,000. The company has received orders and expects to begin deliveries in August.

As a technology alternative to optical-based CD measurement in the submicron regime, Nanometrics introduced its Nano 150Z CD, a low-voltage SEM measurement system. The 150Z CD is an extension from the Model 100 which it replaces. One important feature of the system is that it utilizes an IBM PC-driven software user interface. The price of the 150Z CD is approximately $500,000. Nanometrics has just begun marketing this product. As of SEMICON/West, no orders had been received.

The NanoStation I represents Nanometrics' entry into the wafer defect inspection equipment market. The NanoStation I is a dual-cassette system designed for inspection of 100mm, 125mm, and 150mm wafers. The system has many automated features, including robotic wafer handling; however, it does require an operator to perform the defect detection and classification tasks. An optional feature is a computer ImageFile that allows 2,500 images to be identified and stored with rapid retrieval for later defect review. The NanoStation I is priced at less than $65,000 in the United States. As of SEMICON/West, no orders had been received.

Nikon

Nikon exhibited four new products and enhancements in the area of mask and wafer metrology and inspection: the LAMPAS-HD (linewidth and overlay measurement on wafers), the XY-3i (mask metrology measurement system), the RMX-3/3P (mask and reticle inspection systems), and the OST-Mapping System (software enhancement to the Optistation wafer inspection system).

The LAMPAS-HD critical dimension measurement system had its West Coast debut at SEMICON/West this year. (The system was announced at SEMICON/East last September and first shown at SEMICON/Japan last December.) The LAMPAS-HD utilizes a 325nm helium-cadmium laser source and is capable of measuring linewidths down to 0.7 micron on silicon wafers with 1.0-micron-thick photoresist lines. Wafer throughput for the LAMPAS-HD is 30 to 35 wafers per hour at five measurements per wafer. The system is priced at $495,000 in the United States. Demonstrations of the LAMPAS-HD began in early May at Nikon Precision's facility in San Bruno, California. A number of systems have already been shipped to customers in Japan.

Nikon also exhibited its next-generation laser-based coordinate measurement system for mask metrology, the XY-3i. The XY-3i is an upgrade from Nikon's XY-2i that has dominated the mask metrology market for a number of years. One of the major system improvements of the 3i is a measurement repeatability specification of 0.05 micron (3 sigma); this is compared with the 2i's specification of 0.15 micron (3 sigma). System software has also been enhanced and includes new user-friendly features that were suggested by users of the 2i system. The XY-3i is priced at approximately $1.0 million. Demonstrations of the 3i will begin in July at Nikon Precision's facility in San Bruno.

Nikon announced its new RXM-3/3P mask and reticle inspection systems. The RXM-3 is a die-to-database mask and reticle inspection system that compares design data with the actual mask or reticle in order to detect the presence of defects that may have arisen during the maskmaking process. (The RXM-3P has the additional capability of inspecting through pellicles.) The system is priced at approximately $1.2 million. Several systems have already been delivered to customers in Japan. Demonstrations of the RXM systems will begin later this summer at Nikon Precision's facility in San Bruno.

Nikon's Instrument Group introduced the OST-Mapping System, a software enhancement to the Optistation wafer inspection station. The OST-Mapping System simplifies the task of final inspection after probe by providing "good die" coordinate information from a host computer to the motorized stage of an Optistation inspection system. An operator can then perform a final defect inspection cycle on die that have successfully passed through probe, and mark (with inker attachment) any die that still have defects present that would kill device performance. The price of this system is approximately $10,000.

Olympus

Olympus introduced the Cue 2000 Wafer Inspection Station. The system utilizes image recognition software and a user-defined defect library to perform automatic defect detection of up to 15 different types of defects including breaks, bridges, mouse nips, necking, contamination, scratches, and particulates. The Cue 2000 can also be used to produce a library of defect images for future reference. The system can handle wafers of 100mm, 125mm, 150mm, and 200mm diameter. Automated functions include positioning and scanning, autofocus, wafer-handling, and inspection routines, with additional capability for remembering and recalling nonstandard defects. The Cue 2000 was fully developed in the United States, and the price range is expected to be $135,000 to $150,000. Olympus expects to start beta site evaluation for the Cue 2000 in the August time frame.

Opal Inc.

Opal Inc. introduced its new automatic e-beam wafer metrology and inspection system at SEMICON/West this year. The Opal 702, a low-voltage SEM system, is initially being targeted at submicron linewidth and overlay measurement. The system has measurement capability down to 0.1 micron with 10-nanometer repeatability. The Opal 702 performs spatial metrology (linewidth as well as line profile) measurements, as it has the ability to simultaneously measure the top, middle, and bottom of submicron features.

Throughput of the Opal 702 for CD measurement is 30 wafers per hour at five sites per wafer. This is substantially higher than the typical 8 to 15 wafer-per-hour throughput of most e-beam-based metrology systems. Opal achieves this enhanced throughput with multichamber processing and advanced software that provides pattern recognition and fast measurement capability. The base price of the Opal 702 is approximately $650,000. The system is currently in beta site.

Opal Inc., headquartered in San Jose, California, was founded in December 1986 by Optrotech, a major manufacturer of printed circuit board inspection systems. Investors from the venture capital community include TA Associates as well as Adler and Company. Opal is currently undergoing its second round of venture funding.

Optical Specialties, Inc.

Optical Specialties, Inc. (OSI) introduced next-generation systems for several of its CD and wafer inspection products at SEMICON/West. In addition to these new systems, the OSI Polycheck and OSI Microcheck metrology systems were also displayed in the company's booth. These products from Reichert-McBain, along with the Polycheck VLSI, have recently been incorporated into the OSI product line as a result of last December's agreement between OSI and Cambridge Instruments. In that decision, Cambridge Instruments agreed to acquire a 40 percent equity interest in OSI in exchange for the transfer of its Reichert-McBain division to OSI.

Among OSI's new products at the show was the MV-400, a dedicated wafer inspection station that is the next generation of OSI's MV-360 system. The major enhancement in the MV-400 has been a new design of the automated wafer-handling system. The price of the MV-400 is comparable with that of the MV-360 at $65,000.

Two other new products, the MV-500 and the MV-PLUS LaserLine, both incorporate a new solid-state infrared laser autofocus system for improving measurement precision. The MV-500 is the next-generation system of OSI's VLS-I linewidth measurement tool. The price of the MV-500 is approximately $85,000. The MV-PLUS LaserLine, priced at $185,000, incorporates the LaserLine technology into the company's MV-PLUS system, a joint CD/inspection station. The LaserLine autofocus system has been part of the technology development for OSI's MV-5000 system, a fully automatic CD and defect inspection system. OSI plans to start beta site evaluation of the MV-5000 at its facility this summer.

Prometrix

Prometrix introduced the FT-500, a new film thickness measurement system. The FT-500 utilizes spectrophotometric techniques to obtain film thickness measurements on production wafers. The cassette-to-cassette system has automatic wafer handling and also includes Prometrix's sophisticated data analysis package, StatTrax. The FT-500 is priced at $160,000, and Prometrix expects deliveries to begin at the end of third quarter 1988. Dataquest believes that the development of the FT-500 marks a significant strategic decision for Prometrix. Prior to the FT-500, all Prometrix products have been focused on the test wafer environment. Dataquest expects that as part of a strategy for growth, Prometrix will expand its product line to encompass more systems for the product wafer market.

SiSCAN Systems

SiSCAN announced several enhancements to its SiSCAN-IIA confocal scanning laser microscope system at the show this year. Enhancements include pattern recognition, SECS-II communications capability, and a new parallel processor for its autoloader system. In addition, SiSCAN now offers a 325nm helium-cadmium laser as the standard source on the IIA system. The SiSCAN-IIA is priced at approximately $400,000.

SiSCAN Systems is also offering the Monolith workstation through a marketing agreement with Shipley/Obelisk. The Monolith workstation provides CD and overlay mapping capability and will plot out stepper correction values for focus and exposure settings. The system can communicate directly to a stepper through a SECS-II communications link. The Monolith workstation was originally developed at GCA, where it was used in conjunction with the GCA stepper to optimize focus and exposure settings. GCA sold the technology to Obelisk, which was later acquired by Shipley. No price has been set yet for Monolith workstation.

Technical Instruments

Technical Instruments introduced its new K-2 Real-Time Confocal Tandem Scanning Microscope with automatic linewidth measurement capability. This is Technical Instruments' first entry into the confocal laser microscope market; however, the company currently offers other optical-based linewidth measurement systems. The K-2 system is priced at approximately $110,000 and has optional wafer-handling capability. Technical Instruments plans to start shipping this product in the September time frame.

Tencor

Tencor introduced the Surfscan 7000 Patterned Wafer Contamination Analyzer, a fully automated inspection system for detecting particles as small as 0.8 micron on patterned process wafers. This is the first product in the Surfscan family that has been developed specifically for patterned wafer (as compared with bare wafer) inspection. The Surfscan 7000, like the other Surfscan products, utilizes low-angle laser light scattering off the wafer surface to detect the presence and location of particles on the

surface. One of the major features of the 7000 is its periodic feature elimination mode, which increases the sensitivity of the system by eliminating the signal from repetitive features present in the wafer pattern. Specifications for the system cite a 200mm wafer scan in less than 5 minutes and a 100mm wafer scan in approximately 2.5 minutes. The Surfscan 7000 is priced at $325,000. The first system was expected to be shipped in June to the European facility of a U.S. semiconductor manufacturer.

Vickers Instruments

Vickers Instruments introduced several enhancements to its Quaestor CD–07A critical dimension measurement system. These include the introduction of a CCD camera in place of the vidicon camera used previously, a new software package to improve throughput on overlay registration and contact hole measurement, and a hard disk with 50–MByte capability. With the new CCD camera and software, throughput for overlay measurements is now on the order of 20 wafers per hour at five sites per wafer.

In addition to enhancements on the Quaestor CD–07A, Vickers also exhibited the Nanolab SR, a SEM–based CD measurement system for the production environment. Its sister tool, the DL3206 SEM–based CD measurement system, was exhibited at last year's show. The difference in the two systems is that the DL3206 SEM has been designed for use in process development and troubleshooting, in contrast to the Nanolab SR Series which has been designed for in–line processing in the production environment.

Waterloo Scientific

Waterloo Scientific introduced the CD–II Critical Dimension Measurement System. The CD–II is an automated CD measurement system based on confocal scanning laser microscopy. The system has a smaller footprint than the engineering prototype that was shown at last's year SEMICON/West. Other system features include a CCD camera detector, robotic wafer handling, and menu–driven software for system operation and image processing. The CD–II is a dual–laser system; two helium–neon lasers at 543nm and 632nm wavelengths are standard system sources. However, the company can provide laser sources from 325nm to 1.15–micron wavelength to cover a range of applications. The price of the system has not yet been fixed but is expected to be approximately $300,000. No systems have been shipped.

Wild Leitz

Wild Leitz introduced its SMIF version of the LTS–S Wafer Transport System for wafer inspection. This system consists of a SMIF interface combined with a transparent anticontamination enclosure that guarantees protection against contamination during the wafer inspection process. (SMIF boxes are used to prevent contamination and maintain wafer integrity during transportation between processing stations in the fab.) Meissner and Wurst, a West German clean room manufacturer, manufactured the integrated airflow and filter system used to maintain a Class 1 environment within the enclosure. The price of the system is approximately $220,000 to $250,000. Deliveries to European customers began in late 1987; several systems have been shipped.

Zeiss

Zeiss introduced the LSM-20, a confocal laser scan microscope system. This tool has been initially targeted at the research and development environment. It can be used in a variety of surface and materials analyses including wafer surface inspection, testing procedures such as optical beam-induced current, as well as materials testing by photoluminescence. The LSM-20 is a dual-laser system and includes a 632nm helium-neon laser and 488nm argon-ion laser as standard sources. Zeiss also offers a version with infrared laser sources (632nm and 1150nm helium-neon lasers) for materials characterization of III-V wafers. The system is priced at approximately $150,000.

AUTOMATION

Dataquest divides the semiconductor automation market into four sections: factory automation software, cell/station controllers, fixed-wafer transport, and robotics. There was a lot of excitement in all four of these areas at SEMICON/West. Digital Equipment shared its booth with seven other vendors and displayed an integrated fab manufacturing operation.

In addition to the Digital display, factory automation systems and software generally offered enhancements of existing systems. Software vendors, for example, also offered enhancements such as icon-based interfaces and more statistical process control (SPC).

Robotic systems and factory transport systems generally featured refinements of control systems, such as touch control screens, more flexibility, and lower numbers of particulates per wafer-handling operation.

Factory Automation Software

Cameo Systems, Incorporated

Cameo Systems introduced CAMSTAT, a statistical process control (SPC) software applications package, designed to analyze engineering and/or test data. CAMSTAT can be used as a standalone applications package or integrated into existing data collection systems. It is available on several different computer systems.

Consilium

Although Consilium did not have a booth of its own at SEMICON/West this year, it did share a booth with Digital Equipment and other complementary vendors (see Digital in this section). At this booth, Consilium demonstrated how its COMETS Smart Shop Floor Control software package works in an integrated distributed environment. One of the newer modules of the COMETS package (introduced at SEMICON/West 1987) is its rule-based, short-interval scheduling system with priority dispatch.

Digital Equipment

Digital demonstrated the semiconductor industry's first totally integrated computerized manufacturing operation using SECS protocol, DECnet local area network hardware and software, and standard products from automation and equipment industry suppliers.

The production system shown portrayed the distributed control of a diffusion cell. The entire process was integrated through network links. Companies providing components of the integrated system were: BBN, which provided statistical analysis software; Consilium, which provided factory systems software; ProgramMation, which provided a monorail track system; Semitool, which provided a prediffusion clean station; Silicon Valley Group, which provided a vertical thermal reactor; Thesis, Inc., which provided cell controller software; and Westinghouse/Unimation, which provided two robots.

The manufacturing cell is designed so that as the needs of a cell change, additional resources can be integrated into the networked system. No single point of failure in the cell can cause production to stop. The networked systems are configured so that almost all operations can continue in case of system failure, thus minimizing lost production revenue.

The system shown at SEMICON/West took only three months from development of the initial concept to the completion of the finished operation at SEMICON/West. In the demonstration, the host computer system scheduled wafer lots, downloaded recipes to a local production computer or cell controller, and collected information on process, production, and the environment. Data from the operations were processed by the statistical analysis package, which generated reports on the processes and associated items.

Promis Systems Corporation

Promis has introduced a new status board for its PROMIS software package. This new status board, which is icon based, will track all lots and reflect changes in lot status and equipment status, such as down equipment.

It also has a graphical user interface, the Factory Top, which is a software link between Apple's Macintosh and Digital Equipment's VAX system. Factory Top translates data base information into pictorial form.

Cell Stations/Controllers

CTX International

CTX International, a Motorola New Enterprises company, announced a cell controller, the CTX System 8000. The 8000 is based on a real-time distributed computer system and adds a level of control between factory floor equipment and host systems. Its functions include collecting and analyzing real-time data from equipment, forwarding appropriate aspects for analysis to both operators and the host system, and directing intracell activities with information from the host system to perform supervisory control of shop floor operations.

The 8000 uses a building block approach that begins with control of process data. The next level is control of equipment availability, utilization, and throughput, and process management through SPC procedures. The final level consists of supervisory control, where process decisions, based on input from equipment and process control modules, are automated.

Thesis Group, Inc.

Thesis Group demonstrated its AutoCell Reconfigurable Cell Control Software at Digital Equipment's demonstration booth. The AutoCell can be used in photolithography, diffusion, etch, or implant. AutoCell runs on Digital's VAX family computers and interfaces to higher levels of facility-wide software systems. Autocell performs material entry/exit, status monitoring, intracell material scheduling and tracking, real-time data collection and SPC analysis, feed forward and feed back, complete WIP control, exception handling, and environmental alarm actions.

Westinghouse Electric Corporation

Westinghouse showed its recently introduced robotic controller, UNIVAL. UNIVAL features open architecture modular hardware with advanced VAL II programming language. The controller is designed to be modular, so that it can efficiently be applied in either single-robot applications or more sophisticated cell control configurations. It can simultaneously operate as many as 13 process control programs.

Fixed Wafer Transport

ProgramMation, Incorporated

ProgramMation has redesigned its ProgrammaTrak System material delivery system and was part of the Digital Equipment demonstration. The system transported cassettes of wafers between two robotic workcells while under the direction of Digital's computers. Actual installation of the equipment at the show took less than one day.

The ProgrammaTrak is capable of transporting payloads of up to 15 pounds while operating in a Class 10 environment. The ProgrammaTrak system includes vehicles, the monorail track, and a routing and tracking computer. The system also can be configured for either inter- or intrabay transport, new construction, or for retrofits. The track may be mounted above the floor, from the walls, or from a HEPA ceiling.

Each vehicle is autonomous, microcomputer controlled, and independently powered. In addition, each is uniquely identified and is capable of communicating with each of the track network modules. This allows complete control and tracking of materials being transported on the vehicles. Each vehicle includes obstacle sensing, station sensing, communications capabilities, and user-programmable I/O.

Veeco

Veeco showed its S.A.L.T. (Semiautomatic Lot Tracking) system, which provides the networking of bar code readers with Veeco's complement of Work-in-Process Storage Stations (WIPSS) and controlling software. The S.A.L.T. system allows manufacturers to begin to automatically track work in process in an environment where people still provide the physical lot movement and still act as the interface to the process equipment.

Westinghouse Electric Corporation

Westinghouse introduced its Unimate Clean Room Track, which it claims meets Class 1 performance criteria. This track system was developed in conjunction with Accu-Fabs Systems, Inc., of Corvallis, Oregon. The track system is applicable to robotic wet process stations and uses the Unimate PUMA 500CR and 700CR robots. The robots can move wafer cassettes or disks from between equipment or from WIP station to WIP station.

Modular in construction, the track system allows standard sections to be linked to a total track length of 36 feet. The track has its own controller, which communicates to the robot's control system over an RS-232-C port.

Robotics

Asyst Technologies

Although Asyst Technologies did not show any new systems at SEMICON/West, it did make a significant announcement prior to the show. Asyst has confirmed the receipt of a multimillion dollar order for more than 100 SMIF-Arms and other related equipment, which will be installed at several major Siemens European locations.

Asyst showed its complete SMIF isolation system, as well as its SMART Traveler System. The Asyst-SMIF System consists of an SMIF Pod, an equipment isolation enclosure, and a SMIF Arm. The Asyst-SMIF System achieves an ultraclean environment for the storage, transport, and processing of semiconductor products by applying the principles of clean space isolation and mechanized cassette loading. The SMART-Traveler System provides automation for material control transactions through use of an electronic work traveler to replace lot cards and paperwork.

Genmark Automation

Genmark introduced the Gencobot I and II wafer-handling robots. Both versions are designed to handle hard disks and silicon or GaAs wafers. The Gencobot I is interchangeable with any other Gencobot without the need for reprogramming. It has been tested to meet Class 1 standards. It can be ordered with as much as 25 inches of vertical Z axis. It is also has a fully programmable controller and can be run as either a standalone model or integrated with a host computer.

The Gencobot II is also interchangeable with other Gencobots and is a table-mounted version of the Gencobot I.

Precision Robots, Incorporated

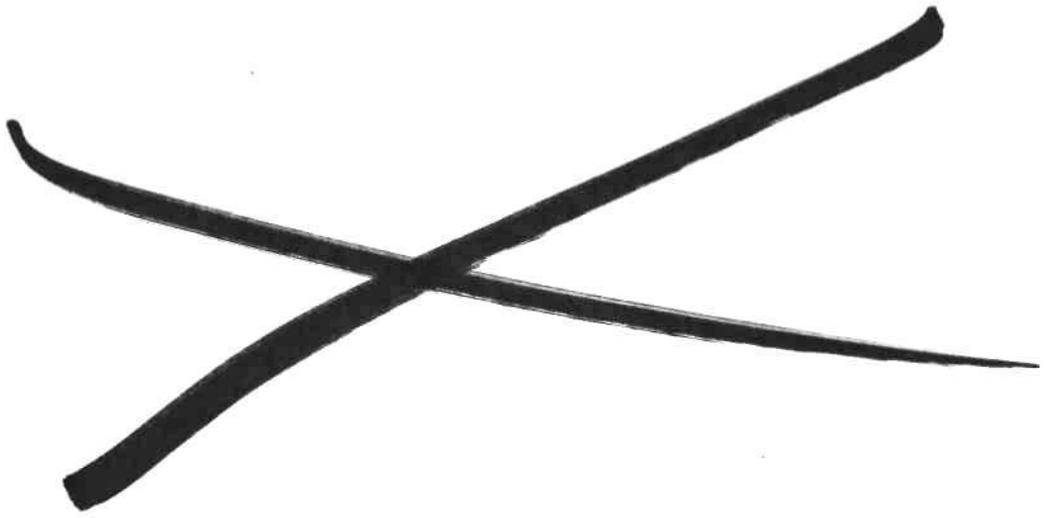
Precision Robots, Incorporated, introduced the PRI-4000 Series Spray Tool Automations System. The 4000 completely automates all wafer transfer and cassette load/unload operations for FSI and Semitool spray processing equipment. The 4000 is designed for Class 10 or better clean rooms. The 4000 consists of a PRI-2000 robot with sealed body parts and arm joints to prevent the escape of particulates. The 4000 also has a wafer-transfer station, input/output conveyors, and a supervisory computer.

RobopTek, Incorporated

RobopTek introduced a pick-and-place SMIF-compatible robot. This robot is being used at National Semiconductor's OASIS project, and its average selling price is approximately $40,000.

RobopTek also introduced a wafer combiner that can reorder wafers on a cassette. It can also handle, queue, and track hot individual wafers and dummy wafers.

George Burns
Joe Grenier
Kaz Hayashi
Robert McGeary
Mark Reagan
Peggy Marie Wood



Dataquest
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The Dun & Bradstreet Corporation

Research *Newsletter*

SEMS Code: 1987–1988 Newsletters: August
1988–24
0000939

THE OASIS PROJECT: A MORE RELAXED AND LESS COSTLY FAB FUTURE?

An experiment to manufacture VLSI devices outside of a clean room, yet with particles per wafer pass (PWP) and defect densities comparable to those in a clean room, is taking place in Silicon Valley. Dataquest analysts visited this room recently. Dressed merely in street clothes and sipping coffee from styrofoam cups, we stood next to a stepper. Nearby stood two healthy potted plants in containers of dirt (i.e., the real world).

THE OASIS PROJECT

This is all part of National Semiconductor's OASIS Project. The goal of the OASIS Project is to evaluate the effectiveness of manufacturing that uses Standard Mechanical Interface (SMIF)/isolation technology. Rather than using standard clean rooms, the OASIS Project uses a standard office in which processing equipment is isolated from the ambient air by basic SMIF/isolation components. These components consist of a sealed box for wafer cassettes, a mechanism for loading/unloading and placement/removal of the cassettes into or out of the process equipment, a canopy/enclosure to cover part or all of the process equipment, and an air supply/exhaust interface to the processing tool.

Standard clean room practice, to put it rather simply, is to use large, isolated rooms that protect the manufacturing equipment and the wafers from contact with everyday "dirty" environments. Operators and process engineers are kept from contaminating these clean rooms by a combination of automation strategies and gowning procedures—wearing either "bunny suits" or state-of-the-art "spacesuits." If the OASIS experiment is successful, only the part of the equipment that handles or processes the wafers will be kept isolated from an everyday environment. People will be free to come and go as they please, dressed in their normal work attire.

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398 / (408) 437-8000 / Telex 171973 / Fax (408) 437-0292

EXPERIMENT GOALS

The goal of this particular experiment is to prove the feasibility of such an approach by achieving PWPs and defect densities at least as good as those achieved in standard clean rooms. The final results probably will not be reported until October, but preliminary results look encouraging.

With clean room construction costs reportedly surpassing $1,000 per square foot and going higher, the implications of a successful OASIS experiment could be profound. VLSI IC manufacturing could take place in rooms without HEPA ceilings. Laminar flow would still take place, but it would be within the protective canopy that covers the equipment.

Perhaps even more revolutionary than manufacturing without special air-handling systems would be the absence of special clothing for people in the manufacturing environment—no more cumbersome and expensive bunny suits.

CONSTRUCTION AND OPERATING COST REDUCTIONS

Removal of Class 1 and Class 10 air-handling systems would mean savings in both construction costs and monthly operational expenses. The construction costs for the filters, fans, return air systems, and associated structural support would no longer be necessary. Additionally, the removal of these air-handling systems could reduce the need for expensive vibration-dampening foundations, since the air-handling systems themselves are a major source of vibration.

Up to 15 to 20 percent of clean room space is devoted to gowning areas and air showers for human beings. A successful OASIS strategy, however, would not need either gowning areas or air showers, thereby saving the cost of floor space currently required by them.

The proponents of OASIS believe that the savings in operating costs will be at least as great as the savings in construction costs. An obvious operating expense that could be saved is garment costs. Currently, this can amount to $1,000 or more per clean room garment, not counting cleaning costs.

Perhaps not so obvious, but possibly substantial, are productivity savings. Operators, for example, spend up to 30 minutes per shift in gowning areas. Not only is time lost in gowning up, but many workers report that it is harder and more time consuming to work and talk in bunny suits.

Some industry observers believe that because the suits are uncomfortable, they discourage process engineers from going into the clean rooms. Of course automatic data collection might make it unnecessary for them to do so in the future, but for the manufacturing process to continue to achieve recognition, we believe that the manufacturing floor ought to be a comfortable place—a place where those directly responsible for the process like to go. The OASIS concept will make this possible.

Another significant operational saving would be the cost of moving and cleaning large volumes of clean room air. Professor Takahiro Ohmi of Tohoku University in Japan estimates that a conventional clean room's air-handling system can cost up to ¥810 ($6.25) per square meter of clean room space per day. This implies, assuming that electricity is two to three times more expensive in Japan than in the United States, that a conventional air-handling system for a 20,000-square-foot clean room in the United States costs approximately $2 million per year to operate.

REVOLUTIONARY IMPLICATIONS

Unfortunately, most of the signs that we see (decreasing line geometries, increasing cleanliness requirements, and device complexity) point in one direction for fab costs—up.

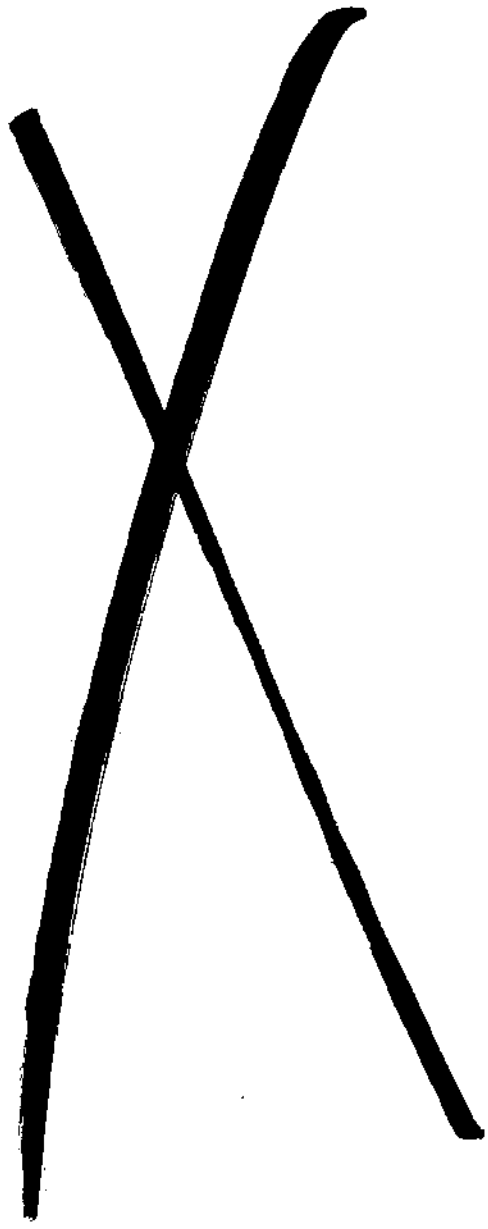
The cost of building a new fab today can easily exceed $100 million. This is a tremendous sum of money, even for large manufacturers. For small and start-up companies, this amount of money can be prohibitive. Rather than do their own manufacturing, these companies will enter into arrangements with either foundries or strategic partners for the manufacture of their devices.

OASIS, however, is a significant sign to the contrary. If it is successful (and that is a big if), then it is possible that fab costs could begin to come down. Millions of dollars in each fab could be spent on equipment rather than on the room that houses the equipment. The capital cost of a clean room is currently about one-third the capital cost of equipment.)

One caveat: blacksmiths were not among the first to use the horseless carriage. If the OASIS experiment is successful, it may be difficult to motivate the clean room construction industry and facilities managers to adopt it. The direction of current technology (better air filters and air handling, more vibration dampening, electropolished gas and chemical lines, automated, and people-less) is well defined. It is safe, it is profitable to the participants, and it has now become "the way we've always done it." Many honorable careers have been made by building ever more clean and expensive facilities. Facilities managers, confronted with demands to be more and more vigilant against smaller and smaller particles, look to the clean room construction industry for solutions. These solutions are always forthcoming and always more expensive.

The final ingredient for the success of the OASIS Project, in our opinion, is a CEO with the courage and daring to be out in front when there's no one else there.

George Burns
Joe Grenier



Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987–1988 Newsletters: October
1988–25
0001631

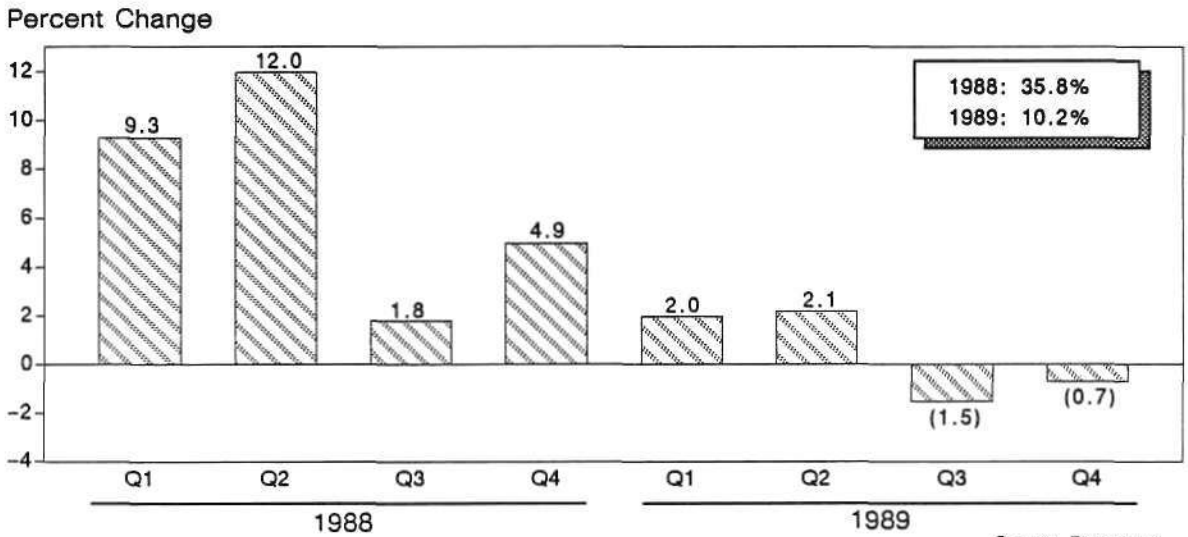
WORLDWIDE SEMICONDUCTOR INDUSTRY UPDATE: WHEN WILL THE DOWNTURN HIT?

SUMMARY

The year 1988 has been a booming one for the worldwide semiconductor industry, with estimated total growth of 35.8 percent, continuing the good times of 1987 (a year of 22.8 percent growth). During the third quarter of 1988, bookings began to soften, and many semiconductor manufacturers experienced poorer than usual August bookings. However, the existing backlog, combined with shortages in key product areas—most notably, DRAMs and SRAMs—should keep shipments strong through the end of the year. Dataquest forecasts much slower growth in the first two quarters of 1989. This slow growth will be followed by negative growth in the second half of 1989, as supply catches up with and then exceeds demand and both unit shipments and ASPs fall. The short-term forecast is summarized in Figure 1.

Figure 1

Worldwide Semiconductor Shipment Forecast



Source: Dataquest
October 1988

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398 / (408) 437-8000 / Telex 171973 / Fax (408) 437-0292

WORLDWIDE FORECAST

A summary of the worldwide forecast by region is shown in Tables 1 and 2.

Table 1

Estimated Worldwide Semiconductor Market
(Billions of U.S. Dollars)

	1988	1989	1990	1991	1992	1993	CAGR 1988-1993
North America	15.7	17.2	17.5	20.4	24.8	26.7	11.2%
Japan	19.5	21.3	21.5	25.2	30.5	33.3	11.3%
Europe	8.2	8.8	8.8	9.8	11.3	12.5	8.8%
Rest of World	6.1	7.3	7.9	9.9	12.7	14.3	18.4%
Total World	49.5	54.6	55.7	65.3	79.3	86.8	11.9%

Source: Dataquest
October 1988

Table 2

Estimated Worldwide Semiconductor Market
(Percent Change, U.S. Dollars)

	1988	1989	1990	1991	1992	1993
North America	32%	10%	1%	17%	22%	8%
Japan	36%	9%	1%	17%	21%	9%
Europe	29%	7%	0	12%	15%	11%
Rest of World	57%	19%	9%	25%	28%	13%
Total World	36%	10%	2%	17%	22%	10%

Source: Dataquest
October 1988

North America

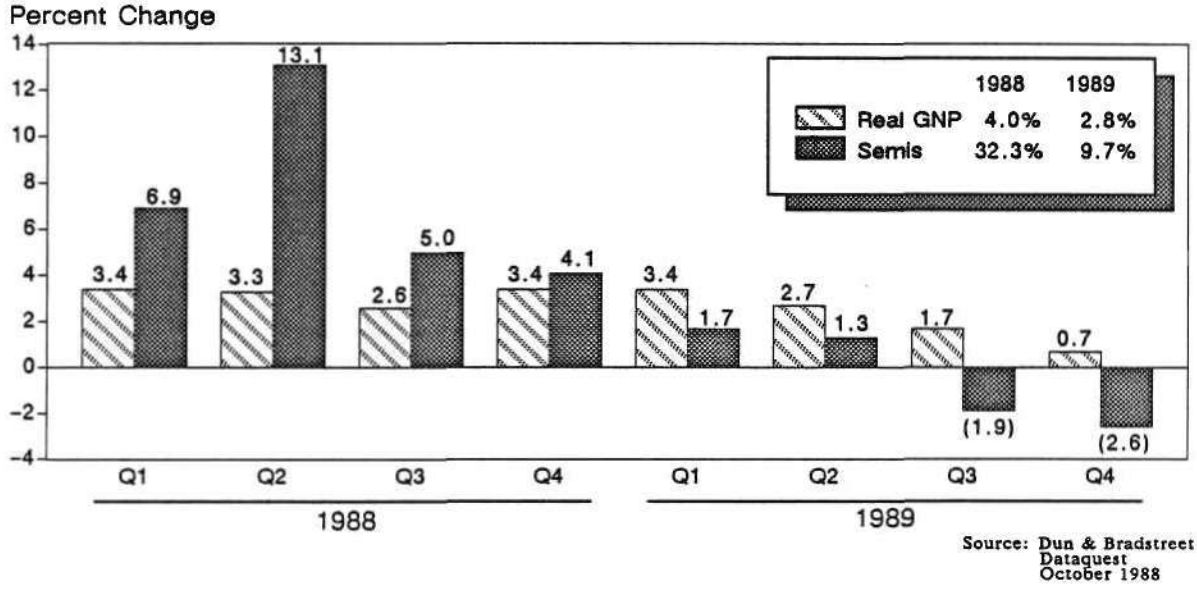
Both in the 1988 to 1989 time frame and over the long term, we believe that North America will be the second slowest growing market after Europe; through 1993, however, it will remain second largest in overall size after Japan. In 1988, North America will account for 31.7 percent of worldwide semiconductor consumption. Although capital spending in North America will increase by some 40.0 percent in 1988, this growth is modest compared with the capacity buildup in 1983 and 1984, which led to the 1985 market glut.

Historical patterns of billings and bookings show that bookings may begin to fall on a 12/12 basis any time now, but billings will not start to decline until 9 to 10 months later (i.e., mid–1989). Semiconductor inventory levels are rising, but they are being held in better check by OEMs than in 1984, due to careful tracking of target and actual inventory levels.

Dun & Bradstreet forecasts show that the U.S. economy will slow in 1989, with real GNP growth of 2.8 percent, versus 4.0 percent growth in 1988. This reduced GNP growth, combined with slower electronic equipment production growth and lowered capital expansion plans, will slow the semiconductor industry as well. We believe that the sluggishness in semiconductors will last through the first half of 1990. Figure 2 compares U.S. GNP growth with North American semiconductor consumption growth.

Figure 2

U.S. Economy versus Semiconductors



Source: Dun & Bradstreet
Dataquest
October 1988

Japan

The GNP outlook for Japan is very strong, with growth rates forecast at 4.6 percent for fiscal 1988 and 3.5 percent for fiscal 1989. We expect Japan to be the second fastest growing market after the ROW market, in both the short and long term. We expect prices to remain firm through the second half of this year, with shortages of DRAMs and SRAMs continuing at least until the first quarter of 1989 (one quarter sooner than in the United States). Although Japanese capital spending will grow 56.0 percent in dollar terms in 1988, the yen growth will be significantly lower, at 40.0 percent.

Europe

PCs are the driving factor in European semiconductor growth this year, particularly in MOS microdevices, memory, and bipolar digital logic. The PC build rate has slowed substantially, and bookings are collapsing, except for 1Mb DRAMs. We expect Europe to be the slowest growing market in the long term, and we believe that ROW will surpass Europe in dollar size in 1991.

ROW

The 1988 Seoul Olympics drove 1988 consumer demand worldwide, stimulating the ROW semiconductor market. Currently, PC shipments are slowing because of memory shortages. The telecommunications industry is growing extremely quickly in ROW, but telecommunications is still a small market. We expect the ROW market to be the fastest growing in both the short and long term. ROW will surpass Europe in total dollar consumption in 1991 to become the world's third largest market.

Shipments by Product

Tables 3 and 4 give Dataquest's short- and long-term forecasts, respectively, for the worldwide semiconductor industry. By 1993, we forecast a total market of $86.7 billion. In the long term, the fastest growing products will continue to be MOS ICs. Bipolar memory is forecast to decline steadily through 1993, as BICMOS memory edges it out. Optoelectronics growth will continue to be strong over the long term, as its use in consumer and telecommunications products continues to grow; at the same time, new applications such as medical, dental, machine vision, and submarine communications are proliferating.

Table 3

Estimated Worldwide Semiconductor Shipments
(Millions of U.S. Dollars)

	1987	Q1/88	Q2/88	Q3/88	Q4/88	1988	% Chg. 1988
Total Semiconductor	$36,449	$11,112	$12,442	$12,669	$13,286	$49,509	35.8%
Total IC	$28,619	$ 8,718	$ 9,885	$10,128	$10,672	$39,403	37.7%
Bipolar Digital	$ 4,672	$ 1,297	$ 1,359	$ 1,419	$ 1,495	$ 5,570	19.2%
Memory	565	154	163	166	169	652	15.4%
Logic	4,107	1,143	1,196	1,253	1,326	4,918	19.7%
MOS Digital	$16,739	$ 5,385	$ 6,380	$ 6,561	$ 6,924	$25,250	50.8%
Memory	6,019	2,182	2,762	2,785	2,904	10,633	76.7%
Micro	4,770	1,521	1,765	1,813	1,906	7,005	46.9%
Logic	5,950	1,682	1,853	1,963	2,114	7,612	27.9%
Linear	$ 7,208	$ 2,036	$ 2,146	$ 2,148	$ 2,253	$ 8,583	19.1%
Discrete	$ 6,112	$ 1,805	$ 1,918	$ 1,887	$ 1,939	$ 7,549	23.5%
Optoelectronic	$ 1,718	$ 589	$ 639	$ 654	$ 675	$ 2,557	48.8%
Exchange Rate Yen/$	144	128	125	134	134	130	(9.7%)
European Basket/$	1.25	1.17	1.17	1.20	1.20	1.18	(5.6%)

	1988	Q1/89	Q2/89	Q3/89	Q4/89	1989	% Chg. 1989
Total Semiconductor	$49,509	$13,556	$13,843	$13,636	$13,536	$54,571	10.2%
Total IC	$39,403	$10,882	$11,104	$10,917	$10,833	$43,736	11.0%
Bipolar Digital	$ 5,570	$ 1,518	$ 1,519	$ 1,451	$ 1,400	$ 5,888	5.7%
Memory	652	169	161	151	146	627	(3.8%)
Logic	4,918	1,349	1,358	1,300	1,254	5,261	7.0%
MOS Digital	$25,250	$ 7,058	$ 7,209	$ 7,101	$ 7,057	$28,425	12.6%
Memory	10,633	2,950	3,022	2,972	2,953	11,897	11.9%
Micro	7,005	1,944	1,990	1,969	1,959	7,862	12.2%
Logic	7,612	2,164	2,197	2,160	2,145	8,666	13.8%
Linear	$ 8,583	$ 2,306	$ 2,376	$ 2,365	$ 2,376	$ 9,423	9.8%
Discrete	$ 7,549	$ 1,976	$ 2,010	$ 1,996	$ 1,988	$ 7,970	5.6%
Optoelectronic	$ 2,557	$ 698	$ 729	$ 723	$ 715	$ 2,865	12.0%
Exchange Rate Yen/$	130	134	134	134	134	134	3.1%
European Basket/$	1.18	1.20	1.20	1.20	1.20	1.20	1.2%

Source: Dataquest
October 1988

Table 4

Estimated Worldwide Semiconductor Shipments
(Millions of U.S. Dollars)

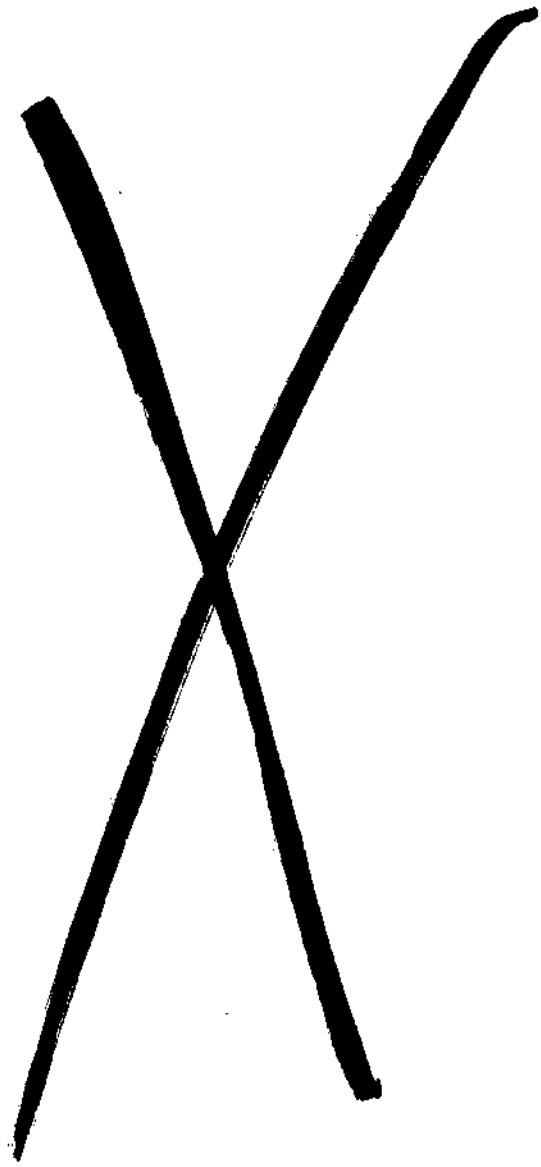
	1988	1989	1990	1991	1992	1993	CAGR 1988-1993
Total Semiconductor	$49,509	$54,571	$55,600	$65,230	$79,233	$86,730	11.9%
Total IC	$39,403	$43,736	$44,767	$53,295	$65,734	$73,213	13.2%
Bipolar Digital	$ 5,570	$ 5,888	$ 5,878	$ 6,737	$ 7,813	$ 8,509	8.8%
Memory	652	627	606	595	546	530	(4.1%)
Logic	4,918	5,261	5,272	6,142	7,267	7,979	10.2%
MOS Digital	$25,250	$28,425	$29,333	$35,487	$44,610	$49,663	14.5%
Memory	10,633	11,897	12,141	14,762	18,562	20,262	13.8%
Micro	7,005	7,862	7,993	9,800	12,482	13,867	14.6%
Logic	7,612	8,666	9,199	10,925	13,566	15,534	15.3%
Linear	$ 8,583	$ 9,423	$ 9,556	$11,071	$13,311	$15,041	11.9%
Discrete	$ 7,549	$ 7,970	$ 7,917	$ 8,668	$ 9,712	$ 9,254	4.2%
Optoelectronic	$ 2,557	$ 2,865	$ 2,916	$ 3,267	$ 3,787	$ 4,263	10.8%
Exchange Rate Yen/$	130	134	134	134	134	134	
European Basket/$	1.18	1.20	1.20	1.20	1.20	1.20	

Source: Dataquest
October 1988

DATAQUEST CONCLUSIONS

We believe that worldwide semiconductor shipments will slow down through the first half of 1989 and begin to decline slightly in the second half of 1989, continuing into the first half of 1990. However, due to careful OEM management of semiconductor inventory, careful semiconductor manufacturer management of capacity (capacity utilization is at 86 percent in 1988, and we expect it to be a still-healthy 80 percent in 1989 and 78 percent in 1990), and a generally healthy world economy, we forecast the downturn to be modest, particularly in comparison with the 1985 industry depression.

Patricia S. Cox



Dataquest
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The Dun & Bradstreet Corporation

Research *Newsletter*

SEMS Code: 1987–1988 Newsletters: November
1988–27
0001925

"AND THEN THERE WERE NONE . . . "
LAST MAJOR U.S. SILICON SUPPLIER TO BE ACQUIRED BY EUROPEAN FIRM

SUMMARY

The rumors surrounding Monsanto Company for the last several years finally are founded in fact. On November 9, Monsanto announced that it had signed a letter of intent concerning the sale of its silicon operations (Monsanto Electronic Materials Company) to Huels AG of West Germany. This agreement puts Monsanto, the last major U.S. silicon company, under European ownership and reduces the U.S.–owned merchant silicon wafer supplier base to a handful of small, niche–oriented companies. While this acquisition is not expected to become final until early 1989, this newsletter examines the potential impact of this decision by looking at the following issues:

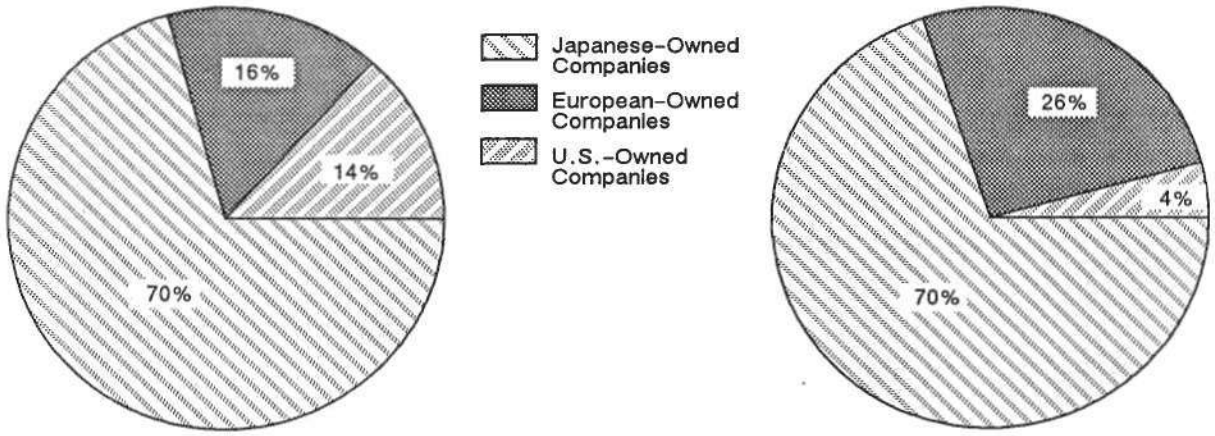
- The shift in market share of regionally owned silicon companies
- The whys and wherefores behind Monsanto's decision to leave the market
- The emergence of a new and greatly strengthened European force in the silicon wafer industry

SHIFTS IN SHARE

Perhaps the most significant aspect of Huels AG's acquisition of Monsanto is that the U.S.–owned silicon supplier base has been reduced to an inconsequential position in the world merchant silicon industry. Based on 1987 market analysis, Figure 1 illustrates that the acquisition of Monsanto will result in a substantial decline in market share of U.S.–owned silicon companies from 14 to 4 percent. The impact on market share in the United States is significant, particularly with the share of U.S.–owned merchant silicon companies dropping from 45 to 16 percent in the home market if the proposed acquisition is approved. This can be compared with the early 1970s when U.S.–owned silicon suppliers enjoyed 100 percent of their domestic market.

Figure 1

1987 World Merchant Silicon and Epitaxial Wafer Market
By Regional Corporate Ownership



Total = $1,836.0 Million

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Source: Dataquest
November 1988

Of the nine remaining U.S. merchant wafer companies, eight had 1987 world sales ranging from $1.0 million to $9.5 million. These companies can be characterized as niche-oriented players that supply products based on custom wafer specifications. The ninth company, Cincinnati Milacron, had sales of $34.0 million in 1987, but this was entirely epitaxial wafers, the majority of which were for discrete device applications. In addition, Cincinnati Milacron may be exiting the wafer business. In February 1988, the corporate office announced its plans to sell its semiconductor materials division as part of a restructuring plan.

With the Monsanto acquisition, silicon production by U.S.-owned merchant suppliers will drop below the level of captive silicon production in the United States. Captive silicon producers are those semiconductor manufacturers that grow single-crystal silicon to produce wafers for their own consumption. In the United States, four semiconductor manufacturers—AT&T, IBM, Motorola, and Texas Instruments—have captive silicon operations, typically maintained for manufacturing wafers with custom specifications as well as providing familiarity with silicon technology. No captive silicon producer relies solely on its internal production for its silicon consumption requirements.

MONSANTO

Monsanto is, and has been, the acknowledged leader among U.S. merchant silicon wafer suppliers. Financial reports, however, reaching back into the early 1980s, reveal that the silicon operations have returned little if any profits to their corporate parent over the past six years (see Table 1). Dataquest believes that this poor financial

performance and the tremendous swings in the semiconductor business cycle, coupled with Monsanto Company's corporate focus on agricultural products, the life sciences, and biotechnology, ultimately made the Electronic Materials division an unattractive component in the company's portfolio.

Table 1

Monsanto Electronic Materials Company
Net Sales and Operating Income
(Millions of Dollars)

	1983	1984	1985	1986	1987	1988*
Net Sales	$120	$220	$137	$154	$185	$187
Operating Income (Loss)	($ 56)	$ 4	($ 84)	($139)	($ 5)	$ 8

*First nine months of calendar year 1988

Source: Monsanto Company

It is interesting to note that all of the major merchant silicon companies in the world today have large corporate parents. This provides a cash flow buffer against downturns in the business cycle, as well as a source of funding for new facilities and capacity expansions. In today's competitive business environment, it is not clear that a standalone entrepreneurial silicon operation could compete and survive against the major silicon suppliers that have extensive financial backing from their corporate parents. It is, therefore, not surprising that a suitor for Monsanto would fall into this category.

WHO IS HUELS?

Huels AG, a subsidiary of Veba AG, is a diversified chemical company based in Marl, West Germany. The company has annual sales of approximately $5 billion. Huels' first venture into the silicon wafer industry was in May 1987, when it was announced that Huels would acquire the silicon and photoresist operations of Dynamit Nobel AG. As Table 2 illustrates, the combined operations of DNS Electronic Materials and Monsanto offer Huels an impressive international manufacturing presence.

Together, the Monsanto and DNS Electronic Materials operations place Huels in a commanding position within the merchant silicon industry, with combined 1987 wafer sales of $248 million. As shown in Table 3, this corresponds to a ranking of third in the world merchant silicon and epitaxial wafer market after Shin-Etsu Handotai and Mitsubishi Metal of Japan. With these two very strategic acquisitions, Huels also has catapulted over long-time European silicon leader, Wacker Chemitronic, which ranked fifth in world sales in 1987.

Table 2

Huels AG Silicon Plant Locations

Location	Polysilicon	Single-Crystal Ingots	Wafers	Technical Center
DNS Electronic Materials				
Merano, Italy	X	X		
Novara, Italy			X	
Research Triangle Park, North Carolina			X	
Sunnyvale, California				X
Monsanto				
Saint Peters, Missouri	X*	X	X	X
Spartanburg, South Carolina		X	X	
Kuala Lumpur, Malaysia			X	
Utsonomiya, Japan			X	
Milton Keynes, United Kingdom			X	
Gumi, South Korea**			X	

*This facility currently is not operational.
**It is not yet clear if the acquisition of Monsanto's silicon operations will include its joint venture in Korea, Korsil Company, Ltd.

Source: Dataquest
November 1988

Table 3

1987 World Merchant Silicon Company Ranking Before and After the Monsanto Acquisition (Millions of Dollars)

Ranking Before	Ranking After	Company	Silicon and Epitaxial Wafer Sales
1	1	Shin-Etsu Handotai	$484.7
2	2	Mitsubishi Metal	265.3
3	4	Osaka Titanium Company	235.5
4	5	Wacker	214.8
5	6	Komatsu Electronic Metals	197.3
6	-	Monsanto	185.0
7	7	Toshiba Ceramics	78.9
8	3	Huels AG*	63.0

*Includes DNS Electronic Materials

Source: Dataquest
November 1988

DATAQUEST ANALYSIS

Problems with Profitability

While Monsanto's financial history has been made public through annual reports, Dataquest believes that the silicon wafer supplier is not alone in its problems with profitability over the last several years. We believe that several factors are significantly impacting the profitability of many of the silicon wafer companies around the world. Overall silicon consumption (in square inches) is experiencing slower growth than semiconductor device production revenue, as device manufacturers improve yields and high-priced devices become a larger part of the product mix. Competition is becoming more intense as several new silicon companies enter the marketplace. Finally, wafer pricing pressures have been fueled not only by increasing competition but by demands from cost-conscious semiconductor manufacturers as well. Dataquest believes that it is only in 1988 that silicon wafer companies have returned to profitability as a result of long-awaited wafer pricing increases going into effect.

Acquisition Activities

Rumors have flourished for the last several years regarding the possible sale of Monsanto's silicon operations, partly because of its poor financial performance and partly because several other U.S. silicon operations have been acquired by Japanese silicon suppliers. In 1986, Mitsubishi Metal acquired Siltec Corporation, a silicon wafer and equipment supplier, while Osaka Titanium Company acquired U.S. Semiconductor, a small epitaxial wafer company. In 1985, Kawasaki Steel acquired NBK Corporation, a Silicon Valley-based wafer company, while Nippon Kokan K.K. bought the Great Western polysilicon facility in Arizona. (Shin-Etsu Handotai and Wacker established a strong presence in the United States through wholly owned subsidiaries founded in the late 1970s.)

In light of these recent acquisitions, Dataquest has maintained the position that if Monsanto were to be acquired, it would be unlikely that the U.S. government, with its recent intervention in the Fairchild-Fujitsu case and ongoing trade friction with Japan, would allow Monsanto to be acquired by a Japanese corporation.

Strategic Loss?

With the announcement of the proposed Monsanto acquisition, many industry watchers and participants are bemoaning the loss of the domestically owned merchant silicon supplier base in the United States. Some also speculate whether silicon will be considered a strategic material by the U.S. government and thus trigger its involvement in this acquisition. Certainly, regulatory approvals of the Hart-Scott-Rodino Antitrust Act must be met before the acquisition is finalized. Whether provisions of the Omnibus Trade Bill recently signed by the U.S. Congress will be invoked is still not clear. The trade bill amends Title VII of the Defense Production Act of 1950, allowing the president of the United States to block a foreign takeover if it is determined, upon investigation, that U.S. national security is compromised.

Finally, the ultimate irony of the Monsanto acquisition may be the issue of who will supply SEMATECH with silicon wafers. As conceived, the main purposes of SEMATECH are to revitalize manufacturing excellence and help build a stronger domestic supplier base in the United States for semiconductor equipment, materials, and devices. SEMATECH could, of course, rely on one of its member companies that has captive silicon production to provide silicon wafers, but it is more likely that merchant suppliers will be called upon to provide their services. If the Monsanto acquisition is approved, SEMATECH will have to look to European or Japanese silicon companies to provide it with the wafer material and technology required to build tomorrow's advanced devices.

Peggy Marie Wood

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Research Newsletter

SEMS Code: 1987–1988 Newsletters: November
1988–26
0001945

THE THREE FACES OF JAPAN: CONSUMER, PARTNER, COMPETITOR

SUMMARY

During the past decade, Japan's impact on the worldwide semiconductor industry has been characterized in a variety of ways. Japan has been cast as a low–cost, high–reliability source of commodity ICs, a market spoiler, a technology pirate, the driver of leading–edge processes, a strategic partner, and a market prize. For many U.S. companies, alternately understanding the Japanese as consumers, partners, and competitors amid all the current media hyperbole is a difficult exercise.

Dataquest's Japanese Semiconductor Industry Service (JSIS) recently conducted a half–day seminar to provide an update on various aspects of the Japanese semiconductor industry: its markets, manufacturers, and end–use drivers. From this seminar emerged a number of insights regarding the Japanese semiconductor industry. Among these were the following:

- From a $132 billion figure in 1988, the production value of Japan's electronics equipment is forecast to reach nearly $190 billion by 1992. Dataquest believes that the if–sold value of these goods will surpass the U.S. electronics industry at this time.
- Having become the world's largest semiconductor market in 1986, Japan's consumption of devices by 1991 will exceed $21 billion.
- In 1980, the number of semiconductor alliances entered into by Japanese suppliers could have been counted on one hand. In 1986 alone, Japanese semiconductor agreements numbered more than 100.
- Through the Neural Computer Project undertaken by Japan's Ministry of International Trade and Industry (MITI), current research is paving the way for a massively parallel computer using neural networks and/or biodevices. Dataquest expects stunning breakthroughs in system and chip architectures stemming from this program and others in the 1990s.

This newsletter distills a number of recent Dataquest research efforts in order to characterize the Japanese semiconductor industry as a device consumer, a strategic alliance partner, and a growing competitive force worldwide.

JAPAN THE CONSUMER

In 1987, yen-based Japanese electronic equipment production was nearly flat, with negative growth rates in the industrial and consumer electronics segments. Despite the continued appreciation of the yen, however, Japan's electronic equipment industry is currently in recovery, with 15 percent growth in yen and 27 percent growth in dollars forecast for 1988. Dataquest expects this recovery to last until mid-1989.

The macroeconomic factors behind this growth are easy enough to understand—Japan's GNP growth for 1987 is expected to be 4 percent. What is more significant is that export-oriented Japan is being spurred by increased domestic demand, which contributed to 5 percent of its economic growth in 1987. Dataquest believes that private sector and domestic demand will continue leading the Japanese economy into 1989, with data processing, communications, and industrial electronic equipment output as well as consumer electronics growing.

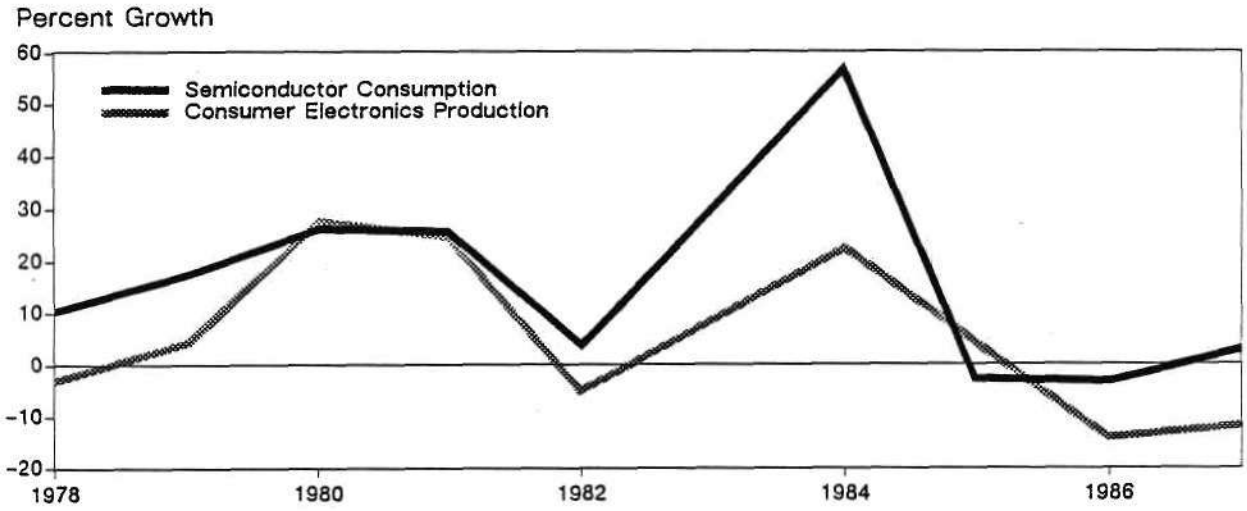
The nature of Japan's electronic equipment industry is changing rapidly. Analysts in Dataquest's Semiconductor User and Applications Group believe that in the period between 1987 and 1991, Japan's personal computer market will double in dollar-based production value, growing at a compound annual rate of 18.4 percent—well over twice that of color TVs and VCRs. By 1991, Dataquest believes that the production value of PCs and mainframe computers in Japan will be roughly equal in dollars to the combined total of its VCR and TV production.

The Japanese consumer electronics industry is no longer the driving force in the Japanese semiconductor market, although it accounted for better than 32 percent of semiconductor consumption in 1987. In fact, as Figure 1 illustrates, semiconductor consumption in the consumer segment has not grown for the past three years. Dataquest estimates that consumer electronics production in Japan will increase by 7.6 percent in 1988. By contrast, however, computer production in Japan grew 15 percent in 1987 and has maintained this strong growth through 1988. The computer/data processing market now accounts for nearly 43 percent of Japan's semiconductor consumption.

With computer manufacturing growing in importance, microprocessor (MPU), controller, and peripheral device consumption will surge. Traditional growth products such as linear ICs and discrete components will grow more slowly due to lower demand for consumer electronics equipment. Table 1 shows Dataquest's near term analysis of the Japanese semiconductor market by major product area.

Figure 1

Semiconductor Consumption versus Consumer Electronics Production



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Source: Dataquest
November 1988

Table 1

Estimated Japanese Semiconductor Consumption (Millions of Dollars)

	1987	1988	1989
Total Semiconductor	14,329	19,149	21,141
Total IC	11,006	14,986	16,634
Bipolar Digital	1,491	1,981	2,148
Memory	183	299	323
Logic	1,308	1,682	1,825
MOS	6,327	8,979	10,211
Memory	2,311	3,633	4,355
Microdevice	1,732	2,442	2,706
Logic	2,284	2,904	3,150
Linear	3,188	4,026	4,275
Discrete	2,424	3,043	3,266
Optoelectronic	899	1,120	1,241
Exchange Rate (¥ per $1)	130	125	124

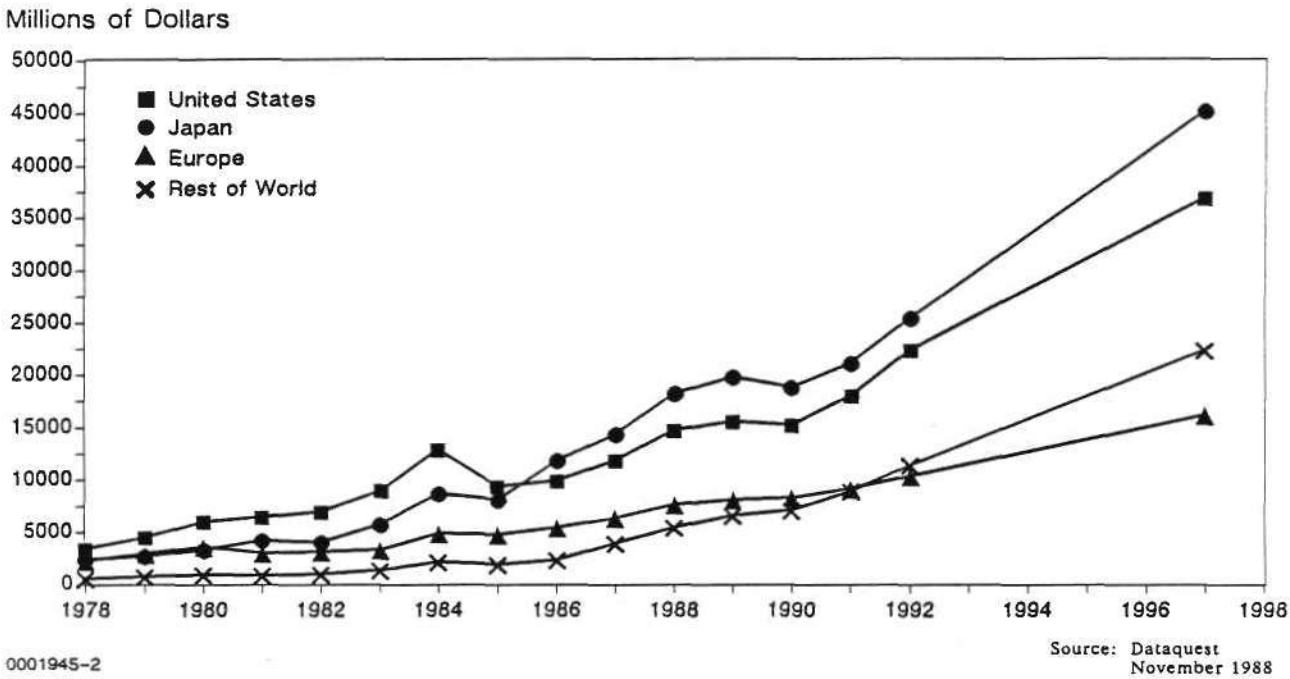
Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
November 1988

W.E. Davis, vice president of the Semiconductor Industry Association (SIA), recently noted that Japan and the Pacific Rim will account for two-thirds of the world's semiconductor consumption by the year 2000. Figure 2 compares regional consumption for the world, illustrating the fact that not only has Japan become the world's largest consumer of semiconductor devices since 1986, but that it will continue to outpace all other world markets for the foreseeable future.

Figure 2

Estimated Semiconductor Consumption by Region



In light of Japan's changing semiconductor market, Dataquest believes that the best potential for increased penetration by foreign suppliers will be in the following product areas:

- 32-bit microprocessors, RISC, and SPARC architectures
- Digital signal processing (DSP)
- Complex standard cells and software
- High-performance bipolar devices

- Video digital-to-analog converters
- Analog devices

JAPAN THE PARTNER

Since 1980, Dataquest has recorded more than 350 strategic alliances between Japanese semiconductor producers and other Japanese or foreign companies. In the early 1980s, agreements generally involved one-way licensing or second-sourcing of U.S. microprocessors and ASICs and joint developments between U.S. and Japanese equipment makers. In most cases, these agreements were signed during the 1983-to-1984 boom years because of inadequate U.S. fab capacity and marketing presence in Japan. Several agreements ended up in court during the 1985 downturn as some of the Japanese partners began competing for a shrinking market.

Like the semiconductor market itself, the nature of Japanese alliances has been changing. More recent Japanese semiconductor alliances have become more sophisticated and varied, reflecting the shift of Japanese companies into application-specific memories, high-end microprocessors, smart cards, signal processors, CAD tools, power MOSFETs, and other emerging areas. CAD tools and software constituted a particularly hot alliance area in 1987, with Fujitsu, Hitachi, and Toshiba actively entering agreements to bolster their CAD capabilities in the fiercely competitive ASIC market. Table 2 lists these alliances.

Table 2

Japanese Semiconductor CAD Tool Alliances in 1987

Japanese Company	Partner	Product
Toshiba	SDA Systems	ASICs CAD software
Nippon Steel	Sun Microsystems	CAD workstations
Fujitsu Facom	Nippondenso (Japan)	Analog IC CAD system
Fujitsu	Tektronix	Gate array workstation
NEC/Fujitsu/Hitachi/ Toshiba/Mitsubishi	SDA Systems	ASICs CAD software
Tokyo Electron	Sun Microsystems	CAD OEM agreement
Seiko Instruments	Tangent Systems	CAD software
Toshiba	Viewlogic Systems	PC-based CAE software
Hitachi/Toshiba	FutureNet	Simulation library
Toshiba	Tangent Systems	Channelless array CAD

Source: Dataquest
November 1988

JAPAN THE COMPETITOR

Where Japan has been frustrated in its alliance efforts, most notably in obtaining 32-bit microprocessor technology from U.S. companies, it has turned inward. No better example of this exists than the TRON (The Real-time Operating Nucleus) Project. Starting out with a man-machine interface, TRON has progressed to an operating system followed by a microprocessor architecture. The TRON concept has now developed along several application areas: BTRON for personal computers, CTRON for mainframes, and ITRON for industrial applications. In January of this year, the "Gmicro Group," a chip technology committee made up of Fujitsu, Hitachi, and Mitsubishi Electric, announced that it had successfully developed a 32-bit microprocessor and three models of peripheral chips based on TRON technology. Hitachi, under whose auspices the 32-bit MPU was developed, is expected to begin volume production of the device, the GMICRO0200, in the fall of this year.

Table 3 provides a list of the major Japanese companies involved in the various TRON committees and reveals the extent of their unity in creating an industry standard, multiapplication computing engine. This show of unity compares favorably (for the Japanese) with the fractiousness of the U.S. microprocessor market. Those who view TRON as an attempt by Japanese companies to go head-to-head with Intel or Motorola in the microprocessor arena miss the point. Japan simply does not want to be dependent on the United States for the microprocessor technology that will define its future electronics systems.

Table 3

TRON Project Organization

	ITRON Technology Committee	BTRON Technology Committee	CTRON Technology Committee	Chip Technology Committee
Hitachi	O	O	O	X
Fujitsu	O	O	O	X
Mitsubishi	O	O	O	X
Toshiba		O	O	O
NEC	O	O	O	
Matsushita		O		O
Oki		O	O	O
NTT			O	

O = Under development
X = Gmicro family

Source: Dataquest
November 1988

The increased efforts at consensus between U.S. chip manufacturers, represented by the SIA, and chip users, represented by the American Electronics Association (AEA), acknowledge the recognition by both industries that Japan's greatest threat as a chip competitor will ultimately come about through its success in systems. Conversely, its greatest threat as a competitor in the systems arena will come about through its success in higher-integration chips such as ASICs and MPUs and advances in materials and interconnect technology.

While Japan's impact on the U.S. data processing market has up until now been most visible in the laptop PC segment, Dataquest expects to see a future increase in the export of office automation and personal communications products from Japanese companies that made their initial inroads into the U.S. market through consumer electronics. Examples of such horizon products include:

- Home control systems
- Auto navigation systems
- Built-in phone/fax systems for autos
- Memo-to-text and graphics electronic tablets for rapid production of hard copy and transparent overheads
- "PC watches" for internal office communications
- Videophone PCs
- Electronic shopping systems

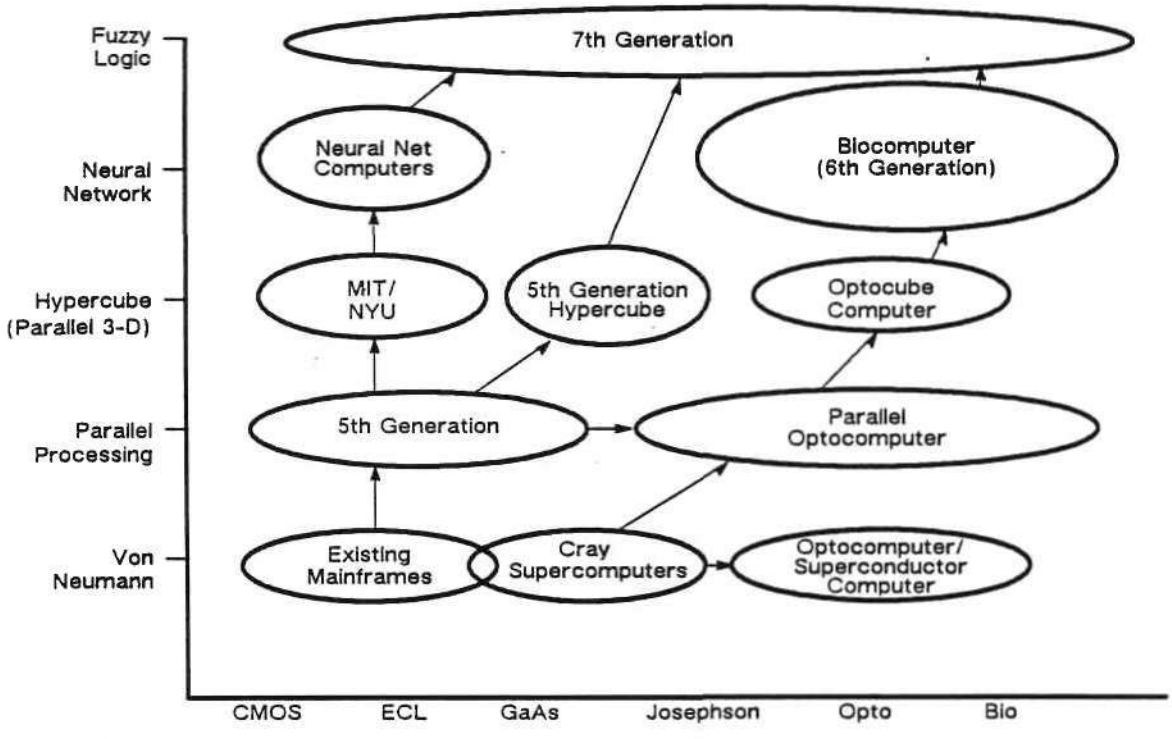
To support products such as these, component manufacturers will have to meet technology requirements in a number of areas. These will include 2-D and 3-D megabit memories (video and voice storage), specialized 32-bit MPUs (video and voice processing, parallel processing), optoelectronic ICs (semiconductor laser controllers and optical computing), and superconductors (ultrasupercomputing interconnection). Needless to say, the implementation of these technologies to systems solutions will require continued advances in submicron manufacturing, ASIC design, packaging, and interconnect techniques.

Looking beyond the office automation/data processing market as a driver of semiconductor technology, MITI and other Japanese government agencies have begun laying the foundations for next-generation computing in the 1990s and beyond. MITI recently announced the funding of a nine-year Neural Computer Project to begin in April 1989. The purpose of this project is to develop neural network systems and devices capable of massive parallel processing and "fuzzy" logic recognition. Dataquest believes that neural network technology will be the basis for breakthroughs in sophisticated ISDN voice, image, and pattern recognition computing and language translation.

MITI also expects the Neural Computer Project to complement its work on parallel processing and language translation currently under way in its Fifth-Generation Computer Project. Dataquest has observed intense research activity in Japan focusing on neural networks and fuzzy logic since the first IEEE Neural Network Conference in San Diego in June 1987. To place current Japanese computer projects in perspective, analysts in Dataquest's Japanese Semiconductor Industry Service have developed a technology road map for future computing systems, as shown in Figure 3. Today, existing mainframes and supercomputers have limited computing performance. Future computers will employ optical switches to link with optical communications and video systems, and hypercube architecture will be used for various technologies. In MITI's Biocomputer Project, neural network and bioelectronic research are converging.

Figure 3

Future Computing Trends



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Source: Dataquest November 1988

DATAQUEST CONCLUSIONS

In support of its current and future systems demands, the Japanese semiconductor industry has entered into a new era. The industry of pre-1985 Japan was marked by commodity ICs, microprocessor licensing and second-source deals, and DRAM dominance. The post-1985 Japanese semiconductor industry is witnessing the development of ASICs and CAD software, proprietary microprocessors (TRON and RISC), and an increasing interest in specialty memories.

In the battle to keep the U.S. semiconductor industry a world-class competitor, domestic chip producers are engaged in a number of major skirmishes: dumping prevention, increased access to the Japanese market, more effective protection of intellectual property, and the use of consortia to improve manufacturing technology. The U.S. could conceivably win all of these battles, however, and still lose the war. As James Smaha, the head of National Semiconductor's components division, has put it, "application drives specification." If Japan ultimately sets the pace for future electronics systems, it will be in the position of defining component product standards. In such an environment, the U.S. chip industry will have to choose between adhering to such standards and accepting the role of follower rather than leader or fighting against them and risking isolation and irrelevance.

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George Burns
Michael J. Boss

Dataquest
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Research *Bulletin*

SEMS Code: 1987–1988 Newsletters: December
1988–28
0002116

"AND THEN THERE WERE LESS THAN NONE . . ." OTC TO ACQUIRE EPI WAFER DIVISION OF CINCINNATI MILACRON

As 1988 draws to a close, another rumor in the silicon wafer industry has been put to rest. On December 2, Osaka Titanium Company (OTC) of Japan announced that it is negotiating to purchase the semiconductor materials division of Cincinnati Milacron, one of the largest suppliers of epitaxial wafers in the United States. This announcement comes fast on the heels of last month's news regarding the intent of West German Huels AG to acquire Monsanto's silicon operations. (Please refer to SEMS Newsletter 27, "And Then There Were None . . .") This bulletin briefly examines the impact of this latest announcement on regionally owned company shares, provides a snapshot of Cincinnati Milacron's epi operations, and concludes with comments on OTC's strategy for growth in the 1990s.

SHIFTS IN SHARE—REVISITED

The impact of both the Monsanto and Cincinnati Milacron acquisitions on the shift in regionally owned silicon company market shares is illustrated in Table 1. Based on 1987 market analysis, the silicon market share of U.S.–owned merchant silicon companies drops to a mere 2 percent of the world market and 8 percent of the domestic market if these two acquisitions are approved.

Table 1

Shifts in Market Share of Regionally Owned Merchant Silicon and Epitaxial Wafer Companies

	1987 Actual Share	With Monsanto Acquisition	With Cincinnati Milacron Acquisition
World Market Share			
Japanese Companies	70%	70%	72%
European Companies	16%	26%	26%
U.S. Companies	14%	4%	2%
United States Market Share			
Japanese Companies	32%	32%	40%
European Companies	23%	52%	52%
U.S. Companies	45%	16%	8%

Source: Dataquest
December 1988

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 437-8000, Telex 171973, Fax (408) 437-0292

Eight merchant silicon and epitaxial wafer companies would still remain under U.S. ownership. These companies are small, niche-oriented players with 1987 world sales ranging from $1.0 million to $9.5 million. In addition, four captive silicon producers—AT&T, IBM, Motorola, and Texas Instruments—have internal silicon operations to supply some portion of their own requirements.

A LOOK AT CINCINNATI MILACRON

Cincinnati Milacron is a major manufacturer of robots and metrology and inspection systems for industrial automation applications. It had 1987 sales of $828 million. In February 1988, it announced a reorganization strategy that included plans to sell its semiconductor materials division and to restructure its machine tools and robot operations.

The company's epi wafer division (along with Monsanto) is one of the largest producers of epitaxial wafers in the United States, with estimated 1987 world sales of $34 million. Dataquest believes that approximately 70 percent of the company's epi business is for discrete semiconductor applications, with the remaining 30 percent directed at CMOS devices. In 1985, the epi wafer manufacturing facility in Maineville, Ohio, was expanded, and reportedly has production capacity to generate $125 million in epitaxial wafers sales per year if the facility were fully equipped. Historically, the company has built its own epitaxial reactors, which have not been for sale on the commercial epitaxial reactor market. Dataquest expects, however, that under OTC management, commercial reactors with new design features for process uniformity, reliability, and higher throughput also would be employed at the facility.

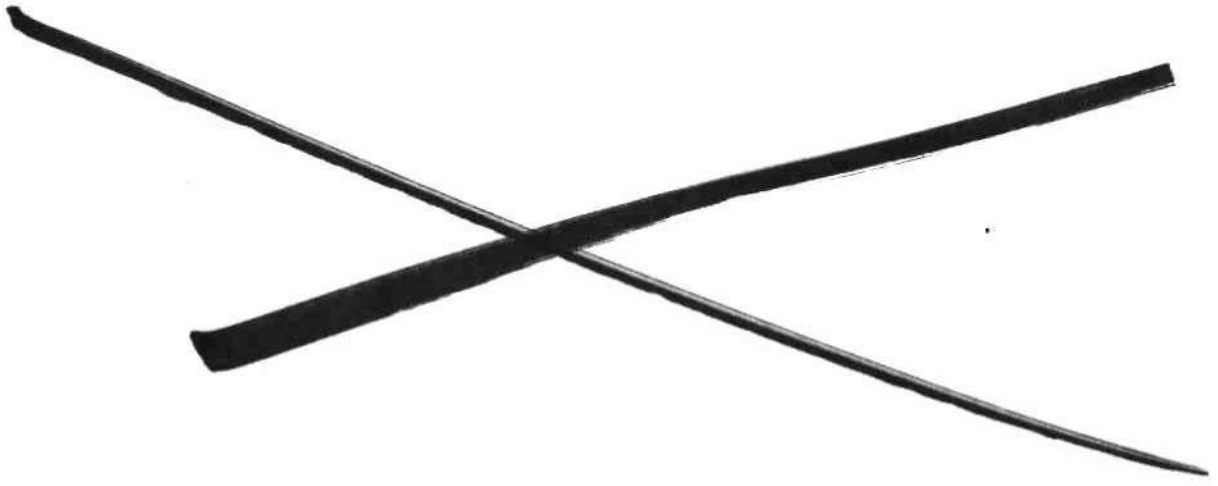
OTC STEPS IN

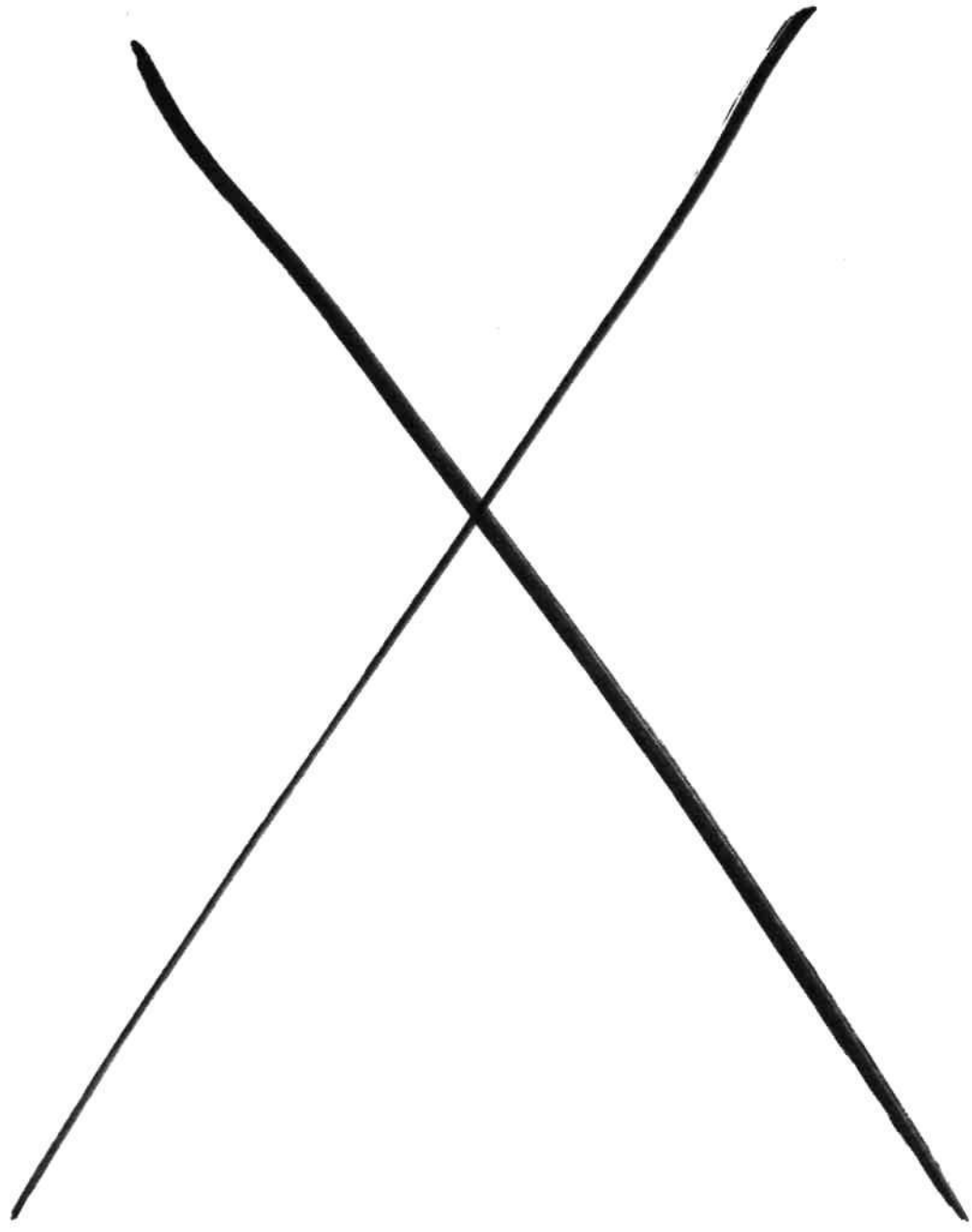
Dataquest expects that OTC's bid to acquire Cincinnati Milacron's epi operations would proceed along a relatively smooth course. While Cincinnati Milacron is the second largest U.S.-owned wafer supplier after Monsanto, its epi wafer business is niche oriented and, for the most part, has focused on discrete device applications. Unlike Monsanto, which has a worldwide manufacturing and distribution network and almost 40 percent of its sales outside the United States, Cincinnati Milacron has focused on the domestic market and had less than 10 percent of 1987 sales going to export markets. In addition, Cincinnati Milacron has only one-fifth the wafer sales level of Monsanto. Dataquest believes that because of these factors, the Cincinnati Milacron acquisition will not raise the level of concern that the Monsanto acquisition has generated.

Dataquest believes that the acquisition of Cincinnati Milacron epi operations is an important strategic move for OTC. While OTC is a major supplier in Japan, it recognizes that it must have a local manufacturing presence in the United States if it is to compete effectively in the long term. As part of this same strategy, OTC acquired U.S. Semiconductor, a Silicon Valley-based epitaxial wafer company, in 1986. The Cincinnati Milacron acquisition, however, brings a larger presence in the U.S. market, as well as expanded manufacturing capability. Dataquest believes that OTC would eventually use the Cincinnati Milacron facility to produce single-crystal ingots and polished wafers in the United States, in addition to its existing epi wafer operations.

OTC's two major competitors in Japan—Shin-Etsu Handotai (SEH) and Mitsubishi Metal—already have a significant manufacturing presence in the United States. SEH established a U.S. subsidiary in the 1970s, while Mitsubishi Metal acquired Siltec Corporation in 1986. With the acquisition of Cincinnati Milacron, OTC now would be well positioned to go head-to-head with these competitors in the United States as well as in Japan, and will have effectively charted a course for growth in the 1990s.

Peggy Marie Wood





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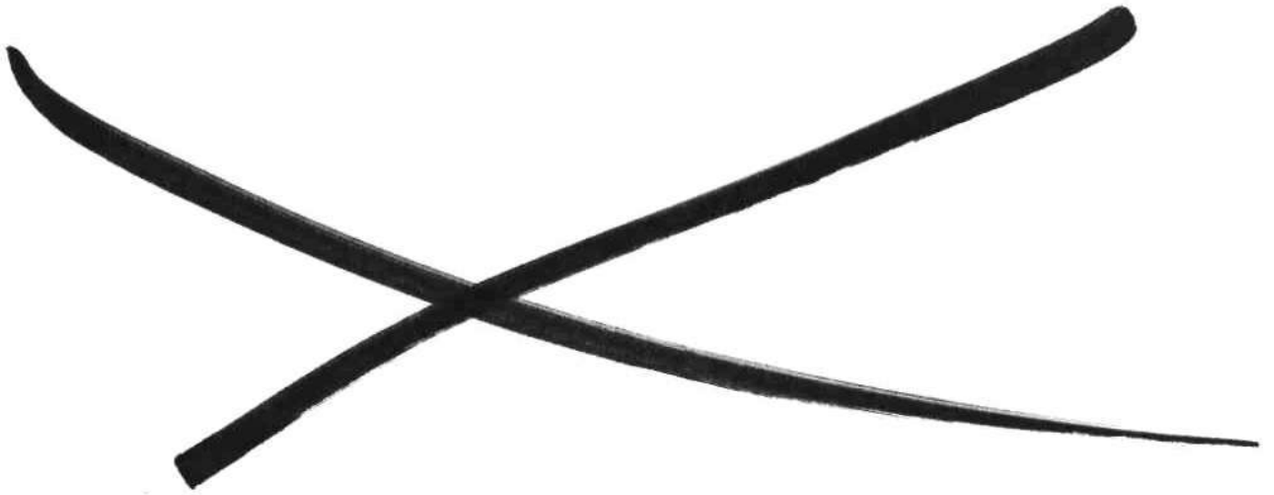

SEMS 1987 Newsletter Index

The 1987 SEMS Newsletter Index is a quick reference guide to the SEMS newsletters. It is structured as follows:

- Titles are organized by both subject and company.
  - Pages 2 and 3 are a company list, e.g., LSI Logic.
  - Pages 4 through 7 are a subject list, e.g., Memory.
- The newsletter type, month, and year follow each title listing in the index. Refer to the month tab to locate a specific newsletter.

This index is updated quarterly.

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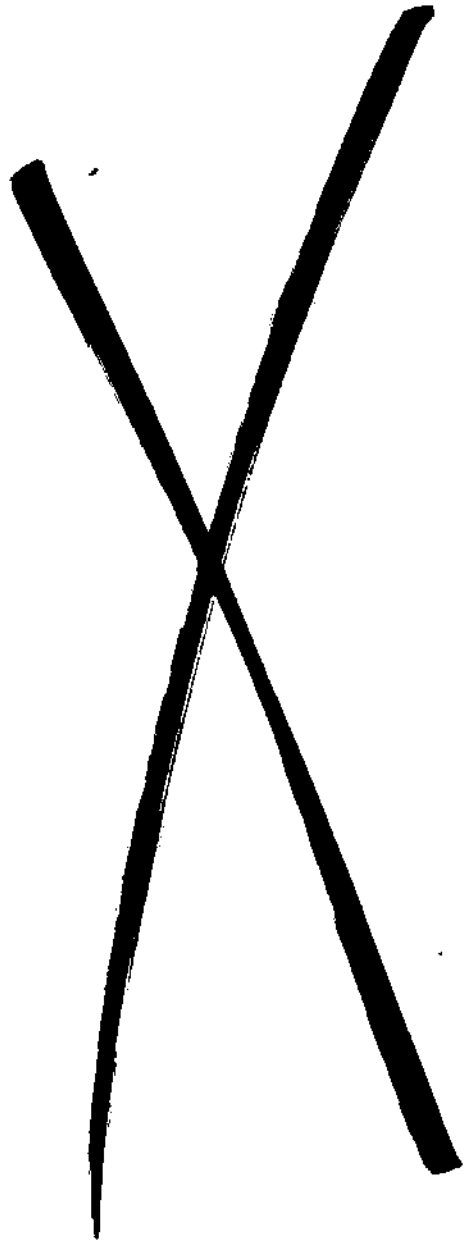

January Newsletters

The following is a list of the newsletters found in this section:

- Capital Spending in North America:
  Survey Results Point To Lift-Off In 1987
  1987 - #2

- SEMICON TOKYO 1986: What Goes Around, Comes Around
  1987 - #1

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RESEARCH NEWSLETTER

SEMS Code: 1987-1988 Newsletters, January 1987-2

CAPITAL SPENDING IN NORTH AMERICA: SURVEY RESULTS POINT TO LIFT-OFF IN 1987

DESCRIPTION OF A ROLLER COASTER RIDE

The results of Dataquest's latest survey of merchant semiconductor manufacturers are in. Most of the companies contacted by Dataquest indicate that they will increase their capital spending in 1987 (see Table 1). This long-awaited lift-off, however, was bought by two years of severe contraction--the most severe on record (see Figure 1).

Table 1

MAJOR MERCHANT CAPITAL SPENDING--1986 AND 1987
(Millions of Dollars)

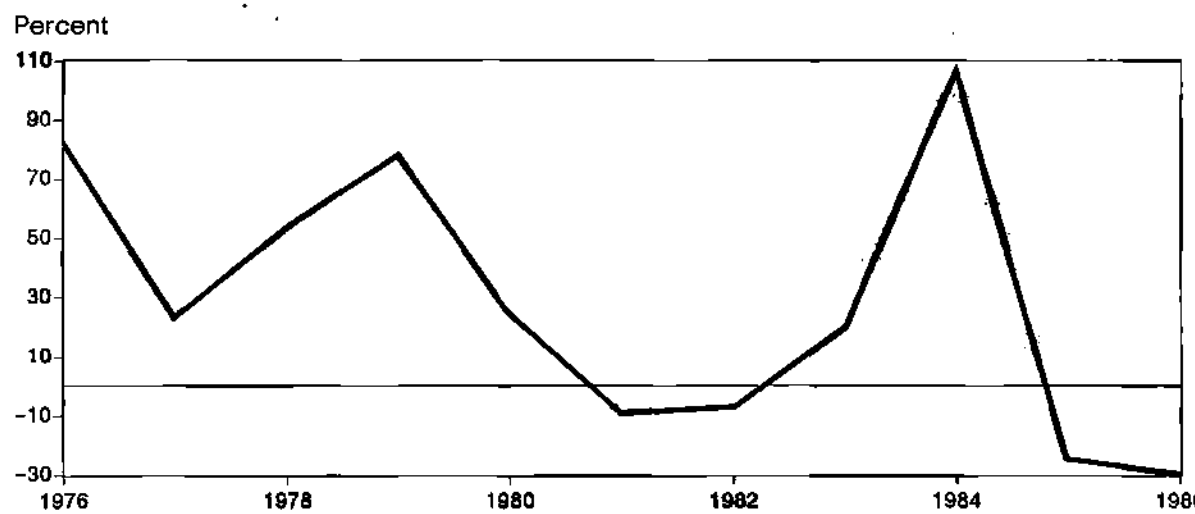
Company	1986	1987	Percent Change
AMD	$ 55	$ 63	14%
Analog Devices	$ 37	$ 43	15%
Fairchild	$135	$ 68	(50%)
General Electric	$ 90	N/A	N/A
Harris	$ 40	$ 30	(25%)
Intel	$150	$173	15%
MMI	$ 35	N/A	N/A
Motorola	$250	$275	10%
National Semiconductor	$117	$100	(15%)
Texas Instruments	$213	$230	8%
Thomson-Mostek	$ 9	$ 12	33%
Philips-Signetics	$ 60	$100	67%

N/A = Not Available

Source: Dataquest
January 1987

Figure 1

PERCENTAGE OF CHANGE IN NORTH AMERICAN CAPITAL SPENDING



Source: Dataquest
January 1987

This contraction was itself the result of the tremendous boom of 1984, when capital spending increased 110 percent (see Table 2). New manufacturing capacity was created by this boom, just as the semiconductor manufacturers in North America skidded into the recession of 1985. The result was a plummet of capacity utilization in North America from more than 90 percent in 1984 to a low of 56 percent in early 1986.

In our capital spending survey of a year ago, semiconductor manufacturers indicated that their capital spending in 1986 would be down. In the sections that follow, we will detail the capital spending activities of major North American merchant companies in 1986. We will also point to their planned activities for 1987--to what we hope will be the beginning of a solid and healthy recovery.

Table 2

NORTH AMERICAN COMPANY CAPITAL SPENDING
(Millions of Dollars)

Company	1975	1976	1977	1978	1979	1980
AMD	$ 1	$ 6	$ 10	$ 20	$ 39	$ 49
Analog Devices	2	4	7	12	10	19
Fairchild	20	36	15	23	58	83
Gould-AMI (1982)	2	3	4	5	10	13
Harris	N/A	N/A	N/A	N/A	N/A	45
Intel	11	32	46	104	97	156
MMI	N/A	N/A	N/A	N/A	4	6
Thomson-Mostek	3	10	24	19	42	85
Motorola	21	33	43	72	159	177
National Semiconductor	17	26	31	51	84	116
Philips-Signetics	4	10	19	40	50	90
Texas Instruments	35	62	88	122	251	300
Others	54	91	101	172	320	300
Total	$170	$312	$388	$639	$1,123	$1,438
Percent Change		84%	24%	65%	76%	28%

	1981	1982	1983	1984	1985	1986
AMD	$ 58	$ 67	$ 111	$ 237	$ 172	$ 55
Analog Devices	16	19	24	58	62	37
Fairchild	140	156	125	195	135	135
General Electric	N/A	N/A	64	107	81	90
Gould-AMI	17	27	31	38	30	12
Harris	45	35	25	50	50	40
Intel	157	138	146	388	214	150
MMI	20	25	25	52	49	35
Thomson-Mostek	98	47	78	123	39	9
Motorola	184	160	174	412	330	250
National Semiconductor	105	82	120	300	184	117
Philips-Signetics	115	55	58	133	50	60
Texas Instruments	145	140	232	472	281	213
Others	248	259	237	476	640	437
Total	$1,348	$1,210	$1,450	$3,041	$2,317	$1,640
Percent Change	(6%)	(10%)	20%	110%	(24%)	(29%)

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
January 1987

1986 AND 1987 NORTH AMERICAN COMPANY CAPITAL SPENDING

Only three of the companies contacted by Dataquest did not experience a decline in their 1986 capital spending. Capital spending for Philips/Signetics and General Electric (RCA and Intersil included) increased in 1986; Fairchild held spending even with 1985's results (see Table 2).

Of those companies that spent less in 1986, AMD and Thomson-Mostek had the steepest declines: 68 percent and 77 percent, respectively (see Table 2). Motorola and Texas Instruments led 1986 merchant capital spending with $250 million and $213 million, respectively.

In contrast with 1986, only three companies contacted by Dataquest indicated that they might decrease their capital spending in 1987. These three companies are Fairchild, National Semiconductor, and Harris. Each of these has recently completed major expansion of capacity.

Of those companies that will probably increase their expenditures in 1987, Thomson-Mostek and Philips-Signetics will have the largest percentage increases, reflecting their European parents' commitments to increase market share.

Advanced Micro Devices (AMD)

AMD's capital expenditures increased each year until the 1985 downturn. However, its expenditures turned down from $237 million in 1984 to $172 million in 1985. In calendar year 1986, AMD decreased its capital spending by 68 percent to approximately $55 million. We currently estimate that AMD will spend approximately $50 million to $75 million in 1987.

The focus of AMD's 1986 spending was on assembly automation equipment and on steppers. In 1986, AMD added extensive test facilities and design and process engineering facilities in both San Antonio and Austin, Texas. The company also plans to complete its Bangkok, Thailand, plastic assembly facility by early 1987.

Future fab capital spending for AMD depends in large part on how soon the company needs extra capacity. Fab 4 in Austin has been closed and may be revamped to 6-inch capacity, when that capacity is needed. Fab 10 will be closed this year and eventually refurbished, perhaps with 8-inch capability in 1988. AMD now has three lines in Austin: two 6-inch lines and one 5-inch. Fab 14 in Austin is capable of both NMOS and CMOS. Eventually, we expect to see four 6-inch, 1.5-micron or less lines at Austin.

AMD reportedly has its 6-inch bipolar line in San Antonio in production. The company also has plans, but with as yet no firm dates, to add two additional lines at San Antonio.

Analog Devices

Analog Devices' calendar year capital spending rose from $19 million in 1980 to a high of $62 million in 1985. We estimate the company's calendar year 1986 capital spending to be $37 million, down 41 percent from 1985. We believe that Analog's capital spending in 1987 will be up to approximately $40 million to $50 million.

Analog's new line in Wilmington, Massachusetts, is now making and shipping Word Slice digital signal processing products with a 1.5-micron CMOS process. At the same facility, Analog also began running products utilizing a BIMOS technology in 1986. At Wilmington, in 1987 Analog is looking forward to running a new complementary 4-inch bipolar line for high-speed pnp transistors with 4-micron geometries.

Analog's 4-inch line in Limerick, Ireland, is partially equipped and will begin production when capacity is needed. This could be in 1987.

Fairchild

Fairchild spent $135 million on property, plant, and equipment (PPE) in 1986, even with spending in 1985. In 1986, we estimate that Fairchild spent $85 million on equipment. We expect Fairchild to cut its capital spending by probably half in 1987.

Fairchild's 1986 spending was directed toward assembly and to building and equipping its Nagasaki and Wasserburg plants. Since the end of 1983, Fairchild has brought up or designed all of its fabs with the ability to do sub-2-micron CMOS processing. At the facility in Wasserburg, West Germany, Fairchild is adding to its existing assembly and test plant a wafer fab that will be in production in 1988. This plant will have a sub-2-micron, 6-inch CMOS line producing logic products in a Class 10 environment. Altogether, there will be three lines at Wasserburg, and the total facility will be 150,000 square feet, of which 25,000 square feet will be clean room. A sub-1-micron CMOS fab at this site, originally planned for 1986, will be shipping product in 1988.

The Nagasaki, Japan, facility is expected to be in production in 1987; it will eventually ship 256K SRAMs, CMOS gate arrays, and standard logic. In 1988, Fairchild plans to begin running a BIMOS line at Nagasaki.

Fairchild closed its Palo Alto, California, fab in 1986. R&D work is still performed at this facility, however. Fairchild's 32-bit MPU, the Clipper, which was originally produced at Palo Alto, is now being produced at its Portland, Maine, fab.

The company also has recently upgraded its Singapore test and assembly facility, which runs FAST (its logic family) and FACT (its new CMOS family).

General Electric

General Electric's capital spending for 1986 (including RCA and Intersil) was approximately $90 million, 11 percent higher than for 1985. All of its capital spending was directed toward equipment, with particular emphasis on 1.25-micron processing and on test equipment.

In 1986, General Electric brought into production its 1.25-micron facility in Research Triangle Park, North Carolina. Currently the production line is running 4-inch wafers, but the company plans to run 5-inch wafers eventually.

We have been unable to ascertain General Electric's 1987 plans. Our sources indicate that General Electric may be withdrawing from the merchant business and looking for a buyer of its merchant capabilities.

Harris Corporation

In 1986, Harris spent approximately $40 million, which represented 80 percent of the $50 million the company spent in 1985. We estimate that Harris will spend approximately $30 million in 1987.

The focus of Harris' spending in both 1985 and 1986 was on its CMOS class I facility, which is capable of handling 5-inch wafers. The focus of the company's 1987 capital spending will be on equipping and upgrading existing fabs, as well as on analog test equipment.

Intel

Intel's 1986 capital spending dipped 30 percent from 1985 spending to $150 million. Of this $150 million, $135 million was for equipment. We expect Intel to increase its capital spending by approximately 15 percent to $173 million in 1987.

Intel's 6-inch Fab 7 in Albuquerque, New Mexico, is now on-line. Work is proceeding on the company's 6-inch Fab 9, which is also in Albuquerque. Fab 8, which is in Jerusalem, Israel, and produces EPROMs on 6-inch wafers, is now operational.

The company's Folsom, California, facility will by completed this year. This facility will include offices, test facilities, and engineering facilities for memories and for controllers.

Intel plans to have approximately 20 percent of the capacity in the 1.0-micron range by 1986. The company also plans to double its equipment utilization in the next two years and to invest significantly in automation.

Monolithic Memories Inc. (MMI)

MMI's capital spending plans are currently estimated to be $35 million in 1986, down 29 percent from 1985. Approximately 85 percent was for equipment.

In 1984, MMI began facilitizing Fab 5 in Santa Clara. With 4-inch wafers and 2-micron geometries, this fab features advanced photolithography and implantation. Products on this line include PAL and LSI logic.

The focus of MMI's spending in 1986 was to continue to facilitate its CMOS 5-inch, 1.3-micron Santa Clara, California, fab and to begin construction of a CMOS fab in Albuquerque, New Mexico.

Motorola

Dataquest estimates that Motorola's capital spending for calendar year 1986 was down almost 25 percent, from $330 million in 1985 to $250 million in 1986. This spending level for 1986 is still significantly higher than pre-1984 levels, however. At least 90 percent of Motorola's 1986 spending was for equipment.

We currently estimate that Motorola's 1987 capital spending will increase to $270 million, exclusive of the expenditures in Izumi City, Japan, for its joint venture with Toshiba. Expenditures for this facility by both Motorola and Toshiba will total about $220 million. Production could begin at this facility as early as 1988. Plans are to begin production with 1MB DRAMs and 256K SRAMs, and then eventually to produce 4MB DRAMs. Microprocessors will also be produced at this facility, starting with 8- and 16-bit MPUs and eventually producing 32-bit MPUs.

In 1986, a large part of Motorola's spending was for the conversion of all its domestic MOS fabs to CMOS. Motorola's new fab in East Kilbride, Scotland, is expected to begin production in the second quarter of 1987. This facility, which Motorola calls "one of the finest in the world," will feature automatic wafer handling, 6-inch lines, and 1-micron geometries.

Also in 1986, Motorola expanded its back-end facilities in Guadalajara, Mexico; Korea; and Kuala Lampur. It also began building a new facility in Munich, West Germany, for final test of ASICs and digital ICs.

Future areas of focus for Motorola's capital spending could include test equipment, assembly automation, and the lowering of equipment mean-time-between failure. The company plans to continue with construction of its Munich facility and to add assembly capability both in Hong Kong and in Korea.

Motorola has moved its MOS ASIC production from Austin, Texas, to Chandler, Arizona. At Austin, the company currently has plans, but as yet no schedule, to upgrade its 4-inch lines to 6-inch. It has continued

to expand its 5-inch, 2-micron MOS facility at Aizu, Wakamatsu, Japan. At Aizu, Motorola has recently expanded its logic capabilities and added an MPU capability.

National Semiconductor

Dataquest estimates that National's calendar year 1986 capital spending will be down 36 percent to $117 million from 1985's level of $184 million. Approximately 80 percent of its 1986 capital spending was for equipment. Expansion of the facility in Salt Lake City, Utah, is now complete, and it is producing 6-inch CMOS wafers. The Arlington, Texas, fab is now in production and producing 6-inch CMOS wafers. In Israel, work is under way on a microprocessor fab.

We estimate that National's 1987 capital spending will be less than in 1986, down to approximately $100 million.

Philips-Signetics

From 1979 to 1981, Signetics' capital spending rose from $50 million to $115 million as it expanded its Orem, Utah, facility. In 1986, Signetics spent $60 million on capital spending, up 20 percent from 1985's level of $50 million. Approximately 83 percent, or $50 million, of its 1986 expenditures was for equipment.

The company's 250,000-square-foot plant in Albuquerque, New Mexico, was completed in 1984. Eventually, this will house four fab lines; one is operational now. Signetics began equipping a second MOS line this year and plans to begin production in 1987. Also in 1986, Signetics began to equip its research and development MOS/bipolar fab in Sunnyvale, California.

We expect Signetics' capital spending for 1987 to be up over 1986, to about $100 million. Most of 1987's outlay will be for expansion of the Albuquerque fab. Other areas of interest for Signetics in 1987 include small-outline and PLCC packaging, testers, and improvements at the Orem, Utah, bipolar facility.

Texas Instruments (TI)

Texas Instruments' 1985 capital spending for semiconductor PPE was $281 million, of which approximately 80 percent was for equipment. In 1986, Texas Instruments' capital spending decreased 24 percent to $213 million. Of the $213 million that TI spent in 1986, we estimate that approximately 90 percent was for equipment. In 1987, we expect the company to increase its capital spending to between $220 million and $230 million.

Texas Instruments plans to continue those key investments that it feels are necessary to maintain a flow of technologically advanced products in both Japan and Europe as well as in the United States. The company plans to eventually produce 1MB DRAMs at both its Dallas, Texas, and Miho, Japan, facilities. Both the Miho and Dallas facilities are continuing to be ramped up, and the company claims that these facilities have the most modern clean rooms in the industry (Class 1). TI is equipping its Houston, Texas, facility with advanced bipolar equipment to run its IMPACT process, which the company developed as a high-performance, low-power, and faster bipolar process featuring small geometries. TI will also be expanding its FAM (flexible assembly module) at Sherman, Texas.

Thomson-Mostek

Thomson-Mostek's capital spending was down 77 percent in 1986 from 1985. This precipitous drop is due in part to the acquisition of Mostek by Thomson. Thomson has only had Mostek since the latter part of 1985. Thomson reports that it has a firm commitment to Thomson-Mostek, however, and that Thomson-Mostek is an integral part of the company's plans to be a major worldwide semiconductor manufacturer. We believe that Thomson-Mostek's capital spending will increase in 1987 to approximately $12 million.

IS THE ROLLER COASTER RIDE OVER?

Although 1986 experienced the worst decline ever, it looks as if the downward ride is ending. Our survey results point to a modest upswing this year, and we expect 1988 to be even better, with growth in the 20 percent range. But will capital spending, which is now beginning to inch up, again come crashing down as happened in 1985 and 1986? Probably not, although of course there will be downturns.

The advent of JIT relationships with major customers will allow device manufacturers a better window on future sales, and thus on capacity needs. Additionally, manufacturers are much more cautious now than they were in 1984. Manufacturers are planning over the next five years to increase productivity, rather than capacity. Real-time process control, now possible because of advances in inspection equipment and CIM software, will cause equipment productivity to increase. (See the SEMS newsletter, "The Changing Landscape of Capital Spending," November 1986.)

Hopefully, lessons have been learned, and with new tools such as JIT and CIM, the ups and downs, although still alternatively thrilling and then chilling, will not be so wild in the near future as in the recent past.

George Burns

Dataquest

Product Offerings

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Computer Storage—Rigid Disks
Computer Storage—Flexible Disks
Computer Storage—Tape Drives
Copying and Duplicating
Display Terminal
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Electronic Publishing
Electronic Typewriter
Electronic Whiteboard
European Semiconductor*
European Telecommunications
Gallium Arsenide
Graphics
Imaging Supplies
Japanese Semiconductor*
Office Systems
Personal Computer
Personal Computer—Worldwide Shipments and Forecasts
Robotics
Semiconductor*
Semiconductor Application Markets*
Semiconductor Equipment and Materials*
Semiconductor User Information*
Software—Artificial Intelligence
Software—Personal Computer
Software—UNIX
Technical Computer Systems
Technical Computer Systems—Minisupercomputers
Telecommunications
Western European Printer

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Corporate Alliance Program
Coporate Technology Program
Financial Services Program
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Newsletters

European PC Monitor
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Focus Reports

The European PC Market 1985-1992
European PC Retail Pricing
PC Distribution in Europe
PC Software Markets in Europe
PC Local Area Networking Markets in Europe
The Education Market for PCs in Europe
Japanese Corporations in the European PC Markets
Home Markets for PCs in Europe
Integrated Office Systems—The Market and Its Requirements
European Market for Text Processing
Korean Semiconductor Industry Analysis
Diskettes—The Market and Its Requirements

Directory Products

I.C. Start-Ups—1987
SpecCheck—Competitive Copier Guide
SpecCheck—Competitive Electronic Typewriter Guide
SpecCheck—Competitive Whiteboard Guide
Who's Who in CAD/CAM 1986

Future Products

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  - PC-based Publishing
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For further information about these products, please contact your Dataquest sales representative or the Direct Marketing Group at (408) 971-9661.

October 1986

Dataquest

Conference Schedule

1987

Semiconductor Users/Semiconductor Application Markets	February 4–6	Saddlebrook Resort Tampa, Florida
Copying and Duplicating	February 23–25	San Diego Hilton Resort San Diego, California
Imaging Supplies	February 25–26	San Diego Hilton Resort San Diego, California
Electronic Printer	March 23–25	Silverado Country Club Napa, California
Imaging Supplies	March 25–26	Silverado Country Club Napa, California
Computer Storage	April 6–8	Red Lion Inn San Jose, California
Japanese Semiconductor	April 13–14	The Miyako Kyoto, Japan
Color Conference	April 24	Red Lion Inn San Jose, California
European Telecommunications	April 27–29	The Beach Plaza Hotel Monte Carlo, Monaco
CAD/CAM	May 14–15	Hyatt Regency Monterey Monterey, California
Graphics/Display Terminals	May 20–22	San Diego Hilton Resort San Diego, California
European Semiconductor	June 4–5	Palace Hotel Madrid, Spain
European Copying and Duplicating	June 25–26	The Ritz Hotel Lisbon, Portugal
Telecommunications	June 29–July 1	Silverado Country Club Napa, California
Financial Services	August 17–18	Silverado Country Club Napa, California
Western European Printer	September 9–11	Palace Hotel Madrid, Spain
Manufacturing Automation	September 14–15	San Diego Hilton Resort San Diego, California
Business/Office Systems and Software	September 21–22	Westford Regency Hotel Littleton, Massachusetts
Asian Peripherals and Office Equipment	October 5–8	Tokyo American Club Tokyo, Japan
Technical Computers	October 5–7	Hyatt Regency Monterey Monterey, California
Semiconductor	October 19–21	The Pointe Resort Phoenix, Arizona
Office Equipment Dealers	November 5–6	Hyatt Regency Monterey Monterey, California
Military IC	November 12	Hotel Meridien Newport Beach, California
Electronic Publishing	November 16–17	Stouffer Hotel Bedford, Massachusetts
Asian Information Systems	November 30–December 4	Tokyo, Japan
CAD/CAM Electronic Design Automation	December 10–11	Santa Clara Marriott Santa Clara, California

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RESEARCH NEWSLETTER

SEMS Code: 1987-1988 Newsletters, January 1987-1

SEMICON TOKYO 1986: WHAT GOES AROUND, COMES AROUND

INTRODUCTION

Each year Dataquest surveys the Semicon Equipment and Materials Expositions at San Mateo, California; Tokyo, Japan; and Zurich, Switzerland. These industry trade shows, sponsored by the Semiconductor Equipment and Materials Institute (SEMI), are yearly milestones for semiconductor equipment and materials vendors.

Last December, SEMS personnel travelled to Japan to visit Semicon Tokyo and to research the state of the equipment and materials industry. This newsletter serves as a report on that visit.

OVERVIEW

We visited a number of semiconductor manufacturing plants. Each plant looked like a ghost town compared to the activity we witnessed in 1984. Through interviews with plant personnel, we learned that each facility reported about 60 percent capacity utilization, which confirms our analysis (which comes from silicon usage) that the total capacity utilization for 1986 was 63 percent. Figure 1, capital spending as a percent of semiconductor revenue for U.S. and Japanese companies, shows quite clearly that Japanese companies "bought" the commodities market from the years 1983 to 1985. This strategy has come around to haunt these companies as the unrelenting business cycle imposes itself on the industry.

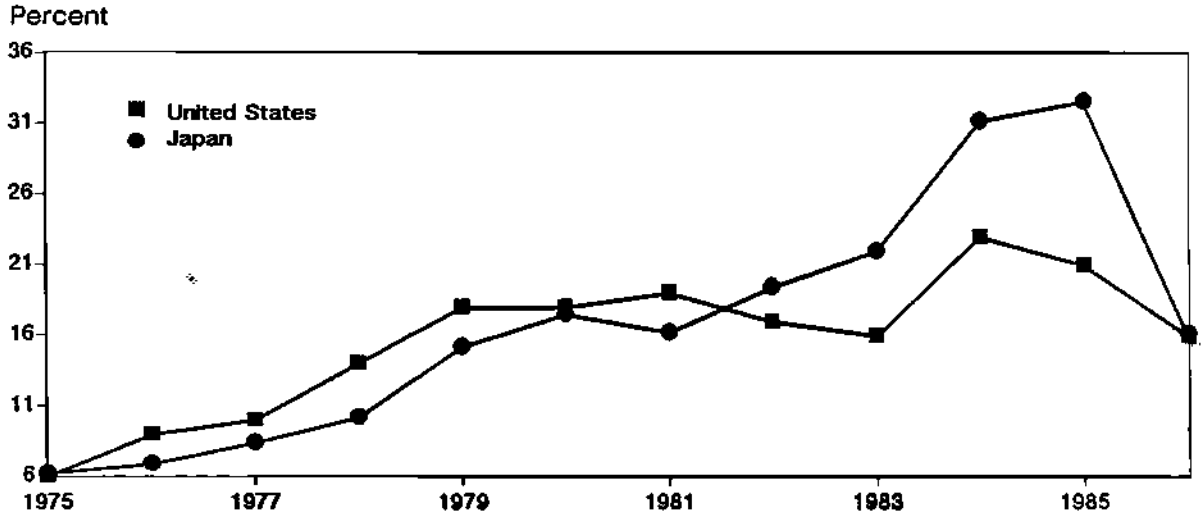
Like their counterparts in other world regions, Japanese plant personnel are far removed from the levels where trade agreements, foreign market values (FMVs), and trade sanctions are decided. Nevertheless, they are concerned about whether the United States will take further

measures to restrict the import of Japanese ICs. The only bright spot in the general atmosphere of pessimism was the robust revenue that came from shipments of application specific ICs (ASICs). Those companies that are active in the ASIC market increased both capacity utilization and revenue.

The atmosphere of pessimism affected Semicon Tokyo, where attendance was 10 percent lower than in 1985. We noticed that there were very few new products but there were many product enhancements that were designed to be user friendly and to increase the users' productivity. The general consensus at the show, derived from dozens of interviews, was that capital equipment expenditures would not increase in 1987 but would wait until the first quarter of 1988. This is consistent with Dataquest's forecast that Japanese capital spending will decrease in 1987.

Figure 1

CAPITAL SPENDING AS A PERCENT OF REVENUE
U.S. VERSUS JAPAN



Source: Dataquest
January 1987

SEMICON TOKYO

Semicon Tokyo continued to outpace Semicon West as the most attended of SEMI's expositions for the second year. This year, a record 868 worldwide corporations participated, marking continual growth in the number of exhibitors for four consecutive years. The number of visitors to the show was about 50,000, which was 10 percent lower than SEMI expected. Table 1 illustrates the history of the exhibitors' profile at the show.

Table 1

SEMICON TOKYO EXHIBITORS BY REGION OF ORIGIN

Country of Origin	1982	1983	1984	1985	1986
Japan	232	327	413	468	507
United States	204	289	288	282	291
United Kingdom	11	15	19	19	22
West Germany	12	14	20	13	14
Other	16	30	28	25	34
Total	475	675	768	807	868

Source: SEMI

A quick analysis shows that the prodigious spending by Japanese semiconductor companies, as indicated in Figure 1, seemed to benefit Japanese suppliers the most as measured by number of exhibitors. Japanese suppliers represented 49 percent of the exhibitors in 1982 but grew to 58 percent of the total in 1986. U.S. companies represented 43 percent in 1982 but fell to only 34 percent of the total in 1986. Other regional suppliers, as a group, held their own during that period at approximately 8 percent of the total. This is but another indication that the semiconductor technological base is shifting to the Pacific rim.'

A substantial portion of exhibits was dedicated to products related to magnetic disks, CDs, and LCDs, a reflection of the diversification effort against the backdrop of bearish demand in 1986 and the pessimistic market projection for 1987. Conspicuous by their absence were 200mm wafer processors. The market appears to be premature for movement into larger wafer sizes.

The most popular product categories at the show were testing and measurement (496 exhibits), wafer processing (279 exhibits), and chemicals, parts, and accessories (324 exhibits). The exhibits also included thin-membrane deposition devices and excimer lasers, as well as radiographic lithography instruments, harbingers of the next generation of LSI production technology.

WAFER FAB EQUIPMENT ANALYSIS

We found no company that was sanguine about its own sales or the market in general. Some market segments, such as ion implantation, have been devastated by the prolonged recession. In general, the new products that were introduced at Semicon West last May have not taken off; they are still waiting for the production buys that carry products from R&D sunk-costs into mature profitability. Some of these newer technologies, such as rapid thermal processing (RTP), vertical furnaces, wafer transport systems, new stepper lenses (i.e., I-line and high numerical aperture types), x-ray steppers, in-line wafer inspection systems, and new CVD systems, will have to wait at least three quarters before they see fab expansions. In Japan the waiting will be longer. This delay will put a severe strain on cash flow and will test the pocket depth of equity investors, setting back business plans and timing.

Excess Capacity

Several issues will affect the growth of equipment segments this year. It appears that semiconductor manufacturers are developing processes that will enable them to manufacture 4-Mbit DRAMs using existing optical technology with a modicum of modification. This will certainly increase return on capital in the near term, but will delay production purchases for new capacity until new products are introduced during the 4-Mbit-design-rule era.

However, there are equipment segments that do not have adequate capacity for the new generation of devices, notably deposition and particulate control. As the 1-Mbit and 4-Mbit DRAMs ramp up, these segments should do relatively well for the new products that have been recently released. As these newer equipment technologies make their way out of pilot production lines, we should see a very heated market by the end of 1987. Lagging behind CVD and particulate control in priority will be RTP and inspection.

Lithography Philosophy

We are seeing a polarization of lithography philosophy between Japan and the rest of the world. The two leading stepper manufacturers in Japan, Nikon and Canon, have shown a reluctance to develop a production, I-line lens. Canon has even publicly stated that it will not develop such a lens, but will concentrate on improving the resolution of the G-line lens and bettering the registration of the wafer alignment system. While most of the stepper manufacturers have R&D versions of I-line capability, these Japanese companies seem convinced that high numerical aperture (NA) lenses, even with their concomitant smaller depth of focus, will be the production technique for 4-Mbit DRAMs. Such a strategy implies that semiconductor manufacturers will choose planarization as a processing technique for these devices. Dataquest's research determines that the Japanese semiconductor companies are far more inclined to use this technique than their competitors in the rest of the world.

In the United States, the remaining stepper manufacturers, GCA, Perkin-Elmer, American Semiconductor Equipment Technologies (ASET), and Ultratech (a unit of General Signal), are mixed in their philosophies. GCA and ASET are moving into products based on illuminating with shorter wavelengths. GCA has introduced its I-line lens and will introduce an excimer laser source in 1987; a source that will vastly improve the illumination at this wavelength. ASET has an I-line and is concentrating on niche markets such as gallium arsenide production. Perkin-Elmer has introduced an H-line lens (390nm wavelength). Ultratech, with its 1X, catadioptic lens, will concentrate on improving the performance at its present broadband spectrum (390nm to 465nm).

In Europe, ASM Lithography (a Netherlands-based joint venture between ASM International and Philips, with sales and service in Phoenix, Arizona), has introduced an I-line capability using Zeiss lenses. ASM Lithography has sold this product into silicon markets for advanced products such as megabit memories.

In theory, I-line lenses should outperform longer-wavelength lenses, but the high quality glass that provides low absorption at this wavelength has been in short supply. The high-numerical-aperture G-line lens is a viable alternative (1) if semiconductor manufacturers are willing to compromise their processes to compensate for a smaller depth of focus, and (2) if these process compromises do not reduce the effectiveness of stepper alignment techniques. It is interesting to note that compromises, such as planarization techniques, may be required because of other considerations, which would tend to prolong the life of G-line lenses anyway.

NEW COMPETITION

One of the ways in which Japanese equipment companies have gained entry into the market place has been to spin-off from semiconductor manufacturers. Anelva, originally affiliated with NEC and Varian, and Tokuda, originally affiliated with Toshiba, are examples. When the smaller company reached adequate capacity to supply the market, the parent gave permission for it to become a merchant. This is a natural outcome of the tendency for Japanese manufacturers to engage in considerable equipment development. Two semiconductor manufacturers were conspicuous at Semicon Tokyo this year: Hitachi and Toshiba. (Incidentally, Texas Instruments and Philips also have considerable equipment development.)

Hitachi

Hitachi is one of the leading semiconductor manufacturers in the world. In its fiscal year ending March 31, 1986, Hitachi reported $29.5 billion (¥170 to the dollar), essentially unchanged from fiscal 1985. Dataquest estimates that Hitachi was second in worldwide semiconductor sales at $2.3 billion in calendar 1986, behind NEC and ahead of Toshiba. Hitachi has 164,000 employees and $30.4 billion of assets. The company reports its sales in five main categories:

- Power systems and equipment
- Consumer products
- Information and communication systems, and electronic devices
- Industrial machinery and plants
- Wire and cable, metals, chemicals, and other products

This huge company has developed more types of semiconductor equipment than any one single company, captive or merchant. The Hitachi booth at Semicon Tokyo was very popular and the company had most of its equipment exhibited. Table 2 lists Hitachi's fabrication equipment.

As can be seen by this list of 42 models, Hitachi has had considerable experience in developing equipment. The parent company's semiconductor facilities make excellent beta sites. (Note: A beta site is a manufacturing facility that will test an early version of a product to identify potential problems with the use of the product in production.)

Hitachi's equipment is manufactured in two factories, the Kasado Works and the Naka Works. The Kasado Works manufactures chemical equipment, material-handling equipment, and rolling stock. It is part of the Industrial Processes Group. The Naka Works manufactures scientific and industrial instruments. It is part of the Electronic Devices group, Instrument Division.

Hitachi estimates that its equipment production was 9 percent of the total Japanese market for fab, assembly, and test equipment. By Dataquest's market estimates for the total equipment purchases in Japan in 1986, that would equate to approximately $58 million of equipment sales for Hitachi. The distribution of this equipment is through Hitachi, Ltd. and Nissei Sangyo, a wholly owned subsidiary. Nissei Sangyo also manufacturers some of Hitachi's equipment in two factories.

Hitachi is active in the marketing of several types of fab equipment and will become more active in others. The fab equipment to watch from Hitachi in the near future is the reduction stepper, the high current ion implanter, the sputtering system, the electron beam system, and the microwave dry etcher. For instance, we expect Hitachi to introduce a Zeiss, I-line lens in 1987 capable of 0.15 micron registration (3 sigma) in 1987. We also expect that the company will actively market its microwave etcher in the United States in 1987 or in early 1988. With the right marketing and support, any of the above systems could become leading products in their respective markets.

Table 2

HITACHI'S SEMICONDUCTOR FABRICATION

Model	Type	Comments
Production Equipment		
HL-700	E-beam lithography	
LD-5010A	Reduction stepper	
FEB S-6000	CD measurement	Automatic wafer loading
FEB S-900	Super CD measurement	
PD-1000	Reticle/mask inspection	
M-206A	Microwave dry etcher	Single wafer, RIE
PS-306A	Sputtering	
TVP-60	Turbo vacuum pump	Oil free
WD-6100-P	Plasma CVD	Single wafer
IP-825A	High current implanter	
HLD-100M	Mask substrate inspection	
WF-610	Photoresist coater	Automatic
LAMU-600	CD measurement	
UG-12360-P	Gas analyzer	
PM-1400	Photoresist stripper	Wet
SEB-W100	Wafer polisher	
HILIS-200	Wafer inspection	Patterned wafers
LS-5000	Laser surface testing	
CD-10/CD-11	Wafer drying	
S-806	SEM inspection	
H-9000	Electron microscope	
IMA-3	Ion microanalyzer	

(Continued)

Table 2 (Continued)

HITACHI'S SEMICONDUCTOR FABRICATION

Model	Type	Comments
Assembly Equipment		
WB-230-TS	Wire bonder	Automated
AU-1200A	IC assembly	Multiple pin
AT-2000A	IC assembly	
AT5000	Ultrasonic detection	
EC-126MH2	Temp./humidity bath	
ES-64LTA	Heat shock test	
FH-103	FPP handler	
EA-175MT	Dynamic edging	
EA-8821HC	PLCC type 8 handler	High/low temperature
EA-61611H-FA	DIP type 16 handler	High temperature
Facilities Equipment		
KCL	Clean line	KCL type
TS-1400	Dust monitor	
DCV-1600BY	Clean draft chamber	
SC-30TT	Clean room unit	Temperature controlled
PCJ-750GII	Air shower	
PCV	Clean bench	PCV type
Clean Liner	Wafer transfer system	
Clean Carrier	Automatic guided vehicle	For clean room
DSP-15A5	Air compressor	Oil free, air cooled
CSV-5Z4	Vacuum pump	Oil free, screw type

Source: Hitachi

Toshiba Machine Co., Ltd.

Toshiba Machine is a wholly owned subsidiary of Toshiba Corporation. The corporation had sales of $14.1 billion in its fiscal year ending March 31, 1985. Dataquest estimates that the Electronic Components and Industrial Electronic Business Division had $4.7 billion in revenue in that fiscal year. Dataquest estimates that Toshiba's semiconductor revenue for calendar 1986 was $2.3 billion, which puts it third in the world, behind Hitachi and ahead of Motorola.

Toshiba Machine also has a captured user and an excellent beta site in its sister division, the electronics components division. This division has rapidly advanced the company's worldwide semiconductor market share, jumping from fifth in 1985 to third in 1986. Toshiba is the largest user of equipment from Toshiba Machine, typically using 70 percent of its production. Table 3 is a listing of the equipment that is available from Toshiba Machine.

Toshiba had exhibited a new product at Semicon Tokyo: a radiantly heated, cylinder-type reactor. Toshiba's installed base of epitaxial reactors is approximately 60 reactors, 70 percent of which are internal installations. We believe that most of the equipment it produces is used in the sister company, Toshiba Semiconductor. However, we suspect that Toshiba's manufacturing capacity may be high enough to be considered potential competitors in each of the segments the company addresses. Semiconductor-related equipment is manufactured at Toshiba's Numazu Plant along with machine tools, plastics-processing machines, precision molds, and beverage-dispensing equipment.

Table 3

TOSHIBA MACHINE'S SEMICONDUCTOR PRODUCTION EQUIPMENT

Model	Type	Comments
MCG-150S	Silicon growing reactor	100mm to 150mm capacity
DSPM-1000B	Wafer polishing system	100mm to 150mm capability
EGV-28F	Epitaxial reactor	Vertical configuration with several models, 100mm to 125mm capability
EPM-130/40P	E-beam exposure system	Masks and reticles only
APC-130R	Reticle inspection system	Compares reticles to design data
APF	Wafer track system	Scrubber, dehydrator, coater, developer, 125mm to 150mm wafers
CVA-5/6	Atmospheric CVD system	Continuous belt feed, 100mm to 150mm wafers
MTS-250	IC molding press	
EBT	E-beam tester	In-circuit inspection of electrical signals

Source: Toshiba Machine Co.

Automation

Wafer transport systems have always been a major emphasis in the automation programs of Japanese semiconductor manufacturers. In our visits to Japanese semiconductor plants, we have noted the presence of sophisticated cell-to-cell wafer transport systems, which have included both automatic guided vehicles (AGVs) as well as elevated wafer tracks running between processing bays. These cell-to-cell wafer transport systems have typically been designed in-house at a semiconductor manufacturer's plant, and either built by a sister division within the company, or the construction has been contracted to an outside engineering firm. At Semicon Tokyo this year, both Shimizu Construction Co. and Toshiba Corporation announced what Dataquest believes are the first commercially available products for wafer transport systems from Japanese companies.

Shimizu Construction has combined efforts with Shinko Electric to jointly develop CLEANWARP, an automatic wafer transport system. The CLEANWARP product includes a stocker system, an interprocess transfer system to transfer wafer cassettes between processing bays, an intraprocess transfer system that includes robotic load/unload at designated processing equipment, and a system controller to link with the shop floor's host computer. The full system can support 13 processing bays and has been designed for a class 10 (0.1 micron particle size) clean room environment.

Toshiba's product is a magnetically levitated carrier system that includes overhead traffic guideways and elevator stations for load/unload processing of wafer cassettes. The system is manufactured by Toshiba's Heavy Apparatus Division (which also builds AGVs), and is being marketed by Toshiba's Factory Automation and Industrial Electronic Components Group. The system has been designed for a class 10/100 clean room environment, and is currently being tested at Toshiba semiconductor manufacturing locations.

Both products will be available in the spring of 1987. Preliminary prices of these systems will be on the order of ¥1,000,000 per meter of transport system. At the 1986 exchange rate of 167 yen per dollar, this would correspond to approximately $6,000 per meter, or $750,000 for a 125-meter distance.

Dataquest believes that these are the first wafer transport systems to be offered by Japanese manufacturers. Several competitive products are already available from U.S. manufacturers including flexible AGVs from FMS and Veeco, and fixed wafer transport systems from Nacom, Programmation, and Shuttleworth. Both Toshiba and Shimizu are leveraging existing technology and automation know-how to penetrate an as-yet-untapped product segment within the automation products market in Japan.

SEMICONDUCTOR PROCESSING MATERIALS

Like a cascade of falling dominoes, Japanese electronic materials companies along with process equipment companies and semiconductor manufacturers, have felt the impact of the continuing semiconductor industry recession. Japanese materials companies have been affected by decreased demand for their products, downward pricing pressures from semiconductor manufacturers, and intense domestic competition for market share. In addition, the appreciation of the yen in 1986 has further reduced market opportunities and penetration strategies in markets overseas. This final portion of our newsletter focuses on the three major processing materials used in wafer fabrication--silicon, photoresist, and gases--and describes the current market conditions for these materials in Japan.

Silicon

In 1985, Japanese semiconductor manufacturers consumed 594 million square inches (MSI) of silicon, down 10 percent from 1984's consumption of 661 MSI. Dataquest believes that demand for silicon and epitaxial wafers remained essentially flat in 1986, and that only modest growth on the order of 10 percent will occur in 1987.

The silicon market in Japan is strongly dominated by the domestic merchant silicon manufacturers that had a combined market share of 97.5 percent of the $648.6 million silicon and epitaxial wafer market in 1985. The major Japanese merchant silicon companies are Shin-Etsu Handotai, Osaka Titanium Corporation, Nippon Silicon (a subsidiary of Mitsubishi Metal, Nippon Silicon is also known as Japan Silicon or JASIL), Komatsu Electronic Metals, and Toshiba Ceramics. Captive silicon production in Japan is limited to only one major semiconductor manufacturer, Hitachi, which meets 25 percent to 30 percent of its needs with internal silicon production.

There were two new entrants in the Japanese silicon market in 1986, Nittetsu Denshi (a subsidiary of Nippon Steel) and Showa Denko. Showa Denko brings 10 years of experience in compound semiconductor material manufacturing and an existing distribution network, factors that Showa Denko hopes will provide it with a competitive advantage. Nittetsu Denshi (also referred to as Nittetsu Shoji or NSC Electron) was established as a wholly owned subsidiary of Nippon Steel in June 1985. In addition to financial backing, the steelmaker can provide its new venture with a strong background in support technologies for silicon manufacturing such as crystal growth control and precision measurement. To speed its entry into the silicon market, Nippon Steel has agreed to provide Hitachi Ltd. a stable supply of silicon wafers from its new subsidiary in exchange for technological assistance. Both Showa Denko and Nittetsu Denshi started sampling 125mm polished wafers in the third quarter of 1986, and industry sources expect both companies to be significant competition in the 1987/1988 time frame.

If domestic competition were not enough, Japanese silicon companies also faced the pressures of restricted markets overseas because of the yen appreciation in 1986. Silicon wafer pricing has always varied from region to region. However, Japanese silicon companies found it difficult to compete in the U.S. and European markets in 1986 due to large differences in wafer pricing affected by exchange rate factors. For example, in 1984, the average price of a 100mm wafer in the United States was $10.50. At an exchange rate of ¥237 per US$1, a Japanese silicon company would receive ¥2,490 for a 100mm wafer. In 1986, the average selling price of a 100mm wafer in the United States came down to $10.00. However, at the 1986 exchange rate of ¥167 per US$1, a Japanese silicon company would now only receive ¥1,750 for a 100mm wafer in the United States.

Because of the high yen, Japanese silicon companies exporting silicon wafers to the United States have two options: 1) meet and maintain U.S. average selling prices for wafers and lose on margins in order to maintain U.S. market share and customer relationships, or 2) raise wafer prices in the United States to regain a given yen rate of return, and as a consequence, lose market share. Similar analysis of wafer pricing for 125mm and 150mm wafers confirms that Japanese silicon companies in 1986 were caught between the proverbial rock and a hard place, and had difficulty in competing for silicon sales overseas.

While the high yen has made silicon exports from Japan prohibitive, it has also made the acquisition of U.S. firms more attractive. In 1986, two more Japanese silicon companies have chosen to compete in the U.S. market by acquiring U.S.-based silicon manufacturing capability. Mitsubishi Metal acquired Siltec in the third quarter of 1986, and Osaka Titanium announced its plans in December to acquire U.S. Semiconductor, an epitaxial silicon wafer manufacturer.

Other Japanese companies that have established or acquired silicon facilities in the United States include silicon manufacturer Shin-Etsu Handotai (established SEH America, a wholly owned subsidiary in Vancouver, Washington) and steelmakers Kawasaki Steel and Nippon Kokan K.K. Kawasaki Steel acquired Santa Clara-based NBK Corporation in 1984, while Nippon Kokan K.K. bought Great Western's polysilicon facility in 1985. In December, Nippon Kokan K.K. announced its purchase of land in Oregon for a new 1,000 metric-ton polysilicon plant.

Photoresist

The consumption of photoresist in a given region of the world is strongly tied to the consumption of silicon wafers, so, as goes silicon, so goes photoresist in Japan. In 1986, photoresist manufacturers supplying the Japanese semiconductor industry experienced growth on the order of a few percent in photoresist (by volume) over the approximately 1,075,000 liters (284,000 gallons) of optical resist consumed in 1985. The photoresist market size in yen increased in 1986 due to the trend toward increased usage of positive resist (47 percent positive in 1986 versus 42 percent in 1985). Positive optical resist traditionally

commands a price approximately four to five times that of negative resist so as a market shifts toward increased positive resist consumption, even with little or no growth in volume, the market value increases.

However, in Japan in 1986, the increased usage of positive resist was offset by the decrease in the average selling price of positive resist; down on the order of 10 percent in yen in 1986 over 1985's price of ¥17,500 per liter. Downward pricing pressure for both positive and negative resists in Japan reflects aggressive pricing policies of the smaller resist companies attempting to wrest away a few percentage points of market share from the market leader, Tokyo Ohka Kogyo (TOK). Dataquest estimates that in 1985, TOK had approximately 65 percent to 70 percent of the optical resist market in Japan. Other major suppliers to the optical resist market in Japan include Dainippon Ink and Chemicals, Fuji-Hunt, Hoechst Japan, Japan Synthetic Rubber, Merck Japan, Shipley Far East, and Sumitomo Chemical. In its efforts to expand its presence in overseas markets, TOK recently opened a new sales office and warehouse center in Livingston, Scotland for packaging and storage of TOK resist materials for distribution to the European market.

Semiconductor Process Gases

The semiconductor process gas manufacturers in Japan have felt many of the same competitive pressures as the silicon and photoresist companies. Nitrogen, however, represents a large percentage of the market value of the bulk gases, and since the nitrogen market exhibits remarkable stability during industry recessions, bulk gas suppliers have not been affected to quite the same extent as the specialty gas companies. (The other bulk gases--argon, hydrogen, and oxygen--as well as the specialty gases, typically track with silicon and photoresist consumption.)

The semiconductor gas companies have focused on international alliances in order to survive in a global competitive market. At the Semicon Tokyo show, the booths of the Japanese semiconductor gas companies prominantly displayed the logos, literature, and equipment of their international partners. Table 4 illustrates those relationships between Japanese gas companies and their foreign partners that are based on investment position, joint ventures, or ownership.

In addition to the formal investment positions identified in Table 4, several Japanese specialty gas companies at Semicon Tokyo identified their major supplier relationships through promotional displays; examples include Seitetsu Kagaku (obtains silane from the Linde division of Union Carbide) and Tokyo Kaseihin Co., Ltd. (supplies excimer and other laser source gases from Messer Griesheim).

Table 4

SEMICONDUCTOR GAS COMPANIES AT SEMICON TOKYO

Foreign Partner		Japanese Gas Company	Nature of Relationship
Air Products	------>	Daido Sanso	Air Products has investment position in Daido Sanso
Linde	<------>	Iwatani	Linde and Iwatani have joint venture, Iwatani Industrial Gases
Matheson	<------	Nippon Sanso	Nippon Sanso has ownership position in Matheson through joint venture with Amerigas
B.O.C.	------->	Osaka Sanso	B.O.C. has investment position in Osaka Sanso
L'Air Liquide	------->	Teisan	Teisan is wholly owned by L'Air Liquide

Source: Dataquest
January 1987

These international partnerships are particularly important in the area of specialty gases, since no one specialty gas company has full manufacturing capability for all of the specialty gases. Thus, it is necessary to obtain some types of specialty gases from other gas companies. For example, Japan currently has no primary manufacturing capability for arsine gas, though industry sources indicate that Furukawa Electric may consider building such a facility in the near term. Dataquest believes that the only primary manufacturer of phosphine in Japan is Nissan Kogyo K.K., a subsidiary of Nippon Sanso, and its sales of phosphine are limited to its parent company. Therefore, the specialty gas companies in Japan are dependent on international partners to maintain the supply and flow of these vital dopant gases into Japan to support semiconductor device fabrication.

Kaz Hayashi
Robert McGeary
Peggy Marie Wood

Dataquest

Product Offerings

Industry Services

Business Computer Systems
CAD/CAM
Computer Storage—Rigid Disks
Computer Storage—Flexible Disks
Computer Storage—Tape Drives
Copying and Duplicating
Display Terminal
Electronic Printer
Electronic Publishing
Electronic Typewriter
Electronic Whiteboard
European Semiconductor*
European Telecommunications
Gallium Arsenide
Graphics
Imaging Supplies
Japanese Semiconductor*
Office Systems
Personal Computer
Personal Computer—Worldwide Shipments and Forecasts
Robotics
Semiconductor*
Semiconductor Application Markets*
Semiconductor Equipment and Materials*
Semiconductor User Information*
Software—Artificial Intelligence
Software—Personal Computer
Software—UNIX
Technical Computer Systems
Technical Computer Systems—Minisupercomputers
Telecommunications
Western European Printer

Executive and Financial Programs

Corporate Alliance Program
Coporate Technology Program
Financial Services Program
Strategic Executive Service

Newsletters

European PC Monitor
First Copy
Home Row
I.C. ASIA
I.C. USA

Focus Reports

The European PC Market 1985-1992
European PC Retail Pricing
PC Distribution in Europe
PC Software Markets in Europe
PC Local Area Networking Markets in Europe
The Education Market for PCs in Europe
Japanese Corporations in the European PC Markets
Home Markets for PCs in Europe
Integrated Office Systems—The Market and Its Requirements
European Market for Text Processing
Korean Semiconductor Industry Analysis
Diskettes—The Market and Its Requirements

Directory Products

I.C. Start-Ups—1987
SpecCheck—Competitive Copier Guide
SpecCheck—Competitive Electronic Typewriter Guide
SpecCheck—Competitive Whiteboard Guide
Who's Who in CAD/CAM 1986

Future Products

- Industry Services
  - Manufacturing Automation
  - Computer Storage—Optical
  - Computer Storage—Subsystems
- Focus Reports
  - Japanese Printer Strategy
  - Japanese Telecommunications Strategy
  - Canon CX Laser—User Survey
  - Digital Signal Processing
  - PC-based Publishing
  - Taiwan Semiconductor Industry Analysis
  - China Semiconductor Industry Analysis
  - PC Distribution Channels
- Directory Products
  - SpecCheck—Competitive Facsimile Guide
  - SpecCheck—Competitive Electronic Printer Guide

*On-line delivery option available

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Dataquest

Conference Schedule

1987

Semiconductor Users/Semiconductor Application Markets	February 4–6	Saddlebrook Resort Tampa, Florida
Copying and Duplicating	February 23–25	San Diego Hilton Resort San Diego, California
Imaging Supplies	February 25–26	San Diego Hilton Resort San Diego, California
Electronic Printer	March 23–25	Silverado Country Club Napa, California
Imaging Supplies	March 25–26	Silverado Country Club Napa, California
Computer Storage	April 6–8	Red Lion Inn San Jose, California
Japanese Semiconductor	April 13–14	The Miyako Kyoto, Japan
Color Conference	April 24	Red Lion Inn San Jose, California
European Telecommunications	April 27–29	The Beach Plaza Hotel Monte Carlo, Monaco
CAD/CAM	May 14–15	Hyatt Regency Monterey Monterey, California
Graphics/Display Terminals	May 20–22	San Diego Hilton Resort San Diego, California
European Semiconductor	June 4–5	Palace Hotel Madrid, Spain
European Copying and Duplicating	June 25–26	The Ritz Hotel Lisbon, Portugal
Telecommunications	June 29–July 1	Silverado Country Club Napa, California
Financial Services	August 17–18	Silverado Country Club Napa, California
Western European Printer	September 9–11	Palace Hotel Madrid, Spain
Manufacturing Automation	September 14–15	San Diego Hilton Resort San Diego, California
Business/Office Systems and Software	September 21–22	Westford Regency Hotel Littleton, Massachusetts
Asian Peripherals and Office Equipment	October 5–8	Tokyo American Club Tokyo, Japan
Technical Computers	October 5–7	Hyatt Regency Monterey Monterey, California
Semiconductor	October 19–21	The Pointe Resort Phoenix, Arizona
Office Equipment Dealers	November 5–6	Hyatt Regency Monterey Monterey, California
Military IC	November 12	Hotel Meridien Newport Beach, California
Electronic Publishing	November 16–17	Stouffer Hotel Bedford, Massachusetts
Asian Information Systems	November 30– December 4	Tokyo, Japan
CAD/CAM Electronic Design Automation	December 10–11	Santa Clara Marriott Santa Clara, California

February Newsletters

The following is a list of newsletters found in this section.

- Advanced Wafer Processing Technology:
  The United States Is Losing Its Lead To Japan
  1987 - #3

Dataquest
a company of
The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987-1988 Newsletters: February
1987-3

ADVANCED WAFER PROCESSING TECHNOLOGY: THE UNITED STATES IS LOSING ITS LEAD TO JAPAN

In mid-1985, the National Research Council initiated a study to evaluate the relative strengths and competitiveness of the United States versus Japan in the area of advanced wafer processing technology in the fabrication of future electronic devices. The results of the study have recently been made available in a short publication entitled "Advanced Processing of Electronic Materials in the United States and Japan" (copies available from The National Materials Advisory Board, 2101 Constitution Avenue, N.W., Washington, D.C. 20418).

Dataquest believes that the results of this study have important implications for the U.S. semiconductor device and equipment industries. This newsletter summarizes some of its key findings.

The study was conducted by the Panel on Materials Science. To assess Japanese technology, several members of the panel visited Japanese industrial and university laboratories, including laboratories at Fujitsu; Hitachi; Mitsubishi; NEC; Nippon Telegraph and Telephone (NTT); the Optoelectronics Joint Research Laboratory sponsored by MITI; Anelva Corporation; and university labs at Osaka University and Tokyo Institute of Technology. The assessment team was high-level, consisting of eight nationally recognized experts in wafer fabrication technology.

The following material, including the Executive Summary, is excerpted from the study, and does not include any Dataquest comments, except where noted. The newsletter concludes with Dataquest's comments on the general awareness of this topic in the U.S. government, with a look at what is being done about it from government and industry points of view.

EXECUTIVE SUMMARY

Future devices will have patterned structures with submicron lateral and vertical dimensions to achieve the desired speeds and packing densities, and many will require entirely new materials, materials

combinations, and device configurations. This requires the development of new processing techniques. Energetic ion, electron, plasma, and laser beam processing, as well as advanced epitaxial growth techniques, have emerged as essential technologies capable of doping, selective etching or deposition, and patterning on the submicron level. It appears that these advanced processing technologies will play a crucial role in the future development of the electronics industry.

Both the United States and Japan are actively involved in advanced processing R&D, but within the past few years the Japanese have entered a stage of vigorous activity that has accelerated their progress relative to the United States. It appears that the United States still holds the technological edge in three areas: ion implantation, thin film epitaxy, and film deposition and etching. The Japanese, however, have mounted strong programs in all three areas, and this balance could easily shift in the next few years.

There are several emerging technological areas that will be the key to future electronic and optical device development. The panel believes that the Japanese are now leading in these areas: microwave plasma processing, lithographic sources, electron and ion microbeams, laser-assisted processing, compound semiconductor processing, optoelectronic ICs, and three-dimensional device structures

The panel believes that within the past year the United States has lost control of optical lithography.

The long-term Japanese commitment to the development of these critical technologies is being carried out by at least 10 major industrial companies, whereas only a few U.S. companies maintain a comparable effort. The overall competitiveness of the United States has worsened dramatically relative to Japan in the last five years. The Japanese are now developing the science and technology needed for the future. Unless the United States responds to this challenge, this trend is likely to continue.

LIMITS AND TRENDS

Typical device dimensions in silicon VLSI circuits are now 1 to 3 microns. We can project that in 10 years these dimensions will be nearly an order of magnitude smaller. The drive to increase density by shrinking lateral dimensions necessitates concomitant reductions in vertical dimensions. For example, future circuit elements will require submicron-wide conductor lines, gate oxides of a few hundred angstroms thick, and junction depths of 1,000 angstroms or less. At these dimensions the material constraints become much more critical. Control of material fabrication and interactions on this atomic scale requires new approaches to the wafer fabrication process.

The lithography, etching, deposition, and implantation processes must be capable of performing within these dimensional constraints. In addition, the trend is to low-temperature processing to prevent unwanted motion of dopants or materials interaction in this submicron world.

A new silicon device configuration is emerging that relies heavily on surface processing techniques. Multiple layers of silicon separated by insulating layers of SiO_2 can be built, thus allowing the construction of three-dimensional circuits. Three-dimensional circuits allow increased packing densities and speed of operation and, in the long term, the possibility of quite new circuit functions.

Other semiconductor materials and device structures are becoming increasingly important such as optical devices fabricated from GaAs and other III-V compounds. These complex structures and materials require entirely new approaches to crystal growth and processing technologies such as molecular beam epitaxy (MBE) and processing in ultrahigh vacuum (UHV) environments.

WHY JAPAN?

The future lies in smaller ICs, more complex device architecture, and innovative use of new materials. In order to fabricate these structures, new surface modification techniques must be developed. This is recognized in semiconductor research laboratories in the United States and throughout the world. However, it appears that Japanese industry is ahead in making a long-term commitment to the advancement and exploitation of these techniques.

Much of Japan's systematic approach to identifying R&D priorities is accomplished under the auspices of MITI. MITI has designated 12 key 10-year R&D projects to support emerging technologies in the 1990s. The three categories for these projects are future electron devices, new materials, and biotechnology. The major emphasis in future electron devices is in superlattice devices, three-dimensional circuits, and hardened ICs.

The assessment team chose to visit Japan because of the strong programs there devoted to developing surface modification techniques for the processing of electronic materials. These R&D programs appear to be the most comprehensive and far-reaching of any country. The emphasis of this study is on the differences in the U.S. and Japanese positions in the advanced processing that is essential for the next generation of devices.

PROCESSING TECHNOLOGIES

The study discusses the key areas of wafer processing technology. Following are brief summaries of the assessment team's observations in the areas of:

- Ion implantation
- Annealing and recrystallization
- Thin film epitaxy
- Film deposition
- Etching and machining
- Lithography

Ion Implantation

Ion implantation has become one of the dominant processing techniques in wafer fabrication as current VLSI ICs may have from 6 to 12 separate implantation steps. The characteristics that have made implantation an essential process include control of lateral uniformity, control of implanted dopant profiles, accurate and reproducible dopant concentration and purity, low temperature processing, and spatial definition.

In future devices these characteristics will be of increasing importance. The need for shallow abrupt junctions requires better control of implantation at low energies. On the other hand, higher energy implanters are finding applications in the fabrication of CMOS devices to replace n- and p-well diffusions and for creating buried layers. High-energy, high-dosage implanters will find applications in implanting oxygen (or nitrogen) to form an oxide (or nitride) buried layer to form a $Si/SiO_2/Si$ heterostructure for building three-dimensional ICs.

There is more activity in the United States in the area of high-energy low-dose implants. In contrast, the Japanese have a clear commitment to the use of high-energy high-dose implanters for buried insulation layer applications.

In addition to these extensions of conventional broad-beam ion implantation, focused ion beams are being used to explore maskless implantation on advanced circuits. Other applications for focused ion beams include fine-line lithography, selective etching and sputtering. It was observed that Japanese laboratories are making significantly more use of focused ion beams in the development of advanced circuits, and that there are about 30 commercial focused ion beam systems in Japanese industrial laboratories.

Conclusion

The United States leads the world in materials and physics research related to the basic understanding of implantation processes. In the area of equipment for conventional applications, the United States still commands a lead in quantity and innovation; on the other hand, the initiative for the development of equipment for focused ion beam technologies appears to lie with Japan.

Annealing and Recrystallization

The heating of wafers in furnaces over the range of 500°C to 1,000°C has been an intrinsic part of semiconductor manufacturing for the past 30 years. However, these temperatures are not compatible with the fine dimensional control required by advanced silicon devices nor with the special constraint of chemical decomposition of compound semiconductor surfaces. To overcome these problems rapid thermal annealing (RTA) technology has been developed.

Both the United States and Japan recognize the potential of RTA and are pursuing this technology. The effort in Japan is particularly intensive. For example, at Hitachi Central Research Laboratory, RTA is being studied for the following processes: activation of implanted dopants, silicide formation, implantation annealing, formation of contacts to GaAs, oxide film growth, and densification of phosphosilicate glass. The panel knows of no comparable effort in the United States.

The area of silicon-on-insulator (SOI) research is extensive in the United States and is probably the most active area of silicon crystal growth research. The goal is to achieve device-worthy silicon over insulating layers on production wafers. The emphasis in Japan is different. The goal there is to fabricate stacked insulated layers of silicon for three-dimensional circuits. This has involved the development of scanning laser and electron beam systems for lateral epitaxy. Such systems are used to crystallize the silicon overlayers while maintaining the low substrate temperatures necessary to preserve the integrity of the underlying layers of devices.

An alternative approach to laser or electron beam thin-film melting and recrystallization is lateral epitaxial growth in the solid phase, and there are several Japanese groups pursuing this technology.

These recrystallization technologies are currently being used in the development of three-dimensional circuits, a MITI-targeted goal. Three-dimensional circuits are now being realized in numerous laboratories. Mitsubishi's goal, for example, is to fabricate a three-dimensional circuit embodying an optical sensor on the upper layer and signal processing circuits in the four lower layers.

Conclusion

While U.S. researchers are at the forefront of the science of laser annealing with regard to basic solidification and phase transformation studies, Japanese researchers are ahead in the application of laser and electron beams and solid phase epitaxy for the fabrication of SOI structures. Furthermore, their active development of rapid thermal annealing will assure Japan of a leading position in this new area of semiconductor processing.

Thin Film Epitaxy

Metallo-organic chemical vapor deposition (MOCVD) and MBE are used to grow very thin epitaxial layers with precise interface definition. These techniques have opened up entirely new crystal growth possibilities, thus allowing the fabrication of advanced devices. MBE was initiated in the United States 20 years ago, and most of the forefront research continues to orginate from here. Similarly, in the area of MOCVD epitaxial growth, U.S. researchers are pioneering the new developments.

The Japanese recognize the importance of MBE and MOCVD, and their research is accelerating rapidly in these areas, particularly with emphasis on GaAs structures. A limitation in the implementation of GaAs technology has been the production of defect-free bulk GaAs ingots; however, the Japanese are now able to grow high-quality ingots.

For silicon epitaxy, the Japanese are intent on developing low-temperature epitaxy growth processes. They are accomplishing this by the use of energetic beams to impart additional surface mobility and reactivity to obtain defect-free crystal growth at these low temperatures. Scientists at NEC, for example, are growing CVD epitaxy layers on silicon through a SiO_2 mask at temperatures of 700 to 850°C with excimer lasers or mercury-xenon lamps. There is also much emphasis in Japan on the use of microwave plasmas for film deposition and etching; researchers at NTT have demonstrated that plasma-stimulated epitaxial growth of silicon can occur at temperatures as low as 400°C.

Conclusion

MBE and MOCVD will play an increasingly important role in future devices. Both countries are devoting significant effort to these technologies, and the United States still appears to have the edge. The Japanese are giving particular emphasis to energetic beam- and plasma-stimulated low-temperature crystal growth. In addition, the Japanese success in the growth of high-quality bulk GaAs ingots puts them in the leading position in the GaAs IC area and in their efforts to develop an optoelectronics technology.

Film Deposition

At present conventional CVD processes are used throughout the industry to deposit films of good dielectric and topographical quality. However, there are significant drawbacks to the use of these processes for future submicron devices. Process temperatures are usually high, or in the case of plasma CVD, high ion energies can cause radiation damage.

The Japanese are tackling these problems by the use of microwave power for plasma generation. Researchers at NTT are using an electron cyclotron resonance (ECR) plasma technique to deposit SiO_2 and Si_3N_4 films on silicon at temperatures of less than 150°C with no radiation damage. Film quality was comparable to high-temperature CVD nitrides and thermally-grown oxides. Mitsubishi researchers view ECR deposition as the only technique capable of depositing suitable SiO_2 films for coverage of 0.5 micron devices with step patterns having aspect ratios greater than one.

The most active area of thin film conductor research in both the United States and Japan is that of silicides. Although $MoSi_2$, $TaSi_2$, and WSi_2 are currently used in devices, the best candidate appears to be $TiSi_2$, and research in this area appears to be on a par in the United States and Japan. Where Japan leads the United States is in the novel use of silicides. For example, Fujitsu has pioneered the use of silicides on GaAs where they are patterned to act as electrodes and masks for implantation. This self-aligned gate technology is now widely used in GaAs fabrication throughout the world.

There is considerable work in Japan on the use of beam techniques to enhance deposition of metals. Researchers at NEC are using lasers to deposit chromium for selective mask repair, and to direct-write tungsten lines without the aid of a mask. Researchers at Osaka University are writing 0.5 micron aluminum lines by 35 keV ion bombardment in a $(CH_3)_3Al$ atmosphere. This system can also be used to repair submicron defects in masks in a few milliseconds.

Conclusion

The United States would appear to be ahead of, or on a par with, Japan in most areas of current deposition technology. However, there are obvious differences in areas that may be crucial to future processing technology. The Japanese effort in low-pressure microwave plasma research for dielectric films surpasses anything in the United States. Likewise, the Japanese effort in the use of focused beams to enhance deposition in selective areas is also extensive and appears to be surpassing similiar research in the United States.

Etching and Machining

Currently, RF plasma reactive ion etching is widely used to etch ICs with good anisotropy. However, reactive ion etching on submicron circuits has potential radiation damage and sidewall etching problems. These inherent problems are well recognized in Japan, and Japanese researchers are addressing these problems in several innovative ways.

For example, they are widely studying the use of 2.45-GHz microwaves to excite the plasma. In this type of system, only low gas pressures (10^{-4} torr) are required so gas scattering is reduced, and hence, etch anisotropy is improved. Also, low-energy ions etch the surface instead of the higher energy bombardment required for the dense high-pressure plasmas.

At Mitsubishi, the use of microwave plasma etching is considered an essential technology for patterning 4- and 16-megabit DRAMs. Researchers are developing a system in cooperation with Tokyo Electron Ltd. to produce high currents with ion energies of less than 50 eV and with demonstrated feature sizes of 0.2 micron. Other major Japanese companies are developing their own systems, and Anelva is now marketing a commercial microwave plasma system developed with NTT.

Another approach to etching currently under investigation in both Japan and the United States is the use of excimer lasers to excite etchant gases and induce selective etching by photothermal and photochemical processes. For example, Toshiba is investigating laser-assisted dry etching in chlorine gas. Microwave excitation of the chlorine gas with organic gas additives is combined with excimer laser stimulation to enhance etch rates and improve anisotropy.

Focused ion beams can be used for direct physical sputtering or can be combined with etchant gases to achieve reactive ion etching results without the use of etch masks. Although maskless focused ion beam etching and machining is unlikely for silicon devices because of the intrinsic slowness of serial writing, it may find use in optoelectronic devices. At one Japanese research facility, focused ion beams were used for both maskless ion implantation and reactive ion etching in the fabrication of optical ICs. Research and equipment development on focused ion beams is being carried out at many Japanese laboratories.

Conclusion

The United States leads in the science and technology of conventional RF reactive ion etching, and U.S. firms dominate the manufacturing of the equipment. The Japanese are firmly convinced that new techniques must be developed for etching and patterning future devices. They have developed microwave etching processes and are well ahead in the microwave plasma area on all accounts. Laser and ion-assisted etching techniques are being researched in both Japan and the United States, but there is much greater emphasis in Japan on the use of focused ion beams.

Lithography

U.S. companies dominated the optical lithography market through 1985; however, in the past year Japanese companies have taken a major market share. (Dataquest comment: The United States actually lost its domination in 1985. Japanese stepper manufacturers had 38 percent of the worldwide stepper market in units in 1984, but rose to 51 percent in 1985, and will have about the same market share in 1986.) Optical

lithography will possibly be extended to 0.5 micron; higher resolutions can be obtained by using X-rays, electrons, or ions. However, broad-beam ion lithography is only being explored to a limited extent in the United States and Europe.

The United States has the major share of the e-beam maskmaking market, and the Japanese dominate the e-beam direct-write market; both applications utilize focused electron beams. Focused ion beams are a derivative technology, and they currently achieve resolutions below 0.1 micron. However, the problem with doing lithography with any direct writing on production wafers is that the serial writing time is too great for economical fabrication of ICs. Thus, there is great interest in the development of new lithographic techniques using X-ray or electron-beam projection techniques while using serial electron and ion beams in niche applications such as mask repair, prototyping circuits, and altering discretionary interconnections.

There was an emphasis on reducing geometries in all the Japanese companies visited by the assessment team; it was noted that the need for 0.1 micron lithography has spurred active development of e-beam, X-ray, and ion-beam lithography systems on a scale not seen elsewhere in the world. In the field of X-ray lithography it appears that the United States has lost the initiative to Japan and possibly also to Europe for the development of commercial equipment. Development of synchrotron radiation sources for IC fabrication is underway in West Germany and at several research laboratories in Japan. Many of the synchrotron designs emphasize compact systems with diameters on the order of one meter. In contrast, there is no such activity in the United States.

In Japan, as elsewhere, advanced ICs are being made with direct-write e-beam, but it was noted with surprise the frequent use of ion microbeams for experimental device fabrication. In addition to direct doping or etching enhancement, focused ion beams were used to expose resists for standard lithographic applications. Although several companies in the United States are developing focused ion beams, the efforts in Japan in the development of commercial systems appear to be more advanced.

Conclusion

The Japanese have a very substantial commitment to advancing high-resolution lithography at a very rapid pace. They are now working from a base where two companies, Nikon and Canon, command the optical lithography business. Japanese researchers at many institutions are developing increasingly efficient focused ion beam systems and high-throughput e-beam systems. In addition they are making a large commitment to X-ray lithography.

NEW STRUCTURES AND MATERIALS

Thus far, only processing techniques have been discussed. However, when new processing techniques are coupled with materials, radically new structures and devices can result. In Japan, there is an evident synergism between processing and materials, and two examples that typify the synergistic climate for research and development in this area are SOI structures and molecular beam epitaxy combined with focused ion beam implantation to fabricate heterostructure lasers. The panel knows of no equivalent work in any U.S. industrial, government, or university laboratory that demonstrates such a concentrated intellectual and financial commitment.

A short-term objective of SOI technology is the production of 4- to 6-inch wafers for one-level circuit fabrication, and it appears that the U.S. and Japanese technologies are on an equal footing. What is unique in the Japanese SOI effort, however, is the longer-term objective of constructing working circuits that employ many active layers of silicon stacked between insulation layers of SiO_2. Perhaps, the most amazing aspect of the Japanese research is the present level of effort and progress on a potential product that is clearly seen to be 7 to 10 years away from the marketplace. To the panel's knowledge, there are no comparable efforts on such long-term products being carried out in the U.S. semiconductor industry.

The goal in optoelectronics is to create a new class of devices that integrate optical and electrical components onto a single chip. A single optoelectronic IC (OEIC) could combine lasers, photodetectors, and active electronic devices such as amplifiers and modulators onto a single GaAs chip. Although such circuits would have significant advantages, they pose serious fabrication difficulties.

To circumvent some of these difficulties the Optoelectronics Joint Research Laboratory in Japan has developed an equipment design for the fabrication of optoelectronic ICs. The system consists of a series of ultra-high-vacuum chambers in which MBE is used to deposit epitaxial films and focused ion beam is used for maskless implantation. The starting material is a GaAs wafer, and a variety of complex structures required for OEICs are produced in the system without ever exposing the wafer to the atmosphere. The intent in the future is to introduce processing steps for insulator and metal film deposition and for etching, all within the same system. No such experimental facility like this exists in the United States.

REPORT SUMMARY

The importance of electronic materials to U.S. science and commerce has become immense, and the field is large and rapidly evolving. Yet, for semiconductor device production alone, the U.S. share of the world market has been decreasing. A loss of leadership in this area will have

significant consequences for the national security and economic well-being of the United States. The future of electronic materials and devices depends crucially on the advanced processing technologies discussed above. It is in this increasingly important area that the United States is losing its leadership to Japan.

The Japanese Position

It is the panel's observation that there are certain key ingredients to the Japanese success story:

- Commitment--The Japanese have made a long-term commitment to the development of new processing technologies and the application of these technologies to new semiconductor structures.

- Coupling--Within individual Japanese companies, the coupling between exploratory R&D and device fabrication is remarkably efficient. Coupling is also apparent between the equipment manufacturers and the semiconductor manufacturers.

- Commerce--Japan's semiconductor industry is made up of at least 10 entities that pursue long-range R&D on a scale matched by only a few U.S. companies. Each company covers the spectrum of product development from the laboratory to the marketplace, and each entity is a giant in its own right.

- Creativity--Creativity and innovation are central to the development of any new technology, and the Japanese are demonstrating both of these attributes in their R&D programs.

The United States And The Future

Advanced processing technologies are essential for the fabrication of future devices, which are necessary for advances in electronic technology. The United States must aggressively pursue a position of prominence in surface processing if it is to be competitive in future device production. At present the Japanese are ahead of the United States in the development and application of advanced processing technologies. At least 10 major Japanese semiconductor companies have vigorous programs on projects with an expected payoff of 7 to 10 years. There are only a few, perhaps two, U.S. firms similarly involved.

One area where the United States has significant strength is in its university programs. There are at least a half a dozen universities in the United States that have strong academic programs in electronic materials that are backed by equally strong internal research programs directly pertinent to industry needs. Some universities without strong internal programs are becoming involved in joint research ventures with government and industry. Examples of joint programs include the Microelectronics and Computer Technology Corporation, the Semiconductor Research Corporation, and the Microelectronics Center of North Carolina.

In comparison, there are perhaps half as many Japanese universities similarly involved in electronic materials research. Overall, U.S. universities fare very well in comparison; it is U.S. companies and government laboratories that appear to be lagging behind their Japanese counterparts. Government-funded research in Japan has served as a potent catalyst for long-range R&D in its industries, and has significantly influenced the worldwide competitiveness of Japanese products.

Government laboratories in the United States have the potential to provide substantial support to U.S. companies in this critical technology, but this would require a change in emphasis from current policy. In contrast to Japan, where MITI focuses government funding into areas that are commercially viable in 5 to 10 years, the majority of U.S. government funding for electronics research is directed toward national defense and aerospace programs. Since the technology requirements of these programs are very different from the needs of consumer and communications electronics, they are not designed to contribute directly to the U.S. position in these competitive areas. At present there is little emphasis in government laboratories on advanced semiconductor processing technology except in the specialized defense activities.

Government laboratories have the equipment and expertise to contribute to advanced processing science, but this area has not been identified as a prime mission. The area of most need appears to be intermediate between the truly long-range research and short-term processing R&D necessary for present device technology. To ensure success U.S. industry should be intimately involved with the government laboratories. This would allow the combined resources of government and industry to be directed toward relevant problems and to solve these problems with a schedule in mesh with industry needs.

DATAQUEST ANALYSIS

There is increasing awareness and concern among U.S. government agencies that the U.S. semiconductor industry is losing its international competitiveness, and that the decline of the U.S. semiconductor industry will erode the high technology base on which both the U.S. defense and economy rely. Further, there is concern that decline of the American semiconductor industry could leave the country dependent on foreign suppliers for ICs that are vital for national defense. Self-sufficiency in semiconductor technology and manufacturing is an absolute prerequisite for a strong domestic electronics industry and a strong national defense. Loss of leadership in electronics will result in a weakened economy and a weakened defense.

Leadership in semiconductor manufacturing requires leadership in advanced wafer fabrication technology, and as the above report from the National Research Council shows, the United States is losing its edge in this area. In addition to this report, the U.S. Department of Commerce issued, in March 1985, a 110-page study entitled "A Competitive Assessment of The U.S. Semiconductor Manufacturing Equipment Industry,"

which discusses the erosion of the U.S. leadership in this segment of the industry. Other government studies are still underway, including the National Science Foundation's study of the impact of a declining U.S. semiconductor industry on the "upstream" semiconductor equipment industry and the "downstream" electronic system industry, and the National Security Council's study on the effect of semiconductor manufacturers withdrawing from major market segments.

Perhaps the most publicized study is that of the Defense Science Board (DSB), a scientific advisory arm of the Pentagon. The DSB recently found that in the 14 critical areas necessary for a viable semiconductor industry, the United States has lost its leadership position in 7 of the areas. The 7 include: processing knowledge and skills, fabrication and testing equipment, particulate control, automation, device packaging, materials and supplies, and information management. In the remaining 7 areas, the United States was competitive in 4 and ahead in only 3.

Thus, there is a growing awareness in government circles that the United States has a problem and that something needs to be done about it. To help rectify the problem, the DSB has recently proposed a Defense Semiconductor Initiative that would provide funding of $335 million annually for five years to help support and produce next-generation DRAMs for the commercial market. Of the $335 million, $250 million would be provided to an industry consortium of U.S. IC manufacturers to fund a facility that would develop and manufacture advanced ICs, most likely 16Mb DRAMs. Part of the $250 million would be used for the investigation of new lithographic techniques, such as synchrotron X-ray sources, and other key wafer fabrication technologies.

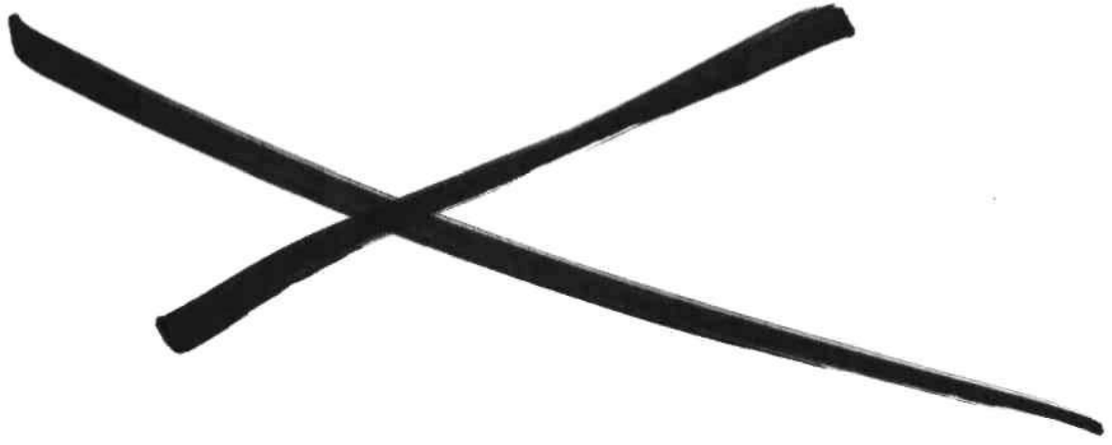
The remaining $85 million would go to government laboratories for integrated circuit R&D, to universities to expand IC manufacturing engineering education, and to a research program that would develop new IC manufacturing processes to lower costs and improve productivity. The DSB has also recommended that the White House set up a top-level government semiconductor council that would set national strategic goals in electronics.

Not only is the government calling for an industry consortium, but the semiconductor industry, in a parallel move, is also proposing its own industry consortium. The Semiconductor Industry Association (SIA), last November, formed a committee to formulate plans to establish a consortium of semiconductor manufacturers to cooperatively develop and manufacture advanced ICs, most likely this would include 4 or 16Mb DRAMS.

The consortium, called the Semiconductor Manufacturing Technology Institute (Sematech), would be funded by industry, government, and capital financing sources. The bulk of the financing is expected to come from government sources, such as the Defense Semiconductor Initiative, and the scope of Sematech will depend largely on the amount of government funding. It is expected that the consortium plans of the Defense Science Board and the SIA will be fine tuned and eventually merge, although the DSB is not committed to the SIA consortium.

One final comment: Although the Defense Semiconductor Initiative recommended $250 million for the proposed industry consortium, the Pentagon recently announced that only $50 million would be allocated in Fiscal 1988 and 1989 due to budget constraints. Most likely, the $85 million proposed funding to government laboratories and universities and for the research program will also be reduced substantially or deferred. This level of funding should be contrasted with the $101 million sought by the DOD for its ongoing VHSIC program, and the $49 million to be requested by the DOD for the development of gallium arsenide devices under the new MIMIC (Millimeter and Microwave Integrated Circuits) program. It would appear, at least from the level of funding, that the DOD is still placing a higher priority on the development of specialized military ICs than on support of the commercial semiconductor market to maintain international competitiveness. This should be contrasted with the Japanese government, which very actively supports its commercial semiconductor industry.

Joe Grenier



March Newsletters

The following is a list of newsletters found in this section:

- 1987 IEEE Solid-State Circuits Council:
  New Technology Perspective
  1987 - #4

Dataquest
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Research Newsletter

SEMS Code: Newsletters 1987-1988: March 1987-4

1987 IEEE SOLID-STATE CIRCUITS COUNCIL: NEW TECHNOLOGY PERSPECTIVE

The Institute of Electrical and Electronic Engineers (IEEE) sponsored the IEEE Solid-State Circuits Council (ISSCC) at the Hilton Hotel in New York City from February 25 through February 27. This newsletter will analyze that conference with respect to the view it may give to future fabrication trends. It is the identification of these trends that determines which equipment and materials markets will be selected over the others.

We will concentrate on the technologies to be used on next-generation manufacturing of DRAMs. However, it must be remembered that, while the papers that were presented represent the application of a particular technology, the eventual winning technique may be as yet untried. Our analysis is meant to shed light on the pros and cons of the various trends, and the statistics that we present will serve only as a snapshot of this event.

PRESENTATION OF PAPERS

There were 116 papers presented at the conference. We will analyze these papers as to regional and technical distributions.

Regional

Table 1 gives the segmentation of the papers by country in which the research was done. Each region, the United States, Japan, and Europe, is segmented by company or organization type (i.e., merchant, captive, university/institution). Sixty-three percent of the papers were from merchant semiconductor companies, 16 percent from captives, and

21 percent from universities/institutions. It is interesting to note that 90 percent of the Japanese papers were from merchants while only 44 percent of the U.S. papers and 33 percent of the European papers were from merchants. All of the Japanese companies are also captive semiconductor manufacturers that sell chips in the merchant market. Therefore, they are counted as merchants. Thus, the United States had 31 percent of its papers from captives while Europe had 20 percent and Japan had none.

It is also interesting that 47 percent of European papers came from universities while 25 percent of U.S. papers and only 10 percent of Japanese papers came from this segment. From these figures it can be argued that Japanese companies have a focus on the marketing implementation of technology because of the predominance of merchant companies as presenters. It might also appear that the technology in Japan is slightly more advanced toward implementation because of the lower percentage of universities and institutions among the presenters.

Table 1

COMPANY TYPE SEGMENTATION
(By Numbers and Percentage)

Region	Merchant		Captive		Institution		Total
United States	22	44%	16	31%	12	25%	50
Japan	46	90%	0	0	5	10%	51
Europe	5	33%	3	20%	7	47%	15
Total	73	63%	19	16%	24	21%	116

Source: ISSCC

Product Group

The breakdown of papers according to device segment is represented in Table 2. The table breaks down each region's papers into five major segments: memory, microprocessor, custom IC, analog, and other types of devices. The memory category was the largest single segment, with 25 percent of the papers. Micros and analog tied at 15 percent each. The "other" category comprised several types, including processors, logic, GaAs, and sense amps.

Table 2

SEGMENTATION BY PRODUCT GROUP
(By Numbers and Percentage)

Region	Memory		Micro		Custom		Analog		Other	
United States	7	24%	8	47%	1	20%	9	53%	25	52%
Japan	20	69	6	35	4	80	5	29	16	33
Europe	2	7	3	18	0	0	3	18	7	15
Total	29	100%	17	100%	5	100%	17	100%	48	100%

Source: ISSCC

Some interesting relationships appear from this table. First, 69 percent of the memory presentations were Japanese papers, while the United States had 24 percent and Europe had 7 percent of the memory papers. This is not surprising considering the Japanese position in DRAM markets. It would seem that they will not relinquish this position easily.

The second interesting relationship is in the microprocessor segment. The Japanese presented 35 percent of the papers, the United States presented 47 percent, and the Europeans presented 18 percent. It is clear that the United States and European companies consider micros to be a future target area within which they will be competitive against the Japanese manufacturing juggernaut. But the Japanese showing of 35 percent represents a significant effort toward competing in this area.

The third remarkable relationship is in the five semicustom array papers; four were Japanese and one was American. After observing this ratio, it would be specious to think that the burgeoning application-specific IC (ASIC) market will be a refuge for local manufacturers.

It is also interesting to note that 32 percent of the U.S. papers are in the segments that will comprise 60 percent of the total semiconductor market in 1990 (memories, micros, and ASICs). Fifty-nine percent of the Japanese papers were in the same segments. However, there were many U.S. semiconductor companies that were conspicuous by their absence. This may signify that they would rather develop their technologies quietly and not give away anything that could give Japanese and European manufacturers an advantage.

DRAM ANALYSIS

There were nine dynamic random access memory (DRAM) papers presented this year. Also, an evening panel convened to discuss issues in cell structures for future DRAM evolutions. We will discuss this session and these papers with respect to their impact on fabrication process technology.

Evening Session: DRAM Cell Structures

The moderator for the special evening session, Ashwin Shah from Texas Instruments, outlined specific issues that must impact future cell design. These issues are:

- Use of trench or stacked capacitors
- Use of planar or trench architecture
- Availability of submicron process capability
- Device isolation schemes
- Number of interconnect levels
- Scalability of cell structures
- Minimum storage capacitance
- Alternate dielectric materials
- Trade-offs in cell size, array efficiency, die size, and performance
- Power supply voltage

In his opening remarks, Mr. Shah identified the DRAM as the "technology driver" because of the need for low cost, high performance and reliability, and timely market introduction. The DRAM cell structure has evolved from a 3-transistor (3-T) cell for the 1K DRAM in the early 1970s to a 1-T cell for the 4K DRAMs. This evolution provided density improvements without great demands on the technology. With the 1-T cell, further reductions in cell size were not possible without technology enhancements in lithography, dielectrics, multilevel polysilicon, polycides, trench, and multilevel metallization.

The current generation of 256Kb and 1Mb DRAMS does not use all of the above enhancements. Each of them carries with it trade-offs in cost, performance, and manufacturability. Both planar 1-T cells with triple-level poly and those with trench and double-level poly are employed in first-generation 1Mb production DRAMs. It appears that the 1-T cell may continue into next-generation technologies, and a dozen or so 1-T structures have been proposed for the 4Mb and 16Mb DRAM.

Although the trench technology was proposed for 1Mb generation devices, they are not in widespread use. Some companies began using the trench technique but stopped before production quantities were being shipped. This is very similar to the case of CMOS on epitaxial layers. Several companies began 256K DRAMs with epi layers but abandoned epitaxy when the cost became apparent. Nevertheless, trench capacitors that use 3-D integration down into the silicon are expected to be used in the next generation of commercial devices. This technology will also compete with stacked structures that provide 3-D integration upward.

Panelists' Opinions

There was little consensus among the seven panelists. Their proposals for the best cell structures varied from planar to twin-tub capacitors. They all agreed that one of the biggest impediments to 3-D cell structures is the ability to deposit high-quality, defect-free oxide films. The following paragraphs summarize the panelists' opinions.

T. Furuyama, Toshiba - He prefers simple manufacturing processing in order to maintain high yields. A low electric field across the gate oxide is necessary to maintain reliability. He prefers a 1-T cell with CMOS compatibility, which would necessitate planarization in order to process advanced devices.

H.C. Kirsch, AT&T Bell Laboratories - He proposes the $6F^2$ Planar Cell that was proposed in the Journal of Solid State Physics in 1985 by Bell Labs. It uses a simple technology, optimized cell area, and a planar capacitor.

K. Mashiko, Mitsubishi - He prefers a 3-D structure over planar. He proposes diffusion storage, rather than storing the charge on the polysilicon, with groove trench rather than pit trench. His preference for cell structure is the Folded-Bitline Adaptive Sidewall-Isolated Capacitor (FASIC) structure for 4Mb and 16Mb DRAMs.

N. Lu, IBM - He proposes the Substrate-Plate-Trench (SPT) cell for 4Mb DRAMs and beyond. This cell uses a 1-T, 3-D structure with a trench capacitor that reaches deep into the silicon substrate. It stores the charge on polysilicon, which fills the trench and employs an epitaxial layer on a heavily doped substrate. He believes that significant efforts will be devoted to retaining the planar bulk transistor as the access device because of its high performance and long manufacturing experience.

E. Terada, NEC - He believes that further gains in density will come from a combination of Silicon-On-Insulator (SOI) and trench capacitor cells. He favors the stacked capacitor, which will become more difficult to manufacture as design rules shrink. The biggest impediment to SOI is defect-free oxides deposition.

T. Mano, NTT - He favors 3-D structures for new-generation devices. The paper presented by NTT uses Isolation Merged Vertical Capacitor cells at 0.7 microns design rules.

Discussion

The discussion that followed tried to determine the driving force for the new cell structures. The issue focused on whether to implement the lowest cost solution, which is at the end of its usefulness, or to implement an advanced design that, while not being the lowest cost, would provide the experience to capture the succeeding device markets.

An interesting repartee ensued between the panel and an engineer from Hitachi. His preference was for the SPT cell with a stacked capacitor. While he admitted that Hitachi uses a special dielectric material with a high dielectric constant (not oxide), the panel could not persuade him to divulge what it was. His opinion was that the lowest cost solution will determine the preferred cell for any given generation.

From the discussion, Dataquest perceived that, while lithography is still important, gains in film technology, both in etching and deposition, will be necessary to carry the industry into production on next-generation devices.

Megabit DRAMs

We have analyzed the nine DRAM papers as to trade-offs between device performance and manufacturability. While the number of papers by no means represents a quorum by which to judge future generations, it does shed some light on these trade-offs.

Table 3 gives a tabulation of the specifications of the various papers. It shows that the line geometries vary between 0.7 microns and 1.0 microns (if we exclude the BiCMOS chip from Hitachi).

Observing only 4Mb DRAMS, we see that the chip sizes are between 64,000 and 149,000 mil^2. Three large chips, Hitachi's double-well chip at 111,000 mil^2, Oki's at 149,000 mil^2, and Toshiba's at 111,000 mil^2 seem to sacrifice size for performance; they have fast access speeds at less than 65 nanoseconds. However, three chips, IBM's at 78,000 mil^2, Matsushita's at 67,000 mil^2, and Fujitsu's at 64,000 mil^2, match the speed performance of the larger chips at much less area. IBM's chip uses the simple SPT process and would seem to be the easiest to manufacture. IBM also lowered the power supply voltage to 3.3 volts in order to increase the reliability. The chips presented by Matsushita and Fujitsu, while having excellent size and performance characteristics, would be extremely difficult to manufacture at production quantities with existing fabrication equipment.

Table 3

DRAM SPECIFICATIONS

Company	Paper	Mbits	Cell Structure	Tech	Interconnect P #	Interconnect S #	Interconnect A #	Design Rule micron sq.	Chip Size 1,000 mils.	Cell Size sq. mic.	Access Speed nsec	Vcc volts	Oxide angstrom	Trench Depth micron
Mitsubishi	WAM 1.1	4	FACIC+FBL	CMOS	1	2	1	0.8	72	10.9	90	5.0	180	2.0
IBM	WAM 1.2	4	SPT	CMOS	1	1	1	0.8	78	11.0	65	3.3	N/A	Y
Hitachi	WAM 1.4	4	Double well	CMOS	2	N/A	2	0.8	111	14.7	65	5.0	N/A	N
Oki	WAM 1.5	4	N-Well bur stcd cap	CMOS	2	1	1	1.0	149	16.8	60	5.0	N/A	8.0
NTT	WAM 1.6	16	ISOL merg vert cap	CMOS	1	1	2	0.7	148	4.9	80	3.3	120	4.0
Hitachi	FAM 20.6	1	BiCMOS	BMOS	1	1	2	1.3	75	36.0	35	5.0	200	N
Matsushita	FAM 20.7	4	Twin tub hic trench	CMOS	2	1	1	0.8	67	8.0	60	5.0	170	4.0
Fujitsu	FAM 20.8	4	3-D stacked cap	CMOS	3	1	1	0.7	64	7.5	70	5.0	N/A	N
Toshiba	FAM 20.9	4	Twin tub trench	CMOS	2	1	1	0.9	111	14.0	60	5.0	N/A	5.5

P = Polysilicon
S = Silicide
A = Aluminum
N = No
Y = Yes
N/A = Not Available

Source: ISSCC

To illustrate the economics of the chip-size trade-off, if a 111,000 mil^2 chip and 78,000 mil^2 chip are manufactured at a defect level of 0.5 defects per $inch^2$, the larger chip would return 56 percent less revenue from each 150mm wafer. To get comparable yields, the larger chip would need a defect density of 0.35 defects per $inch^2$. This would bring the yield to 56 percent at die sort but would still only return 71 percent of the revenue of the smaller chip because there would be less chips per wafer. It would be a matter of product strategy to bet that a high-performance device could command a price premium to make up for this cost deficit.

DATAQUEST CONCLUSIONS

The world's first production 4Mb DRAM will almost certainly be IBM's SPT device as reported in the New York Times on March 8, quoted as "only months away from full-scale production." This chip will be produced at IBM/Burlington. From our analysis, this chip provided the best trade-off among manufacturability, size, and performance of the chips presented at the conference this year. The chip uses high energy implant for retrograde N-wells and employs a lightly doped epitaxial layer. The fact that IBM manufactures about 7 percent of the world's semiconductors would add some weight to these techniques.

IBM's aggressiveness indicates that it does not intend to let its manufacturing expertise go the way of U.S. semiconductor manufacturers vis-a-vis Japanese manufacturers. Because of the volume of IBM's business, its production capability will help drive American manufacturers (and all other manufacturers) to equal its cost and performance. One caveat to this analysis is that IBM does not necessarily need to be the lowest-cost manufacturer, since they have a captive buyer. (It is its culture to achieve this position.)

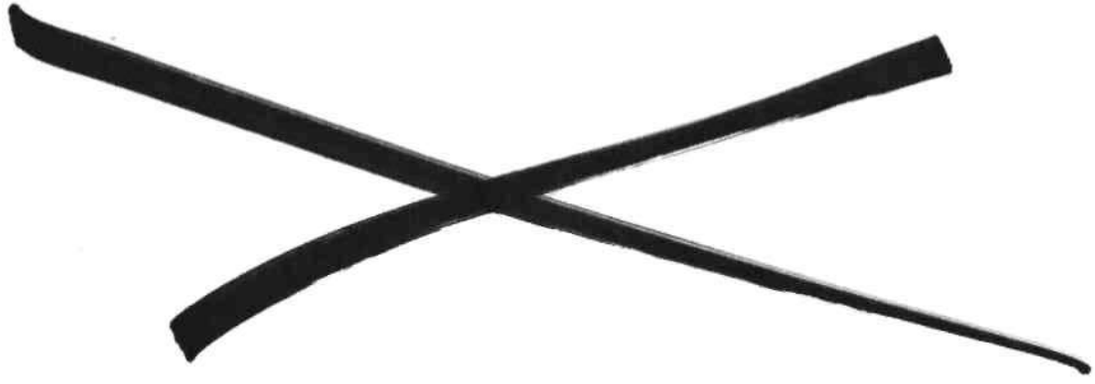
The evolution to the next devices, both 4Mb and 16Mb DRAMs, reveals important processing conclusions. The existing capacity has the lithographic capability for these new devices. For instance, the average line geometry of all the papers was 1.5 microns, 0.9 microns for DRAMs, 1.2 microns for memory, 1.5 microns for micros, and 1.5 for others. Even the DRAM devices at 0.7 microns can be done with some retrofits of existing equipment. The important processing area for future production will be thin film processes, both deposition and etching.

Film thickness reductions have not kept up with line geometry reductions. The tools are not in place to produce the thin films of these new devices in production with adequate quality, throughput, and uniformity. For instance, the average gate-oxide thickness was 281 angstroms, 148 angstroms for DRAMs, 192 angstroms for memory, 283 angstroms for micros, and 575 angstroms for others. These films will

require uniformities of less than 2 percent. Current tools average 5 percent in production. Defect densities must also be decreased, both for particulate and film defects. With these thicknesses, etch tools must be developed that maintain high throughputs while increasing the selectivity over the gate oxide.

Finally, the new processing techniques will require new capacity in high energy implantation, rapid thermal processing, and epitaxy. These new techniques cannot be developed by capital equipment companies operating in a void. Does the absence of prominent American companies signify reclusion rather than cooperation in the marketplace? We do not believe that secrecy can be a competitive advantage against superior manufacturing practices.

Robert McGeary



April Newsletters

The following is a list of newsletters found in this section:

- Coping With The Crises Of Moderate Growth
  1987-5
- Falling Dollar Overstates Lackluster Growth
  1987-6
- Surface Mount Technology: The Opportunity Is Meeting the Challenge
  1987-7
- III-V Materials--Who's On First?
  1987-8

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Research Newsletter

SEMS Code: 1987-1988 Newsletters: April 1987-8

III-V MATERIALS--WHO'S ON FIRST?

Since our August 1986 newsletter on GaAs materials, the compound semiconductor materials situation has evolved into a new game. In most high-technology business areas, innovation never ceases, leading to gyrations in the competitive lineup. The III-V materials industry is no exception.

Recent developments that we consider worth watching include:

- GaAs on Si substrates
- Progress in NDF wafer manufacture
- New entrants and start-ups
- Increases in the price of gallium in Japan
- Innovations in InP manufacture

DATAQUEST ANALYSIS

Although Sumitomo Electric in Japan is the acknowledged leader in GaAs wafers with an estimated world market share of 50 percent, the competition is heating up with major expansions under way. For this newsletter, Dataquest identified 39 companies in the Free World marketplace that are involved in compound semiconductor materials manufacturing operations. These include 18 in the United States, 2 in Canada, 11 in Japan, 3 in West Germany, 2 in the United Kingdom, 2 in France, and 1 in Sweden. As we predicted earlier, materials companies are becoming increasingly aggressive in their attempts to establish a significant presence in this market.

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 971-9000, Telex 171973

A key factor in the growth of the compound semiconductor industry is the ability to move into LSI and VLSI levels of integration. This movement is presently limited by the quality of substrate material. Although NTT announced development of a 16K SRAM in 1984, none of the device suppliers has been able to mass-produce the chip for the commercial market, at any price. Dataquest believes that recent laboratory work by Westinghouse and others on GaAs crystal growth has resolved the technical problems associated with VLSI from the standpoint of materials. Which company or companies will be first to benefit from this in the merchant market is not yet clear.

A promising alternative to GaAs substrates is the possible move to GaAs on silicon substrates, with pioneering work under way at start-up Kopin Corporation and other companies. Vertically integrated companies believed to be working in the field of GaAs on Si include AT&T Bell Laboratories, Ford, Fujitsu, GTE, HP, NEC, NTT, Oki, Texas Instruments, and Xerox. TI demonstrated a 1K SRAM implemented on a GaAs on Si substrate, in 1986. IBM's position in this area is not known, although it is believed to be heavily engaged in GaAs device and chip development, and has publicized its work on GaAs ballistic transistors. GaAs on Si, when perfected, will also significantly reduce wafer and, therefore, chip costs, bringing GaAs cost/performance at the system level much closer to that of Si ECL.

Table 1 summarizes the activities of merchant suppliers of GaAs and other compound semiconductor materials companies. It is arranged alphabetically and identifies the companies' corporate nationalities, major compound semiconductor products, methods of manufacture, wafer sizes, expansion plans, and other information that Dataquest believes is of value to its clients.

In addition to Kopin Corporation, the table shows other compound semiconductor materials start-up companies including Picogiga (France) and Preussag AG (West Germany). Dataquest expects 1987 to bring more new players to this field, as if it weren't crowded already.

Peggy Wood
Gene Miles

Table 1

WORLDWIDE III-V COMPOUND SEMICONDUCTOR MATERIALS SUPPLIERS

Company	Country	Products	Comments
Airtron	U.S.	GaAs undoped and Si-doped wafers	Growth method: LPLEC Firm is a division of Litton Industries 2", 2.5", and 3" wafers available
Bertram Labs	U.S.	GaAs wafers	Growth method: HB 2" GaAs wafers available
Boliden Finemet AB	Sweden	GaAs wafers	Growth method: HPLEC 2" and 3" GaAs wafers available
Cominco Electronic Materials	Canada	GaAs GaSb, InSb, InAs, CdTe, HgTe, and CdHgTe wafers	Growth methods: HPLEC, HB Completed expansion of LEC GaAs wafer plant in Trail, BC, Canada in 1985. Capacity 250K sq. in./year; 2", 3", and 4" wafers available
Commercial Crystal	U.S.	GaAs, GaP, InP wafers	Growth methods: LEC, HB 2" wafers available
Cryscon Technologies	U.S.	GaAs wafers	Growth method: LEC Subsidiary of Alcan Aluminum of Canada. Started shipping GaAs Q4/85. Cryscon supplies 2" and 3" GaAs wafers produced by LEC and electrodynamic gradient freeze (EFG) technique. Annual capacity approx. 2 million sq. in./year. Cryscon was for sale as of 10/22/86
Crystacomm Inc.	U.S.	InP crystals and wafers	Growth method: LEC 2.5" wafers available
Crystal Specialties	U.S.	GaAs wafers, MOULD epi reactors	CSI became subsidiary of Rollmorgen Co. in summer 1984. Wafer facility moved to Colorado Springs, CO, from Ephraim, UT, in Q3/86; reactor facility in Portland, OR
Dowa Mining	Japan	GaAs, InP wafers, poly InP, high purity In	Growth method: HB Research lab located in Akita
EMCORE	U.S.	GaAs epitaxial wafers (MOCVD epi reactors)	Start-up in New Jersey Founded in late 1984 2" and 3" wafers
Epitaxy	U.S.	Epi wafers, photodetectors	Start-up in Puncton, NJ, founded in 1984. Adding InGaAs layer onto InP wafers for photonics and other applications
Epitronics	U.S.	GaAs expitaxial wafers	MOCVD and LPE epi methods Subsidiary of Alcan Aluminum of Canada

(Continued)

Table 1 (Continued)

WORLDWIDE III-V COMPOUND SEMICONDUCTOR MATERIALS SUPPLIERS

Company	Country	Products	Comments
Furukawa Electric	Japan	GaAs, InP wafers, GaAs epi wafers	Growth method: LEC Wafers produced at Tokyo lab
GAIN Corporation	U.S.	GaAs epi wafers	Production expected in 1987
Galarix Corporation	U.S.	GaAs wafers, poly and single-crystal GaAs ingots	Growth method: HB Started in 1983 as research organization Marketing of GaAs materials primarily focused toward R&D facilities
Gallium Arsenide Substrates	U.S.	GaAs wafers, poly and single-crystal GaAs ingots	Using gradient freeze process with less than 1,000 dislocation defects/square cm Capitalized with $1 million in private funding
Hitachi Cable	Japan	GaAs, InP epi wafers, single-crystal GaAs ingots	Growth method: LEC Production of III-V materials at Takasago plant in Ibaraki. Investing ¥2 billion to expand two plants including epi plant at Kidaka
Hitachi Metals	Japan	Single-crystal GaAs ingots	Growth method: LEC Developing single-crystal undoped GaAs
ICI Wafer Technology	U.K.	GaAs, InP wafers, poly and single-crystal GaAs and InP ingots	Growth method: LEC ICI bought Cambridge Instruments' III-V operations in 1/85. 2" and 3" GaAs and 2" InP wafers available
Iwaki Handotai	Japan	GaAs wafers	Growth method: LEC 50-50 joint venture of Furukawa Mining/Shin-Etsu Handotai (SEH), founded 1982. Plant in Fukushima prefecture began 2" and 3" wafer production in June 1983. SEH began shipping 2" GaAs wafers to subsidiary, SEH America, from Iwaki Handotai June 1985. 3" wafers available in R&D quantities
Kopin Corporation	U.S.	GaAs-on-Si wafers	Start-up in Taunton, MA 3" and 4" wafers. Developing MOCVD epi process
M/A-COM Semiconductor Products	U.S.	GaAs and GaAs epi wafers	Growth method: LEC Merchant sales as well as captive consumption of GaAs wafers. Microwave Assoc. Ltd. is M/A-COM distributor in the United Kingdom
MCP Limited	U.K.	GaAs wafers	Located in Wembley, Middlesex, England

(Continued)

Table 1 (Continued)

WORLDWIDE III-V COMPOUND SEMICONDUCTOR MATERIALS SUPPLIERS

Company	Country	Products	Comments
Metal-Specialties Inc.	U.S.	GaAs, GaP, GaSb InAs, InP, InSb wafers	Growth methods: LEC, HB
Meteaux Speciaux	France	InP ingots wafers	Growth method: LEC Plant located in Moutiers, France Production expected mid-1987
Mitsubishi Metal Corporation	Japan	GaAs wafers	Growth methods: LEC, HB Wafer plant located in Omiya, Saitama prefecture. Nissho Iwai Corp. is the U.K. distributor
Mitsubishi Monsanto Kasei (MMK)	Japan	GaAs, GaP wafers	Growth methods: LEC, HB Production system for 3" NDF GaAs wafers developed at Tsukuba plant. MMK spending ¥3 billion for expansion; plans to double sales by 1989. Planned capacity is 500 wafers/month. MMK using NTT's vertical magnetic CZ method to produce 3" wafers with 10 defects/ square cm. max. MEMC to sell MMK wafers in U.S. market
Morgan Semiconductor (division of Ethyl Corp.)	U.S.	GaAs wafers; GaAs epitaxial wafers	Growth methods: LEC, HB Started sampling LP LEC 3" GaAs wafers in 1984; med. pressure LEC 3" GaAs in September 1986. Shipment of 2" and 3" GaAs epi wafers began 4Q/1986
Nippon Mining	Japan	InP wafers, poly and single-crystal InP, single-crystal GaAs and CdTe ingots	Growth method: LEC First Japanese company to grow NDF 3" InP crystal material. Nimio (Cupertino, CA) is a Nippon Mining subsidiary; purpose is to promote sales of GaAs, InP, CdTe, other III-V and II-VI materials in the U.S. market
OMVPE Technologies	Canada	GaAs epitaxial wafers	Start-up located in St. Laurent, Quebec, Canada
Picogiga	France	GaAs epi wafers	Start-up with $4 million in private funding, located in Les Ulis (Orsay). Began operation in August 1986. 2" GaAs MBE wafers
Preussag AG	West Germany	GaAs wafers	New division of Preussag, located in Gossiar, West Germany. Spending $30 million+ to develop wafer capability. Preussag is a major mining interest and supplier of Ga material.

(Continued)

Table 1 (Continued)

WORLDWIDE III-V COMPOUND SEMICONDUCTOR MATERIALS SUPPLIERS

Company	Country	Products	Comments
Raytheon	U.S.	GaAs epitaxial wafers	Growth methods: LEC, HB
Showa Denko	Japan	GaAs, GaP, InP wafers	Growth method: LEC First company in Japan to produce InP wafers by MLEC. Sampled reduced-defect GaAs wafers in summer 1985
Siemens Company, Inc. Opto Div. (Litronix)	U.S.	GaAs wafers	Growth method: HB Facility located in Cupertino, CA 1.6" to 3" wafers available
Spectrum Technology	U.S.	GaAs wafers	Growth method: HP and LP LEC Spectrum founded in 1982, acquired in Q2/1985 by NERCO Advanced Materials, Inc. (Portland, OR), a large mining interest
Spire Corporation	U.S.	GaAs epitaxial wafers and equipment	Located in Bedford, MA. MOCVD growth of III-V and II-VI compounds, including GaAs, AlGaAs, GaAsP, InP, ZnS, ZnSe on 2" and 3" substrates
Sumitomo Electric	Japan	GaAs, GaP, InP, InSb, InAs, GaSb wafers	Growth method: LEC, HB Largest III-V substrate supplier in the world; 50 percent share of GaAs market. Has capacity for 3,000 3" GaAs wafers/month. GaAs material produced in Itami City (north of Osaka), Hyogo prefecture
Sumitomo Metal Mining	Japan	GaAs, GaP and CdTe wafers	Growth method: LEC
United Epitaxial Technologies	U.S.	GaAs and AlGaAs epitaxial wafers	Start-up in Oregon; received approx. $5 million in first-round venture funding. Founded mid-1984. Working with Crystal Specialties to develop MOCVD equipment. 2" and 3" epi wafers
Wacker	West Germany	GaAs, GaP InP wafers	Growth methods: LEC, HB Shipping 2" and 3" epi wafers

Note: LPLEC = Low Pressure Liquid-Encapsulated Czochralski, HB = Horizontal Bridgeman, HPLEC = High Pressure Liquid-Encapsulated Czochralski, LEC = Liquid Encapsulated Czochralski, MOCUD = Metal Organic Chemical Vapor Desposition, LPE = Liquid Phase Epitaxy, MBE = Molecular Beam Epitaxy, MLEC = Magnetic Liquid-Encapsulated Czochralski

Source: Dataquest
April 1987

Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987-1988 Newsletters: April 1987-7

SURFACE MOUNT TECHNOLOGY: THE OPPORTUNITY IS MEETING THE CHALLENGE

OVERVIEW

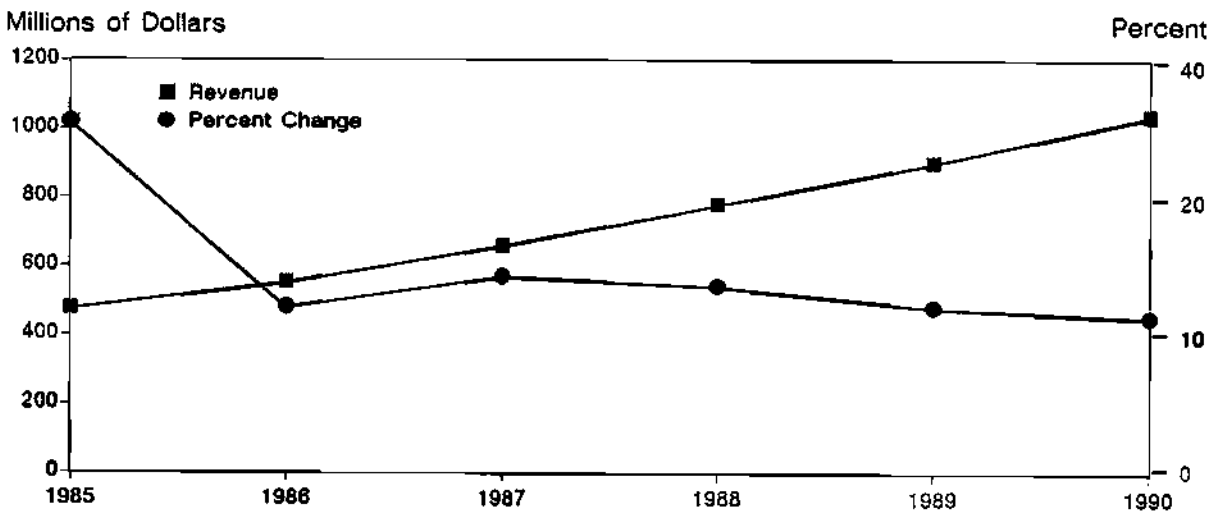
Dataquest forecasts that by 1990, the PCB CAD market will grow to more than $1 billion from $477 million in 1985. Yet the percent change in revenue from year to year is declining from 34 percent in 1985 to only 15 percent growth in 1990 (please refer to Figure 1 and Table 1). How can vendors grow amid such change?

Dataquest believes that surface-mount technology (SMT) represents a significant opportunity for vendors looking to grow their businesses in the PCB CAD market. We recently completed a survey focusing specifically on the needs of end users implementing SMT on CAD systems. The survey has yielded information and analysis regarding this design technology. In addition to reviewing the survey results and six months of focus research, this newsletter discusses the following issues:

- Technology differences between traditional, through-hole design methodologies (THT) and SMT
- End-user attitudes that directly impact their impressions of currently available CAD systems for SMT
- What vendors can do to meet the challenges SMT offers

Figure 1

PCB CAD REVENUE FORECAST
(Percent Change)



Source: Dataquest
April 1987

Table 1

PCB CAD MARKET FORECAST

	1985	1986	1987	1988	1989	1990
Revenue	477	552	659	778	902	1,038
Percent Change	34%	16%	19%	18%	16%	15%

Source: Dataquest
February 1987

SMT--What is it?

Before taking an in-depth look at survey results we offer a brief history and definition of surface-mount design methodologies.

SMT was first used in the United States in the early 1960s by the military because it met their requirements for space savings and high reliability. Surface-mount technology was available for commercial use in the United States in the 1970s. Today, SMT is used most often in the automotive, computer, and consumer electronics industries as well as aerospace.

Dataquest defines SMT CAD as the laying out of printed circuit boards (PCBs) with chips mounted to the surface of the board. The differences between through-hole technology and SMT that affect CAD systems include device footprints, packaging, and access to internal layers of the board.

How is it Different?

When designers lay out PCBs with through-hole devices, footprints (the graphic shape of a device) for components consist of round pads that go through all layers of the board. In SMT, footprints are made up of rectangular pads that reside on the external layers of the board only (please refer to Figure 2).

Looking further into the differences among THT and SMT devices, there are standards for through-hole device packages (i.e., the same-shaped device is available from a variety of vendors), while there are no such standards for SMT devices. Although there are several organizational efforts to standardize SMT device packages, today's users contend with the confusion caused by the same technology or device being available in too many packages.

The variation in packages causes designers confusion because they must create the footprints and physical library for each SMT device. Before they begin the physical layout, users need to know which manufacturer's components will be used so that the footprint graphic will match the actual device.

Another difference between these technologies is that through-hole devices use vias that go through all layers of the board, whereas in surface mounting, designers use blind and/or buried vias to access the internal layers of the board (see Figure 3).

Figure 2

DEVICE FOOTPRINTS

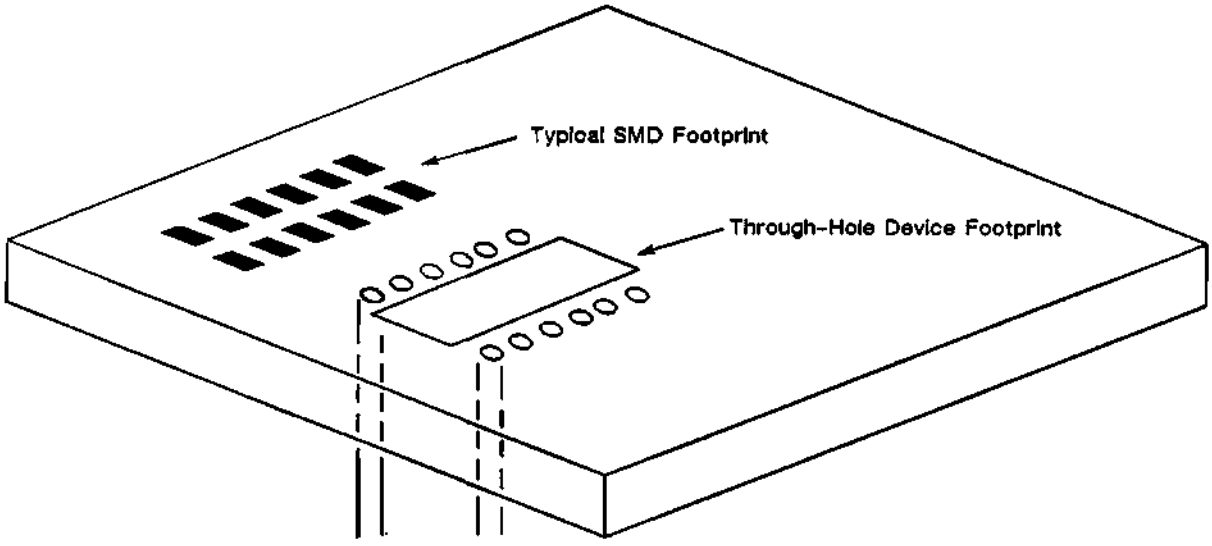
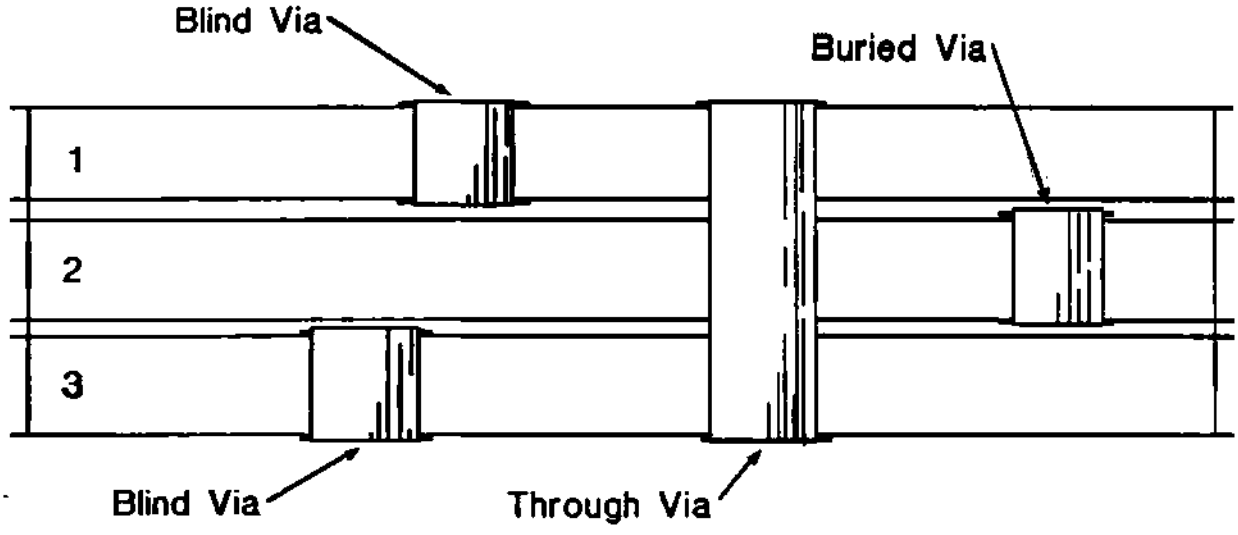


Figure 3

VIAS



Source: Nugrafix Group
Design Guideline Book

THE SURVEY

Demographics

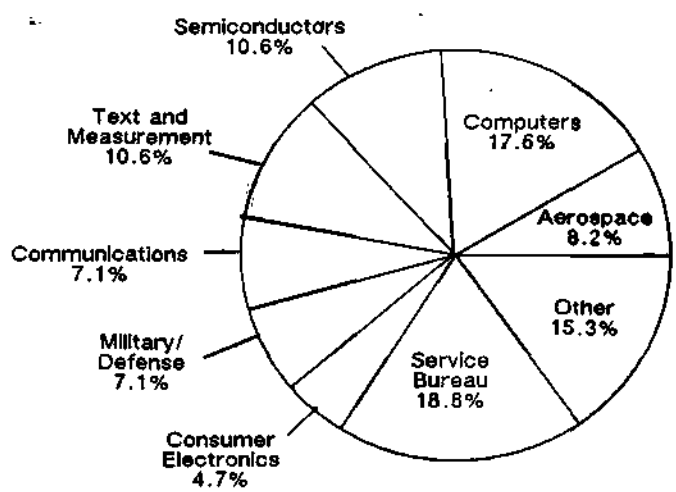
The survey sample consisted of 100 PCB CAD end users. Our selection criterion was based on whether the users were using their CAD systems for PCB layout rather than whether they were using SMT or not.

Nineteen percent of the responses came from service bureaus and another 18 percent from computer companies. Please refer to Figure 4 for further details on the industries of the respondents.

Thirty-three percent of the respondents indicated that they have been using SMT for one year or less. However, the bulk of the respondents, 47 percent, responded that they have been using surface-mount technology for two to three years. Approximately 20 percent have been using SMT for more than three years. Less than 1 percent indicated that they do not use SMT and have no plans to do so in 1987.

Figure 4

RESPONDENTS BY END-USER INDUSTRY

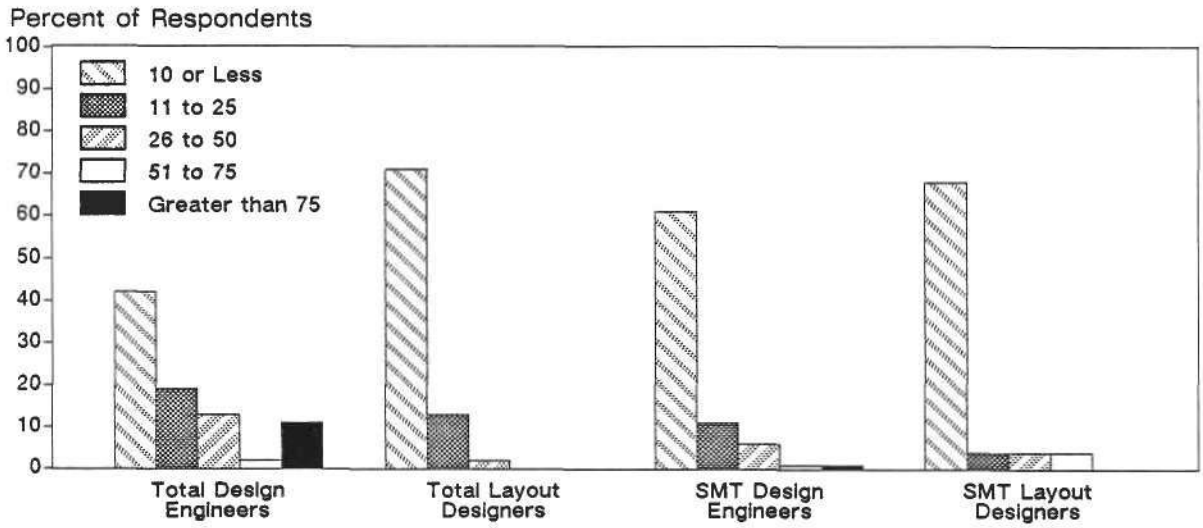


Source: Dataquest
April 1987

Most responding organizations had a total design engineering staff of 10 people or less. Sixty-one percent responded that these engineers are doing surface-mount design. Similarly, total layout designers numbered 10 or less for the majority of respondents, with 68 percent indicating that 1 to 10 designers are designing with surface-mount technology (please see Figure 5).

Figure 5

NUMBER OF ENGINEERS AND DESIGNERS



Source: Dataquest
April 1987

How is SMT Being Used?

In examining the prevalence of SMT design in proportion to traditional through-hole technology (THT), we looked at this issue from several angles: Total annual design starts (see Figure 6); which of those use SMT (see Figure 7); how SMT is implemented (see Figure 8); the number of components and the number of layers per design (see Figures 9 and 10).

Results indicate that implementation of surface-mount technology on CAD systems is still relatively new and definitely not widespread. Why are users converting to SMT? Figure 11 shows the top five reasons respondents have chosen to use surface-mount technology over through-hole design methods.

In spite of the sparsity of SMT usage, there is a perception, particularly among responding service bureaus, that users must support SMT to stay in business because their customers demand it and their competition supports it.

Figure 12 shows the layout phase of the design cycle as a percent of the total design time, comparing through-hole technology to SMT. In our focus research, end users indicated that one of the benefits of using SMT was that they could get their products designed and manufactured faster. Yet, the results of our survey show that there is little or no time saved by choosing surface-mount technology instead of THT. In researching this issue further, we learned that the time savings involved in SMT comes from the manufacturing process, where SMDs are more suited to automated manufacturing processes.

Figure 6

TOTAL ANNUAL PCB DESIGN STARTS

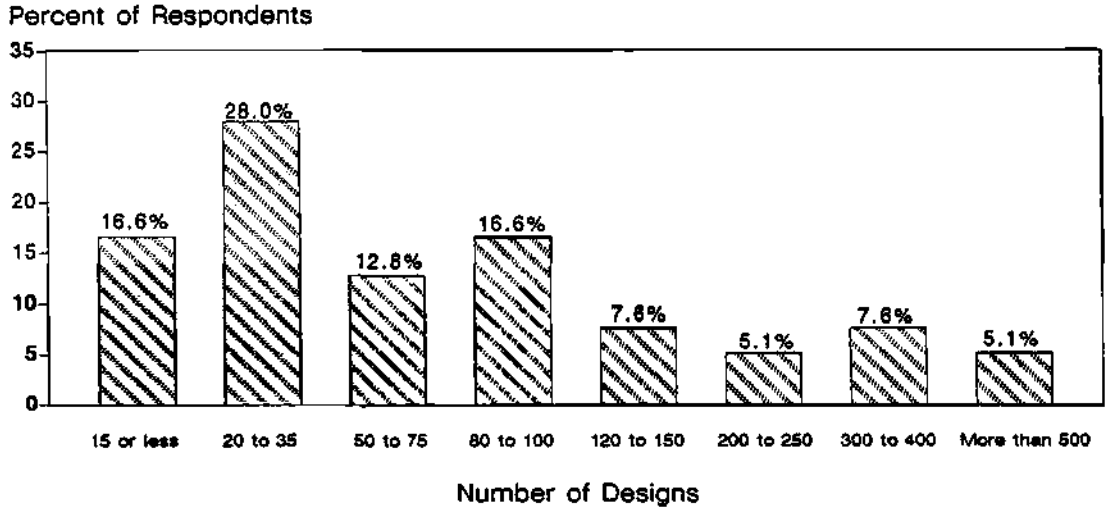
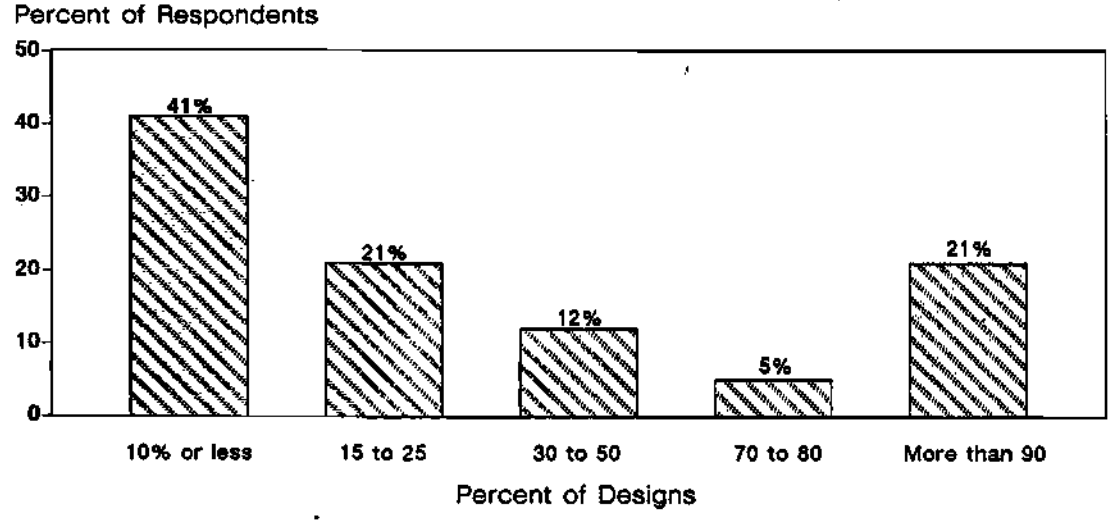


Figure 7

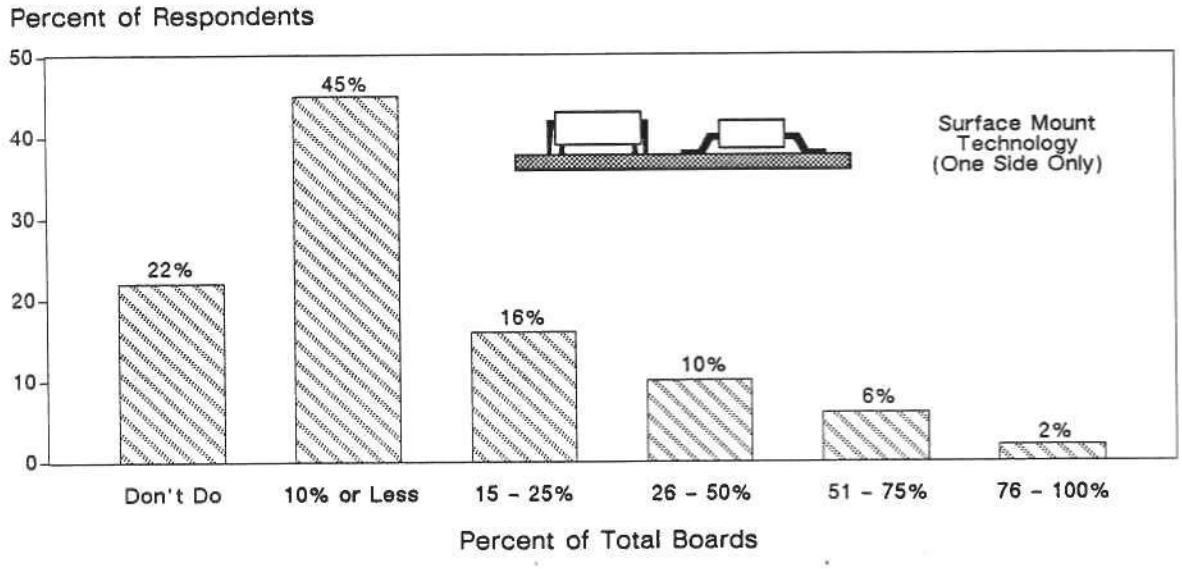
DESIGNS WITH SMT

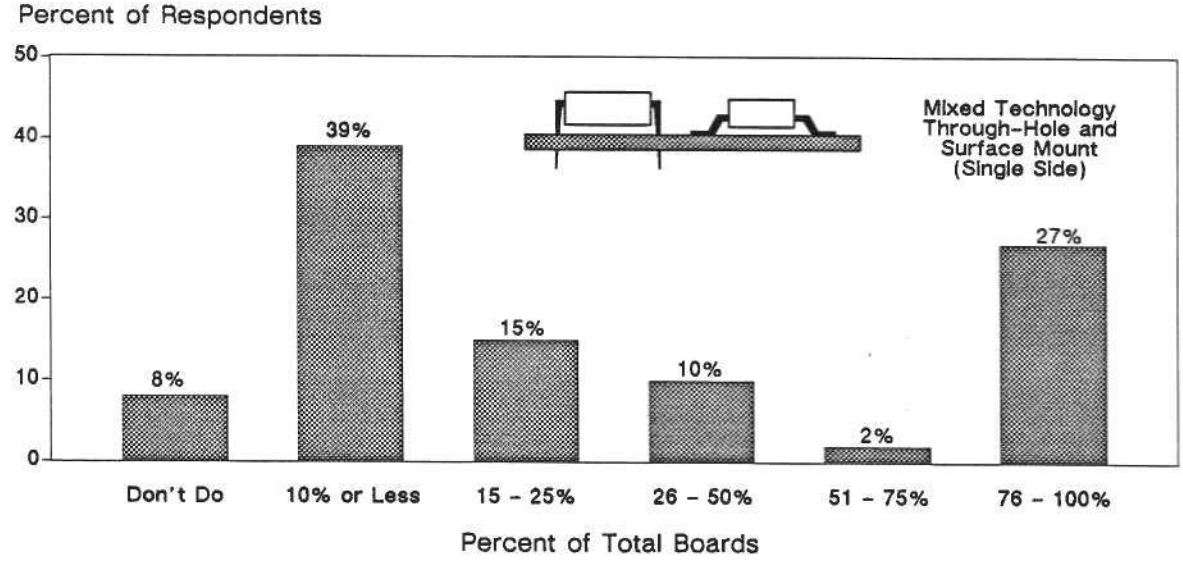


Source: Dataquest
April 1987

Figure 8

DISTRIBUTION OF DESIGNS
BY TECHNOLOGY IMPLEMENTATION

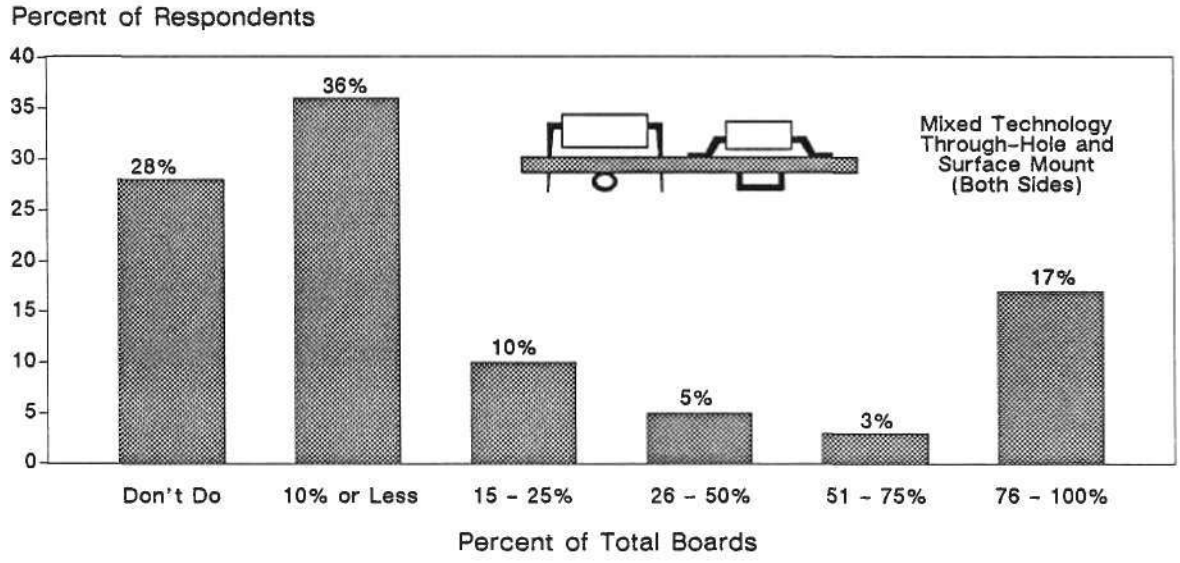


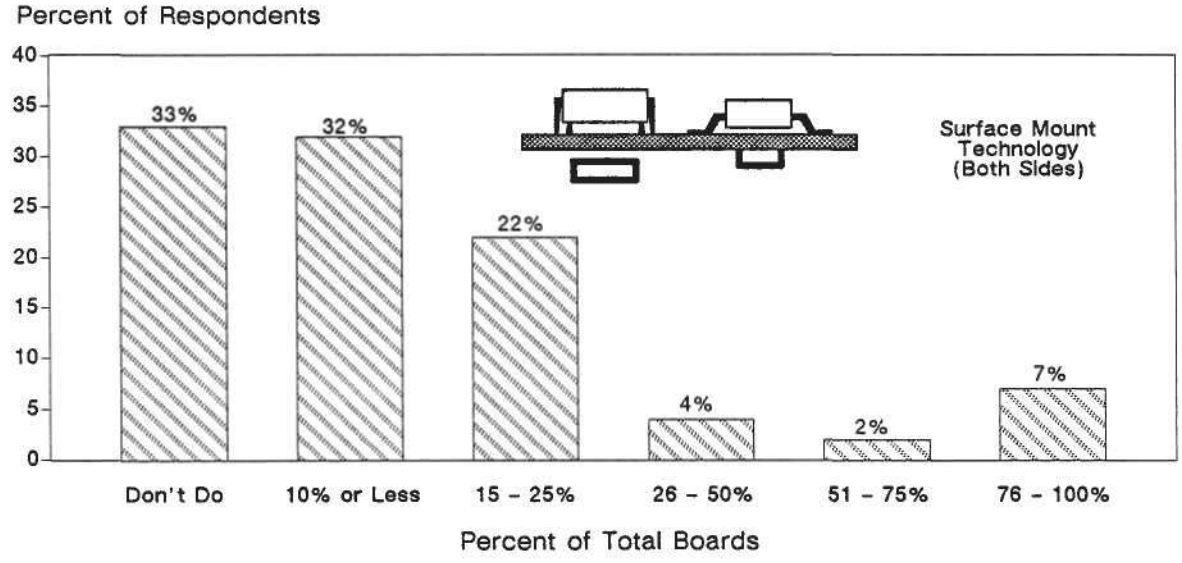


Continued

Figure 8 (Continued)

DISTRIBUTION OF DESIGNS BY TECHNOLOGY IMPLEMENTATION

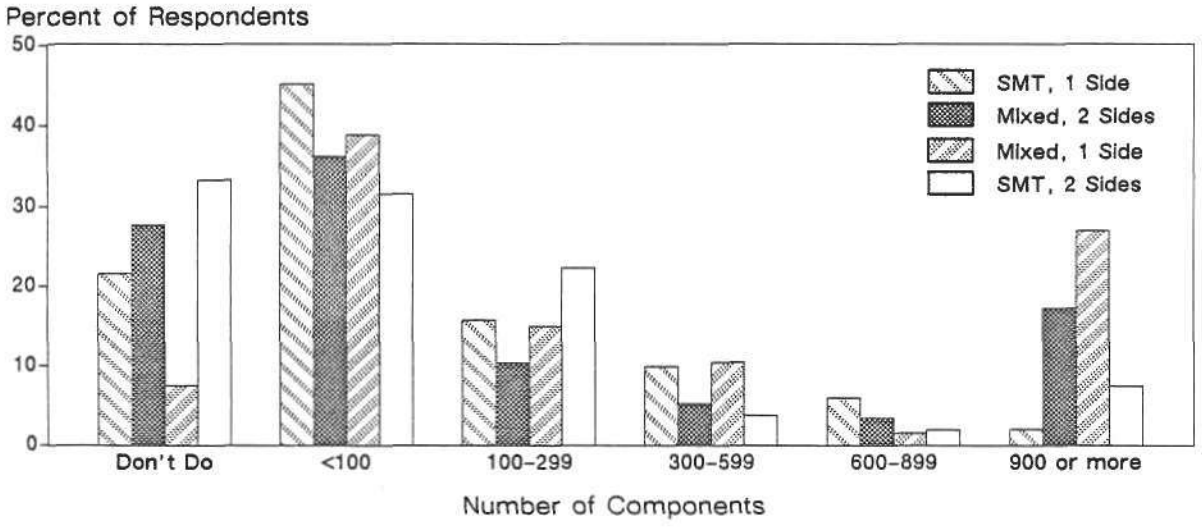




Source: Dataquest
April 1987

Figure 9

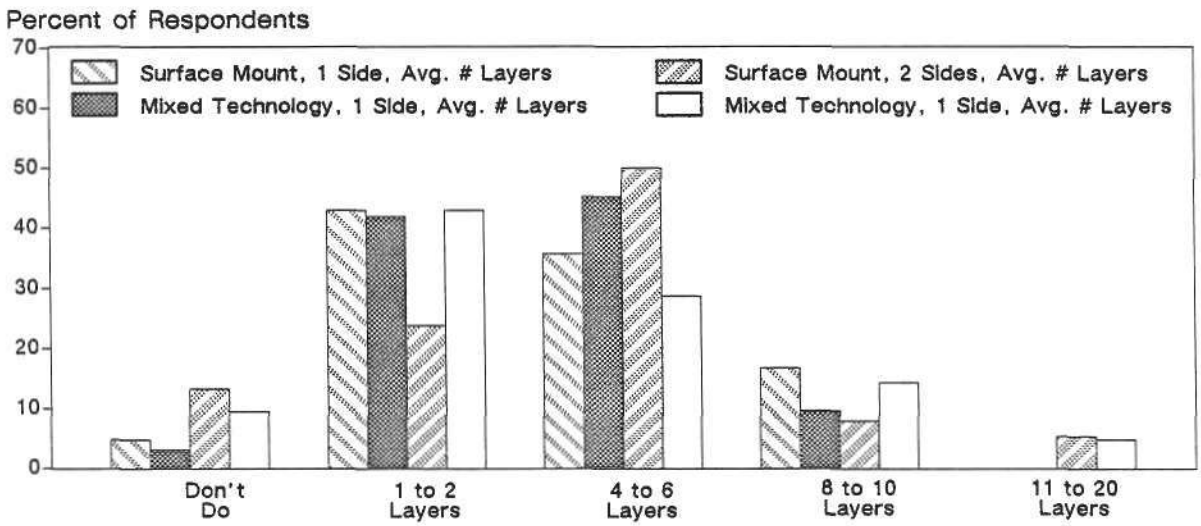
AVERAGE NUMBER OF COMPONENTS BY BOARD TYPE



Source: Dataquest
April 1987

Figure 10

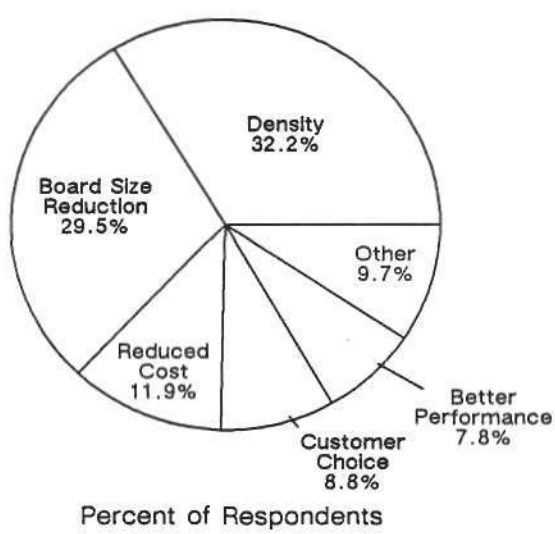
AVERAGE NUMBER OF LAYERS BY BOARD TYPE



Source: Dataquest
April 1987

Figure 11

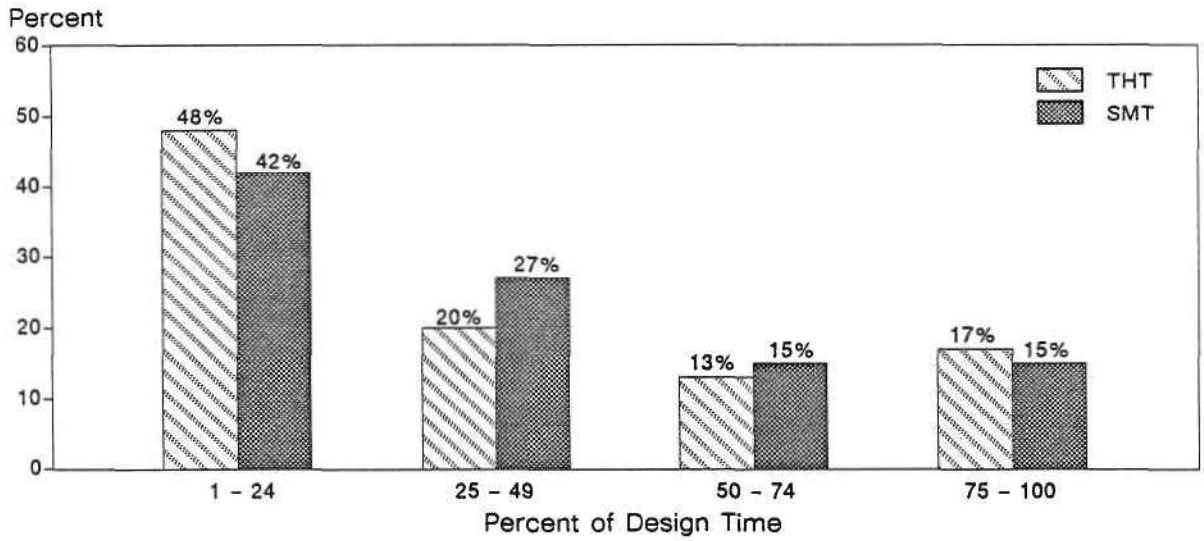
REASONS FOR USING SMT



Source: Dataquest
April 1987

Figure 12

LAYOUT AS A PERCENT OF TOTAL DESIGN TIME



Source: Dataquest
April 1987

SMT and CAD

What Do End Users Think?

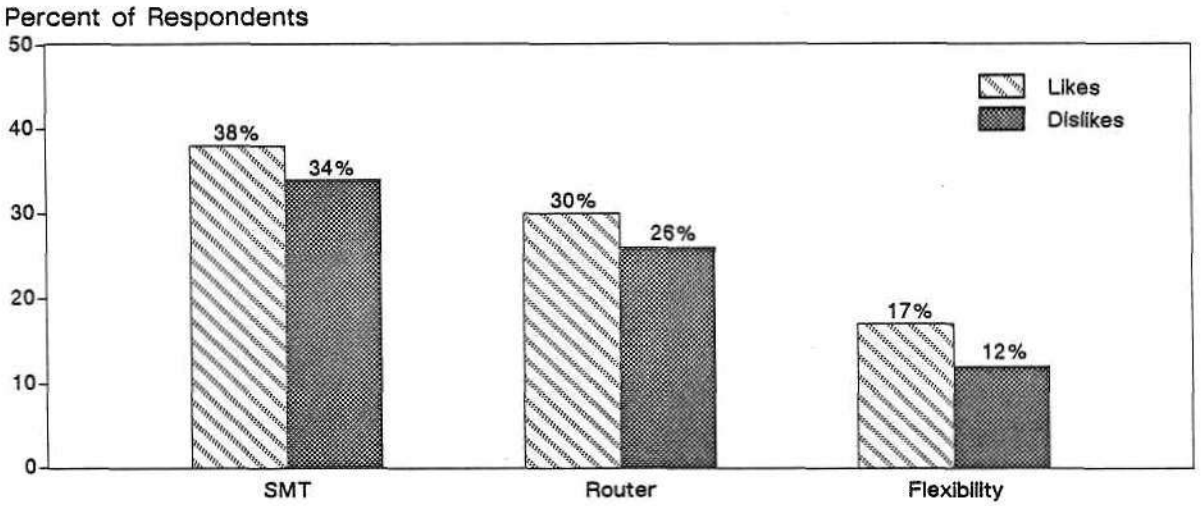
The attitude of most end users is less than optimistic regarding the currently available CAD tools. They feel that although CAD vendors have made a good start, they have a long way to go in terms of adequately supporting SMT. Other end users stated that they had been sold tricks and workarounds as true design solutions. Overall, less than 10 percent of the respondents were satisfied with the way their CAD systems support SMT.

As Figure 13 shows, the likes and dislikes of the end users closely parallel each other. Closer inspection of the data revealed no technological reasons, thus leaving us with one conclusion: The likes and dislikes cited are vendor-specific.

Ranking specific SMT support functions in order of importance, definition of pad geometries topped the list, followed by multilayer routing, off-grid design, and auto-routing of two-sided boards. End users are saying that, in order to support these important SMT functions, PCB CAD systems must be flexible and interactive enough to accommodate SMT as well as THT features.

Figure 13

END-USER LIKES AND DISLIKES



Source: Dataquest
April 1987

Users are also saying that they view SMT support as a PCB CAD system feature that must be capable of integration into users' particular design environments. Because SMT is highly process-dependent, users need to interface easily with manufacturing to ensure the manufacturability of the design.

Flexibility and integration are the two most important buying criteria for future SMT CAD purchases cited by respondents.

What Are the Challenges of SMT?

Earlier, we referred to several characteristics of SMT that affect CAD systems that support through-hole technology:

- Footprints
- The lack of standards
- Access to internal layers of the board

It is the shape of SMT device footprints as well as the fact that they reside only on the surface of the board that affects PCB CAD systems. Most systems are set up to acknowledge the footprints of through-hole devices and are not surface-intelligent.

The lack of standard geometries for the same device functionality was cited by respondents as the major drawback in converting designs to SMT. The lack of standards for SMD has created a need for a high degree of flexibility and interactivity in PCB CAD systems.

Because most PCB CAD systems are not surface-intelligent, users have to trick the system into believing that it is routing a through-hole device. To accomplish this, designers place stringers (round pads) at the end of each rectangular pad so that the system thinks it is routing a component whose leads run through all layers of the board. Although this workaround does route the board, it does not provide a long-term design solution.

How Big is the Market?

End users are budgeting for design solutions that support SMT. Nearly 60 percent of the respondents replied that they have budgeted up to $100,000 for SMT CAD tools in 1987. The highest figure budgeted for SMT CAD expenditures in 1987 was just over $1 million, cited by nearly 10 percent of the respondents.

To quantify and qualify the SMT opportunity, we based the forecast in Figure 14 on a combination of factors:

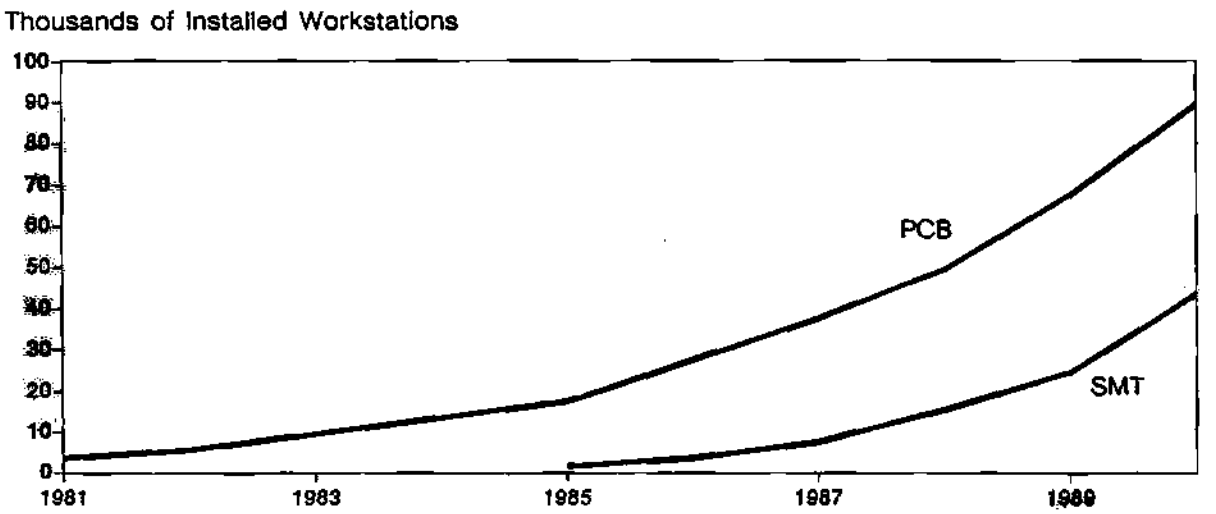
- Dataquest forecast data base, which consists of four years of research on more than 140 companies
- Data from another ECAD end-user survey, indicating number of designs and engineers
- The Dataquest Semiconductor Industry Service's forecast for SMDs that approximately 16 billion units will be shipped in 1990
- End-users' forecast for 1987, where more than 61 percent indicated that they will use SMT in 15 to 25 percent of their designs

As Figure 14 shows, Dataquest estimated that in 1985, there were more than 17,000 workstations in the installed base for PCB CAD. Of those, we estimate that approximately 2,000 supported SMT. We forecast that by 1990 the installed base of workstations used for PCB applications will be more than 90,000 units, more than half of which will support SMT.

In compiling our forecast, we considered SMT to be a function of a PCB CAD system, not a turnkey product offering. Therefore, we believe that a number of software licenses may be sold as repeat business to a vendor's installed base as well as to new customers.

Figure 14

PCB WORKSTATION INSTALLED BASE
WITH SMT CAPABILITY



Source: Dataquest
April 1987

DATAQUEST CONCLUSIONS

We believe that SMT is here to stay because end users need reduced board size with increased density, more reliable end products, and faster and less expensive manufacturing processes to keep up with their worldwide competition.

Dataquest believes that SMT support tools will be marketed as features of a CAD system, not standalone turnkey products. As such, meeting the technological differences with true design solutions is the challenge for CAD vendors in this market.

To recapitulate, the likes and dislikes of responding end users are vendor-specific. We believe that in addition to watching the competition, vendors have to overcome the negative attitudes of the end users by demonstrating that they understand the nature of their customers' problems.

Dataquest believes that the successful CAD vendors will be those who work closely with their customers to provide the needed solutions. To meet the opportunity SMT offers, vendors need to project that their products are what the end user wants: A means to an end--a quick turnaround on a manufacturable design.

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Peggy Wood
Kelly D. Leininger

Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987-1988 Newsletters: April 1987-6

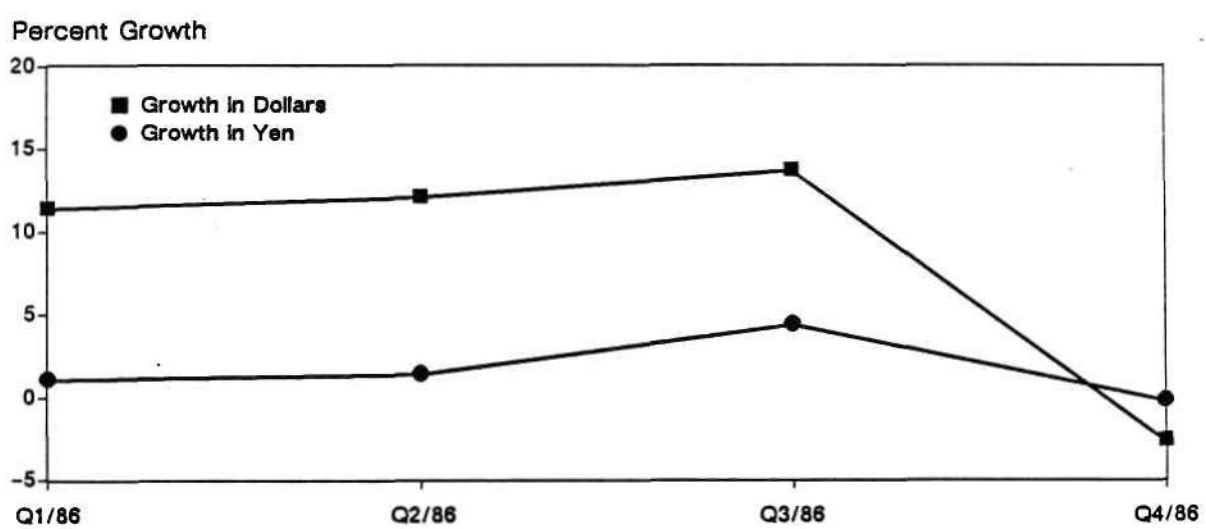
FALLING DOLLAR OVERSTATES LACKLUSTER GROWTH

SUMMARY

Worldwide semiconductor consumption measured in U.S. dollars rose 25.6 percent in 1986. This seems anomalous considering the mere 6.5 percent growth in North America. Did Japan strike again? Not really. The falling dollar overstates the real growth in consumption in overseas markets. Note the disparity in quarterly growth rates of Japanese semiconductor consumption measured in U.S. dollars versus growth rates measured in yen (see Figure 1). Japanese semiconductor consumption grew only 1.9 percent in 1986 as measured in yen, but this translates to a 44.9 percent growth rate as measured in U.S. dollars.

Figure 1

1986 JAPANESE SEMICONDUCTOR CONSUMPTION GROWTH RATES
(Dollars Versus Yen)



Source: Dataquest
April 1987

Dataquest expects slow but positive growth in all regions of the world in the first quarter of 1987, recovering to a healthy but moderate 15.1 percent growth in worldwide semiconductor consumption for 1987. We expect the recovery to pick up momentum in 1988, resulting in a hefty 21.6 percent growth. Though these growth rates pale in comparison to historical boom years, we must bear in mind that the industry has now grown much bigger and seems to be maturing in certain product markets.

Our projections assume a fairly stable U.S. dollar exchange rate with the yen. Given the steep fall of the U.S. dollar in 1986, readers should exercise much caution when comparing growth rates in 1986 to subsequent years. We are indeed projecting a much healthier semiconductor industry for 1987 and 1988 in all regions, compared to the lackluster industry growth in 1986.

ASSUMPTIONS FOR THIS FORECAST

Book/Bill Trend is Up

The U.S. book/bill ratio has been rising since October, and we expect it to stay above 1.0 during the first quarter of 1987. The worldwide book/bill ratio rose to parity in November 1986, after falling to 0.9 in the third quarter of 1986. We expect the worldwide book/bill ratio to stay above parity during the first quarter of 1987.

Movement to ROW Dampens U.S. Growth

Preliminary results from a Dataquest Semiconductor Application Markets (SAM) procurement survey indicate a 9 percent shift in semiconductor purchases from the United States to the Asia-Pacific basin in 1987, compared to a 7 percent shift in 1986. Since the U.S. dollar exchange rate remains virtually unchanged relative to Korea and Taiwan, U.S. electronics companies are leveraging this movement to compete with the Japanese. The movement to ROW (Rest of World) has a significant moderating effect on the growth in U.S. semiconductor consumption.

Exchange Rates Remain Stable

Since the forecast is expressed in U.S. dollars, it is critical to note the assumption that the U.S. dollar remains stable with respect to the yen, the European basket of currencies, and the Asia-Pacific currencies. The yen is pegged at 160 for a dollar.

TRACKING REGIONAL SHIFTS

North American share of worldwide semiconductor consumption declined from about 39 percent in 1985 to less than a third in 1986. At the same time, Japanese share rose from about 35 percent in 1985 to 40 percent in 1986. European share declined one percentage point in 1986. Though the shifts in 1986 are attributed mostly to the rise of the yen, the gain in ROW share from 7.7 percent in 1985 to 9.5 percent in 1986 has been under fairly stable currency exchange rates. We are projecting the trend to continue, with ROW share rising to 12 percent by 1988 (see Table 1).

Table 1

WORLDWIDE SEMICONDUCTOR CONSUMPTION
(Percent Change, U.S. Dollars)

	Yearly Growth			Market Share		
	1986	1987	1988	1986	1987	1988
North America	6.5%	12.7%	23.4%	32.8%	32.1%	32.6%
Japan ($)	44.9%	14.0%	19.0%	40.0%	39.6%	38.7%
Japan (yen)	1 9%	9.0%	19.0%			
Europe	17.2%	10.0%	19.9%	17.7%	16.9%	16.7%
ROW	55.6%	38.1%	28.2%	9.5%	11.4%	12.0%
Worldwide	25.6%	15.1%	21.6%	100.0%	100.0%	100.0%

Source: Dataquest
April 1987

WORLD PRODUCT CONSUMPTION TRENDS

Our 1987 quarterly forecast of worldwide product consumption is shown in Table 2. During 1986, MOS logic was the star product category, growing more than 41 percent. MOS microdevices grew 35 percent. Linear and discrete devices showed surprising strength, growing 32 percent and 22 percent, respectively. MOS memory was the weakest product category, growing less than 8 percent.

Table 2

ESTIMATED WORLDWIDE SEMICONDUCTOR CONSUMPTION
(Millions of U.S. Dollars)

	1986	Q1/87	Q2/87	Q3/87	Q4/87	1987	% Chg. 1987
Total Semiconductor	31,173	8,444	8,771	9,125	9,550	35,889	15.1%
Total IC	23,885	6,551	6,834	7,140	7,495	28,019	17.3%
Bipolar Digital	4,397	1,162	1,220	1,262	1,314	4,957	12.7%
Memory	680	180	191	200	204	774	13.8%
Logic	3,717	982	1,029	1,062	1,110	4,183	12.5%
MOS Digital	13,192	3,757	3,929	4,144	4,372	16,202	22.8%
Memory	4,329	1,192	1,246	1,321	1,392	5,151	19.0%
Micro	3,699	1,029	1,078	1,145	1,218	4,470	20.8%
Logic	5,164	1,536	1,605	1,678	1,762	6,581	27.4%
Linear	6 296	1,632	1,685	1,734	1,809	6,860	9.0%
Discrete	5,697	1,475	1,504	1,540	1,597	6,116	7.4%
Optoelectronic	1,591	418	433	445	458	1,754	10.2%

	1987	Q1/88	Q2/88	Q3/88	Q4/88	1988	% Chg. 1988
Total Semiconductor	35,889	9,953	10,683	11,262	11,750	43,647	21.6%
Total IC	28,019	7,861	8,526	9,052	9,517	34,955	24.8%
Bipolar Digital	4,957	1,387	1,479	1,531	1,592	5,988	20.8%
Memory	774	210	219	228	236	892	15.3%
Logic	4,183	1,177	1,260	1 303	1,356	5,096	21.8%
MOS Digital	16,202	4,612	5,101	5,506	5,858	21,077	30.1%
Memory	5,151	1,475	1,727	1,885	1,971	7,058	37.0%
Micro	4,470	1,271	1,352	1,451	1,559	5,633	26.0%
Logic	6,581	1,866	2,022	2,170	2,328	8,386	27.4%
Linear	6,860	1,862	1,946	2,015	2,067	7,890	15.0%
Discrete	6,116	1,619	1,660	1,689	1,699	6,667	9.0%
Optoelectronic	1,754	473	497	521	534	2,025	15.5%

Source: Dataquest
April 1987

Our projection is for MOS logic and MOS micros to remain strong growth areas in 1987 and 1988, with growth rates in the 20 to 30 percent range. MOS memory is expected to rebound to 19 percent in 1987 and 38 percent in 1988, as production ramps up for 1Mb DRAMs. Discretes are projected to slow down as ASIC penetration increases. Linear (analog) growth will slow down to track total semiconductors.

DATAQUEST CONCLUSIONS

Although the sharp fall of the U.S. dollar against the yen dramatically overstates the Japanese consumption growth rates, 1986 was a slow year. We expect healthy but moderate growth in world semiconductor consumption in 1987, strengthening into 1988. We seem to miss the fever of the customary upswing, but the reality is a moderate and more stable growth in a bigger industry that is getting older and wiser.

George Burns
Howard Bogert

Dataquest
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Research Newsletter

SEMS Code: 1987-1988 Newsletters: April 1987-5

COPING WITH THE CRISES OF MODERATE GROWTH

SUMMARY

The semiconductor industry is accustomed to wide swings in its marketplace--frenzied growth followed by abrupt recessions. Now, for the second year in a row, it looks like there will be only moderate growth, lacking the luster of the usual industry upswings.

The challenge for the U.S. semiconductor industry is to learn to cope with this moderate growth in consumption. Industry participants are continuing to consolidate and restructure to deal with the reality of lower long-term growth rates. The continued shift of U.S. electronic equipment production to the Asia-Pacific basin will have a significant moderating effect on growth in U.S. semiconductor consumption.

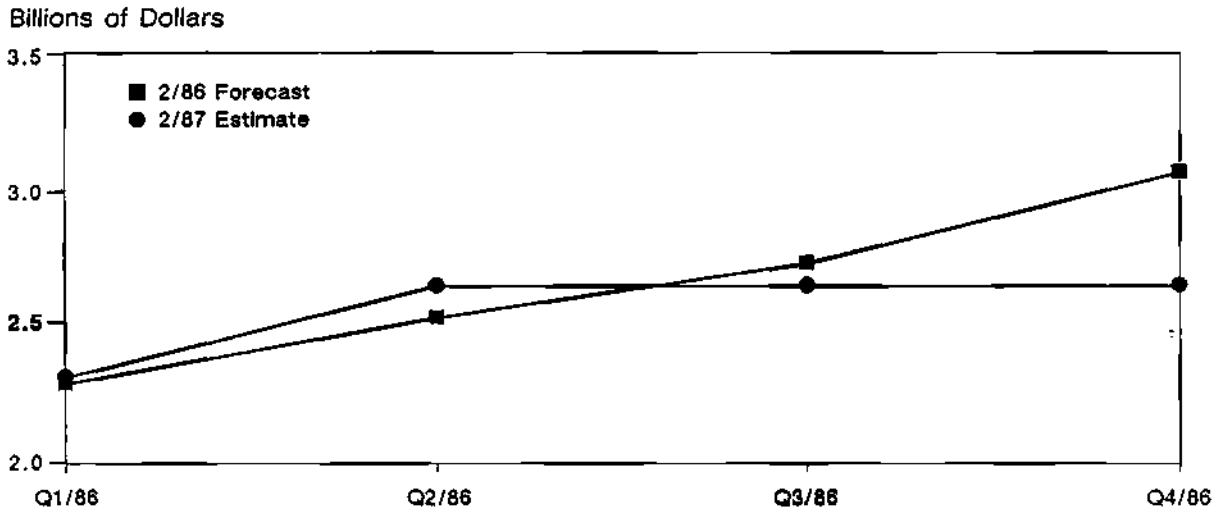
U.S. semiconductor consumption grew 6.5 percent in 1986 as Dataquest projected at the October Semiconductor Industry Conference. We now project positive growth in the first quarter and an upswing in the second quarter of 1987. Though annual consumption in 1987 is expected to grow 12.7 percent or twice the 1986 rate, this growth rate pales in comparison to the historical rates in the boom years. We do not anticipate growth rates in excess of 20 percent until in 1988.

HOW DID WE DO WITH LAST YEAR'S FORECAST?

A comparison of the quarterly growth rates that we forecast in February 1986 with our current estimate of 1986 consumption is shown in Figure 1. Shipments grew faster than we predicted in the second quarter of 1986, and then flattened out rather than continuing to grow as we expected. Annual shipments in 1986 in U.S. dollars came within 4 percent of what we predicted in February 1986.

Figure 1

U.S. QUARTERLY SEMICONDUCTOR CONSUMPTION
1986



Source: Dataquest
April 1987

ASSUMPTIONS FOR THIS FORECAST

The Book-to-Bill is Up

The book-to-bill ratio has been rising since October, and we expect the current level of bookings to result in 1.1 percent growth in first-quarter shipments. We expect the book-to-bill to stay above 1.0 percent in the first quarter, contributing to a healthy 6.2 percent growth in the second quarter. Recent upward movement in semiconductor stocks also anticipates this growth.

Modest Growth in End Equipment

Our current semiconductor industry forecast assumes a modest 7 percent growth in end-equipment shipments in 1987. End-equipment trends tracked include computers, communications, industrial, transportation (including automotive), military, and consumer electronics.

Movement to ROW Dampens U.S. Growth

Preliminary results from a Dataquest Semiconductor Application Markets (SAM) procurement survey indicate a 9 percent shift in electronics production from the United States to the Asia-Pacific basin in 1987, compared with a 7 percent shift in 1986. Since the U.S. dollar exchange rate remains virtually unchanged relative to Korea and Taiwan, U.S. electronics companies are leveraging this movement to compete with the Japanese. The movement to ROW has a significant moderating effect on the growth in U.S. semiconductor consumption.

Other Economic Assumptions--1987

GNP is expected to grow about 3 percent in 1987, with about a 4 percent rise in the consumer price index. Further interest rate cuts are expected to spur investment.

For the semiconductor industry, we expect a stable environment with tight inventory levels and no large swings. We do not expect shortages or steep price erosions. Capacity remains largely underutilized, with about 70 percent utilization in 1987.

THE FORECAST: MODERATE GROWTH

Our quarterly forecast of North American semiconductor consumption for 1987 and 1988 is shown in Table 1.

Table 1

ESTIMATED NORTH AMERICAN SEMICONDUCTOR CONSUMPTION
(Millions of Dollars)

	1986	Q1/87	Q2/87	Q3/87	Q4/87	1987	% Chg. 1987
Total Semiconductor	10,233	2,678	2,845	2,922	3,087	11,532	12.7%
Total IC	8,162	2,159	2,300	2,362	2,502	9,323	14.2%
Bipolar Digital	2,061	513	545	563	605	2,226	8.0%
Memory	339	90	97	101	106	394	16.2%
Logic	1,722	423	448	462	499	1,832	6.4%
MOS Digital	4,449	1,229	1,297	1,325	1,383	5,234	17.6%
Memory	1,570	416	441	448	459	1,764	12.4%
Micro	1,241	330	348	354	375	1,407	13.4%
Logic	1,638	483	508	523	549	2,063	25.9%
Linear	1,652	417	458	474	514	1,863	12.8%
Discrete	1,652	413	431	444	466	1,754	6.2%
Optoelectronic	419	106	114	116	119	455	8.6%

	1987	Q1/88	Q2/88	Q3/88	Q4/88	1988	% Chg. 1988
Total Semiconductor	11,532	3,265	3,551	3,666	3,744	14,226	23.4%
Total IC	9,323	2,667	2,925	3,031	3,116	11,739	25.9%
Bipolar Digital	2,226	638	681	701	718	2,738	23.0%
Memory	394	109	113	118	123	463	17.5%
Logic	1,832	529	568	583	595	2,275	24.2%
MOS Digital	5,234	1,501	1,682	1,761	1,824	6,768	29.3%
Memory	1,764	499	585	615	598	2,297	30.2%
Micro	1,407	409	456	479	526	1,870	32.9%
Logic	2,063	593	641	667	700	2,601	26.1%
Linear	1,863	528	562	569	574	2,233	19.9%
Discrete	1,754	475	493	499	488	1,955	11.5%
Optoelectronic	455	123	133	136	140	532	16.9%

Source: Dataquest
April 1987

CONSUMPTION TRENDS

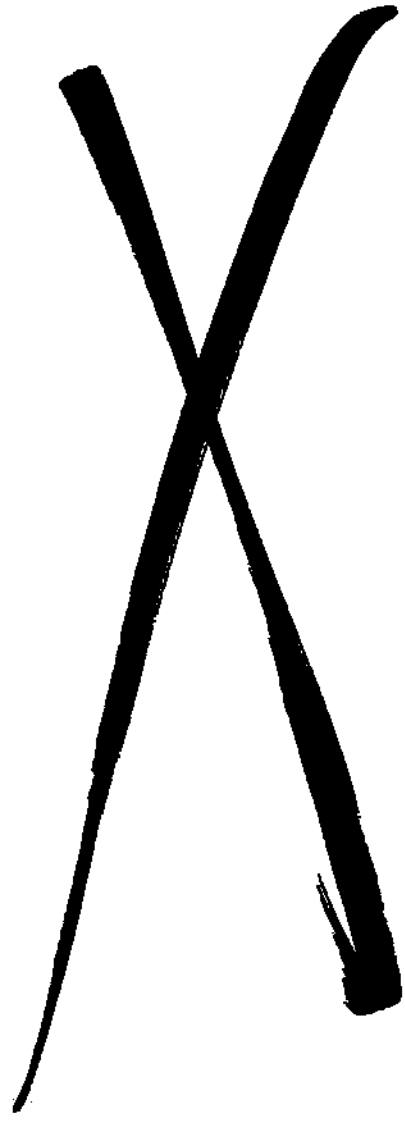
While 1986 was a slow year with only 6.5 percent growth in overall North American semiconductor consumption, some product categories fared better than others. MOS logic was a winner, growing 28.2 percent, particularly due to the strength in ASICs. MOS memory declined 11.5 percent and MOS micros grew only 3.8 percent, slower than total semiconductors. Linear and discrete product categories did better than total semiconductors.

Our projection for 1987 is for MOS logic to remain the fastest-growing segment, with ASICs showing stellar performance. MOS memories and micros are expected to rebound with growth rates more than 12 percent, hinging on an upswing in computers and data processing equipment.

DATAQUEST CONCLUSIONS

Dataquest projects 12.7 percent growth in U.S. semiconductor consumption in 1987. Though this is moderate growth, this rate is about twice the rate of growth in 1986. We are already seeing signs of an upswing. There is optimism in the industry. End-equipment demand seems to be bottoming out, inventory levels are low, prices are holding, and bookings are up.

George Burns
Howard Z. Bogert



May Newsletters

The following is a list of newsletters found in this section:

Dataquest
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Research Newsletter

SEMS Code: Newsletters 1987-1988
1987-14

CAPITAL SPENDING FORECAST: SLOWER BUT STEADIER GROWTH

INTRODUCTION

The capital equipment industry has just experienced its worst downturn in history. In 1986, worldwide capital spending, including captive spending, declined 30 percent. Dataquest believes that the capital equipment industry can now look forward to growth in four out of the next five years. This growth, however, will not be as strong as it has been in the past. We believe that future growth will be slower for two reasons: first, the growth of semiconductor consumption and production will be slower; second, a dollar's worth of capital equipment will be more productive than it has been in the past.

1986: MARKET CRASH

Japan's capital expenditures fell from ¥793 billion in 1985 to ¥293 billion in 1986, a 63 percent drop during calendar 1986. Expressed in dollars, the decline, although severe, was not quite as precipitous. The 1985 figure of $3.3 billion dropped to $1.7 billion in 1986, or 47 percent.

This severe decline in Japanese capital spending is due to major shocks that have hit the Japanese economy in general and the semiconductor industry in particular. These changes include:

- Sluggish exports due to trade friction with Japan's leading trading partners, including the United States and Europe
- Sharply reduced profits and even some layoffs
- Excess capacity and declining domestic prices caused by growing competition from new entrants into the commodity DRAM market, especially from Pacific Rim countries
- The yen shock, which has raised production costs by more than 50 percent within the last year

Spending by merchant semiconductor manufacturers in North America also experienced a severe decline, from $2.3 billion in 1985 to $1.6 billion in 1986, a full 28 percent.

Capital spending by captive semiconductor manufacturers also fell in 1986, from $1.0 billion in 1985 to $0.9 billion in 1986, or 12 percent.

Europe and the rest of the world (ROW) were the two 1986 capital spending bright spots. Measured in dollars, spending in Europe increased 12 percent, from $600 million in 1985 to $670 million in 1986. Many equipment companies have reported sales either even with 1985 or higher. However, measured in local currency units, capital spending, even in Europe, experienced an 11 percent decline in 1986.

Spending in ROW (especially in Korea, Taiwan, Hong Kong, Thailand, and Singapore) was the only unalloyed bright spot in 1986; it grew 25 percent. However, ROW represented only 5 percent of the market for property, plant, and equipment (PPE) in 1986.

Figure 1 summarizes the 1986 market for capital spending in dollars. On a worldwide basis, capital spending declined 30 percent--from 1985's $7.5 billion to $5.3 billion in 1986.

1987 AND BEYOND: THE FORECAST

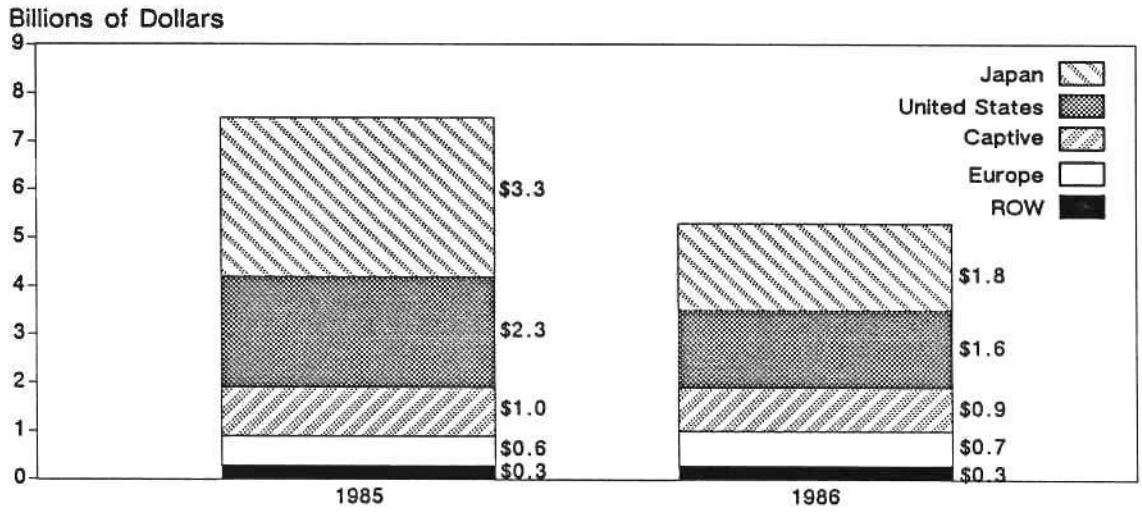
Except in Japan, we expect 1987 to be a year of recovery for the capital equipment industry. We look forward to a 10 percent increase in capital spending worldwide. The main force behind this increase is the continuing recovery of the semiconductor industry itself. Semiconductor manufacturers contacted by Dataquest in April and May were markedly more confident about their business than they were in January. Semiconductor companies are firm about their capital spending plans and in some cases have increased their plans markedly since the first of the year. We believe that semiconductor production will increase 10 percent worldwide in 1987.

When measured in dollars, capital spending in Japan will decline another 4 percent, to $1.7 billion. When measured in yen, the decline sounds even more painful: 11 percent. The reasons for this downward trend are the continuing uncertainty about exchange rates, overcapacity, low or nonexistent profit levels, and continuing trade friction.

Table 1 presents a regional breakdown of capital spending in 1987 versus 1986.

Figure 1

MARKET CRASH



Source: Dataquest
May 1987

Table 1

ESTIMATED REGIONAL CAPITAL SPENDING
(Millions of Dollars)

	1986	1987	Percent Change
North America	$1,640	$1,812	10%
Japan	1,754	1,688	(4%)
Europe	670	764	14%
ROW	275	406	48%
Captive	920	1,104	20%
Total	$5,260	$5,774	10%

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
May 1987

1987 and Beyond: Highlights

As semiconductor consumption and production continue to expand in 1988, capacity utilization levels will rise. We therefore expect capital spending, including Japan's, to increase again in 1988. However, since we believe that semiconductor consumption and production will not grow in 1989, we expect a pause in capital spending growth that year. After 1989, however, we expect a renewed growth in capital spending (see Table 2). Also, after 1989, we expect a significant proportion of capital spending to be technology driven as a new generation of devices such as the 4Mb DRAM begins to go into production.

European capital spending will reach $1.7 billion by 1992, which represents a compound annual growth rate (CAGR) of 17 percent between 1986 and 1992.

Table 2

ESTIMATED CAPITAL SPENDING

	1982	1983	1984	1985	1986
North America	$1,212	$1,452	$3,051	$2,291	$1,640
Japan	921	1,698	3,578	3,332	1,754
Europe	315	350	630	600	670
ROW	45	91	201	220	275
Captive	501	542	965	1,045	920
Worldwide Capital Spending	$2,994	$4,133	$8,424	$7,488	$5,260
Percent Change		38%	104%	(11%)	(30%)

	1987	1988	1989	1990	1991	1992
North America	$1,812	$2,428	$2,292	$2,727	$ 3,436	$ 4,285
Japan	1,688	2,026	2,330	3,495	4,893	6,543
Europe	764	953	965	1,125	1,405	1,728
ROW	406	606	648	810	969	1,135
Captive	1,104	1,309	1,244	1,294	1,527	1,852
Worldwide Capital Spending	$5,774	$7,322	$7,478	$9,451	$12,230	$15,543
Percent Change	10%	27%	2%	26%	29%	27%

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
May 1987

ROW capital spending will grow at a CAGR of 27 percent between 1986 and 1992, to $1.1 billion.

Captive manufacturers such as IBM and AT&T are a major market for semiconductor equipment. Captives accounted for 35 percent of total North American capital spending in 1986. We expect spending by the captives to increase 20 percent in 1987 and to grow to $1.8 billion in 1992.

Merchant capital spending in North America will grow at a slower rate than in the past--a 17 percent CAGR from 1986 to 1992. Because of this slower growth rate and the severity of the recent decline in capital spending, merchant capital spending will not reach its 1984 level of over $3 billion again until 1991.

Individual company capital spending in North America is shown in Table 3.

Table 3

NORTH AMERICAN COMPANY CAPITAL SPENDING

	1975	1976	1977	1978	1979	1980	1981
AMD	$ 1	$ 6	$ 10	$ 20	$ 39	$ 49	$ 58
Analog Devices	2	4	7	12	10	19	16
Fairchild	20	36	15	23	58	83	140
General Electric							
Harris						45	45
Intel	11	32	46	104	97	156	157
Thomson-Mostek	3	10	24	19	42	85	98
Motorola	21	33	43	72	159	177	184
National	17	26	31	51	84	116	105
Others	56	94	105	177	333	318	285
Philips-Signetics	4	10	19				
Texas Instruments	35	62	88	122	251	300	145
Subtotal of Domestic Company Spending	$170	$312	$388	$599	$1,073	$1,348	$1,233
Non-U.S.-Owned Company Spending in United States							
NEC	-	-	-	-	-	-	-
Philips-Signetics	-	-	-	$ 40	$ 50	$ 90	$ 115
Siemens	-	-	-	-	-	-	-
Thomson-Mostek	-	-	-	-	-	-	-
Total North American Capital Spending	$170	$312	$388	$639	$1,123	$1,438	$1,348
Percent Change		84%	24%	65%	76%	28%	(6%)

(Continued)

Table 3 (Continued)

NORTH AMERICAN COMPANY CAPITAL SPENDING

	1982	1983	1984	1985	1986	1987
AMD	$ 67	$ 111	$ 237	$ 172	$ 55	$ 120
Analog Devices	19	24	58	62	37	50
Fairchild	156	125	195	135	135	68
General Electric		64	107	81	50	50
Harris	35	25	50	50	40	30
Intel	138	146	388	214	150	225
Thomson-Mostek	47	78	123			
Motorola	160	174	412	330	250	338
National	82	120	300	184	117	100
Others	311	293	567	703	494	451
Philips-Signetics						
Texas Instruments	140	232	472	281	213	230
Subtotal of Domestic Company Spending	$1,155	$1,392	$2,908	$2,213	$1,541	$1,660
Non-U.S.-Owned Company Spending in United States						
NEC					$ 10	$ 12
Philips-Signetics	$ 55	$ 58	$ 133	$ 50	60	100
Siemens					20	15
Thomson-Mostek				39	9	25
Total North American Capital Spending	$1,210	$1,450	$3,041	$2,302	$1,640	$1,812
Percent Change	(10%)	20%	110%	(24%)	(29%)	(11%)

Source: Dataquest
May 1987

A Burst of Spending in Japan after 1987

We expect Japanese capital spending to recover somewhat in 1988, increasing from $1.69 billion in 1987 to $2.0 billion in 1988, or 20 percent. After 1988, we expect Japanese capital spending to increase at a rate much faster than the worldwide average. This is because the $6.9 billion of capital put on-stream in 1984 and 1985 will be nearing the end of its productive life and will have to be replaced. This 1984-1985 equipment will represent more than 50 percent of the Japanese installed base through the remainder of this decade.

As a consequence of the aging of a significant part of the Japanese installed base, we expect Japanese capital spending to increase 15 percent in 1989 when the worldwide market for capital goods will be flat; we also expect that in 1990 and 1991, Japanese capital spending will increase by 50 percent and 40 percent, respectively.

Table 4 shows individual Japanese company spending on a calendar year basis.

Table 4

JAPANESE MERCHANT COMPANY CAPITAL SPENDING
(Calendar Years, Millions of Dollars)

	1976	1977	1978	1979	1980	1981
Fuji Electric	0	0	0	0	0	0
Fujitsu	$ 3	$ 22	$ 48	$ 64	$110	$145
Hitachi	20	22	43	59	93	149
Japan Semiconductor	0	0	0	0	0	0
Matsushita	10	11	19	41	88	86
Mitsubishi	17	22	19	41	35	59
NEC	34	37	67	105	132	172
NJRC	0	0	0	0	0	0
NMB	0	0	0	0	0	0
Oki	10	15	10	14	53	54
Rohm	0	0	0	0	0	0
Sanken Electric	0	0	0	0	0	0
Sanyo	7	7	7	18	35	54
Sharp	0	0	7	37	37	43
Shindengen	0	0	0	0	0	0
Seiko Epson	0	0	0	0	0	0
Sony	0	0	0	0	0	0
Toshiba	14	19	24	37	48	72
Others	0	0	0	0	0	0
Total	$115	$156	$242	$416	$632	$834

(Continued)

Table 4 (Continued)

JAPANESE MERCHANT COMPANY CAPITAL SPENDING
(Calendar Years, Millions of Dollars)

	1982	1983	1984	1985	1986
Fuji Electric	$ 16	$ 26	$ 51	$ 50	$ 30
Fujitsu	141	226	485	303	96
Hitachi	145	264	506	387	132
Japan Semiconductor	0	0	0	0	30
Matsushita	36	89	371	366	144
Mitsubishi	80	132	274	261	120
NEC	169	247	544	517	180
NJRC	8	9	17	21	30
NMB	0	0	59	59	0
Oki	44	47	110	109	60
Rohm	8	13	25	38	48
Sanken Electric	8	13	25	25	24
Sanyo	40	51	135	197	108
Sharp	32	68	110	151	132
Shindengen	4	4	13	13	18
Seiko Epson	20	38	76	34	30
Sony	20	38	59	151	96
Toshiba	113	366	574	517	389
Others	36	68	143	134	90
Total	$921	$1,698	$3,578	$3,332	$1,754

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
May 1987

A SLOWER LONG-TERM GROWTH

As shown in Table 2, we expect healthy growth during four out of the next five years. This growth, however, will not be as robust as it has been in the past. For the period from 1985 to 1992, the worldwide CAGR is 11 percent; for the period from 1980 to 1985 it was 27 percent.

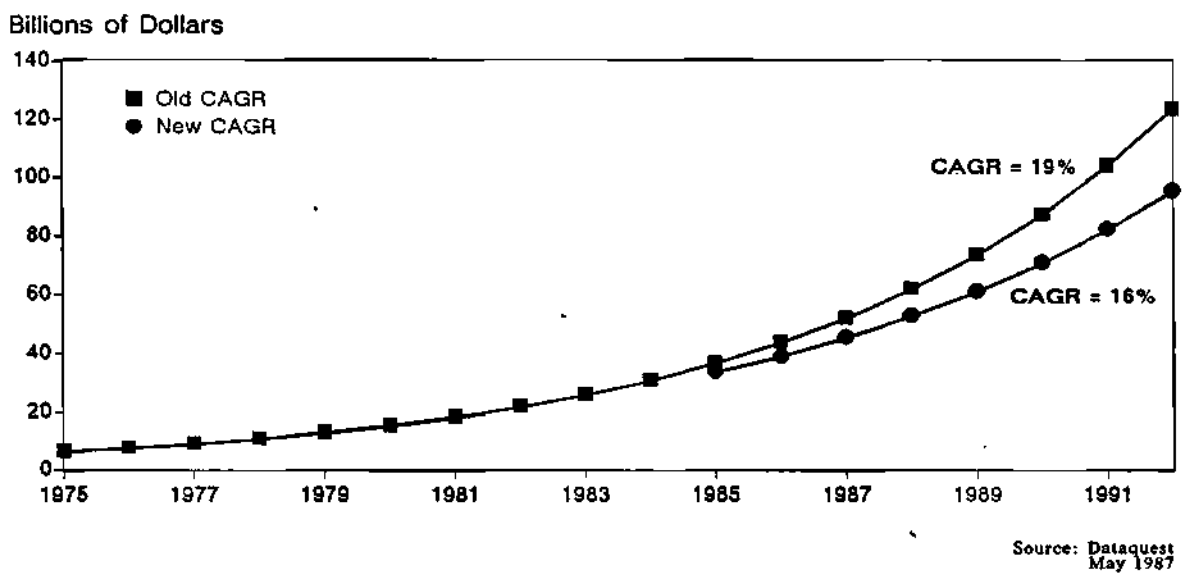
The CAGR of capital spending has slowed down for two reasons: first, the CAGR of the semiconductor industry itself has slowed; second, the productivity of capital has begun to increase.

From 1975 to 1985, worldwide merchant semiconductor production has grown at a 19 percent CAGR. Dataquest now expects semiconductor production to grow at a slower rate of 16 percent. This new, lower, long-term growth rate is

due to the absence of a new "hoola-hoop" such as the PC to drive the industry as it did in 1982 through 1984. It is also due to the success of the industry. Because semiconductors are now found throughout the economy, they will increasingly be influenced by the secular trends of the economy. The effect of this new, slower growth rate will be that the market for semiconductors will be $28 billion less in 1992 than it would have been (see Figure 2). For equipment makers this means $5 billion fewer revenue dollars in 1992 than if the CAGR had remained constant.

Figure 2

A SLOWER WORLDWIDE MERCHANT CAGR
(The Old and the New)

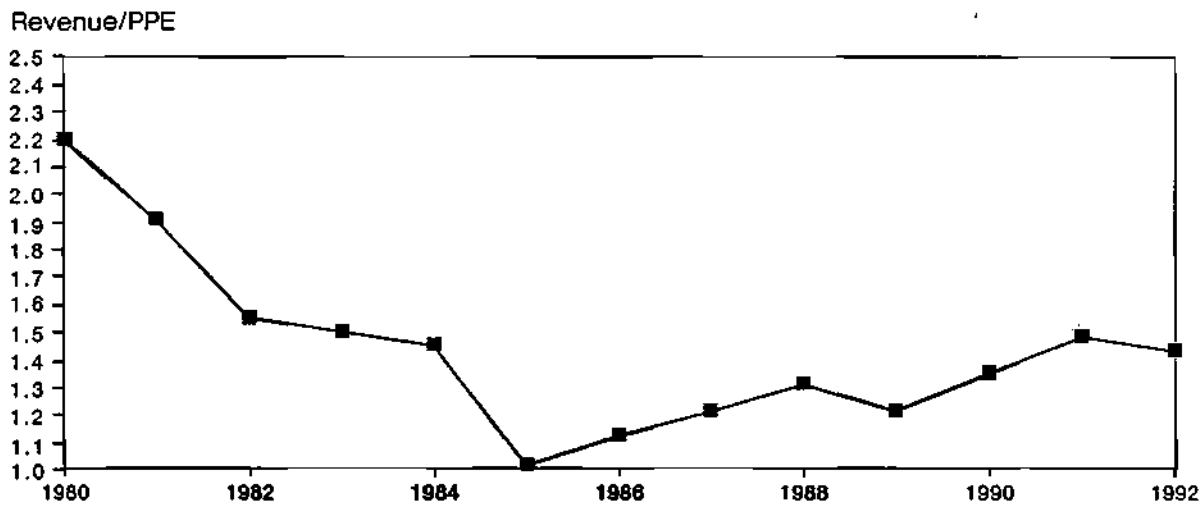


Source: Dataquest May 1987

As mentioned above, the second reason for the slowdown in the capital spending CAGR is the increasing productivity of capital. Capital productivity is the amount of revenue that is generated with a given installed PPE base. Historically, this ratio has declined (see Figure 3). We believe, however, that capital productivity has begun to rise and will continue to do so. There are several reasons for this. Computer-integrated manufacturing (CIM) will allow manufacturers to schedule many different product mixes and maintain line balance while increasing equipment utilization. (We estimate that equipment utilization is presently in the neighborhood of 40 percent.) Manufacturers will increase their yields because automation will remove people from clean rooms. Lower particulate from semiconductor equipment and materials will also increase yields.

Figure 3

REVENUE/PPE
WORLDWIDE INSTALLED BASE



Source: Dataquest
May 1987

Figure 4 shows the effects of both the slowdown of semiconductor production and of increasing capital productivity. For the first period, from 1975 to 1985, worldwide capital spending grew at a CAGR of 41 percent; worldwide semiconductor production, including captives, grew at a CAGR of 21 percent. From 1980 to 1985, however, both capital spending and production CAGRs had fallen; the CAGR of capital spending fell more. From 1985 to 1992, we expect that the capital spending CAGR will fall below that of semiconductor production. Growth will occur, but it will be slower than it has been in the past.

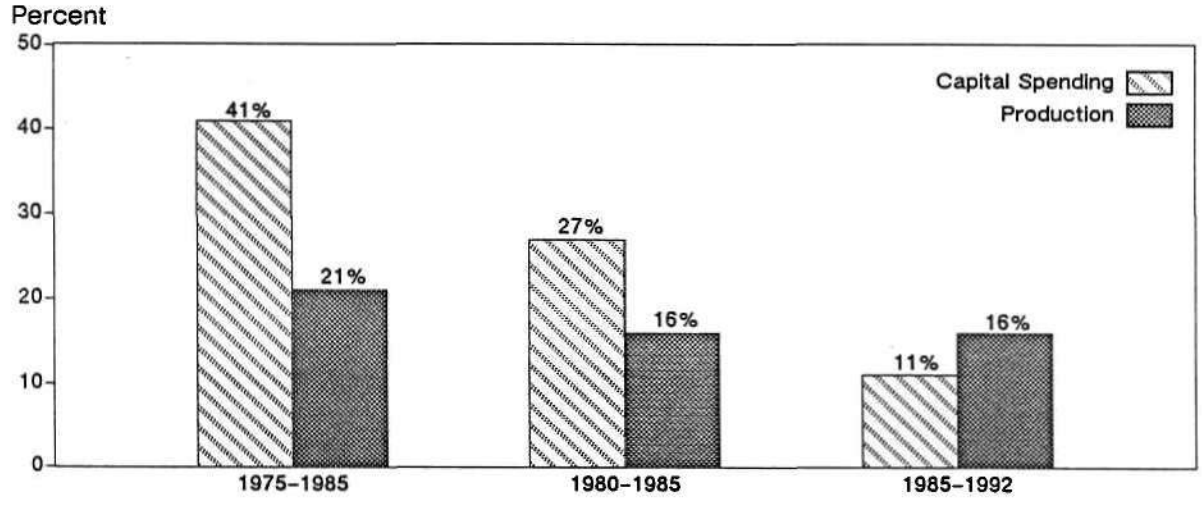
CONCLUSION

Although growth will be slower for the capital equipment industry than it has been in the past, there will be growth--and that is an improvement over the last two years. Moreover, the growth will be relatively sustained: we expect healthy growth in four out of the next five years. Semiconductor manufacturers will spend first to increase capacity and then to introduce new manufacturing technology. We expect that the CAGR of the semiconductor equipment industry from 1985 to 1992 will be 11 percent, about four times the growth rate of the U.S. economy, and almost 50 percent higher than the growth rate for the electronics industry in the United States. Although less so than in the past, the semiconductor capital equipment industry is still a growth industry.

George Burns

Figure 4

DECLINING CAGR
CAPITAL SPENDING VERSUS PRODUCTION



Source: Dataquest
May 1987

Dataquest
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Research Newsletter

SEMS Code: Newsletters
1987-13

SILICON AND EPITAXIAL WAFER MARKETS: AN INDUSTRY OVERVIEW

Dataquest recently completed an analysis of the worldwide silicon and epitaxial markets. This newsletter provides an overview of silicon and epitaxial wafer companies, the silicon and epitaxial wafer market size by region, the effects of yen appreciation on wafer pricing, and concludes with Dataquest's forecast of silicon consumption by region and U.S. wafer size distribution.

MARKET SUMMARY

In 1985, silicon and epitaxial wafer sales to the worldwide semiconductor industry by merchant silicon companies were $1,266.5 million. Silicon wafers accounted for $1,020.9 million (80.6 percent) of this figure, and epitaxial wafer sales accounted for $245.6 million (19.4 percent). These sales represented 1,038 million square inches of silicon wafers and 85 million square inches of epitaxial wafers. The average selling price of silicon wafers ranged from $0.90 to $1.00 per square inch as compared with $2.80 to $2.90 per square inch for epitaxial wafers. Several semiconductor manufacturers have captive production of silicon material, which accounted for an additional 177 million square inches of silicon that year. When merchant wafer sales are added to captive silicon production, total silicon consumption amounted to 1,300 million square inches in 1985.

Table 1 summarizes worldwide silicon and epitaxial wafer sales (and market share) for the top six merchant silicon companies in 1985. The market is strongly dominated by four Japan-based silicon companies, Monsanto of the United States, and Wacker of West Germany.

SILICON PRODUCERS

Dataquest defines companies that produce silicon and epitaxial wafers as either merchant silicon companies or captive silicon producers. Merchant silicon companies are suppliers such as Monsanto Electronic Materials Company

in the United States, Shin-Etsu Handotai (also known as SEH) in Japan, and Wacker in Western Europe. These three merchant silicon companies, along with about 20 more companies worldwide, produce most of the silicon consumed by the semiconductor industry today.

Silicon is also produced to a lesser extent by both merchant and captive semiconductor manufacturers. Dataquest refers to these semiconductor manufacturers collectively as captive silicon producers because they grow single-crystal silicon to produce wafers for their own internal consumption. Captive producers with significant internal silicon production include AT&T, IBM, Motorola, and Texas Instruments in the United States, Philips in Europe, and Hitachi in Japan. Dataquest estimates that the U.S. captive silicon producers meet from 50 to 75 percent of their silicon requirements with captive silicon operations, whereas this amount is approximately 30 percent for Hitachi and Philips.

WORLDWIDE MERCHANT SILICON MARKET

Table 2 contains a list of merchant silicon manufacturers that were active in the world market in 1985. This list, organized by region in which the company headquarters are based, summarizes whether a company offers silicon and/or epitaxial wafers. Fifteen of the 23 companies are located in the United States, 3 in Europe, and 5 in Japan. (The acquisition by Japanese manufacturers of U.S. silicon companies NBK, Siltec, and U.S. Semiconductor will be discussed in a later section.) Fourteen manufacturers supply epitaxial wafers, 16 supply silicon wafers, and 7 provide both types of wafers. (Dynamit Nobel began manufacturing epitaxial wafers in late 1986, so is not included in the count of epitaxial wafer suppliers for 1985.) Table 2 also includes five new merchant silicon companies that entered the market in 1986/1987; two are located in Japan, two in Europe, and one in Korea.

Table 2 shows the percentage of silicon substrate material (based on square inches) each company produces internally and the percentage purchased from other silicon vendors. This is an important distinction since several United States-based epitaxial wafer manufacturers purchase some or all of their silicon substrate from other companies. For example, in 1985, Cincinnati-Milacron, an epitaxial silicon wafer company, internally produced 60 percent of its silicon substrate and purchased 40 percent from other merchant silicon companies. This practice must be noted when evaluating total wafer consumption because of the potential problem of double-counting million square inches of silicon based on company sales alone.

Table 3 presents the combined sales of silicon and epitaxial wafers by regionally based merchant companies to given regions of the world. For example, in these tables, Shin-Etsu Handotai's worldwide sales, which include the sales of Shin-Etsu's U.S. subsidiary, SEH America, are included under the heading "Japan-Based Companies." Similarly, the worldwide sales of Europe-based Wacker Chemitronic include the sales of its U.S. affiliate, Wacker Siltronic.

EFFECTS OF YEN APPRECIATION

In 1986, Japanese silicon companies had to face the pressures of restricted markets overseas because of the yen's appreciation. Silicon wafer pricing has always varied from region to region. However, Japanese silicon companies found it difficult to compete in the U.S. and European markets in 1986 due to large differences in wafer pricing affected by exchange rate factors. For example, in 1984, the average U.S. price of a 100mm wafer was $10.50. At an exchange rate of ¥237/$1, a Japanese silicon company would receive ¥2,490 for a 100mm wafer. In 1986, the U.S. average selling price of a 100mm wafer came down to $10.00. However, at the 1986 exchange rate of ¥167/$1, a Japanese silicon company would now only receive ¥1,750 for a 100mm wafer sold in the United States.

Because of the high yen, Japanese silicon companies exporting silicon wafers to the United States have two options: 1) meet and maintain U.S. average selling prices for wafers and lose on margins in order to maintain U.S. market share and customer relationships, or 2) raise wafer prices in the United States to regain a given yen rate of return, and as a consequence, lose market share. Similar analysis of wafer pricing for 125mm and 150mm wafers confirms that Japanese silicon companies in 1986 were caught between the proverbial rock and a hard place, and had difficulty competing for silicon sales overseas.

Overseas Acquisitions

On the one hand, the high yen has made silicon exports from Japan more difficult. On the other hand, it has made the acquisition of U.S. firms more attractive. As mentioned earlier, in 1986, two Japanese silicon companies chose the latter method of competing in the U.S. market. Mitsubishi Metal acquired Siltec in the third quarter of 1986, and Osaka Titanium Company announced its plans in December to acquire U.S. Semiconductor, an epitaxial silicon wafer manufacturer.

Other Japanese companies that have established or acquired silicon facilities in the United States include silicon manufacturer Shin-Etsu Handotai (which established SEH America, a wholly owned subsidiary in Vancouver, Washington) and steelmakers Kawasaki Steel and Nippon Kokan K.K. Kawasaki Steel acquired Santa Clara-based NBK Corporation in 1984, and Nippon Kokan K.K. bought Great Western's polysilicon facility in 1985. In December 1986, Nippon Kokan K.K. announced its purchase of land in Oregon for a new 1,000-metric-ton polysilicon plant.

TOTAL MILLION-SQUARE-INCH MARKET

Table 4 combines 1985 million-square-inch sales by the merchant silicon companies and captive silicon production in the four regions of the world. Captive silicon production has been allocated to the semiconductor manufacturer's home region. Internal production by the captive silicon producers, at 150 MSI, accounts for a sizable percentage of the U.S. million square inch market of 490 MSI. The captive silicon market in Japan and Europe is much

smaller, and ROW has no captive silicon producers at this time. Japan has the largest share of the world million square inch market with 594 MSI, or 45.7 percent of the total square inch market in 1985.

FORECAST SILICON CONSUMPTION BY REGION

Table 5 contains Dataquest's forecast of silicon consumption by captive and merchant semiconductor manufacturers by region of device production. In general, we believe that the growth in silicon consumption will follow growth in device production revenue in each of the four regions through 1991. We believe that the long-term trend will be for silicon consumption (in MSI) to grow more slowly than production revenue (as measured in dollars). This translates to a slowly increasing revenue per square inch as a function of time. Factors that increase revenue per square inch include higher device ASPs and device yields. ASPs will increase as higher-valued products such as ASICs become a larger percentage of the product mix. Yields should improve as manufacturers focus on tighter particulate control and achieve shorter cycle times through manufacturing automation. However, as devices become more complex, die size typically increases. This will slow the upward trend of average revenue per square inch since yields drop with proportionately larger chips.

WAFER SIZE

The changing mix of wafer size is an indicator of the penetration of leading-edge equipment and new fab capacity. Further, as wafer diameter increases, poly usage increases at a more rapid rate, due to greater wafer thickness at the larger diameters. Estimated percent consumption of MSI of silicon by wafer size for 1982 through 1991 is presented in Table 6. This information reflects Dataquest's estimate of wafer size consumption for semiconductor production in North America.

Dataquest does not expect 125mm wafer consumption to reach the maximum levels of 100mm wafers in the United States. This is because the 125mm wafer is viewed as an interim step in the transition to 150mm wafers. The increase of 125mm wafer consumption to 30 percent of square inches in 1985 is believed to have been caused by difficulties that semiconductor manufacturers had in bringing on-line the fab equipment designed to handle 150mm wafers. This situation, coupled with the industry slowdown during 1985, increased 125mm wafer penetration, slowed the expected rise in 150mm wafer usage, and decreased 3-inch wafer usage.

The 100mm wafer will continue to account for the highest percent of consumption (as measured in MSI) for U.S. production until 1989. The 150mm wafer category is expected to increase its share throughout the decade and, by 1991, is expected to account for approximately 52 percent of silicon MSI. Although several U.S. semiconductor manufacturers are working with 200mm wafers in research and development, Dataquest does not expect this wafer size to enter the general production environment until 1988.

Peggy Marie Wood

Table 1

WORLDWIDE MERCHANT SILICON COMPANY MARKET SHARE, 1985
(Millions of Dollars)

Company	Silicon and Epitaxial Wafer Sales	Percent Share
Shin-Etsu Handotai	$ 310.0	24.5%
Wacker	205.0	16.2
Osaka Titanium Company	160.0	12.6
Monsanto	137.0	10.8
Japan Silicon	128.0	10.1
Komatsu Electronic Metals	116.0	9.2
Others	210.5	16.6
Total	$1,266.5	100.0%

Source: Dataquest
May 1987

Table 2

WORLDWIDE MERCHANT SILICON COMPANIES

	Substrate Grown	Substrate Purchased	Silicon Wafers	Epitaxial Wafers
U.S. Companies				
Cincinnati Milacron	60%	40%		X
Crysteco, Inc.	100%	0	X	
Epitaxy, Inc.	0	100%		X
General Instruments Power Semiconductor Div.	0	100%		X
Gensil	100%	0	X	
M/A-Com	50%	50%		X
Monsanto Electronic Materials Company	100%	0	X	X
NBK Corporation	100%	0	X	
Pensilco	100%	0	X	
Recticon	100%	0	X	
Silicon Services	0	100%		X
Siltec	100%	0	X	
Spire Corporation	0	100%		X
U.S. Semiconductor	0	100%		X
Virginia Semiconductor	100%	0	X	

(Continued)

Table 2 (Continued)

WORLDWIDE MERCHANT SILICON COMPANIES

Companies	Substrate Grown	Substrate Purchased	Silicon Wafers	Epitaxial Wafers
Japanese Companies				
Japan Silicon	100%	0	X	X
Komatsu Electronic Metals	100%	0	X	X
Osaka Titanium Company	100%	0	X	X
Shin-Etsu Handotai	100%	0	X	X
Toshiba Ceramics	100%	0	X	X
European Companies				
Dynamit Nobel Silicon	100%	0	X	(X-1986)
Topsil Semiconductor Materials A/S	100%	0	X	
Wacker	100%	0	X	X
New Entrants--1986				
Lucky Advanced Materials (Korea)	100%	0	X	
Nittetsu Denshi (Japan)	100%	0	X	
Okmetic (Finland)	100%		(X-1987)	
Rhone-Siltec (France)	100%	0	X	
Showa Denko (Japan)	100%	0	X	

Table 3

WORLDWIDE MERCHANT SILICON AND EPITAXIAL WAFER MARKET, 1985
(Millions of Dollars)

Region of Sales	United States-Based Company Sales	Japan-Based Company Sales	Europe-Based Company Sales	Total
United States	$216.3	$ 84.9	$ 86.7	$ 387.9
Japan	7.9	632.1	8.6	648.6
Europe	18.8	10.4	130.0	159.2
Rest of World	12.7	26.6	31.5	70.8
Total	$255.7	$754.0	$256.8	$1,266.5
Percent	20.2%	59.5%	20.3%	100.0%

Source: Dataquest
May 1987

Table 4

SILICON AND EPITAXIAL MILLION-SQUARE-INCH MARKET BY REGION, 1985

Region	Merchant	Captive	Total	Percent
United States	340	150	490	37.7%
Japan	574	20	594	45.7
Europe	143	7	150	11.5
ROW	66	0	66	5.1
Total	1,123	177	1,300	100.0%

Source: Dataquest
May 1987

Table 5

TOTAL FORECAST SILICON CONSUMPTION BY REGION*, 1986-1991
(Million Square Inches)

	1986	1987	1988	1989	1990	1991	CAGR 1987-1991
United States Merchant Mfg.	429	514	681	586	708	910	15.4%
Growth	24.8%	19.8%	32.4%	(13.9%)	20.8%	28.4%	
Captive Mfg.	135	158	185	218	256	300	17.4%
Growth	(7.9%)	17.4%	17.4%	17.4%	17.4%	17.4%	
United States	564	672	867	804	964	1,210	15.8%
Growth	15.0%	19.3%	28.9%	(7.2%)	19.9%	25.5%	
Japan	573	651	814	804	893	1,060	13.0%
Growth	(3.5%)	13.6%	25.0%	(1.3%)	11.1%	18.8%	
Europe	150	182	229	218	266	317	14.9%
Growth	0	22.4%	26.1%	(5.2%)	22.5%	19.0%	
ROW	79	99	146	161	207	254	26.7%
Growth	19.7%	38.6%	47.1%	10.3%	28.5%	22.8%	
Worldwide Silicon	1,366	1,605	2,056	1,986	2,330	2,841	15.4%
Growth	5.1%	17.5%	28.1%	(3.4%)	17.3%	21.9%	

*Region of silicon consumption, not country of company ownership

Source: Dataquest
May 1987

Table 6

UNITED STATES MILLION-SQUARE-INCH DISTRIBUTION BY WAFER SIZE
(Percent Million Square Inches)
1982-1991

Diameter	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991
2 inch	3.0%	2.5%	2.0%	0.5%	0.4%	0.4%	0.3%	0.2%	0.2%	0.1%
3 inch	45.0%	33.0%	21.0%	6.8%	5.9%	5.1%	4.2%	3.4%	2.5%	1.7%
100mm	51.0%	57.0%	63.0%	55.3%	49.9%	44.4%	39.0%	33.5%	28.1%	22.7%
125mm	1.0%	6.0%	11.0%	29.9%	28.9%	27.7%	25.7%	23.4%	21.1%	18.9%
150mm	0.0%	1.5%	3.0%	7.5%	14.9%	22.4%	29.8%	37.2%	44.6%	52.1%
200mm	0	0	0	0	0	0	1.0%	2.2%	3.4%	4.6%
Total MSI	480	566	707	490	564	672	867	804	964	1,210

Source: Dataquest
May 1987

Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987-1988 Newsletters, May 1987-12

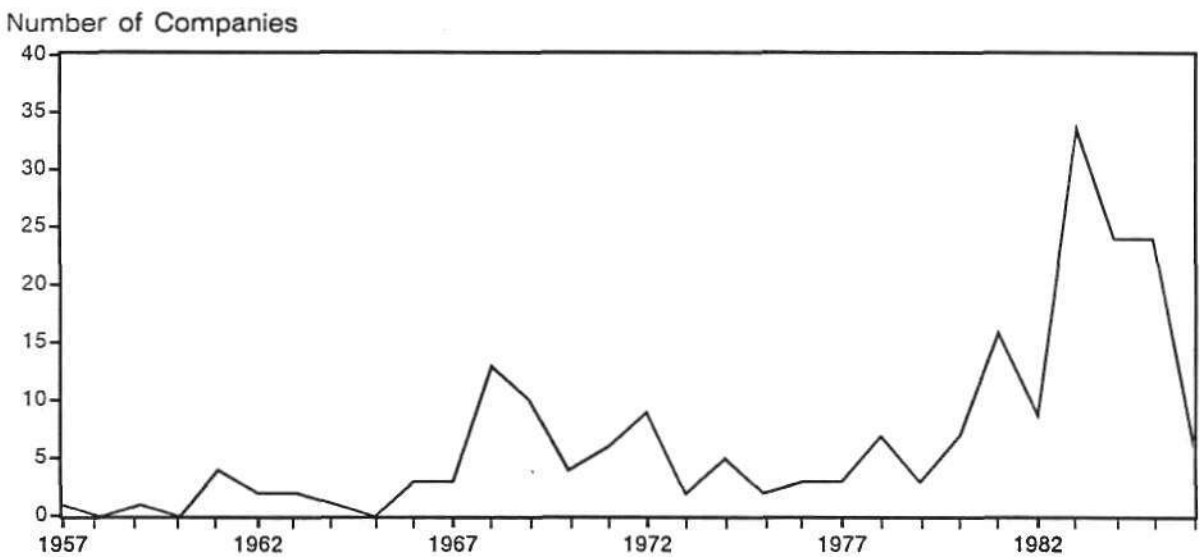
START-UP COMPANIES EXPANDING

This newsletter is the first in a series of quarterly updates on recent activities of start-up semiconductor companies. This information supplements I.C. Start-Ups 1987, a new Dataquest directory of semiconductor start-ups, which was published in October 1986. The newsletters will include information on new companies formed, initial and additional rounds of financing, significant company announcements, and new alliances.

Figure 1 illustrates the activity in company formation between 1957 and 1986.

Figure 1

FORMATION OF COMPANIES
1957-1986



Source: Dataquest
May 1987

MAJOR DEVELOPMENTS

Start-up activity continues at a strong pace. Seven companies, formed in 1986, have emerged. Dataquest expects the number to grow as companies raise initial financing and complete their initial product offerings.

We have noted also that many of the start-ups are experiencing extraordinary growth. In 1986, Cypress Semiconductor approximately tripled its sales from $18 million in 1985; Samsung and UMC doubled their sales from $95 million and $33 million, respectively, in 1985. Many other companies increased revenue by 25, 30, or 50 percent.

Major developments for start-up companies include the following:

- Start-up companies have attracted $73.6 million in additional financing since the publishing of I.C. Start-Ups 1987 in October 1986.
- VLSI Technology acquired Visic, Inc.; Custom MOS Arrays and its sister company, California Micro Devices, merged activities.
- Start-ups have expanded with the formation of subsidiaries in Asia and additional manufacturing facilities in the United States and Europe.
- Several start-ups have also announced reorganizations and changes of presidents and CEOs, indicating business expansion.
- Many new alliances have been formed, involving a total of 33 companies.

Table 1 lists the semiconductor companies formed in 1985 and 1986.

Table 1

START-UP COMPANIES

Companies Formed in 1986

Company	Location	Product
Gazelle Microcircuits	Sunnyvale, CA	GaAs digital
Graphics Communications	Japan	Graphics chips
Innovative Silicon Technology	Italy	ASICs
MemTech	Folsom, CA	Bubble memory
Solid State Technologies	San Jose, CA	Bipolar memory
Taiwan Semiconductor Mfg. Corp.	Taiwan	Foundry
Telcom Devices	Newbury Park, CA	GaAs opto

(Continued)

Table 1 (Continued)

START-UP COMPANIES

Companies Formed in 1985

Company	Location	Product
ABM Semiconductor, Inc.	San Jose, CA	AlGaAs Opto
ACTEL Corporation	Sunnyvale, CA	ASICs
Acumos, Inc.	San Jose, CA	CMOS ASICs
Advanced Linear Devices	Sunnyvale, CA	Linear
American Information Technology	Cupertino, CA	MPUs
Anadigics, Inc.	Warren, NJ	GAas A/D converters
BT&D Technologies, Inc.	United Kingdom	Optoelectronics
Catalyst Semiconductor	Santa Clara, CA	Memory
Chips & Technologies	Milpitas, CA	Micros
Dolphin Integration	Europe	ASICs
European Silicon Structures	West Germany	ASICs
GAIN Electronics	Somerville, NJ	GaAs
Hittite Microwave Corp.	Massachusetts	GaAs
Intercept Microelectronics	San Jose, CA	ASICs
Level One Communications	Folsom, CA	Linear
Orbit Semiconductor	Sunnyvale, CA	Foundry
Sahni Corporation	Sunnyvale, CA	Closed (1986)
Saratoga Semiconductor	Cupertino, CA	Memory
Spectrum Semiconductor	Canada	ASICs
III-V Semiconductor	Arizona	GaAs
Tachonics Corporation	Bethpage, NY	GaAs
Topaz Semiconductor	San Jose, CA	DMOS ICs
Triad Semiconductor Intl.	Colorado	Memory
Wolfson Microelectronics	United Kingdom	ASICs

Source: Dataquest
May 1987

NEW COMPANIES

American Information Technology

American Information Technology (AIT), a start-up company in Cupertino, California, was formed in 1985. AIT has recently raised additional financing, is in its development stage, and will be releasing information on its activities later this year.

Gazelle Microcircuits, Inc.

Gazelle was founded in the summer of 1986 by ex-GigaBit Logic executives Andy Graham and David McMillan. In January 1987, Jerry Crowley, vice chairman and founder of Oki Semiconductor, left Oki to head the start-up. Gazelle is located in Sunnyvale, California, and was recently financed by Hambrecht & Quist and Kleiner, Perkins, Caufield & Byers. The company also has floated 900,000 shares of preferred stock at $1 a share and currently is putting together another round of financing. Gazelle will concentrate on very high speed digital ICs for military, telecommunications, and EDP applications.

Graphics Communications Technology

Ascii Inc., a Japanese software house, established a graphics start-up called Graphics Communications. Graphics Communications will be 70 percent financed by the joint MITI/MPT (Ministry of Posts & Telecommunications) Key Technology Research Promotion Center and 30 percent by 11 companies, including Iwasaki Communications, Mitsui Corporation, and Okura Electric. Ascii will maintain a 5 percent share in the venture, which will be headed by Ascii vice president, Kazuhiko Nishi.

Innovative Silicon Technology

Innovative Silicon Technology (IST) is a spin-off of SGS that was formed in May 1986 and is headed by Piero Martinotti and others from Motorola. SGS transferred the assets of its ASIC activities to IST, which will use a 1.5-micron, double-layer metal and direct-write on E-beam. It is providing gate arrays in one and one-half weeks and standard cells in two weeks. IST is planning a new R&D facility, fab, and operations, separate from SGS, that will be located northeast of Milan, Italy. Products are expected in 1987.

MemTech

MemTech was formed to acquire Intel's bubble memory operation. In February 1987, Intel signed the final purchase agreement covering the sale of Intel's magnetics operation to MemTech. The final sale terms provide for the transfer of Intel bubble memory manufacturing and test

equipment, inventory, product designs, personnel, and manufacturing and quality specifications to MemTech for an undisclosed price. Operations will remain in Folsom, California.

MemTech is affiliated with Helix Systems & Development, Canoga Park, California, a bubble memory systems manufacturer. MemTech is headed by Richard H. Loeffler, formerly chairman and chief executive of Helix, and William H. Almond, the former head of Eaton's microlithography division. MemTech offers a complete bubble memory product line that includes 1- and 4-megabit bubble memory components and support circuitry, bubble memory boards, subsystems, and a cassette product, all available in a variety of temperature ranges.

Solid State Technologies

Solid State Technologies is a 1986 start-up located in San Jose, California. The company was founded by George W. Brown, presently serving as president, and Marshall Wilder, vice president of operations, both from Advanced Micro Devices. Initially, Solid State Technologies plans to offer high-performance bipolar memory products. It is presently in its developmental stage and will be releasing more information in a few months.

Taiwan Semiconductor Manufacturing Corp.

Taiwan Semiconductor Manufacturing Corp. (TSMC) has been set up as a foundry operation that will produce a wide variety of ICs. Taiwan's Executive Yuan, or legislature, has earmarked monies from its Development Fund for a 48 percent stake in the new company. N.V. Philips will take a 27.5 percent share in the $150 million investment in TSMC.

Chips are now being produced at the company's initial fab, which is capable of producing 10,000 6-inch wafers per month. In the second phase, which will be completed in 1988, it will be able to produce 30,000 1.5-micron, 6-inch wafers per month.

Telcom Devices Corp.

Telcom Devices was formed in early 1986 to offer indium gallium arsenide (InGaAs) photodiodes and indium gallium phosphide (InGaP) light-emitting diodes. Telcom Devices is a subsidiary of Opto Diode Corp. (ODC) and is operating from ODC's facilities in Newbury Park, California. The two companies share clean room and manufacturing space. Larry Perillo, formerly with Rockwell, is director of optoelectronics materials. Telcom Devices started volume production of its first product in May 1986, an InGaAs PIN photodiode for fiber-optic applications.

FINANCING

Table 2 lists by company the funding raised in the fourth quarter of 1986 and the first quarter of 1987.

Table 2

ADDITIONAL START-UP FINANCING

Company	Date	Round	Amount	Sources
Anadigics Inc.	Nov. 1986	2	$10.0M	Century IV Fund; Englehard Corp.; Memorial Drive Fund; Metropolitan Life Insurance Co.
California Devices Inc.	Oct. 1986	3	$ 3.9M	Alan Patricof Assoc.; Partners; Brentwood Assoc.; Dougery, Jones & Wilder; Edelson Technology; Hook Partners; InnoVen Group; John Hancock Ventures; Lambda Fund; Merrill Lynch Venture; Oxford Partners; J.F. Shea & Co.; Xerox
Cirrus Logic Inc.	Nov. 1986	3	$ 4.5M	Brentwood Assoc.; Institutional Venture Partners; Kuwait & Middle East Financial; Nazem & Co.; New Enterprises Assoc.; NY Life Insurance; Robertson, Colman & Stephens; Technology Venture
Elantec Inc.	Dec. 1986	4	$ 7.8M	Harvard Mgmt.; Cypress Fund; Morgan-Holland; New England Capital; Riksa Trust; Sequoia Capital; St. James Venture Capital Fund; U.S. Venture Partners; CEI; and others
European Silicon Systems	Nov. 1986	Equity	$ 9.0M	Banque International a Luxembourg; European Investment Bank
Krysalis Corp.	Dec. 1986	1	$ 3.0M	Columbine; Crosspoint Venture Partners; Meadows Resources; OSCCO Ventures
Laserpath Corp.	Dec. 1986	2	$ 4.5M	Crosspoint Venture Partners; Emerging Growth Partners; GE Venture Capital; Wolfensen Assoc.

(Continued)

Table 2 (Continued)

ADDITIONAL START-UP FINANCING

Company	Date	Round	Amount	Sources
Performance Semiconductor Inc.	Nov. 1986	1	$10.0M	Advanced Technology Ventures; Albion Venture Fund; Asset Mgmt.; Brentwood Assoc.; DSV Partners; Harvard Mgmt.; IAI Venture Partners; North Star Ventures; Northwest Venture Capital; Reynolds Creek Ltd. Partnership; L.F. Rothschild, Unterberg Towbin; Taylor & Turner; U.S. Venture Partners; VenWest Partners
Seeq Technology Inc.	Oct. 1986	Private placement post IPO	$ 6.0M	Bridge Capital; GE Venture Capital; Hillman Ventures; John Hancock; Kleiner, Perkins, Caufield & Byers
Sensym Inc.	Aug. 1986	3	$ 1.5M	Becton & Dickinson
Vitesse Electronics Corp.	Feb. 1987	2	$10.0M	Sequoia Capital and others
Xilinx Inc.	Jan. 1987	3	$ 3.4M	Fleming Ventures Ltd.; Hambrecht & Quist; Kleiner, Perkins, Caufield & Byers; Interfirst Venture; Interwest Partners; Matrix Partners; Morgan Stanley; Rainier Venture Partners; Security Pacific Venture Capital; J. H. Whitney

Source: Dataquest
May 1987

COMPANY ANNOUNCEMENTS

Acrian Inc.

Acrian Inc. has named Gary Irvine president and chief operating officer. Jack Harris remains as chairman and chief executive. Mr. Irvine, formerly president of EH Electronics, will be responsible for new products and market expansion as well as possible acquisitions by the company.

Adaptec, Inc.

Adaptec announced plans to open a subsidiary in Singapore in the first quarter of 1987 to manufacture surface mount controllers. The new company, called Adaptec Manufacturing (Singapore) Private Ltd., plans to begin pilot production in April and full production in early summer.

Altera Corporation

Altera entered the military market with its EPLDs, offering the first products to meet Class B specifications of MIL-STD-883 Rev. C--the EP310 and EP1210.

California Devices Inc.

Douglas Ritchie has been elected chairman of the board of CDI in addition to his responsibilities as president and chief executive officer. Wilmer R. Bottoms, the former chairman, has been named vice chairman.

Custom MOS Arrays

Custom MOS Arrays has merged with California Micro Devices (CMD). CMD was incorporated in 1980 to acquire the assets of a thin-film company. No changes in personnel assignments are planned. Handel Jones, formerly president of Custom MOS Arrays, will be the president and chief operating officer of the new combined company.

Cypress Semiconductor Corporation

Cypress announced that it will file a registration statement with the SEC to offer 4,400,000 shares of common stock. The proceeds will be used as working capital and to increase its capital base.

Harris Microwave Semiconductor

Harris Microwave Semiconductor has transferred its CAE tools developed for CMOS digital ASICs in Melbourne, Florida, to its GaAs operation in Milpitas, California. The company has set up a commercial GaAs standard cell operation.

Integrated Device Technology Inc.

Leonard C. Perham, former vice president and general manager of IDT's SRAM Division, has assumed the duties of president and chief operating officer of Integrated Device Technology Inc. John Carey remains as chief executive officer and chairman of the board.

International Microelectronic Products Inc.

Barry Carrington, president, has been promoted to chief executive officer from chief operating officer. Mr. Carrington succeeds George W. Gray, who remains IMP's chairman.

Krysalis Corporation

Franc R.J. deWeeger has joined Krysalis as president and chief executive officer. Joseph T. Evans, who was a Krysalis cofounder and served as the company's president, now becomes vice president of research and engineering. Mr. deWeeger was previously at ASM International, where he served as president since 1984; he remains on the ASM America board of directors. Before that, he spent two years as president of Zilog, Inc.

Lattice Semiconductor Corporation

Lattice announced that Rahul Sud resigned as president and Jay McBride resigned as general manager. C. Norman Winningstad, chairman of the board, is acting CEO. Lattice also announced that Rahul Sud, Jay McBride, S. Robert Breitbarth, and Kishan C. Sud resigned from Lattice's board of directors.

Linear Technology Corporation

LTC has established a Japanese company to strengthen its services to its Japanese customers. The company is called Linear Technology K.K. and is wholly subscribed by the U.S. parent. Robert Swanson has been appointed president, and Atsushi Nakata has been appointed general manager.

LSI Logic Corporation

LSI Logic has reorganized into four strategic business units with separate profit and loss responsibilities. The four units and vice presidents heading them are: Components and Technology, Cy Hannon; Engineering Services, Ven Lee; Software and Computer Services, Jim Koford; and Military/Aerospace, Norm Chanoski. Each of the four vice presidents will report to George Wells; each unit will be supported by decentralized sales, marketing, purchasing, finance, and MIS staff.

LSI Logic also plans to offer part of its European affiliate, LSI Logic Europe, on London's second-tier Unlisted Securities Market (USM). More than 80 percent is owned by the parent company, with the remainder held by local private investors, insurance companies, and other financial interests. The most visible industrial investor in LSI Logic Europe is Sulzer Brothers AG, a Swiss engineering firm.

In West Germany, LSI Logic Europe is building a mass production assembly and test facility in Braunschweig, which will form part of the corporation's worldwide capacity. It should be operational later this year, acting as a subcontractor to the U.S. parent company.

Micron Technology, Inc.

Micron has placed approximately 3,500,000 shares of common stock with certain foreign institutional investors at a price of $4.375 per share in a private placement assisted by Montgomery Securities.

Samsung Semiconductor Inc.

Samsung announced that it is building a new facility in San Jose, California, which will house its headquarters, R&D operations, and research fab. Included in the new 80,000-square-foot facility will be a 12,000-square-foot fab equipped with 6-inch wafer processing equipment.

Seeq Technology Inc.

Monolithic Memories Inc. purchased a 16 percent equity in Seeq Technology for $4 million. The two companies also have agreed to a four-year joint product and technology program to develop CMOS PLDs. Seeq received MIL-STD-883 Rev. C Class B specifications for its products.

Sierra Semiconductor Corporation

Sierra Semiconductor announced Stephen Forte as president of its new European joint venture, Sierra Semiconductor B.V., formed in June 1986 in the Netherlands.

Silicon Systems Inc.

Stephen E. Cooper, formerly senior vice president and general manager of the Microperipheral Division of Silicon Systems, succeeds Carmelo J. Santoro as president and chief operating officer. Mr. Santoro remains as chairman and chief executive officer.

Telmos Inc., Universal Semiconductor Inc., and Zytrex

Investment Management International Inc. (IMI), the finance group that acquired Zytrex last spring, has acquired Universal Semiconductor and the assets and product rights of Telmos Inc.

Vitesse Electronics Corp.

The Vitesse Electronics' Integrated Circuit Division raised $10 million and is now an independent company, called Vitesse Semiconductor Corporation. Dr. Louis R. Tomasetta, former president of the IC Division, is president and CEO of the new company. Vitesse Semiconductor will remain in the 70,000-square-foot existing facility and will use the new funding to develop additional products and expand into higher-volume production.

VLSI Technology, Inc.

VLSI Technology's Government Products Division in Phoenix, Arizona, has been certified for production of devices that are fully compliant with MIL-STD-883C.

VLSI Technology completed the acquisition of Visic, Inc. Visic will maintain its own board of directors, which will include members of both Visic and VLSI Technology. Products designed and developed by Visic will be manufactured in the VLSI Technology facility and marketed under the VLSI name.

VLSI Technology's ASIC operation is now a separate division, joining the memory, logic, and government divisions. Former vice president of design and technology, Douglas G. Fairbairn, has been promoted to the new position of vice president and general manager of the new ASIC Division. He will continue to report to both chairman Alex Stein and president Henri Jarrat.

Xicor, Inc.

Xicor announced that it has completed MIL-STD-883C Class B qualification for its X28256 EEPROM device. This qualification affects all versions of the X28256 in the 32-pad leadless chip carriers.

Table 3 lists some recent alliances involving start-up companies.

Mark Reagan
Michael Boss

Table 3

ALLIANCES INVOLVING START-UP COMPANIES

Company	Date	Comments
Altera WaferScale Sharp	Jan. 1987	Altera and WSI agreed to a 5-year technology exchange to develop new user-configurable logic products; Sharp will manufacture the products using WSI's process.
Chips Ascii Corp.	Sept. 1986	Chips & Technologies and Ascii, a major software company in Japan, will start a new company to develop communication products. Chips will design the products; manufacturing will be done by companies in Japan. Chips and Ascii will hold equal shares of the majority interest in the new venture.
Chips NSC	Nov. 1986	National Semiconductor will second source Chips & Technologies CMOS ICs in exchange for fabrication services. National is Chips' first U.S. source.
Cirrus Logic Silicon Systems	Oct. 1986	Cirrus Logic and Silicon Systems will exchange controller and buffer manager functions and mutually second source the ASICs. Both chips will be processed in 2-micron CMOS.
Crystal Asahi Chemical	Jan. 1987	Asahi Chemical acquired an 8 percent share in Crystal Semiconductor for about $4 million. Asahi will provide foundry services in exchange for a license to all of Crystal's existing products and to be its principal distributor in the Far East. Both companies will develop new products.
Custom Silicon NCR	Feb. 1987	NCR has licensed CSi's standard cell library, including 342 TTL macrocells and microcomputer building blocks of up to 5,863 gates. CSi's library was built from NCR's existing library, which CSi licensed.
ES2 N.V. Philips TI	Feb. 1987	Texas Instruments Ltd. of England and Philips International N.V. will offer accelerated prototyping for the SystemCell Library of standard cells in cooperation with ES2. The SystemCell Library is the result of a collaborative relationship between TI and Philips who provide high volume manufacturing and standard prototyping.

(Continued)

Table 3 (Continued)

ALLIANCES INVOLVING START-UP COMPANIES

Company	Date	Comments
ICT Asahi Chemical	Jan. 1987	Asahi Chemical Industry will receive technology from ICT (International CMOS Technology) and will also market its EEPROMs.
IDT VTC, Inc.	Jan. 1987	VTC will second source Integrated Device Technology's FCT product line of TTL-compatible CMOS logic devices.
iLSi Sumitomo Corp.	Dec. 1986	Sumitomo licensed ASIC design technology from Integrated Logic Systems Inc. (iLSi); in addition to royalty payments, iLSi has gained rights to use any foundries Sumitomo uses.
IMP Micro Linear MBB	Aug. 1986	International Microelectronic Products and Micro Linear have agreed to transfer ASIC design know-how to Messerschmitt-Bolkow-Blohm GmbH over a three-year period.
Lattice SGS	Feb. 1987	Lattice Semiconductor signed a technology agreement with SGS Semiconductor, giving SGS a license to second source Lattice's GAL products. SGS will manufacture GAL products for Lattice, and both companies will cooperate on the design of future PLD products.
Seeq MMI	Nov. 1986	Monolithic Memories purchased a 16 percent equity in Seeq for $4 million. The companies also agreed to a 4-year joint product and technology program to develop CMOS PLDs.
Seeq Motorola	Dec. 1986	Seeq and Motorola agreed to work on a multimillion-dollar EEPROM technology project.
XTAR Fairchild	Sept. 1986	Fairchild agreed to second source XTAR's 2-chip set graphic MPU.

Source: Dataquest
May 1987

Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987-1988 Newsletters, May
1987-11

A WORLDWIDE IC PACKAGING UPDATE

OVERVIEW

The normal state of affairs in the semiconductor industry is to be in a "state of transition" or to have "reached a milestone." Or, something has occurred that will "revolutionize" the industry. Packaging of semiconductors is no exception.

Significant achievements in VLSI fabrication and design technologies have reached the point where concurrent improvements in die-level interconnection technologies are necessary for continued system performance. Of all the packaging and interconnection technology issues discussed, one issue readily agreed upon is that both users and suppliers of semiconductors are going through a demanding transitional phase of component packaging decisions--decisions that will have to be dealt with in the near future, as the industry approaches submicron geometries.

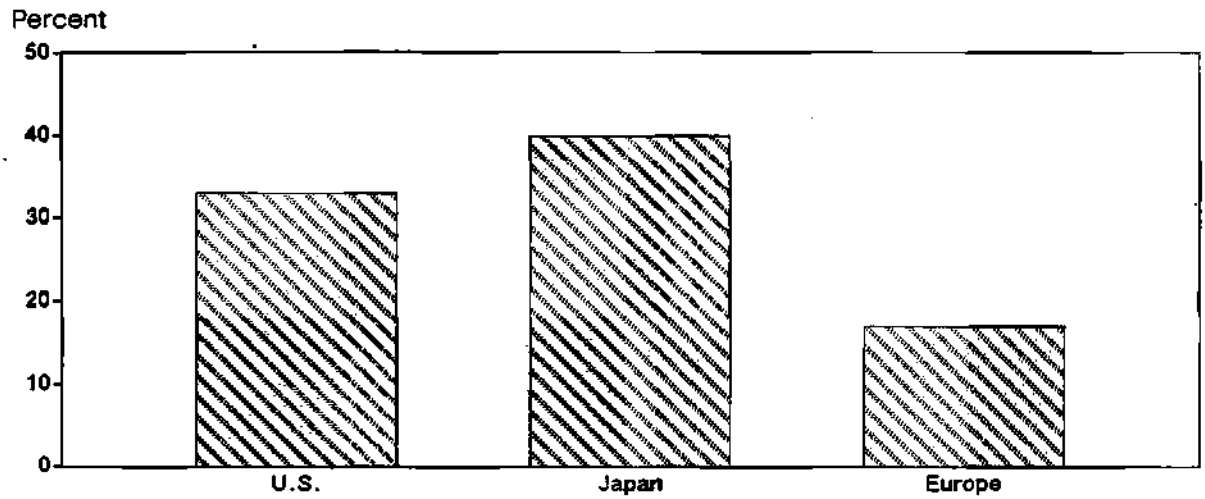
One very clear trend that we are seeing is that equipment manufacturers are using more and more VLSI devices. There is a sweeping desire to reduce space and cost through more condensed packaging and to automate as much as possible. To accomplish this, packaging technology must approach chip technology.

PACKAGE CONSUMPTION

Figure 1 shows the estimated worldwide integrated circuit (IC) package consumption for 1986. The estimates are based on Dataquest's worldwide IC consumption data and therefore show consumption by all packaged ICs. Japan captured 40 percent of packaged ICs in 1986, while U.S. market share dropped to approximately 33 percent and Europe came in at 17 percent. The remaining 10 percent not shown went to ROW.

Figure 1

ESTIMATED 1986 WORLDWIDE PACKAGING TRENDS
(Units)



Source: Dataquest
May 1987

We expect that the Japanese will maintain their lead in the 1988 market using 44 percent of packaged ICs, with the United States holding approximately 38 percent, and Europe with 18 percent. By 1991, we anticipate that Japan will strengthen its lead to 45 percent, by virtue of its majority share of the consumer business, concerted efforts in the industrial sector, and its lead in automated assembly. At this point, U.S. market share will drop to 34 percent, and Europe's share will climb to 21 percent. While Europe is obviously not defeating its American and Asian competitors, we do expect it to modestly regain market share. At this time, we believe that European users are changing to surface-mount technology more readily than the American and Japanese users. Telecommunications and IC smart card applications, focusing on small-outline (SO) and tape-automated bonding (TAB) will provide Europe with the biggest growth opportunities for the next 10 years.

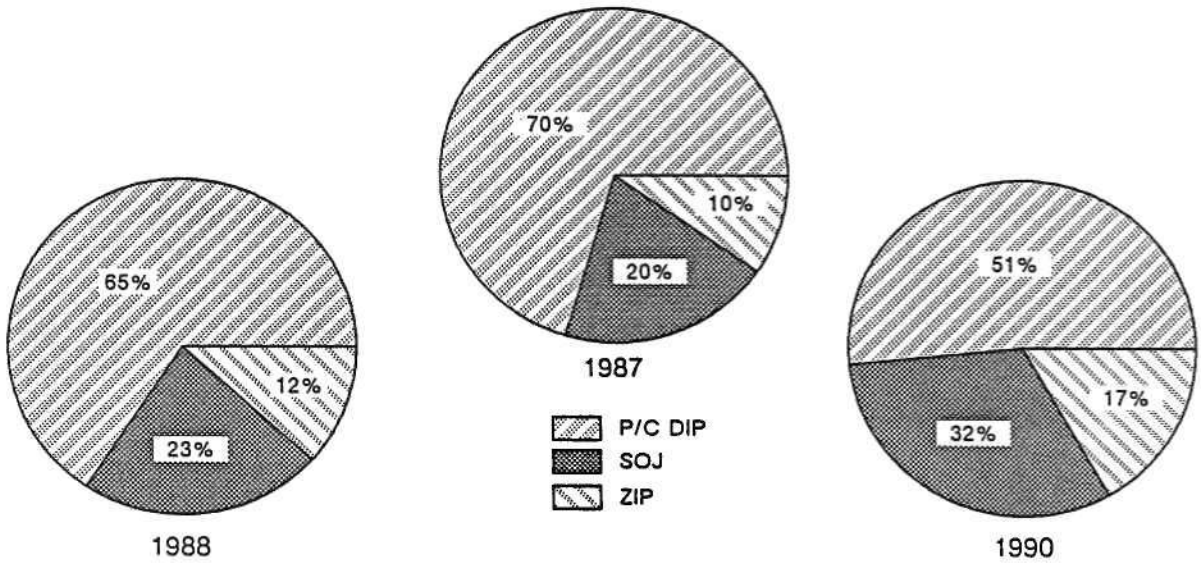
THE MEMORY ROLE

Over the last few years, memory devices have been on the leading edge of packaging technology due to density requirements. We have forecast that approximately 55 million 1 Mbit DRAMs will be shipped worldwide in 1987. As shown in Figure 2, 70 percent of those units will be shipped in either plastic or ceramic dual in-line packages (DIPs). By 1988, DIP package usage for DRAMs will shrink to 65 percent, while zig-zag in-line package (ZIP) and small-outline J-lead (SOJ) usage will grow. As we move into the 1990s, the SOJ package is expected to grow to 32 percent. High-density device

architectures, led by smaller geometries and line widths, coupled with the desire to bring down costs while maintaining price competitiveness and building better and faster machines, will require the increased use of surface-mount technology (SMT).

Figure 2

ESTIMATED 1Mb DRAM PACKAGES



Source: Dataquest
May 1987

SMT ISSUES

Despite the many advantages, implementation of surface-mount (SM) packages into systems manufacturing is taking longer than anticipated. Surface-mount technology is still immature and as such the manufacturing infrastructure is not fully developed. Preferring the tested reliability of through-hole (TH) packages, users continue to mix SM/TH designs. Reliability of SM devices has not yet been proven and solder joint inspection is difficult. However, as shown on Table 1, concentrated use of SM devices is occurring in applications where small size and weight are the primary issues. As shown on Table 2, computers were the leading end-use segment for SMDs in the United States, in 1986. While cost reduction was the driving force, reliability continues to play a major role in acceptance of SMT. Europe led the United States in acceptance and usage of SMT in telecom applications; and by virtue of its command over the consumer market, Japan led the market with 10 percent of ICs packaged in SMT. As a comparison, Japan's Printed Circuit Association (JPCA) estimated that SM consumption in Japan reached 13 percent for ICs, and that over the next five years, ICs in SMT will grow to 33.9 percent in Japan.

Table 1

SURFACE-MOUNT TECHNOLOGY

Where?

- Consumer
- Automotive
- Disk storage
- Avionics, missiles, and space
- High-density memories
- Power supplies

Source: Dataquest
May 1987

Table 2

SURFACE-MOUNT TECHNOLOGY
END-USE SEGMENTS
1986

	Japan	Europe	United States
End Use	Consumer	Telecommunications	Computers
Driving Force	Small size	Reliability	Cost reduction/ reliability
Percent of ICs Consumed Worldwide	40%	17.7%	32.8%
Percent of ICs in SMT	10%	8.0%	4.0%
Dominant SMT Approach	TAB/QUAD/SO	SO	SO/CC/TAB

Source: Dataquest
May 1987

SUMMARY

At the present time, we believe that there is no single solution to future VLSI packaging problems. For the 1990s and beyond, we expect that package designs will continue to proliferate. Advanced multichip product designs will incorporate ASICs, use advanced circuit design techniques, and use advanced board assembly methods incorporating TAB and other multichip packages. While plastic packaging has its hermetic limitations, its high-volume, low-cost, high-performance, 40 pin-and-below characteristics will make it the dominant package by 1990.

Automated assembly will change the way that ICs and other components are packaged. TAB or some variation of this method of construction is the most likely packaging style for ICs in the 1990s. Chip-on-board (COB) has also made its way up the automated assembly ladder in consumer applications. From early single-chip digital watch applications, it is now being used in multi-chip applications such as copiers, facsimile, and IC cards.

REGIONAL ANALYSIS

If we use the premise that memory devices have been on the leading edge of packaging technology due to density requirements, then we can assume that Japan has a two-year lead on the industry and will gain overall leadership in packaging technology before the 1990s. With its vertically integrated structure, Japan can maintain closer technical and strategic cooperation among members of its packaging chain. Their command over the consumer market and surface-mount approach has given them a lead in packaging technology. There are already major efforts among equipment suppliers in Japan to develop automated assembly processes.

Despite major engineering efforts dedicated to designs, substrate and component materials, and assembly equipment, cooperation lags among members of the packaging chain in the United States. At times, cooperation seems better between U.S./Japanese partners than between U.S./U.S. alliances. The strong financial/technical megacorporate links of Japan are nonexistent in the United States. Outside of Texas Instruments and a few systems groups, everyone else has transported assembly offshore. Unlike Europe and Japan, there is very little academic research and cooperation. There is some hope in U.S. research consortiums, but cooperative efforts in packaging are weak. Finally, except for a few systems houses, the fear of capital investments in automated assembly technology has paralyzed many companies into making the decision to automate, a decision that could prevent them from staying on the competitive edge.

Peggy Marie Wood
Mary A. Olsson

Dataquest
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Research Newsletter

SEMS Code: Newsletters 1987-1988
1987-10

A BLOATED INDUSTRY: JAPANESE SEMICONDUCTOR OVERCAPACITY CONTINUES

SUMMARY

Plant overcapacity continues to haunt the Japanese semiconductor industry. In 1986, Japanese semiconductor capital spending declined 63.1 percent in yen, and Dataquest believes that the industry will reduce spending another 11.3 percent in 1987. But several developments threaten to worsen an already bad situation in Japan:

- MITI's request for Japanese vendors to cut overall semiconductor production by 11 percent during the second quarter of 1987
- A huge inventory of 4.7 billion semiconductor units, consisting primarily of commodity devices
- Real prospects of a stronger yen, possibly reaching ¥130 to a U.S. dollar in 1987, which would cause a further weakening of the Japanese economy and semiconductor consumption
- Plans for new plants by major semiconductor users, such as the ¥45 billion ($300 million) Toyota Motors plant
- The shift to six-inch wafers, which requires fewer wafer starts to achieve comparable production levels

Given these trends, short-term prospects look bad for Japanese makers struggling with excess inventories and plant capacity. But there is a caveat to this overcapacity situation. Dataquest already observes spot shortages and lengthening lead times for surface-mounted 256K DRAMs. MITI-mandated production cutbacks may cause serious shortages later this year since Japanese vendors supply 80 percent of all 256K DRAMs and a higher portion of surface-mounted DRAMs. The irony is that Japanese semiconductor makers have excess capacity--but on the wrong side of the Pacific ocean.

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 971-9000, Telex 171973

JAPANESE CAPITAL SPENDING DOWN SHARPLY

Since the early 1980s, Japanese semiconductor makers have invested heavily in new plant and equipment. Japanese capital spending grew at a compound annual growth rate (CAGR) of 65.2 percent between 1981 and 1984, then dropped sharply in 1985. As shown in Table 1, cumulative spending during the last five years totaled ¥2.6 trillion ($15.3 billion), leading to the current overcapacity situation. Although top makers accounted for the largest investments, spending was up sharply at Sony (26.2 percent CAGR), Rohm (32.0 percent), Shindengen (24.6 percent), and New Japan Radio (20.1 percent).

As the market turned soft, Japanese makers reduced their capital spending by 6.5 percent in 1985, followed by a sharp cutback of 62.7 percent in 1986. However, excess capacity still remains. In 1987, Dataquest forecasts another 11.3 percent decline in capital spending to ¥260 billion ($1.8 billion).

Table 1

ESTIMATED JAPANESE CAPITAL SPENDING
(Billions of Yen)

Company	1982	1983	1984	1985	1986	1982-1986 Cumulative	5 Year CAGR %
Fuji Electric	¥ 4	¥ 6	¥ 12	¥ 12	¥ 5	¥ 39	4.6%
Fujitsu	35	53	115	72	16	291	(14.5%)
Hitachi	36	62	120	92	22	332	(9.4%)
Japanese Semiconductor	0	0	0	0	5	5	N/A
Matsushita	9	21	88	87	24	229	21.7%
Mitsubishi	20	31	65	62	20	198	0
NEC	42	58	129	123	30	382	(6.5%)
NJRC	2	2	4	5	5	18	20.1%
NMB	0	0	14	14	0	28	N/A
Oki	11	11	26	26	10	84	(1.9%)
Rohm	2	3	6	9	8	28	32.0%
Sanken	2	3	6	6	4	21	14.9%
Sanyo	10	12	32	47	18	119	12.5%
Sharp	8	16	26	36	22	108	22.4%
Shindengen	1	1	3	3	3	11	24.6%
Seiko Epson	5	9	18	8	5	45	0
Sony	5	9	14	36	16	80	26.2%
Toshiba	28	86	136	123	65	438	18.3%
Other	9	16	34	32	15	106	10.8%
Total	¥229	¥399	¥848	¥793	¥293	¥2,562	5.1%
Exchange Rate* (Yen Per Dollar)	248	235	237	238	167		

*To convert to U.S. dollar basis.
N/A = Not Applicable

Source: Dataquest
May 1987

EXCESS INVENTORIES REMAIN HIGH

Due to this massive investment, Japanese semiconductor makers ramped up production rapidly, which led to large inventory buildups from early 1984. As shown in Table 2, inventories doubled from 1.6 billion units to 3.2 billion units in 1984, then increased another 50 percent in 1985 to 4.8 billion units. In 1986, excess inventories dipped only slightly. This situation--overcapacity, excess inventories, and a stagnant market--led to severe pricing pressures and strong trade friction with the U.S. makers over dumping.

Dataquest believes Japanese semiconductor makers will continue to face serious excess inventory and overcapacity problems in 1987. Because makers reduced overall inventories by only 0.1 billion units last year, total inventories remain at 4.7 billion units--nearly an historic high. To further reduce inventories, MITI has ordered an 11 percent production cutback in the second quarter of 1987 due to U.S. government pressure.

Table 2

JAPANESE SEMICONDUCTOR PRODUCTION, SHIPMENTS, AND INVENTORY
(Billions of Units)

	Q1	Q2	Q3	Q4	1984
Production	11.4	12.5	13.7	14.0	51.6
Shipments	10.9	12.4	13.5	13.1	50.0
Open Inventory	1.6	2.1	2.1	2.4	1.6
End Inventory	2.1	2.1	2.4	3.2	3.2
	Q1	**Q2**	**Q3**	**Q4**	**1985**
Production	12.2	12.6	12.4	11.4	48.6
Shipments	11.5	12.1	12.3	11.1	47.0
Open Inventory	3.2	3.9	4.4	4.5	3.2
End Inventory	3.8	4.4	4.5	4.8	4.8
	Q1	**Q2**	**Q3**	**Q4**	**1986**
Production	12.3	14.2	13.9	13.9	54.3
Shipments	12.3	14.3	13.9	13.9	54.4
Open Inventory	4.8	4.7	4.7	4.7	4.8
End Inventory	4.8	4.7	4.7	4.7	4.7

Source: MITI
U.S. Department of Commerce
Dataquest
May 1987

AN EXCESS OF SIX-INCH WAFER FABS?

Given the need to reduce production, the decision of Japanese makers to proceed with new six-inch wafer fabs has led to significant short-term overcapacity. As shown in Table 3, Dataquest has recorded 23 six-inch fabs in Japan, primarily for memory and logic products. Several new gate-array fabs are now coming on line. We believe that many of these new plants are running at low utilization rates (below 50 percent capacity), being used for preproduction R&D, or sitting idle. MITI-enforced production cutbacks will worsen the situation in 1987.

Despite this overcapacity, several companies recently announced plans to build new six-inch wafer fabs, including major users such as Toyota Motors, which will invest ¥45 billion ($300 million) to produce ICs for car and truck engines. If pursued by other Japanese carmakers, these investments could seriously hurt Japanese semiconductor vendors.

Table 3

SIX-INCH WAFER FABS IN JAPAN

Company	Plant Name	Prefecture	Name of Fab Line	Products	Total Clean Room (Square Meter)	Technology	Year Production Began
Fuji Electric	Matsumoto	Nagano		MEM			1986
Fujitsu	Iwate	Iwate	No. 4, 5	MEM	5,630	MOS	1980
Fujitsu	Mie	Mie		MEM, Logic, Gate Array	161,376	MOS	1984
Hitachi Hokkai Semiconductor	Chitose	Hokkaido		MEM	20,000	MOS	1983
Hitachi	Kofu	Yamanashi	K4	MEM	43,435	MOS	1969
Hitachi	Mobara	Chiba	No. 3	MEM, Logic, MPU	10,000	CMOS	1985
Hitachi	Naka	Ibaragi		MEM	15,000	MOS	1985
Iwate Toshiba Elec.		Iwate		MEM	6,300	MOS	N/A
Kansai NEC	Ohtsu	Shiga		MEM, Logic	88,000	CMOS	1985
Kyushu NEC		Kumamoto	No. 6, 7	MEM, Logic, MPU	64,000	CMOS	1987
Matsushita Elec.	Oozu	Toyama	No. C	MEM, Logic, MPU	48,500	CMOS	1985
Mitsubishi	Kouchi	Kouchi		MPU	215,168	CMOS	1986
Mitsubishi	Saijo	Ehime		MEM	22,000	CMOS	1985
NEC	Sagamihara	Kanagawa	8 line	MEM, Gate Array	133,861	CMOS	1962
Ninon Semiconductor		Ibaragi		Gate Array	N/A	CMOS	1987
Nigata Sanyo Donshi		Nigata		MEM, NPU	32,500	CMOS	1986
Niyazaki Oki		Miyazaki	N3	MEM, Logic, Gate Array	30,800	CMOS	1980
Miyagi Oki		Miyagi		MEM	N/A	CMOS	1988
Ricoh		Osaka		MEM, MPU	7,300	CMOS	1981
Seiko Epson	Fujimi	Nagano		SRAM, Gate Array	42,000	CMOS	1983
Sharp	Fukuyama	Hiroshima		MEM, Gate Array	32,000	CMOS	1986
TI	Miho	Ibaragi		MEM	64,000	CMOS	1984
Toshiba Ohita		Ohita		MEM	90,000	DMOS	1987

N/A = Not Available

Source: Dataquest
May 1987

LARGER WAFERS REQUIRING FEWER WAFER STARTS

In addition to increasing capacity, Dataquest observes that six-inch wafers account for a growing share of Japanese wafer starts. As shown in Table 4, Dataquest estimates that six-inch wafers increased from 6.2 percent of all wafer starts in 1985 to 8.7 percent in 1986. It appears that Japanese makers are shifting from smaller wafers to 6-inch wafers, while maintaining 5-inch wafer production at a constant percentage level.

This shift to six-inch wafers has led to slower increases in wafer starts. As shown in Table 5, average monthly semiconductor production was up 11.6 percent in 1986, while monthly IC production increased 19.2 percent. But average monthly wafer starts increased only 11.2 percent. Dataquest believes that, despite sluggish market conditions, monthly wafer starts increased in 1986 because of lower yields for 6-inch wafers and the extensive use of wafers for R&D purposes.

Table 4

PERCENT OF MILLION WAFER STARTS

	1985	1986
2-inch	1.4%	1.2%
3-inch	12.3	11.1
4-inch	49.9	48.8
5-inch	30.2	30.2
6-inch	6.2	8.7
Total	100.0%	100.0%

Source: Dataquest
May 1987

Table 5

JAPANESE MONTHLY PRODUCTION AND WAFER STARTS

	Average Monthly Production (Millions of Units)			Average Monthly Wafer Starts (Thousands of Units)		
	1985	1986	Percent Growth	1985	1986	Percent Growth
Fujitsu	49.5	55.2	11.5%	196.5	223.3	13.5%
Hitachi	475.0	522.8	10.1%	344.8	388.2	12.6%
Matsushita	525.0	584.5	11.3%	262.4	263.1	0.3%
Mitsubishi	163.8	180.0	9.9%	274.2	319.4	16.5%
NEC	517.8	555.0	7.2%	368.6	424.7	15.2%
Oki	25.7	30.5	18.7%	118.6	146.5	23.5%
Sanyo	158.0	170.0	7.6%	130.8	147.7	12.9%
Sharp	28.2	33.0	17.0%	86.6	105.2	21.5%
Toshiba	631.6	704.6	11.6%	344.0	418.5	21.7%
Other	1,474.9	1,689.6	14.6%	805.5	824.1	2.3%
Total	4,049.5	4,525.2	11.7%	2,932.0	3,260.7	11.2%
Year-End Inventory	4,804.0	4,725.0	(1.6%)			
Shipments	3,948.8	4,567.5	15.7%			

Source: Dataquest
May 1987

DATAQUEST CONCLUSIONS

Despite sluggish market conditions, Dataquest believes that Japanese semiconductor makers are increasing production levels and wafer starts because of their heavy fixed capital investments. In 1986, Japanese makers exported 36.9 percent of all semiconductor devices to unload this excess production, resulting in serious trade friction with the United States and Europe.

In 1987, we believe that Japanese makers face even more serious challenges, including:

- MITI's request for an 11 percent cutback in production during the second quarter of 1987
- Growing U.S. congressional demands for a tougher trade policy, beginning with the proposed $300 million in U.S. tariffs on Japanese electronic imports, which will heat up with the approach of the 1988 presidential election
- The strengthening yen, which could reach a worst case of ¥130 to the dollar by the end of 1987, and a weakening domestic economy
- Foreign demands for increasing access to the Japanese market
- A growing surplus labor force due to the movement toward offshore manufacturing
- Increasing competition from Malaysia, Singapore, South Korea, and Taiwan

On the positive side, Dataquest forecasts a growth in Japanese electronic equipment production, especially for products such as digital audio disks (DAD) and page printers. But the strengthening yen and growing U.S. and European protectionism could easily weaken market demand. Whether Japanese semiconductor makers will be able to successfully overcome these obstacles will depend upon the flexibility and creativity of their research and management policies.

George Burns
Sheridan Tatsuno

Dataquest
a company of The Dun & Bradstreet Corporation

Research *Bulletin*

SEMS Code: 1987-1988 Newsletters: May 1987-9

A CLIMATE OF CONSOLIDATION: UNION CARBIDE ACQUIRES KODAK RESIST OPERATIONS

On Tuesday, May 5, Eastman Kodak announced the sale of its photoresist operations to Union Carbide Corporation. Dataquest views this acquisition as an important strategic move on the part of Union Carbide to strengthen its position as a major electronic materials supplier to the semiconductor industry. The sale of Kodak's resist operations to Union Carbide is one of the many examples of the mergers, acquisitions, and consolidation that currently characterize the business climate within the industry. This research bulletin details the acquisition, provides a brief overview of the semiconductor photoresist industry, discusses the sale of Kodak's resist operations in light of its impact on other resist companies, and concludes with a look at Union Carbide's position in the electronic materials market.

THE SALE OF KODAK'S RESIST OPERATIONS

With the acquisition of Kodak's photoresist operations, Union Carbide obtains the manufacture and sales of Kodak photoresist products, including both macro- and microresists and the ancillary products. Application markets for Kodak's macroresists include printed circuit boards, gravure cylinders, and chemical milling. Microresists are used in the semiconductor industry to transfer circuit patterns to wafers and photomasks. Current Kodak microresists include positive and negative optical resists, negative e-beam and negative X-ray resists. In addition to existing resist technology, Union Carbide has acquired Kodak's current research projects in advanced photoresist materials. This research includes product development in new deep-UV, e-beam, and X-ray resist materials.

The Kodak resist products will be customized, packaged, and distributed by KTI Chemicals, Inc., a wholly owned subsidiary of Union Carbide. This should not be viewed as a new avenue of business for KTI Chemicals--the company has been a major supplier of Kodak photoresist products for many years. KTI, however, does not have primary resist manufacturing capability within its organization. Although Union Carbide has been involved in some R&D aspects of photoresist development, Dataquest believes that the acquisition of Kodak's technology will substantially augment Union Carbide's existing programs. Photoresist manufacturing will occur at Union Carbide's plant in South Charleston, West Virginia, where its Chemicals and Plastics Group has its primary manufacturing facility.

Dataquest, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 971-9000, Telex 171973

SEMICONDUCTOR PHOTORESIST INDUSTRY OVERVIEW

Approximately thirty companies supply photoresist to the worldwide semiconductor industry for device fabrication and maskmaking applications. Resist product categories include positive and negative optical resists, deep-UV, e-beam, and X-ray resists. The majority of these photoresist companies have primary manufacturing capability; however, some vendors supply only reformulated resist products. Photoresist reformulators purchase bulk resist materials from other resist companies, formulate and custom blend the photoresist products according to individual customer specifications, and provide focused technical support and service to their customers. This type of service-oriented approach to materials distribution in the photoresist market was pioneered by KTI Chemicals in the mid-1970s. KTI currently provides reformulated resists based on products from AZ Photoresist, Eastman Kodak, Shipley Corporation, and Toray Industries of Japan.

ACQUISITION IMPACT ON OTHER SUPPLIERS

Eastman Kodak does not sell its microresists directly to semiconductor manufacturers, but instead has depended on reformulator companies to do so. In the United States, these companies are J.T. Baker, KTI Chemicals, and ROK Industries (Chemtech Microelectronic Chemicals Industries). Micro Image Technology supplies Kodak resists to the European semiconductor community while Nagase Chemicals, Eastman Kodak's exclusive distributor in Japan, supplies Kodak microresists in that country. Dataquest believes that, of these five companies, KTI is the largest supplier of Kodak microresists.

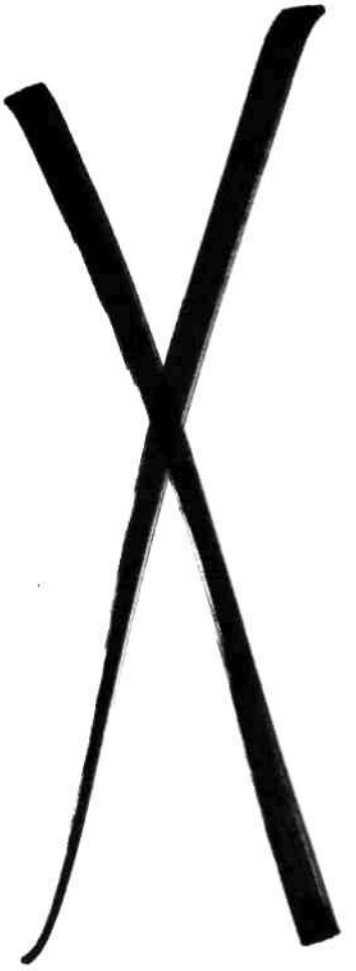
What Now?

Union Carbide and KTI Chemicals have planned in the short term to continue to honor existing supplier/distributor relationships with the other microresist reformulator companies. Long-term continuation of such relationships will be under evaluation during the next few months. Dataquest, however, expects that the Kodak microresist supplier relationship with other reformulator companies will be severed since KTI Chemicals is a direct competitor with these companies in the photoresist market place.

CONCLUSION

Union Carbide was a logical suitor for Kodak's resist operations. Through its subsidiary, KTI Chemicals, Union Carbide already has an established photoresist distribution network as well as years of experience with the Kodak resist line. The acquisition of Kodak's resist operations provides Union Carbide with a strong base of primary manufacturing technology for photoresist, a factor that Dataquest believes is essential for establishing a significant market-share position in this electronic materials segment. The strengthening of Union Carbide's photoresist operations enhances the company's position overall as a major worldwide supplier of electronic materials to the semiconductor industry. In addition to photoresist, Union Carbide has extensive operations in polysilicon as well as in bulk and specialty semiconductor gases. Dataquest views the acquisition of Eastman Kodak's resist operations by Union Carbide as another example of the continuing process of consolidation within a maturing semiconductor industry.

Peggy Marie Wood



June Newsletters

The following is a list of newsletters found in this section:

- SEMICON/West 1987 Equipment Survey
  1987-15

Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987-1988 Newsletters, June 1987-15

SEMICON/West 1987 EQUIPMENT SURVEY

The SEMICON/West Equipment and Materials Exposition is held annually in San Mateo, California. This industry trade show is sponsored by the Semiconductor Equipment and Materials Institute and is a yearly milestone for the semiconductor equipment and materials vendors. Each year, Dataquest surveys the wafer fabrication equipment vendors and reports on significant new products and enhancements introduced at the show. The results of the survey are published in this annual newsletter.

INTRODUCTION

While many exhibitors seemed to think that attendance was low, there were actually more than 45,000 attendees at this year's show, compared with 50,000 last year. One reason that attendance seemed low is that the show was spread over four days instead of three days as in the past. There were 1,035 companies at the show, compared with 1,061 in 1986.

The last two years have been tough for the equipment and materials vendors as they have seen orders and shipments slide to very low levels compared with the boom year of 1984. Everyone is anxiously awaiting an upturn, which has definitely occurred in the semiconductor industry, but because of the world's excess semiconductor manufacturing capacity, has not yet manifested itself in the equipment and materials industry.

However, Dataquest believes that the long slide down in the equipment and materials industry has been halted and that the industry has, indeed, turned the corner. Many vendors at the show told Dataquest that orders have increased recently, and interestingly, they uniformly reported that their orders have picked up within the same time span--six to eight weeks prior to the show. A leading indicator for the equipment industry is assembly equipment. Since this equipment segment is largely driven by capacity, it is

the first to feel the downturn when there is excess capacity and is a good barometer when the semiconductor industry begins to need additional capacity. Therefore, it is welcome news that some assembly equipment vendors are reporting that orders are finally on the increase after a two-year dearth.

SEMICON/West is a key event for vendors to introduce new products, and it is a time to view the collective results of the industry's R&D activities during the past year. As we reported in the 1986 newsletter, the level of new product introductions was very high. This year, new product introductions were at a much lower level. Because of the worldwide recession in the industry, many of the 1986 new products have not had an opportunity to really get off the ground. It appeared to Dataquest that sales of the new products have been disappointingly slow. Thus, without sales revenue to fund the R&D cycle, new products and product enhancements for the industry will fall off, which is what we witnessed at this year's SEMICON/West.

Not all equipment segments were off in new product introductions, however, as the chemical vapor deposition (CVD) and wafer inspection segments continued their higher level of activity. Last year, we reported that SEMICON/West 1986 was the "coming-out party" for CVD equipment. This year, the pace continued as several significant new products were introduced. Last year we did not report on wafer inspection, but do so this year because of the higher level of interest and significant new products in this area.

Because of space considerations, we can give only a brief overview of the products. For further information please contact the manufacturers directly. Please refer to last year's newsletter. Together, the two newsletters provide a good picture of the direction of the equipment industry.

LITHOGRAPHY

The key developments in steppers were mainly in the area of submicron lenses, as the stepper manufacturers pushed further and further into the submicron realm. As lens resolution continues to increase, however, concomitant improvements in overlay accuracy need to be made to take full advantage of the resolution gains. Accordingly, we also saw improvements in alignment systems and barometric and magnification control systems. The technical approach towards submicron lenses vary: the Japanese are continuing their strategy of high numerical aperture, g-line lenses, while U.S. and European manufacturers are taking the i-line approach.

The advent of the excimer laser optical stepper may have dealt another delay to X-ray. Nevertheless, a new X-ray stepper manufacturer appeared in the market while another X-ray stepper manufacturer was fighting for survival. It is still not clear when the X-ray market will become a reality, although development of synchrotron sources continues to increase on a worldwide level.

In maskmaking lithography, new high-speed laser optical pattern generators were introduced by two companies. One company, ATEQ, has a novel approach of putting the laser pattern generator in the wafer fab area, next to the steppers for quick prototype device turnaround.

Steppers

Most of the key developments were in lenses. Last year at this time there were nine stepper vendors; six of the vendors used either Zeiss or Wild Heerbrugg lenses, and the other three built their own lenses. Since then, Eaton has left the stepper market, Perkin-Elmer has decided to build its lenses in-house, and GCA is relying more and more on its own Tropel lenses. Now only three companies rely solely on Zeiss for its lenses. In last year's newsletter, we remarked that with so many vendors relying on Zeiss for lenses, supply could be a problem. It now appears that this is no longer a concern. Incidentally, it was always a puzzlement why Perkin-Elmer did not build its own lenses earlier, since it has had world-class optical fabrication facilities for some time.

Other developments in lenses include the introduction of variable numerical aperture lenses by two companies (Canon and Ultratech). Also introduced was a special lens designed by GCA for production use in excimer laser steppers.

Last year, American Semiconductor Equipment Technologies introduced the world's first large-substrate stepper or flat panel display stepper. Since then, both Canon and Nikon have introduced large-substrate steppers and another U.S. company will soon enter the market. This is an embryonic market, and Dataquest believes only a few systems have been delivered.

ASM Lithography

ASM exhibited the PAS 2500/10, which was first exhibited in the United States at last year's SEMICON/West. This system uses the Zeiss 10-78-46 lens, which is a 5X, 0.38 NA, g-line lens with 0.9-micron resolution over a field size of 20mm. ASM claims the highest throughput in the industry for the 2500/10, which is 62 125mm or 50 150mm wafers per hour with global alignment. Overlay accuracy is specified to be 0.15 micron (3 sigma). The system was basically the same as exhibited last year, except that the automatic reticle changer is SMIF compatible and handles 6 instead of 7 reticles. Perhaps the most significant new feature introduced for the PAS 2500 is the 2-year warranty on parts and labor.

Other recent developments include the replacement of the PAS 2500/20 system with the PAS 2500/40. These systems differ only in the choice of lens used: the 2500/20 uses the Zeiss 10-78-52 i-line lens, while the 2500/40 uses the Zeiss 10-78-58 i-line lens. The 10-78-58 is a 5X, 0.40 NA lens with a resolution of 0.7 micron over a field size of 20mm. Throughput for the 2500/40 is the same as that for the 2500/10.

Since no calibration is required for the PAS 2500, ASM claims that equipment utilization, or system production availability, can be as high as 80 percent.

The price of the 2500/10 is $1.035 million, the 2500/40 is $1.2 million.

American Semiconductor Equipment Technologies (ASET)

ASET has just successfully completed its first full year of operation after the February 1986 buyout of the assets and technology of TRE Semiconductor.

ASET exhibited the 900 SLR Series stepper, which it announced but did not exhibit at last year's SEMICON/West. The five steppers in the 900 Series, three g-line and two i-line steppers, all use Zeiss lenses and are summarized in Table 1.

Table 1

LENSES USED BY ASET

Model	Zeiss Lens	Wavelength	Reduction Ratio	NA	Field Diameter (mm)	Resolution (micron)
945	10-78-45	g-line	10X	0.38	14.5	0.91
946	10-78-46	g-line	5X	0.38	20.0	0.91
947	10-78-47	g-line	5X	0.28	29.0	1.25
948	10-78-48	i-line	10X	0.42	13.0	0.70
952	10-78-52	i-line	5X	0.32	23.0	0.91

Source: ASET

The 900 Series has an overlay accuracy of 0.2 micron (3 sigma). The 900 Series offers a choice of a 4-reticle carousel with a 5-second reticle change time, or a 10-reticle cassette with a change time of 15 to 20 seconds. Other new features of the 900 Series include automatic compensation for barometric pressure changes, magnification control via keyboard, a more user-friendly computer system with expanded capability, and the use of a nonactinic wavelength alignment system, which enables capturing of difficult targets.

The price of the 900 Series g-line systems is about $900,000; i-line systems are in the range of $1.2 million to $1.3 million.

ASET also purchased the assets and technology of TRE's maskmaking operations and is continuing to manufacture a line of optical pattern generators and image repeaters for use in the maskmaking industry. At SEMICON/West, ASET introduced the 600 Series image repeater, a repeater with superior positional resolution especially designed for manufacturing 1X masks. Currently, highly accurate 1X must be completely written on an E-beam pattern generator, as present optical image repeaters do not have the required positional accuracy. Writing a 1X mask on an E-beam could take three to four hours, and hence, be very costly. The 600 Series image repeater will once again allow 1X masks to be made by the less costlier optical step-and-repeat method.

There are three models in the 600 Series. Depending upon the choice of Zeiss lens, resolutions down to 0.91 micron can be obtained.

Canon

Canon exhibited the FPA-1550MII stepper with the new selectable numerical aperture lens. By means of a switch, the numerical aperture can be changed from 0.35 to 0.43. This lens has a field diameter of 21.2mm and programmable masking blades under computer control, which can be varied at each site if desired. Resolution of the lens is 0.8 micron (at 0.43 NA) or 1 micron (at 0.35 NA) with a total depth of focus of 2 microns with the 0.43 NA.

The price of the FPA-1550MII with selectable lens is $1.15 million, and this system is currently being shipped.

Canon also introduced, but did not exhibit, the MPA-1500 Mirror Projection Mask Aligner to the U.S. market. This system, which is specifically designed for flat panel displays, has a 280mm x 332mm exposure area that is exposed with four step-and-repeat exposures. Either four different masks can be used in the step-and-repeat operation, or a single mask can be stepped four times in the exposure field. Throughput is 35 to 46 substrates per hour, using four different masks, or 41 to 57 per hour, using a single mask.

The MPA-1500 was introduced in Japan in 1986 and exhibited at SEMICON/Europe in March 1987. The system uses the same optical system as that used by the MPA-500/600 series of projection aligners, which Canon has been marketing since 1981.

Until recently, only lithography products manufactured by Canon's semiconductor equipment operations have been marketed by Canon in the United States. At SEMICON/West, however, Canon exhibited a wider range of its semiconductor equipment, including the AIM-630 Automatic Identify Marker, the ARS-630 Automatic Reader and Sorter, the ESC-530 Epitaxial Spike Crusher, the MAS-800 Microwave Asher, and the CDS-650 Coater/Developer. Thus, it is apparent that Canon, like Nikon, wants to market more of its products in the United States.

GCA

GCA exhibited its new wide-field i-line version of the Model 8500 DSW Wafer Stepper fitted with the new Tropel 2235i lens. This 5X i-line lens has a numerical aperture of 0.35, resolution of 0.7 to 0.8 micron, a 22mm diameter field, and a depth of focus of 2 microns. Previously, GCA offered the Model 8000 DSW with the Tropel 1635 5X i-line lens, which will still be available. The 1635 lens has the same NA and resolution as the 2235i, but the 1635 has a smaller field size of 16mm diameter.

The 8500 includes the new dark field alignment system, a through-the-lens local alignment technique that provides 0.2 micron (3 sigma) overlay accuracy on a single machine, or 0.3 micron (3 sigma) for matched steppers, machine-to-machine. Also new to the 8500 is an auto focus system that provides focus and tilt at each exposure site. Throughput for the 8500 is 48 125mm wafers per hour and 38 150mm wafers per hour.

The price of the 8500 DSW with the 2235i lens is $1.2 million.

GCA also showed the Tropel lens designed for use with 248nm excimer lasers. This is a 5X, 0.35 NA lens, with a resolution of 0.5 micron and a field size of 20mm diameter. The GCA stepper designed for use with excimer lasers was developed under a VHSIC contract, and the first GCA excimer laser stepper is expected to be shipped to a VHSIC contractor in June 1987.

Nikon

Nikon exhibited the NSR-1505G4 stepper which can be equipped with several g-line lenses. The submicron g-line lenses offered for this system are listed in Table 2.

Table 2

LENSES USED BY NIKON

NSR Model	Reduction Ratio	Resolution (micron)	NA	Exposure Area (mm)
1505G4D	5X	0.75	0.45	15 X 15
1505G4C	5X	0.8	0.42	15 X 15
1505G4B	5X	0.9	0.35	15 X 15
0510G4	10X	0.6	0.60	5 X 5

Source: Nikon

The 0.45 NA lens (Model 5A3S) was announced by Nikon in January 1987. This lens has a distortion, including magnification error, of less than 0.13 micron. Total depth of focus is 1.5 microns for 0.75-micron geometries.

The 1505G4 series steppers offer two alignment options: dark field, site-by-site alignment and enhanced global alignment (EGA) to obtain an alignment accuracy of 0.18 micron (3 sigma) in either mode of operation. Machine-to-machine interchangeability is 0.18 micron (95 percent). Throughput for the 1505G4 steppers with EGA is 58 125mm wafers per hour and 48 150mm wafers per hour. The 1505G4 series also includes automatic magnification adjustment and site-by-site focus control.

Nikon has also recently introduced, both in Japan and the United States, the NSR-L7501G stepper for flat panel displays (not exhibited at SEMICON/West). This is a 1:1 system that uses conventional reticles. The 300mm x 300mm exposure area is covered in a step-and-repeat fashion with eight 75mm x 75mm exposures. The price of the NSR-L7501G is $1.3 million.

Perkin-Elmer

Perkin-Elmer exhibited the new Micrastep, an enhanced version of the SRA-9000 Series stepper that uses lenses fabricated by Perkin-Elmer in lieu of the Zeiss and Wild Heerbrugg lenses used in the SRA-9000 steppers. Two lens options are available for the Micrastep: one is a 0.35 NA lens that provides 1.0-micron resolution and the other is a 0.8-micron lens. Both lenses have 24mm diameter fields that can expose 17mm x 17mm fields.

New features on the Micrastep, besides the new lenses, include air gauge, site-by-site focusing and leveling, dark field/bright field alignment, and digital signal processing for alignment on tough levels. Site-by-site alignment accuracy is 0.15 micron (98 percent), and machine-to-machine overlay is 0.25 (98 percent). Throughput is 60 125mm wafers per hour.

Micrastep 1 (1-micron resolution) is priced at $995,000; Micrastep 2 (0.8-micron resolution) is priced at $1.15 million. Perkin-Elmer began shipping Micrasteps in November 1986.

Ultratech

Ultratech exhibited two new products: the UltraStep 990, a wide-field, high-throughput stepper designed to replace projection aligners and the UltraStep 1100-4035 variable aperture stepper.

The Model 990 uses a lens with a 0.21 NA and a production resolution of 1.4 microns over a very large field size of 30mm x 15mm (4.5cm^2) maximum rectangle or 18mm x 18mm maximum square. Throughput is 65 125mm or 50 150mm wafers per hour. The price of the 990 is $440,000. The first system has been shipped to Linear Technology.

The UltraStep 1100-4035 is the Model 1100 stepper fitted with the new 4035 variable numerical aperture lens. The 4035 lens uses an adjustable iris to vary the numerical aperture from 0.20 to 0.40. At 0.32 NA the resolution of the lens is 0.95 micron; at 0.35 NA it is 0.85 micron; and at 0.40 NA it is 0.70 micron. Field size at 0.32 NA is 30mm x 15mm ($4.5cm^2$), or 18mm x 18mm. At 0.40 NA, the field size is 30mm x 12mm ($3.6cm^2$), or 15mm x 15mm.

Depth of focus of the 4035 at 0.40 NA is 1.5 microns total. Throughput at 0.40 NA and 0.70-micron resolution is 40 125mm or 30 150mm wafers per hour.

In 1987 the 1100-4035 will be offered only as a limited product. One reason for this is the lens material availability. Also, Ultratech will discuss each customer's specifications so that the stepper is individually configured to meet customer requirements. In the future, Ultratech expects to see more and more custom steppers. An interesting side note is that the 4035 lens weighs 180 pounds.

Ultratech is also pushing its retrofit strategy by which it can upgrade its first stepper, the Model 900 (initially delivered in 1981), to the latest Model 1100-4035. A historical note of interest is that the 900 had a field size of $1.52cm^2$ as compared to $4.5cm^2$ on today's systems.

The price of the 1100-4035 is more than $1 million. A Model 1100 with the 4035 lens has not yet been delivered.

X-ray Lithography

With the advent of Hampshire Instrument's new X-ray stepper, three companies are now offering X-ray steppers to the commercial market. Each company has taken a different technical approach. Hampshire uses a pulsed laser source, Micronix uses a fixed palladium source, and Karl Suss's stepper is intended for a synchrotron source. The resolution of the Hampshire and Micronix steppers is 0.5 micron, which is the same resolution that the optical people say they can attain with excimer laser steppers. Thus, it is still not clear what lithography technology will be used in the realm of 0.5 micron and below, and the outlook for nonsynchrotron source, X-ray lithography remains vague.

Worldwide development of synchrotron sources is increasing. Besides the extensive work being done by the West Germans, the Japanese, and IBM at Brookhaven, there is activity in Italy, France, and at other locations in the United States. In fact, the first commercial synchrotron-compatible X-ray stepper, outside of IBM and the Fraunhofer Institute, will most likely be installed at the University of Wisconsin's large synchrotron ring. Before X-ray synchrotron becomes a production reality, however, compact rings must be developed, and such activity is being undertaken in Europe and Japan. Besides Cosy-Microtec in Germany and Oxford Instruments in England, there are two organizations in Japan. Cosy-Microtec's system, using superconducting magnets, is expected to be on the market about 18 months from now.

Hampshire Instruments

Hampshire, a start-up company formed in late 1983, exhibited its first product, the XRL 5000 X-ray stepper. The XRL 5000 uses a pulsed, highpeak power, solid state slab laser that illuminates a target to generate a source of X-rays with a diameter of 100 microns and a range of 0.8 to 2.2nm. Target life is one 8-hour shift (20,000 exposures). Source-to-mask distance is 7 to 12cm and mask-to-wafer distance is nominally 20 microns. A single pulse from the source exposes a field of 20mm x 20mm on the wafer with a depth of field of 30 microns.

The XRL 5000 has a resolution limit of 0.3 micron and a working resolution of 0.5 micron. Throughput is 15 to 40 wafers per hour. Dark field alignment is used to provide an alignment precision of 0.15 micron (2 sigma).

Hampshire uses 76mm diameter masks that can be fabricated with conventional thin film technologies. Mounted on top of a 76mm diameter support ring is a silicon wafer with the center etched out. On the wafer is an epitaxial layer of silicon then a layer of tungsten on the epi silicon, and finally a layer of photoresist. After patterning the photoresist, the tungsten is etched and the photoresist stripped. Hampshire has its own X-ray mask shop, and intends to supply its customers with masks.

The XRL 5000 is priced at $1.75 million, and the first systems will be delivered late in 1987. Dataquest believes that the first machines will be delivered to Digital Equipment Corporation, with whom Hampshire has had a joint development agreement since 1985.

Karl Suss

Last year, Suss introduced its XRS-200 X-ray stepper, but exhibited only a model. This year, an actual system was on display. The XRS-200 is a joint development effort between Karl Suss America, which developed the entire electronic subsystem, and Karl Suss West Germany, which developed the rest of the machine. The XRS-200 alignment system, which has an alignment accuracy of 0.1 micron (2 sigma), was developed by Siemens.

The XRS-200, specifically designed for use with X-ray synchrotron sources, holds the mask and wafer in a vertical position and scans them through the X-ray beam. Mask-to-wafer distance is typically 40 microns. Field size can range from 26mm x 26mm to 45mm x 45mm, although initially field size will be limited by maskmaking technology. Both alignment and exposure times for each field are typically one second. Stepping time from field to field is one second. The XRS-200 is capable of 0.2-micron resolution and a throughput of 20 150mm wafers per hour with a synchrotron source.

Suss is also developing a plasma source for use with the XRS-200, but because exposure time per field will be in minutes rather than seconds obtainable with a synchrotron source, it will only be suitable for R&D use.

The first XRS-200 will ship to the Fraunhofer Institute in Berlin to replace one of the two Karl Suss prototype X-ray aligners that have been operating for the last three years. Suss will begin shipments in the first half of 1988 to the commercial market to those organizations that have access to synchrotron sources. The price of the XRS-200 is $1 million. Suss says it has orders in hand for the commercial market.

Optical Maskmaking Lithography

In the past, optical pattern generation has given way to the much higher-speed e-beam pattern generators. While laser beam optical pattern generators have been on the market, they were still quite slow compared with e-beam machines. This year, however, two high-speed optical systems appeared on the market. ATEQ's high-speed system, in particular, is intended to compete against e-beam machines.

ATEQ

ATEQ introduced its CORE-2000, a high-speed optical pattern generator intended to compete directly against the industry-standard e-beam pattern generator. The CORE-2000 is a raster scan system that writes the reticle with eight parallel laser beams and is especially designed to write 5X and 10X reticles. As each beam can potentially write at a rate of 50 MHz, the CORE-2000 can achieve a system rate of 400 MHz.

The CORE-2000 accepts standard industry format tapes and exposes standard optical photoresists. ATEQ has exceeded its composite overlay specification design goals and now claims the tightest specification in the industry at 0.15 micron (3 sigma). ATEQ has also increased addressing to 0.1 micron.

Besides the market for the CORE-2000 as a maskmaking tool for the maskmaking industry, ATEQ is targeting the semiconductor manufacturer for the quick-turn prototyping market. In this application, a CORE-2000 would be installed in the wafer fab area next to a stepper. The reticle for the prototype IC would be generated on the CORE-2000, processed immediately in the lithography area, and then inserted directly into the stepper for exposure. Reticle inspection and repair may or may not be used, depending upon the strategy.

The CORE-2000 is priced at $1.8 million. ATEQ shipped its first machine in early 1987 to Canon Sales, Tokyo, its representative in Japan. ATEQ has had a second system accepted by Canon Sales, and in addition, has received two more orders from Cannon. ATEQ has also received an order from Master Images, the first order from a U.S. maskmaker.

Micronic Lasersystem

This Swedish company introduced the LASERSKAN II, a second-generation, laser pattern generator for the production of masks and reticles. Micronic Lasersystem introduced its first laser pattern generator in 1978, but only sold a few systems. The current system is 10 times faster than the earlier system. The LASERSKAN II, a single-beam system, can focus the laser beam into a spot 0.5 micron in diameter and uses raster scan to expose the optical photoresist. Throughput for a 70mm x 70mm 5X substrate is 30 minutes for a 1-micron raster.

Besides maskmaking use, it can be used in direct-write applications, such as quick-turn prototyping, gate arrays, and small-volume production.

The price of the system is $800,000 to $1 million. No systems have yet been delivered.

AUTOMATIC PHOTORESIST PROCESSING EQUIPMENT

Eleven new track systems premiered at SEMICON/West, as well as enhancements of existing systems. Improvements and enhancements of existing systems tended to focus on increased manufacturing flexibility, improved process control, improved wafer handling, and increased throughput.

Dainippon Screen

Dainippon Screen did not show any equipment at SEMICON/West, but did have a booth to announce its products. We think this is significant because Dainippon is a major semiconductor equipment manufacturer in Japan, and this is the first time it had exhibited at SEMICON/West. In addition to track equipment, Dainippon Screen also manufactures maskmaking process equipment, wet and dry etch equipment, and lead bonders.

Eaton

Eaton introduced a new spin-on-glass (SOG) system, the 6030XL. This system has an SOG process module and dispense system that features both a teflon tub bowl wash and a nozzle wash. It also has three different pump options for its dispense station: a pressurized pump, a Millipore pump, or a Tri Tech pump. It also has a programmed pre-dispense purge and a Sierra systems programmable exhaust to maintain a constant exhaust pressure in the system. Each of the two hotplates on the 6030XL can be set to three different temperatures.

GCA

Shown for the first time at SEMICON/West was the Wafertrac III V, made specifically for fragile gallium arsenide wafers. The Wafertrac III V is designed to handle wafer sizes from 2 inches to 125mm. It has no air bearings, as wafers are transferred on an O-ring transport system. The system has a moving arm resist dispense system with a nozzle purge, plus a spinner program step capability for flexibility. The III V also has spin speed control of +/- 0.5 percent and a spinner edge-bead removal feature.

GCA also showed its Microtrac for the first time at SEMICON/West. The Microtrac is a one-track module for develop/bake, coat/bake, or vapor/prime. First shipments for the Microtrac were made in fourth quarter 1986.

GCA has added vacuum vapor prime to its 1006 track equipment, which it believes will provide better uniformity than the older batch prime process. The new vacuum vapor prime can be retrofitted to older 1006s.

Machine Technology Inc. (MTI)

MTI introduced a new handler for its MultiFab system. The new handler has full backside support for the wafer and does not use a vacuum to support the wafer. The MultiFab also has a double bake station featuring new software for increased processing flexibility or throughput.

MTI also announced, but did not show, a new spin-on-glass system.

Solitec

Solitec offered several new track systems for the first time at SEMICON/West. These new systems were the Optimist Positive Developer Nozzle, the Auto Coat, the In-Line Thickness Monitor, and the Flood Exposure Track.

Solitec designed the Optimist to meet a number of goals, including to reduce developer usage by 50 percent, to prevent any developer drips from falling on the wafer, to provide a process that is insensitive to ambient air movement, to provide a nozzle with wide position latitude, and to provide a process with excellent CD control (0.3 micron with 1 sigma variation across a 150mm wafer with 2-micron line geometries.) A unique feature of the Optimist nozzle is that nitrogen is pumped through the nozzle with the developer. The nitrogen is then able to act as a protective shroud over the wafer.

Solitec also introduced the Auto Coat, which Solitec claims reduces photoresist usage by 50 percent ($2cm^3$ per 150mm wafer). The Auto Coat also monitors suckback and bubbles in the resist line and then alerts the operator to conditions that might cause defective coatings. Solitec claims coating uniformities of 60 angstroms (3 sigma) across a 150mm wafer.

The In-line Thickness Monitor (ILTM) features real-time in-line thickness measurement. It can measure resist thickness in 2 seconds per point (up to 17 points) and at either the hotplate or inspection station. The ILTM has a process analysis software package that monitors single or multiple tracks. The method of measurement is based on a spectrometer and incorporates fiber optics.

The Flood Exposure Track has a DUV flood exposure simultaneous with the hotplate bake. The system is designed for high throughput and for a small clean room footprint.

Semix

Semix introduced the Spin-on-Glass Coat/Bake System manufactured in Japan by Tazmo. The new system, the TR 6002, is a fourth generation SOG coating system. It offers a new noncontact alignment option (patent pending) for soft handling of gallium arsenide wafers. The TR 6002 has the only patented dispense system for spin-on-glass and has a wafer transfer system that is both beltless and without air bearings. It features a small footprint and a user interface that has remote capabilities. The home position for the dispense nozzle arm is on the side of the dispense cup so it is impossible for drips to fall on the wafer. The TR 6002 also has a new cup design to control the air flow of programmable exhaust. Semix reports that it has shipped some units.

Silicon Valley Group (SVG)

SVG introduced the 8632 CTD-MD, positive develop/hot plate system. The 8632 features a radial dispense system to achieve a uniform develop and to eliminate hot spots. The 8632 CTD-MD can dispense developer by spray, puddle, or spuddle methods (spuddle is a combination of spray and puddle).

SVG also introduced the 8642 SOG MHP. The 8642 is a spin-on-glass system with a radial dispense and bowl wash. It features an alcohol bath system at the dispense tip to prevent crystallization. The 8642 also features a multiple hotplate with a linear transfer arm that has a three-position vacuum wand pick up. This arm does not pass over another process module. The 8642 operates in either series or parallel mode. The 8642 has a programmable Sierra flow controller to maintain constant exhaust. SVG reports that it has already shipped some units.

Semiconductor Systems, Inc. (SSI)

SSI introduced the System One-B, a new automatic spin coating and baking system designed for increased reliability, improved process control, and higher throughput. Available modules include automated spin coaters for application of photoresists, polyimides and dopants; modules for spin-on-glass; spray developers; bake modules; and cooling units. An open electronics architecture, designed around an RS-485 bit-bus network, allows microprocessor control of each module.

DRY STRIP AND ETCH

Dry Strip

Consistent with the general showing at this year's exposition, there was a deficit of new products. The trend in this equipment segment was demonstrated last year with the introduction of nine single-wafer strippers. This new product is envisioned to solve many problems that arise from processing resist in very harsh environments such as during reactive ion etching and high-current implantation.

Under the high energy conditions of these processes, the resist becomes akin to Bakelite and is extremely difficult to remove. These resists are traditionally removed by wet stripping, which introduces the problems associated with process-induced particulates and hazardous chemicals. If dry stripping in barrels were used, the time that the substrate film is exposed to the oxygen plasma causes oxidation, which in turn compromises subsequent processing steps. Even after dry stripping, the wafer must be dipped in acid to remove the residual resist scum and the unwanted oxide film.

Semiconductor manufacturers would choose to suffer the process complications in barrels if they could solve the problem of C-V shift and threshold voltage shifts in the devices. These electrical problems are believed to be caused by residual sodium from the photoresist being driven into the film during stripping. With the introduction of single-wafer strippers, in which the plasma is generated remotely from the wafer, these problems of removing tenacious resists are drastically reduced.

The data that Dataquest have seen demonstrate that C-V and threshold voltage shifts and film oxidation are much lower in single-wafer strippers than in barrel systems. The intense plasma stream efficiently removes the baked-on resist, completing processing in typically less than two minutes. This brief processing time reduces the oxidation of the substrate. In addition, end-point can be more accurately assessed on a single wafer than over a batch of wafers; hence, oxidation from overetching is reduced. Finally, the added advantages include cassette-to-cassette operation and reduced wet chemical usage and waste.

In 1986, the market for dry strip was $32 million. We estimate that the market for wet strip adds $13 million, bringing the total market to $45 million. Companies that are introducing products into this segment perceive that the whole strip process installed base, including both barrels and wet benches, will convert to single-wafer dry stripping. This could indeed be a high-growth market niche. However, this market niche is currently somewhat crowded. This year, two companies introduced new single-wafer systems: General Signal/Drytek and Yield Engineering Systems.

Table 3 lists the various companies that market single-wafer strippers.

Table 3

SINGLE-WAFER STRIPPERS

Company	Price	Comments
Alcan Tech, Inc.	$100,000	Includes pump
Drytek	$100,000	Without pump
Branson/IPC	$130,000	Without pump, two chambers
Emergent Technologies	$110,000	Includes pump
Gasonics	$ 78,000	Without pump
Machine Technology	$110,000	Includes pump
Matrix	$ 87,500	Includes pump
Plasma Systems (Semix)	$125,000	Includes pump
Plasma-Therm	N/A	Discontinued product
Tegal	$110,000	Includes pump, contact plasma
Yield Engineering Sys.	$ 40,000	With pump

N/A = Not Applicable

Source: Dataquest
June 1987

General Signal/Drytek

Drytek introduced a downstream plasma stripper that utilizes the same frame as that used in the company's other dry etch products. The stripper accommodates two gases. The plasma is created remotely in a chamber above the wafer chamber and is pumped from below the wafer. There is not line-of-sight from the remote chamber to the wafer. The system has cassette-to-cassette operation. The price of the system is approximately $100,000 without the pump.

Yield Engineering Systems

This company manufactures various resist processing equipment. It introduced a manually loaded, single-wafer stripper with no bells and whistles that sells for approximately $40,000, including the pump.

Dry Etch

As in most other equipment categories, this segment saw product development efforts materialize into system introductions at last year's SEMICON/West. This year, companies that are selling into this segment are still waiting for some return on their investment.

Most vendors took the opportunity to distance themselves from the competition by featuring cleanliness, particularly, particulate control. While this is an extremely important feature, the emphasis will shift to equipment versatility.

The process shift is in the etching of refractory metals and single crystal silicon. It is apparent now that the next evolution of technology, that of the 4-Mbit DRAM, will use both refractory metal interconnects and trenches. Unlike the previous evolutionary step, the 1-Mbit DRAM, in which semiconductor manufacturers did not move the R&D devices into production, there appears to be little choice at line geometries below 1 micron. There are numerous scenarios for the process flow and architecture of these new devices, and the competitive drama is again centered on the "batch/ single-wafer" issue.

The versatility necessary for solving these new processing problems may be achieved by leveraging productivity over a large batch, or by adding multiple processing chambers. The former approach is dominated by Applied Materials, with its hexode configuration. The company has gained 10 percent market share, growing from 25 percent in 1985 to 35 percent in 1986. The latter approach has been taken by several companies vying for position in the single-wafer segment: Lam Research Corporation (LRC) and Tegal are the leaders in this segment; LRC fell from 11.4 percent in 1985 to 11 percent in 1986, while Tegal grew from 8.4 percent in 1985 to 10.6 percent in 1986.

Since last year's SEMICON/West, Dataquest has seen several new products that target these new markets. These are featured below.

Lam Research Corporation

The company introduced the much-heralded Rainbow Etcher at this year's SEMICON/West. The system is remarkably similar to the earlier product in that it has a similar chamber configuration, can adjust electrode spacing, and uses a 13.5 MHz power supply. The attractiveness of the system is more in the added value than in the visible features.

One obvious change from the previous design is that the power supply can supply both the upper and lower electrodes. With its grounded chamber walls, this systems falls into the triode category, a feature which greatly enhances its versatility. The hidden feature, which could greatly improve its competitiveness, is the cleanliness of the system. The specification is less than 0.3 particle per cm^2 for particles 0.3 micron or larger.

The company will offer a family of products to target all processes and chemistries being used on advanced devices. The price of the system will be approximately $550,000.

Varian/Zylin

Zylin has leapfrogged its new Zylin 100 system to introduce the Model 6100. This system incorporates downstream, microwave processing to remove and/or passivate photoresist after aluminum etching. Zylin has added the ability to power either the upper or lower electrode, so the system can be used in plasma or RIE configuration. The system can be configured with two, three, or four in-line chambers, each isolated from the other. This flexibility can enhance throughput in single-layer applications or provide multilayer processing for composite structures.

The 6100 series uses helium, beneath-the-wafer cooling to control the processing temperature. Dataquest learned that Varian holds the patent on this technique and will "go after" other equipment vendors that have adopted it. The system price is $550,000.

Tegal

Tegal has beefed up its Model 1500. The system can power both the upper or lower electrodes and can use either 2.45 GHz or 13.6 MHz on the upper electrode. By using two frequencies, the energy/ion density ratio of the plasma can be adjusted to enhance process versatility. Three models in the family can target several processes, including advanced processes for next-generation devices. The system cost is $350,000 to $390,000

Electron Cyclotron Resonance

Although systems utilizing electron cyclotron resonance (ECR) were not exhibited at SEMICON/West this year, they warrant some mention as advanced new products. This technology was invented by Nippon Telephone and Telegraph (NTT) in 1978 as a deposition technique.

The technique utilizes the excitation and ionization of the working gas by a microwave source in a high magnetic field at the cyclotron resonance of the outer shell electrons. This produces an extremely high density plasma, one or two orders of magnitude more dense than conventional plasmas, which can be utilized at low energy levels to etch or deposit. The strong magnetic field induces a small electric field of about 20V at the extraction exit. This low energy, directional stream of high-density ions can then impinge on the wafer surface below the excitation chamber. Etch or deposition by-products are pumped out at very low pressures from below the wafer.

Several companies have experimented with this technology, including Anelva, Sumitomo Metal, Plasma Technology, and Hitachi. Sumitomo, Plasma Technology, and Hitachi have formal product introductions in this area.

Sumitomo Heavy Metal

This Japanese company introduced a multichamber version of ECR processing at SEMICON/Japan last December. The system uses two chambers and operates at less than 1 millitorr chamber pressure. The price of the system is approximately ¥90 million ($600,000 at current exchange rates).

Plasma Technology

This U.K. company is a spin-off from E.T. Electrotech and is located in Bristol, England. The company has introduced an R&D version, manual load system for deposition or etching and intends to introduce a cassette-to-cassette version by the end of 1987. For the R&D version, it recorded processing pressures of 10^{-5} torr, etch rates 100 times greater than conventional plasma, and nonuniformities of less than 3 percent across a 200mm wafer. The company is targeting silicon dioxide, silicon trench, aluminum alloy, and GaAs processes.

Hitachi

This Japanese company has vertically integrated systems, semiconductors, and equipment under one parent. The equipment division was actually 13th in the world in 1986 sales of front-end fabrication equipment. It publicly introduced a version of an ECR system that does not use NTT technology, but does use a microwave power supply to excite the plasma.

The plasma and wafer are confined within a quartz bell jar surrounded with magnetic coils. While a magnetron waveguide is used to excite the plasma, the wafer sits on a powered cathode which can be biased by 13.5 MHz RF power. Without RF bias, the voltage at the substrate is about 20V. Bias raises the plasma potential between 100 and 200V. The company claims that the damage is from one-tenth to one-thirtieth that caused by reactive ion etching (RIE). The price for this system is approximately ¥140 million ($930,000 at current exchange rates). The company expects to begin exporting the system in 1988.

CHEMICAL VAPOR DEPOSITION

Last year we remarked that SEMICON/West 1986 was the "coming-out party" for CVD equipment, as new companies appeared in this segment, and many new models of equipment were introduced by both new and established companies. The intense activity in CVD equipment has continued into 1987, as still more new equipment and improved processes were introduced. It is likely that there is more activity in the CVD area than in any other area of wafer fab equipment, as CVD technology advances to meet the needs of leading-edge ICs.

This portion of the newsletter reports only on the dedicated CVD reactor market (nontube market--please refer to the section on diffusion for horizontal/vertical tube CVD) that for the most part has emerged only in the last two to three years. For instance, of the 12 companies listed below, all have introduced significant new products within the last three years. Even at this year's SEMICON/West, where new product introductions were generally more subdued across the industry, there were five significant new CVD equipment introductions.

Four of the companies (Genus, Spectrum CVD, Ulvac, and Varian) provide reactors for the deposition of tungsten films, an area where only a year ago Genus had the market to itself. The other companies are mainly concentrating on depositing dielectrics, and here competition is intense as film quality becomes the battleground. Particular emphasis is being addressed to high-quality intermetal dielectrics, resulting from the industry move to double-metal ICs. Particulates is another battleground, and many vendors are beginning to provide cleanliness specifications for their equipment.

Currently, CVD is one of the more exciting areas in wafer fab equipment. We expect it to continue to be so, as CVD technology continues to evolve and as the players compete for a market that is forecast to be $350 million by 1990.

Applied Materials

Applied Materials exhibited its new Precision 5000 CVD system for the low-temperature deposition of dielectrics. Processes include intermetal dielectrics, passivation, and conformal depositions in such applications as, sidewall spacers, trench liner, or trench isolation.

The system deposits pyrolytic (thermal) oxide at a rate of 3000 angstroms per minute for a 100 percent conformal film using TEOS as the source. Applied has developed a proprietary process that deposits TEOS oxides below 400°C; thus, TEOS films can be used as intermetal dielectrics. The Precision 5000 also provides for plasma enhanced deposition (PECVD) at rates of 8000 angstroms per minute. For passivation, nitride, oxide, oxynitride, or combination films can be deposited. Liquid sources only are used for all deposition processes.

The system uses a multichamber approach in which multiple processes can occur in a single chamber. A multiple in-situ process, for example, would be a PECVD oxide deposition, followed by a pyrolytic oxide deposition, and then an etch-back step. The resulting film would be a planarized, void-free oxide film. The final process is the plasma clean cycle that occurs after every wafer is processed during the wafer transfer cycle. Two chambers are standard, with four chambers optional.

Price of the Precision 5000 with two chambers is $750,000; with four chambers the price is $1.2 million. Applied Materials says it has commitments for 20 systems from 10 customers. The first systems were shipped in May 1987.

Electrotech

Electrotech introduced a higher throughput version of the ND6200 PECVD system, called the ND6201. In the ND6200, batches of wafers are transferred and processed in batches in the parallel plate process chamber. The ND6201 uses the same process chamber except that individual wafers are continuously transferred into and out of the chamber. The result is that throughput for

the ND6201 has been increased to 50 100mm wafers per hour for a 1-micron film of oxide. The ND6201 is for an oxide process only. For the ND6200, Electrotech has introduced plasma BPSG and oxynitride processes.

Price of the ND6200 is $450,000; the ND6201 is priced at $480,000. Also available is the ND8200, a 200mm version of the ND6200 introduced last year; it is priced at $500,000.

Focus Semiconductor

Focus, a venture capital backed firm established in May 1984, exhibited the F1000 LTO Deposition System. This system, the firm's initial product, was displayed for the first time at SEMICON/West 1986 and is described more fully in last year's newsletter.

The battle for the CVD market will be fought not only on film quality, but also cleanliness. Focus presented the typical cleanliness results of the F1000. For particle sizes greater than 0.4 micron, average particles on a 100mm wafer were measured to be 0.04 particles per cm^2 before processing in the F1000, and 0.08 particles per cm^2 were counted after processing. These results were obtained after 25 microns of film had been deposited in the F1000 after 11 hours of operation.

Focus is currently shipping the F1000.

Genus

Genus introduced the Model 8710 system for the deposition of tungsten silicides. The 8710, a cold-wall reactor, is a further development of Genus's cold-wall technology, as used in its 8300/8400 series reactors. The 8700 is a 200mm, production system with dual load-locks that uses a batch type reactor processing six wafers per batch. Throughput is 20 to 40 wafers per hour.

The 8710 can use either silane chemistry, or the newly developed dichlorosilane chemistry, for the deposition of tungsten silicide. The dichlorosilane process uses higher deposition temperatures (525°C versus 360°C for the silane process) to provide films with more surface mobility, thus enhancing step coverage. This is particularly beneficial in EPROM devices, where higher steps are encountered.

The 8710 is priced at $750,000. The first production unit was shipped in December 1986, but a 200mm prototype 8710 was shipped 18 months ago.

Currently, the 8710 is for tungsten silicide films; under development is a selective tungsten-on-aluminum process targeted for double metal ICs.

Machine Technology, Inc. (MTI)

MTI introduced, at last year's SEMICON/West, the AfterGlo CVD system, a downstream 2.45 GHz plasma system for the deposition of undoped oxide. This year, however, MTI did not exhibit the product, and Dataquest believes that only a very few of the systems have been delivered since June 1986. The price of the AfterGlo CVD system is $250,000.

Novellus

Novellus, a venture capital-backed company formed in 1984, exhibited its first product, the Concept One CVD system. (Last year only a model was exhibited.)

The reaction chamber in the Concept One consists of a circular rotating platen with positions for multiple wafers. Each wafer rotates under seven plasma deposition stations, such that the final film is built up from seven sequential depositions. As the wafer completes its deposition sequence, it is transferred back into the cassette in the load-lock, and a new wafer is transferred onto the platen. Thus, the Concept One is a continuous process system.

The load-lock contains three cassettes, and during the time it takes to exchange cassettes in the load-lock, a self-clean cycle can be initiated in the process chamber so as not to affect the throughput of the system. The Concept One has a cycle time of 80 minutes for 75 wafers for an 8000-angstrom film.

The Concept One provides +/-1 percent uniformity (1 sigma), both within a wafer and wafer-to-wafer, on undoped oxide, PSG, and BPSG films. Low temperature (400°C) TEOS oxide, nitride, and planarized oxide processes are under development. All processes on the Concept One are plasma processes. Novellus claims excellent hillock suppression for the system as film deposition begins within 10 seconds after the wafer is brought to deposition temperature.

Price of the Concept One is $550,000. Dataquest believes that the first system was just shipped immediately prior to SEMICON/West.

Plasma-Therm

Last year we reported on Plasma-Therm's new plasma vertical reactor for the deposition of oxides and nitrides. The vertical reactor had a capacity of 25 wafers; this has been increased to 50 wafers per load. Also new is the addition of an oxynitride process. The system is priced at $500,000, and Dataquest does not believe that any systems have yet been sold in the United States.

SVG/Anicon

In February 1987, Silicon Valley Group purchased Anicon for $8.5 million in stock and simultaneously renamed the Anicon operation SVG/Anicon.

Last year Anicon exhibited its new Pro-II CVD system, which was basically the same machine shown this year by SVG/Anicon. However, SVG/Anicon has made some improvements in its quartzware policy; the price has been reduced by 50 percent, and SVG/Anicon will now give the quartzware drawings to the customers to choose their own fabricators.

The Pro-II is still not automated as the automation strategy promoted by Anicon before to its acquisition was not cost effective. Dataquest believes that development activity at Anicon before its acquisition had been moving very slowly. Now that they are under the aegis of SVG, we should see development activity increase, particularly in the area of automation.

The price of the Pro-II is $350,000.

Spectrum CVD

Last year Spectrum CVD, a Motorola New Enterprise Group company, introduced its Model 202 manual system and Model 211 cassette-to-cassette system for the deposition of tungsten silicide, selective tungsten, and blanket tungsten films. The Model 202 ($250,000) is intended for R&D use, while the 211 ($419,000), which uses the same reaction chamber as the 202, is for production use. The 211 has a three wafer load-lock and utilizes continuous processing of wafers in the single-wafer reaction chamber. Throughput is approximately 20 wafers per hour.

First deliveries were made for the 202 in December 1986; several systems have been shipped since then. Deliveries for the 211 were scheduled to begin in December 1986, but first shipments will not actually begin until the end of 1987.

Ulvac

Ulvac introduced, for the first time in the United States, its new ERA-1000 CVD system for the deposition of tungsten silicide, selective tungsten, and blanket tungsten. The ERA-1000 has two reaction chambers, which can be used in parallel to process two wafers simultaneously. Also possible is a sequential mode of operation for multistep processes. For example, for the deposition of two layers, one layer is deposited in one chamber and then moved to the other chamber for a second deposition. Another multistep process would be a plasma pretreatment prior to deposition.

Although selective tungsten deposition rate is a function of deposition conditions, typical rates of 500 to 1500 angstroms per minute are obtained. For an 8000-angstrom selective tungsten film, throughput is 5 to 15 wafers per hour using both chambers. Throughput for an 3,000-angstrom tungsten silicide film is 20 to 30 wafers per hour, also using both chambers.

The ERA-1000 has 200mm wafer capability and is priced at $750,000.

Varian

Last year Varian introduced its Model 5101 load-locked, single-wafer system for the deposition of tungsten silicide, selective tungsten, and blanket tungsten. Varian has delivered several of these systems for R&D use, mostly for tungsten silicide applications. Because of its low throughput, Varian is developing a two-chamber system for use in production. Price of the 5101 is $350,000.

Varian also announced last year that it was developing the Model 5150 hot-wall CVD reactor intended for low-temperature oxides, nitrides, and polysilicon. However, this program has subsequently been put on hold.

Watkins-Johnson

Watkins-Johnson (WJ) exhibited its new WJ-998 CVD system for the deposition of oxides, PSG, and BPSG. The WJ-998, which is a compact version of the much larger WJ-985 continuous belt system, occupies little clean room space, because the entire system, with the exception of the input/output stations, can be installed in the chase area.

The WJ-998, which is an atmospheric CVD (APCVD) reactor, appears to have overcome the limitations of APCVD that were problems in the past. For oxides and PSG, film uniformity on 150mm wafers is +/-4 percent within a wafer, and +/-2 percent wafer to wafer. For BPSG the within wafer uniformity is +/-5 percent. Guaranteed particulate contamination is less than 0.1 particle per cm^2 for particles greater than 0.3 micron. Throughput for a 6000-angstrom oxide film is 96 150mm wafers per hour. Watkins-Johnson is also stressing quality of intermetal dielectric: planarized coverage with no voids and anti-hillock control.

For increased productivity, the WJ-999, a high throughput version of the WJ-998, is available. The WJ-999 has a continuous belt that is wider than the belt on the WJ-998; thus, wafers can be placed side by side on the belt. Throughput for a 6000-angstrom oxide film is 192 150mm wafers per hour, double that of the WJ-998.

The WJ-998 is priced at $550,000; the WJ-999 is $650,000. Several systems have already been shipped to VHSIC contractors.

PHYSICAL VAPOR DEPOSITION

The PVD equipment market includes sputtering and evaporation technologies. In sputtering, the most notable new developments involved planarization of aluminum. At last year's SEMICON/West show only Varian had announced a planarization capability for sputtering. Varian began shipments of the technology near the end of 1986. At this year's show several new contenders entered the planarization arena: Electrotech, Gryphon Products, Machine Technology Inc. (MTI), and Materials Research Corp. (MRC).

Planarized Aluminum is being developed to overcome the topographical problems arising from the demands of micron and submicron line geometries and vias. The most common topographical problems are related to poor step coverage, which can cause electromigration problems and voids in the contacts and vias. With typical sputtering techniques, step coverage ranges between 30 to 50 percent. All manufacturers offering these new planarization technologies are claiming step coverage better than 80 percent. Planarization of aluminum appears to be the PVD answer to filling 1 x 1-micron vias in the near future. Planarization technology will most likely be faced with severe competition for advanced via filling applications by the emerging selective tungsten-on-aluminum CVD processes.

In the evaporation segment of the PVD market, most new evaporators designed for semiconductor applications were being targeted toward the gallium arsenide (GaAs) industry. Of all the semiconductor-related evaporation sales made, approximately 90 percent are being used for GaAs lift-off processing. It has become apparent to evaporation equipment manufacturers that the GaAs industry will drive the semiconductor-related segment of their market in the future.

While the nonsemiconductor-related PVD equipment introductions will not be covered in this section, it should be noted that most PVD equipment suppliers are diversified into other thin film markets. These equipment markets include compact disks, memory hard disks, optics/sunglasses, razor blades, windows/mirrors, flat panel screens, jet turbines, hybrid circuits and solar cells. At SEMICON/West there were many new pieces of equipment designed for compact disks and memory hard disk sputtering. The vendors at the show indicated that these markets have enjoyed robust growth.

The PVD product introductions in the following section cover only new products that have been introduced since SEMICON/West 1986 and existing equipment with significant product enhancements. All of the equipment mentioned in this section are also production-oriented equipment.

Alcatel

Alcatel, previously only a European vendor, has now decided to market its products in North America. Sales, service, plus a demo lab are now available in San Jose, California. Two products are now available in North America, the LINA 350 and the PUMA 500.

The LINA 350 is a horizontal, in-line sputtering system. The system has a throughput of 50 to 60 wafers per hour, and can coat substrates up to 400mm x 550mm. The deposition module is capable of single deposition or multilayer modes. Three types of deposition can be performed with this machine: reactive sputtering, RF bias sputtering, and co-sputtering. The deposition chamber can be set up to run one to four rectangular DC/RF magnetrons. The system is being used in Europe for the production of ICs, hybrid circuits, disks, flat panel screens, sensors, and solar cells. The price of the system runs between $500,000 and $750,000, depending on the system configuration.

The PUMA 500 is a magnetron, horizontal batch load, sputtering system. Operation modes include sequential sputtering and co-sputtering. Wafer batch capacity is 17 3-inch wafers, 9 100mm wafers, or 7 125mm wafers. Throughput is 35 wafers per hour; the price ranges from $275,000 to $400,000. This system is being used in Europe to produce ICs, optics, and compact disks.

Balzers

Model BAK 640 SC is a new evaporation system designed primarily for GaAs lift-off processing. The system is equipped with a split chamber, which allows the source to remain isolated and under constant vacuum during the loading, evacuation, substrate heating, or RF etching and venting phases. This chamber configuration is said to greatly improve the results when doing highly contamination-sensitive metalization processes such as lift-off technology. Two-inch or 3-inch wafers can be processed in this machine. In addition to the lift-off processes, other applications include interconnect, multilayer systems, silicides, wafer backside metalization, dielectric layers, power devices and contact layers for bonding.

Circuits Processing Apparatus (CPA)

CPA featured the C/C 100, a cassette-to-cassette sputtering system designed for single loading and unloading of wafers up to 150mm in diameter. Operation is completely menu driven. Throughput of 120 wafers per hour for 1-micron deposition using four targets is possible. It processes wafer sizes up to 150mm, with an optional 200mm wafer package available. The wafers are held at a near-vertical position on the outside of a carousel that continuously rotates as it loads and unloads. Film uniformity is within +/- 3.5 percent, and either RF or DC bias can be used. Price of the system is between $600,000 and $700,000.

CVC Products

Some improvements were made to the Model 2800, including an improved robotic arm that has increased throughput. The system is now equipped with a menu-driven system. Also available is a new third-chamber option, retro-fittable to installed 2800 systems. The third-chamber option will increase

throughput from 60 to 100 wafers per hour for 100mm wafers for a 1-micron film of Al/Si. The third chamber modifies the system into a true continuous process. The price for the two-chamber system is $500,000; that for the three-chamber system is $600,000.

Electrotech

The successor to the Model MS6200 sputtering system was introduced this year as the Model MS6210. Throughput for the new system is 96 wafers per hour for a deposition of 1.2 microns of Al/Si. The system can handle wafers from 3 inches to 150mm. The MS6200 is now offered with a RF bias option that provides a lower temperature reflow than the competition. With this option planarization and filling of contact holes 1 micron deep by 1.2 microns wide with 1 micron of Al/1%Si can be obtained. The eight-chamber, multitarget design allows cosputtering of barrier layer materials. The MS6200 basic system cost is $620,000. Electrotech also offers the model MS8200 sputtering system which can process wafers from 125mm to 200mm.

Gryphon Products

Gryphon Products announced its new product called the Horizon. This system is fully automated and provides true planarization of aluminum and aluminum alloys. The Horizon uses a proprietary low-temperature process that can planarize features of 1.5 microns and less, while not exceeding 360°C. Dual chamber, parallel batch processing is offered with single-wafer tracking. Gryphon Products sees temperature control as a critical factor for maintaining the quality, accuracy, and repeatability of a sub two-micron process. With the Horizon, the user can control the temperature of the growing film within +/-20°C.

The Horizon will handle wafers from 3 inches to 150mm and will provide step coverage uniformity of +/-5 percent over an entire 150mm wafer. System throughput ranges from 90 100mm to 50 150mm wafers per hour. The chamber is configured with three targets that sputter down. The chamber processes 12 100mm, 10 125mm, or 8 150mm wafers. The Horizon is priced at $1.25 million.

Machine Technology, Inc. (MTI)

The SypherLine sputtering system can now planarize aluminum films over severe geometrical structures. MTI is guaranteeing +/-4 percent uniformity over 200mm wafers (3 sigma). Throughput is 40 wafers per hour for deposition of 1-micron aluminum films. MTI's planarization process is based on a combination of geometrical, thermal, and ion bombardment effects. Deposition rates exceeding 1 micron per minute are being achieved without high-temperature heating of the wafer and without DC/RF bias. The wafer size range for the SypherLine is 100mm to 200mm.

Materials Research Corp. (MRC)

MRC now offers planarization of aluminum as an option for the ECLIPSE sputtering system. This optional process is capable of via filling for submicron geometries. MRC claims thickness uniformity of +/-5 percent using RF bias, tight control over wafer temperature, and a low base volume. Throughput for Al/1%Si at a temperature of 530°C is 25 wafers per hour for a 1-micron deposition.

Temescal

Temescal has been integrated into Edwards High Vacuum International. Temescal introduced a Ultra High Vacuum (UHV), linear, four-pocket, E-gun source. This E-gun source has been developed for molecular beam epitaxy (MBE) vendors to the GaAs industry. The source is conflat flange mounted and is available now.

Ulvac

The ISOVAP-400 load-lock evaporator is designed to handle wafers from 2 inches to 200mm. The system can handle wafers using single dome or planetary motion systems. For lift-off processing which requires the single dome, the chamber can process 99 3-inch GaAs wafers per batch. A menu-driven touch-screen system is available. The price is $300,000.

The MCH-9800 sputtering system is an improved version of the MCH-9000 that Ulvac introduced last year. The 9800 is equipped with eight in-line chambers, compared with six last year. The two additional chambers allow for isolated heatup and cooldown modes. The chamber process sequence is load/pump down, heatup, four sputter chambers, cool down, and unload. The 9800 has a throughput of 50 wafers per hour, up from 35 last year. The throughput was increased by pumping down one wafer at time in a very small chamber, as opposed to pumping down an entire cassette. The MCH-9800 can process 125mm and 150mm wafers and is priced at $1.2 million.

Varian

The XM-90 sputtering system has replaced the XM-8. The XM-90 has all the features of the XM-8, plus expanded flexibility, process recipe control, and backside substrate heating. The addition of a microcontroller allows precise set and control of load-lock pressure, deposition time, deposition power, and substrate heater temperatures. The system allows separate control of the four in-line process stations, plus the capability of depositing three separate times in a single process station. The features allow the user to interlayer sputtered films reactively and nonreactively. Varian also introduced a backside, gas conduction substrate heater option for the XM-90. This option is also available as a retrofit for the XM-8. The XM-90 will operate with DC or RF bias. The price of the XM-90 is $350,000.

Varian now has 8 to 10 3290 sputtering systems installed that use Varian's Viafill planarization process. These systems are now planarizing aluminum over 1 x 1-micron steps. The Viafill process can be tweaked at Varian's demo labs for each customer's requirements before the system is shipped. Varian is working with NTT on a reduced-heat planarization process. Sputtering applications for titanium nitride are also being developed by Varian.

EPITAXY

Silicon Epitaxy

The market for epitaxial reactors has been very weak during this recessionary period. It has been one of the hardest-hit of all front-end equipment segments because of the poor demand for bipolar devices. Total industry sales fell 55 percent from $101 million in 1984 to $46 million in 1986. To exacerbate the situation, the expected usage of epitaxy in CMOS processes simply has not materialized. Extreme over-capacity continues to exist.

Several companies have devoted valuable resources to product development in an attempt to be early winners in the CMOS epi market. Such an investment was necessary because the previous generation of epitaxial reactors were not cost effective for the fabrication of commodity devices such as DRAMs. Companies with appreciable investments in silicon epitaxy for CMOS processing include Applied Materials, Gemini, Anicon, and Epsilon Technology, Inc. (a limited partnership with ASM America as the principal investor).

Only two of these companies have brought a system to market: Applied Materials and Gemini. Anicon's system, announced at SEMICON/West last year, has been tied-up by the acquisition of Anicon by Silicon Valley Group. (The product was developed within an R&D partnership from which investors must recoup their investment before the product is marketed.) Epsilon has told Dataquest that its product will be introduced in third quarter 1987. We believe that it will be a single-wafer system using multichambers, or rapid thermal processing.

Of Applied and Gemini, Applied's system has had nearly a year head start. Because of the market softness, this delay has not cost Gemini any market share. Both systems are poised to take advantage of the incipient industry up-turn. The market for epitaxial wafers is increasing, and silicon wafer vendors are nearly at full production capacity. However, these companies are purchasing reactors of the old vintage, which requires them to sell the product wafers at prices too high to be used for commodity devices. However, the epitaxial wafers produced on these systems can command a premium because they are being used for high-end devices, such as microcontrollers in the U.S. and for charge-coupled devices in Japan. Dataquest believes that the 1Mb CMOS DRAMs and the concomitant CMOS devices that follow, will use epitaxy layers. These epitaxial layers must be processed on the new generation of reactors.

Gemini

Gemini did, however, introduce its third-generation vertical reactor, the Gemini III. The Gemini series has been very successful in wrestling market share away from Applied Materials for very thick films and for less critical films. This is because the system uses two bell jars and tends to be more cost effective for those processes. The series uses a heated graphite susceptor, as opposed to the radiant heating technique of Applied Materials. The heated-susceptor technique tends to be more susceptible to slip faults in the crystal structure, which positions Applied as the vendor of choice for advanced films.

Applied Materials has been able to maintain its dominant position, capturing nearly 70 percent of the market in 1986. However, Gemini hopes to gain share in the bipolar market with its new product. The Gemini III has included a metal can around the bell jar to reflect the heat back into the chamber. This will tend to flatten the temperature profile and reduce slip. Its uniformity guarantee is now +/-1.5 percent (1.6 sigma). It has added robotic handling to reduce the need to rely on an operator. This should increase the productivity of the system. It has also added the ability to process at pressures as low as 80 torr.

The system price is $1.1 million, fully loaded. The Applied Model 7810, priced at approximately $800,000, was essentially the same price as the previous Gemini version, the Gemini II. Applied overcame the throughput disadvantage with excellent marketing, applications support, field service, and process quality. This new price structure essentially reduces the productivity advantage that Gemini previously enjoyed.

Molecular Beam Epitaxy

ISA Riber introduced a chemical beam epitaxy system, and Varian showed its Modular GEN II MBE System for the first time. Chief features of these systems were increased throughput, better yields, decreased downtime, and enhanced manufacturing flexibility.

ISA Riber

ISA Riber announced, although it did not exhibit, a chemical beam epitaxy (CBE) system, the CBE 32. Chemical beam epitaxy is a technique that combines features from both molecular beam epitaxy (MBE) and metalorganic CVD (MOCVD). Traditional MBE uses a solid source, while CBE uses a gas source such as that used in MOCVD. The advantage of a gas source in CBE is increased cleanliness and a more abrupt interface between the epitaxial layer and the substrate. ISA Riber has already delivered a CBE 32 to Bell Labs in New Jersey and has orders for the system in Europe, Japan, as well as the United States. The price of the CBE 32 starts at $750,000.

ISA Riber also introduced a new solid arsenide cracker source for its MBE 32 system. This new solid source enhances the sticking coefficient of arsenide, which reduces downtime because the source need not be reloaded as often as previously.

Varian Associates, Inc.

Varian showed its Modular GEN II MBE System for the first time as a complete unit. The new system is modular and thus allows users greater flexibility in selecting an MBE for particular process requirements. The new system has a new entry/exit chamber that allows outgassing of up to 16 wafers at once for improved throughput. The modular configurations use a unique trolley cassette wafer handling system that travels from one chamber to another in a vacuum; it is not necessary to house the entire system in a clean room environment, only the entry door. The new system handles up to 3-inch wafers, has a new silicon wafer heater in the buffer chamber, and has larger effusion cells to provide longer periods between cell changes.

Varian believes that perhaps the most significant feature of the new system is the nonindium bonded wafer holder. This new holder holds the wafer with minimum strain and also yields temperature uniformity of better than 5°C over the exposed wafer area.

Metalorganic CVD

New systems, new generations, and enhancements were the order of the day in metalorganic CVD. Crystal Specialties introduced a new system, Emcore showed its new growth chamber, and Cambridge Instruments offered a new enhancement. The focus of enhancements and improvements was to bring MOCVD out of the R&D environment and into a production environment, and to increase yields.

Cambridge Instruments, Inc.

Although Cambridge did not show its MOCVD system, it has added load-lock capability on its MO102 system. This load-lock will allow the system to be pumped down without as much purging as before. Cambridge now has a cadmium mercury telluride (CMT) cell for its MOCVD system. This CMT cell is now undergoing beta site testing.

Crystal Specialties, Inc.

Crystal Specialties introduced the Model 411 MOCVD system. The 411 is a production system which features a new radial injection head to minimize gas residence time. The 411 also has four chambers within the growth chamber (one within the other) to minimize chamber volume, and thus, achieve thinner layers and more abrupt junctions. Additionally, the 411 features a magnetically coupled wafer carrier rotation system that eliminates O-rings to minimize leaks and seal maintenance. The 411 also features a new load/unload station with a pure nitrogen glove box.

Emcore

Emcore displayed the GS3300M MOCVD system. This system features the semiautomated load-lock for processing up to 12 3-inch gallium arsenide wafers per load. A load-lock can significantly cut production time. New wafers can be loaded and pre-heated for insertion while the growth chamber is in use. Finished wafers can be unloaded into the load-lock, thus the system need not be shut down between runs. The load-lock also cuts down on production time since it eliminates the need to manually insert wafers after each run. Loading wafers without exposing the reactor chamber to atmospheric impurities reduces particulate.

Emcore also introduced the Emcore Toxic Gas Absorber to remove hazardous emissions from semiconductor process effluent.

DIFFUSION

This section of the SEMICON/West newsletter contains new product and feature information for horizontal and vertical tube diffusion furnaces, and the associated LPCVD processes. It also discusses horizontal tube plasma enhanced CVD equipment (PECVD).

Almost all introductions in the vertical and horizontal tube markets were focused on robotic wafer handling capability and software automation. As fabs produce larger wafers the diffusion area is being driven to robotic loading due to the sheer weight of quartz boats, which hold up to 200 wafers. Almost every vendor in the diffusion market now sells 200mm robotic wafer-handling capability.

In the horizontal tube PECVD market, only ASM had a new introduction. ASM introduced a system with a very small footprint targeted towards the ASIC and R&D market.

ASM America

The System 250, a horizontal tube furnace, is a low-pressure chemical vapor deposition (LPCVD) system that processes 150mm wafers and is now available in the United States. System 250 is offered with a fully automated cassette-to-cassette material management system. Quartz tubes of up to 235mm inner diameter can be used to accommodate advanced LPCVD processes. Standard process guarantees are offered for silicon nitride, HTO, TEOS, LTO, and in-situ doped polysilicon. ASM has developed dedicated quartzware, quartz injectors, in-tube temperature measurement, and special gas systems for these processes. Also available with System 250 is ASM's Stand-Alone Tube Controller (SATC II), based on the Motorola 68000 microprocessor. Each tube is controlled by its own SATC II. Up to 250 user-defined steps can be accommodated. The System 250 is priced at $400,000 to $700,000, depending upon options.

The SF-50 is a PECVD system. It is designed with a very small footprint ($15ft^2$) and is intended for ASIC, moderate-volume production and R&D applications. The SF-50 can process wafers from 3 inches to 200mm. Throughput is 30 wafers per hour for a 1-micron nitride film. The price of the SF-50 is $200,000.

BTU Engineering

The Series 2000 Automated Material Handling System is a wafer handling robot for horizontal tube diffusion furnaces. This system is capable of automatic tool changing for processing 100mm to 200mm wafers. The module is fully enclosed in a free-standing structure that maintains a class 10 environment. First deliveries of the system will begin during the third quarter of this year. The price of the Series 2000 is $450,000.

A compact cassette-to-cassette loading module was also being demonstrated. The module consists of a two-axis elevator combined with a mass transfer system and an integrated controller. The system provides wafer handling and tube loading for the BTU models BDF-4 and BDF-41 vertical tube systems. The loading module is designed to occupy aisle space formerly needed by the operator. Operator tasks are reduced to supplying and removing product in plastic carriers, removing and supplying empty carriers between transfers, and initiating process cycles at the tube controller. The loading module can change the spread of wafers in the boat and uses slot sensors for precise wafer placement. Load capacity is 200 wafers for sizes of 75mm to 150mm. The price of the system is $145,000.

BTU also has phase one of its APEX software product line available. The software is based on the Apollo workstation and permits the user to manage diffusion tubes or to integrate wafer processing systems with related equipment in a flexible manufacturing cell architecture. The system is compatible with Bruce Systems' automated material handling modules. APEX offers an optional SECS host communications link and is consistent with CIM/MAP cell architectures.

Dainippon Screen

Brochures for the vertical furnace were available at the show for the first time. Although the brochure is sketchy, it appears that Dianippon may begin to market the system in the U.S. The system is designed to automatically load the wafers into the quartz cassette, and then load the cassette into the furnace. The system is designed to operate in the 200°C to 600°C range and has an effective heating length of 300mm.

Gasonics

Gasonics is the only U.S. supplier of high pressure diffusion furnaces. The system is now capable of processing 200mm wafers and is equipped with two tubes per unit. The basic system price is $800,000. The system equipped with the Wafer Robotic Automation Package (WRAP) has a price of $1.5 million.

Process Technology Limited (PTL)

As an improvement to its LPCVD system, PTL has developed a reduced temperature, all liquid source process for the deposition of BPSG films. Undoped oxide, PSG, and BPSG can all be produced with this process. Successful depositions of BPSG have been performed at temperatures below 575°C with deposition rates competitive with conventional hydride processes. The price per tube is $100,000.

PTL now has a wafer carrier handling system available for demonstration. The system is based on a scaled-down model of a robot used in the motion picture industry. The system is strong enough to handle full 200mm wafer quartz boats. The entire system breaks down into sections five feet long or less. The system allows installation in any floor plan, requires no wall moving and will fit through standard fab doors. The system can be equipped with three-axis or five-axis robots and is Class 10 compatible.

Semitherm

Semitherm displayed its vertical tube reactor for diffusion and/or LPCVD processing. The system can process up to 100 150mm wafers at a time. Key benefits of the system include the low-temperature processes and the total control of the process atmosphere during heatup and cool down. Wafers can be processed both vertically and horizontally. The price for the diffusion process is $100,000; the LPCVD process costs $140,000.

Silicon Valley Group (SVG)

The SVG vertical tube reactor (VTR) is now equipped with 200mm wafer automation capability. SVG now guarantees less than 0.01 particle per cm^2 larger than 0.4 micron. SVG is also guaranteeing 10,000 operations without failure. The price of the diffusion VTR is $170,000; the LPCVD VTR is $190,000.

Tempress

The Tempress VR-2000 VTR is now available for shipment. Bottom-up loading is intended to minimize contamination and heat loss. The loading chamber is class 10. The system operates continuously at temperatures between 1250°C and 1350°C. The price for the diffusion process is $150,000; the LPCVD process costs $200,000.

Tempress also exhibited its direct digital controller, which is designed to control temperature and process parameters during diffusion and LPCVD operations. The system features a simplified touch-screen flat panel control for easy data input and user-friendly operation. The system can be linked to a host computer manager and is SECS I/II compatible.

Thermco

The model HLF 5110 Laminar Flow Load Station is designed to be used in conjunction with the 5000 series Thermco four-stack diffusion/LPCVD furnace. The load station is compatible with various cantilever loading systems. This station offers full robotic cassette-to-cassette handling. The system handles wafer transfer from plastic to quartz and back-up boats. Test wafers and solid source wafers can also be automatically loaded. The price of the system is $450,000.

A symmetrically exhausted scavenger exhaust system designed to carry away heat and process gases is available with the load station. The scavenger includes a method of adjusting the air flow velocity without changing the symmetrical, exhausting pattern around the tube. The symmetrical design reduces trapping of particles in the scavenger and also reduces particle-laden, turbulent swirl across the wafer surfaces during insertion and extraction of the load. The price for the load station is $55,000

RAPID THERMAL PROCESSING

In rapid thermal processing the emphasis seemed to be in "application-specific" equipment in an attempt to broaden the applications for this type of equipment. AG Associates introduced a low-temperature machine for contact alloying. Peak introduced a system for thin film deposition. Eaton, which finally repackaged its unit into a more reasonable size, added mass flow controllers and vacuum capability to the new system.

The market for rapid thermal processors is expected to have high growth rates. There was little growth in 1986 sales, however, mainly because of the semiconductor recession, and because we have yet to see the movement of rapid thermal processors into the production environment.

AG Associates

Last year AG introduced its first "application-specific" system, the Heatpulse 2146 Oxidation System, to meet thin film requirements in oxidation, nitridation, or annealing applications. This year AG introduced another application-specific system, the Heatpulse 2126 Contact Alloying System, specifically designed for low-temperature contact alloying of aluminum and other materials in silicon and gallium arsenide applications.

The Heatpulse 2126 has a temperature range of 400°C to 700°C with a maximum temperature ramp-up rate of 100°C per second. The 2126 uses a proprietary, low-temperature pyrometer which measures the temperature of the wafer through quartz. Compared with a typical diffusion furnace anneal, a Heatpulse 2126 alloy cycle of 5 to 10 seconds at 400°C to 500°C will reduce spiking by as much as 90 percent, and eliminate hillock formation.

The system can handle up to two noncorrosive gases. Unlike the other AG rapid thermal processors that use upper and lower banks (each of 11 lamps) the 2126 uses a single bank of eight lamps. The price of the 2126 is $144,000.

Eaton

Eaton introduced the ROA-500 rapid thermal processor, which is essentially a repackaged version of the ROA-400. The ROA-400 had a very large footprint of 63 ft^2, while the new ROA-500's footprint is 33 ft^2. The newer system uses the same 100kW lamp with the same temperature specifications, but has provision for handling up to six corrosive gases.

The price of the ROA-500 is $240,000. First deliveries are scheduled to begin at the end of 1987.

Peak Systems

Peak, a start-up company formed in 1983, exhibited its first product, the ALP 6000, at last year's SEMICON/West. This year Peak exhibited its new Model 6500, which uses the same 35kW lamp as the 6000, but is specifically designed for deposition of thin films. Typically, the thin films deposited in the 6500 would be less than 800 angstroms. It has eight mass flow controllers (the 6000 uses rotameters) and has vacuum processing capability.

Dataquest believes that more than a dozen 6000s have been delivered since last May and that one 6500 has been shipped. The 6500 is priced at $250,000.

Thermco

Last year Thermco made the U.S. introduction of the LA-14AD rapid thermal processor manufactured by TEL/Thermco in Japan. Thermco did not have the system at this year's SEMICON/West, Dataquest believes that the reason for this is that the LA-14AD may still be undergoing debugging.

ION IMPLANTATION

SEMICON/West saw the debut of an new player in the ion implantation market--ASM America--and the introduction of a new system from National Electrostatics. In addition to new players or systems, most of the established players in the market showed systems with improvements in contamination control, automation, yield enhancements, smaller footprints, or wafer handling.

Applied Materials

Applied showed the process wheel of its 6000 for the first time at SEMICON/West. The wheel can hold 25 wafers per batch. The company believes the process wheel has several advantages over the process disk, since it eliminates cross contamination and aluminum contamination. The 6000 is designed to operate at less than 80°C, and Applied claims that it processes wafers in the 45°C to 50°C range because the beam is spread over a large batch size.

In addition to the 25 wafer batch process wheel, the 6000 features automatic wafer handling, automatic setup and conditioning, closed loop beam-line and incipient warning and failure diagnostics. The price of the 6000 is $2.2 million. Shipments began in 1986.

ASM America

ASM America introduced the ASM-220 medium current serial process ion implanter. This is a fully automated system that is optimized for small geometries and wafer sizes up to 200mm. The 220 was designed as a serial wafer processing system in order to minimize the number of wafers at risk at any one time. This system uses a unique parallel-beam scanning technique which ASM claims minimizes nonuniformity from shadowing and channeling due to implant angle variations.

The 220 also features a proprietary in situ dose monitoring and correction system that records the dose accumulated on each pass and corrects errors during the implant. By using fiber optics whenever possible, ASM claims that it has eliminated a major source for high voltage transients throughout the system.

The 220 also features easy-to-use touch screen graphics with color display. The machine initiates automatic setup and optimization of all beam parameters, including ion sources.

The price of the 220 is $700,000.

Eaton Corporation

The NV6200, a medium-current implanter, featured a new adjustable implant angle that can be varied from 0 to 10 degrees.

The NV20, high-current implanter featured a new improved wafer handling system that features little or no wafer breakage. The new system is a pick-and-place system with wafer position feedback. The NV20 is made in Japan by Sumitomo/Eaton, a joint venture. The NV20 was first introduced in Japan in early 1987 and was introduced into the United States at SEMICON/West. The NV20 also features a single chamber that is tilted at 45 degrees for a smaller footprint on the cleanroom floor. The chamber also features a faster pump speed for better handling of photoresist outgassing. Eaton claims that the NV20 can handle 100,000 wafers without breakage.

Eaton also showed the NV200 Simox oxygen implanter for silicon on insulator technology. This system was designed to be used for 16- and 64-Mbit DRAM production.

Eaton also introduced the SKM Medium Current Ion Source. This source can provide a boron beam current in excess of 1mA and delivers a fourfold increase in doubly charged beam currents. Eaton believes that the SKM sources offer the highest beam currents available in the medium current marketplace. The SKM can be used for the NV6200, NV4200, and NV3200 ion implantation systems.

National Electrostatics Corporation (NEC)

National Electrostatics announced a new 2 MeV production implant system, the Model MV-H20. The H20 is designed for the production processing of silicon wafers and can deliver ion beam energies that range from below 300 keV to above 2000 keV for singly charged ions. This system will implant phosphorus ions to the same depth in silicon as 800 keV boron ions. National Electrostatics has quoted prices for this system but has not yet delivered a system.

National Electrostatics also introduced a batch wafer handler for its MeV production ion implantation system. This mechanically scanning, batch wafer handler increases the throughput of the NEC high-energy ion implanter to 300 wafers per hour. It is equipped with a unique beam monitor control which eliminates inaccuracies due to beam neutralization. The wafer handler is retrofitable on existing NEC high energy implanters.

Nissin Electric Company, Ltd.

Nissin had no implanters at SEMICON/West. It did, however, announce its new STAR (Selectable, Tilt, Adjustable, Rotational) end station. The STAR features a self-spinning platten with a 0 to 60 degree tilt and deep well trenching with uniformity of 0.5 percent. Nissin is now taking orders for the STAR.

Varian Associates, Inc.

While Varian did not introduce any new systems, it did show some interesting new enhancements and improvements to its existing systems. The 160XP medium current implanter has a new automated loader which can handle 100mm to 150mm wafers. This new loader features automatic orientation of the wafer.

Varian has reduced the number of parts by two-thirds on the 160XP's disk drive for both increased reliability and easier maintenance. Additional new features on the 160XP include: an improved seal in the faraday cup valve, improved beam spot size control, and an improved electron flood gun. The 160XP can be run either manually or automatically.

The 300XP high-current system has new software to check auto-cyclying. The 300XP specifications now include breakage: one broken wafer in 20,000, with a 70 percent confidence level. It has been designed to contribute no more than 0.1 particle per cm^2 for particles greater than 0.5 micron.

WAFER INSPECTION

In today's semiconductor industry, line geometries are shrinking, while device complexity, processing steps, and mask levels continue to increase. In response to requests for smaller, smarter, and faster measurements, new generations of wafer inspection tools are being developed to meet the

requirements of advanced device processing technology. Wafer inspection currently is making a transition from operator-intensive inspection and measurement systems to fully automated tools as the semiconductor industry looks to automate its manufacturing processes. Accordingly, the price of wafer inspection tools has also increased, and in some cases has reached the price of a wafer stepper at approximately $1 million.

This portion of the newsletter examines new equipment introductions and enhancements in the area of wafer inspection, with particular emphasis on automatic critical dimension (CD)/linewidth and defect inspection systems. Some selected information on new equipment announcements and enhancements in other areas of process control, such as film thickness measurement, mask metrology, resisitivity mapping, and surface defect inspection is also presented.

Critical Dimension And Defect Inspection Equipment

Cambridge Instruments

Cambridge Instruments introduced its Microcheck 1 and Polycheck critical dimension measurement systems. The Microcheck 1 is a completely manual tool with applications in optical linewidth and overlay registration measurements. The price is approximately $60,000. Several systems have been installed at semiconductor manufacturers' facilities in the United States in the last year. The Polycheck is a fully automated CD measurement system and provides measurement capability down to 0.5 micron in addition to macro measurements of larger dimensions. The price of this system is $115,000. There are no deliveries of the Polycheck system at this time.

The Polycheck VLSI was also exhibited at the show, although the formal introduction of this system will be at SEMICON/East in September. The Polycheck VLSI is a fully automated CD measurement system with pattern recognition and auto-align capability. This tool has a four-cassette material handling system with 200mm wafer capability. The system displayed at the SEMICON/West show was a second-generation prototype tool. The price of the Polycheck VLSI is approximately $170,000. The Polycheck VLSI has been designed specifically for wafer inspection applications in the semiconductor industry in contrast to the Microcheck 1 and Polycheck systems, which have cross-industry applications.

Cambridge Instruments introduced its automated Scanline-CD Electron Optical Comparator at SEMICON/West this year. The nondestructive electron-beam comparator can measure linewidths from 0.1 to 30 microns and has a throughput of 12 wafers per hour at five sites per wafer. The Scanline system has cassette-to-cassette automatic wafer loading, and the price of the system is less than $200,000.

Heidelberg Instruments

Heidelberg Instruments introduced its fully automated, LPM Line Profile Measurement system. The LPM is a confocal laser scanning microscope designed for three-dimensional measurement of line geometries with measurement capability down to 0.3 micron for linewidth and 0.05 micron for lineheight. Typical throughput for 150mm wafers is 30 wafers per hour based on 10 chips per wafer, 5 measurements per chip. The LPM was first introduced at SEMICON/Europa in March 1987, and the first system was shipped to Siemens in late May. Additional orders were received in mid-May. The price of the Heidelberg LPM system is $340,000.

Heidelberg Instruments was formed in 1984 by five researchers from Heidelberg University and four industrial partners. One of the major investors in Heidelberg Instruments is E. Leitz, a West German manufacturer of wafer inspection and mask metrology equipment for the semiconductor industry. Other products from Heidelberg Instruments include laser scanning microscope systems for biological, chemical, and medical applications.

Insystems

Insystems introduced its Model 8600 wafer defect inspection system, a fully automated, full wafer, submicron defect detection tool that utilizes holography and spatial filtering technology. The Model 8600 has been designed for in-process patterned wafer inspection, and can inspect an entire wafer surface for defects in less than 30 minutes. This is in comparison with the several hours required for conventional optical- or SEM- (scanning electron microscope) based inspection tools. This reduction in measurement time is achieved because the Model 8600 relies on parallel optical processing rather than a serial analysis of the wafer on a die-by-die basis.

The Model 8600, with up to 150mm wafer capability, can detect submicron defects in high-density, repetitive areas in single and multiple-process levels in photoresist; oxides; polysilicon; metal; and other films, such as nitride, phosphosilicate glass, and polyimide. The Model 8600 is priced at slightly more than $1 million. Insystems first introduced the tool at SEMICON/Europa in March 1987. The Model 8600 was in beta site during 1986, the first systems were shipped in the May/June time frame of 1987.

Insystems, founded in 1981, is a privately held company. Insystem's first product was the Model 8405 Automatic Photomask Inspection system. The first unit, at a price of $800,000, was shipped to Motorola in April 1986. Insystems views the Model 8405 as an interim product and plans to focus on wafer inspection as its primary market.

IVS, Inc.

IVS, Inc. introduced a fully automated, cassette-to-cassette, CD/linewidth and registration alignment measurement system. The AccuVision 4 (ACV4), priced at $250,000, utilizes digital image processing techniques to enhance the signal-to-noise ratio, and achieves a linewidth resolution down to 0.3 micron with 0.003 micron repeatability. The ACV4 has a throughput of 35 wafers per hour at five sites per wafer. The first shipment of the ACV4 is expected to go to a semiconductor manufacturer in Texas in the third quarter of 1987.

IVS first introduced its AccuVision family of digital imaging process tools at SEMICON/West 1986. The AccuVision family currently includes the ACV, ACV1, ACV2, ACV3, and ACV4 which range in price from $50,000 to $250,000. The AccuVision systems are modular in hardware and software design, and each member of the AccuVision system can be upgraded to the next system level without price penalty.

In addition to linewidth and registration alignment measurement, the IVS tools also provide defect detection, inspection, and analysis. To implement this function, the operator identifies a given area of the wafer as a "golden" image. Then the system, with its pattern recognition capability, performs a comparison analysis of selected portions of the wafer with the "golden" image. The difference between the two digitized signals is presented on a color monitor--areas in red represent what is present on the wafer but should not be, while areas in green identify what is missing on the wafer but should be there.

IVS, Inc. received its first round of venture funding in early 1985. The first investors were Charles River Partners, First Chicago, and Turner Revis. IVS received a second round of venture financing for $2.3 million in March 1987 from Memorial Drive Trust, Venture Founders, and Zero Stage Capital Corporation.

KLA Instruments

At SEMICON/West this year, KLA Instruments introduced a software enhancement for its KLA 2020 Wafer Inspector. The software package, known as KLASS, is an applications package for optimizing stepper setup parameters. The software loads on the KLOUT (KLA Utility Terminal) computer system which is used to collect and process data from the KLA 2020. The software package is priced at $20,000.

The KLA 2020 is an automated in-process wafer inspection system which integrates CD, registration, and area measurements with defect monitoring and macro inspection. The KLA 2020 was introduced in 1984 and the first systems were shipped in February 1985. The price of this system is approximately $1 million.

At the show this year, KLA also displayed the KLA/Holon 2711, a low-voltage, electron-beam, submicron metrology system designed for automated critical dimension and registration measurements. Its primary application is in the characterization of process parameters in the initial stages of process development and for process control monitoring as device volumes increase. Wafer throughput is about 20 wafers per hour at five sites per wafer, and the system can handle 100mm through 200mm wafers. This nondestructive measurement system has a precision less than or equal to 0.05 micron (three standard deviation) for automatic CD measurement. The price of this system, depending on options, is less than $500,000. The KLA/Holon 2711 is the first product to be introduced under an agreement announced in November 1986 by KLA and Holon Co., Ltd. of Japan. KLA is the exclusive distributor of this product in the United States and Europe.

Nanometrics

Nanometrics introduced the Model 400 Linewidth and Registration Measurement Station at SEMICON/West this year. This fully automated, cassette-to-cassette tool provides both bright field and fluorescence measurement capability for CD and overlay registration measurements. The price of the Model 400 is $150,000, which includes material handling capability. Wafer throughput for the fully automated system is approximately 20 wafers per hour at five sites per wafer. The fluorescence capability of the Model 400 tool is specific to fluorescing resists. Nanometrics has demonstrated a performance of 5 percent precision on 0.4 micron measurements when operating in this mode. Nanometrics has developed a proprietary CCD (charged couple device) camera to collect the characteristically weak fluorescing signals. The Nanometrics Model 400 tool shown at the show this year is a post-engineering prototype system.

Nanometrics also introduced the Model 51, a fluorescence CD measurement system. This is a manual version of the Model 400, and utilizes a scanning PMT (photomultiplier tube) to form a high-resolution reflectance profile. The Model 51 has programmable sensitivity and 200mm wafer capability. This microscope-based system is priced at less than $45,000.

Optical Specialties, Inc.

Optical Specialties, Inc. (OSI) announced several new products at SEMICON/West this year. In the category of defect inspection, OSI announced its Micropatterning Process Control System. The new system is designed to perform a variety of tasks without operator intervention. The tool automatically receives wafers from robotic material handling equipment, reads the wafer's identification code (alphanumeric optical character reader), creates a wafer pattern array map, performs macroscopic defect inspection and classification, reads the photo mask layer identifier (optical character verification), measures registration overlay and linewidths, detects and classifies microscopic defects, and displays macro or micro images and test data. The OSI systems uses proprietary software algorithms for defect inspection and classification.

The Micropatterning Process Control System has been designed for use in the production environment as well as for the setup and qualification of new processes. The equipment can handle 100mm through 200mm wafers. The system will be in beta site during fourth quarter 1987. First product shipments are expected in first quarter 1988. The tool's target selling price will be approximately $500,000.

The second new product announced at the show this year is the MV-360CD, a fully integrated linewidth and defect wafer inspection system. The MV-360CD combines the functionality of two existing OSI tools: the Video Linewidth System (VLS-I) and the Microvision 360 (MV-360). The system features a robotic wafer handling system which is characterized by a very low contaminant count, as verified by VLSI Standards, a contamination analysis firm in the Silicon Valley. The price of the MV-360CD is approximately $120,000. Several systems have been shipped.

The third product announcement from OSI this year is an applications software package, the Metrology Analysis Program I (MAP-I), which is used to optimize stepper/aligner operating parameters. The software analysis package operates on a dedicated IBM PC, XT, AT or compatible system and receives measurement data from OSI's MV-PLUS, a fully automatic optical linewidth system. The MAP-I software package for OSI's MV-PLUS is priced at $20,000.

SiScan Systems

SiScan Systems displayed the SiScan-IIA wafer measurement system this year at SEMICON/West. The SiScan-IIA, like its predecessor the SiScan-I, utilizes confocal scanning laser technology to measure registration overlay and critical dimensions of circuit features including metal layers, nitrides, and photoresist. The SiScan-IIA was designed to measure and inspect submicron circuit features in a Class 10 clean room environment. SiScan-IIA system enhancements include a smaller footprint, a new focus mechanism, and improvements in the speed of stage movements. In addition, the SiScan-IIA features an automatic robotic wafer-handling system.

Wafer throughput is greater than 20 wafers per hour at five sites per wafer, and linewidths can be measured down to 0.3 micron with 0.005-micron repeatability. The price of the SiScan-IIA is $350,000. The first two units will be shipped in August 1987. The SiScan-IIM, at a price of $267,000, is the manual version of the SiScan-IIA. Several units of the SiScan-IIM are already in the field.

SiScan Systems was founded in 1982. Its first product, the SiScan-I, was first introduced at SEMICON/West in 1986. There are a number of units in the installed base including systems at Cypress Semiconductor, IDT, and Motorola. SiScan Systems received its seed funding from Bay Ventures Corporation. Investors in the second round of funding included EG&G Venture Partners, Mitsubishi Corporation, Sevin Rosen Bayless Borovoy, and Shaw Venture Partners, while third round investors were Oscco Ventures and Rothschild Unterberg Towbin. SiScan has received a total of $10 million in venture funding.

Vickers Instruments

Vickers Instruments introduced its Nanolab SR Series at SEMICON/West this year. The Nanolab SR Series is an automatic, nondestructive, submicron CD and inspection system. The tool utilizes SEM (scanning electron microscope) technology, and has been designed to operate in the production environment. The wafer throughput rate is greater than 15 wafers per hour assuming 100 percent sampling at five sites per wafer. The linewidth measurement range is from 0.1 to 10.0 microns. Inspection capability is based on visual observations made by an operator. The first shipment for the Nanolab SR Series was in late 1986. The price for this system is $500,000.

Vickers also offers a sister tool to the Nanolab SR Series. This system, the Nanolab DL3206 SEM, is based on the same SEM technology as the Nanolab SR tool. The difference in the two systems is that the Nanolab DL3206 SEM has been designed for use in process development and troubleshooting, such as in the early stages of setting up a production line. In contrast, the Nanolab SR Series has been designed for in-line processing in a production environment. The price of the DL3602 system is $280,000.

At the show this year, Vickers Instruments displayed its Quaestor CD07A, a fully automatic, optical-based, CD measurement and inspection system. The tool has a wafer throughput rate of 20 to 25 wafers per hour at five sites per wafer, and can reliably measure down to 0.7 micron. The Quaestor CD07A can handle wafers sizes from three inches to 150mm, with upgrade capability to 200mm wafers. Inspection capability is based on visual observations made by an operator. The system was introduced one year ago, and several systems have been shipped. The price of the Quaestor CD07A is approximately $200,000.

Waterloo Scientific

Waterloo Scientific introduced its new automatic CD measurement system based on confocal laser scanning microscopy. The system (model WSI-1000CD) is priced at approximately $300,000 which includes robotic material handling capability. The tool shown at SEMICON/West was a prototype model. The full production system is expected to be available in the third quarter of 1987.

Waterloo Scientific is a small, privately owned, Canadian firm. The company was formed in 1983. Its main products are laser scanning microscopes. In addition to its automatic CD measurement tool, Waterloo Scientific has a second laser scanning microscope system, the WSI 100, which features optical beam induced current (OBIC) measurements for semiconductor material and device characterization.

Other Inspection Systems

Information is presented in the following section on new equipment announcements and enhancements in the areas of film thickness measurement, mask metrology, resistivity mapping, and surface defect inspection. This information is not meant to be a thorough investigation of the other categories of inspection tools at SEMICON/West this year. Rather, it has been presented to add some additional perspective on the diversity of inspection products available today.

Estek

Estek, an Eastman Kodak subsidiary, displayed the Aeronca wafer inspection equipment at SEMICON/West this year. (Eastman Kodak acquired Aeronca in early 1987.) New to the show this year is the WIS 800, a laser-based wafer inspection tool, that can conduct a variety of surface flaw analyses. The WIS 800 is 200mm compatible, and is priced at $120,000. The WIS 600 is similar in design to the WIS 800 but is 150mm compatible. Its price is $100,000. Both the WIS 600 and 800 systems are designed for measuring surface flaws and defects in films on unpatterned wafers.

The AE 1000 is a patterned wafer inspection system. An operator can accept or reject wafers based on visual inspection. Up to 300 points can be programmed in memory for specific site inspection. The price of the AE 1000 is approximately $80,000.

The Estek ISD LIS 5000 was also introduced at SEMICON/West. This system is an acoustic cleaning system integrated with an inspection station, the WIS 600 system. With this integrated system, it is possible to accept or reject wafers based on parameter analysis which uses input from the WIS tool. The ISD LIS 5000 is currently in beta site. The price for this system is approximately $250,000.

Inspex

Inspex announced the EX 3000, a patterned wafer inspection system for particle measurement. The Inspex EX 3000 provides both count and particle size distribution information in a color graphics representation. The particle size measurement sensitivity can range from 0.3 micron and more, depending upon the type of film and the number of preceding mask levels. System throughput is difficult to quantify because sampling amounts and procedures may vary, however, typically it takes 1.5 seconds to analyze a 10mm x 10mm field of view. It is possible to program the area to be sampled, in both random sampling mode and from 10 to 100 percent of the wafer surface. Software is included for statistical analysis. The EX 3000 is 200mm compatible and is priced at $300,000. The system was developed approximately 18 months ago and currently, Inspex has 20 systems installed at one customer's facilities. Inspex, a Japanese inspection company, was previously named Hamamatsu.

Lasertec

Lasertec displayed two new products this year: the 1LM11 Laser Scanning Microscope and the 2LM11 Color Laser Scanning Microscope, with CD measurement capability. The 1LM11 Laser Scanning Microscope utilizes confocal optics to provide a high-quality image capable of 0.3-micron resolution. The 1LM11 is best suited for the R&D environment or in the area of quality and process control applications as the 1LM11 has no automatic wafer-handling capability. The price of this system is approximately $78,000.

The 2LM11 Color Scanning Laser Microscope, also designed with confocal optics, utilizes beam output from both helium-neon and argon ion lasers to produce a real-time high-quality color image. The system, which includes a CD measurement system, has a resolution of 0.3 micron and an optional OBIC display. An optical beam induced current, OBIC, is produced when a light beam is focused on the surface of P-N junction. When viewing the OBIC image, it is possible to observe real-time internal current flow by varying the TTL input signal. Applications for both the 1LM11 and 2LM11 systems outside of the semiconductor industry include the study of metal surfaces, ceramics, polymers, synthetic textiles, and biological/biomedical specimens. Lasertec (formerly named NJS Corporation) also manufactures automatic mask/reticle inspection systems.

Leitz-Image Micro Systems Company

The LMS-2000 Laser Metrology System was displayed at SEMICON/West this year. The advanced high-speed mask/reticle metrology tool was developed by Letiz-IMS, a partnership between Ernst Leitz Wetzlar GmbH of West Germany and Image Micro Systems, Inc., of Billerica, Massachusetts. The LMS-2000 uses a light scanning system to provide critical dimensions and pattern dimensional

integrity data with nanometer accuracy and repeatability over an 8 x 8-square-inch area. The LMS-2000 can support the output of several e-beam mask generating systems.

Siemens AG was the first beta test site for the LMS-2000 in the summer of 1986. In addition to Siemens, Leitz-IMS has shipped one additional system to Tau Laboratories, a U.S. maskmaking company. While the LMS-2000 is approximately one year old, the first commercial product was available in first quarter 1987. The price of the LMS-2000 system is approximately $1 million.

Nanometrics

In addition to its announcements of advanced CD tools, Nanometrics introduced the Model 300 Automatic Film Thickness Measurement Station. This tool is a fully automated, microcomputer-controlled system. Wafer throughput is a nominal 20 wafers per hour. The Model 300 has 100mm, 125mm, and 150mm multicassette capability and can perform measurements in an unattended operations mode. First shipments of this system will begin in the June/July time frame to customers in the United States. The price is approximately $140,000.

Prometrix

Multilayer film thickness capability has been added to the SpectraMap SM200, a film thickness mapping system available from Prometrix. The SM200 uses a spectral response technique to measure the thickness of single or multilayer films in a range from 100 angstroms to 4 microns; films include oxide, nitride, polysilicon, photoresist, as well as others. The multilayer film thickness capability particularly lends itself to the measurement of poly-on-oxide film thickness. The SM200 measures and determines the poly thickness based on first-principle calculations, rather than relying on look-up tables of previously prepared samples. The system presents summary information in three-dimensional contour maps and control charts, and utilizes StatTrax, Prometrix's proprietary data base management system, for statistical quality control and trend chart analysis. The SM200 was first introduced at SEMICON/West 1986 and is priced at approximately $80,000. It handles 2-inch to 200mm wafers and can be configured cassette-to-cassette as an option. The SM200 has received acceptance from both sides of the industry; systems have been installed at both semiconductor and equipment manufacturers' facilities.

Prometrix introduced the OmniMap RS30 mapping system at the show this year. OmniMap is a resistivity mapping system which measures sheet resistance electrically at a number of preprogrammed locations on a fabricated wafer, stores the data, and generates a resistivity contour map. Resistivity changes as small as 0.1 percent can be detected. The OmniMap RS30 replaces the OmniMap RS20 system, which was introduced at SEMICON/West 1985. As part of the RS30 upgrade, a 20-Mbyte hard drive has replaced one of the previous 3-1/2-inch micro floppy drives. In addition, trend parameter and charting capability have been added to the system. The price of the RS30 is the same as the RS20 system at $56,000. Two of the new systems were shipped to European customers in May 1987. Upgrades to RS20 systems in the field are available.

AUTOMATION

Manufacturing automation continues to be a topic of interest within the industry, even though many semiconductor automation programs have been on hold during the recent recession. Companies exhibiting automation products at the show this year were cautiously optimistic that their semiconductor markets were starting to turn upward. However, many companies have opted to pursue automation markets outside the semiconductor industry as a strategy for surviving the "boom-bust" business cycles of semiconductor manufacturers. Market opportunities for semiconductor automation software and equipment companies include printed circuit board assembly and pharmaceutical operations. The philosophy of the automation vendors is that the knowledge and products required to meet the rigorous cleanliness and complexity requirements of the semiconductor industry will translate to any automation environment. While these firms have adopted customer base diversification as a growth strategy, they consider the semiconductor industry as the primary market for their products.

This section of the newsletter reviews some of the new products and activities in semiconductor automation. Major topics discussed are automation software systems, a cell/station controller, fixed wafer transport equipment, and robotics.

Automation Software

The two major vendors of manufacturing automation software in the semiconductor industry are Consilium and PROMIS Systems. This year at SEMICON/West, Consilium announced a new module for its COMETS software package. The Short Interval Scheduling (SIS) module provides dynamic dispatch capability and is priced at $65,000. PROMIS Systems introduced two new modules for the PROMIS software package: Advanced Production Reporting, which provides a broad scope and flexibility in report generation, and the Translator module which allows the user interface, both screen and hardcopy, to be translated and presented in non-English languages. Both modules were part of the PROMIS 4.2 software release announced in second quarter 1987. Cameo Systems, a third vendor of automation software, announced an enhancement to its CAM (computer-aided manufacturing) software package, CAMEO II. The new module, called Manufacturing Forecasting and Simulation, simulates the behavior of the factory floor in terms of material movement, process flow, and lot processing.

Qronos Technology is a new start-up in the manufacturing automation software market. This year, Qronos introduced the Qronos Production Master, a software product for manufacturing automation. The Production Master consists of three modules: WIP tracking, area planning and dispatch, and engineering data collection. The software system runs on IBM System 88 hardware. The total price for the Production Master (including software, hardware, and installation) is $1.2 million. Qronos expects to introduce three additional "Master" products later this year: order management, sales and marketing, and corporate planning. The entire system of "Master" products is known as the Qronos Advantage. Qronos software is currently in beta site at a Silicon Valley semiconductor company.

The semiconductor automation software packages are available on various computer hardware systems. For the software and hardware vendors, such alliances are important strategic decisions, since both groups are striving to increase the visibility and market share of their products within the semiconductor industry. Digital Equipment Corporation has been particularly successful in this respect since the software packages of both Consilium and PROMIS Systems, the two market leaders, run on DEC hardware. However, last year at SEMICON/West, PROMIS Systems announced the availability of IBM-compatible software, and recently, Qronos Technology became an Industrial Marketing Partner of IBM. Table 4 identifies the computer hardware for the software packages from Cameo Systems, Consilium, PROMIS Systems, and Qronos Technology.

Table 4

SEMICONDUCTOR AUTOMATION SOFTWARE PRODUCTS AND HARDWARE

	Computer Hardware Systems			
Software Vendors (Packages)	Data General	Digital Equipment	Hewlett-Packard	IBM
Cameo Systems (CAMEO II)	X	X	X	
Consilium (COMETS)		X		
PROMIS Systems (PROMIS)		X		X
Qronos Technology (Qronos Advantage)				X

Source: Dataquest
June 1987

Cell/Station Controller

CTX International introduced its CTX 1100 Station Controller. This system provides a step toward factory automation by automating data collection and recipe downloading to metrology equipment; statistical process control on collected data; and automating host data upload transactions. Current metrology interfaces include Nanometrics' Nanoline and Nanospec tools and Rudolph Auto LF Ellipsometer. The CTX 1100 has 16 ports that can be interfaced to up to 7 metrology tools, as well as to host (or multiple host) systems and off-site terminals. The price for CTX 1100 can range from $40,000 to $100,000, depending on the number of ports utilized. The system was completed in first quarter 1987. The beta site for the CTX 1100 was at Intel in Santa Clara, California. Four units of the CTX 1100 have been installed as of May 1987.

Fixed Wafer Transport

Toshiba exhibited Space Linear, its magnetically levitated carrier system for automated wafer transport; this system was first introduced at SEMICON/Japan in December 1986, as reported in our January 1987 newsletter. The system is an elevated wafer transport track which utilizes a ferromagnetic guide rail to achieve a completely contactless suspension system. The Space Linear system is priced at approximately $3,500 per foot of track; a typical system is approximately 1000 feet long. The price of the typical system would include 10 elevators, a traffic controller computer, and the guide rail system. This system is currently being used at a Toshiba semiconductor facility in Japan.

Robotics

Robotic systems were exhibited at SEMICON/West this year by processing equipment manufacturers and robotics companies that both OEM and direct supply their products to the semiconductor industry. Over the last few years, robotics companies have worked together with the front-end processing equipment vendors, particularly those firms that manufacture wet processing stations and diffusion equipment. These have been two popular fab areas where operator-intensive tasks have been replaced by robotics for reasons of both safety and manufacturing efficiency. (See the "Diffusion" section for more information on new product announcements, which include robotics and automation activities of diffusion equipment companies.) Table 5 contains a list of robotics companies at the show this year and identifies those equipment vendors displaying their products.

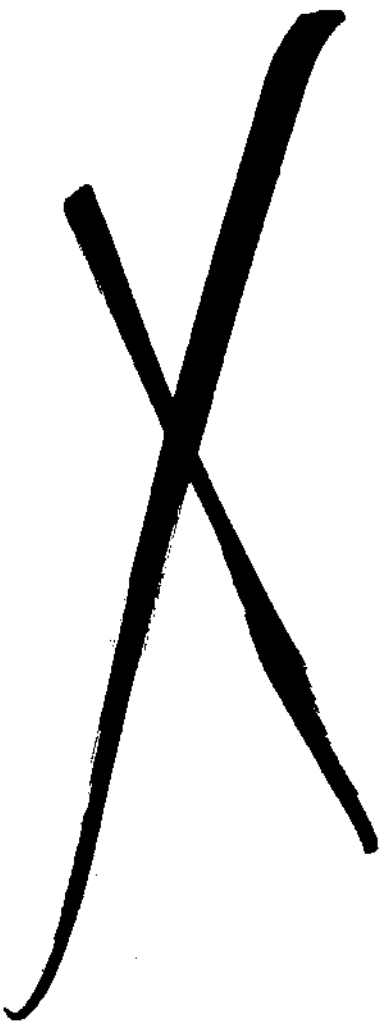
George Burns
Joseph Grenier
Robert McGeary
Mark Reagan
Peggy Marie Wood

Table 5

ROBOTICS COMPANIES AT SEMICON/WEST

Robotics Company	Equipment Company	Equipment Category
Intelledex	Thermco	Diffusion furnace
	FSI	Wet processing equipment
	Integrated Air Systems	Wet processing equipment
	Universal Plastics	Wet processing equipment
	Flexible Manufacturing Systems (FMS)	OEM supplier to FMS for automatic guided vehicle
Precision Robots, Inc.	ASM America	PECVD furnace
	Pacific Western	PECVD furnace
Unimation, A Westinghouse Company	Applied Materials	Epitaxial reactor
	ASM America	LPCVD furnace
	Quartz International	OEM supplier to Quartz International for diffusion furnace load/unload station
	Semitherm	Diffusion furnace
	Veeco	OEM supplier to Veeco for automatic guided vehicle
United States Robots	(United States Robots company product)	AB110 - Automated wet process station; (OEM for wet bench is Desert Technologies)
Wollman Engineering	Tempress	Diffusion furnace

Source: Dataquest
June 1987



July Newsletters

The following is a list of newsletters found in this section:

- Taiwan Semiconductor Manufacturing Company's Shared Resource Concept: An Idea Whose Time Has Come
  1987 - 16

Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987-1988 Newsletters: July 1987-16

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY'S SHARED RESOURCE CONCEPT: AN IDEA WHOSE TIME HAS COME

SUMMARY

Recent market and technological trends have given rise to conditions that make the strategically based fab and foundry business viable as a mainstay. The Taiwan Semiconductor Manufacturing Company (TSMC) is one such enterprise that has seen fit to enter this new arena. This newsletter explains what factors have contributed to this change in business environment, and TSMC's plan to become a leader in this emerging industry.

MARKET TRENDS

The time was when the chief attraction for U.S. and European semiconductor firms that were moving their assembly and test operations offshore to Asia was the economy of the cheaper foreign labor costs. These days, U.S. and European companies continue to shift production to the Far East for an additional reason--the newly industrialized Pacific Rim countries, Taiwan in particular, are adding technology to their already low-cost manufacturing bases. A host of other factors now hasten this global movement:

- Rapid Asian semiconductor consumption growth fed by their burgeoning electronics industry
- An increased level of business climate uncertainty due to greater volatility in foreign exchange markets and hightened protectionist sentiment among politicians
- The formation of strategic alliances to enhance long-run competitiveness by providing access to foreign countries' comparative advantages and markets

Modern fabrication equipment has enabled state-of-the-art semiconductor processes to become transportable. Worldwide computer networks allow remote linking of multiple design centers to strategically located manufacturing sites. Thus now more than ever, maximizing a silicon fab's proximity to an OEM site improves just-in-time material support, thereby reducing customer inventory costs and simplifying logistics.

On the Taiwanese domestic front, government industrial policy encourages the rapid proliferation of high-tech start-ups through, for example, the Science-Based Industrial Park Administration. Also, a rapidly rising standard of living has stimulated the indigenous demand for consumer electronics goods. Finally, about 20 Taiwanese semiconductor design houses are in place and in need of silicon fab and foundry support. Insufficient manufacturing support is the binding constraint that hinders long-run semiconductor production growth. This hindrance must be removed if the Taiwanese semiconductor industry is to compete with the Koreans and the Japanese.

With respect to technological trends, Dataquest estimates that CMOS will represent 40 percent of total worldwide wafer starts by 1989, an increase from only 16 percent in 1986. CMOS is clearly the technological choice of the future. Given that much of the existing fab capacity is dedicated to bipolar production, conversion of this equipment to CMOS production is not economically feasible. Wafer fab equipment costs continue to rise, exacerbating the semiconductor manufacturers' need to invest in changing production technology. Finally, custom and semicustom application-specific ICs (ASICs), the bread and butter of the next wave of semiconductor start-ups, are expected to be the dominant chip type by the turn of the decade. These small and medium-size IC companies will require outside silicon fab support.

These days, the typical foundry relationships are characterized by:

- Idle capacity or mature technology for sale
- Leading-edge technology/capacity sold for reciprocal product design rights
- Capital investment (i.e., capacity) traded for technology and/or product design rights

In most cases, foundry relationships are opportunistic--not strategic. They arise from the simultaneous, unanticipated variability in product demand, supply and capacity utilization, and generally speaking, the deviation of the actual outcomes of past consumer/producer decisions from their expected outcomes.

TSMC'S SHARED RESOURCE CONCEPT

The essence of TSMC's shared resource concept is to seize the profitable opportunities these market and technological trends create by establishing strategically founded, mutually beneficial relationships with the demanders of silicon fab and foundry support. TSMC's business concept is to provide a one-stop semiconductor manufacturing service including:

- Mask and wafer fabrication
- Probing test
- Packaging
- Final test
- Burn-in

The company's role in the emerging fab and foundry industry can best be seen in Figure 1. TSMC expects to attract the bulk of its business from system-house end users and design and marketing houses. Many integrated semiconductor companies' designs are expected to continue to be fabricated in-house, though some of this work will be contracted to TSMC and other foundries in times of peak capacity utilization.

TSMC's business scope is thus seen to include:

- System companies
- IC design companies
- Start-up companies
- Integrated IC companies

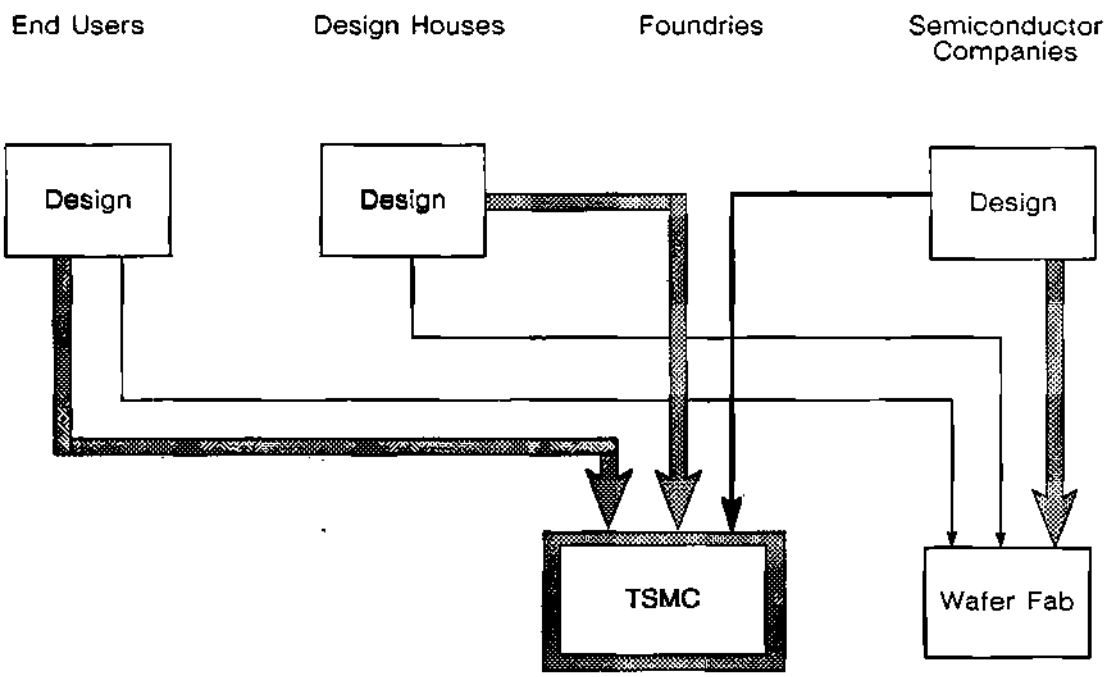
TSMC's customers should benefit from such strategically based relationships by seeing their investment costs reduced. In the short run, inventory levels--both work in progress and finished goods--should be lower since TSMC's emphasis is on just-in-time delivery.

In the long run, since TSMC is committed to bearing the cost of semiconductor manufacturing equipment investment, its customers should expect dramatic reductions in capital spending for new technology and/or capacity. Allied with this, since TSMC will be shouldering the burden of staying technologically current (and competitive) and having capacity available, many of its customers should expect to see reduced R&D budgets for process development.

Thus, in the same way that demanders of commercial or industrial floor space minimize the cost and risk of building use through lease arrangements instead of outright ownerships, the costs and risks of plant and equipment investment are shifted to TSMC from its customers.

Figure 1

TSMC'S ROLE



Source: TSMC

Finally, the shift to silicon-system IC designs with fast-cycle foundry is expected to enhance ASIC distribution by reducing the time to market for new products.

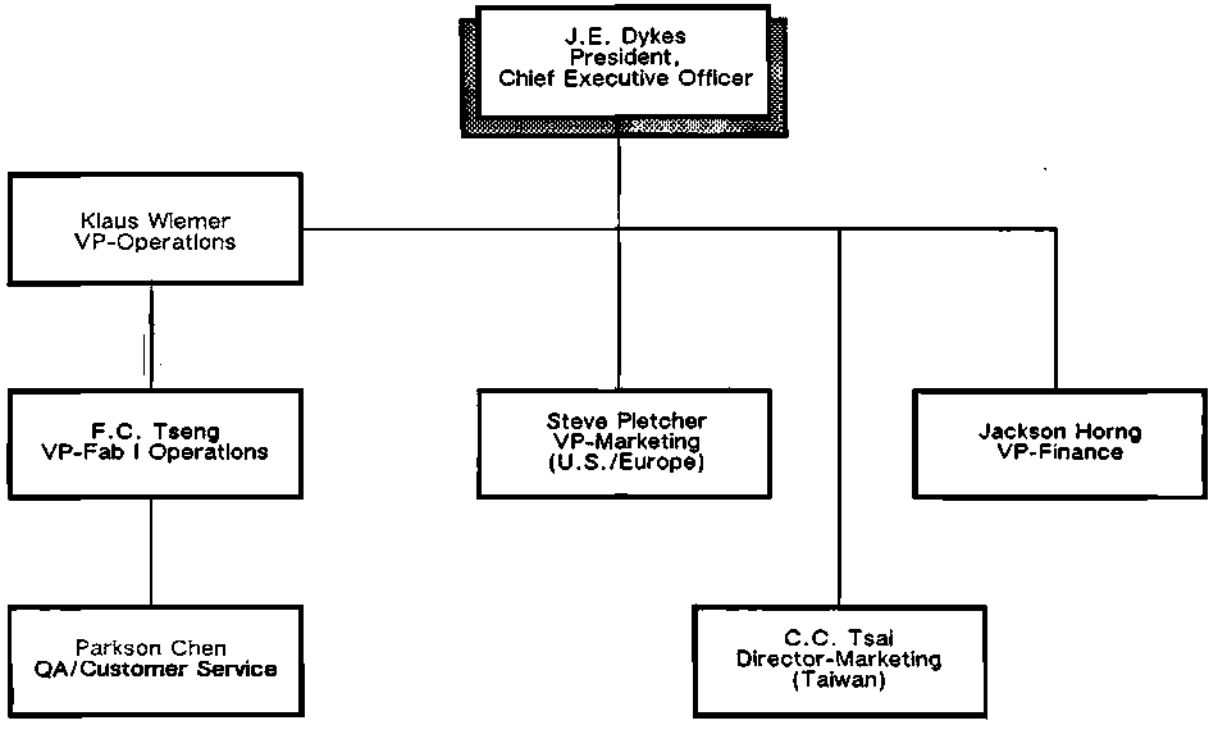
The shared resource concept thus presents TSMC not as a competitor but as a partner in strategic long-term technology and manufacturing relationships with IC designers, producers, and users. TSMC's charter prohibits the company from entering into product designs or the commercial sale of finished products to end users.

ORGANIZATION AND HISTORY

The joint-venture shareholders' agreement leading to the formation of TSMC was consummated in late 1986. By February 1987, TSMC was commercially licensed as a Taiwanese private enterprise. Reporting to a 10-person board of directors, TSMC's chairman is Dr. Morris Chang (formerly of TI and GE), and its president and CEO is James Dykes (formerly of Harris Corporation and GE). The organizational structure is shown in Figure 2.

Figure 2

THE TSMC ORGANIZATION



Source: TSMC

The venture began operation immediately through an innovative arrangement with ITRI's ERSO branch. The existing 6-inch wafer fab and an in-place contingent of approximately 100 employees were transferred in situ from ERSO to TSMC. Headcount as of June 1 was approximately 220 and year-end headcount is expected to be 320.

Generating investor interest has not been a problem. TSMC successfully raised $153 million in initial authorized capital. As Table 1 shows, more than 75.0 percent of the outside investment capital has been provided by two parties: 48.3 percent from the Executive Yuan's Development Fund and 27.5 percent from N.V. Philips' Gloeilampenfabrieken. The number of outside investors serves to indicate the broad acceptance of TSMC's business plans.

Table 1

TSMC's OUTSIDE INVESTORS

Organization	Percentage of Total Outside Capital
Development Fund, Executive Yuan	48.3%
N. V. Philips' Gloeilampenfabrieken	27.5
Formosa Plastics Corporation Nan Ya Plastics Corporation Formosa Chemicals and Fiber Corporation	5.0
China American Petrochemical Company, Ltd.	5.0
China General Plastics Corporation Asia Polymer Corporation Mabuchi Taiwan Company, Ltd.	3.0
USI Far East Corporation	2.0
Yao Hua Glass Company, Ltd.	2.0
Union Petrochemical Corporation	1.0
Tai Yuen Textile Company, Ltd.	1.0
ADI Corporation	1.0
Central Investment Holding Company, Ltd.	4.2
Total	100.0%

Source: Dataquest
July 1987

Cooperation agreements are also an indication of the markets' perception of TSMC's expected viability. Since its formation, TSMC has succeeded in consummating four significant agreements:

- Philips/TSMC Technical Cooperation
  - Mainstream processes (current and future plans)
  - Patent license
- ITRI/TSMC Technical Cooperation
  - Mainstream processes (current and future plans)
  - Patent license
  - CAD support
  - Mask-making support
  - Development contract
  - Foundry services to Taiwan-based customers
- ITRI/TSMC
  - Fab-1 Lease
- PEBEI/TSMC
  - Assembly contract

Since the Technology Cooperation Agreement (TCA) with Philips is a 10-year renewable contract, the signs are that continuing access to technology should not be a problem.

At the present time, TSMC leases its Fab-1 facility from ITRI. The total area of the plant, which is detailed in Table 2, is 6,823 square meters. Current output is about 800 wafers per month, with output expected to be about 2,400 wafers per month by the end of June. Capacity is scheduled for expansion to about 10,000 wafers per month by year end. A second wafer fabrication plant is expected to be opened in the Hsin Chu Science-Based Industrial Park when the need arises (probably mid 1989).

Table 2

FAB-1 AREA

			ft^2	m^2	Ping
Plant					
Clean Room	Class 1/10	0.2um	6,436	598	179
	Class 100	0.3um	1,201	112	33
	Class 10,000	0.3um	5,955	553	165
Other	Class 10,000	0.5um	13,318	1,237	370
Subtotal			26,910	2,500	747
Utility			11,903	1,106	331
Chemical Storage			2,637	245	73
Office					
First Floor			11,115	1,033	309
Second Floor			14,350	1,333	399
Basement			6,522	606	181
Subtotal			31,987	2,972	889
Total Area			73,437	6,823	2,040

Source: Dataquest
July 1987

The process technology mix currently being used at TSMC spans a broad range of geometries and is not unlike that of many other foundries presently in operation:

- 3um silicon-gate NMOS/CMOS (P-well) process
- 2um silicon-gate CMOS (N-well) process with single-layer metallization/dual-layer metallization options, ASIC
- 1.5um silicon-gate CMOS (N-well) process with single polysilicon/ double polysilicon options, SRAM, DRAM
- 1.25um silicon-gate CMOS (N-well) process with single-layer metallization/double-layer metallization options

KEYS TO TSMC'S SUCCESS

This newsletter has shown the trends that have created a significant, profitable opportunity for entrepreneurs to pursue fab and foundry ventures based on strategically oriented relationships with their customers. One entry into this arena is the Taiwan Semiconductor Manufacturing Company. Time will tell, however, whether TSMC's shared resource concept will prove viable and to what extent. TSMC's success factors for future performance will include:

- Continuing access to capital resources
- Continuing access to technology
- Long-term customer relationships

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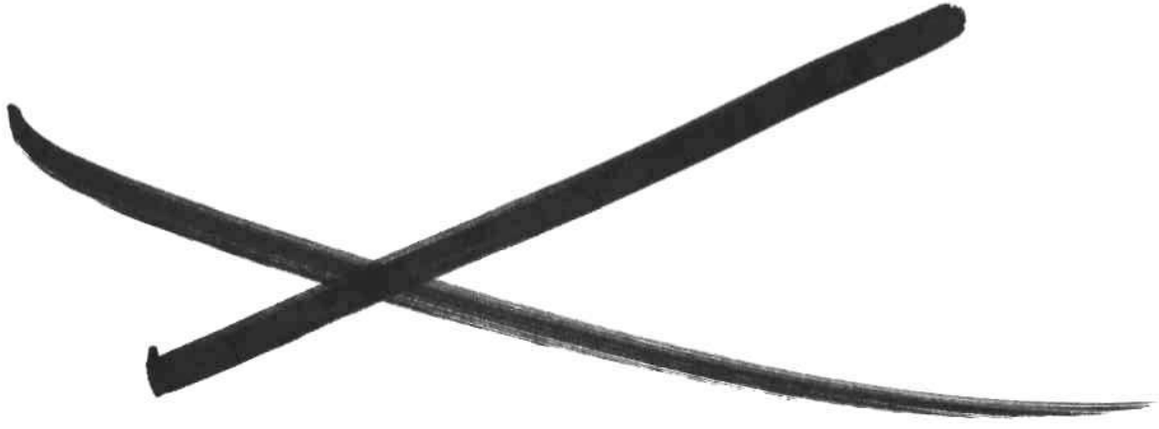
Mark Reagan
Terrance A. Birkholz



August Newsletters

The following is a list of newsletters found in this section:

- Worldwide Semiconductor Shipments Forecast
  1987 - #20
- Sustained Recovery: North American Forecast
  1987 - #19
- Second Quarter Start-Up Update
  1987 - #18
- Synchrotron Orbital Radiation: Japan's Push Into Ultradense Megabit Memories
  1987 - #17

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Research Newsletter

SEMS Code: 1987-1988 Newsletters: August 1987-20

WORLDWIDE SEMICONDUCTOR SHIPMENTS FORECAST

Dataquest projects that worldwide semiconductor shipments will rise 17.9 percent in 1987 and 20.3 percent in 1988, measured in U.S. dollars. Though this forecast is virtually the same as our April quarterly forecast, the regional breakup has changed (see Table 1).

During the first half of 1987, semiconductor shipments to North America showed the strongest growth worldwide. In comparison, shipments to Japan declined, and Europe experienced slower than anticipated growth. We are raising our estimate of 1987 semiconductor shipments to North America to growth of 18 percent rather than 15 percent as previously forecast. Signs of a turnaround are evident in the U.S. computer industry, leading Dataquest to expect sustained but slower growth in the U.S. semiconductor market during the second half of 1987.

Because of impact of yen appreciation on electronic equipment production in Japan, we are lowering our estimate of 1987 semiconductor shipments to Japan. We now project that the Japanese market will decline 4.8 percent in 1987, measured in yen, rather than grow 5.3 percent, as previously forecast. Measured in U.S. dollars, this projection translates to 10.3 percent growth.

Table 1

ESTIMATED WORLDWIDE SEMICONDUCTOR SHIPMENTS
(Billions of U.S. Dollars)

	1986	1987	1988
North America	$10.2	$12.0	$14.4
Japan	12.4	13.6	16.0
Europe	5.5	6.7	8.1
Rest of World	2.9	4.2	5.5
Worldwide	$31.0	$36.5	$44.0

Source: Dataquest
August 1987

The estimated worldwide quarterly semiconductor shipments by product category are shown in Table 2.

Joseph Grenier
Joseph Borgia

Table 2

ESTIMATED WORLDWIDE SEMICONDUCTOR SHIPMENTS
(Millions of U.S. Dollars)

	1986	Q1/87	Q2/87	Q3/87	Q4/87	1987	% Chg. 1987
Total Semiconductor	$31,009	8,361	9,032	9,380	9,787	$36,559	17.9%
Total IC	$23,601	6,424	6,972	7,311	7,649	$28,355	20.1%
Bipolar Digital	$ 4,321	1,116	1,228	1,285	1,335	$ 4,963	14.9%
Memory	675	179	190	196	198	762	12.9%
Logic	3,646	937	1,038	1,089	1,137	4,201	15.2%
MOS Digital	$13,064	3,695	4,086	4,331	4,564	$16,675	27.6%
Memory	4,338	1,176	1,317	1,421	1,503	5,417	24.9%
Micro	3,661	1,061	1,171	1,231	1,297	4,760	30.0%
Logic	5,065	1,458	1,598	1,679	1,764	6,498	28.3%
Linear	$ 6,216	1,614	1,658	1,695	1,750	$ 6,717	8.1%
Discrete	$ 5,818	1,529	1,627	1,636	1,680	$ 6,472	11.2%
Optoelectronic	$ 1,590	408	433	433	458	$ 1,732	8.9%
Exchange Rate Yen/$	167	153	142	142	142	145	(13.2%)
Exchange Rate ECU/$	146	129	125	125	125	126	(13.7%)

	1987	Q1/88	Q2/88	Q3/88	Q4/88	1988	% Chg. 1988
Total Semiconductor	$36,559	10,197	10,790	11,292	11,688	$43,968	20.3%
Total IC	$28,355	7,991	8,497	8,924	9,249	$34,662	22.2%
Bipolar Digital	$ 4,963	1,377	1,454	1,532	1,594	$ 5,957	20.0%
Memory	762	202	211	220	228	861	13.0%
Logic	4,201	1,175	1,243	1,312	1,366	5,096	21.3%
MOS Digital	$16,675	4,825	5,180	5,478	5,708	$21,191	27.1%
Memory	5,417	1,596	1,718	1,811	1,871	6,996	29.1%
Micro	4,760	1,365	1,467	1,556	1,618	6,006	26.2%
Logic	6,498	1,864	1,995	2,111	2,219	8,189	26.0%
Linear	$ 6,717	1,789	1,864	1,914	1,947	$ 7,514	11.9%
Discrete	$ 6,472	1,730	1,799	1,853	1,909	$ 7,291	12.7%
Optoelectronic	$ 1,732	476	494	515	530	$ 2,015	16.3%
Exchange Rate Yen/$	145	142	142	142	142	142	(2.1%)
Exchange Rate ECU/$	126	125	125	125	125	125	(1.0%)

Note: This table was previously entitled "Estimated Worldwide Semiconductor Consumption."

Source: Dataquest
August 1987

Table 2

ESTIMATED WORLDWIDE SEMICONDUCTOR SHIPMENTS
(Millions of U.S. Dollars)

	1986	Q1/87	Q2/87	Q3/87	Q4/87	1987	% Chg. 1987
Total Semiconductor	$31,009	8,361	9,032	9,380	9,787	$36,559	17.9%
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Memory	5,417	1,596	1,718	1,811	1,871	6,996	29.1%
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Linear	$ 6,717	1,789	1,864	1,914	1,947	$ 7,514	11.9%
Discrete	$ 6,472	1,730	1,799	1,853	1,909	$ 7,291	12.7%
Optoelectronic	$ 1,732	476	494	515	530	$ 2,015	16.3%
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Exchange Rate ECU/$	126	125	125	125	125	125	(1.0%)

Note: This table was previously entitled "Estimated Worldwide Semiconductor Consumption."

Source: Dataquest
August 1987

Dataquest
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Research Newsletter

SEMS Code: 1987 Newsletters: August 1987-19

SUSTAINED RECOVERY: NORTH AMERICAN FORECAST

SUMMARY

The semiconductor recovery got a head start during the first half of 1987. Shipments grew faster than anticipated in both the first and second quarters. Bookings continue to be very strong and broad-based. Book-to-bill ratios stayed above parity for the entire first half of 1987, resulting in a healthy order backlog for the industry. Sustained recovery through the rest of 1987 is apparent, albeit with some slowing in the summer months. Dataquest is raising the 1987 forecast from 15 percent growth to 18 percent growth for semiconductor shipments to North America.

The electronic equipment production in the United States is regaining strength in several key areas. Signs of recovery are evident in the computer industry, which is emerging from the cyclical low shipment and booking levels experienced during late 1986. Annual rate of change in bookings has now turned positive, and we expect the same for shipments by late summer. The communications industry shipments have bottomed, and are expected to rise in the coming months. Another healthy sign is that equipment inventory levels remain low.

The semiconductor industry is approaching this recovery with much caution. Shortages are being experienced in some product areas, and prices are firming for commodity products. The industry is carefully gearing up to meet the anticipated rise in demand. This recovery lacks the fervor of earlier upsurges, but the industry participants are well prepared for the long-awaited up cycle.

MONITORING OUR QUARTERLY INDUSTRY FORECAST

Table 1 compares our current forecast to our prior forecasts.

ASSUMPTIONS FOR THIS FORECAST

Book-to-Bill Stays above Parity

The semiconductor book-to-bill ratio has been rising since October and should stay above or close to parity for the rest of 1987. The healthy rise in backlog is supporting shipments for the year.

Computer Industry Registers Positive Growth

Computer industry bookings rose to a positive annual rate during the second quarter of 1987. The annual rate of growth in shipments is expected to become positive this summer.

Communications Industry Remains Healthy

Communications industry bookings and shipments bottomed in the second quarter of 1987 and are expected to rise during the coming months.

Other Economic Assumptions--1987

Real GNP is expected to grow in excess of 3 percent in 1987, with about a 4 percent rise in the consumer price index. Federal fund rates should stabilize in the 6 to 7 percent range.

Capacity utilization should rise to 70 percent by year end, with some product areas becoming capacity-constrained.

THE FORECAST: SUSTAINED RECOVERY

Our quarterly forecast of semiconductor shipments to North America for 1987 and 1988 is shown in Table 2.

DATAQUEST ANALYSIS

Dataquest projects 18 percent growth in 1987 semiconductor shipments to North America. With 1987's strong first half, we are more than halfway there. The rising backlog and the above parity book-to-bill ratios assure sustained growth during the rest of the year. Signs of a recovery are evident in the U.S. computer industry, and the communications industry is at a turning point. Healthy growth in these electronic equipment industries should sustain the recovery in semiconductor shipments through 1988.

Joseph Grenier
Joseph K. Borgia

Table 1

QUARTERLY INDUSTRY FORECAST: STAGGER CHART
SEMICONDUCTOR SHIPMENTS TO NORTH AMERICA
(Billions of Dollars)

Forecast Date	Q1/87	Q2/87	Q3/87	Q4/87	1987
Oct. 1986	$2.6	$2.8	$2.9	$3.1	$11.4
Jan. 1987	$2.7	$2.8	$2.9	$3.1	$11.5
Apr. 1987	$2.7	$2.9	$3.0	$3.1	$11.7
July 1987	-	$3.0	$3.1	$3.2	$12.0

Forecast Date	Q1/88	Q2/88	Q3/88	Q4/88	1988
Oct. 1986	-	-	-	-	$14.9
Jan. 1987	$3.3	$3.5	$3.7	$3.7	$14.2
Apr. 1987	$3.3	$3.6	$3.7	$3.7	$14.3
July 1987	$3.4	$3.6	$3.7	$3.8	$14.4

Source: Dataquest
August 1987

Table 2

ESTIMATED SEMICONDUCTOR SHIPMENTS TO NORTH AMERICA
(Millions of Dollars)

	1986	Q1/87	Q2/87	Q3/87	Q4/87	1987	% Chg. 1987
Total Semiconductor	$10,201	2,731	2,974	3,092	3,235	$12,032	18.0%
Total IC	$8,136	2,205	2,413	2,522	2,651	$9,791	20.3%
Bipolar Digital	$2,021	511	561	593	626	$2,291	13.4%
Memory	335	88	91	94	97	370	10.4%
Logic	1,686	423	470	499	529	1,921	13.9%
MOS Digital	$4,484	1,296	1,424	1,487	1,565	$5,772	28.7%
Memory	1,560	435	479	507	538	1,959	25.6%
Micro	1,262	368	408	418	438	1,632	29.3%
Logic	1,662	493	537	562	589	2,181	31.2%
Linear	$1,631	398	428	442	460	$1,728	5.9%
Discrete	$1,649	426	456	461	469	$1,812	9.9%
Optoelectronic	$416	100	105	109	115	$429	3.1%

	1987	Q1/88	Q2/88	Q3/88	Q4/88	1988	% Chg. 1988
Total Semiconductor	$12,032	3,375	3,588	3,689	3,788	$14,440	20.0%
Total IC	$9,791	2,778	2,967	3,060	3,154	$11,959	22.1%
Bipolar Digital	$2,291	639	664	683	698	$2,684	17.2%
Memory	370	99	103	105	108	415	12.2%
Logic	1,921	540	561	578	590	2,269	18.1%
MOS Digital	$5,772	1,666	1,806	1,872	1,941	$7,285	26.2%
Memory	1,959	575	620	640	655	2,490	27.1%
Micro	1,632	469	520	540	559	2,088	27.9%
Logic	2,181	622	666	692	727	2,707	24.1%
Linear	$1,728	473	497	505	515	$1,990	15.2%
Discrete	$1,812	481	501	507	511	$2,000	10.4%
Optoelectronic	$429	116	120	122	123	$481	12.1%

Note: This table was previously titled "Estimated North American Semiconductor Consumption"

Source: Dataquest
August 1987

Dataquest
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Research Newsletter

SEMS Code: 1987-1988 Newsletters: August 1987-18

SECOND QUARTER START-UP UPDATE

The second-quarter update on start-up companies includes information on new company formations, acquisitions, and company announcements made in the second quarter. It also includes information on financing raised and agreements made in the first half of 1987.

HIGHLIGHTS

Second-quarter highlights include the following:

- Four companies were formed in 1987.
- European Silicon Structures and Microwave Technology have made acquisitions.
- VTC became a wholly owned subsidiary of Control Data Corporation.
- Approximately $238.3 million was raised in new and additional funding in the first half.
- Twenty-six agreements were signed by start-up companies in the first half.
- Significant management announcements were made.
- International Microelectronic Products went public.
- VLSI Technology broke ground on a 25,000-square-foot wafer fab in Texas.

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 971-9000, Telex 171973

NEW COMPANIES

GL Micro Devices

GL Micro Devices was formed in February 1987 to develop high-performance, advanced CMOS products. The company was founded by Norman Godinho and Frank Lee, both formerly with Integrated Device Technology. Glenwood Management and El Dorado Ventures participated in $2.4 million seed financing, which was completed in April of this year.

Mr. Godinho served as vice president and general manager of IDT's digital signal processing division, and Mr. Lee was codirector of IDT's corporate research and development group.

LOGICSTAR Inc.

LOGICSTAR was formed in 1987 to design, manufacture, and sell high-performance PC AT logic, VLSI graphics, and local area network chips. The company is addressing the PC AT market and is using a VLSI design methodology to bring products to market quickly.

LOGICSTAR was formed by Mark Kaleem, who was formerly president of OSM Computer and Unilogic. Vice president of marketing is Saeed Kazmi, who was formerly with VLSI Technology Inc. in technical sales support.

LOGICSTAR's initial products are a five-chip PC AT chip set that is pin-for-pin compatible with Chips & Technologies' chip set, a monographics controller, a dual-channel NRZI encoder/decoder, and a STARLAN interface chip. Future products will include a VGA chip, PS/2 chip, 386 chip sets, additional data communication chips, and disk controllers.

Foundry services are being provided by companies in the United States and Japan.

Ramax Limited

Ramax Limited is an Australian-based company that is being formed through a $45 million joint venture between Australia's state of Victoria and other investors. A development company owned by the state of Victoria is providing $850,000, for which the state will receive between 7 and 13 percent equity in the company, with the balance in first-round equity coming from both U.S. and Australian investors. The financing should be complete by September 30.

Peter J. Solomon is executive director of Ramax, and Dr. Bruce Godfrey is manager of product and technology development. Dr. Godfrey has been an adjunct assistant professor at the University of Colorado and one of the researchers involved in developing technology the company will be using.

Ramax has licensed high-speed, nonvolatile memory technology using a ferroelectric semiconductor process and a companion technology that uses a thin-film process from Ramtron, an Australian R&D company located in Colorado Springs, Colorado. Ramax acquired a 12 percent stake in Ramtron for $8.0 million and paid $6.9 million in licensing fees.

Initially, the company will produce prototype silicon-based circuits using Ramtron's technology. Future plans include the manufacture of GaAs circuits using the ferroelectric thin-film technology under terms of a license that gives Ramax exclusive worldwide rights to use the Ramtron technology on GaAs.

SIMTEK Corporation

On May 15, 1987, Dr. Richard L. Petritz and Dr. Gary F. Derbenwick announced the formation of SIMTEK Corporation, which will develop, manufacture, and market a broad range of advanced semiconductor products. The company will initially focus on new memory components for consumer, commercial, and government markets.

Dr. Petritz, a founder of Mostek and Inmos, will serve as chairman and chief executive officer of the company. Dr. Derbenwick, who was formerly product technology manager at Inmos, will serve as president and chief operating officer.

The initial capitalization for SIMTEK is from Nippon Steel Corporation of Japan, which will own about 20 percent of the company and have a seat on the board. Nippon Steel produced 28 million tons of steel products in 1986, with sales of $15 billion. The investment by Nippon Steel is part of a diversification plan to expand into other business areas.

SIMTEK's headquarters are located in Colorado Springs, Colorado. During the next three months, the company will be conducting studies for its permanent U.S. facilities, which will include a substantial manufacturing capability. The company plans to begin manufacturing within the next 18 months.

MERGERS AND ACQUISITIONS

European Silicon Structures

European Silicon Structures (ES2) is negotiating to acquire Lattice Logic Ltd., an Edinburgh-based silicon compiler software house. ES2 has been marketing Lattice Logic's compilers in Europe since 1985. The merger should give Lattice Logic financial security and the finances to develop software with ES2.

Microwave Technology, Inc.

Microwave Technology, Inc. (MwT), completed the acquisition of Monolithic Microsystems, Inc., of Santa Cruz, California, in June 1987. Monolithic Microsystems makes detector log video amplifiers (DLVAs), logarithmic video amplifiers (LVAs), and threshold detectors, based on its proprietary monolithic silicon LVA ICs. Monolithic Microsystems is manufacturing devices used in various electronic warfare systems and other defense electronic applications.

MwT designs, manufactures, and sells GaAs epitaxial materials, GaAs field-effect transistor devices and monolithic circuits, hybrid microwave ICs, and microwave subassemblies.

Monolithic Microsystems will operate as a wholly owned subsidiary of MwT and will continue its manufacturing operations in its 8,200-square-foot Santa Cruz facility.

VTC, Inc.

VTC has signed a merger agreement under which it will become a wholly owned subsidiary of Control Data Corporation, its largest investor and major customer. The companies declined to disclose the terms of the proposed purchase. Control Data has invested $56 million in VTC since it was founded and holds nonvoting preferred shares in the company that are convertible to 49 percent of the company's voting stock.

The arrangement provides VTC with revenue and financial support. VTC's founders, Thomas E. Hendrickson and John R. Hodgson, will continue to manage the company.

Table 1 lists financing raised by start-up companies in the first half of 1987.

Table 1

FINANCING RAISED BY START-UP COMPANIES
FIRST HALF 1987

Company	Month	Round	Amount ($M)	Investors
Dallas Semiconductor	April 1987	3	$ 5.0	Abingworth; Alex Brown & Sons Emerging Growth Stocks; British Petroleum BP Ventures; HLM Partners; Merifin N.V.; New Enterprise Associates; Southwest Enterprise Associates; T. Rowe Price; Threshold Fund; Ventech Partners
Gigabit Logic	May 1987	3	$ 15.0	Analog Devices; Cray Research; Digital Equipment; First Interstate Capital; General Electric Venture; Interfirst Venture; New Enterprises Associates II; Riodan Venture; Union Venture
GL Micro Devices	April 1987	Seed	$ 2.4	Glenwood Management; El Dorado Ventures
International CMOS Technology	June 1987	3	$ 2.0	Undisclosed institutional investors
LSI Logic	April 1987	Eurobond Offer	$125.0	Convertible subordinated debentures offered on London's Unlisted Securities Market
Ramax Limited	June 1987	1	$ 0.8	State of Victoria, Australia

(Continued)

Table 1 (Continued)

FINANCING RAISED BY START-UP COMPANIES
FIRST HALF 1987

Company	Month	Round	Amount ($M)	Investors
Saratoga Semiconductor	March 1987	3	$ 11.5	Initial investors: Berry Cash Southwest Partners; Dougery, Jones & Wilder; Interwest Partners; Matrix Partners; MBW Venture Partners; Merrill, Pickard, Anderson & Eyre; Sierra Ventures; Sigma Partners; Weiss Peck & Greer Venture Partners
			$ 7.6	New investors: Bank of America Capital; HLM Management; John Hancock Venture Capital; New York Life Insurance; Security Pacific Capital; T. Rowe Price Associates
Vitesse Semiconductor	Feb. 1987	2	$ 10.0	Bryan & Edwards; J.H. Whitney; New Enterprises Associates; Oxford Venture Corporation; Robertson, Colman & Stephens; Sequoia Capital; Suez Technology Fund; Walden Capital
VLSI Technology	April 1987	Bond Offer	$ 48.75	Offered convertible subordinated debentures

(Continued)

Table 1 (Continued)

FINANCING RAISED BY START-UP COMPANIES
FIRST HALF 1987

Company	Month	Round	Amount ($M)	Investors
Xilinx	Jan. 1987	3	$ 3.4	Fleming Ventures Ltd.; Hambrecht & Quist; Kleiner, Perkins, Caufield & Byers; Interfirst Venture; Interwest Perkins; Matrix Partners; Morgan Stanley; Rainier Venture Partners; Security Pacific Venture Capital; J.H. Whitney
Zoran	April 1987	4	$ 6.8	Adler & Company; Concorde Partners; Elron Electronics; Grace Ventures Corp.; Kleiner, Perkins, Caufield & Byers; Mitsui & Company; Montgomery Securities; Vista Ventures; Welsh, Anderson & Stowe

Source: Dataquest
August 1987

Table 2 lists agreements start-up companies formed in the first half of 1987.

Table 2

AGREEMENTS WITH START-UP COMPANIES
FIRST HALF 1987

Company	Date	Comments
Altera WaferScale Sharp	Jan. 1987	Altera and WSI agree to a five-year technology exchange focused on developing new user-configurable logic products. Sharp will manufacture the products using WSI's process.
Altera Cypress	June 1987	Cypress Semiconductor Corporation and Altera Corporation announced a five-year technology development agreement focused on new high-performance, high-density, user-configurable logic products. Altera will provide the architecture, circuit design, and software support. Cypress will provide its CMOS process and EPROM device development and manufacturing capacity from its new Austin, Texas fab. The first devices, designated MAX (for Multiple Array Matrix), promise to extend the EPLD density capability up to 5,000 equivalent gates.
Catalyst Oki Electric	March 1987	Catalyst and Oki Electric agreed to a second-source agreement covering a wide range of CMOS EEPROMs. This is another phase of their continuing CMOS memory technology partnership, which was signed in July 1986. The two companies will jointly introduce a 1K serial EEPROM, which will be followed with 256-bit and 512-bit serial EEPROMs, 16K and 64K CMOS EEPROMs, and a 256K CMOS EEPROM that will be introduced at the end of the year.
CDI IST	April 1987	California Devices Inc. (CDI) and Innovative Silicon Technology (IST) have reached an agreement that provides for joint product development and second-sourcing of two families of ASICs using channelless ASIC architectures. The first family will be based on a 2-micron, double-metal layer CMOS and will have a complexity of up to 24,000 gates. The second family, which is slated for introduction in 1988, will be based on 1.5-micron technology and will have more than 100,000 gates.

(Continued)

Table 2 (Continued)

AGREEMENTS WITH START-UP COMPANIES
FIRST HALF 1987

Company	Date	Comments
Crystal Asahi Chemical	Jan. 1987	Asahi Chemical has acquired an 8 percent share in Crystal Semiconductor for about $4 million. Asahi will provide foundry services in exchange for a license to all of Crystal's existing products and for principle distribution rights in the Far East. Both companies will develop new products.
Custom Silicon NCR	Feb. 1987	NCR has licensed CSi's standard cell library, that includes 342 TTL macrocells and microcomputer building blocks of up to 5,863-gates. CSi's library was built from NCR's existing library, which CSi licensed.
Dallas Xecom	May 1987	Dallas Semiconductor Corporation and Xecom Inc. signed a second-source agreement giving both companies marketing rights for several of their existing products. In addition, the companies will cooperate on developing, manufacturing, and marketing future modem-related products--the area of Xecom's expertise. As part of the agreement, Dallas will alternate-source two of Xecom's modem components--the XE1251 and XE1253 modem development kits and the standalone XE0002 Data Access Arrangement unit, which is registered by the FCC. Xecom will second-source Dallas' SmartSocket and the SmartWatch families of products.
ES2 N.V. Philips TI	Feb. 1987	Texas Instruments Ltd. of England and Philips International N.V. will offer accelerated prototyping for the SystemCell Library of standard cells in cooperation with ES2. The SystemCell Library is the result of a collaborative relationship between TI and Philips, which provides high-volume manufacturing and standard prototyping.

(Continued)

Table 2 (Continued)

AGREEMENTS WITH START-UP COMPANIES
FIRST HALF 1987

Company	Date	Comments
GigaBit Logic Seattle Silicon WTC	April 1987	GigaBit Logic, Seattle Silicon Corp., and the Washington Technology Center (WTC) announced that a joint design project has resulted in the fabrication of a functional compiler-based GaAs IC design. The design is based on GigaBit's standard cell library and uses Seattle Silicon's Concorde Blue Chip Compiler. WTC provided design and engineering support and will be involved in the packaging and testing of the ICs. The device is equivalent to the 100K ECL 4-bit ALU (100181).
ICT Asahi Chemical	Jan. 1987	Asahi Chemical Industry will receive technology from International CMOS Technology (ICT) and will also market its EEPROMs.
IDT VTC	Jan. 1987	VTC will second-source Integrated Device Technology's FCT product line of TTL-compatible CMOS logic devices.
IST SDA Systems	May 1987	Innovative Silicon Technology Corp. (IST), a wholly owned subsidiary of SGS Corp., signed an agreement with SDA Systems Inc. to develop CAD systems based on SDA technology for use by IST customers.
Lattice SGS	Feb. 1987	Lattice Semiconductor signed a technology agreement with SGS Semiconductor, giving SGS a license to second-source Lattice's Generic Array Logic (GAL) products. SGS will manufacture GAL products for Lattice, and both companies will cooperate on the design of future PLD products.
Lattice National	May 1987	National Semiconductor Corporation made a minority capital investment in Lattice Semiconductor Corporation and licensed its Generic Array Logic (GAL) technology. The five-year agreement includes codevelopment of denser architectures of both standard and in-system programmable GALs, as well as a new line of FPLAs and sequencer devices.

(Continued)

Table 2 (Continued)

AGREEMENTS WITH START-UP COMPANIES
FIRST HALF 1987

Company	Date	Comments
LTC TI	March 1987	Linear Technology Corporation (LTC) and Texas Instruments Inc. (TI) agreed to a five-year alliance for advanced linear ICs. TI will select six products each six months from LTC's line to manufacture and market as TI parts. TI will pay LTC $500,000 and undisclosed royalties on a descending scale for a 10-year period and will directly purchase a number of products for resale. In addition, TI will invest approximately $1 million for warrants to purchase 735,000 shares of LTC stock at $17.50 per share over a four-year period. TI is also free to add the LTC parts to its standard cell library in exchange for specific royalty payments outlined by the agreement. LTC designers are to gain access to TI's CAD system and will also be able to design parts, thereby taking advantage of TI's advanced processes. The two companies plan joint designs in the near future. LTC will be able to situate its own test systems at TI assembly facilities.
LSI Logic Case Technology	March 1987	Case Technology Inc. and LSI Logic have completed a joint development effort that allows LSI Logic's LL5000, LL8000, and LL9000 schematic libraries to be designed on Case Technology's PC-based workstations.
LSI Logic Logic Automation	May 1987	LSI Logic Corporation and Logic Automation Inc. have signed a joint development agreement to make available LSI Logic's LL5000, LL7000, LL8000, and LL9000 channeled gate arrays on Logic Automation's Mentor Graphics workstations.
LSI Logic ASIX Systems	June 1987	LSI Logic Corporation will license design verification software to ASIX Systems Corporation of Fremont.

(Continued)

Table 2 (Continued)

AGREEMENTS WITH START-UP COMPANIES
FIRST HALF 1987

Company	Date	Comments
Samsung Intel	June 1987	Samsung Semiconductor will supply Intel with 64K, 256K, and 1Mb DRAMs, which Intel will sell to its customers in the United States. Shipments will begin from Korea in July.
Tachonics CMD	March 1987	California Micro Devices Corporation (CMD) signed an agreement with Tachonics for the production of gallium arsenide (GaAs) based ICs. Tachonics will manufacture the commercial and military products, and CMD will provide cell design and tools in the 0.5- to 1.0-micron range. Initial products will be a series of GaAs gate arrays with 500 to 2,500 gates and with radiation-hardened capabilities.
TriQuint TRW	June 1987	TRW Components and TriQuint Semiconductor have agreed to jointly supply gallium arsenide devices for space applications. Both companies are working together on procedures for producing Class S-level GaAs components. TriQuint will provide microwave and digital GaAs technology in addition to foundry services.
Vitesse Ford	June 1987	Vitesse Semiconductor Corporation and Ford Microelectronics are close to a second-source agreement involving gallium arsenide (GaAs) IC foundry services. The two companies have an agreement in principle to develop common design rules. Vitesse and Ford each use an enhancement/depletion mode, self-aligned gate technology. Initially, the agreement involves custom and semicustom circuits but may be extended to standard products.

(Continued)

Table 2 (Continued)

AGREEMENTS WITH START-UP COMPANIES
FIRST HALF 1987

Company	Date	Comments
VLSI Technology TCMC	March 1987	VLSI Technology Inc. and Thomson Components-Mostek Corporation (TCMC) have signed a comprehensive agreement for mutual second-sourcing and future new product development in specialized memory products. Each company will provide five existing memory designs for immediate second-sourcing. Both companies will incorporate the devices into megacells for use in their respective ASIC product families and plan to develop future products. Products covered include FIFOs, dual-ported RAMs, cache-tag RAMs, and lithium cell-powered nonvolatile SRAMs.
VLSI Technology Zilog	May 1987	Zilog signed VLSI Technology Inc. as a second source for its Super8 microcontroller. Included in the agreement are the Super8, the Z8038 FIFO I/O interface unit, and the Z8060 FIFO buffer unit and FIFO expander.
VTC Inc. TRW Components	March 1987	VTC and TRW Components International have signed a three-year agreement to cross sample space-quality Class S devices. VTC will supply TRW with unpackaged, high-performance ICs that meet the military Class S specifications. The devices include radiation-hardened CMOS SRAMs and high-speed comparators, op amps, and transceivers that are manufactured with VTC's radiation-hardened bipolar technology. TRW will assemble, test, qualify, and market these devices to customers that require Class S products, including radiation lot qualification where required.
Weitek Hewlett-Packard	May 1987	Weitek Corporation and Hewlett-Packard (HP) have formed a supplier/end-user agreement involving product and manufacturing exchanges. HP will incorporate the Weitek model 2264/65 chip set for high-performance, floating-point computation in current and future HP Precision Architecture computers. HP will also manufacture the chip set using its 1.2-micron CMOS process.

Source: Dataquest
August 1987

COMPANY ANNOUNCEMENTS

Altera Corporation

Altera and Monolithic Memories Incorporated (MMI) have settled the patent infringement suit brought against Altera by MMI. Altera agreed to entry of a consent of judgment, and the parties have agreed to license each other under certain patents in the programmable logic field.

Catalyst Semiconductor

Stephen Michael, one-time vice president of GE Semiconductor's Custom Integrated Circuit department, joined Catalyst as executive vice president and chief operations officer. He will have responsibility for all day-to-day operations at Catalyst, reporting directly to B.K. Marya, president and chief executive.

Dallas Semiconductor

Dallas Semiconductor began producing chips in a newly constructed $10 million wafer fabrication facility adjacent to its Dallas headquarters. The Class 1 facility produces CMOS chips with geometries down to 0.7 microns.

GigaBit Logic

GigaBit Logic named president and chief executive John Heightly chairman of the board. Mr. Heightly takes over the chairman's post from Henrich Krabbe, who will remain on GigaBit's board as director. Mr. Krabbe is vice president of new business development for Analog Devices, an investor in GigaBit.

GigaBit Logic announced that Cray Research, Inc., has increased its 1987 order to $5.5 million from $3.2 million. Cray will use the logic and memory device procured under this order to enter the next phase of development of a GaAs-based parallel processor supercomputer.

Integrated Device Technology (IDT)

IDT has established a company in Japan named Integrated Device Technology K.K. It is capitalized at $142,857 and plans to begin contract assembly in Japan, by Japanese semiconductor makers, sometime this year.

International Microelectronic Products (IMP)

IMP made an initial public offering of 6.5 million shares of common stock on June 10, 1987. The company provided 4.5 million shares and 2 million were from certain shareholders. The offering was underwritten by Shearson Lehman Brothers and Montgomery Securities. Proceeds will be used to acquire capital equipment, make leasehold improvements, redeem Series A preferred stock, and provide working capital for general corporate purposes. The company will have about 25 million shares outstanding after the offering.

IXYS Corporation

IXYS has relocated into a new 53,000-square-foot facility in San Jose. The facility, which is six-times larger than its former one, will be occupied by a highly automated assembly line and custom-packaging facility. The automated manufacturing line for commercial products is expected to be operational in eighteen months. IXYS plans to invest $2 million to $3 million in this line over the next two years.

Laserpath

Jim Hively, formerly general manager of Monolithic Memories Inc. semicustom division, has joined Laserpath as president and chief executive officer. Mr. Hively replaces former Laserpath president Michael Watts, who resigned last summer to participate in venture financing. He will report to Laserpath chairman John Mumford.

Lattice Semiconductor Corporation

Lattice filed for Chapter 11 protection to ensure that new funding will be applied only toward financing the company's ongoing operations.

LSI Logic Corporation

LSI Logic announced that it will take its Canadian affiliate, LSI Logic Corporation of Canada Inc., public and offer 4 million newly issued shares. The company plans to raise more than $20 million in the offering.

LSI Logic and Sun Microsystems Inc. announced that they are joining forces to support San Jose State University with the establishment of an ASIC laboratory (ASIC Laboratory Project) at the university. LSI will contribute instructional versions of its LDS-III logic design and verification software and instructional versions of a macrocell library to develop ASICs. Sun Microsystems will donate the SUN-3/160C color workstation and three SUN-3/50 monochrome workstations, as well as the operating system (SunOS) and networking software.

NMB Semiconductor Corporation

William C. Connell, vice president of NMB (USA) Inc., is acting president of NMB Semiconductor. Gary Ater, who was vice president and general manager of U.S. Operations, has left NMB Semiconductor to join Vitelic Corporation as vice president of Sales and Worldwide Marketing.

NMB Semiconductor relocated its domestic headquarters to Garden Grove, California, in April. NMB will share existing facilities with HI-TEK Corporation, another subsidiary company of NMB (USA) Inc. The new location provides additional space for engineering and test and evaluation functions. The existing Santa Clara, California, facility will be maintained as a regional office for the northwestern United States.

The new location is:

11621 Monarch Street
Garden Grove, CA 92641
(714) 897-6272; fax: (714) 891-0895; Telex: 67-8486

Samsung Semiconductor Inc.

Samsung Semiconductor, Goldstar Semiconductor Inc., and Hyundai Electrical Engineering Co. announced that they are preparing to launch full-scale production of a 1Mb DRAM chip jointly developed by the three South Korean firms last year.

Samsung Semiconductor formally opened its national headquarters in San Jose. The new $36 million facility will be used for administration, including sales, marketing, and product support, as well as for chip manufacturing. The company employs 250 people at the site and expects to increase that number to 400 within a year.

Silicon Systems Inc.

Chairman Carmelo J. Santoro retook operational control of Silicon Systems in May 1987, after Stephen E. Cooper, president and chief operating officer, and John V. Crosby, senior vice president, resigned.

Mr. Santoro said the reason for the change was to move toward a leaner, more efficient organization to "substantially improve profitability."

Taiwan Semiconductor Manufacturing Company (TSMC)

Dr. Morris Chang, former president and chief executive officer of General Instrument Corporation and president of the Industrial Technology Research Institute (ITRI) in Hsinchu, was made chairman of TSMC. Dr. Chang is also chairman of United Microelectronics Corporation.

Jim Dykes, who set up General Electric Company's Semiconductor Division, will join TSMC as president and chief executive officer.

Stephen L. Pletcher, who had been vice president of sales and marketing for GE Semiconductor, was named director of the new North American and European marketing and sales operation of TSMC.

TSMC, formed in late 1986, has already made its first wafer shipment from its 6-inch CMOS fab line in Hsinchu, Taiwan.

Three-Five Semiconductor Corp.

Three-Five Semiconductor has closed down its gallium arsenide facility in Troy, Michigan, idling about 50 workers.

United Microelectronics Corporation (UMC)

Dr. Morris Chang has been elected chairman of UMC. Dr. Chang is also chairman of the newly established Taiwan Semiconductor Manufacturing Corporation (TSMC) and president of the Industrial Technology Research Institute (ITRI) in Hsinchu. Formerly, Dr. Chang was a vice president at Texas Instruments and president and chief executive officer of General Instrument Corporation.

Vitesse Semiconductor

Vitesse has elected Pierre R. Lamond, cofounder of National Semiconductor and a general partner of Sequoia Capital, as chairman of the board. Mr. Lamond recently organized a $10 million financing of Vitesse and also serves on the boards of Cypress Semiconductor, Convex Computer, and several private companies.

VLSI Technology Inc.

VLSI Technology has broken ground on a 25,000-square-foot 6-inch wafer fabrication facility in San Antonio, Texas. Initially, the plant, equipped with a Class 1 clean room, will fabricate CMOS ASIC devices with minimum feature sizes down to 1.2 microns. The company plans features below 1.0 micron. The facility is expected to begin operation with 100 employees in late 1988.

VLSI Technology Inc.

VLSI Technology sold $48.75 million worth of 7 percent subordinated debentures convertible to common stock in an issue managed by Goldman Sachs & Co., Hambrecht & Quist, and Cowen & Co. VLSI plans to use money to fund new ASIC designs and defray expenses incurred by acquiring Visic Inc. and finance the new fab under construction in San Antonio, Texas.

In April, VLSI Technology repurchased a $7.6 million warrant that had been issued to Bendix Corporation six years ago.

VTC Inc.

VTC announced that it was awarded a $7.5 million contract from Control Data Corp., Government Systems Division, to supply chips for the U.S. Navy's AN/AYK-14(V) standard airborne computer. The contract calls for the production of five VLSI chip types designed with VTC's 1-micron CMOS standard cell library.

Xicor, Inc.

In April 1987, Xicor announced a public offering of 2.1 million shares of common stock at a price of $11.50 with Montgomery Securities and Smith Barney, Harris Upham & Co. Incorporated acting as underwriters. Net proceeds will be used for repayment of a bank debt of approximately $1.5 million and the balance will be added to working capital.

Intel Corporation has terminated a contract worth more than $7 million with Xicor on EEPROM technology and has begun end-of-life procedures on 64K and 256K ICs.

Zoran Corporation

John Ekiss resigned as president and chief executive officer of Zoran. Before joining Zoran in mid-1985, Mr. Ekiss was general manager of Intel's special components division. Terry Martin, vice president of operations, is acting president and chief executive.

ZyMOS Corporation

David Handorf has joined ZyMOS as president and chief executive officer from VLSI Technology Inc., where he was general manager of application-specific memories. He replaces the president's office of Haller Moyers, B.J. Chang, and Alex Young, who were appointed to serve until a successor was named.

Mark Reagan
Penny Sur

Dataquest
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Research Newsletter

SEMS Code: 1986-1987 Newsletters: August 1987-17

SYNCHROTRON ORBITAL RADIATION: JAPAN'S PUSH INTO ULTRADENSE MEGABIT MEMORIES

SUMMARY

Since early 1986, Japanese companies have accelerated their research into X-ray lithography using synchrotron orbital radiation (SOR) technology to develop 64Mb+ (megabit+) memories. Current optical steppers are capable of submicron geometries, but it is believed that they will reach a manufacturing limit between 0.25 and 0.50 micron, despite expected advances in mask and photoresist technologies. Below that level, researchers are exploring various approaches, including excimer lasers, X-ray lithography (plasma and SOR), e-beam, and ion beam. Since the introduction of the Compact Synchrotron (COSY) by BESSY GmbH of West Germany, SOR has attracted intense attention in Japan because of its high wafer throughput, making it ideal for mass production.

Currently, Japanese government laboratories are focusing on basic SOR technology, while Japanese companies are developing compact SOR rings and advanced resists for near-term commercialization. A few of the key projects are the following:

- In June 1986, 13 companies formed Sortec, a quasigovernment corporation under the auspices of MITI and the Ministry of Posts and Telecommunications (MPT), which will build a testing lab in Tsukuba by 1989.
- In late 1986, NEC and Toshiba separately tested SOR prototypes capable of 0.25- to 0.30-micron geometries.
- NEC and Sumitomo Heavy Industries are jointly developing a compact SOR ring with a diameter of less than 1 meter (m).
- In fiscal 1987, the Science and Technology Agency (STA) has allocated ¥69 million ($492,000) to investigate SOR technology at its Physical Research Laboratory (Riken).

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 971-9000, Telex 171973

Dataquest believes that compact SOR rings will be used to develop prototype 64Mb+ memories during the late 1980s. West Germany and Japan are currently leading in SOR commercialization, but the United States has a strong scientific base at its national laboratories. The recently proposed Sematech is one effort to maintain parity in next-generation semiconductor manufacturing technology. Compact SOR rings should clearly be one of its research goals.

MEGABIT MEMORIES PUSH DEMAND FOR ADVANCED EQUIPMENT

Since 1981, Japanese memory technology has advanced at a rate of two years per density level, as reflected by technical papers announced at the International Solid State Circuits Conference (ISSCC) by Nippon Telegraph and Telephone (NTT). In recent years the pace has quickened. As shown in Table 1, only one year elapsed between the 1Mb and 4Mb, and the 4Mb and 16Mb papers.

Table 1

MEMORY DEVICE TECHNOLOGY TRENDS*

Device	Prototype	Line Width (Microns)	Technology
64K	1981	3.0	1:1 projection
256K	1983	2.0	5:1 g-line steppers; projection
1Mb	1985	1.0-1.3	5:1 g-line steppers
4Mb	1986	0.7-0.8	5:1 g- or i-line steppers
16Mb	1987	0.5	X ray, excimer laser, e-beam
64Mb	1990	0.30-0.35	X ray, excimer laser, SOR, e-beam
256Mb	1992-93	0.20-0.25	SOR, e-beam, focused ion beam
1Gb	1994-96	0.18	SOR, focused ion beam

*Development of working prototypes, not commercial samples

Source: Dataquest
August 1987

Despite the accelerated pace of memory development, commercialization remains a major problem for the industry. Currently, the U.S.-Japan Semiconductor Trade Arrangement may be prolonging the life cycle of 256K DRAMs, which could affect future generations. For example, mass production of 1Mb DRAMs began only recently despite their being commercially available for over a year. Will production of 4Mb DRAMs be similarly delayed to avoid cannibalizing 1Mb DRAMs? Will the current prolongation of 256K DRAMs force semiconductor makers to develop new applications, such as

video RAMs, silicon disks, and speech recognition chips, in order to utilize megabit memories sooner? If so, will these new applications become the industry drivers? How will they influence the introduction of 4Mb and 16Mb DRAMs?

Despite the applications lag, or perhaps due to these emerging applications, Japanese makers are pushing into ultradense memory devices. Efforts to develop working 16Mb DRAM prototypes and basic research on 64Mb DRAM processes are well under way at major Japanese semiconductor R&D centers. Compact SOR rings are central to these research efforts.

NEXT-GENERATION EQUIPMENT TRENDS

Japanese companies are developing various types of lithography equipment for megabit memories, including excimer lasers, optical steppers, plasma X rays, SOR, hybrid beam sources, reactive ion etchers, and direct-write e-beams. Table 2 shows prototype production equipment announced by major Japanese companies in 1986.

Table 2

JAPANESE SUBMICRON EQUIPMENT ANNOUNCEMENTS

Date	Company	Micron	Mb	Announcement
Q1/86	Hitachi	0.6	4Mb+	Wafer stepper (RA-101VL)
Q1/86	Mitsubishi/TEL	N/A	16Mb	Plasma excimer laser
Q1/86	Sumitomo Metal	N/A	N/A	Experimental reactive ion etcher using electron cyclotron resonance
Q2/86	Toshiba/ Toyohashi Univ.	N/A	64Mb	Hybrid ion beam system
Q2/86	Matsushita	0.1	64Mb+	Conventional e-beam system
Q2/86	JEOL	0.1	64Mb+	Ion beam system (JIBL 150)
Q2/86	Japan Steel	0.2	16Mb	Ion beam etcher using electron cyclotron resonance (ECR)
Q2/86	Mitsubishi	0.3	4Mb	X-ray lithography system
Q2/86	NTT	0.5	16Mb	Prototype e-beam system (EB60)
Q2/86	Sumitomo Heavy	N/A	4Mb+	1m-diameter SOR ring technology
Q3/86	NTT	0.3	64Mb	Plasma X-ray source
Q3/86	Hitachi/MOE/ Toyohashi Univ.	N/A	64Mb	Hybrid beam source
Q3/86	JEOL	0.3	N/A	e-beam system (JBX6AIII)
Q3/86	Nikon/NTT	N/A	N/A	Direct-write e-beam system
Q3/86	Seiko Instrum.	0.1	N/A	Ion beam machine (SMI-3M)
Q3/86	Toshiba	0.35	16Mb	Krypton fluorine (KrF) excimer laser
Q3/86	Hitachi/NTT	0.1	64Mb+	Direct-write e-beam system (EB-F)
Q4/86	Matsushita	0.4	64Mb	KrF excimer laser
Q4/86	NEC	N/A	N/A	KrF excimer laser

(Continued)

Table 2 (Continued)

JAPANESE SUBMICRON EQUIPMENT ANNOUNCEMENTS

Date	Company	Micron	Mb	Announcement
Q4/86	NEC	0.25	64Mb	Prototype SOR system
Q4/86	Nikon	0.35	16Mb	Current stepper and multilayer resist
Q4/86	Matsushita	0.5	16Mb	Holographic wafer stepper
Q4/86	NTT/Nichicon Capacitor	0.5	16Mb	Gas-injection plasma X-ray source
Q4/86	Nikon	0.35	4Mb	Conventional optical stepper
Q4/86	Toshiba/Tokuda	Sub-0.50	16Mb-64Mb	Automated reactive ion etcher
Q4/86	Anelva	N/A	4Mb	Reactive ion etcher (ILD-4031)
Q4/86	NTT	0.3	64Mb	Plasma X-ray source
Q4/86	Tokyo Ohka	N/A	4Mb	ECR etcher (TSMe-5300)

N/A = Not Available

Source: Dataquest
August 1987

WHAT IS SYNCHROTRON ORBITAL RADIATION?

A synchrotron is an oval- or doughnut-shaped machine that uses powerful magnets to accelerate electrons to almost the speed of light. It bends the orbit of the light by applying strong magnetic fields to generate high-energy X-ray beams from the accelerated electrons. These beams can be used to draw ultrafine circuit patterns for 16Mb and higher density memories and other ICs. SOR has several unique characteristics:

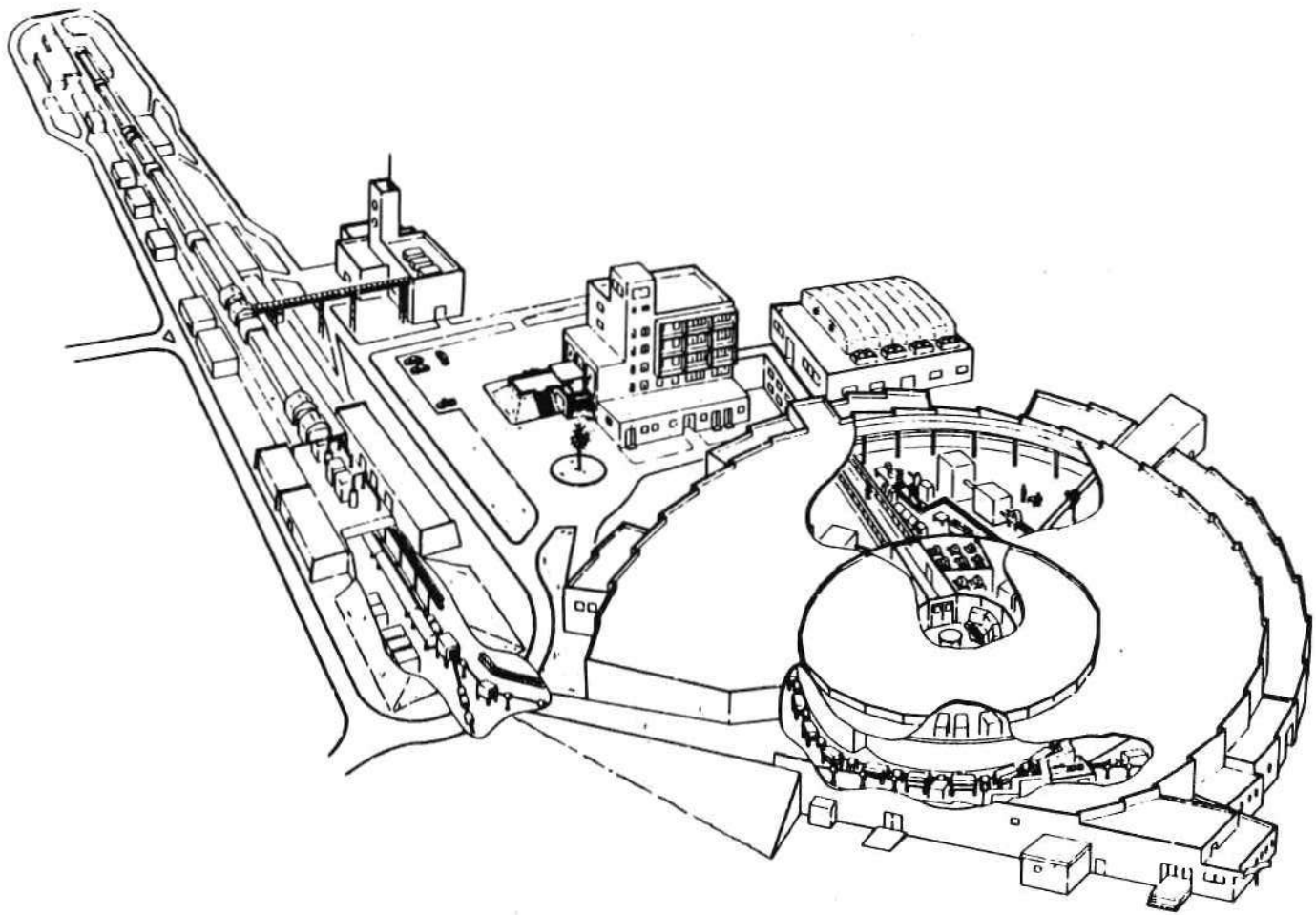
- Brightness--Its very tight beam is 100,000 times more intense than any other X-ray source, enabling faster, clearer exposures.
- Tunability--Unlike lasers, which can produce light only at discrete energies, SOR can be tuned to any frequency throughout its entire spectrum.

In a synchrotron, the electrons emit energetic radiation throughout the infrared to high-energy X-ray region. As the size of the SOR ring increases, the radiation expands into the high-energy spectrum. Stronger magnets increase the intensity of the e-beam. Although the National Synchrotron Light Source at the Brookhaven National Laboratory and other U.S. laboratories pioneered large oval-shaped synchrotron rings for basic research, the Japanese are focusing on compact, circular SOR rings for IC production.

Figure 1 shows the SOR Photon Factory operated by the Ministry of Education's High-Energy Physics Laboratory in the Tsukuba Science City. The 28m-diameter ring is capable of generating 2.5 GeV of electron energy. Figure 2 shows the 1m-diameter SOR ring announced by Sumitomo Heavy Industries in November 1986 at the Ninth Conference on Accelerator Applications in Research and Industry in Denton, Texas. The Sumitomo Heavy ring uses a superconducting, weak-focusing single-body magnet to inject high-energy e-beams into a small SOR ring at 150 MeV. The beam is then accelerated to 650 MeV to draw submicron geometries on silicon substrates. The machine is 3.0m in outer diameter and 2.2m in height.

Figure 1

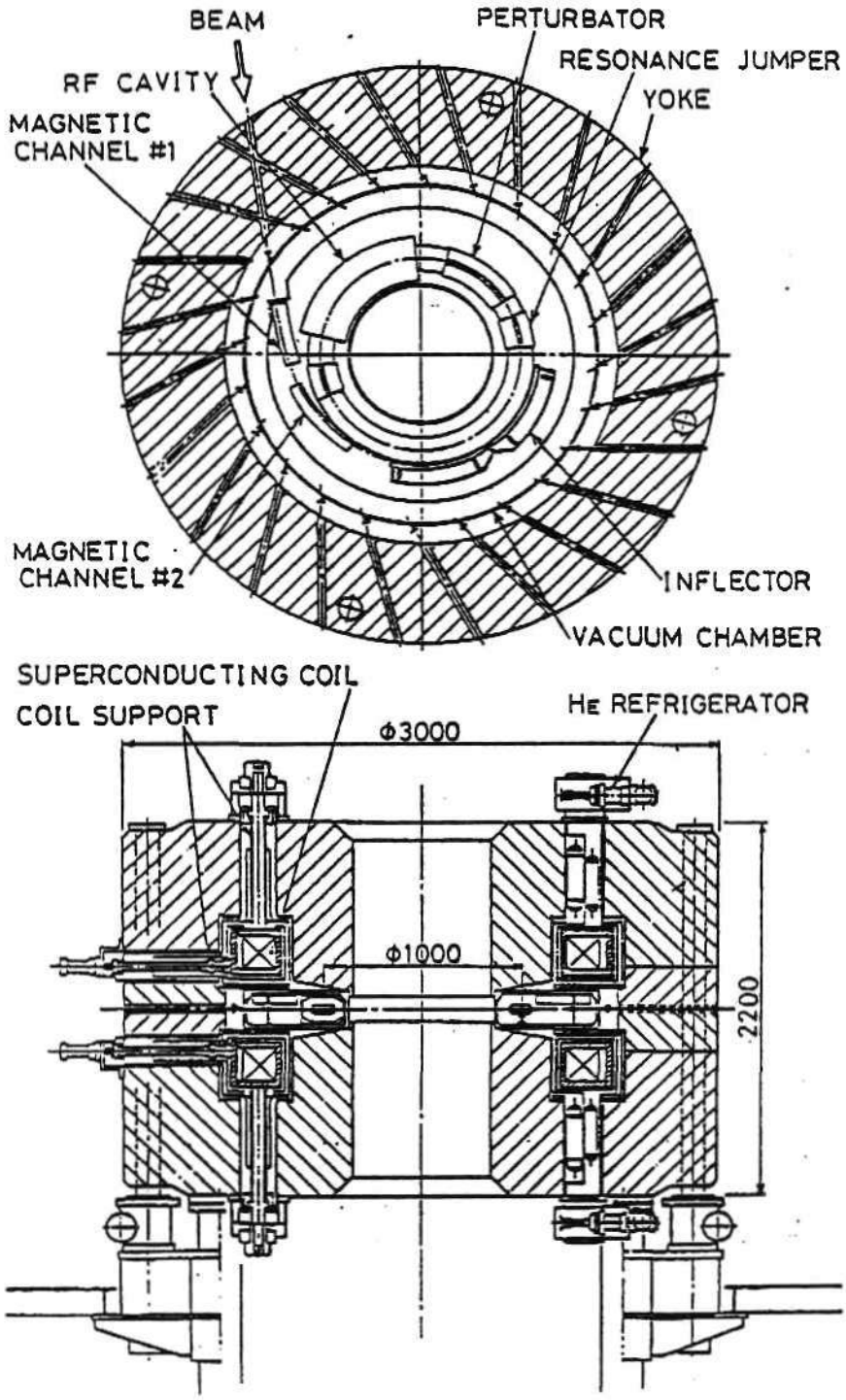
SOR PHOTON FACTORY IN TSUKUBA SCIENCE CITY



Source: Ministry of Education

Figure 2

SUMITOMO HEAVY'S 1m-DIAMETER COMPACT SOR RING



Source: Sumitomo Heavy Industries

WHY SYNCHROTRON ORBITAL RADIATION?

Why is SOR being pursued so avidly by the Japanese? Currently, research on megabit memory equipment is focused on six areas: optical steppers, excimer lasers, conventional plasma X rays, SOR, focused ion beam (FIB), and direct-write e-beam. However, as shown in Table 3, technical disadvantages limit the use of most of these technologies in manufacturing. Optical steppers are expected to reach their physical limits soon, since existing visible light and ultraviolet lithography is limited to about 0.25 to 0.50 microns. Prototype 0.35-micron patterns have been drawn by optical steppers, but there is still uncertainty over the ultimate linewidths that can be practically implemented in mass production. X-ray steppers with excimer lasers are capable of drawing sub-0.5-micron line widths for 16Mb DRAMs, but lens and laser improvements are still being developed. Excimer lasers are capable of extending the use of optical steppers for mass production, but further lens and laser improvements are required before they can be commercialized. Plasma X ray, direct-write e-beam, and FIB offer sub-0.5-micron capabilities but suffer from low wafer throughput, which limits their use to small volumes. Figure 3 illustrates the potential use of various submicron lithography methods.

On the other hand, SOR offers two features that the Japanese value highly in manufacturing: excellent depth of focus (fine-line capability) and high wafer throughput (volume production). Japanese researchers are focusing on SOR technology because it offers the highest wafer throughput of all X-ray techniques, and can theoretically achieve 0.1- to 0.2-micron geometries for 64Mb and 256Mb memories. Moreover, if compact SOR rings are developed, SOR rings can be used with steppers on existing fab lines.

However, SOR technology faces several technical hurdles. X-ray masks are difficult to produce and pattern because they are fragile, being made of thin membranes only 2.0 to 3.0 microns thick, unlike the thicker glass or quartz plates used in optical masks. Thicker SOR masks could be used, but they would stop X rays and reduce contrast, requiring vertical steppers to expose multiple chips per wafer. Japan is currently lagging both West Germany and the IBM Brookhaven operation in the development of vertical steppers.

Another problem is the mask distortion resulting from thermal stresses occurring between the silicon substrate and gold or tungsten X-ray-absorbing material, which presents problems for mass production.

Finally, cost and size will be obstacles to immediate commercialization. Existing SOR rings cost about ¥1 billion ($7.1 million) and require significant floor space, limiting their use to large mass-production lines. Japanese makers are vigorously working to develop sub-1m-diameter rings to make SOR more space- and cost-effective for market-niche semiconductor production.

Table 3

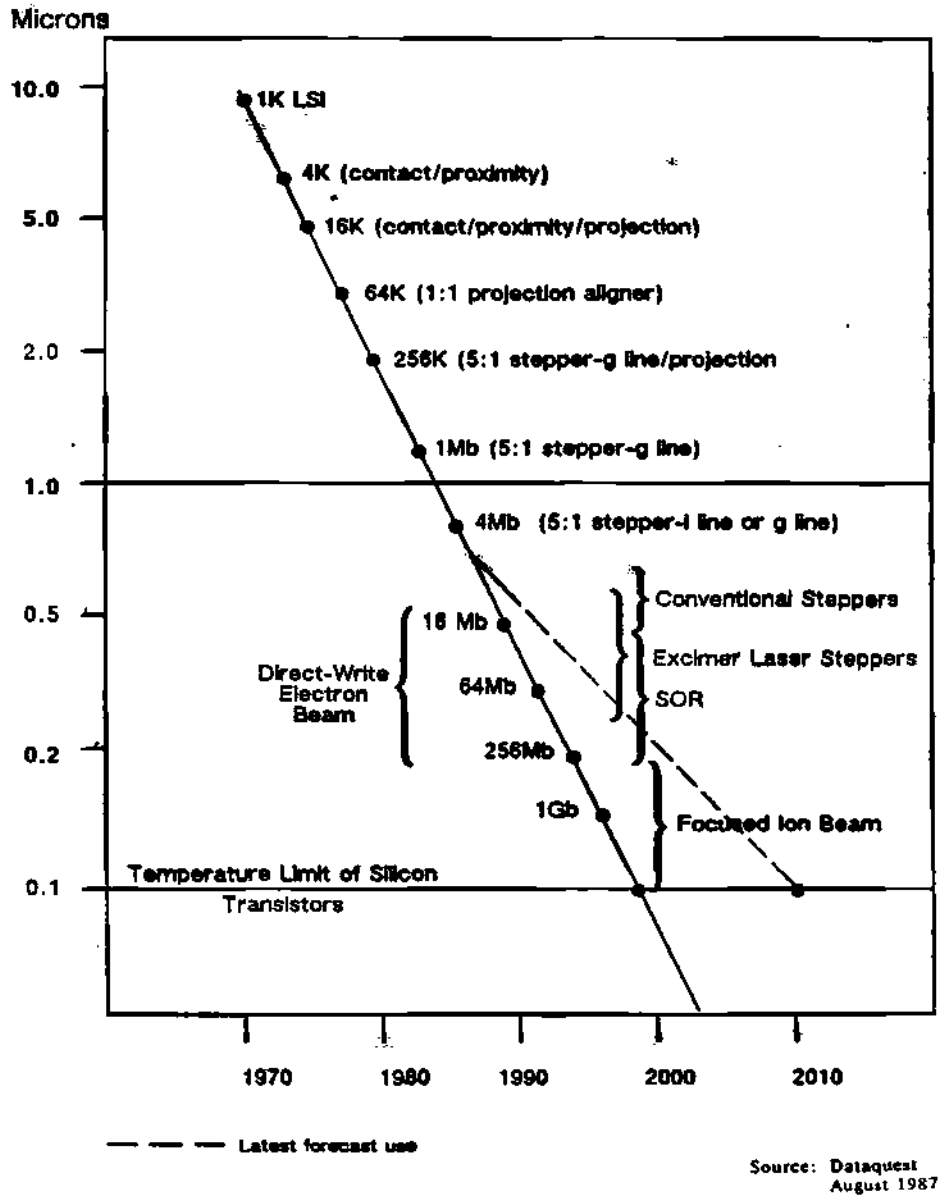
COMPARISON OF SUBMICRON LITHOGRAPHY APPROACHES

Technology	Advantages	Disadvantages
Optical Stepper (to 0.5 micron)	Familiar technology High wafer throughput	Resolution limited to 0.25 micron Pushing technical limits (depth of focus)
Excimer laser (0.6-0.35 micron)	Continued use of optical steppers possible High resolution High wafer throughput	Satisfactory lens and laser technology still being developed
Plasma X-ray (0.5-0.25 micron)	Depth of focus High resolution	Low wafer throughput Unfamiliar technology Sources, masks, and photoresists still being developed
Direct-write e-beam (0.5-0.2 micron)	Commercially available High resolution Maskless (fast ASIC turnaround time)	Low wafer throughput Complex system
SOR (0.25-0.1 micron)	Depth of focus High resolution High wafer throughput	Sources, masks, and photoresists still being developed Complex system
Focused ion beam (sub-0.2 micron)	High resolution Maskless process Serial writing (niche markets)	Low wafer throughput Unfamiliar technology

Source: Dataquest
August 1987

Figure 3

LITHOGRAPHY TECHNOLOGY TRENDS



Source: Dataquest
August 1987

SOR RESEARCH IN JAPAN

SOR was originally developed in 1947 by General Electric, which developed a circular 70 MeV high-speed electron synchrotron. The first Japanese experiments were conducted in 1977 by Susumu Namba of Osaka University's engineering science faculty, using the storage ring at Tokyo University's Institute for Nuclear Study. Since then, numerous SOR projects have been established in Japan. As shown in Table 4, five government laboratories are involved: the Ministry of Education's High-Energy Physics Laboratory, MITI's Electrotechnical Laboratory, Osaka University, Nagoya University, and the STA. In the early 1990s, two technopolis regions are planning SOR research facilities. Japanese companies are focusing primarily on compact SOR rings that can be commercialized.

Table 4

JAPANESE SOR RESEARCH ACTIVITY

Date	Company/Agency	Research Focus
1977	Osaka University, Faculty of Engineering Science	Basic research using Tokyo University SOR ring
10/81	MITI Electrotechnical Lab	10m-diameter octagonal SOR ring with undulating beam
1982	MOE High-Energy Physics Lab	10m-diameter SOR for 1Mb+ DRAMs
1984	Nagoya University/ Meijo	Basic SOR research by Molecular Science Laboratory
02/86	MITI Electrotechnical Lab/ Sumitomo Electric	4.19m-diameter SOR for VLSI
06/86	Sortec (13 companies)/ MITI	Ultrasmall SOR basic technology
06/86	Sumitomo Heavy Industries	Developing 50cm-diameter SOR ring for 16Mb+
11/86	NEC Microelectronics Lab	0.25-micron pattern drawn using MOE High-Energy Physics Lab's SOR
11/86	Toshiba	SOR-applied stepper with 0.03-micron alignment precision developed
05/87	MOE High-Energy Physics Lab	60-70 GeV TRISTAN (Transposable Ring Intersecting Storage Accelerator)

(Continued)

Table 4 (Continued)

JAPANESE SOR RESEARCH ACTIVITY

Date	Company/Agency	Research Focus
12/87	NEC/Sumitomo Heavy SOR Research Lab	Joint 50cm-diameter SOR ring hardware and software development
1988	NTT/Hitachi/Toshiba	SOR ring for 64Mb+ DRAMs
1988*	Kamo Science City (Hiroshima Technopolis)	Plans for SOR development center
1989	Science & Technology Agency	Large-scale SOR at Kansai Science & Technology Basic Research Lab
1990	Osaka University Kyoto University	Plans for a 6-GeV SOR development (either at Tsukuba or West Harima Technopolis near Kobe)

*Still in planning phase; synchrotron construction would begin in 1988 if plans are approved.

Source: Dataquest
August 1987

The following paragraphs are short descriptions of major SOR research activities, as listed in Table 4, being conducted at Japanese ministries and corporations.

MITI Electrotechnical Laboratory

In October 1981, MITI's Electrotechnical Laboratory in the Tsukuba Science City developed a 10m-diameter SOR with an octagonal configuration based on the work of Takio Tomimasu, director of the lab's Quantum Technology Division. The electrons are accelerated by a 70m linear accelerator into a 2m-radius orbit along a 31m electron path. A major contribution has been the use of undulating e-beams to widen the X-ray beam to 25mm at 10m, which is not quite large enough for 40 x 40mm exposure areas generated by current steppers.

Ministry of Education High-Energy Physics Laboratory

Since the spring of 1982, the Ministry of Education's (MOE's) High Energy Physics Laboratory in the Tsukuba Science City has operated an electron linear accelerator 400m in length and an electron storage ring 180m in circumference (28m in diameter) to conduct SOR research. The linear accelerator is capable of 2.5 GeV. More recently, the lab has developed a 10m-diameter 645 MeV SOR ring, which is being used by Fujitsu, Hitachi, NEC, and NTT for their megabit-memory research.

In October 1986, the TRISTAN (Transposable Ring-Intersecting Storage Accelerator in Nippon) was completed at a cost of ¥87 billion ($620 million) after five years of construction. The 60-70-GeV facility puts it ahead of the 42-43 GeV particle accelerator in West Germany. To date, the accelerator achieved a record energy output of 50 GeV in a trial run. Professor Sukeyasu Yamamoto of Tokyo University, a project coordinator, will lead research on the sixth quark, the key to understanding the nature of matter and the origin of the universe.

Nagoya University/Meijo

Since 1984, Nagoya University's Molecular Physics Laboratory has conducted basic research on SOR technology.

MITI/Sumitomo Electric

MITI's Electrotechnical Laboratory (ETL) is working on two SOR projects. In February 1986, MITI and Sumitomo Electric jointly developed and tested a 4.19m-diameter compact SOR test ring (NIJI-1), using eight magnets. The maximum stored current of 200mA was achieved at an injection energy of 160 MeV. Currently, new 4m-diameter rings are being developed under contract by a consortium of Mitsubishi Electric, Shimadzu, Sumitomo Electric, and Toshiba. A superconducting-magnet SOR ring will accelerate electrons around a 10m-long circular racetrack, and be linked to a 10m-long linear accelerator with an energy potential of 150 MeV. Tomimasu is coordinating both projects.

Concurrently, Sumitomo Electric is perfecting a sub-1m-diameter electron accumulating ring, the core of the SOR machine, which would make it the world's smallest synchrotron. The MITI/MPT (Ministry of Posts and Telecommunications) New Technology Development Corporation granted Sumitomo a consignment loan of ¥1.2 billion ($8.6 million) to develop a commercially viable compact SOR by 1989.

To support these efforts, MITI is developing basic mask, stepper, mark-detection, and alignment technology, and the use of sensors and actuators at its ETL Electronic Device Division, which is headed by Toshio Tsurushima. Japan Synthetic Rubber, Sanyo, and other companies are developing X-ray resists, as shown in Table 5.

Table 5

JAPANESE PHOTORESIST AND MATERIALS ANNOUNCEMENTS

Date	Company	Design Rule	DRAM	Announcement
Q2/86	Mitsubishi	N/A	4Mb	Negative-type X-ray resist
Q3/86	Matsushita	0.1	64Mb+	Polymethyl methacrylate resist
Q4/86	Japan Synthetic Rubber	0.8	N/A	Positive e-beam resist (PFR7700)
Q4/86	Japan Synthetic Rubber	0.4	N/A	Negative X-ray resist (MES-X)
Q4/86	Matsushita	0.3	64Mb	Langmuir-Blodgett photoresist
Q4/86	Sanyo Electric	0.75	4Mb+	Positive e-beam resist (SEBR-115)
Q4/86	Toshiba	0.5	16Mb	Double-layer ultraviolet photoresist

N/A = Not Available

Source: Dataquest
August 1987

Sortec/MITI/MPT

In June 1986, the government-regulated Japan Key Technology Center and 13 Japanese semiconductor device and equipment makers formed Sortec, a joint venture company, to develop SOR generating equipment by 1995. The company was capitalized at ¥214.3 million ($1.5 million). Participating companies, which are members of MITI's Future Electron Devices Project, include Canon, Fujitsu, Hitachi, Matsushita Electric, Mitsubishi Electric, NEC, Nikon, Oki Electric, Sanyo, Sharp, Sony, Sumitomo Electric, and Toshiba. The Key Technology Center is under the auspices of MITI and MPT.

Sortec plans to spend ¥14.3 billion ($102 million) during the 10-year R&D program, of which 70 percent will be funded by the Key Technology Center and 30 percent by the participating companies. The staff will peak at 40 to 50 full-time researchers. During our visit in 1986, Dataquest observed that many Sortec researchers are former members of MITI's VLSI Project. Their goal is to develop compact, practical SOR equipment that can be installed in semiconductor wafer manufacturing plants. Current 4m- to 10m-diameter SOR systems are too large to be installed in plants.

In June 1987, Sortec announced that Hitachi, Mitsubishi, Sumitomo Electric, and Toshiba are planning joint design and production of SOR equipment.

Toshiba

In November 1986, Toshiba successfully test-produced an SOR-applied stepper system capable of 0.5-micron geometries for 16Mb DRAMs, paving the way for 64Mb DRAMs by the mid-1990s. The system has an alignment precision of 0.03 micron and a vertical aligning system in which X rays emitted from the SOR source are moved horizontally along vertically placed wafers. Toshiba, which is a member of Sortec, plans to commercialize its SOR system around 1990.

Sumitomo Heavy Industries/NEC

Sumitomo Heavy Industries, a member of Sortec, is using superconducting magnets to develop an ultrasmall 50cm-diameter SOR ring with an overall 3m diameter. The company has researched helium-cooled superconductors over the last 25 years and recently shifted from two superconducting magnets to one for its SOR ring, which was successfully tested. Unlike NTT, which is developing an SOR ring like COSY, Sumitomo is developing a proprietary circular superconducting magnet technology. By the end of 1987, Sumitomo Heavy and NEC plan to establish a joint research laboratory. NEC will develop an SOR hardware prototype and Sumitomo will write the software for an R&D unit by late 1988. Marketing will be done independently by both companies. Sumitomo plans to sample its SOR ring by 1990-1991.

NEC

In November 1986, NEC successfully drew a 0.25-micron pattern, which will eventually be used for 64Mb DRAMs, by using the large SOR ring at MOE's High-Energy Physics Laboratory in Tsukuba. The test pattern was 3.0 microns high and 0.25 micron thick.

In December 1986, NEC completed a prototype machine that uses SOR X rays to evaluate electronic materials. Developed at the "photon factory" of the MOE High-Energy Physics Laboratory, the machine measures distortions and atomic holes in silicon and GaAs materials used for optoelectronic ICs (OEICs). Possible semiconductor applications include the ability to evaluate the interface between two epitaxial layers in complex VLSI structures, such as superlattices.

NTT/Hitachi/Toshiba

NTT is constructing a 5m-diameter SOR ring at a cost of ¥7 billion ($50 million) to develop 64Mb+ DRAMs and other ULSI devices with Hitachi and Toshiba. Operation is scheduled for 1988. NTT's SOR technology is like the COSY machine, but reduced in size.

Kamo Science City

In September 1986, Hiroshima University issued an outline of its HiSOR Plan to develop an ¥8 billion ($57 million) Synchrotron Applications Research

Center at its Saijo campus, which is in the Kamo Science City of the Hiroshima Technopolis. The plan calls for building a 1.5-GeV synchrotron ring (25m diameter) and a 45-MeV electron storage ring (20m diameter). Construction would occur in three phases: synchrotron ring (1988-1989), storage ring (1989-1991), and beam channel testing equipment (1991-1992). The center would be staffed by 40 researchers and be open to government, university, and industry researchers throughout western Japan for advanced research in VLSI development, natural sciences, and basic physics. As shown in Table 6, the Hiroshima SOR would be the fifth synchrotron facility in Japan.

Table 6

SOR FACILITIES IN JAPAN

Research Center	Location	Facility
MOE High-Energy Physics Laboratory	Tsukuba Science City	2.5 GeV photon factory 8.0 GeV TRISTAN accelerator ring
Tokyo University Physics Department	Tokyo	0.4 GeV SOR facility 4.0 KeV photon energy
Nagoya University Okazaki Molecular Science Lab	Nagoya	0.6 GeV UVSOR facility
MITI Electrotechnical Laboratory	Tsukuba Science City	0.5 GeV TERAS facility
Hiroshima Synchrotron Applications Research Center	Kamo Science City (Hiroshima)	1.5 GeV SOR ring 45.0 MeV electron storage ring

Source: Hiroshima University
Dataquest
August 1987

Science and Technology Agency

In 1989, STA plans to build a large-scale 6-GeV SOR ring in the Kansai (Osaka) region. Slated to cost ¥100 billion ($714.2 million), the project will involve STA's Physics Research Laboratory and the Japan Nuclear Power Research Laboratory. In November 1986, STA established the Large-Scale SOR Equipment Planning Office to conduct surveys of overseas and domestic SOR facilities. Two candidate sites are being evaluated by STA, industry leaders, local governments, and university professors. The SOR ring will be used in the early 1990s to conduct basic research in new materials, physics, life sciences, and VLSI manufacturing.

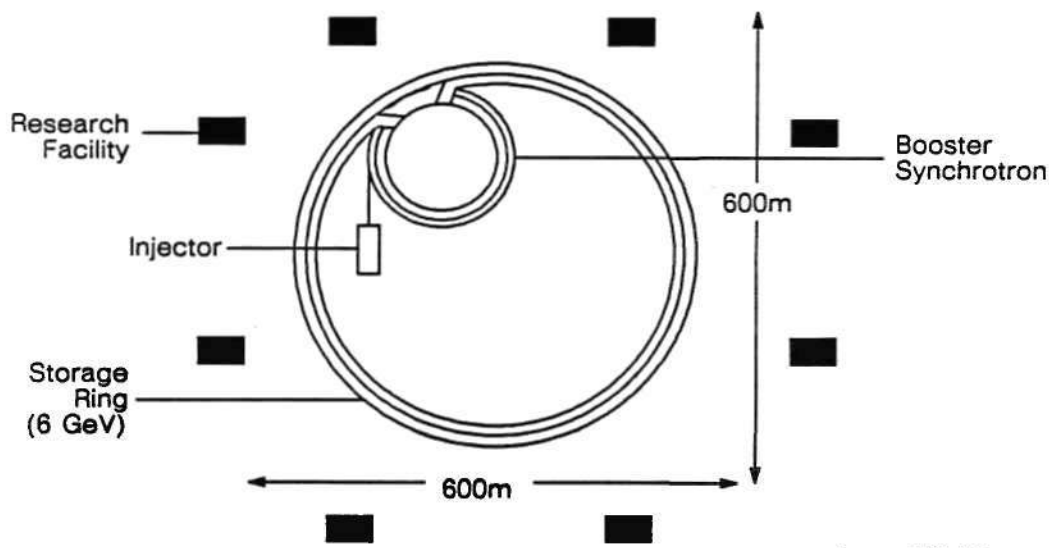
During fiscal 1986 through 1988, STA has allocated ¥412 million ($2.9 million) to develop new semiconductor manufacturing beam technology, including SOR, electron beam, and submicron analysis and evaluation techniques. Of this amount, STA allocated ¥69 million ($492,000) for SOR research at its Physics Research Laboratory in fiscal 1987.

Osaka University/Kyoto University

In February 1986, Osaka University and Kyoto University announced plans to construct an SOR Development Center by 1990 in either the Tsukuba Science City or West Harima Technopolis near Kobe. The facility would feature a booster SOR ring built within a 600m-diameter, 6-GeV SOR storage ring, as shown in Figure 4. The machine would be 1,000 times more powerful than the Tsukuba SOR facility. Research would focus on a broad range of submicron VLSI manufacturing and biological topics. Professor Masao Kakuto of Himeji University is the chairman of the SOR Development Center Promotion Association, which involves 100 scientists.

Figure 4

PLANNED 600m-DIAMETER RING WITH BOOSTER AT KANSAI SOR DEVELOPMENT CENTER



Source: Nikkei Sangyo

THE FAB-OF-THE-FUTURE

Japanese semiconductor makers are clearly interested in developing future VLSI plants that will utilize compact SOR rings for megabit DRAM and SRAM production. Dataquest believes that future ULSI fabs will utilize ultrasmall SOR equipment, such as the 0.5m-diameter SOR machine being developed by NEC and Sumitomo Heavy. Each plant is likely to be equipped with several SOR units, depending on per unit cost. We believe that SOR units will be used initially for preproduction R&D prototyping of next-generation DRAMs and SRAMs to refine them for eventual mass production.

SOR RESEARCH ACTIVITIES WORLDWIDE

Currently, the world leaders in SOR technology are the West Germans. Research on X-ray lithography began as a joint government-industry project at the Fraunhofer Institute for Microstructure Technology in West Berlin. Eurosil, Siemens, Telefunken, and Valvo contributed as subcontractors. Hoechst AG is producing X-ray resist and Karl Suss GmbH is working with Siemens AG on X-ray steppers. As shown in Table 7, the institute has developed a practical 4m x 2m SOR ring called COSY, which is being produced by BESSY GmbH. The project goal is to develop 0.5-micron geometries by late 1987 and 0.2- to 0.3-micron geometries by the mid-1990s. A COSY prototype has already achieved a 0.2-micron design rule.

Table 7

TECHNICAL PARAMETERS OF SMALL SOR RINGS

Parameter	COSY I	COSY II	NEYRPIC	MITI/ Sumitomo Electric	MITI/MPT Key Technology Corp.	Sumitomo
Diameter (meters)	Sub-2	4 x 2	5	4	Sub-4	3
Energy (MeV)	560	630	800	270 (800)	(615)	650
R (centimeters)	37	44	160	70 (160)	(50)	50
B (T)	5	4.5	1.7	1.29	(4.1)	4.34
I (mA) (h)	(300) 10	(100) 8	(100) 10	100 (10)	(200)	(300)
Arc (angstroms)	4.9	4.1	7.3	83	(5.0)	4.3
BL	8	12		(12)	(12)	

Source: Dataquest
August 1987

Recently, COSY Microtec GmbH, a West Berlin start-up funded by Leybold-Heraeus, Philips, Siemens, and Telefunken, developed a compact SOR electron storage ring developed by the Berlin Electron-Storage Ring Society for Synchrotron Radiation (BESSY) and the Fraunhofer Institute. The COSY storage ring (XRS 200), which sells for about $10 million, features two 180-degree superconducting magnets, and can be linked to Karl Suss X-steppers.

In May 1987, Karl Suss introduced a fixed-beam vertical proximity X-ray stepper with 0.2-micron resolution and 0.1-micron alignment accuracy for production runs using either an SOR or plasma-focus source. The Suss XRS-200 system is based on Suss' Max-1 X-ray system, which was been used since 1984 at the Fraunhofer Institute. It is priced at $1 million and handles up to 6-inch wafers.

In the United States, research is focused on X-ray lithography systems using plasma sources, with research on SOR picking up because of the challenge from West Germany and Japan. As shown in Table 8, there are five U.S. facilities: Brookhaven's National Synchrotron Light Source (NSLS), Cornell's High Energy Synchrotron Source (SOURCE), the National Bureau of Standards' SURF-II, Stanford's Synchrotron Radiation Laboratory, and the University of Wisconsin's Aladdin Light Source and Tantalus I. These centers are used by scientists from Allied, Bell Labs, General Electric, IBM, Merck, United Technologies, Xerox, and other U.S. companies. Major research activities include:

- AT&T Bell Labs--X-ray lithography using a water-cooled, electron-impact palladium source, boron nitride mask and high-sensitivity X-resists
- IBM Watson Research Center--SOR research at Brookhaven on 0.5-micron geometries, prototype vertical stepper, compact storage rings, and beam line design
- Micronix--Commercial X-ray stepper 0.5-micron geometries and mask substrates
- Perkin-Elmer--Optical, e-beam, and X-ray lithography work, including a high-speed, high-resolution e-beam system (Aeble 150) and VHSIC phase 2 work on a 0.5-micron prototype stepper using a plasma source

The race to develop SOR technology is spreading rapidly, as shown in Table 9. As a result, the U.S. Defense Science Board Task Force recently issued a report on the U.S. semiconductor industry's lagging competitiveness, which has stimulated interest in SOR research. In March, the Department of Defense announced a preliminary $1 million contract to Brookhaven National Laboratories to design a compact SOR X-ray source and facilities. In May, the House of Representatives passed a bill to fund the initial $20 million increment of a six-year, potentially $400 million, SOR lithography R&D program. If passed by the Senate and the president, the DOD would be authorized to spend $20 million in fiscal 1988 to develop a compact SOR source and support technologies. Chief beneficiaries would be Brookhaven National Laboratories and the University of Wisconsin at Madison.

Table 8

SOR FACILITIES WORLDWIDE*

Year	Institution	Name	Energy (GeV)	Energy (KeV)
		Japan		
1975	Tokyo University	INS-SOR II	0.4	0.13
1982	MOE High-Energy Physics Lab	Photon Factory	2.5	4.00
1984	Molecular Research Lab	UV-SOR	0.7	0.22
1981	MITI Electrotechnical Lab	TERAS	0.66	0.32
		United States		
1968	University of Wisconsin	Tantalus-I	0.24	0.05
	University of Wisconsin	Aladdin	1.0	1.07
1974	Stanford University	SSRL	3.5	7.5
1976	National Bureau of Standards	SURF-II	0.28	0.06
1979	Cornell University	CHESS	5.5	11.37
1981	Brookhaven National Lab	NSLS-UV	0.75	0.94
1984	Brookhaven National Lab	NSLS-X	2.5	4.34
		West Germany		
1974	DESY	HASYLAB	5.0	22.9
1982	BESSY	BESSY	0.8	0.62
		Other European		
1980	Dulesberry (U.K.)	SRS	2.0	3.2
1973	University of Paris (France)	LURE-ACO	0.54	0.32
1976	University of Paris (France)	LURE-DCI	1.8	3.39
1978	Francaty National Lab (Italy)	ADONE	1.5	1.50
1980	Moscow University (U.S.S.R.)	PAKHRA	1.3	1.22
1977	Novobirsk Laboratory (U.S.S.R.)	VEPP-III	2.25	4.11

*As of December 1986.

Source: MOE High-Energy Physics Lab

Table 9

MAJOR SOR RESEARCH GROUPS IN THE UNITED STATES AND EUROPE

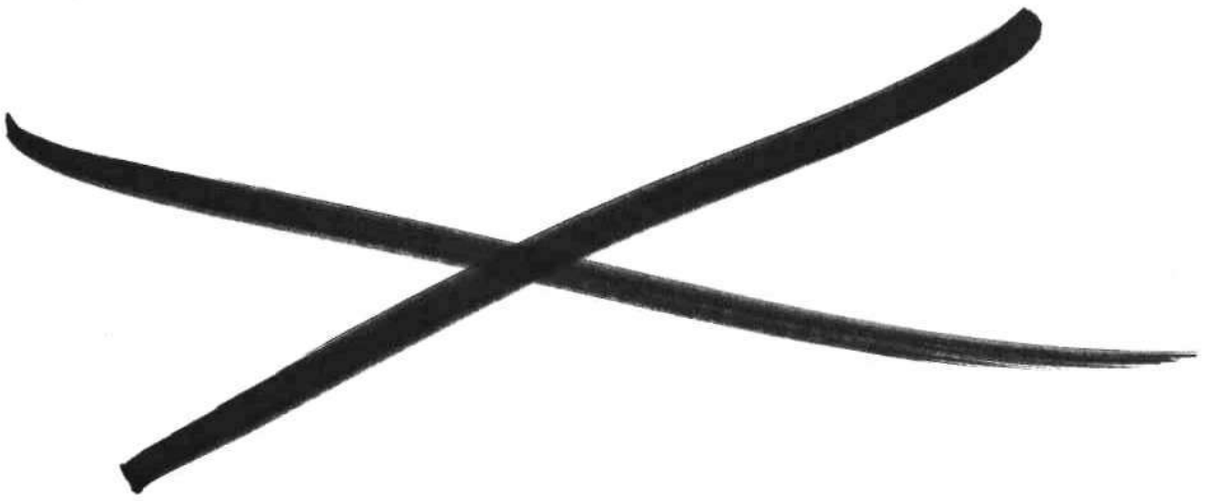
Institution	Location
AT&T Bell Laboratories	Murray Hill, NJ
Brookhaven National Laboratory	Upton, NY
Berlinger Elektrenspeicherring-Gesellshaft fur Synchrotronstrahlung m.b.h. (BESSY)	Berlin, W. Germany
Cobilt-GI-Bell	
Cornell University High Energy Synchrotron Source	Ithaca, NY
COSY Microtech GmbH	Berlin, W. Germany
Deutsche Elektronensynchrotron (DESY)	W. Germany
Electron Storage Ring Corporation (ESRC)	San Francisco, CA
European Center for Nuclear Research	Geneva, Switzerland
Eurosil	Etching, W. Germany
Exxon Research & Development Center	
Fraunhofer Institut fur Mikrostrukturtecknik	Berlin, W. Germany
Hamburger Synchrotron Sprahlungslabor (HASYLAB)	Hamburg, W. Germany
Harvard-Smithsonian Center for Astrophysics	Cambridge, MA
Hoechst AG	Frankfurt, W. Germany
Hewlett-Packard Corporation	Palo Alto, CA
Hughes Microelectronics Research Center	Malibu Beach, CA
IBM Thomas J. Watson Laboratory	Yorktown Heights, NY
Karl Suss KG-GmbH	Munich, W. Germany
Los Alamos National Laboratory	Los Alamos, NM
Oakridge National Laboratory	Oakridge, AL
Micronix Corporation	Los Gatos, CA
Perkin-Elmer Corporation	Norwalk, CT
PETRA	W. Germany
Stanford Synchrotron Radiation Laboratory	Stanford, CA
Sandia National Laboratory	Sandia, NM
Siemens	Berlin, W. Germany
Telefunken	Heilbronn, W. Germany
University of California/Lawrence Berkeley Lab	Berkeley, CA
University of Paris	Paris Sud, France
University of Wisconsin	Madison, WI
U.S. Naval Research Laboratory	
Valvo (Philips subsidiary)	Netherlands
Xerox Palo Alto Research Center	Palo Alto, CA

Source: Dataquest
August 1987

DATAQUEST CONCLUSIONS

The global race to develop SOR technology, especially compact SOR rings, for future megabit memory production is accelerating. Dataquest believes that the shift to X-ray lithography for R&D purposes by 1990 is inevitable because of the physical limits of photolithography. SOR technology offers high resolution and wafer throughput, making it suitable for mass production, but technical hurdles in the area of masks, resists, and stepper interface must be resolved before compact SOR rings can be widely commercialized. At ¥1 billion ($7.1 million), SOR rings are still expensive, but West German and Japanese companies are racing to develop smaller rings, which would also solve the problem of fab space. We observe that Japanese companies, which are actively developing SOR technology, will utilize compact SOR rings internally by the late 1980s and commercialize them by the early 1990s.

Joe Grenier
Kaz Hayashi
Sheridan Tatsuno



September Newsletters

The following is a list of newsletters found in this section:

- A Harvest Of Excess Capacity
  1987 - #21

Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987-1988 Newsletters: September 1987-21

A HARVEST OF EXCESS CAPACITY

The semiconductor industry is enjoying sunny weather for the first time in a few years. The book-to-bill ratio continues to sport a healthy tan and capital spending budgets are beginning to fatten up after a long and very lean winter. However, there is still evidence of the storms and turbulations of the recent past: Capacity utilization will continue to be lower than it has been in the past, and the installed base will grow at a slower rate than production.

WORLDWIDE CAPACITY AND CONSUMPTION

Dataquest measures capacity in square inches of silicon. Silicon is the raw material of the semiconductor industry, and it is an important measure of productivity. Figure 1 shows the 1973 through 1991 growth of both historical and forecast silicon capacity and actual silicon consumption.

Until 1980, silicon capacity and consumption grew at about the same rates. After 1980 and the rapid buildup of capacity in Japan, capacity grew faster than consumption, and until 1984, there was excess capacity. This excess capacity all but disappeared in the boom of 1984, and in many areas there were shortages of capacity.

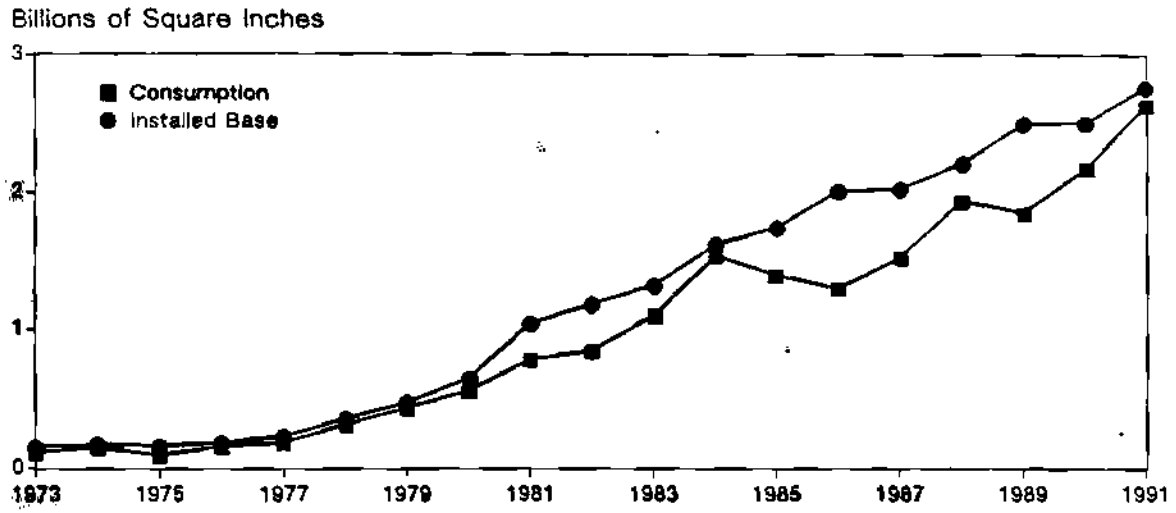
In 1985, two things happened: Silicon consumption actually fell, while capacity continued to grow. Capacity continued to grow because capital expansions have a momentum of their own; expansions that began in 1984 continued to come on-stream in 1985, even though the stream was dry. By 1986, however, semiconductor manufacturers were able to slow the growth of their installed base. The gap between capacity and consumption began to decrease.

We believe that the gap between capacity and consumption, though narrowing, will continue for the remainder of this decade. In 1991, however, capacity and consumption will be close together.

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 971-9000, Telex 171973

Figure 1

WORLDWIDE SEMICONDUCTOR MANUFACTURING CAPACITY



Source: Dataquest
September 1987

INSTALLED BASE AND PRODUCTION

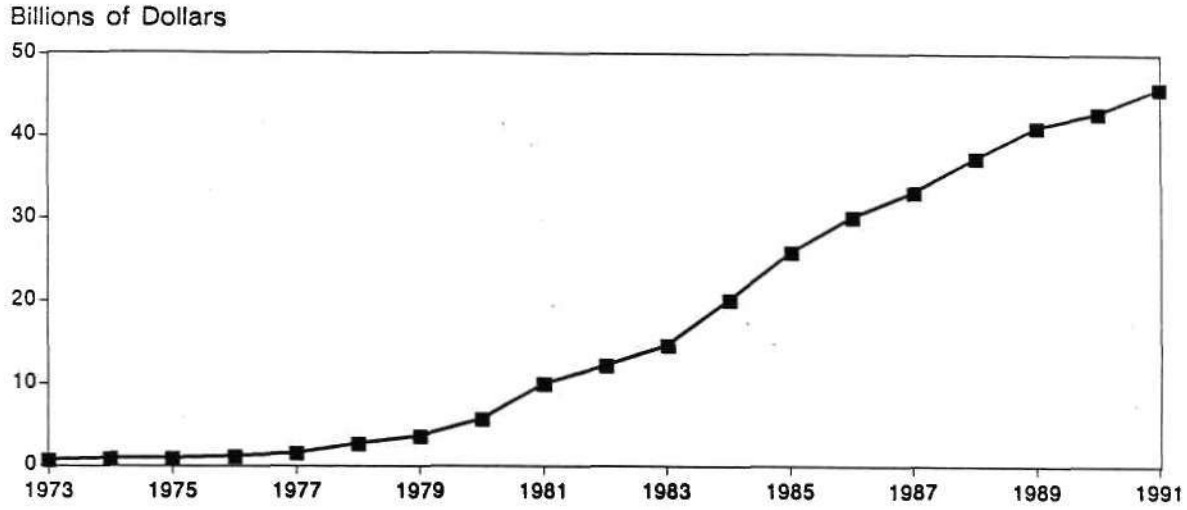
Capacity depends on the industry's installed base of property, plant, and equipment (PPE). As shown in Figure 2 the installed base of PPE has grown steadily since 1973. The installed base is an accumulation of several previous years' investment; it has a tendency to keep growing, regardless of where the industry is in the business cycle.

Figure 3 charts the change in installed base versus changes in semiconductor production. Until the recession of 1985, the installed base tended to grow faster than semiconductor production. In 1986, production and PPE grew almost equally. We expect, however, that in 1987, production will grow more than the installed base of PPE. We expect production to outpace the growth of PPE for most of the remainder of the decade.

Semiconductor manufacturers still remember the capital spending boom of 1984 and the consequent over-capacity of 1985. Though their spending plans have strengthened of late, they are still cautious about overexpansion. Spending to improve productivity will occur before significant capacity expansions.

Figure 2

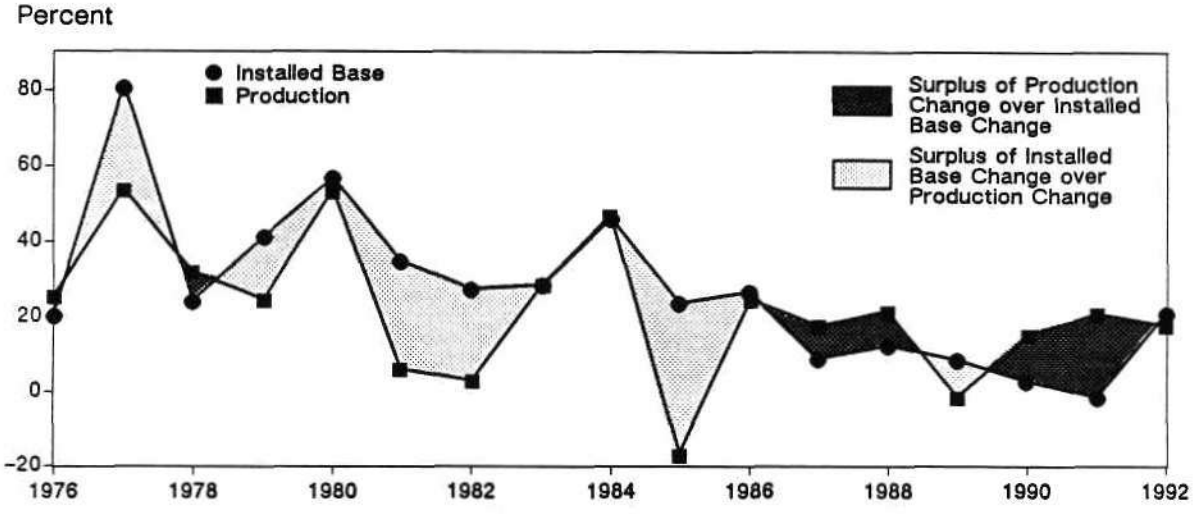
WORLDWIDE SEMICONDUCTOR MANUFACTURING
(PPE Installed Base)



Source: Dataquest
September 1987

Figure 3

WORLDWIDE CHANGE IN SEMICONDUCTOR BASE
VERSUS CHANGE IN SEMICONDUCTOR PRODUCTION



Source: Dataquest
September 1987

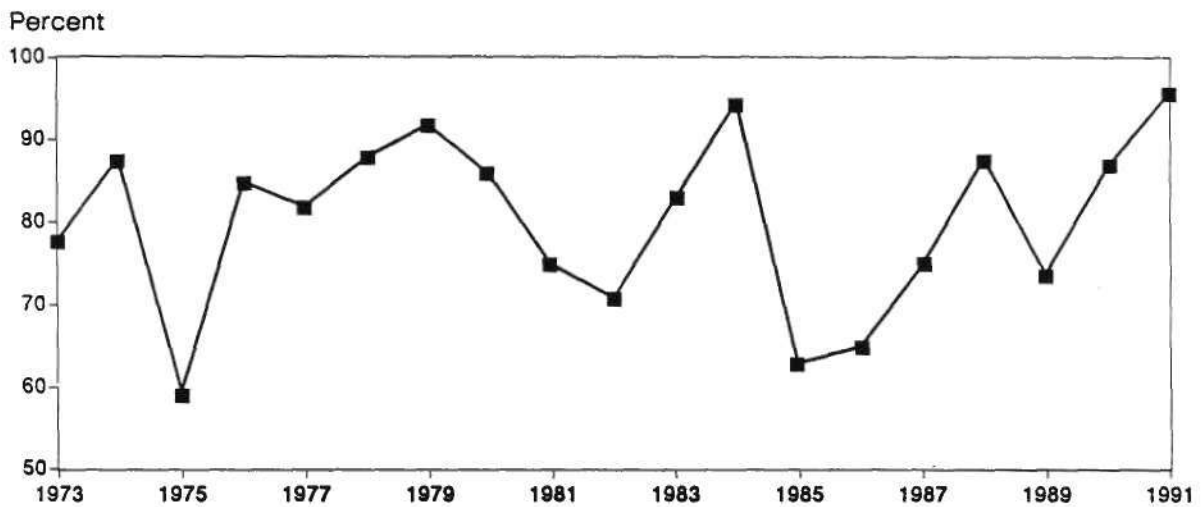
WHAT GOES UP, GOES DOWN, BUT NOT AS FAR

Figure 4 shows Dataquest's estimates of capacity utilization for 1973 through 1991. Capacity utilization peaks when the industry is at the height of its expansion, then it descends to a recession. In 1984, capacity utilization was at an all-time high; in 1985, it was at an all-time low. As manufacturers expand their installed base at rates lower than production expansion, the excess capacity of 1985 will be worked off slowly. Capacity utilization will rise to a peak in 1988, then it will fall, but not nearly as far as in the previous downturn.

We expect excess capacity to dry up quickly after 1989. The large amounts of PPE brought on-stream in 1983 through 1985 will begin to be obsolete, and new equipment will be needed for new generations of devices. By 1991, capacity utilization could be as high as it was in 1984.

Figure 4

WORLDWIDE CAPACITY UTILIZATION



Source: Dataquest
September 1987

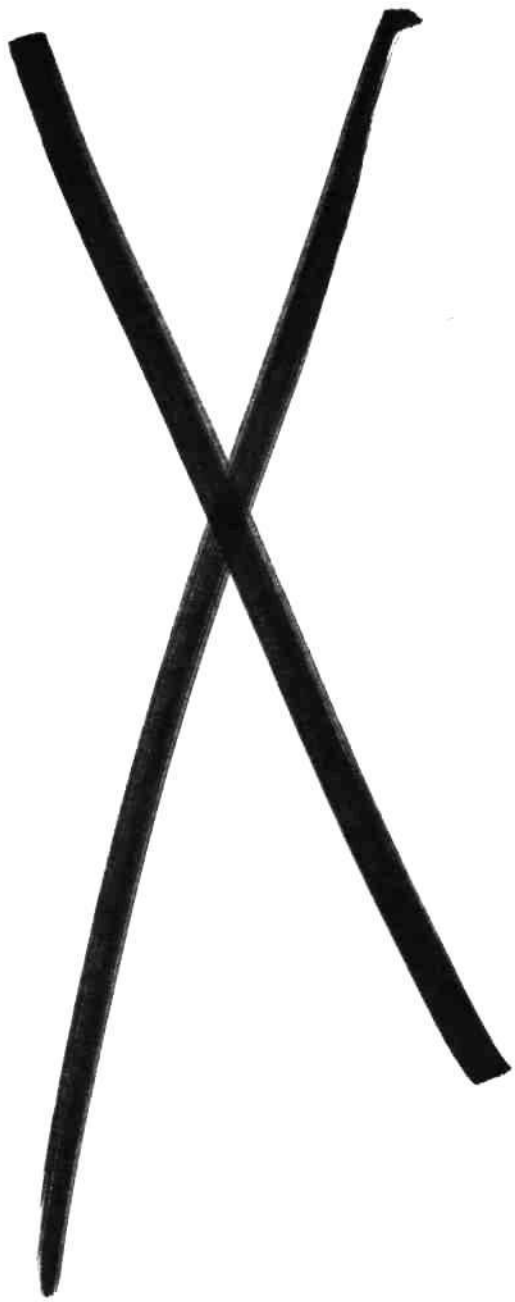
CAN WE HAVE TOO MUCH OF MODERATION?

Our forecast of capacity utilization assumes that manufacturers have learned to be cautious from the recession of 1985. We believe that the installed base will expand at a rate that is generally lower than the expansion of production. This will have the effect of slowly drying up the excess capacity brought on in the boom of 1985.

There's an old military adage to the effect that generals are always planning better ways to fight the last war, not the one coming up. Is the same thing true for semiconductor manufacturers? Can they be spending all their time trying to prevent the downturn of 1984, rather than the downturn of 1989 or the early 1990s?

A look at capacity utilization in 1991 suggests that this might be so. It is at a rate equal to 1984. As Figure 3 shows, the path to this high peak of utilization will be different than before. The late 1980s will see the installed base expand at a lesser rate than production. At the end of the decade, manufacturers will have to be careful that they do not unduly limit the growth of PPE. High peaks of utilization bring on surges of capacity spending, overcapacity, and sharp descents into recession.

George Burns



October Newsletters

The following is a list of newsletters found in this section:

- The Next Five Years: Sustained Capital Spending Growth
  1987 - #23

- Dataquest's 1987 Semiconductor Conference- One To Remember
  1987 - #22

Dataquest
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Research Newsletter

SEMS Code: 1987–1988 Newsletters: October 1987–23

THE NEXT FIVE YEARS: SUSTAINED CAPITAL SPENDING GROWTH

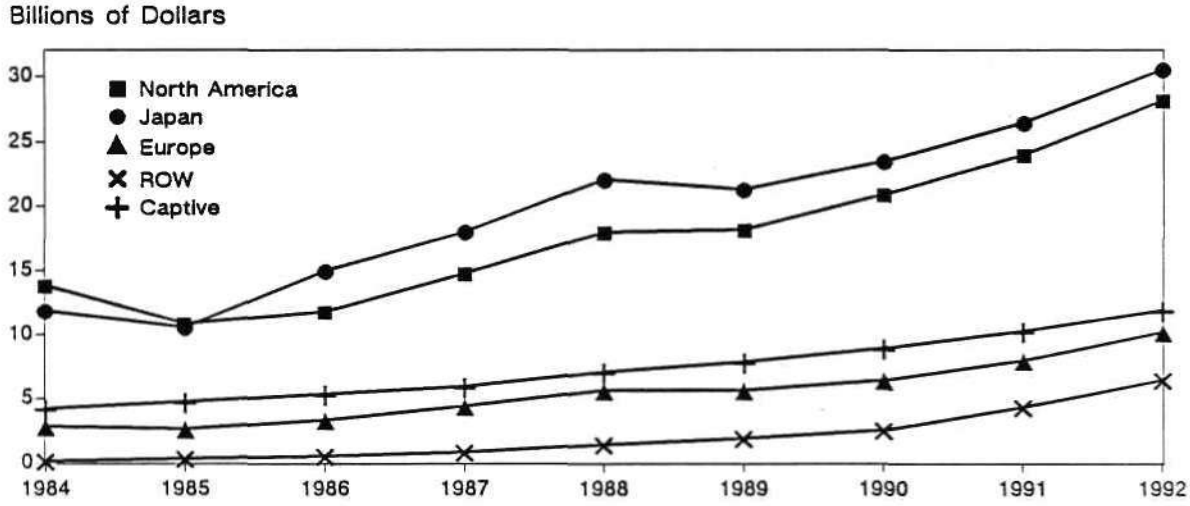
INTRODUCTION

Capital spending in 1987 will show an increase of 9.9 percent, from $5.4 billion to $5.9 billion (slightly higher than our previous estimate of $5.7 billion). Japan will probably show a slight decrease in capital spending; the other regions of the world, including captives, will show an increase. We expect a year of strong capital spending growth in 1988, which will be followed by a slight downturn in 1989.

In spite of the growth in 1987 and 1988, spending will not reach 1984's level until 1990. We expect 1990 through 1992 to be very healthy years (see Figure 1). In sum, if 1989 does not turn into a deep general economic recession, we expect the next five years to be years of long-awaited growth for the capital equipment industry.

Figure 1

Regional Capital Spending (Billions of Dollars)



Source: Dataquest October 1987

One of the major growth areas for capital spending is the Rest of World (ROW) region, which includes the Asian–Pacific Rim countries. We expect that, because of their commitment to capital spending, their share of the total worldwide device fabrication base will increase to 10 percent by 1992. ROW's acquisition of a significant share of the world's semiconductor manufacturing resources will lead to a large gain in market share for ROW companies.

As this newsletter went to press, the stock market crash of 1989 occurred. It is possible that this crash is anticipating 1989's mild downturn; it is also possible that the severity of the downturn is heralding a steeper and deeper downturn than we had expected. It is too soon to tell. We are analyzing the situation and will shortly publish an update of our forecast.

PRODUCTION AND THE ECONOMY

The anticipation of salable production is the engine that drives capital spending. In 1988, both semiconductor manufacturers and semiconductor equipment manufacturers will be faced with decisions about capacity expansion. These decisions will depend in large part on the general economic outlook for 1989 and 1990. Dataquest, through its relationship with Dun & Bradstreet, will be monitoring these economic developments closely.

We expect that consumption and production of semiconductors will grow at a compound annual growth rate (CAGR) of 16 percent from 1986 to 1992 (see Table 1). This growth will be interrupted by a slight pause in 1989, when the growth of semiconductor consumption and production will be essentially flat because of general economic conditions.

Most economists expect that the current period of economic growth, which is already the longest peacetime expansion on record, will run out of gas after 1988. In 1988, the manufacturing sector is expected to continue its expansion because previous drops in the value of the dollar are favorable to expansion of manufacturing exports.

By 1989, this momentum from expanding international trade will be exhausted; Graham–Rudman cuts that will have to be made after the election will probably be in the neighborhood of $60 billion. This, along with slightly higher inflation and interest rates, will probably bring about a recession. Dun & Bradstreet expects that the recession will be mild, however.

Table 1

Regional Production
(Millions of Dollars)

	1984	1985	1986	1987	1988
North America	$13,925	$10,964	$11,857	$14,870	$18,057
Japan	11,952	10,689	15,031	18,069	22,147
Europe	2,972	2,759	3,498	4,519	5,729
ROW	238	411	623	961	1,592
Captive	4,377	4,875	5,422	6,088	7,199
	$33,464	$29,698	$36,431	$44,508	$54,723
Percent Change	44%	(11%)	23%	23%	23%

	1989	1990	1991	1992	CAGR 1986-1992
North America	$18,222	$20,926	$24,053	$28,292	16%
Japan	21,343	23,582	26,583	30,688	13%
Europe	5,727	6,591	8,079	10,232	20%
ROW	2,047	2,692	4,413	6,566	48%
Captive	7,992	9,074	10,361	11,999	14%
	$55,332	$62,865	$73,488	$87,778	16%
Percent Change	1%	14%	17%	19%	

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
October 1987

CAPITAL SPENDING: 1987

Because we expect only a mild recession in 1989, we are forecasting flat semiconductor production and capital spending in 1989. If, however, the expected recession is more severe than expected, then capital spending could fall 10 to 20 percent in 1989.

From reports in Japan, we believe that capital spending hit bottom in the first or second quarter of this year and is now on the rise. However, for the entire calendar year, spending will be down 4 percent in dollars and 12 percent in yen; this will make three years in a row of spending decline in Japan. We expect Japanese capital spending for the calendar year to be $1.7 billion (see Table 2).

While we expect an overall decline of 4 percent in Japan, some companies will actually increase their spending in 1987. Fuji Electric, Fujitsu, Hitachi, NEC, Oki, Rohm, Sanyo, Seiko Epson, Sony, and Toshiba are all expected to show increases (see Table 3).

Table 2

Regional Capital Spending
(Millions of Dollars)

	1984	1985	1986	1987	1988
North America	$3,051	$2,291	$1,640	$1,908	$2,650
Japan	3,671	3,219	1,760	1,682	2,119
Europe	630	600	670	823	1,037
ROW	201	220	275	406	606
Captive	965	1,045	1,043	1,104	1,309
	$8,517	$7,375	$5,389	$5,924	$7,722
Percent Change	106%	(13%)	(27%)	10%	30%

	1989	1990	1991	1992	CAGR 1986-1992
North America	$2,498	$2,918	$ 3,482	$ 4,326	18%
Japan	2,437	3,655	5,118	6,912	26%
Europe	1,063	1,220	1,468	1,829	18%
ROW	648	810	969	1,135	27%
Captive	1,244	1,294	1,527	1,920	11%
	$7,889	$9,897	$12,564	$16,122	20%
Percent Change	2%	25%	27%	28%	

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
October 1987

Table 3

Japanese Company Capital Spending
(Millions of Dollars)

Company	CY 1986	CY 1987	Percent Change
Fuji Electric	$ 30	$ 32	8%
Fujitsu	96	130	36%
Hitachi	132	162	23%
Japan Semiconductor	30	0	(100%)
Matsushita	150	117	(22%)
Mitsubishi	120	65	(46%)
NEC	180	195	8%
NJRC	30	19	(35%)
NMB	0	19	-
Oki	60	97	63%
Rohm	48	65	36%
Sanken Electric	24	19	(19%)
Sanyo	108	130	20%
Sharp	132	65	(51%)
Shindengen	18	6	(64%)
Seiko Epson	30	32	8%
Sony	96	104	8%
Toshiba	389	325	(17%)
Others	90	97	8%
	$1,760	$1,682	(4%)

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
October 1987

Spending in North America will show an increase of 16 percent in 1987 to $1.9 billion. This increase is fairly broadly based, with only four companies showing a decline (see Table 4). AMD will increase its spending over 1986 spending by more than 100 percent, following by Intel, with a 94 percent increase.

Spending in Europe will increase a robust 23 percent in 1987. This increase will be led by some non-European companies expanding facilities or ramping up new production. Examples of such activity include Analog Devices in Limerick, Ireland; Motorola in East Kilbride, Scotland; and NEC in Livingston, Scotland.

Table 4

North American Company Capital Spending
(Millions of Dollars)

Company	CY 1986	CY 1987	Percent Change
AMD	$ 55	$ 111	101%
Analog Devices	37	49	33%
Fairchild	135	68	(50%)
General Instrument	8	12	50%
General Electric	50	50	0
Harris	45	29	(36%)
IDT	18	18	0
Intel	155	300	94%
Micron Technology	11	14	22%
Motorola	250	338	35%
National Semiconductor	88	104	18%
NEC	10	12	20%
Philips-Signetics	60	90	50%
Siemens	20	15	(25%)
Texas Instruments	213	240	13%
Thomson-Mostek	9	8	(11%)
Others	476	451	(5%)
	$1,640	$1,908	16%

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
October 1987

Spending in ROW will increase by 48 percent in 1987. Hyundai and Lucky Goldstar in South Korea reportedly will increase their spending in 1987 by 50 percent, and UMC will be beginning production in an $80 million fab in Taiwan by the end of 1988.

Spending by captives will also probably increase in 1987. This spending involves significant upgrades at IBM's facilities in East Fishkill, New York; Essex Junction, Vermont; and Sindlefingen, West Germany; and AT&T's new facility in Spain, near Madrid.

BEYOND 1987: THE FORECAST

We expect worldwide capital spending to increase by 30 percent in 1988 to $7.7 billion. This increase will be led by the continuing increase in semiconductor demand through 1988. However, because of the severe overcapacity brought on by the 1984 to 1985 capital spending boom, 1988's spending level will still be only 91 percent of 1984's level. This is in spite of the fact that 1988's production will be 163 percent of 1984's.

We expect the demand for semiconductors to soften in 1989, and correspondingly, we expect capital spending to be approximately flat, with only 2 percent growth. North American merchants and captives will probably lower their spending in 1989. ROW and Europe will see only modest growth in 1989 as they too moderate their spending because of softening demand.

Japan, however, will probably increase its spending by 15 percent in 1989. Japan will be doing this to make up for its very low capital budgets of 1986 and 1987. However, even with a relatively strong 15 percent increase in 1989, Japan's spending level will still be slightly below North America's.

European capital spending will reach $1.8 billion by 1992 and will grow at a CAGR of 18 percent between 1986 and 1992.

ROW capital spending will grow at a CAGR of 27 percent between 1986 and 1992. We expect that by 1992, ROW's capital spending will be more than $1 billion. As a result of ROW's strong commitment to capital spending, we expect that ROW will have 10 percent of the worldwide merchant installed base by 1992. This will translate into a strong gain in market share for ROW semiconductor manufacturers. Today, ROW companies have approximately 2 percent market share. We expect that this share will grow to 8 percent in 1992.

Capital spending by captive manufacturers such as AT&T and IBM will experience slower growth than any of the major merchant geographical segments. We expect captive capital spending to grow at an 11 percent rate for the period 1986 to 1992. Captive capital spending will be almost $2 billion by 1992.

Merchant capital spending in North America will grow at a CAGR of 18 percent from 1986 to 1992. Capital spending in North America will be $4.3 billion by 1992.

Japanese capital spending fell below that of North America in 1987. We expect that Japanese capital spending will overtake North America's level of spending in 1990 and then continue to grow. In fact, because of the strong levels of spending from 1989 on, we expect that Japan will have a CAGR of 26 percent for 1986 through 1992.

The reasons for this burst of spending in Japan after 1989 were discussed in some detail in SEMS newsletter number 1987–14, "Capital Spending Forecast: Slower but Steadier Growth." In general, Japanese spending will accelerate at the end of the decade because of the need to replace a significant portion of its installed base, and also because of its need for new equipment for the next generation of devices.

DATAQUEST CONCLUSION

Although spending levels will not reach 1984's levels until 1990, the recovery of capital spending is under way. Moreover, unless there is a severe general economic recession in 1989, this recovery should be a sustained recovery. There will be growth in 1987, 1988, 1990, 1991, and 1992.

Economic analysis by Dun & Bradstreet indicates that the recession in 1989 will be a mild one. Because we expect only a mild recession in 1989 and because end-use markets will remain healthy (as forecast by the Semiconductor Industry Group's Semiconductor Application Markets Service), we are forecasting that production and capital spending will not decline. However, if conditions change and the recession is harsher than expected, then capital spending could fall 10 to 20 percent in 1989.

Not only will the growth in capital spending be sustained, but it will be dispersed geographically. Growth will be strongest in the Asia-Pacific Rim countries and will exceed $1 billion in 1992. Spending in North America will exceed spending in Japan until 1990. Japanese spending will be very strong after 1989, expanding at a CAGR of 38 percent from 1990 to 1992. In 1992, the semiconductor equipment industry will have long since surpassed the heights of 1984 and will again be standing at a new high point.

George Burns

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Research *Bulletin*

SEMS Code: 1987–1988 Newsletters: October 1987–22

DATAQUEST'S 1987 SEMICONDUCTOR CONFERENCE—ONE TO REMEMBER

This is it. The conference of conferences is rapidly approaching, and from all indications, it will be exciting and thought provoking.

From its lowly beginning 40 years ago, the $42.5 billion chip industry now supports a world electronics industry of $470 billion. The industry has not only reached this lofty revenue level, but it has also become the economic battleground of the industrialized nations, including the United States, Japan, West Germany, and many others. This is a dubious distinction. It has been called the "crude oil of the '80s" by Jerry Sanders, the "rice of industry" by Governor Hiramatsu of Japan's Oita Prefecture (formerly the head of MITI's Electronics Policy Bureau), and the "brains of Star Wars" by U.S. Secretary of Defense Casper Weinberger.

Over its 40-year history, the industry has gone through many significant evolutionary changes, one of which Mel Thomsen, director of Dataquest's Semiconductor Industry Service, will address in his remarks. Mr. Thomsen will note that the industry has reached a very high level of consolidation, and analysis of his chart, shown in Figure 1, suggests that 20 percent of the companies now represent 80 percent of the industry. Robert McGeary, director of the Semiconductor Equipment and Materials Service, will discuss how this fact relates to regional device fabrication.

A standard feature of all our conferences is a presentation of our outlook for the coming year. This forecast is the combined effort of our entire research staff.

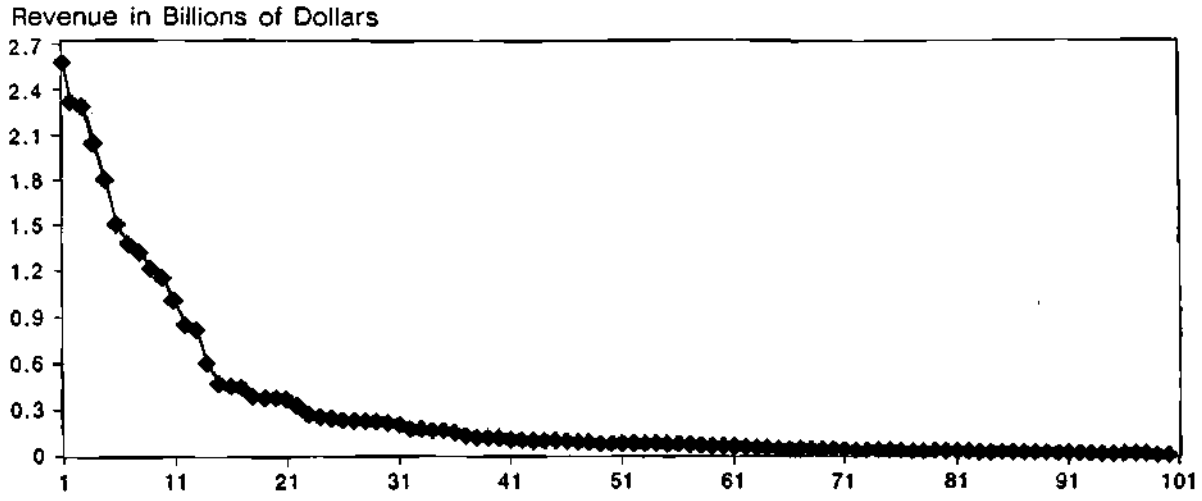
As is true each quarter, we produce an eight-quarter rolling forecast by product and by region of the world, compiled through the aid of our integrated data base. This quarter we are predicting that the 1988 industry will stack up as indicated in Table 1.

The third quarter is almost a wrap, and by the time you read this, it will be. Currently we see bookings in the regional markets rising more slowly than billings, but still growing at a healthy level. We anticipate that October orders will be stronger and that orders will continue to rise sequentially from quarter to quarter for the next three quarters. Gene Norrett, director of the Semiconductor Industry Group, will examine market forces and elaborate on the trends in his address at the conference.

Dataquest, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 971-9000, Telex 171973

Figure 1

1986 Worldwide Semiconductor Revenue



Source: Dataquest
October 1987

Table 1

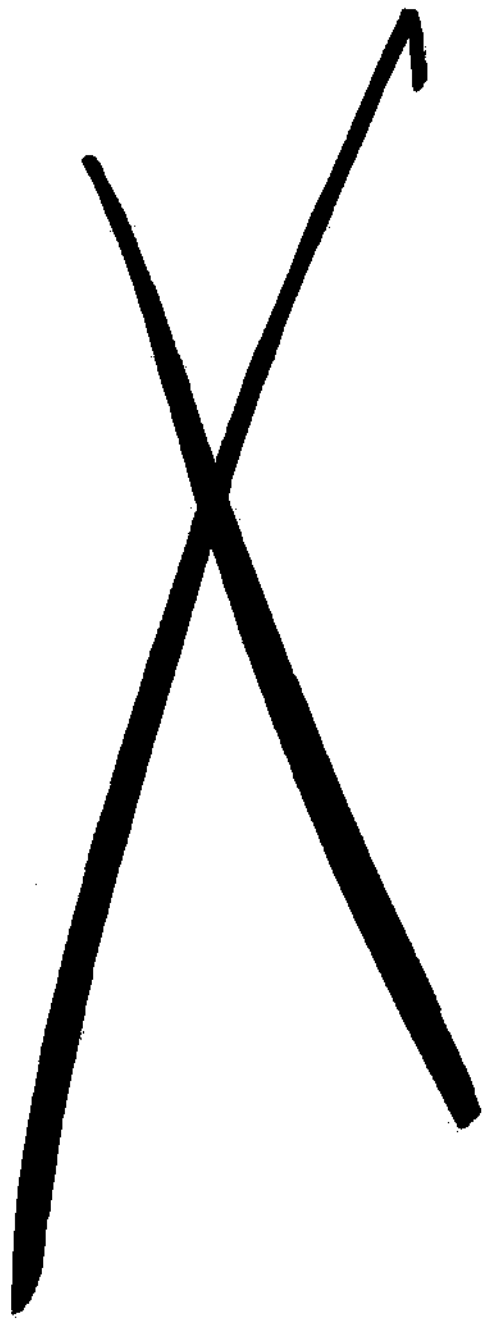
Estimated Worldwide Semiconductor Consumption—1988 (Preliminary) (Percent Change in U.S. Dollars)

	Quarter				
	1	2	3	4	Year
North America	5.2%	9.9%	3.0%	2.1%	24.2%
Japan	2.3%	6.6%	7.2%	4.8%	18.3%
Europe	5.1%	5.9%	3.1%	5.1%	19.0%
ROW	11.6%	13.0%	10.5%	4.8%	44.9%
Total	5.0%	8.4%	5.6%	4.0%	23.7%

Source: Dataquest
October 1987

Please expedite your registration—we are sure you do not want to miss hearing the important speakers we have lined up for this conference.

Robert McGeary
Gene Norrett



November Newsletters

The following is a list of newsletters found in this section:

- The Semiconductor Industry Faces Midlife Crisis
  1987 - #25

- Contamination Control in Semiconductor Processing
  1987 - #24

Dataquest
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Research Newsletter

SEMS Code: 1987–1988 Newsletters: November 1987–25

THE SEMICONDUCTOR INDUSTRY FACES MIDLIFE CRISIS

SUMMARY: DATAQUEST HOSTS AN INDUSTRY BIRTHDAY PARTY

The semiconductor industry has attained middle age, and Dataquest is throwing a birthday party. On October 19–21, the Semiconductor Industry Group proudly hosts its annual Semiconductor Conference at The Pointe at Squaw Peak in Phoenix, Arizona.

As might be expected, the mood surrounding the conference is one of celebration. The worldwide semiconductor industry has now clearly begun its recovery from two years of recession. Dataquest believes that the dollar value of world semiconductor consumption in 1987 will grow nearly 24 percent over 1986, to a total of more than $38 billion. We expect this growth to continue in 1988, with semiconductor consumption increasing by another 24 percent to $47.5 billion.

Why Midlife Crisis?

While attaining middle age certainly entitles one to reflect on the past, it is a rite of passage that demands facing the future as well. With industries as with individuals, confronting the remainder of one's life from the perspective of full adulthood can be at once profound and intimidating. For this reason, the Dataquest Semiconductor Industry Group has chosen the theme of "midlife crisis" for its upcoming conference.

What has the semiconductor industry learned from the past four decades? How have the structure and identity of the industry changed? How will these changes affect the future of the semiconductor business? This newsletter identifies some of the major transformations facing the semiconductor industry as it looks toward the next 40 years, and in doing so offers some insight into the Dataquest Semiconductor Conference agenda.

THE PAST AS PROLOGUE

Forty years ago, three Bell Laboratories scientists invented the point contact transistor, and the semiconductor industry was born. Eight years later, Texas Instruments began to manufacture silicon transistors on a commercial scale, ushering in

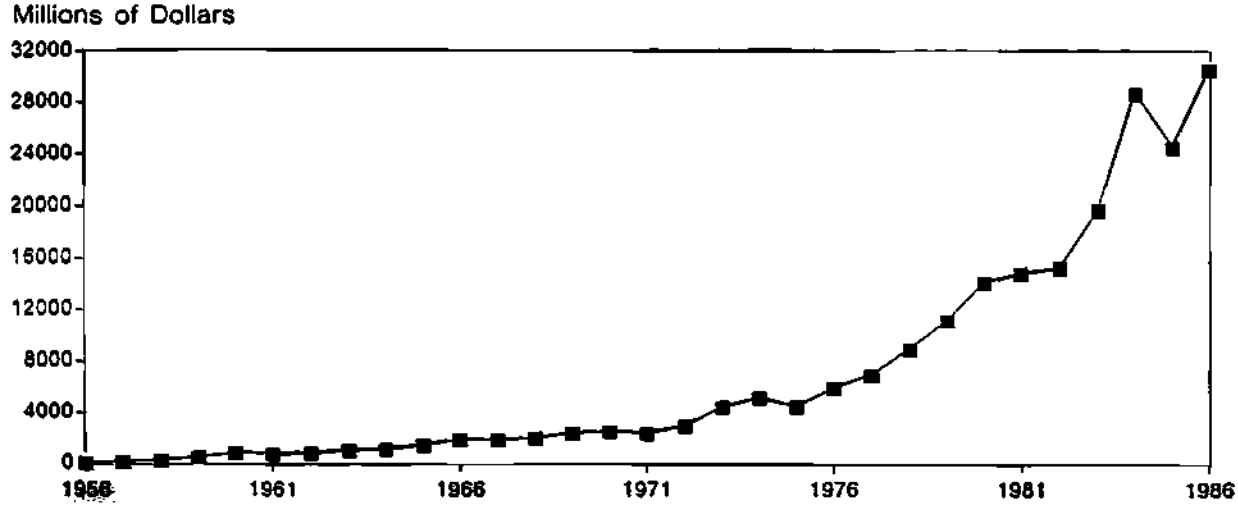
Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 437-8000, Telex 171973, Fax (408) 437-0292

a new era in electronics. In 1958, less than three decades ago, a Texas Instruments scientist named Jack Kilby and a Fairchild scientist named Bob Noyce independently developed the integrated circuit. At that time, worldwide semiconductor sales totaled $352 million.

The growth of the semiconductor industry, as illustrated by Figure 1, has been nothing less than phenomenal. While this growth has slowed over the years, Dataquest believes that the world's demand for semiconductors will continue to expand at a compound annual growth rate of 14 to 16 percent into the 1990s. If the worldwide semiconductor market were to continue to grow at its historical exponential rate for the next 40 years, semiconductor consumption in the year 2027 would reach $22.6 trillion! Such an extrapolation obviously overstates the potential market. Considering that semiconductor consumption by the electronic equipment industry currently accounts for approximately 5 percent of its total sales, a $22.6 trillion semiconductor market would require a $452 trillion electronic equipment industry to support it!

Figure 1

Historical Worldwide Semiconductor Consumption



Source: Dataquest
November 1987

GROWTH: IS THERE LIFE AFTER THE PERSONAL COMPUTER?

Going through a midlife crisis often elicits the question, "Have I lived through the best years of my life?" During the past two years, Dataquest has heard a number of variations on this theme from semiconductor industry leaders. Clearly, growth in many semiconductor end markets is slowing down (Table 1). Nevertheless, the outlook for semiconductor consumption in major electronic equipment segments remains positive (Table 2).

Table 1

Estimated Compound Annual Growth Rates for Selected North American Electronic Equipment Segments (Based on Total End-User Revenue)

Segment	CAGR 1982-1986	CAGR 1987-1991
Single-User Enhanced Computers	156.1%	30.0%
Personal Computers	42.8%	8.7%
Electronic Typewriters	49.4%	(7.0%)
Rigid Disk Drives	20.3%	3.6%
Computer Storage	15.9%	4.8%
CAD/CAM Workstations	38.7%	7.6%
Telecom Equipment	14.0%	8.2%

Source: Dataquest
November 1987

Table 2

Estimated North American Semiconductor Consumption by Application Market (Millions of Dollars)

	1984	1985	1986	1987	1990	CAGR 1985-1990
Total Semiconductor	$13,139.0	$9,607.0	$10,201.0	$11,743.0	$15,998.0	10.7%
Data Processing	6,031.0	3,715.0	3,948.0	4,553.0	6,326.0	11.2%
Communications	2,057.0	1,357.0	1,505.0	1,731.0	2,491.0	12.9%
Industrial	2,107.0	1,561.0	1,608.0	1,890.0	2,555.0	10.4%
Consumer	970.0	698.0	732.0	830.0	1,138.0	10.3%
Military	1,276.0	1,488.0	1,560.0	1,777.0	2,176.0	7.9%
Transportation	698.0	788.0	848.0	962.0	1,312.0	10.7%

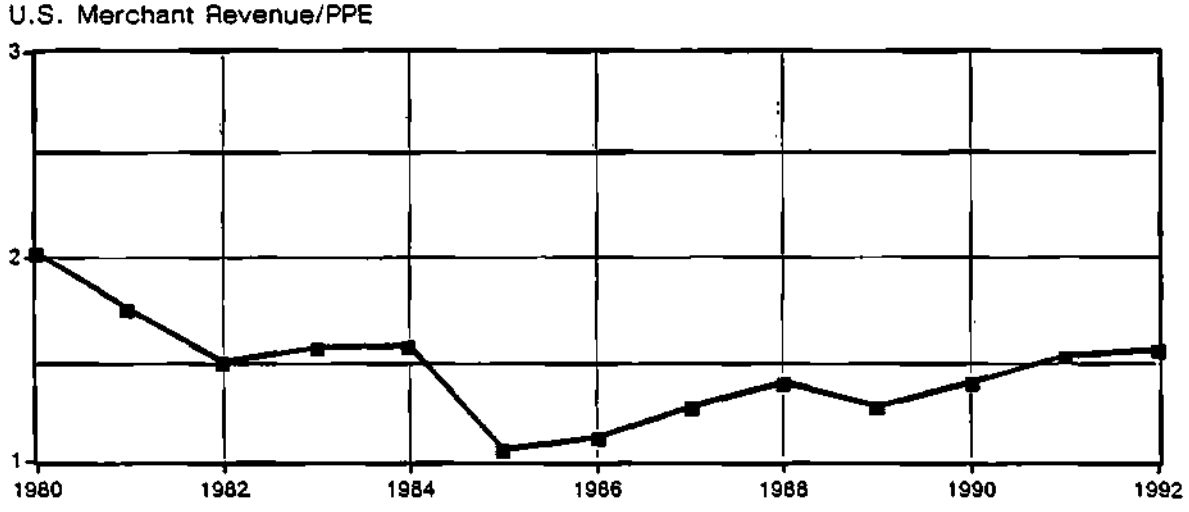
Source: Dataquest
November 1987

The Mixed Blessings of Commodities

As the industry continues to mature, it will continue to play the role of both creator and supplier to new end markets. But will these new markets offer the growth potential of the hand-held calculator and personal computer? If the industry has learned from its turbulent adolescence, it must seek out high-growth markets while avoiding the boom/bust pattern of its past. The blessings of commodities markets, as illustrated in Figure 2, have been mixed to say the least.

Figure 2

Estimated Revenue/Property, Plant, and Equipment Ratio
Worldwide Installed Base



Source: Dataquest
November 1987

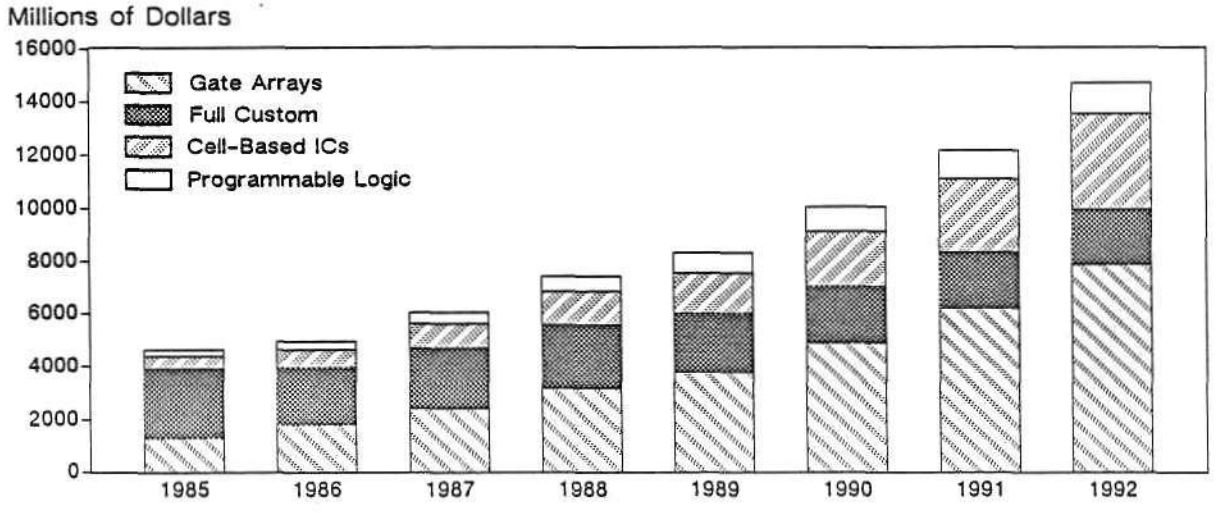
During the last decade, semiconductor manufacturers have invested heavily in capital equipment to shrink line geometries and increase capacity, while the price per function of semiconductor products has decreased at a rate unprecedented in any industry. Aggravated still further by overcapacity in the face of the most recent electronics industry slump, the industry's return on its investments has been the stuff of a venture capitalist's nightmare. As the industry faces the next 40 years, semiconductor manufacturers must reflect on their profligate youth and find new ways of adding value to their products and black ink to their bottom lines.

FROM JELLY BEANS TO VADs: HOW THE INDUSTRY ADDS VALUE

Experiencing a midlife crisis often brings about a changed perception of who one is and the values one holds. The forecast growth in consumption of ASIC devices (Figure 3) reflects a fundamental shift in the way semiconductor manufacturers and end users perceive the adding of value by the chip industry.

Figure 3

Estimated Worldwide ASIC Consumption



Source: Dataquest
November 1987

The Third Wave

The ASIC business is creating a new duality within the semiconductor industry—the distinction between adding value through the low-cost manufacturing of "jelly bean" commodity products and adding value through addressing applications' needs through semicustom design. The industry's increasing applications focus, combined with production overcapacity, CAD tool advances, and venture capital, has created a "third wave" of semiconductor start-up activity—the emergence of "value-added designers" (VADs).

Out of the 127 start-ups that Dataquest has observed between 1977 and 1986, 42 are ASIC companies—half of which offer cell-based design capability. There are another 25 start-ups in the microcomponents area, the majority of which are devoted to applications such as communications, keyboard display, mass storage, and other special functions. In the growing market for digital signal processing (DSP), 9 companies have come into existence, with many more expected. In all, nearly 60 percent of the latest crop of start-up companies are now competing in an environment that stresses value-added design.

CONSOLIDATION AND RESTRUCTURING

The semiconductor industry's changing perception of how value is added has been a contributing factor to the dramatic restructuring of many major U.S. suppliers during the past year. The following are some notable examples of this restructuring:

- In 1986, 75 percent of Fairchild's semiconductor revenue came from standard logic products. Prior to its acquisition by National Semiconductor, Fairchild's corporate strategy envisioned 75 percent of 1995 revenue coming from customer-specific and application-specific products.

- As a result of its acquisition of Monolithic Memories Inc., Advanced Micro Devices' (AMD) largest semiconductor revenue segment is now in the ASIC category.

- Intel and Texas Instruments (TI) joined forces a few months ago to jointly pursue the building of cell libraries around successful standard products. In its annual report, TI stressed the importance of applying systems expertise to silicon in achieving its corporate goals.

MANAGING CAPACITY: THE IMPORTANCE OF DOING MORE WITH LESS

Decreasing line geometries, the benefits of economies of scale, and cost-effective production will continue to be key issues in the semiconductor industry. In addition to these issues, however, the growing applications focus of the industry and the necessity to improve profitability will drive changes in the industry's view of manufacturing.

During a recent analysts' meeting, National Semiconductor's president and CEO, Charlie Sporck, stated that during the current recovery, his company would buy capacity from its competitors rather than invest solely in its own.

The hesitancy to dedicate brick and mortar to less proprietary areas is also evident in Intel's recent decisions to to satisfy rising demand in its memory markets through foreign sources. So far this year, Intel has entered into a DRAM agreement with Samsung and an EPROM agreement with Mitsubishi, while building its own capacity to meet the demand for 80286 and 80386 microprocessors.

The $600 Million Dollar Fab

The strategic use of capacity in 1987 is just the tip of the iceberg of manufacturing issues. Based on trends that we have observed recently, the revenue that a future state-of-the-art wafer fab will be able to generate will represent a significant barrier to market entry by the year 2000. In order to justify building a fab in 1980, a strategic planner had to find $35 million dollars worth of business. By the year 2000, this number will rise to approximately half a billion dollars!

Table 3, below, makes some rather conservative assumptions: an optimum fab operating level of 14,000 wafers per four-week period and a CAGR in revenue per square inch of 1 percent between 1985 and 2000. It is also assumed that the industry will be using 10-inch wafers by 1995 and 12-inch wafers by the year 2000.

Table 3

Estimated Revenue per Wafer Fab
(Millions of Dollars)

	1980	1985	1990	1995	2000
Wafer Size	100mm	150mm	200mm	250mm	300mm
Revenue/In.^{2}*	$15.50	$ 19.91	$ 20.93	$ 21.99	$ 23.11
Revenue/Fab	$35.00	$102.00	$191.00	$314.00	$476.00

*Assumes CAGR of 1 percent from 1985 to 2000.

Source: Dataquest
November 1987

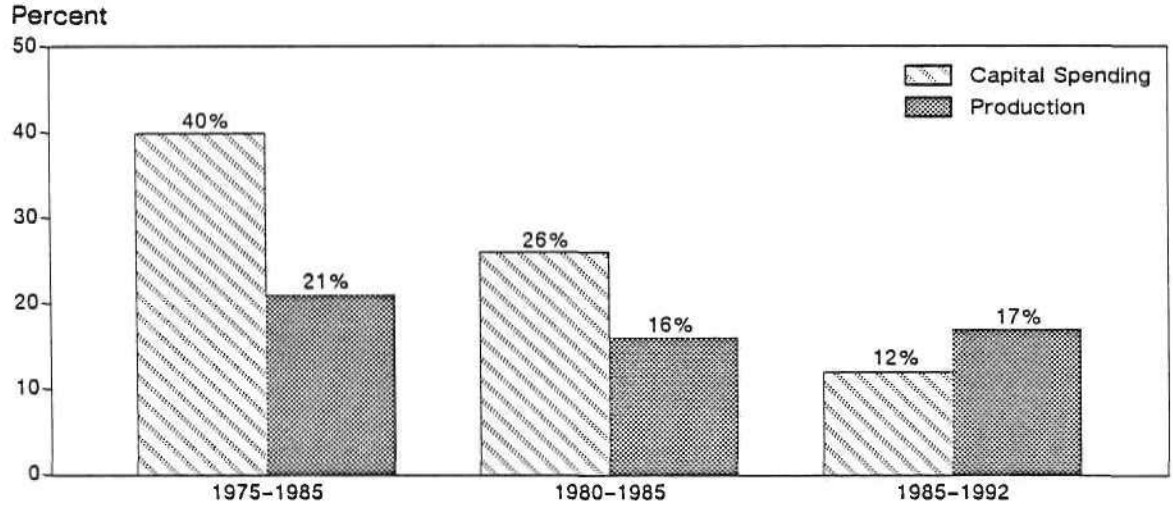
If one takes a slightly more aggressive forecasting posture and assumes an operating rate of 20,000 12-inch wafers per four-week period, the revenue potential of a single fab rises to more than $670 million—a level of revenue higher than AMD's total semiconductor sales in 1985. Looking ahead, semiconductor manufacturers will not only have to be concerned with how many clients buy their products, but perhaps with how many will do foundry in their facilities as well.

The "Fab in a Box"

As the semiconductor industry finds ways of doing more with less, Dataquest also believes that its capital investments will diminish in relation to productivity improvements, as illustrated in Figure 4. The need for broad product line suppliers to meet smaller, faster turnaround orders without throwing away profit will result not only in increased foundry relationships, but in the creation of smaller, more highly automated fabs. Dataquest analysts already see evidence of systems no larger than two telephone booths that are capable, using laser pantography, of performing the final metallization layers on already-packaged semicustom chips. The proliferation of such systems in design centers could make the "fab in a box" a reality.

Figure 4

Estimated Capital Spending versus Production



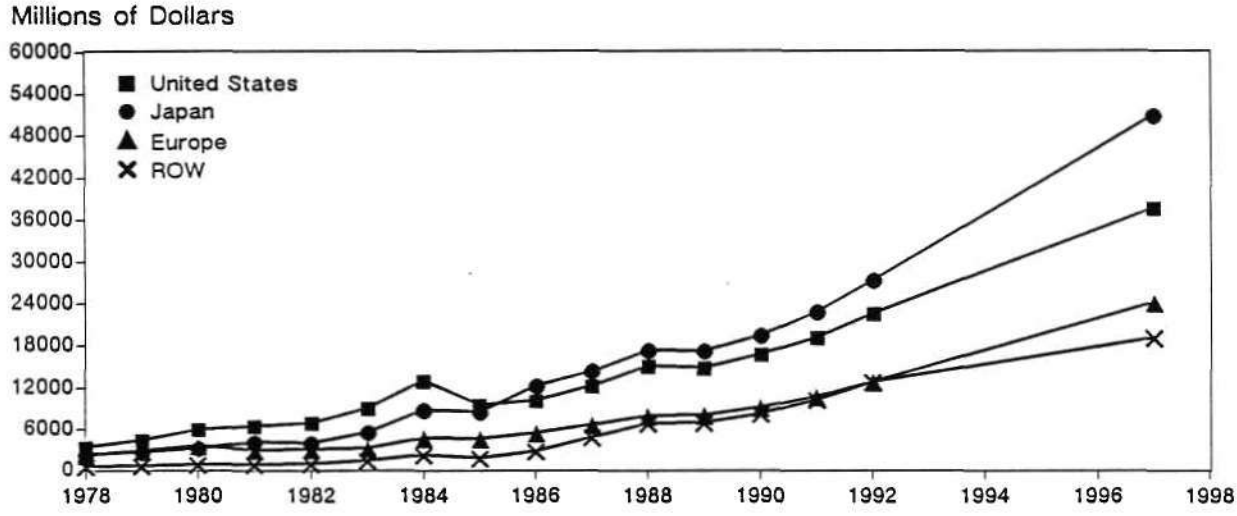
Source: Dataquest
November 1987

HOLDING ON TO WHAT YOU'VE GOT: MARKET SHARE IN A GLOBAL INDUSTRY

In the past 40 years, the U.S. semiconductor business has passed through the euphoria of being a brave new economic order, to arrive at the anguish of being yet another beleaguered U.S. industry under pressure from the Japanese juggernaut. U.S. semiconductor manufacturers now face a future in which they no longer possess the home field advantage—in 1986 the Japanese semiconductor market became the largest in the world, and is likely to remain so for the foreseeable future (see Figure 5).

Figure 5

Estimated Semiconductor Consumption by Region



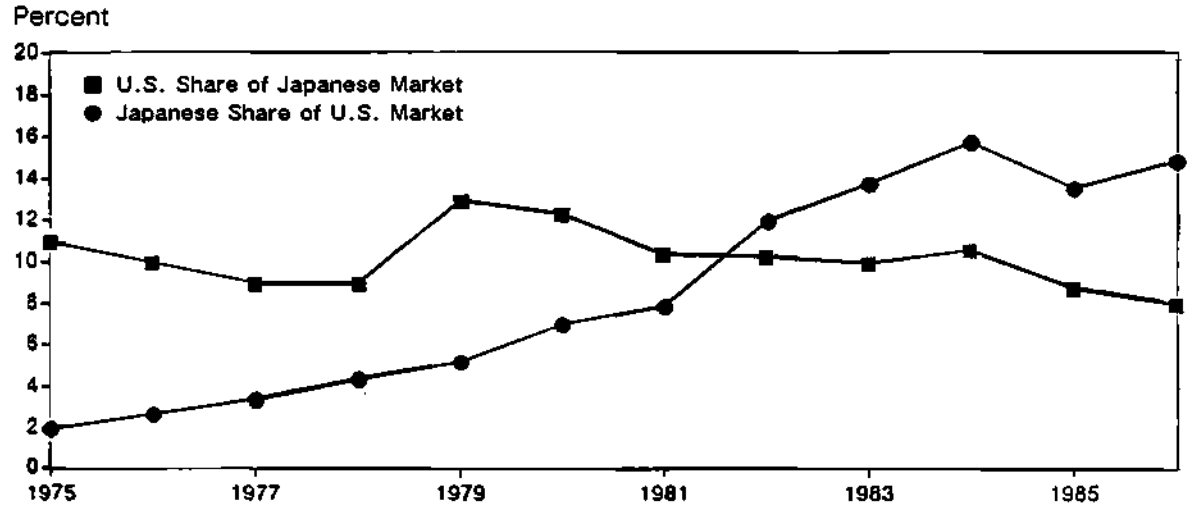
Source: Dataquest
November 1987

Market Access: The New Battle Cry

With trade tensions subsiding over the issue of semiconductor dumping, access to the Japanese market looms large in the minds of U.S. semiconductor manufacturers—and the U.S. Department of Commerce. Since the late 1970s, however, the U.S. share of the Japanese semiconductor market has diminished, while Japan's share of the U.S. market has increased (see Figure 6).

Figure 6

Japan's Share of the U.S. Semiconductor Market versus U.S. Share of Japan's Market



Source: Dataquest
November 1987

A Tale of Two Markets

While changes in currency exchange rates and the imposition of trade sanctions will have some impact on U.S. competitiveness vis-a-vis Japan, a fundamental problem remains for U.S. semiconductor suppliers: the Japanese electronic equipment market is a very different one from that of the United States. Dataquest believes that in 1987, the Japanese consumer electronics industry will account for nearly 39 percent of all semiconductor devices consumed in Japan. By contrast, the consumer segment will represent only 7.1 percent of the U.S. semiconductor market. With Japan's shift to offshore production in the wake of the rising yen, U.S. suppliers may be able to increase their share of the Japanese market and still find their percentage of the world market in decline.

The Role of Intellectual Property

Possessing technology has been an assumed prerequisite to entry into the semiconductor market. In the past, start-up companies with brilliant technology have floundered because they could not transition from the role of innovator into the role of world class manufacturer. The cost of making this transition has proved to be as much of a barrier to market entry as the possession of technology itself.

More recently, however, the industry has experienced the proliferation of alliances between U.S. start-up companies and Asian semiconductor manufacturers. Through second-source agreements and technology exchanges, smaller semiconductor companies in the United States have the potential to become more significant competitors. Of greater concern to established U.S. companies is the fact that in the process, overseas competitors with deep pockets may acquire technology cheaply and with it, access to U.S. distribution channels.

As the semiconductor industry turns increasingly to the creation of new products through cell-based design technology, another emerging intellectual property issue concerns the migration of standard products into alterable cells. Ultimately, the burden of protecting one's investment in standard products rests on patents and mask-level copyrights. Just how these protections will apply to cell-based libraries has yet to be tested through litigation.

THE POLITICS OF SEMICONDUCTORS

Just as the semiconductor industry's view of itself has changed in the past four decades, so too has its role in the geopolitical arena of world trade and national defense. For better or for worse, the semiconductor industry has become politicized. The Pentagon's Defense Science Board found that the U.S. semiconductor industry enjoys a lead in only three of 25 semiconductor technologies surveyed. This conclusion played a major role in raising the U.S. government's consciousness on the strategic importance of the domestic semiconductor industry and the need to establish Sematech as a vehicle for shared investment in generic manufacturing technology.

The imposition of trade sanctions against Japan by the Reagan administration have come about as a direct result of the U.S.-Japan semiconductor trade agreement. In its role as protector of the U.S. semiconductor industry, the federal government has sought to put an end to unfair trade practices and force greater access to Japan's markets.

Conflicting Interests

The extent to which the U.S. government can champion the cause of the semiconductor industry, however, has been called sharply into question. Given the current dependency of U.S. electronic equipment manufacturers on Japanese memory IC suppliers and the necessity of the U.S. electronic equipment industry to compete globally, trade legislation must carefully weigh the interests of a $12 billion U.S. semiconductor industry against those of a $234 billion U.S. electronic equipment industry.

The current situation regarding DRAM pricing highlights the conflict above. In its attempts to satisfy the U.S. government's concerns over predatory pricing, Japan's Ministry of International Trade and Industry (MITI) has created production controls and pricing guidelines affecting 256K and 1Mb DRAMs. As a result, Dataquest believes that by the fourth quarter of 1988, the cost of a 150ns 256K DRAM will be $3.00 (100,000 units/year volume), and that current DRAM pricing will delay a 4X price-per-bit crossover from the 256K to the 1Mb DRAM until the end of next 1988. In the meantime, Dataquest is observing consternation among a number of U.S. electronic equipment manufacturers over the supply/demand disparity that they perceive in the 1Mb DRAM market.

The complexity of the relationships between government, semiconductor suppliers, and end users will continue to grow as the newly industrialized countries of the world enter the competitive fray. In just the past few months, the International Trade Commission and the U.S. Customs Department have been pulled into intellectual property disputes between major U.S. semiconductor manufacturers and Asian competitors.

FACING MORTALITY

One of the more sobering aspects of midlife crises is facing one's mortality—the recognition that one's life is finite. The issue of mortality confronting the semiconductor industry is whether or not clear technological alternatives to etching circuits in silicon exist on the horizon.

At this time, the most obvious alternative to current silicon-based technology is the rapid progress being made in superconductive materials. In June of this year, Dataquest analysts attended the International Workshop on Novel Mechanisms of Superconductivity sponsored by the University of California at Berkeley. Several physicists at the conference expressed the belief that it might be possible to build simple superconducting devices within two to three years by layering superconducting thin films onto new substrate materials.

Death by Success

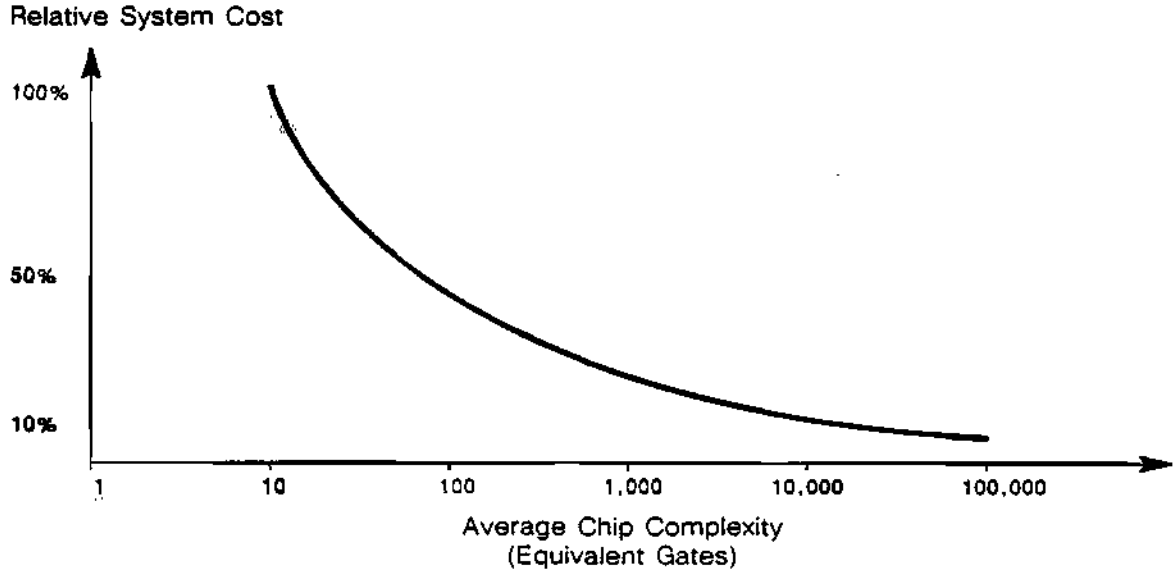
The demise of the semiconductor industry as we know it, however, may not come about through a technological revolution, but rather through tendencies already in the "genes" of the industry. The semiconductor industry could very well become a victim of its own success.

As suggested by Figure 7, the trends toward higher chip complexities, coupled with decreasing cost per function, have benefited end users and semiconductor manufacturers alike by endowing electronic equipment markets with greater elasticity of demand. Semiconductor chip sets are a current example of the industry's success in creating more powerful, less expensive systems through the continuing consolidation of ICs.

The sinister side of the industry's genius, however, has to do with the ultimate impact on the value of one's total available market when the potential exists to replace more than $20 worth of semiconductor devices with a $1 gate array. The semiconductor industry has now entered into a race between innovation and cannibalization. During 1987, we believe that semiconductor manufacturers will deliver as many gates of logic through gate array products as they will through standard logic products (Figure 8).

Figure 7

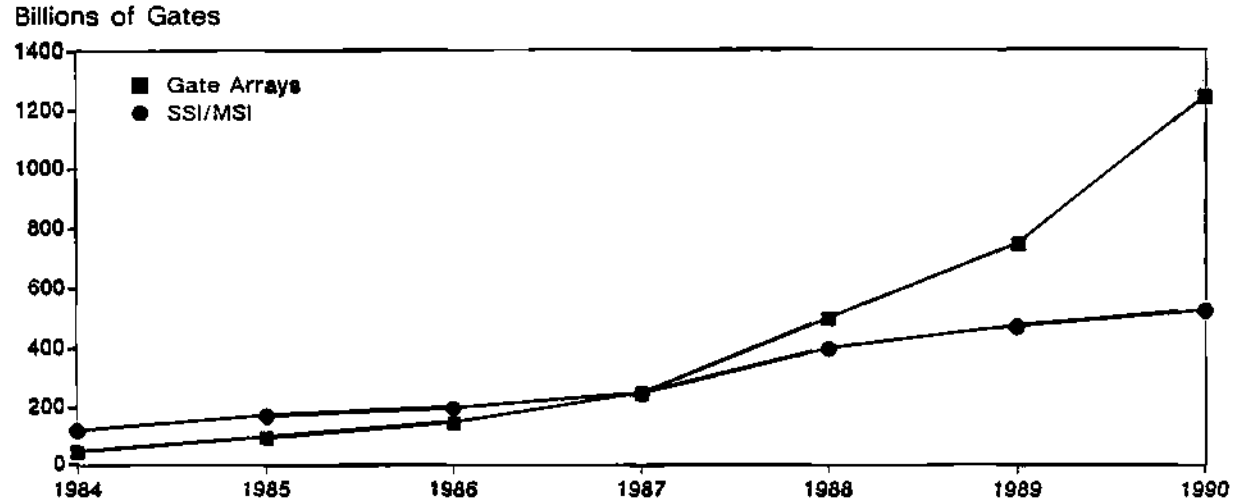
System Cost as a Function of Average Chip Complexity



Source: Bogert/Thomas Research

Figure 8

Expected Impact of Gate Arrays
on Semiconductor Logic Function Shipments



Source: Dataquest
November 1987

A BILLION TRANSISTORS ON A CHIP?

It has been predicted that by 1990 the semiconductor industry will be able to place a billion transistors on a chip. The following are a few examples of the kind of computing power this would make available to end users:

- 128 megabytes of RAM
- 1,000 VAX CPUs
- 20 Cray 2 CPUs
- 10 VAXs with memory
- 1/40 of a Cray 2 with memory

But can electronic equipment markets keep pace with the capability of the semiconductor industry to deliver higher levels of integration in silicon at lower costs per function? In a recent interview with Dataquest, Dr. K. Odagawa, the "founding father" of Toshiba's CMOS technology, observed, "Now that the ability to place more than one million transistors on a chip is a routine production event, the capability to design and process . . . far exceeds the technical requirements at this time. Market application is now the driving element."

What Business Are We In?

In the past four decades, it seems beyond belief that the semiconductor industry could have passed from the invention of the discrete transistor to envisioning the incorporation of a billion transistors on a single piece of silicon. During this transition, the industry has changed from a supplier of integrated circuits to a creator of integrated systems. In facing the next four decades, the success of the industry will depend on how it responds to this new role.

Perhaps the lessons of the steel industry apply here. The downfall of the U.S. steel industry may fundamentally have been that U.S. steel makers saw themselves in the business of producing steel, and were therefore buried by offshore competitors who could provide this service at a lower cost. Japanese steel makers, by comparison, see themselves as being in the business of supplying core materials. Faced with competition from the Pacific Rim, many of Japan's steel manufacturers have broadened their definition of core materials to include substances other than steel—such as silicon.

The future of the semiconductor industry may similarly depend on just what kind of business chip manufacturers see themselves participating in. If it is the business of etching circuits on silicon, the industry will sooner or later face its demise. If, on the other hand, chip manufacturers define their business as the consolidation of integrated systems, there is seemingly no limit to the industry's horizons.

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Peggy Wood
Michael Boss

Dataquest
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Research *Newsletter*

SEMS Code: 1987–1988 Newsletters: November
1987–24

CONTAMINATION CONTROL IN SEMICONDUCTOR PROCESSING

THE IMPORTANCE OF CONTAMINATION CONTROL

Major battles of the marketplace are being fought on the fab floor. Manufacturing yields and quality are today's new competitive battlegrounds. Today's manufacturer can no more do without the discipline of contamination control than the Armed Forces can do without basic training.

With existing methods of contamination control, it is possible to achieve minimum defect densities of approximately 0.1 defects per square centimeter. Yet most advanced processes today run somewhere in the neighborhood of 3.0 to 10.0 defects per square centimeter. Clearly, existing methods of contamination control could be substantially improved. Even slight improvements can substantially increase yields and productivity. As Table 1 illustrates, a decrease of 0.1 defect density per square centimeter can increase monthly net income by $830,000 per month (if the market exists to absorb the increased yields).

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 971-9000, Telex 171973

Table 1

Effects of Decreasing Defect Density

	Process 1	Process 2
Wafer Starts	10,000	10,000
Fab Yield	0.85	0.85
Wafer Size	100mm	100mm
Wafer Cost	$129.00	$129.00
Critical Masks	7	7
Defect Density	0.20	0.30
Random Yield	0.51	0.38
System Yield	0.70	0.70
Die Yield	0.36	0.26
Dice per Wafer	113	113
Good Dice	40	30
Die Cost	$ 3.20	$ 4.37
Package Cost	$ 1.00	$ 1.00
Burn-In/Text Cost	$ 0.50	$ 0.50
Test Yield	$ 0.90	$ 0.90
Circuit Cost	$ 5.22	$ 6.52
Circuit Price	$ 12.00	$ 12.00
Price/Cost Ratio	2.30	1.84
Sales per Wafer	$437.00	$320.00
Sales/Month ($M)	$ 3.71	$ 2.72
Mfg. Cost/Month ($M)	$ 1.80	$ 1.64
Net per Month ($M)	$ 1.91	$ 1.08

Source: Dataquest
November 1987

METHODS OF STUDYING PARTICULATES

One reason for the large discrepancy between achievable levels of contamination control and actual levels is that the application of the techniques of contamination control to the fab is relatively recent. Process engineers could not measure particulate contamination; therefore, they could not control it. However, about six years ago, with the advent of optical scattering methods, process engineers gained the ability to both count the number of particles on a wafer and to size them. The Great Particle Hunt had started.

However, process engineers in the fab still needed a theory of how particulates moved into the environment and onto the wafer. One theory arose from aerosol particle physics, a relatively old field that studied phenomena in areas such as meteorology and environmental sciences. Its principles had been used very sparingly in semiconductor processing until very recently.

An early systematic and quantitative analysis of particle movements in the fab was undertaken by a University of Minnesota group headed by Professor Benjamin Liu. Over the past several years, the group has developed a theory that describes the deposition of particles on wafers, taking sedimentation (or settling) and diffusion into account. The latest version of the theory also considers electrostatic effects on particle deposition.

One very interesting and potentially very useful phenomenon that may be used to help produce very clean equipment is thermophoresis. Thermophoresis is a force that drives particles from an area of hot gas to an area of cooler gas. It may be possible to use thermophoresis to shield wafers from particle deposition.

SOURCES OF CONTAMINATION

People

In the past, the major source of contamination in the fab was people. People are an important source of contamination simply because human skin regenerates from the inside out, and the dead outer cells flake off. Not only does skin regenerate, but it is also a very resistant chemical barrier. It can withstand various solvents, basic or acidic solutions, and the like. Because of this chemical stability, skin particles cannot be easily dissolved or eliminated from a wafer's surface. Skin oils are also very difficult to remove from a wafer.

One person can shed 100,000 skin particles of 0.3 microns or larger per minute. When a person exercises vigorously, this number can go up by almost an order of magnitude. Clean room gowns are not perfect filters; they are not able to contain all the particles cast off by humans. Therefore, it is important to realize that people are and will be continuous sources, or "torches," of contamination in a fab.

There are several simple means by which wafers can be protected from contamination from people; one is the adoption of a restricted product space that is always separate and upstream from the air flowing past people or any other source of contamination.

Second, because product space needs to be continuously washed by the steady flow of clean air, another useful principle can be applied: stagnant air is dirty air. Manufacturing situations are subject to continuous sources of contamination, so a constant flow of air is a very efficient method of removing particles from the area where they could cause a lot of damage.

Equipment manufacturers, then, need to design their equipment with operators and air flow in mind. Operators should be effectively isolated from wafers. Air flow should be directed in such a way that it will effectively prevent contamination under normal operating conditions. Dataquest believes that in the near future, computer-aided design of the flow and the distribution of contamination will be used to minimize air flow contamination on a routine basis.

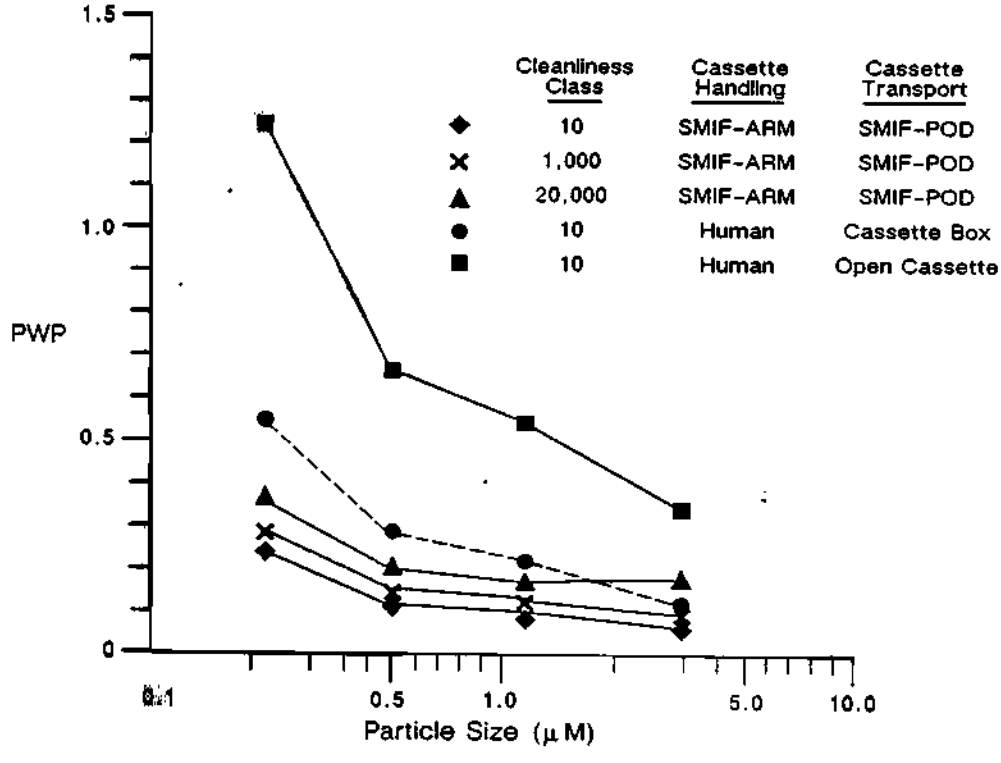
Robotics, which would allow the complete removal of people from the clean room, is yet another method of contamination control. This technology awaits further software developments that would enable in-process decisions to be made.

Another method of contamination control that has been suggested is the use of standard mechanical interface (SMIF) systems. SMIF systems are sealed ultraclean containers that are used for the storage, transport, and transfer of wafer cassettes into processing equipment. The effectiveness of the SMIF system is shown in Figure 1, which shows a comparison of SMIF handling versus human handling. A SMIF system was used in class 10, class 1,000, and class 20,000 clean rooms. This was compared to human transport in a class 10 clean room using both a closed and an open cassette of wafers. Interestingly, for the smaller particle sizes, there were fewer particles per wafer pass (PWP) with the SMIF system in a class 20,000 clean room than with human transport in a class 10 clean room with a closed cassette.

The first fab that uses SMIF boxes for all wafer transport has recently been completed in Bloomington, Minnesota, for VHSIC Technology Corporation (VTC). The SMIF technology was provided by ASYST Technologies, a San Jose, California, firm founded in 1982. We believe that the rest of the merchant semiconductor manufacturers will be watching this fab intently to monitor its success.

Figure 1

Comparison of SMIF and Human Handling



Source: Y. Shimizu Construction Co., Ltd.
Dataquest
November 1987

Equipment

In advanced VLSI fabs, the major source of contamination is no longer people, but equipment. A major source of equipment contamination is vacuum chambers. Vacuum chambers create considerable environmental disturbance during processing. When a vacuum chamber is vented, particles are agitated by the initial gas flow, which can be supersonic. When the chamber is pumped down, the small particles (less than 1 micron), which without a vacuum would remain airborne, are pulled to the wafer's surface by gravitational forces.

Additional equipment contamination problems occur because the equipment has to be maintained and repaired. Although a piece of equipment may be clean after manufacture, problems can arise when its rigorously clean environment is broken into for routine maintenance and repair. One remedy for this is the use of modular equipment that allows entire sections of equipment to be replaced in the fab while maintenance and repair work is performed off-site.

Contamination control is especially important in two areas of wafer manufacturing: photolithography and high-temperature processing. In photolithography, particulate control is important because particles can be printed, thus distorting the pattern on the wafer and causing defects. In high-temperature processing, particles (such as metal particles or sodium particles from humans) can diffuse into the wafer and create defect mechanisms.

Liquids

Liquids are also a significant source of contamination. Filtration of liquids and the transfer of particles from liquids to wafers is not well understood. Much basic work still needs to be done in this area, and liquids are a very difficult medium to study or work with. Many liquids are chemically very active, viscous, and difficult to store and transport.

Gases

Unlike liquids, the art of filtration of gases like nitrogen, oxygen, hydrogen, and argon is so well developed that it is possible to achieve extremely high particulate cleanliness. Filters should be tested under varying pressures, because most filters perform similarly under a steady state of pressure.

An interesting technique to decrease particulate contamination in gases even further has been recently developed by VLSI Standards, a company that specializes in providing particulate measuring and resistivity standards to semiconductor manufacturers. A double filter is placed at every point of use. Only the first filter is changed, and the debris created by changing the first filter is caught in the second filter, which will never have to be changed. The cleanliness of the reaction chamber, therefore, is guaranteed.

Air is, of course, a gas that is always present in a fab. Contamination by air is the best-understood and best-controlled source of contamination. Today's high-quality HEPA or ULPA filters produce class 10 or better air every time. However, some care has to be taken with regard to flow instabilities in air supply systems. Some researchers in the field report that a low-frequency vibration can cause sloughing of very large particles from the HEPA filters, which, because of their size, may not be detected by airborne particle counters.

MEASURES OF CONTAMINATION

A common measure of equipment cleanliness is particles per wafer pass, or PWP. PWP is a count of the number of particles of 0.3 microns or larger that a given piece of equipment contributes to a 100mm wafer for each pass of the wafer through the equipment.

State-of-the-art PWPs are shown on Table 2. Reliable PWP data for CVD and LPCVD do not exist, although this equipment is believed to be relatively dirtier than other types of equipment.

Table 2

State-of-the-Art PWP for Common Equipment Types

Equipment Type	PWP
Furnaces (cantilever, oxidation only)	1 PWP
Etchers	<10 PWP
Ion Implanters	2 PWP
Photolithography and Wafer Inspection	<1 PWP
Wafer Transport	<0.1 PWP

Source: Dataquest
November 1987

A great deal of variance of PWP exists within each category of equipment. For example, in photolithography and wafer inspection, some equipment available on the market today has performance of four to five orders of magnitude worse than 1 PWP, literally snowing the wafer with hundreds of particles per wafer pass. On the other hand, some automated robotic vehicles that perform cassette transport in the fab have achieved cleanliness levels of only about 1 particle added per 100 cassette-handling steps. One hundred cassette-handling steps are the total amount of handling that a cassette of wafers receives in a complete CMOS manufacturing cycle. This level of cleanliness is extremely good.

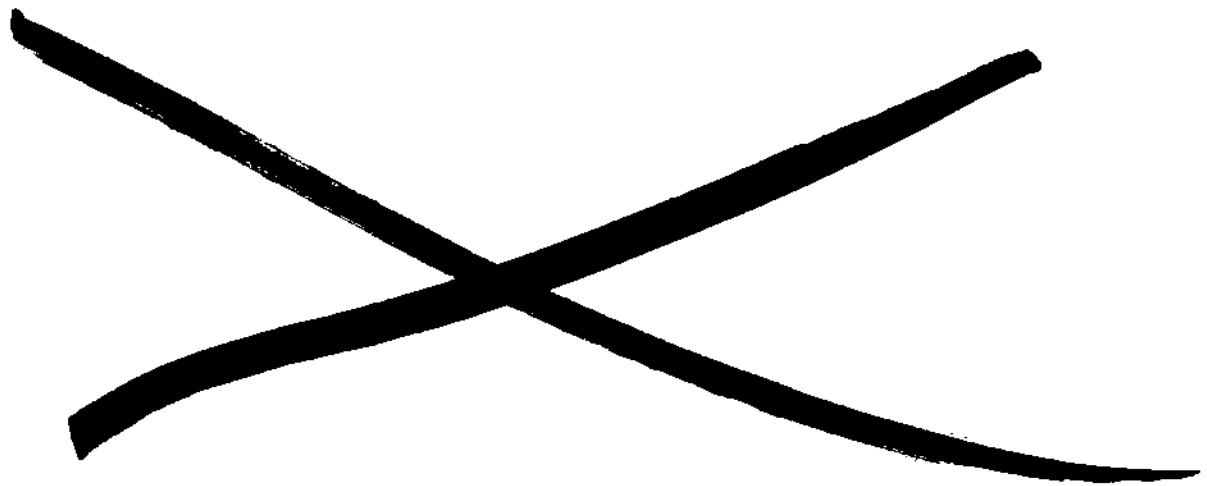
COMPONENTS OF A SUCCESSFUL CONTAMINATION-REDUCTION STRATEGY

The best way to achieve reduced particulate contamination is with a systematic, long-term, committed approach. There are, however, no easy solutions.

The most important thing to do is to start on the biggest problem first. In many cases, the biggest problem is—not surprisingly—the largest particles. A 5-micron particle will cause a defect almost anywhere on the wafer. After the large particles are eliminated, the next step is to look at the smaller particles in the most critical processing steps. Eliminate these next. Only after they are cleaned and continuously monitored should the less critical steps be examined.

In the end, how the fab is organized, what its level of discipline is, and how the materials, wafers, and masks are moved about the fab determines the overall cleanliness of the processing area. Particulate contamination reduction is a way of life in the fab that, if practiced religiously, will increase yields, quality, and competitiveness.

George Burns



December Newsletters

The following is a list of newsletters found in this section:

Dataquest
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Research Newsletter

SEMS Code: 1987–1988 Newsletters: December 1987–26

THE SEMICONDUCTOR GAS INDUSTRY: OUTLOOK ON THE U.S. MARKET

INTRODUCTION

In the semiconductor industry, process gases represent one category of consumable materials that are used throughout the fabrication of semiconductor devices, from polysilicon manufacturing and the growing of single silicon crystals, through the many steps of wafer fabrication, to the final stages of assembly and test. Dataquest recently completed an analysis of the 1985 and 1986 semiconductor gas markets in the United States. This newsletter provides a summary of the results from our study, including estimates of the nitrogen and silicon–precursor gas market segments in 1986, and our forecast of semiconductor gas consumption in the United States through 1991. Please note that the regional designation, United States, includes Canadian semiconductor manufacturing operations.

MARKET SUMMARY

In 1986, the U.S. bulk and specialty gas market was $215.5 million, up 8.0 percent from 1985 sales of $199.6 million. Four companies—Airco Industrial Gases, Air Products and Chemicals, Liquid Air Corporation, and Union Carbide Corporation—dominated the market with more than 90 percent of semiconductor gas sales in 1986. Table 1 summarizes Dataquest's estimates of the 1985 and 1986 bulk and specialty gas markets.

Table 1

U.S. 1985 and 1986 Bulk and Specialty Gas Markets
(Millions of Dollars)

Gas Category	1985	1986	% Growth 1985–1986
Bulk Gases	$160.4	$173.8	8.4%
Specialty Gases	39.2	41.7	6.4%
Total	$199.6	$215.5	8.0%

Source: Dataquest
December 1987

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 437-8000, Telex 171973, Fax (408) 437-0292

MARKET DEFINITIONS

An important part of any analysis of the semiconductor gas industry is a clear understanding of the definitions that are used to describe market segments, suppliers, and applications.

Gas Categories

Semiconductor gases are generally divided into two categories: bulk and specialty gases. The bulk semiconductor gases are nitrogen, oxygen, hydrogen, and argon. The designation of "bulk" typically refers to a discrete delivery of a large volume of gas by truck transport. These gases typically are delivered as cryogenic liquids because of the efficiency of transportation and storage prior to the vaporization stage at the semiconductor manufacturer's facility. Nitrogen gas provided through direct pipeline delivery, as well as customer on-site nitrogen generation plants, is also considered as part of the bulk gas category, even though the supply of nitrogen, in this sense, cannot be classified as discrete.

There are a large number of gases (more than 35) that are classified as semiconductor specialty gases. For that reason, a further segmentation of this category is necessary and is based on the chemical reactivity and functionality of the various specialty gases. Dataquest segments the specialty gas market into six categories: silicon-precursor gases, dopants, etchant gases, reactant gases, atmospheric/purge cylinder gases, and others. Specialty gases are used in comparatively smaller volumes than the bulk gases and, thus, are delivered in high-pressure cylinders.

Who Supplies?

In the United States, the major suppliers of bulk gases to the semiconductor industry include Airco, Air Products, Liquid Air, and the Linde division of Union Carbide. Some of the smaller bulk gas suppliers include Big Three (acquired by Liquid Air in 1987), Liquid Carbonic, and MG Industries/Scientific Gases. The major specialty gas suppliers to the U.S. semiconductor industry are Airco, Air Products, Matheson, Scientific Gas Products (acquired by Scott Environmental Technology in 1987), and Union Carbide. Smaller players in the specialty gas market are Big Three, Liquid Air (Alphagaz Division), Liquid Carbonic, MG Industries/Scientific Gases, Southland Cryogenic, and Synthatron (acquired by Solkatronic in 1986). While the major suppliers of specialty gas to the semiconductor industry typically supply the full complement of specialty gases, it is interesting to note that no one company has complete primary manufacturing capability. Therefore, in the specialty gas industry, it is necessary that companies sell products among themselves.

Who Buys?

For most gas companies, the semiconductor industry represents part of a loosely defined category of "electronics" customers. Because the designation of electronics is ambiguous, Dataquest has defined the customer base for semiconductor bulk and specialty gases to include the following:

- Polysilicon, silicon, and gallium arsenide operations
- Semiconductor manufacturers (both merchant and captive)
- Research cooperatives, government labs, and university semiconductor programs

Dataquest's gas market estimates reflect direct sales of bulk and specialty gases to the U.S. semiconductor industry. Sales of gases between companies are excluded because of the problems that arise from double– if not triple–counting of gas molecules along the distribution chain. In addition, revenue from gas–handling equipment sales and from those gases sold to semiconductor equipment companies is excluded; the exception is tungsten hexafluoride. Gases that are used in nonsemiconductor industry segments such as fiber optics, solar applications, or the printed circuit board industry are also excluded from our analysis.

It is important to note that direct comparison is not appropriate between Dataquest's 1984 market estimates and the 1985/1986 market estimates presented in this newsletter. The reason lies in the difficulty of defining the appropriate customer base and gas applications that constitute the semiconductor bulk and specialty gas markets. There was some confusion regarding these definitions in our 1984 study. For example, our 1984 U.S. specialty gas market estimate is likely on the high side due to the inclusion of some revenue from gas–handling equipment and sales of specialty gases between companies. As another example, our 1984 estimate of U.S. oxygen consumption is much higher than expected when compared with 1985 and 1986 estimates. In this case, oxygen consumption in nonsemiconductor applications was incorrectly included in our estimates.

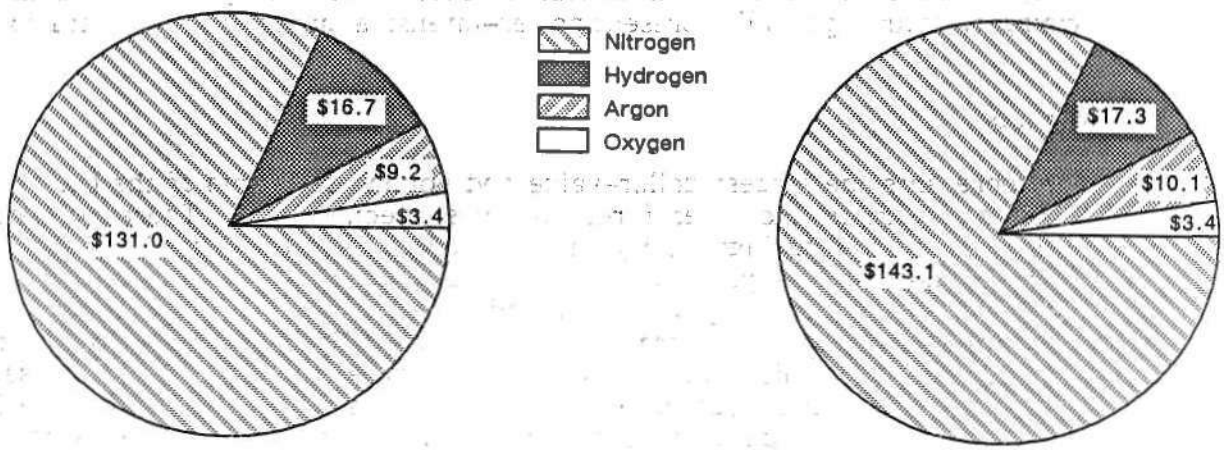
SEMICONDUCTOR BULK GASES

Market Overview

In 1986, the U.S. semiconductor bulk gas market was $173.8 million, up 8.4 percent from 1985 sales of $160.4 million. Figure 1 presents the 1985 and 1986 bulk gas markets, segmented by individual gas revenue. Table 2 presents volume estimates and average selling prices for the individual bulk gases in those same years. Nitrogen remains the major gas within this category, representing 82.3 percent of the dollar market in 1986 and 96.7 percent of the total bulk gas volume. Note, however, that while the volume of argon consumed in 1986 represents a mere 0.6 percent of the total bulk gas volume, it accounts for 5.8 percent of total bulk gas revenue.

Figure 1

U.S. 1985 and 1986 Bulk Gas Market
(Millions of Dollars)



1985 = $160.4 Million

1986 = $173.8 Million

Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
December 1987

Table 2

U.S. 1985 and 1986 Bulk Gas Market
Volumes and Average Selling Prices
(Billion Cubic Feet and Dollars per Hundred Cubic Feet)

	1985		1986	
Bulk Gas	Volume	ASP	Volume	ASP
Nitrogen (Total)	51.9		55.4	
On-Site	23.0	$ 0.14	24.7	$ 0.15
Pipeline	9.0	$ 0.23	9.5	$ 0.23
Liquid	19.9	$ 0.39	21.2	$ 0.40
Hydrogen	1.05	$ 1.59	1.09	$ 1.59
Oxygen	0.39	$ 0.88	0.41	$ 0.84
Argon	0.34	$ 2.74	0.37	$ 2.71
Total Bulk Gas Market	53.7	$160.4M	57.3	$173.8M

Source: Dataquest
December 1987

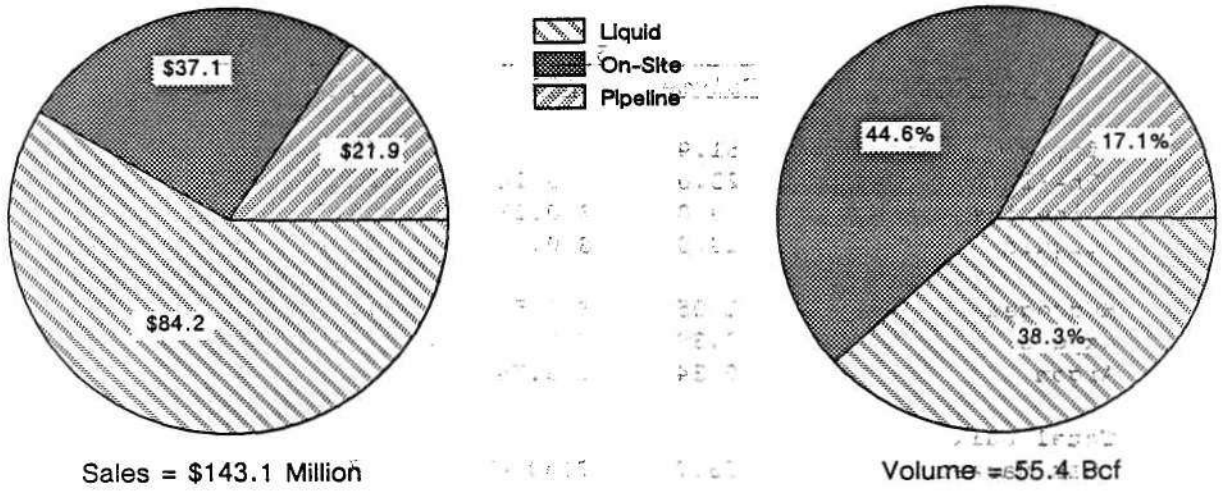
In general, the average selling price of the bulk gases in 1986 remained at or close to the 1985 level. This was due, in part, to sluggish market conditions within the semiconductor industry but also was influenced by low inflation rates holding down the cost of power production in the United States. The cost of power is a major factor in bulk gas pricing because nitrogen, oxygen, and argon generated from air separation plants, and hydrogen obtained from industrial processes such as thermal cracking or steam reforming of natural gas, all represent power-intensive manufacturing operations.

Nitrogen Markets

Nitrogen represents the largest dollar-value and volume segments of the U.S. semiconductor bulk gas market and, therefore, deserves special note. There are three different modes of delivering high-purity nitrogen to a semiconductor facility in the United States: an on-site air separation plant, a multicustomer pipeline network, and merchant deliveries of liquid nitrogen. (Dedicated single-customer pipeline delivery of nitrogen is included in on-site nitrogen generation.) Dataquest estimates that approximately 55.4 billion cubic feet (Bcf) of nitrogen were supplied to the U.S. semiconductor industry in 1986, up 6.7 percent over the 1985 consumption figure of 51.9 Bcf. Figure 2 presents the volume percentage and corresponding sales associated with each type of delivery mode for the 1986 nitrogen market. Between 1985 and 1986, there was no measurable change in the percentage of volume distribution of nitrogen among the three delivery modes.

Figure 2

1986 U.S. Nitrogen Market
(Billion Cubic Feet, Millions of Dollars)



Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
December 1987

Company Market Share

Table 3 ranks the leading bulk gas suppliers by 1985 and 1986 sales in the United States. Air Products had a substantial share of the bulk gas market, with sales of $77.4 million in 1986, or 44.5 percent of the $173.8 million market. Air Products' two nitrogen pipeline networks (in the Silicon Valley and Chandler, Arizona) accounted for approximately $21.9 million of that $77.4 million, or 28.3 percent of Air Products' bulk gas revenue from the U.S. semiconductor industry. The pipeline networks, evaluated on their own, correspond to 15.3 percent of 1986 nitrogen revenue and 12.6 percent of the total U.S. bulk gas revenue. It is clear that these two pipeline networks represent a strategic segment within Air Products' semiconductor bulk gas business.

Table 3

U.S. Bulk Gas Market—1985 and 1986 Company Rankings
(Millions of Dollars, Percent Market Share)

	1985		1986	
Company	Sales	Share	Sales	Share
Air Products	$ 71.6	44.7%	$ 77.4	44.5%
Linde/UCC	42.4	26.5	46.1	26.5
Liquid Air	21.0	13.1	23.1	13.3
Airco	20.3	12.7	21.8	12.5
Others	5.0	3.1	5.5	3.2
Total	$160.4	100.0%	$173.8	100.0%

Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
December 1987

The Linde division of Union Carbide ranked a strong second in the 1986 bulk gas market, with sales of $46.1 million, or 26.5 percent share. The Linde high-purity nitrogen pipeline system in the International Business Park in San Jose, California, still represents a very small portion of the overall nitrogen delivered by pipeline; however, volume usage along this pipeline is increasing. Liquid Air and Airco were closely ranked, with 13.3 percent and 12.5 percent of the 1986 bulk gas market, respectively.

SEMICONDUCTOR SPECIALTY GASES

Market Overview

In 1986, the U.S. specialty gas market was $41.7 million, up 6.4 percent over the 1985 market of $39.2 million. Silicon–precursor gases (silane, dichlorosilane, trichlorosilane, and silicon tetrachloride) continue to represent the largest revenue category within the specialty gas market, followed by the etchant gas category, which includes carbon tetrafluoride, a variety of halocarbon gases, as well as others. Table 4 presents the 1985 and 1986 U.S. specialty gas markets by gas category. In Table 4, atmospheric/purge cylinder gases and other gases have been combined into a single category.

Table 4

U.S. 1985 and 1986 Specialty Gas Market
(Millions of Dollars)

Gas Category	1985 Sales	1985 Percent	1986 Sales	1986 Percent
Silicon Precursors	$13.3	33.9%	$14.0	33.6%
Etchants	10.7	27.3	11.5	27.6
Atmospheric/Other*	6.2	15.8	7.0	16.8
Reactants	5.5	14.0	5.7	13.7
Dopants	3.5	8.9	3.5	8.4
Total	$39.2	100.0%	$41.7	100.0%

*Atmospheric/Other contains both the atmospheric/purge cylinder gases and the "other gases" categories.

Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
December 1987

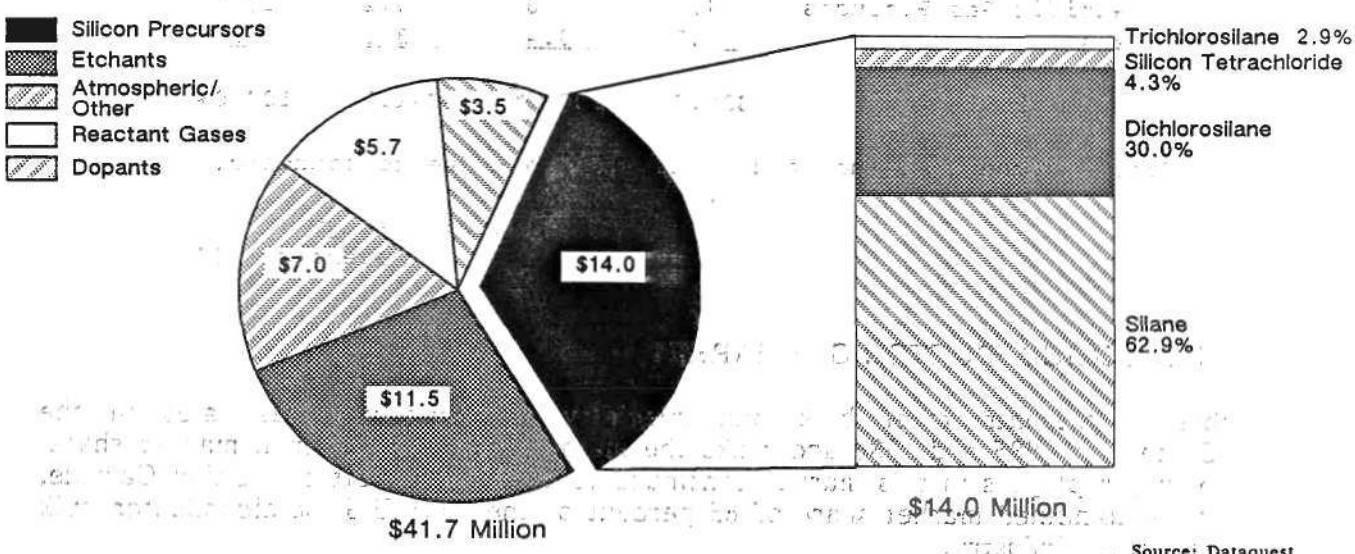
Silicon–Precursor Gases

Dataquest has chosen to examine the market for individual gases within the silicon–precursor gas segment. The silicon–precursor gases are used in epitaxial and chemical vapor deposition processes to deposit layers of silicon or silicon compounds (i.e., silicon dioxide, silicon nitride) onto silicon substrates. In 1986, the silicon–precursor gases represented $14.0 million of the $41.7 million U.S. specialty gas market. Figure 3 presents the silicon–precursor gas segment, by individual gas revenue in the context of the total 1986 specialty gas market. Silane sales in 1986 were

$8.8 million, or 62.9 percent of the silicon–precursor market, while dichlorosilane sales were $4.2 million, or 30.0 percent of the $14.0 million market. These two gases combined represented almost 93.0 percent of the silicon–precursor gas segment and 31.2 percent of the total U.S. specialty gas market in 1986.

Figure 3

1986 U.S. Specialty and Silicon–Precursor Gas Markets
(Millions of Dollars)



Source: Dataquest December 1987

Company Market Share

Table 5 presents Dataquest's market share estimates for the major suppliers of specialty gases to the U.S. semiconductor industry in 1985 and 1986. Airco was the market leader in 1986 with $11.0 million in sales, or 26.4 percent of the $41.7 million market. Airco and Air Products experienced a slight increase in market share in 1986 over 1985, while Union Carbide's market position remained essentially constant. The three top players in the specialty gas market are also major bulk gas suppliers to the semiconductor industry, and Dataquest believes that the infrastructure and service support networks of those companies were significant factors in gaining or maintaining specialty gas market share in 1986, a recession year in the industry. Both Matheson and Scientific Gas Products dropped a small amount in market share in 1986.

The Alphagaz specialty gas division of Liquid Air, the third major bulk gas supplier in the United States, was still a small player in the 1986 specialty gas market and is included in the "Others" category. However, Dataquest believes that the company will become a more significant player in the next few years, since Liquid Air is committed to expanding its semiconductor customer and applications bases.

Table 5

U.S. Specialty Gas Market—1985 and 1986 Company Rankings (Millions of Dollars)

Company	1985 Sales	1985 Share	1986 Sales	1986 Share
Airco	$10.2	26.0%	$11.0	26.4%
Linde/UCC	8.6	21.9	9.1	21.8
Air Products	6.0	15.3	7.5	18.0
Matheson	6.0	15.3	6.1	14.6
Scientific Gas Products	4.7	12.0	4.2	10.1
Others	3.7	9.4	3.8	9.1
Total	$39.2	100.0%	$41.7	100.0%

Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
December 1987

TOTAL U.S. SEMICONDUCTOR GAS MARKET

Table 6 presents total bulk and specialty semiconductor gas sales in the United States for 1985 and 1986 and ranks the major suppliers by overall market share. The two major players in this market continued to be Air Products and Union Carbide, which had a combined market share of 65 percent of the 1986 U.S. semiconductor bulk and specialty gas industry.

Table 6

U.S. Semiconductor Gas Market—1985 and 1986 Company Rankings (Millions of Dollars)

Company	1985 Sales	1985 Share	1986 Sales	1986 Share
Air Products	$ 77.6	38.9%	$ 84.9	39.4%
Linde/UCC	51.0	25.6	55.2	25.6
Airco	30.5	15.3	32.8	15.2
Liquid Air	21.0	10.5	23.1	10.7
Matheson	6.0	3.0	6.1	2.8
Scientific Gas Products	4.7	2.4	4.2	2.0
Others	8.7	4.4	9.3	4.3
Total	$199.6	100.0%	$215.5	100.0%

Note: Numbers may not add to totals shown due to rounding.

Source: Dataquest
December 1987

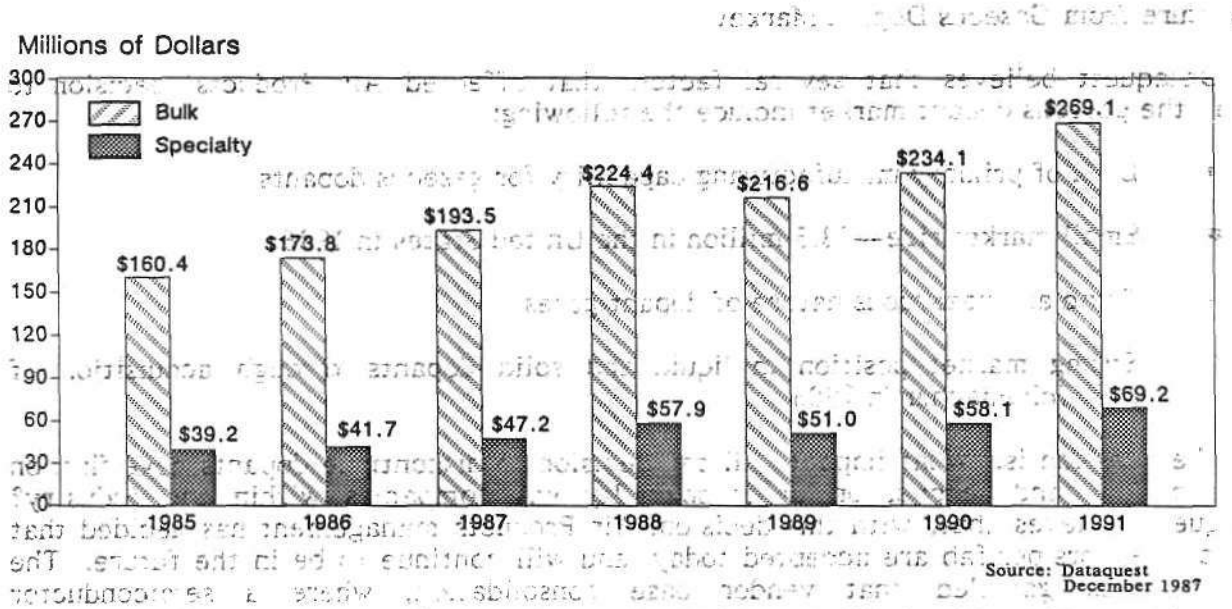
SEMICONDUCTOR GAS FORECAST

Dataquest's U.S. bulk and specialty gas forecast is based on our silicon forecast, in particular, the forecast of silicon consumption, as measured in wafer starts and the trend in increasing wafer size. For the bulk gas forecast, our forecast includes a factor that depends upon the installed base of equipment, since a large volume of nitrogen is used to maintain the integrity of processing equipment, even in times of low production levels. This means that nitrogen consumption has a stabilizing influence on the bulk gas market during times of industry recession.

It has been assumed that gas pricing remains constant at 1986 levels, and no inflationary factors have been included. This is not an unreasonable assumption, since power costs are not expected to increase substantially over the next few years. In general, while new higher-purity gases will command higher prices, competitive market pressures will keep prices relatively stable at their 1986 values.

Figure 4 presents the U.S. bulk and specialty gas forecast through 1991. Bulk gases are expected to grow at a compound annual growth rate (CAGR) of 9.0 percent between 1985 and 1991, while specialty gases are expected to grow at a CAGR of 9.9 percent. The combined semiconductor bulk and specialty gas market in the United States is projected at $338.3 million in 1991.

Figure 4
U.S. 1985–1991 Semiconductor Gas Markets
(Millions of Dollars)



DATAQUEST ANALYSIS

Insight Into Specialty Gases

The specialty gas companies are unique when compared with other electronic materials companies that sell products to the semiconductor industry. What makes this market different is that no one specialty gas company has primary manufacturing capability for all of the specialty gases that it provides to the industry. Thus, a specialty gas company typically must buy some of its products from a competitor.

In contrast to the bulk gas market, where a single gas company supplies a given fab facility, multiple specialty gas vendors per fab are the norm, rather than the exception. Dataquest estimates that, on the average, there are two to three specialty gas companies supplying a given fabrication facility in the United States; however, in some cases, this number can be as high as five or six. Because of this practice of multiple vendors per facility, a semiconductor manufacturer can select and choose between specialty gas companies in order to obtain the lower possible price for a given specialty gas product.

In light of these factors, an important question facing specialty gas suppliers is whether it is a cost-effective practice and makes good market sense for a company to compete in all specialty gas segments, if that company does not have the cost-competitive advantage of being a primary manufacturer of certain gases. Dataquest believes that Air Products recently went through just such an analysis as part of its decision to discontinue supplying dopant gases to the semiconductor industry in early 1987. This strategic reassessment of market opportunities by a major vendor is worthy of further examination.

Departure from Gaseous Dopant Market

Dataquest believes that several factors that affected Air Products' decision to depart the gaseous dopant market include the following:

- Lack of primary manufacturing capability for gaseous dopants
- Small market size—$3.5 million in the United States in 1986
- Toxic and hazardous nature of dopant gases
- Strong market position in liquid and solid dopants through acquisition of J.C. Schumacher in 1986

The question is: What impact will the decision to discontinue dopants have first on Air Products, and second, on other specialty gas companies within the industry? Dataquest believes that, with this decision, Air Products management has decided that multiple vendors per fab are accepted today, and will continue to be in the future. The company has gambled that vendor base consolidation, where a semiconductor manufacturer will favor a single-supplier relationship, will not occur, at least in this electronic materials segment. The company has, in a sense, decided to play to its strengths rather than finance what was probably a less-than-profitable product segment.

Dataquest believes that this decision probably will not have a negative impact on Air Products' specialty gas sales to the semiconductor industry. The company is very strong in the bulk gas industry, fluorine gas chemistry, and the etchant gas segment. There likely will be some transition period while purchasing agents readjust their procedures to accommodate a specialty gas supplier that will not place a bid on every specialty gas that a customer requires. In the long run, however, we do not believe that this decision will seriously affect Air Products' position within the industry.

Finally, Dataquest believes that a potential impact on other specialty gas suppliers will be a domino effect, in that other players may decide to follow suit and stress their strengths rather than invest in their weaknesses. This will continue to be an interesting area to watch in the specialty gas market in the months to come.

Peggy Marie Wood

Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

SEMS Code: 1987–1988 Newsletters: December 1987–27

STOCK MARKET CRASH LOWERS LEVEL OF OPTIMISM

SEMICONDUCTOR MARKET OUTLOOK

At the Dataquest Semiconductor Conference on October 19, we presented our 1988 outlook for the worldwide semiconductor market and for capital spending by projecting 24 percent and 30 percent growth, respectively. The worldwide stock market crash that began the same day, however, has prompted us to reevaluate our assumptions and monitor the market for any change in conditions. Although we have seen no signs of major revisions in business plans, the caution that we hear in response to our surveys leads us to consider it critical that we articulate a downside to our original forecast. Given these current cautionary consumer and business expectations, we project the downside for the worldwide semiconductor market to be only 17 percent growth in 1988, as shown in Table 1.

Table 1

Worldwide Semiconductor Market—Downside Estimate
(Percent Change in U.S. Dollars)

	1987	Q1'88	Q2'88	Q3'88	Q4'88	1988
North America	22.6%	1.5%	4.0%	2.2%	1.0%	15.0%
Japan	17.9%	1.5%	2.3%	3.4%	0.3%	17.1%
Europe	22.6%	2.9%	1.9%	0.1%	2.5%	10.7%
Rest of World	65.7%	3.8%	8.8%	7.8%	1.7%	30.2%
Worldwide	24.8%	2.0%	3.6%	3.1%	1.2%	17.0%
Japan (in Yen)	1.8%	1.5%	2.3%	3.4%	0.3%	12.0%
Europe (in ECU)	6.8%	2.9%	1.9%	0.1%	2.5%	10.4%

Source: Dataquest
December 1987

Dataquest Incorporated, 1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 437-8000, Telex 171973, Fax (408) 437-0292

We see a window of opportunity in 1988 for the world semiconductor market in the 17 percent to 24 percent range, as shown in Table 2. Should the caution escalate to panic, resulting in order cancellations and rescheduling, we will modify this bandwidth. No evidence of any such actions exists as yet. Our next scheduled Quarterly Industry Forecast will be issued on January 15, 1988, showing the customary product details for the next eight quarters.

Table 2

Worldwide Semiconductor Market—Forecast Range
(Percent Change in U.S. Dollars)

	1987	1988
North America	21%-23%	15%-23%
Japan	18%-20%	17%-20%
Europe	20%-23%	11%-17%
Rest of World	65%-68%	30%-41%
Worldwide	24%-25%	17%-24%
Japan (in Yen)	2%-3%	12%-18%
Europe (in ECU)	5%-7%	10%-12%

Source: Dataquest
December 1987

CAPITAL SPENDING OUTLOOK

The manufacturers' continuing commitment to capital spending is encouraging. Dataquest, therefore, expects that capital spending will continue to expand, even in a less optimistic climate. Our downside forecast for 1988 looks for worldwide capital spending to expand over 1987 levels by 20 percent (see Table 3).

The forecast window for capital spending in 1988 ranges from 20 percent to 30 percent as shown in Table 4.

Table 3
Downside 1988 Capital Spending and Production Forecast
(Millions of Dollars)

	1987	1988	Percent Change 1987-1988
		Capital Spending	
United States	$1,908	$2,279	19%
Japan	1,682	2,119	26%
Europe	823	892	8%
Rest of the World	406	606	49%
Captive	1,104	1,225	11%
Total	$5,924	$7,121	20%
		Production	
United States	$14,870	$17,139	15%
Japan	18,069	20,934	16%
Europe	4,519	5,340	18%
Rest of the World	961	1,510	57%
Captive	6,088	6,730	11%
Total	$44,508	$51,652	16%

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
December 1987

Table 4

Capital Spending Forecast Range: 1988
(Percent Change in U.S. Dollars)

United States	19%-39%
Japan	26%-26%
Europe	8%-26%
Rest of the World	49%-49%
Captives	11%-19%
Total	20%-30%

Source: Dataquest
December 1987

ANALYSIS

End Markets and Semiconductors

A survey of leading economists projects 1988 gross national product (GNP) growth at least one full percentage point lower than the estimates before the crash in both the United States and Japan. The Dun & Bradstreet chief economist, Joe Duncan, in particular, has lowered his estimate of 1988 real GNP growth in the U.S. from 3.3 percent to 2.8 percent. It is significant to note the deceleration of growth from 3.1 percent in 1987 to 2.8 percent in 1988. Dataquest's own estimate for real gross domestic product (GDP) growth in Japan is for a mild acceleration from 2.5 percent in 1987 to 3.0 percent in 1988, contrasted with our previous estimate of 4.0 percent. We are continually monitoring the impact of the yen appreciation on Japanese electronics exports. We expect the European economy to continue to stagnate at 2 percent growth in 1988.

Dataquest projects that U.S. electronic equipment production will grow 6 to 7 percent in 1988. We had projected earlier that computer and communications equipment production would accelerate into 1988, topping 15 percent growth next year. This accelerated growth would have caused significant inventory build-up and price increases in semiconductors. We now expect 1988 communications equipment production to grow only 6 to 7 percent and computer equipment production to grow 8 to 9 percent. The lower growth ramps, coupled with tightening control over inventories and costs would lower the growth rate in the U.S. semiconductor market by as much as 7 to 8 percent, to only 15 percent.

While the demand should continue to exceed supply in the leading-edge products such as 1Mb DRAMs and high-end microprocessors, we should begin to see softening demand and price erosion for commodity products in 1988.

Japanese electronic equipment production should grow only 6 to 7 percent in 1988; this estimate is lower than our earlier estimate of 10 percent. While we expect the telecom sector to continue to be strong locally, the sharp yen appreciation to the ¥135 level should limit equipment exports and production. The net result is a 12 percent growth in the Japanese semiconductor market, measured in yen.

Electronic equipment production in Europe is expected to be very soft, with only 3 to 5 percent growth in 1988. This lowers the European semiconductor market growth rate to only 10 percent in 1988, measured in local currency.

The Rest of World market, including Asia/Pacific, is most sensitive to the U.S. economy; we anticipate softness here, compared with the high growth in 1987. The saving grace is that the Korean Olympics should bolster local demand.

Capital Spending

The capital spending plans of semiconductor manufacturers have not changed since the crash. Some companies—Intel, for example—have increased their capital spending plans because demand continues to exceed supply. All of the companies contacted by Dataquest, however, reported that they are watching developments in the general economy and their customer base very closely, and that they are prepared to cut their spending plans if the need arises.

Our analysts in Japan and in the Pacific Rim countries report vigorous growth of orders. We do not expect semiconductor manufacturers in either of these areas to decrease their spending plans unless the downside risk of a recession becomes much greater.

Japan will continue to replace capacity (see our SEMS Newsletter code 1987-23 "Capital Spending Forecast: Slower but Steadier Growth," May, 1987), especially for state-of-the-art devices such as 1- and 4-megabit production.

Capital spending in Europe will show the least growth in the event of slower growth in 1988. We expect capital spending in Europe to grow only 8 percent in 1988, while production in Europe grows 18 percent because the relatively large amounts of plant and equipment brought on-stream in the last few years are now coming into full production.

Dun & Bradstreet has lowered its growth projections for the U.S. economy in 1988, from 3.3 percent growth to 2.8 percent. As we have already noted, there is some potential that the generally slower economic growth in 1988 will slow down the growth of the semiconductor industry, and hence, capital spending in 1988. This need not be bad news.

In the past, semiconductor equipment companies have been at the very tip of the whip of the semiconductor business cycle. For example, in 1984, semiconductor production increased 44 percent while capital spending increased 106 percent; in the semiconductor recession of 1985 to 1986, semiconductor production increased only 9 percent from 1984 to 1986, while capital spending plunged 37 percent. The impending slowdown could ameliorate this volatility. There will be less of a mismatch between supply and demand for semiconductors; orders, though perhaps slower than they would have been, will remain real. There will therefore be less "overheating," both in the general economy and in the semiconductor industry. With less overheating, there will less of a likelihood of sliding into a recession, which can only be good news for an equipment industry just climbing out of the last industry recession.

CONCLUSION

In summary, we are presenting a downside to our 1988 worldwide semiconductor market estimate and capitol spending forecast, anticipating cautionary consumer and business expectations as a result of the less optimistic investor expectations evidenced by the recent stock market crash. At the downside, our level of optimism is lowered to 17 percent growth in the worldwide semiconductor market in 1988.

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George Burns
Joseph Borgia
Stan Bruederle

