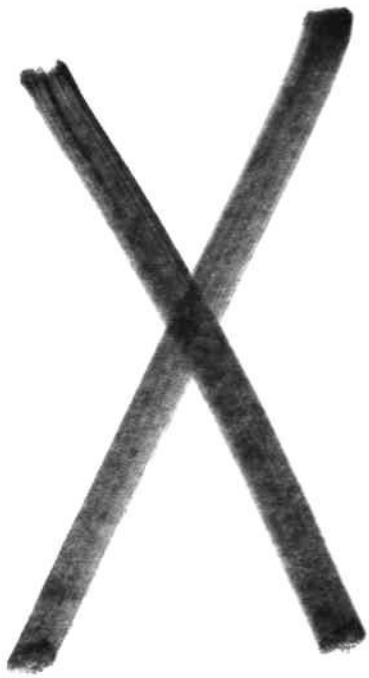

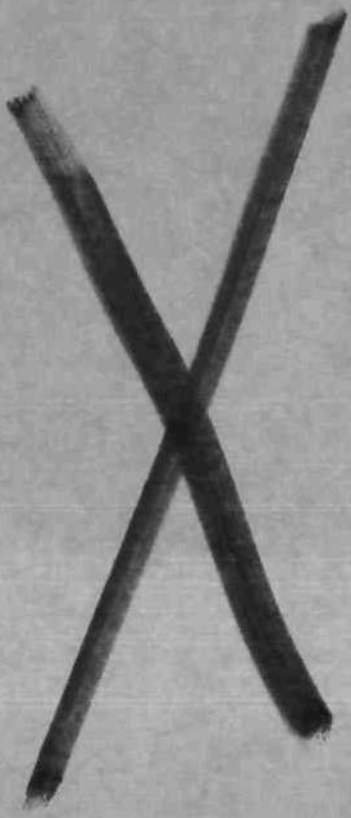

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Research Newsletter

MIXED-SIGNAL ICs: NORTH AMERICAN DOMINATION MASKS A WORLDWIDE OPPORTUNITY

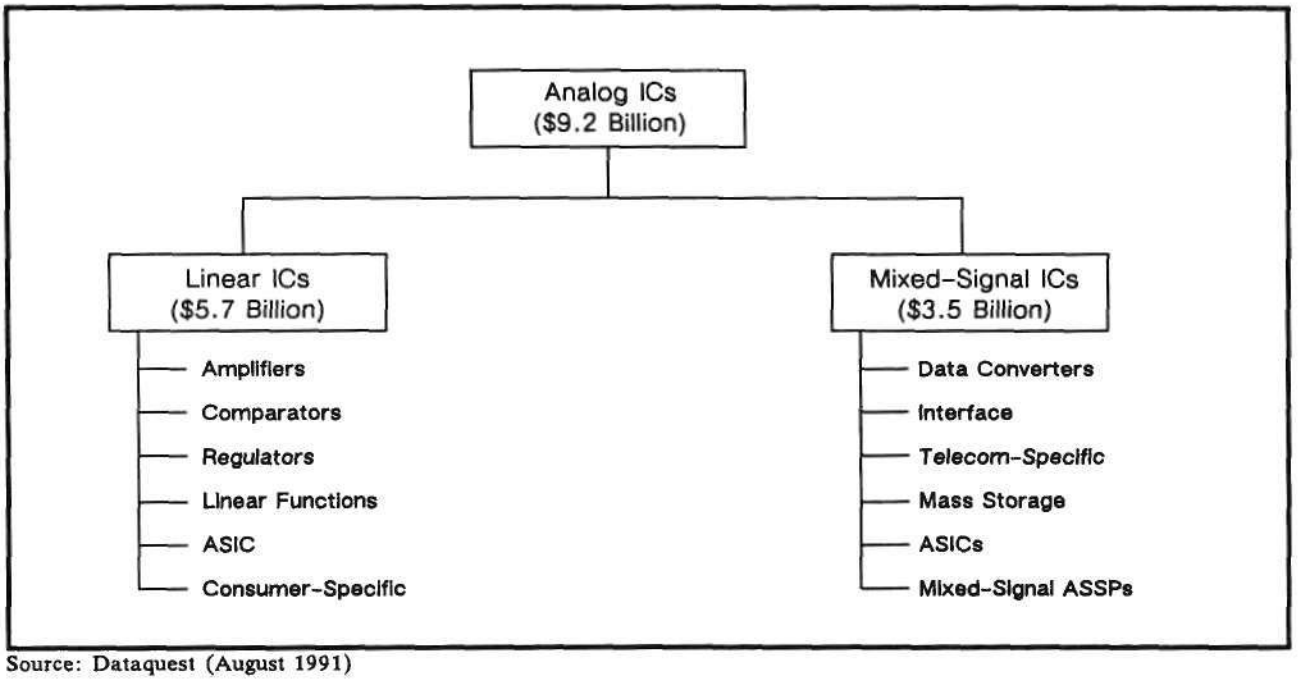
SUMMARY

Although North American suppliers of analog ICs have been losing worldwide market share during the past decade, mixed-signal IC dominance still belongs strongly to North American vendors. Mixed-signal IC manufacturing requires a combination of analog design, process, and test expertise and specialty processing capabilities such as linear-compatible CMOS and BiCMOS. These particular skills have traditionally been the strength of North American suppliers. This newsletter looks at the mixed-signal IC market, examining the strength of regional suppliers to penetrate this growing worldwide market.

MIXED-SIGNAL VERSUS LINEAR ICs

Both mixed-analog/digital and linear ICs are included in the analog IC category. Figure 1 shows these two major divisions of the analog IC market. Although not always completely clear-cut, general categories can be assigned to the mixed-signal or linear IC divisions. Mixed-signal IC categories

FIGURE 1
Analog Product Family



Source: Dataquest (August 1991)

SIS Newsletters 1991 Analog

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include data converters, interface ICs, mass-storage ICs, telecommunications-specific ICs, and mixed-signal ASICs. Linear ICs, which are completely analog in nature, include the standard linear functions such as amplifiers, comparators, regulators, and special-function ICs as well as the very large consumer-specific IC category.

Competition

The 1990 mixed-signal IC market share listing shown in Table 1 shows the strong presence of North American suppliers, which hold 8 of the top 10 positions. It is significant that not one of the top 10 suppliers is a Japanese company.

TABLE 1
1990 Market Shares for Mixed-Signal ICs

Rank	Company	Percent Share	Revenue (Millions of Dollars)
1	SGS-Thomson	8.1	282.3
2	National Semiconductor	7.5	263.5
3	Analog Devices	6.8	236.0
4	Texas Instruments	6.3	219.8
5	Silicon Systems	4.6	162.0
6	Rockwell	4.6	160.0
7	Harris Semiconductor	3.9	136.9
8	AT&T	3.9	135.7
9	Motorola	3.6	124.2
10	GEC Plessey	2.5	89.0
	Others	48.0	1,660.6
	Total	100.0	3,470.0

Source: Dataquest (August 1991)

TABLE 2
1990 Market Shares for Linear ICs

Rank	Company	Percent Share	Revenue (Millions of Dollars)
1	Philips	9.1	521.7
2	Toshiba	8.5	483.0
3	Sanyo	6.7	380.8
4	Matsushita	6.2	353.4
5	National Semiconductor	5.7	326.6
6	NEC	5.1	289.0
7	Sony	5.0	284.0
8	SGS-Thomson	4.8	271.7
9	Motorola	4.7	268.8
10	Mitsubishi	4.6	262.0
	Others	40.0	2,297.0
	Total	100.0	5,738.0

Source: Dataquest (August 1991)

North America's mixed-signal IC market share, as shown in Table 1, contrasts dramatically with the linear IC segment market shares shown in Table 2. Note that only two North American companies made the top 10 in the linear supplier listing. Six Japanese suppliers and two European suppliers also were in the top 10. The linear listing is dominated by vertically integrated manufacturers that supply ICs for their own internal use as well as to the merchant market. The linear listing also shows a stronger share of the total market by the top 10 suppliers than the does mixed-signal market (60 versus 52 percent), a common characteristic of a more mature product line.

REGIONAL MARKETS

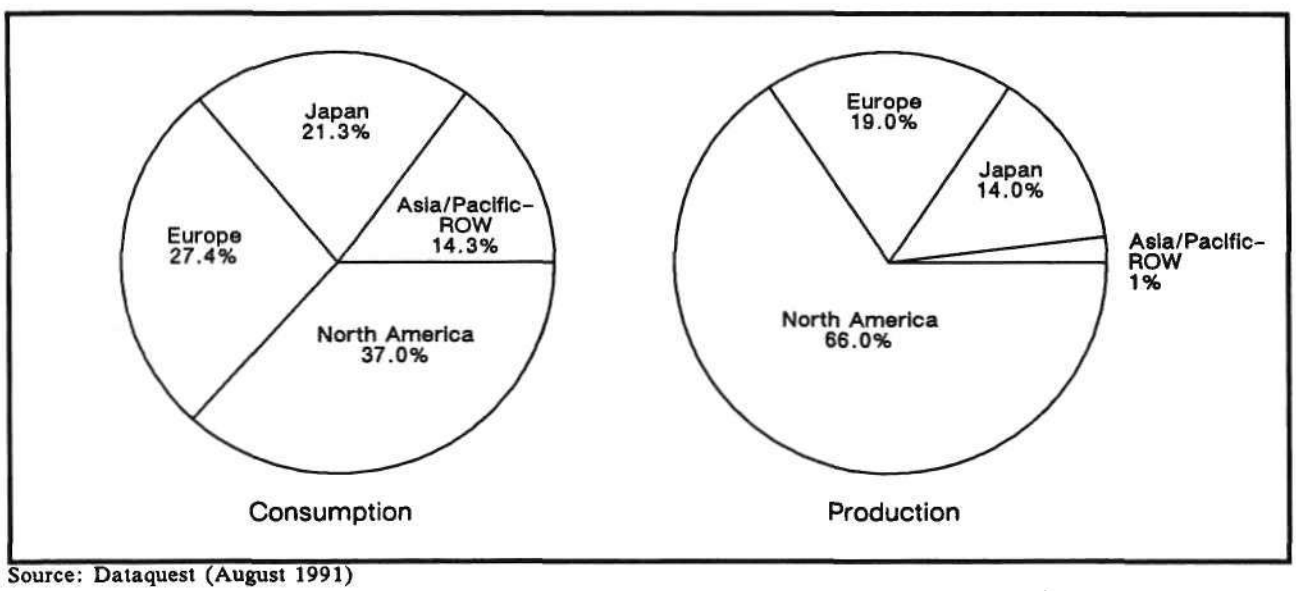
The market share tables show North America's strength in supplying to the mixed-signal market, which is due, in part, to the size of the North American market for mixed-signal ICs. Mixed-signal IC consumption by region is compared with production by region in Figure 2. This figure shows North America to be both the dominant consumer and producer of mixed-signal ICs, which contrasts with the comparable regional consumption/production graphs for linear ICs (see Figure 3). It is interesting to note that Japan and North America have reversed mixed-signal and linear IC consumption profiles (21 and 39 percent, respectively, for Japan, and 37 and 20 percent, respectively, for North America).

Europe is notably consistent in both mixed-signal and linear IC consumption and production, a position that is less likely to be jarred by dynamic changes in the local market. Although it is apparent that Japan is not likely to be displaced from its dominance in the relatively mature consumer-specific linear IC market, it is less apparent (and far less likely) that North American dominance in mixed-signal ICs will continue at this magnitude. Purely linear solutions in all markets, including the consumer market, are being displaced by mixed-analog/digital solutions involving microprocessor control and/or digital signal processing (DSP). The emergence of large mixed-signal IC markets such as communications, improvement in mixed-signal design tools, and the growing presence of mixed-signal ICs in consumer and automotive products suggests that the mixed-signal arena will become more hotly contested in the future. Despite all of these competitive pressures, the mixed-signal product area offers the greatest potential for growth, for penetration into relatively closed markets, and for high-margin products with average selling prices.

Regional Market Penetration

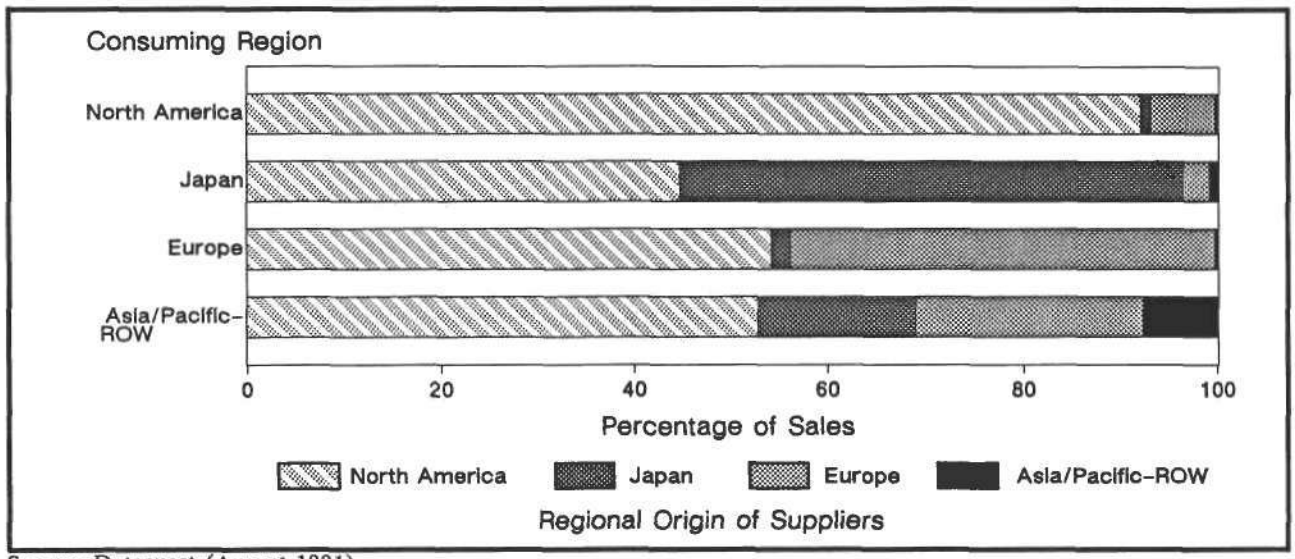
Figures 2 and 3 show the relative size of the regional IC consumption and production but do not indicate where the ICs consumed in any given

FIGURE 2
Mixed-Signal ICs—Regional Consumption/Production



Source: Dataquest (August 1991)

FIGURE 3
Linear ICs—Regional Consumption/Production



Source: Dataquest (August 1991)

region originate. Figures 4 and 5 provide a means of understanding the mix of regional suppliers to each consuming region. Each horizontal bar represents 100 percent of a region's IC consumption. The percentage supplied by the regional vendors is shown as a proportional part of the stacked bar. Figure 4 shows that the North American mixed-signal IC market is largely supplied by North American vendors. In addition, North American vendors have a more than 40 percent share of the Japanese, European, and Asia/Pacific-Rest of World (ROW) markets. Figure 5 shows that the regional pattern of consumption for linear ICs is less dominated by supply from a single region. These mature linear products are relatively well supplied by vendors within each geographic region and represent a less attractive growth market for companies outside of each region.

Figures 4 and 5 emphasize the significant North American dominance in mixed-signal ICs as well as highlighting the relative worldwide opportunity offered by mixed-signal ICs compared with linear ICs. Mixed-signal application-specific ICs represent the easiest way to penetrate foreign markets. Mixed-signal IC consumption in Japan and the Far East, although currently relatively small compared with the North American market, will experience equal, if not greater, growth in coming years.

The fact that Japanese mixed-signal IC production lags their mixed-signal IC consumption has provided an opportunity for non-Japanese suppliers to gain some share of the Japanese market. Digital-audio, computer graphics, and disk-drive support ICs have allowed North American mixed-signal suppliers to enter this marketplace. The mixing of analog/digital functions and analog/digital processing technologies has long been a technical strength of North American companies. This strength will be important for minimizing any further decline of North American suppliers in the worldwide market.

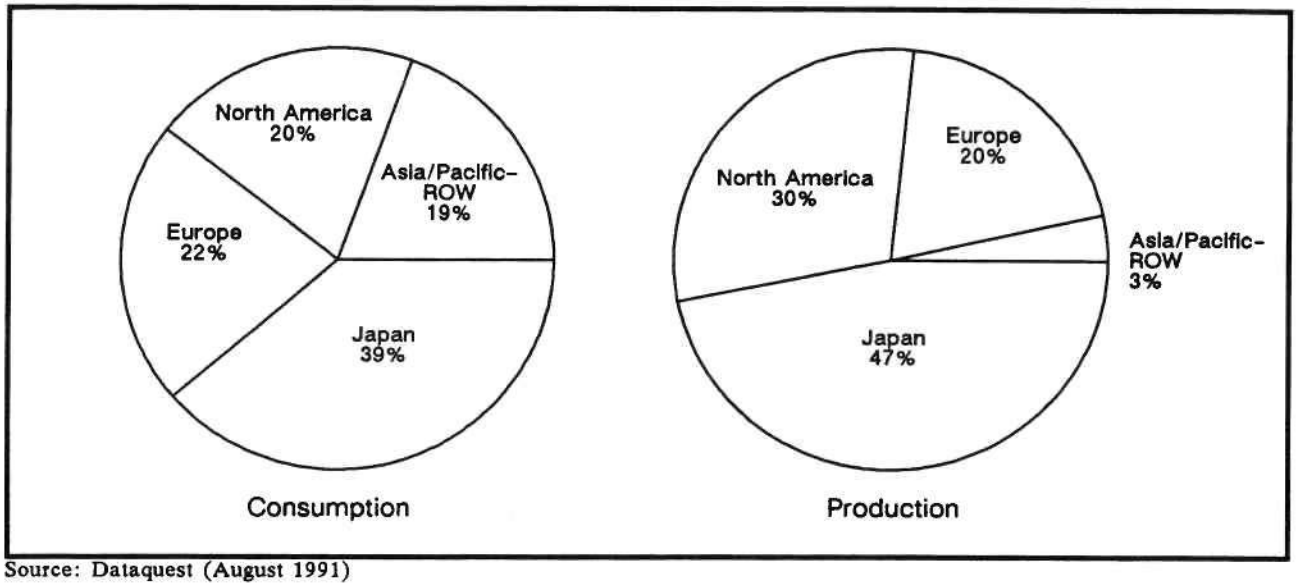
TOP SUPPLIERS BY REGION

The major mixed-signal IC suppliers to each consuming region are listed in Table 3. The more parochial listing of the top linear IC suppliers is shown in Table 4.

DATAQUEST CONCLUSIONS AND RECOMMENDATIONS

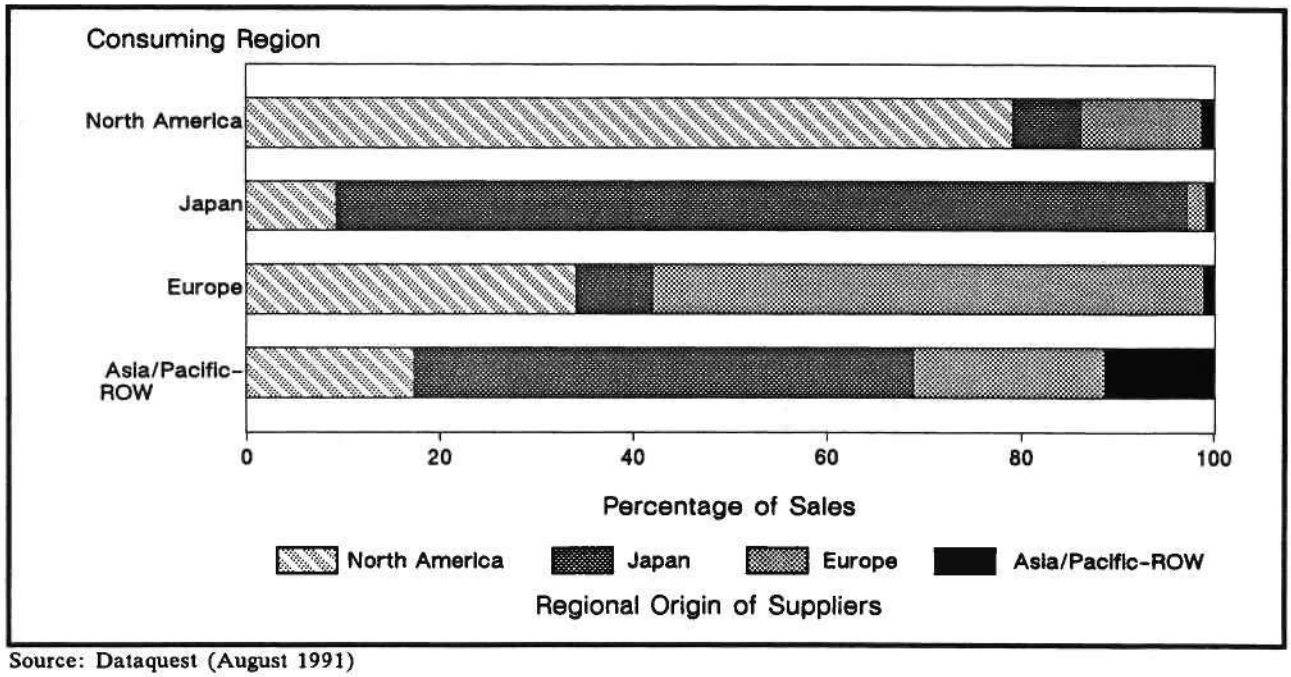
North American suppliers currently have the edge in one of the fastest-growing pieces of the semiconductor marketplace. Dataquest has forecast mixed-signal ICs to have a 16.7 percent compound annual growth rate (CAGR) from 1990 through 1995, which is considerably higher than the 9.6 percent CAGR expected for linear ICs. Mixed-signal ICs are moving into consumer and

FIGURE 4
Mixed-Signal ICs—Regional Share by Supplier Origin



Source: Dataquest (August 1991)

FIGURE 5
Linear ICs—Regional Share by Supplier Origin



Source: Dataquest (August 1991)

TABLE 3
Mixed-Signal ICs—Top Five Suppliers to Each Geographic Region

	Geographic Region			
Rank	North America	Japan	Europe	Asia/Pacific-ROW
1	Analog Devices	Rockwell	SGS-Thomson	Silicon Systems
2	National Semiconductor	Texas Instruments	National Semiconductor	SGS-Thomson
3	AT&T	Sony	Mietec	National Semiconductor
4	Texas Instruments	Fujitsu	Analog Devices	Motorola
5	Harris Semiconductor	Matsushita	Texas Instruments	GEC Plessey

Source: Dataquest (August 1991)

TABLE 4
Linear ICs—Top Five Suppliers to Each Geographic Region

	Geographic Region			
Rank	North America	Japan	Europe	Asia/Pacific-ROW
1	National Semiconductor	Matsushita	Philips	Toshiba
2	Motorola	Toshiba	SGS-Thomson	Sanyo
3	Texas Instruments	Sanyo	Siemens	Philips
4	Harris Semiconductor	NEC	National Semiconductor	Samsung
5	Philips	Mitsubishi	Motorola	Matsushita

Source: Dataquest (August 1991)

automotive products, displacing the traditional linear bipolar blocks that have characterized these markets for so long. Innovative mixed-signal ICs such as those originated by Burr-Brown (audio DACs), Brooktree (palette DACs), and PMI/Analog Devices (Pro-logic Sensurround IC) have been able to penetrate the difficult Japanese market. The movement to mixed-signal IC solutions has been difficult because of the problems of analog design capability, the availability of CAD/CAE tools, product definition, testing, and performance trade-offs. Although offering a considerable barrier to the mixed-signal market, these problems represent an avenue for engineering-oriented niche suppliers to tap into a rapidly growing IC market with international opportunities.

Gary Grandbois

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Dataquest Perspective

Analog ICs *Worldwide*

Vol. 1, No. 2 **December 9, 1991**

Market Analysis

Company Analysis

Market Analysis

Mixed-Signal and Linear ICs—1990 Market Review

Mixed-Signal ICs—A Definition

Mixed-signal ICs carry information in both digital (numeric) and analog (signal processing or power control) formats. An IC has the quality of being a mixed-signal device if it has both an analog I/O pin and a digital I/O pin. This definition is not based on the comparative size of analog-to-digital functions, nor of relative chip area. It is essentially an external, pin-based definition. ICs that are mainly digital but have some nominal analog housekeeping functions such as voltage monitors, power-on reset, or clock oscillators are not considered to be mixed-signal because there is no analog signal being received or sent to another component.

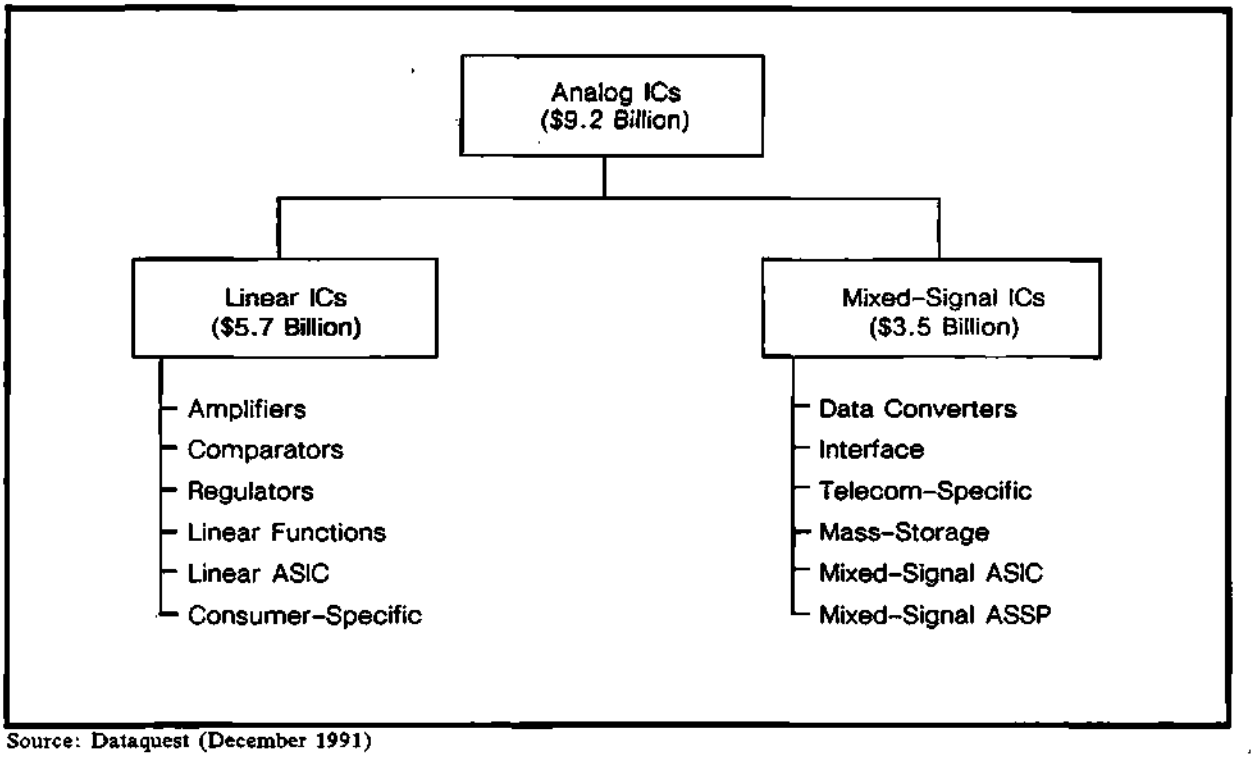
The following ICs are considered to be inherently mixed-signal:

- Data converters (analog-to-digital and digital-to-analog converters)
- Analog switches and multiplexers
- Voltage-to-frequency converters
- Sample and hold ICs
- Interface ICs
- Line driver/receiver ICs
- Codecs
- Modems
- Telecommunications-specific ICs
- Analog/digital application-specific ICs (ASICs)

Mixed-Signal versus Linear ICs

Both mixed analog/digital and linear ICs are included in the analog IC category (see Figure 1). Although not always completely clear-cut, general categories can be assigned to the mixed-signal or linear IC divisions.

Figure 1
Analog Product Family



Source: Dataquest (December 1991)

Mixed-signal IC categories include data converters, interface ICs, mass-storage ICs, telecommunications-specific ICs, and mixed-signal ASICs. Linear ICs, which are completely analog in nature, include the standard linear functions such as amplifiers, comparators, regulators, and special-functions ICs as well as the very large consumer-specific IC category.

1990 Mixed-Signal ICs Market

The year 1990 continued the strong growth for mixed analog/digital ICs. The three major growth categories were telecommunications ICs, mass storage support ICs, and mixed-signal ASICs; their respective growth rates were 18, 29, and 39 percent. Data converters showed 12.5 percent growth over 1989, weaker than the historical compound annual growth rate (CAGR), but still relatively good considering the generally weak growth for all ICs in 1990.

The proportional representation of the various mixed-signal product categories also changed in 1990. Telecommunications ICs represent the dominant product category at 32 percent of the total mixed-signal revenue, the venerable data converter category declining to 25 percent of the total. Figure 2 shows the historical growth trend of both mixed-signal and linear ICs. Linear IC revenue in 1990 grew by 11.5 percent, showing a strong recovery from the revenue decline of 1989.

Segmentation by Product Type

Figure 3 further breaks down the linear and mixed-signal IC segments into product categories.

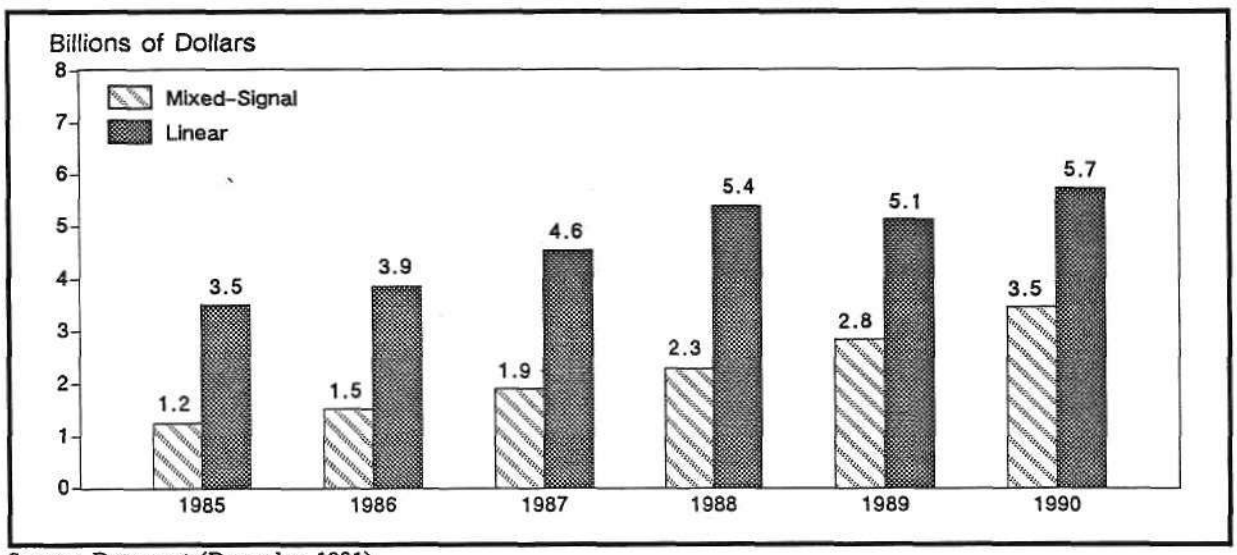
The product segmentation is further defined in Tables 1 and 2, which show revenue by product category and growth from 1989 to 1990. The largest segment of the mixed-signal revenue comes from telecommunications ICs. Data converters have held onto a sizable portion of the total and are expected to contribute one-fourth of the revenue for the foreseeable future, even though many data converters are being integrated into more application-specific ICs.

The net effect is that the general-purpose interface ICs are giving way to the application-specific standard products and ASICs that incorporate the interface function with higher levels of digital logic.

Interface ICs present a problem product segment for mixed-signal IC growth. This product family, made up as it is of peripheral drivers and line drivers, suffers from apparent low growth that can be attributed to three problems, as follows:

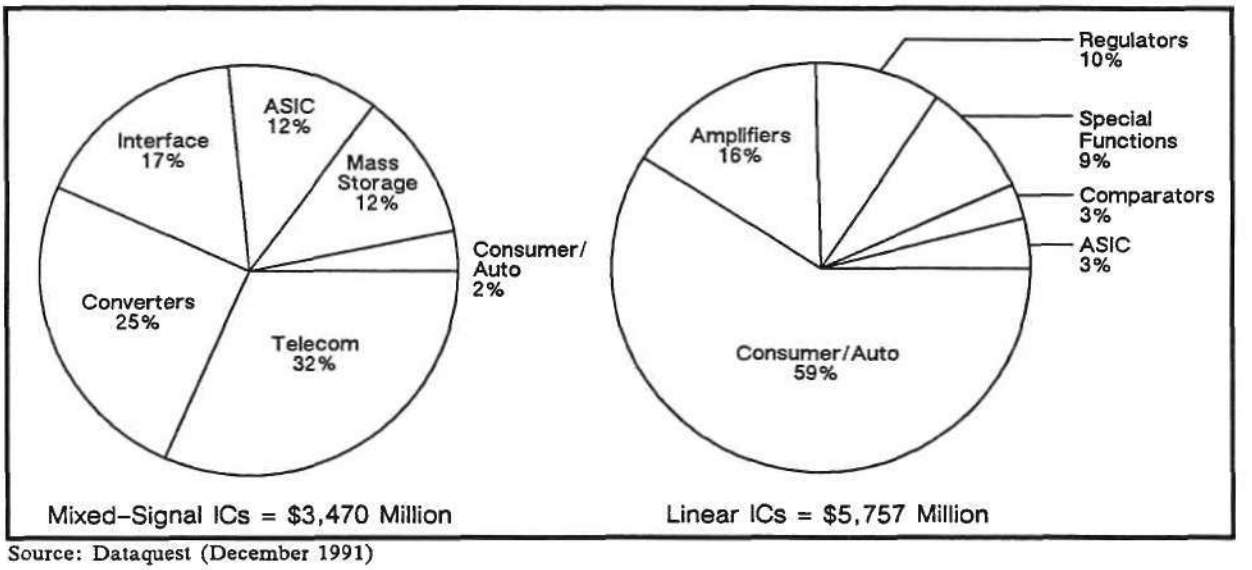
- Integration to more market or application-specific ICs

Figure 2
Mixed-Signal and Linear IC Revenue, by Year



Source: Dataquest (December 1991)

Figure 3
Mixed-Signal and Linear IC Revenue, by Product



Source: Dataquest (December 1991)

Table 1
1990 Mixed-Signal IC Revenue, by Product Category

	Revenue ($M)	Percent of Mixed-Signal	1989/1990 Growth (%)	CAGR (%) 1986-1990
Telecom-Specific ICs	1,122	32.3	18.0	31
Data Converters	875	25.2	12.5	17
Interface ICs	601	17.3	-1.3	4
Mixed-Signal ASICs	431	12.4	29.0	44
Mass Storage and Others	441	12.7	39.1	66
Mixed-Signal Total	3,470	100.0	22.2	28

Source: Dataquest (December 1991)

Table 2
1990 Linear IC Revenue, by Product Category

	Revenue ($M)	Percent of Linear	1989/1990 Growth (%)	CAGR (%) 1986-1990
Amplifiers	931	16.2	3.4	7
Comparators	154	2.7	-2.5	4
Voltage Regulators	592	10.3	6.1	16
Special Functions	523	9.1	20.5	8
Analog ASICs	185	3.2	18.0	28
Consumer Specific	3,352	58.4	13.7	11
Linear Total	5,737	100.0	11.5	10

Source: Dataquest (December 1991)

- Price erosion because of many commodity interface blocks
- Frequent assignment to other categories

The net effect is that the general-purpose interface ICs are giving way to the application-specific standard products and ASICs that incorporate the interface function with higher levels of digital logic. This change in product categories helps grow other categories of mixed-signal products, but at the expense of the interface category.

The linear IC story (see Table 2) differs considerably from that of mixed-signal ICs. In this case, the product family is dominated, both in magnitude and growth, by the consumer-specific IC market. The other categories are largely functional linear blocks subject to a double whammy: integration into higher-level functions and severe price erosion. The notable exception is the voltage regulator, a basic functional block that is needed to power all electronics, and for which integration into the general signal processing or control ICs simply does not make sense.

Process Technology

CMOS and merged bipolar-CMOS processed mixed-signal ICs show a very healthy 62 percent of the total (see Table 3). Bipolar processed ICs, while offering high levels of analog performance and drive capability, are limited in the amount of digital logic they can incorporate. As mixed-signal ICs become more application-specific and more digitally complex, bipolar ICs must necessarily give way to CMOS and BiCMOS products.

Table 3
1990 Worldwide Mixed-Signal ICs, by Technology

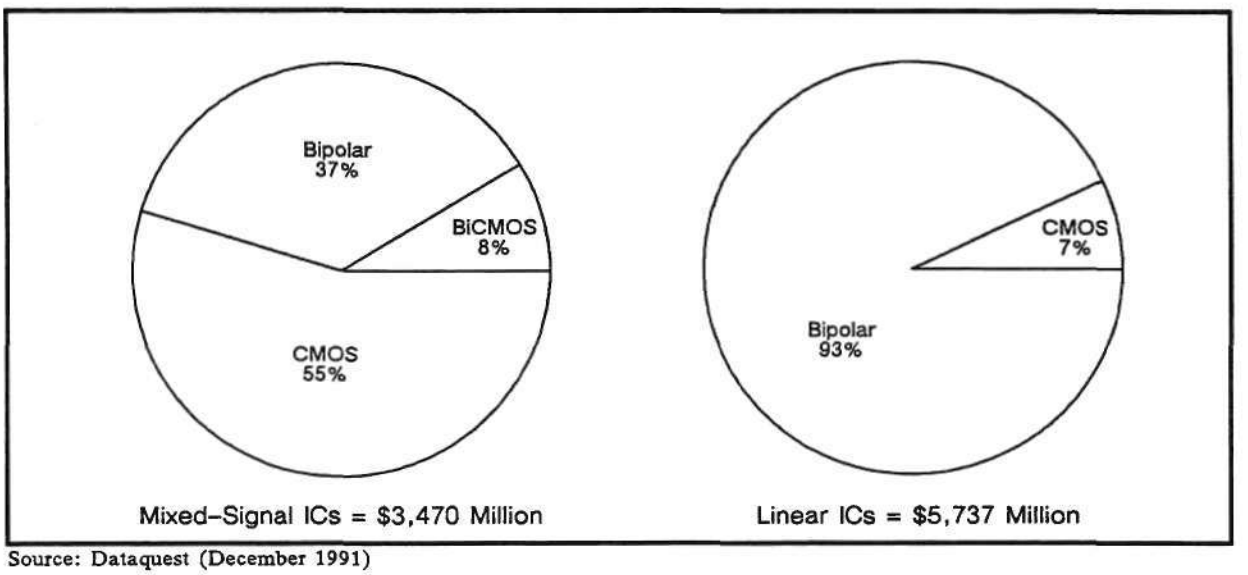
Technology	Revenue ($M)	Market Share (%)
Bipolar	1,300	37.5
CMOS	1,896	54.5
BiCMOS	274	8.0
Total	3,470	100.0

Source: Dataquest (December 1991)

Although Dataquest expects growth in both CMOS and BiCMOS technologies, BiCMOS technology will be a major factor in the growth of mixed-signal ICs. BiCMOS combines the benefits of CMOS' high density and low power consumption with the superior speed, noise, and reference capabilities of the bipolar process. CMOS will remain an important general-purpose, mixed-signal process, and BiCMOS will allow mixed-signal designs to attain the higher performance levels the market consistently demands. Bipolar will remain viable in the fastest signal processing and data converter ICs.

Figure 4 contrasts process technology for mixed-signal ICs and linear ICs and shows the proportion of revenue by process.

Figure 4
1990 Revenue, by Process Technology



Source: Dataquest (December 1991)

Application Markets

Figure 5 shows the end-equipment markets that consume mixed-signal and linear ICs. At present, these two product types address significantly different markets and regions. An important change for the mixed-signal market is that mixed-signal ICs have moved out of the realm of computer and communications end products into the broad signal processing and control markets. Increased digital processing in audio, video, and other consumer products as well as the consumer-orientation of multimedia products will accelerate the movement of mixed-signal ICs into this market.

Regional Consumption

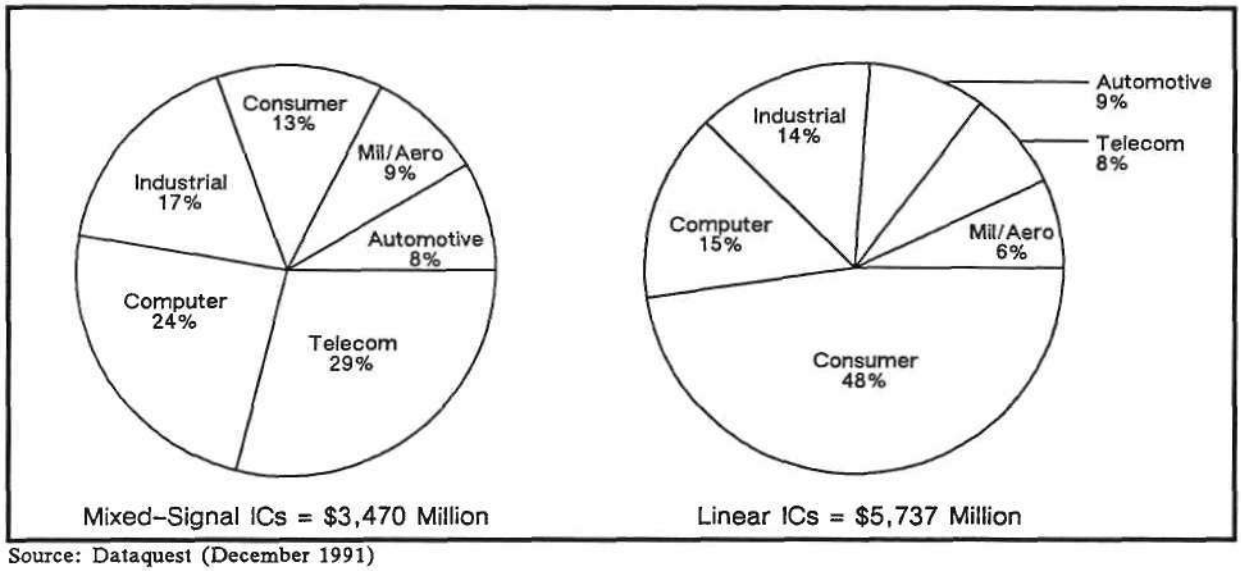
Table 4 lists the regional consumption of mixed-signal ICs by revenue and percent of total. These data are plotted in Figure 6.

Because of its strong data processing and telecommunications markets, North America is the dominant consumer of mixed-signal ICs. The Japanese market for mixed-signal ICs is growing rapidly as consumer electronics moves to combined analog/digital signal processing.

IC Growth Comparison

Table 5 compares linear, mixed-signal, and digital IC growth over the past five years. Revenue and unit shipment growth for mixed-signal ICs have both grown more than 21 percent over the past five years. Unit shipment growth for linear ICs has remained at a respectable 12.6 percent, exceeding the unit growth of digital ICs. Nonetheless, linear ICs do not show the revenue growth of digital ICs. The difference is that linear ICs have not seen the equivalent of gate or bit growth to offset the declining price per function. The result is an eroding average sales price (ASP) for linear functions and a drive to integrate into mixed-signal devices.

Figure 5
1990 Consumption, by Application Markets



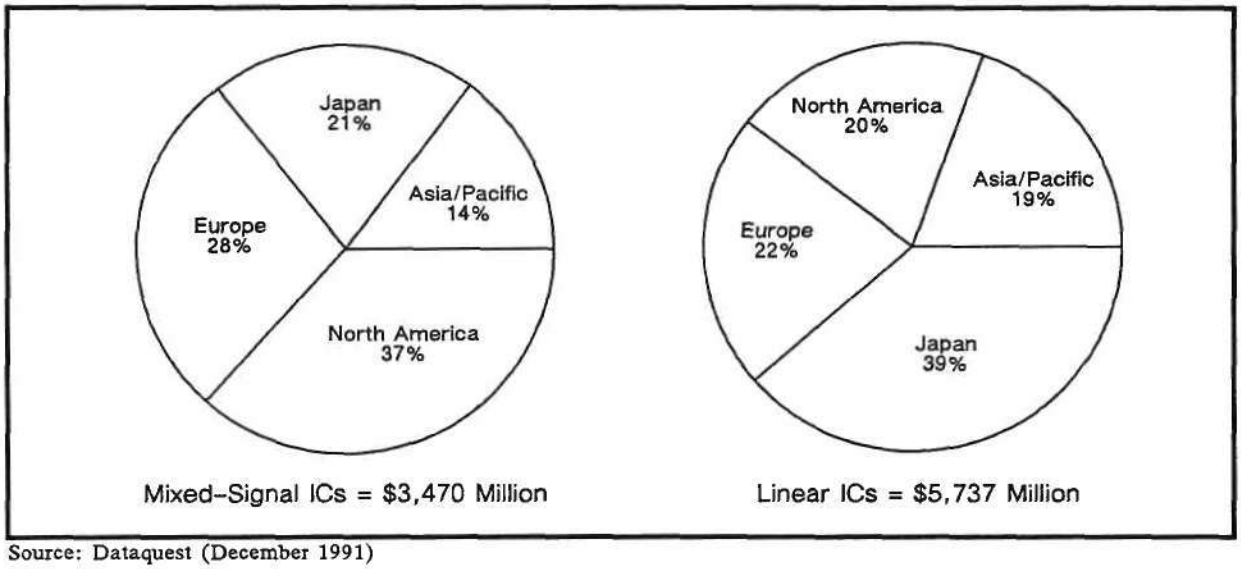
Source: Dataquest (December 1991)

Table 4
1990 Mixed-Signal and Linear IC Consumption, by Region

	Mixed-Signal ($M)	(%)	Linear ($M)	(%)
Japan	741	21.3	2,250	39.2
North America	1,281	37.0	1,123	19.6
Europe	952	27.4	1,264	22.0
Asia/Pacific	496	14.3	1,100	19.2
Total	3,470	100.0	5,738	100.0

Source: Dataquest (December 1991)

Figure 6
1990 Mixed-Signal and Linear IC Consumption, by Region



Source: Dataquest (December 1991)

Table 5
Five-Year Growth of Linear, Mixed-Signal, and Digital ICs (CAGR Percentage)

	Revenue	Units
Digital ICs	17.6	12.0
Linear ICs	9.2	2.6
Mixed-Signal ICs	22.6	21.3

Source: Dataquest (December 1991)

(Historical revenue, unit shipment, and ASP data for the period from 1985 to 1990 are presented in Tables 8 and 9 of the article entitled "Mixed-Signal IC Forecast: A Tough Market Accents the Growth Potential.")

Dataquest Perspective

The late 1980s represented the useful end of a period where systems partitioning into analog and digital ICs made sense. The drive toward smaller equipment, fewer ICs, more digital signal processing, and a higher level of voice, video, and data communication has created a growing emphasis on the mixed-signal IC. Despite a somewhat slow market for other ICs, 1990 continued to be a winning year for mixed-signal ICs. The trend is clear. Mixed-signal ICs are one of the fastest-growing categories within the semiconductor market. ■

By Gary Grandbois

Mixed-Signal IC Forecast: A Tough Market Accents the Growth Potential

Dataquest expects the worldwide mixed-signal IC market to grow from $3.47 billion in 1990 to $7.52 million in 1995. The compound annual growth rate (CAGR) from 1990 to 1995 will be 16.7 percent. By definition, mixed-signal ICs bridge the analog and digital environments and show the very strong growth rates that computers, digital signal processing (DSP), and embedded control have shown. Mixed-signal ICs are crucial to the major growth areas of the 1990s: communication, control, and multimedia.

Despite a generally slow IC market, two strong trends are driving this growth. The first is the growing trend toward digitization of electronics, which creates the need for more mixed-signal components, especially in data converters, communications interfaces, drivers, and other mixed-signal application-specific standard products (ASSPs). The second trend is the need for fewer components and more integrated, application-specific ICs (ASICs).

The analog IC proportion of the total IC units shipped has been growing substantially (see

Figure 1). Because there is no corresponding growth in analog IC revenue as a percentage of the total, the implication is clear: Digital ICs have undergone substantial functional integration over the past decade, reducing unit growth even as revenue growth has soared. We expect more than 40 percent of the ICs on the average circuit board to be analog (including mixed analog/digital ICs) in 1991, while analog revenue will remain largely unchanged at about 20 percent of the IC total. This means that the average PC board today contains a few relatively large scale digital functions surrounded by a myriad of simple analog functional ICs. This analog/digital functional discrepancy is a major driving force for the integration provided by mixed-signal ICs.

Applications: The Real Driving Force

In the 1970s, IC vendors supplied a large number of relatively simple logic and analog functions. The microprocessor as well as ASICs and the large markets for standard functions allowed digital integration to grow at a substantial pace. For a while, the artificial partitioning shown in Figure 2a was workable. It had the benefit of allowing IC suppliers to focus their technical expertise on the piece of an application that suited their design and manufacturing abilities.

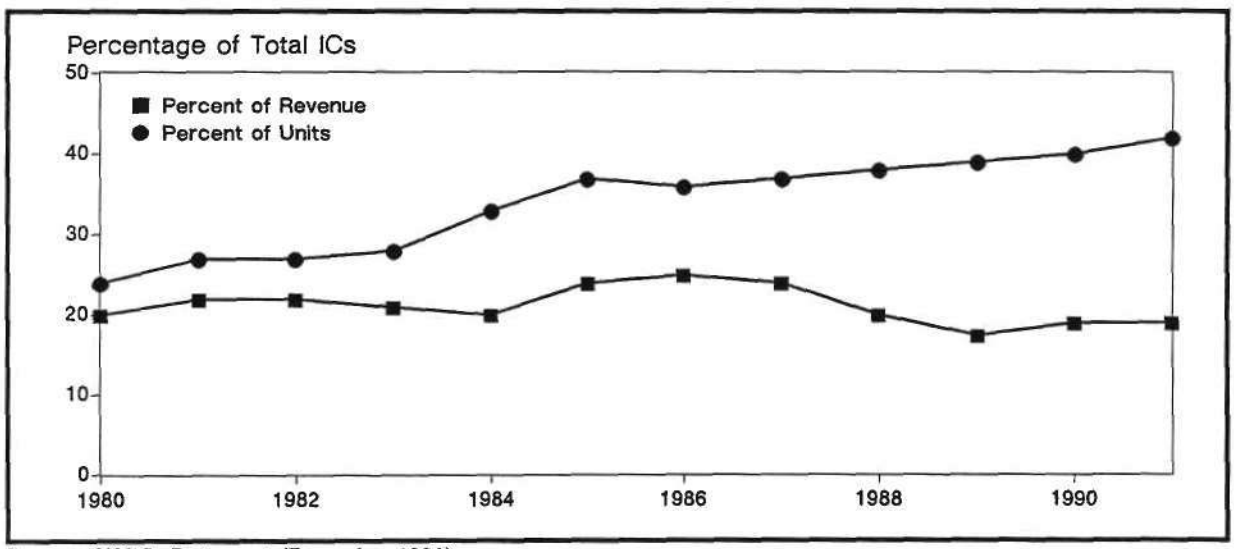
The problem is that the analog segment is very fragmented in serving a diverse range of needs, from power supply to drivers to signal processing and conversion. The mix of analog application needs had no consistent requirements and relatively small volumes because of user-specificity. In the long term, the needs of the end products will dictate that ICs be partitioned more by application subsystems (that is, motor control, amplification, audio, and video) than by whether the information is in the signal or numerical domain. The IC suppliers must focus on the end applications (see Figure 2b), which dictate a mixed-signal capability in many of the important products of the 1990s.

The movement to mixed-signal ICs, although demanded by the market, has only recently been facilitated by advances in the design, process, and test capabilities available. These still have a long way to go. In addition, new circuit techniques are developed (or old techniques revived) that make more sense in a mixed-mode environment. Delta-sigma converters are a perfect example of an old conversion technique that has moved into importance because it provides useful advantages when combined with lots of digital processing.

The Mixed-Signal IC Forecast

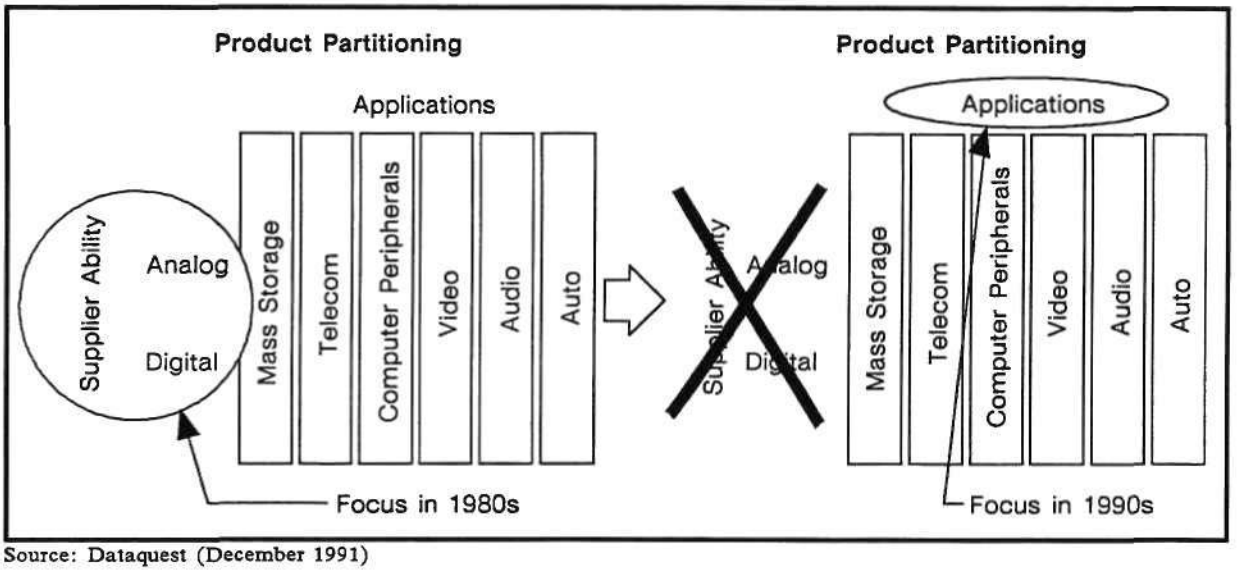
This section will discuss the mixed-signal and linear IC forecasts in parallel. Much of the growth dynamics in mixed-signal ICs involves the change from linear functions to more application-specific mixed-signal ICs. Linear ICs

Figure 1
Analog Revenue and Units, as a Percentage of Total ICs



Source: WSTS, Dataquest (December 1991)

Figure 2
Analog and Digital Partitioning



Source: Dataquest (December 1991)

and mixed-signal ICs differ in many ways, but they do address the same markets and applications. Figure 3 shows Dataquest's mixed-signal IC forecast.

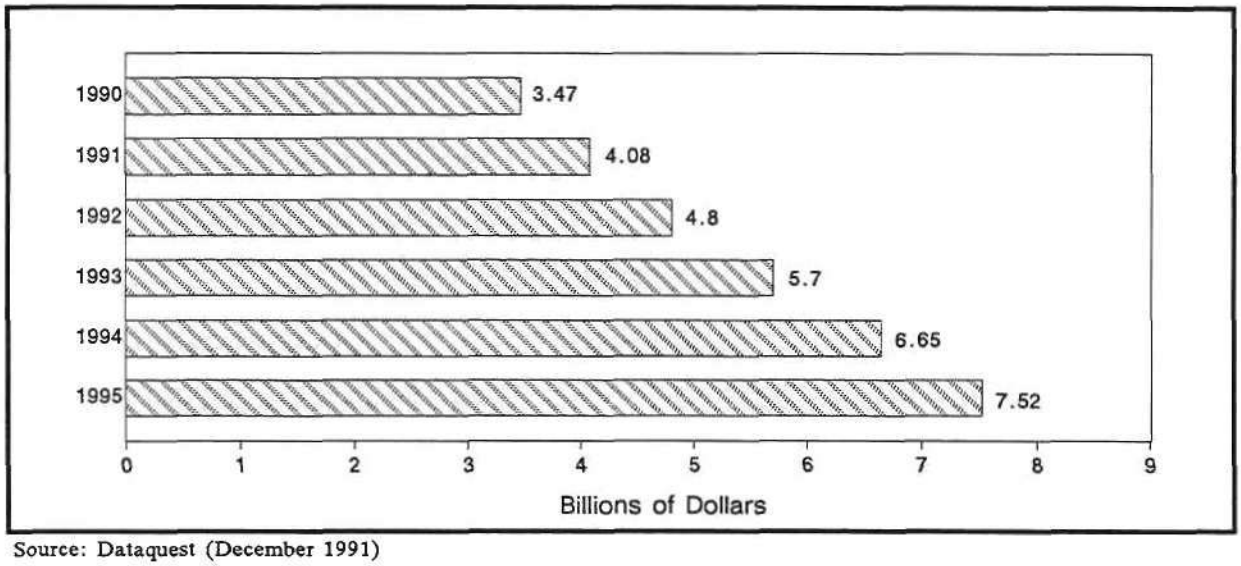
This forecast derives from the growth of both general-purpose and application-specific mixed-signal ICs.

Forecast Assumption

The forecast illustrated in Figure 3 is based on end applications and the growth of their markets. These considerations are tempered by the anticipated economic environment. Some assumptions underlying the forecast are as follows:

- The major part of the forecast IC slowdown occurred in 1989 and 1990. Although the slowdown had less impact on mixed-signal ICs than on mature product families, a stronger end-equipment market will further enhance the mixed-signal IC growth possibilities in 1992.
- The 12.5 percent CAGR forecast over the coming five-year period for all analog ICs is considerably higher than the 7.8 percent CAGR forecast for the electronic equipment market. The breakdown is for a 16.7 percent mixed-signal CAGR and a 9.6 percent linear CAGR. The linear IC content of equipment is not growing very rapidly. Most of the growth in semiconductor content is in the mixed-signal and digital IC segments.
- Mixed-signal average selling prices (ASPs) will remain relatively flat over the forecast period.
- Linear ASPs will continue to decline at a 2 percent CAGR.
- Commodity linears showed a significant ASP erosion in 1989 and 1990. ASPs for these products have stabilized, but revenue growth will not be strong over the coming five-year period. Voltage regulators remain an exception because they are needed to power all electronic systems.
- Integration into higher-level ICs will continue to stunt the growth of commodity analog blocks as analog evolves into more application-specific products.
- The IC business will see increasing mergers and alliances between digital IC companies and analog IC companies as they both recognize the need to supply system-level products that mix analog and digital functions.
- Multimedia means multisignal. Mixed-signal ICs will be basic to this market.
- Consumer electronics will start to develop an accelerating need for mixed-signal ICs as digital techniques are employed for control, for digital signal processing, and to create "smart" products.
- Despite the continued media coverage, high-definition television (HDTV) is not likely to

Figure 3
Worldwide Mixed-Signal IC Forecast, 1990-1995 (Millions of Dollars)



Source: Dataquest (December 1991)

contribute much to the growth of mixed-signal ICs over the next five years. Personal communication, data processing, and automotive needs will be far more significant.

- Mixed-signal ICs enable DSP in audio and video as well as embedded control. Consequently, they will realize equivalent growth rates.
- Pressure for higher performance or more highly integrated mixed-signal ICs will result in new products with higher ASPs. Growing sales of these newer products will offset the price decreases that will always occur in the maturing products.
- Data converters will show tremendous growth over the coming five-year period. Although a great deal of this growth will be due to converters integrated onto ASSPs and ASICs, general-purpose data converters will still experience strong growth over the next five years. This growth will be spurred by the expanding use of DSP in many product areas, including entertainment, and because of the growing need for sense and control in smart products.
- Hard disk drive support ICs will continue to grow, but not at the 29 percent growth rate seen in 1990. The rapid growth will subside into a more modest 13.4 percent CAGR.
- North American domination in the production and consumption of mixed-signal ICs cannot continue over the long term. As the consumer products and near-consumer products (cellular phones and computers) increase their content of mixed-signal ICs, the Japanese and Asia/Pacific regions will show strong growth in consumption.
- Continued confusion in the proper categorization of these complex mixed-signal ASSPs and ASICs will result in many mixed-signal ICs being reported in digital logic categories. It is likely that the actual mixed-signal revenue and growth rates will be understated in the next few years.

Linear/Mixed versus Total IC Market

Table 1 compares the linear IC and mixed-signal IC forecasts, as well as the total analog and combined analog and digital (total IC) forecasts. This table shows how the mixed-signal segment will increase not only as a percentage of the analog market but also as a percentage of the total IC market (including digital). Linear ICs, however, will slip as a percentage of the total IC picture.

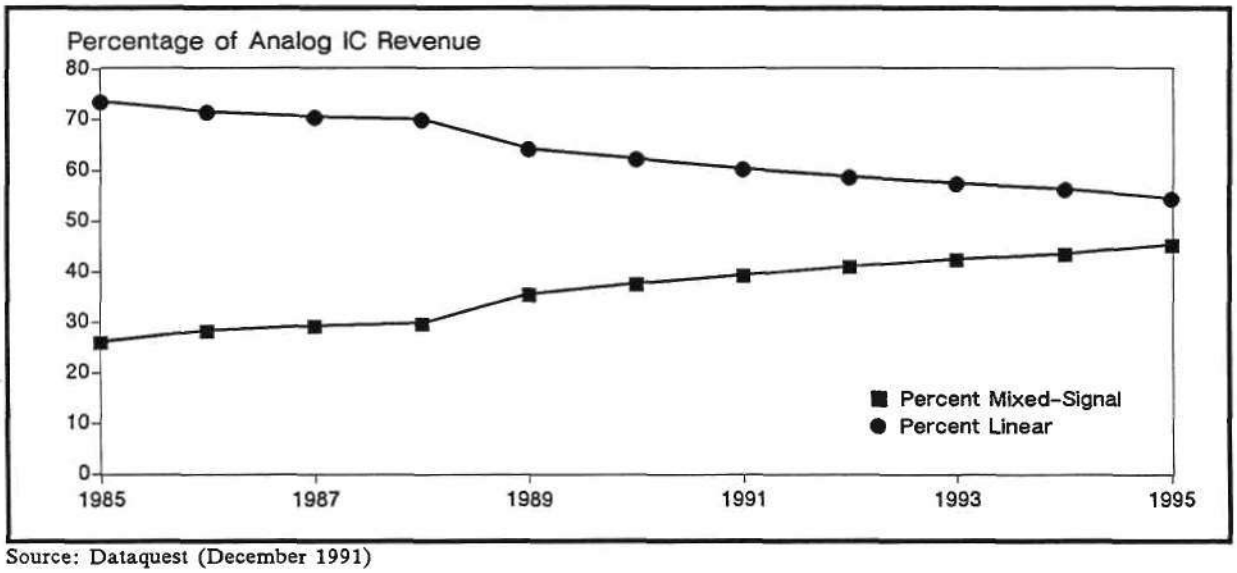
Linear ICs are slipping as a percentage of the total IC revenue as well as a proportion of analog. The forecast assumes about a 2 percent change per year in the proportion of analog IC revenue (a 2 percent per year decline for linear and a 2 percent per year gain for mixed-signal) (see Figure 4).

Table 1
Mixed-Signal, Linear, and Analog IC Forecasts Compared

Product Type	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-1995
Total IC Revenue ($M)	47,220	52,377	58,214	64,820	72,297	80,761	11.4
Analog Revenue ($M)	9,208	10,332	11,665	13,425	15,235	16,560	12.5
% of Total ICs	19.5	19.7	20.0	20.7	21.1	20.5	
Mixed-Signal Revenue ($M)	3,471	4,080	4,800	5,700	6,645	7,520	16.7
% of Total ICs	7.4	7.8	8.2	8.8	9.2	9.3	
Linear Revenue ($M)	5,737	6,252	6,865	7,725	8,590	9,040	9.6
% of Total ICs	12.1	11.9	11.8	11.9	11.9	11.2	

Source: Dataquest (December 1991)

Figure 4
Total Analog Revenue Percentages



Source: Dataquest (December 1991)

Forecast by Product

Dataquest's mixed-signal IC forecast consolidates the forecast of five major sectors of the mixed-signal market: data converters, mass storage ICs, interface, mixed-signal ASICs, and telecommunications ICs. Small portions of the consumer and automotive-specific IC categories can be considered mixed-signal and are expected to grow at a prodigious rate. Table 2 shows the contributions of each of these categories to the forecast.

Figure 5 shows the change of the product proportions over the five years covered by this forecast. Note that the consumer/automotive specific products, as well as ASICs and data converters, show the largest growth. The data converter category at this time includes a number of application-specific converters such as palette digital-to-analog converters, digital audio converters, and video analog-to-digital converters. General-purpose converters are not expected to grow as strongly as the application-specific products.

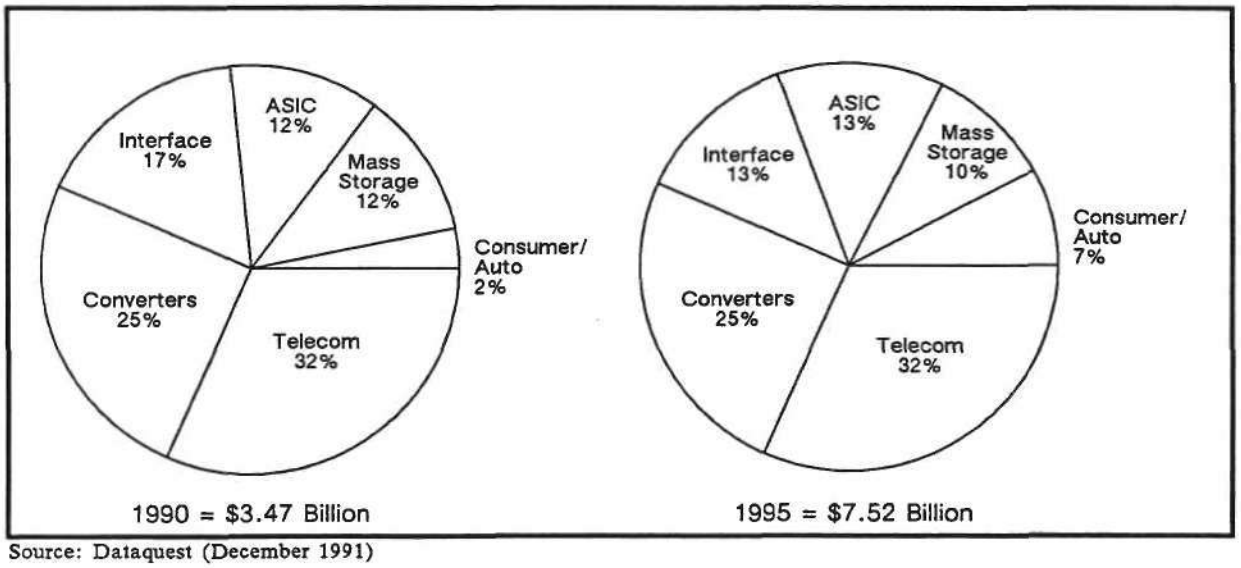
The mixed-signal forecast shows double-digit growth in every category, a strong contrast with the linear IC forecast of Table 3, which shows that single-digit growth is expected for most categories. A notable exception is the voltage regulator product, which experiences strong growth as the power management block fundamental to all electronics.

Table 2
Mixed-Signal IC Forecast, by Product, 1990-1995 (Millions of Dollars)

Product Type	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-1995
Mass Storage*	382	441	512	584	647	714	13.4
Data Converters	875	1,057	1,240	1,470	1,700	1,900	16.8
Interface	601	680	740	820	910	1,000	10.7
ASIC*	432	476	598	750	889	1,000	18.3
Telecom	1,122	1,270	1,500	1,785	2,090	2,350	15.9
Others (Consumer, etc.)	59	156	210	291	409	556	55.6
Mixed-Mode Total	3,471	4,080	4,800	5,700	6,645	7,520	16.7

*Note: Dataquest believes that the total mixed-signal, mass storage revenue was $442 million in 1990; $60 million was reported in the ASIC category.
Source: Dataquest (December 1991)

Figure 5
Mixed-Signal IC Product Forecast, 1990 and 1995



Source: Dataquest (December 1991)

Technology Forecast

Dataquest expects CMOS processing to dominate in mixed-signal ICs, but to give ground to BiCMOS technology. BiCMOS will be the preferred way to target the high-performance signal processing market. BiCMOS offers the ability to mix the superiority of bipolar linear functions (amplifiers, comparators, and references) with CMOS analog switches and logic, an ideal combination for higher levels of integration and performance in converters. BiCMOS also offers advantages in high-speed interface drivers.

Processes that optimize digital CMOS can still provide high-speed bipolar drive capabilities. Both linear and digitally optimized BiCMOS will make inroads in the mixed-signal market. Figure 6 shows Dataquest's technology forecast for mixed-signal ICs in 1995. For comparison, 1990 showed respective mixed-signal process segmentation of 37, 55, and 8 percent for bipolar, CMOS, and BiCMOS processing. The movement into MOS processes from bipolar is expected to increase considerably more quickly in mixed-signal IC—where we expect to see a 10 percent decline in bipolar in five years—than in the linear ICs, where CMOS is used only for very specialized applications.

Regional Consumption Forecast

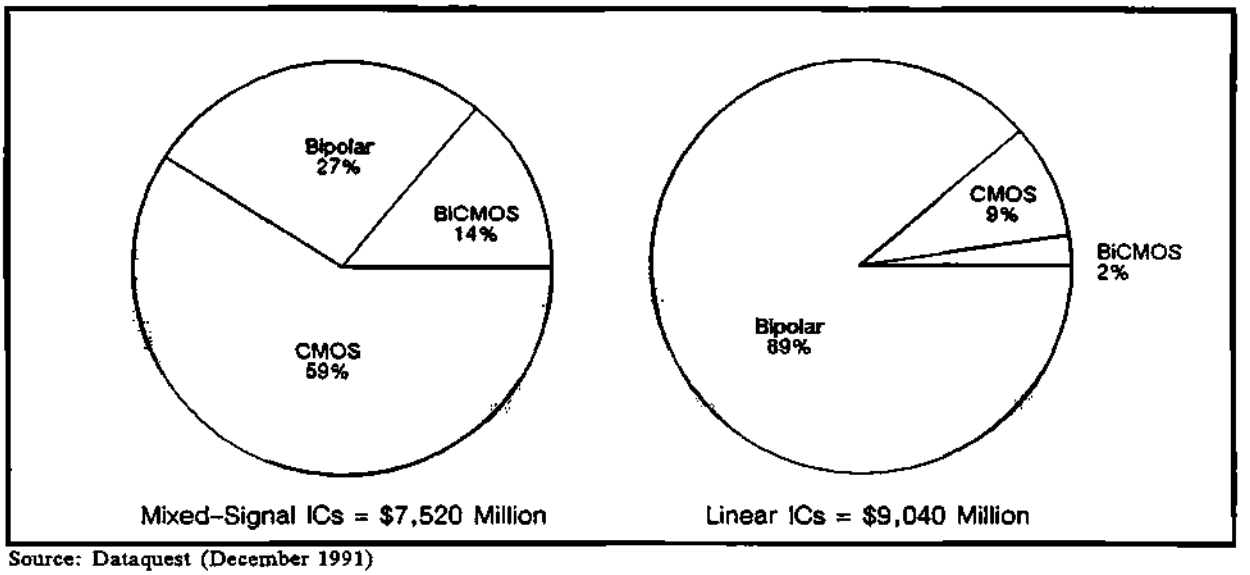
Tables 4 and 5 give the forecasts by region for both mixed-signal and linear ICs. The biggest

Table 3
Linear IC Forecast, by Product, 1990-1995 (Millions of Dollars)

Product Type	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-1995
Amplifiers	931	975	1,100	1,250	1,375	1,480	9.7
Comparators	154	160	165	170	170	170	2.0
Voltage Regulators	592	677	800	980	1,100	1,160	14.4
Special Functions	523	609	708	806	893	986	13.5
Analog ASICs	185	204	232	250	251	250	6.2
Consumer/Auto Spec.	3,352	3,627	3,860	4,269	4,801	4,994	8.4
Linear IC Total	5,737	6,252	6,865	7,725	8,590	9,040	9.6

Source: Dataquest (December 1991)

Figure 6
Forecast 1995 Revenue, by Technology (Millions of Dollars)



Source: Dataquest (December 1991)

Table 4
Forecast Mixed-Signal IC Revenue, by Region (Millions of Dollars)

	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-1995
North America	1,281	1,444	1,664	1,955	2,264	2,550	14.8
Japan	741	954	1,185	1,400	1,600	1,790	19.3
Europe	952	1,062	1,170	1,370	1,570	1,808	13.7
Asia/Pacific	496	618	782	975	1,211	1,372	22.5
Total	3,470	4,100	4,800	5,700	6,645	7,520	16.8

Source: Dataquest (December 1991)

growth contrast is seen in Japan, where the mixed-signal forecast is very strong and linear is weak. It is important to realize that a small percentage increase of mixed-signal ICs into the consumer market will show up as very substantial growth. In addition, the use of mixed-signal ICs will increase in communications and computer markets within Japan. The linear IC forecast of 6.1 percent CAGR in Japan is below the expected growth of linear ICs in the consumer market. This results from a movement of equipment manufacturing away from Japan and into the Asia/Pacific region.

The growth for both linear and mixed-signal ICs in the Asia/Pacific region is expected to be strong (16 percent and 22.5 percent, respectively). The movement of consumer product manufacturing has a great deal to do with these high growth rates. Mixed-signal ICs benefit from the newer equipment designs.

Market Forecast

Part of the impetus for the changing regional consumption is because of the change in the end applications of mixed-signal ICs. Figure 7 shows that Dataquest expects the consumer, communications, and computer markets to substantially increase consumption of mixed-signal ICs. The consumer market is a strong driver for the growth in consumption in Japan and the Asia/Pacific regions.

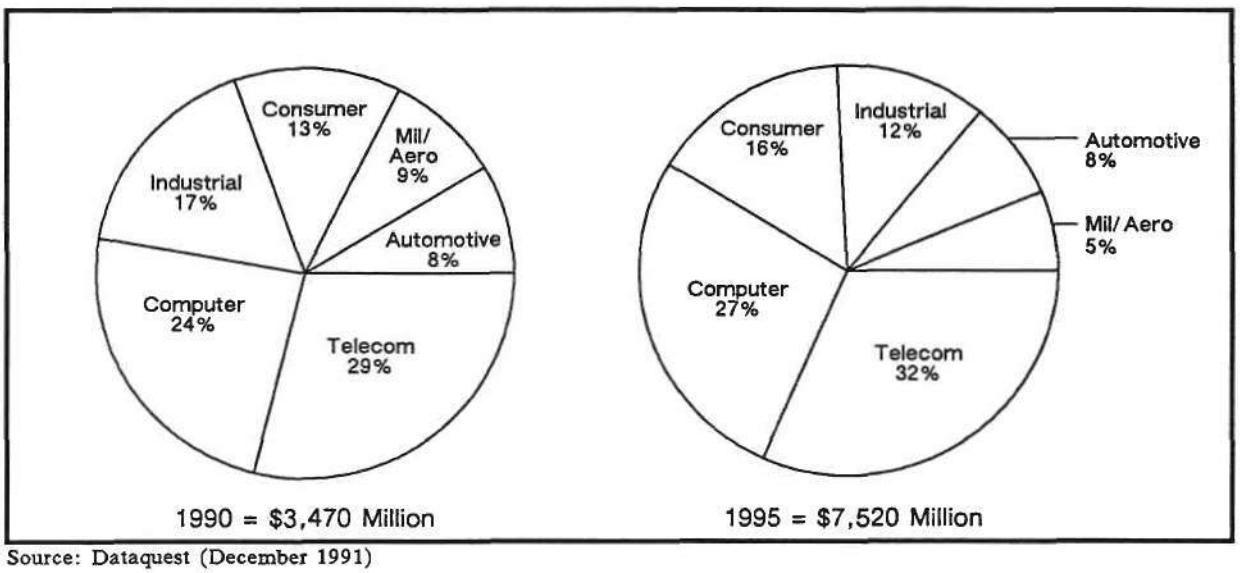
The forecast data behind the change shown in Figure 7 are listed in Table 6. The communications market dominated the mixed-signal market in 1990 and will continue that market dominance over the forecast period. The size of the consumer market makes it the greatest opportunity for mixed-signal IC growth, especially as DSP becomes more firmly entrenched in audio and video consumer products.

Table 5
Forecast Linear IC Revenue, by Region (Millions of Dollars)

	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-1995
North America	1,160	1,252	1,400	1,558	1,660	1,721	8.2
Japan	2,252	2,434	2,533	2,755	2,988	3,033	6.1
Europe	1,231	1,350	1,468	1,634	1,827	1,890	9.0
Asia/Pacific	1,094	1,216	1,464	1,778	2,115	2,396	16.0
Total	5,737	6,232	6,865	7,725	8,590	9,040	9.5

Source: Dataquest (December 1991)

Figure 7
Mixed-Signal IC Market Forecast, 1990 and 1995



Source: Dataquest (December 1991)

Table 6
Mixed-Signal IC Revenue Forecast, by End Market (Millions of Dollars)

End Market	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-1995
Industrial	589	620	680	755	810	900	8.9
Data Processing	820	960	1,150	1,400	1,720	2,020	19.8
Communication	1,024	1,210	1,400	1,690	2,080	2,400	18.6
Military	312	330	350	370	390	420	6.1
Consumer	445	650	835	1,025	1,130	1,200	22.0
Automotive	280	330	385	460	515	580	15.7
Total	3,470	4,100	4,800	5,700	6,645	7,520	16.8

Source: Dataquest (December 1991)

Figure 8 shows the change in the linear IC market by 1995. The consumer market dominates the linear IC consumption both in 1990 and in the future. The growing automotive market and its demand for sensors and linear signal conditioning, as well as for automotive entertainment systems, provides additional growth opportunities for linear ICs. Table 7 shows the linear forecast by market.

Mixed-Signal IC Unit and Revenue Forecast

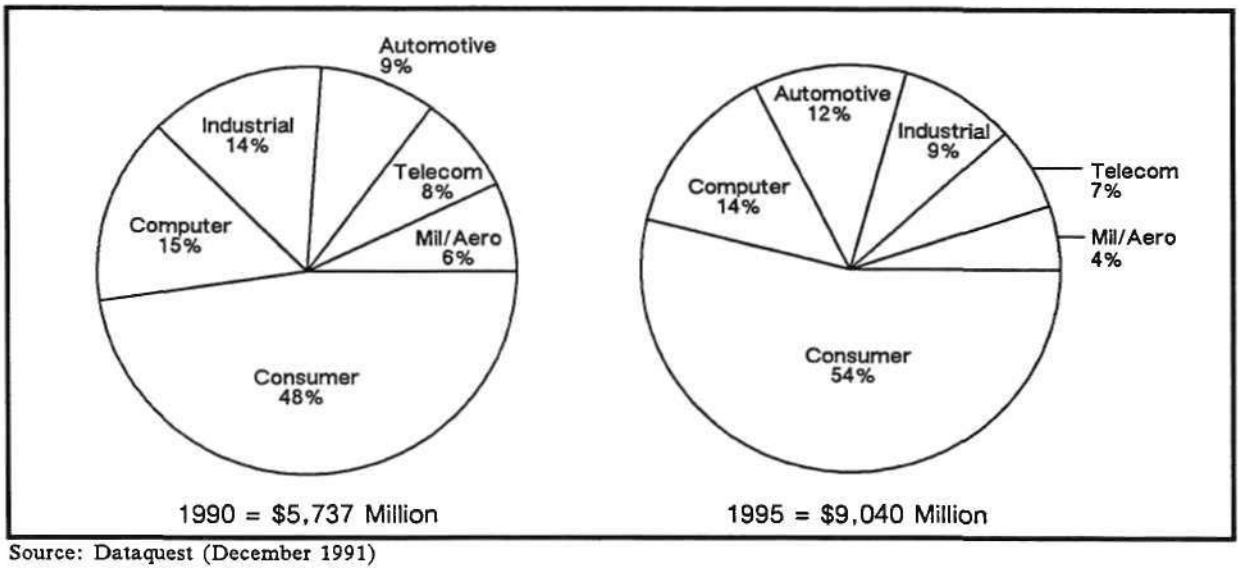
Table 8 shows the complete mixed-signal forecast for units and ASPs. Historical data from 1985 to 1990 also are provided. Dataquest's forecast compound annual revenue growth for the 1990 to 1995 period is 16.7 percent. ASPs rose slightly from 1985 to 1990 as higher-ASP mixed-signal products were introduced. We expect unit growth to remain very close to revenue growth over the 1990 to 1995 period because ASPs are expected to change little. Units and ASP are plotted by year in Figure 9.

Linear IC Units, ASP, and Revenue Growth

Table 9 expands the linear IC forecast from revenue into units and ASP. These forecast values are listed with the historical data from 1985 for comparison.

Dataquest forecasts 9.5 percent compound annual revenue growth for the linear IC segment from 1990 to 1995. Unit growth will

Figure 8
Linear IC Market Forecast, 1990 and 1995



Source: Dataquest (December 1991)

Table 7
Linear IC Revenue Forecast, by End Market (Millions of Dollars)

End Market	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-1995
Industrial	801	832	870	845	830	830	0.7
Data Processing	840	910	1,025	1,175	1,290	1,280	8.8
Communication	470	570	650	660	670	655	6.9
Military	335	280	290	330	325	330	-0.3
Consumer	2,762	3,050	3,365	3,925	4,540	4,900	12.2
Automotive	530	590	665	790	935	1,045	14.5
Total	5,737	6,232	6,865	7,725	8,590	9,040	9.5

Source: Dataquest (December 1991)

Table 8
Forecast Mixed-Signal IC Revenue, Units, and ASP

Year	Revenue ($M)	Units (M)	ASP ($)
1985	1,250	800	1.56
1986	1,520	1,030	1.48
1987	1,900	1,300	1.46
1988	2,290	1,490	1.54
1989	2,840	1,780	1.60
1990	3,470	2,100	1.65
1991	4,100	2,450	1.67
1992	4,800	2,900	1.66
1993	5,700	3,400	1.68
1994	6,645	4,000	1.66
1995	7,520	4,580	1.64
1985-1990 CAGR (%)	22.6	21.4	1.2
1990-1995 Forecast CAGR (%)	16.7	16.9	-0.1

Source: Dataquest (December 1991)

exceed revenue growth as ASPs continue to decline at a rate of about 2 percent per year. Revenue and unit growth trends are not expected to show any drastic change over the next five years. The forecast CAGR differs only slightly from that of the past five years, showing only the declining growth trends we expect for all semiconductors. Neither mixed-signal ICs nor digital ICs will eliminate the need for linear ICs in the foreseeable future. Figure 10 shows the unit shipment and ASP data for linear ICs, plotted by year.

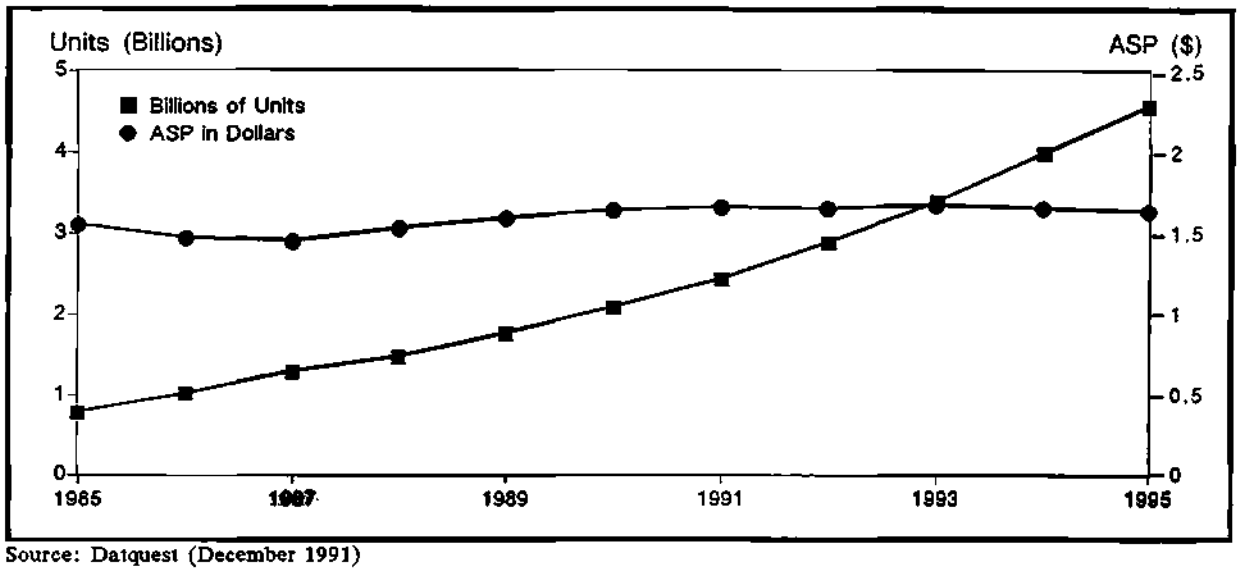
Figure 11 plots historical revenue data through 1990 and the five year forecast for both linear and mixed-signal ICs. Although both segments show growth, the mixed-signal portion is growing into one of the more substantial pieces of the IC market.

Dataquest Perspective

Forecast growth for both linear and mixed-signal ICs depends on the growth of the end markets. Unlike the "kick" to the electronic marketplace offered by such innovative products as the IC op-amp, the microprocessor, or the semiconductor memory, mixed-signal ICs are not inherently creating new applications and markets. They are merely offering the next logical step in ASICs. This is especially true as digital techniques become further employed in traditionally analog products such as consumer entertainment and communications equipment.

Another driving force is the increasing appearance of analog interfaces in data processing systems such as high-quality video and audio outputs, and pen-based, speech, or video

Figure 9
Mixed-Signal IC Forecast—ASP and Unit Shipments



Source: Dataquest (December 1991)

Table 9
Forecast Linear IC Revenue, Unit Shipments, and ASP

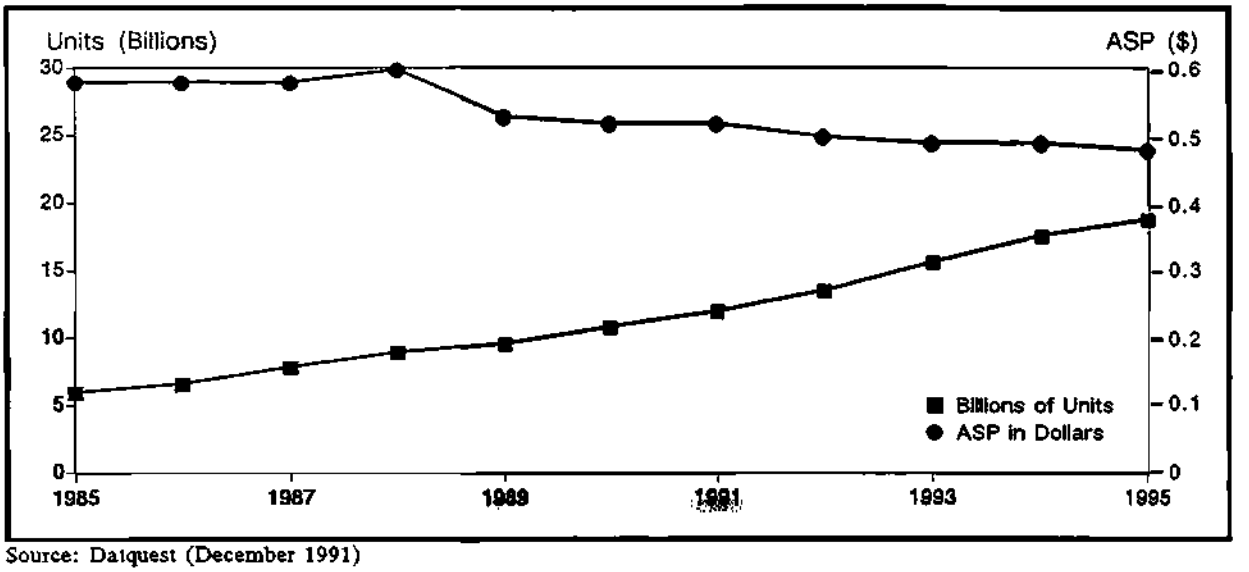
Year	Revenue ($M)	Units (M)	ASP ($)
1985	3,511	6,036	0.582
1986	3,858	6,690	0.577
1987	4,552	7,900	0.576
1988	5,385	9,010	0.598
1989	5,143	9,660	0.532
1990	5,737	10,930	0.525
1991	6,252	12,050	0.519
1992	6,865	13,600	0.505
1993	7,725	15,700	0.492
1994	8,590	17,700	0.485
1995	9,040	18,920	0.478
1985-1990 CAGR (%)	10.3	12.6	-2.0
1990-1995 Forecast CAGR (%)	9.5	11.6	-1.9

Source: Dataquest (December 1991)

inputs. Because they represent a more efficient way to define IC architectures for the supplier and a more easily used product for the end-equipment manufacturer, mixed-signal ICs will continue to show substantial growth over both linear and digital ICs in the next few years. However, there is no market that escapes the current recession. Growth in both mixed-signal and linear ICs will be reduced because of the slow end-equipment markets projected in the coming years. ■

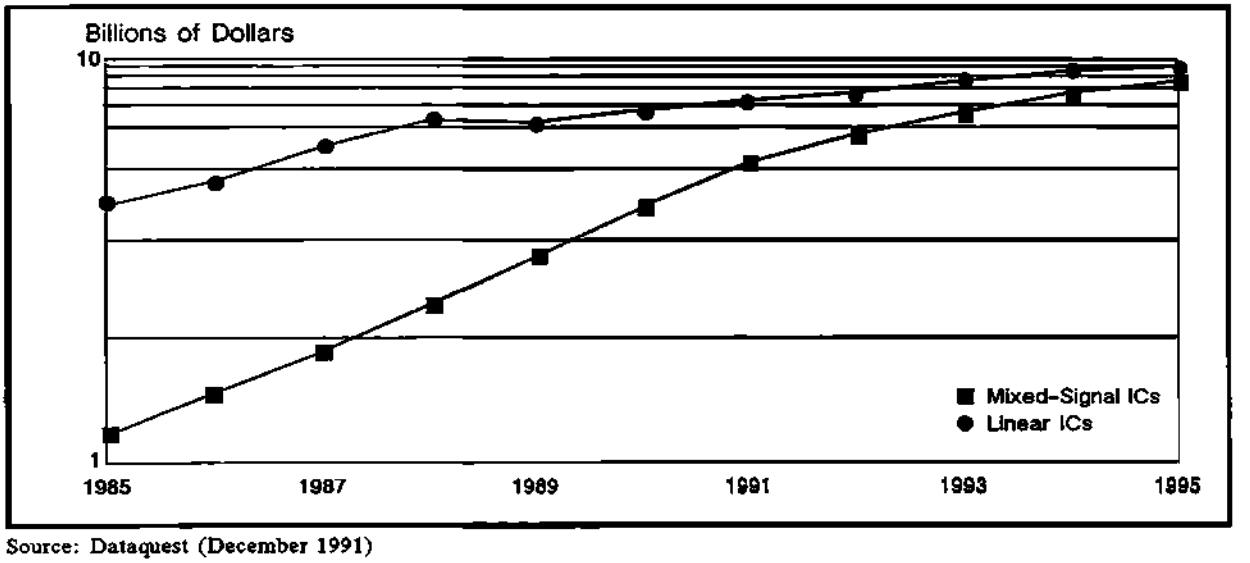
By Gary Grandbois

Figure 10
Linear IC Forecast—ASP and Unit Shipments



Source: Dataquest (December 1991)

Figure 11
Mixed-Signal and Linear IC Forecast Revenue Growth, 1985-1995



Source: Dataquest (December 1991)

Company Analysis

Cirrus Logic and Crystal Semiconductor: A Powerful Combination

Cirrus Logic Inc. and Crystal Semiconductor Corporation have signed an agreement for a merger of the two companies. Effective September 3, Crystal Semiconductor became a wholly owned subsidiary of Cirrus Logic. Crystal will remain autonomous but will work closely with Cirrus on joint projects that combine the companies' expertise.

Cirrus Logic's strength is its marketing capability and systems knowledge in the peripheral controller arena. Crystal Semiconductor's expertise is in the mixed-signal and analog arena. The coupling of Crystal and Cirrus creates a strong mixed-signal market contender for the peripheral controller functions.

The mixed-signal market is one of the fastest growing segments in the semiconductor market. The combination of analog and digital on a single chip has become the wave of the future, and more and more companies are entering the market. The combining of these technologies has also created solutions that could not have existed previously in either technology alone.

Cirrus Logic

Cirrus is known as a leading supplier of mass storage, user interface, and communications control functions for high-speed personal computer, workstation, and other office automation products. Cirrus specializes in identifying opportunities for these markets, designing solutions in a timely manner, and applying a cost-effective manufacturing structure.

Cirrus is headquartered in Fremont, California, and currently employs 530 people worldwide. The company was founded in 1985 and held its initial public offering in June 1989. Net revenue of $5 million in fiscal year ending March 31, 1987, grew to $141.8 million in fiscal 1991.

The company's stated strategy is to exploit the flexibility and power of its design automation system to serve large and emerging markets in which sophisticated architectural solutions, high performance, systems integration, and time to market are vital to customers. This strategy is the key element driving Cirrus toward its market-leader position.

Cirrus holds strong market positions in several of its targeted application markets. In the mass storage arena, Cirrus introduced PC AT-compatible Winchester disk drive control logic that established new levels of integration and is now offered by Cirrus as a one-chip solution. The VGA-compatible graphics controller, a user-interface application introduced by Cirrus, currently leads the industry in VGA controllers used for liquid crystal displays in the high-growth notebook computer market. Cirrus also applied innovative architecture in the communications market and developed a multichannel, multiprotocol datacom solution that improves overall system performance.

Currently a fabless company, Cirrus focuses its resources on designing solutions to enhance overall system performance by improving the performance of peripheral devices. Until recently, it has been successful using digital technology and adding higher levels of integration and architectural innovation to increase performance. However, the need to incorporate analog to obtain continued added performance became apparent as many of its target applications require analog functions to interface to the real world. The incorporation of analog is a powerful factor toward a continued hold on strong architecture and performance in the peripheral controller market. Acquiring Crystal Semiconductor gives Cirrus the ability to integrate the complex analog functions into next-generation controllers.

Crystal Semiconductor

Crystal Semiconductor is located in Austin, Texas, and is a supplier of advanced mixed analog/digital integrated circuits. A privately held company, Crystal's revenue was about $20 million in 1990; the company currently employs 150 people. Crystal, like Cirrus, is a fabless company. The targeted applications for its products are the communications, data acquisition, and audio markets.

Crystal's primary focus is on analog devices that incorporate enough digital circuitry to enhance the analog circuitry. Crystal has patented this technique as the SmartAnalog IC.

Crystal was an early and leading proponent of the delta-sigma data converter technique, which

offers many advantages when combined with digital circuitry on mixed-signal ICs. Because of its low cost and inherent advantages, it has been designed into voice-band digital signal processing-based products as diverse as modems, cellular phones, and consumer digital audio. Crystal's strong engineering and applications knowledge of data conversion and digital filtering provides a powerful complement to Cirrus' systems expertise in computer peripherals.

Crystal uses CMOS technology for its mixed-signal products, rather than bipolar, reducing cost, power consumption, and die size. However, for future high-end workstation markets, CMOS will not provide the necessary performance and will require the addition of BiCMOS technology.

Crystal Semiconductor participates in three key markets: communication, data acquisition, and audio. In communication, Crystal participates in the T1, T3, and ethernet LAN transceiver markets. The data acquisition area has greatly benefited from Crystal's inroads into delta-sigma technology and has been the foundation for the low-frequency analog-to-digital converters (ADCs) used in this market.

The third applications area that Crystal participates in is the audio market. Crystal and its partner Asahi Chemical are strong market participators in audio ADCs and digital-to-analog converters for compact disk, digital audio tape, special-effects processors, FM broadcast editing workstations, PC stereo audios, and other audio applications.

Dataquest Perspective

Dataquest believes that the synergy between Cirrus Logic and Crystal Semiconductor provides an excellent opportunity for a dynamic combination. Access to Crystal's mixed-signal technology enables Cirrus Logic to continue as an architecturally leading-edge company, supplying to the peripheral controller market.

Cirrus gains technology from Crystal that has already been proven as viable, and together they can work to implement the mixed-signal technology into current controller functions. Cirrus provides significant systems understanding in the computer and peripheral markets, along with strong existing market access and marketing savvy. This systems knowledge and understanding will be crucial in the years to come as the IC becomes more and more integrated and moves to single-chip system solutions.

Additional applications opportunities for the Cirrus/Crystal merger remain in the communications markets as LANs and modem chips move onto the motherboard and as other communications functions become more prevalent. Other areas of opportunity may be in the automotive and consumer arena as mixed-signal technology advantages are realized and are implemented in these markets. ■

By Anna Cahill

In Future Issues

Look for the articles on the following topics in future issues of *Dataquest Perspective*:

- An examination of data converter ICs
- First look at 1991 market shares for the analog market

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Dataquest Perspective

Analog ICs *Worldwide*

Vol. 1, No. 1 November 25, 1991

Market Analysis

1991 Bookings and Billings—How Does the Forecast Look?

Analog ICs are showing growth in 1991, but the growth is limited to certain products and regions. Although the Dataquest forecast is driven by product and market growth considerations, it is important to review that forecast against recent industry bookings and billings data. For this purpose, we will use the monthly bookings and billings data of the World Semiconductor Trade Statistics (WSTS) program.

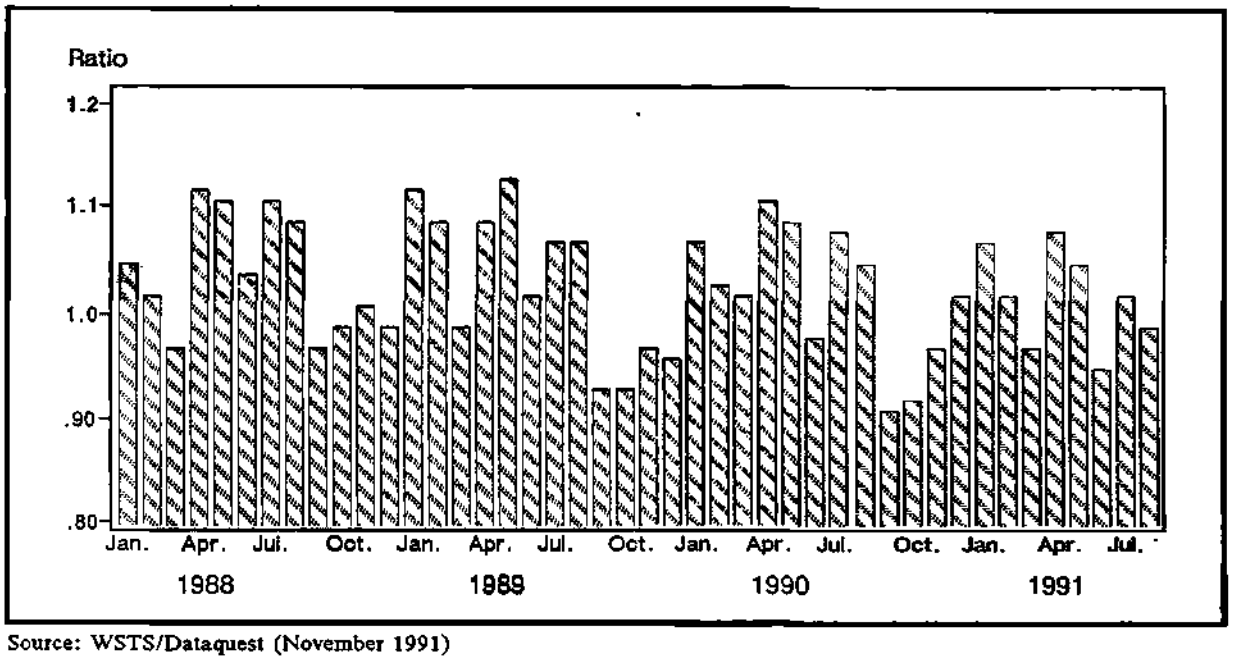
One of the most popular industry barometers is the book-to-bill ratio. Figure 1 shows three-and-a-half years of WSTS book-to-bill ratios for analog ICs. It is difficult to make any significant judgment about industry trends from these revenue ratios. The most salient points from the book-to-bill figure are that January, April, and July are always strong, whereas March, June, and September generally show weak ratios. The current year has shown no major difference from this pattern except that peaks and valleys are somewhat lower than in past years. It is quite easy to predict very low September and October book-to-bill ratios from the trend.

More can be learned from the revenue numbers for analog bookings and billings as plotted in Figure 2. It is apparent from this curve that the growth trend of 1990 has flattened in 1991. Lack of growth in billings from the first of the year does not alter the fact that 1991 is consistently higher in billings by month and will therefore show significant growth over 1990. The disturbing aspect is that the flat bookings profile implies a flat 1992. Dataquest forecasts growth of 11.4 percent in 1991 and 12.7 percent in 1992. Do these forecasts still make sense based on the trends? The answer is a cautious yes. Although we see a flattening trend, the bookings and billings are actually in a more dynamic pattern than the figure shows.

Historical Growth Pattern

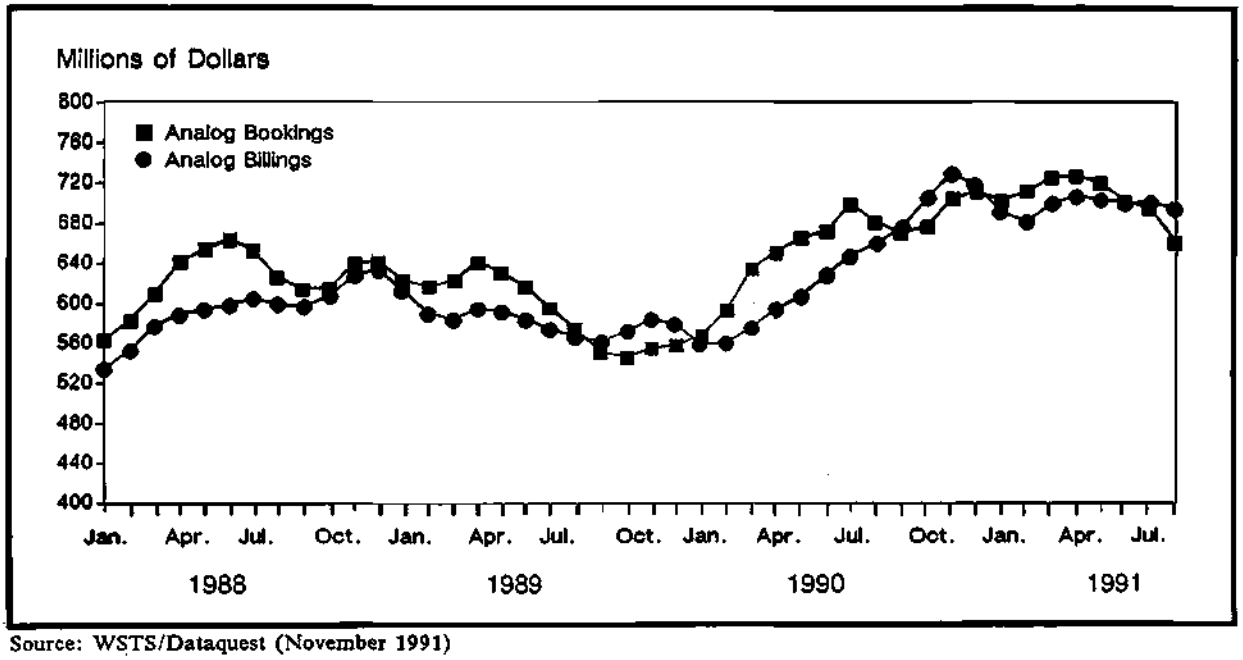
Figure 3 shows another way to look at bookings: by plotting monthly bookings growth over the same month in the previous year. This approach takes seasonality out of the numbers and makes booking trends much more obvious. Although 1988 was a very strong growth year, the booking growth trend consistently dropped for a two-year period, passing the zero point in 1989, a poor year for analog sales (about 3 percent growth over 1988). A trend toward an increasing rate of growth emerged in January 1990 and continued until January 1991, when the growth rate started slowing.

Figure 1
Analog IC Book-to-Bill Ratios, 1988-1991



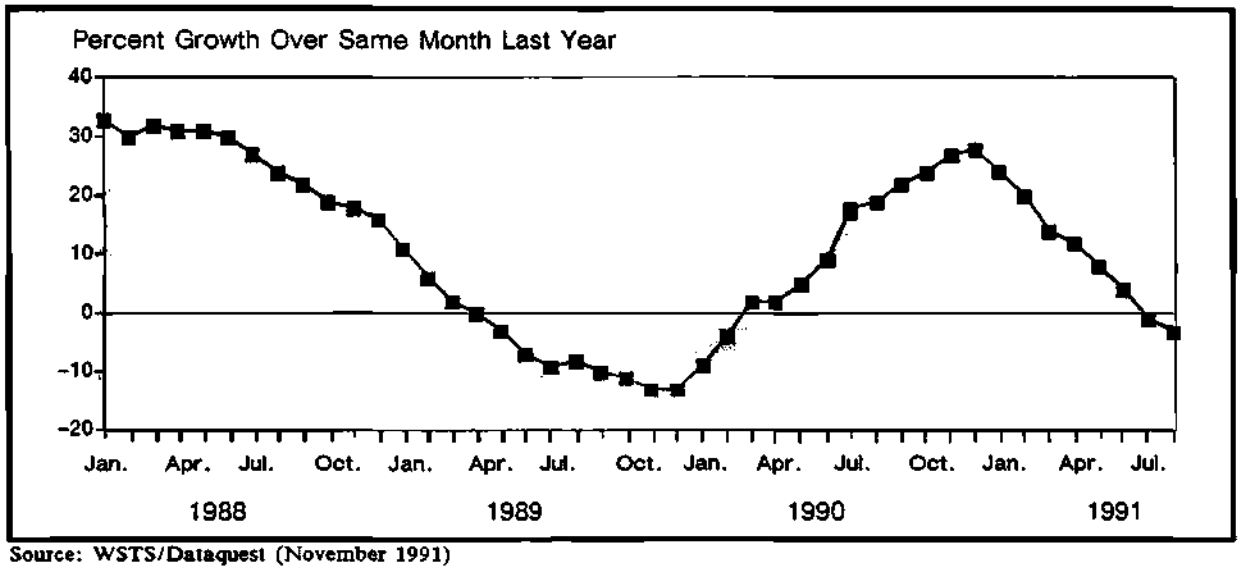
Source: WSTS/Dataquest (November 1991)

Figure 2
Analog IC Bookings and Billings (Three-Month Rolling Average)



Source: WSTS/Dataquest (November 1991)

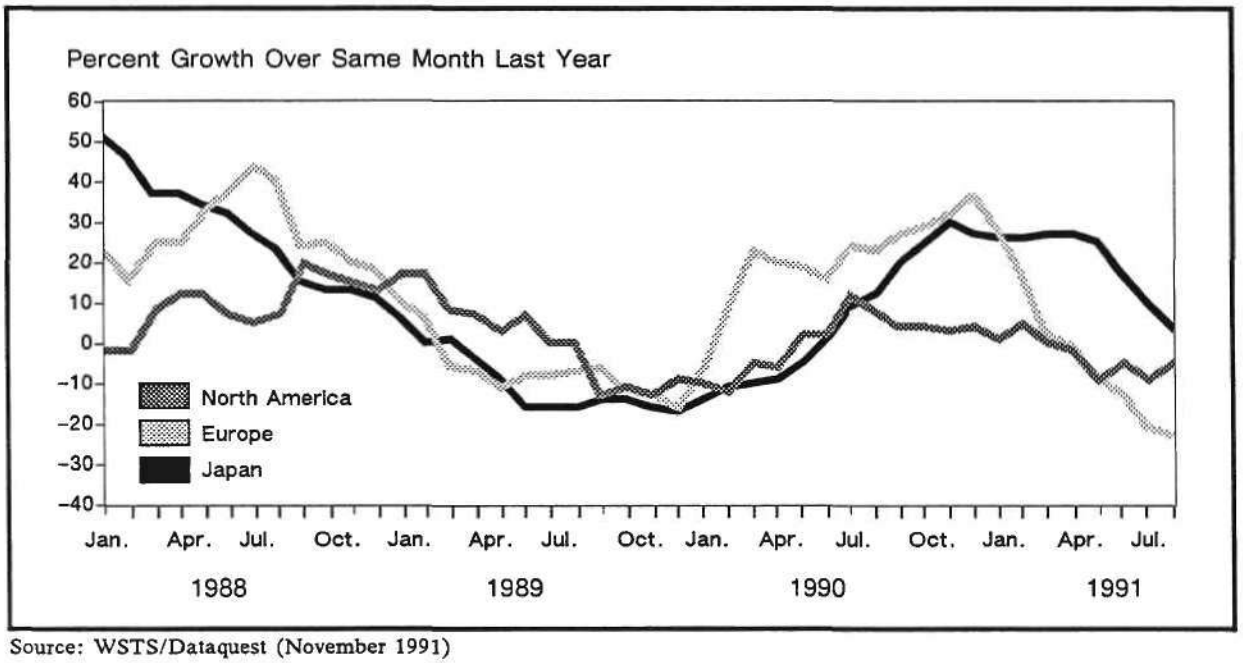
Figure 3
Analog Bookings Monthly Growth Comparison



Source: WSTS/Dataquest (November 1991)

The analog market is now caught in a trend of slowing growth. If we believe the consistency of this trend, it is reasonable to forecast bookings that will be below 1990 levels for the rest of 1991. It is also likely that the upturn in bookings (where it passes the zero growth line) will probably not occur until the second quarter of 1992. Essentially, Dataquest expects the trend from May 1989 to December 1989 to be repeated in the coming months. Although we have not plotted billings, the billings growth rate pattern follows that of bookings very closely and can be considered to be equivalent.

Figure 4
Analog Bookings Growth by Region



Source: WSTS/Dataquest (November 1991)

Forecast by Region

Breaking the consolidated growth pattern of Figure 3 into the three main constituent regions results in the plot of Figure 4. The North American market shows less volatility but also appears to miss out on the stronger growth patterns. Japan shows a strong but declining growth profile in 1991; Europe shows a rapid erosion of its 1990 bookings growth.

The problem in North America is twofold. First, it missed the growth offered by the consumer and communications markets in 1990. Part of this growth was the result of a weaker dollar compared with local currency in those regions. Second, North American industrial and computer markets have been slower than anticipated.

Forecast

In terms of Dataquest's analog forecast, the trend considerations are consistent with our quarterly growth forecast, where we expect negative 0.6 percent growth for the first quarter of 1992 and 1.5, 3.4, and 6.4 percent growth for the second, third, and fourth quarters, respectively. The five-year forecast, along with annual growth, is shown in Table 1.

Dataquest Perspective

The changing rate of bookings is not unexpected. Although it is difficult to anticipate patterns many years in the future, the near-term results are consistent with past book/bill ratios and growth trends. Although patterns and trends do not explain the underlying fundamentals that drive consumption, they are a useful check on the value of Dataquest assumptions about the changing nature of analog IC consumption. Recent results do not contradict the analog forecasts made last year. ■

By Gary Grandbois

Table 1
Analog IC Forecast (Millions of Dollars)

	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-1995
Total Analog	10,571	11,772	13,265	15,225	17,235	18,710	12.1
Annual Growth (%)	13.25	11.36	12.68	14.78	13.20	8.56	

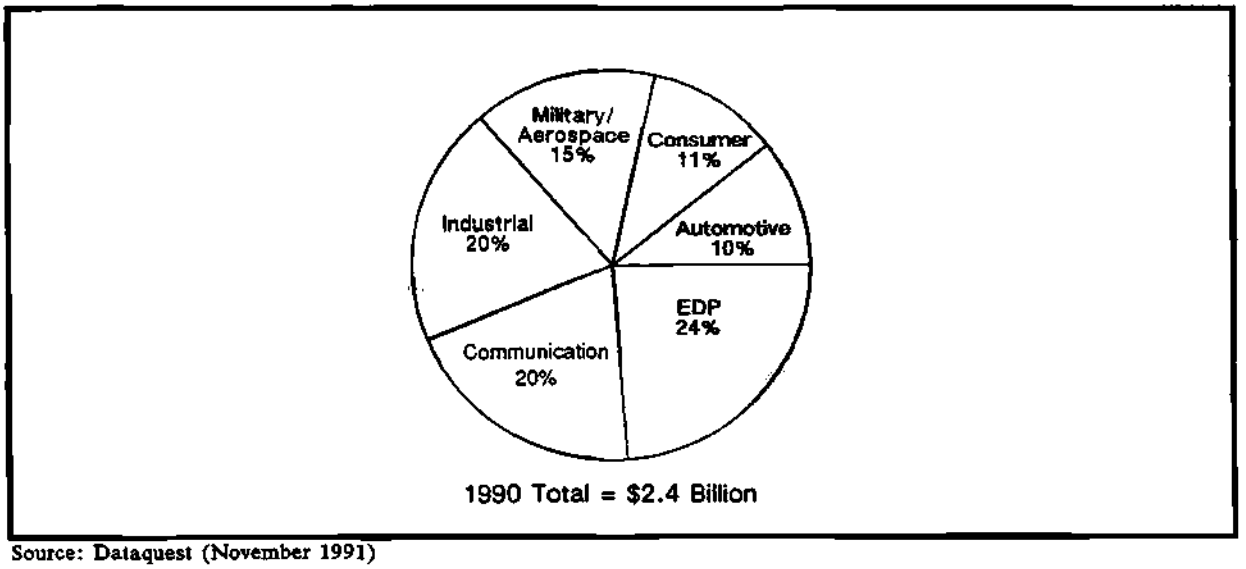
Source: Dataquest (November 1991)

Mixed-Signal ICs: The Silver Lining in the North American Market

The potential for analog IC growth in North America has been somewhat clouded in recent years because of many mature products being sold into slow growth markets such as military and industrial. The North American market missed much of the analog growth in 1990, which occurred in market segments such as consumer-specific ICs that are relatively weak locally. On the other hand, North America is the major consumer of mixed-signal ICs for the significant communications and computer markets. Figure 1 shows the North American analog IC market segmented into six major end markets. Almost two-thirds of the North American market goes to combined consumption by the industrial, communications, and computer markets.

North American analog IC consumption can be broken down further into mixed-signal and linear IC products, with mixed-signal ICs taking about 53 percent of the total revenue. These two components have important ramifications for growth of the North American market. Table 1 shows the forecast five-year compound annual growth rate (CAGR) by market for both linear and mixed-signal ICs. Mixed-signal ICs show far stronger anticipated growth than do linear ICs. Mixed-signal IC growth in North American communications and data processing markets is substantial and counterbalanced by

Figure 1
Estimated North American Mixed-Signal Market by End Application



Source: Dataquest (November 1991)

Table 1
Worldwide Growth Rates by Application Market—Mixed-Signal versus Linear ICs

Market	1990-1995 Linear IC CAGR (%)	1990-1995 Mixed-Signal IC CAGR (%)
Industrial	0.7	8.9
Data Processing	8.8	19.8
Communications	6.9	18.6
Military	-0.3	6.1
Consumer	12.2	22.0
Automotive	14.5	15.7

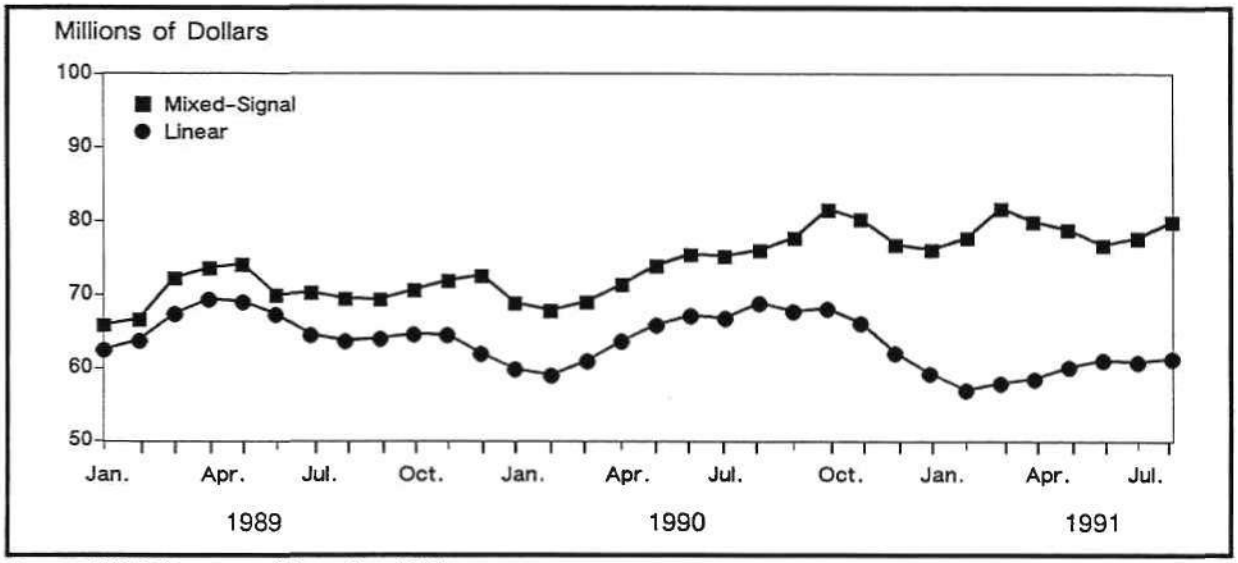
Source: Dataquest (November 1991)

Table 2
North American Analog IC Consumption Forecast (Millions of Dollars)

	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-1995
Mixed-Signal	1,281	1,444	1,664	1,955	2,264	2,550	14.8
Linear	1,160	1,252	1,400	1,558	1,660	1,721	8.2
Total	2,441	2,696	3,064	3,513	3,924	4,271	11.9
Annual Growth (%)	6.1	10.4	13.6	14.7	11.6	8.8	

Source: Dataquest (November 1991)

Figure 2
North American Analog IC Billings, Mixed-Signal versus Linear ICs



Source: WSTS/Dataquest (November 1991)

weak growth of linear ICs in general and by a limited growth outlook for the industrial and military markets. The net effect of these markets on the North American analog IC forecast is shown in Table 2. Note that although mixed-signal IC growth in North America is about twice that of linear ICs, it is still less than that of mixed-signal IC growth worldwide (16.7 percent CAGR, 1990-1995). North America is an early user of mixed-signal ICs and can be considered a more mature market (slower growth) than the Japanese consumer IC market and others that are now adopting mixed-signal solutions.

Figure 2 shows two-and-a-half years of North American linear and mixed-signal billings by month. These data are from the World Semiconductor Trade Statistics (WSTS) program and differ from Dataquest slightly in magnitude and product coverage. Linear ICs have been showing little growth over this two-year, low-growth period for North America. In fact, linear ICs have shown a slight declining trend over this period. Growth has come totally from the mixed-signal segment of analog IC products.

Dataquest Perspective

Dataquest expects a return to a stronger North American market in mid-1992. The market will show moderate growth in linear ICs and a strong 15.2 percent growth in mixed-signal ICs. We expect linear ICs to trail mixed-signal growth by about 6 percent on average over the coming five-year period. Mixed-signal ICs already represent more than half the analog ICs consumed in North America and will exceed 60 percent in 1995. North American suppliers of linear ICs, especially commodity linear ICs, should be prepared for a perpetually weak market. High-performance niche linears will be the only way to achieve significant growth. ■

By Gary Grandbois

Product Analysis

Palette DACs: A Colorful Market Encompasses a Spectrum of Products

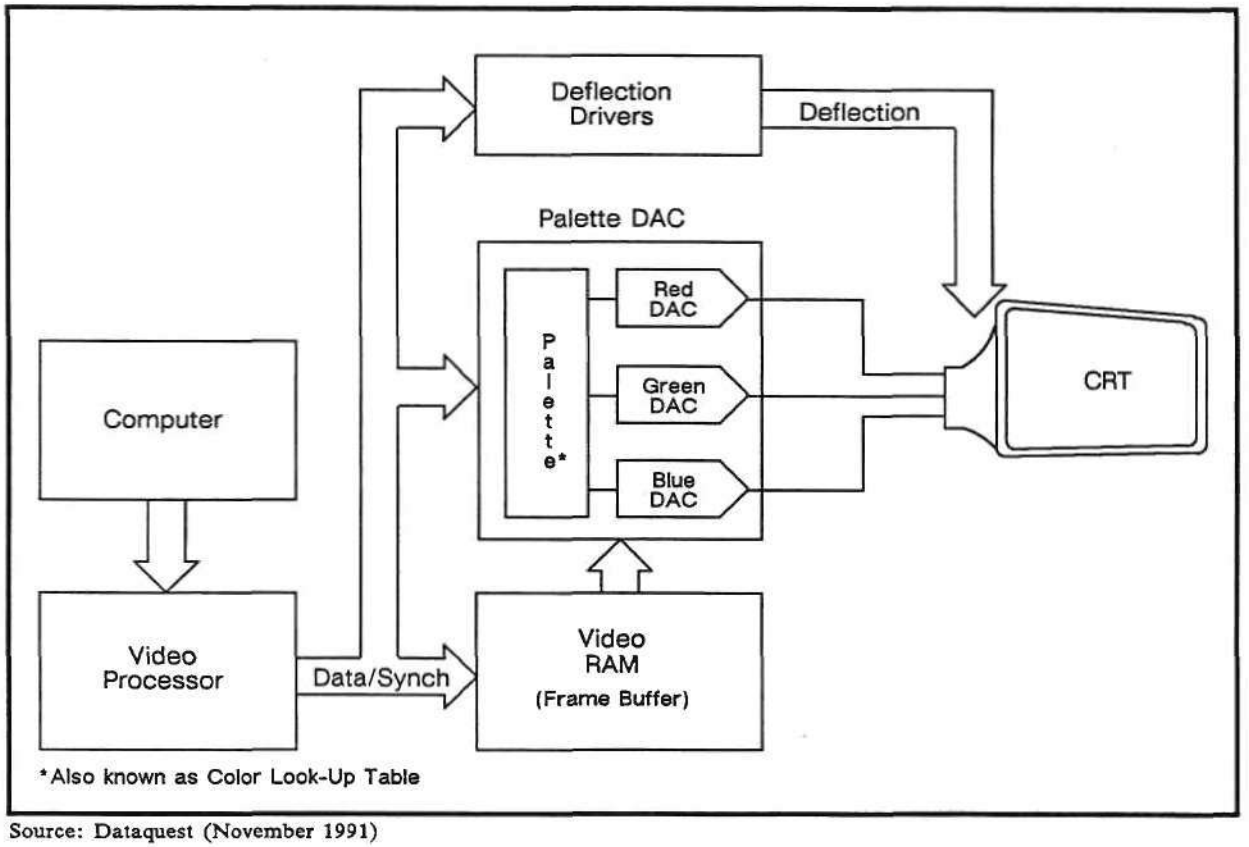
The Product

A niche market success story that has developed over the past couple of years is the video digital-to-analog converter (DAC), a specialized version of the traditional DAC. The video DAC market is composed of the products referred to as RAMDACs, palette DACs, and RGB DACs, which are devices that convert digital color data into the analog signal representation of the three primary colors (red, blue, and green). The video DAC started out as a hybrid triple DAC and migrated to a monolithic video DAC. The monolithic video DAC combined with RAM to enable on-chip color lookup tables (CLUTs, or palettes) creates the palette DAC or RAMDAC. These ICs have not stopped integrating functions at the CLUT but are on a steady path of increasing the digital controller content. Figure 1 shows a typical application of a triple DAC in a graphics application.

The Market

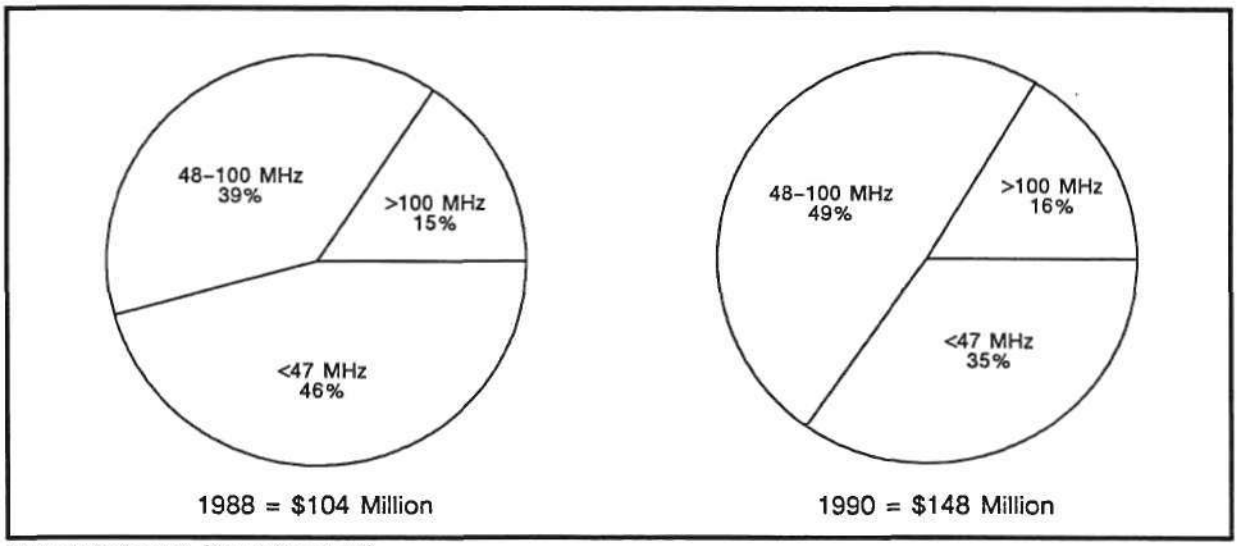
Growth in the video DAC market during the past few years has been strong in both the workstation and color graphics PC markets. Combined with growth in unit shipments is the movement to higher resolutions (bandwidth of the palette DAC). In 1988 the bulk of video DAC demand was in lower-resolution applications such as video graphics array (VGA) (640x480). However, as the PC arena moves from VGA to super VGA (800x600) and other high-resolution PC standards requiring 1,024x768 resolution emerge, video DAC demand has shifted accordingly. This change in conversion rates is shown in Figure 2. The shift to higher conversion rates has pushed lower-speed devices into the commodity category with prices significantly less than $2.

Figure 1
Palette DAC Application



Source: Dataquest (November 1991)

Figure 2
Video DAC Revenue in 1988 and 1990—Estimated Percentage by Conversion Rate



Source: Dataquest (November 1991)

Market Share

The video DAC market has many players. More than 75 percent of the revenue is held by five players, with a plethora of companies in the "Others" category (see Figure 3). Some of these other suppliers are Atmel, AT&T, Avasem, IMP, Motorola, Samsung, Sierra, Suntac, Trigem/Music, Texas Instruments, TRW, and Winbond. The largest player, with 40.5 percent of market share, is Brooktree Corporation. Brooktree was one of the originators of monolithic palette DACs and has stayed with the high-performance product (for further information on Brooktree, see "Brooktree: A Leading-Edge Company," in this issue).

Forecast

Although revenue growth in the past few years has been stunted by severe price erosion, Dataquest is still optimistic about the growth of this product. The broad need for video DAC in all graphics and imaging areas suggests a strong future. We forecast 22 percent compound annual growth rate (CAGR) from 1990 to 1995. Figure 4 presents the video DAC forecast in millions of dollars from 1991 to 1995, along with 1988 to 1990 actuals.

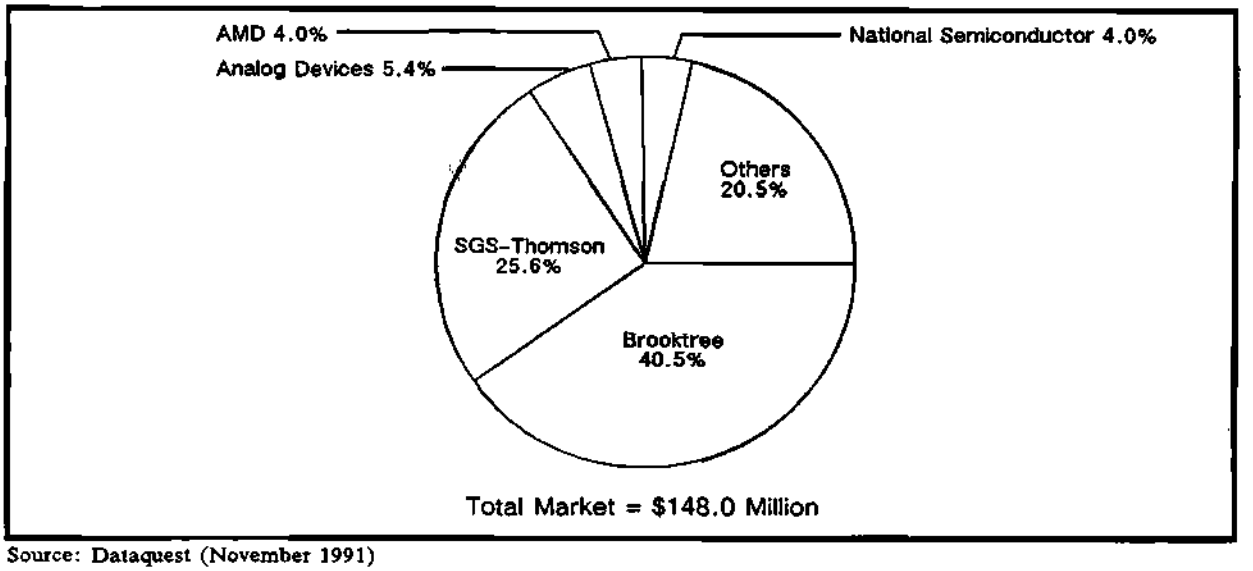
Pricing

As seen in Figure 5, pricing declined dramatically from 1988 to 1990. Video DAC pricing for the 6-bit low-end DAC has fallen to well below $2, which is more than a threefold decline from pricing of two years ago. However, as computer graphics demand higher resolutions and video DACs continue to integrate more features, price erosion, in the aggregate, is expected to level off. The increasing proportion of higher-performance, higher-priced video DACs will tend to offset the price decline seen in the lower-speed, 6-bit palette DAC.

Continuous-Edge Graphics

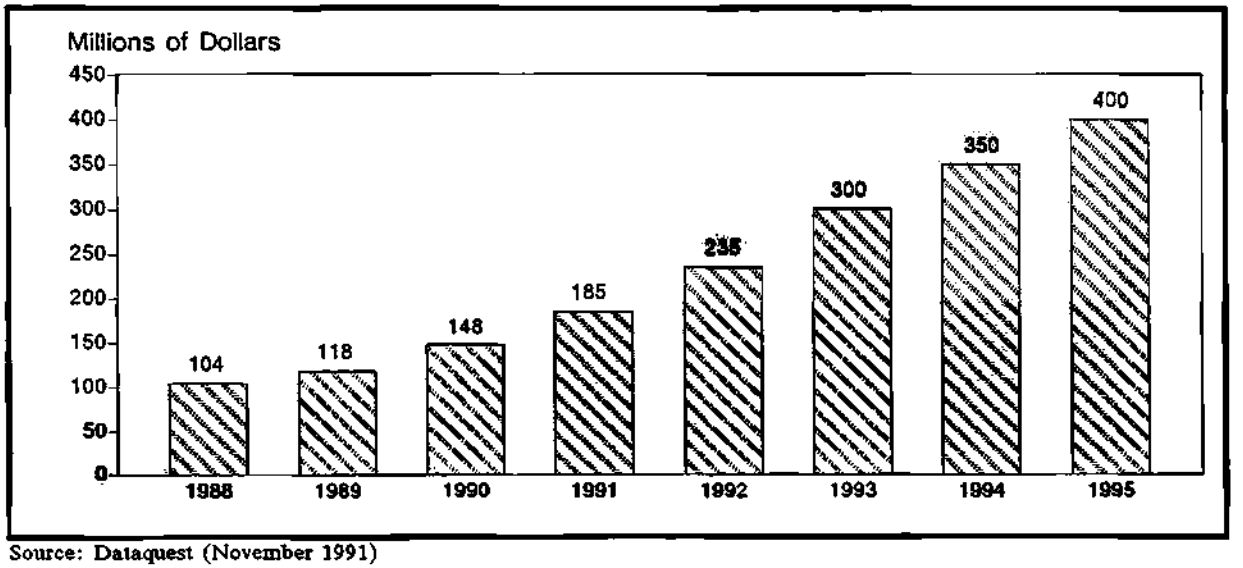
Analog Devices/Edsun Labs introduced the continuous-edge graphics (CEG) technique to achieve higher apparent resolution from relatively low-resolution palette DACs such as VGAs. This technique employs digital signal processing (DSP) techniques to eliminate jagged lines and provide smooth shading in color transitions. The CEG technique had some strong cost advantages when high-resolution monitors were relatively expensive because it could render "high resolution" on lower-resolution monitors. However, high-resolution monitor prices and high-resolution palette DAC prices have come down very rapidly, somewhat diminishing cost advantages of this technique. The CEG technique still retains an edge in shading, but it requires software drivers to take advantage of this capability. A number of software vendors are providing these drivers. This technique has not yet made a significant dent in the palette DAC market.

Figure 3
Video DAC Market Shares (Millions of Dollars)



Source: Dataquest (November 1991)

Figure 4
Video DAC Forecast—1988-1995 (Millions of Dollars)

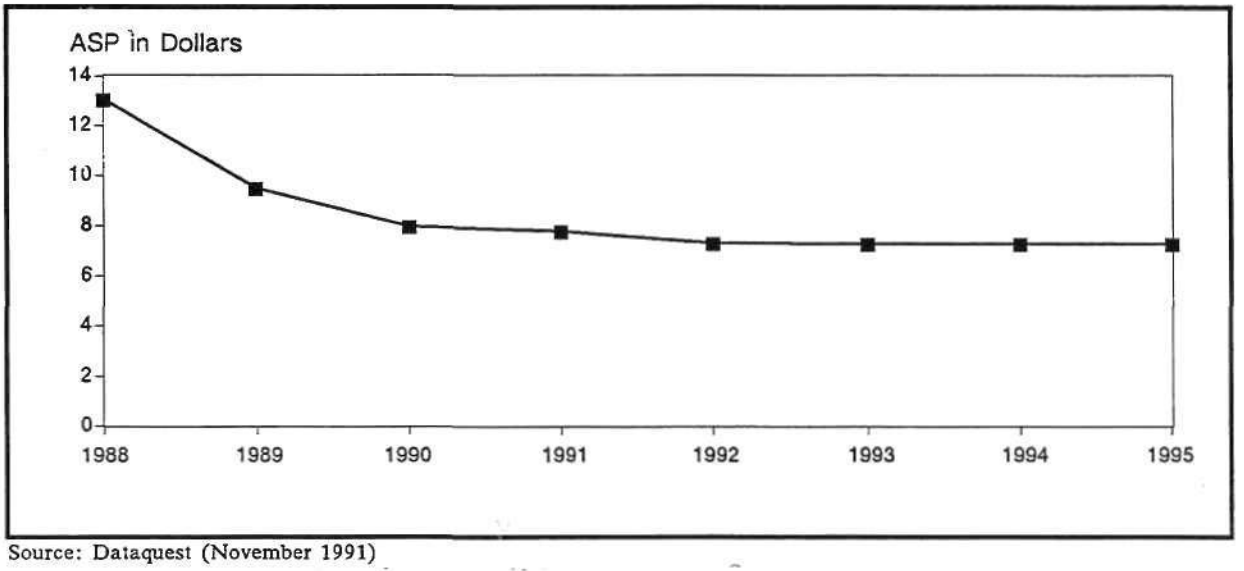


Source: Dataquest (November 1991)

Dataquest Perspective

Revenue and unit shipments, especially those of video ICs with triple RGB outputs, are growing at a substantial rate. Devices may range from palette DACs, multimedia ICs, or digital TV video ICs. Video DACs are placed on-chip in LCD controllers to provide laptop-to-desktop compatibility. Although all these devices are truly mixed-signal ICs, they are placed in any of a dozen categories both analog and digital. The forecast in this article embraces computer and imaging/multimedia markets in the broad sense, including all ICs that provide a video DAC function on-chip. In the long term, the

Figure 5
Palette DAC Forecast—Average Selling Price (Dollars)



Source: Dataquest (November 1991)

palette DAC may actually decline as a standalone IC, as it is readily incorporated into various video/graphics controller functions. We believe this device to be one of the major growth areas in computer and multimedia peripherals, and we will continue to follow it as a mixed-signal video DAC IC. ■

By Gary Grandbois and Anna Cahill

Company Analysis

Brooktree: A Leading-Edge Company

Brooktree Corporation is currently the leading supplier of RAMDACs to the computer graphics market. (For additional video DAC market information, see "Palette DACs: A Colorful Market Encompasses a Spectrum of Products," in this issue.) Brooktree's mission is to target niche markets requiring mixed-signal technology expertise and then create a single VLSI mixed-signal IC solution for these markets. Brooktree also has identified imaging and automatic test equipment (ATE) markets as possible niche markets that would benefit from the mixed-signal solution.

Brooktree was founded in 1981, began operations in 1983, and shipped its first product, an integrated video DAC, in 1985. Brooktree is currently a fabless company and has no stated intention of building one. In April 1991, Brooktree had its first public offering under the symbol BTRE. During the past five years, Brooktree's financial performance has been very strong, as shown in Table 1.

Brooktree seeks to maintain a leadership position in the mixed-signal arena by being able to add substantial value to customers' systems and develop lasting customer relationships with systems vendors. However, to maintain a leadership position Brooktree must continually identify newly emerging niche markets to develop. The company allocates approximately 21 percent of its revenue to R&D to be able to accomplish continual product development. This percentage is very large compared with the industry average of 9 to 10 percent allocated to R&D.

Technology

The company pursues niche areas requiring challenging mixed-signal capabilities and, by being first to market, strives to create a de facto standard for the marketplace. Brooktree developed a proprietary technology that it calls its "matrix" theory. The matrix provides the base technology to integrate analog and digital portions in a single chip and enables Brooktree

Table 1
Brooktree Corporation—Financial History (Millions of Dollars)

	1986	1987	1988	1989	1990
Revenue	1.7	12.7	38.8	51.2	68.5
Gross Profit	-1.4	4.9	23.0	31.5	40.4
R&D Expense	4.7	4.8	7.3	11.3	13.4
Net Income	-9.3	-4.9	6.0	8.2	8.1
Working Capital	7.5	9.9	15.5	23.3	26.0
Total Assets	16.6	23.3	33.4	44.0	55.0

Source: Brooktree Corporation Annual Report

to provide single-chip mixed-signal VLSI solutions as exemplified by its computer graphics product line.

Computer Graphics

Video DAC revenue accounts for 90 percent of Brooktree's total revenue, and the company enjoys a 40 percent share of the entire video DAC market. Brooktree offers a plethora of video DACs for the computer graphics arena, from low-end desktop and laptop applications to high-end workstation graphics. However, as the low-end DAC market experiences price erosion and as integration of DACs and graphics controllers occurs, Brooktree will decrease its focus in the low-end DAC market and increase focus in the high-end market. Alternatively, Brooktree is also willing to work with digital companies to license them with low-end DAC expertise for incorporation into graphics controller chips.

Dataquest believes that Brooktree's technology strength and value can continue to be realized in the high-end DAC arena without need to compete in the already satiated commodity low-end video DAC market. Brooktree's strategy is to develop enabling technology for its customers' systems and to maintain lasting customer relationships through allocation of resources to marketing, testing, quality assurance, and customer support. Brooktree has developed strong supplier relationships with workstation vendors that require the high-end video DAC solution. These companies include Apple Computer, Digital Equipment Corporation, Hewlett-Packard Company, IBM Corporation, Intergraph Corporation, NeXT Computers, Silicon Graphics, Sony Corporation, and Sun Microsystems. However, the high-end DAC market is not without its emerging competitors. Companies such as Analog Devices, AT&T, Inmos Corporation/SGS-Thomson Microelectronics B.V., and TRW are entering the computer graphics market with alternative solutions and challenging Brooktree's strong leadership position.

Seeking New Product Areas

Brooktree has developed and continues to announce products for the computer imaging and ATE marketplace. Both areas are forecast to emerge in the next few years and are viewed by Brooktree as niche markets that will benefit from the development of VLSI mixed-signal ICs. Currently, imaging and ATE together make up only 10 percent of the company's revenue, but these products garner high average selling prices to offset high development costs.

Dataquest Perspective

Brooktree Corporation is an exemplary successful start-up semiconductor company. The computer graphics video DAC market requires the technology Brooktree is able to offer, and Brooktree has been able to maintain a leadership position in this market. It has, in some cases, successfully contested the threat of competitive entry through legal action for patent infringement. Brooktree has pursued patent infringement litigation in four separate cases, as follows:

- Advanced Micro Devices Inc. (AMD)—This case resulted in a $26 million award to Brooktree and an injunction stating that AMD was to cease manufacture of the product.
- Integrated Device Technologies (IDT)—An agreement was reached for IDT to abandon the market by a specified time.
- Samsung Semiconductor—This case is still being litigated.
- Sierra Semiconductor—This case began in June.

Although Brooktree has a strong patent position for fast SRAMs and DACs used in RAMDACs,

competition is still emerging with viable solutions for the high-end video DAC market. Dataquest believes that Brooktree will be able to maintain its leadership position in video DACs for the near future. Current customer confidence in Brooktree's technical capability and service is high. But as competition becomes more established in the market, other companies will begin to differentiate their products through added features or cost benefits and gradually will make inroads into Brooktree's customer base.

Brooktree is able to keep its operating expenses low by being fabless and using foundry services to manufacture its devices. The high financial cost of filling and maintaining a fab is a burden Brooktree chose not to bear, allowing it to focus on design and marketing aspects of the business, rather than operate a fab. However, the downside of not having a fab is lack of control over the process or supply from the foundry. To become a high-volume supplier, a company needs more control of these activities. Brooktree's goal is not to become a high-volume, low-cost supplier; rather, the company is constantly identifying new niche markets where it can excel with its technology.

Brooktree has identified imaging/multimedia as a potential growth market in the near future. The imaging market is still in its infancy, with systems companies beginning to implement new imaging techniques as customers begin to become aware of the need for advanced imaging products.

Brooktree is betting on the imaging market, the ATE market, and other opportunities that may arise, much as it did on the computer graphics market, for continued success of the company. This strategy of continually being a leading-edge company would seem to characterize Brooktree as forever a start-up. The challenges presented by this strategy are the ongoing need to invest large amounts of money into R&D, the potential of entering an overcrowded market, and the general softness of the semiconductor industry. However, as in Brooktree's case, benefits of high margins can significantly outweigh challenges if the right opportunities are discovered. ■

By Anna Cahill

In Future Issues

The mixed-signal and linear IC market forecasts will be presented and contrasted in the next issue. The product focus will be on data converters.

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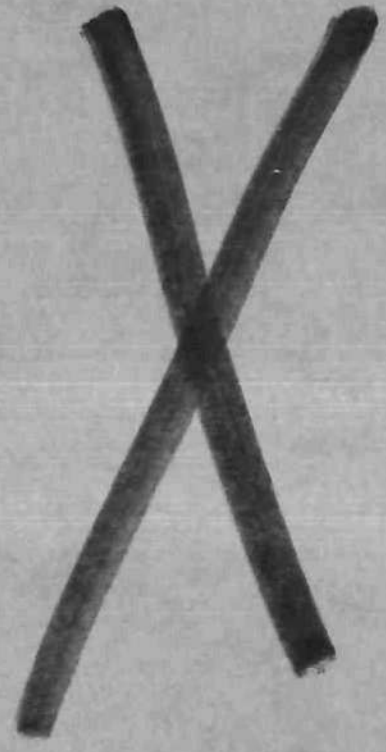

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Research Newsletter

EDA INDUSTRY UPDATE AND OUTLOOK

SUMMARY

The turmoil that has become the hallmark of the electronic design automation (EDA) industry through the mid-1980s continued unabated through 1989 and 1990; more mergers and acquisitions, new players displacing onetime industry leaders, new standards emerging, the accelerating trend toward open systems, and changes in market conditions that demand revamped business models and strategies.

A tremendous amount of confusion existed in the market regarding which EDA products and companies provided the best technology as customers tried to sort out the conflicting claims of all the EDA vendors, each expounding its superiority. The market had major concerns about the stability of other EDA companies in light of the Dazix experience. Because of the extremely high costs associated with switching Dazix tools with other vendors' tools, the market was understandably cautious about investment decisions regarding new EDA suppliers.

MARKET ANALYSIS

The total EDA market grew by 12.6 percent in 1989, amounting to $2.9 billion. This figure includes hardware (including peripherals when shipped as a turnkey system), software, and service for the CAE, printed circuit board (PCB) layout, and IC layout markets. The EDA software market expanded by 14.4 percent, or $1.06 billion.

Table 1 shows that the leading EDA software players in 1989 were Mentor Graphics, Cadence, Valid Logic, Dazix, and Racal-Redac.

TABLE 1
1989 Worldwide EDA Market Share Scorecard

Company	Total Percentage*	Software-Only Percentage
Mentor Graphics	14.6	19.6
Cadence Design Systems	4.7	11.0
Valid Logic Systems	6.1	9.5
Dazix	5.4	6.5
Racal-Redac	3.2	6.5
Others	66.0	46.9
Total	100.0	100.0

*Market share based on revenue from hardware, software, and maintenance
Source: Dataquest (January 1991)

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EDA INDUSTRY FACES FUNDAMENTAL STRUCTURAL CHANGES

Dataquest believes that the EDA industry will continue to undergo significant structural changes during the next five years. These changes are expected to manifest themselves in the following ways:

- Because of the fragmented nature of the EDA industry, it will continue to experience consolidation via mergers, acquisitions, and fallout.
- Because of the trend toward open systems and standards, both of which lower the barriers to entry, Dataquest expects an increasing number of niche product suppliers to enter the market.
- Another structurally significant change that is occurring in the EDA industry relates to the shift in bargaining power between EDA customers and EDA suppliers. Tools developed in-house are rapidly losing ground to commercial tools in terms of functionality, user-interface capabilities, integration with other tools, and performance. Although we believe that most large electronics manufacturers will continue to develop tools in-house, they will concentrate on leveraging their R&D investment by focusing on developing tools and technologies unavailable on the open market.
- Dataquest believes that the distribution channels used by EDA companies, which were predominantly direct in the 1970s and 1980s, will include more use of the OEM channel. We anticipate that large EDA companies, as well as ASIC suppliers, will become OEM purchasers of niche products to help round out their product lines.

DATAQUEST PERSPECTIVE

Dataquest believes that if the 1980s can be characterized as the EDA industry's consolidation phase, the 1990s will be marked as a shakeout period, with several major players exiting the business or scaling down operations. The rules that guided EDA suppliers in the 1980s will be dramatically different in the 1990s, driving suppliers to adopt new business strategies. But the challenges of the 1990s will herald many market opportunities for the EDA industry. Dataquest believes that a significant market opportunity exists for the following kinds of products and technologies:

- Tools supporting top-down design
- System-level EDA design tools
- Tools facilitating design partitioning, so that the design team can optimally partition a design to meet such constraints as performance, size, cost, reliability, testability, and manufacturability
- Tools enabling implementation trade-off analyses, thus facilitating the optimal selection of ASICs
- Tools supporting analog design automation
- EDA products supporting the design of high-speed electronic systems
- Tools supporting the design of digital signal processing systems

Note: This newsletter is based on research performed by analysts in Dataquest's CAD/CAM Industry Service.

Patricia Galligan
Ron Collett

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Research Newsletter

CMOS PLDs TURN IN ANOTHER YEAR OF STRONG GROWTH

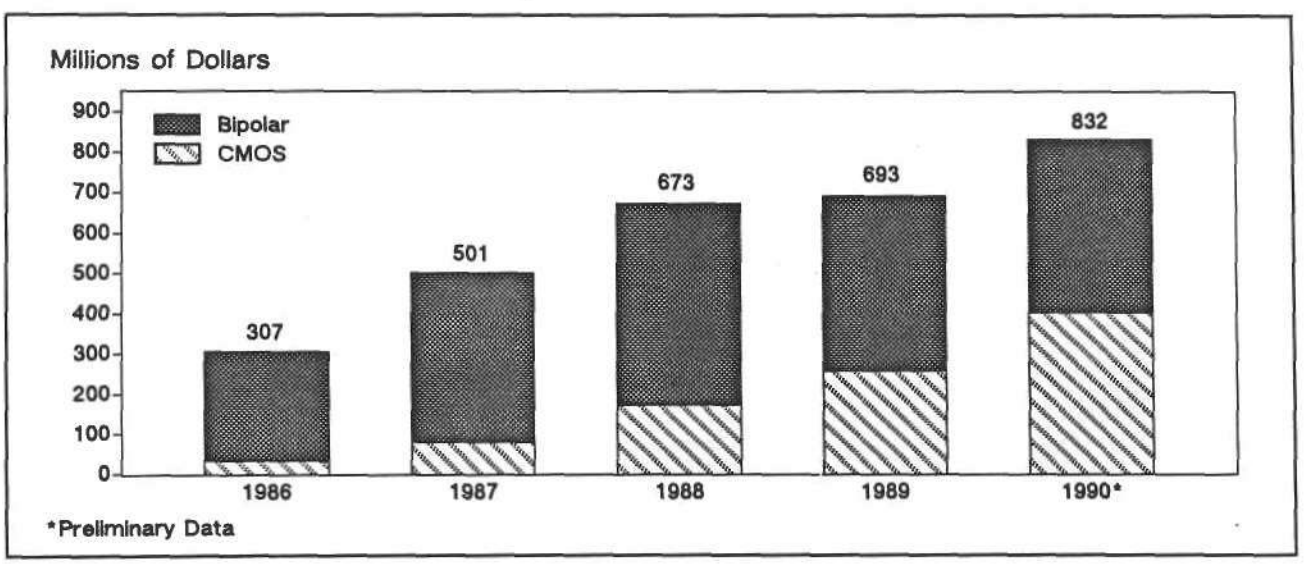
SUMMARY

According to preliminary market share results, the programmable logic device (PLD) market grew by a robust 20 percent in 1990 to $832 million. This growth rate was attributable to the strong performance of CMOS PLDs, which continued their meteoric rise. As occurred in 1989, CMOS PLDs experienced another year of strong growth, increasing in the 56 percent range to $402 million. The bipolar segment of the market experienced a slight decline of 1 percent decreasing to $430 million. Our long-term forecast remains predicated on the belief that bipolar will continue to be a declining market. CMOS PLDs are expected to continue to outpace bipolar in growth rates, and our forecast calls for CMOS PLD shipments to overtake bipolar device shipments within 1991. This trend is reflected in Figure 1, which shows the split between CMOS and bipolar as a percentage of total PLD revenue during the past five years.

COMPETITIVE PROFILE

By virtue of their very large bipolar PLD portfolios, Advanced Micro Devices (AMD) and Texas Instruments (TI) retained their number one and two positions, respectively, in the worldwide PLD market in 1990. However, as is evident in Figure 2, the most impressive growth came from the smaller companies, the majority of which participate only in the CMOS segment of the market. TI, the only bipolar supplier to record growth, did so mostly at the expense of the other market players.

FIGURE 1
Estimated PLD Revenue from 1986 through 1990



Source: Dataquest (February 1991)

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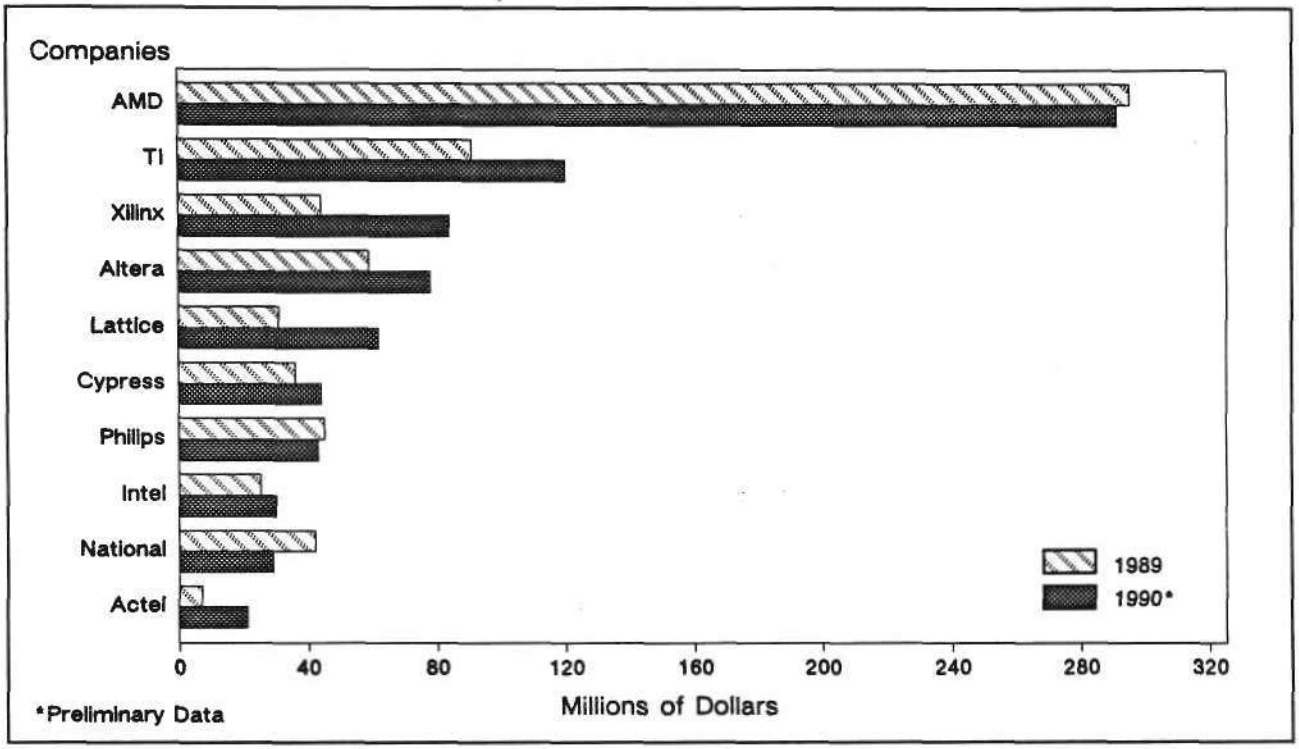
FIGURE 2
Top 10 PLD Companies Worldwide—1990



Source: Dataquest (February 1991)

TABLE 1
Estimated Preliminary Worldwide 1990
CMOS PLD Market Share Rankings

1990 Rank	1989 Rank	Company	1989 ($M)	1990* ($M)	Percent Change	Market Share (%)
1	2	Xilinx	44	84	90.9	20.9
2	1	Altera	59	78	32.2	19.4
3	4	Lattice Semiconductor	31	62	100.0	15.4
4	5	Cypress Semiconductor	36	44	22.2	10.9
5	3	Advanced Micro Devices	27	42	55.6	10.4
6	6	Intel	23	30	30.4	7.5
7	8	Actel	7	21	200.0	5.2
		Others	31	41	32.3	10.2
		Total	258	402	55.8	100.0

*Preliminary Data
Source: Dataquest (February 1991)

CMOS: Where the Action Is

Xilinx, which supplies field-programmable gate arrays (FPGAs), overtook 1989's leading CMOS PLD supplier to become number one in 1990. As can be seen in Table 1, the top seven suppliers accounted for about 90 percent of the total market. Actel, another FPGA supplier, also registered spectacular growth. The group of companies designated as Others accounts for only 10 percent of the market but represents some 10 companies vying for market share.

TABLE 2
Estimated Preliminary Worldwide
1990 Bipolar Market Share Rankings

1990 Rank[1]	Company	1989 ($M)	1990[2] ($M)	Percent Change	Market Share (%)
1	Advanced Micro Devices	268	249	-7.1	57.9
2	Texas Instruments	90	117	30.0	27.2
3	Philips Components	43	42	-2.3	9.8
4	National Semiconductor	34	22	-35.3	5.1
	Total	435	430	-1.1	100.0

[1]
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Bipolar Market is Lackluster

Table 2 shows the competitive position in the bipolar segment of the market, with all players except TI losing market share. Given the rapid growth of CMOS compared with the declining prospects for bipolar, it makes sense that these companies are also positioning themselves to participate in the CMOS market.

DATAQUEST PERSPECTIVE

CMOS PLDs are the drivers for market growth in PLDs. The CMOS segment of the PLD market comprises PLAs (or simple PLDs) and PMDs and FPGAs (or complex PLDs). Simple CMOS PLDs grew at the rapid rate of 43 percent in 1990 over the previous year to $274 million. Complex PLDs grew more than 94 percent in 1990 over the prior year to approximately $128 million. Dataquest believes that complex PLDs represent the greatest potential for growth and expansion. Although a few standards appear to be forming, the market is young and there is still room for innovative companies.

Patricia Galligan

Dataquest
a company of The Dun & Bradstreet Corporation

Research Newsletter

CMOS PLDs TURN IN ANOTHER YEAR OF STRONG GROWTH

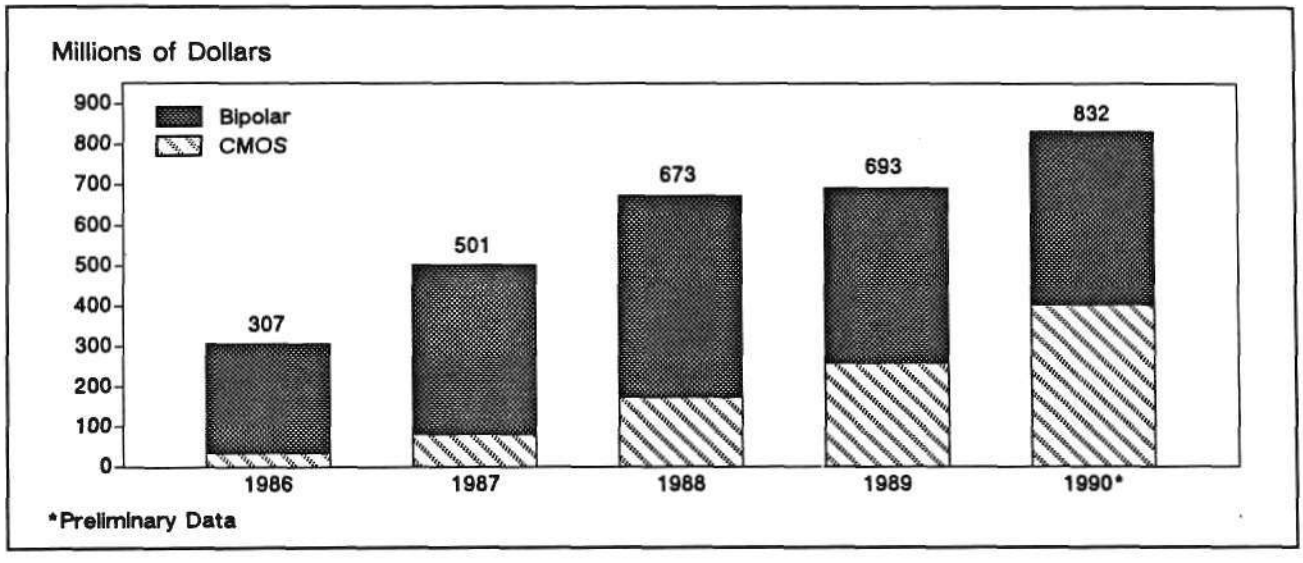
SUMMARY

According to preliminary market share results, the programmable logic device (PLD) market grew by a robust 20 percent in 1990 to $832 million. This growth rate was attributable to the strong performance of CMOS PLDs, which continued their meteoric rise. As occurred in 1989, CMOS PLDs experienced another year of strong growth, increasing in the 56 percent range to $402 million. The bipolar segment of the market experienced a slight decline of 1 percent decreasing to $430 million. Our long-term forecast remains predicated on the belief that bipolar will continue to be a declining market. CMOS PLDs are expected to continue to outpace bipolar in growth rates, and our forecast calls for CMOS PLD shipments to overtake bipolar device shipments within 1991. This trend is reflected in Figure 1, which shows the split between CMOS and bipolar as a percentage of total PLD revenue during the past five years.

COMPETITIVE PROFILE

By virtue of their very large bipolar PLD portfolios, Advanced Micro Devices (AMD) and Texas Instruments (TI) retained their number one and two positions, respectively, in the worldwide PLD market in 1990. However, as is evident in Figure 2, the most impressive growth came from the smaller companies, the majority of which participate only in the CMOS segment of the market. TI, the only bipolar supplier to record growth, did so mostly at the expense of the other market players.

FIGURE 1
Estimated PLD Revenue from 1986 through 1990



Source: Dataquest (February 1991)

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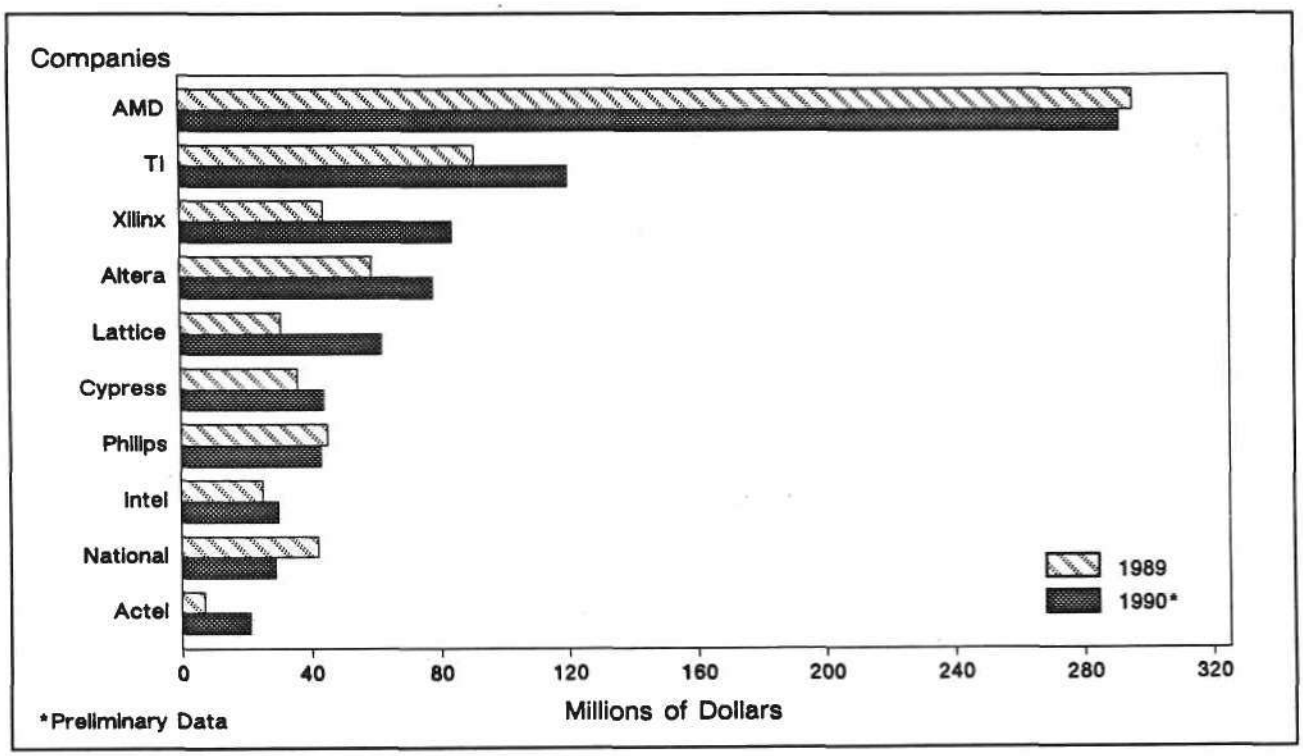
FIGURE 2
Top 10 PLD Companies Worldwide—1990



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Perhaps the most noteworthy aspect of the conference was the amount of third-party EDA vendors in attendance. The densities and complexities offered by CPLDs are such that they will require more sophisticated support than do simple PLDs. For instance, Synopsys announced its Design Compiler, a product that allows designers to use VHDL or Verilog hardware description languages to describe the function of an ASIC and then synthesize the design in an Actel, Texas Instruments, or AT&T FPGA. VIEWlogic's presentation reviewed its existing support of FPGA suppliers such as Actel, Xilinx, and other PLD vendors. The capabilities of CPLDs are such that they will have significant implications for and impact on the ASIC market; already these devices are encroaching on low-gate-count gate-array design starts. Time to market is driving complex PLD growth now and is likely to become more intense. Higher systems integration and ever-shortening system product life cycles, combined with the costs of these devices as they start to come down the learning curve, will propel consumption of these devices in increasingly higher volume applications. This means that although these devices are typically used as prototypes and in early production quantities today, they could be used as production vehicles in the future. Third-party software tool companies are motivated to provide tools that capture and synthesize designs so that the design can be migrated among various products and technologies. This means that, for a faster-time-to-market approach, a customer may initially implement a design in an FPGA from his or her choice of suppliers and later decide to migrate the design into a gate array should market acceptance call for a lower-cost solution.

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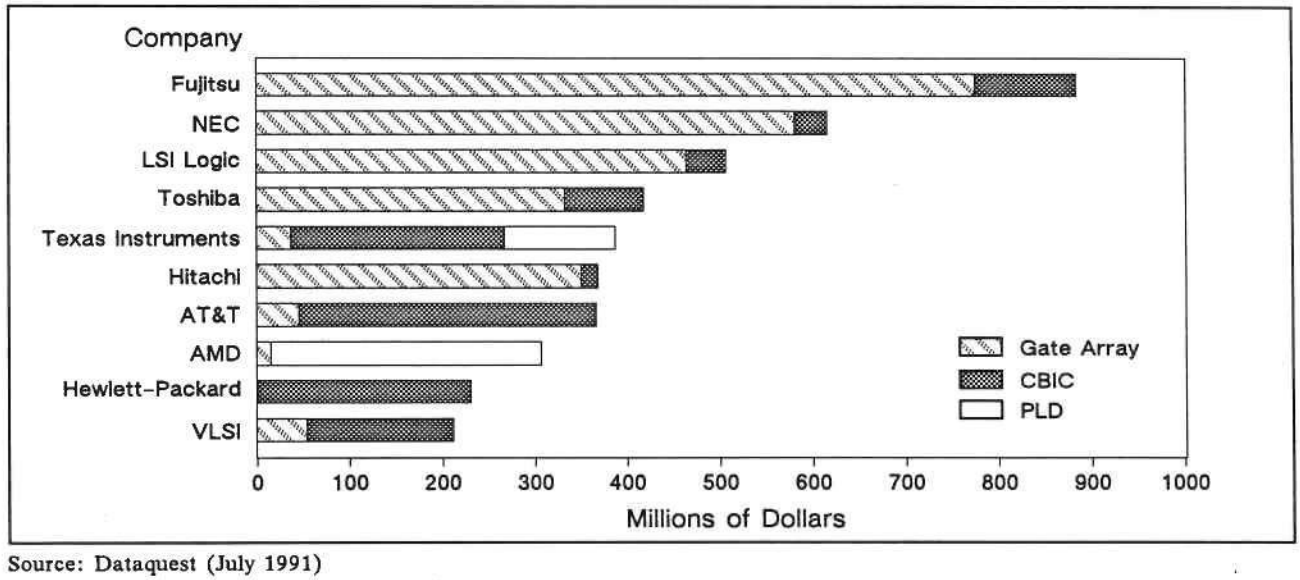
As Figure 1 shows, the top 10 ASIC suppliers consist of a healthy balance of U.S.- and Japan-based suppliers. At the same time, the product mix among the top 10 varies considerably. The Japan-based companies, for example, derive the bulk of their revenue from gate arrays. In contrast, U.S.-based suppliers are dominant in the CBIC market. Only one company, AMD, now claims a spot in the top 10 by virtue of its PLD revenue.

Although it may seem that companies such as LSI Logic are not growing as fast as Fujitsu and NEC, it is important to recognize that increasing revenue alone will not be a good enough gauge of success in the 1990s. LSI Logic's slower revenue growth is a reflection of its greater focus on profitability. The challenge facing all suppliers is to increase profit margins, not just increase revenue. Vendors such as LSI Logic and VLSI Technology are trying to focus on high-margin products while decreasing their exposure to low-margin commodity ASIC business.

FIGURE 1
Top 10 ASIC Suppliers—1990



Source: Dataquest (July 1991)

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For example, National Semiconductor fell from the top 10 rankings in 1990 because, in attempting to compete head-on in the low-density, low-margin commodity CMOS gate array business, it was at a competitive disadvantage with vertically integrated ASIC suppliers that could amortize their ASIC costs over both their internal system business and their merchant ASIC business.

PRODUCT OVERVIEW

Gate Arrays

The worldwide ASIC market grew approximately 12 percent over 1989 to $9.27 billion. Figure 2 presents the composition of the ASIC market by product and shows that gate arrays continue to dominate the market.

For gate arrays, 1990 was a year that yielded few surprises. Generally, the year can be characterized as exhibiting modest growth with the strong growing stronger and a significant segment of suppliers experiencing very tough times. Dataquest's final market share data show the gate array market growing by almost 12 percent over 1989. Figure 3 shows the picture in terms of supplier rankings. The market share rankings remained essentially unchanged from the previous year with the exception of the new conglomerate, GEC/Plessey/MEDL, switching places with Oki in the lineup. Fujitsu, the market leader, expanded its revenue by 25 percent over the prior year. Gains in the company's ECL gate array business for use in testers and very high end computer systems contributed significantly to this strong performance.

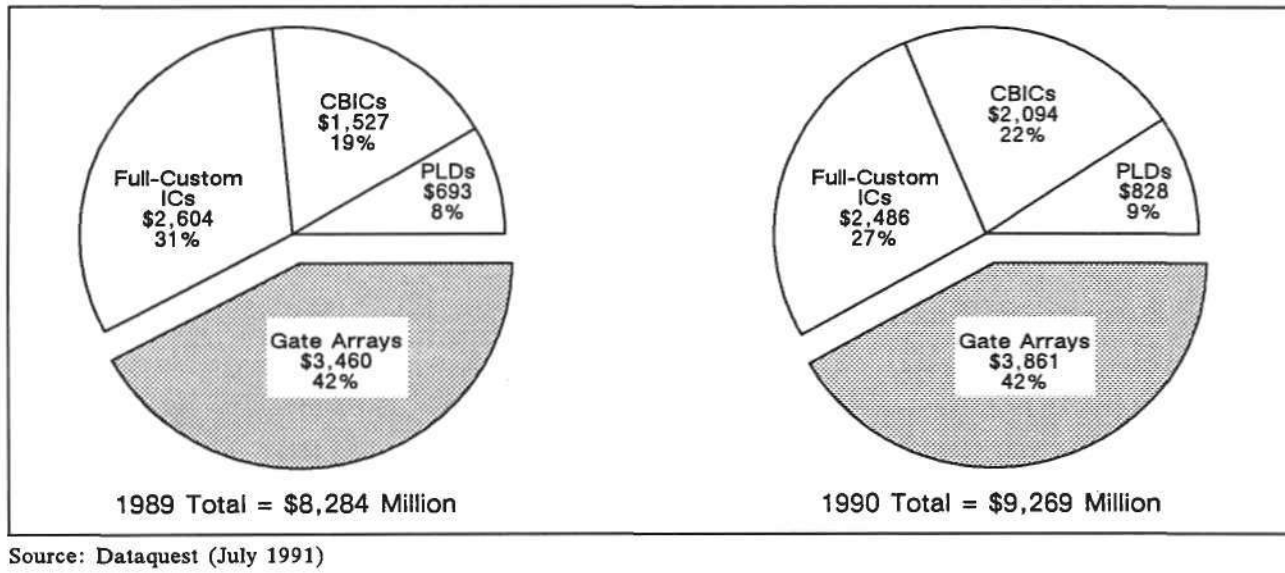
Figure 4 compares worldwide gate array consumption between 1990 and 1989 from a technology perspective. MOS gate arrays grew by 13 percent, whereas bipolar gate arrays grew a mere 6 percent. Meanwhile, growth in the BiCMOS arena significantly picked up. Indeed, the BiCMOS market grew by 40 percent in 1990. NEC, Fujitsu, and Hitachi are the only companies at this time with any significant revenue in this process category.

Cell-Based ICs

Although a 37 percent increase in CBIC revenue in 1990 over 1989 might seem to point to a very rapidly growing market, the jump in revenue stems from Hewlett-Packard's entry into the merchant CBIC market in 1990. For purposes of comparison, if we take out HP's $230 million contribution to the market, the corresponding growth rate of 22 percent is more in keeping with our forecast. Figure 5 represents the top 10 CBIC suppliers in terms of merchant and captive sales.

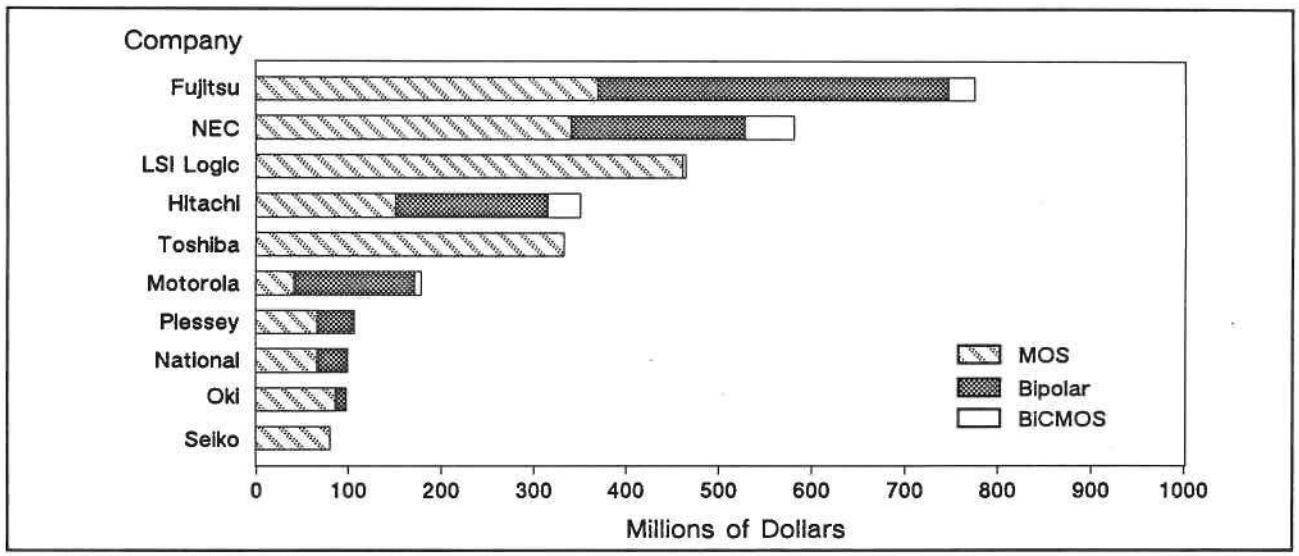
AT&T's combined internal and merchant CBIC business places the company first in the CBIC rankings. AT&T has been attempting to increase its merchant share of CBIC revenue. Indeed, in 1990, the company succeeded

FIGURE 2
Worldwide ASIC Consumption by Product



Source: Dataquest (July 1991)

FIGURE 3
Top 10 Worldwide Gate Array Suppliers—1990



Source: Dataquest (July 1991)

FIGURE 4
Worldwide Gate Array Consumption by Technology

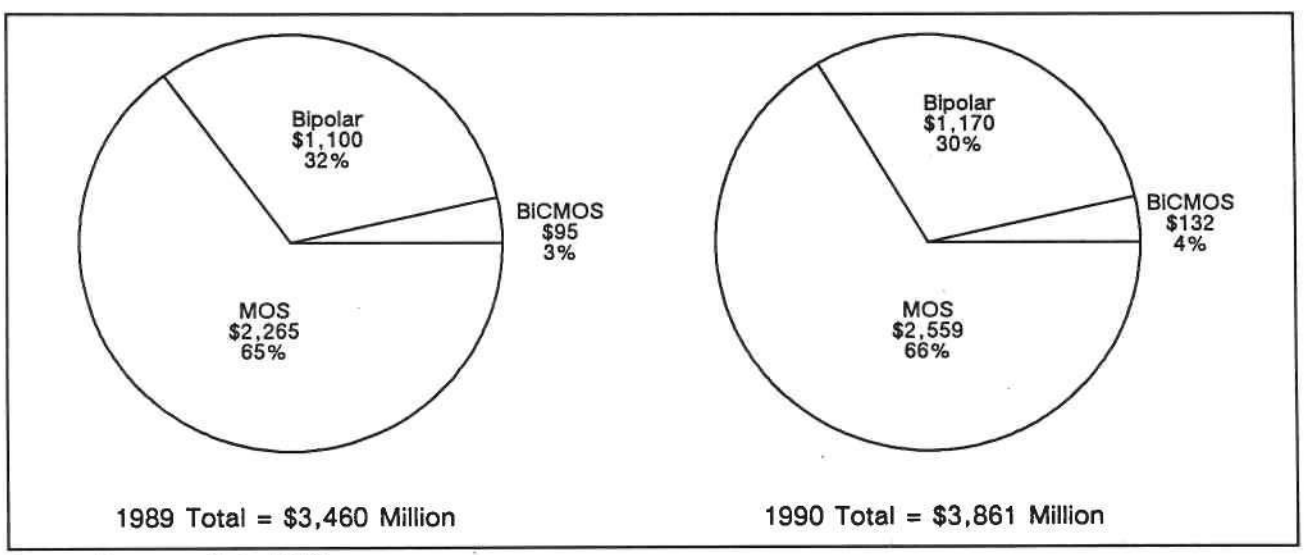


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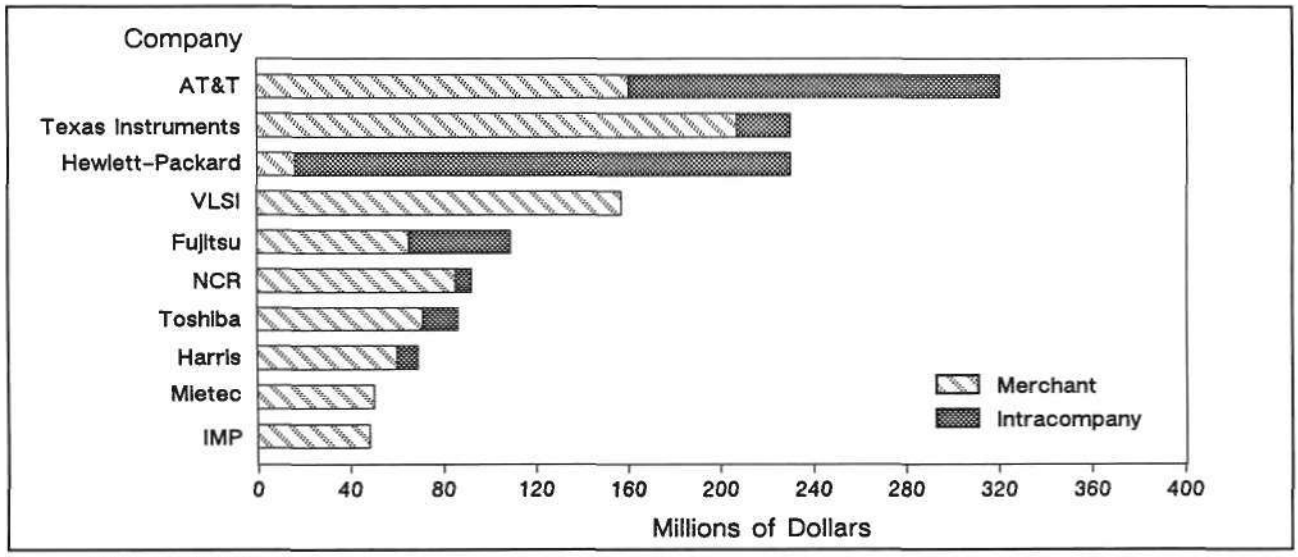
FIGURE 5
Top 10 CBIC Suppliers Worldwide—1990



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in capturing a significant chunk of merchant CBIC revenue by securing business from Western Digital. When AT&T eventually takes over NCR, the addition of that company's merchant CBIC business will make AT&T the number one CBIC supplier in the merchant market. Although suppliers such as Fujitsu, NEC, and Toshiba are not as prominent in the CBIC arena as in the gate array market, Dataquest expects to see them work aggressively to increase their penetration in this market. Already Fujitsu and Toshiba have captured solid business in this arena by focusing on applications including video games, printers, hard disk drives, and instrumentation. Finally, Mietec, a European company, is noteworthy because it is the only supplier with substantial BiCMOS CBIC revenue.

Programmable Logic Devices

Although representing the smallest portion of the ASIC market, the PLD market is receiving much attention. The dynamics of this market are such that the traditional bipolar PLD market continues to decline, whereas CMOS continues to make inroads. This represents an opportunity for a host of small companies to offer replacement CMOS parts and enter the market with new and innovative PLD architectures.

The number one supplier to the CMOS PLD market in 1990 was Xilinx with its FPGA products. Altera and Lattice ranked second and third, respectively, in the CMOS market. They are prominent suppliers of simple CMOS PLDs and are offering (or will be offering) complex PLD products. Although the gate array market is dominated by Japan-based suppliers, which are also strengthening their portfolios to compete more aggressively in CBICs, the PLD market is solidly commanded by U.S.-based companies. This dominance can be seen from Figure 6, which depicts the top 10 suppliers to this market.

In 1990, the CMOS portion of the PLD market grew so rapidly, it almost caught up with the bipolar market. CMOS PLD revenue amounted to $405 million in 1990 compared with bipolar's $423 million. This year, 1991, represents the crossover point when CMOS will overtake bipolar shipments.

FIGURE 6
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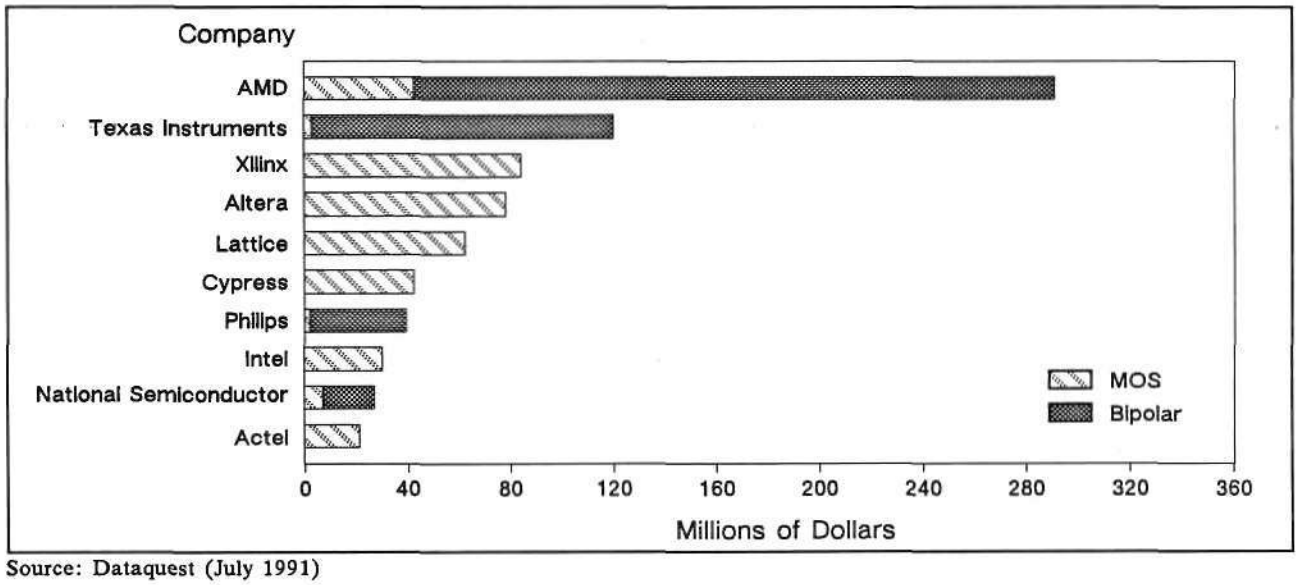

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DATAQUEST PERSPECTIVE

Low-end gate arrays have been described as the ultimate commodity in terms of silicon availability. Certainly the cutthroat pricing in the CMOS arena is testimony to a commodity pricing profile. Dataquest believes that the area of greatest opportunity in gate arrays will be embedded gate arrays (i.e., megacells such as static RAM and selected microperipherals that are diffused in the array base wafer). We view these devices as representing a future trend that will impact the CBIC arena. We continue to believe that gate arrays will remain the dominant ASIC technology throughout the decade.

Yet the CBIC market will continue to evolve. In applications demanding the highest performance and/or the greatest level of customization flexibility, we believe that CBIC will be the preferred solution over gate arrays. In fact, as the traditional handcrafted, full-custom portion of the ASIC market continues to decline, much of this business will continue to migrate into the CBIC camp. CBIC libraries and tools are infiltrating many standard product groups in large, broad-based IC suppliers so that by the mid-1990s, nearly all standard logic products should be developed using some form of ASIC design methodology.

In the never-ending challenge to meet time-to-market constraints, PLDs are providing the ideal vehicle and thus are eating away at the low end of the gate array market. As complex PLDs such as programmable multilevel logic devices and field programmable gate arrays increase in density, they will capture a greater share of the gate array market, especially as they charge down the learning curve.

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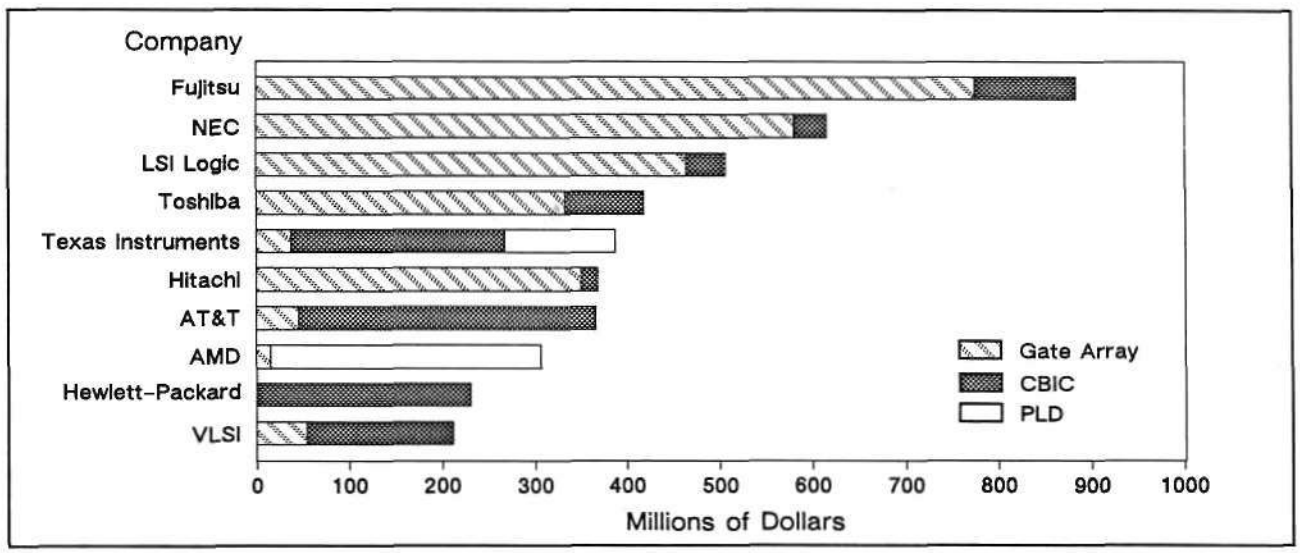
FIGURE 1
Top 10 ASIC Suppliers—1990



Source: Dataquest (July 1991)

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For example, National Semiconductor fell from the top 10 rankings in 1990 because, in attempting to compete head-on in the low-density, low-margin commodity CMOS gate array business, it was at a competitive disadvantage with vertically integrated ASIC suppliers that could amortize their ASIC costs over both their internal system business and their merchant ASIC business.

PRODUCT OVERVIEW

Gate Arrays

The worldwide ASIC market grew approximately 12 percent over 1989 to $9.27 billion. Figure 2 presents the composition of the ASIC market by product and shows that gate arrays continue to dominate the market.

For gate arrays, 1990 was a year that yielded few surprises. Generally, the year can be characterized as exhibiting modest growth with the strong growing stronger and a significant segment of suppliers experiencing very tough times. Dataquest's final market share data show the gate array market growing by almost 12 percent over 1989. Figure 3 shows the picture in terms of supplier rankings. The market share rankings remained essentially unchanged from the previous year with the exception of the new conglomerate, GEC/Plessey/MEDL, switching places with Oki in the lineup. Fujitsu, the market leader, expanded its revenue by 25 percent over the prior year. Gains in the company's ECL gate array business for use in testers and very high end computer systems contributed significantly to this strong performance.

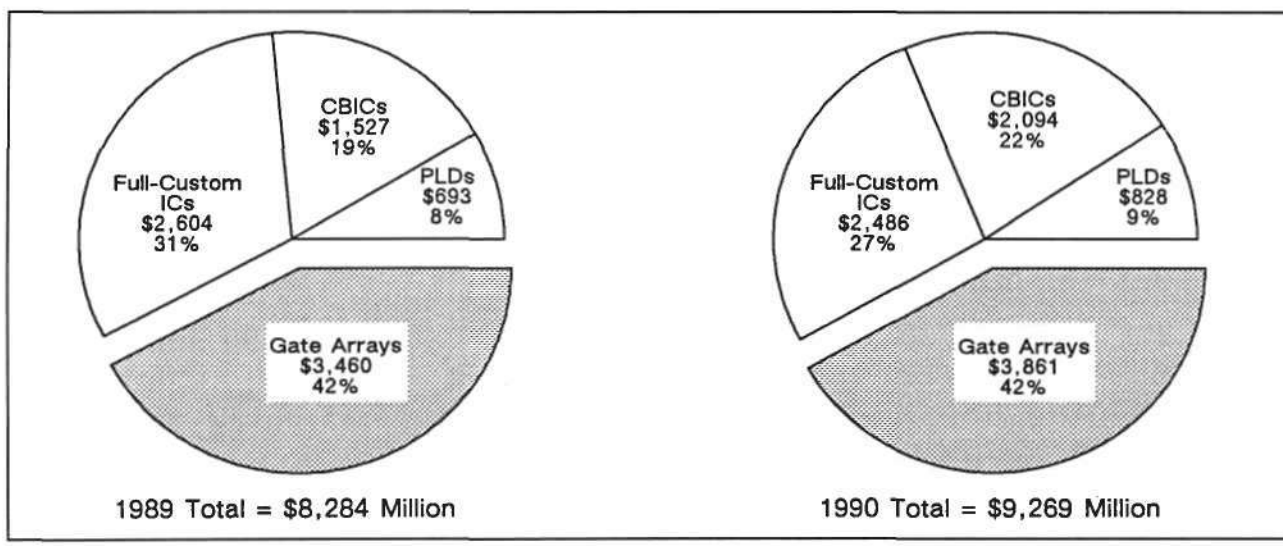
Figure 4 compares worldwide gate array consumption between 1990 and 1989 from a technology perspective. MOS gate arrays grew by 13 percent, whereas bipolar gate arrays grew a mere 6 percent. Meanwhile, growth in the BiCMOS arena significantly picked up. Indeed, the BiCMOS market grew by 40 percent in 1990. NEC, Fujitsu, and Hitachi are the only companies at this time with any significant revenue in this process category.

Cell-Based ICs

Although a 37 percent increase in CBIC revenue in 1990 over 1989 might seem to point to a very rapidly growing market, the jump in revenue stems from Hewlett-Packard's entry into the merchant CBIC market in 1990. For purposes of comparison, if we take out HP's $230 million contribution to the market, the corresponding growth rate of 22 percent is more in keeping with our forecast. Figure 5 represents the top 10 CBIC suppliers in terms of merchant and captive sales.

AT&T's combined internal and merchant CBIC business places the company first in the CBIC rankings. AT&T has been attempting to increase its merchant share of CBIC revenue. Indeed, in 1990, the company succeeded

FIGURE 2
Worldwide ASIC Consumption by Product



Source: Dataquest (July 1991)

FIGURE 3
Top 10 Worldwide Gate Array Suppliers—1990

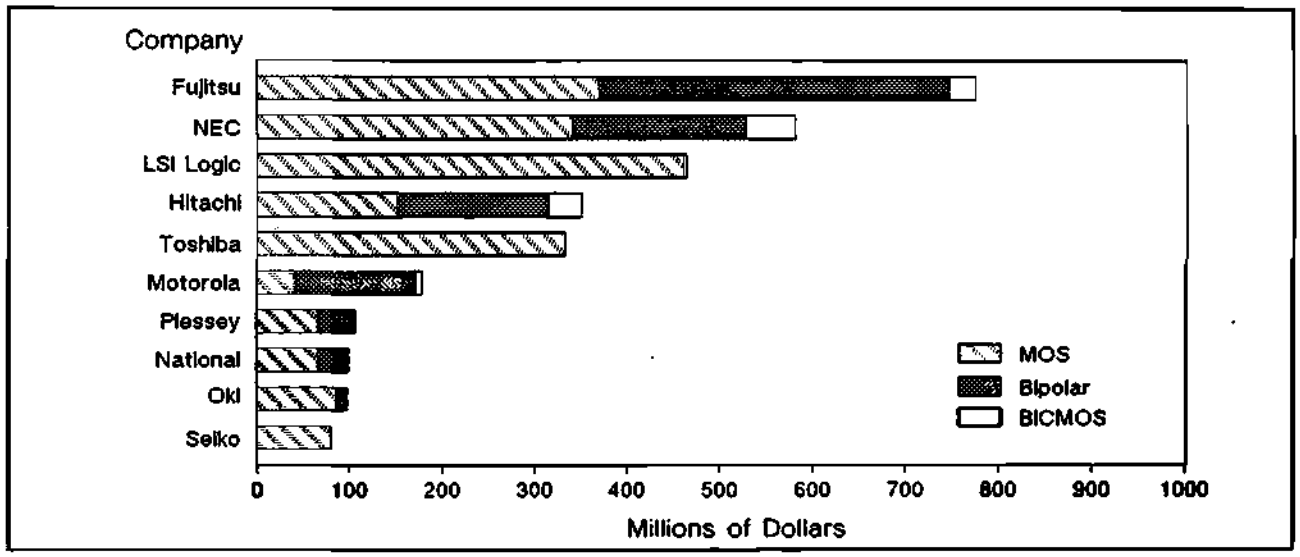


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FIGURE 4
Worldwide Gate Array Consumption by Technology

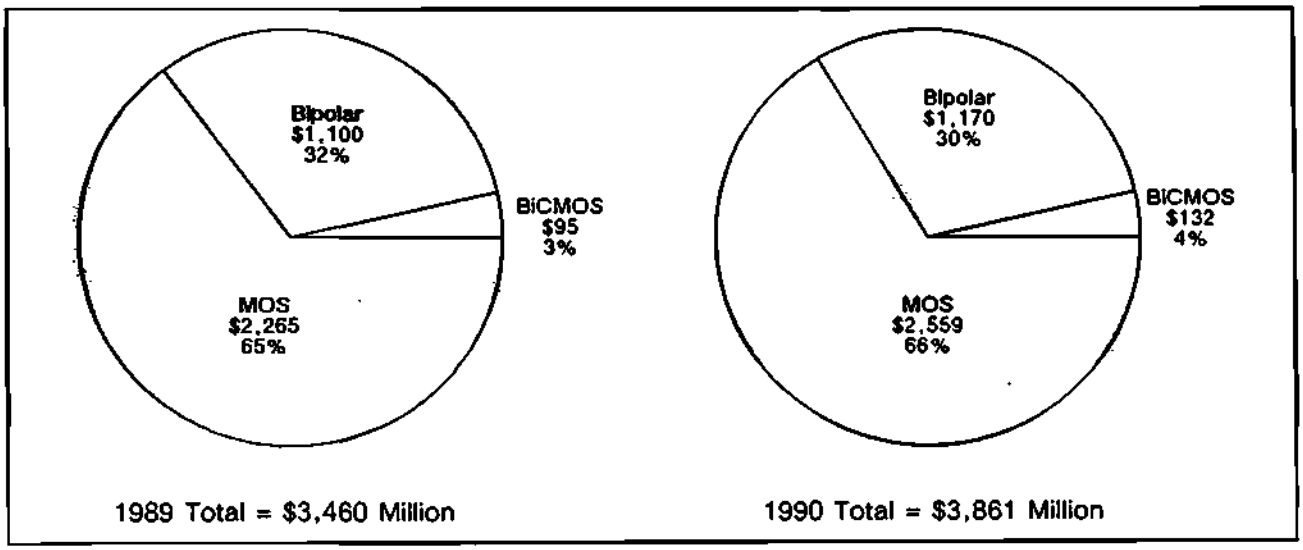

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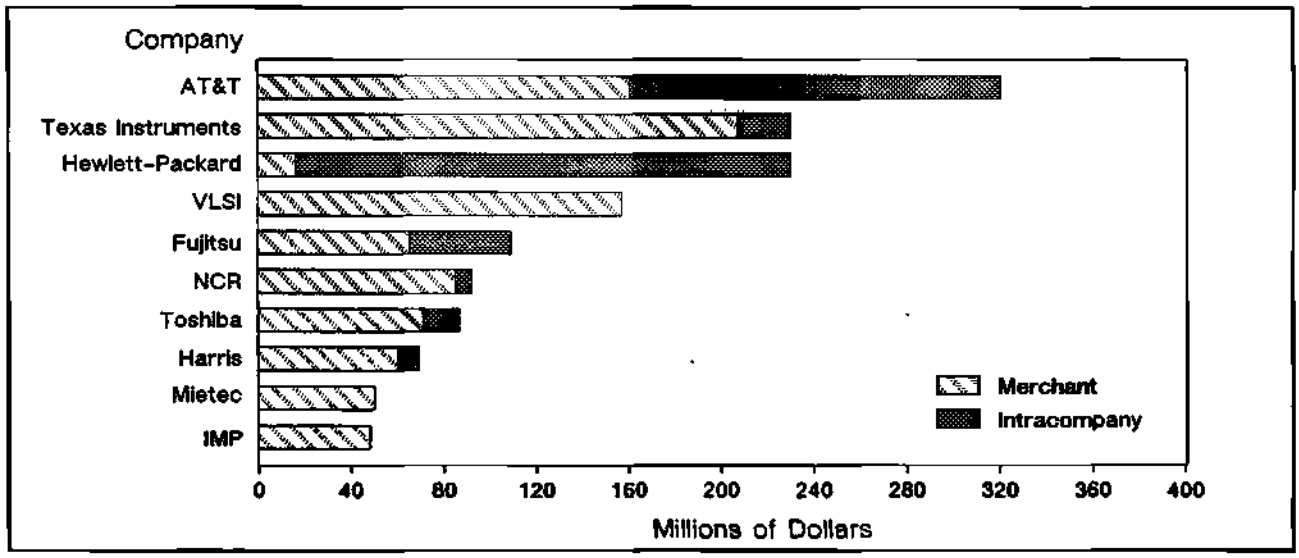
FIGURE 5
Top 10 CBIC Suppliers Worldwide—1990



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in capturing a significant chunk of merchant CBIC revenue by securing business from Western Digital. When AT&T eventually takes over NCR, the addition of that company's merchant CBIC business will make AT&T the number one CBIC supplier in the merchant market. Although suppliers such as Fujitsu, NEC, and Toshiba are not as prominent in the CBIC arena as in the gate array market, Dataquest expects to see them work aggressively to increase their penetration in this market. Already Fujitsu and Toshiba have captured solid business in this arena by focusing on applications including video games, printers, hard disk drives, and instrumentation. Finally, Mietec, a European company, is noteworthy because it is the only supplier with substantial BiCMOS CBIC revenue.

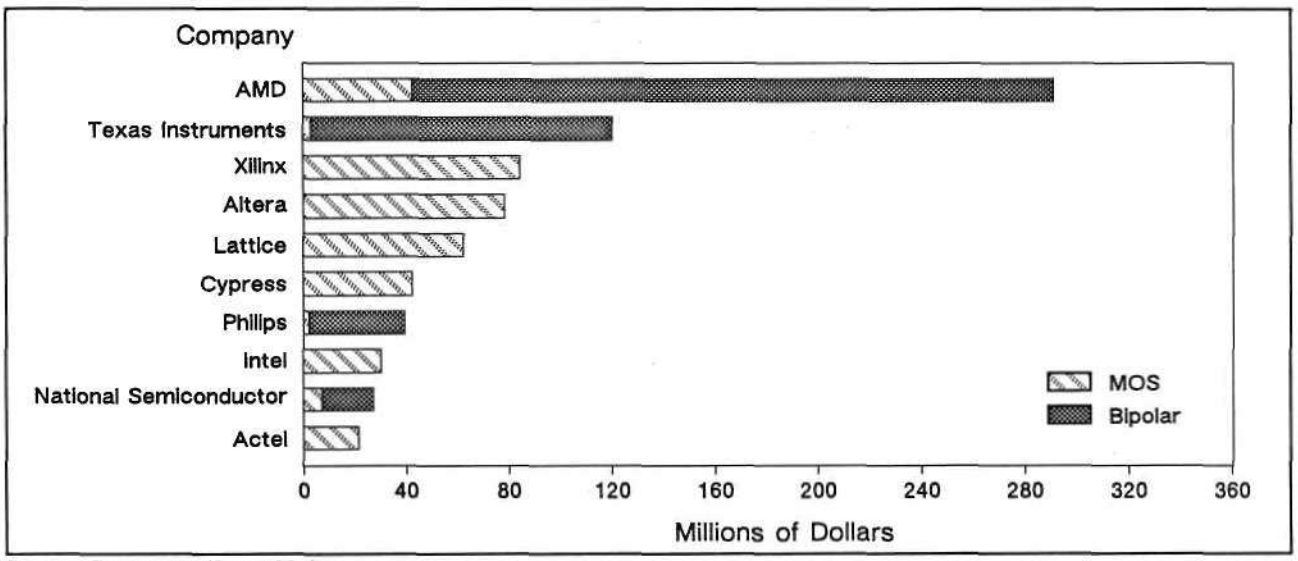
Programmable Logic Devices

Although representing the smallest portion of the ASIC market, the PLD market is receiving much attention. The dynamics of this market are such that the traditional bipolar PLD market continues to decline, whereas CMOS continues to make inroads. This represents an opportunity for a host of small companies to offer replacement CMOS parts and enter the market with new and innovative PLD architectures.

The number one supplier to the CMOS PLD market in 1990 was Xilinx with its FPGA products. Altera and Lattice ranked second and third, respectively, in the CMOS market. They are prominent suppliers of simple CMOS PLDs and are offering (or will be offering) complex PLD products. Although the gate array market is dominated by Japan-based suppliers, which are also strengthening their portfolios to compete more aggressively in CBICs, the PLD market is solidly commanded by U.S.-based companies. This dominance can be seen from Figure 6, which depicts the top 10 suppliers to this market.

In 1990, the CMOS portion of the PLD market grew so rapidly, it almost caught up with the bipolar market. CMOS PLD revenue amounted to $405 million in 1990 compared with bipolar's $423 million. This year, 1991, represents the crossover point when CMOS will overtake bipolar shipments.

FIGURE 6
Top 10 PLD Suppliers Worldwide—1990



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DATAQUEST PERSPECTIVE

Low-end gate arrays have been described as the ultimate commodity in terms of silicon availability. Certainly the cutthroat pricing in the CMOS arena is testimony to a commodity pricing profile. Dataquest believes that the area of greatest opportunity in gate arrays will be embedded gate arrays (i.e., megacells such as static RAM and selected microperipherals that are diffused in the array base wafer). We view these devices as representing a future trend that will impact the CBIC arena. We continue to believe that gate arrays will remain the dominant ASIC technology throughout the decade.

Yet the CBIC market will continue to evolve. In applications demanding the highest performance and/or the greatest level of customization flexibility, we believe that CBIC will be the preferred solution over gate arrays. In fact, as the traditional handcrafted, full-custom portion of the ASIC market continues to decline, much of this business will continue to migrate into the CBIC camp. CBIC libraries and tools are infiltrating many standard product groups in large, broad-based IC suppliers so that by the mid-1990s, nearly all standard logic products should be developed using some form of ASIC design methodology.

In the never-ending challenge to meet time-to-market constraints, PLDs are providing the ideal vehicle and thus are eating away at the low end of the gate array market. As complex PLDs such as programmable multilevel logic devices and field programmable gate arrays increase in density, they will capture a greater share of the gate array market, especially as they charge down the learning curve.

Bryan Lewis
Patricia Galligan
Ron Collett

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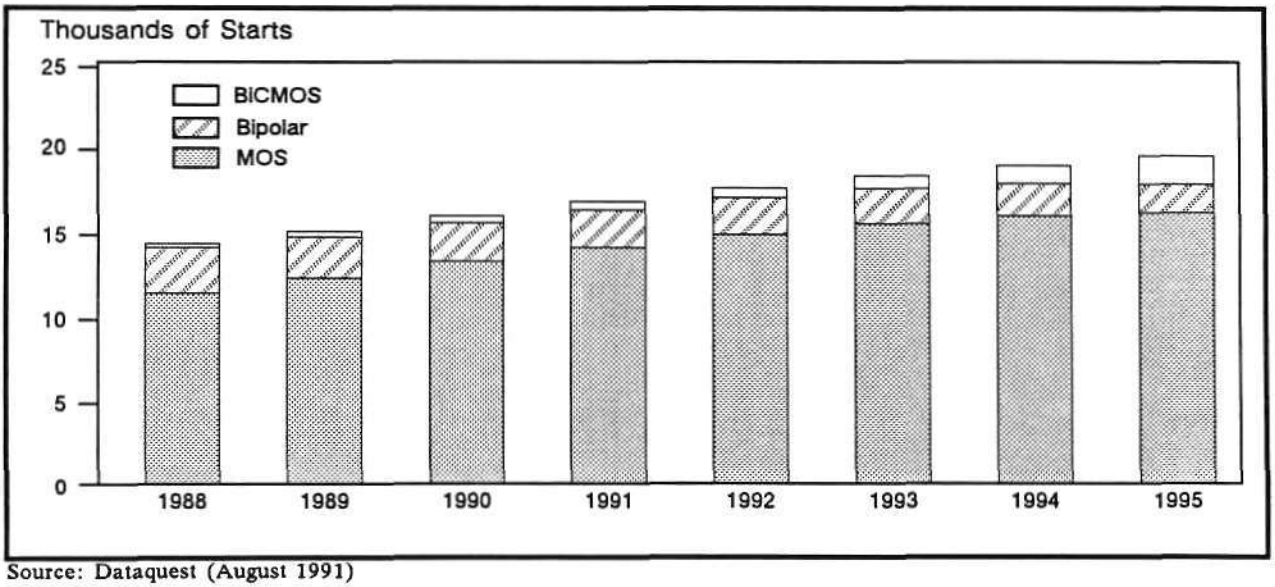
Research Newsletter

SEARCHING FOR ADDED-VALUE OPPORTUNITY AS ASIC MARKET DYNAMICS SHIFT

The ASIC market has begun to stall. Primary indicators of the ASIC business are profitability and design starts—both are slowing (see Figure 1). The ASIC market appears to be going through a stage of metamorphosis. Dataquest believes that the market is waiting for ASIC vendors to transform from chip suppliers to what we call "system solution" suppliers. Becoming a system solution supplier demands that chip vendors be capable of delivering (but not necessarily creating) a more diversified portfolio of products and services to the customer. In short, ASIC suppliers of the future must share in the burden of the entire system development.

To meet this challenge, it will be crucial for ASIC suppliers to gain a far better understanding of the system manufacturers' complete design requirements. These include design flow, functional elements of the system, interaction among functional elements, system interconnect requirements and constraints, system packaging, and system testing. The days when ASIC suppliers could simply maintain an arm's length relationship with the system design market are finished. ASIC suppliers must add value on the system level if they are to be profitable in the future. To do so, they must put in place organizations that can quickly respond to the changing dynamics of the electronic design market.

FIGURE 1
Estimated Worldwide Gate Array and CBIC Design Starts by Technology



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This newsletter examines the following:

- ASIC design start activity
- Future impact of ASSPs and FPGAs on the ASIC business
- Future directions ASIC suppliers should take

WHERE HAVE ALL THE DESIGN STARTS GONE?

Today, profit margins are razor thin for low-complexity ASICs because of the vast number of suppliers and the continuous encroachment of substitute products, namely, field-programmable gate arrays (FPGAs) and application-specific standard products (ASSPs) or chip sets. Not only have these products impacted profit margins, they have also worked to slow the ASIC design start growth. Dataquest's preliminary estimates show that there were over of 20,000 FPGA designs captured during 1990 compared with only 16,000 total gate array and CBIC designs. The FPGA market alone grew 92 percent from $61 million during 1989 to $117 million in 1990. Logic and graphic chip sets combined have reached an astounding $1 billion in just five years. These products have and will continue to impact the ASIC market.

Increasing chip density is another source acting to slow design start activity. For example, five 20,000-gate chips are rapidly becoming one 100,000-gate chip. Thus, five design starts are becoming one.

Figure 1 illustrates the projected growth of worldwide gate array and CBIC design starts.

DESIGN STARTS BY TECHNOLOGY, REGION, AND PRODUCT

The growth in design starts varies by process technology, by region of the world, and by product.

Figure 1 shows that bipolar design starts will continue to decline, CMOS design start growth is flattening out, and BiCMOS designs are growing, with strong growth expected in the mid- to late 1990s.

Although design start activity throughout the world is slowing, Japan has the highest growth rate followed by Rest of World countries, Europe, and North America, which has close to flat growth. FPGAs and chip sets are having the most pervasive impact on ASIC design starts in North America, hence the low growth rate.

Figure 2 illustrates gate array and CBIC design starts. Table 1 shows Dataquest's worldwide design start forecast by technology and product.

Assumptions

Key assumptions incorporated in the design start forecast include the following:

- A design start is counted when a prototype is delivered. On average, approximately 50 percent of the designs go to volume production.
- Captive design activity from pure captives that do not sell ASICs to the merchant market (e.g., IBM, DEC, and Unisys) are excluded from this forecast (Dataquest estimates the total 1990 captive ASIC designs to be 2,000 to 3,000).
- Bipolar design start growth (ECL) will continue declining because of its high cost and high power consumption and will be replaced by BiCMOS, CMOS, and GaAs ASICs.
- BiCMOS growth will increase in the mid- to late 1990s as large, vertically integrated semiconductor manufacturers such as Fujitsu, NEC, and AT&T begin incorporating them into their system products, which, in turn, will drive the product down the price learning curve.
- ASIC chip density will rise at an increasing rate because of increasing on-chip functions such as SRAM and the increasing reuse of soft megacells based on hardware description languages (HDLs) such as Verilog HDL and VHDL.
- Embedded gate arrays (i.e., megacells such as static SRAM that are diffused in the array base wafer) are included in the gate array category and are expected to experience a high growth rate by the mid-1990s.
- CBIC design start growth will be higher than gate array growth over the next few years because of increasing demand for CBICs in telecom, mixed-analog/digital devices, high-performance circuits, and high-volume applications.
- FPGAs and ASSPs will continue to experience rapid proliferation and will further reduce the growth of gate array and CBIC design starts.

FIGURE 2
Estimated Worldwide ASIC Design Starts by Product

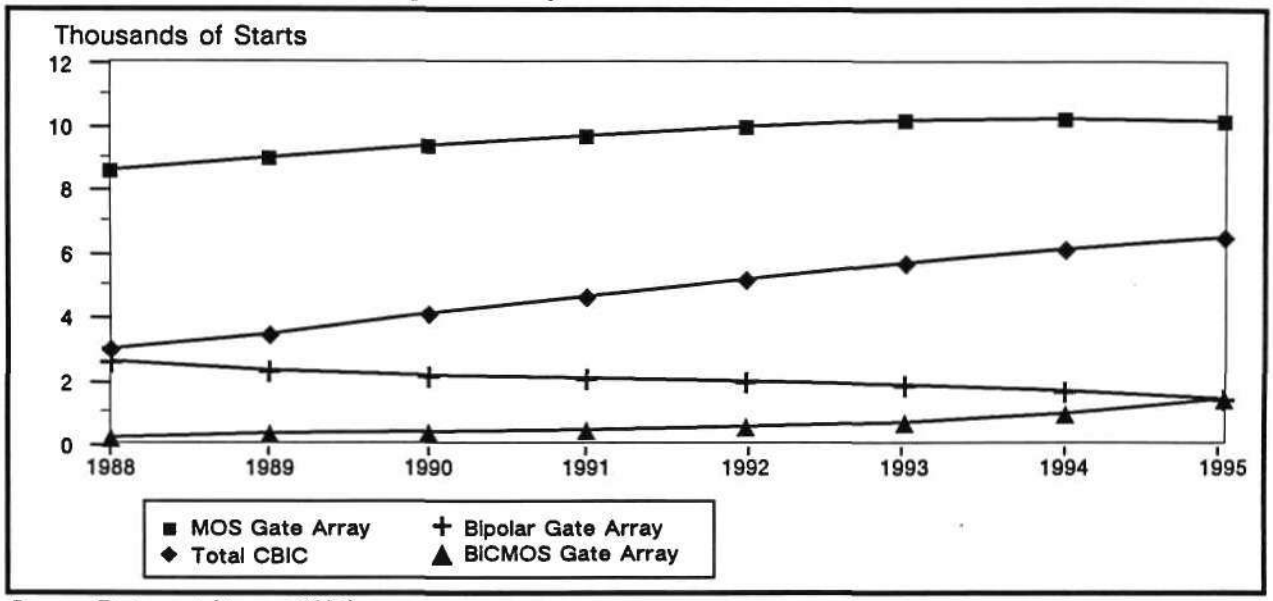

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TABLE 1
Estimated Worldwide Gate Array and CBIC Design Starts

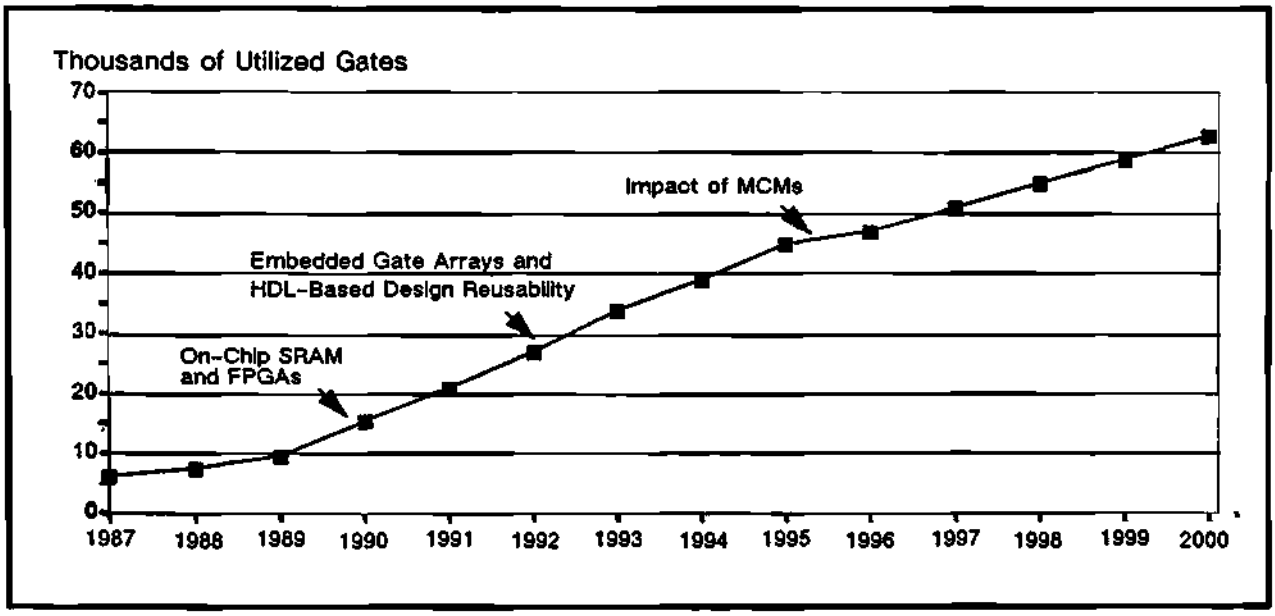
	1987	1988	1989	1990	1991	1992	1993	1994	1995
Total Gate Array and CBIC	13,229	14,335	15,066	15,970	16,811	17,622	18,320	18,945	19,489
MOS Gate Array and CBIC	10,506	11,448	12,294	13,297	14,123	14,897	15,523	15,963	16,179
Bipolar Gate Array and CBIC	2,637	2,694	2,432	2,279	2,215	2,138	2,050	1,890	1,657
BiCMOS Gate Array and CBIC	86	193	340	394	473	587	747	1,092	1,653
Total Gate Array	10,689	11,355	11,614	11,877	12,174	12,456	12,655	12,830	12,993
MOS Gate Array	8,078	8,601	8,998	9,390	8,708	9,996	10,181	10,247	10,178
Bipolar Gate Array	2,539	2,583	2,307	2,135	2,047	1,943	1,825	1,643	1,405
BiCMOS Gate Array	72	171	309	352	419	517	649	940	1,410
Total CBIC	2,540	2,980	3,452	4,093	4,637	5,166	5,665	6,115	6,496
MOS CBIC	2,428	2,847	3,296	3,907	4,415	4,901	5,342	5,716	6,001
Bipolar CBIC	98	111	125	144	167	195	225	247	252
BiCMOS CBIC	14	22	31	42	55	70	98	152	243

Source: Dataquest (August 1991)

Increasing Density

As mentioned earlier, a key reason behind the slowing of worldwide ASIC design start growth is that ASIC chip density is climbing at an increasing rate. As Figure 3 illustrates, the average number of utilized gates per MOS gate array design in North America during 1988 was 7,700, in 1989 it was 9,900 and in 1990 it was estimated to be 15,500. The primary reason for the big jump in 1990 gate counts was due to increasing use of on-chip SRAM. During 1989, 13 percent of MOS gate array design starts had on-chip SRAM compared with 21 percent in 1990. Furthermore, the average size of on-chip gate array SRAM increased from 2Kb in 1989 to 4Kb in 1990. An increasing number of gate array designs also had on-chip micro-peripherals and SCAN path logic, which also increased the average 1990 gate count.

FIGURE 3
Estimated North American Average MOS Gate Array Design Starts by Gate Count



Source: Dataquest (August 1991)

Looking forward, Dataquest believes that larger SRAMs (128Kb and 256Kb) will be diffused in the gate array base wafers and used for cache memory. Other functions such as SCSI, ALU, multiplier, multiplier-accumulator, FIFO, DMA controller, cache controller, and 82XX microperipherals will also be diffused in the gate array and drive average gate counts upward.

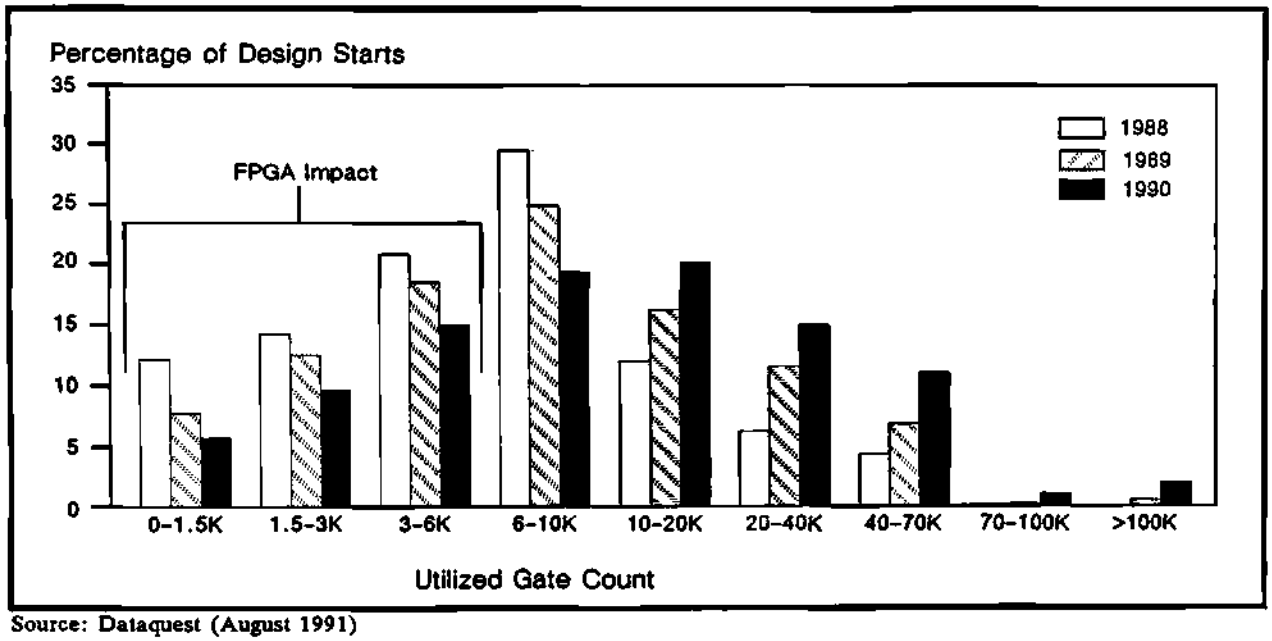
Dataquest also believes that there will be an increasing trend toward design reusability, which will push gate counts significantly higher than they have been in the past. ASIC designers will describe logic functions in VHDL or Verilog HDL, and the HDL functions then will be archived. Designers will retrieve these functions and reuse them on subsequent designs. We believe that functions will include both LSI and VLSI functions.

Dataquest expects multichip modules (MCMs) to temporarily stall average gate counts in the 1995 time frame. In Dataquest's view, MCMs will be moving quickly down the price learning curve by 1995 and, thus, are expected to become attractive for a wide range of applications. For many applications, it will more cost effective, for example, to put four 50,000-gate chips in an MCM compared with one 200,000-gate chip without losing much system performance. MCMs also offer a solution to the problem of high-gate-count ASICs having a limited number on bonding pads. With an MCM, a high-gate-count ASIC can be divided into multiple ASICs to more closely match individual device gate counts to I/O requirements. We expect the I/O problem to intensify over the next five years. Our belief stems from the fact that fabrication process technology developments (e.g., feature size reductions) are drastically outpacing corresponding reductions in pad pitch.

Encroaching Products

FPGAs are also having a dramatic impact on the growth of gate array design starts. Dataquest estimates that the installed base of FPGA development systems surpassed 10,000 units by the end of 1990. If each system were used for two designs per year (a conservative estimate), that would equal 20,000 total FPGA designs. This is not to suggest that either gate arrays would have been used for all of these designs or that the dollar market for FPGAs is larger than the gate array market; of course, it is not. The gate array market was $3.9 billion in 1990 compared with a $117 million market for FPGAs. Rather, it is clear that FPGAs are capturing many sockets that at one time would have been exclusively reserved for gate arrays. FPGAs are affecting low-density/low-volume gate array designs today; they will impact

FIGURE 4
Estimated North American MOS Gate Array Design Starts by Gate Count



Source: Dataquest (August 1991)

medium-density/medium-volume gate array designs in the future.

Today, most FPGAs are used for prototyping or applications that require less than 5,000 units for the life of the design. Furthermore, most of the FPGAs captured to date have less than 5,000 equivalent gate array gates. Figure 4 illustrates the impact that FPGAs have had on MOS gate array design starts in North America.

While FPGAs are attacking low-volume applications, chip sets and ASSPs are attacking high-volume applications. There have been several waves of application-specific chip sets to date. Among the most recent were logic and graphic chip sets, which in 1990 accounted for close to $700 million and $275 million, respectively. Another wave is well on the way—telecom/local area network chip sets. Other high-volume applications and products that Dataquest expects to be penetrated by application-specific chip sets include memory cards, multimedia including video compression, facsimile machines, laser printers, ISDN, and HDTV.

Dataquest believes that more high-volume gate array and CBIC applications will be recognized over the next five years and will be lost to chip sets. ASIC suppliers must complement their semicustom product lines by identifying ASSP market needs as early as possible and acting quickly to seize the opportunity. Time to market and/or including a high level of unique intellectual property will be the crucial elements necessary to achieve success in this business.

SUPPLIERS CHART NEW COURSES

It is clear that FPGAs will continue their assault on the low-end gate array market. Indeed, FPGAs will experience improvements in gate counts, speed, and price. As a result, FPGAs will gradually shift from the low-density market to today's midrange gate array market. Outflanking FPGAs will be a constant battle for ASIC suppliers. Many ASIC suppliers have resorted to dropping low-end gate array prices and further reducing prototype turnaround times to combat the FPGA onslaught. But this tactic struggles to come to terms with the changes in the paradigm—namely, that the definition of added value must change.

System knowledge is the critical element in offering added-value products. Knowing the entire system design flow and functional elements required for each type of system being targeted is crucial for successful ASIC suppliers of the 1990s.

ASIC suppliers must form close relationships with the systems design market to gain the necessary understanding of added value. Added value can come in many forms. Areas of opportunity include the following:

- Solving the test problem on both the IC and system level
- Offering new packages such as multichip modules
- Offering new high-performance/low-cost manufacturing processes
- Providing high-complexity megacells than can be diffused in gate array base wafers
- Reducing time to market
- Offering standard products that provide targeted system solutions

The ASIC market continues to evolve. The market will reward those suppliers that anticipate the changes and deliver added-value products and services.

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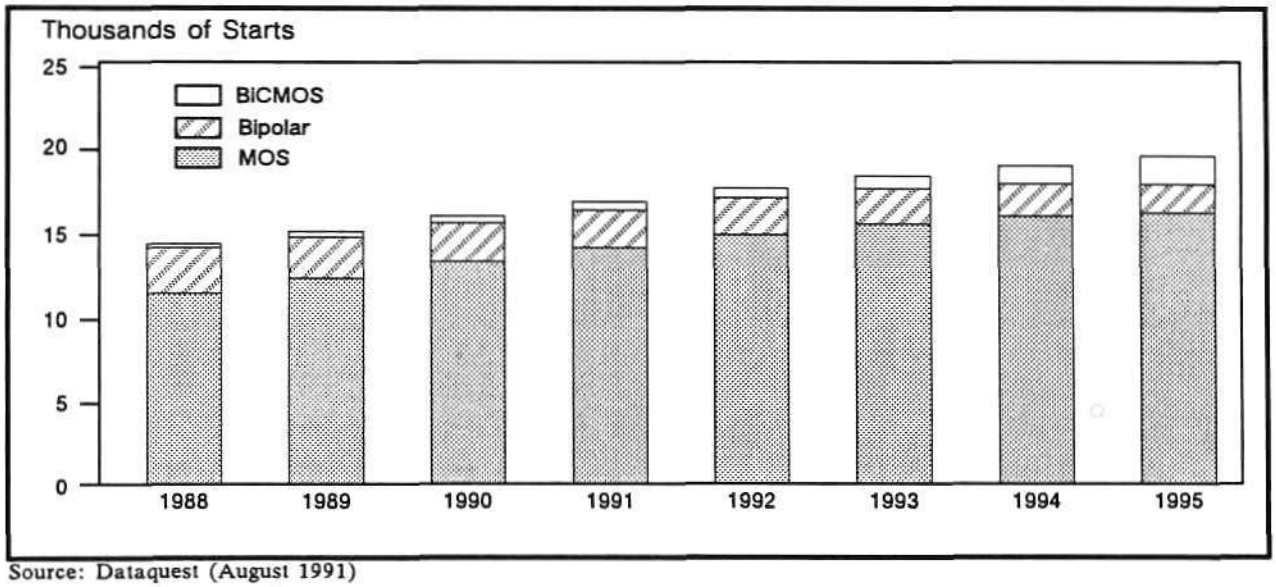

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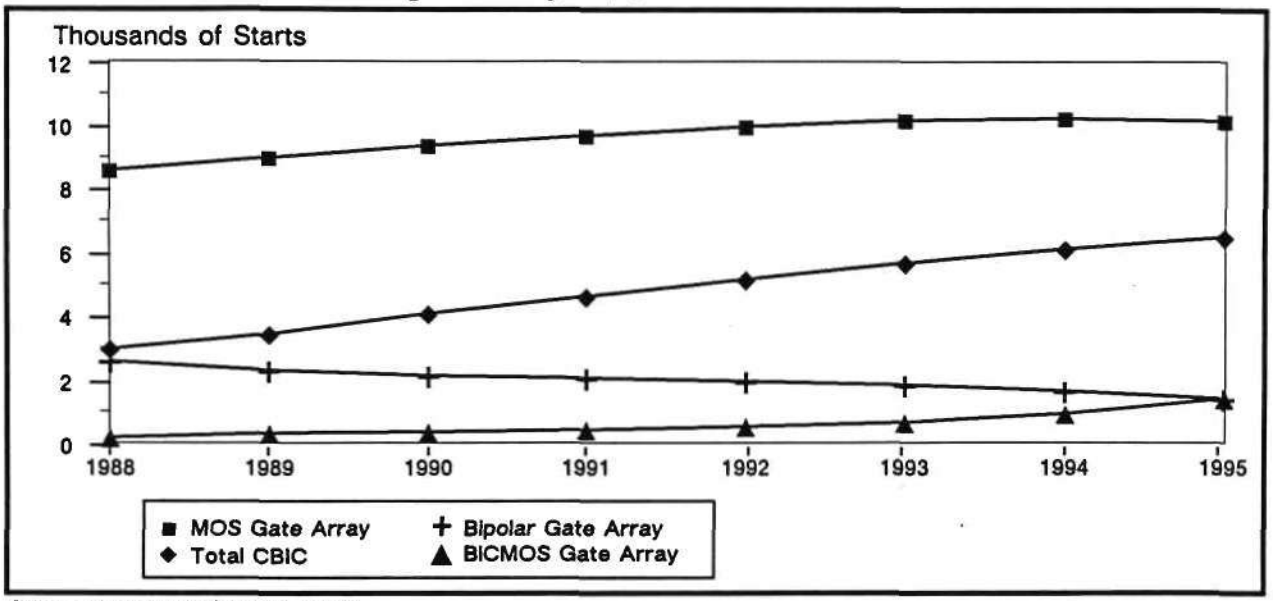

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Total CBIC	2,540	2,980	3,452	4,093	4,637	5,166	5,665	6,115	6,496
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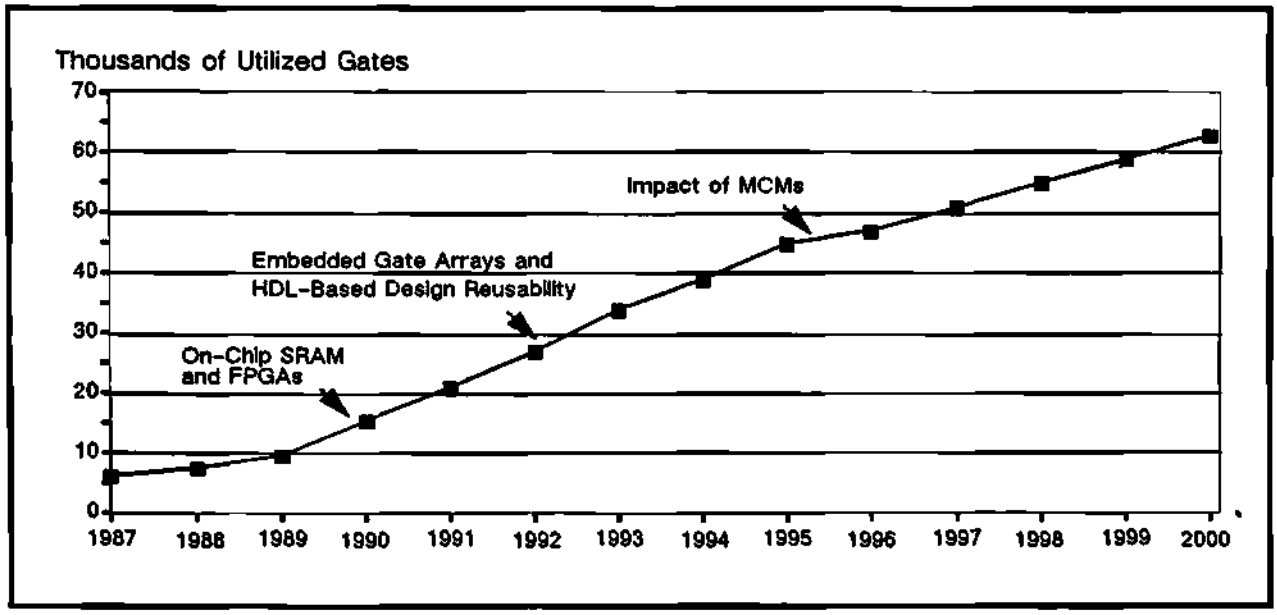
Source: Dataquest (August 1991)

Increasing Density

As mentioned earlier, a key reason behind the slowing of worldwide ASIC design start growth is that ASIC chip density is climbing at an increasing rate. As Figure 3 illustrates, the average number of utilized gates per MOS gate array design in North America during 1988 was 7,700, in 1989 it was 9,900 and in 1990 it was estimated to be 15,500. The primary reason for the big jump in 1990 gate counts was due to increasing use of on-chip SRAM. During 1989, 13 percent of MOS gate array design starts had on-chip SRAM compared with 21 percent in 1990. Furthermore, the average size of on-chip gate array SRAM increased from 2Kb in 1989 to 4Kb in 1990. An increasing number of gate array designs also had on-chip micro-peripherals and SCAN path logic, which also increased the average 1990 gate count.

FIGURE 3
Estimated North American Average MOS Gate Array Design Starts by Gate Count



Source: Dataquest (August 1991)

Looking forward, Dataquest believes that larger SRAMs (128Kb and 256Kb) will be diffused in the gate array base wafers and used for cache memory. Other functions such as SCSI, ALU, multiplier, multiplier-accumulator, FIFO, DMA controller, cache controller, and 82XX microperipherals will also be diffused in the gate array and drive average gate counts upward.

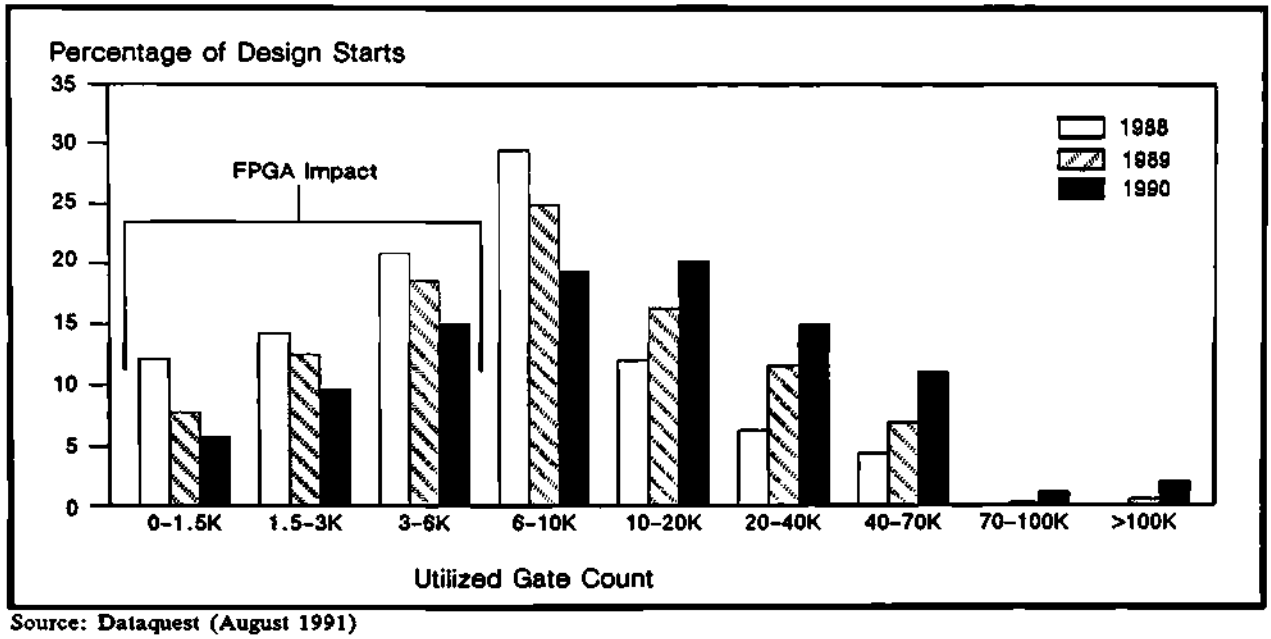
Dataquest also believes that there will be an increasing trend toward design reusability, which will push gate counts significantly higher than they have been in the past. ASIC designers will describe logic functions in VHDL or Verilog HDL, and the HDL functions then will be archived. Designers will retrieve these functions and reuse them on subsequent designs. We believe that functions will include both LSI and VLSI functions.

Dataquest expects multichip modules (MCMs) to temporarily stall average gate counts in the 1995 time frame. In Dataquest's view, MCMs will be moving quickly down the price learning curve by 1995 and, thus, are expected to become attractive for a wide range of applications. For many applications, it will more cost effective, for example, to put four 50,000-gate chips in an MCM compared with one 200,000-gate chip without losing much system performance. MCMs also offer a solution to the problem of high-gate-count ASICs having a limited number on bonding pads. With an MCM, a high-gate-count ASIC can be divided into multiple ASICs to more closely match individual device gate counts to I/O requirements. We expect the I/O problem to intensify over the next five years. Our belief stems from the fact that fabrication process technology developments (e.g., feature size reductions) are drastically outpacing corresponding reductions in pad pitch.

Encroaching Products

FPGAs are also having a dramatic impact on the growth of gate array design starts. Dataquest estimates that the installed base of FPGA development systems surpassed 10,000 units by the end of 1990. If each system were used for two designs per year (a conservative estimate), that would equal 20,000 total FPGA designs. This is not to suggest that either gate arrays would have been used for all of these designs or that the dollar market for FPGAs is larger than the gate array market; of course, it is not. The gate array market was $3.9 billion in 1990 compared with a $117 million market for FPGAs. Rather, it is clear that FPGAs are capturing many sockets that at one time would have been exclusively reserved for gate arrays. FPGAs are affecting low-density/low-volume gate array designs today; they will impact

FIGURE 4
Estimated North American MOS Gate Array Design Starts by Gate Count



Source: Dataquest (August 1991)

medium-density/medium-volume gate array designs in the future.

Today, most FPGAs are used for prototyping or applications that require less than 5,000 units for the life of the design. Furthermore, most of the FPGAs captured to date have less than 5,000 equivalent gate array gates. Figure 4 illustrates the impact that FPGAs have had on MOS gate array design starts in North America.

While FPGAs are attacking low-volume applications, chip sets and ASSPs are attacking high-volume applications. There have been several waves of application-specific chip sets to date. Among the most recent were logic and graphic chip sets, which in 1990 accounted for close to $700 million and $275 million, respectively. Another wave is well on the way—telecom/local area network chip sets. Other high-volume applications and products that Dataquest expects to be penetrated by application-specific chip sets include memory cards, multimedia including video compression, facsimile machines, laser printers, ISDN, and HDTV.

Dataquest believes that more high-volume gate array and CBIC applications will be recognized over the next five years and will be lost to chip sets. ASIC suppliers must complement their semicustom product lines by identifying ASSP market needs as early as possible and acting quickly to seize the opportunity. Time to market and/or including a high level of unique intellectual property will be the crucial elements necessary to achieve success in this business.

SUPPLIERS CHART NEW COURSES

It is clear that FPGAs will continue their assault on the low-end gate array market. Indeed, FPGAs will experience improvements in gate counts, speed, and price. As a result, FPGAs will gradually shift from the low-density market to today's midrange gate array market. Outflanking FPGAs will be a constant battle for ASIC suppliers. Many ASIC suppliers have resorted to dropping low-end gate array prices and further reducing prototype turnaround times to combat the FPGA onslaught. But this tactic struggles to come to terms with the changes in the paradigm—namely, that the definition of added value must change.

System knowledge is the critical element in offering added-value products. Knowing the entire system design flow and functional elements required for each type of system being targeted is crucial for successful ASIC suppliers of the 1990s.

ASIC suppliers must form close relationships with the systems design market to gain the necessary understanding of added value. Added value can come in many forms. Areas of opportunity include the following:

- Solving the test problem on both the IC and system level
- Offering new packages such as multichip modules
- Offering new high-performance/low-cost manufacturing processes
- Providing high-complexity megacells than can be diffused in gate array base wafers
- Reducing time to market
- Offering standard products that provide targeted system solutions

The ASIC market continues to evolve. The market will reward those suppliers that anticipate the changes and deliver added-value products and services.

Bryan Lewis
Ron Collett

Dataquest
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Dataquest Perspective

ASICs *Worldwide*

Vol. 1, No. 1 November 25, 1991

Product Analysis

DQ Feature—*Are System Designers Ready for the New Breed of CMOS Gate Arrays?*

ASIC suppliers throughout the industry are announcing CMOS gate array products with dramatically higher gate counts than the previous generation of products. Dataquest analyzes the 1990 CMOS gate array design start trends and projects the impact of the new gate array product offering.

By Bryan Lewis *Page 2*

ASIC Packaging Trends

As gate counts rise, new demands are placed on ASIC packages. Dataquest examines the packaging and pin-count trends for both MOS gate array and cell-based ICs.

By Bryan Lewis *Page 6*

Market Analysis

ASIC Applications Fuel Future Market Growth

Despite the fact that ASIC design start growth is slowing and profit margins are narrowing, ASIC revenue growth remains healthy. Increasing demand for ASICs is being driven by a range of high-growth application markets. Dataquest highlights the applications that ASIC vendors should be exploring and provides its gate array and CBIC application market forecasts.

By Bryan Lewis *Page 8*

Product Analysis

Are System Designers Ready for the New Breed of CMOS Gate Arrays?

The gun has sounded and the race has begun for the highest-density gate array. ASIC suppliers throughout the industry are announcing CMOS gate arrays with dramatically higher gate counts than the previous generation of products. Although these products will find their way into the market over the next five years, Dataquest believes that the bulk of the high-density design starts will not begin until the 1993 to 1994 time frame.

Table 1 ranks the top 15 worldwide CMOS gate array suppliers by their 1990 shipment revenue and lists their leading gate array products. Most of the suppliers to date have announced 0.8-micron three-layer metal products that can achieve utilized gate counts in excess of 100,000 gates and also incorporate diffused SRAM blocks.

Although it is important for leading suppliers to have a flagship product that can be used to demonstrate their technical capabilities, most of the 1990 design starts were in much less sophisticated products. Dataquest estimates that the average utilized design start gate count in North America was 15,500 gates during 1990, with only 3 percent of the designs greater than 100,000 gates. Furthermore, only 9 percent of the 1990 designs were triple metal and only 1 percent of the designs had diffused SRAM blocks.

1990 Design Starts by Gate Count

Figure 1 illustrates the distribution of 1989 and 1990 North American MOS gate array design starts by gate count. Dataquest analysis of this figure reveals the following important points:

- The most cost-effective gate count shifted from 6,000 to 10,000 gates in 1989 to 10,000 to 20,000 in 1990.
- PC/workstation designers are very cost sensitive; therefore, a large portion of their 1990 designs were in the 10,000- to 20,000-gate range.
- Midrange computer designers wanted more integration and higher performance than the PC/workstation designers; thus, a large portion of their 1990 designs were in the 40,000- to 70,000-gate range.

Table 1
Estimated Worldwide CMOS Gate Array Shipments and Leading Products

1990 Rank	Company	1990 ($M)	Leading Process (Drawn)	Maximum Gates (Gross)	Metal Layers	Maximum Gates (Usable)	Embedded Cells
1	LSI Logic	461.0	0.7	307K	3	200K	Yes
2	Fujitsu	369.0	0.8	200K	3	120K	Yes
3	NEC	340.0	0.8	250K	3	150K	Yes
4	Toshiba	332.0	0.8	302K	3	210K	Yes
5	Hitachi	150.0	0.8	250K	3	100K	?
6	Oki	86.0	0.8	231K	2	100K	Yes
7	Seiko	80.0	0.8	255K	2	102K	?
8	GEC Plessey	69.0	1.0	220K	3	150K	?
9	National Semiconductor	66.0	1.0	250K	3	125K	?
10	Matsushita	66.0	1.2	35K	2	30K	?
11	VLSI Technology	54.0	1.0	172K	3	125K	Yes
12	Motorola	41.0	1.0	318K	3	195K	Yes
13	Sharp	38.0	1.0	30K	2	15K	?
14	Mitsubishi	38.0	0.8	400K	3	250K	?
15	SGS-Thomson	35.0	0.7	288K	3	216K	?

Source: Dataquest (November 1991)

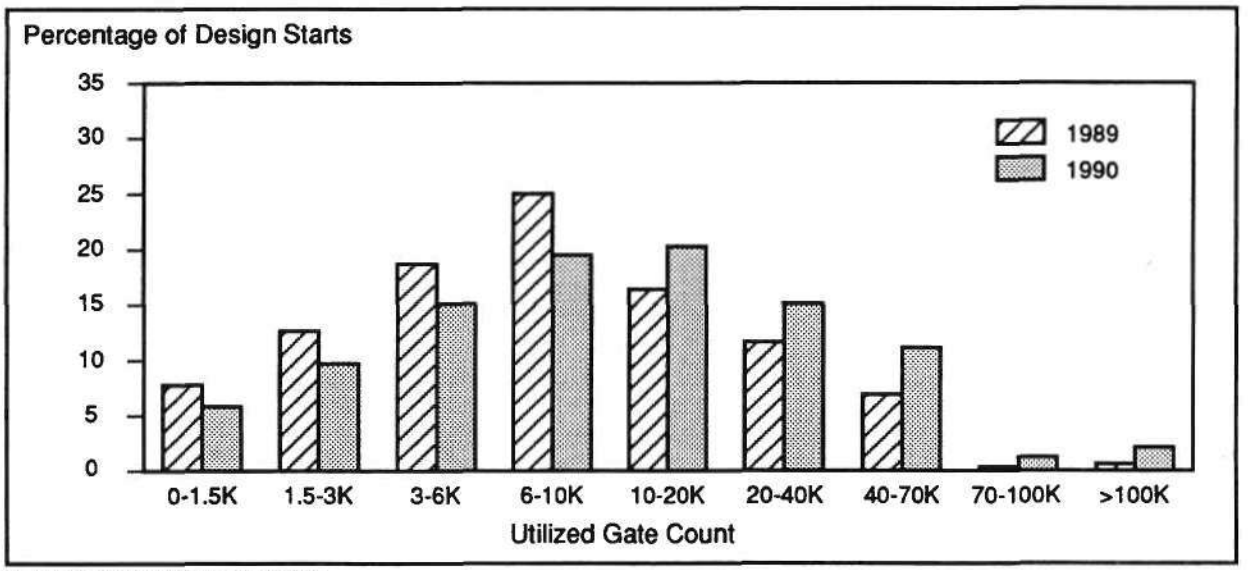
- Supercomputer and military applications require the ultimate in performance and integration; hence, these applications accounted for the majority of 1990 designs greater than 70,000 gates.

1990 Design Starts by Function

Figure 2 illustrates North American MOS gate array design starts by function. Figure 3 illustrates the percentage of North American MOS gate array designs starts that incorporated memory, by the number of bits. Dataquest's analysis from these figures is as follows:

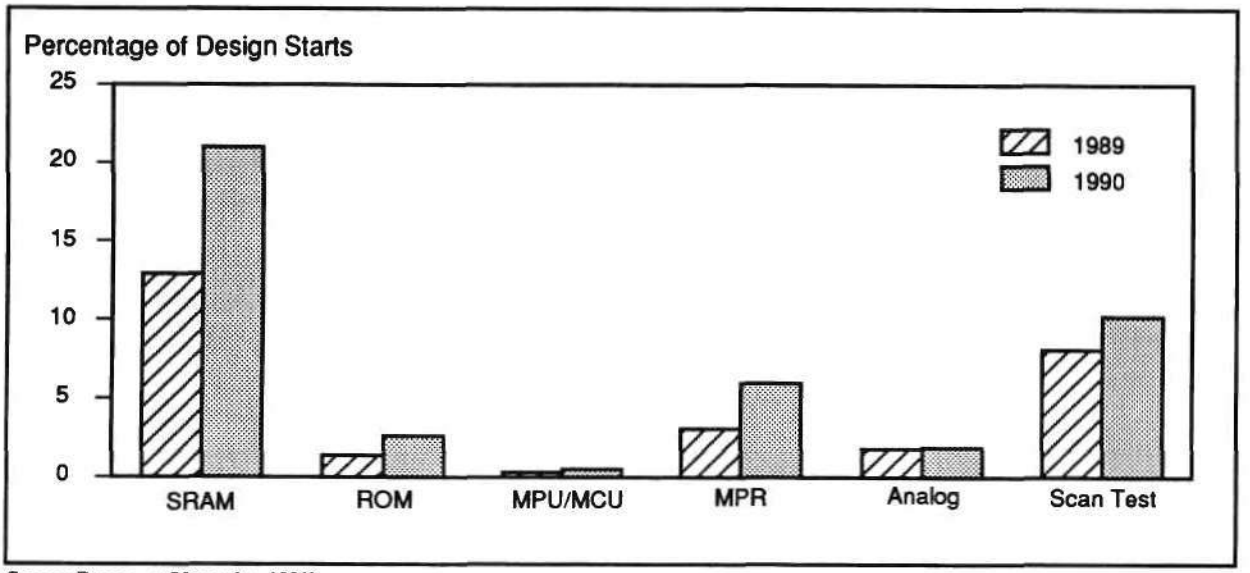
- Approximately 60 percent of the 1990 MOS gate array market comprises data processing applications, such as cache memory, which are driving the strong trend toward on-chip SRAM.

Figure 1
Estimated North American MOS Gate Array Design Starts by Gate Count



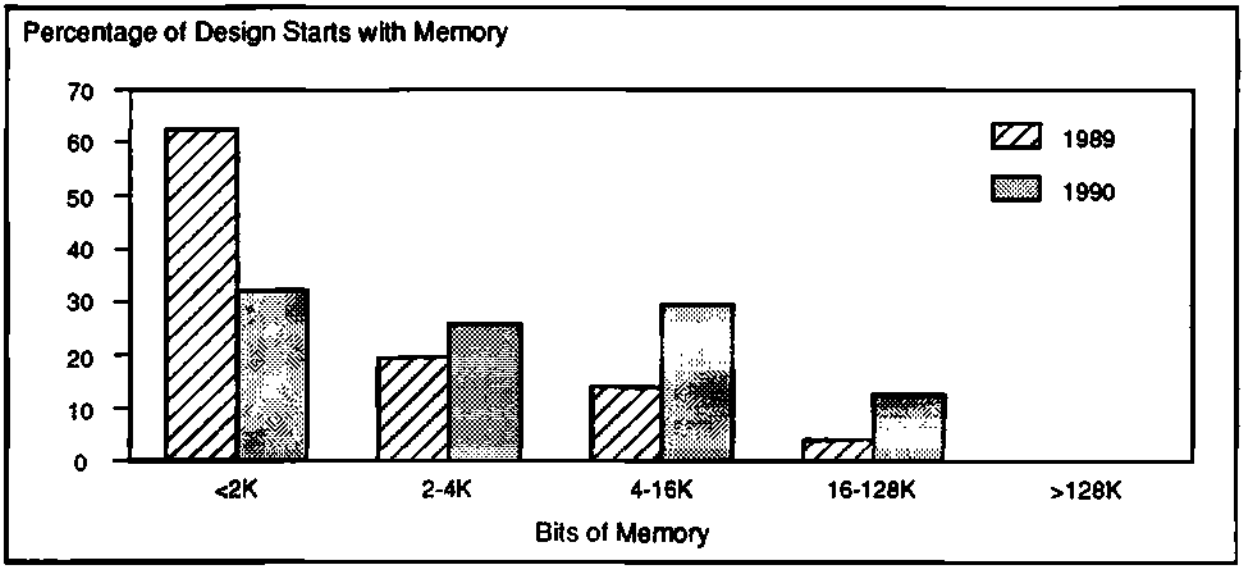
Source: Dataquest (November 1991)

Figure 2
Estimated North American MOS Gate Array Design Starts by Function



Source: Dataquest (November 1991)

Figure 3
Estimated North American MOS Gate Array Design Starts by Memory Bits



Source: Dataquest (November 1991)

- Only 5 percent of the 1990 memories were diffused in the base wafer (95 percent were metal-configured memories).
- ROM is not as cost-effective in a sea-of-gates architecture as in a CBIC product. Therefore, only 3 percent of the 1990 gate array design starts had on-chip ROM versus 15 percent of the 1990 CBIC designs.
- Most of the microprocessing units/microcontroller units (MPUs/MCUs) that have been incorporated in gate array designs to date have been CISC (that is, 80C51, 2901, and Z80). The advantages of on-chip CISC products (performance and footprint) in general are not great enough to offset the lower cost of just using a standard CISC product on a PC board in conjunction with gate arrays. The jury is still out as to whether RISC cores will have the same argument.
- Most of the microperipheral (MPR) functions incorporated in ASICs to date were 82XX peripherals.
- Analog functions are difficult to implement in logic gates. Therefore, most of the analog functions tracked to date have been implemented in pure analog arrays from companies such as GEC Plessey and Exar.
- As gate densities continue to rise at a rapid rate, on-chip test has become critical. JTAG compatibility also is emerging as the industry standard for board-level testing.

Dataquest Perspective

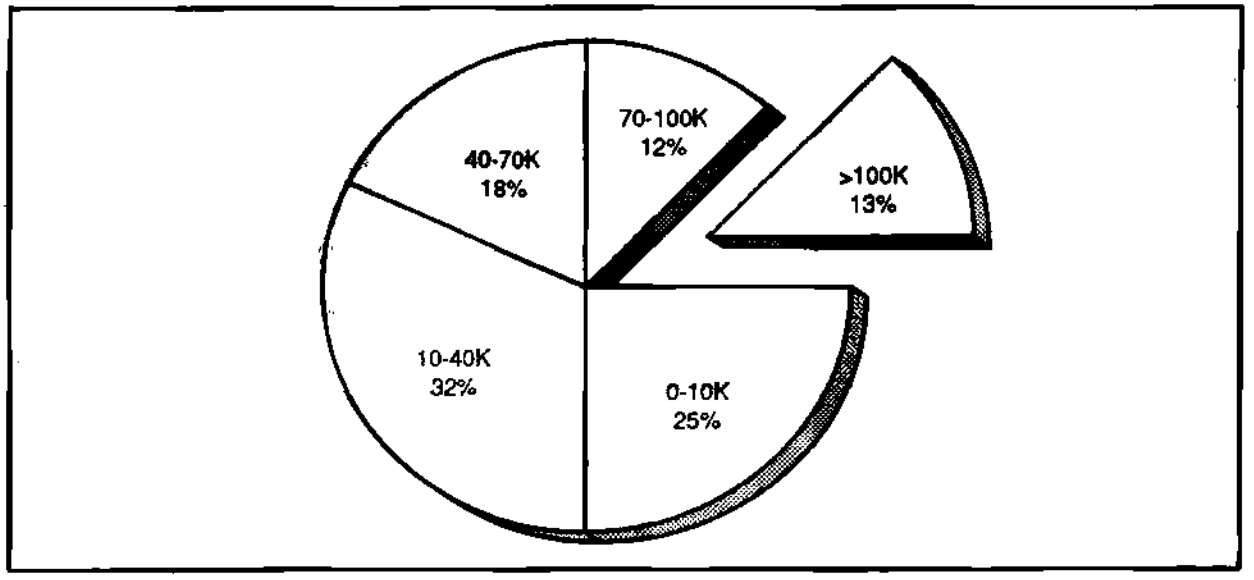
Although it is true that the 1991 leading-edge CMOS gate array products are far ahead of the 1990 applications, Dataquest believes that these products will be absorbed by the market over the next three years. High-performance computers and military applications will be the early adopters of these high-density arrays. Figure 4 illustrates Dataquest's vision of 1994 North American MOS gate array design starts by gate count.

Dataquest believes that larger SRAMs (128K and 256K) will be diffused in gate array base wafers and used for cache memory. Other functions such as SCSI, arithmetic logic unit (ALU), multiplier, multiplier-accumulator, first-in/first-out (FIFO), direct memory access (DMA) controller, cache controller, and 82XX microperipherals will also be diffused in the gate array and will drive gate counts upward.

We also believe that an increasing trend toward design reusability will push gate counts significantly higher than they have been in the past. ASIC designers will describe logic functions in VHDL or Verilog HDL, and the HDL functions then will be archived. Designers will retrieve these functions and resynthesize them on subsequent designs. We believe that functions will include both LSI and VLSI functions.

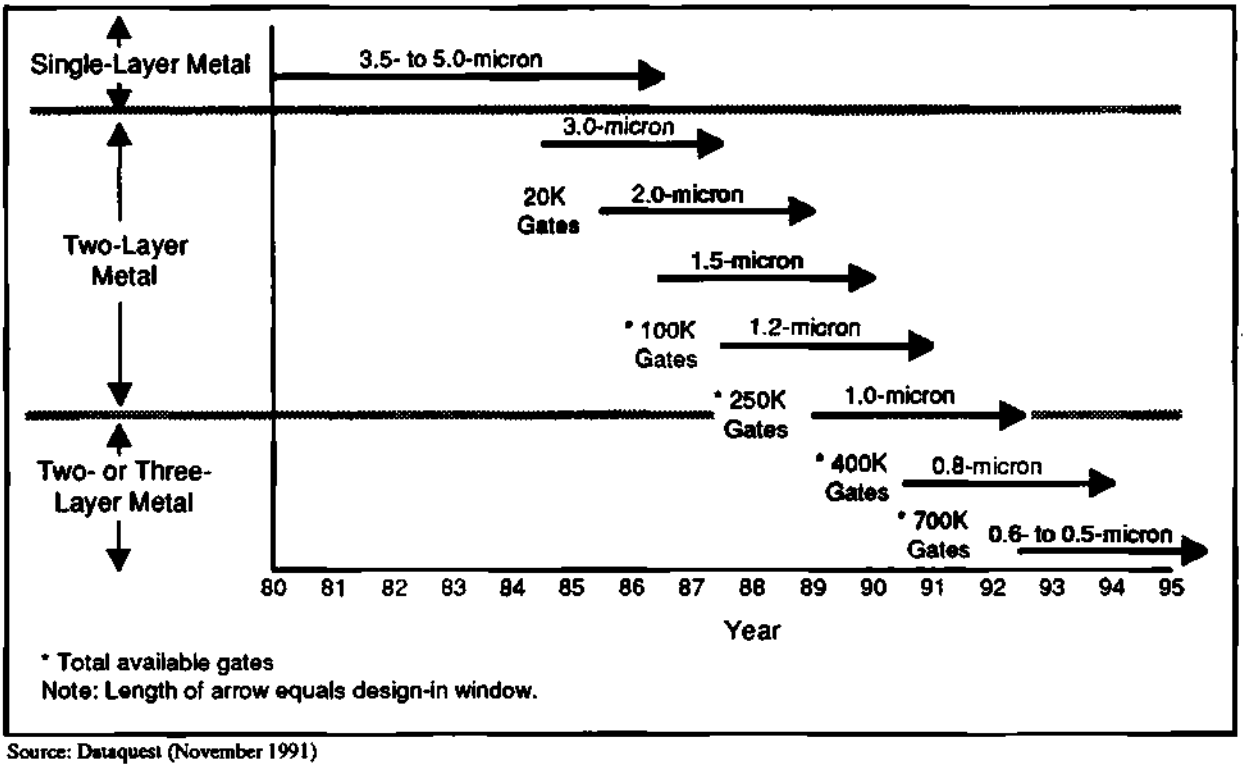
Figure 5 illustrates Dataquest's technology road map and design-in window for CMOS gate array design starts over time by drawn process geometry and maximum total available gates. On average, two-layer metal interconnect achieves approximately 40 to 50 percent gate

Figure 4
Estimated 1994 North American MOS Gate Array Design Starts by Utilized Gate Count



Source: Dataquest (November 1991)

Figure 5
CMOS Gate Array Design Start Technology Road Map



Source: Dataquest (November 1991)

utilization, while three-layer metal interconnect achieves approximately 65 to 75 percent gate utilization.

Each generation of products always seems far ahead of its time. It was only 1985 when a 2.0-micron 20,000 gate gate array seemed enormous. The question raised at the time was, "What will we do with 20,000 gates?" But the numbers now speak for themselves: the average North American MOS gate array design start gate count in 1990 was close to 16,000 gates, and the average for 1991 is expected to be 21,000 gates. The question being asked today is "What will we do with 400,000 gates?" If we can use history as a judge, designers will find applications that demand such high integration.

By Bryan Lewis

ASIC Packaging Trends

MOS Gate Arrays

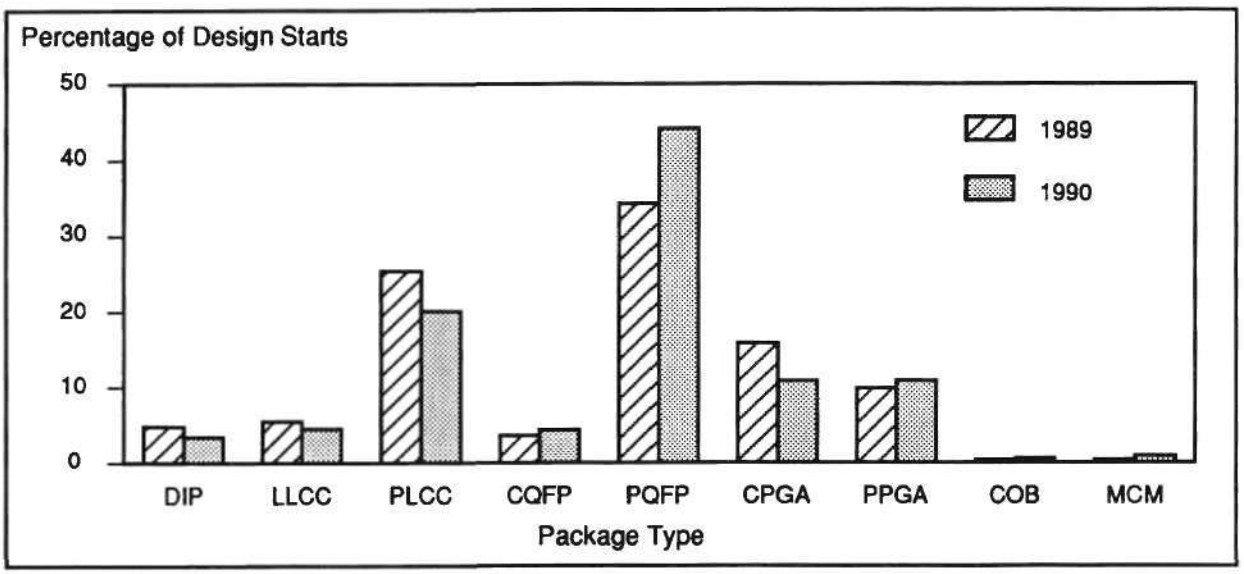
As gate counts rise, new demands are placed on package types and pin counts. Dataquest's analysis indicates that today's MOS gate array users are likely to start with a dual in-line package (DIP) for low-gate-count devices, subsequently move to a plastic-leaded chip carrier (PLCC) for medium-size arrays, then end up with a plastic quad flatpack (PQFP) or pin grid array (PGA) for higher gate counts.

Figure 1 illustrates estimated North American MOS gate array design starts by package type. Dataquest notes the following trends from this figure:

- The PQFP continues to gain market acceptance in North America. This PQFP package dominates the Japan MOS gate array market, accounting for approximately 70 percent of the 1990 market.
- The PLCC is losing market share to the PQFP, primarily because most PLCCs have a maximum of 84 pins, which are not enough for the increasing demands of today's market.
- The ceramic PGA is a costly package and is gradually being replaced by less expensive packages such as the plastic PGA.
- PPGA growth has been slow because of the lack of standards and hermetic problems experienced on early-generation packages.
- Chip-on-board (COB) packaging and multichip modules (MCMs) are immature and still too expensive for the bulk of the 1990 MOS gate array market.

High-pin-count packages will clearly be needed for a range of applications that demand high-complexity gate arrays. Indeed, some suppliers are now introducing PQFPs and PGAs with more than 500 pins. Although there are many introductions of packages with high pin counts, less than 1 percent of the 1990 North American design starts had greater than 244 pins. Figure 2 shows the North American

Figure 1
Estimated North American MOS Gate Array Design Starts by Package Type



Source: Dataquest (November 1991)

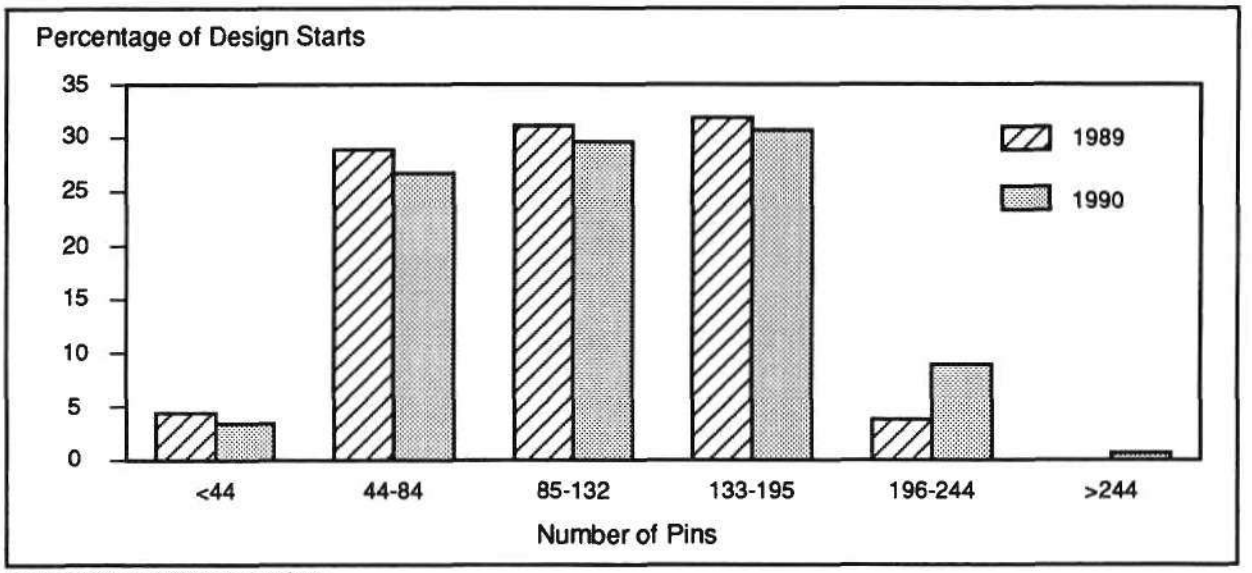
pin count distribution, where most of the growth in 1990 was in the 196- to 244-pin range (208-pin PQFP).

ASIC Packaging

Figure 3 contrasts estimated 1990 North American gate array and cell-based IC (CBIC) design starts by package type.

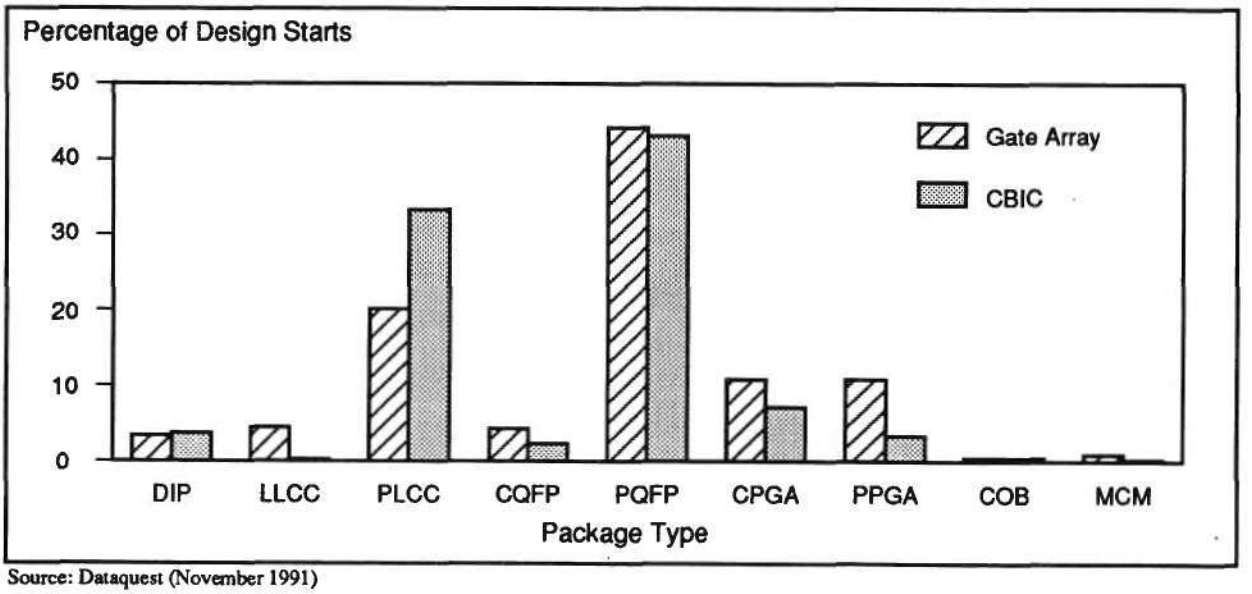
When comparing CBIC packages with those of gate arrays, we see a similar trend: As gate counts rise, designers start with DIPs, then move to PLCCs, and end up with PQFPs or PGAs for the higher gate counts. The notable exception between CBIC and gate array package types is that a higher percentage of CBIC designs are in the PLCC. We believe that the high percentage of communication applications in the CBIC market account for this difference. We believe that most telecom applications require fewer I/O pins than data processing

Figure 2
Estimated North American MOS Gate Array Design Starts by Pin Count



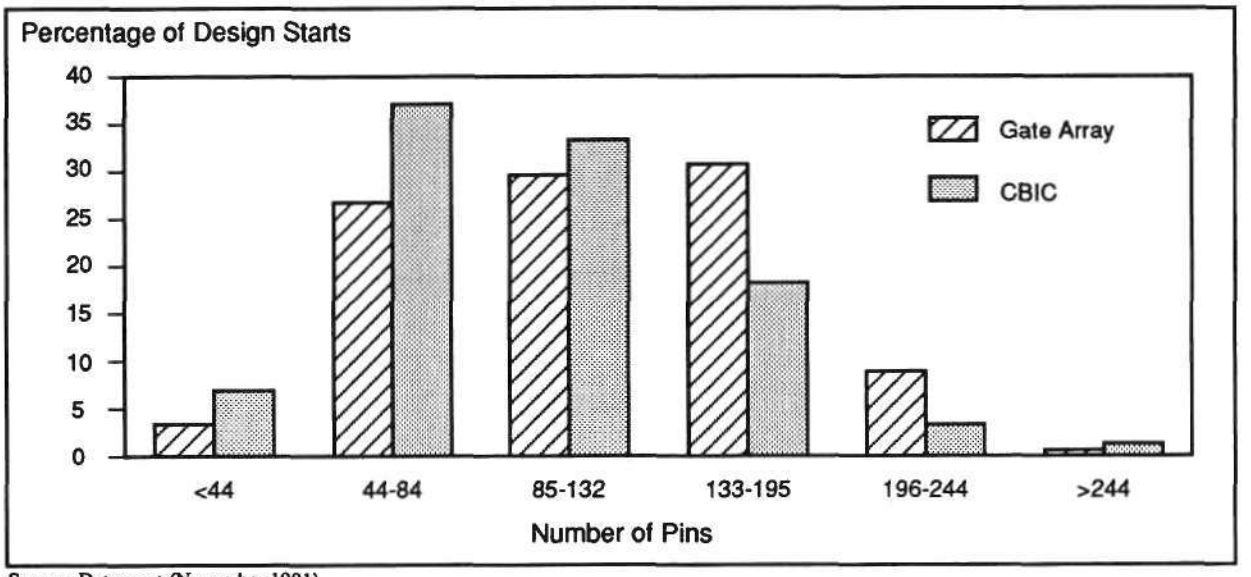
Source: Dataquest (November 1991)

Figure 3
Estimated 1990 North American MOS ASIC Design Starts by Package Type



Source: Dataquest (November 1991)

Figure 4
Estimated 1990 North American MOS ASIC Design Starts by Pin Count



Source: Dataquest (November 1991)

applications; thus, a higher portion of the CBIC market will fit within the 84-pin limitation of the PLCC.

Figure 4 contrasts estimated 1990 North American gate array and CBIC design starts by pin count.

Dataquest Perspective

Dataquest believes that a wide variety of package types and pin counts will coexist over the next five years because of the wide variety of ASIC applications. Important ASIC packaging trends that Dataquest envisions over the next five years include the following:

- Pin counts will continue to increase as gate counts rise.
- The DIP, LLCC, and PLCC will continue to lose market share because of their low pin counts.
- The PQFP is expected to remain the dominant package type throughout the decade and take market share from the DIP, LLCC, and PLCC.
- The CQFP is expected to lose market share to the metal quad flatpack (MQFP).
- The MQFP is expected to emerge and take market share from both the CQFP and CPGA in applications that are cost-sensitive and consume large amounts of power.
- The PPGA will capture increased market share as suppliers adopt industry standards and address the power dissipation issues.
- MCMs will gain significant market share as they move down the price learning curve.

By Bryan Lewis

Market Analysis

ASIC Applications Fuel Future Market Growth

Despite narrowing profit margins, demand for ASICs remains strong. Although ASIC design start growth is slowing because of increasing device complexity and encroaching products such as field-programmable gate arrays, the revenue opportunity continues to grow. ASICs are pervasive in today's application markets and will have high value in future applications.

Tables 1 through 4 show the historical and projected North American gate array and CBIC consumption by application market from 1988 through 1995. The forecasts include nonrecurring engineering revenue, device revenue, and intracompany revenue. The forecasts do not

Table 1
Estimated North American Gate Array Consumption by Application Market
(Percentage of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995
Data Processing	59.4	61.2	62.0	63.1	64.8	66.5	67.8	68.5
Communication	12.6	12.4	12.5	12.5	12.2	12.1	12.1	12.2
Industrial	8.5	7.2	7.0	6.8	6.6	6.4	6.3	6.0
Consumer	1.4	2.0	2.1	2.2	2.3	2.5	2.6	2.7
Military	17.0	16.2	15.3	14.4	13.2	11.6	10.3	9.5
Transportation	1.1	1.1	1.0	1.0	0.9	0.9	0.9	0.9
Total	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (November 1991)

Table 2
Estimated North American Gate Array Consumption by Application Market
(Millions of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995
Data Processing	685	784	841	917	1,086	1,340	1,645	1,930
Communication	145	159	170	181	204	243	295	344
Industrial	98	92	96	99	111	130	152	170
Consumer	17	25	28	32	39	51	62	76
Military	196	208	208	210	221	234	251	269
Transportation	12	14	14	14	15	18	23	27
Total	1,152	1,281	1,357	1,453	1,676	2,016	2,427	2,815

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (November 1991)

Table 3
Estimated North American Cell-Based IC Consumption by Application Market
(Percentage of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995
Data Processing	50.7	51.2	51.4	50.7	50.5	50.2	49.4	48.6
Communication	23.4	24.0	23.0	23.1	23.2	23.6	24.0	24.4
Industrial	11.4	10.0	11.0	10.8	10.5	10.2	10.1	10.0
Consumer	3.7	4.2	5.0	5.4	5.9	6.2	6.5	6.9
Military	8.0	7.8	6.5	6.0	5.5	5.0	4.9	4.8
Transportation	2.8	2.8	3.1	4.0	4.4	4.8	5.1	5.3
Total	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0

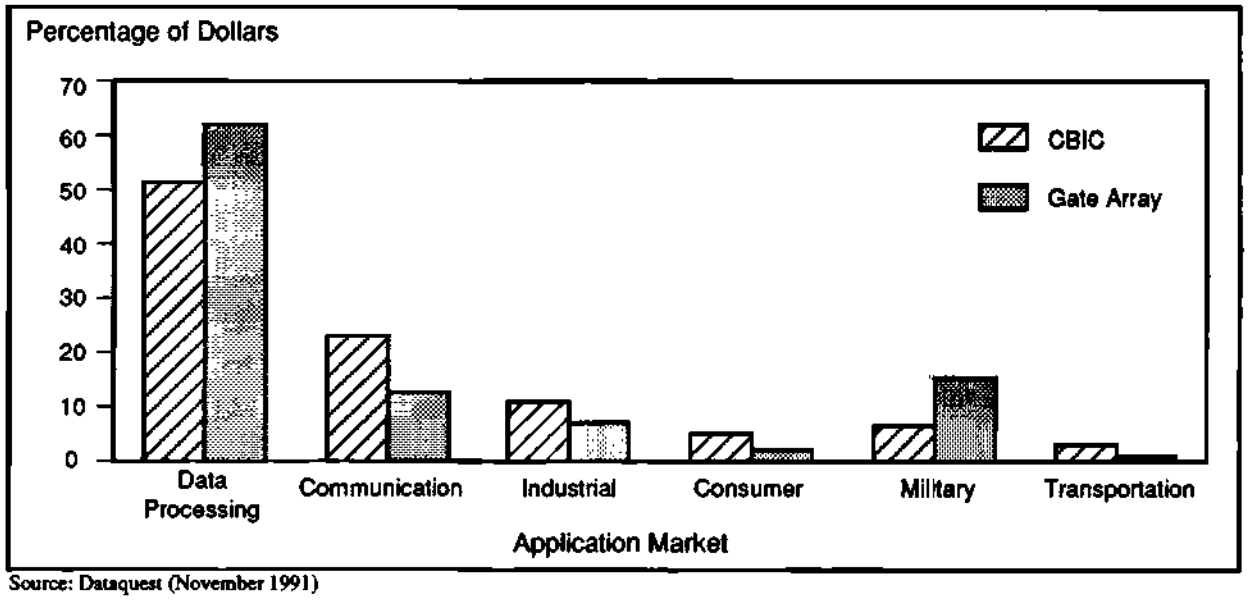
Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (November 1991)

Table 4
Estimated North American Cell-Based IC Consumption by Application Market (Millions of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995
Data Processing	408	436	583	665	801	967	1,075	1,158
Communication	188	204	261	303	368	455	522	582
Industrial	92	85	125	142	166	197	220	238
Consumer	30	36	57	71	94	119	141	164
Military	64	66	74	79	87	96	107	114
Transportation	23	24	35	52	70	92	111	126
Total	805	851	1,134	1,312	1,585	1,927	2,176	2,384

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (November 1991)

Figure 1
Estimated 1990 North American ASIC Consumption by Application Market



Source: Dataquest (November 1991)

include revenue captured from standard product groups or from captive manufacturing of system suppliers that do not sell ASICs to the merchant market such as IBM Corporation, Digital Equipment Corporation, and Unisys Corporation.

Figure 1 contrasts the 1990 North American gate array and CBIC application markets.

Application Market Segmentation

Data Processing

Data processing is defined as computer systems, data storage devices, input/output devices (such as media-to-media data conversion, scanning equipment, plotters, and voice recognition/synthesizer equipment), electronic printers, and office equipment (such as copiers, duplicators, and electronic calculators).

Key data processing products that consume large quantities of ASICs include the following:

- Workstations and personal computers
- Midrange computers, mainframes, and supercomputers
- Disk drives
- Electronic printers
- Copiers

Emerging data processing products with ASIC opportunity include the following:

- Notebook and palm-top computers

- 2.5-inch and 1.8-inch disk drives
- Video compression and decompression
- Digital video (color space conversion, image digitizing)

Subsystems within data processing products that are often implemented in ASICs include the following:

- Glue logic consolidation
- Central processing unit
- Graphic processor
- Memory manager
- I/O manager
- Disk drive controller
- Floating-point register
- Network controller
- Bus interface
- Cache controller

Communication

Communication is defined as personal communication, networking, image communication, and voice communication.

Applications for ASICs in the communication segment include the following:

- PBX
- Central office switching systems
- T-1 multiplexing
- Modems
- LANs
- ISDN
- Line cards
- Fiber-optic transmission
- Encryption

Industrial

Industrial is defined as test equipment, manufacturing systems, process control equipment, instrumentation, medical equipment, and robotics.

Applications for ASICs in the industrial segment include the following:

- Automated test equipment
- Medical CAT scanners
- Logic analyzers
- Motor control
- Robotics

Military

Military is defined as military electronic equipment.

Applications for ASICs in the military segment include the following:

- Radar
- Sonar
- Missile guidance and control
- Navigation
- Reconnaissance
- Flight simulators

Transportation

Transportation is defined as in-car entertainment systems, body control electronics, driver information, power-train electronics, safety electronics, and convenience electronics.

Applications for ASICs in the transportation segment include the following:

- Automatic braking systems
- Active suspension
- Collision-avoidance systems
- Multiplex systems such as driver door and steering wheel
- Electronic instrument clusters
- Power-train controls
- Engine management

Dataquest Perspective

As can be seen from the list of ASIC applications, there is a broad market for ASIC technology. Strong market pull for ASIC technology translates to a healthy revenue opportunity, but, of course, this does not necessarily equate to sustainable profitability.

By Bryan Lewis

In Future Issues

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- BiCMOS ASICs
- CBIC Product Analysis

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Dataquest Perspective

ASICs *Worldwide*

Vol. 1, No. 1 November 25, 1991

Product Analysis

DQ Feature—*Are System Designers Ready for the New Breed of CMOS Gate Arrays?*

ASIC suppliers throughout the industry are announcing CMOS gate array products with dramatically higher gate counts than the previous generation of products. Dataquest analyzes the 1990 CMOS gate array design start trends and projects the impact of the new gate array product offering.

By Bryan Lewis *Page 2*

ASIC Packaging Trends

As gate counts rise, new demands are placed on ASIC packages. Dataquest examines the packaging and pin-count trends for both MOS gate array and cell-based ICs.

By Bryan Lewis *Page 6*

Market Analysis

ASIC Applications Fuel Future Market Growth

Despite the fact that ASIC design start growth is slowing and profit margins are narrowing, ASIC revenue growth remains healthy. Increasing demand for ASICs is being driven by a range of high-growth application markets. Dataquest highlights the applications that ASIC vendors should be exploring and provides its gate array and CBIC application market forecasts.

By Bryan Lewis *Page 8*

Product Analysis

Are System Designers Ready for the New Breed of CMOS Gate Arrays?

The gun has sounded and the race has begun for the highest-density gate array. ASIC suppliers throughout the industry are announcing CMOS gate arrays with dramatically higher gate counts than the previous generation of products. Although these products will find their way into the market over the next five years, Dataquest believes that the bulk of the high-density design starts will not begin until the 1993 to 1994 time frame.

Table 1 ranks the top 15 worldwide CMOS gate array suppliers by their 1990 shipment revenue and lists their leading gate array products. Most of the suppliers to date have announced 0.8-micron three-layer metal products that can achieve utilized gate counts in excess of 100,000 gates and also incorporate diffused SRAM blocks.

Although it is important for leading suppliers to have a flagship product that can be used to demonstrate their technical capabilities, most of the 1990 design starts were in much less sophisticated products. Dataquest estimates that the average utilized design start gate count in North America was 15,500 gates during 1990, with only 3 percent of the designs greater than 100,000 gates. Furthermore, only 9 percent of the 1990 designs were triple metal and only 1 percent of the designs had diffused SRAM blocks.

1990 Design Starts by Gate Count

Figure 1 illustrates the distribution of 1989 and 1990 North American MOS gate array design starts by gate count. Dataquest analysis of this figure reveals the following important points:

- The most cost-effective gate count shifted from 6,000 to 10,000 gates in 1989 to 10,000 to 20,000 in 1990.
- PC/workstation designers are very cost sensitive; therefore, a large portion of their 1990 designs were in the 10,000- to 20,000-gate range.
- Midrange computer designers wanted more integration and higher performance than the PC/workstation designers; thus, a large portion of their 1990 designs were in the 40,000- to 70,000-gate range.

Table 1
Estimated Worldwide CMOS Gate Array Shipments and Leading Products

1990 Rank	Company	1990 ($M)	Leading Process (Drawn)	Maximum Gates (Gross)	Metal Layers	Maximum Gates (Usable)	Embedded Cells
1	LSI Logic	461.0	0.7	307K	3	200K	Yes
2	Fujitsu	369.0	0.8	200K	3	120K	Yes
3	NEC	340.0	0.8	250K	3	150K	Yes
4	Toshiba	332.0	0.8	302K	3	210K	Yes
5	Hitachi	150.0	0.8	250K	3	100K	?
6	Oki	86.0	0.8	231K	2	100K	Yes
7	Seiko	80.0	0.8	255K	2	102K	?
8	GEC Plessey	69.0	1.0	220K	3	150K	?
9	National Semiconductor	66.0	1.0	250K	3	125K	?
10	Matsushita	66.0	1.2	35K	2	30K	?
11	VLSI Technology	54.0	1.0	172K	3	125K	Yes
12	Motorola	41.0	1.0	318K	3	195K	Yes
13	Sharp	38.0	1.0	30K	2	15K	?
14	Mitsubishi	38.0	0.8	400K	3	250K	?
15	SGS-Thomson	35.0	0.7	288K	3	216K	?

Source: Dataquest (November 1991)

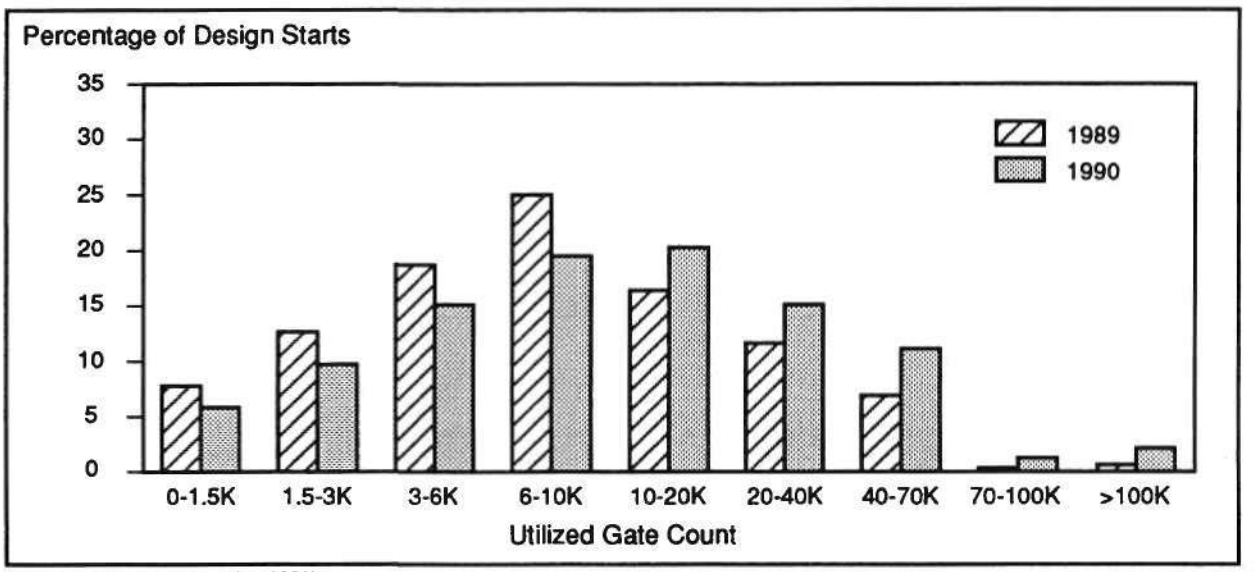
- Supercomputer and military applications require the ultimate in performance and integration; hence, these applications accounted for the majority of 1990 designs greater than 70,000 gates.

1990 Design Starts by Function

Figure 2 illustrates North American MOS gate array design starts by function. Figure 3 illustrates the percentage of North American MOS gate array designs starts that incorporated memory, by the number of bits. Dataquest's analysis from these figures is as follows:

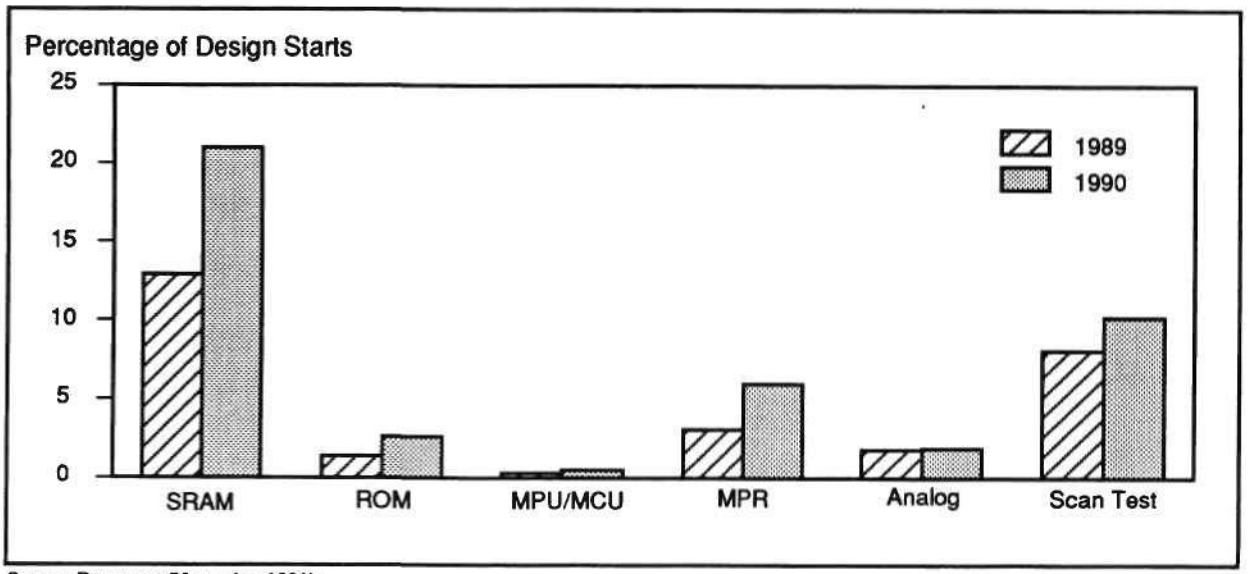
- Approximately 60 percent of the 1990 MOS gate array market comprises data processing applications, such as cache memory, which are driving the strong trend toward on-chip SRAM.

Figure 1
Estimated North American MOS Gate Array Design Starts by Gate Count



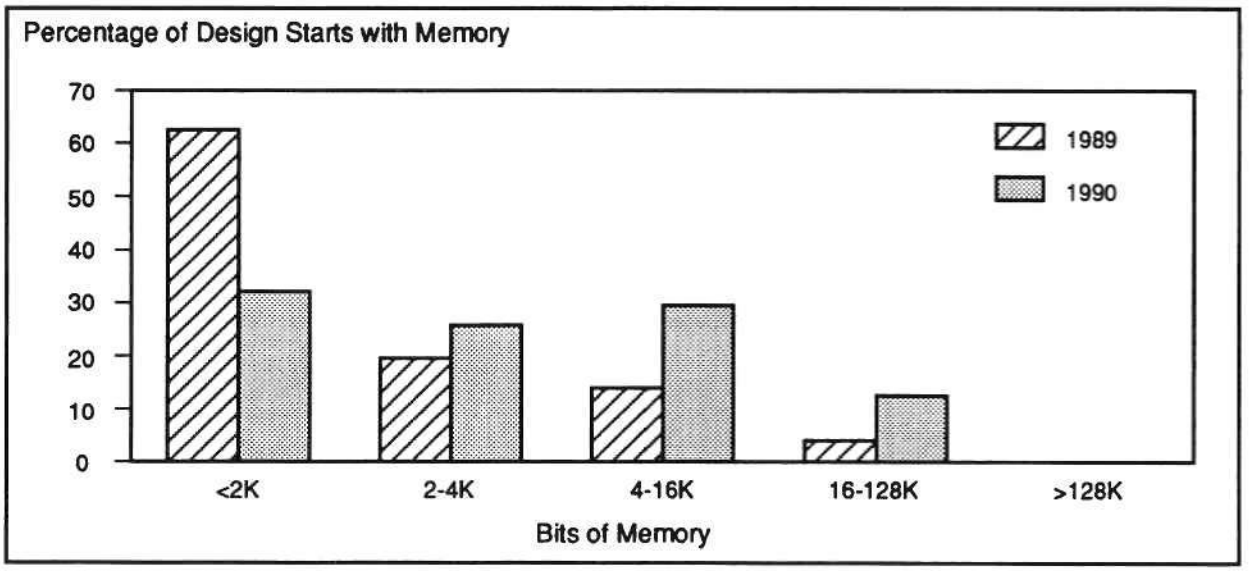
Source: Dataquest (November 1991)

Figure 2
Estimated North American MOS Gate Array Design Starts by Function



Source: Dataquest (November 1991)

Figure 3
Estimated North American MOS Gate Array Design Starts by Memory Bits



Source: Dataquest (November 1991)

- Only 5 percent of the 1990 memories were diffused in the base wafer (95 percent were metal-configured memories).
- ROM is not as cost-effective in a sea-of-gates architecture as in a CBIC product. Therefore, only 3 percent of the 1990 gate array design starts had on-chip ROM versus 15 percent of the 1990 CBIC designs.
- Most of the microprocessing units/microcontroller units (MPUs/MCUs) that have been incorporated in gate array designs to date have been CISC (that is, 80C51, 2901, and Z80). The advantages of on-chip CISC products (performance and footprint) in general are not great enough to offset the lower cost of just using a standard CISC product on a PC board in conjunction with gate arrays. The jury is still out as to whether RISC cores will have the same argument.
- Most of the microperipheral (MPR) functions incorporated in ASICs to date were 82XX peripherals.
- Analog functions are difficult to implement in logic gates. Therefore, most of the analog functions tracked to date have been implemented in pure analog arrays from companies such as GEC Plessey and Exar.
- As gate densities continue to rise at a rapid rate, on-chip test has become critical. JTAG compatibility also is emerging as the industry standard for board-level testing.

Dataquest Perspective

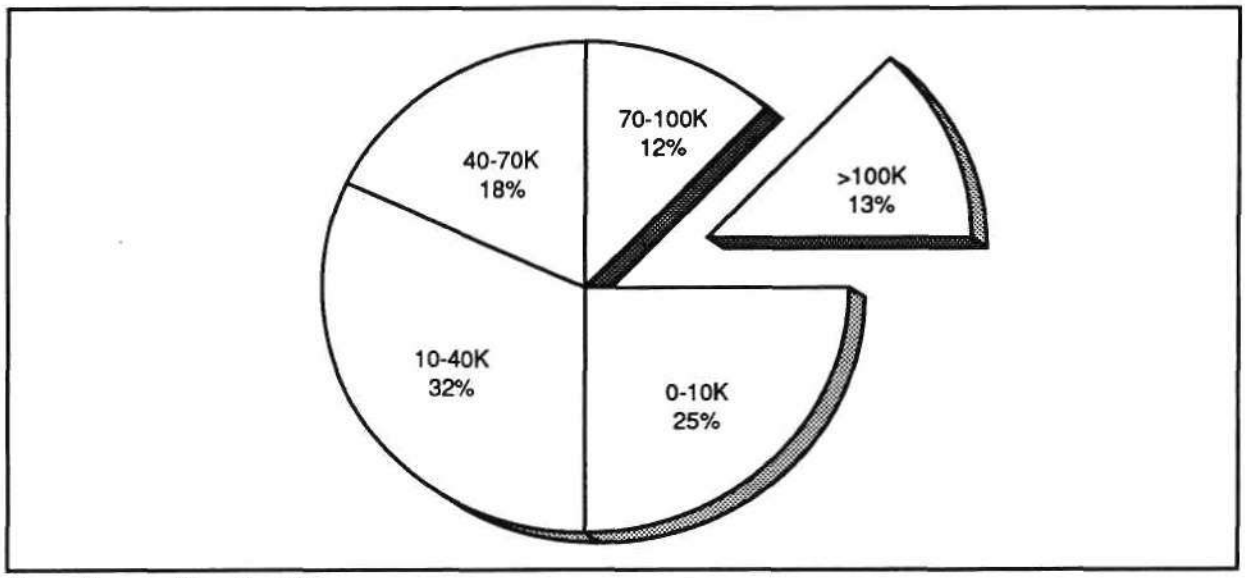
Although it is true that the 1991 leading-edge CMOS gate array products are far ahead of the 1990 applications, Dataquest believes that these products will be absorbed by the market over the next three years. High-performance computers and military applications will be the early adopters of these high-density arrays. Figure 4 illustrates Dataquest's vision of 1994 North American MOS gate array design starts by gate count.

Dataquest believes that larger SRAMs (128K and 256K) will be diffused in gate array base wafers and used for cache memory. Other functions such as SCSI, arithmetic logic unit (ALU), multiplier, multiplier-accumulator, first-in/first-out (FIFO), direct memory access (DMA) controller, cache controller, and 82XX microperipherals will also be diffused in the gate array and will drive gate counts upward.

We also believe that an increasing trend toward design reusability will push gate counts significantly higher than they have been in the past. ASIC designers will describe logic functions in VHDL or Verilog HDL, and the HDL functions then will be archived. Designers will retrieve these functions and resynthesize them on subsequent designs. We believe that functions will include both LSI and VLSI functions.

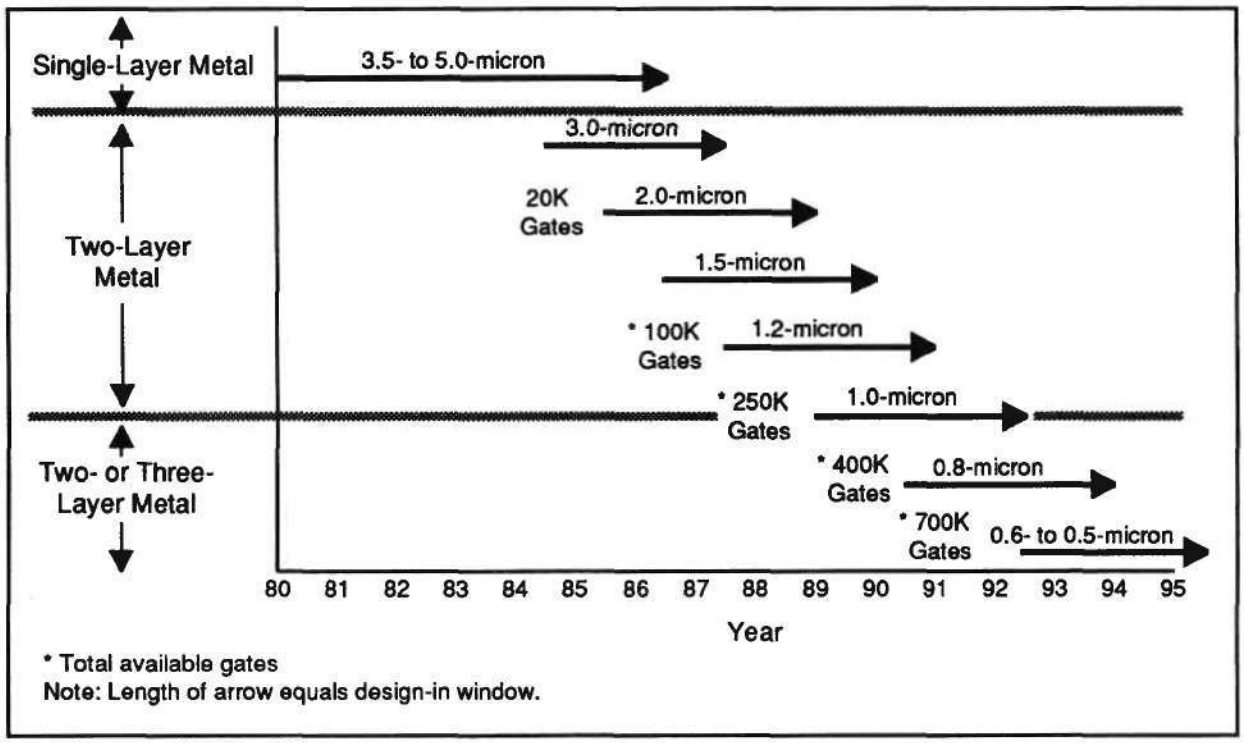
Figure 5 illustrates Dataquest's technology road map and design-in window for CMOS gate array design starts over time by drawn process geometry and maximum total available gates. On average, two-layer metal interconnect achieves approximately 40 to 50 percent gate

Figure 4
Estimated 1994 North American MOS Gate Array Design Starts by Utilized Gate Count



Source: Dataquest (November 1991)

Figure 5
CMOS Gate Array Design Start Technology Road Map



Source: Dataquest (November 1991)

utilization, while three-layer metal interconnect achieves approximately 65 to 75 percent gate utilization.

Each generation of products always seems far ahead of its time. It was only 1985 when a 2.0-micron 20,000 gate gate array seemed enormous. The question raised at the time was, "What will we do with 20,000 gates?" But the numbers now speak for themselves: the average North American MOS gate array design start gate count in 1990 was close to 16,000 gates, and the average for 1991 is expected to be 21,000 gates. The question being asked today is "What will we do with 400,000 gates?" If we can use history as a judge, designers will find applications that demand such high integration.

By Bryan Lewis

ASIC Packaging Trends

MOS Gate Arrays

As gate counts rise, new demands are placed on package types and pin counts. Dataquest's analysis indicates that today's MOS gate array users are likely to start with a dual in-line package (DIP) for low-gate-count devices, subsequently move to a plastic-leaded chip carrier (PLCC) for medium-size arrays, then end up with a plastic quad flatpack (PQFP) or pin grid array (PGA) for higher gate counts.

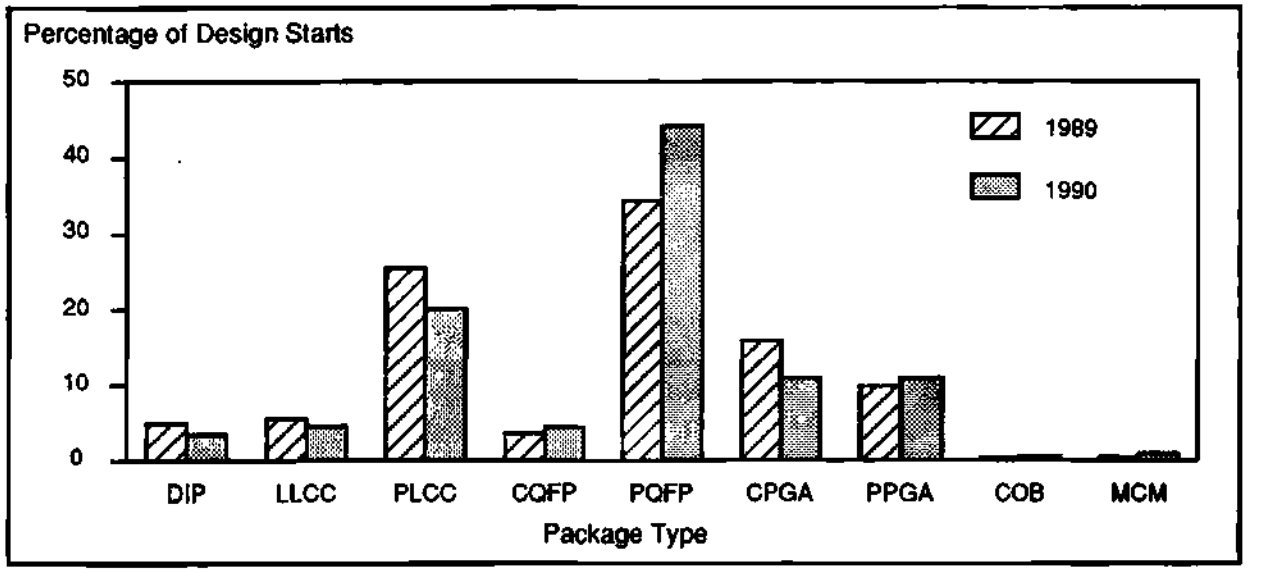
Figure 1 illustrates estimated North American MOS gate array design starts by package type.

Dataquest notes the following trends from this figure:

- The PQFP continues to gain market acceptance in North America. This PQFP package dominates the Japan MOS gate array market, accounting for approximately 70 percent of the 1990 market.
- The PLCC is losing market share to the PQFP, primarily because most PLCCs have a maximum of 84 pins, which are not enough for the increasing demands of today's market.
- The ceramic PGA is a costly package and is gradually being replaced by less expensive packages such as the plastic PGA.
- PPGA growth has been slow because of the lack of standards and hermetic problems experienced on early-generation packages.
- Chip-on-board (COB) packaging and multichip modules (MCMs) are immature and still too expensive for the bulk of the 1990 MOS gate array market.

High-pin-count packages will clearly be needed for a range of applications that demand high-complexity gate arrays. Indeed, some suppliers are now introducing PQFPs and PGAs with more than 500 pins. Although there are many introductions of packages with high pin counts, less than 1 percent of the 1990 North American design starts had greater than 244 pins. Figure 2 shows the North American

Figure 1
Estimated North American MOS Gate Array Design Starts by Package Type



Source: Dataquest (November 1991)

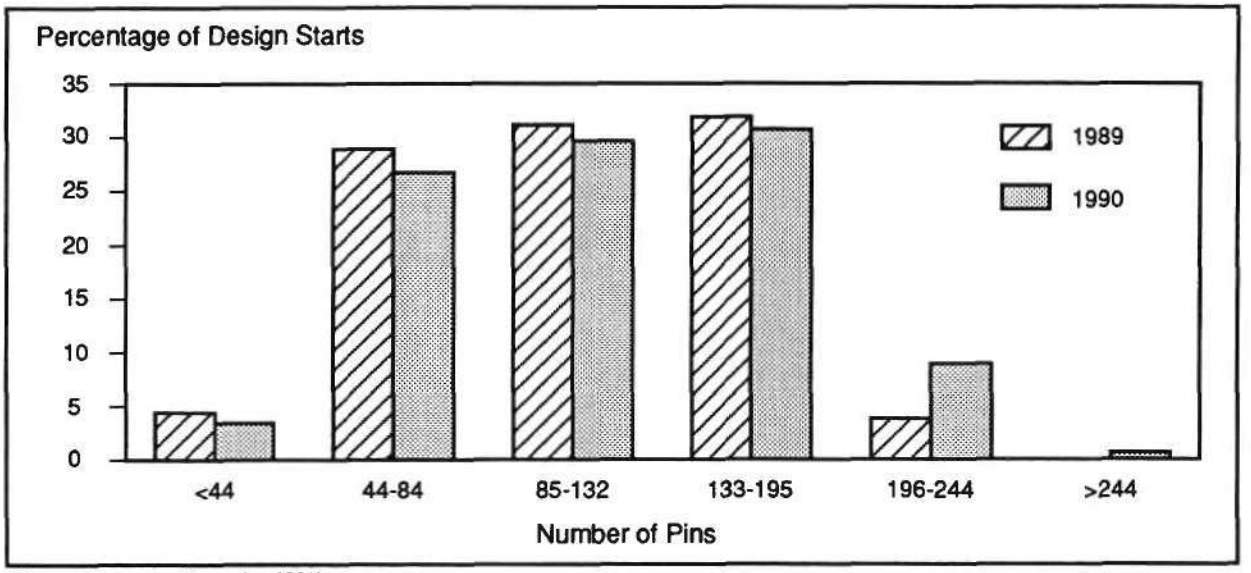
pin count distribution, where most of the growth in 1990 was in the 196- to 244-pin range (208-pin PQFP).

ASIC Packaging

Figure 3 contrasts estimated 1990 North American gate array and cell-based IC (CBIC) design starts by package type.

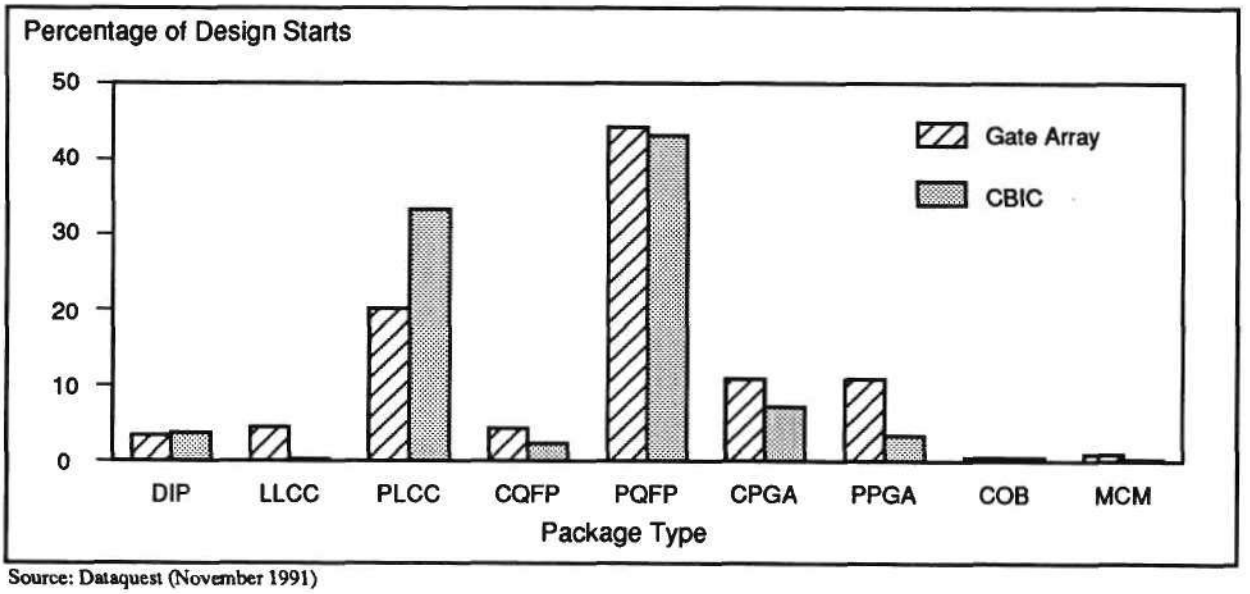
When comparing CBIC packages with those of gate arrays, we see a similar trend: As gate counts rise, designers start with DIPs, then move to PLCCs, and end up with PQFPs or PGAs for the higher gate counts. The notable exception between CBIC and gate array package types is that a higher percentage of CBIC designs are in the PLCC. We believe that the high percentage of communication applications in the CBIC market account for this difference. We believe that most telecom applications require fewer I/O pins than data processing

Figure 2
Estimated North American MOS Gate Array Design Starts by Pin Count



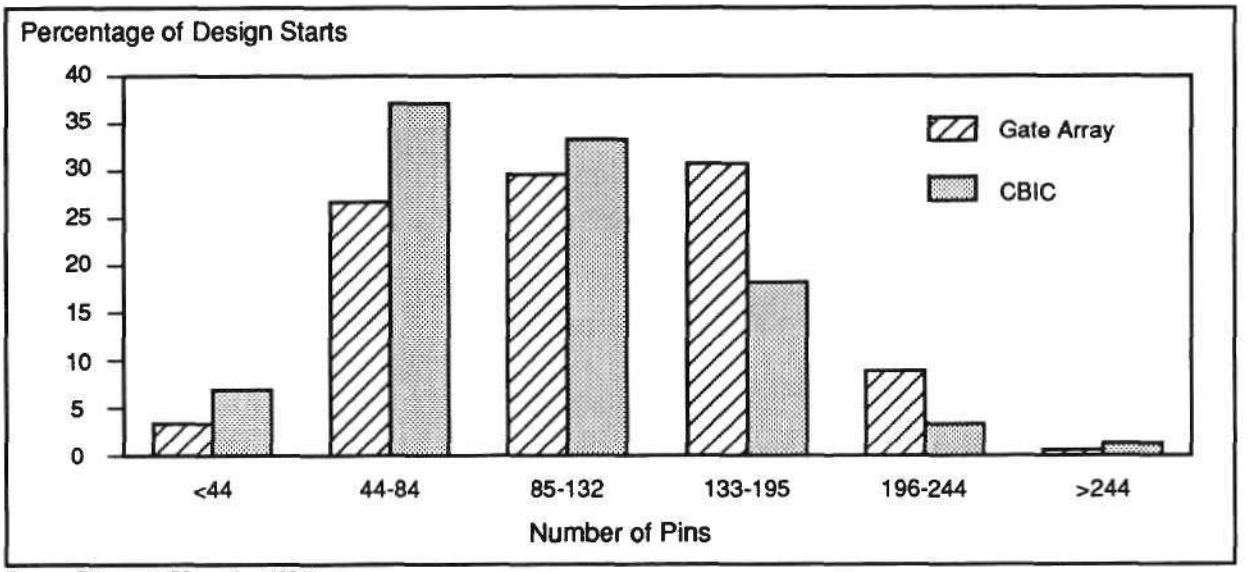
Source: Dataquest (November 1991)

Figure 3
Estimated 1990 North American MOS ASIC Design Starts by Package Type



Source: Dataquest (November 1991)

Figure 4
Estimated 1990 North American MOS ASIC Design Starts by Pin Count



Source: Dataquest (November 1991)

applications; thus, a higher portion of the CBIC market will fit within the 84-pin limitation of the PLCC.

Figure 4 contrasts estimated 1990 North American gate array and CBIC design starts by pin count.

Dataquest Perspective

Dataquest believes that a wide variety of package types and pin counts will coexist over the next five years because of the wide variety of ASIC applications. Important ASIC packaging trends that Dataquest envisions over the next five years include the following:

- Pin counts will continue to increase as gate counts rise.
- The DIP, LLCC, and PLCC will continue to lose market share because of their low pin counts.
- The PQFP is expected to remain the dominant package type throughout the decade and take market share from the DIP, LLCC, and PLCC.
- The CQFP is expected to lose market share to the metal quad flatpack (MQFP).
- The MQFP is expected to emerge and take market share from both the CQFP and CPGA in applications that are cost-sensitive and consume large amounts of power.
- The PPGA will capture increased market share as suppliers adopt industry standards and address the power dissipation issues.
- MCMs will gain significant market share as they move down the price learning curve.

By Bryan Lewis

Market Analysis

ASIC Applications Fuel Future Market Growth

Despite narrowing profit margins, demand for ASICs remains strong. Although ASIC design start growth is slowing because of increasing device complexity and encroaching products such as field-programmable gate arrays, the revenue opportunity continues to grow. ASICs are pervasive in today's application markets and will have high value in future applications.

Tables 1 through 4 show the historical and projected North American gate array and CBIC consumption by application market from 1988 through 1995. The forecasts include nonrecurring engineering revenue, device revenue, and intracompany revenue. The forecasts do not

Table 1
Estimated North American Gate Array Consumption by Application Market
(Percentage of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995
Data Processing	59.4	61.2	62.0	63.1	64.8	66.5	67.8	68.5
Communication	12.6	12.4	12.5	12.5	12.2	12.1	12.1	12.2
Industrial	8.5	7.2	7.0	6.8	6.6	6.4	6.3	6.0
Consumer	1.4	2.0	2.1	2.2	2.3	2.5	2.6	2.7
Military	17.0	16.2	15.3	14.4	13.2	11.6	10.3	9.5
Transportation	1.1	1.1	1.0	1.0	0.9	0.9	0.9	0.9
Total	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (November 1991)

Table 2
Estimated North American Gate Array Consumption by Application Market
(Millions of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995
Data Processing	685	784	841	917	1,086	1,340	1,645	1,930
Communication	145	159	170	181	204	243	295	344
Industrial	98	92	96	99	111	130	152	170
Consumer	17	25	28	32	39	51	62	76
Military	196	208	208	210	221	234	251	269
Transportation	12	14	14	14	15	18	23	27
Total	1,152	1,281	1,357	1,453	1,676	2,016	2,427	2,815

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (November 1991)

Table 3
Estimated North American Cell-Based IC Consumption by Application Market
(Percentage of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995
Data Processing	50.7	51.2	51.4	50.7	50.5	50.2	49.4	48.6
Communication	23.4	24.0	23.0	23.1	23.2	23.6	24.0	24.4
Industrial	11.4	10.0	11.0	10.8	10.5	10.2	10.1	10.0
Consumer	3.7	4.2	5.0	5.4	5.9	6.2	6.5	6.9
Military	8.0	7.8	6.5	6.0	5.5	5.0	4.9	4.8
Transportation	2.8	2.8	3.1	4.0	4.4	4.8	5.1	5.3
Total	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0

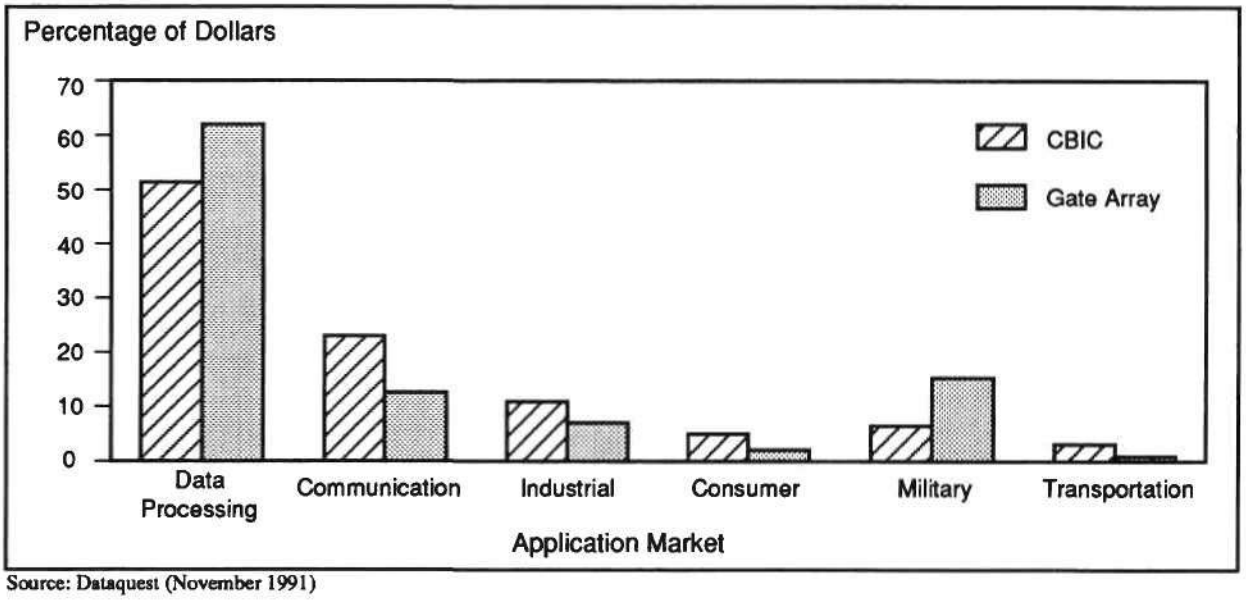
Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (November 1991)

Table 4
Estimated North American Cell-Based IC Consumption by Application Market (Millions of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995
Data Processing	408	436	583	665	801	967	1,075	1,158
Communication	188	204	261	303	368	455	522	582
Industrial	92	85	125	142	166	197	220	238
Consumer	30	36	57	71	94	119	141	164
Military	64	66	74	79	87	96	107	114
Transportation	23	24	35	52	70	92	111	126
Total	805	851	1,134	1,312	1,585	1,927	2,176	2,384

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (November 1991)

Figure 1
Estimated 1990 North American ASIC Consumption by Application Market



Source: Dataquest (November 1991)

include revenue captured from standard product groups or from captive manufacturing of system suppliers that do not sell ASICs to the merchant market such as IBM Corporation, Digital Equipment Corporation, and Unisys Corporation.

Figure 1 contrasts the 1990 North American gate array and CBIC application markets.

Application Market Segmentation

Data Processing

Data processing is defined as computer systems, data storage devices, input/output devices (such as media-to-media data conversion, scanning equipment, plotters, and voice recognition/synthesizer equipment), electronic printers, and office equipment (such as copiers, duplicators, and electronic calculators).

Key data processing products that consume large quantities of ASICs include the following:

- Workstations and personal computers
- Midrange computers, mainframes, and supercomputers
- Disk drives
- Electronic printers
- Copiers

Emerging data processing products with ASIC opportunity include the following:

- Notebook and palm-top computers

- 2.5-inch and 1.8-inch disk drives
- Video compression and decompression
- Digital video (color space conversion, image digitizing)

Subsystems within data processing products that are often implemented in ASICs include the following:

- Glue logic consolidation
- Central processing unit
- Graphic processor
- Memory manager
- I/O manager
- Disk drive controller
- Floating-point register
- Network controller
- Bus interface
- Cache controller

Communication

Communication is defined as personal communication, networking, image communication, and voice communication.

Applications for ASICs in the communication segment include the following:

- PBX
- Central office switching systems
- T-1 multiplexing
- Modems
- LANs
- ISDN
- Line cards
- Fiber-optic transmission
- Encryption

Industrial

Industrial is defined as test equipment, manufacturing systems, process control equipment, instrumentation, medical equipment, and robotics.

Applications for ASICs in the industrial segment include the following:

- Automated test equipment
- Medical CAT scanners
- Logic analyzers
- Motor control
- Robotics

Military

Military is defined as military electronic equipment.

Applications for ASICs in the military segment include the following:

- Radar
- Sonar
- Missile guidance and control
- Navigation
- Reconnaissance
- Flight simulators

Transportation

Transportation is defined as in-car entertainment systems, body control electronics, driver information, power-train electronics, safety electronics, and convenience electronics.

Applications for ASICs in the transportation segment include the following:

- Automatic braking systems
- Active suspension
- Collision-avoidance systems
- Multiplex systems such as driver door and steering wheel
- Electronic instrument clusters
- Power-train controls
- Engine management

Dataquest Perspective

As can be seen from the list of ASIC applications, there is a broad market for ASIC technology. Strong market pull for ASIC technology translates to a healthy revenue opportunity, but, of course, this does not necessarily equate to sustainable profitability.

By Bryan Lewis

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Dataquest Perspective

ASICs *Worldwide*

Vol. 1, No. 2 December 23, 1991

Market Analysis

PLD Prospects in the Face of a Weak Economy

Although the CMOS programmable logic devices (PLDs) market continues to outpace the growth rate of the overall semiconductor market, efficient manufacturing and strong distribution have not been enough to insulate it from widespread slowing in the electronics industry. There is little growth expected for the fourth quarter of 1991. Is this a short-term aberration or does it spell trouble for the PLD industry? Dataquest analyzes the dynamics of the CMOS PLD market and predicts its future.

By Robert Beachler and Ron Collett

Page 2

Product Analysis

The ASIC Battle Rages On

Cell-based ICs have long been involved in a design war with gate arrays, which entered the electronic system design market a few years prior to CBICs and quickly established domination. CBIC product designers still search for new weapons in the form of unique cell libraries to attack the well-entrenched gate array product. But these gate array product designers can counter with a weapon of their own: the embedded gate array. In this article, Dataquest examines the probable winner in this battle.

By Bryan Lewis

Page 5

Market Analysis

PLD Prospects in the Face of a Weak Economy

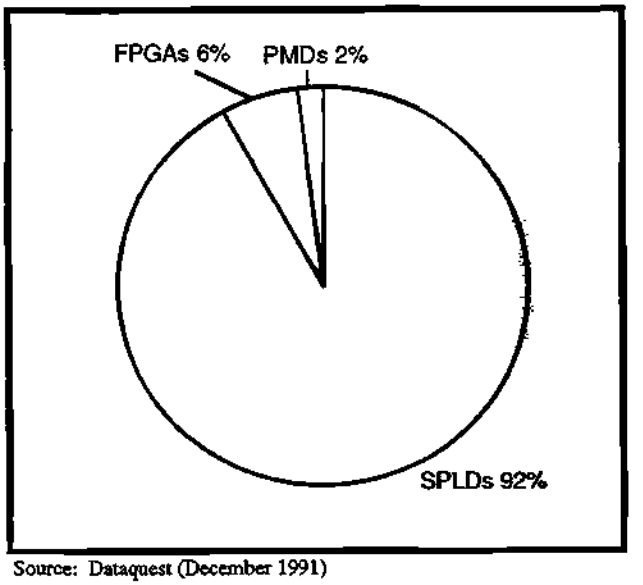
CMOS programmable logic devices (PLDs), which include simple PLDs (SPLDs), programmable multilevel devices (PMDs), and field programmable gate arrays (FPGAs), are the fastest-growing segment of the semiconductor market. Their projected five-year compound annual growth rate (CAGR) is 36 percent. Yet high demand, efficient manufacturing, and strong distribution have not been enough to insulate the segment from the widespread downturn in the electronics industry. Indeed, recent announcements by PLD manufacturers suggest that the fourth quarter of 1991 will show little if any growth compared with the previous quarter. Despite the slowdown, Dataquest believes that this condition is a short-term aberration. We expect market conditions to improve in 1992 as more users adopt the technology, a larger segment of the market uses the technology in production, and several new FPGA suppliers enter the market.

Weathering the Downturn Demands Diversified PLD Product Portfolios

Segmenting the PLD market into its submarkets reveals that the SPLD market is less immune to downturns in the electronics industry than are its FPGA and PMD cousins. Because of their similarities, PMDs and FPGAs are grouped by Dataquest into a complex PLD (CPLD) market. Unlike FPGAs and PMDs, the SPLD is a mature product that has reached commodity status. So profitability and high revenue depend heavily on high-volume shipments. About 80 percent of SPLDs shipped are used in data processing and communications markets. It is not surprising that the recent electronics market slowdown has impacted both segments, especially data processing, which of course includes personal computers. The lion's share of the total PLDs shipped are in fact SPLDs, which include PALs, FPLAs, and GALs (see Figure 1).

It is also not surprising that several CMOS PLD manufacturers announced that the fourth quarter of 1991 will witness flat growth, compared with the previous quarter. For manufacturers such as Lattice Semiconductor and Integrated CMOS

Figure 1
Estimated 1990 Worldwide CMOS PLD Units, by Product



Source: Dataquest (December 1991)

Technology, whose primary PLD offerings fall into the SPLD camp, the current market conditions are especially challenging. The primary avenue for growth among these vendors is reapportionment of market share. In short, they must "steal sockets" and wrestle existing market share from competitors. Expansion of the SPLD market is limited by the following factors:

- The high level of market penetration achieved by these products
- The limited number of new applications that SPLDs can target
- The large number of suppliers serving this market
- The limited differentiation among SPLD products
- The availability of substitute products, namely PMDs and FPGAs

Unlike the SPLD market, the CPLD market is not saturated. Devices in these categories continue to find new applications and in fact are readily capturing sockets once the exclusive territory of standard logic, SPLDs, and, in some cases, gate arrays. Because PMDs and FPGAs are finding use across a broad range of applications, they are less susceptible to industry-specific downturns. Thus, for most CPLD suppliers, weathering the current economic downturn is not nearly as daunting as the challenges facing SPLD-only vendors.

The fact that the business models of most CPLD vendors do not depend heavily on high-volume applications also works in their favor. This situation, of course, contrasts sharply with the models employed by SPLD vendors. The current economic downturn will continue to impact those suppliers relying on high-volume, low-cost products such as the current generation of 20- and 24-pin devices. As Table 1 shows, the majority of high-end PLDs and FPGAs are shipped in packages that boast 28 to 84 pins. Segmenting a supplier's product revenue portfolio by pin count is a quick way to get an indication of that company's business model, as well as its ability to weather economic downturns. The fragility of such a business model that relies extensively on low-pin-count devices is clearly manifesting itself in today's market.

Vulnerability of PMDs and FPGAs

Despite the advantages that CPLDs hold over SPLDs, they are not fully immune to the economic flu gripping the electronics industry. The combination of a slowdown in military spending and a softening of the telecommunications and computer markets has caused some suppliers to re-evaluate heretofore bold expansion plans.

Several CPLD vendors have also not done much to help themselves lately by preannouncing products. FPGA makers are working hard not to fall into the trap of preannouncing products. As can be seen, however, preannouncements have a domino effect; one company's preannouncement engenders the same from competitors.

For FPGA vendors, problems of preannouncement are exacerbated by having to deliver not only silicon but also software support tools. Customers must have confidence that a vendor will be able to protect the software purchase by supplying them with an uninterrupted flow of advanced silicon. Customers' investments in software provides FPGA vendors additional account control. In sum, FPGA vendors must continuously deliver advanced silicon to protect their software installed base, which is a strategic element of the FPGA vendor's battle plan.

Account control can be a double-edged sword. FPGA and PMD vendors that stumble when attempting to deliver new devices to an installed base risk alienating customers. Vendors that have stumbled in the past find that recapturing customers that have defected to other suppliers is extremely difficult. In short, vendor credibility is seriously tarnished. We believe that these product transitions, and to a lesser extent the economy, will impact financial performance of the CPLD market. Various preannouncements by several vendors are also likely to give recent FPGA market entrants a window, albeit narrow, to win disenchanted customers.

CPLD Market Outlook

In some ways the CPLD industry parallels the CMOS gate array industry. Indeed, many FPGA vendors view the technology as a direct replacement for gate arrays. Dataquest expects the high price of FPGAs to prevent the technology from threatening the 10,000-gate-and-above gate array market for at least two years. Yet, in our view, because there are a range of similarities between the FPGA and gate array markets, it is useful to briefly explore the historical market dynamics of this arena.

Figure 2 compares year-to-year growth rates of CMOS gate arrays and CMOS PLDs. After the first three years, CMOS gate array growth declined rapidly, leveling off by the mid-1980s. The declining growth rates stemmed from price pressure caused by a myriad of competitors entering the market as well as an economic downturn in high-technology industries during that period. We believe that the CPLD industry is facing a similar future, although projected growth rates of FPGAs and PMDs will remain higher than those of the gate array market.

Projected growth rates of the CMOS PLD and CMOS gate array markets closely parallel each other, with CMOS PLD rates consistently higher than gate array. Figure 2 plots Table 2 data and

Table 1
Percentage of Worldwide 1990 PLD Units, by Pin Count

	Pin Count				
	<28	28-44	45-84	>84	Total
PLA	89	9	2	0	100
PMD	21	52	27	0	100
FPGA	1	5	85	9	100

Source: Dataquest (December 1991)

reflects the most recent update to our CMOS PLD forecast. (CMOS PLD category includes SPLDs, PMDs, and FPGAs.) We have adjusted our previous forecast to reflect the combination of the softening economy and supply-side product transitions. We expect the market to continue experiencing robust growth as the next generation of devices becomes production viable in 1992 and 1993. Dataquest's research indicates that a significantly larger percentage of the market expects to use FPGA and CPLD technology for its next generation of product designs.

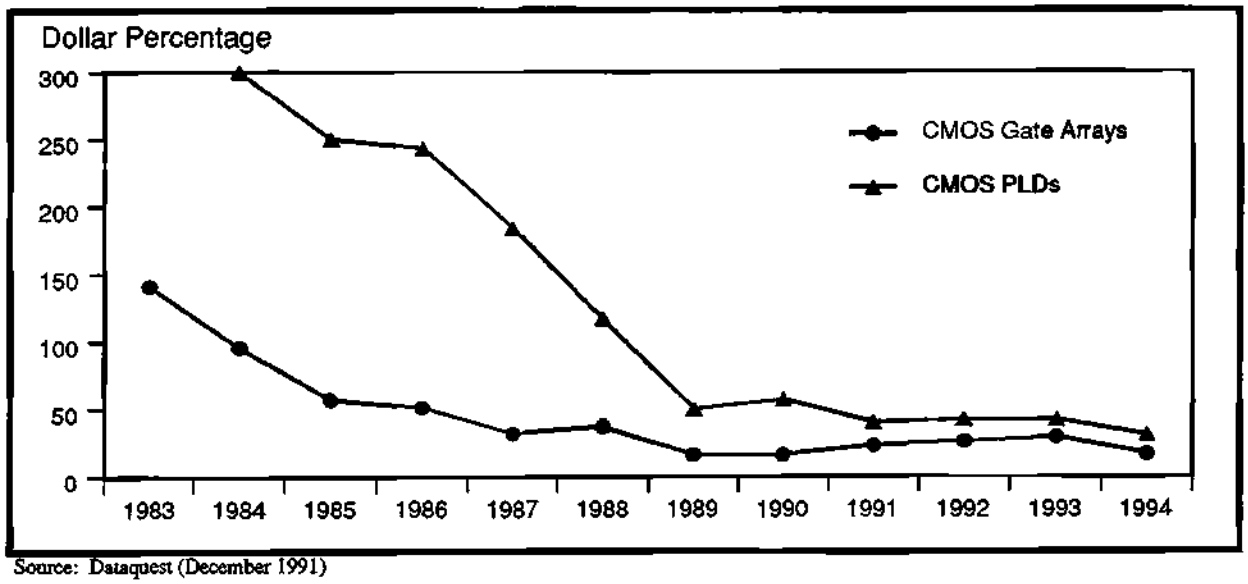
We believe that CMOS PLDs will not experience as rapid profit margin erosion as gate arrays have over the past five years. Product differentiation among vendors in the CMOS PLD camp should help sustain profit margins. However, average selling prices will certainly fall as PLD suppliers attempt to compete more aggressively against new FPGA market entrants such as Concurrent Logic, Crosspoint Solutions, and Quicklogic as well as against the lower-priced gate array technology alternative.

Dataquest Perspective

The recent slowdown in the CMOS PLD market can be attributed to the softening economy and the corresponding downturn in SPLD sales, as well as to product transitions of both the CPLD and FPGA vendors. Despite the impending weak financial reports from various CMOS PLD makers, Dataquest believes that the overall outlook for the PLD market is bright. In particular, PMDs and FPGAs will continue experiencing healthy growth as the coming generation of devices becomes production viable. Finally, we expect the overall PLD market to experience growth rates significantly higher than in the CMOS gate array market for the foreseeable future. We also anticipate profit margins for CPLDs and FPGAs to remain healthy, despite the influx of new players entering the market. ■

By Robert Beachler and Ron Collett

Figure 2
Worldwide Year-to-Year Dollar Percentage Growth, CMOS Gate Arrays and CMOS PLDs



Source: Dataquest (December 1991)

Table 2
Worldwide CMOS PLD Consumption
(Millions of Dollars)

	1989	1990	1991	1992	1993	1994	1995
CMOS PLDs	258	405	565	802	1,135	1,487	1,859
Growth (%)		57.0	39.5	42.0	41.5	31.0	25.0

Source: Dataquest (December 1991)

Product Analysis

The ASIC Battle Rages On

Cell-based ICs (CBICs) have been in a design war with gate arrays since their inception in the late 1960s. Gate arrays entered the electronic system design market a few years prior to CBICs and were quick to establish a dominant position. CBIC product designers continue to search for new weapons in the form of unique cell libraries to attack the well-entrenched gate array product. Gate array product designers have a battle plan of their own and a new weapon called an embedded gate array. Which product will win the war? This article discusses the probable outcome.

ASIC Evolution

Dataquest defines gate arrays and cell-based ICs as follows:

- Gate arrays—These application-specific integrated circuits (ASICs) contain a configuration of uncommitted elements in a prefabricated base wafer. They are customized by interconnecting the elements with one or more routing layers. Included in this category are traditional gate arrays (channeled and sea-of-gates architecture) and embedded gate arrays (channeled or sea-of-gates architecture that also include megacells such as SRAM diffused into the gate array base wafer).
- Cell-based ICs (CBICs)—These ASICs are customized using a full set of masks and use automatic place and route tools. Included in this category are traditional standard cells (fixed-height/fixed-width cells) as well as megacells (variable-height/variable-width cells) and compiled cells.

To get a better understanding of ASIC products, it is helpful to examine the ASIC product evolution (see Figure 1).

The first gate arrays were introduced to the industry in the mid-1960s by companies such as Fujitsu and IBM. They consisted of a configuration of uncommitted logic elements (32 gates) on a prefabricated base wafer. The elements were then customized by applying one final mask layer of interconnect. Most gate arrays were used for replacement of standard logic until the early 1980s, when higher-gate-count devices emerged and made single-chip systems practical.

Memory blocks were brought on-chip in 1984. Complex cells such as processor cores emerged in 1985. By 1988, RISC on-chip microprocessor cores were announced and maximum densities had reached 100,000 usable gates. Today, large SRAM blocks and microprocessors are available, and maximum chip complexities are reaching 200,000 usable gates.

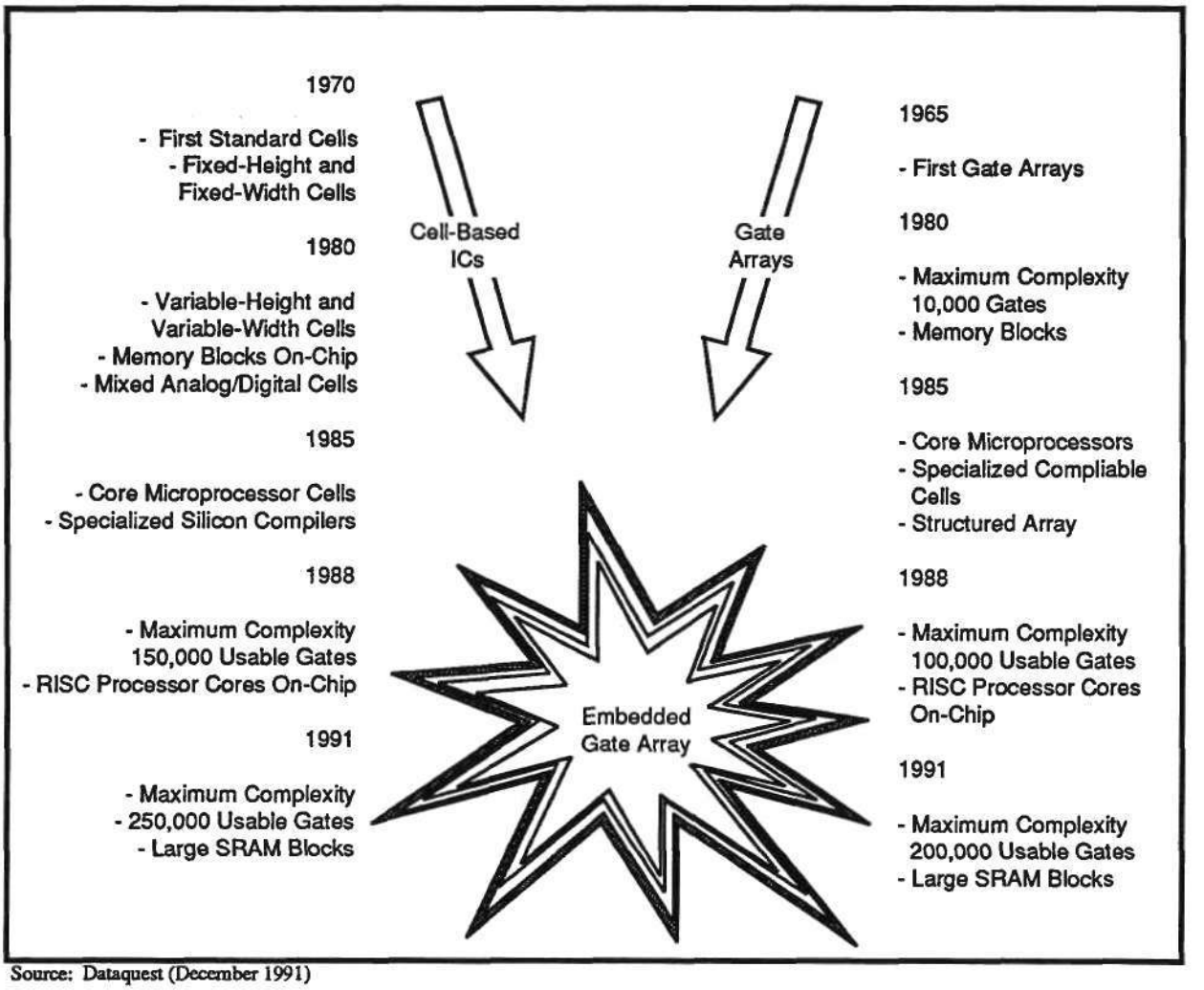
Cell-based ICs or standard cells did not emerge until a few years after the first gate arrays. IBM was again a leader in this area. The company followed its master slice approach, which used generic gate arrays, with what IBM called the "open part number set" consisting of a library of cells. Early standard cells started with fixed-height and fixed-width cells, which were implemented through the late 1970s.

After several years of development, the area inefficiency of fixed-height/fixed-width cells led to the addition of fixed-height/variable-width cell libraries. This was an interim stop on the way to today's variable-height/variable-width cell libraries. Megacells evolved as an aid to further improve efficiency in CBIC design, eliminating the need to reinvent the wheel every time a complex cell is needed. Memory blocks were brought on-chip in 1982, mixed analog/digital cells in 1984, and core microprocessors in 1985. Today, microprocessor cores and large SRAM blocks are available, and maximum chip complexities reach 250,000 gates.

During 1985, the embedded gate arrays concept was started by LSI Logic Corporation with a product called Structured Arrays, which offered metal-configurable memory and large dedicated building blocks called megacells added to a logic array. The product was unsuccessful because new technology was needed to implement the product strategy. The product was five years ahead of its time.

In 1990, ASIC suppliers throughout the world began announcing products that used a similar concept with new technology and a new name—it is now called an embedded gate array. Instead of using metal-configurable memory and metal-configurable dedicated building blocks, these cells are now diffused in an embedded gate array base wafer that is more efficient than Structured Arrays. Embedded gate arrays offer reduced die size and increased performance when compared with structured arrays and traditional gate arrays. In short, embedded gate arrays offer reduced risk and turnaround time associated with gate arrays, along with increased functionality and performance associated with CBICs. Embedded gate arrays

Figure 1
ASIC Product Evolution



Source: Dataquest (December 1991)

are included in the gate array category because they are built from a prefabricated base wafer and the random logic is customized using the final routing layers.

ASIC Product Analysis

What Product Is Winning the War?

Figure 2 shows the percentage of 1990 worldwide design starts and dollars captured by gate arrays and cell-based ICs. Cell-based ICs have higher unit volumes per design than gate arrays, but fewer designs were implemented with CBIC technology. Indeed, in capturing 26 percent of the designs, CBICs managed to capture a higher percentage of ASIC revenue. However, gate arrays are winning the war in both design starts and revenue.

Where Is the War Being Fought?

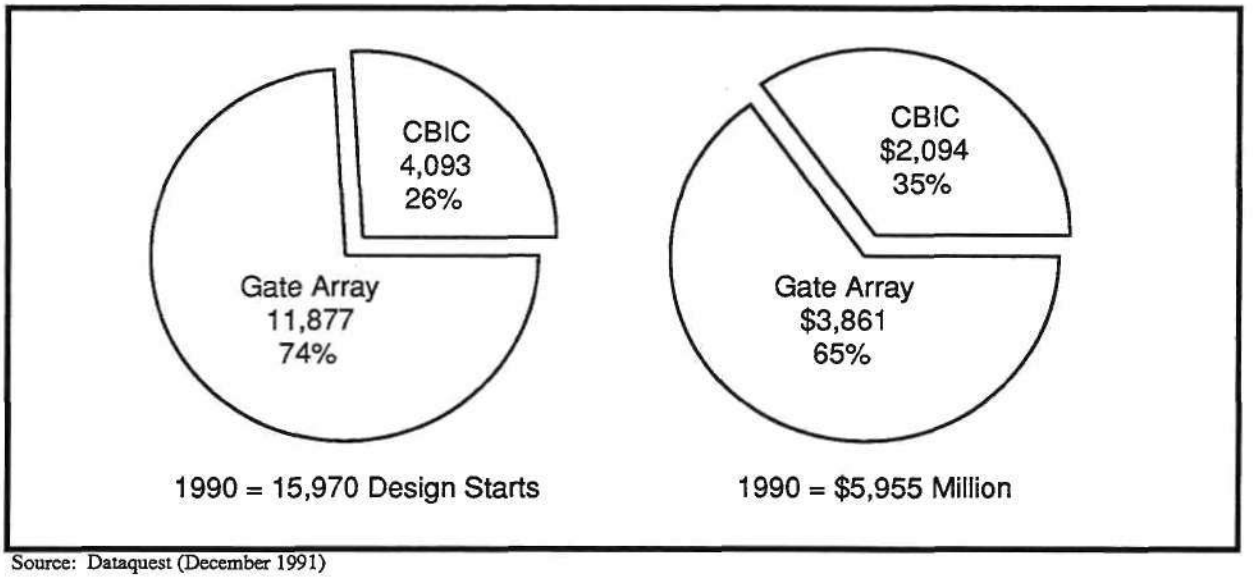
Although gate arrays dominate the Japan market, CBICs are more popular in North America (see Figure 3). This phenomenon has a direct correlation with the origins of the leading ASIC suppliers. Four of the top five leading gate array suppliers are Japan-based, while four of the top five CBIC suppliers are headquartered in North America (see Figure 4).

Design Starts by Gate Count

Figure 5 contrasts the 1990 MOS North American gate array and CBIC design starts by gate count. Dataquest analysis reveals the following important points:

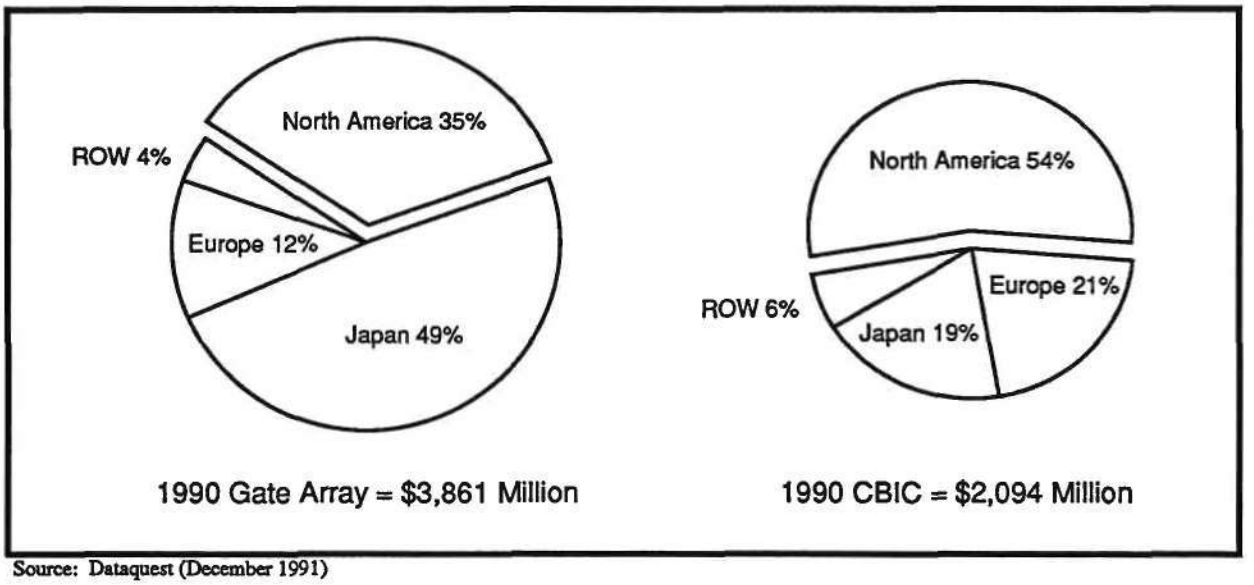
- The most cost-effective gate count in 1990 for both gate arrays and CBICs was in the 10,000- to 20,000-gate range.

Figure 2
Estimated 1990 Worldwide Gate Array and CBIC Design Starts and Dollar Consumption



Source: Dataquest (December 1991)

Figure 3
Estimated 1990 Worldwide Gate Array and CBIC Dollar Consumption, by Region



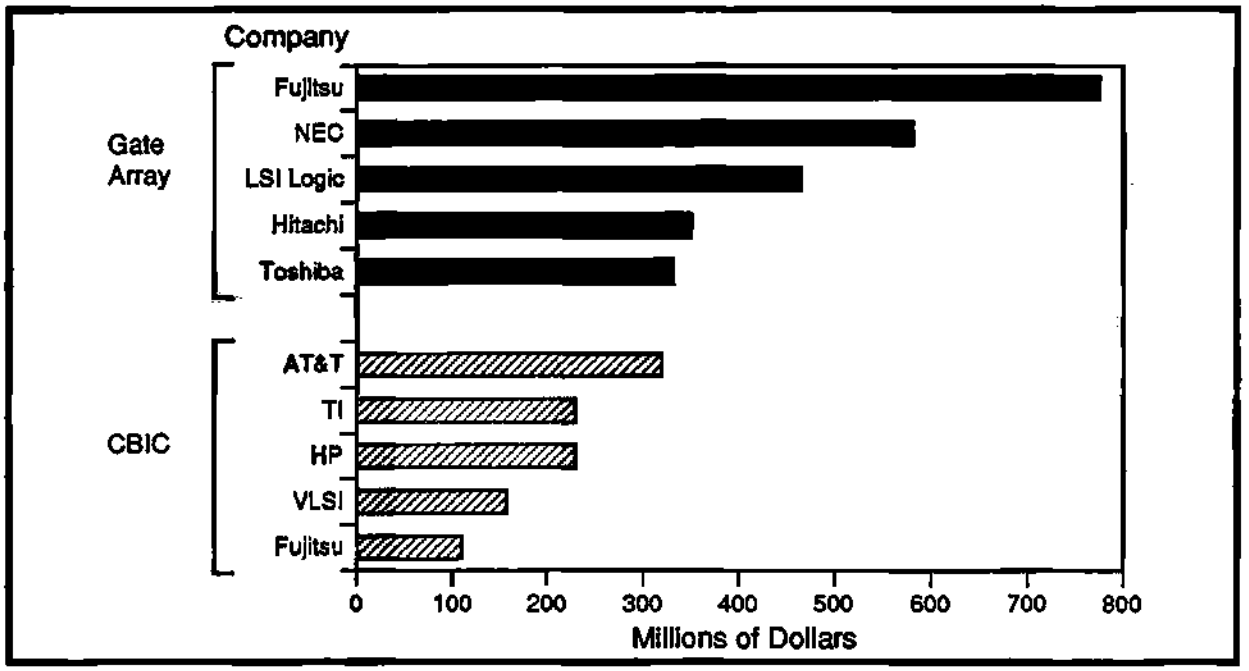
Source: Dataquest (December 1991)

- Gate arrays have traditionally been the low-cost vehicle for consolidating random logic and programmable logic devices (PLDs); thus, gate arrays dominated CBICs below 10,000 gates.
- CBICs have traditionally been used in applications requiring large functional blocks such as a 128K SRAM or a microprocessor/microperipheral; hence, CBICs captured a high percentage of designs above 70,000 gates.

Design Starts by Function

Figure 6 contrasts the 1990 MOS North American gate array and CBIC design starts by function. Figure 7 shows the percentage of 1990 North American MOS gate array and CBIC

Figure 4
1990 Top Five Worldwide Gate Array and CBIC Suppliers (Millions of Dollars)

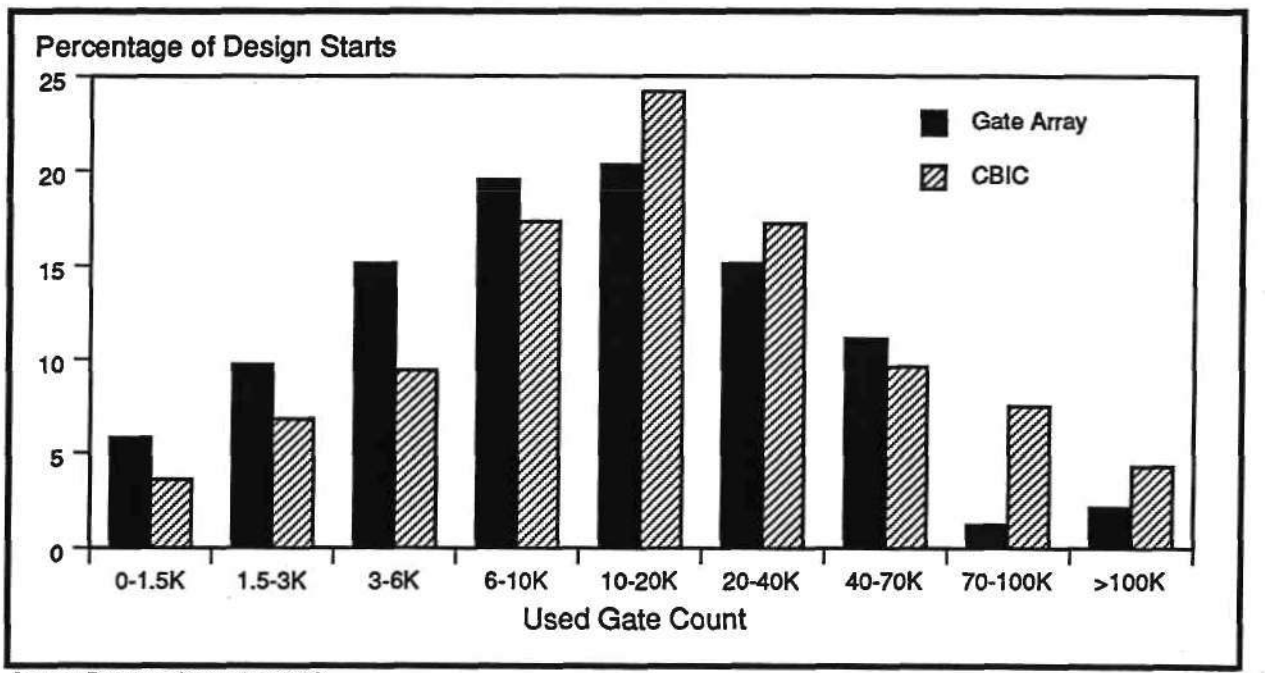


Source: Dataquest (December1991)

design starts that incorporated memory, by size of memory. Dataquest analysis from these figures is as follows:

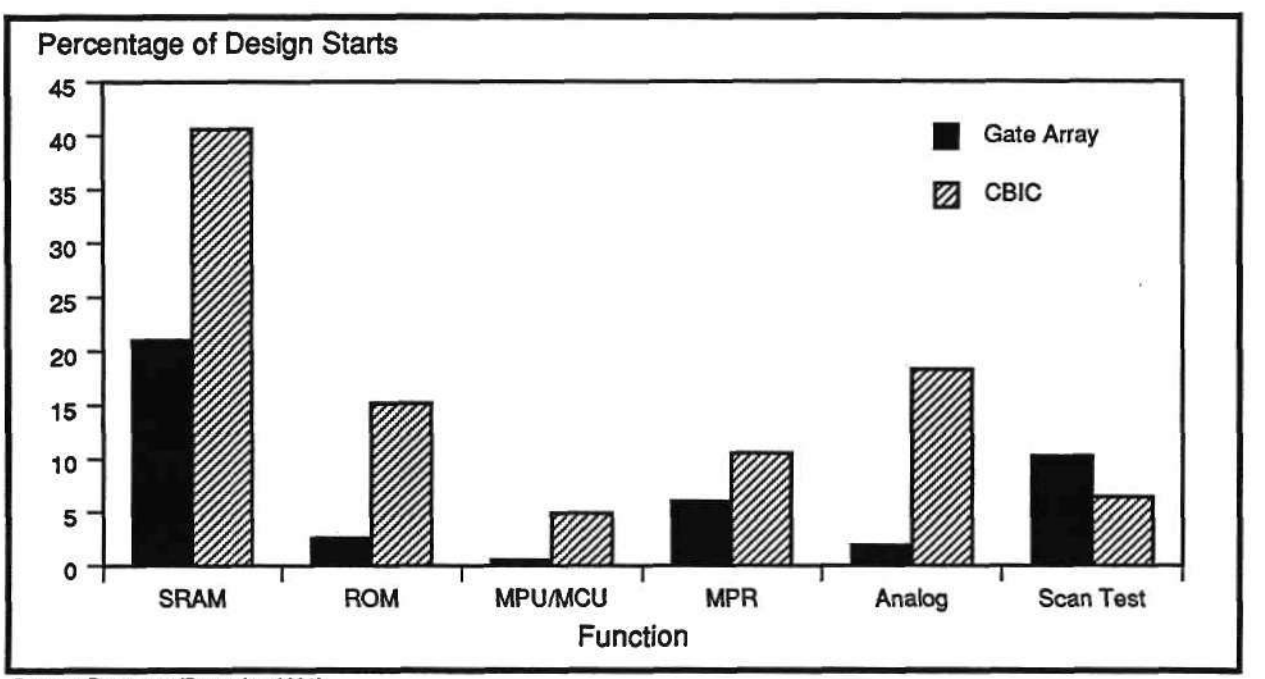
- Although SRAM is the most popular on-chip function in both gate arrays and CBICs, the rate of change in the percentage of designs that had on-chip SRAM is much higher for gate arrays than CBICs. Gate arrays went from 13 percent of the 1989 designs having on-chip SRAM to 21 percent in 1990, while CBIC design starts only grew from 39 percent to 40 percent. SRAMs implemented with CBICs have traditionally been five to seven times more silicon-efficient than metal-configured SRAMs in gate arrays. The dramatic increase of on-chip gate array SRAMs is because of suppliers offering much higher raw gate counts than before (more gates to use for the metal-configured SRAMs) and because of the availability of embedded gate arrays that have large SRAM blocks. Gate arrays with diffused SRAM blocks are just as silicon-efficient as implementing SRAMs in CBICs and are now emerging in applications that are SRAM-intensive.
- Because CBICs have traditionally been more silicon-efficient for implementing SRAM, not only were there more 1990 CBIC designs with on-chip SRAM, CBIC designs also had larger memories (see Figure 7).
- ROM is more cost-effective in a CBIC than is a traditional gate array; therefore, 15 percent of the 1990 CBIC designs had on-chip ROM compared to only 3 percent of the 1990 gate array designs.
- Despite the myriad of announcements of on-chip microprocessing units/microcontroller units (MPUs/MCUs), less than 1 percent of the gate array designs and less than 5 percent of the CBIC designs had on-chip MPUs/MCUs in 1990. As the numbers indicate, there has been slow user acceptance of on-chip ASIC microprocessors because of their high design cost, high device cost, and difficult testing issues.
- Most on-chip microperipherals (MPRs) in gate array and CBICs during 1990 were 82XX peripherals.
- Analog functions are difficult to implement with transistors within gate arrays. Therefore, in 1990, about 95 percent of the gate array designs that had analog functions were pure analog arrays (no digital) and only 5 percent

Figure 5
1990 Estimated North American MOS ASIC Design Starts, by Gate Count



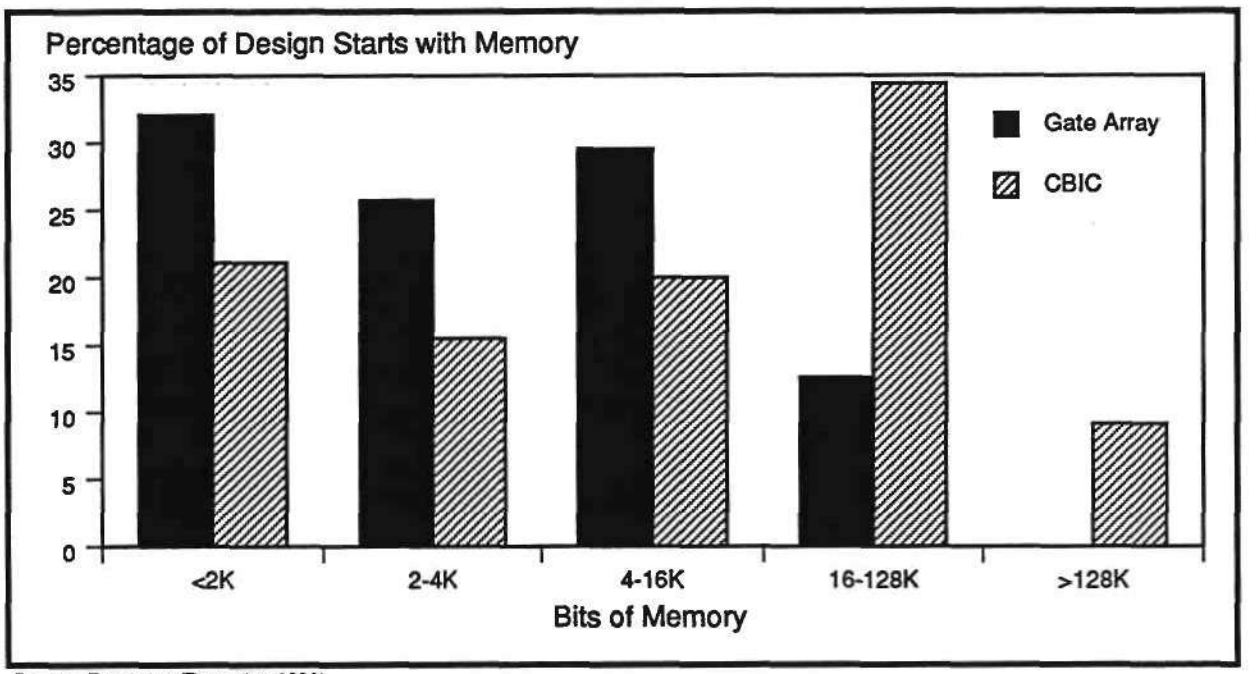
Source: Dataquest (December 1991)

Figure 6
1990 Estimated North American MOS ASIC Design Starts, by Function



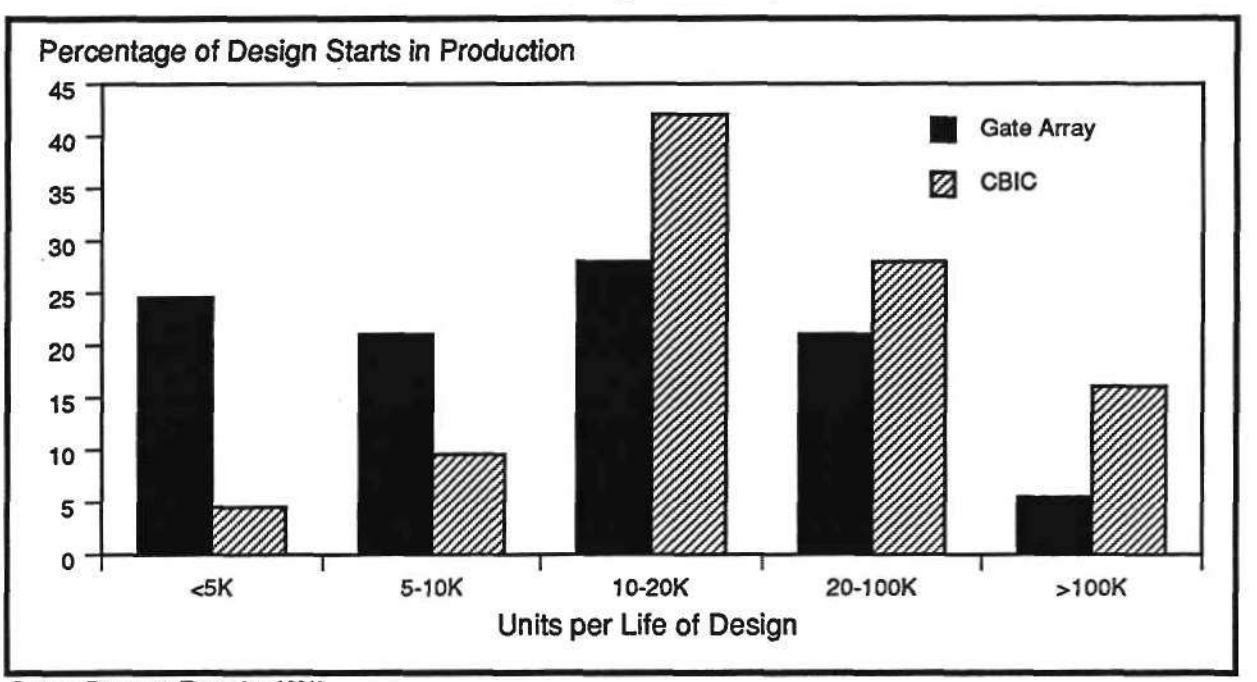
Source: Dataquest (December 1991)

Figure 7
1990 Estimated North American MOS ASIC Design Starts, by Memory Bits



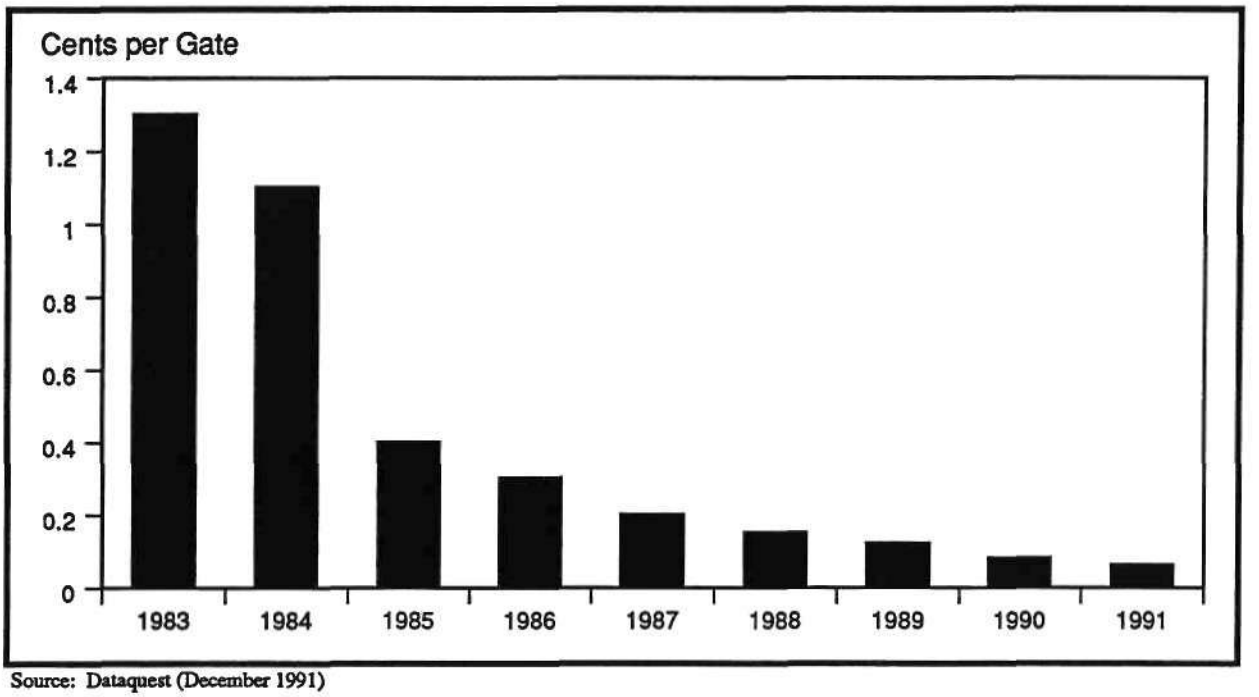
Source: Dataquest (December 1991)

Figure 8
1990 Estimated North American MOS ASIC Design Starts, by Unit Volume



Source: Dataquest (December 1991)

Figure 9
Estimated North American CMOS Gate Array Pricing (3,000 Gates, 15,000-Unit Volume)



Source: Dataquest (December 1991)

were mixed analog/digital arrays. On the other hand, CBICs are well suited to optimize the analog functions and mix them with digital functions. Therefore, about 95 percent of CBIC designs were mixed analog/digital designs and only 5 percent were pure analog CBICs. Common analog functions being implemented in ASICs include: comparators, amplifiers, voltage regulators, interface drivers, data converters, and phase-locked loops.

- As gate densities continue to rise at a rapid rate, on-chip testing has become critical for both gate arrays and CBICs. JTAG compatibility is emerging as the industry standard for board-level testing. Our analysis also shows a higher use of built-in self test (BIST) in CBICs than gate arrays for memory testing.

Units and Pricing Trends

Figure 8 shows estimated North American ASIC unit volume for the life of designs in production during 1990. We note the following trends:

- The most common 1990 unit volume for gate arrays and CBICs ranged from 10,000 to 20,000 units.
- Gate arrays have been more cost-effective than CBICs in low volumes (below 10,000 units) because of their lower design cost.
- Military users prefer gate arrays over CBICs because they purchase in low volumes. Therefore, we believe that military designs accounted for a large portion of the gate array designs below 5,000 units.
- CBICs have traditionally been more cost-effective than gate arrays in high volumes (greater than 100,000 units) because they have a smaller die size.

Although CBICs cost less to manufacture than do gate arrays (given the same set of functions because the die is smaller), CBICs will not necessarily cost less than gate arrays to the user in high volume. Gate arrays experienced rapid price erosion because of oversupply during the last seven years. Figure 9 shows the severe price erosion on a low-gate count CMOS gate array in North America. CBIC prices have also declined but at a much slower rate than gate arrays because of the reduced number of suppliers. Therefore, in high volumes, gate arrays are often less expensive to the user than are CBICs because there is always one or two gate array suppliers willing to slash the gate array price below that of the CBIC suppliers.

Dataquest Perspective

The dividing line between gate array applications and CBIC applications is in a state of flux. CBICs have historically been used in high-volume applications as well as in applications

Table 1
ASIC Feature Trade-Off Matrix

Feature	Traditional Gate Array	Embedded Gate Array	CBIC
Memory Efficeiency	Low	High	High
Die Size	Large	Medium	Small
Device Cost	Highest	Low	Lowest
NRE Cost	Low	High	High
Retooling Cost	Low	Low	High
Retooling Time	Short	Short	Long
Performance	Medium	Medium-High	High
Risk	Lowest	Low	Highest

Source: Dataquest (December 1991)

that need increased functionality such as large SRAM blocks. Compared with CBICs, gate arrays offer quicker time to market, lower risk, and lower design cost. Embedded gate arrays have now emerged as a crossbreed and are a viable option to CBICs and traditional gate arrays.

Embedded gate arrays and CBICs are the most efficient technologies for implementing memory and other large functional blocks. Embedded gate arrays still retain a portion of the chip area available for random logic gates, so die size and device cost will not be quite as good as with CBICs but will be far better than with traditional gate arrays. Although the first embedded gate array design cost or nonrecurring engineering charge is the same as for CBIC, big savings occur when the design is retooled. Most high-density gate array designs are retooled two to three times because they do not meet system requirements. With embedded gate arrays, only the random logic will need to be reconfigured with the final layers of interconnect; therefore, retooling turnaround time and cost are far less than for CBICs. With reduced turnaround time and cost comes embedded gate arrays' reduced risk (see Table 1).

Although embedded gate arrays only accounted for 1 percent of the 1990 North American gate array designs, demand is strong for such a product. As mentioned earlier, embedded gate arrays are efficient and satisfy the strong need for on-chip SRAM. Dataquest believes that larger SRAMs (128K and 256K) will be diffused in gate array base wafers and used for cache memory. Furthermore, we believe that other functions such as SCSI, arithmetic logic units, multiplier-accumulators, first in/first out memories, direct memory access controllers, cache controllers, and 82XX microperipherals will also be diffused in the gate array, fueling the growth of the embedded gate array market.

In conclusion, Dataquest believes that gate arrays (including traditional gate arrays and embedded gate arrays) will continue to remain the dominant technology throughout the decade. Furthermore, we believe that embedded gate arrays will wrestle market share from the CBIC market because they will increasingly be capable of matching the functionality and performance of CBICs, with reduced cost and risk. However, Dataquest does not believe that embedded gate arrays will replace traditional gate arrays or CBICs in the foreseeable future. Each product brings value to the market. Hence, we believe that each product will coexist and system designers will select the products that best suit their unique applications.

By Bryan Lewis

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Dataquest Perspective

ASICs *Worldwide*

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Market Analysis

PLD Prospects in the Face of a Weak Economy

Although the CMOS programmable logic devices (PLDs) market continues to outpace the growth rate of the overall semiconductor market, efficient manufacturing and strong distribution have not been enough to insulate it from widespread slowing in the electronics industry. There is little growth expected for the fourth quarter of 1991. Is this a short-term aberration or does it spell trouble for the PLD industry? Dataquest analyzes the dynamics of the CMOS PLD market and predicts its future.

By Robert Beachler and Ron Collett

Page 2

Product Analysis

The ASIC Battle Rages On

Cell-based ICs have long been involved in a design war with gate arrays, which entered the electronic system design market a few years prior to CBICs and quickly established domination. CBIC product designers still search for new weapons in the form of unique cell libraries to attack the well-entrenched gate array product. But these gate array product designers can counter with a weapon of their own: the embedded gate array. In this article, Dataquest examines the probable winner in this battle.

By Bryan Lewis

Page 5

Market Analysis

PLD Prospects in the Face of a Weak Economy

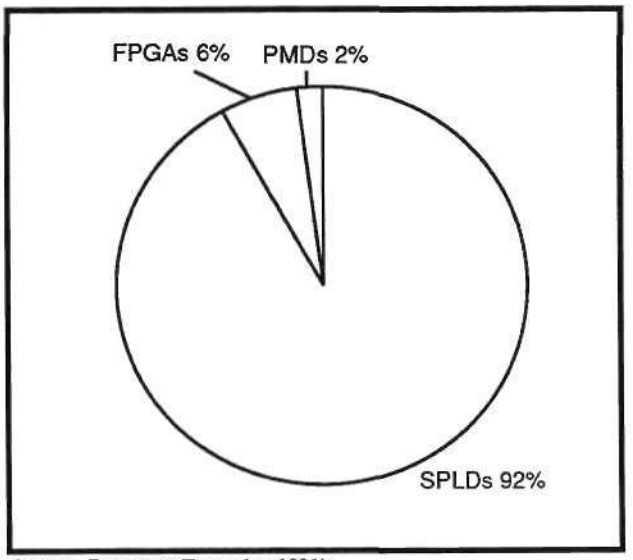
CMOS programmable logic devices (PLDs), which include simple PLDs (SPLDs), programmable multilevel devices (PMDs), and field programmable gate arrays (FPGAs), are the fastest-growing segment of the semiconductor market. Their projected five-year compound annual growth rate (CAGR) is 36 percent. Yet high demand, efficient manufacturing, and strong distribution have not been enough to insulate the segment from the widespread downturn in the electronics industry. Indeed, recent announcements by PLD manufacturers suggest that the fourth quarter of 1991 will show little if any growth compared with the previous quarter. Despite the slowdown, Dataquest believes that this condition is a short-term aberration. We expect market conditions to improve in 1992 as more users adopt the technology, a larger segment of the market uses the technology in production, and several new FPGA suppliers enter the market.

Weathering the Downturn Demands Diversified PLD Product Portfolios

Segmenting the PLD market into its submarkets reveals that the SPLD market is less immune to downturns in the electronics industry than are its FPGA and PMD cousins. Because of their similarities, PMDs and FPGAs are grouped by Dataquest into a complex PLD (CPLD) market. Unlike FPGAs and PMDs, the SPLD is a mature product that has reached commodity status. So profitability and high revenue depend heavily on high-volume shipments. About 80 percent of SPLDs shipped are used in data processing and communications markets. It is not surprising that the recent electronics market slowdown has impacted both segments, especially data processing, which of course includes personal computers. The lion's share of the total PLDs shipped are in fact SPLDs, which include PALs, FPLAs, and GALs (see Figure 1).

It is also not surprising that several CMOS PLD manufacturers announced that the fourth quarter of 1991 will witness flat growth, compared with the previous quarter. For manufacturers such as Lattice Semiconductor and Integrated CMOS

Figure 1
Estimated 1990 Worldwide CMOS PLD Units, by Product



Source: Dataquest (December 1991)

Technology, whose primary PLD offerings fall into the SPLD camp, the current market conditions are especially challenging. The primary avenue for growth among these vendors is reapportionment of market share. In short, they must "steal sockets" and wrestle existing market share from competitors. Expansion of the SPLD market is limited by the following factors:

- The high level of market penetration achieved by these products
- The limited number of new applications that SPLDs can target
- The large number of suppliers serving this market
- The limited differentiation among SPLD products
- The availability of substitute products, namely PMDs and FPGAs

Unlike the SPLD market, the CPLD market is not saturated. Devices in these categories continue to find new applications and in fact are readily capturing sockets once the exclusive territory of standard logic, SPLDs, and, in some cases, gate arrays. Because PMDs and FPGAs are finding use across a broad range of applications, they are less susceptible to industry-specific downturns. Thus, for most CPLD suppliers, weathering the current economic downturn is not nearly as daunting as the challenges facing SPLD-only vendors.

The fact that the business models of most CPLD vendors do not depend heavily on high-volume applications also works in their favor. This situation, of course, contrasts sharply with the models employed by SPLD vendors. The current economic downturn will continue to impact those suppliers relying on high-volume, low-cost products such as the current generation of 20- and 24-pin devices. As Table 1 shows, the majority of high-end PLDs and FPGAs are shipped in packages that boast 28 to 84 pins. Segmenting a supplier's product revenue portfolio by pin count is a quick way to get an indication of that company's business model, as well as its ability to weather economic downturns. The fragility of such a business model that relies extensively on low-pin-count devices is clearly manifesting itself in today's market.

Vulnerability of PMDs and FPGAs

Despite the advantages that CPLDs hold over SPLDs, they are not fully immune to the economic flu gripping the electronics industry. The combination of a slowdown in military spending and a softening of the telecommunications and computer markets has caused some suppliers to re-evaluate heretofore bold expansion plans.

Several CPLD vendors have also not done much to help themselves lately by preannouncing products. FPGA makers are working hard not to fall into the trap of preannouncing products. As can be seen, however, preannouncements have a domino effect; one company's preannouncement engenders the same from competitors.

For FPGA vendors, problems of preannouncement are exacerbated by having to deliver not only silicon but also software support tools. Customers must have confidence that a vendor will be able to protect the software purchase by supplying them with an uninterrupted flow of advanced silicon. Customers' investments in software provides FPGA vendors additional account control. In sum, FPGA vendors must continuously deliver advanced silicon to protect their software installed base, which is a strategic element of the FPGA vendor's battle plan.

Account control can be a double-edged sword. FPGA and PMD vendors that stumble when attempting to deliver new devices to an installed base risk alienating customers. Vendors that have stumbled in the past find that recapturing customers that have defected to other suppliers is extremely difficult. In short, vendor credibility is seriously tarnished. We believe that these product transitions, and to a lesser extent the economy, will impact financial performance of the CPLD market. Various preannouncements by several vendors are also likely to give recent FPGA market entrants a window, albeit narrow, to win disenchanted customers.

CPLD Market Outlook

In some ways the CPLD industry parallels the CMOS gate array industry. Indeed, many FPGA vendors view the technology as a direct replacement for gate arrays. Dataquest expects the high price of FPGAs to prevent the technology from threatening the 10,000-gate-and-above gate array market for at least two years. Yet, in our view, because there are a range of similarities between the FPGA and gate array markets, it is useful to briefly explore the historical market dynamics of this arena.

Figure 2 compares year-to-year growth rates of CMOS gate arrays and CMOS PLDs. After the first three years, CMOS gate array growth declined rapidly, leveling off by the mid-1980s. The declining growth rates stemmed from price pressure caused by a myriad of competitors entering the market as well as an economic downturn in high-technology industries during that period. We believe that the CPLD industry is facing a similar future, although projected growth rates of FPGAs and PMDs will remain higher than those of the gate array market.

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PLA	89	9	2	0	100
PMD	21	52	27	0	100
FPGA	1	5	85	9	100

Source: Dataquest (December 1991)

reflects the most recent update to our CMOS PLD forecast. (CMOS PLD category includes SPLDs, PMDs, and FPGAs.) We have adjusted our previous forecast to reflect the combination of the softening economy and supply-side product transitions. We expect the market to continue experiencing robust growth as the next generation of devices becomes production viable in 1992 and 1993. Dataquest's research indicates that a significantly larger percentage of the market expects to use FPGA and CPLD technology for its next generation of product designs.

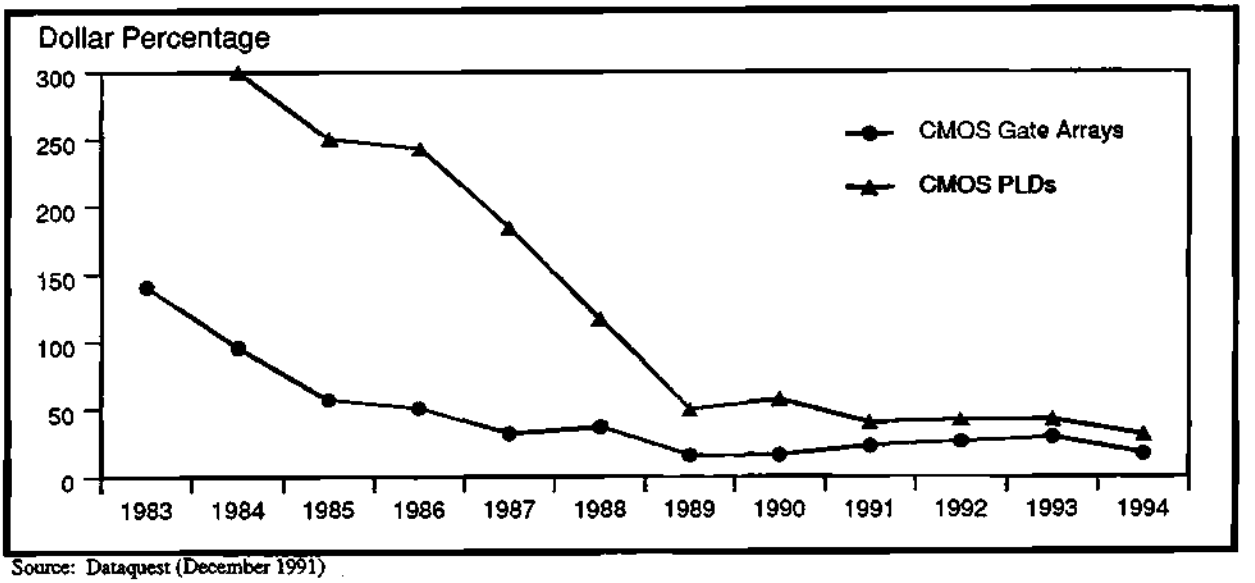
We believe that CMOS PLDs will not experience as rapid profit margin erosion as gate arrays have over the past five years. Product differentiation among vendors in the CMOS PLD camp should help sustain profit margins. However, average selling prices will certainly fall as PLD suppliers attempt to compete more aggressively against new FPGA market entrants such as Concurrent Logic, Crosspoint Solutions, and Quicklogic as well as against the lower-priced gate array technology alternative.

Dataquest Perspective

The recent slowdown in the CMOS PLD market can be attributed to the softening economy and the corresponding downturn in SPLD sales, as well as to product transitions of both the CPLD and FPGA vendors. Despite the impending weak financial reports from various CMOS PLD makers, Dataquest believes that the overall outlook for the PLD market is bright. In particular, PMDs and FPGAs will continue experiencing healthy growth as the coming generation of devices becomes production viable. Finally, we expect the overall PLD market to experience growth rates significantly higher than in the CMOS gate array market for the foreseeable future. We also anticipate profit margins for CPLDs and FPGAs to remain healthy, despite the influx of new players entering the market. ■

By Robert Beachler and Ron Collett

Figure 2
Worldwide Year-to-Year Dollar Percentage Growth, CMOS Gate Arrays and CMOS PLDs



Source: Dataquest (December 1991)

Table 2
Worldwide CMOS PLD Consumption
(Millions of Dollars)

	1989	1990	1991	1992	1993	1994	1995
CMOS PLDs	258	405	565	802	1,135	1,487	1,859
Growth (%)		57.0	39.5	42.0	41.5	31.0	25.0

Source: Dataquest (December 1991)

Product Analysis

The ASIC Battle Rages On

Cell-based ICs (CBICs) have been in a design war with gate arrays since their inception in the late 1960s. Gate arrays entered the electronic system design market a few years prior to CBICs and were quick to establish a dominant position. CBIC product designers continue to search for new weapons in the form of unique cell libraries to attack the well-entrenched gate array product. Gate array product designers have a battle plan of their own and a new weapon called an embedded gate array. Which product will win the war? This article discusses the probable outcome.

ASIC Evolution

Dataquest defines gate arrays and cell-based ICs as follows:

- Gate arrays—These application-specific integrated circuits (ASICs) contain a configuration of uncommitted elements in a prefabricated base wafer. They are customized by interconnecting the elements with one or more routing layers. Included in this category are traditional gate arrays (channeled and sea-of-gates architecture) and embedded gate arrays (channeled or sea-of-gates architecture that also include megacells such as SRAM diffused into the gate array base wafer).
- Cell-based ICs (CBICs)—These ASICs are customized using a full set of masks and use automatic place and route tools. Included in this category are traditional standard cells (fixed-height/fixed-width cells) as well as megacells (variable-height/variable-width cells) and compiled cells.

To get a better understanding of ASIC products, it is helpful to examine the ASIC product evolution (see Figure 1).

The first gate arrays were introduced to the industry in the mid-1960s by companies such as Fujitsu and IBM. They consisted of a configuration of uncommitted logic elements (32 gates) on a prefabricated base wafer. The elements were then customized by applying one final mask layer of interconnect. Most gate arrays were used for replacement of standard logic until the early 1980s, when higher-gate-count devices emerged and made single-chip systems practical.

Memory blocks were brought on-chip in 1984. Complex cells such as processor cores emerged in 1985. By 1988, RISC on-chip microprocessor cores were announced and maximum densities had reached 100,000 usable gates. Today, large SRAM blocks and microprocessors are available, and maximum chip complexities are reaching 200,000 usable gates.

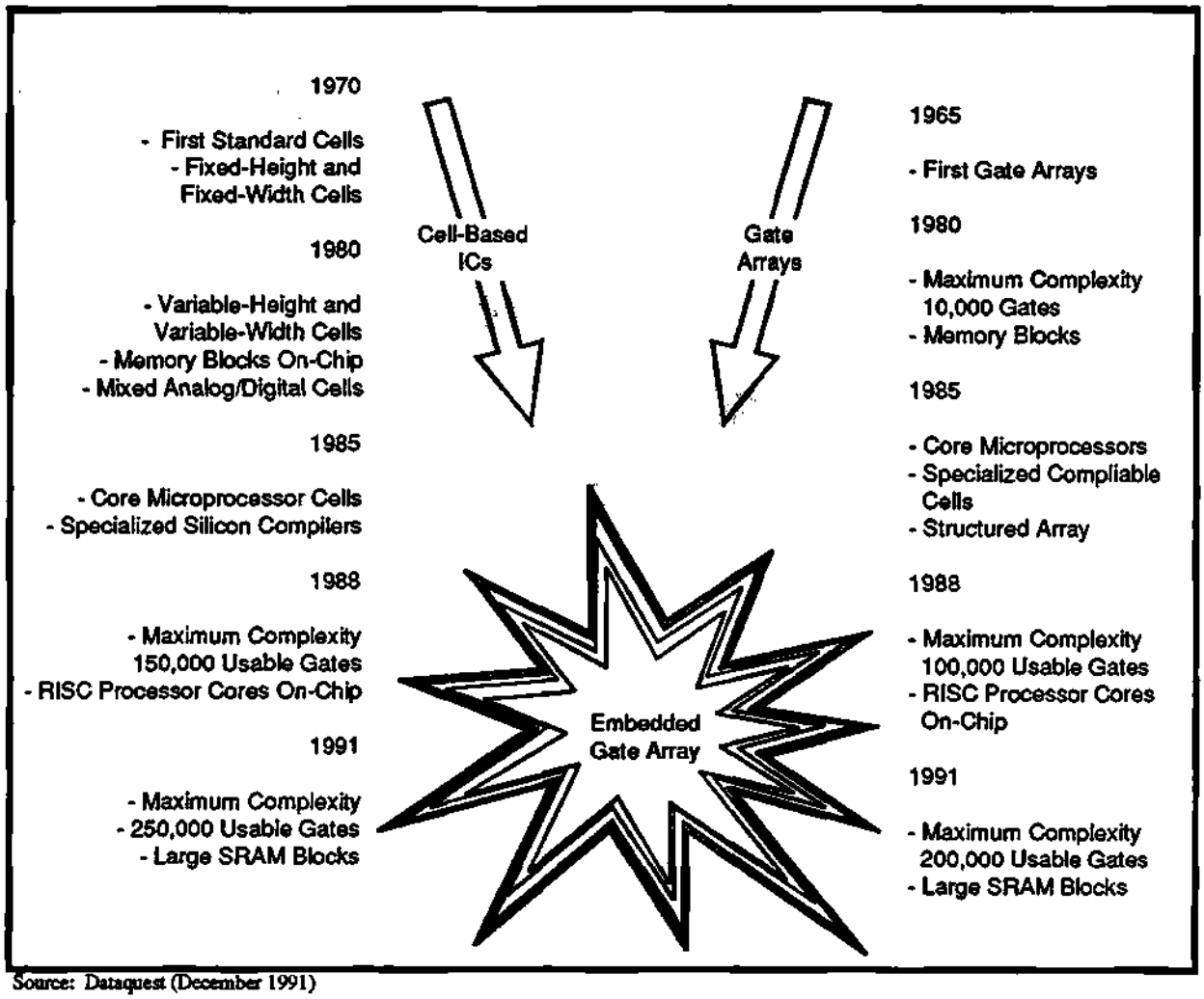
Cell-based ICs or standard cells did not emerge until a few years after the first gate arrays. IBM was again a leader in this area. The company followed its master slice approach, which used generic gate arrays, with what IBM called the "open part number set" consisting of a library of cells. Early standard cells started with fixed-height and fixed-width cells, which were implemented through the late 1970s.

After several years of development, the area inefficiency of fixed-height/fixed-width cells led to the addition of fixed-height/variable-width cell libraries. This was an interim stop on the way to today's variable-height/variable-width cell libraries. Megacells evolved as an aid to further improve efficiency in CBIC design, eliminating the need to reinvent the wheel every time a complex cell is needed. Memory blocks were brought on-chip in 1982, mixed analog/digital cells in 1984, and core microprocessors in 1985. Today, microprocessor cores and large SRAM blocks are available, and maximum chip complexities reach 250,000 gates.

During 1985, the embedded gate arrays concept was started by LSI Logic Corporation with a product called Structured Arrays, which offered metal-configurable memory and large dedicated building blocks called megacells added to a logic array. The product was unsuccessful because new technology was needed to implement the product strategy. The product was five years ahead of its time.

In 1990, ASIC suppliers throughout the world began announcing products that used a similar concept with new technology and a new name—it is now called an embedded gate array. Instead of using metal-configurable memory and metal-configurable dedicated building blocks, these cells are now diffused in an embedded gate array base wafer that is more efficient than Structured Arrays. Embedded gate arrays offer reduced die size and increased performance when compared with structured arrays and traditional gate arrays. In short, embedded gate arrays offer reduced risk and turnaround time associated with gate arrays, along with increased functionality and performance associated with CBICs. Embedded gate arrays

Figure 1
ASIC Product Evolution



Source: Dataquest (December 1991)

are included in the gate array category because they are built from a prefabricated base wafer and the random logic is customized using the final routing layers.

ASIC Product Analysis

What Product Is Winning the War?

Figure 2 shows the percentage of 1990 worldwide design starts and dollars captured by gate arrays and cell-based ICs. Cell-based ICs have higher unit volumes per design than gate arrays, but fewer designs were implemented with CBIC technology. Indeed, in capturing 26 percent of the designs, CBICs managed to capture a higher percentage of ASIC revenue. However, gate arrays are winning the war in both design starts and revenue.

Where Is the War Being Fought?

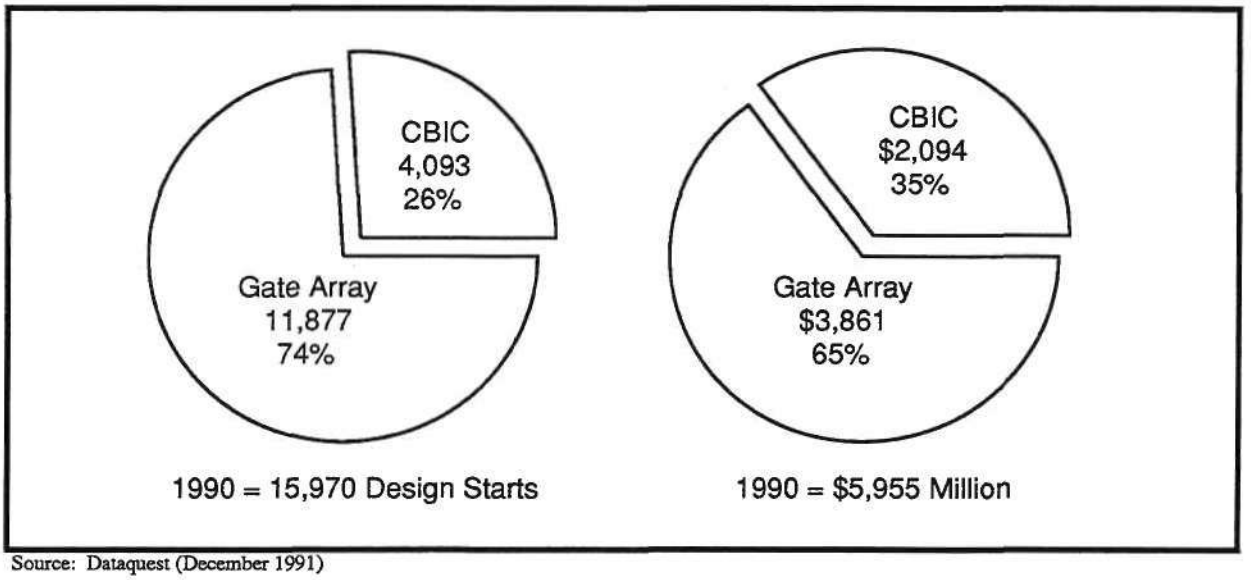
Although gate arrays dominate the Japan market, CBICs are more popular in North America (see Figure 3). This phenomenon has a direct correlation with the origins of the leading ASIC suppliers. Four of the top five leading gate array suppliers are Japan-based, while four of the top five CBIC suppliers are headquartered in North America (see Figure 4).

Design Starts by Gate Count

Figure 5 contrasts the 1990 MOS North American gate array and CBIC design starts by gate count. Dataquest analysis reveals the following important points:

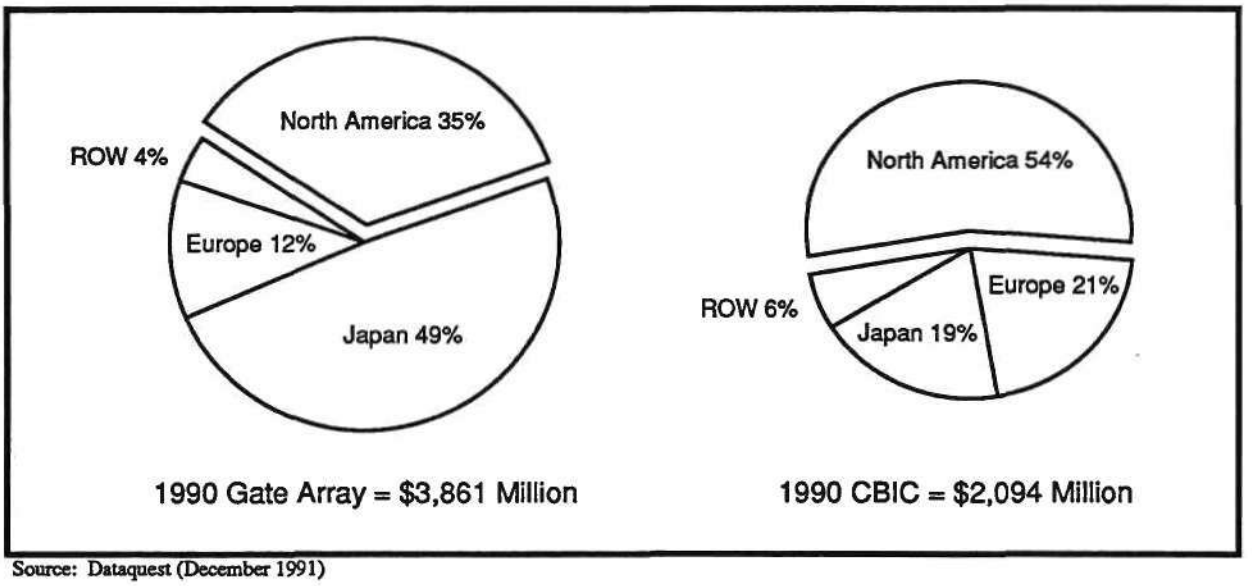
- The most cost-effective gate count in 1990 for both gate arrays and CBICs was in the 10,000- to 20,000-gate range.

Figure 2
Estimated 1990 Worldwide Gate Array and CBIC Design Starts and Dollar Consumption



Source: Dataquest (December 1991)

Figure 3
Estimated 1990 Worldwide Gate Array and CBIC Dollar Consumption, by Region



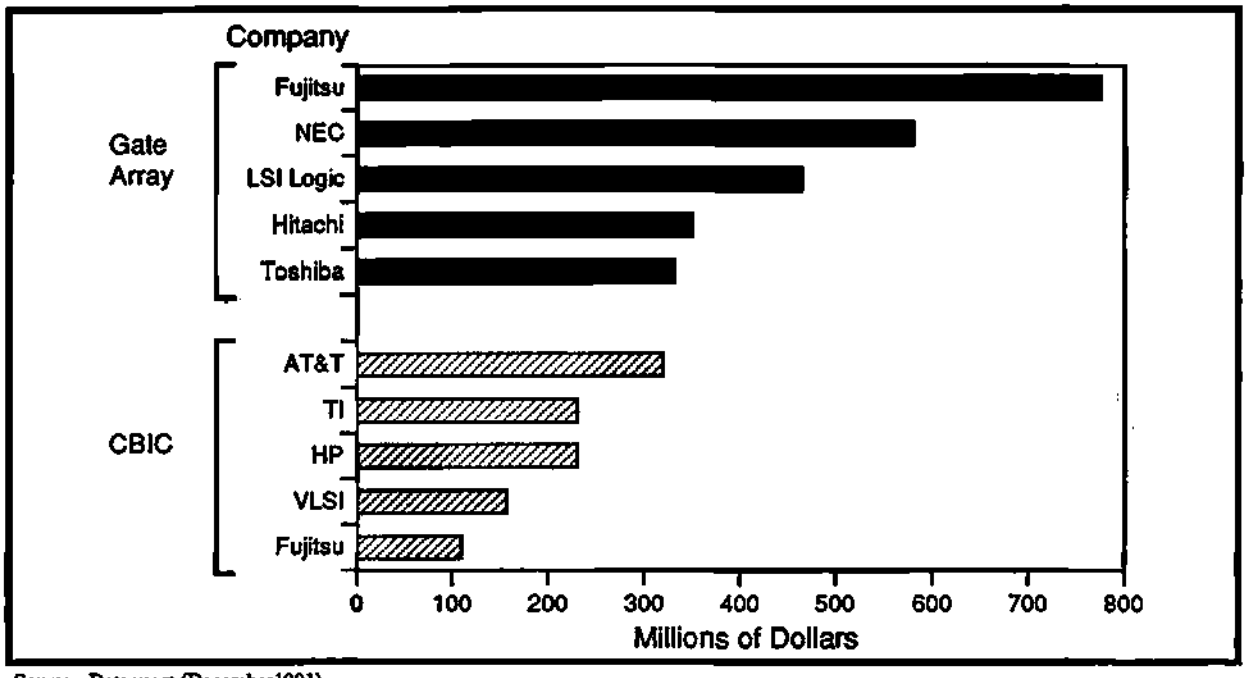
Source: Dataquest (December 1991)

- Gate arrays have traditionally been the low-cost vehicle for consolidating random logic and programmable logic devices (PLDs); thus, gate arrays dominated CBICs below 10,000 gates.
- CBICs have traditionally been used in applications requiring large functional blocks such as a 128K SRAM or a microprocessor/microperipheral; hence, CBICs captured a high percentage of designs above 70,000 gates.

Design Starts by Function

Figure 6 contrasts the 1990 MOS North American gate array and CBIC design starts by function. Figure 7 shows the percentage of 1990 North American MOS gate array and CBIC

Figure 4
1990 Top Five Worldwide Gate Array and CBIC Suppliers (Millions of Dollars)

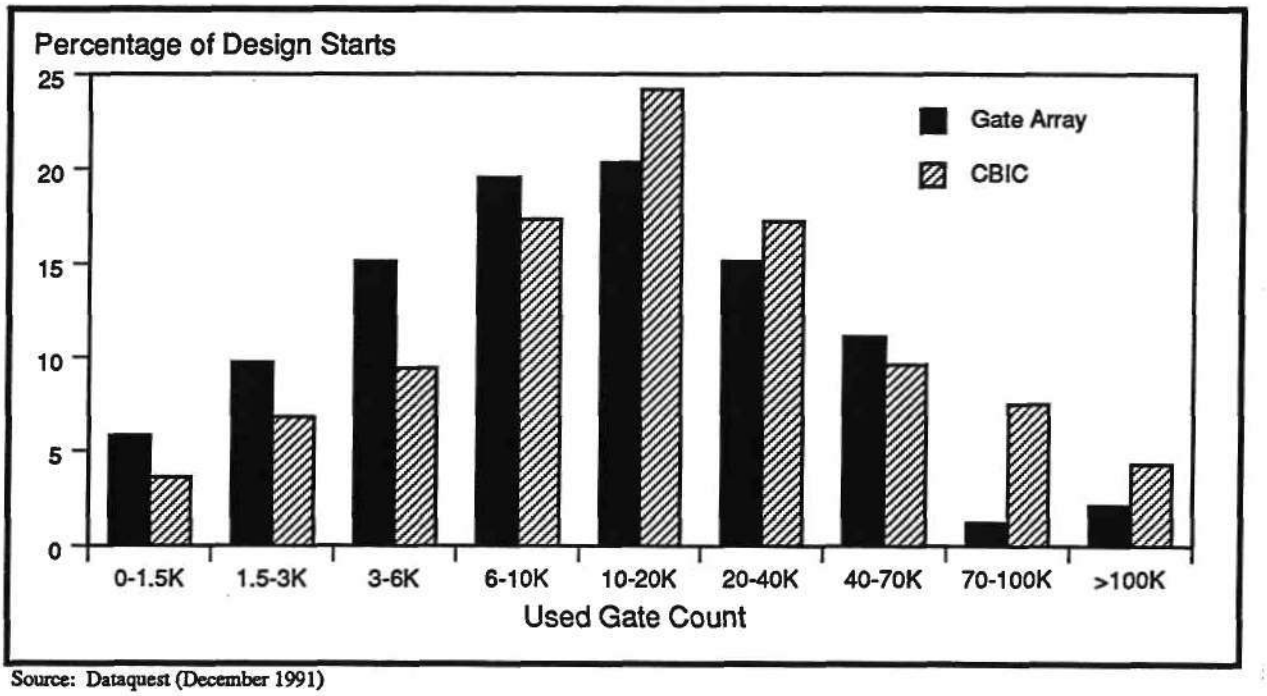


Source: Dataquest (December 1991)

design starts that incorporated memory, by size of memory. Dataquest analysis from these figures is as follows:

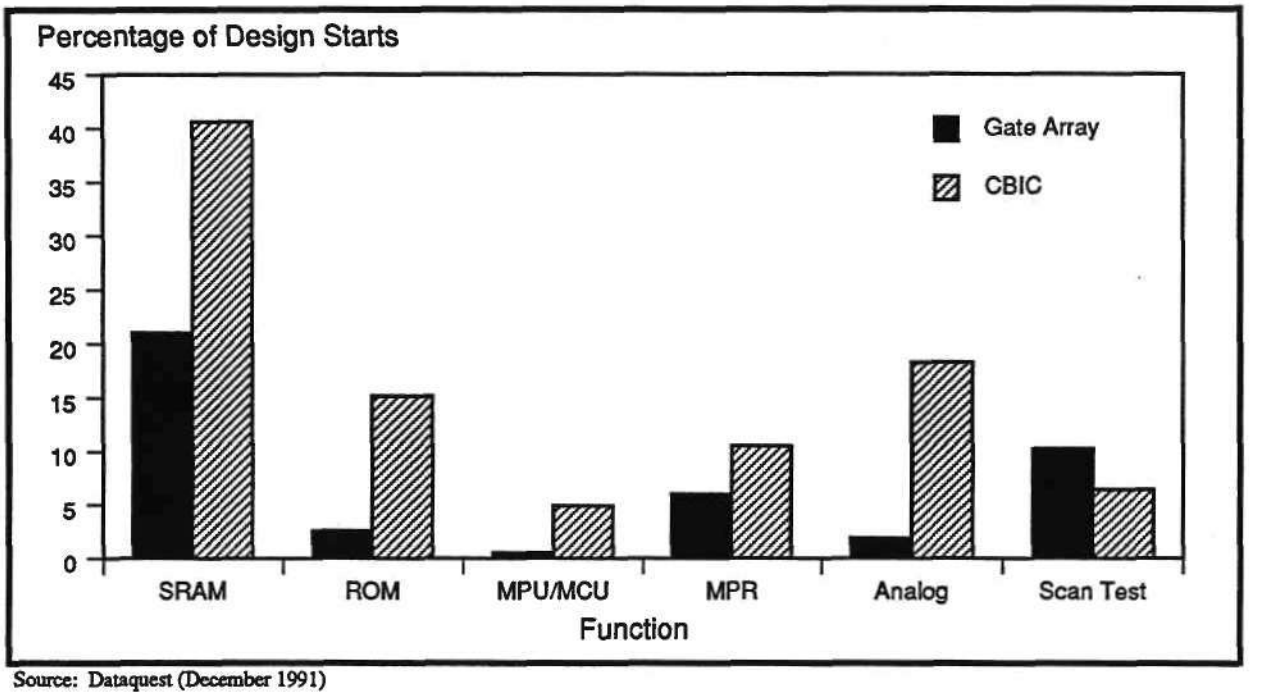
- Although SRAM is the most popular on-chip function in both gate arrays and CBICs, the rate of change in the percentage of designs that had on-chip SRAM is much higher for gate arrays than CBICs. Gate arrays went from 13 percent of the 1989 designs having on-chip SRAM to 21 percent in 1990, while CBIC design starts only grew from 39 percent to 40 percent. SRAMs implemented with CBICs have traditionally been five to seven times more silicon-efficient than metal-configured SRAMs in gate arrays. The dramatic increase of on-chip gate array SRAMs is because of suppliers offering much higher raw gate counts than before (more gates to use for the metal-configured SRAMs) and because of the availability of embedded gate arrays that have large SRAM blocks. Gate arrays with diffused SRAM blocks are just as silicon-efficient as implementing SRAMs in CBICs and are now emerging in applications that are SRAM-intensive.
- Because CBICs have traditionally been more silicon-efficient for implementing SRAM, not only were there more 1990 CBIC designs with on-chip SRAM, CBIC designs also had larger memories (see Figure 7).
- ROM is more cost-effective in a CBIC than is a traditional gate array; therefore, 15 percent of the 1990 CBIC designs had on-chip ROM compared to only 3 percent of the 1990 gate array designs.
- Despite the myriad of announcements of on-chip microprocessing units/microcontroller units (MPUs/MCUs), less than 1 percent of the gate array designs and less than 5 percent of the CBIC designs had on-chip MPUs/MCUs in 1990. As the numbers indicate, there has been slow user acceptance of on-chip ASIC microprocessors because of their high design cost, high device cost, and difficult testing issues.
- Most on-chip microperipherals (MPRs) in gate array and CBICs during 1990 were 82XX peripherals.
- Analog functions are difficult to implement with transistors within gate arrays. Therefore, in 1990, about 95 percent of the gate array designs that had analog functions were pure analog arrays (no digital) and only 5 percent

Figure 5
1990 Estimated North American MOS ASIC Design Starts, by Gate Count



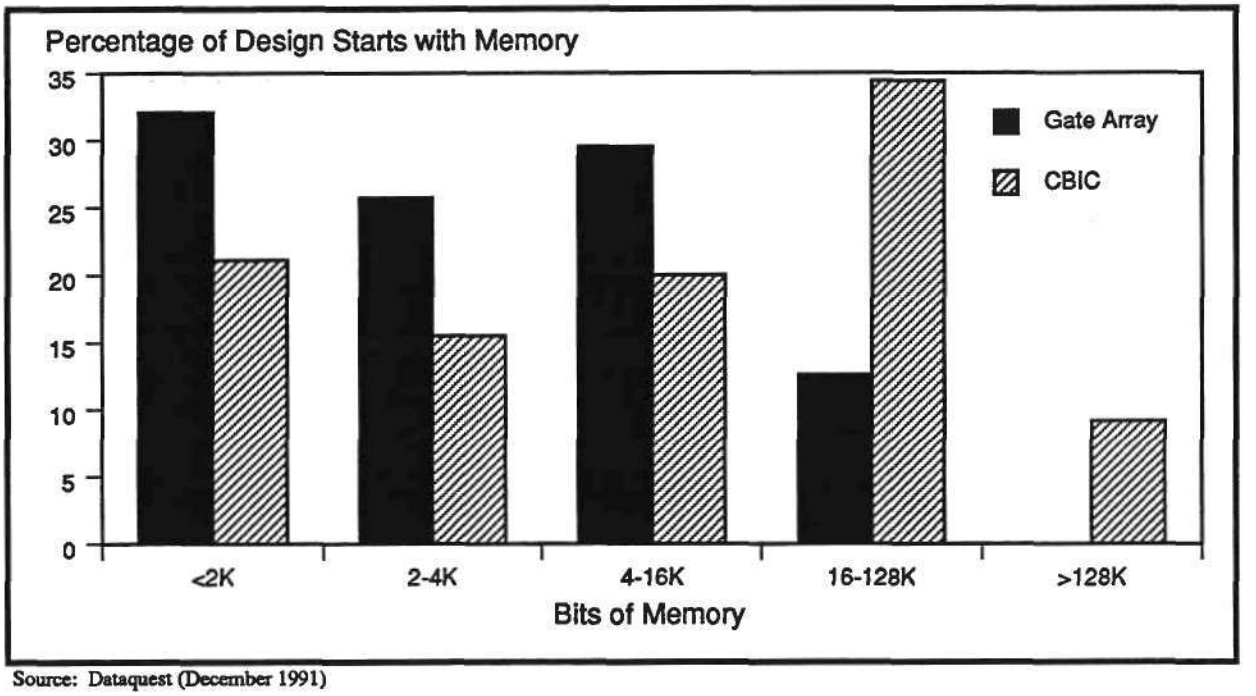
Source: Dataquest (December 1991)

Figure 6
1990 Estimated North American MOS ASIC Design Starts, by Function



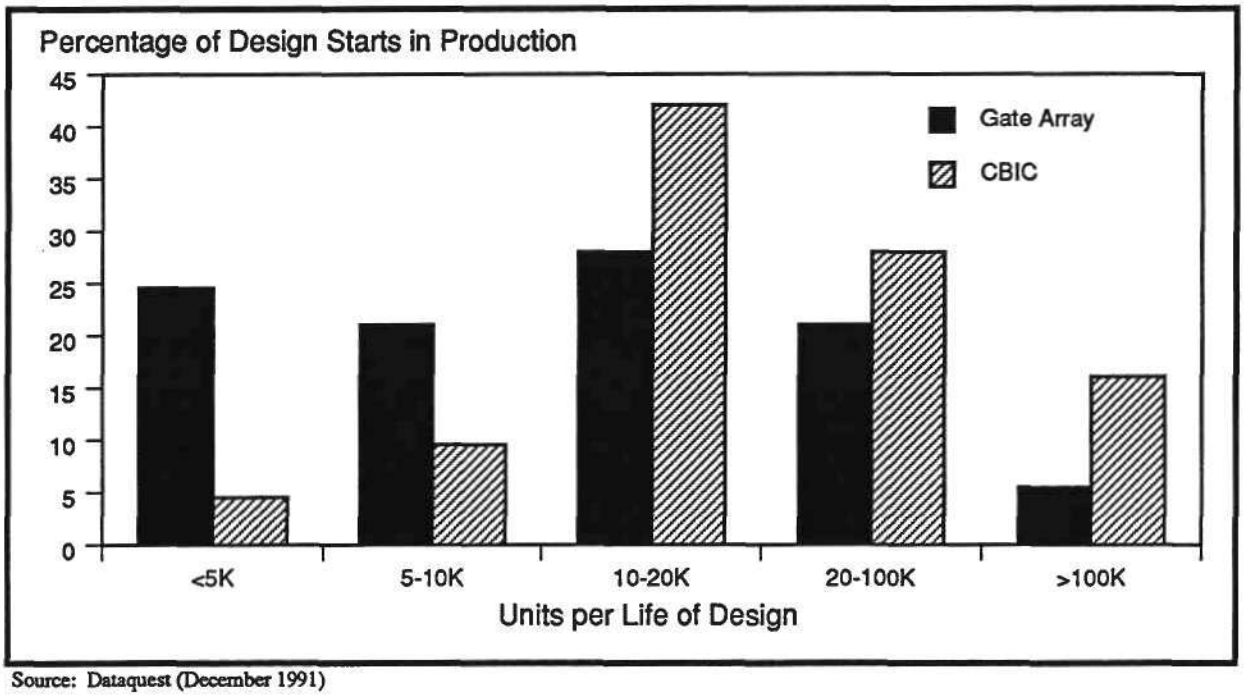
Source: Dataquest (December 1991)

Figure 7
1990 Estimated North American MOS ASIC Design Starts, by Memory Bits



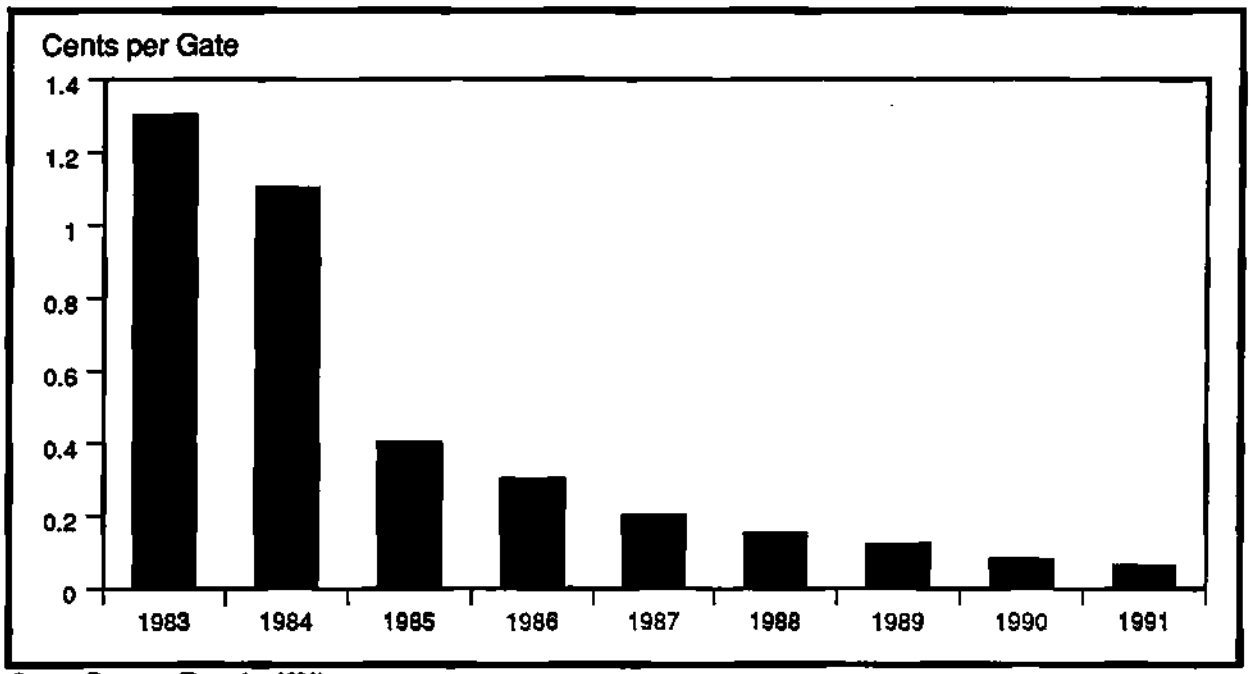
Source: Dataquest (December 1991)

Figure 8
1990 Estimated North American MOS ASIC Design Starts, by Unit Volume



Source: Dataquest (December 1991)

Figure 9
Estimated North American CMOS Gate Array Pricing (3,000 Gates, 15,000-Unit Volume)



Source: Dataquest (December 1991)

were mixed analog/digital arrays. On the other hand, CBICs are well suited to optimize the analog functions and mix them with digital functions. Therefore, about 95 percent of CBIC designs were mixed analog/digital designs and only 5 percent were pure analog CBICs. Common analog functions being implemented in ASICs include: comparators, amplifiers, voltage regulators, interface drivers, data converters, and phase-locked loops.

- As gate densities continue to rise at a rapid rate, on-chip testing has become critical for both gate arrays and CBICs. JTAG compatibility is emerging as the industry standard for board-level testing. Our analysis also shows a higher use of built-in self test (BIST) in CBICs than gate arrays for memory testing.

Units and Pricing Trends

Figure 8 shows estimated North American ASIC unit volume for the life of designs in production during 1990. We note the following trends:

- The most common 1990 unit volume for gate arrays and CBICs ranged from 10,000 to 20,000 units.
- Gate arrays have been more cost-effective than CBICs in low volumes (below 10,000 units) because of their lower design cost.
- Military users prefer gate arrays over CBICs because they purchase in low volumes. Therefore, we believe that military designs accounted for a large portion of the gate array designs below 5,000 units.
- CBICs have traditionally been more cost-effective than gate arrays in high volumes (greater than 100,000 units) because they have a smaller die size.

Although CBICs cost less to manufacture than do gate arrays (given the same set of functions because the die is smaller), CBICs will not necessarily cost less than gate arrays to the user in high volume. Gate arrays experienced rapid price erosion because of oversupply during the last seven years. Figure 9 shows the severe price erosion on a low-gate count CMOS gate array in North America. CBIC prices have also declined but at a much slower rate than gate arrays because of the reduced number of suppliers. Therefore, in high volumes, gate arrays are often less expensive to the user than are CBICs because there is always one or two gate array suppliers willing to slash the gate array price below that of the CBIC suppliers.

Dataquest Perspective

The dividing line between gate array applications and CBIC applications is in a state of flux. CBICs have historically been used in high-volume applications as well as in applications

Table 1
ASIC Feature Trade-Off Matrix

Feature	Traditional Gate Array	Embedded Gate Array	CBIC
Memory Efficeiency	Low	High	High
Die Size	Large	Medium	Small
Device Cost	Highest	Low	Lowest
NRE Cost	Low	High	High
Retooling Cost	Low	Low	High
Retooling Time	Short	Short	Long
Performance	Medium	Medium-High	High
Risk	Lowest	Low	Highest

Source: Dataquest (December 1991)

that need increased functionality such as large SRAM blocks. Compared with CBICs, gate arrays offer quicker time to market, lower risk, and lower design cost. Embedded gate arrays have now emerged as a crossbreed and are a viable option to CBICs and traditional gate arrays.

Embedded gate arrays and CBICs are the most efficient technologies for implementing memory and other large functional blocks. Embedded gate arrays still retain a portion of the chip area available for random logic gates, so die size and device cost will not be quite as good as with CBICs but will be far better than with traditional gate arrays. Although the first embedded gate array design cost or nonrecurring engineering charge is the same as for CBIC, big savings occur when the design is retooled. Most high-density gate array designs are retooled two to three times because they do not meet system requirements. With embedded gate arrays, only the random logic will need to be reconfigured with the final layers of interconnect; therefore, retooling turnaround time and cost are far less than for CBICs. With reduced turnaround time and cost comes embedded gate arrays' reduced risk (see Table 1).

Although embedded gate arrays only accounted for 1 percent of the 1990 North American gate array designs, demand is strong for such a product. As mentioned earlier, embedded gate arrays are efficient and satisfy the strong need for on-chip SRAM. Dataquest believes that larger SRAMs (128K and 256K) will be diffused in gate array base wafers and used for cache memory. Furthermore, we believe that other functions such as SCSI, arithmetic logic units, multiplier-accumulators, first in/first out memories, direct memory access controllers, cache controllers, and 82XX microperipherals will also be diffused in the gate array, fueling the growth of the embedded gate array market.

In conclusion, Dataquest believes that gate arrays (including traditional gate arrays and embedded gate arrays) will continue to remain the dominant technology throughout the decade. Furthermore, we believe that embedded gate arrays will wrestle market share from the CBIC market because they will increasingly be capable of matching the functionality and performance of CBICs, with reduced cost and risk. However, Dataquest does not believe that embedded gate arrays will replace traditional gate arrays or CBICs in the foreseeable future. Each product brings value to the market. Hence, we believe that each product will coexist and system designers will select the products that best suit their unique applications.

By Bryan Lewis

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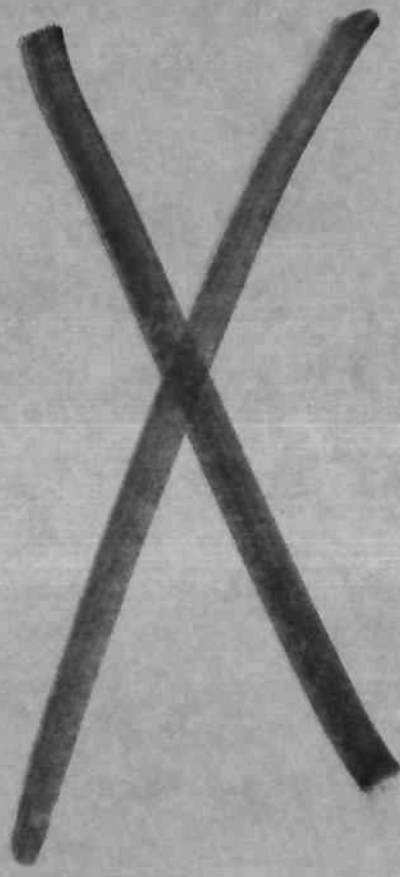

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Research *Bulletin*

HDI FOR GaAs AND OTHER IC MODULES

A new hybrid microcircuit high-density interconnection (HDI) technique dramatically reduces IC subsystem size and boosts performance. HDI has been applied to GaAs RAM modules and at least 20 other applications. This bulletin describes the development of the methodology by General Electric Company (GE), some of its applications, and implications for the GaAs IC industry.

WHAT IS HDI?

As its name implies, HDI accomplishes high-density IC interconnections on a dielectric material using laminates, sputtered metal, and laser drilling. A typical HDI process flow starts with a ceramic substrate, which is selectively milled to accommodate IC chips of various thicknesses and layouts. Aluminum pads are then deposited, and chips are bonded to the pads. Kapton laminate is overlayed; via holes are laser-drilled. Metallization is achieved by sputtering a thin film of titanium and copper. Next, photoresist is applied, laser-exposed, and etched to form conductors that range from 1-1/2 to 3-1/2 thousandths of an inch wide. Application of a dielectric layer allows repeating laser-drilled via holes, metallization, photoresist, etch, and dielectric steps in this order to achieve multilayer interconnections. After the last dielectric layer, passivation is applied and provision is made for external connections. The module is then packaged and tested. Repairability has been demonstrated by removing and replacing chips and HDI layers numerous times on the same substrate.

HDI was developed at GE's corporate R&D center in Schenectady, New York, with funding by GE, the Defense Area Research Project Agency (DARPA), the United States Air Force, and the United States Office of Naval Research. GE has licensed HDI to Texas Instruments Inc. (TI), and TI expects to be on the Pentagon's qualified manufacturer's list (QML) with its HDI facility by mid-1992. TI will produce HDI modules for DARPA's evaluation by fourth quarter 1992, in a company-funded facility supplemented by a $9 million DARPA contract. TI expects to offer what it describes as turnkey service to both government and industry customers, requiring only that a customer supply a circuit schematic, parts list, and required module dimensions.

HDI APPLICATIONS

HDI is ideally suited to many GaAs IC applications, because GaAs is often applied to achieve more power-efficient, higher-performance circuit operation than is possible with silicon. The precision layers of HDI allow construction of transmission lines with carefully controlled characteristic impedance, essential to subnanosecond microwave and millimeter-wave operation of GaAs ICs. However, HDI also provides higher-density packaging of silicon chips than is possible with most other hybrid approaches, so it will find application in all-silicon IC systems as well. The variable chip height provision enables mixing active and passive, GaAs and silicon, analog and digital, electronic and photonic ICs on a single substrate. Because pads interior to a chip can be used for interconnection, overall chip sizes may be made smaller. The use of topside metal for connections eliminates "flip-chipping," enhancing repairability. The laser steps eliminate mask layers, which reduces turnaround time from weeks to days.

GE has demonstrated the HDI technology with a module containing nine GaAs SRAM ICs and having a module access rate above 100 MHz.

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Use of HDI in a signal processor allowed a 30-fold reduction in module size. Another application achieved interconnection of 36 ICs, which operate at 90 MHz or about 50 percent improvement in speed, in an area less than two inches on a side. GE has fabricated a static RAM module containing 20 silicon ICs, which has a substrate area of only 11 percent greater than the silicon chip area. In many applications, the chips may be spaced only 0.01 inches apart.

DATAQUEST CONCLUSIONS

As already demonstrated, continued application of HDI technology will eliminate the need for printed circuit boards in many hardware designs. Dataquest perceives HDI as a technology whose time has come and expects rapid acceptance in the high-performance segments of the electronic equipment marketplace.

Gene Miles

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Research *Bulletin*

MIMIC PHASE II CONTRACTORS SELECTED

Three teams of companies have been selected by DARPA, and awards totaling approximately $228 million have been made by three United States military services for Phase II of the MIMIC hardware program. The awards are summarized in Table 1.

The MIMIC program is a DARPA initiative aimed toward the economic insertion of microwave and millimeter-wave (3GHz to >100GHz) GaAs ICs into military systems. Phase II objectives include addressing the needs of the military services by continuing the technology and product developments started in Phase I, further demonstrating affordability, pursuing new technology approaches, and demonstrating system use and foundry support of MIMICs. Phase III activities, conducted in parallel with Phases I and II, address additional special issues. System applications for MIMIC program technology include military communications, radar, electronic warfare, smart munitions, smart fuzes, and missiles. The advanced technology fighter (ATF) and many other military platforms and systems will benefit from MIMIC technology insertion.

Gene Miles

TABLE 1
MIMIC Phase II Awards

Prime Contractor	Team Members	Service	Award Amount ($M)
Hughes Radar Systems Group	Alliant, AT&T, Cascade Microtech, EEsof, General Electric, Litton, M/A-COM, Rockwell	U.S. Air Force	78.9
Raytheon/Texas Instruments	Aerojet, Airtron, Cadence, Consilium, General Dynamics Hewlett-Packard, Hittite, Lockheed-Sanders, Teledyne	U.S. Navy	83.4
TRW Electronic Systems Group	Alliant, Avantek (acquired by Hewlett-Packard), COMSAT, EEsof, General Dynamics, Hercules, Mentor Graphics, Texas Instruments, Westinghouse	U.S. Army	65.7

Source: Dataquest (September 1991)

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Research *Bulletin*

III-V SEMICONDUCTOR ICs MAY BOOST MACHINE VISION

A recent study shows that approximately half of a human's brain cells are associated with visual activity. Computers, particularly PCs in ever-growing numbers, are increasingly used to relieve people of complex, highly repetitive mental tasks. To date, computers have not been applied very well to replacing human visual routines. The necessary speeds of the algorithms required for all but the most rudimentary real-time machine vision are above those speeds attainable using state-of-the-art silicon ICs. However, GaAs ICs have achieved system-operating speeds above 30 giga operations per second (GOPS) and complexities of 1 million transistors per chip, and ZnSe/GaAs chips are capable of extending OEIC operation into the blue area of the visible spectrum. Furthermore, production-worthy InP chips routinely operate in the millimeter-wave range. Thus, machine vision represents a huge potential for growth in applicable III-V ICs.

WHAT IS BEING DONE THAT III-V ICs COULD DO BETTER?

Two examples show the potential for GaAs and other III-V compound ICs in the field of machine vision: scanners used as OCR input devices for PCs and video cameras.

Scanners for PCs

PC-compatible hand-held scanners, supported with crude recognition software, are capable of scanning and recognizing the majority of characters in a column of newsprint. Such scanner subsystems have been on the market for less than $200 since early 1991. Color page scanners also are available for desktop PCs, priced below $1,100 each (single quantity). However, the recognition time and overall character recognition rate on a document basis appear to be unacceptable for anything other than limited academic use. The primary limitations are use of relatively slow silicon ICs for recognition (hardware) and crude learning algorithms (hardware and software). Although some speedup will be achieved with software improvements, the hardware problems must also be solved before a viable solution is attained.

Many PC owners' near-term needs will not be satisfied until page scanning at a level supportable by an automatic spelling-checker becomes a routine method of data entry, priced in the $200 to $300 range. The need exists for a self-contained, easily trainable, scanner-recognition package that can read, recognize, and enter mixed-font characters several times faster than an expert human typist. GaAs linear CCD and parallel DSP chips based on currently available processes could be developed to perform these functions. The unit demand probably exceeds 60 percent of all PCs in use today, representing a GaAs IC market niche of several hundred million dollars. As occurred with the desktop PC, once a several-chip solution is accomplished, cloners will ensure that affordable pricing follows.

Video Minicams

A miniature video camera (minicam) uses a silicon CCD front end to convert photonic data to electronic data. The electronic signals are processed through silicon ICs, either to drive recording electronics that store images on magnetic film, or to be amplified and transmitted for broadcast, or both. In low-level light, rapidly changing light, fast panning, and other normal visual conditions, the use of silicon results in streaking, blooming, and several other undesirable effects. Battery duration between recharges is also a major performance factor in

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some law enforcement and other applications. GaAs ICs for the CCD "retina," A/D conversion, signal processing, and data transmission chips would greatly enhance sensitivity and speed, allowing at least an order of magnitude improvement in image quality over that of present minicams while simultaneously extending battery time between charges.

DOES MAJOR POTENTIAL EXIST FOR SYSTEMS INNOVATION?

The future for systems innovation appears bright for entrepreneurs and enterprises alike. To avoid compromising sensitive development activity already under way, the following hypothetical example serves as an available technology within two years.

Little imagination is required to combine a high-performance minicam function such as that of the Magnavox CVM710 with a cellular radio, a small color display, or both, to build a highly portable, receive-only or transceiver videophone capability. GaAs IC technology has already been applied individually to high-volume-production cellular phones, video displays, and VCRs for subsystem cost and power reductions.

Applications for such a device occur in every facet of life where there is a need to enhance personal communication. Examples include law enforcement, news reporting, and emergency services. A volume production cost well below $600 per unit is achievable with available IC and other hardware technology.

Although bandwidth requirements coupled with frequency allocation constraints prevent real-time application of portable color video transceivers to mass usage, a lower-cost black-and-white version and a still-picture color version could become consumer products before the mid-1990s. (Note that ultralightweight, 6-inch black-and-white video receivers can now be produced at a volume cost below $12.) And, bandwidth limitations could be relieved by allocation of higher communications frequencies, allowing application of InP IC technology to the transceiver.

Dataquest believes that the first company to produce such equipment for professional use is likely to enjoy initial unit pricing in the several thousand dollar range because of the value perceived by the initial user markets. This is but one example of the rapidly growing potential for increasingly pervasive GaAs technology.

Gene Miles

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Research Newsletter

GaAs INDUSTRY SURVEY REVEALS OPPORTUNITIES

A Dataquest survey of the GaAs IC industry infrastructure, performed during June and July 1991, shows a range of opportunities for participants in this growing marketplace. A record 48 percent of the sample contacted responded in depth to the question set rather than the expected 20 to 30 percent for this type of survey. This newsletter reports significant results and summarizes key findings of the analysis to date.

ISSUES CONSIDERED

Many of Dataquest's clients and potential clients have indicated high interest in acquiring more information about the following:

- The extent of GaAs penetration of the high-performance end of the silicon IC market and whether this penetration will continue
- Potential for growth in usage of existing GaAs IC chip types
- Plans for future usage of GaAs ICs, including potential demand for GaAs charge-coupled devices (CCDs)
- Changes in competitive positions of industry participants, including potential impact of the recent merger of TriQuint, GigaBit Logic, and Gazelle
- Future needs for additional GaAs IC chip types, engineering software, test equipment, and related product functions and parameter improvements
- Recommendations for additional improvements in products and services offered by the GaAs industry

The question set used in this survey was designed to elicit response in sufficient depth to address these issues and allow collection of additional detail about the perceptions of the industry participants regarding industry shortcomings, competition, and several other relevant factors.

SURVEY POPULATION, SAMPLE SET, AND METHODOLOGY

For purposes of this newsletter, the following terminology is used to distinguish major subsets of the population:

- Group B denotes members of the "bottom" of the food chain, supplying raw or epi wafers, chemicals, processing equipment, CAD/CAM/CAE hardware and/or software, and related goods and services to GaAs IC suppliers.
- Group M denotes the GaAs IC suppliers ("middle" of the food chain).
- Group T denotes actual or potential users of GaAs ICs that build equipment for sale or system integration, not including those company divisions surveyed as suppliers of equipment for GaAs IC processing, production, and/or test.

Dataquest chose the following sample from the industry population, comprising primarily companies that have offices in North America, regardless of country of origin. Thus, virtually all of the Europe- and Asia/Pacific-based companies participating in the GaAs IC industry infrastructure were surveyed. They include:

- 8 GaAs wafer suppliers (a group B subset)
- 15 other GaAs materials producers (a group B subset)
- 18 GaAs IC processing/production/test equipment manufacturers (a group B subset)

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- 5 GaAs IC development software suppliers (a group B subset)
- 31 GaAs IC suppliers (group M)
- 28 actual/potential GaAs IC users: computer/EDP/workstation manufacturers (a group T subset)
- 25 actual/potential GaAs IC users: communication equipment manufacturers (a group T subset)
- 28 actual/potential GaAs IC users: military/aerospace equipment manufacturers (a group T subset)
- 25 actual/potential GaAs IC users: all other electronic equipment manufacturers (a group T subset)

The initial selection for sampling was performed using random numbers to select from several alphabetized lists, except the GaAs IC supplier list, which consisted of all the GaAs IC merchant market suppliers known to Dataquest (excluding distributors and stocking representatives). Selected names within the companies were then contacted by Dataquest's Survey Group to verify qualifications as potential respondents. The incentive offered to potential respondents was a copy of this newsletter summarizing survey results. The Survey Group used telephone interviews to collect the data, which were entered into a Dataquest computer database for summarization.

SURVEY RESULTS

A total of 87 respondents participated from a sample of 182 potential candidates. Breakdowns of the sample and respondent data are presented in Table 1. The wafer suppliers, software suppliers, and GaAs IC producers indicated the highest interest levels (80 to 100 percent) in cooperating in this survey effort, as the table illustrates. GaAs IC users and potential users showed a much lower interest level, varying by subgroup from 20 to 48 percent.

Table 2 describes industry material/equipment/software, GaAs IC supplier, and GaAs IC user companies' perceptions of relative competitor positioning among the GaAs IC suppliers. Interestingly, 75 percent of GaAs IC suppliers and 50 percent of GaAs IC users perceive TriQuint as the top-ranked GaAs IC competitor compared with 35 percent of those that supply major goods and services to GaAs IC houses.

CURRENT AND FUTURE GaAs IC PRODUCT NEEDS

Eighty-eight percent of the respondents identified which types or functions of the GaAs ICs now produced by the suppliers are considered most important. Of these, 27 percent identified digital functions as most important, with 7 percent specifically naming gate arrays. Ten percent stated that amplifiers were most important.

TABLE 1
GaAs Survey Respondent Group

Group/Subset	Sampled	Respondents	Percent of Sample Subset	Percent of Responent Group	Percent of Total Respondents
B/Wafer Suppliers	8	8	100	28	9
B/Other Materials Suppliers	15	10	67	34	11
B/Equipment Suppliers	18	7	39	24	8
B/Software Suppliers	5	4	80	14	5
M/GaAs IC Producers	31	28	90	100	32
T/Computer/EDP/Workstations	28	6	21	20	7
T/Communication Equipment	25	5	20	17	6
T/Mil/Aero	28	7	25	23	8
T/Other Users	25	12	48	40	14

Source: Dataquest (August 1991)

TABLE 2
Perceived Ranking of "1, 2, and 3" GaAs IC Suppliers

GaAs IC Company (Number/Percent)	Ranked as #1 by Respondents (Number/Percent)	Ranked as #2 by Respondents (Number/Percent)	Ranked as #3 by Respondents (Number/Percent)
TriQuint	54/60	16/18	4/4
Vitesse	13/15	27/31	2/2
Anadigics	2/2	2/2	6/7
Texas Instruments	3/3	4/4	2/2
Avantek	2/2	1/1	0/0
Harris Microwave	0/0	2/2	2/2
Pacific Monolithics	0/0	2/2	1/1
Fujitsu	0/0	2/2	1/1
M/A-COM	0/0	0/0	5/5

Source: Dataquest (August 1991)

When questioned about future GaAs IC needs and industry opportunities, 92 percent of the respondents described specific application opportunities, and 65 percent of the participants identified specific types or characteristics of circuits they require. Eleven percent of the respondents want more and better communication circuits, some describing chips for fiber-optic applications. Personal communications and cellular communications were most frequently mentioned (39 percent) as the greatest opportunity for the GaAs IC industry during the next five years, followed by computer applications (26 percent).

Respondents among the sample of 106 companies that are GaAs IC users or potential users (group T) were asked if they currently use GaAs ICs. Thirty percent of respondents said they are using GaAs ICs in designs that are currently under way, and 20 percent are using GaAs ICs in production. Thirteen percent of group T respondents refused to answer these questions.

When asked about the percentage mix of GaAs and silicon ICs used by themselves and by the industry, respondents indicated a mean usage of 5.7 percent GaAs ICs for themselves and 6.8 percent for the overall industry in 1990, forecast to grow to 15 and 14 percent, respectively, by 1995 and remaining at about the same percentages through 1999. Twenty-seven percent of group T respondents stated that they now use GaAs optoelectronic ICs. Of those not now using OEICs, less than half stated that they will not be using OEICs in 1993 and only 20 percent of group T respondents foresee no needs for OEICs through the next decade. The respondents indicated virtually no interest in GaAs CCDs.

Regarding the GigaBit and Gazelle mergers with TriQuint, 81 percent of respondents expect no impact on their company activities and half of the remainder expect a positive impact.

FOR FURTHER INFORMATION

Dataquest clients may use the normal inquiry procedure to obtain further information resulting from this survey. Non-Dataquest clients may contact the nearest Dataquest office for additional assistance.

DATAQUEST CONCLUSIONS

Overall growth in the GaAs IC industry is assured for several years to come, as the participants respond to user demands for a greater variety of GaAs ICs in a broadening range of applications. However, some participants will not benefit from this increasing demand unless their images change significantly from what is currently perceived by their potential client base. This still-young industry faces heavy competition in the years ahead because of the desire of all participants to maintain rapid growth, decreasing military budgets, consolidation in the computer and communications industries, and other factors.

Gene Miles

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Research *Bulletin*

CONVEX C3800 SUPERCOMPUTERS USE 45,000-GATE GaAs ASICs

CONVEX Computer Corporation has announced its 3C Series of supercomputers, which includes the industry's first all-GaAs IC supercomputer family. This announcement further confirms the general industry acceptance of GaAs ICs for high-performance electronic data processing (EDP) applications, already in use at Cray Computer Corporation and several Japanese computer houses. Classed as "enterprise"-level machines, the air-cooled C3800 Series features implementation of one to eight CPUs using 45,000-gate GaAs ASICs, up to 4GB of physical memory, and 2 gflops (billions of floating point operations per second) peak performance. CONVEX plans to beta-site the C3800 in the third quarter of 1991. Additional C3800 shipments are scheduled for the fourth quarter of 1991.

Vitesse Semiconductor Corporation is believed to be the major supplier of 45,000-gate GaAs ASICs to CONVEX, although Fujitsu and other suppliers are capable of producing the chips. In 1990, Vitesse announced GaAs ASICs with gate densities to 350,000 gates and transistor counts of up to 1 million per chip. In February 1991, Fujitsu announced GaAs HEMT-based ICs with a density of 45,000 gates, as well as GaAs HEMT 64K SRAMs. Vitesse has alternate-sourcing agreements on its FURY series of GaAs ASICs with both Fujitsu and Thomson. CONVEX and Vitesse share two board members, Pierre Lamond and Robert Paluck.

The CONVEX C3 Series also comprises the C3400 family of 150,000-gate BiCMOS ASIC-based "departmental" supercomputers and the C3200 family of ECL and CMOS IC-based "server" machines. Maximum physical memory for either of the families is 2GB. Peak performances are 0.8 gflops and 0.2 gflops, respectively. Announced price ranges are $2 million to $8 million for the C3800s, $650,000 to $2 million for the C3400s, and starting at $350,000 for the C3200s.

CONVEX developed the C3 family to address the demands of supercomputer users for relatively low-cost, air-cooled, interactive open systems supported by a wide range of third-party application software. More than 1,000 UNIX-based software applications are available on the C3 Series. All CONVEX machines are upward and downward binary compatible.

At press time CONVEX, which was founded in 1982 and introduced its first supercomputer in 1985, had sold more than 850 systems to nearly 500 customers in at least 36 countries. The company markets its products primarily to scientific, engineering, and technical users worldwide. The pervasiveness of supercomputers in the worldwide marketplace is well illustrated by a sampling of CONVEX's customer base. CONVEX customers as of December 31, 1990, included the following:

- Government/aerospace—Aerospatiale (France); British Aerospace plc (U.K.); Canadair (Canada); Daimler-Benz (Germany); Joint Electronic Warfare Center, Lockheed, McDonnell Douglas, NASA (Ames, Langley, and Lewis Research Centers), Naval Ocean Systems Center, Naval Research Lab, Naval Surface Warfare Center, Rockwell, Texas Instruments, and TRW (United States)
- Computer-aided engineering—Air Liquide, ESI, GEC ALSTHOM, and Hutcheson (France); AVL List (Germany); DSM Research (The Netherlands); Nissan Motor Co., Sanyo, and Taisei (Japan); Jaguar Cars Ltd. (U.K.); Saab-Scandia (Sweden); AT&T, 3M Company, EDS/General Motors, and Ford Motor Company (United States)
- Computational chemistry—Biomolecular Research Institute (Australia); Pasteur Institute and Roussel UCLAF (France); Bayer AG and Boehringer Ingelheim (Germany); Institute of

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Fundamental Chemistry and Sekisui Chemical Co. (Japan); Cambridge University (U.K.); Agouron Pharmaceuticals, Amgen, Eastman Kodak, Johns Hopkins University, Mount Sinai Medical Center, National Institutes of Health, Scripps Clinic, and Schering-Plough (United States)

- Petroleum—Commonwealth Scientific and Industrial Research Organisation (Australia); Compagnie Generale de Physique, French Petroleum Institute, and Total (France); Telefunken Systemtechnik and Preussag (Germany); Delft Geophysical, Jason Geosystems, and Royal Dutch/Shell Group (The Netherlands); CogniSeis Development, Inc. (U.K.); ITA (Canada); Allied Geophysical Labs, Mobil, PT Caltex Pacific Indonesia, Seismograph Service, and Texaco (United States)
- Advanced research—University of Bielefeld and University of Marburg (Germany); Labein Industrial Research Laboratory (Spain); Exeter University (U.K.); University of Odense (Denmark); University of Utrecht (The Netherlands); NTT and Sony (Japan); GE, Los Alamos National Labs, National Center for Supercomputing Applications, and these universities—Arizona, California, North Carolina, Princeton, and Rice (United States)
- Environmental—Alfred Wegener Institute, DKRZ, IFU, and Polarstern research vessel (Germany); Catania Observatory and Institute of Radio Astronomy (Italy); Natural Environment Research Council (U.K.); Ministry of Health and Environment (Belgium); Royal Netherlands Meterological Institute (The Netherlands); Korean Aerospace Research Institute (Korea); Air Force Geophysics Lab, Naval Oceanographic Research and Development Agency, and Woods Hole Oceanographic Institution (United States)
- Emerging Markets—Center for Scientific Computing (France); Erasmus University and Gasunie (The Netherlands); India Institute of Technology (India); Acer Sertek (Taiwan); NKK, Ricoh, and Schimizu (Japan); Dow Jones & Company, E-Systems, and the following universities—Notre Dame, Texas (three locations), and Wisconsin (United States)

DATAQUEST CONCLUSIONS

The displacement of silicon ECL ICs by GaAs ICs at VLSI density levels is well under way. CONVEX's C3800 products are encroaching on markets once dominated by the silicon current-mode architectures of CDC, Cray, and other companies, further ensuring rapid growth of the GaAs VLSI chip marketplace. Although the C3800 line is priced at $2 million or more, it is substantially below the expected $10 million to $20 million CRAY 3 price tag and reflects the cost efficiencies provided by air-cooled GaAs VLSI ASICs and memories. Dataquest expects a growing number of EDP houses to announce the adoption of GaAs ICs in their hardware designs as they increasingly compete in high-performance niches.

Gene Miles

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Research *Bulletin*

TRIQUINT-GIGABIT MERGER INCLUDES GAZELLE

On May 10, TriQuint Semiconductor Inc. announced a definitive agreement that adds Gazelle Microcircuits to the TriQuint-GigaBit Logic merger. Regulatory and shareholder approval are expected, and transactions are to be completed by May 31. The combined company will have 320 employees, 97,000 square feet of facilities, and annual sales in excess of $40 million per year. Operations are located in Beaverton, Oregon; Newbury Park, California; and Santa Clara, California. TriQuint is the world's largest commercial GaAs IC products company.

TriQuint is experiencing rapid growth in the consumption of GaAs custom and semicustom ICs by the computer, communications, military systems, and instrumentation markets. The company's customer base totals more than 1,200, including many Fortune 500 companies.

Gazelle, founded in 1986, utilized TriQuint as its primary foundry. Gazelle initially focused on TTL-compatible GaAs PLDs and other high-performance circuits based on GaAs technology. The merger provides a vehicle for continuation of the $4 million DARPA development contract booked by Gazelle, amid some controversy, in April 1990. Gazelle's performance in 1990 was lackluster, and 1990 saw the departure of cofounder David MacMillan and other key employees.

The new company will be jointly owned by existing investors in the three merging companies. Corporate investors include Tektronix, Digital Equipment Corporation, Analog Devices, NKT (Denmark), and several venture capital firms. Venture capital investors include Kleiner, Perkins, Caufield and Byers; Hambrecht & Quist; Dillon-Reed-Concord Partners; Merrill, Pickard, Anderson and Eyre; Venrock Associates; InterVen Partners; Canaan Venture; and DFC (New Zealand).

The new seven-person board of directors includes chairman Gary Arnold, vice president and CFO of Tektronix; John Vold, vice president of business development for Tektronix; Richard Hill, vice president of test and measurement operations for Tektronix; Spencer Brown, former president of GigaBit Logic; David B. Jones, general partner with InterVen Partners; Steve Sharp, with Mohr-Davidow; and Floyd Kvamme, partner in Kleiner, Perkins, Caufield and Byers. A three-person management operating committee has been formed, consisting of interim president and CEO A.J. "Bert" Moyers, formerly vice president and CFO of Western Digital and National Semiconductor; executive vice president Al Patz, former president of TriQuint; and executive vice president Spencer Brown.

DATAQUEST CONCLUSIONS

The combined companies bring many strengths to the marketplace, including state-of-the-art innovative designs, automated circuit analysis, fabrication, packaging and test facilities and capabilities, extensive market coverage, remote design centers, and a 10-year history of performance in making new GaAs products a reality. Dataquest expects TriQuint to capitalize on these strengths.

Gene Miles

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Research Newsletter

GaAs ADVANCES INTO THE MILLIMETER-WAVE REGIME

INTRODUCTION

GaAs technology continues to evolve to higher-frequency operation. Recent advances in production processes make possible the fabrication of transistors and ICs suited for operation above 30 GHz. This newsletter examines some of the recent developments and potential applications of millimeter-wave GaAs semiconductors.

WHAT IS THE MILLIMETER-WAVE REGIME?

Because energy radiates at approximately 186,000 miles per second in free space, energy fluctuating at a frequency of more than 30 GHz has a wavelength of less than one centimeter. The wavelength becomes one millimeter at approximately 300 GHz. Hence the name "millimeter-wave" is used to refer to frequencies in the range of 30 to 300 GHz.

For comparison, the "microwave" range of frequencies extends from 3 to 30 GHz, which is about 1,000 times higher than the clock rates of today's personal computers (4.77 to 33 MHz). Although very high, the millimeter-wave frequency range is 10,000 times slower than the visible (human eye response) range of frequencies, which have wavelengths of approximately 400 to 800 angstroms.

IMPORTANCE OF MILLIMETER-WAVE TECHNOLOGY

For many years, the microwave range of frequencies has been used for such applications as radar and radio communications, initially in military equipment and more recently in commercial hardware. As the frequency bands allocated for the various applications have become more crowded, equipment design constraints have increased. The semiconductor industry responded at first by improving silicon technology and later by introducing GaAs substrate material.

As a result of recent advances in GaAs and other compound semiconductor technologies, it is now feasible to produce transistors and SSI- to MSI-density ICs capable of processing millimeter-wave signals. Extending the available frequency range for applications from 30 GHz up to 300 GHz and adding the millimeter-wave bands to the existing bands (which range through the microwave regime) increases available bandwidth by a factor of nine. This element is critical in enabling future portable personal communications, which will be required to operate in an environment containing many times today's channel traffic.

Another important aspect of millimeter-wave technology is physical in nature. The earth's atmosphere attenuates energy propagation at most frequencies above 3 GHz and into the lower infrared spectrum (10 THz) by at least 0.1dB per kilometer; this increases to as much as 100 to 1,000dB per kilometer at certain frequencies. This property enables highly localized transmission and reception of signals for such applications as collision-avoidance radar, which Detroit sources prefer to refer to as "proximity detection" for fear of legal consequences of implying that collision avoidance is a problem with today's vehicles. Because this attenuation is characteristic of the oxygen, water vapor, and other gases in the earth's atmosphere, space communications at millimeter-wave frequencies are much more efficient. The attenuation characteristics also allow local earthbound communications to occur with less interference with each other and with other equipment, and they enable certain forms of secure communications.

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MILLIMETER-WAVE SEMICONDUCTOR DEVELOPMENTS

GaAs and InP are compound semiconductor substrate materials that allow electrons to be switched much more efficiently than silicon, hence enabling higher-frequency operation at a given minimum device feature size. Scaling semiconductors to smaller feature sizes increases potential operating frequency until materials limitations or geometric tolerances become excessive. Table 1 describes recent device developments by four companies, all indicating millimeter-wave range operating capability. All of the devices in Table 1 use AlGaAs layers in their construction.

The U.S. DOD MIMIC Program includes provision for development of millimeter-wave ICs for defense applications. Other companies working in this regime include TRW and Alpha Industries. TRW has developed GaAs power transistors capable of 94-GHz operation. Several European and Japanese companies, including Thomson, Siemens, Fujitsu, NEC, and Plessey, are developing millimeter-wave ICs for government and commercial applications.

MILLIMETER-WAVE IC APPLICATIONS

In addition to space communications, radar, and military applications, potentially large volumes of mm-wave ICs will be required to support vehicular traffic control and collision avoidance systems. In Germany, the AEG Verkehrs Erfassungs (AVES) system, operating at 61.5 GHz, has been tested under actual traffic conditions. This system uses radar transmitter and sensor units mounted on signboard bridges above the roadway, coupled with hardware algorithms, to determine vehicle speeds, lengths, and spacings. The German Bundesanstalt has approved the system, and a production order for 1,000 units is in process. Similar systems are in use in Tennessee and other U.S. states, as well as in Japan.

DATAQUEST CONCLUSIONS

The potential commercial applications for millimeter-wave ICs are growing in number. Microwave semiconductor applications originated in the military and aerospace sectors and migrated to the commercial arena, and millimeter-wave chips are expected to experience similar evolution. In addition to the radar, automotive, and communications markets already described, Dataquest expects many niche markets to develop in the early to mid-1990s for mm-wave GaAs and InP transistors and ICs. Only a small number of IC houses are now adequately positioned to take advantage of the emerging opportunities in this field of applications. A major obstacle today is the relative lack of microwave/mm-wave engineering talent at the IC houses influencing the selection and development of new IC products.

Gene Miles

TABLE 1
Some Recently Developed Millimeter-Wave Low-Noise Transistors

Company	Substrate Material	Gate Size (Microns)	F_{min} (GHz)	Noise Constant (K/GHz)	Achievable NF at: 44 GHz (dB)	60 GHz (dB)	94 GHz (dB)
Linear Monolithics	GaAs	0.1x100	113	2.4	2.0	2.9	6.4
GE	GaAs	0.08x50	270	2.7	2.0	2.6	3.9
COMSAT Labs	GaAs	0.35x60	107	7.1	4.1	5.6	11.4
GE	InP	0.25	380	1.9	1.6	2.1	3.1
Hughes	InP	0.2x50	175	0.9	1.0	1.4	2.4

Source: Martin Marietta

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Research Newsletter

THE IMPENDING BATTLE OF THE GaAs HETEROSTRUCTURES

INTRODUCTION

GaAs technology is maturing; E/D MESFET gate arrays are available in volume from three suppliers at densities of 30,000 gates per chip. The next generation of logic families is now being chosen by various industry participants. The decision to use some form of heterojunction transistors for gate and latch structures already has been made. The remaining decisions, regarding circuit form, are much more difficult because they involve relative volumes of emerging applications. Each major player has a unique perspective of end uses and must avoid tunnel vision. To assist our client base, this newsletter examines the heterostructure issue.

THE CONTENDERS

The participants in the heterostructure war of the early 1990s are the vertically integrated electronic systems houses and their compound semiconductor materials and equipment supplier base. These companies will determine their future viability in many end-equipment markets by their choice of technology for multi-GHz digital hardware. Affected applications include almost every electronics market segment from spaceborne systems and electronic warfare to microwave-frequency personal communications and future notebook computers.

THE ISSUES

The primary points of contention are similar to those in most of the silicon logic wars of the past. They include the following:

- Gate delay—translating to logic speed
- Power/gate—setting the level of integration and driving packaging cost
- Process complexity (manufacturability)—limiting chip (and therefore, system) cost
- Market viability—the ultimate determinant of practicality

THE APPROACHES

Currently, three basic transistor structures are contending for leadership as technologists strive to develop the successor to E/D MESFET technology for high-performance applications. They are high electron-mobility transistors (HEMTs), complementary heterostructure transistors (C-HFETs), and heterojunction bipolar transistors (HBTs). Each offers advantages for specific applications, as summarized later.

HEMTs

Dr. Raymond Dingle and others at Bell Laboratories invented selectively doped heterostructure transistors (SDHT, later labeled HEMT by Bell's competitors) and reported structures using this approach in 1978. The 64K SRAM (1.2ns access time) and 45K gate array devices announced by Fujitsu on February 12, 1991, are representative of the current state of the art of HEMT. Fujitsu is obviously "doing its homework" in preparation for bringing its $200 million GaAs fab facility on-line next year. Table 1 describes major details of the Fujitsu devices.

C-HFETs

Notable work has resulted from IBM's efforts in C-HFET logic structures. Others (notably Honeywell) are pursuing this approach because of its inherent similarities to silicon CMOS, which include lowest attainable logic power for complex

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functions and because of its radiation hardness. Sources at Boeing and other companies believe that C-HFET is the logical alternative to E/D MESFET logic, just as silicon CMOS displaced NMOS.

HBTs

Theoretical work on HBTs traces to 1957, and GaAs HBTs were functional by 1972. However, until recently, HBT ICs were limited to low-LSI-density functions fabricated on an R&D basis (measured by silicon standards). In mid-1990, AT&T reported a carbon-doped process sustainable in economic high-volume production. A joint effort of IBM and Rockwell accomplished the integration of 5,090 transistors on a 1,100-gate equivalent logic array, reported in 1990. An October 1987 paper describes a TI/CDC GaAs RISC microprocessor chip containing 13,000 HBT transistors interconnected to perform I^2L logic.

The DARPA MIMIC program includes sponsorship of development of millimeter-wave (mW) (>30 GHz) ICs, and at least one MIMIC contractor has produced 25,000 HBT ICs with excellent yields. Companies such as AT&T, Hughes, Pacific Monolithics, Rockwell, TI, and TRW now have considerable expertise in HBT IC design and fabrication.

THE TRADE-OFFS

Table 2 summarizes major advantages of the three types of GaAs heterostructure ICs and indicates approximate levels of speed, power, and

TABLE 1
Fujitsu HBT ICs Described at 1991 ISSCC

Feature	SRAM	Gate Array	Notes
Complexity	8,192 x 8 bits	45,600 gates	
Power	5.9 watts	11 watts	GA power at 80% gate usage
Supply Voltages	-1.0,-2.0,-3.6V	-1.4,-2.0V	
Speed	1.2ns typical	35ps (DCFL) 50ps (BDCFL)	Gate array delays do not include interconnect C
I/Os	ECL-compatible	ECL-compatible	
Die Size	7.4mm x 6.5mm	9.8mm x 9.8mm	Produced on 3-inch wafers
Cell Size	17.5u x 13.5u	30 x 66	
Transistors	E/D HEMT	E/D HEMT	38 GHz cutoff frequency
Gate Length	0.6u	0.6u	AlGaAs/GaAs dry-etched
Metal Pitch	2.4u	3.0u	
Linewidth	1.2u	1.2u	L1 = Al; L2 = Ti/Pt/Au

Source: Fujitsu Ltd.

TABLE 2
GaAs Heterostructure ICs
(State of the Art, 1990)

IC Type	Advantage	Speed/Power Product	Reported Level of Integration	Representative IC Suppliers
HEMT	Lowest cost	5.8ps x 1.8mW per gate	64K SRAM	Fujitsu, Philips, Thomson, TI, TRW
C-HFET	Lowest power	100ps x 0.1uW per MHz per bit	1K SRAM	Honeywell
HBT	Highest speed	1.9ps x 40mW per gate	13,000 transistors/chip	Hughes, Pacific Monolithics, Rockwell, Thomson, TI, Toshiba, TRW

Note: At least 53 companies, universities, and other organizations are active in internal research and development of one or more of these circuit forms.
Source: Aztek Associates

density achievable in volume production in 1991 and 1992.

WHAT'S NEXT?

The technologies discussed in this newsletter and the suppliers investing in them are arrayed in a battle for supremacy in heterostructures. The stakes involved in betting on the winning technology are increased by the fact that the costs of production facilities are in an upward spiral. As a result, Dataquest believes that the days of the $30 million GaAs start-up are over, particulary in light of the fact that some vertically integrated suppliers have failed to make as much as a $30 million dollar profit in a bad year.

However, in spite of the risks, the failure of any company to place its bets will surely amount to conceding a market share victory to its competitors—missing the time-to-market window can be just as disastrous as backing the wrong technology.

Gene Miles

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Research Newsletter

ASIAN ACTIVITIES IN COMPOUND SEMICONDUCTORS IN 1990

SUMMARY

Annually, Dataquest prepares a summary of significant activities involving GaAs and related compound ICs and discrete semiconductors in Japan and other Asian countries. This newsletter highlights Asian companies' progress in this field during 1990. It includes information about the performance of GaAs ICs used in Japan's National Supercomputer Project. For the first time, particular focus is placed on GaAs ICs and related devices for optical data-processing applications.

JANUARY

Honda began captive pilot production of GaAs ICs for engine control sensors. Expansion of the facility, which is located in Hoga, Japan, will cost $14 million before its completion in 1992. Toyota and Nissan also have in-house IC capability, but Honda was first to produce GaAs ICs.

Fujitsu Ltd. announced that it will build a GaAs 4-inch wafer fab facility in Yamanashi Prefecture at its wholly owned subsidiary, Fujitsu Yamanashi Electronics Ltd. The plant is part of Fujitsu's five-year plan to boost its communications equipment sales through intelligent communications and information-processing services, in which GaAs ICs are positioned as strategic devices.

Hitachi Ltd. and Mitsubishi Electric Corp. completed the prototype development of 4K GaAs SRAMs and demonstrated system operation as a part of the National Supercomputer Project. This program is sponsored by the Agency of Industrial Science and Technology, a division of MITI.

Engineers at Hitachi's Consumer Products Research Center have developed a compact GaAs tuner for use in 12-GHz satellite communications. The tuner uses a downconverter IC and an amplifier IC to reduce unit size by 50 percent to 40cc; Hitachi contends that it is the most compact tuner in the world.

Shizuoka University (Hamamatsu City, Japan) and Swiss Federal Institute scientists reported the first photovoltaic IR sensors fabricated in PbS layers on Si wafers. The design uses a stacked CaF_2-BaF_2 buffer layer to overcome the large lattice and thermal-expansion mismatches between the PbS and the Si.

Scientists at Academy Sinica (Beijing, China) performed photoluminescence studies in an effort to better understand the radiation mechanisms in heavily doped n-type and p-type GaAs materials. Silicon and beryllium were used as dopants in the studies.

NTT's Optoelectronic Laboratories reported operating relatively stable GaInAs single-quantum well lasers at 30mW CW and pumping Er (erbium)-doped fiber amplifiers with maximum signal gain of 37.8dB at 1.536-micron wavelength. The use of Er-doped fiber in communication links has previously been demonstrated by AT&T as a means of eliminating regenerator circuits in undersea cables, greatly enhancing reliability.

FEBRUARY

Mitsubishi Electric Corp. has plans to build a GaAs semiconductor facility at an expected cost of ¥5 billion ($34.5 million) to support its satellite communications business. Monthly capacity will be 500,000 ICs, using a 4-inch fabrication process.

In a paper presented at the ISSCC in San Francisco, Fujitsu Ltd. reported developing a high-speed random-number generator using high electron mobility transistor (HEMT)-based ICs. The three types of ICs used were a system controller LSI, a data buffer LSI, and a 3319-gate shift register/logic chip. The subsystem operates at liquid nitrogen temperature at 1.6 GHz and has

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4.5W power consumption. The development was part of the National Supercomputer Project.

NEC developed a 0.5-micron-gate metal-insulator semiconductor field-effect transistor using AlGaAs layered onto a GaAs substrate. The transistor, referred to by NEC as a doped-metal transistor, allows a gate-switching speed of 4.8ns in a 25-stage ring oscillator. A 5-stage shift register using the device was operated at 5 Gbps while consuming 45mW of power. NEC plans to apply the technology to optical communications systems.

Toshiba began marketing samples of its TOLD9220, a semiconductor (InGaAlP) index-guided CW laser operating at 660nm wavelength. Priced at approximately $200, the device is intended to replace 670nm models and surpass helium-neon gas lasers in many applications. Toshiba expects to market 638nm diode lasers within a few years.

MARCH

Major Asian chipmakers plan to increase production of GaAs HEMTs used in downconverters for satellite broadcast receivers. The market in Japan for satellite antennas grew 40 percent in 1989 to 650,000 units and was expected to triple in 1990. Mitsubishi doubled its HEMT production to approximately 300,000 units per month, and Sony tripled its output to 100,000 units per month. Other manufacturers were expected to follow these moves.

Hamamatsu Photonics engineers fabricated metal-semiconductor-metal photodiodes for use in ultrafast optical impulse detection applications. The photodiode area is 10 microns on each side. Measured rise and fall times were each less than 10ps.

Mitsubishi's Central Research Lab (CRL) (Amagasaki, Hyogo) built and characterized quantum well wires (QWWs) on GaAs by MBE. The 7nm-thick-by-90nm-wide wires were spaced on 220nm centers. The structures will be applied to photonic ICs. Mitsubishi's CRL also reported demonstrating ultrahigh gain HBTs (gain values ranging from 112,000 to 141,000) of InGaAsP-on-InP substrates.

NEC scientists (Fundamental Research Labs, Tsukuba, Ibaraki) achieved atomic layer epitaxy (ALE) growth of InGaP/GaAs alternating layers on GaAs with monolayer control. The process, more precisely defined than is possible with metal-organic CVD or MBE, supports ultrafine IC fabrication.

NEC Corp. has reached an agreement with the Chinese government (People's Republic of China) to build an IC plant in Beijing for production of ICs for communications systems. The joint-venture agreement follows the lifting of economic sanctions by the Japanese government and relaxation of COCOM regulations.

APRIL

Fujitsu Ltd. planned to boost its production of HEMTs to 3 million units per month by the end of 1990, tripling its rate. As many as five HEMTs are in each satellite broadcast receiver antenna, and more than 1 million such antennas will be consumed by the Japanese market in 1990.

NEC announced a 20-year plan to invest ¥30 trillion ($200 billion) to connect every household and office in Japan through a digital fiber-optic network. The plan includes development of terahertz transmission-rate hardware and HDTV service and is expected to place large additional demand on the compound semiconductor IC industry infrastructure.

A U.S. District Court ruled that Sumitomo Corporation infringed on Corning Inc.'s optical waveguide patents. Sumitomo was ordered to pay $25 million in settlement.

Toshiba America began marketing 5mW visible laser diodes (VLDs) that use index guiding to reduce astigmatism by a factor of three. The VLDs have threshold current of 50mA versus the industry standard of 80mA, making the devices suitable for battery operation.

A research group at Toyohashi University of Technology built a prototype optical-calculating chip. The device uses a laterally variable refractive film as a light switch. By processing photons instead of electrons, the chip performs arithmetic literally at the speed of light. Expected applications include computers, pattern recognition, and artificial intelligence systems.

Hewlett-Packard Company established a research laboratory in Tokyo, which will focus on applied research in photonics. The staff will work with other HP scientists as well as visiting scientists and professors on projects of interest to HP and its joint venture, Yokagawa Hewlett-Packard.

MAY

Mitsubishi Electric Corporation, a major supplier of semiconductors including GaAs and related

compound semiconductor ICs, lasers, and other discretes, launched a major market expansion initiative in Southeast Asia. The company set up a technical support center in Singapore, adding to its current sales and marketing bases in Taiwan, Hong Kong, and South Korea.

NTT's Optoelectronic Laboratory (Atsugi, Japan) achieved 40ps response times on photodiodes fabricated by the MBE growth of AlGaInAs/InAs MQW structures on GaAs substrates. Intended applications include detection of 160nm wavelength signals.

Scientists at the Indian Institute of Technology and the Tata Institute of Fundamental Research, Bombay, India, fabricated and analyzed OPFETs (photo-metal semiconductor FETs), which are capable of detecting 100ps light pulses at a 2-GHz rep rate. They found that the light-energy level above the bandgap of the transistor is detected by band-to-band excitation, and light energy below the bandgap of the transistor is detected by internal photoemission. In each case, the MESFET gate Schottky barrier is acting as a photodiode.

Japan's Optoelectronic Industry Trade and Development Association reported that Japan's production of optoelectronic detectors and sensors grew by 13 percent, from ¥26.2 billion to ¥29.5 billion ($187 million to $210 million) for the year ended March 31, 1990, versus fiscal year 1988 ended March 31, 1989.

JUNE

Toyohashi Institute of Technology (Aichi, Japan) students proposed a photodiode/4-FET cell for application in neural networks as an OEIC synaptic-connection circuit with variable analog weights. This work is supported by the Japan Ministry of Education, Science, and Culture.

Scientists at the Tokyo Institute of Technology completed characterization studies of CuInSe and other II-VI compounds for solar-cell applications. A conversion efficiency of 8.16 percent was achieved for cadmium sulfide on CuInSe by optimizing the structures using Raman scattering spectrometry.

Toshiba's Kawasaki R&D Center reported using a KrF excimer laser to grow GaAs epitaxial layers over the range of 470 to 530°C, enabling volume production by the ALE method. The allowable temperature spread without laser irradiation was so narrow that it prevented highly repeatable results.

NTT's Yokosuka Electrical Communication Laboratories (Kanagawa, Japan) developed a digital mobile transceiver containing the following chips:

- GaAs MSI quadrature modulator IC
- GaAs LNA, frequency divider, and detector IC
- Si CMOS LSI waveform generator, coherent demodulator, codec, and framing circuit

JULY

Matsushita built and operated a 32 x 32 array of optoelectronic bistable switches, with each cell consisting of an HPT and an LED. Optical feedback from the LED to the HPT causes latching. The chip is called a photonic parallel memory.

Engineers at NEC's Optoelectronic Research Labs, Ibaraki, Japan, reported building and testing MBE-grown matrices of vertical-to-surface transmission electrophotonic device structures. The devices have optical-switching energy of 2pJ when biased at 1.9 volts. By using a laser diode light beam through an optical-mask pattern, the parallel operation functions of optical pattern writing, memory retention, optical regeneration, and erasing were performed. NEC plans to integrate the functions into larger arrays for use in optical data-processing systems.

Sumitomo fabricated a GaAs 16 x 16 multiplier IC using electron-cyclotron resonance CVD (ECR-CVD). Yields were at the 50 percent level, using 0.45u gate FETs, which demonstrated 39-GHz cutoff frequency.

Researchers at Sophia University (Tokyo, Japan) demonstrated what they reported to be the first emission of yellow light using MQW lasers grown by GS-MBE. The lasers consist of GaInP/AlInP layers on InP substrate, emitting at 576nm wavelength.

NEC introduced an optical hand-held range finder based on an Er-doped fiber amplified (EFDA) laser emitting at 2.8-micron wavelength, considered "eye-safe" by the manufacturer. Resolution is 5 meters over a working range of 100 to 10,000 meters.

Researchers at Fujitsu and KDD reported that EFDAs could be cascaded up to 100 stages without restricting 2.5-Gbps optical signals. The limit for semiconductor laser amplifiers was considered to be 20 stages at a 2.5-Gbps transmission rate.

AUGUST

Recent III-V device work by Asia/Pacific organizations is described in Table 1.

SEPTEMBER

Sumitomo developed a mass-production, back-grinding technology for thinning GaAs wafers containing MMICs to less than 150 microns. The technique incorporates a chemical etch after the grinding operation to reduce wafer bow. The use of this approach caused threshold voltage shift of less than 5mV. The technique was demonstrated on a 16 x 16 parallel multiplier IC as well as on SSI-density OEICs. Sumitomo now uses this technology in the production of raw wafers as well as in IC manufacturing.

Matsushita developed a microbump bonding method for assembling GaAs LED array modules. The first modules were functions containing LED chips and LSI driver chips, mounted on a glass substrate.

NTT reported a new method of measuring strain distribution within an optical fiber, in contrast to previous methods, which were limited to measuring average strain over the entire cable length. The method involves using laser-induced pump and probe beams to measure back-traveling power over time.

OCTOBER

Hitachi described test results for the Japanese National Supercomputer Project at the 1990 GaAs IC Symposium. Japanese government funding of approximately $120 million, supplemented by R&D support from Fujitsu, Hitachi, Mitsubishi, NEC, Oki, and Toshiba, supported the project. Objectives included a thousandfold improvement in computing speed and a hundredfold reduction in package volume.

To achieve system performance objectives, device technology requirements were set at 30ps per gate at room temperature and 10ps per gate at 77°K for logic LSI chips and sub-10ns cycle time for 16K SRAMs. The demonstration hardware consisted of a high-speed parallel processor with four processing elements, a distributed parallel processor, and a 4-Gbyte high-speed storage unit. In January 1990, the demonstration unit was operated at 10.9 Gflops. GaAs IC applications in the demonstration system were as follows:

- Bus drivers for HPP—1.1K-gate logic LSI using 0.5-micron-gate AlGaAs/GaAs HEMTs (8 chips, supplied by Fujitsu)
- Pseudorandom number generator—3.3K-gate E/D DCFL HEMT LSIs operating at 77°K (8 chips, supplied by Fujitsu)

TABLE 1
Recent III-V Semiconductor Developments in Asia/Pacific

Organization	Location	Topic
National Defense Academy	Yokosuka, Japan	Properties of AlGaAs
National Cheng Kung University	Tainan, Taiwan	MBE-grown AlGaAs
Nagoya Institute of Technology	Santa Clara, California	MOCVD of GaAs on Si wafers
NTT Opto-Elec. Lab	Kanagawa, Japan	Ar laser-assisted epi growth of GaAs, GaP, GaAsP
Osaka University	Osaka, Japan	MBE-grown GaAs on Si wafers
Mitsubishi Opto and Microwave R&D Lab	Hyogo, Japan	AlGaAs laser diode fabrication techniques
Japan Broadcasting Corp.	Setagaya, Japan	Bistable laser diode operation
Sony Corp. Research Center	Yokohama, Japan	Modeling and characterization of GaAs JFETs and MESFETs
KAIST (Korea Advanced Institute of Science and Technology	Seoul, South Korea	HFETs using GaAs
NEC R&D Laboratories	Kawasaki, Japan	Sidegating in GaAs MESFETs

Source: Arnak Associates

- System controller—1.3K-gate HEMT LSIs with 17ps gate delay, operating at 77°K (4 chips, supplied by Fujitsu)
- Data buffer—0.7-micron-gate HEMT-based 4Kb SRAMs with 0.5ns cycle time, operating at 77°K (8 chips, supplied by Hitachi)
- Cellular array processor—16Kb (4Kx4) SRAMs with 4.4ns access time, using buried-p-layer, lightly doped-drain MESFETs, and three-layer metal interconnects (64 chips, supplied by Mitsubishi)
- Variable pipeline processor—3,376-logic gates and 76-bit dual-port register file (8-bit bus logic) LSIs using 0.8-micron-gate MESFETs (48 chips, supplied by Toshiba)
- Display processor—100-gate and 700-gate, 0.5-micron inverted-HEMT MSIs, one each per chip set (3 sets or 6 chips)

These chips were used to implement a demonstration system, which transferred data from storage at 1.6 Gbps and performed color signal processing at 400 MHz. The four-element parallel processor was operated at 10.9 Gflops, placing it near the high end of available supercomputing systems. Based on demonstrations already completed, Hitachi concluded from this work that GaAs LSI is ready for the mainstream EDP marketplace.

NOVEMBER

KDD and AT&T planned a new transpacific cable system, which will connect Japan and the U.S. mainland by 1996. The 2.4-Gbps system will employ Er-doped fiber repeaters rather than optoelectronic repeaters, eliminating the need for reconfiguration when bit rates or modulation schemes change.

Matsushita's Semiconductor Research Center (Osaka, Japan) has generated 12.3mW of second-harmonic blue light from a semiconductor laser source. This was done by using a $LiNbO_3$ proton-exchanged waveguide doped with MgO, driven by an AlGaAs laser.

NTT's Lightwave Communications Laboratory (Tokai, Japan) engineers accomplished 180-250fs (femtosecond) optical pulse generation with peak power of 260W and average power of 32mW using a gain-switched DFB laser diode, erbium-doped amplifiers, and three-stage soliton compression. NTT operated a 40-Gbps time division cell multiplexer for a photonic asynchronous transfer mode switch. By using MQW lasers, NTT hopes to raise the bit rate to several hundred Gbps.

NTT LSI Labs (Kanagawa, Japan) reported building high-gain, carbon-doped MOCVD-grown AlGaAs/GaAs HBTs. The transistors demonstrated current gain of 100. NTT is developing AlInAs/InP HEMTs and has demonstrated 0.8u-gate devices with f_{max} of 65 GHz and f_T of 22 GHz. The company claims these to be the best results reported to date.

DECEMBER

NTT Optoelectronic Labs (Kanagawa, Japan) reported improved InAlAs/InGaAs on InP HBTs, achieving gain of 200 at I_c of 10mA and f_T of 96 GHz. Potential applications involve integrating the HBTs onto OEICs along with 1.3- to 1.55-micron-range optical sources and detectors.

Engineers at Hamamatsu Photonics KK have designed a dynamic optical memory cell consisting of two photodiodes and a laser diode. The cell, measuring 100 x 100 microns, requires minimum speed-power products for set and reset operations of 5 and 35pJ, respectively. Applications will include optical data-processing (ODP) systems.

Other ODP developments under way at various Asia/Pacific organizations include those shown in Table 2.

DATAQUEST CONCLUSIONS

As 1990 ended, Japan maintained its lead among Asia/Pacific competition in the compound semiconductor arena, particularly in GaAs digital and linear ICs and in semiconductor lasers. Among Asia/Pacific companies, NTT continues to lead in basic compound semiconductor device R&D, particularly in those areas expected to result in more efficient optical communications and switching systems. In fact, on a worldwide basis, NTT appears to be second only to AT&T's Bellcore.

Although much effort has been directed toward optical computing and data processing, the rewards to date have been few. The primary benefits so far have appeared in digital communication systems within Japan. The technology required to build an all-optical computer still appears a few years away from critical mass in Japan, with other Asian countries behind Japan in this technology.

TABLE 2
Representative ODP Activities

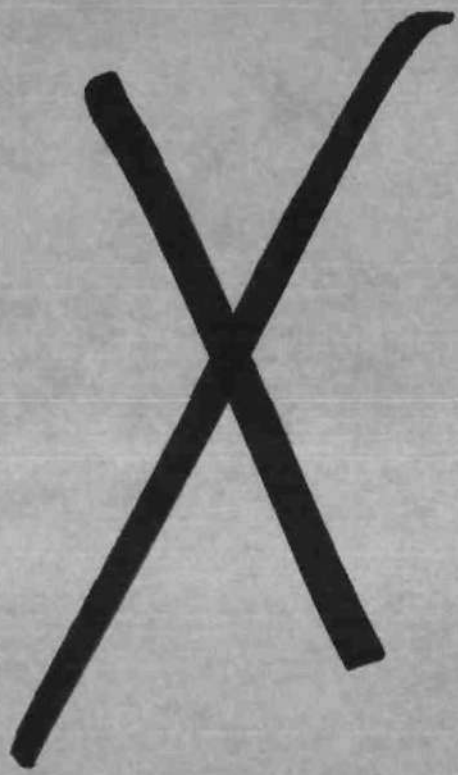
Organization	Location	ODP Activity
Hamamatsu Photonics KK	Hamamatsu, Japan	Learning capability studies of photonic CAMs
Kyushu University	Fukuoka, Japan	Design of laser diode modules with spherical and other lens types
NTT Labs	Kanagawa and Tokyo, Japan	Developing ODP ICs; implementation of ODP hardware using SLMs in electronic host computer
Osaka University	Osaka, Japan	Optoelectronic parallel processing logic
Shanghai Inst.	Shanghai, PRC	Optoelectronic implementation of cellular logic with polarization coding
Sony, Cal. Tech	Tokyo, Japan; Pasadena, California	ODP hardware development using WORM disk and GaAs neurons
Yonsei University	Seoul, South Korea	R&D of coding algorithms for logic operations in photorefractive crystals

Source: Aztek Associates

Following NEC's lead, Fujitsu and Hitachi are helping to bring IC technology into the consumer household, finding applications in portable radiotelephones, TV front-end hardware, and satellite TV downconverters. With expansion under way at Honda, the automotive industry now has a Japanese supplier capable of producing its own GaAs chips for engine control and other applications.

Perhaps most disconcerting of the 1990 developments to U.S. and European computer makers alike, is this: The Japan National Supercomputer Project is running (at 10.9 Gflops) on GaAs LSI chips. Cray and others are letting huge opportunities slip away as yet another U.S.-invented industry yields to growing Japanese competition.

Gene Miles



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Research Newsletter

SIS MEMORY QUARTERLY NEW PRODUCTS NEWSLETTER

This newsletter contains a synopsis of memory product news events gathered from the trade press and company releases during the third quarter of 1990. This newsletter is meant to be used as a reference guide of new products for competitive analysis, monitoring technology trends, and tracking future developments and improvements. Dataquest assumes no responsibility for the accuracy of the contents.

Table 1 shows the new products announced during the third quarter of 1990.

DRAM DEVELOPMENTS

EDI

Electronic Designs Inc. (EDI) introduced the 1Mb CMOS DRAM. The device is available in two organizations—a page-mode 256Kx4 (EDI44256C) and the 1Mbx1 (EDI411024C). The access times available for both devices are 70, 80, 100, 120, and 150ns. All I/Os are fully TTL compatible and operate from a single 5V power supply.

NEC

NEC Electronics announced the availability of its 4Mb DRAM, organized in 4Mbx1 and 1Mbx4. The devices are manufactured using NEC's 0.7-micron CMOS process. The product is available in a 300-mil SOJ package.

NMB

NMB Technologies Inc. announced shipments of 1Mb DRAMs clocked at 53ns. The devices are configured in 1Mbx1 and 256Kx4 versions. The high-speed design allows for direct memory access with 16-MHz and 20-MHz microprocessors, which NMB claims eliminates the need for cache memory devices.

SRAM DEVELOPMENTS

SGS-Thomson

During the third quarter, SGS-Thomson announced its MK48256, a 32Kx8 static RAM. This CMOS circuit is available with 100 or 120ns access and cycle times and standard or low-power options. Packaging is a 28-pin PDIP with plans to have a 32-pin SOIC package available in the future.

Micron

Micron Technology, Inc., announced a military standard 128Kx8 SRAM with an address time of 14ns. The device is available in DIP and LCC packaging, with a 32-lead flatpack available in early 1991.

EDI

Electronic Designs Inc. has introduced two 256K high-speed CMOS static RAMs. The EDI8834C is a 32Kx8 standard power device available in both plastic and hermetic packages and is available with access times of 35, 45, and 55ns. The EDI8833C/P is also organized as 32Kx8 but is available only in hermetic package styles. Access times are 35, 45, and 55ns.

Vitesse

Vitesse Semiconductor Corporation announced the availability of the VS12G478, which

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TABLE 1
New Memory Products—Third Quarter of 1990

Company	Density/Description	Speed
DRAM Developments		
EDI	1Mb	70, 80, 100, 120, and 150ns
NEC	4Mb	60 to 100ns
NMB	1Mb	53ns
SRAM Developments		
SGS-Thomson	32Kx8 SRAM	100, 120ns
Micron	128Kx8 SRAM	14ns
EDI	32Kx8	35, 45, and 55ns
Vitesse	GaAs 4K Purge	5ns
IDT	16K and 256K	7, 12ns
	64K	7ns
	64K synchronous	12ns
Quality Semiconductors	64K	12ns
Samsung	1Mb	85, 100, 120ns
Nonvolatile Memory Developments		
Xicor	2K EEPROM	NA
Samsung	RAM DACs	NA
ICT	1K CMOS serial EEPROM	NA
Hitachi	256K EPROM	200ns
	1Mb Flash	120, 150ns
	1Mb UV EPROM	100ns
	4Mb UV EPROM	100ns
	4Mb mask ROM	100ns
AMD	1Mb Flash	90ns
Specialty Memory Developments		
Micron	Video card	NA
	Triple-port DRAM	NA
	1Mb video RAM	NA
	1Mb video RAM	80ns
SGS-Thomson	32-bit cache	25ns
IDT	FIFO	25ns
	Cache RAM	NA

Source: Dataquest (January 1991)
NA = Not available

is a gallium arsenide (GaAs) 4,096-bit, read/write self-timed SRAM. The design is organized as 2,048 words by 2 bits and features a "clear-all-bits-to-zero" purge capability. The design has a maximum read/write cycle time of 5ns. The device requires only a standard negative 2V power supply and has a power dissipation of less than 1W. Packaging is 28-pin leaded ceramic chip carrier (LCCC).

IDT

Integrated Device Technology (IDT) announced two additional BiCEMOS ECL I/O SRAMs: 16K and 256K. The 16K SRAMs are organized as 4Kx4 and produced using IDT's 0.6-micron BiCEMOS II process with speeds as fast as 7ns. The 256K devices are organized as 64Kx4 and attain speeds as fast as 12ns. Both devices are available in 300-mil small-outline J-bend packages.

In conjunction with IDT's above-mentioned SRAMs, the company also announced a BiCEMOS ECL 64K SRAM with address access times of 7ns. These devices are organized as 16Kx4 with separate data I/Os. They are available with address access times of 7, 8, 10, and 15ns.

IDT announced a synchronous 64K BiCEMOS ECL self-timed SRAM organized in 16Kx4 using IDT's 0.6-micron BiCEMOS II process. The devices deliver cycle times as fast as 12ns while typically consuming only 1,000 milliwatts (mW). They are available in a 400-mil ceramic package or a 300-mil plastic SOJ package.

Quality Semiconductors

Quality Semiconductors, located in Santa Clara, California, announced its 16Kx4, 12ns access time devices. The products are available in 300-mil plastic DIP, SOIC, SOJ, and ZIP packaging.

Samsung

Samsung announced its 1Mb SRAM organized as 128Kx8 in access times of 85, 100, and 120ns. The device is powered from a single +5V source and features very low power dissipation in both standby and data-retention modes. This SRAM is available in a standard 32-pin plastic DIP 600 mils wide and in a 32-pin plastic SOJ 525 mils wide for surface-mount applications.

NONVOLATILE MEMORY DEVELOPMENTS

Xicor

Xicor, Inc., announced the availability of a CMOS 2K serial EEPROM. The X24C02 is organized as 256x8 and offers low active current of less than 1mA at 100 KHz and a standby current of less than 50uA. The device is available in an 8-pin plastic DIP, Type P, and an 8-pin plastic SOG package, Type S.

Samsung

Triple 6-bit and 8-bit high-performance digital-to-analog (D/A) converters known as RAM DACs have been developed by Samsung. These devices are being manufactured using a double-metal 1-micron CMOS process. The RAM DACs are available in three versions: KDA0471, which contains a 256x18-bit look-up table and three 6-bit video D/A converters; KDA0476, which is similar to the previous device but does not contain overlays or synch information on the analog inputs; and KDA0478, which contains a 256x24-bit look-up table and three 8-bit video D/A converters.

ICT

International CMOS Technology Inc. (ICT) announced the availability of 93C46A, a 1K CMOS serial EEPROM. The device is targeted toward low-cost, low-power microcomputer-based systems such as telephones, cameras, VCRs, pagers, meters, and modems.

Hitachi

Hitachi's HN58C256 is a 256K EEPROM with access times of 200ns, available in 28-pin DIP, SOP, and TSOP.

Hitachi's 1Mb Flash EEPROM, HN29C101, is organized as 128Kx8 with access times of 120 or 150ns. These devices are available in plastic DIPs.

The 1Mb UV EPROM from Hitachi, HN27C101A/301, is organized as 128Kx8 and provides access times to 100ns.

HN27C4096 is a high-speed 4Mb UV EPROM, is organized as 256Kx16, and offers access speeds of 100ns. The device is available in JEDEC-approved package types, a 40-pin DIP, and a 44-pin JLCC.

Hitachi's 4Mb mask ROM offers access speeds to 100ns. Multichip versions are available in both 8Mb and 16Mb densities in 48-pin packages.

AMD

Advanced Micro Devices (AMD) announced its entry into the Flash memory market with a 1Mb device clocked at 90ns. AMD will use its CMOS process technology for producing the Flash memory devices. The packages available for these devices are 32-pin DIP and PLCC.

SPECIALTY MEMORY DEVELOPMENTS

Micron

Micron Technology introduced the Xceed NB12-108 multiple-resolution video card for Apple Mac II computers. The video card delivers twin-page image capability (1,152 x 870 resolution) and is designed to take advantage of the higher refresh rates of the newer 19-inch screens.

A new device in the video RAM area also was introduced by Micron. The device, a multiple-port video RAM (MT43C4257), is a CMOS 256-kword-x-4-bit DRAM with twin 512-kword-x-4-bit serial-access memory (SAM) ports built from static memory cells. All three ports are asynchronous and operate independently of one another.

Added to Micron's product family was its 1Mb video RAM in 128Kx8 and 256Kx4 organizations. The 128Kx8 offers standard speed grades and comes in a 40-pin SOJ package. The 256Kx4 has the same speed grades and is packaged in 28-pin ZIP and 28-pin SOJ types.

Micron also announced the 1Mb triple-port DRAM configured as a 256Kx4 DRAM with dual 512Kx4 serial access memory ports. The new CMOS devices have fast access times of 80ns for random access memory and 25ns for serial access memory. The device comes in a 40-pin SOJ package.

SGS-Thomson

SGS-Thomson announced the availability of a 2Kx20 cache 20-bit-wide TAGRAM. The MK4202 operates at access speeds of up to 50 MHz. The device has an 11-bit tag address and a 19-bit tag width that can handle a 30-bit address and most 32-bit applications.

IDT

Integrated Device Technology introduced its communications FIFO, which is an integrated parallel-to-serial device with a 16-bit data bus and a high-speed shift register with a frequency of 50 MHz. The devices are available in 256Kx16, 512Kx16, and 1Kx16 configurations with access speeds of 25ns. They are available in DIP, SOIC, and PLCC packages.

IDT announced the availability of its IDT71589 cache RAM, which is a 32Kx9 cache designed for zero-wait secondary caches in 25 and 33 MHz and faster Intel i486 systems. The device is available in 32-pin plastic SOJ packages, as well as plastic and hermetic DIP packages.

Ione Ishii

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Research Newsletter

SIS MEMORY QUARTERLY NEW PRODUCTS NEWSLETTER

This newsletter contains a synopsis of detailed memory product news events gathered from the trade press and company releases during the fourth quarter of 1990. This newsletter is meant to be used as a reference guide of new products for competitive analysis, monitoring technology trends, and tracking future developments and improvements. Dataquest assumes no responsibility for the accuracy of the contents.

Table 1 shows new products announced during the fourth quarter of 1990.

TABLE 1
New Memory Products—Fourth Quarter 1990

Company	Density/Description	Speed
	DRAM Developments	
NMB Technologies, Inc.	1Mb	53ns
Texas Instruments	16Mb	NA
	SRAM Developments	
Samsung	64K	70ns
NEC Electronics, Inc.	1Mb	70, 80, 100ns
NEC Corporation	1Mb	20ns
Micron	1Mb	25ns
	1Mb, military	25ns
IDT	BiCMOS 256K	12, 15ns
	256K, CacheRAM	NA
UMC	1Mb	60ns
Inova	1Mb	25, 35ns
	Nonvolatile Memory Developments	
AMD	256K EPROMs	35, 45, 55, 70ns
	2Mb EPROMs	150ns
Microchip	64K, 128K, 256K, 512K EPROMs	120 to 250ns
Xicor	8K EEPROMs	NA
Intel	4Mb EPROMs	150, 200ns

(Continued)

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TABLE 1 (Continued)
New Memory Products—Fourth Quarter 1990

Company	Density/Description	Speed
	Specialty Memory Developments	
Dallas Semiconductor	4Mb memory card	NA
Cypress	FIFOs	30, 40, 50, 65ns
Vitelic	DRAM memory modules	70, 80, 100ns
AMD	FIFOs	15ns
EDI	2Mb SRAM modules	85 to 150ns
Smart Modular Technologies	4Mb SRAM modules	100ns
IDT	Dual-port RAMs JEDEC modules	25ns 15, 30ns
Micron	1Mb video RAMs	10, 12, 15ns

NA = Not available
Source: Dataquest (January 1991)

DRAM DEVELOPMENTS

NMB Technologies

NMB introduced its new AAA1M300 series 1Mb DRAM, which is clocked at 53 nanoseconds (ns). The high-speed device is offered in 1Mbx1 and 256Kx4 configurations. Speeds are available in 53, 60, and 70ns. Read/write cycle times are reported to be as low as 100ns. The company claims that this design allows for direct memory access with 16-MHz and 20-MHz microprocessors, eliminating the need for cache memory and improving system performance. The device is available in plastic DIP, ZIP, and SMT packages with industry-standard interfaces and pinouts.

Texas Instruments (TI)

TI began customer sampling of its two versions of the 16Mb DRAM. The device is constructed using a modified trench capacitor cell and 0.6-micron design rules with a CMOS technology. The versions available are configured as 16Mbx1 and 4Mbx4.

SRAM DEVELOPMENTS

Samsung

Samsung Semiconductor redesigned its industry-standard 64K SRAM with submicron CMOS technology. The SRAM is organized as 8Kx8 and has a lower power consumption than does the original version. Active power has been reduced by 45 percent and now is less than 250mW, which is maximum. The device is available in three types of packages: 28-pin 300-mil skinny plastic DIP, 28-pin 600-mil DIP, and 28-pin 330-mil gull-wing plastic small-outline package for surface-mount applications.

NEC Electronics, Inc.

The North American subsidiary of NEC Electronics announced the availability of a 1Mb SRAM, uPD43100A, which is a low-power, low-profile memory that is ideal for high-density applications such as laptop computers, calculators, bar-code readers, disk drivers, and pocket computers. This 0.8-micron CMOS device features access speeds of 70 to 100ns. The device operates on a single +5V power supply with TTL-compatible inputs and outputs. The device is available in DIP, SOP, and TSOP.

NEC Corporation announced its development of a 1Mb SRAM with access speeds clocked at 20ns. Sample shipments occurred in November 1990.

Micron

Micron Technology, Inc., announced its 25ns 1Mb SRAM organized as 128Kx8, 256Kx4, and

1Mbx1. The product is offered in plastic and ceramic DIP, plastic SOJ, and ceramic flatpack and LCC packages.

Late in 1990, Micron announced the availability of its 25ns 128Kx8 SRAM, which was qualified to the MIL-STD-883C military level. The 1Mb SRAM is available in a 400-mil ceramic DIP package.

IDT

Integrated Device Technology (IDT) introduced three versions of its BiCMOS 256K with access speeds as low as 12ns. One device is organized as 32Kx8 and has a JEDEC Standard 28-pin device with power consumption of 450mW and address access time of 15ns. Another device is organized as 64Kx4, with a 5ns output-enable function. Access speeds as low as 12ns can be obtained; the product consumes 450mW and uses conventional JEDEC 28-pin PDIP and SOJ packages. The last device is organized as 64Kx4 in the standard 24-pin 300-mil PDIP and 24-pin SOJ packages, with power consumption of 450mW and access times as low as 12ns.

IDT announced its IDT71589 CacheRAM, which is a 32Kx9 cache memory designed for zero-wait secondary caches in 25-MHz, 33-MHz, and faster Intel i486 systems. The device is available in 32-pin plastic SOJ packages as well as plastic and hermetic DIP packages.

UMC

United Microelectronics Corporation (UMC) announced the development of its 1Mb SRAM, which is built using its 0.8-micron double-metal and double-polysilicon technology. The device has a standby current of 0.1mA, operating current of 15mA, and speeds as fast as 60ns.

Inova

Inova Microelectronics Corporation announced a series of 25 and 35ns 1Mb SRAMs organized as 128Kx8. Packaging options include 32-pin ceramic DIP, 32-pin CSOJ, and 32-pin flatpacks.

NONVOLATILE MEMORY DEVELOPMENTS

AMD

Advanced Micro Devices (AMD) announced production of its 256K EPROM, which has an access speed of 35ns. The device is organized as 32Kx8 and is offered in 28-pin ceramic DIP and 32-pin LCC packages. The device is available in access speeds of 35, 45, 55, and 70ns versions in the commercial temperature range with 10 percent power-supply tolerances.

AMD also announced that it is shipping its CMOS 2Mb EPROM, which is configured 256Kx8 and operates at 150ns. Aimed at the military applications market, the device is manufactured using the 1.0-micron CMOS technology.

Microchip

Microchip has introduced a line of CMOS EPROMs in SOIC surface-mount packages. The parts—in 64K, 128K, 256K, and 512K densities—all are in x8 configurations with access times ranging from 120 to 250ns.

Xicor

Xicor Inc. announced the availability of a new CMOS 8K EEPROM device specifically designed for use as a data and program memory for single-chip microcontrollers. The device is available in 24-pin DIP, Type P; 24-pin CERDIP, Type D; and 32-pin PLCC, Type J packages.

Intel

Intel Corporation announced its 27C400, a 4Mb EPROM that is pin-compatible with the emerging industry standard pinout for x16 mask ROM devices. The device is housed in a 40-pin ceramic DIP and is manufactured on Intel's 1-micron CMOS III-E process technology. The product is configurable either as 256Kx16 or 512Kx8 and offers access times of 150 and 200ns.

SPECIALTY MEMORY DEVELOPMENTS

Dallas Semiconductor

Dallas Semiconductor introduced a 4Mb memory card that reportedly reduces the number of

contacts needed to five. The cards use JEDEC-standard bytewide static RAM with an internal lithium battery that is said to maintain memory for ten years.

Cypress Semiconductor

Cypress Semiconductor introduced a pair of FIFOs organized as x9 that can read and write asynchronously at clock speeds of up to 25 MHz. The device is available in 30, 40, 50, and 65ns versions. Packaged in 28-pin, 600-mil ceramic DIP modules, the two parts feature independent read and write ports, full and empty flags, and expansion signals that reportedly allow unlimited expansion in width and depth.

Vitelic

Vitelic Corporation announced the availability of two-performance DRAM memory modules with configurations of 1Mbx8 and 1Mbx9. Access times have been clocked as low 70ns and are available in standard 30-lead SIMM and SIP modules.

AMD

AMD announced volume availability of its first CMOS FIFOs organized as 4Kx9 with an access time of 15ns. The device is built using a 1.2-micron CMOS process and is available in a 300-mil, 28-pin plastic DIP and 32-pin PLCC package.

EDI

Electronic Designs Inc. (EDI) now offers a 2Mb surface-mountable SRAM module. The device provides full 2Mb functionality with access times of 85ns through 150ns in a machine-placeable 32-lead package having the standard SOIC footprint and JEDEC pinout of a monolithic device.

Smart Modular Technologies

Fremont, California-based Smart Modular Technologies announced its availability of a 4Mb SRAM with a standard 32-pin, 600-mil-wide JEDEC dual-in-line package. The module is organized as 512Kx8 with an access time of 100ns. Operating from a standard 5V source, the device typically consumes only 90mW of power when active at 1 MHz.

IDT

IDT announced its 9-bit-wide dual-port RAM with access times as low as 25ns. The devices are offered in 48-pin PDIP, LCC, side-brazed 52-pin LCC, and PLCC packages with speeds ranging from 25ns to 55ns.

Also available from IDT are the JEDEC modules for cache and memory applications. The modules vary in density and speed, such as 16Kx32 at 15ns to 512Kx8 at 30ns. The modules are offered in DIP, ZIP, and SIMM packaging types.

Micron

Micron announced its 256Kx4 video RAM, which meets MIL-STD-883C military level. The device is available in a 28-pin ceramic DIP package at speeds of 10, 12, and 15ns.

Ione Ishii

Dataquest
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Research Newsletter

NORTH AMERICAN MEGABIT-DENSITY DRAM PRICE OUTLOOK: TODAY (1991), TOMORROW (1993), AND THE DISTANT FUTURE (1995)

EXECUTIVE SUMMARY

While the Gulf War wages, IC procurement teams grapple with plans for long-term megabit-density DRAM price trends. Meanwhile, a recent abrupt shift in global DRAM market conditions has altered the 1991 DRAM/VRAM pricing outlook to the joy of suppliers and the consternation of most users. As shown in Table 1, this newsletter provides a strategic perspective on Dataquest's Semiconductor User Information Service (SUIS) forecast of North American bookings prices for megabit-density DRAMs through the year 1995 and also sheds instant light on the altered 1991 price scenario. This newsletter states the critical assumptions behind the forecast regarding DRAM supply and demand, cost models, trade issues, and suppliers' strategies so that users and suppliers can respond to volatile DRAM market shifts.

OVERVIEW: AN ALTERED 1991 OUTLOOK PLUS THE LONG-RANGE VIEW

This newsletter focuses on four DRAM price

TABLE 1
Semiconductor Price and Lead Time Trends
(North American Bookings[1], Volume Orders)

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4Mbx1 80ns DRAM, SOJ (300 mil)	17.00 to 28.10	18.00 to 29.00	11.30	8.50
256Kx4 120ns VRAM, ZIP	10.05 to 10.55	10.05 to 10.55	7.67	6.85
4Mbx9 80ns SIMM	NA	NA	111.87[4]	86.05[4]

1 This SUIS forecast is for North American bookings pricing. *Worldwide* bookings pricing is somewhat higher.
2 These prices correlate with the SUIS forecast dated December 1990.
3 This price range is a *preliminary* estimate that correlates with the SUIS forecast that will be published during March 1991. Japan-based suppliers cut production during late 1990, which enabled DRAM pricing to increase during early 1991, as shown in this column.
4 Estimated but not by survey.
NA = Not available
Source: Dataquest (February 1991)

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estimates: the range of North American bookings prices, *originally* expected for the first quarter of 1991, as garnered through the SUIS year-end 1990 survey of users and suppliers; the preliminary results of the actual prices for the first quarter of 1991; the 1993 price forecast; and the 1995 price forecast. An emphasis is placed on highlighting the assumptions on which Dataquest bases the forecast in order to provide deeper insight into Dataquest's SUIS pricing outlook for 1991 and beyond. Because global DRAM market conditions have shifted so sharply since the quarterly price survey was conducted during November and December 1990, emphasis will also be made on the altered 1991 DRAM market/price outlook.

The price analysis presented here correlates with the quarterly and long-range price tables mailed to SUIS clients on December 20, 1990. For SUIS clients that use the SUIS on-line service, the quarterly pricing presented here correlates with the quarterly and long-range price tables dated December 1990 in the SUIS on-line service. The price analysis in this newsletter also correlates with the *Source Dataquest* report entitled "Semiconductor Price Outlook: First Quarter 1991," dated January 1991. For additional product coverage and more detailed product specifications, please refer to those sources.

DRAM MARKET CONDITIONS

The 1991 market for 1Mbx1 DRAMs recently changed sharply—and so have Dataquest's assumptions on the 1991 price outlook. The 4Mbx1 DRAM scenario remains in line with original assumptions, although it is somewhat modified. Although the 1991 price forecast for 1Mb DRAMs has changed, the assumptions for the long-range DRAM price forecast have *not* changed dramatically since December 1990.

1Mb DRAM: Japanese Suppliers Raise Prices and Other Suppliers Tag Along

Table 1 reveals that the participants in Dataquest's year-end 1990 price survey originally expected the North American bookings price for 1Mbx1 80ns DRAM SOJ in volume contract orders to range from $4.00 to $4.90 during the first quarter of 1991. From now on, the SUIS price forecast on DRAMs will refer to volume orders instead of the former specification, which was 100,000-piece orders. On this basis, in December 1990 SUIS forecast a price of $4.29 for the first quarter of 1991.

A Short-Term Assumption Proves Wrong

Under Ministry of International Trade and Industry (MITI) guidance, some Japanese suppliers have begun to withdraw from this market and have either raised the price for the 1Mb DRAM during early 1991 or held pricing stable at high levels. SUIS anticipated this trend by Japan-based suppliers but assumed that 1Mb DRAM suppliers from other regions would not join Japanese companies in raising prices. This assumption proved wrong. In fact, non-Japanese suppliers *for the time being* have joined Japan-based suppliers in raising the price for 1Mb DRAMs.

An Early Look at the Updated SUIS 1991 Price Forecast for 1Mbx1 DRAM

The SUIS first-quarter 1991 price survey is being conducted during February 1991, and the updated forecast will be published in March 1991. The early results of this survey indicate, in conjunction with other market information, that the actual first-quarter North American bookings price for the 1Mbx1 DRAM as specified will be between $4.25 and $4.90 versus the December 1990 forecast of $4.29.

Dataquest assumes that current market conditions—which are marked by Japan-based price "leadership" in terms of upward pressure on 1Mb DRAM prices, with other suppliers opportunistically following—will hold true for the first half of 1991. Under this assumption, North American bookings prices for 1Mbx1 DRAMs could edge *upward* during the second quarter of 1991. The early results of the current price survey signal such a price trend, followed by a flat or slowly declining price profile for the second half of 1991. For the fourth quarter of 1991, the North American bookings price forecast for 1Mbx1 DRAMs will likely be increased to $4.25 versus the original December 1990 forecast of $3.79 for year-end 1991.

4Mbx1 DRAM: Demand to Pick Up and Prices to Decline during 1991

Table 1 shows that participants in the fourth-quarter 1990 price survey originally expected the North American bookings price for 4Mbx1 80ns DRAM SOJ in volume contract orders to range from $17 to $28 during the first quarter of 1991. On this basis, SUIS forecast a price of $19.80 for the first quarter of 1991.

No Major Change in the SUIS 1991 Price Forecast for 4Mbx1 DRAM

The early results of the current (February 1991) price survey indicate that the actual first-quarter North American bookings price for 4Mbx1 DRAMs will be quite close to $19.80, which was forecast in December 1990.

Dataquest's operating assumption for 4Mb DRAM is that first-tier Japanese suppliers, along with other worldwide suppliers, will ramp up production during 1991 and cut prices in order to win business in line with historical crossover experience. This assumption has proved sound. Current market conditions are marked by a strong move by Japan-based suppliers from the 1Mb DRAM to the 4Mb device with consequent downward pressure on 4Mb DRAM prices. Although upward pressure on 1Mb DRAM prices reduces the incentive for sharp 4Mb DRAM price declines, Dataquest still foresees a 4Mb DRAM crossover (4:1 unit/price ratio) for the second quarter of 1991.

In fact, Dataquest believes that capacity for 4Mb DRAM is likely to *exceed* demand for 1991; however, suppliers will avoid bringing all of the capacity on-line this year in order to avoid a 4Mb DRAM market glut. The early results of the survey also indicate that the SUIS forecast on the North American bookings price for 4Mbx1 DRAMs for the fourth quarter of 1991 will likely be increased in nondramatic fashion to a price in the $14.50 to $15.00 range versus the original December 1990 forecast of $14.00.

MEGABIT-DENSITY DRAM: THE LONG-RANGE ASSUMPTIONS

As noted, most of the assumptions for the long-range DRAM price forecast have *not* changed dramatically since December 1990. Clearly, one assumption—that non-Japanese suppliers will continue to lower prices while Japan-based suppliers depart any given DRAM market segment—has been controverted for the short term.

The following key assumptions guide the SUIS long-range megabit-density DRAM price forecast for North America. First, global DRAM capacity will exceed market DRAM demand during the first half of this decade. A second assumption is that the foreign market value (FMV) system of pricing either will terminate during mid-1991 or will be replaced by a pricing system that assures low-priced DRAMs for North American users. Third, cost-based price reductions will assure lower pricing for 4Mb DRAMs and competitive pricing for 1Mb devices. A fourth assumption—which Dataquest still believes will hold true after 1991—is that non-Japanese suppliers will again continue to lower megabit-density DRAM prices to take market share as leading-edge Japan-based suppliers migrate to next-generation products.

During February and March 1991, Dataquest Semiconductor Industry Service (SIS) and SUIS analysts in San Jose, California, will work closely with SIS DRAM analysts in Tokyo and London to reassess these assumptions and the concomitant SUIS DRAM price forecast.

1Mbx1 80ns DRAM: The Critical Assumptions

Under these assumptions and as shown in Table 1, Dataquest anticipates that the North American bookings price for 1Mbx1 80ns DRAM SOJ in volume orders will be $3.40 for 1993 and reach bottom at a price of $3.20 for 1995.

In terms of the four assumptions, these points should be stressed. First, analysts in Dataquest's Semiconductor Equipment, Manufacturing, and Materials Service (SEMMS) and SIS Memory recently analyzed the combined worldwide demand for 1Mb DRAMs and 4Mb DRAMs against the megabit-density DRAM fab capacity outlook for the 1990 to 1994 time frame. This analysis *conservatively* estimates that megabit-density DRAM capacity utilization should reach its highest level, 77 percent, during 1991 and decline to 74 percent for 1994. Succinctly, megabit-density DRAM capacity should exceed demand over the long term, barring a major and unexpected supplier reduction of production capability.

Second, a 1Mb DRAM cost model developed by SUIS and SEMMS analysts reveals that suppliers will be able to profitably manufacture this device at the prices specified in the SUIS forecast (i.e., $3.40 for 1993 and $3.20 for 1995). Next, Dataquest anticipates the demise of the FMV system—but the remaining 1Mb DRAM suppliers will be non-Japanese and thus will be unaffected even if FMVs do survive in some form.

An Early Look at the Updated Long-Range Forecast for 1Mbx1 DRAM

Because non-Japanese suppliers opportunistically raised 1Mbx1 80ns DRAM prices early in 1991, Dataquest realizes that the anticipated

long-term decline in 1Mb DRAM pricing is likely to start at a higher 1991 level than the original 1991 forecast price of $4.02. Suppliers may aim for continued *upward* pressure on pricing, but long-term market forces should dictate otherwise. During March 1991, the North American bookings price forecast likely will be increased for 1993 to a price of about $3.80 and for 1995 to a price range of $3.40 to $3.60.

4Mbx1 80ns DRAM: The Forecast Remains Consistent

In line with the previously mentioned four assumptions and supporting analysis, as shown in Table 1, Dataquest anticipates that the North American bookings price for the 4Mbx1 80ns DRAM SOJ in volume orders will be $11.30 for 1993 and $8.50 for 1995.

In terms of the four assumptions, the following points are stressed. First, as noted, megabit-density DRAM capacity should exceed demand over the long term, barring an unanticipated cutback in capacity. Next, Dataquest's 4Mb DRAM cost model conservatively shows that suppliers will be able to profitably manufacture this device at the price levels indicated in the long-range SUIS forecast. Third, the anticipated termination of the FMV system—or its replacement by a less onerous pricing scheme—would permit pricing to decline at an even more rapid rate than projected by the SUIS forecast.

A volatile element of risk always lurks in the DRAM marketplace. Regarding the long-range 4Mb DRAM market/price outlook, one such risk would be a jump by several suppliers to the 16Mb DRAM, in effect bypassing the 4Mb generation. As of early 1991, suppliers speak of such a move, but none has done so.

Changes in the Rules of the Game: 1Mb VRAMs and 4Mb SIMMs

In the DRAM business, many of the prior rules of the game (e.g., process technology, fab funding) will change with the move from 1Mb DRAM to 4Mb densities and above. A major change derives from system needs in terms of video applications, meaning more rapid growth in demand for video RAMs (VRAMs) and system size constraints, which translates into increased demand for single in-line memory modules (SIMMs). In response to client inquiries, this newsletter now shifts attention to two less familiar DRAM devices—the 256Kx4 VRAM and the 4Mbx9 SIMM—which will command more market attention over the long term.

256Kx4 VRAM: The 1991 Price Forecast Remains Consistent

Table 1 shows that participants in the fourth-quarter 1990 price survey originally expected the North American bookings price for 256Kx4 120ns VRAM ZIP in volume orders to range from $10.05 to $10.55 during the first quarter of 1991. Partly on this basis, SUIS forecast a price of $10.10 for the first quarter of 1991. The early results of the current price survey indicate that the actual first-quarter North American bookings price for this 1Mb VRAM will be on target with a price of $10.10 as forecast in December 1990.

Conservative Assumptions for 1Mb VRAM Price Forecasts

SUIS assumptions for 1Mb VRAM prices have been *conservative*. First, as of late 1990 and early 1991, the supplier base for devices such as 256Kx4 VRAM and 128Kx8 VRAM has been narrow. Dataquest expects the supplier base for VRAMs to widen over time. Until the supplier base does *in fact* widen, SUIS conservatively assumes moderate, not aggressive, short- and long-term rates of price decline. A second and related assumption is that some suppliers remain uncertain regarding their strategy for this market. The VRAM market to date seems more similar to the fast SRAM micromarkets than to the mainstream 1Mb DRAM and 4Mb DRAM markets. For example, not all suppliers will offer a full range of 1Mb VRAMs. Instead, depending on market demand patterns—some of which are being set during 1991—some suppliers will focus on 256Kx4 VRAM, some on 128Kx8 VRAM, some on both configurations, and others on wider configurations. Still other prospective suppliers could choose either to not enter the VRAM market or to enter but then depart.

The early results of the current survey indicate that the SUIS forecast on the North American bookings price for 256Kx4 VRAMs for the fourth quarter of 1991 will *decrease* to somewhat below—but still near—the $9.20 that was forecast in December 1990.

256Kx4 VRAM: A More Aggressive Long-Term Price Forecast

Table 1 also shows that Dataquest anticipates that the North American bookings price for the

256Kx4 VRAM as specified will decline to the $7.67 level for 1993 and to $6.85 for 1995. *Some* survey participants consistently project a price for the VRAM that is below the SUIS forecast. If the supplier base for this IC continues to expand, the price for the 256Kx4 VRAM is likely to decline at a more rapid pace and could reach just under $6 for 1995. The early results of the current price survey indicate that the long-range SUIS forecast on the North American bookings price for 256Kx4 VRAMs will likely be decreased, although the precise changes are not yet known.

Another Change in the Rules of the DRAM Game: More SIMMs

Dataquest sees continued growth in demand and supply of SIMMs. For system design engineers, SIMMs can help reduce system size. For procurement teams, SIMMs can serve as an effective tool for hedging against volatile price swings of different density DRAMs (e.g., 1Mb DRAMs versus 4Mb devices). For purposes of this newsletter, SUIS makes its preliminary projection of long-term pricing for 4Mbx9 80ns SIMMs.

4Mbx9 80ns SIMM: Conservative Assumptions

Table 1 shows that SUIS expects the North American bookings price for 4Mbx9 80ns SIMMs in volume orders to be $111.87 for 1993, decreasing to $86.05 for 1995. This product is not yet covered in the quarterly price survey, so no current price range is available.

The following assumptions guide this forecast. First, Dataquest firmly expects the SIMM supplier base to steadily expand over the long term. The number of suppliers is likely to increase. Also, *some* DRAM suppliers anticipate that SIMMs will represent a much larger share of their total DRAM revenue vis-à-vis past or current levels. Second, Dataquest makes a conservative cost model assumption in formulating the long-range forecast for 4Mb SIMM pricing. The 4Mbx9 SIMM cost model correlates directly with the conservative assumption on which the 4Mb DRAM price outlook is based. Should 4Mb DRAM prices decrease more rapidly than is now forecast, 4Mbx9 SIMM prices are also likely to fall at a faster rate than now expected.

DATAQUEST CONCLUSIONS AND RECOMMENDATIONS

This newsletter provides strategic insight into Dataquest's SUIS forecast of North American bookings prices of 1Mbx1 DRAMs, 4Mbx1 DRAMs, 256Kx4 VRAMs, and 4Mbx9 SIMMs for today (1991), tomorrow (1993), and the distant future (1995). It spells out the critical assumptions on supply/demand, cost models, FMVs, and suppliers' strategies on which SUIS bases the forecast. Under the current volatile market conditions, Dataquest makes the following recommendations.

Users should adjust to a new reality: Suppliers of 1Mb DRAMs will hold pricing power over the first half of 1991. Supply/demand patterns do not fully explain the current market shortage, which means that 1Mb DRAM prices should decrease over the second half of this year, perhaps abruptly.

The market should still plan for the 4Mb DRAM crossover during the second quarter of 1991. Early survey results indicate that prices for 4Mb DRAMs will continue to erode in line with prior expectations and that the current 1Mb DRAM shortage should *not* be a stabilizing factor on 4Mb DRAM pricing.

Users must coordinate closely with suppliers of devices such as 4Mb DRAMs, 1Mb VRAMs, and 4Mbx9 SIMMs over the long term in order to avoid scenarios such as today's spot shortage of 1Mb DRAMs. The rules of the DRAM games are changing, and users and suppliers must work together to adapt to the new market forces.

Ron Bohn
Mark Giudici
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Research Newsletter

NORTH AMERICAN MEGABIT-DENSITY DRAM PRICE OUTLOOK: TODAY (1991), TOMORROW (1993), AND THE DISTANT FUTURE (1995)

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An Early Look at the Updated SUIS 1991 Price Forecast for 1Mbx1 DRAM

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Dataquest assumes that current market conditions—which are marked by Japan-based price "leadership" in terms of upward pressure on 1Mb DRAM prices, with other suppliers opportunistically following—will hold true for the first half of 1991. Under this assumption, North American bookings prices for 1Mbx1 DRAMs could edge *upward* during the second quarter of 1991. The early results of the current price survey signal such a price trend, followed by a flat or slowly declining price profile for the second half of 1991. For the fourth quarter of 1991, the North American bookings price forecast for 1Mbx1 DRAMs will likely be increased to $4.25 versus the original December 1990 forecast of $3.79 for year-end 1991.

4Mbx1 DRAM: Demand to Pick Up and Prices to Decline during 1991

Table 1 shows that participants in the fourth-quarter 1990 price survey originally expected the North American bookings price for 4Mbx1 80ns DRAM SOJ in volume contract orders to range from $17 to $28 during the first quarter of 1991. On this basis, SUIS forecast a price of $19.80 for the first quarter of 1991.

No Major Change in the SUIS 1991 Price Forecast for 4Mbx1 DRAM

The early results of the current (February 1991) price survey indicate that the actual first-quarter North American bookings price for 4Mbx1 DRAMs will be quite close to $19.80, which was forecast in December 1990.

Dataquest's operating assumption for 4Mb DRAM is that first-tier Japanese suppliers, along with other worldwide suppliers, will ramp up production during 1991 and cut prices in order to win business in line with historical crossover experience. This assumption has proved sound. Current market conditions are marked by a strong move by Japan-based suppliers from the 1Mb DRAM to the 4Mb device with consequent downward pressure on 4Mb DRAM prices. Although upward pressure on 1Mb DRAM prices reduces the incentive for sharp 4Mb DRAM price declines, Dataquest still foresees a 4Mb DRAM crossover (4:1 unit/price ratio) for the second quarter of 1991.

In fact, Dataquest believes that capacity for 4Mb DRAM is likely to *exceed* demand for 1991; however, suppliers will avoid bringing all of the capacity on-line this year in order to avoid a 4Mb DRAM market glut. The early results of the survey also indicate that the SUIS forecast on the North American bookings price for 4Mbx1 DRAMs for the fourth quarter of 1991 will likely be increased in nondramatic fashion to a price in the $14.50 to $15.00 range versus the original December 1990 forecast of $14.00.

MEGABIT-DENSITY DRAM: THE LONG-RANGE ASSUMPTIONS

As noted, most of the assumptions for the long-range DRAM price forecast have *not* changed dramatically since December 1990. Clearly, one assumption—that non-Japanese suppliers will continue to lower prices while Japan-based suppliers depart any given DRAM market segment—has been controverted for the short term.

The following key assumptions guide the SUIS long-range megabit-density DRAM price forecast for North America. First, global DRAM capacity will exceed market DRAM demand during the first half of this decade. A second assumption is that the foreign market value (FMV) system of pricing either will terminate during mid-1991 or will be replaced by a pricing system that assures low-priced DRAMs for North American users. Third, cost-based price reductions will assure lower pricing for 4Mb DRAMs and competitive pricing for 1Mb devices. A fourth assumption—which Dataquest still believes will hold true after 1991—is that non-Japanese suppliers will again continue to lower megabit-density DRAM prices to take market share as leading-edge Japan-based suppliers migrate to next-generation products.

During February and March 1991, Dataquest Semiconductor Industry Service (SIS) and SUIS analysts in San Jose, California, will work closely with SIS DRAM analysts in Tokyo and London to reassess these assumptions and the concomitant SUIS DRAM price forecast.

1Mbx1 80ns DRAM: The Critical Assumptions

Under these assumptions and as shown in Table 1, Dataquest anticipates that the North American bookings price for 1Mbx1 80ns DRAM SOJ in volume orders will be $3.40 for 1993 and reach bottom at a price of $3.20 for 1995.

In terms of the four assumptions, these points should be stressed. First, analysts in Dataquest's Semiconductor Equipment, Manufacturing, and Materials Service (SEMMS) and SIS Memory recently analyzed the combined worldwide demand for 1Mb DRAMs and 4Mb DRAMs against the megabit-density DRAM fab capacity outlook for the 1990 to 1994 time frame. This analysis *conservatively* estimates that megabit-density DRAM capacity utilization should reach its highest level, 77 percent, during 1991 and decline to 74 percent for 1994. Succinctly, megabit-density DRAM capacity should exceed demand over the long term, barring a major and unexpected supplier reduction of production capability.

Second, a 1Mb DRAM cost model developed by SUIS and SEMMS analysts reveals that suppliers will be able to profitably manufacture this device at the prices specified in the SUIS forecast (i.e., $3.40 for 1993 and $3.20 for 1995). Next, Dataquest anticipates the demise of the FMV system—but the remaining 1Mb DRAM suppliers will be non-Japanese and thus will be unaffected even if FMVs do survive in some form.

An Early Look at the Updated Long-Range Forecast for 1Mbx1 DRAM

Because non-Japanese suppliers opportunistically raised 1Mbx1 80ns DRAM prices early in 1991, Dataquest realizes that the anticipated

long-term decline in 1Mb DRAM pricing is likely to start at a higher 1991 level than the original 1991 forecast price of $4.02. Suppliers may aim for continued *upward* pressure on pricing, but long-term market forces should dictate otherwise. During March 1991, the North American bookings price forecast likely will be increased for 1993 to a price of about $3.80 and for 1995 to a price range of $3.40 to $3.60.

4Mbx1 80ns DRAM: The Forecast Remains Consistent

In line with the previously mentioned four assumptions and supporting analysis, as shown in Table 1, Dataquest anticipates that the North American bookings price for the 4Mbx1 80ns DRAM SOJ in volume orders will be $11.30 for 1993 and $8.50 for 1995.

In terms of the four assumptions, the following points are stressed. First, as noted, megabit-density DRAM capacity should exceed demand over the long term, barring an unanticipated cutback in capacity. Next, Dataquest's 4Mb DRAM cost model conservatively shows that suppliers will be able to profitably manufacture this device at the price levels indicated in the long-range SUIS forecast. Third, the anticipated termination of the FMV system—or its replacement by a less onerous pricing scheme—would permit pricing to decline at an even more rapid rate than projected by the SUIS forecast.

A volatile element of risk always lurks in the DRAM marketplace. Regarding the long-range 4Mb DRAM market/price outlook, one such risk would be a jump by several suppliers to the 16Mb DRAM, in effect bypassing the 4Mb generation. As of early 1991, suppliers speak of such a move, but none has done so.

Changes in the Rules of the Game: 1Mb VRAMs and 4Mb SIMMs

In the DRAM business, many of the prior rules of the game (e.g., process technology, fab funding) will change with the move from 1Mb DRAM to 4Mb densities and above. A major change derives from system needs in terms of video applications, meaning more rapid growth in demand for video RAMs (VRAMs) and system size constraints, which translates into increased demand for single in-line memory modules (SIMMs). In response to client inquiries, this newsletter now shifts attention to two less familiar DRAM devices—the 256Kx4 VRAM and the 4Mbx9 SIMM—which will command more market attention over the long term.

256Kx4 VRAM: The 1991 Price Forecast Remains Consistent

Table 1 shows that participants in the fourth-quarter 1990 price survey originally expected the North American bookings price for 256Kx4 120ns VRAM ZIP in volume orders to range from $10.05 to $10.55 during the first quarter of 1991. Partly on this basis, SUIS forecast a price of $10.10 for the first quarter of 1991. The early results of the current price survey indicate that the actual first-quarter North American bookings price for this 1Mb VRAM will be on target with a price of $10.10 as forecast in December 1990.

Conservative Assumptions for 1Mb VRAM Price Forecasts

SUIS assumptions for 1Mb VRAM prices have been *conservative*. First, as of late 1990 and early 1991, the supplier base for devices such as 256Kx4 VRAM and 128Kx8 VRAM has been narrow. Dataquest expects the supplier base for VRAMs to widen over time. Until the supplier base does *in fact* widen, SUIS conservatively assumes moderate, not aggressive, short- and long-term rates of price decline. A second and related assumption is that some suppliers remain uncertain regarding their strategy for this market. The VRAM market to date seems more similar to the fast SRAM micromarkets than to the mainstream 1Mb DRAM and 4Mb DRAM markets. For example, not all suppliers will offer a full range of 1Mb VRAMs. Instead, depending on market demand patterns—some of which are being set during 1991—some suppliers will focus on 256Kx4 VRAM, some on 128Kx8 VRAM, some on both configurations, and others on wider configurations. Still other prospective suppliers could choose either to not enter the VRAM market or to enter but then depart.

The early results of the current survey indicate that the SUIS forecast on the North American bookings price for 256Kx4 VRAMs for the fourth quarter of 1991 will *decrease* to somewhat below—but still near—the $9.20 that was forecast in December 1990.

256Kx4 VRAM: A More Aggressive Long-Term Price Forecast

Table 1 also shows that Dataquest anticipates that the North American bookings price for the

256Kx4 VRAM as specified will decline to the $7.67 level for 1993 and to $6.85 for 1995. *Some* survey participants consistently project a price for the VRAM that is below the SUIS forecast. If the supplier base for this IC continues to expand, the price for the 256Kx4 VRAM is likely to decline at a more rapid pace and could reach just under $6 for 1995. The early results of the current price survey indicate that the long-range SUIS forecast on the North American bookings price for 256Kx4 VRAMs will likely be decreased, although the precise changes are not yet known.

Another Change in the Rules of the DRAM Game: More SIMMs

Dataquest sees continued growth in demand and supply of SIMMs. For system design engineers, SIMMs can help reduce system size. For procurement teams, SIMMs can serve as an effective tool for hedging against volatile price swings of different density DRAMs (e.g., 1Mb DRAMs versus 4Mb devices). For purposes of this newsletter, SUIS makes its preliminary projection of long-term pricing for 4Mbx9 80ns SIMMs.

4Mbx9 80ns SIMM: Conservative Assumptions

Table 1 shows that SUIS expects the North American bookings price for 4Mbx9 80ns SIMMs in volume orders to be $111.87 for 1993, decreasing to $86.05 for 1995. This product is not yet covered in the quarterly price survey, so no current price range is available.

The following assumptions guide this forecast. First, Dataquest firmly expects the SIMM supplier base to steadily expand over the long term. The number of suppliers is likely to increase. Also, *some* DRAM suppliers anticipate that SIMMs will represent a much larger share of their total DRAM revenue vis-à-vis past or current levels. Second, Dataquest makes a conservative cost model assumption in formulating the long-range forecast for 4Mb SIMM pricing. The 4Mbx9 SIMM cost model correlates directly with the conservative assumption on which the 4Mb DRAM price outlook is based. Should 4Mb DRAM prices decrease more rapidly than is now forecast, 4Mbx9 SIMM prices are also likely to fall at a faster rate than now expected.

DATAQUEST CONCLUSIONS AND RECOMMENDATIONS

This newsletter provides strategic insight into Dataquest's SUIS forecast of North American bookings prices of 1Mbx1 DRAMs, 4Mbx1 DRAMs, 256Kx4 VRAMs, and 4Mbx9 SIMMs for today (1991), tomorrow (1993), and the distant future (1995). It spells out the critical assumptions on supply/demand, cost models, FMVs, and suppliers' strategies on which SUIS bases the forecast. Under the current volatile market conditions, Dataquest makes the following recommendations.

Users should adjust to a new reality: Suppliers of 1Mb DRAMs will hold pricing power over the first half of 1991. Supply/demand patterns do not fully explain the current market shortage, which means that 1Mb DRAM prices should decrease over the second half of this year, perhaps abruptly.

The market should still plan for the 4Mb DRAM crossover during the second quarter of 1991. Early survey results indicate that prices for 4Mb DRAMs will continue to erode in line with prior expectations and that the current 1Mb DRAM shortage should *not* be a stabilizing factor on 4Mb DRAM pricing.

Users must coordinate closely with suppliers of devices such as 4Mb DRAMs, 1Mb VRAMs, and 4Mbx9 SIMMs over the long term in order to avoid scenarios such as today's spot shortage of 1Mb DRAMs. The rules of the DRAM games are changing, and users and suppliers must work together to adapt to the new market forces.

Ron Bohn
Mark Giudici
Sam Young

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Research Newsletter

A GLIMPSE AT FUTURE 64Mb DRAM TECHNOLOGIES

SUMMARY

The IEEE International Solid State Circuits Conference (ISSCC) held every February is a good barometer of future trends in device technology and applications. The 1991 conference featured several experimental versions of 64Mb DRAM devices. Although these devices are at least five years away from volume production, they provide a glimpse of future high-volume process technologies. In this newsletter, Dataquest analyzes key implications of these prototype 64Mb DRAM technologies for the semiconductor equipment, manufacturing, and materials industries in the years ahead.

64Mb DRAM TRENDS

Table 1 illustrates the key features of experimental 64Mb DRAMs unveiled by Fujitsu, Matsushita, Mitsubishi, and Toshiba at ISSCC 1991. Dataquest believes that DRAM companies will continue to push optical lithography to 0.4-micron geometries for the 64Mb DRAM. All of the 64Mb DRAM devices were characterized by multiple levels of poly/polycide and double-level interconnect technology. Gate and capacitor dielectric thickness values are expected to be in the 50- to 100-angstrom range. All four companies used variations of a stacked-capacitor cell scheme.

U.S.-based DRAM manufacturers have traditionally favored a trench capacitor-based memory cell. In contrast, Japan-based DRAM companies favor the simple stacked capacitor scheme over the more complex trench capacitor scheme with its attendant problems of trench etch damage and trench sidewall leakage currents. Toshiba appears to have the most aggressive 64Mb DRAM design. Toshiba's use of excimer laser lithography, together with the asymmetric stacked trench capacitor design, yields the smallest cell size (0.9 x 1.7 um^2) and the fastest speed (33ns).

LITHOGRAPHY TRENDS

All of these 64Mb DRAMs were fabricated with 0.4-micron design rules using optical lithography tools. Fujitsu and Mitsubishi opted for i-line steppers and Matsushita and Toshiba chose excimer laser steppers. The astonishing progress of optical lithography in combination with technology such as phase-shift masks pushes X-ray lithography even further out into the future. Semiconductor manufacturers have a huge installed base of investment and experience in optical lithography that they are reluctant to throw away. Japan-based DRAM companies are racing to convert development results in phase-shift masks into commercially useful technologies to extend the lifetime of optical lithography tools through the 64Mb DRAM generation and potentially to the 256Mb DRAM generation.

Issues such as global and local planarization, depth of focus, wafer flatness, and intrafield focus on large fields may yet force semiconductor manufacturers to eventually migrate to X-ray lithography, which has far higher depth-of-focus latitude. However, X-ray lithography has to contend with the challenges of 1X mask technology. The prohibitive costs associated with synchrotron orbital rings (SORs) for X-ray lithography, together with the technical challenges of 1X mask materials, mask fabrication, inspection, and repair, have prompted 64Mb DRAM manufacturers to stay with the evolutionary, incremental advantages of optical lithography.

Dataquest believes that the extension of optical lithography using i-line and excimer laser steppers in combination with phase-shift mask technology may enable the 64Mb DRAM device to follow the traditional decrease in the cost-per-bit curve. Given the extension of optical lithography to the 64Mb DRAM generation, lithography equipment companies need to focus on high-throughput, wide-field steppers that can offer better productivity in

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Company	Minimum Feature size (Microns)	Lithography	Poly/ Polycide Levels	Metal Levels	Gate Oxide Thickness (Angstroms)	Capacitor Type	Cell Size um x um	Chip Size mm x mm	Access Time (ns)
Fujitsu	0.4	I-line Phase-shift	4	2	NA	Double-fin stacked	1.0 x 1.8	11.27 x 19.94	40
Matsushita	0.4	KrF excimer laser	3	2	120	Tunnel stacked	1.0 x 2.0	10.85 x 21.60	50
Mitsubishi	0.4	I-line	3	2	120	Dual-cellplate stacked	1.0 x 1.7	12.5 x 18.7	45
Toshiba	0.4	KrF excimer laser	4	2	50	Asymmetric stack trench	0.9 x 1.7	9.22 x 19.13	33

NA = Not available
Source: ISSCC/Dataquest (March 1991)

spite of higher average selling prices (ASPs). Significant opportunities exist for companies to target new business areas such as i-line and excimer laser photoresists, ancillary lithography chemicals, phase-shift masks, mask coatings, mask etch, and mask inspection/repair equipment.

ETCH/CLEAN TRENDS

Dataquest estimates that the number of mask/etch levels will almost double between the 1Mb DRAM (16 levels) and the 64Mb DRAM (about 30 levels). In fact, the number of wet clean/dry etch processes will exceed the number of masking processes because of the addition of more elaborate wet/dry vapor cleans as well as blanket (maskless) etchback steps such as trench refill etchback, LDD spacer etchback, and contact/via plug etchback, intermetal planarization etchback. The unique requirements of the 3-D stacked or trench 64Mb DRAM capacitor offer extraordinary challenges to the ability of wet chemical/vapor phase cleans to truly "clean" the wafer without adding additional particles and contamination.

Dry etch equipment has to offer extremely high selectivities, uniformity, critical dimension (CD) control across 8-inch wafers, and low ionization damage in order to etch 0.4-micron gate features. A variety of plasma sources are being considered in order to handle the stringent processing requirements of 64Mb DRAM dry etch processes. New gas chemistries such as bromine, NF_3, and other non-fluorocarbon processes offer significant processing challenges to gas suppliers and dry etch equipment companies.

DEPOSITION TRENDS

DRAM manufacturers have already switched from single-level metal to double-level metal for the 16Mb DRAM generation. The challenges associated with metal step coverage dramatically increase as contact and via dimensions approach the 0.4-micron level. CVD titanium nitride, CVD tungsten, and CVD polysilicon are being examined as viable candidates for contact plug processes. Meanwhile, the efforts to improve the step coverage of sputtered aluminum and refractory barrier metals such as titanium nitride continue vigorously. Many opportunities exist for materials companies to develop new sputtering materials and CVD source materials for interconnect applications in the 64Mb DRAM generation.

The polysilicon CVD equipment market is expected to grow dramatically over the next five years in order to cater to mushrooming applications for high-quality polysilicon films at multiple levels in the 64Mb DRAM process. For example, Toshiba is reportedly planning to use four levels of poly/polycide films in its 64Mb DRAM process. Stacked capacitors and trench capacitors will use multiple poly depositions to achieve the desired cell capacitor area. Many new types of poly CVD equipment such as improved vertical LPCVD poly tubes and integrated cluster tools incorporating rapid thermal oxidation/nitridation (RTO/RTN), low-pressure poly CVD, and low-pressure tungsten silicide CVD may emerge in response to these applications.

Interlayer dielectrics between poly and first-level metal and intermetal dielectrics between metal levels need to be highly planarized because of metal step coverage, bridging, depth of focus, resist uniformity, and over-etch considerations in 64Mb DRAM wafers. In addition to the familiar spin-on-glass planarization schemes, Dataquest believes that 64Mb DRAM companies will examine other global planarization techniques such as biased electron cyclotron resonance (ECR) CVD techniques, chemical-mechanical polishing, TEOS-based plasma-enhanced CVD oxide fill/etchback, and in-situ deposition/low-temperature reflow oxides. Tungsten, poly, aluminum, and copper CVD plugs are being explored for contact and via fills. The choice of the optimum planarization and back-end interconnect process will have profound effects on 64Mb DRAM speeds, yield, and reliability.

DIFFUSION/IMPLANT TRENDS

Vertical diffusion and LPCVD tubes will probably be used for all diffusion and oxidation processes on 8-inch 64Mb DRAM wafers. Vertical furnaces offer high-quality thin oxides, thermal nitride, and polysilicon. Vertical tubes are also more compatible with the automation and film uniformity requirements of 8-inch fabs. Load-locked vertical diffusion furnaces may be used to implement tube-to-tube transfer between oxidation, nitridation, and LPCVD poly/nitride processes.

The number of implant steps continues to rise significantly in order to precisely control the electrical behavior of 0.4-micron geometry transistors. In addition to the traditional requirements for dose uniformity and low particulates across 8-inch wafers, continuously variable tilt angles and

parallel beam scanning are expected to become the norm for implanting 3-D 64Mb DRAM device structures.

PROCESS CONTROL TRENDS

CD and wafer-inspection equipment companies will enjoy major business opportunities at the 64Mb DRAM generation. The process of analyzing variations in critical dimensions at the 0.4-micron level across 8-inch wafers is a major challenge. The move toward integrated processes will lead to the loss of critical intermediate CD and wafer-condition information. Some equipment companies are evaluating the incorporation of in-situ metrology tools such as CD SEM measurement chambers and particle-detection/wafer-inspection chambers onto cluster tool platforms.

Thin films and resistivity measurement systems will face similar challenges in measuring thin oxides and shallow doped junctions. Electrical measurement techniques may be used to augment physical thin-film thickness and resistivity measurements.

DATAQUEST CONCLUSIONS

Dataquest believes that DRAM process technology will continue its evolutionary progress between generations. The extension of optical lithography and the stacked capacitor cell structure to the 64Mb DRAM devices are aimed at keeping the DRAM cost per bit on its historical decline. Dramatic increases in the complexity of lithography, interconnect, planarization, dry etch, and process-control processes may push the price tag of a 8-inch high-volume 64Mb DRAM fab to well over $600 million. At the 0.4-micron 64Mb DRAM level, interconnect process complexity and performance will be the limiting factors that control the device speed and cost per bit.

Sam Young
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Research Newsletter

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Research Newsletter

MERCHANT DRAM SUPPLIERS: ANOTHER SHAKEOUT COMING?

The prices of 1Mb and 4Mb DRAMs have been falling steadily. In the fourth quarter of 1989, the worldwide average selling price (ASP) of a 1Mb DRAM was $9.45. Today, the price of a 1Mb DRAM ranges from $4.30 to $5.00. In the fourth quarter of 1989, the ASP of a 4Mb DRAM was $87.78. Today, the price of a 4Mb DRAM ranges from $18.00 to $23.00.

Part of this decline is normal. Learning-curve price declines are a part of each generation of DRAMs. These declines stimulate demand and allow buyers to economically cross over to the next generation of DRAMs. However, in the fourth quarter of 1990, 1Mb DRAM price declines seemed much sharper than would be expected from learning-curve experience only. Prices were squeezing profits. Japanese DRAM manufacturers responded with production cutbacks of 1Mb DRAMs.

These recent and larger-than-expected 1Mb DRAM price declines are due to a simple economic fact: oversupply. Based on our analysis of existing merchant capacity and planned, publicly announced capacity additions, Dataquest believes that there is an oversupply of 1Mb and 4Mb DRAMs. We believe that this condition is likely to continue.

DRAM SUPPLY AND DEMAND

Dataquest maintains a worldwide fab database that contains wafer start capacity for individual semiconductor companies. From our fab database we determine current DRAM capacity in wafer starts and add to it all the announced plans for building future DRAM capacity. This DRAM wafer start capacity is converted to DRAM unit capacity by applying the set of assumptions for die size and yield shown in Table 1. Unit DRAM capacity is then compared with Dataquest's forecast of DRAM demand to determine if there is or will be an imbalance of DRAM demand and supply.

We believe that our capacity assumptions are on the conservative side. For example, all fab lines that produce non-DRAM devices in addition to DRAMs were excluded from the analysis. If these fabs and some appropriate fraction of their capacity were included in the analysis, the resulting DRAM capacity numbers would be much higher.

Many fabs in our database are listed as capable of producing either 1Mb or 4Mb DRAMs. Thus, this study is based on an aggregate analysis of 1Mb and 4Mb DRAM capacity. In this newsletter, we provide three scenarios regarding the mix of fabs capable of either 1Mb or 4Mb DRAM production. These scenarios reflect assumptions for low

TABLE 1
Assumptions for DRAM Die Size, Probe Yields, and Good Die Per Wafer

	Die Size (mm^2)	Probe Yield (%)	Good Die per 6-Inch Wafer
1Mb DRAM	40	79	293
4Mb DRAM	96	48	66
4Mb DRAM (Shrink)	71	65	128

Source: Dataquest (March 1991)

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capacity, high capacity, and intermediate capacity for 1Mb and 4Mb DRAMs.

The low-capacity scenario assumes that all 1Mb DRAM fabs that are also capable of 4Mb DRAM production will indeed shift their production to 4Mb DRAMs. This scenario is low capacity because fewer 4Mb DRAM die can be fabricated from a wafer than 1Mb DRAMs. (The die for 4Mb DRAMs are larger than the die for 1Mb DRAMs.)

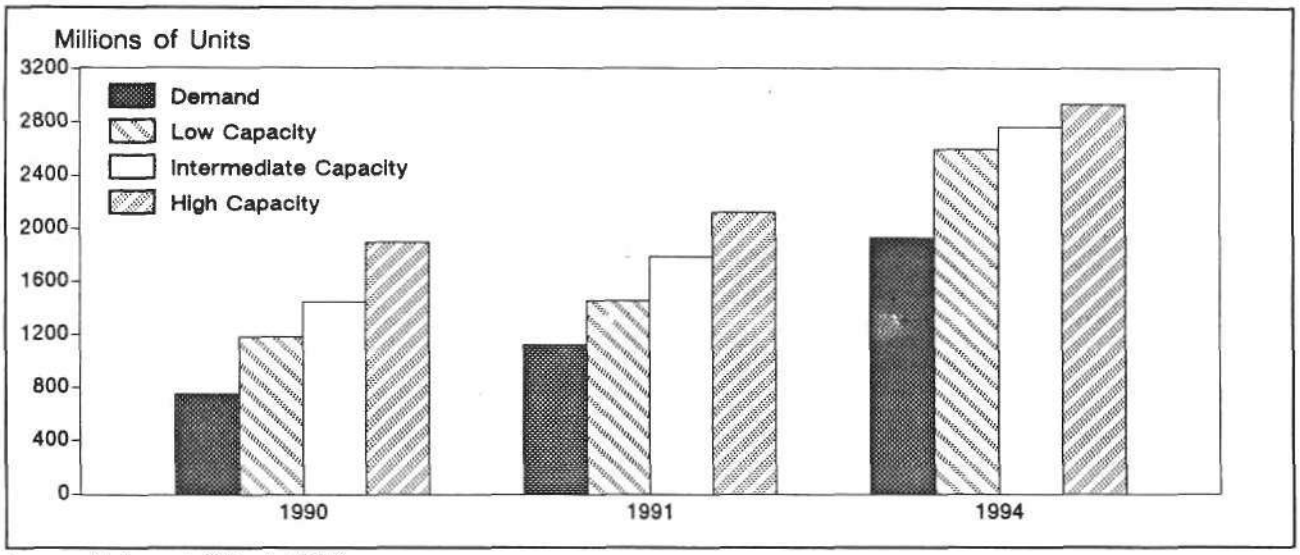
The high-capacity scenario assumes that none of the fabs listed as capable of either 1Mb or 4Mb DRAMs will shift production to 4Mb DRAMs. This scenario is high capacity because more 1Mb DRAM die than 4Mb DRAM die can be fabricated from a wafer.

The intermediate-capacity scenario assumes that 50 percent of the fabs listed as capable of producing both 1Mb and 4Mb DRAMs will actually shift production to 4Mb DRAMs.

DRAM demand and our estimated DRAM capacity for the three scenarios are shown in Figure 1. What is striking about this figure is that the combined capacity of 1Mb and 4Mb DRAMs—under all three of our capacity scenarios—exceeds the projected combined demand for these devices by a substantial margin. For example, in 1994, the low-capacity scenario projects a capacity of slightly over 2,500 million units and a demand of just under 2,000 million units, an excess of over 25 percent.

Table 2 evaluates the supply-and-demand estimates in Figure 1 in terms of percentages. For example, in 1994, demand will be only 66 percent of the potential supply under the high-capacity scenario and 74 percent of supply under the low-capacity scenario.

FIGURE 1
Estimated Aggregate of 1Mb and 4Mb DRAM Supply and Demand



Source: Dataquest (March 1991)

TABLE 2
Estimated Merchant Demand as a Percentage of Worldwide Merchant Capacity for 1Mb and 4Mb DRAMs Combined

	Low Capacity	Intermediate Capacity	High Capacity
1990	63	52	40
1991	77	63	53
1994	74	70	66

Source: Dataquest (March 1991)

DATAQUEST CONCLUSIONS

It should be emphasized that this large DRAM capacity has to be utilized for oversupply to occur. In the short term, DRAM producers could very well choose not to use their full-production capacity. This happened in fall 1990 when Japanese producers announced cutbacks in production of 1Mb DRAMs.

A longer-term strategy to reduce overcapacity is to switch some DRAM capacity to other products, such as SRAMs or ASICs. An example of this strategy would be Motorola's recent announcement that its MOS 11 fab in Oak Hill, Texas, will be used to produce SRAMs rather than 4Mb DRAMs as originally planned. A third alternative strategy is that a DRAM fab facing overcapacity could aggressively pursue foundry relationships to fill unused capacity.

In the early and mid-1980s the industry faced a similar, although not identical, situation. There were too many DRAM manufacturers, and oversupply resulted. Many DRAM producers decided to leave the DRAM business for what they hoped were more profitable product lines. Capital spending fell more sharply than ever before. Equipment companies folded, merged, restructured, laid off staff, and some even cut back on R&D.

Since the mid-1980s, the industry has been much more circumspect about adding capacity. The growth rate of capital spending was much less in the second half of the 1980s than in the first half. Inventories, because of just-in-time deliveries and closer supplier/vendor relationships, are much better managed than in 1985. Since the shakeout in the mid-1980s, the industry has matured.

However, new DRAM players have emerged since the mid-1980s. These companies (Motorola, Asia/Pacific companies, and second-tier Japanese companies) have added capacity in order to gain market share. The capacity from the new, plus the capacity from the established players, today add up to overcapacity. Clearly, the industry faces a challenge: how to manage overcapacity without the corrective of another shakeout.

Ione Ishii

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Research Newsletter

MERCHANT DRAM SUPPLIERS: ANOTHER SHAKEOUT COMING?

The prices of 1Mb and 4Mb DRAMs have been falling steadily. In the fourth quarter of 1989, the worldwide average selling price (ASP) of a 1Mb DRAM was $9.45. Today, the price of a 1Mb DRAM ranges from $4.30 to $5.00. In the fourth quarter of 1989, the ASP of a 4Mb DRAM was $87.78. Today, the price of a 4Mb DRAM ranges from $18.00 to $23.00.

Part of this decline is normal. Learning-curve price declines are a part of each generation of DRAMs. These declines stimulate demand and allow buyers to economically cross over to the next generation of DRAMs. However, in the fourth quarter of 1990, 1Mb DRAM price declines seemed much sharper than would be expected from learning-curve experience only. Prices were squeezing profits. Japanese DRAM manufacturers responded with production cutbacks of 1Mb DRAMs.

These recent and larger-than-expected 1Mb DRAM price declines are due to a simple economic fact: oversupply. Based on our analysis of existing merchant capacity and planned, publicly announced capacity additions, Dataquest believes that there is an oversupply of 1Mb and 4Mb DRAMs. We believe that this condition is likely to continue.

DRAM SUPPLY AND DEMAND

Dataquest maintains a worldwide fab database that contains wafer start capacity for individual semiconductor companies. From our fab database we determine current DRAM capacity in wafer starts and add to it all the announced plans for building future DRAM capacity. This DRAM wafer start capacity is converted to DRAM unit capacity by applying the set of assumptions for die size and yield shown in Table 1. Unit DRAM capacity is then compared with Dataquest's forecast of DRAM demand to determine if there is or will be an imbalance of DRAM demand and supply.

We believe that our capacity assumptions are on the conservative side. For example, all fab lines that produce non-DRAM devices in addition to DRAMs were excluded from the analysis. If these fabs and some appropriate fraction of their capacity were included in the analysis, the resulting DRAM capacity numbers would be much higher.

Many fabs in our database are listed as capable of producing either 1Mb or 4Mb DRAMs. Thus, this study is based on an aggregate analysis of 1Mb and 4Mb DRAM capacity. In this newsletter, we provide three scenarios regarding the mix of fabs capable of either 1Mb or 4Mb DRAM production. These scenarios reflect assumptions for low

TABLE 1
Assumptions for DRAM Die Size, Probe Yields, and Good Die Per Wafer

	Die Size (mm^2)	Probe Yield (%)	Good Die per 6-Inch Wafer
1Mb DRAM	40	79	293
4Mb DRAM	96	48	66
4Mb DRAM (Shrink)	71	65	128

Source: Dataquest (March 1991)

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capacity, high capacity, and intermediate capacity for 1Mb and 4Mb DRAMs.

The low-capacity scenario assumes that all 1Mb DRAM fabs that are also capable of 4Mb DRAM production will indeed shift their production to 4Mb DRAMs. This scenario is low capacity because fewer 4Mb DRAM die can be fabricated from a wafer than 1Mb DRAMs. (The die for 4Mb DRAMs are larger than the die for 1Mb DRAMs.)

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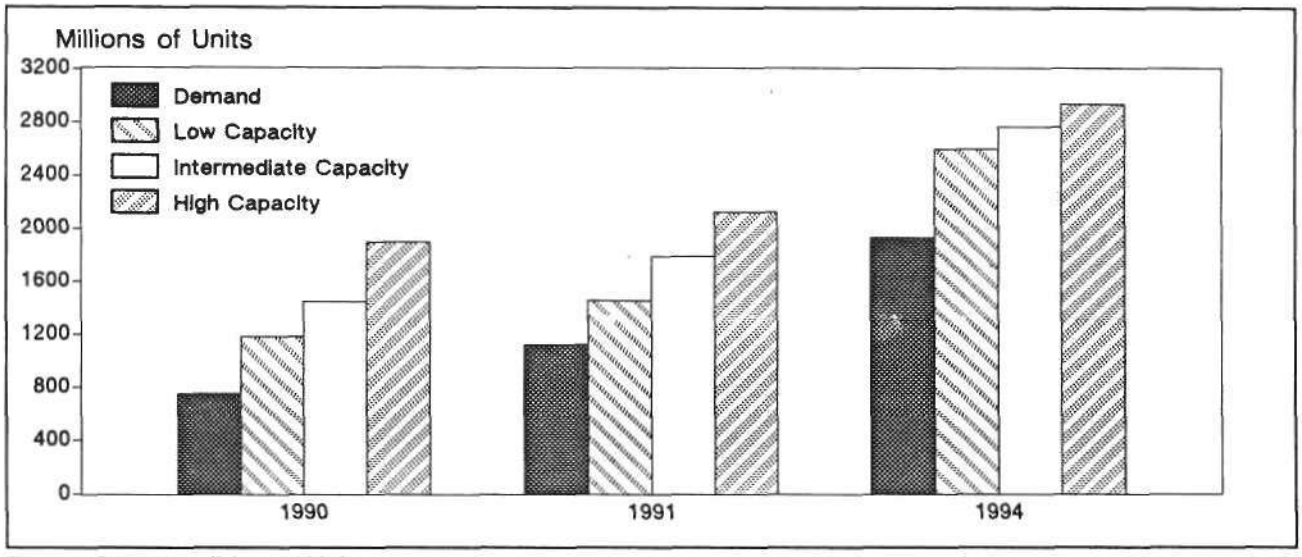

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Research *Bulletin*

ENGINEERING SAMPLING OF 4Mb SLOW SRAMs

SUMMARY

Hitachi and NEC have announced shipments of engineering samples of a 4Mb slow SRAM starting in the March/April time frame. During December 1990, Sony Europe commented that it would have engineering samples available for the 4Mb SRAM by the fourth quarter of 1991. Whereas most companies are not expected to ship volume quantities until sometime in 1992, Dataquest forecasts that an estimated 100,000 units of 4Mb slow SRAMs will be shipped during 1991 and that shipments of this slow SRAM density will peak in 1996 at the 111.2 million unit level.

In this bulletin, Dataquest looks briefly at various technology, packaging, and application aspects of the 4Mb slow SRAM. We examine several application opportunities for 4Mb slow SRAM suppliers. We also discuss which companies may announce engineering samples of this device during 1991.

ASPECTS OF THE 4Mb SLOW SRAM

4Mb Slow SRAM Specifications

Both Hitachi and NEC have similar device specifications for their engineering samples of the 4Mb slow SRAM. The NEC chip size is approximately 7.9x17.8mm^2, and the cell size is 3.2x5.8um^2. The device is organized in 512Kx8. Other specs are listed as follows:

- Speeds—55, 70, 85, 100ns
- Low power—operation: 75mW/MHz, typical; standby: 10 microwatts
- Capability of battery backup operation
- Single 5-volt supply
- Completely static memory; no clock or timing strobe required
- CMOS technology
- 0.5-micron design rule
- TTL-compatible I/O

Packaging Details

The die sizes range from 116 to 140mm^2, thereby requiring a 32-pin, 600-mil DIP or a 525-mil SOG package. NEC's device is also available in a 32-pin, 400-mil TSOP package. All available packages meet JEDEC standards.

Applications

The arrival of the 4Mb slow SRAM is perhaps most welcomed by the design engineer who focuses on hand-held digitized consumer products. We believe that the new density will be designed into portable CD players such as Sony's Discman, minicameras, and personal organizers.

Midrange applications include memory modules, supercomputers, point of sales (POS) systems, and personal computers. Long-range applications may evolve in the industrial segment (for products such as controllers) and the telecommunications area (for satellite usage).

Dataquest's most recent applications forecast presents new business opportunities for companies competing in the 4Mb slow SRAM area. Table 1 presents the estimated 1991 and 1995 worldwide electronic equipment production forecast.

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SIS Newsletters 1991 Memory

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TABLE 1
Estimated Worldwide Electronic Equipment Production (Millions of Dollars)

	1991	1995
Data Processing	252.9	360.6
Communications	104.9	144.8
Industrial	98.4	130.1
Consumer	143.3	187.6
Military/Aerospace	85.1	105.1
Transportation	16.9	25.9
Total	701.5	954.1

Source: Dataquest (April 1991)

SLOW SRAM PLAYERS: TODAY AND TOMORROW

Table 2 is based on the most recent quarterly memory shipment survey for 1990. This table presents the top 10 suppliers in the slow SRAM market, ranked according to percentage of market share by units.

TABLE 2
Preliminary 1990 Slow SRAM Unit Market Share (Percentage)

Rank	Company	Market Share (%)
1	Hitachi	16.6
2	NEC	11.6
3	Sony	11.2
4	Toshiba	10.2
5	Sharp	9.9
6	Fujitsu	7.3
7	Sanyo	6.2
8	Mitsubishi	5.7
9	Hyundai	5.2
10	Matsushita	2.6

Source: Dataquest (April 1991)

During 1990, a number of slow SRAM manufacturers elected to leave the slow SRAM business because of declining profits, the required capital investments for upgrades, the perception that prices would continue to erode, and strong competition from the large number of manufacturers competing in this market. Companies that left the market in 1990 include AMD, National Semiconductor, Matra MHS, and VLSI Technology. It is worth noting that in the past few weeks, National Semiconductor reentered the slow SRAM market by selling SRAMs manufactured by Sharp. National has also been selling NEC SRAMs. It is Dataquest's belief that more slow SRAM companies will withdraw from this highly competitive market in the next few years.

DATAQUEST CONCLUSIONS AND RECOMMENDATIONS

Dataquest projects that other slow SRAM vendors that have been successful in providing engineering samples for 16Mb DRAMs will enter the 4Mb area. To date, companies that have been supplying 16Mb DRAM samples are Fujitsu, Hitachi, Mitsubishi, NEC, Samsung, Siemens, Texas Instruments, and Toshiba. The 4Mb slow SRAM and the 16Mb DRAM have similar die sizes and number of transistors, thereby requiring manufacturing facilities with similar specifications such as cleanness, defect density, line geometries, process complexities, and equipment.

As previously mentioned, it is likely that Sony, which does not manufacture DRAMs, will be sampling the 4Mb slow SRAM before the end of 1991. We also anticipate that, throughout the life cycle of the 4Mb slow SRAM, additional applications will be developed in all six segments listed in Table 1.

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Research *Newsletter*

SIS MEMORY QUARTERLY NEW PRODUCTS NEWSLETTER

This newsletter contains a synopsis of memory product news events gathered from the trade press and company releases during the first quarter of 1991. This newsletter is meant to be used as a reference guide of new products for competitive analysis, monitoring technology trends, and tracking future developments and improvements. Dataquest assumes no responsibility for the accuracy of the contents.

Table 1 shows the new products announced during the first quarter of 1991.

DRAM DEVELOPMENTS

Fujitsu

Fujitsu announced it will ship multibit 4Mb DRAMs by the end of 1991. The 256Kx16 memory device functions the same as do 16 256K DRAMs.

Fujitsu announced it will start pilot 16Mb DRAM production using 8-inch wafers at its Mei prefecture plant during the second half

TABLE 1
New Memory Products—First Quarter 1991

Company	Density/Description	Speed
DRAM Developments		
Fujitsu	Multibit 4Mb DRAM	
	16Mb	
	64Mb prototype	40ns
Hitachi	4Mb DRAM	
Hitachi/TI	16Mb SOJ package design	
Intel	4Mb DRAM	80ns
Matsushita	64Mb prototype	50ns
Mitsubishi	64Mb prototype	45ns
Motorola	4Mb DRAM	
NMB	Zero-wait state	53, 60ns
NEC	16Mb	70, 80, 100ns
Siemens	16Mb	60, 80ns
Toshiba	64Mb prototype	33ns
	1Mb, TSOP package	60, 70, 80, 100ns
	512Kx8, 4Mb DRAM	70, 80, 100ns
	4Mb	60ns

(Continued)

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TABLE 1 (Continued)
New Memory Products—First Quarter 1991

Company	Density/Description	Speed
SRAM Developments		
Cypress	64K, BiCMOS	10ns
Fujitsu	4Mb 1Mb	7, 10ns 15ns
Hitachi	256K SRAM 4Mb	15ns
IBM	512K SRAM	4ns
Intel	1Mb SRAM	100ns
Mitsubishi	256K	10ns
Motorola	256K, synchronous 256K, 3 new versions	12ns 25, 35ns
NEC	4Mb	60, 70ns
Paradigm	256K CMOS 128Kx8 1Mb	12ns 20ns 20ns
Rohm	1Mb SRAM	
S-MOS	1Mb	70, 85, 100ns
Silicon Connections	256K, BiCMOS	8-15ns
Sharp	1Mb SRAM 1Mb SRAM	25, 35ns 100, 120ns
Thunderbird	64K	8ns
Nonvolatile Memory Developments		
Atmel	1Mb EEPROM	120ns
Mitsubishi	16Mb EEPROM	60ns
NEC	4Mb flash Flash EEPROM	
SGS-Thomson	64K smart RAM	100, 120ns
Toshiba	16Mb	62ns
Speciality Memory Developments		
EDI	SRAM modules	
IDT	SRAM dual-port modules SRAM module	40-100ns 70ns
Mitsubishi Electric	16Mb SRAM module	
Nippon LSI Card	8MB flash memory card	
Sharp	FIFO	15, 20, 25ns

Source: Various Publications, Dataquest (May 1991)

of 1991. The company's goal is to increase production efficiency right from the beginning of the 16Mb DRAM demand. The plant has been producing memory devices in small quantities using an 8-inch wafer pilot line. The line processes 3,000 wafers per month, but the company plans to increase production to 10,000 units by the second half of this year.

Fujitsu described its newly developed 64Mb prototype at the ISSCC conference in San Francisco in February. Fujitsu claims the 40ns device has a current-sensing data bus amplifier combined with bus-on-cell architecture for parallel wideband data processing of 64Mb compressed test functions. The device is fabbed in 0.4-micron CMOS using i-line phase-shift lithography.

Hitachi

Hitachi sample shipped 4Mb DRAMs starting in March 1991. The device is designed using a 0.5-micron process and integrates 25.5 million elements on the chip. The 512Kx8 chip comes in four types, featuring access times ranging from 55 to 100ns. The devices are packaged in 32-pin 600-mil DIP and 525-mil SOP.

Hitachi and Texas Instruments Joint Venture

Hitachi and Texas Instruments (TI) have jointly developed an SOJ package designed for 16Mb DRAM devices. The 28- or 24-pin LOCCB package is made of plastic, meets the 400-mil x 725-mil JEDEC standard, and can store a chip as large as 330-mil x 660-mil. This development is in conjunction with the 16Mb DRAM technology exchange agreement signed late in 1988.

Intel

Intel Corporation announced its line of 4Mb DRAMs with organizations of 4Mbx1 and 1Mbx4. Both devices are available in 300-mil SOJ packages with 80ns access times. The devices feature fast page-mode operation.

Matsushita

Matsushita presented a paper on its 64Mb DRAM prototype during the ISSCC conference. The circuit is built using a tunnel-shaped stacked-capacitor cell in a twin-cell 0.4-micron CMOS.

Mitsubishi Electric

During the ISSCC conference, Mitsubishi presented a paper on its 45ns 64Mb DRAM prototype, which will be manufactured using a 0.4-micron linewidth i-line microlithography. The device is divided into four segments, each having 16Mb of memory and an individual peripheral circuit.

Motorola

Motorola and Toshiba expanded their 4Mb DRAM relationship. Starting in the third quarter of 1991, the Tohoku Semiconductor Corporation joint venture facility in Sendai, Japan, will produce 4Mb DRAMs. Motorola plans to offer the 4Mb DRAM in plastic SOJ and ZIP packages. A TSOP is currently under development.

NMB Technologies

NMB now offers a high-speed DRAM that allows direct memory addressing without resorting to page interleaving or cache assistance for 20-MHz microprocessors. Devices are manufactured using 5- and 6-inch wafers with 1.2-micron linewidths in fully automated Class 1 clean room facilities.

NEC

NEC announced that engineering sampling of its 16Mb DRAM started in March 1991. The company will initially ship 16Mbx1 and 4Mbx4 samples. The devices are available in three packaging types.

Siemens AG

Siemens AG is providing 16Mb DRAM samples to major customers for evaluation. The parts are available in 16Mbx1 and 4Mbx4 configurations and have access speeds of 60 and 80ns. The prototypes are housed in SOJ package types that are 400 mils wide with 24 and 28 pins.

Toshiba

Toshiba presented a paper at the ISSCC conference on its 64Mb prototype with 33ns typical RAS access time and 15ns typical column address access time. It uses an asymetrical stacked trench capacitor cell in a PMOS centered interdigitated twisted bit line scheme. The circuit is fabricated in a double-poly, double-polycide, double-metal 0.4-micron triple-well CMOS technology.

Toshiba announced the addition of TSOP package types available on its 1Mb DRAM lineup. The parts are available in 60, 70, 80, or 100ns speed sorts. Operating current is 90mA and standby current is 2mA at TTL levels, 1mA at CMOS levels. The devices operate with a 5V power supply with a ±10 percent tolerance.

Toshiba also introduced a new series of 4Mb DRAMs with a 512Kx8 organization, which offers efficient exchanges of information with CPUs. This configuration frees system designers from having to provide the refresh signals from the CPUs. The device features access times of 70, 80, and 100ns. The device is packaged in a 400-mil-wide 28-pin SOJ and 400-mil 28-pin ZIP.

Toshiba is sample shipping a 60ns 4Mb DRAM that is packaged in TSOP. The device is organized in 1Mbx4 and 4Mbx1.

SRAM DEVELOPMENTS

Cypress Semiconductor

Cypress announced shipment of its 64K TTL I/O BiCMOS SRAM with access times of 10ns, made possible with its 0.8-micron BiCMOS technology.

Fujitsu

Fujitsu announced development of two 4Mb SRAMs featuring access times of 7 and 10ns. The device is configured 4Mbx1 and 1Mbx4 and was designed using the 0.5-micron CMOS process and 0.8-micron bipolar CMOS processes. The memory device operates on 3.4V and requires 450mW to operate.

Fujitsu has developed a 1Mb SRAM with an access speed of 15ns. The device was designed using a 0.8-micron bipolar CMOS process and consumes only 800mW in operation mode.

Hitachi

Hitachi started sample shipping 256K SRAMs that feature a 15ns access time. The SRAM has a 32Kx8 configuration and is housed in a 28-pin 300-mil SOJ or DIP. A 20ns version is also available.

Hitachi also began sample shipping its 4Mb SRAM during March 1991. The device is manufactured using a 0.5- to 0.6-micron design rule.

IBM

IBM Corporation announced development of an SRAM device that holds 512K of information and has an access time speed of 4ns.

Intel

Intel Corporation announced its 100ns 1Mb slow SRAM organized as 128Kx8. The product is offered in 32-pin plastic DIP and 32-pin SOG. The device operates on a single +5V power supply with TTL-compatible inputs and outputs.

Mitsubishi

Mitsubishi Electric announced entry into the 256K SRAM market with a 10ns device designed using a 0.8-micron CMOS process. The device is intended for use for cache memory and is configured in 32Kx8 and 32Kx9.

Motorola

Motorola announced production of four new 64Kx4 fast synchronous SRAMs. The memory cycle time of 12ns for the pipelined memories allows cache memories to operate, with no wait states, up to 83-MHz line transfer rates. The non-pipelined memories have memory cycle times of 15ns and allow cache operations to 66 MHz. All four devices are manufactured in Motorola's MOS 8 facility in Austin, Texas, using advanced-1.0 micron CMOS technology. The devices are available in plastic SOJ packages.

Motorola announced three fast SRAMs suited for main memory and battery backup applications. The devices are configured in 256Kx1, 64Kx4, and 64Kx4 and are available in 25 and 35ns access

speeds. The products are available in 24-lead plastic dual-in-line or SOJ packaging and 28-lead PDIP.

NEC

NEC announced plans to begin engineering sampling of its 4Mb SRAM, featuring an access time of 60 and 70ns, which began in the first part of April. NEC plans to advance to 15ns models when volume productions start later in the year.

Paradigm

Paradigm Technology announced its 256K CMOS SRAM with access times of 12ns. The 256K is available in 32Kx8, 64Kx4, and 256Kx1 organizations. Inputs and outputs are fully TTL compatible. The devices operate from a single ±5V power supply and are available in standard-power (typical 400mW active, 400uW standby) and low-power (typical 350mW active, 100uW standby) versions. Packaging options are plastic DIP, CERDIP, plastic SOJ-SO, ceramic LCC, and flatpack.

Paradigm also announced its 128Kx8 SRAM with a 20ns access time over the full military temperature range. The device is in a leadless chip carrier and is approximately 30 percent smaller than any other megabit SRAM package.

Paradigm also announced its addition of two 1Mb SRAMs configured in 1Mbx1 and 256Kx4 and featuring 20ns access times. The new devices are CMOS technology and were developed specifically for the multimegabit SRAM market. The devices are inputs and outputs fully TTL compatible. Packaging options are 400-mil sidebrazed DIP packages and, for surface-mount applications, plastic SOJ or ceramic LCC packages. The devices operate from a single +5V power supply and are available in versions for standard and low power.

Rohm

Rohm announced plans to enter the commercial 1Mb SRAM market by the spring of 1993. Its LSI Research Center, which was established in 1989, will become fully operational by then and will have had submicron processing lines installed.

S-MOS

S-MOS, a division of Seiko Epson in San Jose, California, announced that it will market a 1Mb SRAM. The device is designed for storage systems requiring battery backup, such as portable laptop and hand-held computers. The current product is configured in 131,072 words x 8 bits. Access times available are 70, 85, and 100ns. The device operates from a 5V power source and is completely static, requiring no clock.

Silicon Connections Inc.

Silicon Connections Inc., located in San Diego, California, has developed and started marketing a family of BiCMOS SRAMs with access times ranging from 8 to 15ns. The company uses a 1.0-micron design rule, and the devices are organized in 256Kx1, 64Kx4, and 16Kx4. The 256Kx1 at 15ns is available in a 24-pin ceramic flatpack package.

Sharp

Sharp introduced two of its 1Mb SRAMs, arranged as 128Kx8 and 256Kx4 with access times of 25 and 35ns. The 128Kx8 device is available in a JEDEC standard 32-pin, 400-mil SOJ package, and the 256Kx4 is available in a 28-pin SOJ package that provides an output-enable function. Both devices are produced in Japan using 0.8-micron CMOS technology.

Sharp has developed a new low-power 1Mb CMOS SRAM that uses thin-film transistor (TFT) memory cells and consumes only 0.1-micron amps when it just retains data and 1-micron amps when it operates.

Thunderbird Technologies

Thunderbird Technologies Inc., a new start-up located in Research Triangle Park, North Carolina, announced that it will manufacture fast (8ns) SRAMs. The 64K device is manufactured using a 0.8-micron MOS transistors with an active power dissipation of less than 300 milliwatts and idle power of 200 microwatts.

NONVOLATILE DEVELOPMENTS

Atmel

Atmel, located in San Jose, California, announced its fast (120ns) EEPROM in two

different organizations: 64Kx16 and 128Kx8. The 64Kx16 device requires 400 microamps of power in standby mode and 100mA during full operation, while the 128Kx8 part uses 300 micro amps and 70mA, respectively. The 128Kx8 device is available as a 32-pin sidebrazed DIP, 44-pad ceramic LCC, 30-pin ceramic PGA, and 32-lead ceramic flatpack. The 64Kx16 is available as a 44-pin sidebrazed DIP or a 44-pad LCC.

Mitsubishi

Mitsubishi Electric announced the development of a 16Mb EEPROM with a built-in sequence controller capable of automatically erasing and writing data. Designed using a 0.6-micron CMOS process, the chip measures 18.4mm x 6.5mm. The stacked-gate memory cell measures 1.8 micron x 2.0 micron. Four 4Mb memory arrays are divided into 16 segments each, thus achieving an erasing time almost as fast as 1Mb flash EEPROMs. The chip has an access time of 60ns and is configured in 2Mbx8 and 1Mbx16.

NEC

NEC announced plans to put a 4Mb flash memory on the market by the end of 1991. Anticipating that the 16Mb DRAM will be in great demand, the company will enter the flash memory market with a 4Mb version without commercializing the 1Mb and 2Mb devices.

NEC also announced that it plans to enter the flash EEPROM market and will ship 4Mb samples within the end of the year. NEC has elected to enter this market because a wider range of applications, such as IC cards, electronic still cameras, and electronic filing systems, have increased the market's size significantly.

SGS-Thomson

SGS-Thomson Microelectronics announced full-volume production of two new nonvolatile Smart RAM memories that include built-in real-time clocks and calendars. Each contains an ultralow power 8Kx8 CMOS SRAM, a CMOS clock and power-fail detection circuits, a crystal, and a lithium battery, all housed in a single JEDEC standard 28-pin plastic DIP package. The power-down and clock functions are fully implemented within the devices so that no external components are required.

Toshiba

Toshiba announced development of a 16Mb EPROM with an access time of 62ns. The device was designed using a 0.6-micron process.

SPECIALTY DEVELOPMENTS

Electronic Designs Inc.

EDI of Hopkinton, Massachusetts, announced the availability of 32-bit wide SRAM modules for military applications. These modules are intended to save board space for designers through their use of double-sided surface-mount technology. Two modules are 2Mb and 8Mb devices, organized as 64Kx32 and 256Kx32. These modules are also available for commercial use.

Integrated Device Technology Inc.

IDT expanded its family of modules with the introduction of a series of 4Mb and 8Mb TSOP modules. All three modules are available in speeds up to 70ns and are mounted on an FR-4 single in-line board.

IDT has announced the availability of a dual-port memory module configured in 16Kx32. The device is packaged as a 121-lead pin-grid array. This package density is achieved by mounting four 16Kx8 dual-port devices on a 68-lead LCC package with 25-mil lead pitch. The module is available in 40, 45, 50, 55, 65, 80, and 100ns access speeds.

IDT also announced its availability of SRAM modules in a series of 4Mb and 8Mb TSOP.

Mitsubishi

Mitsubishi Electric developed a 16Mb SRAM module and started shipping product in April 1991. The module consists of 16 1Mb SRAM devices that are housed in TSOPs; four are mounted on both sides of a substrate, and two substrates are stacked. The module has an access time of 85ns.

Nippon LSI Card

Nippon LSI Card shipped an 8MB flash memory card. The company offers other super-FD memory cards.

Sharp

Sharp introduced its first 36-bit wide bidirectional FIFO. Sharp claims the FIFO is ideal for interfacing to 32/36-bit wide busses and processors. The device is organized as 256 words x 36 bits x 2 and is available in 15, 20, and 25ns access time versions and 25, 30, and 35ns cycle time versions, respectively.

Ione Ishii

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Research Newsletter

SIS MEMORY QUARTERLY NEW PRODUCTS NEWSLETTER

This newsletter contains a synopsis of detailed memory product news events gathered from the trade press and company releases during the first quarter (January, February, and March) of 1990. It is meant to be a reference guide of new products for competitive analysis, monitoring technology trends, and tracking feature developments and improvements. Dataquest assumes no responsibility for the accuracy of the contents.

Table 1 shows the new products for the first quarter of 1990.

DRAM DEVELOPMENTS

Micron Technology

Micron Technology has announced the JAN 38510, a 1Mb DRAM. The DRAM is available in

TABLE 1
New Memory Products—First Quarter 1990

Company	Density	Speed
	DRAM Developments	
Micron Technology, Inc.	1Mb	80, 100, 120, 150ns
	256Kx4	70, 80, 100ns
Mitsubishi Electronics	1Mb	70, 80ns
NEC	1Mb	60ns
Samsung Semiconductor	4Mb	
	SRAM Developments	
Catalyst Semiconductor	256K	85ns
Cypress Semiconductor	64K	12ns
Dense Pac Microsystems Inc.	4Mb	85-150ns
Goldstar Technology	8Kx8	150ns
Hitachi America, Ltd.	4Mb	100ns
Integrated Silicon Solution, Inc.	8Kx8	20, 25, 30ns
Intel Corporation	32Kx8	25ns
Logic Devices Inc.	256K	12, 15ns
LSI Logic Inc.	NA	NA
Micron Technology, Inc.	256K	25, 35, 45, 55ns
Mitsubishi Electric	1Mb	35ns

(Continued)

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TABLE 1
New Memory Products—First Quarter 1990 (Continued)

Company	Density	Speed
Motorola, Inc.	256K	15, 20, 25ns
Philips International N.V.	8Kx8	55 to 70ns
Samsung Electronics Co.	1Mb	70, 80, 100, 120ns
Sharp	256K	12, 100ns
VLSI Technology, Inc.	1Mb	35, 45ns
	16K	12, 15ns

Company	Density	Type	Speed
	Nonvolatile Memory Developments		
Advanced Micro Devices	2Mb	EPROM	100ns
Cypress Semiconductor Corporation	256K	PROM	35ns
International CMOS Technology	1Mb	EPROM	55, 70, 90ns
Microchip Technology		EEPROM	
Mitsubishi	4Mb	EPROM	100, 120, 150ns
Sharp Electronics	16Mb, 4Mb	ROM	200, 100ns
Texas Instruments	256K	EEPROM	
Toshiba	1Mb	EPROM	85ns
	1Mb	EPROM	55, 70ns
	4Mb	EPROM	120, 150ns
White Technology	4Mb	EEPROM	150ns
	Specialty Memory Developments		
Advanced Micro Devices	512x9	FIFO	25, 35ns
Brooktree	256x24	Ramdac	
Inmos Ltd.		Color lookup table	
NEC	4Mb, 2Mb	Muse HDTV	21ns
Samsung Semiconductor	512x9	FIFO	20ns
SGS-Thomson Microelectronics	1,024x9, 512x9	FIFO	35ns
Sharp	512X9	FIFO	15, 20ns
Texas Instruments	16Kx5	Cache address comparators	18, 20ns

NA = Not available
Source: Various publications, Dataquest (July 1990)

an 18-pin DIP, a 20-pin rectangular LCC, and 20-pin flatpack. It is available in 80, 100, 120, and 150ns.

Also announced by Micron Technology is a 256Kx4 fast static-column DRAM. It features access speeds of 70, 80, and 100ns. The DRAM is obtainable in four package types: plastic DIP, ceramic DIP, plastic ZIP, and plastic SOJ, all with industry standard dimensions.

Mitsubishi Electronics

Mitsubishi Electronics has introduced two 1Mb CMOS DRAMs in a thin small-outline

package (TSOP), the M5M41000BVP/RVP organized 1Mbx1, and the M5M44256BVP/RVP organized 256Kx4. Both are attainable in 24/20-pin, 300-mil TSOPs and have access times of 70 and 80ns.

NEC

Released by NEC are two 1Mb DRAMs—the uPD421000-60, 1Mbx4-bit and the uPD424256-60, 256Kx4-bit. Both have an access time of 60ns and are packaged in DIPs, SOJs, and ZIPs. Each DRAM measures 4.55x10.4mm and consumes 90mA.

Samsung Semiconductor

Samsung Semiconductor is now offering the KM41C-4000, a 4Mb CMOS DRAM. It is available in a JEDEC standard pinout plastic SOJ package.

SRAM DEVELOPMENTS

Catalyst Semiconductor

Introduced by Catalyst Semiconductor is a new 256K CMOS SRAM. The CAT71C256LPI has a configuration of 32Kx8 and a maximum access time of 85ns.

Cypress Semiconductor Corporation

Cypress Semiconductor has announced a family of 64Kb BiCMOS SRAMs. The CY7B160, B161, B162, B164, and B166 are 16Kx4 chips, and the CY7B185 and B186 are 8Kx8 chips. The B185 is available in a 300-mil-wide package and the B186 is available in a 600-mil-wide package. All of the chips are available in plastic DIP versions with an access time of 12ns. The RAMs consume 600mW when active and 200mW when the dissipation drops.

Dense Pac Microsystems Inc.

Introduced by Dense Pac Microsystems is a 4Mb CMOS SRAM, the DPS512S8. Its configuration is 512x8 bits, and it is packaged in a 32-pin DIP. It is a 600-mil module that conforms to the JEDEC standard pinout. The SRAM has access times ranging from 85 to 150ns.

Goldstar Technology

Goldstar Technology is selling 8Kx8 SRAMs, which are attainable in 28-pin DIPs and SOPs with an access time of 150ns. The SRAMs have 40 milliamps in operating current and 100 microamps in standby.

Hitachi America, Ltd.

Hitachi America is now offering the HM658512 series, a 4Mb pseudo SRAM (PSRAM). The PSRAM is configured as 512Kx8 and has an access time of 100ns. It is available in a 600-mil, 32-pin DIP package and a 525-mil, 32-pin surface-mount SOP package.

Integrated Silicon Solution, Inc.

Integrated Silicon Solution has launched the IS61C64, a 8Kx8 SRAM that is available with access times of 20, 25, and 30ns. The SRAM is packaged in the JEDEC standard 28-pin, 600-mil DIP, 300-mil DIP, and SOP.

Intel Corporation

Released by Intel Corporation are two 32Kx8 SRAMs, the M51256 and M51256L. Both have an access time of 25ns and are available in four different package types: a 28-pin ceramic DIP; a 32-lead pin grid array; a 32-pin LCC; and a 32-lead J-lead gull-wing chip carrier.

Logic Devices Inc.

Logic Devices is sampling 256K SRAMs: the L7C197 (256Kx1), the L7C194, 195, and 196 (64Kx4), the L7C191 and 192 (64Kx4 with separate I/O), and the L7C199 (32Kx8). All have an access time of 15ns except for the L7C197, which has an access time of 12ns. The SRAMs are obtainable in plastic DIP and SOIC packages; CERDIPs, LCCs, and flatpacks are offered for military applications.

LSI Logic Inc.

Released by LSI Logic is a new SRAM, the L64212. A 30-MHz version is now attainable in a 95-lead ceramic pin-grid array.

Micron Technology, Inc.

Micron Technology has announced the JAN 38510, a 32x8 256K SRAM. The device is offered in 300- and 600-mil DIPs and 28- and 32-pin LCCs. The SRAM has speeds of 25, 35, 45, and 55ns.

Mitsubishi

Being sample-released by Mitsubishi Electric are two 1Mb SRAMs. Both have an access time of 35ns and measure 6.1x15.84mm. The M5M51001 is configured as a 1Mbx1 construction, and the M5M51004 is configured with a 256Kx4 construction. The SRAMs are available in a 400-mil-wide, 28-pin SOJ package. DIP and TSOP packages will be available soon.

Motorola Inc.

Motorola introduced the MCM6207 (256Kx1), MCM6208 (64Kx4), and MCM6209 (64Kx4 w/OE). All of the fast SRAMs have access times of 15, 20, and 25ns. They are obtainable in standard 300-mil PDIP and plastic SOJ packages.

Philips International NV

Now being offered by Philips International NV is the FCB1C65, an SRAM-configured 8Kx8. It has access times between 55 and 70ns and is offered in a 600-mil 28-pin DIP and a 330-mil SOP.

Samsung Semiconductor

Samsung Semiconductor has launched a 1Mb high-speed SRAM. The KM681000/L is available in speeds of 70, 80, 100, and 120ns and is packaged in a 32-pin DIP (600 mil) and 32-pin SOP (450 mil).

Sharp

Sharp has begun sampling the LH51256, a 256K SRAM. The LH51256-10L is offered at a speed of 100ns, and the LH51256-12L is offered at 12ns. It is offered in a 600-mil, 28-pin DIP and a 450-mil, 28-pin SOP.

VLSI Technology, Inc.

VLSI Technology, along with Hitachi, has released a 1Mb (256Kx4) SRAM, known both as the VT624256 and the VT624256L. The SRAM is presented in a 400-mil, 28-pin SOJ package. It has a fast access time of 35ns, but also is available in 45ns. Both access times offer an extremely low power consumption of 350 milliwatts in active mode and 100 microwatts in standby mode.

Also introduced by VLSI Technology are two high-speed SRAMs, the VT20C19 (2Kx8) and the VT20C79 (4Kx4). Both have access times of 12 and 15ns.

NONVOLATILE MEMORY DEVELOPMENTS

Advanced Micro Devices

Offered by Advanced Micro Devices is the 2Mb Am27C020 (256Kx8) EPROM. It has an access time of 100ns and is available in a 32-pin DIP or an LCC.

Cypress Semiconductor Corporation

Cypress Semiconductor has released a threesome of 256K PROMs, the CY7C279, CY7C271, and CY7C277. All three have an access time of 35ns and are offered in 300-mil-wide 28-pin DIPs. A fourth PROM, the CY7C274, is housed in a 600-mil-wide DIP and has a standard EPROM pinout.

International CMOS Technology

International CMOS Technology has introduced the 27CX010, a 1Mb EPROM with access times of 55, 70, and 90ns. It is configured 128Kx8 and is obtainable in a 32-pin windowed DIP.

Microchip Technology

Microchip Technology is sampling four families of EEPROMs. The 24C01A, 02A, and 04A are 1, 2, and 4Kb and have configurations of 128x8, 256Kx8, and 512x8. The 85C72, 82, and 92 are similar except for the different pin organizations. The 93C06 and C46 are available in 256- and 1,024-bit densities and are organized 16x16 and 64x16. Ultimately, the 59C11 is an enhanced

version of the 93Cxx series, with an organization of 128x8 or 64x16. All of the chips are attainable in CERDIPs and plastic DIPs, as well as small-outline ICs.

Mitsubishi

Mitsubishi Electric is offering two 4Mb EPROMs. One has a bit construction of x8 and the other is x16. Both EPROMs are available with access times of 100, 120, and 150ns and have a power consumption of 30mA in active mode and 100uA in standby mode.

Sharp Electronics

Sharp Electronics has unveiled a 16Mb mask ROM with an access time of 200ns and is developing a 4Mb ROM with an access time of 100ns.

Texas Instruments

Being released by Texas Instruments are 256K flash EEPROMs. The EEPROMs have a 5V power supply. They are offered in 28-pin plastic and ceramic DIPs and in 32-pin PLCCs.

Toshiba

The TC57H1024D, a 1Mb EPROM, has been introduced by Toshiba. The EPROM has an organization of 64Kx16 and an access time of 85ns.

Toshiba launched two new 1Mb EPROMs with access times of 55ns (TC57H1025AD-55) and 70ns (TC57H1025AD-70). Both are available in a 40-pin cirdip DIP (JEDEC standard).

Also introduced by Toshiba is a 4Mb EPROM that is fully compatible with 4Mb mask ROMs. The 4Mb EPROM is configured in 512Kx8 or 256Kx16 and is available in 120 and 150ns. It will be packaged in a 40-pin CERDIP, a 40-pin plastic DIP, and a 40-pin plastic SOP. The EPROM has an operating current of 60mA and a standby current of 100uA.

White Technology

White Technology has announced the M4194E, a 4Mb EEPROM. The EEPROM is configured in three modes, 512x8, 256x16, or 128x32. All three configurations are available in a 76-pin flatpack and have a maximum speed of 150ns.

SPECIALTY MEMORY DEVELOPMENTS

Advanced Micro Devices

Advanced Micro Devices has unveiled the Am4601 CMOS FIFO. It is organized 512x9, with access times of 25 and 35ns. The 35ns chip is obtainable in a 28-pin 300-mil plastic DIP or 32-pin PLCC.

Brooktree

The Bt474 Ramdac has been released from Brooktree. The Ramdac offers a 256Kx24 color RAM and 15-color overlay. The Bt474 also can handle 640- by 480-pixel VGA graphics. It is attainable in a 84-pin PLCC.

Inmos Ltd.

Inmos has introduced a color lookup table, the IMS G176L. The device has a supply current of less than 10mA in standby. The G176L is available in three package types: a 28-pin plastic DIP, a 32-pin PLCC, and a 44-pin PLCC.

NEC

NEC now is offering the uPD42290DW, a 4Mb field memory that can adapt a Muse HDTV system. It has an access time of 21ns and is obtainable in a 64-pin ceramic DIP. NEC also is sampling the uPD42291R, a 2Mb product that is packaged in a 68-pin ceramic PGA.

Samsung Semiconductor

Samsung Semiconductor has announced two CMOS FIFOs, the KM75C01A-15 (512x9) and the KM75C02A-15 (1024x9). Both chips have an access time of 15ns and are 120mA in active mode and 15mA in power-down mode.

SGS-Thomson Microelectronics

SGS-Thomson Microelectronics has introduced the MK45H02 (1024x9) and the MK45H01 (512x9), two low-power, high-speed FIFOs. Both have an access time of 35ns.

Sharp

Sharp has announced the LH5496D-15, a CMOS FIFO with an access time of 20ns. The part is packaged in a 28-pin DIP or a 32-pin PLCC. It has an organization of 512x9.

Texas Instruments

Introduced by Texas Instruments are two cache address comparators, the SN74ACT2163 and SN7ACT2164. Both consist of a high-speed 16Kx5 SRAM array and a 5-bit high-speed comparator. These cache address comparators have access times of 18 and 20ns, are packaged in a 32-pin PLCC, and can operate from a single 5V power supply.

Ione Ishii
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Research Newsletter

MOS EPROM: FLAGSHIP OF THE NONVOLATILE PRODUCTS

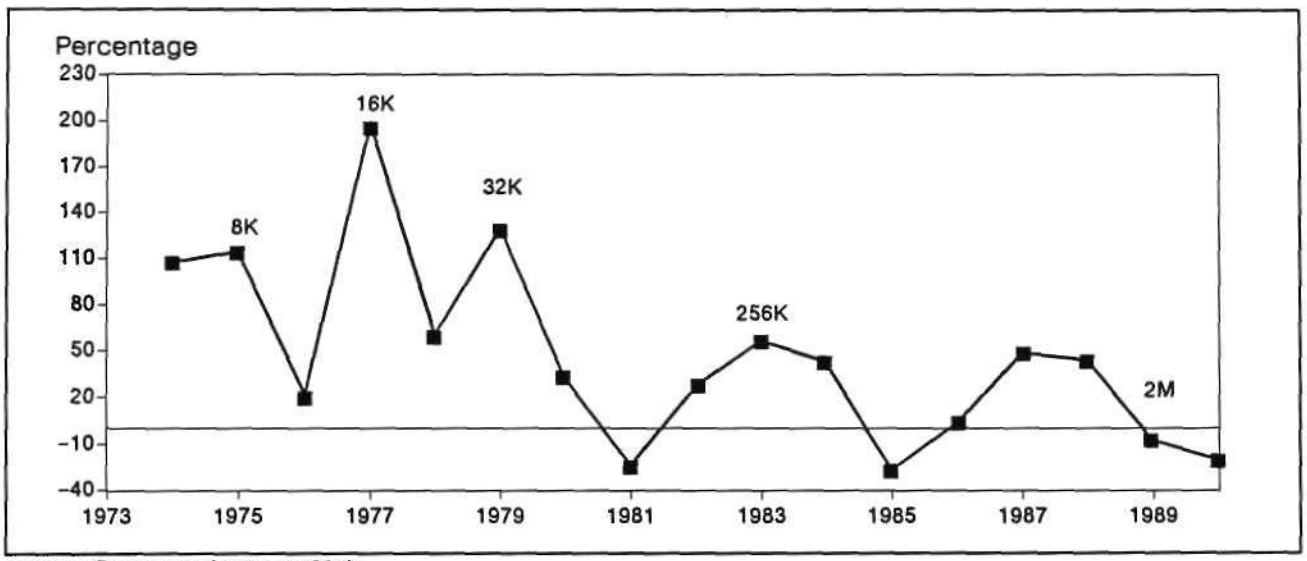
SUMMARY ANALYSIS

The EPROM product was introduced in 1971 by Intel Corporation. It shares a 20-year anniversary with the introduction of the microprocessor and was initially developed as a prototype device for ROMs. The pinnacle of EPROM development was reached in 1977, as shown in Figure 1, with the introduction of the 16K EPROM. The 16K density became the industry standard for EPROMs and also was compatible with microprocessors. In essence, the marriage of the EPROM and the microprocessor accelerated the development of both products and the advance of the microcomputer industry. In 1991, both Intel and Signetics announced their intent to stop manufacturing EPROMs during the 1990s. Although the EPROM product became a profitable growth market for Intel, Signetics, and others, it has not achieved, nor has it sustained, comparable yearly revenue growth rate patterns since the 16K density. As a revenue generator, the product is besieged by too many suppliers. As a performance indicator, the product is being eroded by other nonvolatile trade-offs. From all indications, the commodity EPROM is a sunset technology.

MARKET ANALYSIS

Since Dataquest began coverage of EPROM technology, worldwide EPROM suppliers have generated over $12.5 billion in revenue from 1976 through 1990. Viewed as the largest EPROM supplier to the worldwide market, Intel has generated over $2.5 billion in EPROM revenue during this same time frame. The 1990 forecast predicted that EPROM revenue would decline 5 percent to $1,690 million with a 3 percent unit growth to 405 million devices produced during 1989. Actual

FIGURE 1
MOS EPROM Revenue—Yearly Growth Rates



Source: Dataquest (August 1991)

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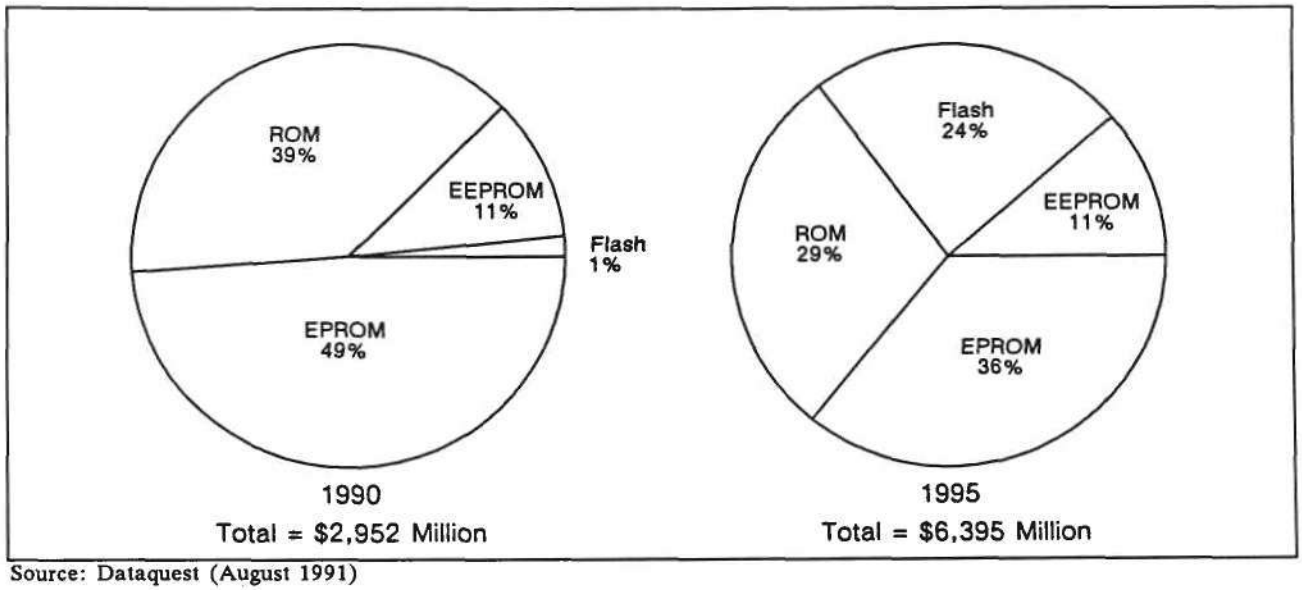
product revenue for 1990 declined 20 percent to $1,446 million with a 5 percent unit growth to 424 million devices over 1989 actuals. Long viewed as the lackluster product area of MOS memory products, EPROMs continue to claim the lion's share of the nonvolatile market, as shown in Figure 2. Year-to-year changes in revenue, units, and average selling prices are located in the Source: Dataquest booklet entitled *MOS EPROM Market Statistics 1990*.

During the 1988-through-1990 time frame, the nonvolatile market became a jungle fraught with predatory supplier tactics and low profit margins. Although total MOS memory revenue is expected to have a compound annual growth rate (CAGR) of 17.9 percent from 1990 through 1995, EPROM is expected to have a modest CAGR of 9.4 percent during the same time frame. The forecast revenue of $2.2 billion by 1995, as shown in Figure 3, will occur as an end result of submicron high density, 4Mb, 8Mb, and 16Mb EPROM products.

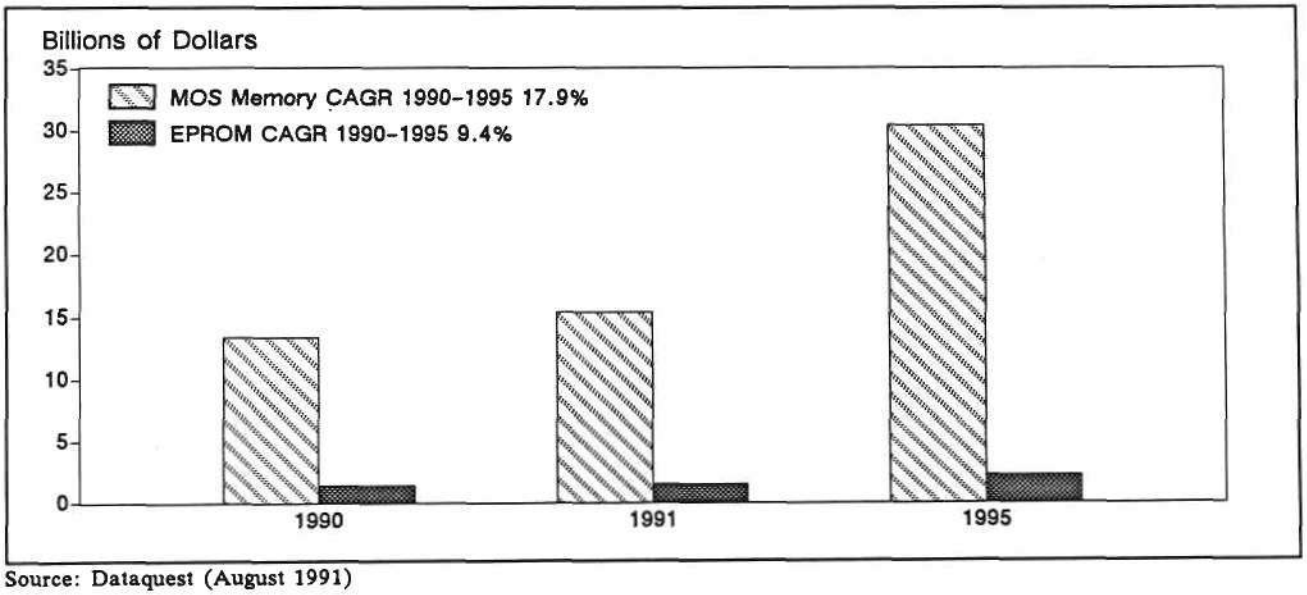
Potential conversion to other nonvolatile solutions and/or a slowdown in next-generation product

FIGURE 2
Worldwide Nonvolatile Revenue—Market Projections



Source: Dataquest (August 1991)

FIGURE 3
MOS EPROM Revenue—Share of MOS Memory



Source: Dataquest (August 1991)

development into new applications could interrupt this growth pattern, thus furthering decline of the EPROM market. The following developments offer further proof of the decline and possible demise of MOS EPROM products throughout the next decade:

- Shrinking vendor base
- Shrinking revenue per vendor
- Declining bit growth
- Maturing product base
- High cost of leading-edge technology
- Growth of replacement technologies
- Fragmented nonvolatile market
- Trade friction influences

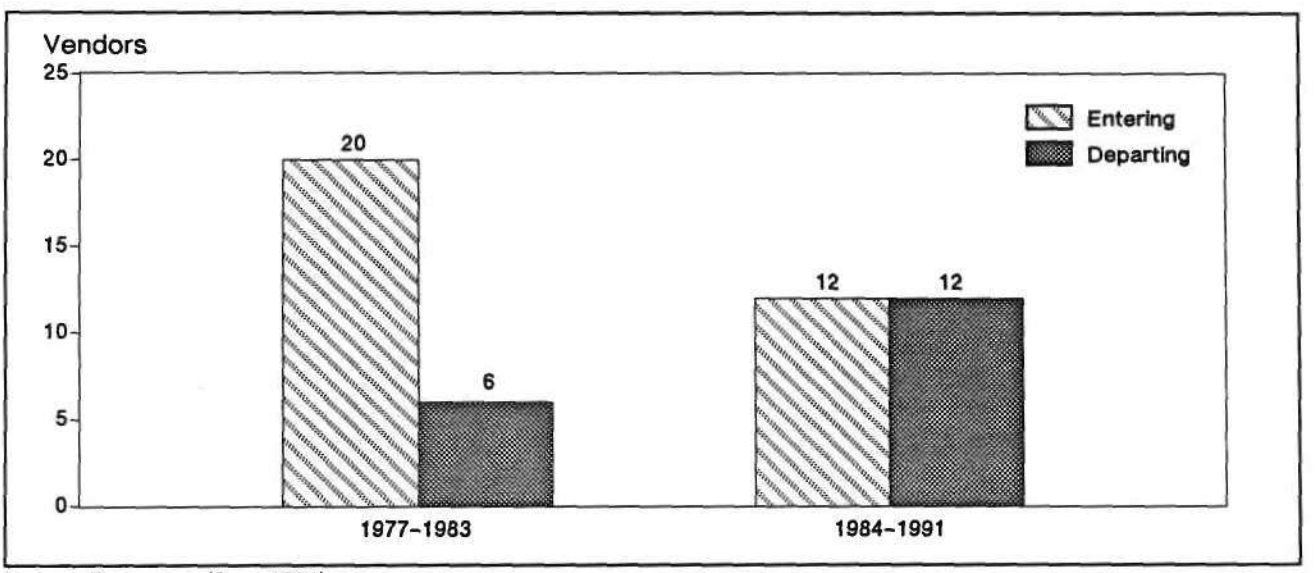
VENDOR-BASE ANALYSIS

Historically, the number of EPROM vendors entering the market has always surpassed the number of departing vendors until the 1988-through-1990 time frame (see Figure 4). Traditionally, companies that left the market represented a marginal share of the EPROM market. From 1982 through 1987, companies that entered the EPROM market made great gains in market share and revenue. From 1988 through 1990, the EPROM product area became a highly competitive and very commodity-oriented product area. Price erosion, other nonvolatile product competition, and a computer market downturn resulted in shrinking vendor revenue. Revenue distribution for the top 5 and top 10 companies in each region is shown in Table 1. Vendor revenue by region is shown in Table 2.

TECHNOLOGY ANALYSIS—LEARNING CURVES

The price learning curve is a strategic tool for forecasting and interpreting the sensitivity of EPROM prices to various factors such as business cycles and trade friction. Unlike cost-experience curves, price curves are heavily influenced by extraneous market forces such as competition, substitute technology, general economic conditions, and/or supply and demand dynamics. The price learning curve is defined by EPROM prices in millicents per bit and accumulated bit shipments. Figure 5 shows the accumulated bits shipped for total EPROMs from 1976 through 1990. Figure 6 illustrates how bit prices gravitate toward the declining slope of an experience curve over time. During the industry boom periods of 1978 and 1979 and again in 1983 and 1984, product shortages and vendor controls drove prices up above the 80 percent curve norm. During the 1980s and again in 1985 and 1986, the industry balloon burst. Capacity utilization rates declined, prices dropped—sometimes below cost—and the industry fell into a deep recession. A price-stabilization period, a result of the trade agreement between the

FIGURE 4
MOS EPROM Entering and Departing Vendors



Source: Dataquest (June 1991)

TABLE 1
MOS EPROM Top 5/10 Revenue Distribution (Percentage)

Top 5 and 10 Shares	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990
Top 5													
United States	91.0	79.1	70.9	75.6	72.0	60.9	68.2	68.0	71.1	61.6	54.0	58.3	61.0
Japan	87.4	73.3	52.7	49.3	27.8	34.9	26.5	29.4	23.1	19.0	17.1	39.5	43.4
Europe	3.6	5.8	18.1	26.3	44.1	26.0	41.7	38.6	48.0	42.6	26.5	9.9	6.7
Korea	NM	NM	NM	NM	NM	NM	NM	NM	NM	NM	10.4	8.9	10.9
Next 5													
United States	8.2	18.0	20.0	20.8	23.9	25.9	27.1	27.8	24.8	29.7	32.8	29.6	25.6
Japan	5.8	10.9	15.6	16.5	21.1	14.2	17.8	9.4	14.8	18.6	27.5	10.7	6.7
Europe	2.4	7.1	4.4	4.3	2.8	10.5	9.3	15.0	6.9	5.2	5.2	18.9	14.4
Korea	NM	NM	NM	NM	NM	1.2	NM	3.5	3.1	5.9	NM	NM	4.5
Top 10													
United States	99.2	97.1	90.8	96.4	95.8	86.8	95.3	95.8	95.9	91.2	86.7	88.0	86.6
Japan	93.2	84.2	68.3	65.8	48.9	49.1	44.3	38.7	37.9	37.6	44.6	50.2	50.1
Europe	6.0	12.9	22.5	30.6	46.9	36.5	51.1	53.6	54.9	47.8	31.7	28.8	21.1
Korea	NM	NM	NM	NM	NM	1.2	0	3.5	3.1	5.9	10.4	8.9	15.4
Top 5/10 Concentration													
No. of Vendors	12	13	15	16	17	17	17	20	24	23	24	22	21
Average Revenue per Vendor ($M)	11.044	30.907	35.114	21.578	33.927	51.724	73.312	43.317	37.918	58.688	81.110	82.198	59.507
Top 10 Share	99	97	91	96	96	87	95	96	96	91	87	88	87
Top 5 Share	91	79	71	76	72	61	68	68	71	62	54	58	54

NM = Not meaningful
Source: Dataquest (August 1991)

United States and Japan, is reflected in the 1986-through-1987 time frame. Foreign market values (FMVs) were stipulated in the agreement to act as minimum prices for EPROMs fabricated in Japan and sold in the United States. The trade agreement also called for narrowing the price differentials between U.S. prices and those in Asia and Europe. Shortages and increased demand in 1987 and 1988 raised EPROM prices substantially. An economic downturn and a computer industry slowdown resulted in price erosion during 1989 and 1990, dropping the price per bit below the profit margin range. The CAGR of EPROM bit growth from 1975 through 1990 is shown as follows:

- 1975 to 1980—201.5 percent
- 1980 to 1985—98.1 percent
- 1985 to 1990—53.2 percent

LIFE CYCLES

Understanding product life cycles can be an important element of a company's strategic planning. How well semiconductor manufacturers and users implement the following EPROM life cycles may well determine their strength and future direction compared with worldwide competition. The actual life cycle curves for EPROMs and how they vary by density are shown in Figures 7a and 7b. Traditionally, the lower-density EPROMs peaked during their sixth year of production, although anomalies did occur in a few product areas as a result of package changes or industry downturns. Figure 8 illustrates the long-range forecast behavior of each EPROM density on an extended 13-year life cycle through the year 2000.

NONVOLATILE TRADE-OFFS

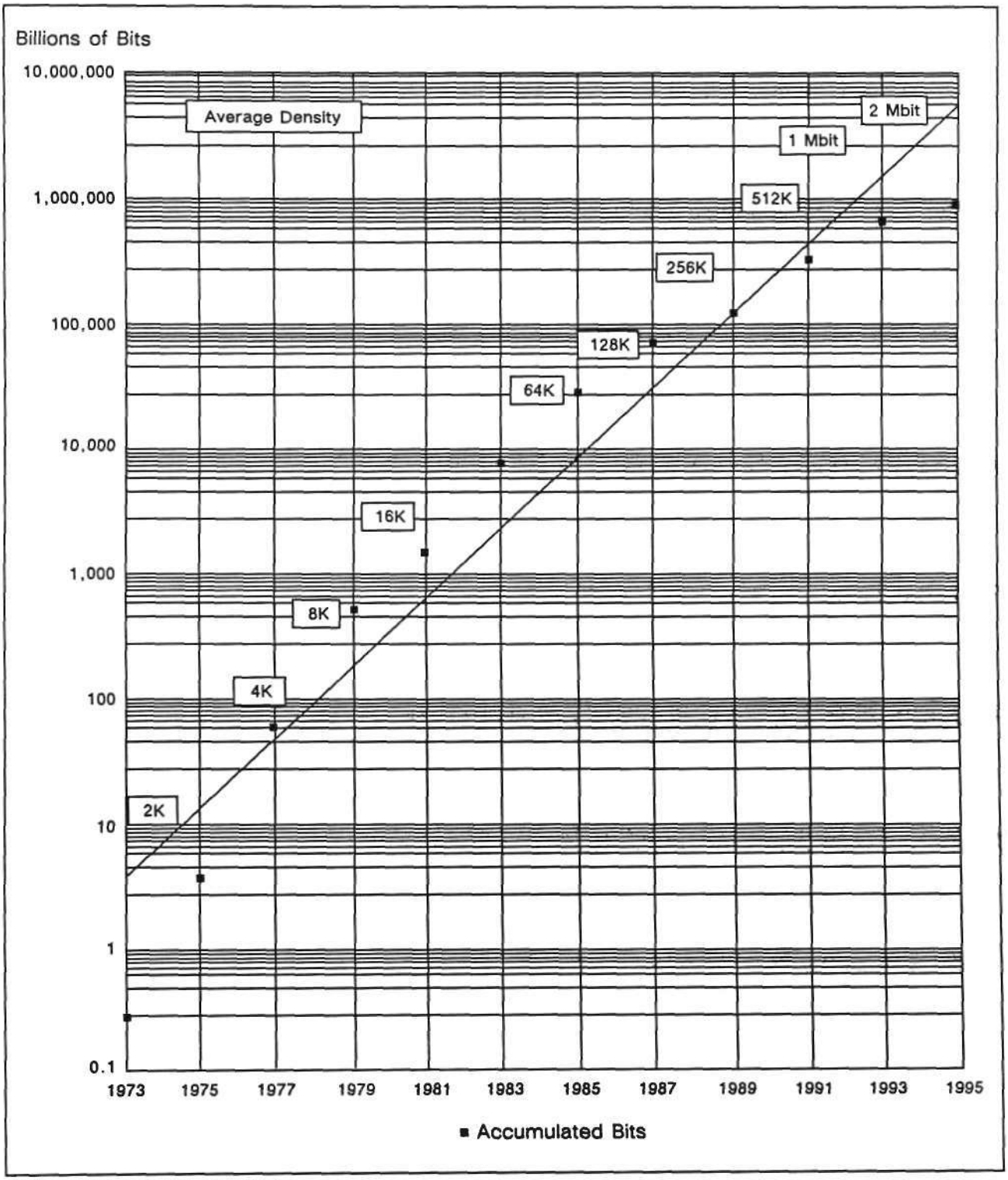
Dataquest believes that the next five years in the EPROM market will be characterized by moderate unit growth and slow bit growth. In the late 1970s, growth of both volatile and nonvolatile memory products resulted from a conversion from core memories. In the 1980s, memory growth was spurred by the PC market boom. Although more use of memory bits per system is expected, more memory devices with nonvolatile features, with or

TABLE 2
MOS EPROM Regional Vendor Concentration

Regional Concentration	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990
Number of U.S. Vendors	8	8	8	7	8	8	8	10	9	10	11	11	10
U.S. Market Share (%)	92	88	72	66	52	49	46	40	40	44	52	58	61
Average Revenue per Vendor ($)	14,468	40,220	44,196	31,033	33,684	56,170	75,008	35,495	41,823	56,852	84,371	87,044	82,342
Number of Japanese Vendors	4	5	7	7	7	7	8	8	10	9	9	8	9
Japanese Market Share (%)	8	13	26	33	45	49	50	54	56	47	33	27	20
Average Revenue per Vendor ($)	1,957	11,568	23,837	15,493	37,431	58,751	86,054	59,106	50,285	76,402	76,366	78,377	44,445
Number of European Vendors	0	0	0	2	2	2	2	2	3	2	2	2	2
European Market Share (%)	0	0	3	0	3	3	4	6	5	8	15	15	15
Average Revenue per Vendor ($)	0	0	17,617	318	5,729	9,345	15,560	19,267	10,248	46,531	123,659	110,321	111,522
Number of Korean Vendors	0	0	0	0	0	0	0	0	2	2	2	1	0
Korean Market Share (%)	0	0	0	0	0	0	0	0	0	0	1	0	0
Average Revenue per Vendor ($)	0	0	0	0	0	0	0	0	13	315	3,793	3,224	0

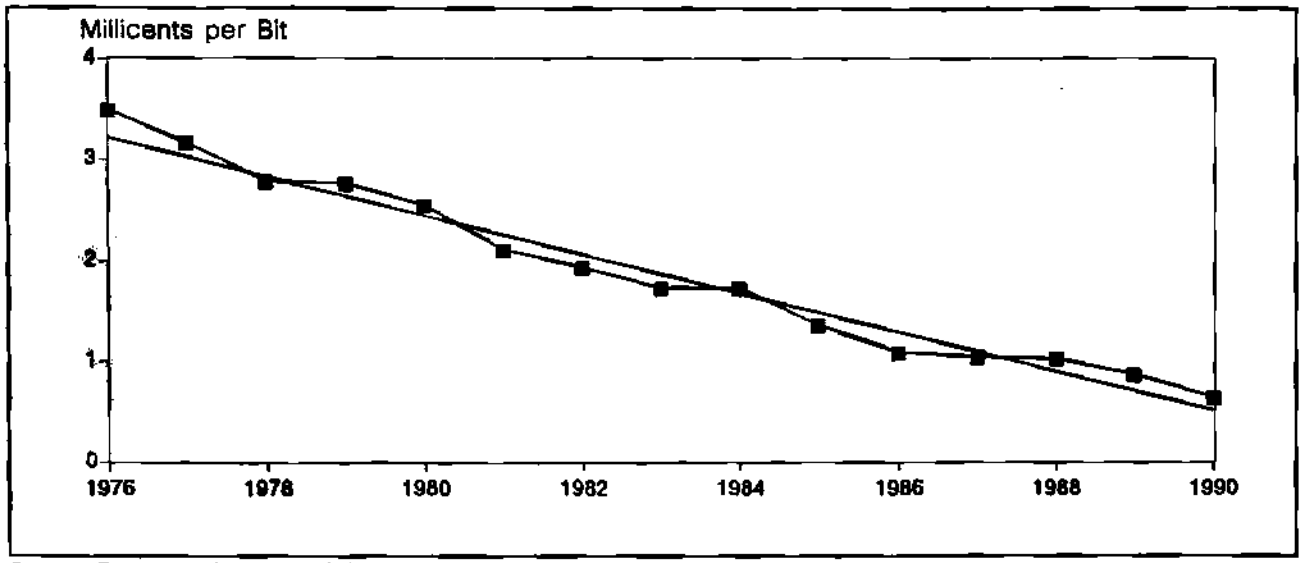
Source: Dataquest (August 1991)

FIGURE 5
MOS EPROM Bit Growth



Source: Dataquest (August 1991)

FIGURE 6
MOS EPROM Price Learning Curve



Source: Dataquest (August 1991)

without a battery, will also be available. As shown in Figure 9, users are now offered a broad spectrum of nonvolatile selections that fulfill or surpass the need for EPROM density upgrades. High-speed megabit ROMs, emerging 5V/12V Flash, and more cost-efficient EEPROMs and battery-backed SRAMs provide the user with a variety of comparable performing nonvolatile solutions.

DATAQUEST CONCLUSIONS

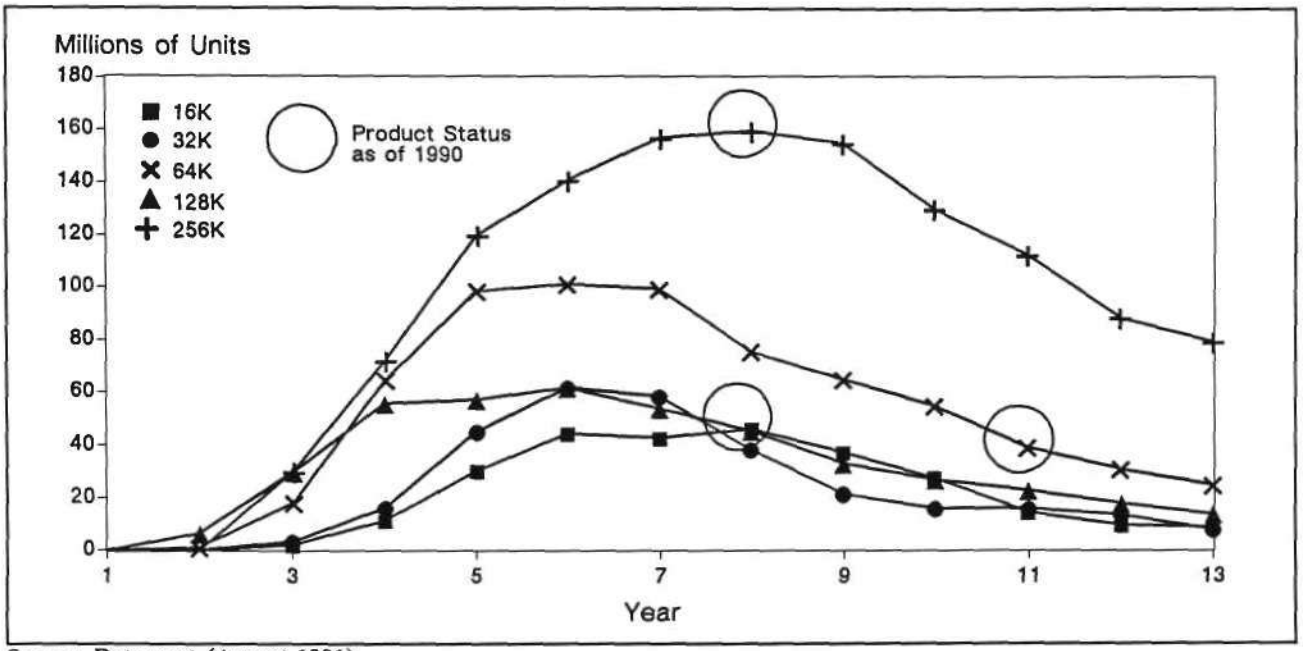
Dataquest has forecast increased EPROM revenue during the 1993-through-1995 time frame. This will be driven primarily by higher prices: a direct result of the advent of submicron products, as shown in Figure 10. These new submicron products will require greater capital investment, are technically more challenging to develop, and will demand more complex package and design expertise. All of these developments add up to increased costs and risks of financial recovery to the manufacturer. For these reasons, Dataquest expects a number of scenarios to occur during the next decade that could radically change the structure of the MOS EPROM market and vendor base:

- The EPROM vendor base will continue to decline as a result of increased R&D costs and trade restrictions.
- Shrinking EPROM revenue will force the need for memory partnering agreements.
- Surviving EPROM vendors will focus on specialty high-performance, more profitable, and risk-free EPROM products.
- EPROM products will be divided into two major segments—high-speed (85 to 120ns) EPROMs and specialty bipolar replacement (sub-70ns) devices.

In the midst of all this change, regional trade developments between the United States, Europe, and Japan in 1991 will continue to wreak havoc in the memory market for both users and suppliers. The officially released information on the new U.S./Japan trade agreement is as follows:

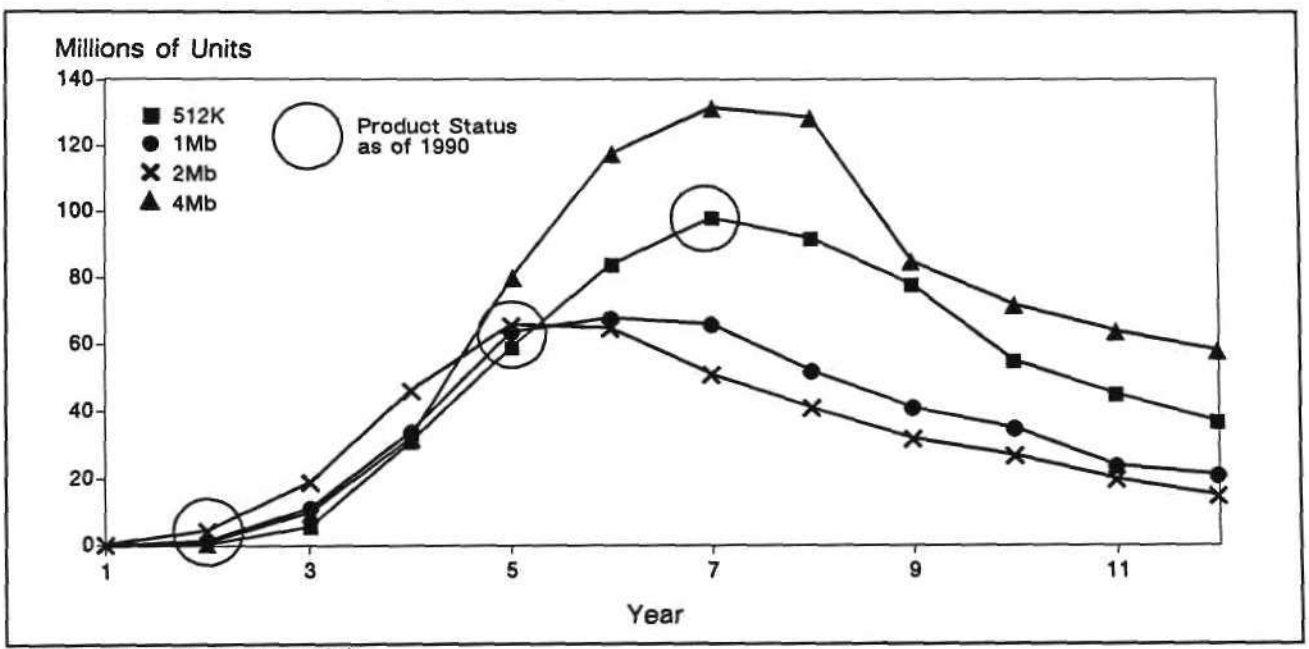
- It is a five-year, government-to-government agreement with an option to end the agreement in three years.
- The Japanese government reaffirms its commitment to an open market.
- There are no FMVs. Japanese companies will collect cost and price data to be reviewed by the U.S. government for dumping violations.
- Non-Japanese producers should achieve a 20 percent share of the Japanese semiconductor market by the end of 1992.
- There are two formulas to calculate market share—a U.S. formula that excludes branded and captive data and a Japanese Ministry of International Trade and Industry formula that includes branded and captive data.

FIGURE 7a
MOS EPROM Product Life Cycle by Density



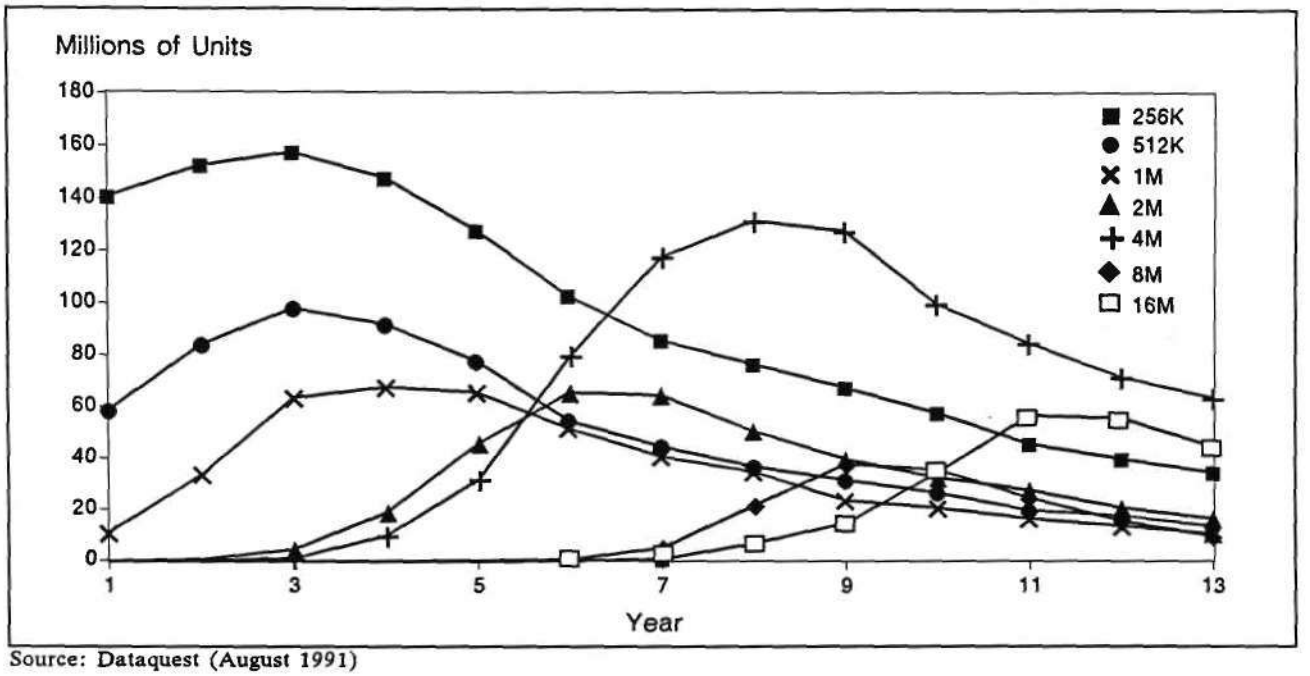
Source: Dataquest (August 1991)

FIGURE 7b
MOS EPROM Product Life Cycle by Density



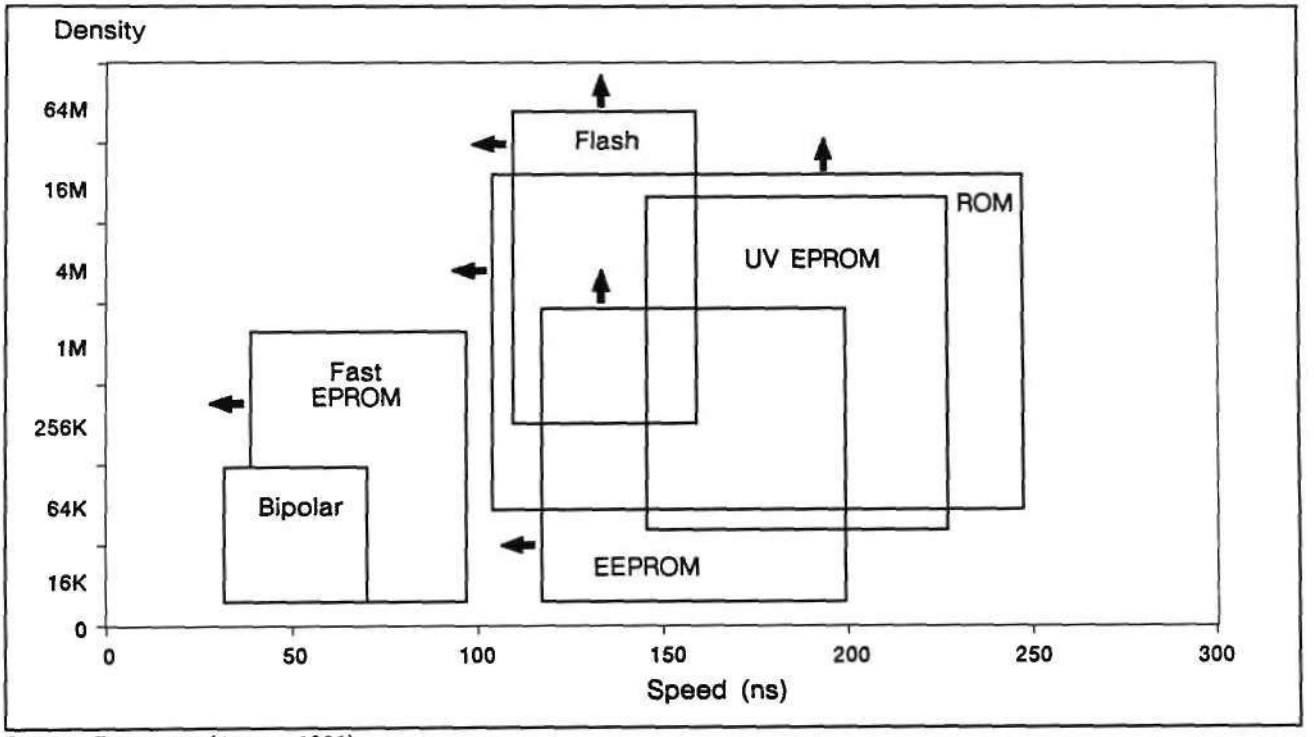
Source: Dataquest (August 1991)

FIGURE 8
MOS EPROM Life Cycle Forecast



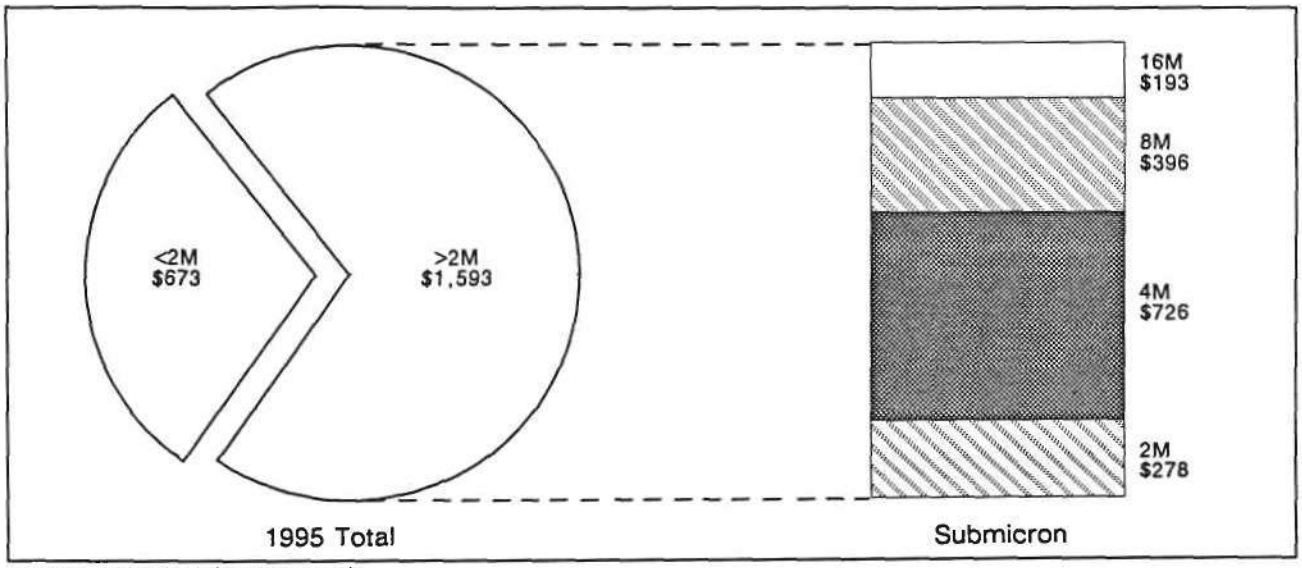
Source: Dataquest (August 1991)

FIGURE 9
Nonvolative Trade-Offs



Source: Dataquest (August 1991)

FIGURE 10
MOS EPROM Forecast—Submicron Revenue (Millions of Dollars)



Source: Dataquest (August 1991)

- The two governments will meet three times a year to evaluate the results of the agreement.

As a result of the agreement, the remaining sanctions of $165 million per year against Japanese products will be suspended. The suspension agreement on EPROMs will be extended.

The European Commission has introduced a definitive antidumping duty of 94 percent on all Japanese-manufactured EPROM products. Concurrently, the EC has agreed that seven Japanese EPROM manufacturers will undertake to abide by reference prices, providing for a conditional suspension of this duty. The regulation and undertakings came into effect March 13, 1991. Further analysis on the trade agreements can be located in *Dataquest Perspectives* and Dataquest's March 1991 *Research Newsletter* entitled "EC EPROM Reference Price Agreement."

Are there any winners in government-enforced trade agreements? In the United States and Europe, users must pay higher prices for the memory products than they would in a free-trade environment. Since the implementation of the U.S.-Japan trade agreement, U.S. suppliers have regained EPROM market share; however, this share only relates to the lower 16K-through-256K mature densities. While Japanese EPROM suppliers pursued the higher 4Mb, 8Mb, and 16Mb EPROM densities, the U.S. suppliers waged price wars against each other for market share instead of building technological infrastructure.

Successful vendors that choose to stay in the EPROM business will be those that continue to make product enhancements in speed, packaging, and power. Supplier staying power in the MOS EPROM market during the next decade will be a true test of a company's quality of management, strength of financing, and product innovation.

Mary A. Olsson

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Research Newsletter

SIS MEMORY QUARTERLY NEW PRODUCTS NEWSLETTER

This newsletter contains a synopsis of memory product news events gathered from the trade press and company releases brought to Dataquest's attention during the second quarter of 1991. Significant developments include the availability of 4Mb SRAMs, 10ns 256K SRAMs, 8ns 64K SRAMs, 90ns flash devices, an 8Kx9 monolithic FIFO, and important speed upgrades in both FIFOs and dual-port RAMs. Table 1 shows the new products announced during the second quarter of 1991.

DRAM DEVELOPMENTS

Micron Technology

Micron has announced that it is currently taking orders for a recently qualified MIL-STD-883 version of its 80ns 1Mx4 device.

In another announcement, the company disclosed a manufacturing agreement allowing Sanyo to manufacture Micron's 64Kx16 design in Japan. The agreement exchanges the design and process technology for undisclosed royalties. Finally, Micron introduced JEDEC standard DRAM cards in both 4 and 8MB configurations, organized as either 1-2Mx36 or 2-4Mx18 bits. These devices are expected to sample in the third quarter of this year and will be followed by smaller 2MB configurations (256Kx36, and 512Kx18).

NEC

More than 50 varieties of 16Mb DRAM are planned for introduction by NEC beginning this summer. Engineering samples of 16Mx1 and 4Mx4 devices were delivered in March.

TABLE 1
New Memory Products—Second Quarter 1991

Company	Density/Description	Speed
DRAM Developments		
Micron	4Mb military	70ns
	4MB memory card	
	8MB memory card	
Sanyo	1Mb (Micron licensee)	
Toshiba	1Mb video RAM	80ns
SRAM Developments		
Cypress	64K, BiCMOS	8ns
	16K, ECL	6ns
	64K, ECL synchronous	
EDI	1Mb	25ns
	256K	15ns
	256K, synchronous	12ns

(Continued)

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TABLE 1 (Continued)
New Memory Products—Second Quarter 1991

Company	Density/Description	Speed
SRAM Developments (Continued)		
Hitachi	4Mb, pseudo static, 3V	120ns
IDT	16KB RISC cache module	33 MHz
	2Mb modules	15ns
	1Mb modules	15ns
	128KB, i486 cache module	50 MHz
	64K	8ns
	2Mb module	15ns
	512K module	10ns
Logic Devices	256K	16ns
Micron	1Mb	20ns
	256K	15ns
	64K	10ns
	256K, latched	15ns
	256K, synchronous	15ns
	1Mb	20ns
Motorola	256K	10ns
NEC	4Mb	55ns
Paradigm	4Mb module	20ns
Sharp	1Mb low power	100ns
Toshiba	4Mb pseudo static	70ns
	1Mb	85ns
Nonvolatile Memory Developments		
AMD	512K flash	90ns
	256K flash	90ns
Cypress	512K EPROM	20ns
Intel	1Mb block-erase flash	120ns
Xicor	1K serial EEPROM	
	8K serial EEPROM	
	2Mb EEPROM	
	64K microcontroller EEPROM	
Specialty Memory Developments		
IDT	FIFO	25ns
	FIFO modules	30ns
	Dual-port SRAM	25ns
	FIFO	15ns

Source: Various Publications, Dataquest (August 1991)

Texas Instruments

Karl M. Guttag, a TI fellow and graphics strategy manager, was awarded the National Computer Graphics Association's Award for Technical Excellence for leading the TI team that defined the video RAM (VRAM).

Toshiba Corporation

Toshiba has introduced a third-generation, 80ns 1Mb video RAM in both 128Kx8 and 256Kx4 configurations. Standard devices are available in addition to versions that boast several added features such as persistent write per bit, in support of the TI TMS34020 graphics processor, block write, flash write, and split transfers. All versions of the devices are in full production.

In another announcement, Toshiba revealed the development of a new e-beam process technique that reduces 0.25-micron mask layer calculation by almost three orders of magnitude. This process reduces the time required by current computing equipment to draw all layers of a 1Gb DRAM from months to a day or two.

SRAM DEVELOPMENTS

Cypress Semiconductor

Cypress has announced a technology transfer with National Semiconductor wherein Cypress' Aspen subsidiary will produce National's ECL I/O 6ns 2Kx9 SRAM in both ECL 100K and ECL 101K versions. Under this agreement, Cypress will also receive the right to manufacture National's 8Kx9 synchronous ECL I/O SRAMs.

Cypress has announced that it is now shipping first product from its new Bloomington, Minnesota, fab, which was purchased from Control Data Corporation. Cypress Minnesota Inc.'s first product was a high-speed SRAM used by Network Systems Inc., also of Minnesota.

Cypress Semiconductor and IDT

Cypress and IDT both have independently announced the availability of 8ns 64K TTL-I/O BiCMOS SRAMs. Both are targeted at the 40-MHz R3000 RISC microprocessor. Several versions of both companies' devices are slated for production, with common I/O versions with and without output-enable pins in current production.

Cypress and IDT also announced new 8Kx8 BiCMOS SRAMs having access times of 9ns, and 10ns, respectively.

EDI

EDI has announced two new commercial 1Mb SRAMs and four synchronous 256K SRAMs, both targeted at the commercial market. The 1Mb devices are offered in 256Kx4 and 128Kx8 organizations, in both SOJ and 400-mil ceramic DIP packages. Both organizations run at 25ns and are in production.

The synchronous devices are offered in either a 64Kx4 or a 16Kx16 configuration. The 64Kx4 device can be procured either with (12ns) or without (15ns) registers, and the 16Kx16 device operates at 17ns and can be ordered with or without latches. These four 256K-bit devices are now being shipped under a second-source agreement with Motorola and a development agreement with Sharp.

Hitachi

Hitachi is shipping samples of a 3-volt 4Mb pseudo-static RAM. The device is organized as 512Kx8 bits and is packaged in a 525-mil 32-pin SOIC. Access times are as fast as 120ns, and power consumption is reportedly 12 to 30 percent lower than competing devices.

Integrated Device Technology

IDT has announced several SRAM modules including processor-specific caches and general-purpose high-density SRAMs. One processor-specific device is a resettable dual 16KB cache module for R3000 RISC processors with clock speeds of up to 33 MHz. The reset feature is expected to be used as a consistency mechanism between cache and main memory, especially in multiprocessing systems. Another module is aimed at the Intel i486 and supports zero-wait caches at speeds up to 50 MHz. A 128KB cache increment can be added by plugging in a 72-pin SIMM. Both cache modules are now in production.

Standard 256Kx8 and 256Kx9 15ns modules in smaller packages than the JEDEC standard were also announced and are currently available. Speed upgrades were announced for three wide modules, a 16Kx32 ZIP (10ns), a 64Kx16 DIP, and a

64Kx32 SIMM (both now at 15ns). Samples of all three are now available, with production slated for the third calendar quarter.

A module that incorporates an R3000 RISC CPU, 32KB of instruction cache, and either 16 or 32KB of data cache, and can be obtained either with or without a floating point coprocessor, became available this April. This module is a means of simplifying high-speed cache design in RISC-based embedded systems where space is at a premium. Clock speeds of up to 33 MHz are supported.

Logic Devices Inc.

Boasting the capability of supporting future 50-MHz speeds of the SPARC RISC microprocessor, Logic Devices announced its alternate-source design of the Cypress 16Kx16 SPARC cache RAM. The plug-compatible part is offered in 33, 24, 20, and 16ns speed grades to support SPARC clock speeds of 25, 33, 40, and 50 MHz, respectively. Production volume is now available.

Micron Technology

Two 16Kx16 and two 16Kx18 fast static RAMs were announced this quarter. Both organizations are offered either with latched inputs or with input registers. The x16 parts are equivalent to existing Motorola products, and the x18 versions are similar with the addition of parity bits. The press release did not mention if the x18 versions conformed to the JEDEC standard x18 pinout. All four parts come in 52-lead PLCCs or small-footprint PQFPs and are available as engineering samples at speeds as fast as 15ns.

Micron also has introduced a monolithic 128Kx8 in a 400-mil DIP package with only a single chip select. Although most monolithic devices have two chip selects, the industry-standard module has only one. The single-chip select pin of Micron's 128Kx8 allows its new monolithic device to be pin-compatible with the industry-standard 128Kx8 module. Speeds of up to 20ns are in production.

Speed upgrades have been performed on all densities of Micron's standard SRAM family. The 64K density is now offered at 10ns, 256Ks are as fast as 15ns, and the megabit is now offered at 20ns. The megabit and 256K densities are in production, with the 64Ks sampling to go into production in the third quarter.

Micron is now making its megabit and 256K products available in die form, all tested to speed via hot chuck testing. Fastest guaranteed speeds are 25ns for the megabit, and 20ns for the 256K devices. The dice, as well as all of the previously mentioned products, are offered in four temperature ranges: commercial, industrial, automotive, and military.

Motorola

Motorola has introduced 10ns versions of its 32Kx8 and 64Kx4 SRAMs. These SRAMs have been manufactured using Motorola's 1.0-micron triple-metal BiCMOS process. Samples are now available, with production scheduled for late in the second quarter.

NEC

Samples of a 55ns low-power 4MB SRAM have been shipped by NEC. The device is aimed at notebook and laptop PCs and consumes only 0.4µA when in standby mode.

Paradigm Technology

Paradigm announced a 4Mb 20ns SRAM module, reportedly the first of a forthcoming family. The 512Kx8 device is constructed using Paradigm's own 128Kx8 SRAM chips. Availability information should be requested from Paradigm.

Sharp

Sharp will be increasing its monthly 1Mb SRAM production from a current rate of 100K to 500K units by the end of the year. The 20ns version, which has been shipping in the United States, has just begun shipment in Japan.

In May, the company sampled a 100ns, 1Mb SRAM with power consumption reported to be only 20 percent of that required by existing devices. This product ships in a 32-pin DIP, SOJ, and TSOP.

Sharp plans to sample 4Mb SRAMs this fall and should enter production in the spring of 1992.

Toshiba

Toshiba America has introduced a 70ns, 4Mb pseudo-static RAM in a 512Kx8 organization. The

JEDEC-standard pinout used by this device is an upgrade to the pinout of a standard 400-mil 128Kx8. These devices are in full production and are targeted at such applications as laptop PCs and hand-held instrumentation.

Toshiba also has announced a low-power 128Kx8 standard SRAM with a typical power dissipation of 27.5mW per MHz and a maximum standby current of 30 microamperes. Designed for battery backup applications such as bar code readers and volt meters, the SRAM runs at speeds as fast as 85ns and is in full production in JEDEC standard 600-mil DIP and 525-mil SOP packages.

NONVOLATILE DEVELOPMENTS

Advanced Micro Devices Inc.

AMD has announced what it claims to be the industry's fastest 64Kx8 and 32Kx8 flash devices, featuring 90ns access times. They are packaged in 32-pin DIP and PLCC packages to facilitate upgrades to higher densities. These devices follow the Intel/AMD convention for 12-volt programming, the same as followed in both companies' 1Mb devices. The 64Kx8 is in volume production, and the 32Kx8 was to go into volume production by the end of the quarter.

Cypress Semiconductor

Cypress Japan is now sampling a 512Kb EPROM whose access time is 20ns for any address within a 64-byte range but is 65ns whenever a 64-byte boundary is crossed. This device is being marketed as a support component for the SPARC processor in embedded applications.

Fujitsu

Fujitsu plans to enter the flash market with a 16Mb device that is expected to sample at the end of 1992.

Intel Corporation

A novel architecture of flash memory has come out of Intel. Although the part is in a 128Kx8 organization, it is split into an 8Kx8 segment, two 4Kx8 segments, and a 112Kx8 segment. The 8Kx8 segment has a hardware lockout feature to allow a BIOS bootstrapping routine to be locked into the memory. Intel hopes that designers will use this single component to replace several devices (EPROM, EEPROM, and battery-backup SRAM) within their systems. Packaged in DIP, PLCC, and TSOP packages, 120ns and slower versions are now in production in two varieties: one whose lockout segment is in the top part of memory and one with this segment at the bottom.

Xicor Inc.

Xicor introduced two serial I/O EEPROMs in 1Kb and 8Kb densities. The devices are pin-compatible with each other, and their simple two-wire interface allows devices of 1, 2, 4, 8, or 16Kb to be inserted into the same 8-pin socket. Both parts are in production now and operate over either the commercial or industrial temperature ranges using a 3.3V +/- 10 percent power supply.

Another product is Xicor's new 8Kx8 EEPROM, with address and data multiplexed to the same pins in order to support the needs of Motorola microcontrollers. Control pins have been optimized to simplify connecting this product to Motorola's line of microcontrollers. According to Xicor, the part is now in production.

Xicor's third announcement was for a 256Kx8 EEPROM module in a JEDEC standard DIP pinout. Composed of four Xicor 64Kx8 monolithic EEPROMs, the module is in production. Xicor claims that this device is the densest EEPROM on the market today.

SPECIALTY DEVELOPMENTS

Integrated Device Technology Inc.

On the FIFO front, IDT has introduced one new FIFO, speed upgrades of three existing FIFOs, and a FIFO module family. IDT's 9-bit wide FIFOs in 256, 512, and 1K depths were all upgraded from 25ns to 15ns and 20ns speed grades, with production now available. An 8Kx9 25ns asynchronous FIFO, which IDT claims is the deepest in the industry, was announced for immediate availability. This deep device is intended to simplify design and reduce board space in high-resolution graphics boards and data acquisition systems. Finally, FIFO modules in 8/16/32Kx9 and 16/32Kx18 organizations were announced. All devices are now available in 30ns speed grades.

A new 25ns speed grade of 10 current IDT dual-port RAMs was announced. Production

quantities are now available for 25ns version upgrades of IDT's master and slave 1Kx8s, 2Kx8s, and 2Kx8s with interrupt. The master and slave 1Kx8 and 2Kx8 devices are now also being offered in a center power/ground DIP pinout to reduce internal noise and ground bounce.

Jim Handy

This newsletter is meant to be used as a reference guide of new products for competitive analysis, to monitor technology trends, and to track future developments and improvements. Dataquest assumes no responsibility for the accuracy of the contents.

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Research Newsletter

IBM AND SIEMENS SIGN AGREEMENT TO MANUFACTURE 16Mb DRAMs

SUMMARY

On July 4, 1991, IBM and Siemens signed an agreement to manufacture 16Mb DRAMs at IBM's fab in Corbeil-Essonnes (France). This agreement will capitalize on the technology of both companies and enable them to implement the latest semiconductor manufacturing technology in Europe. This agreement is part of an ongoing effort to strengthen an independent European electronics industry, and it will also allow both companies to transfer this technology to other manufacturing sites.

In 1990, both companies introduced 16Mb DRAM samples. However, as a result of this agreement, 16Mb DRAMs with increased functionality will be developed at a Siemens facility in Munich. Dataquest estimates that Siemens will contribute between $400 million and $600 million for design and equipment, and IBM will contribute the manufacturing process technology and fab. This is IBM's biggest joint-manufacturing agreement and exemplifies the action that major semiconductor manufacturers are taking to reduce the risk and cost associated with a new submicron state-of-the-art fab.

MANUFACTURING PLANS

Manufacturing will begin by the end of this year with shipments scheduled to begin in the second half of 1992. An existing IBM facility is being upgraded to handle the strict contamination control required to manufacture these devices. The upgrade is based on Dr. Ohmi's ultraclean technology. A Dr. Ohmi-specified fab includes a Class 1 clean room; electrostatic discharge control; and high-purity chemical, gas, and DI water delivery systems. Dataquest estimates that a Dr. Ohmi-specified clean room costs about $2,900 per square foot. When fully operational, the facility will employ a total of 600 people, roughly 300 from each company.

The manufacturing process is based on existing IBM process technology developed at Corbeil-Essonnes. Dataquest estimates that between 375 and 525 process steps are required to manufacture a 16Mb DRAM. The manufacturing test vehicle used to bring up the line will be an IBM device. However, this device was designed for mainframe computer applications. Therefore, after the line is up and running, the newly designed Siemens 16Mb DRAM with increased functionality will be manufactured. When fully equipped, the fab will have the capacity to start 12,000 8-inch wafers per month. The fab will also have the capability to produce ASIC products that feature linewidths of 0.5 micron.

WHERE THE CHIPS ARE GOING

IBM plans to retain the chips for captive use, and Siemens plans to sell the chips on the merchant market. This strategy will enhance Siemens' product line and guarantee its customers DRAM availability. If excess capacity is available, participation by other companies will be allowed in this agreement.

Last year, IBM and Siemens also entered into a 64Mb DRAM agreement. This agreement is of strategic importance to both companies; the following section analyzes its strategic importance.

LAST YEAR'S 64Mb DRAM AGREEMENT

On January 23, 1990, IBM and Siemens signed an agreement to develop 64Mb DRAMs. This agreement focused on process-technology

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development and chip design. Both IBM and Siemens decided that the cost of developing the new process technology required to make leading-edge DRAMs is too risky and costly to do alone. As a result, IBM and Siemens entered into an agreement in which they would share equally in 64Mb DRAM technology development costs. They each dedicated 100 engineers to this project. No financial transaction took place between the two companies.

The goal of the agreement is to introduce a 64Mb DRAM into volume production in about 1995. Before this agreement, Siemens' goal was to complete 64Mb DRAM development by 1995. With IBM's help, this goal could be achieved one year early, which is of strategic importance because time to market is critical in today's environment. In the DRAM market, the best profit margins occur during the first year a chip is in volume production. This is the point at which demand is strong and supply is tight.

As a starting point for this agreement, each company disclosed its strengths and weaknesses as they relate to DRAM production. Although a common process and product are being developed, each company will manufacture and market the 64Mb DRAMs separately. IBM plans to manufacture the 64Mb DRAMs in Essex Junction, Vermont, and Siemens plans to manufacture in Munich and Regensburg, Germany. As with the 16Mb DRAM agreement, IBM will use the chips for captive purposes and Siemens will expand its device product line offering.

IBM and Siemens both use a trench capacitor for the 64Mb DRAM process rather than the stack capacitor process. The trench capacitor will most likely be used for higher-density designs. This deal is not a technology-transfer arrangement but a codevelopment arrangement that will give both companies equal ownership in the process and base product.

JOINT VENTURES—A WAY OF LIFE

Dataquest believes that the 1990s will bring a substantial amount of joint-venture activity. This increase in activity is being driven by escalating fab and equipment costs. Even the giant semiconductor manufacturers are managing their financial resources more carefully than in the past. This section briefly describes two other unrelated recently announced joint ventures that illustrate this point.

A significant joint venture was announced in April 1991. Texas Instruments, Hewlett-Packard, Canon, and the Singapore Economic Development Board announced that they will form a venture that will use submicron CMOS manufacturing technology to manufacture DRAMs. The fab being constructed for this venture will also have the capability to manufacture advanced logic if market demand shifts.

Also in April, a joint-development agreement was reached between AT&T Microelectronics and NEC that will have a positive impact on U.S.-Japan trade relations. The purpose of this agreement is to reduce the risks and costs associated with developing a 0.35-micron process. Twenty-six research teams were assembled to carry out this agreement. AT&T plans to incorporate the results of this agreement into its new fab in Orlando, Florida, which will incorporate microenvironments. The most important aspect of this agreement is that AT&T and NEC will have the same process and tool set, which means that they can second-source each other's products. This is truly second-sourcing for ASIC customers.

In 1990, Dataquest ranked NEC number 1 with semiconductor revenue of $5 billion, and AT&T was ranked number 20 with semiconductor revenue of $830 million. It is evident that if these financially sound companies are entering into agreements to reduce cost and risk, the others will have to follow.

DATAQUEST PERSPECTIVE

The Siemens/IBM 16Mb DRAM agreement increases the chances of Siemens remaining a contender in the fiercely competitive DRAM market. This is of strategic importance because Europe does not want to become dependent on foreign sources for its DRAMs. However, before this agreement, it was questionable if Siemens would have survived in the DRAM market by itself.

As semiconductor manufacturing complexity increases, agreements of this nature are mandatory to survival. Forces that make these agreements mandatory include the mammoth R&D investment required to design a chip such as the 16Mb DRAM, the huge initial capital investment required for manufacturing equipment and facilities, and the cost of capital.

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Jeff Seerley
Sam Young

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Research Newsletter

DRAM SUPPLIER ANALYSIS

This newsletter analyzes the product and market strategies of leading DRAM suppliers. It covers each company's DRAM market ranking, product/technology positioning, strategic direction, and related issues.

Current or prospective users of megabit-density DRAMs must be aware that the highly competitive early stages of the DRAM product life cycles—an intense R&D period followed by a short introductory phase—often mean a sharp competitive advantage for early entrants, who are able to enjoy premium pricing through the introduction and growth phases. The extended maturity phase eventually tips the competitive balance to low-cost producers. This reality serves as the background on analysis of the 1Mb and 4Mb DRAM supplier base.

Table 1 shows the 1990 worldwide ranking of DRAM suppliers as measured in dollarized units. The table presents each company's ranking in terms of units for densities from 64K through 4Mb. It also shows which suppliers have sampled 16Mb DRAMs as of July 1991.

As noted, early leadership for the next-generation product often signals future DRAM market leadership. Dataquest restates what we said previously: For users looking ahead, Dataquest expects the 1992 to 1993 total ranking to be strongly influenced by 4Mb DRAM ranking.

TOSHIBA

As shown in Table 1, which is based on 1990 worldwide dollarized units, first-ranked Toshiba holds first-place ranking in 1Mb DRAMs and second in the 4Mb product area. The industry giant held the number one spot in the 4Mb segment during 1989; however, during 1990 Toshiba adjusted to a 4Mb DRAM market shift from a 350-mil-wide device—the 4Mb part with which it started—to the now industry-standard 300-mil part. Toshiba should remain a leader in the DRAM market for the foreseeable future.

As shown by Toshiba's huge state-of-the-art DRAM fab network, this vertically integrated supplier positions itself at the leading edge of DRAM technology. In the 1991 to 1992 time frame, the company will emphasize the 4Mb DRAM density and de-emphasize 256K DRAMs and 1Mb DRAMs. The product portfolio includes high-speed DRAMs (60ns or faster), wide-word configurations (e.g., ×8, ×9, ×16, ×18), and SIMMs. As of mid-year 1991, 16Mb DRAM samples are available. Toshiba is a leading supplier of 1Mb VRAMs (e.g., 256K×4, 128K×8) and should be a major player in the 4Mb VRAM segment as that market emerges.

SAMSUNG

Second-ranked Samsung of the Republic of Korea continues an impressive advance in the global DRAM marketplace, moving one notch higher in the ranking during 1990 versus its third-place ranking for 1989. Table 1 reveals that Samsung ranks first in the older 64K and 256K segments, which is no surprise, but somewhat surprisingly ranks second in the maturing but still mainstream 1Mb segment. A key factor is that the company has used its vertically integrated structure to emerge as a low-cost DRAM producer.

Samsung strives to position itself as a DRAM technology leader. As shown by its sixth-place ranking in the 4Mb segment, Samsung still lags leaders such as Hitachi and Toshiba. A strategic factor—the goal of maintaining a reputation for DRAM product quality—partially accounts for the sixth-place ranking. The sound strategy caused Samsung to be conservative in terms of bringing

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Table 1
Top Worldwide DRAM Suppliers[1]

Supplier	1990 Total Ranking[2]	Ranking by Density[3] 64K	256K	1Mb	4Mb	16Mb[4]
Toshiba	1		12	1	2	S
Samsung	2	1	1	2	6	S
NEC	3		2	3	3	S
Hitachi	4		12	6	1	S
Fujitsu	5		9	4	4	S
Texas Instruments	6	2	4	5	10	S
Oki	7	3	3	9	7	S
Mitsubishi	8		8	8	5	S
Micron	9	4	7	10		
Motorola	10		18	7	11	
NMB	11		5	12	12	S
Siemens	12		16	11	8	
Matsushita	13	5	14	12	8	S
Hyundai	14		6	15		
Intel	15		16	14		
Vitelic	16		10	18		
Goldstar	17		11	18		
Sharp	18		15	17		
Sanyo	19		19	16		
Total (Million of Units)		24	617	728	30.3	0

[1] In terms of "dollarized units," which represent the sum of all units sold by a company weighted by each DRAM density's 1990 worldwide ASP
[2] Includes VRAMs
[3] In units
[4] Samples as of July 1991
Source: Dataquest (September 1991)

the complex 4Mb DRAM device to market during 1990.

Users can continue to look to Samsung for 1Mb DRAMs during 1991 and 1992. The product portfolio includes SIMMs (e.g., 1Mb×8, 1Mb×9), and some users of 64K DRAMs and 256K DRAMs can forge long-term supply arrangements with this supplier. Users can expect a competitive 4Mb DRAM product line from Samsung including wide-word configurations (e.g., ×8, ×9, ×16, ×18) and SIMMs. Table 1 shows that 16Mb DRAM samples have been available as of midyear 1991.

In order to protect its long-term position in the worldwide DRAM arena, Samsung must avoid trade friction, which will be challenging. For example, this supplier, along with other Korean companies, is being investigated for alleged dumping in Europe.

NEC

NEC, ranked third overall, holds third-place ranking in the 1Mb DRAM and 4Mb DRAM segments and second ranking in the declining 256K arena, as shown in Table 1. Users can expect NEC to de-emphasize 256K and 1Mb DRAMs during the 1991 to 1992 period.

In line with prior history, NEC continues to act from a DRAM technology "catch-up position" in a learning-curve-dominated segment of the semiconductor business. The vertically integrated company has in the past successfully executed this somewhat risky strategy by supporting superior manufacturing planning with "deep-pockets" financial strength. An early leader in the 4Mb market, NEC should remain a top worldwide DRAM supplier.

NEC's strategy for 1991 and beyond focuses on success at DRAM densities of 4Mb and greater. Users of 4Mb DRAMs can look to NEC for a competitive product portfolio: high-speed 4Mb DRAMs, wide-word configurations (e.g., ×8, ×9, ×16, ×18), and SIMMs. NEC should make an orderly migration from 1Mb VRAMs such as the 256K×4 device to 4Mb VRAMs in line with market demand trends.

HITACHI

Hitachi ranks fourth among DRAM suppliers—the same ranking as in 1989—but ranks *first* at the critical 4Mb level (see Table 1). As with other leading Japan-based suppliers, users can expect Hitachi to de-emphasize 256K and 1Mb DRAMs during 1991 and 1992. Users can look to Hitachi for 256K VRAMs (e.g., 64K×4), 1Mb VRAMs (e.g., 256K×4, 128K×8), and SIMMs (e.g., 1Mb×8, 1Mb×9). The supplier will make an orderly move to the 4Mb VRAM when demand grows.

As a former top player in the DRAM business, Hitachi's strategy calls for an aggressive effort to win the 4Mb market battle and the concomitant market stature. Along with DRAM design know-how, manufacturing prowess, and marketing skill, users can expect Hitachi to display the device speed and packaging technology expertise that previously enabled the company to achieve effective DRAM product differentiation.

Hitachi's competitive 4Mb DRAM product portfolio offers wide-word configurations (e.g., ×8, ×9, ×16, ×18), SIMMs, and high-speed DRAMs. Samples of 16Mb DRAMs reflect Hitachi's future strategic direction.

FUJITSU

Table 1 shows that Fujitsu held the same ranking in 1990 as in 1989—fifth place. As a vertically integrated supplier, a high percentage of captive DRAM demand shields Fujitsu somewhat from DRAM merchant market volatility. Users can look to Fujitsu for VRAMs (e.g., 64K×4) and SIMMs (e.g., 1Mb×8, 1Mb×9, 256K×36). This company will place less emphasis on 256K and 1Mb DRAMs during 1991 and 1992.

As indicated by its fourth-place ranking, to some extent Fujitsu is playing catch-up in the 4Mb segment. In terms of technology, the supplier emphasizes the thin small-outline package (TSOP) for the 4Mb and 16Mb devices in line with the market trend toward higher pin-count packages.

Although not the 4Mb DRAM technology leader, users can look to Fujitsu as a dependable and competitive supplier of 4Mb DRAMs during 1991 and 1992. The product portfolio will be familiar and competitive: SIMMs, wide-word configurations (e.g., ×8, ×9, ×16, ×18), and high-speed choices.

TEXAS INSTRUMENTS

Sixth-ranked Texas Instruments (TI) continues to hold the same ranking as in 1989. Table 1 reveals that this company ranks second in the 64K segment, fourth at the 256K density, fifth in the 1Mb arena, and tenth in the critical 4Mb business. It pursues the same strategic direction during the second half of 1991 as other leading DRAM suppliers—to emphasize 4Mb DRAM production and de-emphasize lower-density devices.

The company is leaving the 64K business. Current TI customers that use 256K devices should be able to forge special supply arrangements. TI will be de-emphasizing the 1Mb device during the 1991 to 1992 period; however, the pace of the trend will depend on events in the 4Mb arena. If the market moves quickly to the 4Mb product, the 1Mb part will be more quickly de-emphasized. If the 4Mb trend stalls—as has already occurred at times—TI will likely shift some support to users of the 1Mb device.

The supplier offers a competitive 4Mb DRAM product portfolio that includes wide-word configurations (e.g., ×8, ×9, ×16, ×18) and SIMMs. As the market shifts over time to 4Mb VRAMs, TI will migrate from the current line of 256K VRAMs (e.g., 64K×4 devices) and 1Mb VRAMs such as the 256K×4 part. Currently, 16Mb samples are available.

To maintain its long-term stake in the competitive megabit-density DRAM market, TI's strategy calls for the forging of alliances and other arrangements for sharing the risks and benefits of participation in this worldwide business. One example is an alliance among Canon, Hewlett-Packard, TI, and the government of Singapore for production/consumption of DRAMs in Singapore. Another example is a prior venture between TI and the Italian government on a megabit-density DRAM fab in Italy. At the time this newsletter was written, the TI-Acer fab in Taiwan had just started 4Mb DRAM production.

A second prong of TI's DRAM strategy calls for aggressive protection of its DRAM/IC patent portfolio via litigation or negotiation toward the goal of collecting royalty payments.

OKI

Oki has consistently ranked seventh or eighth among worldwide DRAM suppliers since 1988. Table 1 reveals that seventh-ranked Oki ranks third in the 64K and 256K segments, ninth at the 1Mb density, and seventh in the emerging 4Mb arena.

In addition to 4Mb DRAMs, Oki's strategy emphasizes SIMMs, with a trend toward SIMMs based on the 4Mb device. Users can expect Oki to de-emphasize 64K DRAMs and 256K DRAMs. The 1Mb device will also be de-emphasized, except for some use in SIMMs.

For example, Oki's 1Mb SIMM product portfolio includes modules organized as follows: 1Mb×8, 1Mb×9, 1Mb×32, and 1Mb×36 as well as 2Mb versions (e.g., 2Mb×36). The trend is toward expanding use of 4Mb DRAMs in these SIMMs. For example, in prior years the 1Mb×8 SIMM used eight 1Mb×1 DRAMs. Increasingly, Oki and other SIMM suppliers base this module on two 1Mb×4 DRAMs and one 1Mb×1 DRAM.

Users can expect Oki to be a leader in the migration of the market to 4Mb SIMMs (e.g., ×8, ×9, ×32, ×36, and evolving organizations). Oki also offers 16Mb DRAM samples.

MITSUBISHI

Table 1 shows that Mitsubishi, ranked eighth overall, ranks eighth in the 256K and 1Mb segments but fifth in the critical 4Mb arena. This supplier's overall DRAM ranking has declined somewhat in recent years, which might be deceptive.

Dataquest restates what we stated in the *DRAM Product Trends* service section dated August 1990: "The competitive advantage of Mitsubishi's process and packaging technology expertise is likely to grow more significant as the industry moves to the 16Mb and 64Mb densities." Success in the 4Mb DRAM business can serve as a long-term indicator of long-term survival—and the Mitsubishi strategy to some extent already signals 4Mb success.

Mitsubishi's typical but competitive 4Mb DRAM product portfolio includes high-speed DRAM and wide-word configurations (e.g., ×8, ×9, ×16, ×18). Currently, 16Mb DRAM samples are available.

MICRON

As shown in Table 1, ninth-ranked Micron ranks fourth in the 64K DRAM segment, seventh in the 256K density, and tenth in the 1Mb market. The company broke into the top 10 tier of DRAM suppliers in 1990.

One prong of Micron's strategy calls for cost-oriented competitive ability, meaning that the product portfolio is weighted toward mature DRAM devices with densities of 1Mb and below. For these mature devices, the market typically favors low-cost producers such as Micron. Users of 256K DRAMs, 1Mb DRAMs including 64K×16 configuration, VRAMs (e.g., 256K×4, 128K×8), and SIMMs (e.g., 1Mb×8, 1Mb×9, 256K×9, 256K×36) can look to Micron during the 1991 to 1992 period. Users of 64K DRAMs should be able to forge special long-term supply arrangements with Micron.

As indicated by the 4Mb DRAM ranking, Micron is not a DRAM technology leader like Hitachi or Toshiba. Even so, a second prong of the company's strategy—to serve specialty applications—is leadership in a sense. For example, in addition to mainstream 1Mb devices, users can look to Micron for 64K×16 DRAMs, 256K×4 VRAMs, and 128K×8 VRAMs. Users can also expect Micron to become an increasing force in the 4Mb DRAM segment as the product nears the maturity stage of the life cycle.

MOTOROLA

Tenth-ranked Motorola slipped one notch during 1990 from its ninth-place position in 1989. As shown in Table 1, Motorola ranks seventh in the 1Mb segment and eleventh in the 4Mb market. Motorola departed the mainstream 256K arena. SIMMs such as the 1Mb×8, 1Mb×9, 256K×9, and 256K×36 modules represent a key aspect of the product portfolio.

Motorola has used an alliance with Toshiba as part of its DRAM strategy. The agreement started for product densities of 4Mb and below and eventually also applied to densities of 16Mb and above. The industry giant will emphasize 4Mb DRAMs but can remain responsive to market demand for 1Mb products.

NMB

Eleventh-ranked NMB positions itself as the leading supplier of high-speed DRAM devices that operate at speeds of 60ns and faster, which conforms nicely with the DRAM market trend. Table 1 shows that NMB ranks fifth in the 256K DRAM arena and twelfth in the 1Mb and 4Mb segments.

NMB relies heavily on a shifting set of strategic alliances for design technology and foundry service. The list of its alliance partners over time has included Alliance Semiconductor, Intel, Inmos (now owned by SGS-Thomson), Ramtron, and Vitelic.

SIEMENS

Twelfth-ranked Siemens slipped from the top 10 tier of DRAM suppliers during 1990. Table 1 shows that Siemens ranks eleventh in the 1Mb DRAM segment and eighth in the critical 4Mb business—an augur of future challenge.

A major strategic response for Siemens was the IBM alliance on 16Mb DRAMs that was announced in July 1991. This alliance augments a prior agreement between Siemens and IBM on 64Mb DRAMs. Even so, the 1991 to 1992 period will be critical in terms of Siemens' ability to grow its share of the European market for 1Mb/4Mb DRAMs and penetrate the North American marketplace.

SUPPLY BASE ANALYSIS

This section of the newsletter uses information on DRAM life cycles and suppliers to present a density-by-density evaluation of the supply base for these devices in the medium to long term. Figures 1 through 4 show the 1990 total market size in unit shipments and the shares of the leading suppliers of each density. This information correlates with information presented in Table 1.

Supply Base for 64K DRAMs

The 64K DRAM device is being phased out. Figure 1 shows that production of 64K DRAMs during 1990 totaled 24 million units—less than half of the 1989 volume.

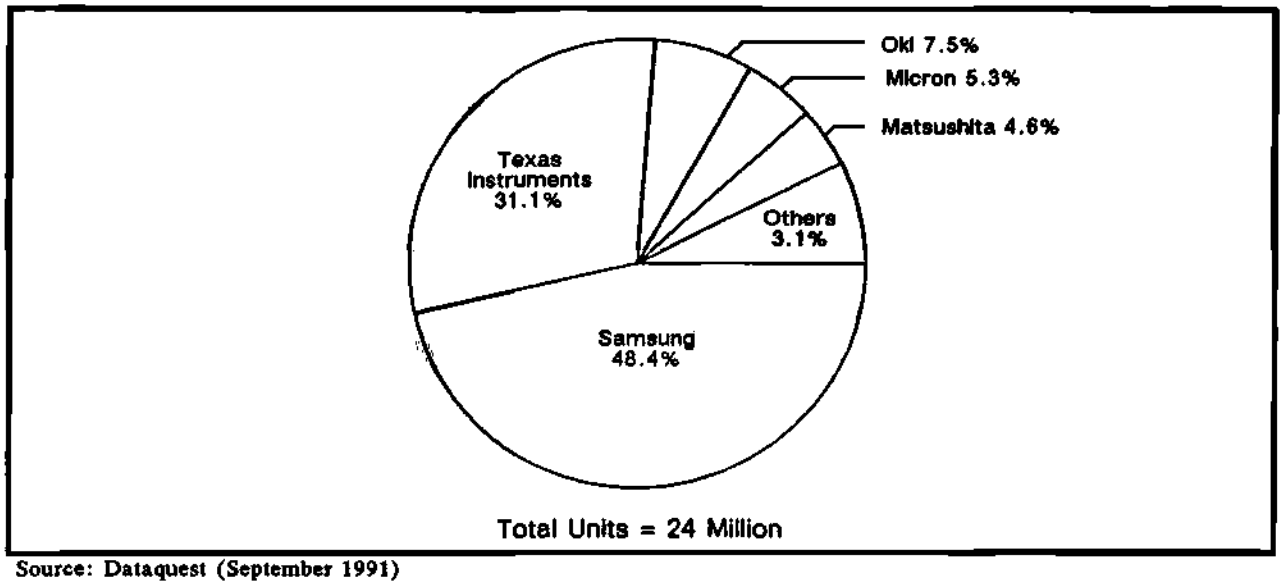
Dataquest recommends that users migrate from this device in system designs lacking a long-term procurement arrangement. Figure 1 shows that the leading suppliers are Samsung and TI; however, TI likely will limit support, if any, to long-term customers.

Supply Base for 256K DRAMs

Figure 2 lists the top-ranked 256K DRAM suppliers based on 1990 unit shipments.

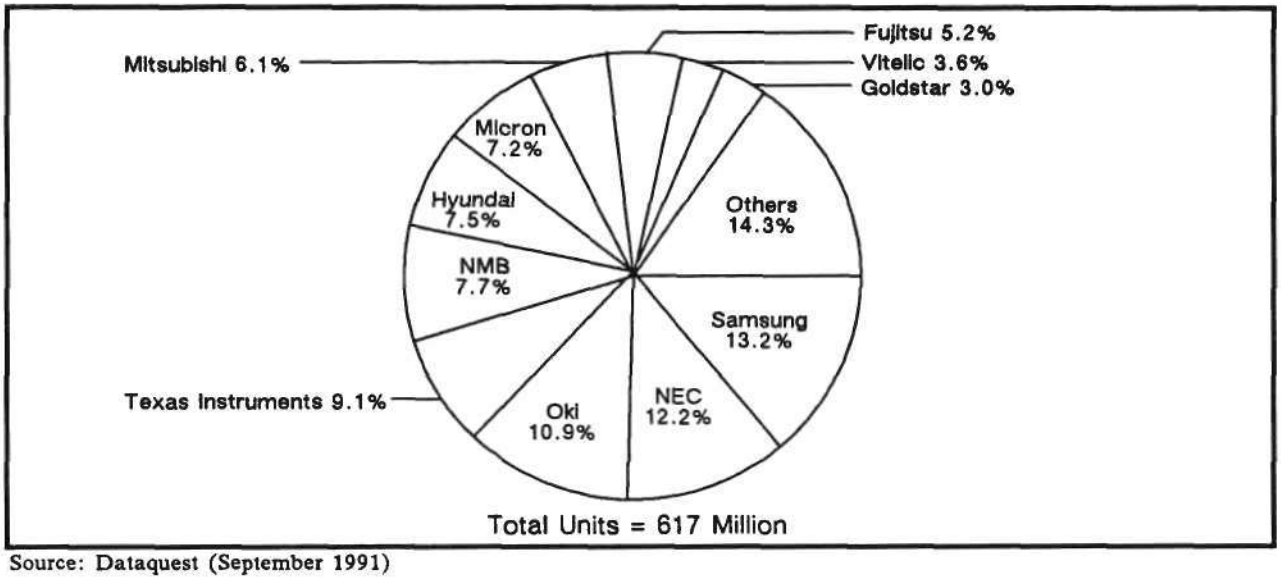
Figure 2 shows that leading suppliers in descending order are Samsung, NEC, Oki, TI, NMB, Hyundai, Micron, Mitsubishi, Fujitsu,

Figure 1
64K DRAM Supplier Base



Source: Dataquest (September 1991)

Figure 2
256K DRAM Supplier Base



Source: Dataquest (September 1991)

Vitelic, and Goldstar. Table 1 shows the full spectrum of suppliers.

Periodic Spot Shortages

The 256K DRAM product is moving through its decline stage. Worldwide production of 256K DRAMs for 1991 is expected to total 450 million units—that number may seem impressive, but in fact it is just half of the peak volumes of 1988 to 1989. Annual supply should exceed 100 million units through the year 1993; however, users should expect periods of spot shortage as suppliers make production cutbacks during the 1991 to 1993 time frame. For example, at the time this newsletter was written, planned cutbacks in production of 256K DRAMs by some suppliers signaled a supply crunch for late 1991 or early 1992.

Dataquest Recommendation

To minimize supply line disruption, users should be prepared to forge long-term supply arrangements with current suppliers or qualify new suppliers. The other alternative is to migrate to megabit-density DRAMs.

Suppliers likely to remain committed to the 256K segment include the following Korean companies, which increased market share during 1990: Goldstar, Hyundai, and Samsung. Micron has maintained its share of the 256K market and is likely to consider special supply agreements for some users. The life cycle for high-speed DRAMs lags general DRAM life cycles, so NMB should remain supportive to users of high-speed 256K DRAMs.

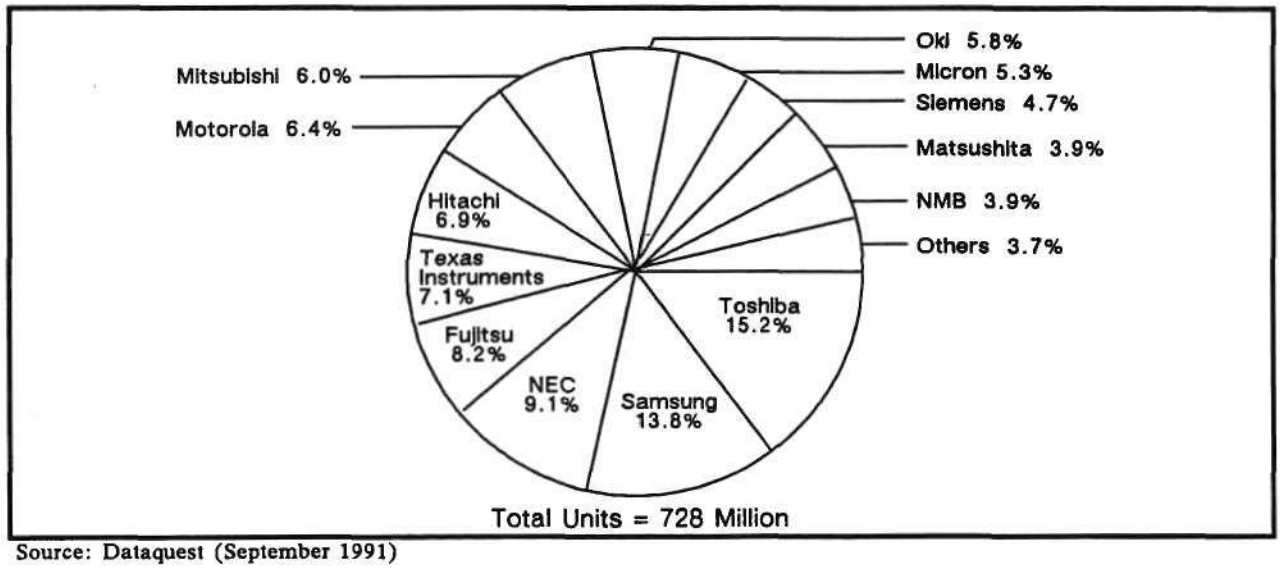
Supply Base for 1Mb DRAMs

Figure 3 presents the top-ranked 1Mb DRAM suppliers based on 1990 unit shipments. Figure 3 shows that the top-ranked suppliers in descending order are Toshiba, Samsung, NEC, Fujitsu, Texas Instruments, Hitachi, Motorola, Mitsubishi, Oki, Micron, Siemens, Matsushita, and NMB. Global production of 1Mb DRAMs totaled 728 million units in 1990.

An Adequate Supply of 1Mb DRAMs?

Users can expect the 1Mb DRAM to reach the peak stage—or saturation stage—of its life cycle during the 1991 to 1992 period with output exceeding 800 million units each year. Supply should decrease thereafter as the device moves along the decline stage of the curve, but it should still exceed 200 million units for the year 1995. Users can expect an adequate supply of 1Mb products during the 1990s, but only to the extent that users accurately forecast and "spec" product demand *and* also align themselves with an appropriate set of suppliers.

Figure 3
1Mb DRAM Supplier Base



Source: Dataquest (September 1991)

For example, under guidance from Japan's Ministry of International Trade and Industry (MITI), some Japan-based suppliers have shifted and will continue shifting capacity to 4Mb DRAMs. Other suppliers vacillate but will continue to support users of 1Mb DRAMs as warranted by market demand and price trends. Another set of suppliers fully intend to increase their share of the 1Mb DRAM marketplace during the 1991 to 1992 time frame.

User Alternatives to 1Mb DRAMs

The first alternative for users is to redesign systems and migrate to 4Mb DRAM, as many users are doing. For systems where redesign might be feasible although not urgent, the use of SIMMs provides a hedge alternative, especially with the 4Mb DRAM market still somewhat unsettled.

Some older system applications remain profitable, such that any system redesign might not be a feasible alternative. The following recommendation is targeted for users that expect to continue using 1Mb DRAMs.

Dataquest Recommendation

To establish a dependable supply of 1Mb DRAMs at competitive prices, users should forge annual purchase contracts and special supply commitments. Otherwise, users must be prepared to buy on the 1MB DRAM spot market, which is likely to be highly volatile and erratic.

Users must *now* reevaluate the 1Mb DRAM supplier base, deciding whether to keep or drop current suppliers and requalify new suppliers. In order to target 1Mb DRAM suppliers, look for suppliers that have recently increased or decreased market share. For example, the following suppliers increased market share by more than 2 percent in 1990: Fujitsu, Micron, Motorola, NEC, and Samsung. The Japan-based suppliers are likely to de-emphasize 1Mb output. Micron, Motorola, and Samsung are likely to continue emphasis on the 1Mb device during 1991 and 1992. Some suppliers also are likely to remain committed to serving demand for the 1Mb part—these supplers are Goldstar, Hyundai, Intel, Matsushita, NMB, and Sanyo. These companies increased market share, albeit by less than 2 percent, during 1990.

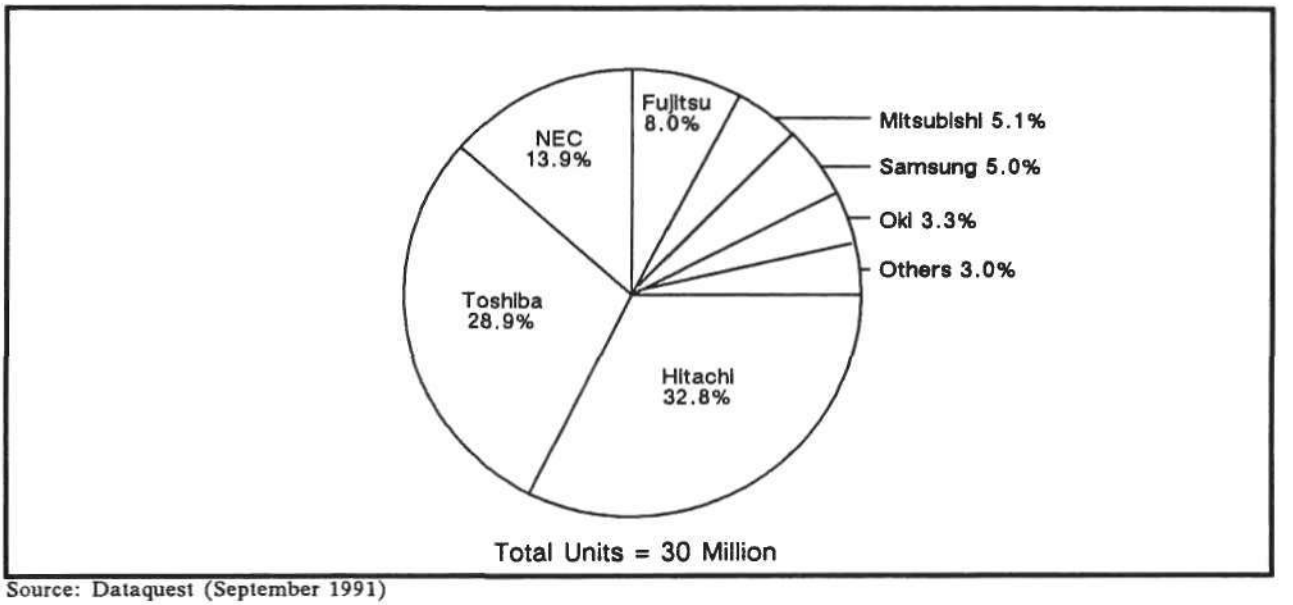
By contrast, the following suppliers lost more than 2 percent of market share during 1990: Hitachi, Mitsubishi, Oki, and Toshiba. Their emphasis will be on the 4Mb DRAM device. Sharp, Siemens, and Texas Instruments lost ground during 1990, but by less than 2 percent of market share. Siemens and Texas Instruments are increasing their roles in the 4Mb DRAM market but are watching 1Mb DRAM supply/demand trends.

Supply Base for 4Mb DRAMs

Figure 4 lists the top-ranked 4Mb DRAM suppliers in terms of 1990 unit share.

In descending order, the leading suppliers of 4Mb DRAMs are Hitachi, Toshiba, NEC, Fujitsu, Mitsubishi, Samsung, and Oki. Siemens, Matsushita, Texas Instruments, Motorola, and

Figure 4
4Mb DRAM Supplier Base



Source: Dataquest (September 1991)

NMB hold less than 1 percent of 1990 market share. Other suppliers such as Micron are joining the fray. Although the 4Mb DRAM race is just ramping up, Hitachi and Toshiba have positioned themselves early for long-term success.

As shown in Figure 4, global 4Mb DRAM production totaled 30 million units in 1990. The 4Mb DRAM device is now moving through the growth stage of the life cycle. Supply should exceed 100 million units during 1991. The peak maturity stage of the life cycle should be reached during the 1994 to 1995 time frame, when annual output should exceed 800 million units. The 4Mb DRAM life cycle should extend to the end of this decade.

Dataquest Recommendation to Current and Prospective Users of 4Mb DRAMs

Dataquest strongly advises users to carefully and *continuously* monitor the 4Mb DRAM supplier base during 1991 and 1992 for signs of early market exit by any suppliers that may conclude they cannot win the 4Mb DRAM market battle—and might migrate more quickly to 16Mb DRAMs or rethink their DRAM strategies.

In addition to supplier selection, a major challenge for users will be the choice and designation of product specification. As noted, the 4Mb DRAM product line will include wide-word DRAMs (e.g., ×8, ×9, ×16, ×18) and a profusion of SIMMs and VRAMs. The 4Mb DRAM packages will include less familiar versions such as zigzag-in-line package (ZIP), thin small-outline package (TSOP) in two types, and tape-automated bonding (TAB).

Supply Base for 16Mb DRAMs

The 16Mb DRAM product is now moving from the R&D stage toward the introductory stage of its cycle. Table 1 shows which suppliers offer 16Mb DRAM samples as of mid-August 1991 and which suppliers have 16Mb samples on the way. The product life cycle of this part should extend beyond the year 2005.

DATAQUEST PERSPECTIVE

DRAM cost management represents the stiffest challenge for many of Dataquest's SPS clients. This article lays out a strategy based on system/DRAM life cycle analysis, coupled with a evaluation of the supplier base at each density of DRAM, for cost-effective management of DRAM demand now and through the year 2000. A key element of the strategy invites users to assess system migration paths against Dataquest's DRAM life cycle forecasts.

DRAM users face a host of risks that can be reduced to two extremes. The first and most immediate risk is the all-too-familiar scenario of

DRAM spot shortages and erratic prices, which may affect *some* users of 256K DRAM as this product moves through the decline stage of its life cycle during the second half of 1991 and in 1992.

A second risk entails a long-term mismatch between a system's specific DRAM requirements in the face of a shifting global supplier base. Regarding megabit-density DRAM, the latter risk will not manifest its results for several years; however, this threat can be managed today through careful DRAM life cycle and supplier base evaluation.

DATAQUEST RECOMMENDATIONS

Life will remain challenging in our DRAM-hungry world. However, users should be able to minimize, if not avoid, the impact of periodic DRAM supply constraints.

A strategic recommendation is that purchasing managers, component engineers, and system designers use the DRAM supplier base/life cycle assessment to coordinate system and DRAM life cycles during this decade. SPS analysts can provide support toward this goal through the inquiry service.

As noted, users of 256K DRAMs should expect periodic spot shortages during the 1991 to 1993 time frame, perhaps as soon as by late 1991 or early 1992. Users can either forge supply relationships with suppliers such as Goldstar, Hyundai, Micron, and Samsung or migrate to higher-density DRAMs.

Many users are migrating now from 1Mb DRAMs. Dataquest recommends that users in general be prepared to make the migration during the 1992 to 1994 time frame in line with declining supply of this device. For users of 1Mb DRAMs that have no alternative but continue to use 1Mb DRAMs in the long term—through 1993 and beyond—Dataquest advises that the following suppliers be targeted for special long-term supply arrangements: Micron, Motorola, and Samsung. NMB should be targeted for higher-speed DRAMs. A less visible set of suppliers—Goldstar, Hyundai, Intel, Matsushita, Sanyo, and Sharp—also can be targeted.

Hitachi and Toshiba have taken the early but often critical lead in the 4Mb DRAM, with NEC again playing catch-up. Dataquest strongly recommends that users monitor the 4Mb DRAM supplier base via the *On-Line Dataquest Monday* service or by inquiry for clarification of any reports of either new market entrants or early market exits.

Sam Young
Ronald Bohn

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Research Newsletter

TRENDS IN CACHE USAGE, 1989-1994

There has been a profound increase over the past three years in the use of cache memory. Caches that once accounted for less than 50 percent of the dollar sales of static RAMs (SRAMs) now account for more than 80 percent and have significantly bolstered the growth of the SRAM market. Caches used to be found almost exclusively in large mainframes, but now they are common in desktop systems. Dataquest believes that few general-purpose processing systems of any sort will be sold without a cache in the near future.

The main reason for this increasing use of cache memory comes from device speed increases resulting from semiconductor process improvements. Although dynamic RAMs (DRAMs) have become faster during the past decade, microprocessors have increased in speed at a rate that outstrips DRAM improvements. Certain parameters, such as write cycle setup and hold times, refresh buffer propogation delays, and delays due to the capacitance of the DRAM's I/O pins, cannot be improved as significantly by semiconductor process improvements as can address access time or processor clock speed. This means that a DRAM cannot keep pace with the doubling of a CPU's clock rate simply by halving its access time; the access time must be cut by two-thirds or even three-fourths. This means that, as processor clock speeds continually evolve upward, the processors' thirst for data will become harder and more expensive to support using the equivalent DRAM technology.

CACHE MEMORY OPERATION

Because any processor system tends to spend most of its cycles repetitively accessing a limited set of data out of a relatively small area of memory, a cache memory can usually offer significant performance improvements to systems whose throughput is limited by the system DRAM. Hence many designers will now add a cache, a relatively small very fast SRAM, to enhance the speed of their high-performance systems. The effective performance improvement that can be obtained through the use of a typical direct-mapped cache in an i386 or AMD386-based PC is in Figure 1. In many cases, designers find that they can actually reduce system cost for a given processing throughput requirement simply by adding a small cache and more than offset the cost of the cache by using significantly slower (and less costly) DRAMs as the system main memory.

CACHES IN PCs

There has been a strong increase in the number of PC systems using cache memories over the past three years. Few, if any, 286-based PCs use cache. The introduction of the 386 at 25 MHz and faster frequencies initiated the broad use of cache in PC applications. The growth in the number of cached PC systems is in Figure 2. A typical cache size in early 25-MHz i386 systems was 32KB. More recent systems based on a 33-MHz or 40-MHz i386 or AMD386 generally offer 64KB caches. Options are often included on the processor board to increase the cache size to as large as 256KB.

Although the i486 processor has an internal cache on the processor's chip, it is interesting to note that most PC designers will still employ an external cache built from discrete fast SRAM. This is done not only to improve performance; the consumer has now become aware that cache is good to have and usually assumes that more is better, so PC manufacturers now use cache size to help give their products market differentiation. In this configuration the i486's internal cache is referred to as the primary cache, and the external cache is referred to

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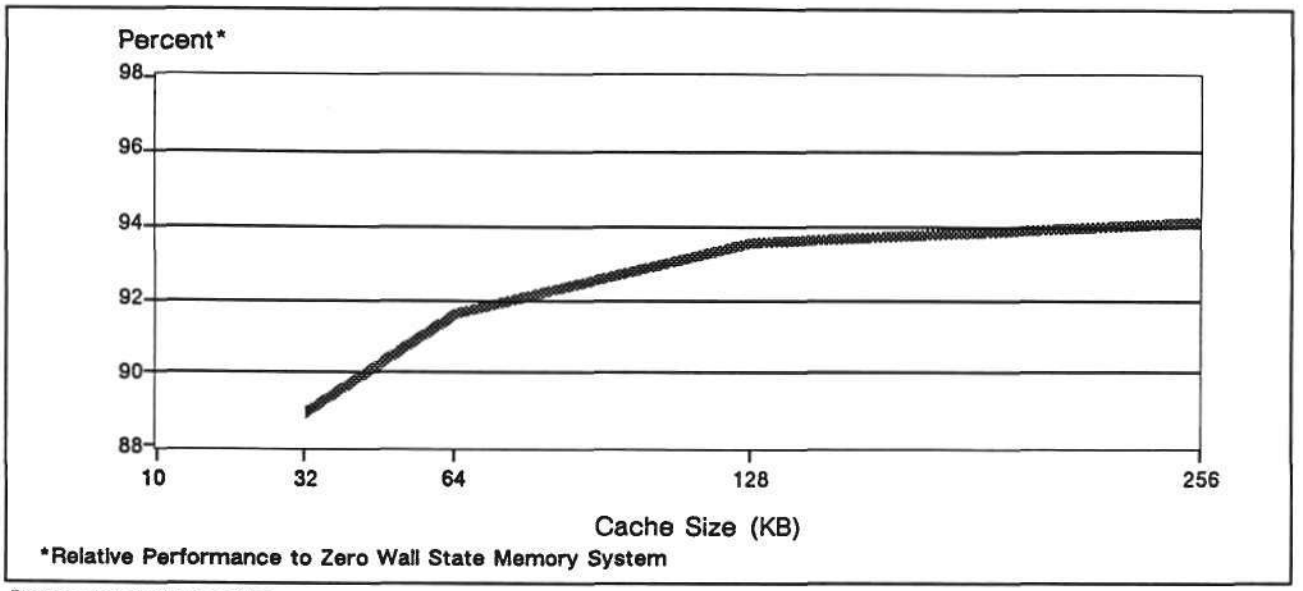
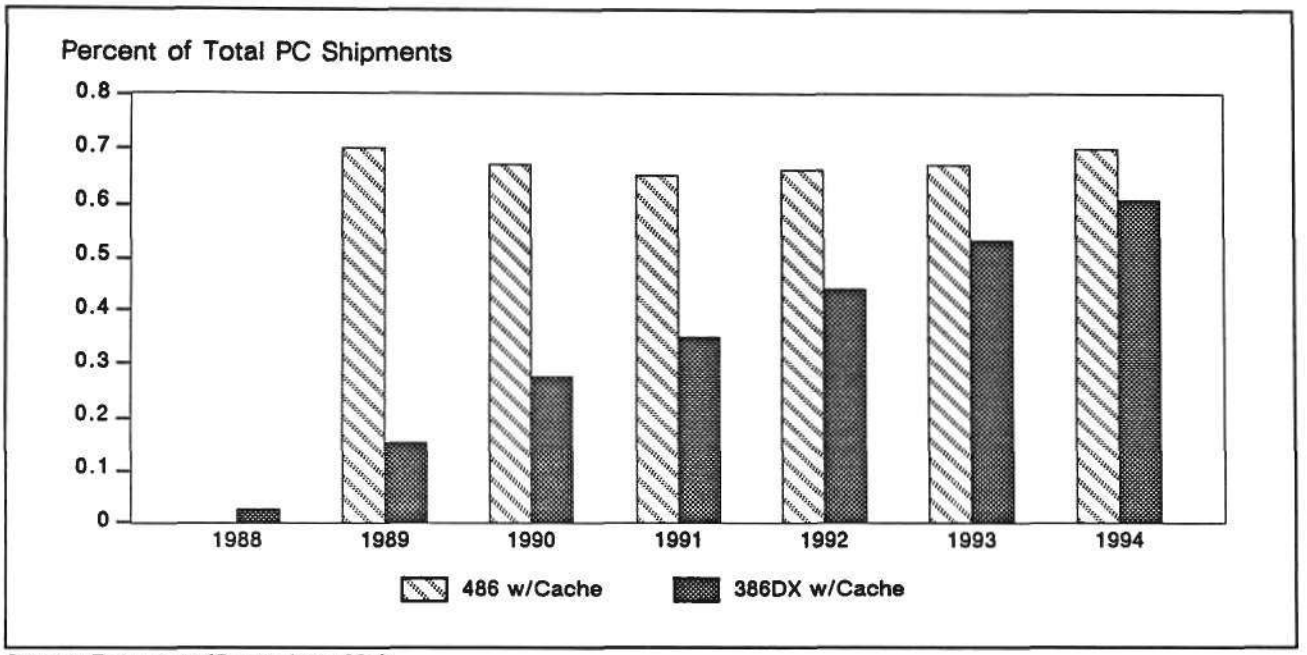
FIGURE 1
First-Level Cache Performance versus Cache Size, Basic Direct-Mapped Cache Architecture



Source: Intel Corporation

FIGURE 2
Personal Computer Cache Growth



Source: Dataquest (September 1991)

as a secondary cache. Secondary cache size is usually chosen to be much larger (128KB to 256KB) than the primary cache it supports.

WORKSTATION CACHES

Cache memory is found in many applications other than PCs, but the PC market is sufficiently large that it often overshadows other important cache memory markets. Most workstations are based upon RISC processors whose design criteria automatically assume the use of cache. Cache use estimates for workstations are in Table 1.

The MIPS R3000 is a good example of a RISC processor used in engineering workstations. The R3000 is designed to accommodate a wide variety of cache sizes, yet most designers choose to use 64KB of instruction cache and 64KB of data cache. The cache's tag bits and several parity bits are stored in external RAM along with the cached 32-bit instruction or data word, making the total cache word width for each cache 60 bits. This size cache is most often implemented using 16Kx4 SRAMs, amounting to a per-processor requirement of 30 SRAMs. Obviously, increases in R3000 processor sales will cause a dramatic increase in SRAM sales.

Just as CISC processors tax the performance of DRAMs, RISC processors require almost impossibly fast SRAMs. The R3000 requires extremely fast SRAMs. At 40-MHz operation, an 8ns t_{AA} and a 4.5ns t_{OE} are required. A slower 33-MHz R3000 still requires a 12ns SRAM access time with an output enable time of 8.5ns. The increasing performance requirements of these fast machines is placing a severe strain on the ability of manufacturers to supply adequately fast memories cost effectively.

In order to allow current and future SRAM processes to supply those cache RAMs that will support today's RISC and tomorrow's CISC CPUs at clock frequencies at or above 40-MHz, SRAM manufacturers are moving to produce parts optimized to support specific processors. This generation of specialized SRAMs, called application-specific memories, addresses speed issues while also focusing upon component count reduction. The application-specific SRAM can incorporate latches, registers (for self-timed write), burst counters, fast address pins, and multibanked architectures, among others.

Cache memory implementations are closely tied to the choice of cache controller design. Several component choice options for i386-, AMD386-, and i486-based systems are Tables 2 and 3, respectively.

Given the trends outlined for continual processor clock speed increases, insufficiency of DRAM speed improvements, and end-user demand, Dataquest forecasts significant growth in total bits for high-performance SRAMs. Table 4, Dataquest's general forecast of fast SRAM demand,

TABLE 1
Estimated Workstation Cache Use

	Low-End Workstations					
	1989	1990	1991	1992	1993	1994
System with Cache (%)	70	80	85	90	95	100
Cache Size (KB)	64K	72K	128K	256K	256K	384K
Cache Speed (ns)	25ns	20ns	15ns	15ns	12ns	10ns
	High-End Workstations					
	1989	1990	1991	1992	1993	1994
System with Cache (%)	98	100	100	100	100	100
Cache Size (KB)	128K	128K	256K	384K	768K	1MB
Cache Speed (ns)	20ns	15ns	12ns	10ns	10ns	8ns

Source: Dataquest (September 1991)

TABLE 2
386DX Cache SRAM Requirements

Controller Used	SRAM Device(s) Required	Quantity	Speed Required 25 MHz	33 MHz
OPTi	16Kx4	2	20ns	15ns
	8Kx8	8	35ns	25ns
Chips & Technologies	4Kx4 (with output enable)	2	25ns	15ns
	8Kx8	8	35ns	25ns
Discrete Implementation #1	8Kx9	1	25ns	15ns
	8Kx8	8	35ns	25ns
Discrete Implementation #2	16Kx4	2	25ns	15ns
	16Kx4	8	25ns	20ns

Source: Dataquest (September 1991)

TABLE 3
486 Cache Requirements

Implementation	SRAM Device(s) Required	Quantity	Speed Required 25 MHz	33 MHz	50 MHz
Discrete Design #1	8Kx9	16	25ns	20ns	-
	8Kx8	1	20ns	15ns	-
Discrete Design #2	32Kx9 (with burst and self-timed write)	4	34ns	24ns	14ns
	8Kx8 (with reset and internal comparator)	2	45ns	30ns	12ns

Source: Dataquest (September 1991)

does not specify speed, organization, or application, yet the explosive growth in SRAM usage due to the pervasion of cache memories is self-evident.

In conclusion, there will be a need for accelerating volumes of faster, more complex SRAMs in the very near future, products that will be designed to meet the needs of the very high clock frequency processors that now exist or will shortly exist.

Sam Young
Jim Handy

TABLE 4
Fast SRAM Forecast

	1990		1991		1992		1993		1994	
Year	Units	ASP ($)	Units	ASP ($)	Units	ASP ($)	Units	ASP ($)	Units	ASP ($)
Density										
4K	4.0	2.87	3.0	2.74	2.3	2.17	1.6	2.62	0.8	2.18
16K	33.5	2.46	24.1	3.01	19.3	2.66	16.4	2.12	12.0	1.98
64K	72.4	5.92	88.3	3.58	98.9	3.42	99.4	3.70	89.5	3.56
256K	24.8	16.49	51.4	10.06	74.8	8.57	96.1	8.08	104.8	7.62

Source: Dataquest (September 1991)

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Research Newsletter

IBM AND SIEMENS SIGN AGREEMENT TO MANUFACTURE 16Mb DRAMs

SUMMARY

On July 4, 1991, IBM and Siemens signed an agreement to manufacture 16Mb DRAMs at IBM's fab in Corbeil-Essonnes (France). This agreement will capitalize on the technology of both companies and enable them to implement the latest semiconductor manufacturing technology in Europe. This agreement is part of an ongoing effort to strengthen an independent European electronics industry, and it will also allow both companies to transfer this technology to other manufacturing sites.

In 1990, both companies introduced 16Mb DRAM samples. However, as a result of this agreement, 16Mb DRAMs with increased functionality will be developed at a Siemens facility in Munich. Dataquest estimates that Siemens will contribute between $400 million and $600 million for design and equipment, and IBM will contribute the manufacturing process technology and fab. This is IBM's biggest joint-manufacturing agreement and exemplifies the action that major semiconductor manufacturers are taking to reduce the risk and cost associated with a new submicron state-of-the-art fab.

MANUFACTURING PLANS

Manufacturing will begin by the end of this year with shipments scheduled to begin in the second half of 1992. An existing IBM facility is being upgraded to handle the strict contamination control required to manufacture these devices. The upgrade is based on Dr. Ohmi's ultraclean technology. A Dr. Ohmi-specified fab includes a Class 1 clean room; electrostatic discharge control; and high-purity chemical, gas, and DI water delivery systems. Dataquest estimates that a Dr. Ohmi-specified clean room costs about $2,900 per square foot. When fully operational, the facility will employ a total of 600 people, roughly 300 from each company.

The manufacturing process is based on existing IBM process technology developed at Corbeil-Essonnes. Dataquest estimates that between 375 and 525 process steps are required to manufacture a 16Mb DRAM. The manufacturing test vehicle used to bring up the line will be an IBM device. However, this device was designed for mainframe computer applications. Therefore, after the line is up and running, the newly designed Siemens 16Mb DRAM with increased functionality will be manufactured. When fully equipped, the fab will have the capacity to start 12,000 8-inch wafers per month. The fab will also have the capability to produce ASIC products that feature linewidths of 0.5 micron.

WHERE THE CHIPS ARE GOING

IBM plans to retain the chips for captive use, and Siemens plans to sell the chips on the merchant market. This strategy will enhance Siemens' product line and guarantee its customers DRAM availability. If excess capacity is available, participation by other companies will be allowed in this agreement.

Last year, IBM and Siemens also entered into a 64Mb DRAM agreement. This agreement is of strategic importance to both companies; the following section analyzes its strategic importance.

LAST YEAR'S 64Mb DRAM AGREEMENT

On January 23, 1990, IBM and Siemens signed an agreement to develop 64Mb DRAMs. This agreement focused on process-technology

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development and chip design. Both IBM and Siemens decided that the cost of developing the new process technology required to make leading-edge DRAMs is too risky and costly to do alone. As a result, IBM and Siemens entered into an agreement in which they would share equally in 64Mb DRAM technology development costs. They each dedicated 100 engineers to this project. No financial transaction took place between the two companies.

The goal of the agreement is to introduce a 64Mb DRAM into volume production in about 1995. Before this agreement, Siemens' goal was to complete 64Mb DRAM development by 1995. With IBM's help, this goal could be achieved one year early, which is of strategic importance because time to market is critical in today's environment. In the DRAM market, the best profit margins occur during the first year a chip is in volume production. This is the point at which demand is strong and supply is tight.

As a starting point for this agreement, each company disclosed its strengths and weaknesses as they relate to DRAM production. Although a common process and product are being developed, each company will manufacture and market the 64Mb DRAMs separately. IBM plans to manufacture the 64Mb DRAMs in Essex Junction, Vermont, and Siemens plans to manufacture in Munich and Regensburg, Germany. As with the 16Mb DRAM agreement, IBM will use the chips for captive purposes and Siemens will expand its device product line offering.

IBM and Siemens both use a trench capacitor for the 64Mb DRAM process rather than the stack capacitor process. The trench capacitor will most likely be used for higher-density designs. This deal is not a technology-transfer arrangement but a codevelopment arrangement that will give both companies equal ownership in the process and base product.

JOINT VENTURES—A WAY OF LIFE

Dataquest believes that the 1990s will bring a substantial amount of joint-venture activity. This increase in activity is being driven by escalating fab and equipment costs. Even the giant semiconductor manufacturers are managing their financial resources more carefully than in the past. This section briefly describes two other unrelated recently announced joint ventures that illustrate this point.

A significant joint venture was announced in April 1991. Texas Instruments, Hewlett-Packard, Canon, and the Singapore Economic Development Board announced that they will form a venture that will use submicron CMOS manufacturing technology to manufacture DRAMs. The fab being constructed for this venture will also have the capability to manufacture advanced logic if market demand shifts.

Also in April, a joint-development agreement was reached between AT&T Microelectronics and NEC that will have a positive impact on U.S.-Japan trade relations. The purpose of this agreement is to reduce the risks and costs associated with developing a 0.35-micron process. Twenty-six research teams were assembled to carry out this agreement. AT&T plans to incorporate the results of this agreement into its new fab in Orlando, Florida, which will incorporate microenvironments. The most important aspect of this agreement is that AT&T and NEC will have the same process and tool set, which means that they can second-source each other's products. This is truly second-sourcing for ASIC customers.

In 1990, Dataquest ranked NEC number 1 with semiconductor revenue of $5 billion, and AT&T was ranked number 20 with semiconductor revenue of $830 million. It is evident that if these financially sound companies are entering into agreements to reduce cost and risk, the others will have to follow.

DATAQUEST PERSPECTIVE

The Siemens/IBM 16Mb DRAM agreement increases the chances of Siemens remaining a contender in the fiercely competitive DRAM market. This is of strategic importance because Europe does not want to become dependent on foreign sources for its DRAMs. However, before this agreement, it was questionable if Siemens would have survived in the DRAM market by itself.

As semiconductor manufacturing complexity increases, agreements of this nature are mandatory to survival. Forces that make these agreements mandatory include the mammoth R&D investment required to design a chip such as the 16Mb DRAM, the huge initial capital investment required for manufacturing equipment and facilities, and the cost of capital.

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