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LSI Logic Ends Year Reporting Modest Growth

LSI Logic Corporation closed the books on 1997 reporting revenue of $1.29 billion, a 4 percent increase over the $1,239 billion reported for 1996. Revenue for the fourth quarter of 1997 was $323 million, a 7 percent increase over the $301.8 million in the fourth quarter of 1996 and a 1 percent decrease from the prior quarter.

LSI Logic has a book-to-bill ratio of about 1.0 and is running at a 70 percent fab utilization rate. The communications sector, specifically networking, is strong for LSI, while the data processing sector is still recovering. LSI has many design-wins in the consumer sector and expects significant revenue increases in 1998 as a result. LSI's guidance for the first quarter of 1998 was for results to be flat to up slightly, and the company is expecting annual growth of around 15 percent.

Dataquest Perspective

LSI has been struggling to make significant revenue gains over the past two years. Although the company's strategy is fundamentally sound—targeting the top suppliers in each application market and codeveloping system-level products—the competition is getting stronger. Specifically, IBM and Lucent Technologies have implemented similar strategies and have made major investments in people and R&D to increase their presence. LSI Logic spent over $226 million on R&D during 1997. It is difficult to compare R&D investments from vertically integrated companies because the money is spent over a wide range of products; however, it is clear that IBM has been investing heavily in ASIC product development, as can be seen by the copper interconnect breakthrough. These investments by IBM and Lucent are paying off with increases in ASIC market share. In 1996, both IBM and Lucent had ASIC revenue gains of more than 35 percent, compared to a flat year by LSI Logic. Dataquest is currently working on the final 1997 ASIC market share and expects both IBM and Lucent to have ASIC revenue growth rates of better than 30 percent, compared to LSI Logic's 4 percent. Vertically integrated companies with deep pockets have gained significant momentum against the focused ASIC suppliers over the last three years. All three companies are investing in advanced design methodologies, targeted cell libraries, and advanced manufacturing; the key difference is the deeper pockets of vertically integrated companies and their ability to amortize costs over more products, giving them a pricing edge. Vertical market system knowledge is also key to penetrating the system-level integration (SLI) markets, and, clearly, IBM knows the data processing market and Lucent knows the communications markets. Although LSI Logic is a strong competitor in both data processing and communications, it has unique systems knowledge in the consumer market and is the top consumer supplier. The road is getting more

challenging for the focused ASIC suppliers as the vertically integrated suppliers continue to gain strength.

By Bryan Lewis

March 24, 1998
ASIC/SLI Worldwide
Dataquest Alert
Jordan Selburn

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LSI Logic Introduces O.18-Micron ASICs

LSI Logic Corporation announced its latest generation of ASIC products. This product, designated the G12, has a drawn gate length of 0.18 micron and features two transistor options.

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LSI Logic Corporation announced its latest generation of ASIC products. This product, designated the G12, has a drawn gate length of 0.18 micron and features two transistor options. One transistor is optimized for low power dissipation at an operating voltage of 1V and the other for high performance at 1.8V; both transistors can be used on the same die. The maximum gate count is specified at 26,000,000 used logic gates.

The G12 is scheduled for prototype availability in the fourth quarter of 1998, with volume production beginning about six months later.

Like other dedicated ASIC vendors, LSI needs to find ways to continue differentiating its products. The growing threat posed by foundry manufacturing will make it difficult to survive with commodity products alone. The G12 appears to provide LSI with differentiation in a number of important areas.

First, the G12 is clearly targeted at the mobile and wireless markets. The 1V transistor was designed to reduce static as well as dynamic power dissipation. Coupled with a targeted set of system-level macros and a dual gate oxide process to enhance mixed-signal functionality, the G12 should win a lot of friends in the cellular market. The specified performance, along with plans for discrete elements including inductors, may ultimately allow LSI to incorporate some of the radio frequency (RF) front end onto the baseband IC, although there is likely to be some strong competition from emerging technologies such as silicon-germanium.

Second, LSI is introducing a low-K dielectric with the G12. Development of the low-K dielectric was chosen over copper interconnect, which LSI claims has too large a yield impact to be cost-effective at this time. Although details on the process are sketchy, the claimed results (a dielectric constant under 3) are significant and will have about the same impact on wire loading as copper does–a loading reduction of about 30 percent. This translates directly into improved performance at the chip level and will help provide LSI an edge in high-performance applications. Copper wiring, pioneered by IBM in its SA-27, does provide advantages over a low-K approach for power distribution and should still have an edge for overall performance impact. Dataquest speculates that LSI is not using fluorinated silicon oxide, but whatever the material choice, this represents a major step forward.

Third, the G12 has set the current standard (although this is usually fleeting) for logic density at 65,000 used gates per square millimeter. This eclipses IBM by a few percent and VLSI Technology Inc. by a little more, but it keeps LSI well ahead of the foundry manufacturers for at least a little while. Given the lower cost per wafer for the foundries, it is critical for LSI to strive for parity where it counts–the die cost. This level of logic density, aided by the tightest metal routing grid of which Dataquest is aware (0.63 micron on the lower routing levels), should allow LSI to maintain a competitive cost position, assuming that the company can keep the fabs running close to optimum capacity.

What's missing in the G12? Not much was said about embedded memory capabilities in the G12. Some of the areas for which the G12 is targeted, such as wireless, are pushing for embedded flash memory to achieve system-level integration. Embedded DRAM is a growing need, and, while LSI is working toward a solution in partnership with Micron Technology Inc., we suspect that a final product is still a way off. Availability of the complete product is also an issue. As with every other vendor's ASIC announcement, there is a gap between the initial product release and what is required for a true system-level product; Dataquest estimates that it will be the second quarter of 1999 before the G12 is really ready for system-on-a-chip designs. Although this is by no means unique to or a flaw in the G12, system designers should consider this when reading any ASIC product announcement.

LSI needs advanced products to succeed in today's market. A commodity ASIC would not survive against the ever-broadening set of competitors, both focused, dedicated ASIC manufacturers and the foundries. With the ASIC product becoming more horizontal than vertical (aided by the foundries, design houses such as Cadence, and a burgeoning system-level macro market), it will become increasingly difficult to differentiate ASICs in the future. For now, however, the G12 will certainly help LSI hold off the "barbarians at the logic gate."

By Jordan Selburn

Product Code: ASIC-WW-DA-9803

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Dataquest ALERT

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Dataquest Releases 1997 ASIC Market Share Rankings

IBM and Lucent Technologies were the big winners, according the Dataquest's 1997 ASIC market share rankings. IBM grew an outstanding 53.6 percent in total ASIC sales, while Lucent posted excellent numbers, growing 40.2 percent, as shown in Table 1. For both these companies, as well as for other ASIC suppliers, the majority of the percentage gains were from cell-based ICs at the expense of gate arrays. Table 2 shows that the worldwide cell-based IC market grew 25.2 percent in 1997, compared to a 6.3 percent decline in gate arrays. IBM grew over 80 percent in cell-based ICs and declined 40 percent in gate arrays, as shown in Tables 3 and 4. NEC Corporation, LSI Logic Corporation, and Texas Instruments Inc. were among the many that experienced a similar trend.

Cell-based ICs are winning over gate arrays because they offer increased functionality per square millimeter, better performance, and a lower device cost from the reduced die size. Gate arrays beat cell-based ICs in terms of time to market; however, programmable logic devices (PLDs) are the clear winner over both gate arrays and cell-based ICs in this area. PLD suppliers had a tough year in 1997 and grew only 12.3 percent because of fierce price wars and continued inventory adjustments by OEMs and distributors. Altera Corporation still managed to grow 27 percent in 1997, but other companies such as Xilinx Incorporated, Vantis Corporation, and Actel Corporation were not as fortunate, as shown in Table 5.

Table 1
Top 10 Worldwide ASIC Ranking (Millions of Dollars)

1996 Rank	1997 Rank		1996 Revenue	1997 Revenue	Change (%)
1	1	NEC	1,689	1,863	10.3
5	2	IBM	1,003	1,541	53.6
4	3	Lucent Technologies	1,060	1,486	40.2
3	4	Fujitsu	1,120	1,248	11.4
2	5	LSI Logic	1,136	1,182	4.0
6	6	Texas Instruments	841	886	5.4
8	7	VLSI Technology	615	667	8.5
7	8	Toshiba	836	660	-21.1
11	9	Altera	497	631	27.0
10	10	Xilinx	566	612	8.1

Source: Dataquest (April 1998)

Table 2
Worldwide ASIC Consumption by Product (Millions of Dollars)

Product	1996	1997	Growth (%)
PLD	1,872	2,103	12.3
Gate Array	5,612	5,260	-6.3
Cell-Based IC	7,317	9,164	25.2
Total	**14,801**	**16,527**	**11.7**

Source: Dataquest (April 1998)

Table 3
Top 10 Worldwide Cell-Based IC Ranking (Millions of Dollars)

1996 Rank	1997 Rank		1996 Revenue	1997 Revenue	Change (%)
1	1	Lucent Technologies	965	1,396	44.7
3	2	IBM	733	1,380	88.3
2	3	NEC	741	888	19.8
4	4	LSI Logic	556	765	37.6
5	5	VLSI Technology	549	595	8.4
6	6	Texas Instruments	406	480	18.2
7	7	Hewlett-Packard	380	466	22.6
8	8	Fujitsu	346	439	26.9
10	9	SGS-Thomson	305	305	0
9	10	Symbios	345	288	-16.5

Source: Dataquest (April 1998)

Table 4
Top 10 Worldwide Gate Array Ranking (Millions of Dollars)

1996 Rank	1997 Rank		1996 Revenue	1997 Revenue	Change (%)
1	1	NEC	948	975	2.8
2	2	Fujitsu	774	809	4.5
3	3	LSI Logic	580	417	-28.1
4	4	Toshiba	568	408	-28.2
5	5	Texas Instruments	430	403	-6.3
6	6	Hitachi	388	353	-9.0
8	7	Mitsubishi	223	254	13.9
7	8	IBM	270	161	-40.4
9	9	Motorola	209	147	-29.7
11	10	Matsushita	98	124	26.5

Source: Dataquest (April 1998)

Table 5
Top 10 Worldwide PLD Ranking (Millions of Dollars)

1996 Rank	1997 Rank		1996 Revenue	1997 Revenue	Change (%)
2	1	Altera	497	631	27.0
1	2	Xilinx	566	612	8.1
3	3	Vantis	243	243	0.0
4	4	Lattice	200	242	21.0
5	5	Actel	149	156	4.7
6	6	Lucent Technologies	75	90	20.0
7	7	Cypress Semiconductor	60	52	-13.3
8	8	Atmel	34	33	-2.9
9	9	QuickLogic	25	29	16.0
11	10	Philips	3	4	33.3

Source: Dataquest (April 1998)

The purpose of this Dataquest Alert is to get the numbers to our clients as soon as possible; it will soon be followed by a detailed Dataquest Perspective analyzing supplier trends and a Market Statistics report that will quantify all ASIC suppliers' revenue by product.

By Bryan Lewis

This Dataquest Alert is being delivered to the following service:

- ASIC/SLI Worldwide (ASIC-WW)

April 7, 1998
ASIC/SLI Worldwide
Dataquest Alert
Jordan Selburn

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Lucent, Chip Express Partner to Reduce Time to Market

Lucent Technologies Microelectronics Group today announced a partnership with Chip Express for rapid ASIC customization and modification.

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Lucent Technologies Microelectronics Group today announced a partnership with Chip Express for rapid ASIC customization and modification. Lucent and Chip Express will develop and offer 0.25-micron cell-based ASICs with embedded laser programmable gate array (LPGA) blocks. In addition to an equity investment, Chip Express also gets access to Lucent's 0.25-micron process technology.

Initial product and library availability is scheduled for the fourth quarter of 1998.

Dataquest Perspective

The main thrust of the Lucent-Chip Express partnership is to provide customers with a faster time-to-market solution than traditional ASICs provide, with a particular focus on rapid turnaround for system-level ASICs. Although they do not provide the instant gratification of programmable logic, the Laser Programmable System Chips (LPSCs) will allow rapid modification of a design without requiring a new and costly complete mask set.

Essentially, the LPSCs are akin to a late-1990s version of the embedded array in that most designs will have embedded system-level blocks and logic that can be programmed (or in this case, reprogrammed) in the metal layers. These parts will be designed to order, however, and not banked by Lucent and Chip Express. This technology does open the possibility of incorporating LPGA blocks into Lucent-designed ASSPs in what would be true system-level embedded arrays; this could be particularly attractive in the communications market in which Lucent specializes. The LPSC product is certainly attractive and should definitely shave some time off the design cycle, although in our opinion the majority of designs will see less than the advertised three- to four-month reduction.

For production, customers have several choices. First, they can continue with LPSCs, which may make sense for small production runs in which the nonrecurring engineering (NRE) costs associated with new masks may be prohibitive. Second, and in our opinion the approach most customers will take, they can redo the top two layers of metal to incorporate any modifications made during the LPSC phase. High-volume designs could always be respun in a pure cell-based ASIC if necessary to minimize cost,

although it is our experience that this is often planned but rarely executed. Lucent estimates that the typical design will incur about a 10 percent area penalty by including the LPGA block, and the cost and time associated with the move to a cell-based ASIC makes sense only for the very highest-volume parts or in situations in which the design can be migrated to a more advanced process technology.

There are competing approaches for reducing system-level ASIC turnaround time. Some ASIC vendors already offer (although not on a production basis) the ability to incorporate unused gates or modules within a cell-based design. These blocks can than be used to patch a design, again using only metal mask changes. More interestingly from both a technological and business standpoint is Lucent's own plan to embed FPGA blocks within a cell-based design (field-programmable system chips, or FPSCs, if yet another acronym is needed). This is the ultimate for flexibility and turnaround time improvement, and the cost in die size (FPGA logic is much less dense than either ASIC or LPGA) may be outweighed by faster time to market if days really do matter. With either approach, customers could use paths similar to those outlined above for cost reduction of production parts.

There is one other area for speculation: Was this a preemptive strike by Lucent? Other ASIC vendors could use embedded LPGAs as an effective counter to Lucent's upcoming FPSCs, and this partnership may cut the competition off from access to Chip Express' technology. In any case, time to market is a key differentiating feature for system-level designs, and Lucent and Chip Express have an attractive offering. But Lucent may have something still more attractive yet to come.

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January 29, 1998
ASIC/SLI Worldwide
Dataquest Alert
Bryan Lewis

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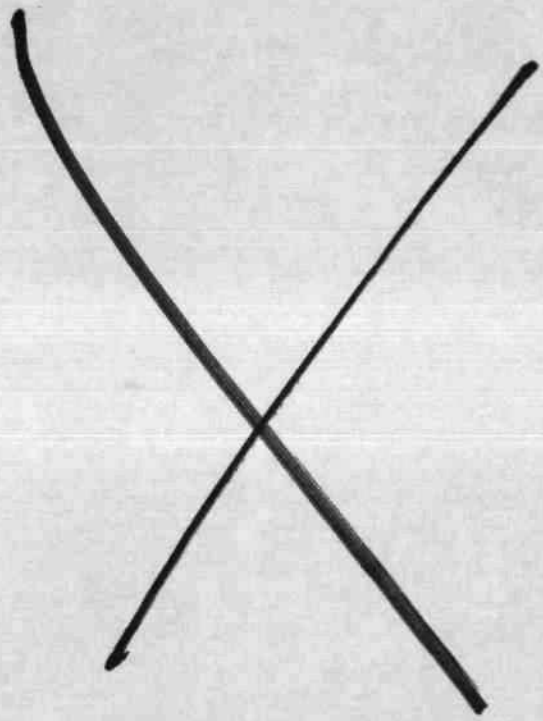

Perspective

ASIC/SLI Worldwide

Market Analysis

SLI Market to Reach $24 Billion by 2002

Abstract: *System-level integration (SLI), or system-on-a-chip, is rapidly becoming the most significant trend in the semiconductor industry since the introduction of the microprocessor in the early 1970s. System-level ICs are penetrating many of the leading high-volume applications, ranging from cell phones to computers to consumer products. Most of the leading semiconductor suppliers realize that SLI is the wave of the future and are formulating strategies to address this high-growth market. In this Perspective, Dataquest introduces a new methodology for tracking the SLI market, examines key market/supplier dynamics, and provides a series of SLI forecasts.*

By Bryan Lewis

Dataquest Expands SLI Coverage

Dataquest is expanding the coverage of the system-level integration (SLI) market to include application-specific standard products (ASSPs) as well as application-specific integrated circuits (ASICs). SLI ASSPs will account for more than half of the total $24 billion SLI market in the year 2002.

SLI devices are defined as ICs dedicated to a specific application that include a compute engine (microprocessor core, digital signal processor [DSP] core, or Motion Picture Experts Group [MPEG] core), logic, and memory on a single chip. ASICs are sold to one user; ASSPs are sold to multiple users.

To get a better understanding of the size of the SLI ASIC market versus the SLI ASSP market, Dataquest did an extensive study of the two markets using a bottom-up, application-driven demand methodology. Past Dataquest SLI ASIC forecasts were primarily supply driven. Our new methodology starts with system unit shipments for a selected market, then examines the dollar value of the ASIC and ASSP content in each system to come up with a demand forecast by application market. We then examine the current and

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projected percentage of each application market that includes on-chip compute engines (microprocessor cores, DSP cores, and MPEG cores) to determine the size of each SLI market.

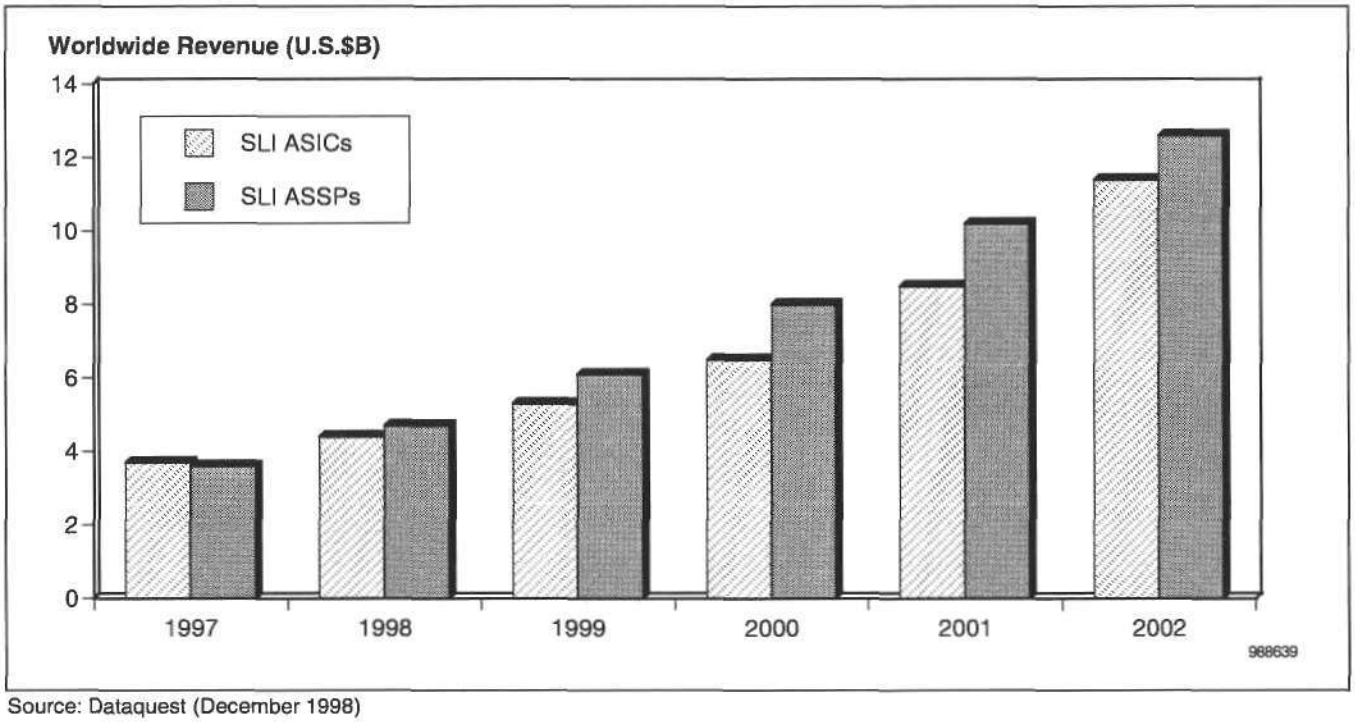
The aggregate results of our demand-driven study showed that the SLI ASSP market would overtake the SLI ASIC market in 1998 and would continue to remain the largest market through the forecast period. The results also indicated that past SLI ASIC forecasts included some SLI ASSPs. For further details on the SLI ASIC versus SLI ASSP splits by application market, please see Dataquest's report titled "Worldwide ASIC/SLI Forecast: Fall 1998" (ASIC-WW-MS-9803), dated November 23, 1998.

Key findings from the SLI market study are presented in this newsletter.

SLI ASSPs Gain Momentum

The SLI market emerged from the ASIC industry about five to seven years ago, led by focused companies that knew how to take ASIC design methodology to the next level—the system level. Microprocessor cores such as MIPS and ARM became the cores of choice as the SLI market blossomed. Soon after, ASSP vendors adopted ASIC methodology and cores as a way to get to market quicker. The SLI ASSP market has been gaining momentum over the past two years and is expected to eclipse SLI ASICs during 1998 (see Figure 1).

Figure 1
Estimated Worldwide SLI ASIC/ASSP Consumption



Source: Dataquest (December 1998)

Most high-growth application markets start with an ASIC solution when the standards are uncertain and system designers are experimenting with new architectures. As standards become set and the application matures, SLI ASSPs emerge as the viable low-cost alternative. ASSP solutions offer better time to market and no design fees. The first ASSP usage usually comes from second- or third-tier system suppliers that are late to market and have less design experience. As an application market matures, first-tier system suppliers start to examine how much product differentiation is gained through their custom ASIC solutions. First-tier system suppliers will shift to ASSP solutions if ASIC cost outweighs the product differentiation.

ASIC design fees are taking a step function jump as we move to each new generation manufacturing process because of the rise in mask charges. The cost for a 0.35-micron mask is around $7,000, compared with around $12,000 for a 0.25-micron mask. The cost for 0.18-micron masks is also expected to take a significant jump. This additional mask cost, coupled with the fact that more masks are used in a 0.18-micron process (typically around 25 to 30 masks per design set), leads to skyrocketing design fees. It is common to hear of high-end SLI ASIC design fees in excess of a half a million dollars.

The preferred solution for a given application market hinges on its position in the product life cycle. Table 1 illustrates the emerging SLI applications and the dominant product type for the year 2000.

Table 1
Emerging SLI ASIC/ASSP Markets

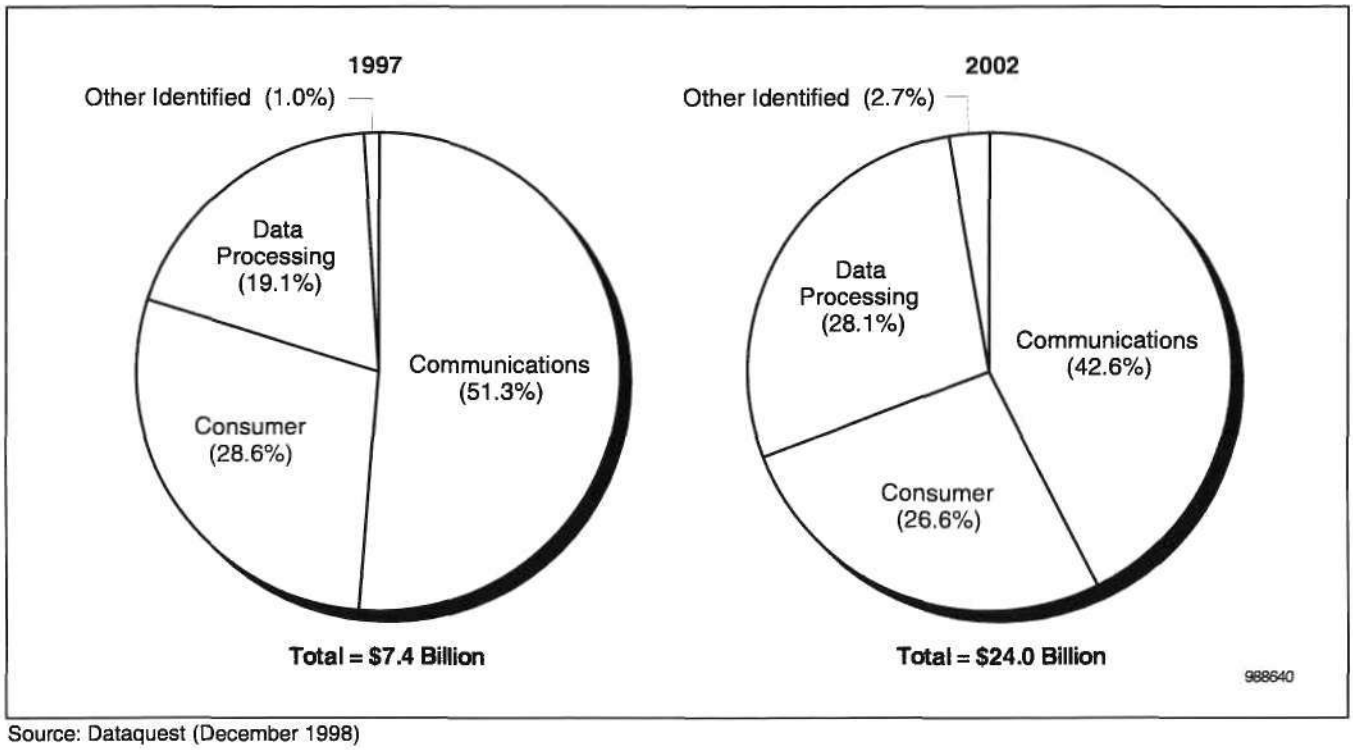
	2000 Dominant	
	ASIC	**ASSP**
Communications		
Digital Cellular	X	X
LAN/WAN	X	
Modems/Remote Access		X
Wireless Infrastructure		X
Consumer		
Digital Set-Top Boxes	X (cable)	X (satellite)
DVD Players		X
Video Games	X	
Digital Still Cameras		X
Data Processing		
Personal Computers		X
Workstations	X	
Disk Drives	X	
Printers	X	
Audio and Graphics		X

Source: Dataquest (December 1998)

Application Forecast

There are three major markets for SLI products: communications, data processing, and consumer applications. The communications segment accounts for more than half the 1997 market, followed up by consumer and data processing (see Figure 2). Table 2 provides device forecasts for the leading SLI ASIC/ASSP application markets. It is interesting to note that the application markets listed in this table account for about 90 percent of the total known SLI market, a percentage that remains relatively constant over the forecast period.

Figure 2
Estimated Worldwide SLI ASIC/ASSP Consumption by Application Group



Source: Dataquest (December 1998)

The largest single market for system-level ICs is for use in digital cellular handsets. Digital cellular handsets have achieved a reduced form factor, lower power consumption, and lower system costs through the use of SLI devices. This market is starting to mature, and we are starting to see the introduction of ASSP solutions. There are many companies attacking this market with both SLI ASICs and SLI ASSPs. ARM and DSP cores are very common in this market and are offered by many suppliers. Our digital cellular forecast assumes 98 million handsets (system units) in 1997 growing to 312 million handsets in 2002, or a five-year compound annual growth rate (CAGR) of 26 percent. Semiconductor dollar value per system is expected to decline rapidly because of the vast number of suppliers targeting this market. We assume $73 in 1997 dropping to $37 in the year 2002. In "ballpark" terms, we have units tripling over the next five years while average selling prices (ASPs) are cut in half. There is also more functionality going on chip during this same time period as we move to third-generation handsets that provide

some graphics and video capabilities. This increased functionality helps drive this market to SLI solutions. About one-third of the total semiconductor handset content was system-level ICs in 1997 and this is expected to rise to about 50 percent in the year 2002. The net result of our digital cellular assumptions is that SLI unit demand is very strong but ASPs will decline rapidly because there are 20-plus suppliers targeting this market.

Table 2
Estimated Worldwide SLI ASIC/ASSP Consumption by Application Market (Millions of U.S. Dollars)

	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Digital Cellular Handsets	2,361	2,674	3,193	3,883	4,618	5,757	19.5
Wireless Infrastructure	351	467	602	784	1,009	1,262	29.2
LAN/WAN	20	52	155	323	597	953	116.4
Modem/Remote Access	882	985	1,050	1,173	1,426	1,661	13.5
Personal Computer/ Workstation	696	923	1,240	1,655	2,226	2,906	33.1
Disk Drives	677	1,000	1,428	2,026	2,668	3,727	40.7
Digital Set-Top Box	749	1,088	1,631	2,197	2,640	2,832	30.5
DVD Video Player	50	89	182	263	469	629	65.9
Next-Generation Video Game Console	873	927	824	773	961	1,387	9.7
DTV Receiver	0	1	9	51	325	560	790.5
Total	**6,658**	**8,207**	**10,312**	**13,127**	**16,938**	**21,675**	**26.6**

Source: Dataquest (December 1998)

Wireless infrastructure, primarily base stations, constitutes a much smaller market than handsets but still shows promise for those with DSP technology. The LAN/WAN market is small today for SLI devices but is targeted for explosive growth as new technologies such as embedded DRAM come down in cost. The modem market is relatively flat, but there is growth in remote access.

The growth in personal computers/workstations comes primarily from graphics, audio, and disk drives. Disk drive suppliers are striving to reduce prices by incorporating more and more on a single chip thus driving SLI growth. On-chip functions that are starting to be incorporated on the single chip disk drives include read/write channel, servo control, motor control, and drive control, along with compute engines like ARM, SH, and DSPs. The PC-on-a chip market is negligible today, but we have programmed in some growth in the later part of the forecast period.

In the consumer area, set-top boxes are one of the primary SLI drivers. We have pushed out the adoption of DVD and DTV, but these still remain high-growth areas. We assume there will be 2.2 million TV-version DVD players in 1998, growing to 27 million by the year 2002. The semiconductor content per TV-version DVD player is expected also to decline rapidly, from $62 per system in 1998 to $26 per system in 2002. Most of these DVD TV players

incorporate system-level ICs with MPEG cores. We see a quick transition from SLI ASICs to SLI ASSPs in the DVD market as DVDs become more of a commodity product during the next two years. We believe that the video game market will remain a solid market for SLI ASICs over the forecast period and will not switch to SLI ASSPs because there are a small number of system suppliers that differentiate their system performance through hardware. This is not a standards-driven market; thus it remains an ASIC market. The video game market is a clear revenue driver for MIPS processor cores. We have programmed in a revenue dip in video games around the year 2000 as we transition to the next-generation systems from Sony, Nintendo, and Sega.

SLI Suppliers

SLI suppliers must invest in a number of areas to be successful. The challenges for SLI ASSP suppliers are similar to those facing SLI ASIC suppliers, but are somewhat less. Successful SLI ASIC suppliers need to invest in the following areas:

- Comprehensive design methodology
- Targeted cell-libraries/cores
- State-of-the-art manufacturing processes
- High-pin-count packages
- System knowledge
- Services

Having a comprehensive design methodology is a key element for both ASIC and ASSP suppliers. With reduced product life cycles, it is important that both types of suppliers have solid high-end design methodology and toolsets with a focus on verification and test, so that they can avoid multiple design iterations.

Application-specific cell-libraries and cores are one of the major ways for SLI ASIC suppliers to demonstrate their focus on a specific market. SLI ASIC suppliers must offer a variety of hard cores tuned for performance or size as well as a comprehensive set of soft cores that are easily migrated to the next-generation process. ASSP suppliers must also have a comprehensive library for their specific applications, but they do not have to offer library and design support to system designers, providing these suppliers with a savings.

One of the real differences between SLI ASIC suppliers and SLI ASSP suppliers is in manufacturing strategies. Most SLI ASIC suppliers have fabs and continue to make significant investments in updating the fabs and processes to stay competitive. Many SLI ASSP suppliers are fabless and use foundries, providing them with a huge R&D savings. We believe that most of the focused ASIC suppliers, especially the small-to-medium-size suppliers, will go fabless and become more design companies over the 10-year horizon because of the high costs of the next-generation fabs. On the packaging front, SLI ASIC suppliers are hit with a serious challenge of offering a wide range

of high-pin count packaging and support that they can either develop internally or buy from the merchant market. ASSP suppliers have an advantage here because they do not need to offer support to such a wide range of packaging options.

System knowledge is perhaps the most important element for both SLI ASIC and ASSP suppliers. For SLI ASIC suppliers, system knowledge will be used to determine exactly what unique cores must be developed for a specific application. System designers select their preferred SLI ASIC suppliers by their system knowledge, library elements that address the designers' specific application, and the suppliers' track record in delivering high-end silicon for the specific application. For SLI ASSP suppliers, system knowledge is essential for determining in advance the exact IC product requirements for each next-generation system.

Services can come in many forms, including providing design centers, on-site customer support, and foundry capabilities or, more recently, offering design services to do the entire design for the customer. We believe that there will be a significant rise in the number of suppliers offering design services over the next two years. Another interesting trend on the service front is for SLI suppliers to provide reference platforms with some software support so the customer can get through the design process more quickly.

An important point to keep in mind is that many SLI ASIC suppliers will also become SLI ASSP suppliers. SLI ASIC suppliers are in a great position to know future SLI ASSP product requirements from their ASIC experience.

Table 3 shows a sampling of the leading SLI ASIC and SLI ASSP suppliers.

Table 3
Leading SLI ASIC/ASSP Suppliers

SLI ASIC	SLI ASSP
LSI Logic	Siemens
IBM	Motorola
Lucent Technologies	QUALCOMM
VLSI Technology	Lucent Technologies
NEC	Texas Instruments
Texas Instruments	Rockwell
Motorola	C-Cube
Hitachi	STMicroelectronics
Toshiba	Creative Technologies
Fujitsu	S3, Trident, Cirrus

Source: Dataquest (December 1998)

Dataquest Perspective

SLI is clearly the wave of the future. Judging from the number of suppliers attacking this market, that is not a well-kept secret. The question is how many suppliers each application market will support. SLI is creating a fundamental shift in the number of IC suppliers required per system. We are moving from a large number of smaller ICs on a printed circuit board provided by many suppliers to one system-level IC provided by one supplier. SLI thus creates a great opportunity for the chosen supplier and a reduced market need for a large number of suppliers.

As part of our SLI study, we polled many of the leading SLI suppliers and asked them to rank in order of importance their specific target markets. The results were quite revealing: The vast majority of suppliers we polled were targeting the same high-growth markets covered in this newsletter. Although these markets provide great opportunity and are slated for high unit growth, the concern is that there will be increased margin pressure. It is important that suppliers look for unique ways to differentiate their products to get increased margins. Suppliers can differentiate through system knowledge, unique cores, process enhancements (copper, SOI, silicon germanium, BiCMOS), system architecture improvements, or the provision of unique services.

Another major point to keep in mind is that SLI will enable system companies to invent entirely new markets with new opportunities. SLI suppliers must think out of the box and work with system companies to find new markets to exploit. The opportunities are endless for those with creative minds.

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Perspective

ASIC/SLI Worldwide

Technology Analysis

Next-Generation High-Density Packaging Technology

Abstract: *Low-cost chip scale package (CSP) technology is now entering its growth stage as a package for system-level integration ASICs, memory, and standard logic devices. Demand from compact and lightweight systems, such as mobile communications and digital consumer equipment, is a major driver for the growth of CSP and other emerging package technologies, such as ball grid array and flip chip. This Perspective analyzes these new technologies, which hold the key to the miniaturization and successful implementation of next-generation submicron devices.*
By Yoshihisa Toyosaki and Mary Ann Olsson

Emerging Package Technology Drivers

The economic turmoil in Asia, coupled with the financial troubles in Japan, resulted in tremendous price pressure on electronic goods being shipped to Europe and the Americas during the past 12 months. The industry downturn that began in December 1995 continues to depress the pricing of most devices. A handful of semiconductor companies are reporting early signs of improvement in sales of new low-voltage, high-performance products. However, most semiconductor suppliers, including fabless suppliers, are still in the throes of a serious demand and pricing slump. System-pricing pressure has forced many competitors to increase the pressure on manufacturing margins for several key electronics products. Declining system average selling prices (ASPs) in many applications are putting pressure on semiconductor makers. Although volume demand is good in many communications, consumer, and data processing segments, declining ASPs are damaging system revenue growth and putting pressure on the dollar value of semiconductor content.

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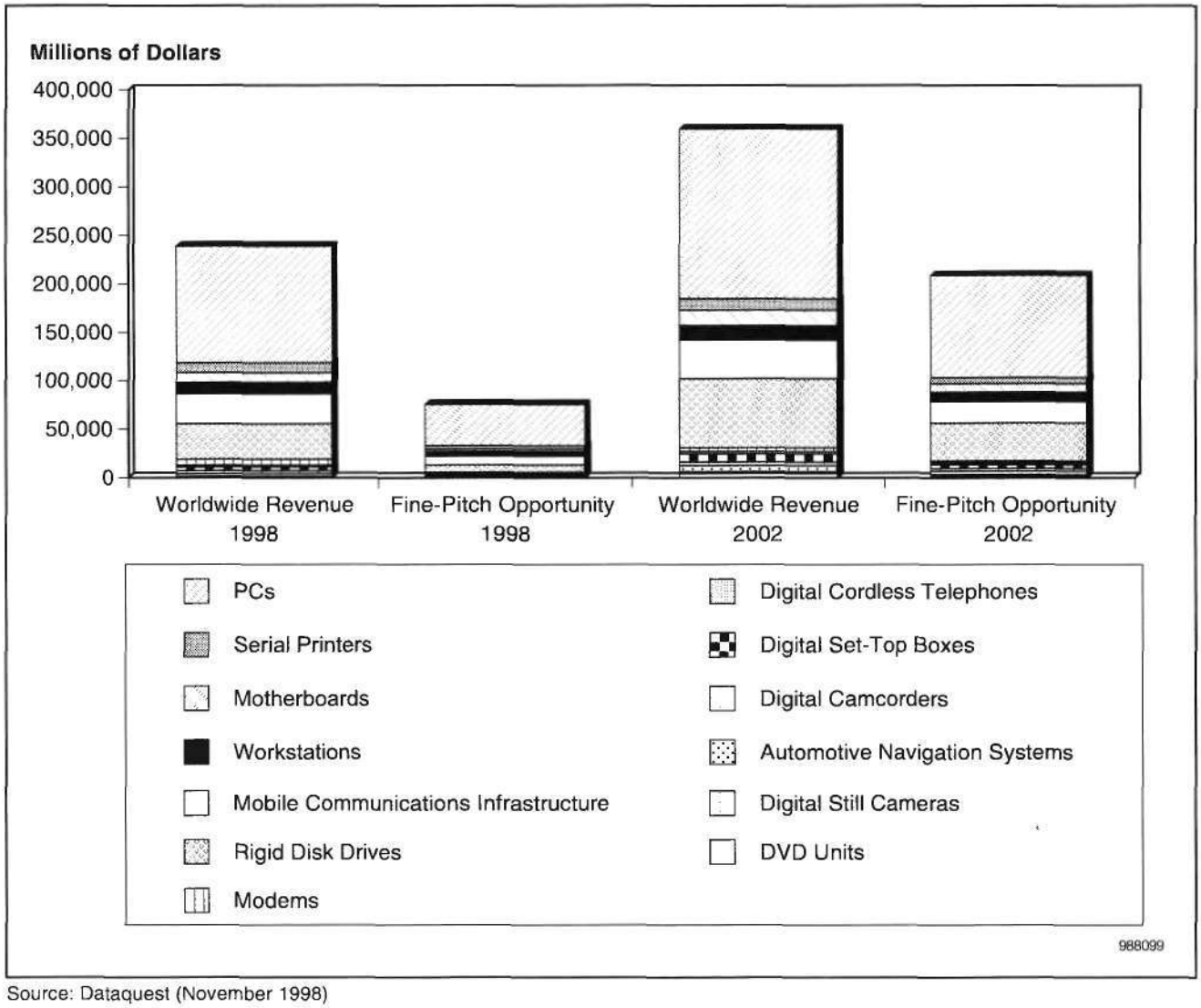
To increase their profit margins and distinguish their value-added products, many semiconductor manufacturers are positioning their emerging products and technologies for growth. They are offering new cost-effective, high-performance value-added product and technology solutions that meet various price points for both high-end and low-end systems. Manufacturers are concentrating their efforts on growth opportunities in the top emerging consumer, communications, and data processing equipment markets. In particular, wireless and digital consumer applications have the potential to enhance growth of digital signal processors (DSPs) and embedded and digital application-specific IC (ASIC) products. A large proportion of these value-added solutions will come from new and emerging package technologies. Figure 1 highlights selected applications that are revenue opportunities for new fine-pitch packages. These applications, in addition to next-generation digital consumer applications, PC cards, memory modules, switches and routers, base stations, thin server workstations, and notebook and laptop PCs, are increasing demand for small form-factor packages.

Figure 1
Selected Worldwide Semiconductor Application Opportunities for Fine-Pitch Packages (Millions of Dollars)



Source: Dataquest (November 1998)

Emerging Package Developments

The greatest package challenge in 1979 came from two electronics sectors. First, the consumer sector began its initial phase of growth of semiconductor content. Valued at less than $5 billion in the United States in 1970, the consumer sector's semiconductor content represented about 5 percent of total semiconductor consumption. Between 1970 and 1975, this percentage grew to 12 percent, which precipitated one of the greatest changes in semiconductor package technology. Through-hole technology remained king of the computer, industrial, and military sectors. Hybrids were the mainstay technology for communications and automotive equipment. However, the need for low cost and miniaturization drove the consumption of new small outline (SO) and chip carrier surface mount technology (SMT) packages that offered up to 5:1 area reductions and up to 84 input/output (I/O) pins. The improved parameters offered by SMT became critical in the consumer sector in watches, calculators, video games, clocks, handheld radios, disk cameras, and TVs. Development of these systems would not have been possible without SMT.

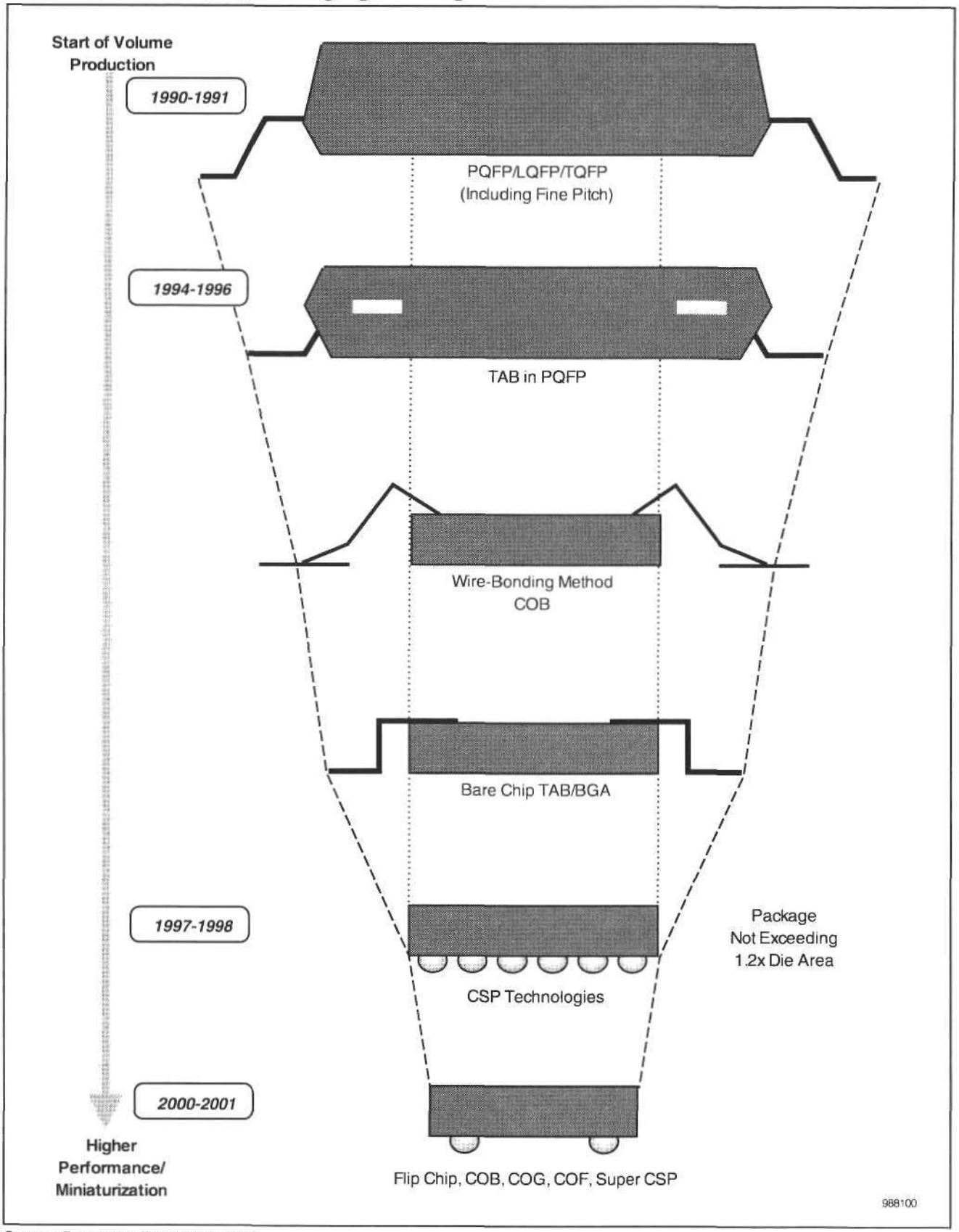
Second, the semiconductor industry's shift to VLSI technology and the rapid entry of Japanese companies into the DRAM markets pushed through-hole technology to its limits. SMT technology offered not only low cost and reduced board space, but also high I/O capability, improved electrical performance characteristics, and ease of handling by automated assembly processes. Japanese companies, by virtue of their majority share of the consumer business, their lead in automated assembly, and their strong SMT focus on SO for logic and memory devices, led the charge and changed the course of package history.

Current Market Status

Today's semiconductor package industry is in the throes of another major upheaval. Volume production is currently focused on shrink versions of existing SO and quad flat packages (QFPs). Advanced area array packages and attach techniques such as ball grid array (BGA), flip chip, multichip module (MCM), direct chip attach (DCA), column grid array (CGA), and chip scale package (CSP) formats are being designed in at a faster pace than previously forecast. Widely used in new applications, these packages meet the increased demand for miniaturization, lower cost, and improved electrical performance. Because of their chip-size appearance, many of these package techniques are lumped into the very popular market category now referred to as CSP.

By industry definition, a true CSP is a die size no larger than 1.2 times the size of the chip design. The Ultra BGA, microBGA and other advanced BGA packages with flip chip attach are advertised as CSPs. This marketing cognomen adds even more confusion to a market already overburdened with package-acronym proliferation. From a density point of view, a CSP by any other name is positioned between standard packages and wafer-level techniques such as flip chip, chip stacks, and DCA. These various technical idiosyncrasies or nuances will eventually be surpassed by volume design wins. Given the industrywide trend toward increasingly high-density ultra-VLSI designs, most of the latest CSP and BGA designs are feasible solutions for a wide range of applications. Figure 2 illustrates the evolution of some of these ultra-VLSI and system-level interconnect designs. Table 1 shows new technologies implemented by some of the major semiconductor companies.

Figure 2
Evolution of Emerging Packaging Techniques



Source: Dataquest (November 1998)

Table 1
Emerging Package Technologies by Selected Companies

	Fujitsu	Hitachi	Hyundai	Intel	LG Semicon	LSI Logic	Matsushita	Mitsubishi	NEC	Oki	Rohm	Samsung	Sharp	Sony	Texas Instruments	Toshiba	VLSI Technology
Product	SON	µBGA	µBGA	µBGA	BLP	Sharp agreement	MNPAC	FPBGA	D2BGA	µBGA	FµBGA	µBGA	-	TGA	microStar BGA	CSTP	FPBGA
CSP Technologies	FPBGA, µBGA, FC-BBG, BCC, SOC	T-TFBGA, P-TFBGA	-	-	-	SFP	QFN	P-FBGA	FPBGA, Mold BGA	Tab BGA, FC-BGA, WB-BGA, WB-LGA	TFBGA	-	µBGA	NT-CSP, FPBGA	-	µBGA, P-FPBGA	FPBGA
Terminal Pitch (mm)	0.5	0.8, 0.75, 0.5	0.75, 0.65	0.75	0.8, 0.65, 10.5	1.0, 0.8, 0.5	1.0, 0.8	0.8	0.8, 0.5	0.8, 0.75	0.8	0.75	1.0, 0.8	0.8, 0.5	0.8, 0.65, 0.5	0.8, 0.75	0.8, 0.5
Interposer Substrate Material	Lead frame	Polyimide	Polyimide	Polyimide	Polyimide	Polyimide	Ceramic (alumina)	Glass epoxy	Polyimide	Polyimide	Polyimide	Polyimide	Polyimide	Organic resin	Polyimide	Polyimide	Polyimide
Die Connection Technology	Wire bond	Beam lead bond	Beam lead bond	Beam lead bond	Wire bond	Wire bond	Flip chip	Wire bond	Wire bond	Beam lead bond	Wire bond	Beam lead bond	Wire bond	Flip chip	Wire bond	Wire bond	Wire bond
Die Electrode Layout	Peripheral/ center	Peripheral	Peripheral	Peripheral	Center	Peripheral	Peripheral/ full array	Peripheral	Adaptable to all types	Peripheral/ full array	Peripheral	Peripheral/ Center	Peripheral	Peripheral/ full array	Peripheral	Peripheral/ Center	Peripheral
Die Circumference (mm)	0.6	0.3, 0.5	0.5	0.5	0.6	0.5	0.4	1.0	0.5	0.5	1.0	0.3-0.5	0.5	1.0	1.0	0.3	0.3
Devices	Flash	DRAM, ASIC	SRAM	Flash	DRAM	ASIC	ASIC	DRAM	ASIC	DRAM, ASIC	ASIC	DRAM	Flash	ASIC	ASIC, DSP	DRAM, ASIC	ASIC
Volume Production	Now	Now	Now	Now	Now	Now	Now	Now	Now	Now	Now	Now	Now	Now	Now	Q4/98	Now
Proprietary CSP Technology	Yes	No (Tessera license)	No (Tessera license)	No (Tessera license)	Yes	No (Sharp foundry agreement)	Yes (joint development with Kyocera)	Yes	Yes	Yes	Yes	No (Tessera license)	Yes	Yes	Yes	Yes	No (Amkor)

Source: Dataquest (November 1998)

Traditionally, the time scale involved from package technology acceptance to implementation has been substantially longer than a semiconductor device or system application life cycle. To illustrate the time required for market penetration of a new package technology, the cycle has been divided into four phases, as shown on Table 2. We have attempted to position the new package categories (area arrays, CSPs, flip chip, and wafer level interconnects) in this time line.

Table 2
Emerging Package Technology Timeline, 1992 to 2010

Category/Description	Year of Adoption
Development	
Preliminary package design, selection of materials, process development, standards development	1992 to 1997
Prototype Use	
Sample shipment, reliability testing, socket and manufacturing equipment developments	1995 to 1998
Application Development	
Product evaluation, supply of printed circuit board and CAD tools	1996 to 1999
Volume Production	
Enhancement of product offerings, diversification of printed circuit board and CAD vendors, diversification of test tools	1998 to 2010

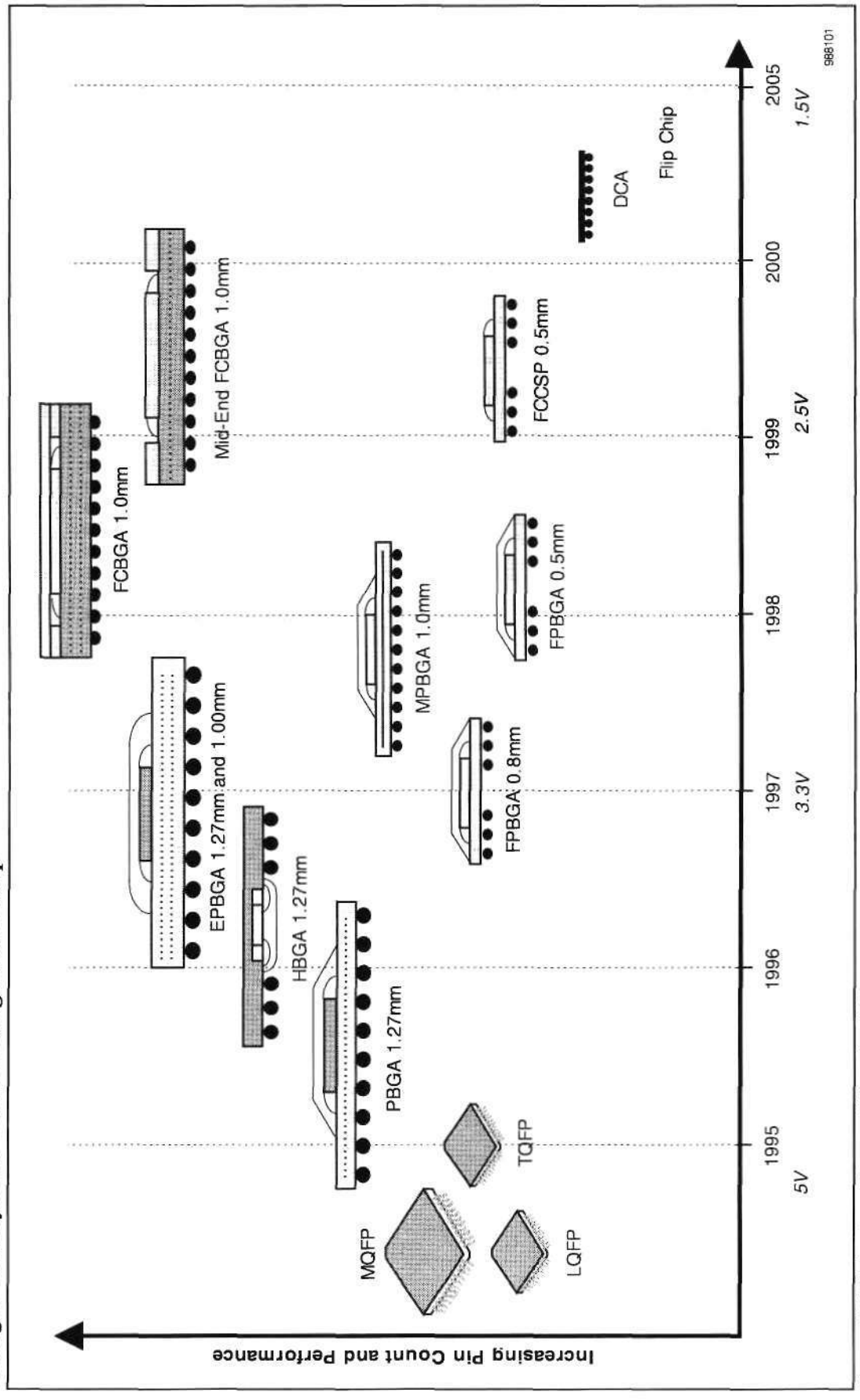
Source: Dataquest (November 1998)

Package Opportunities

From a demand side, the largest group of users of new miniature, below-100 I/O CSP designs will be suppliers of passive, discrete, flash memory, RDRAM, and optical components, IC cards, and memory modules. According to Amkor, about 80 percent of CSP designs have involved lead counts of between 28 and 48 pins.

The second-largest group of users for fine-pitch or CSP designs is the high-I/O ASIC suppliers. Figure 3 illustrates a road map littered with new CSP designs that will satisfy form factor requirements for ASIC users. This market is being driven by system cost, form factor and size, feature set, and time to market. VLSI Technology is shipping ASIC devices in 0.8mm fine-pitch BGAs (FPBGAs), in volume (over 1 million) in the fourth quarter of 1998. The second-generation 0.5mm FPBGAs will be shipped in 1999. These products were designed for the wireless/portable market. Suppliers such as VLSI Technology, LSI Logic, and Xilinx and equipment manufacturers such as Ericsson, Nokia, QUALCOMM, and Motorola all agree that the new FPBGAs, which will represent 10 percent of the handset market in 1999, could represent almost 50 percent of that wireless market by 2000. For many of the ASIC designs in the high-lead arena, current FPBGAs are priced at 1.2 times the cost of a thin quad flat package (TQFP) design.

Figure 3
A High-Density Fine-Pitch Package Road Map



Source: VLSI Technology, Dataquest (November 1998)

In the memory category, flash memory suppliers entered the CSP market using various microBGA designs. The larger-volume DRAM suppliers could turn the tide of capacity challenges when and if they switch package designs from thin small-outline packages (TSOPs) to some of the new, smaller BGA designs. As cost per lead of CSPs and BGAs reaches parity with comparable TSOP and QFP designs in 1999, the capacity of advanced packaging technologies could become constrained.

In the memory area, some of the most recent announcements from Mitsubishi include new molded CSP (M-CSP), multichip package (MCP), and stacked MCP (S-MCP) designs for SRAMs and flash memories. Mitsubishi and Sharp are collaborating on common pin compatibility and package size configurations. Xicor has introduced the XBGA for EEPROM. Toshiba and Fujitsu have jointly agreed on the BGA MCP design, which allows mounting of both SRAM and flash in a single package. This new configuration takes up about 70 percent less space than two TSOPs. In volume production, the new MCP will be priced the same as a flash and an SRAM in separate TSOP packages.

In the logic area, Integrated Device Technology, Philips Semiconductors, and Texas Instruments have jointly agreed to source several logic device designs in new low-profile fine-pitch BGAs (LFBGAs) with 0.8mm 96-lead designs. Compared to thin shrink small-outline packages (TSSOPs), the new LFBGAs reduce board space up to 65 percent for the same functionality. The companies have announced that these new designs are up to 50 percent more efficient at dissipating heat than TSSOPs.

Technology Advantages and Disadvantages

It is not the role of Dataquest to sing the praises or assess the capability of one supplier's or subcontractor's package over another's. It is important to report the user concerns about the advantages or disadvantages of various technologies. Many of the advanced BGA and CSP designs proliferating in the market pose multiple challenges, obstacles, and advantages that need to be addressed before complete market acceptance is reached. Some of these obstacles include the following:

- Limited test techniques and higher test costs
- Narrow terminal pitch width
- Increased costs of wiring patterns on PCs
- Lack of standards on lead and package design
- Test socket connection
- Standardization on tape and reel
- Assembly-handling equipment
- Visual inspection equipment requirements
- Routing, signal integrity, thermal, and mechanical issues

Some of the advantages include the following:

- Smaller form factor than standard SO and QFP packages

- Board space savings from miniaturization
- Higher chip performance because of electrical and thermal characteristics
- Lower power consumption in application
- Lower system board cost

Some of the design challenges result from increased demand for alternative technologies, which now include flip chip attach and known good die. Most of the latest advanced BGA and CSP designs have reached the 0.8mm-to-0.5mm ball pitch required for the 0.35-micron-to-0.25-micron device regime. The high cost of substrates, assembly techniques (either flip chip or wire bond), smaller die, and smaller pad pitch require a more advanced regime of testing, handling, and inspection and CAD tools not readily available. Ultimately, the level of market penetration will govern the price. A technology cannot achieve the lowest possible cost unless it follows the learning curves determined by very high-volume production. Any advanced package technology involves certain risk until official standards or pseudo-standards are established to determine a "technological winner."

Dataquest Perspective

The semiconductor industry has entered the age of system-level integration (SLI) for ASICs and embedded applications for memory, microprocessor, DSP, and other logic products. It has become imperative for semiconductor suppliers and package subcontractors to respond effectively to the needs of application equipment vendors. Advanced package developments, analyzed in this light, promise to be a haven for profit and growth. Historically, most semiconductor companies have developed products on the basis of supply-side dynamics, but they lacked the marketing savvy to serve the needs of the application market. Their future success will be based on their ability to cooperate with subcontractors (foundry and assembly). The shift from 0.8mm to 0.5mm and below pitch packages will involve a tremendous technological challenge over the next few years. The differences among the various BGA- or CSP-type designs and standards being proposed clearly indicate that all efforts must be directed toward package miniaturization, increased lead counts, and low cost. As the industry drives semiconductor process technology into the realm of 0.18-micron geometries between 2005 and 2010, the next package challenge will be faced by the users and developers of the DCA and flip chip technology platforms.

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Perspective

ASIC/SLI Worldwide

Dataquest Predicts

Application-Specific Programmable Products: The Coming Revolution in System Integration

Abstract: *With single-chip systems becoming more reality than daydream, system-level integration (SLI) is one of the few hot areas in semiconductors, with a projected growth rate far in excess of the market as a whole. For the next few years, SLI will progress in an evolutionary fashion, but with the development of embedded programmable logic the industry is facing dramatic change. The emergence of a new product category—application-specific programmable products—will take SLI to the next level of market penetration, but could spell disaster for some standalone programmable logic device (PLD) manufacturers.*
By Jordan Selburn

The March toward Single-Chip Systems

At present, the revenue from system-level ICs—more than $7 billion in 1997—is derived principally from a comparatively small number of high-volume designs, some of which exceed $200 million per year of peak sales. These designs merit the large engineering teams and effort that system-level integration (SLI) vendors allocate to the job. Conventional wisdom states that for system integration to achieve its full potential, the roadblocks to design reuse (the only practical solution to the "design gap" between the silicon's capabilities and those of the average designer) must be eliminated. Major industrywide efforts such as Virtual Socket Interface Alliance (VSIA) are under way to achieve practical and widespread reuse of intellectual property (IP) cores. However, there is an alternative scenario that allows for strong SLI growth strictly from high-volume designs: the application-specific programmable product (ASPP), which can expand the role of system-level design from the few highest-volume designs to the average OEM.

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System Integration beyond 2002: The Supercomponent of the Future

Clearly, SLI will continue to grow both in absolute terms and in market share beyond 2002. The magnitude of this growth is difficult to quantify, but there are some interesting possibilities concerning how this growth will be driven. Perhaps the most interesting, and to our view a highly likely, prospect is something Dataquest refers to as the application-specific programmable product. An ASPP is essentially an application-specific standard product (ASSP) with embedded programmable logic, which can be used to provide additional features specific for each design. Also the embedded programmable logic can modify existing functions placed on-chip by the semiconductor vendor, allowing a single manufactured part to meet multiple standards (such as differing communications protocols or modulation schemes) depending on how the chip is programmed.

ASPP Advantages

One issue with standard products is that, despite the significant advantages ASSPs provide for SLI vendors and customers, it is difficult to deliver exactly what the customer wants to buy; this was the problem with embedded array ASICs. Another limitation is that, as a standard product, by definition every customer is purchasing the same part, and therefore the ASSP does not enable any end-product differentiation. This approach is fine for mainstream system manufacturers without leading-edge systems expertise, which primarily differentiate themselves on a price, distribution, support, or other nontechnical basis. However, it is not an optimal approach for those OEMs that need advanced product features in order to distinguish their goods. By allowing user customization, ASPPs take the standard product approach, yet deliver unique functionality to each system OEM.

For the semiconductor vendor, the high volume of SLI standard products represents the closest thing available to the manufacturing efficiency of microprocessors or DRAM. With a few exceptions, single-customer parts are low in volume and make inefficient use of increasingly expensive fab capacity. The long-term move to larger wafer sizes compounds this problem. Table 1 shows an approximation of the wafer requirements for a typical consumer SLI chip, assumed in this case to be 7mm/side and built with a fairly mature process technology having a defect density of 0.3/cm^2. This analysis also assumes a production volume of 1 million parts per year, which for SLI ASICs or ASSPs is quite a high-volume application.

Table 1
Annual Wafer Requirements for Typical SLI Design

Manufacturing Equipment	150mm	200mm	300mm
Net Die per Wafer	269	501	1,169
Net Die per 24-Boat Wafer	6,456	12,024	28,056
Wafer Requirement per Year	3,717	1,996	855

Source: Dataquest (August 1998)

What becomes clear is that the economics of semiconductor manufacturing will force vendors to maximize the production volume of their designs.

Except for the very rare ultra-high-volume SLI ASICs, manufacturing parts for a single customer is inefficient even in a small wafer fab and will become much more so when the equipment moves to the 300mm standard. In fact, without some way to expand the unit volume per design, logic vendors may never move beyond the 200mm equipment set, putting them at a disadvantage compared with vendors that find a way to fill a 300mm wafer fab efficiently. ASPPs address this issue by providing a way to build and sell a single SLI part to a broad range of OEMs.

The First Step toward ASPPs: Embedded Programmable Logic

Several recent product announcements have started the move toward combining fixed and programmable logic. In April of 1998, Lucent Technologies and Chip Express announced plans to develop what they term laser-programmable system chips (LPSCs). These are Lucent cell-based ASICs with embedded blocks of Chip Express' laser-programmed gate array. Lucent followed this announcement with a field programmable peripheral component interconnect (PCI) interface chip, consisting of a 64-bit, 66-MHz PCI controller and I/Os implemented in a cell-based architecture with 30,000 to 60,000 gates of programmable logic. Other companies have since announced similar parts.

So far, the main goal of this type of product is to reduce development time, using the programmable logic's flexibility in two ways. First, the manufacture of the chip can begin while some of the logic—the parts to be implemented in the programmable logic device (PLD) blocks—is still being designed. Second, at least some errors can be fixed quickly by changing the programmable logic, minimizing the need for any mask-level changes. There are competing solutions, but the embedded PLD approach provides for virtually instant turnaround.

In the long term, however, embedded PLD can bring much, much more to system-level designs. Making ASPPs by adding programmability to ASSPs brings a host of benefits to both the system OEM and the SLI vendor. ASPPs allow OEM that are systems experts to add new features and state-of-the-art capabilities to their products while using off-the-shelf parts. The OEM lacking systems knowledge build a mainstream system and use core competencies in other areas such as manufacturing and distribution to differentiate their products. Both types of customers purchase the same ASPP component, but they are buying very different capabilities. Product development time, so crucial in short-lived consumer-oriented products, is also minimized as the semiconductor manufacturing cycle is substantially reduced or even eliminated for all design iterations.

The semiconductor vendor also benefits mightily. The increasingly expensive manufacturing capacity is used more efficiently through the aggregation of multiple customers. Just as if not more important is the leveraging of scarce engineering resources.

ASPP Applications: The 100,000-Foot View

The set-top box of the future serves as an example of what can be accomplished with ASPP technology. The set-top box has the characteristics

of an ideal ASPP application. The overall volumes are very high, but there is no one OEM that dominates the market; it would take multiple SLI designs but just one ASPP to address the majority of available market. Most of the functionality within a set-top box must conform to industry standards. ASPPs deliver the embedded IP cores to meet these standards in a way that guarantees functionality in silicon yet still allows for a differentiated design. Also, the short lifetime of a consumer product requires a rapid design and manufacturing cycle. As off-the-shelf parts, ASPPs can be delivered while the final design effort is still under way, and redesigns take no manufacturing time at all. Similarly, ASPPs can serve as software development platforms and enable true hardware and software co-design.

What would this part look like? In addition to the microprocessor, DRAM, and some type of nonvolatile memory included on-chip, one advantage to the ASPP approach could come from IP cores enhanced to support multiple standards and formats. For example, it may be possible to build a universal demodulator block with a core of common cell-based logic and programmable logic used to set the demodulator for QAM, QPSK, VSB, or other formats. The same could hold for the transport section, audio and video decompression functions, and so on. Programmable logic could also be used for conditional access, depending on the way in which it is physically built on the chip. Finally, additional blocks of programmable logic would serve as a means for OEMs to differentiate their products.

ASPP Time Frame

For the embedded PLD approach to be practical in the high-volume consumer-oriented applications, it must be economically as well as technically feasible to integrate sufficient logic on-chip. This means that the programmable logic must be dense enough to not dominate the die, yet still provide OEMs with the flexibility that they need. Table 2 gives a rough forecast of the time required to integrate 200,000 gates of programmable logic economically. The choice of 200,000 gates was made because it represents the average cell-based design of 1997 and should provide the OEM with substantial differentiation possibilities. Other assumptions include a target die size of 7mm/side; the programmable logic is allowed to occupy 20 percent of this area, or 14.8 mm^2. Under these conditions, the addition of the PLD block will add roughly 20 percent to the die cost (assuming a compatible semiconductor process and discounting yield effects) and probably less than 15 percent to the finished part cost. The ASIC logic density forecast is slightly modified from the Semiconductor Industry Association technology road map, and it is assumed that programmable logic remains roughly 5 percent of the density of cell-based logic.

From Table 2, it is clear that around the 0.07-micron generation it should be both technically and economically feasible to develop ASPPs with sufficient embedded programmable logic. Depending on the specific application requirements, ASPPs could be practicable in the 0.10-micron generation and perhaps even as early as the 0.13-micron generation. Dataquest suspects that many application areas would require substantially less than the 200,000 programmable gates used in the example, accelerating the arrival of the time when embedding programmable logic will be practical. Therefore ASPPs

should be widely available by 2009 and potentially by 2003. This prediction has major implications for the programmable logic industry.

Table 2
Programmable Logic Area Road Map

Generation	ASIC Logic Density (Gates/mm^2)	PLD Logic Density (Gates/mm^2)	Programmable Logic Area (200,000 Gates)
0.18-Micron	50,000	2,500	80 mm^2
0.15-Micron	60,000	3,000	67 mm^2
0.13-Micron	90,000	4,500	44 mm^2
0.10-Micron	140,000	7,000	29 mm^2
0.07-Micron	240,000	12,000	17 mm^2
0.05-Micron	360,000	18,000	11 mm^2

Source: Dataquest (August 1998)

The Decline and Fall of PLDs?

How does the ASPP affect the standalone PLD industry? It is important to distinguish between programmable logic *functionality* and programmable logic *devices*. While the use of programmable logic will increase substantially over the next 10 years or so, Dataquest feels that the impact of ASPPs on PLDs is likely to be severe, perhaps even catastrophic. When one looks at how PLDs are used, it seems clear that embedded programmable logic has superior attributes for almost all applications.

Today's dominant PLD companies are emphasizing system solutions using "soft" IP blocks. This approach provides maximum design flexibility; however, the embedded programmable logic in ASPPs can provide equivalent usable flexibility—that is, the ability to modify those parts of the design that are most likely to benefit from modification. ASPPs also offer the needed I/Os in the right physical location, a difficult feature for PLDs to match. PLDs also can be used for immediate design turnaround, which is especially handy for system emulation, while ASPPs are still on the drawing board. This capability provides only a short-lived advantage, though. Once an ASPP solution is available, the roughly 20x PLD logic area penalty means that standalone PLDs will be unable to compete on a cost, performance, or power basis with ASPP alternatives. Also, the performance edge allows ASPPs to deliver at-speed emulation.

Of course, this represents one possible scenario, and there are also considerations that argue for continued growth in standalone PLDs. There will continue to be a market for PLDs in areas such as relatively small pure logic designs; this market is likely to grow for the next several years at the expense of gate arrays. In the not-too-distant future, it may be difficult for cell-based ASICs to address designs below 1 million logic gates economically without a breakthrough in I/O placement technology. For these designs PLDs may, at some point in the future, attain cost parity or even superiority to ASIC solutions by using 300mm manufacturing equipment sets to reduce costs.

Additionally, if the system requirements for programmability remain beyond what can be reasonably embedded, standalone PLDs will continue to have a place in the system ecology. It does seem difficult to conceive that system designers will need or want to program multimillions of gates for each system, although it is never wise to underestimate the technology needs of future systems.

Dataquest Perspective

In the long term, the future looks bright for a new class of product: the ASPP. The ASPP brings attributes that make system integration attractive to manufacturers and a broad range of customers alike, fueling the continued growth of the SLI market. ASPPs represent very bad news, however, to the standalone PLD vendors. Dataquest recommends that, in order to catch the full benefit of the ASPP market, ASIC and ASPP vendors begin investigating embedded PLD technology immediately. One way to do so could be through a partnership with (or the acquisition of) one of the small standalone PLD companies. These companies may have solid technology but have encountered difficulty finding a place in the PLD sales channel. Also, the revenue from such a partnership, whether in the form of royalties or engineering fees, could make the difference between survival or failure for a small PLD company.

The larger PLD companies are likely to face the biggest threat from ASPPs, and yet would benefit least (at least on a percentage-of-revenue basis) from such a partnership. These vendors are looking to move into the SLI space on their own, primarily using soft IP for a time-to-market advantage. Dataquest feels that ASPPs provide a much too attractive alternative for the multimillion gate PLD approach to succeed, however, and the dominant PLD vendors will need to seriously reconsider their business model in order to avoid catastrophic consequences.

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Perspective

ASIC/SLI Worldwide

Market Analysis

System-Level Integration: The Near Term

Abstract: *With single-chip systems becoming more reality than daydream, system-level integration (SLI) is one of the few hot areas in semiconductors, with a projected growth rate far in excess of the market as a whole. For the next few years, SLI will progress in an evolutionary fashion, with the market growing to $27 billion in 2002. Not surprisingly, the SLI market is attracting many new entrants. The battle will be between ASIC and ASSP solutions, with the winners determined by systems and manufacturing expertise.*
By Jordan Selburn

The March toward Single-Chip Systems

The concept of system-level integration (SLI) has been discussed since at least the early 1990s. In just the past year or so, however, we have seen the first steps toward the system on a chip becoming a mainstream solution. Why has this development taken until now? It has been possible to put a system's worth of gates on a chip for a few years, but in 1997, with 0.35-micron manufacturing technology becoming widespread and mature, it has become economically feasible as well. Also, we are starting to see types of functions other than logic becoming commonly available, to the point that it seems that virtually every ASIC vendor in existence is claiming to differentiate itself with its mixed-signal offering. Embedded memory is also becoming a standard feature, with at least half a dozen companies offering embedded DRAM and several offering embedded flash. Lastly, the infrastructure to support design reuse, both in the availability of intellectual property (IP) cores and a design methodology supporting their usage, is beginning to emerge, although a robust design reuse solution remains on the horizon. All of the pieces to the SLI puzzle are being put in place. This Perspective takes a look at the evolution of the SLI market over the next few years.

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SLI: A Look at the Near Term

The benefits of integrating a system on a chip are widely known. In the right system, SLI can lower overall cost. It is important to note that by no means do all of today's systems fall into this category; as an example, most of the embedded DRAM applications today are more costly than component DRAM solutions. System performance can also be improved both through physical effects (elimination of I/Os and printed circuit board traces as well as closer proximity of functions) and through enhanced architectures such as very wide memory buses. The system form factor is reduced. Perhaps less commonly stated as a benefit of SLI is reduced power consumption; this may actually be the primary reason for integration of many of today's SLI applications.

SLI Revenue Forecast

The key, and perhaps the only, measure of success of a product in the market is whether or not the customer will buy. Many technically elegant products, such as the Beta format VCR currently rusting in this author's garage, have failed in this test.

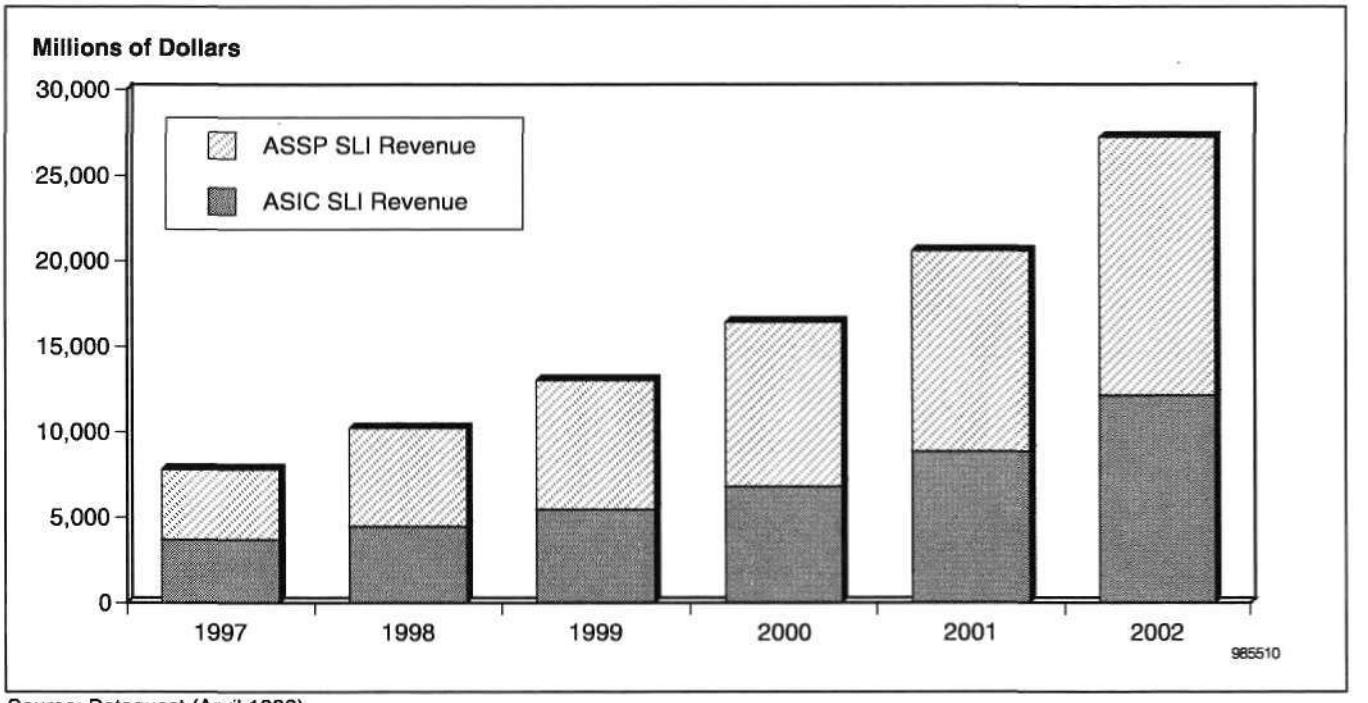
Dataquest has expanded the definition of SLI to include application-specific standard product (ASSP) as well as ASIC solutions. Figure 1 shows the current and forecast revenue for ASIC and ASSP SLI semiconductors; it is clear that system integration is already a success and will become a significant part of the semiconductor market within a few years. In 1997, total SLI revenue already exceeded $7 billion, and by 2002, system-level semiconductors will represent almost 50 percent of the total combined ASIC and ASSP market. Although Dataquest has not made any quantitative forecast for the market beyond this time frame, SLI will certainly continue to grow in semiconductor market share as well as in absolute numbers.

Forecast Enhancers and Inhibitors

A point forecast represents a nominal outcome. A number of factors could substantially change the amount of SLI revenue over the forecast period, including the following:

- The continuation of financial difficulties throughout Japan, their spread into China resulting in a currency devaluation, or both of these would affect the entire electronics industry and significantly decrease SLI revenue.
- Equivalent financial crises in Europe or North America would similarly affect the SLI market.
- A rapid market acceptance of digital video products, particularly new applications such as digital television, would increase SLI revenue.
- The introduction of a compelling new PC application, such as practical voice recognition, would be a positive influence.
- A continued collapse beyond historic norms of standalone component prices would delay the ramp of SLI.

Figure 1
SLI Revenue Forecast through 2002



Source: Dataquest (April 1998)

- The failure of various standards such as Virtual Socket Interface Alliance (VSIA) to facilitate the rapid and widespread dissemination of IP cores would significantly hinder the growth of the SLI market. Conversely, a solution in the next year or so (sooner than Dataquest expects) would enable foundries to participate in the SLI market more rapidly than forecast and increase SLI revenue.
- Unforeseen manufacturing difficulties, for example a lack of direction in 0.13-micron lithography, would delay the next generation of integrated solutions and hinder the SLI market.

ASIC versus ASSP Solutions

Dataquest has broadened the definition of SLI to include ASSPs. At present, ASSPs make up slightly more than one-half of the SLI market. The dominance of standard over custom integrated solutions will continue and likely expand in the future. ASSP solutions provide advantages for both the vendor and customer. To the system designer, ASSPs provide a rapid time to market and guaranteed functionality. In some instances, the standard product approach can enable an OEM with no system expertise to quickly enter growing markets—for example, cellular handsets. Several SLI vendors offer cellular phone chipsets and development platforms. For the SLI vendor, ASSPs allow maximum return on development efforts by making possible the sale of the same part to multiple customers. Also, building standard parts in high volumes can allow for manufacturing economies of scale difficult to match with custom ASICs.

However, the custom ASIC solution allows the OEM that is systems-savvy to differentiate its product. New innovations in system features or architecture, pioneered by the OEM, will appear in ASICs before becoming available as ASSPs. An ASIC could also allow for higher performance and smaller die size if the competing ASSP contains "everything but the kitchen sink" in order to appeal to a broad customer base. Still, given the commodity nature of many consumer products, we expect that ASSPs will retain the majority of SLI revenue for the foreseeable future.

SLI Application Focus

Not all application areas (consumer, data processing, and so on) are adopting SLI at the same rate. Given today's technology, and the very low price of some standalone components such as DRAM, the main advantages from SLI are reduced power consumption and a smaller form factor. This is the reason wireless communications, for example, is a leader in adopting SLI. Many fixed-location, wall socket-powered consumer products, in contrast, are driven almost exclusively by cost and will move more slowly toward SLI as the economics begin to favor integrated over discrete solutions.

SLI versus Embedded Components, 1998 to 2002

One area of concern for manufacturers of standalone memory and analog components is the effect that SLI will have on their business. At present, the mixed-signal capabilities of most system-level vendors do not match the precision analog capabilities of standalone components. About 70 percent of the analog market falls into this category and is currently out of reach of most SLI manufacturers. Most SLI vendors do, however, offer a substantial selection of digital-to-analog and analog-to-digital converters (DACs and ADCs) for mainstream applications and could impact the remaining 30 percent of the analog business. Over the next five years, the impact of SLI on standalone analog is likely to increase as more and more vendors introduce precision analog product enhancements such as dual-poly and embedded BiCMOS processes.

DRAM is currently the most interesting of embedded memories. SRAM is already mature and flash is too new to have much impact on the component markets over the next five years. In contrast, embedded DRAM is now available from a number of vendors, yet has only begun to find a market. A year ago embedded DRAM appeared ready to take the ASIC and ASSP world by storm, but the overall slowdown in the electronics industry and the continued free fall in commodity DRAM has limited the market for embedded solutions to the mobile and high-performance markets.

The following is Dataquest's preliminary forecast for ASICs and ASSPs with embedded DRAM, in millions of U.S. dollars:

- 1997: 125
- 1998: 326
- 1999: 1,055
- 2000: 2,888
- 2001: 5,010
- 2002: 7,496

By 2002, Dataquest forecasts that 25 to 30 percent of system-level chips revenue will come from components with embedded DRAM.

Making SLI a Mainstream Solution

At present, only a few semiconductor vendors have any type of rigorous approach to system-level design; even among the leaders, each design requires substantial engineering effort and time. Although the SLI market is already showing strong growth, rapid expansion can continue only if system integration moves within reach of the average OEM. This result may occur in different ways:

- VSIA, or some other standard, must be put in place to achieve the goal of making IP cores as easy to use as logic gates, and these cores must be easily reusable across vendors and across process generations.
- The architecture of ASSPs must change to allow for rapid and easy modification, broadening the potential customer base for this standard-part SLI approach.

Both solutions are likely to happen, and there is already progress on each front. Although more effort seems to be placed on the "IP cores as Lego block" standards solution, Dataquest feels that ultimately the ASSP approach provides greater benefits to a majority of users, particularly in terms of time to market, and will fuel SLI growth in the long run.

Dataquest Perspective

The move toward SLI is accelerating with a forecast growth well beyond that of the overall semiconductor market. The impact of SLI on today's vendors will be profound, and companies that position themselves well will be able to thrive. How can a company do so? Dataquest feels that the key is understanding the system market and the features that provide true differentiation and added value. More and more vendors are jumping on the SLI bandwagon, and it does not appear that this system market understanding is widespread. Too many companies are placing their bets on commodity offerings without recognizing that they have serious competition. These companies do not acknowledge that IP has a life cycle just as any other product does, and they try to differentiate themselves with a core offered by many other vendors.

Where will this trend lead? Some few companies will continue to offer added value in the form of advanced technology, whether that means higher performance, true hardware and software co-design, or other capabilities not offered by many competitors. These vendors, which understand that having the same ARM7 processor or 8-bit DAC as the rest of the industry does not differentiate their offerings, will survive and command above-market profit margins. Other vendors—including some foundries—with the lowest cost manufacturing can make a living in the commodity SLI market with reasonable margins. It will be a difficult road for the remaining SLI vendors, particularly those with insufficient resources (or resources poorly invested) to stay ahead of the pack technologically or economically. It is hard to imagine a scenario in which there are several dozen truly successful players in the SLI market. When the dust settles in 10 or so years, expect to see a couple of technology leaders, a few huge manufacturing conglomerates, a handful of vertically integrated companies, and perhaps a dozen major IP vendors.

Now more than ever, the ASIC and ASSP worlds are at a crossroads. SLI brings the promise of a larger piece of the semiconductor pie, but also the risk that any changing market brings. In 10 years, the structure of the SLI market will look very different from today, and we will see a few companies that are wise (or lucky) prosper. Strategic planning, and a mind-set that looks beyond the next quarter or the next three years, will make the difference between the quick and the dead.

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Perspective

ASIC/SLI Worldwide

Dataquest Predicts

Embedded DRAM Revisited

Abstract: *DRAM embedded in ASICs and application-specific standard products (ASSPs) seemed poised in 1997 to take system-level integration (SLI) to new levels. Dataquest forecast immediate strong growth continuing steadily for the next five years; however, we did raise a warning flag regarding the decline in standalone DRAM prices. Combined with the global electronics slowdown, this has caused Dataquest to review the embedded DRAM market. While we still envision significant opportunities, the growth ramp no longer appears so soon nor is quite as strong.*
By Jordan Selburn

What Changes a Year Hath Wrought

In 1997, Dataquest made its first forecast for system-level ASICs and application-specific standard products (ASSPs) that incorporated embedded DRAM with logic. Embedded DRAM was one of the most interesting areas within the semiconductor industry, generating a great deal of excitement as company after company announced either products or development efforts bringing logic and DRAM together on a single chip. In the intervening year, there have been some significant changes to the industry that mandate a second look at the status and future prospects for this type of component.

Perhaps the most significant change from Dataquest's initial look at the embedded DRAM market is not a change at all, but the continuing free fall in standalone DRAM prices. A year ago, DRAM pricing seemed to hit the ground floor but there turned out to be a deep basement—memory prices have fallen by yet another two-thirds. The impact on embedded DRAM is profound, and applications driven primarily (in some cases, exclusively) by price will hold off moving to an embedded solution.

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Another change is a slowdown in the perceived momentum behind embedded DRAM. There are fewer product announcements and less coverage in the press than was seen in the latter half of 1997. Does this reflect a real change, though? Not really—it is just inevitable that what was at one point the latest and greatest innovation becomes mundane as the technology becomes mainstream (or at least is perceived to be mainstream). In the automobile industry, it is no longer news when somebody introduces air bags; the same will hold for on-board navigation systems in a few years. In the world of semiconductors, the "excitement life cycle" is even shorter. Another reason for perceived lack of media attention is the diminishing number of new product announcements—most of the companies that are committed to today's embedded DRAM market have already introduced products; most of the other vendors are choosing to remain on the sideline for now.

Embedded DRAM Competition

A number of companies have jumped on the embedded DRAM bandwagon in the past 12 months. The spectrum of participants ranges from companies making embedded DRAM their main product focus to those with the technology ready, yet unwilling to enter until the market matures somewhat. This latter category is new—the distinction used to be those companies with embedded DRAM technology felt the market was ready now. Following is an overview of some of the leading players in the embedded DRAM arena.

Semiconductor Companies

- **IBM:** While IBM has a very advanced process technology and offers embedded DRAM through its foundry services, there are currently no firm plans to release embedded DRAM ASICs or ASSPs. It is certain, however, that IBM could release embedded DRAM ASIC products with very little notice and enter this market at any time. With very high-performance logic and trench capacitor DRAM, IBM should be considered as strong competition, particularly in applications such as workstation graphics and high-speed data communications.
- **Toshiba Corporation:** Toshiba is betting very heavily on the success of the embedded DRAM marketplace. Virtually the entire ASIC product strategy has been built around embedded DRAM using Toshiba's trench capacitor process. The trench capacitor DRAM, developed in partnership with IBM, Motorola Incorporated, and Siemens, should allow for higher-performance logic capability than is possible with the stacked capacitor alternative. Toshiba's product allows integration of up to 128Mb of DRAM, which, along with Siemens, is the current leader for embedded memory density.
- **NEC Electronics Inc.:** NEC has had the ability to embed DRAM for some time, being able to incorporate up to 64Mb in its 0.25-micron CB-C10 ASIC product. However, for some undisclosed reason, the embedded DRAM option has not been offered as a general capability but rather on a selected basis only. This might be an indication that embedded DRAM

has not been truly productized yet, but rather requires a substantial amount of manual effort to implement.

- **LSI Logic Corporation:** In June 1997, LSI and Micron Technology announced a technology partnership to develop merged logic and DRAM products. The originally stated goal was for production silicon in 1998. Given that embedded DRAM was not mentioned as a capability in LSI's 0.18-micron G12 technology introduced in the spring of this year, it seems highly unlikely that this milestone will be met.
- **VLSI Technology Inc.:** No products have been announced containing embedded DRAM. VLSI's primary focus area—the wireless communication market—will not be a leading adopter of embedded DRAM technology, so VLSI is putting its efforts into other areas for the time being. It should be noted, however, that VLSI's longstanding technology partnership with Hitachi could allow for a relatively rapid product development introduction.
- **Lucent Technologies:** Rather than follow the throng with an embedded DRAM ASIC product, Lucent has gone in a different direction. The emphasis here has been a leadership position in other technologies such as embedded Flash and embedded programmable logic devices (PLDs). Given its focus on the communications market including data communications, however, it seems unlikely that Lucent will delay much longer in developing an embedded DRAM capability, which would give the company the ability to integrate virtually every system function, with the exception of high-frequency RF and microwave.
- **Siemens:** Until recently, Siemens has not been a factor in the ASIC market, but it has just announced an embedded DRAM product. Based upon a 0.24-micron silicon process and trench capacitor DRAM, Siemens has the capability to combine 128Mb of DRAM with 1M gates of logic. Initial production has already begun.
- **Samsung Semiconductor Inc.:** No mention of the DRAM world would be complete without Samsung. Not surprisingly, Samsung places a great emphasis on its embedded memory capability (DRAM, Flash, and dense 4T SRAM). Despite a major push in the ASIC area, however, Samsung remains a generation behind the industry leaders.
- **Foundries:** In addition to ASIC vendors, several of the leading contract manufacturers, including Taiwan Semiconductor Mfg. Co., are offering embedded DRAM products. While the level of interaction is somewhat more distant than with ASIC vendors, the foundries are able to offer a very low wafer cost alternative and a compelling solution for some customers. The process technology, and therefore density, tends to lag traditional ASIC manufacturers, however, which may offset the lower wafer cost.

Embedded DRAM Generators

The past year has also seen the emergence of third-party memory generators for embedded DRAM. The first company to enter the market was Silicon Access, whose products offer embedded DRAM blocks ranging up to 18Mb with up to 288 I/Os. Mosaid also has an embedded DRAM compiler. Other

leading third-party memory vendors, such as Virage Logic Corporation, Dolphin Integration, and Artisan Components Inc., have not yet announced any embedded DRAM generators, but are almost certainly developing some products as well.

It should be noted that the need for embedded DRAM generators may not be as great as for SRAM. A compiled embedded DRAM block is convenient and allows for an exact solutions, but there are some inevitable inefficiencies. As an alternative, a semiconductor company can develop a relatively small range of combinable fixed DRAM blocks (1Mb and 4Mb in a few bit-widths), which would allow for close to optimal solutions that may be superior to a compiled memory.

The Embedded DRAM Forecast: Down, Down, Down

The changes in the semiconductor market, and for that matter the global economy, over the past year will have a major impact on the adoption of embedded DRAM products. The effect in almost every case is to lower the forecast for products using embedded DRAM.

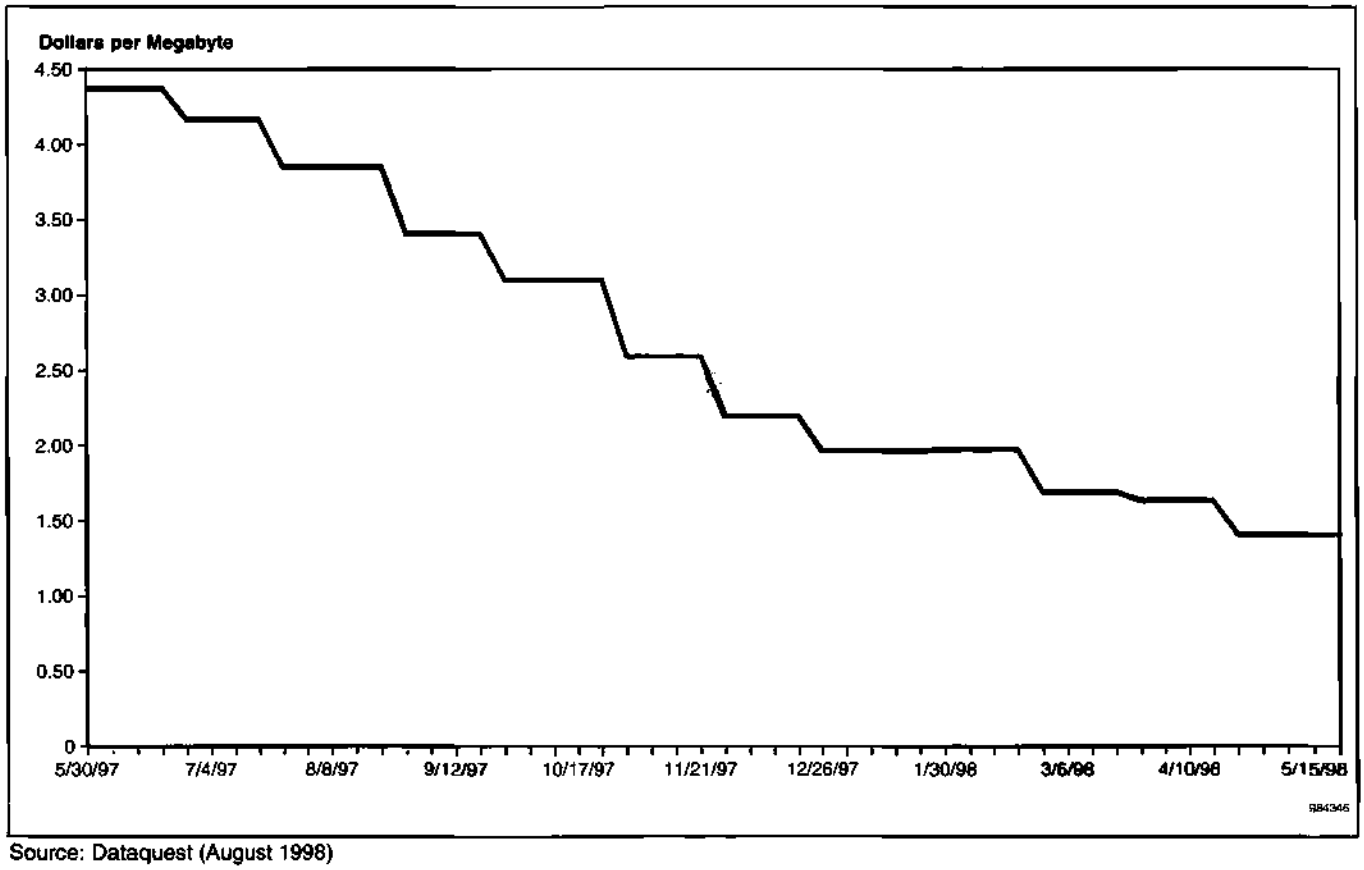
The Asian Financial Crisis and Global Slowdown

The Asian financial crisis, blamed for every semiconductor company's revenue shortfall for the past year, actually has impacted the embedded DRAM market. In 1998 alone, there has been zero to little growth in the overall semiconductor market. This comes as a result of flat electronic system sales where the embedded DRAM chips would be used. While the exact duration and spread of the financial situation is unclear, what is certain is that the effects are substantial. Based upon this slowdown, we see a clear negative impact upon the forecast for embedded DRAM semiconductors.

DRAM Prices—No Bottom Yet

Although it seems hard to believe, the prices for standalone DRAM have continued to collapse. From what seemed to be rock-bottom prices in mid-1997, we have seen a further decline of over two-thirds to an average price of $1.41/MB (as of May 1998). Figure 1 details the drop in DRAM prices over the past 12 months.

Figure 1
DRAM Prices, June 1998



Source: Dataquest (August 1998)

As we mentioned in the Dataquest Perspective titled "System-Level Integration ASICs Add Embedded DRAM" (ASIC-WW-DP-9705), dated June 2, 1997, a continued rapid price decline beyond the long-term industry average of 30 percent would delay the ramp-up of embedded DRAM ASICs and ASSPs. Some leading embedded DRAM applications, such as disk drives for home PCs and consumer desktop digital video, will move to embedded DRAM solutions strictly when the cost becomes superior to a standalone component solution. At present, there is little compelling cost reason to migrate many of these designs to embedded DRAM (barring specific DRAM granularity issues, for example, mobile graphics controllers requiring 1.1MB would still have to purchase 4MB standalone chips), and as such, Dataquest's forecast is dropping from the 1997 numbers. Of course, for applications that use embedded DRAM for its lower power and higher performance, the forecast is changing little if at all.

It should be noted that, particularly when one looks at the large investment in semiconductor manufacturing equipment during 1997, there is little reason to expect DRAM prices to recover before the end of 2000 at the earliest.

The Embedded DRAM Forecast

All factors point to a decline from the previous forecast. There is ample supply from manufacturers, many of whom are desperate to fill their underutilized DRAM fabs. On the demand side, global economic trends and low DRAM prices are reducing the need for embedded DRAM solutions.

A detailed forecast is under way. Some insight is gained, however, from Table 1, which shows the previous and current forecast for embedded DRAM semiconductors used in the storage market. There is an almost exact one-year shift in embedded DRAM consumption in this market. Direct feedback from disk drive manufacturers supports this pushout and confirms that little design-in of embedded DRAM ASICs or ASSPs is happening at present; given the typical design cycle, this means little production prior to 2000 at the earliest.

Table 1
Embedded DRAM Consumption in the Storage Market (Millions of Dollars)

	1997	1998	1999	2000	2001	2002
Current Forecast	11	68	125	546	1,050	1,746
Previous Forecast	5	90	350	1,050	1,700	-
Change	6	-22	-235	-504	-650	-

Source: Dataquest (August 1998)

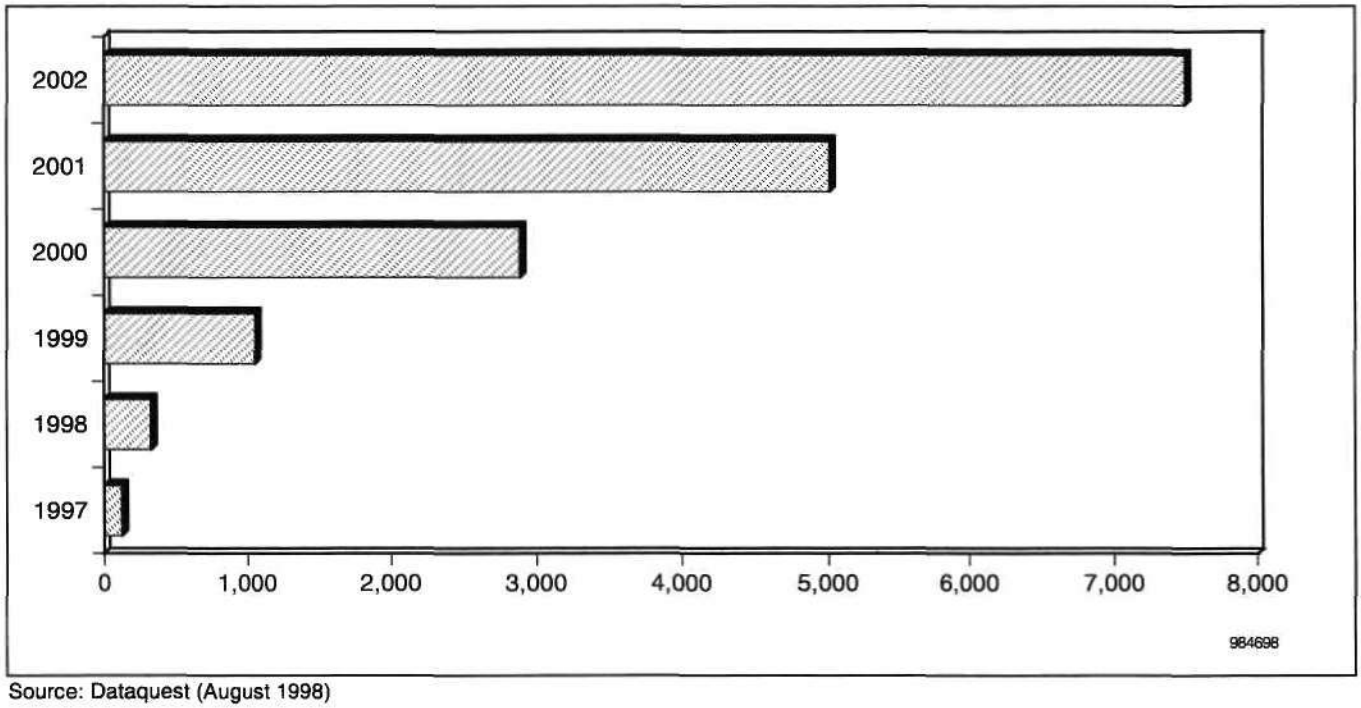
Given these trends, Dataquest's present estimate is for the embedded DRAM market to still show significant growth, yet much less than our previous forecast. Figure 2 shows our preliminary forecast for embedded DRAM ASICs and ASSPs.

Dataquest Perspective

Our message a year ago was that embedded DRAM represented the next major step toward true system-level integration. There can be no question that despite the market forces at work, embedded DRAM remains a key feature that will become part of the mainstream; the change we see in the market is more one of "when" rather than "if" in the relatively near future.

The competitive field is maturing. There are now at least half a dozen suppliers with product available and several other heavyweight vendors on the sidelines that could enter with little notice and are waiting for the market to ramp. What this means is that while crucial to compete for system-level designs, having embedded DRAM technology is no longer a product differentiator for the most part. There are vendors with embedded DRAM technology that allows for product differentiation (higher speed logic, lower power memory, and so on) but for the most part, embedded DRAM will be a commodity by 2000.

Figure 2
Preliminary Embedded DRAM Forecast (Millions of U.S. Dollars)



Source: Dataquest (August 1998)

Does embedded DRAM still represent an attractive market? Can a vendor opt to ignore these opportunities with impunity? Certainly the growth rate looks strong, particularly in comparison with the rest of the semiconductor market. In addition, the system-level designs in which embedded DRAM will by typically found tend to represent a relatively high-margin segment of semiconductors. However, the embedded DRAM tends to be a checklist requirement rather than a significant value-adding attribute. The majority of added value will come from noncommodity intellectual property, and embedded DRAM is rapidly falling off that list. A company without this capability in a few years will find itself shut out of a number of lucrative designs, but conversely, a company focusing on embedded DRAM as its primary core competency will find itself in a crowded field indeed.

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Perspective

ASIC/SLI Worldwide

Technology Analysis

Design Reuse: The OEM Dimension

Abstract: *Reusable modules are the key to system-level integration (SLI), and OEMs currently own two-thirds of all modules in use. This Perspective examines the cost of reuse, the make-buy decision, and the trends in OEM-designed blocks versus other sources. Surprisingly, it forecasts a decline in the number of OEM reuse instances.*
By Jim Tully

Introduction

Previous Dataquest studies of the future growth of the semiconductor industry have identified the "design gap" as a major impediment to growth. This showed that the capacity of the industry to design system-level semiconductor devices lags the capability to manufacture such devices. The only way to close this gap is through the use of predesigned and preverified blocks, hence the tremendous interest in the sale and use of these blocks and in the concept of design reuse. Currently, most functional blocks are created by hand and are rarely used again, with the exception of cell libraries from a single vendor. Clearly, there is scope for much productivity improvement through greater levels of reuse.

Most of the discussion of design reuse in the press and at design conferences has been focused on the vendor community. Yet, Dataquest research has shown that two-thirds of system-level blocks are currently designed and owed, not by vendors, but by OEMs. Will this continue? What are the costs? How will the cost benefits trade-offs develop in the future?

According to vendor advertisements and discussion in the press, reusable blocks are commonplace and readily available. Reuse today lacks several key elements. The blocks themselves are not enough. Tools, an appropriate methodology and standard for interoperability are also required. Design

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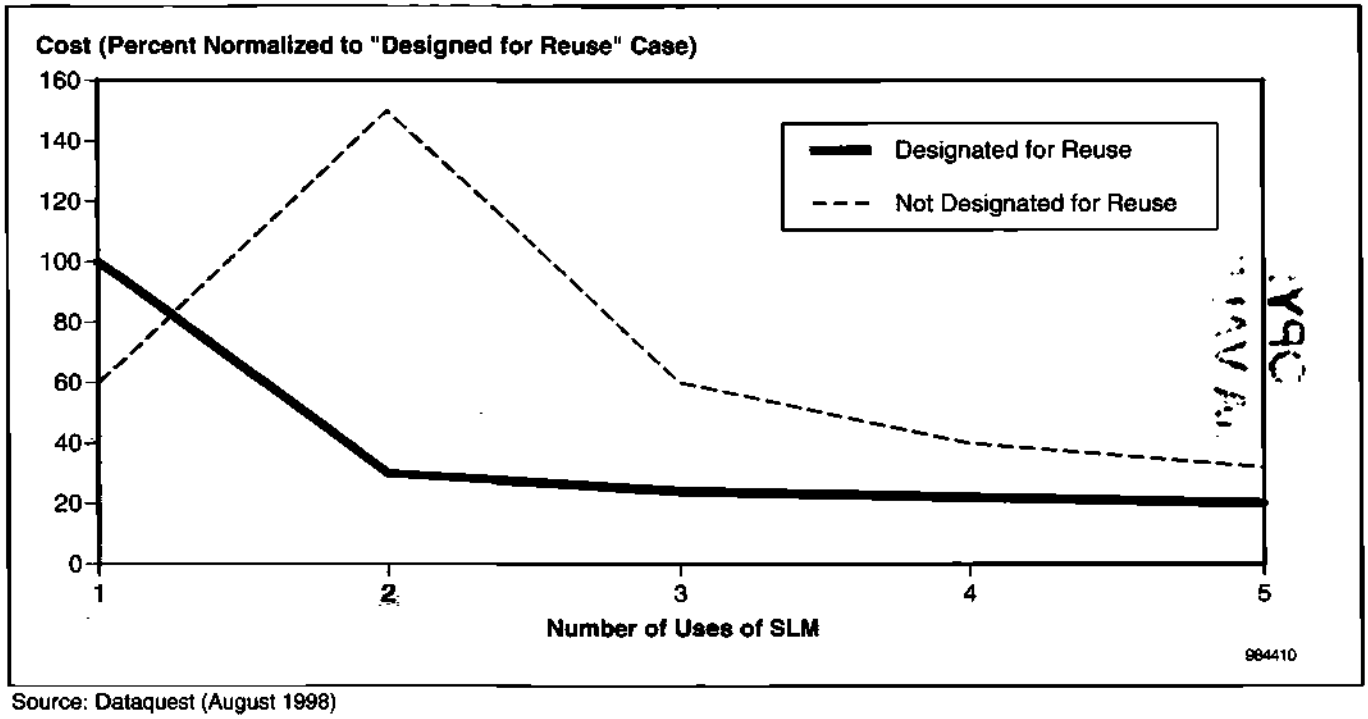
source formats are not sufficiently standard, and the infrastructure for reimplementation, resynthesis, and system verification infrastructure area is underdeveloped. As a result, reuse is only undertaken as a last resort.

Design for Reuse

It is clear from our user research that designing for reuse costs more—at least initially. However, the benefits are soon realized with subsequent uses of the module, as shown in Figure 1. Designing for reuse costs an average of 50 percent more for the first use of the module. The additional costs involved in the first use of the system-level macro (SLM) (in the design for reuse case) are because of the additional documentation and the greater generalization of the macro if it is known in advance that the module is to be reused. If these additional requirements have to be back-fitted to the SLM, the cost is significantly greater. Therefore, if a module has not been designed for reuse, a second use costs an average of five times more. Each subsequent reuse of the "not-designed-for-reuse" case produces a more general solution at each stage. A totally general-purpose SLM is never actually achieved, hence the costs never fall to zero.

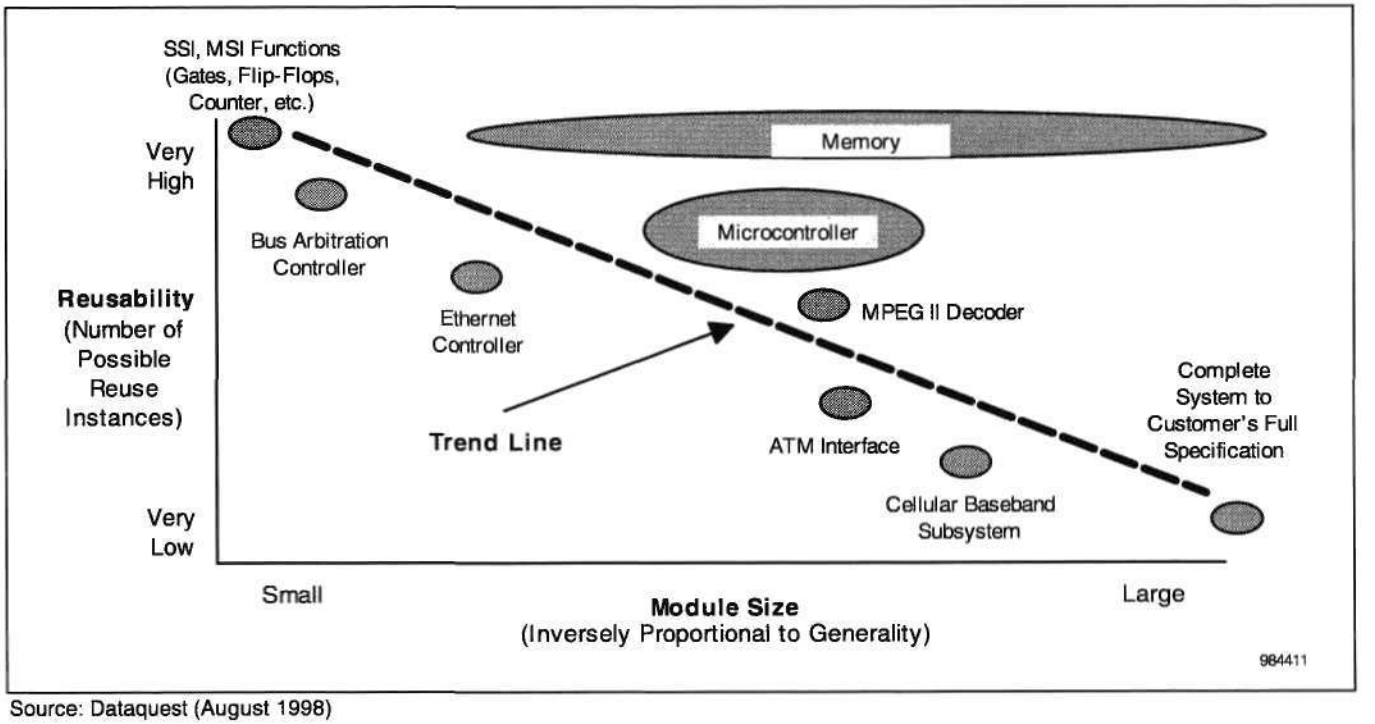
The level at which circuit elements are built is a critical factor in design reuse (see Figure 2). Often, a large block will be highly specific to a particular product and application. However, the subblocks that constitute the original block may be good candidates for reuse. The architecture of the product must be designed accordingly in order to ensure that large special-purpose blocks can be decomposed into smaller general-purpose blocks. This factor is highly relevant if the OEM intends to supply modules on the open market.

Figure 1
Cost of Design Reuse



Source: Dataquest (August 1998)

Figure 2
Relationship between Module Size and Reusability



Source: Dataquest (August 1998)

OEM Reuse Trends

The number of opportunities for OEMs to reuse modules is limited because of the relatively small number of ASICs designed by each OEM. Also, while the rate of change of technology is faster than the rate of designing new devices, the full reuse of high-level functions (from specification to layout) will not be attractive. After an OEM has developed a module, there is a good chance that technology will have changed before an opportunity exists to reuse the module. In these cases, design for reuse is not a viable strategy. Only those OEMs engaged in a large number of ASIC design starts will be able to take advantage of reuse, notably those vendors in short product life cycle sectors such as consumer electronics and mobile telephone handsets. For an ASIC vendor, the situation is completely different, as opportunities will exist to use modules in several customer projects. This implies the following:

- Reuse will increasingly fall into the ASIC vendor's domain (and the domain of design houses focusing on specific applications).
- The productivity gap between OEMs and ASIC vendors will widen. OEMs will, therefore, increasingly focus on core technology only, leaving ASIC vendors and design houses to design other aspects of the system.

The pattern of system blocks developed will change dramatically over the next 10 years as shown in Figure 3. Today, most system blocks are designed and owned by OEMs, but it will become increasingly attractive to source these blocks externally for the reasons outlined earlier. We believe that the percentage of blocks designed by OEMs will fall from about two-thirds of the

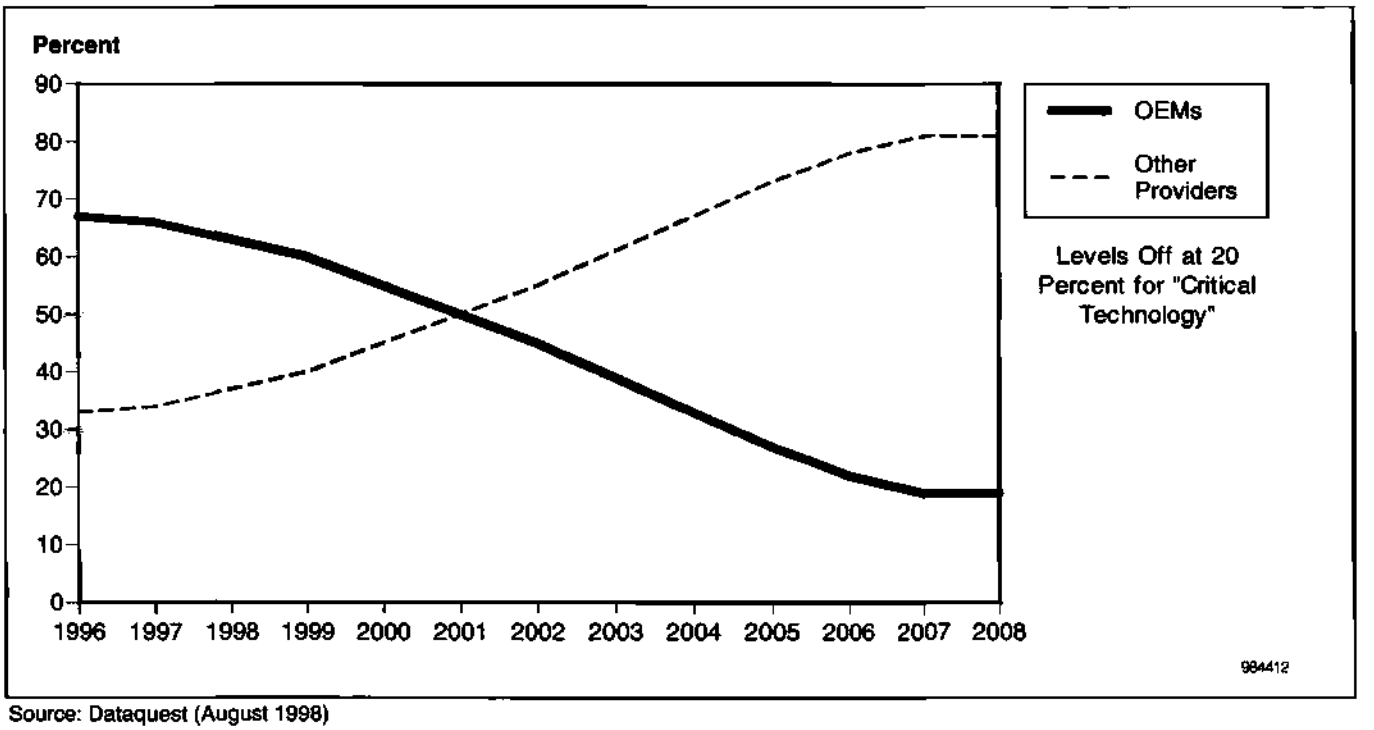
total today to about 20 percent. This 20 percent will be the core technology that the OEM decides it must design in-house for reasons of core competence and competitive advantage.

We believe that forward-thinking OEMs will follow this logical trend; others will not. OEMs that do not move in this direction will not be competitive, will lose market share, and will lengthen the time to market of new products. In other words, they will be placed in a serious position.

The current trend in OEMs is for greater reuse of modules. For the reasons outlined earlier, the number of reuse instances is likely to rise to a little over two (see Figure 4) and then fall back as OEMs focus more on core technology. As it becomes more cost-effective to source common modules from external sources, the requirements to reuse internally developed modules will fall. However, the demand for reuse technology will continue to grow rapidly in the OEM community to facilitate the use of externally sourced modules.

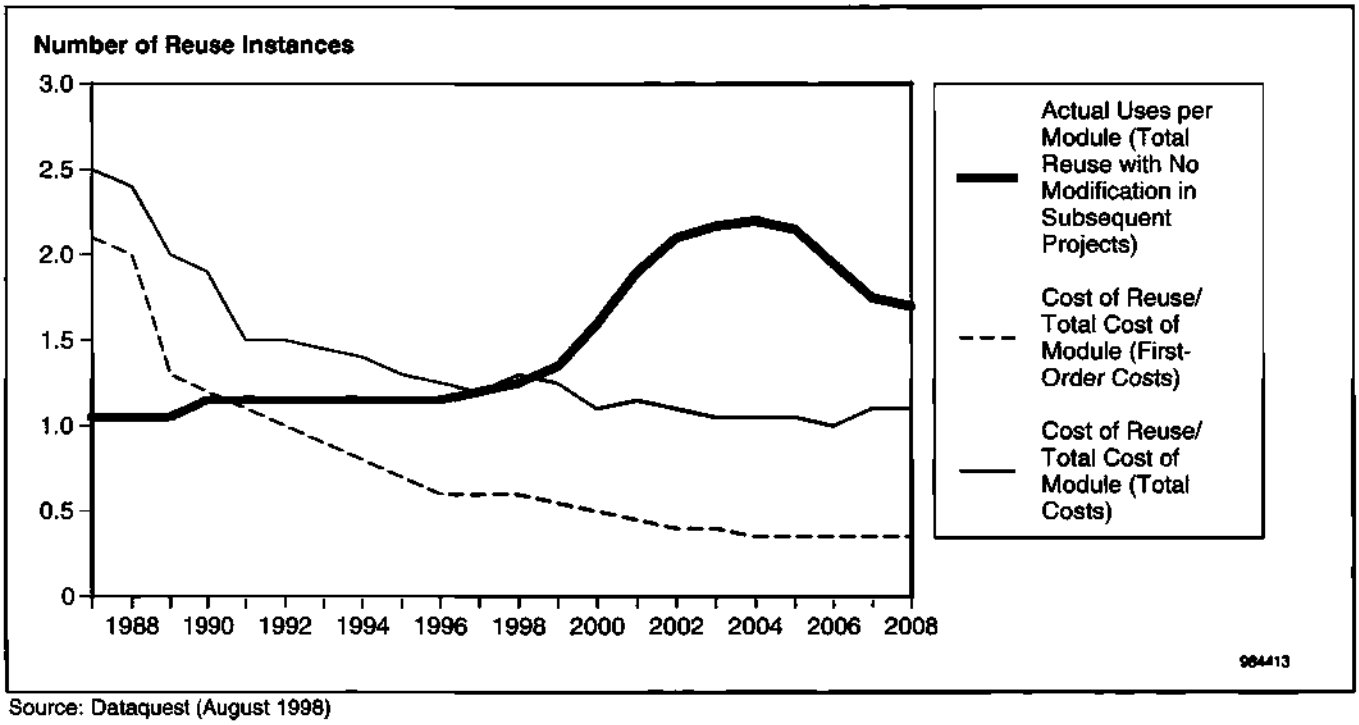
Over this 10-year forecast period, it will become easier to reuse modules as reuse technology matures and the methodology becomes better understood. As a result, the overhead cost of designing for reuse will fall steadily. However, in these OEM situations, many modules designed for reuse are never actually reused. Situations change, standards change, and technology changes faster than anticipated. The effort involved in the reuse element of the design is therefore wasted. The total cost of reuse is higher than the apparent (first order) costs. Furthermore, we believe the gap between these two cost elements will widen, as an increasing number of reusable blocks are never used.

Figure 3
System Blocks Developed: OEMs versus Other Providers



Source: Dataquest (August 1998)

Figure 4
Costs and Number of Reuse Instances (OEMs)



Source: Dataquest (August 1998)

At the same time, much intellectual property owned by OEMs will be commercialized and sold to a wide range of customers. However, this will be handled by ASIC vendors and other third-party IP providers—not by the OEM. This is independent of the discussion above and the number of reuse instances by the OEM will not increase appreciably in these cases.

The Make-Buy Decision

From the foregoing discussion, a key decision faced by OEMs is whether to develop a module in-house or to externally source it. In the short-term (over the next four to five years), this will not be an easy decision to make as several factors are involved. For example, some modules may be strategically important to the OEM and may be at the heart of the company's core competence. In this situation, the company will probably be in a more advanced and knowledgeable position than a module provider and will be unlikely to find a purchased module to meet the required specification.

Other issues such as internal resource availability and relative costs also have an impact on the decision. These issues are summarized in Figure 5.

Dataquest Perspective

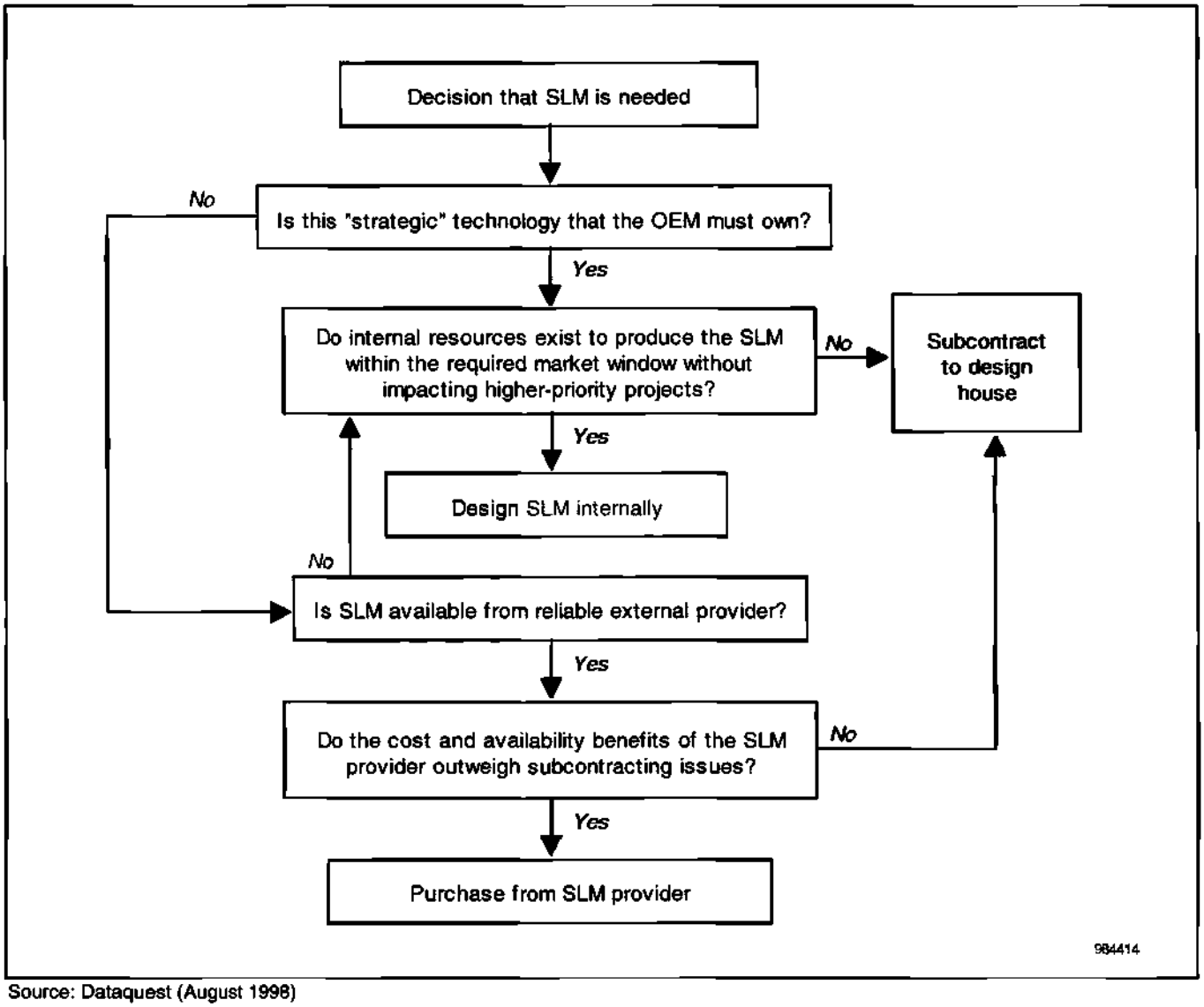
The pattern of usage and development of SLMs by OEMs has changed appreciably over the past few years and will change more dramatically in the future. Contrary to common perception, the number of modules designed for reuse by OEMs will fall in the future as these companies turn their attention to outside suppliers. The ultimate cost of these modules is determined

largely by the number of possible sales (and, therefore, the number of reuse instances). For common modules, ASIC vendors and other SLM providers will always achieve a larger number of reuse instances and will represent a lower-cost source.

But what of existing SLMs? OEMs have played a key role in the development of system-level macros for some years and currently own around two-thirds of all blocks in use today. As we move further into the system on-chip era, this offers a tremendous opportunity for OEMs to capitalize on their position of power. Big additional revenue streams await those OEMs that grasp this opportunity. But OEMs do not have the distribution channels or support infrastructure to directly sell these modules. Nor should they wish to, as this would divert them from their main task of designing and producing systems. Some OEMs will, no doubt, ultimately withdraw from the systems business and become IP providers, but this will be outside the timescale of the current forecasts.

In the shorter term, the most effective way for OEMs to channel intellectual property into the wider market is to partner with ASIC vendors or possibly independent SLM providers.

Figure 5
Internal Resource Availability and Relative Costs



Source: Dataquest (August 1998)

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Perspective

ASIC/SLI Worldwide

Technology Analysis

ASSPs for the Fourth-Generation MiniDisc: SLI as Technology Driver

Abstract: *Since the debut of the first MiniDisc (MD) audio recorder in the fall of 1992, application-specific standard products (ASSPs) have evolved side by side by using system-level integration (SLI) technology, now in the fourth generation. These MD ASSPs use leading-edge technologies, including a 0.35-micron low-voltage process, an intellectual property (IP) core, embedded DRAMs, and a thin LSI package, in order to survive in the cost-competitive digital consumer market. This Perspective analyzes the MD market, forecast its demand, and evaluates the future direction of MD systems and technology requirements for SLI chips.*

By Yoshihisa Toyosaki

The Emerging Market Driven by the Digital System Revolution

In 1996, MD audio systems, introduced in the fall of 1992, started full-fledged market expansion in its fourth year. The compact disc (CD), forerunner of the digital audio system product, underwent rapid market expansion four years after commercialization. As the MD market follows in its predecessor's footsteps, Dataquest believes that the digital audio market has spawned a new hot product and MD will form an emerging market in the coming 10-year period. Figure 1 lists emerging markets driven by leading-edge digital system technologies.

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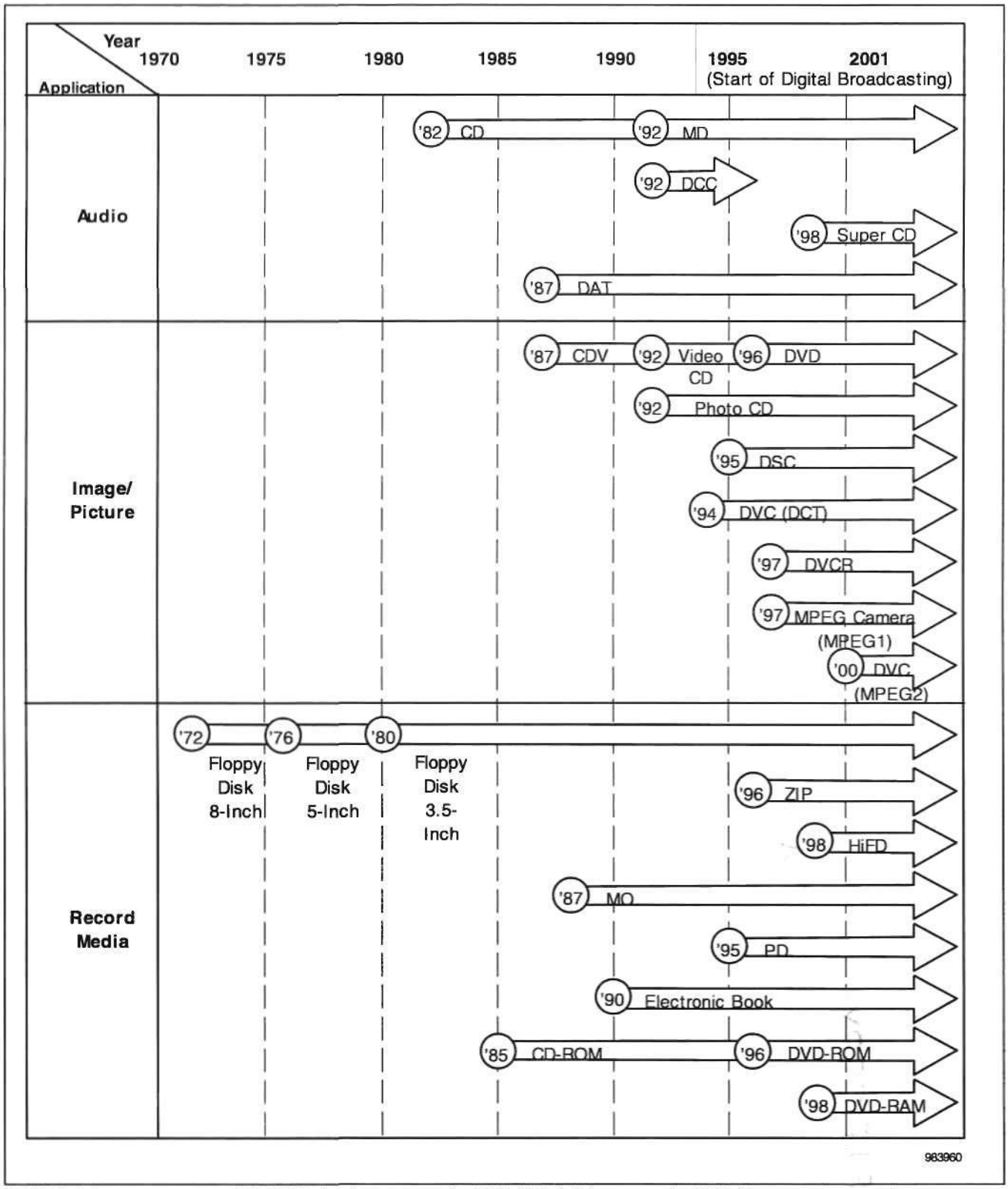
(For Cross-Technology, file in the Semiconductor Devices and User Issues binder)

Figure 1
Evolution of Emerging Markets Driven by Leading-Edge Digital System Technologies



DCC: Digital compact cassette, DAT: Digital audio tape recorder, DVC: Digital video camcorder, DCT: Discrete cosine transform
DSC: Digital still camera
Source: Dataquest (July 1998)

The Basic System for MD

The MD system consists of a 64mm diameter, recordable/replayable, magneto-optical (MO) audio disk that is housed in a cartridge. Audio data is recorded by a field modulation method onto an MO disk. It is based on CD-ROM's mode 2 capabilities that apply rewritable CD technology. Digital audio signals are processed by adaptive transform acoustic coding (ATRAC) technology, on the basis of acoustic characteristics, to be compressed by a 1:5 ratio on the disk for a maximum duration of 74 minutes. MD audio's major characteristics and specifications are summarized in Table 1 and by the following:

- Use of a 64mm diameter MO disk that is housed in a cartridge
- The ability to handle two types of MO disks (a replay-only optical disk including music and an MO disk that can be recorded by users)
- The potential for random access, as with a CD
- ATRAC audio data compression technology that allows high acoustic quality recording/replaying for 74 minutes at maximum
- Use of semiconductor memory (DRAM) for vibration resistance

Table 1
Specifications of MD Audio Systems

Feature	Specification
Recording Method	Field modulation
Master Clock	
Operating Environment	16.9334 MHz to 22.5792 MHz (varying with vendors)
Signal Format	
Sampling Frequency	44.1 KHz
Coding System	ATRAC
Modulation System	Eight to 14 modulation (EFM)
Error Correction System	Cross Interleave Reed Solomon Code (CIRC)
Audio Features	
Number of Channels	2 channels (stereo)
Frequency Bandwidth	5Hz to 20 KHz
Dynamic Range	105dB

Source: Dataquest (July 1998)

New Faces of MD Application Technology

In 1997, Sony Corporation unveiled new format standards for the next-generation MD, MD DATA2, which boasts data storage capacity of 650MB on an MO disk. Dataquest believes that Sony has already developed MD DATA2 standards. MD DATA2 also supports existing formats of recording and replaying an MD DATA disk and is compatible with existing systems (see Table 2).

One major change has taken place in the modulation system onto write data into an MD disk, from EFM to run length limited (RLL) (1,7). Dataquest sees that the change reflects Sony's intent to adopt partial response maximum likelihood (PRML) for future processing of replay signals, which will accompany the changes in specifications for multiplexing of address and clock signals.

Technically, the EFM method uses a wobbled groove, whereas the RLL method arranges two grooves with and without wobbling alternately to place wobble signals only on one side of record track. Sony claims that this technique can control cross talk of wobble signals, which becomes a problem when the track pitch is narrowed.

Table 2
Comparison of MD Format Standards

Item	Present	Future
Format Specifications	MD DATA	MD DATA 2
Disk Diameter	64mm	64mm
Disk Thickness	1.2mm	1.2mm
Medium Memory Capacity	140MB	650MB
Track Pitch	1.6μm	0.95μm
Record per Bit	0.55μm	0.34μm
Disk's Linear Speed	1.2 m/sec. to 1.4m/sec.	2 m/sec.
Modulation System	EFM	RLL (1,7)
Data Transfer Rate	150 KB/sec.	580 KB/sec.
Clock Signal Embedding Method	Wobbling	Wobbling
Address Signal Multiplexing Method	Wobble of guide groove	Double spiral of wobbled and straight grooves

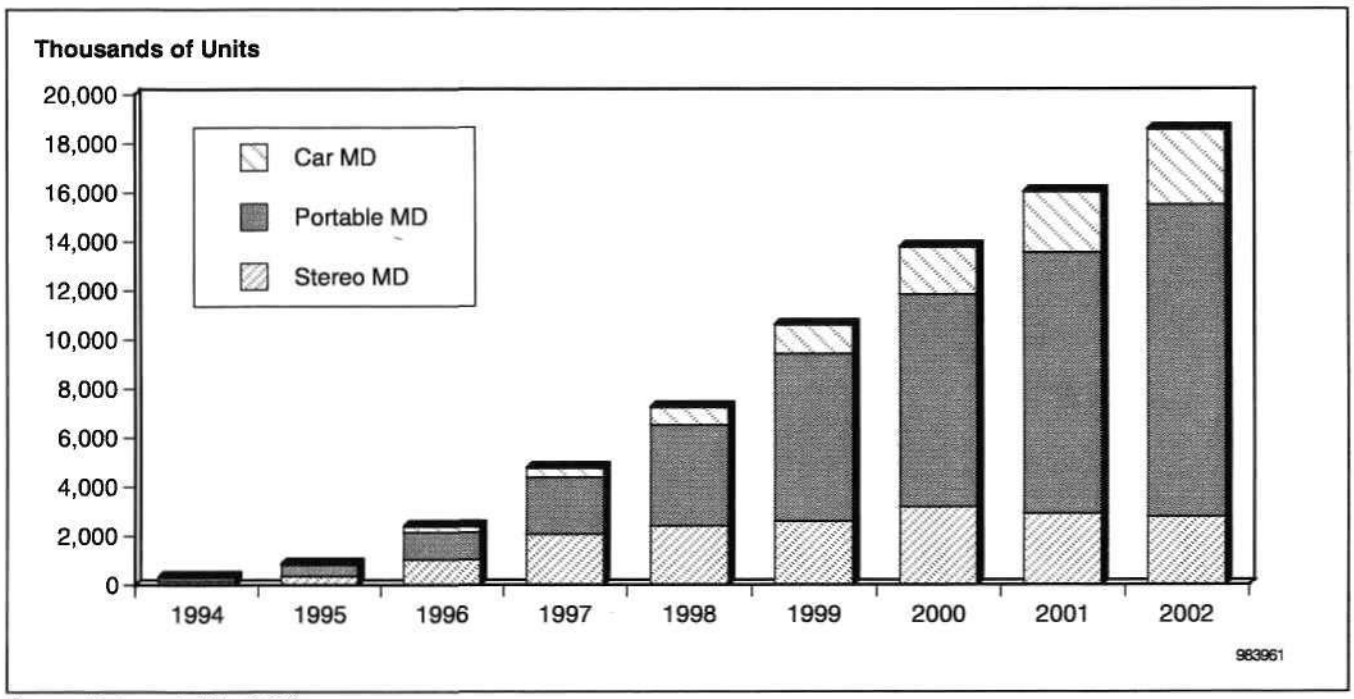
Source: Dataquest (July 1998)

Forecasting Worldwide MD Demand

As of 1998, as many as 100 types of MD audio systems have been released, including portable, fixed, and onboard. Last year, substantial growth was seen in the Japanese market where portable MD players were booming. In 1997, total unit shipment of MD audio systems to the worldwide market jumped nearly 100 percent from the previous year to reach 4.77 million units. According to Dataquest's forecast, it will continue to expand at a compound annual growth rate (CAGR) of 31.2 percent between 1997 and 2002, exceeding 10.5 million units in 1999 and reaching 18.6 million units in 2002 (see Figure 2 and Table 3).

In the meantime, portable MDs' share of unit shipments in the Japanese headphone stereo market is estimated at 25 percent, assuming that total shipments of cassette-type headphone stereo equipment were 3.5 million in 1997 and those of portable CD players 2 million. Figure 3 and Table 4 show the MD audio demand forecast by region. In 1997, the Japanese market dominated consumption, with small portions coming from Europe, Asia/Pacific, and part of South America. Nevertheless, as MD follows a similar pattern of market penetration to CD, the global trend in digitization of audio equipment will soon drive world demand for MD audio system products (see Figure 4).

Figure 2
Demand Forecast for MD Audio System Products



Source: Dataquest (July 1998)

Table 3
Demand Forecast for MD Audio System Products

	1994	1995	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Stereo MD	144	377	1,046	2,079	2,419	2,603	3,192	2,924	2,785	6.0
Portable MD	172	452	1,114	2,315	4,102	6,821	8,646	10,634	12,721	40.6
Car MD	17	45	242	378	720	1,170	1,935	2,469	3,064	52.0
Total	**333**	**874**	**2,402**	**4,772**	**7,241**	**10,594**	**13,773**	**16,027**	**18,570**	**31.2**

Source: Dataquest (July 1998)

For MD audio systems (particularly portable), a low-voltage, standard microcontroller is used in each system for system control purposes. With sophistication of MD features, instruction programs grow in size and increase the ROM capacity embedded in the microcontroller year after year.

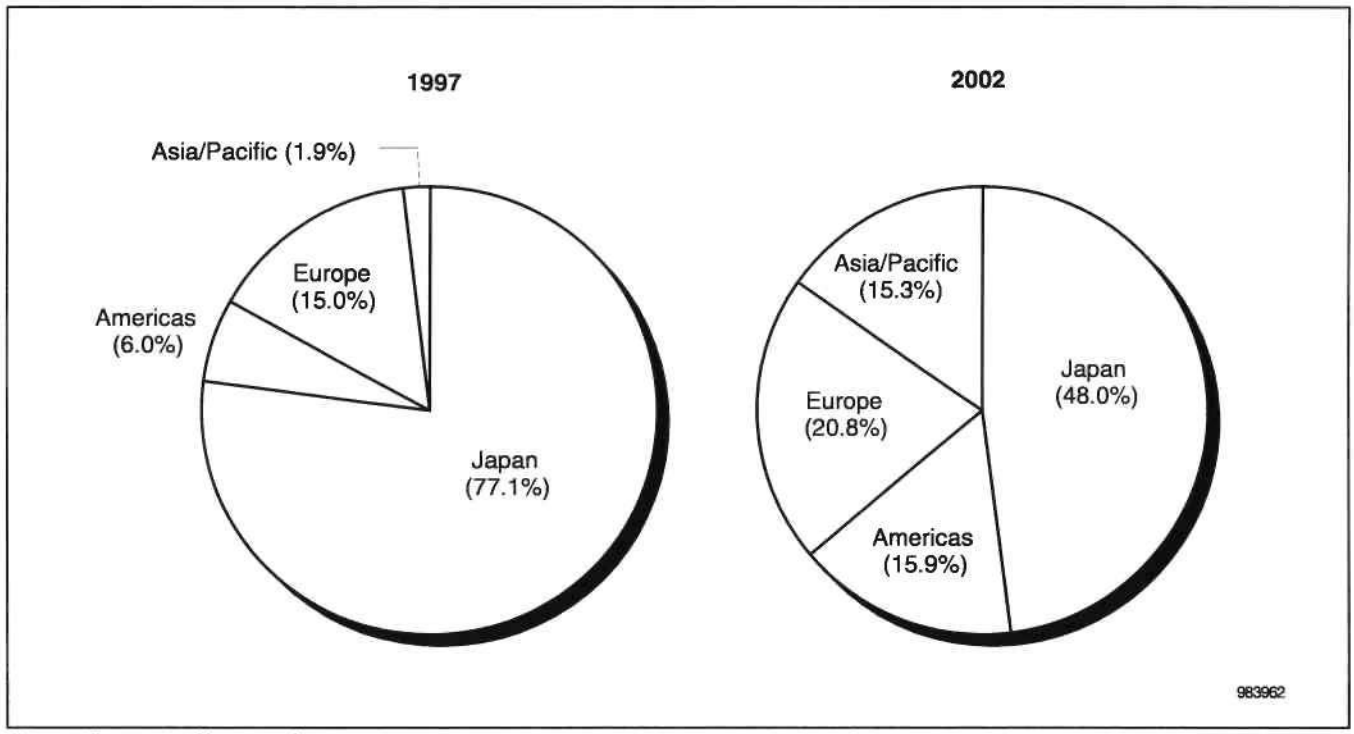
A similar trend is seen in instruction ROMs of digital signal processors (DSPs) that are used for signal processing on the ATRAC circuit contained in the chipset.

Availability of MD Chipsets

Table 5 compares MD chipsets using system-level integration (SLI) technology offered by major ASSP vendors.

Figure 5 shows block diagrams of MD audio systems, illustrating the integration of circuits into LSIs between the first- and fourth-generation MD audio systems.

Figure 3
MD Audio Demand Forecast by Region



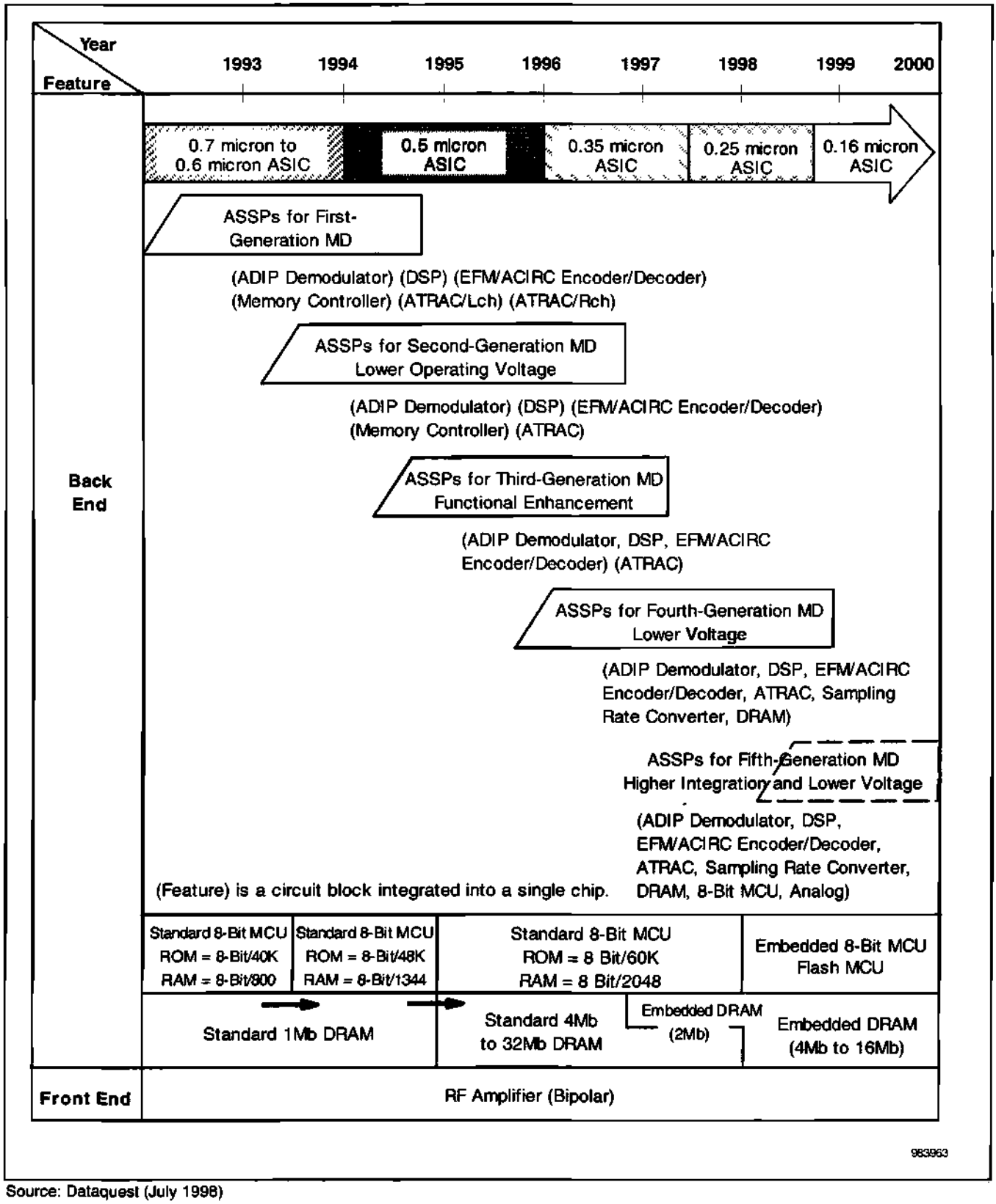
Source: Dataquest (July 1998)

Table 4
MD Audio Demand Forecast by Region

	1994	1995	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Japan	244	752	1,958	3,681	5,079	7,235	8,119	8,538	8,922	19.4
Americas	10	21	121	286	560	922	1,391	2,072	2,960	59.6
Europe	72	98	288	718	1,380	1,999	2,629	3,245	3,865	40.0
Asia/Pacific	7	3	35	87	222	438	1,634	2,172	2,823	100.6
Worldwide	333	874	2,402	4,772	7,241	10,594	13,773	16,027	18,570	31.2

Source: Dataquest (July 1998)

Figure 4
Technology Road Map for MD ASSPs



Source: Dataquest (July 1998)

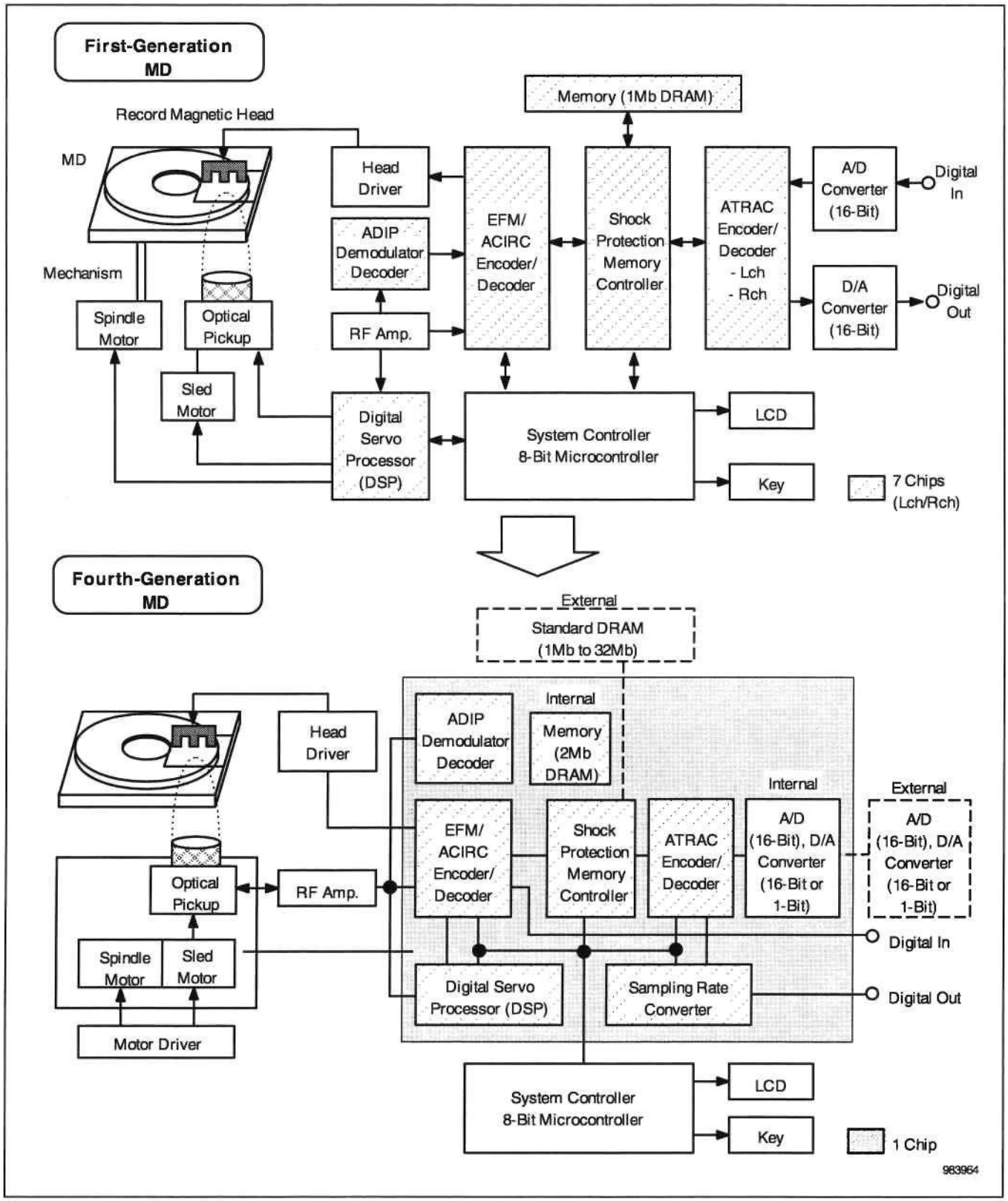
Table 5
Comparison of MD Chipsets by Function

Front End			
Vendor	Sony	Sharp	SANYO
Product Name	CXA2523AR	IR3R48	LA9605W
Process	Bipolar	Bipolar	2.5 µm bipolar
Commercial Process	In-house production	In-house production	In-house production
Package	48LQFP	100LQFP	48LQFP
Volume Production	Now	Now	Now

Back End					
Vendor	**Sony**		**Sharp**		**SANYO**
Product Name	MDL40 series CXD2650R	CXD2655R[1] CXD2652AR[2]	LR3765	LR3766	LC89640
Number of Chipsets	1	1	2		1
Signal Processing Features	Incorporation of all circuits except for RF amp. and 8-bit micro-controller into a single chip	Incorporation of all circuits except for DRAM, RF amp., and 8-bit microcontroller into a single chip	Major features —2 DSPs (16-bit/ 24-bit ATRAC)	Major features —EFM and ACIRC	Incorporation of all circuits except for DRAM, RF amp., and 8-bit microcontroller into a single chip
ASSP Generation	Fourth generation		Third generation		Fourth generation
CMOS Process[3] µm	0.4		0.5		0.35
Commercial Process	In-house production		In-house production		In-house production
Chip Architecture	Embedded array		Embedded array		Cell-based IC
Embedded DRAM	Yes (2Mb)	No	No		No
Source Voltage	Single power supply Core: 3.0V ± 10 percent		Single power supply Core: 3.5V ± 10 percent I/O: 3.5V, 5V		Double power supply Core: 2.0V ± 10 percent I/O: 3.0V ± 10 percent Single power supply 3.0V ± 10 percent
Power Consumption (mW)	150	100 to 80	180	35	40
Package	100LQFP		96LQFP	100LQFP	100LQFP
Volume Production	Now		Now		Now

[1] D/A embedded
[2] Sampling converter embedded
[3] Drawn gate length
Source: Dataquest (July 1998)

Figure 5
Conceptual Block Diagrams of MD Audio Systems

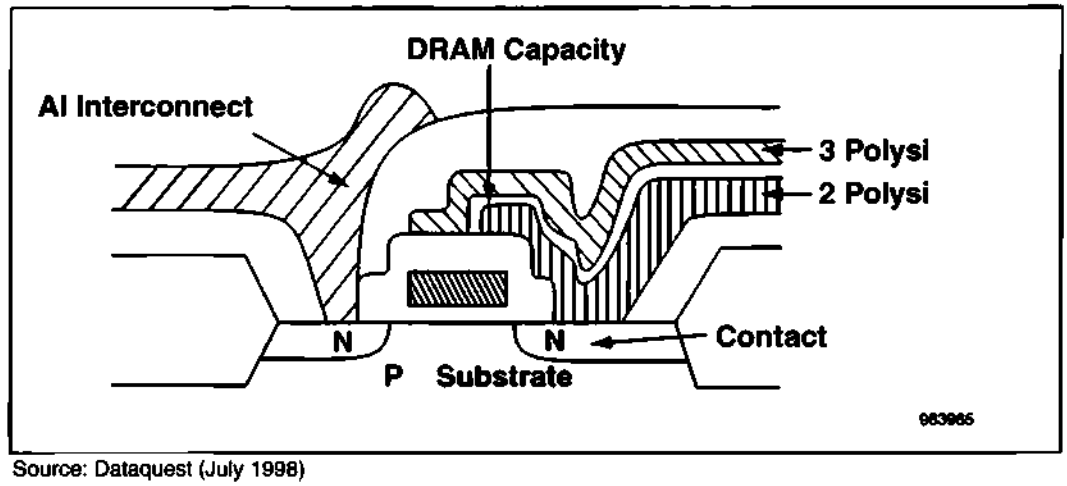


Source: Dataquest (July 1998)

Embedded DRAM Technologies Implemented in MD ASSPs

Sony has adopted leading-edge SLI technology for its fourth-generation MD ASSP, MDL40, by quasi-merging 2Mb DRAM in a back-end signal processing LSI (see Figure 6). The technology is based on a 0.4-micron logic process and delivers high-speed and low-power consumption requirements for portable MD audio products.

Figure 6
Sectional View of Embedded DRAM with Vertical Structure, Stacked Capacitor



Source: Dataquest (July 1998)

Sony and Fujitsu Ltd. are under alliance in the area of manufacturing technology for the 0.18-micron process (including development of a 0.13-micron process). Dataquest believes that this alliance reflects Sony's need for Fujitsu's high-integration DRAM memory cell and logic/DRAM quasi-merging technologies, which are essential technologies for Sony's future portable application strategy.

Why DRAMs in MD Systems?

MD systems incorporate DRAM memory between an optical pickup and an ATRAC voice compression decoder as data buffer. For instance, if a 1Mb DRAM is used, it takes 0.9 seconds to fill it with compressed data from an MO disk. If the system becomes unable to read out data because of vibration, data can be sent from the DRAM to the decoder for around three seconds (1Mb/0.3Ms bit per sec). Thus, the DRAM serves as a safeguard against interruption of replay. Major advantages of embedded DRAMs in MD audio systems are as follows:

- Reduction of total power consumption
- Prolonged system operation
- Optimization of system design (memory capacity, bit width, source voltage)
- Reduction of printed circuit board area and chip counts through system miniaturization

- Reduction of package pin counts
- Attenuation of electromagnetic interference (EMI) noise
- Availability of small capacity DRAM memory devices

As a result, Sony's MDL40 (having a 2Mb DRAM) does not experience sound interruption so far as the optical pickup returns to its original position above the disk within six seconds.

Logically, the use of a large capacity, standard DRAM in an MD system allows a larger margin of time against the sound skip. The MDL40 has an interface with an external DRAM to allow deployment to diverse MD products, thus delivering LSI design-enabling versatility and system scalability. Dataquest believes that the product can flexibly adapt to a quick price change in DRAM, as seen now, and permits less LSI development costs, leading to total cost reduction and abatement of risks (see Table 6).

Table 6
Specifications of Sony's Embedded DRAM Process

Product Name	ASC5	ASC6
Production Time	Now	Q3/98
Drawn Gate Length (μm)	0.4	0.25
Chip Architecture	Embedded array	Embedded array
Logic Gate Density (gate/mm^2)	7,000	18,000
Gate Oxide (Å)	100	-
Metal Layer	3	3 to 5
Salicide	No	Yes
Core Voltage (V)	3.3, 2.2	2.5<1.5
Embedded DRAM	Yes	Yes
Ownership of DRAM Technology	Sony	Alliance with Oki
DRAM Architecture	Stacked capacitor (vertical structure cell)	Stacked capacitor
DRAM Cell Area (μm)	3.5	0.72
Maximum DRAM Capacity (Mb)	4	32
Bandwidth (Memory Capacity)	1.3GB/sec. (2Mb)	Maximum 6.4GB/sec. (16Mb)
Bus Width	256 (2Mb)	512 (16Mb)
Maximum Bus Transfer Frequency (MHz)	40	100

Source: Dataquest (July 1998)

Power Consumption by MD LSI, by Generation

Power consumption required per chip in the MD system has been lowered in each generation as follows:

- First generation: 1500 mW/7 chips
- Second generation: 500 mW/6 chips

- Third generation: 250 mW/3 chips
- Fourth generation: 150 mW to 40 mW/1 chip (quasi-merged)
- Fifth generation: Under 100 mW to 60 mW/1 chip (quasi-merged)

Note that the basis of estimation has been obtained by averaging parameters representing DC characteristics of MD LSIs, except for the front-end bipolar RF amplifier.

MD Design Requirements

Table 7 summarizes the typical design requirements for MD audio.

Table 7
Typical System Design Requirements for MD Audio

Item	Fourth Generation	Fifth Generation
Development and Production Time	1996 to 1998	1998 to 1999
Digital Block/Back End (Chip)	1	1
Usable Logic Gates	200,000	200,000 to 250,000
Target Die Size (mm/size)	8.5 to 10 [1]	6 to 10 [1]
Process Technology (μm^2)	0.4 to 0.35	0.25 to 0.18
Chip Architecture	Cell-based IC	Cell-based IC
Metal Layers	Three	Three to four
Core Voltage (V)	3.0 to 2.0	2.5 to <1.5 (0.9)
I/O Voltage (V)	3.0, 2.0	3.0, 2.5, 2.0, 1.8, <1.5 (0.9)
Embedded Memory	SRAM/ROM/DRAM	SRAM/DRAM/Flash
Phase-Locked Loop (PLL)	Digital	Digital
IP Core	Yes	Yes
Special circuit features	PML[3]	PML[3]
Mixed Signal	Yes (No, D/A)	Yes (A/D, D/A)
Package Technology	LQFP	LQFP/CSP
Pin Count	100 pins	100 pins
Pin Pitch (mm)	0.5	0.5/0.8 to 0.5
Interposer Technology	Au wire bonding	Au wire bonding/SBB[4]
Test	Full scan/BIST	Full and partial scan/BIST/IDDQ
JTAG I/O	No	Yes
EDA	Verilog/SSB[5]	VHDL/Verilog/Synopsys, plus power estimation, synthesis, and analysis

[1] Chip size varies with embedded DRAM capacity on a single chip.
[2] Drawn Gate Length
[3] Power management logic
[4] Stud bump bonding technology
[5] Sony System Bench
Source: Dataquest (July 1998)

Competitive Analysis

Major semiconductor players in the MD market are as follows:

- Sony
- Sharp
- SANYO
- Nippon Motorola Ltd.
- Asahi Kasei Microsystems Co. Ltd. (AKM)

Semiconductor vendors supplying for MD audio system products are Sony (mainly captive consumption), Sharp, and SANYO, which have developed MD chipsets based on SLI application-specific interface (ASI) technology. Eight-bit controllers (16-bit for fixed-type MD) are supplied by Sony, Sharp, SANYO, Fujitsu, Mitsubishi Electric Corporation, and Texas Instruments Japan. Other vendors include Nippon Motorola (MD motor control ICs using SMART MOS technology) and AKM and Sony (standard analog products). Semiconductor vendors active in the MD market are limited to those having R&D bases in Japan.

Dataquest Perspective

Dataquest believes that 1998 will be the year of new innovations, sparked by advancements in SLI and digital signal processing technologies, that bring the highly sophisticated multimedia society closer to reality. One application is promised to be MD players, for which signs of market ramp-up, as the next-generation digital portable audio system to supplant CD players, have been since 1996. In particular, Sony has commercialized a new MD audio system that can be linked to PCs, a development that is expected to spur potential demand among PC users for convergence of the computer and the MD audio medium.

Chipsets for MD players have already evolved to the fourth generation, where 0.35-micron cell-based IC technology is used for volume production of highly integrated, low-voltage, and low-cost devices. While the first- and second-generation MD players have focused on integration of recording capabilities into fewer chips, Dataquest analyzes that the third-generation and later MD systems, which have become the mainstay of the market, are increasingly vying for miniaturization and prolonged battery life.

In particular, the fourth-generation MD chipsets are based on mixed configuration of digital and analog signal processing LSIs. Essentially, a DRAM (including an embedded type) that stores data readout from an MD disk and an 8-bit microcontroller used for system control implement today's MD player. The digital signal processing LSI is developed by using an SLI technique, and Sony and Sharp use DSP technology in the signal component. SANYO configures the circuit by hardwired logic in place of DSP technology, largely because hardwired logic demand minimizes used gate accounts in a coding algorithm by which the system's standard processing is established, thereby reducing chip size. Furthermore, SANYO has lowered internal

operating frequency to 4.23 MHz, thereby cutting power consumption during LSI operation. Dataquest believes that hardwired logic design, coupled with the ability to optimize internal memory and configure a control circuit with minimum overhead in instruction processing,has a cost advantage over DSP.

As the embedded processor has enabled explosive growth of ASIC and ASSP performance, the embedded DRAM has made a significant step toward system-level integration. Today's priority in commercializing device technology for portable consumer equipment is cost, followed by miniaturization and performance. Although technologies to implement the embedded DRAM have a relatively short history with many technological hurdles remaining to be cleared, the market undoubtedly has high potential for exponential growth. Consequently, the embedded DRAM will play a key role as the intellectual property (IP) core, essential within the next few years for ASIC and ASSP vendors who are targeting the digital consumer market.

At the same time, however, Dataquest is concerned about the current sluggishness of the DRAM market, which may delay market acceptance of embedded DRAMs for system optimization in terms of low-power consumption, resulting in a slow start-up of the digital consumer market. In 1997, standard DRAM prices plummeted to offer cost advantage over quasi-merging of embedded DRAMs. In fact, Sony has responded to the market trend by supplying new MD chipsets without embedded DRAM (internal DRAM).

Nevertheless, in the digital consumer market, where competition is usually based on system price, flexibility to meet system requirements becomes critical. Dataquest believes that the technologies required for the portable market in such a competitive environment are leading-edge SLI technologies such as EDA tools that implement low-power consumption designs, low voltage processes and libraries, IP cores, embedded DRAMs, and high-density mounting commerce service providers (CSP) technology. As 0.25-to-0.18-micron processes come to stream, incorporation of 4Mb DRAM into a single chip will be an economically justifiable option.

From a business perspective, in the digital consumer market such as MD audio, often semiconductor vendors develop LSIs for system companies in their own groups, as seen with Sony, Sharp, and SANYO. These vendors carry out design and development by sharing resources with captive customers. For outside vendors to obtain design wins in the digital consumer market, therefore, they must be abreast of the requirements of application users and market trends, as well as able to provide technology and resources in a timely manner. More precisely, outside vendors must clearly focus on a specific market segment that constitutes the core of their strategy and develop the readiness, including a flexible organization, to propose to application users a total solution at a system level. These requirements are translated into the need for a strong partnership with a system vendor, which must be quickly established if merchandise semiconductor vendors are to succeed in the emerging markets.

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Perspective

ASIC/SLI Worldwide

Market Analysis

Vertically Integrated Suppliers Dominate 1997 ASIC Market

Abstract: *Vertically integrated companies such as IBM and Lucent Technologies gained significant ASIC market share during 1997 from focused ASIC companies such as LSI Logic. Internally developed system knowledge as well as advanced manufacturing were the key weapons used to gain new customers in the merchant market. In this Perspective, Dataquest examines the leading ASIC and PLD suppliers and focuses on their merchant presence.*
By Bryan Lewis

Record Changes Hit 1997 ASIC Ranking

The balance of power is shifting at a record rate. Four of the top five ASIC suppliers changed their ranking status in 1997, and we have a new No. 1 programmable logic device (PLD) supplier. IBM rocketed up the ASIC rankings in 1997 to become the No. 2 ASIC supplier, gaining three positions over 1996. Meanwhile, LSI Logic Corporation had a tough year and fell to the No. 5 position, losing three slots. Lucent Technologies and Fujitsu Ltd. swapped for the No. 3 position in ASICs, while Altera Corporation passed Xilinx Incorporated to become the No. 1 PLD supplier.

IBM and Lucent Technologies stand out as having the most lucrative gains in 1997, each increasing its revenue by over $400 million with over 40 percent growth. NEC Corporation was the only top-five supplier to retain the same ranking status as in 1996, holding down the No. 1 position; however, its lead diminished from 1996 levels because it only grew by 10 percent. Most ASIC suppliers experienced a subpar year in 1997, with single- or low double-digit growth.

Why did IBM and Lucent do so well when others struggled?

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First, both IBM and Lucent are vertically integrated suppliers and have vast system knowledge gained from years (or should we say decades) of experience of selling to their system divisions. Second, by selling to their internal divisions as well as the merchant market, they have achieved great economies of scale in manufacturing. Third, the R&D budgets of vertically integrated suppliers are large and can support internal design tool groups and advanced processes including copper interconnect. You may wonder why other vertically integrated companies, such as NEC and Fujitsu, didn't perform better, considering that they share the same advantages. That brings us the fourth point: Both IBM and Lucent are willing to offer the same advanced technology they offer to internal divisions to the merchant market with almost no time lag. Offering the most advanced technology with nearly no time lag is a key ingredient to their success in the merchant market.

ASIC Rankings

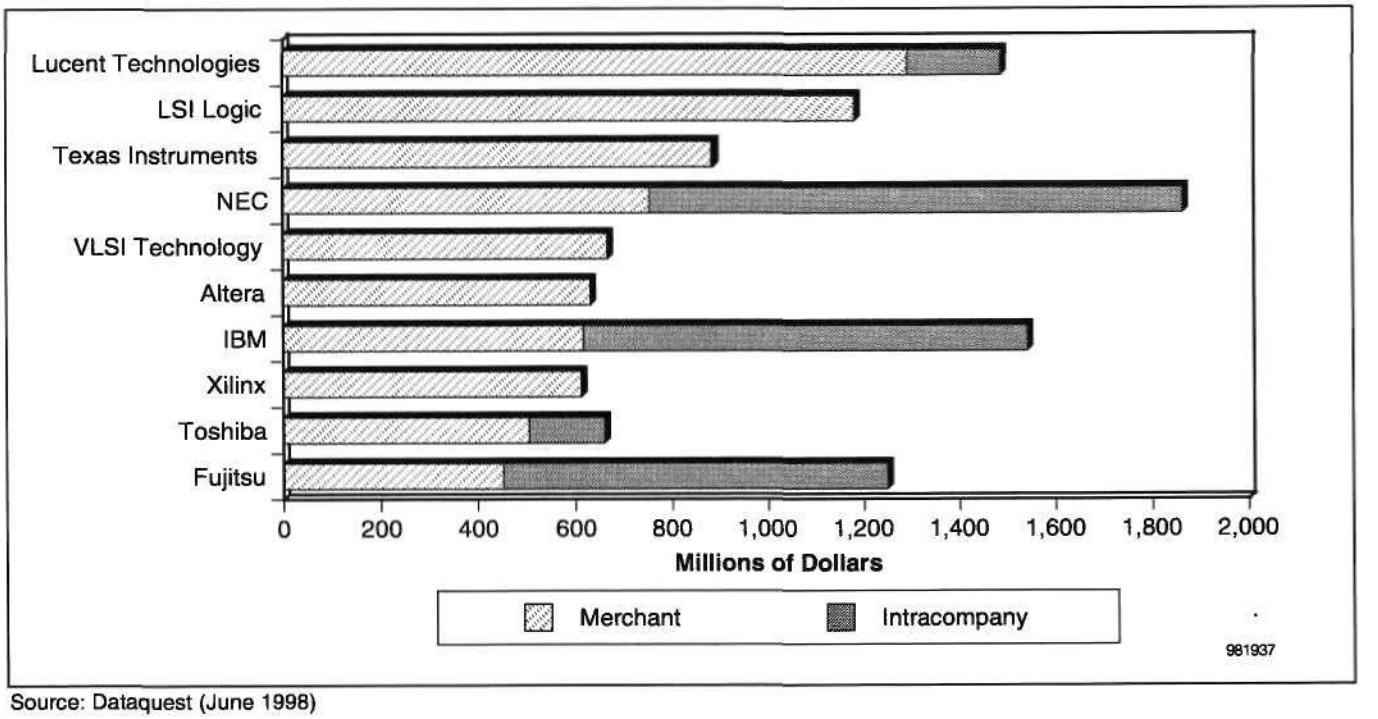
Table 1 shows the top 20 worldwide ASIC rankings. Figure 1 shows the estimated 1997 top 10 worldwide ASIC suppliers' sales, merchant versus intracompany (sales to internal divisions).

Table 1
1997 Worldwide ASIC Market Share Ranking and Revenue (Millions of Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Change (%)	1997 Market Share (%)
1	1	NEC	1,689	1,863	10.3	11.3
5	2	IBM	1,003	1,541	53.6	9.3
4	3	Lucent Technologies	1,060	1,486	40.2	9.0
3	4	Fujitsu	1,120	1,248	11.4	7.6
2	5	LSI Logic	1,136	1,182	4.0	7.2
6	6	Texas Instruments	841	886	5.4	5.4
8	7	VLSI Technology	615	667	8.5	4.0
7	8	Toshiba	836	660	-21.1	4.0
11	9	Altera	497	631	27.0	3.8
10	10	Xilinx	566	612	8.1	3.7
9	11	Hitachi	577	521	-9.7	3.2
13	12	Hewlett-Packard	380	466	22.6	2.8
12	13	SGS-Thomson	392	387	-1.3	2.3
16	14	Mitsubishi	256	296	15.6	1.8
15	15	Motorola	325	294	-9.5	1.8
14	16	Symbios	356	289	-18.8	1.7
17	17	Matsushita	252	258	2.4	1.6
18	18	Vantis (AMD)	243	243	0	1.5
19	19	Lattice	200	242	21.0	1.5
21	20	Alcatel Microelectronics	179	204	14.0	1.2

Source: Dataquest (June 1998)

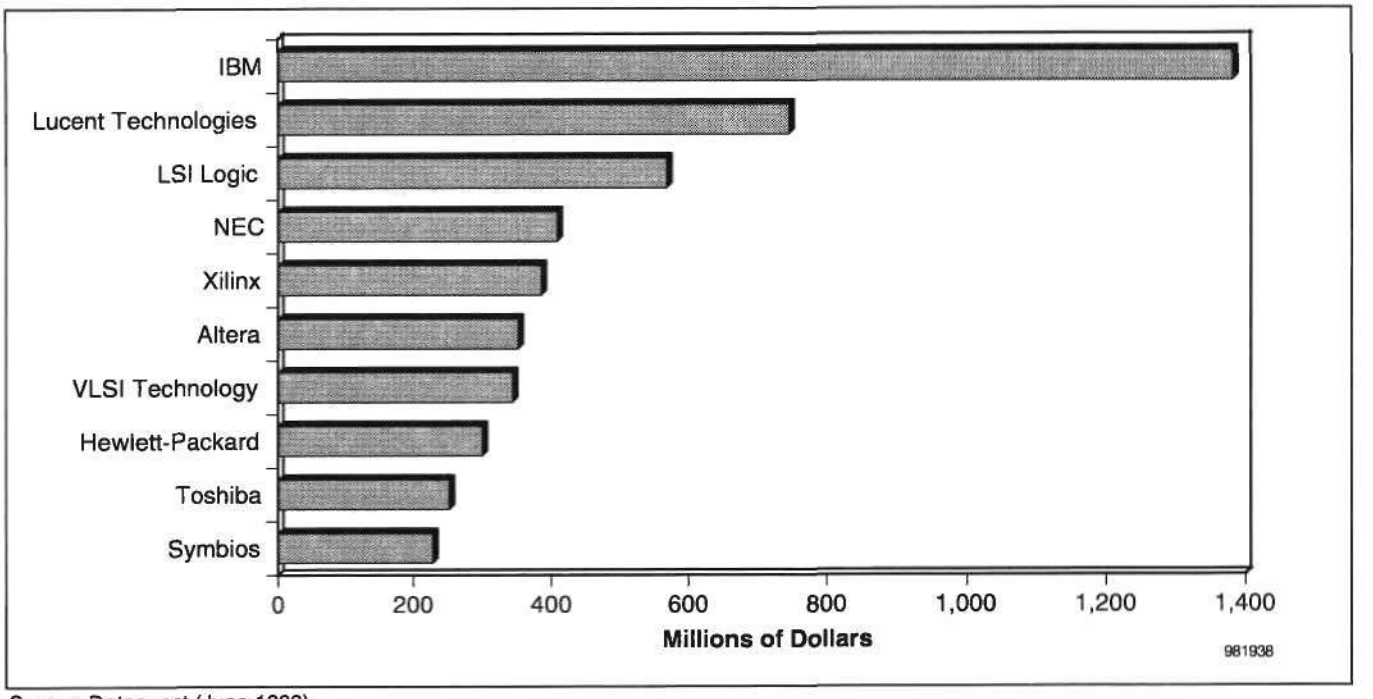
Figure 1
Estimated 1997 Top 10 Worldwide ASIC Suppliers by Type of Sale



Source: Dataquest (June 1998)

Lucent took over the No. 1 merchant supplier position from LSI Logic in 1997. We should keep in mind that Lucent Technologies is a separate company from AT&T, so sales to AT&T are counted as merchant. Lucent is a leading merchant supplier in the communications and data processing markets. IBM gained significant ground the 1997 merchant ASIC market, growing close to $400 million in just one year. IBM's merchant growth stems from four areas: computers/workstations, disk drives, networking, and wireless communications. The company has penetrated a good portion of the business of the leaders in each of the stated markets. LSI Logic is 100 percent merchant and has a well-balanced portfolio between data processing and communications; it is the leading consumer supplier. It is interesting to note that Altera and Xilinx are major players in terms of merchant revenue. Figure 2 shows a snapshot of the leading ASIC suppliers in the Americas region. For a detailed listing of all the ASIC suppliers by region, please see Dataquest's Market Statistics report, *Final 1997 Worldwide ASIC Market Share* (ASIC-WW-MS-9801, May 1998).

Figure 2
1997 Top 10 ASIC Suppliers to Americas



Source: Dataquest (June 1998)

Cell-Based IC Rankings

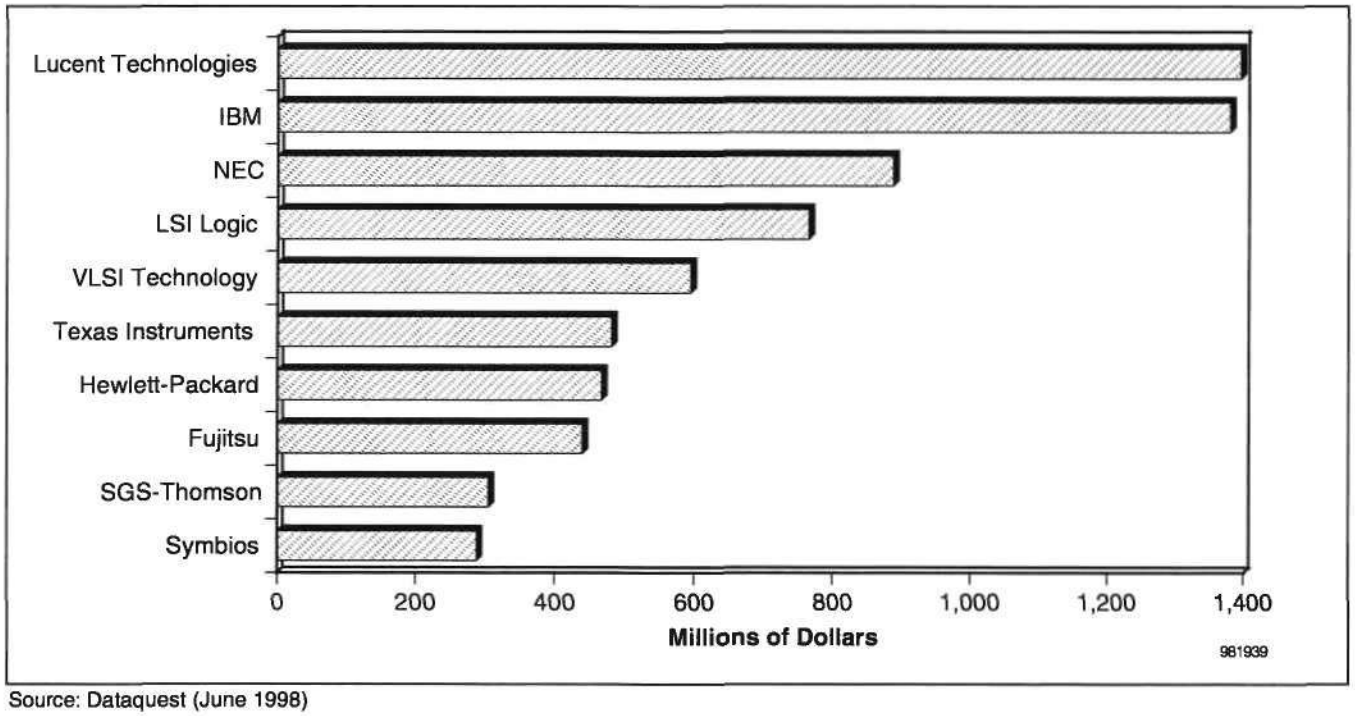
Most cell-based IC suppliers posted very respectable 1997 growth rates, as shown in Table 2. Figure 3 illustrates that Lucent and IBM have a significant lead over the remaining top 10 suppliers. NEC is taking major steps to become a leading cell-based IC supplier and has just shown the world its product road map for 0.18- and 0.15-micron ASIC products (see *The Semiconductor DQ Monday Report*, dated April 27, 1998, "NEC Tips ASIC Hand"). LSI Logic is the No. 2 merchant cell-based IC supplier, trailing only Lucent. VLSI Technology and IBM are not far behind LSI Logic, and the race is for the No. 2 merchant position, as shown in Figure 4.

Table 2
1997 Worldwide Cell-Based IC Market Share Ranking and Revenue (Millions of Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Change (%)	1997 Market Share (%)
1	1	Lucent Technologies	965	1,396	44.7	15.2
3	2	IBM	733	1,380	88.3	15.1
2	3	NEC	741	888	19.8	9.7
4	4	LSI Logic	556	765	37.6	8.3
5	5	VLSI Technology	549	595	8.4	6.5
6	6	Texas Instruments	406	480	18.2	5.2
7	7	Hewlett-Packard	380	466	22.6	5.1
8	8	Fujitsu	346	439	26.9	4.8
10	9	SGS-Thomson	305	305	0	3.3
9	10	Symbios	345	288	-16.5	3.1
11	11	Toshiba	266	250	-6.0	2.7
13	12	Alcatel Microelectronics	179	204	14.0	2.2
12	13	Hitachi	189	168	-11.1	1.8
15	14	Motorola	116	147	26.7	1.6
14	15	Matsushita	154	134	-13.0	1.5
16	16	Austria Mikro Systeme	116	109	-6.0	1.2
28	17	Gould AMI	28	107	282.1	1.2
18	18	National Semiconductor	80	87	8.7	0.9
19	19	GEC Plessey	78	80	2.6	0.9
21	20	Integrated Circuit Systems	57	73	28.1	0.8

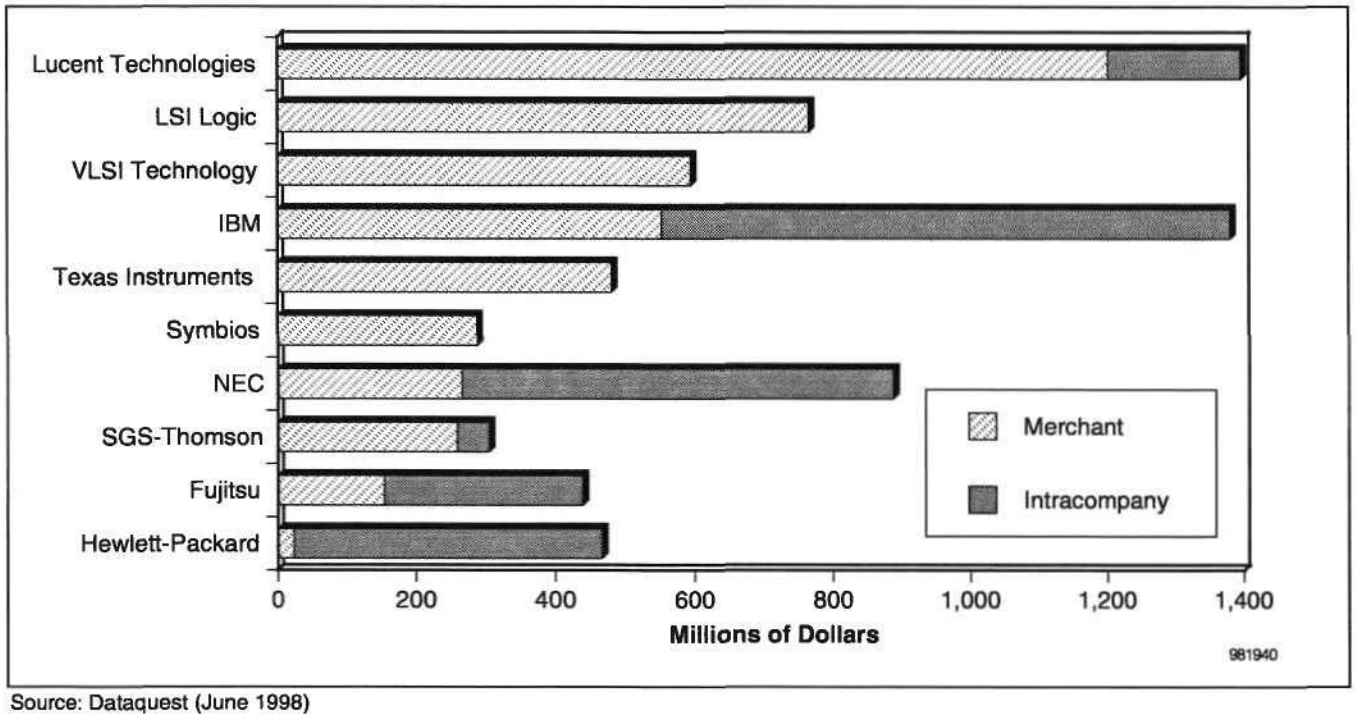
Source: Dataquest (June 1998)

Figure 3
1997 Top 10 Worldwide Cell-Based IC Suppliers



Source: Dataquest (June 1998)

Figure 4
Estimated 1997 Top 10 Worldwide Cell-Based IC Suppliers by Type of Sale



Source: Dataquest (June 1998)

Gate Array Rankings

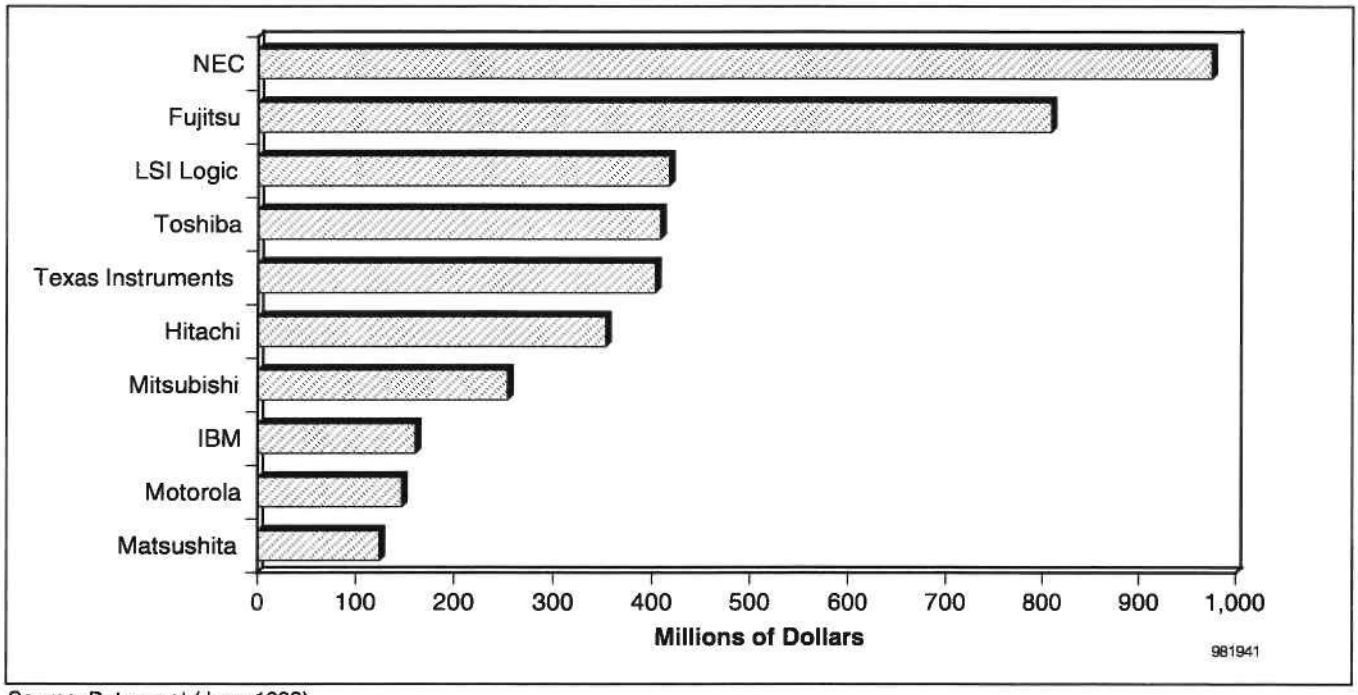
Most ASIC suppliers are not very concerned about gate array rankings because they are in a product transition from gate arrays to cell-based ICs. Table 3 shows the top 20 worldwide gate array suppliers. Figure 5 illustrates that NEC and Fujitsu remain the largest gate array suppliers because of the fact that the Japan market is holding onto gate array technology longer than the other regions. Figure 6 shows the estimated merchant gate array sales by supplier.

Table 3
1997 Worldwide Gate Array Market Share Ranking and Revenue (Millions of Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Change (%)	1997 Market Share (%)
1	1	NEC	948	975	2.8	18.5
2	2	Fujitsu	774	809	4.5	15.4
3	3	LSI Logic	580	417	-28.1	7.9
4	4	Toshiba	568	408	-28.2	7.8
5	5	Texas Instruments	430	403	-6.3	7.7
6	6	Hitachi	388	353	-9.0	6.7
8	7	Mitsubishi	223	254	13.9	4.8
7	8	IBM	270	161	-40.4	3.1
9	9	Motorola	209	147	-29.7	2.8
11	10	Matsushita	98	124	26.5	2.4
10	11	GEC Plessey	108	106	-1.9	2.0
13	12	Seiko Epson	90	98	8.9	1.9
12	13	Samsung	92	95	3.3	1.8
16	14	Gould AMI	67	87	29.9	1.7
14	15	SGS-Thomson	87	82	-5.7	1.6
18	16	VLSI Technology	66	72	9.1	1.4
17	17	LG Semicon	67	68	1.5	1.3
19	18	Sharp	65	66	1.5	1.3
15	19	Oki	69	65	-5.8	1.2
NA	20	Vitesse	0	53	NA	1.0

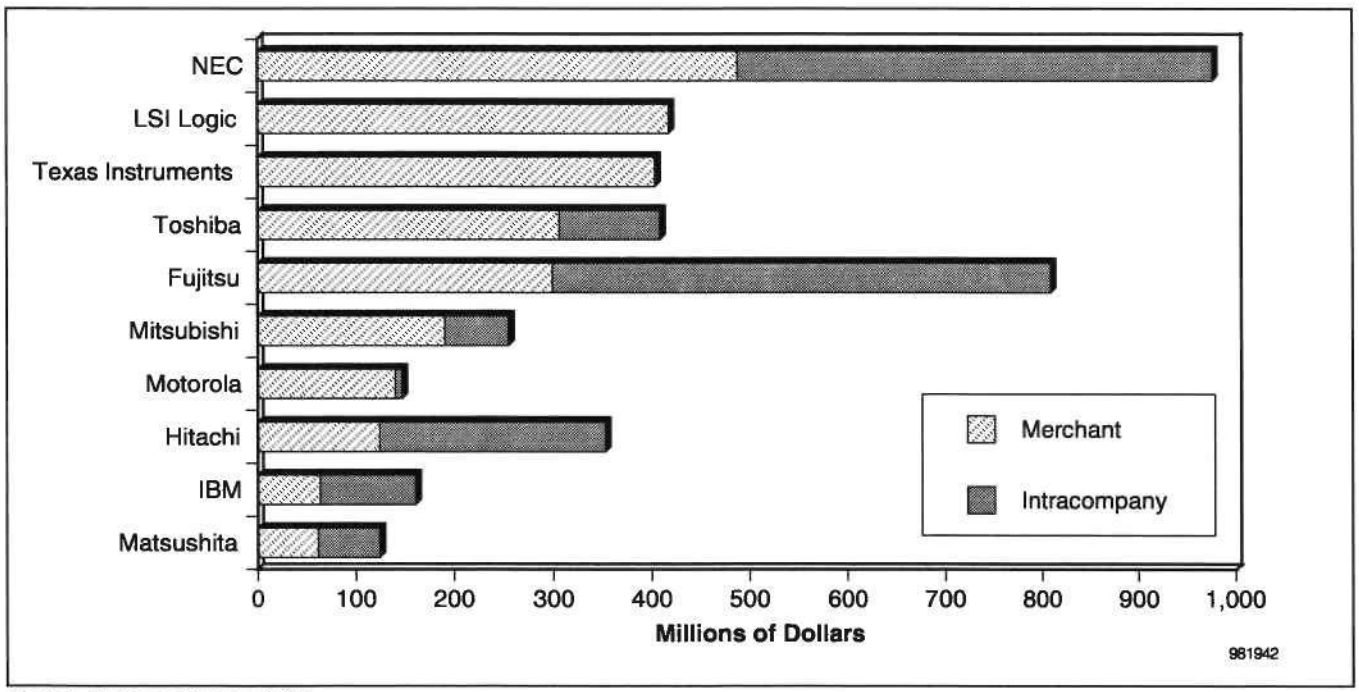
NA = Not available
Source: Dataquest (June 1998)

Figure 5
1997 Top 10 Worldwide Gate Array Suppliers



Source: Dataquest (June 1998)

Figure 6
Estimated 1997 Top 10 Worldwide Gate Array Suppliers by Type of Sale



Source: Dataquest (June 1998)

PLD Rankings

The big news on the PLD front is that Altera passed Xilinx to become the No. 1 PLD supplier. Table 4 shows that the PLD ranking remained relatively unchanged with the exception of the Altera and Xilinx exchange. Altera had the highest growth rate, 27 percent, followed by Lattice Semiconductor Corporation with 21 percent. Cypress Semiconductor Corporation was the only supplier to have a major decline in PLD revenue because of its slow product introductions caused by lack of focus on the PLD market. Figure 7 illustrates that Altera and Xilinx have a substantial lead over the rest of the field. Virtually all of the PLD market is merchant.

Table 4
1997 Worldwide PLD Market Share Ranking and Revenue (Millions of Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Change (%)	1997 Market Share (%)
2	1	Altera	497	631	27.0	30.0
1	2	Xilinx	566	612	8.1	29.1
3	3	Vantis	243	243	0	11.6
4	4	Lattice	200	242	21.0	11.5
5	5	Actel	149	156	4.7	7.4
6	6	Lucent Technologies	75	90	20.0	4.3
7	7	Cypress Semiconductor	60	52	-13.3	2.5
8	8	Atmel	34	33	-2.9	1.6
9	9	QuickLogic	25	29	16.0	1.4
11	10	Philips	3	4	33.3	0.2

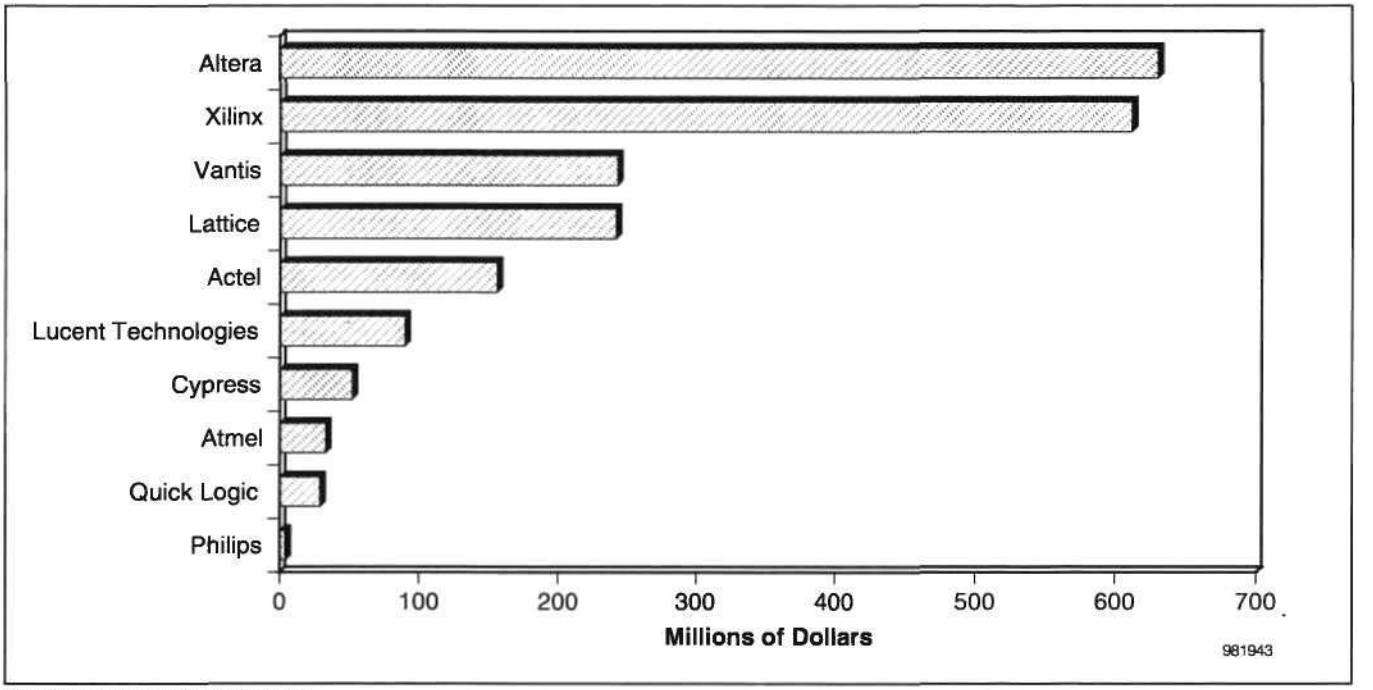
Source: Dataquest (June 1998)

Dataquest Perspective

The old school of thought was that the focused ASIC suppliers would win the war over the vertically integrated suppliers. The industry believed that ASIC companies could make quick changes because of size and the fact that they were focused. The old school has gone on an extended recess.

Vertically integrated suppliers have shown that they have some proven weapons and have the focused ASIC suppliers on the run. Large R&D budgets from prior years are paying off. Vertically integrated suppliers on the manufacturing front have proven they are a force, but the battle is far from over; they must now not only fight the ASIC suppliers but also the dedicated foundries. System knowledge is and will continue to be a beachhead for all ASIC suppliers, as this will determine the focus and cell offerings that are of paramount importance. The "system solution" offering will become the way all ASIC suppliers are evaluated. Each supplier should focus on selected target markets that suit their strengths and offer the best "system solution." For most suppliers, this will mean partnering on many fronts, including design tools, libraries, and manufacturing. The days when any individual supplier could dominate without partners are gone.

Figure 7
1997 Top 10 Worldwide PLD Suppliers



Source: Dataquest (June 1998)

Perspective

ASIC/SLI Worldwide

Market Analysis

The Convergence of Foundries and ASIC Vendors in Manufacturing SLI

Abstract: *The emergence of "system on a chip," or system-level integration, will bring new challenges and opportunities in semiconductor manufacturing. The success of the foundry and fabless models can be expected to extend to the design and manufacture of SLI chips. What impact will the new manufacturing paradigm have on traditional ASIC vendors? And how can they respond to the competitive threat posed by the foundries?*
By James Hines and Jordan Selburn

What Is System-Level Integration?

System-level integration (SLI) can be defined as putting the functionality that previously required a printed circuit board onto a single silicon chip. Originally conceived in the early 1990s, advanced silicon manufacturing, design automation tools and component libraries are now allowing the "system on a chip" to move into the mainstream market. The initial system-level designs consisted almost exclusively of digital logic constructions, but today's designs can include embedded DRAM, flash memory, and analog functions, among others.

SLI Will Dominate ASIC Revenue

Fueling the projected growth in the ASIC industry, Dataquest expects system-level designs to contribute more than 50 percent of the market's total revenue by 2002 (see Figure 1). Clients should be aware, however, that the ASICs that will contribute most of the system-level integration revenue between 2000 and 2002 are the designs that are now on the drafting board.

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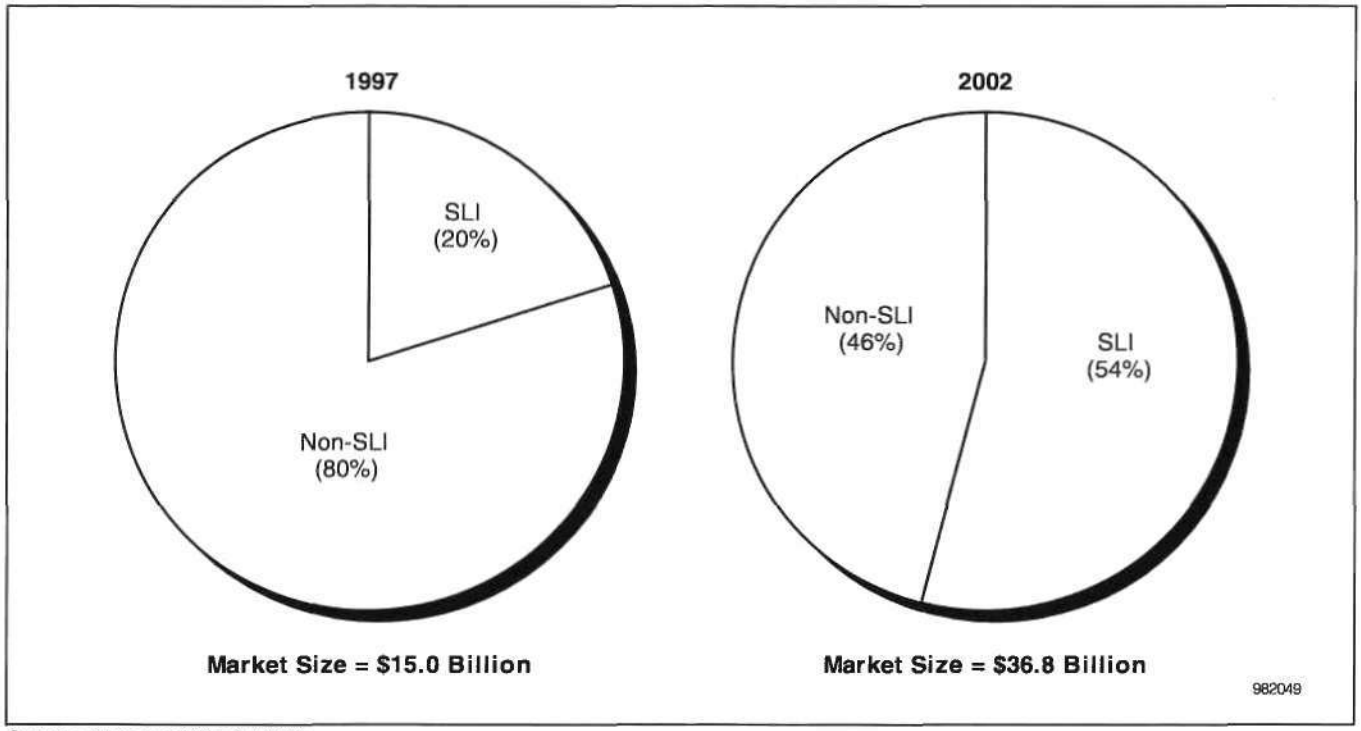
Figure 1
ASIC Market Forecast



Source: Dataquest (April 1998)

SLI Driving Foundry Market Growth

Foundry market growth is outpacing the general semiconductor market and is being driven by the explosion of fabless semiconductor companies and a trend toward greater levels of outsourcing on the part of integrated device manufacturers (IDMs). Fabless semiconductor companies represent 35 percent of foundry demand in 1997, and we expect this to grow to 40 percent by 2002.

As will become clear, the foundries and their fabless customers are well positioned to benefit from the opportunities created by SLI technology. Figure 2 shows the forecast growth of the semiconductor contract manufacturing (SCM) market from 1997 through 2002 and the increasing share of the market represented by SLI designs. Foundries and traditional ASIC vendors will be in direct competition for many of these SLI designs.

What Are the Major Drivers and Inhibitors of Foundry Manufacturing of SLI?

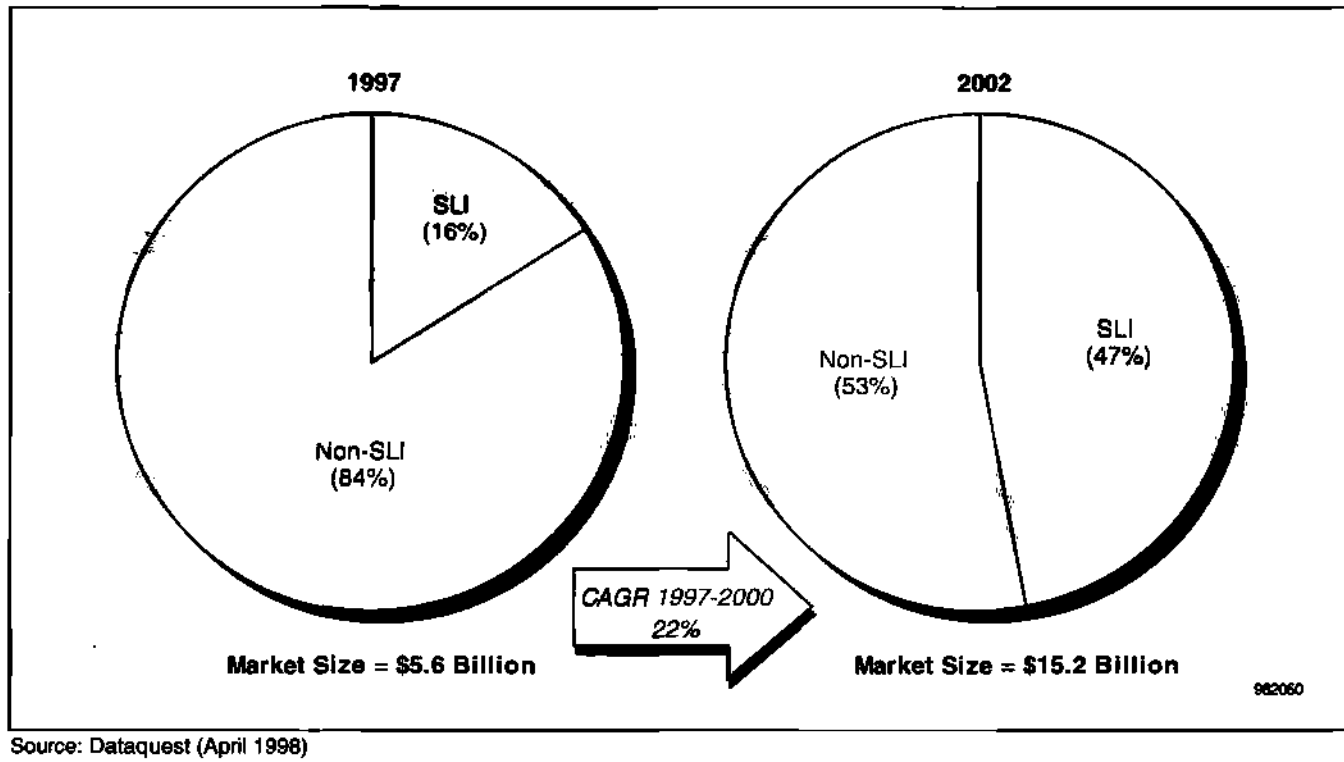
There are several factors that will influence the growth in foundry manufacturing of SLI designs, both positively and negatively. The major drivers and inhibitors are shown in Figure 3. The trend toward foundry manufacturing of SLI will be supported by the success of the Virtual Socket Interface Association (VSIA), International SEMATECH, an expanding application-specific standard product (ASSP) market, escalating fab costs, and the accelerated pace of technology development of foundries. Potential inhibitors include the continuing financial crisis in Asia, the low revenue per

square inch of silicon inherent in SLI designs, lack of adequate electronic design automation (EDA) solutions to support the most advanced manufacturing technology, and manufacturing process integration issues.

How Will Foundries Compete for SLI Designs?

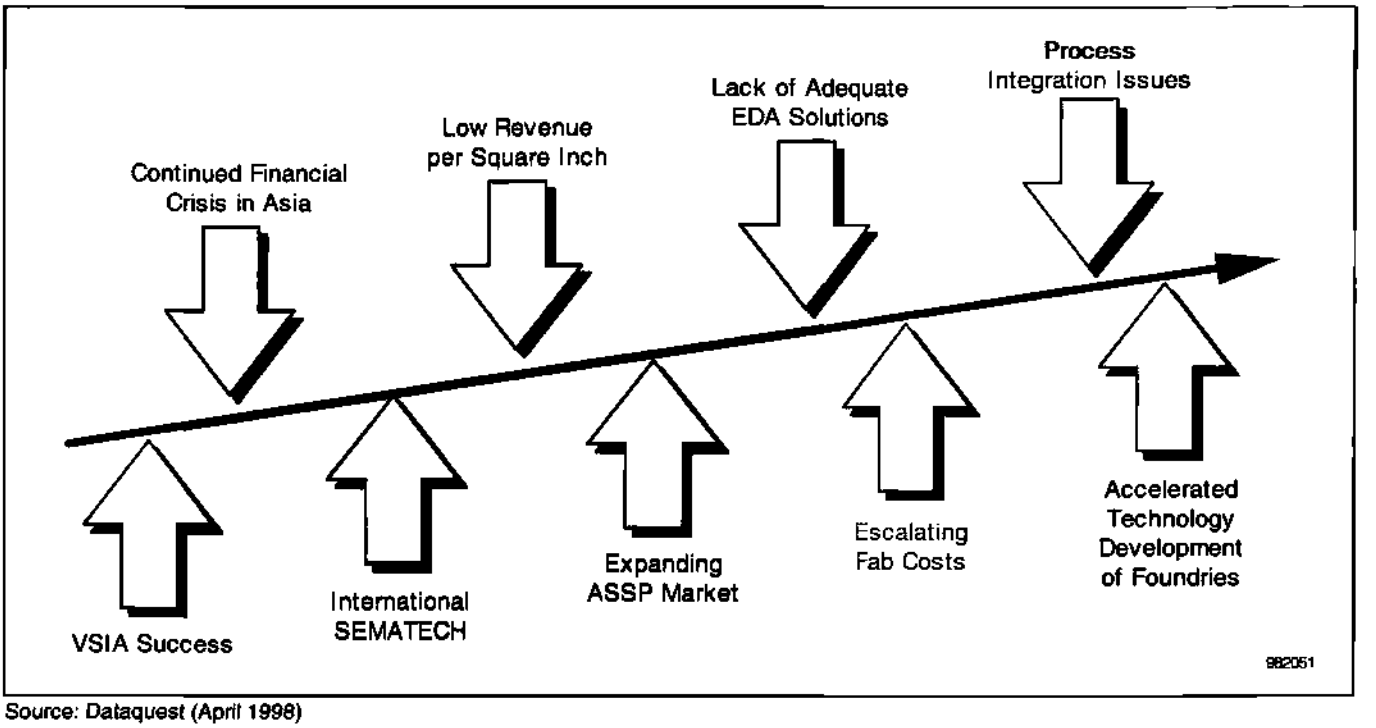
The challenge of manufacturing consumer-oriented SLI chips, as with many other semiconductor products, is fundamentally one of minimizing manufacturing cost. (In this category of SLI designs, it is assumed that lower overall system costs is one of the primary reasons for moving to SLI.) True, there are some technical problems to be overcome in mating logic and DRAM or other memory processes on the same wafer, but solutions are at hand, and even these will ultimately be evaluated on the basis of their impact on manufacturing cost. SLI chips, by virtue of their combination of memory and logic functions, will generate less revenue per square inch of silicon than most pure logic chips, including traditional ASIC designs. In order to sustain acceptable margins, costs must be reduced.

Figure 2
SCM Market Forecast



Source: Dataquest (April 1998)

Figure 3
Drivers and Inhibitors of Foundry Manufacture of SLI



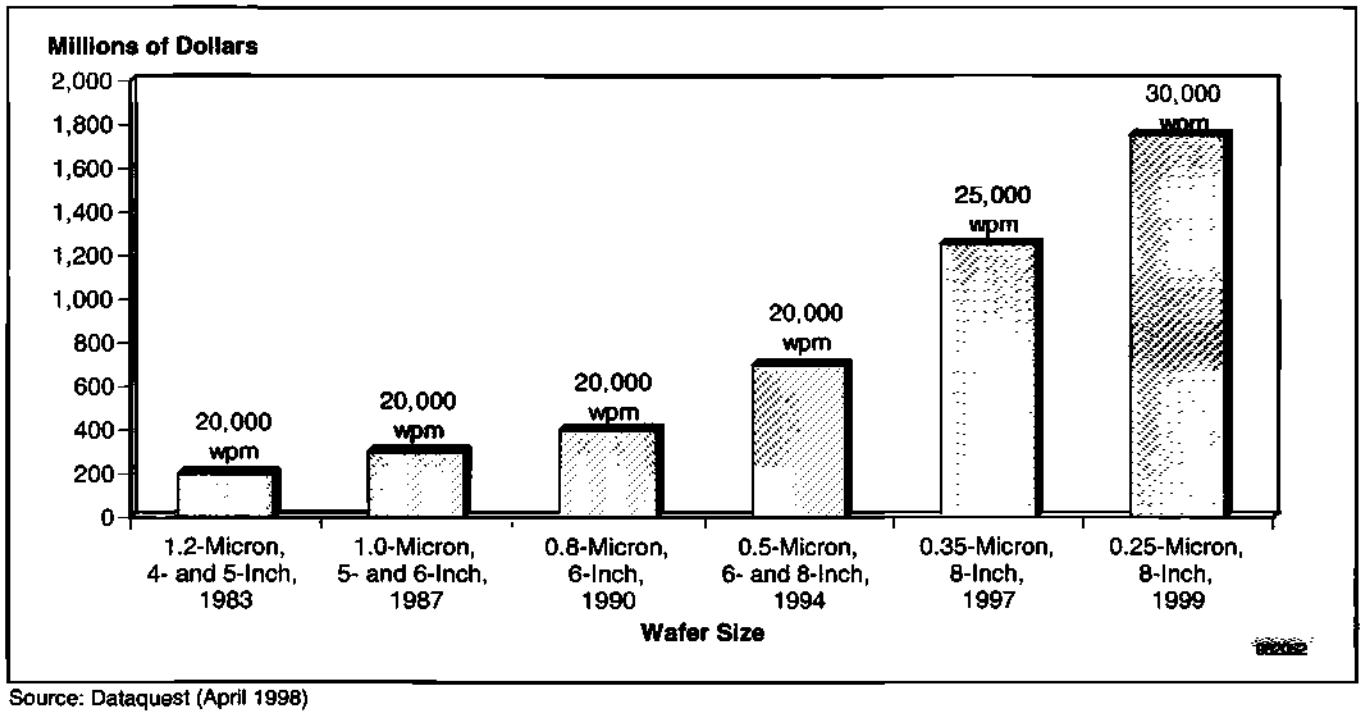
Source: Dataquest (April 1998)

Foundries are expert at minimizing manufacturing cost. This is achieved primarily through economies of scale, aggregating the demand of several customers in a high-volume factory operating at very high capacity utilization rates. In the capital-intensive semiconductor manufacturing business, capacity utilization is the key to achieving low manufacturing cost. Foundries have also standardized their process flows, enabling them to accommodate a variety of customer requirements with a minimum of configuration changes. Also, many foundries are taking advantage of developments in factory automation technology to further enhance manufacturing efficiency and reduce cycle time.

Concentration of Capital and Concentration of Capacity

Rising wafer fabrication facility costs greatly increase the capital requirements for semiconductor manufacturing companies. The escalating cost of new fabs is shown in Figure 4. Only large semiconductor manufacturers can justify investing $1.5 billion or more in a new advanced technology fab solely for production of their own products. Foundries keep their large fabs full by aggregating the demand of smaller customers, thus achieving high factory utilization rates. Higher fab costs will favor a concentration of capital in the large fabs of foundry suppliers, giving them greater economies of scale.

Figure 4
The Escalating Cost of Fab Construction



Source: Dataquest (April 1998)

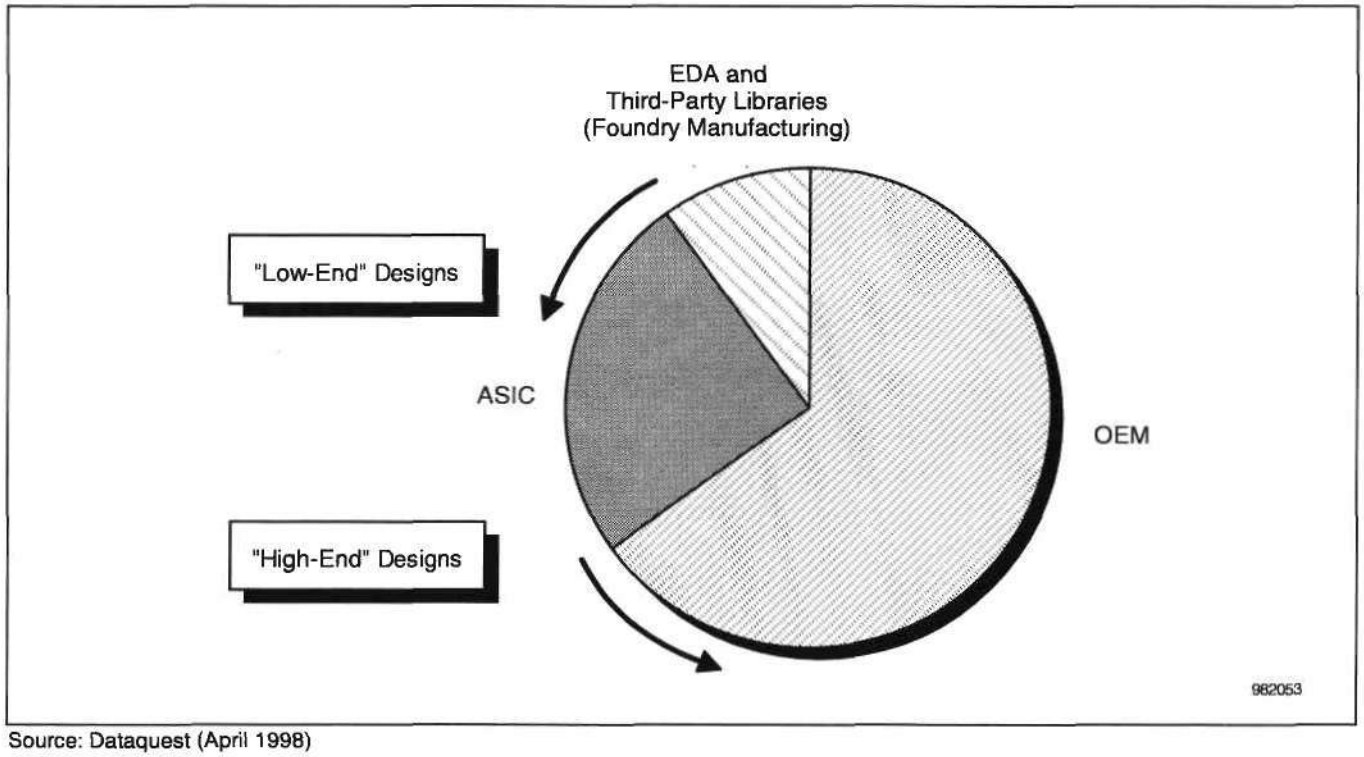
New fabs are not only more costly, but they are also larger in terms of total silicon production capacity. In 1983, semiconductors were being manufactured on 4-inch and 5-inch diameter wafers, and the largest fabs were being operated at 20,000 wafer starts per month. Since then, both the size of the wafers and the wafer capacity have increased, combining to give dramatic increases in capacity in terms of total silicon area. So a portion of the cost increase of a new fab can be directly attributed to an increase in the real silicon capacity of that fab. This trend is giving rise to a concentration of capacity in ever larger high-volume fabs, many of which are now being built by foundry companies. This increasing capacity per fab will make it more difficult for a dedicated ASIC vendor to fill a new captive fab.

Shifting Roles in Semiconductor Design

The widespread availability of standardized EDA tools and third-party libraries is enabling fabless companies and design service companies to compete for designs that have historically been the province of ASIC vendors. These designs are then manufactured by foundries. This shift in the distribution of semiconductor designs is shown in Figure 5.

Dataquest expects the emergence of these foundry-manufactured designs to squeeze the traditional ASIC companies and cause them to look toward systems OEMs for design opportunities. Fabless semiconductor companies and so-called "chipless" design companies are likely to participate in many SLI designs in a variety of low- to high-volume applications.

Figure 5
Semiconductor Design Market Segmentation



Source: Dataquest (April 1998)

The Impact of VSIA

The design of single-chip systems becomes almost impossible without the ability to reuse system-level macro (SLM) blocks. The Virtual Socket Interface Alliance is one of several ongoing efforts to enable design reuse; if successful, this would allow for rapid and widespread distribution of third-party SLMs. OEMs and design houses would then have access to the system-level macros necessary for foundry manufacture of system-level chips. In-demand SLMs will quickly become commodities, and their ability to add value will decrease rapidly.

The VSIA consortium has defined the problems that must be solved by OEMs and design houses to compete with ASIC vendors and is now working toward the solution. Dataquest believes that a usable implementation of a VSIA solution could occur in about two years. There are some major potential roadblocks in addition to the technical challenges, however. VSIA was initiated by the EDA community, and there is a lingering question as to whether the leading SLI ASIC companies will participate with their hearts as well as their minds. VSIA must also overcome the "designed by committee" problem—more than two people can't decide on where to have lunch, much less anything important.

How Will ASIC Manufacturers Respond to Competition from the Foundries?

ASIC Vendors Will Target Specific End Markets

To achieve economies of scale, the silicon foundries must try to appeal to as broad a customer base as possible. This requires a process technology that is designed to avoid shutting out potential customers rather than one designed to attract customers. The result of this approach is a process that is fairly fast with reasonably low power consumption; if the foundry tunes the process in one direction, it is likely to optimize it in the direction of highest logic density to minimize costs.

The ASIC vendor, on the other hand, can make trade-offs that result in a product optimized for some applications at the expense of others—for example, in a silicon process targeted for the wireless communications market, a transistor could be designed to sacrifice largely unneeded performance and reduce static and dynamic power consumption, extending battery life. An example of this is the trade-off between transistor speed and leakage current. In a cellular phone system-level ASIC, an optimal process would trade performance (to the minimum level required by the on-chip digital signal processor, or DSP) for a lower leakage current; a process targeted toward high-performance desktop applications such as workstations would make the opposite trade-off. This is one way that the dedicated ASIC vendors can continue to differentiate their products, although it can make that vendor highly vulnerable to variations in the targeted market. This approach can also make it more difficult to fill a modern high-capacity fab.

In comparison to markets for standard parts such as DRAM and microprocessors, ASIC vendors require significantly more customer interaction.

As a way to provide targeted support beyond the current capability of the foundries, ASIC vendors are (and, in some cases, have been for a while) setting up engineering teams dedicated to specific application markets. This approach also allows an ASIC vendor to design its own chips—ASSPs—and sell these parts to multiple customers. Examples of these include DVD controllers and Global System for Mobile Communications (GSM) chipsets. At present, foundries lag far behind leading ASIC vendors in application-focused customer support; making up this difference will be an expensive and time-consuming effort and may not be successful ultimately.

ASIC Vendors Will Take Foundry Business

One option for an ASIC vendor determined to own and operate a silicon fabrication plant is to compete with the foundries at their own game. Foundry business can allow an ASIC vendor to fill some unused capacity. Even if this business has a low gross profit margin (and the fab business is likely to have a low margin, compared to system-level ASIC designs), it can be beneficial for the ASIC vendor by spreading fab and other corporate fixed costs over a larger amount of production. Some of the issues in pricing against foundry competition are compensated for in the ASIC vendor's lead in process technology, which allows the production of smaller, lower-cost

die. This lead, currently at about one process generation, is decreasing, however, and may not last more than a few more years.

ASIC vendors must be extremely careful not to overcommit to the foundry business, however attractive this business may seem during down cycles. When business for SLI designs improves, the ASIC vendor may not be able to book these higher-value opportunities if the fab is full of low-margin foundry business. Because the average design is in volume production for more than two years, the ASIC company must perform a careful evaluation of foundry production.

ASIC Vendors Will Partner with the Foundries

"If you can't beat 'em, join 'em." Some ASIC vendors are working with the foundries rather than competing against them. VLSI Technology Inc. and Wafer Technology Malaysia are an example of this type of working relationship. VLSI, while still making some investment in its captive San Antonio, Texas, fab, has the right to purchase a sizable amount of WTM's capacity; this capacity is scheduled to come on line in 2000. This partnership gives VLSI the option, for example, to tune the San Antonio process for the wireless market, which represents VLSI's largest segment, while using WTM for more generic production. In addition to the business partnership, VLSI and WTM are working together on process development.

Another major advantage to partnering with foundries is manufacturing flexibility. With a foundry partner, an ASIC vendor can reduce the business and financial risks associated with a new or expanded fab. In down cycles, the ASIC vendor does not carry the sizable fixed costs of unused fab capacity, yet retains the ability to quickly ramp production for a major SLI design. Also, the second-source capability of a foundry partner can be quite attractive to customers concerned about putting the manufacturing of a key system component in one fab.

Dataquest Perspective

The OEM Perspective

In most supplier wars, the customer comes out the winner, and the foundry-ASIC vendor battle is no exception. In this case, the OEM will have more competition vying for its mainstream SLI business. As the industry infrastructure of design houses and third-party system-level macro providers matures, OEMs will have a number of options:

- Outsource manufacturing to the foundries for the lowest-cost products, with the design done either in-house or by a third-party design services company. The former allows the OEM to maintain total control of intellectual property value-added, and the latter can provide easy access to a wide range of independent intellectual property and a broad selection of foundries. Some foundries are starting to offer turnkey solutions (for example, wafer fabrication, packaging, assembly, and testing services).

- Partner with ASIC vendors for application optimization. This is the current business model for most SLI designs, and it can provide the OEM with significant influence over the product development process within an ASIC vendor. This may continue to be the choice of OEMs striving to differentiate their products on a basis other than cost.

The Foundry Perspective

The name of the game in manufacturing SLI, as with most other semiconductor products, will be to minimize cost. Because of their superior economies of scale and manufacturing efficiencies, foundries are best suited to meet the challenge of low-cost SLI production. The concentration of capital in the high-capacity fabs of the foundries and the importance of manufacturing process technology will continue to drive the shift to the foundry model. The widespread availability of EDA tools and third-party intellectual property libraries, and the standardization efforts of the VSIA, will give designers the ability to implement SLI designs in silicon, which can then be transferred to the foundries for production.

The ASIC Vendor Perspective

ASIC vendors will come under increasing pressure from foundries. The time frame is far from certain, but in the not too distant future Dataquest believes that foundry manufacture will become a viable approach for many mainstream SLI designs. When this happens, the price pressure on dedicated ASIC vendors will become intense.

ASIC vendors must continue to focus on product differentiation. Either processes tuned to applications or dedicated customer support familiar with the market as well as the OEM will be critical factors. ASIC vendors that can target application markets will have the best chance to survive the foundry onslaught; those that try to be everything to every customer will almost certainly be doomed to failure.

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Perspective

ASIC/SLI Worldwide

Technology Analysis

Evolution of Packaging Technology for SLI ASICs

Abstract: *The low-cost ball grid array package has gained wide acceptance for 0.35-micron system-level integration ASICs. As gate counts reach 500,000 to 1.5 million and system frequency exceeds 100 MHz, a cost-effective package design is critical. To maximize performance of these devices, package designs need to be 200 to 350 pins, with external operating frequencies of 66 MHz to 150 MHz. ASIC vendors are using low-cost BGAs at or below the cost of conventional PQFPs. This has accelerated BGA market growth and the implementation of other new package technologies, such as chip-scale packages and flip-chip attach.*

By Yoshihisa Toyosaki

Evolution of High-Density Attach Technology

Increased use of high-density attach technologies has emerged with new information equipment markets, such as personal digital assistants (PDAs), cellular phone, and mobile computers, and with new consumer electronics markets, such as digital camcorders and digital still cameras. Growth of small-form-factor and handheld equipment designs increased demand earlier than expected for new chip-scale packages (CSPs), ball grid arrays (BGAs), combinations of BGAs with flip chip, as well as direct chip attach (DCA) and known good die (KGD). To house leading-edge packages and KGD printed circuit board (PCB) developments such as surface laminate circuit (SLC), a buildup substrate technique developed by IBM Japan is being widely adopted in numerous applications that require miniaturization. Dataquest believes, however, that there are hurdles to these new package and substrate technologies. Some of the hurdles include a limited number of buildup substrate suppliers, high design costs, and delay in the effort to develop package standards between Japan and the United States for CSPs and BGAs.

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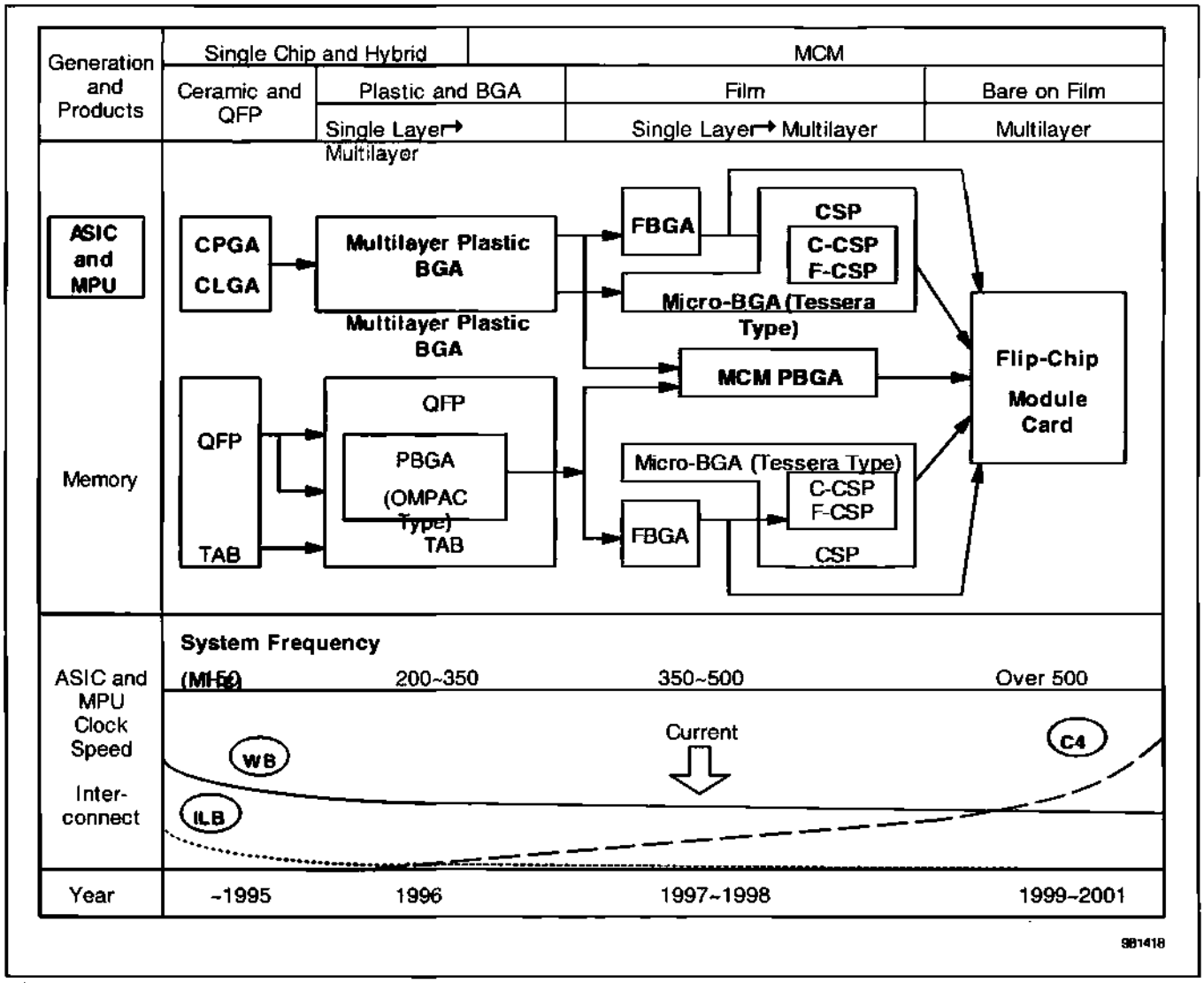
Figure 1 shows a road map for leading-edge packaging technologies to 2001. The evolutionary path is based on the system block frequency required for each generation of MPU, which is closely associated with application-specific ICs (ASICs), and the key technologies required to implement the designs.

Figure 1
Advanced Packaging Road Map



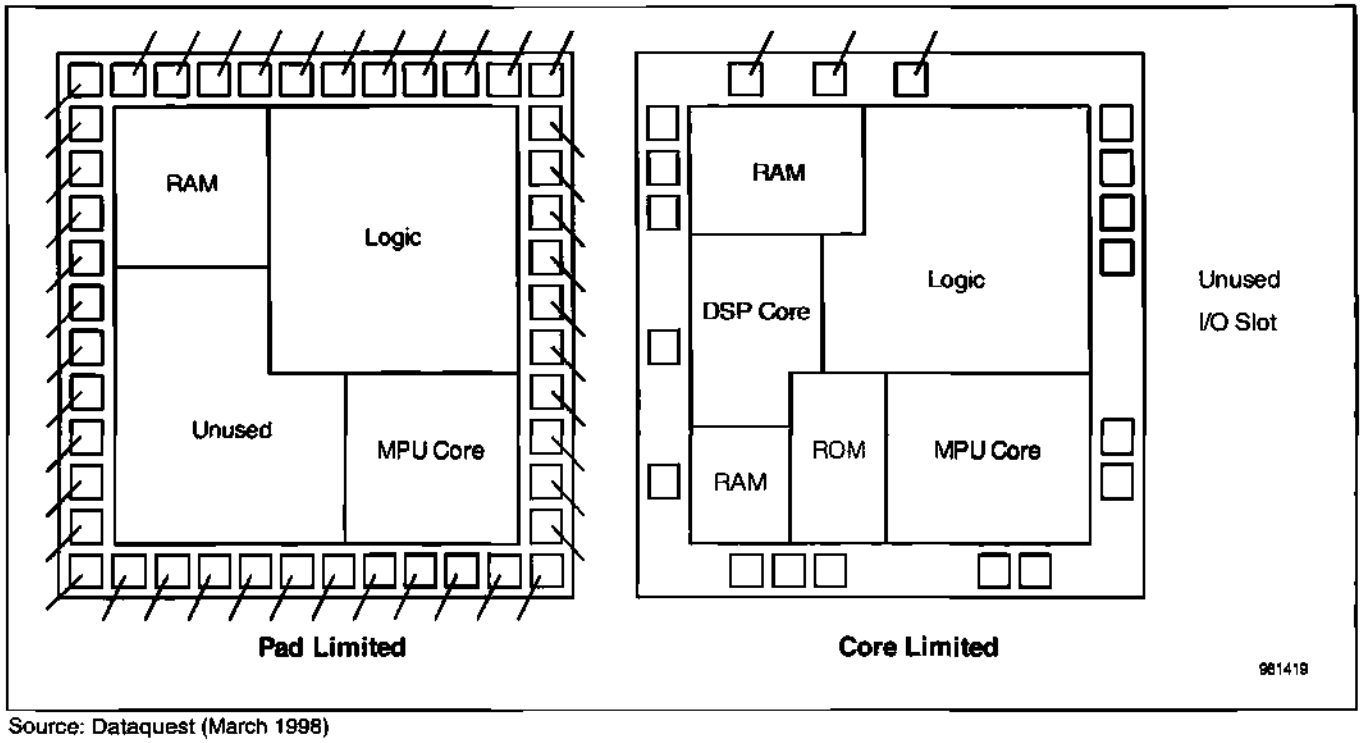
WB = Wire bonding
ILB = Inner lead bonding
C4 = Controlled-collapse chip connection
Source: Dataquest (March 1998)

Pad-Limited and Core-Limited Designs in SLI ASICs

Although finer process technologies lead directly to an increase in gate counts accommodated in the same die size, Dataquest sees a risk of "I/O pad-limited design," where the die size is governed by the number of I/Os in some applications. Interconnect technology varies with package type, but the ability to reduce the I/O pad size required for bonding a die and a package is

limited. The area of the die per side (in square millimeters) needed to secure the required I/O counts is a physical limitation resulting in a larger die area than that designed (see Figure 2). This design trend is frequently seen in gate arrays. Previously, "core-limited designs" were common. Applications limited by die size have declined with the pervasiveness of 0.5- to 0.35-micron process technology and commercialization of a 0.25-micron high-density ASIC process technology. Nevertheless, core-limited designs will persist in some applications, such as DVD encoders that require large circuits and switching systems demanding large DRAM capacities (memory space switchlike applications). In particular, Dataquest believes that this need will continue in consumer applications in which single-chip implementation using system-level integration (SLI) ASICs is an important goal.

Figure 2
Situation of Pad-Limited and Core-Limited Designs



Source: Dataquest (March 1998)

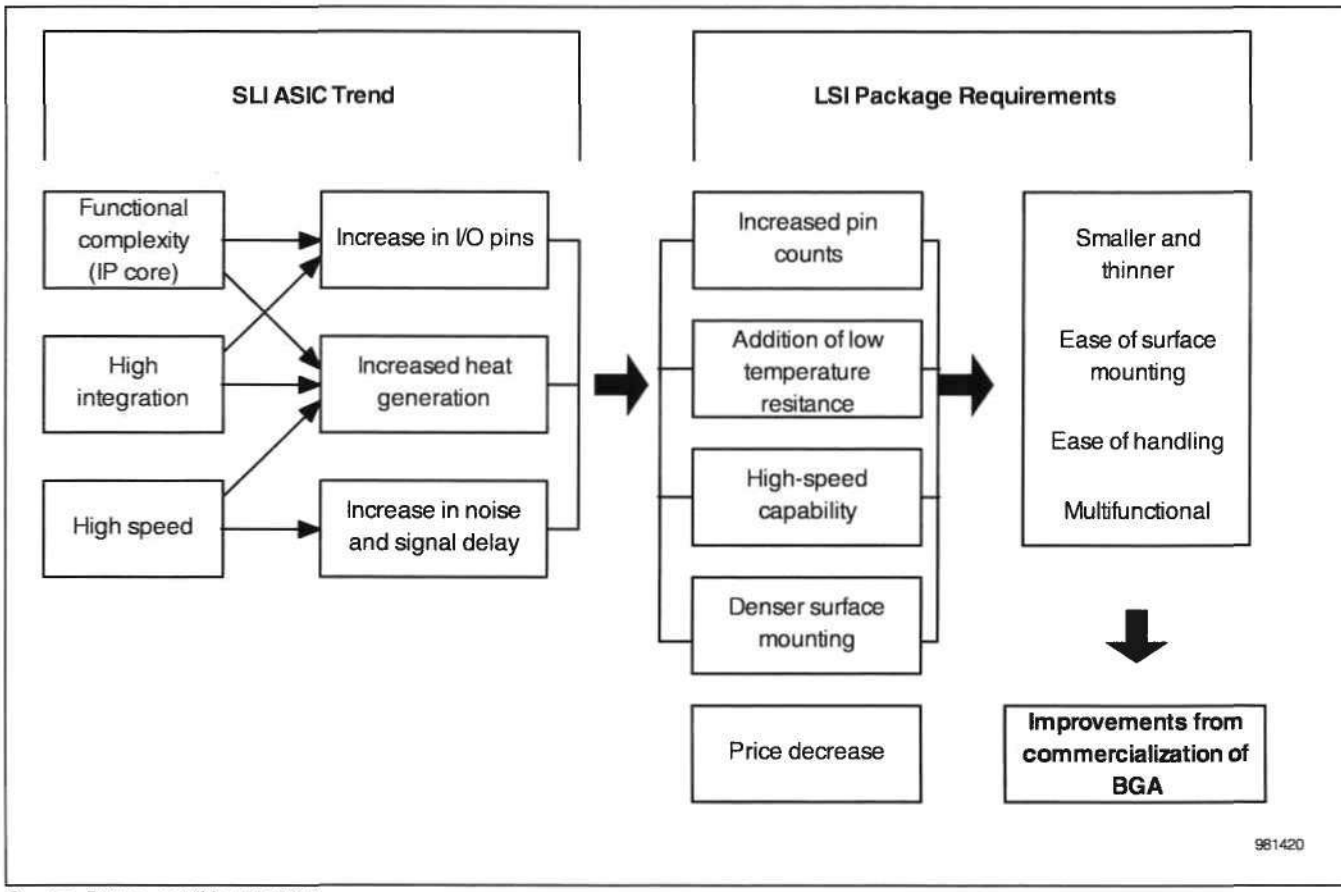
BGA Package and Development Targets

Conventional plastic quad flat packages (PQFPs) are generally limited to 304 pins and 50 MHz by inductance issues. BGA technology raises limitation levels to 750 pins and 200 MHz.

In the plastic ball grid array (PBGA) package structure, the chip surface area contains circuitlike die attach patterns and signal patterns. The chip is mounted by using a die bonder and epoxy-based silver paste. The package is characterized by a single-side resin sealing structure that allows an array of solder balls (I/O and power source) to reach the lower side of the IC, resulting in a wider pitch and enabling a smaller and thinner package. Major characteristics of the low-cost BGA (overmolded plastic pad array, or

OMPAC) developed by Motorola Incorporated, currently the mainstream BGA package design, are shown in Figure 3.

Figure 3
BGA Package for ASICs



Source: Dataquest (March 1998)

Current State of CSP

CSP is a compact package with a size more or less equivalent to the die area. Although many CSP technologies have been developed, most of them have a common feature, which is to provide a dense area array on the underside of a package. Compared to BGAs, CSPs offer better marketability because they occupy a relatively smaller area on a PCB, resulting in a cost advantage, especially for portable applications. Size reduction also leads to improved electrical performance.

Major markets for the CSP include consumer applications such as digital camcorders and portable DVD and communications applications such as modem cards and mobile phones. As designs for these applications face increasingly strict size and cost demands, the CSP must also satisfy other requirements. Emerging applications require relatively small pin counts (176 or fewer as of 1997), and many of these are limited by the height, length, and width of a package. CSP, the smallest package, is primarily used for memory products such as flash and SRAM, as well as for discrete devices. These

devices have variable die sizes and yet require very small pin counts (50 or fewer). This makes them highly suitable for the chip-size CSPs.

Naturally, there are various problems with CSPs. Obstacles include a higher initial packaging cost and limited wiring patterns on a PCB. These are important design considerations in consumer applications. Higher equipment costs could delay full acceptance of the CSP, but suppliers must meet user demands for package miniaturization and the most cost-effective package solution. Some of the current solutions include the narrow-pitched low quad flat pack (LQFP) as well as the BGA. As the industry's infrastructure improves, CSPs will gradually move into mainstream applications with high pin counts. CSPs are now used in digital camcorders, which use PCBs with six to eight layers with buildup substrates.

The CSP is best suited to applications that require mounting of devices with low pin counts on very small, very dense PCBs. Some of these applications use PCB designs with 176 or fewer pins (see Table 1 and Figure 4). DVD manufacturers set the highest priority on small form factor and light weight, using SLC, a high-cost laminate substrate. This design application enables CSP packaging in an area array pattern. However, CSP is unsuitable for computing and communications applications that use very large PCBs with high pin counts. CSPs used in memory applications are expected to go into volume production late 1998. This will accelerate development of the infrastructure and widen market acceptance for CSP technology.

The CSP design of Sharp Electronics Corporation and Texas Instruments Japan is an extension of existing technologies, rather than a technological breakthrough. The primary goal is to minimize costs and development risks. Technological advances include a ball pitch of less than 1.27mm—for example, 1.0mm, and 0.8mm. The package size will continue to be reduced until the die becomes a limiting factor.

Table 1
Expected Pin Counts in Digital Camcorders by Generation

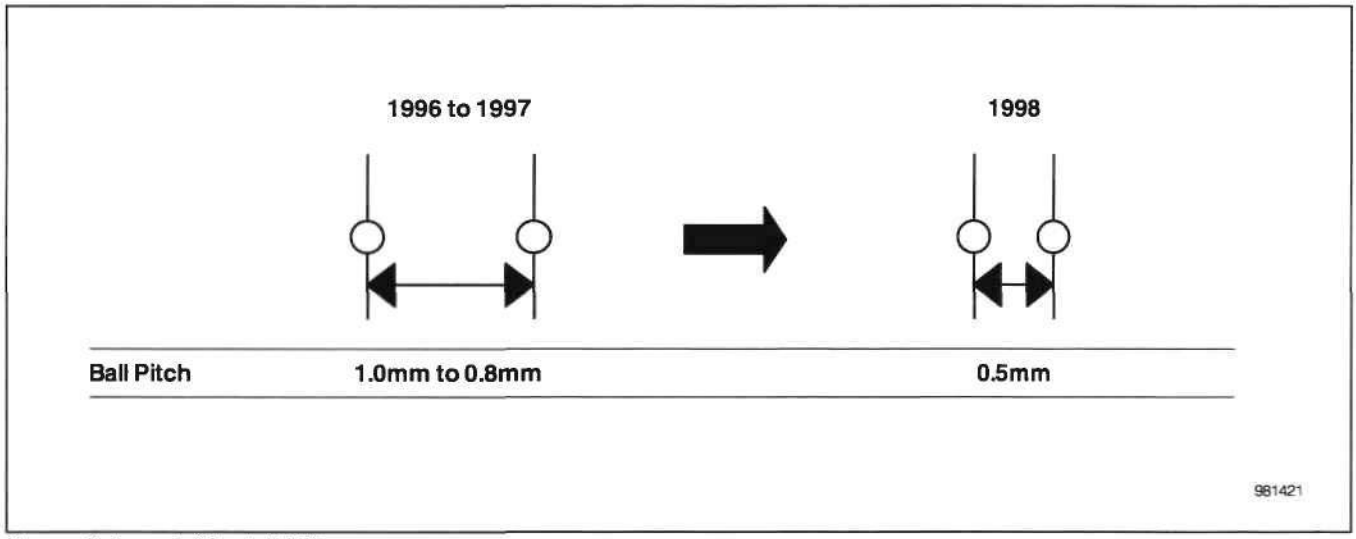
Digital Camcorder Manufacturer	First Generation	Second Generation	Third Generation
Company A	64 to 144 pins	80 to 144 pins	100 to 120 pins
Company B and Company C	80 to 164 pins	100 to 176 pins	176 to 256 pins
Company D	100 to 160 pins, mainly 144 pins	176 pins	208 to 304 pins, single chip

Source: Dataquest (March 1998)

According to digital camcorder designers, assembly cost for the LQFP package with about 100 pins is around ¥1 per pin. However, the cost of CSP assembly is relatively high because it is in the prevolume production stage (see Figure 5). Major cost adders include higher material costs, assembly yield, and new equipment requirements (including tooling, R&D, and

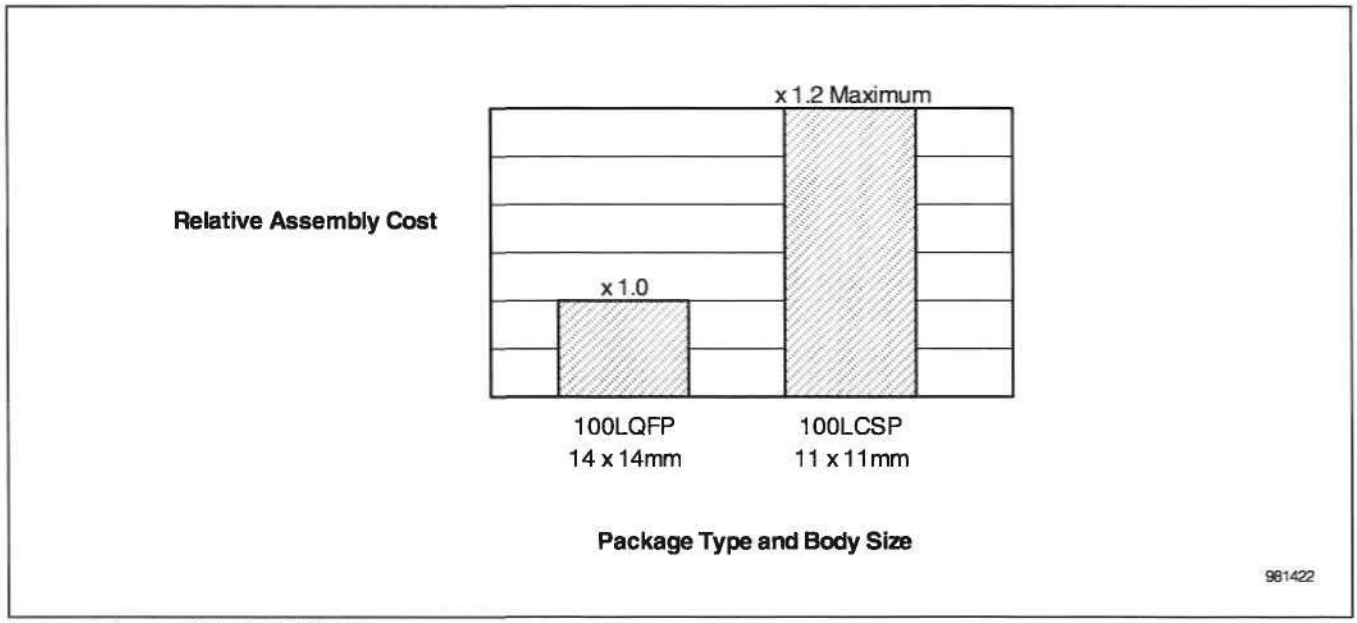
qualification costs). The CSP assembly cost acceptable to digital camcorder users is a maximum of 20 percent higher than the LQFP cost.

Figure 4
Expected Narrowing of Ball Pitch in CSP Package for Digital Camcorder Application



Source: Dataquest (March 1998)

Figure 5
Analysis of CSP Package Cost Demanded by Digital Camcorder Makers



Source: Dataquest (March 1998)

Flip-Chip Technology

Flip-chip technology is being viewed as another advanced attach solution for high-performance and high-pin-count application markets. Yet, there are

many issues to be overcome before commercial application of the flip-chip technology to ASICs. Some of these issues are summarized as follows:

- A limited number of designers and engineers who have experience in development and volume production of flip-chip products
- Restriction on package assembly technology using the new flip-chip technology, including internal wiring (often conflicting with package patents held by IBM, Tessera Inc., Matsushita Electrical Industrial Company Ltd., and Hitachi Ltd.)
- Production capacities of suppliers and subcontractors, as well as their business strategies and investment in flip-chip technology
- Additional cost incurred according to structure, varying with package type and design (mask cost and turnaround time)
- Failure analysis requirements attributable to design (circuit and bump, among others)
- Issues related to alpha particles and electric coupling, attributable to design
- CAD systems (to establish layout methods for internal core and I/O cells)
- Wafer sort (high-cost probe guard, long lead times, and customized development because of the nonstandard footprint)
- Establishment of flip-chip technology and package qualification methods

Figure 6 shows flip-chip technology road map trends required for the technology to evolve through each generation and mature at a low cost.

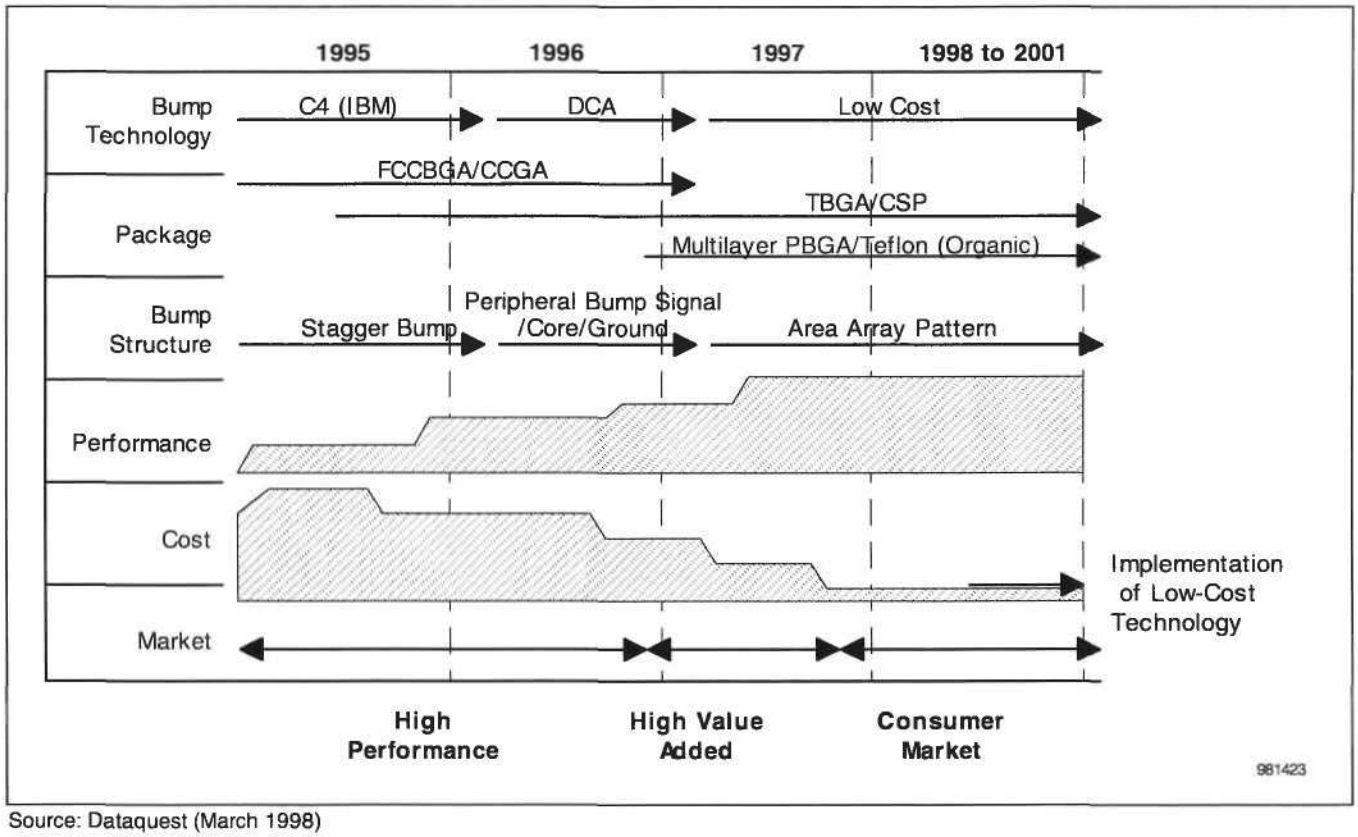
IBM's Controlled Collapse Chip Connection (C4) flip-chip technology, now licensed by many semiconductor suppliers, is widely used in advanced computer and emerging communications handset applications. Major characteristics of flip-chip technology developed by IBM include the following:

- Ease of securing high contact points: Electrical contacts can be placed over the entire surface of a semiconductor device in an array pattern. Although the present basic designs are limited to a 250-micron pitch and a solder ball diameter of 100 microns, further shrinkage is feasible by taking into account the consistency of coefficient of thermal expansion between the device and the substrate and selection of a soldering material.
- Ease of high-performance design: Contacts can be placed on any location over the entire surface of a device. The ability to minimize inductance or impedance leads to electrically advantageous designs.
- Enabling higher integration on the device: By allowing formation of contacts on an active area of a device, the flip-chip design enables finer-geometry design for a die.
- High productivity: High-quality batch bonding by reflow methods facilitates the reworkability of a device.

- High reliability: In addition to field-proven highly reliable soldering, the self-alignment effect created by surface tension as the solder melts assures highly precise and reliable bonding of a small form factor.

In spite of the technological challenges of flip chip, leading-edge ASIC companies are stepping up their efforts to commercialize flip-chip technology in order to leverage its advantages, which are being demanded by systems companies.

Figure 6
Evolution of Flip-Chip Technology and Cost Trends



Source: Dataquest (March 1998)

Technical Requirements for ASIC Packages by Market Segment

Tables 2 through 4 show technical requirements for ASIC packages by major applications in each market segment. Table 5 shows market requirements for high-speed I/O, an important factor in package development.

Performance requirements for packages from the system side are shown in Table 6 and rated on a five-point scale. Table 7 shows the relative importance of packaging characteristics for data processing, communications, and consumer applications. Figure 7 illustrates package and mounting technologies for advanced ASIC designs.

Table 2
Packaging Technology Requirements in the Data Processing Market

	Mainframe/ Supercomputer	Server	Workstation	Desktop/ Notebook PC	Personal Digital Assistant
Gate Count/ Memory Integration	400,000-3,000,000	100,000-500,000	200,000-1,500,000	50,000-100,000	2,000-300,000
Performance					
Core	150-300 MHz	66-150 MHz	66-150 MHz	66-100 MHz	1-70 MHz
I/O	150 MHz-1.2 GHz (actual: 800 MHz, serial transmission)	75-500 MHz (600 MHz, serial transmission)	66-500 MHz	66-500 MHz	33 MHz
Source Voltage					
Core	2.5V	≤1V/3.3V	1.8/2.5/3.3V	1.8V/3.3V	2.5V
I/O	≤1V/2.5V/3.3V	≤1V/3.3V/5V	≤1V/3.3V/5V	5V/3.3V	2.5V/3.3V
Pin Count	500-1,600	208-750	208-750	120-400	100-400
Package Requirements	FCBGA, multilayer PBGA	Multilayer PBGA, TBGA	Multilayer PBGA, TBGA	TBGA, PBGA, PQFP	LQFP, CSP

Source: Dataquest (March 1998)

Table 3
Packaging Technology Requirements in the Telecommunications Market

	Transmission	Switch	Networking	Wireless
Gate Count/ Memory Integration	600,000-1,200,000	100,000-400,000	100,000-200,000	2,000-50,000 Baseband
Performance				
Core	155 MHz	50-74 MHz	50 MHz	50-100 MHz
I/O	622 MHz-1.2 GHz	622 MHz-1.2 GHz	300 MHz	150 MHz
Source Voltage				
Core	3.3V	3.3V	3.3V	≤2.5V/3.3V
I/O	1V/3.3V	3.3V	1V/3.3V	≤2.5V/3.3V (1V core required in 2000)
Pin Count	225-527	225-650	100-500	100-225
Package Requirements	FCBGA, multilayer PBGA	Multilayer PBGA, TBGA	PQFP, CSP, PBGA	LQFP, CSP, module integration

Source: Dataquest (March 1998)

Environment of Attach Technology

Traditionally, suppliers have generated revenue by supplying customer-specific designs. However, to achieve high-density mounting at a lower cost, packages having area array terminals on the rear side, such as BGA and CSP, have emerged. Dataquest believes that the future package development should be based on the concept of reducing total system cost.

Packages and high-density printed circuit boards, including buildup substrates, will be offered by multiple suppliers. Buildup substrates with 100-micron wiring pitch have been introduced for bare die attach, intended for multichip modules (MCMs).

Table 4
Packaging Technology Requirements in the Consumer Market

	Broadcast	DVD	Digital TV	Digital Audio	Digital Video
Gate Count/ Memory Integration	10,000-100,000	50,000-1,000,000	10,000-150,000	10,000-100,000	100,000-1,000,000
Performance					
Core	20-33 MHz	27 MHz	27 MHz	33 MHz	18-25 MHz
I/O	33 MHz	51-81 MHz	33 MHz	33 MHz	25-50 MHz
Source Voltage					
Core	3.3V	2.5V/3.3V	2V/3.3V	2V/3.3V	≤2V/2.5V
I/O	3.3V	2.5V/3.3V	2V/3.3V	2V/3.3V	≤2V/2.5V
Pin Count	100-400	160-208	64-208	100-304	100-304
Package Requirements	PQFP	PQFP, CSP	PQFP	LQFP, CSP	LQFP, CSP

Source: Dataquest (March 1998)

Table 5
Market Requirements for High-Speed I/O

Application	Wide Path I/O	High-Speed Serial I/O
Data Processing		
Supercomputer/Networking	+++	++
Workstation/Server	++	+
Desktop/Notebook PC	+	-
Telecommunications		
Networking	+	-
Transmission	+	+++
Digital Video		
DVD, Digital Camcorder, Digital Still Camera	-	-

+++ = Critical
++ = Very important
+ = Important
- = Not important (no influence)
Source: Dataquest (March 1998)

Table 6
Performance Analysis of Package Technologies

Package Type	I/O Integration Level/Performance	Thermal Characteristics	Electrical Characteristics
Single Layer			
PLCC	5	5	5
PQFP (Copper Lead)	4	4	4
TAB in PQFP	4	4	4
LQFP/TQFP	3	3	3.5
MQUAD	4	1	3.5
TAB (TCP)	2	2-5	3
Two-Layer (Power/Ground Partially Reinforced Type)			
PBGA (OMPAC)	1-2	3	2-3
Two-Layer (Ground/Plain)			
TBGA	1	2-3	1-2
Two or More Layers (Ground/Power Plain)			
Multilayer PBGA	1	1	1
CPGA	2	1	2

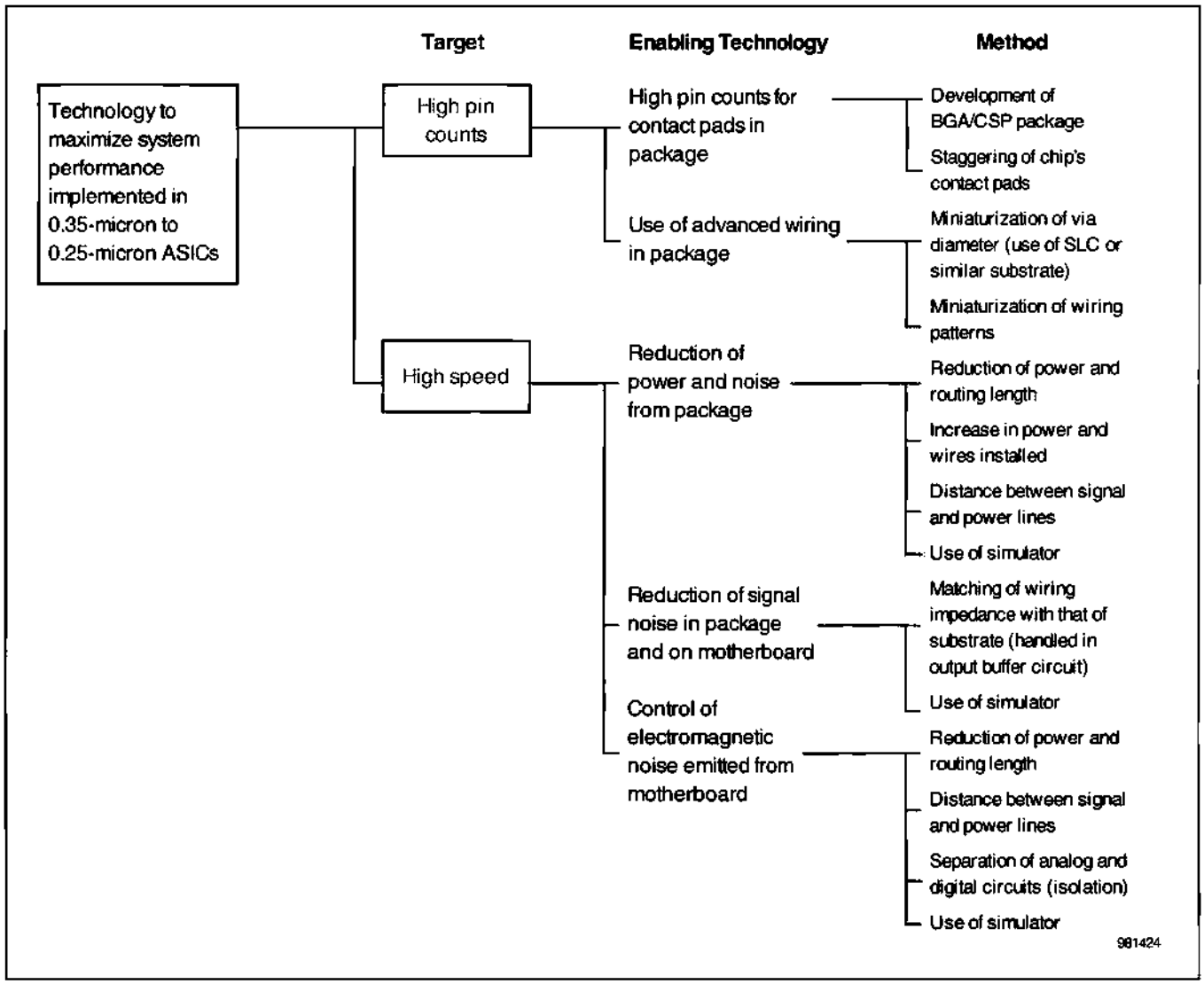
Note: Performance evaluation criteria: 5 = highest, 1 = lowest.
Source: Dataquest (March 1998)

Table 7
Performance Analysis of Packaging Technologies

Market Segments/ Applications	Pad Limited	Core Limited	Multipin	Big Die	Electrical Characteristics	Thermal Characteristics	Size
Data Processing							
Mainframe/Supercomputer	+++	-	+++	+	+++	+++	-
Server	++	-	++	-	+	++	-
Workstation	+++	-	++	-	+++	+++	+
Desktop/Notebook PC	++	-	-	-	-	-	+++
Telecommunications							
Transmission	-	++	+	++	+++	+++	-
Networking	+	-	-	-	+	+	+
Consumer							
Digital TV	+	-	+	+	+	+	++
DVD Decoder	-	++	+	+	+	+	+
DVD Encoder	-	+++	+	+++	+	++	+
Digital Camcorder	-	+	-	-	-	+	+++
Home Video Game	+++	+	+	-	+	++	+

+++ = Critical
++ = Very important
+ = Important
- = Not important (no influence)
Source: Dataquest (March 1998)

Figure 7
Package and Mounting Technologies for 0.35- to 0.25-Micron ASICs



Source: Dataquest (March 1998)

Technological Challenges for ASIC Packages

Increased function and integration at the system level, as well as miniaturization and lower power consumption, now require higher integration, higher speed, higher pin counts, and enhanced functions from ASIC products. The ASIC package domain has often been relatively neglected, compared to the process, library, and intellectual property core areas. However, system design specifications for ASIC products, packages, and attach technologies are becoming critical. Technical challenges for ASIC process and package designs include the following:

- Accurate analysis of stress produced in the fab process, such as oxidization and diffusion, as well as analysis of electrical characteristics of circuit devices that vary according to the degree of stress

- Thermal stress related to the complexity of multilayer plastic packages composed of multiple materials. The packaged device goes through many thermal processes, so it must be robust enough to withstand destruction of the composite materials by thermal stress—for example, destruction of a die by thermal stress, destruction of resin by thermal fatigue, and destruction of a passivation film. Also, increased use of smaller and thinner ASIC packages makes destruction by external forces at the time of mold separation and lead forming an important issue.

Given the diverse technological challenges, if the ASIC business is to change from the traditional custom production approach, ASIC vendors will have to establish standard procedures for package design and analysis that go beyond the realm of the traditional single-chip package.

Dataquest Perspective

In 1997, when 0.35-micron process technology became the mainstay, the integration level of LSIs was driven by finer geometries. SLI ASICs, led by cell-based ICs, increased demand for high-performance packages with smaller and thinner form factors and high reliability. This technology development demanded higher pin counts, higher heat emission, electrical characteristics that match the increase in I/O counts, lower power consumption, and higher speed. The traditional QFP and tape automated bonding-based lead frames and films were reaching their limits of pitch, heat emission, and electrical characteristics.

Packages with an external contact pitch of 0.4mm for miniaturization and higher-pin-count system ICs required a finer pattern. To meet higher-performance system requirements, new packages were developed, such as BGA and CSP, and new solder bump techniques progressed rapidly. CSP technology has overcome major obstacles, but many challenges remain for volume commercialization of CSPs.

In theory, direct chip attach to the substrate is the most effective means of maximizing performance of ASIC products. For this reason, many companies have been working with MCM designs. Nevertheless, the supply of bare die, especially for known good die, involves increased technical challenges, reliability issues, and additional test costs.

The development of an optimum ASIC package requires further understanding of system user requirements. ASIC vendors need to further analyze the needs of the entire application market and decide on the applicable technical solution for these products to ensure the optimum package design. Ultimately, this would guarantee a "true" SLI ASIC that would meet the user's needs.

To reduce package cost, ASIC vendors should employ a more flexible strategy, possibly involving an alliance with a subcontractor with a leading-edge package. Such a joint technology effort could be critical in meeting the shorter time to market required by customer cycles.

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Perspective

ASIC/SLI Worldwide

Market Analysis

The 1997 Worldwide Semiconductor Spending of 44 North American Companies Examined

Abstract: *The worldwide semiconductor spending of 44 North American companies is examined by application, device type, and region. These companies used an estimated $56 billion in semiconductors, representing 37 percent of the forecast total of $149 billion in semiconductors consumed worldwide in 1997. As well as providing company-specific information, this document also provides a representative picture of worldwide semiconductor application markets.*
By Xavier Pucel

Methodology

In this document, Dataquest analyzes the worldwide semiconductor spending activity of a selected list of 44 companies with North American headquarters. The companies surveyed for this report were classified in the following categories, with some companies involved in more than one:

- Personal computers (PCs) and additional motherboards: desktop/deskside and mobile computers
- Other computers: workstations, midrange computers, mainframes, and supercomputers
- Data storage: rigid disk, tape, floppy, and optical drives and RAID controllers
- Input/output devices: printers, monitors, terminals, scanners, mice, and keyboards, among others

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- Other data processing: dedicated systems (copiers, among others) and adapter cards
- Networking: LAN equipment (network interface cards, switches and hubs, and routers), WAN equipment, remote access, and modems
- Mobile communications: pagers, cellular phones, other portable terminals, and infrastructure equipment
- Other communications: central office public switch, public transmission equipment, PBX/KTS equipment, corded and cordless phones, answering machines, voice messaging equipment, automatic call distributors, interactive voice response, broadcast communications equipment, and other communications equipment not counted elsewhere
- Automotive electronics
- All other applications: consumer electronics, industrial and medical electronic equipment, and military/aerospace electronic equipment

The purchasing estimates were developed through a combination of direct surveys and semiconductor content modeling. Each company' spending reflects a combination of merchant and captive purchases, as well as purchases made on behalf of the company by contract manufacturers. Note that for the purposes of this report and for consistency with other Semiconductor Application Markets Worldwide reports, the definitions used were those detailed in the *Semiconductor Application Market Definitions Guide* (SAMM-WW-GU-9701, October 1997). To reduce the impact of double-counting, the semiconductor value of storage drives, monitors, and other peripherals was extracted from the value of semiconductors used in computers.

IBM Still Is No. 1

IBM again came out on top as the leading purchaser in the survey for 1997, just at it did in prior years, followed closely by Hewlett-Packard Company and Compaq Computer Corporation. Note that the top 10 companies are leading players in either the PC or communications segment, with the exception of Hughes Electronics Corporation, which used the majority of its total semiconductor consumption in automotive applications (Delco Electronics). The top 10 companies in Dataquest's sample accounted for 24 percent of the forecast 1997 $149 billion worldwide semiconductor market. The total sample of 44 North American companies accounted for an estimated $55.7 billion in chip purchases, representing 37 percent of the 1997 worldwide semiconductor market.

Tables 1 and 2 compare the sample's semiconductor purchases to the worldwide semiconductor market, and Figure 1 illustrates each company's total semiconductor purchases.

Table 1
The Sample's Worldwide Semiconductor Spending Compared to Worldwide Semiconductor Market by Semiconductor Device Type (Millions of Dollars)

	Volatile Memory	Nonvolatile Memory	Microcomponents and Logic	Standard Analog	Discrete and Opto	Total
Worldwide Market	26,689	6,157	73,874	22,762	20,181	149,663
Total Sample*	12,710	2,572	32,447	4,133	3,828	55,690
Sample's Share of Worldwide Market (%)	48	42	44	18	19	37

*Includes double-counting of contract manufacturers' totals
Source: Dataquest (February 1998)

Table 2
The Sample's Worldwide Semiconductor Spending Compared to Worldwide Semiconductor Market by Key Application Segment (Millions of Dollars)

	Data Processing	Communications	Automotive	All Others	Total
Worldwide Market	69,702	31,974	7,240	40,747	149,663
Total Sample*	34,777	13,082	2,245	5,586	55,690
Sample's Share of Worldwide Market (%)	50	41	31	14	37

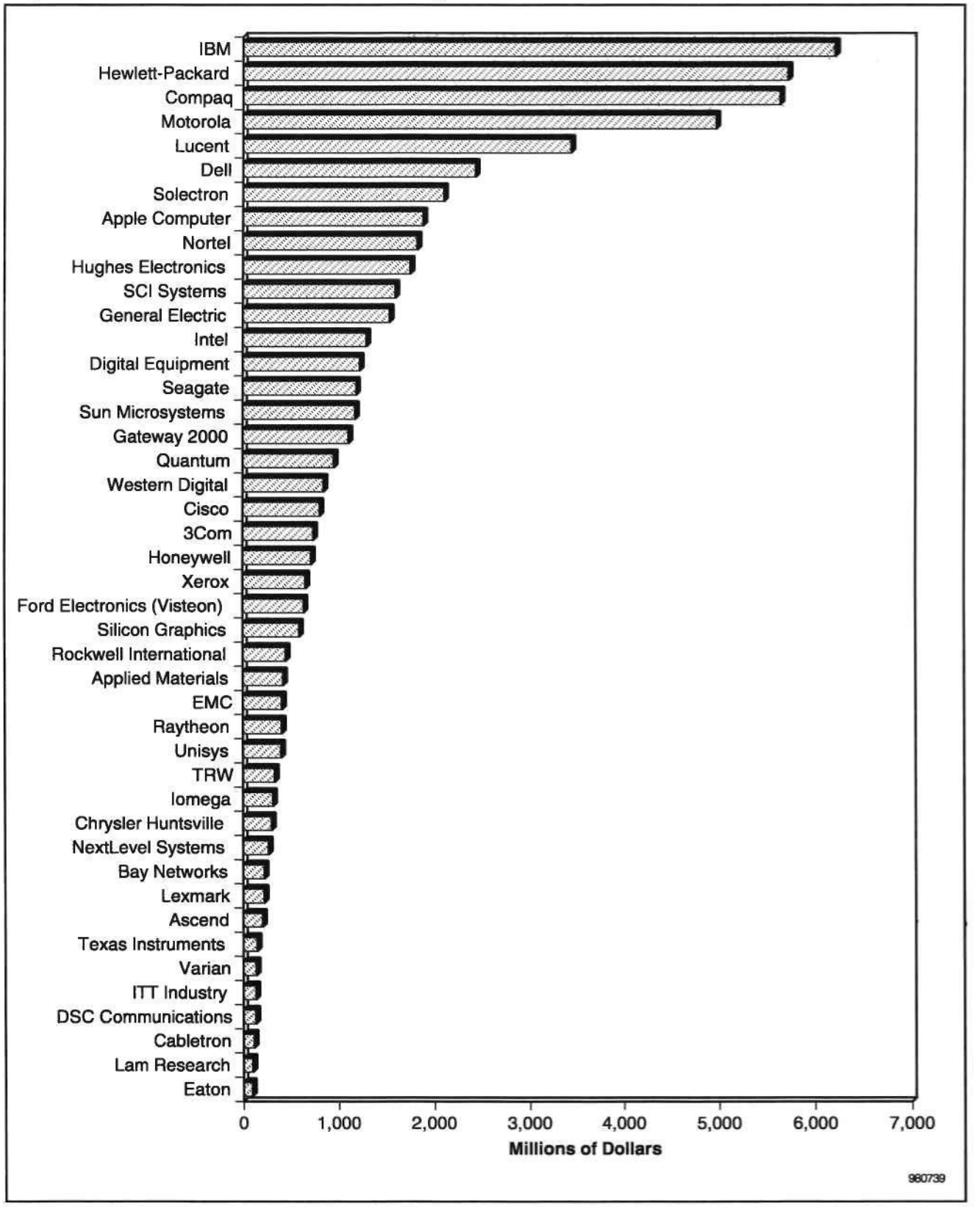
*Includes double-counting of contract manufacturers' totals
Source: Dataquest (February 1998)

Key Company Events In 1997

The following is a partial list of key acquisitions, mergers, and divestitures that occurred in 1997:

- 3Com Corporation acquired U.S. Robotics.
- AST Research was acquired by Samsung Electronics Company Ltd. and has been removed from Dataquest's survey of North American companies.
- Ascend Communications Inc. acquired Cascade Communications in June.
- Compaq acquired Tandem in July.
- Eaton Corporation sold its appliance controls business unit to U.K.-based Siebe plc in December.
- Ford Motor Company's Automotive Products Operation, a free-standing parts supplier, was renamed Visteon Corporation in September.
- General Instrument Corporation separated into three new public companies in July. The three companies are General Semiconductor, CommScope (coaxial and high-performance electronic cables), and NextLevel Systems. For the purpose of this survey, Dataquest considered NextLevel Systems only. NextLevel changed its name back to General Instrument as of February 2, 1998.
- GTE Corporation acquired BBN in September and created GTE Internetworking as a result of the merger.

Figure 1
Top North American Semiconductor Buyers



Source: Dataquest (February 1998)

- Hughes Electronics' automotive electronics business (Delco) was transferred to Delphi, another division of parent company General Motors Corporation in the last quarter of 1997. Also, Hughes' defense electronics business was merged with Raytheon Company, and Hughes-Avicom International (in-flight entertainment) was acquired by Rockwell International Corporation in the same time frame.
- Lucent Technologies' phone handset business was combined with Philips Electronics NV into a joint venture called Philips Consumer Communications in October. The product of the two companies' union designs, manufactures, and markets digital and analog cellular phones, corded and cordless phones, answering machines, screen phones, and pagers.
- Raytheon completed a merger with Hughes Defense and acquired Texas Instruments Inc.'s defense system business.
- Rockwell International dismantled its automotive business unit. The Driver Information Division was acquired by Magellan Corporation in the summer, and other divisions were spun off into an independent company called Meritor Automotive Inc. in October. Rockwell acquired Hughes-Avicom.
- Solectron Corporation acquired Force Computer at the end of 1996 and Ericsson Telecom AB's printed circuit board manufacturing operation in Sao Jose dos Campos, Brazil, in September.
- Texas Instruments sold its printer business to Genicom Corporation in 1996, its portable PC business unit to Acer Computer International Ltd., its telecom systems business to DSC Communications Corporation, its Multipoint System technology to Robert Bosch Corporation, and its defense systems business to Raytheon.

Review of OEM Semiconductor Spending

Not surprisingly, PCs were again the dominant application and accounted for 37 percent of the sample's aggregated worldwide semiconductor spending. Because non-PC companies were added to the survey to diversify the sample, this share has decreased compared to prior years' surveys (54 percent in 1995 sample and 46 percent in 1996 sample).

Table 3 presents total chip purchasing by OEMs, with the value allocated by application area, and Figure 2 illustrates the sample's aggregated worldwide semiconductor spending by key application area.

Overall, this year's survey results indicate an increase in spending on application-specific standard products (ASSPs) and slowing spending on volatile memory, microcomponents, and application-specific ICs (ASICs), compared to last year's survey results. Further analysis presented later will show that changes in the constitution of the sample (32 companies in 1996, 44 this year) are only accountable in part for the differences. Looking at certain industry groupings of companies can clarify the underlying trends that are driving these differences between the 1996 and 1997 semiconductor spending survey results.

Table 4 presents total chip purchasing by OEMs, with the value allocated by semiconductor device type, and Figure 3 illustrates the sample's aggregated worldwide semiconductor spending by semiconductor device type.

Table 3
Worldwide 1997 Estimated Value of Semiconductors Used by Top North American Companies, by Application Segment (Millions of Dollars)

	PCs and Additional Motherboards	Other Computer	Data Storage	Input/Output Devices	All Other Data Processing	Networking	Mobile Communications	All Other Communications	Automotive Electronics	All Other Applications	Company Total
Total Sample*	20,535	6,139	4,205	2,943	956	3,446	6,937	2,700	2,245	5,586	55,690
3Com	-	-	-	-	-	733	-	-	-	-	733
Apple Computer	1,736	-	-	148	-	-	-	-	-	-	1,884
Applied Materials	-	-	-	-	-	-	-	-	-	415	415
Ascend	-	-	-	-	-	200	-	-	-	-	200
Bay Networks	-	-	-	-	-	218	-	-	-	-	218
Cabletron	-	-	-	-	-	110	-	-	-	-	110
Chrysler/Acustar	-	-	-	-	-	-	-	-	294	-	294
Cisco	-	-	-	-	-	800	-	-	-	-	800
Compaq (Including Tandem)	5,049	255	-	244	-	85	-	-	-	-	5,633
Dell	2,282	82	-	69	-	-	-	-	-	-	2,432
Digital Equipment	694	469	-	32	-	31	-	-	-	-	1,226
DSC Communications	-	-	-	-	-	-	-	129	-	-	129
Eaton	-	-	-	-	-	-	-	-	54	36	90
EMC	-	-	402	-	-	-	-	-	-	-	402
Ford Electronics (Visteon)	-	-	-	-	-	-	-	-	632	-	632
Gateway 2000	1,039	-	-	66	-	-	-	-	-	-	1,105
General Electric	-	-	-	-	-	-	-	-	-	1,542	1,542
Honeywell	-	-	-	-	-	-	-	-	-	710	710
Hewlett-Packard	2,222	1,254	21	1,672	-	26	-	-	-	522	5,716
Hughes Electronics	-	-	-	-	-	15	183	311	920	326	1,754
IBM	3,600	1,733	356	218	167	129	-	5	-	-	6,208
Intel	1,232	-	-	-	-	64	-	-	-	-	1,296
Iomega	-	-	308	-	-	-	-	-	-	-	308
ITT Industry	-	-	-	-	-	-	-	-	82	48	130
Lam Research	-	-	-	-	-	-	-	-	-	96	96
Lexmark	-	-	-	216	-	-	-	-	-	-	216
Lucent	-	-	-	-	-	-	2,190	1,241	-	-	3,431
Motorola	1,056	-	-	-	-	112	3,640	-	105	54	4,967
NextLevel Systems	-	-	-	-	-	-	-	78	-	184	261
Nortel	-	-	-	-	-	139	924	762	-	-	1,825
Quantum	-	-	950	-	-	-	-	-	-	-	950
Raytheon	-	-	-	-	-	-	-	-	-	400	400

Table 3 (Continued)
Worldwide 1997 Estimated Value of Semiconductors Used by Top North American Companies, by Application Segment (Millions of Dollars)

	PCs and Additional Motherboards	Other Computer	Data Storage	Input/Output Devices	All Other Data Processing	Networking	Mobile Communications	All Other Communications	Automotive Electronics	All Other Applications	Company Total
Rockwell International	-	-	-	-	-	-	-	6	-	436	442
SCI Systems	1,171	-	77	25	-	154	-	-	-	174	1,601
Seagate	-	-	1,187	-	-	-	-	-	-	-	1,187
Silicon Graphics	-	572	-	11	-	-	-	-	-	-	582
Solectron	231	483	63	189	-	630	-	168	-	336	2,100
Sun Microsystems	-	1,138	-	38	-	-	-	-	-	-	1,175
Texas Instruments	-	-	-	-	139	-	-	-	5	-	144
TRW	-	-	-	-	-	-	-	-	153	175	328
Unisys	222	155	-	15	-	-	-	-	-	-	393
Varian	-	-	-	-	-	-	-	-	-	133	133
Western Digital	-	-	841	-	-	-	-	-	-	-	841
Xerox	-	-	-	-	650	-	-	-	-	-	650

*Includes double-counting of contract manufacturers' totals
Source: Dataquest (February 1998)

Table 4
Worldwide 1997 Estimated Value of Semiconductors Used by Top North American Companies, by Device Type (Millions of Dollars)

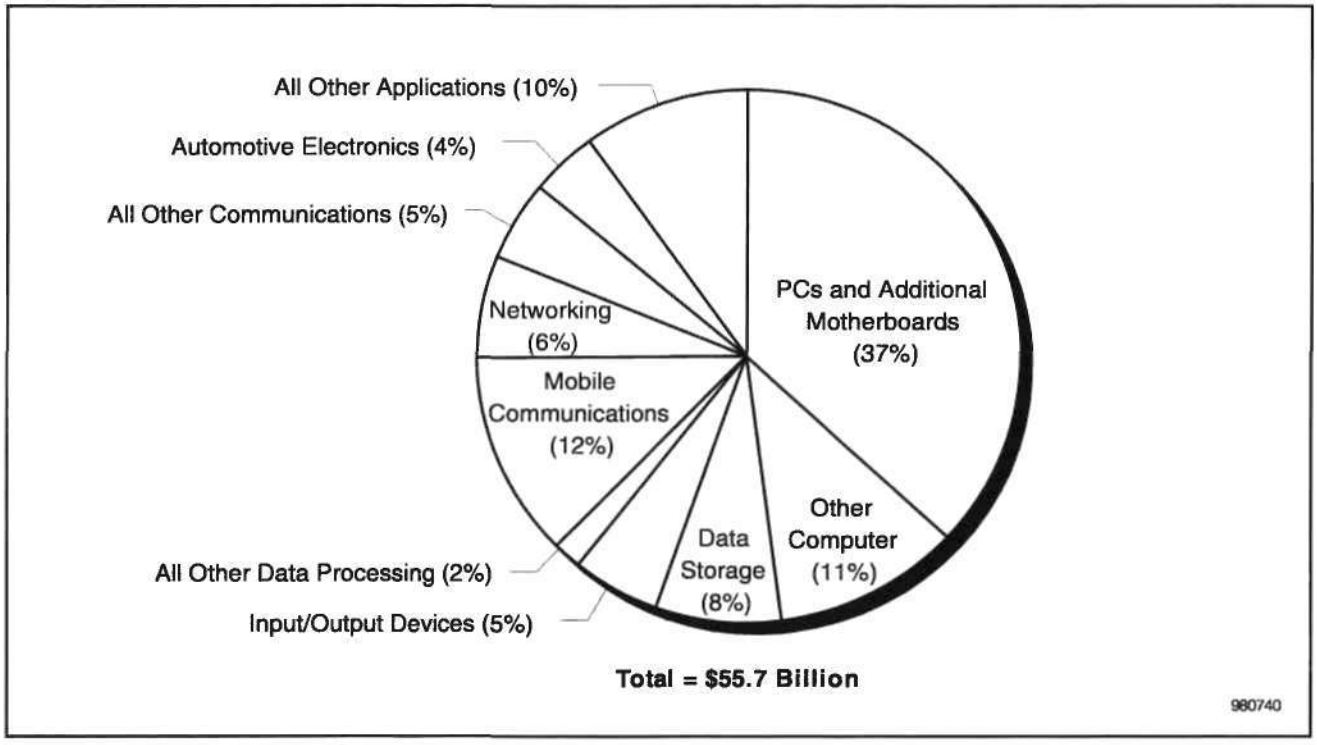
	Volatile Memory	Nonvolatile Memory	MPU/MCU/DSP	ASIC	ASSP	Standard Logic	Standard Analog	Discrete and Opto	Total
Total Sample*	12,710	2,572	13,860	9,379	8,293	916	4,133	3,828	55,690
3Com	42	55	67	250	232	25	45	19	733
Apple Computer	699	50	663	104	166	21	94	89	1,884
Applied Materials	39	6	115	47	13	2	85	110	415
Ascend	16	10	18	2	140	10	2	2	200
Bay Networks	29	30	41	52	55	4	4	2	218
Cabletron	15	13	14	23	36	3	4	2	110
Chrysler Huntsville	0	17	98	108	0	6	32	33	294
Cisco	216	88	136	224	64	17	39	16	800
Compaq	2,108	100	1,972	328	534	62	265	262	5,633
Dell	932	31	867	34	314	25	112	116	2,432
Digital Equipment	423	37	558	49	-	110	12	37	1,226
DSC Communications	18	3	7	22	42	1	6	29	129
Eaton	3	4	28	22	3	1	13	16	90
EMC	29	11	38	115	180	1	20	9	402
Ford Electronics (Visteon)	1	36	210	232	0	14	68	70	632
Gateway 2000	415	23	391	19	137	12	54	53	1,105
General Electric	160	23	323	114	142	75	351	353	1,542
Hewlett-Packard	1,641	493	1,737	541	545	67	400	291	5,716
Honeywell	70	10	188	47	58	4	147	186	710
Hughes Electronics	70	98	334	628	212	18	161	232	1,754
IBM	2,084	117	2,036	1,313	385	65	146	62	6,208
Intel	482	10	446	73	148	15	58	64	1,296
Iomega	19	16	73	55	121	3	17	3	308
ITT Industry	6	6	36	34	5	2	19	21	130
Lam Research	9	1	26	12	2	1	20	25	96
Lexmark	29	60	52	38	10	4	21	2	216

Table 4 (Continued)
Worldwide 1997 Estimated Value of Semiconductors Used by Top North American Companies, by Device Type (Millions of Dollars)

	Volatile Memory	Nonvolatile Memory	MPU/MCU/DSP	ASIC	ASSP	Standard Logic	Standard Analog	Discrete and Opto	Total
Lucent	138	282	164	880	1,249	27	369	322	3,431
Motorola	515	371	533	1,114	1,344	21	686	383	4,967
NextLevel Systems	25	7	41	31	44	14	51	48	261
Nortel	101	118	132	436	646	25	179	188	1,825
Quantum	58	39	121	382	287	4	48	10	950
Raytheon	49	7	84	31	39	3	87	101	400
Rockwell International	42	6	117	50	17	2	90	115	442
SCI Systems	498	32	493	170	171	21	107	109	1,601
Seagate	74	54	209	471	296	8	63	11	1,187
Silicon Graphics	248	5	160	108	15	3	21	22	582
Solectron	504	126	420	336	420	168	63	63	2,100
Sun Microsystems	489	16	325	250	23	8	33	32	1,175
Texas Instruments	10	1	54	15	24	2	14	24	144
TRW	23	12	84	71	18	5	55	60	328
Unisys	126	7	150	54	23	5	14	14	393
Varian	12	2	37	9	11	1	27	35	133
Western Digital	77	48	145	446	108	5	7	5	841
Xerox	163	91	117	39	13	26	20	182	650

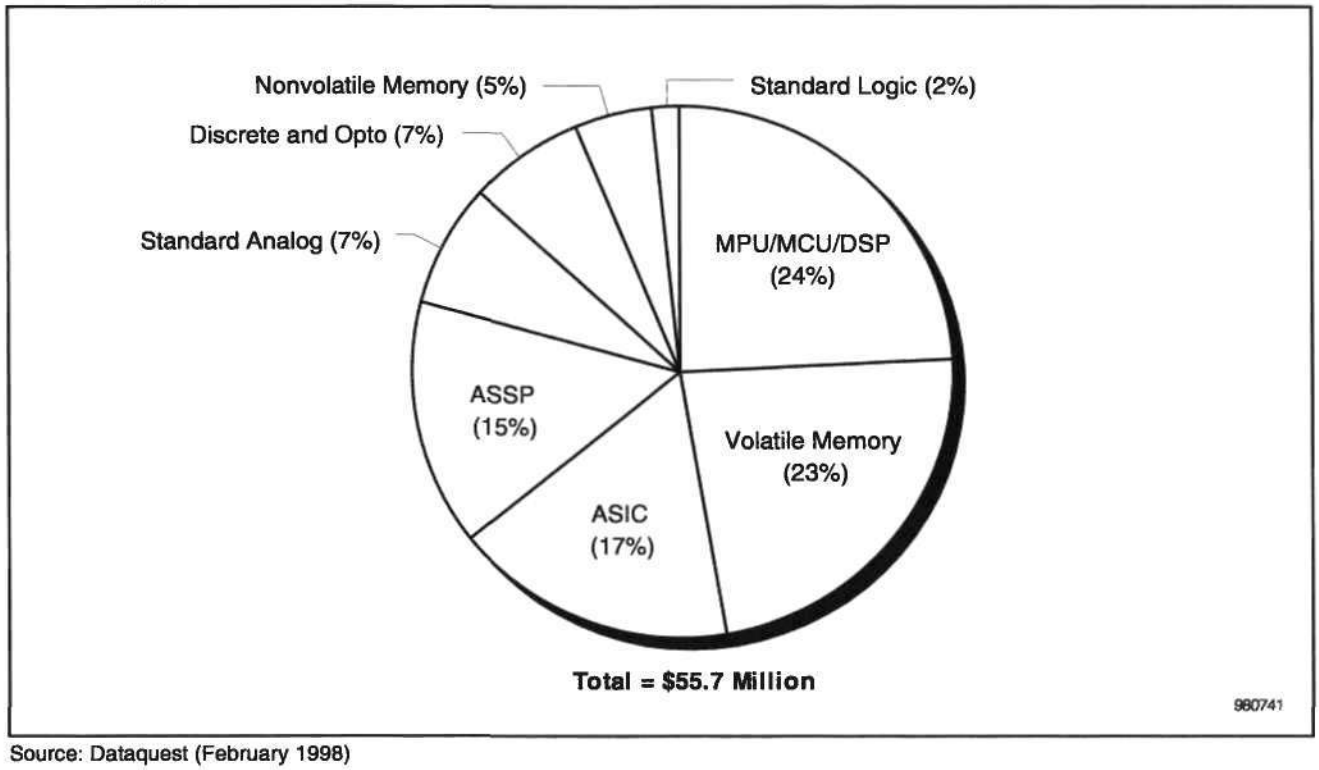
*Includes double-counting of contract manufacturers' totals
Source: Dataquest (February 1998)

Figure 2
The Sample's Aggregated Worldwide Semiconductor Spending, by Application Segment



Source: Dataquest (February 1998)

Figure 3
The Sample's Aggregated Worldwide Semiconductor Spending, by Semiconductor Device Type



Source: Dataquest (February 1998)

The Sample's Spending on Memory

The overall sample's share of nonvolatile memory spending remained the same as last year's (4.6 percent). However, volatile memory is a different story. Volatile memory represented 28 percent of spending by last year's sample, but only 23 percent this year. As shown in Table 5, the volatile memory spending share declined primarily for companies involved in the "all other applications" segment, which mainly includes automotive electronics and industrial controls. This actually makes sense. Computer and communications companies are taking advantage of the DRAM price decline and are buying more megabytes per system to improve their system performance. In other applications, more memory does not necessarily add up to better products, so companies are buying the same amount of memory at a lower price, which accounts for a more drastic reduction of memory spending share.

The Sample's Spending on Microcomponents

The overall sample's share of microcomponents spending (microprocessors, microcontrollers, and digital signal processors) decreased from 30 percent of the 1996 sample's total to 25 percent of the 1997 sample's. As Table 6 shows, communications companies are spending much less on these devices (most likely because of the benefits of ASSPs, as discussed later), but their importance is growing among companies involved in "other" areas. Most likely, the components are finding new homes in automotive electronics and embedded industrial control applications. Other research also shows that video games and Internet appliances, in particular, continued to drive the embedded MPU RISC market. Also, MCUs and DSPs continue to find new homes in every conceivable electronic product.

The microcomponents spending of the sampled computer companies seems rather stable, and this came as a bit of a surprise. Other research showed that the average selling prices (ASPs) of MPUs used in PCs have risen as the MPU absorbed other system functions, and growth of the PC-based workstation and server system markets is also fueling the need for an increasing number of more expensive MPUs.

Table 5
Volatile Memory Spending for Computer, Communications, and Other Companies (Percentage of Total Subgroup's Semiconductor Spending)

	1996	1997	Change in Share
Computer Companies	38	37	-1
Communications Companies	10	9	-1
All Others	21	17	-4

Source: Dataquest (February 1998)

Table 6
Microcomponents Spending for Computer, Communications, and Other Companies (Percentage of Total Subgroup's Semiconductor Spending)

	1996	1997	Change in Share
Computer Companies	36	34	-2
Communications Companies	25	9	-16
All Others	22	24	3

Source: Dataquest (February 1998)

The Sample's Spending on ASICs and ASSPs

The overall sample's ASIC spending share decreased slightly, from 18 percent of the 1996 sample's total spending to 17 percent of the 1997 sample's. However, the ASSP share increased to 15 percent in 1997 from 9 percent in 1996. Table 7 shows that, although computer companies spent the same amount of money (as a percentage of the their total semiconductor spending) in 1997 as in 1996, ASICs were becoming less important for other companies but still represented a major portion of the spending. In computer applications, the fundamental technology enabling the rise of digital multimedia is highly integrated silicon based on ASIC methodology. In other areas, low volumes and factors such as cost, form factor, power consumption, and lack of standards have been major driving forces for ASIC technology. In recent years, many new high-volume applications have fueled use of ASICs, including LAN switches, satellite links, high-performance workstations, and network-centric client/servers. In the automotive electronics industry, various functions implemented on several ASICs are being integrated onto single or dual ASIC processor core chips. ASICs still represent a big portion of the total semiconductor spending of companies involved in these businesses, but there is a growing interest in ASSPs. Table 8 shows that ASSPs are becoming key devices in many applications, in particular, communications equipment. Volume is key for ASSPs—the volume used must be large enough to justify their existence.

Table 7
ASIC Spending for Computer, Communications, and Other Companies (Percentage of Total Subgroup's Semiconductor Spending)

	1996	1997	Change in Share
Computer Companies	11	11	0
Communications Companies	29	24	-5
All Others	25	19	-6

Source: Dataquest (February 1998)

Table 8
ASSP Spending for Computer, Communications, and Other Companies (Percentage of Total Subgroup's Semiconductor Spending)

	1996	1997	Change in Share
Computer Companies	9	8	-1
Communications Companies	10	31	21
All Others	9	15	6

Source: Dataquest (February 1998)

The following further observations can be made from Table 9, which outlines companies' semiconductor consumption by application and by semiconductor device type:

- Volatile memory and MCUs/MPUs represent the largest portion of the semiconductor spending of companies involved primarily in the data processing segment (that is, computers, data storage, and input/output devices).
- Companies involved primarily in the communications segment (networking, mobile, and other communications) purchased mostly ASIC and ASSP devices.
- Automotive electronics, industrial/medical equipment, and military/aerospace electronics companies seem to have more balanced spending, skewed primarily toward analog and discrete devices.

Company Spending by Region

Table 10 presents the regional breakdown of chip consumption. As with last year's results, Dataquest found that about half the chips purchased by these companies were actually consumed in America, with the majority of the remainder split between Europe and Asia/Pacific. PC companies tend to do the final configuration and assembling close to the end market. Note that Dataquest's definitions of the world's regions was updated in 1996; in particular, the Rest of World (ROW) region was divided and merged with other regions.

Locations of Companies' Key Sites

Table 11 shows major company R&D (or primary design house), chip procurement, and manufacturing sites. For a large majority, purchasing and design activity occurs in the United States. Some purchasing of standard components, such as memories and standard logic, may be done near the regional market where the manufacturing takes place.

Table 9
Companies' Semiconductor Use by Main Application Segment and Main Semiconductor Category (Percentage of Total Dollar Value)

	Application Segment			Semiconductor Category			
	Data Processing	Communications	All Other Applications	Memory	Microcomponents	Logic	Analog, Discrete, and Others
3Com	0	100	0	13	9	69	9
Apple Computer	100	0	0	40	35	15	10
Applied Materials	0	0	100	11	28	15	47
Ascend	0	100	0	13	9	76	2
Bay Networks	0	100	0	27	19	51	3
Cabletron	0	100	0	26	13	56	5
Chrysler/Acustar	0	0	100	6	33	39	22
Cisco	0	100	0	38	17	38	7
Compaq (Including Tandem)	98	2	0	39	35	16	9
Dell	100	0	0	40	36	15	9
Digital Equipment	97	3	0	38	46	13	4
DSC Communications	0	100	0	17	5	51	27
Eaton	0	0	100	8	31	29	32
EMC	100	0	0	10	9	74	7
Ford Electronics (Visteon)	0	0	100	6	33	39	22
Gateway 2000	100	0	0	40	35	15	10
General Electric	0	0	100	12	21	21	46
Honeywell	0	0	100	11	26	15	47
Hewlett-Packard	90	0	9	37	30	20	12
Hughes Electronics	0	29	71	10	19	49	22
IBM	98	2	0	35	33	28	3
Intel	95	5	0	38	34	18	9
Iomega	100	0	0	12	24	58	7
ITT Industries	0	0	100	9	28	32	31
Lam Research	0	0	100	11	28	15	47
Lexmark	100	0	0	41	24	24	11

Table 9 (Continued)
Companies' Semiconductor Use by Main Application Segment and Main Semiconductor Category (Percentage of Total Dollar Value)

	Application Segment			Semiconductor Category			
	Data Processing	Communications	All Other Applications	Memory	Microcomponents	Logic	Analog, Discrete, and Others
Lucent	0	100	0	12	5	63	20
Motorola	21	76	3	18	11	50	22
NextLevel Systems	0	30	70	12	16	34	38
Nortel	0	100	0	12	7	61	20
Quantum	100	0	0	10	13	71	6
Raytheon	0	0	100	14	21	18	47
Rockwell International	0	1	99	11	27	16	47
SCI Systems	80	10	11	33	31	23	13
Seagate	100	0	0	11	18	65	6
Silicon Graphics	100	0	0	44	27	22	7
Solectron	46	38	16	30	20	44	6
Sun Microsystems	100	0	0	43	28	24	6
Texas Instruments	97	0	3	8	38	28	27
TRW	0	0	100	11	26	28	35
Unisys	100	0	0	34	38	21	7
Varian	0	0	100	11	28	15	47
Western Digital	100	0	0	15	17	67	1
Xerox	100	0	0	39	18	12	31

Source: Dataquest (February 1998)

Table 10
Worldwide 1997 Estimated Value of Semiconductors Used by Top North American Companies, by Geographic Area (Millions of Dollars)

	Americas	Japan	Europe	Asia/Pacific	Worldwide Total
3Com	513	-	110	110	733
Apple Computer	817	-	399	668	1,884
Applied Materials	207	83	54	71	415
Ascend	170	20	-	10	200
Bay Networks	174	-	-	44	218
Cabletron	66	-	44	-	110
Chrysler/Acustar	147	-	147	-	294
Cisco	800	-	-	-	800
Compaq (Including Tandem)	2,253	-	1,690	1,690	5,633
Dell	454	-	368	405	1,226
Digital Equipment	851	-	851	730	2,432
DSC Communications	52	-	52	26	129
Eaton	32	7	37	14	90
EMC	241	-	161	-	402
Ford Electronics (Visteon)	461	-	171	-	632
Gateway 2000	937	-	50	118	1,105
General Electric	617	77	386	463	1,542
Hewlett-Packard	3,703	236	959	818	5,716
Honeywell	355	-	156	199	710
Hughes Electronics	1,662	-	37	55	1,754
IBM	3,476	993	1,552	186	6,208
Intel	729	-	249	318	1,296
Iomega	-	-	-	308	308
ITT Industry	78	-	26	26	130
Lam Research	96	-	-	-	96
Lexmark	123	-	54	39	216
Lucent	2,573	103	206	549	3,431
Motorola	1,893	-	2,192	883	4,967
NextLevel Systems	261	-	-	-	261
Nortel	1,007	-	197	620	1,825
Quantum	95	190	190	475	950
Raytheon	280	20	48	52	400
Rockwell International	309	-	88	44	442
SCI Systems	960	-	320	320	1,601
Seagate	59	-	178	950	1,187
Silicon Graphics	349	-	233	-	582
Solectron	1,428	-	399	273	2,100
Sun Microsystems	1,022	-	153	-	1,175
Texas Instruments	106	13	10	14	144
TRW	246	-	82	-	328
Unisys	275	-	118	-	393
Varian	53	13	40	27	133
Western Digital	-	-	-	841	841
Xerox	228	325	98	-	650
Total Sample	**30,162**	**2,080**	**12,104**	**11,344**	**55,690**

Source: Dataquest (February 1998)

Table 11
Company Purchasing, Design, and Manufacturing Locations

Company	Site Location	Site Activity
3Com	Santa Clara, CA	Central design, procurement, and board assembly
	Grass Valley, CA	Board assembly
	San Diego, CA	Board assembly
	Salt Lake City, UT	Board assembly
	Chicago, IL	Board assembly
	Skokie, IL	Design and board assembly
	Boxborough, MA	Design and final assembly
	Dublin, Ireland	Board assembly
	Tel Aviv, Israel	Design and board assembly
	Singapore	Board assembly (networking products)
Apple Computer	Cupertino, CA	Central PC design and procurement (strategic)
	Singapore	Board assembly (PCs) and procurement
	Cork, Ireland	Board assembly (PCs) and procurement
	Sacramento, CA	Board assembly (PCs) and procurement
Ascend Communications	Mountain View, CA	Design (WAN)
	Calabasas, CA	Design (DSL)
	Alameda, CA	Design, procurement, and board assembly (modems, WAN)
	Tinton Falls, NJ	Design (PIPE)
	Minneapolis, MN	Design (routers)
	Wallingford, CT	Design (frame relay)
	Littleton, MA	Design, procurement, and board assembly (ATM, frame relay)
Applied Materials	Santa Clara, CA	Design, procurement and board assembly
	Austin, TX	Procurement and board assembly
	Horsham, U.K.	Design procurement and board assembly
	Tel Aviv, Israel	Design procurement and board assembly
	Chiba, Japan	Design procurement and board assembly
	Chungnam, Korea	Board assembly
	Hsinchu, Taiwan	Design procurement and board assembly
Bay Networks	Santa Clara, CA	Board assembly (networking products)
	Billerica, MA	Board assembly (networking products)
	Limerick, Ireland (being built)	Board assembly (networking products)
	Valbonne, France	Board assembly (networking products)
Cabletron	Limerick, Ireland	Board assembly (networking products)
	Ironton, OH	Board assembly (networking products)
	Rochester, NH	Board assembly (networking products)
Chrysler/Acustar	Huntsville, AL	Design, procurement, and board assembly

Table 11 (Continued)
Company Purchasing, Design, and Manufacturing Locations

Company	Site Location	Site Activity
Cisco	San Jose, CA	Central procurement, internetworking design and production
	Raleigh, NC	Internetworking design
	Chelmsford, MA	Internetworking and ATM high end product design
Compaq	Houston, TX	Central design, procurement, and board assembly
	Singapore	Procurement and board assembly
	Erskine, U.K.	Procurement and board assembly
	Sao Paulo, Brazil	Board assembly
	Shenzen, China	Board assembly
Dell	Penang, Malaysia	Board assembly for PCs
	Limerick, Ireland	Board assembly for PCs
	Austin, TX	Design, procurement, and board assembly
Digital Equipment	Maynard, MA	Design
	Marlborough, MA	Central procurement management and design
	Salem, NH	Board assembly
	Kanata, Ontario, Canada	Procurement and board assembly
	Ayr, U.K.	Procurement and board assembly (small to midrange computers)
	Taipei, Taiwan	Design, procurement, and board assembly
	Singapore	Procurement and board assembly
DSC Communications	Plano, TX	Board assembly
	Petaluma, CA	Board assembly
	San Jose, Costa Rica	Board assembly
	Aguadilla, Puerto Rico	Board assembly
	Copenhagen, Denmark	Board assembly
	Coventry, England, U.K.	Board assembly
	Drogheda, Ireland	Board assembly
	Feltham, England, U.K.	Board assembly
	New Delhi, India	Board assembly
Eaton	Cleveland, OH	Design
	Southfield, MI	Design
	Milwaukee, WI	Design
	Peabody, MA	Board assembly
	Rochelle, IL	Board assembly (automotive controls)
	Winamac and Hamilton, IN	Board assembly (automotive controls)
	Three Rivers and Rochester Hills, MI	Board assembly (automotive controls)
	Sanford, NC	Board assembly (automotive controls)

Table 11 (Continued)
Company Purchasing, Design, and Manufacturing Locations

Company	Site Location	Site Activity
	Wauwatosa, WI	Board assembly (automotive controls)
	St. Thomas, Ontario, Canada	Board assembly (automotive controls)
	Matamoros, Mexico	Board assembly (automotive controls)
	Zagreb, Croatia	Board assembly (automotive controls)
	Langenlonsheim, Germany	Board assembly (automotive controls)
	Monte Carlo, Monaco	Board assembly (automotive controls)
	Gdansk, Poland	Board assembly (automotive controls)
	Barcelona, Spain	Board assembly (automotive controls)
	Montfoort, Netherlands	Board assembly (automotive controls)
	Beverly, MA	Board assembly (semiconductor manufacturing equipment)
	Rockville, MD	Board assembly (semiconductor manufacturing equipment)
	Austin, TX	Board assembly (semiconductor manufacturing equipment)
	Kyunggi-do, Korea	Board assembly
	Toyo, Japan	Board assembly
	Shandong, China	Board assembly
EMC	Milford, MA	Board assembly
	Franklin, MA	Board assembly
	Cork, Ireland	Board assembly
Ford Motor Company	Dearborn, MI	Central procurement and design
	Markham, Ontario, Canada	Board assembly of instrumentation electronics/ air bags
	Sao Paulo, Brazil	Procurement; board assembly (audio, power-train)
	Cadiz, Spain	Board assembly (engine control and ABS electronics)
	Basildon, U.K.	Board assembly (audio products and selected instrumentation/powertrain)
	North Penn, PA	Board assembly (ABS, engine control modules)
	Altec, Mexico	Board assembly (radios, ABS electronics, instrumentation)
	Palmella, Portugal	Board assembly (audio products, instrumentation, air bags)
Gateway 2000	North Sioux City, SD	Board assembly (PCs)
	Salt Lake City, UT	Board assembly (PCs)
	Hampton, VA	Board assembly (PCs)
	Dublin, Ireland	Board assembly (PCs)
	Malacca, Malaysia	Board assembly (PCs)

Table 11 (Continued)
Company Purchasing, Design, and Manufacturing Locations

Company	Site Location	Site Activity
GE	250 manufacturing plants in 26 countries	-
Hewlett-Packard	Palo Alto, CA	Central procurement, design (general, medical)
	Boise, ID	Design, procurement, board assembly (printers)
	Camas, WA	Design, procurement, board assembly (printers)
	Covallis, OR	Design, procurement, board assembly (computers/handhelds)
	Cupertino, CA	Design (computers)
	Santa Clara, CA	Design and board assembly (test and measurement)
	Colorado Springs, CO	Design and board assembly (test and measurement)
	Ft. Collins, CO	Design and board assembly (computers)
	Chelmsford, U.K.	Design (computers)
	Grenoble, France	Design, procurement (PCs)
	Lyon, France	Board assembly (PCs)
	Boblingen, Germany	Board assembly (computer)
	South Queensferry, U.K.	Board assembly (test and measurement)
	Bristol, U.K.	Board assembly (disk drives)
	Singapore	Board assembly
	Aquadilla, Puerto Rico	Board assembly
Honeywell	Minneapolis, MN	Design
	Phoenix, AZ	Design
	Clearwater, FL	Board assembly
	Freeport, IL	Board assembly
	Schoenaich, Germany	Board assembly (building control products)
	Tianjin, China	Board assembly
Hughes Electronics Corporation	Malibu, CA	Design
	El Segundo, CA	Design and board assembly (satellite products)
	Germantown, MD	Design, procurement, and board assembly (networking products)
	San Diego, CA	Design, procurement, and board assembly (satellite and mobile radio products)
Hughes—Delco Electronics	Kokomo, IN	Central procurement, design and board assembly (engine control and SIR)
	Flint, MI	Design and board assembly (instrument panels)
	Milwaukee, WI	Board assembly
	Torrance, CA	Design and board assembly
	Tucson, AZ	Design and board assembly (microwave-radar object detection)
	Singapore	Design and board assembly (radios)

Table 11 (Continued)
Company Purchasing, Design, and Manufacturing Locations

Company	Site Location	Site Activity
	Matamoros and Reynosa, Mexico	Board assembly (radio, ABS, SIR)
	Liverpool, U.K.	Design and board assembly (engine control and instrument panels)
IBM	Fishkill, NY	Electronic component procurement, global contracting, and PC company procurement
	Bordeaux, France	Procurement
	Lagaude, France	Procurement, design, and board assembly (networking products)
	Charlotte, NC	Design, procurement, and board and product assembly
	Raleigh, NC	Design, procurement, and assembly (PCs and networking products)
	Rochester, MN	Design, procurement, and board assembly (midrange systems)
	Austin, TX	Design, procurement, and assembly (workstations, servers)
	San Jose, CA	Design, procurement, and assembly (storage systems)
	Poughkeepsie, NY	Design, procurement, and board assembly (mainframe systems)
	Endicott, NY	Design, procurement, and assembly (large range systems)
	Hopewell Junction, NY	Design and manufacture microcomponents
	Burlington, VT	Design and manufacture microcomponents
	Boulder, CO	Design, procurement, and assembly (printers)
	Greenock, U.K.	Design, procurement, and board assembly
	Vimercate, Italy	Board assembly
	Fujisawa, Japan	Procurement, board assembly (storage systems and PCs)
	Kvant, Russia	Board assembly (PCs)
	Mainz, Germany	Design, purchasing, board assembly (storage systems)
	Szekesfahervar, Hungary	Board assembly (PC disk drives)
Intel	Chandler AZ	Design and manufacturing (fab); board assembly (PC)
	Santa Clara, CA	Design, procurement and board assembly (PC)
	Beaverton, OR	Design and manufacturing (fab); procurement and board assembly (PC)
	Rio Rancho NM	Fab
	Leixlip, Ireland	Procurement and board assembly (PC)
	Jerusalem, Israel	Fab
	Kulim, Malaysia	Design and board assembly (PC)
	Manila, Philippines	Board assembly (PC)

Table 11 (Continued)
Company Purchasing, Design, and Manufacturing Locations

Company	Site Location	Site Activity
	Las Piedras, Puerto Rico	Board assembly (PC)
Iomega	Roy, Utah	Design and procurement
	Penang, Malaysia	Board assembly (storage drives)
ITT Industries	Auburn Hills, MI	Design
	Asheville, NC	Board assembly (automotive products)
	Kettering, OH	Board assembly (automotive products)
	Frankfurt, Germany	Board assembly (automotive products)
	Shanghai, China	Board assembly (automotive products)
Lam Research Corporation	Fremont, CA	Design and board assembly
	San Jose, CA	Design and board assembly
	Wilmington, MA	Design and board assembly
Lexmark International	Lexington, KY	Design and board assembly (printers)
	Boulder, CO	Board assembly (printers)
	Juarez, Mexico	Board assembly (printers)
	Rosyth, Scotland	Board assembly (printers)
	Orleans, France	Board assembly (printers)
	Sydney, Australia	Board assembly (printers)
Lucent Technologies	Allentown, PA	Central procurement
	Murray Hill, NJ	Central design (AT&T Bell Labs)
	Dayton, OH	Procurement
	Wichita, KS	Procurement, design, and board assembly
	Richmond, VA	Board assembly of network systems
	Morristown, NJ	Board assembly of network systems
	San Diego, CA	Design and board assembly of computers
	Largo, FL	Design and board assembly of modems
	West Columbia, SC	Design and board assembly of PCs and workstations
	Duluth, GA	Design and board assembly of retail systems
	Pathum Thani, Thailand	Board assembly of corded telephones
	Singapore	Board assembly of corded telephones
	Oiso, Japan	Design and board assembly of retail systems
	Indonesia	Board assembly of corded telephones
	Guadalajara, Mexico	Board assembly of answering machines
	Augsburg, Germany	Board assembly of computers
	Donegal, Ireland	Board assembly of network systems
Motorola	Schaumburg, IL	PC card assembly
		Analog and digital two-way voice and data radio systems

Table 11 (Continued)
Company Purchasing, Design, and Manufacturing Locations

Company	Site Location	Site Activity
	McHenry, IL	Analog cellular infrastructure equipment assembly
	Arlington Heights, IL	Radio base station systems
	Libertyville, IL	Cellular telephones
	Northbrook, IL	Design and board assembly (automotive products)
	Dearborn, MI	Board assembly (automotive products)
	Rochester Hills, MI	Board assembly (automotive products)
	Elma, NY	Board assembly (automotive products)
	Seguin, TX	Design and board assembly (automotive products)
	Fort Worth, TX	Radio and Personal Handyphone base station equipment
	Austin, TX	Wafer fab
	Tempe, AZ	PowerPC MPU-based control boards
	Huntsville, AL	PC cards and transmission products assembly
	Lawrenceville, GA	Portable energy systems (batteries and chargers)
	Fort Lauderdale, FL	Portable energy systems (batteries and chargers)
	Boynton Beach, FL	PC cards and pagers assembly
	Plantation, FL	Two-way radio assembly
	Puerto Rico	Portable energy systems (batteries and chargers)
	Costa Rica	Portable energy systems (batteries and chargers)
	Sao Paulo, Brazil	Board assembly (base stations)
	Angers, France	Board assembly (automotive products)
	Stotfold, U.K.	Design and board assembly (automotive products)
	Dublin, Ireland	Portable energy systems (batteries and chargers)
	Penang, Malaysia	Portable energy systems (batteries and chargers)
NextLevel Systems	Horsham, PA	Headquarters (transferred from Chicago in Q1/98)
	Hatboro, PA	Design (Broadband Networks Group)
	San Diego, CA	Design (Satellite Data Networks Group)
	Rohnert Park, CA	Design (Communications Group)
	Nogales, Mexico	Board assembly (satellite receivers)
Northern Telecom	Belleville, Ontario, Canada	Board assembly (integrated services network products)
	Calgary, Alberta, Ontario	Board assembly (digital key telephone sets, cellular)
	Burnaby, B.C., Canada	Board assembly (digital and analog multiplex, teleprotection, and fiber optic transmission systems)

Table 11 (Continued)
Company Purchasing, Design, and Manufacturing Locations

Company	Site Location	Site Activity
	Santa Clara, CA	Board assembly (integrated services network products)
	Shekou, Shenzhen, China	Board assembly (Meridian SL-1 PABX products)
	Norcross, GA	Design and board assembly (telecom digital products; Digital central office switches; broadband markets)
	Mervue, Galway, Ireland	Board assembly (many products)
	Penang, West Malaysia	Board assembly (magnetics, printed circuit packs, acoustic components)
	Monterrey, Mexico	Board assembly (telephones)
	Research Triangle Park, NC	Design and board assembly (digital central office switches)
	Newtownabbey, Northern Ireland	Board assembly (transmission products)
	Brampton, Ontario, Canada	Board assembly (central office applications)
	Brockville, Ontario, Canada	Board assembly (digital telephone switching equipment)
	Nepean, Ontario, Canada	Design and board assembly (custom semiconductors and electronic components)
	Lachine, Quebec	Board assembly (power systems)
	St. Laurent, Quebec	Board assembly (electronic transmission products)
	Verdun, Quebec	Design (cellular phone and video)
	Istanbul, Turkey	Board assembly (switching systems, power systems, telephones)
	Richardson, TX	Design
	Harlow, Essex, England	Design (telecommunications products)
	Newport, Gwent, Wales	Board assembly (U.K. defense products)
	Paignton, Devon, England	Design and board assembly (optoelectronic telecommunications)
	Hong Kong	Supply and commodity management
	Mississauga, Ontario, Canada	Supply and commodity management
	Lachine, Quebec, Canada	Supply and commodity management
	Nashville, TN	Supply and commodity management
	London, England, U.K.	Supply and commodity management
Quantum	Milpitas, CA	Headquarters, design and procurement
	Shrewsbury, NH	Board assembly (tape drives)
	Japan	Procurement
	Singapore	Procurement and board assembly (tape drives)
	Batam Island, Indonesia	Board assembly (tape drives)
Raytheon	More than 100 offices, plants, and R&D centers worldwide	-

Table 11 (Continued)
Company Purchasing, Design, and Manufacturing Locations

Company	Site Location	Site Activity
Rockwell	More than 142 plants and R&D centers worldwide	-
SCI Systems	Huntsville, AL	Design, board assembly, procurement (PCs)
	Augusta, ME	Board assembly
	Hooksett, NH	Board assembly
	Graham, NC	Board assembly
	Watsonville, CA	Board assembly
	San Jose, CA	Design and board assembly (PCs)
	Colorado Springs, CO	Board assembly
	Rapid City, SD	Board assembly
	Netherlands	Board assembly (PCs)
	Singapore	Procurement and board assembly (PCs)
	Thailand	Board assembly (PCs)
	Grenoble, France	Board assembly (PCs)
	Fermoy, Ireland	Board assembly (PCs)
	Guadalajara, Mexico	Board assembly (PCs)
	Irvine, Scotland	Procurement and board assembly
	Montreal, Canada	Board assembly
Seagate	Bloomington, MN	Design and board assembly (disk drives)
	Costa Mesa, CA	Design and Central procurement (tape drives)
	Longmont, CO	Design and board assembly (tape drives)
	Oklahoma City, OK	Design and board assembly (disk drives)
	Santa Maria, CA	Design
	Scotts Valley, CA	Headquarters, procurement, design
	Indonesia	Board assembly
	Thailand	Board assembly (components)
	Perai, Malaysia	Disk drive assembly
	Penang, Malaysia	Disk drive assembly
	Johor Baharu, Malaysia	Board assembly (disk drives)
	Wuxi, China	Board assembly (disk drives)
	Shenzen, China	Board assembly (disk drives)
	Singapore	Design, procurement and board assembly (disk drives)
	Springtown, N. Ireland	Board assembly
Silicon Graphics	Mountain View, CA	Design and board assembly
	Chippewa Falls, WI	Board assembly (supercomputers)
	Neuchatel, Switzerland	Board assembly
Solectron	Milpitas, CA	Board assembly for PCs, networking, workstations
	Charlotte, NC	Board assembly for PCs, networking, workstations

Table 11 (Continued)
Company Purchasing, Design, and Manufacturing Locations

Company	Site Location	Site Activity
	Boston, MA	Board assembly for PCs, networking, workstations
	Austin, TX	Board assembly for PCs, networking, telecom, workstations
	Everett, WA	Board assembly
	Guadalajara, Mexico	Board assembly
	Sao Paulo, Brazil	Board assembly for telecom
	Penang, Malaysia	Board assembly for PCs, networking, telecom, workstations
	Johor, Malaysia	Board assembly for PCs, networking, telecom, workstations
	Cestas Cedex, France	Board assembly for PCs, networking, telecom, workstations
	Dunfermline, Scotland	Board assembly for PCs, networking, telecom, workstations
	Herrenberg, Germany	Board assembly for PCs, networking, workstations
	Suzhou, China	Board assembly
	Atlanta, GA (4/98)	Board assembly
	Columbia, S.C. (4/98)	Board assembly
	Dublin, Ireland (4/98)	Board assembly
Sun Microsystems	Palo Alto, CA	Design
	Menlo Park, CA	Design
	Milpitas, CA	Design, procurement, board assembly
	Linlithgow, Scotland	Board assembly
Texas Instruments	Stafford, TX	Design (automotive products)
	Attleborough, MA	Board assembly (automotive products)
	Almelo, Netherlands	Board assembly (automotive products)
	Aguascalientes, Mexico	Board assembly (automotive products)
	Oyama, Japan	Board assembly (automotive products)
	Chincon, Korea	Board assembly (automotive products)
TRW	Farmington Hills, MI	Design
	Irwindale, CA	Board assembly (automotive sensors)
	Rochester Hills, MI	Board assembly (automotive sensors)
	Marshall, IL	Board assembly (automotive products)
	Auburn, NY	Board assembly (automotive products)
	Union Springs, NY	Board assembly (automotive products)
	Brantford, Ontario, Canada	Board assembly (automotive products)
	Reynosa, Mexico	Board assembly (automotive products)
	Sao Paulo, Brazil	Board assembly (automotive products)
	Radolfzell, Germany	Design, board assembly (automotive products)

Table 11 (Continued)
Company Purchasing, Design, and Manufacturing Locations

Company	Site Location	Site Activity
	Paris, France	Design
	Osny, France	Board assembly (automotive products)
	Barcelona, Spain	Board assembly (automotive products)
	Turin, Italy	Board assembly (automotive products)
	Benesov, Czech Republic	Board assembly (automotive products)
	Sunderland, U.K.	Board assembly (automotive products)
Unisys	Mission Viejo, CA	Design (storage products)
	San Jose, CA	Board assembly (PCs and servers)
	Rancho Bernard, CA	Board assembly (servers and storage products)
	Plymouth, MI	Board assembly (image and document processing products
	Roseville, MN	Board assembly (servers)
	Tredyffrin, PA	Board assembly (servers)
	Salt Lake City, UT	Design
	Winnipeg, Manitoba, Canada	Board assembly (storage products)
	Villers-Ecalles, France	Board assembly
	Sao Paulo, Brazil	Board assembly
Varian Associates	Palo Alto, CA	Design and assembly (health care products and analytical instruments)
	Baden, Switzerland	Board assembly (health care products)
	Helsinki, Finland	Board assembly (health care products)
	Salt Lake City, UT	Board assembly (health care products)
	Arlington Heights, IL	Board assembly (health care products)
	Charleston, SC	Board assembly (health care products)
	Gloucester, MA	Design and board assembly (semiconductor manufacturing equipment)
	Seoul, Korea	Board assembly (semiconductor manufacturing equipment)
	Songtan, Korea	Board assembly (semiconductor manufacturing equipment)
	Nirasaki, Japan	Board assembly (semiconductor manufacturing equipment)
	Melbourne, Australia	Board assembly (analytical instruments)
	Walnut Creek, CA	Board assembly (analytical instruments)
	Harbor City, CA	Board assembly (analytical instruments)
	Lexington, MA	Board assembly (analytical instruments)
	Turin, Italy	Board assembly (analytical instruments)
	Tempe, AZ	Board assembly
Western Digital	San Jose, CA	Design (HDDs)
	Irvine, CA	Design (HDDs)
	Singapore	Board assembly (HDDs)

Table 11 (Continued)
Company Purchasing, Design, and Manufacturing Locations

Company	Site Location	Site Activity
	Malaysia	Board assembly (HDDs)
Xerox	Palo Alto, CA	Design
	El Segundo, CA	Board assembly
	Manaus, Brazil	Final assembly (printers, office equipment)
	Resende, Brazil	Final assembly (printers, office equipment)
	Shanghai, China	Manufacturing (printers)
	Suzhou, China	Manufacturing (printers)
	Wuhan, China	Manufacturing (printers)
	Rampur, India	Manufacturing and final assembly
	Ebina, Japan	Final assembly (copiers)
	Iwatsuki, Japan	Final assembly (printer peripherals)
	Suzuka, Japan	Board assembly
	Aguascalientes, Mexico	Final assembly (office equipment)
	Venray, Netherlands	Final assembly (office equipment)
	Coslada, Spain	Final assembly (office equipment)
	Mitcheldean, U.K.	Board assembly

Source: Dataquest (February 1998)

Dataquest Perspective

This document presented some key information about leading North American-based purchasers of semiconductor. Last year's survey results showed that the memory price decreases of 1996 drove a decline in semiconductor spending. In 1997, although memory prices continued to decrease, the results of the study indicate that companies seemed to have increased their overall purchases of semiconductors. More specifically, the results of the study show that:

- Companies have spent proportionately less on memory. Volatile memory represented 28 percent of the 1996 sample's spending, but it represented only 23 percent of the 1997 sample's spending. However, other research indicates that, in general, bit consumption has increased.
- Spending was highest in the MPU/MCU/DSP and ASIC/ASSP categories. Spending on ASICs and ASSPs combined represented 32 percent of the total sample's spending, and spending on microcomponents represented 25 percent of the total. Companies are using ASIC and ASSP devices to differentiate their products and using more MPUs and MCUs (or higher-performance/higher-density devices) to improve their products' performance or to add features enabled by the power of microprocessors or microcontrollers.

The success of electronic systems depends to a significant extent on semiconductor technology advances. Also, a majority of the electronics application industries have reached critical mass and have enough volume to support markets for standard semiconductor devices, ASSPs in particular.

Semiconductor manufacturers need to remain focused and application oriented and strengthen their relationships with customers, which are being more selective. Semiconductor vendors must become customer-centric and service oriented, because lead time, delivery time, and availability have become critical issues to systems OEMs focusing on total cost , not price alone, when determining component buying. Service points should be maintained around the globe, emphasizing applications engineering in the United States and field sales in Europe, Japan, and Asia/Pacific.

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Perspective

ASIC/SLI Worldwide

Market Analysis

Evaluating the Market for ASIC Intellectual Property

Abstract: *As system-level ASICs move into the mainstream, the market focus moves to the business of intellectual property. This analysis establishes a definition of intellectual property in ASICs that allows for a meaningful market assessment. Based on an incremental value model, Dataquest forecasts the ASIC intellectual property market to reach $2.3 billion by 2001.*

By Jordan Selburn

Just What Is Intellectual Property?

The term "intellectual property" inspires discussions that approach religious wars in their ferocity. As system-level ASICs start to move into the mainstream, conflict is occurring among ASIC vendors, systems designers, and third parties over who provides the value-adding intellectual content of these chips.

For the purposes of evaluating the true size of the ASIC intellectual property (IP) market, only that property for which a customer is willing to pay should be considered. Furthermore, to determine what people are willing to pay for the intellectual content of an ASIC, it is essential to subtract the value of any commodity content. For example, to establish the intellectual content of a $2 pint of Ben and Jerry's vanilla ice cream, the $1.50/pint cost of the store-brand product must be subtracted; that is, customers are paying $0.50 per pint for Ben and Jerry's intellectual property, which in this case includes everything from a better recipe to name-brand status. Adapting this approach to the ASIC market provides the following definition: *Intellectual property is a process, library, or other similar attribute in an ASIC that adds incremental value over generically available ASIC logic functions.*

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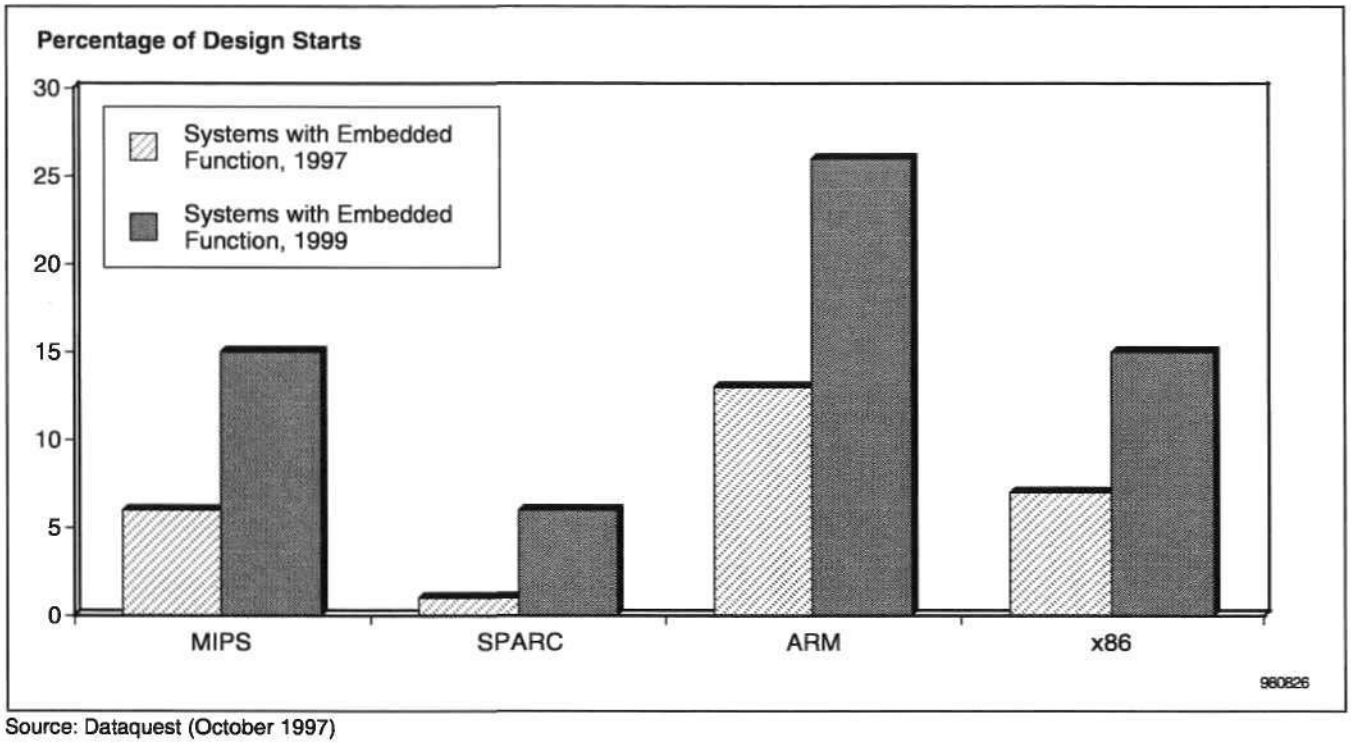
This results in a very broad characterization of intellectual property in an ASIC yet one that is most appropriate for determining the value of the intellectual property marketplace. This definition includes the following ASIC attributes and features:

- System-level macros such as embedded microprocessors, among others
- Logic and memory libraries, architectures, or generators that enhance performance, heighten density, or reduce power consumption
- High performance or otherwise nonstandard (such as low-voltage differential signaling, or LVDS) I/Os
- Analog and mixed analog/digital functions

The User's Demand for IP

Dataquest's 1997 ASIC User Survey (*Designers Focus on System Integration*, ASIC-WW-UW-9701, October 1997) confirms the growing appetite for intellectual property. The percentage of ASIC designs that incorporate system-level functions is growing, from about 26 percent in 1996 to 40 percent in 1998, a 50 percent increase in two years. An example of this is in Figure 1, which shows the increasing usage of some of the more popular embedded microprocessors. Other forms of system-level macros, such as digital signal processors (DSPs), show an equally strong growth trend.

Figure 1
Embedded Microprocessor Usage



Source: Dataquest (October 1997)

Sources of Intellectual Property

The provider of value-adding components within an ASIC is in a position to capture a disproportionate share of the end price. One of the best examples of this is Intel's leverage with its microprocessor in the personal computer market, which is discussed later. This battle to own the intellectual content of an ASIC can vary as a function of the type of content. Table 1 provides some examples of different kinds of intellectual property and the competition to develop them. There can also be competition between types of intellectual property. For example, power consumption by logic elements can be reduced through either custom silicon process enhancements or custom library elements, yet both approaches add value to the end product.

Table 1
Ownership of Intellectual Property

Type Of Intellectual Property	Example	Example's Added Value	Owner
Process Enhancement	Copper interconnect	Improved performance	Semiconductor manufacturer
Enhanced Libraries	Low-power memories	Reduced ASIC power consumption	Semiconductor manufacturer or third-party library developer
System-Level Macro	MPEG decoder	Reduced time to market, meeting industry standard	Third-party developer, semiconductor manufacturer, or system designer

Source: Dataquest (February 1998)

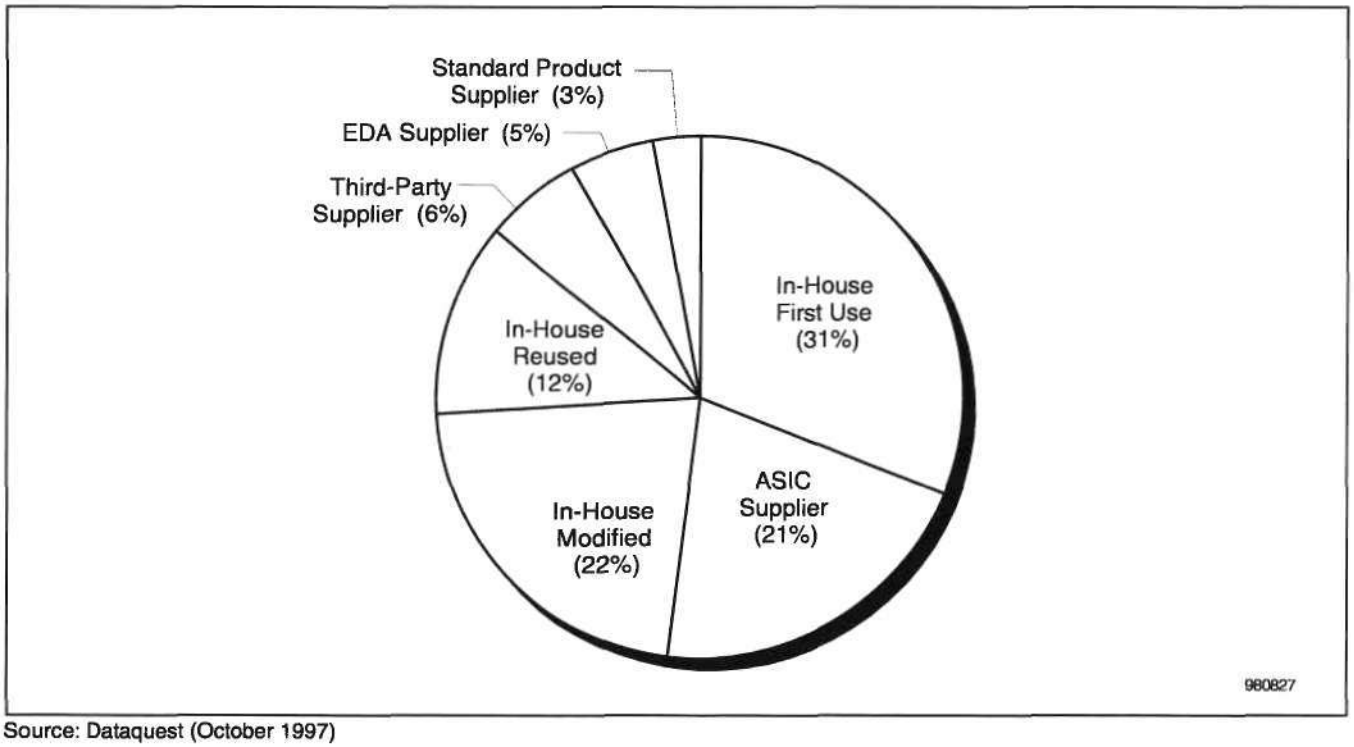
With the widest range of potential participants, the battle to supply system-level macros is being fought particularly hard. Dataquest asked users their sources of system-level macros, and the results are shown in Figure 2. In 1997, the overall percentage of embedded macros from in-house sources was about 65 percent, with the majority of the remainder supplied by ASIC vendors. Although this split has not changed significantly over the past two years, design reuse is on the upswing, with only 31 percent of the in-house functional blocks developed from scratch in 1997 versus 39 percent in the previous year. This trend will accelerate as design methodologies that support reuse become more available.

Intellectual Property and the Value Chain

Value Chain Example: The Intel Microprocessor

One clear example of an intellectual property owner extracting value from its property is Intel and the x86 microprocessor. From 1994 through 1997, the average price for a personal computer stayed relatively constant at about $2,000. During the same period, the average price of an Intel x86 microprocessor increased from $175 to $200, although Intel's average costs were decreasing. By recognizing the value of its intellectual property, Intel was able to capture an additional 1 percent of the system price for its own top line.

Figure 2
Functional Block Sources



Source: Dataquest (October 1997)

The Intellectual Property Life Cycle

Just like any other product, intellectual property has a life cycle. An example of intellectual property that added incremental value to ASICs in the early 1990s was embedded six-transistor SRAM. With the exception of specialized SRAM in ASICs, such as very high-performance or low-power memory, the value added by this feature has dwindled to that of a commodity product. Table 2 shows how some of today's intellectual property is progressing through the product life cycle. The examples were chosen to represent a snapshot of different points in the ASIC intellectual property life cycle; of course, the specific products chosen are moving through the various phases with time.

An especially important aspect of the ASIC intellectual property life cycle is the revenue split between the owner and "distributor," that is, the ASIC manufacturer (sometimes these are the same entity), and the dynamics of this split over time. In the introduction phase, there is often only one owner and distributor of a given piece of intellectual property, and both can claim a share of the incremental profits. If substitutes are few or expensive, these profits can be quite handsome. However, as the intellectual property matures and more ASIC vendors offer the capability, simple economics dictates that the ASIC vendor's incremental profits will diminish. As substitutes (such as competing microprocessor architectures) arise or others are able to own the same intellectual property (which can and does happen in the case of industry standards, such as PCI), the owner's incremental profits decrease, as well.

Table 2
The Intellectual Property Life Cycle

	Availability	Usage	IP Owner	Silicon Vendor	Example
Introduction	One to two owners, few silicon vendors, limited substitutes	Limited number of applications	High value capture	High value capture	Embedded flash
Adoption	One to two owners, several vendors, some substitutes	Growing number of applications benefit from on-chip integration	High value capture	Decreasing value capture	Oak DSP
Maturity	One owner or more, many silicon vendors, widespread substitutes	Majority of applications benefit from on-chip integration	Decreasing value capture	Little to zero value capture	ARM processor
Standard	Public ownership, majority of silicon vendors	Standard feature of many designs	Continuing decrease of value capture	Little to zero value capture	PCI I/O

Source: Dataquest (February 1998)

Intellectual Property Revenue Models and Forecasts

There is no one way to measure the size of the ASIC intellectual property market. Despite this, there have been a number of forecasts of the market size made without specifying exactly what is being forecast. With a concept as recent as intellectual property, it is essential to define the market before developing a forecast.

Standalone IP Vendors

Perhaps the most restrictive way to bound the market is to look at only those companies whose sole business is licensing intellectual property. These companies, such as Advanced RISC Machines Ltd., Artisan Components Inc., and the DSP Group develop various types of intellectual property and sell them to ASIC vendors or directly to OEMs. The business model varies by company, with most revenue to date coming from licensing fees. Most of the leading intellectual property vendors are moving toward a royalty-based model, which could prove very effective for companies with leading-edge products. Other companies, especially those offering intellectual property that is more of a commodity, frequently use a one-time access fee.

The problem with this revenue model is that it ignores the intellectual property developed by vertically integrated semiconductor vendors and by OEMs. An example of this is shown in Table 3, which demonstrates how an ASIC vendor could use dense cell libraries to command a higher profit margin. Die 2 uses libraries that are 14 percent denser than Die 1, such as could be achieved through a reduction in metal grid from 1.4 to 1.3 microns; the result is a product that can be sold for less yet produce higher profits. Particularly interesting in this case is that this intellectual property provides a win-win: the end cost to the customer is less, but the ASIC vendor makes a larger gross margin and frees manufacturing capacity. In the case in which

the advanced cell libraries are developed by a third party, this incremental profit must be split.

Table 3
Example of Intellectual Property Value Calculation

	Die 1	Die 2
Core Area (Sq. mm)	56.25	48.21
Die Area (Sq. mm)	72.25	63.09
Die Height (mm)	8.5	7.9
Yield (%)	81	83
Gross Die per Wafer	143	164
Net Die per Wafer	115	135
Die Cost ($)	8.69	7.39
Package Cost ($)	2.40	2.40
Total Cost ($)	**11.09**	**9.79**
Profit Margin (%)	45	50
Price ($)	20.17	19.57

Source: Dataquest (February 1998)

System-level macros developed by ASIC vendors or OEMs are also ignored by this revenue model yet probably represent the bulk of the market. In addition, it would be difficult, if not impossible, for vertically integrated companies to identify the revenue associated with a particular piece of intellectual property.

Silicon Acreage

Yet another way to calculate the value of intellectual property is simply to calculate the ratio of the area taken by system-level macros and advanced memories, among others, to the die area as a whole. This ratio could then be applied to the total price to determine the price charged for this intellectual content. The major drawback to this method is that it assumes that all intellectual property is of the same value per unit area, clearly incorrect when the intellectual property life cycle is considered, and will grossly overestimate the total value. An example of this could be one of the commonly available embedded microprocessor cores, which, although an important part of the design, is widely available and has many substitutes; it therefore can command little incremental value over random logic.

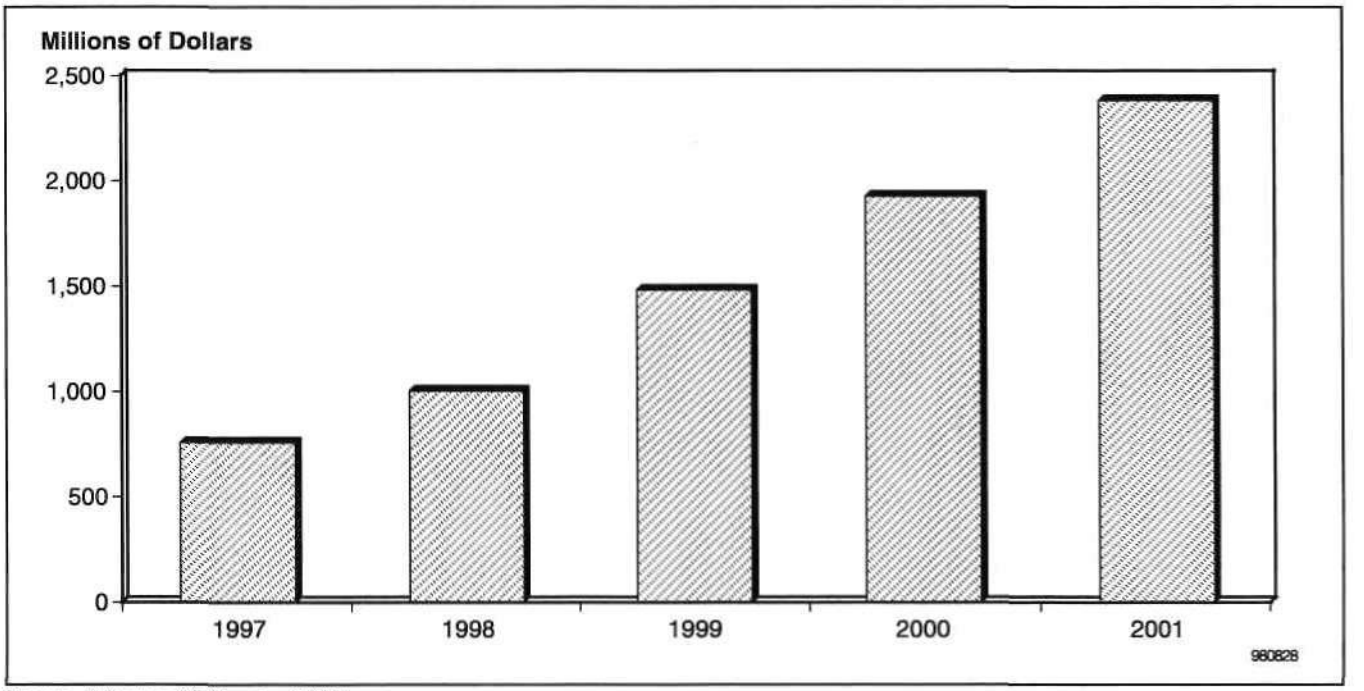
Incremental Value

The clearest measure of value is what the customer is willing to pay—strictly a function of basic economics. Again, as shown in the ice cream example in the beginning of this document, it is essential to subtract the commodity portion of the market to arrive at the true value of intellectual property. The typical gate array ASIC profit margin can be used as a proxy for the value of commodity logic. The higher margin commanded by cell-based ASICs is due to the intellectual content; in general, customers would otherwise purchase gate arrays, with their faster turnaround time. This intellectual content can

take many forms, and some of those forms (such as dense cell libraries) may reduce the end cost yet still boost the gross margin.

The incremental margin commanded by cell-based ASICs over gate arrays is then applied to the cell-based market as a whole to determine the value of intellectual property in ASICs. The result is shown in Figure 3, with the ASIC intellectual property value nominally forecast to exceed $2.3 billion in 2001.

Figure 3
Intellectual Property Revenue Forecast



Source: Dataquest (February 1998)

It is important to remember two things about this forecast. First, this revenue represents the incremental value of the intellectual property in the ASIC, not the total revenue from the ASIC. Second, these numbers represent the total of both real revenue for dedicated intellectual property vendors and "virtual" revenue for ASIC vendors; there is no income statement line item calling out the latter number.

Revenue Scenarios

There are a number of factors that could significantly affect intellectual property revenue.

The VSIA Wild Card

System-level macro standards such as the Virtual Socket Interface Alliance (VSIA) standard could become widespread sooner than 2000. This would be good news for third-party developers, because they would be able to disseminate their intellectual property widely and rapidly, but it would be bad news for the semiconductor manufacturer distributors, because they would face more competition, including, potentially, foundries. The result

would be higher revenue for standalone vendors but lower total intellectual property revenue.

Programmable Logic Failing to Compete with Gate Arrays

Programmable logic companies could fail to provide a reasonably priced solution for pure logic designs below 100,000 gates. One of the main reasons for the erosion of the gate array market has been the onslaught of comparatively high-gate-count programmable logic devices (PLDs), which outdo the gate arrays in time to market. If, for some reason (such as a foundry manufacturing undersupply), PLDs lose their momentum in this market, gate array margins—representing the commodity logic baseline—could stabilize and decrease the overall incremental value of intellectual property.

Manufacturing Consortiums

In a fashion similar to VSIA, groups such as the recently announced International Sematech could reduce the total revenue for intellectual property. As advances in manufacturing technology spread more rapidly and widely, the premium charged for this intellectual content diminishes. In general, the success of consortiums means trouble for dedicated ASIC vendors, which could lose an important edge to lower-cost competitive foundries. This effect is already starting to be seen, but successful technology sharing will accelerate the trend. Tempering this downside potential, though, is the traditional problem that committees encounter: a group of more than three people cannot decide where to have lunch, much less anything important.

Dataquest Perspective—How to Succeed Using Intellectual Property

The key to surviving the industry changes wrought by intellectual property is recognizing what content adds value and what content is a commodity. When manufacturing becomes a commodity, as may happen for most consumer-type designs, ASIC vendors should question the wisdom of building a shiny new $1 billion-plus fab. Partnerships with foundries, which can attain economies of scale beyond those available to most vertically oriented companies, may be the only way to thrive or even just survive. Dedicated fabs may make sense when the manufacturing process is optimized for a market niche such as wireless, however.

Implicit in the distinction between valuable versus commodity intellectual property is an understanding of the product life cycle. When an ASIC vendor is the 20th licensee of some microprocessor, the vendor must realize that this particular system-level macro will bring little or no incremental margin although it may be a requirement even for bidding on a new design. Only ownership of or access to intellectual property in the early stages of the life cycle will allow a company to achieve beyond-market profit margins. Partnerships with small start-up intellectual property "garage shops" may be one good way to stay ahead of the curve.

The ASIC product is becoming more horizontal than vertical. Packaging, EDA tools, and, now, library functions are all moving away from the standalone ASIC vendor. In response, the ASIC vendor must move closer to the customer, becoming an expert in systems design as well as silicon and recognizing where and how to invest in the intellectual property (processes as well as libraries) that will prove crucial to the customer, and for which the customer is willing to pay.

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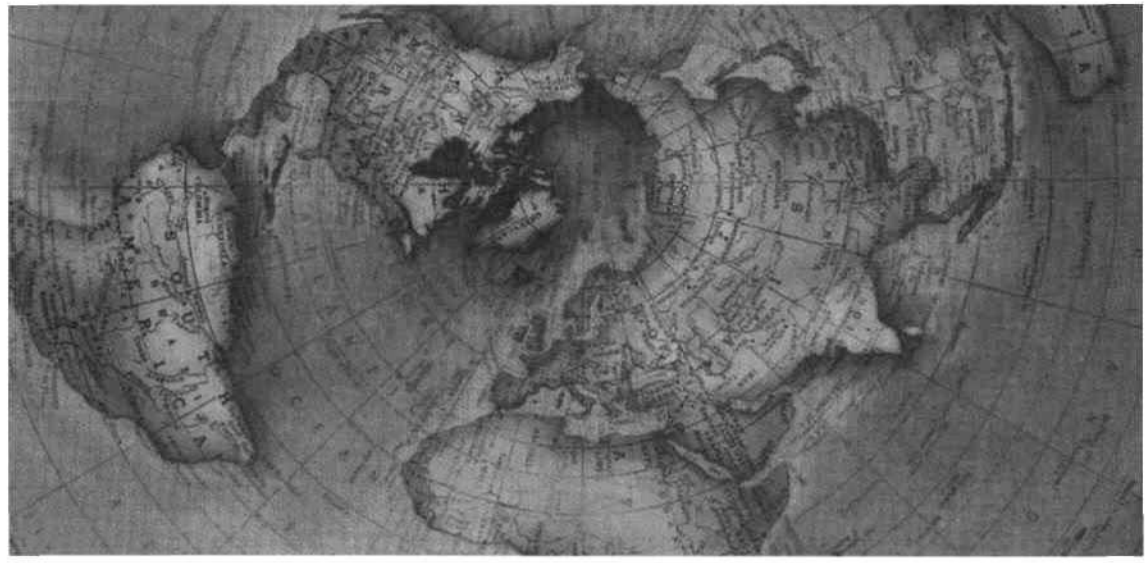
Perspective



ASIC/SLI Worldwide

Market Analysis

1997 European ASIC Design Starts Survey

Abstract: *The European design starts survey analyzes the number of design starts, cell-based versus gate array trends, and industry sector issues in the 1996-to-1997 period. The communications sector is analyzed in further detail because of its importance to the European ASIC market. Trends in core usage, feature size, and interconnect are considered, together with the impact of system-level integration (SLI). The number of designs in each European country or region is also presented.*
By Jim Tully

Executive Summary

Dataquest's 1997 European ASIC design starts survey was based on responses from 21 vendors. These vendors accounted for 86 percent of the gate array and cell-based ASIC markets by revenue in 1996. The results of the survey are therefore highly representative of the overall market and provide a sound basis on which to make decisions. The main findings of the survey are as follows:

- Europe accounted for 1,229 ASIC design starts in 1996, a rise of 4.9 percent over 1995. The figure is projected to rise by 7.7 percent in 1997.
- The majority of designs result in device shipments of well over half a million units.
- The average ASIC revenue per design will rise from $2.0 million in 1996 to $2.2 million in 1997, an increase of 10 percent.
- Cell-based designs account for more than 60 percent of all design starts. Total array designs fell by 1.2 percent over the period. Even embedded

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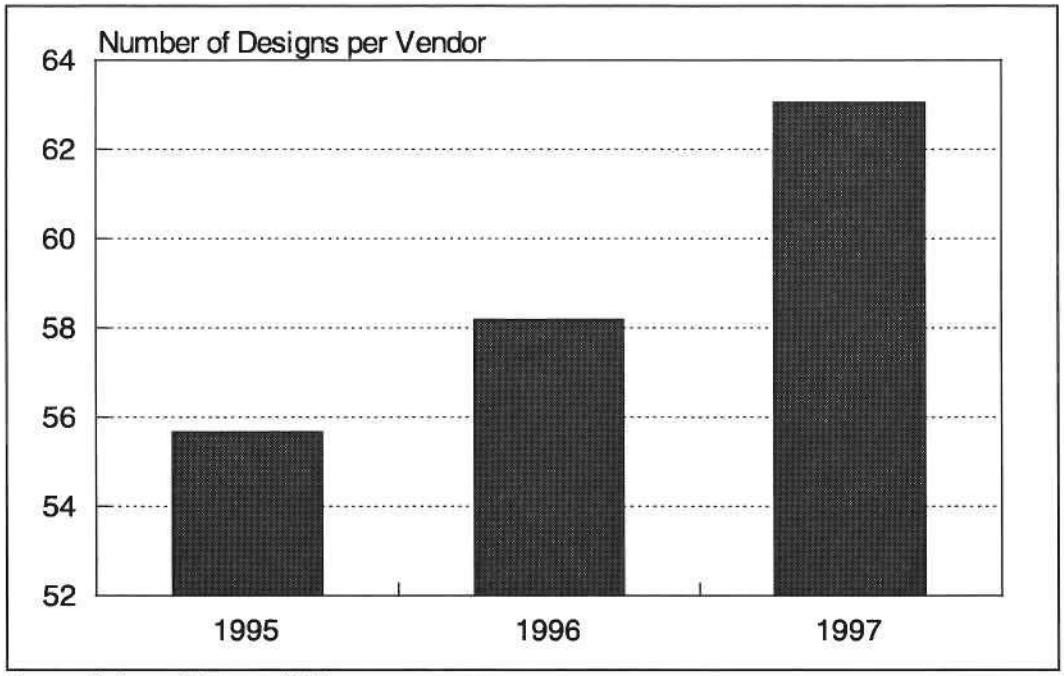
arrays lost share in terms of percentage of all design starts, although this category grew by about 3 percent in unit terms.

- The communications sector continues to dominate ASIC design and production in Europe, growing from 55 percent to 57 percent of all designs in the 1996 to 1997 period.
- The single largest gate count category is still "less than 50,000 gates," with 41 percent of all design starts in 1996.
- In 1996, 0.5-micron geometry dominated designs, with almost twice as many designs as the second-largest category—0.8 micron. During 1997, the gap has closed considerably, with the second-largest category now 0.35 micron.
- Three-level metal now accounts for more design starts than any other category. At the high end of the market, five-level metal has continued to gain share.
- In 1997, 277 design starts are designated as system-level integration (SLI) designs, a rise of 147 percent over 1996. These designs are undertaken by a handful of vendors and are still a small minority of all European designs but are expected to dominate the ASIC market within three years.
- SRAM, ROM, and microcontroller cores are by far the most commonly used in view of the large number of embedded applications for these devices.
- Germany continues to account for the largest number of designs, followed by the United Kingdom. The German market has continued its growth for the second year, led by its telecommunications sector following two or three years of relative decline. The United Kingdom saw a considerable amount of design activity in the computer, mobile communications, and data communications sectors.
- Digital designs continue to account for the bulk of ASIC design starts in Europe; however, mixed-signal technology has long been of growing importance in Europe owing mainly to the requirements of the telecommunications sector. The gap is continuing to narrow, with mixed-signal design starts approximately one-third of the number of digital designs.

Quantity of Designs and Revenue Contribution

Europe accounted for 1,229 ASIC design starts in 1996, a rise of 4.9 percent over 1995. The figure is projected to rise by 7.7 percent to 1,324 design starts in 1997. The average number of designs per vendor in Europe will rise to approximately 63 in 1997 (see Figure 1). This successive rise in design starts over a three-year period is a healthy sign for the ASIC market because the number of design starts is a reliable leading indicator of the ASIC market. The last fall in European design starts occurred in 1995, and this was reflected in sharply reduced ASIC market revenue growth in 1996 coupled with an impact on forecast 1997 revenue.

Figure 1
Average Number of Designs per Vendor—Europe, 1995-1997



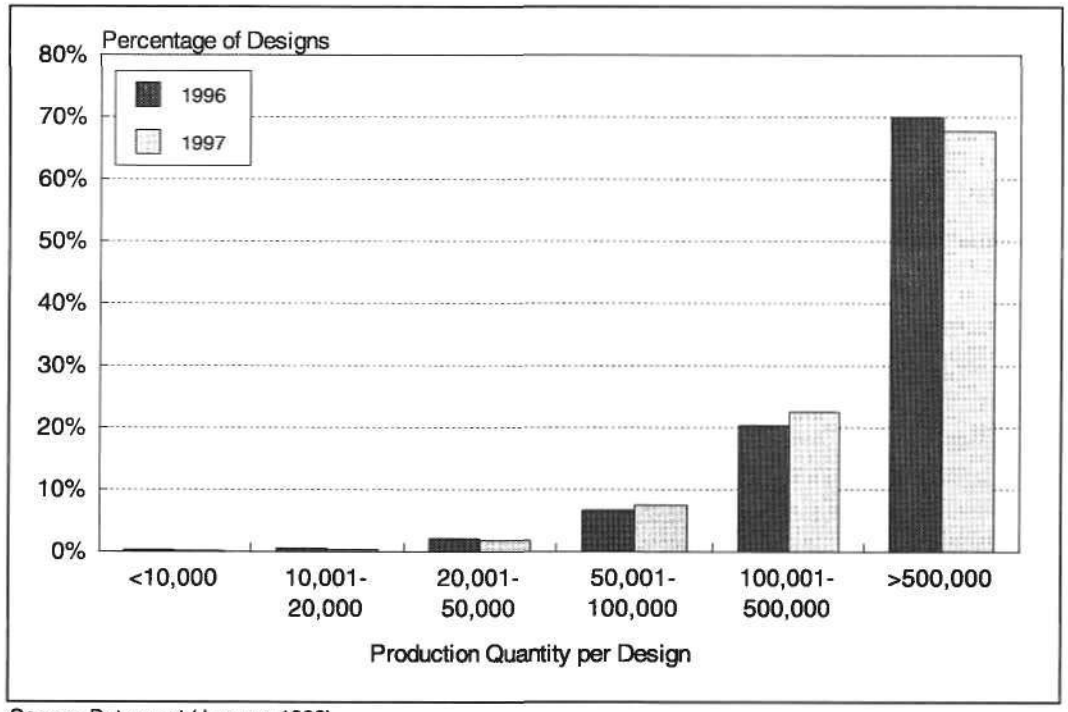
Source: Dataquest (January 1998)

Over the past three years the average production quantity of ASIC devices resulting from each design has risen considerably as vendors have focused on higher-value accounts. This shift has stabilized over the past two years to a situation where the majority of designs result in device shipments of more than half a million units (see Figure 2).

Another measure of the effectiveness of ASIC designs is the average revenue resulting from each design. In this Perspective, Dataquest assumes that ASIC revenue in a given year comprises revenue components originating from design starts in previous years according to the breakdown in Table 1 (individual designs will, of course, vary depending on the product and industry sector into which the ASIC is designed).

Dataquest assumes that ASIC designs have a revenue-generating lifetime of three years, with most of the contribution occurring in the first year. Coupling these assumptions with Dataquest's latest revenue forecast, the overall ASIC revenue per design will rise from $2.0 million in 1996 to $2.2 million in 1997, an increase of 10 percent. On closer examination, cell-based designs are responsible for the bulk of the revenue and for all of the growth, from $2.3 million in 1996 to $2.6 million in 1997 (see Table 2).

Figure 2
ASIC Production Quantity per Design—Europe, 1996 and 1997



Source: Dataquest (January 1998)

Table 1
Revenue Contribution of Design Start

Time after Year X Design Start	Revenue Contribution from Design Start (%)
Year X + One Year	55
Year X + Two Years	37
Year X + Three Years	8

Source: Dataquest (January 1998)

Table 2
Average Revenue per ASIC Design—Europe, 1996 and 1997

	1996			1997		
	Number of Designs	Resulting Revenue ($M)	Revenue per Design ($M)	Number of Designs	Resulting Revenue ($M)	Revenue per Design ($M)
Gate Array	461	708	1.5	455	704	1.5
Cell-Based	768	1,780	2.3	869	2,255	2.6
Total ASIC	**1,229**	**2,488**	**2.0**	**1,324**	**2,959**	**2.2**

Source: Dataquest (January 1998)

Cell-Based Continues to Lead

Europe has long been a stronghold of cell-based design, largely owing to the interest in mixed-signal devices for telecommunications applications. Cell-based designs account for more than 60 percent of all design starts (see Figure 3). Total array (that is, traditional plus embedded) designs fell by

1.2 percent over the period. Even embedded arrays lost share in terms of percentage of all design starts, although this category grew by about 3 percent in unit terms.

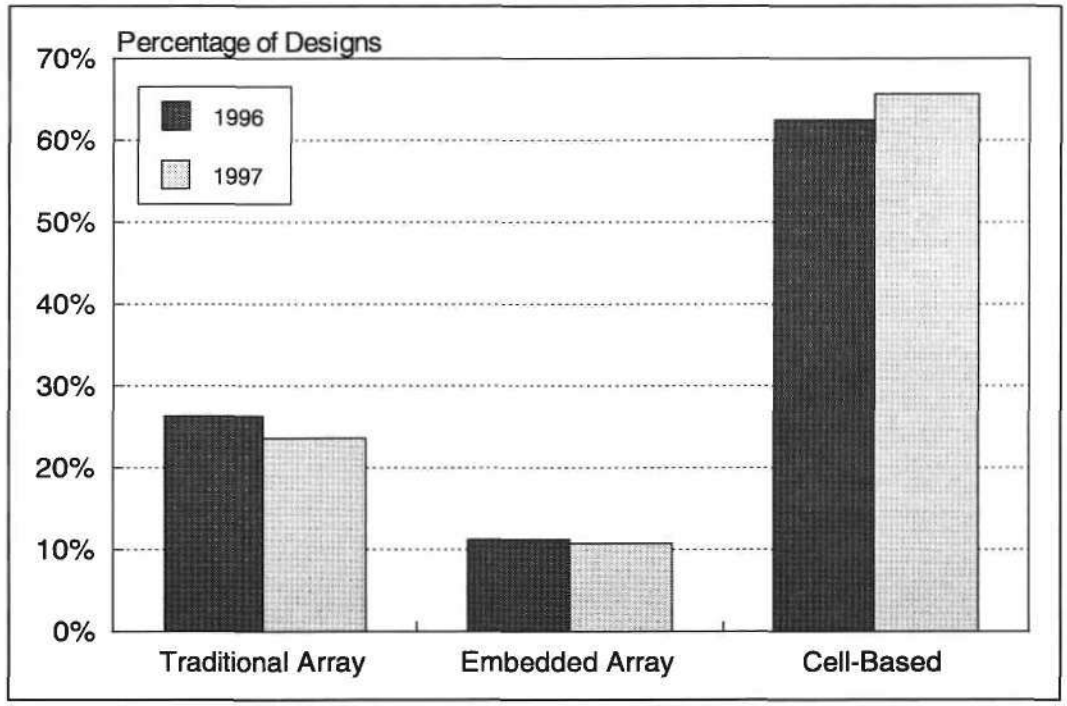
Differentiation for gate array suppliers is limited mainly to offering lower prices and faster turnaround time, although engineering charges are also lower. Originally consisting of prefabricated logic blocks requiring only a final customized mask layer, the gate array became the preferred solution for most random logic applications. But gate arrays are becoming larger and more complex, requiring additional metallization levels as a result, and, therefore, some of the advantages of gate arrays have been lost. Also, many designs include a processor core or a large section of memory. Here, gate arrays cannot offer the same level of efficiency as cell-based devices, so these designs tend to go to cell-based device suppliers. However, embedded arrays are stepping in to fill the gap in part and are having some degree of success.

The increase in cell-based designs acts as a multiplier of future ASIC revenue in view of the higher price of these devices compared to gate arrays. This follows from the increased functionality that cell-based devices typically have. This is consistent with Dataquest's current revenue forecast, which shows cell-based device revenue pulling away from gate arrays at an accelerating rate over the next two to three years.

Design Starts by Sector

The communication sector continues to dominate ASIC design and production in Europe, growing from 55 percent to 57 percent of all designs in the 1996-to-1997 period (see Figure 4). This reflects the strength of Europe in several major communications applications, notably mobile communications and public switching and transmission. Each of these applications is forecast to account for 33 percent of European communications design starts (see Figure 5). Public switching and transmission applications have fallen for the third successive year as a result of the completion of most of the large-scale digitization projects in the major European countries. Mobile communications continues to rise after a slight decline in 1996, with major ongoing design programs under way in mobile telephone handsets and cellular base stations. Changes in non-European standards and protocols, such as CDMA and D-AMPS, trigger much design in this sector in Europe in view of the worldwide strength of European cellular OEMs. Data networking is another fast-growing application, accounting for more than 20 percent of communications designs. This application has been fueled by a strong PC aftermarket, changing standards and protocols and a growing proportion of European-designed units.

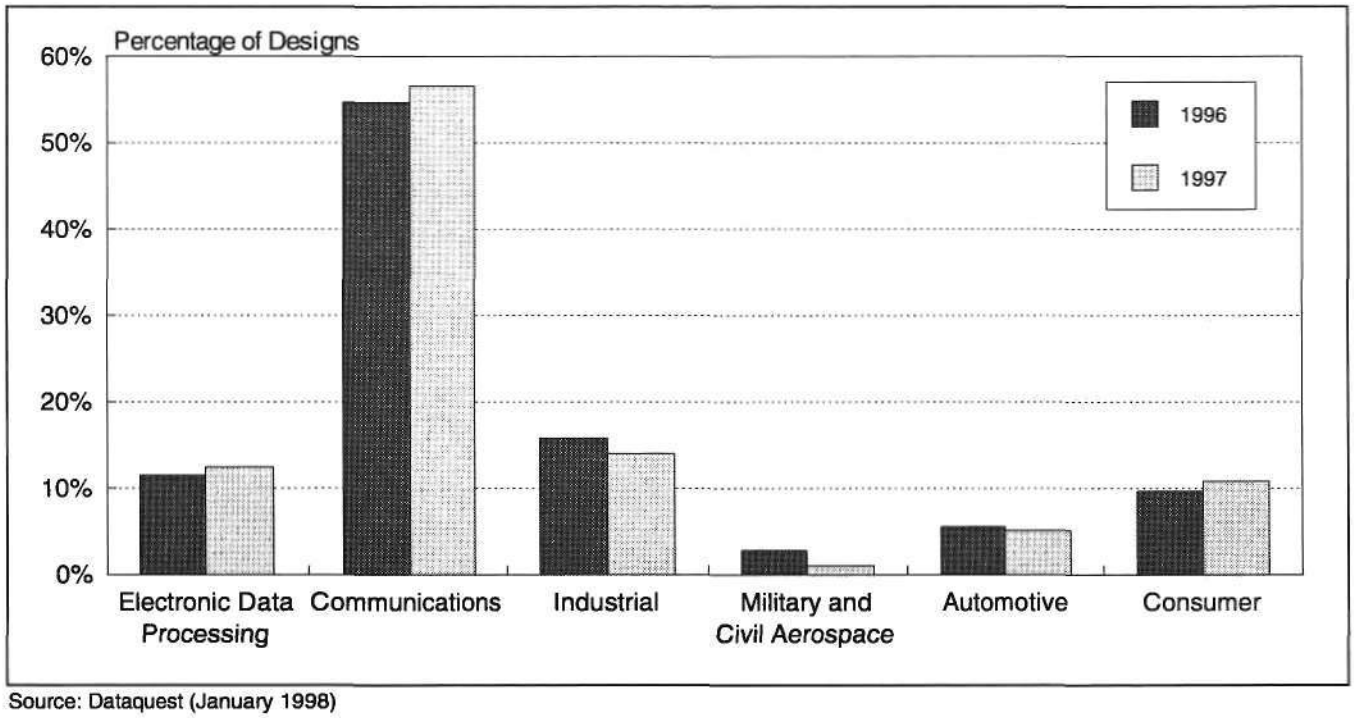
Figure 3
ASIC Design Starts by Product—Europe, 1996 and 1997



Source: Dataquest (January 1998)

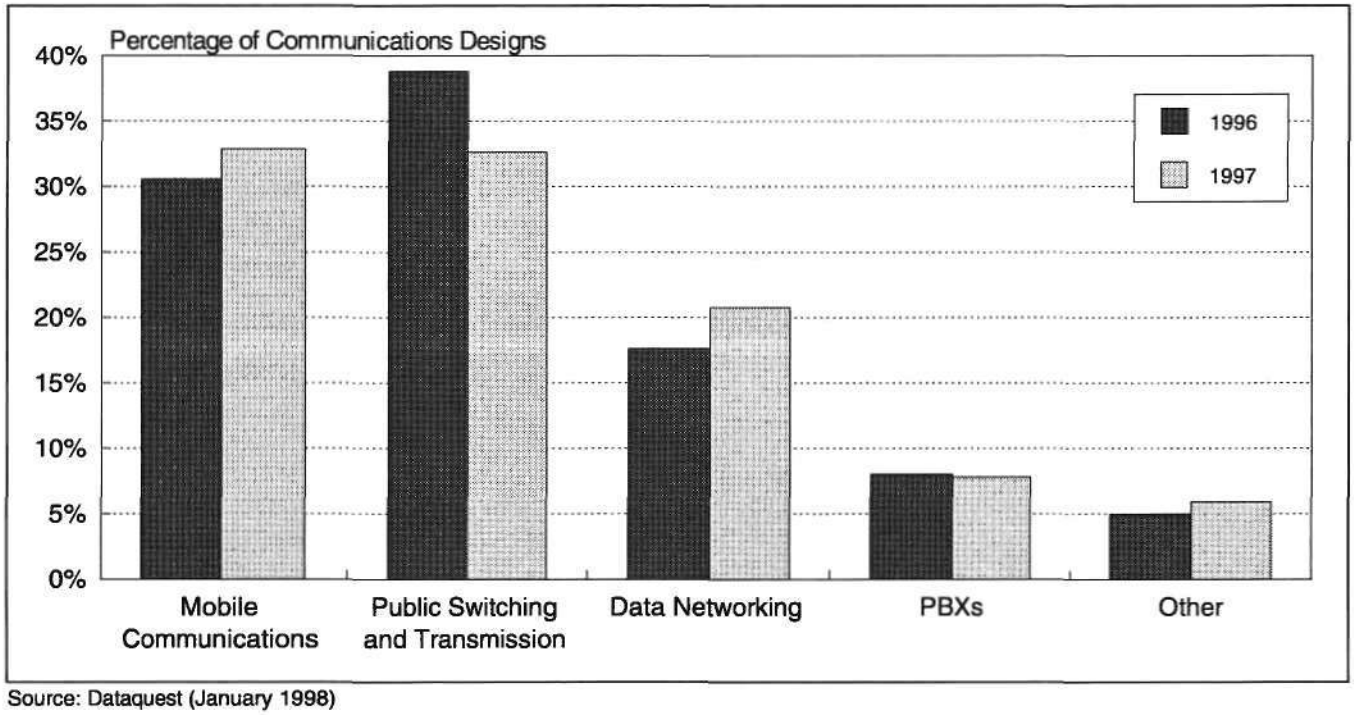
The industrial sector accounts for the second-largest block of designs, falling slightly from 16 percent to 14 percent over the period. This sector consumes many ASIC devices and is responsible for a significant number of design starts, but the designs are typically of lower complexity and relatively low value. Traditional gate arrays are frequently used in industrial applications. Both the electronic data processing and consumer sectors saw an increase in design starts over the period. The increase in electronic data processing is of little surprise and tends to mirror PC market growth. Consumer sector growth is more significant and is a sign of the accelerating digitization of consumer products. A significant amount of design activity has been occurring in various consumer products, including digital set-top boxes and even digital cameras, many of which are destined for manufacturing outside Europe. These application trends are consistent with the results of Dataquest's annual procurement survey of major semiconductor buyers as discussed in a User Wants and Needs report titled *European Semiconductor Purchasing Trends, 1997-1998* (SEMI-EU-UW-9701).

Figure 4
ASIC Designs by Application Market—Europe, 1996 and 1997



Source: Dataquest (January 1998)

Figure 5
ASIC Communications Designs by Category—Europe, 1996 and 1997



Source: Dataquest (January 1998)

Increasing Complexity

Device complexity continues to rise as demonstrated by several metrics, as follows.

- *Gate counts continue to rise.* The median gate count in 1997 is projected to rise by 25 percent from 148,000 to 184,000 gates. However, this is a misleading figure in view of the skew introduced by a relatively small number of designs containing a very large gate count. Clearly, the survey shows a continuation of the trend toward increased gate counts (see Figure 6). However, the single largest category is still "less than 50,000 gates," with 41 percent of all design starts in 1996. (Note also that Figure 6 has a nonlinear horizontal scale).
- *Feature sizes continue to fall.* 0.5-micron geometry still accounts for the largest category of design starts (see Figure 7). In 1996, 0.5-micron geometry dominated designs, with almost twice as many designs as the second-largest category—0.8 micron. In 1997, the gap closed considerably, with the second-largest category, 0.35 micron, representing a definite shift downwards. Designs at 0.35 micron are becoming mainstream, growing from 8 percent of designs in 1996 to 29 percent of designs in 1997. This year also shows the start of 0.25-micron designs.
- *Interconnect levels increase.* The number of metal interconnect levels has risen again such that three-level metal accounts for more design starts than other categories (see Figure 8). At the high end of the market, five-level metal has continued to gain share, accounting for 6 percent of all designs in 1997. Interestingly, a few vendors are involved in four-level metal designs.

System-Level Integration Steps Forward

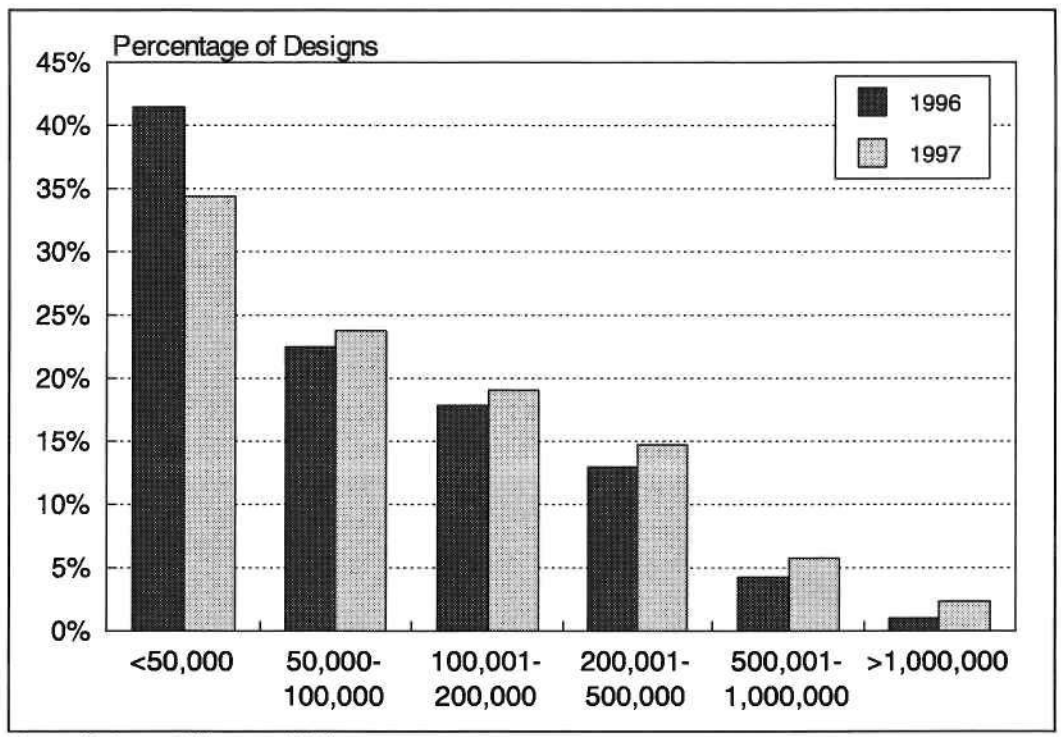
Dataquest's definition of an SLI design includes all designs over 100,000 gates that contain a compute engine (micro or digital signal processing, or DSP core), memory, and user logic. In 1997, 277 design starts are designated as SLI designs, a rise of 147 percent over 1996 (see Figure 9). These designs are undertaken by a handful of vendors and are still a small minority of all European designs. Even so, the percentage of SLI designs will rise from 9 percent of all designs in 1996 to 21 percent in 1997. Dataquest believes this figure will continue to rise to a point at which SLI designs will dominate the ASIC market within a period of three years.

The availability of cores and the technology to design cores into a device are critically important prerequisites for vendors wishing to move into the SLI market. The availability and use of cores has been increasing for several years and the survey further demonstrates this (see Figure 10). Dataquest has increased the number of core types in this year's survey to nine categories. SRAM, ROM, and microcontroller cores are by far the most commonly used, in view of the large number of embedded applications for these devices. These three categories are also the most mature, having been available for some years. Microcontroller cores, in particular, are exhibiting strong growth, with much interest in ARM and several ASIC vendor-owned

cores. DSP is another high-growth core, with accelerating growth between 1995 and 1997. In 1997 alone, the number of designs containing DSP cores will grow by 99 percent in applications such as cellular handsets, GSM base stations, and set-top boxes. Some of these applications are also responsible for the consumption of specialized cores such as ATM and MPEG, which are also showing significant growth. Embedded DRAM in ASICs is an expensive technology in view of the technical difficulties of combining high-level logic and DRAM processes, yet the benefits for memory-intensive applications are considerable considering the area efficiency of DRAM. This technology is offered by very few vendors at present but is already contained in 3 percent of designs.

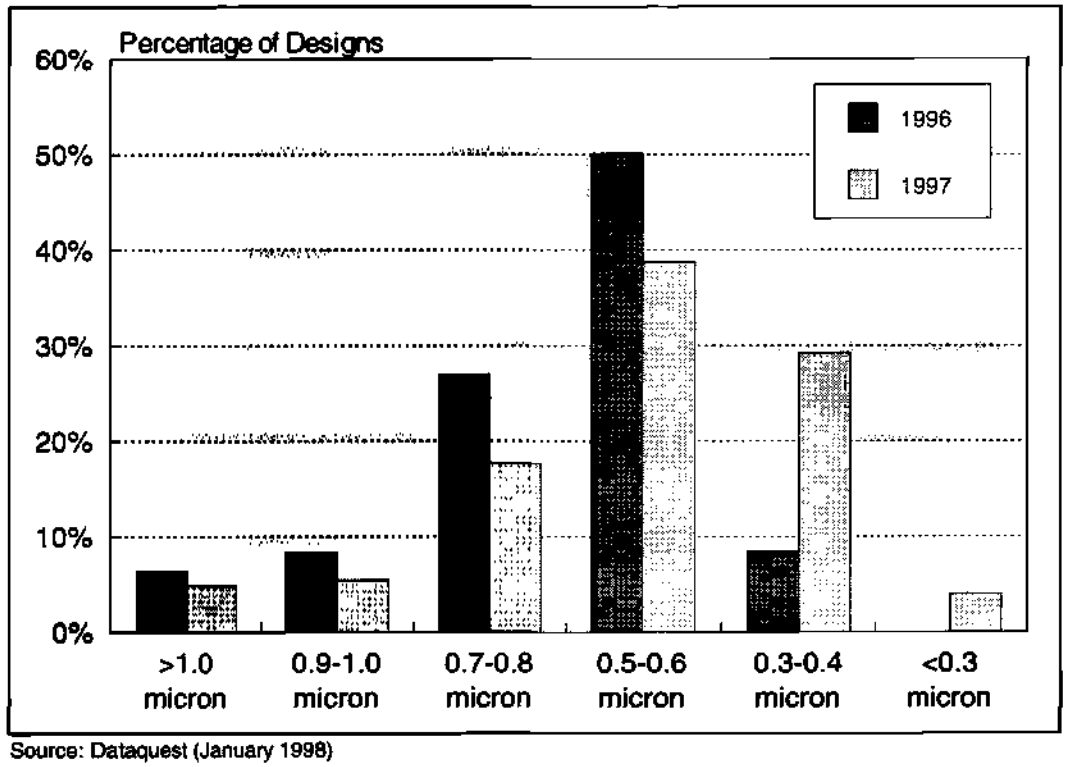
Cores are an area of intense interest to ASIC vendors and OEMs; their availability is a key differentiator for ASIC vendors. Appropriate use of cores can reduce an OEM's time to market and, therefore, make the difference between profit and loss in the final product. As a result, cores represent an increasing percentage of the value of both ASICs and end systems, with some cores often commanding selling prices of more than $1 million. The use of previously designed blocks is also the only way to use fully the tens of millions of transistors in the latest devices.

Figure 6
ASIC Designs by Gate Count—Europe, 1996 and 1997



Source: Dataquest (January 1998)

Figure 7
ASIC Designs by Feature Size—Europe, 1996 and 1997

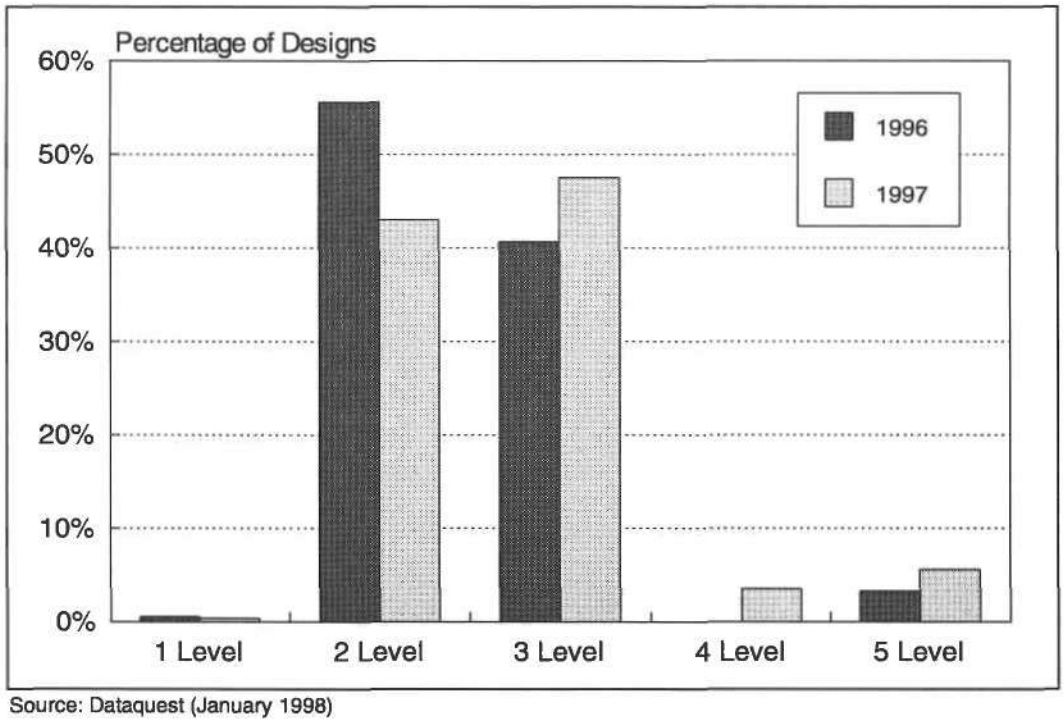


Source: Dataquest (January 1998)

Country Distribution

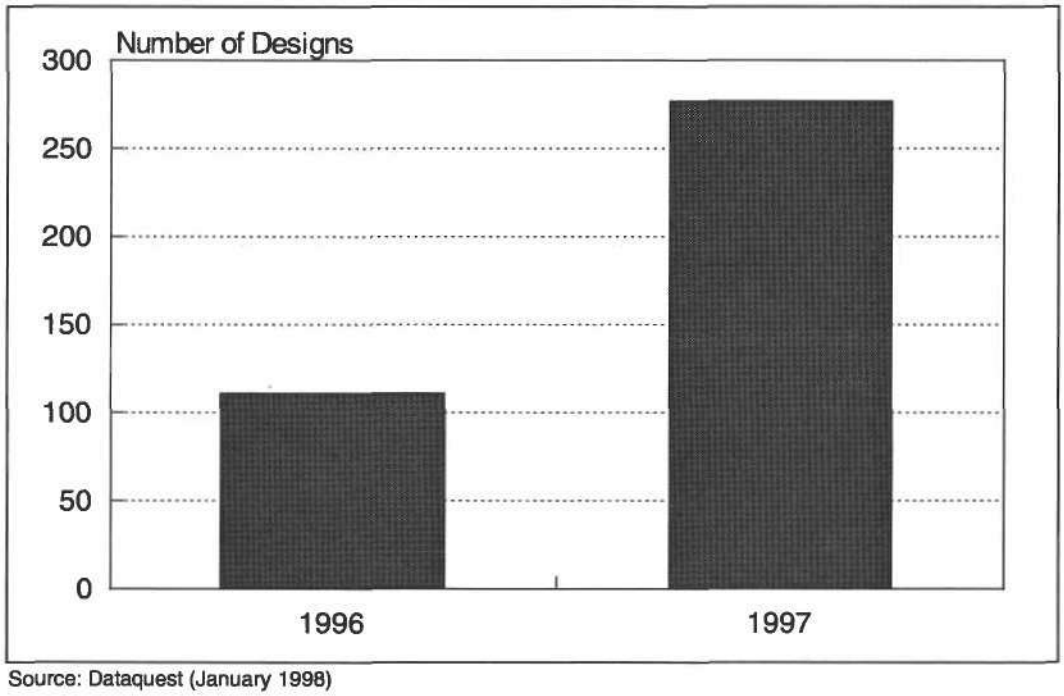
The percentage of designs reported by European country or region is shown in Figure 11. Germany continues to account for the largest number of designs, followed by the United Kingdom. The German market has continued its growth for a second year, led by its telecommunications sector, following two or three years of relative decline. In the United Kingdom a considerable amount of design activity in the computer, mobile communications, and data communications sectors was helped by the strong domestic economic climate. The only fall in design starts occurred in Benelux; design starts in all other countries and regions grew. Nordic fell in terms of percentage of design starts but grew in terms of number of designs. Italy showed the strongest percentage growth in number of designs, followed by the United Kingdom. In Italy, a strong automotive electronics sector boosted the figures, but Italy is a fragmented and turbulent market with many small electronics businesses and few large companies; the sharp rise in designs follows last year's survey in which Italy's design starts fell more than any other country.

Figure 8
ASIC Designs by Metal Interconnect—Europe, 1996 and 1997



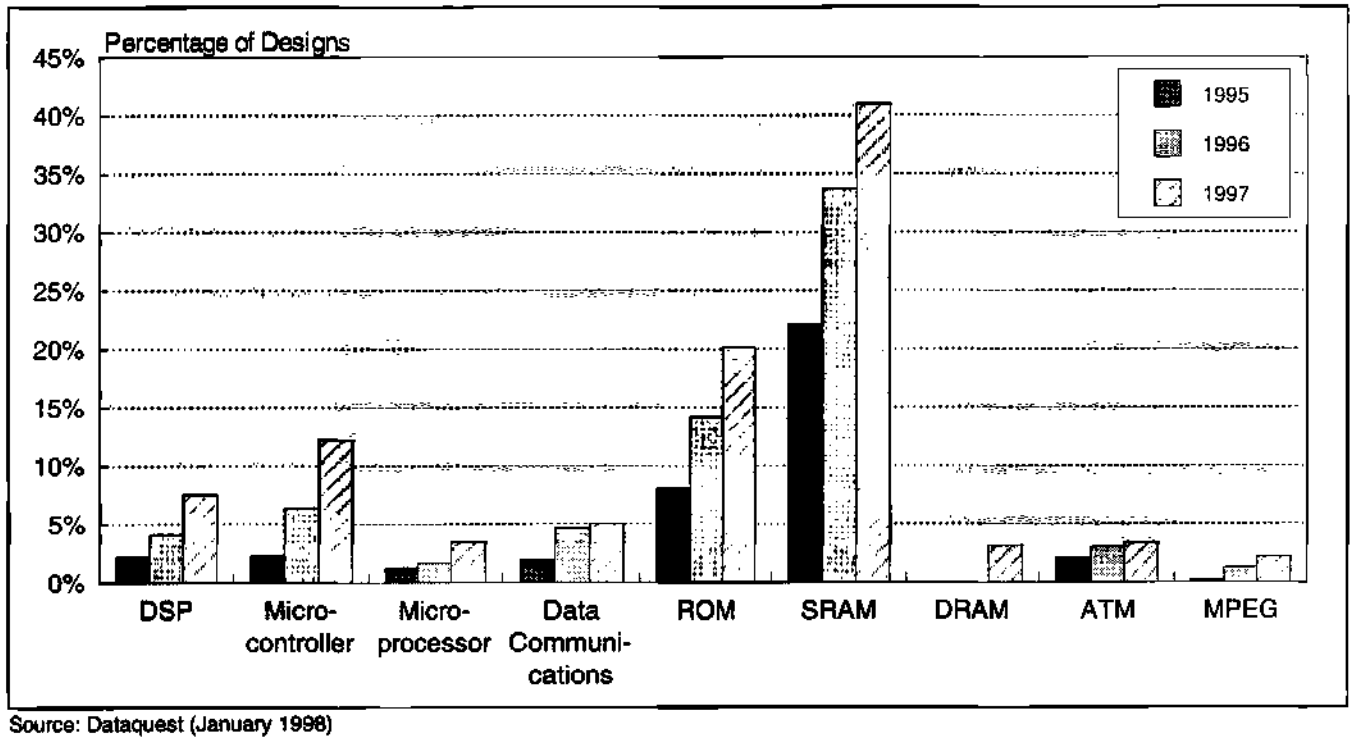
Source: Dataquest (January 1998)

Figure 9
Number of System Level Design Starts—Europe, 1996 and 1997



Source: Dataquest (January 1998)

Figure 10
ASIC Designs by Core/Macro Usage—Europe, 1995-1997

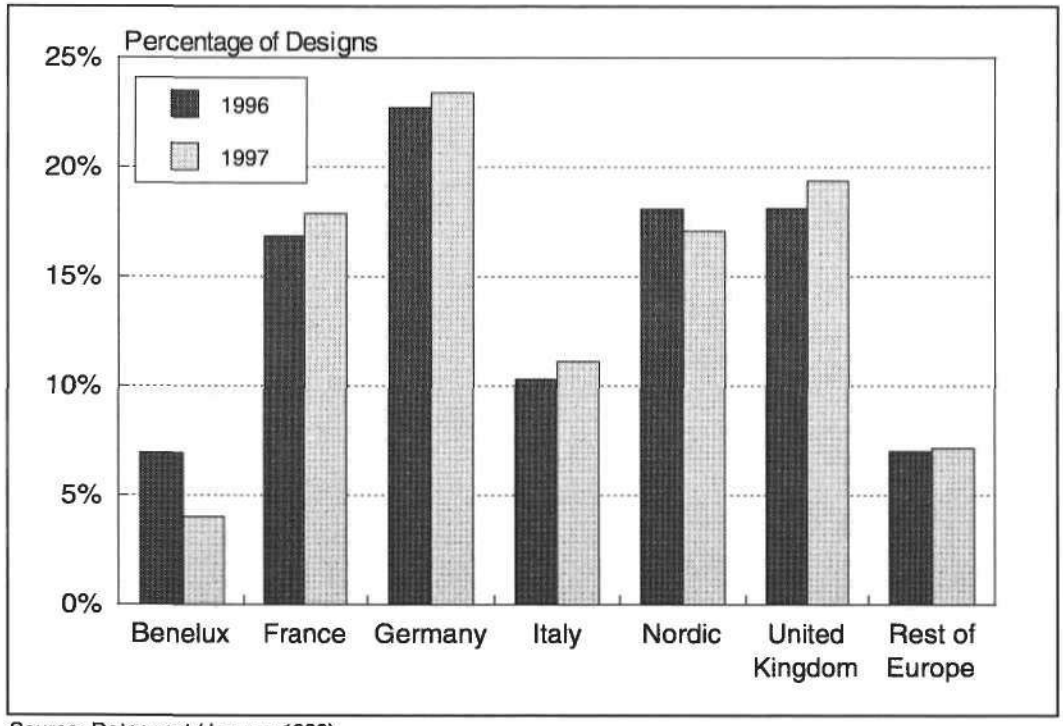


Source: Dataquest (January 1998)

Digital Leads the Way

Digital designs continue to account for the bulk of ASIC design starts in Europe. However, mixed-signal technology has long been of growing importance in Europe, mainly because of the requirements of the telecommunications sector. The gap is continuing to narrow, with mixed-signal design starts approximately one-third of the number of digital designs in 1997 (see Figure 12). Most of the mixed-signal design starts are associated with mobile communications but this could change under the influence of SLI in the drive to single-chip solutions. If this trend was to continue indefinitely, most ASICs would ultimately be mixed signal because most systems must interface with real-world signals of speech, vision, and so on. However, many OEMs are reluctant to introduce analog elements into their primary ASICs, preferring instead to employ separate analog/RF devices. This solution may be less than optimal in terms of integration, reliability, and printed circuit board (PCB) area, but it gives maximum flexibility to choose the most competitive vendor or foundry throughout the life of the product.

Figure 11
ASIC Designs by Country or Region—Europe, 1996 and 1997

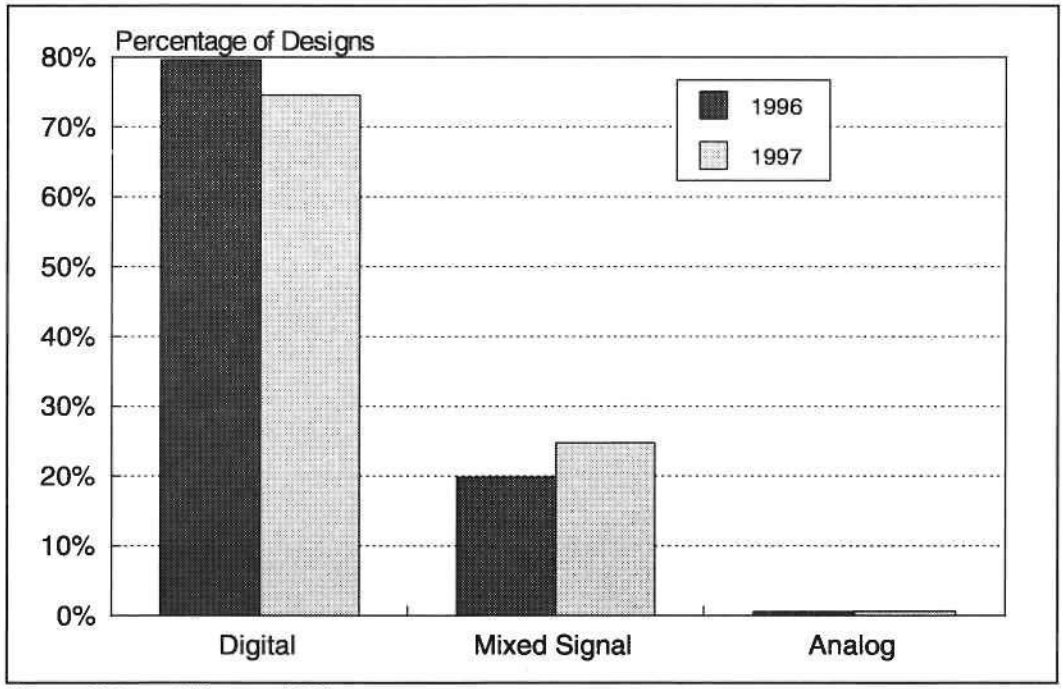


Source: Dataquest (January 1998)

Dataquest Perspective

Yet again, no downturn in ASIC design activity in Europe was evident. Instead, there were rises in numbers of designs and complexity of designs, more use of macros, and greater numbers of mixed-signal designs. The demand for more highly complex ASICs designed in a shorter time seems to be inexhaustible. This is a positive indicator for the ASIC market, yet ASIC vendors and OEMs are feeling the strain—the main limiting factors are design engineers and design tools. The rate at which new design centers have been locating in Europe has been incredible—the DRAM vendors are the latest entrants to establish design operations with an eye to better using fab capacity for high-value ASICs while developing embedded DRAM technology. OEM demand for ASIC designers also continues to rise sharply, yet the supply of engineers is not keeping pace. One solution is the greater use of cores and more effective overall reuse of designs and design elements. This is a good solution for low-speed, low-technology applications but does not work for 200-MHz designs at 0.25 micron. Here, the engineering effort to integrate cores in the form of hard macros is very complex, requiring highly skilled engineers and expensive software tools. The skill shortage is a major problem that is likely to get worse before it gets better.

Figure 12
Digital, Mixed-Signal and Analog ASIC Designs—Europe, 1996 and 1997



Source: Dataquest (January 1998)

The shortage of engineers is one reason that many OEMs have formed design houses, operating on a contract basis to fill the gap for OEMs during peak loads. Engineers can often earn higher salaries in this way than by working for a permanent employer. These design houses are thriving in Europe to a greater extent than in any other region of the world and are an essential ingredient in the success of many companies involved in ASIC design.

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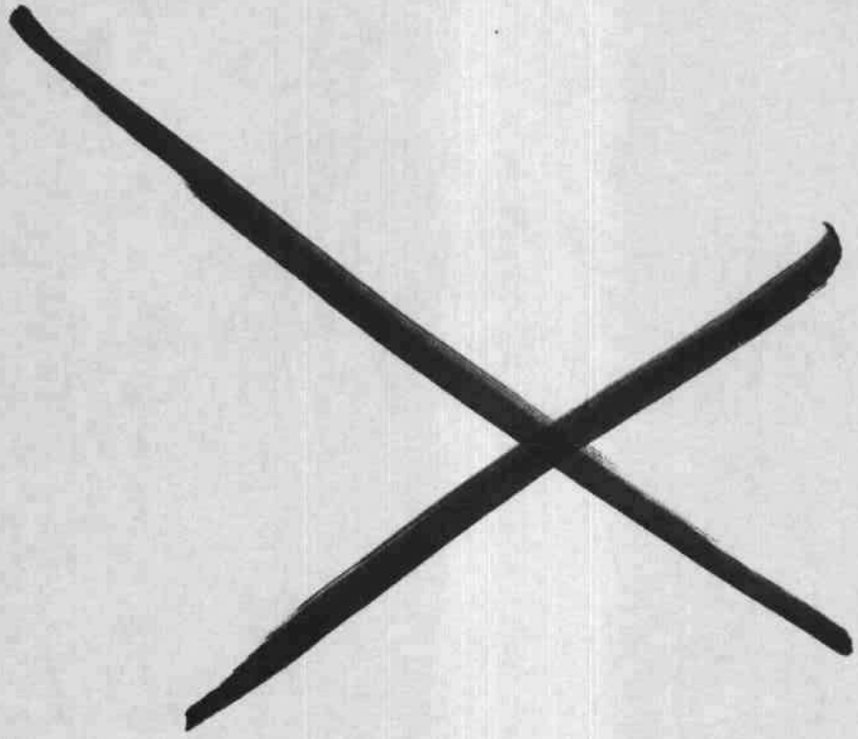

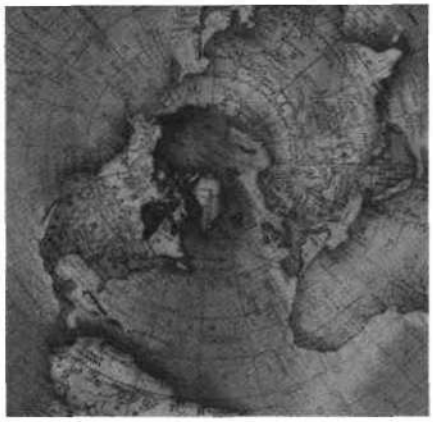

Dataquest

ASIC Suppliers Target System-Level Integration

Market Trends

Program: ASIC/SLI Worldwide
Product Code: ASIC-WW-MT-9801
Publication Date: April 16, 1998
Filing: Market Trends

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Chapter 1
Executive Summary

The dream of system-level integration (SLI), or "system on a chip," is now a reality. Dataquest estimates the 1997 SLI ASIC market at $3 billion, with a target of $21 billion by 2002. Today's market enablers of SLI are as follows:

- Advanced manufacturing, including 0.35 micron and below
- Commercial microprocessor and digital signal processor (DSP) cores such as ARM and MIPS
- Comprehensive cell libraries dedicated to specific applications
- Efficient memory, including SRAM and DRAM

Future areas of SLI that must be developed include:

- New, improved CAD tools
- Possibly a new design language for the next level of system integration
- Standards for cell compatibility from supplier to supplier

With the 0.35-micron drawn process, system designers can effectively utilize up to 2 million gates. Today's 0.25-micron products offer up to 5 million gates, while 0.18-micron products being announced can deliver about 10 million to 15 million gates. Dataquest estimates that 46 percent of 1997 ASIC design starts were done with 0.35-micron drawn line rules and 4 percent with 0.25-micron design rules. In 1998, Dataquest forecasts that 3 percent of ASIC designs will be using 0.18-micron design rules, 14 percent will use 0.25-micron rules, and 46 percent will use 0.35-micron design rules. Manufacturing processes can now provide a more than ample number of gates to put the entire system on a chip. Dataquest forecasts the average ASIC count in 2002 to be around 1.3 million utilized gates.

The key to SLI is incorporating the microprocessor core or DSP core in the ASIC device. Dataquest estimates that about 16 percent of 1997 IC designs had an on-chip microprocessor core or DSP core. ARM was the dominant microprocessor core, followed by MIPS, and the PineDSPCore and OakDSPCore continue to gain market acceptance.

Dataquest has forecast the average ASIC count in 2002 to be around 1.3 million utilized gates. We believe that 30 to 50 percent of the die area will be memory. Most of today's ASIC designs use SRAM, but on-chip DRAM is beginning to emerge.

Cell-based ICs are the primary product being used for SLI designs. Dataquest estimates that there were 5,300 cell-based IC designs done worldwide during 1997 and that about 20 percent were SLI. Furthermore, we estimate that there will be about 11,500 cell-based IC designs done in 2002, and about 60 percent will be SLI, meaning that they will have an on-chip microprocessor or DSP core. About 40 percent of the total 1997 ASIC design starts were in the data processing sector, 35 percent in communications, and 15 percent in consumer.

Project Analyst: Bryan Lewis

Chapter 2
Methodology and Definitions

Methodology

Dataquest uses both primary and secondary sources of information to produce market statistics, forecasts, and market trends. We use measures of both demand-side and supply-side data in the forms of surveys and audits. Dataquest analysts have many years of experience applying this information—in conjunction with opinions developed through industry contacts—to get the most accurate information possible.

Demand-Side Data

Dataquest demand side (end-user) data is gathered using extensive survey techniques. End users are identified through the registered user and prospect lists of ASIC and EDA companies and respective periodicals. Surveys were distributed throughout the Americas region and Japan, enabling Dataquest to gather a snapshot from a user point of view of the current and future system design requirements and the applications driving the ASIC usage. Relying upon Dataquest's international expertise, surveys distributed in Japan were translated into kanji, the Japanese character set, in order to improve the survey's accuracy. Dataquest received statistically significant numbers of responses in all areas and bases current and future end-user system trends upon this data.

For more information on demand-side data, please see our User Wants and Needs report.

Supply-Side Data

Dataquest supply-side data is gathered by surveying ASIC suppliers with highlv detailed questionnaires. Dataquest receives input from most of the leading ASIC suppliers, which account for more than 70 percent of the ASIC market. The information was then compiled and audited on a corn-pann, basis. The aggregate trends were then cross-checked for accuracy with ASIC demand-side information as well as with system information derived from other Dataquest services.

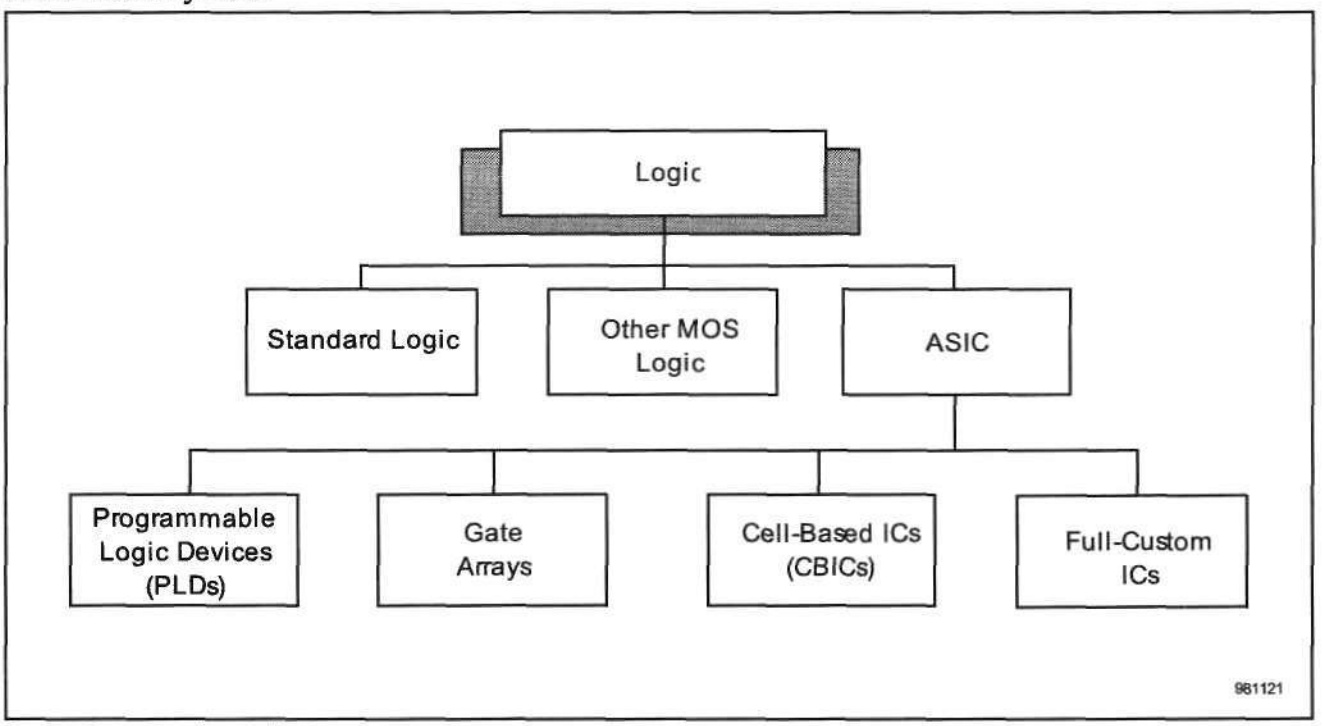
We believe that the information presented in this report is the most accurate information available today.

Definitions

Dataquest defines the ASIC market according to the segmentation scheme shown in Figure 2-1.

Dataquest segments logic into the two main categories: standard logic and ASIC. The ASIC family tree breaks down into PLDS, gate arrays, CBICS, and full-custom ICs. CBICs and full-custom ICs are customized by altering the full set of masks, whereas PLDs and gate arrays are customized by electrically programming the devices or by altering only the final layers of interconnect.

Figure 2-1
ASIC Family Tree



Source: Dataquest (March 1998)

Product Definitions

The following are definitions used in this document.

- Application-Specific Integrated Circuits (ASICs): This term is used to describe all IC products customized for a single user. ASIC products are a combination of digital, mixed-signal, and analog products. Customized ICs purchased by more than one user become standard products and are no longer counted as ASICS.
- Programmable Logic Devices (PLDs): PLDs are defined as ICs programmed after assembly. Memory devices such as PROMs and ROMs are not included in this market segment. PLDs are subdivided into two main categories as follows:
  - Simple Programmable Logic Devices (SPLDs): These devices have fixed or preconnected architectures capable of providing up to two levels of logic without using additional I/0 cells or pins.
  - High-Density PLDs: Included in this category are FPGAs and CPLDs.
- Gate Arrays: Gate arrays are ASICs that contain a configuration of uncommitted elements in a prefabricated base wafer. They are customized by interconnecting these elements with one or more routing layers. Included in this category are traditional gate arrays (channeled and sea-of-gates architecture) and embedded gate arrays (channeled or sea-of-gates architecture that also includes megacells such as SRAM diffused into the gate array base wafer).

- Cell-Based ICs (CBICs): CBICs are ASICs that are customized using a full set of masks and use automatic place and route tools. Included in this category are traditional standard cells (fixed-height/fixed-width cells), as well as megacells (variable-height/variable-width cells) and compiled cells.
- Full-Custom ICs: Full-custom ICs are defined as ASICs customized using a full set of masks and using manual place and route.

SLI Definition

At its October 1995 Semiconductor Conference, Dataquest introduced a new term and area of research to the industry-system-level integration (SLI). Other terms used in the industry today that have a similar meaning include "system on a chip" or "systems on silicon." We have not chosen these terms because they imply that the system is hardware only. We strongly believe that future system design will include hardware/software co-design, so we have chosen a broader term that emcompasses both elements. This document focuses on the hardware portion of the market, and we define the hardware market as follows:

- System-Level Integration: An integrated circuit that contains a compute engine, memory, and logic on a single chip.

There are two types of SLI devices: ASICs (application-specific integrated circuits that are sold to a single user) and ASSPs (application-specific standard products that are sold to more than one user).

Consumption and Revenue Definitions

Because systems may be fabricated, assembled, and sold in different locations, Dataquest regional device consumption is defined as the region where the device is assembled on the printed circuit board.

Consumption and revenue estimates include the following five sources of revenue:

- Intracompany revenue (sales to internal divisions)
- Nonrecurring engineering (NRE) revenue
- ASIC software revenue
- PLD development kit revenue
- Device production revenue

Dataquest includes all revenue, both merchant and captive, for semiconductor suppliers selling to the merchant market. Dataquest's consumption estimates do not include captive-only manufacturing companies represented by companies such as Digital Equipment Corporation, Northern Telecom Inc., or Unisys Corporation, which do not sell semiconductor products in the merchant market.

Despite the care taken in gathering, analyzing, and categorizing the data in a meaningful way, careful attention must be paid to the definitions and assumptions used herein when interpreting the estimates presented in this report. Various companies, government agencies, and trade associations may use slightly different definitions of product categories and regional groupings, or they may include different companies in their summaries. These differences should be kept in mind when making comparisons between data and numbers provided by Dataquest and those provided by other suppliers.

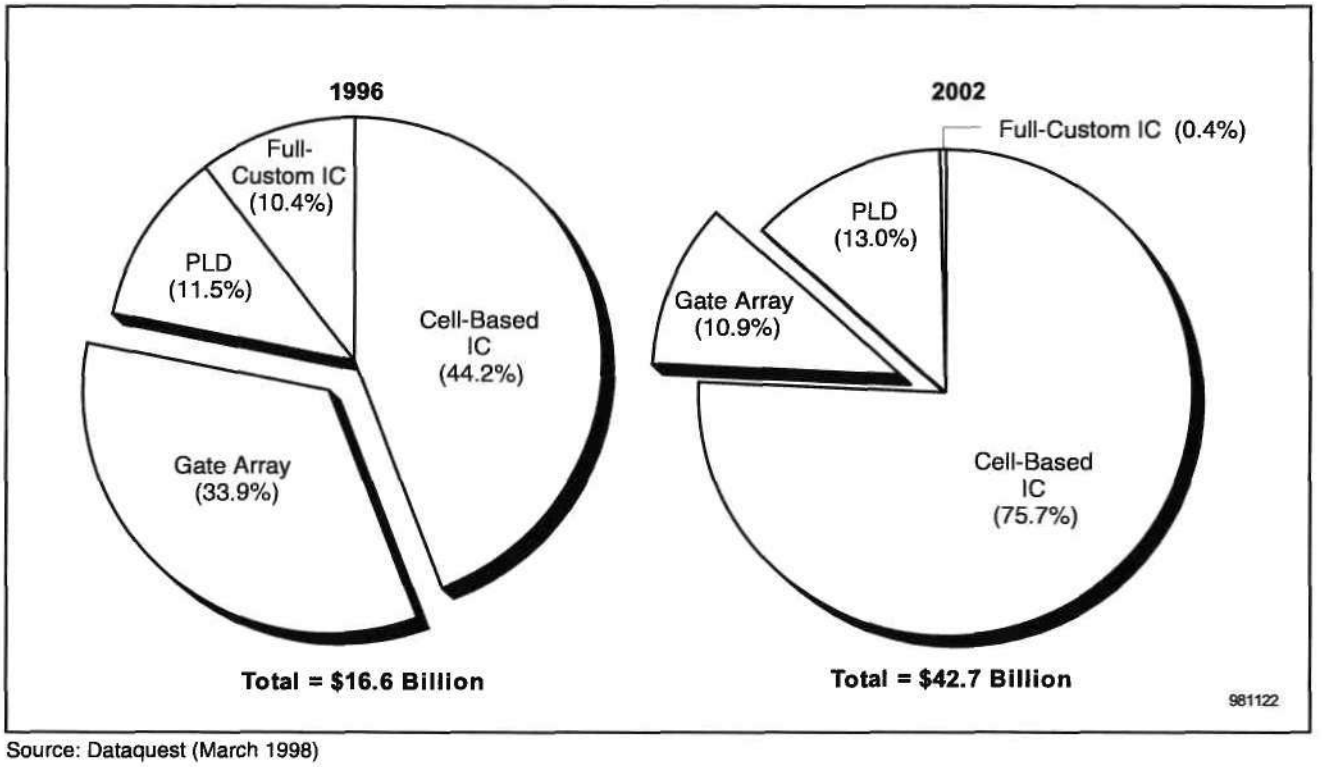
Chapter 3
ASIC/SLI Consumption Forecasts

The ASIC market is in a state of flux. Gate arrays, once the dominant product, are rapidly being replaced by cell-based ICs and PLDs. System-level ASICs targeted at specific applications are entering the mainstream, and generic ASICs are starting to fade. Figure 3-1 shows the rapid erosion of gate array market share and the dominance of cell-based ICs in 2002. PLDs gain some market share in 2002, also at the expense of the gate array market.

ASIC Forecast

At the time of this report, Dataquest's final market share estimates were not complete, so this report provides a preliminary ASIC forecast, shown in Table 3-1, that will be updated in April or May. Preliminary 1997 market data shows that the cell-based IC market will indeed have grown around 29 percent, as previously forecast, but the gate array market may have declined more than the 1 percent that was forecast. The PLD market was forecast to grow around 18 percent in 1997, and preliminary data shows that it grew closer to 13 percent, as shown in the updated PLD forecast in Table 3-1. Table 3-2 shows the preliminary PLD forecast by logic complexity. For the PLD industry, 1998 will be a tough year, with simple PLDs expected to decline about 17 percent and high-density PLDs forecast to grow around 16 percent—the lowest growth in PLD history.

Figure 3-1
Estimated Worldwide ASIC Consumption by Product



Source: Dataquest (March 1998)

Table 3-1
Estimated Worldwide ASIC Consumption—Preliminary, 1995 to 2002 (Millions of Dollars)

	1995	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Total ASIC	15,567	16,554	18,436	21,544	25,633	30,893	36,318	42,735	18.3
Gate Array	5,977	5,609	5,571	5,544	5,450	5,291	5,049	4,645	-3.6
PLD	1,701	1,904	2,144	2,406	2,999	3,703	4,481	5,553	21.0
Cell-Based IC	5,747	7,317	9,467	12,552	16,472	21,420	26,490	32,358	27.9
Full-Custom IC	2,142	1,724	1,254	1,041	711	479	298	179	-32.3

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (March 1998)

Table 3-2
Estimated Worldwide PLD Consumption by Logic Complexity—Preliminary, 1995 to 2002 (Millions of Dollars)

	1995	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Total CMOS PLD	1,701	1,904	2,144	2,406	2,999	3,703	4,481	5,553	21.0
Total SPLD	403	316	271	224	178	139	100	65	-24.8
Total High-Density (CPLD and FPGA)	1,298	1,588	1,873	2,182	2,821	3,564	4,381	5,488	24.0

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (March 1998)

SLI ASIC Forecast

System-level ASICs are the fastest-growing product in the ASIC industry. Dataquest is doing extensive research in the SLI ASIC area. Table 3-3 and Figure 3-2 show Dataquest's preliminary SLI ASIC forecast. This forecast was generated using the following:

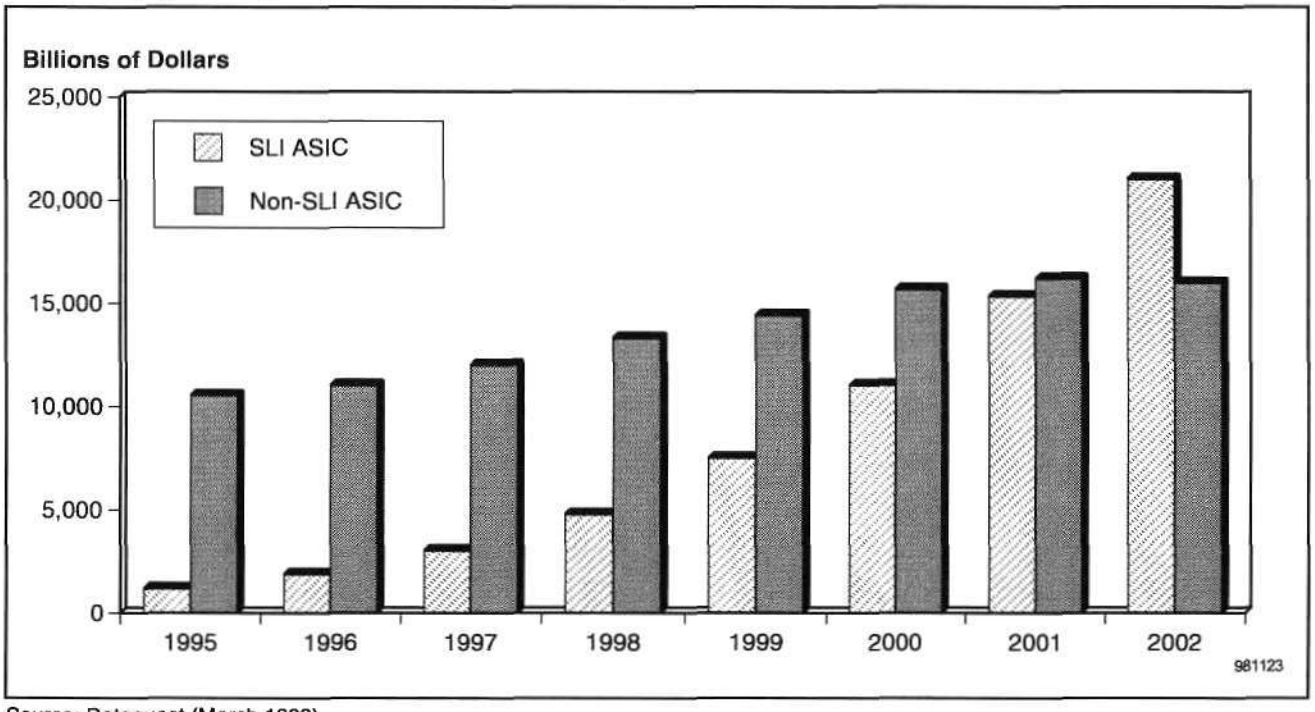
- Bottom-up estimates made by suppliers
- Top-down estimates made by looking at the percentage of ASIC products going to SLI
- Applications driving the SLI market demand

Table 3-3
Estimated Worldwide SLI ASIC (Gate Array and Cell-Based IC) Consumption by Logic Complexity—Preliminary, 1995 to 2002 (Millions of Dollars)

	1995	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
SLI ASIC	1,180	1,891	3,026	4,780	7,505	11,033	15,336	21,010	47.3
Non-SLI ASIC	10,544	11,035	12,012	13,316	14,417	15,678	16,203	15,993	5.9

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (March 1998)

Figure 3-2
Preliminary Worldwide SLI ASIC Market



Source: Dataquest (March 1998)

Dataquest's previous SLI ASIC forecast showed the 1997 market at about $3.8 billion. Bottom-up data by supplier from ASIC companies and ASIC divisions within broad-based semiconductor companies shows that the 1997 SLI ASIC market totaled about $3 billion. This $3 billion is based on ASIC products being shipped that incorporate on-chip microprocessor or DSP cores from ASIC companies and ASIC divisions. Leading SLI ASIC companies include LSI Logic Corporation, IBM, VLSI Technology Inc., Lucent Technologies, NEC Corporation, Texas Instruments Inc., Motorola Incorporated, Hitachi Ltd., Toshiba Corporation, and Fujitsu Ltd. Both LSI Logic and VLSI Technology are making a name in the SLI ASIC market by being the earliest to push third-party on-chip microprocessor cores such as MIPS and ARM and third-party DSP cores such as the DSP Group's Pine and Oak. If all the products were counted that include sole-source DSP cores from Lucent Technologies and Texas Instruments and from DSP divisions within these companies, SLI ASIC revenue could be about $500 million higher. The reason Dataquest is not counting DSP core revenue from DSP divisions at this point is that the bulk of this revenue

consists of standard products, and the SLI ASIC numbers have not yet been determined. We believe that another part of the difference comes from the fact that the CAD tools and standards on libraries are not yet in place. We believe the industry is well aware of this and is working on the problem with consortiums such as the Virtual Socket Initiative Alliance and the Silicon Integration Initiative's ASIC Council, comprising companies including IBM, LSI Logic, Lucent Technologies, Motorola, NEC, Texas Instruments, and VLSI Technology. Dataquest believes the CAD tools and standards problems will be fixed; however, we have pushed out the growth of the SLI ASIC market about one year from the previous forecast (the previous 2001 dollar total available market, or TAM, is now close to the new 2002 TAM).

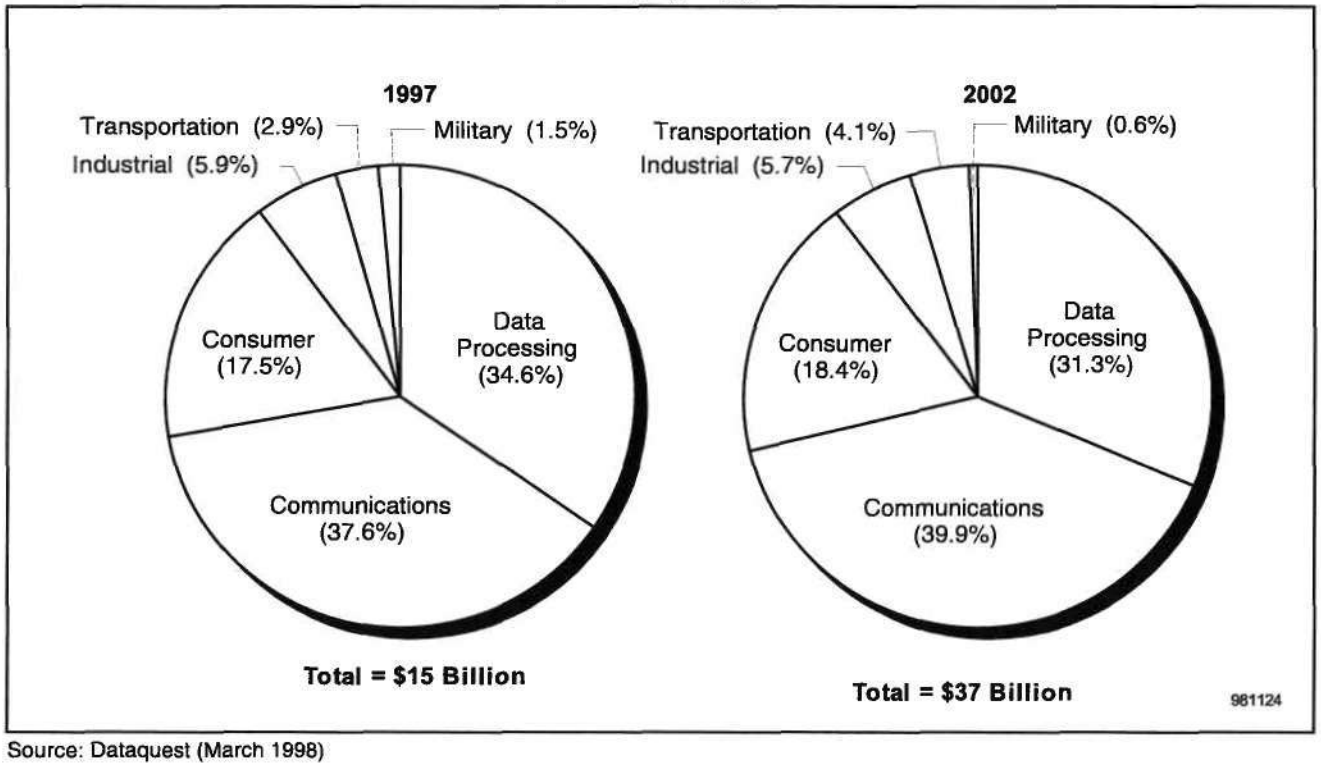
Throughout the forecast period, the majority of SLI ASICs will be cell-based ICs. In 1997, cell-based IC account for about 80 percent of the SLI ASIC market, with gate arrays around 20 percent. In 2002, cell-based ICs account for about 95 percent and gate arrays for the remainder. About 20 percent of the 1997 cell-based IC market is SLI, moving to 60 percent in 2002. We believe that about 40 percent of the 1997 SLI ASIC market is in the communications sector, 30 percent in data processing, and 30 percent in consumer. The highest revenue per design was in the Sony PlayStation, with more than $200 million in 1997, but there are far more designs in the telecommunications and data communications sectors.

Chapter 4
Application Trends

To get a better understanding of the size of the ASIC application markets, Dataquest polled the leading ASIC suppliers about their application mix. These application percentages were then rolled up to get aggregate trends for the ASIC industry. Figure 4-1 shows that communications was the largest market worldwide for ASICs in 1997, followed by data processing, then consumer. Communications remains the largest worldwide ASIC market, as shown in Tables 4-1 and 4-2. Many data processing applications are turning to ASSPs or chipsets at the expense of ASICs as the application has become more of a commodity and standards have been set.

Figure 4-2 shows that consumer and communications are experiencing rapid growth. Tables 4-3 and 4-4 show the size of the application markets in the Americas.

Figure 4-1
Estimated Worldwide ASIC Consumption, by Application Market



Source: Dataquest (March 1998)

Table 4-1
Estimated Worldwide ASIC (Gate Array and Cell-Based IC) Consumption, by Application Market, 1995 to 2002 (Millions of Dollars)

	1995	1996	1997	1998	1999	2000	2001	2002
Data Processing	4,349	4,591	5,203	6,189	7,322	8,788	10,092	11,582
Communications	3,866	4,597	5,655	6,949	8,572	10,497	12,521	14,764
Industrial	682	769	887	1,050	1,250	1,523	1,766	2,123
Consumer	2,242	2,389	2,632	3,131	3,858	4,755	5,709	6,791
Military	240	218	226	235	241	240	252	206
Transportation	345	362	436	543	680	908	1,198	1,521
Total	**11,724**	**12,926**	**15,039**	**18,096**	**21,922**	**26,711**	**31,539**	**37,003**

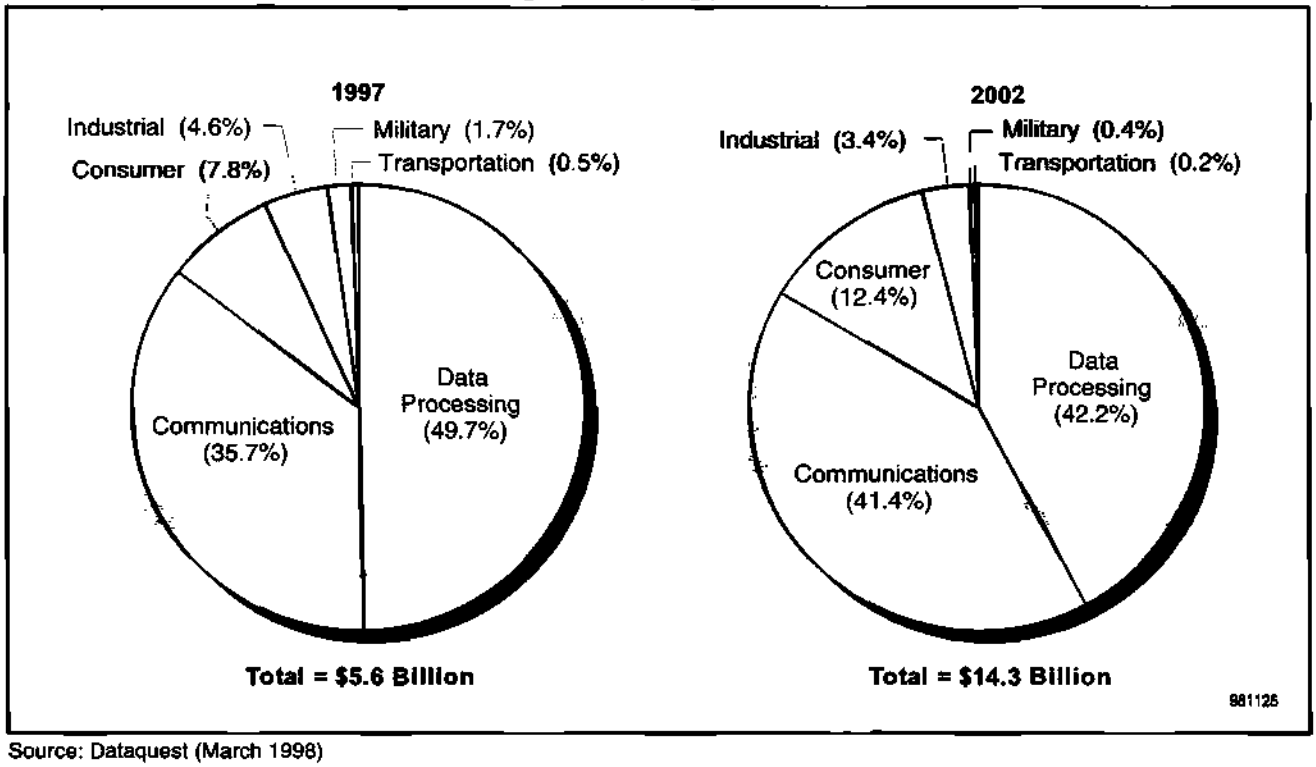
Source: Dataquest (March 1998)

Table 4-2
Estimated Worldwide ASIC (Gate Array and Cell-Based IC) Consumption, by Application Market (Percentage of Revenue)

	1995	1996	1997	1998	1999	2000	2001	2002
Data Processing	37.1	35.5	34.6	34.2	33.4	32.9	32.0	31.3
Communications	33.0	35.6	37.6	38.4	39.1	39.3	39.7	39.9
Industrial	5.8	6.0	5.9	5.8	5.7	5.7	5.6	5.7
Consumer	19.1	18.5	17.5	17.3	17.6	17.8	18.1	18.4
Military	2.0	1.7	1.5	1.3	1.1	0.9	0.8	0.6
Transportation	2.9	2.8	2.9	3.0	3.1	3.4	3.8	4.1

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (March 1998)

Figure 4-2
Estimated Americas ASIC Consumption, by Application Market



Source: Dataquest (March 1998)

Table 4-3
Estimated Americas ASIC (Gate Array and Cell-Based IC) Consumption, by Application Market, 1995 to 2002 (Millions of Dollars)

	1995	1996	1997	1998	1999	2000	2001	2002
Data Processing	2,372	2,509	2,795	3,243	3,780	4,531	5,260	6,030
Communications	1,334	1,604	2,008	2,534	3,216	4,047	4,934	5,915
Industrial	222	231	259	284	327	383	434	486
Consumer	278	342	439	574	745	1,019	1,339	1,772
Military	109	101	96	95	90	81	72	57
Transportation	30	29	28	27	25	30	24	29
Total	**4,345**	**4,816**	**5,624**	**6,757**	**8,182**	**10,092**	**12,064**	**14,288**

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (March 1998)

Table 4-4
Estimated Americas ASIC (Gate Array and Cell-Based IC) Consumption, by Application Market, 1995 to 2002 (Percentage of Revenue)

	1995	1996	1997	1998	1999	2000	2001	2002
Data Processing	54.6	52.1	49.7	48.0	46.2	44.9	43.6	42.2
Communications	30.7	33.3	35.7	37.5	39.3	40.1	40.9	41.4
Industrial	5.1	4.8	4.6	4.2	4.0	3.8	3.6	3.4
Consumer	6.4	7.1	7.8	8.5	9.1	10.1	11.1	12.4
Military	2.5	2.1	1.7	1.4	1.1	0.8	0.6	0.4
Transportation	0.7	0.6	0.5	0.4	0.3	0.3	0.2	0.2

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (March 1998)

ASIC Applications

The following section shows the specific applications for ASICs.

Data Processing

Data processing is defined as computer systems, data storage devices, I/O devices (that is, media-to-media data conversion, scanning equipment, plotters, voice recognition/synthesizer equipment), electronic printers, and office equipment (that is, copiers, duplicators, electronic calculators).

Key data processing products that consume large quantities of ASICs include:

- Workstations and personal computers
- Midrange computers, mainframes, and supercomputers
- Disk drives
- Electronic printers
- Copiers

Emerging data processing products with ASIC opportunity include:

- Portable computers
- High-density 3.5-inch disk drives
- 2.5-inch and 1.8-inch disk drives
- Video compression and decompression
- Digital video (color space conversion, image digitizing)

Subsystems within data processing products that are often implemented in ASICs include the following:

- Glue logic consolidation
- Central processing unit
- Graphics processor
- Memory manager
- I/O manager
- Disk drive controller
- Floating-point register
- Network controller
- Bus interface
- Cache controller
- MPEG-1 and MPEG-2
- SCSI and PCI
- Digital signal processing (DSP)
- PC upgrade cards (multimedia)
  - Graphics
  - Audio

Communications

Communications is defined as personal communication, networking, image communication, andf voice communication.

Applications for ASICs in the communications segment include the following:

- Cellular and cordless phones
- LAN systems
  - Network interface cards
  - Hubs
  - Switches
  - Routers
- PBX
- Central office switching systems
- Multiplexing
- Modems
- ISDN adapters
- Line cards
- Fiber-optic transmission
- Encryption
- Infrared communications
- Asynchronous Transfer Mode

Industrial

Industrial is defined as test equipment, manufacturing systems, process control equipment, instrumentation, medical equipment, and robotics.

Applications for ASICs in the industrial segment include the following:

- Automated test equipment
- Medical electronics
- Logic analyzers
- Motor control
- Robotics

Military

Military is defined as military electronic equipment.

Applications for ASICs in the military segment include the following:

- Radar
- Sonar
- Missile guidance and control
- Navigation
- Reconnaissance
- Flight simulators

Transportation

Transportation is defined as in-car entertainment systems, body control electronics, driver information, power train electronics, safety electronics, and convenience electronics.

Applications for ASICs in the transportation segment include the following:

- Navigation systems
- Automatic braking systems (ABS)
- Active suspension
- Collision avoidance systems
- Multiplex systems such as driver door and steering wheel
- Electronic instrument clusters
- Power train controls
- Engine management

Consumer

Key consumer applications include the following:

- Set-top boxes
- DVD
- Camcorders
- Digital TV
  - Standard-definition TV
  - High-definition TV
- Electronic games
- Digital still cameras
- Video CDs

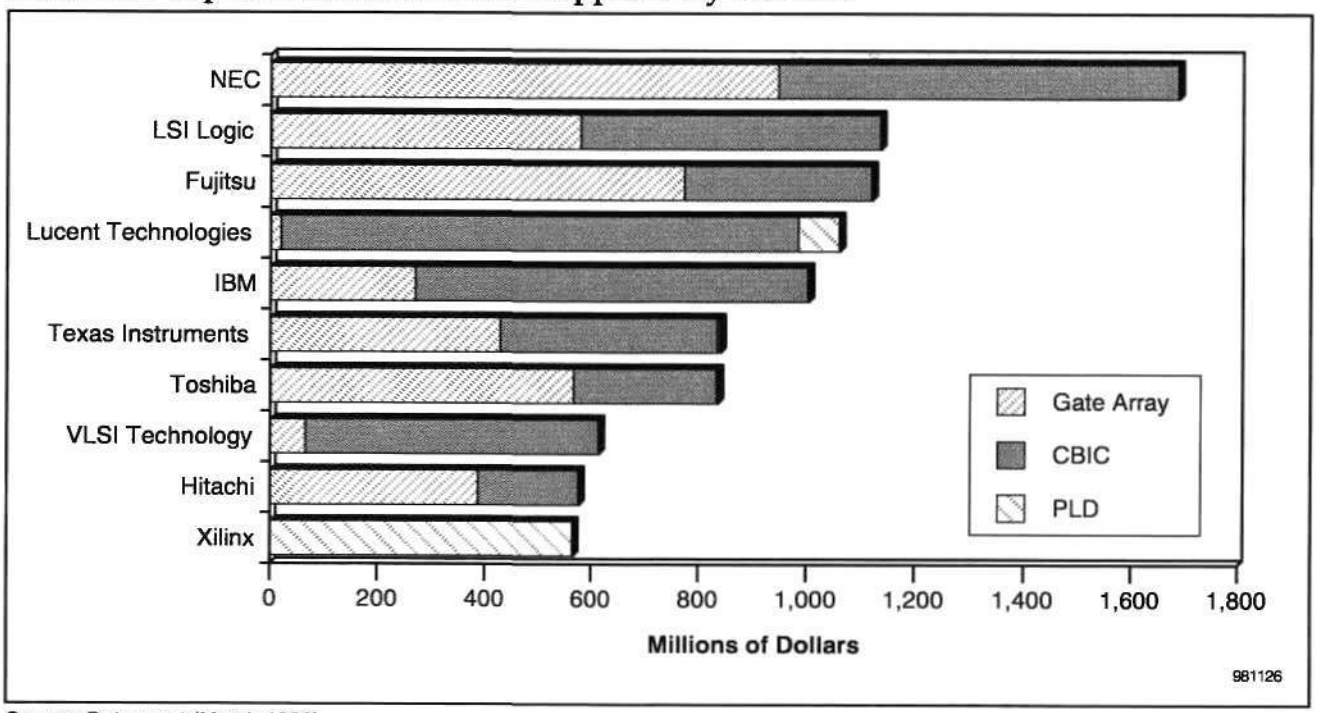
Chapter 5
ASIC Supplier Trends

At the time of this publication, Dataquest was in the process of finalizing 1997 ASIC market share. To give a more up-to-date picture of the ASIC industry, this report provides final 1996 rankings and preliminary 1997 market share data, which may change after the final ASIC rankings are determined.

ASIC Supplier Ranking

Figure 5-1 shows Dataquest's final 1996 ASIC supplier ranking by product. The leading suppliers were all focusing on cell-based IC products and emphasizing gate array products. Table 5-1 shows Dataquest's preliminary 1997 ASIC ranking. The key change in the 1997 rankings is that LSI Logic, a focused ASIC supplier, dropped in the rankings, while both IBM and Lucent moved up. IBM and Lucent are both broad-based semiconductor suppliers and vertically integrated suppliers. It was once thought that focused ASIC suppliers would dominate the market because they are more nimble. It turns out that broad-based and vertically integrated suppliers are now winning because they have large R&D budgets, standard products to turn into reusable intellectual property (IP), and much better economies of scale in manufacturing.

Figure 5-1
Final 1996 Top 10 Worldwide ASIC Suppliers by Product



Source: Dataquest (March 1998)

Table 5-1
Preliminary 1997 Top 10 Worldwide ASIC Suppliers
(Millions of Dollars)

Rank	Supplier	Revenue ($M)
1	NEC	1,836
2	IBM	1,541
3	Lucent Technologies	1,486
4	Fujitsu	1,248
5	LSI Logic	1,182
6	Texas Instruments	886
7	VLSI Technology	667
8	Toshiba	660
9	Altera	631
10	Xilinx	612

Source: Dataquest (March 1998)

Cell-Based IC Supplier Ranking

Figure 5-2 shows Dataquest's final 1996 cell-based IC ranking. Table 5-2 shows preliminary 1997 cell-based IC revenue. IBM was the big winner in 1997, moving into the No. 2 position close behind Lucent. Vertically integrated and broad-based IC suppliers such as IBM and Lucent had much larger revenue gains in 1996 and 1997 in this product than focused ASIC suppliers such as LSI Logic and VLSI Technology.

Gate Array Supplier Ranking

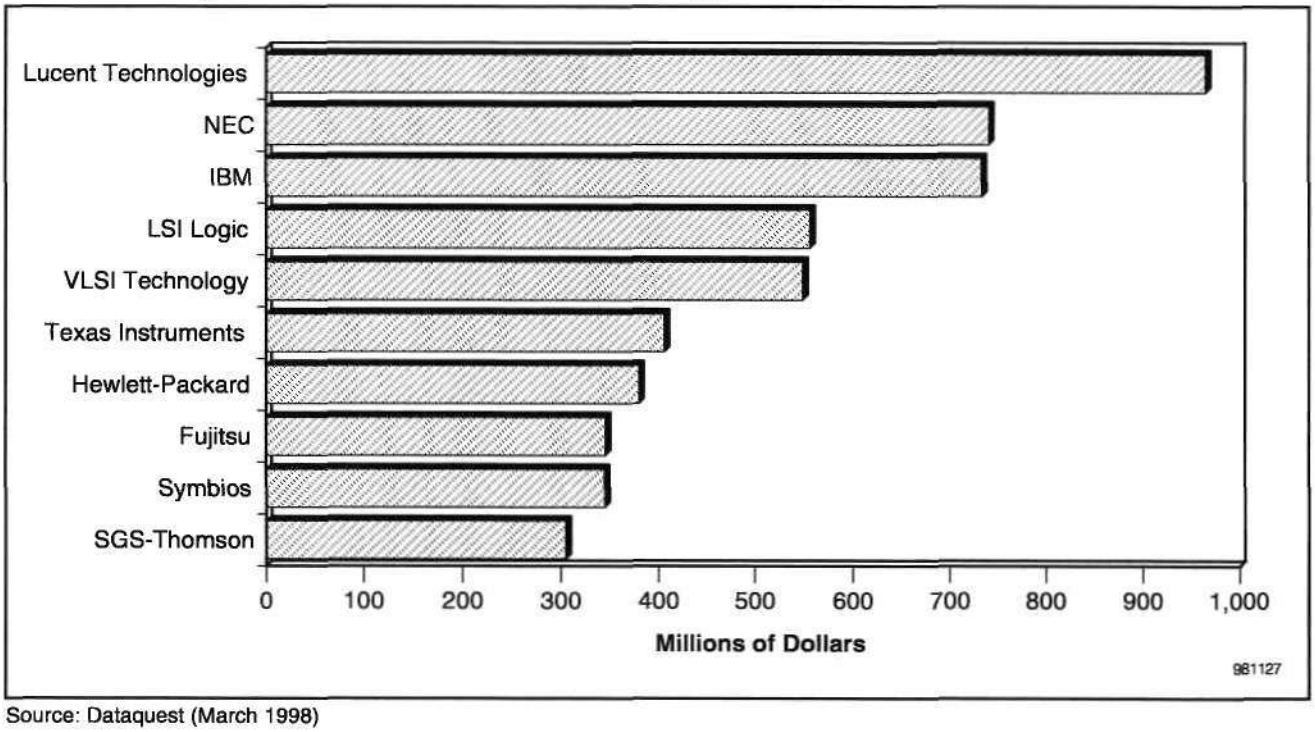
Being the top gate array supplier in a declining market does not mean much, compared to being the top cell-based IC supplier in a fast-growing market. The gate array rankings remained relatively unchanged, and most suppliers had a decline in 1997 revenue, compared to that of 1996. Figure 5-3 shows the final 1996 gate array ranking, and Table 5-3 shows preliminary 1997 gate array revenue by supplier.

PLD Supplier Ranking

Altera Corporation and Xilinx Incorporated have been in a PLD battle for more than five years. Altera became the No. 1 supplier in 1997 for the first time; however, the victory was greeted with little celebration because the PLD market did not grow nearly as much as anticipated. Figure 5-4 shows final 1996 PLD market share, and Table 5-4 shows preliminary 1997 PLD market share. Another noteworthy battle is the one between Lattice Semiconductor Corporation and Vantis; it was almost a tie for 1997, but Lattice showed much stronger growth and will most likely take the lead over Vantis in 1998.

Further information on market share rankings will be available in the worldwide ASIC market share document, to be released in May.

Figure 5-2
Final 1996 Top 10 Worldwide Cell-Based IC Suppliers by Product



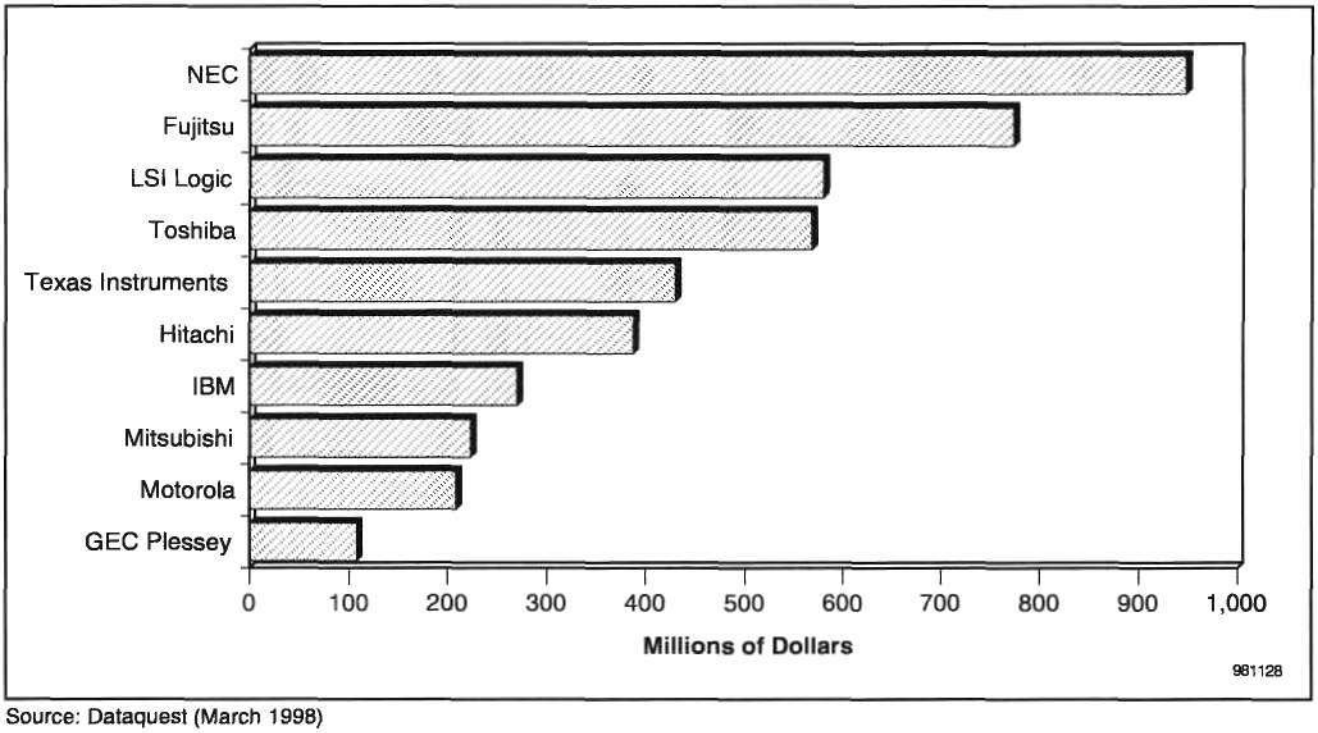
Source: Dataquest (March 1998)

Table 5-2
Preliminary 1997 Top 10 Worldwide Cell-Based IC Suppliers (Millions of Dollars)

Rank	Supplier	Revenue ($M)
1	Lucent Technologies	1,396
2	IBM	1,380
3	NEC	888
4	LSI Logic	765
5	VLSI Technology	595
6	Texas Instruments	480
7	Hewlett-Packard	466
8	Fujitsu	439
9	SGS-Thomson	305
10	Symbios	288

Source: Dataquest (March 1998)

Figure 5-3
Final 1996 Top 10 Worldwide Gate Array Suppliers by Product



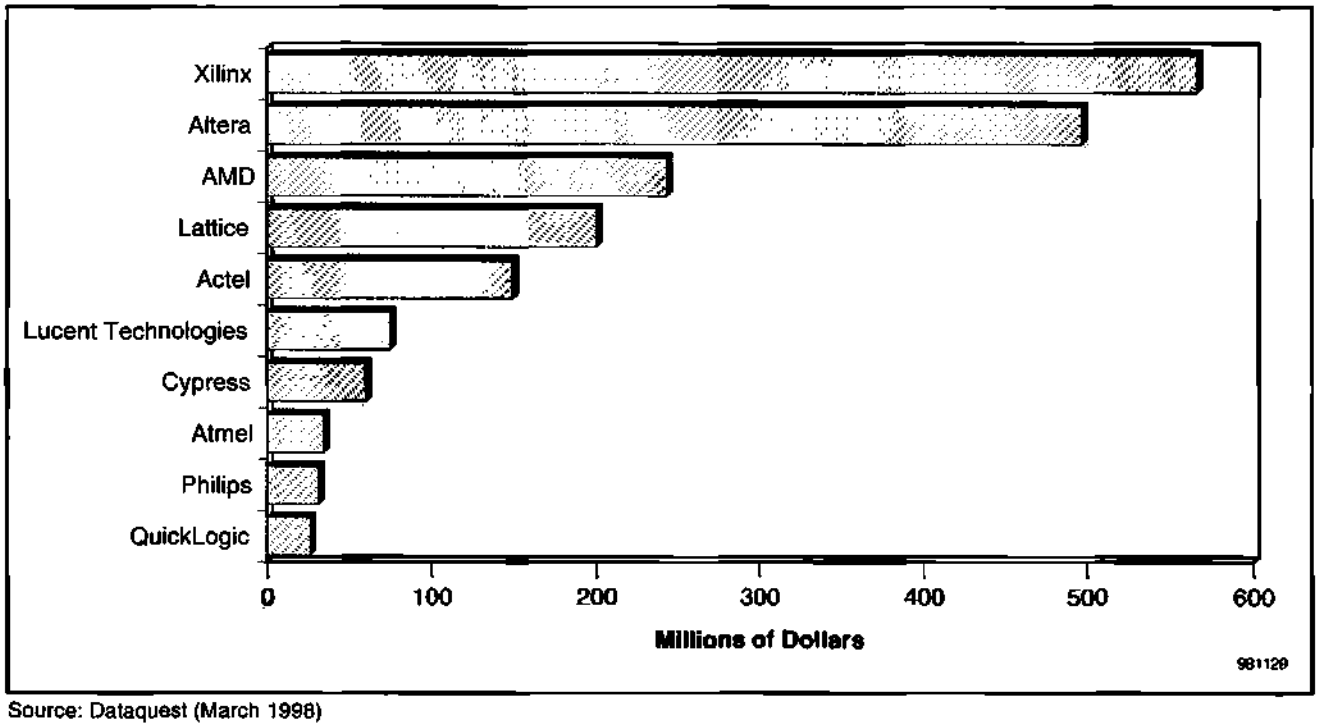
Source: Dataquest (March 1998)

Table 5-3
Preliminary 1997 Top 10 Worldwide Gate Array Suppliers (Millions of Dollars)

Rank	Supplier	Revenue ($M)
1	NEC	975
2	Fujitsu	809
3	LSI Logic	417
4	Toshiba	408
5	Texas Instruments	403
6	Hitachi	353
7	Mitsubishi	254
8	IBM	161
9	Motorola	147
10	Matsushita	130

Source: Dataquest (March 1998)

Figure 5-4
Final 1996 Top 10 Worldwide PLD Suppliers by Product



Source: Dataquest (March 1998)

Table 5-4
Preliminary 1997 Top 10 Worldwide PLD Suppliers
(Millions of Dollars)

Rank	Supplier	Revenue ($M)
1	Altera	631
2	Xilinx	612
3	Vantis	243
4	Lattice	242
5	Actel	156
6	Lucent Technologies	90
7	Cypress	52
8	Atmel	33
9	QuickLogic	29
10	Philips	4

Source: Dataquest (March 1998)

Chapter 6
Gate Array and Cell-Based IC Product Trends

Dataquest collected and analyzed design start trends from all the leading ASIC suppliers. The supplier data was then cross checked with the user data, and the results are reported in this chapter. Design start trends are the primary vehicle used to determine revenue trends because they lead revenue by one to two years.

Design Start Trends

Design Start Forecast

Cell-based IC design starts boomed in 1997 at the expense of gate array designs. Dataquest projects that the number of cell-based IC designs will surpass the number of gate array designs this year, as shown in Figure 6-1 and Table 6-1. A design start is counted when a unique prototype is shipped. These numbers include respins, when a customer redesigns the application because of a change in the system. The design start numbers are based on designs from ASIC suppliers and from ASIC divisions of semiconductor suppliers and do not include designs from standard product divisions. Table 6-2 shows that traditional gate array designs are and have been in decline, and Dataquest projects a five year average contraction of 23 percent. Embedded arrays have experienced some growth over the last couple of years, but we believe that the growth will decelerate because cell-based ICs are a better solution for most applications. Cell-based IC designs are the big winner, and Dataquest expects that they will account for more than 75 percent of the market in 2002, as shown in Figure 6-2.

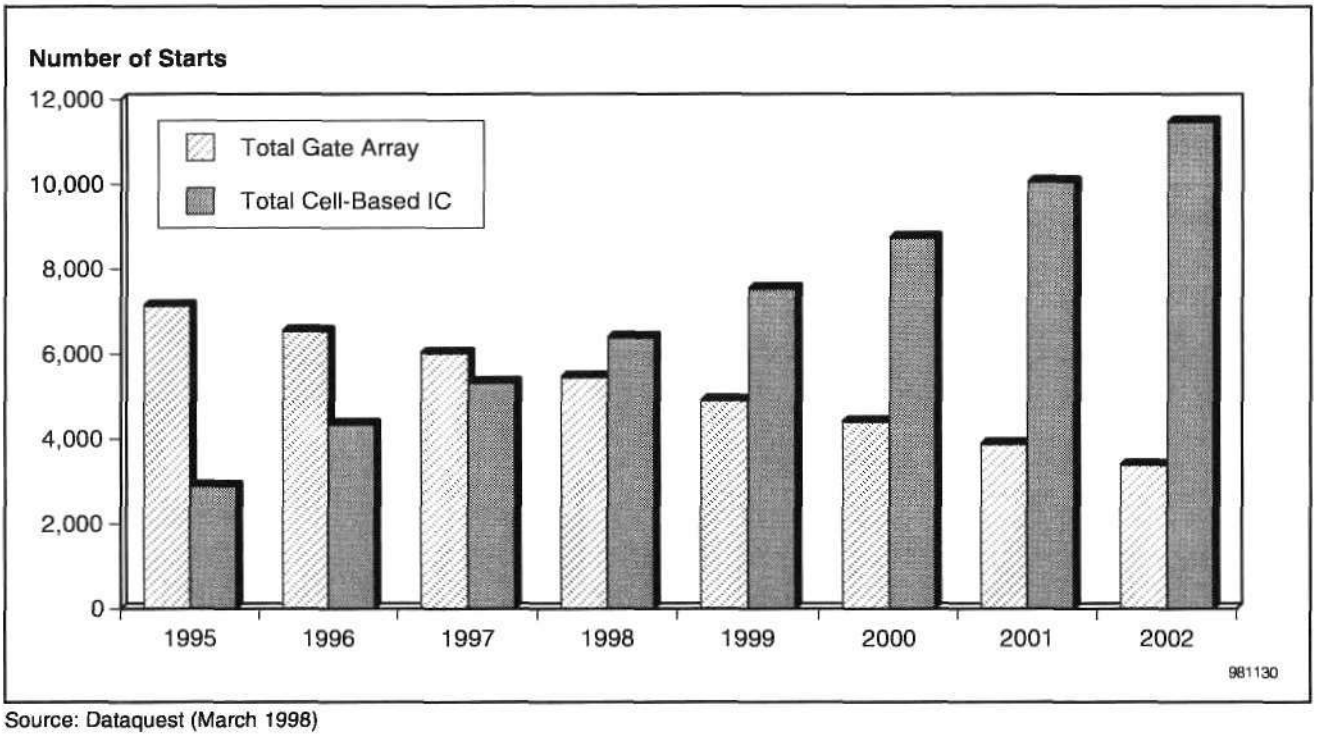
Although the mix of ASIC designs is changing, the total number of designs is growing at only a modest rate, with five-year CAGR of 5.5 percent. There are factors raising the numbers and factors lowering the numbers. New applications are clearly entering the market every year, which is boosting the numbers. There are three primary factors lowering the numbers:

- PLD designs are capturing the low-density and low-volume markets from ASICs
- Once standards have been set, chipsets or ASSPs are capturing the high-volume markets
- Design complexity is increasing at a rapid rate; what once were four 50,000-gate designs are now one 200,000-gate design

The bottom line is that new applications are winning by only a slight edge over the factors depleting the market.

North American companies' designs are much more complex than designs from Japanese companies, but the number of designs is relatively equal, as shown in Figure 6-3. Asia/Pacific has been growing fastest in number of designs, but from a much lower base. Design start growth will likely slow in Asia/Pacific during 1998, if not beyond, as the regional financial crisis forces budgets to be cut. Data processing ASIC designs lead but are not growing as fast as communications or consumer designs, as shown in Figure 6-4.

Figure 6-1
Estimated Worldwide ASIC Design Start Forecast



Source: Dataquest (March 1998)

Table 6-1
Estimated Worldwide Gate Array and Cell-Based IC Designs (Number of Design Starts)

	1995	1996	1997	1998	1999	2000	2001	2002
Total Gate Array and Cell-Based IC IC	10,025	10,884	11,348	11,846	12,451	13,156	13,941	14,856
Total Gate Array	7,138	6,543	6,022	5,455	4,909	4,408	3,880	3,387
Traditional Gate Array	6,367	5,359	4,501	3,691	2,916	2,274	1,683	1,212
Embedded Array	771	1,184	1,521	1,764	1,994	2,133	2,197	2,175
Total Cell-Based IC IC	2,887	4,341	5,326	6,391	7,542	8,748	10,061	11,469

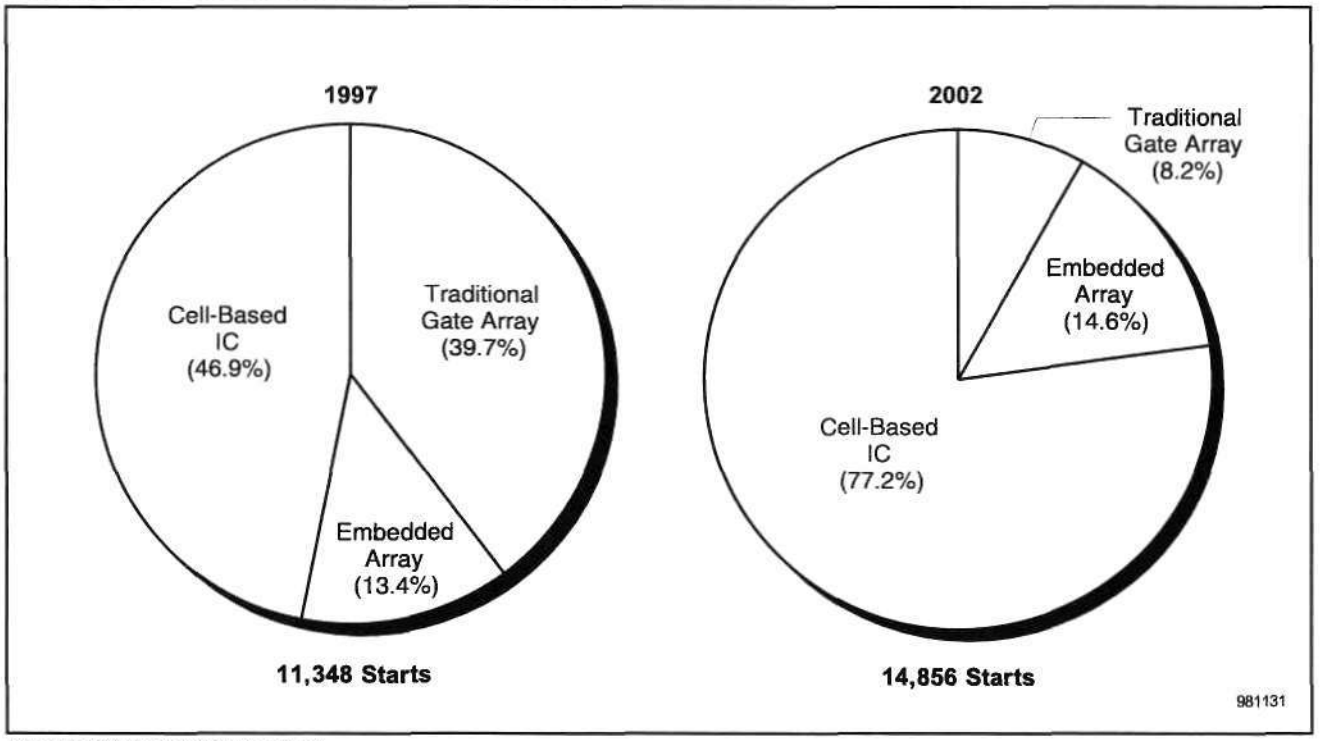
Source: Dataquest (March 1998)

Table 6-2
Estimated Worldwide Gate Array and Cell-Based IC Designs (Percentage Growth)

	1995	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Total Gate Array and Cell-Based IC	2.1	8.6	4.3	4.4	5.1	5.7	6.0	6.6	5.5
Total Gate Array	-4.9	-8.3	-8.0	-9.4	-10.0	-10.2	-12.0	-12.7	-10.9
Traditional Gate Array	-7.8	-15.8	-16.0	-18.0	-21.0	-22.0	-26.0	-28.0	-23.1
Embedded Array	29.6	53.6	28.5	16.0	13.0	7.0	3.0	-1.0	7.4
Total Cell-Based IC	25.0	50.4	22.7	20.0	18.0	16.0	15.0	14.0	16.6

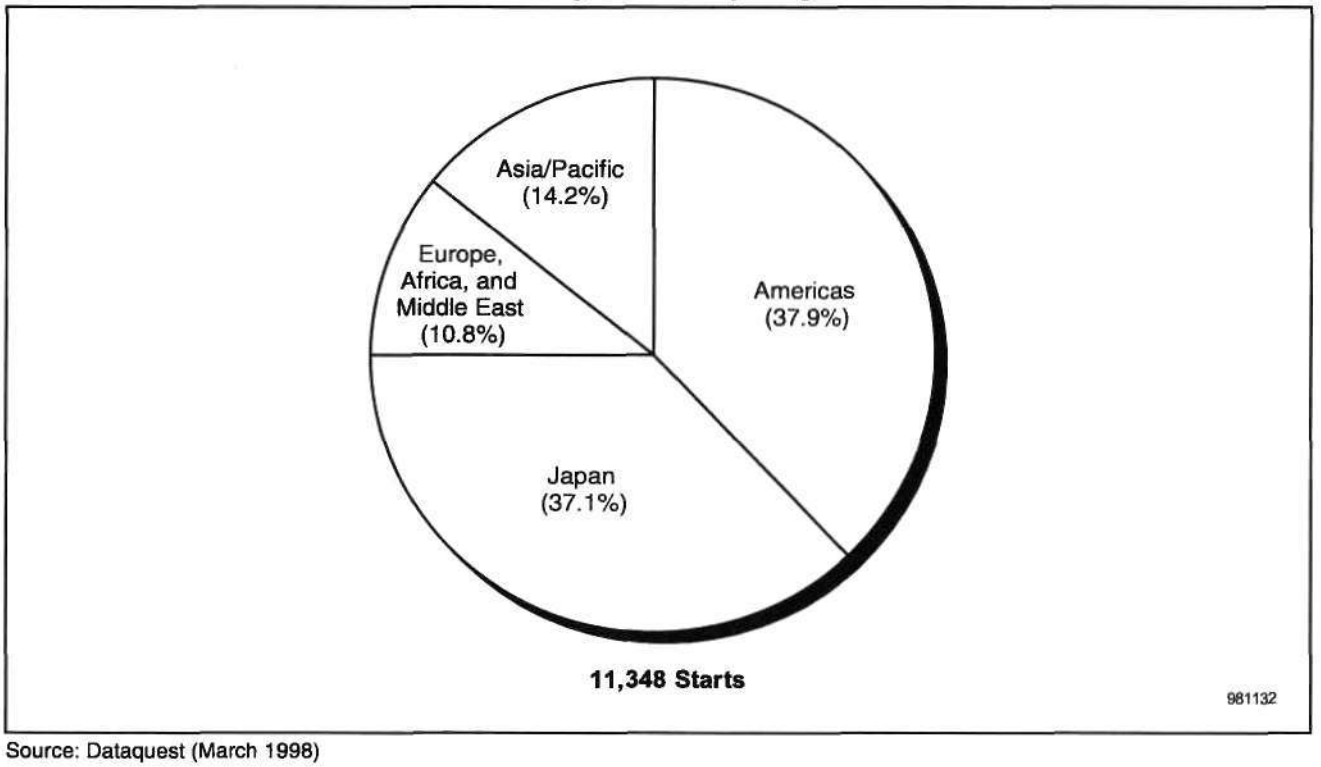
Source: Dataquest (March 1998)

Figure 6-2
Estimated Worldwide ASIC Design Starts by Product



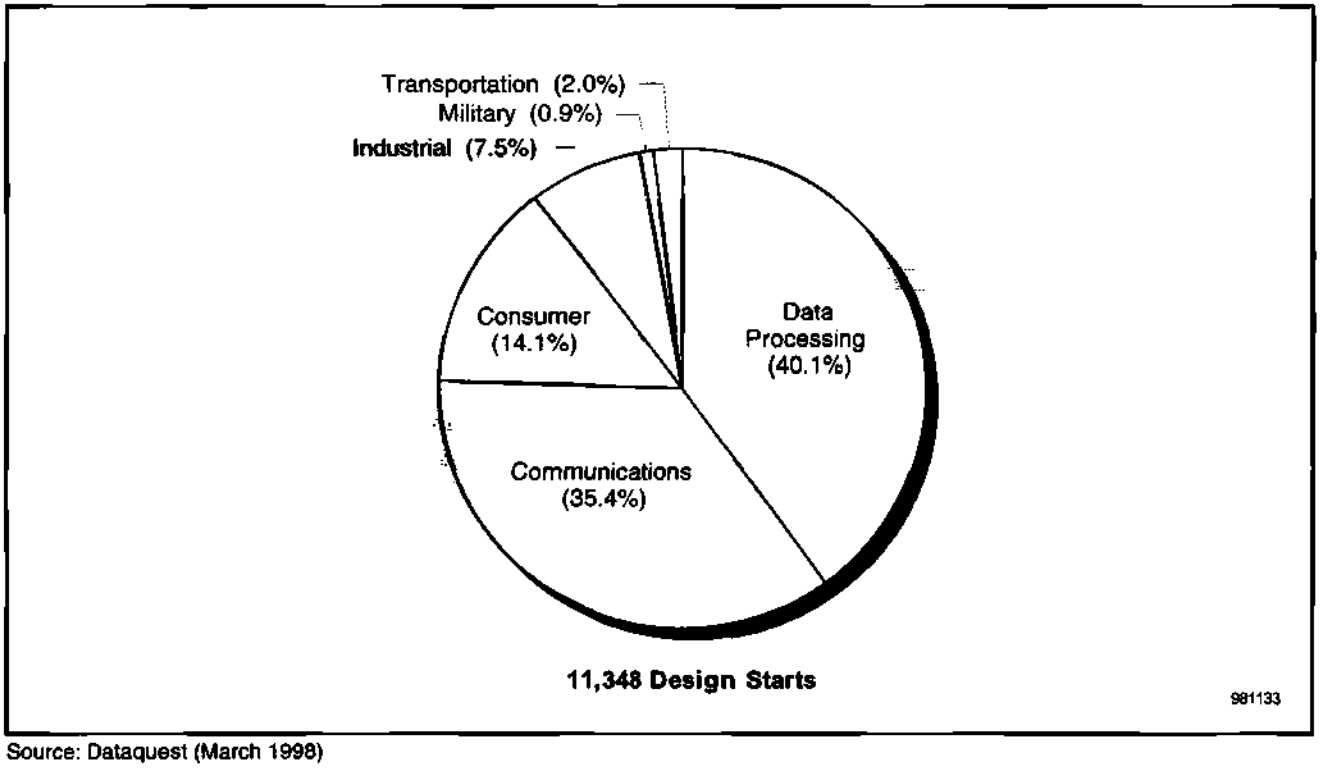
Source: Dataquest (March 1998)

Figure 6-3
Estimated 1997 Worldwide ASIC Design Starts by Region



Source: Dataquest (March 1998)

Figure 6-4
Estimated 1997 Worldwide ASIC Design Starts by Application Market



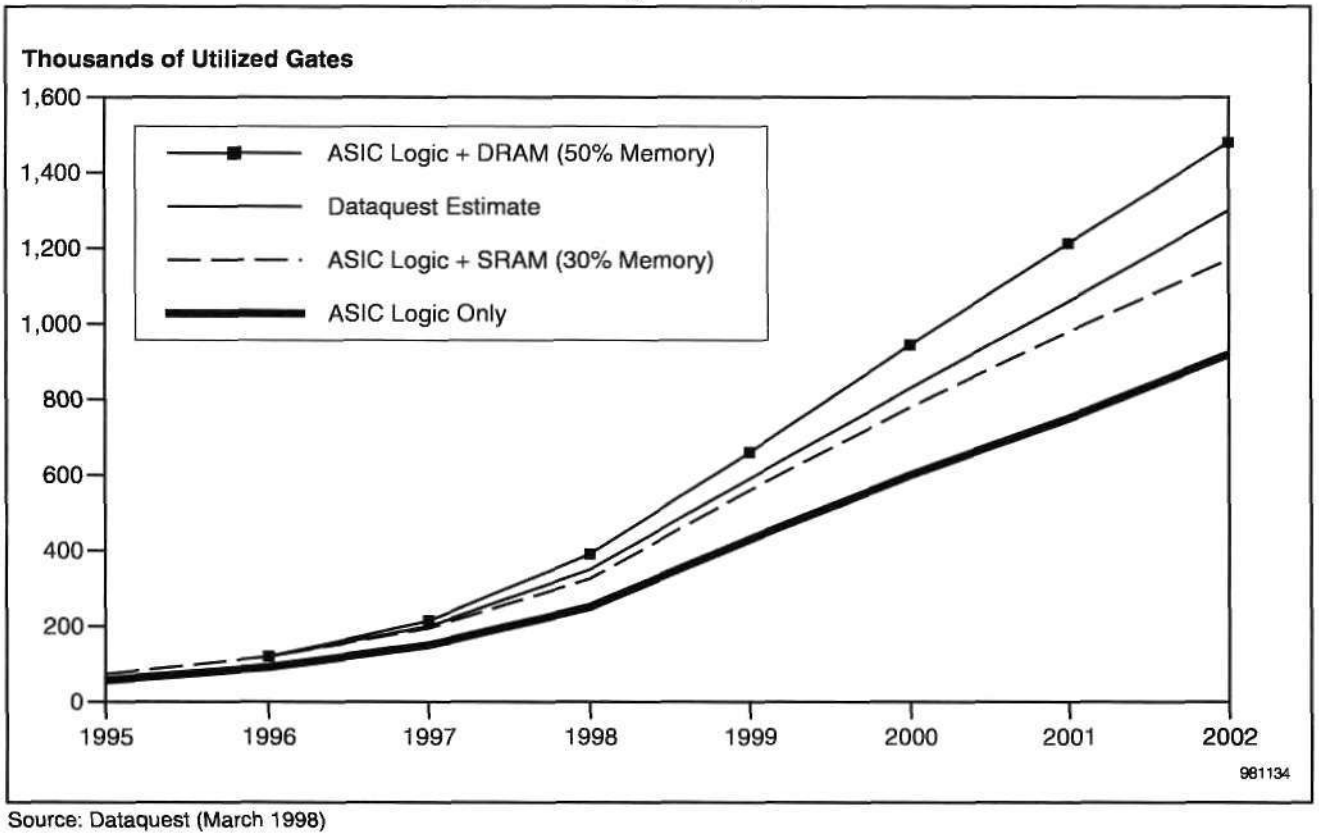
Source: Dataquest (March 1998)

Design Complexity Accelerates

As system-level integration enters the mainstream, design complexity is increasing at nearly exponential rates. On-chip microprocessors, DSPs, and related cores are here today and gaining momentum, helping to boost gate counts. More and more memory is also moving on chip and is one of the largest contributor to increasing gate counts. Figure 6-5 illustrates the impact of on-chip SRAM and DRAM over time. SRAM is a given for today's ASIC designs, so at least a 30 percent increase in gate counts over pure logic can be expected. On-chip DRAM is the wild card. How soon will it enter the mainstream? Dataquest believes it will gain momentum over the next five years but will not dominate designs in this period. The net result is that Dataquest is projecting average ASIC gate counts to rise from about 200,000 in 1997 to 1.3 million by 2002.

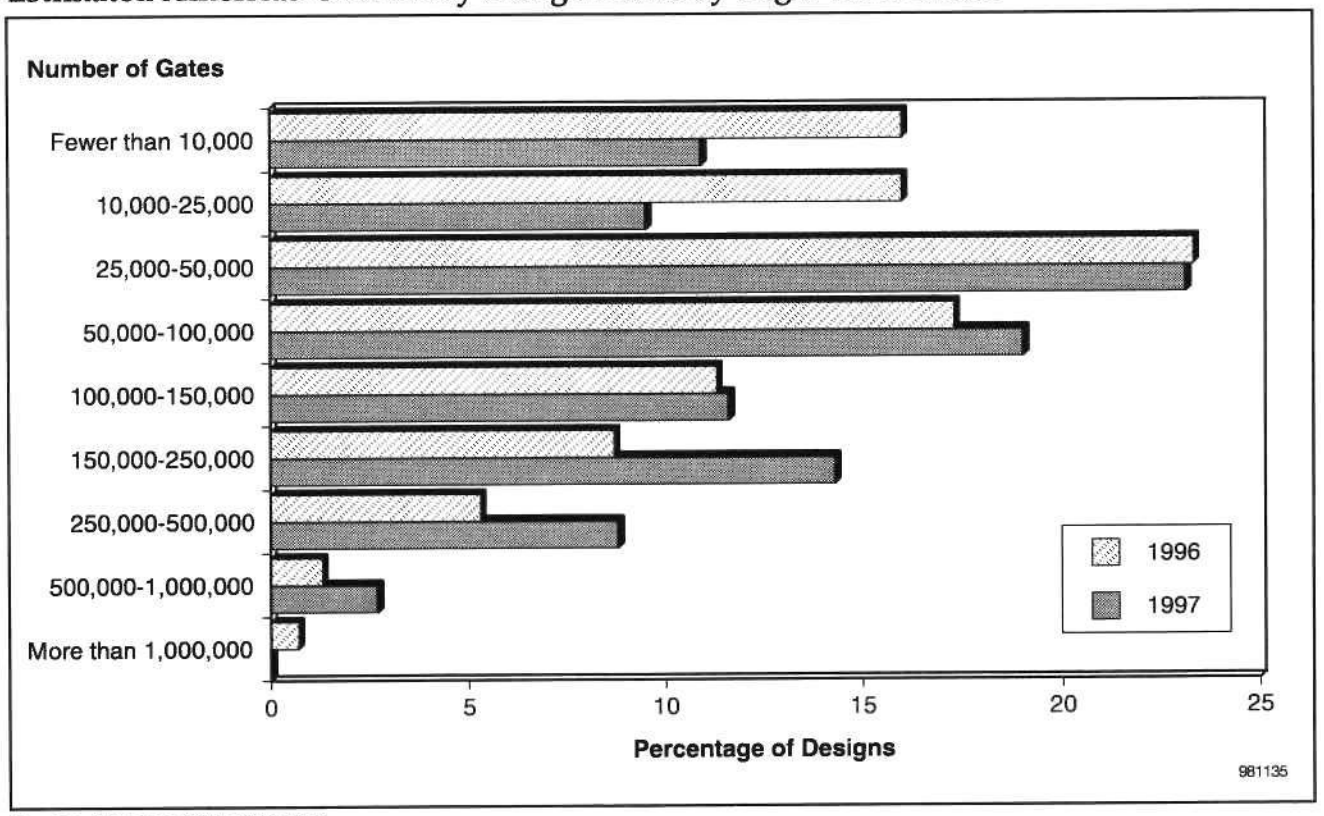
Logic complexity is also rising at an increasing rate for both gate arrays and cell-based ICs. Cell-based IC average gate counts are much higher than those of gate arrays. Figures 6-6 and 6-7 show the distribution for gate array and cell-based IC designs by logic gate count.

Figure 6-5
Estimated Americas ASIC Design Starts by Average Utilized Gate Count



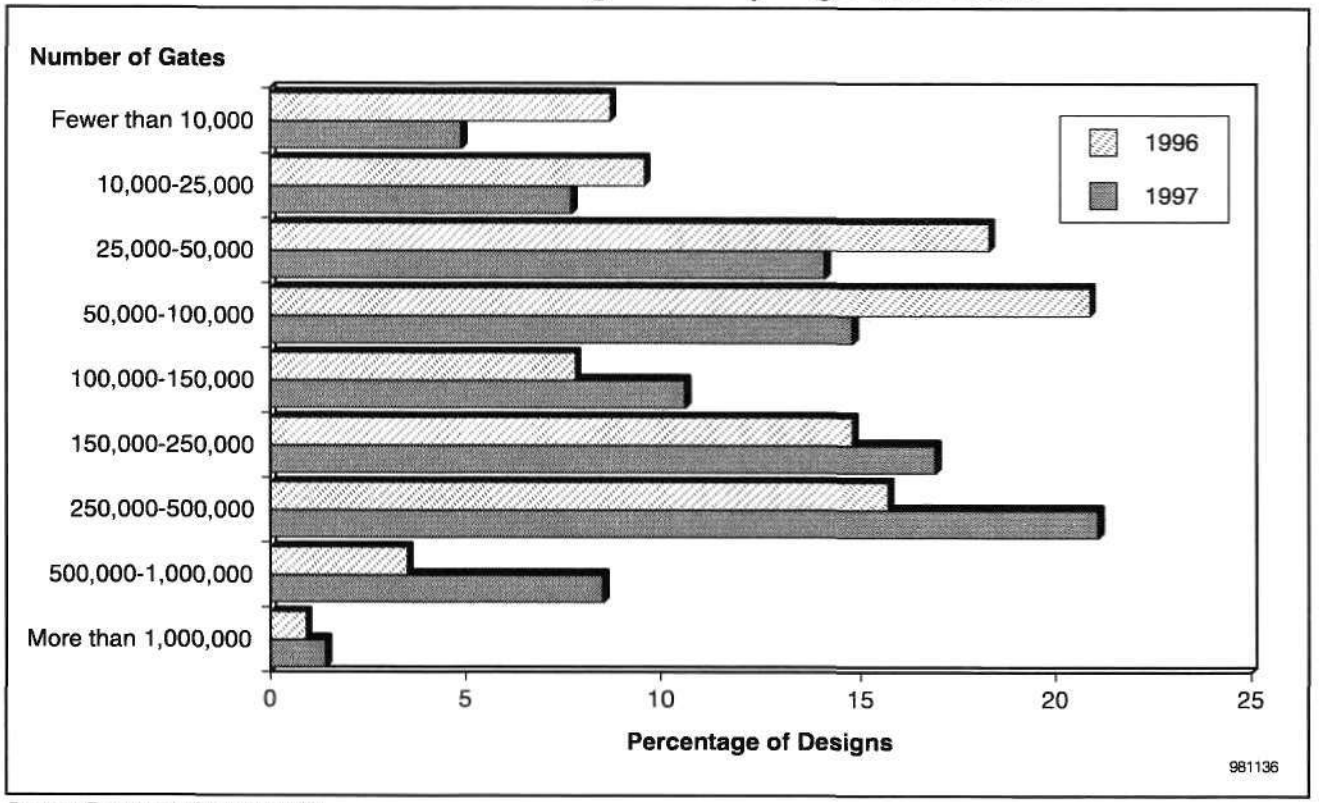
Source: Dataquest (March 1998)

Figure 6-6
Estimated Americas Gate Array Design Starts by Logic Gate Count



Source: Dataquest (March 1998)

Figure 6-7
Estimated Americas Cell-Based IC Design Starts by Logic Gate Count

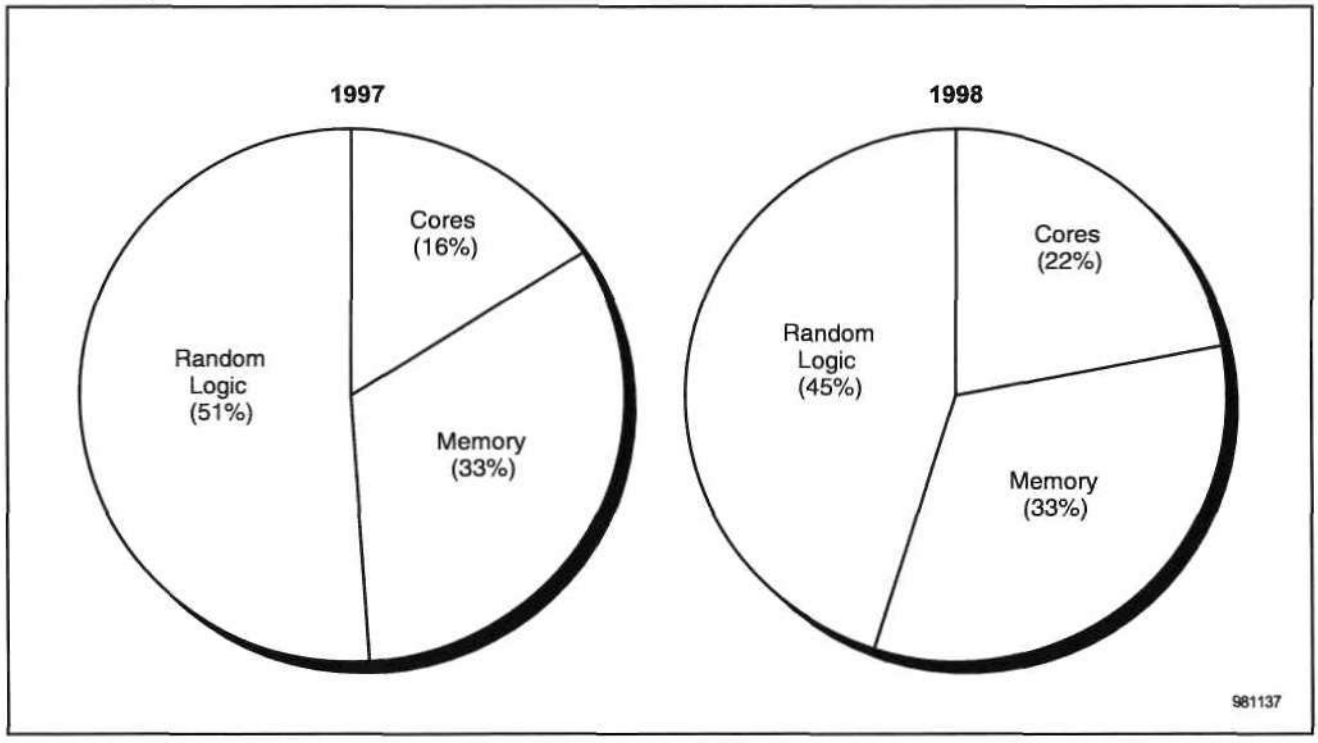


Source: Dataquest (March 1998)

Design Reuse—The Key to Increasing Complexity

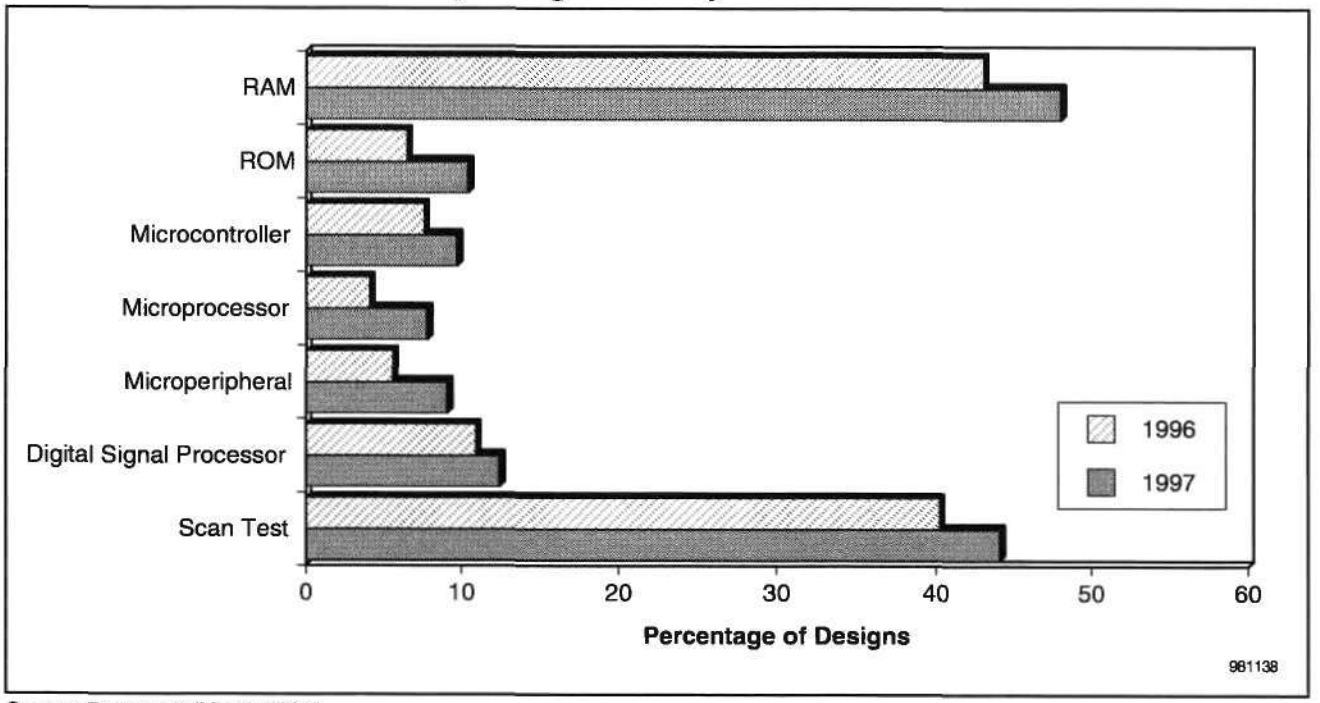
As ASIC complexities continue to skyrocket, design reuse becomes a must if suppliers and users are going to hit today's narrow time-to-market windows. The use of cores or large functional blocks that are pretested is clearly on the rise. According to Dataquest's last user wants and needs survey, cores are taking up a larger portion of the die area at the expense of random logic, as shown in Figure 6-8. Other large functional blocks such as microperipherals, microcontrollers, and test are going on chip in both gate arrays and cell-based ICs, as shown in Figures 6-9 and 6-10.

Figure 6-8
Estimated SLI ASIC Design Starts by Function/Implementation (Percentage of Die Area)



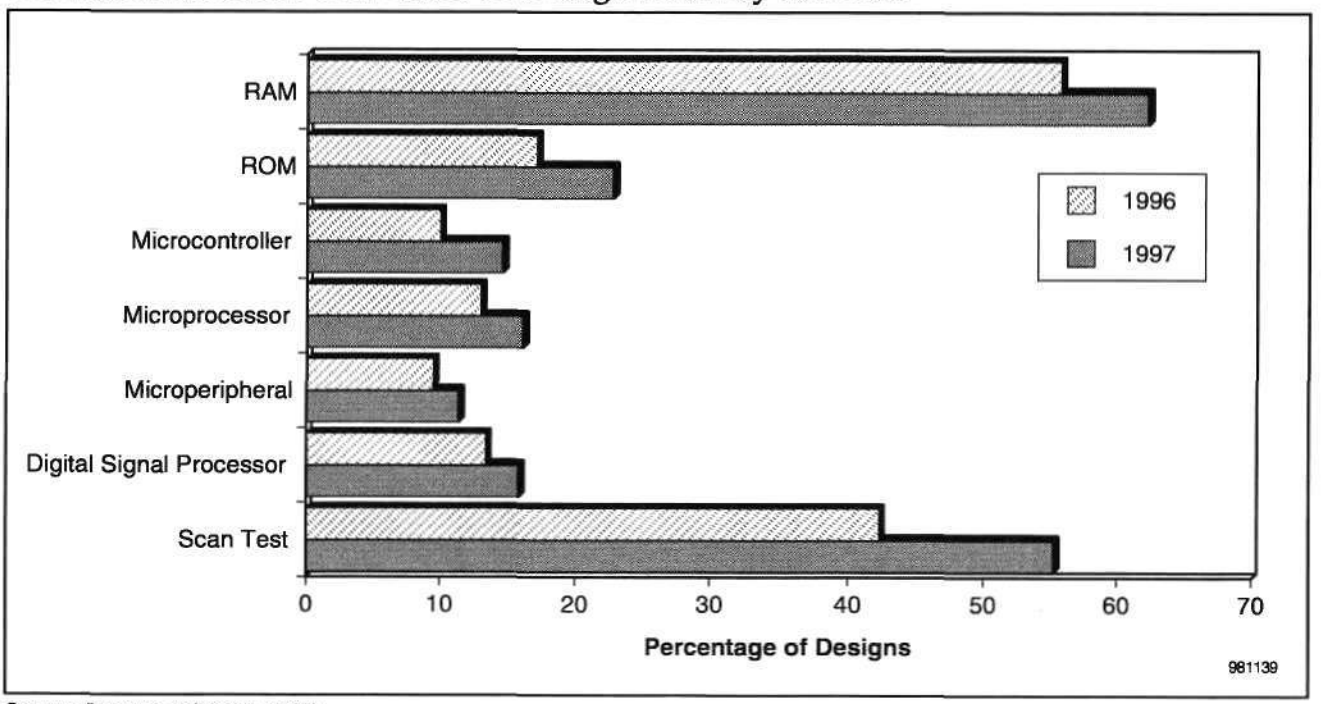
Source: Dataquest (March 1998)

Figure 6-9
Estimated Americas Gate Array Design Starts by Cell Use



Source: Dataquest (March 1998)

Figure 6-10
Estimated Americas Cell-Based IC Design Starts by Cell Use

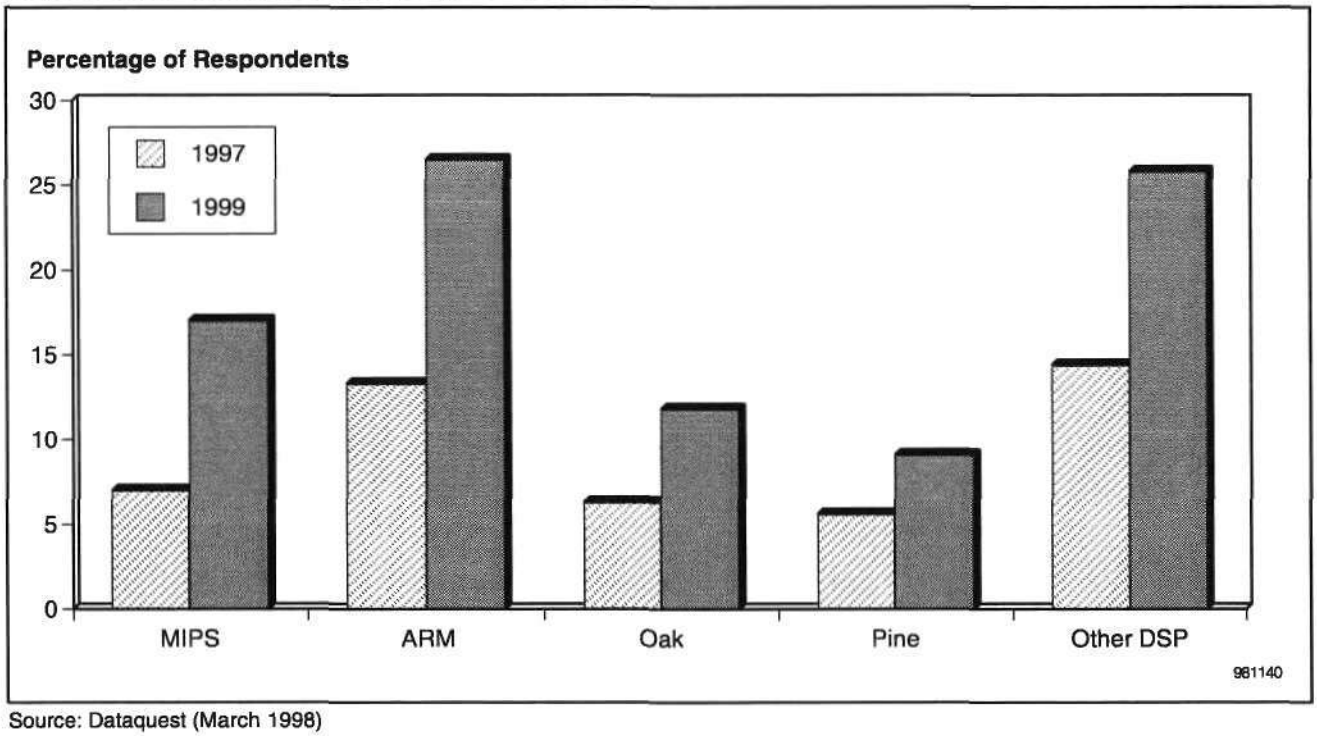


Source: Dataquest (March 1998)

Microprocessor/DSP Cores Determine SLI

Most ASIC designs have memory and logic, so SLI designs are differentiated from non-SLI designs by whether the design has an on-chip microprocessor or DSP core. If it has one of these cores, then it is SLI. As shown in Figure 6-10, about 16 percent of 1997 cell-based IC designs had on-chip microprocessors and about 16 percent had on-chip DSPs. This correlates well with Dataquest's estimate that about 20 percent of cell-based IC revenue was from SLI, because these designs tend to have higher volumes and higher average selling prices, owing to the added value of the IP. The big question that then must be asked is which microprocessor and DSP cores are most popular. Although the appropriate MPU/DSP core varies by application market, Figure 6-11 shows the perceived demand in general for the various MPU and DSP cores, according to our user wants and needs survey. ARM is winning the battle over the MIPS core, especially in the communications market, and the DSP Group's OakDSPCore and PineDSPCore are doing well. Texas Instruments' DSP cores are the primary "other DSP" cores in the figure and are still the leading DSP cores. The only problem for most ASIC suppliers is that Texas Instruments is not licensing these cores to any other suppliers.

Figure 6-11
Perceived Demand for MPU and DSP Cores



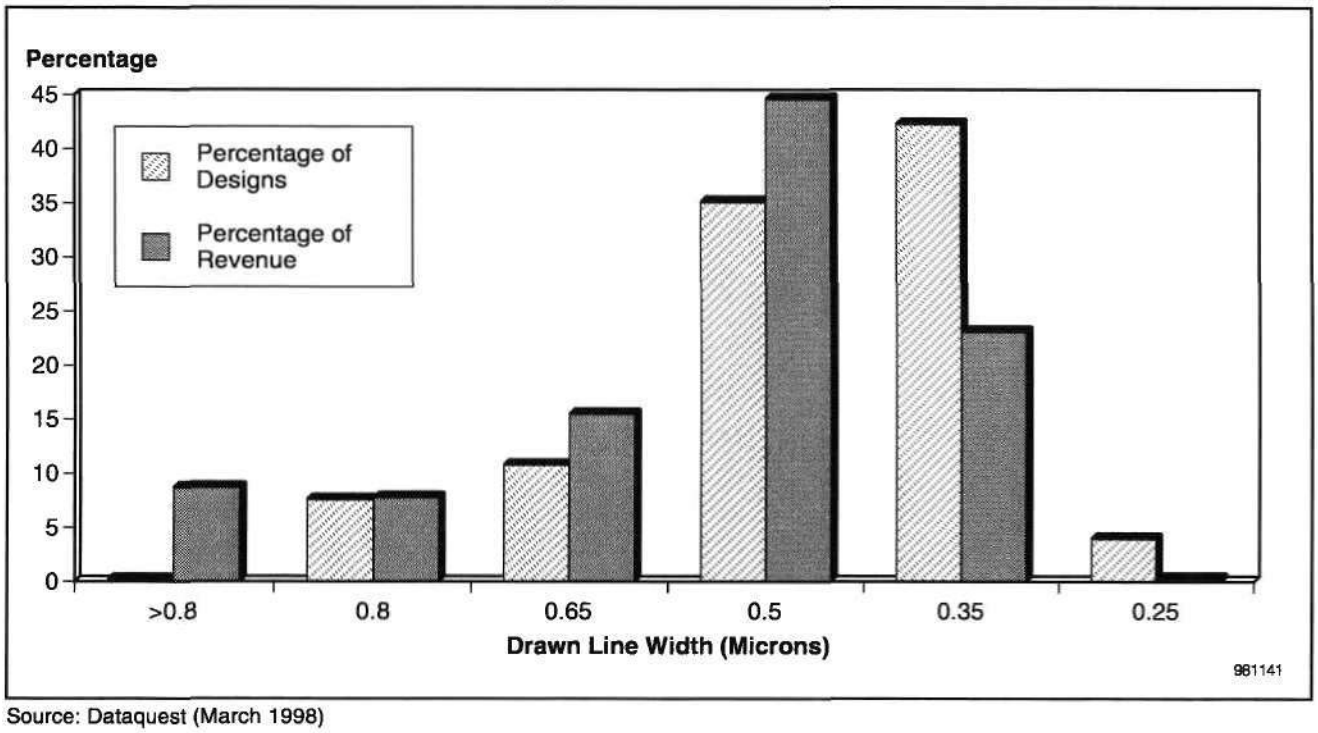
Source: Dataquest (March 1998)

Process Trends

Design Starts by Drawn Line Width

There are at least four to five process generations in design and in production at any given time. Dataquest polled all the leading ASIC suppliers to quantify current generations of both designs and production. Figure 6-12 illustrates the results of the survey for designs and production revenue for 1997. It is clear that designs lead production by as least one year; the workhorse design process is 0.35 micron and the mainstream production process is still 0.5 micron. Table 6-3 shows Dataquest's ASIC design start forecast by drawn line width.

Figure 6-12
Estimated 1997 Americas ASIC Designs and Revenue by Drawn Line Width



Source: Dataquest (March 1998)

Table 6-3
Estimated Americas ASIC Design Starts by Drawn Line Width (Percentage of Designs)

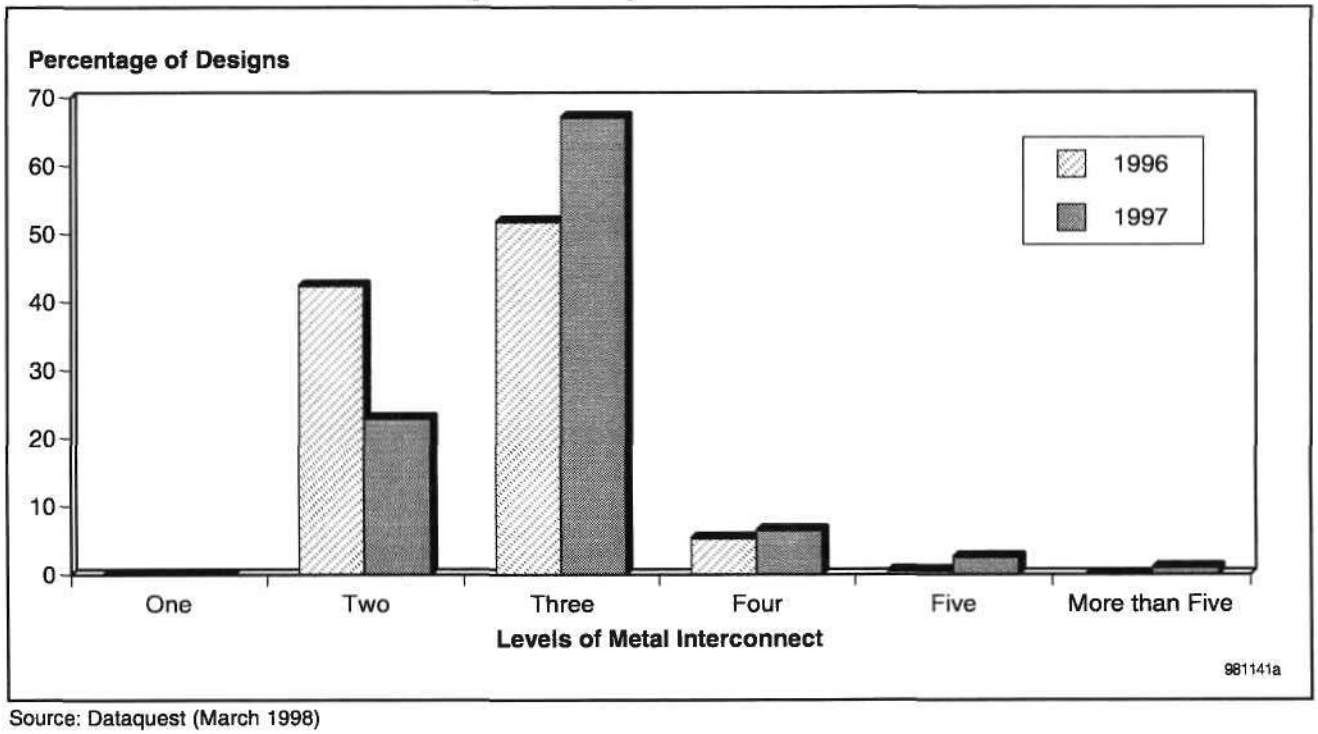
	1996	1997	1998	1999	2000	2001	2002
Over 0.8 Micron	2.4	0.2	0	0	0	0	0
0.8 Micron	14.8	7.6	3.5	2.2	0.3	0	0
0.65 Micron	14.2	10.8	7.4	3.1	1.1	0.2	0
0.5 Micron	34.1	35.1	26.1	14.1	7.9	3.3	1.7
0.35 Micron	33.5	42.3	46.2	37.9	22.1	14.2	9.3
0.25 Micron	1.0	4.0	14.1	34.1	43.1	42.4	41.2
0.18 Micron and Below	0	0	2.7	8.6	25.5	39.9	47.8

Source: Dataquest (March 1998)

Design Starts by Metal Interconnect

On-chip metal interconnect delays are rising in importance as chip densities continue to climb. It was only five year ago that the first three-level ASIC products were first announced to attack the interconnect bottleneck. Today, companies such as IBM are announcing ASIC products with more than five levels of interconnect. Although there have been many announcements from the leading ASIC suppliers about four- and five-level metal interconnect, the bulk of today's ASIC designs are being done with three-level interconnect, as shown in Figure 6-13.

Figure 6-13
Estimated Americas ASIC Design Starts by Metal Interconnect



Source: Dataquest (March 1998)

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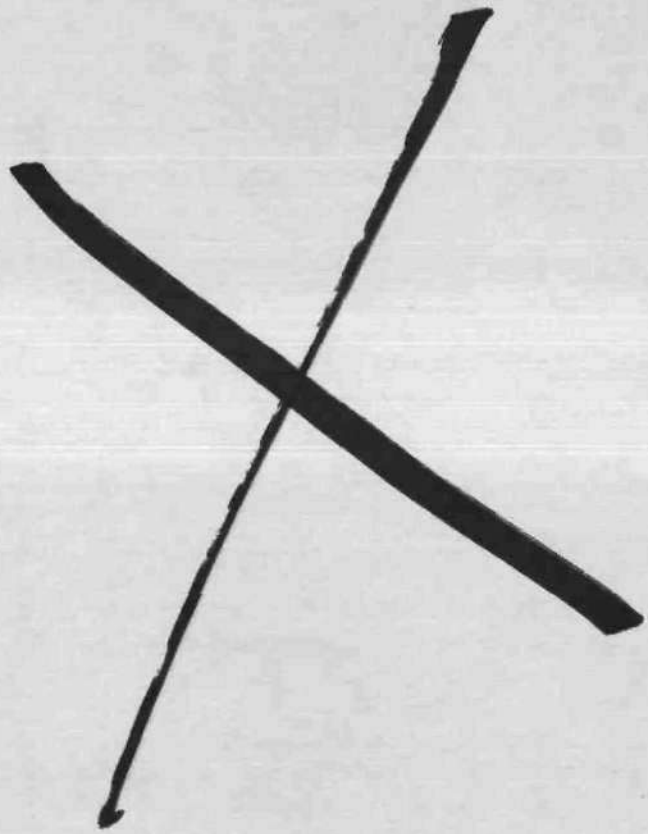

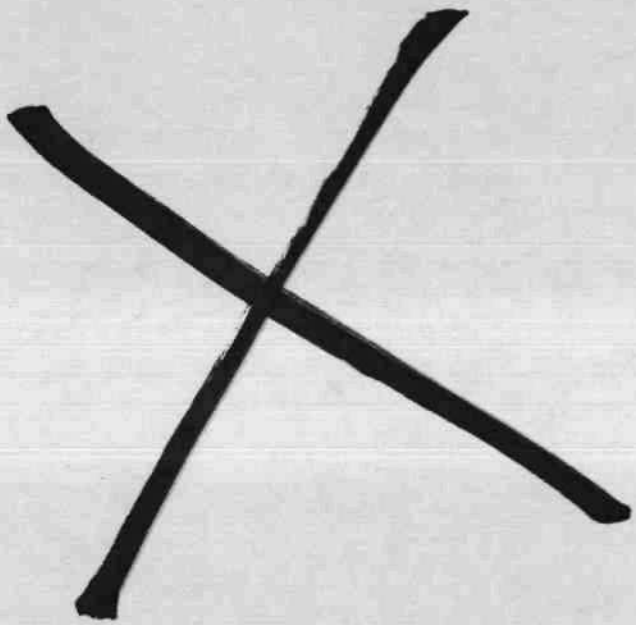

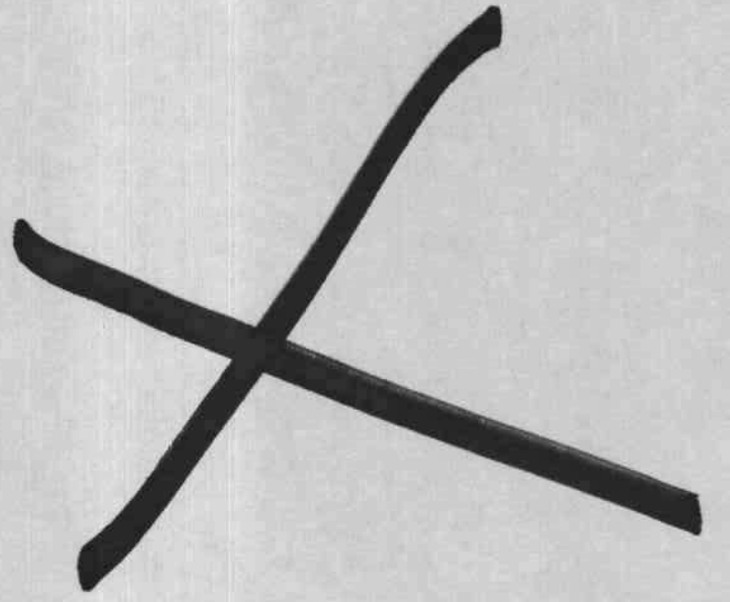

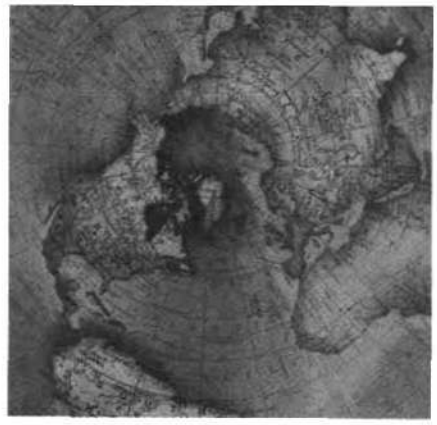

Dataquest

Worldwide ASIC/SLI Forecast: Fall 1998

Market Statistics

Program: ASIC/SLI Worldwide
Product Code: ASIC-WW-MS-9803
Publication Date: November 23, 1998
Filing: Market Statistics

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Chapter 1
The 1998 Worldwide ASIC Market

Introduction

This document contains detailed information on Dataquest's view on the application-specific integrated circuit (ASIC) market. We are expanding our coverage in this report to include system-level integration (SLI). The SLI market is composed of ASICs and application-specific standard products (ASSPs). To get an accurate picture of this emerging market, we have developed a new methodology based on bottom-up, application-driven demand forecasts. Past SLI ASIC forecasts were primarily supply driven. Our new methodology starts with system unit shipments for a selected market, then examine the dollar value of ASIC and ASSP content in each system to come up with a demand forecast by application market. We then examine the current and projected percentage of each application market that includes on-chip compute engines (microprocessor cores, digital signal processor—DSP—cores, or MPEG cores) to determine the size of each SLI market.

The second chapter gives the traditional supply-based consumption forecasts by product and by region. The third chapter includes new demand-based, application-driven forecasts to determine the size of the ASIC and ASSP SLI markets.

Segmentation

This section outlines the market segments that are specific to this document. Dataquest's objective is to provide data along lines of segmentation that are logical, appropriate to the industry in question, and immediately useful to clients.

Dataquest defines the ASIC market according to the segmentation scheme in Figure 1-1.

The figure shows Dataquest's segmentation of the logic market, which comprises four subcategories: standard logic, other MOS logic, full-custom ICs, and ASICs. Full-custom ICs have been pulled out of the ASIC category because they represent a declining market. These products are being replaced by gate arrays and cell-based ICs, which provide faster time to market. The ASIC family tree contains PLDs, gate arrays, and cell-based ICs.

Definitions

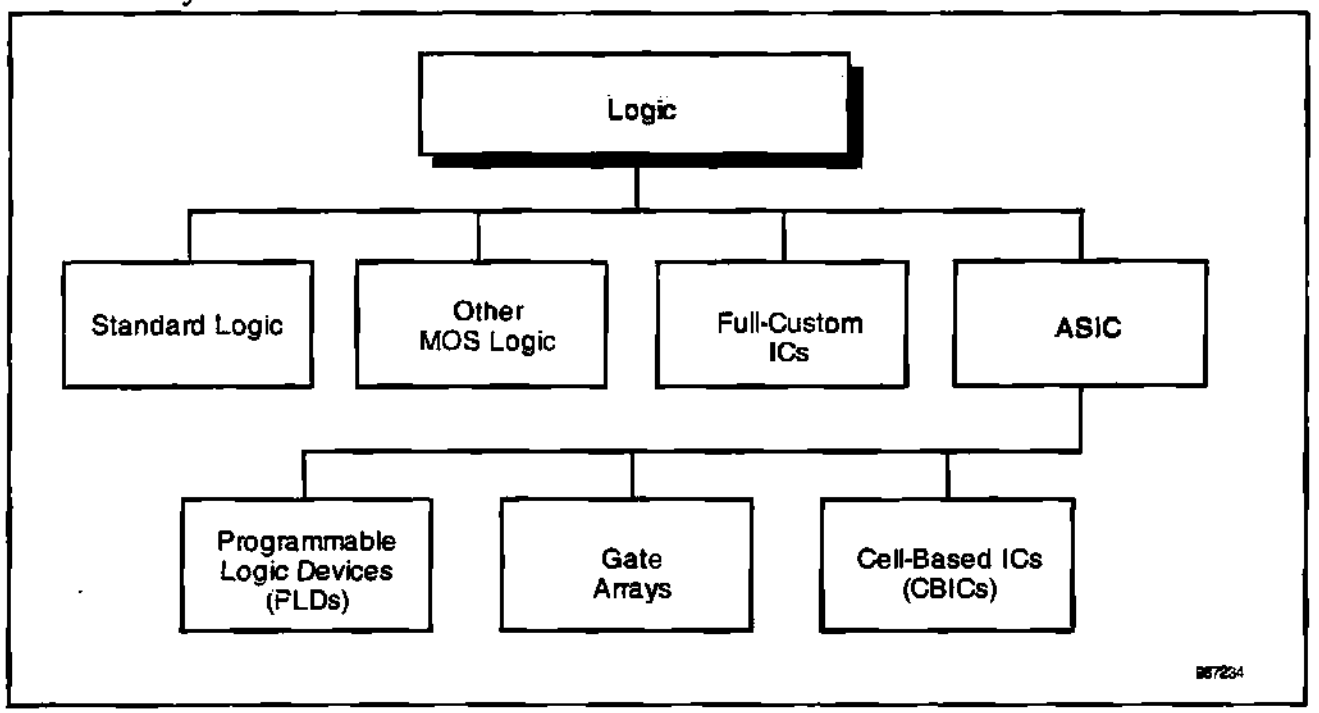
This section lists the definitions used by Dataquest to present the data in this document.

Product Definitions

Application-Specific Integrated Circuits

The term ASIC is used to describe all IC products dedicated to a specific application market that are customized for a single user. ASIC products are combinations of digital, mixed-signal, and analog products. Customized ICs purchased by more than one user become ASSPs and are no longer counted as ASICs.

Figure 1-1
ASIC Family Tree



Note: Data for full-custom ICs is not included.
Source: Dataquest (October 1998)

Application-Specific Standard Products

The term ASSP is used to describe all IC products dedicated to a specific application market that are sold to more than one user. ASSPs are combinations of digital, mixed-signal, and analog products.

Programmable Logic Devices

PLDs are defined as ICs programmed after assembly. Memory devices such as PROM and ROM are not included in this market segment. There has been some confusion in the industry regarding complex programmable logic device (CPLD) and field-programmable gate array (FPGA) definitions. Dataquest has simplified the PLD subcategories as follows:

- Simple programmable logic devices (SPLDs) are commonly referred to as programmable array logic (PAL). PAL devices consist of an array of AND gates, called product terms, connected to an array of AND gates or fixed OR gates. These devices are capable of providing up to two levels of logic without using additional input, output, or I/O cells or pins.
- High-density PLDs are a combination of FPGAs and CPLDs.

Gate Arrays

Gate arrays are ASICs that contain a configuration of uncommitted elements in a prefabricated base wafer. They are customized by interconnecting these elements with one or more routing layers. Included in this category are traditional gate arrays (channeled and sea-of-gates architecture) and embedded gate arrays (channeled or sea-of-gates architecture that also include megacells such as SRAM diffused into the gate array base wafer).

Cell-Based ICs

Cell-based ICs are ASICs that are customized using a full set of masks and use automatic place-and-route tools. Included in this category are traditional standard cells (fixed-height/fixed-width cells) as well as megacells (variable-height/variable-width cells) and compiled cells.

Full-Custom ICs

Full-custom ICs are defined as ASIC devices that are produced for a single user using a full set of masks. This process involves manual routing and placement of cells.

SLI Definition

At its October 1995 Semiconductors Conference, Dataquest introduced a new term and area of research to the industry—system-level integration (SLI). Other terms used in the industry today that have a similar meaning include "system on a chip" or "systems on silicon." We have chosen not to use these terms because they imply that the system is hardware only. We strongly believe that future system design will include hardware/software codesign, so we have chosen a broader term that encompasses both elements. This document focuses on the hardware portion of the market, and we define the hardware market as follows:

- System-level integration: An integrated circuit that contains a compute engine, memory, and logic on a single chip

There are two types of SLI devices: ASICs (application-specific integrated circuits that are sold to a single user) and ASSPs (application-specific standard products that are sold to more than one user).

Revenue Classification

Because systems may be fabricated, assembled, and sold in several different locations, Dataquest's regional device consumption is defined according to the shipping destination.

Consumption estimates include the following five sources of revenue:

- Intracompany revenue (sales to internal divisions)
- Nonrecurring engineering (NRE) revenue
- ASIC software revenue
- PLD development kit revenue
- Device production revenue

Despite the care taken in gathering, analyzing, and categorizing the data in a meaningful way, careful attention must be paid to the definitions and assumptions used herein when interpreting the estimates presented in this document. Various companies, government agencies, and trade associations may use slightly different definitions of product categories and regional groupings, or they may include different companies in their summaries. These differences should be kept in mind when making comparisons between data and numbers provided by Dataquest and those provided by other suppliers.

Merchant versus Captive Consumption

Dataquest includes all revenue, both merchant and captive, for semiconductor suppliers selling to the merchant market. Dataquest's consumption estimates do not include captive-only manufacturing companies represented by companies such as Digital Equipment Corporation, Northern Telecom, or Unisys that do not sell semiconductor products in the merchant market.

Regional Definitions

Americas

North America: Includes Canada, Mexico, and the United States (50 states).

South America

Central America

Japan

Japan is the only single-country region.

Europe, Middle East, and Africa

Western Europe: Includes Austria, Belgium, Denmark, Eire (Ireland), Finland, France, Germany (including former East Germany), Greece, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, the United Kingdom, and rest of western Europe (Andorra, Cyprus, Gibraltar, Liechtenstein, Monaco, San Marino, Vatican City, Iceland, Malta, and Turkey).

Eastern Europe: Includes Albania, Bulgaria, the Czech Republic and Slovakia, Estonia, Hungary, Latvia, Lithuania, Poland, Romania, the republics of the former Yugoslavia, and the republics of the former USSR (Belarus, Russian Federation, Ukraine, Georgia, Moldova, Armenia, Azerbaijan, Kazakhstan, Uzbekistan, Tajikistan, Kyrgyzstan, and Turkmenistan).

Asia/Pacific

Includes Hong Kong, Singapore, South Korea, Taiwan, Australia, Bangladesh, Cambodia, China, India, Indonesia, Laos, Malaysia, Maldives, Myanmar, Nepal, New Zealand, Pakistan, the Philippines, Sri Lanka, Thailand, and Vietnam.

Line Item Definitions

Factory revenue is defined as the money value received by a semiconductor manufacturer for its products. Revenue from the sale of semiconductors sold either as finished goods, die, or wafers to another semiconductor vendor for resale is attributed to the semiconductor vendor that sells the product to a distributor or equipment manufacturer.

Forecast Methodology and Assumptions

Dataquest publishes five-year factory revenue forecasts for the ASIC market during the first and third quarter of each year. In doing so, Dataquest utilizes a variety of forecasting techniques (both qualitative and quantitative) that vary by technology area. An overview of Dataquest forecasting techniques can be found in the Dataquest Research Methodology guide.

ASIC Forecast Methodology

Dataquest's ASIC forecast methodology includes the following steps:

- Formally and informally survey the leading ASIC vendors (in gate arrays, cell-based ICs, and PLDs) throughout the year for their expectations, as well as for their views of the application markets in which they participate
- Formally survey ASIC users for their expected buying patterns, in addition to their views on the growth of the application markets in which they participate
- Examine statistics provided by a number of industry and government organizations (such as the World Semiconductor Trade Statistics, the Japanese Ministry of International Trade and Industry, and the U.S. Department of Commerce) for up-to-date monthly trends
- Perform time-series analysis as well as apply judgmental industry knowledge to product and application trends

ASIC Forecast Assumptions

ASICs

The worldwide ASIC market has been hit hard in 1998 and will post a revenue decline for the first time in history. The Asian financial crisis, general industry slowdown, and above-normal price pressure are the primary causes for the decline. Worldwide ASIC consumption is expected to decline about 4 percent, with gate arrays—the hardest hit—experiencing an 18 percent decline, PLDs showing a 1 percent decline, and cell-based ICs growing only 4 percent. A large portion of the gate array market is in Japan, so this market has been impacted by the low yen-to-U.S. dollar exchange rate for the majority of the year as well as by weak demand caused by the Japanese recession. Couple these problems with major price reductions and the fact that many gate arrays are being replaced by PLDs on the low end and cell-based ICs on the high end, and the result is a market in serious trouble.

Dataquest has clearly reduced substantially all the 1998 and 1999 growth rates from our prior spring forecast. There has been major price erosion in each market as suppliers bid for reduced demand. We are not expecting a significant upturn until the second half of 1999. If Japan's banking problems continue to worsen, our 1999 forecast will become optimistic. We have reduced our 1998 and 1999 growth rates in all regions, with the largest reduction in Japan. We are expecting about a 13 percent decline in ASIC consumption in Japan and expecting the remaining regions to have relatively flat growth in 1998. In 1999, we are expecting modest growth of about 10 percent for all regions, with the exception of Japan, which is likely to be flat, depending on the yen/U.S. dollar exchange rate.

The long-term view for ASIC products is that PLDs will continue to replace gate arrays at the low end of the market and that cell-based ICs will continue to beat gate arrays at the high end of the market. The net effect is that PLDs should grow at a 15 percent compound annual growth rate (CAGR) for the next five years, cell-based ICs should grow at a 21 percent five-year CAGR, and gate arrays should decline at about a 10 percent rate.

Long-term ASIC growth rates will decline as ASSPs replace ASICs in mature applications.

Cell-Based ICs

The cell-based IC market is the largest and fastest growing of all the ASIC markets. The electronics industry is rapidly moving to system-level integration, or system-on-a-chip, and cell-based ICs are and will be the product of choice. Of the ASIC alternatives for high-volume applications, cell-based ICs offer the best performance, the smallest die, and the lowest cost. Emerging high-volume SLI applications that will provide significant growth in the cell-based IC market include digital cellular, LAN/WAN, switching (premise and central office), workstations/servers, disk drives, set-top boxes, video games, digital camcorders and still cameras, and digital TV.

Gate Arrays

The gate array market is clearly in the decline phase of the product life cycle. North American and European companies were first to reduce their gate array consumption in favor of cell-based ICs. Japanese companies are now moving quickly from gate arrays to cell-based ICs to reduce costs and expedite the move to SLI. The gate array market will not disappear overnight—note the long life cycle of standard logic—but the number of new gate array designs is clearly dropping at a fairly fast pace in favor of cell-based ICs and PLDs. We expect some gate array suppliers to get out of the market because demand will be limited and suppliers are far too numerous.

PLDs

For the PLD industry, 1998 is expected to be the toughest year in history. The global slowdown has hit a PLD market suffering from the lingering effects of 1997's PLD price wars. Worldwide growth in 1998 is expected to be down 1 percent. Dataquest is expecting modest growth for the first half of 1999, with more typical growth to resume in the second half of 1999. Although unit shipments of high-density devices continue to increase at a solid clip, reduced average selling prices (ASPs) have held down market growth. PLDs are making rapid progress in terms of increased density, increased speeds, and reduced costs. PLDs are increasingly becoming a solid ASIC alternative and are starting to experience the same effects as the ASIC industry: The user gets much more functionality with a new device but at the same price paid for the previous device with less functionality. Demand will continue to increase at a rapid clip, but price-per-gate declines will continue to offset unit growth. There is major demand, however, so the net effect is that PLDs will remain a good market, with a solid 15 percent five-year CAGR.

Exchange Rates

Dataquest uses an average annual exchange rate in converting revenue to U.S. dollar amounts. Table 1-1 outlines these rates for 1996 through 1998.

Table 1-1
Exchange Rates (Foreign Currency per U.S. Dollar)

	1996	1997	1998*
Japan (Yen)	108.81	121.10	131.20
France (Franc)	5.12	5.84	5.87
Germany (Deutsche Mark)	1.50	1.73	1.75
United Kingdom (Pound Sterling)	0.64	0.61	0.60

*Preliminary
Source: Dataquest (April 1998)

Project Analyst: Bryan Lewis

Chapter 2
ASIC Product Forecasts

Tables 2-1 through 2-17 show ASIC product trends.

Table 2-1
Estimated Worldwide ASIC Consumption by Technology (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Total ASIC	**14,802**	**16,526**	**15,898**	**17,213**	**20,895**	**25,332**	**30,540**	**13.1**
Digital ASIC	13,737	15,108	14,374	15,392	18,504	22,265	26,645	12.0
Mixed-Signal ASIC	1,065	1,418	1,524	1,821	2,392	3,067	3,894	22.4

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1998)

Table 2-2
Estimated Worldwide ASIC Consumption by Product (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Total ASIC	**14,802**	**16,526**	**15,898**	**17,213**	**20,895**	**25,332**	**30,540**
Gate Array	5,612	5,260	4,330	3,850	3,592	3,371	3,103
PLD	1,873	2,103	2,081	2,332	2,866	3,488	4,154
Cell-Based IC	7,317	9,163	9,486	11,032	14,437	18,472	23,283

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1998)

Table 2-3
Estimated Worldwide ASIC Consumption by Product (Percentage Growth)

	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Total ASIC	**10.3**	**11.6**	**-3.8**	**8.3**	**21.4**	**21.2**	**20.6**	**13.1**
Gate Array	-6.1	-6.3	-17.7	-11.1	-6.7	-6.1	-7.9	-10.0
PLD	10.1	12.3	-1.0	12.0	22.9	21.7	19.1	14.6
Cell-Based IC	27.3	25.2	3.5	16.3	30.9	28.0	26.0	20.5

Source: Dataquest (October 1998)

Table 2-4
Estimated Worldwide ASIC Consumption by Region (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Worldwide Total	**14,802**	**16,526**	**15,898**	**17,213**	**20,895**	**25,332**	**30,540**
Americas	5,986	7,099	7,086	7,820	9,553	11,678	14,269
Japan	4,402	4,576	4,002	4,117	4,745	5,565	6,404
Europe, Middle East, and Africa	2,825	3,189	3,170	3,446	4,290	5,248	6,404
Asia/Pacific	1,589	1,662	1,640	1,830	2,308	2,842	3,463

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1998)

Table 2-5
Estimated Worldwide ASIC Consumption by Region (Percentage Growth)

	1996	1997	1998	1999	2000	2001	2001	CAGR (%) 1997-2002
Worldwide Total	**10.3**	**11.6**	**-3.8**	**8.3**	**21.4**	**21.2**	**20.6**	**13.1**
Americas	11.3	18.6	-0.2	10.3	22.2	22.2	22.2	15.0
Japan	2.4	4.0	-12.5	2.9	15.2	17.3	15.1	7.0
Europe, Middle East, and Africa	22.2	12.9	-0.6	8.7	24.5	22.3	22.0	15.0
Asia/Pacific	10.7	4.6	-1.3	11.6	26.1	23.1	21.9	15.8

Source: Dataquest (October 1998)

Table 2-6
Estimated Worldwide ASIC Consumption by Region (Percentage of Revenue)

	1996	1997	1998	1999	2000	2001	2002
Worldwide Total	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**
Americas	40.4	43.0	44.6	45.4	45.7	46.1	46.7
Japan	29.7	27.7	25.2	23.9	22.7	22.0	21.0
Europe, Middle East, and Africa	19.1	19.3	19.9	20.0	20.5	20.7	21.0
Asia/Pacific	10.7	10.1	10.3	10.6	11.0	11.2	11.3

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1998)

Table 2-7
Estimated Worldwide Cell-Based IC Consumption (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Worldwide Total	**7,317**	**9,163**	**9,486**	**11,032**	**14,437**	**18,472**	**23,283**
Americas	2,788	4,098	4,417	5,206	6,744	8,614	10,908
Japan	1,839	1,997	1,865	2,117	2,795	3,614	4,490
Europe, Middle East, and Africa	1,753	2,013	2,093	2,385	3,126	3,971	5,014
Asia/Pacific	937	1,055	1,112	1,324	1,772	2,274	2,872

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1998)

Table 2-8
Estimated Worldwide Cell-Based IC Consumption (Percentage Growth)

	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Worldwide Total	**27.3**	**25.2**	**3.5**	**16.3**	**30.9**	**28.0**	**26.0**	**20.5**
Americas	25.1	47.0	7.8	17.9	29.5	27.7	26.6	21.6
Japan	18.2	8.6	-6.6	13.5	32.1	29.3	24.2	17.6
Europe, Middle East, and Africa	34.5	14.8	4.0	14.0	31.0	27.0	26.3	20.0
Asia/Pacific	42.3	12.6	5.4	19.1	33.9	28.3	26.3	22.2

Source: Dataquest (October 1998)

Table 2-9
Estimated Worldwide Cell-Based IC Consumption (Percentage of Revenue)

	1996	1997	1998	1999	2000	2001	2002
Worldwide Total	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**
Americas	38.1	44.7	46.6	47.2	46.7	46.6	46.8
Japan	25.1	21.8	19.7	19.2	19.4	19.6	19.3
Europe, Middle East, and Africa	24.0	22.0	22.1	21.6	21.6	21.5	21.5
Asia/Pacific	12.8	11.5	11.7	12.0	12.3	12.3	12.3

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1998)

Table 2-10
Estimated Worldwide Gate Array Consumption by Region (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Worldwide Total	**5,612**	**5,260**	**4,330**	**3,850**	**3,592**	**3,371**	**3,103**
Americas	2,082	1,748	1,441	1,238	1,130	1,024	934
Japan	2,308	2,299	1,847	1,664	1,533	1,445	1,314
Europe, Middle East, and Africa	697	751	639	584	571	554	530
Asia/Pacific	525	462	403	364	357	348	326

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1998)

Table 2-11
Estimated Worldwide Gate Array Consumption by Region (Percentage Growth)

	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Worldwide Total	**-6.1**	**-6.3**	**-17.7**	**-11.1**	**-6.7**	**-6.1**	**-7.9**	**-10.0**
Americas	-1.6	-16.0	-17.5	-14.1	-8.7	-9.4	-8.8	-11.8
Japan	-8.8	-0.4	-19.6	-9.9	-7.9	-5.7	-9.1	-10.6
Europe, Middle East, and Africa	1.9	7.7	-14.9	-8.6	-2.1	-3.0	-4.4	-6.7
Asia/Pacific	-18.9	-12.0	-12.8	-9.6	-1.8	-2.6	-6.4	-6.8

Source: Dataquest (October 1998)

Table 2-12
Estimated Worldwide Gate Array Consumption by Region (Percentage of Revenue)

	1996	1997	1998	1999	2000	2001	2002
Worldwide Total	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**
Americas	37.1	33.2	33.3	32.2	31.5	30.4	30.1
Japan	41.1	43.7	42.7	43.2	42.7	42.9	42.3
Europe, Middle East, and Africa	12.4	14.3	14.8	15.2	15.9	16.4	17.1
Asia/Pacific	9.4	8.8	9.3	9.5	9.9	10.3	10.5

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1998)

Table 2-13
Estimated Worldwide PLD Consumption by Region (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Worldwide Total	**1,873**	**2,103**	**2,081**	**2,332**	**2,866**	**3,488**	**4,154**
Americas	1,116	1,253	1,228	1,375	1,679	2,040	2,428
Japan	255	280	290	337	416	505	600
Europe, Middle East, and Africa	375	425	438	477	593	723	860
Asia/Pacific	127	145	126	142	178	220	266

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1998)

Table 2-14
Estimated Worldwide PLD Consumption by Region (Percentage Growth)

	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Worldwide Total	**10.1**	**12.3**	**-1.0**	**12.0**	**22.9**	**21.7**	**19.1**	**14.6**
Americas	7.8	12.3	-2.0	12.0	22.1	21.5	19.0	14.1
Japan	20.1	9.8	3.5	16.2	23.6	21.4	18.7	16.5
Europe, Middle East, and Africa	15.5	13.3	3.0	9.0	24.2	22.0	19.0	15.1
Asia/Pacific	-1.8	14.2	-13.1	13.0	25.3	23.1	21.0	12.9

Source: Dataquest (October 1998)

Table 2-15
Estimated Worldwide PLD Consumption by Region (Percentage of Revenue)

	1996	1997	1998	1999	2000	2001	2001
Worldwide Total	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**
Americas	59.6	59.6	59.0	59.0	58.6	58.5	58.5
Japan	13.6	13.3	13.9	14.4	14.5	14.5	14.4
Europe, Middle East, and Africa	20.0	20.2	21.0	20.5	20.7	20.7	20.7
Asia/Pacific	6.8	6.9	6.1	6.1	6.2	6.3	6.4

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1998)

Table 2-16
Estimated Worldwide PLD Consumption by Logic Complexity (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Total CMOS PLD	1,877	2,103	2,081	2,332	2,866	3,488	4,154
Total SPLD	316	271	214	184	169	154	139
Total High Density (CPLD + FPGA)	1,561	1,832	1,866	2,148	2,697	3,334	4,015
CPLD	592	771	794	885	1,105	1,340	1,587
FPGA	969	1,061	1,072	1,262	1,591	1,994	2,428

Note: Columns may not add to totals shown because of rounding.
CPLDs are product-term-only devices in this forecast.
Source: Dataquest (October 1998)

Table 2-17
Estimated Worldwide PLD Consumption by Logic Complexity (Percentage Growth)

	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Total CMOS PLD	10.4	12.0	-1.1	12.1	22.9	21.7	19.1	14.6
Total SPLD	-21.6	-14.2	-21.0	-14.0	-8.0	-8.9	-9.9	-12.5
Total High Density (CPLD + FPGA)	20.3	17.3	1.9	15.1	25.5	23.6	20.4	17.0
CPLD	16.8	30.2	3.0	11.5	24.9	21.2	18.5	15.5
FPGA	22.5	9.5	1.1	17.7	26.0	25.3	21.7	18.0

Note: Columns may not add to totals shown because of rounding.
CPLDs are product-term-only devices in this forecast.
Source: Dataquest (October 1998)

Chapter 3
ASIC Application Forecasts

SLI Application Forecasts

The SLI market is one of the fastest-growing segments of the semiconductor industry. The key to understanding where the growth will be is to start with application forecasts for ASICs and ASSPs, then project the percentage of each application market that will move to SLI. Dataquest considers a device to fit the SLI definition if it contains an on-chip compute engine (on-chip microprocessor core, on-chip DSP, or on-chip MPEG), memory, and logic and if it is dedicated to a specific application.

Provided in this chapter are detailed forecasts for the communications and consumer markets for both SLI ASICs and SLI ASSPs. Top-line estimates for the SLI data processing market and other identified SLI markets are then combined with the SLI communications and consumer markets to get the estimated total application demand for SLI ASICs and SLI ASSPs.

Table 3-1 shows the worldwide communications ASIC market split into wireless and wired communications, then into each submarket. Table 3-2 shows the estimated percentage of SLI revenue for each submarket shown in the first table. Table 3-3 shows the worldwide SLI communications market, which is the total ASIC communications market shown in the first table multiplied by the estimated market percentages for SLI ASICs shown in the second table. Tables 3-4 through 3-6 show the same progression for worldwide communications ASSPs. Tables 3-7 through 3-9 show worldwide consumer ASIC and SLI ASIC consumption, and Tables 3-10 through 3-12 show worldwide consumer ASSP and SLI ASSP consumption. Tables 3-13 and 3-14 show the estimated total worldwide SLI ASIC and SLI ASSP consumption by application market.

Table 3-1
Estimated Worldwide ASIC Communications Consumption (Millions of Dollars)

	1997	1998	1999	2000	2001	2002
Wireless Communications						
Analog Cellular	285	167	103	61	29	10
Digital Cellular/PCS	2,424	2,521	2,702	2,862	3,113	3,504
Pagers (One- and Two-Way)	-	-	-	-	-	-
Infrastructure	234	265	310	350	410	447
Other Mobile	138	142	139	136	135	132
Total	3,081	3,095	3,254	3,409	3,687	4,093
Cordless Phones	8	5	-	-	-	-
Total Wireless	**3,089**	**3,100**	**3,254**	**3,409**	**3,687**	**4,093**
Wired Communications						
LAN	602	593	699	741	768	797
WAN	200	245	331	428	558	629
Premise Switching	253	274	354	300	336	376
Modem (Analog and Digital)	35	42	44	46	51	52
Remote Access	72	103	150	214	281	336
Public Switching	467	476	521	555	593	633
Public Transmission	240	273	323	382	463	562
Total Identified	1,870	2,005	2,422	2,666	3,051	3,385
Other Wired	296	366	429	449	491	537
Total Wired	**2,166**	**2,371**	**2,851**	**3,115**	**3,541**	**3,922**
Total Wireless and Wired	**5,255**	**5,471**	**6,105**	**6,524**	**7,228**	**8,015**

Source: Dataquest (October 1998)

Table 3-2
Estimated Worldwide ASIC Communications Consumption (Percentage SLI)

	1997	1998	1999	2000	2001	2002
Wireless Communications						
Analog Cellular	0	0	0	0	0	0
Digital Cellular/PCS	65.0	70.0	76.0	82.0	88.0	95.0
Pagers (One- and Two-Way)	0	0	0	0	0	0
Infrastructure	55.0	59.0	64.0	70.0	75.0	80.0
Other Mobile	40.0	43.0	47.0	52.0	60.0	70.0
Cordless Phones	0	0	0	0	0	0
Wired Communications						
LAN	3.0	5.0	10.0	17.0	27.0	40.0
WAN	1.0	3.0	7.0	12.0	18.0	25.0
Premise Switching	2.0	3.0	4.0	5.0	6.0	8.0
Modem (Analog and Digital)	85.0	85.0	86.0	87.0	88.0	90.0
Remote Access	50.0	53.0	57.0	61.0	66.0	70.0
Public Switching	2.0	3.0	4.0	5.0	6.0	8.0
Public Transmission	0.3	0.6	1.0	2.0	3.0	4.0
Other Wired	0.1	0.2	0.3	0.4	0.5	0.6

Source: Dataquest (October 1998)

Table 3-3
Estimated Worldwide SLI ASIC Communications Consumption (Millions of Dollars)

	1997	1998	1999	2000	2001	2002
Wireless Communications						
Analog Cellular	-	-	-	-	-	-
Digital Cellular/PCS	1,576	1,765	2,054	2,347	2,739	3,329
Pagers (One- and Two-Way)	-	-	-	-	-	-
Infrastructure	129	156	198	245	308	358
Other Mobile	55	61	65	71	81	92
Total	1,760	1,982	2,317	2,663	3,128	3,779
Cordless Phones	-	-	-	-	-	-
Total Wireless	**1,760**	**1,982**	**2,317**	**2,663**	**3,128**	**3,779**
Wired Communications						
LAN	18	30	70	126	207	319
WAN	2	7	23	51	100	157
Premise Switching	5	8	14	15	20	30
Modem (Analog and Digital)	30	35	37	40	45	47
Remote Access	36	55	86	131	185	235
Public Switching	9	14	21	28	36	51
Public Transmission	1	2	3	8	14	22
Total Identified	101	151	254	398	608	861
Other Wired	-	1	1	2	2	3
Total Wired	**102**	**152**	**256**	**400**	**610**	**865**
Total Wireless and Wired	**1,861**	**2,134**	**2,573**	**3,063**	**3,738**	**4,643**

Source: Dataquest (October 1998)

Table 3-4
Estimated Worldwide ASSP Communications Consumption (Millions of Dollars)

	1997	1998	1999	2000	2001	2002
Wireless Communications						
Analog Cellular	201	153	128	117	98	54
Digital Cellular/PCS	2,243	2,458	2,778	3,339	3,684	4,415
Pagers (One- and Two-Way)	77	125	186	283	356	455
Infrastructure	889	1,109	1,301	1,497	1,712	1,925
Other Mobile	389	449	509	576	622	648
Total	3,798	4,294	4,902	5,812	6,472	7,497
Cordless Phones	515	626	744	881	1,014	1,115
Total Wireless	**4,314**	**4,920**	**5,646**	**6,693**	**7,486**	**8,612**
Wired Communications						
LAN	1,370	1,254	1,352	1,476	1,649	1,900
WAN	243	289	375	465	584	646
Premise Switching	239	256	336	289	328	372
Modem (Analog and Digital)	823	849	773	701	737	740
Remote Access	292	405	569	785	995	1,188
Public Switching	832	839	930	1,055	1,087	1,176
Public Transmission	472	563	698	826	1,002	1,214
Total Identified	4,271	4,454	5,034	5,597	6,382	7,236
Other Wired	592	732	837	891	961	1,037
Total Wired	**4,862**	**5,186**	**5,870**	**6,487**	**7,343**	**8,273**
Total Wireless and Wired	**9,176**	**10,106**	**11,516**	**13,180**	**14,829**	**16,885**

Source: Dataquest (October 1998)

Table 3-5
Estimated Worldwide ASSP Communications Consumption (Percentage SLI)

	1997	1998	1999	2000	2001	2002
Wireless Communications						
Analog Cellular	0	0	0	0	0	0
Digital Cellular/PCS	35.0	37.0	41.0	46.0	51.0	55.0
Pagers (One- and Two-Way)	0	0	1.0	2.0	3.0	5.0
Infrastructure	25.0	28.0	31.0	36.0	41.0	47.0
Other Mobile	20.0	22.0	25.0	29.0	34.0	40.0
Cordless Phones	0	0	0	0	0	0
Wired Communications						
LAN	0	1.0	4.0	8.0	14.0	20.0
WAN	0	1.0	2.0	6.0	10.0	15.0
Premise Switching	1.0	1.5	2.0	2.6	3.1	4.0
Modem (Analog and Digital)	85.0	85.0	86.0	87.0	88.0	90.0
Remote Access	40.0	43.0	46.0	50.0	55.0	60.0
Public Switching	1.0	1.2	1.7	2.3	3.0	4.0
Public Transmission	0.3	0.6	1.0	1.5	2.0	3.0
Other Wired	0.1	0.2	0.3	0.4	0.5	0.6

Source: Dataquest (October 1998)

Table 3-6
Estimated Worldwide SLI ASSP Communications Consumption (Millions of Dollars)

	1997	1998	1999	2000	2001	2002
Wireless Communications						
Analog Cellular	0	0	0	0	0	0
Digital Cellular/PCS	785	909	1,139	1,536	1,879	2,428
Pagers (One- and Two-Way)	-	-	2	6	11	23
Infrastructure	222	311	403	539	702	905
Other Mobile	78	99	127	167	212	259
Total	1,085	1,319	1,671	2,248	2,803	3,615
Cordless Phones	-	-	-	-	-	-
Total Wireless	**1,085**	**1,319**	**1,671**	**2,248**	**2,803**	**3,615**
Wired Communications						
LAN	-	13	54	118	231	380
WAN	-	3	8	28	58	97
Premise Switching	2	4	7	8	10	15
Modem (Analog and Digital)	699	721	665	609	649	666
Remote Access	117	174	262	393	547	713
Public Switching	8	10	16	24	33	47
Public Transmission	1	3	7	12	20	36
Total Identified	828	928	1,018	1,192	1,548	1,954
Other Wired	1	1	3	4	5	6
Total Wired	**829**	**930**	**1,020**	**1,196**	**1,553**	**1,960**
Total Wireless and Wired	**1,914**	**2,248**	**2,692**	**3,443**	**4,356**	**5,575**

Source: Dataquest (October 1998)

Table 3-7
Estimated Worldwide ASIC Consumer Consumption (Millions of Dollars)

	1997	1998	1999	2000	2001	2002
Digital Cable Set-Top Boxes	128	242	378	474	552	540
Digital Satellite Set-Top Boxes	295	232	138	87	83	80
DVD Video Players	9	15	28	35	62	97
Video CD Players	38	34	20	10	8	5
Next-Generation Video Game Consoles	1,408	1,405	1,177	1,045	1,216	1,632
DTV Receivers	-	1	6	28	159	274
Digital Still Cameras	166	75	69	55	49	54
Digital Camcorders	156	211	221	211	209	214
Other Next-Generation Products	7	11	16	29	46	71
Total	**2,207**	**2,226**	**2,053**	**1,974**	**2,383**	**2,967**

Source: Dataquest (October 1998)

Table 3-8
Estimated Worldwide ASIC Consumer Consumption (Percentage SLI)

	1997	1998	1999	2000	2001	2002
Digital Cable Set-Top Boxes	100	100	100	100	100	100
Digital Satellite Set-Top Boxes	100	100	100	100	100	100
DVD Video Players	100	100	100	100	100	100
Video CD Players	0	0	0	0	0	0
Next-Generation Video Game Consoles	62	66	70	74	79	85
DTV Receivers	100	100	100	100	100	100
Digital Still Cameras	100	100	100	100	100	100
Digital Camcorders	10	13	16	21	25	30
Other Next-Generation Products	50	53	58	62	66	70

Source: Dataquest (October 1998)

Table 3-9
Estimated Worldwide SLI ASIC Consumer Consumption (Millions of Dollars)

	1997	1998	1999	2000	2001	2002
Digital Cable Set-Top Boxes	128	242	378	474	552	540
Digital Satellite Set-Top Boxes	295	232	138	87	83	80
DVD Video Players	9	15	28	35	62	97
Video CD Players	-	-	-	-	-	-
Next-Generation Video Game Consoles	873	927	824	773	961	1,387
DTV Receivers	-	1	6	28	159	274
Digital Still Cameras	166	75	69	55	49	54
Digital Camcorders	16	27	35	44	52	64
Other Next-Generation Products	3	6	9	18	30	49
Total	**1,490**	**1,525**	**1,488**	**1,515**	**1,948**	**2,546**

Source: Dataquest (October 1998)

Table 3-10
Estimated Worldwide ASSP Consumer Consumption (Millions of Dollars)

	1997	1998	1999	2000	2001	2002
Digital Cable Set-Top Boxes	27	68	186	367	583	572
Digital Satellite Set-Top Boxes	299	546	928	1,269	1,422	1,640
DVD Video Players	41	74	154	228	407	532
Video CD Players	239	310	357	400	413	457
Next-Generation Video Game Consoles	-	-	-	-	-	-
DTV Receivers	-	-	3	23	166	286
Digital Still Cameras	-	108	131	135	143	156
Digital Camcorders	69	152	198	231	276	290
Other Next-Generation Products	2	9	21	40	73	132
Total	**677**	**1,267**	**1,978**	**2,693**	**3,483**	**4,065**

Source: Dataquest (October 1998)

Table 3-11
Estimated Worldwide ASSP Consumer Consumption (Percentage SLI)

	1997	1998	1999	2000	2001	2002
Digital Cable Set-Top Boxes	100	100	100	100	100	100
Digital Satellite Set-Top Boxes	100	100	100	100	100	100
DVD Video Players	100	100	100	100	100	100
Video CD Players	100	100	100	100	100	100
Next-Generation Video Game Consoles	0	0	0	0	0	0
DTV Receivers	100	100	100	100	100	100
Digital Still Cameras	100	100	100	100	100	100
Digital Camcorders	10	13	16	21	25	30
Other Next-Generation Products	50	53	58	62	66	70

Source: Dataquest (October 1998)

Table 3-12
Estimated Worldwide SLI ASSP Consumer Consumption (Millions of Dollars)

	1997	1998	1999	2000	2001	2002
Digital Cable Set-Top Boxes	27	68	186	367	583	572
Digital Satellite Set-Top Boxes	299	546	928	1,269	1,422	1,640
DVD Video Players	41	74	154	228	407	532
Video CD Players	239	310	357	400	413	457
Next-Generation Video Game Consoles	-	-	-	-	-	-
DTV Receivers	-	-	3	23	166	286
Digital Still Cameras	-	108	131	135	143	156
Digital Camcorders	7	20	32	49	69	87
Other Next-Generation Products	1	5	12	25	48	93
Total	**614**	**1,131**	**1,803**	**2,495**	**3,251**	**3,823**

Source: Dataquest (October 1998)

Table 3-13
Estimated Worldwide SLI ASIC Consumption by Application Market (Millions of Dollars)

	1997	1998	1999	2000	2001	2002
Data Processing	395	673	1,105	1,761	2,549	3,745
Communications	1,861	2,134	2,573	3,063	3,738	4,643
Consumer	1,490	1,525	1,488	1,515	1,948	2,546
Other Identified	31	57	95	171	273	426
Total	**3,778**	**4,389**	**5,261**	**6,508**	**8,508**	**11,361**

Source: Dataquest (October 1998)

Table 3-14
Estimated Worldwide SLI ASSP Consumption by Application Market
(Millions of Dollars)

	1997	1998	1999	2000	2001	2002
Data Processing	1,010	1,299	1,625	2,003	2,439	2,997
Communications	1,914	2,248	2,692	3,443	4,356	5,575
Consumer	614	1,131	1,803	2,495	3,251	3,823
Other Identified	42	50	63	88	133	216
Total	**3,580**	**4,729**	**6,187**	**8,029**	**10,179**	**12,610**

Source: Dataquest (October 1998)

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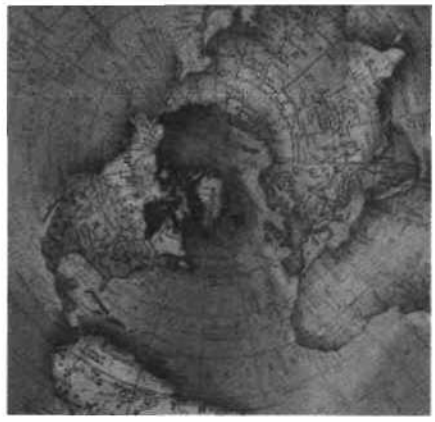

Dataquest

Worldwide ASIC Forecast: Spring 1998

Market Statistics

Program: ASIC/SLI Worldwide
Product Code: ASIC-WW-MS-9802
Publication Date: June 1, 1998
Filing: Market Statistics

Worldwide ASIC Forecast: Spring 1998

Market Statistics

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Chapter 1
The 1998 Worldwide ASIC Market

Introduction

This document contains detailed information on Dataquest's view of the application-specific integrated circuit (ASIC) market. A new section on applications has been added to provide a better understanding of ASIC consumption by region. Included in this document are the following:

- 1998-2002 ASIC consumption forecast
- 1998-2002 gate array consumption forecast
- 1998-2002 cell-based IC (CBIC) consumption forecast
- 1998-2002 programmable logic device (PLD) consumption forecast
- 1998-2002 ASIC application forecasts by region

More detailed data on this market may be requested through Dataquest's client inquiry service. Qualitative analysis of this data is provided in the Dataquest Market Trends and other documents located in the binder of the same name.

Segmentation

This section outlines the market segments that are specific to this document. Dataquest's objective is to provide data along lines of segmentation that are logical, appropriate to the industry in question, and immediately useful to clients.

Dataquest defines the ASIC market according to the segmentation scheme in Figure 1-1.

The figure shows Dataquest's segmentation into the two main categories of standard logic and ASIC. The ASIC family tree breaks out ASICs as follows: PLDs, gate arrays, CBICs, and full-custom ICs. CBICs and full-custom ICs are personalized by altering the full set of masks, whereas PLDs and gate arrays are personalized by electrically programming the devices or by altering only the final layers of interconnect.

Definitions

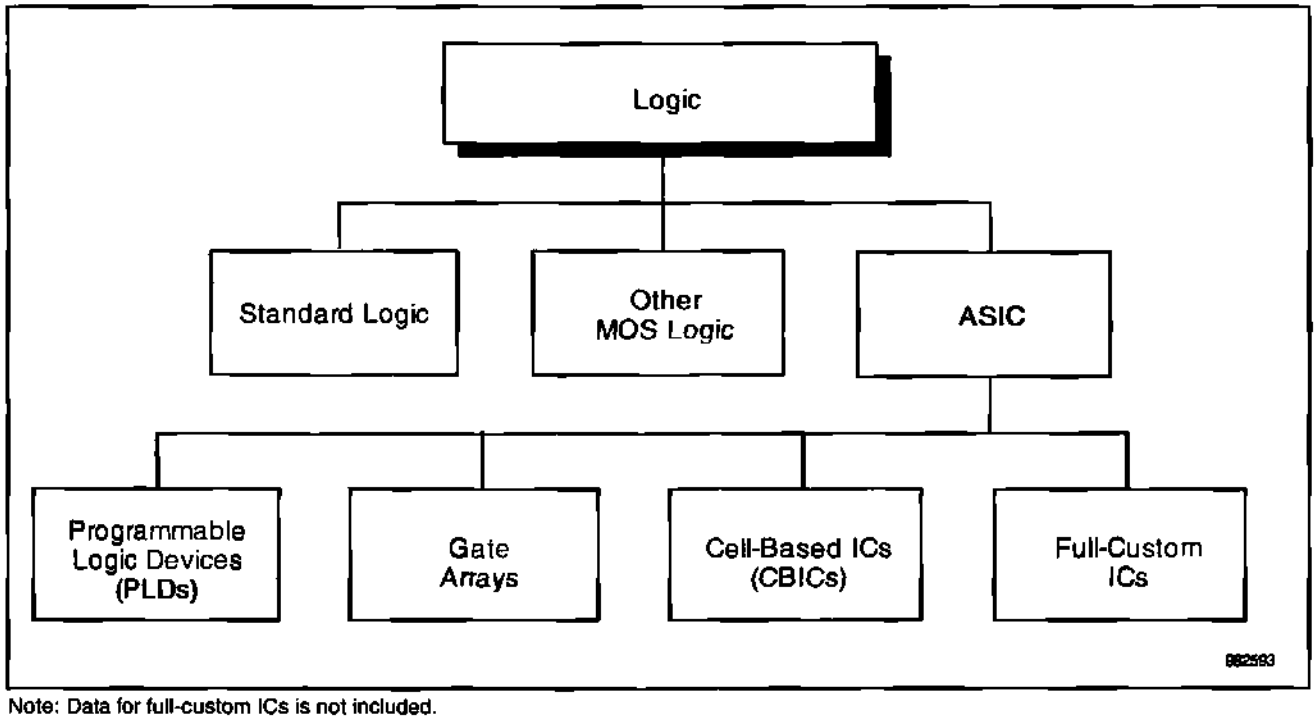
This section lists the definitions used by Dataquest to present the data in this document.

Product Definitions

Application-Specific Integrated Circuits

The term ASIC is used to describe all IC products customized for a single user. ASIC products are a combination of digital, mixed-signal, and analog products. Customized ICs purchased by more than one user become standard products and are no longer counted as ASICs.

Figure 1-1
ASIC Family Tree



Note: Data for full-custom ICs is not included.
Source: Dataquest (May 1998)

Programmable Logic Devices

PLDs are defined as ICs programmed after assembly. Memory devices such as PROM and ROM are not included in this market segment. There has been some confusion in the industry regarding complex programmable logic device (CPLD) and field-programmable gate array (FPGA) definitions. Dataquest has simplified the PLD subcategories as follows:

- Simple programmable logic devices (SPLDs) are commonly referred to as programmable array logic (PAL). PAL devices consist of an array of AND gates, called product terms, connected to an array of AND gates or fixed OR gates. These devices are capable of providing up to two levels of logic without using additional input, output, or I/O cells or pins.
- High-density PLDs are a combination of FPGAs and CPLDs.

Gate Arrays

Gate arrays are ASICs that contain a configuration of uncommitted elements in a prefabricated base wafer. They are customized by interconnecting these elements with one or more routing layers. Included in this category are traditional gate arrays (channeled and sea-of-gates architecture) and embedded gate arrays (channeled or sea-of-gates architecture that also include megacells such as SRAM diffused into the gate array base wafer).

Cell-Based ICs

CBICs are ASICs that are customized using a full set of masks and use automatic place-and-route tools. Included in this category are traditional standard cells (fixed-height/fixed-width cells) as well as megacells (variable-height/variable-width cells) and compiled cells.

Full-Custom ICs

Full-custom ICs are defined as ASIC devices that are produced for a single user using a full set of masks. This process involves manual routing and placement of cells.

Revenue Classification

Because systems may be fabricated, assembled, and sold in several different locations, Dataquest's regional device consumption is defined according to the shipping destination.

Consumption estimates include the following five sources of revenue:

- Intracompany revenue (sales to internal divisions)
- Nonrecurring engineering (NRE) revenue
- ASIC software revenue
- PLD development kit revenue
- Device production revenue

Despite the care taken in gathering, analyzing, and categorizing the data in a meaningful way, careful attention must be paid to the definitions and assumptions used herein when interpreting the estimates presented in this document. Various companies, government agencies, and trade associations may use slightly different definitions of product categories and regional groupings, or they may include different companies in their summaries. These differences should be kept in mind when making comparisons between data and numbers provided by Dataquest and those provided by other suppliers.

Merchant versus Captive Consumption

Dataquest includes all revenue, both merchant and captive, for semiconductor suppliers selling to the merchant market. Dataquest's consumption estimates do not include captive-only manufacturing companies represented by companies such as Digital Equipment Corporation, Northern Telecom, or Unisys that do not sell semiconductor products in the merchant market.

Regional Definitions

Americas

North America: Includes Canada, Mexico, and the United States (50 states).

South America

Central America

Japan

Japan is the only single-country region.

Europe, Africa, and the Middle East

Western Europe: Includes Austria, Belgium, Denmark, Eire (Ireland), Finland, France, Germany (including former East Germany), Greece, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, the United Kingdom, and rest of western Europe (Andorra, Cyprus, Gibraltar, Liechtenstein, Monaco, San Marino, Vatican City, Iceland, Malta, and Turkey).

Eastern Europe: Includes Albania, Bulgaria, the Czech Republic and Slovakia, Estonia, Hungary, Latvia, Lithuania, Poland, Romania, the republics of the former Yugoslavia, and the republics of the former USSR (Belarus, Russian Federation, Ukraine, Georgia, Moldova, Armenia, Azerbaijan, Kazakhstan, Uzbekistan, Tadjikistan, Kyrgyzstan, and Turkmenistan).

Asia/Pacific

Includes Hong Kong, Singapore, South Korea, Taiwan, Australia, Bangladesh, Cambodia, China, India, Indonesia, Laos, Malaysia, Maldives, Myanmar, Nepal, New Zealand, Pakistan, the Philippines, Sri Lanka, Thailand, and Vietnam.

Line Item Definitions

Factory revenue is defined as the money value received by a semiconductor manufacturer for its products. Revenue from the sale of semiconductors sold either as finished goods, die, or wafers to another semiconductor vendor for resale is attributed to the semiconductor vendor that sells the product to a distributor or equipment manufacturer.

Forecast Methodology and Assumptions

Dataquest publishes five-year factory revenue forecasts for the ASIC market during the first and third quarter of each year. In doing so, Dataquest utilizes a variety of forecasting techniques (both qualitative and quantitative) that vary by technology area. An overview of Dataquest forecasting techniques can be found in the Dataquest Research Methodology guide.

ASIC Forecast Methodology

Dataquest's ASIC forecast methodology includes the following steps:

- Formally and informally survey the leading ASIC vendors (in gate arrays, CBICs, and PLDs) throughout the year for their expectations, as well as for their views of the application markets in which they participate
- Formally survey ASIC users for their expected buying patterns, in addition to their views on the growth of the application markets in which they participate

- Examine statistics provided by a number of industry and government organizations (such as the World Semiconductor Trade Statistics, the Japanese Ministry of International Trade and Industry, and the U.S. Department of Commerce) for up-to-date monthly trends
- Perform time-series analysis as well as apply judgmental industry knowledge to product and application trends

ASIC Forecast Assumptions

ASIC

The worldwide ASIC market in 1998 is forecast to be quite similar to the 1997 market. For the total ASIC market, Dataquest expects 11.4 percent growth in 1998 (excluding full-custom ICs), compared to 11.6 in 1997. This is lower than the fall 1997 forecast in all regions, with Japan and Asia/Pacific reduced the most.

Dataquest has reduced the 1998 growth rates for all products since the fall forecast, with the highest percentage reductions in PLDs. PLDs will have a tough year in 1998. Major price wars and inventory reductions took their toll in 1997, and we think 1998 will be worse. In 1997, PLDs grew about 12.3 percent. The current forecast for 1998 shows only 11 percent growth—this is optimistic, and there could easily be single-digit growth if the second half does not turn around.

The long-term view for ASIC products is that PLDs will continue to replace gate arrays on the low end and that cell-based ICs continue to beat gate arrays on the high end. The net effect is that PLDs should grow at a 20 percent compound annual growth rate (CAGR) for the next five years, cell-based ICs should grow at a 27 percent five-year CAGR, and gate arrays should decline at about a 5 percent CAGR. Custom ICs (devices designed at the transistor level) are not the place to be. These devices are rapidly being replaced by cell-based ICs. Dataquest forecasts a 23 percent decline in 1998 and a 33 percent decline over five years.

Cell-Based ICs

Cell-based ICs are the place to be. This is now the largest market, accounting for $11 billion of the market's $18 billion total in 1998. Cell-based ICs are the primary method used to achieve system-level integration (SLI), or systems on a chip. Dataquest's ASIC/SLI Market Trends report, ASIC Suppliers Target System-Level Integration (April 1998), predicts that the SLI market will be about $4.7 billion in 1998, rising to $21 billion in 2002. Most of this will result from using cell-based ICs. Key assumptions for this forecast as as follows:

- Cell-based ICs tend to be used in high-volume or high-complexity applications.
- Cell-based ICs are widely used in the communications market, and this market represents over 30 percent of worldwide cell-based IC consumption.
- Data processing system designers are moving to cell-based ICs from gate arrays to improve performance, increase functionality, and lower costs.
- Consumer systems are rapidly incorporating cell-based ICs over gate arrays because of the lower cost structure and increased functionality.

Gate Arrays

Gate array usage is declining in favor of cell-based ICs and PLDs. Japan, once the gate array nation, is now moving quickly to cell-based ICs because of the lower cost structure, increased functionality, and increased performance they offer. Key assumptions for the gate array forecast include the following:

- Gate arrays have entered the decline phase of the product life cycle.
- Tier-one ASIC suppliers will continue to reduce R&D on gate array technology, and many will completely abandon the market.
- Tier-two ASIC suppliers and foundries will become stronger players in this market.
- Asia/Pacific will maintain gate array technology longer than the other regions, followed by Japan.
- PLD suppliers will continue to capture the low-end gate array market, meaning below 100,000 gates, over the next three years and the market below 200,000 gates starting in two years.

PLDs

PLDs are one of the fastest-growing areas in the ASIC market. PLD growth will come from five-year areas as follows:

- Standard logic replacement
- Gate array replacement
- ASIC prototyping
- New applications created by the instant time to market and low risk of PLDs
- New applications created by in-system programming (ISP), including reconfigurable computing

Exchange Rates

Dataquest uses an average annual exchange rate in converting revenue to U.S. dollar amounts. Table 1-1 outlines these rates for 1995 through 1997.

Table 1-1
Exchange Rates

	1996	1997	1998*
Japan (Yen/U.S.$)	108.81	117.93	128.85
France (Franc/U.S.$)	5.12	5.87	6.12
Germany (Deutsche Mark/U.S.$)	1.50	1.74	1.82
United Kingdom (U.S.$/Pound Sterling)	0.64	0.61	0.60

*Preliminary
Source: Dataquest (April 1998)

Chapter 2
ASIC Product Forecasts

Tables 2-1 through 2-17 show ASIC product trends.

Table 2-1
Estimated Worldwide ASIC Consumption by Technology (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Total ASIC	**16,526**	**18,043**	**19,574**	**23,153**	**28,004**	**33,025**	**39,993**	**17.3**
Digital ASIC	15,461	16,625	17,829	20,866	24,986	29,256	35,184	16.2
Mixed-Signal ASIC	1,065	1,418	1,745	2,287	3,018	3,769	4,810	27.7

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 2-2
Estimated Worldwide ASIC Consumption by Product (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Total ASIC	**16,526**	**18,043**	**19,574**	**23,153**	**28,004**	**33,025**	**39,993**
Gate Array	5,612	5,260	4,911	4,731	4,522	4,280	4,007
PLD	1,873	2,103	2,339	2,899	3,564	4,288	5,249
Cell-Based IC	7,317	9,163	11,159	14,701	19,360	24,108	30,533
Full-Custom	1,724	1,517	1,164	823	557	349	205

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 2-3
Estimated Worldwide ASIC Consumption by Product (Percentage Growth)

	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Total ASIC	**6.2**	**9.2**	**8.5**	**18.3**	**21.0**	**17.9**	**21.1**	**17.3**
Gate Array	-6.1	-6.3	-6.6	-3.7	-4.4	-5.4	-6.4	-5.3
PLD	10.1	12.3	11.2	23.9	23.0	20.3	22.4	20.1
Cell-Based IC	27.3	25.2	21.8	31.7	31.7	24.5	26.7	27.2
Full-Custom	-19.5	-12.0	-23.2	-29.4	-32.3	-37.3	-41.4	-33.0

Source: Dataquest (April 1998)

Table 2-4
Estimated Worldwide ASIC Consumption by Region (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Worldwide Total	**14,802**	**16,526**	**18,409**	**22,330**	**27,446**	**32,675**	**39,789**
Americas	5,986	7,099	8,094	9,912	12,296	14,795	18,200
Japan	4,402	4,576	4,775	5,580	6,574	7,581	8,935
Europe, Africa, and Middle East	2,825	3,189	3,647	4,458	5,561	6,674	8,210
Asia/Pacific	1,589	1,662	1,893	2,380	3,015	3,625	4,443

Notes: Columns may not add to totals shown because of rounding.
Full-custom ICs are excluded from this table.
Source: Dataquest (April 1998)

Table 2-5
Estimated Worldwide ASIC Consumption by Region (Percentage Growth)

	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Worldwide Total	**10.3**	**11.6**	**11.4**	**21.3**	**22.9**	**19.1**	**21.8**	**19.2**
Americas	11.3	18.6	14.0	22.5	24.1	20.3	23.0	20.7
Japan	2.4	4.0	4.3	16.9	17.8	15.3	17.9	14.3
Europe, Africa, and Middle East	22.2	12.9	14.4	22.2	24.7	20.0	23.0	20.8
Asia/Pacific	10.7	4.6	13.9	25.7	26.7	20.2	22.6	21.7

Note: Full-custom ICs are excluded from this table.
Source: Dataquest (April 1998)

Table 2-6
Estimated Worldwide ASIC Consumption by Region (Percentage of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Worldwide Total	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**
Americas	40.4	43.0	44.0	44.4	44.8	45.3	45.7
Japan	29.7	27.7	25.9	25.0	24.0	23.2	22.5
Europe, Africa, and Middle East	19.1	19.3	19.8	20.0	20.3	20.4	20.6
Asia/Pacific	10.7	10.1	10.3	10.7	11.0	11.1	11.2

Note: Full-custom ICs are excluded from this table.
Source: Dataquest (April 1998)

Table 2-7
Estimated Worldwide Cell-Based IC Consumption by Region (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Worldwide Total	**7,317**	**9,163**	**11,159**	**14,701**	**19,360**	**24,108**	**30,533**
Americas	2,788	4,098	5,203	6,828	8,959	11,171	14,145
Japan	1,839	1,997	2,251	3,018	3,986	4,982	6,319
Europe, Africa, and Middle East	1,753	2,013	2,421	3,123	4,096	5,077	6,436
Asia/Pacific	937	1,055	1,284	1,732	2,319	2,877	3,634

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 2-8
Estimated Worldwide Cell-Based IC Consumption by Region (Percentage Growth)

	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Worldwide Total	**27.3**	**25.2**	**21.8**	**31.7**	**31.7**	**24.5**	**26.7**	**27.2**
Americas	25.1	47.0	27.0	31.2	31.2	24.7	26.6	28.1
Japan	18.2	8.6	12.7	34.1	32.1	25.0	26.8	25.9
Europe, Africa, and Middle East	34.5	14.8	20.3	29.0	31.2	24.0	26.8	26.2
Asia/Pacific	42.3	12.6	21.7	34.9	33.9	24.1	26.3	28.1

Source: Dataquest (April 1998)

Table 2-9
Estimated Worldwide Cell-Based IC Consumption by Region (Percentage of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Worldwide Total	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**
Americas	38.1	44.7	46.6	46.4	46.3	46.3	46.3
Japan	25.1	21.8	20.2	20.5	20.6	20.7	20.7
Europe, Africa, and Middle East	24.0	22.0	21.7	21.2	21.2	21.1	21.1
Asia/Pacific	12.8	11.5	11.5	11.8	12.0	11.9	11.9

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 2-10
Estimated Worldwide Gate Array Consumption by Region (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Worldwide Total	**5,612**	**5,260**	**4,911**	**4,731**	**4,522**	**4,280**	**4,007**
Americas	2,082	1,748	1,511	1,381	1,257	1,136	1,033
Japan	2,308	2,299	2,222	2,190	2,129	2,042	1,929
Europe, Africa, and Middle East	697	751	741	728	711	688	657
Asia/Pacific	525	462	438	432	425	414	387

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 2-11
Estimated Worldwide Gate Array Consumption by Region (Percentage Growth)

	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Worldwide Total	**-6.1**	**-6.3**	**-6.6**	**-3.7**	**-4.4**	**-5.4**	**-6.4**	**-5.3**
Americas	-1.6	-16.0	-13.6	-8.6	-9.0	-9.6	-9.1	-10.0
Japan	-8.8	-0.4	-3.4	-1.4	-2.8	-4.1	-5.5	-3.4
Europe, Africa, and Middle East	1.9	7.7	-1.3	-1.8	-2.3	-3.2	-4.5	-2.6
Asia/Pacific	-18.9	-12.0	-5.3	-1.2	-1.7	-2.6	-6.4	-3.5

Source: Dataquest (April 1998)

Table 2-12
Estimated Worldwide Gate Array Consumption by Region (Percentage of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Worldwide Total	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**
Americas	37.1	33.2	30.8	29.2	27.8	26.5	25.8
Japan	41.1	43.7	45.2	46.3	47.1	47.7	48.2
Europe, Africa, and Middle East	12.4	14.3	15.1	15.4	15.7	16.1	16.4
Asia/Pacific	9.4	8.8	8.9	9.1	9.4	9.7	9.7

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 2-13
Estimated Worldwide PLD Consumption by Region (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Worldwide Total	**1,873**	**2,103**	**2,339**	**2,899**	**3,564**	**4,288**	**5,249**
Americas	1,116	1,253	1,380	1,704	2,080	2,488	3,023
Japan	255	280	302	371	459	557	687
Europe, Africa, and Middle East	375	425	485	607	754	909	1,118
Asia/Pacific	127	145	172	216	271	334	422

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 2-14
Estimated Worldwide PLD Consumption by Region (Percentage Growth)

	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Worldwide Total	**10.1**	**12.3**	**11.2**	**23.9**	**23.0**	**20.3**	**22.4**	**20.1**
Americas	7.8	12.3	10.1	23.5	22.1	19.6	21.5	19.3
Japan	20.1	9.8	7.9	22.9	23.6	21.4	23.2	19.6
Europe, Africa, and Middle East	15.5	13.3	14.2	25.1	24.2	20.5	23.0	21.3
Asia/Pacific	-1.8	14.2	18.6	25.8	25.3	23.1	26.4	23.8

Source: Dataquest (April 1998)

Table 2-15
Estimated Worldwide PLD Consumption by Region (Percentage of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Worldwide Total	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**
Americas	59.6	59.6	59.0	58.8	58.4	58.0	57.6
Japan	13.6	13.3	12.9	12.8	12.9	13.0	13.1
Europe, Africa, and Middle East	20.0	20.2	20.8	20.9	21.2	21.2	21.3
Asia/Pacific	6.8	6.9	7.4	7.5	7.6	7.8	8.0

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 2-16
Estimated Worldwide PLD Consumption by Logic Complexity (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Total CMOS PLD	**1,873**	**2,103**	**2,339**	**2,899**	**3,564**	**4,288**	**5,249**
Total SPLD	316	271	238	203	169	138	109
Total High-Density(CPLD + FPGA)	1,557	1,832	2,101	2,696	3,395	4,150	5,140

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 2-17
Estimated Worldwide PLD Consumption by Logic Complexity (Percentage Growth)

	1996	1997	1998	1999	2000	2001	2002	CAGR (%) 1997-2002
Total CMOS PLD	**10.1**	**12.3**	**11.2**	**24.0**	**22.9**	**20.3**	**22.4**	**20.1**
Total SPLD	-21.6	-14.2	-12.2	-14.5	-16.8	-18.2	-21.3	-16.7
Total High-Density(CPLD + FPGA)	20.0	17.7	14.7	28.3	25.9	22.2	23.9	22.9

Source: Dataquest (April 1998)

Chapter 3
ASIC Application Forecasts

Tables 3-1 through 3-10 show ASIC application trends.

Table 3-1
Estimated Worldwide Gate Array and Cell-Based IC Consumption by Application Market (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Data Processing	4,606	5,065	5,563	6,569	7,895	9,130	10,843
Communications	4,603	5,438	6,269	7,756	9,658	11,615	14,268
Industrial	769	841	915	1,076	1,317	1,532	1,868
Consumer	2,375	2,456	2,653	3,249	4,032	4,886	6,046
Military/Civil Aerospace	218	216	216	218	217	225	190
Transportation	359	406	456	562	763	999	1,325
Total	**12,929**	**14,423**	**16,070**	**19,431**	**23,882**	**28,388**	**34,539**

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 3-2
Estimated Worldwide Gate Array and Cell-Based IC Consumption by Application Market (Percentage of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Data Processing	35.6	35.1	34.6	33.8	33.1	32.2	31.4
Communications	35.6	37.7	39.0	39.9	40.4	40.9	41.3
Industrial	5.9	5.8	5.7	5.5	5.5	5.4	5.4
Consumer	18.4	17.0	16.5	16.7	16.9	17.2	17.5
Military/Civil Aerospace	1.7	1.5	1.3	1.1	0.9	0.8	0.5
Transportation	2.8	2.8	2.8	2.9	3.2	3.5	3.8
Total	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 3-3
Estimated North American Gate Array and Cell-Based IC Consumption by Application Market (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Data Processing	2,537	2,905	3,223	3,792	4,587	5,366	6,405
Communications	1,622	2,087	2,518	3,226	4,097	5,034	6,284
Industrial	234	269	282	328	388	443	516
Consumer	346	456	571	747	1,032	1,366	1,882
Military/Civil Aerospace	102	99	94	90	82	74	61
Transportation	29	29	27	25	31	25	30
Total	**4,870**	**5,846**	**6,714**	**8,208**	**10,216**	**12,307**	**15,178**

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 3-4
Estimated North American Gate Array and Cell-Based IC Consumption by Application Market (Percentage of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Data Processing	52.1	49.7	48.0	46.2	44.9	43.6	42.2
Communications	33.3	35.7	37.5	39.3	40.1	40.9	41.4
Industrial	4.8	4.6	4.2	4.0	3.8	3.6	3.4
Consumer	7.1	7.8	8.5	9.1	10.1	11.1	12.4
Military/Civil Aerospace	2.1	1.7	1.4	1.1	0.8	0.6	0.4
Transportation	0.6	0.5	0.4	0.3	0.3	0.2	0.2
Total	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 3-5
Estimated Japanese Gate Array and Cell-Based IC Consumption by Application Market (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Data Processing	1,124	1,151	1,185	1,339	1,535	1,693	1,947
Communications	975	1,104	1,185	1,391	1,651	1,910	2,276
Industrial	236	253	268	323	397	471	602
Consumer	1,460	1,400	1,422	1,656	1,920	2,177	2,474
Military/Civil Aerospace	83	86	89	89	92	105	82
Transportation	270	301	322	411	520	667	866
Total	**4,147**	**4,296**	**4,473**	**5,208**	**6,115**	**7,024**	**8,248**

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 3-6
Estimated Japanese Gate Array and Cell-Based IC Consumption by Application Market (Percentage of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Data Processing	27.1	26.8	26.5	25.7	25.1	24.1	23.6
Communications	23.5	25.7	26.5	26.7	27.0	27.2	27.6
Industrial	5.7	5.9	6.0	6.2	6.5	6.7	7.3
Consumer	35.2	32.6	31.8	31.8	31.4	31.0	30.0
Military/Civil Aerospace	2.0	2.0	2.0	1.7	1.5	1.5	1.0
Transportation	6.5	7.0	7.2	7.9	8.5	9.5	10.5
Total	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 3-7
Estimated European Gate Array and Cell-Based IC Consumption by Application Market (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Data Processing	170	215	263	350	437	524	645
Communications	1,826	2,044	2,306	2,765	3,373	3,964	4,788
Industrial	204	203	227	241	284	306	348
Consumer	171	208	243	346	479	642	865
Military/Civil Aerospace	31	29	30	37	41	42	43
Transportation	47	64	93	111	194	288	404
Total	**2,450**	**2,764**	**3,162**	**3,851**	**4,807**	**5,766**	**7,093**

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 3-8
Estimated European Gate Array and Cell-Based IC Consumption by Application Market (Percentage of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Data Processing	6.9	7.8	8.3	9.1	9.1	9.1	9.1
Communications	74.6	74.0	72.9	71.8	70.2	68.7	67.5
Industrial	8.3	7.3	7.2	6.3	5.9	5.3	4.9
Consumer	7.0	7.5	7.7	9.0	10.0	11.1	12.2
Military/Civil Aerospace	1.3	1.1	1.0	1.0	0.9	0.7	0.6
Transportation	1.9	2.3	2.9	2.9	4.0	5.0	5.7
Total	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 3-9
Estimated Asia/Pacific Gate Array and Cell-Based IC Consumption by Application Market (Millions of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Data Processing	775	793	892	1,089	1,336	1,547	1,846
Communications	180	203	260	374	538	708	921
Industrial	95	115	138	184	247	313	402
Consumer	398	391	417	500	601	701	824
Military/Civil Aerospace	1	2	2	2	3	3	4
Transportation	13	12	14	15	19	20	24
Total	**1,462**	**1,517**	**1,721**	**2,164**	**2,744**	**3,291**	**4,021**

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

Table 3-10
Estimated Asia/Pacific Gate Array and Cell-Based IC Consumption by Application Market (Percentage of Dollars)

	1996	1997	1998	1999	2000	2001	2002
Data Processing	53.0	52.3	51.8	50.3	48.7	47.0	45.9
Communications	12.3	13.4	15.1	17.3	19.6	21.5	22.9
Industrial	6.5	7.6	8.0	8.5	9.0	9.5	10.0
Consumer	27.2	25.8	24.2	23.1	21.9	21.3	20.5
Military/Civil Aerospace	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Transportation	0.9	0.8	0.8	0.7	0.7	0.6	0.6
Total	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**	**100.0**

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (April 1998)

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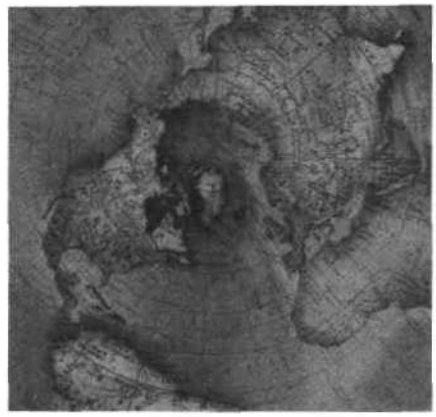

Dataquest

Final 1997 Worldwide ASIC Market Share

Market Statistics

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MARIA VALENZUELA

Program: ASIC/SLI Worldwide
Product Code: ASIC-WW-MS-9801
Publication Date: May 25, 1998
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Final 1997 Worldwide ASIC Market Share

Market Statistics

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Chapter 1
Final 1996 Worldwide ASIC Market Share

Introduction

This document contains detailed information on Dataquest's view of the application-specific integrated circuit (ASIC) market. Included in this document are the following:

- 1995-1997 ASIC market share estimates
- 1995-1997 gate array market share estimates
- 1995-1997 cell-based IC (CBIC) market share estimates
- 1995-1997 programmable logic device (PLD) market share estimates

Analyses of market share by company provide insight into high-technology markets and reinforce estimates of consumption, production, and company revenue.

ASIC market share estimates combine data from many countries, each of which has a different and fluctuating exchange rate. Estimates of non-U.S. market consumption or revenue are based on the average exchange rate for the given year. Refer to the section titled "Exchange Rates" for more information regarding these average rates. As a rule, Dataquest's estimates are calculated in local currencies and then converted to U.S. dollars.

More detailed data on this market may be requested through Dataquest's client inquiry service. Qualitative analysis of this data is provided in Market Analysis documents and in a future ASIC Market Trends report.

Definitions

Dataquest defines the ASIC market according to the segmentation scheme shown in Figure 1-1.

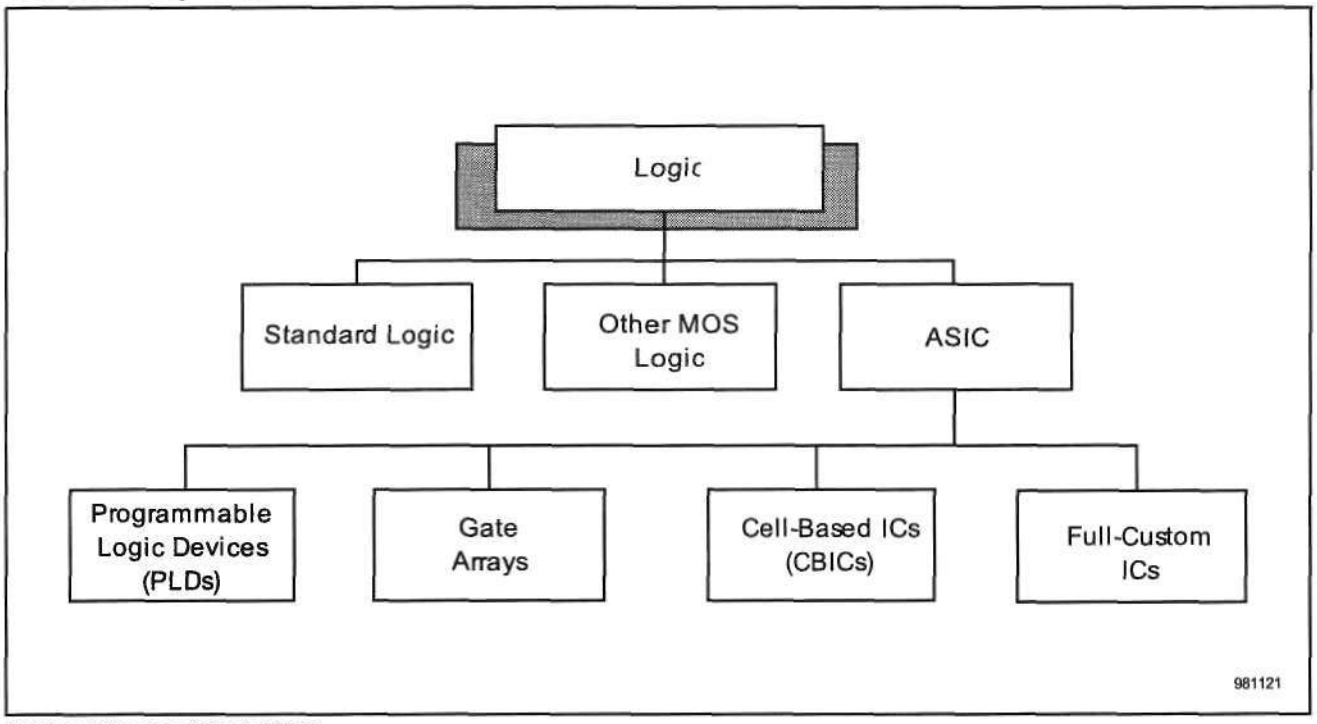
Dataquest segments logic into the two main categories: standard logic and ASIC. The ASIC family tree breaks down into PLDS, gate arrays, CBICS, and full-custom ICs. CBICs and full-custom ICs are customized by altering the full set of masks, whereas PLDs and gate arrays are customized by electrically programming the devices or by altering only the final layers of interconnect.

Product Definitions

The following are definitions used in this document.

- Application-Specific Integrated Circuits (ASICs): This term is used to describe all IC products customized for a single user. ASIC products are a combination of digital, mixed-signal, and analog products. Customized ICs purchased by more than one user become standard products and are no longer counted as ASICS.

Figure 1-1
ASIC Family Tree



Source: Dataquest (March 1998)

- Programmable Logic Devices (PLDs): PLDs are defined as ICs programmed after assembly. Memory devices such as PROMs and ROMs are not included in this market segment. PLDs are subdivided into two main categories as follows:
  - Simple Programmable Logic Devices (SPLDs): These devices have fixed or preconnected architectures capable of providing up to two levels of logic without using additional I/0 cells or pins.
  - High-Density PLDs: Included in this category are FPGAs and CPLDs.
- Gate Arrays: Gate arrays are ASICs that contain a configuration of uncommitted elements in a prefabricated base wafer. They are customized by interconnecting these elements with one or more routing layers. Included in this category are traditional gate arrays (channeled and sea-of-gates architecture) and embedded gate arrays (channeled or sea-of-gates architecture that also includes megacells such as SRAM diffused into the gate array base wafer).
- Cell-Based ICs (CBICs): CBICs are ASICs that are customized using a full set of masks and use automatic place and route tools. Included in this category are traditional standard cells (fixed-height/fixed-width cells), as well as megacells (variable-height/variable-width cells) and compiled cells.
- Full-Custom ICs: Full-custom ICs are defined as ASICs customized using a full set of masks and using manual place and route.

Revenue Classification

Because ASICs may be fabricated, assembled, and sold in several different locations, Dataquest regional device consumption is defined according to the shipping destination.

Consumption estimates include the following five sources of revenue:

- Intracompany revenue (sales to internal divisions)
- Nonrecurring engineering (NRE) revenue
- ASIC software revenue
- PLD development kit revenue
- Device production revenue

Merchant versus Captive Consumption

Dataquest includes all revenue, both merchant and captive, for semiconductor suppliers selling to the merchant market. Dataquest's revenue estimates do not include captive-only manufacturing companies represented by companies such as Digital Equipment, Northern Telecom, or Unisys that do not sell semiconductor products in the merchant market.

Regional Definitions

Americas

North America: Includes Canada, Mexico, and the United States (50 states).

South America

Central America

Japan

Japan is the only single-country region.

Europe, Africa, and the Middle East

Western Europe: Includes Austria, Belgium, Denmark, Eire (Ireland), Finland, France, Germany (including former East Germany), Greece, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, the United Kingdom, and rest of western Europe (Andorra, Cyprus, Gibraltar, Liechtenstein, Monaco, San Marino, Vatican City, Iceland, Malta, and Turkey).

Eastern Europe: Includes Albania, Bulgaria, the Czech Republic and Slovakia, Estonia, Hungary, Latvia, Lithuania, Poland, Romania, the republics of the former Yugoslavia, and the republics of the former USSR (Belarus, Russian Federation, Ukraine, Georgia, Moldova, Armenia, Azerbaijan, Kazakhstan, Uzbekistan, Tadjikistan, Kyrgyzstan, and Turkmenistan).

Asia/Pacific

Includes Hong Kong, Singapore, South Korea, Taiwan, Australia, Bangladesh, Cambodia, China, India, Indonesia, Laos, Malaysia,

Maldives, Myanmar, Nepal, New Zealand, Pakistan, the Philippines, Sri Lanka, Thailand, and Vietnam.

Line Item Definitions

Factory revenue is defined as the money value received by a semiconductor manufacturer for its products. Revenue from the sale of semiconductors sold either as finished goods, die, or wafers to another semiconductor vendor for resale is attributed to the semiconductor vendor that sells the product to a distributor or equipment manufacturer.

Market Share Methodology

Dataquest uses both primary and secondary sources to produce market statistics data. In the fourth quarter of each year, Dataquest surveys all major participants within each industry. Selected companies are resurveyed during the first quarter of the following year to verify final annual results. This primary research is supplemented with additional primary research and secondary research to verify market size, shipment totals, and pricing information. Sources of data used by Dataquest include the following:

- Information published by major industry participants
- Estimates made by knowledgeable and reliable industry spokespersons
- Government data or trade association data (such as WSTS, MITI, and U.S. DOC)
- Published product literature and price lists
- Interviews with knowledgeable manufacturers, distributors, and users
- Relevant economic data
- Information and data from online and CD-ROM data banks
- Articles in both the general and trade press
- Reports from financial analysts
- End-user surveys

Dataquest believes that the estimates presented in this document are the most accurate and meaningful statistics available. Despite the care taken in gathering, analyzing, and categorizing the data in a meaningful way, careful attention must be paid to the definitions and assumptions used herein when interpreting the estimates presented in this document. Various companies, government agencies, and trade associations may use slightly different definitions of product categories and regional groupings, or they may include different companies in their summaries. These differences should be kept in mind when making comparisons between data and numbers provided by Dataquest and those provided by other suppliers.

Notes on Market Share

In the process of conducting data collection and preparing market statistics information, Dataquest will sometimes consolidate or revise a particular company, model, series, or industry's numbers. In this section, we explain any such changes contained within this document for your reference.

Dataquest market share estimates include both digital ASIC products and mixed signal ASIC products, and linear array products.

Notes on Market Share Tables

1. Full-custom IC revenue is not included in the data presented here.

2. ASIC product revenue is based on the combined revenue from digital, mixed analog and digital, and analog products.

3. Linear array products were added to total gate array starting in 1997.

4. Total rankings include the sales of CMOS, NMOS, BiCMOS, and gallium arsenide. Bipolar revenue is not included.

5. Advanced Micro Devices (AMD) has formed a PLD division called Vantis. However, all revenue is listed under AMD.

6. Philips' 1996 PLD revenue was restated in 1997.

7. IBM's 1996 revenue was restated in 1997.

8. Microna's acquired ITT in 1997.

9. Vitesse was added in 1997.

Exchange Rates

Dataquest uses an average annual exchange rate in converting revenue to U.S. dollar amounts. Table 1-1 outlines these rates for 1995 through 1997.

Table 1-1
Exchange Rates

	1995	1996	1997
Japan (Yen/U.S.$)	93.90	108.81	121.10
France (Franc/U.S.$)	4.97	5.12	5.84
Germany (Deutsche Mark/U.S.$)	1.43	1.50	1.73
United Kingdom (U.S.$/Pound Sterling)	1.59	1.56	1.64

Source: Dataquest (April 1998)

Project Analysts: Kevin McClure and Bryan Lewis

Chapter 2
Each Company's Worldwide ASIC Revenue

Table 2-1
Each Company's 1997 Vendor Revenue from Shipments of ASICs by Product Worldwide (Millions of U.S. Dollars)

	Revenue			Market Share (%)		
	Gate Arrays	Cell-Based ICs	PLDs	Gate Arrays	Cell-Based ICs	PLDs
Total Market	**5,260**	**9,164**	**2,103**	**100.0**	**100.0**	**100.0**
Americas Companies	**1,579**	**6,114**	**2,096**	**30.0**	**66.7**	**99.7**
Actel	0	0	156	0	0	7.4
Advanced Micro Devices	0	0	243	0	0	11.6
Allegro MicroSystems	0	9	0	0	0.1	0
Altera	0	0	631	0	0	30.0
Analog Devices	0	19	0	0	0.2	0
Applied Micro Circuits Corp.	15	2	0	0.3	0	0
Atmel	46	70	33	0.9	0.8	1.6
Cherry Semiconductor	11	0	0	0.2	0	0
Chip Express	31	0	0	0.6	0	0
Cypress Semiconductor	0	0	52	0	0	2.5
Eteq Microsystems	4	0	0	0.1	0	0
Exar	8	16	0	0.2	0.2	0
Gennum	9	0	0	0.2	0	0
Gould AMI	87	107	0	1.7	1.2	0
Harris Semiconductor	1	53	0	0	0.6	0
Hewlett-Packard	0	466	0	0	5.1	0
Hughes	9	29	0	0.2	0.3	0
IBM	161	1,380	0	3.1	15.1	0
IMI	11	5	0	0.2	0.1	0
Integrated Circuit Systems	0	73	0	0	0.8	0
ISD	0	48	0	0	0.5	0
International CMOS Technology	0	0	5	0	0	0.2
Lattice	0	0	242	0	0	11.5
LSI Logic	417	765	0	7.9	8.3	0
Lucent Technologies	0	1,396	90	0	15.2	4.3
Micro Linear	8	3	0	0.2	0	0
Mitel	0	15	0	0	0.2	0
Motorola	147	147	0	2.8	1.6	0
Symbios	1	288	0	0	3.1	0
National Semiconductor	42	87	0	0.8	0.9	0

Table 2-1 (Continued)
Each Company's 1997 Vendor Revenue from Shipments of ASICs by Product Worldwide (Millions of U.S. Dollars)

	Revenue			Market Share (%)		
	Gate Arrays	Cell-Based ICs	PLDs	Gate Arrays	Cell-Based ICs	PLDs
QuickLogic	0	0	29	0	0	1.4
Raytheon	20	8	0	0.4	0.1	0
Rockwell	0	5	0	0	0.1	0
PMC Sierra Semiconductor	0	28	0	0	0.3	0
Texas Instruments	403	480	3	7.7	5.2	0.1
Vitesse	53	0	0	1.0	0	0
VLSI Technology	72	595	0	1.4	6.5	0
Xilinx	0	0	612	0	0	29.1
Other Americas Companies	23	20	0	0.4	0.2	0
Japanese Companies	**3,257**	**2,048**	**3**	**61.9**	**22.3**	**0.1**
Fujitsu	809	439	0	15.4	4.8	0
Hitachi	353	168	0	6.7	1.8	0
Matsushita	124	134	0	2.4	1.5	0
Mitsubishi	254	42	0	4.8	0.5	0
NEC	975	888	0	18.5	9.7	0
Oki	65	20	0	1.2	0.2	0
Ricoh	4	0	1	0.1	0	0
Rohm	22	18	0	0.4	0.2	0
SANYO	43	22	0	0.8	0.2	0
Seiko Epson	98	17	0	1.9	0.2	0
Sharp	66	45	0	1.3	0.5	0
Sony	33	0	0	0.6	0	0
Toshiba	408	250	2	7.8	2.7	0.1
Yamaha	3	5	0	0.1	0.1	0
European Companies	**219**	**936**	**4**	**4.2**	**10.2**	**0.2**
Austria Mikro Systeme	7	109	0	0.1	1.2	0
Melexis	0	9	0	0	0.1	0
Elmos	0	9	0	0	0.1	0
EM Microelectronics Marin	0	25	0	0	0.3	0
Ericsson	0	30	0	0	0.3	0
GEC Plessey	106	80	0	2.0	0.9	0
Micronas	0	35	0	0	0.4	0
Alcatel Microelectronics	0	204	0	0	2.2	0
Philips	0	21	4	0	0.2	0.2
SGS-Thomson	82	305	0	1.6	3.3	0
Siemens	0	23	0	0	0.3	0
TEMIC	17	51	0	0.3	0.6	0

Table 2-1 (Continued)
Each Company's 1997 Vendor Revenue from Shipments of ASICs by Product Worldwide (Millions of U.S. Dollars)

	Revenue			Market Share (%)		
	Gate Arrays	Cell-Based ICs	PLDs	Gate Arrays	Cell-Based ICs	PLDs
TCS	5	35	0	0.1	0.4	0
Zetex	2	0	0	0	0	0
Asia/Pacific Companies	**205**	**66**	**0**	**3.9**	**0.7**	**0**
Daewoo	3	0	0	0.1	0	0
LG Semicon	68	31	0	1.3	0.3	0
Hualon Microelectronics Corp.	0	1	0	0	0	0
Holtek	3	0	0	0.1	0	0
Hyundai	3	1	0	0.1	0	0
Macronix	33	3	0	0.6	0	0
Samsung	95	30	0	1.8	0.3	0

Source: Dataquest (April 1998)

Table 2-2
Each Company's Vendor Revenue from Shipments of Total ASICs Worldwide (Millions of U.S. Dollars)

	Revenue			Market Share (%)		
	1995	1996	1997	1995	1996	1997
Total Market	**13,425**	**14,801**	**16,527**	**100.0**	**100.0**	**100.0**
Americas Companies	**7,087**	**8,213**	**9,789**	**52.8**	**55.5**	**59.2**
Actel	109	149	156	0.8	1.0	0.9
Advanced Micro Devices	271	243	243	2.0	1.6	1.5
Allegro MicroSystems	0	7	9	0	0	0
Altera	402	497	631	3.0	3.4	3.8
Analog Devices	17	14	19	0.1	0	0.1
Applied Micro Circuits Corp.	20	20	17	0.1	0.1	0.1
Atmel	47	157	149	0.4	1.1	0.9
Cherry Semiconductor	0	0	11	0	0	0
Chip Express	0	25	31	0	0.2	0.2
Cypress Semiconductor	56	60	52	0.4	0.4	0.3
Eteq Microsystems	7	4	4	0	0	0
Exar	0	15	24	0	0.1	0.1
Gennum	0	0	9	0	0	0
Gould AMI	109	95	194	0.8	0.6	1.2
Harris Semiconductor	50	54	54	0.4	0.4	0.3
Hewlett-Packard	342	380	466	2.5	2.6	2.8
Hughes	13	33	38	0	0.2	0.2
IBM	719	1,003	1,541	5.4	6.8	9.3
IMI	30	39	16	0.2	0.3	0
IMP	9	5	0	0	0	0
Integrated Circuit Systems	45	57	73	0.3	0.4	0.4
International CMOS Technology	16	12	5	0.1	0	0
ISD	0	0	48	0	0	0.3
Lattice	186	200	242	1.4	1.4	1.5
LSI Logic	1,162	1,136	1,182	8.7	7.7	7.2
Lucent Technologies	772	1,060	1,486	5.8	7.2	9
Micro Linear	4	3	11	0	0	0
Mitel	0	24	15	0	0.2	0
Motorola	302	325	294	2.2	2.2	1.8
National Semiconductor	93	117	129	0.7	0.8	0.8
PMC Sierra Semiconductor	12	25	28	0	0.2	0.2
QuickLogic	16	25	29	0.1	0.2	0.2
Raytheon	6	7	28	0	0	0.2
Rockwell	4	4	5	0	0	0
Symbios	317	356	289	2.4	2.4	1.7

Table 2-2 (Continued)
Each Company's Vendor Revenue from Shipments of Total ASICs Worldwide (Millions of U.S. Dollars)

	Revenue			Market Share (%)		
	1995	1996	1997	1995	1996	1997
Texas Instruments	787	841	886	5.9	5.7	5.4
Vitesse	0	0	53	0	0	0.3
VLSI Technology	479	615	667	3.6	4.2	4.0
Xilinx	520	566	612	3.9	3.8	3.7
Other Americas Companies	150	40	43	1.1	0.3	0.3
Japanese Companies	**5,061**	**5,242**	**5,308**	**37.7**	**35.4**	**32.1**
Fujitsu	1,157	1,120	1,248	8.6	7.6	7.6
Hitachi	445	577	521	3.3	3.9	3.2
Matsushita	275	252	258	2.0	1.7	1.6
Mitsubishi	297	256	296	2.2	1.7	1.8
NEC	1,308	1,689	1,863	9.7	11.4	11.3
Oki	159	137	85	1.2	0.9	0.5
Ricoh	79	32	5	0.6	0.2	0
Rohm	56	48	40	0.4	0.3	0.2
SANYO	57	56	65	0.4	0.4	0.4
Seiko Epson	129	104	115	1.0	0.7	0.7
Sharp	118	103	111	0.9	0.7	0.7
Sony	43	23	33	0.3	0.2	0.2
Toshiba	923	836	660	6.9	5.6	4.0
Yamaha	15	9	8	0.1	0	0
European Companies	**1,056**	**1,092**	**1,159**	**7.9**	**7.4**	**7.0**
Alcatel Microelectronics	182	179	204	1.4	1.2	1.2
Austria Mikro Systeme	132	124	116	1.0	0.8	0.7
Elmos	7	7	9	0	0	0
EM Microelectronics Marin	0	25	25	0	0.2	0.2
Ericsson	19	19	30	0.1	0.1	0.2
GEC Plessey	199	186	186	1.5	1.3	1.1
Melexis	0	9	9	0	0	0
Micronas	37	33	35	0.3	0.2	0.2
Philips	5	3	25	0	0	0.2
SGS-Thomson	278	392	387	2.1	2.6	2.3
Siemens	29	31	23	0.2	0.2	0.1
TCS	13	28	40	0	0.2	0.2
TEMIC	55	56	68	0.4	0.4	0.4
Zetex	0	0	2	0	0	0

Table 2-2 (Continued)
Each Company's Vendor Revenue from Shipments of Total ASICs Worldwide (Millions of U.S. Dollars)

	Revenue			Market Share (%)		
	1995	1996	1997	1995	1996	1997
Asia/Pacific Companies	**221**	**254**	**271**	**1.6**	**1.7**	**1.6**
Acer	3	0	0	0	0	0
Daewoo	4	3	3	0	0	0
Holtek	6	4	3	0	0	0
Hualon Microelectronics Corp.	0	1	1	0	0	0
Hyundai	13	9	4	0	0	0
LG Semicon	90	89	99	0.7	0.6	0.6
Macronix	0	36	36	0	0.2	0.2
Samsung	105	112	125	0.8	0.8	0.8

Source: Dataquest (April 1998)

Table 2-3
Each Company's Vendor Revenue from Shipments of Total Cell-Based ICs Worldwide (Millions of U.S. Dollars)

	Revenue			Market Share (%)		
	1995	1996	1997	1995	1996	1997
Total Market	**5,747**	**7,317**	**9,164**	**100.0**	**100.0**	**100.0**
Americas Companies	**3,457**	**4,502**	**6,114**	**60.2**	**61.5**	**66.7**
Allegro MicroSystems	0	7	9	0	0	0
Analog Devices	17	14	19	0.3	0.2	0.2
Applied Micro Circuits Corp.	0	2	2	0	0	0
Atmel	9	87	70	0.2	1.2	0.8
Exar	0	15	16	0	0.2	0.2
Gould AMI	55	28	107	1.0	0.4	1.2
Harris Semiconductor	50	51	53	0.9	0.7	0.6
Hewlett-Packard	342	380	466	6.0	5.2	5.1
Hughes	4	23	29	0	0.3	0.3
IBM	417	733	1,380	7.3	10.0	15.1
IMI	0	5	5	0	0	0
IMP	9	5	0	0.2	0	0
Integrated Circuit Systems	45	57	73	0.8	0.8	0.8
ISD	0	0	48	0	0	0.5
LSI Logic	485	556	765	8.4	7.6	8.3
Lucent Technologies	650	965	1,396	11.3	13.2	15.2
Micro Linear	0	3	3	0	0	0
Mitel	0	24	15	0	0.3	0.2
Motorola	95	116	147	1.7	1.6	1.6
National Semiconductor	50	80	87	0.9	1.1	0.9
PMC Sierra Semiconductor	12	25	28	0.2	0.3	0.3
Raytheon	6	7	8	0.1	0	0
Rockwell	4	4	5	0	0	0
Symbios	290	345	288	5.0	4.7	3.1
Texas Instruments	410	406	480	7.1	5.5	5.2
VLSI Technology	385	549	595	6.7	7.5	6.5
Other Americas Companies	115	15	20	2.0	0.2	0.2
Japanese Companies	**1,445**	**1,918**	**2,048**	**25.1**	**26.2**	**22.3**
Fujitsu	318	346	439	5.5	4.7	4.8
Hitachi	99	189	168	1.7	2.6	1.8
Matsushita	162	154	134	2.8	2.1	1.5
Mitsubishi	34	33	42	0.6	0.5	0.5
NEC	345	741	888	6.0	10.1	9.7
Oki	76	68	20	1.3	0.9	0.2
Ricoh	47	17	0	0.8	0.2	0
Rohm	21	18	18	0.4	0.2	0.2

Table 2-3 (Continued)
Each Company's Vendor Revenue from Shipments of Total Cell-Based ICs Worldwide (Millions of U.S. Dollars)

	Revenue			Market Share (%)		
	1995	1996	1997	1995	1996	1997
SANYO	27	29	22	0.5	0.4	0.2
Seiko Epson	16	14	17	0.3	0.2	0.2
Sharp	42	38	45	0.7	0.5	0.5
Toshiba	246	266	250	4.3	3.6	2.7
Yamaha	12	5	5	0.2	0	0
European Companies	**808**	**851**	**936**	**14.1**	**11.6**	**10.2**
Alcatel Microelectronics	182	179	204	3.2	2.4	2.2
Austria Mikro Systeme	129	116	109	2.2	1.6	1.2
Elmos	7	7	9	0.1	0	0
EM Microelectronics Marin	0	25	25	0	0.3	0.3
Ericsson	19	19	30	0.3	0.3	0.3
GEC Plessey	78	78	80	1.4	1.1	0.9
Melexis	0	9	9	0	0.1	0
Micronas	37	33	35	0.6	0.5	0.4
Philips	0	0	21	0	0	0.2
SGS-Thomson	189	305	305	3.3	4.2	3.3
Siemens	29	31	23	0.5	0.4	0.3
TCS	12	27	35	0.2	0.4	0.4
TEMIC	26	22	51	0.5	0.3	0.6
Asia/Pacific Companies	**37**	**46**	**66**	**0.6**	**0.6**	**0.7**
Daewoo	1	0	0	0	0	0
Hualon Microelectronics Corp.	0	1	1	0	0	0
Hyundai	0	0	1	0	0	0
LG Semicon	18	22	31	0.3	0.3	0.3
Macronix	0	3	3	0	0	0
Samsung	18	20	30	0.3	0.3	0.3

Source: Dataquest (April 1998)

Table 2-4
Each Company's Vendor Revenue from Shipments of Total Gate Arrays Worldwide (Millions of U.S. Dollars)

	Revenue			Market Share (%)		
	1995	1996	1997	1995	1996	1997
Total Market	**5,977**	**5,612**	**5,260**	**100.0**	**100.0**	**100.0**
Americas Companies	**1,940**	**1,845**	**1,579**	**32.5**	**32.9**	**30.0**
Applied Micro Circuits Corp.	20	18	15	0.3	0.3	0.3
Atmel	21	36	46	0.4	0.6	0.9
Cherry Semiconductor	0	0	11	0	0	0.2
Chip Express	0	25	31	0	0.4	0.6
Eteq Microsystems	7	4	4	0.1	0	0
Exar	0	0	8	0	0	0.2
Gennum	0	0	9	0	0	0.2
Gould AMI	50	67	87	0.8	1.2	1.7
Harris Semiconductor	1	3	1	0	0	0
Hughes	9	10	9	0.2	0.2	0.2
IBM	302	270	161	5.1	4.8	3.1
IMI	30	34	11	0.5	0.6	0.2
LSI Logic	677	580	417	11.3	10.3	7.9
Lucent Technologies	50	20	0	0.8	0.4	0
Micro Linear	3	0	8	0	0	0.2
Motorola	207	209	147	3.5	3.7	2.8
National Semiconductor	41	37	42	0.7	0.7	0.8
Raytheon	0	0	20	0	0	0.4
Symbios	27	11	1	0.5	0.2	0
Texas Instruments	361	430	403	6.0	7.7	7.7
Vitesse	0	0	53	0	0	1.0
VLSI Technology	94	66	72	1.6	1.2	1.4
Other Americas Companies	32	25	23	0.5	0.4	0.4
Japanese Companies	**3,613**	**3,321**	**3,257**	**60.4**	**59.2**	**61.9**
Fujitsu	839	774	809	14.0	13.8	15.4
Hitachi	346	388	353	5.8	6.9	6.7
Matsushita	113	98	124	1.9	1.7	2.4
Mitsubishi	263	223	254	4.4	4.0	4.8
NEC	963	948	975	16.1	16.9	18.5
Oki	83	69	65	1.4	1.2	1.2
Ricoh	31	14	4	0.5	0.2	0
Rohm	35	30	22	0.6	0.5	0.4
SANYO	30	27	43	0.5	0.5	0.8
Seiko Epson	113	90	98	1.9	1.6	1.9
Sharp	76	65	66	1.3	1.2	1.3
Sony	43	23	33	0.7	0.4	0.6

Table 2-4 (Continued)
Each Company's Vendor Revenue from Shipments of Total Gate Arrays Worldwide (Millions of U.S. Dollars)

	Revenue			Market Share (%)		
	1995	1996	1997	1995	1996	1997
Toshiba	675	568	408	11.3	10.1	7.8
Yamaha	3	4	3	0	0	0
European Companies	**243**	**238**	**219**	**4.1**	**4.2**	**4.2**
Austria Mikro Systeme	3	8	7	0	0.1	0.1
GEC Plessey	121	108	106	2.0	1.9	2.0
SGS-Thomson	89	87	82	1.5	1.6	1.6
TCS	1	1	5	0	0	0
TEMIC	29	34	17	0.5	0.6	0.3
Zetex	0	0	2	0	0	0
Asia/Pacific Companies	**181**	**208**	**205**	**3.0**	**3.7**	**3.9**
Daewoo	3	3	3	0	0	0
Holtek	6	4	3	0.1	0	0
Hyundai	13	9	3	0.2	0.2	0
LG Semicon	72	67	68	1.2	1.2	1.3
Macronix	0	33	33	0	0.6	0.6
Samsung	87	92	95	1.5	1.6	1.8

Source: Dataquest (April 1998)

Table 2-5
Each Company's Vendor Revenue from Shipments of PLDs Worldwide (Millions of U.S. Dollars)

	Revenue			Market Share (%)		
	1995	1996	1997	1995	1996	1997
Total Market	**1,698**	**1,872**	**2,103**	**100.0**	**100.0**	**100.0**
Americas Companies	**1,687**	**1,866**	**2,096**	**99.4**	**99.7**	**99.7**
Actel	109	149	156	6.4	8.0	7.4
Advanced Micro Devices	271	243	243	16.0	13.0	11.6
Altera	402	497	631	23.7	26.5	30.0
Atmel	17	34	33	1.0	1.8	1.6
Cypress Semiconductor	56	60	52	3.3	3.2	2.5
Gould AMI	4	0	0	0.2	0	0
International CMOS Technology	16	12	5	0.9	0.6	0.2
Lattice	186	200	242	11.0	10.7	11.5
Lucent Technologies	72	75	90	4.2	4.0	4.3
National Semiconductor	2	0	0	0.1	0	0
QuickLogic	16	25	29	0.9	1.3	1.4
Texas Instruments	16	5	3	0.9	0.3	0.1
Xilinx	520	566	612	30.6	30.2	29.1
Japanese Companies	**3**	**3**	**3**	**0.2**	**0.2**	**0.1**
Ricoh	1	1	1	0	0	0
Toshiba	2	2	2	0.1	0.1	0
European Companies	**5**	**3**	**4**	**0.3**	**0.2**	**0.2**
Philips	5	3	4	0.3	0.2	0.2
Asia/Pacific Companies	**3**	**0**	**0**	**0.2**	**0**	**0**
Acer	3	0	0	0.2	0	0

Source: Dataquest (April 1998)

Chapter 3
Top Companies' Worldwide ASIC Revenue

Table 3-1
Top 74 Worldwide Companies' Vendor Revenue from Shipments of Total ASICs Worldwide (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	NEC	1,689	1,863	10.3	11.3
5	2	IBM	1,003	1,541	53.6	9.3
4	3	Lucent Technologies	1,060	1,486	40.2	9.0
3	4	Fujitsu	1,120	1,248	11.4	7.6
2	5	LSI Logic	1,136	1,182	4.0	7.2
6	6	Texas Instruments	841	886	5.4	5.4
8	7	VLSI Technology	615	667	8.5	4.0
7	8	Toshiba	836	660	-21.1	4.0
11	9	Altera	497	631	27.0	3.8
10	10	Xilinx	566	612	8.1	3.7
9	11	Hitachi	577	521	-9.7	3.2
13	12	Hewlett-Packard	380	466	22.6	2.8
12	13	SGS-Thomson	392	387	-1.3	2.3
16	14	Mitsubishi	256	296	15.6	1.8
15	15	Motorola	325	294	-9.5	1.8
14	16	Symbios	356	289	-18.8	1.7
17	17	Matsushita	252	258	2.4	1.6
18	18	Advanced Micro Devices	243	243	0	1.5
19	19	Lattice	200	242	21.0	1.5
21	20	Alcatel Microelectronics	179	204	14.0	1.2
30	21	Gould AMI	95	194	104.2	1.2
20	22	GEC Plessey	186	186	0	1.1
23	23	Actel	149	156	4.7	0.9
22	24	Atmel	157	149	-5.1	0.9
26	25	National Semiconductor	117	129	10.3	0.8
27	26	Samsung	112	125	11.6	0.8
25	27	Austria Mikro Systeme	124	116	-6.5	0.7
28	28	Seiko Epson	104	115	10.6	0.7
29	29	Sharp	103	111	7.8	0.7
31	30	LG Semicon	89	99	11.2	0.6
24	31	Oki	137	85	-38.0	0.5
33	32	Integrated Circuit Systems	57	73	28.1	0.4

Table 3-1 (Continued)
Top 74 Worldwide Companies' Vendor Revenue from Shipments of Total ASICs Worldwide (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
35	33	TEMIC	56	68	21.4	0.4
34	34	SANYO	56	65	16.1	0.4
36	35	Harris Semiconductor	54	54	0	0.3
NA	36	Vitesse	0	53	NA	0.3
32	37	Cypress Semiconductor	60	52	-13.3	0.3
NA	38	ISD	0	48	NA	0.3
37	39	Rohm	48	40	-16.7	0.2
44	40	TCS	28	40	42.9	0.2
40	41	Hughes	33	38	15.2	0.2
39	42	Macronix	36	36	0	0.2
41	43	Micronas	33	35	6.1	0.2
50	44	Sony	23	33	43.5	0.2
45	45	Chip Express	25	31	24.0	0.2
52	46	Ericsson	19	30	57.9	0.2
46	47	QuickLogic	25	29	16.0	0.2
47	48	PMC Sierra Semiconductor	25	28	12.0	0.2
60	49	Raytheon	7	28	300.0	0.2
48	50	EM Microelectronics Marin	25	25	0	0.2
67	51	Philips	3	25	733.3	0.2
53	52	Exar	15	24	60.0	0.1
43	53	Siemens	31	23	-25.8	0.1
54	54	Analog Devices	14	19	35.7	0.1
51	55	Applied Micro Circuits Corp.	20	17	-15.0	0.1
38	56	IMI	39	16	-59.0	0
49	57	Mitel	24	15	-37.5	0
66	58	Micro Linear	3	11	266.7	0
NA	59	Cherry Semiconductor	0	11	NA	0
57	60	Melexis	9	9	0	0
59	61	Allegro MicroSystems	7	9	28.6	0
61	62	Elmos	7	9	28.6	0
NA	63	Gennum	0	9	NA	0
56	64	Yamaha	9	8	-11.1	0
42	65	Ricoh	32	5	-84.4	0
55	66	International CMOS Technology	12	5	-58.3	0
64	67	Rockwell	4	5	25.0	0
58	68	Hyundai	9	4	-55.6	0
63	69	Eteq Microsystems	4	4	0	0

Table 3-1 (Continued)
Top 74 Worldwide Companies' Vendor Revenue from Shipments of Total ASICs Worldwide (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
65	70	Holtek	4	3	-25.0	0
68	71	Daewoo	3	3	0	0
NA	72	Zetex	0	2	NA	0
69	73	Hualon Microelectronics Corp.	1	1	0	0
62	74	IMP	5	0	-100.0	0
		All Others	40	43	7.5	0.3
		Americas Companies	8,213	9,789	19.2	59.2
		Japanese Companies	5,242	5,308	1.3	32.1
		European Companies	1,092	1,159	6.1	7
		Asia/Pacific Companies	254	271	6.7	1.6
		Total Market	**14,801**	**16,527**	**11.7**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Table 3-2
Top 57 Worldwide Companies' Vendor Revenue from Shipments of Total Cell-Based ICs Worldwide (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	Lucent Technologies	965	1,396	44.7	15.2
3	2	IBM	733	1,380	88.3	15.1
2	3	NEC	741	888	19.8	9.7
4	4	LSI Logic	556	765	37.6	8.3
5	5	VLSI Technology	549	595	8.4	6.5
6	6	Texas Instruments	406	480	18.2	5.2
7	7	Hewlett-Packard	380	466	22.6	5.1
8	8	Fujitsu	346	439	26.9	4.8
10	9	SGS-Thomson	305	305	0	3.3
9	10	Symbios	345	288	-16.5	3.1
11	11	Toshiba	266	250	-6.0	2.7
13	12	Alcatel Microelectronics	179	204	14.0	2.2
12	13	Hitachi	189	168	-11.1	1.8
15	14	Motorola	116	147	26.7	1.6
14	15	Matsushita	154	134	-13.0	1.5
16	16	Austria Mikro Systeme	116	109	-6.0	1.2
28	17	Gould AMI	28	107	282.1	1.2
18	18	National Semiconductor	80	87	8.7	0.9
19	19	GEC Plessey	78	80	2.6	0.9
21	20	Integrated Circuit Systems	57	73	28.1	0.8
17	21	Atmel	87	70	-19.5	0.8
22	22	Harris Semiconductor	51	53	3.9	0.6
35	23	TEMIC	22	51	131.8	0.6
NA	24	ISD	0	48	NA	0.5
23	25	Sharp	38	45	18.4	0.5
24	26	Mitsubishi	33	42	27.3	0.5
25	27	Micronas	33	35	6.1	0.4
29	28	TCS	27	35	29.6	0.4
34	29	LG Semicon	22	31	40.9	0.3
36	30	Samsung	20	30	50.0	0.3
37	31	Ericsson	19	30	57.9	0.3
33	32	Hughes	23	29	26.1	0.3
30	33	PMC Sierra Semiconductor	25	28	12.0	0.3
31	34	EM Microelectronics Marin	25	25	0	0.3
26	35	Siemens	31	23	-25.8	0.3
27	36	SANYO	29	22	-24.1	0.2
NA	37	Philips	0	21	NA	0.2

Table 3-2 (Continued)
Top 57 Worldwide Companies' Vendor Revenue from Shipments of Total Cell-Based ICs Worldwide (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
20	38	Oki	68	20	-70.6	0.2
42	39	Analog Devices	14	19	35.7	0.2
38	40	Rohm	18	18	0	0.2
41	41	Seiko Epson	14	17	21.4	0.2
40	42	Exar	15	16	6.7	0.2
32	43	Mitel	24	15	-37.5	0.2
43	44	Melexis	9	9	0	0
44	45	Allegro MicroSystems	7	9	28.6	0
45	46	Elmos	7	9	28.6	0
46	47	Raytheon	7	8	14.3	0
47	48	IMI	5	5	0	0
48	49	Yamaha	5	5	0	0
50	50	Rockwell	4	5	25.0	0
51	51	Macronix	3	3	0	0
52	52	Micro Linear	3	3	0	0
53	53	Applied Micro Circuits Corp.	2	2	0	0
54	54	Hualon Microelectronics Corp.	1	1	0	0
NA	55	Hyundai	0	1	NA	0
39	56	Ricoh	17	0	-100.0	0
49	57	IMP	5	0	-100.0	0
		All Others	15	20	33.3	0.2
		Americas Companies	4,502	6,114	35.8	66.7
		Japanese Companies	1,918	2,048	6.8	22.3
		European Companies	851	936	10.0	10.2
		Asia/Pacific Companies	46	66	43.5	0.7
		Total Market	**7,317**	**9,164**	**25.2**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Table 3-3
Top 48 Worldwide Companies' Vendor Revenue from Shipments of Total Gate Arrays Worldwide (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	NEC	948	975	2.8	18.5
2	2	Fujitsu	774	809	4.5	15.4
3	3	LSI Logic	580	417	-28.1	7.9
4	4	Toshiba	568	408	-28.2	7.8
5	5	Texas Instruments	430	403	-6.3	7.7
6	6	Hitachi	388	353	-9.0	6.7
8	7	Mitsubishi	223	254	13.9	4.8
7	8	IBM	270	161	-40.4	3.1
9	9	Motorola	209	147	-29.7	2.8
11	10	Matsushita	98	124	26.5	2.4
10	11	GEC Plessey	108	106	-1.9	2.0
13	12	Seiko Epson	90	98	8.9	1.9
12	13	Samsung	92	95	3.3	1.8
16	14	Gould AMI	67	87	29.9	1.7
14	15	SGS-Thomson	87	82	-5.7	1.6
18	16	VLSI Technology	66	72	9.1	1.4
17	17	LG Semicon	67	68	1.5	1.3
19	18	Sharp	65	66	1.5	1.3
15	19	Oki	69	65	-5.8	1.2
NA	20	Vitesse	0	53	NA	1.0
21	21	Atmel	36	46	27.8	0.9
26	22	SANYO	27	43	59.3	0.8
20	23	National Semiconductor	37	42	13.5	0.8
24	24	Macronix	33	33	0	0.6
28	25	Sony	23	33	43.5	0.6
27	26	Chip Express	25	31	24.0	0.6
25	27	Rohm	30	22	-26.7	0.4
NA	28	Raytheon	0	20	NA	0.4
22	29	TEMIC	34	17	-50.0	0.3
30	30	Applied Micro Circuits Corp.	18	15	-16.7	0.3
23	31	IMI	34	11	-67.6	0.2
NA	32	Cherry Semiconductor	0	11	NA	0.2
33	33	Hughes	10	9	-10.0	0.2
NA	34	Gennum	0	9	NA	0.2
NA	35	Exar	0	8	NA	0.2
NA	36	Micro Linear	0	8	NA	0.2
35	37	Austria Mikro Systeme	8	7	-12.5	0.1

Table 3-3 (Continued)
Top 48 Worldwide Companies' Vendor Revenue from Shipments of Total Gate Arrays Worldwide (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
41	38	TCS	1	5	400.0	0
31	39	Ricoh	14	4	-71.4	0
37	40	Eteq Microsystems	4	4	0	0
34	41	Hyundai	9	3	-66.7	0
36	42	Yamaha	4	3	-25.0	0
38	43	Holtek	4	3	-25.0	0
40	44	Daewoo	3	3	0	0
NA	45	Zetex	0	2	NA	0
32	46	Symbios	11	1	-90.9	0
39	47	Harris Semiconductor	3	1	-66.7	0
29	48	Lucent Technologies	20	0	-100.0	0
		All Others	25	23	-8.0	0.4
		Americas Companies	1,845	1,579	-14.4	30.0
		Japanese Companies	3,321	3,257	-1.9	61.9
		European Companies	238	219	-8.0	4.2
		Asia/Pacific Companies	208	205	-1.4	3.9
		Total Market	**5,612**	**5,260**	**-6.3**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Table 3-4
Top 14 Worldwide Companies' Vendor Revenue from Shipments of PLDs Worldwide (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
2	1	Altera	497	631	27.0	30.0
1	2	Xilinx	566	612	8.1	29.1
3	3	Advanced Micro Devices	243	243	0	11.6
4	4	Lattice	200	242	21.0	11.5
5	5	Actel	149	156	4.7	7.4
6	6	Lucent Technologies	75	90	20.0	4.3
7	7	Cypress Semiconductor	60	52	-13.3	2.5
8	8	Atmel	34	33	-2.9	1.6
9	9	QuickLogic	25	29	16.0	1.4
10	10	International CMOS Technology	12	5	-58.3	0.2
12	11	Philips	3	4	33.3	0.2
11	12	Texas Instruments	5	3	-40.0	0.1
13	13	Toshiba	2	2	0	0
14	14	Ricoh	1	1	0	0
		All Others	-	-	NA	0
		Americas Companies	1,866	2,096	12.3	99.7
		Japanese Companies	3	3	0	0.1
		European Companies	3	4	33.3	0.2
		Asia/Pacific Companies	0	0	NA	0
		Total Market	**1,872**	**2,103**	**12.3**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Chapter 4
Top Companies' Americas ASIC Revenue

Table 4-1
Top 66 Worldwide Companies' Vendor Revenue from Shipments of Total ASICs to Americas (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	IBM	789	1,382	75.2	19.5
3	2	Lucent Technologies	485	745	53.6	10.5
2	3	LSI Logic	670	569	-15.1	8.0
4	4	NEC	378	408	7.9	5.7
5	5	Xilinx	363	386	6.3	5.4
9	6	Altera	265	353	33.2	5.0
6	7	VLSI Technology	314	345	9.9	4.9
10	8	Hewlett-Packard	247	301	21.9	4.2
7	9	Toshiba	289	253	-12.5	3.6
8	10	Symbios	285	229	-19.6	3.2
11	11	Texas Instruments	213	202	-5.2	2.8
18	12	Gould AMI	88	181	105.7	2.6
13	13	Mitsubishi	139	155	11.5	2.2
12	14	Motorola	184	141	-23.4	2.0
14	15	Advanced Micro Devices	134	136	1.5	1.9
16	16	Lattice	112	127	13.4	1.8
17	17	Actel	100	111	11.0	1.6
15	18	SGS-Thomson	116	106	-8.6	1.5
20	19	Fujitsu	69	98	42.0	1.4
19	20	Atmel	73	72	-1.4	1.0
23	21	National Semiconductor	47	64	36.2	0.9
25	22	GEC Plessey	40	59	47.5	0.8
21	23	Hitachi	66	55	-16.7	0.8
24	24	Samsung	41	42	2.4	0.6
42	25	Matsushita	9	40	344.4	0.6
29	26	Harris Semiconductor	26	39	50.0	0.5
26	27	Cypress Semiconductor	35	37	5.7	0.5
28	28	Hughes	31	36	16.1	0.5
27	29	Seiko Epson	35	35	0	0.5
22	30	Oki	48	28	-41.7	0.4
NA	31	Vitesse	0	28	NA	0.4
30	32	Chip Express	22	25	13.6	0.4
33	33	Integrated Circuit Systems	18	23	27.8	0.3
47	34	Raytheon	5	22	340.0	0.3
35	35	PMC Sierra Semiconductor	17	19	11.8	0.3

Table 4-1 (Continued)
Top 66 Worldwide Companies' Vendor Revenue from Shipments of Total ASICs to Americas (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
37	36	LG Semicon	15	19	26.7	0.3
60	37	Philips	1	18	1,700.0	0.3
32	38	Applied Micro Circuits Corp.	18	15	-16.7	0.2
40	39	Exar	9	15	66.7	0.2
34	40	QuickLogic	18	13	-27.8	0.2
NA	41	Cherry Semiconductor	0	11	NA	0.2
39	42	Austria Mikro Systeme	12	10	-16.7	0.1
45	43	Analog Devices	5	10	100.0	0.1
NA	44	ISD	0	10	NA	0.1
43	45	Micronas	8	9	12.5	0.1
31	46	IMI	20	8	-60.0	0.1
56	47	Micro Linear	2	8	300.0	0.1
48	48	Rohm	5	7	40.0	0
44	49	Allegro MicroSystems	5	6	20.0	0
53	50	TEMIC	3	6	100.0	0
41	51	International CMOS Technology	9	5	-44.4	0
51	52	Rockwell	4	5	25.0	0
52	53	Alcatel Microelectronics	4	5	25.0	0
NA	54	Gennum	0	5	NA	0
38	55	SANYO	14	3	-78.6	0
49	56	Sony	5	3	-40.0	0
50	57	Mitel	4	3	-25.0	0
59	58	Melexis	1	3	200.0	0
55	59	Eteq Microsystems	2	2	0	0
NA	60	EM Microelectronics Marin	0	2	NA	0
54	61	Hyundai	3	1	-66.7	0
58	62	Yamaha	2	1	-50.0	0
36	63	Macronix	16	0	-100.0	0
46	64	IMP	5	0	-100.0	0
57	65	Ricoh	2	0	-100.0	0
61	66	Holtek	1	0	-100.0	0
		All Others	40	43	7.5	0.6
		Americas Companies	4,664	5,732	22.9	80.8
		Japanese Companies	1,061	1,086	2.4	15.3
		European Companies	185	218	17.8	3.1
		Asia/Pacific Companies	76	62	-18.4	0.9
		Total Market	**5,986**	**7,098**	**18.6**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Table 4-2
Top 48 Worldwide Companies' Vendor Revenue from Shipments of Total Cell-Based ICs to Americas (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	IBM	581	1,249	115.0	30.5
2	2	Lucent Technologies	415	685	65.1	16.7
5	3	LSI Logic	250	337	34.8	8.2
6	4	Hewlett-Packard	247	301	21.9	7.3
4	5	VLSI Technology	264	287	8.7	7.0
3	6	Symbios	274	228	-16.8	5.6
7	7	NEC	159	196	23.3	4.8
14	8	Gould AMI	28	103	267.9	2.5
10	9	Toshiba	47	92	95.7	2.2
8	10	SGS-Thomson	69	69	0	1.7
9	11	Motorola	60	59	-1.7	1.4
12	12	National Semiconductor	31	46	48.4	1.1
13	13	Texas Instruments	29	40	37.9	1.0
21	14	Fujitsu	17	40	135.3	1.0
15	15	Harris Semiconductor	24	38	58.3	0.9
11	16	Hitachi	41	36	-12.2	0.9
17	17	GEC Plessey	21	30	42.9	0.7
18	18	Hughes	21	27	28.6	0.7
20	19	Integrated Circuit Systems	18	23	27.8	0.6
22	20	PMC Sierra Semiconductor	17	19	11.8	0.5
23	21	Mitsubishi	13	16	23.1	0.4
NA	22	Philips	0	16	NA	0.4
19	23	Atmel	18	14	-22.2	0.3
26	24	Samsung	9	13	44.4	0.3
24	25	Austria Mikro Systeme	12	10	-16.7	0.2
27	26	Exar	9	10	11.1	0.2
30	27	Analog Devices	5	10	100.0	0.2
NA	28	ISD	0	10	NA	0.2
28	29	Micronas	8	9	12.5	0.2
29	30	Seiko Epson	6	8	33.3	0.2
16	31	Oki	23	7	-69.6	0.2
31	32	Allegro MicroSystems	5	6	20.0	0.1
32	33	Raytheon	5	6	20.0	0.1
34	34	Rockwell	4	5	25.0	0.1
35	35	Alcatel Microelectronics	4	5	25.0	0.1
38	36	TEMIC	3	5	66.7	0.1
36	37	Mitel	4	3	-25.0	0

Table 4-2 (Continued)
Top 48 Worldwide Companies' Vendor Revenue from Shipments of Total Cell-Based ICs to Americas (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
37	38	IMI	3	3	0	0
41	39	LG Semicon	2	3	50.0	0
43	40	Rohm	2	3	50.0	0
45	41	Melexis	1	3	200.0	0
40	42	Matsushita	2	2	0	0
42	43	Applied Micro Circuits Corp.	2	2	0	0
44	44	Micro Linear	2	2	0	0
NA	45	EM Microelectronics Marin	0	2	NA	0
25	46	SANYO	10	1	-90.0	0
33	47	IMP	5	0	-100.0	0
39	48	Macronix	3	0	-100.0	0
		All Others	15	20	33.3	0.5
		Americas Companies	2,336	3,533	51.2	86.2
		Japanese Companies	320	401	25.3	9.8
		European Companies	118	149	26.3	3.6
		Asia/Pacific Companies	14	16	14.3	0.4
		Total Market	**2,788**	**4,099**	**47.0**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Table 4-3
Top 43 Worldwide Companies' Vendor Revenue from Shipments of Total Gate Arrays to Americas (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	LSI Logic	420	232	-44.8	13.3
3	2	NEC	219	212	-3.2	12.1
5	3	Texas Instruments	180	161	-10.6	9.2
2	4	Toshiba	242	160	-33.9	9.2
6	5	Mitsubishi	126	139	10.3	8.0
4	6	IBM	208	133	-36.1	7.6
7	7	Motorola	124	82	-33.9	4.7
8	8	Gould AMI	60	78	30.0	4.5
9	9	Fujitsu	52	58	11.5	3.3
10	10	VLSI Technology	50	58	16.0	3.3
27	11	Matsushita	7	38	442.9	2.2
11	12	SGS-Thomson	47	37	-21.3	2.1
13	13	Atmel	30	37	23.3	2.1
12	14	Samsung	32	29	-9.4	1.7
19	15	GEC Plessey	19	29	52.6	1.7
NA	16	Vitesse	0	28	NA	1.6
14	17	Seiko Epson	29	27	-6.9	1.5
17	18	Chip Express	22	25	13.6	1.4
16	19	Oki	25	21	-16.0	1.2
15	20	Hitachi	25	19	-24.0	1.1
21	21	National Semiconductor	16	18	12.5	1.0
23	22	LG Semicon	13	16	23.1	0.9
NA	23	Raytheon	0	16	NA	0.9
22	24	Applied Micro Circuits Corp.	16	13	-18.8	0.7
NA	25	Cherry Semiconductor	0	11	NA	0.6
26	26	Hughes	10	9	-10.0	0.5
NA	27	Micro Linear	0	6	NA	0.3
20	28	IMI	17	5	-70.6	0.3
NA	29	Exar	0	5	NA	0.3
NA	30	Gennum	0	5	NA	0.3
30	31	Rohm	3	4	33.3	0.2
28	32	Sony	5	3	-40.0	0.2
29	33	SANYO	4	2	-50.0	0.1
33	34	Eteq Microsystems	2	2	0	0.1
25	35	Symbios	11	1	-90.9	0
31	36	Hyundai	3	1	-66.7	0
32	37	Harris Semiconductor	2	1	-50.0	0

Table 4-3 (Continued)
Top 43 Worldwide Companies' Vendor Revenue from Shipments of Total Gate Arrays to Americas (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
34	38	Yamaha	2	1	-50.0	0
NA	39	TEMIC	0	1	NA	0
18	40	Lucent Technologies	20	0	-100.0	0
24	41	Macronix	13	0	-100.0	0
35	42	Ricoh	2	0	-100.0	0
36	43	Holtek	1	0	-100.0	0
		All Others	25	23	-8.0	1.3
		Americas Companies	1,213	949	-21.8	54.4
		Japanese Companies	741	684	-7.7	39.2
		European Companies	66	67	1.5	3.8
		Asia/Pacific Companies	62	46	-25.8	2.6
		Total Market	**2,082**	**1,746**	**-16.1**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Table 4-4
Top 13 Worldwide Companies' Vendor Revenue from Shipments of PLDs to Americas (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	Xilinx	363	386	6.3	30.8
2	2	Altera	265	353	33.2	28.2
3	3	Advanced Micro Devices	134	136	1.5	10.9
4	4	Lattice	112	127	13.4	10.1
5	5	Actel	100	111	11.0	8.9
6	6	Lucent Technologies	50	60	20.0	4.8
7	7	Cypress Semiconductor	35	37	5.7	3.0
8	8	Atmel	25	21	-16.0	1.7
9	9	QuickLogic	18	13	-27.8	1.0
10	10	International CMOS Technology	9	5	-44.4	0.4
12	11	Philips	1	2	100.0	0.2
11	12	Texas Instruments	4	1	-75.0	0
NA	13	Toshiba	0	1	NA	0
		All Others	-	-	NA	0
		Americas Companies	1,115	1,250	12.1	99.8
		Japanese Companies	0	1	NA	0
		European Companies	1	2	100.0	0.2
		Asia/Pacific Companies	0	0	NA	0
		Total Market	**1,116**	**1,253**	**12.3**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Chapter 5
Top Companies' Japanese ASIC Revenue

Table 5-1
Top 48 Worldwide Companies' Vendor Revenue from Shipments of Total ASICs to Japan (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	NEC	1,069	1,128	5.5	24.6
2	2	Fujitsu	921	972	5.5	21.2
3	3	Hitachi	393	381	-3.1	8.3
5	4	LSI Logic	240	355	47.9	7.8
4	5	Toshiba	378	284	-24.9	6.2
6	6	Texas Instruments	237	220	-7.2	4.8
7	7	Matsushita	211	191	-9.5	4.2
8	8	Mitsubishi	114	132	15.8	2.9
9	9	Altera	95	114	20.0	2.5
11	10	Sharp	91	99	8.8	2.2
10	11	Lucent Technologies	95	87	-8.4	1.9
15	12	Seiko Epson	55	66	20.0	1.4
14	13	Xilinx	55	61	10.9	1.3
22	14	SANYO	23	57	147.8	1.2
12	15	Oki	61	40	-34.4	0.9
17	16	Lattice	40	40	0	0.9
16	17	IBM	41	36	-12.2	0.8
13	18	VLSI Technology	55	35	-36.4	0.8
20	19	Motorola	31	34	9.7	0.7
18	20	Rohm	35	33	-5.7	0.7
38	21	Macronix	2	33	1,550.0	0.7
19	22	Advanced Micro Devices	33	29	-12.1	0.6
24	23	Sony	12	21	75.0	0.5
23	24	Actel	15	14	-6.7	0.3
NA	25	QuickLogic	0	10	NA	0.2
25	26	National Semiconductor	11	9	-18.2	0.2
26	27	Hewlett-Packard	8	9	12.5	0.2
77	28	ISD	0	9	NA	0.2
27	29	Integrated Circuit Systems	7	8	14.3	0.2
32	30	Samsung	5	8	60.0	0.2
28	31	Yamaha	7	7	0	0.2
31	32	GEC Plessey	5	7	40.0	0.2
33	33	SGS-Thomson	3	7	133.3	0.2

Table 5-1 (Continued)
Top 48 Worldwide Companies' Vendor Revenue from Shipments of Total ASICs to Japan (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
21	34	Ricoh	30	5	-83.3	0.1
30	35	Symbios	5	5	0	0.1
NA	36	Vitesse	0	5	NA	0.1
NA	37	TEMIC	0	5	NA	0.1
29	38	Cypress Semiconductor	6	3	-50.0	0
36	39	Exar	2	3	50.0	0
37	40	Gould AMI	2	3	50.0	0
42	41	Raytheon	1	3	200.0	0
34	42	Analog Devices	2	2	0	0
35	43	Atmel	2	2	0	0
40	44	Harris Semiconductor	1	2	100.0	0
39	45	Chip Express	1	1	0	0
43	46	Micronas	1	1	0	0
NA	47	Gennum	0	1	NA	0
41	48	International CMOS Technology	1	0	-100.0	0
		All Others	-	-	NA	0
		Americas Companies	986	1,100	11.6	24.0
		Japanese Companies	3,400	3,416	0.5	74.6
		European Companies	9	20	122.2	0.4
		Asia/Pacific Companies	7	41	485.7	0.9
		Total Market	**4,402**	**4,577**	**4.0**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Table 5-2
Top 35 Worldwide Companies' Vendor Revenue from Shipments of Total Cell-Based ICs to Japan (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	NEC	464	512	10.3	25.6
2	2	Fujitsu	286	328	14.7	16.4
3	3	LSI Logic	185	328	77.3	16.4
5	4	Texas Instruments	156	160	2.6	8.0
4	5	Toshiba	171	115	-32.7	5.8
6	6	Matsushita	130	115	-11.5	5.8
8	7	Hitachi	87	88	1.1	4.4
7	8	Lucent Technologies	90	82	-8.9	4.1
10	9	Sharp	38	45	18.4	2.3
9	10	VLSI Technology	55	35	-36.4	1.8
12	11	IBM	28	29	3.6	1.5
13	12	Mitsubishi	20	24	20.0	1.2
20	13	SANYO	5	19	280.0	1.0
15	14	Rohm	16	15	-6.3	0.8
NA	15	Motorola	0	11	NA	0.6
11	16	Oki	32	9	-71.9	0.5
17	17	Seiko Epson	8	9	12.5	0.5
18	18	Hewlett-Packard	8	9	12.5	0.5
NA	19	ISD	0	9	NA	0.5
16	20	National Semiconductor	10	8	-20.0	0.4
19	21	Integrated Circuit Systems	7	8	14.3	0.4
24	22	SGS-Thomson	3	7	133.3	0.4
21	23	Yamaha	5	5	0	0.3
22	24	Symbios	5	5	0	0.3
23	25	GEC Plessey	4	5	25.0	0.3
NA	26	TEMIC	0	5	NA	0.3
25	27	Analog Devices	2	2	0	0.1
26	28	Exar	2	2	0	0.1
27	29	Samsung	1	2	100.0	0.1
29	30	Harris Semiconductor	1	2	100.0	0.1
NA	31	Macronix	0	2	NA	0.1
28	32	Atmel	1	1	0	0
30	33	Raytheon	1	1	0	0
31	34	Micronas	1	1	0	0
14	35	Ricoh	17	0	-100.0	0
		All Others	-	-	NA	0

Table 5-2 (Continued)
Top 35 Worldwide Companies' Vendor Revenue from Shipments of Total Cell-Based ICs to Japan (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
		Americas Companies	551	692	25.6	34.6
		Japanese Companies	1,279	1,284	0.4	64.3
		European Companies	8	18	125.0	0.9
		Asia/Pacific Companies	1	4	300.0	0.2
		Total Market	**1,839**	**1,998**	**8.6**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Table 5-3
Top 28 Worldwide Companies' Vendor Revenue from Shipments of Total Gate Arrays to Japan (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	Fujitsu	635	644	1.4	28.0
2	2	NEC	605	616	1.8	26.8
3	3	Hitachi	306	293	-4.2	12.7
4	4	Toshiba	205	168	-18.0	7.3
5	5	Mitsubishi	94	108	14.9	4.7
6	6	Matsushita	81	76	-6.2	3.3
7	7	Texas Instruments	80	59	-26.3	2.6
10	8	Seiko Epson	47	57	21.3	2.5
9	9	Sharp	53	54	1.9	2.3
14	10	SANYO	18	38	111.1	1.7
12	11	Oki	29	31	6.9	1.3
20	12	Macronix	2	31	1,450.0	1.3
8	13	LSI Logic	55	27	-50.9	1.2
11	14	Motorola	31	23	-25.8	1.0
17	15	Sony	12	21	75.0	0.9
13	16	Rohm	19	18	-5.3	0.8
15	17	IBM	13	7	-46.2	0.3
18	18	Samsung	4	6	50.0	0.3
NA	19	Vitesse	0	5	NA	0.2
16	20	Ricoh	12	4	-66.7	0.2
21	21	Gould AMI	2	3	50.0	0.1
19	22	Yamaha	2	2	0	0
23	23	GEC Plessey	1	2	100.0	0
NA	24	Raytheon	0	2	NA	0
22	25	National Semiconductor	1	1	0	0
24	26	Chip Express	1	1	0	0
NA	27	Exar	0	1	NA	0
NA	28	Gennum	0	1	NA	0
		All Others	-	-	NA	0
		Americas Companies	183	130	-29.0	5.7
		Japanese Companies	2,118	2,130	0.6	92.6
		European Companies	1	2	100.0	0
		Asia/Pacific Companies	6	37	516.7	1.6
		Total Market	**2,308**	**2,299**	**-0.4**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Table 5-4
Top 13 Worldwide Companies' Vendor Revenue from Shipments of PLDs to Japan (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	Altera	95	114	20.0	40.7
2	2	Xilinx	55	61	10.9	21.8
3	3	Lattice	40	40	0	14.3
4	4	Advanced Micro Devices	33	29	-12.1	10.4
5	5	Actel	15	14	-6.7	5.0
NA	6	QuickLogic	0	10	NA	3.6
7	7	Lucent Technologies	5	5	0	1.8
6	8	Cypress Semiconductor	6	3	-50.0	1.1
8	9	Toshiba	2	1	-50.0	0.4
9	10	Texas Instruments	1	1	0	0.4
10	11	Ricoh	1	1	0	0.4
11	12	Atmel	1	1	0	0.4
12	13	International CMOS Technology	1	0	-100.0	0
		All Others	-	-	NA	0
		Americas Companies	252	278	10.3	99.3
		Japanese Companies	3	2	-33.3	0.7
		European Companies	0	0	NA	0
		Asia/Pacific Companies	0	0	NA	0
		Total Market	**255**	**280**	**9.8**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Chapter 6
Top Companies' Europe, Africa, and Middle East ASIC Revenue

Table 6-1
Top 59 Worldwide Companies' Vendor Revenue from Shipments of Total ASICs to Europe, Africa, and Middle East (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	Lucent Technologies	280	285	1.8	8.9
4	2	VLSI Technology	179	272	52.0	8.5
2	3	Texas Instruments	195	242	24.1	7.6
7	4	NEC	156	219	40.4	6.9
6	5	SGS-Thomson	167	217	29.9	6.8
3	6	LSI Logic	188	204	8.5	6.4
5	7	Alcatel Microelectronics	173	196	13.3	6.1
8	8	Xilinx	125	128	2.4	4.0
10	9	Altera	104	126	21.2	3.9
11	10	GEC Plessey	103	103	0	3.2
9	11	Austria Mikro Systeme	106	102	-3.8	3.2
17	12	Fujitsu	68	99	45.6	3.1
12	13	Toshiba	94	86	-8.5	2.7
14	14	Motorola	88	80	-9.1	2.5
18	15	Hewlett-Packard	59	77	30.5	2.4
13	16	IBM	90	70	-22.2	2.2
15	17	Atmel	79	60	-24.1	1.9
19	18	Advanced Micro Devices	54	59	9.3	1.8
20	19	TEMIC	53	56	5.7	1.8
16	20	Hitachi	70	55	-21.4	1.7
23	21	Lattice	30	55	83.3	1.7
21	22	National Semiconductor	51	53	3.9	1.7
24	23	TCS	28	40	42.9	1.3
31	24	Ericsson	19	30	57.9	0.9
27	25	Micronas	24	25	4.2	0.8
22	26	Siemens	31	23	-25.8	0.7
25	27	Actel	26	23	-11.5	0.7
26	28	Symbios	26	22	-15.4	0.7
NA	29	ISD	0	18	NA	0.6
28	30	EM Microelectronics Marin	22	17	-22.7	0.5
NA	31	Vitesse	0	17	NA	0.5

Table 6-1 (Continued)
Top 59 Worldwide Companies' Vendor Revenue from Shipments of Total ASICs to Europe, Africa, and Middle East (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
30	32	Mitel	20	12	-40.0	0.4
32	33	Oki	15	11	-26.7	0.3
33	34	Cypress Semiconductor	14	11	-21.4	0.3
29	35	Harris Semiconductor	20	10	-50.0	0.3
37	36	Elmos	7	9	28.6	0.3
34	37	Seiko Epson	8	8	0	0.3
36	38	Integrated Circuit Systems	7	8	14.3	0.3
35	39	Melexis	8	6	-25.0	0.2
39	40	Gould AMI	5	6	20.0	0.2
51	41	Mitsubishi	1	6	500.0	0.2
52	42	Philips	1	6	500.0	0.2
38	43	Analog Devices	5	5	0	0.2
41	44	PMC Sierra Semiconductor	5	5	0	0.2
40	45	QuickLogic	5	4	-20.0	0.1
42	46	Samsung	5	4	-20.0	0.1
43	47	Exar	2	3	50.0	0
47	48	Chip Express	1	3	200.0	0
NA	49	Gennum	0	3	NA	0
44	50	Hughes	2	2	0	0
50	51	Raytheon	1	2	100.0	0
NA	52	Zetex	0	2	NA	0
45	53	Allegro MicroSystems	1	1	0	0
46	54	Applied Micro Circuits Corp.	1	1	0	0
48	55	Eteq Microsystems	1	1	0	0
NA	56	SANYO	0	1	NA	0
218	57	Sony	0	1	NA	0
49	58	International CMOS Technology	1	0	-100.0	0
53	59	Holtek	1	0	-100.0	0
		All Others	-	-	NA	0
		Americas Companies	1,665	1,868	12.2	58.6
		Japanese Companies	412	486	18.0	15.2
		European Companies	742	832	12.1	26.1
		Asia/Pacific Companies	6	4	-33.3	0.1
		Total Market	**2,825**	**3,190**	**12.9**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Table 6-2
Top 40 Worldwide Companies' Vendor Revenue from Shipments of Total Cell-Based ICs to Europe, Africa, and Middle East (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	Lucent Technologies	270	275	1.9	13.7
3	2	VLSI Technology	170	264	55.3	13.1
2	3	Alcatel Microelectronics	173	196	13.3	9.7
4	4	SGS-Thomson	138	174	26.1	8.6
7	5	NEC	93	147	58.1	7.3
8	6	Texas Instruments	85	110	29.4	5.5
6	7	Austria Mikro Systeme	98	95	-3.1	4.7
5	8	LSI Logic	101	83	-17.8	4.1
11	9	Hewlett-Packard	59	77	30.5	3.8
9	10	IBM	69	60	-13.0	3.0
10	11	Atmel	68	49	-27.9	2.4
12	12	Motorola	47	45	-4.3	2.2
21	13	TEMIC	19	41	115.8	2.0
16	14	TCS	27	35	29.6	1.7
13	15	Hitachi	46	34	-26.1	1.7
14	16	National Semiconductor	33	32	-3.0	1.6
24	17	GEC Plessey	18	32	77.8	1.6
25	18	Fujitsu	18	31	72.2	1.5
22	19	Ericsson	19	30	57.9	1.5
26	20	Toshiba	17	26	52.9	1.3
18	21	Micronas	24	25	4.2	1.2
15	22	Siemens	31	23	-25.8	1.1
17	23	Symbios	26	22	-15.4	1.1
NA	24	ISD	0	18	NA	0.9
19	25	EM Microelectronics Marin	22	17	-22.7	0.8
20	26	Mitel	20	12	-40.0	0.6
23	27	Harris Semiconductor	19	10	-47.4	0.5
28	28	Elmos	7	9	28.6	0.4
29	29	Integrated Circuit Systems	7	8	14.3	0.4
27	30	Melexis	8	6	-25.0	0.3
31	31	Analog Devices	5	5	0	0.2
32	32	PMC Sierra Semiconductor	5	5	0	0.2
NA	33	Philips	0	5	NA	0.2
30	34	Oki	5	2	-60.0	0
33	35	Exar	2	2	0	0
34	36	Hughes	2	2	0	0
NA	37	Gould AMI	0	2	NA	0

Table 6-2 (Continued)
Top 40 Worldwide Companies' Vendor Revenue from Shipments of Total Cell-Based ICs to Europe, Africa, and Middle East (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
NA	38	Mitsubishi	0	2	NA	0
35	39	Allegro MicroSystems	1	1	0	0
36	40	Raytheon	1	1	0	0
		All Others	-	-	NA	0
		Americas Companies	990	1,083	9.4	53.8
		Japanese Companies	179	242	35.2	12.0
		European Companies	584	688	17.8	34.2
		Asia/Pacific Companies	0	0	NA	0
		Total Market	**1,753**	**2,013**	**14.8**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Table 6-3
Top 33 Worldwide Companies' Vendor Revenue from Shipments of Total Gate Arrays to Europe, Africa, and Middle East (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	Texas Instruments	110	131	19.1	17.4
2	2	LSI Logic	87	121	39.1	16.1
5	3	NEC	63	72	14.3	9.6
3	4	GEC Plessey	85	71	-16.5	9.4
6	5	Fujitsu	50	68	36.0	9.0
4	6	Toshiba	77	60	-22.1	8.0
9	7	SGS-Thomson	29	43	48.3	5.7
7	8	Motorola	41	35	-14.6	4.7
10	9	Hitachi	24	21	-12.5	2.8
12	10	National Semiconductor	18	21	16.7	2.8
NA	11	Vitesse	0	17	NA	2.3
8	12	TEMIC	34	15	-55.9	2.0
11	13	IBM	21	10	-52.4	1.3
13	14	Oki	10	9	-10.0	1.2
14	15	VLSI Technology	9	8	-11.1	1.1
16	16	Seiko Epson	8	8	0	1.1
15	17	Austria Mikro Systeme	8	7	-12.5	0.9
20	18	TCS	1	5	400.0	0.7
17	19	Atmel	6	4	-33.3	0.5
18	20	Gould AMI	5	4	-20.0	0.5
19	21	Samsung	5	4	-20.0	0.5
22	22	Mitsubishi	1	4	300.0	0.5
23	23	Chip Express	1	3	200.0	0.4
NA	24	Gennum	0	3	NA	0.4
NA	25	Zetex	0	2	NA	0.3
24	26	Applied Micro Circuits Corp.	1	1	0	0.1
25	27	Eteq Microsystems	1	1	0	0.1
NA	28	Exar	0	1	NA	0.1
NA	29	Raytheon	0	1	NA	0.1
NA	30	SANYO	0	1	NA	0.1
NA	31	Sony	0	1	NA	0.1
21	32	Harris Semiconductor	1	0	-100.0	0
26	33	Holtek	1	0	-100.0	0

Table 6-3 (Continued)
Top 33 Worldwide Companies' Vendor Revenue from Shipments of Total Gate Arrays to Europe, Africa, and Middle East (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
		All Others	-	-	NA	0
		Americas Companies	301	361	19.9	48.0
		Japanese Companies	233	244	4.7	32.4
		European Companies	157	143	-8.9	19.0
		Asia/Pacific Companies	6	4	-33.3	0.5
		Total Market	**697**	**752**	**7.9**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Table 6-4
Top 12 Worldwide Companies' Vendor Revenue from Shipments of PLDs to Europe, Africa, and Middle East (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	Xilinx	125	128	2.4	30.1
2	2	Altera	104	126	21.2	29.6
3	3	Advanced Micro Devices	54	59	9.3	13.9
4	4	Lattice	30	55	83.3	12.9
5	5	Actel	26	23	-11.5	5.4
6	6	Cypress Semiconductor	14	11	-21.4	2.6
7	7	Lucent Technologies	10	10	0	2.4
8	8	Atmel	5	7	40.0	1.6
9	9	QuickLogic	5	4	-20.0	0.9
10	10	Philips	1	1	0	0.2
NA	11	Texas Instruments	0	1	NA	0.2
11	12	International CMOS Technology	1	0	-100.0	0
		All Others	-	-	NA	0
		Americas Companies	374	424	13.4	99.8
		Japanese Companies	0	0	NA	0
		European Companies	1	1	0	0.2
		Asia/Pacific Companies	0	0	NA	0
		Total Market	**375**	**425**	**13.3**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Chapter 7
Top Companies' Asia/Pacific ASIC Revenue

Table 7-1
Top 59 Worldwide Companies' Vendor Revenue from Shipments of Total ASICs to Asia/Pacific (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	Lucent Technologies	200	369	84.5	22.2
2	2	Texas Instruments	196	222	13.3	13.4
4	3	NEC	86	108	25.6	6.5
7	4	LG Semicon	74	80	8.1	4.8
9	5	Hewlett-Packard	66	79	19.7	4.8
10	6	Fujitsu	62	79	27.4	4.8
11	7	Samsung	61	71	16.4	4.3
3	8	SGS-Thomson	106	57	-46.2	3.4
14	9	LSI Logic	38	54	42.1	3.2
5	10	IBM	83	53	-36.1	3.2
21	11	Motorola	22	39	77.3	2.3
16	12	Altera	33	38	15.2	2.3
6	13	Toshiba	75	37	-50.7	2.2
19	14	Xilinx	23	37	60.9	2.2
18	15	Integrated Circuit Systems	25	34	36.0	2.0
13	16	Symbios	40	33	-17.5	2.0
12	17	Hitachi	48	30	-37.5	1.8
17	18	Matsushita	32	27	-15.6	1.6
24	19	Lattice	18	20	11.1	1.2
20	20	Advanced Micro Devices	22	19	-13.6	1.1
15	21	GEC Plessey	38	17	-55.3	1.0
8	22	VLSI Technology	67	15	-77.6	0.9
37	23	Atmel	3	15	400.0	0.9
27	24	Sharp	12	12	0	0.7
NA	25	ISD	0	11	NA	0.7
22	26	IMI	19	8	-57.9	0.5
28	27	Actel	8	8	0	0.5
33	28	Sony	6	8	33.3	0.5
26	29	Oki	13	6	-53.8	0.4
32	30	Seiko Epson	6	6	0	0.4
39	31	EM Microelectronics Marin	3	6	100.0	0.4
23	32	SANYO	19	4	-78.9	0.2
34	33	Austria Mikro Systeme	6	4	-33.3	0.2

Table 7-1 (Continued)
Top 59 Worldwide Companies' Vendor Revenue from Shipments of Total ASICs to Asia/Pacific (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
38	34	PMC Sierra Semiconductor	3	4	33.3	0.2
NA	35	Gould AMI	0	4	NA	0.2
25	36	Macronix	18	3	-83.3	0.2
29	37	National Semiconductor	8	3	-62.5	0.2
31	38	Harris Semiconductor	7	3	-57.1	0.2
35	39	Hyundai	6	3	-50.0	0.2
40	40	Daewoo	3	3	0	0.2
42	41	Exar	2	3	50.0	0.2
44	42	Mitsubishi	2	3	50.0	0.2
45	43	Alcatel Microelectronics	2	3	50.0	0.2
46	44	Holtek	2	3	50.0	0.2
52	45	Micro Linear	1	3	200.0	0.2
NA	46	Vitesse	0	3	NA	0.2
41	47	Analog Devices	2	2	0	0.1
43	48	QuickLogic	2	2	0	0.1
47	49	Allegro MicroSystems	1	2	100.0	0.1
49	50	Chip Express	1	2	100.0	0.1
36	51	Cypress Semiconductor	5	1	-80.0	0
48	52	Applied Micro Circuits Corp.	1	1	0	0
50	53	Eteq Microsystems	1	1	0	0
53	54	Philips	1	1	0	0
54	55	Hualon Microelectronics Corp.	1	1	0	0
NA	56	Raytheon	0	1	NA	0
NA	57	TEMIC	0	1	NA	0
30	58	Rohm	8	0	-100.0	0
51	59	International CMOS Technology	1	0	-100.0	0
		All Others	-	-	NA	0
		Americas Companies	898	1,089	21.3	65.5
		Japanese Companies	369	320	-13.3	19.3
		European Companies	156	89	-42.9	5.4
		Asia/Pacific Companies	165	164	-0.6	9.9
		Total Market	**1,588**	**1,662**	**4.7**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Table 7-2
Top 37 Worldwide Companies' Vendor Revenue from Shipments of Total Cell-Based ICs to Asia/Pacific (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	Lucent Technologies	190	354	86.3	33.6
2	2	Texas Instruments	136	170	25.0	16.1
4	3	Hewlett-Packard	66	79	19.7	7.5
3	4	SGS-Thomson	95	55	-42.1	5.2
6	5	IBM	55	42	-23.6	4.0
11	6	Fujitsu	25	40	60.0	3.8
12	7	Integrated Circuit Systems	25	34	36.0	3.2
7	8	Symbios	40	33	-17.5	3.1
10	9	NEC	25	33	32.0	3.1
19	10	Motorola	9	32	255.6	3.0
14	11	LG Semicon	20	28	40.0	2.7
9	12	Toshiba	31	17	-45.2	1.6
13	13	Matsushita	22	17	-22.7	1.6
15	14	LSI Logic	20	17	-15.0	1.6
18	15	Samsung	10	15	50.0	1.4
8	16	GEC Plessey	35	13	-62.9	1.2
NA	17	ISD	0	11	NA	1.0
16	18	Hitachi	15	10	-33.3	0.9
5	19	VLSI Technology	60	9	-85.0	0.9
24	20	EM Microelectronics Marin	3	6	100.0	0.6
NA	21	Atmel	0	6	NA	0.6
22	22	Austria Mikro Systeme	6	4	-33.3	0.4
25	23	PMC Sierra Semiconductor	3	4	33.3	0.4
21	24	Harris Semiconductor	7	3	-57.1	0.3
27	25	Alcatel Microelectronics	2	3	50.0	0.3
17	26	SANYO	14	2	-85.7	0.2
20	27	Oki	8	2	-75.0	0.2
26	28	IMI	2	2	0	0.2
28	29	Analog Devices	2	2	0	0.2
29	30	Exar	2	2	0	0.2
30	31	Allegro MicroSystems	1	2	100.0	0.2
NA	32	Gould AMI	0	2	NA	0.2
23	33	National Semiconductor	6	1	-83.3	0
31	34	Micro Linear	1	1	0	0
32	35	Hualon Microelectronics Corp.	1	1	0	0
NA	36	Macronix	0	1	NA	0
NA	37	Hyundai	0	1	NA	0
		All Others	-	-	NA	0

Table 7-2 (Continued)
Top 37 Worldwide Companies' Vendor Revenue from Shipments of Total Cell-Based ICs to Asia/Pacific (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
		Americas Companies	625	806	29.0	76.5
		Japanese Companies	140	121	-13.6	11.5
		European Companies	141	81	-42.6	7.7
		Asia/Pacific Companies	31	46	48.4	4.4
		Total Market	**937**	**1,054**	**12.5**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Table 7-3
Top 37 Worldwide Companies' Vendor Revenue from Shipments of Total Gate Arrays to Asia/Pacific (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	NEC	61	75	23.0	16.2
4	2	Samsung	51	56	9.8	12.1
2	3	Texas Instruments	60	52	-13.3	11.2
3	4	LG Semicon	54	52	-3.7	11.2
6	5	Fujitsu	37	39	5.4	8.4
9	6	LSI Logic	18	37	105.6	8.0
5	7	Toshiba	44	20	-54.5	4.3
7	8	Hitachi	33	20	-39.4	4.3
13	9	Sharp	12	12	0	2.6
8	10	IBM	28	11	-60.7	2.4
15	11	Matsushita	10	10	0	2.2
19	12	Sony	6	8	33.3	1.7
12	13	Motorola	13	7	-46.2	1.5
11	14	IMI	17	6	-64.7	1.3
17	15	VLSI Technology	7	6	-14.3	1.3
20	16	Seiko Epson	6	6	0	1.3
NA	17	Atmel	0	5	NA	1.1
22	18	Oki	5	4	-20.0	0.9
23	19	GEC Plessey	3	4	33.3	0.9
24	20	Daewoo	3	3	0	0.6
26	21	Mitsubishi	2	3	50.0	0.6
27	22	Holtek	2	3	50.0	0.6
NA	23	Vitesse	0	3	NA	0.6
10	24	Macronix	18	2	-88.9	0.4
14	25	SGS-Thomson	11	2	-81.8	0.4
18	26	Hyundai	6	2	-66.7	0.4
21	27	SANYO	5	2	-60.0	0.4
25	28	National Semiconductor	2	2	0	0.4
28	29	Chip Express	1	2	100.0	0.4
NA	30	Gould AMI	0	2	NA	0.4
NA	31	Micro Linear	0	2	NA	0.4
29	32	Applied Micro Circuits Corp.	1	1	0	0.2
30	33	Eteq Microsystems	1	1	0	0.2
NA	34	Exar	0	1	NA	0.2
NA	35	TEMIC	0	1	NA	0.2
NA	36	Raytheon	0	1	NA	0.2
16	37	Rohm	8	0	-100.0	0
		All Others	-	-	NA	0

Table 7-3 (Continued)
Top 37 Worldwide Companies' Vendor Revenue from Shipments of Total Gate Arrays to Asia/Pacific (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
		Americas Companies	148	139	-6.1	30.0
		Japanese Companies	229	199	-13.1	43.0
		European Companies	14	7	-50.0	1.5
		Asia/Pacific Companies	134	118	-11.9	25.5
		Total Market	**525**	**463**	**-11.8**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

Table 7-4
Top 11 Worldwide Companies' Vendor Revenue from Shipments of PLDs to Asia/Pacific (Millions of U.S. Dollars)

1996 Rank	1997 Rank	Company	1996 Revenue	1997 Revenue	Percentage Change	1997 Market Share (%)
1	1	Altera	33	38	15.2	26.2
2	2	Xilinx	23	37	60.9	25.5
4	3	Lattice	18	20	11.1	13.8
3	4	Advanced Micro Devices	22	19	-13.6	13.1
5	5	Lucent Technologies	10	15	50.0	10.3
6	6	Actel	8	8	0	5.5
8	7	Atmel	3	4	33.3	2.8
9	8	QuickLogic	2	2	0	1.4
7	9	Cypress Semiconductor	5	1	-80.0	0.7
10	10	Philips	1	1	0	0.7
11	11	International CMOS Technology	1	0	-100.0	0
		All Others	-	-	NA	0
		Americas Companies	125	144	15.2	99.3
		Japanese Companies	0	0	NA	0
		European Companies	1	1	0	0.7
		Asia/Pacific Companies	0	0	NA	0
		Total Market	**126**	**145**	**15.1**	**100.0**

NA = Not available
Source: Dataquest (April 1998)

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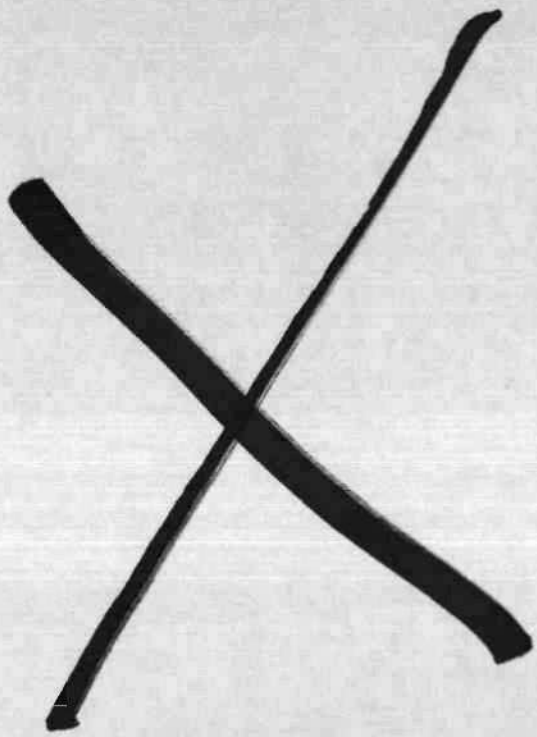

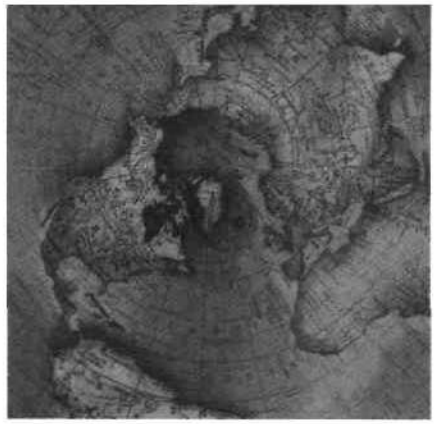

Dataquest

Designers Emphasize the "System" in SLI

User Wants and Needs

Program: ASIC/SLI Worldwide
Product Code: ASIC-WW-UW-9801
Publication Date: December 14, 1998
Filing: Reports

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Chapter 1
Executive Summary

In 1998, driven by a manufacturing overcapacity and overall global economic slowdown, the electronics industry has remained in the doldrums. The application-specific IC (ASIC) and programmable logic device (PLD) industries have not been immune, and only very fortunate (or well-positioned) vendors have shown any growth at all. On the technology side, however, advances keep coming, and the products of 1998 look nothing like those of just a few years ago. Among the most significant trends in the industry include the following:

- System-level integration (SLI) is becoming more of a mainstream solution, rather than being confined to just a few leading applications from a few leading vendors. A large number of second- and third-tier ASIC vendors are searching for ways to enter the market for single-chip systems.
- PLD companies are moving ever more aggressively into the ASIC market. This development has hastened the decline in gate array ASICs, particularly in the 20,000-gate and under segment, as discussed later in this report. PLD vendors are also looking to enter the SLI space as well.
- Semiconductor intellectual property (SIP) is becoming the hottest issue in the ASIC and PLD industries and one of the most exciting areas in electronics overall. Third-party SIP specialists, semiconductor manufacturers, fabless IC companies, and OEMs are all battling to control system SIP content, for this is the key to value and perhaps the only way to garner above-market profit margins.

From the user perspective, the message is clear. Dataquest's User Wants and Needs survey is designed to give semiconductor vendors insight into the hearts and minds of their customer base. Regardless of the world's economic pressures—or, more likely, as a result of these pressures—users are asking more and more from their suppliers. More functionality—in 1998, the average cell-based ASIC will have almost 200,000 logic gates and more than 64Kb of embedded memory; by 2000, over one-third of users will design mega/mega-chips, with more than 1,000,000 gates and 1Mb of memory. More performance, as well—well over one-half the cell-based designs in 1998 are targeted for speeds over 60 MHz, with this number exceeding 100 MHz in two years. However, these added capabilities must still be delivered in a timely fashion and at a low price.

Going beyond the basics required by the users, it is clear that the engagement model between vendor and customer is evolving. As more and more of the system finds its way onto a single chip, the ASIC or PLD vendor must continue to become more system savvy and be able to provide some of the basic system functions as predefined SIP. Users continue to guard the key system SIP jealously, however, and with good reason, because this is where the value lies. The ASIC and PLD vendors that find innovative ways to meet users' needs without becoming their customers' competitors are the ones that will successfully navigate the current doldrums and thrive when the industry sees the next upturn.

Project Analyst: Jordan Selburn, Principal Analyst

Chapter 2
Survey Methodology

Dataquest demand-side data is gathered using extensive survey techniques. End users are identified through a variety of means, including databases of past survey respondents, the registered user and prospect lists of the leading electronic design automation (EDA) companies, and subscribers to engineering periodicals. Surveys were distributed throughout North America, enabling Dataquest to put together, from a user point of view, a snapshot of current and future system design requirements and the applications driving ASIC and PLD usage.

This User Wants and Needs study includes data collected from the North American surveys. Surveys were received and processed in the second and third quarters of 1998. The responses of this survey were entered in a statistical package for analysis. This database allows Dataquest to do cross-tabulation of the data for improved analysis. Because of the timing of the survey, the responses allow comprehensive understanding of the current state of the industry as well as future user requirements.

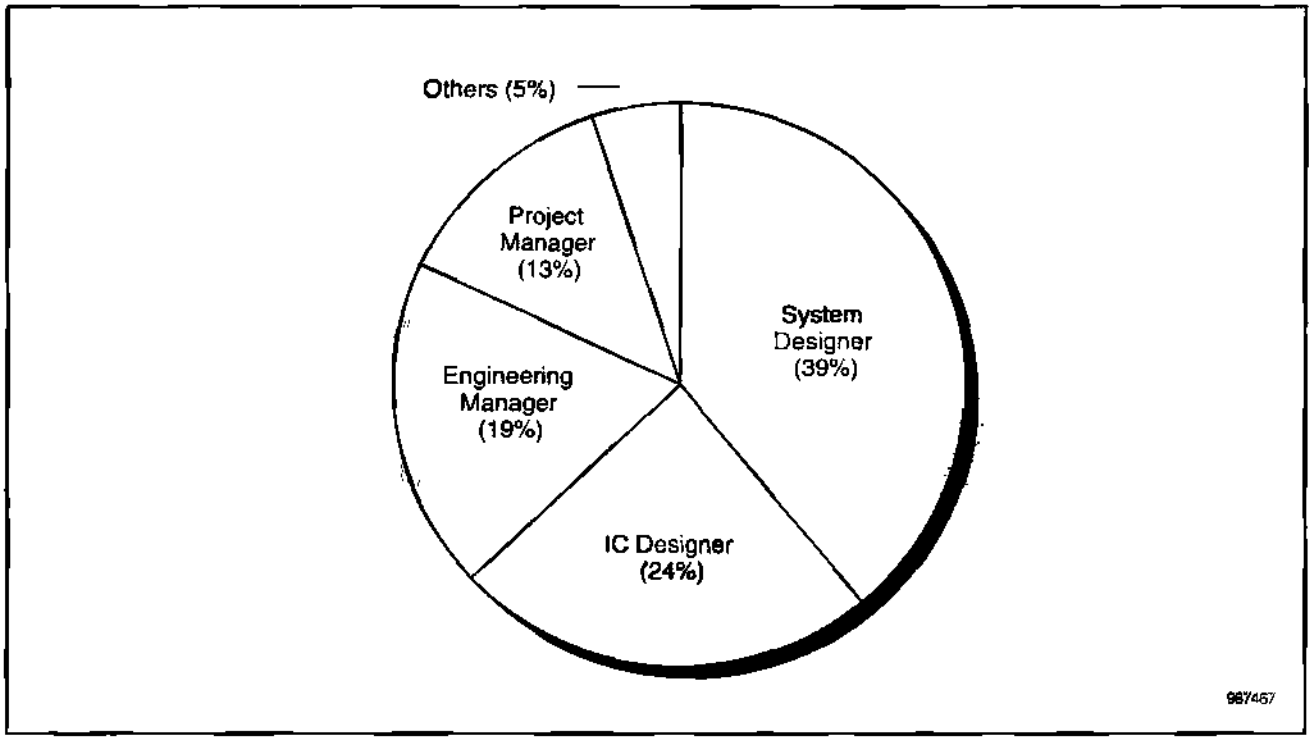
Respondent Demographics

Dataquest strives to gather an accurate representation of the design community, making sure to survey a large cross section of designers. Data collected in North America is predominantly from system design engineers and IC designers, who make up about 70 percent of the respondents. Engineering managers, the next largest category, provided 17 percent of the responses. Figure 2-1 shows the breakdown of respondents by job title. Dataquest believes that the data represents a statistically significant sample to gauge the needs and trends of the electronic system design community.

More than 10,000 surveys were distributed to sites across North America. The response rate, while decreased from 1997, is still sufficient to allow for analysis of the data not just as an aggregate but also by specific application type. Figure 2-2 shows the primary application areas that project team members designed in North America. It is important to note that designers often work on more than one application area; therefore, survey respondents were allowed to check more than one box for their project team's primary line of business. For this reason, certain responses have been classified under more than one application area.

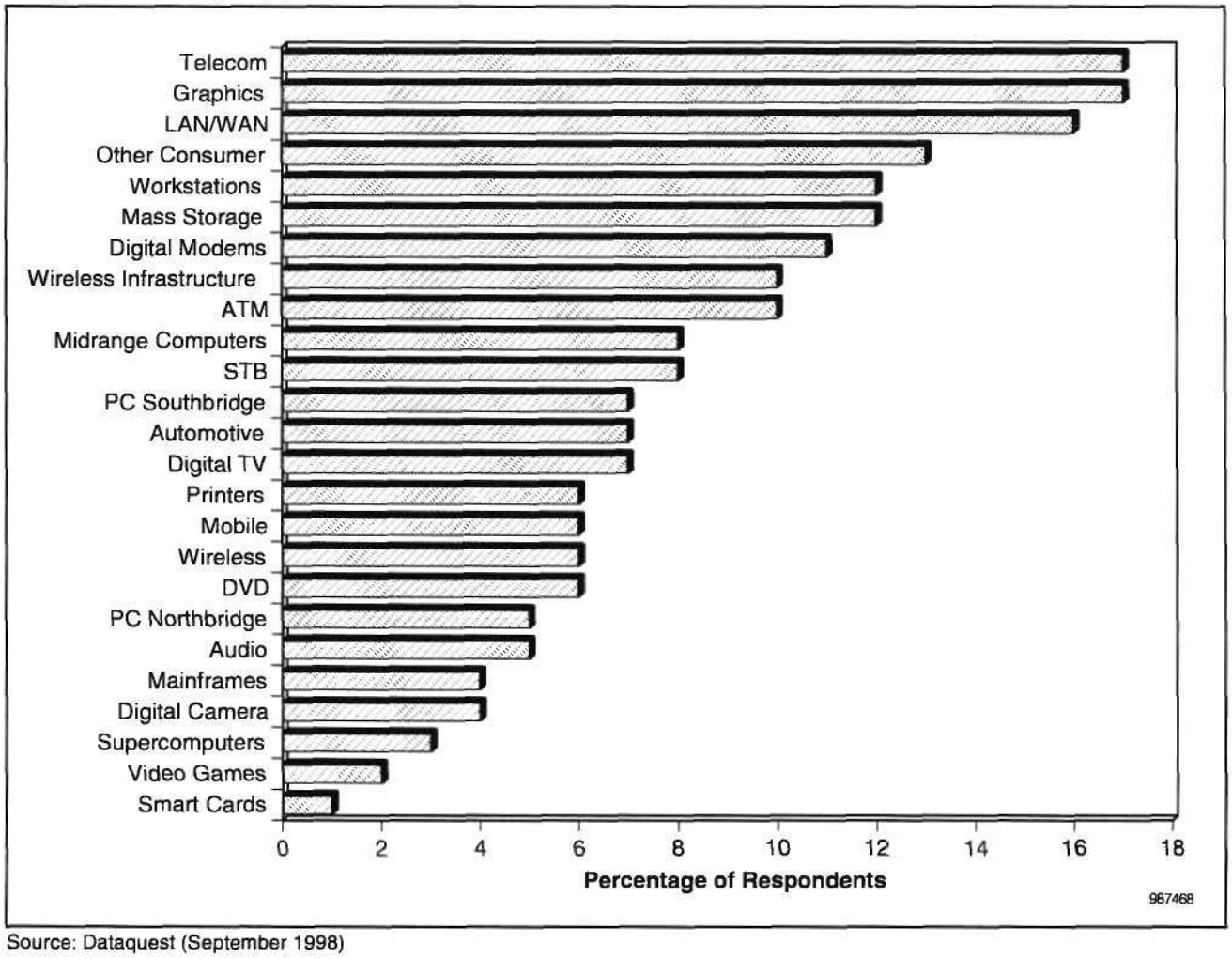
For this year's survey, Dataquest has substantially modified the application area breakdown to reflect new types of systems, as well as to provide more meaningful analysis of high-growth areas such as wireless. Although this modification may limit direct comparison of the 1998 survey with those of prior years, it allows for greater insight into the mind of today's ASIC and PLD user.

Figure 2-1
Respondents by Job Title



Source: Dataquest (September 1998)

Figure 2-2
Respondents by Application Project Team



Source: Dataquest (September 1998)

Chapter 3
Product Issues

The past year has been a difficult one in the semiconductor industry, with an upturn still perhaps a year away. One of the few bright spots is the integrated system subset of the ASIC market. Users are looking to bring more and more functionality on-chip as technology advances allow, yet this integration must be economically as well as technically feasible.

Systems designers have provided insight into their requirements and preferences for designing real ASICs in the real world. In this chapter, Dataquest investigates the various characteristics of today's design environment.

Critical Success Factors for ASICs

Functionality is only one attribute, albeit the most basic one, of a successful design. Beyond functionality, systems designers face cost, power consumption, performance, and other requirements. Although designers want to fulfill the "faster, cheaper, better" maxim with every design, tradeoffs are inevitable, and some attributes will be weighted more heavily than others. Different categories of products exhibit varying ranges of requirements. For example, wireless designs place a premium on integration and power consumption, with performance a secondary consideration. Fixed-location communications applications, in contrast, may be able to trade off savings in power consumption and board space for lower system cost and faster time to market.

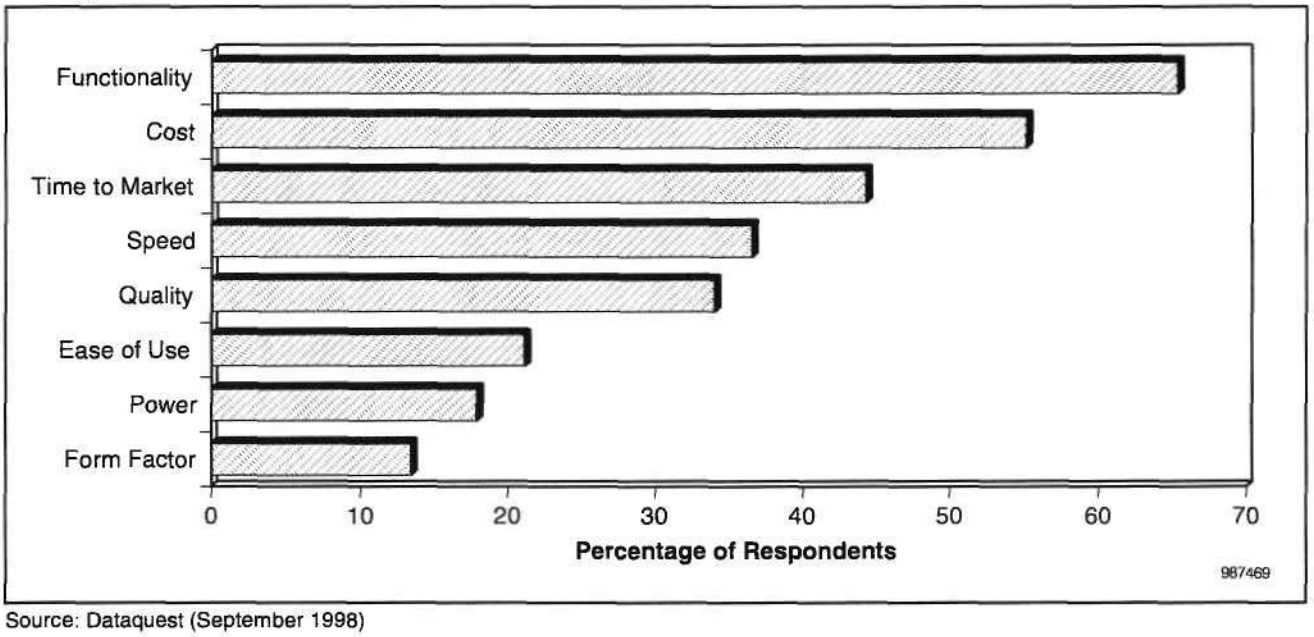
In this survey, Dataquest requested that respondents select the three characteristics most important for success in their particular marketplace. The top three responses overall were as follows (in order):

- Increasing functionality
- Reducing cost
- Reducing time to market

The overall results are shown in Figure 3-1. The top three responses commanded a significant lead over all others, as they have in previous versions of the survey. The continuing move toward system-level integration and the recognition that reducing ASIC cost is not necessarily the same as reducing the system cost and that a higher-priced ASIC may, in fact, provide the lowest overall system cost.

Still, it is clear that all three of the leading attributes must be met for the typical design to be successful. Time to market is becoming more important as end-product life cycles shorten; missing two months of an 18-month product life is much worse than missing two months of a 24-month window. The time-to-market factor conflicts somewhat with the drive toward system-level integration (it may be quicker to leave some parts of the design as standalone components, rather than embedding the functions), but increased design reuse and the availability of system-level macros will mitigate this conflict to some extent. One implication of the importance of time to market may be the rapid growth of relatively large-gate count PLDs at the expense of low-end gate arrays. PLDs, with virtually no turnaround time, beat gate arrays at their own game of short turnaround time (compared to cell-based ASICs).

Figure 3-1
Design Success Factors



Source: Dataquest (September 1998)

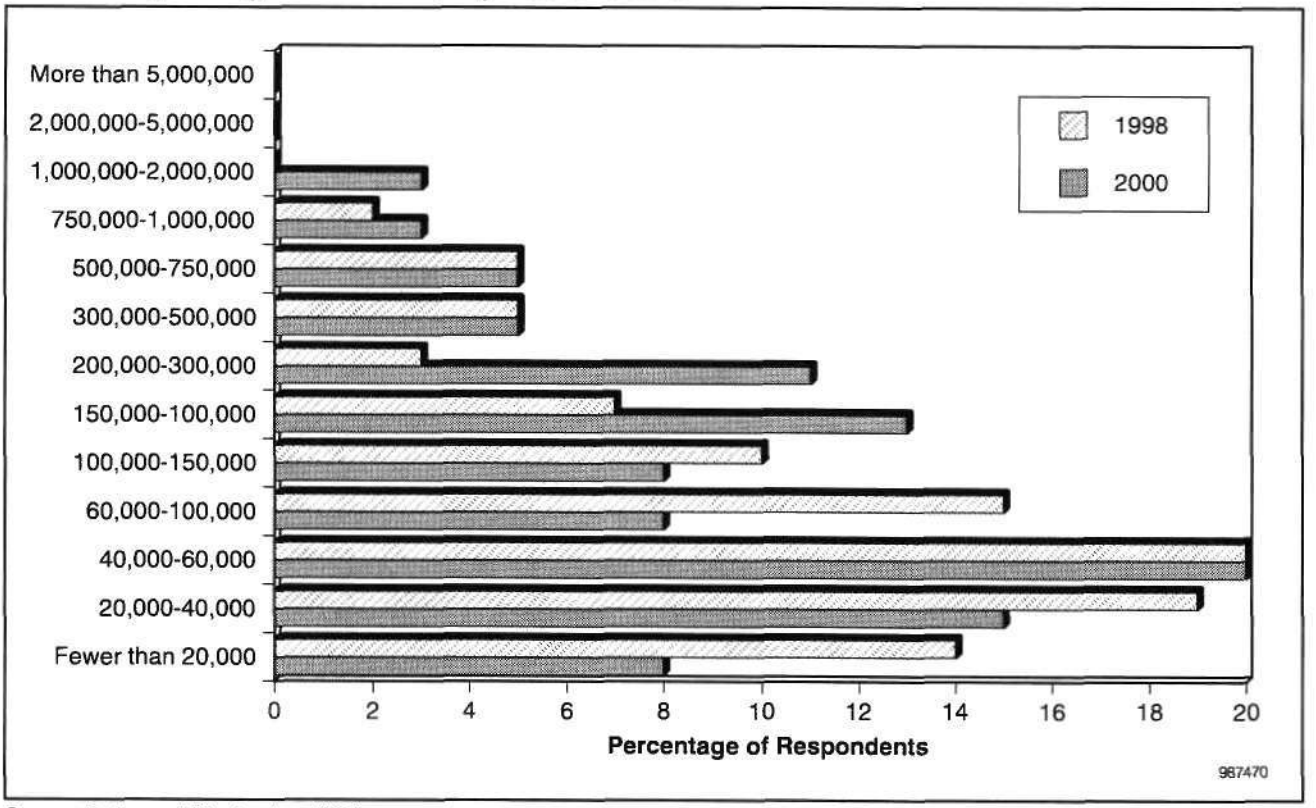
Cell-Based ICs and Gate Arrays

Gate Count Trends

ASIC design complexity continues to increase but not in a linear fashion. The ASIC of just a few years ago, which consisted of pure logic, has undergone a major transformation. The user's demand for embedded functions and embedded memory, coupled with the manufacturer's ability to incorporate them, has brought a fundamental change in the composition of ASICs, with a commensurate increase in content and complexity. As a result, yesterday's groundbreaking 100,000-gate design is less than the median logic content of today's cell-based ASICs.

For the 1998 version of the survey, Dataquest changed the way designers were asked about logic gate count. Figure 3-2 shows the *average* gate count for gate array designs; Figure 3-3 shows the *maximum*. The median gate count is now approaching 50,000 logic gates, and the number of design starts in the sub-20,000 gate range continues to decrease rapidly. This change most likely reflects the emergence of PLDs as a cost-competitive solution to these small gate arrays. The number of very large designs—those over 1,000,000 gates—continues to increase dramatically on a percentage basis. However, this increase in percentage almost certainly reflects the decrease in small designs rather than an explosion in the absolute number of large designs.

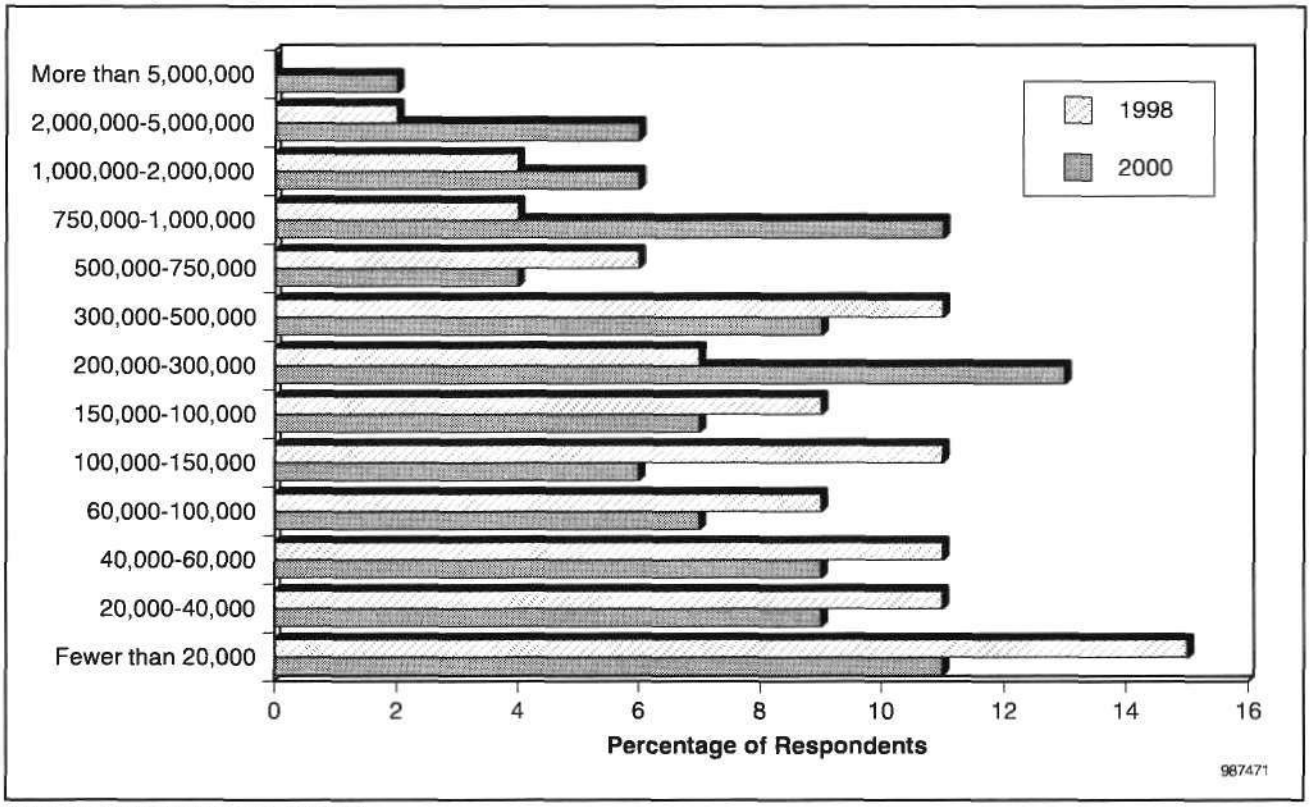
Figure 3-2
Gate Array Design Starts: Average Gate Count



Source: Dataquest (September 1998)

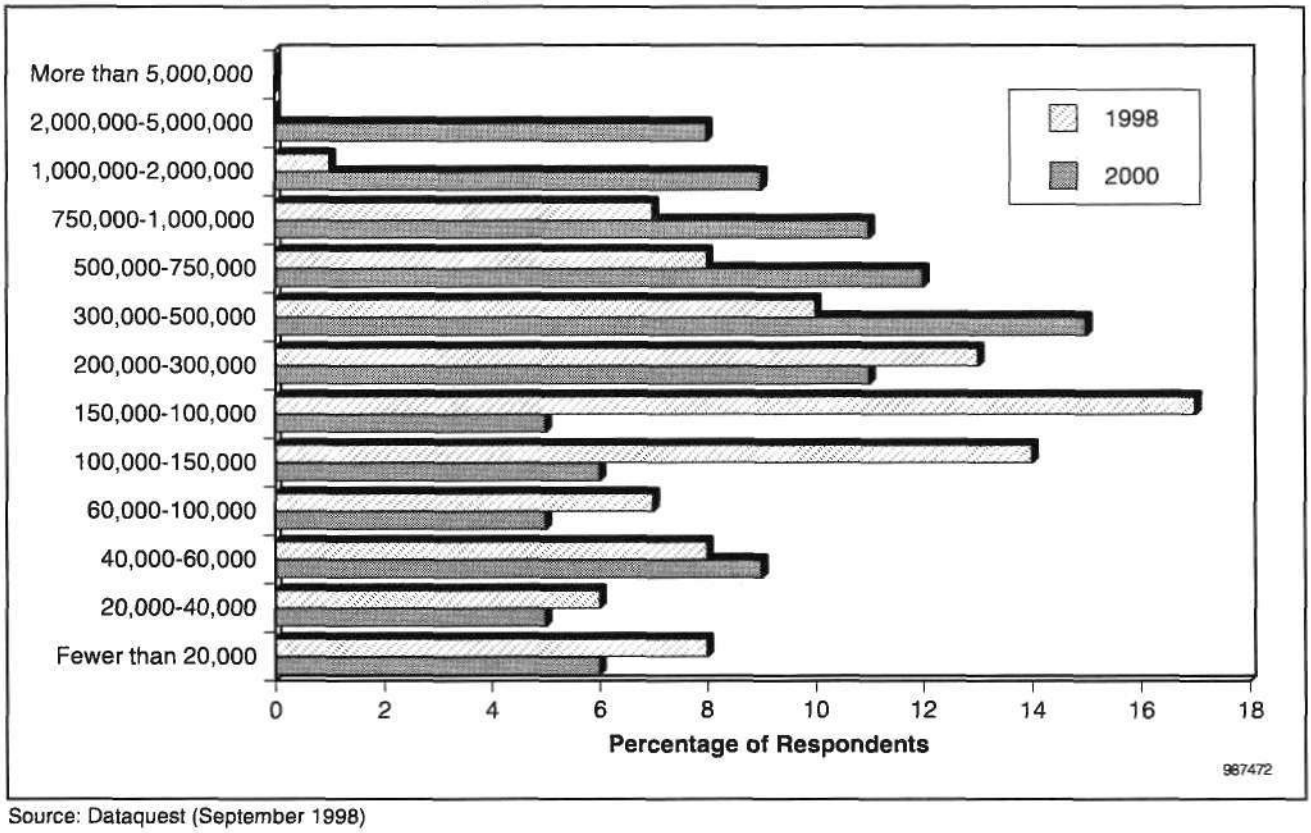
Cell-based gate counts are shown similarly in Figures 3-4 and 3-5. The median cell-based design in 1998 will use roughly 180,000 logic gates. Transistor gate geometries of 0.25-micron and below will become the mainstream for designers by 2000, with each generation providing a quantum leap in design capability (assuming that the design methodology improvements keep pace). As such, the median gate count will increase to about 340,000 logic gates by 2000. The maximum design size will continue to skyrocket—as the 0.15-micron and finer products become available, more than 30 percent of designs are predicted to break the 1,000,000 barrier in 2000.

Figure 3-3
Gate Array Design Starts: Maximum Gate Count



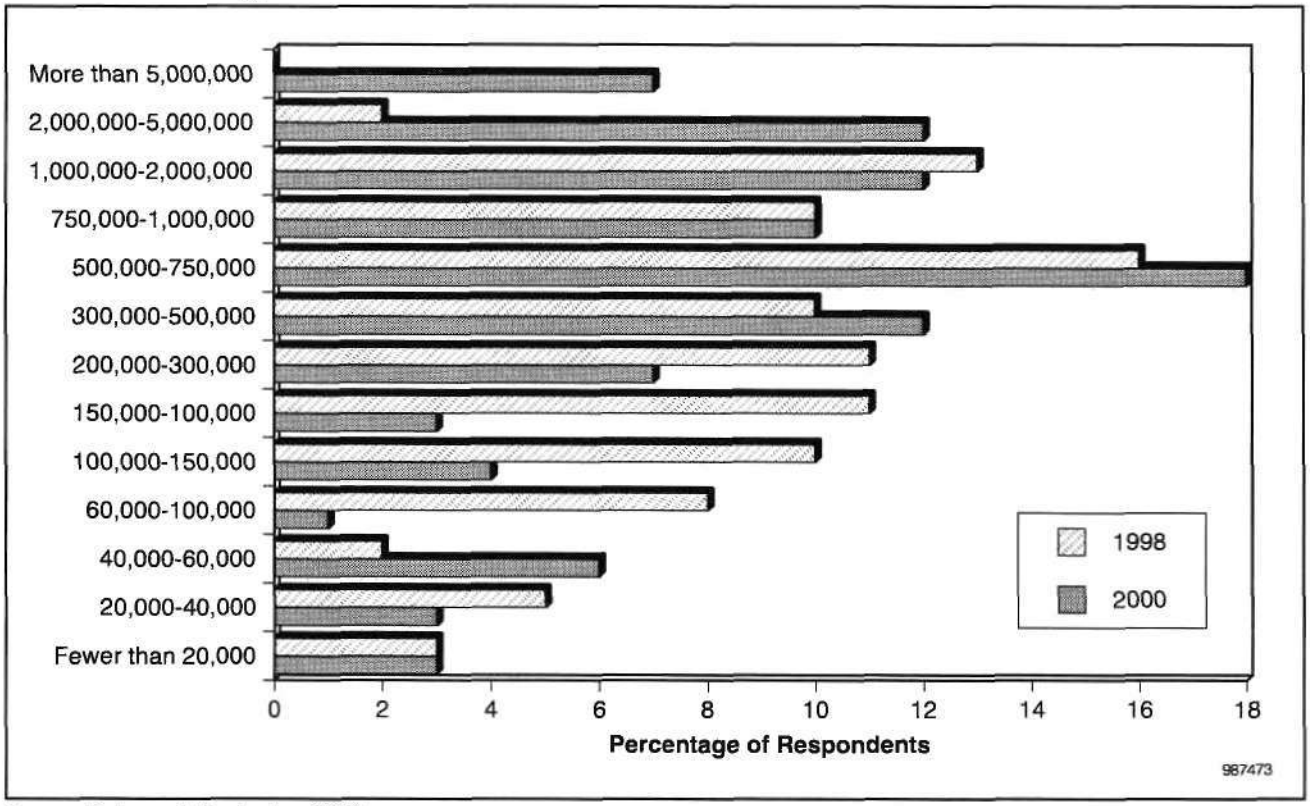
Source: Dataquest (September 1998)

Figure 3-4
Cell-Based Design Starts: Average Gate Count



Source: Dataquest (September 1998)

Figure 3-5
Cell-Based Design Starts: Maximum Gate Count



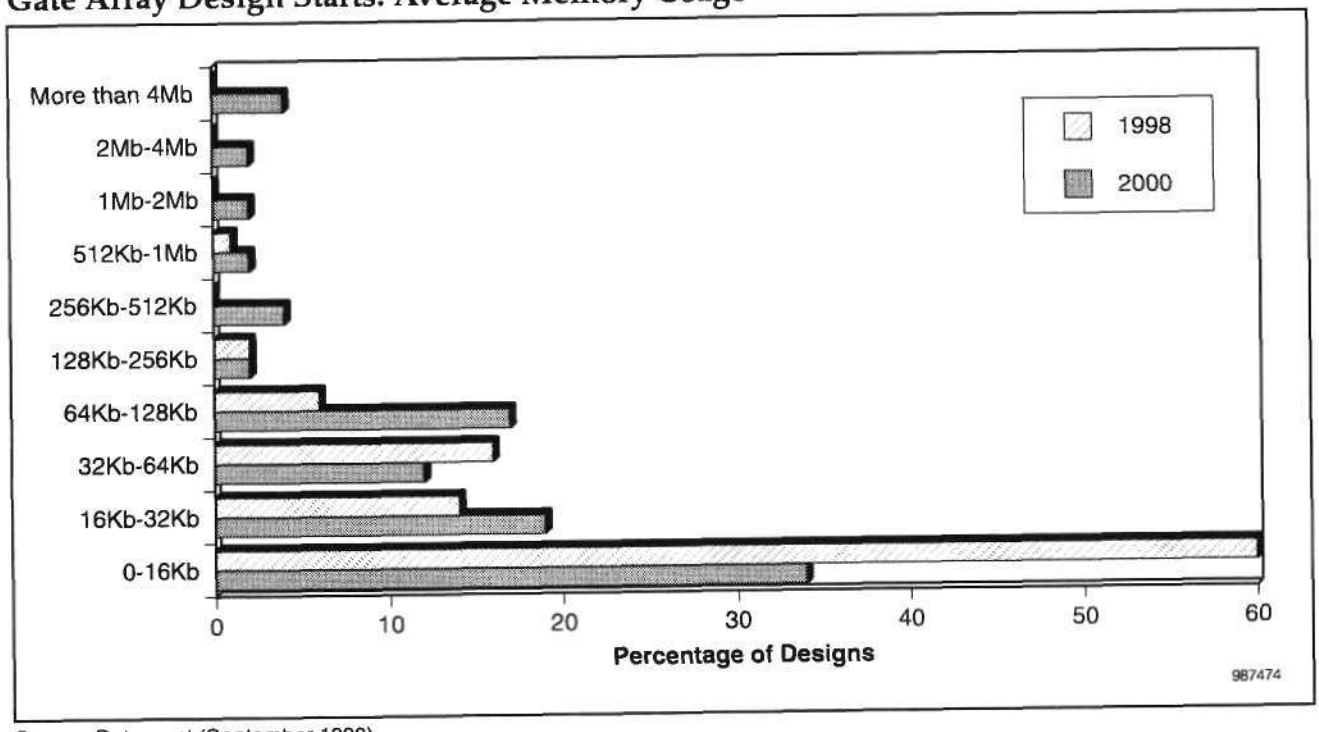
Source: Dataquest (September 1998)

ASIC Memory Usage

The past year has seen a large increase in the number of ASIC vendors offering various types of embedded memory. SRAM is universal, and a large number of vendors offer embedded DRAM products even though the market for such technology has yet to really take off. There are even several vendors with the ability to embed flash memory, although like DRAM the majority of embedded flash applications are still in the future. Not surprisingly, the memory content of the typical gate array is relatively small. Building large blocks of metalized SRAM is very inefficient. Figure 3-6 details the average memory usage in gate arrays, and Figure 3-7 shows the maximum. In 1998, well over one-half of the gate array design starts had less than 16Kb of memory. Although the content is expected to increase, the majority of gate arrays will still have under 32Kb in 2000. On the high side, a surprising number of designers (although vastly in the minority) claim to be interested in using over 256Kb; these clearly refer to embedded arrays for any reasonable die size.

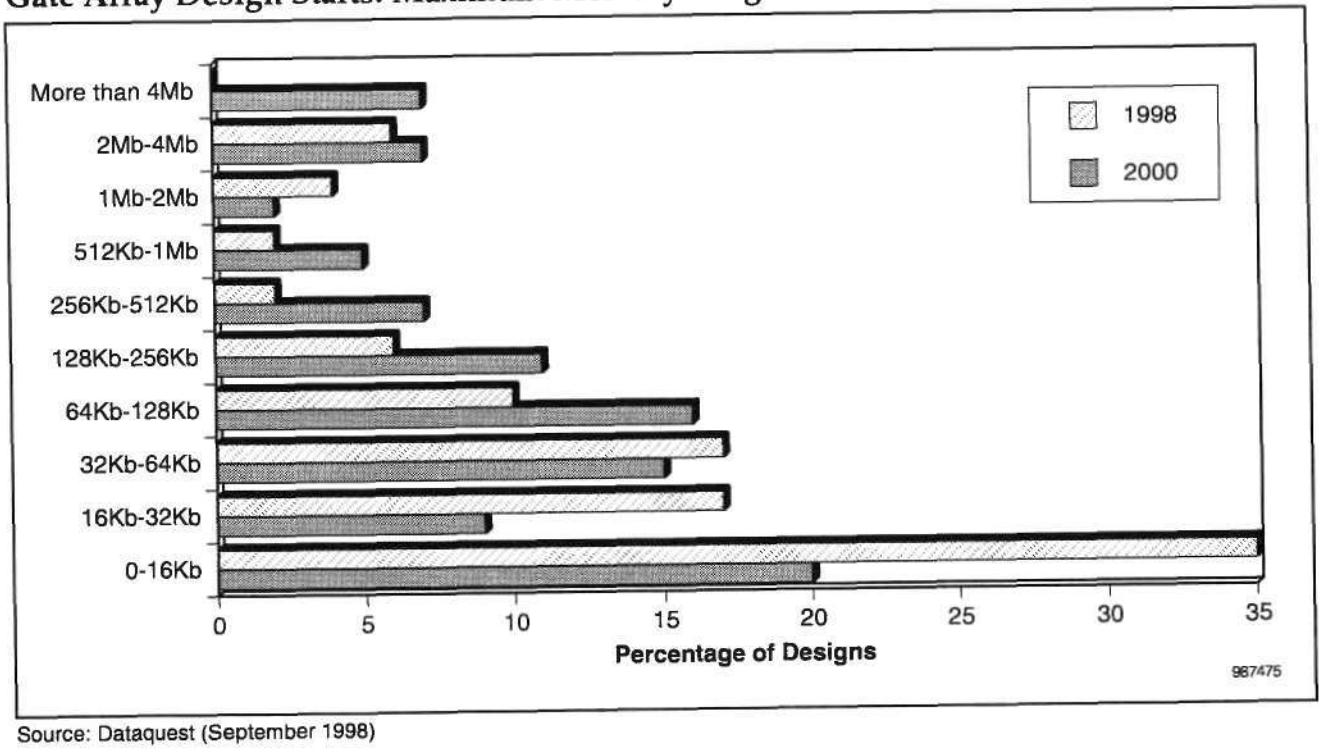
When designers do need to incorporate substantial amounts of memory, cell-based ASICs are the vehicle of choice. Figures 3-8 and 3-9 show the average and maximum memory content in cell-based ASICs. Although one-fifth of users do not use much embedded memory, more than one-half of the designs use more than 64Kb and almost one-third more than 128Kb. Memory usage is expected to increase greatly, especially with the availability of embedded DRAM, with almost one-half of designers saying that the average memory content will exceed 256Kb by 2000. Again, there is a great increase in the number of designs with substantial memory. Forty percent of designers say that, as a maximum, they will have a design with more than 1Mb by 2000.

Figure 3-6
Gate Array Design Starts: Average Memory Usage



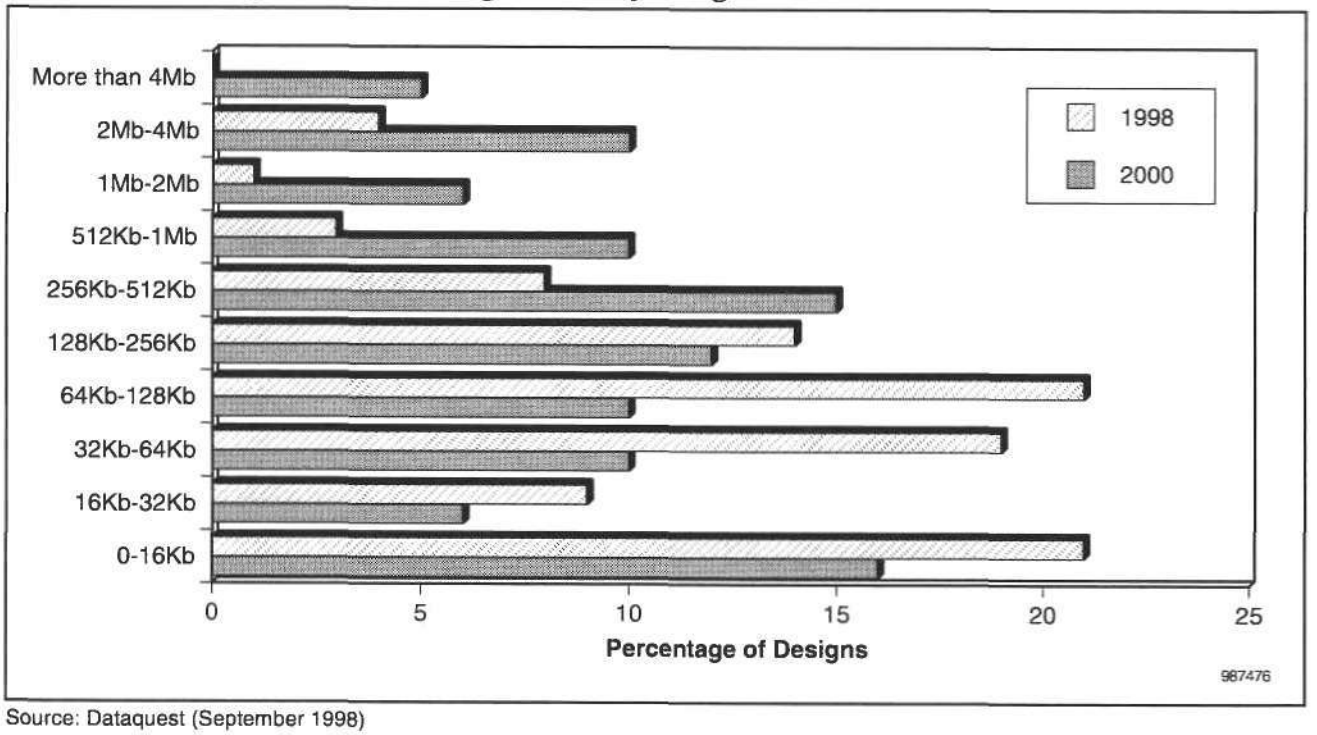
Source: Dataquest (September 1998)

Figure 3-7
Gate Array Design Starts: Maximum Memory Usage



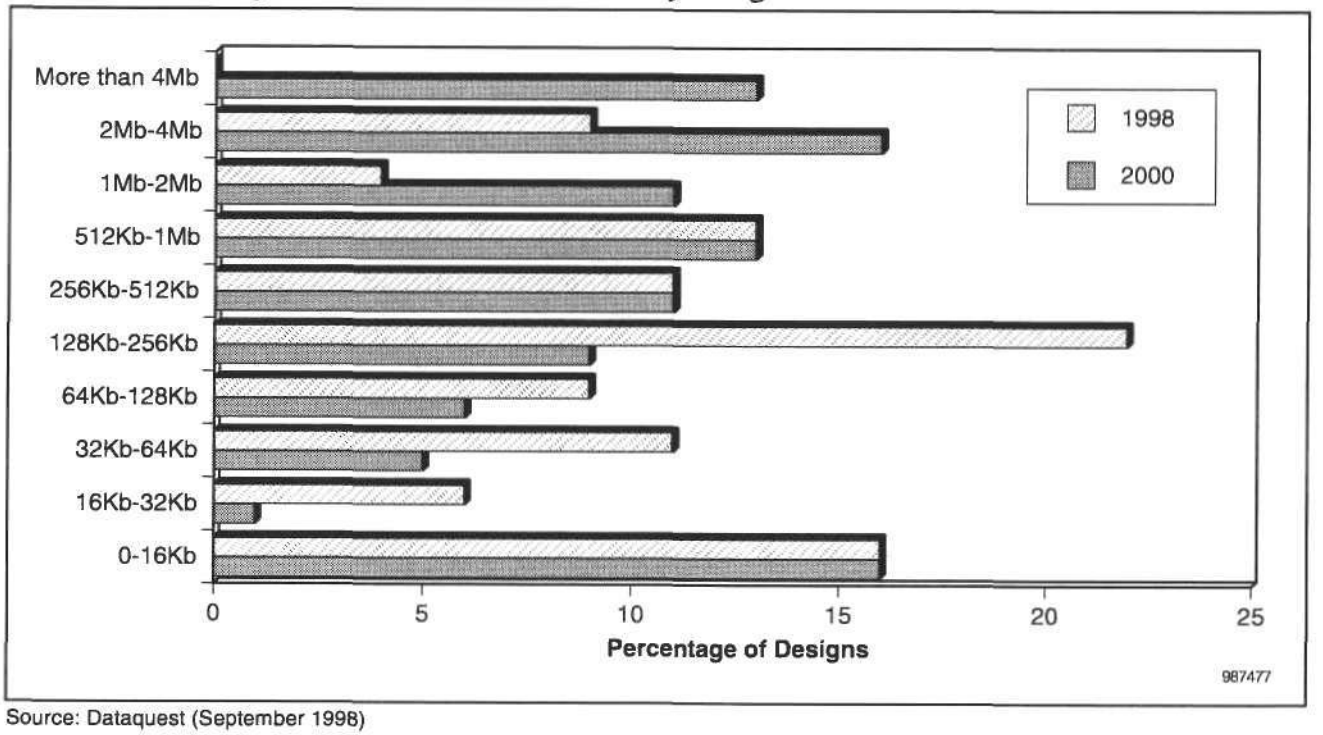
Source: Dataquest (September 1998)

Figure 3-8
Cell-Based Design Starts: Average Memory Usage



Source: Dataquest (September 1998)

Figure 3-9
Cell-Based Design Starts: Maximum Memory Usage



Source: Dataquest (September 1998)

System-Level Designs

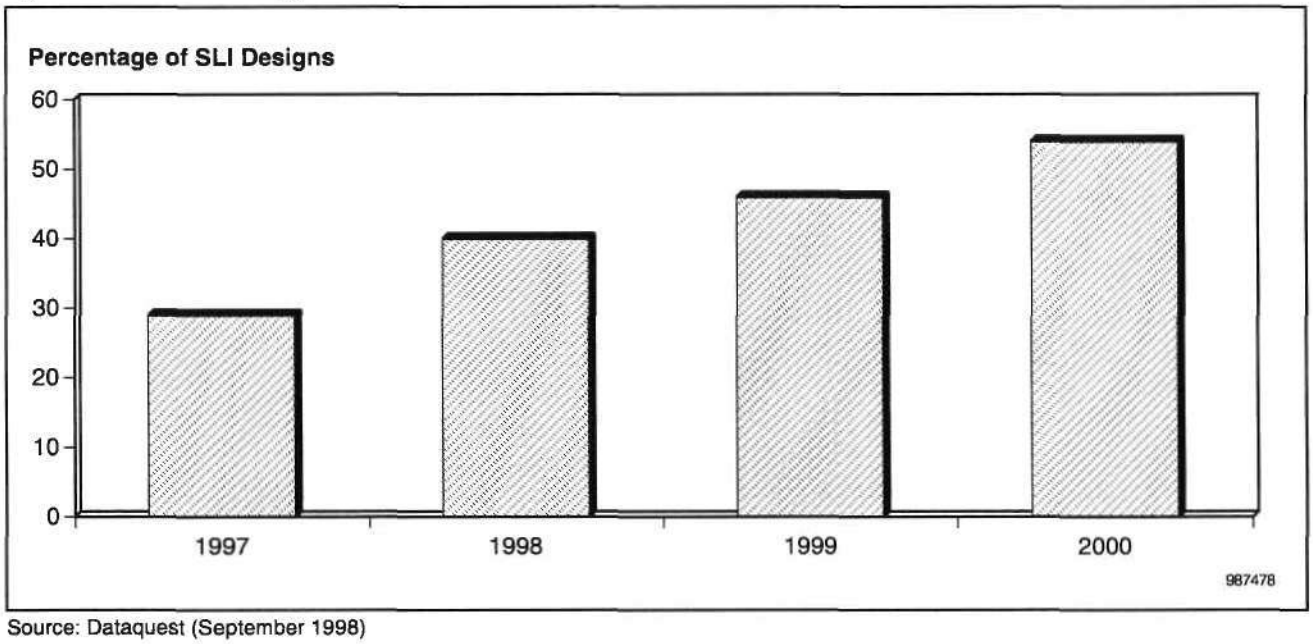
Talked about since 1990, single-chip systems took a major step toward realization in the past year. In the right application, high levels of system integration can benefit all the areas identified as major success factors: system functionality, overall cost, and, with design reuse, faster time to market. Although not every application realizes these benefits today, the number is growing. Figure 3-10 shows the trend toward system-level designs, where a system-level design has been defined as one having 100,000 or more gates of logic, embedded memory, and an embedded processor (either a microprocessor, digital signal processor [DSP], or fixed-function processor such as MPEG).

Users expect the number of SLI designs to increase rapidly. Although the growth is slowing somewhat on a percentage basis, more than 50 percent of designs will qualify as "system-level" by 2000. It must be acknowledged that part of the reason for this growth is the current SLI definition. In particular, the 100,000-gate limit is no longer representative of the high end (in fact, as discussed earlier, it is well below the average) and as such needs to be re-evaluated for future surveys.

ASIC Core Composition and Embedded Features

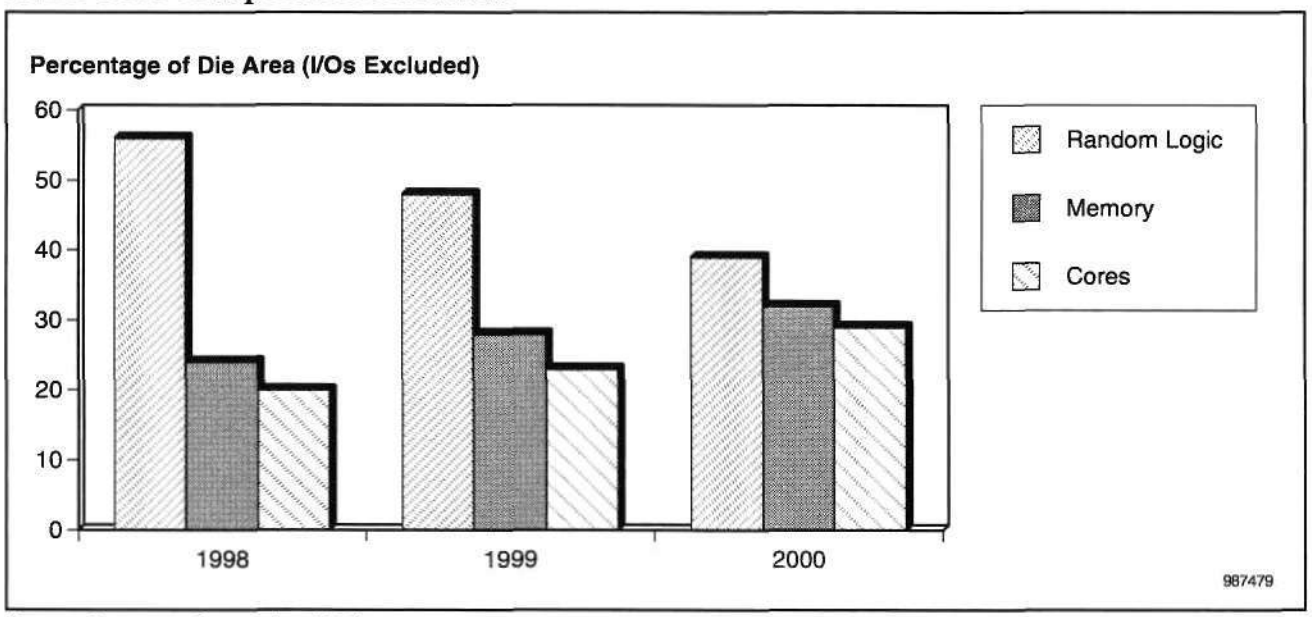
The manufacturing sweet spot for silicon has remained fairly constant over the years, with the most efficient die size at about 6 to 10mm per side. This range produces economical yields for a fairly mature process technology, a reasonable number of dice per wafer, and a good ratio of core area to I/O area. The composition of the core area of the die, however, is changing significantly. A few years ago, the core contained only logic elements (some of which were used to build memory blocks); around 1990, dedicated SRAM was incorporated. Now, system-level macros (also known as "intellectual property [IP] cores") add a third type of component to the functional area of the die. Dataquest asked users about the makeup of existing and future designs, with the results found in Figure 3-11.

Figure 3-10
System-Level Design Starts



Source: Dataquest (September 1998)

Figure 3-11
ASIC Core Composition Breakout



Source: Dataquest (September 1998)

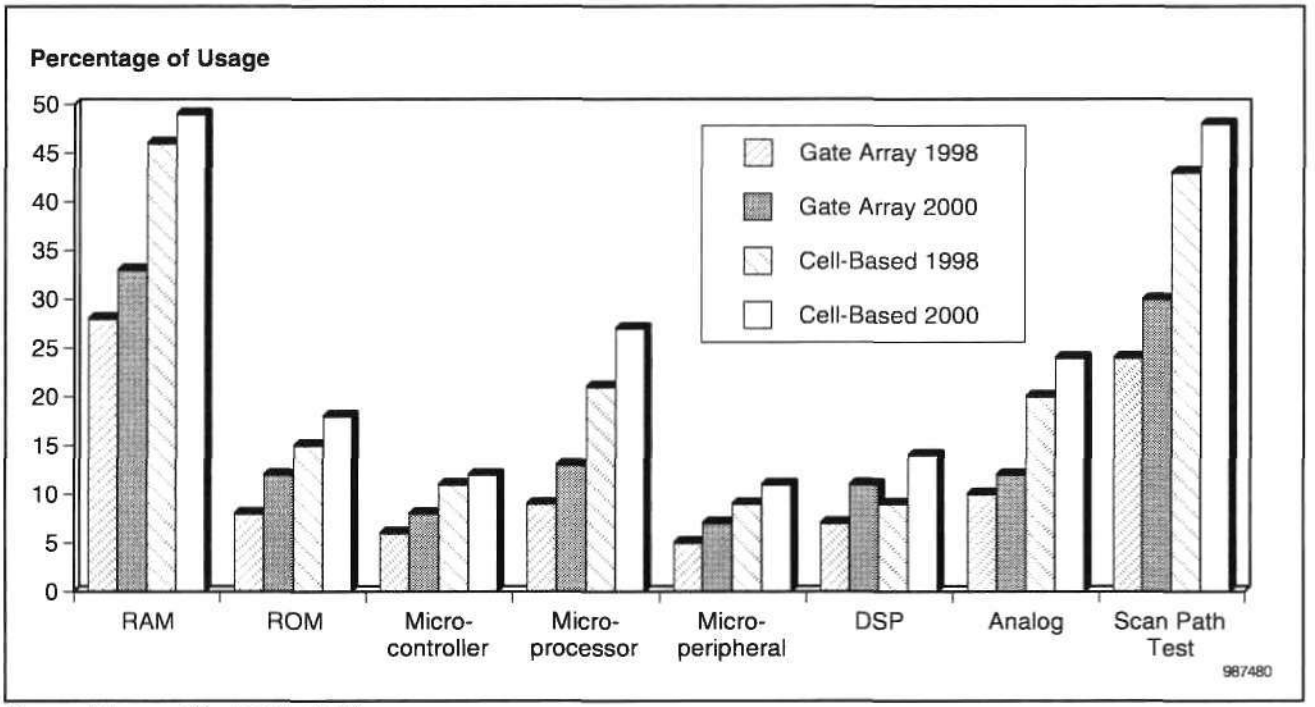
Memory usage continues to increase. As new types of memory become available on-chip, the move to SLI includes a greater proportion of the die area allocated to memory. Growing even faster is the area taken by IP cores, representing almost 30 percent of the die area by 2000. Part of the reason for the decrease in random logic area is that, while ASIC content is increasing, designer productivity is not keeping pace, and the only way to build parts in the manufacturing sweet spot is to incorporate additional, predesigned capabilities.

As a greater percentage of these IP cores are developed by third parties, the ASIC designer contributes proportionately less value to the chip. The ASIC vendor and other contributors of intellectual property will capture more of the end-system price through higher margins on the ASIC. However, the majority of IP cores today, with the exception of microprocessors and DSPs, are typically interface standards such as Peripheral Component Interconnect (PCI). As a commodity, this type of core captures very little of the intellectual content of the chip.

The trend toward specific embedded functions is sharply up in almost every case. In the survey, Dataquest asked users whether various components are used in a system. The results for overall embedded function usage are detailed in Figure 3-12. These results are further broken down into microprocessor usage (shown in Figure 3-13), DSP usage (Figure 3-14), and memory types (Figure 3-15).

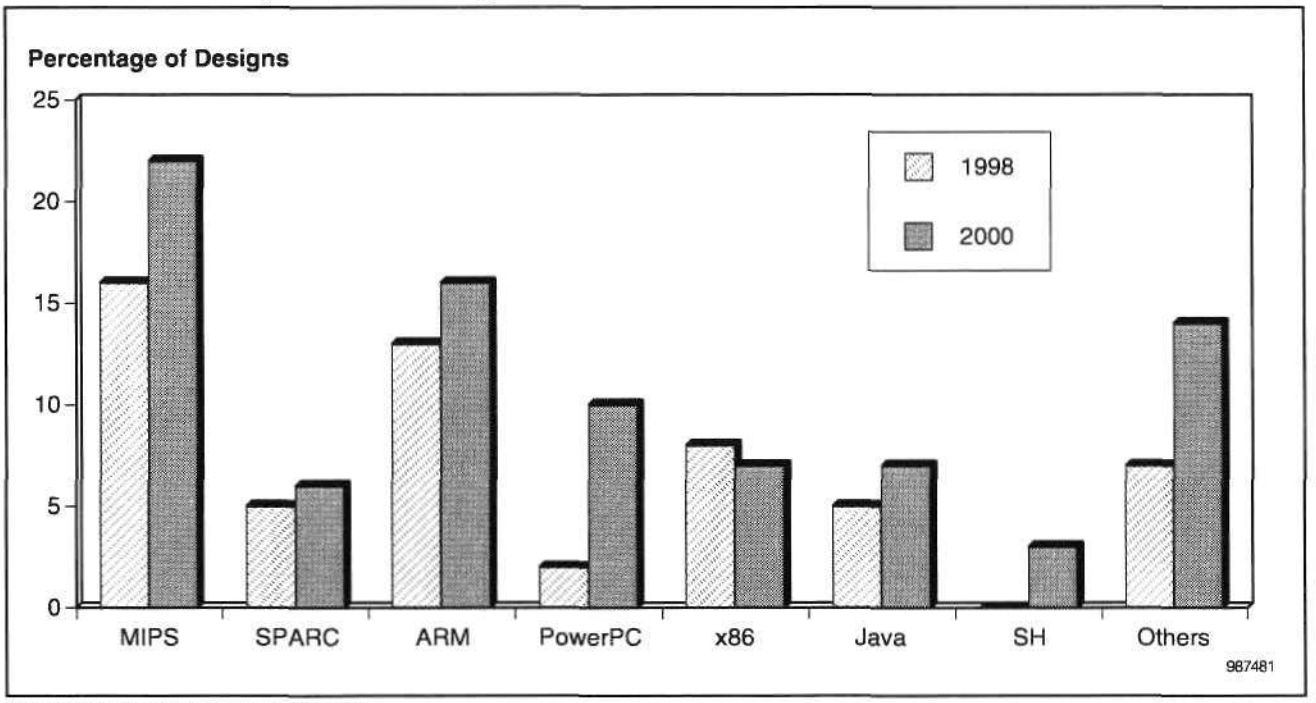
Of the embedded microprocessors, the most successful to date is the ARM, although MIPS currently generates slightly more revenue because of its use in the phenomenally successful video game market. There are about 30 licensees, and the ARM is proving very successful in portable applications, from cellular phones to personal digital assistants, because of its low power consumption. Most other processors, although gaining licensees and growing in usage, still lag behind ARM and MIPS.

Figure 3-12
Embedded Function Usage



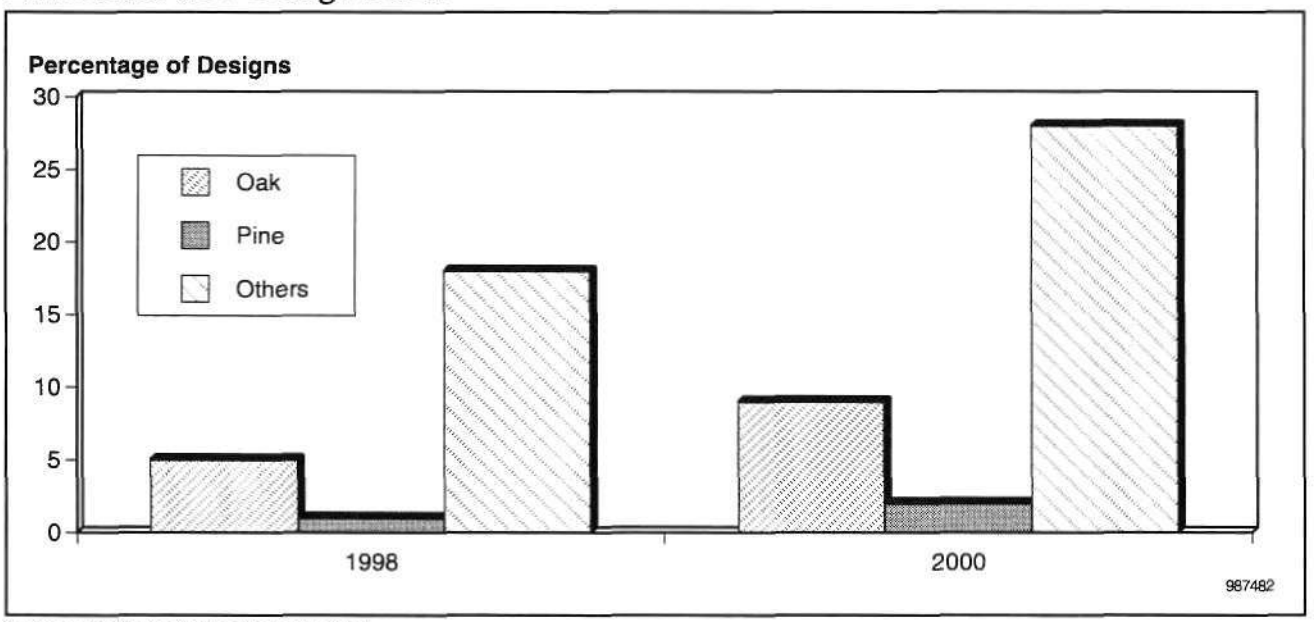
Source: Dataquest (September 1998)

Figure 3-13
Embedded Microprocessor Design Starts



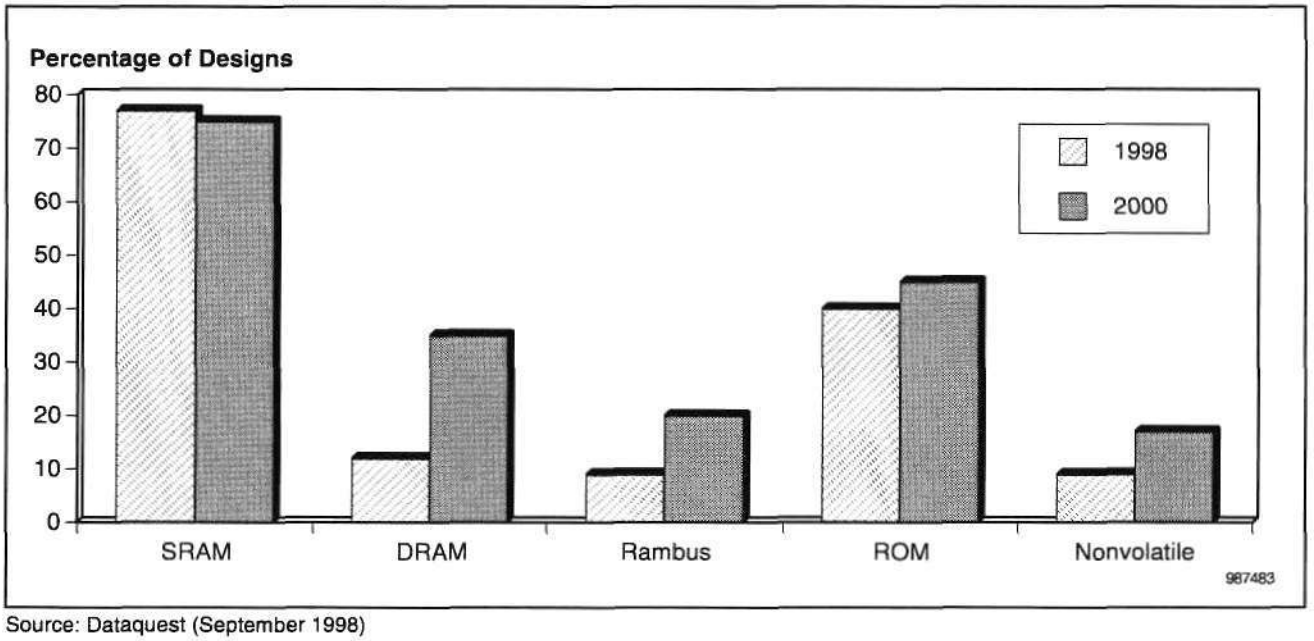
Source: Dataquest (September 1998)

Figure 3-14
Embedded DSP Design Starts



Source: Dataquest (September 1998)

Figure 3-15
Embedded Memory Design Starts



Source: Dataquest (September 1998)

DSPs are also starting to become widely available. This functional group is somewhat different from the microprocessor segment in that the leading DSPs (from Texas Instruments and Lucent Microelectronics) are not available as embedded cores from multiple vendors. So far, the only widely available embedded DSPs are the Oak and Pine cores from DSP Group (although there are some relatively new competitors, such as Siemens' Carmel) ; whereas these are now used in about 6 percent of the design starts, users indicate that the two will be used in more than 10 percent of ASIC design starts by 1999, still lagging the single-source DSPs.

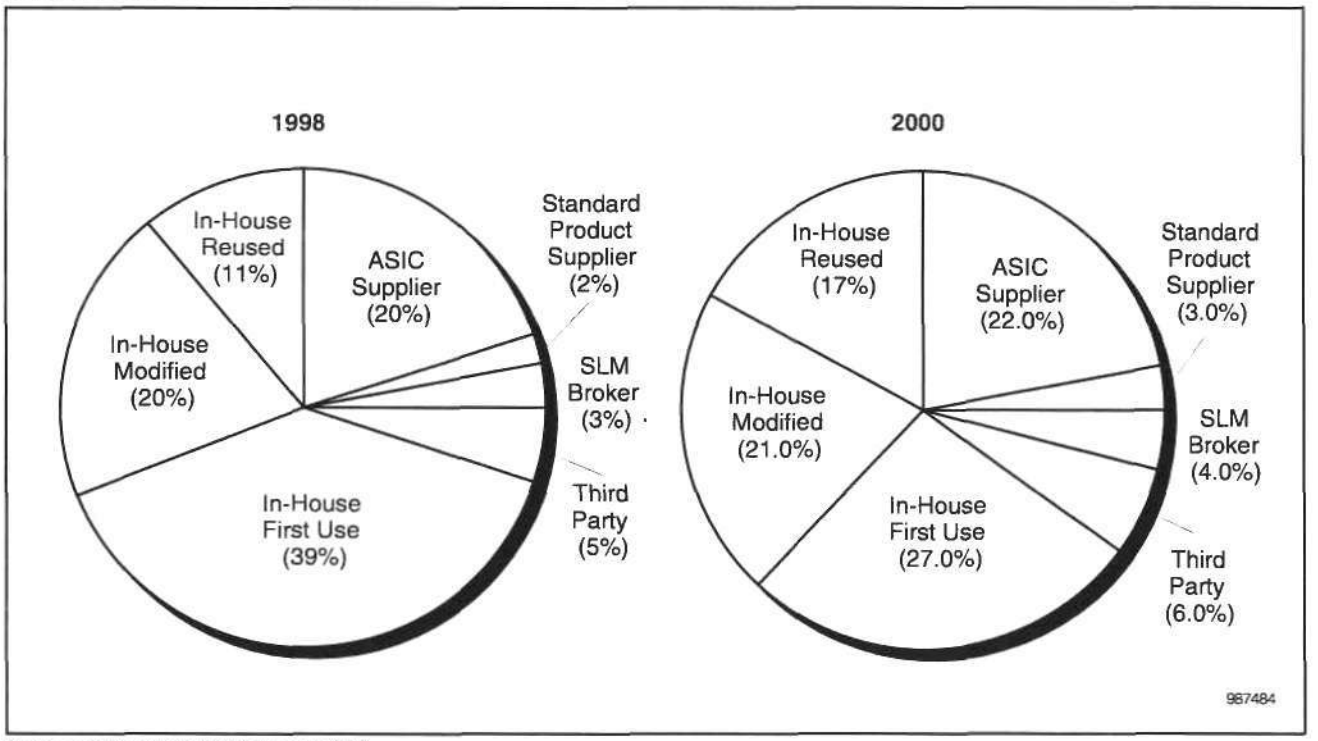
Dataquest also asked users about their plans for embedded memory. SRAM has been available for a number of years, and this availability is reflected in the very high usage percentages. Note, however, that SRAM usage appears to be static (pun intended), and that DRAM usage is skyrocketing; within a few years, most large memory blocks (over 2Mb or so) will be implemented in DRAM. In the past year, several major ASIC vendors have announced embedded DRAM capability, and numerous others appear to be on the verge. Some very hot applications markets, such as graphics controllers, disk drive controllers, and LAN switches, benefit from embedded DRAM, and within a few years, embedded DRAM will be a required feature for a vendor wishing to participate in these markets. It must be noted that with the continuing free fall in standalone DRAM prices, applications driven primarily by cost will be slow to move to an embedded DRAM solution.

Functional Block Sources and Formats

There is a scramble for both OEMs and third-party vendors to stake a claim to the high-value part of the silicon real estate. Dataquest asked users their sources for system-level macros; the results are presented in Figure 3-16. The percentage of embedded system-level macros from in-house sources remains about constant at 69 percent in 1998 and 65 percent in 2000; however, the number of functional cores being reused (rather than newly developed) is increasing substantially. This change follows the need to get products to market quickly with scarce engineering resources. ASIC vendors and other system-level macro suppliers continue to have about one-third of the market, with little shifting of relative positions. The battle for control of the value-added portion of the ASIC is clearly being fought hard.

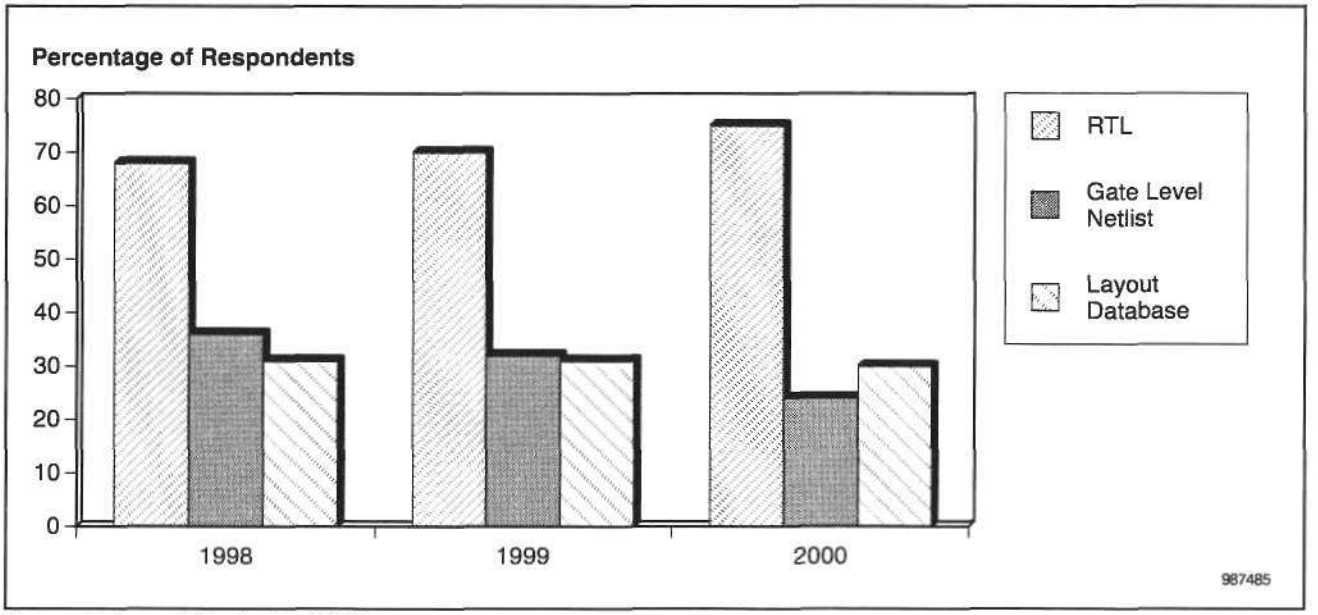
The preferred format of these functional blocks still remains RTL, with more than two-thirds of the survey respondents using at least one block in this form. Figure 3-17 details the user's choice of block format. RTL and gate-level implementations are "soft blocks," where only the block functionality is determined. Although this arrangement allows for rapid migration of the system-level macro from one generation of process technology to the next (or even from one ASIC manufacturer to another), it may be difficult to maintain performance as the layout varies. It is somewhat surprising that the layout format for system-level macros, sometimes known as "hard macros," is not growing from 30 percent. As hard implementations become more widely available, this number should increase.

Figure 3-16
Functional Block Sources



Source: Dataquest (September 1998)

Figure 3-17
Functional Block Format



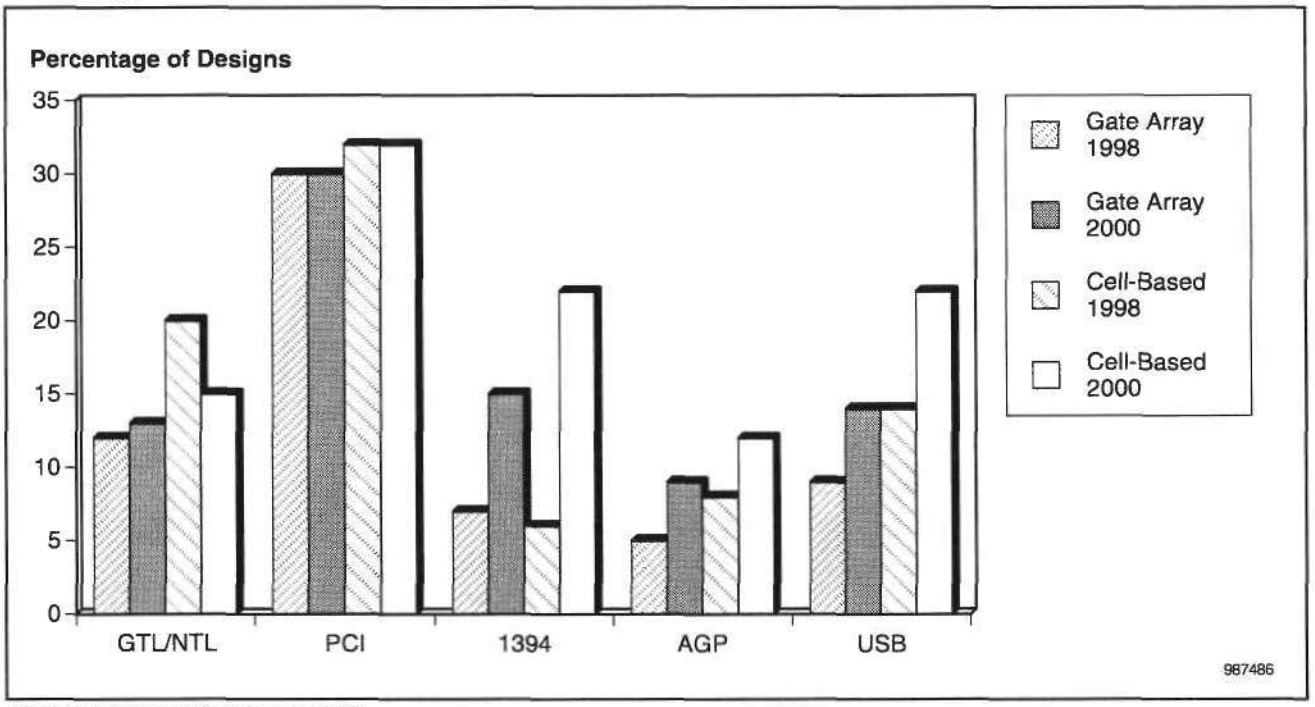
Source: Dataquest (September 1998)

I/O Trends

Aside from IP cores, one area where ASIC vendors seek to differentiate themselves is through their I/O offerings. Dataquest asked users about I/O usage and plans, and the results are found in Figure 3-18. Traditional low-voltage transistor-transistor logic (LVTTL) I/Os are still the most commonly used by a great margin; however, the last few years have seen an explosion of new I/O types. High-speed I/Os such as low-voltage differential signal (LVDS) ensure that system bus speeds do not become a bottleneck and can reduce die size in some cases by moving from a parallel to serial I/O scheme. New mainstream I/Os such as PCI, universal serial bus (USB), and IEEE 1394 are used to meet industry-standard requirements in high-volume applications.

The more mainstream I/Os are typically used in PCs and ancillary consumer products such as digital video still cameras. Figure 4-14 details the user demand for these I/Os, which include PCI, SCSI, AGP (the new graphics standard used in Pentium II systems), USB, and 1394. PCI is clearly the leader in this group, with users anticipating PCI in more than 30 percent of cell-based design starts in 1998. All of the others lag, but it should be remembered that most of these standards are just beginning to be incorporated into the end systems. Use of these I/Os should accelerate rapidly, as is confirmed by the survey.

Figure 3-18
I/O Usage in ASICs



Source: Dataquest (September 1998)

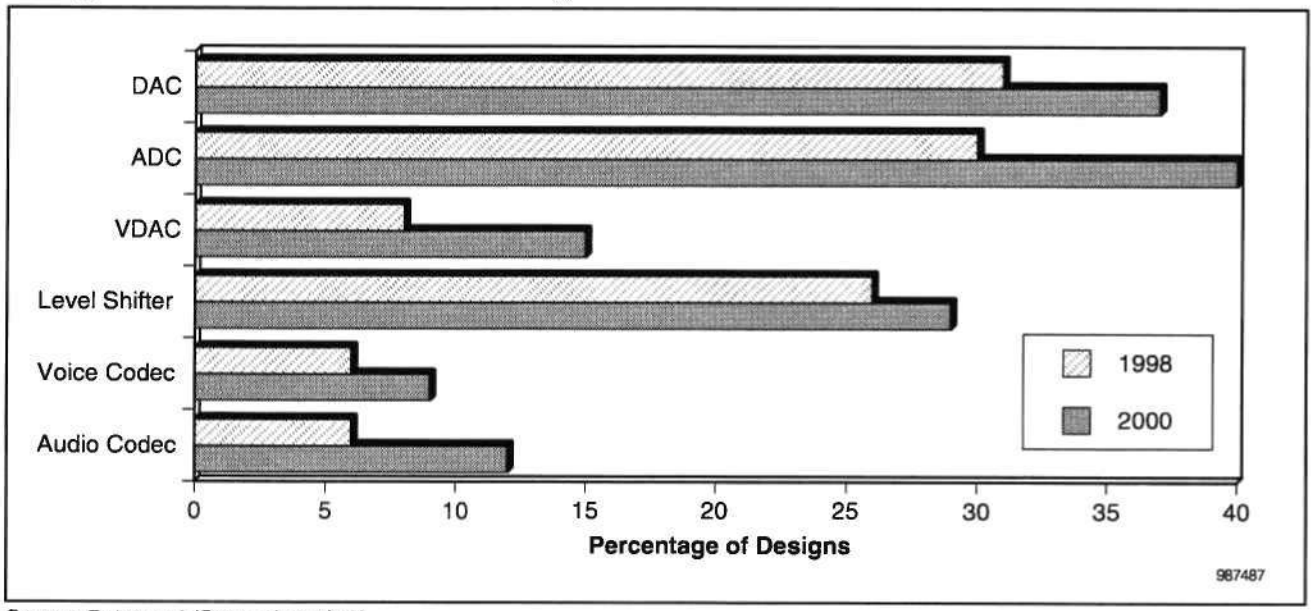
Analog Functions

As more parts of a system are incorporated onto the ASIC, analog components are beginning to join the digital logic. By 2000, about one-half of users said that some analog functionality was or will be incorporated on-chip. There are several ways to incorporate analog functions onto a digital ASIC, although each involves trade-offs between functionality and cost.

- The silicon process can be enhanced to build precision analog components (resistors or capacitors) on-chip. This enhanced process brings a high level of analog functionality onto the ASIC, essentially equivalent to off-the-shelf standalone analog components. However, the more complex process adds cost to the entire die—both the digital and the analog portion.
- It is possible to build analog components using a logic-optimized silicon process. This maintains the existing wafer cost, but the analog components are somewhat restricted in functionality (less resolution, for example, in a digital-to-analog [D/A] converter).

A broad range of analog functions can be incorporated into an ASIC. Figure 3-19 shows the user demand for these functions in 1998 and 2000.Toward 2000, users are expecting to put some type of analog functions on a majority of designs, with converters (digital-to-analog and analog-to-digital) being especially common. The system goal is becoming "convert to digital as soon as possible and to analog as late as possible," moving system-level ASICs ever nearer to both the front and back ends of a signal-processing chain. Some applications, particularly early movers to system-level integration that have significant analog requirements, show an even faster move to embed the analog functions. An example is the wireless market, which requires system-level integration to reduce chip count and power consumption.

Figure 3-19
Design Starts with Embedded Analog Functions



Source: Dataquest (September 1998)

Voltage Trends

The 5V power supply was the only game in town for a number of years. Now, however, 3.3V systems are taking the largest percentage of design wins. Even more significant is the rapid ramp of even lower supply voltages, with 2.5V and even 1.8V and lower appearing in some systems. With ASICs, each new generation of technology is being targeted at a lower voltage for several reasons:

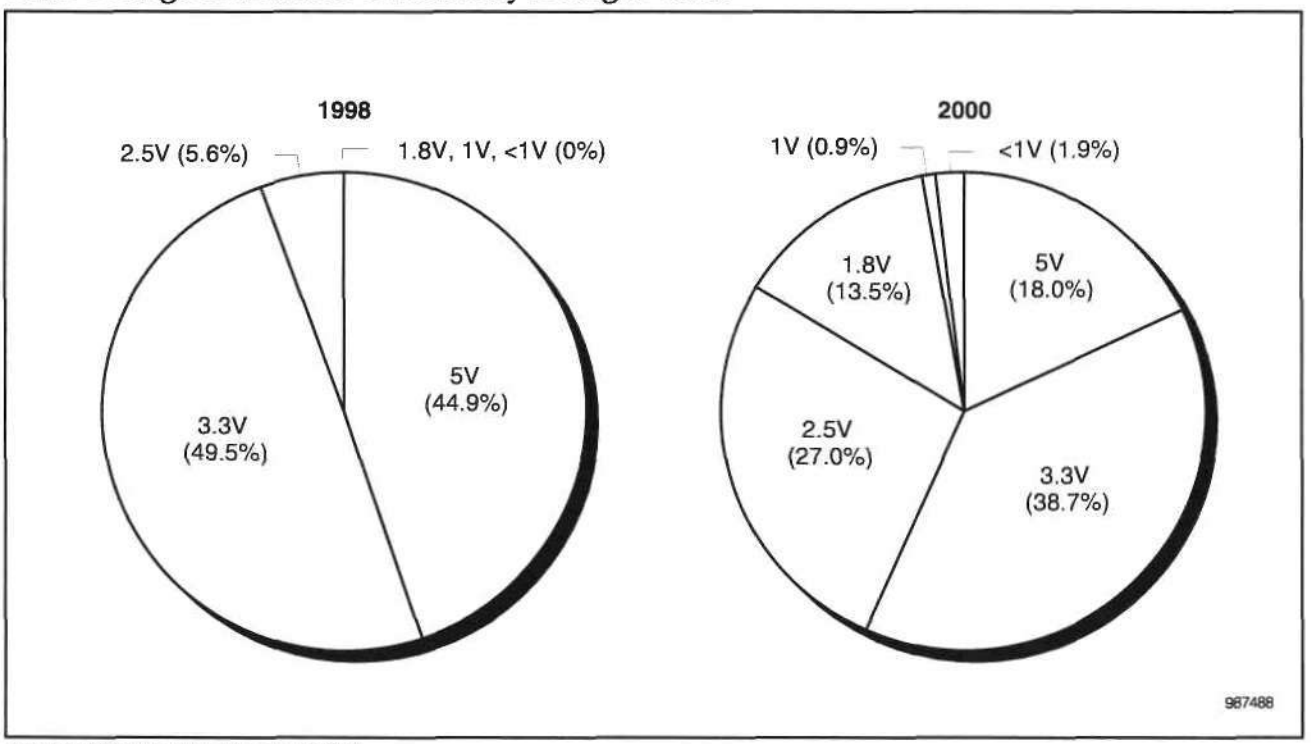
- The physical dimensions of the transistor shrink with each generation, and some of these dimensions, particularly gate oxide thickness, impose limitations on the voltage a transistor can reliably tolerate.
- For many applications, power saving is more important than an incremental performance improvement. Typically, there is relatively little performance difference between, for example, a 0.35-micron transistor operating at 3.3V and a 0.25-micron transistor operating at 2.5V, but the smaller transistor will dissipate much less power (perhaps 75 percent less).
- The highest-performance designs, such as workstations, also tend to have a high level of integration. An ASIC with 1,000,000 gates with a 300-MHz clock rate could dissipate more than 100W when operating at 3.3V but has a much more feasible power consumption at 2.5V.

Figures 3-20 and 3-21 show the core voltage trends for gate arrays and cell-based ASICs, respectively. For gate arrays, the overwhelming number of designs remain at 3.3V or 5V. This trend reflects the lag in gate array development by vendors and the concurrent move to cell-based ASIC for mainstream as well as leading-edge designs. Note that for cell-based ASIC designs in 2000, there is almost as much demand for designs at 1V and below as there is for older 5V products. As new process generations continue to be introduced at a rapid pace, this trend is certain to accelerate, with only the process attributes such as threshold voltage establishing an ultimate lower limit.

The I/O voltages are also changing rapidly, although they tend to lag the core operating voltages because new designs must sometimes interface with an existing, higher-voltage-supply system. Figures 3-22 and 3-23 detail the I/O voltage trends for gate arrays and cell-based ASICs, respectively. The news in cell-based ASIC is that 1.8V systems are expected to become relatively common by 2000, although there is still a call for support of older standards, particularly 3.3V.

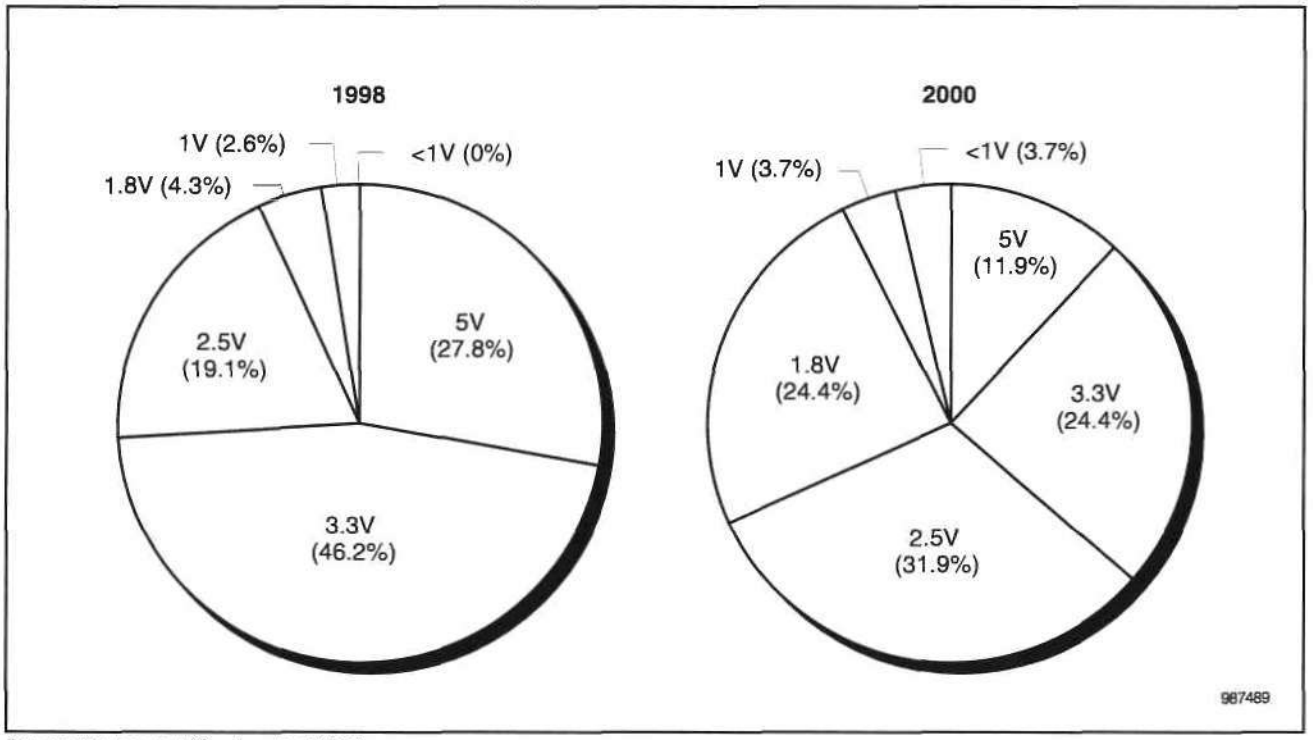
For both core and I/O operation voltages, it is clear that the era of one standard voltage is gone for the foreseeable future. This development has implications for the product life cycle of an ASIC generation—that is, there will be a long lifetime for 0.5-micron products, as very few finer-geometry transistors can support true 5V operation; the same holds for 0.35-micron products supporting 3.3V, and so on down the line.

Figure 3-20
Core Voltage Trends for Gate Array Design Starts



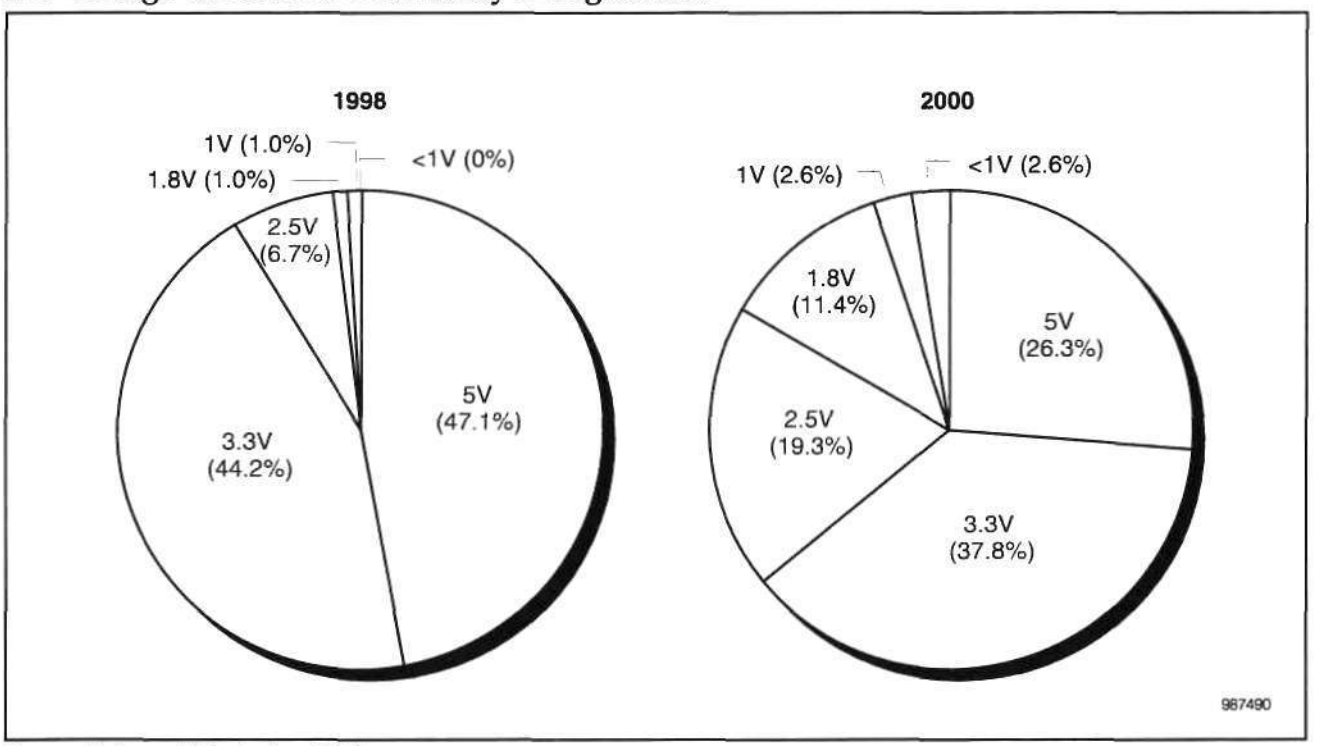
Source: Dataquest (September 1998)

Figure 3-21
Voltage Trends for Cell-Based Design Starts



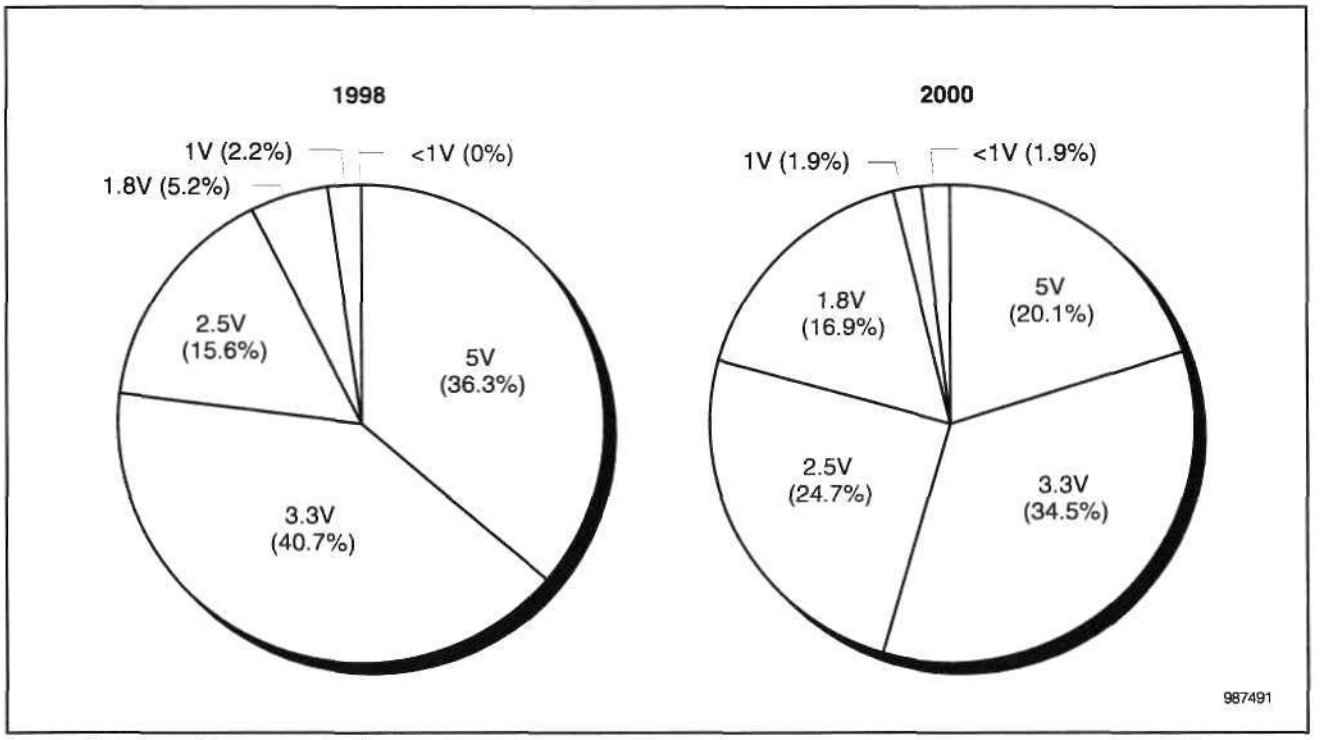
Source: Dataquest (September 1998)

Figure 3-22
I/O Voltage Trends for Gate Array Design Starts



Source: Dataquest (September 1998)

Figure 3-23
I/O Voltage Trends for Cell-Based Design Starts



Source: Dataquest (September 1998)

Clock Speeds

Not surprisingly, system clock speeds continue to climb. In 1998, vendors responded to this trend with ever more frequent process announcements, with a number of "tweaks" such as low-k dielectric materials and copper interconnect, that today are oriented primarily toward the high-end designer. For some designs, speed is the holy grail, and users cannot get enough performance. However, a great number of applications—such as the typical consumer design—only need performance sufficient to meet an industry standard such as MPEG-2 decoding; anything more is unnecessary. This accounts for performance being rated fourth out of the eight critical success factors mentioned earlier, and for the wide spread in gate array and cell-based ASIC clock speeds (shown in Figures 3-24 and 3-25, respectively). For a number of users, the performance of 0.5-micron ASICs remains sufficient, while others clamor for the latest 0.15-micron products.

ASIC Packaging

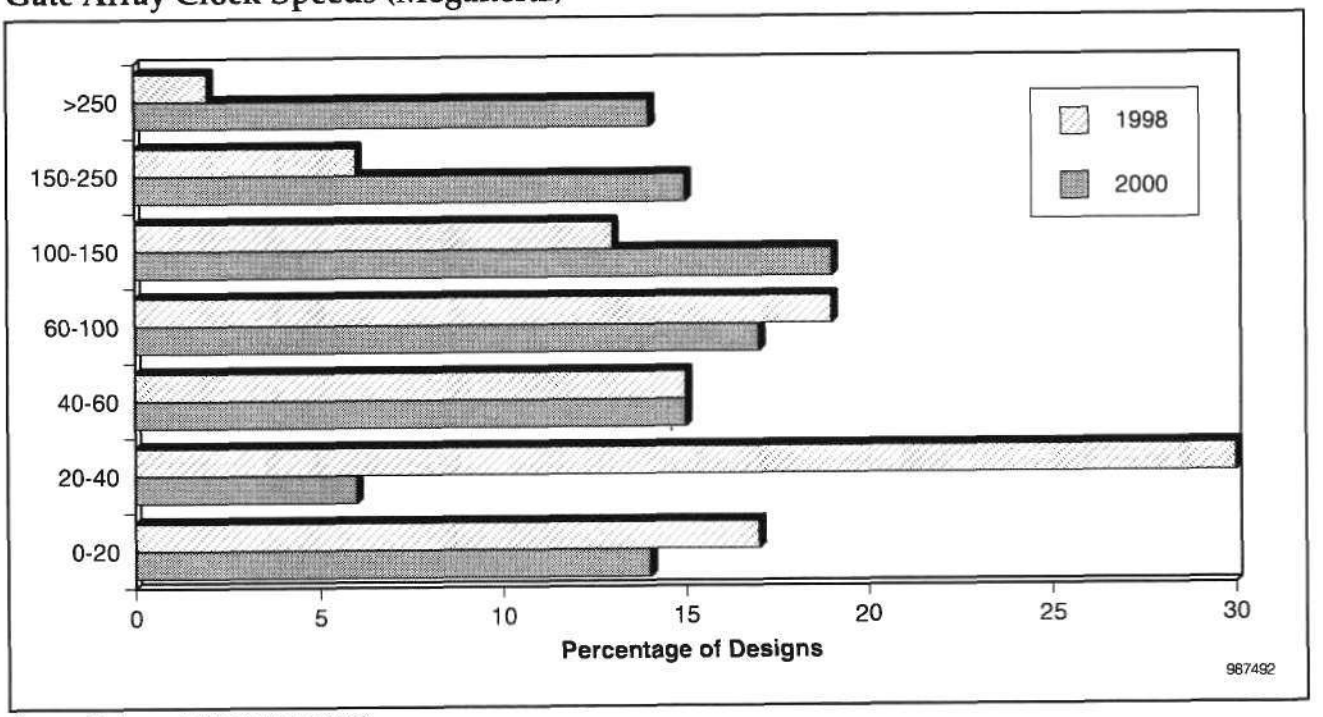
All the advances in the silicon process, design methodology, and libraries would be of no avail without equivalent advances in packaging. Figure 3-26 shows the user response to the survey. Two trends are of note, the most important being that ball grid array (BGA) will clearly eclipse PQFPs by 2000. Many vendors have qualified BGAs, which are now cost-competitive with QFPs in the 180-plus lead count segment and continue to provide a very strong cost and performance solution for higher-lead count designs. Flip-chip packages continue to gain ground as well. Cost issues are beginning to be addressed, and flip-chip packages deliver the highest levels of performance and lead counts to 1,200 pins and beyond; as more vendors introduce this technology and as advances in organic laminate and plastic flip-chips reduce the cost, flip-chip packaging will continue to grow at a rapid rate.

The average pin count of designs is increasing somewhat, but not tremendously, from 1998 to 2000. Figure 3-27 details the spread of user requirements for pin count. Although there is some increase in the high-pin count designs (particularly for those over 731 pins, at least on a percentage basis), the move toward serial I/Os versus wide parallel buses works to mitigate this increase somewhat. As with all other attributes, this one is highly application-specific, with wireless and consumer designs at the low and middle pin counts and computers pushing the high end. Substantial demand for the traditional low-pin count design remains.

Programmable Logic

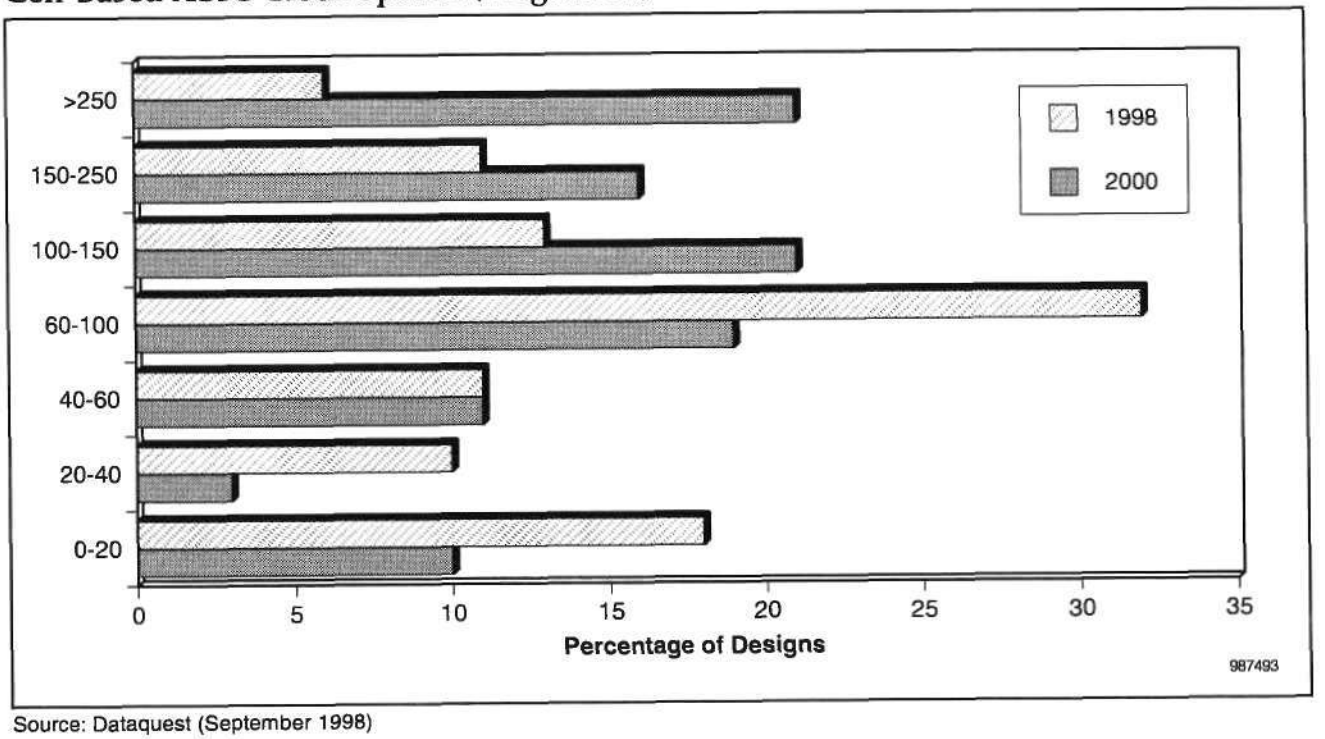
Along with the system-level integration phenomenon, the activity in programmable logic proved one of the industry's most significant aspects. In a market in which reducing time to market is one of the top three factors in the success of a design, PLDs provide instant gratification. PLDs supporting 20,000 gates and more are moving into the mainstream, and vendors talk of 1,000,000 gates in the very near future (or even now, depending on how you define a gate).

Figure 3-24
Gate Array Clock Speeds (Megahertz)



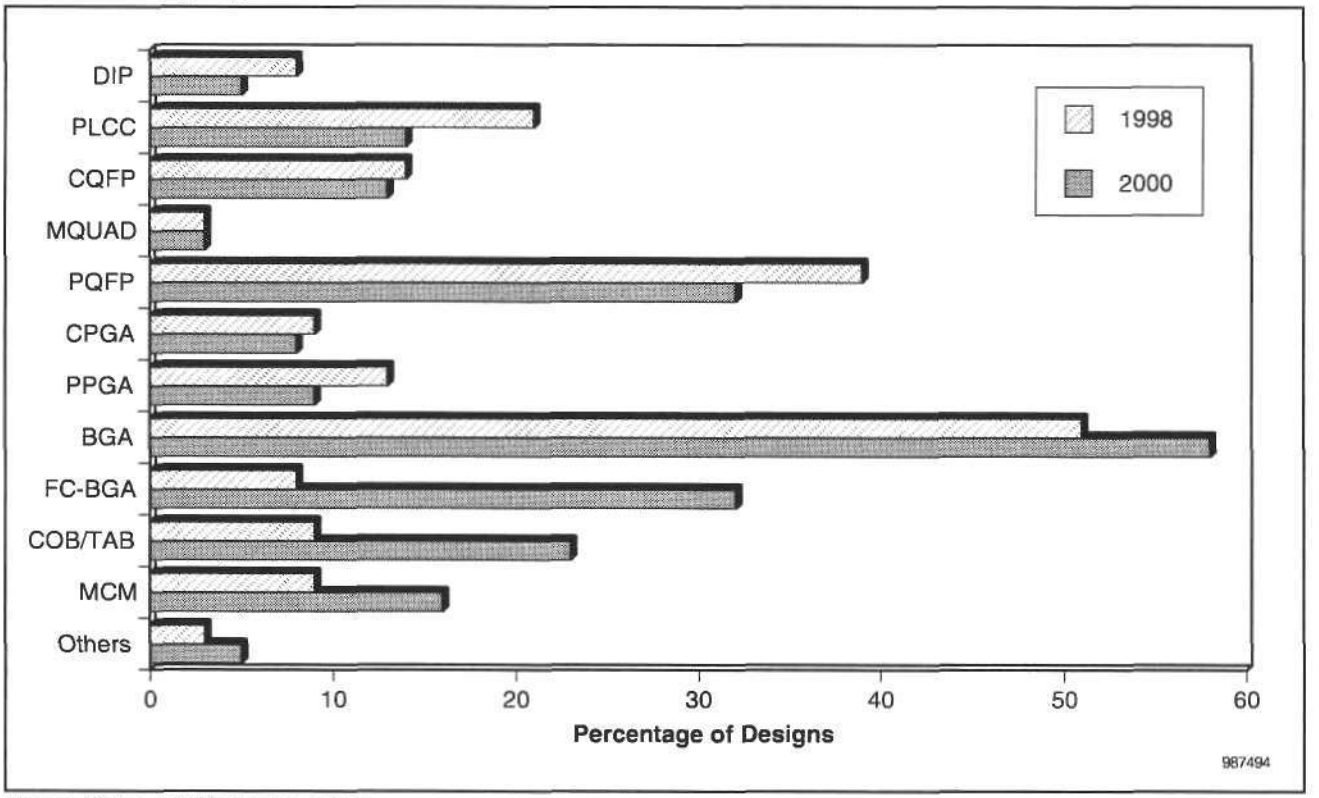
Source: Dataquest (September 1998)

Figure 3-25
Cell-Based ASIC Clock Speeds (Megahertz)



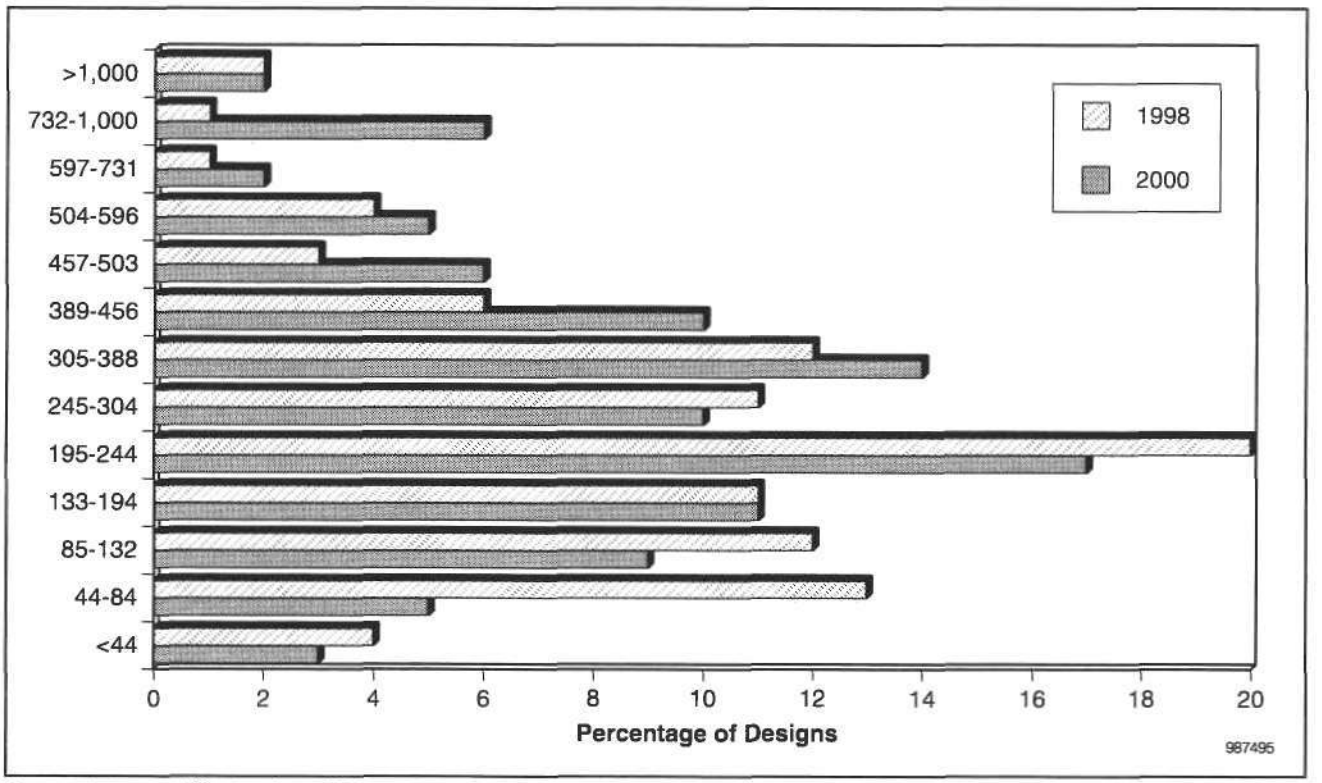
Source: Dataquest (September 1998)

Figure 3-26
ASIC Packaging



Source: Dataquest (September 1998)

Figure 3-27
ASIC Pin Count



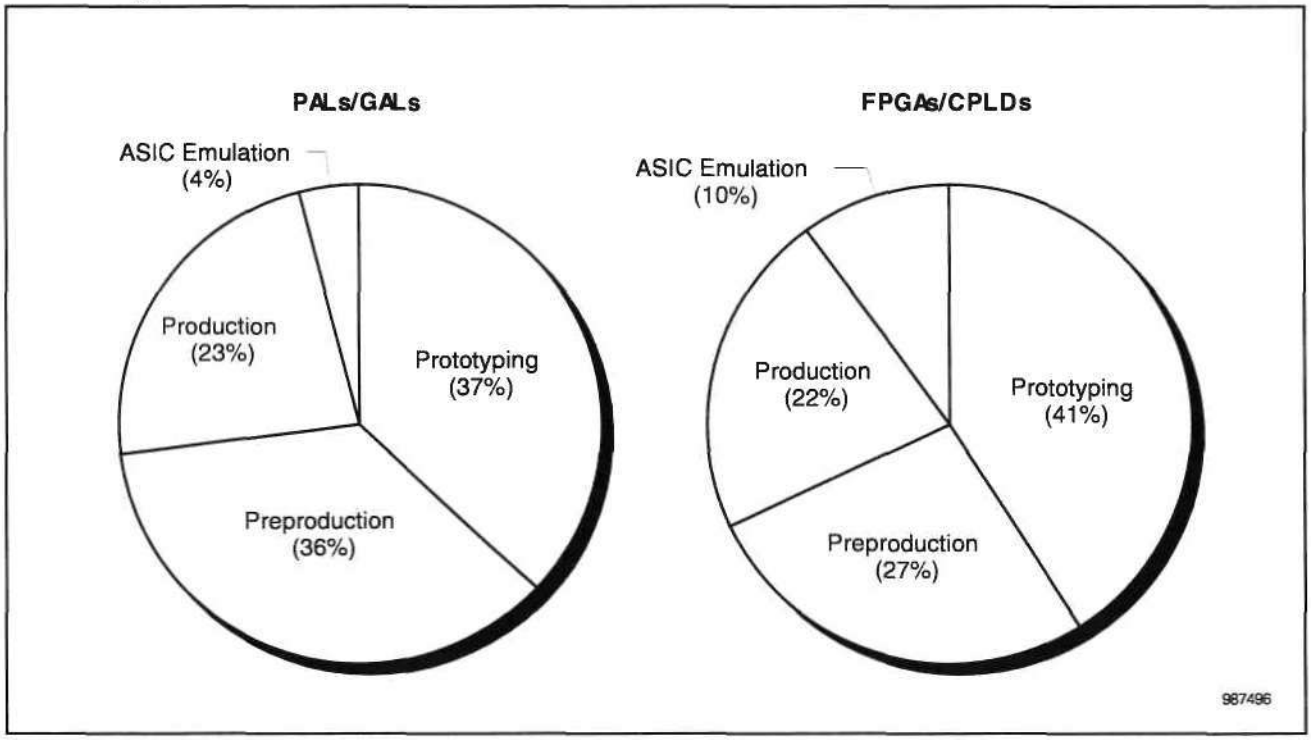
Source: Dataquest (September 1998)

PLD Device Usage

One of the major uses of PLDs is prototyping designs, where the instantaneous turnaround time is a boon to designers. Many designers plan on using PLDs only in the prototype stage, however, with a conversion to a smaller-die gate array for production volumes. Anecdotal evidence indicates that PLD conversion to gate arrays is like the weather: Everybody talks about it, but nobody does anything about it. PLD vendors continue to see production volumes of a number of designs originally slated for gate arrays.

Programmable array logic (PAL) and gate array logic (GAL), the simplest PLDs, show about an equal split in use among prototyping, preproduction, and production. Given the limited size of PALs and GALs, it makes sense that many of these designs continue all the way into production volumes. Figure 3-28 details the device usage for both PALs/GALs and complex programmable logic devices (CPLDs)/field-programmable gate arrays (FPGAs). CPLDs and FPGAs tell a similar tale, with a majority used for prototyping but still in substantial use as preproduction and production parts.

Figure 3-28
PLD Usage



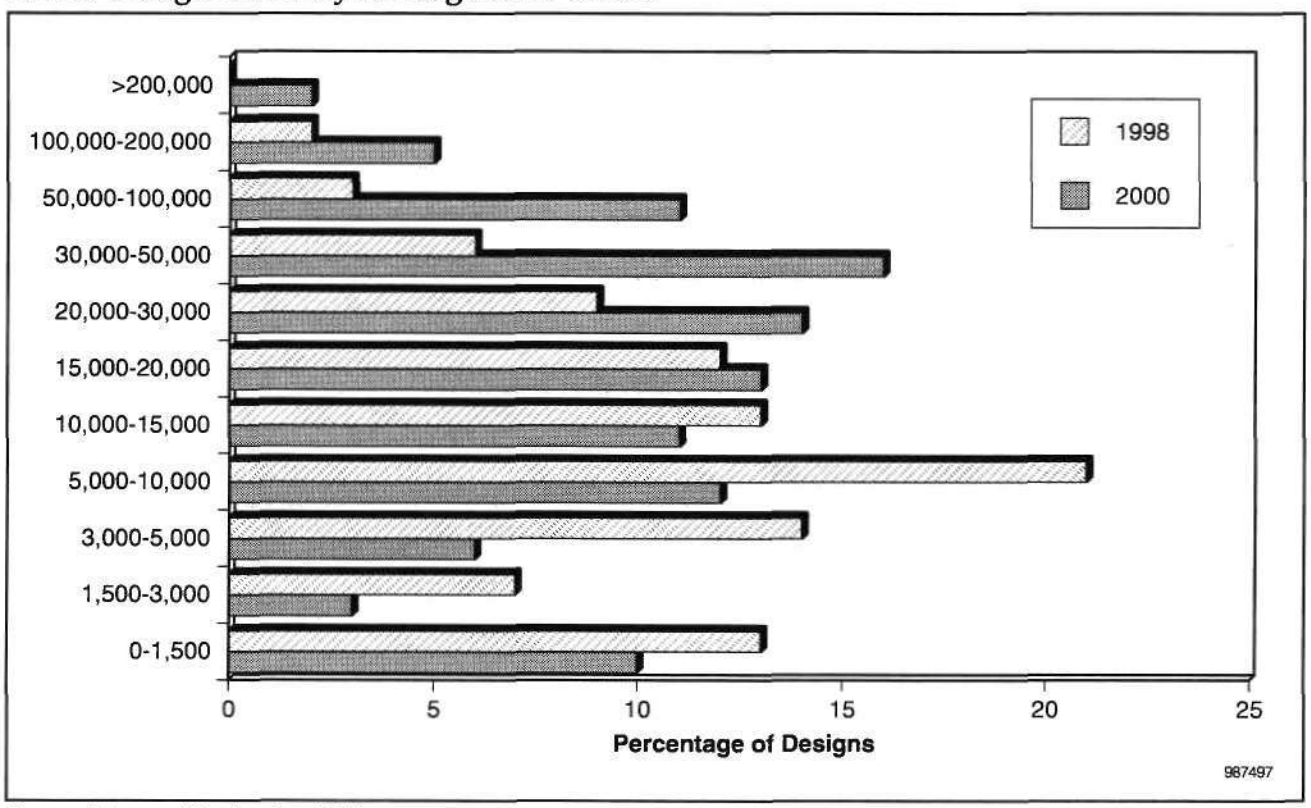
Source: Dataquest (September 1998)

PLD Gate Count

The major architectural battle in the semicustom semiconductor industry is that of high-end PLDs versus low-end gate arrays. As PLD gate counts increase, many leading gate array vendors are either abandoning the battlefield (about 10,000 to 50,000 logic gates) or are not aggressively pursing business. Dataquest surveyed users to establish their requirements for PLD gate count. Figures 3-29 and 3-30 show the average gate count for FPGAs and CPLDs, respectively. For designers pushing the envelope of technology, Figures 3-31 and 3-32 show the user's maximum gate count requirement for FPGAs and CPLDs, respectively.

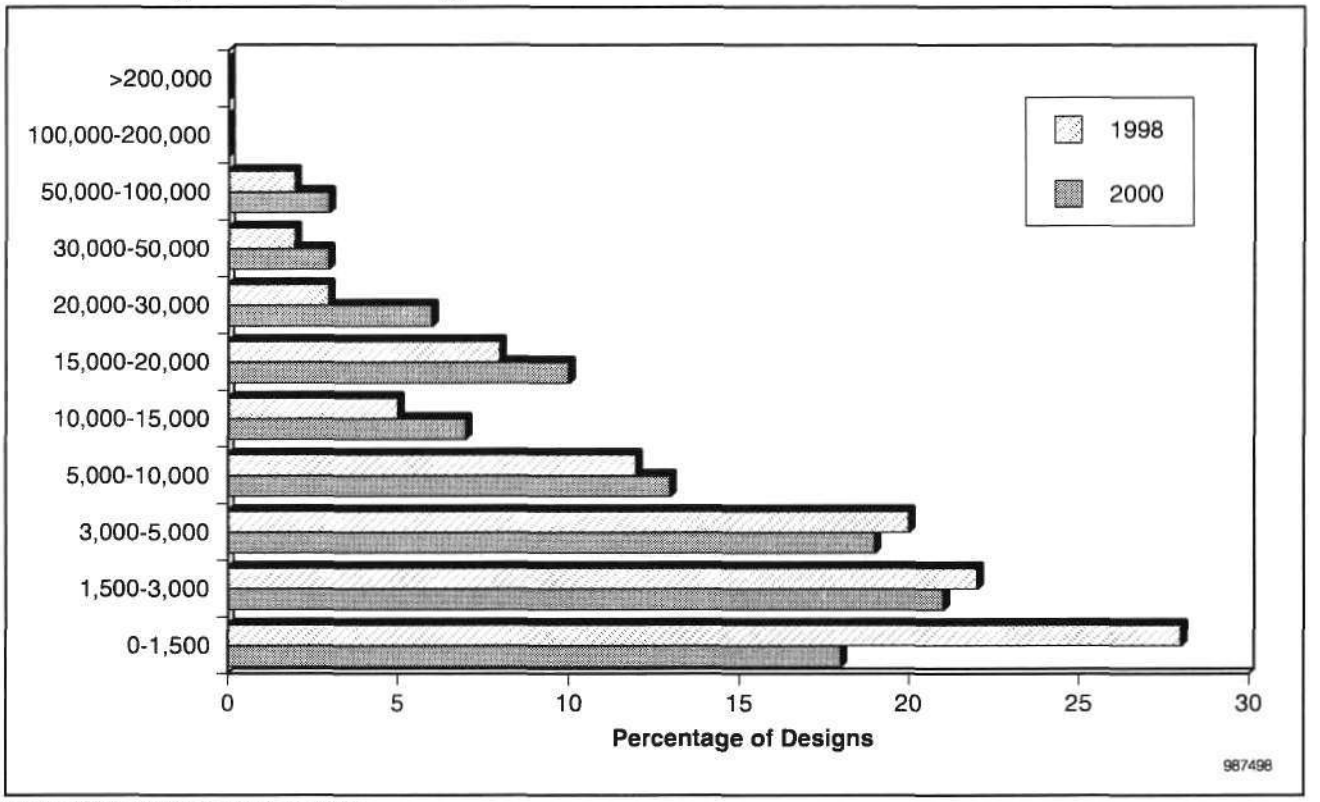
For CPLDs, there is some increase in larger designs (above 15,000 gates). However, a vast majority of CPLDs continue to be designed for lower gate counts, with designs under 5,000 gates the vast majority, even in 2000. Applications that require programmability and larger gate counts are moving to FPGAs when possible. The sweet spot for FPGA designs today is in the 3,000-to-15,000-gate range. By 2000, this is expected to move up substantially, with the majority of designs in the 15,000-to-100,000-gate range. This is the area of excitement, with users (and vendors) pushing the gate count envelope as much as possible. At the high end, by 2000 more than one-fifth of designers say they will use an FPGA over 100,000 gates.

Figure 3-29
FPGA Design Starts by Average Gate Count



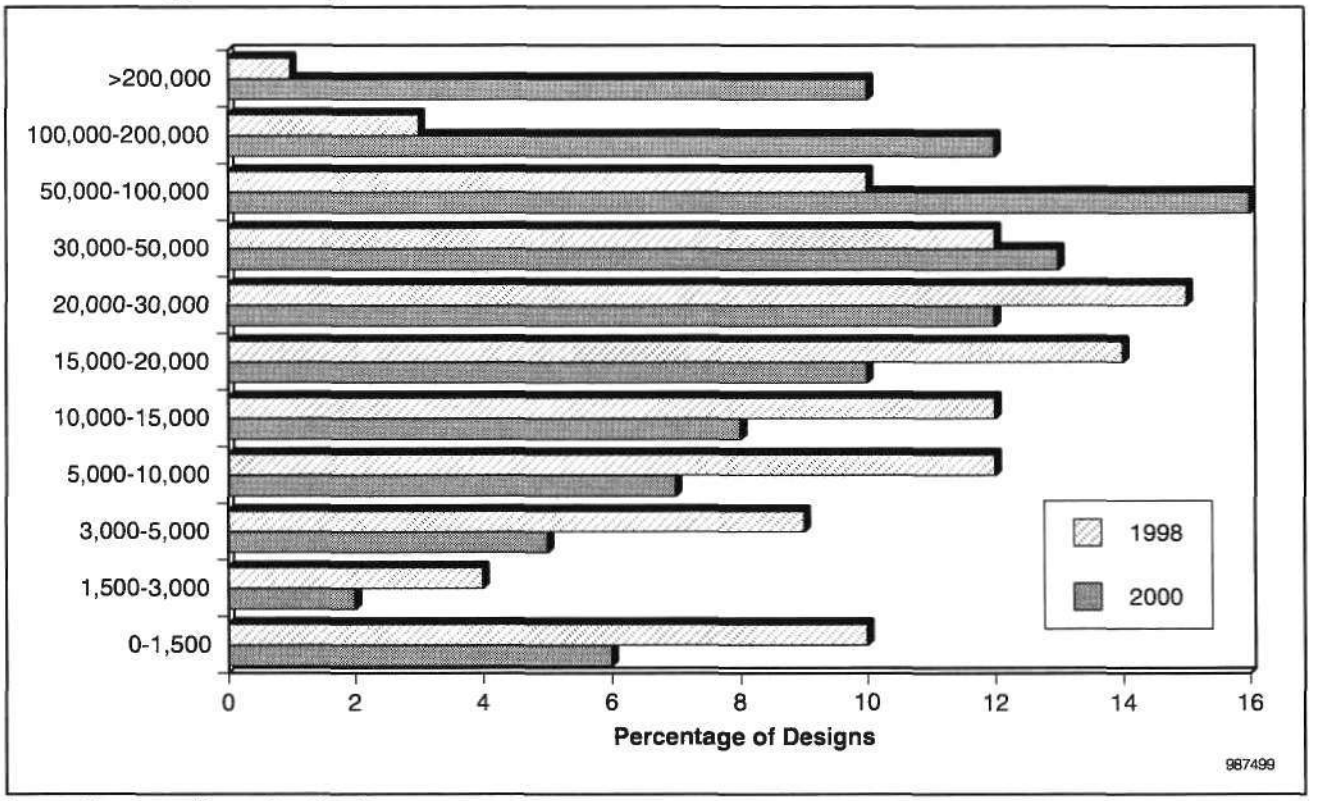
Source: Dataquest (September 1998)

Figure 3-30
CPLD Design Starts by Average Gate Count



Source: Dataquest (September 1998)

Figure 3-31
FPGA Design Starts by Maximum Gate Count



Source: Dataquest (September 1998)

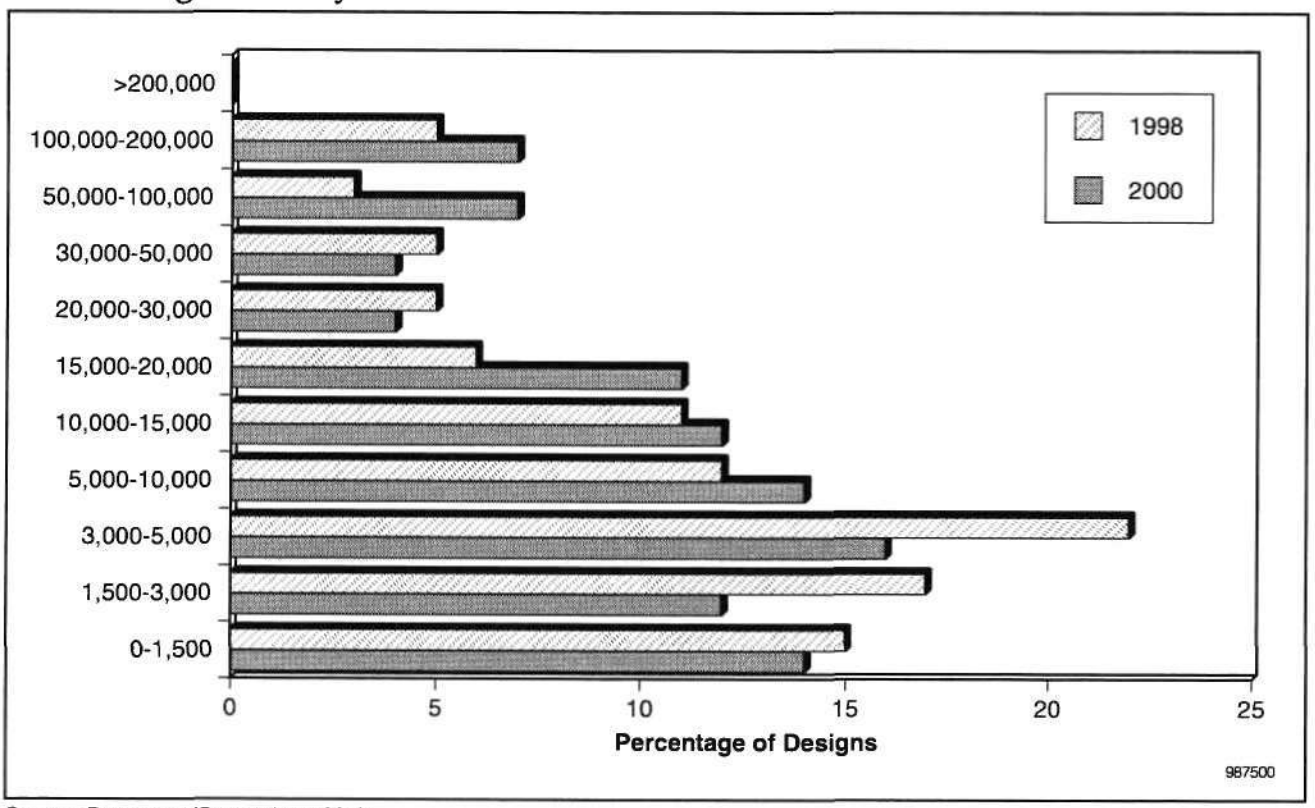
PLD Memory Usage

Memory usage in programmable devices also continues to increase. Figures 3-33 and 3-34 show the average and maximum memory usage in FPGAs; Figures 3-35 and 3-36 show the same for CPLDs. Today, even the majority of FPGAs uses less than 1Kb of memory, but by 2000 there is demand for 4Kb or more in half of the designs; more than one-quarter of users say that they will need a maximum of over 16Kb on-chip by 2000. CPLDs lag a great deal, of course, with the overwhelming majority of designs requiring little memory even by 2000.

PLD Functions

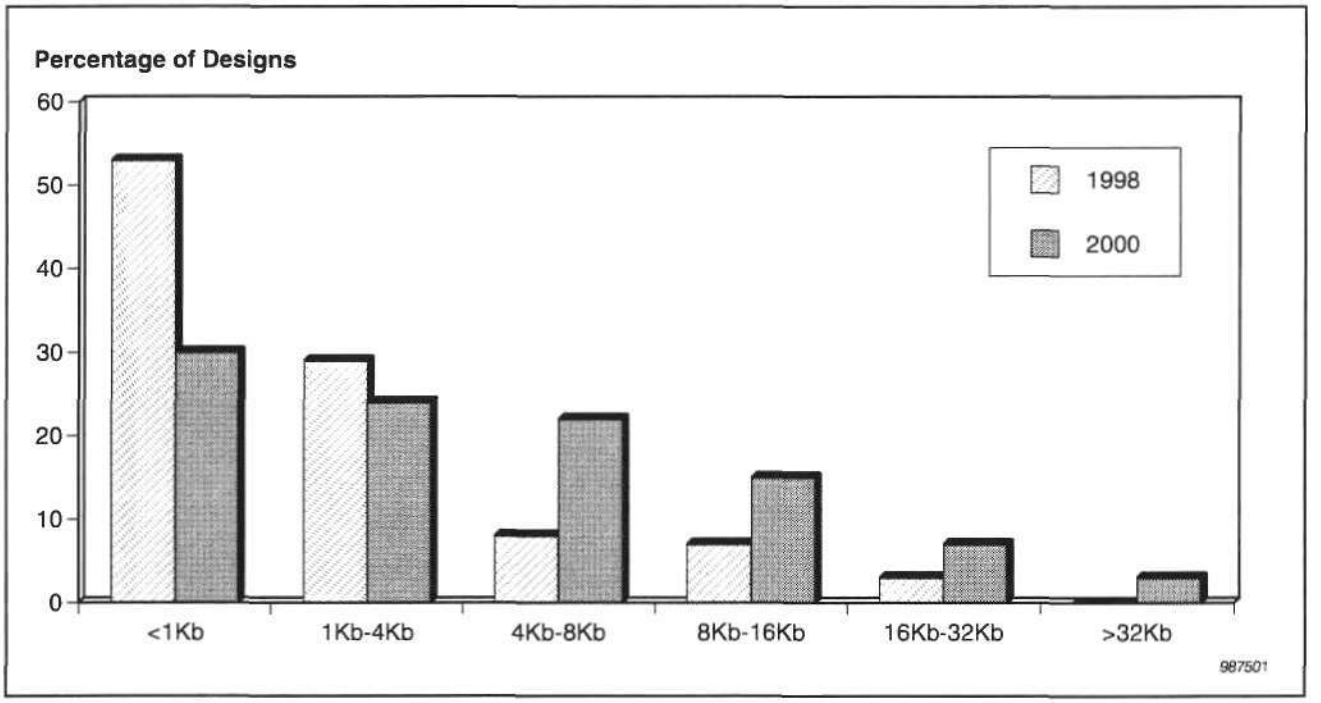
The push for system-level integration is present in the programmable market as well as in ASICs. Given the lower density of PLDs, however, there is a significant lag in integrating other system functions with logic, compared to ASICs, particularly cell-based ASICs. The primary focus is on embedding functions within FPGAs, because CPLDs lag in density, making embedded functions somewhat inefficient. Figure 3-37 details the users' requirements in embedded functions for PLDs. As PLD capacity increases, demand for more complex embedded functions such as microprocessors will begin to increase.

Figure 3-32
CPLD Design Starts by Maximum Gate Count



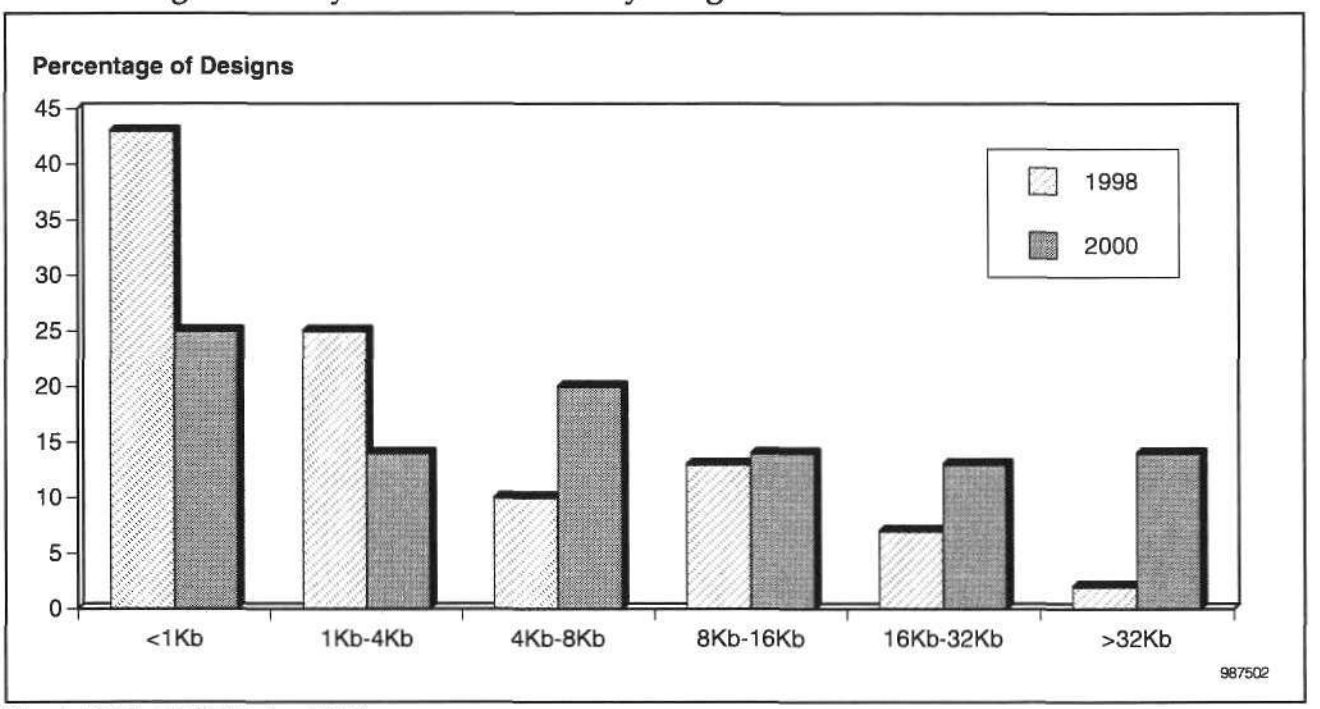
Source: Dataquest (September 1998)

Figure 3-33
FPGA Design Starts by Average Memory Usage



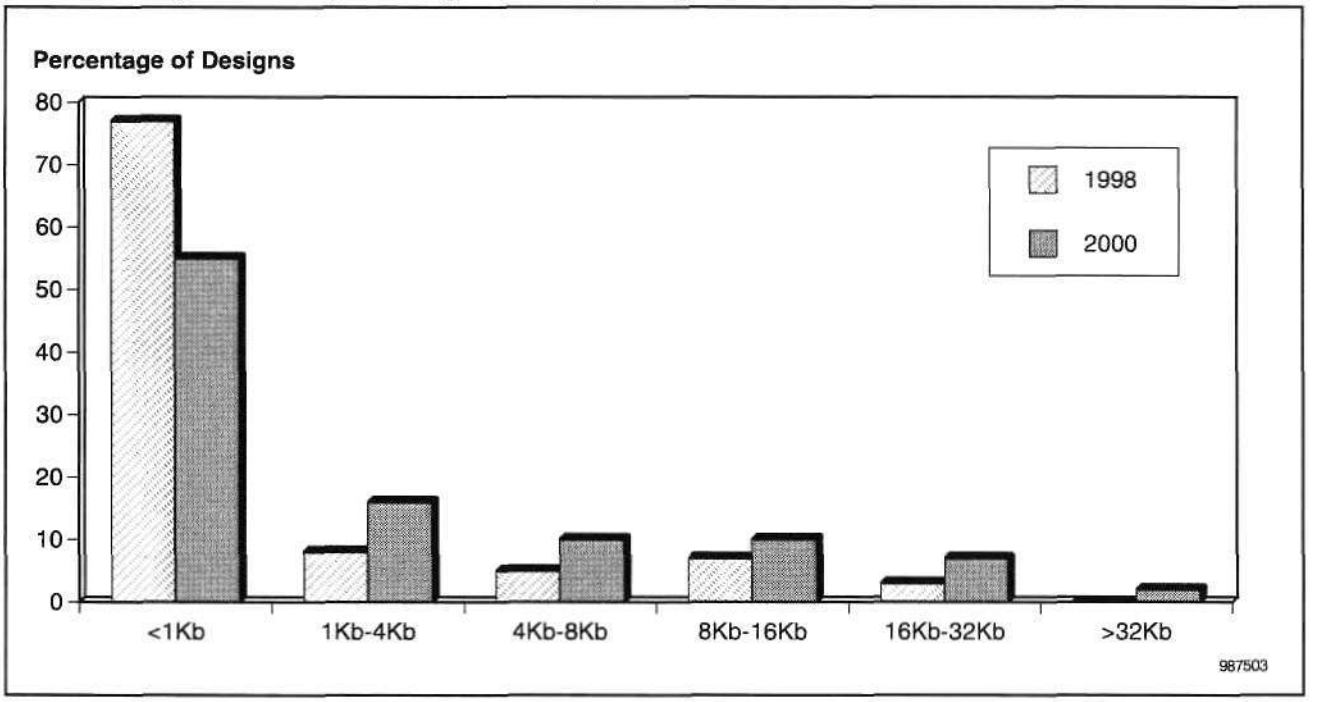
Source: Dataquest (September 1998)

Figure 3-34
FPGA Design Starts by Maximum Memory Usage



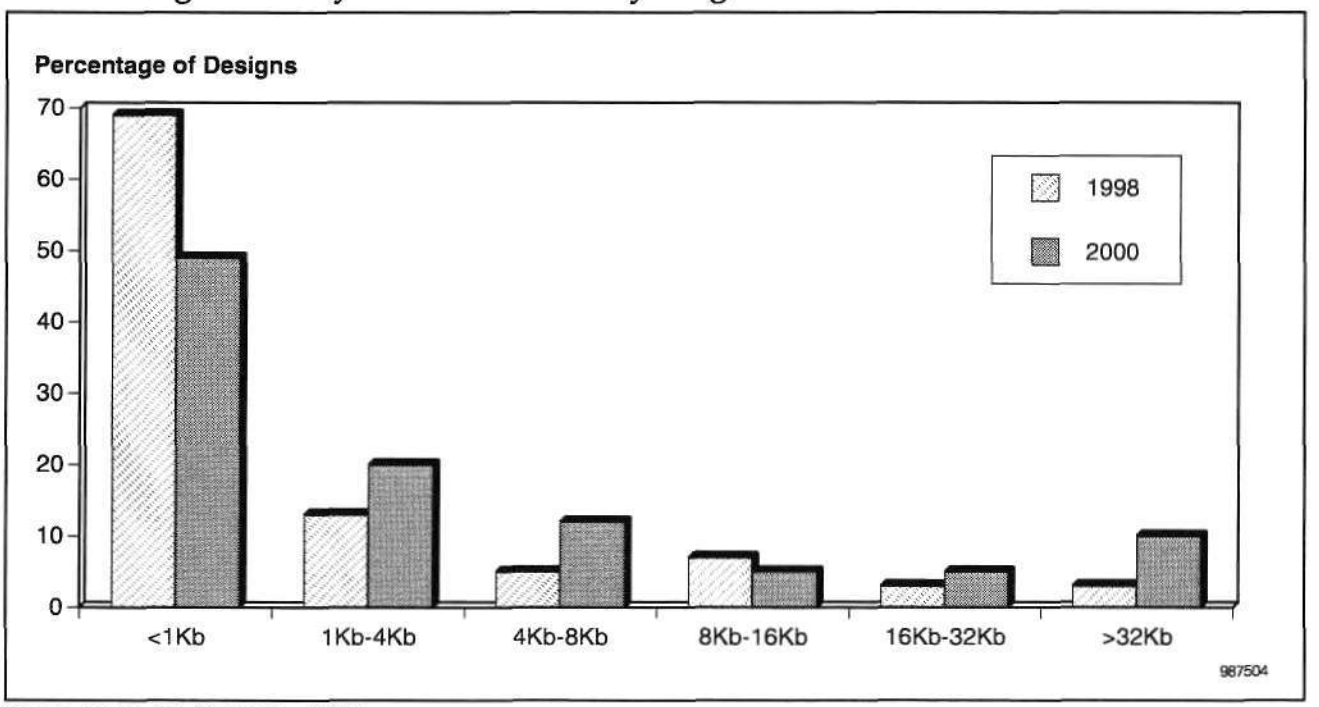
Source: Dataquest (September 1998)

Figure 3-35
CPLD Design Starts by Average Memory Usage



Source: Dataquest (September 1998)

Figure 3-36
CPLD Design Starts by Maximum Memory Usage



Source: Dataquest (September 1998)

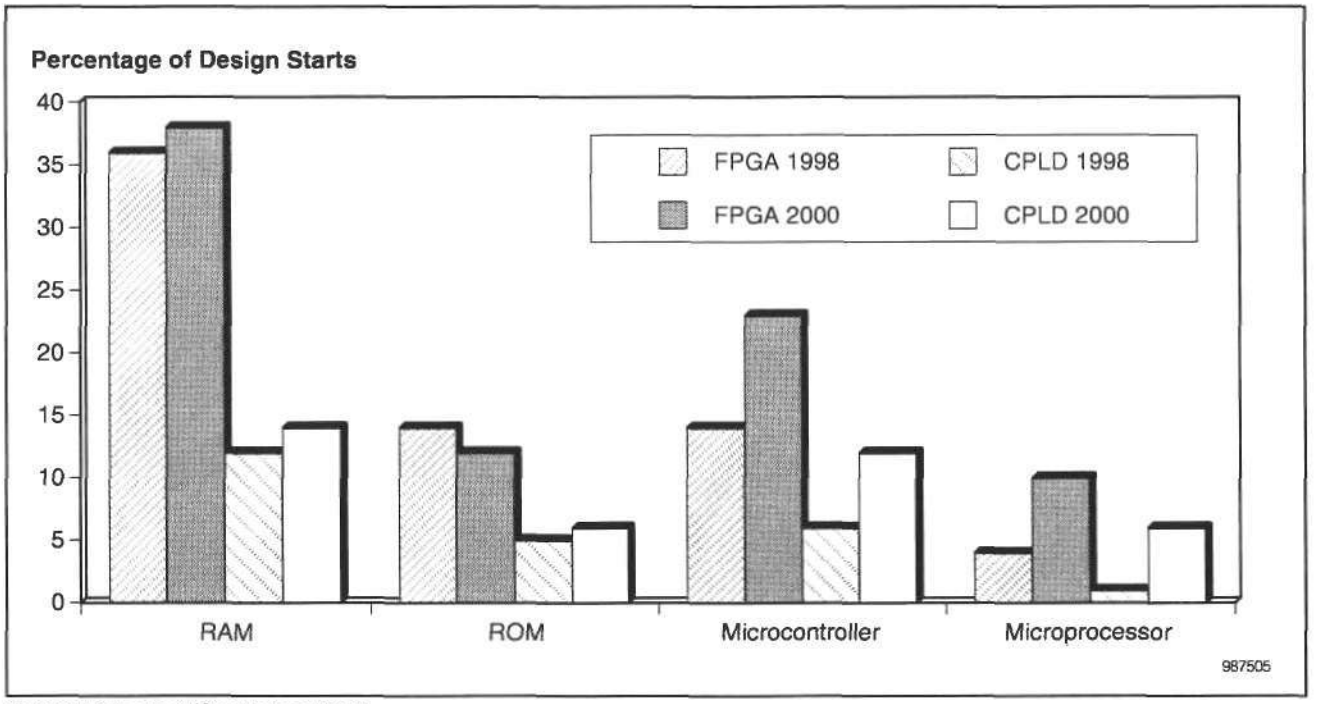
PLD Voltages

Typically, the programmable logic market lags the gate array market by about two years in terms of operating voltages. One of the reasons for this lag is that PLDs have been about one process generation behind ASICs, although we have seen a recent closure of this gap as PLD vendors take advantage of state-of-the-art foundry capacity. Figure 3-38 provides details on FPGA and CPLD operating voltage trends. Although the 5V and 3.3V designs dominate, there is clearly a move for users to synchronize the PLD voltages with ASIC, and there will be a large increase in demand for 2.5V and lower devices, particularly in FPGAs.

PLD Clock Speeds

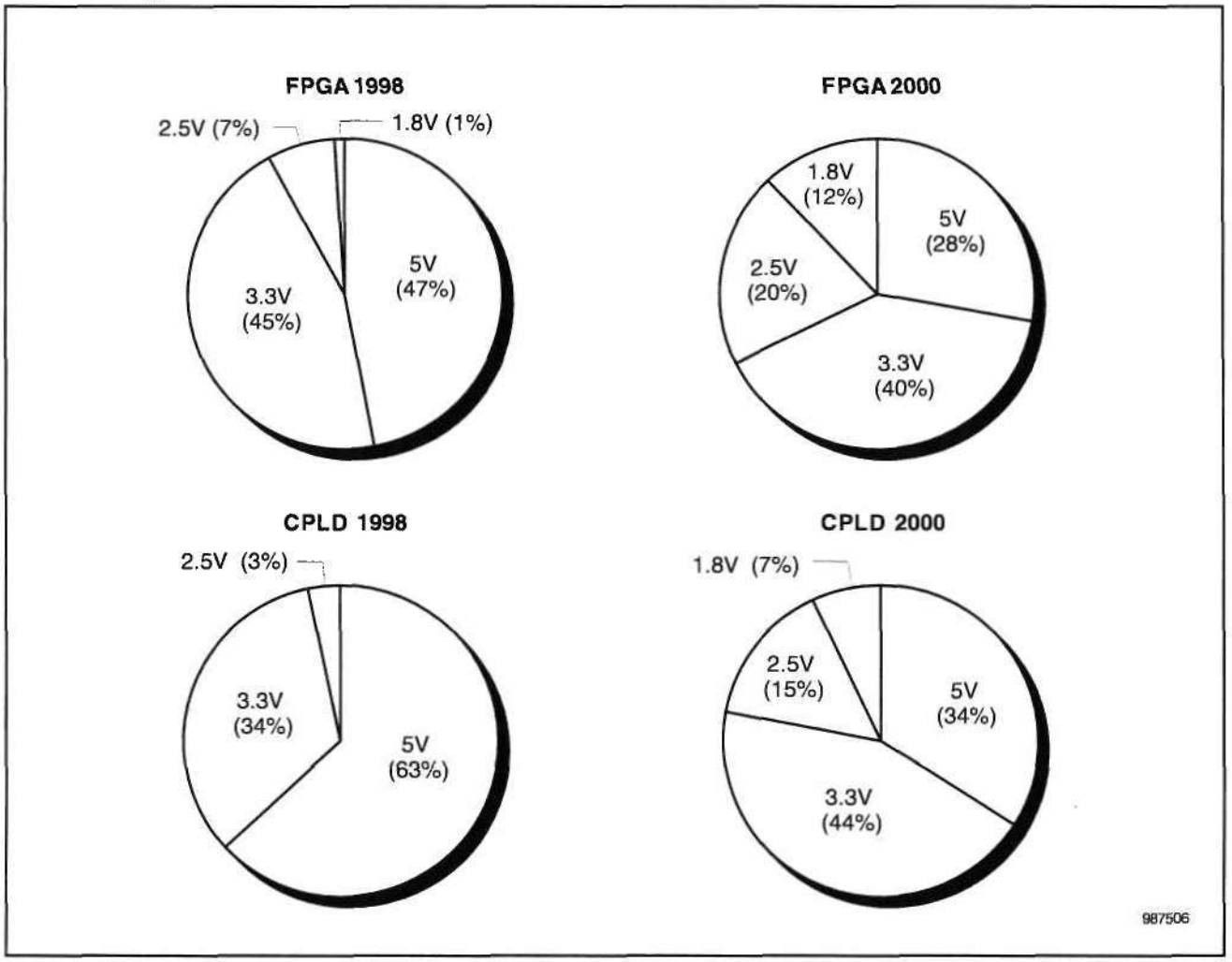
Typical users are asking for clock speeds over a broad range. Different applications have differing performance requirements, and there is not really any one particular sweet spot. Figure 3-39 details the distribution of users' maximum clock speeds in CPLDs; Figure 3-40 gives the data for FPGAs. The one area that stands out is the expectation of significantly more designs in the 75 MHz and faster category. This expectation should be easily met as PLD vendors move to 0.25-micron and finer transistor geometries.

Figure 3-37
PLD Embedded Functions



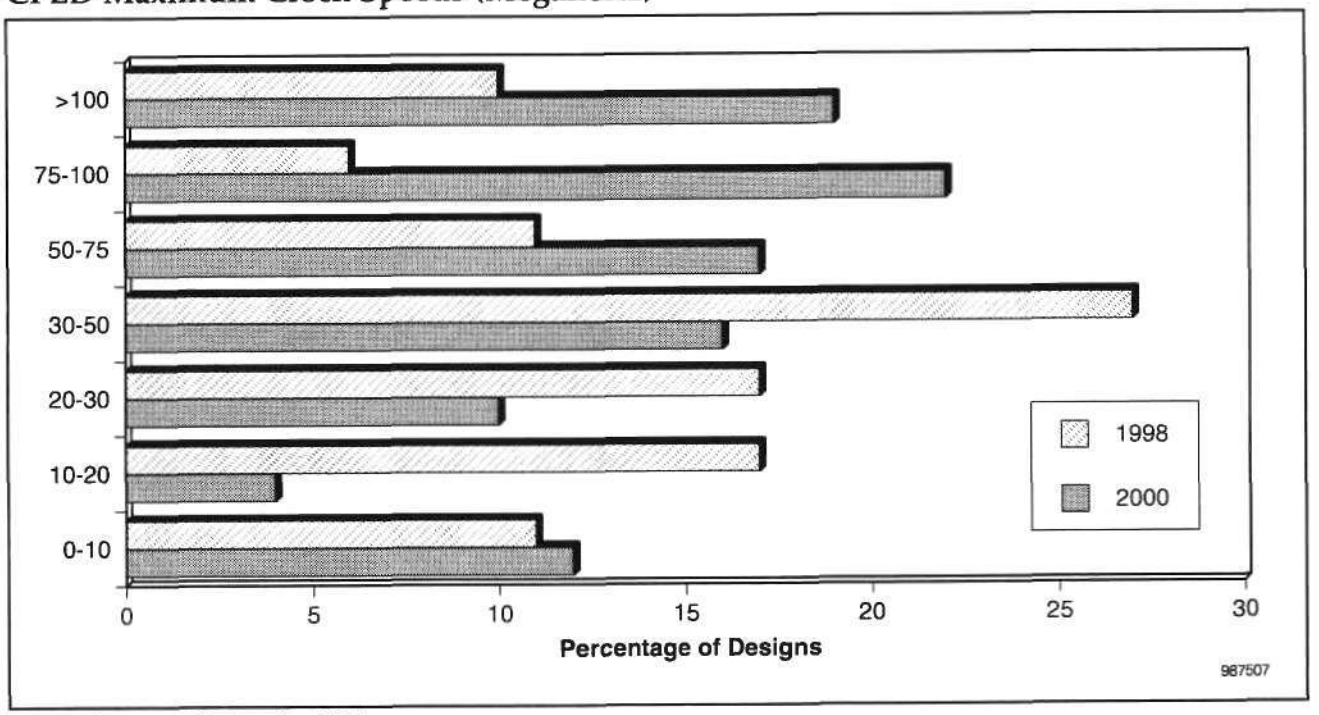
Source: Dataquest (September 1998)

Figure 3-38
PLD Voltage



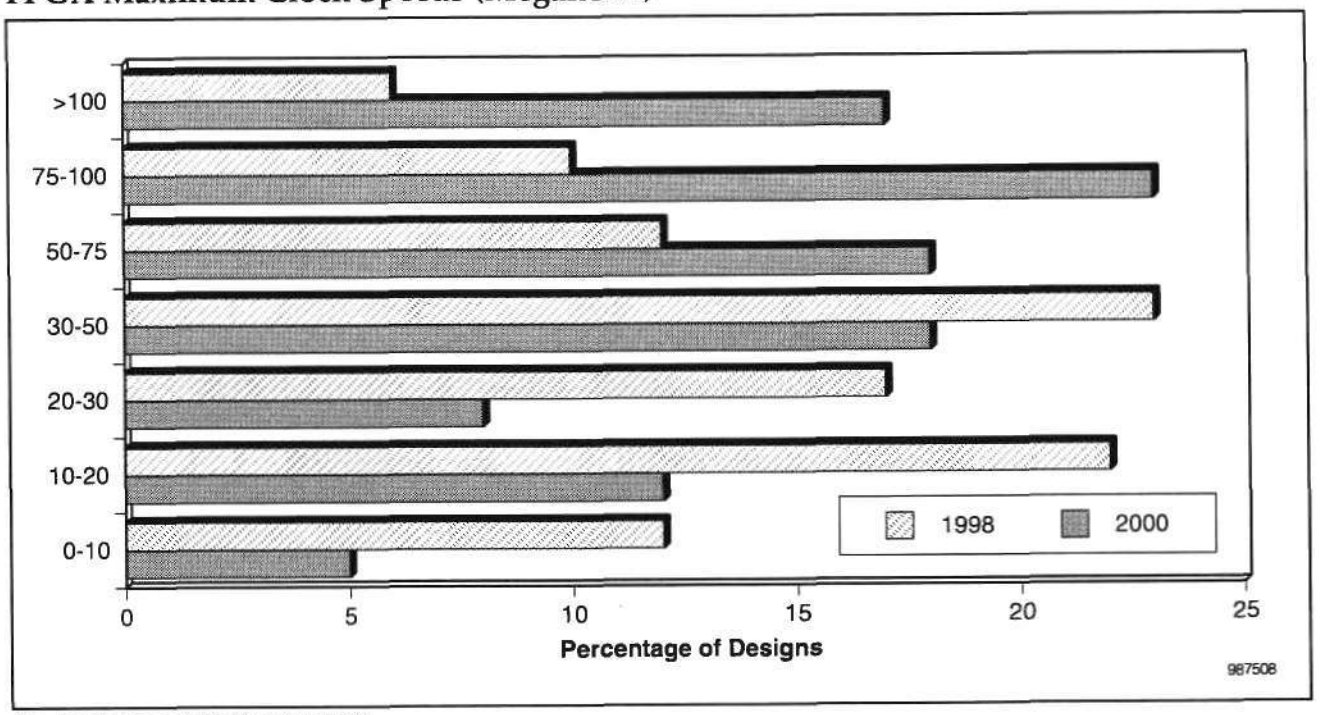
Source: Dataquest (September 1998)

Figure 3-39
CPLD Maximum Clock Speeds (Megahertz)



Source: Dataquest (September 1998)

Figure 3-40
FPGA Maximum Clock Speeds (Megahertz)



Source: Dataquest (September 1998)

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