ASICs WORLDWIDE 1995

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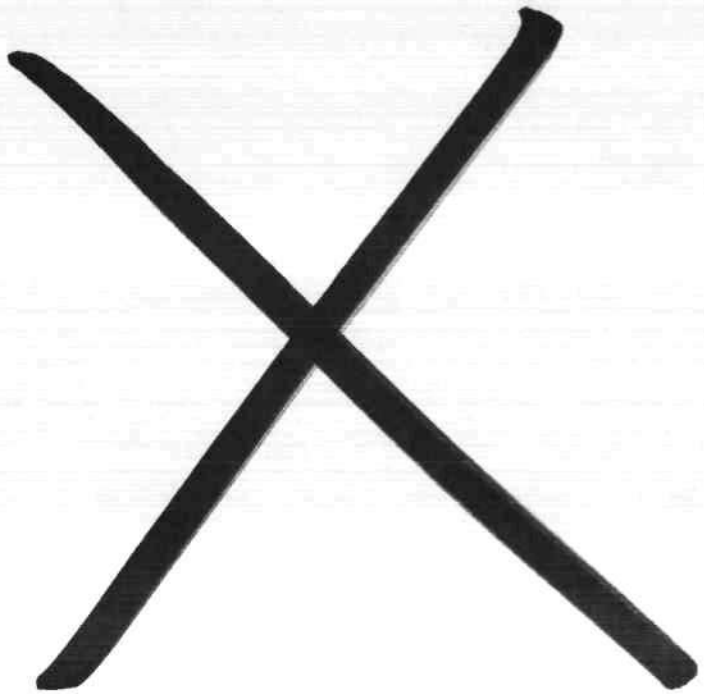

Dataquest

Perspective

ASICs Worldwide

Dataquest Predicts

SLI to Dominate ASIC Market by 2000

Abstract: *Dataquest is introducing a new area of research called "system-level integration" (SLI), also known as "system on a chip." Under the SLI umbrella is both hardware and software co-design, as well as SLI application-specific integrated circuits (ASICs) sold to one user and SLI application-specific standard products (ASSPs) sold to more than one user. Today, the SLI ASIC market is about $1.1 billion and accounts for about 10 percent of the ASIC market (gate arrays and cell-based ICs). Dataquest predicts the SLI ASIC market will reach $14 billion by the year 2000 and account for about 60 percent of the ASIC market. In this document, Dataquest explores SLI applications, leading suppliers, and technology drivers. We also forecast the future of this dynamic market.*
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SLI Definition

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- System-Level Integration: An integrated circuit that contains a compute engine, memory, and logic on a single chip and has more than 100,000 utilized gates.

There are two types of SLI devices: ASICs (application-specific integrated circuits that are sold to a single user) and ASSPs (application-specific standard products that are sold to more than one user).

Market Size and Applications

Dataquest's preliminary 1995 estimate for the SLI ASIC market is $1.1 billion, and we estimate $0.9 billion for SLI ASSPs. About half of the 1995 SLI ASSP market is in telecom chips, including LANs, modems, switching, wireless, and Asynchronous Transfer Mode (ATM). The other half of the SLI ASSP market is in graphics, audio, core logic, and consumer.

SLI ASICs are entering the market at a rapid pace, with many high-volume applications slated to use the technology, including the following:

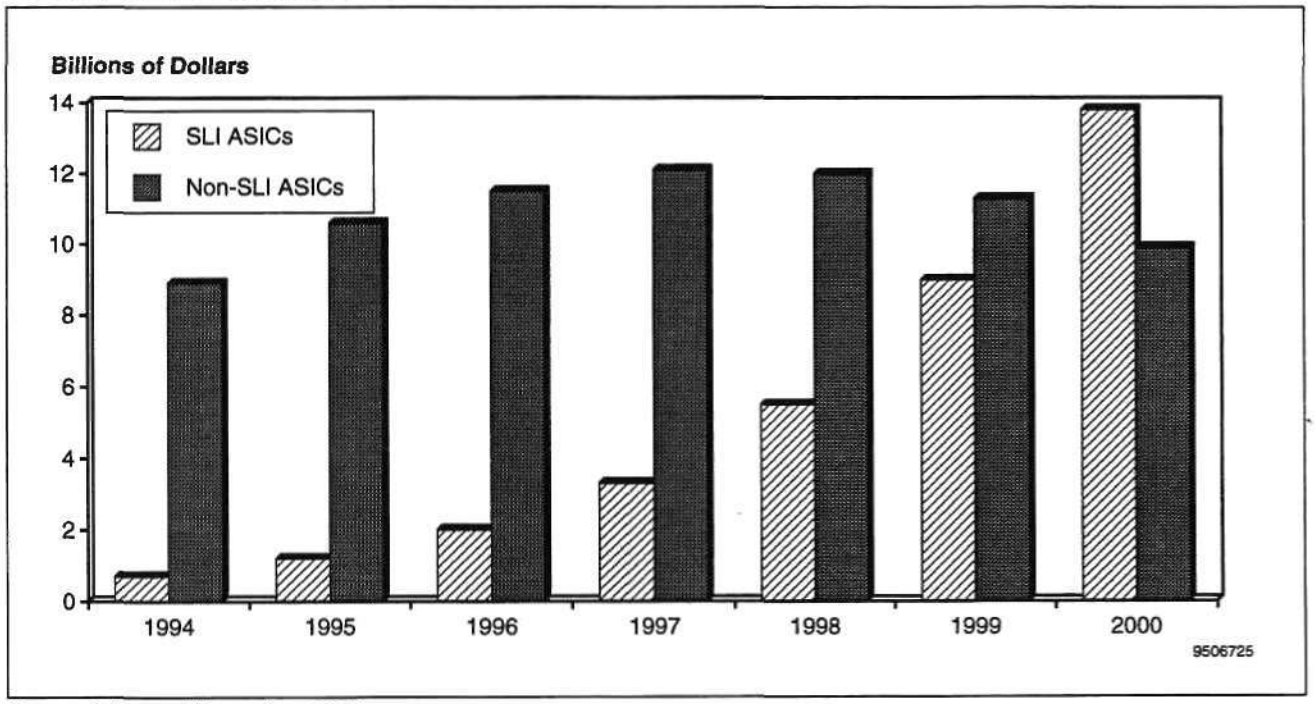
- Personal electronics
- Video games
- Set-top boxes
- Portable computing
- Portable communications
- Multimedia

There are three primary reasons to move to SLI technology: improved functionality, improved performance, and reduced size. The majority of SLI applications today benefit from improved functionality and reduced size, but we believe that speed improvements will soon play a role.

We believe that SLI ASICs account for about 10 percent of the combined total of the 1995 gate array and cell-based IC market and will account for about 60 percent of the market by the year 2000 (see Figure 1).

As a cross-check to our forecast, we looked back six years, when 50,000-to-100,000-gate technology was just being introduced and mainstream was 5,000 to 10,000 gates. In 1989, about 15 percent of ASIC designs were greater than 20,000; 85 percent of designs were less than 20,000 gates. In 1995, about 25 percent of ASIC designs are less than 20,000 gates and about 15 percent are greater than 100,000 utilized gates. We believe that average ASIC complexity in 2000 will be about 125,000 gates and that SLI ASICs will account for the majority of all ASICs. Judging from history, our SLI forecast could be conservative.

Figure 1
Preliminary Worldwide SLI ASIC Market



Source: Dataquest (December 1995)

Leading SLI Suppliers

Nearly all ASIC companies have targeted this market for growth. Leading companies in this market include the following:

- LSI Logic
- IBM
- AT&T
- VLSI Technology
- Toshiba
- NEC

Other companies actively pursuing the SLI market with increasing revenue include Hewlett-Packard, Motorola, Texas Instruments, Mitsubishi, Fujitsu, Hitachi, Oki, Symbios, Samsung, and LG Semicon.

LSI Logic is the largest supplier in this market and has proven that ASIC companies can be profitable with a strong focus on system-level integration and intellectual property. Although LSI Logic struggled to post profits in its first ten years of operation, the company continued to invest in advanced system design methodology and intellectual property that paved the road to profitability. The company has now been highly profitable for over two years and is experiencing record revenue and record profits.

VLSI Technology is another publicly owned ASIC/ASSP company that has pursued the same strategy as LSI Logic and is also posting record revenue

and profits. Other companies with a strong focus on the SLI market with profits that are more difficult to track include IBM, AT&T, Toshiba, and NEC. All of the leading SLI companies have or are close to announcing 0.35-micron processes that are capable of over 2 million gates; they are also investing heavily in advanced system design methodology and intellectual property, including dedicated cell libraries tailored to specific applications.

New Technologies Enable SLI

System-level integration has been dreamed of for many years, but the technologies required to execute SLI have only recently emerged. Five key areas are critical for the success of the SLI market, as follows:

- 0.35-micron processes with up to 5 million usable gates
- Comprehensive focused cell libraries
- Improved test capabilities
- Improved design tools
- New packages with high pin counts

While the mainstream market is still designing in gate counts far below 1 million gates, leading ASIC suppliers are announcing 0.35-micron products with up to 5 million usable gates. The 0.35-micron product families not only give a high maximum gate count but also increase the usable gate count of the cost-effective solution. The cost-effective solution, or sweet spot, of 1995 ASIC designs is in the 50,000-to-100,000-gate range (see Figure 2). We are seeing a much higher percentage of designs with greater than 100,000 usable gates as system designers use 0.6-micron and 0.5-micron ASIC families. As system designers strive for system-level solutions and embrace 0.35-micron ASIC families, the sweet spot of these product families will be close to 1 million gates, which offers considerable silicon real estate for incorporating system functions on a single chip.

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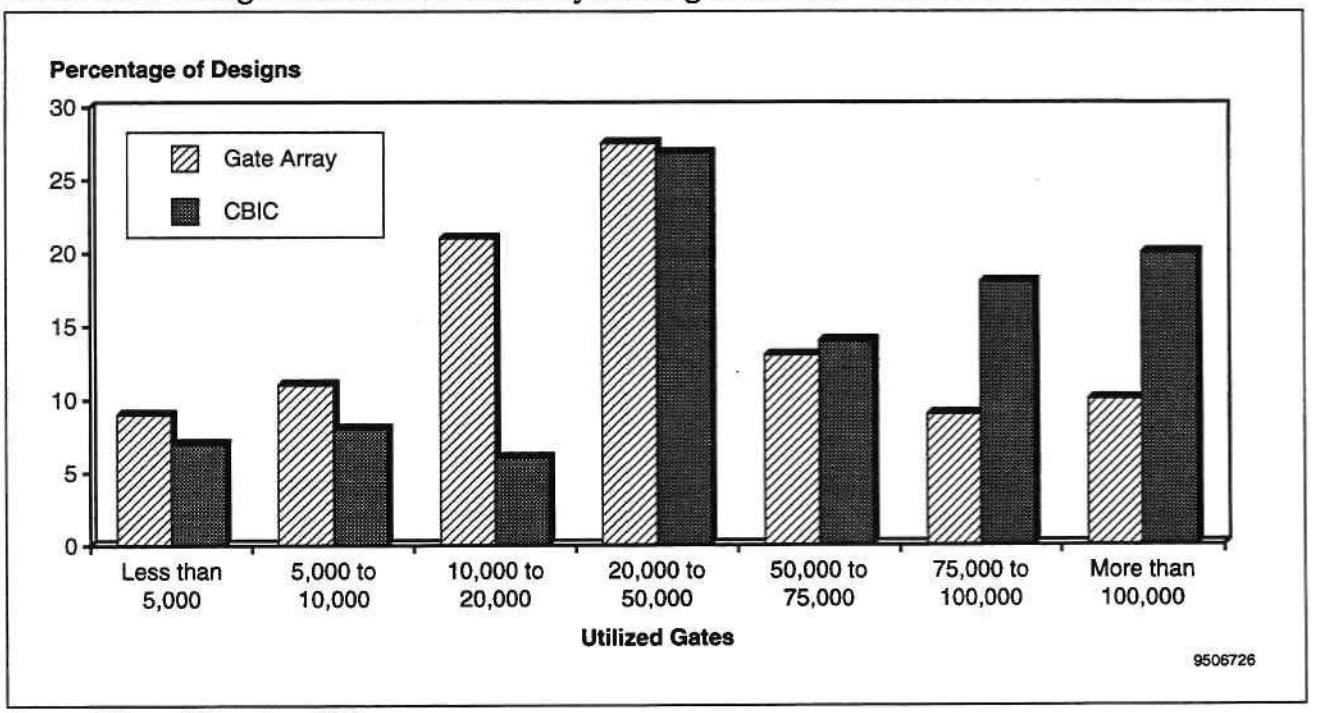

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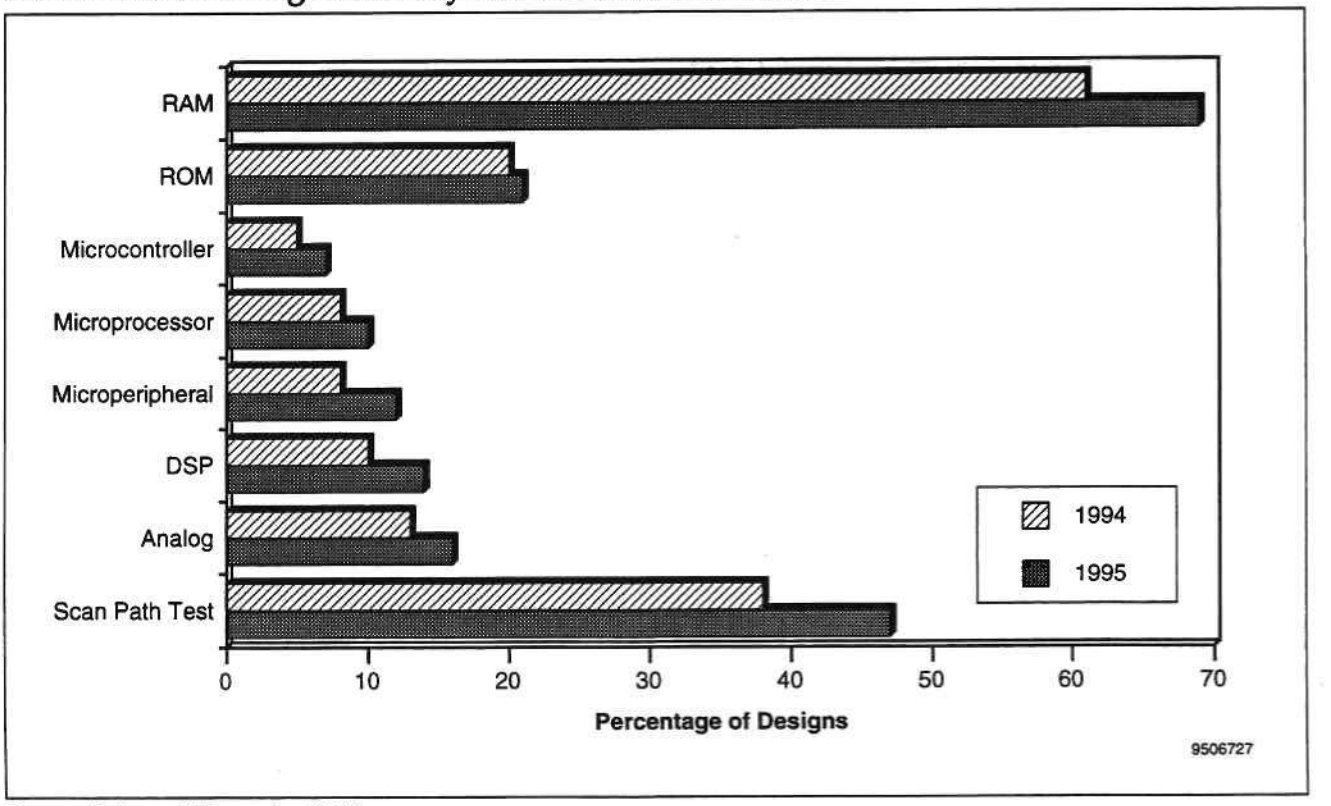
Figure 3
Cell-Based IC Design Starts by Cell Use: North America



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New developments in packaging technology are also spurring the growth of the SLI market. Ball grid array packages (BGA) have made major strides in the high-pin-count area (greater than 250 pins), and we believe that BGAs will be the package of choice for mainstream SLI designs of the future. BGAs now account for about 10 percent of gate array designs today (see Figure 5) and we believe that they will account for over 40 percent of all ASIC designs and over 70 percent of SLI designs in the year 2000.

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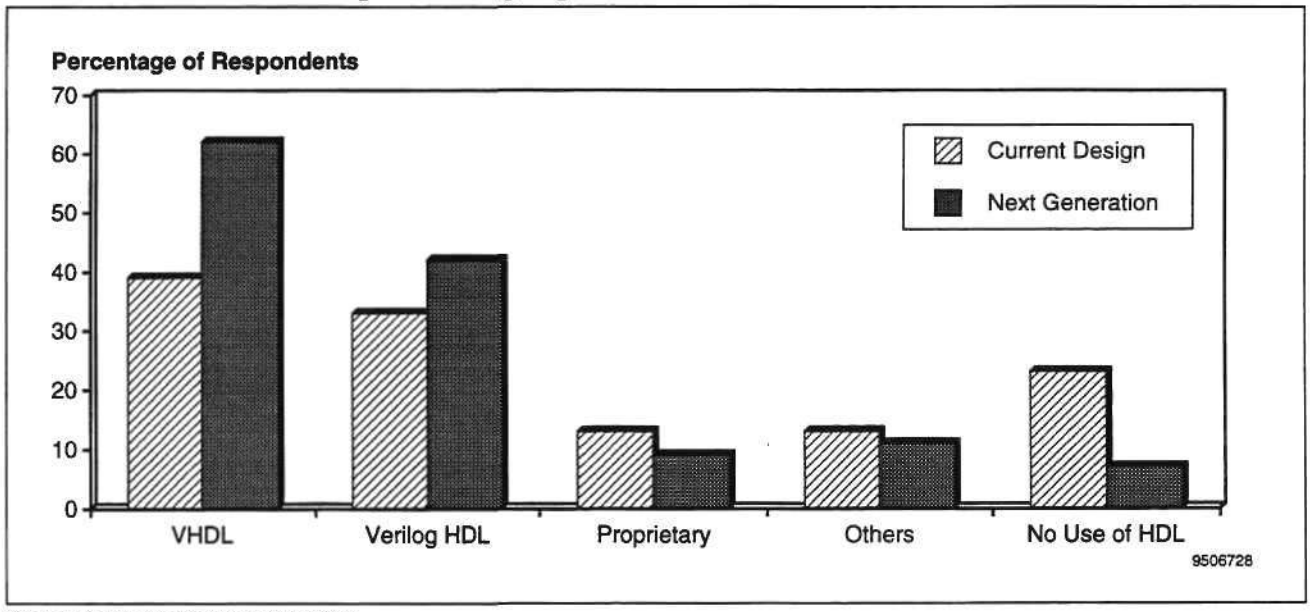
Use of Hardware Description Languages: North America



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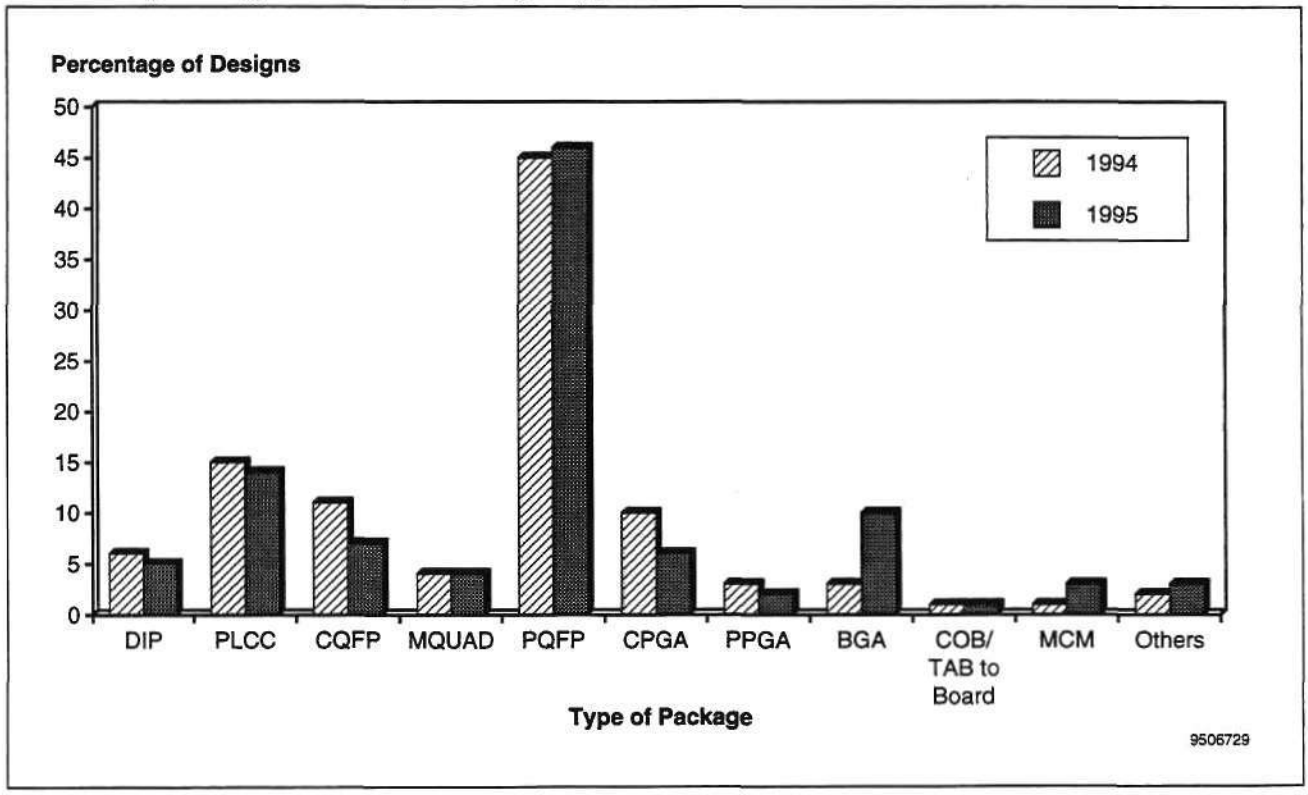

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- Improved functionality
- Improved system profit margins

The bottom line is that if system designers receive improved system profit margins by using SLI technology, SLI suppliers will also receive improved profit margins. Invest now or be left behind!

For More Information...
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Internet address ..... blewis@dataquest.com
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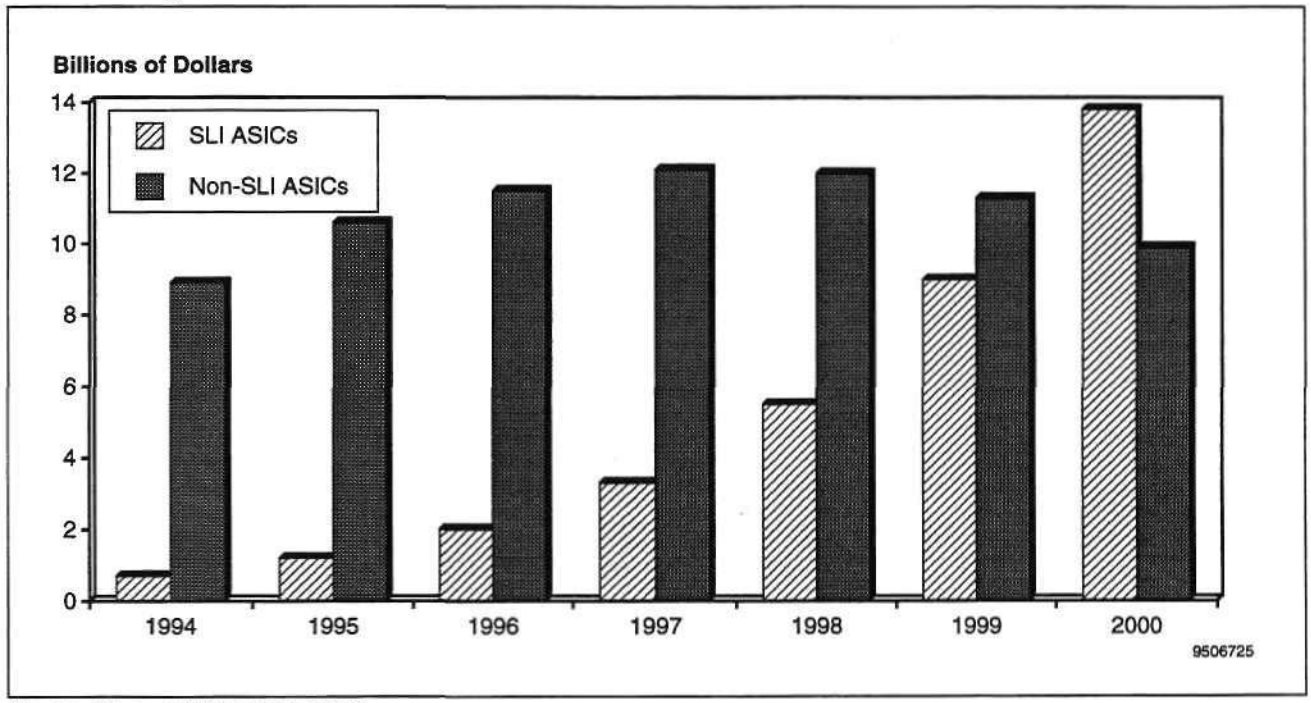

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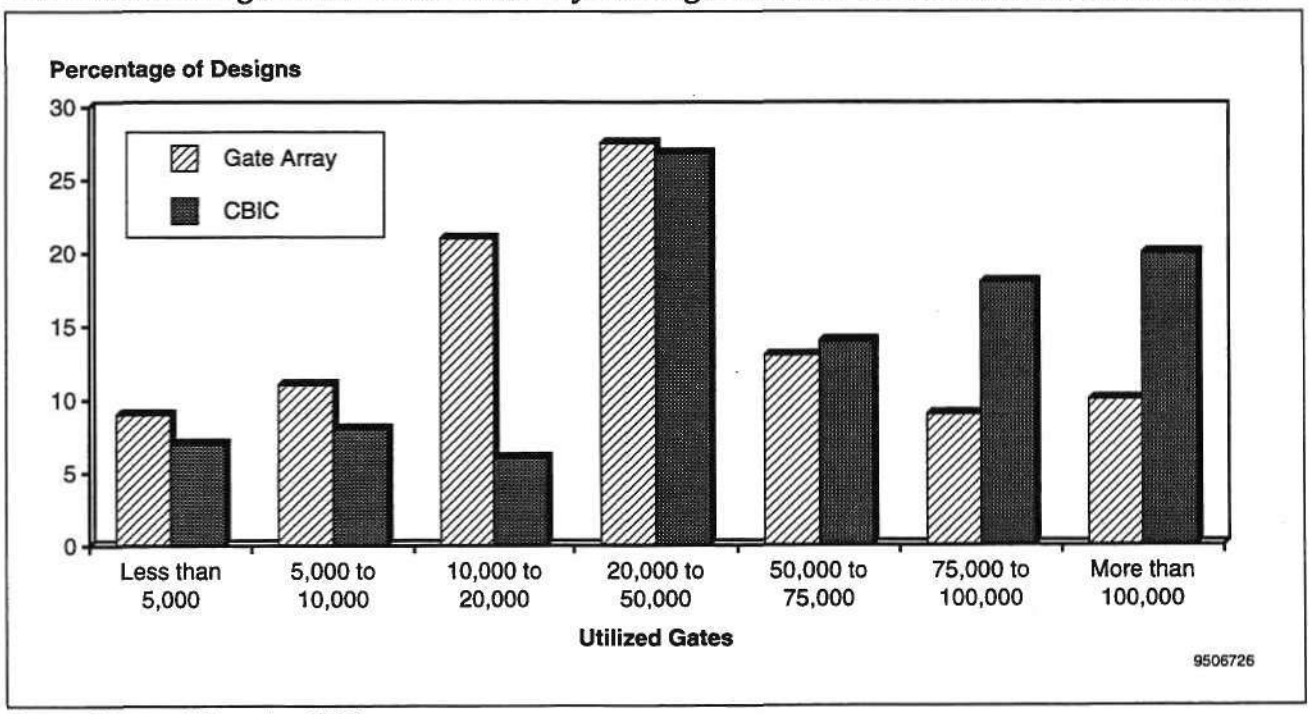

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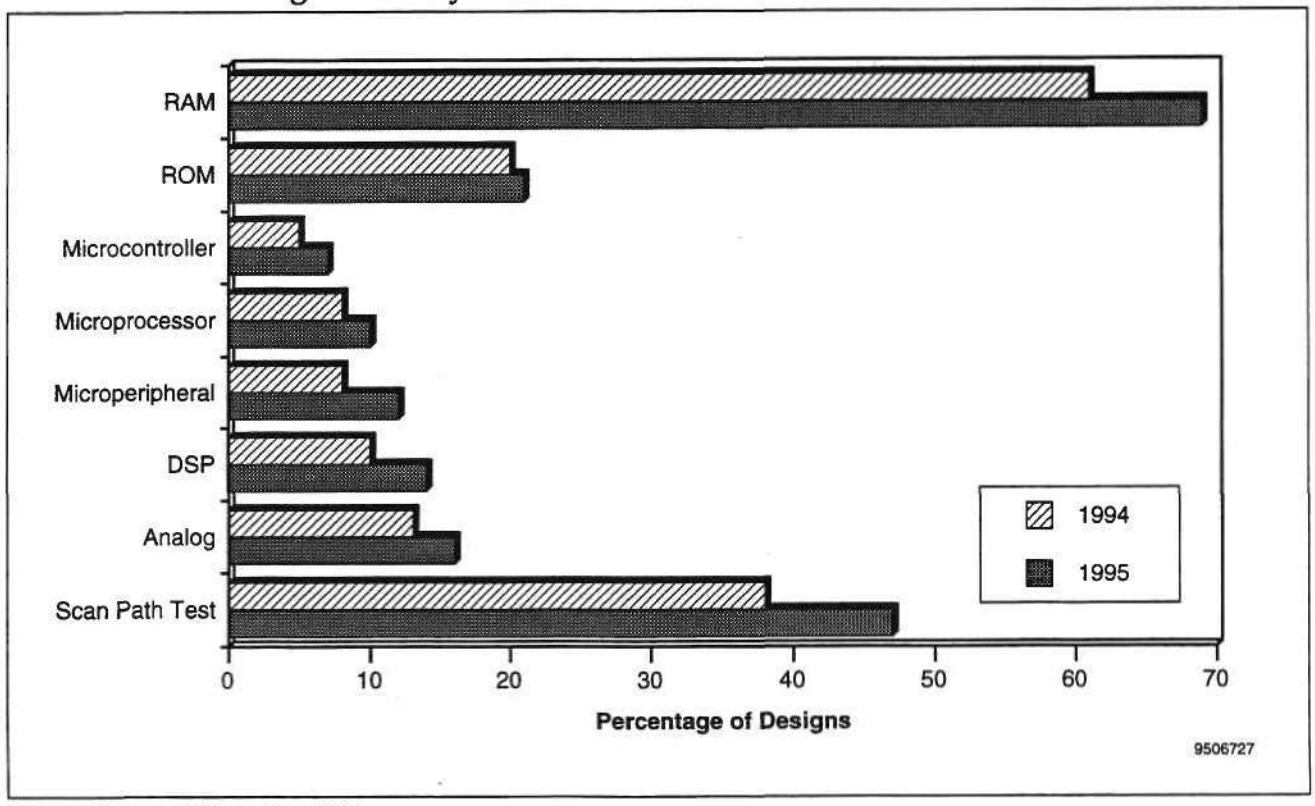

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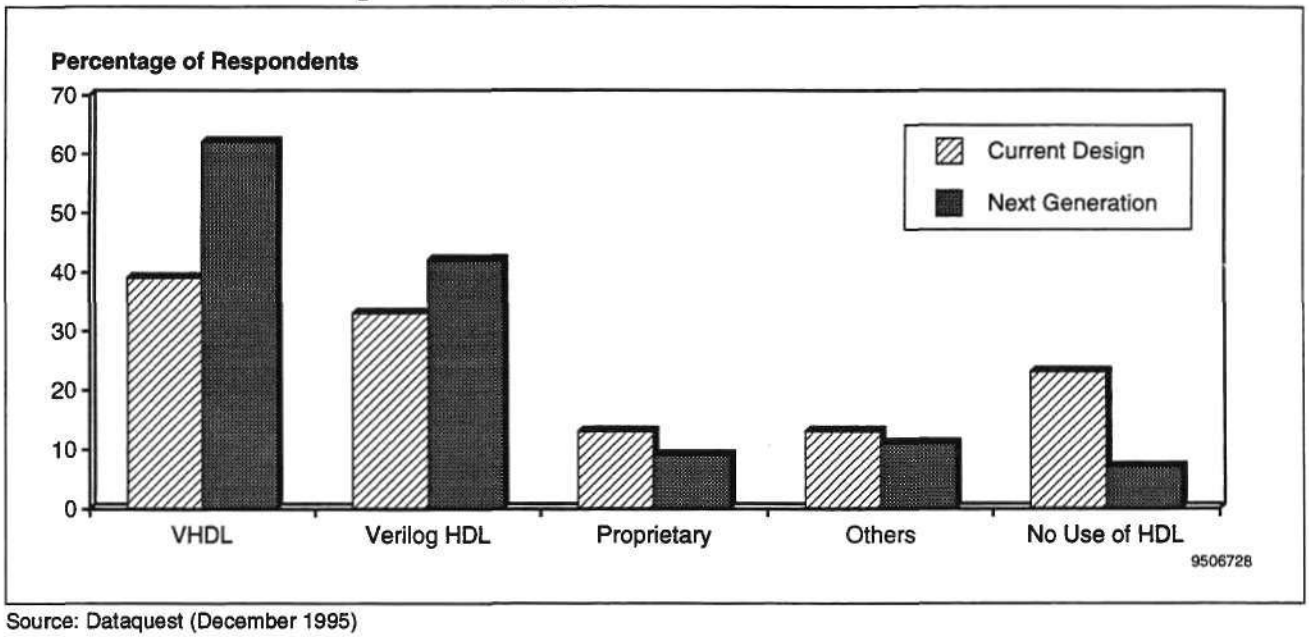

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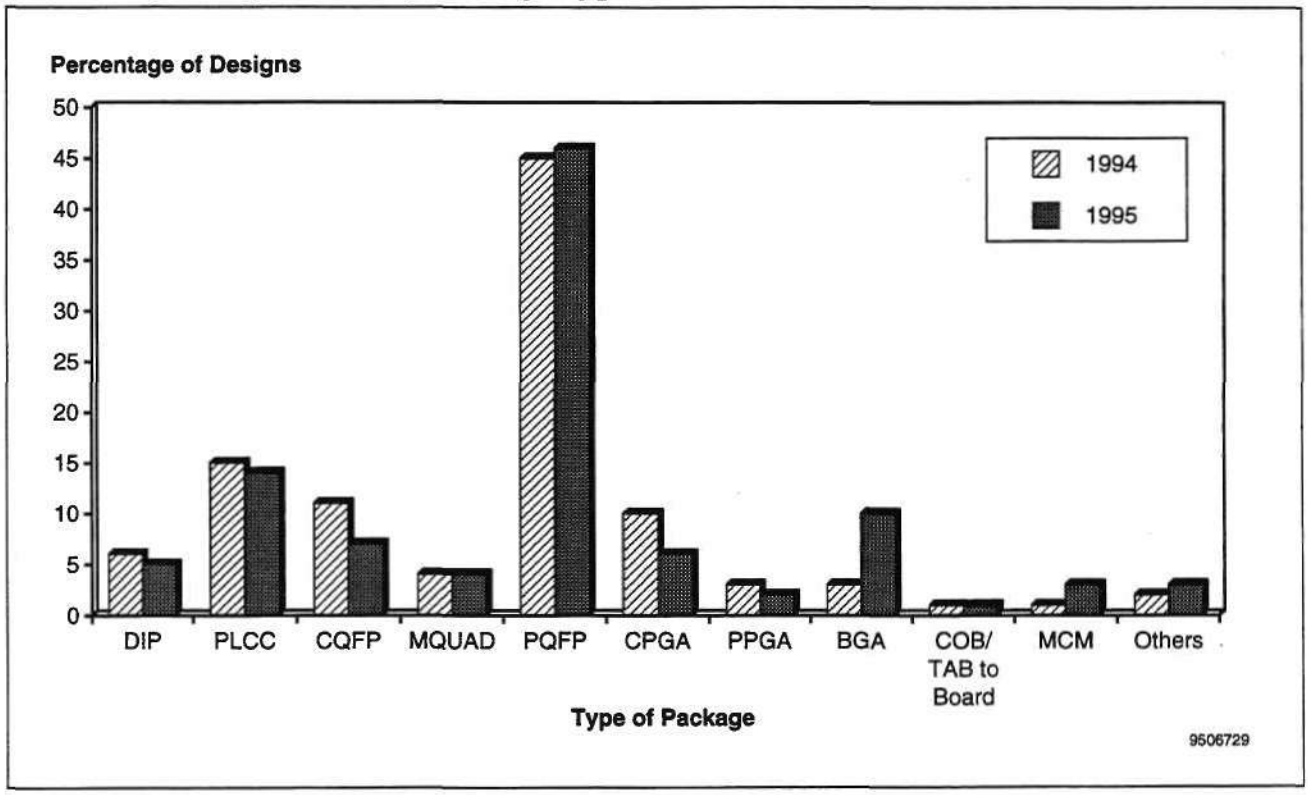

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Market Analysis

ASICs Worldwide

Market Analysis

Cell-Based ICs Soar in 1994 ASIC Market Share

Abstract: *Cell-based IC revenue growth outpaced that of MOS PLDs and gate arrays, according to Dataquest's 1994 market share survey. In this article, Dataquest examines the 1994 ASIC market share rankings by company and product and explores the key areas where suppliers can invest to maximize profits.*
By Bryan Lewis

Traditional ASIC Suppliers Move to Higher Ground

Leading ASIC suppliers are shifting their focus from low-value commodity gate arrays to higher-margin, value-added cell-based ICs (CBICs). According to Dataquest's 1994 market share estimates, the top five ASIC suppliers experienced a combined 50 percent increase in CBIC sales over 1993, compared to a 15 percent increase in MOS gate array sales. LSI Logic, the largest merchant ASIC supplier and second-largest MOS gate array supplier, posted an outstanding 176 percent increase in CBIC sales, compared to a meager 4 percent increase in gate array sales. The entire worldwide MOS CBIC market had the highest growth rate of all the ASIC products, posting a 29 percent increase, followed by MOS PLDs with a 23 percent increase and MOS gate arrays with a 19 percent increase. Traditional ASIC suppliers are moving to higher-density devices (more than 100,000 gates) using large functional blocks where margins are higher, while FPGA and CPLD suppliers are moving in on the lower-density market to fill the void.

During 1994, NEC extended its lead over Fujitsu in total ASIC sales (see Figure 1) by increasing its CBIC sales 87 percent. LSI Logic strengthened its position in total ASIC sales by jumping from the No. 12 position in 1993 total CBIC sales to No. 6 in 1994 sales. Xilinx was one of the big winners in 1994 and set the record for the first exclusively MOS PLD company to make the top 10 in total ASIC sales. Xilinx's success in making the top 10 supplier

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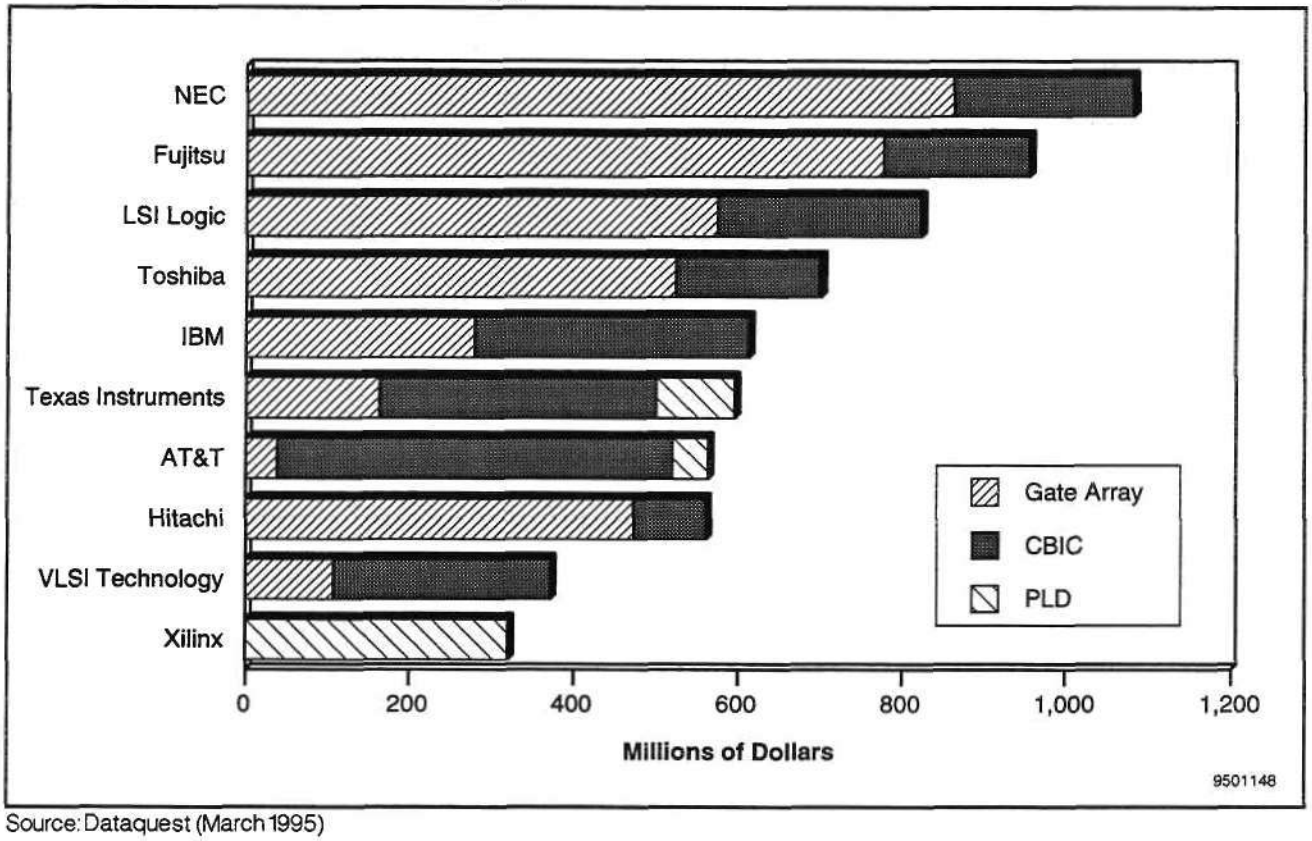
Figure 1
1994 Top 10 Worldwide ASIC Suppliers



Source: Dataquest (March 1995)

list is proof that MOS PLDs are filling the gap as traditional ASIC suppliers are abandoning the lower-density market.

Two important points should be kept in mind when examining the following market share rankings. First, yen appreciation against the dollar helped most Japanese companies post better-than-average growth rates (the yen appreciated about 8 percent against the dollar). Second, Dataquest estimates include sales to internal division (intracompany sales). Although NEC is the largest total ASIC supplier, LSI Logic is the largest merchant market ASIC supplier.

1994 ASIC Market Share

Table 1 shows the 1994 top 20 ASIC suppliers.

The following are footnotes to the ASIC market estimates:

- Total ASIC rankings include gate arrays plus CBICs plus PLDs.
- Rankings are based on dollar shipments, which include the following five sources of revenue:
  - Intracompany revenue (sales to internal divisions)
  - Nonrecurring engineering (NRE) revenue
  - ASIC software revenue

Table 1
1994 Worldwide Market Share Ranking: Total MOS/BiCMOS and Bipolar ASIC (Millions of Dollars)

1994 Rank	1993 Rank		1993 Revenue	1994 Revenue	Percentage Change (%)	1994 Market Share (%)
1	1	NEC	851	1,082	27	10.0
2	2	Fujitsu	832	956	15	8.8
3	3	LSI Logic	642	823	28	7.6
4	5	Toshiba	542	700	29	6.5
5	6	IBM	540	613	14	5.7
6	4	Texas Instruments	556	596	7	5.5
7	7	AT&T	499	564	13	5.2
8	8	Hitachi	428	561	31	5.2
9	9	VLSI Technology	344	372	8	3.4
10	12	Xilinx	231	321	39	3.0
11	11	Motorola	269	316	17	2.9
12	10	Advanced Micro Devices	288	281	-2	2.6
13	14	NCR	202	273	35	2.5
14	13	Hewlett-Packard	230	255	11	2.4
15	17	SGS-Thomson	168	212	26	2.0
16	18	Matsushita	154	212	38	2.0
17	19	Altera	140	199	42	1.8
18	16	GEC Plessey	170	173	2	1.6
19	25	Mitsubishi	73	170	133	1.6
20	20	Mietec	139	165	19	1.5

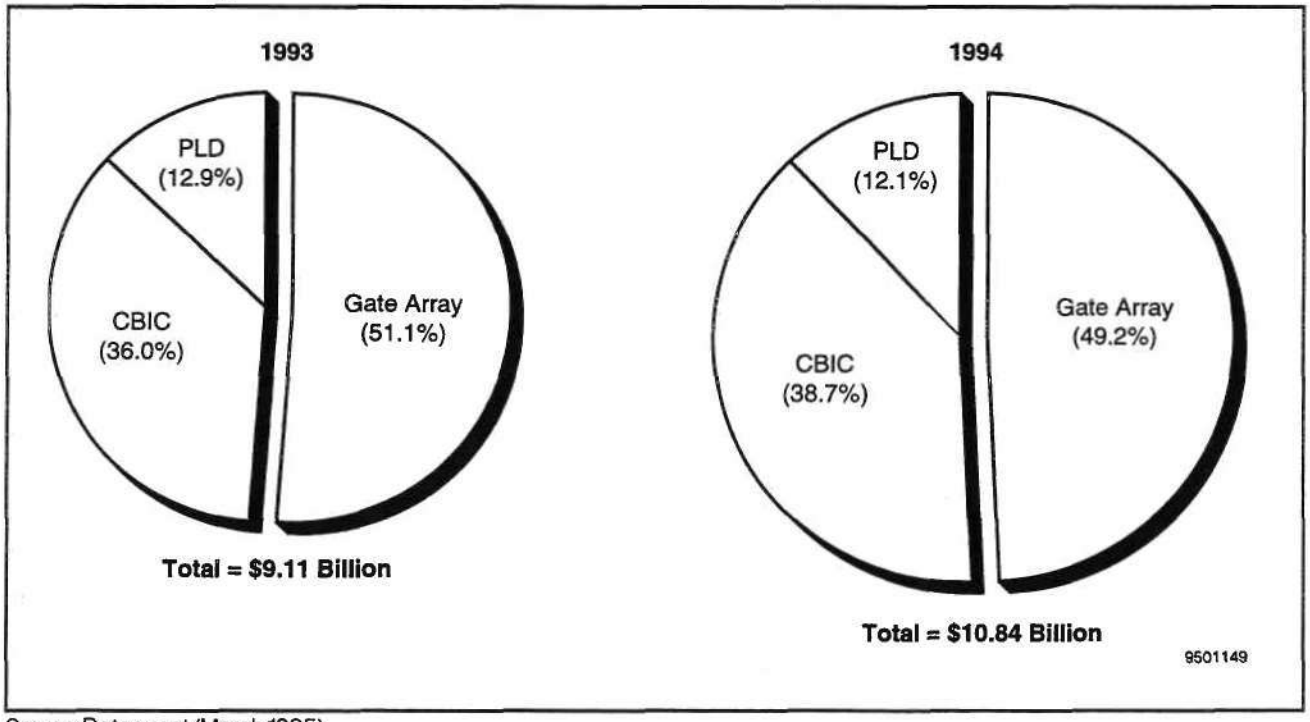
Source: Dataquest (March 1995)

  - PLD development kit revenue
  - Device production revenue
- Full-custom IC revenue is excluded from ASIC market share.
- ASIC product revenue is based on the combined revenue from digital, mixed analog/digital, and analog product.
- The U.S. dollar depreciated 8.4 percent against the yen during 1993. Dataquest's exchange rates are: U.S.$1 = ¥111.20 (1993), U.S.$1 = ¥101.81 (1994).

Product Overview

Figure 2 presents the composition of the ASIC market by product. Although gate arrays continue to dominate the market, CBICs are gaining market share. Total PLDs lost market share because bipolar PLDs had a dismal year, declining 29.4 percent (see Table 2). Bipolar PLDs are being replaced by MOS PLDs, which had a solid 22.6 percent growth rate, exceeding the growth rate of the total ASIC market.

Figure 2
Estimated 1993/1994 Worldwide ASIC Consumption, by Product



Source: Dataquest (March 1995)

Table 2
Estimated 1993/1994 Worldwide ASIC Consumption, by Product (Millions of Dollars)

	1993	1994	Percentage Change
MOS/BiCMOS Gate Array	3,785	4,520	19.4
Bipolar Gate Array	873	818	-6.3
MOS/BiCMOS Cell-Based IC	3,201	4,116	28.6
Bipolar Cell-Based IC	82	77	-6.1
MOS/BiCMOS PLD	925	1,134	22.6
Bipolar PLD	248	175	-29.4
Total Market	9,114	10,840	18.9

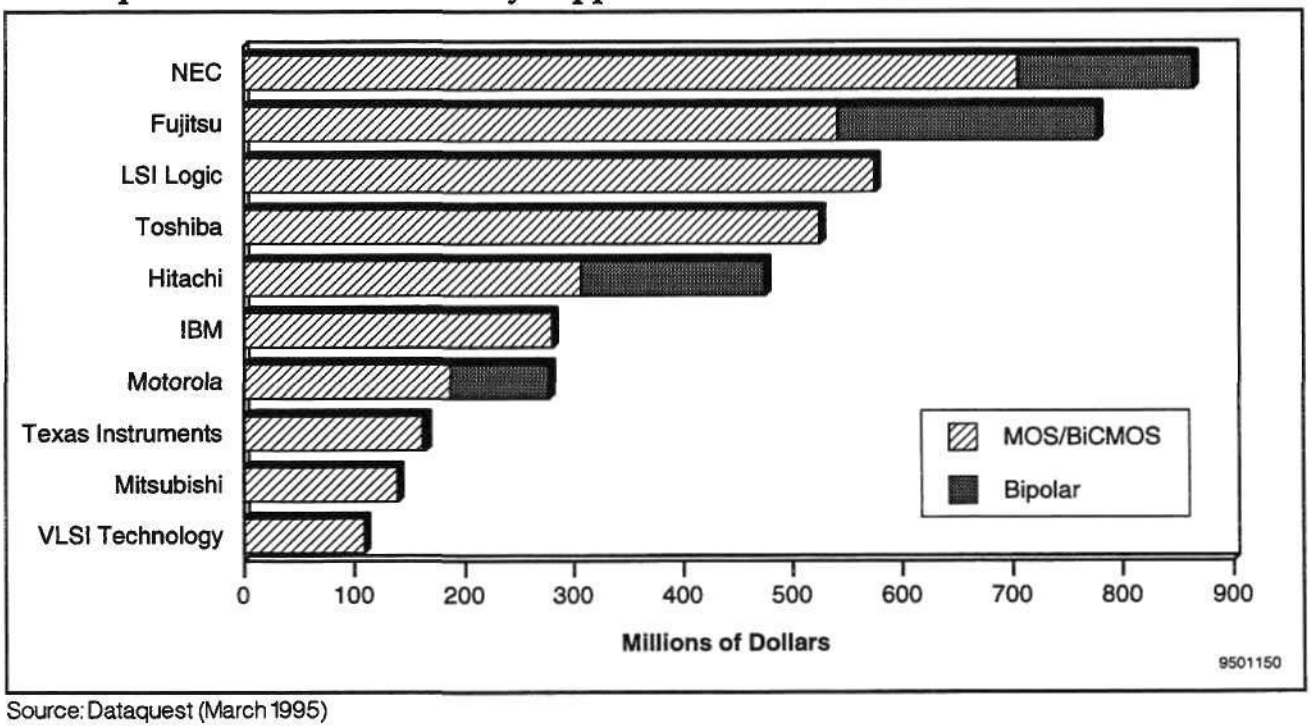
Source: Dataquest (March 1995)

Gate Arrays

The year 1994 was good for the MOS/BiCMOS gate array market, which had 19.4 percent growth, and an above-average year for bipolar gate arrays, with a 6.3 percent decline. MOS/BiCMOS gate array growth was fueled by strong market performance in personal computers/workstations and telecommunications. The bipolar gate array market was expected to decline faster than the 6 percent reported because of declining mainframe sales. Companies such as Fujitsu had a temporary increase in mainframe computer sales, which reduced the percentage decline in bipolar gate arrays.

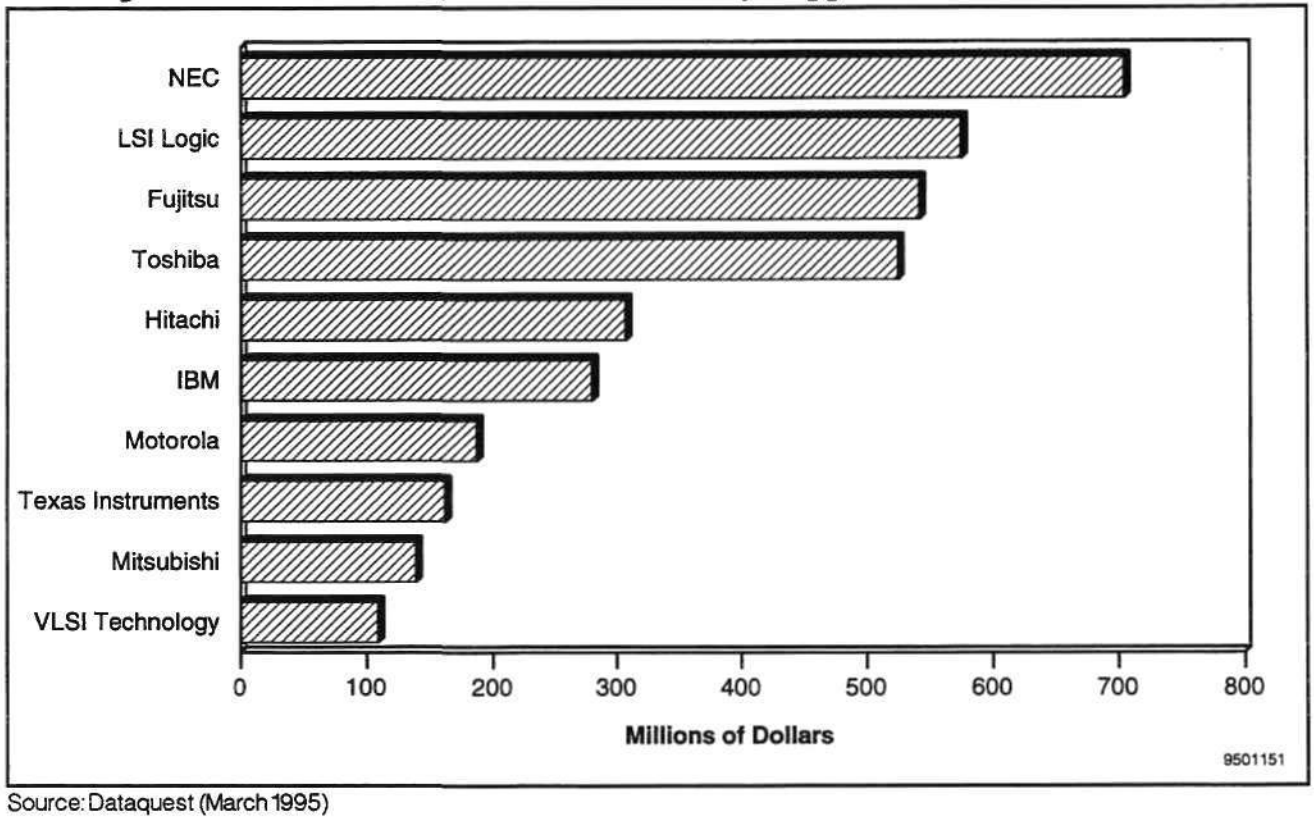
Figure 3 shows the 1994 worldwide gate array suppliers' revenue by technology of the top 10 companies. Figure 4 shows the top 10 1994 MOS/BiCMOS gate array suppliers, while Figure 5 ranks the same suppliers by

Figure 3
1994 Top 10 Worldwide Gate Array Suppliers



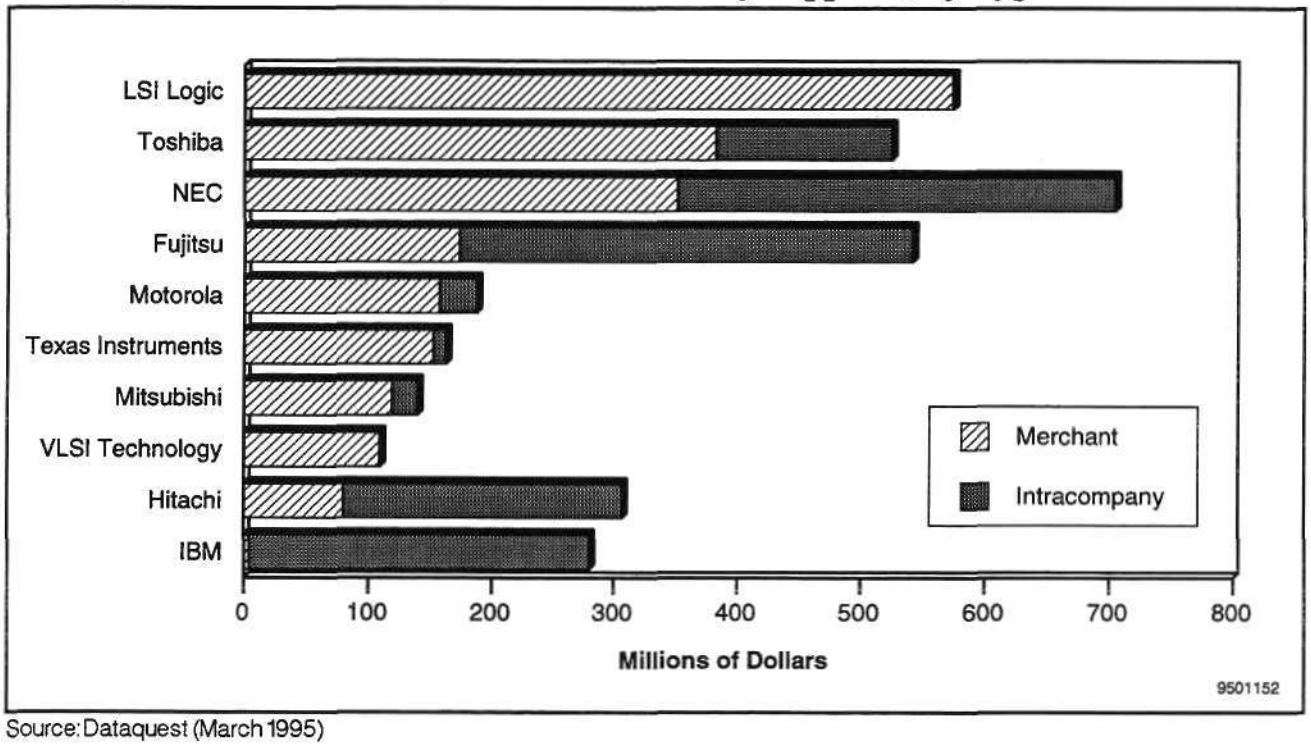
Source: Dataquest (March 1995)

Figure 4
1994 Top 10 Worldwide MOS/BiCMOS Gate Array Suppliers



Source: Dataquest (March 1995)

Figure 5
1994 Top 10 Worldwide MOS/BiCMOS Gate Array Suppliers, by Type of Sale



Source: Dataquest (March 1995)

size of estimated merchant sales. Table 3 lists the hotly contested top 20 1994 worldwide MOS gate array suppliers and their respective revenue, growth rates, and market shares. Figure 6 takes a snapshot of leading MOS/BiCMOS gate array suppliers in North America.

North America-based companies grew 9 percent in 1994 worldwide MOS/BiCMOS gate array sales, compared with 28 percent growth (including 8.4 percent yen appreciation) for Japan-based companies, 4 percent growth for Europe-based companies, and 27 percent growth for Asia/Pacific companies.

Noteworthy points regarding the 1994 gate array rankings include the following:

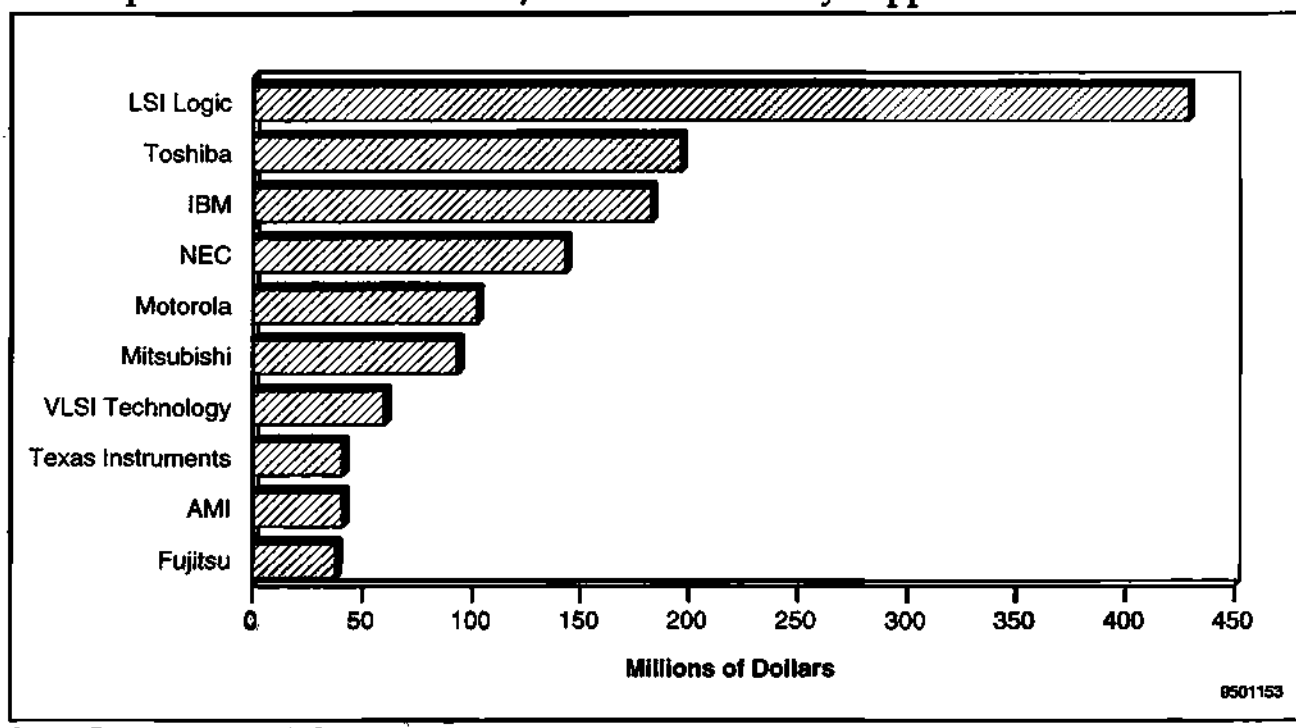
- NEC passed LSI Logic to become the No. 1 MOS/BiCMOS gate array supplier. However, a significant portion of NEC's sales are to internal divisions. LSI Logic remains the largest merchant gate array supplier, as shown in Figure 5.
- VLSI Technology had a weak year in MOS/BiCMOS gate arrays because the company focused on the CBIC market, where it had a solid year.
- Mitsubishi had an outstanding year, leaping from the No. 16 position in 1993 to No. 9 in 1994 MOS/BiCMOS gate arrays. Mitsubishi's 140 percent growth was driven by a few high-volume designs in the PC/workstation market.

Table 3
1994 Worldwide Market Share Ranking: MOS/BiCMOS Gate Array
(Millions of Dollars)

1994 Rank	1993 Rank		1993 Revenue	1994 Revenue	Percentage Change (%)	1994 Market Share (%)
1	2	NEC	550	705	28	15.6
2	1	LSI Logic	552	575	4	12.7
3	3	Fujitsu	466	542	16	12.0
4	4	Toshiba	427	525	23	11.6
5	6	Hitachi	235	307	31	6.8
6	5	IBM	243	280	15	6.2
7	7	Motorola	147	187	27	4.1
8	9	Texas Instruments	99	162	64	3.6
9	16	Mitsubishi	58	139	140	3.1
10	8	VLSI Technology	145	109	-25	2.4
11	13	Matsushita	73	95	30	2.1
12	11	Seiko Epson	80	91	14	2.0
13	10	GEC Plessey	83	88	6	1.9
14	12	SGS-Thomson	73	80	10	1.8
15	15	OKI	61	78	28	1.7
16	17	Samsung	57	68	19	1.5
17	18	Sharp	48	62	29	1.4
18	23	AMI	21	43	105	1.0
19	19	National Semiconductor	42	40	-5	0.9
20	20	Sony	25	36	44	0.8

Source: Dataquest (March 1995)

Figure 6
1994 Top 10 North American MOS/BiCMOS Gate Array Suppliers



Source: Dataquest (March 1995)

Cell-Based ICs

The CBIC market was the place to be for ASIC suppliers in 1994. MOS/BiCMOS CBICs had a record year with 28.6 percent growth. One key reason for this record growth was the increased use of CBICs in Japan, primarily by large vertically integrated Japanese companies.

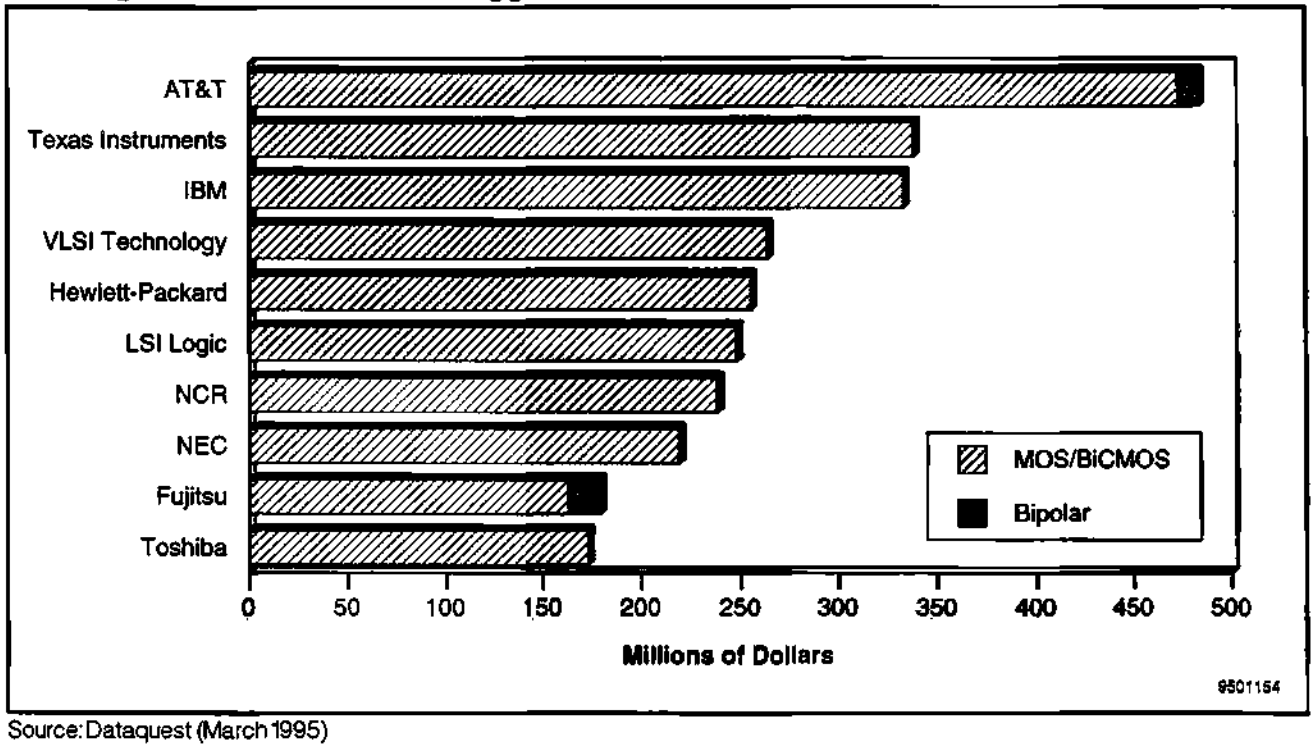
Although many North American companies had a good year in CBICs, total North America-based companies grew 23 percent in 1994 worldwide MOS/BiCMOS CBIC sales, compared with 54 percent growth for Japan-based companies, and 23 percent growth for Europe-based companies. Japan-based companies continue to target this market for future growth.

Figure 7 shows the top 10 1994 worldwide CBIC suppliers' revenue by technology. Table 4 shows the top 20 1994 worldwide MOS CBIC suppliers by their respective revenue, growth rates, and market shares. Figure 8 illustrates the top 10 worldwide MOS/BiCMOS CBIC suppliers, while Figure 9 shows the same suppliers ranked by estimated merchant sales. Figure 10 examines the top 10 1994 North American MOS/BiCMOS CBIC suppliers.

Noteworthy points regarding the 1994 CBIC rankings include the following:

- LSI Logic had a stellar year in CBICs, jumping from No. 11 in 1993 MOS/BiCMOS CBIC sales to No. 6 in 1994. LSI Logic's Core-ware products are primarily CBICs, and many previously captured computer and telecom designs moved into high-volume production in 1994.

Figure 7
1994 Top 10 Worldwide CBIC Suppliers



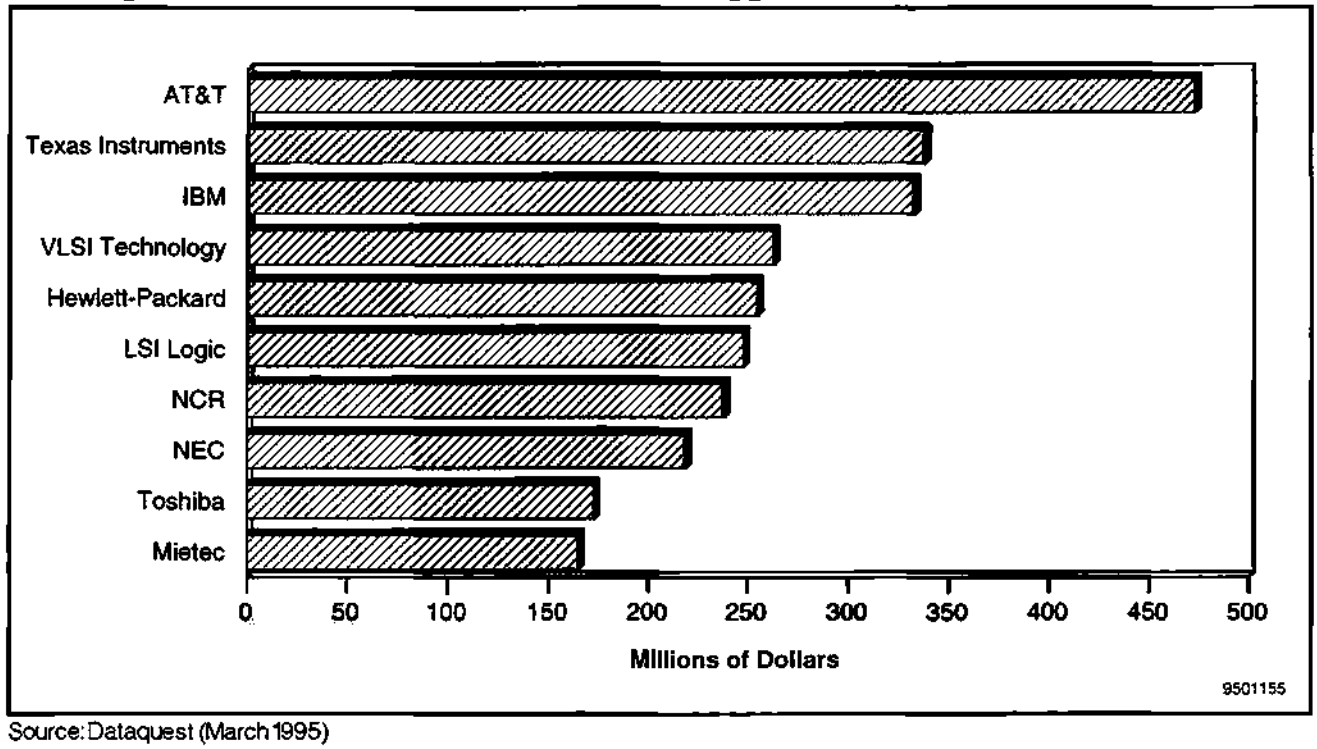
Source: Dataquest (March 1995)

Table 4
1994 Worldwide Market Share Ranking: MOS/BiCMOS Cell-Based IC (Millions of Dollars)

1994 Rank	1993 Rank		1993 Revenue	1994 Revenue	Percentage Change (%)	1994 Market Share (%)
1	1	AT&T	419	473	13	11.5
2	2	Texas Instruments	344	338	-2	8.2
3	3	IBM	297	333	12	8.1
4	5	VLSI Technology	199	263	32	6.4
5	4	Hewlett-Packard	230	255	11	6.2
6	11	LSI Logic	90	248	176	6.0
7	7	NCR	137	238	74	5.8
8	9	NEC	117	219	87	5.3
9	10	Toshiba	114	173	52	4.2
10	6	Mietec	139	165	19	4.0
11	8	Fujitsu	134	163	22	4.0
12	12	Matsushita	81	117	44	2.8
13	13	SGS-Thomson	80	113	41	2.7
14	14	Austria Mikro Systeme	67	86	28	2.1
15	18	Hitachi	39	86	121	2.1
16	15	GEC Plessey	63	67	6	1.6
17	21	OKI	35	62	77	1.5
18	17	National Semiconductor	58	58	0	1.4
19	16	Harris	62	47	-24	1.1
20	19	AMI	39	45	15	1.1

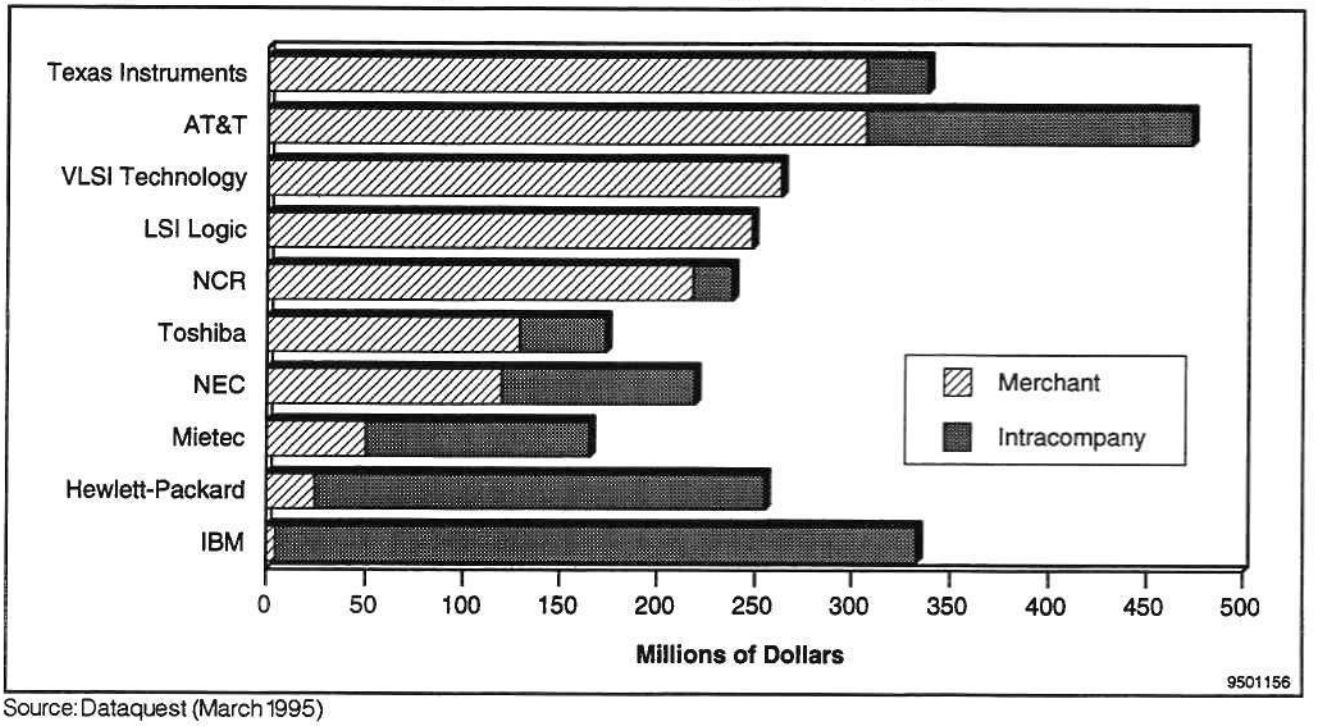
Source: Dataquest (March 1995)

Figure 8
1994 Top 10 Worldwide MOS/BiCMOS CBIC Suppliers



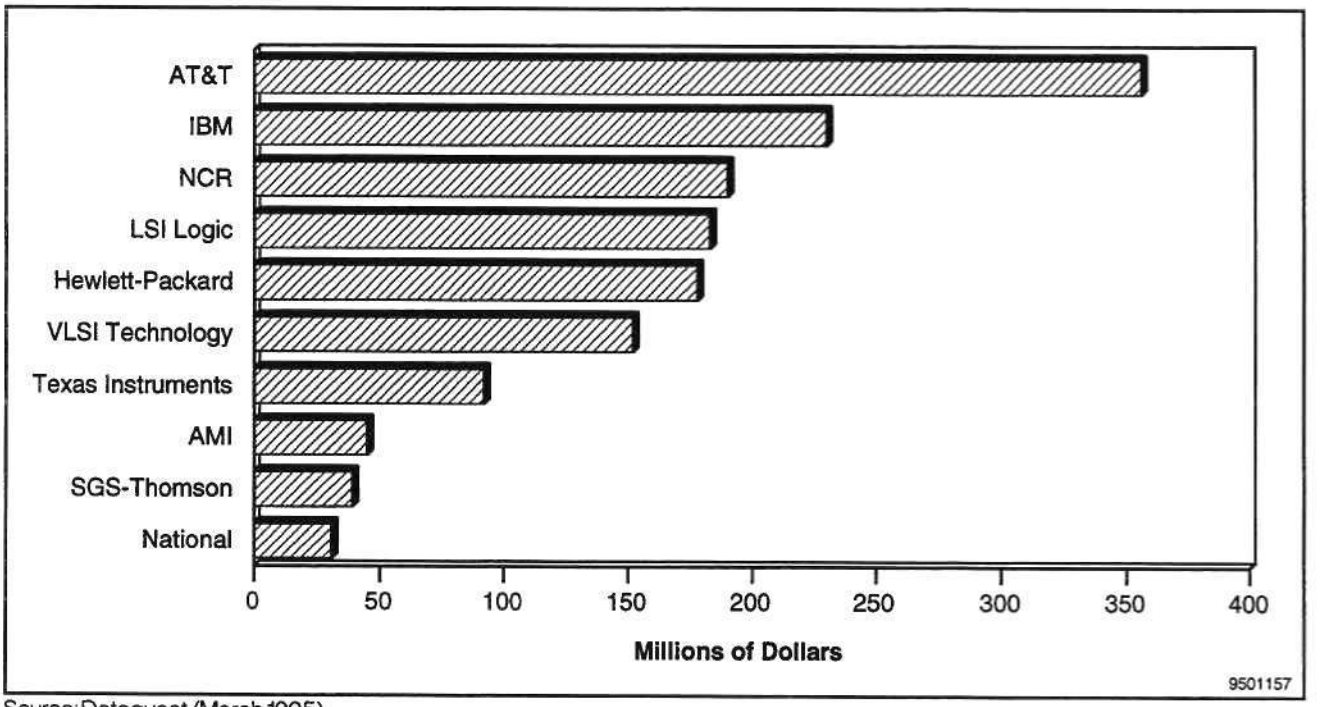
Source: Dataquest (March 1995)

Figure 9
1994 Top 10 Worldwide MOS/BiCMOS CBIC Suppliers, by Type of Sale



Source: Dataquest (March 1995)

Figure 10
1994 Top 10 North American MOS/BiCMOS CBIC Suppliers



Source: Dataquest (March 1995)

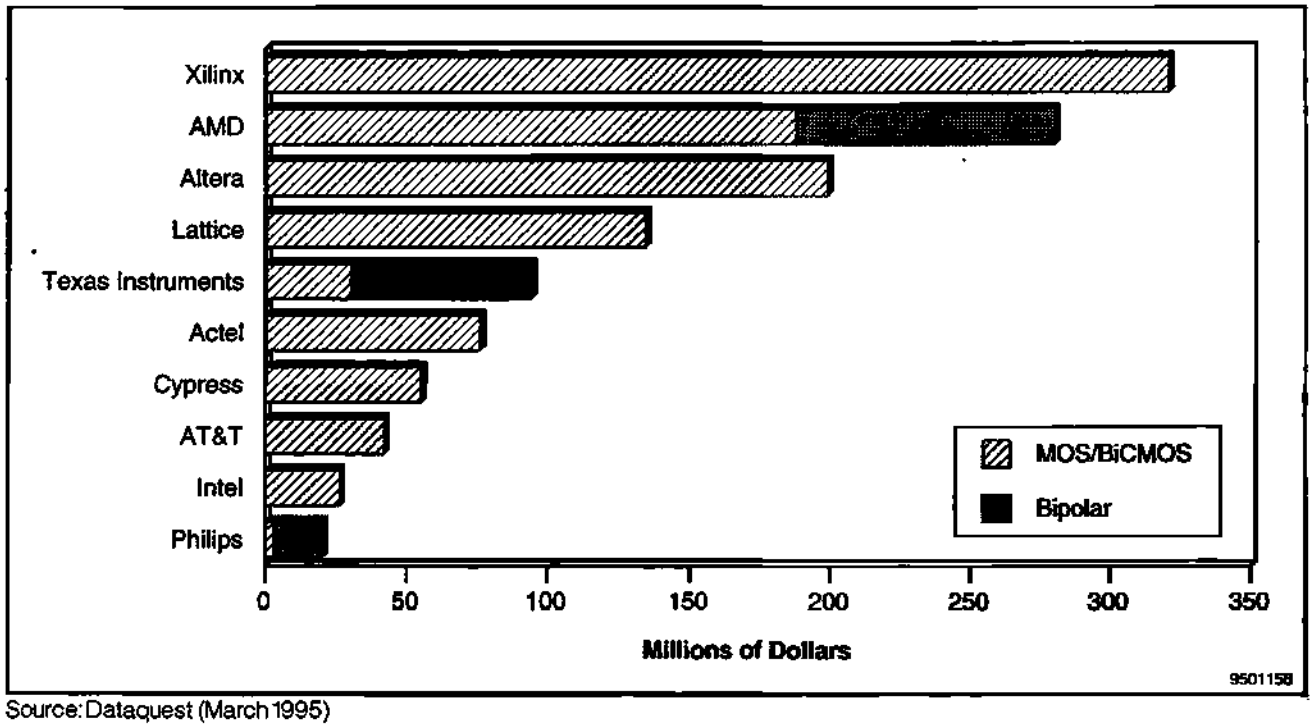
- Texas Instruments maintained its No. 2 position in CBICs. However, the company had a submarket performance in CBICs in part because it is changing its focus to gate array products. Furthermore, TI has a large portion of its CBIC sales in Japan in older designs that are starting to be phased out.
- AT&T had a good year in the merchant market and is tied with TI in 1994 merchant CBIC sales, as shown in Figure 9.
- Companies on the move in the CBIC market with high 1994 growth rates include: VLSI Technology, NCR (now called Symbios), NEC, and Toshiba.

PLDs

MOS/BiCMOS PLD growth continued at a solid pace in 1994 (22.6 percent), while bipolar PLDs had the worst year in history (down 29.4 percent). Of the MOS/BiCMOS products, CPLDs lead the pack with an annual growth rate of 45.7 percent, followed by FPGAs with 36.8 percent and SPLDs with a decline of 2.1 percent. Growth rates can be deceiving because of the differences in the dollar bases. FPGAs continued to dominate the market by growing about $121 million in 1994 for a total market of $450 million, compared to a $96 million dollar increase for CPLDs for a total market of $306 million in 1994. SPLDs declined about $8 million in 1994 for a total market of $378 million. MOS/BiCMOS PLD growth came at the expense of bipolar PLDs, which dropped $73 million for a total 1994 market of $175 million.

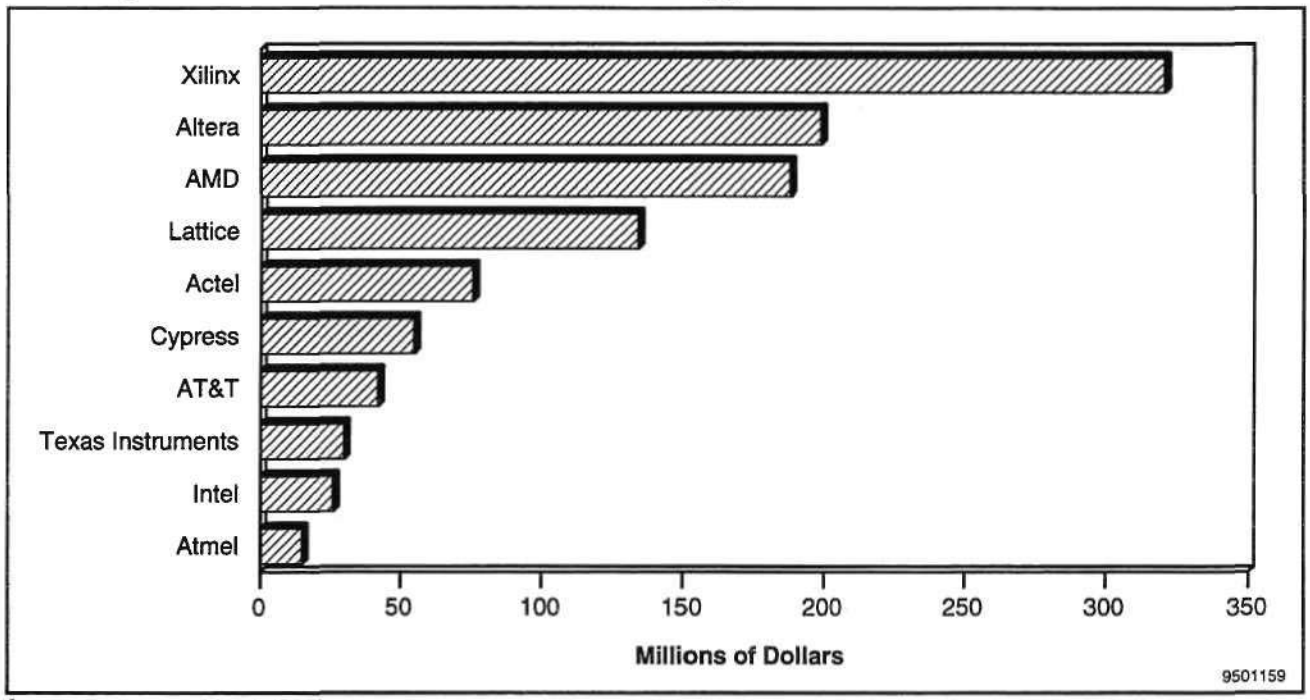
Figure 11 shows the top 10 1994 worldwide PLD suppliers' revenue by technology, while Figure 12 and Table 5 show the leaders in the hotly contested MOS/BiCMOS PLD market.

Figure 11
1994 Top 10 Worldwide PLD Suppliers



Source: Dataquest (March 1995)

Figure 12
1994 Top 10 Worldwide MOS/BiCMOS PLD Suppliers



Source: Dataquest (March 1995)

Table 5
1994 Worldwide Market Share Ranking: MOS/BiCMOS PLD (Millions of Dollars)

1994 Rank	1993 Rank		1993 Revenue	1994 Revenue	Percentage Change (%)	1994 Market Share (%)
1	1	Xilinx	231	321	39	28.3
2	3	Altera	140	199	42	17.5
3	2	Advanced Micro Devices	160	188	18	16.6
4	4	Lattice	127	134	6	11.8
5	5	Actel	60	76	27	6.7
6	6	Cypress Semiconductor	47	55	17	4.9
7	8	AT&T	32	42	31	3.7
8	9	Texas Instruments	29	30	3	2.6
9	7	Intel	45	26	-42	2.3
10	11	Atmel	12	15	25	1.3

Source: Dataquest (March 1995)

Noteworthy points regarding the 1994 PLD rankings include the following:

- Xilinx passed AMD for the No. 1 supplier in total PLDs with an exclusive MOS PLD product line.
- Altera passed AMD to capture the No. 2 position in MOS PLDs by growing 42 percent, compared to AMD's 18 percent.

- To accurately reflect the sale of Intel's PLD Division to Altera, the first three quarters of Intel's 1994 PLD revenue is included under Intel, and the last quarter's revenue is included in Altera's revenue.
- Actel outpaced the MOS PLD market in 1994 with 27 percent growth and is well-positioned with the recent acquisition of TI's FPGA business for a battle with Lattice for the No. 4 position.
- Although Lattice's MOS PLD sales only grew 6 percent in 1994, the company doubled its CPLDs sales, which helps position it for stronger growth in 1995.

Dataquest Perspective

The ASIC wave continues to grow in size and power as the 1994 market exceeded $10 billion with nearly 20 percent growth. LSI Logic, the largest merchant ASIC supplier, posted record sales and profits during 1994. LSI Logic's net income after tax (profits) increased from 7.5 percent of its 1993 sales to 12.1 percent of 1994 sales. The ASIC market is growing and is profitable for those companies that have invested in three key areas: intellectual property, value-added cell libraries, and system knowledge.

The low-density market (fewer than 20,000 gates) is now being ruled by a half dozen FPGA and CPLD suppliers that have a major patent position in device architectures. These companies enjoy rising revenue streams as well as healthy profit margins because of their intellectual property position.

On the other end of the spectrum, the high-density market (more than 100,000 gates), ASIC suppliers that have established value-added cell libraries targeted at specific applications are the most profitable. System knowledge is critical in developing complete, focused cell libraries where system designers can differentiate their systems. The market is quickly moving to system-level integration (SLI) where the entire system or subsystems can be implemented on a single chip. Such high integration requires a solid understanding of system design, design tools, library support, and test methodologies.

Cell-based ICs are gaining momentum as the preferred ASIC product for high-density designs and SLI because of their small die size. Embedded gate arrays (megacells such as SRAM diffused into the gate array base wafer) have also become a viable option for the high-end market because of their improved time to market over CBICs. As sub-0.35-micron, four- and five-layer-metal, 2-million-gate ASICs become common, we believe that CBICs will offer only minor advantages over the high utilization and quick time-to-market benefits of embedded gate arrays.

The need for system designers to differentiate their systems to achieve higher profit margins is driving the growth of the ASIC market. Although revenue will continue to grow for most ASIC suppliers, profits will only increase for those suppliers that continue to invest in intellectual property, focused cell libraries, and system knowledge.

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Perspective

ASICs Worldwide

Dataquest Predicts

Cell-Based ICs to Dominate Gate Arrays in 1998

Abstract: *Dataquest predicts that cell-based ICs will be the largest ASIC market by 1998. Dataquest also predicts that embedded arrays will account for half the gate array consumption by the year 2000. In this newsletter, Dataquest forecasts all ASIC products by technology through 1999. For more details on ASIC forecasts and assumptions, please see the ASIC Market Statistics report entitled "Worldwide ASIC Forecast," dated May 22, 1995 (ASIC-WW-MS-9502).*

By Bryan Lewis

Cell-Based ICs Strike It Rich

According to Dataquest's new ASIC forecast, total cell-based IC (CBIC) revenue is expected to surpass total gate array revenue in 1998. Furthermore, MOS CBIC revenue should exceed MOS gate array revenue in 1996.

To some, the crossover between CBIC revenue and gate array revenue may come as a great surprise. CBICs are winning in high-volume applications where cost is critical and in high-density applications where increased functionality is important. In North America and Europe, CBIC revenue has been larger than gate array revenue for some time. Japan, once the die-hard gate array nation, is now moving to CBICs to reduce cost and improve functionality. Japan's move toward CBIC technology is causing the shift in worldwide ASIC consumption from gate array to CBIC.

One important point that should be considered, when examining the ASIC product trends, is that embedded arrays (megacells such as SRAM blocks defused in the gate array base wafer) historically have been counted under the gate array category. In this newsletter, we have estimated the portion of the MOS gate array market we believe will be embedded array versus traditional gate arrays. Some ASIC suppliers have been counting embedded

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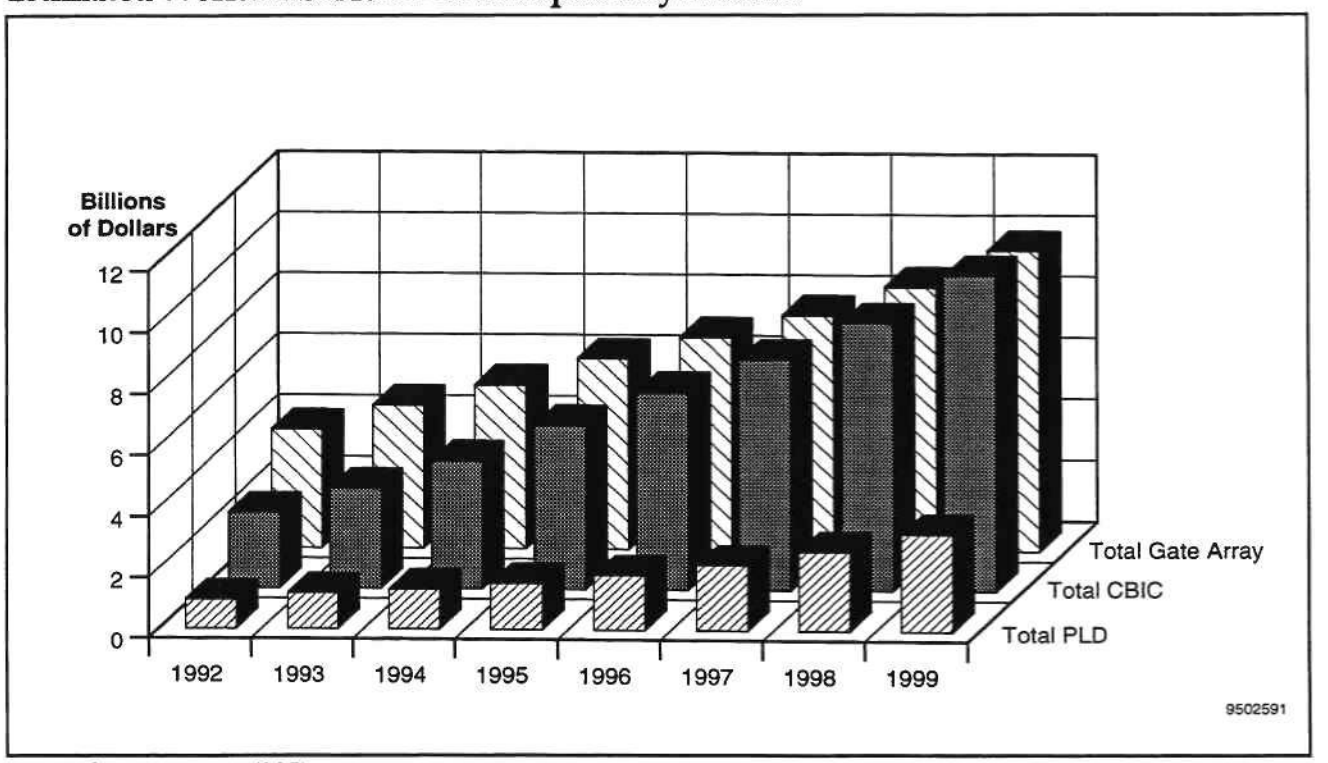
arrays under the CBIC category in their reporting to Dataquest, and we have attempted to pull this revenue out of CBICs and report it under the gate array category. It is possible that some embedded array revenue slipped into the CBIC category during market collection. To avoid this confusion, Dataquest will start breaking out embedded arrays as a separate category versus traditional arrays and CBICs in 1995 market share collection. Embedded arrays are a very competitive product to CBICs in high-volume and high-density applications.

ASIC Consumption by Product

The worldwide 1995 ASIC market is expected to experience the highest growth rate in recent history (20.7 percent, excluding full-custom ICs). Although yen appreciation against the dollar will increase 1995 dollar growth rates (we factored in 10 percent yen appreciation at the time of the forecast), we believe the ASIC market will post outstanding growth rates because of a fundamental change in the products being shipped. Leading ASIC suppliers are shifting their focus from low-value commodity gate arrays to higher-margin, value-added CBICs. CBICs had the highest growth rate of all ASIC products in 1994 (28 percent), and we believe this trend will hold true for 1995 in all regions.

Figure 1 shows ASIC consumption from 1992 through 1999 for total gate array, total CBIC, and total PLD. Table 1 shows a detailed product forecast for all the ASIC products by technology. Figure 2 illustrates the 1995 to 1996 crossover between MOS gate array and MOS CBIC on a worldwide basis, while Figure 3 illustrates the point that MOS CBIC revenue has been larger than MOS gate array revenue in North America for more than three years.

Figure 1
Estimated Worldwide ASIC Consumption by Product



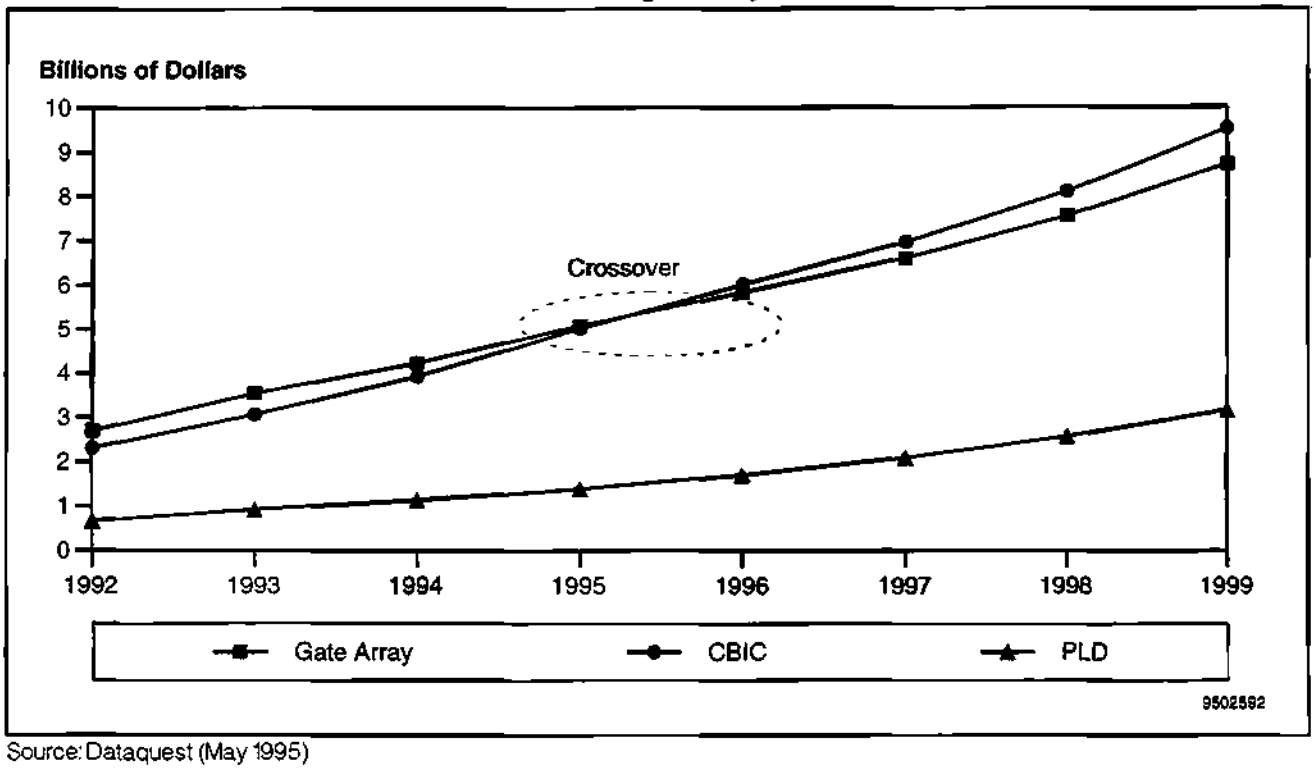
Source: Dataquest (May 1995)

Table 1
Estimated Worldwide ASIC Consumption by Technology (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Total ASIC	9,648	11,657	13,309	15,430	17,397	19,419	21,866	25,088	13.5
MOS ASIC	7,632	9,739	11,448	13,540	15,500	17,475	19,883	22,960	14.9
Bipolar ASIC	1,746	1,543	1,388	1,267	1,078	906	747	613	-15.1
BICMOS ASIC	270	375	473	623	819	1,038	1,236	1,515	26.2
Total Gate Array	3,861	4,658	5,338	6,214	6,929	7,668	8,604	9,820	13.0
MOS Gate Array	2,701	3,544	4,232	5,087	5,844	6,612	7,555	8,733	15.6
Bipolar Gate Array	969	873	818	768	642	524	412	317	-17.3
BICMOS Gate Array	191	241	288	359	443	532	637	770	21.7
Total PLD	957	1,173	1,309	1,515	1,795	2,150	2,614	3,202	19.6
MOS PLD	677	925	1,134	1,388	1,705	2,087	2,569	3,170	22.8
Bipolar PLD	280	248	175	127	90	63	45	32	-28.8
Total Cell-Based IC	2,486	3,283	4,193	5,359	6,466	7,545	8,757	10,327	19.8
MOS Cell-Based IC	2,313	3,067	3,931	5,022	6,022	6,978	8,105	9,535	19.4
Bipolar Cell-Based IC	94	82	77	73	68	61	53	47	-9.4
BICMOS Cell-Based IC	79	134	185	264	376	506	599	745	32.1
Total Full-Custom IC	2,344	2,543	2,469	2,342	2,207	2,056	1,891	1,739	-6.8
MOS Full-Custom IC	1,941	2,203	2,151	2,043	1,929	1,798	1,654	1,522	-6.7
Bipolar Full-Custom IC	403	340	318	299	278	258	237	217	-7.3

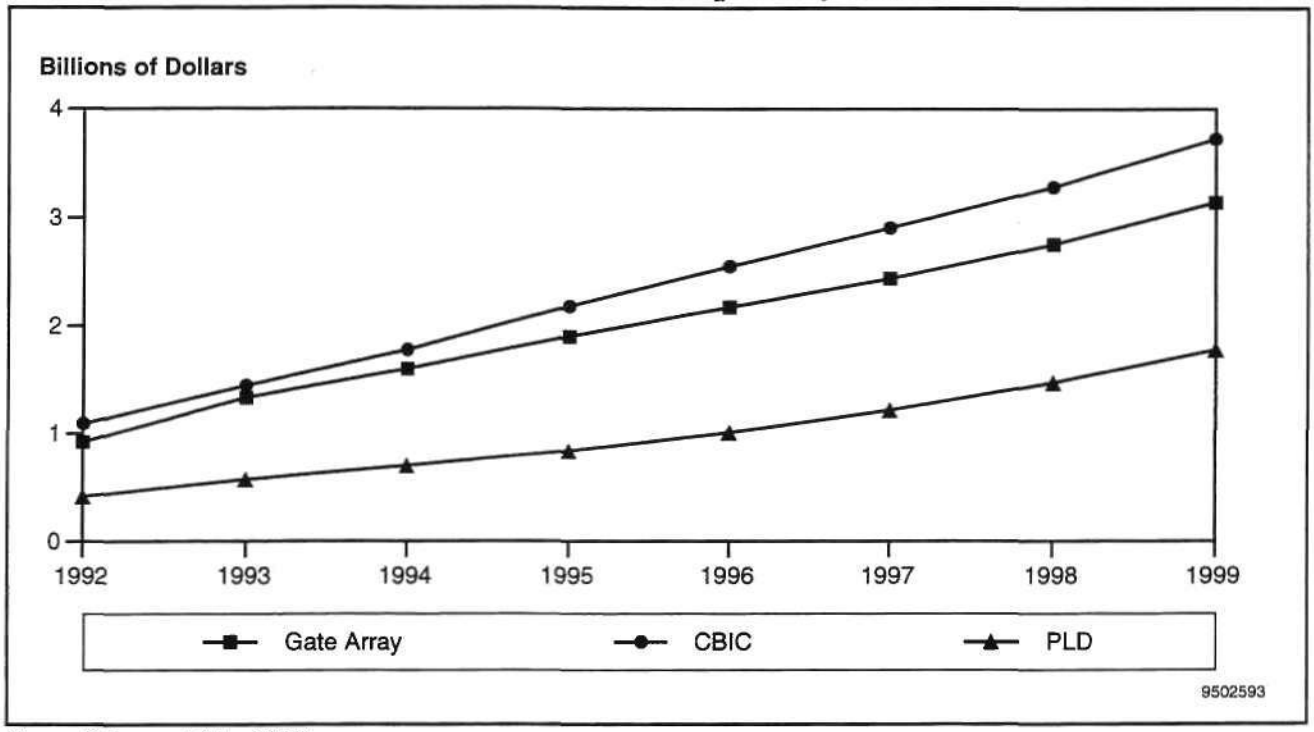
Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (May 1995)

Figure 2
Estimated Worldwide MOS ASIC Consumption by Product



Source: Dataquest (May 1995)

Figure 3
Estimated North American MOS ASIC Consumption by Product



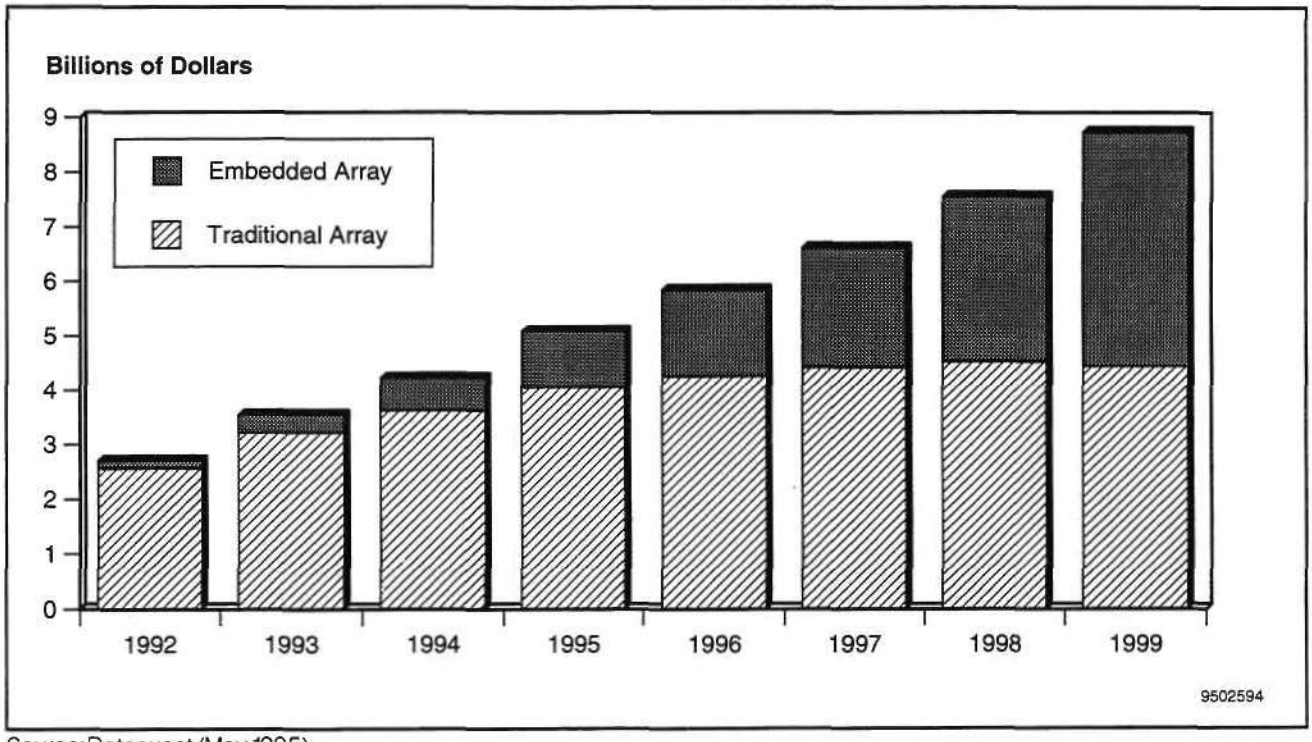
Source: Dataquest (May 1995)

Gate Array

Although CBIC growth rates are higher than those of gate array, we still expect strong gate array growth in 1995. The worldwide MOS gate array market is expected to grow 20.2 percent in 1995, compared with the 19.4 percent experienced in 1994. Part of the increase is because of the strong yen appreciation against the dollar. MOS gate array revenue growth by region in 1995 is forecast as follows: almost 19 percent increase for North America, 24 percent increase for Japan, 7 percent increase for Europe, and 27 percent increase for Rest of World (ROW). Europe is expected to experience a very high growth rate in CBICs at the expense of gate arrays.

As mentioned, embedded arrays are counted under the gate array category. Our belief is that embedded arrays will experience rapid growth over the next five years (see Figure 4). Embedded arrays offer the reduced turnaround times of gate arrays, along with the increased functionality of CBICs. Traditional sea-of-gates gate array growth will flatten out over the next three years, then decline because they are being squeezed by PLDs on the low end (fewer than 20,000 gates) and embedded arrays and CBICs on the high end (more than 100,000 gates). Furthermore, Dataquest predicts that about half the gate arrays consumed in the year 2000 will be embedded arrays.

Figure 4
Estimated Worldwide MOS Gate Array Consumption by Product



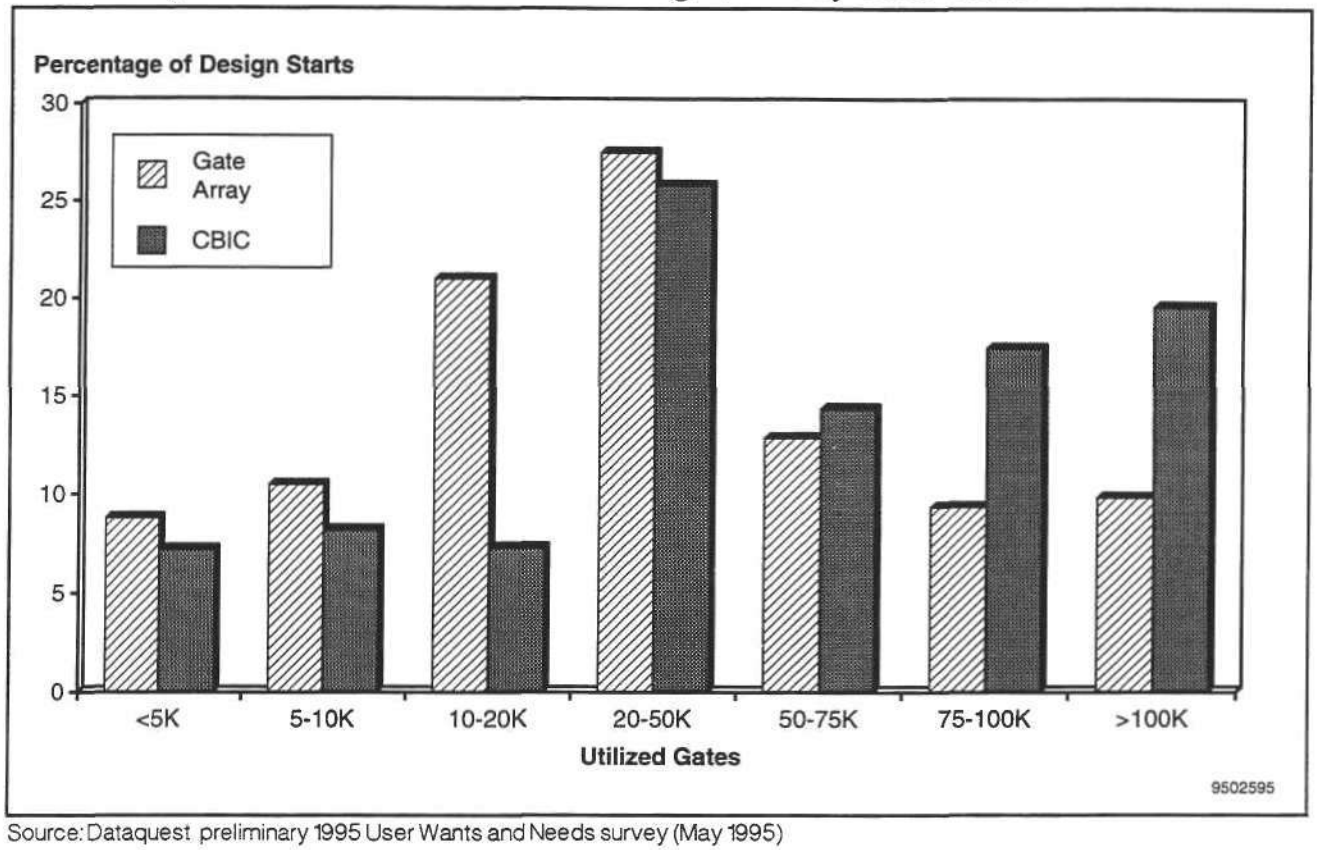
Source: Dataquest (May 1995)

Cell-Based ICs

Worldwide 1995 MOS CBIC growth is expected to be the highest of all the ASIC products (27.7 percent). MOS CBIC revenue growth by region in 1995 is forecast as follows: 22.5 percent increase for North America, 34 percent increase for Japan, 32.9 percent increase for Europe, and 26 percent increase for ROW. The shift in focus from gate array to CBIC in Japan is increasing the worldwide MOS CBIC growth rate and causing the 1996 crossover in revenue from gate array to CBIC.

Strong CBIC growth is a result of CBICs winning the battle with gate arrays in high-volume and high-density applications. According to preliminary results from our 1995 User Wants and Needs survey of more than 650 system designers in North America, Japan, and Europe, CBICs have a higher percentage of designs with greater than 100,000 usable gates. Figure 5 shows preliminary 1995 North American ASIC design starts by gate count by product. CBICs clearly are winning the battle above 100,000 usable gates.

Figure 5
Preliminary 1995 North American ASIC Design Starts by Gate Count



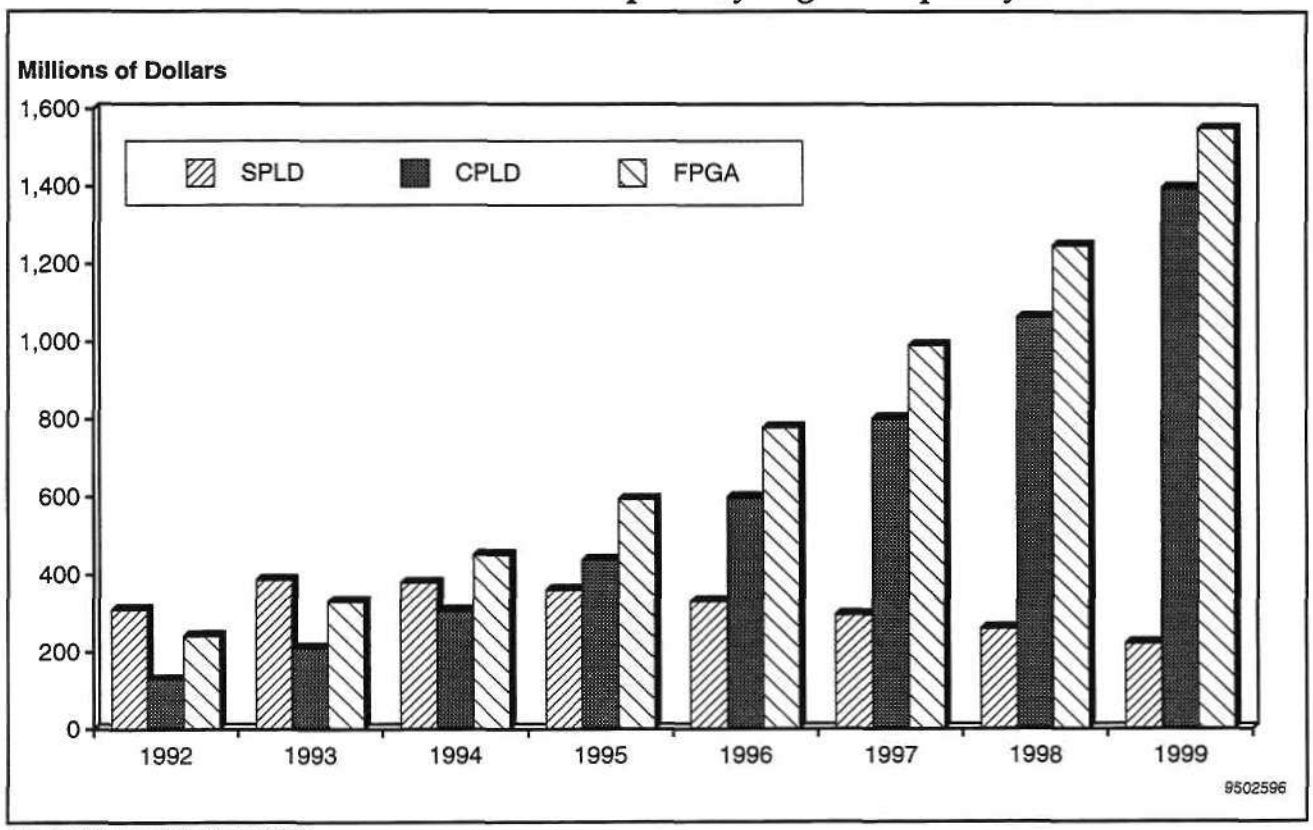
Source: Dataquest preliminary 1995 User Wants and Needs survey (May 1995)

PLDs

Worldwide MOS PLD growth in 1995 is expected to be very similar to that of 1994 (22.4 percent in 1995 versus 22.6 percent in 1994). On a regional basis, we are expecting about 20 percent growth in North America, 32.5 percent in Japan, 21.5 percent in Europe, and 32.2 percent in ROW. The MOS PLD dollar base in North America and Europe is quite large in comparison to Japan and ROW, and therefore it is much more difficult for these regions to experience growth rates in the 30 percent range.

Key products contributing to the growth of the PLD market are field-programmable gate arrays (FPGAs) and complex PLDs (CPLDs). We expect 31.8 percent growth in 1995 for FPGAs and 42.4 percent growth for CPLDs. Contrasting with these two rapidly growing segments is a 5.1 percent decline in simple PLDs (SPLDs), which are being swept into high-density programmable logic. FPGA and CPLD growth stems from the replacement of standard logic, SPLDs, and low-end gate arrays (fewer than 20,000 gates). Figure 6 illustrates the size of the worldwide MOS PLD market by logic complexity.

Figure 6
Estimated Worldwide MOS PLD Consumption by Logic Complexity



Source: Dataquest (May 1995)

Dataquest Perspective

The year 1995 will be outstanding for the ASIC market. Many ASIC suppliers posted record sales, bookings, and profits during the first quarter of 1995. We believe that 1995 ASIC growth rates will be the highest in recent history. High ASIC growth rates are being fueled by booming electronic equipment markets coupled with the need for systems integration and system differentiation.

Dataquest predicts that traditional gate arrays will start to decline in revenue within three years as they wrestle with PLDs for the low-density/low-volume business and with CBICs for the cost-sensitive business such as video games, printers, and disk drives. Furthermore, we predict that embedded array will account for half the gate array revenue by the year 2000. Embedded arrays and CBICs will battle for the largest pot of gold, namely the high-volume and high-density market. Each market can be profitable for suppliers with the appropriate intellectual property and system knowledge.

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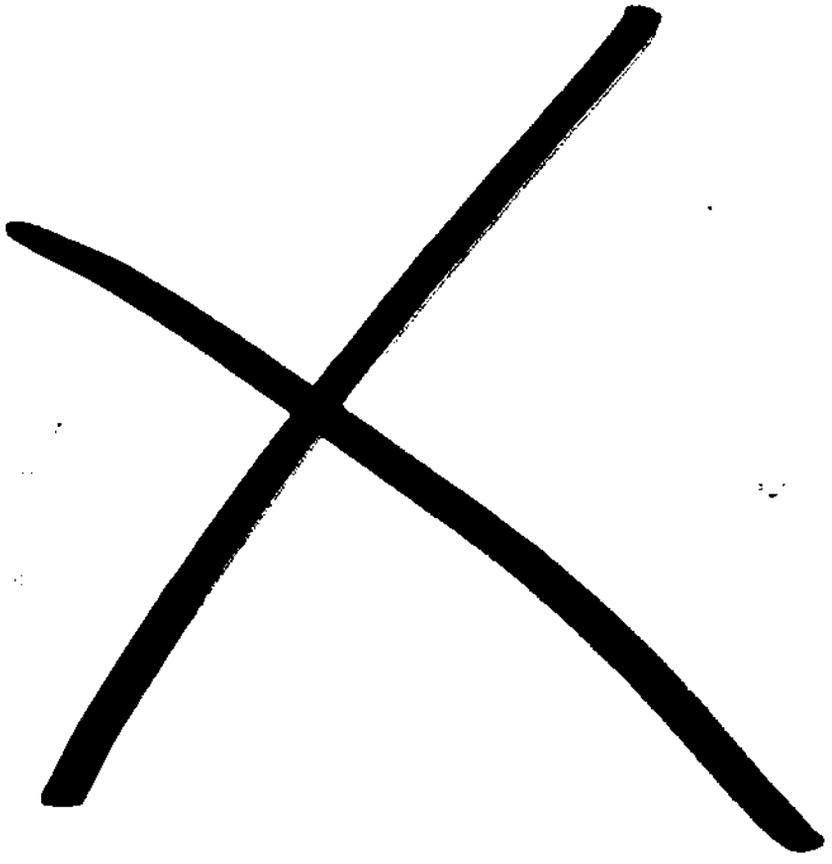
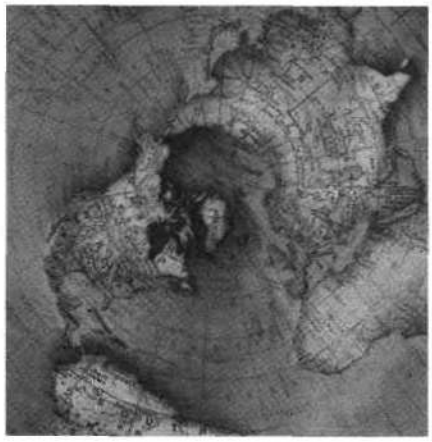


Market Analysis

Dataquest



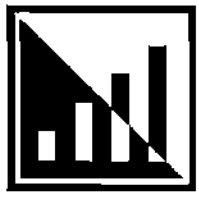
Dataquest

Worldwide ASIC Forecast

Market Statistics

Program: ASICs Worldwide
Product Code: ASIC-WW-MS-9503
Publication Date: October 23, 1995
Filing: Market Analysis

Worldwide ASIC Forecast



Market Statistics

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Note: All tables show estimated data.

Worldwide ASIC Forecast

Introduction

This document contains detailed information on Dataquest's view of the application-specific integrated circuit (ASIC) market. Included in this document are the following:

- 1995-1999 ASIC consumption forecast
- 1995-1999 gate array consumption forecast
- 1995-1999 cell-based IC (CBIC) consumption forecast
- 1995-1999 programmable logic device (PLD) consumption forecast

More detailed data on this market may be requested through Dataquest's client inquiry service. Qualitative analysis of this data is provided in the Dataquest Market Trends and other documents located in the binder of the same name.

Segmentation

This section outlines the market segments that are specific to this document. Dataquest's objective is to provide data along lines of segmentation that are logical, appropriate to the industry in question, and immediately useful to clients.

Dataquest defines the ASIC market according to the segmentation scheme in Figure 1.

Figure 1 shows Dataquest's segmentation into the two main categories of standard logic and ASIC. The ASIC family tree breaks out ASICs as follows: PLDs, gate arrays, CBICs, and full-custom ICs. CBICs and full-custom ICs are personalized by altering the full set of masks, whereas PLDs and gate arrays are personalized by electrically programming the devices or by altering only the final layers of interconnect. ASICs are further classified according to process technology: MOS, bipolar, and BiCMOS.

Definitions

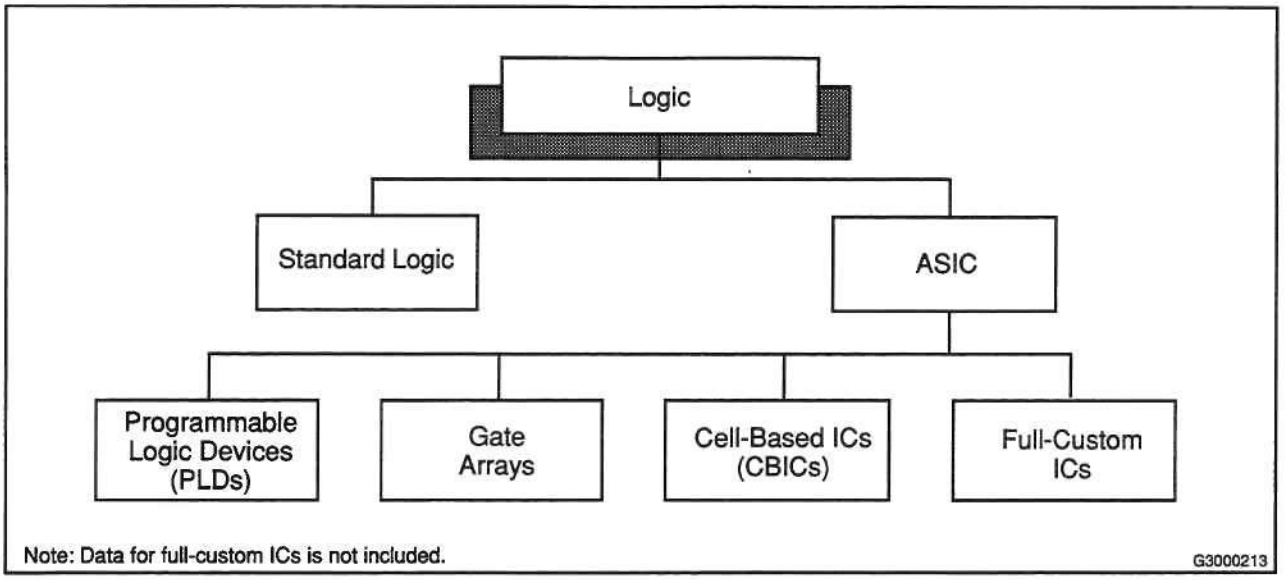
This section lists the definitions used by Dataquest to present the data in this document.

Product Definitions

Application-Specific Integrated Circuits (ASICs)

This term is used to describe all IC products customized for a single user. ASIC products are a combination of digital, mixed-signal, and analog products. Customized ICs purchased by more than one user become standard products and are no longer counted as ASICs.

Figure 1
ASIC Family Tree



Source: Dataquest (April 1995)

Programmable Logic Devices (PLDs)

PLDs are defined as ICs programmed after assembly. Memory devices such as PROMs and ROMs are not included in this market segment. PLDs are subdivided into three main categories:

- Simple programmable logic devices (SPLDs): SPLDs have fixed or preconnected architectures capable of providing up to two levels of logic without using additional input, output, or I/O cells or pins.
- Complex programmable logic devices (CPLDs): CPLDs are product-term or segmented PAL-based devices that may or may not implement multiple levels of logic without using additional input, output, or I/O cells or pins.
- Field-programmable gate arrays (FPGAs): FPGAs are based on segmented programmable interconnect and typically consist of an X-Y matrix of logic modules typically fed by a limited number of preconnected signals.

Gate Arrays

Gate arrays are ASICs that contain a configuration of uncommitted elements in a prefabricated base wafer. They are customized by interconnecting these elements with one or more routing layers. Included in this category are traditional gate arrays (channeled and sea-of-gates architecture) and embedded gate arrays (channeled or sea-of-gates architecture that also include megacells such as SRAM diffused into the gate array base wafer).

CBICs

CBICs are ASICs that are customized using a full set of masks and use automatic place-and-route tools. Included in this category are traditional standard cells (fixed-height/fixed-width cells) as well as megacells (variable-height/variable-width cells) and compiled cells.

Full-custom ICs

Full-custom ICs are defined as ASIC devices that are produced for a single user using a full set of masks. This process involves manual routing and placement of cells.

Revenue Classification

Because systems may be fabricated, assembled, and sold in several different locations, Dataquest's regional device consumption is defined according to the shipping destination.

Consumption estimates include the following five sources of revenue:

- Intracompany revenue (sales to internal divisions)
- Nonrecurring engineering (NRE) revenue
- ASIC software revenue
- PLD development kit revenue
- Device production revenue

Despite the care taken in gathering, analyzing, and categorizing the data in a meaningful way, careful attention must be paid to the definitions and assumptions used herein when interpreting the estimates presented in this document. Various companies, government agencies, and trade associations may use slightly different definitions of product categories and regional groupings, or they may include different companies in their summaries. These differences should be kept in mind when making comparisons between data and numbers provided by Dataquest and those provided by other suppliers.

Merchant versus Captive Consumption

Dataquest includes all revenue, both merchant and captive, for semiconductor suppliers selling to the merchant market. Dataquest's consumption estimates do not include captive-only manufacturing companies represented by companies such as Digital Equipment Corporation, Northern Telecom, or Unisys that do not sell semiconductor products in the merchant market.

Regional Definitions

North America: Includes Canada, Mexico, and the United States

Europe: Western Europe and eastern Europe

Japan: Japan

Asia/Pacific-Rest of World: All other countries

Forecast Methodology and Assumptions

Dataquest publishes five-year factory revenue forecasts for the ASIC market during the first and third quarter of each year. In doing so, Dataquest utilizes a variety of forecasting techniques (both qualitative and quantitative) that vary by technology area. An overview of Dataquest forecasting techniques can be found in the Dataquest Research Methodology guides.

ASIC Forecast Methodology

Dataquest's forecast methodology includes the following steps:

- Formally and informally survey the leading ASIC vendors (in gate arrays, CBICs, and PLDs) throughout the year for their expectations, as well as for their views of the application markets in which they participate
- Formally survey ASIC users for their expected buying patterns, in addition to their views on the growth of the application markets in which they participate
- Examine statistics provided by a number of industry and government organizations (such as the World Semiconductor Trade Statistics, the Japanese Ministry of International Trade and Industry, and the U.S. Department of Commerce) for up-to-date monthly trends
- Perform time-series analysis as well as apply judgmental industry knowledge to product and application trends

ASIC Forecast Assumptions

ASIC

The worldwide 1995 ASIC market is expected to experience the highest growth rate in recent history (23.7 percent, excluding full-custom ICs). Although yen appreciation against the dollar will increase the 1995 dollar growth rate of the ASIC market (we factored in about 10 percent yen appreciation at the time of the forecast), we believe the market will post outstanding growth rates because of a fundamental change in the products being shipped. Leading ASIC suppliers are shifting their focus from low-value commodity gate arrays to higher margin, value-added cell-based ICs. Cell-based ICs had the highest growth rate of all ASIC products in 1994 (30.4 percent), and we believe this trend will hold true for 1995 in all regions. Furthermore, Dataquest predicts the size of the worldwide cell-based IC market to surpass that of the gate array market by 1998, and for it to become the largest ASIC market.

Gate Arrays

MOS Gate Arrays

CMOS continues to be the dominant gate array technology for the foreseeable future because of its low cost, low power consumption, and high integration.

The North American CMOS gate array market will closely track the computer market because more than 60 percent of all gate arrays are consumed in data processing applications.

The Japanese MOS gate array market continues to see severe price erosion. However, margins will improve as Japanese companies start to invest in unique cell libraries to gain intellectual property.

The low-end CMOS market (fewer than 20,000 gates) will continue to be adversely impacted by field-programmable gate arrays (FPGAs).

Embedded gate arrays (that is, megacells such as SRAMs that are diffused in the array base wafer) are included in the gate array category and are expected to fuel gate array growth by the mid- to late 1990s.

Although we believe that the price per gate will continue to drop, average selling prices (ASPs) still are expected to rise because of the increasing use of on-chip functions such as SRAM, ALU, multiplier, multiplier-accumulator, FIFO, DMA controller, cache controller, and 82XX microperipherals.

Bipolar Gate Arrays

Bipolar gate arrays are being replaced by CMOS, BiCMOS, and GaAs ASICs because of their high cost and high power consumption. The TTL gate array market is declining, primarily because there have been no new TTL arrays designed in the past three years, and production of these devices is accordingly winding down.

The ECL gate array market is declining at a rapid rate in all regions because most ECL arrays are consumed in large mainframe and supercomputers, which are declining markets.

BiCMOS Gate Arrays

BiCMOS gate array growth has been lowered substantially from our previous forecast because of the lack of high-volume production from vertically integrated companies such as Fujitsu, NEC, and AT&T. At this point, the costs of these BiCMOS devices do not outweigh the benefits from BiCMOS in comparison to CMOS. According to Dataquest's worldwide end-user survey of more than 500 systems designers, demand for BiCMOS ASICs in their next-generation systems design is dropping significantly from two years ago.

Cell-Based ICs

MOS CBICs

There will be an increased use of CBICs in North America in high-density applications (greater than 100,000 gates) and/or high-volume applications (greater than 50,000 units a year) such as dataprocessing, telecom, and consumer.

There will be an increasing use of CBICs in Japan (at the expense of gate arrays) in high-volume applications such as video games, printers, and disk drives, mainly because of the smaller die size of CBICs. CBICs are also penetrating high-complexity applications in Japan such as computers and HDTV.

Telecom applications are driving the CBIC growth in Europe.

Bipolar CBICs

Bipolar CBIC growth stems from two product types: ECL CBICs and analog CBICs. ECL CBICs are expected to experience negative growth, primarily because system designers do not want macros supplied by

ASIC vendors; they want to design their own macros on the transistor level to optimize their designs for their unique applications.

Analog CBICs, such as National's "Classic" line, are expected to experience flat to modest growth.

BiCMOS CBICs

BiCMOS CBICs are a good solution for mixed analog/digital applications. The analog portion can be implemented using bipolar technology and the digital portion with CMOS technology.

BiCMOS CBICs are expected to be used in many telecommunications applications.

PLDs

CMOS PLDs

CMOS PLD growth stems from three types of devices: simple PLDs (SPLDs), complex PLDs (CPLDs), and field-programmable gate arrays (FPGAs). The critical element for the success of all three device types is the time to market.

The SPLD market is expected to experience negative growth rates during the next few years. The current market is driven by the conversion from bipolar SPLDs and standard logic. However, the decline in growth will accelerate as these small devices are replaced with higher-density CPLDs and FPGAs, which can now match all but the fastest SPLDs for particular functions.

Dataquest believes that CPLDs will continue to grow faster than the semiconductor industry. The CPLD growth rate has outpaced the FPGA growth rate for the last five years and will continue to do so for the duration of this forecast. However, FPGA total dollars remain higher than CPLD dollars and are expected to remain higher through 1998. Although CPLDs hold a slight ease-of-use and speed advantage over FPGAs, FPGAs have traditionally offered higher gate counts (than CPLDs), which users are demanding for future system design. As CPLDs and FPGAs approach similar density and functionality, we expect the CPLD growth and FPGA growth to stabilize just beyond 1998.

The FPGA market is expected to show excellent growth over the next five years for the following reasons:

- The shift continues from TTL- and PAL-based designs toward FPGA usage.
- FPGAs will attack not only the low-end gate array market (fewer than 10,000 gates), but also the 10,000- to 40,000-gate array market in the 1995 to 1997 time frame as prices drop and gate array vendors migrate to higher-density devices.
- Additional market impetus will come from the introduction of new architectures in 1995 and 1996. New entrants into the market may also contribute to increased growth.

Dataquest believes that FPGAs will encounter increased price competition in the 1994 to 1996 time frame as lagging suppliers try to buy market share and entrenched competitors shore up their positions.

The factors influencing CMOS PLD growth are as follows (by region):

- Europe: Designs here tend to favor lower volume and lower gate counts, a category that PLDs fit well. As a result, PLD growth will continue to be strong.
- Japan: PLDs will penetrate internal development and play a significant role in prototyping, increasing growth.
- North America: The U.S. market is maturing, and concomitant decrease in growth rates will ensue.
- ROW: As design expertise increases, demand for CPLD and FPGA products will also increase.

Bipolar PLDs

The PC boom ended in 1993, and with it the surge in bipolar PLD sales. The ensuing negative growth will again help bipolar PLDs to resume the previous market dynamics; the bipolar PLD market will decline as users shift from bipolar PLDs to MOS PLDs. Furthermore, we believe that the bipolar PLD market will continue to decline until only a few high-speed ECL devices and specialty high-drive PLDs remain.

Exchange Rates

Dataquest used an average annual exchange rate in converting revenue to U.S. dollar amounts. Table 1 outlines these rates for 1992 through 1994. The 1995 rates are based on a weighted average.

Table 1
Exchange Rates

	1992	1993	1994	1995
Japan (Yen/U.S.$)	126.45	112.20	101.96	88.48
France (Franc/U.S.$)	5.27	5.67	5.91	4.92
Germany (Deutsche Mark/U.S.$)	1.56	1.66	1.74	1.41
United Kingdom (U.S.$/Sterling Pound)	1.77	1.50	1.49	0.63
European Community (U.S.$/ECU)	0.770	0.858	0.896	0.76

Source: Dataquest (May 1995)

Table 2
Estimated Worldwide ASIC Consumption by Product (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Total ASIC	9,648	11,657	13,309	15,749	17,783	19,948	22,535	25,927	14.3
MOS ASIC	7,632	9,739	11,448	13,817	15,870	17,992	20,543	23,793	15.8
Bipolar ASIC	1,746	1,543	1,388	1,288	1,094	918	756	619	-14.9
BICMOS ASIC	270	375	473	644	819	1,038	1,236	1,515	26.2
Total Gate Array	3,861	4,658	5,338	6,237	6,963	7,706	8,640	9,859	13.1
MOS Gate Array	2,701	3,544	4,232	5,089	5,862	6,638	7,582	8,767	15.7
Bipolar Gate Array	969	873	818	789	658	536	421	323	-17.0
BICMOS Gate Array	191	241	288	359	443	532	637	769	21.7
Total PLD	957	1,173	1,309	1,704	2,061	2,521	3,109	3,845	24.0
MOS PLD	677	925	1,134	1,577	1,971	2,458	3,064	3,813	27.4
Bipolar PLD	280	248	175	127	90	63	45	32	-28.8
Total Cell-Based IC	2,486	3,283	4,193	5,466	6,552	7,665	8,895	10,484	20.1
MOS Cell-Based IC	2,313	3,067	3,931	5,108	6,108	7,098	8,243	9,691	19.8
Bipolar Cell-Based IC	94	82	77	73	68	61	53	47	-9.4
BICMOS Cell-Based IC	79	134	185	285	376	506	599	746	32.2
Total Full-Custom IC	2,344	2,543	2,469	2,342	2,207	2,056	1,891	1,739	-6.8
MOS Full-Custom IC	1,941	2,203	2,151	2,043	1,929	1,798	1,654	1,522	-6.7
Bipolar Full-Custom IC	403	340	318	299	278	258	237	217	-7.3

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1995)

Table 3
Estimated Worldwide ASIC Consumption by Product (Percentage Growth)

	1992	1993	1994	1995	1996	1997	1998	1999
Total ASIC	1.4	20.8	14.2	18.3	12.9	12.2	13.0	15.1
MOS ASIC	3.7	27.6	17.5	20.7	14.9	13.4	14.2	15.8
Bipolar ASIC	-9.3	-11.6	-10.0	-7.2	-15.0	-16.1	-17.7	-18.1
BICMOS ASIC	16.4	38.9	26.1	36.2	27.2	26.7	19.1	22.6
Total Gate Array	-1.4	20.6	14.6	16.8	11.6	10.7	12.1	14.1
MOS Gate Array	1.1	31.2	19.4	20.3	15.2	13.2	14.2	15.6
Bipolar Gate Array	-9.8	-9.9	-6.3	-3.5	-16.6	-18.5	-21.5	-23.3
BICMOS Gate Array	13.0	26.2	19.5	24.7	23.4	20.1	19.7	20.7
Total PLD	6.1	22.6	11.6	30.2	21.0	22.3	23.3	23.7
MOS PLD	21.1	36.6	22.6	39.1	25.0	24.7	24.7	24.4
Bipolar PLD	-18.4	-11.4	-29.4	-27.4	-29.1	-30.0	-28.6	-28.9
Total Cell-Based IC	10.1	32.1	27.7	30.4	19.9	17.0	16.0	17.9
MOS Cell-Based IC	10.0	32.6	28.2	29.9	19.6	16.2	16.1	17.6
Bipolar Cell-Based IC	2.2	-12.8	-6.1	-5.2	-6.8	-10.3	-13.1	-11.3
BICMOS Cell-Based IC	25.4	69.6	38.1	54.1	31.9	34.6	18.4	24.5
Total Full-Custom IC	-4.1	8.5	-2.9	-5.1	-5.8	-6.9	-8.0	-8.0
MOS Full-Custom IC	-4.4	13.5	-2.4	-5.0	-5.6	-6.8	-8.0	-8.0
Bipolar Full-Custom IC	-3.0	-15.6	-6.5	-6.0	-6.9	-7.4	-8.2	-8.2

Source: Dataquest (October 1995)

Table 4
Estimated Worldwide ASIC Consumption by Technology (Millions of Dollars and Percentage of Revenue)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Total ASIC	9,648	11,657	13,309	15,749	17,783	19,948	22,535	25,927	14.3
MOS ASIC	7,632	9,739	11,448	13,817	15,870	17,992	20,543	23,793	15.8
Bipolar ASIC	1,746	1,543	1,388	1,288	1,094	918	756	619	-14.9
BICMOS ASIC	270	375	473	644	819	1,038	1,236	1,515	26.2
Total ASIC (%)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	
MOS ASIC (%)	79.1	83.5	86.0	87.7	89.2	90.2	91.2	91.8	
Bipolar ASIC (%)	18.1	13.2	10.4	8.2	6.2	4.6	3.4	2.4	
BICMOS ASIC (%)	2.8	3.2	3.6	4.1	4.6	5.2	5.5	5.8	

Source: Dataquest (October 1995)

Table 5
Estimated Worldwide ASIC Consumption by Region (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total ASIC	7,304	9,114	10,840	13,407	15,577	17,892	20,642	24,189
MOS ASIC	5,691	7,536	9,297	11,774	13,940	16,194	18,888	22,272
Bipolar ASIC	1,343	1,203	1,070	989	817	660	518	401
BICMOS ASIC	270	375	473	644	820	1,038	1,235	1,515
North America	3,168	3,943	4,562	5,532	6,369	7,266	8,321	9,616
MOS ASIC	2,501	3,346	4,070	5,082	5,970	6,904	7,980	9,272
Bipolar ASIC	609	528	408	346	269	205	150	111
BICMOS ASIC	58	69	84	104	130	157	190	233
Japan	2,326	2,810	3,435	4,327	4,919	5,464	6,144	7,051
MOS ASIC	1,650	2,164	2,725	3,547	4,147	4,694	5,362	6,223
Bipolar ASIC	547	486	507	518	444	369	297	234
BICMOS ASIC	129	160	203	262	329	401	485	595
Western Europe	1,370	1,592	1,860	2,301	2,691	3,125	3,555	4,131
MOS ASIC	1,130	1,304	1,569	1,952	2,297	2,650	3,043	3,544
Bipolar ASIC	163	158	131	111	92	75	62	49
BICMOS ASIC	77	130	160	238	302	399	450	539
ROW	440	769	983	1,247	1,598	2,037	2,622	3,390
MOS ASIC	410	722	933	1,193	1,527	1,946	2,504	3,234
Bipolar ASIC	24	31	24	14	12	10	9	7
BICMOS ASIC	6	16	26	40	59	81	109	149

Note: Columns may not add to totals shown because of rounding. Full-Custom ICs are excluded from this table.
Source: Dataquest (October 1995)

Table 6
Estimated Worldwide ASIC Consumption by Region (Percentage Growth)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Worldwide Total ASIC	3.3	24.8	18.9	23.7	16.2	14.9	15.4	17.2	17.4
North America	5.4	24.5	15.7	21.3	15.1	14.1	14.5	15.6	16.1
Japan	-6.1	20.8	22.2	26.0	13.7	11.1	12.4	14.8	15.5
Western Europe	8.5	16.2	16.8	23.7	17.0	16.1	13.8	16.2	17.3
ROW	34.1	74.8	27.8	26.8	28.2	27.5	28.7	29.3	28.1
Worldwide MOS ASIC	6.7	32.4	23.4	26.6	18.4	16.2	16.6	17.9	19.1
North America	10.0	33.8	21.6	24.9	17.5	15.6	15.6	16.2	17.9
Japan	-3.6	31.2	25.9	30.2	16.9	13.2	14.2	16.1	18.0
Western Europe	8.3	15.4	20.3	24.4	17.6	15.4	14.8	16.5	17.7
ROW	34.9	76.1	29.2	27.8	28.0	27.5	28.6	29.2	28.2
Worldwide Bipolar ASIC	-11.0	-10.4	-11.1	-7.6	-17.4	-19.2	-21.4	-22.6	-17.8
North America	-10.3	-13.3	-22.7	-15.2	-22.3	-23.6	-26.8	-26.1	-22.9
Japan	-15.6	-11.2	4.3	2.2	-14.3	-16.8	-19.6	-21.2	-14.3
Western Europe	1.2	-3.1	-17.1	-15.4	-16.5	-18.7	-17.6	-20.6	-17.8
ROW	14.3	29.2	-22.6	NA	NA	NA	NA	NA	NA
Worldwide BICMOS ASIC	16.4	38.9	26.1	36.1	27.3	26.6	19.0	22.6	26.2
North America	11.5	19.0	21.7	23.8	24.8	20.8	21.3	22.6	22.7
Japan	9.3	24.0	26.9	29.1	25.5	22.0	21.0	22.6	24.0
Western Europe	30.5	68.8	23.1	48.7	26.9	32.1	12.9	19.6	27.5
ROW	100.0	166.7	62.5	53.2	47.8	37.4	35.3	35.7	41.7

Note: Full-custom ICs are excluded from this table.
NA = Not available
Source: Dataquest (October 1995)

Table 7
Estimated Worldwide ASIC Consumption by Region (Percentage of Revenue)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total ASIC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	43.4	43.3	42.1	41.3	40.9	40.6	40.3	39.8
Japan	31.8	30.8	31.7	32.3	31.6	30.5	29.8	29.2
Western Europe	18.8	17.5	17.2	17.2	17.3	17.5	17.2	17.1
ROW	6.0	8.4	9.1	9.3	10.3	11.4	12.7	14.0
Worldwide MOS ASIC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	43.9	44.4	43.8	43.2	42.8	42.6	42.3	41.6
Japan	29.0	28.7	29.3	30.1	29.7	29.0	28.4	27.9
Western Europe	19.9	17.3	16.9	16.6	16.5	16.4	16.1	15.9
ROW	7.2	9.6	10.0	10.1	11.0	12.0	13.3	14.5
Worldwide Bipolar ASIC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	45.3	43.9	38.1	35.0	32.9	31.1	29.0	27.7
Japan	40.7	40.4	47.4	52.4	54.3	56.0	57.3	58.3
Western Europe	12.1	13.1	12.2	11.2	11.3	11.4	11.9	12.3
ROW	1.8	2.6	2.2	1.4	1.5	1.5	1.8	1.8
Worldwide BICMOS ASIC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	21.5	18.4	17.8	16.2	15.8	15.1	15.4	15.4
Japan	47.8	42.7	42.9	40.7	40.1	38.6	39.3	39.3
Western Europe	28.5	34.7	33.8	37.0	36.9	38.5	36.5	35.5
ROW	2.2	4.3	5.5	6.2	7.2	7.8	8.9	9.8

Note: Columns may not add to totals shown because of rounding. Full-custom ICs are excluded from this table.
Source: Dataquest (October 1995)

Table 8
Estimated Worldwide Gate Array Consumption by Technology (Millions of Dollars and Percentage of Revenue)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Total ASIC	9,648	11,657	13,309	15,749	17,783	19,948	22,535	25,927	14.3
Total Gate Array	3,861	4,658	5,338	6,237	6,963	7,706	8,640	9,859	13.1
MOS Gate Array	2,701	3,544	4,232	5,089	5,862	6,638	7,582	8,767	15.7
Bipolar Gate Array	969	873	818	789	658	536	421	323	-17.0
BICMOS Gate Array	191	241	288	359	443	532	637	769	21.7
Total Gate Array (%)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	
MOS Gate Array (%)	70.0	76.1	79.3	81.6	84.2	86.1	87.8	88.9	
Bipolar Gate Array (%)	25.1	18.7	15.3	12.7	9.4	7.0	4.9	3.3	
BICMOS Gate Array (%)	4.9	5.2	5.4	5.8	6.4	6.9	7.4	7.8	

Source: Dataquest (October 1995)

Table 9
Estimated Worldwide Gate Array Consumption by Region (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total Gate Array	3,861	4,658	5,338	6,237	6,963	7,706	8,640	9,859
MOS Gate Array	2,701	3,544	4,232	5,089	5,862	6,638	7,582	8,767
Bipolar Gate Array	969	873	818	789	658	536	421	323
BICMOS Gate Array	191	241	288	359	443	532	637	769
North America	1,423	1,728	1,923	2,144	2,374	2,602	2,889	3,263
MOS Gate Array	992	1,333	1,596	1,832	2,094	2,350	2,655	3,030
Bipolar Gate Array	379	337	259	231	180	135	94	65
BICMOS Gate Array	52	58	68	82	100	117	140	168
Japan	1,699	1,950	2,331	2,823	3,094	3,347	3,668	4,093
MOS Gate Array	1,081	1,361	1,677	2,113	2,400	2,667	2,995	3,405
Bipolar Gate Array	498	446	475	485	417	350	284	224
BICMOS Gate Array	120	143	179	226	277	330	390	464
Western Europe	529	635	640	703	769	839	915	1,009
MOS Gate Array	426	517	533	602	675	749	824	914
Bipolar Gate Array	89	89	84	74	62	51	43	34
BICMOS Gate Array	14	29	23	27	32	39	48	61
ROW	210	345	444	566	727	918	1,167	1,496
MOS Gate Array	202	333	426	541	693	873	1,108	1,418
Bipolar Gate Array	3	1	0	0	0	0	0	0
BICMOS Gate Array	5	11	18	25	34	45	59	78

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1995)

Table 10
Estimated Worldwide Gate Array Consumption by Region (Percentage Growth)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Worldwide Total Gate Array	-1.4	20.6	14.6	16.8	11.7	10.7	12.1	14.1	13.1
North America	1.3	21.4	11.3	11.5	10.7	9.6	11.0	12.9	11.2
Japan	-7.8	14.8	19.5	21.1	9.6	8.2	9.6	11.6	11.9
Western Europe	6.2	20.0	0.8	9.9	9.3	9.1	9.1	10.2	9.5
ROW	25.0	64.3	28.7	27.5	28.4	26.3	27.1	28.2	27.5
Worldwide MOS Gate Array	1.1	31.2	19.4	20.2	15.2	13.2	14.2	15.6	15.7
North America	4.8	34.4	19.7	14.8	14.3	12.2	13.0	14.1	13.7
Japan	-7.1	25.9	23.2	26.0	13.6	11.1	12.3	13.7	15.2
Western Europe	6.5	21.4	3.1	13.0	12.0	11.0	10.0	11.0	11.4
ROW	25.5	64.9	27.9	27.0	28.0	26.0	27.0	28.0	27.2
Worldwide Bipolar Gate Array	-9.8	-9.9	-6.3	-3.5	-16.5	-18.6	-21.5	-23.2	-17.0
North America	-7.6	-11.1	-23.1	-11.0	-22.0	-25.0	-30.0	-31.0	-24.1
Japan	-12.5	-10.4	6.5	2.0	-14.0	-16.0	-19.0	-21.0	-14.0
Western Europe	-2.2	0	-5.6	-11.9	-16.2	-17.7	-15.7	-20.9	-16.5
ROW	-25.0	-66.7	-100.0	NA	NA	NA	NA	NA	NA
Worldwide BICMOS Gate Array	13.0	26.2	19.5	24.7	23.4	20.0	19.7	20.9	21.7
North America	8.3	11.5	17.2	20.0	22.0	18.0	19.0	20.0	19.8
Japan	8.1	19.2	25.2	26.0	23.0	19.0	18.0	19.0	21.0
Western Europe	100.0	107.1	-20.7	17.0	19.0	22.0	24.0	25.0	21.4
ROW	66.7	120.0	63.6	40.0	36.0	32.0	30.0	32.0	34.0

NA = Not available

Source: Dataquest (October 1995)

Table 11
Estimated Worldwide Gate Array Consumption by Region (Percentage of Revenue)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total Gate Array	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	36.9	37.1	36.0	34.4	34.1	33.8	33.4	33.1
Japan	44.0	41.9	43.7	45.3	44.4	43.4	42.5	41.5
Western Europe	13.7	13.6	12.0	11.3	11.0	10.9	10.6	10.2
ROW	5.4	7.4	8.3	9.1	10.4	11.9	13.5	15.2
Worldwide MOS Gate Array	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	36.7	37.6	37.7	36.0	35.7	35.4	35.0	34.6
Japan	40.0	38.4	39.6	41.5	41.0	40.2	39.5	38.8
Western Europe	15.8	14.6	12.6	11.8	11.5	11.3	10.9	10.4
ROW	7.5	9.4	10.1	10.6	11.8	13.1	14.6	16.2
Worldwide Bipolar Gate Array	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	39.1	38.6	31.7	29.2	27.3	25.2	22.4	20.2
Japan	51.4	51.1	58.1	61.4	63.3	65.3	67.4	69.3
Western Europe	9.2	10.2	10.3	9.4	9.4	9.5	10.2	10.5
ROW	0.3	0.1	0	0	0	0	0	0
Worldwide BICMOS Gate Array	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	27.2	24.1	23.6	22.7	22.5	22.1	22.0	21.8
Japan	62.8	59.3	62.2	62.8	62.6	62.1	61.2	60.2
Western Europe	7.3	12.0	8.0	7.5	7.2	7.3	7.6	7.9
ROW	2.6	4.6	6.3	7.0	7.7	8.5	9.2	10.1

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1995)

Table 12
Estimated Worldwide Cell-Based IC Consumption by Technology (Millions of Dollars and Percentage of Revenue)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Total ASIC	9,648	11,657	13,309	15,749	17,783	19,948	22,535	25,927	14.3
Total Cell-Based IC	2,486	3,283	4,193	5,466	6,552	7,665	8,895	10,484	20.1
MOS Cell-Based IC	2,313	3,067	3,931	5,108	6,108	7,098	8,243	9,691	19.8
Bipolar Cell-Based IC	94	82	77	73	68	61	53	47	-9.4
BICMOS Cell-Based IC	79	134	185	285	376	506	599	746	32.2
Total Cell-Based IC (%)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	
MOS Cell-Based IC (%)	93.0	93.4	93.8	93.5	93.2	92.6	92.7	92.4	
Bipolar Cell-Based IC (%)	3.8	2.5	1.8	1.3	1.0	0.8	0.6	0.4	
BICMOS Cell-Based IC (%)	3.2	4.1	4.4	5.2	5.7	6.6	6.7	7.1	

Source: Dataquest (October 1995)

Table 13
Estimated Worldwide Cell-Based IC Consumption by Region (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total Cell-Based IC	2,486	3,283	4,193	5,466	6,552	7,665	8,895	10,484
MOS Cell-Based IC	2,313	3,067	3,931	5,108	6,108	7,098	8,243	9,691
Bipolar Cell-Based IC	94	82	77	73	68	61	53	47
BICMOS Cell-Based IC	79	134	185	285	376	506	599	746
North America	1,155	1,499	1,837	2,311	2,698	3,070	3,468	3,936
MOS Cell-Based IC	1,094	1,443	1,775	2,246	2,628	2,995	3,384	3,841
Bipolar Cell-Based IC	55	45	46	43	40	36	33	30
BICMOS Cell-Based IC	6	11	16	22	30	39	50	65
Japan	540	739	965	1,307	1,583	1,827	2,128	2,526
MOS Cell-Based IC	507	701	922	1,254	1,517	1,745	2,024	2,388
Bipolar Cell-Based IC	24	21	19	17	14	11	9	7
BICMOS Cell-Based IC	9	17	24	36	51	71	96	131
Western Europe	629	728	976	1,320	1,596	1,898	2,172	2,552
MOS Cell-Based IC	551	611	827	1,096	1,312	1,525	1,759	2,064
Bipolar Cell-Based IC	15	16	12	13	14	13	11	10
BICMOS Cell-Based IC	63	101	137	211	270	360	402	478
ROW	162	317	415	527	676	869	1,126	1,469
MOS Cell-Based IC	161	312	407	513	651	834	1,075	1,398
Bipolar Cell-Based IC	0	0	0	0	0	0	0	0
BICMOS Cell-Based IC	1	5	8	15	25	36	51	71

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1995)

Table 14
Estimated Worldwide Cell-Based IC Consumption by Region (Percentage Growth)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Worldwide Total Cell-Based IC	10.1	32.1	27.7	30.3	19.9	17.0	16.0	17.9	20.1
North America	10.2	29.8	22.5	25.8	16.7	13.8	12.9	13.5	16.5
Japan	5.1	36.9	30.6	35.5	21.1	15.4	16.5	18.7	21.2
Western Europe	8.1	15.7	34.1	35.2	20.9	18.9	14.5	17.5	21.2
ROW	42.1	95.7	30.9	27.1	28.1	28.6	29.5	30.4	28.8
Worldwide MOS Cell-Based IC	10.0	32.6	28.2	29.9	19.6	16.2	16.1	17.6	19.8
North America	10.5	31.9	23.0	26.5	17.0	14.0	13.0	13.5	16.7
Japan	5.8	38.3	31.5	36.0	21.0	15.0	16.0	18.0	21.0
Western Europe	6.0	10.9	35.4	32.5	19.7	16.2	15.3	17.3	20.1
ROW	41.2	93.8	30.4	26.0	27.0	28.0	29.0	30.0	28.0
Worldwide Bipolar Cell-Based IC	2.2	-12.8	-6.1	-5.6	-6.2	-10.9	-13.2	-11.7	-9.6
North America	1.9	-18.2	2.2	-5.7	-7.0	-9.7	-10.0	-9.0	-8.3
Japan	-14.3	-12.5	-9.5	-12.0	-15.0	-20.0	-25.0	-23.0	-19.1
Western Europe	50.0	6.7	-25.0	5.0	8.0	-5.0	-12.0	-11.0	-3.3
ROW	NA	NA	NA	NA	NA	NA	NA	NA	NA
Worldwide BICMOS Cell-Based IC	25.4	69.6	38.1	53.8	32.2	34.5	18.3	24.5	32.1
North America	50.0	83.3	45.5	40.0	35.0	30.0	28.0	30.0	32.5
Japan	28.6	88.9	41.2	52.0	41.0	38.0	35.0	37.0	40.5
Western Europe	21.2	60.3	35.6	54.0	28.0	33.3	11.7	18.9	28.4
ROW	NA	400.0	60.0	83.0	68.0	45.0	42.0	40.0	54.7

NA = Not available

Source: Dataquest (October 1995)

Table 15
Estimated Worldwide Cell-Based IC Consumption by Region (Percentage of Revenue)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total Cell-Based IC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	46.5	45.7	43.8	42.3	41.2	40.1	39.0	37.5
Japan	21.7	22.5	23.0	23.9	24.2	23.8	23.9	24.1
Western Europe	25.3	22.2	23.3	24.1	24.4	24.8	24.4	24.3
ROW	6.5	9.7	9.9	9.7	10.3	11.3	12.7	14.0
Worldwide MOS Cell-Based IC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	47.3	47.0	45.2	44.0	43.0	42.2	41.1	39.6
Japan	21.9	22.9	23.5	24.5	24.8	24.6	24.6	24.6
Western Europe	23.8	19.9	21.0	21.5	21.5	21.5	21.3	21.3
ROW	7.0	10.2	10.4	10.0	10.7	11.7	13.0	14.4
Worldwide Bipolar Cell-Based IC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	58.5	54.9	59.7	59.7	59.2	60.0	62.2	64.1
Japan	25.5	25.6	24.7	23.0	20.9	18.7	16.2	14.1
Western Europe	16.0	19.5	15.6	17.3	20.0	21.3	21.6	21.8
ROW	0	0	0	0	0	0	0	0
Worldwide BICMOS Cell-Based IC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	7.6	8.2	8.6	7.9	8.0	7.8	8.4	8.8
Japan	11.4	12.7	13.0	12.8	13.7	14.0	16.0	17.6
Western Europe	79.7	75.4	74.1	74.2	71.8	71.2	67.1	64.1
ROW	1.3	3.7	4.3	5.1	6.5	7.0	8.5	9.5

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1995)

Table 16
Estimated Worldwide PLD Consumption by Technology (Millions of Dollars and Percentage of Revenue)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Total ASIC	9,648	11,657	13,309	15,749	17,783	19,948	22,535	25,927	14.3
Total PLD	957	1,173	1,309	1,704	2,061	2,521	3,109	3,845	24.0
MOS PLD	677	925	1,134	1,577	1,971	2,458	3,064	3,813	27.4
Bipolar PLD	280	248	175	127	90	63	45	32	-28.8
Total PLD (%)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	
MOS PLD (%)	70.7	78.9	86.6	92.5	95.6	97.5	98.6	99.2	
Bipolar PLD (%)	29.3	21.1	13.4	7.5	4.4	2.5	1.4	0.8	

Source: Dataquest (October 1995)

Table 17
Estimated Worldwide PLD Consumption by Region (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total PLD	957	1,173	1,309	1,704	2,061	2,521	3,109	3,845
MOS PLD	677	925	1,134	1,577	1,971	2,458	3,064	3,813
Bipolar PLD	280	248	175	127	90	63	45	32
North America	590	716	802	1,077	1,298	1,593	1,964	2,417
MOS PLD	415	570	699	1,005	1,249	1,559	1,941	2,401
Bipolar PLD	175	146	103	72	49	34	23	16
Japan	87	121	139	197	242	290	348	433
MOS PLD	62	102	126	180	229	282	343	429
Bipolar PLD	25	19	13	17	13	8	5	3
Western Europe	212	229	244	278	327	388	468	570
MOS PLD	153	176	209	254	310	377	460	565
Bipolar PLD	59	53	35	24	17	11	8	5
ROW	68	107	124	153	195	250	329	425
MOS PLD	47	77	100	139	183	240	320	418
Bipolar PLD	21	30	24	14	12	10	9	7

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1995)

Table 18
Estimated Worldwide PLD Consumption by Region (Percentage Growth)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Worldwide Total PLD	6.1	22.6	11.6	30.2	20.9	22.3	23.3	23.7	24.0
North America	6.9	21.4	12.0	34.2	20.5	22.8	23.3	23.1	24.7
Japan	-28.1	39.1	14.9	41.7	22.8	19.8	20.0	24.3	25.5
Western Europe	15.8	8.0	6.6	14.0	17.5	18.7	20.5	22.0	18.5
ROW	47.8	57.4	15.9	23.3	27.5	28.2	31.7	29.1	27.9
Worldwide MOS PLD	21.1	36.6	22.6	39.1	25.0	24.7	24.7	24.5	27.5
North America	23.1	37.3	22.6	43.7	24.3	24.8	24.5	23.7	28.0
Japan	-11.4	64.5	23.5	42.9	27.2	23.1	21.6	25.1	27.8
Western Europe	24.4	15.0	18.8	21.5	22.0	21.5	22.1	22.9	22.0
ROW	62.1	63.8	29.9	38.9	31.7	31.1	33.3	30.6	33.1
Worldwide Bipolar PLD	-18.4	-11.4	-29.4	-27.3	-28.9	-30.0	-29.3	-29.5	-29.0
North America	-18.6	-16.6	-29.5	-30.1	-32.6	-29.9	-32.4	-30.4	-31.1
Japan	-51.0	-24.0	-31.6	30.8	-23.5	-38.5	-37.5	-32.0	-23.5
Western Europe	-1.7	-10.2	-34.0	-30.9	-30.2	-33.4	-33.0	-33.0	-32.1
ROW	23.5	42.9	-20.0	-41.7	-14.3	-16.7	-8.2	-22.7	-21.6

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1995)

Table 19
Estimated Worldwide PLD Consumption by Region (Percentage of Revenue)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total PLD	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	61.7	61.0	61.3	63.2	62.9	63.2	63.2	62.9
Japan	9.1	10.3	10.6	11.6	11.7	11.5	11.2	11.3
Western Europe	22.2	19.5	18.6	16.3	15.9	15.4	15.0	14.8
ROW	7.1	9.1	9.5	9.0	9.5	9.9	10.6	11.1
Worldwide MOS PLD	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	61.3	61.6	61.6	63.7	63.4	63.4	63.3	63.0
Japan	9.2	11.0	11.1	11.4	11.6	11.5	11.2	11.3
Western Europe	22.6	19.0	18.4	16.1	15.7	15.3	15.0	14.8
ROW	6.9	8.3	8.8	8.8	9.3	9.8	10.4	11.0
Worldwide Bipolar PLD	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	62.5	58.9	58.9	56.6	53.7	53.8	51.4	50.7
Japan	8.9	7.7	7.4	13.4	14.4	12.7	11.2	10.8
Western Europe	21.1	21.4	20.0	19.0	18.7	17.8	16.8	16.0
ROW	7.5	12.1	13.7	11.0	13.3	15.8	20.5	22.5

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1995)

Table 20
Estimated Worldwide PLD Consumption by Logic Complexity (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Total PLD	957	1,173	1,309	1,704	2,061	2,521	3,109	3,845	24.0
Total SPLD	589	634	553	517	466	412	362	314	-10.7
Total High Density (CPLD + FPGA)	369	539	756	1,187	1,596	2,110	2,747	3,531	36.1
Total CMOS PLD	677	925	1,134	1,577	1,971	2,458	3,064	3,813	27.4
SPLD	309	386	378	390	376	348	317	282	-5.7
CPLD	128	210	306	519	715	967	1,292	1,714	41.1
FPGA	241	329	450	668	881	1,143	1,455	1,817	32.2
Total Bipolar PLD	280	248	175	127	90	63	45	32	-28.9
SPLD	280	248	175	127	90	63	45	32	-28.9

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1995)

Table 21
Estimated Worldwide PLD Consumption by Logic Complexity (Percentage Growth)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Total PLD	6.1	22.5	11.6	30.2	20.9	22.3	23.3	23.7	24.0
Total SPLD	-6.4	7.7	-12.8	-6.4	-10.0	-11.6	-12.1	-13.1	-10.7
Total High Density (CPLD + FPGA)	35.0	46.2	40.3	57.0	34.4	32.2	30.2	28.5	36.1
Total CMOS PLD	21.1	36.6	22.6	39.1	25.0	24.7	24.7	24.4	27.4
SPLD	7.9	25.1	-2.1	3.2	-3.7	-7.3	-9.0	-10.9	-5.7
CPLD	51.9	64.6	45.7	69.6	37.7	35.2	33.7	32.6	41.1
FPGA	27.5	36.5	36.8	48.5	31.8	29.8	27.3	24.9	32.2
Total Bipolar PLD	-18.4	-11.4	-29.4	-27.3	-29.1	-29.9	-29.6	-28.8	-28.9
SPLD	-18.4	-11.4	-29.4	-27.3	-29.1	-29.9	-29.6	-28.8	-28.9

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (October 1995)

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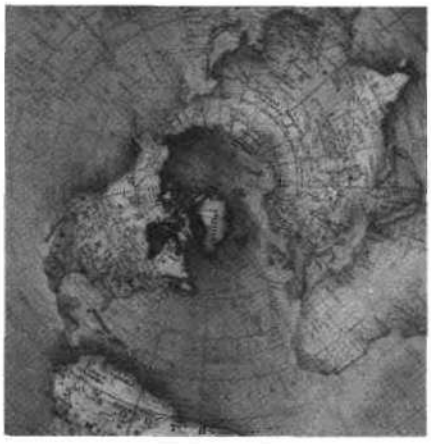

Dataquest

Worldwide ASIC Forecast

Market Statistics

Program: ASICs Worldwide
Product Code: ASIC-WW-MS-9502
Publication Date: May 22, 1995
Filing: Market Analysis

Worldwide ASIC Forecast

Market Statistics

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Worldwide ASIC Forecast

Introduction

This document contains detailed information on Dataquest's view of the application-specific integrated circuit (ASIC) market. Included in this document are the following:

- 1995-1999 ASIC consumption forecast
- 1995-1999 gate array consumption forecast
- 1995-1999 cell-based IC (CBIC) consumption forecast
- 1995-1999 programmable logic device (PLD) consumption forecast

More detailed data on this market may be requested through Dataquest's client inquiry service. Qualitative analysis of this data is provided in the Dataquest Market Trends and other documents located in the binder of the same name.

Segmentation

This section outlines the market segments that are specific to this document. Dataquest's objective is to provide data along lines of segmentation that are logical, appropriate to the industry in question, and immediately useful to clients.

Dataquest defines the ASIC market according to the segmentation scheme in Figure 1.

Figure 1 shows Dataquest's segmentation into the two main categories of standard logic and ASIC. The ASIC family tree breaks out ASICs as follows: PLDs, gate arrays, CBICs, and full-custom ICs. CBICs and full-custom ICs are personalized by altering the full set of masks, whereas PLDs and gate arrays are personalized by electrically programming the devices or by altering only the final layers of interconnect. ASICs are further classified according to process technology: MOS, bipolar, and BiCMOS.

Definitions

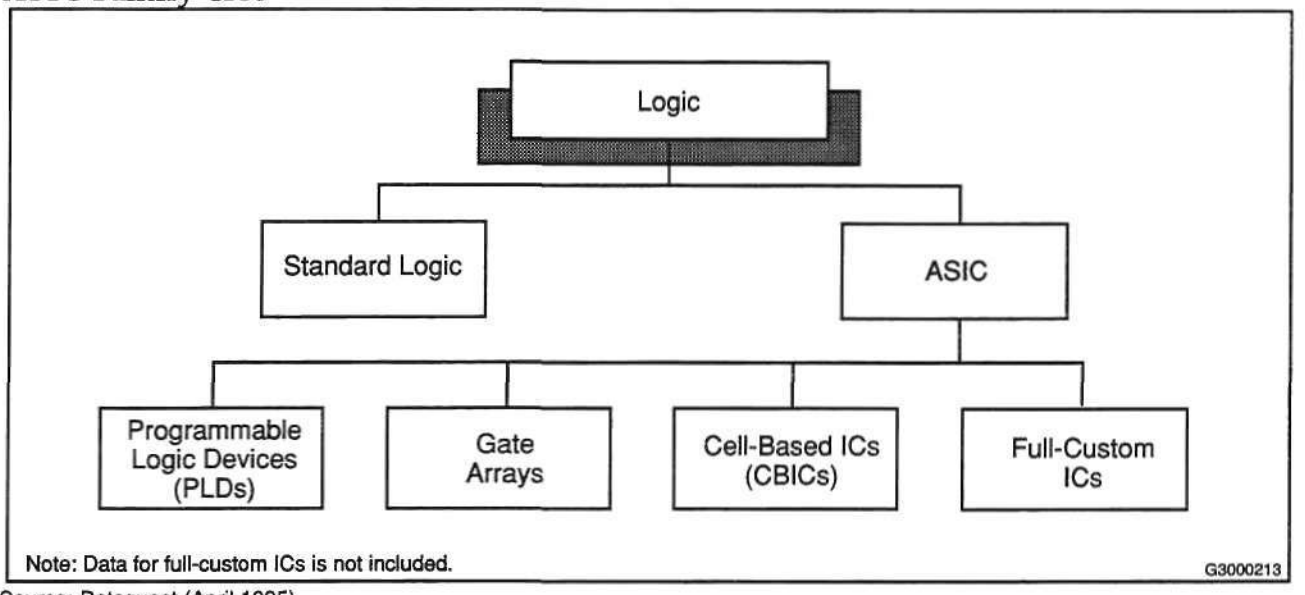
This section lists the definitions used by Dataquest to present the data in this document.

Product Definitions

Application-Specific Integrated Circuits (ASICs)

This term is used to describe all IC products customized for a single user. ASIC products are a combination of digital, mixed-signal, and analog products. Customized ICs purchased by more than one user become standard products and are no longer counted as ASICs.

Figure 1
ASIC Family Tree



Source: Dataquest (April 1995)

Programmable Logic Devices (PLDs)

PLDs are defined as ICs programmed after assembly. Memory devices such as PROMs and ROMs are not included in this market segment. PLDs are subdivided into three main categories:

- Simple programmable logic devices (SPLDs): SPLDs have fixed or preconnected architectures capable of providing up to two levels of logic without using additional input, output, or I/O cells or pins.
- Complex programmable logic devices (CPLDs): CPLDs are product-term or segmented PAL-based devices that may or may not implement multiple levels of logic without using additional input, output, or I/O cells or pins.
- Field-programmable gate arrays (FPGAs): FPGAs are based on segmented programmable interconnect and typically consist of an X-Y matrix of logic modules typically fed by a limited number of preconnected signals.

Gate Arrays

Gate arrays are ASICs that contain a configuration of uncommitted elements in a prefabricated base wafer. They are customized by interconnecting these elements with one or more routing layers. Included in this category are traditional gate arrays (channeled and sea-of-gates architecture) and embedded gate arrays (channeled or sea-of-gates architecture that also include megacells such as SRAM diffused into the gate array base wafer).

CBICs

CBICs are ASICs that are customized using a full set of masks and use automatic place-and-route tools. Included in this category are traditional standard cells (fixed-height/fixed-width cells) as well as megacells (variable-height/variable-width cells) and compiled cells.

Full-custom ICs

Full-custom ICs are defined as ASIC devices that are produced for a single user using a full set of masks. This process involves manual routing and placement of cells.

Revenue Classification

Because systems may be fabricated, assembled, and sold in several different locations, Dataquest's regional device consumption is defined according to the shipping destination.

Consumption estimates include the following five sources of revenue:

- Intracompany revenue (sales to internal divisions)
- Nonrecurring engineering (NRE) revenue
- ASIC software revenue
- PLD development kit revenue
- Device production revenue

Despite the care taken in gathering, analyzing, and categorizing the data in a meaningful way, careful attention must be paid to the definitions and assumptions used herein when interpreting the estimates presented in this document. Various companies, government agencies, and trade associations may use slightly different definitions of product categories and regional groupings, or they may include different companies in their summaries. These differences should be kept in mind when making comparisons between data and numbers provided by Dataquest and those provided by other suppliers.

Merchant versus Captive Consumption

Dataquest includes all revenue, both merchant and captive, for semiconductor suppliers selling to the merchant market. Dataquest's consumption estimates do not include captive-only manufacturing companies represented by companies such as Digital Equipment Corporation, Northern Telecom, or Unisys that do not sell semiconductor products in the merchant market.

Regional Definitions

North America: Includes Canada, Mexico, and the United States

Europe: Western Europe and eastern Europe

Japan: Japan

Asia/Pacific-Rest of World: All other countries

Forecast Methodology and Assumptions

Dataquest publishes five-year factory revenue forecasts for the ASIC market during the first and third quarter of each year. In doing so, Dataquest utilizes a variety of forecasting techniques (both qualitative and quantitative) that vary by technology area. An overview of Dataquest forecasting techniques can be found in the Dataquest Research Methodology guides.

ASIC Forecast Methodology

Dataquest's forecast methodology includes the following steps:

- Formally and informally survey the leading ASIC vendors (in gate arrays, CBICs, and PLDs) throughout the year for their expectations, as well as for their views of the application markets in which they participate
- Formally survey ASIC users for their expected buying patterns, in addition to their views on the growth of the application markets in which they participate
- Examine statistics provided by a number of industry and government organizations (such as the World Semiconductor Trade Statistics, the Japanese Ministry of International Trade and Industry, and the U.S. Department of Commerce) for up-to-date monthly trends
- Perform time-series analysis as well as apply judgmental industry knowledge to product and application trends

ASIC Forecast Assumptions

ASIC

The worldwide 1995 ASIC market is expected to experience the highest growth rate in recent history (20.7 percent, excluding full-custom ICs). Alhough yen appreciation against the dollar will increase the 1995 dollar growth rate of the ASIC market (we factored in 10 percent yen appreciation at the time of the forecast), we believe the market will post outstanding growth rates because of a fundamental change in the products being shipped. Leading ASIC suppliers are shifting their focus from low-value commodity gate arrays to higher margin, value-added cell-based ICs. Cell-based ICs had the highest growth rate of all ASIC products in 1994 (28 percent), and we believe this trend will hold true for 1995 in all regions. Furthermore, Dataquest predicts the size of the worldwide cell-based IC market to surpass that of the gate array market by 1998, and for it to become the largest ASIC market.

Gate Arrays

MOS Gate Arrays

CMOS continues to be the dominant gate array technology for the foreseeable future because of its low cost, low power consumption, and high integration.

The North American CMOS gate array market will closely track the computer market because more than 60 percent of all gate arrays are consumed in data processing applications.

The Japanese MOS gate array market continues to see severe price erosion. However, margins will improve as Japanese companies start to invest in unique cell libraries to gain intellectual property.

The low-end CMOS market (fewer than 20,000 gates) will continue to be adversely impacted by field-programmable gate arrays (FPGAs).

Embedded gate arrays (that is, megacells such as SRAMs that are diffused in the array base wafer) are included in the gate array category and are expected to fuel gate array growth by the mid- to late 1990s.

Although we believe that the price per gate will continue to drop, average selling prices (ASPs) still are expected to rise because of the increasing use of on-chip functions such as SRAM, ALU, multiplier, multiplier-accumulator, FIFO, DMA controller, cache controller, and 82XX microperipherals.

Bipolar Gate Arrays

Bipolar gate arrays are being replaced by CMOS, BiCMOS, and GaAs ASICs because of their high cost and high power consumption. The TTL gate array market is declining, primarily because there have been no new TTL arrays designed in the past three years, and production of these devices is accordingly winding down.

The ECL gate array market is declining at a rapid rate in all regions because most ECL arrays are consumed in large mainframe and supercomputers, which are declining markets.

BiCMOS Gate Arrays

BiCMOS gate array growth has been lowered substantially from our previous forecast because of the lack of high-volume production from vertically integrated companies such as Fujitsu, NEC, and AT&T. At this point, the costs of these BiCMOS devices do not outweigh the benefits from BiCMOS in comparison to CMOS. According to Dataquest's worldwide end-user survey of more than 500 systems designers, demand for BiCMOS ASICs in their next-generation systems design is dropping significantly from two years ago.

Cell-Based ICs

MOS CBICs

There will be an increased use of CBICs in North America in high-density applications (greater than 100,000 gates) and/or high-volume applications (greater than 50,000 units a year) such as dataprocessing, telecom, and consumer.

There will be an increasing use of CBICs in Japan (at the expense of gate arrays) in high-volume applications such as video games, printers, and disk drives, mainly because of the smaller die size of CBICs. CBICs are also penetrating high-complexity applications in Japan such as computers and HDTV.

Telecom applications are driving the CBIC growth in Europe.

Bipolar CBICs

Bipolar CBIC growth stems from two product types: ECL CBICs and analog CBICs. ECL CBICs are expected to experience negative growth, primarily because system designers do not want macros supplied by

ASIC vendors; they want to design their own macros on the transistor level to optimize their designs for their unique applications.

Analog CBICs, such as National's "Classic" line, are expected to experience flat to modest growth.

BiCMOS CBICs

BiCMOS CBICs are a good solution for mixed analog/digital applications. The analog portion can be implemented using bipolar technology and the digital portion with CMOS technology.

BiCMOS CBICs are expected to be used in many telecommunications applications.

PLDs

CMOS PLDs

CMOS PLD growth stems from three types of devices: simple PLDs (SPLDs), complex PLDs (CPLDs), and field-programmable gate arrays (FPGAs). The critical element for the success of all three device types is the time to market.

The SPLD market is expected to experience negative growth rates during the next few years. The current market is driven by the conversion from bipolar SPLDs and standard logic. However, the decline in growth will accelerate as these small devices are replaced with higher-density CPLDs and FPGAs, which can now match all but the fastest SPLDs for particular functions.

Dataquest believes that CPLDs will continue to grow faster than the semiconductor industry. The CPLD growth rate has outpaced the FPGA growth rate for the last five years and will continue to do so for the duration of this forecast. However, FPGA total dollars remain higher than CPLD dollars and are expected to remain higher through 1998. Although CPLDs hold a slight ease-of-use and speed advantage over FPGAs, FPGAs have traditionally offered higher gate counts (than CPLDs), which users are demanding for future system design. As CPLDs and FPGAs approach similar density and functionality, we expect the CPLD growth and FPGA growth to stabilize just beyond 1998.

The FPGA market is expected to show excellent growth over the next five years for the following reasons:

- The shift continues from TTL- and PAL-based designs toward FPGA usage.
- FPGAs will attack not only the low-end gate array market (fewer than 10,000 gates), but also the 10,000- to 40,000-gate array market in the 1995 to 1997 time frame as prices drop and gate array vendors migrate to higher-density devices.
- Additional market impetus will come from the introduction of new architectures in 1995 and 1996. New entrants into the market may also contribute to increased growth.

Dataquest believes that FPGAs will encounter increased price competition in the 1994 to 1996 time frame as lagging suppliers try to buy market share and entrenched competitors shore up their positions.

The factors influencing CMOS PLD growth are as follows (by region):

- Europe: Designs here tend to favor lower volume and lower gate counts, a category that PLDs fit well. As a result, PLD growth will continue to be strong.
- Japan: PLDs will penetrate internal development and play a significant role in prototyping, increasing growth.
- North America: The U.S. market is maturing, and concomitant decrease in growth rates will ensue.
- ROW: As design expertise increases, demand for CPLD and FPGA products will also increase.

Bipolar PLDs

The PC boom ended in 1993, and with it the surge in bipolar PLD sales. The ensuing negative growth will again help bipolar PLDs to resume the previous market dynamics; the bipolar PLD market will decline as users shift from bipolar PLDs to MOS PLDs. Furthermore, we believe that the bipolar PLD market will continue to decline until only a few high-speed ECL devices and specialty high-drive PLDs remain.

Exchange Rates

Dataquest used an average annual exchange rate in converting revenue to U.S. dollar amounts. Table 1 outlines these rates for 1992 through 1994. The 1995 rates are based on a weighted average.

Table 1
Exchange Rates

	1992	1993	1994	1995
Japan (Yen/U.S.$)	126.45	112.20	101.96	88.12
France (Franc/U.S.$)	5.27	5.67	5.91	4.94
Germany (Deutsche Mark/U.S.$)	1.56	1.66	1.74	1.41
United Kingdom (U.S.$/Sterling Pound)	1.77	1.50	1.49	1.61
European Community (U.S.$/ECU)	0.770	0.858	0.896	0.770

Source: Dataquest (May 1995)

Table 2
Estimated Worldwide ASIC Consumption by Technology (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Total ASIC	9,648	11,657	13,309	15,430	17,397	19,419	21,866	25,088	13.5
MOS ASIC	7,632	9,739	11,448	13,540	15,500	17,475	19,883	22,960	14.9
Bipolar ASIC	1,746	1,543	1,388	1,267	1,078	906	747	613	-15.1
BICMOS ASIC	270	375	473	623	819	1,038	1,236	1,515	26.2
Total Gate Array	3,861	4,658	5,338	6,214	6,929	7,668	8,604	9,820	13
MOS Gate Array	2,701	3,544	4,232	5,087	5,844	6,612	7,555	8,733	15.6
Bipolar Gate Array	969	873	818	768	642	524	412	317	-17.3
BICMOS Gate Array	191	241	288	359	443	532	637	770	21.7
Total PLD	957	1,173	1,309	1,515	1,795	2,150	2,614	3,202	19.6
MOS PLD	677	925	1,134	1,388	1,705	2,087	2,569	3,170	22.8
Bipolar PLD	280	248	175	127	90	63	45	32	-28.8
Total Cell-Based IC	2,486	3,283	4,193	5,359	6,466	7,545	8,757	10,327	19.8
MOS Cell-Based IC	2,313	3,067	3,931	5,022	6,022	6,978	8,105	9,535	19.4
Bipolar Cell-Based IC	94	82	77	73	68	61	53	47	-9.4
BICMOS Cell-Based IC	79	134	185	264	376	506	599	745	32.1
Total Full-Custom IC	2,344	2,543	2,469	2,342	2,207	2,056	1,891	1,739	-6.8
MOS Full-Custom IC	1,941	2,203	2,151	2,043	1,929	1,798	1,654	1,522	-6.7
Bipolar Full-Custom IC	403	340	318	299	278	258	237	217	-7.3

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest (May 1995)

Table 3
Estimated Worldwide ASIC Consumption by Technology (Percentage Growth)

	1992	1993	1994	1995	1996	1997	1998	1999
Total ASIC	1.4	20.8	14.2	15.9	12.7	11.6	12.6	14.7
MOS ASIC	3.7	27.6	17.5	18.3	14.5	12.7	13.8	15.5
Bipolar ASIC	-9.3	-11.6	-10.0	-8.7	-14.9	-16	-17.6	-17.9
BICMOS ASIC	16.4	38.9	26.1	31.7	31.5	26.7	19.1	22.6
Total Gate Array	-1.4	20.6	14.6	16.4	11.5	10.7	12.2	14.1
MOS Gate Array	1.1	31.2	19.4	20.2	14.9	13.1	14.3	15.6
Bipolar Gate Array	-9.8	-9.9	-6.3	-6.1	-16.4	-18.4	-21.4	-23.1
BICMOS Gate Array	13.0	26.2	19.5	24.7	23.4	20.1	19.7	20.9
Total PLD	6.1	22.6	11.6	15.7	18.5	19.8	21.6	22.5
MOS PLD	21.1	36.6	22.6	22.4	22.8	22.4	23.1	23.4
Bipolar PLD	-18.4	-11.4	-29.4	-27.4	-29.1	-30.0	-28.6	-28.9
Total Cell-Based IC	10.1	32.1	27.7	27.8	20.7	16.7	16.1	17.9
MOS Cell-Based IC	10.0	32.6	28.2	27.8	19.9	15.9	16.2	17.6
Bipolar Cell-Based IC	2.2	-12.8	-6.1	-5.2	-6.8	-10.3	-13.1	-11.3
BICMOS Cell-Based IC	25.4	69.6	38.1	42.7	42.4	34.6	18.4	24.4
Total Full-Custom IC	-4.1	8.5	-2.9	-5.1	-5.8	-6.9	-8.0	-8.0
MOS Full-Custom IC	-4.4	13.5	-2.4	-5.0	-5.6	-6.8	-8.0	-8.0
Bipolar Full-Custom IC	-3.0	-15.6	-6.5	-6.0	-6.9	-7.4	-8.2	-8.2

Source: Dataquest (May 1995)

Table 4
Estimated Worldwide ASIC Consumption by Technology (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Total ASIC	9,648	11,657	13,309	15,430	17,397	19,419	21,866	25,088	13.5
MOS ASIC	7,632	9,739	11,448	13,540	15,500	17,475	19,883	22,960	14.9
Bipolar ASIC	1,746	1,543	1,388	1,267	1,078	906	747	613	-15.1
BICMOS ASIC	270	375	473	623	819	1,038	1,236	1,515	26.2
Total ASIC (%)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	
MOS ASIC (%)	79.1	83.5	86.0	87.8	89.1	90.0	90.9	91.5	
Bipolar ASIC (%)	18.1	13.2	10.4	8.2	6.2	4.7	3.4	2.4	
BICMOS ASIC (%)	2.8	3.2	3.6	4.0	4.7	5.3	5.7	6.0	

Source: Dataquest (May 1995)

Table 5
Estimated Worldwide ASIC Consumption by Region (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total	7,304	9,114	10,840	13,087	15,171	17,362	19,974	23,348
MOS ASIC	5,691	7,536	9,297	11,497	13,551	15,677	18,229	21,438
Bipolar ASIC	1,343	1,203	1,070	968	801	647	510	395
BICMOS ASIC	270	375	473	623	820	1,038	1,235	1,515
North America	3,168	3,943	4,562	5,336	6,104	6,897	7,825	8,966
MOS ASIC	2,501	3,346	4,070	4,906	5,719	6,546	7,491	8,627
Bipolar ASIC	609	528	408	326	256	195	143	106
BICMOS ASIC	58	69	84	104	130	157	190	233
Japan	2,326	2,810	3,435	4,254	4,836	5,378	6,060	6,961
MOS ASIC	1,650	2,164	2,725	3,482	4,070	4,611	5,280	6,133
Bipolar ASIC	547	486	507	510	437	366	295	233
BICMOS ASIC	129	160	203	262	329	401	485	595
Western Europe	1,370	1,592	1,860	2,251	2,638	3,059	3,483	4,045
MOS ASIC	1,130	1,304	1,569	1,923	2,243	2,585	2,970	3,457
Bipolar ASIC	163	158	131	111	92	75	62	49
BICMOS ASIC	77	130	160	217	302	399	450	539
Asia/Pacific-Rest of World	440	769	983	1,246	1,594	2,028	2,607	3,376
MOS ASIC	410	722	933	1,186	1,519	1,935	2,488	3,220
Bipolar ASIC	24	31	24	20	15	12	9	7
BICMOS ASIC	6	16	26	40	59	81	109	149

Notes: Columns may not add to totals shown because of rounding. Full-custom ICs are excluded from this table.

Source: Dataquest (May 1995)

Table 6
Estimated Worldwide ASIC Consumption by Region (Percentage Growth)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Worldwide Total ASIC	3.3	24.8	18.9	20.7	15.9	14.4	15.0	16.9	16.6
North America	5.4	24.5	15.7	17.0	14.4	13.0	13.5	14.6	14.5
Japan	-6.1	20.8	22.2	23.9	13.7	11.2	12.7	14.9	15.2
Western Europe	8.5	16.2	16.8	21.0	17.2	16.0	13.9	16.1	16.8
Asia/Pacific-Rest of World	34.1	74.8	27.8	26.7	27.9	27.2	28.5	29.5	28.0
Worldwide MOS ASIC	6.7	32.4	23.4	23.7	17.9	15.7	16.3	17.6	18.2
North America	10.0	33.8	21.6	20.5	16.6	14.5	14.4	15.2	16.2
Japan	-3.6	31.2	25.9	27.8	16.9	13.3	14.5	16.2	17.6
Western Europe	8.3	15.4	20.3	22.6	16.6	15.2	14.9	16.4	17.1
Asia/Pacific-Rest of World	34.9	76.1	29.2	27.1	28.1	27.4	28.6	29.4	28.1
Worldwide Bipolar ASIC	-11.0	-10.4	-11.1	-9.6	-17.2	-19.1	-21.3	-22.4	-18.1
North America	-10.3	-13.3	-22.7	-20.0	-21.7	-23.9	-26.3	-25.8	-23.6
Japan	-15.6	-11.2	4.3	0.7	-14.3	-16.3	-19.3	-21.1	-14.4
Western Europe	1.2	-3.1	-17.1	-15.2	-16.7	-18.7	-17.6	-20.6	-17.8
Asia/Pacific-Rest of World	14.3	29.2	-22.6	-16.7	-25.0	-20.0	-25.0	-22.2	-21.8
Worldwide BICMOS ASIC	16.4	38.9	26.1	31.7	31.6	26.6	19.0	22.6	26.2
North America	11.5	19.0	21.7	23.8	24.8	20.8	21.3	22.6	22.7
Japan	9.3	24.0	26.9	29.1	25.5	22.0	21.0	22.6	24.0
Western Europe	30.5	68.8	23.1	35.6	39.2	32.1	12.9	19.6	27.5
Asia/Pacific-Rest of World	100.0	166.7	62.5	53.2	47.8	37.4	35.3	35.7	41.7

Note: Full-custom ICs are excluded from this table.

Source: Dataquest (May 1995)

Table 7
Estimated Worldwide ASIC Consumption by Region (Percentage of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total ASIC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	43.4	43.3	42.1	40.8	40.2	39.7	39.2	38.4
Japan	31.8	30.8	31.7	32.5	31.9	31	30.3	29.8
Western Europe	18.8	17.5	17.2	17.2	17.4	17.6	17.4	17.3
Asia/Pacific-Rest of World	6.0	8.4	9.1	9.5	10.5	11.7	13.0	14.5
Worldwide MOS ASIC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	43.9	44.4	43.8	42.7	42.2	41.8	41.1	40.2
Japan	29	28.7	29.3	30.3	30.0	29.4	29.0	28.6
Western Europe	19.9	17.3	16.9	16.7	16.6	16.5	16.3	16.1
Asia/Pacific-Rest of World	7.2	9.6	10.0	10.3	11.2	12.3	13.6	15.0
Worldwide Bipolar ASIC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	45.3	43.9	38.1	33.7	31.9	30.0	28.1	26.9
Japan	40.7	40.4	47.4	52.7	54.6	56.5	57.9	58.9
Western Europe	12.1	13.1	12.2	11.5	11.6	11.6	12.1	12.4
Asia/Pacific-Rest of World	1.8	2.6	2.2	2.0	1.9	1.8	1.8	1.8
Worldwide BICMOS ASIC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	21.5	18.4	17.8	16.7	15.8	15.1	15.4	15.4
Japan	47.8	42.7	42.9	42.1	40.1	38.6	39.3	39.3
Western Europe	28.5	34.7	33.8	34.8	36.9	38.5	36.5	35.5
Asia/Pacific-Rest of World	2.2	4.3	5.5	6.4	7.2	7.8	8.9	9.8

Note: Columns may not add to totals shown because of rounding. Full-custom ICs are excluded from this table.

Source: Dataquest (May 1995)

Table 8
Estimated Gate Array Consumption by Technology (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Total ASIC	9,648	11,657	13,309	15,430	17,397	19,419	21,866	25,088	13.5
Total Gate Array	3,861	4,658	5,338	6,214	6,929	7,668	8,604	9,820	13.0
MOS Gate Array	2,701	3,544	4,232	5,087	5,844	6,612	7,555	8,733	15.6
Bipolar Gate Array	969	873	818	768	642	524	412	317	-17.3
BICMOS Gate Array	191	241	288	359	443	532	637	770	21.7
Total Gate Array (%)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	
MOS Gate Array (%)	70.0	76.1	79.3	81.9	84.3	86.2	87.8	88.9	
Bipolar Gate Array (%)	25.1	18.7	15.3	12.4	9.3	6.8	4.8	3.2	
BICMOS Gate Array (%)	4.9	5.2	5.4	5.8	6.4	6.9	7.4	7.8	

Source: Dataquest (May 1995)

Table 9
Estimated Worldwide Gate Array Consumption by Region (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total Gate Array	3,861	4,658	5,338	6,214	6,929	7,668	8,604	9,820
MOS Gate Array	2,701	3,544	4,232	5,087	5,844	6,612	7,555	8,733
Bipolar Gate Array	969	873	818	768	642	524	412	317
BICMOS Gate Array	191	241	288	359	443	532	637	770
North America	1,423	1,728	1,923	2,187	2,430	2,672	2,973	3,362
MOS Gate Array	992	1,333	1,596	1,896	2,167	2,432	2,748	3,135
Bipolar Gate Array	379	337	259	210	164	123	86	59
BICMOS Gate Array	52	58	68	82	100	117	140	168
Japan	1,699	1,950	2,331	2,790	3,056	3,305	3,620	4,039
MOS Gate Array	1,081	1,361	1,677	2,079	2,362	2,625	2,947	3,351
Bipolar Gate Array	498	446	475	485	417	350	284	224
BICMOS Gate Array	120	143	179	226	277	330	390	464
Western Europe	529	635	640	671	716	773	843	923
MOS Gate Array	426	517	533	570	622	683	751	828
Bipolar Gate Array	89	89	84	74	62	51	43	34
BICMOS Gate Array	14	29	23	27	32	39	48	61
Asia/Pacific-Rest of World	210	345	444	566	727	918	1,167	1,496
MOS Gate Array	202	333	426	541	693	873	1,108	1,418
Bipolar Gate Array	3	1	0	0	0	0	0	0
BICMOS Gate Array	5	11	18	25	34	45	59	78

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (May 1995)

Table 10
Estimated Worldwide Gate Array Consumption by Region (Percentage Growth)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Worldwide Total Gate Array	-1.4	20.6	14.6	16.4	11.5	10.7	12.2	14.1	13.0
North America	1.3	21.4	11.3	13.8	11.1	9.9	11.3	13.1	11.8
Japan	-7.8	14.8	19.5	19.7	9.6	8.1	9.6	11.6	11.6
Western Europe	6.2	20.0	0.8	4.9	6.6	8.0	9.0	9.5	7.6
Asia/Pacific-Rest of World	25.0	64.3	28.7	27.5	28.4	26.3	27.1	28.2	27.5
Worldwide MOS Gate Array	1.1	31.2	19.4	20.2	14.9	13.1	14.3	15.6	15.6
North America	4.8	34.4	19.7	18.8	14.3	12.2	13.0	14.1	14.5
Japan	-7.1	25.9	23.2	24.0	13.6	11.1	12.3	13.7	14.8
Western Europe	6.5	21.4	3.1	7.0	9.0	9.9	10.0	10.2	9.2
Asia/Pacific-Rest of World	25.5	64.9	27.9	27.0	28.0	26.0	27.0	28.0	27.2
Worldwide Bipolar Gate Array	-9.8	-9.9	-6.3	-6.1	-16.4	-18.5	-21.3	-23.1	-17.3
North America	-7.6	-11.1	-23.1	-19.0	-22.0	-25.0	-30.0	-31.0	-25.5
Japan	-12.5	-10.4	6.5	2.0	-14.0	-16.0	-19.0	-21.0	-14.0
Western Europe	-2.2	0	-5.6	-11.9	-16.2	-17.7	-15.7	-20.9	-16.5
Asia/Pacific-Rest of World	-25	-66.7	-100.0	NM	NM	NM	NM	NM	NM
Worldwide BICMOS Gate Array	13.0	26.2	19.5	24.7	23.4	20.0	19.7	20.9	21.7
North America	8.3	11.5	17.2	20.0	22.0	18.0	19.0	20.0	19.8
Japan	8.1	19.2	25.2	26.0	23.0	19.0	18.0	19.0	21.0
Western Europe	100.0	107.1	-20.7	17.0	19.0	22.0	24.0	25.0	21.4
Asia/Pacific-Rest of World	66.7	120.0	63.6	40.0	36.0	32.0	30.0	32.0	34.0

NM = Not meaningful

Source: Dataquest (May 1995)

Table 11
Estimated Worldwide Gate Array Consumption by Region (Percentage of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total Gate Array	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	36.9	37.1	36.0	35.2	35.1	34.8	34.6	34.2
Japan	44.0	41.9	43.7	44.9	44.1	43.1	42.1	41.1
Western Europe	13.7	13.6	12.0	10.8	10.3	10.1	9.8	9.4
Asia/Pacific-Rest of World	5.4	7.4	8.3	9.1	10.5	12.0	13.6	15.2
Worldwide MOS Gate Array	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	36.7	37.6	37.7	37.3	37.1	36.8	36.4	35.9
Japan	40.0	38.4	39.6	40.9	40.4	39.7	39.0	38.4
Western Europe	15.8	14.6	12.6	11.2	10.6	10.3	9.9	9.5
Asia/Pacific-Rest of World	7.5	9.4	10.1	10.6	11.9	13.2	14.7	16.2
Worldwide Bipolar Gate Array	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	39.1	38.6	31.7	27.3	25.5	23.4	20.8	18.7
Japan	51.4	51.1	58.1	63.1	64.9	66.8	68.7	70.6
Western Europe	9.2	10.2	10.3	9.6	9.7	9.7	10.4	10.7
Asia/Pacific-Rest of World	0.3	0.1	0	0	0	0	0	0
Worldwide BICMOS Gate Array	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	27.2	24.1	23.6	22.7	22.5	22.1	22.0	21.8
Japan	62.8	59.3	62.2	62.8	62.6	62.1	61.2	60.2
Western Europe	7.3	12.0	8.0	7.5	7.2	7.3	7.6	7.9
Asia/Pacific-Rest of World	2.6	4.6	6.3	7.0	7.7	8.5	9.2	10.1

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (May 1995)

Table 12
Estimated CBIC Consumption by Technology (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Total ASIC	9,648	11,657	13,309	15,430	17,397	19,419	21,866	25,088	13.5
Total Cell-Based IC	2,486	3,283	4,193	5,359	6,446	7,545	8,757	10,327	19.8
MOS Cell-Based IC	2,313	3,067	3,931	5,022	6,002	6,978	8,105	9,535	19.4
Bipolar Cell-Based IC	94	82	77	73	68	61	53	47	-9.4
BICMOS Cell-Based IC	79	134	185	264	376	506	599	745	32.1
Total Cell-Based IC (%)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	
MOS Cell-Based IC (%)	93.0	93.4	93.8	93.7	93.1	92.5	92.6	92.3	
Bipolar Cell-Based IC (%)	3.8	2.5	1.8	1.4	1.1	0.8	0.6	0.5	
BICMOS Cell-Based IC (%)	3.2	4.1	4.4	4.9	5.8	6.7	6.8	7.2	

Source: Dataquest (May 1995)

Table 13
Estimated Worldwide CBIC Consumption by Region (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total Cell-Based IC	2,486	3,283	4,193	5,359	6,446	7,545	8,757	10,327
MOS Cell-Based IC	2,313	3,067	3,931	5,022	6,002	6,978	8,105	9,535
Bipolar Cell-Based IC	94	82	77	73	68	61	53	47
BICMOS Cell-Based IC	79	134	185	264	376	506	599	745
North America	1,155	1,499	1,837	2,240	2,614	2,976	3,360	3,815
MOS Cell-Based IC	1,094	1,443	1,775	2,174	2,544	2,900	3,277	3,720
Bipolar Cell-Based IC	55	45	46	43	40	36	33	30
BICMOS Cell-Based IC	6	11	16	22	30	39	50	65
Japan	540	739	965	1,289	1,560	1,802	2,099	2,491
MOS Cell-Based IC	507	701	922	1,235	1,495	1,719	1,994	2,353
Bipolar Cell-Based IC	24	21	19	17	14	11	9	7
BICMOS Cell-Based IC	9	17	24	36	51	71	96	131
Western Europe	629	728	976	1,302	1,596	1,898	2,172	2,552
MOS Cell-Based IC	551	611	827	1,099	1,312	1,525	1,759	2,064
Bipolar Cell-Based IC	15	16	12	13	14	13	11	10
BICMOS Cell-Based IC	63	101	137	190	270	360	402	478
Asia/Pacific-Rest of World	162	317	415	527	676	869	1,126	1,469
MOS Cell-Based IC	161	312	407	513	651	834	1,075	1,398
Bipolar Cell-Based IC	0	0	0	0	0	0	0	0
BICMOS Cell-Based IC	1	5	8	15	25	36	51	71

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (May 1995)

Table 14
Estimated Worldwide CBIC Consumption by Region (Percentage Growth)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Worldwide Total Cell-Based IC	10.1	32.1	27.7	27.8	20.3	17.0	16.1	17.9	19.8
North America	10.2	29.8	22.5	21.9	16.7	13.8	12.9	13.5	15.7
Japan	5.1	36.9	30.6	33.5	21.1	15.4	16.5	18.7	20.9
Western Europe	8.1	15.7	34.1	33.4	22.6	18.9	14.5	17.5	21.2
Asia/Pacific-Rest of World	42.1	95.7	30.9	27.1	28.1	28.6	29.5	30.4	28.8
Worldwide MOS Cell-Based IC	10.0	32.6	28.2	27.7	19.5	16.3	16.2	17.6	19.4
North America	10.5	31.9	23.0	22.5	17.0	14.0	13.0	13.5	15.9
Japan	5.8	38.3	31.5	34.0	21.0	15.0	16.0	18.0	20.6
Western Europe	6.0	10.9	35.4	32.9	19.4	16.2	15.3	17.3	20.1
Asia/Pacific-Rest of World	41.2	93.8	30.4	26.0	27.0	28.0	29.0	30.0	28.0
Worldwide Bipolar Cell-Based IC	2.2	-12.8	-6.1	-5.6	-6.2	-10.9	-13.2	-11.7	-9.6
North America	1.9	-18.2	2.2	-5.7	-7.0	-9.7	-10.0	-9.0	-8.3
Japan	-14.3	-12.5	-9.5	-12.0	-15.0	-20.0	-25.0	-23.0	-19.1
Western Europe	50.0	6.7	-25.0	5.0	8.0	-5.0	-12.0	-11.0	-3.3
Asia/Pacific-Rest of World	NM	NM	NM	NM	NM	NM	NM	NM	NM
Worldwide BICMOS Cell-Based IC	25.4	69.6	38.1	42.4	42.8	34.5	18.3	24.5	32.1
North America	50.0	83.3	45.5	40.0	35.0	30.0	28.0	30.0	32.5
Japan	28.6	88.9	41.2	52.0	41.0	38.0	35.0	37.0	40.5
Western Europe	21.2	60.3	35.6	38.7	42.1	33.3	11.7	18.9	28.4
Asia/Pacific-Rest of World	NM	400.0	60.0	83.0	68.0	45.0	42.0	40.0	54.7

NM = Not meaningful

Source: Dataquest (May 1995)

Table 15
Estimated Worldwide CBIC Consumption by Region (Percentage of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total Cell-Based IC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	46.5	45.7	43.8	41.8	40.6	39.4	38.4	36.9
Japan	21.7	22.5	23.0	24.1	24.2	23.9	24.0	24.1
Western Europe	25.3	22.2	23.3	24.3	24.8	25.2	24.8	24.7
Asia/Pacific-Rest of World	6.5	9.7	9.9	9.8	10.5	11.5	12.9	14.2
Worldwide MOS Cell-Based IC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	47.3	47.0	45.2	43.3	42.4	41.6	40.4	39.0
Japan	21.9	22.9	23.5	24.6	24.9	24.6	24.6	24.7
Western Europe	23.8	19.9	21.0	21.9	21.9	21.9	21.7	21.6
Asia/Pacific-Rest of World	7.0	10.2	10.4	10.2	10.9	11.9	13.3	14.7
Worldwide Bipolar Cell-Based IC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	58.5	54.9	59.7	59.7	59.2	60.0	62.2	64.1
Japan	25.5	25.6	24.7	23.0	20.9	18.7	16.2	14.1
Western Europe	16.0	19.5	15.6	17.3	20.0	21.3	21.6	21.8
Asia/Pacific-Rest of World	0	0	0	0	0	0	0	0
Worldwide BICMOS Cell-Based IC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	7.6	8.2	8.6	8.5	8.0	7.8	8.4	8.8
Japan	11.4	12.7	13	13.8	13.7	14.0	16.0	17.6
Western Europe	79.7	75.4	74.1	72.1	71.8	71.2	67.1	64.1
Asia/Pacific-Rest of World	1.3	3.7	4.3	5.6	6.5	7.0	8.5	9.5

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest (May 1995)

Table 16
Estimated PLD Consumption by Technology (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Total ASIC	9,648	11,657	13,309	15,430	17,397	19,419	21,866	25,088	13.5
Total PLD	957	1,173	1,309	1,515	1,795	2,150	2,614	3,202	19.6
MOS PLD	677	925	1,134	1,388	1,705	2,087	2,569	3,170	22.8
Bipolar PLD	280	248	175	127	90	63	45	32	-28.9
Total PLD (%)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	
MOS PLD (%)	70.7	78.9	86.6	91.6	95.0	97.1	98.3	99.0	
Bipolar PLD (%)	29.3	21.1	13.4	8.4	5.0	2.9	1.7	1.0	

Source: Dataquest (May 1995)

Table 17
Estimated Worldwide PLD Consumption by Region (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total PLD	957	1,173	1,309	1,515	1,795	2,150	2,614	3,202
MOS PLD	677	925	1,134	1,388	1,705	2,087	2,569	3,170
Bipolar PLD	280	248	175	127	90	63	45	32
North America	590	716	802	909	1,059	1,249	1,491	1,789
MOS PLD	415	570	699	835	1,007	1,214	1,466	1,772
Bipolar PLD	175	146	103	73	52	35	25	17
Japan	87	121	139	176	219	272	341	431
MOS PLD	62	102	126	167	213	267	338	429
Bipolar PLD	25	19	13	9	6	4	3	2
Western Europe	212	229	244	278	326	388	468	570
MOS PLD	153	176	209	254	310	377	460	565
Bipolar PLD	59	53	35	24	17	11	8	5
Asia/Pacific-Rest of World	68	107	124	152	191	241	314	411
MOS PLD	47	77	100	132	176	229	304	404
Bipolar PLD	21	30	24	20	15	12	9	7

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest (May 1995)

Table 18
Estimated Worldwide PLD Consumption by Region (Percentage Growth)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Worldwide Total PLD	6.1	22.6	11.6	15.7	18.5	19.7	21.6	22.5	19.6
North America	6.9	21.4	12.0	13.3	16.6	18.0	19.4	20.0	17.4
Japan	-28.1	39.1	14.9	26.7	24.4	24.1	25.6	26.4	25.4
Western Europe	15.8	8.0	6.6	14.1	17.3	18.8	20.5	22.0	18.5
Asia/Pacific-Rest of World	47.8	57.4	15.9	22.6	25.6	26.1	30.2	31.0	27.1
Worldwide MOS PLD	21.1	36.6	22.6	22.4	22.8	22.4	23.1	23.4	22.8
North America	23.1	37.3	22.6	19.5	20.6	20.5	20.8	20.9	20.4
Japan	-11.4	64.5	23.5	32.5	27.4	25.7	26.5	26.9	27.8
Western Europe	24.4	15.0	18.8	21.5	21.9	21.7	22.1	22.9	22.0
Asia/Pacific-Rest of World	62.1	63.8	29.9	32.3	32.7	30.4	32.9	32.6	32.2
Worldwide Bipolar PLD	-18.4	-11.4	-29.4	-27.7	-28.7	-30.3	-29.1	-29.0	-28.9
North America	-18.6	-16.6	-29.5	-28.9	-29.6	-31.4	-30.1	-30.1	-30.0
Japan	-51.0	-24.0	-31.6	-29.8	-30.1	-30.1	-28.9	-28.9	-29.6
Western Europe	-1.7	-10.2	-34.0	-30.1	-31.0	-33.4	-33.0	-33.0	-32.1
Asia/Pacific-Rest of World	23.5	42.9	-20.0	-17.7	-21.8	-23.1	-22.7	-22.7	-21.6

Source: Dataquest (May 1995)

Table 19
Estimated Worldwide PLD Consumption by Region (Percentage of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999
Worldwide Total PLD	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	61.7	61.0	61.3	60.0	59.0	58.1	57.1	55.9
Japan	9.1	10.3	10.6	11.6	12.2	12.6	13.1	13.5
Western Europe	22.2	19.5	18.6	18.4	18.2	18.0	17.9	17.8
Asia/Pacific-Rest of World	7.1	9.1	9.5	10.0	10.6	11.2	12.0	12.8
Worldwide MOS PLD	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	61.3	61.6	61.6	60.2	59.1	58.2	57.1	55.9
Japan	9.2	11.0	11.1	12.0	12.5	12.8	13.2	13.5
Western Europe	22.6	19.0	18.4	18.3	18.2	18.1	17.9	17.8
Asia/Pacific-Rest of World	6.9	8.3	8.8	9.5	10.3	11.0	11.8	12.7
Worldwide Bipolar PLD	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	62.5	58.9	58.9	57.9	57.1	56.2	55.4	54.6
Japan	8.9	7.7	7.4	7.2	7.1	7.1	7.1	7.1
Western Europe	21.1	21.4	20.0	19.3	18.7	17.8	16.9	15.9
Asia/Pacific-Rest of World	7.5	12.1	13.7	15.6	17.1	18.9	20.6	22.4

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (May 1995)

Table 20
Estimated Worldwide PLD Consumption by Logic Complexity (Millions of Dollars)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Total PLD	957	1,173	1,309	1,515	1,795	2,150	2,614	3,202	19.6
Total SPLD	589	634	553	486	419	358	303	252	-14.5
Total High Density (CPLD + FPGA)	369	539	756	1,029	1,376	1,792	2,310	2,949	31.3
Total CMOS PLD	677	925	1,134	1,388	1,705	2,087	2,569	3,170	22.8
SPLD	309	386	378	359	329	295	259	221	-10.2
CPLD	128	210	306	436	598	802	1,062	1,398	35.5
FPGA	241	329	450	593	778	991	1,248	1,551	28.1
Total Bipolar PLD	280	248	175	127	90	63	45	32	-28.9
SPLD	280	248	175	127	90	63	45	32	-28.9

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest (May 1995)

Table 21
Estimated Worldwide PLD Consumption by Logic Complexity (Percentage Growth)

	1992	1993	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
Total PLD	6.1	22.5	11.6	15.7	18.5	19.8	21.6	22.5	19.6
Total SPLD	-6.4	7.7	-12.8	-12.1	-13.7	-14.6	-15.3	-16.8	-14.5
Total High Density (CPLD + FPGA)	35.0	46.2	40.3	36.1	33.7	30.3	28.9	27.7	31.3
Total CMOS PLD	21.1	36.6	22.6	22.4	22.9	22.4	23.1	23.4	22.8
SPLD	7.9	25.1	-2.1	-5.1	-8.3	-10.4	-12.2	-14.7	-10.2
CPLD	51.9	64.6	45.7	42.4	37.2	34.1	32.5	31.6	35.5
FPGA	27.5	36.5	36.8	31.8	31.2	27.3	26.0	24.3	28.1
Total Bipolar PLD	-18.4	-11.4	-29.4	-27.3	-29.1	-29.9	-29.6	-28.8	-28.9
SPLD	-18.4	-11.4	-29.4	-27.3	-29.1	-29.9	-29.6	-28.8	-28.9

Source: Dataquest (May 1995)

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Market Analysis

ASICs Worldwide

Market Analysis

Cell-Based ICs Soar in 1994 ASIC Market Share

Abstract: *Cell-based IC revenue growth outpaced that of MOS PLDs and gate arrays, according to Dataquest's 1994 market share survey. In this article, Dataquest examines the 1994 ASIC market share rankings by company and product and explores the key areas where suppliers can invest to maximize profits.*
By Bryan Lewis

Traditional ASIC Suppliers Move to Higher Ground

Leading ASIC suppliers are shifting their focus from low-value commodity gate arrays to higher-margin, value-added cell-based ICs (CBICs). According to Dataquest's 1994 market share estimates, the top five ASIC suppliers experienced a combined 50 percent increase in CBIC sales over 1993, compared to a 15 percent increase in MOS gate array sales. LSI Logic, the largest merchant ASIC supplier and second-largest MOS gate array supplier, posted an outstanding 176 percent increase in CBIC sales, compared to a meager 4 percent increase in gate array sales. The entire worldwide MOS CBIC market had the highest growth rate of all the ASIC products, posting a 29 percent increase, followed by MOS PLDs with a 23 percent increase and MOS gate arrays with a 19 percent increase. Traditional ASIC suppliers are moving to higher-density devices (more than 100,000 gates) using large functional blocks where margins are higher, while FPGA and CPLD suppliers are moving in on the lower-density market to fill the void.

During 1994, NEC extended its lead over Fujitsu in total ASIC sales (see Figure 1) by increasing its CBIC sales 87 percent. LSI Logic strengthened its position in total ASIC sales by jumping from the No. 12 position in 1993 total CBIC sales to No. 6 in 1994 sales. Xilinx was one of the big winners in 1994 and set the record for the first exclusively MOS PLD company to make the top 10 in total ASIC sales. Xilinx's success in making the top 10 supplier

Dataquest

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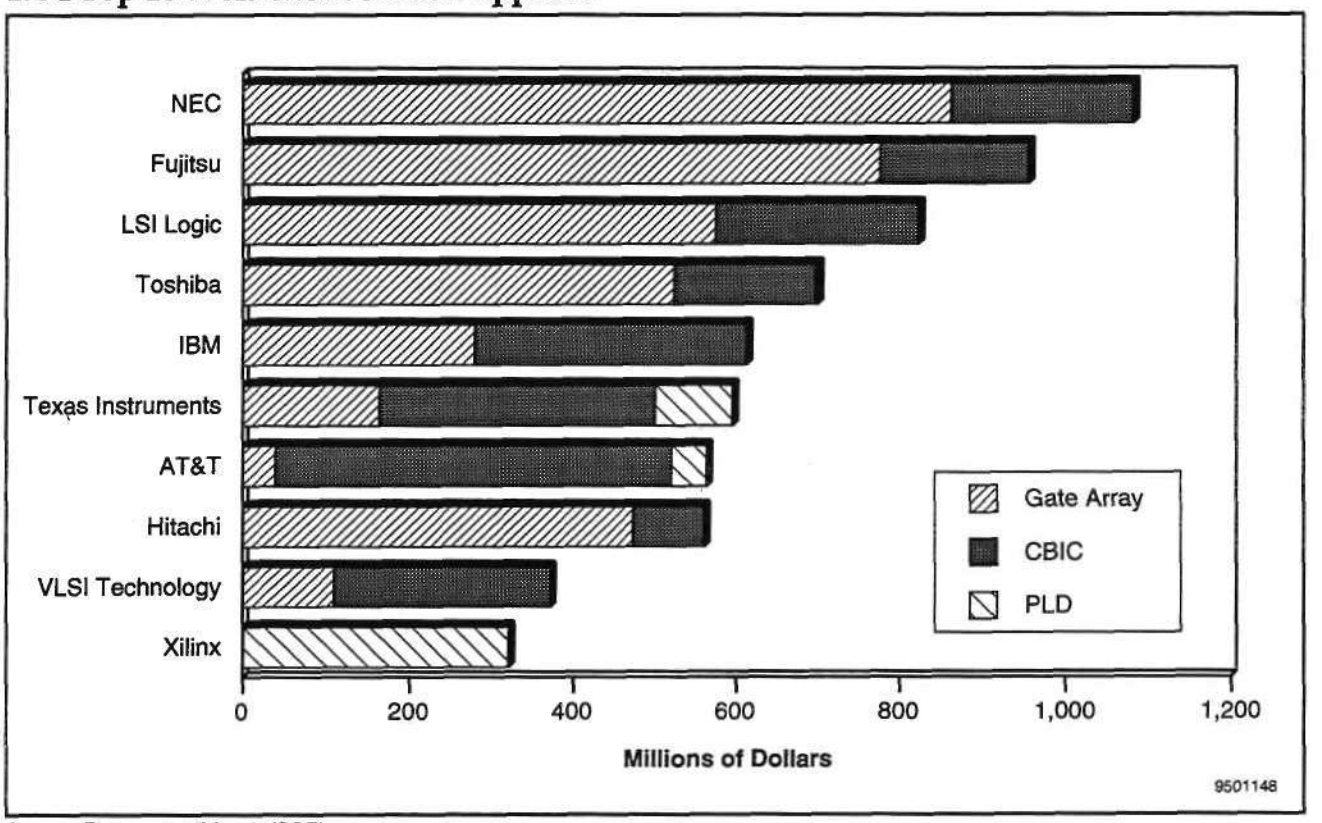
Figure 1
1994 Top 10 Worldwide ASIC Suppliers



Source: Dataquest (March 1995)

list is proof that MOS PLDs are filling the gap as traditional ASIC suppliers are abandoning the lower-density market.

Two important points should be kept in mind when examining the following market share rankings. First, yen appreciation against the dollar helped most Japanese companies post better-than-average growth rates (the yen appreciated about 8 percent against the dollar). Second, Dataquest estimates include sales to internal division (intracompany sales). Although NEC is the largest total ASIC supplier, LSI Logic is the largest merchant market ASIC supplier.

1994 ASIC Market Share

Table 1 shows the 1994 top 20 ASIC suppliers.

The following are footnotes to the ASIC market estimates:

- Total ASIC rankings include gate arrays plus CBICs plus PLDs.
- Rankings are based on dollar shipments, which include the following five sources of revenue:
  - Intracompany revenue (sales to internal divisions)
  - Nonrecurring engineering (NRE) revenue
  - ASIC software revenue

Table 1
1994 Worldwide Market Share Ranking: Total MOS/BiCMOS and Bipolar ASIC (Millions of Dollars)

1994 Rank	1993 Rank		1993 Revenue	1994 Revenue	Percentage Change (%)	1994 Market Share (%)
1	1	NEC	851	1,082	27	10.0
2	2	Fujitsu	832	956	15	8.8
3	3	LSI Logic	642	823	28	7.6
4	5	Toshiba	542	700	29	6.5
5	6	IBM	540	613	14	5.7
6	4	Texas Instruments	556	596	7	5.5
7	7	AT&T	499	564	13	5.2
8	8	Hitachi	428	561	31	5.2
9	9	VLSI Technology	344	372	8	3.4
10	12	Xilinx	231	321	39	3.0
11	11	Motorola	269	316	17	2.9
12	10	Advanced Micro Devices	288	281	-2	2.6
13	14	NCR	202	273	35	2.5
14	13	Hewlett-Packard	230	255	11	2.4
15	17	SGS-Thomson	168	212	26	2.0
16	18	Matsushita	154	212	38	2.0
17	19	Altera	140	199	42	1.8
18	16	GEC Plessey	170	173	2	1.6
19	25	Mitsubishi	73	170	133	1.6
20	20	Mietec	139	165	19	1.5

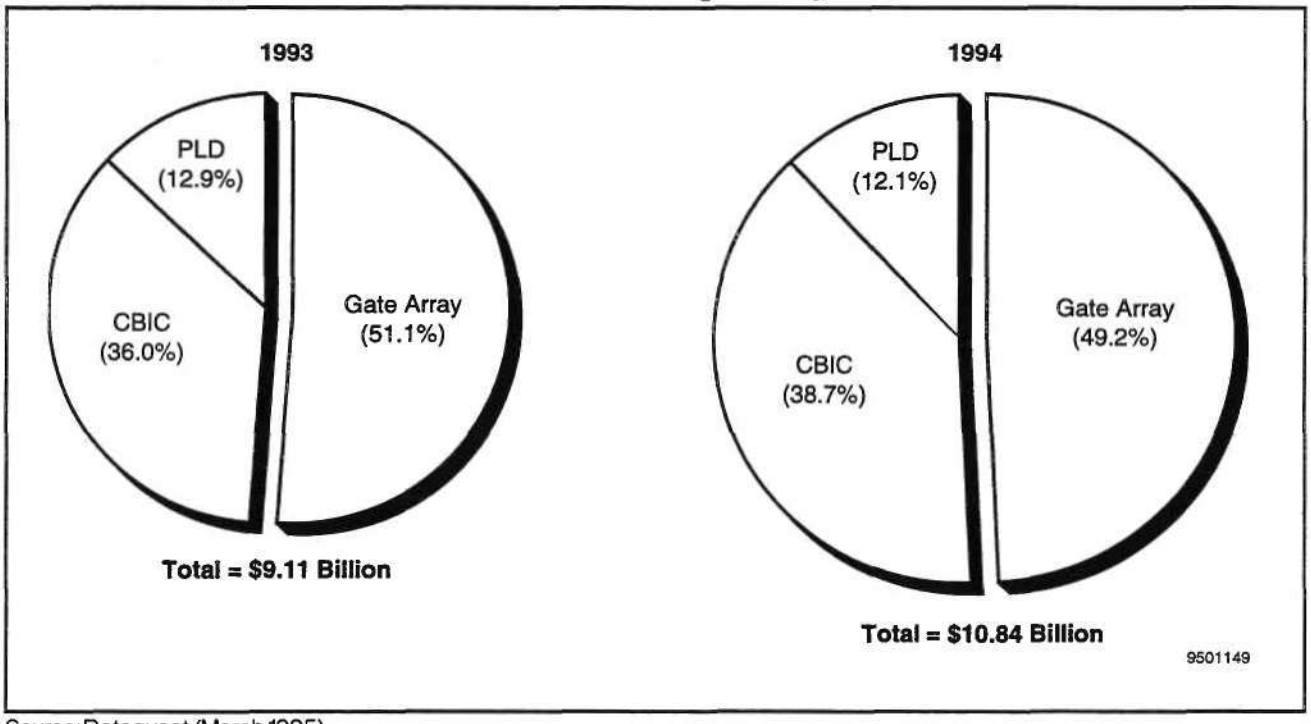
Source: Dataquest (March 1995)

  - PLD development kit revenue
  - Device production revenue
- Full-custom IC revenue is excluded from ASIC market share.
- ASIC product revenue is based on the combined revenue from digital, mixed analog/digital, and analog product.
- The U.S. dollar depreciated 8.4 percent against the yen during 1993. Dataquest's exchange rates are: U.S.$1 = ¥111.20 (1993), U.S.$1 = ¥101.81 (1994).

Product Overview

Figure 2 presents the composition of the ASIC market by product. Although gate arrays continue to dominate the market, CBICs are gaining market share. Total PLDs lost market share because bipolar PLDs had a dismal year, declining 29.4 percent (see Table 2). Bipolar PLDs are being replaced by MOS PLDs, which had a solid 22.6 percent growth rate, exceeding the growth rate of the total ASIC market.

Figure 2
Estimated 1993/1994 Worldwide ASIC Consumption, by Product



Source: Dataquest (March 1995)

Table 2
Estimated 1993/1994 Worldwide ASIC Consumption, by Product (Millions of Dollars)

	1993	1994	Percentage Change
MOS/BiCMOS Gate Array	3,785	4,520	19.4
Bipolar Gate Array	873	818	-6.3
MOS/BiCMOS Cell-Based IC	3,201	4,116	28.6
Bipolar Cell-Based IC	82	77	-6.1
MOS/BiCMOS PLD	925	1,134	22.6
Bipolar PLD	248	175	-29.4
Total Market	9,114	10,840	18.9

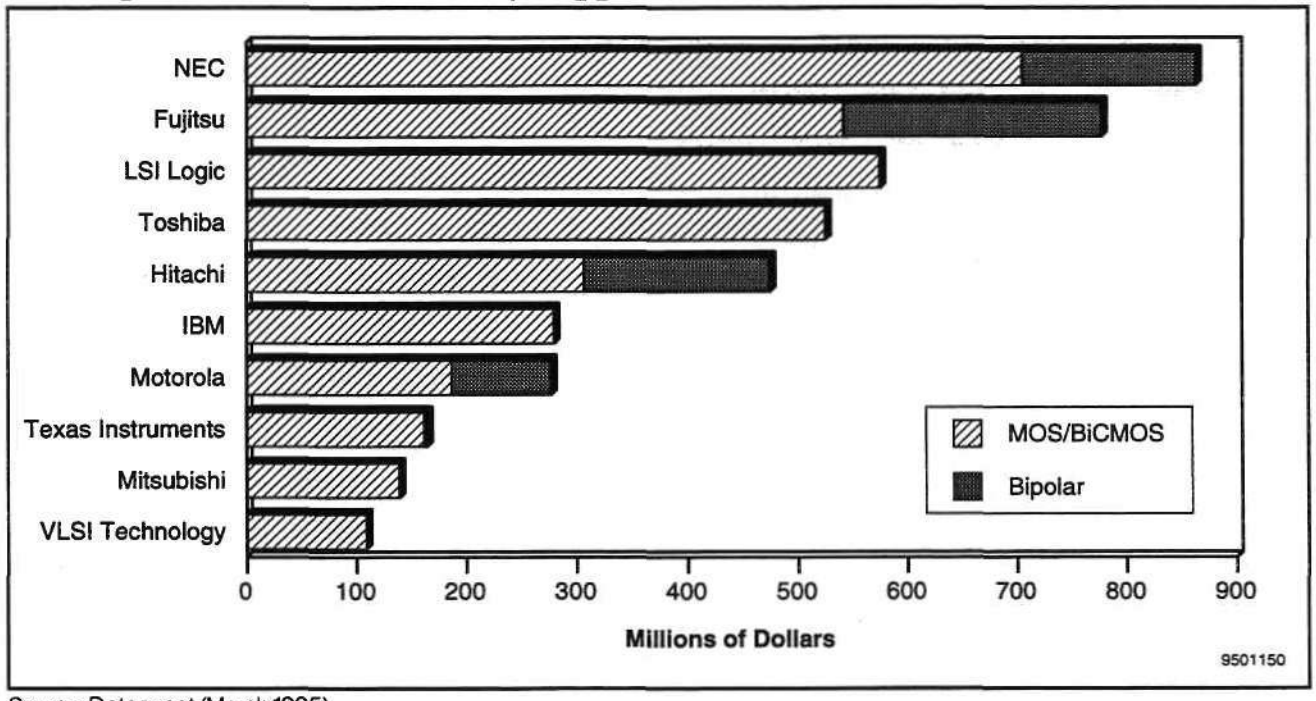
Source: Dataquest (March 1995)

Gate Arrays

The year 1994 was good for the MOS/BiCMOS gate array market, which had 19.4 percent growth, and an above-average year for bipolar gate arrays, with a 6.3 percent decline. MOS/BiCMOS gate array growth was fueled by strong market performance in personal computers/workstations and telecommunications. The bipolar gate array market was expected to decline faster than the 6 percent reported because of declining mainframe sales. Companies such as Fujitsu had a temporary increase in mainframe computer sales, which reduced the percentage decline in bipolar gate arrays.

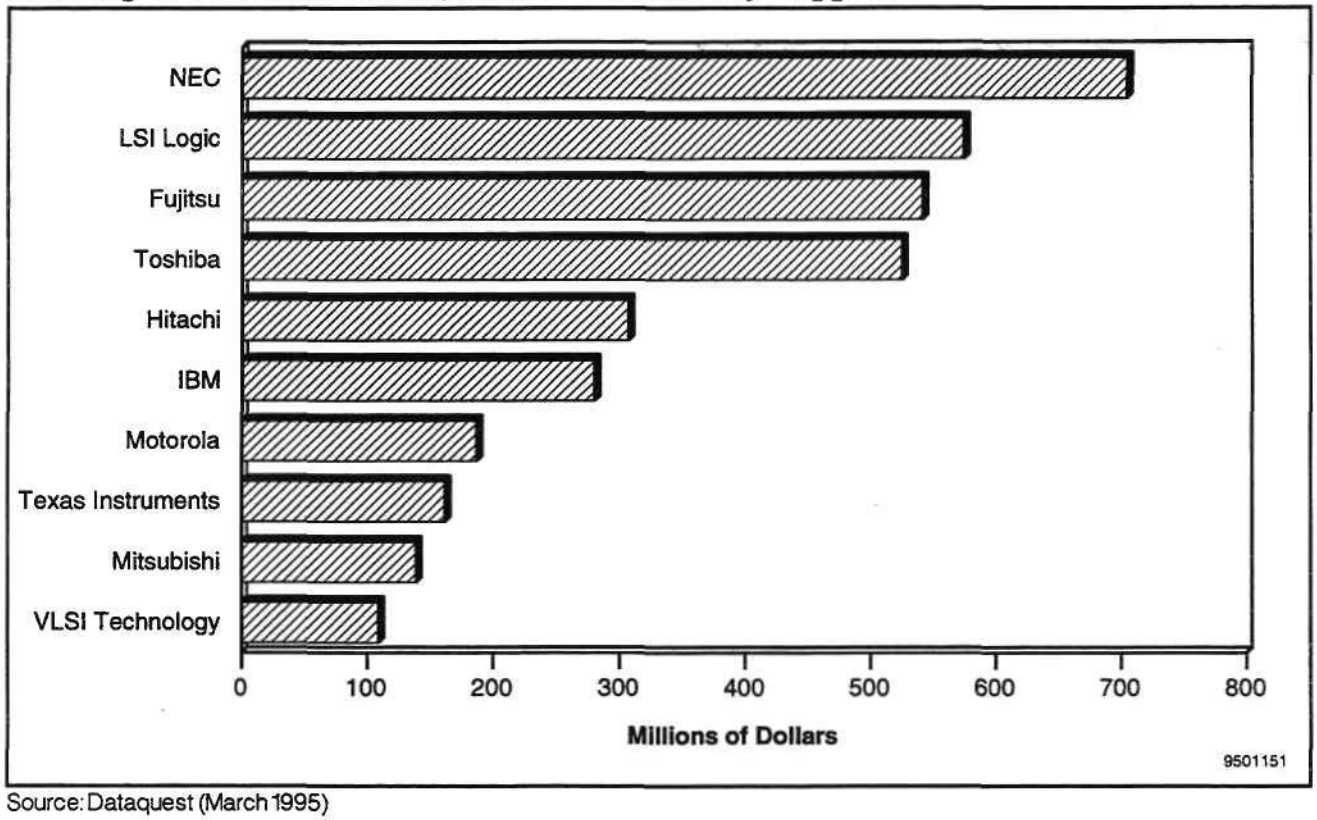
Figure 3 shows the 1994 worldwide gate array suppliers' revenue by technology of the top 10 companies. Figure 4 shows the top 10 1994 MOS/BiCMOS gate array suppliers, while Figure 5 ranks the same suppliers by

Figure 3
1994 Top 10 Worldwide Gate Array Suppliers



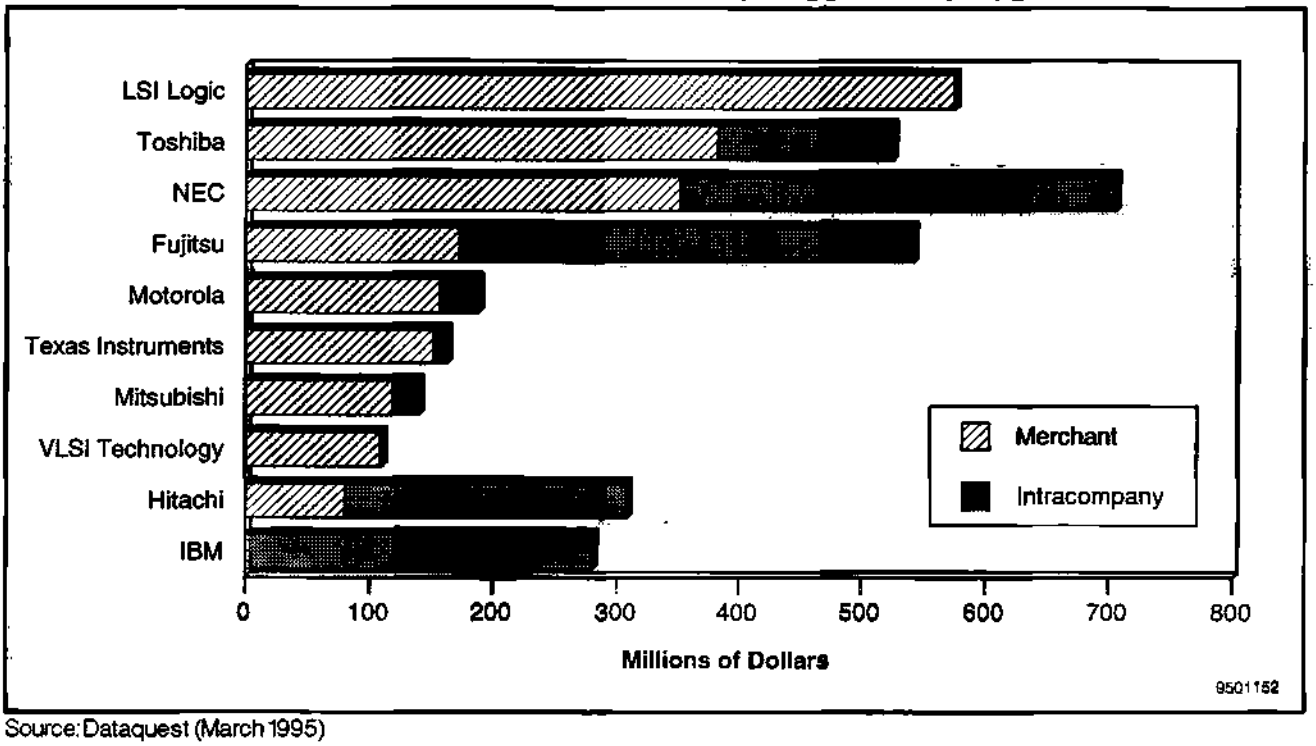
Source: Dataquest (March 1995)

Figure 4
1994 Top 10 Worldwide MOS/BiCMOS Gate Array Suppliers



Source: Dataquest (March 1995)

Figure 5
1994 Top 10 Worldwide MOS/BiCMOS Gate Array Suppliers, by Type of Sale



Source: Dataquest (March 1995)

size of estimated merchant sales. Table 3 lists the hotly contested top 20 1994 worldwide MOS gate array suppliers and their respective revenue, growth rates, and market shares. Figure 6 takes a snapshot of leading MOS/BiCMOS gate array suppliers in North America.

North America-based companies grew 9 percent in 1994 worldwide MOS/BiCMOS gate array sales, compared with 28 percent growth (including 8.4 percent yen appreciation) for Japan-based companies, 4 percent growth for Europe-based companies, and 27 percent growth for Asia/Pacific companies.

Noteworthy points regarding the 1994 gate array rankings include the following:

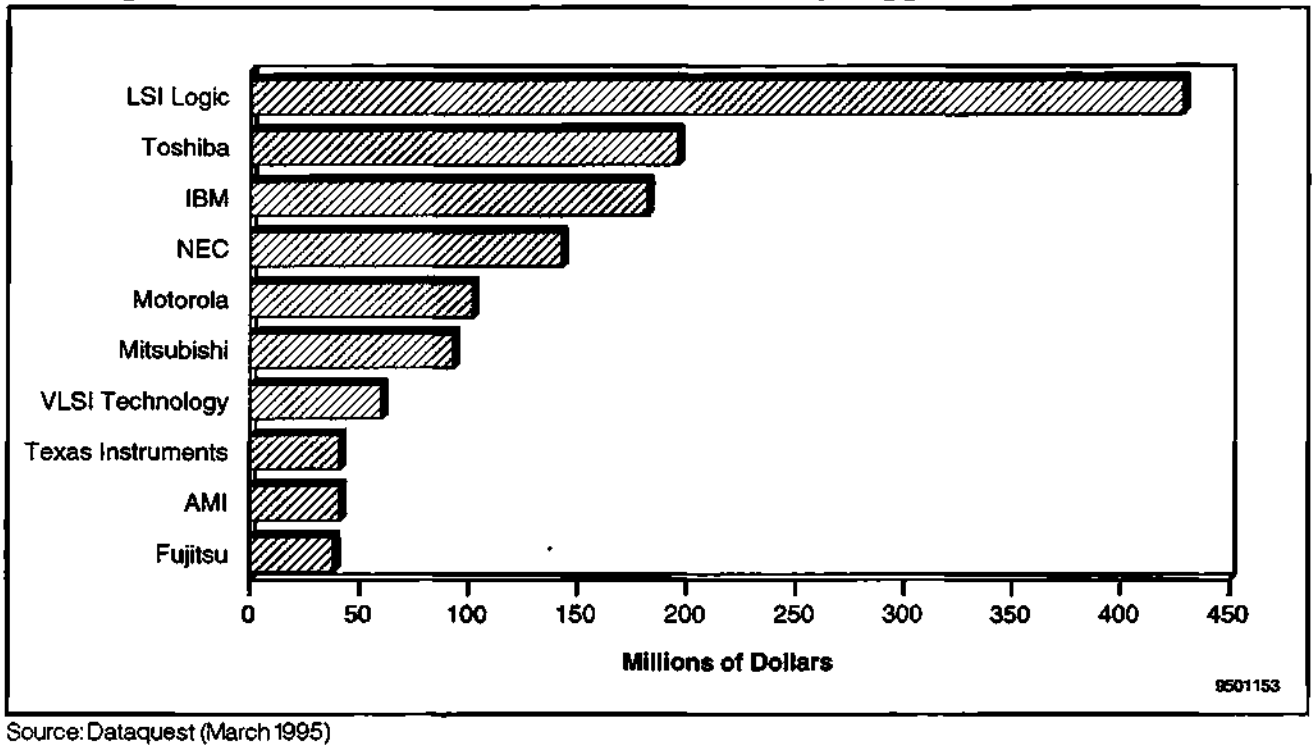
- NEC passed LSI Logic to become the No. 1 MOS/BiCMOS gate array supplier. However, a significant portion of NEC's sales are to internal divisions. LSI Logic remains the largest merchant gate array supplier, as shown in Figure 5.
- VLSI Technology had a weak year in MOS/BiCMOS gate arrays because the company focused on the CBIC market, where it had a solid year.
- Mitsubishi had an outstanding year, leaping from the No. 16 position in 1993 to No. 9 in 1994 MOS/BiCMOS gate arrays. Mitsubishi's 140 percent growth was driven by a few high-volume designs in the PC/workstation market.

Table 3
1994 Worldwide Market Share Ranking: MOS/BiCMOS Gate Array
(Millions of Dollars)

1994 Rank	1993 Rank		1993 Revenue	1994 Revenue	Percentage Change (%)	1994 Market Share (%)
1	2	NEC	550	705	28	15.6
2	1	LSI Logic	552	575	4	12.7
3	3	Fujitsu	466	542	16	12.0
4	4	Toshiba	427	525	23	11.6
5	6	Hitachi	235	307	31	6.8
6	5	IBM	243	280	15	6.2
7	7	Motorola	147	187	27	4.1
8	9	Texas Instruments	99	162	64	3.6
9	16	Mitsubishi	58	139	140	3.1
10	8	VLSI Technology	145	109	-25	2.4
11	13	Matsushita	73	95	30	2.1
12	11	Seiko Epson	80	91	14	2.0
13	10	GEC Plessey	83	88	6	1.9
14	12	SGS-Thomson	73	80	10	1.8
15	15	OKI	61	78	28	1.7
16	17	Samsung	57	68	19	1.5
17	18	Sharp	48	62	29	1.4
18	23	AMI	21	43	105	1.0
19	19	National Semiconductor	42	40	-5	0.9
20	20	Sony	25	36	44	0.8

Source: Dataquest (March 1995)

Figure 6
1994 Top 10 North American MOS/BiCMOS Gate Array Suppliers



Source: Dataquest (March 1995)

Cell-Based ICs

The CBIC market was the place to be for ASIC suppliers in 1994. MOS/BiCMOS CBICs had a record year with 28.6 percent growth. One key reason for this record growth was the increased use of CBICs in Japan, primarily by large vertically integrated Japanese companies.

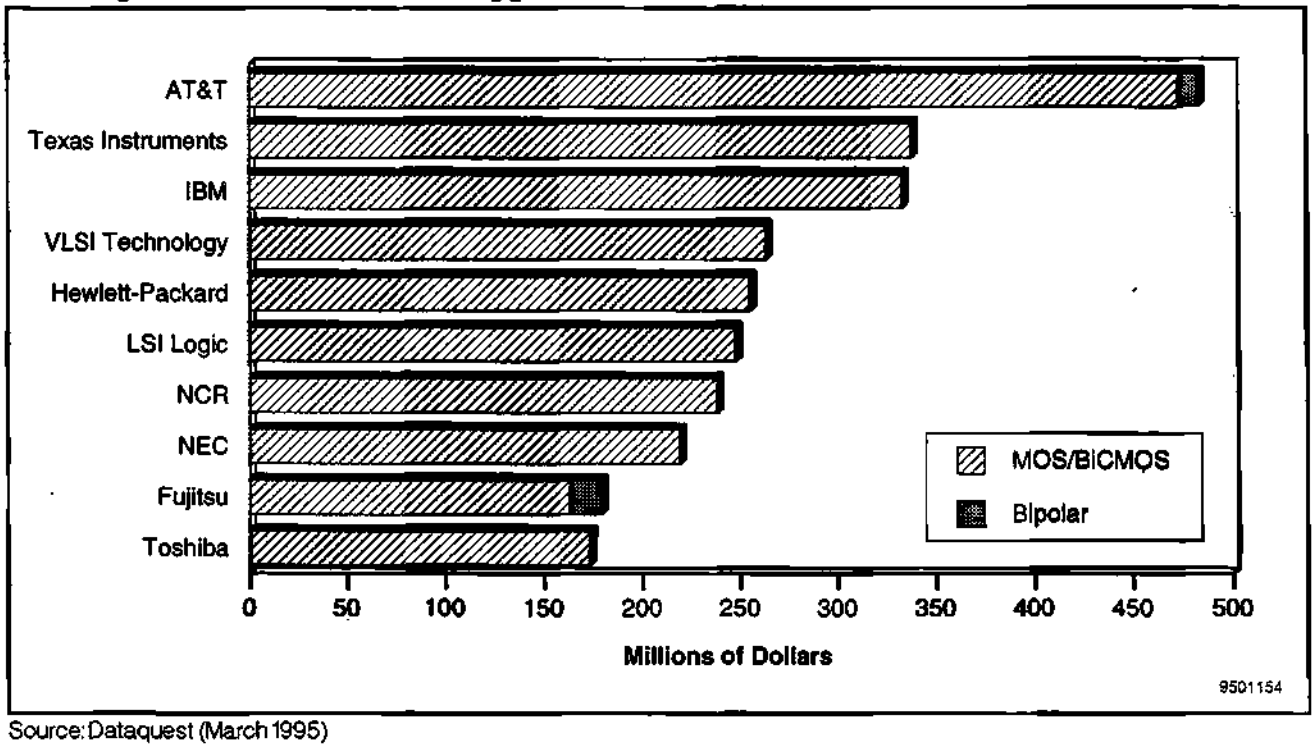
Although many North American companies had a good year in CBICs, total North America-based companies grew 23 percent in 1994 worldwide MOS/BiCMOS CBIC sales, compared with 54 percent growth for Japan-based companies, and 23 percent growth for Europe-based companies. Japan-based companies continue to target this market for future growth.

Figure 7 shows the top 10 1994 worldwide CBIC suppliers' revenue by technology. Table 4 shows the top 20 1994 worldwide MOS CBIC suppliers by their respective revenue, growth rates, and market shares. Figure 8 illustrates the top 10 worldwide MOS/BiCMOS CBIC suppliers, while Figure 9 shows the same suppliers ranked by estimated merchant sales. Figure 10 examines the top 10 1994 North American MOS/BiCMOS CBIC suppliers.

Noteworthy points regarding the 1994 CBIC rankings include the following:

- LSI Logic had a stellar year in CBICs, jumping from No. 11 in 1993 MOS/BiCMOS CBIC sales to No. 6 in 1994. LSI Logic's Core-ware products are primarily CBICs, and many previously captured computer and telecom designs moved into high-volume production in 1994.

Figure 7
1994 Top 10 Worldwide CBIC Suppliers



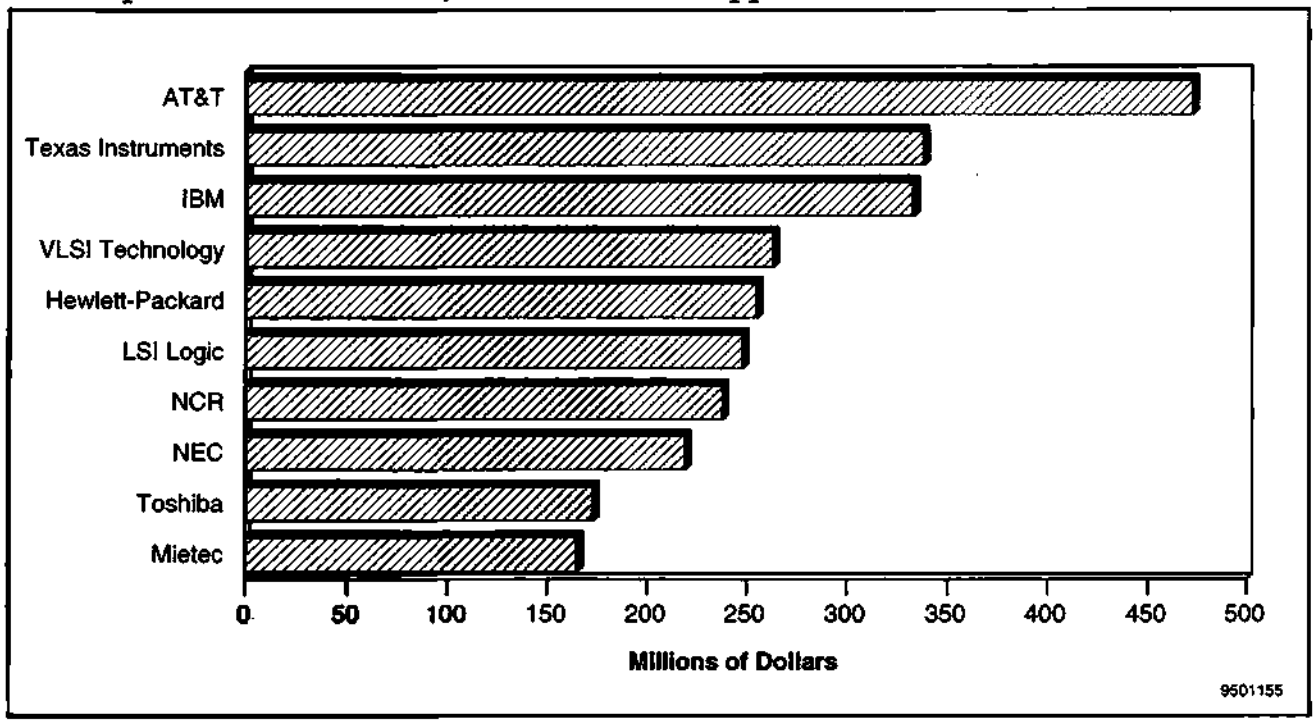
Source: Dataquest (March 1995)

Table 4
1994 Worldwide Market Share Ranking: MOS/BiCMOS Cell-Based IC (Millions of Dollars)

1994 Rank	1993 Rank		1993 Revenue	1994 Revenue	Percentage Change (%)	1994 Market Share (%)
1	1	AT&T	419	473	13	11.5
2	2	Texas Instruments	344	338	-2	8.2
3	3	IBM	297	333	12	8.1
4	5	VLSI Technology	199	263	32	6.4
5	4	Hewlett-Packard	230	255	11	6.2
6	11	LSI Logic	90	248	176	6.0
7	7	NCR	137	238	74	5.8
8	9	NEC	117	219	87	5.3
9	10	Toshiba	114	173	52	4.2
10	6	Mietec	139	165	19	4.0
11	8	Fujitsu	134	163	22	4.0
12	12	Matsushita	81	117	44	2.8
13	13	SGS-Thomson	80	113	41	2.7
14	14	Austria Mikro Systeme	67	86	28	2.1
15	18	Hitachi	39	86	121	2.1
16	15	GEC Plessey	63	67	6	1.6
17	21	OKI	35	62	77	1.5
18	17	National Semiconductor	58	58	0	1.4
19	16	Harris	62	47	-24	1.1
20	19	AMI	39	45	15	1.1

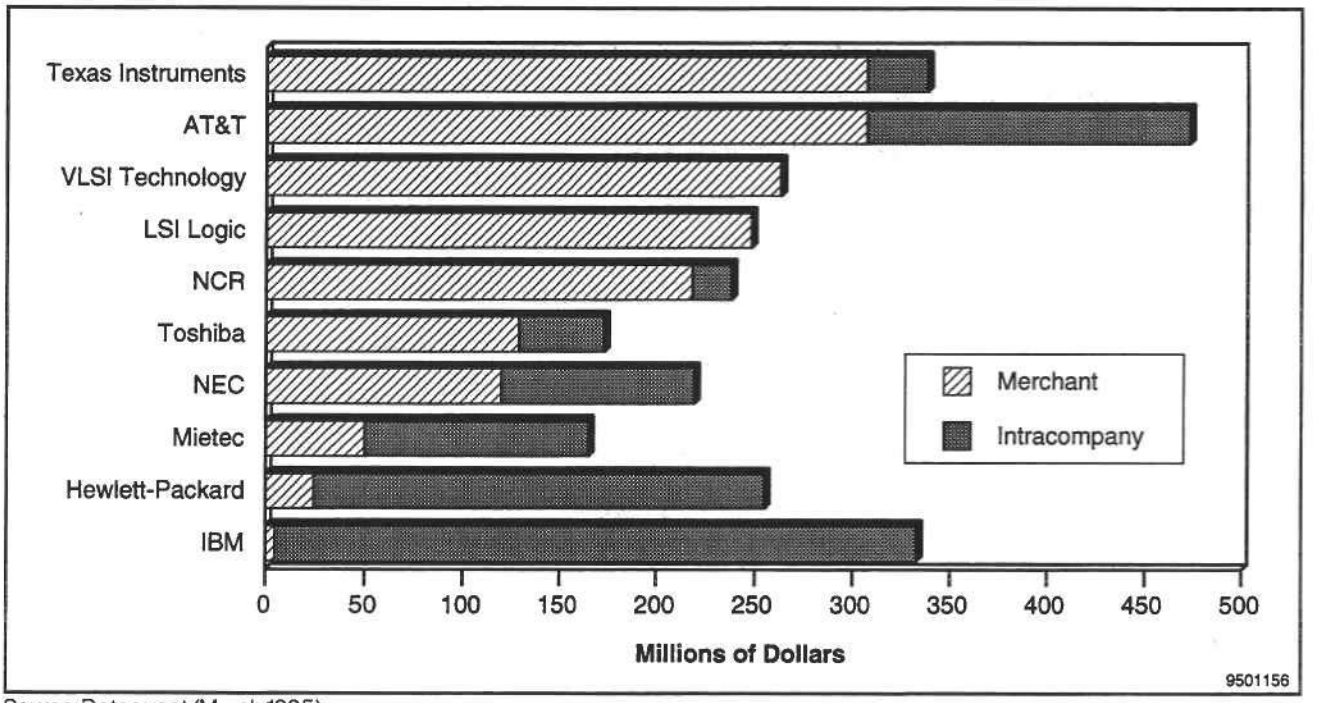
Source: Dataquest (March 1995)

Figure 8
1994 Top 10 Worldwide MOS/BiCMOS CBIC Suppliers



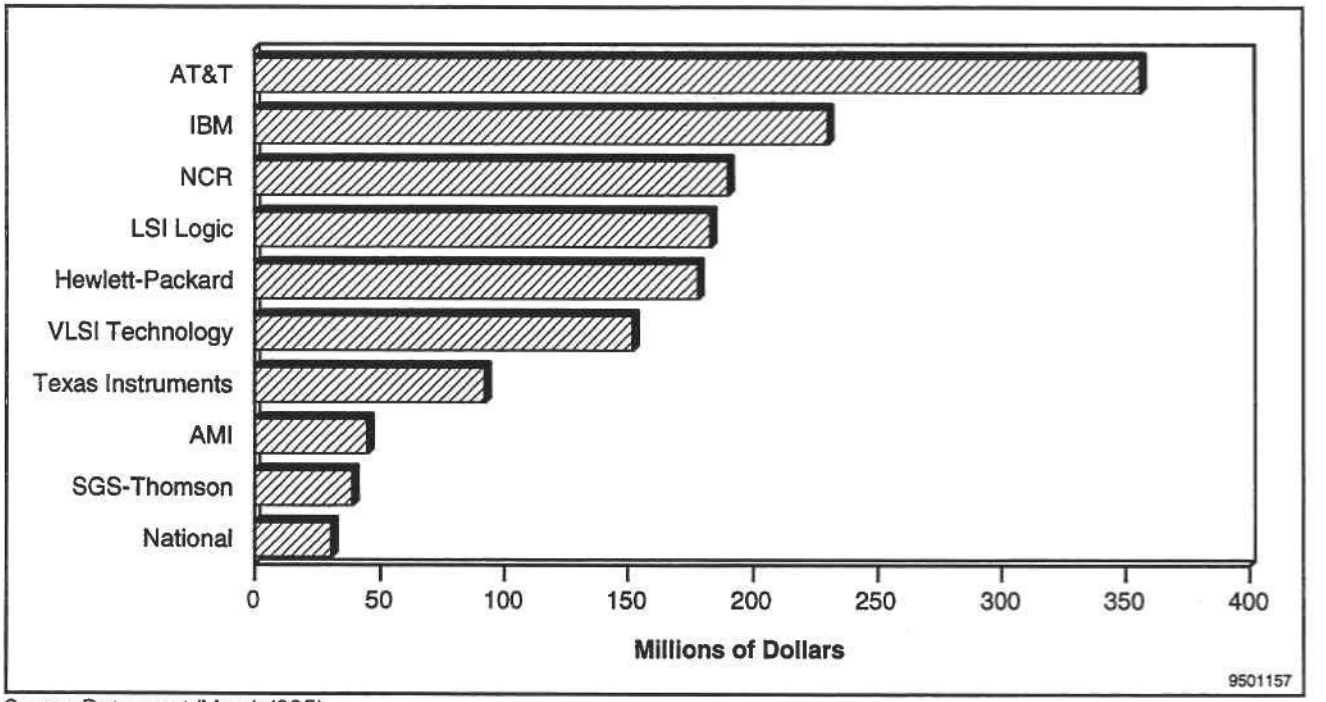
Source: Dataquest (March 1995)

Figure 9
1994 Top 10 Worldwide MOS/BiCMOS CBIC Suppliers, by Type of Sale



Source: Dataquest (March 1995)

Figure 10
1994 Top 10 North American MOS/BiCMOS CBIC Suppliers



Source: Dataquest (March 1995)

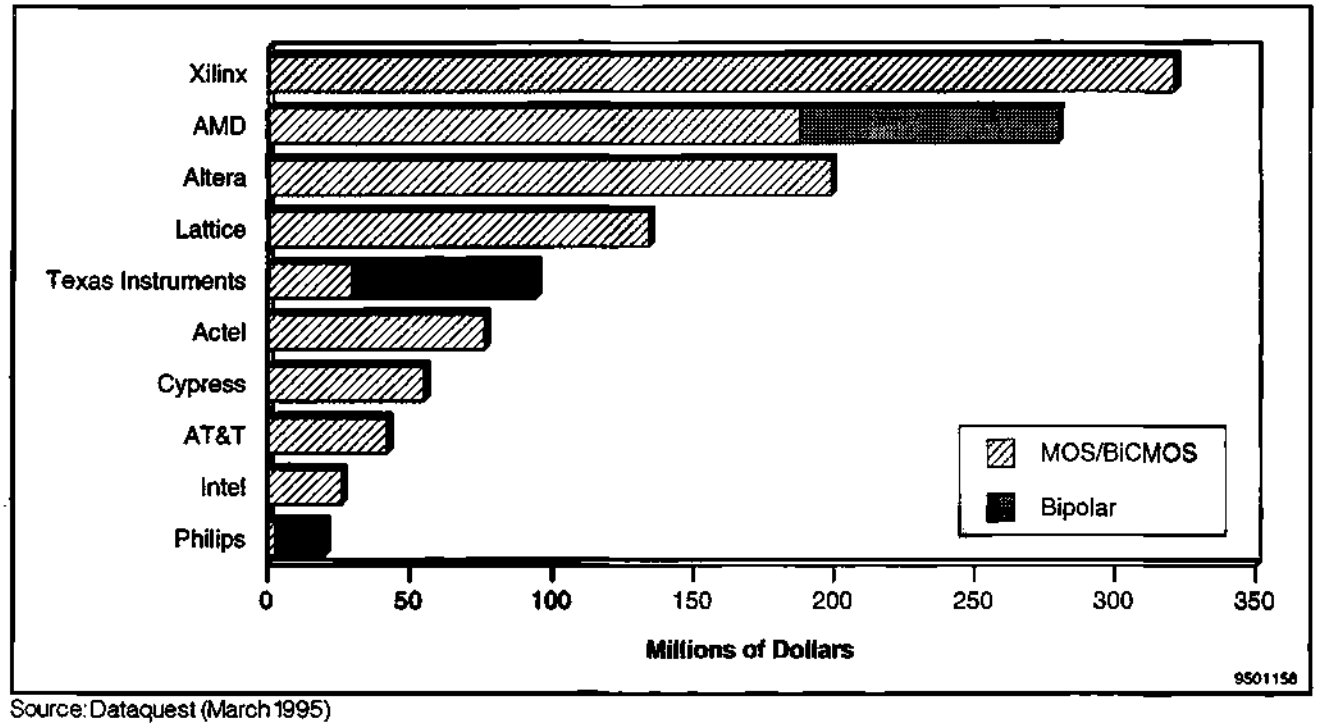
- Texas Instruments maintained its No. 2 position in CBICs. However, the company had a submarket performance in CBICs in part because it is changing its focus to gate array products. Furthermore, TI has a large portion of its CBIC sales in Japan in older designs that are starting to be phased out.
- AT&T had a good year in the merchant market and is tied with TI in 1994 merchant CBIC sales, as shown in Figure 9.
- Companies on the move in the CBIC market with high 1994 growth rates include: VLSI Technology, NCR (now called Symbios), NEC, and Toshiba.

PLDs

MOS/BiCMOS PLD growth continued at a solid pace in 1994 (22.6 percent), while bipolar PLDs had the worst year in history (down 29.4 percent). Of the MOS/BiCMOS products, CPLDs lead the pack with an annual growth rate of 45.7 percent, followed by FPGAs with 36.8 percent and SPLDs with a decline of 2.1 percent. Growth rates can be deceiving because of the differences in the dollar bases. FPGAs continued to dominate the market by growing about $121 million in 1994 for a total market of $450 million, compared to a $96 million dollar increase for CPLDs for a total market of $306 million in 1994. SPLDs declined about $8 million in 1994 for a total market of $378 million. MOS/BiCMOS PLD growth came at the expense of bipolar PLDs, which dropped $73 million for a total 1994 market of $175 million.

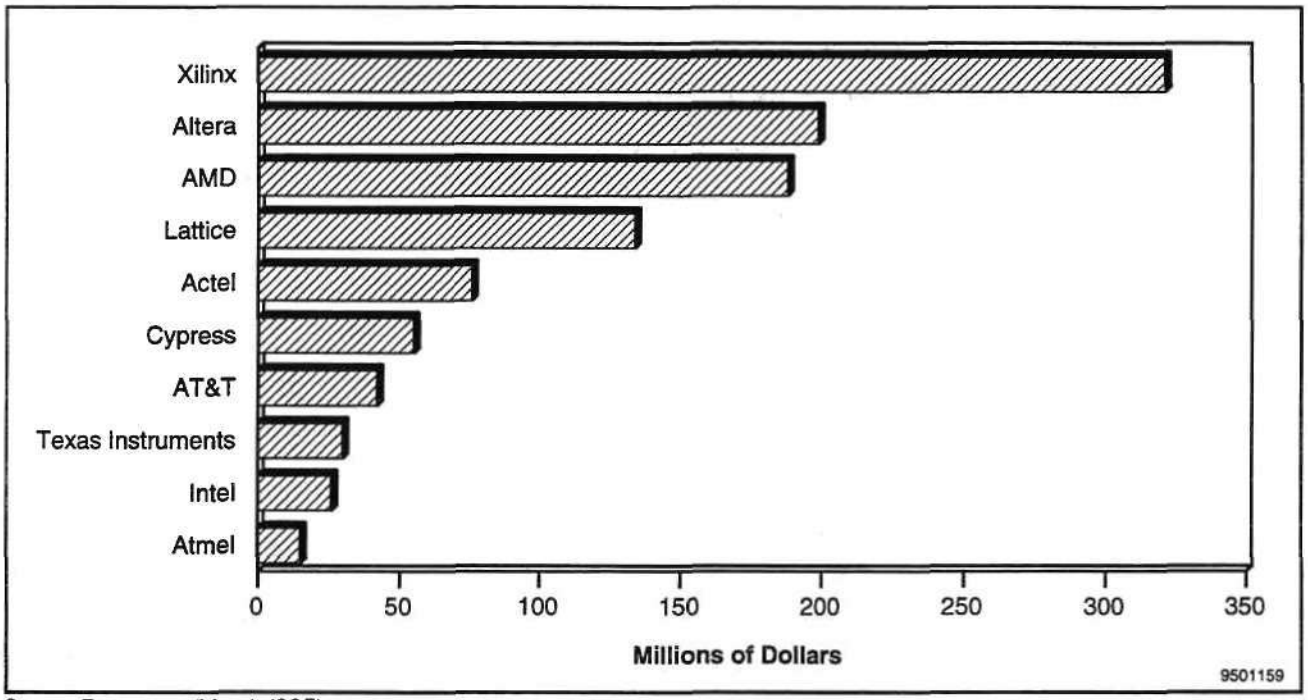
Figure 11 shows the top 10 1994 worldwide PLD suppliers' revenue by technology, while Figure 12 and Table 5 show the leaders in the hotly contested MOS/BiCMOS PLD market.

Figure 11
1994 Top 10 Worldwide PLD Suppliers



Source: Dataquest (March 1995)

Figure 12
1994 Top 10 Worldwide MOS/BiCMOS PLD Suppliers



Source: Dataquest (March 1995)

Table 5
1994 Worldwide Market Share Ranking: MOS/BiCMOS PLD (Millions of Dollars)

1994 Rank	1993 Rank		1993 Revenue	1994 Revenue	Percentage Change (%)	1994 Market Share (%)
1	1	Xilinx	231	321	39	28.3
2	3	Altera	140	199	42	17.5
3	2	Advanced Micro Devices	160	188	18	16.6
4	4	Lattice	127	134	6	11.8
5	5	Actel	60	76	27	6.7
6	6	Cypress Semiconductor	47	55	17	4.9
7	8	AT&T	32	42	31	3.7
8	9	Texas Instruments	29	30	3	2.6
9	7	Intel	45	26	-42	2.3
10	11	Atmel	12	15	25	1.3

Source: Dataquest (March 1995)

Noteworthy points regarding the 1994 PLD rankings include the following:

- Xilinx passed AMD for the No. 1 supplier in total PLDs with an exclusive MOS PLD product line.
- Altera passed AMD to capture the No. 2 position in MOS PLDs by growing 42 percent, compared to AMD's 18 percent.

- To accurately reflect the sale of Intel's PLD Division to Altera, the first three quarters of Intel's 1994 PLD revenue is included under Intel, and the last quarter's revenue is included in Altera's revenue.
- Actel outpaced the MOS PLD market in 1994 with 27 percent growth and is well-positioned with the recent acquisition of TI's FPGA business for a battle with Lattice for the No. 4 position.
- Although Lattice's MOS PLD sales only grew 6 percent in 1994, the company doubled its CPLDs sales, which helps position it for stronger growth in 1995.

Dataquest Perspective

The ASIC wave continues to grow in size and power as the 1994 market exceeded $10 billion with nearly 20 percent growth. LSI Logic, the largest merchant ASIC supplier, posted record sales and profits during 1994. LSI Logic's net income after tax (profits) increased from 7.5 percent of its 1993 sales to 12.1 percent of 1994 sales. The ASIC market is growing and is profitable for those companies that have invested in three key areas: intellectual property, value-added cell libraries, and system knowledge.

The low-density market (fewer than 20,000 gates) is now being ruled by a half dozen FPGA and CPLD suppliers that have a major patent position in device architectures. These companies enjoy rising revenue streams as well as healthy profit margins because of their intellectual property position.

On the other end of the spectrum, the high-density market (more than 100,000 gates), ASIC suppliers that have established value-added cell libraries targeted at specific applications are the most profitable. System knowledge is critical in developing complete, focused cell libraries where system designers can differentiate their systems. The market is quickly moving to system-level integration (SLI) where the entire system or subsystems can be implemented on a single chip. Such high integration requires a solid understanding of system design, design tools, library support, and test methodologies.

Cell-based ICs are gaining momentum as the preferred ASIC product for high-density designs and SLI because of their small die size. Embedded gate arrays (megacells such as SRAM diffused into the gate array base wafer) have also become a viable option for the high-end market because of their improved time to market over CBICs. As sub-0.35-micron, four- and five-layer-metal, 2-million-gate ASICs become common, we believe that CBICs will offer only minor advantages over the high utilization and quick time-to-market benefits of embedded gate arrays.

The need for system designers to differentiate their systems to achieve higher profit margins is driving the growth of the ASIC market. Although revenue will continue to grow for most ASIC suppliers, profits will only increase for those suppliers that continue to invest in intellectual property, focused cell libraries, and system knowledge.

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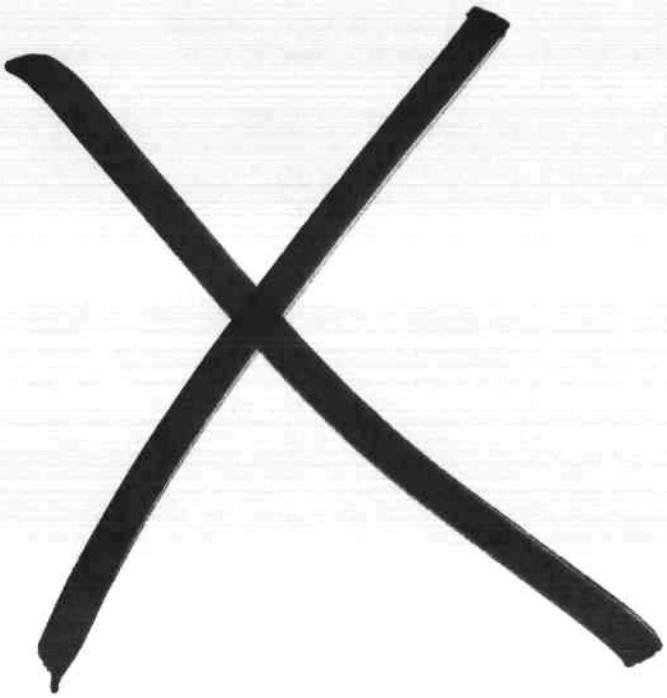

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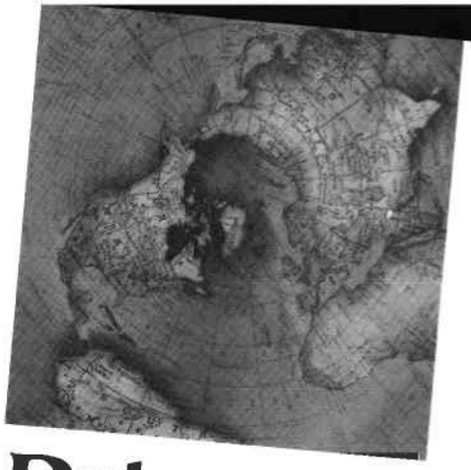

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Dataquest Research Methodology

Guides

Product Code: RSOP-NA-GU-9501
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Chapter 1
Introduction

Fundamental to the way Dataquest conducts its research is the underlying philosophy that the best research and analysis uses appropriate methodology. Such methodology includes a balance between primary and secondary data collection; between supply-side, vendor-based analysis and demand-side, consumer-preference analysis; between focused, industry-specific research and coordinated, "big picture" analysis; and between the informed, insightful perspectives of experienced industry professionals and the rigorous, disciplined techniques of seasoned market researchers. Ultimately, this leads to a balance between data and analysis—the combination of which provides unique insight and maximum tangible value to our clients.

The purpose of the Dataquest Research Methodology Guide is to provide a clear and concise overview of Dataquest's research methodologies. This guide discusses research methodology as it pertains to vendor-based research, user-based research, and market forecasting.

Each methodology is discussed separately for explanatory clarity. In no way does this organization imply that one type of research is done in isolation of the other types. For example, vendor-based research, user-based research, and market forecasts all rely on the services provided by both primary and secondary research. Also, results from vendor-based research and user-based research are inputs to market forecasting. Indeed, the free flow of information among the different research specialties creates synergy that is key to Dataquest's research methodology.

Dataquest is committed to a rigorous research methodology. Dataquest applies accepted market research techniques to the dynamic world of changing technology, fluctuating business conditions, and evolving client needs. The methodologies described in this document serve the multiple needs of our clients in a constantly changing marketplace.

Chapter 2
Research Methods

Dataquest recognizes the importance of a variety of information sources and the impact they have on the value of the services we provide. Dataquest conducts primary market research as well as secondary research to produce timely, detailed, and accurate analyses of high-technology marketplaces. The combination of these two research approaches yields a rich pool of data that can be used to answer specific questions, to produce market statistics, and to analyze and forecast industry trends.

Primary research can be distinguished from secondary research in several important ways, as follows:

- Primary information is first-hand data collected by the researcher. Secondary research is information that already has been published and typically is bought for research purposes.
- Primary research is custom research in areas where data or information does not previously exist. On the other hand, much of the secondary information has been compiled and published for some particular purpose other than market research.
- Availability is another key distinction between primary and secondary research. Primary research is proprietary data and available on a selective basis. Secondary research is public information and is more readily available.

Dataquest views primary and secondary research as complementary components in its data gathering, drawing on each to produce vital information for high-tech markets.

Primary Research

Dataquest relies heavily on primary research as a means to collect original data. Primary research is conducted with end users in business, households, government, and schools; and with product vendors, suppliers, manufacturers, and distributors. Primary information is collected by Dataquest's in-house field interviewing groups as well as by industry analysts worldwide.

There are three basic interviewing methods used by Dataquest: telephone interviews, mail interviews, and personal interviews. The method used is determined by the objective of the project.

Telephone Interviews

Dataquest uses telephone-based field interviewing for much of its primary research. This method is usually employed when the study design requires a large, randomly selected sample from a population, when eligibility is difficult to determine (necessitating many contacts for a completed interview), when the interview is relatively short, or when face-to-face contact is impossible or unnecessary. In some cases, questionnaires are faxed to the respondent prior to the telephone interview.

Telephone interviewing is conducted regularly by Dataquest's in-house field interviewing groups in San Jose and the United Kingdom. The charter of Dataquest's field interviewing groups is to collect and ensure quality data in a timely and cost-effective manner. These objectives are possible because of the following competitive advantages unique to Dataquest's interviewing group:

- Dataquest uses interviewers who specialize by industry, ensuring consistent, high-quality information.
- Dataquest has complete access to information-gathering resources.
- Dataquest experiences increased productivity because of industry contacts and knowledge of technologies.

Dataquest's San Jose facility conducts interviews in North America, South America, Japan, and Asia/Pacific. Interviewing in Japan is also conducted from Dataquest's Tokyo office. Dataquest's Primary Research Centre, located in the United Kingdom, conducts interviews in 12 languages throughout the European region.

Central location interviewing has many advantages. It allows for central monitoring to ensure that correct interviewing procedures are being followed. Furthermore, if a respondent requests clarification on the meaning or intent of a question, it can be handled on the spot.

Dataquest's field interviewers participate in a briefing on each project prior to implementation. Interviewers are trained specifically in handling open-ended questions and questions that ask for "other" responses.

Mail Questionnaires

Dataquest uses mail questionnaires infrequently for the following three reasons:

- Low response rate—Mail surveys have a lower response rate than do personal or telephone interviews. The danger with low response rates is that those who return the questionnaires may be "different" from or not representative of the universe of respondents, thereby introducing bias.
- Accuracy—There is no interviewer in mail surveys who can explain the purpose of the project, clarify the questions, or resolve any problems. Respondent confusion about the questions can adversely affect survey accuracy.
- Time—It takes several weeks to conduct a mail survey, and most clients cannot wait that long.

Mail surveys cannot be used for an unstructured study in which the interviewer formulates the questions as the interview progresses. Personal and telephone interviews are more flexible in that they can be terminated or altered at any point, whereas mail surveys are inflexible.

Paper and pencil questionnaires are used in some specialized situations such as trade conferences and other group meetings.

Personal Interviews

Personal interviews are less structured and more intensive than phone interviews. There is a longer and more flexible relationship with the respondent, resulting in data that has more depth and richness.

There are two basic types of personal interviews: nonstructured and semistructured. Nonstructured and semistructured interviews differ in the amount of guidance given by the interviewer. In the nonstructured interview, the respondent is given considerable freedom to respond within the bounds of topics specified by the interviewer. In semistructured interviews, the interviewers have a specific list of topics to cover with the respondent.

Focus groups are another form of personal interviews. Focus groups consist of 8 to 12 people who gather for two to three hours with a trained group facilitator to discuss a product, service, organization, or other marketing entity. The participants are paid an honorarium for attending. The meeting is held in a focus group room equipped with a two-way mirror for filming and observation. The group facilitator encourages remarks from the participants, while at the same time focusing their discussion. The comments are tape-recorded and analyzed.

Secondary Research

Dataquest recognizes the importance of secondary research in all its analytical and intelligence functions. Although secondary information alone does not answer complex market research questions, secondary research has major advantages and roles in the market research process. Dataquest uses secondary information for the following:

- Provide basic working knowledge of industries
- Gather facts about the technology, products, and applications
- Monitor developments
- Explore new territory or emerging technologies
- Gain insight for preliminary analysis
- Signal need for primary research
- Gather information quickly and at a lower cost than primary research

In conducting secondary research, Dataquest employs a methodology to ensure that appropriate information is obtained to meet the diverse needs of its researchers. With a process-oriented approach, Dataquest is not only able to achieve time and cost efficiencies but is also able to focus on finding the desired data from the pool of secondary information that exists. This process can be summarized as follows:

- Define the topic and data points to be collected
- Select secondary sources to search
- Conduct information search through multiple sources, using electronic databases, CD-ROMs, and print resources
- Assemble and review information from all sources
- Present results of the information gathered

Because an impressive amount of secondary information exists concerning high-technology industries and the companies within these markets, Dataquest's researchers routinely use secondary research in the following key areas:

- Market sizing
- Validating estimates
- Cross-checking information, such as market share
- Checking trends that influence markets
- Checking company growth rates
- Verifying shipment totals and pricing information
- Supporting assumptions used in forecasting

Because our researchers and analysts are expected to review all types of information to keep abreast of market trends and industry events, Dataquest understands that access to information is a crucial part of the market research process. Dataquest has invested substantial resources to ensure that current information is available and accessible by all research staff.

The secondary research process is managed by professional librarians who understand how and where to get the secondary information necessary to support the needs of analysts and researchers. Dataquest's librarians are expert not only in searching all types of information sources but also in selecting and obtaining key resources that researchers need on a frequent basis. The librarians work closely with the research staff to answer the complex questions that arise during the course of our market research.

Each major Dataquest location maintains a library facility that typically offers a comprehensive collection of information sources covering the full range of high-technology companies, markets, and industries tracked by Dataquest. Sources of secondary information typically utilized by Dataquest include the following:

- Articles in the general business and trade press
- Financial information from annual reports and other SEC documents
- Company and product directories
- Company press releases and product literature
- Government reports, statistics, and economic data
- Trade association data
- Credit reports

In-house research collections are supplemented by online database services including Dialog, Lexis/Nexis, Dow Jones, Newsnet, Data-Star, CompuServe, and the Internet. Other specialized databases from such companies as Dun & Bradstreet and Thomson Financial are also available to the research staff.

The benefits of buying secondary information on CD-ROM were recognized a number of years ago, and Dataquest became an early adopter of this information format. Today we have numerous CD-ROMs available in the library and on the local area network for retrieving financial information, trade press articles, product information, and company profiles. Because of the high information content and ease of use of these products, these resources are used heavily by our research staff.

In addition, Dataquest has made a significant investment and commitment to supplying every analyst with current secondary information on the desktop. Our analysts use a state-of-the-art electronic information filtering system, which delivers real-time information feeds from such companies as Dow Jones, Business Wire, PR Newswire, and Ziff. In 1995, the analyst desktop will be further enhanced with several other news and wire services and full Internet access.

Chapter 3
Vendor-Based Research

Each year, Dataquest tracks the shipments and revenue of thousands of vendors worldwide. This research helps Dataquest maintain a dynamic database of product shipments by company, and product consumption by region of the world.

Dataquest conducts product market share surveys on a quarterly, semi-annual, or annual basis. The annual market share research actually includes two phases—a preliminary phase and a final survey. The preliminary estimates are completed by the end of the calendar year being reported, and the results are summarized in a report released early in the new year. Preliminary vendor rankings are featured in a Dataquest press release. Final market share estimates are prepared during the first quarter, and the results are published in a reference report released in the spring.

Dataquest believes that the estimates presented in its market share documents are the most accurate and meaningful statistics available. While Dataquest takes care in gathering, analyzing, and categorizing its data, clients must be aware of the definitions and assumptions that Dataquest uses when they interpret the estimates presented in the market statistics documents. Other companies, government agencies, and trade associations may use slightly different definitions of product categories and regional groupings, thereby reporting different results. These differences should be kept in mind when making comparisons between data provided by Dataquest and data provided by other suppliers.

Dataquest's Methodology

Dataquest's vendor-based research incorporates both market sizing and market share research activities.

Market Size

Market size is defined as the universe of all companies competing in a market. The universe of companies is based on a core list of companies that Dataquest has developed over time. Each year, Dataquest checks the list to add companies previously not included and to delete companies no longer competing in the market.

Dataquest uses its proprietary market sizing bibliography as a foundation for market sizing research. The market sizing bibliography describes sources of information that identify companies participating in various markets. These sources include industry associations, business and financial sources, and other secondary sources. Dataquest analysts search these sources to develop a list of companies that is as comprehensive as possible. Special attention is devoted to identifying companies not included in our previous data collection.

Once the universe of companies in an industry is identified, researchers estimate the approximate size of each company. Size is one of the variables used in identifying a company as a leading vendor and as a company that Dataquest will track in greater detail. The largest companies are usually

considered to be leading vendors in an industry. In addition to size, identification of a company as a vendor that merits more detailed attention is based on our ongoing relationships with industry contacts and industry events.

Smaller companies in each market are also noted. Shipments and revenue for smaller companies are estimated using the same general procedures applied to larger companies. The data from smaller companies is usually aggregated and reported as "other companies." These estimates are incorporated into overall market size statistics.

Market Share

The purpose of market share is to estimate the presence of a leading vendor in a product market. Market presence may be measured in terms of unit shipments or revenue. Market share is critical for companies to assess their absolute and relative position in a market and thus to develop appropriate competitive strategies.

Definitions

The Dataquest Market Definitions books are the corporatewide reference for segmentation and definition of technologies and markets. Definitions explain Dataquest's understanding of technologies. Segmentation refers to the way in which a market is divided into different dimensions, including companies, products, regions, distribution, applications, and user environments. These dimensions are illustrated in Figure 3-1. The segmentation and definitions found in the Dataquest Market Definitions books are used consistently throughout Dataquest's products and within all Dataquest's worldwide offices.

Dataquest has defined regions of the world for the purposes of tracking and reporting markets, companies and products, and company production and consumption. Those regions are North America, Europe, Japan, Asia/Pacific, and Rest of World. The country composition of these regions is given in the Dataquest Market Definitions books and in Appendix B.

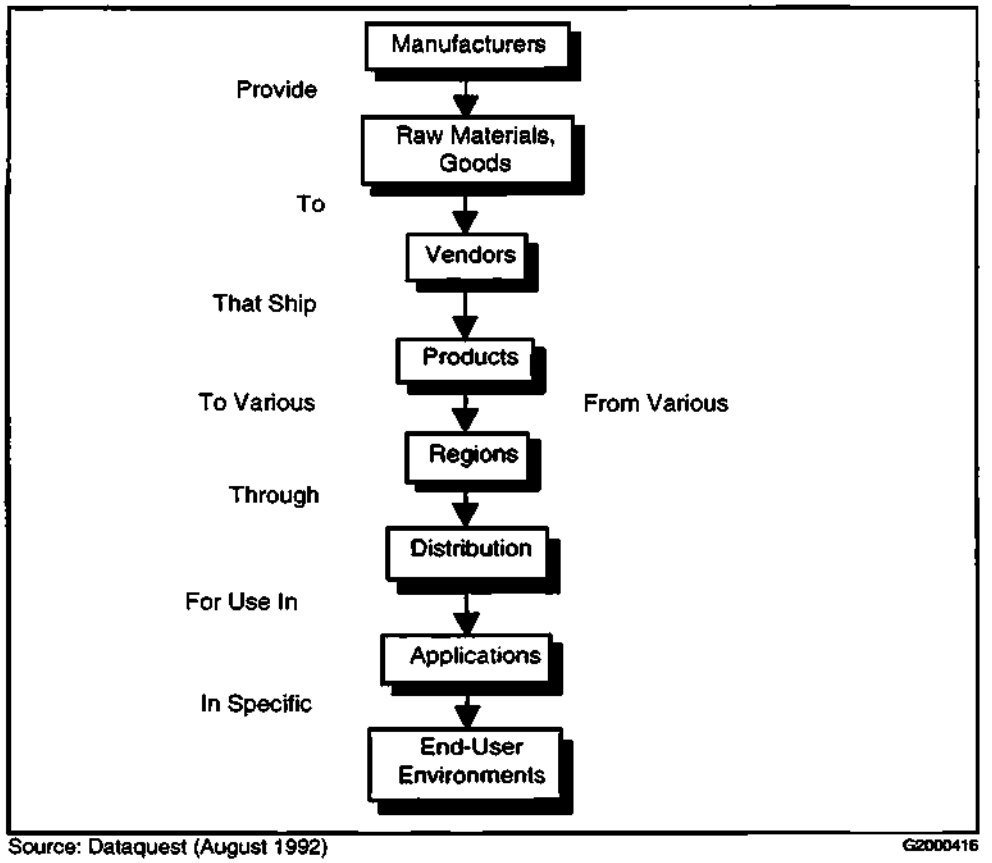
Shipment Estimates

Dataquest prepares estimates of shipments for each product and company prior to market share data collection. Shipments are estimated at the most disaggregate level possible (such as by company, by product, or by region). These initial estimates are based on the following:

- Company year-to-date performance
- Validating information, such as press releases, Wall Street news items, industry contacts, and online sources
- Dataquest forecasts of product revenue and shipments, by product and by regional market

Initial estimates represent Dataquest's best estimate of company performance during the previous year. The estimates are treated as confidential.

Figure 3-1
Dataquest's Research Dimensions



Source: Dataquest (August 1992) G2000416

Data Collection

Data collected in our vendor surveys is used in a bottom-up analysis defining market revenue, market size, and market share. Market share data collection involves virtually all Dataquest researchers and interviewers. Dataquest estimates of product shipments and revenue for the year are provided to each company. The company is asked to respond to Dataquest with revisions or corrections as appropriate.

The accuracy of information provided to Dataquest varies. Some companies are known for consistently reporting accurate numbers, whereas other companies are less uniform in their reporting practices. With experience, analysts become familiar with the different and varied reporting styles of the companies involved.

Dataquest analysts cross-check all information with the goal of defining the most accurate estimate possible. This effort requires the ability to integrate information from different sources. It relies on the analyst's ability to perceive and process information provided indirectly. The skill and sensitivity of the individual researcher is a critical element.

Collection of top-level aggregate data (worldwide and regional unit shipments and revenue) from a vendor is the responsibility of the Dataquest

office located within the same region of the world as the vendor being surveyed. Collection of bottom-up disaggregate data (regional and country shipments of each vendor) is the responsibility of the Dataquest office located within the region of consumption. The rationale for this division of labor is that the Dataquest office located within a particular region is best suited to perform data collection tasks related to manufacturers located within that region. The local Dataquest office is also most able to comment on facets of consumption within that region, regardless of the location of company headquarters.

For example, Dataquest San Jose is responsible for data estimation and collection for North America-based vendors and their worldwide and regional shipments. Similarly, Dataquest Europe estimates and collects data on worldwide and regional shipments for European vendors; Dataquest Japan is responsible for the estimates and collection of worldwide and regional shipments for Japanese vendors. Dataquest Asia/Pacific estimates and collects the worldwide shipments data for vendors in the Asia/Pacific region. Vendors located in the Rest-of-World region are, in most cases, the responsibility of Dataquest San Jose. This assignment forces a reconciliation between Dataquest's analysts and Dataquest's offices, resulting in a single worldwide estimate for any given product.

Once the vendor-based data is collected, it is compiled into a single, market-specific database. Subsets of the data based upon the region of consumption are then furnished to Dataquest's regional offices. The regional analysts examine their specific regional consumption data (worldwide vendors' shipments into their regions) and compare the estimates to the results of their individual regional data collection efforts.

This methodology capitalizes on the advantage provided by Dataquest's regional analysts. It supports regional analysts, by strength of their location, in collecting data from vendors based within their region. Furthermore, it allows for differences in regional pricing, distribution methods, and application usages, and their effects on the market share estimates. At the same time, this methodology allows the regional analysts to examine the shipment data of worldwide vendors into their region in order to account for differences within their region of the marketplace.

An additional advantage of this approach is the assignment of ultimate responsibility for a particular vendor to a particular analyst. This assignment forces a running dialogue and information exchange among offices.

Quality Control and Validation

All market share data is validated through cross-checks to assure quality, including the following:

- Checking aggregate data against at least two other data points
- Checking large market share changes
- Checking large volume changes
- Checking current trends against historical trends
- Checking against complementary or substitute products

- Checking against installed base
- Checking against other Dataquest data
- Checking company growth rates against competitors

Dataquest utilizes both primary and secondary sources to produce market statistics data. Primary research is supplemented with secondary research to verify market size, shipment totals, and pricing information. Either primary or secondary information is used to validate estimates. Where data cannot be collected from primary sources, estimates are checked against secondary sources. Revenue reported in one market covered by a vendor is also evaluated against that vendor's revenue in other markets covered by Dataquest to make sure that revenue is not double counted. In addition, Dataquest may check with multiple sources at one company to verify data.

The data collected in our vendor surveys is considered public information. The names of respondents are always kept confidential, and all data is published as Dataquest estimates. All respondents are notified of Dataquest policies when market estimates are initially sent.

Companies in the market share survey review Dataquest's initial estimates and respond with their comments or revisions. If a company chooses not to participate in the data collection effort, Dataquest either uses initial estimates or adjusts the initial estimates based on responses by other companies.

Documentation

Detailed notes and documentation are maintained on each company surveyed in the market share sample, as well as the supplemental group of companies used to estimate total market size. Documentation includes handwritten notations indicating sources of data and any relevant secondary information.

Quarterly and Semiannual Shipments and Pricing

Dataquest monitors selected companies on a monthly, quarterly, or semiannual basis. Typically, this research and analysis focuses on unit shipments and product pricing of the most important leading companies in a market. Companies selected for this in-depth research have products that meet the following criteria:

- Significantly greater than average growth
- "Bell-weather" indicators of future market activity
- Receive disproportionate market-participant attention

The purpose of this in-depth research is to assure that Dataquest estimates are timely and to report important market shifts. This research serves as valuable input for updating expectations of short-range market activity.

Chapter 4
User-Based Research

User-based research serves as a complement to Dataquest's vendor-based research. By focusing on the consumer, user-based research reflects the demand-side of product markets. Dataquest's user-based research includes studies of market penetration, installed base, technology plans, product configurations, product pricing and positioning, customer satisfaction, and new product testing and concept evaluations.

Project Design

The most important aspect of user-based research is to define the purpose of the research. What question does the client want answered? If there are multiple questions, what is the main question? Once the project's purpose is identified, a project plan is prepared to guide research activity. The plan covers the entire range of research activity, including definition of research objectives, questionnaire development, sample design, field interviewing, statistical analysis, and the final report. It also includes a time line and milestones that can be used to assess progress.

Questionnaire Development

Questionnaires are developed in consultation with the project leader or client. Questions are phrased in a form that will facilitate complete and usable responses. Special attention is devoted to minimizing response biases potentially caused by such factors as answer order, question order, generalization, and scaling.

Questionnaires typically contain the following three main sections:

- Introduction and screener page that outlines the purpose of the study and identifies the correct person to participate in the interview
- Specific questions to meet the project's objectives
- Demographic questions that enable the respondents to be grouped together and the data analyzed in subsets

Sample Design

Sample design involves definition of sample parameters, determination of the sample approach, and the most appropriate source for the sample. Sample parameters are determined according to the population of interest in the study. For example, a survey of corporate computer use would likely include parameters such as the number of employees and annual sales. A study measuring users' interest level in video games would include sample parameters such as household composition and annual household income.

Once the sample parameters have been defined, a sampling approach is developed. Dataquest uses two types of sampling approaches: probability sampling and quota sampling.

Probability sampling is used for data to be projected to the population at large, such as market penetration data. In this approach, each potential respondent has an equal probability of being selected. A study that

requires 200 completed interviews would begin with names of 1,000 potential respondents if the anticipated response rate is 20 percent.

Quota sampling is an alternative to probability sampling and is used when simplicity and cost-effectiveness are important considerations. In quota sampling, a profile of the population to be studied is developed and quotas are set so that the final sample is forced to fit the main population profile. An example would be a study of U.S. business establishments with results reported by industry. The 1990 U.S. Census data reveal that government institutions represent approximately 3 percent of U.S. business establishments, services represent 31 percent, manufacturing represents 7 percent, and other businesses represent 59 percent. For a study requiring 500 completed interviews, quotas would be set so that 15 respondents would come from government institutions, 155 respondents would come from services, 35 respondents would be from manufacturing businesses, and 295 respondents would represent other businesses.

Dataquest uses a variety of sampling sources depending on the nature of the research. Databases from Dun & Bradstreet, including Dun's Marketing Service databases of 10 million U.S. businesses, are frequently used. Other sources include UCC1 filings that identify sites with specific computer and telecommunications equipment, and mailing lists from industry trade publications. Dataquest also has proprietary respondent databases that are used for research in specific high-technology markets.

Data Collection

Data collection in end-user research relies heavily on primary research. Dataquest's primary research procedures are described in detail in an earlier section of this document.

Dataquest maintains sizable primary research units in San Jose, California, and High Wycombe, United Kingdom. In addition, staff responsible for primary research data collection are located in Hong Kong, Singapore, Tokyo, Seoul, Taiwan, and Framingham, Massachusetts.

Preparation for the primary research includes in-depth briefings with the interviewers to review details of the project, the questionnaire, and procedures for collecting information. At the beginning of the project, preliminary interviews are conducted to validate the effectiveness of the questionnaire. Suggested changes can then be discussed and incorporated into the final questionnaire. The actual interviews are conducted online or with hard copy, depending on the format most appropriate for the objective of the study. Considerable time goes into quality control. The interview process is carefully monitored, and responses are reviewed for accuracy and completeness at all stages of a project.

Data Analysis

Dataquest uses a full range of methods to conduct statistical analysis of user-based data. After data collection is completed, the data is cleaned and prepared for analysis. As a quality-control check, frequency and percentage data are calculated for each response to every question.

Specific cuts of data are determined jointly by Dataquest and the client. Initial tables are produced according to predetermined specifications.

Once the initial tables are reviewed, the need for further cuts of data often becomes apparent. An iterative process then occurs in which questions are formulated, additional analyses are conducted, and new sets of tables are prepared.

A variety of data analysis techniques are used to answer Dataquest's research questions. Techniques commonly used include validity and reliability testing, correlations, regression analysis, factor analysis, analysis of variances, and significance testing. Dataquest also measures customer satisfaction and importance ratings using a matrix gap analysis technique. The statistical analysis packages used to analyze data at Dataquest include SPSS, Survey System, and ACA/Ci2.

Chapter 5
Market Forecasting

Dataquest's charter includes the task of forecasting high-technology markets. There are two important benefits of forecasting market activity, as follows:

- Forecasting provides a structured and logically rigorous setting in which to clarify expectations about the future. This structured setting maximizes the likelihood of generating forecasts that are internally consistent.
- Forecasts help reduce business risk by aiding executives in planning strategy and tactics based on likely events and trends.

There are two basic components to Dataquest's forecasting methodology: theory and facts. Theory and facts are complementary— one cannot be substituted for the other. Theory provides a simplified situation with the same logical structure as more complicated reality, and it uses the former to understand the latter. Facts may appear to be self-evident; however, facts do not "speak for themselves." To use facts effectively, they must be interpreted in terms of an underlying structure, embodied in a theory.

Dataquest forecasts begin with facts about real-world events. Most generally, facts regarding the real world include level of economic activity, prices, technology characteristics, user demographics, political environment, and other exogenous or outside influences.

Facts lead to data representing observations. Data is broadly classified as either demand-side or supply-side, depending on the side of the market it influences. Empirical methods combine data with economic theory to yield market analysis and forecasts.

Figure 5-1 outlines the key elements and flow of Dataquest's forecasting methodology.

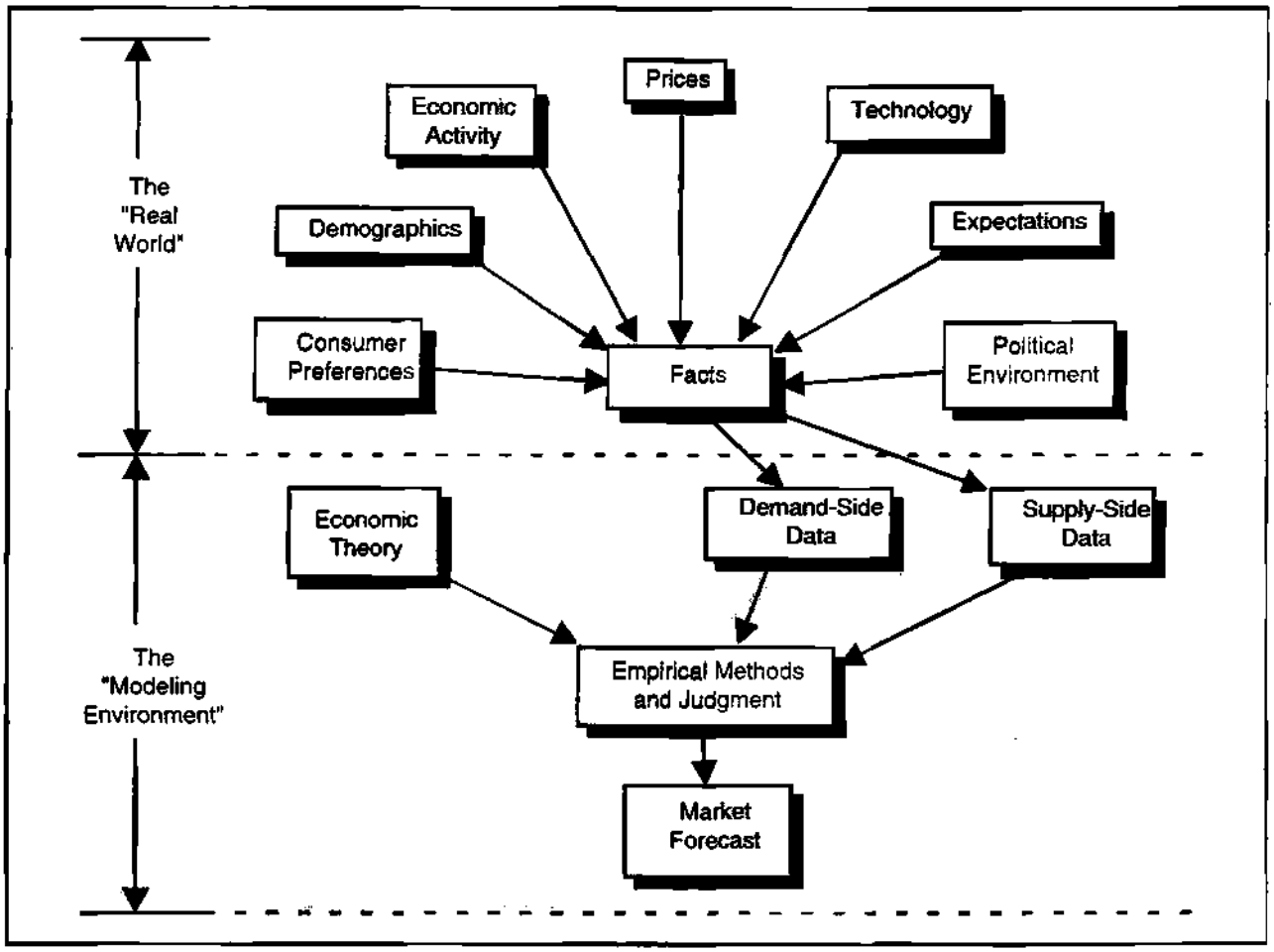
Theoretical Framework, Variables, and Data

High-technology markets are complex; furthermore, high-technology markets generate an abundance of facts. The volume of high-technology publications and information is evidence of this situation. Therefore, before generating a market forecast, it is necessary to reduce the market's complexity to a manageable level with a simplifying conceptual framework, typically referred to as an analytical model.

Dataquest uses standard microeconomic models as the basic theoretical framework for analyzing high-technology markets. These models include the following:

- Models of consumer behavior to analyze the demand side of a market
- Models of production, the company, and the industry to analyze the supply side of a market
- Models of market supply and demand

Figure 5-1
Dataquest's Forecasting Methodology



Source: Dataquest (August 1992)

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These models are the accepted paradigms for analyzing economic and market phenomena. They have withstood years of rigorous empirical testing and verification.

High-technology markets also yield an abundant flow of facts about real-world events. These facts lead to a set of data, representing observations such as unit shipments, revenue, market share, and average selling prices. Dataquest classifies this data according to broad categories called variables that are grouped as demand-side variables or supply-side variables.

Dataquest includes the following demand-side variables in its product forecasts:

- Overall level of economic and business activity, industry conditions, and related industry conditions
- Prices of substitute products
- Prices of complementary products
- Expected future prices of the product being forecast

- Consumer preferences
- Demographics

Dataquest also includes the following supply-side variables in its product forecasts:

- Prices of resources and inputs used in a product's production
- Technological improvements that allow for decreases in the cost of production
- Outside factors that may alter supply or influence a company's production costs, such as trade barriers

Some variables are more easily quantified than others. For example, a country's overall level of economic activity can be measured directly by estimating its gross domestic product (GDP). Product prices and resource prices are normally directly observable as well. Other variables are more elusive and intangible. Information on consumer tastes and preferences may have to be sampled. Likewise, expectations of future products and resource prices are not directly observable but must be inferred. Thus, a variable's consideration does not necessarily imply collection of the corresponding data.

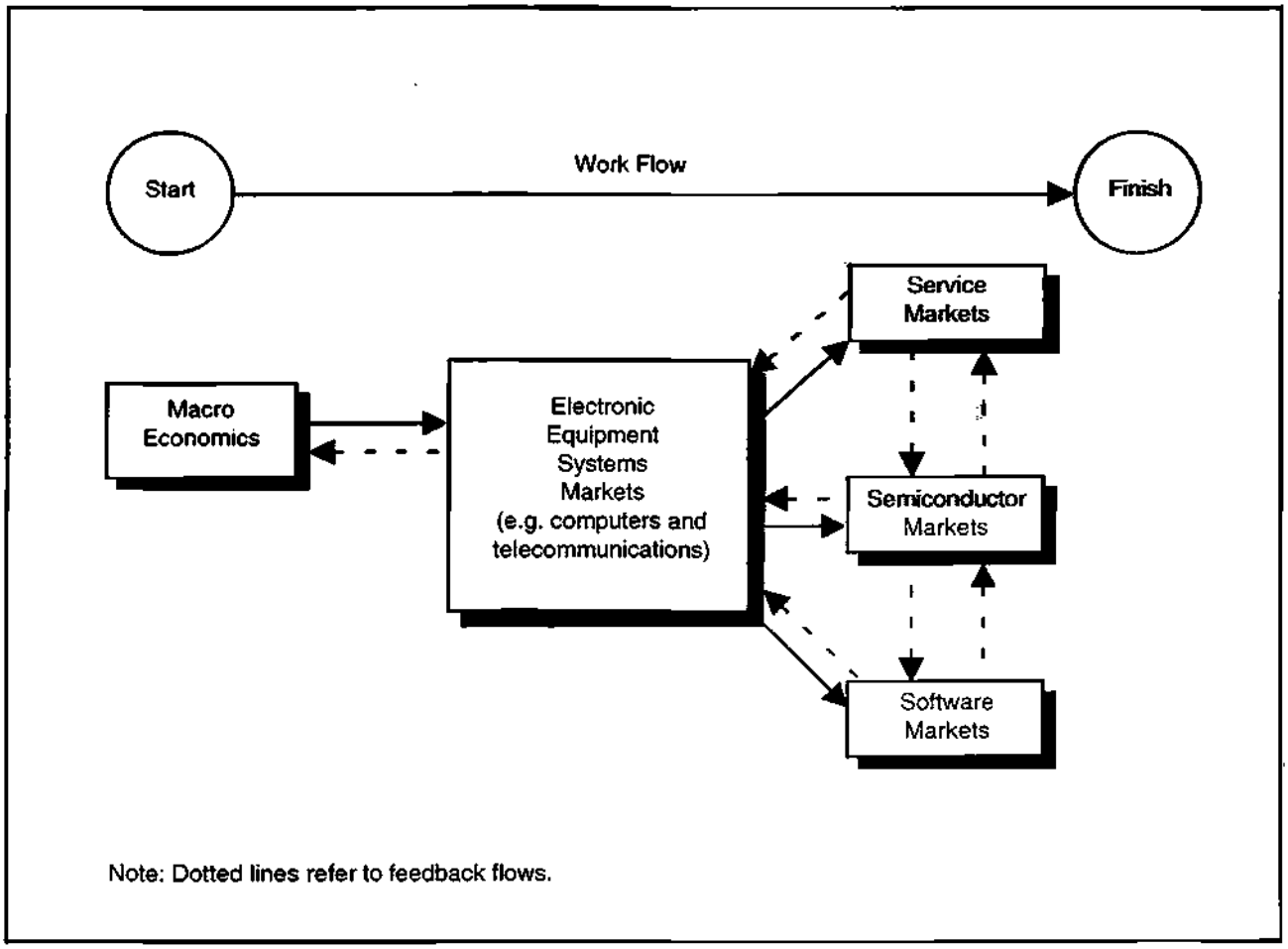
Examples of specific data used in Dataquest forecasts include the following:

- Unit consumption and production
- Consumption and production revenue
- Average selling price (final user price, list price, and manufacturer price)
- Installed base, saturation, and retirements
- Input/output (I/O) ratios and tie ratios
- Market penetration and total available market (TAM)

Supply and demand market models have the added advantage of maximizing the internal consistency of Dataquest's numerous forecasts. By modeling and forecasting the supply side and the demand side of a product, Dataquest analysts are able to check for "market clearing." The principle of market clearing states that whatever quantity of a product is supplied to a market must by necessity find a "home" in the market, either with the final or ultimate user or in inventory, and vice versa. In other words, after the fact, supply equals demand. (This does not imply that planned supply necessarily equals planned demand.) Whatever inconsistencies arise in the modeling and forecasting process must be eliminated or rationalized by changes in inventory levels or prices, or both.

Another check for internal consistency makes use of the high-technology food chain (see Figure 5-2). The high-technology food chain is the simplified conceptual arrangement of the production of high-technology goods according to the order of utilization. In the food-chain approach, each product uses the preceding product as an input to production. For example, integrated circuits (ICs) are produced from silicon wafers,

Figure 5-2
The High-Technology Food Chain



Source: Dataquest (August 1992)
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workstations are produced from ICs, and so on. By checking product flows through the food chain, Dataquest is able to monitor the consistency of its various forecasts at different stages of the food chain. In addition, modeling the food chain enables Dataquest to forecast possible production bottlenecks and their implications for other product markets.

At the beginning of each forecast cycle, Dataquest assesses current and expected international macroeconomic conditions. Dataquest uses the macroeconomic forecasts and analysis developed by the Economic Analysis Department of The Dun & Bradstreet Corporation.

In the next stage, given the macroeconomic outlook, forecasts of the electronic equipment systems markets are developed. At this stage, effort is concentrated on the systems markets and the important variables that influence these markets. All other things are held constant.

In the final stage, given the macroeconomic outlook and the systems outlook, forecasts of the semiconductor, software, and services markets are developed. Again, all other things are held constant; feedback from the semiconductor, software, and services markets to the systems markets, and the economy in general, are ignored.

The serial flow of effort just described should not be construed to imply that there is not a free forward or backward flow of communication between, for example, workstation analysts and semiconductor analysts; or lateral communication between, for example, mainframe analysts and personal computer analysts, or between semiconductor analysts and software analysts. The purpose of Dataquest's forecasting framework is to mirror real-world conditions and then to use the approach to logically analyze business conditions and to generate expectations about the future.

The factors or variables that are given or "held constant" are referred to as forecast assumptions. Forecast assumptions are the conditions upon which a forecast is based. A typical set of forecast assumptions includes expectations about macroeconomic conditions, currency exchange rates, technology characteristics, productive capacity, end-user market conditions, and political conditions.

While some assumptions may be universally applied to all market forecasts (macroeconomic expectations and currency exchange rates), assumptions about other markets may themselves forecast markets further up the food chain. For example, a semiconductor market forecast will use the most recent PC market forecast as a given assumption.

Long-Run Trends versus Short-Run Fluctuations

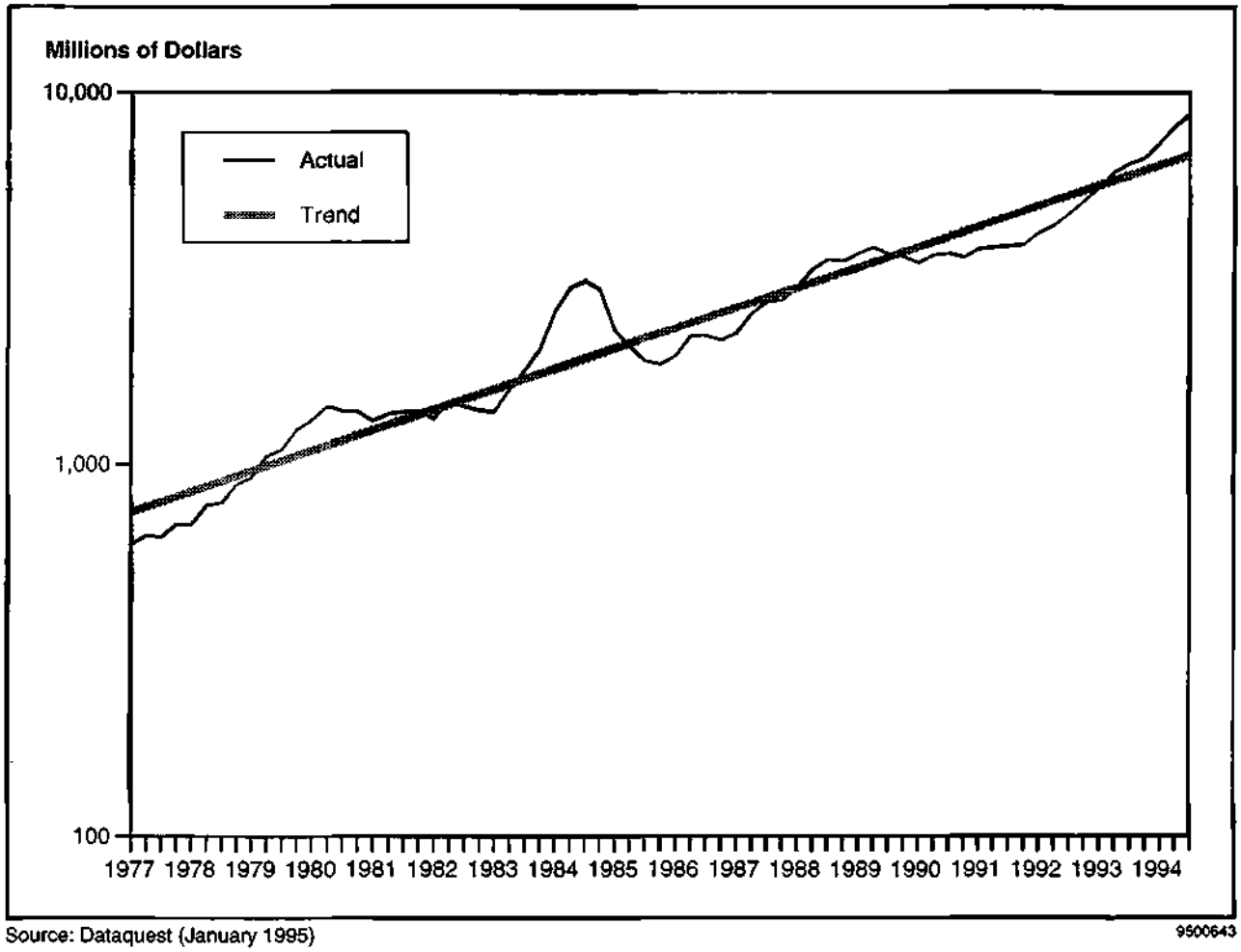
The basic thrust of the Dataquest forecasting models is that high-technology markets show short-term fluctuations around long-term trends.

The long-run equilibrium movements determine the basic trends of the markets as they grow over time. The short-run movements around the long-run equilibrium are referred to as market fluctuations.

Market fluctuations result from unexpected changes in market conditions or from changes in technology. Manufacturers' expectations about future market conditions may differ significantly from actual market conditions. As an example, personal computer manufacturers accumulated huge semiconductor inventories in 1984 and 1985 in anticipation of a boom in PC sales (see Figure 5-3). When actual PC sales fell short of the expected boom, the quantity of chips supplied to the market was greater than the quantity demanded at prevailing prices, and prices fell. Chip producers and consumers revised their plans in light of the new information and market conditions, and the market adjusted accordingly, albeit painfully. Discontinuous changes in technology may be either anticipated or unanticipated. For example, the emergence of 1Mb DRAM technology (an anticipated technological change) put a discontinuity, or a kink, in what would have been an otherwise relatively smooth revenue growth path of DRAM devices.

Seldom, if ever, does a high-technology market settle down to its long-run equilibrium long enough to grow along its trend growth path. Therefore, what we observe over time is a continuously fluctuating market tracing out its trend or long-run growth envelope. This is demonstrated in Figure 5-3. The solid line represents the actual growth path of North American market semiconductor revenue; the dotted line represents the trend growth path of revenue.

Figure 5-3
North America Semiconductor Market



Source: Dataquest (January 1995)

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The further into the future one forecasts, the greater the level of uncertainty about the expected state of a market. We have a clearer idea of events that we expect to disturb the market in the short term—and thus give rise to market fluctuations— than we do in the long term. The significance of the trend value in the final year of the forecast is that it is simply the expected value—or midpoint—of an ever-widening confidence interval or envelope. Of the range of possible future outcomes, it is the most likely or probable outcome.

Although Dataquest is constrained to forecasting under conditions of incomplete information, by no means are we completely unaware of all future events. For example, the analysts that monitor technology markets usually have information regarding manufacturing capacity at some future date. Dataquest includes such information in its forecasts.

In summary, the trend or long-range values of a forecast represent the expected value of a probability distribution of likely future outcomes. In the absence of shocks and other disturbances, high-technology markets tend to converge toward a long-run equilibrium growth path.

Empirical Methods

Microeconomic models provide a general conceptual framework to analyze market behavior. The task of forecasting, however, requires more specific, empirical models. No single empirical model or method is necessarily appropriate for forecasting all the different products and services that Dataquest follows. Furthermore, a strong case can be made for using more than one empirical model to forecast a product as a check of the robustness of a forecast.

All Dataquest empirical models combine prior information with sample data to produce forecast estimates. Prior information includes historical data of an industry, product, or market; knowledge accumulated by Dataquest analysts from industry experience; and the collective body of knowledge resident at Dataquest. Sample data consists of information that Dataquest collects and analyzes describing recent events about an industry, product, or market. Sample data is obtained through primary research, technical discussions with industry and company officials, announcements and articles in the trade press, and judgmental data based on knowledge, experience, and professional intuition.

There are four types of empirical techniques commonly used for forecasting at Dataquest.

Judgmental Methods

Judgmental methods are useful in situations where past data is scarce, causal relationships have not been identified or quantified, or some other major change has occurred in the forecasting context (such as a war or a trade agreement) that is not accounted for by other techniques. The validity of using these methods by themselves is uncertain, although using them correctly can provide very good forecasts, especially in uncertain environments. The objective of these judgmental methods is to provide logical, unbiased, and systematic quantitative estimates. Examples of judgmental methods include the Jury of Executive Opinion and the Delphi method.

Technological Methods

Technological methods are particularly appropriate for very new technologies with little or no data, or for very long range forecasting. These methods are highly exploratory, and large errors are quite likely. Examples of technological methods include curve fitting, including trend extrapolation, S-shaped curves, and envelope S-curves; and analogous data.

Time Series Models

Time-Series methods extrapolate past data into the future. The premise is that some underlying pattern exists in the variable being forecast. Examples of time series models include moving averages, exponential smoothing, decomposition models, and Box-Jenkins techniques.

Causal Models

The premise of causal models is that changes in the value of the variable of interest (for example, shipments of Product A) are closely associated with changes in some other variables (for example, the cost of Product B). Consequently, if future values of these other variables (cost of Product B) can be estimated, they can be used to forecast the desired variable (shipments of Product A). Examples of causal models include regression analysis, leading indicator analysis, and I/O models.

Forecast Quality Control

All forecasts must strictly adhere to the following guidelines to ensure internal consistency:

- The same value of a variable must be used throughout Dataquest.
- Analysts may vary the relationship between variables, according to their own research findings, but not the values of the variables.
- Not all variable relationships hold true for all industries; therefore, analysts may specify which sets of data to use.
- Data must conform to Dataquest standard segmentation.
- Final forecasts must be approved before release.
- All preliminary data is clearly stated as such.
- The source of the information and date is always cited

Ultimately, the most important and toughest quality check that Dataquest forecasts must pass before publication is the test of reasonableness. The test of reasonableness is imposed by the team of experienced Dataquest researchers and analysts. Empirical methods are indispensable to economize the task of generating forecast estimates, but they are no substitute for the seasoned intuition of practical experience.

Chapter 6
Summary

When Dataquest clients receive research and analysis with the familiar citation "Source: Dataquest," they receive the end result of a rigorous methodology involving primary and secondary data collection, supply-side and demand-side market analysis, and the cross-industry perspective afforded by Dataquest's uniquely broad and in-depth worldwide coverage of high technology.

Behind the published research is a thorough body of knowledge involving industry professionals and research experts. As a result, Dataquest's clients receive more than simply a single and solitary point of information for planning and decision making. Dataquest provides comprehensive market research to its clients, including the highest-quality vendor-based research, user-based research, and market forecasts.

Appendix A
Currency Conversion

As a worldwide company, Dataquest tracks high-technology markets and companies in five major regions of the world: North America (United States, Canada, and Mexico), Japan, Europe, Asia/Pacific, and Rest of World.

Because most high-technology companies sell their products in more than one country, and because we cannot simply aggregate foreign currencies to estimate worldwide value, we have adopted a common currency, the U.S. dollar, by which we evaluate and compare all markets and all companies. We have chosen the U.S. dollar for the following reasons:

- Since World War II, the U.S. dollar has been the major reserve currency of choice for industrialized nations, although its dominance has diminished in recent years.
- Dataquest is a U.S.-headquartered corporation.

Dataquest tracks data in five regions and deals with regional currencies and currency conversion issues in all regions. The currencies involved are the Austrian schilling, the Belgian franc, the Chinese renminbi, the Danish krone, the Dutch guilder, the Finnish markka, the French franc, the German mark, the Greek drachma, the Hong Kong dollar, the India rupee, the Irish punt, the Italian lira, the Luxembourg franc, the Malaysia ringgit, the Norwegian krone, the Portuguese escudo, the Singapore dollar, the Spanish peseta, the Swedish krona, the Swiss franc, the Thailand baht, the NT dollar, the U.K. pound, the European Currency Unit (ECU), the Japanese yen, and the Korean won. Dataquest deals only in a U.S. dollar base for the North American and Rest of World markets for the following reasons:

- North America: Typically, the Canadian portion of the North American market is quite small (10 percent or less), and the relative values of the U.S. and Canadian dollars do not fluctuate widely.
- Rest of World: This region is made up of hundreds of separate countries, each with its own currency, and accounts for less than 1 percent of most high-technology markets.

Method

Data Collection

Data for Japanese, Asian, and European companies is usually collected in the local currency of the companies being tracked. For example, Dataquest collects Japanese companies' revenue in Japanese yen. If a company wishes to report data in U.S. dollars, we request that it use the most recent year-to-date currency exchange rate supplied by Dataquest.

Average Currency Exchange Rates

Once the data is collected, Dataquest uses the average currency exchange rate for the period of time of interest and converts the foreign currency into U.S. dollars. The average exchange rate for a quarter is calculated by summing the values for the three months of the quarter and dividing the

sum by three. Similarly, the average exchange rate for a year is calculated by summing the values for the 12 months of the year and dividing the sum by 12.

The exchange rate used is determined by the precise period of time being evaluated. Most of our historical market sizing and market share data is evaluated in calendar-year or calendar-quarter time periods. However, in evaluating the fiscal-year or fiscal-quarter performance of an individual company, the exchange rate must be calculated for the specific fiscal period under review. For example, NEC Corporation's fiscal year ends March 31. Therefore, when evaluating NEC's financial performance in U.S. dollars, the proper exchange rate would be the average yen per dollar exchange rate for the 12 months beginning April 1 of the previous year and ending March 31 of the current year.

Currency Conversion: Unweighted Exchange Rates

Handling historical data reported in foreign currencies is relatively straightforward when unweighted exchange rates are used. Dataquest maintains a database of average monthly exchange rates for the currencies of major European and Asian countries. These exchange rates are compiled by Dun & Bradstreet.

Conversion of U.S. Dollar to Currency Unit

The formula for converting U.S. dollars to other currencies is as follows:

(U.S. Dollar Value) × (Currency Unit per U.S. Dollar Exchange Rate) = Currency Unit Value

Example:

If U.S.$1 = £0.65, then

$30,000 = £19,500

The formula used is: $30,000 × £0.65/$ = £19,500.

Conversion of Currency Unit to U.S. Dollar

The formula for converting other currencies to U.S. dollars is as follows:

(Currency Unit Value) / (Currency Unit per U.S. Dollar Exchange Rate) = U.S. Dollar Value

Example:

If £0.65 = U.S.$1, then

£20,000 = $30,769

The formula used is: £20,000 / £0.65/$ = $30,769.

Exchange rates can be expressed in either of two ways: Currency Unit per U.S. Dollar, or U.S. Dollar per Currency Unit. The two are reciprocals of each other. Traditionally, the former is preferred for ease of use, as shown in the following example:

Currency Unit per U.S. Dollar: One U.S. dollar equals 134.68 Japanese yen.

U.S. Dollar per Currency Unit: One Japanese yen equals .00743026 U.S. dollars.

Currency Conversion: Weighted Exchange Rates

In certain circumstances, it is desirable to weight exchange rates according to the chronological pattern of consumption in a market over a period of time, or according to the relative importance of various regional markets (a "basket of currencies").

Weighting According to a Chronological Pattern of Consumption

Dataquest tracks consumption in certain markets on a calendar-quarter basis. Each quarter the European and Japanese currencies are valued differently against the U.S. dollar. Simply summing the values of the four quarters and dividing by four would yield an arithmetic mean annual exchange rate; however, this exchange rate would not be the true, effective exchange rate for the year for that market. The example outlined in Table A-1 shows why.

Table A-1
Example of an Arithmetic Mean Annual Exchange Rate

	Q1	Q2	Q3	Q4	Year
U.S.$ Size of Market	100	150	200	250	700
Japanese Yen Size of Market	16,270	23,145	26,420	27,625	93,460
Exchange Rate (Yen per U.S.$)	162.7	154.3	132.1	110.5	
Weighted Average Exchange Rate					133.5
Arithmetic Mean					139.9

Source: Dataquest (August 1992)

In the example presented in Table A-1, the arithmetic mean is higher than the weighted average. The weighted average is calculated by the following formula:

93,460/700 = 133.5

The arithmetic mean is calculated by the following formula:

(162.7+154.3+132.1+110.5)/4 = 139.9

When more than one market is tracked, and when a weighted average exchange rate is used, every market will have a different effective exchange rate because the pattern of consumption over four quarters will not be identical for every market.

Weighting According to a Basket of Currencies

The European Community (EC) has a ready-made basket of currencies, known as the ECU. The ECU, which was established in March 1979, is a basket of currencies composed of specific amounts of the currencies of the member countries of the EC (excluding Greece prior to September 1984

and including Greece thereafter). Each currency's share in the ECU basket is weighted broadly in line with the respective country's GNP and foreign trade.

Forecasting

Dataquest does not forecast exchange rates per se; however, we do forecast IT markets in several regions of the world, and we use the U.S. dollar as a common currency for intermarket comparisons and aggregation. In the forecast period, Dataquest assumes that the actual exchange rate of the full month prior to the month in which the forecast-input assumptions are set will apply throughout all future months of the forecast interval. For example, if a new forecast iteration begins, and forecast assumptions are set in the month of August of the current year, the following exchange rate assumptions are made:

- Actual monthly exchange rates are used for all months in the historical interval up through July of the current year.
- The July (current year) exchange rate is assumed to hold for all months in the August through December (current year) period, and throughout all future years.

Quarterly or annual exchange rates (over either the historical or forecast interval) are calculated as the simple arithmetic mean of the appropriate 3 or 12 monthly rates, respectively.

Appendix B
Worldwide Geographic Region Definitions

North America

Includes Canada, Mexico, and the United States (50 states).

Japan

Japan is the only single-country region.

Europe

Western Europe

Includes Austria, Belgium, Denmark, Eire (Ireland), Finland, France, Germany (including former East Germany), Greece, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, the United Kingdom, and the rest of western Europe (Andorra, Cyprus, Gibraltar, Liechtenstein, Monaco, San Marino, Vatican City, Iceland, Malta, and Turkey).

Eastern Europe

Includes Albania, Bulgaria, the Czech Republic and Slovakia, Estonia, Hungary, Latvia, Lithuania, Poland, Romania, the republics of the former Yugoslavia, and the republics of the former USSR (Belorussia, Russian Federation, Ukraine, Georgia, Moldova, Armenia, Azerbaijan, Kazakhstan, Uzbekistan, Tajikistan, Kirgystan, and Turkmenistan).

Asia/Pacific

Includes Asia/Pacific's newly industrialized economies (NIEs) and the rest of the Asia/Pacific regions. NIEs include Hong Kong, Singapore, Korea, and Taiwan. The rest of the Asia/Pacific regions includes Australia, Bangladesh, Brunei, Cambodia, China, India, Indonesia, Laos, Malaysia, Maldives, Myanmar, Nepal, New Zealand, Pakistan, the Philippines, Sri Lanka, Thailand, and Vietnam.

Rest of World

Includes Africa, the Caribbean, Central America, the Middle East, Oceania, and South America.

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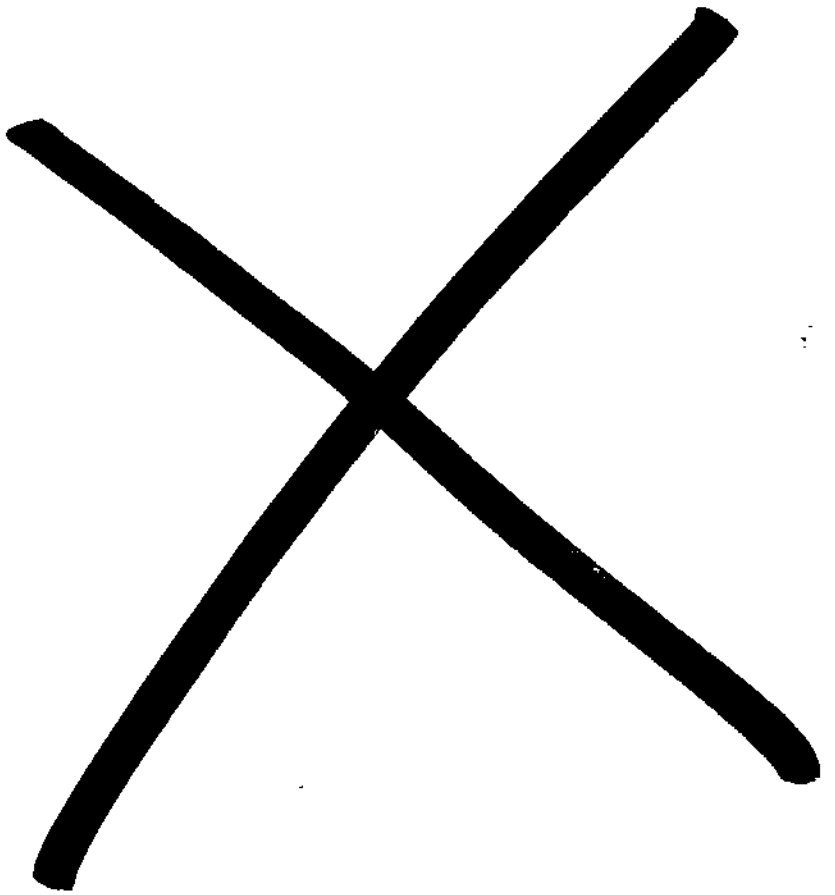

Dataquest

Competitive Dynamics

ASICs Worldwide

Product Analysis

System Dissection: ASICs Continue to Differentiate Systems

Abstract: *Dataquest continues to investigate the inner workings of numerous systems, ranging from workstations and PCs through game machines and cellular phones. Time and time again, the silicon is the system or at least plays a critical role in delivering the functionality required in the competitive marketplace. This newsletter takes a look at some of the technology trends found in the systems dissected by Dataquest's PC Teardown group. By Duane Kuroda*

ASICs Play Key Role in Successful Designs

ASICs continue to make the news, with stories about multimillion-gate designs using a 0.35-micron process recently splashed across the press. Press releases are frequently filled with news of deep-submicron designs, with usable gate counts easily over 100,000 gates, sometimes stretching into the 600,000-gate realm. With all these grand design advances, where is the ASIC production today? Reports from Dataquest in Japan and around the world suggest that 1-micron and greater process geometries are still being used as production vehicles for a number of high-volume designs. While submicron-geometry designs have been discussed for a while, they can easily require a year to 18 months to reach any reasonable volume, and the systems torn down today may still include some chips fabricated on older processes.

By tearing apart those systems that have reached volume production and are still on the market, Dataquest can analyze those that were successful. Dataquest ripped apart more than 20 systems this year to examine system as well as ASIC content, to double-check our end-user research, and to better understand the current configurations of successful systems. The

Dataquest

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systems discussed in this newsletter were torn down and analyzed by Dataquest analysts in 1995 and represent only a sample of the systems available in 1995. As more systems are brought under the microscope, Dataquest will examine the changes or shifts in technology use.

Systems Analyzed

Dataquest's teardown analysts dissected numerous systems and created individual reports about their findings (available through the PC Teardown service). These reports include a bottom-up manufacturing cost estimate, descriptions of the constituent subsystems, and the analyst's perspective. The findings in this article are based on the following systems:

- Notebook/subnotebook
  - Digital HiNote
  - Toshiba Satellite Pro T2150CDT
  - HP Omnibook
- Servers
  - Compaq Prosignia 500
  - ALR Revolution Q-SMP Pentium 90
  - Proliant 4000
- Workstations
  - HP 712/60
  - Motorola PowerStack DT603-66NTW
- Game units
  - Sony Playstation
  - Sega Saturn
- Desktop
  - Acer Acros
  - Compaq Presario 954 CDS
  - Apple Performa
  - IBM Aptiva 330
  - AST Bravo MS P/90
  - Dell Pentium 90
  - Digital Pentium 90
  - HP Vectra XM 4/100i
  - HP Vectra VE
  - IBM PC 750
  - Packard Bell Legend 417CDT

- Palmtop
  - Motorola Marco
  - Sharp Zaurus
  - Sony Magic Link
- Others
  - Orion chipset
  - Cellular phones

ASIC Technology Trends

The evolution of ASIC design can be generally described in terms of movement up and to the right for the ever-popular gate count and pin count discussions. However, that generalization ignores the nuances and dynamics of the ASIC market. By taking a closer look at metalization, line widths, pin counts, and packages, reality can be separated from hype and a deeper understanding realized.

Teardown analysts found 76 ASICs in the 1995 systems. Of those ASICs, CMOS designs were 36 percent digital cell-based designs, 52 percent digital gate array designs, and nearly 5 percent mixed-signal CMOS. The remaining sockets were captured by BiCMOS and bipolar designs (7 percent). Gate counts ran across the board, from under 5,000 gates to more than 220,000 gates. Some bipolar and BiCMOS parts were clearly designed in for their high drive capability.

A note of caution is in order at this point. The ASICs from these systems represent a finite sample of the data-processing segment of the ASIC market. This information covers only those systems torn down, and no claim is made that this sample represents the entire data-processing market or entire ASIC market.

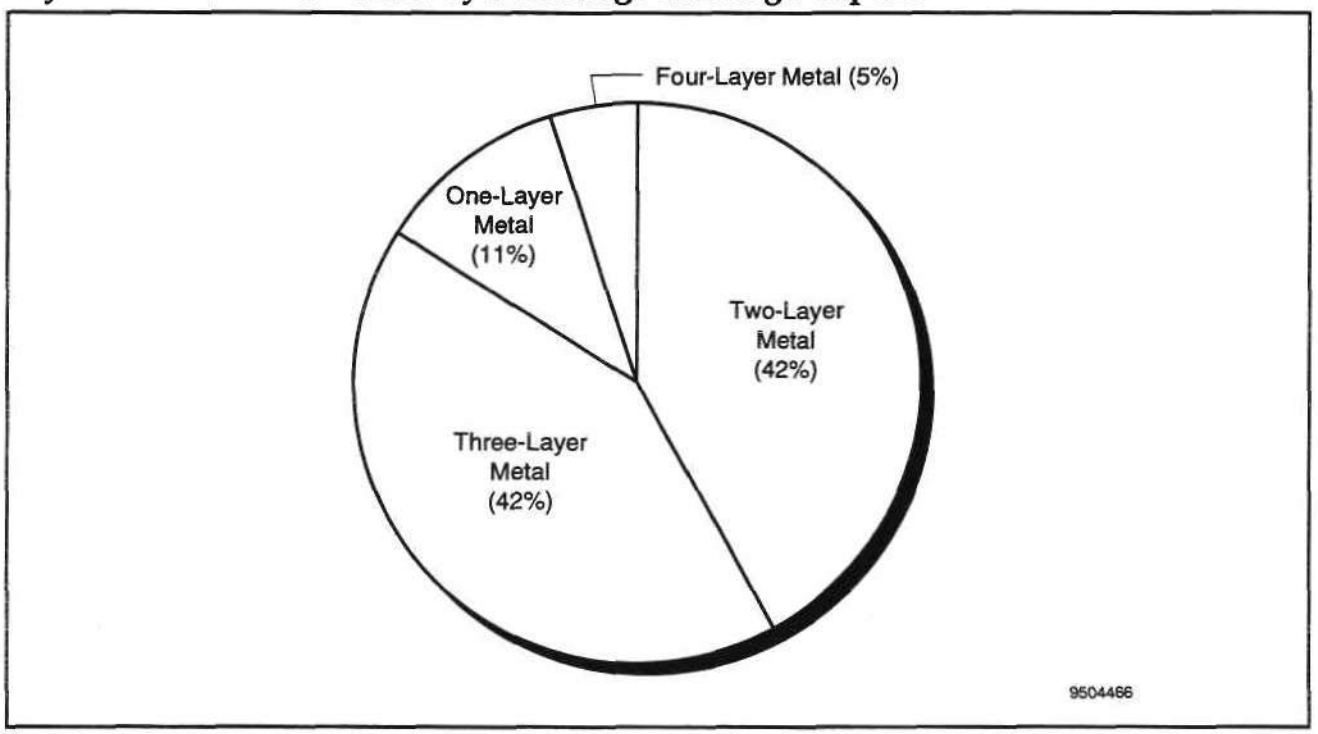
1LM, 2LM, 3LM or More?

The systems torn down in 1995 to date provide a valuable look at the shifting direction of metal layer usage. The industry is at a crossroads, where tried-and-proven two-layer metal is increasingly giving way to three-layer metal designs. Figure 1 shows that, for the systems torn down in 1995, the number of ASICs using three-layer metal equaled the number using two-layer metal. This appears to be slightly optimistic, but could be expected because of the performance requirements of the data-processing market. However, three-layer metal, popularized and often hyped in marketing material, is generally closing the gap with two-layer metal. A major contributing factor is that processing technology and yields have improved to the point where three-, four-, and five-layer metal are not only possible, but have already been implemented. Four-layer metal design was found on a few chips, but the added costs to the wafer will prohibit widespread use for some time.

More than Submicron Fabrication

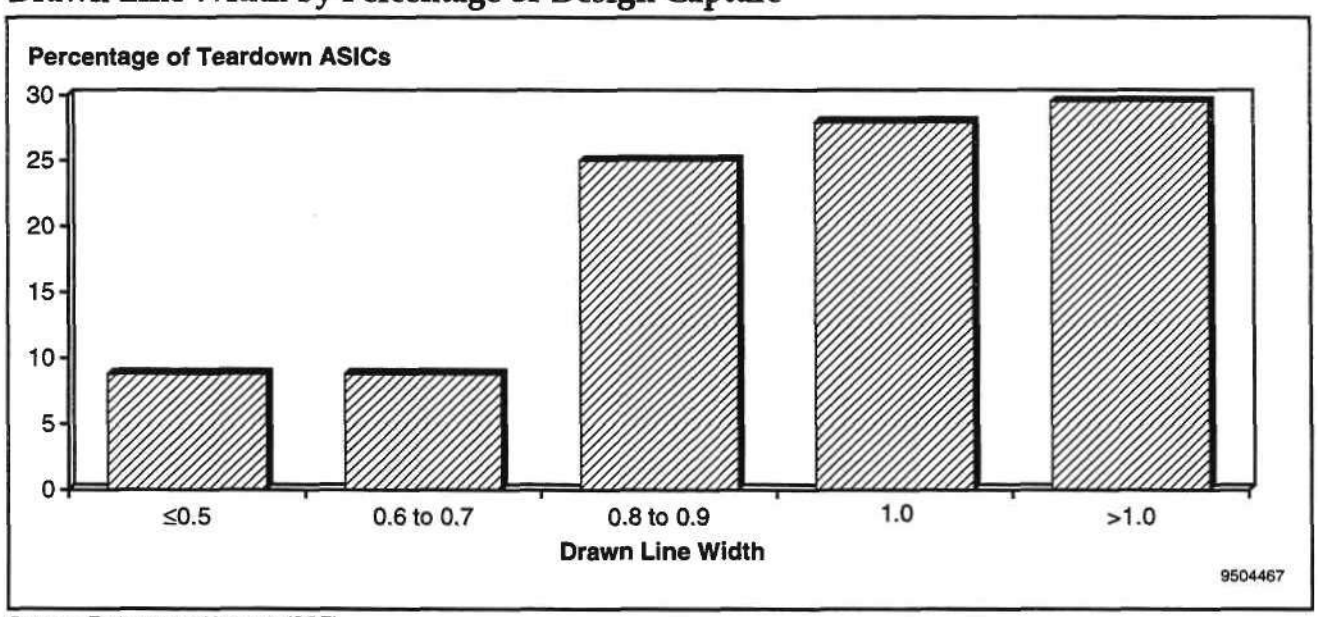
Another item in contrast to the design-start activity is the process geometries of ASICs in production. The suppliers for these systems appear to be cranking out less than 20 percent of their production for designs at 0.7 microns and below (see Figure 2). This contrasts with Dataquest's expectation that over 70 percent of design starts in 1996 will occur in those

Figure 1
Layers of Metal Interconnect by Percentage of Design Capture



Source: Dataquest (August 1995)

Figure 2
Drawn Line Width by Percentage of Design Capture



Source: Dataquest (August 1995)

geometries. The design activity in submicron families typically takes a year to 18 months to reach full production, and that swing should occur as planned. As expected, the use of 0.8 and 0.9 designs fared well as production vehicles; at the same time, excess capacity at 1 micron and larger has been utilized to exhaust that declining technology.

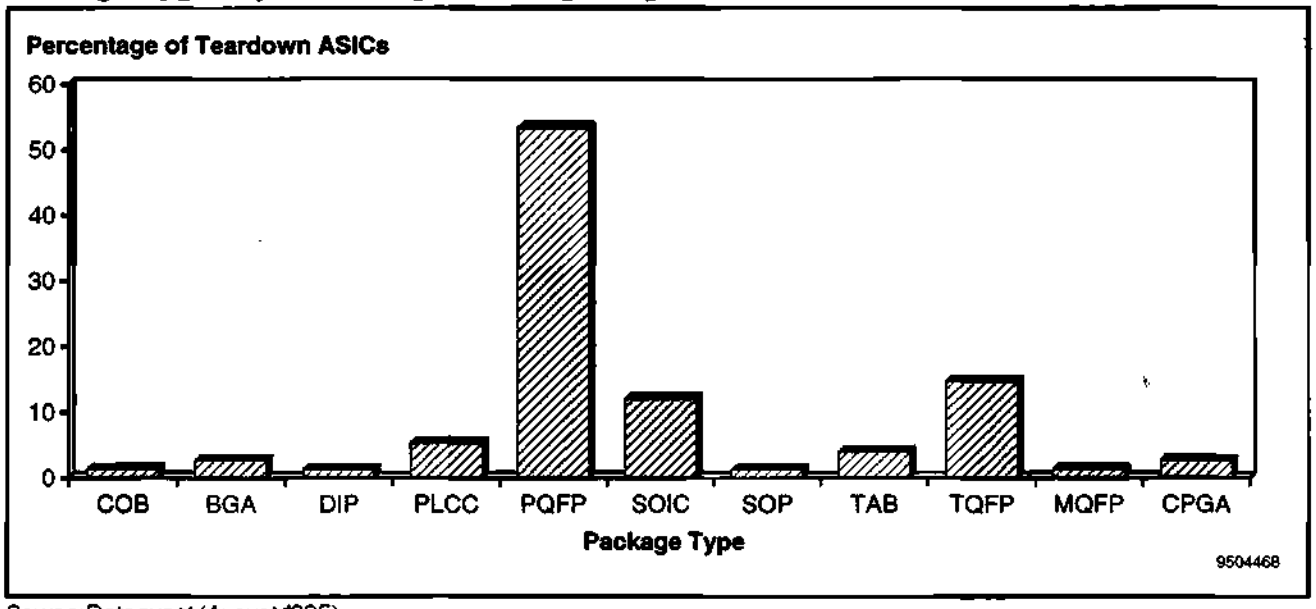
Package a Winner

Dataquest collected and processed data describing the packages used in successful designs. QFPs clearly were the package of choice, capturing easily over 75 percent of the sockets. For systems designed so long ago, BGA usage was respectable, winning about 3 percent of sockets. Design activity in BGA has been growing rapidly, and Dataquest has predicted ("ASICs Fuel BGA Growth," July 31, 1995, ASIC-WW-PA-9502) that BGAs will reach 35 percent of design starts in 1999. Figure 3 shows the percentage of designs in each package type for the torn-down systems. These figures represent actual ASICs from the torn-down systems and should not be confused with design starts, which typically take a year to 18 months to reach production.

Down for the Pin Count

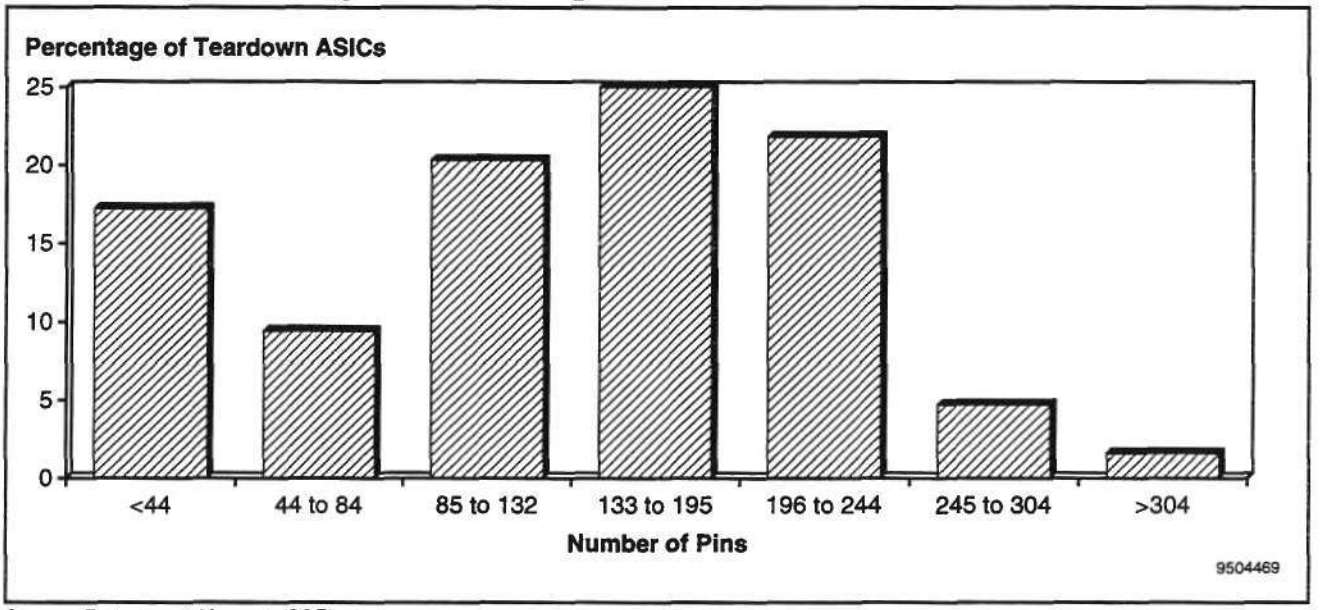
Pin counts were also analyzed for the torn-down systems. The most popular pin count fell at 208, with another strong showing at 100, followed by 160. Figure 4 shows the relative number of ASICs in each pin-count range for the analyzed systems. The pin-count distribution suggests that these ASICs were not significantly affected by the need for 64-bit data and address buses, however, the ASICs with more than 195 pins still formed a significant portion of the systems. The number of low-pin ASICs was influenced by the palmtop and mobile systems in the sample.

Figure 3
Package Types by Percentage of Design Capture



Source: Dataquest (August 1995)

Figure 4
Pin Count by Percentage of Design Capture



Source: Dataquest (August 1995)

ASIC Snapshot of Socket Wins

The leading ASIC suppliers and system vendors need to know who is winning the most data processing sockets. The top six socket winners were (in alphabetical order):

- LSI Logic
- Motorola
- NEC
- SGS-Thomson
- Texas Instruments
- Toshiba

North American suppliers accounted for half of the sockets, Japanese suppliers covered a third, and a European supplier rounded out the group.

Dataquest Perspective

Feature sets continue to be a major factor in the system selection process. To understand the role of custom and semicustom ASIC in these systems, Dataquest tore apart and analyzed the system ASIC content. We took a close look at some leading-edge systems and found that ASICs played an important role for many system OEMs by differentiating their products. The use of ASICs varied widely, but one trend was evident: The more commodity-like the system, the fewer ASICs involved. Teardowns revealed that low-end PCs used more standard chipsets, while high-end, value-added PCs, servers, and workstations incorporated many more ASICs. Also, fierce feature wars in the palmtop, cellular, and game console markets, all targeted at consumer segments, have resulted in significant ASIC usage in those areas.

This trend suggests that ASIC suppliers that want their products to stand out need to provide valued-added products. Similarly, in order to target higher-margin solutions in the data-processing arena, ASIC suppliers need to develop a strategy to attack the workstation, server, and leading-edge PC markets. By establishing strong relationships, ASIC suppliers can develop and maintain targeted cell libraries that enable them to capture early ASIC designs and develop generic chipsets, if they so desire. At the same time, these alliances or partnerships not only provide a foot in the door for the next design-win, but also place the supplier in a premium position for developing higher gate-count parts as well as the required enabling packages.

Although many system manufacturers are trying to reduce the number of ASIC suppliers, this analysis showed that no ASIC suppliers met every need. The sheer number of ASIC vendors per system indicated that no single ASIC vendor had sufficient expertise to provide functionality across each subsystem. There are two main reasons for this trend. One is risk management, because single-sourced ASICs would expose the system OEM to too much risk of dependence on capacity and reduced negotiating power. The other reason is economics, because the expertise required to provide every optimized cell would cost the ASIC supplier too much in terms of resources and capital. Also, ASIC suppliers have been choosing differentiation strategies, with some refusing low gate-count or nonstrategic business, while others are subcontracting out price-sensitive and low value-added ASICs to other suppliers. So while chip counts and the number of ASIC suppliers are going down, opposing forces in the near term will continue the trend of multiple ASIC suppliers per board.

This article has provided information about some trends found in the systems dissected by Dataquest's teardown analysts. It provides a single snapshot of products selling in 1995. As more systems are brought in and dissected through 1995, Dataquest will continue to track the ASIC changes and illuminate the product trends.

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Competitive Dynamics

ASICs Worldwide

Product Analysis

Packaging Update: ASICs Fuel BGA Growth

Abstract: *Ball-grid array (BGA) packages are well on their way to being the greatest package since the plastic quad flat pack (PQFP), and ASICs are playing a vital role in the future development of this package. In this newsletter, Dataquest examines results of a BGA packaging survey, looks at the market status of ASIC packaging, and provides a five-year ASIC package and pin-count forecast. Advantages and disadvantages of the BGA package are also explored to determine the future success of this exciting package.*
By Bryan Lewis and Mary Olsson

BGA Developments

Ball-grid array packages (BGAs) are being touted as the greatest IC package since the plastic quad flat pack (PQFP). It comes as no great surprise that ASICs are leading the charge in these high-pin-count packages. Maximum ASIC gate counts are now exceeding 1 million usable gates as suppliers stride for system-level integration (SLI) or system-on-a-chip. These high-density designs pose the greatest challenge to system and packaging designers. Packaging suppliers, ASIC suppliers, and system suppliers are focusing and investing in BGA packages as the package type for future high-density design.

To pinpoint new developments in BGA package use, Dataquest recently conducted a survey to determine direction and use of various BGA package styles. The majority of package suppliers and users stated that the emerging BGA packages would displace the traditional ceramic and plastic pin grid array (PGA) packages, all types of quad flat packs (metal, ceramic, plastic) beyond 300 pins, and quite possibly tape-automated bonding (TAB) directly on the printed circuit board.

Dataquest

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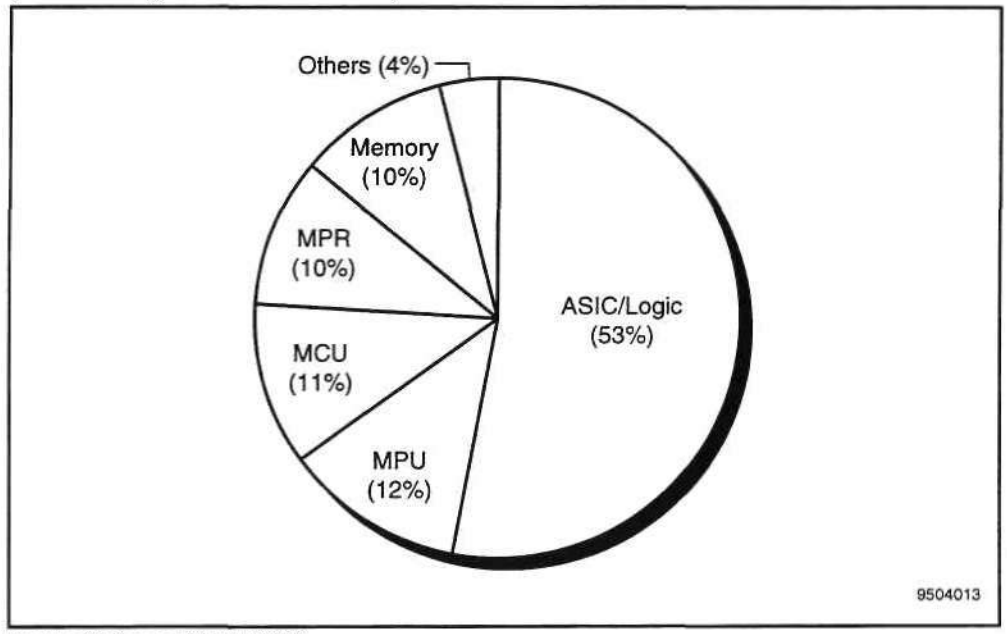
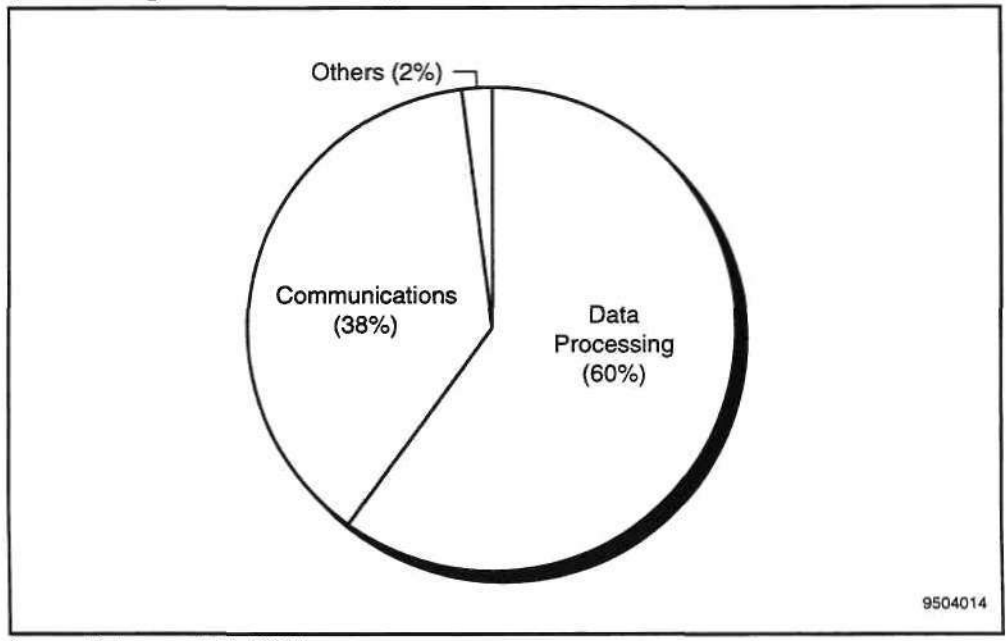
Furthermore, the survey showed that ASICs dominated 1994 BGA production (see Figure 1). Data processing and communications applications have had the largest use of BGAs to date, as shown in Figure 2. The vast majority of BGA use for all products had been in the 196-to-244-pin range (see Figure 3), whereas ASIC BGA use is primarily in the 225-to-475-pin range.

Figure 1
Estimated 1994 BGA Production by IC Product (Percentage of Production)



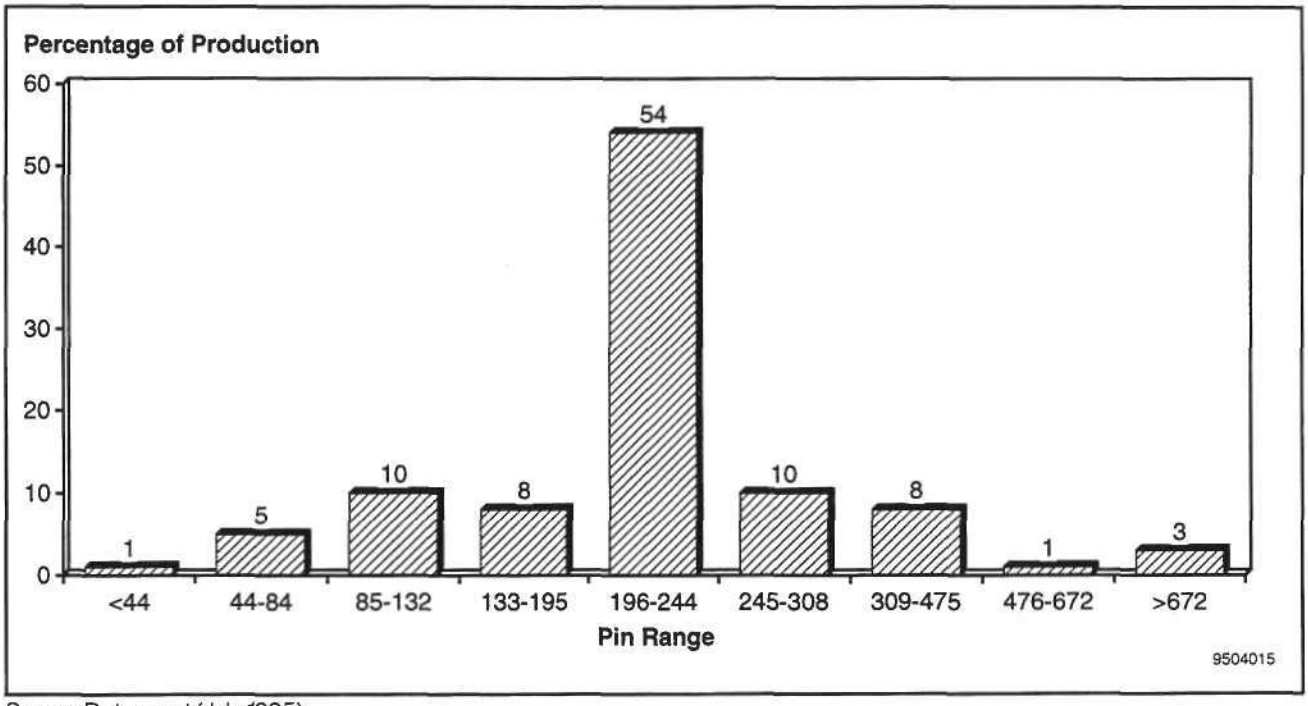
Source: Dataquest (July 1995)

Figure 2
Estimated 1994 Total BGA Production by Application Market (Percentage of Production)



Source: Dataquest (July 1995)

Figure 3
Estimated 1994 Total BGA Production by Pin Count



Source: Dataquest (July 1995)

The majority of BGA volume shipped in 1994 for all IC products was in the single-core plastic BGAs (PBGAs), often referred to as the OMPAC style, a Motorola acronym (see Table 1). As the lead pitch of QFPs drops to less than 0.5mm and 0.4mm, the cost efficiencies of QFPs decrease and the manufacturing process yields diminish. BGAs have the advantage of having higher pin counts and a more relaxed lead pitch than QFPs (see Table 2).

ASIC Packaging

ASICs are in a unique position because of the wide product offering and the diverse set of applications they serve. ASIC products range from simple PLDs with 50 gates to embedded gate arrays and cell-based ICs (CBICs) with over 1 million usable gates. ASIC applications range from cost-driven consumer products such as camcorders where size is the issue, to supercomputers where speed is critical, to automobiles where heat is a factor.

Table 1
Estimated 1994 BGA Production by Product Type

BGA Product	Percentage of Production
Plastic BGA (Single Core)	87
Plastic BGA (Peripheral Array)	10
Enhanced PBGA (Multilayer)	0
µBGA (Tessera Compliant Chip, or TCC)	1
Ceramic BGA	1
Ceramic Column Grid Array (CGA)	0
Tape BGA	1

Source: Dataquest (July 1995)

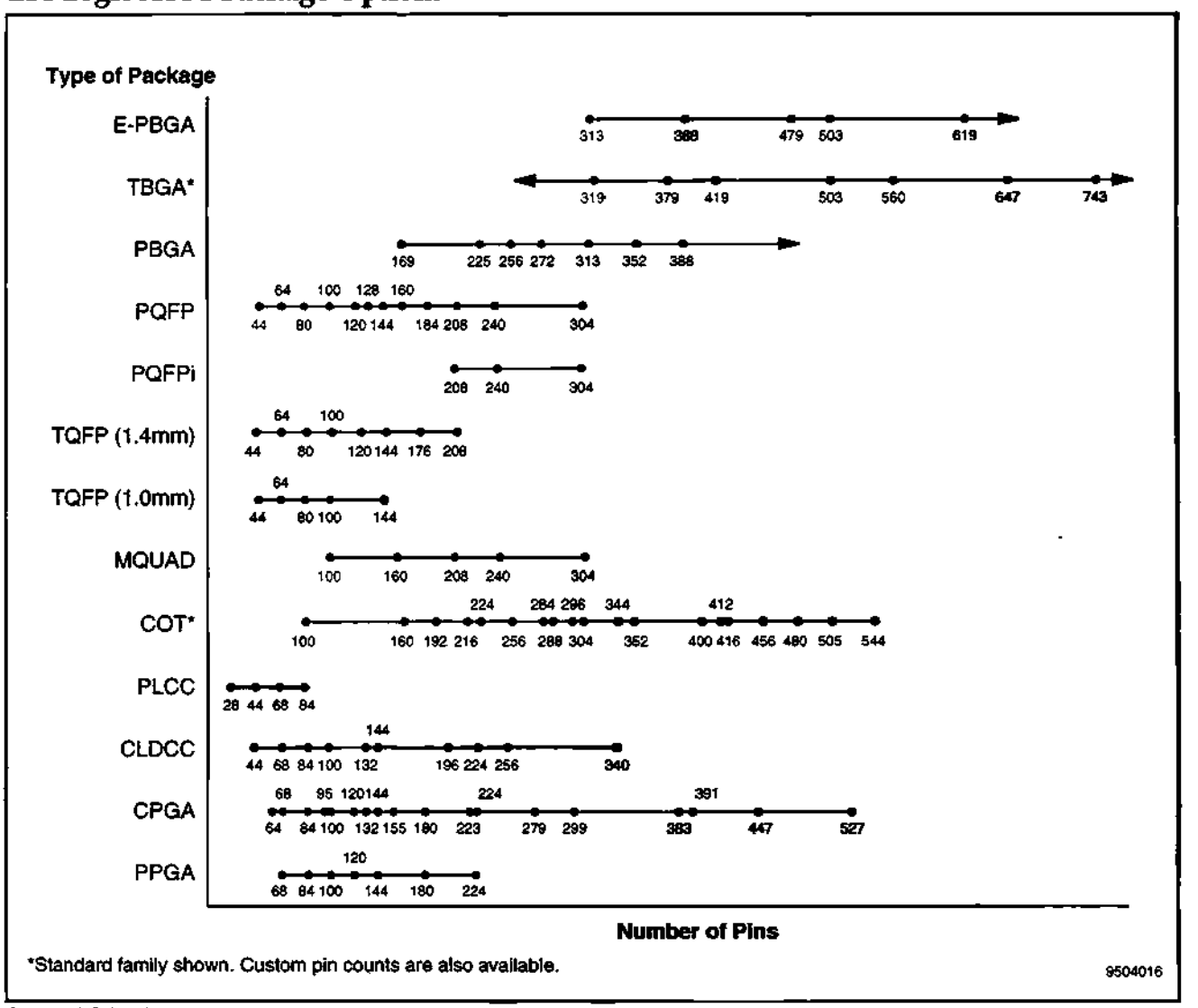
Table 2
Estimated 1994 BGA Production by Lead Pitch

Lead Pitch	Percentage of Production
0.060 Inches	55
0.050 Inches (1.27mm)	14
0.040 Inches (1.00mm)	12
0.020 Inches (0.5mm)	19
0.010 Inches (0.25mm)*	0

*Pitch of direct die mount via flip chip (0.25mm) and TAB (pitch varies from 0.16mm to 0.30mm)
Source: Dataquest (July 1995)

Because ASIC products and applications are unique, successful ASIC suppliers must offer a wide variety of packaging options. LSI Logic, the largest merchant ASIC supplier in the world, has a very extensive packaging offering (see Figure 4).

Figure 4
LSI Logic ASIC Package Options



Source: LSI Logic

Market Status

Our end-user ASIC research of 700 system designs indicates that the average ASIC user started with PLCC for low gate count devices, moved to PQFP for medium to high gate counts, and is now examining BGAs for higher gate count devices. PQFPs are the dominant package type in North America; however, BGAs are gaining acceptance primarily in the data processing and communications markets (see Figure 5).

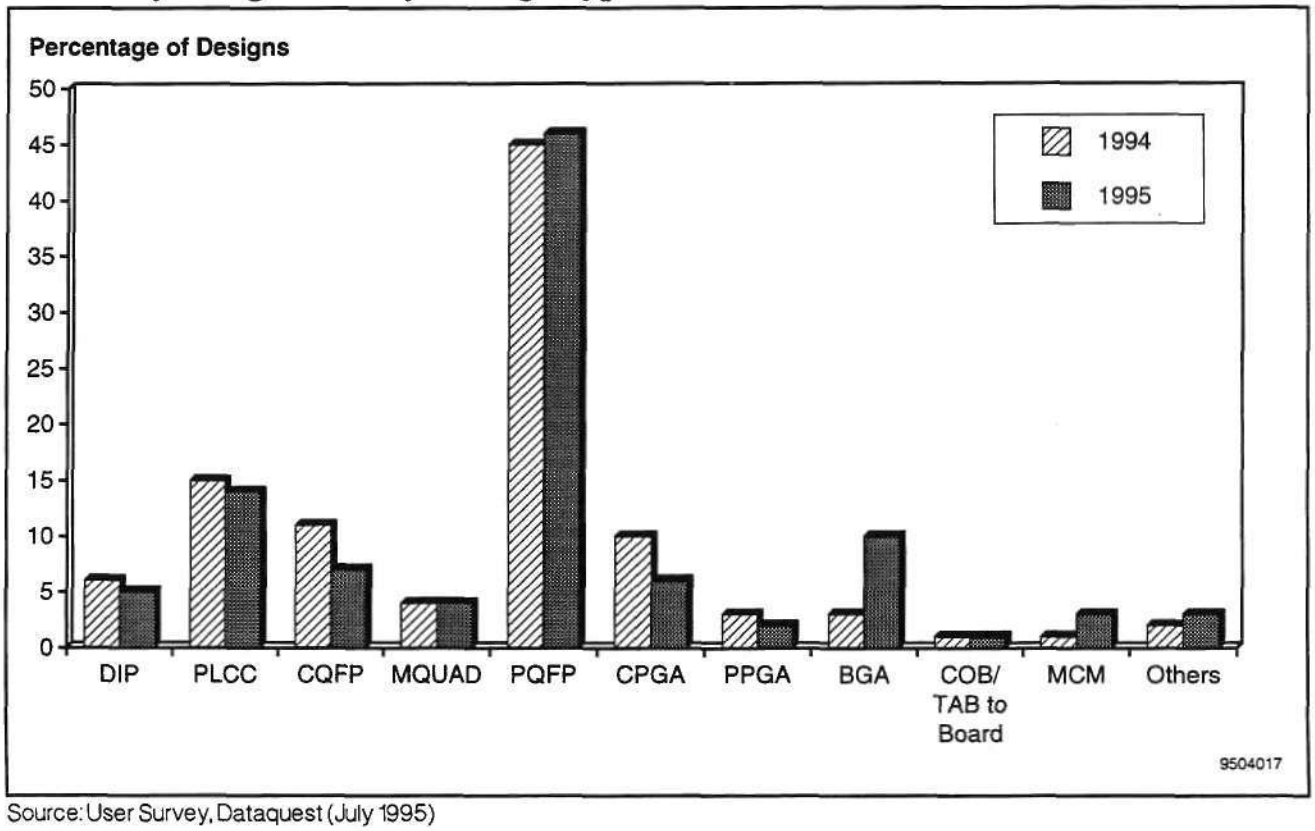
As gate counts rise, system designers cry out for more pins. While many suppliers are now offering packages with more than 500 pins, the vast majority of gate-array design starts have fewer than 304 pins (see Figure 6).

Future ASIC Packages

Dataquest believes that PQFPs (including the TQFP) will be the dominant package technology for the next five years. We foresee a continued decline in the use of low-pin-count packages such as DIPs and PLCCs and to some extent the PQFP because the system market is migrating to high-gate count ASICs. We are in a wait-and-see mode for multichip modules (MCM) packages because the market has progressed much slower than expected. Most important, Dataquest expects to see a sharp rise in BGA packages, as shown in Figure 7.

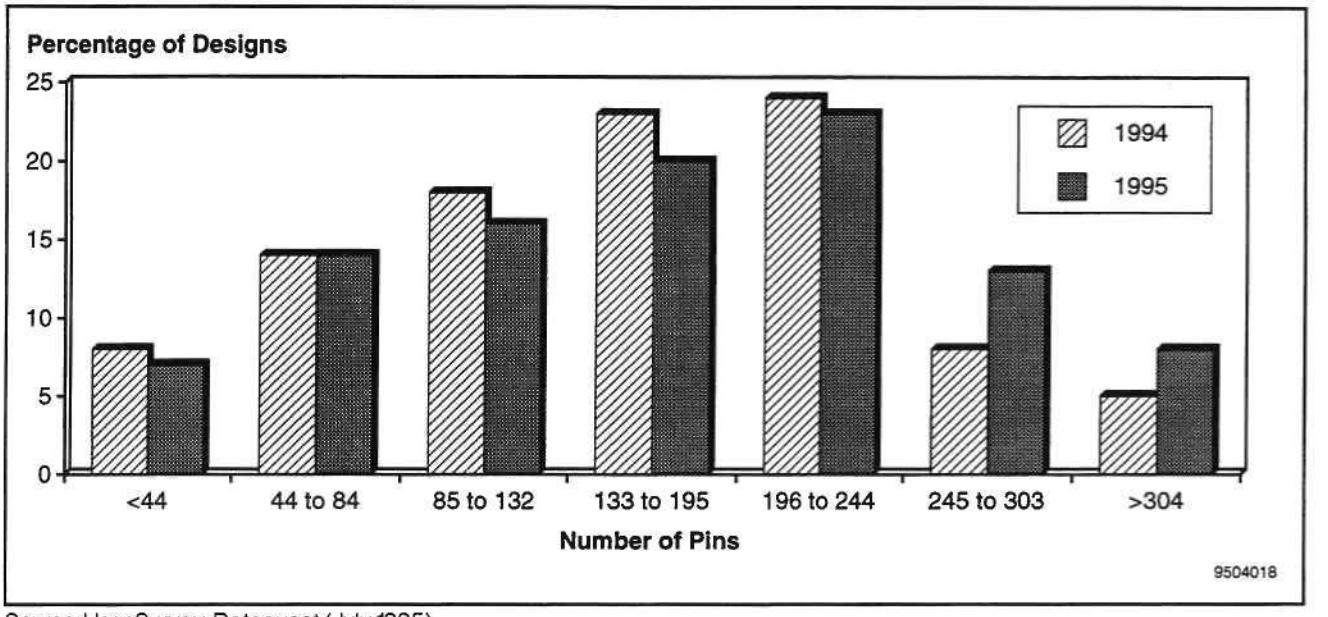
High-pin-count packages are clearly the wave of the future. Dataquest believes that in excess of 56 percent of 1999 North American gate array design starts will be in packages with greater than 245 pins (see Figure 8). Exponential growth in pin counts will fuel growth in BGA packages.

Figure 5
Gate Array Design Starts by Package Type: North America



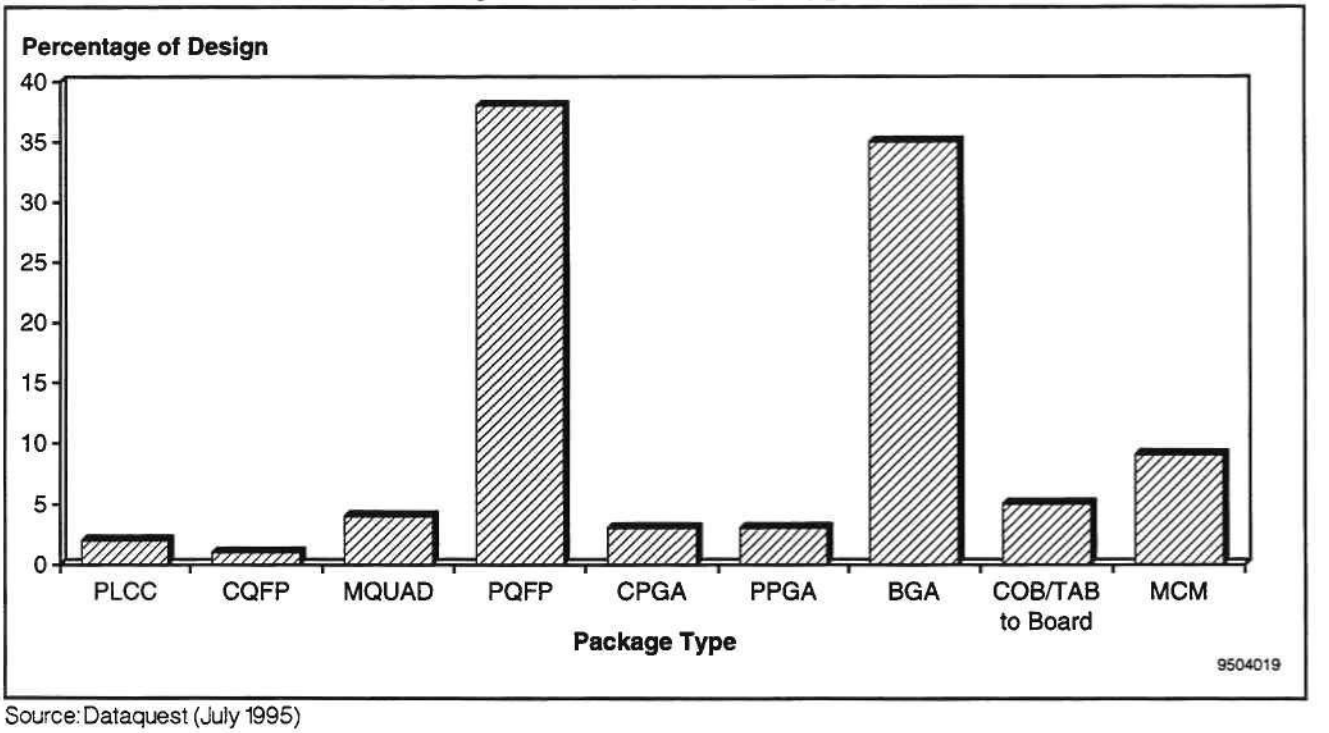
Source: User Survey, Dataquest (July 1995)

Figure 6
Gate Array Design Starts by Pin Count: North America



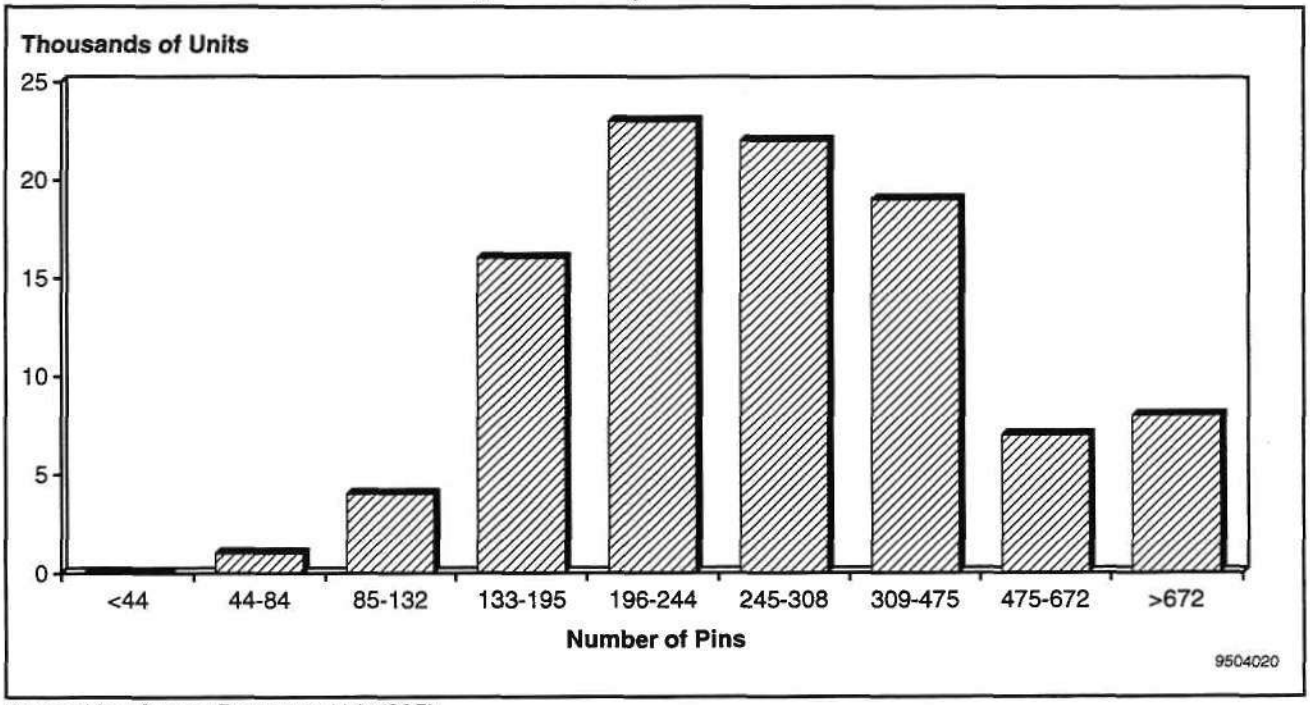
Source: User Survey, Dataquest (July 1995)

Figure 7
Estimated 1999 Gate Array Design Starts by Package Type: North America



Source: Dataquest (July 1995)

Figure 8
Estimated 1999 Gate Array Design Starts by Pin Count: North America



Source: User Survey, Dataquest (July 1995)

Dataquest Perspective

ASIC suppliers and users have been wrestling with the decision of which package option will be the best long-term solution for their high-density/high-pin-count ASICs. Large ASIC users including Apple, Compaq, IBM, and Sun believe that BGAs are just the ASIC package they have been looking for.

There are many considerations to take into account when choosing a high-end ASIC package. Although we will not go into detail on all the packaging issues, some highlights of the BGA package compared to the PQFP are as follows:

- Reduced size
  - Smaller footprint
  - Low profile and low weight
  - PC board savings
- Improved manufacturability
  - Relaxed lead pitch
  - Eliminates concerns over lead coplanarity and skew
  - Vastly improved board manufacturing yields
  - Lower manufacturing cost leveraged by high assembly yields
  - Repairable using hot air flow for removal and resoldering

- Improved electrical and thermal performance
  - Improved electrical performance with lower inductance
  - Comparable or better thermal performance

While the advantages are many, the primary disadvantages have been the limited number of suppliers and the increased package cost. In terms of the former, Dataquest is aware of many third-party BGA packaging suppliers, including Amkor/Anam, ASAT, Citizen, IBM, iPAC, Kyocera, Motorola, Shinko, Selectron, Swire, and Tessera. Six of these suppliers have a license from Motorola. On the pricing issue, while Dataquest believes that the price per BGA package will not reach the same level as the PQFP because of the increased cost associated with extra steps required to add the solder balls, we have seen and expect to see further cost reductions as volume production increases. Dataquest believes the advantages of BGAs far outweigh the disadvantages.

In conclusion, we believe that BGA packages are well on their way to being the greatest package since the PQFP.

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Dataquest
a company of The Dun & Bradstreet Corporation

Competitive Dynamics

ASICs Worldwide

Product Analysis

HD-PLDs: Where Are We Growing?

Abstract: *The high-density programmable logic market is ripe with opportunity. The combined standard logic and low-density gate array market alone represent a $4 billion opportunity. Buffed-up product lines and improved tools make that opportunity ripe for the taking, if the price is right. Before reaching for that apple, however, vendors need to understand whether the opportunity is stagnant or whether there is more available.*
By Duane Kuroda

HD-PLDs: The Future Looks Bright

Sustained growth of more than 30 percent for the last five years—few chip markets can make this claim, and for that reason the combined markets of CPLDs and FPGAs (collectively called high-density PLDs or HD-PLDs) have garnered tremendous attention. The growth continues undaunted, as opportunities exist in the low-density, low-volume gate array market, the disappearing SPLD market, and the remaining standard logic market. This article looks at current opportunities and at the current state of the industry. The information is based upon results from a confidential supplier survey and a Dataquest User Wants and Needs study.

Current Growth Opportunities

The key current areas of focus for programmable logic are continuing to expand. Standard logic, low-density gate arrays, and SPLDs have been the traditional areas of focus. However, new architectures and development efforts have pushed the application boundaries to include reconfigurable computing, DSPs, and data path computing.

Dataquest

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Standard Logic Waits to Be Enveloped

The standard logic market represents a $3 billion market opportunity. Board space continues to be a premium, and the allocation status of standard logic makes it ripe for consolidation into single silicon. Tools and design flows are a major issue here, as the implementation of programmable logic needs to be incorporated into design flows to avoid the hand-picked, tedious task of standard logic selection. Once tools or processes that easily map standard part libraries into programmable logic devices are developed and reliable, cost-effective comparisons will be made and we will see more market share captured from this segment.

Converting SPLDs to High-Density PLDs

The SPLD market represents more than $400 million in potential growth. The conversion process, where SPLDs are swept up into HD-PLDs, continues to grow the sales of HD-PLDs. Continued cost-cutting has placed low-end CPLDs and FPGAs near price parity of the multiple devices they are meant to replace. Not only are the prices competitive, but also many vendors offer free or low-cost software to convert the SPLDs to other high-density designs. When decreased inventory and reduced handling costs are factored in, conversion away from SPLDs almost becomes a nonissue.

Gate Array Opportunities

The low-end gate array business has been talked about frequently, but rarely quantified. Results from Dataquest's recent ASIC user survey suggest that the available market opportunity for programmable logic in the gate array market is nearly $1 billion. This figure represents those designs shipping at or below 1,000 units in designs of 10,000 gates or fewer. That figure grows when the plethora of architectures offering more than 10,000 gates is considered. Similarly, the introduction of multidevice FPGA partitioning not only will make higher-density designs possible, but also eventually economically feasible.

Other Market Opportunities

The growing popularity of DSP-type functionality in ASICs and on individual chips has transferred to programmable logic. Application notes on FPGAs as FIR filters or even 3-D rendering engines are not uncommon. Other areas for adaptive computing have been developed and proven for systems where FPGAs are the processor. The working devices in many of these areas have been relegated to research or academia, although the architectures have been available for proof-of-concept designs. Before this market takes off, however, there needs to be a re-education of the market about the capabilities of programmable logic to perform DSP, processing, and adaptive functions. Likewise, other facets such as operating system development, hardware-software development, and system vendor buying need to be established for this to amount to more than an interesting sidetrack.

Making Strides toward High Density

The factors previously described clearly indicate an important future role for programmable logic. In this section, Dataquest looks at the current product offerings on the road to increased programmable logic proliferation.

Densities of Shipping Parts

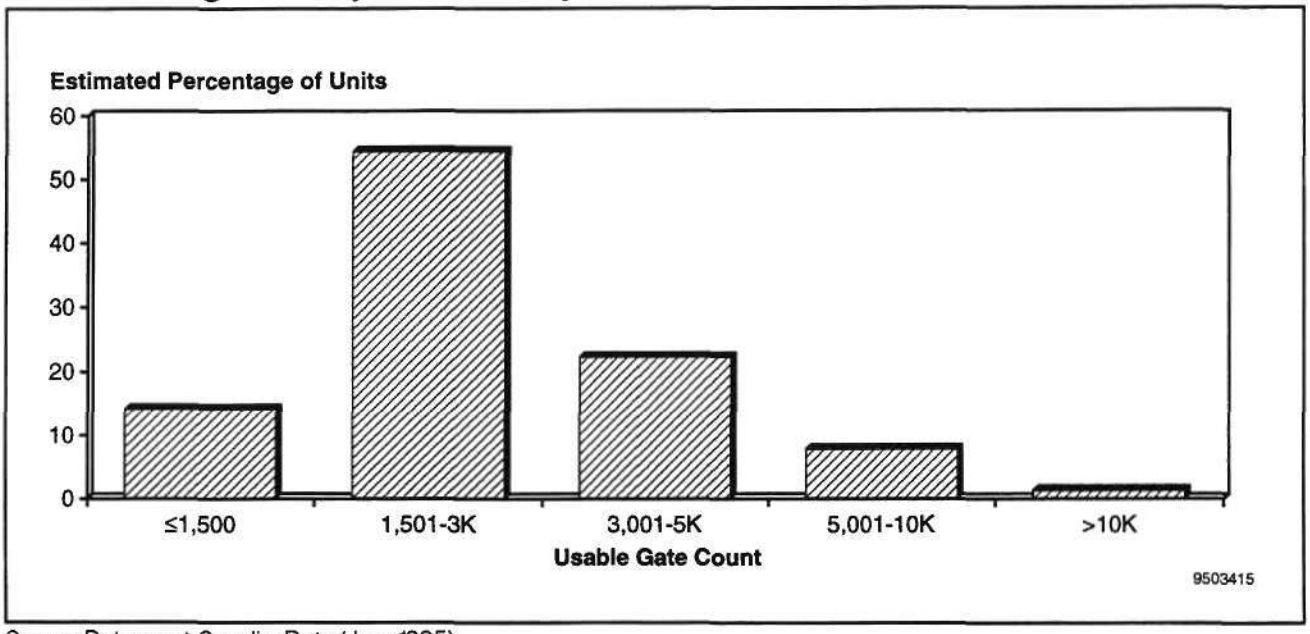
Dataquest predicted that SPLDs would start their decline in 1994, which proved true, contrary to other opinions. SPLDs have started to decline as those designs are migrated to higher-density PLDs. Similarly, current trends indicate many systems are starting to incorporate HD-PLDs as prototyping and production solutions, altogether skipping SPLD use. PLD suppliers reported that, on average, smaller CPLD and FPGA devices of 1,500 to 3,000 gates were the most popular (see Figure 1).

This unit data differed from user projections for programmable logic design starts for 1995. Results from the user survey, found in the 1995 ASIC User Wants and Needs document titled *Systems Designers Uncover ASIC Opportunities* (ASIC-WW-UW-9501, dated June 26, 1995), suggest that designers' confidence is growing and that design activity is increasing in higher-density products. Whether this translates to units will depend on the cost reductions that suppliers pass to the users. If the price perception remains high, programmable logic will remain prototyping and preproduction solutions. If prices continue to drop, we may see higher unit volumes of higher-density parts.

Clock Frequency Trends

Although there is little doubt that the 15ns SPLDs are capturing mainstream designs, the abilities of gate arrays far exceed such capabilities. Consequently there have been questions about HD-PLDs being able to provide the required performance for SPLD conversion as well as low-end gate array design capture. CPLD suppliers reported that their customers definitely have a need for speed (see Figure 2). The most popular devices were those that shipped at 12ns and 15ns, speeds clearly chosen to provide a margin for error in the design process. In fact, nearly 65 percent of the CPLD units are based in the less-than-15ns range.

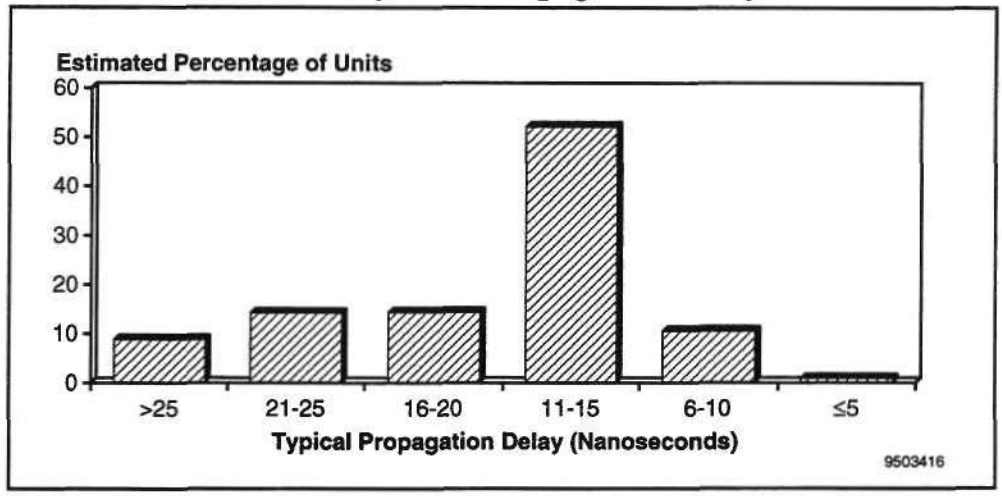
Figure 1
1994 MOS High-Density PLD Units by Usable Gates



Source: Dataquest, Supplier Data (June 1995)

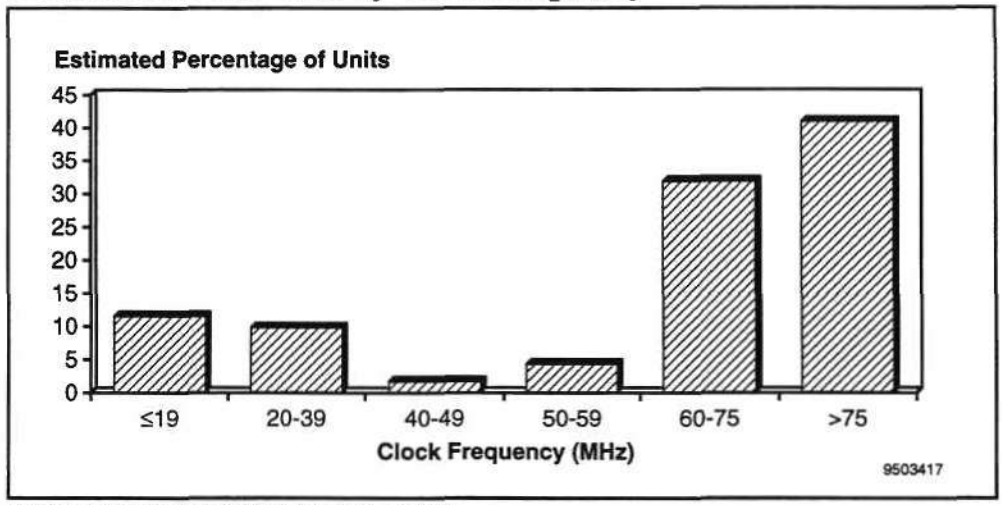
FPGA suppliers, however, reported a bimodal need for speed (see Figure 3). The most popular devices were those that shipped supporting speeds above 75 MHz. Because of the many timing predictability concerns, designers of FPGA also have chosen to provide a margin for error in the design process. In fact, more than 70 percent of the FPGA units were shipped capable of 60-MHz-plus speeds.

Figure 2
1994 MOS CPLD Units by Total Propagation Delay



Source: Dataquest, Supplier Data (June 1995)

Figure 3
1994 MOS FPGA Units by Clock Frequency



Source: Dataquest, Supplier Data (June 1995)

Mainstream ASIC design has not reached the high average speeds provided by many programmable logic vendors. However, the timing predictability problems continue to support perceptions of FPGAs as prototyping or emulation tools. The introduction of timing-driven place-and-route should quell those complaints, as users will be able to actually achieve the clock speeds they desire on their targeted architecture. In the meantime, programmable logic vendors now claim to have devices with speeds easily topping

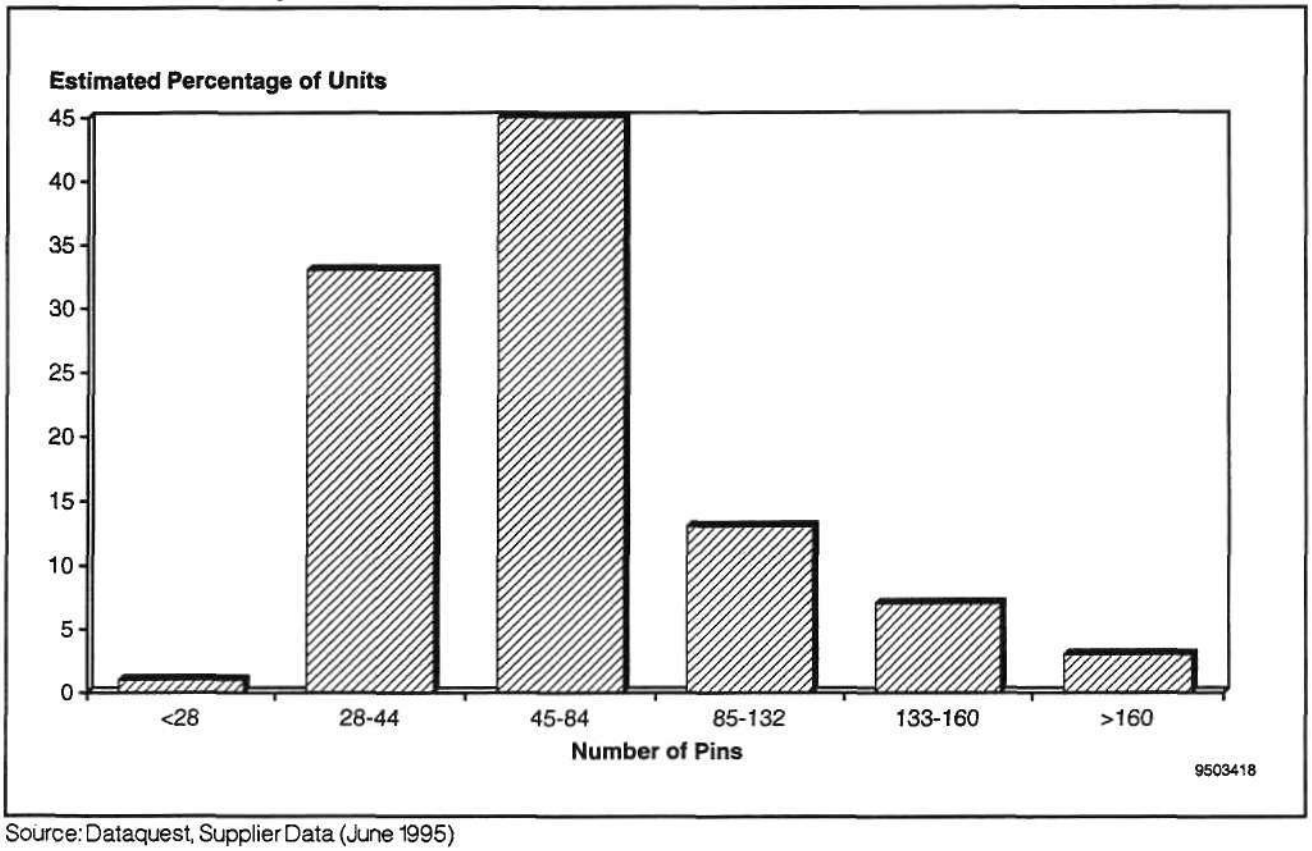
66 MHz, twice the PCI bus speed. And, with other applications such as asynchronous transfer mode on the design horizon, speed will be a critical factor for those emerging applications.

I/Os and Pin Counts

Although about two-thirds of the HD-PLDs were packaged in PLCCs, nearly 80 percent of the HD-PLDs shipped in 1994 were in packages of 84 pins and less. This is evident in Figure 4, which shows that the largest concentration of HD-PLDs was in the 45- to 84-pin-count range (the upper limit of the PLCC) and suggests that designers may soon have to consider other package types for their next-generation designs. Dataquest expects that higher pin counts will follow higher-I/O and higher-density requirements in the near future. Form factor requirements also will drive PLDs into low-profile QFPs and eventually BGAs for the higher-pin-count designs.

As PLD designs move forward into higher densities, the gate arraylike functionality that programmable logic provides will require the high I/O requirements becoming more and more prevalent in the industry. The number of pad-limited gate array designs has provided programmable logic with an opportunity to meet the I/O requirements that gate arrays suppliers have sometimes missed.

Figure 4
1994 MOS PLDs by Pin Count



Source: Dataquest, Supplier Data (June 1995)

The Cost Factor

Programmable logic vendors have been on a mission to dispel the high-price myth. Time and time again, system vendors ask what 10,000 gates of FPGA logic cost, and they expect to hear $800 or $400 price points. Cost-cutting programs are being implemented to pass yield and volume discounts to the users of programmable logic. Although 40 percent discounts, year to year, have all but smashed old perceptions, User Wants and Needs study results still suggest that pricing limits the choice of programmable logic nearly 60 percent of the time. Anecdotal evidence suggests a price multiple of less than 4-to-1, which really makes designers take a closer look. Mix in volume, time to market, and preproduction benefits, and a very compelling argument presents itself.

Dataquest Perspective

Programmable logic devices largely exhibited low-density ASIC characteristics through 1994. As the industry grows, and niche applications expand into broader uses, not only will PLDs successfully impact the traditional standard logic and low-gate-count gate array market worth $4 billion, they also will expand into new emerging segments. Similarly, PLD vendors have realized that their devices must be modified to further meet their customers' needs. As a result, PLD product design continues to change, with the greatest advances coming from HD-MOS PLD architects providing size, speed, and packaging/pin count developments.

PLD prices will continue to drop because of process shrinks, manufacturing efficiencies, and new architectures. At the same time, flexibility and time-to-market advantages will contribute to increased PLD use in system designs. Design start information suggests that future unit growth may finally reach the more-than-3,000-gate range, as long as cost needs are being met. The current product trends in density, speed, and I/Os all suggest that programmable logic has an opportunity for continued growth. All these factors, coupled with the new product advances slated for 1995, promise that the programmable logic market is well worth the effort. Sit back and watch where they're growing.

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Competitive Dynamics

ASICs Worldwide

Competitive Analysis

The Fab Four

Abstract: *Real companies do not need fabs, at least at first. That's what the "Fab Four" might say if they were asked if real companies had fabs. Originally a wild bunch of semiconductor companies bucking the trend, the Fab Four—Actel, Altera, Lattice, and Xilinx—have proven that the fabless model works, in the programmable logic market. Although pure size and wafer demand have led members of the Fab Four to take equity stakes in their foundry partners, the companies insist that the fabless model allowed them the freedom and focus they need to become the Fabulous Four—four pure play programmable logic companies experiencing explosive growth in 1995 with a promise of future growth. This document takes a current snapshot of the Fab Four and reviews those factors contributing to their success.*

By Duane Kuroda

Success by Design

The Fab Four: The name may have meant fabless four at one time, but there's no doubt now that the name could easily translate to the fabulous four. The mix of programmable logic and the fabless semiconductor model has yielded four of the five leaders in the programmable logic market. Actel, Altera, Lattice, and Xilinx are pure play programmable logic vendors; all have estimated 1995 revenue over $100 million. The fab model may have changed for a few of these vendors, but they have grown to dominate the programmable logic industry. Revenue has blown past expectations in 1995 for these companies, and examining the factors behind their recent success reveals the dynamism of one of the most exciting opportunities in the semiconductor market.

PLD Market Overview

The programmable logic market is divided into two process technologies (bipolar and MOS) and three product categories (SPLD, CPLD, and FPGA).

Dataquest

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The bipolar SPLDs represent a declining segment in which designs are being converted to MOS SPLDs and MOS high-density PLDs (CPLDs and FPGAs combined). However, the total SPLD market (bipolar and MOS) is expected to decline over 10 percent between 1994 and 1999. The growth is shifting to other segments of the programmable logic market—the high-density segment. Most companies with a significant investment in high-density PLDs are enjoying healthy growth this year and are looking forward to more in the near future. In fact, a focus in MOS high-density PLDs is the key reason for the explosive growth of Actel, Altera, Lattice, and Xilinx, which combined represented 64 percent of the entire programmable logic market and 80 percent of the high-density programmable logic market in 1994. Table 1 shows the most recent forecast for high-density programmable logic.

Table 1
MOS High-Density Programmable Logic Consumption
(Millions of Dollars)

	1994	1995	1996	1997	1998	1999	CAGR (%) 1994-1999
CPLD	306	519	715	967	1,292	1,714	41.1
FPGA	450	668	881	1,143	1,455	1,817	32.2

Source: Dataquest (October 1995)

The astonishing growth of the high-density products can be attributed to numerous factors, including the following:

- Continued price reductions, typically from 20 percent to 40 percent each year
- Better EDA tools for design at all levels, from SPLDs through FPGAs
- An increased need for integration and reduced chip count
- Increasing pressure on product life cycle

The programmable logic market holds profits for most of its participants; however, the successful players have not made their mark by chance—they are successful by design.

Company Briefs

The Fab Four are discussed in alphabetical order in the following sections, with special attention to the factors behind the success of each company. Each has tackled the programmable logic market in its own way, and no two have identical strategies. As in the ASIC market, programmable logic players must diversify and focus on specific target markets.

Actel Corporation

Actel Corporation
955 East Arques Avenue
Sunnyvale, California 94086
(408) 739-1010

Key Product Offerings

Actel's key product offerings in the FPGA segment as identified by the company are as follows:

- ACT 1 family: 1,200- to 2,000-gate array equivalent gates
- ACT 2 family: 2,500- to 8,000-gate array equivalent gates
- ACT 3 family: 1,500- to 10,000-gate array equivalent gates
- 1200XL family: 2,500-gate to 8,000-gate array equivalent gates
- 3200DX family: 6500- to 40,000-gate array equivalent gates

Actel is the only company in the Fab Four with products in a single market subsegment, FPGAs, and is also the only PLD vendor to use polysilicon antifuse in its products. As the pioneer and market leader of antifuse FPGAs, Actel proved that antifuse design was possible and that it could be a viable production solution.

The company has been experiencing greater growth and expects to surpass $100 million in 1995 after buying out Texas Instruments' FPGA business, its second source. But other factors beyond its reclaimed ownership of the polysilicon antifuse market are contributing to Actel's growth. Such factors include:

- The introduction of the 1200XL family
- The introduction of the 3200DX family
- Continued advances in software and software alliances

On its march to provide higher integration and lower cost, Actel's newly introduced 1200XL family yields 50 percent higher performance at 50 percent lower cost. Such benefits to the design community have been well received, and customers keep asking for more. By driving down cost and increasing performance, Actel continues to address customer's needs. And with the focus on tools discussed later, Actel covers three of the four design needs of the PLD needs pyramid, speed, cost, and ease of design, without ignoring the fourth, density.

That's where the 3200DX family fits in. The 3200DX placed Actel back into the running as a major player in the density game. Not only that, Actel borrowed a play from Altera's offensive play book and introduced a hybrid FPGA. With CPLD-like decode logic combined with embedded SRAM, Actel's 3200DX introduced a product with the features necessary for system logic integration.

Actel deserves a great deal of credit for understanding the market and adjusting to it. A few years ago, Actel stepped aside and took a long hard look at the market and at where the company's strengths lie. Since then, it has repositioned itself as a company where experience and leadership in

the antifuse market are paramount and where churning out the next big device does not supersede quality design. The quality of a design does not lie solely in the hardware, and Actel also realized that software innovation plays a critical role. By understanding and predicting market needs, Actel has used alliances and partnerships in a way that makes the design of its parts less work and more of an art. The Actel team has brought the ActGen macro generator to the market as well as a feature-packed Designer Series of software that can be integrated into the Escalade top-down design methodology.

Table 2 shows a brief history of Actel's growth.

Table 2
Actel Revenue and Net Income (Millions of Dollars)

	Q1/94	Q2/94	Q3/94	Q4/94	Q1/95	Q2/95	Q3/95
Revenue	16.1	18.9	20.2	22.0	19.5	26.6	29.8
Net Income	1.2	2.2	2.2	2.3	-9.6	1.7	2.9

Note: In the first quarter of 1995, Actel took a charge for the acquisition of Texas Instruments' FPGA business.
Source: Dataquest (October 1995)

Altera Corporation

Altera Corporation
2610 Orchard Parkway
San Jose, California 95134-2020
(408) 894-7000

Key Product Offerings

Altera's key product offerings as identified by the company are as follows:

- SPLD (CMOS) segment
  - Classic family: 150- to 900-gate array equivalent nominal gates
- CPLD (CMOS) segment
  - MAX 5000 family: 300- to 3,800-gate array equivalent nominal gates
  - MAX 7000 family: 1,200- to 5,000-gate array equivalent nominal gates
  - MAX 9000 family: 6,000- to 12,000-gate array equivalent nominal gates
  - FLEX 8000 family: 2,500- to 16,000-gate array equivalent nominal gates
  - FLEX 10000 family: 10,000- to 100,000-gate array equivalent nominal gates
  - FlashLogic family: 2,500- to 7,000-gate array equivalent nominal gates

Altera has been recognized as the software leader of the programmable logic market for quite some time. Recently, however, Altera has made hardware announcements the focus of the limelight, while steadily improving the software in the background. With this mix of hardware and software design, Altera has continued to lead the CPLD market in sales. The keys to Altera's success include the following:

- Software widely recognized for ease of use
- A broad range of products, from SPLDs through CPLDs
- Innovations in product architectures

In the programmable logic market, as in the microprocessor market, software sells hardware. In fact, throughout much of the initial growing period of the programmable logic market, the strength of Altera's software program was the deciding factor for many of the companies choosing its devices. Marketing managers were often asked if a package could accomplish the same things as Altera's, so other programmable logic vendors have sought to build "Altera-like" EDA programs. As a result, Altera lays claim to one of the largest installed bases of design software, but an innovative distribution approach has allowed even wider dissemination of its popular design tools.

Besides software, the availability of both simple and complex PLDs has made Altera the de facto upgrade vendor for many system designers migrating from PAL-class devices to higher-density CPLDs. In fact, Altera was a driving force in convincing designers that CPLDs were simply groups of PALs connected with a unique interconnect matrix. Its education program worked, and Altera's growth in the CPLD market reflects that success.

Beyond product breadth and software ease of use, Altera also is known for innovative product architecture. It was the first to break the "box" around conventional CPLD architecture when it released the FLEX 8000, which was an SRAM-based hybrid FPGA-like CPLD. By providing CPLD-type timing with FPGA-type densities, Altera proved that CPLDs were not relegated to the low end while FPGAs had the glamour in the high end. The FLEX 8000 has been a major success story for the company and competes well against the likes of Xilinx for high-density sockets. Altera was also the first to announce embedded SRAM in the FLEX 10000 family, which extends the FLEX 8000-type architecture to even higher densities where embedded SRAM is a must. By carefully analyzing its market, Altera correctly and appropriately recognized the need for memory that is prevalent in the gate array market, where much future growth lies. The FLEX 10000 family, based on the already-hybrid FLEX 8000 family, again presented new possibilities for the CPLD market and programmable logic as a whole.

Altera's product innovations were not limited to FPGA density competition. Altera was also the first to push beyond the 256-macrocell barrier that other combinatorial-intensive CPLDs faced. Thus, the MAX 9000 family proved that Altera's product innovation leadership was not limited to one or two products. With the acquisition of Intel's programmable logic business, Altera also brought another hybrid under its wings, the FlashLogic family of CPLDs. The FlashLogic family mixes low-power SRAM technology with standard, block-of-PALs CPLD design.

Table 3 shows a brief history of Altera's growth.

Table 3
Altera Revenue and Net Income (Millions of Dollars)

	Q1/94	Q2/94	Q3/94	Q4/94	Q1/95	Q2/95	Q3/95
Revenue	43.5	47.1	49.1	59.2	75.0	92.2	109.1
Net Income	7.7	8.3	8.4	-9.8	15.1	19.6	23.7

Note: In the fourth quarter of 1994, Altera took a charge for the acquisition of Intel's PLD business.
Source: Dataquest (October 1995)

Lattice Semiconductor Corporation

Lattice Semiconductor Corporation
5555 Northeast Moore Court
Hillsboro, Oregon 97124
(503) 681-0118

Key Product Offerings

Lattice's key programmable logic product offerings are as follows:

- SPLD (CMOS) segment
  - GAL product family: 100- to 1,000-gate array equivalent nominal gates
- CPLD segment
  - pLSI/ispLSI 1000 product family: 1,000- to 4,000-gate array equivalent nominal gates
  - pLSI/ispLSI 2000 product family: 500- to 2,000-gate array equivalent nominal gates
  - pLSI/ispLSI 3000 product family: 4,000- to 7,000-gate array equivalent nominal gates

Lattice Semiconductor is exhibiting the signs of a successful transformation. Just a few years ago, analysts and industry watchers were cautious about Lattice's prospects. An attempt to acquire QuickLogic failed, high-density products had not taken off, and price competition in the GAL market was on the upswing. Lattice looked like a SPLD supplier in a market where CPLDs and FPGAs were the next big thing.

To its credit, Lattice saw its situation and moved to reposition itself. The keys to Lattice's success include:

- Continued speed leadership in its bread-and-butter market
- Expanded device coverage and software upgrades
- Transition to CPLDs
- Increased isp usage and endorsement by competitors

While the industry appeared to move on to the more interesting CPLD and FPGA market, Lattice quietly chugged along and continued development of its GAL class devices. The result was faster and faster SPLDs, the fastest the market has seen, and Lattice maintained ownership of the title of "speed

leader." In the programmable logic market, bragging rights and company track record are valuable assets.

Also important has been Lattice's attention to software. After analyzing the software ramp-to-revenue cycle so often talked about in the industry, Lattice jumped on the bandwagon and began moving an updated software package. Claiming software run rates nearly as high as those from Altera and Xilinx, Lattice is now reaping the rewards of the industry adage that software sells hardware. Its growth in revenue tells the story.

Concomitant to the ramp in software, Lattice was busy introducing new devices in its isp2000 and isp3000 families. Providing both high speed and increased density gave Lattice a shot in the arm in product development as its competitors duked it out for bragging rights to the densest and fastest CPLDs. The pressure to move to high-density devices was successful. In just over a year, Lattice moved from receiving less than 10 percent of revenue in high-density products to over 25 percent. By continuing to focus on the expanding high-density market, Lattice can remove customers' concerns about its huge installed base in the declining SPLD market.

Further, Lattice received indirect endorsements from its competitors using isp technology. The early evangelist of isp, Lattice held onto the idea of in-system programming when others said it was a problem. Now every major programmable logic vendor competing in the CPLD market claims to use some version of isp. Altera and AMD, the two largest players in the CPLD market, have welcomed isp to the fold and heavily promote such devices for the time, manufacturing, and functional benefits they provide.

Table 4 shows a brief history of Lattice's growth.

Table 4
Lattice Semiconductor Revenue and Net Income
(Millions of Dollars)

	Q1/94	Q2/94	Q3/94	Q4/94	Q1/95	Q2/95	Q3/95
Revenue	30.2	32.9	34.5	36.3	40.3	45.0	48.6
Net Income	5.6	6.0	6.4	6.9	7.7	8.8	9.8

Source: Dataquest (October 1995)

Xilinx Inc.

Xilinx Inc.
2100 Logic Drive
San Jose, California 95124
(408) 559-7778

Key Product Offerings

Xilinx's key CMOS product offerings as identified by the company are as follows:

- CPLD segment
  - XC7200 family: 800- to 1,600-gate array equivalent nominal gates
  - XC7300 family: 800- to 3,000-gate array equivalent nominal gates
  - XC9500 family: 800- to 12,800-gate array equivalent nominal gates

- FPGA segment
  - XC2000 family: 600- to 1,500-gate array equivalent nominal gates
  - XC3000 family: 1,000- to 7,500-gate array equivalent nominal gates
  - XC4000 family: 2,000- to 25,000-gate array equivalent nominal gates
  - XC5000 family: 2,200- to 18,000-gate array equivalent nominal gates
  - XC6200 family: 9,000- to 55,000-gate array equivalent nominal gates
  - XC8100 family: 1,200- to 8,700-gate array equivalent nominal gates

Xilinx fought its way to becoming the No. 1 supplier of programmable logic in 1994 and has kept its lead through 1995. The company has been introducing new families and architectures as if previous devices were going out of style. Xilinx's success factors, which need to be understood by all who play the game, are as follows:

- Large installed base of software seats
- Aggressive pursuit of EDA technology
- Continuous product innovation

Xilinx enjoys one of the largest installed software bases for electronic design automation at any level. By marketing aggressively and assisting its customers in the design process, Xilinx almost single-handedly created the FPGA industry. Being first had its benefits, as Xilinx quickly ramped up its installed base and did nearly everything it could to keep customers. By pursuing both hardware and software improvements, Xilinx graduated its customer base to increasingly high-density designs.

This brings us to the company's focus on EDA technology. Xilinx made no bones about its acquisition of NeoCad, which instantly gave it a shot in the arm, providing the talent and experience necessary to support Xilinx's rapidly growing product portfolio. In a smooth stroke of the pen, Xilinx acquired engineers, incorporated highly regarded software, and placed significant hurdles (at least perceived hurdles) in the paths of its competitors. Merging the existing and acquired software talent may be a challenge, but when the process is complete, Xilinx's software offering will be no less than top of the line.

Xilinx's rapid-fire announcement of four major new architectures was a clever attempt to diversify its product portfolio while making competitors sweat. At a rate of one major announcement a quarter, Xilinx has flexed its R&D muscles to boost its EPLD effort, enter the antifuse fray, address the nascent coprocessing market, and drive toward low-cost solutions. The product map may appear confusing, but a deeper look will reveal that Xilinx is giving its customers a choice. By not forcing them into a single architecture, Xilinx can allow customers to pick and choose the architecture best suited for their application.

Table 5 shows a brief history of Xilinx's growth.

Table 5
Xilinx Revenue and Net Income (Millions of Dollars)

	Q1/94	Q2/94	Q3/94	Q4/94	Q1/95	Q2/95	Q3/95
Revenue	75.4	75.2	79.5	91.3	109.2	125.8	141.2
Net Income	19.3	12.0	11.8	15.6	19.9	18.0	29.8

Source: Dataquest (October 1995)

Dataquest Perspective

System design continues to demand shorter and shorter product-design cycles, while gate array vendors face capacity constraints and seek to fill their fabs with high-gate-count, high-margin products. As a result, gate array vendors have been moving out of the low-density design market and have left a gap that PLD vendors are more than happy to fill. Find a market need and fill it, and the revenue is yours for the taking. The Fab Four continue to find that a winning proposition.

So which is the best PLD company for your needs? It still depends. Each vendor has successfully positioned itself in the market. Pick your market, CPLD or FPGA, and whether you want service, software, or speed. Chances are that one of the Fab Four has the product that will meet your needs.

Although the Fab Four as a group are a success story for the fabless semiconductor model, that does not mean that they have a lock on the programmable logic market. Broad-based semiconductor supplier AMD and vertically integrated AT&T have also made inroads recently with their high-density offerings. They were not discussed in this article because of their fab status, but they cannot be counted out. Such companies bring advantages unseen heretofore in the high-density programmable logic market. As these companies bring their competitive technology to bear, look for increased competition to liven the market even further.

The latest breed of fabless PLD vendors includes Zycad, QuickLogic, and Crosspoint, which are out to prove the model again in their own way. Of these three, only Zycad has multiple foundry sources using a reprogrammable technology. Each has its own strengths and weaknesses; however, each needs to assess its strengths and weaknesses in light of how the Fab Four are positioned. It may be possible for a company to fill a particular niche better than the Fab Four, but a poorly positioned product may lead to more of a battle of resources than of design efficiency. Smaller competitors had better spend their marketing dollars wisely and prepare for a rocky ride. The programmable logic window has just about shut, and current competitors need to position themselves properly to ensure continued growth.

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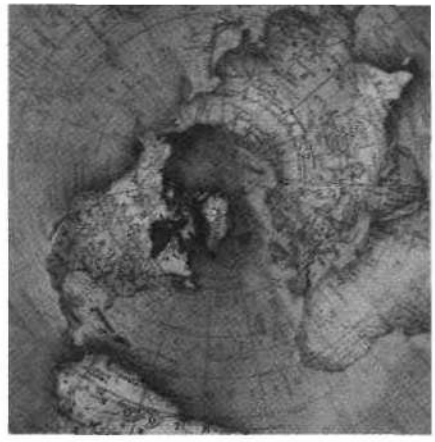
Dataquest

Focus Studies



Dataquest

The ASIC Road Map to the Multimedia Dream

Focus Report

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Chapter 1
Executive Summary

Multimedia and set-top box applications are hot topics in many circles. But, in the final analysis, much of the end-system functionality is dependent on silicon. Dataquest expects that if companies are to be successful in these markets, they must have a thorough understanding of the target customer base as well as system design requirements. The purpose of Dataquest's Focus Reports is to provide our clients with the most in-depth, up-to-date information on electronic system design. Dataquest's ASICs Worldwide service surveys designers of electronic products extensively and reports upon their shifting priorities, desires, and demands to provide a valuable snapshot of user trends.

This ASICs Focus Report is the second in a series of three reports that also includes North America and Japan User Wants and Needs (*System Designers Uncover ASIC Opportunities,* by Duane Kuroda, June 26, 1995, ASIC-WW-UW-9501) and a European ASICs Focus Report. These reports are intended to be used by business executives to identify significant trends in electronic system design and to explore potential target markets for ASIC devices. The basis for these reports is the nearly 700 responses received from an end-user survey.

Report Structure

This report, focusing on multimedia and set-top boxes in North America, is divided into five main chapters, with each investigating a particular aspect of the respective ASIC markets and the associated electronic system design. It begins with an executive summary that includes an overview of the major issues.

Chapter 2 provides a general overview of the components of the multimedia and set-top boxes. Brief discussions cover the important functions being implemented in today's systems.

Chapters 3 and 4 delve into system and device design trends and issues for multimedia and set-top boxes in North America. Besides the demographics of the sample, the systems portion of these chapters covers critical factors for market success, signal layers, and HDL usage. Gate counts, speeds, and packaging required for next-generation system design round out these chapters.

In the final chapter, Dataquest explores the major implications of the findings from this research and looks at how these trends will interact with the trend toward system-level integration (SLI).

Major Issues

Our survey of multimedia ASICs and set-top box ASICs used by system designers provides insight into their preferences and consumption patterns, as well as into the directions of future design. Later chapters expand on the following issues:

- Group 1 multimedia ASICs (multiple-chip solutions) are on the way out.

- Group 2 multimedia ASICs (true system functionality on a chip) lead the pack in proving that system-level integration is a reality.
- Group 3 multimedia ASICs (Group 2 with concurrent processing and hardware-software co-design) are on the horizon.
- Group 4 multimedia ASICs (Group 3 exploiting device physics for performance) usher in the ultimate levels of performance.

An important outgrowth of the above is the functional blocks that ASIC suppliers are providing to enable cutting-edge multimedia to become a reality. It is just not enough to create a Group 2 design with any cells that are available. See Chapter 2 for a special review of some of these issues.

The profile for multimedia and set-top box designers in Chapters 3 and 4 suggests an alignment on HDL choice. These chapters also reveal a divergence in design preferences as designers move to gate array and cell-based technology for different reasons.

The ASIC model is changing, with the emerging applications of multimedia and set-top boxes leading the way. ASIC suppliers and system designers must understand this changing model to remain competitive.

Project Manager: Duane Kuroda

Chapter 2
Multimedia and Set-Top Box ASIC Trends

Multimedia

Gone are the days of working on the gate level or selecting low-level cells such as multipliers, accumulators, and up-down counters as the core of ASICs. Now, designers speak in terms of megafunctions, megacells, specialized cores, and system-level integration. The industry continues to move ahead, and the tried and true library cells that provided an edge a year ago are starting to accumulate dust. System designers are now saying: "Optimize this function, optimize that function, and put it on a newly optimized and characterized process for die savings or performance."

The ASIC market is getting more complex by the day in emerging applications such as multimedia and set-top boxes. The multimedia ASICs represent the core or critical system functionality at the heart of many of these system designs. Typically, buzzwords involve such terms as JPEG, MPEG 1, YUV color space conversion, wavetable synthesis, FM synthesis, or TrueSpeech. Each of those functions can easily represent a single-chip solution today, but for future use, they must be cells in an ASIC library.

Multimedia ASICs represent a wide array of topics, only a few of which are touched on in this report. The old and simple definition—combining audio and video—no longer suffices. Instead, communications functions, including fax, modem, and voice-over-data (DSP-type solutions), have been added to the mix. ASIC solutions have addressed each category separately in the past, but now more frequently combine functionality to provide high performance and cost savings.

Audio

An important part of the multimedia mix is functionality supplied by the audio ASIC. Capable of implementation as a custom solution performing various forms of sound synthesis, audio ASICs can vary widely in incorporating DMA controllers, bus interfaces, DACs, or emulation of PC peripherals such as UART, Soundblaster, and MIDI. Some implementations are performed by a DSP standard product, while others are DSPs integrated onto an ASIC that may include dedicated decode logic or custom audio processing features. No matter what the implementation, key functionality provided by audio subsystems includes:

- Audio compression (TrueSpeech, MPEG, Dolby AC-3)
- Sound synthesis (AM, FM, wavetable, waveguide)
- Resonant filters for improved voice quality

Video

ASICs for video are an important group, not only as VGA or Super VGA accelerators but also as an umbrella including graphics and image processing solutions. Designers responding to the user survey reported average speeds on their video designs at 60 MHz. Trends toward more integrated solutions have been notable. It is not uncommon to find combinations that include a graphics accelerator, graphics controller, RAMDAC,

DMA controllers, and a local bus interface as standard features. Those looking to provide added value can pick and choose from a number of other functions to differentiate products. A few such options include:

- FIFOs
- DACs
- LCD controllers
- ISA interfaces
- Frame buffers and interfaces
- NTSC encoders
- Color space converters

Graphics

As system feature requirements increase, the distinction between a video design and a graphics design blurs further. Standard video solutions are expected to include features formerly relegated to graphics chips. Many graphics subsystems have announced clock speeds of 50 MHz, although some newer designs claim to support speed specifications up to 100 MHz. Graphics/image processing designers reported in the survey that, in 1995, their designs ran at similar speeds, averaging near 50 MHz. The list of features implemented by graphics and image processing designers is quite extensive, with vendors selecting feature sets for competitive advantage. Important functions include:

- Raster ops engines
- Texture mapping
- Flat and Gouraud shading
- Z buffering
- Clock recovery
- Error detection
- Error recovery/correction (Reed Solomon or Viterbi)
- Audio/video synchronization

Integrating Multimedia Functionality

However, the graphics category does not stand alone. The drive for multimedia is adding to the confusion about the functionality expected of graphics subsystems. Multimedia ASICs have garnered press attention because leading-edge technology is bringing a new level of realism to consumers. Audio, video, and graphics solutions can be mixed and matched, then served up with even more functionality, such as MPEG or telephony—and the list of functions or cells needed to cover design requirements becomes even broader. Such features include, but are not limited to:

- Custom motion estimation processors
- 3-D transformation engines

- DigiCipher II
- MPEG 1/MPEG 2—audio and video
- Motion JPEG
- Data modems
- Fax modems
- Telephone answering machines

Multimedia ASICs are not synonymous with MPEG, as some would have you believe. MPEG has many components, some of which have now been standardized, some of which have not. Also, many silicon vendors are taking the second-generation MPEG (MPEG 2) route in an attempt to leapfrog early MPEG pioneers. MPEG decoders typically include:

- Huffman decoder
- Inverse quantizer
- Inverse discrete cosine transform logic (DCT)
- Color space conversion
- Motion estimation logic

Optional feature add-ons (in silicon) include zigzag decoding, interlace circuits, deblurring, or run-length decoding. Clearly, the available optional features make MPEG only a standard as the lead vendor implements it. Similarly, broadcast, or nonphysical, MPEG poses a challenge because it supports a different packet protocol than that agreed upon by the MPEG-2 working group. Add to that the potentially error-prone broadcast source, and buffering FIFOs or depacketizing silicon are now required to synchronize and accelerate audio and video data streams that may arrive asynchronously.

Set-Top Box ASICs

A specific technology to implement multimedia—the set-top box—has also attracted much attention. An early incarnation was very expensive and basically acted as a dedicated Silicon Graphics Indy workstation performing client-type functions. Since then, many more designs have been developed. Set-top box technology is a focused combination of the above multimedia technologies to provide a fixed solution. The lack of standards has provoked controversy, and, as a result, there is a plethora of competing architectures. If one looked at the possibilities for a set-top box's feature mix, the number of combinations would appear quite daunting. In reality, however, there are a number of generic features that can be integrated as ASICs for the set-tops. Such features include:

- Satellite downlink converter
- Cable converter
- VCR hookup/interface
- Bus interface
- Video controller
- Audio controller

- DRAM controller
- MPEG or MPEG 2
- Audio decompression logic

Not all the functionality required to design a single-chip ASIC for the set-top box or multimedia solution may be available as an ASIC from a single vendor. However, by selecting the right provider, a tightly integrated solution can be designed to implement the majority of those functions cost-effectively. In this book, Dataquest takes a quick, first-pass look at multimedia and set-top box ASICs.

Chapter 3
Multimedia—North America

Demographics

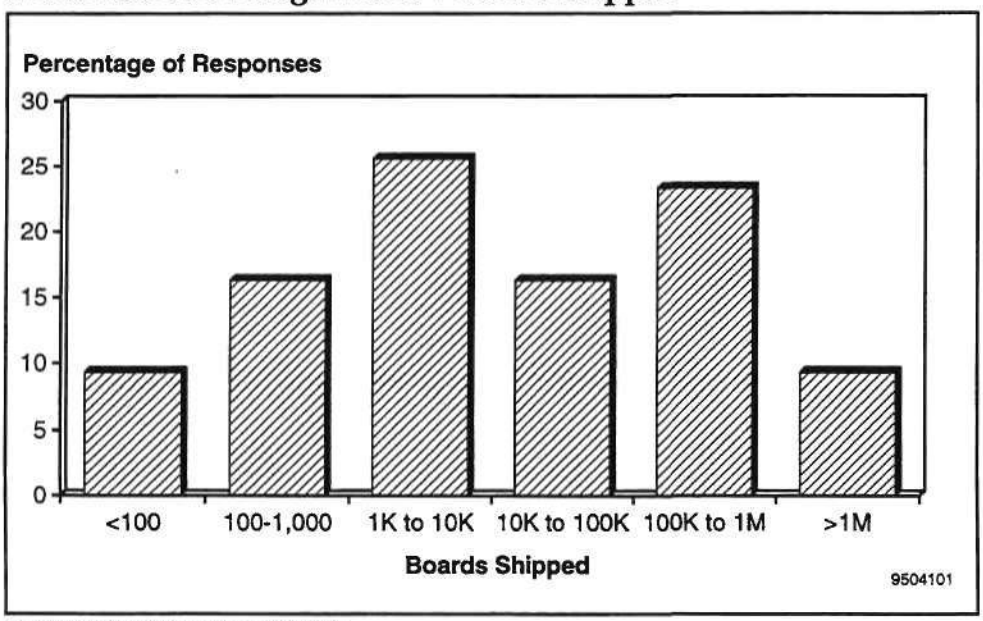
Dataquest analyzed its user data for the multimedia market. More than 45 respondents indicated that they worked on multimedia designs. Nearly 65 percent of the respondents were either system or IC designers and another 20 percent were engineering managers, yielding nearly 85 percent of respondents who work closely with the specified designs.

System Level

Designers in this category indicated that their products achieved a variety of unit volume sales, ranging from 100 units to more than one million units. Figure 3-1 shows the unit volumes shipped reported by designers responding. The bimodal graph clearly shows a demarcation between the high-end, high-value-added suppliers who ship in relatively low volumes and the low- to mid-end suppliers who typically ship in high volumes. Boards in this category average 5.1 signal layers for the current designs, and plans are to incorporate six signal layers in next-generation designs.

Use of partial scan and built-in self-test (BIST) methodologies for ASIC testing is rising as design moves into the next generation. Full scan has lost some ground as fully tested, precharacterized cells have made partial scan feasible. The designers responding reported that use of partial scan will grow nearly 10 percent, from 30 percent in this generation to about 40 percent in next-generation design. Use of full scan will drop only four percent in the next generation, from 43 percent to 39 percent. Board testing is a growing trend, as BIST for the board increased slightly. JTAG penetration is noteworthy, with JTAG for the board expected to increase from over 47 percent in this generation to nearly 55 percent of next-generation designs.

Figure 3-1
Multimedia: Average Board Volume Shipped



Source: Dataquest (August 1995)

Multimedia designers claimed to be Verilog champions, and both Verilog and VHDL use is expected to increase for next-generation designs. Thirty-six percent of respondents indicated that they used VHDL for this generation; nearly 50 percent would use it for next-generation design (see Figure 3-2), an increase of 14 percent. Verilog use starts from a higher base and is also slated to increase, but moves only 10 percent, from 57 percent in this generation to 67 percent in the next generation.

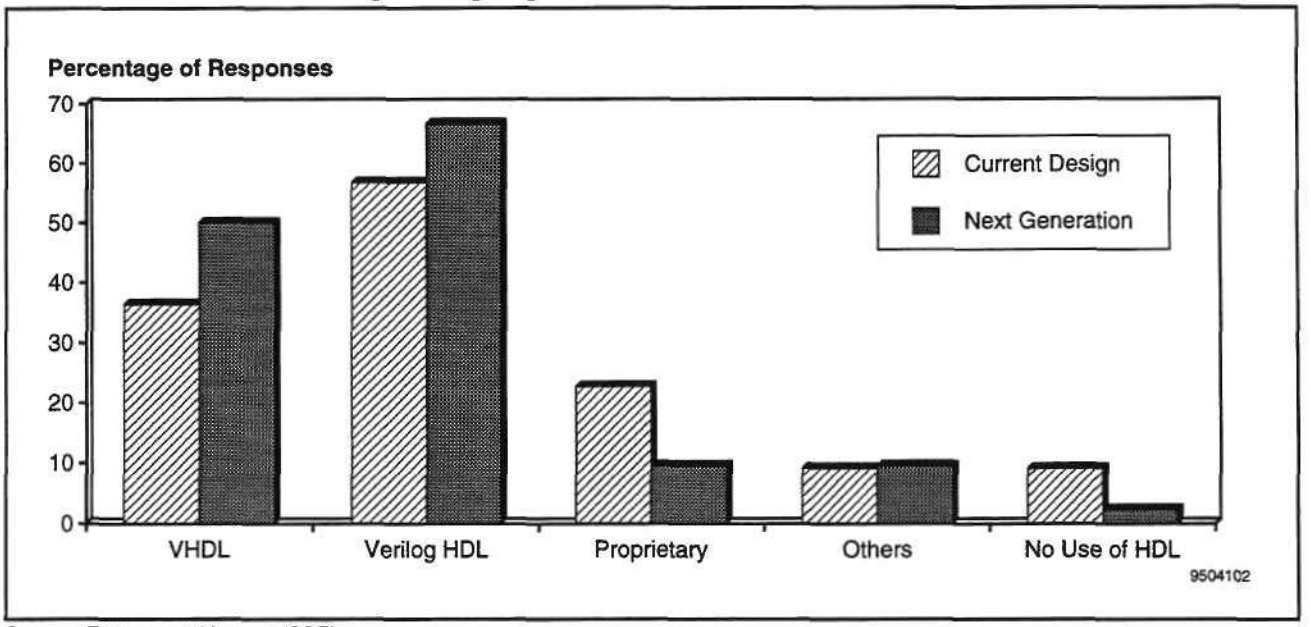
The factors determining market success in multimedia are worth analyzing because of the nature of the market. Multimedia solutions have often been placed on add-in cards, a tough market in terms of margins and price competition. Reducing cost was the No. 1 success factor (see Figure 3-3). The second most important factor was reducing time to market, not unexpected for a market that historically has seen standards built around pioneering companies. Increasing functionality came in a close third, which is also expected because the right combination of bells and whistles (literally, in this case) determines who purchases the product.

Device Trends

Gate Array and CBIC

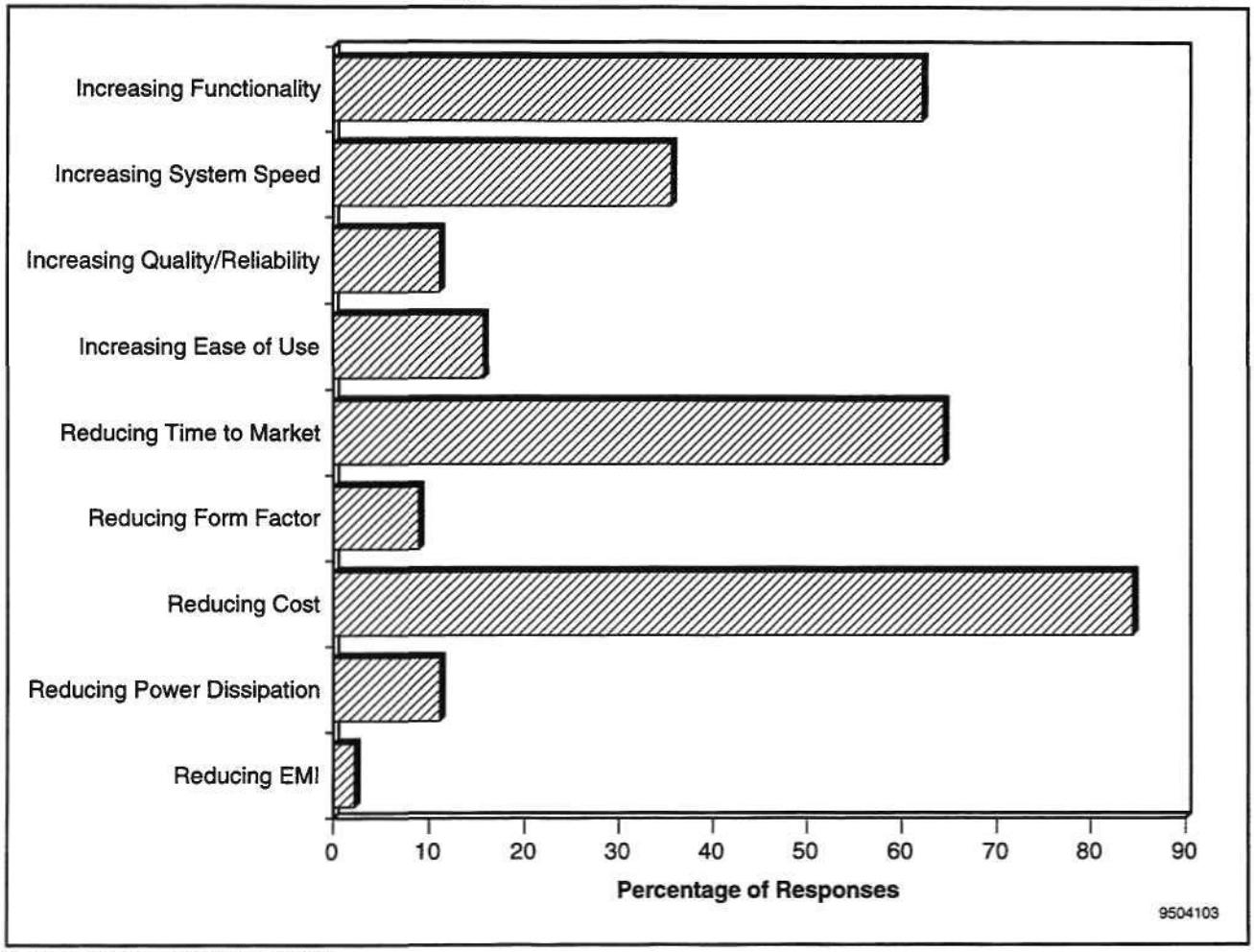
Multimedia designers must, therefore, provide feature-rich products quickly and cheaply. Cost and functionality requirements suggest a lower design rate. Although time-to-market requirements suggest gate array design, and functionality requirements suggest cell-based design, designers in this market are forced to take a close look at the costs and benefits of each technology and the life cycle of the products.

Figure 3-2
Multimedia: Use of Design Languages



Source: Dataquest (August 1995)

Figure 3-3
Multimedia: Factors Determining Market Success



Source: Dataquest (August 1995)

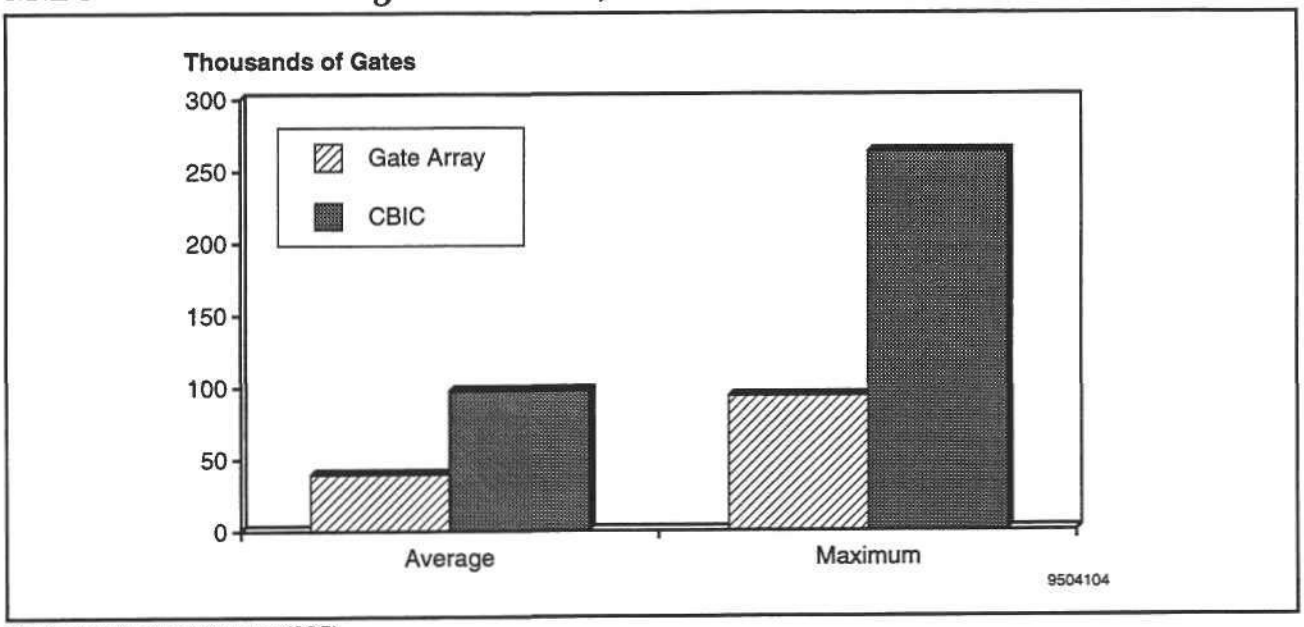
Gate counts for multimedia applications in 1995 are expected to reach 55,000 and 114,000 gates for gate arrays and cell-based ICs, respectively. Clearly, gate array designs are used for lower-density designs (see Figure 3-4) while CBICs are gaining favor for higher gate counts. Multimedia ASICs are incorporating more and more functionality, and the design start distribution (see Figure 3-5) provides a brief snapshot of this emerging market. This graph shows that multimedia designers have the bulk of their designs to the 20K to 50K range.

Design activity also extends fairly evenly into the higher densities, even beyond the 100,000-gate mark, as many of the lower-density designs are being consolidated and/or integrated into larger designs on single chips.

Cell Usage

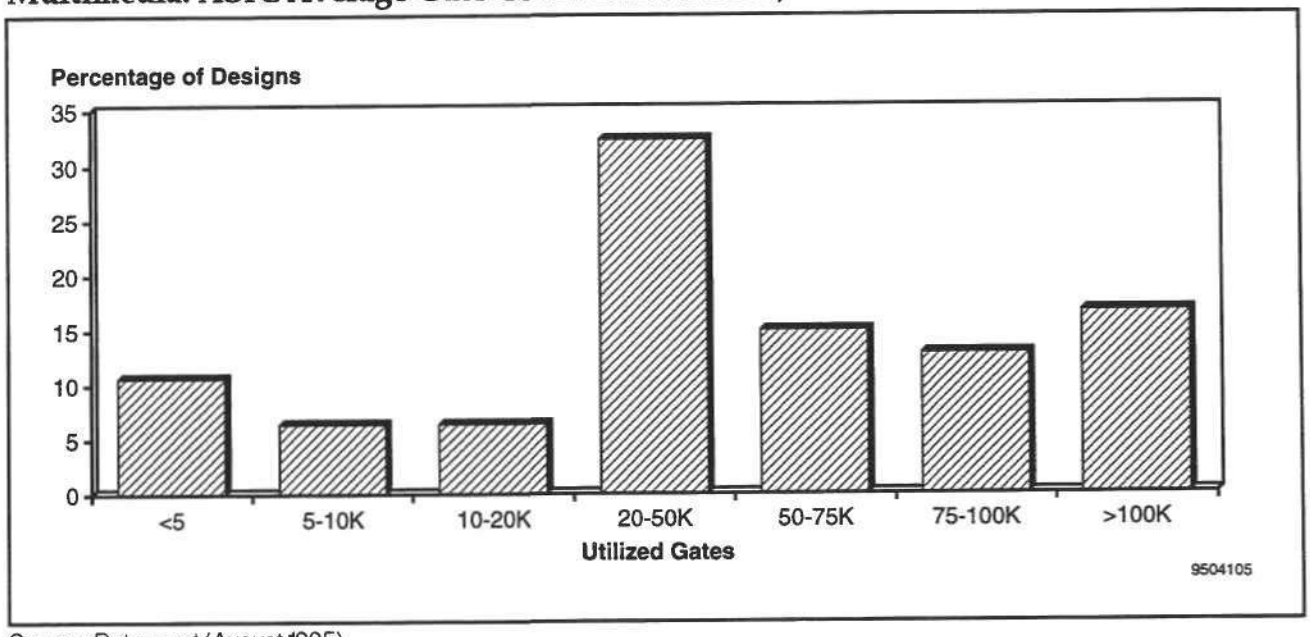
Because of the increasing functionality required for multimedia designs, cell usage has been on the rise for both gate array and cell-based multimedia ASICs. Figure 3-6 shows the respective cell usage in both gate arrays and CBICs. Of note is the heavy use of RAM in cell-based designs. As gate counts increase and integration reaches unheard-of levels, memory use for

Figure 3-4
Multimedia: ASIC Average Gate Counts, 1995



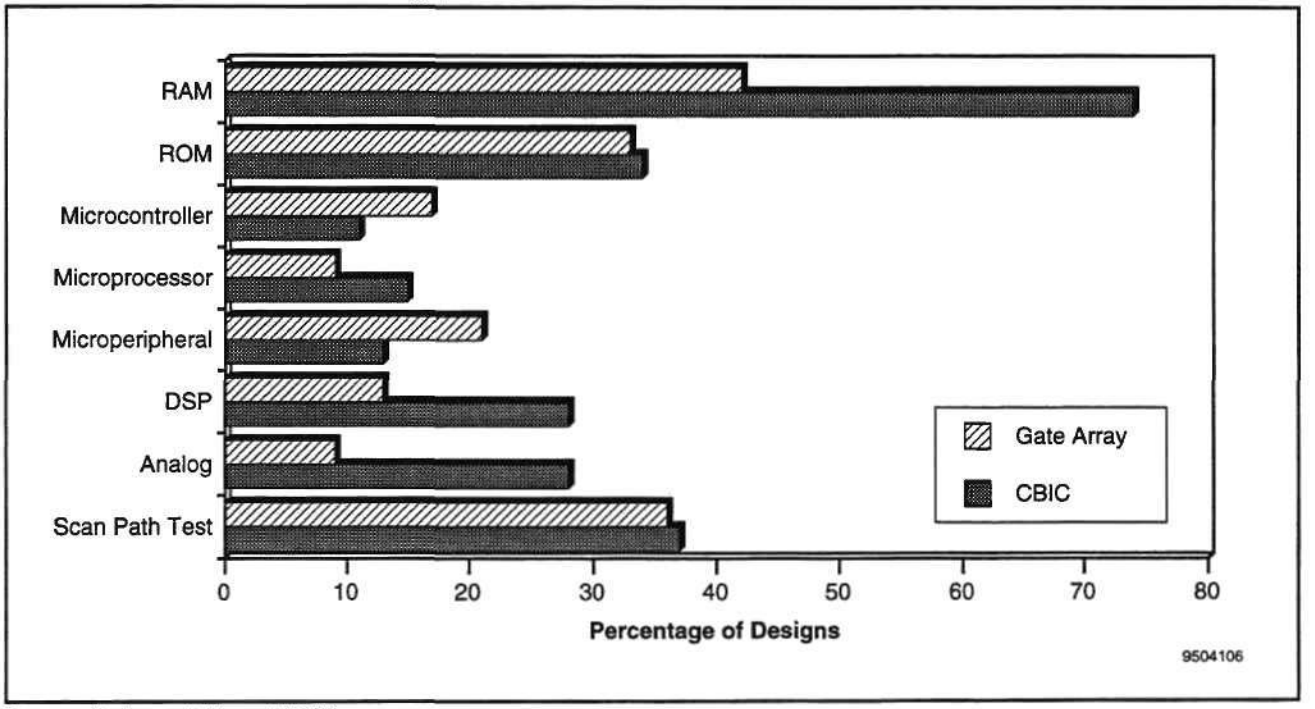
Source: Dataquest (August 1995)

Figure 3-5
Multimedia: ASIC Average Gate Count Distribution, 1995



Source: Dataquest (August 1995)

Figure 3-6
Multimedia: ASIC Cell Usage, 1995



Source: Dataquest (August 1995)

buffering, FIFOs, and scratchpads is on the rise. High-speed memory is most efficiently implemented as compiled cells in CBICs or embedded gate arrays. Expectations for growth of processor use in multimedia seem optimistic; however, R3x00, R4x00, 68xxx, SH70xx, and custom processors are the buzzwords for the multimedia engines of tomorrow. Overall, the inclusion of specialized cells has played an important role in driving gate counts upward for both gate array and cell-based designs.

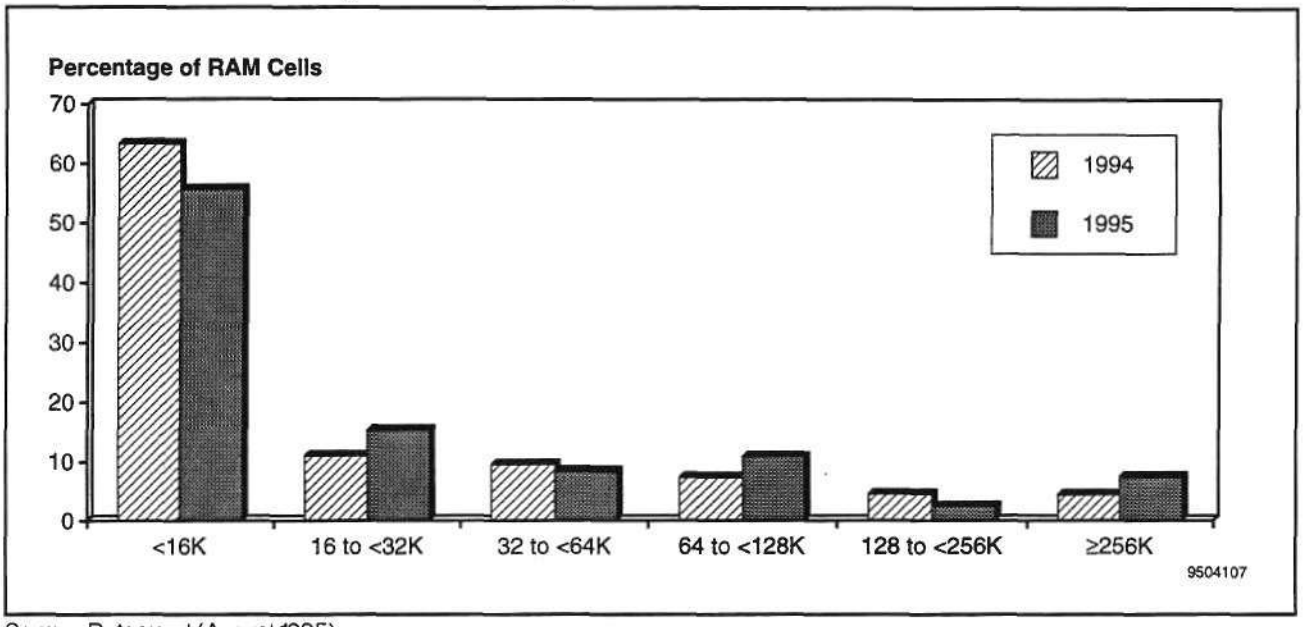
Memory Usage

Inclusion of memory for both gate arrays and cell-based ICs is not only growing in terms of percent of designs, but also in terms of total memory bits used. Figure 3-7 takes a brief look at the total memory bits in gate arrays for 1994 and 1995. The designs behind this distribution include many small distributed memories as well as designs using one or two large blocks on the higher-end ASICs. Designers claim that, for 1995, the total memory usage for those gate arrays using memory will approach a key shift—nearly 50 percent of memory users will require more than 16K total bits.

Clock Frequencies

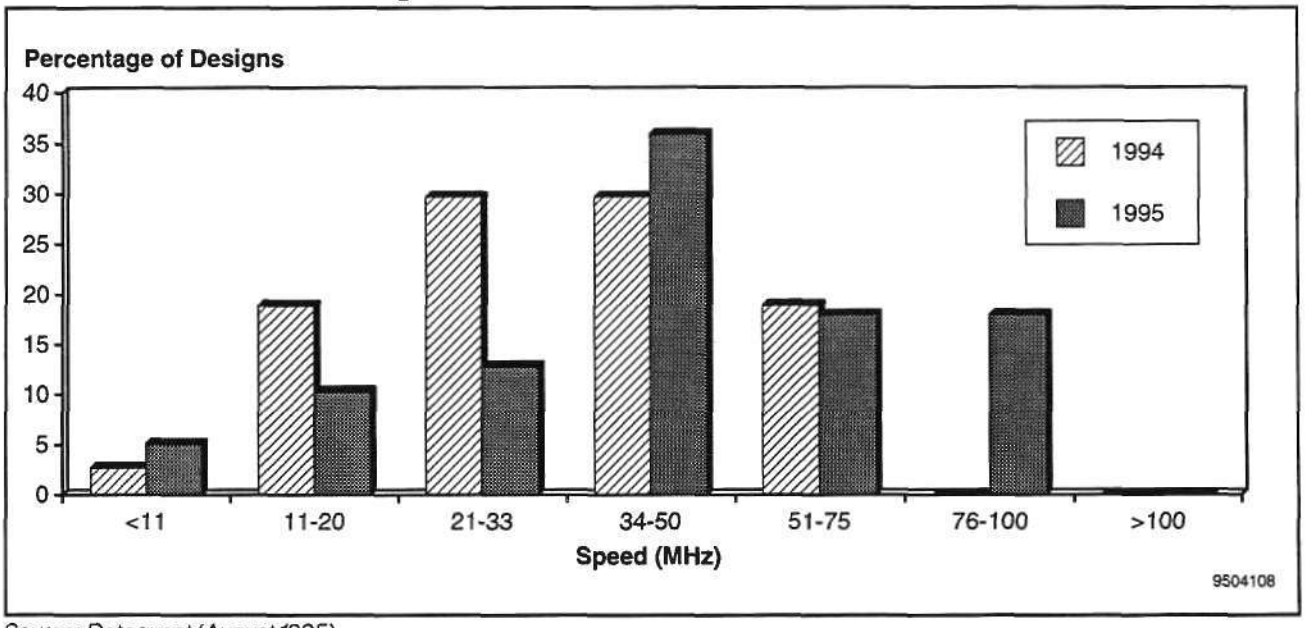
Multimedia designs clocked in at an average of 49 MHz for 1995, ending only slightly above the average. More information is available from the clock frequency distribution (see Figure 3-8). In 1994, very few designs were reported above 75 MHz. Designers planned to change that in 1995, extending ASIC speeds to the 100-MHz realm. Most designs in 1995 lie in the 34-to 50-MHz range. The decline in design starts below 34 MHz reveals a noticeable shift toward higher-frequency solutions.

Figure 3-7
Multimedia: Gate Array Memory Usage



Source: Dataquest (August 1995)

Figure 3-8
Multimedia: ASIC Clock Speeds



Source: Dataquest (August 1995)

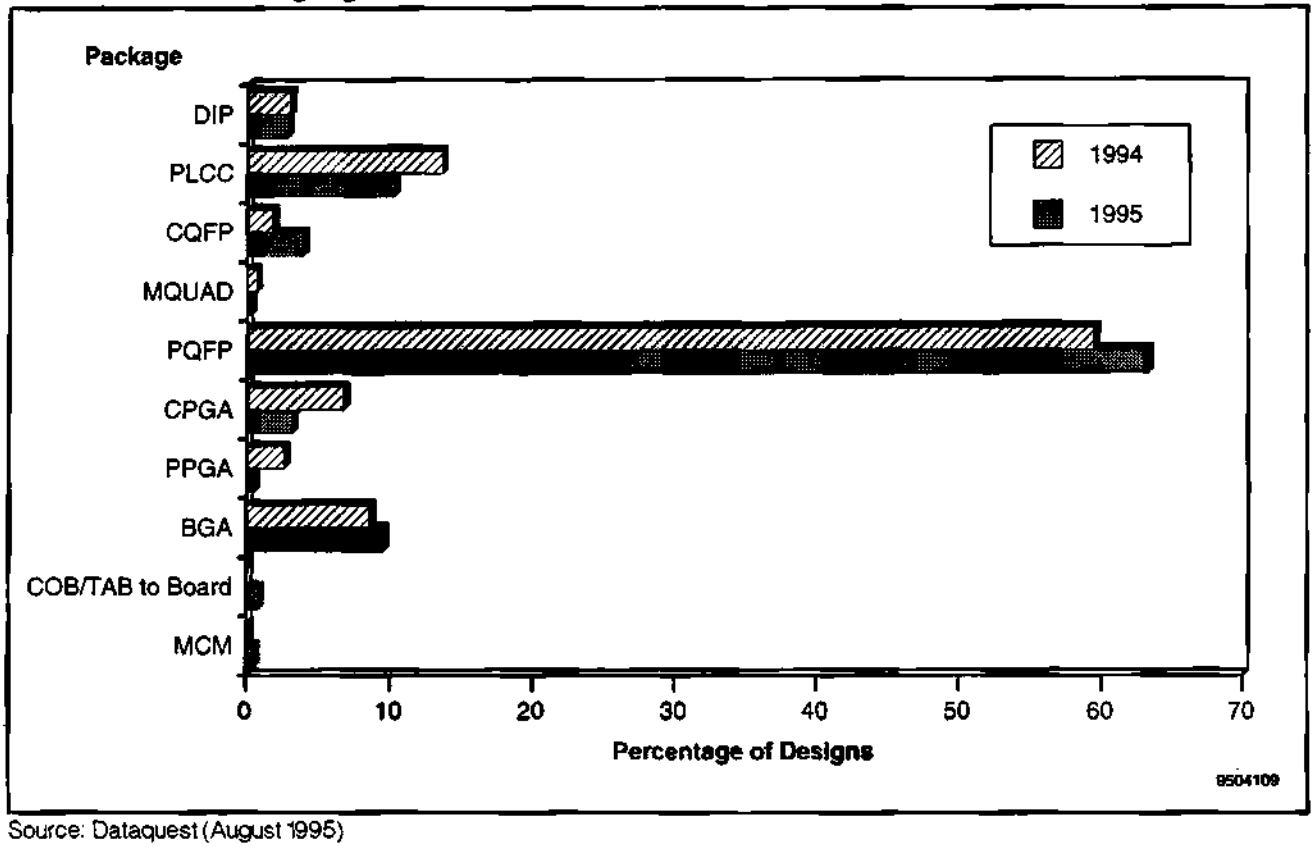
Packaging

Package cost and pin counts are critical to multimedia designers because of board price margins and high I/O requirements. Figure 3-9 shows the gate array design starts by package type, clearly demonstrating that the top three packages are PQFPs, PLCCs, and BGAs. The introduction of thermally enhanced PQFPs has extended the life of PQFPs; however, high I/O requirements will continue to drive designers to consider more reliable packages near and above 300 pins. Current pin use falls largely in the 44 to 244 range, with significant growth above 244 expected (including emerging designs requiring more than 300 pins). BGAs play well into this growth and are gaining in popularity. One chipset vendor has already released a modified BGA that does not require increased signal layers on the board. As these and similar parts reach the market in higher volumes, BGAs will take on more importance.

Programmable Logic

The model for multimedia solutions has typically relied on high value-added at a low price point. Such are the dynamics of the add-in board and PC markets. As a result, programmable logic has not made serious inroads into this market as a production solution. Clearly, simple PLDs continue to find use in glue functions and control logic. Smaller CPLDs and FPGAs, because of their more attractive price points, are sometimes included. However, most programmable logic use has occurred at the prototyping and emulation stage.

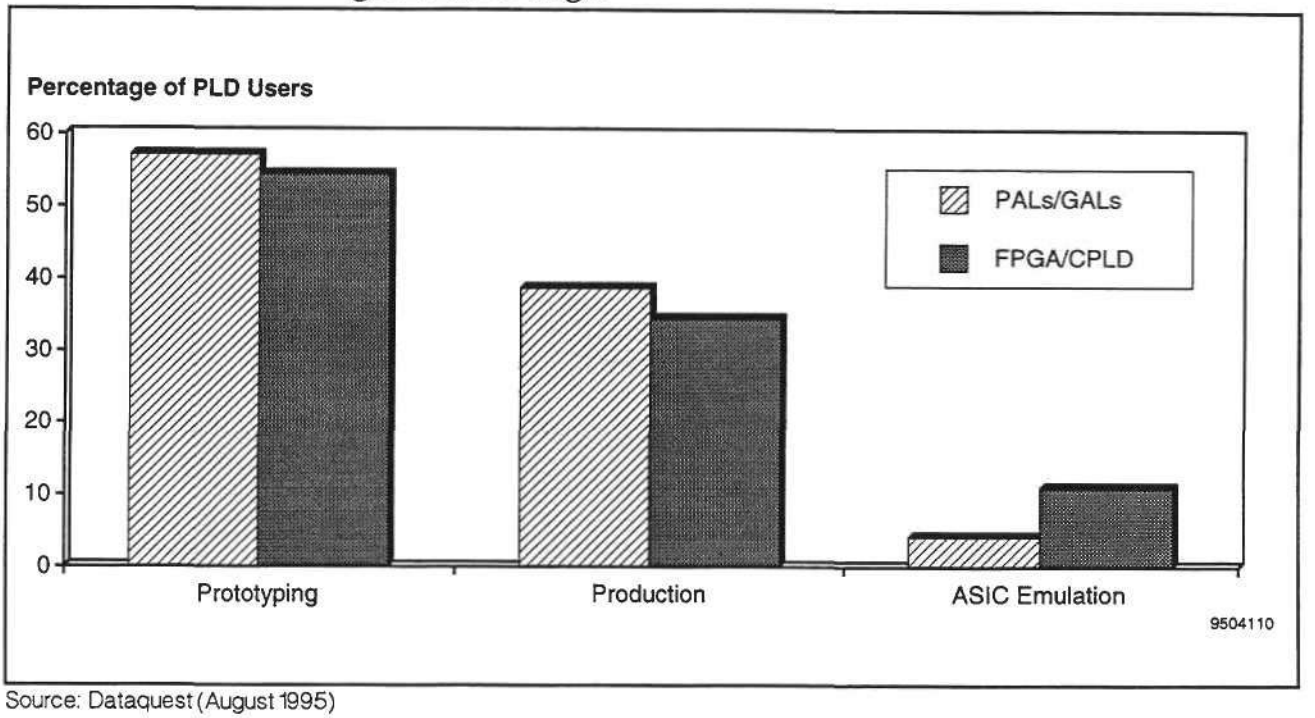
Figure 3-9
Multimedia: Packaging Trends



Source: Dataquest (August 1995)

Figure 3-10 shows use of programmable logic by designers responding to Dataquest's survey. Prototyping use definitely ranked above the all-application average, suggesting that designers have truly awakened to the benefits of programmable logic. Programmable logic has begun to show movement toward achieving the status of a production solution and, for high-end boards (notorious for low volumes), programmable logic supplies critical functionality. PLD usage in emulation is relatively strong for both simple and high-density types.

Figure 3-10
Multimedia: Use of Programmable Logic



Source: Dataquest (August 1995)

Chapter 4
Set-Top Boxes—North America

Demographics

Dataquest analyzed another burgeoning market, the set-top box market. There were more than 25 respondents who indicated that they worked on set-top box designs. Nearly 61 percent of the respondents were either system or IC designers and 27 percent were engineering managers, yielding nearly 88 percent of respondents closely associated with the specified designs. Forty percent of designers reported 50 or fewer employees at their locations, suggesting that many of them came from small companies or tiger teams.

System Level

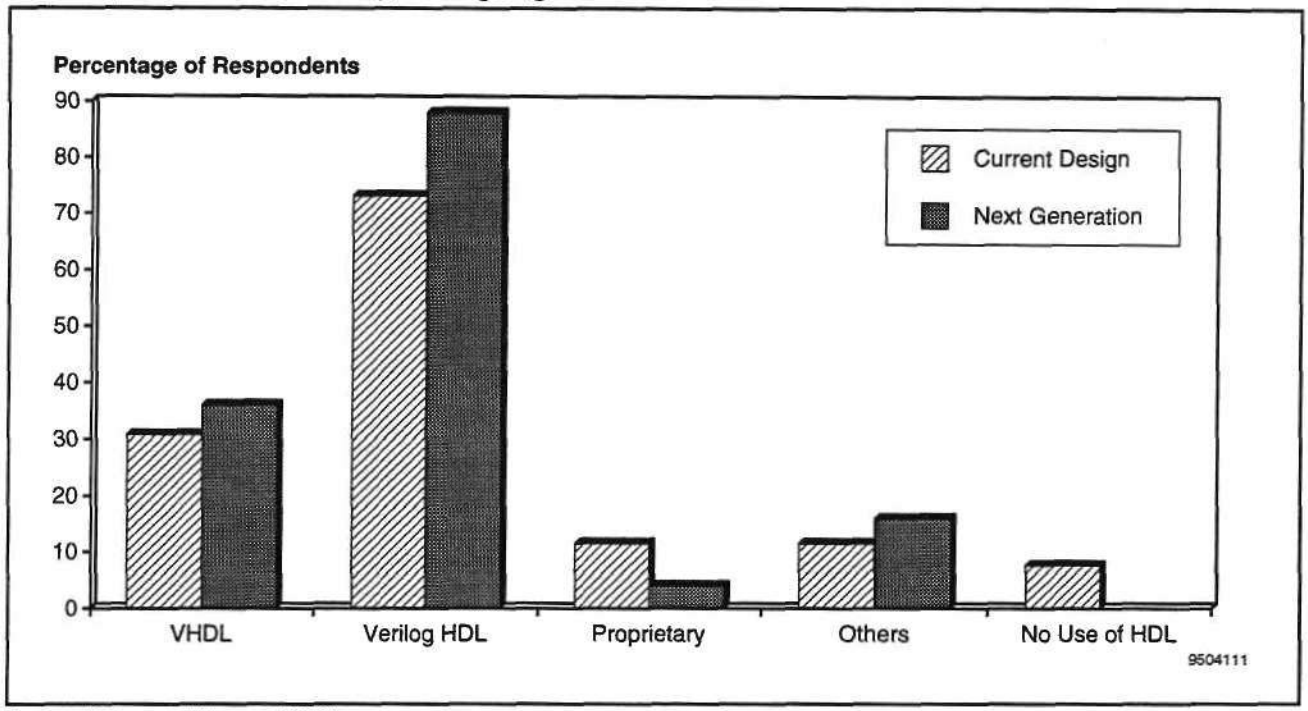
While the press has reported orders for set-top boxes at up to 500,000 units, nearly 50 percent of designers in this category indicated that their products shipped in volumes at or less than 10,000 to date. The set-top box market is in its infancy, with vendors introducing and testing many competing models. Boards in this category average 4.4 signal layers for the current designs and are expected to incorporate five signal layers in next-generation designs.

ASIC testing by partial scan grew nearly 27 percent between current and next-generation design. However, there was a price paid: Full scan lost some popularity in the trade, losing one percent for each one percent gained by partial scan. Next-generation ASIC testing will be 40 percent by full scan and 55 percent by partial scan. JTAG penetration was also on the rise. JTAG for the board will grow 6 percent between current and next-generation design, moving from over 44 percent percent to 50 percent of respondents incorporating that methodology.

Like multimedia designers, set-top box designers claimed to be Verilog champions. Both Verilog and VHDL usage is expected to increase for next-generation designs; however, use of Verilog is double that of VHDL for current and next-generation design (see Figure 4-1). Seventy-three percent of respondents indicated that they used Verilog for current generation design, while 88 percent would use it for next-generation design, an increase of 15 percent. VHDL usage starts from a much lower base and is also slated to increase, but moves only 5 percent, from 31 percent to about 36 percent. This would suggest that some design teams used both languages for current design, a trend Dataquest expects to increase. Additionally, the number of designers reporting that they would not use an HDL sank to near zero.

Though similar to the multimedia market, the set-top box arena differs in some key aspects. First, the high number of competing architectures and overall lack of consumer buying has kept set-top box design in a state of innovation. Home trials represent a form of prototyping, even though actual orders can reach into the tens of thousands of units or more. Similarly, broadcast standards and signal composition have not been standardized, forcing designers to experiment with numerous incompatible solutions.

Figure 4-1
Set-Top Box: Use of Design Languages



Source: Dataquest (August 1995)

Dataquest asked users to report the factors determining market success in this volatile market. Reducing cost was the No. 1 success factor (see Figure 4-2), unsurprisingly. After seeing the troubles encountered by high-cost video games and reviewing the survey results showing that consumers were sensitive to price, designers decided to heed the low-cost mandate. The second most important factor identified was increasing functionality. This is also expected, because the feature set may require not only such high-level features as video on demand, but also other background functions such as customer verification, billing/accounting, and channel locking, blocking, and filtering. Reducing time to market came in a close third and is clearly important for a market built around pioneering companies with the potential for hundreds of millions of customers.

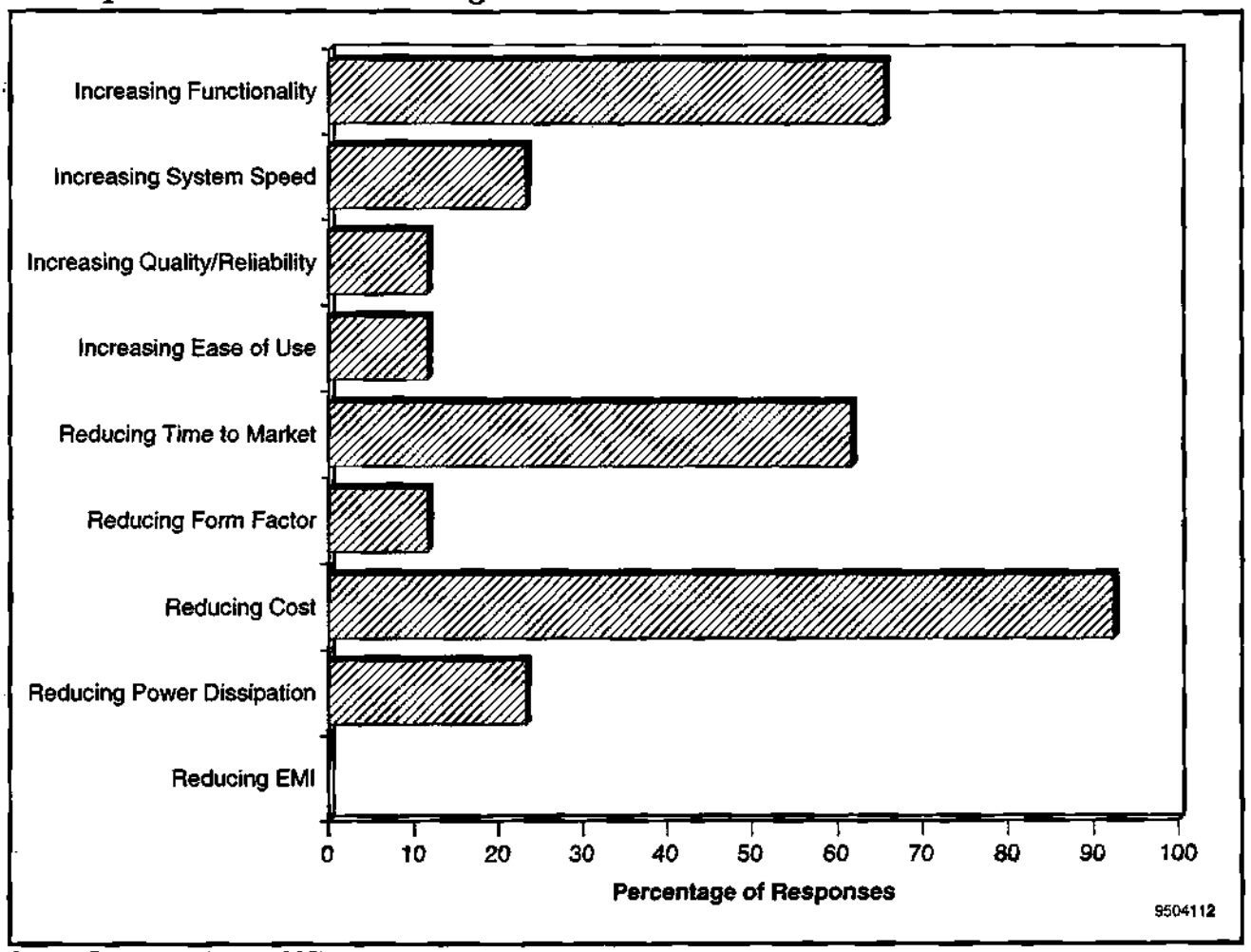
Device Trends

Gate Array and CBIC

Although not in an explicitly tight-margin business, set-top box designers must still provide feature-rich products quickly and economically. The cost and functionality requirements favor cell-based ICs and a lower design rate, while time-to-market pressures favor gate array design. As a result, designers are forced to take a close look at the costs and benefits of each technology and the life cycle of the products.

Set-top box applications in 1995 are expected to reach 43,000- and 105,000-gate counts for gate arrays and cell-based ICs, respectively. Gate array designs have historically provided quick time to market and have been especially useful for products with short life cycles. Cell-based design, however, is quickly becoming the only choice for implementing

Figure 4-2
Set-Top Box: Factors Determining Market Success



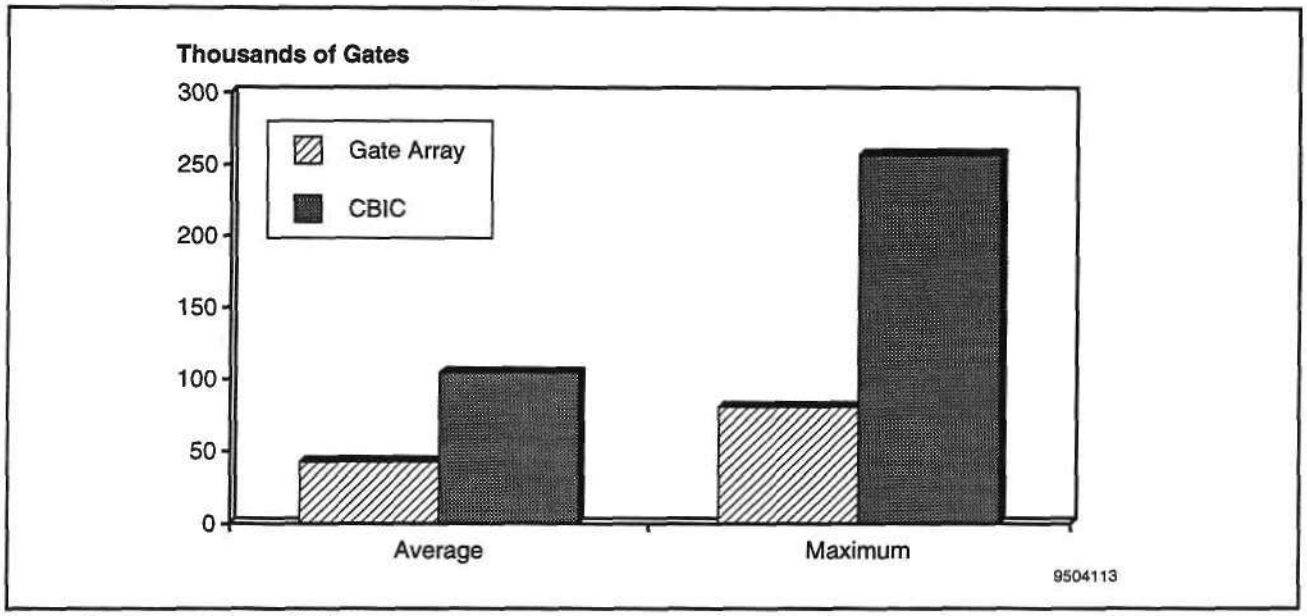
Source: Dataquest (August 1995)

timing-critical functions that cannot fit using a randomized logic approach. Figure 4-3 shows that set-top box designers have a dual technology preference: gate arrays for lower-density designs and cell-based technology for high-density solutions. While the average gate counts are high, the distribution (see Figure 4-4) makes it clear that a solid group of designers is creating high value-added at high densities – greater than 100,000 gates. Other designers continue to create ASICs that fit the traditional curve.

Cell Usage

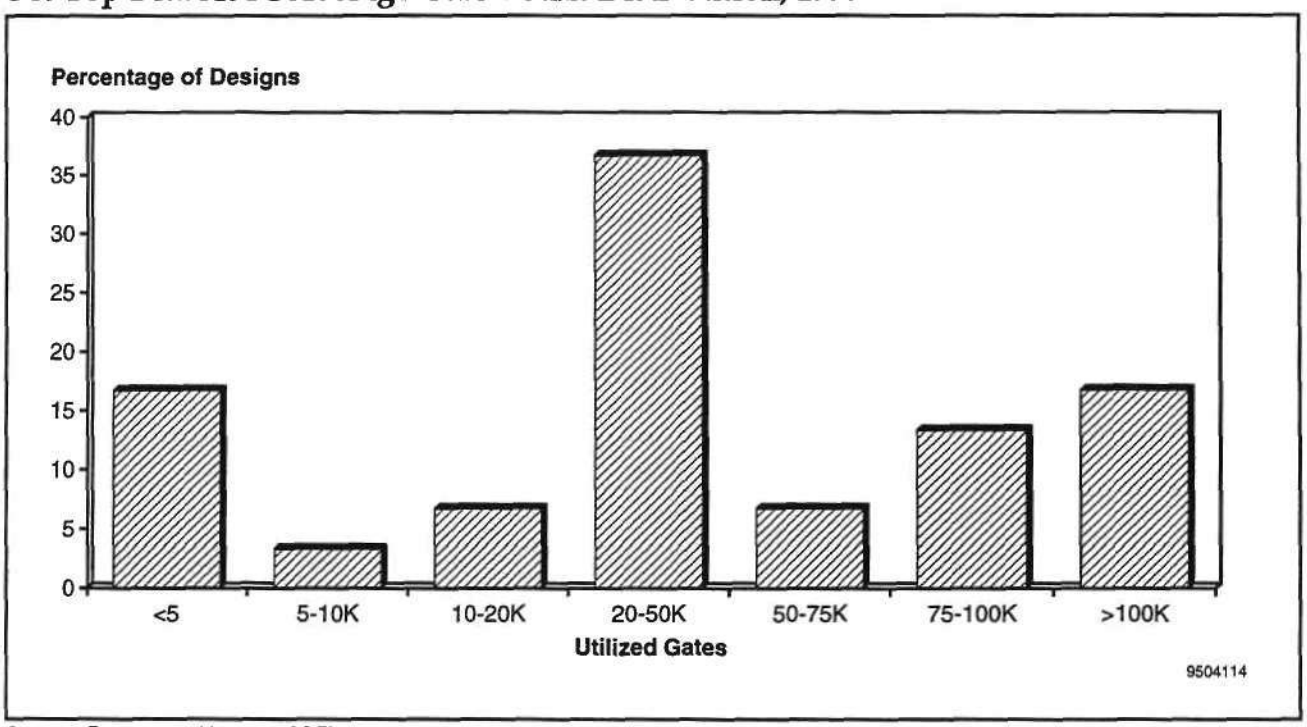
As a result of the increasing functionality required for set-top box designs, cell usage has been on the rise for both gate array and cell-based set-top box ASICs. Figure 4-5 (note the high microprocessor numbers) shows the respective cell usage in both gate arrays and CBICs. As in multimedia designs, there is heavy use of RAM and scan path test in cell-based designs. Optimized memories continue to play a critical role in functionality and die size savings. Similarly, high-speed memory is most efficiently implemented as compiled cells in CBICs or embedded gate arrays. Another important component of these systems, evident in users' responses, is DSP functionality. DSP functionality has been available as an

Figure 4-3
Set-Top Box: ASIC Gate Counts, 1995



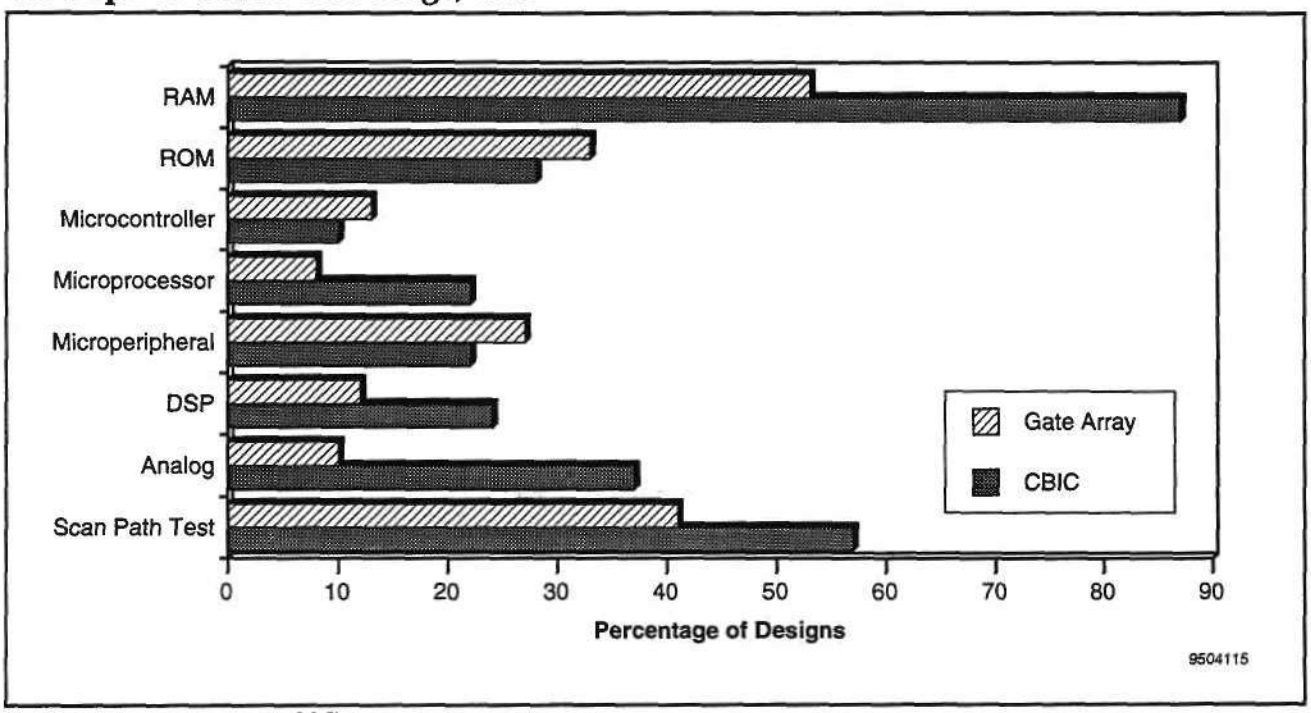
Source: Dataquest (August 1995)

Figure 4-4
Set-Top Box: ASIC Average Gate Count Distribution, 1995



Source: Dataquest (August 1995)

Figure 4-5
Set-Top Box: ASIC Cell Usage, 1995



Source: Dataquest (August 1995)

external (separate chip) solution. However, high-performance systems will bring this functionality on chip to eliminate off-chip delay and to localize such functions as FM, wavetable, and waveguide synthesis. Overall, the inclusion of specialized cells has played an important role in driving gate counts upward for both gate array and cell-based designs.

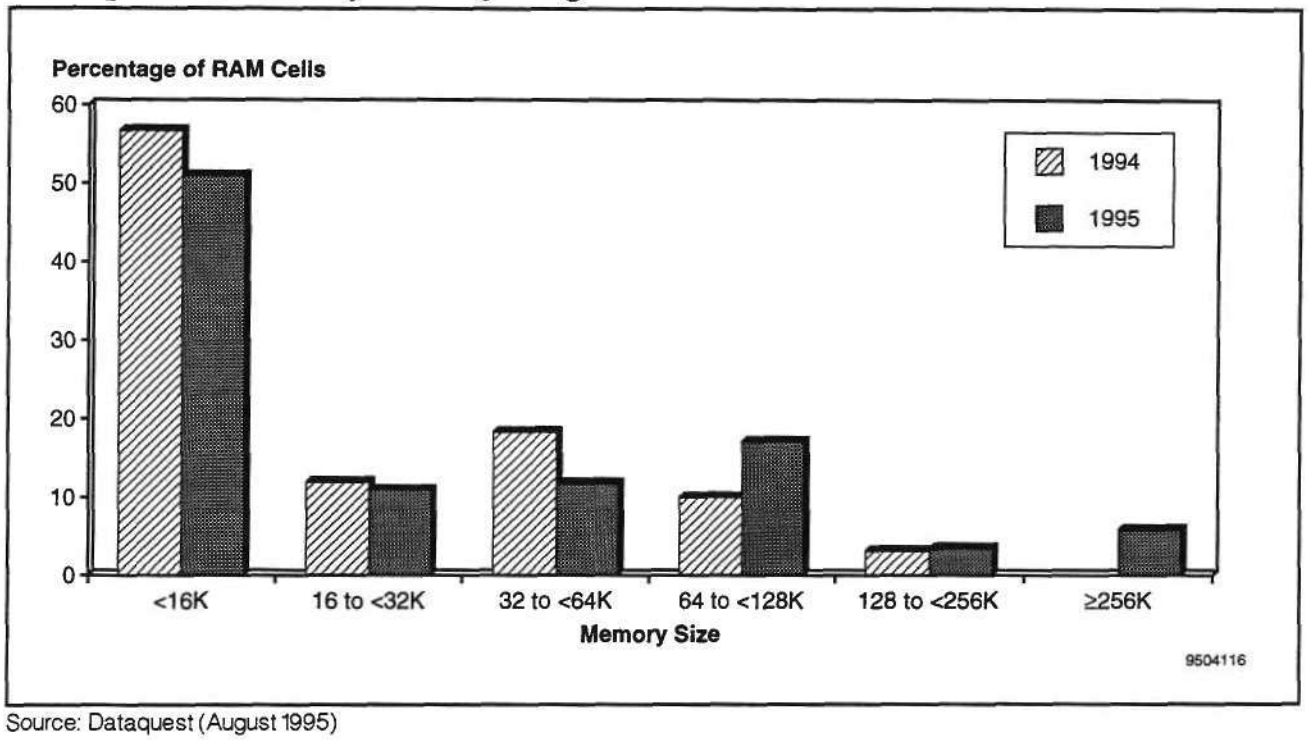
Memory Usage

On-chip RAM has become more and more important as system-level integration becomes a reality. In fact, the dynamics and importance of RAM usage for both gate arrays and cell-based ICs is increasing not only in terms of percent of designs, but also in terms of total memory bits used. Figure 4-6 takes a brief look at the total memory bits in gate arrays for 1994 and 1995. One noticeable trend is the movement of the high-end total memory usage peak, which shifts from the 32- to 64Kb range to the 64- to 128Kb range between 1994 and 1995. In 1995, set-top box designers expect to use over 256Kb of memory on chip, most likely by the addition of extra large memory blocks.

Clock Frequencies

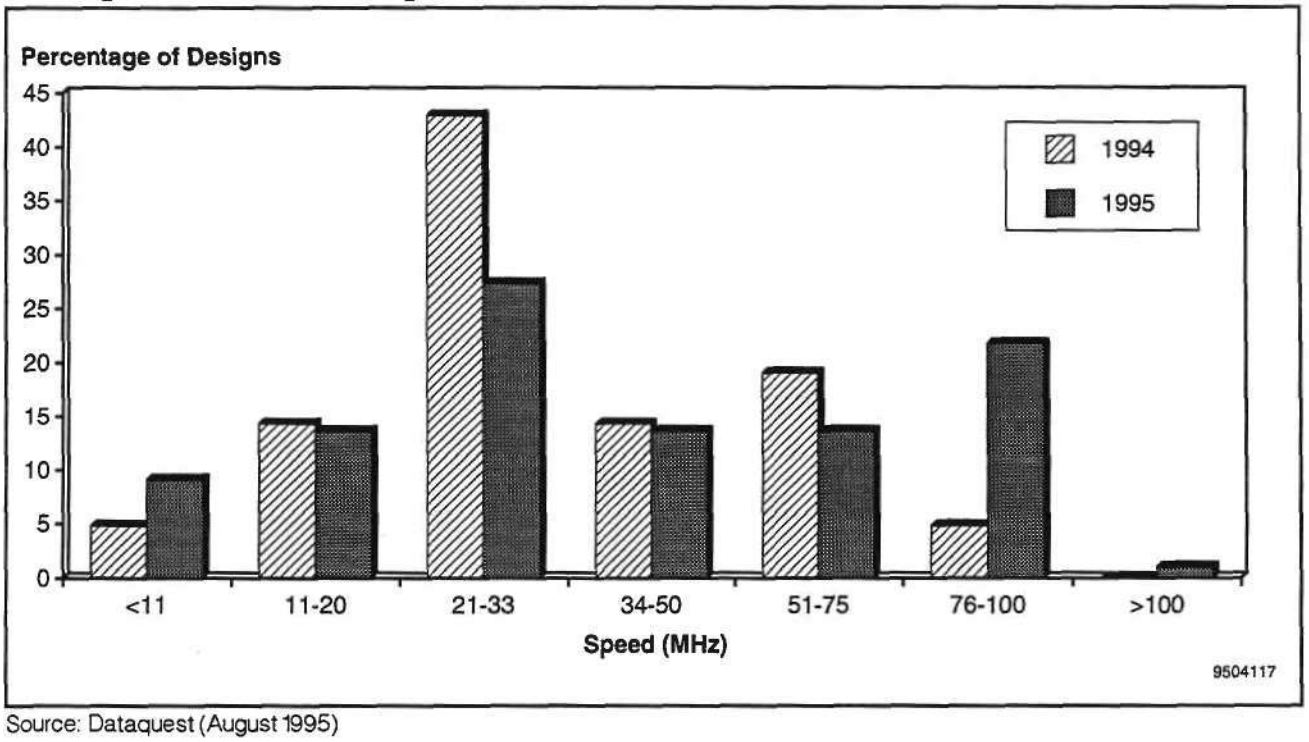
One question of interest to industry watchers is the motherboard of the set-top box. Will it be a PC-type board or will a whole new standard be developed? Dataquest examined the ASIC clock frequencies to be supported by this board. Set-top box designs for 1995 clocked in at an average of 47 MHz. However, clock frequency distribution tells a different story (see Figure 4-7). The majority of designs in 1994 fell into the 21- to 33-MHz range, probably built around the familiar 33-MHz technology that has been around for years. Designers planned to change that in 1995, extending ASIC speeds up to the 100 MHz realm, clearly suggesting clock

Figure 4-6
Set-Top Box: Gate Array Memory Usage



Source: Dataquest (August 1995)

Figure 4-7
Set-Top Box: ASIC Clock Speed Distribution



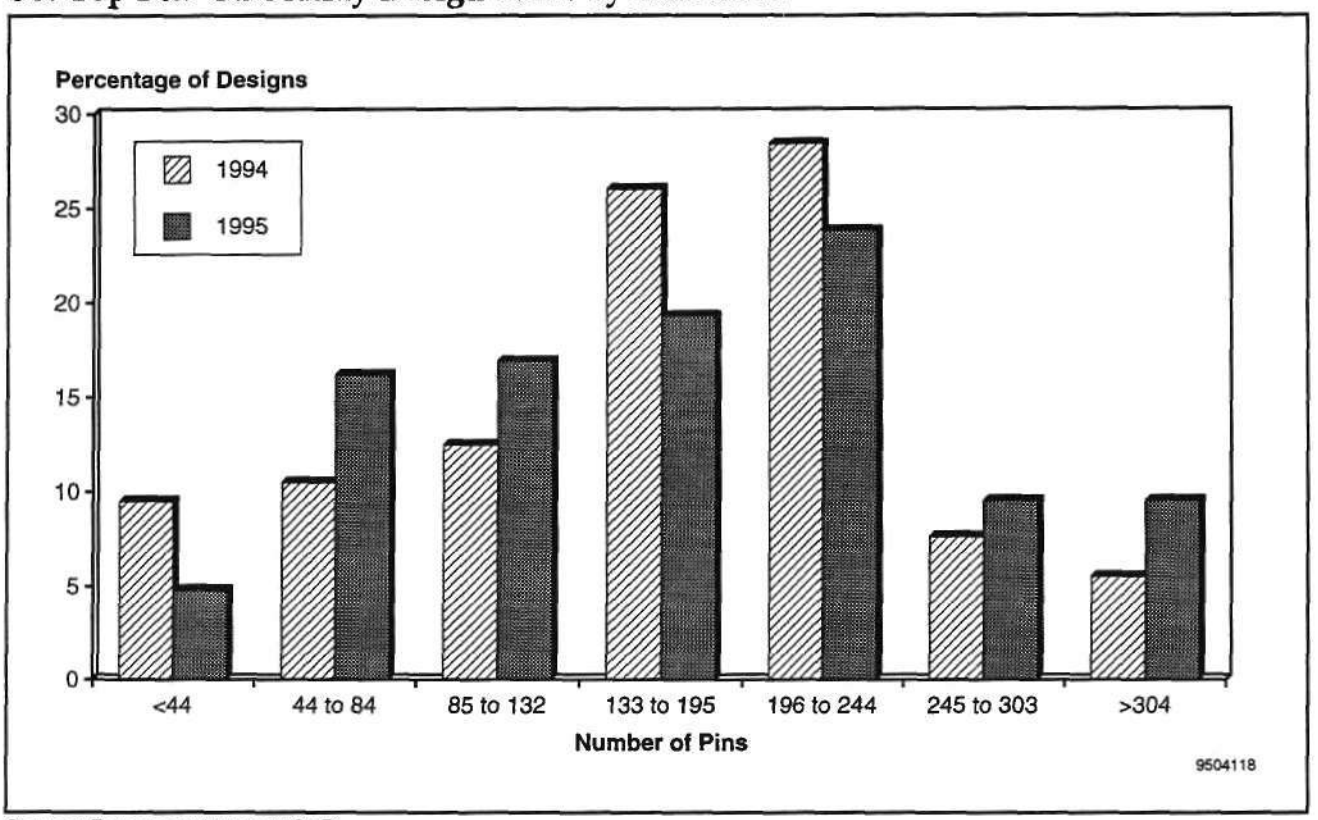
Source: Dataquest (August 1995)

doubling and tripling mechanisms to boost overall system speeds. The bulk of designs in 1995 still lie in the 21- to 33-MHz range, with the greatest design start growth in the 76- to 100-MHz range.

Packaging

The emerging set-top box market has very few standards, as companies continue to disagree as to what final designs will look like, what functions they will perform, and how much they will cost. There are many other issues on the table, too many, in fact, to enumerate in this report. However, this moving target does affect the silicon inside. Semiconductor technology in first-generation systems was often (though not always) proof of concept. As a result, many standard parts in standard packaging were used. The coming generations, and those already in existence, go beyond "can it be done," into the realm of "let's make the best one." However, price and cost-effective packaging are significant issues. As in multimedia, PQFPs, PLCCs, and BGA all played important roles, representing 49 percent, 16 percent, and 6 percent of design starts, respectively. Pin counts, which greatly influence cost and available bandwidth, are also important. Figure 4-8 shows gate array design starts by pin count, demonstrating that high I/Os for set-top box designs are growing in importance. Nearly 20 percent of design starts for 1995 are in pin count ranges higher than 245 pins.

Figure 4-8
Set-Top Box: Gate Array Design Starts by Pin Count



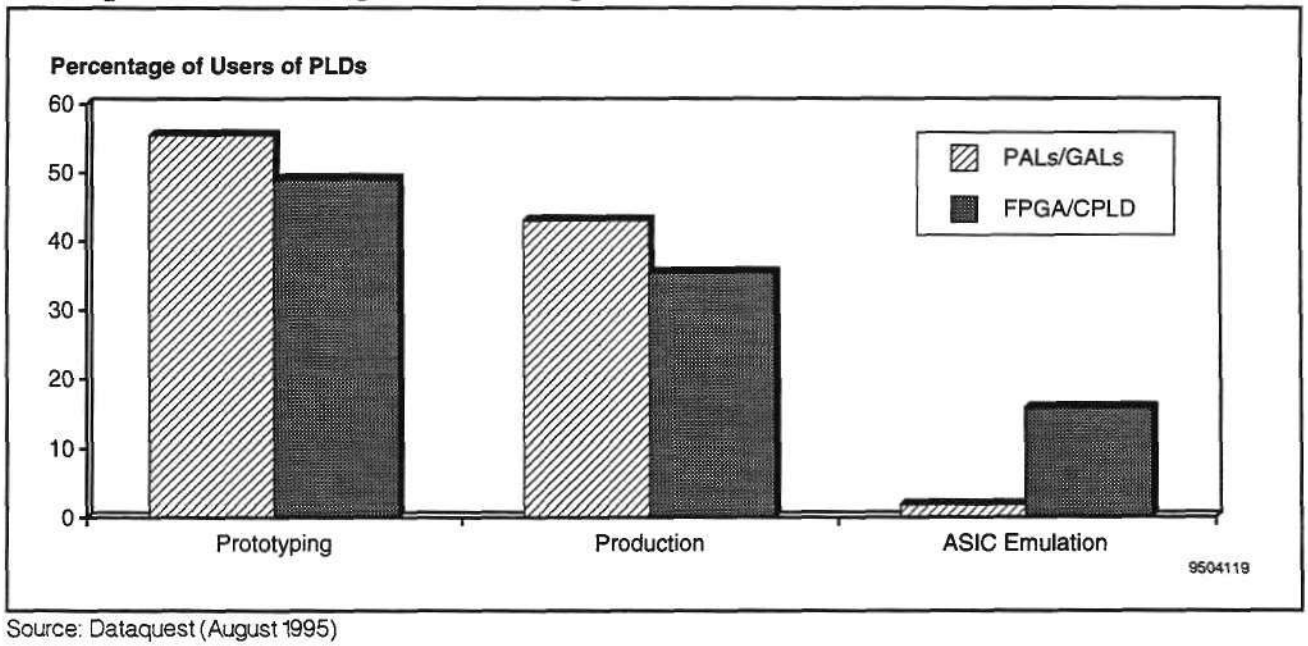
Source: Dataquest (August 1995)

Programmable Logic

The emerging set-top box market still faces with many hurdles, as competing alliances fight to create the de facto standard. As described earlier, the plethora of competing architectures, multiplied by the number of content providers, results in a confusing, yet lucrative market for the company with the winning design. These factors, coupled with the low volumes likely and the flexibility the market requires, would favor a programmable logic solution.

At the same time, however, the elusive price point puts pressure on designers to make the set-top box as economical as possible. These competing factors are reflected in designers' responses about using programmable logic. Both simple PLDs and high-density PLDs (CPLDs and FPGAs) found high usage in the design phase, with at least 50 percent of designs incorporating either form of programmable logic. CPLDs and FPGAs also found significant use in ASIC emulation (see Figure 9). Their use in production is somewhat lower than the all-application average; again, this is the result of pressure to keep the system price low.

Figure 4-9
Set-Top Box: Use of Programmable Logic



Source: Dataquest (August 1995)

Chapter 5
Conclusions

Dataquest Perspective

The movement toward system-level integration (SLI) is occurring across many applications markets. In the silicon world, the development of function-specific building blocks continues to meet the needs for the growing feature set demanded by next-generation design. This trend has been a crucial factor for multimedia, one of the first real applications to benefit from the new design methodology of system-level integration. The route toward SLI maps four main groups:

- Group 1 consists of groups of individual chips.
- Group 2 puts integrated system functionality on a single chip.
- Group 3 is Group 2 design optimized with concurrent processing and hardware-software co-design.
- Group 4 is Group 3 design exploiting capabilities of device physics for performance.

Group 1

In the beginning, most critical features were independent solution pieces (chips) scattered around a board or add-in card. Next, ASIC methodology from suppliers combined two or more features to provide a cheaper, integrated solution. Two-function integrated circuits quickly became standard for suppliers, and the competitive advantage was again diminished. This process continues, and today we have graphic and video subsystems comprising multiple chips, with each chip providing a unique function, multiple functions, or sharing a dedicated function with other chips. This multiple-chip solution is Group 1 multimedia silicon. This capability is provided by the ability of ASIC methodology to create both chipsets and custom ASICs. The same trend will continue, with the market again seeing a herd of newer designs combining the last year's four-chip solutions into two- or three-chip solutions with a few new, added features.

Group 2

The model keeps on churning, however, and companies with large investments in cell libraries, synthesizable cores, and intellectual property have been proving that providing more than just "me-too" solutions can reap big rewards in profits and public perception. These same companies will be in a good position to take those two- or three-chip solutions and integrate them into a single chip. It is old news that memory, logic, and a 286 processor can fit on a single chip. Today's news is that vendors have already delivered silicon with three processors and support logic on board that can perform motion JPEG, texture mapping, CD-quality sound, and parallax scrolling, all for an estimated cost of less than $30. These chips now provide system-level integration by incorporating processing, memory, and system logic on a single die. This is Group 2.

MPEG 2 decoders are being announced almost faster than new car models, but, again, the truly innovative will take the next step and combine that core with other functionality to provide integrated high-performance

solutions. Vendors may be able to address this by supplying not only the MPEG core, but also competing cores such as DigiCipher II. Such integration allows the end system to process bit streams from content providers using either encoding scheme. System-level integration is no longer a distant possibility, and multimedia ASIC solutions have been and will continue to be the first benefactors of this technology.

Group 3

Along with this trend toward integration, running up the clocks will not necessarily be the panacea for increased performance. Smart designers will increasingly look for creative ways of implementing new algorithms. One such direction is concurrent processing, often implemented through parallelism. It is no coincidence that this is the same direction that microprocessors and data processing in general have taken. Concurrent processing of data streams will extend current board technology, while increased parallelism, clock multipliers, and dedicated execution units become more prevalent. The chip in the example in Group 2 reportedly processed 200 mips while running at below 35 MHz.

Future systems will take SLI to the next level: hardware-software co-design. With careful planning and design simulation, an optimum balance of hardware and software code execution can again increase system performance. These systems, which will include massive integration, concurrent processing, and hardware-software optimization, can be called Group 3 multimedia ASICs.

Group 4

Even further into the future, process technology will be enhanced further to allow CMOS processing speeds to exceed current ECL capabilities. Combine improved clock rates with the Group 3 products, and realism levels will meet and eventually exceed those of Silicon Graphics' Reality Engine 1. This performance would represent Group 4 multimedia ASICs.

The road to Group 4 functionality is long and rocky. Not only does the road map suggest that hardware designers must give up some of the crown jewels of design, but it also suggests an even greater dependence on software engineers.

The Beginning of the End of Multichip Solutions

The time-to-market, cost, form factor, and functionality requirements of next-generation multimedia and set-top box systems will make it harder and harder for multichip solutions to compete. In the video game arena, the press has focused on the processing engines of the Sony Playstation and Sega Saturn. Comparisons between the Playstation and Saturn amount to comparisons between the custom ASIC processing engine and standard processors and have focused on the quality of experience, where Sony's box appears to have an advantage. System specifications of the two suggest that the Sony engine may, in fact, cost less, yet provide equivalent or greater performance and functionality. The Sony engine is not a standard product and is unlikely to become one, because the integrated solution provides Sony with a cost and technology edge that translates into competitive advantage. The success of this design, however, lies in the ASIC cells of the ASIC supplier's libraries and the skill used in stitching

them together. While the actual design may remain proprietary, the technology can be leveraged to standard products or other ASIC solutions.

The capture of future ASIC and standard product designs is made possible by reusing cell libraries, especially those key elements that have been proven in the field. The resulting ability to pick and choose the desired functionality can allow system manufacturers to differentiate their products and earn increased margins. The resulting profits can then be reinvested in design technology to allow the OEMs to focus on design for competitive advantage. The competing model of manufacturing muscle to compete on price guarantees only low margins while ignoring the importance of system knowledge.

In conclusion, Dataquest believes that the era of system-level integration has begun, and suppliers and users need to understand the implications. As system design moves to the next generation, expect single-chip solutions to incorporate the following features: many system function blocks stitched together, taking advantage of wide buses and concurrent processing; high clock rates; and application code optimized to the chip architecture. The ASIC market is going through a major transformation, and Dataquest will track it as it happens.

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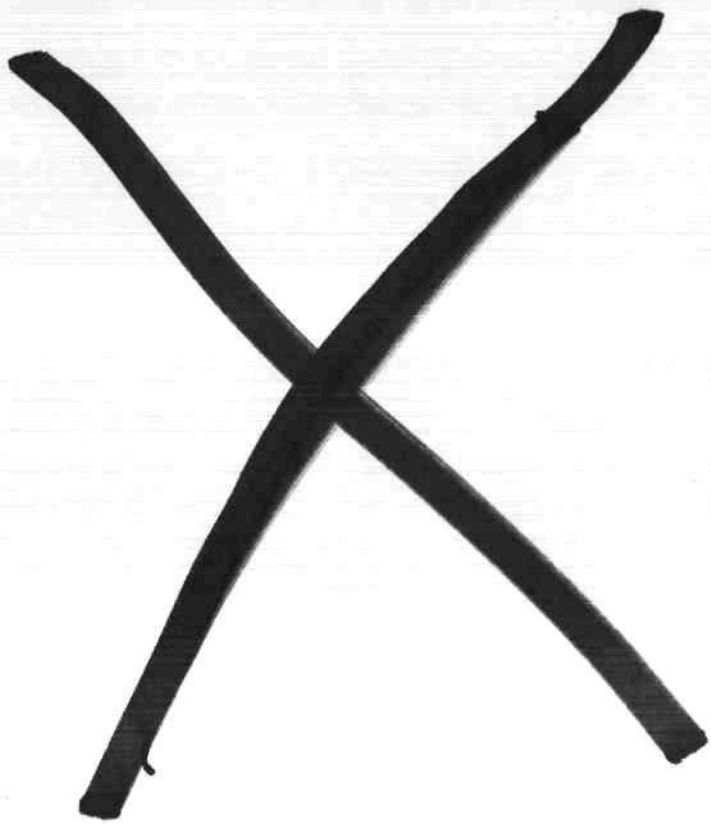

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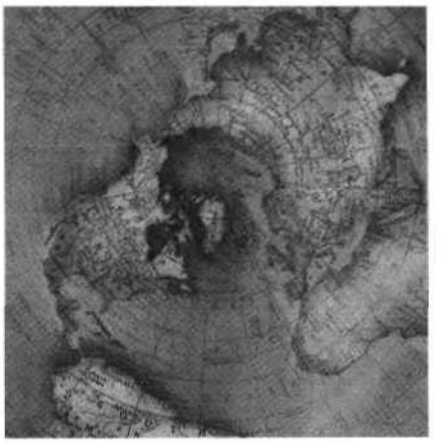

Dataquest

Systems Designers Uncover ASIC Opportunities

User Wants and Needs

Program: ASICs Worldwide
Product Code: ASIC-WW-UW-9501
Publication Date: June 26, 1995
Filing: User and Distribution Studies

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Chapter 1
Executive Summary

Dataquest believes that if companies are to be successful, they must have a thorough understanding of their target customer base as well as their system design requirements. The purpose behind Dataquest's User Wants and Needs studies is to provide our clients with the most in-depth, up-to-date information on electronic system design. Dataquest's ASIC Worldwide Service extensively surveys designers of electronic products and reports on their shifting priorities, desires, and demands, providing a valuable snapshot of user trends.

This year, the survey process was modified to enhance the value to Dataquest's client base. First, coverage was extended to cover three regions: North America, Japan, and Europe. Second, new questions were added to answer common requests. These included questions about the amount of memory use on chip, which processor cores were being implemented, and the degree of programmable logic device (PLD) implementation. With these modifications, the new survey received nearly 700 responses.

ASIC User Wants and Needs report *Systems Designers Uncover ASIC Opportunities* is one of a series of three reports: North America and Japan User Wants and Needs, a vertical markets Focus Report, and a European ASIC Focus Report. These reports are intended to be used by business executives to identify significant trends in electronic system design and explore potential target markets for ASIC devices.

Report Structure

This report, focusing on North America and Japan, is broken into seven main chapters with each investigating a particular aspect of ASIC and electronic system design. It begins with an executive summary that includes an overview of the major findings.

Chapter 2 explains the research process Dataquest employed in gathering the information and the demographics of the survey respondents. Demographic breakdown includes respondents by job title, respondents by project team, and project team profiles.

Chapters 3 and 4 delve into system design trends and issues for North America and Japan, respectively. Critical factors for market success, signal layers, and use of hardware description languages (HDLs) are only some of the topics covered.

Chapters 5 and 6, the core of the book, shed light on the ASIC products being designed into systems in North America and Japan, respectively. ASIC users vote on the gate counts, speeds, and packaging they will need for their next-generation system design. These chapters cover gate arrays, cell-based ICs (CBICs), and programmable logic (including field programmable gate arrays).

In the final chapter, Dataquest explores the major findings from this research and makes recommendations to both ASIC suppliers and ASIC users.

Major Findings

Our research of ASIC and systems designers provides an insightful look into their preferences and consumption patterns. Major findings from the survey include:

- Cost is the dominating success factor.
- Cell-based designs are on the rise.
- On-chip memory and microprocessors contribute to functional density.
- Ball grid array (BGA) packages are gaining significant momentum.
- Pure 3V technologies are rapidly on the rise.

Reducing cost beat out all other success factors to remain the No. 1 factor determining market success. Dataquest's last survey in both North America and Japan found that time to market, reducing cost, and increasing functionality were common leading success factors, with reducing cost commanding the lead for both regions, especially in Japan. Results from our new survey suggest that success dynamics have not changed much. Reducing system cost turned out to be the leading success factor by a margin of 6 percentage points in North America and by 25 percentage points in Japan.

As the cost factor takes center stage, the data revealed that the traditionally lower-cost ASIC, gate arrays, were being sacrificed for the lower-piece-price CBICs. One of the major shifts, evident in Chapter 4, is the large growth in design densities. Designers have responded that they are following a density map for gate array and cell-based designs. As designers suggest in early chapters, gate arrays will dominate the low to midrange density designs, while CBICs capture more designs in the more-than-100k gate range. The switch to cell-based not only affords greater cell reuse for the consumer designs, but also gives them density and die size benefits—which also bring down the total cost of design. In fact, data in Chapter 5 will show that maximum densities for cell-based designs average nearly twice that of gate arrays. Users reports average maximums for data processing at around 250,000 gates, communications at around 230,000 gates, military at over 220,000 gates, industrial at close to 150,000 gates, and consumer at over 270,000 gates.

What makes these high-density designs feasible for CBICs is the stitching together of functional cell blocks. By placing and connecting functional blocks and megacells, designers can quickly provide the desired functionality while quickly boosting gate counts. Thus, cell libraries become the remaining differentiator in the cell-based arena.

One cell used in CBICs and gate arrays is memory. The new research in this year's survey indicated that the most designs used less than 16Kb of total memory. On the other hand, memory use is growing, and designers in both regions reported that memory use in general and even total memory bits larger than 128Kb are also on a healthy ramp. The implementation of such large amounts of memories will require optimized memory cells for both the cell-based and embedded array designs. Another implementation (that is, traditional arrays) will severely inhibit design efficiency

The design and implementation of megacells is also gaining importance. Beyond the use of large memory blocks, Dataquest added a question investigating the implementation of microprocessor cells. Users indicated that microprocessor cell use was an integral part of their system design; later information suggested the same for microcontrollers. 68xxx, MIPS, ARM, and DSPs are finding their way on-chip as functional integration collapses the chip count.

Increased functionality and high densities can often translate to more I/O requirements. Combine that with high-frequency switching, and package choice is a major issue. Since cost was a driving factor, the use of 160- and 208-quad flat packs would appear to be the natural choices for cost reduction; however, the high-density designs often require high bandwidth, and the extra-wide buses can push I/Os to the upper 200s and above. Survey respondents suggested that pin counts were rapidly rising and along with it, the use of BGAs in North America. BGAs address many of those problems, and the newer chip-scale versions address associated board real estate issues. Chapter 4 also discusses this further.

The rush to low voltage has become more like a fast walk; thus, ASIC suppliers still must support 5V libraries. Low- and mixed-voltage ASICs are on a design ramp but not nearly as rapidly as earlier believed. No doubt, mobile computing and size-conscious consumer applications have begun to affect the design of today's ASICs and will play a larger role in the ASICs of tomorrow. However, the sluggishness of the peripherals market to adopt low-voltage signaling technology and the economics of 5V DRAMs have kept up demand for 5V ASIC products. As result, designs go where the dollars are, and while low- and mixed-voltage designs are expected to increase, 5V designs still represent the lion's share of activity.

Across the board, from design languages to test issues, through gate counts and clock speeds, opportunities exist for ASIC suppliers to further develop the ASIC market in North America and Japan. The breadth of changes is extremely important to both ASIC suppliers and ASIC users.

In this report, Dataquest highlights the current shifts in the North American and Japanese ASIC markets and makes recommendations on future directions for both ASIC suppliers and users.

Project Manager: Duane Kuroda

Chapter 2
Survey Methodology

Dataquest demand-side, or end-user, data is gathered using extensive survey techniques. End users are identified through a variety of means, including databases of past survey respondents, the registered user and prospect lists of the leading EDA companies, and relevant periodicals. Surveys were distributed throughout North America and Japan, enabling Dataquest to gather a snapshot from a user point of view of the current and future system design requirements and the applications driving ASIC use.

This User Wants and Needs study includes data collected from the North American and Japanese surveys. Surveys were received and processed in the first quarter of 1995 from North American sites and received and processed in the second quarter of 1995 from sites in Japan. The responses to the survey were entered in a statistical package for cleansing and analysis of the data. This statistical database allows Dataquest to cross-tabulate the data for improved analysis. Because of the timing of the survey, the responses are based on sufficient product planning to allow cohesive understanding of both 1994 and 1995 developments.

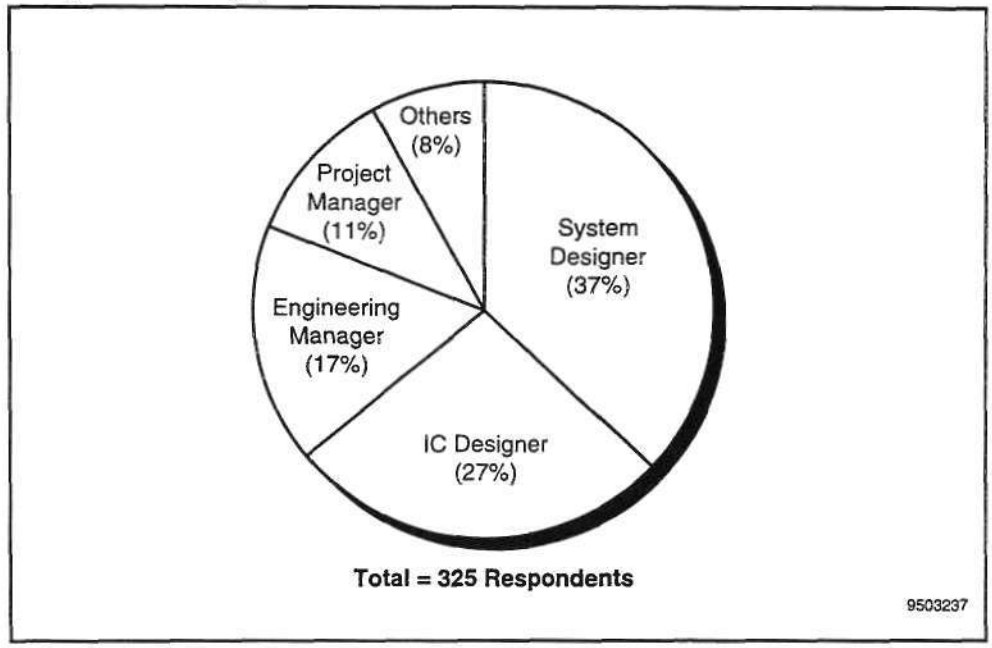
Respondent Demographics

Dataquest strives to gather an accurate representation of the design community, making sure to survey a large cross section of designers. Data collected in North America is predominantly from system design engineers as well as IC designers, making up approximately 64 percent of the respondents. Engineering managers, the next-largest category, provided 17 percent of the responses. Data collected in Japan is split between system design engineers, engineering managers, and IC designers making up approximately 34 percent, 21 percent, and 18 percent of the responses, respectively. Figures 2-1 and 2-2 show the breakdown of respondents by job title. Dataquest believes that the data represents a statistically significant sample to gauge the needs and trends of the electronic system design.

There were 325 survey responses in North America, with almost 70 percent of the respondents from locations with over 100 employees, and about 30 percent at locations with over 1,000 employees. Figure 2-3 shows the distribution of employee numbers at the respondents' locations in North America. In Japan, there were over 225 survey responses, with over 80 percent of the respondents from locations with over 100 employees and about 50 percent at locations with over 1,000 employees. Figure 2-4 shows the distribution of employee numbers at the respondents' locations in Japan.

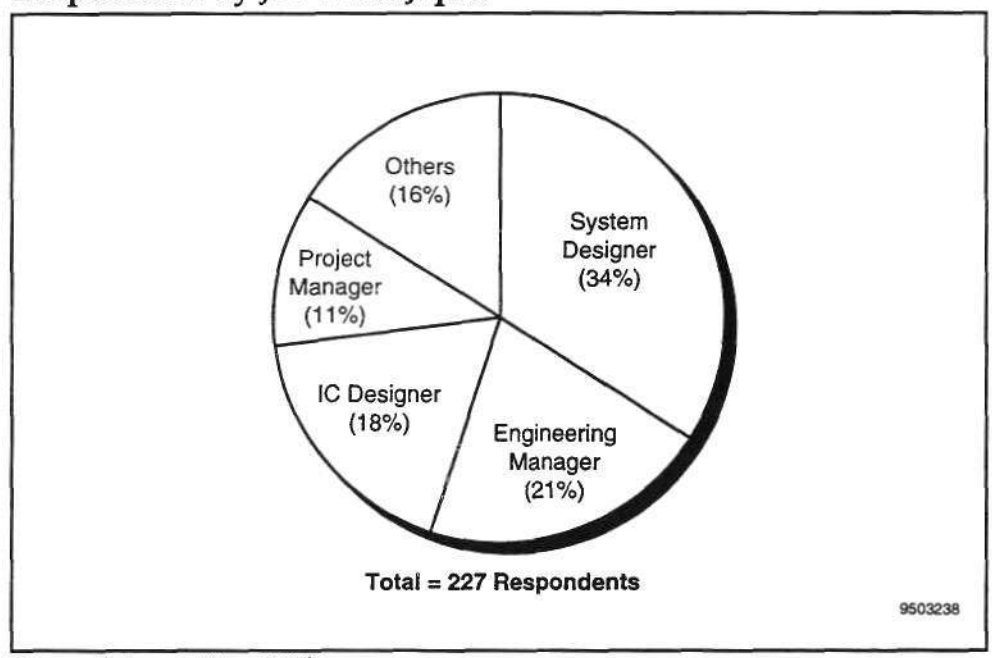
Respondents answered with respect to their project teams. The average project team size was just over 10 in North America, but the size of project teams varied by application market. Figure 2-5 shows the project team size as it varied by general application market. The military designers were clearly pulling the average team size up. In Japan, we saw similar trends (see Figure 2-6).

Figure 2-1
Respondents by Job Title: North America



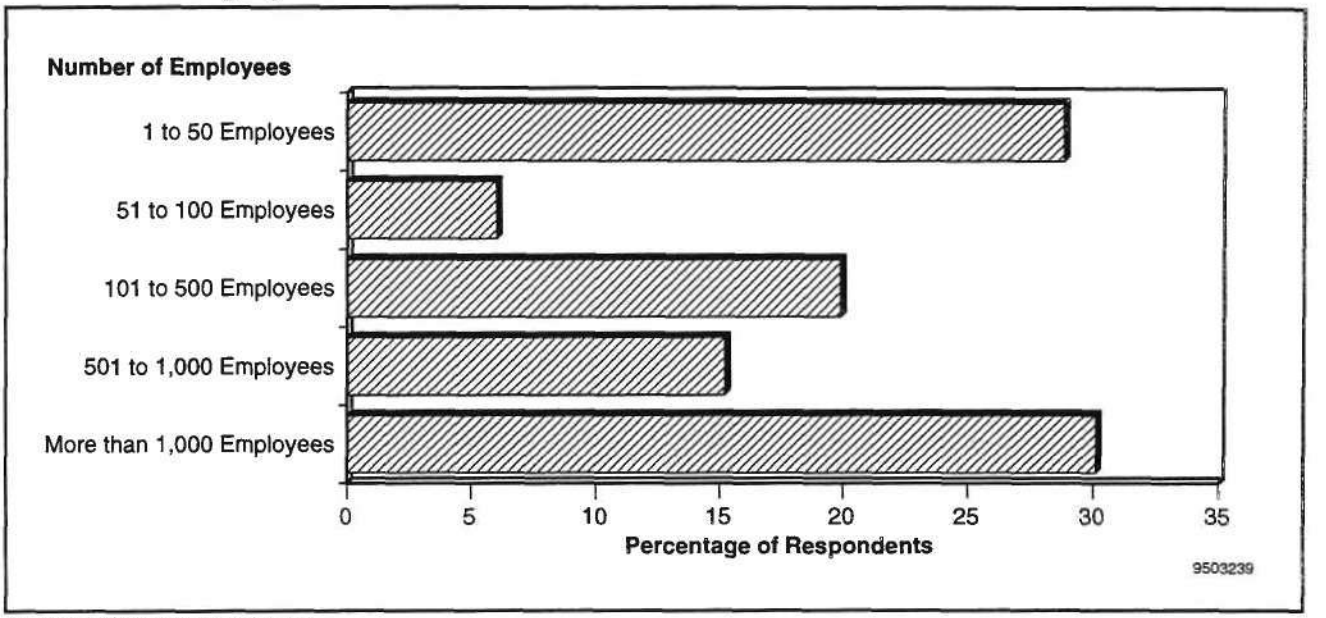
Source: Dataquest (June 1995)

Figure 2-2
Respondents by Job Title: Japan



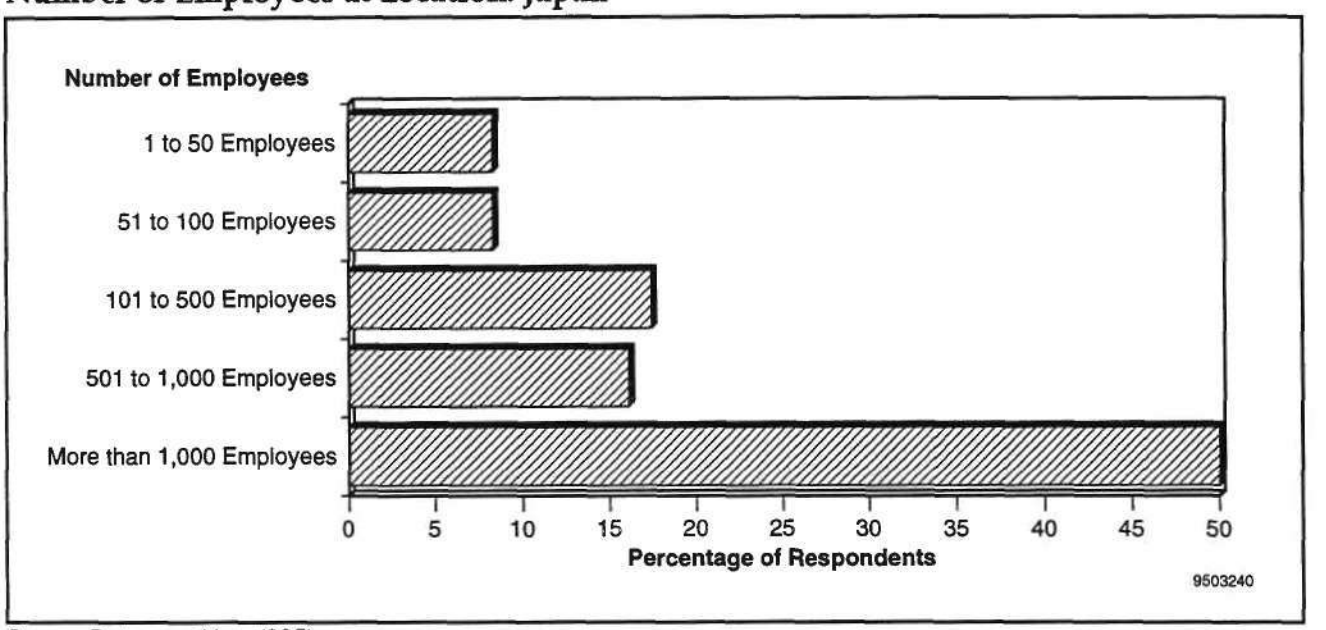
Source: Dataquest (June 1995)

Figure 2-3
Number of Employees at Location: North America



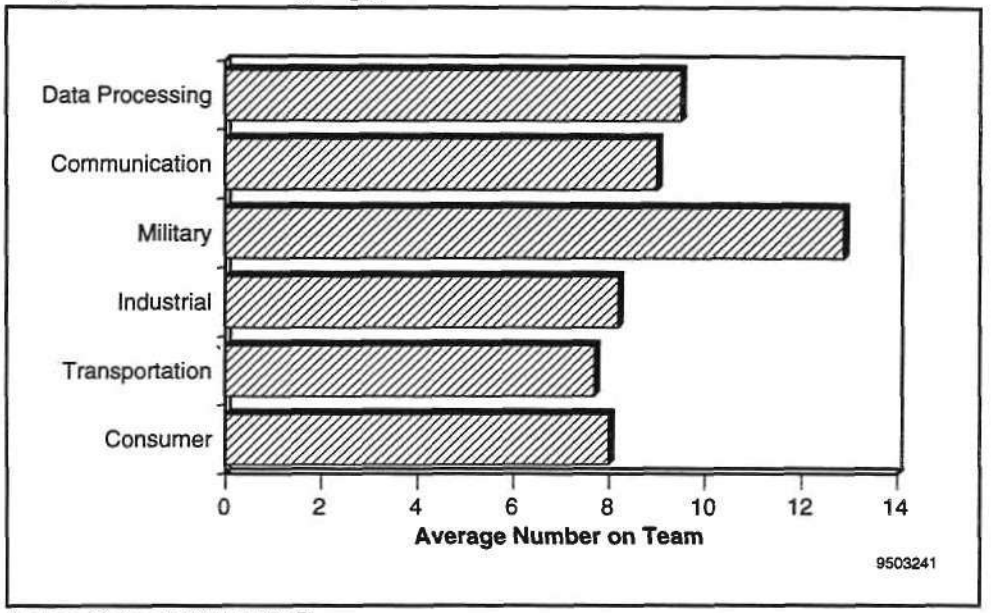
Source: Dataquest (June 1995)

Figure 2-4
Number of Employees at Location: Japan



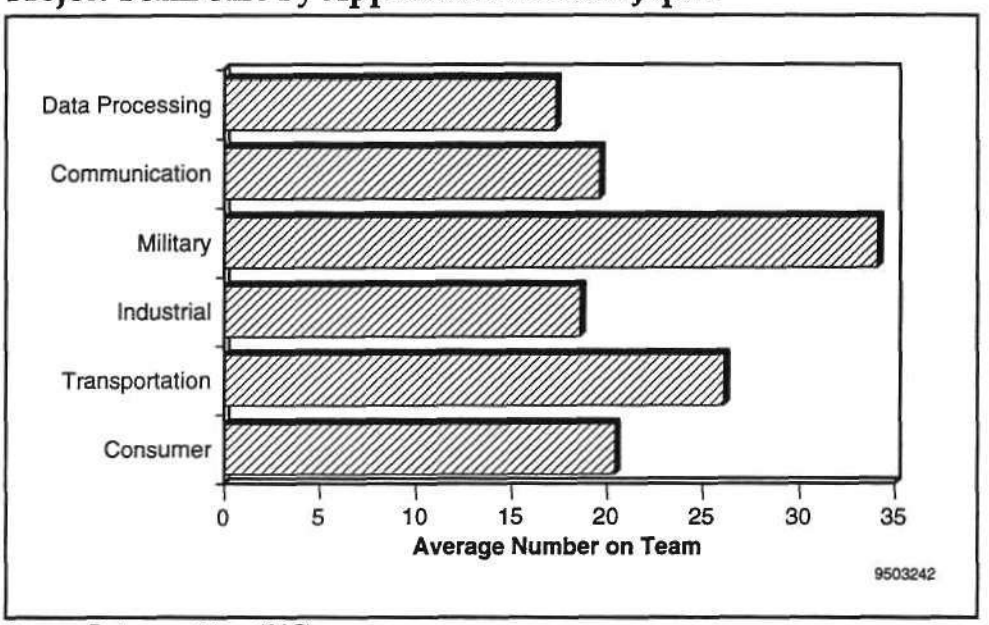
Source: Dataquest (June 1995)

Figure 2-5
Project Team Size by Application Market: North America



Source: Dataquest (June 1995)

Figure 2-6
Project Team Size by Application Market: Japan



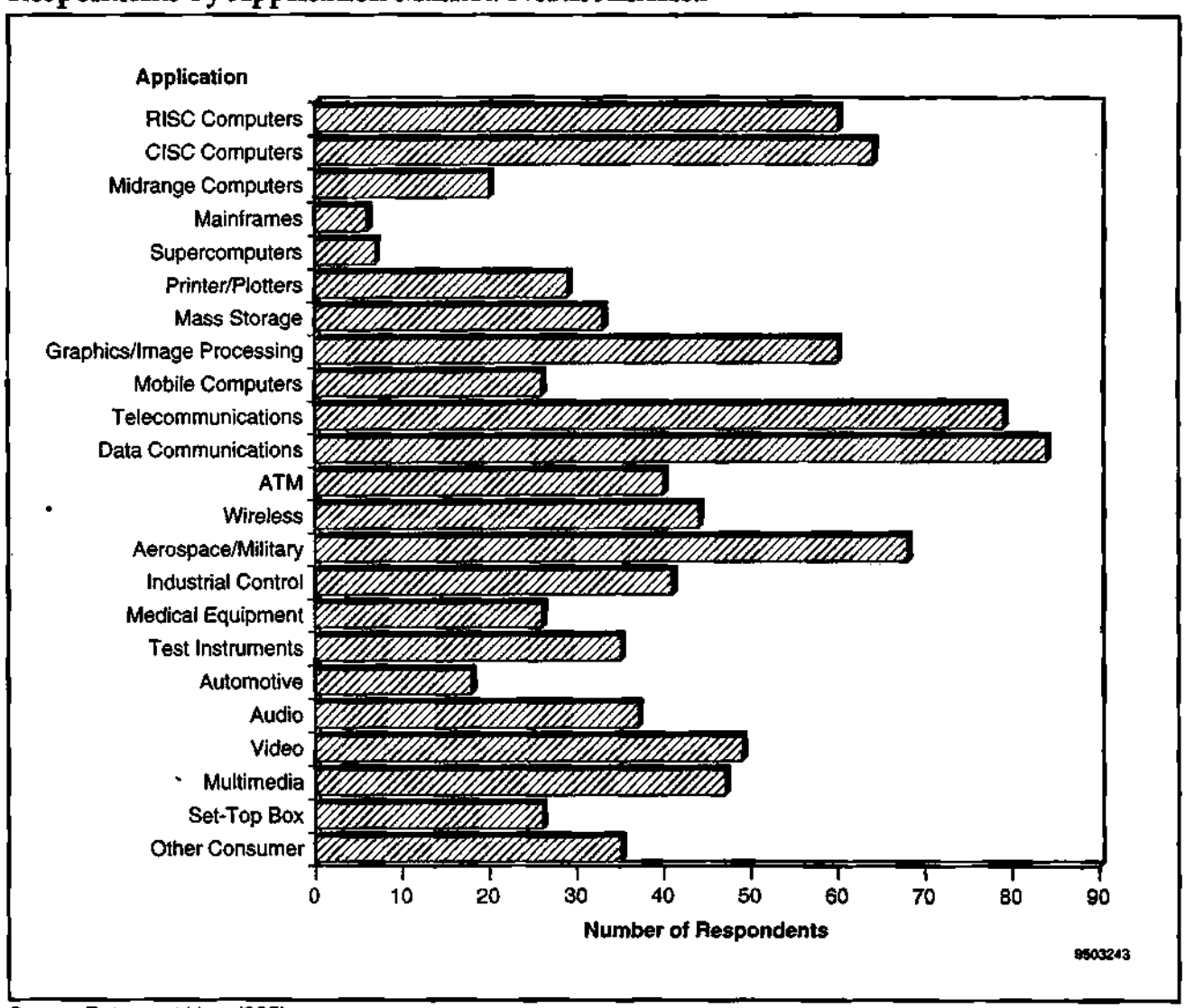
Source: Dataquest (June 1995)

Significant analysis can be derived by examining the types of system designed by the project teams. Figures 2-7 and 2-8 show the primary applications that project team members designed in North America and Japan, respectively.

It is important to note that survey respondents were allowed to check more than one box for their project team's primary line of business. Because of this, certain responses have been classified for more than one application area.

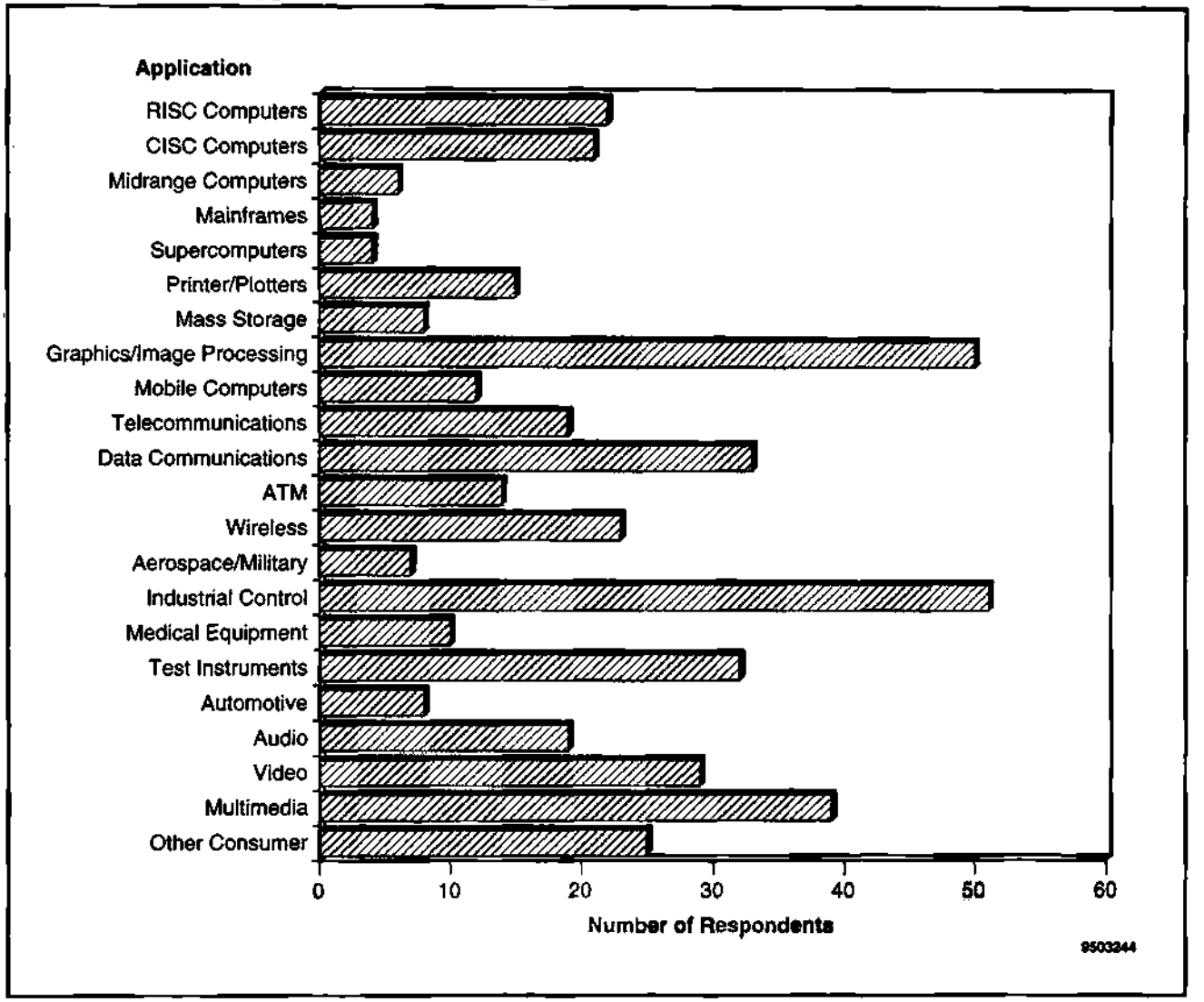
For this year's survey, Dataquest expanded the application coverage to allow designers to more readily describe what applications they were designing. The categories that were added fall into our emerging applications category. These include graphics/image processing, mobile computing, ATM, wireless communication, multimedia, and set-top boxes.

Figure 2-7
Respondents by Application Market: North America



Source: Dataquest (June 1995)

Figure 2-8
Respondents by Application Market: Japan



Source: Dataquest (June 1995)

Chapter 3
Design Trends and Issues: North America

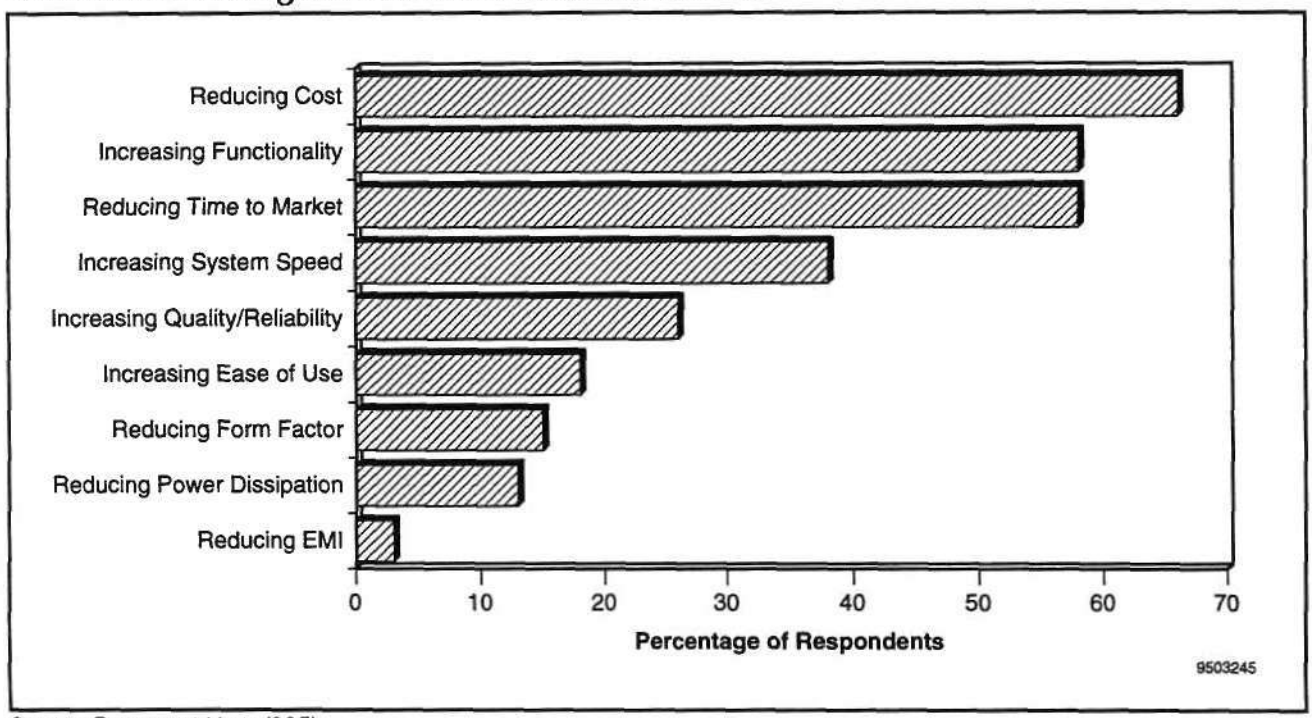
Next-generation product design can be quite complex. The amount of variables that interact can lead to quite a complex model, but those considerations should be addressed after covering other fundamental issues in system design. No one has a better grasp on these issues than the systems designers, so Dataquest asked them to show the way. The key to successfully opening the door to the ASIC market is in understanding how systems designers think and how they build their products. With a better understanding of systems designers' requirements, specific markets can be targeted and penetrated more effectively.

In this chapter, Dataquest analyzes the critical factors that determine success for systems designers, the ASIC design cycle, and the characteristics of the systems designed.

Determining Market Success for Systems Designers

Quantifying the factors that lead to successful products is of critical importance to all companies involved in the fast-paced electronics industry. Not surprisingly, electronics designers are cognizant of the attributes necessary for developing successful systems. Dataquest requested that each respondent select the three attributes most important to their product's future ability to achieve market success. Figure 3-1 shows the most important attributes that lead to market success for systems designers in North America.

Figure 3-1
Factors Influencing Market Success: North America



Source: Dataquest (June 1995)

While the magnitude of the response was varied on an application market basis, the overall results were consistent. The three most important factors were as follows:

- Reducing cost
- Increasing functionality
- Reducing time to market

Reducing cost was the most important success factor. The last time Dataquest surveyed users in North America, reducing cost was the No. 1 driving force, beating out increasing functionality by a small margin. This year, cost reduction maintained a similar lead, while the next two factors, increasing functionality and decreasing time to market, were indistinguishable in the race for No. 2. Increasing speed placed No. 4 as it did in the last survey.

The success factor rankings in North America clearly indicate that cost has maintained its primacy at the forefront of designers' minds and that the other factors form a secondary tier not far behind. The close proximity of the top three factors, however, suggests the existence of a delicate mix in the product development cycle. Failure to pay attention to any of the three could have disastrous effects, though just meeting the requirements does not guarantee success either. Thus it again boils down to value, the meeting of price and functional performance, as the focus for product acceptance.

The importance of cost as the leading success factor suggests that the recovering economy has left purchasers with a jaundiced eye toward the bottom line. A rising consumer index and employment rate has not translated back to rising prices, and it seems that the hardship of the recent recession has left a cost-conscious trend burned into all of our minds. Having it now is still important, but the price still has to be right.

Much talk has been made about the average selling price for computer systems, and time and time again, the figure of $1,500 to $2,000 comes up. But if that is the case, a natural conclusion would be that increased functionality and higher performance were added for free. But before products reach that stage, they must have the right mix of features and performance to migrate down the cost curve to that magical number. Those features then become the selling point for a differentiated product, especially since the efficient market drives similar products toward the same price level.

Reducing time to market is still important, and few will debate that a delayed product can ruin its chances of success. However, the rapid shrinking of product life cycles has occurred across the board, and the high expectations almost make reducing time to market a nonissue. Dataquest has described that use of gate array technology as not only a product differentiator but also as an important factor contributing to quick design. Recently, cell-based design has improved to the point where cell reuse and structured design has also contributed to faster concept-to-prototype times. ASIC vendors have improved their design efficiencies to the point where system level integration (SLI) is becoming more commonplace, again contributing to the shorter time-to-market trend.

In short, there is a delicate balance that designers manipulate that eventually determines product success. Largely affected by the recovering economy, systems designers are determined to provide increased functionality and time to market at a competitive price. Further analysis in this and later chapters will illuminate how this is accomplished and point out other significant trends.

Design-Cycle Trends

Reducing design-cycle time has been an important factor in reducing time to market. In North America, this has been an issue as systems competitors commonly experiment with varied team designs to reduce the product design time. The frequently touted, and often overused, term concurrent engineering has become a competitive weapon with which design-cycle times have been reduced.

In both North America and Japan, time to market has taken a back seat as cost has leaped to the forefront of importance. Designers in North America suggested that time to market held little value unless a product was sufficiently differentiated and cost-effective. At the same time, feedback from designers in Japan has made evident that the design cycle has reached a point of diminishing returns as small reductions in design-cycle time require large capital and personnel investments. As a result, designers in both North America and Japan have indicated that design-cycle time will not drop dramatically.

Signal Layers

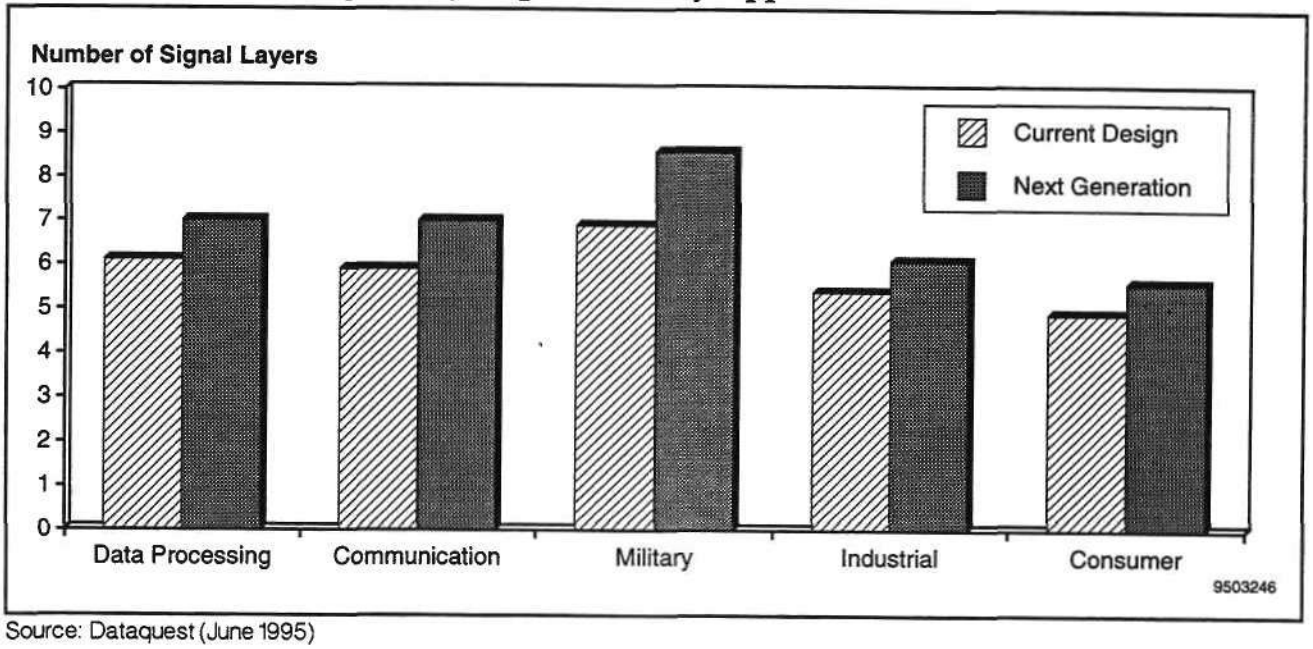
Increased chip complexity and system complexity naturally result in increased board complexity. Increased I/Os in smaller spaces require designers to invent more efficient packing schemes. One such method is increasing signal layer use. Users indicate that current designs require an average of six signal layers per board, while next-generation designs will require seven layers.

This increasing trend in signal layer use is driven by the data processing and aerospace/military arena (see Figure 3-2). Both application markets strive to achieve higher functionality in smaller space, and both concerns directly affect signal layer use.

Design Languages

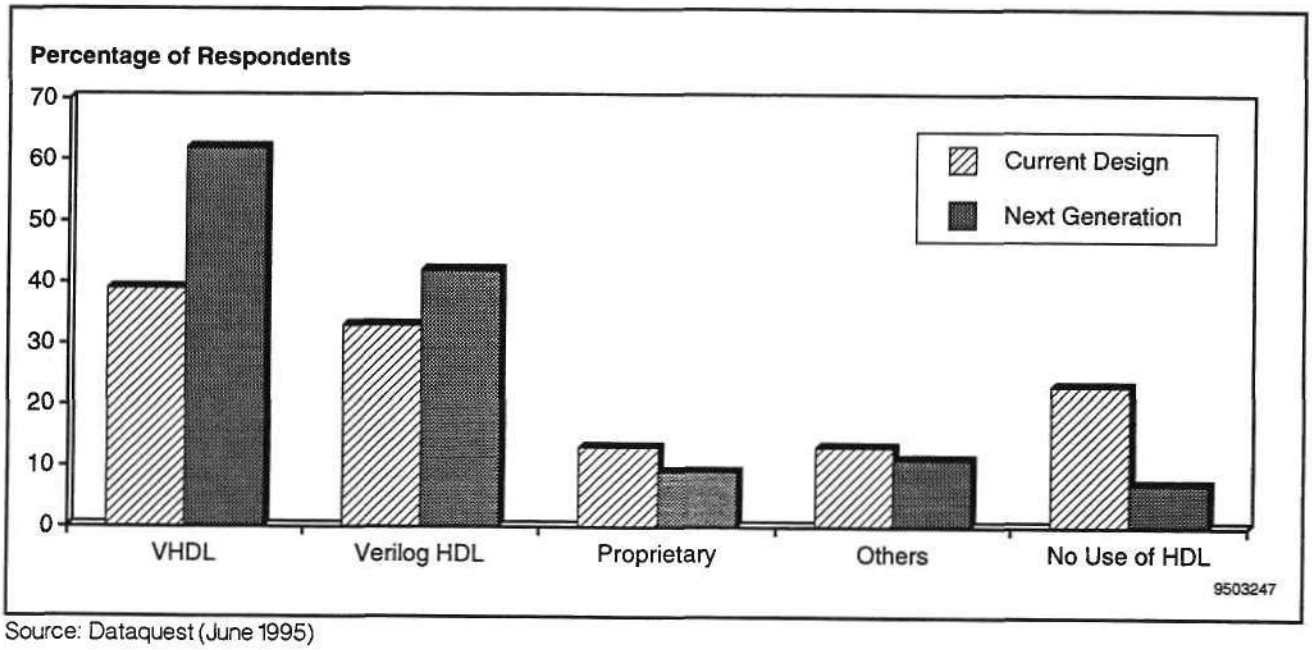
HDLs have played an important role in speeding up system design development times. Once a proprietary/internal-only arena, HDLs have grown into a multimillion dollar market. Dataquest asked their respondents to describe the current and future use of their design tools. Figure 3-3 shows that VHDL, the new standard, is gaining significant momentum in the marketplace. In fact, VHDL use was expected to grow significantly moving into 1994. Most of that growth was realized; however, Verilog use did not stagnate and also grew in 1994. Moving into 1995, designers reported that they would again step up their use of VHDL, with Verilog growth following at a slower pace.

Figure 3-2
Average Number of Signal Layers per Board by Application Market: North America



Source: Dataquest (June 1995)

Figure 3-3
Use of HDLs: North America



Source: Dataquest (June 1995)

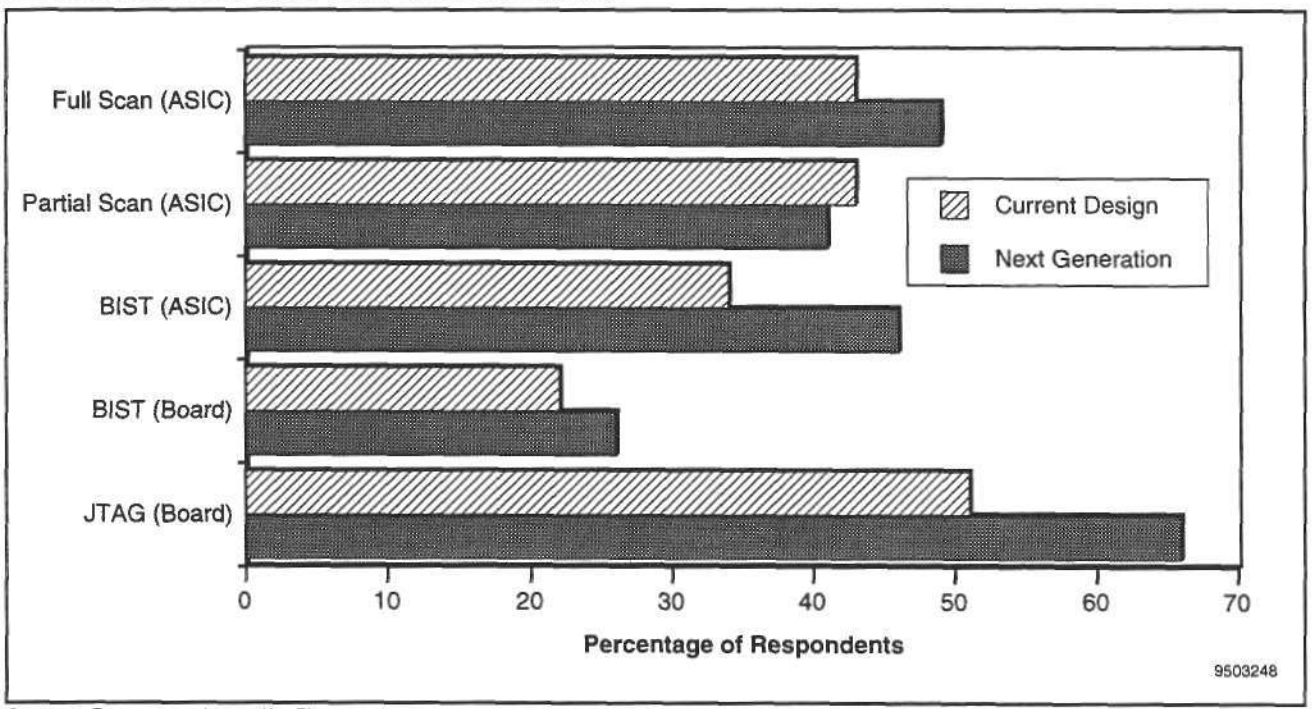
Testing Issues

Increased functionality may be a boon to the user, but it can lead to designs that are not 100 percent testable. Similarly, higher-complexity designs can lead to lower die yields and increased costs. To circumvent some of these problems, designers have been increasing the use of testing features and functions on-chip and on boards. Figure 3-4 shows the trend toward increased testing on the board and device level.

The figure displays an interesting trend for scan test. Users indicated that partial scan was losing popularity in comparison to full scan. Such a trend would suggest that the higher-density designs require more complete testing solutions. This also agrees with the growing use of BIST for the ASIC, almost single-handedly implicating the growing use of memories as a gate count driver. Another trend that also points this out is the large expected jump in JTAG testing for the board.

ASIC complexity and the concomitant increase in system complexity has forced systems designers to boost their utilization of various testing technologies. Some suppliers have focused much energy on providing efficient testing implementations, bringing down the die penalty to under 5 percent in certain cases. As ASIC density continues to rise, the die-size penalty should decrease in importance and allow designers to avoid the performance hit often associated with increased test functionality.

Figure 3-4
ASIC and Board Test Use: North America



Source: Dataquest (June 1995)

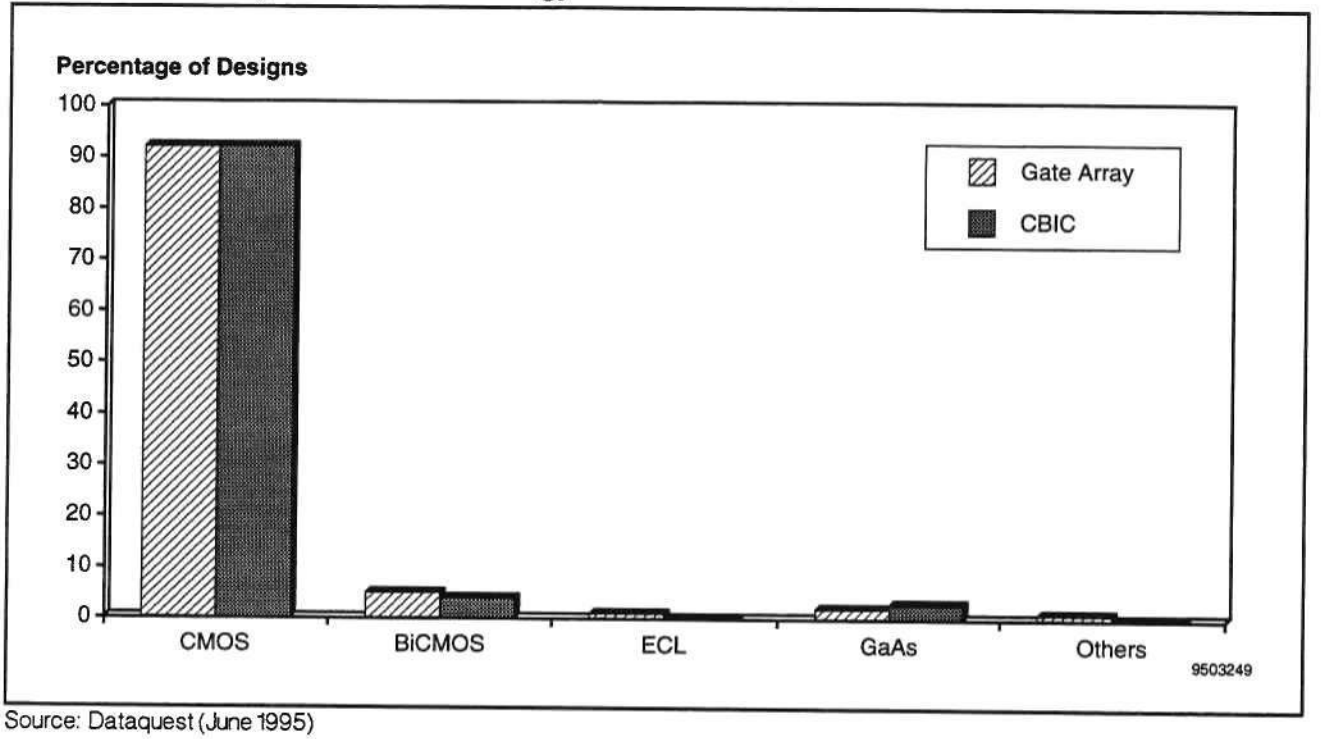
Material Process Technology

On the system and ASIC level, Dataquest wanted to find out if perceptions of new material technologies were gaining momentum. Systems designers reported the same trends as last year, which are expected to continue through 1995. Figure 3-5 shows that CMOS will still capture the mainstream designs in both gate array and cell-based designs. Along with that trend, they also reported that ECL is experiencing little, if any, activity; that GaAs still addresses niche applications; and that BiCMOS has limited application in areas where high speed and high drive are required. Survey respondents in Japan identified the same trends as those in North America.

Voltage Requirement Trends

In North America, the proliferation of "green" technologies and mobile computing has caused an ever-increasing interest in developing low-power devices. Similarly, there has been much hype about the new microprocessors running at 3.3V. What has occurred, however, is that the impact of 3.3V has been largely hype. Low-voltage design has not caught on, as people have not anted up for the mobile products quite as quickly as originally anticipated. Add to that the cost factor of 5V memories and the remainder of peripherals still running at 5V, and we have a perception mismatch.

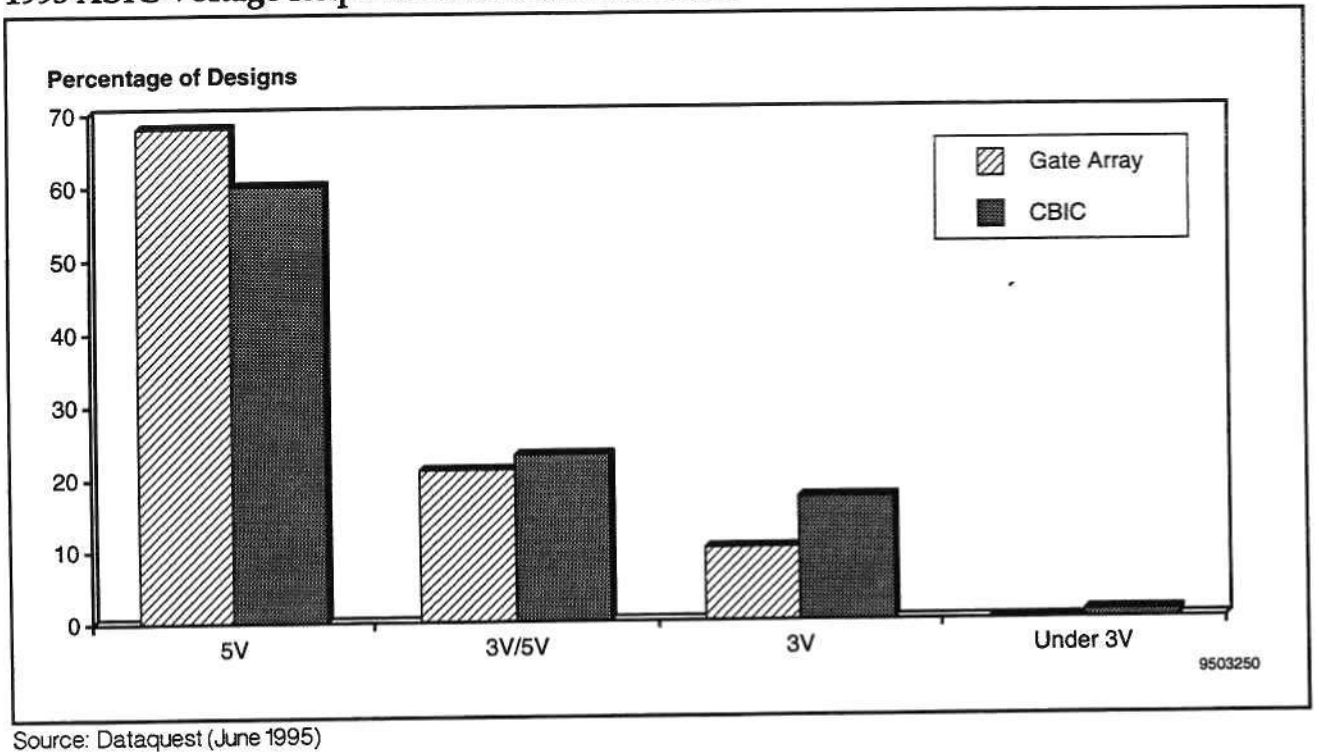
Figure 3-5
1995 ASIC Use by Process Technology: North America



Source: Dataquest (June 1995)

Results showed that about 60 percent or greater design starts in 1995 will occur in pure 5V technology. Suppliers must, therefore, maintain and support optimized 5V libraries for at least two years while 5V remains a significant factor. There is still ongoing development for low- and mixed-voltage products, but ASIC suppliers have seen the 5V drag effect and even released new 5V families to meet their customers' needs until actual low- and mixed-voltage demand catches up with the perceived demand. In the meantime, portable and mobile devices continue to drive low-voltage ASIC design and system design. Figure 3-6 shows the estimated design starts in various voltage requirements for both gate arrays and CBIC. The most noticeable trend is the increasing use of 3V technology in CBICs, which address high-density and mobile applications well. This trend also was consistent with results from Japan.

Figure 3-6
1995 ASIC Voltage Requirements: North America



Source: Dataquest (June 1995)

Chapter 4
Design Trends and Issues: Japan

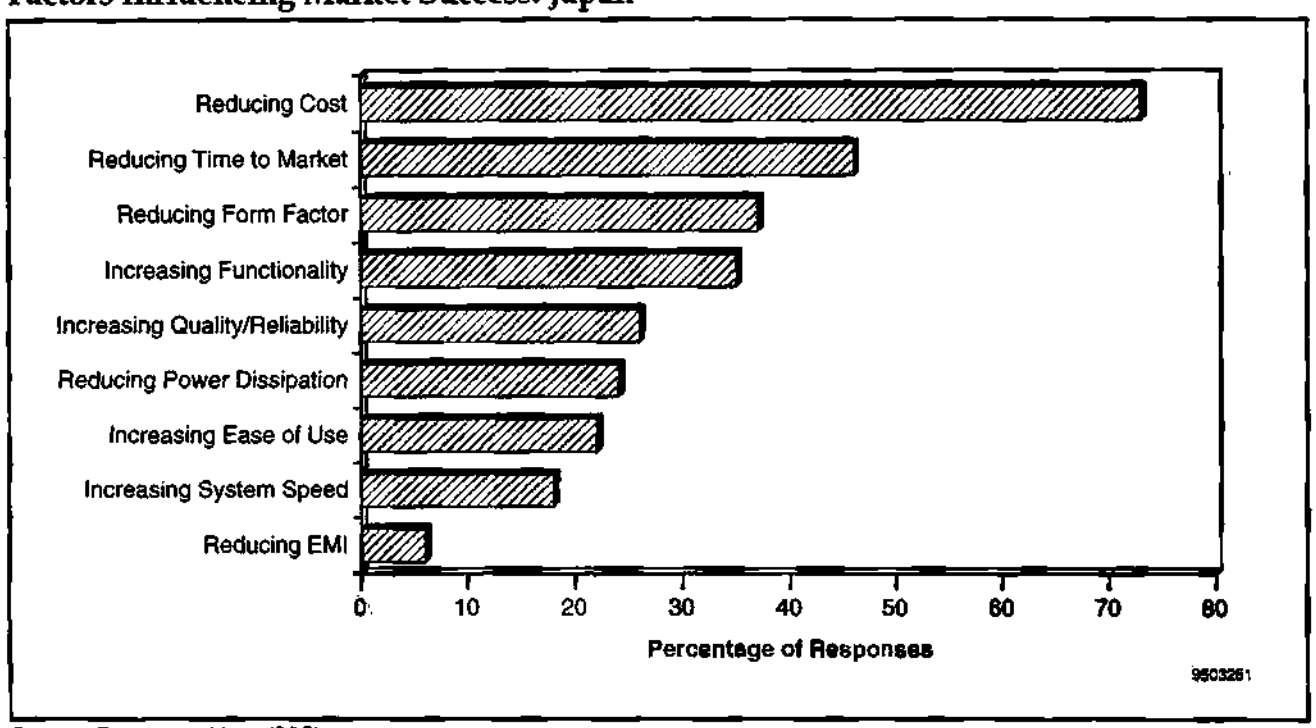
Just as software is adapted to kanji for the Japanese market, products designed in Japan for consumption in Japan need to be tailored to the market's needs. To understand the intricacies and dynamics of the system market in Japan, Dataquest asked systems designers in Japan to explain the market. The key to successfully opening the door to the ASIC market is in understanding how systems designers think and how they build their products. With a better understanding of systems designers' requirements, specific markets can be targeted and penetrated more effectively.

In this chapter, Dataquest analyzes the critical factors that determine success for systems designers, the ASIC design cycle, and the characteristics of the systems designed.

Determining Market Success for Systems Designers

Great design does not guarantee a successful product. In fact, there is a delicate mix of factors that combine to propel a product onto the road of success. The best design on the drawing board may never be successful if it takes too long to build or costs too much. Similarly, the system speed and reliability can determine how well the product fares down the line. To understand the designers' perspective on this issue, Dataquest requested that each respondent select the three attributes most important to their product's future ability to achieve market success. Figure 4-1 shows the most important attributes that lead to market success for systems designers in Japan.

Figure 4-1
Factors Influencing Market Success: Japan



Source: Dataquest (June 1995)

While the magnitude of the response was varied on an application market basis, the overall results were consistent. The four most important factors were as follows:

- Reducing cost
- Decreasing time to market
- Decreasing form factor
- Increasing functionality

Reducing cost was by far the most critical success factor. The last time Dataquest surveyed users in Japan, reducing cost was the No. 1 driving force, beating out decreasing time to market by a 25 percent margin. This year, cost reduction again led with a similar margin over decreasing time to market. After reducing time to market, the next two factors were reducing form factor and increasing functionality.

The success factor rankings in Japan clearly indicate that cost is primary and that the other factors form a tier of secondary importance factors. In fact, the general perception of products from Japan consists of two main points: high quality and very expensive. Because the quality is perceived to be so high, increasing quality has become less important—as a focus there would clearly lead to diminishing returns. But designers can address the other perception and focus on price. Japan's economy has been improving, but the country is cautious because of the strong yen. The natural tendency would be to focus their energy in directions that would strengthen their economy and ensure long-term success. This may be accomplished by utilizing the manufacturing skill prevalent throughout system houses. By streamlining the design to prototype cycle, cost-reduction goals can be achieved.

Once the cost issue is addressed, the other factors come into play: functionality, time to market, and form factor. The time-to-market factor has risen in importance over the last year, taking over No. 2. Increased competition from imports from North America, Taiwan, and Korea has put stress on the design cycle for those companies that want to enjoy the benefits of pioneering new products or features. Basically, the decreasing time-to-market argument is based on the premise that potential revenue is lost for each week the product is not on the market. While this certainly may be the case, the quick cycle time and volume atmosphere in Japan also make time to market a cost and productivity issue. Concurrent engineering with special attention to design for test (DFT), design for assembly (DFA), and design for manufacturing (DFM), places a premium on engineers' time. Time is money, and decreased cycle time translates not only to quicker time to market, but also to reduced engineering costs.

As in North America, increasing functionality in Japan continued to be an important factor because it acts as a differentiator. In Japan, the issue of increased functionality is not simply product differentiation, but it's also a way of life where the philosophical "bar" is raised as new functionality is introduced. One need look no further than the rapid introduction of consumer products to see this at work. In the cost-competitive environment that has developed, the premium for functionality is not readily accepted. The most bells and whistles do not necessarily make a winning product,

but if priced right, the features can at least keep the customer and push a sale in the right direction.

Decreasing form factor has also risen in importance. Form factor ranks not only as a cost issue, but also as an opportunity cost. With space at a premium in Japan, form factor reduction can influence product acceptance. This is especially true in the consumer market, where form factor is a major thrust for handheld and "fits-in-your-pocket" products. Beyond that, at the board and chip level, board shrinks and total reduced silicon area are by definition less expensive. With those two factors working together, smaller, feature-rich products appeal not only to users, but also to management.

In short, the cost factor remains the dominant force in determining product success. Largely driven by the recovering economy, systems designers are determined to provide increased functionality and time to market at a competitive price, in the right form factor to meet customers' needs. Further analysis in this and later chapters will illuminate how this is accomplished and point out other significant trends.

Signal Layers

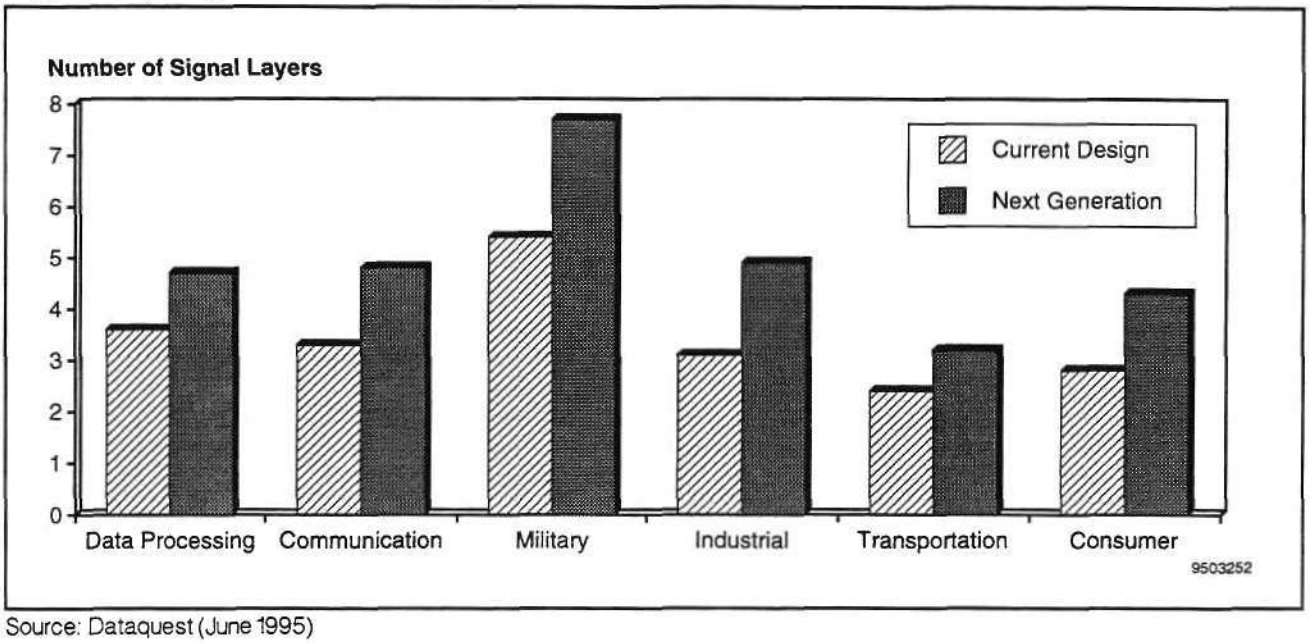
Increased chip complexity and system complexity naturally result in increased board complexity. Increased I/Os in smaller spaces require designers to invent more efficient packing schemes. One such method is increasing signal layer use. Users in Japan indicate that next-generation designs will require an increase in signal layers per board, from an average of 3.2 up to 4.4. While an ambitious percentage increase, the net gain will place the new designs at less signal layers per board than their North American counterparts. The fewer signal layers in the designs from Japan indicate a lower degree of complexity, one factor that allows the products to get to market faster.

This increasing trend in signal layer use is driven by the data processing and communications markets (see Figure 4-2). Both application markets are facing competition to provide greater functionality in smaller space, and both concerns directly affect signal layer use.

Design Languages

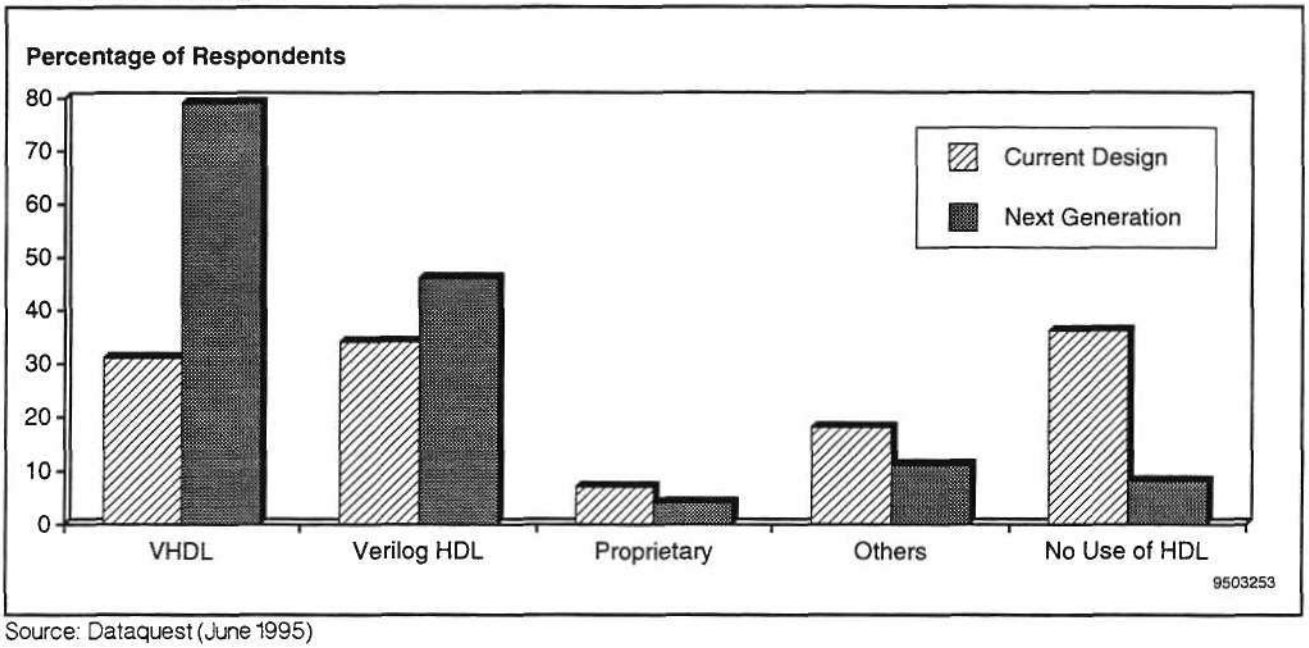
HDLs have played an important role in accelerating system design development times. Once a proprietary/internal-only arena, HDLs have grown into a multimillion dollar market. Dataquest asked our respondents to describe the use and planned use of their design tools. Figure 4-3 shows that VHDL, the new standard, is gaining significant momentum in the marketplace and narrowing the gap between it and Verilog. Looking into next-generation design, however, designers reported that there is an enormous potential for VHDL to surpass Verilog. Closer examination suggests that much of VHDL's growth results from those who do not use an HDL currently. The planned use of HDLs also suggests that in many cases, both HDLs will be used.

Figure 4-2
Signal Layers per Board Design: Japan



Source: Dataquest (June 1995)

Figure 4-3
Use of HDLs: Japan



Source: Dataquest (June 1995)

Chapter 5
Product Trends: North America

To develop and market ASIC products that are competitive in North America, it is important to examine the integration levels used in ASIC designs for current-generation systems and plans for next-generation system designs.

In this chapter, Dataquest explores the ASIC product trends by application. The first section looks at gate arrays and cell-based designs, while the second section examines programmable logic devices. We further subdivided those sections covering gate counts, system clock speeds, and packaging when applicable.

Gate Array and CBICs

The trend toward system level integration and high-density design has been discussed by Dataquest in the past. To further quantify the design activity, Dataquest took a closer look at the trends defining and differentiating the usage of gate arrays and CBICs.

Design Starts by Gate Count

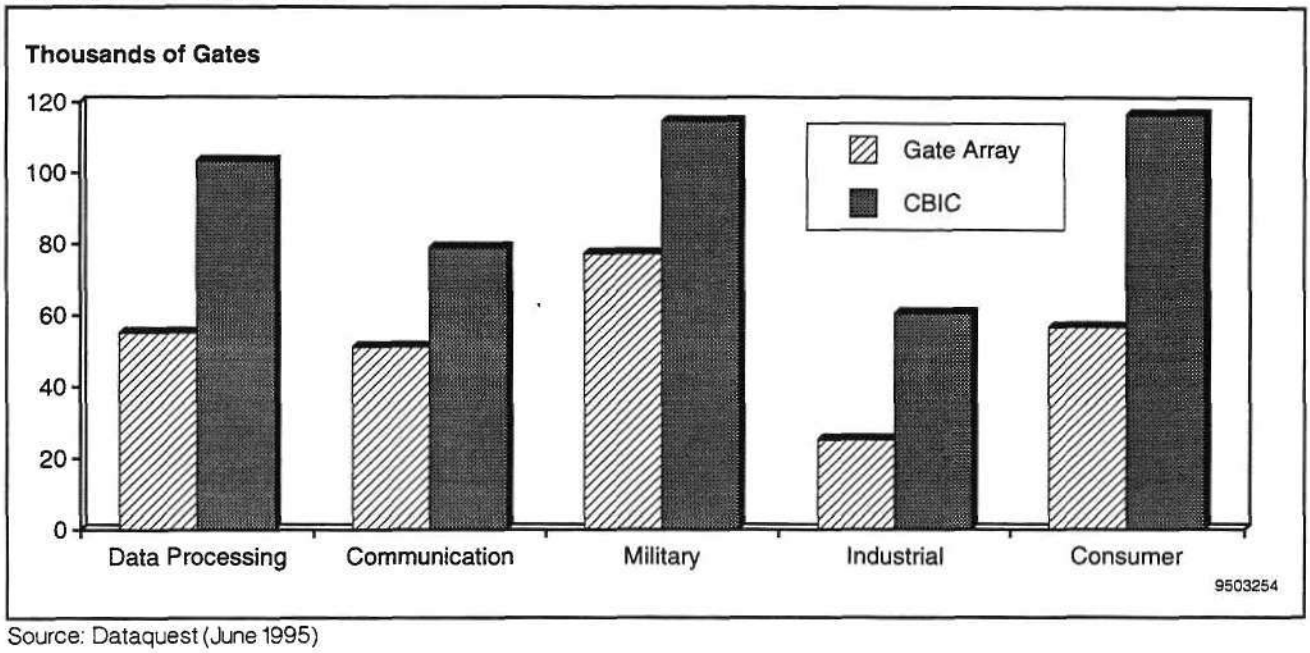
Have ASIC designs increased significantly in size? What will be the face of ASIC densities profiles through 1995? In order to view design-size migration patterns, Dataquest asked respondents to indicate the average and maximum gate densities of their gate array and cell-based designs. Figures 5-1 and 5-2 show the 1995 average and maximum estimates by utilized gate count for gate array and CBIC designs by overall application markets. Both charts show a trend Dataquest has been discussing for quite some time—that CBICs are leading gate arrays in the high-end market. For cost, design reuse, power, and speed considerations, CBICs have gained popularity for high-density designs.

Designers reported that the average gate array design will exceed the 50,000 gates for 1995, averaging about 54,000 gates. Respondents also claim that the average CBIC gate count will climb to over 92,000 gates this year. Both the average and maximum gate sizes should continue to grow healthily as increases in functionality drive multiple solutions onto a single die. Furthermore, Dataquest believes that large SRAMs (128Kb and 256Kb) will be diffused in the gate array base wafers and used for cache memory. Other functions such as SCSI, ALU, multiplier, multiplier-accumulator, FIFO, DMA controllers, cache controller, and 82XX microperipherals will also be diffused in the gate array and will drive the average gate counts upward.

Figure 5-3 shows the distribution of gate array and CBIC designs by average expected gate count in 1995. Dataquest analysis of these figures reveals the following important points:

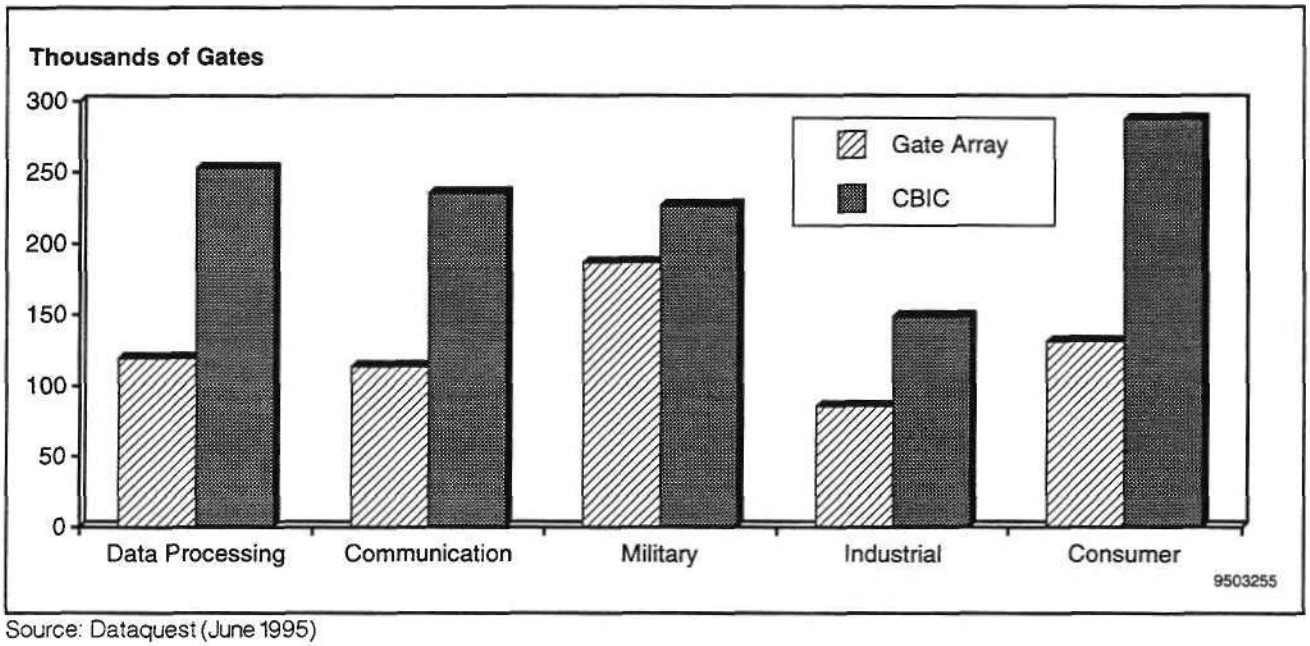
- Peak use for both gate arrays and CBIC designs is in the range of 20,000 to 50,000 gates.
- CBICs are expected to outpace gate array growth in the category of more than 100,000.
- Gate arrays dominate designs with less than 20,000 gates.

Figure 5-1
1995 ASIC Design Starts by Average Gate Count by Application Market: North America



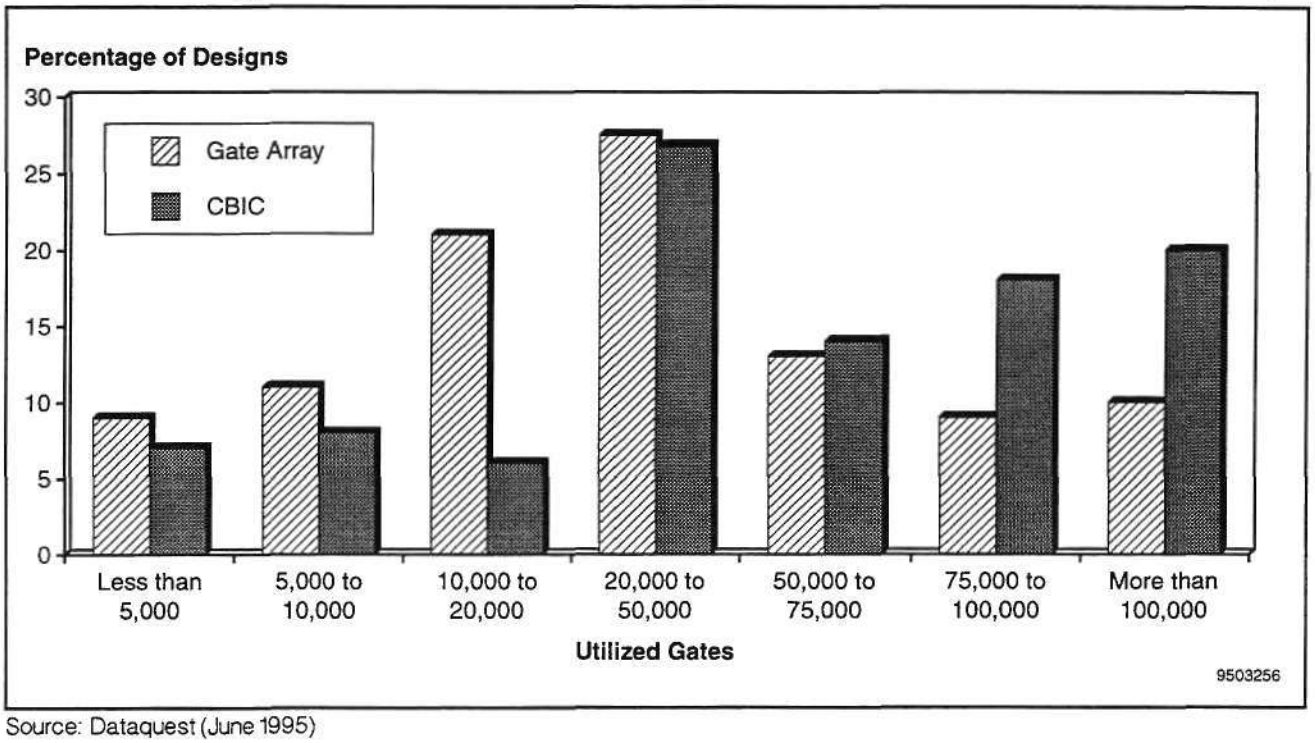
Source: Dataquest (June 1995)

Figure 5-2
1995 ASIC Design Starts by Average Maximum Gate Count by Application Market: North America



Source: Dataquest (June 1995)

Figure 5-3
1995 ASIC Design Start Distribution by Average Utilized Gate Count: North America



Source: Dataquest (June 1995)

System Clock Speeds

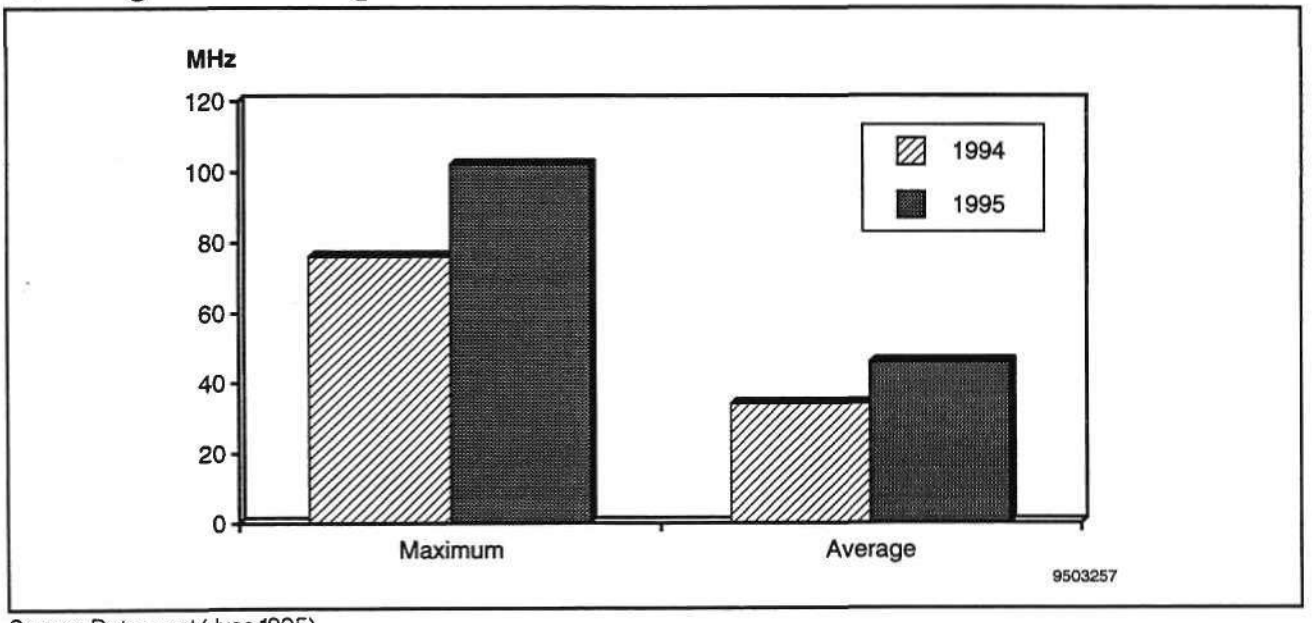
More speed! No one seems to get enough of it. Just as the designers are pushing for more functionality, bells, and whistles, the need for speed continues to rise. As more devices become intelligent and networked, the old communications standards of last year are no longer acceptable. "More bandwidth!" is the accompanying clamor, as computers and communications devices fight for bus presence. ASIC designers described the trend toward more speed: slower devices are getting faster, average speeds are climbing, and maximum speeds are soaring. Figure 5-4 shows the increasing speed trend. The average maximum clock speed will increase from 75.6 MHz in 1994 to 102.1 MHz in 1995. For a true meeting of the minds, silicon providers need to meet the designers' needs with efficient silicon solutions at those high speeds.

Last year was led by designs in the 21- to 33-MHz range (see Figure 5-5). However, the curve was relatively smooth except for a steep decline above the 50-MHz mark. In 1995, this will not be the case. Although the 21- to 33-MHz range is still important, perceived demand of those products is not nearly as strong. The curve appears to be extending and shifting out, with the highest number of designs in the 34- to 50-MHz range.

Cell Libraries

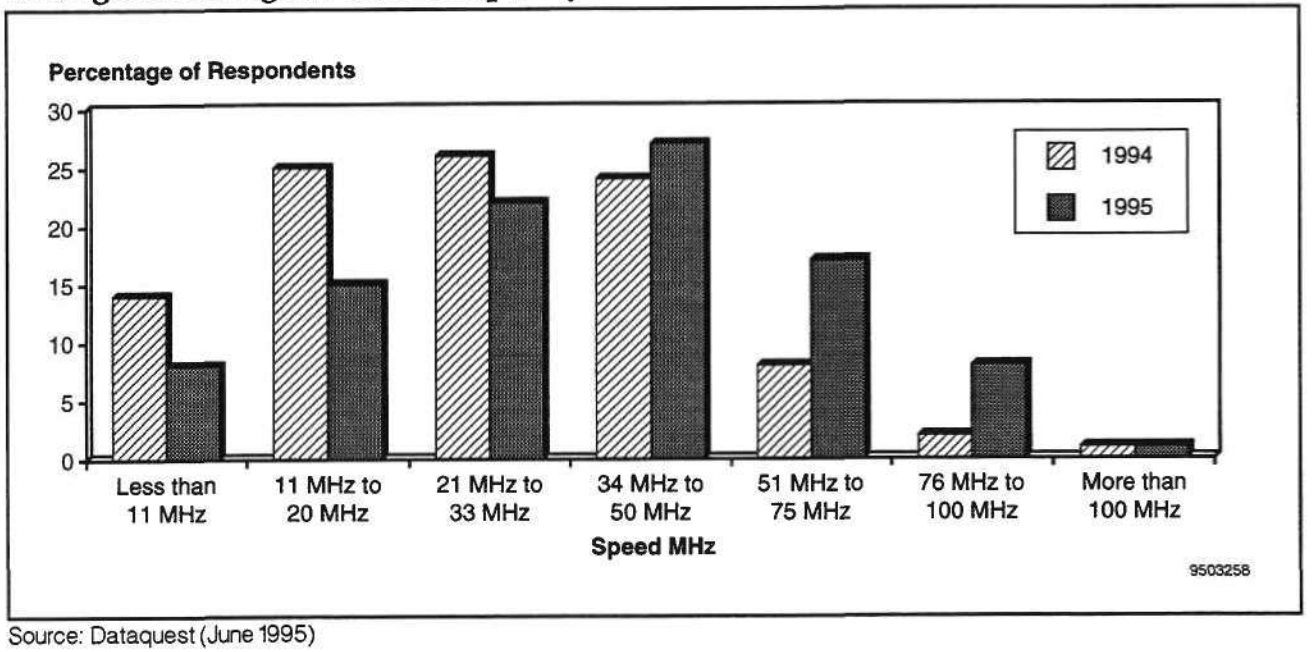
Cell libraries have arisen as an important way to differentiate ASIC suppliers. While some suppliers operate on a pricing strategy, others focus on developing numerous cells to allow them to address a variety of user needs. Dataquest asked users to indicate which cells they used in their 1994 designs and planned for their 1995 designs. Figures 5-6 and 5-7, respectively, show gate array and CBIC cell use.

Figure 5-4
ASIC Digital Clock Frequencies: North America



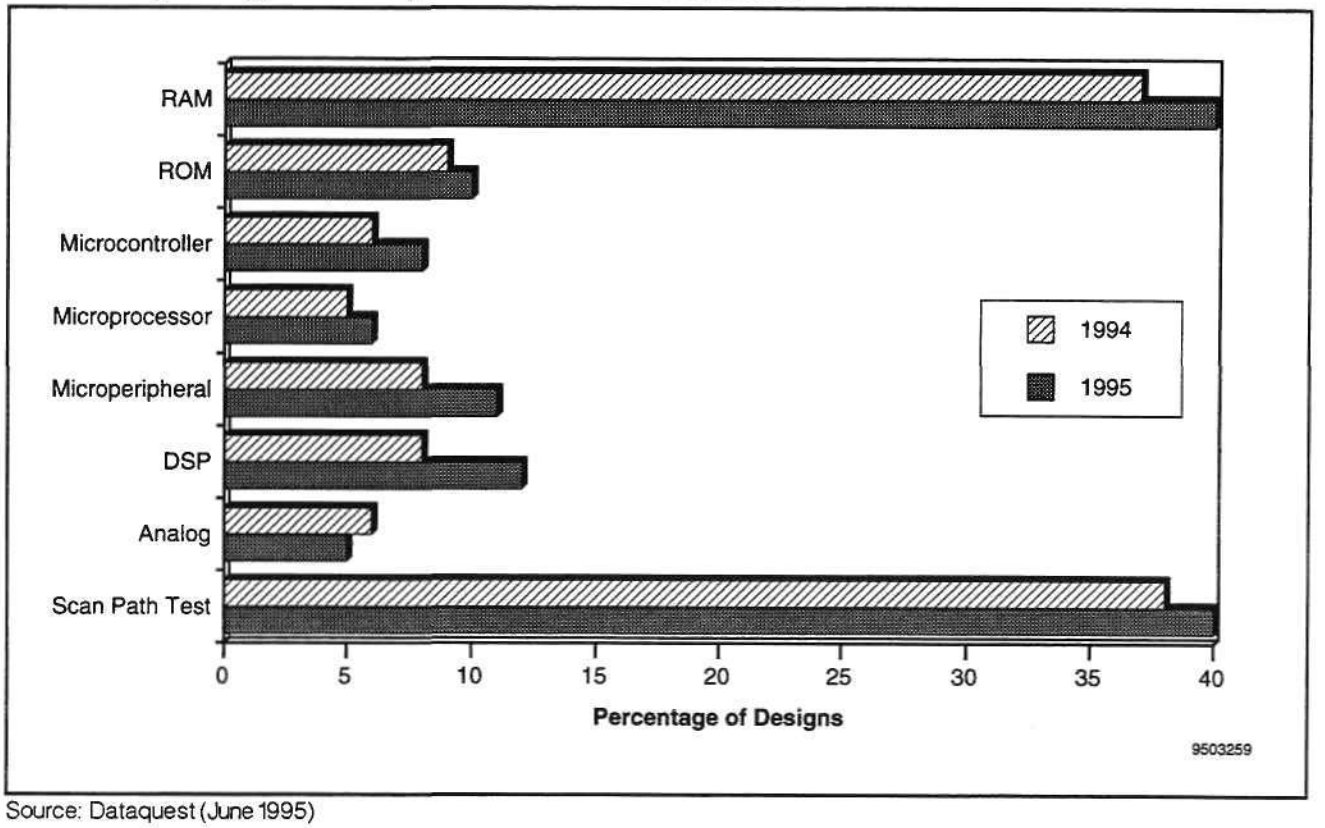
Source: Dataquest (June 1995)

Figure 5-5
Average ASIC Digital Clock Frequency Distribution: North America



Source: Dataquest (June 1995)

Figure 5-6
Gate Array Design Starts by Cell Use: North America



Source: Dataquest (June 1995)

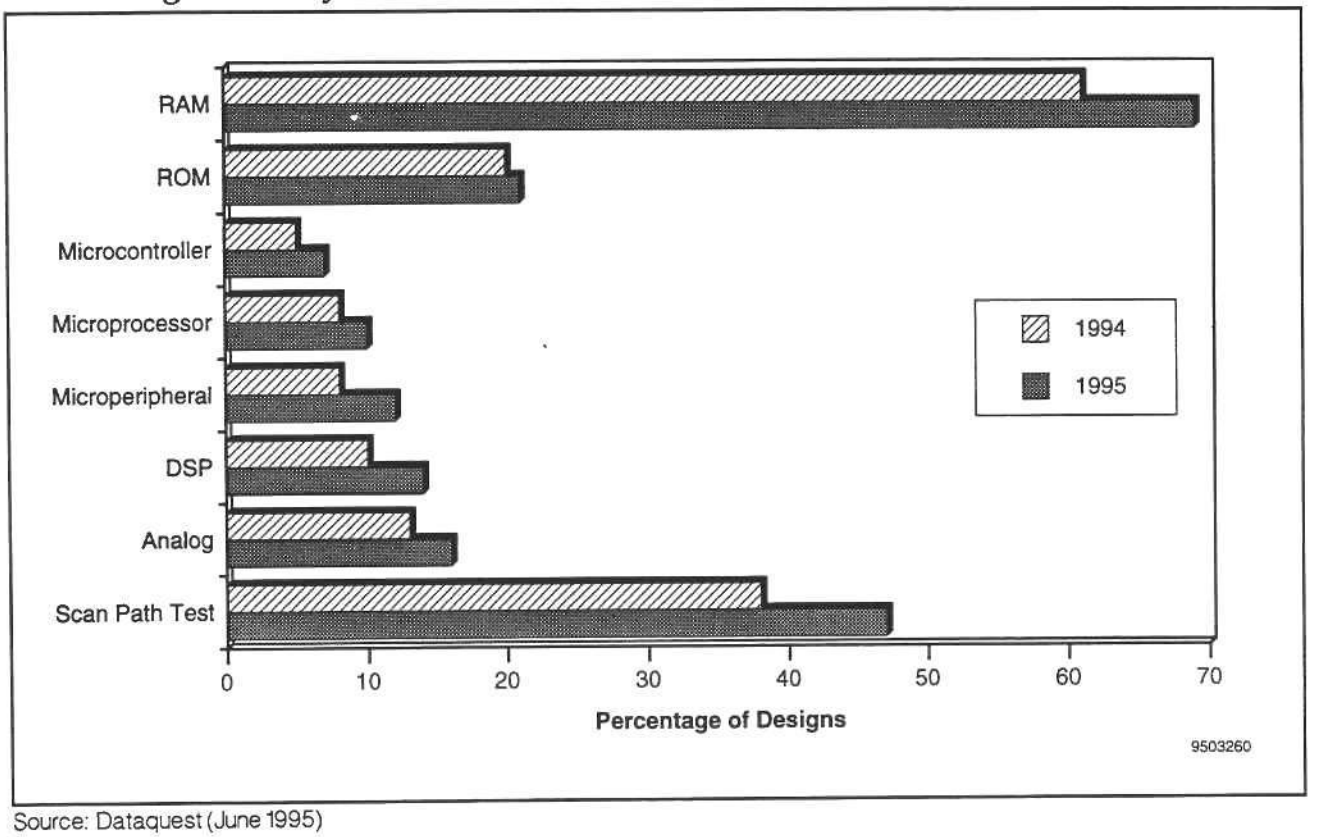
Important points about these figures are as follows:

- RAM and Scan Path Test cells are the most popular cells for both gate arrays and CBICs.
- The high use of Scan Path Test cells in CBICs is needed for the higher densities described earlier.
- There is a rapid rise in on-chip microperipherals, primarily of the 82XX type such as DMA controllers.
- Cell use in ASICs is increasing for all types, except analog in gate arrays, where pure analog arrays are being phased out.

Memory Sizes

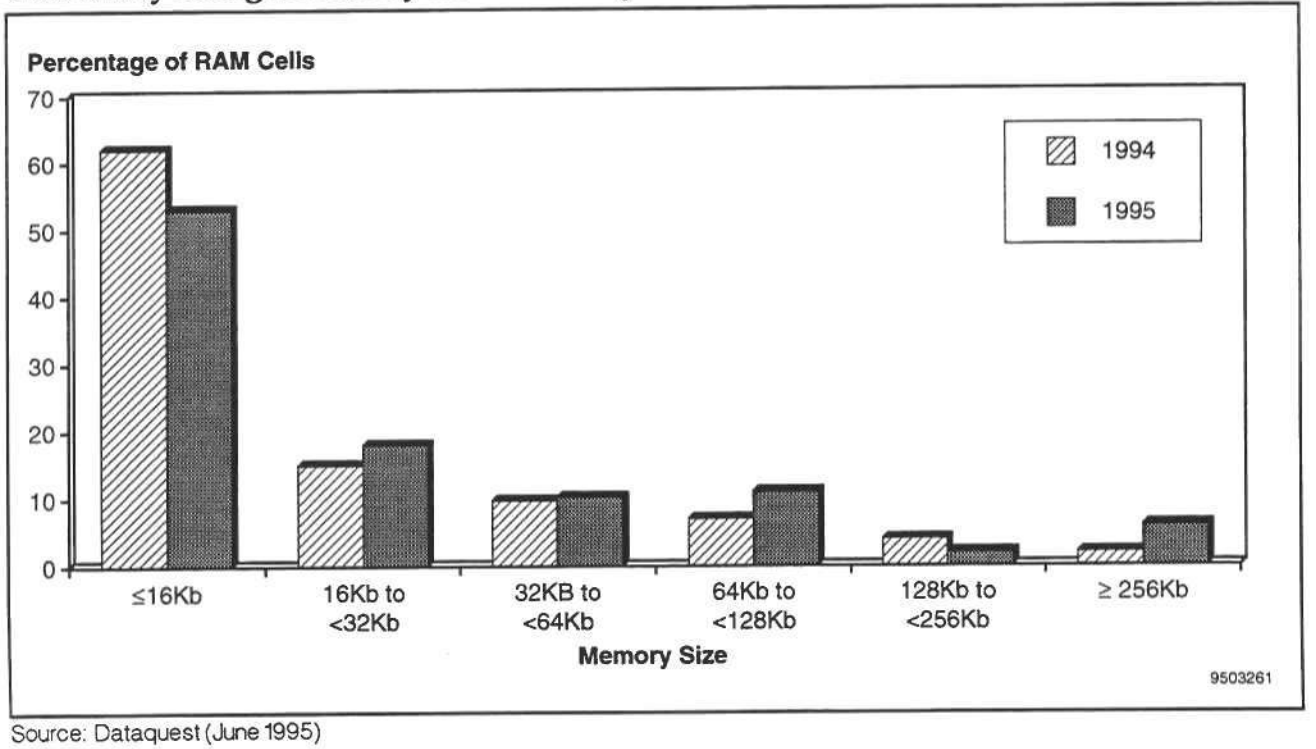
The size and amount of memory used in gate arrays has been increasing, and Dataquest asked designers to describe the trend. Users indicated that over 50 percent of the designs that used memories implemented less than 16Kb (see Figure 5-8). In fact, design starts using the glamorous large SRAMs of 128Kb or larger barely surpassed 5 percent of those design starts. However, users also indicated that they would be increasing their use of SRAM in 1995, where the use of over 256Kb will grow nearly 5 percent in 1995.

Figure 5-7
CBIC Design Starts by Cell Use: North America



Source: Dataquest (June 1995)

Figure 5-8
Gate Array Design Starts by Total Memory Size: North America



Source: Dataquest (June 1995)

Microprocessor Use

As available density increases on a single chip, other functional blocks besides RAMs are being implemented. One such element gaining in popularity are microprocessors. Dataquest found that the 68xxx were the most popular cells for gate arrays and embedded arrays (see Figure 5-9). MIPS and ARM cores were also popular for communications-type applications. Designer also indicated that custom or proprietary processors made up the balance of those not on the survey.

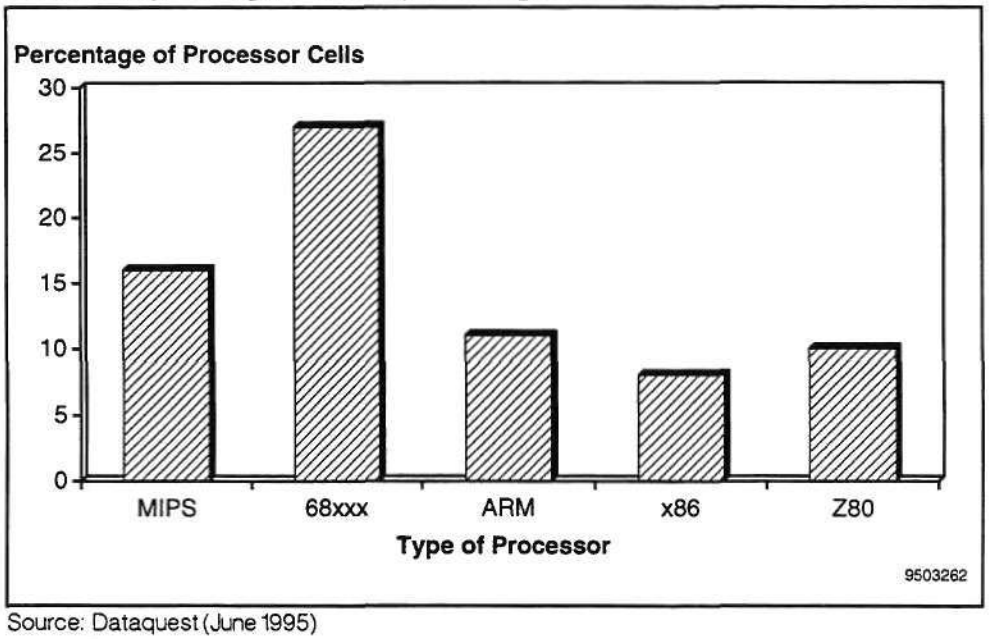
Packaging Trends

Packaging Types

Packaging improvements have allowed complex designs to make the jump from esoteric curiosities to functional realities. High I/O requirements are pushing packaging designers to rethink and reinvent pad-pitch relationships and capacitance issues. Thin-lead requirements and the accompanying problems have led designers to consider the future of their high-density designs alongside the packaging constraints.

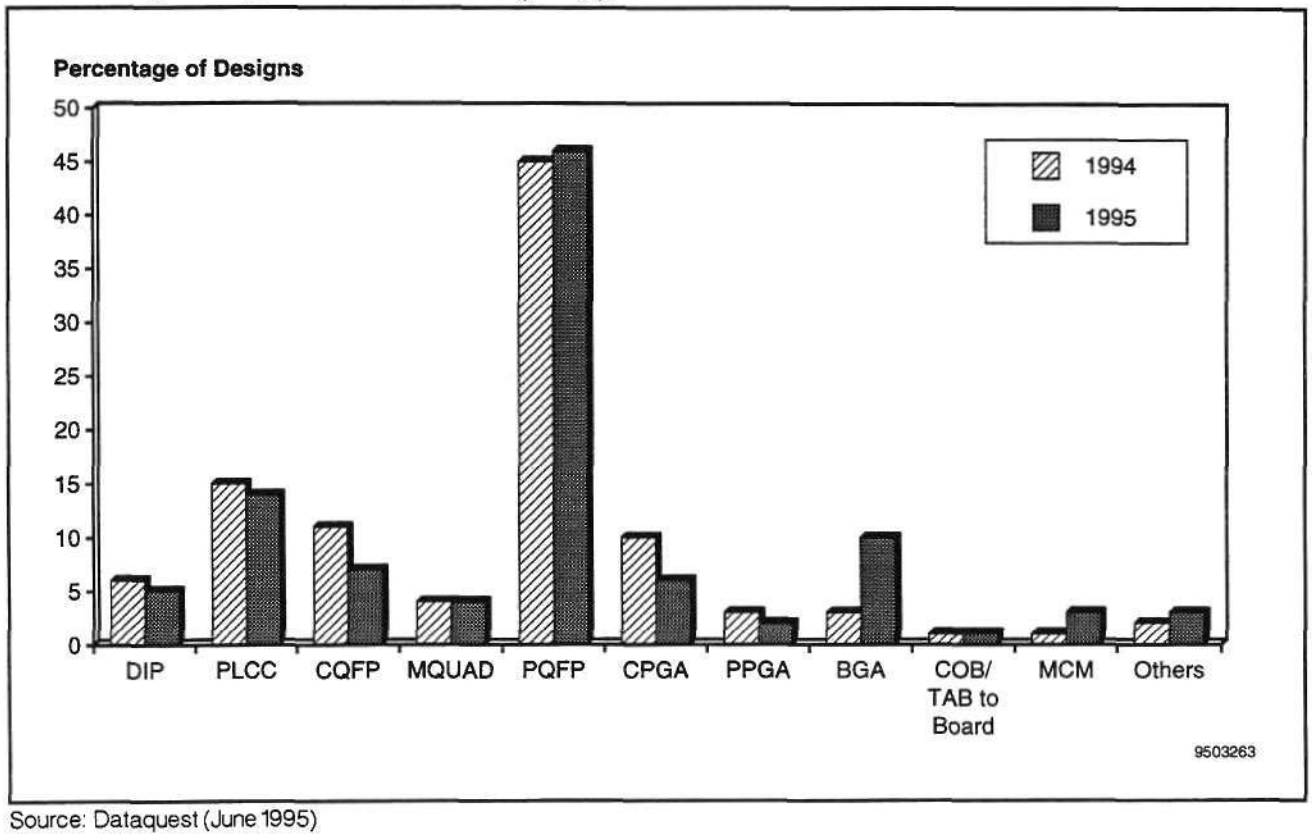
Figure 5-10 shows the trend of packages in the near future. Of importance is the slight resurgence of the PQFPs. With the introduction and ramp-up of thermally enhanced QFPs, designers have targeted their designs in the more cost-effective packages, effectively extending their popularity. As high I/Os become an issue, however, the PQFPs become less feasible design solutions as the fine lead pitch becomes a common handling problem. Pin Grid Arrays (PGA) can accommodate the I/O requirements but have a major drawback when board space is an issue because of the through-hole design requirements. To maintain the surface-mount design savings, many vendors have begun to look closely at the Ball Grid Array

Figure 5-9
Gate Array Design Starts by Microprocessor Cell: North America



Source: Dataquest (June 1995)

Figure 5-10
Gate Array Design Starts by Package Type: North America



Source: Dataquest (June 1995)

(BGA) package, which not only provides the benefits of surface-mount technology and the required I/Os but is also self-aligning. In fact, designers suggested that close to 10 percent of their designs in 1995 will use some form of BGA, more that doubling the use in 1994.

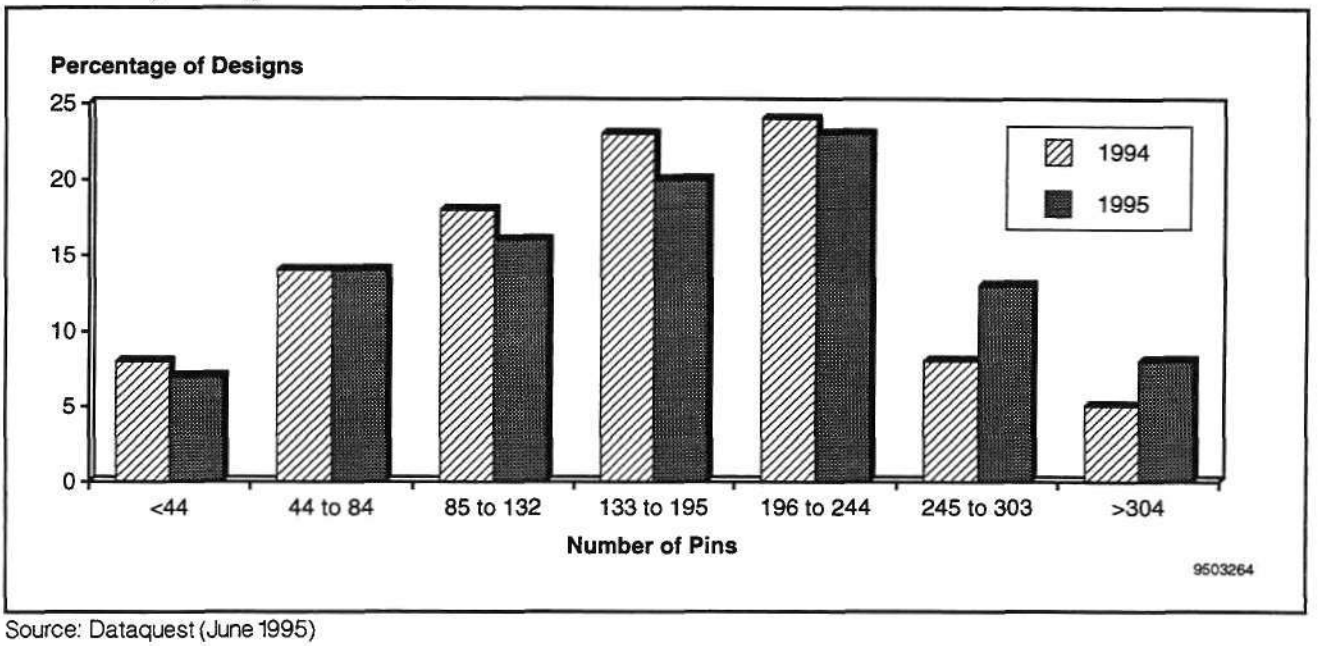
Pin Counts

It is often said that ASICs drive future packaging requirements. As ASIC designs increase in size and complexity, the packages must be developed that enable full access to the ASIC's functionality. Dataquest asked users to estimate the percentage of designs using different pin counts. Figure 5-11 shows how users responded. The bulk of packages had between 196 and 244 leads for 1994, dominated by the 208 quad flat pack. In 1995, the pin-count range of choice remains the same; however, there is almost a unilateral shift upward in the pin-count ratings. The majority of packages will have 133 to 244 pins, with greatest growth occurring in the packages using over 244 pins. Again, increased functionality means higher integration, which can translate to more required pins.

Programmable Logic

Rounding out the ASIC market are the PLDs. Living off the need for flexible solutions and quick time to market, programmable logic has found its way into applications ranging from personal electronics on up to supercomputers. Last year even had high-density PLDs (CPLDs and FPGAs) on motherboards or as the primary logic for supercomputer-class designs.

Figure 5-11
Gate Array Design Starts by Pin Count: North America



Source: Dataquest (June 1995)

MOS PLDs are a fast-growing ASIC market with a compound annual growth rate of nearly 21 percent from 1993 through 1998. To gain insight into this market, Dataquest allocated a significant portion of its survey to PLDs.

Development Seats

To get a better understanding of PLD use, respondents were asked how many development seats their teams had. Respondents indicated that the average number of PLD development seats per team was 3.3. With an overall average team size of 10, this would indicate a situation where sharing seats is required or where teams have a designated-PLD staff member. A typical development seat was responsible for 3 designs per year, though up to 5 designs per seat per team was not uncommon.

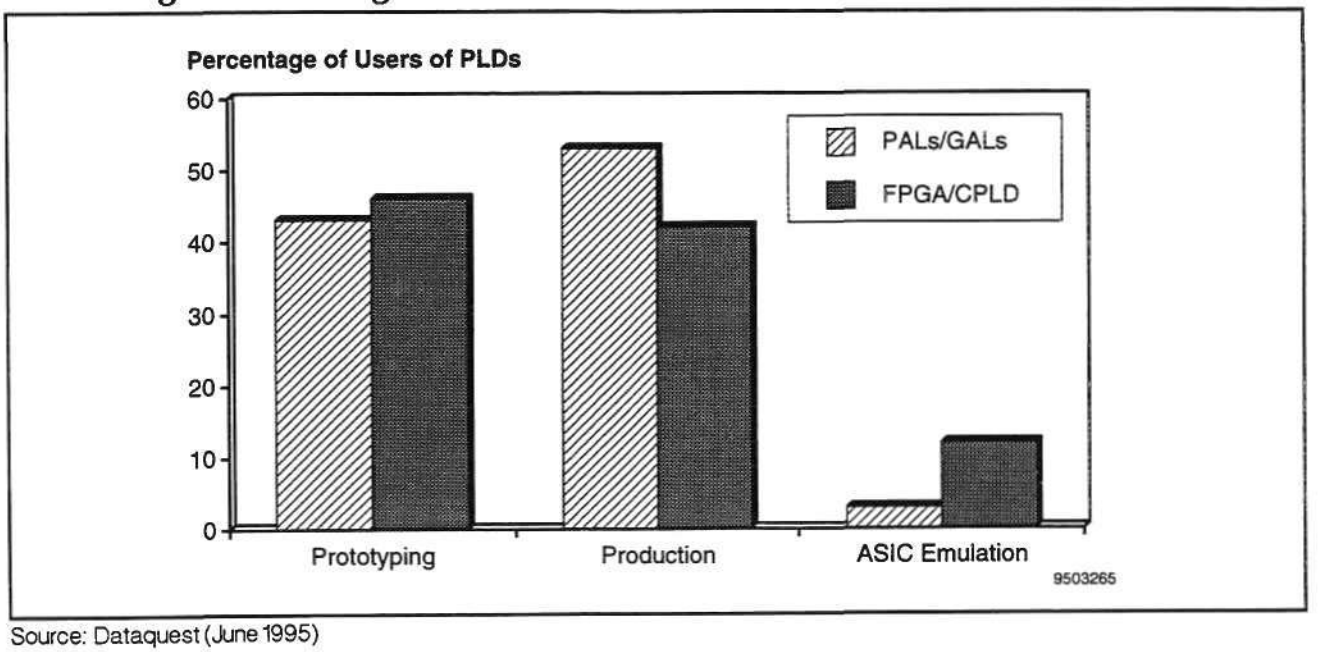
Device Use

Gate array suppliers often ask if PLDs are viable production solutions or simply a prototyping vehicle. Dataquest investigated the uses for both simple PLDs (PALs and GALs) as well as for high-density devices (FPGAs and CPLDs). While it is true that a significant portions of PLDs are used for prototyping, Figure 5-12 shows that a high percentage of both simple and complex PLDs are used for production.

High-Density PLD Designs by Gate Count

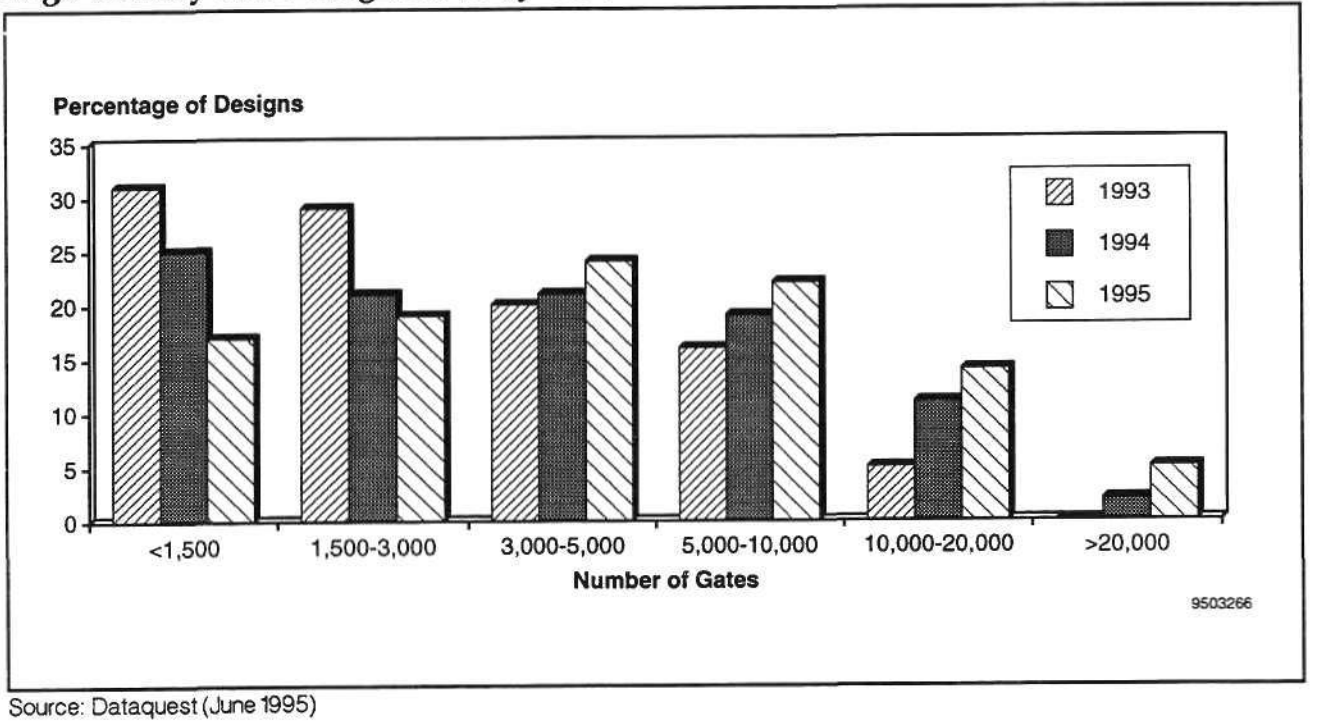
Gate array suppliers have lost a portion of the low-end gate array market to PLDs. The question that remains is: What gate count ranges have PLDs penetrated? Dataquest asked users to indicate what percentage of their designs fell into various gate ranges. Figure 5-13 shows the gate count by design starts for 1993 and 1994 and what users expect to use in 1995. In 1994, the most popular density for programmable logic was the sub-1,500-gate range followed by the 1,500-to-3,000-gate range. Clearly, the work-

Figure 5-12
Use of Programmable Logic: North America



Source: Dataquest (June 1995)

Figure 5-13
High-Density PLD Design Starts by Gate Count: North America



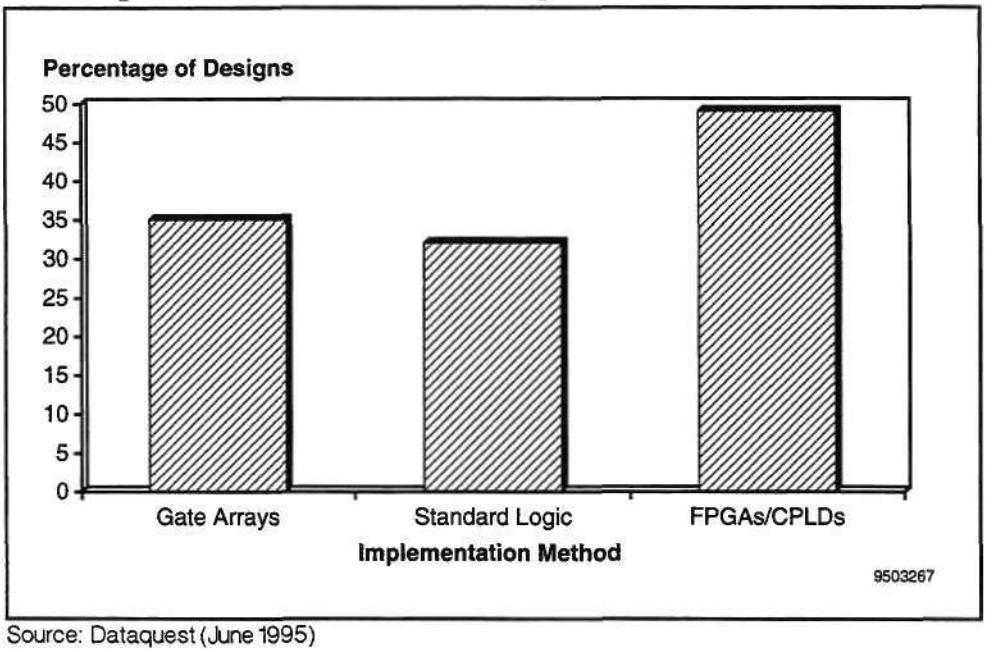
Source: Dataquest (June 1995)

horse designs are on the low end, where PLDs are maturing and more cost-competitive with nonprogrammable solutions. The design profile is changing, however, and designers indicated that they will boost their average design density into the 3,000-to-5,000-gate range for 1995. In fact, confidence and interest has increased to the point where designs over 10,000 gates will constitute over 15 percent of PLDs by year-end. The one caution that needs to be attached to this is that while design activity is extending upward, PLD units remain shipping at the lower densities in volume.

Implementation and Limiting Factors

Programmable logic has been gaining in popularity as designers' confidence in tools, and their own experience, has increased. Dataquest asked users to indicate how they implemented small amounts of random logic (see Figure 5-14) to see how this has impacted system design. Users indicated that nearly a third of systems used standard logic for the implementation while nearly 36 percent responded that gate arrays were used. Just below 50 percent of designers responded that they used high-density programmable logic for the implementation. A quick review of the data suggests that there is still significant opportunity to grow the use of programmable—the designs in gate arrays and standard logic represent growth markets for FPGAs and CPLDs with the exception of high-volume applications. It is important to note that designers indicated that they often used a combination of devices to implement random logic, and, therefore, PLDs and standard logic could coexist on the same board. Similarly, designers were not asked if their response was limited to volume solutions, so it is likely that the programmable logic may have been used in prototyping and preproduction.

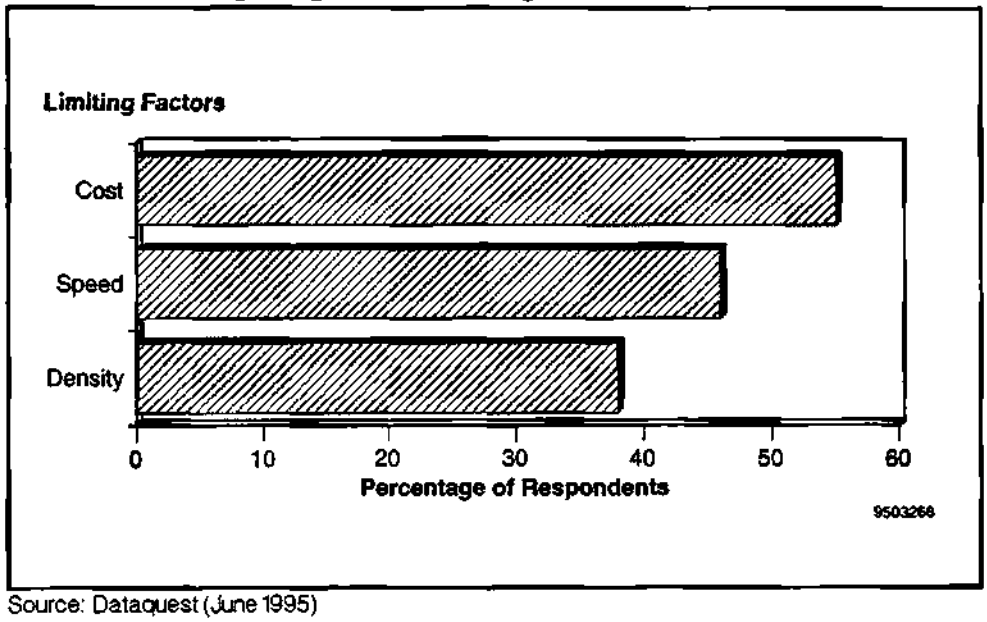
Figure 5-14
1994 Implementation of Random Logic: North America



Source: Dataquest (June 1995)

What prevented the use of programmable logic? Dataquest also asked users to explain why (see Figure 5-15) they do not utilize it. It turns out that cost was the No. 1 reason designers did not implement programmable logic. In fact, it appears that cost may be the only issue for some, limiting their scope and narrowing their vision away from programmable logic solutions. Next most important was speed—a problem designers have raised their voices about because they have been unable to run many ASIC emulations at system speeds. Third in the hierarchy was density. Designers also indicated other reasons for not using programmable logic. These included too few I/Os, too low output drive, excessive board space requirements, poor radiation resistance, and no budget for software tools. Respondents indicated their preferences in this question by selecting a box, and many responded that multiple factors affected their decisions.

Figure 5-15
Factors Limiting Programmable Logic Use: North America



Source: Dataquest (June 1995)

Chapter 6
Product Trends: Japan

To develop and market ASIC products that are competitive in Japan, it is important to examine the integration levels used in ASIC designs for current-generation systems and plans for next-generation system designs. The ASICs designed in Japan provide a snapshot of regional design activity. This chapter was juxtaposed after the chapter on North America to allow the reader to understand how these designs compare to those from another region.

In this chapter, Dataquest explores the ASIC product trends in Japan. The first section looks at gate arrays and cell-based designs, while the second section examines PLDs. We further subdivided those sections covering gate counts, system clock speeds, and packaging when applicable. For a more in-depth understanding of the Japanese and North American markets, Dataquest suggests that the current and previous chapters be read together.

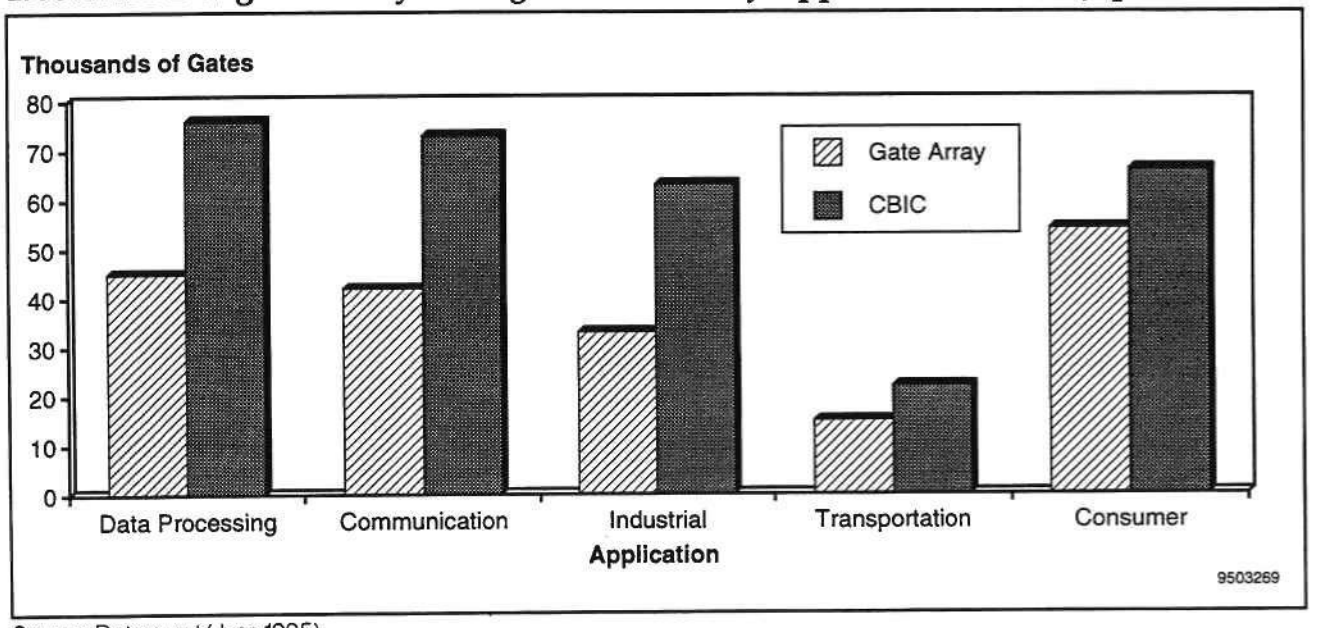
Gate Array and CBICs

The trend toward system-level integration and high-density design has been the thrust of the ASIC industry for some time and equally discussed by Dataquest in the past. To further quantify the design activity in Japan, Dataquest took a closer look at the trends defining and differentiating the use of gate arrays and CBICs.

Design Starts by Gate Count

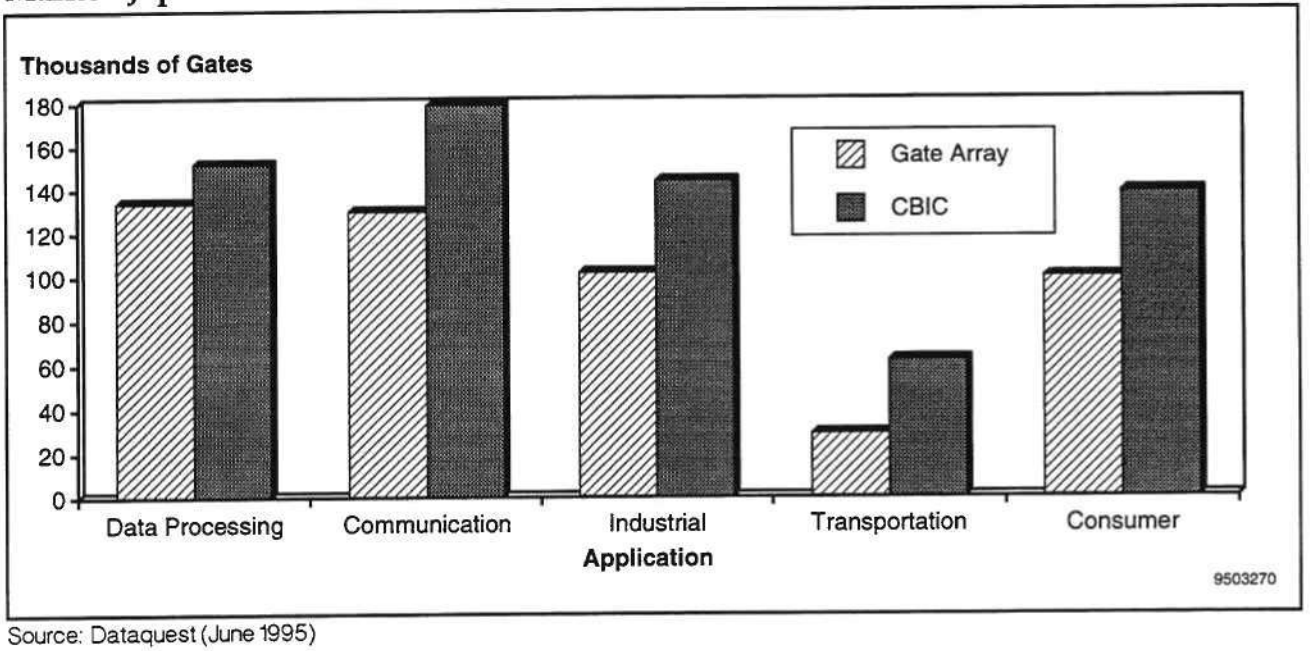
With maximum usable gates at over 1.5 million, the era of true system-level integration can be realized. But while the available densities reach that high, has actual design activity moved into that realm? To investigate design-size migration patterns, Dataquest asked respondents to indicate the average and maximum gate densities of their gate array and cell-based designs. Designers reported that the average gate array gate count moved to about 25,000 gates in 1994, and they expect densities to increase to 41,000 gates by the end of 1995. While gate array gate counts have been rising, many recent discussions have focused on the growth of CBIC gate counts. Figures 6-1 and 6-2 show the 1995 average mean and average maximum estimates by utilized gate count for gate array and CBIC designs by overall application markets. Both charts show a trend Dataquest has been discussing for quite some time—CBICs are leading gate arrays into the high-gate-count market. It is important to note that the designers in Japan, who have traditionally been gate array advocates, indicate that cell-based design will lead high-density design, making even clearer the shift toward preconfigured cell-type solutions. For cost, design reuse, power, and speed considerations, CBICs have gained popularity for high-density designs. Needless to say, this is a tremendous opportunity for suppliers that can facilitate this move. Those suppliers that can help the systems designers reach their goals will no doubt be credited as key members of the product development team.

Figure 6-1
1995 ASIC Design Starts by Average Gate Count by Application Market: Japan



Source: Dataquest (June 1995)

Figure 6-2
1995 ASIC Design Starts by Average Maximum Gate Count by Application Market: Japan



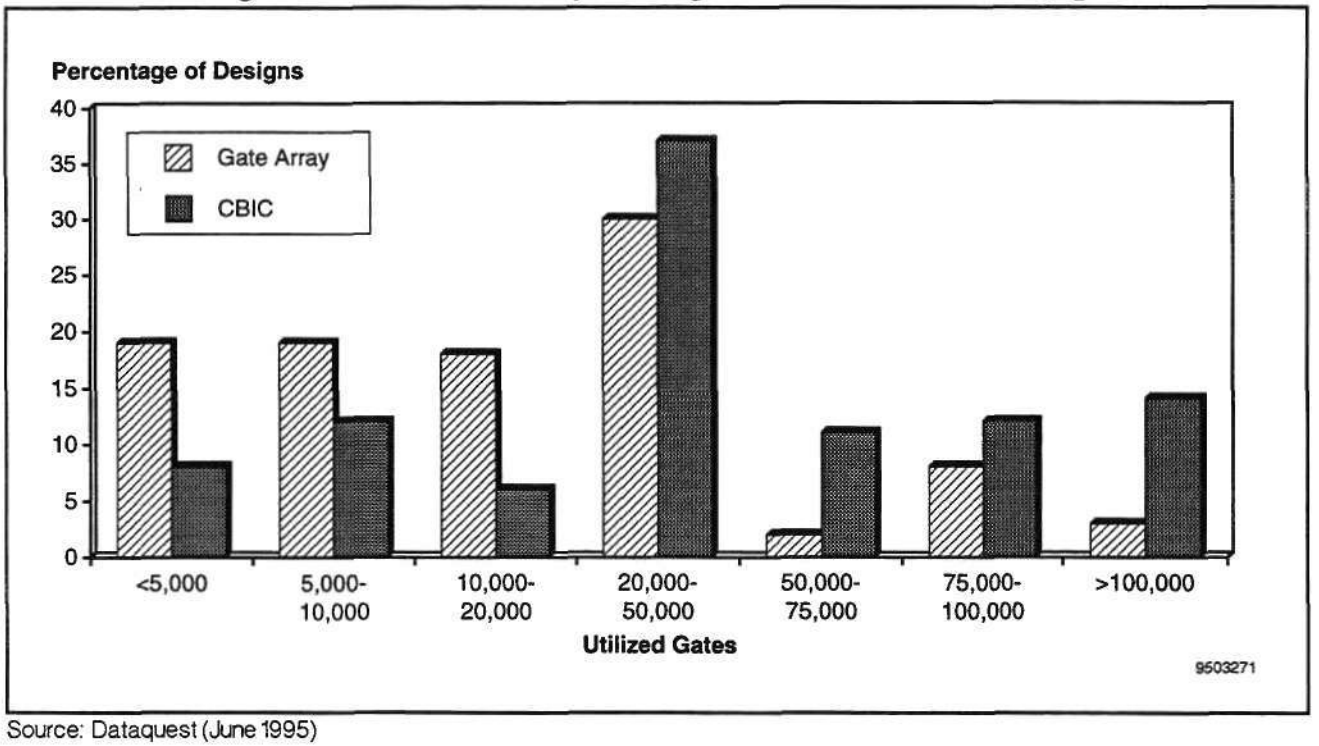
Source: Dataquest (June 1995)

Designers reported that the average CBIC gate count will climb to over 60,000 gates in 1995. Both the average and maximum gate sizes should grow healthily as increases in functionality drive more complex solutions onto a single die. Furthermore, Dataquest believes that large SRAMs (128Kb and 256Kb) will be diffused in the gate array base wafers and used for cache memory. Other functions such as SCSI, ALU, multiplier, multiplier-accumulator, FIFO, DMA controllers, cache controller, and 82XX microperipherals will also be diffused in the gate array and will drive the average gate counts upward.

Figure 6-3 shows the distribution of gate array and CBIC designs by average expected gate count in 1995. Like in North America, the designers in Japan were optimistic in their migration toward higher densities. Nonetheless, the trend needs to be understood, and Dataquest analysis of these figures reveals the following important points:

- Peak use for both gate arrays and CBIC designs is in the range of 20,000 to 50,000 gates.
- CBICs are expected to outpace gate array growth in the category of more than 75,000.
- Gate arrays dominate designs with less that 20,000 gates.

Figure 6-3
1995 ASIC Design Start Distribution by Average Utilized Gate Count: Japan



Source: Dataquest (June 1995)

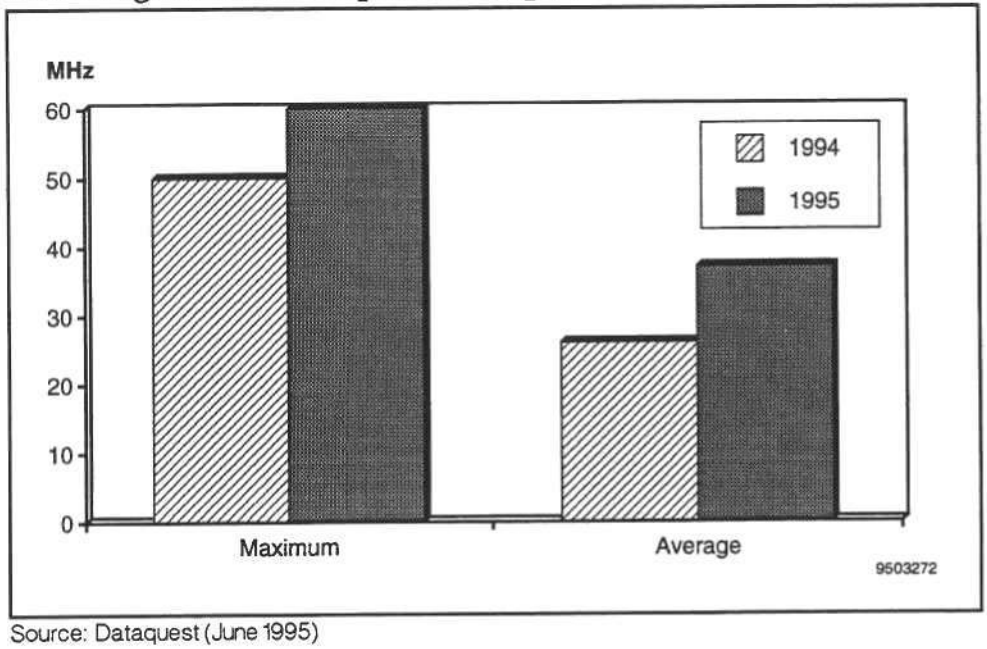
System Clock Speeds

Different applications need different features, and designers in Japan, which is dominated by a swelling consumer electronics industry, has not embraced the need for speed with both arms as designers have in North America. Nonetheless, speed requirements are still increasing, and the designers recognize that the designs of tomorrow will require higher and higher speeds. ASIC designers in Japan described the trend toward more speed: average speeds climbing slightly, and maximum speeds steadily increasing to higher levels. Figure 6-4 shows the increasing speed trend. The average ASIC design had a clock frequency of 26 MHz in 1994, which respondents believe will reach 37 MHz in 1995. The maximum clock, on average, will increase from 50 MHz in 1994 to 60 MHz in 1995.

Cell Libraries

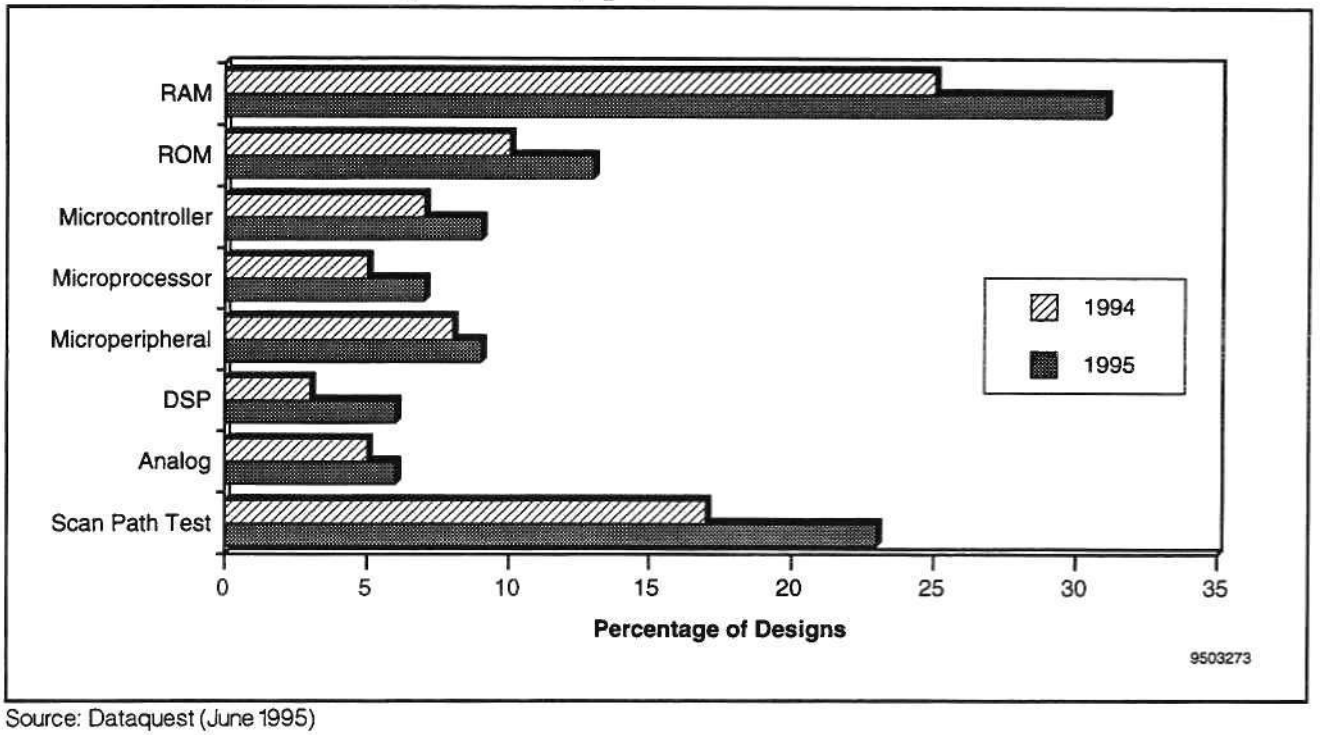
Cell libraries have arisen as an important way to differentiate suppliers. While some suppliers continue to operate on a pricing strategy, others focus on developing numerous cells to allow them to address a variety of user needs. Dataquest asked users to indicate which cells they used in their 1994 designs and planned for their 1995 designs (see Figures 6-5 and 6-6).

Figure 6-4
ASIC Digital Clock Frequencies: Japan



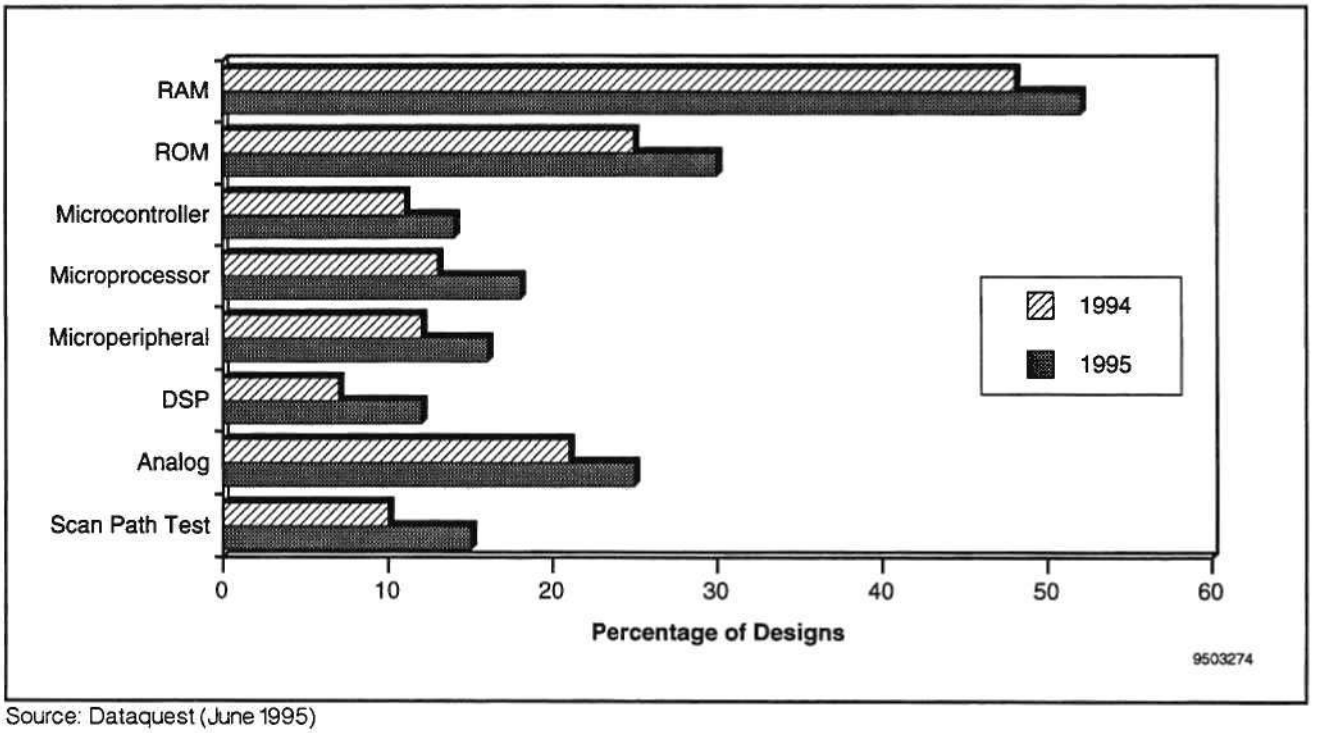
Source: Dataquest (June 1995)

Figure 6-5
Gate Array Design Starts by Cell Use: Japan



Source: Dataquest (June 1995)

Figure 6-6
CBIC Design Starts by Cell Use: Japan



Source: Dataquest (June 1995)

Important points about this data is as follows:

- RAM and Scan Path Test cells are the most popular cells for gate arrays.
- RAM is the most popular for CBICs.
- There is a rapid rise in on-chip microperipherals, primarily of the 82XX type such as DMA controllers.
- While cell use is increasing in both gate arrays and CBICs, the higher values for CBICs confirm that complex functions are more easily implemented in cell-based technology.
- Microprocessor cells, especially Z80s, have been popular in many applications, most notably, games.

Designers from Japan generally reported the same cell use trends as those in North America; however, there was discrepancy in the use of Scan Path Test. North American designs incorporated 20 to 25 percent more of these types of cells than reported in Japan. As pointed out earlier, the testability issue will increase in importance as the designers expand their expertise to accommodate higher densities.

Memory Sizes

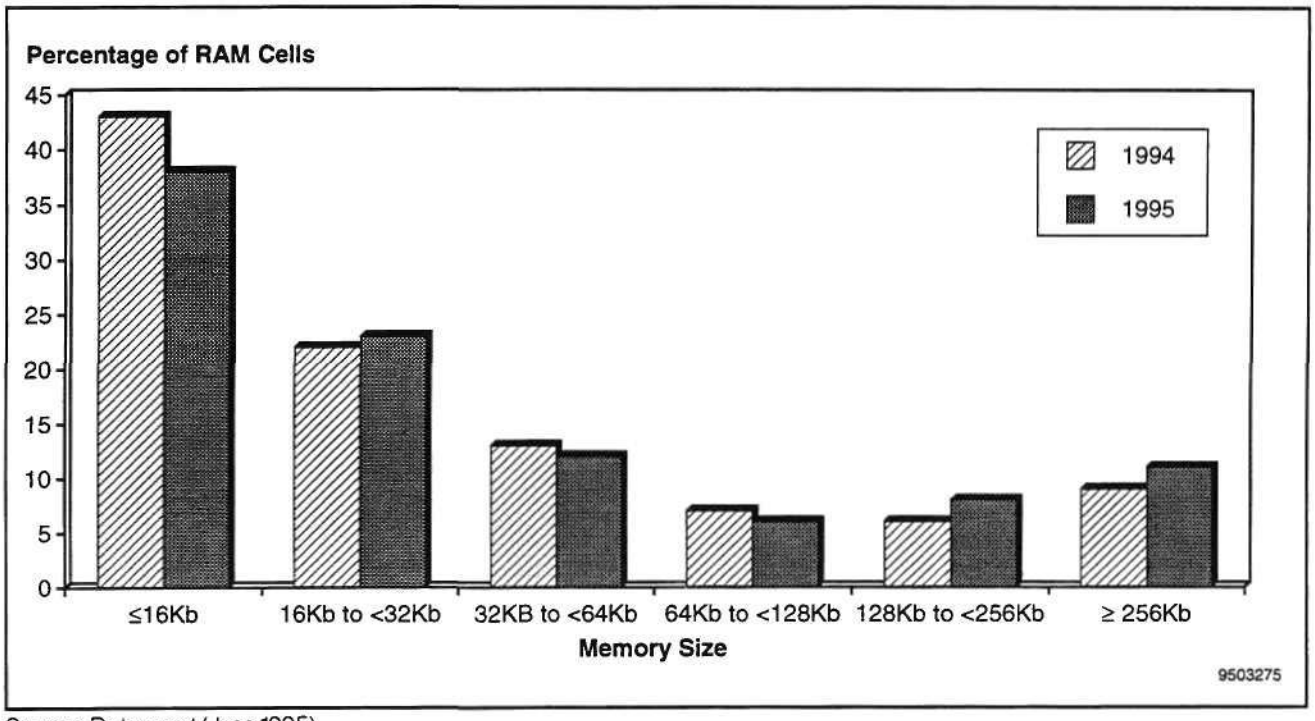
The size and amount of memory used in gate arrays has been increasing, and Dataquest asked designers in Japan to describe the trend. Users indicated that over 40 percent of the designs in 1994 used memories less than 16Kb (see Figure 6-7). However, design starts using the glamorous large SRAMs of 128Kb or larger surpassed 15 percent of those design starts in 1994. Users indicated that they would be increasing their use of SRAM in 1995, where the use of over 256Kb will exceed 10 percent in 1995. Data processing caches, telecommunications data buffers, and increasing use of embedded memories in consumer products continue to drive these figures.

Packaging Trends

Packaging Types

While increasing densities, speed, and cell use have been constantly mentioned throughout this report, the packaging factor acts as an invisible conduit through which the increased functionality is supposed to work. Packaging improvements arise every day, and today's standard quickly becomes tomorrow's old news. The hot package one year may be on the decline the next, and favorite packages in Japan may have reduced acceptance elsewhere. Such is the case when comparing package use in Japan with that on North America. A quick perusal would find that a noticeable gap exists between the two regions when looking at high-pin-count packages. The lesson to be learned from this gap is that designers in Japan have not focused as much energy into large designs as North American designers. The cause could be both cost and time-to-market issues, but the challenge now arises for suppliers to introduce, promote, and support higher-density designs as viable alternatives with complementary packages. The successful vendor that accomplishes this will not only bring the systems company into a greater competitive position, but it will also reap the rewards of experience and customer loyalty on the competitive edge.

Figure 6-7
Gate Array Design Starts by Total Memory Size: Japan

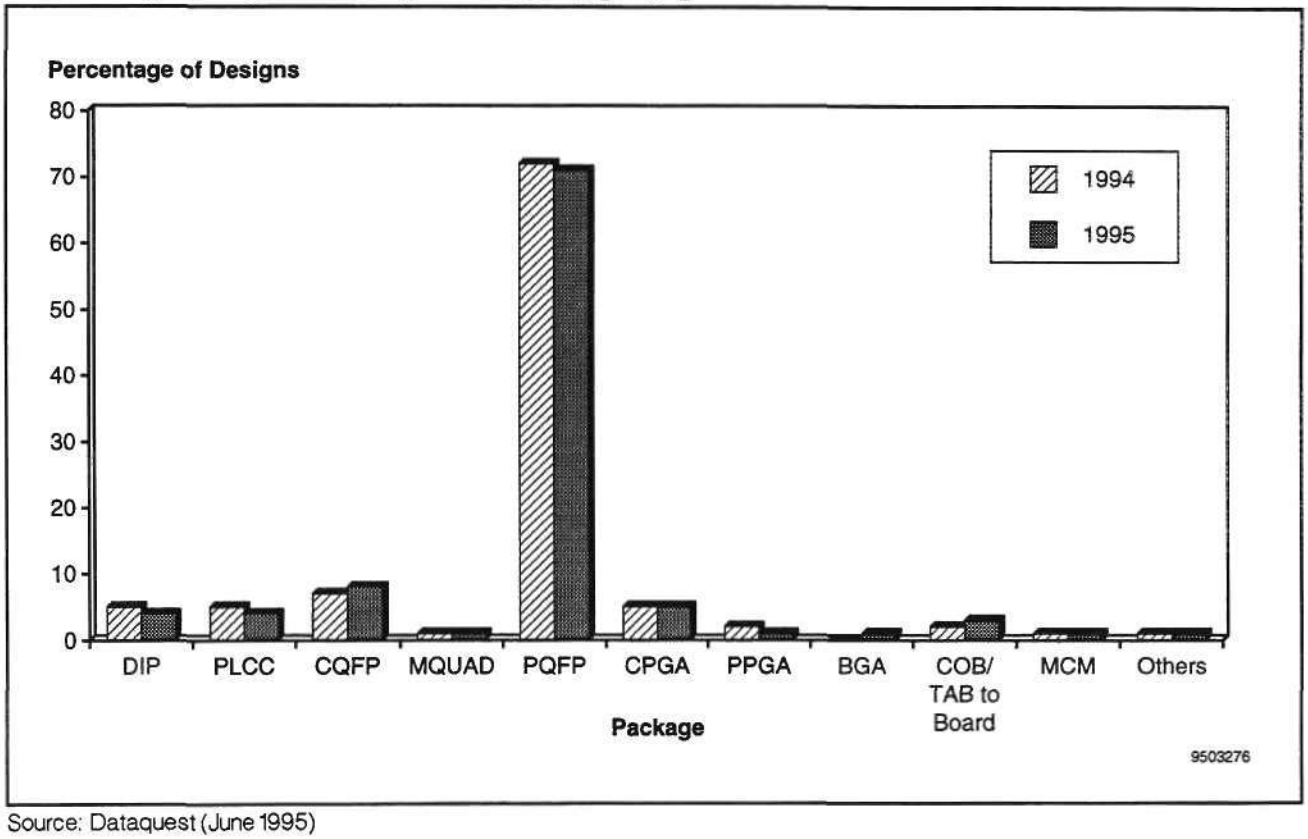


Source: Dataquest (June 1995)

One of the economic hurdles that suppliers will have to overcome is the extensive relationship and attachment that the designers in Japan exhibit toward the PQFP. The PQFP has seen extremely high use across all application markets, with no single market being the stronghold for that package type. In North America, the PQFP was favored only in selected areas. While there are definite economic advantages to adhering to a single package type, there are advantages, sometimes even economic, to migrating to other package types.

Figure 6-8 shows the packaging trend for the near future. With the introduction and ramp-up of thermally enhanced QFPs, designers have targeted their designs in the more efficient packages, effectively extending their popularity. However, as high I/Os become an issue, the PQFPs will become less feasible as design solutions because bent leads and handling problems arise with fine-pitch QFPs. Clearly, designers in Japan have not run into this problem by either keeping design densities down or by clever engineering to avoid that particular situation. Pin Grid Arrays have not been a factor as through-hole design requirements conflict with the surface-mount designs. To maintain the surface-mount design savings, many vendors in North America have begun to look closely at the Ball Grid Array – which provides the benefits of surface-mount technology, required I/Os, and a self-aligning benefit. While BGA technology has clearly been gaining momentum in North America, Japan has seen little action in that package. For 1994, designers in Japan have sparingly planned to design-in the BGA, while designers in North American indicate that they will have five times the design activity in the BGA than what designers in Japan indicated.

Figure 6-8
Gate Array Design Starts by Package Type: Japan



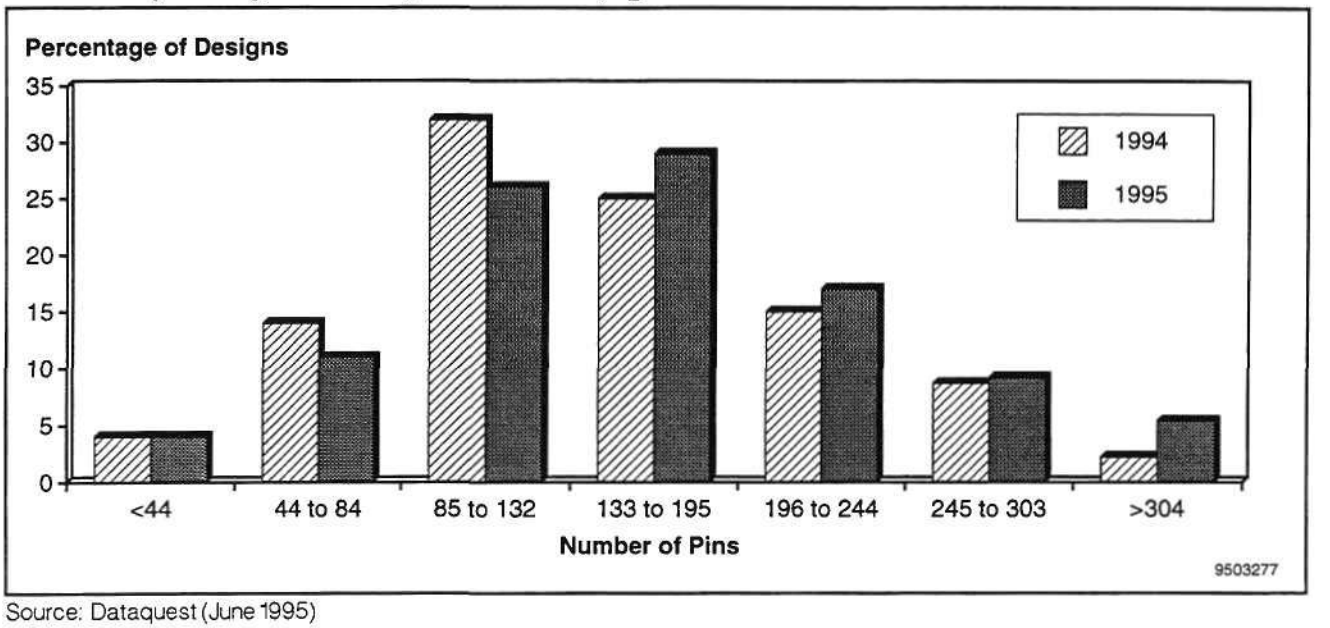
Source: Dataquest (June 1995)

Pin Counts. As ASIC designs increase in size and complexity, the packages must be developed that enable full access to the ASIC's functionality. By analyzing the package use in Japan, it is evident that the quick-concept-to-production reputation Japan is famous for has enabled it to standardize on a single package type while also keeping them from the forefront of packaging technology. Dataquest asked users to estimate the percentage of designs using different pin counts. Figure 6-9 shows how users responded. Looking at 1995, the pin-count range of choice is 133 to 195, apparently revealing that designs from Japan lag those from North America in terms of I/Os. Further analysis indicates that the designs are shifting away from the low end of the range. A great example is the 5 percent of designs slated for packages at 304 and more pins.

Programmable Logic

PLDs have penetrated every major regional market but has its own special dynamics in Japan. Because of the ability to turn gate arrays quickly and the perception of high price, FPGAs have not garnered as much favor as their other kindred, namely CPLDs. The PAL-like architecture of CPLDs has made it easier for designers in Japan to understand the implementation of CPLDs. Based largely on this ability, CPLDs have enjoyed greater visibility and design success in Japan.

Figure 6-9
Gate Array Design Starts by Pin Count: Japan



Source: Dataquest (June 1995)

Development Seats

To get a better understanding of PLD use, respondents were asked how many development seats their teams had. Respondents indicated that the average number of PLD development seats per team was 2.7. With an overall average team size of 17, this would indicate a situation where sharing seats is required or where teams have a designated PLD staff member. A typical development seat was responsible for over 10 designs per year, though higher rates were not uncommon.

Device Use

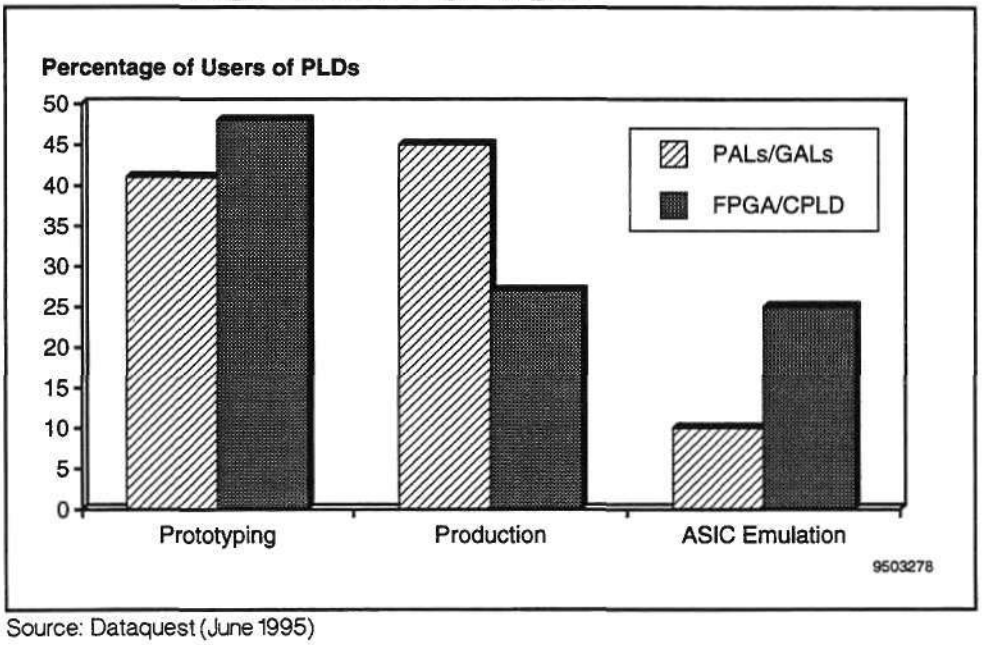
Dataquest investigated the uses for both simple PLDs (PAL- and GAL-class devices) as well as for high-density devices (FPGAs and CPLDs) in Japan. While a significant portions of PLDs are used for prototyping, Figure 6-10 shows that 45 percent of simple and 27 percent of complex PLDs are used for production.

While the prototyping figures are comparable between North America and Japan, there are larger differences in the emulation and production categories. The emulation use in Japan averages nearly five percentage points greater in Japan than in North America. This is again a strong indicator of the quick prototyping and cost-conscious atmosphere in Japan. Similarly, ASIC emulation facilitates concurrent design that has been proven to reduce cycle times and cut costs. The lower use of PLDs in production is a testament to the low-cost drive of designers in Japan and the lingering perception that PLDs are big-ticket items.

High-Density PLD Designs by Gate Count

Glue logic has definitely felt the bite of programmable logic, but the question remains: Have PLDs captured designs of higher complexity? Gate array and PLD suppliers need to look at the designs captured by programmable logic to properly plan their product rollouts. Dataquest asked users

Figure 6-10
1994 Use of Programmable Logic: Japan



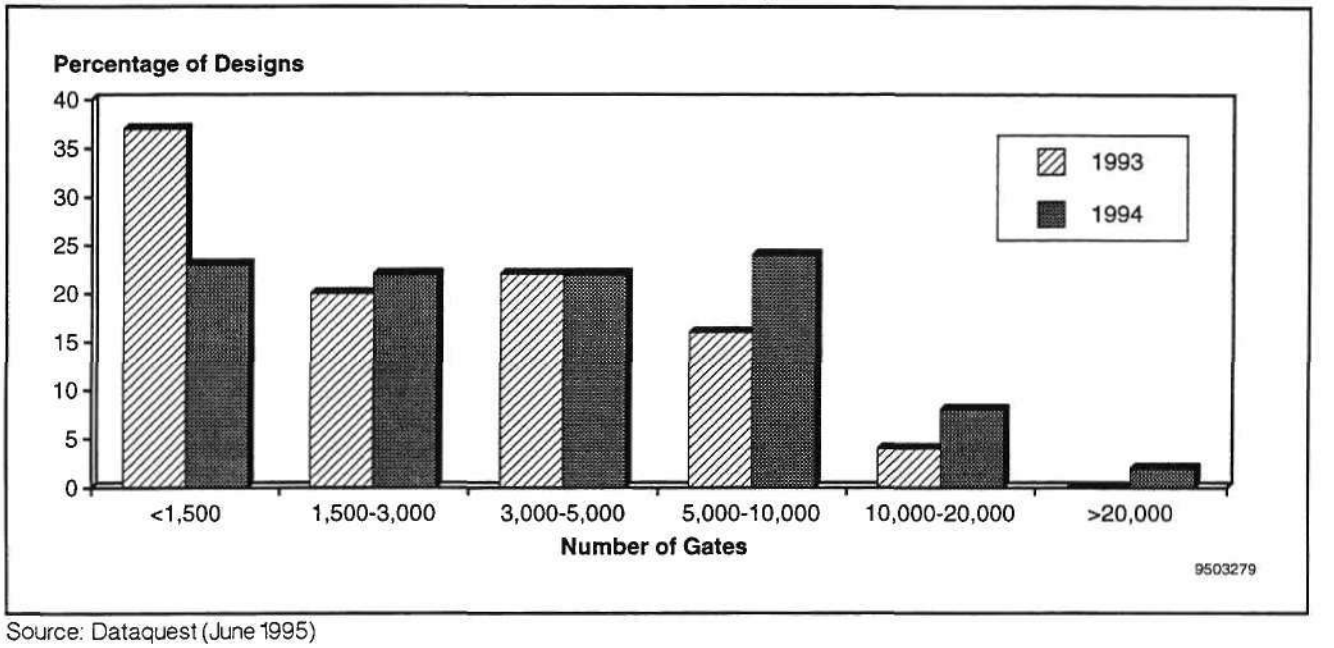
Source: Dataquest (June 1995)

to indicate what percentage of their designs fell into respective gate ranges. Figure 6-11 shows that while the category of less than 1,500 gates was the most popular in 1993, the most popular density for programmable logic in Japan is the range of 5,000 to 10,000 gates in 1994. This is followed by less than 1,500 gates. Apparently, the distribution flattened out through 1994, indicating that designers are comfortable with lower-density and higher-density designs. The workhorse designs were on the low end in 1993, where PLDs are maturing and the most cost-competitive with non-programmable solutions. In 1994, the increased confidence and use of programmable logic in prototyping and emulation has pushed design start densities up. However, the small number of designs with greater than 10,000 gates is relatively small, suggesting that the price of the higher-density parts may play a big role in determining use.

Implementation and Limiting Factors

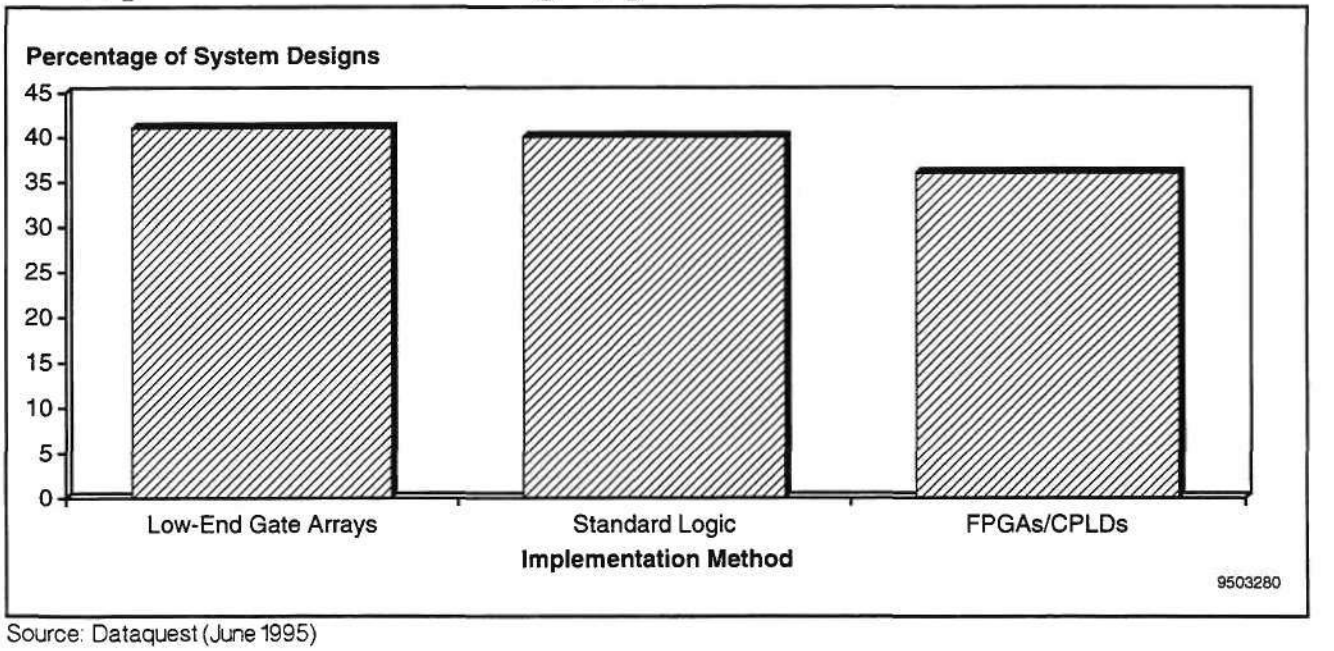
Dataquest asked users to indicate how they implemented small amounts of random logic (see Figure 6-12) to see how this has impacted system design. Users indicated that about 40 percent of systems used standard logic for the implementation while over 40 percent responded that gate arrays were used. Just above 35 percent of designers responded that they already used high-density programmable logic for the implementation. With low-end gate array and standard logic use so high in Japan, suppliers should target the great opportunity there. It is important to note that designers indicated that they often used a combination of devices to implement random logic, and, therefore, PLDs and standard logic could coexist on the same board. Similarly, designers were not asked if their response was limited to volume production solutions, so it is likely that the programmable logic may have been used in prototyping and preproduction.

Figure 6-11
High-Density PLD Design Starts by Gate Count: Japan



Source: Dataquest (June 1995)

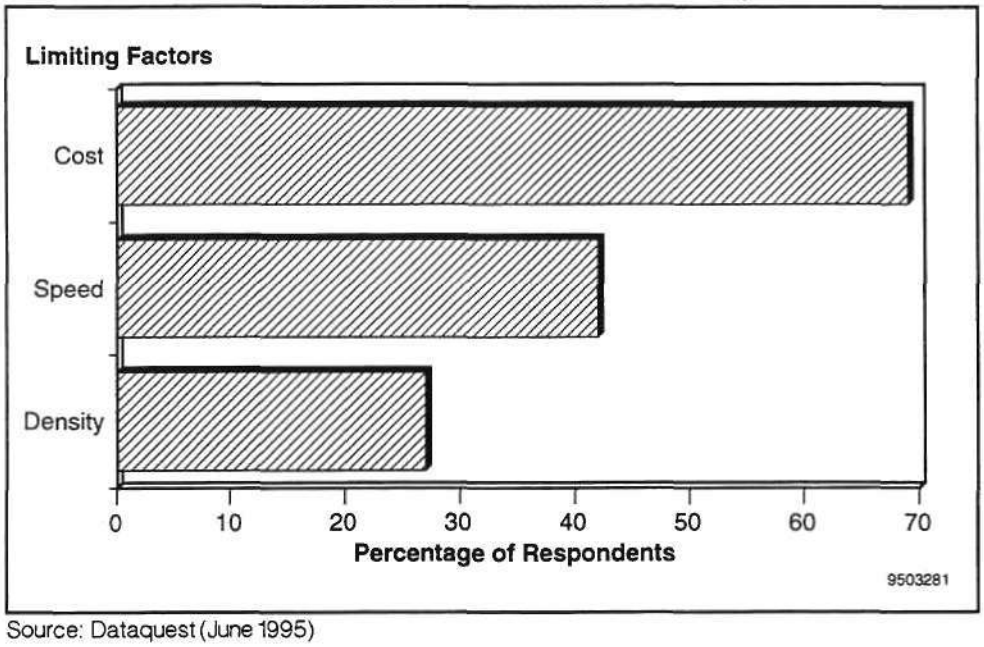
Figure 6-12
1994 Implementation of Random Logic: Japan



Source: Dataquest (June 1995)

What prevented the use of programmable logic? Dataquest also asked users to explain why (see Figure 6-13) they did not use it. It turns out that cost was the No. 1 reason designers did not implement programmable logic. In fact, it appears that cost may be the only issue for some, limiting their scope and narrowing their vision away from programmable logic solutions. In fact, nearly 70 percent of respondents reported that cost was the biggest factor slowing programmable logic's acceptance in Japan. Next most important was speed, a problem designers have raised their voices about as they have been unable to run many ASIC emulations at system speeds. Third in the hierarchy was density. Designers also indicated other reasons for not using programmable logic. These included board space requirements, too high power requirements, and no budget for software tools. Surprisingly, some designers reported that they did not understand, did not have access to information about, or had difficulty programming their PLD solutions. Respondents indicated their preferences in this question by selecting a box, and many responded that multiple factors affected their decisions.

Figure 6-13
1994 Factors Limiting Programmable Logic Use: Japan



Source: Dataquest (June 1995)

Chapter 7
Dataquest Conclusions

The users have spoken, and suppliers should listen. There have been many noteworthy issues made clear by user perceptions, evident from the survey results. The major findings are as follows:

- Cost reduction remains the driving force for market success.
- CBIC use is on the rise in leading high-end products.
- On-chip memory use and bit requirements are on the rise.
- Megacells are playing increasingly critical roles.
- BGA packages are gaining significant momentum.
- Demand for 3V products is growing, but more slowly than previously believed.

Systems designers came out waving the flag of cost reduction in Dataquest's last ASIC user survey. This result suggested that time to market, the No. 1 factor for market success worldwide, no longer was the primary marching order for determining market success. In this year's continuation of the survey, users suggested that the market dynamics have not changed what determines success. Process engineers and product planners have already reduced the design cycle to terms that are acceptable. Extensive effort in this area may lead to diminishing returns and higher costs as a premium for faster turnaround time.

Reduced time to market and increased functionality were also key factors in both Japan and North America. Competition in the IT industry has designers pushing design cycles down while boosting the level of functionality per system. As a result, designers have turned to ASICs for leading-edge differentiation while keeping costs reasonable. So, while the system prices remain nearly the same, the familiar phrase "what do I get for my money" has driven the idea of value deep into the hearts of designers and even deeper into the margins of the semiconductor vendors.

The cost and functionality concerns that designers iterated can clearly be addressed by cell-based design. Similarly, cell reuse in CBICs has been proven to speed large designs to market. As design ability increases and tools facilitate the placement and stitching of cells together, Dataquest expects CBICs to play an important role in enabling high-density design with system-level integration to become a reality.

This current trend was also supported by the designers in our survey. Across the board, CBICs were leading the charge toward higher density and integration. As designers suggested in earlier chapters, gate arrays will dominate the low- to midrange-density designs while CBICs capture more designs in the category of more than 100,000 gates. What makes these high-density designs feasible for CBICs is the stitching together of functional cell blocks. By placing and connecting functional blocks and megacells, designers can quickly provide the desired functionality while quickly boosting gate counts.

Thus cell libraries become the remaining differentiator in the cell-based arena. In North America, suppliers targeted specific application markets and worked with designers to build significant cell libraries. Because of this movement, vendors can compete by meeting customers' needs with optimized cells. As Japan is making a stronger thrust into cell-based design, we expect these cells to become fundamental building blocks for designing complex products. A stark example of this is the amount of integration that can be seen when comparing gate array to CBICs in North America and Japan. Designers in North America reported that while they expected gate array designs to reach over 50,000 gates in 1995, they also claimed that cell-based designs would exceed 90,000 gates. Designers in Japan reported that while they expected gate array designs to reach over 40,000 gates in 1995, they also claimed that cell-based designs would soar past 60,000 gates. While those numbers may seem optimistic, designers in both regions indicate that cell-based design densities will outstrip that of gate arrays—no bones about it.

One cell used in CBICs and gate arrays is memory. The new research in this year's survey indicated that the majority of designs used less than 16Kb of total memory. On the other hand, memory use is growing, and designers in both regions reported that memory use in general and memory densities greater than 128Kb are also on a healthy ramp. The implementation of such large amounts of memories will require optimized memory cells for both the cell-based and embedded array designs. Another implementation (that is, traditional arrays) will severely inhibit design efficiency.

The design and implementation of megacells is also gaining importance. Beyond the use of large memory blocks, Dataquest added a question investigating the implementation of microprocessor cells. Users indicated that microprocessor cell usage was an integral part of their system design; later information suggested the same for microcontrollers. 68xxx, MIPS, ARM, and DSPs are finding their way on-chip as functional integration collapses the chip count.

Increased functionality and high densities can often translate to more I/O requirements. Combine that with high-frequency switching, and package choice is a major issue. Since cost was a driving factor, the use of 160 and 208 quad flat packs would appear to be the natural choices for cost reduction; however, the high-density designs often require high bandwidth, and the extra-wide buses can push I/Os to the upper 200s and above. Survey respondents suggested that pin counts were rapidly rising, and along with it, the use of BGAs in North America. In fact, design starts in BGAs climbed from 3 percent in 1994 and is expected to pass 9 percent of designs in 1995. BGAs address many of those problems designers have been facing, and the newer chip-scale versions address associated issues of board real estate.

Low- and mixed-voltage ASICs are on a design ramp but not nearly as rapidly as earlier believed. The push toward "green" PCs and other low-power products created an atmosphere that convinced designers that low-voltage products would hit like a tidal wave. Now that the hype has died down, the intricacies of low- and mixed-voltage design as well as the economics have hit home. No doubt, mobile computing and size-conscious

consumer applications have begun to affect the design of today's ASICs and will play a larger role in the ASICs of tomorrow. However, the sluggishness of the peripherals market to adopt low-voltage signaling technology and the economics of 5V DRAMs have kept up demand for 5V products. As result, designs go where the dollars are, and while low- and mixed-voltage designs are expected to increase, 5V designs still represent the lion's share of activity.

Supplier Recommendations

ASIC users want and need higher-density ASICs for their next-generation system designs. This presents a great opportunity for ASIC suppliers that can supply the right value.

First of all, ASIC suppliers must address the base needs of their clients. They must be able to meet cost, functionality, and time-to-market requirements. Without these basic elements, they must strive harder to create perceived value. Second, above understanding their clients' needs, suppliers need to understand their relative positions and take action to increase and/or maintain competitiveness. One such example is to maintain and support the libraries for 5V ASICs, which will extend for about two more years.

An important area to improve is testing. ASIC testing is generally on the rise because of the inclusion of larger functional blocks on-chip. As densities increase, the margin for error must decrease, or the absolute error rate in units will grow. This is unacceptable, and to ignore the problem would hold technology back to the implementation of single functions on single chips, a state that many ASIC vendors left behind years ago. To move forward, suppliers need to review innovative testing methodologies that add little real estate penalty or no performance hit and implement them to ensure that increasing densities are reliable.

Amid the rash of price cuts and low-cost bidding, ASIC suppliers need to focus on a differentiation strategy. As mentioned earlier, cost has been the great equalizer, so a cost-cutting strategy may do even more harm than good because most ASIC suppliers offer similar process technologies, design tools, and/or design density. This low-cost strategy can help gain short-term market share but requires very low overhead, reduces margins, and can result in long-term lack of focus and loss of profitability. Another way to differentiate is building focused cell libraries. Earlier, we described the growing importance of cell libraries and how they need to gain momentum. For this to occur, suppliers must work closely with their customers to determine which cells to develop and the best cell mix for each application. The suppliers that do not do so may quickly find themselves designed out of a client because of archaic or unwanted technology.

A combination of these factors suggests that suppliers should also focus on the design environment. Besides being able to support both VHDL and Verilog, which are both on the rise, suppliers need to further examine the cell library portion on the tool equation. Even if HDL use increases and synthesis efficiency cuts design time and cost, there will still be a problem because of a lack of competitive cells. In North America, cell use is high and on the rise. On the other hand, cell use in Japan is rising, but it is still comparatively low. The gap will decrease with proper planning and

execution, but the cell functionality gap can serve to win more business only for those with better, up-to-date cells.

However, an independent effort to develop cells may seem like a costly venture with no guaranteed returns. A more appropriate approach is to work closely with systems designers to develop optimal cells for their ASIC designs. These cells can then be leveraged for reuse in other designs – increasing reuse, and decreasing design time. The reusable cells, as part of an ASIC library, can be used to develop application specific standard products (ASSPs) for a small investment. Hence, the ASIC-to-ASSP link also becomes a factor in revenue generation, cost reduction, and fab filling.

The low-cost model of ASSP development may seem an economical choice, as the standard products can be used by multiple system suppliers. But before ASIC suppliers decide to place all their eggs in the ASSP basket, they must be sure to maintain the ASIC relationship. The ASIC development is what will give the supplier the competitive cells and advantage. Similarly, we have seen system suppliers that actually benefit from the ASIC cost model as opposed to the ASSP route because the technology is optimized for their architecture. Hence the system is tuned to the ASICs for performance, as opposed to the system being compromised on performance to save cost by using standard parts.

The opportunity for improvement spans a plethora of issues. Although they might like to, no single supplier can afford to spend the R&D to develop the best software, best process technology, and best cell libraries alone. In order to effectively take advantage of the opportunities available, suppliers should look into strategic partnerships to build their competitive advantage. On the process side, manufacturers have been forced to look to partnerships to defray the high costs of leading edge submicron technology. Similarly on the software side, suppliers need to form tighter alliances with EDA companies from both Japan and North America to gain continued access to the leading-edge mapping, testing, and synthesis tools. All suppliers should be paying close attention to the recent series of mergers and acquisitions in the EDA market. The third-party tools have become a formidable force in the North American design cycle, making supplier differentiation a critical factor.

User Recommendations

As Dataquest believes that suppliers will become more focused to address particular markets, users must also enter the equation, forging relationships with those suppliers and growing together with the particular application. To choose the particular supplier, Dataquest encourages users to compare vendors on a variety of strengths, including tools, processes, packaging, test capability, cell libraries in their application area, system focus, system expertise, and service and price.

This book reveals an opportunity for suppliers and systems designers to come together and propel ASIC technology to the forefront of competitive market. Dataquest believes that users should pay more attention to industry analysis and company benchmarks regarding supplier capacity, capabilities, and rankings. ASIC designers must set up internal benchmarking as well as examine all independent third-party evaluations of their

suppliers. Furthermore, we advise users to continue monitoring all designs and suppliers on a timely basis. Competitive systems require competitive ASIC suppliers, and users need to work with those suppliers that can deliver competitive products. ASIC suppliers provide the critical key to differentiating users' systems, and users should place their bets wisely.

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