Semiconductor Equipment and Materials Service Newsletters 1989

Dataquest

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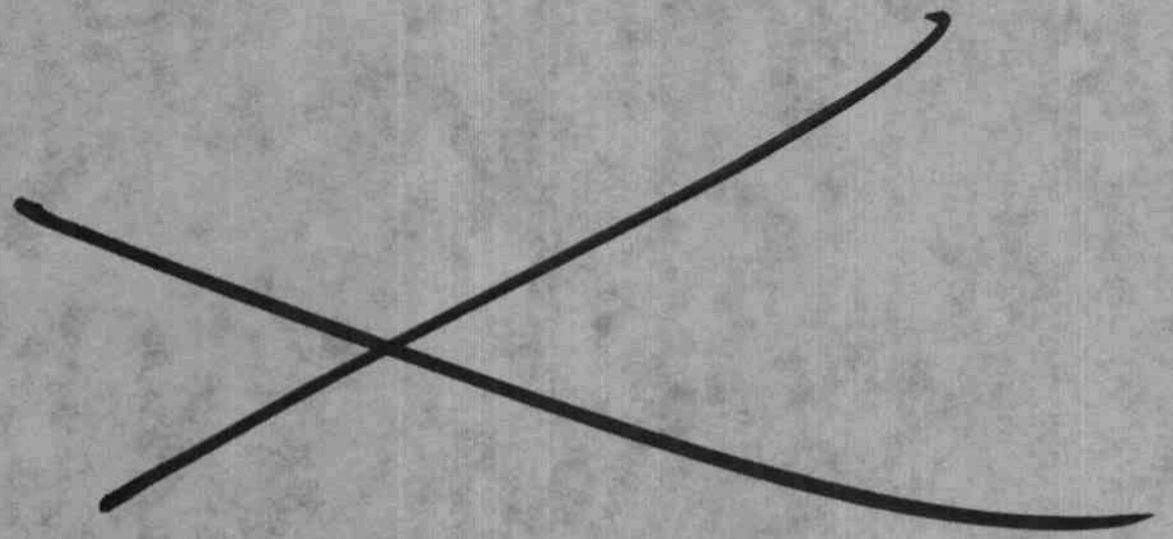


1989 SEMS Newsletters and Bulletins

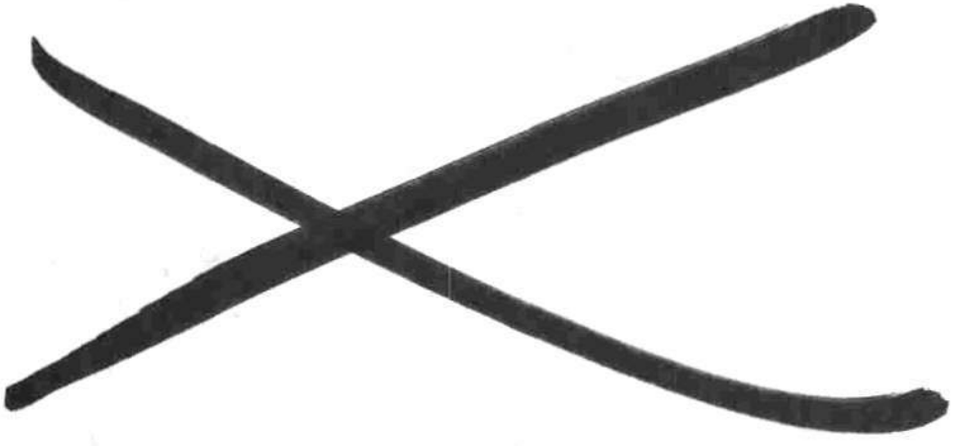
Table of Contents

1989 SEMS Newsletters and Bulletins

TAB	TITLE	MONTH
Capacity	Scaling the Heights: Will Asia/Pacific Surpass Europe as a Center for Semiconductor Production?	June
Industry Issues	High-Tech Business Opportunities in India	June
Equipment Data Base	1988 Wafer Fab Equipment Regional Market Shares	June
Semiconductor Materials	Silicon Wafers: Existing Markets and Future Opportunities	June
Capacity	DRAM Supply Wild Card - Samsung To The Rescue	July
Equipment Data Base	Closing The Gap: Will Japan Become The World's Largest Producer of Fab Equipment?	July
Process Control	CD & Wafer Inspection Equipment: 1988 Was a Very Good Year	July
Industry & Technology Trends	The ASIC Package Proliferation	July
Deposition	Technology-Driven Expansion of the CVD Equipment Market	July
Industry Issues	What's Really Going On At SEMATECH?	August
Trade Shows	SEMICON/West 1989: Taking The Pulse Of The Equipment Industry	August
Deposition	1989 VLSI Multilevel Interconnect Conference How do The Techologies Stack Up?	September
Industry Issues	Make Room Semiconductor World - Here Comes South Korea and Taiwan	October
Industry and Technology Trends	Integrated Processing Technology In A Standardized Market Environment	October
Industry and Technology Trends	Globalization & Concentration of the Wafer Fab Equipment Industry	October

1989 SEMS Newsletters and Bulletins

TAB	TITLE	MONTH
Capacity	Europe 1992: A Model Industrial Policy For The Semiconductor Industry?	December
Forecast	Wafer Fab Equipment Forecast: The Near-Term Outlook	December
Semiconductor Materials	Tungsten Hexaflouride: A Market In Transition	December



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Research *Newsletter*

DUN & BRADSTREET'S ECONOMIC OUTLOOK FOR 1988 THROUGH 1990

SUMMARY

The U.S. economic outlook for 1989 indicates slower growth but no recession. The Dun & Bradstreet Corporation, Dataquest's corporate parent, forecasts an economic downshift starting in the second half and continuing into 1990. However, corporate spending for capital equipment, including computers and telecommunications, may not be greatly affected.

The Dun & Bradstreet Dun's 5000 survey on capital spending indicates that most companies plan to maintain or increase their capital expenditures, supporting a trend of the past three years.

A synopsis of Dun & Bradstreet's economic outlook and capital spending survey results is discussed in the following paragraphs.

ECONOMIC FORECAST

The year 1989 will most likely see slower economic growth than 1988. Weaker contributions to GNP gains from the government and trade sectors and higher interest rates are to blame.

Despite this weakness, no recession is anticipated. In 1989, growth in real GNP should slow from 1988's estimated 3.8 percent to about 2.5 percent. In 1990, the slowdown will continue with a 1.3 percent growth rate, largely as a result of a poor jumping–off point at the end of 1989.

Farm production during the last three quarters of 1988 was adversely affected by the drought in many parts of the country. However, with these climatic conditions behind us, a surge in real GNP will result in the first quarter of this year.

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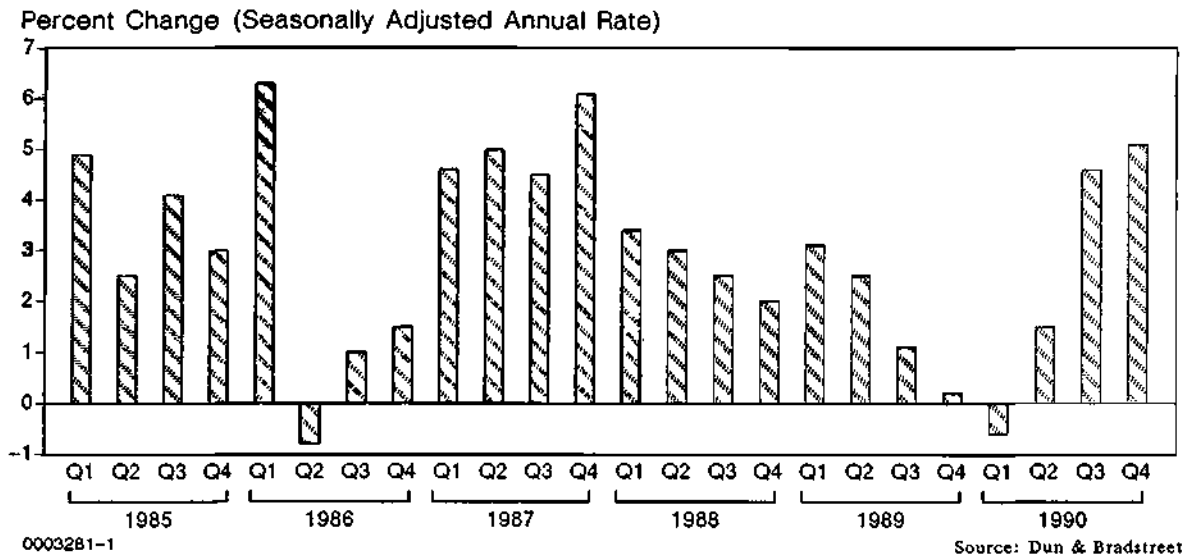
Thereafter, a host of negative factors will come into play, leading to decelerating growth in the remainder of 1989 and through the first half of 1990 (see Figure 1). After these factors have run their course, the economy will resume the moderate-to-strong growth rates that were last seen in 1987 and early 1988.

Figure 1

Gross National Product Growth
(1982 Constant Dollars)



The key factors influencing the economy's short-run performance are as follows:

- Government/fiscal policy
- Interest rates/monetary policy
- Consumer spending
- Capital spending
- Trade/foreign sector

These factors are examined in the following paragraphs.

Government/Fiscal Policy

The fiscal 1989 budget is in place, and, with few exceptions, is largely a clone of the fiscal 1988 budget. In the fiscal 1990 budget, the Bush Administration will stress spending cuts rather than tax increases, although new user fees, excise taxes, and already legislated tax increases appear likely to be included. As a result, the first budget of the Bush Administration will see negligible real growth, if any, in defense and nondefense spending.

Interest Rates/Monetary Policy

By recently raising the discount rate to 7 percent, the Federal Reserve Board has made its strongest statement yet of its determination to hold back inflation. The Fed's tight monetary policy has created a situation in which some short-term interest rates are higher than long-term rates. Experience shows that when this situation persists, economic weakness usually follows. The Fed will maintain its severe anti-inflation policy until it is satisfied that inflation is not accelerating or that recession is on the horizon.

Consumer Spending

Real consumer spending grew 2.8 percent last year and is expected to grow about 2.0 to 2.5 percent in 1989. Expenditures on durable goods are highly interest rate sensitive, and therefore will show less growth this year because of higher rates. But considering that durables account for only 15 percent of all consumer purchases, this slowdown will not have much of an economy-wide effect. Nondurable goods, which account for about one-third of consumer spending, are relatively insensitive to changes in incomes. So, cutbacks in this area will also likely have only a minor effect on the economy. Finally, the diversity of the services category ensures that overall growth of consumer spending in services should be maintained.

Capital Spending

Firms' capital spending plans that are in place are unlikely to be changed by recent interest rate movements. However, the combination of higher interest rates, a stabilizing dollar, and slightly reduced consumer spending likely will adversely affect longer-term capital spending plans that have not been finalized. Real business fixed investment grew 9.5 percent last year, and it is expected to slow to 3.6 percent growth this year and to further slow to 1.6 percent growth in 1990.

Trade/Foreign Sector

Minimal improvement in the trade balance is expected. Capacity constraints among several traditional export industries will make it difficult to expand production. Adding to this, higher interest rates will discourage capacity expansion. These factors, combined with a stabilizing dollar, will dampen continuation of last year's export boom. Meanwhile, demand for imports will likely shrink by a small amount in response to modest consumer and business spending cutbacks.

DUN'S 5000 SURVEY RESULTS

The Dun's 5000 survey has been completed and the results can be summed up in a word—optimistic. The outcome of this survey illustrates a continuing positive trend in capital spending and, in particular, in budget allocations for computers and telecommunications equipment.

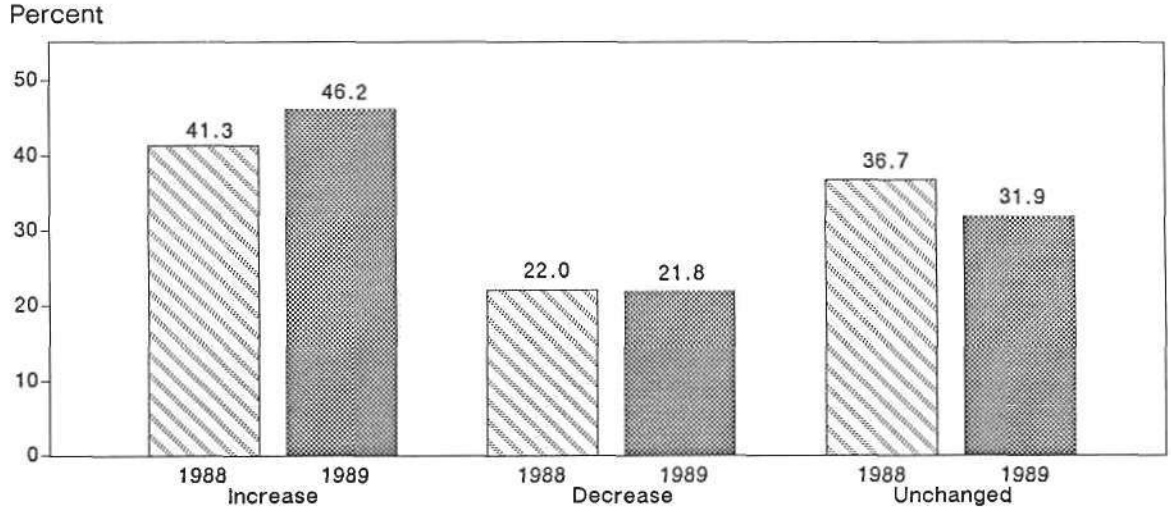
Dun & Bradstreet's Dun's 5000 survey is based on a sample of companies that is statistically representative of the distribution of companies by size in the U.S. economy. The 1989 planned capital spending reflects even greater optimism than was seen in 1988 (see Figure 2). Of the companies surveyed, 46.2 percent plan an increase in capital spending, compared with 41.3 percent one year ago. Plans to decrease capital spending in 1989 were slightly lower than those for 1988—21.8 percent and 22.0 percent, respectively.

According to The Dun & Bradstreet Office of Economic Analysis, the capital spending patterns of 1988 are expected to continue through most of 1989, sustaining an upbeat trend. In 1988, 27.1 percent of companies spent more than planned. The previous year, 25.0 percent of the surveyed companies' actual spending exceeded plan (see Figure 3).

The 1989 capital spending budgets of companies surveyed show that a larger percentage of their budgets is being allocated for computers and telecommunications equipment compared with 1988 (see Figure 4). Although most companies, regardless of size, continue to allocate less than 10 percent of their budgets to computers and telecommunications equipment, the positive shift is toward spending between 11 and 50 percent.

Figure 2

Capital Spending Plans
1989 versus 1988



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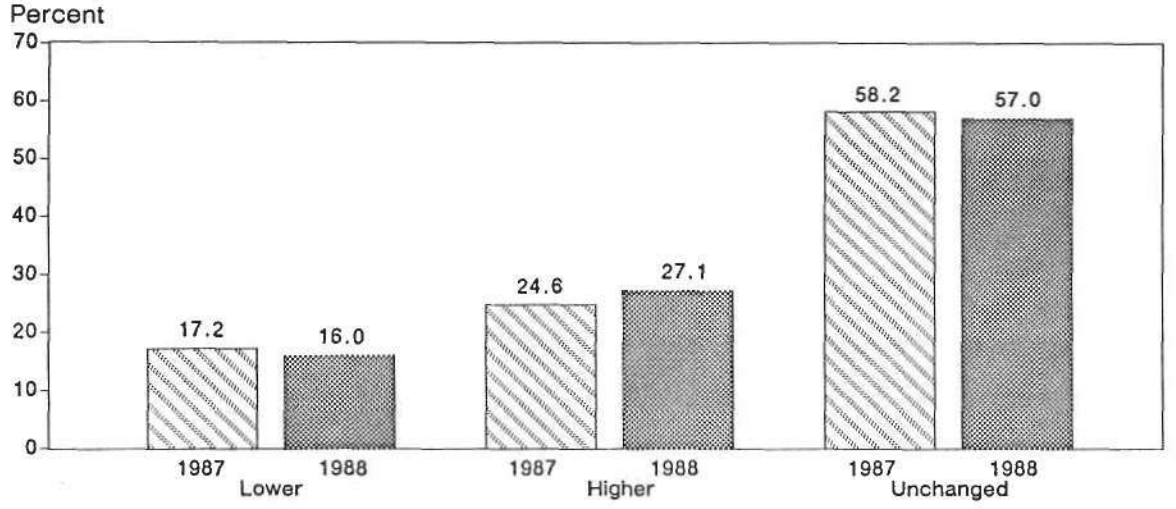
Source: Dun & Bradstreet

Figure 3

Capital Spending—Actual Versus Planned 1987 and 1988



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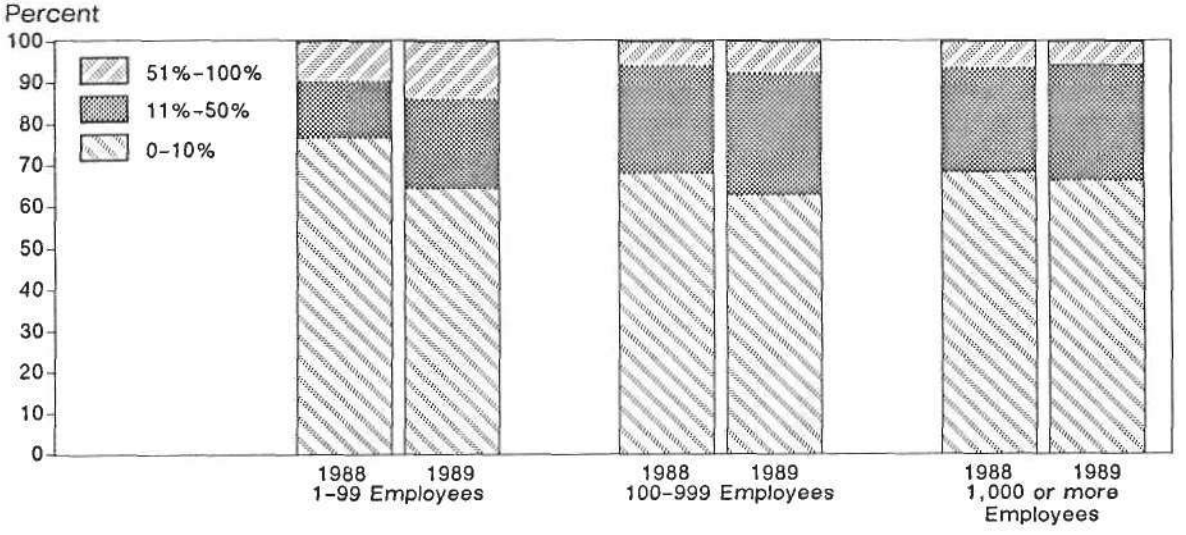
Source: Dun & Bradstreet

Figure 4

Budget Allocation for Computers and Telecommunications Equipment by Company Size



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Source: Dun & Bradstreet

CAPITAL SPENDING SURVEY RESULTS

The manufacturing sector was the most positive in spending plans, with 50.3 percent of those companies surveyed planning to increase capital spending. This situation is probably due to continued strength in exports. According to Dun & Bradstreet, the manufacturing sector contributes approximately 60.0 percent of all exports. Although most manufacturing companies plan increases in capital spending, the percentage allocated toward computers and telecommunications equipment has not increased.

Earlier forecasts pointed to economic slowdowns and the possibility of a recession in 1989. Although the current forecasts are more positive, Dun & Bradstreet considers the following scenarios to be areas of concern for the capital spending outlook:

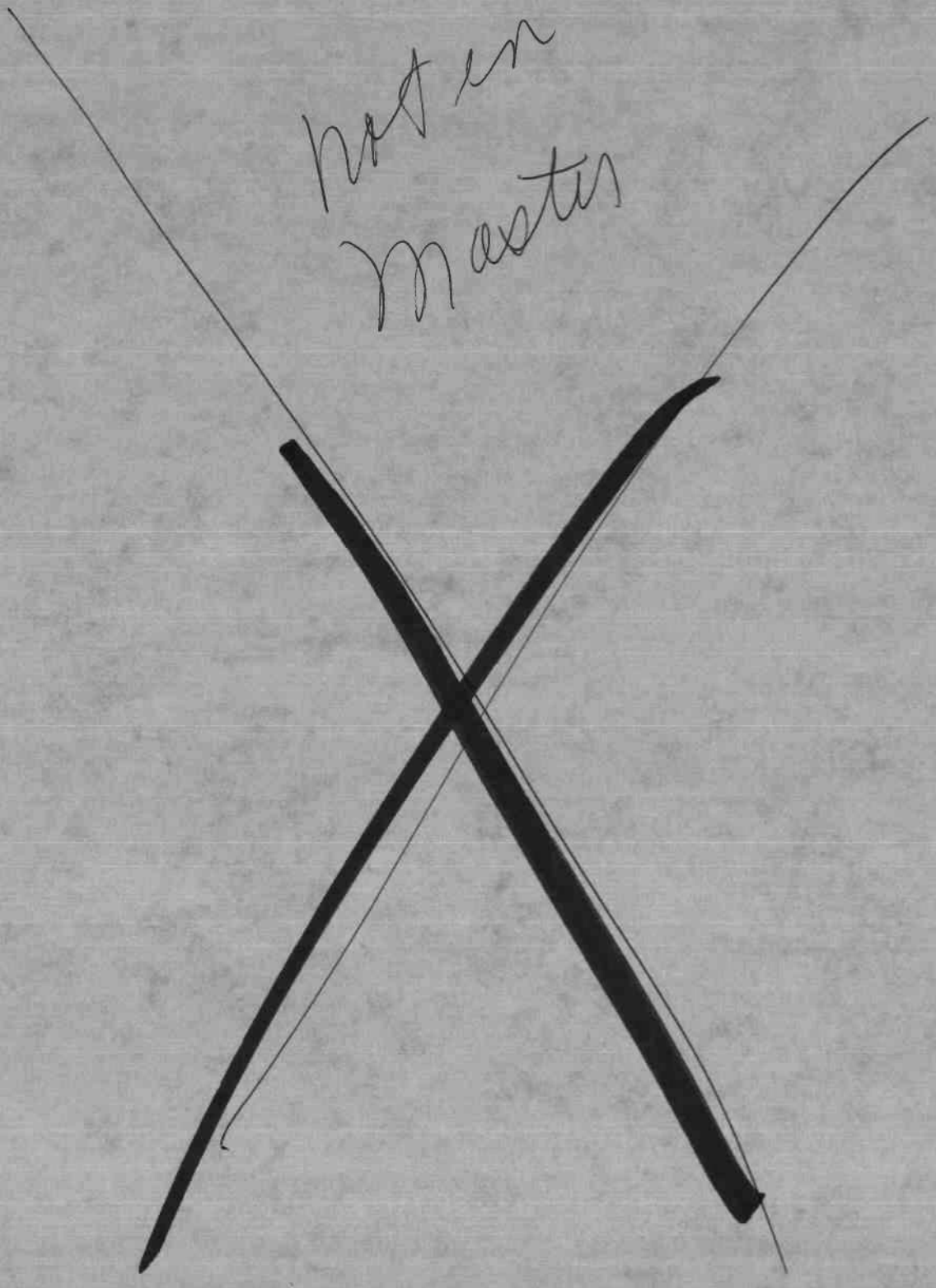
- Higher interest rates, resulting from anti-inflationary monetary policies, could drive up the cost of capital.
- Interest rates increasing in the United States relative to rates in international markets could drive up the dollar and reduce exports.
- Protectionist policies among U.S. trade partners may hinder the ability of U.S. companies to compete in these markets.
- New fiscal deficit-cutting initiatives that increase corporate taxes or reduce investment incentives may affect capital spending.
- A drop in consumer spending growth would free up a sizable amount of productive capacity in many industrial sectors that serve domestic markets. The freed capacity would lessen the demand for new capital equipment.

The overall capital spending picture, as supported by the Dun's 5000 survey, is a positive one. Unless potential pitfalls occur, as outlined by Dun & Bradstreet, these spending plans, should be achieved or exceeded.

DATAQUEST CONCLUSIONS

Although the Dun & Bradstreet forecast calls out a slowing in the economy, the capital spending plans of companies continue to be aggressive. Dataquest clients can still take advantage of this persisting growth pattern in planned capital expenditures while keeping an eye on potentially high-impact economic shifts.

Bernadette Joseph
Terrance A. Birkholz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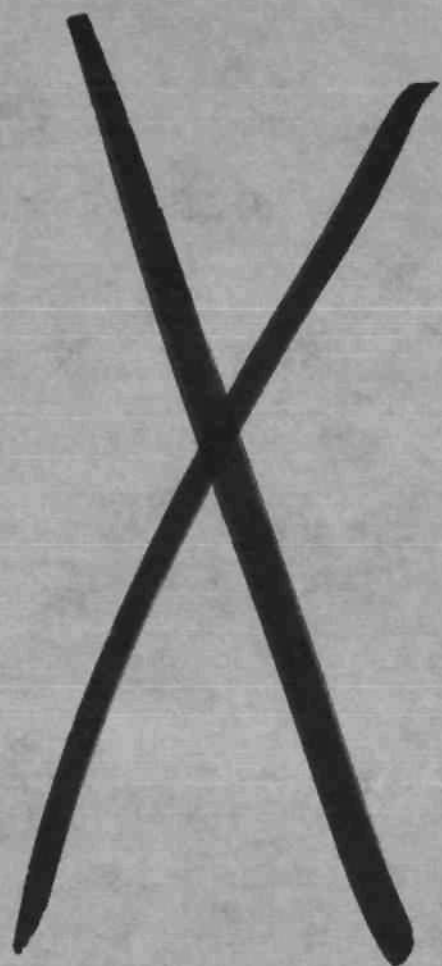

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Research *Bulletin*

SEMS Code: Newsletters 1989
Capital Spending
0003132

TI PLANS TO INCREASE CAPITAL SPENDING BY $100 MILLION

Although Dataquest is forecasting a slowdown in the semiconductor industry beginning in the third quarter of 1989, Texas Instruments (TI) is increasing its semiconductor capital spending plans. TI spent approximately $392 million in 1988 for semiconductor property, plant, and equipment (PPE). TI's current 1989 plans show an increase in capital spending of about $100 million—to $492 million. Table 1 lists TI's major capital spending projects.

Table 1

Major TI Capital Spending Projects

Project	Location	Description
4Mb DRAM Fab	Avezzano, Italy Miho, Japan	$250 million, 0.8-micron, 1990 pilot 1990 pilot
16Mb DRAM	Dallas, Texas	Prototype, 200mm
1Mb DRAM Fab	Miho, Japan	Expansion of existing line
Consumer ICs	Tsukuba, Japan	R&D center
Assembly	Philippines	Expansion of facility
Materials and Control Facility	Korea	Possible site of future fab

Source: Texas Instruments
Dataquest
February 1989

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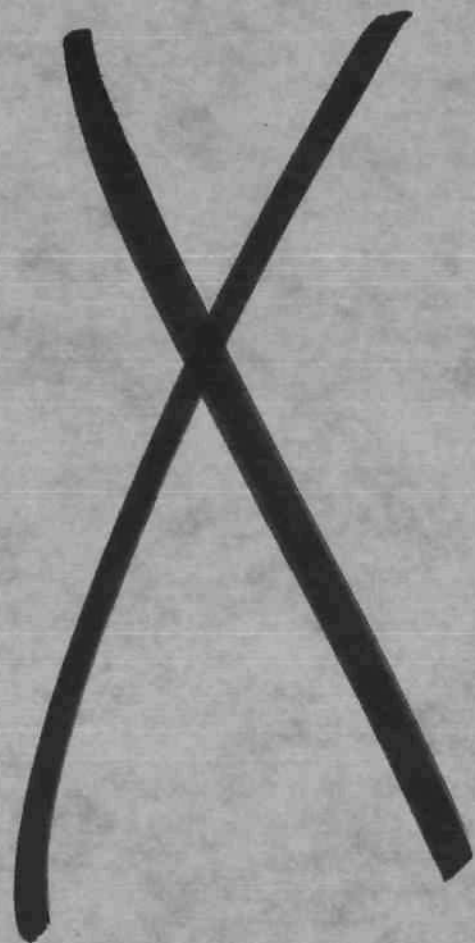
These plans reflect some major strategic thrusts by TI. The company will build a 4Mb–DRAM, 0.8–micron fab in Avezzano, Italy. This fab, including equipment, will cost approximately $250 million. TI anticipates that the facility will eventually be able to produce logic devices as well as memory devices, which is significant in that it would greatly increase the fab's product diversity. Pilot production of memory devices is expected by 1990, volume production by 1991. TI decided to build its fab in Europe in order to have a strong presence on the continent by 1992. This fab is significant for another reason: TI reportedly has financial support from customers that require a strategic source of memory.

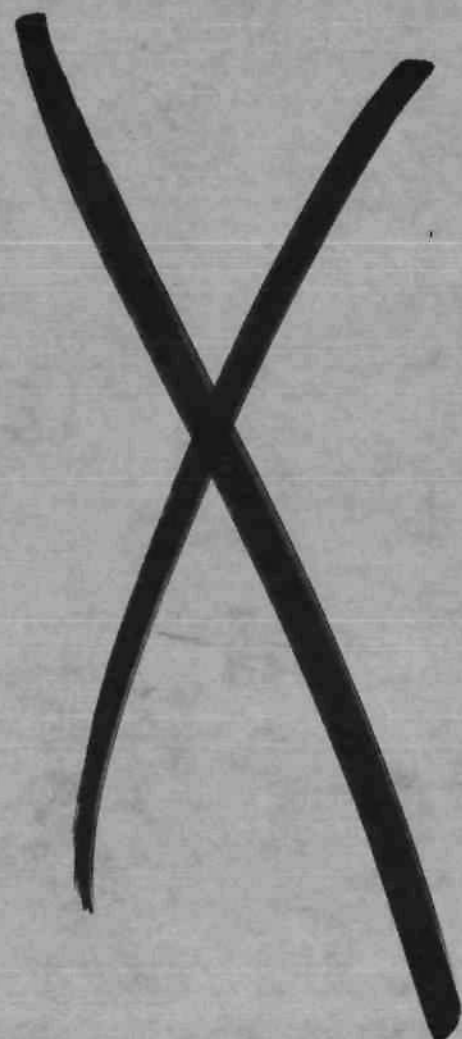
Other DRAM activities that TI says it will fund in 1989 include a 200mm, 16Mb DRAM prototype line in Dallas, Texas, an expansion of the 1Mb DRAM line in Miho, Japan, at a reported cost of $77 million, and a new 4Mb DRAM line, also in Miho.

TI is also setting up an R&D center in Tsukuba, Japan, to develop consumer ICs. The company believes that this is important in order for it to maintain a growing and balanced presence in the Japanese marketplace.

Other areas of spending by TI include the upgrading of logic and memory facilities, and a materials and controls facility in Korea where a fab also could possibly be built in the future. TI also has invested heavily in its assembly facilities, especially, since 1987, in its facility in Baguio City, the Philippines.

George Burns





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Research Newsletter

SEMS Code: SEMS 1989 Newsletters
Worldwide Fabs
0003168

JAPANESE WAFER FAB UPDATE: NEW FABS, ADVANCED DRAMS, AND 8–INCH WAFERS

INTRODUCTION

In 1988, a three–month joint research project between Dataquest's San Jose and Tokyo offices was launched in order to provide in–depth information on Japan's semiconductor manufacturing activities. The results are discussed in this newsletter, and include information on manufacturing trends and fabs that went into production during 1988, as well as information on the announced, initiated, and forecast fab lines that will go into production through the early 1990s.

MANUFACTURING TRENDS

Thirteen production and pilot–based silicon fabs went into production during 1988. In 1989, 14 will go into production, and 12 more are expected to come on–line in 1990. Eight other gallium arsenide and R&D lines also should come on–line during 1988 through 1990. Dataquest also knows of 13 more fab lines that are planned to go into production after 1990.

Details of all known fabs started up since 1988 are listed in Table 1. Table 2 lists the status definitions used in Table 1.

Nine of the 13 production and pilot–based silicon fabs that began operations during 1988 produce advanced DRAMs and SRAMs. Ten of the 14 fabs begun during 1989 and 9 of the 12 during 1990 also will produce advanced DRAMs and SRAMs. Approximately 75 percent of these new fabs will produce advanced 1Mb or 4Mb DRAMs and, with few exceptions, all will process linewidths at 1 micron or less, on 6–inch or 8–inch wafers. The average wafer–start capacity for future production–based DRAM lines is 21,133 wafers per four–week period, while the average wafer–start capacity for future DRAM pilot lines is 8,500 wafers per four–week period. Capacity figures stated here reflect capacity of the fab when it is completely filled with equipment.

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Table 1

Japanese Fab Activity Planned or Initiated to Begin Producing During 1988 and Beyond

Company	Prefecture	City	Plant Name	Fab Name	Status	Target Date Prod. Begins	Wafer Size (In.)	Clean Room Square Feet	Drawn Line Width	Process Technology	Products to be Produced	Start Capacity Per Month	Fab Type
					PRODUCTION BEGAN 1988								
FUJITSU	FUKUSHIMA	AIZU WAKAMATSU-SHI	AIZU F	VLSI 3	EQUIPMENT UPGRADE		6	0	1.00	CMOS MOS	1Mb DRAM SRAM ROM	40,000	F
FUJITSU	KANAGAWA	KAWASAKI-SHI	N/A	N/A	NEW SHELL/CLEAN ROOM		6	0	0.70	CMOS	16Mb DRAM	8,000	R
FUJITSU	KANAGAWA	KAWASAKI-SHI	N/A	N/A	NEW SHELL/CLEAN ROOM		3	0	0.00	GaAs	HEMT PHET	0	R
FUJITSU	KANAGAWA	KAWASAKI-SHI	N/A	N/A	NEW SHELL/CLEAN ROOM		5	0	0.00	N/A	3D ICs JOSEPHSON JUNCTION	15,000	P
HITACHI	HOKKAIDO	CHITOSE-SHI	HOKKAI S/C	CHITOSE F	EQUIPMENT EXPANSION	12/01/88	6	20,000	1.00	CMOS	64K 256K SRAM	15,000	F
HITACHI	IBARAGI	KATSUTA-SHI	NAKA WORKS	N/A	EQUIPMENT UPGRADE		6	20,000	0.80	CMOS	1Mb DRAM SAMPLE 4Mb	35,000	F
HITACHI	IBARAGI	KATSUTA-SHI	NAKA WORKS	N/A	NEW CLEAN ROOM	01/01/88	6	0	1.00	CMOS	1Mb DRAM 1Mb SRAM	9,000	P
HITACHI	YAMANASHI	NAKAKOMA-GUN	KOFU WORKS	NO. K4-2	NEW CLEAN ROOM		6	0	1.00	CMOS	1Mb DRAM	20,000	F
IBM	SHIGA	YASU-GUN	S/C RSRCH CTR	N/A	NEW SHELL/CLEAN ROOM	05/01/88	8	0	0.00	CMOS	1Mb 4Mb DRAM	0	P
MATSUSHITA	NIIGATA	ARAI-SHI	ARAI F	FAB D	EQUIPMENT EXPANSION		5	0	1.50	BIP	LOG LIN CCD	40,000	F
MATSUSHITA	TOYAMA	UOZU-SHI	UOZU F	FAB C-1	NEW SHELL/CLEAN ROOM	07/01/88	6	0	1.00	CMOS	1Mb DRAM SAMPLE 4Mb	20,000	F
MITSUBISHI	EHIME	SAIJO-SHI	SAIJO C	N/A	EQUIPMENT UPGRADE		6	43,060	0.80	CMOS	256K 1Mb DRAM SAMPLE 4Mb	30,000	FAT
MITSUBISHI	KOCHI	KAMI-GUN	KOCHI FACTORY	N/A	EQUIPMENT EXPANSION	06/01/88	6	0	1.00	CMOS	8-bit 16-bit MCU 1Mb DRAM	10,000	FAT
NEC	KANAGAWA	SAGAMIHARA-SHI	SAGAMIHARA	ULSI R&D	NEW CLEAN ROOM	06/01/88	8	0	0.80	CMOS	4Mb DRAM ASIC	13,500	P
NEC	KUMAMOTO	KUMAMOTO-SHI	KYUSHU	FAB 7	NEW CLEAN ROOM	06/01/88	6	30,000	1.00	CMOS MOS	ASIC 32-bit MPU 1Mb DRAM	35,000	F
NEC	YAMAGUCHI	ASA-GUN	YAMAGUCHI LTD	PHASE 2	NEW SHELL/CLEAN ROOM	06/01/88	6	24,760	0.80	CMOS	4Mb DRAM 1Mb SRAM MPU	20,000	FAT
NEC	YAMAGUCHI	ASA-GUN	YAMAGUCHI LTD	PHASE 1	EQUIPMENT UPGRADE		6	0	1.00	CMOS MOS	256K 1Mb DRAM SRAM MPU	20,000	F
NMB SEMICONDUCTOR	CHIBA	TATEYAMA-SHI	N/A	FAB 2	EQUIPMENT EXPANSION	10/01/88	6	43,000	1.00	CMOS MI	1Mb DRAM SRAM SAMPLE 4Mb	10,000	NPAT
OKI	MIYAZAKI	MIYAZAKI-GUN	MIYAZAKI OKI	MI	UPGRADE	04/01/88	5	0	1.50	CMOS	256K DRAM SRAM ARRAYS MPU	50,000	FAT
SEIKO EPSON	NAGANO	SUWA-GUN	FUJIMI PLANT	BLDG D	EQUIPMENT EXPANSION	12/01/88	6	0	1.20	CMOS	ARRAYS CBIC 256K SRAM	20,000	NF
SHINDENGEN	YAMAGATA	HIGASHINE-SHI	HIGASHINE DIV.	BLDG 2 MOS	NEW CLEAN ROOM		5	27,311	2.00	CMOS MOS	CUSTOM	25,000	P
SONY	KAGOSHIMA	KOKUBU-SHI	SONY KOKUBU	N/A	EQUIPMENT EXPANSION		5	0	1.30	BIP CMOS MOS	SRAM MPU CCD LIN A/D D/A	30,000	FAT
SONY	KANAGAWA	ATSUGI-SHI	ATSUGI PLANT	N/A	EQUIPMENT EXPANSION		3	0	0.00	GaAs	FET LASER CCD	0	PAT
TI	IBARAGI	INASHIKI-GUN	MIHO PLANT	MIHO 6.2	EQUIPMENT EXPANSION	12/01/88	6	30,000	0.80	CMOS BICMOS	SRAM 1Mb DRAM SAMPLE 4Mb	24,000	F
TOHOKU SEMICONDUCTOR	MIYAGI	IZUMI-SHI	SENDAI FACTORY	N/A	NEW SHELL/CLEAN ROOM	08/01/88	6	42,000	1.00	CMOS	1Mb DRAM 256K SRAM MPU	20,000	FAT
TOSHIBA	FUKUOKA	KITAKYUSHU-SHI	KITAKYUSHU P	KUBIC 2	NEW CLEAN ROOM	10/01/88	5	21,530	2.00	BICMOS	ASIC OPTO LOG	20,000	NF
TOSHIBA	KANAGAWA	KAWASAKI-SHI	ULSI LAB	N/A	NEW CLEAN ROOM		6	0	0.70	BIP CMOS	3D ICs 16Mb DRAM	4,000	R
TOSHIBA	OITA	OITA-SHI	TOSHIBA OITA	STEP 3 #7	NEW CLEAN ROOM	06/01/88	6	0	1.00	CMOS	1Mb DRAM	30,000	F
YAMAHA	KAGOSHIMA	AIRA-GUN	KAGOSHIMA PLANT	N/A	EQUIPMENT UPGRADE	09/01/88	5	0	1.20	CMOS	ROM CBIC ASSP	35,000	FAT
YAMAHA	SHIZUOKA	HAMAMATSU-SHI	TOYOOKA WORKS	EE DEV CTR	NEW SHELL/CLEAN ROOM	12/01/88	6	0	0.80	CMOS	CBIC LOG	6,000	P

(Continued)

Table 1 (Continued)

Japanese Fab Activity Planned or Initiated to Begin Producing During 1988 and Beyond

Company	Prefecture	City	Plant Name	Fab Name	Status	Target Date Prod. Begins	Wafer Size (In.)	Clean Room Square Feet	Drawn Line Width	Process Technology	Products to be Produced	Start Capacity Per Month	Fab Type
PRODUCTION BEGINS 1989													
CANON	SHIGA	NAGAHAMA-SHI	NAGAHAMA WORKS	N/A	NEW SHELL/CLEAN ROOM	03/01/89	3	0	0.00	GaAs	AMORPHOUS IMAGE SENSORS	0	P
FUJITSU	FUKUSHIMA	AIZU WAKAMATSU-SHI	WAKAMATSU F	NO. 3	NEW SHELL/CLEAN ROOM		6	0	0.00	CMOS	1Mb DRAM ASIC	0	F
FUJITSU	MIE	KUWANA-GUN	MIE F	NO. 3	NEW SHELL/CLEAN ROOM	06/01/89	8	0	0.80	CMOS	4Mb DRAM	7,000	P
FUJITSU	MIYAGI	SHIBATA-GUN	MIYAGI	N/A	NEW SHELL/CLEAN ROOM		6	0	1.20	CMOS	ASIC	0	P
MITSUBISHI	KOCHI	KAMI-GUN	KOCHI FACTORY	N/A	NEW SHELL/CLEAN ROOM	10/01/89	6	0	1.00	CMOS	1Mb DRAM SAMPLE 1Mb SRAM	12,000	P
NEC	IBARAGI	TSUKUBA-GUN	TSUKUBA R&D CTR	N/A	NEW SHELL/CLEAN ROOM	04/01/89	0	0	0.40	GaAs CMOS	OPTO 3D 64Mb DRAM SOR	0	R
NIPPON PRECISION CIRCUITS	TOCHIGI	NASU-GUN	N/A	N/A	N/A		6	21,530	0.00	CMOS	LOG LIN	7,000	P
OKI	MIYAGI	KUROKAWA-GUN	MIYAGI OKI	N/A	NEW SHELL/CLEAN ROOM	05/01/89	6	0	1.00	CMOS	ARRAY 1Mb DRAM SAMPLE 4Mb	20,000	FAT
ROHM	KYOTO	KYOTO-SHI	LSI RESEARCH	N/A	NEW SHELL/CLEAN ROOM	05/01/89	6	27,000	1.20	CMOS	256K SRAM	15,000	F
SANYO	NIIGATA	OJIYA-SHI	NIIGATA SANYO	BLDG 2 CMOS	NEW CLEAN ROOM	06/01/89	6	0	1.00	BICMOS CMOS	ASIC FLD 1Mb DRAM	16,000	P
SHARP	HIROSHIMA	FUKUYAMA-SHI	FUKUYAMA PLANT	BLDG 2	NEW SHELL/CLEAN ROOM	07/01/89	6	0	0.80	CMOS	1Mb DRAM 16Mb ROM CCD	20,000	FAT
SONY	NAGASAKI	ISAHAYA-SHI	SONY NAGASAKI	N/A	READY FOR EQUIPMENT	03/01/89	6	25,000	1.00	CMOS	1Mb SRAM CCD	5,000	P
SORTEC	IBARAGI	TSUKUBA-GUN	N/A	N/A	NEW SHELL/CLEAN ROOM	05/01/89	0	0	0.40	N/A	SOR LITHO RESEARCH	0	R
TI	OITA	ITSUMI-GUN	MIJI PLANT	N/A	NEW SHELL/CLEAN ROOM	06/01/89	8	26,912	0.80	CMOS	4Mb DRAM	0	P
TOSHIBA	IWATE	KITAKAMI-SHI	IWATE TOSHIBA	PHASE 3	NEW SHELL/CLEAN ROOM	10/01/89	6	0	0.00	CMOS	ASIC	36,000	P
TOSHIBA	OITA	OITA-SHI	TOSHIBA OITA	STEP 3	NEW CLEAN ROOM	04/01/89	6	0	0.80	CMOS	4Mb DRAM	30,000	FAT
TOYOTA	AICHI	TOYOTA-SHI	CENTRAL LAB	N/A	NEW SHELL/CLEAN ROOM	03/01/89	5	0	0.00	CMOS	MCU PWR ICs CUSTOM	0	P
PRODUCTION BEGINS 1990													
FUJITSU	IWATE	ISAWA-GUN	IWATE F	NO. 4	NEW SHELL/CLEAN ROOM	10/01/90	8	0	0.80	CMOS MOS POLY3	4Mb DRAM SRAM	25,000	F
HAMAMATSU PHOTONICS	SHIZUOKA	HAMAMATSU-SHI	HAMAKITA R&D	N/A	NEW SHELL/CLEAN ROOM	03/01/90	0	0	0.00	N/A	OPTO	0	R
HITACHI	TOKYO	KODAIRA-SHI	MUSASHI WORKS	N/A	NEW SHELL/CLEAN ROOM	01/01/90	8	0	0.80	CMOS	4Mb DRAM	0	P
HITACHI	YAMANASHI	NAKAKOMA-GUN	KOFU WORKS	INASUNA F	NEW SHELL/CLEAN ROOM	02/01/90	6	0	0.80	CMOS	4Mb DRAM	0	P
IBM	SHIGA	YASU-GUN	N/A	N/A	NEW SHELL/CLEAN ROOM	04/01/90	8	0	0.80	N/A	1Mb 4Mb DRAM LOG	0	F
MATSUSHITA	TOYAMA	UOZU-SHI	UOZU F	FAB C-2	NEW CLEAN ROOM		6	0	0.80	CMOS	4Mb DRAM	0	P
NATIONAL SEMICONDUCTOR	N/A	N/A	N/A	N/A	NEW SHELL/CLEAN ROOM		0	0	0.00	N/A	N/A	0	R
NEC	HIROSHIMA	HIGASHI-HIROSHIMA	CHUGOKU	PHASE 1	NEW SHELL/CLEAN ROOM	08/01/90	6	38,754	0.80	CMOS	4Mb DRAM SRAM 32-bit MPU	30,000	FAT
NEC	KANAGAWA	SAGAMIHARA-SHI	SAGAMIHARA	16Mb PROTO	NEW SHELL/CLEAN ROOM	02/01/90	8	20,000	0.55	CMOS	16Mb DRAM	5,000	P
NIPPON DENSO	AICHI	KARIYA-SHI	KODA WORKS	BLDG. 2	NEW SHELL/CLEAN ROOM	12/01/90	0	0	0.00	MOS	MCU	0	F
NMB SEMICONDUCTOR	CHIBA	TATEYAMA-SHI	N/A	FAB 3	NEW SHELL/CLEAN ROOM	06/01/90	6	0	0.80	CMOS	4Mb DRAM	10,000	F

(Continued)

Table 1 (Continued)

Japanese Fab Activity Planned or Initiated to Begin Producing During 1988 and Beyond

Company	Prefecture	City	Plant Name	Fab Name	Status	Target Prod. Begins	Wafer Size (In.)	Clean Room Square Feet	Drawn Line Width	Process Technology	Products to be Produced	Start Capacity Per Month	Fab Type
PRODUCTION BEGINS 1990 (Continued)													
RICOH	OSAKA	IKEDA-SHI	N/A	N/A	NEW SHELL/CLEAN ROOM		6	0	1.00	CMOS	ARRAYS	0	P
SHINDENGEN	YAMAGATA	HIGASHINE-SHI	HIGASHINE DIV.	BLDG 3	NEW SHELL/CLEAN ROOM		0	0	0.00	CMOS MOS	CUSTOM	0	P
TOSHIBA	OITA	OITA-SHI	TOSHIBA OITA	STEP 3 #9	NEW CLEAN ROOM		6	0	0.80	CMOS	4Mb DRAM	0	P
PRODUCTION BEGINS 1991													
ASAHI MICRO SYSTEMS INTERNATIONAL	MIYAZAKI	N/A	N/A	N/A	NEW SHELL/CLEAN ROOM		0	0	0.00	N/A	ASIC LIN A/D D/A ASSP	0	P
RECTIFIER	AKITA	KAMABE-GUN	AKITA FACTORY	N/A	NEW SHELL/CLEAN ROOM		0	0	0.00	N/A	DIS	0	PAT
MITSUBISHI	EHIME	SAIJO-SHI	SAIJO D	N/A	NEW SHELL/CLEAN ROOM	01/01/91	6	0	0.80	CMOS	4Mb DRAM	0	P
MOTOROLA	MIYAGI	IZUMI-SHI	SENDAI PLANT	MOS 10	NEW SHELL/CLEAN ROOM		6	0	0.80	CMOS	4Mb DRAM MPU	0	P
NEC	HIROSHIMA	HIGASHI-HIROSHIMA	CHUGOKU	PHASE 2	NEW SHELL/CLEAN ROOM	06/01/91	8	0	0.80	CMOS	4Mb DRAM EPROM	0	P
OKI	MIYAZAKI	MIYAZAKI-GUN	MIYAZAKI OKI	M3	NEW CLEAN ROOM	02/01/91	6	0	1.00	CMOS	4Mb DRAM	0	P
SEIKO EPSON	NAGANO	SUWA-GUN	FUJIMI PLANT	BLDG E	NEW SHELL/CLEAN ROOM		6	0	0.80	CMOS	ARRAYS CBIC 1Mb SRAM	0	P
SONY	KANAGAWA	KANAHARA, OKADA	ATSUGI PLANT	N/A	N/A		0	0	0.00	GaAs CMOS	MEM LIN OPTO DIS	0	P
TI	IBARAGI	TSUKUBA-GUN	N/A	N/A	NEW SHELL/CLEAN ROOM	01/01/91	0	0	0.00	N/A	64Mb DRAM CONSUMER ICs	0	R
PRODUCTION BEGINS 1992													
KAWASAKI STEEL	N/A	N/A	N/A	N/A	NEW SHELL/CLEAN ROOM		0	0	0.00	CMOS	ASIC	0	P
SONY	KAGOSHIMA	KOKUBU-SHI	SONY KOKUBU	N/A	N/A		6	0	0.80	BIP CMOS MOS	LOG MEM MPU LIN DIS OPTO	0	PAT
PRODUCTION BEGINS 1993													
NEC	HIROSHIMA	HIGASHI-HIROSHIMA	CHUGOKU	PHASE 3	NEW SHELL/CLEAN ROOM		8	0	0.60	CMOS	16Mb DRAM MPU EPROM	0	P
PRODUCTION BEGINS 1994													
NEC	HIROSHIMA	HIGASHI-HIROSHIMA	CHUGOKU	PHASE 4	NEW SHELL/CLEAN ROOM		8	0	0.60	CMOS	16Mb DRAM MPU EPROM	0	P

Note: P = Production-based fab line
P = Pilot line
R = R&D line
A = Assembly
T = Test

N/A = Not Available

Source: Dataquest
February 1989

Table 2

Nomenclature and Definitions
Status Field

Nomenclature	Definition
New Shell/Clean Room	Brand new from the ground up (green field)
New Clean Room	The building is complete and ready for clean room installation
Ready for Equipment	The clean room is complete and ready for equipment installation
Clean Room Expansion	Increase of total square footage for an existing clean room
Equipment Expansion	The installation of additional equipment to an existing clean room
Expansion	An increase in total clean room square footage and installed equipment
Clean Room Upgrade	Improved cleanliness, design, DI water, and/or vibration isolation
Equipment Upgrade	Conversion to larger wafer size and/or finer linewidths; equipment replacement, retrofit, and/or refurbishment
Upgrade	Clean room upgrade and equipment upgrade
Reramp from Shutdown	Brought back into production from a shutdown

Source: Dataquest
February 1989

Along with the 13 new fabs turned on during 1988, 13 additional fabs received major upgrades and/or capacity expansions. From 1984 through 1990, Japan has, and will, consistently add approximately 12 new fabs per year. When looking at upgrades and capacity expansions, Japan jumped to 13 upgrades and capacity expansions during 1988, up from approximately 3 per year for the years 1984 through 1987.

To summarize, Japan has brought up new fab lines at a fairly consistent rate of 12 per year since 1984. However, upgrade and capacity expansion activity during 1988 increased four times over previous years. Japan has been very consistent about the addition of new fabs when compared with the United States. While Japan will continue to add approximately 12 new production and pilot-based silicon fabs per year from 1984 through 1990, the United States fluctuates between 8 and 21 per year during the same time period. Dataquest believes that most new fabs that have or will come on-line in Japan during industry downturns begin production with a small fraction of the equipment that they will ultimately contain. The companies that own these fabs are therefore well positioned for the next upturn by quickly adding equipment to their partially utilized floor space. There also are new fabs coming on-line during the upturn years that fill their own fab floor with equipment very quickly.

NEXT-GENERATION FABS

During 1988 and 1989, we will see the first dedicated 4Mb DRAM fabs begin operation in Japan. These fabs will most likely supply a good part of the more than 10 million 4Mb DRAMs expected to be shipped per month during 1990 (see Table 3).

Table 3

Fab Generations by DRAM Density

Fab Line Generation	DRAM Density	Sample Year	> 10 Million Units/Mo	Peak Prod. Year	Linewidth, Sample to Full Shrink	Lithography Tools Used in Japan
First	16K	1976	1978	1982	5-3um	Contact/proximity aligner
First	64K	1979	1981	1984	3-2um	Proximity/projection aligner
Second	256K	1983	1984	1988	2-1.2um	G-line stepper
Second	1Mb	1985	1987	1991	1.2-0.8um	High N.A. G-line stepper
Third	4Mb	1988	1990	1994	0.8-0.6um	High N.A. G-line/I-line stepper
Fourth?	16Mb	1991	1993	1997	0.6-0.4um	I-line/excimer laser stepper
Fifth?	64Mb	1994	1996	2000	0.4-0.3um	Excimer laser/SOR X-ray
Sixth?	256Mb	1997	1999	2003	0.3-0.2um	SOR X-ray

Source: Dataquest
February 1989

Historically, an advanced fab in Japan has produced two generations of DRAMs. It has been logical to try to produce as many generations of a DRAM as possible from the same fab because DRAMs have represented the clear majority of Japanese production. Traditionally, these fabs have upgraded or replaced some of the installed equipment in order to produce the second DRAM generation through its die shrink.

Now, however, Japanese DRAM production is decreasing relative to total Japanese IC production. This is due to Japanese gains in ASICs, MCUs, MPUs, and other ICs for consumer, computer, and automotive applications. As Japanese companies gain more market share in the non-DRAM categories, shifting production down the "product food chain," as opposed to retooling the fab for next-generation DRAMs, will be easier to do. Examples of the product food chain that a fab could produce during its useful life, from beginning to end, include: DRAMs/SRAMs, gate arrays, CBICs, MCUs/MPUs, opto devices, standard logic, analog, power ICs, and discretes. Dataquest believes that more of these new and future DRAM fabs will produce one, or perhaps one-and-a-half, DRAM generations instead of two generations due to these gains in non-DRAM IC products and the ability to take production down the product food chain. Other factors that could influence semiconductor manufacturers to move toward this single-DRAM generation fab concept include the following:

- The implementation of common "core" manufacturing processes for all product divisions (Under ideal conditions, this concept only requires that the mask set be changed for manufacturing a different product while using the same "core" process recipe)
- The rapidly increasing cost of semiconductor processing equipment
- Conversion to 8-inch wafers for volume production of next generation DRAMs
- Required purity improvements in deionized (DI) water and gas-handling systems for next generation DRAM manufacturing
- The reduction of process capability overlap for semiconductor processing equipment when moving from one DRAM generation to the next

Dataquest has observed the beginning of this movement toward single-generation DRAM fabs, with some companies bringing up dedicated 1Mb fab lines that are not expected to be upgraded to 4Mb DRAM production. Rather than upgrading, these fabs most likely will shift production down the product food chain toward gate array and MCU/MPU products after 1Mb production peaks in 1991. Although 4Mb DRAMs have been sampled out of these 1Mb fabs, Dataquest has noted that, so far, all Japanese manufacturers have plans to do volume production in new, dedicated 4Mb lines (see Table 4).

Two of the factors that could contribute to the decline of two-generation DRAM fabs are the high costs and physical restrictions associated with the conversion to 8-inch wafers and major improvements in DI water and gas-handling systems. Most conversions from starting up new 6-inch lines to new 8-inch lines will occur during the ramp-up of the 4Mb generation and the following 16Mb generation of DRAMs.

Table 4

Progression of 4Mb/16Mb/64Mb DRAM Activity in Japan

	R&D/Trial Production				Pilot/Prototype Line				Production Line			
Company	Location	DRAM	Year	Wafer Size	Location	DRAM	Year	Wafer Size	Location	DRAM	Year	Wafer Size
NEC	Tamagawa Works	4Mb 16Mb	1986	5-inch	Yamaguchi Ltd.	4Mb	1988	6-inch	Chugoku Ltd.	4Mb	1990	6-inch
NEC					Sagamihara	4Mb	1988	8-inch	Chugoku Ltd.	4Mb	1991	8-inch
NEC					Sagamihara	16Mb	1990	8-inch	Chugoku Ltd.	16Mb	1993	8-inch
NEC									Chugoku Ltd.	16Mb	1994	8-inch
NEC	Tsukuba R&D Ctr.	64Mb	1989	5-inch								
Hitachi					Mobara Works	4Mb	1987	6-inch	Kofu Works	4Mb	1990	6-inch
Hitachi					Naka Works*	4Mb	1988	6-inch				
Hitachi					Musashi Works	4Mb	1990	8-inch				
Hitachi	Central Lab	16Mb	1986	5-inch								
Toshiba					Tamagawa Plant	4Mb	1987	6-inch	Oita Plant	4Mb	1989	6-inch
Toshiba									Oita Plant	4Mb	1990	6-inch
Toshiba	ULSI Lab	16Mb	1988	6-inch								
Fujitsu					Mie Plant*	4Mb	1987	6-inch	Iwate Works	4Mb	1990	8-inch
Fujitsu					Mie Plant	4Mb	1989	8-inch				
Fujitsu	Atsugi Lab	16Mb	1987	6-inch								
Fujitsu	Kawasaki	16Mb	1988	6-inch								
Mitsubishi					Saijo*	4Mb	1988	6-inch	Saijo	4Mb	1991	6-inch
Mitsubishi	Central Research	16Mb	1986	5-inch								
Matsushita	Kyoto Lab	4Mb	1985	6-inch	Uozu Factory	4Mb	1988	6-inch	Uozu Factory	4Mb	1990	6-inch
Matsushita	S/C Research Ctr.	16Mb 64Mb	1986	6-inch								
TI					Miho*	4Mb	1988	6-inch				
TI					Miji Plant	4Mb	1989	8-inch				
TI	Tsukuba	64Mb	1991	N/A								
IBM					Yasu Plant	4Mb	1989	8-inch	Yasu Plant	4Mb	1990	8-inch
NMB					Chiba	4Mb	1989	6-inch	Chiba	4Mb	1990	6-inch
Oki					Miyagi	4Mb	1989	6-inch	Miyazaki	4Mb	1991	6-inch
Motorola									Sendai	4Mb	1991	6-inch

Note: This table does not include existing fab lines that may be upgraded to more advanced DRAM production in the future.

*Denotes fab line that went into production before the year listed on this table and was upgraded for sample production, not newly built.

Source: Dataquest
February 1989

Dataquest also believes that major improvements in the purity of DI water and gases have become necessary for the production of 4Mb DRAMs. We note that many new dedicated 4Mb lines are being built. Dr. Ohme, a professor at the School of Engineering, Tohoku University, Sendai, Japan, is the founder of the ultra clean room and is widely recognized as the originator of the total concept approach to clean room and advanced semiconductor process technologies. His concepts for ultra-clean DI water and gas-handling systems now are gaining acceptance for installation into the future production environment. Recently, an Ultra Clean Technology (UCT) group with nearly 40 Japanese companies as founding members was organized by Dr. Ohme. This group will develop a UCT-based system for supplying materials, parts, and production equipment necessary for manufacturing submicron devices.

Dataquest also notes NEC's announcement that it will build a small, 5,000 wafer per month, dedicated 16Mb DRAM pilot line in Sagamihara at a cost of $160 million, including process equipment. Part of the high cost for NEC's 16Mb line will come from the 8-inch equipment that we expect that it will use. However, Dataquest also believes that major improvements in DI water and gas-handling systems can also help explain the high cost of this pilot line.

Lithography Limits and Options

Companies that construct new 4Mb lines using high numerical aperture (N.A.) g-line steppers are expected to achieve a minimum linewidth of 0.65 micron at 0.55 N.A. Unless unexpected advancements in high N.A. g-line lens technology occur, the final die shrink for 4Mb production at 0.6 micron and initial 16Mb production starting at 0.6 micron will not be likely (see Table 3). This 0.65-micron limit would force the users of g-line to install new lithography tools for the final die shrink of the 4Mb DRAM and to begin production of the 16Mb DRAM.

Companies that construct new 4Mb lines using i-line lithography are expected to achieve the full die shrink of the 4Mb DRAM and get into initial 16Mb production at 0.6 micron. However, they are not anticipated to be capable of achieving any die shrinks, and excimer laser lithography would be required to finish the 16Mb die shrink at 0.4 micron. New 4Mb fabs brought up on high N.A. g-line steppers could, at best, make the final die shrink of the 4Mb DRAM. This shift will mark the end of a long series of incremental improvements in g-line lithography that will have lasted more than 15 years. For new 4Mb fabs brought up on i-line steppers, this shift will mark the beginning of a rather short transitory phase in Japan, most likely beginning and ending with the 4Mb DRAM.

In Japan, little effort appears to be going into i-line lithography when compared with excimer laser lithography. While the future of excimer laser lithography is not clear, most people expect excimer technology to achieve 0.35 micron linewidths. This scenario would take the excimer laser stepper halfway through the 64Mb die shrink, and would provide the most longevity if it becomes production worthy while the 4Mb fabs are still being installed.

The lithography requirements for 4Mb, 16Mb, and 64Mb DRAM production, although not perfectly clear, appear to be more defined and to show less process capability overlap than in the past for the 16K through 1Mb generations. This reduction of equipment overlap from one DRAM generation to the next, and the escalating cost of these systems, are two factors that could influence semiconductor manufacturers toward the single DRAM generation fab concept.

Synchrotron orbital radiation (SOR) X-ray lithography appears to be the next choice in Japan for 64Mb DRAM production, instead of the point-source X-ray stepper. The Japanese have spent large amounts of money on SOR research at 10 major SOR facilities currently installed in Japan. At least 10 more facilities are in the planning stages. The known SOR facilities that are developing 64Mb+ devices include the following:

- The Ministry of Education's High-Energy Physics laboratory in the Tsukuba Science City, a joint development with Fujitsu, Hitachi, NEC, and NTT
- The NTT LSI Laboratory in Atsugi, a joint development with Hitachi and Toshiba
- SORTEC in Tsukuba, formed by the Japan Key Technology Center and 13 Japanese companies; Canon, Fujitsu, Hitachi, Matsushita, Mitsubishi, NEC, Nikon, Oki Electric, Sanyo, Sharp, Sony, Sumitomo, and Toshiba.

NEC also will open a 64Mb DRAM R&D laboratory in Tsukuba that will conduct SOR research this year. The Japanese seem to believe that there are too many difficulties in both mask and photoresist technology for point-source X-ray stepper lithography when compared with SOR X-ray lithography.

8-Inch Production

The first pilot and production-based manufacturing activity on 8-inch wafers began with NEC in Japan during 1988 (see Table 4). IBM also started 8-inch operations in Japan in 1988 with its third 8-inch location; IBM's other two locations are in the United States and Germany. Fujitsu and TI will begin 8-inch pilot production this year. TI's first 8-inch operation in Japan will be at Hiji; however, TI's locations at Miho and Dallas also will process 8-inch wafers shortly after Hiji comes on-line. IBM's second 8-inch line in Japan and Hitachi's first are expected to begin production during 1990.

All of these 8-inch fabs will be producing 4Mb DRAMs with the exception of IBM, which is currently producing 1Mb DRAMs on 8-inch wafers and 4Mb DRAMs on 5-inch wafers. The peak production year for the 4Mb DRAM is forecast to be 1994. At that time, at least one-third of the 4Mb fabs are expected to be processing 8-inch wafers, with the remainder processing 6-inch wafers. By 1997, the peak production year for the 16Mb DRAM, Dataquest anticipates that more than two-thirds of the 16Mb fabs will be processing 8-inch wafers, with the remainder processing 6-inch wafers.

Manufacturing on 8-inch wafers is not without its risks. Future DRAM prices are a consideration for companies that have not yet committed to 8-inch manufacturing. Prices are being looked at because of the high initial cost of setting up an 8-inch fab and

because 8-inch manufacturing during the early stages of the learning curve will not be as cost-effective as a more mature, 6-inch production line. Eight-inch manufacturing in its early stages is not as cost-effective as 6-inch due to the following factors:

- Manufacturing equipment using 6-inch wafers is much more refined than 8-inch equipment.
- Processes using 6-inch wafers are less complex and more mature than processes using 8-inch wafers.
- The cost per square inch for a raw, 6-inch wafer is currently less than for an 8-inch wafer.
- The cost for 6-inch equipment is in many cases less than that for comparable 8-inch equipment.

These risks can be very costly to companies that are just entering 8-inch production if DRAM price competition reappears at the same time. Most companies will prefer to enter price competition on the newest generation of DRAMs with 6-inch lines unless they feel they will be far enough along the 8-inch learning curve to compete when the price competition begins.

All of the companies that have committed to going 8-inch so far will pay a high initial price to drive the 8-inch technology. These companies have the deep pockets that are required for the commitment, and see the long-term rewards that will be realized during future manufacturing battles.

DATAQUEST CONCLUSIONS

Japan is consistently adding fabs, and approximately 75 percent of its new fabs are for the production of advanced DRAMs. New fabs going into production during upturns are quickly filled with equipment, whereas, during downturns, they have a small fraction of the floor space equipped. Fabs turned on during the downturn are poised to respond to the next upturn. Almost all of Japan's new fabs will run submicron processes.

Dataquest believes that more of these new and future DRAM fabs will move toward single-generation DRAM production, because DRAM production is decreasing relative to total IC production. This decrease is due to gains in production and market share being made in ASICs, MCUs, MPUs, and other ICs for consumer, computer, and automotive applications. As Japanese companies gain more market share in the non-DRAM categories, shifting production down the product food chain—as opposed to retooling the fab for next-generation DRAMs—will become more practical. Other factors that could influence semiconductor manufacturers to move toward this single DRAM generation fab concept include:

- The implementation of common "core" manufacturing processes for all product divisions. This concept, under ideal conditions, only requires that the mask set be changed for manufacturing a different product while using the same "core" process recipe. Those companies that implement this concept will be able to switch production over to another product with the least complications while at full capacity.

- The rapidly increasing cost of semiconductor processing equipment. The most cost-effective use of semiconductor equipment is to keep it in the same fab and keep it highly utilized for at least six years.

- Conversion to 8-inch wafers for volume production of next generation DRAMs. Most of the companies that do not adopt 8-inch production during the 4Mb generation will do so at the 16Mb level. The food chain concept will provide alternative products for the 6-inch 4Mb lines.

- Required purity improvements in DI water and gas-handling systems for next generation DRAM manufacturing. The move to 4Mb production appears to require new fabs and support facilities as opposed to upgrading existing fabs. There is a chance that 16Mb production will be better addressed with new fabs and support facilities instead of upgraded 4Mb lines.

- The reduction of process capability overlap for semiconductor processing equipment when moving from one DRAM generation to the next. This issue goes back to the high cost of equipment, as mentioned above.

If the Japanese rapidly adopt the single-generation DRAM fab strategy, a large bubble of advanced and low-cost capacity would begin to move into ASIC, MCU, and MPU production. The first capacity bubble would begin to come in after the 1Mb production peak during 1992, and the second capacity bubble would begin to come in after the 4Mb production peak during 1995. By 1992, Japanese companies should be enjoying the fruits of their current ASIC and MPU efforts that include many technology exchange agreements and joint development projects being conducted on and offshore. At the same time, the Japanese will have some very low-cost and advanced DRAM capacity become available that will contain equipment close to being written off the books, and that should already have provided a minimum of three good years of DRAM profits. The end result could be large gains of market share for Japan in the ASIC and MPU arenas, due to severe price competition as the result of low-cost manufacturing.

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PREPARING FOR THE ASIAN AGE: A RUSH OF NEW SEMICONDUCTOR PLANTS COMING ON-LINE

SUMMARY

Asia's silicon age has arrived. The rapid growth in personal computer, office automation, and consumer electronics production is causing the construction of 39 new semiconductor plants. Most of the activity is centered in South Korea and Taiwan, but Australia, China, Hong Kong, Malaysia, Singapore, and Thailand are also seeing fast growth. In anticipation of the expected worldwide industry slowdown, major Japanese, U.S., and European companies are eyeing Asia's rapid growth as a countercyclical strategy. Dataquest expects to see more new plant announcements as companies prepare for the "Asian age."

THE DRIVING FORCES BEHIND THE INVESTMENT BOOM

Market opportunities in Asia are clearly driving the investment in new semiconductor plants. In 1988, Dataquest estimates Rest of World (mostly Asia) semiconductor consumption at $6.1 billion, up 55.6 percent from 1987. By 1991, we expect the Asian semiconductor market to reach $9.9 billion, surpassing Europe in size.

The booming personal computer (PC) industry has created tremendous pressure for local production. Dataquest estimates that Asian PC production jumped to 4.9 million units in 1988, up 34.6 percent over 1987, and that it will reach 7.6 million units by 1991. Currently, PCs account for almost 30 percent of semiconductor demand. Due to the rapid growth in PC production, we expect the PC device market to grow from $1.8 billion this year to $2.9 billion by 1991. ASICs and chip sets will be the fastest-growing sectors.

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Dataquest observes numerous factors behind the current rush of new semiconductor investment in Asia. Some of these factors, listed by country, include the following:

- Taiwan's dynamic PC clone, consumer, and industrial electronics sectors have led to a serious memory shortage and the opening of 40 ASIC design centers. These factors have prompted government interest in expanded semiconductor production capacity.
- South Korean conglomerates are investing heavily in new semiconductor plants to achieve self-sufficiency and to respond to the huge demand for memory chips.
- Foreign companies are opening plants in mainland China to take advantage of the growing demand for semiconductors.
- The Singapore government pays 100 percent of new plant investments, and by doing so, has attracted Chartered Semiconductor, Hewlett-Packard, and NEC assembly plants.
- Thailand is experiencing massive investment by Japanese companies. MITI estimates that 277 Japanese companies in all sectors opened their doors in Thailand in 1987, and 670 opened in the first nine months of 1988 alone.
- Malaysia has 16 U.S. semiconductor firms, making it the world's third-largest semiconductor exporter, and offers tax breaks and duty-free imports of equipment, materials, and technologies.

Table 1

New Semiconductor Plants Planned for Asia, 1988–1996
(Exchange Rates: US$1 = ¥120, W 680, Y 3.73)

Company	Location	Cost (US$M)	Start Mfg.	Plant Type*	Initial Products	Wafer Size	Wafers/ Month**
			South Korea				
Daewoo	Guro	N/A	Q3/88	Fab	Zymos chip sets	4"	10,000
Goldstar #1	Woomyun	135.0	1988	Fab	CMOS memory	6"	18,000
Goldstar #2	Chongju	2,200#	Q4/90	Fab	1Mb DRAM,256K SRAM	6"	45,000
Goldstar #3	Chongju	above	1993	Fab	4Mb DRAM,1Mb SRAM	6"/8"	90,000
Goldstar #4	Chongju	above	1996	Fab	16Mb DRAM,4Mb SRAM	6"/8"	135,000
Hanil	N/A	7.0	1989	Fab	GaAs laser diodes	N/A	N/A
Hyundai #4	Ichon	N/A	Q1/90	Fab	1Mb DRAM	6"	40,000
Hyundai #5	Ichon	450.0	Q4/90	Fab	4Mb DRAM	6"	20,000
Sammi	N/A	7.0	1989	Fab	GaAs laser diodes	N/A	N/A
Samsung #3	Suwan	N/A	Q1/88	Fab	1Mb DRAM	6"	22,400
Samsung #4	Kiheung	N/A	Q1/89	Fab	1Mb DRAM	6"	18,000
Samsung #5	Kiheung	514.7	Q4/89	Fab	4Mb DRAM	6"	30,000

(Continued)

Table 1 (Continued)

New Semiconductor Plants Planned for Asia, 1988–1996
(Exchange Rates: US$1 = ¥120, W 680, Y 3.73)

Company	Location	Cost (US$M)	Start Mfg.	Plant Type*	Initial Products	Wafer Size	Wafers/ Month**
			Taiwan				
AMPI	Hsinchu	5.3	Q3/88	Fab	Power & consumer ICs	4"	8,000
Diodes Inc.	Taipei	N/A	1989	Fab	Diodes	N/A	N/A
HMC	N/A	N/A	Q4/89	Fab	Memory,telecom ICs	5"	30,000
Hualon	Hsinchu	200.0	Q3/88	Fab	Memory, consumer	5"	25,000
TSMC(ERS0)	Hsinchu	32.5	Q2/88	Fab	Memory, telecom ICs	6"	10,000
TSMC	Hsinchu	220.0	Q4/89	Fab	CMOS foundry	6"/8"	30,000
UMC(Phase I)	Hsinchu	140.0	Q1/89	Fab	Memory,MCU, graphics	6"	30,000
Vitelic	Hsinchu	80.0	Q3/90	Fab	Memory	6"	10,000
Winbond	Hsinchu	50.0	Q4/88	Fab	SRAM, ASIC, consumer, telecom	5"	20,000
			China				
Wuxi	Wuxi	N/A	1991	Fab	Integrated circuits	N/A	100MU/yr##
Motorola	Tianjin	N/A	1990	Fab	Discrete, ICs	6"	N/A
Philips	Shanghai	N/A	Q4/89	Fab	TV/VCR ICs	N/A	70MU/yr
Shanghai #17	Shanghai	N/A	Q3/88	Fab	Consumer	N/A	N/A
			Hong Kong				
Motorola	Hong Kong	50.0	Q3/89	A/T	Analog, memory, MPR, ASIC	N/A	N/A
			Singapore				
Chartered	Singapore	50.0	Q2/89	Fab	CMOS ASICs	6"	5,000
HP	Singapore	N/A	N/A	Fab	GaAs	N/A	N/A
Matsushita	Singapore	N/A	1988	A/T	N/A	N/A	N/A
NEC	Singapore	12.5	1989	A	256K/1Mb DRAM	N/A	1.5MU
					Linear	N/A	500KU##
			Malaysia				
Fujitsu	Kuala Lumpur	25.8	Q1/89	A/T	CMOS memory, logic and linear ICs	N/A	N/A
Hitachi	N/A	N/A	Q3/87	A	1Mb DRAM	N/A	10KU
Motorola	Seremban	48.0	Q3/88	Fab	Small signal trans.	N/A	N/A

(Continued)

Table 1 (Continued)

New Semiconductor Plants Planned for Asia, 1988–1996
(Exchange Rates: US$1 = ¥120, W 680, Y 3.73)

Company	Location	Cost (US$M)	Start Mfg.	Plant Type*	Initial Products	Wafer Size	Wafers/ Month**
			Thailand				
Shindengen	N/A	N/A	Q3/89	A/T	Car electronics	N/A	N/A
Sony	AMD Thai.	N/A	1989	Fab	Bipolar	N/A	3.0MU
Sony	Bangkok	21.7	Q3/90	Fab	Bipolar	N/A	10.0MU
			Australia				
AWA Ltd.	Sydney	52.0	Q1/89	Fab	CMOS ASIC	6"	N/A
Ramax	Melbourne	45.0	1989	Fab	Ferroelectric ICs	N/A	N/A
University of Adelaide	Adelaide	N/A	1988	R&D	GaAs	N/A	N/A

*Type of plant: Fab = fabrication, A = assembly, T = testing
**Total available capacity, not current capacity utilization
#$2.2 billion Goldstar investment will cover three new plants
##MU = million device units per month; KU = thousand device units per month
N/A = Not Available

Source: Dataquest
February 1989

A LOOK AT THE SEMICONDUCTOR COMPANIES

The following sections are company-specific summaries of the new semiconductor plants being built in Asia.

AWA MicroElectronics Ltd./Australia

AWA MicroElectronics Ltd., Australia's largest electronics manufacturer, invested $52 million on a six-inch wafer fab for ASIC products in Sydney. With the 1.5-micron CMOS line, AWA hopes to capture 25 percent of the Australian ASIC market. AWA is a joint venture between AWA Ltd. (64 percent equity), British Aerospace Australia Ltd. (25 percent equity), and Australia's New South Wales state government (11 percent equity). The company has $24 million for future capacity expansions and technology upgrades.

AMPI/Taiwan

In September 1988, Advanced Microelectronic Products (AMPI) began operation of its $5.3 million fab in the Hsinchu Science-Based Research Park to produce power ICs and consumer ICs. The four-inch wafer line has the capacity to produce 8,000 wafers per month during 1989 and 1990.

Chartered Semiconductor/Singapore

Chartered Semiconductor Pte Ltd. is a joint venture between National Semiconductor (9 percent equity), Sierra Semiconductor (17 percent equity), and the Singapore government (74 percent equity). Starting in the second quarter of 1989, Chartered will begin producing CMOS ASICs at its $50 million plant in the Singapore Science Park. Sierra is providing its proprietary Triple Technology CMOS process, while National is providing CMOS process technology, technical training, construction support, and clean room start-up assistance. National also has a testing and packaging facility in Singapore.

Daewoo/South Korea

Daewoo recently finished installing a new four-inch wafer CMOS line at its Guro plant in Seoul. This plant will produce Zymos chip sets and ICs used in PC and telecommunications applications. The capacity is 10,000 wafers per month.

Diodes Inc./Taiwan

Diodes Inc. plans to produce high-precision, high-value-added diodes for sales to the United States at a new plant near Taipei. Production and test equipment currently are being installed.

Fujitsu/Malaysia

In June 1988, Fujitsu Microelectronics began building a semiconductor plant near Kuala Lumpur. This plant will assemble and test MOS memories, standard logic, and linear ICs. The ¥3.1 billion ($25.8 million) plant is scheduled to begin operations in early 1989, and has 7,500 square meters of floor space.

Goldstar/South Korea

Goldstar plans to invest $2.22 billion by 1996 on three new fabs in its semiconductor manufacturing complex in Chong-ju. The plants will be scheduled as follows:

- Phase 1 (1988-1990)—1Mb DRAMs, 0.8-micron process, six-inch wafers, 540,000 MOS wafers annual capacity
- Phase 2 (1992-1993)—4Mb DRAMs, 0.6-micron process, six- or eight-inch wafers, 1,080,000 wafers annual capacity
- Phase 3 (1995-1996)—16Mb DRAMs, 0.4-micron process, six- or eight-inch wafers, 1,620,000 wafers annual capacity

Dataquest estimates Goldstar's semiconductor sales at $120 million. Goldstar plans to increase its sales to W 500 billion ($735 million at US$1 = W 680) by 1991, W 1.5 trillion ($2.2 billion) by 1994, W 3.2 trillion ($4.7 billion) by 1997, and W 4.5 trillion ($6.6 billion) by the year 2000, placing it as one of the top 10 semiconductor producers worldwide.

Hanil/South Korea

Hanil will produce gallium arsenide (GaAs) light-emitting and laser diodes for sales through Kujke Corp., a subsidiary of Hanil.

Hitachi/Malaysia

In September 1987, Hitachi Semiconductor began 1Mb DRAM assembly in Malaysia at the rate of 10,000 units per month.

HMC/Taiwan

In 1988, Hualon Microelectronics (HMC) opened a wafer fab in the Hsinchu Science-Based Research Park to produce 1.5-micron CMOS SRAMs and DRAMs on five-inch wafers. The total capacity is 25,000 wafers per month.

Motorola/China

Motorola announced a plant for ICs and telecommunications that will reportedly cost several hundred-million U.S. dollars. No details are available.

Motorola/Hong Kong

In August 1988, Motorola opened a 320,000-square-foot plant for assembly and testing of analog ICs for surface mounting. Dubbed "Silicon Harbor," the three-story facility will be fully operational in mid-1989 and employ 1,200 people.

Motorola/Malaysia

Motorola began producing small-signal transistors at its $48 million plant in Seremban, Malaysia. The plant has full manufacturing capability—from wafer production to final assembly and test. All output will be exported. Motorola expects to employ 500 people and produce $75 million to $100 million annually when the fab reaches full capacity in 1991.

Hitachi/Malaysia

In August 1988, Hitachi began assembling 1Mb DRAMs at a rate of 10,000 units per month.

NEC/Singapore

NEC plans to begin 1Mb DRAM assembly in Singapore next year at the rate of 500,000 devices per month, using wafers from Japan. In comparison, NEC Scotland manufactures 100,000 devices monthly. Recently, NEC Singapore Electronics increased

its 256K DRAM production to 3 million units per month and began linear IC test manufacturing in September. NEC Electronics Singapore, established in 1976, is 100 percent owned by NEC.

Philips/China

In June 1988, Philips signed a joint venture agreement with Shanghai No. 7 Semiconductor Factory to form the Shanghai Philips Semiconductor Company. The venture will produce 70 million ICs annually for radios, televisions, and future VCRs. Philips, the majority holder, will provide bipolar technology, pending export approval from the Belgium government and Cocom.

Ramax/Australia

In July 1988, Ramax received $5 million to develop a ferroelectric RAM (FRAM). A new $45 million fab will begin operations in Melbourne in 1989. Ramax paid $8 million for a 17 percent equity in Newtech Development Corporation of Sydney. This will go to Ramtron, along with $6.9 million in licensing fees to develop ferroelectric technology at the University of Colorado at Colorado Springs and the Michigan Technology University.

Shindengen/Thailand

Shindengen Electric Manufacturing shifted its production of car electronic devices from the Philippines to Thailand this fall. It will begin production on consignment starting in mid-1989.

Sony/Thailand

In August 1988, Sony announced plans to build its first overseas semiconductor plant in Thailand to manufacture bipolar ICs for compact disc (CD) players and other audio products. The ¥2.6 billion ($21.7 million) plant will be located in Bangkadi Industrial Park outside Bangkok. Construction will begin in 1989, with completion in mid-1990. In the interim, Sony will lease production space from AMD Thailand and produce bipolar ICs at 3 million units per month with a work force of 150 starting in April 1989. When the new 6,000-square-meter plant opens in 1990, production will increase to 10 million units per month.

TSMC/Taiwan

Taiwan Semiconductor Manufacturing Company (TSMC) is a joint venture between the Taiwanese government and N.V. Philips of The Netherlands. TSMC maintains two fabs. Fab I is an existing fab being leased from the Electronic Research and Service Organization (ERSO) for $2.5 million annually, in which TSMC invested $30 million for new equipment. Having opened in mid-1988, it has a capacity of 10,000 six-inch wafers per month. Fab II is a new $220 million plant in Taiwan's Hsinchu Science-Based Industrial Park. Construction began in April 1988 and is scheduled for completion by the end of 1989. Plant capacity will be 30,000 six-inch CMOS wafers per month when it is fully operational. Production will center on 1.2-micron feature sizes. Intel, Motorola, and Texas Instruments have entered long-term purchase commitments with TSMC.

UMC/Taiwan

United Microelectronics Corp. (UMC) has completed a new wafer fab in the Hsinchu Science-Based Research Park. Operations will occur in two phases. In Phase I, beginning in the first quarter of 1989, UMC will produce 10,000 six-inch wafers per month using a 1.0-micron, double-metal CMOS and NMOS process. Products will include MCUs, memory, graphics, speech chips, telecommunications ICs, and ASICs. In Phase II, beginning in the first quarter of 1990, UMC will produce 20,000 wafers per month, adding $210 million in revenue. Total plant investment will be $80 million for Phase I and $60 million for Phase II.

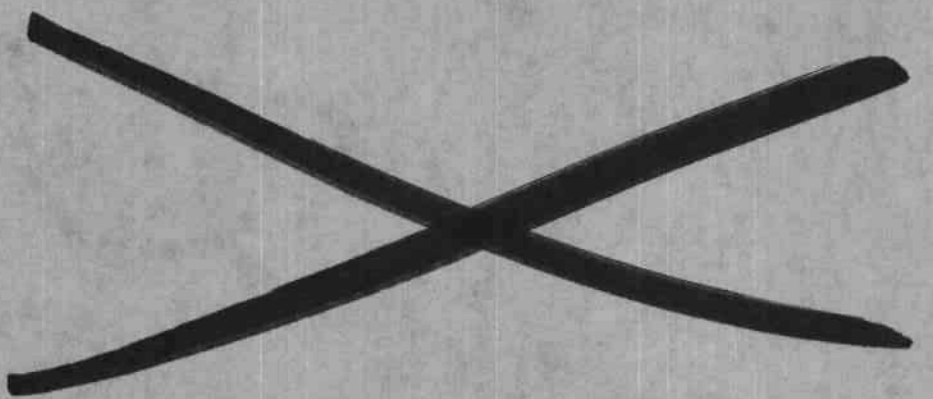
Winbond/Taiwan

Winbond, established in September 1981 by Dr. D.Y. Yang and Dr. Dean Chen of ERSO-ITRI, began operations of its $50 million wafer fab in September 1988 to produce 256K and 1Mb SRAMs, ASICs, telecommunications, PCs, peripherals, and consumer ICs designed by ERSO. The plant has a capacity of 15,000 five-inch wafers per month. In March 1988, ERSO transferred its CMOS VLSI technology to Winbond, giving it the capability of handling 1.2- to 5.0-micron CMOS and NMOS processes. Winbond's fab is 70 percent owned by Wal Sin Li Hwa, Taiwan's largest cable and wire maker. H&Q Taiwan Ltd., an affiliate of H&Q Venture Partners, invested NT$10 million ($333,000) in Winbond.

Wuxi Microelectronics Project/China

The Wuxi Microelectronics Project, begun in January 1988, plans to finish construction of a semiconductor plant and scientific research center by 1991. The facility, occupying a total area of 70,000 square meters, will have a production capacity of 100 million ICs per year.

Mark Reagan
J.H. Son
Sheridan Tatsuno



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Research Newsletter

EUROPE 1992: A MODEL INDUSTRIAL POLICY FOR THE SEMICONDUCTOR INDUSTRY?

This newsletter discusses semiconductor manufacturing in Europe. It looks first at present wafer capacity in Europe in comparison with the United States and then looks at the effectiveness of Europe's 1992 policy on drawing new fabs into Europe. Our data suggest that in some ways, European semiconductor manufacturing already is state of the art and that its 1992 policy already is a success.

WAFER CAPACITY

Wafer Capacity by Technology

As Table 1 shows, the distribution of technology by wafer capacity is very similar in the United States and Europe.

TABLE 1
Wafer Start Capacity by Technology
Europe and the United States

	Europe	United States
BiCMOS	2%	2%
CMOS	32	35
MOS	23	21
Bipolar	43	42
	100%	100%

Source: Dataquest
December 1989

Wafer Capacity by Products

As can be seen in Table 2, the distribution of products produced in Europe differs in several ways from distribution in the United States.

Europe has a significantly larger proportion of its production dedicated to discretes than does the United States. The United States, on the other hand, has a significantly larger percentage of its production in ASICs and MPUs than does Europe. Surprisingly, Europe has a slightly larger percentage of its production in memory products than does the United States. One reason for Europe's slight edge is that all of Siemens' DRAMs are manufactured in Europe, and IBM, Motorola, and NEC all have sizable DRAM plants there.

TABLE 2
Wafer Start Capacity by Products
Europe and the United States

	Europe	United States
Analog	14%	11%
Memory	20	17
MPU	7	13
ASIC	17	27
Logic	12	10
Discrete	29	18
Others	1	4
	100%	100%

Source: Dataquest
December 1989

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Wafer Capacity by Line Geometries

As can be seen in Table 3, the distribution of line geometries in Europe when compared with that of the United States has two distinct and somewhat opposite features.

TABLE 3
Wafer Start Capacity by Line Geometries Europe and the United States

	Europe	United States
>3.0 Microns	42%	18%
>2.5 and ≤3.0 Microns	22	14
>2.0 and ≤2.5 Microns	9	10
>1.5 and ≤2.0 Microns	4	23
>1.0 and ≤1.5 Microns	3	26
≤1.0 Micron	19	9
	100%	100%

Note: Columns may not add to totals shown because of rounding. Source: Dataquest December 1989

On one hand, Europe certainly has proportionately more of the older and larger technologies: 64 percent of its capacity is for devices greater than 2.5 microns, whereas in the United States only 32 percent of the capacity is for such devices. On the other hand, 19 percent of Europe's capacity is capable of doing 1.0 micron or less, compared with 9 percent in the United States. The reason for the large percentage of capacity capable of such small geometries is due to the large DRAM capacity in Europe.

1992-INDUCED FAB BOOM

The European Economic Community (EC) has ruled that, by January 1992, wafer fabrication should be performed within an EC country for ICs to be considered of local origin. Table 4 lists offshore companies that have announced, or Dataquest believes soon will announce, plans for wafer fabs in Europe.

As Table 4 makes clear, the EC's policy is effective. Fifteen new fabs will be built in Europe by foreign-owned semiconductor companies over

TABLE 4
Future Offshore Fabs in Europe

Company	Location	Year
Analog Devices	Limerick, Ireland	1991
Digital Equipment	Queensferry, U.K.	1990
Fujitsu	Newton Aycliffe, U.K.	1990
Fujitsu	Newton Aycliffe, U.K.	1992
Fujitsu	Newton Aycliffe, U.K.	1994
Hitachi	Landshut, U.K.	1992
IBM	Sindelfingen, West Germany	1991
Intel	Leixlip, Ireland	1993
ITT	Freiburg, West Germany	1991
Mitsubishi	N/A	1993
Motorola	East Kilbride, U.K.	1991
Samsung	Wasserburg, West Germany	1991
Texas Instruments	Avezzano, Italy	1990
Texas Instruments	Avezzano, Italy	1995
Toshiba	Braunschweig, West Germany	1991

N/A = Not Available

Source: Dataquest December 1989

the next few years. Some of these fabs would have been built anyway, but most of them will be built because of the EC's policy. Nowhere in the history of the IC has a government policy been so effective in getting semiconductor manufacturers to locate within its boundaries.

The EC's policy will also make semiconductor manufacturing in Europe more state of the art. At least six of these new offshore lines will be for DRAM manufacturing. The line geometries of the new offshore fabs will vary from a high of 1.25 microns for linear fabs to lows of 0.8 and 0.6 micron for DRAM fabs.

DATAQUEST CONCLUSIONS

The EC's policy regarding local origin is bringing in a large number of advanced fabs from offshore. This policy is so successful that it could well inspire other regions to have similar requirements. For larger companies this may not be too onerous a burden, because most of the major semiconductor companies already have plans to put fabs in all of the world's major regions. Smaller companies, however, may not have the resources to do this. Smaller semiconductor companies' use of offshore foundries is a viable way for them to have their devices fabricated overseas and remain competitive.

Europe 1992 will therefore increase the number of advanced fabs in Europe and speed up the pace of globalization of semiconductor manufacturing. It will also encourage the use of foundry services and thereby increase the number of alliances in the industry.

Other regions of the world could well adapt similar policies. These policies, together with generous financial "come-hithers," could cause the worldwide capacity for semiconductors to be higher than they otherwise would be . . . perhaps even higher than future business conditions justify.

George Burns

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Research *Newsletter*

SEMS Code: Newsletters 1989
Capacity Analysis
0005328

A COMPARISON OF JAPANESE AND U.S. FABS

This newsletter highlights an industry presentation recently given by industry analyst Mark T. Reagan. The presentation compared semiconductor manufacturing, fabrication facilities, and market response strategies in Japan and the United States.

- This presentation is limited to fabs that operate within the country of Japan and continental North America.
- The following analysis covers all fabs in the above-mentioned regions regardless of the origin of ownership.
- The following analysis does not include R&D locations, quick-turn ASIC lines, and fabs that handle compound semiconductor materials such as gallium arsenide.
- All comparative analyses include current fabs and fabs that have begun and will be beginning production during 1989.

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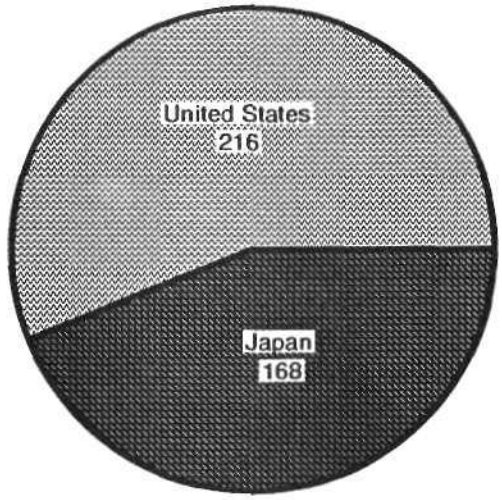
SILICON-BASED FABS



Production Lines

Source: Dataquest

Key points to note:

- In addition to the production lines shown, there are 99 pilot lines in the United States and 39 pilot lines in Japan.
- More fabs are located in the United States, but fabs in Japan have larger capacities and process larger wafers. This gives Japan more capacity in terms of square inches of silicon.
- The 216 production lines in the United States have 100 owners (a ratio of 2.2 fabs per company).
- The 168 production lines in Japan have 35 owners (a ratio of 4.8 fabs per company).
- Control of semiconductor manufacturing capacity in Japan is more concentrated than in the United States.

PRODUCT MIX

	Memory	MPU	Logic	ASIC	Other	Total
Japan	39%	7%	6%	14%	34%	100%
United States	25%	14%	8%	26%	27%	100%

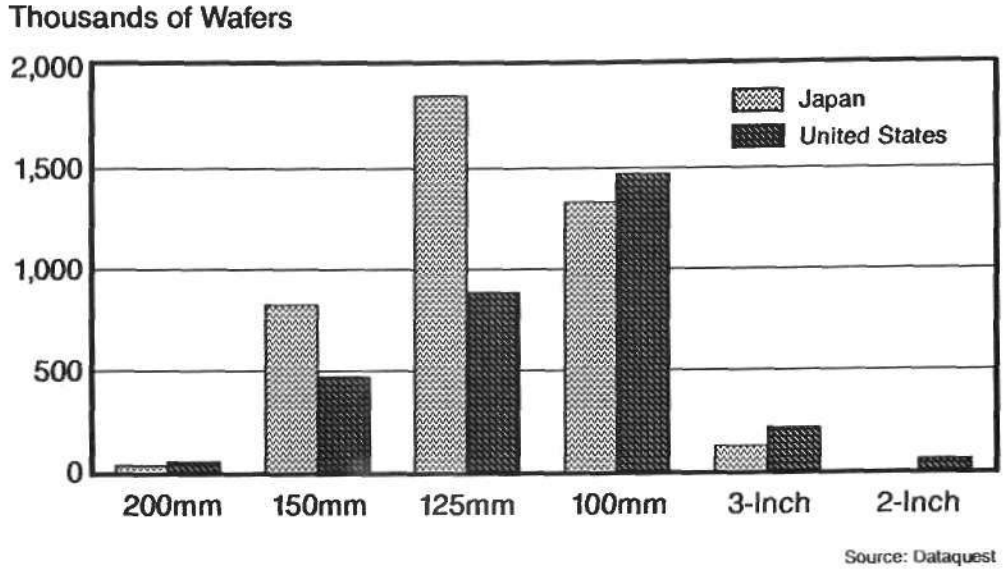
Source: Dataquest

Key points to note:

- This table shows the percentage of wafer start capacity by product measured in wafers per month.
- The total wafer start capacity in Japan is larger than in the United States.
- In terms of wafer start capacity, Japan has twice the memory capacity and six times the optoelectronic capacity of the United States.
- The United States has almost twice the MPU capacity and more capacity for ASIC and logic production than Japan.

SILICON PILOT AND PRODUCTION LINES

Monthly Capacity by Wafer Size



Source: Dataquest

Key points to note:

- This graph shows a comparison of total wafer start capacity by wafer size measured in wafers per month.
- Japan has 28 percent more 125mm lines than the United States (83 versus 65), yet has more than twice the 125mm wafer start capacity of the United States.
- Japan has 26 percent more 150mm lines than the United States (49 versus 39), yet has almost twice the 150mm wafer start capacity of the United States.
- The United States has 125 percent more 100mm lines than Japan (140 versus 62), and the capacities are almost equal.
- The average Japanese fab uses larger wafers and has higher wafer start capacities than the average U.S. fab.

MICRON MIX

	≤1µ	≤1.5µ	≤2.0µ	≤2.5µ	≤3µ	≥3µ
Japan	22%	30%	28%	0	14%	5%
United States	17%	31%	19%	3%	13%	19%

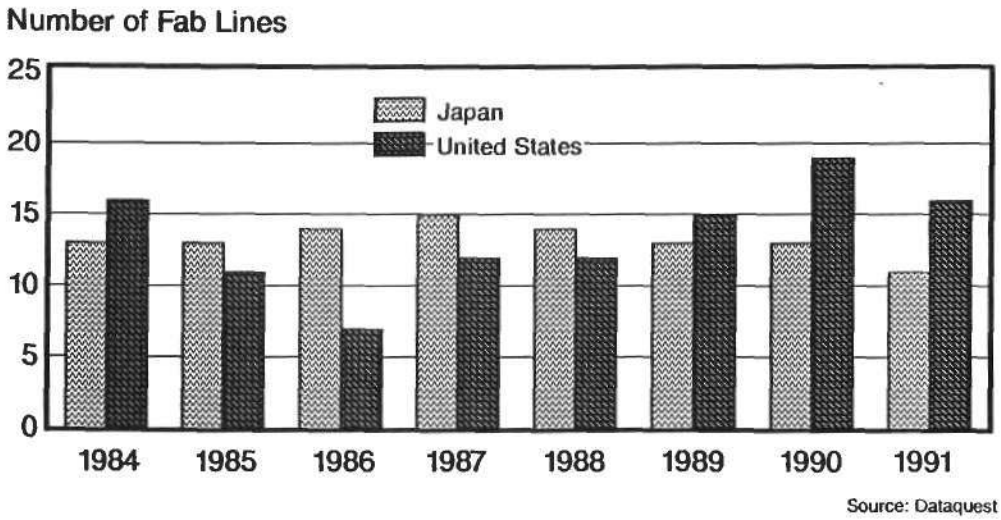
Source: Dataquest

Key points to note:

- This table shows the percentage of wafer start capacity by linewidth measured in wafers per month.
- The total wafer capacity in Japan is larger than in the United States.
- The relative absence of capacity in the 2.1– to 2.5–micron range is due to the natural technology jump from the 2.6– to 3.0–micron range down to the 1.6– to 2.0–micron range (an approximate 30 percent shrink for every new generation of technology).
- In the United States, 67 percent of capacity is at or less than 2 microns; in Japan, 80 percent is at or less than 2 microns.
- In the United States, 19 percent of capacity is at or more than 3 microns; in Japan, 5 percent is at or more than 3 microns.

ESTIMATED SILICON PILOT AND PRODUCTION LINES

Onshore Only



Source: Dataquest

Key points to note:

- This graph shows the estimated number of new fabs that have already begun and/or will go into production per year.
- Generally, more new fabs have been turned on in Japan each year during the last five years.
- The new production–based lines in Japan have average maximum capacities of 23,000 wafers per month, while the new lines in the United States have capacities of 16,000 wafers per month.
- New pilot lines in Japan also are larger, with average maximum capacities of 7,900 wafers per month compared with 3,600 wafers per month in the United States.
- Building and clean room construction in Japan has been fairly consistent from year to year (including downturns).
- The United States has more future fabs planned because of the aging of its existing capacity.
- Although more U.S. fabs will be added, their capacity will be less than the Japanese fabs.

- New fabs in Japan are brought up a with minimal amount of equipment during downturns.
  - This strategy allows the fabs in Japan to be more responsive to rapid demand increases when the upturn begins.
  - These partially equipped fabs have the basic manufacturing infrastructure in place and are well positioned for a rapid ramp–up by adding more people and equipment to the fab.

200mm PILOT AND PRODUCTION LINES

	Japan	United States
1987		IBM, Burlington
1988	NEC, Sagamihara IBM, Yasu Works	IBM, Burlington
1989	Fujitsu, Mie TI, Hiji Plant	TI, Dallas IBM, E. Fishkill IBM, Burlington
1990	Fujitsu, Iwate Hitachi, Musashi IBM, Yasu Works NEC, Sagamihara TI, Miho?	IBM, Burlington
1991	NEC, Chugoku Toshiba, Oita	NEC, Roseville TI, Dallas Tohoku Semiconductor
1992		Intel, Rio Rancho
1993	NEC, Chugoku Toshiba, Oita	

Source: Dataquest

Key points to note:

- Pilot– and production–based manufacturing on 200mm wafers is being driven by large companies that make DRAMs.
- Early U.S. entries into 200mm production have global manufacturing experience.
- Most of the known 200mm fabs will start with 4Mb DRAM production (later will move to logic, MPU, and some ASIC production).

FAB CONSTRUCTION TIMETABLE

	Permits and Planning	Break Ground to Complete Shell	Install Clean Room and Equipment	Turn On to Full Production
Japan	1 Year	7 Months	7 Months	6 to 9 Months
United States	5 Months	11 Months	11 Months	1 to 1 1/4 Years

Source: Dataquest

Key points to note:

- These figures reflect average times; there have been exceptions.
- From groundbreaking to full production, Japan takes approximately 20 to 23 months and the United States takes about 34 to 37 months: a 14-month advantage for Japan.
- In Japan, the permit and planning process mostly involves planning the fab; in the United States, this process mostly involves obtaining the required permits.
- The process in Japan, from groundbreaking to installation of the clean room and the equipment, is shorter because of the very detailed preplanning that is done in Japan; in the United States, most companies use the "design-as-you-build" method.
- Fabs ramp up very quickly in Japan for the following reasons:
  - More developed processes that are transferred into production
  - Better equipment vendor and user relationships
  - Strong knowledge and demonstrated capability in computer-integrated manufacturing

TWO APPROACHES TO BUILDING A FAB

Japan	United States
- One-step shopping for architecture, engineering, and construction	- Hire a person to act as a contractor
- Established relationships among owner, contractor, and subcontractors	- Contractor uses bidding system
- Very little bidding	- Company may not have the same subcontractors building all fabs

(Continued)

Key points to note:

- Dataquest recently witnessed some improvement and more cooperation in the United States between semiconductor companies and their architectural engineering companies.
- Time usually is not wasted on the bidding system in Japan; the contractors and subcontractors know that they will continue to get business as long as their work meets expectations.
- Established relationships have not been the norm in the United States because of the dominance of the bidding system.

TWO APPROACHES TO BUILDING A FAB

Japan	United States
- Less friction between subcontractors; teamwork	- Political friction
- Ergonomic coordination	- Get in each other's way
- Design and planning is completed before breaking ground	- Design as you build
- Changes usually are not allowed after ground is broken	- Delays due to internal conflicts and changes after the fact

(Continued)

Key points to note:

- Most Japanese subcontractors have worked together many times; therefore, they know one another's capabilities and working styles.
- It is common for U.S. semiconductor manufacturers to use different contractors and subcontractors for each project (due to the bidding system). Because of this system, there is less opportunity for teamwork and cooperation to develop between subcontractors.
- The design team must stay ahead of the builders and hope that no major changes are made later when using the "design–as–you–build" method.
- Many U.S. semiconductor manufacturers are not positive about equipment, processes, and fab layouts that will be needed by the time the decision must be finalized. This uncertainty results in delays.

TWO APPROACHES TO BUILDING A FAB

Japan	United States
- Contractor is responsible from design to installation of equipment	- Contractor usually not involved in the whole process
- Contractor guarantees operating performance and equipment installation schedule	- Subcontractors point fingers at each other

Key points to note:

- Japanese contractors usually guarantee a date when the clean room will be ready for equipment installation, as well as point-of-use cleanliness specifications for that equipment.
- When deadlines and performance specifications are not met in the United States, it is usually due to lack of planning and late decision making by the semiconductor manufacturer or to an environment that does not promote cooperation and teamwork between the subcontractors. This environment sometimes can be traced back to the competitive bidding process that currently exists in the United States.

Mark T. Reagan

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Research Newsletter

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Capacity
0004441

DRAM-SUPPLY WILD CARD: SAMSUNG TO THE RESCUE?

SUMMARY

First-tier Japanese DRAM suppliers have reaped high profits with their strategy of managing supply to control prices. As the threat of a market slowdown nears, several of these companies have indicated that they will continue to limit 1Mb DRAM production by shifting capacity to other scarce products, such as SRAMs or 4Mb DRAMs, in order to maintain the relatively high prices of 1Mb DRAMs. The question is whether or not the Japanese companies will succeed in this strategy. Dataquest believes that Korean and U.S. suppliers eventually may prove that Japanese manufacturers do not have as tight a control over the DRAM market as they think.

MANAGING PRODUCTION, CONTROLLING PRICE

When MITI instituted production cuts in the first half of 1987, many Japanese companies learned the lesson of managing supply to control prices. The irony is that the 1986 U.S.-Japan Semiconductor Trade Arrangement prompted these moves by MITI. Since then, production has been fairly limited by MITI based on demand measurements.

Today, however, several Japanese DRAM manufacturers have indicated that they will shift capacity to other scarce products (such as SRAMs) or new products (such as 4Mb DRAMs) if the market softens, in order to preserve the relatively high prices of 1Mb DRAMs. MITI has since dropped its production guidelines. DRAM procurers in the United States see quoted prices and directions from different Japanese companies that are suspiciously close, leading to a feeling of helplessness in the buying community.

Will the Japanese DRAM manufacturers succeed in implementing this strategy?

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ENTER THE WILD CARDS

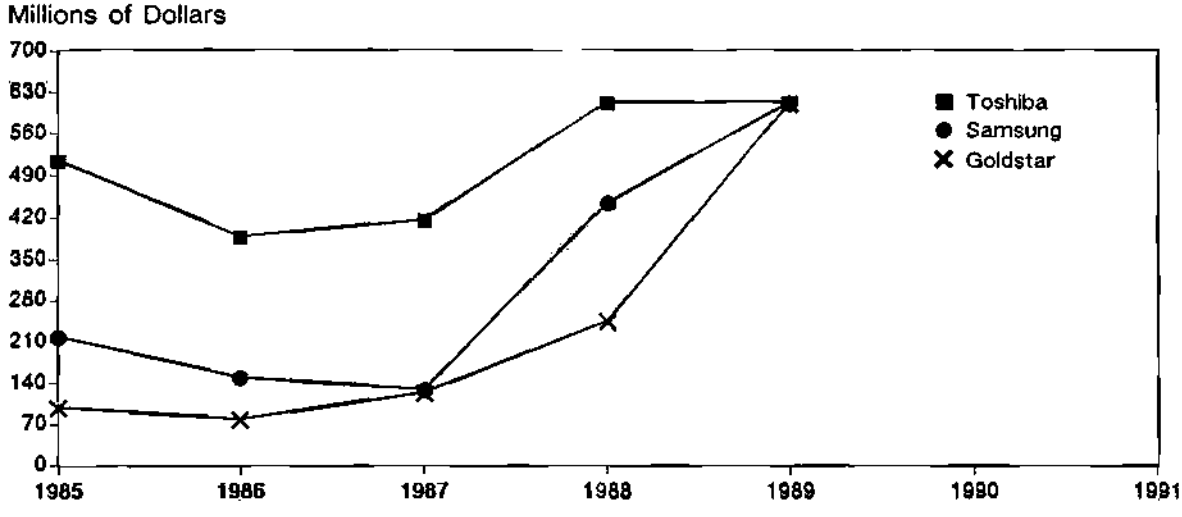
Toshiba has been in the forefront of the 1Mb DRAM market, outproducing others by two to one. Most Japanese companies have stopped trying to outpace Toshiba because of the dangers of excess capacity and the threat to 1Mb DRAM profits. Reports show that Toshiba plans to slow its production buildup in 1990.

The Japanese strategy's success depends on the level of control these companies exert over the 1Mb and 4Mb DRAM market and other factors.

As presented in Figure 1, Samsung's and Goldstar's capital spending have reached Toshiba's level. (Toshiba currently is the most aggressive Japanese manufacturer.) Reports predict that Samsung will have capacity up to 9 million units per month by the end of 1989, just a shade less than Toshiba, and has plans to increase production further while Toshiba slows its growth. Samsung's main challenge will be to increase production yield to 80ns parts and supply of product variations such as SIP/SIMM modules, and to qualify in a wider field of major OEMs.

Figure 1

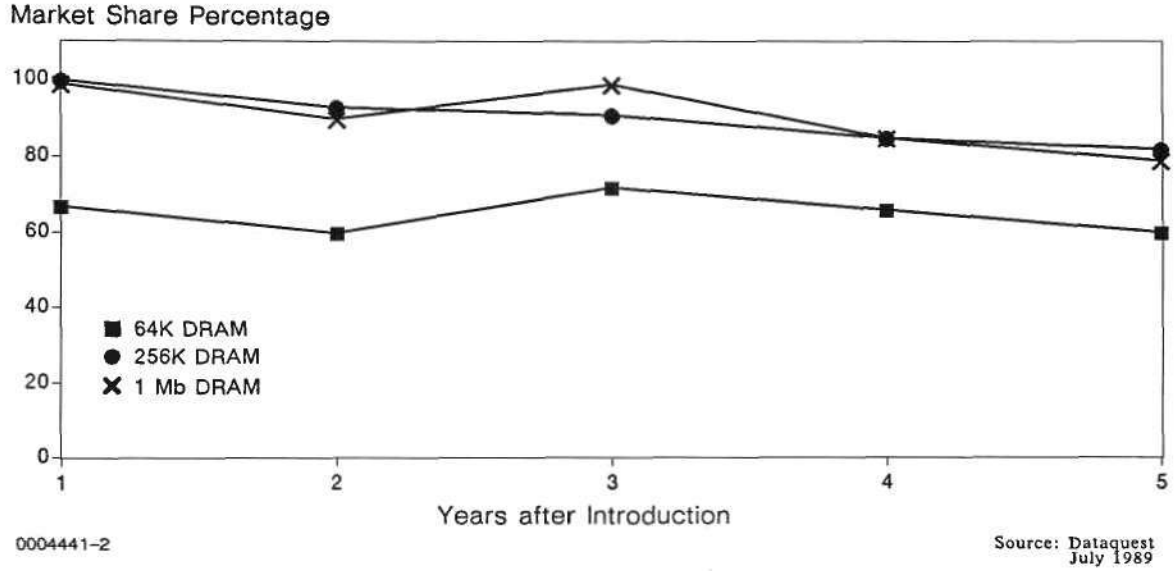
Estimated Semiconductor Capital Spending



With the entry of the Korean manufacturers, a wider field of 1Mb DRAM suppliers will exist in 1990. Estimates show that Japanese manufacturers as a group will have the same control over the market, in terms of market share, as they did with the 256K DRAM (see Figure 2). The 1Mb DRAM estimates assume greater participation by Goldstar, Hyundai, Micron Technology, Samsung, Siemens, and Texas Instruments.

Figure 2

Estimated Japanese Companies' Worldwide Market Share



With such aggressiveness displayed by other manufacturers, the top Japanese companies should be cautious about their strategic assumptions of market control. Although they are threatened in the 1Mb DRAM market, Japanese manufacturers will find good refuge in the profitability of the 4Mb DRAM, which they are ramping quickly.

Can the top-tier Japanese companies shift enough 1Mb DRAM capacity to other products? If these companies do maintain control over the 1Mb DRAM market, they can effectively reduce 1Mb DRAM production by shifting capacity to 32Kx8 SRAMs and 4Mb DRAMs. Dataquest estimates show that if Japanese companies increase the shipments of 32Kx8 SRAMs by 50 percent more in 1990 and use existing 1Mb DRAM capacity to build all 4Mb DRAMs, then they would have effectively cut 1Mb DRAM production by about 20 percent in 1990. Nevertheless, after successfully doing this, they would have reduced their market share in 1990 and their future control over the 1Mb DRAM market. By that time, however, we would hope that their emphasis would have shifted to the 4Mb DRAM.

In keeping the 1Mb DRAM prices up at the cost of market share, these leading Japanese companies also can keep the prices of 4Mb DRAMs, a market that they control, relatively high. The profits that could have been gained from the 1Mb DRAM will be reaped from the higher prices of the 4Mb DRAM.

DATAQUEST ANALYSIS

Korean, European, and U.S. companies currently have the momentum to change the control over the 1Mb DRAM market held by the top-tier Japanese companies. However, they face challenges other than production ramps, such as improving 80ns yields, widening their product offerings, and meeting major OEMs' stringent qualifications.

The top-tier Japanese companies have a plausible profit-maximizing strategy, but it hinges on the assumption that other manufacturers' production plans will slip. In following their strategy, Japanese suppliers will have to trade market share for profits, which means that they need to successfully ramp the 4Mb DRAM in order to keep overall worldwide DRAM market dominance.

DRAM procurers that have had difficulty returning the 1Mb DRAM to its learning curve path will need to try to qualify a wider field of suppliers, especially knowing the aggressiveness of the production plans of Korean companies.

George Burns

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Research Newsletter

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0004133

SCALING THE HEIGHTS: WILL ASIA/PACIFIC SURPASS EUROPE AS A CENTER FOR SEMICONDUCTOR PRODUCTION?

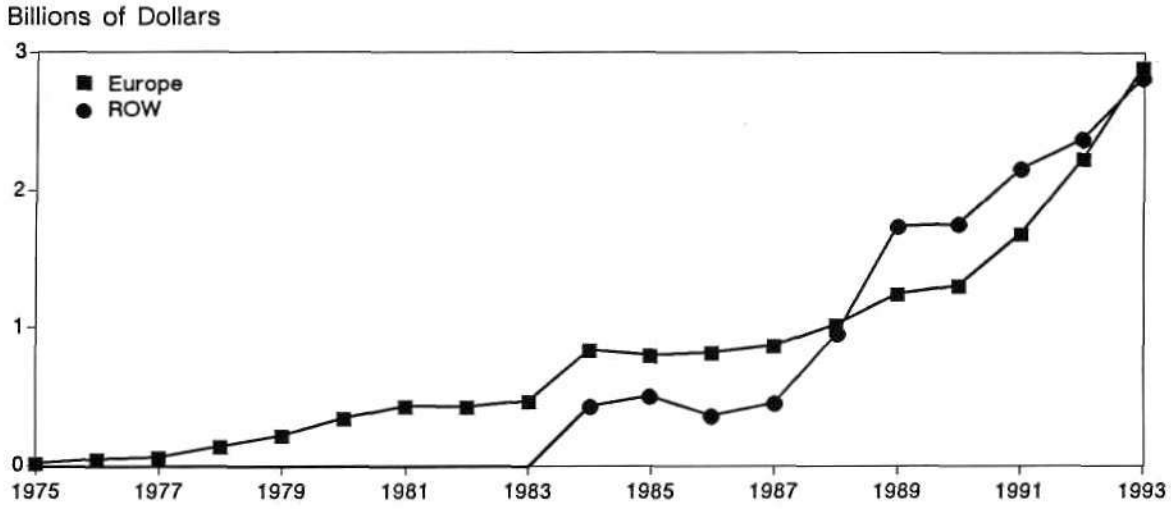
Capital spending and production in the Asia/Pacific region (includes Korea, Taiwan, Hong Kong, and Southeast Asia but not China) is expanding so fast that the Asia/Pacific area may soon surpass Europe as a center for semiconductor manufacturing. This shift may occur in spite of the accelerated European growth due to the integration of 1992.

CAPITAL SPENDING

Capital spending in the Asia/Pacific region jumped 110 percent in 1988, and Dataquest expects the increase in 1989 to be 84 percent. Samsung and Goldstar together will spend more than $1.2 billion in 1989; this amount is approximately equal to what all companies worldwide will spend in Europe in 1989. Only Toshiba, of all the semiconductor companies in the world, will spend as much in 1989. We do not, however, expect capital spending in the Asia/Pacific area to continue growing at this torrid rate. As can be seen from Figure 1, Dataquest expects spending increases in the Asia/Pacific area to moderate after 1989, while spending in Europe will increase in anticipation of 1992. By 1993, spending in Asia/Pacific and Europe will be approximately equal. The five-year growth rate for capital spending in the Asia/Pacific area is forecast to be 24 percent; in Europe, we forecast 23 percent.

Figure 1

Estimated Capital Spending in Asia/Pacific and Europe



0004133-1

Source: Dataquest
June 1989

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PRODUCTION

Front-end production in Asia/Pacific grew at a compound annual growth rate (CAGR) of 61 percent from 1983 through 1988. The Asia/Pacific region's share of worldwide front-end production grew from 1 to 3 percent during this period. We expect front-end production in the Asia/Pacific region to continue to grow faster than that of any other region of the world, representing a CAGR from 1988 through 1993 of 34 percent and propelling Asia/Pacific's share of worldwide front-end production to 7 percent by 1993.

The Asia/Pacific region is already home to many major semiconductor producers. (See Table 1 for a listing of companies with front-end facilities in the region.) SGS-Thomson has had three fabs in Singapore for a number of years. Taiwan is the home of many semiconductor companies, including Taiwan Semiconductor Manufacturing Corporation (TSMC), which is the world's largest foundry-only manufacturer. Samsung is already one of the world's top 20 semiconductor producers, and Goldstar plans to spend $2.5 billion during the next five years to achieve similar status.

Table 1

Asia/Pacific Region Fabs

Company	Country
Chartered Semiconductor	Singapore
Hewlett-Packard	Singapore
SGS-Thomson	Singapore
AMPI	Taiwan
Diodes Inc.	Taiwan
Fine Products	Taiwan
Formosa Plastics (future fab)	Taiwan
Hualon (HMC)	Taiwan
Texas Instruments/Acer (future fab)	Taiwan
TSMC	Taiwan
UMC	Taiwan
Winbond	Taiwan
Vitelic (future fab)	Taiwan
Motorola	Malaysia
Sony (future fab)	Malaysia
Daewoo	Korea
Goldstar	Korea
Hanil	Korea
Hyundai	Korea
KEC	Korea
Sammi	Korea
Samsung	Korea
Elcap	Hong Kong
Hua Ko Electronics	Hong Kong
RCL Semiconductors	Hong Kong

Source: Dataquest
June 1989

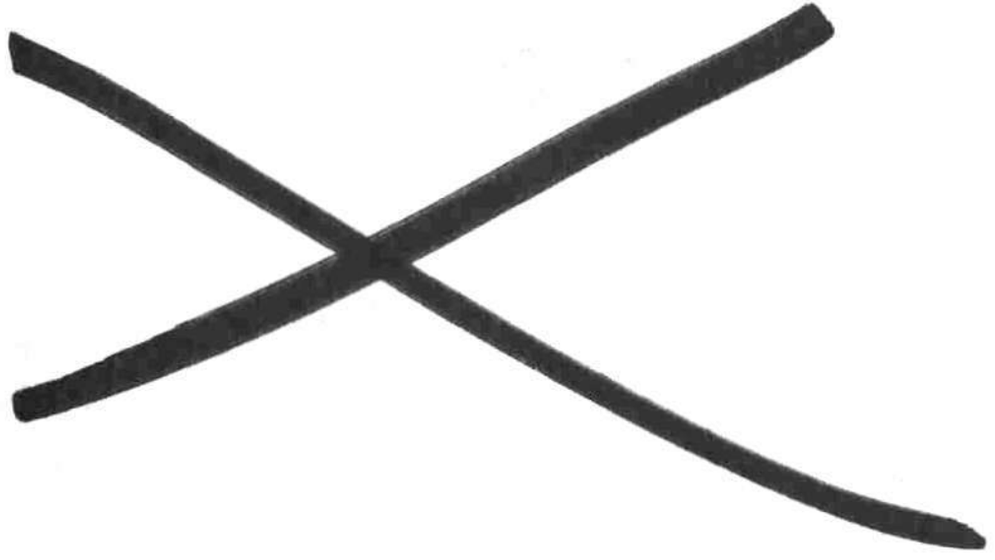
In 1973, production in Japan was approximately one-third that of the United States. Japanese production was one-half that of the U.S. region by 1980, and production in Japan had equaled production in the United States in 1983. Since then, Japan has gone on to become the world's major producer of semiconductors.

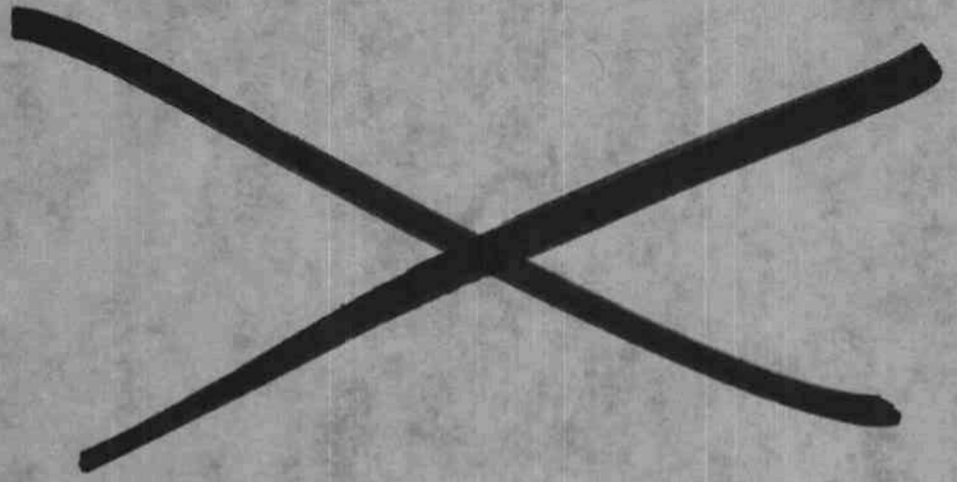
In 1988, production in the Asia/Pacific region was approximately one-third that of Europe. By 1993, we expect Asia/Pacific production to be one-half that of Europe. If the race between Asia/Pacific and Europe runs similar to the race between the United States and Japan, then production in the Asia/Pacific region could equal that of Europe by 1996.

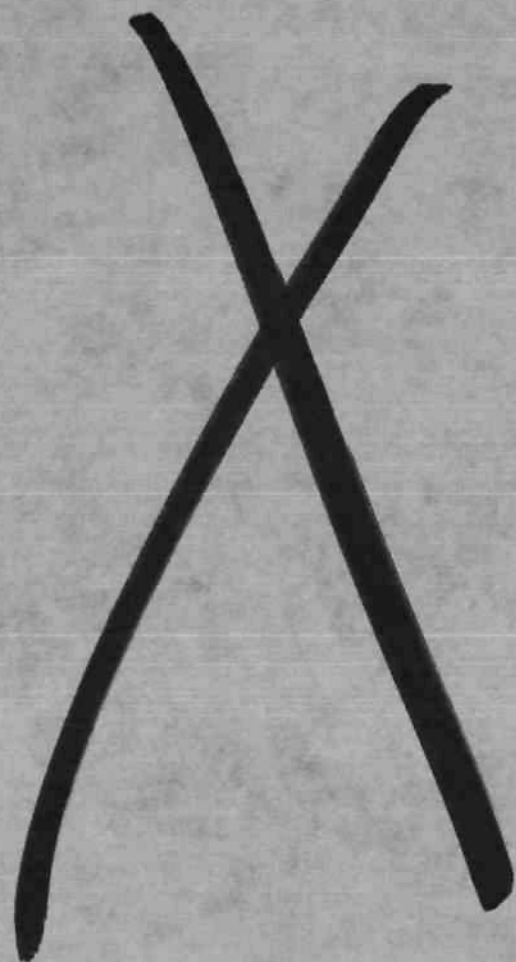
DATAQUEST CONCLUSIONS

Perhaps the growth of production in Europe, spurred by the impetus of 1992, will be such that Europe will not be overtaken as a center of semiconductor production. Clearly, however, the Asia/Pacific region is emerging from the shadows of a footnote at the bottom of market research charts. Asia/Pacific is now a major customer, competitor, and supplier in the world's electronics markets.

George Burns







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Research *Bulletin*

MAKE ROOM, SEMICONDUCTOR WORLD, HERE COME SOUTH KOREA AND TAIWAN

INTRODUCTION

Semiconductor production in the Asia/Pacific region is growing at a rate of more than twice the world's average (see SEMS newsletter number 0004133, entitled "Scaling the Heights: Will Asia/Pacific Surpass Europe as a Center for Semiconductor Production?" published in June 1989). Recently, analysts from Dataquest's Semiconductor Equipment and Materials Service (SEMS) and Asian Semiconductor and Electronics Technology Service (ASETS) visited Taiwan and South Korea to see firsthand evidence of this growth.

Ample evidence of economic growth was everywhere: The skylines were filled with factories and skyscrapers, and giant cranes were building more factories and skyscrapers. Taiwan shook in the grip of stock market fever. In both countries, experienced engineers have returned home from years spent at semiconductor companies in the United States to become the founding fathers of their local semiconductor industries.

Asia/Pacific has come of age technologically. It is now a force to be reckoned with by the giants in the semiconductor industry. The region also holds tremendous opportunity that some equipment companies may be missing through lack of adequate service.

COMPETITIVE DEVICE AND MANUFACTURING TECHNOLOGY

Asia/Pacific is quickly becoming technologically competitive in device technology with Europe, Japan, and the United States. GoldStar, Hulon, Hyundai, Mosel, Samsung, Taiwan Semiconductor Manufacturing Company (TSMC), Texas Instruments/Acer, United Microelectronic Corporation (UMC), Vitelic, and Winbond all either have just completed a new fab or are in the process of building facilities.

GoldStar, Hyundai, and Samsung in South Korea and Texas Instruments/Acer in Taiwan are building new DRAM fabs. Two other Taiwanese companies told Dataquest that they are seriously considering building a DRAM fab in the near future. Thus, not only is Asia/Pacific now manufacturing one of the industry's most technologically sophisticated devices, it also has the potential of affecting the supply and therefore the pricing of DRAMs (see SEMS newsletter number 0004441, entitled "DRAM Supply Wild Card: Samsung to the Rescue," published in July 1989).

Now the Asia/Pacific region is nearing technological parity with the rest of the world in device technology and manufacturing technology. For example, TSMC has just completed its second fab, which is the first fab in the world to use standard mechanical interface (SMIF) equipment from Asyst Technologies throughout its facility.

One of the major reasons for Asia/Pacific's rapid rise to near-technological parity has been the return to the region of engineers who trained and worked in U.S. semiconductor companies. In most of the semiconductor companies that were visited, many of the senior engineers were fresh from the United States. This talent pool, although a drain on U.S. resources, will be a source of continuing technological expertise for the Asia/Pacific region, as well as a source of entrepreneurial and managerial skills. (It should also serve to ensure close cultural and business ties with the United States.)

SEMS Newsletters 1989 Industry Issues

0005325

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ASIA/PACIFIC: THE UNDERSERVICED MARKET

Although the Asia/Pacific region does not appear to lack experienced engineers, the resources of new engineers are, in some cases, severely strained by the lack of local service support from semiconductor equipment vendors. Semiconductor manufacturers told Dataquest repeatedly that they often do not have local service support. Equipment vendors often had to fly someone to the country in order to support downed equipment. Because of this lack of support, fabs had to rely on their own engineering staffs for equipment service and maintenance that in other regions would be performed by equipment vendors.

Despite the large burden this lack of support places on semiconductor manufacturers, it also presents an opportunity for equipment vendors willing to put experienced personnel permanently in the region. Those equipment vendors that do not establish local support can be fairly sure that their local market will disappear.

George Burns

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Research Newsletter

WHAT'S REALLY GOING ON AT SEMATECH?

INTRODUCTION

During a recent visit to Austin, Texas, Dataquest had the opportunity to meet with SEMATECH's senior management and key staff members. We had many questions that originated from Dataquest analysts, Dataquest clients, and the press. During the visit, we realized that there are some misconceptions about what SEMATECH is doing and how SEMATECH will assist the U.S. semiconductor industry. SEMATECH certainly has come a long way during the past year. This newsletter will briefly explain the organization, the external networks, and the programs that SEMATECH has developed.

SEMATECH's management sent us a clear message that it cannot restore U.S. competitiveness on its own and that it is only part of the answer to restoring the U.S. semiconductor industry's competitive position. SEMATECH is focusing on what it believes to be the most logical and critical areas of technology where it, as a consortium, can yield the best return on investment for the U.S. semiconductor industry.

SEMATECH's focus on the U.S. semiconductor equipment and materials industry's health appears to have sharpened during the past year. Many programs aimed at improving the United States' competitive position have been launched. The general message from SEMATECH was strong: The United States will not be able to develop and maintain leading-edge semiconductor manufacturing capabilities without leading-edge United States-based equipment and materials vendors.

HOW SEMATECH WORKS

SEMATECH's mission is to provide the U.S. semiconductor industry with the domestic capability for world leadership in manufacturing. To achieve this goal, SEMATECH is prioritizing resources for maximum impact. Its priorities focus on the following three areas:

- Show stoppers—Critical tools and materials that the United States is in danger of losing access to or technology leadership in
- Key enablers—Tools and methods that would give members the biggest advantage in the shortest time
- High-risk and high-return manufacturing approaches

In order to identify the areas of manufacturing capability that will provide the highest leverage to the U.S. semiconductor industry, SEMATECH so far has completed 34 workshops throughout the United States. These workshops were attended by representatives from the member companies, SEMI/SEMATECH member companies, government, and universities. These workshops produced road maps for guiding R&D and established specific technological targets.

SEMATECH also is guided by its board of directors and 15 technical advisory boards (TABs). SEMATECH's board of directors includes one high-level executive from each member company as well as a representative from SEMI/SEMATECH and DARPA. The TABs consist of 1 executive TAB, and 14 focus TABs that provide expertise in specific areas of semiconductor manufacturing, as follows:

- Executive TAB
- Focus TABs
  - Assembly and Packaging
  - Design and Process Council
  - Environmental Safety

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- Facilities
- Lithography
- Manufacturing Systems
- Metrology
- Plasma Process
- Process Technology
- Quality
- Silicon Materials and Epitaxy
- Standards
- Technology Transfer
- Yield Management

The executive TAB is staffed by one high-level technologist from each member company. Focus TABs are staffed by experts in specific technical areas that represent the member companies and SEMI/SEMATECH member companies.

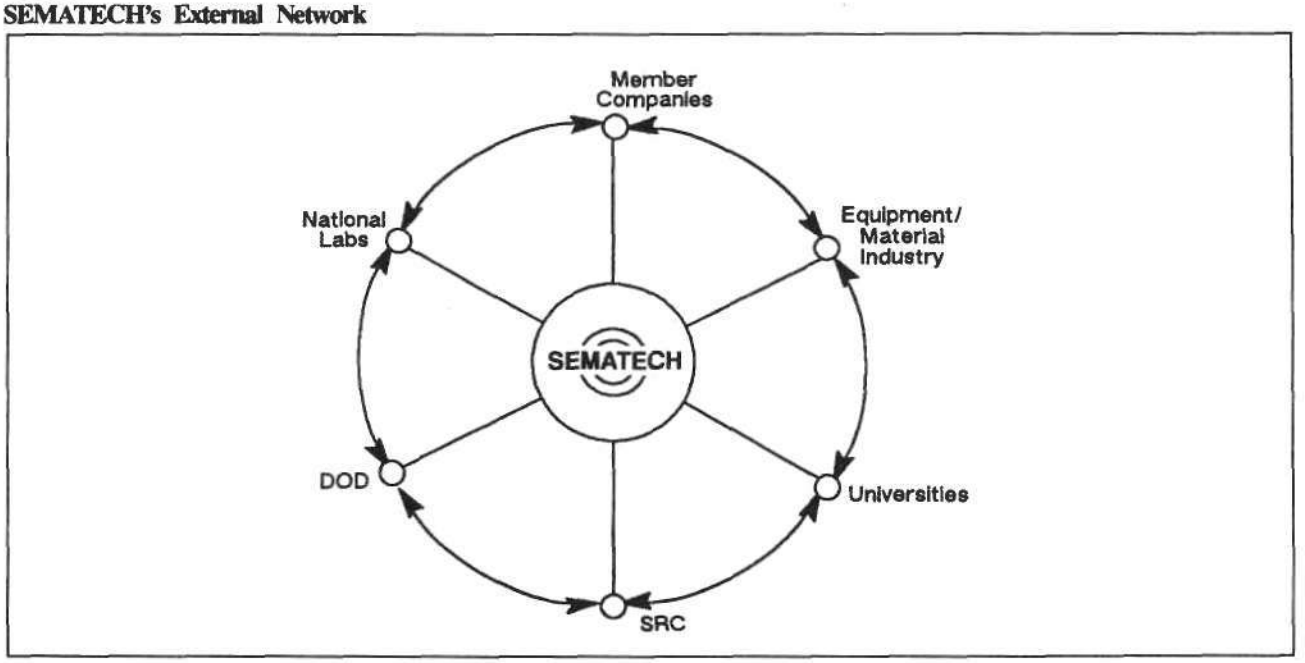
SEMATECH has set up an external network and organization that will maximize the capabilities of external resources. This external network makes SEMATECH the hub of a wagon wheel (see Figure 1) that has communication links with member companies, the equipment/materials industry, national labs, universities, the Semiconductor Research Corporation (SRC), and the Department of Defense (DOD). SEMATECH claims that its activities already have resulted in promising improvements in communication and teamwork for the U.S. semiconductor industry, which goes beyond SEMATECH's specific interests. These external industries have established communication links among themselves, something new for the mavericks in the U.S. semiconductor industry. Examples of these links include informal communication developing among member companies of SEMATECH and among member companies of SEMI/SEMATECH, as well as the teaming of three companies that will provide specialty gases and a delivery system to SEMATECH. Examples of improvement in links outside of SEMATECH's scope include the 25 companies that make up the MESA group and the recent announcement of the U.S. Memories joint venture. These are things that we think SEMATECH likes to see. SEMATECH will promote teaming and technology partnerships when synergistic fits are discovered. SEMATECH also will publish suggested equipment and materials standards for consideration by those industries.

Technology Transfer

Definition

SEMATECH's main product will be generic semiconductor manufacturing technology—i.e., knowledge of advanced semiconductor manufactur-

FIGURE 1
SEMATECH's External Network



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Source: SEMATECH

ing techniques rather than knowledge about how to make a certain device. It does not intend to deliver a DRAM, SRAM, or ASIC device process; rather, it intends to deliver generic subsets of semiconductor manufacturing technology continuously. Examples of these generic subsets could include delivery of an advanced planarization process or of deep UV lithography and photoresist technology. SEMATECH does "volume shortloops" at each generic subset in order to define, develop, demonstrate, and transfer the tools and materials, standards, techniques, and information required to improve U.S. semiconductor manufacturing capability. SEMATECH's fab is like several job shops under one roof, rather than a production-based fab line.

SEMATECH has a technology transfer group that serves the same function as the marketing department of a commercial company. The technology transfer group helps to define member needs, develops transfer methodologies, manages formal training and transfer sessions, provides after-transfer technical support, and evaluates transfer effectiveness. Continuous and effective delivery of the product is the most critical measure of SEMATECH's success.

Methods

Member companies of SEMATECH and SEMI/SEMATECH will not have to wait until 1993 before they see results; continuous technology transfer has already begun. The most important mechanism for effective technology transfer is people; i.e., the assignees that are sent to SEMATECH. Assignees stay at SEMATECH for approximately two years and travel frequently to their home companies with the information they have gathered. These assignees may travel to member companies, and, when necessary for critical technology transfers, assignees from one member company may even go into another member's fabs to ensure proper technology transfer. Member companies also send engineering teams to SEMATECH when necessary for proper technology transfer. In some cases, assignee visits to member company fabs will provide two-way communication between SEMATECH and its members. When SEMATECH needs to test manufacturing technology under high-volume conditions, it may do so at a member company's fab; feedback will be provided by the assignees who travel between SEMATECH and the particular member fab.

Although assignees are the most important mechanisms of technology transfer for SEMATECH, many other vehicles are being used to promote quality information exchange and technology transfer. These vehicles include forums, technical advisory board meetings, workshops, joint development projects, the tool-application program, the equipment-improvement program, the manufacturing-specialist program, and the new-graduate training program. General details of each program are as follows:

- Forums
  - SEMATECH held its first formal technology transfer forum during November 1988. This two-day forum covered issues related to designing, building, and starting up a 0.5-micron fab.
  - SEMATECH has held two President's Day conferences for SEMATECH members and SEMI/SEMATECH members; these conferences were attended by key officials from the member companies of SEMATECH and SEMI/SEMATECH.
    - The primary purpose of these conferences was to share plans for equipment and materials of the future.
    - Part of the agenda was to encourage teaming between suppliers and between suppliers and member companies.
- Technical advisory board meetings
  - Executive TAB (1)—This board consists of representatives from member companies and SEMATECH who review the SEMATECH strategy/focus and provide feedback. Bimonthly meetings are held.
  - Focus TABs (14)—Focus TABs are made up of representatives from member companies, SEMI/SEMATECH member companies, and SEMATECH who analyze competitive information, review specific technical areas (discussed previously), and provide feedback. One meeting per quarter is held for each of the focus areas.
- Workshops
  - Representatives from member companies, SEMI/SEMATECH member companies, universities, and SEMATECH attend the workshops to learn about tactical and strategic planning in specific technical areas.

- Joint development projects
  - Cofunded projects addressing advanced manufacturing capability are being organized by SEMATECH in conjunction with suppliers, supplier teams, or member companies.
  - Expenditures for joint development projects will represent approximately 40 percent of SEMATECH's annual budget.
  - Suppliers that benefit from SEMATECH programs will assure SEMATECH and its members a "right of first refusal."
- Tool-application program
  - Suppliers and member companies work side by side to identify and correct equipment performance problems.
  - The program is expected to shorten the equipment development cycle by at least six months.
  - It allows suppliers to move their equipment into the SEMATECH facility and correct problems during the development cycle before a tool reaches the member companies' manufacturing floors.
- Equipment-improvement program
  - Develop procedures, upgrades, and modifications to improve the performance of existing equipment
  - Demonstrate improvements in a manufacturing environment
  - Establish a method and mechanism for continued improvement of key equipment
- Manufacturing-specialist program
  - The manufacturing-specialist program provides training for the employees at member companies' fabs that is designed to promote individual commitment to quality at each process step.
  - It establishes a basic set of skills on various tools through a certification process.
  - The program helps operators build proficiency in the operation and maintenance of multiple tools within their own work areas.
  - It provides continuous training and development in operation, maintenance, and process control.
- New-Graduate Training Program
  - Selected college graduates receive specialized semiconductor manufacturing training in a "fast track" learning environment.
  - Within three years, the graduate trainees will rotate to member companies, where they can immediately apply this knowledge to improve member capabilities.

SEMI/SEMATECH

The SEMATECH mission statement mentioned show stoppers and key enablers as two of its three primary areas of focus. These show stoppers and key enablers indicate the need for links with the semiconductor equipment and materials industry. SEMI/SEMATECH was established as an independent organization of U.S. materials and equipment manufacturers to establish the primary communications link connecting the equipment/materials vendors, SEMATECH, and the member companies.

SEMI/SEMATECH's mission is to achieve continuous improvement in the relationship between users and suppliers of semiconductor equipment and materials. SEMI/SEMATECH's management is included on the SEMATECH board of directors and the executive TAB. SEMI/SEMATECH also is involved in almost every technology transfer vehicle that has been mentioned in this newsletter.

SEMI/SEMATECH represents 140 companies. Almost one-half of those companies have annual revenue equal to or less than $5 million. Many of these small equipment/materials companies are getting squeezed, and, in many cases, their survival is doubtful. However, these small companies are sources of entrepreneurial ideas and new technology. The impression is that some SEMI/SEMATECH companies are not happy with SEMATECH, that they feel left out. These members are asking questions such as: What is SEMATECH doing to keep the small companies alive?

SEMATECH is doing as much as it can for the SEMI/SEMATECH members, but SEMATECH also gives the impression that it is only part of the answer. SEMATECH is not equipped with an unlimited bankroll, so it must select equipment/materials vendors that are show stoppers or key

enablers. The vendors selected are expected to provide the most return on investment. SEMATECH simply cannot purchase products from, or work with, all 140 of the SEMI/SEMATECH members. However, SEMATECH will debrief all companies that were not selected after submitting a bid to SEMATECH for consideration. These one-on-one debriefings—along with the technology road maps generated from the focus TABs, workshops, and forums—are intended to provide a common direction for the U.S. semiconductor equipment/materials industry in R&D, design, and the development of new tools and materials.

SEMATECH will play matchmaker when it finds equipment/materials companies that would create a synergistic team or a logical acquisition. The impression Dataquest received during the SEMATECH visit is that consolidation of the U.S. equipment/materials industry will—and should—happen. The R&D spending levels that are required to stay in the semiconductor equipment/materials game are just too large for small companies.

DATAQUEST CONCLUSIONS

Dataquest believes that SEMATECH has achieved impressive results in a very short time. The most notable results include the following:

- The development of a well-thought-out organizational structure that will maximize the capabilities and expertise of industry, government, and universities in the United States
- Increasing levels of communication, cooperation, and teamwork within the semiconductor manufacturing industry, within the semiconductor equipment/materials industry, and between the users and vendors of semiconductor equipment and materials
- Completion of a wafer fab in 32 weeks
- Quick growth (SEMATECH quickly grew from 40 people in January 1988 to 400 people in December 1988; and by March 31, 1989, SEMATECH had 524 people on its staff.)
- Continuous formal and informal technology transfer that already has begun

SEMATECH appears to have chosen the most logical path when considering its aggressive mission and finite budget of $200 million per year. It has placed the U.S. equipment and materials industry at a very high priority level and is developing generic and critical technology that will benefit its members no matter what type of devices the members produce. SEMATECH has addressed the matter of how to demonstrate technology in a volume environment and how to transfer technology by using assignees as the main agents for technology transfer going to, and coming from, members' fabs. SEMATECH is also probably the most qualified organization for suggesting teams and acquisitions in the U.S. semiconductor industry, and it has the capability to build vast knowledge on the technology repertoire offered by the industry.

SEMATECH is performing ongoing X-ray lithography evaluations through its centers of excellence program; however, it currently does not have the resources to take on X-ray lithography as one of its programs. Dataquest believes that SEMATECH would like to see an X-ray lithography consortium put in place and that it also would urge the semiconductor equipment and materials industry to consider a consortium of its own.

Dataquest is impressed with what SEMATECH has accomplished so far, but SEMATECH cannot do everything for the U.S. industry. Japan's example of success is, at least partially, the result of many consortiums that have fostered good communication and cooperation in that country.

Mark T. Reagan

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Research *Bulletin*

Components Group 1989 Newsletters
1989–6
0004306

MEMORIES: YESTERDAY AND TOMORROW

Yesterday there were four U.S. merchant DRAM suppliers with silicon fabrication facilities: Alliance Semiconductor, Micron Technology, Motorola, and Texas Instruments. Soon there will be five. The new player on the U.S. scene is U.S. Memories.

U.S. Memories is an independent company started with seed money from seven U.S. semiconductor companies. The seven are: Advanced Micro Devices, Digital Equipment Corporation, Hewlett-Packard, Intel, International Business Machines, LSI Logic, and National Semiconductor. U.S. Memories currently is a company in the process of formation. For it to become a going concern, the company has listed the following preconditions: 1) that several more semiconductor companies provide financial backing; 2) that several systems companies provide financial backing and that this backing exceed the contributions made by the semiconductor manufacturers; 3) that participating systems companies guarantee to purchase 50 percent of U.S. Memories' output; 4) that negotiations for the transfer of IBM's submicron 4Mb DRAM technology be successfully completed; and 5) that a detailed business plan be completed. Full funding is contingent upon completion of these tasks.

The venture will require about $1 billion, with approximately half in the form of an equity investment and the other half from the financial community. By the end of 1989, the company hopes to have all of its preconditions met and to select a site. U.S. Memories plans to have a new fab built and producing in volume by the first half of 1991.

The president and CEO of the new company is Sanford (Sandy) Kane, who will be resigning soon from his present position as vice president of technology at IBM. Mr. Kane was instrumental in SEMATECH's founding and site selection. The chairman of the new company is Wilfred (Wilf) Corrigan, Chairman and CEO of LSI Logic.

DATAQUEST ANALYSIS

U.S. Memories emerged as a result of ongoing efforts by the Semiconductor Industry Association (SIA) to rejuvenate the present U.S. semiconductor industry. Successful formation of a large-scale company based on collaboration of multiple American semiconductor suppliers and systems manufacturers will be unique; this may be the first time in electronics industry history that a number of U.S. semiconductor manufacturers and their customers have shared resources, risk, and output. The purchase guarantee of 50 percent of the company's output will make the company structurally similar to many of its vertically integrated competitors such as Fujitsu and Hitachi, which also consume a large fraction of their own DRAMs.

The company believes that government support is crucial for its success. It does not expect support to be in the form of direct funding or subsidies, but rather, in the form of knocking down potential antitrust barriers. U.S. Memories believes that the federal government will be helpful in this regard.

U.S. Memories' targeted first half 1991 entry date into the 4Mb DRAM market is aggressive from a start-up development standpoint. Although the company's introduction date is ahead of the forecast peak year for 4Mb DRAMs, most Japanese DRAM manufacturers will be ramping up 4Mb DRAM production during 1990, and customer samples of 16Mb DRAMs will be available in 1991. Those companies that have reached volume production levels of 4Mb DRAMs by the time that U.S. Memories enters the market in 1991 could competitively price their products too low for a late entrant to compete, particularly when the FMV regulations elapse in 1991.

Obviously, a maverick cooperative project of this type has innumerable potential problems. However, the strong leadership of Sanford Kane, the endorsement and assistance from some of the most respected executives in the industry, and affiliation with the SIA all provide credence to this unusual start-up company. In addition, we believe that all of these factors should positively impact U.S. Memories' fund-raising efforts.

Yesterday there were four U.S. merchant DRAM manufacturers. Soon there will be five. Yesterday U.S. systems companies were uneasy about their perceived dependance on one set of "foreign suppliers." Tomorrow, with the advent of U.S. Memories, they hope to have taken a significant step toward regaining control of their own destinies. Yesterday U.S. semiconductor manufacturers were worried about losing control of the technology driver DRAMs. With the formation of Sematech last year and U.S. Memories this year, they believe that these efforts will improve their technological position.

George Burns
Fred Jones

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Research *Bulletin*

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Industry Issues
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HIGH-TECH BUSINESS OPPORTUNITIES IN INDIA

INTRODUCTION

Key opportunities exist for high-technology business in India. This bulletin discusses important recommendations by the Joint Scientific Committee, which was appointed by India's Prime Minister Rajiv Gandhi to outline a microelectronics blueprint for the next 10 years. The committee recommends free-market-driven, private-sector development of the electronics components and systems business in India, collaborating with leading foreign companies as needed. The Indian government would play a guiding role in defining technology road maps and coordinating industrial strategies.

The committee has identified several areas for short-term business development. These include design centers for ASICs, microprocessors, and gallium arsenide microwave ICs; semiconductor foundry facilities; and advanced printed circuit board and packaging technology. The markets for these technologies will include low-cost personal computers, office automation products, consumer appliances, telecommunications, and industrial automation. We at Dataquest believe that this information is of particular interest to our clients in the semiconductor manufacturing, equipment, and materials industries.

BACKGROUND

The world has seen the meteoric rise of countries such as Japan, Korea, and Taiwan, based on carefully orchestrated industrial strategies for penetrating all segments of the electronics food chain, from discrete devices to complete systems. Top government policy makers in India are increasingly aware of the importance of microelectronics and its value-added leverage in electronic systems. As shown in Table 1, the Department of Electronics has outlined ambitious production levels for India to become a world player in the electronics business.

Table 1

Semiconductor Components and Electronics Production
(Millions of Dollars)

Year	Annual Components Production	Annual Electronics Production
1988	$ 10	$ 4,500
1995	$ 800	$15,000
2001	$1,600	$30,000

Source: Department of Electronics
Government of India

India is the 10th-ranked industrial country in the world, with a population of 800 million and a gross national product of $225 billion. It has the third-largest engineering and scientific human resource base in the world. The English language is used widely for business communication. Recently, India has emerged as a powerhouse in software products and services. To round out its high-technology portfolio, India is currently embarking into VLSI design and manufacturing to meet the needs of advanced electronic systems.

BUSINESS OPPORTUNITIES IN INDIA

The following areas have been identified by the committee as short-term priorities for high-technology business development in India:

- VLSI design centers—The committee proposed that design centers be set in major industrial cities in India to encourage VLSI use in reducing system costs and improving system performance. Dataquest believes that significant opportunities exist for ASIC design, software, and CAD companies in India.

- VLSI fabs for ASICs—World-class semiconductor manufacturing capability is essential to India's electronic systems business success. Collaboration opportunities exist in setting up fabs for IC manufacturing. A high level of compatibility with ASIC design and software tools will be required. Foreign ASIC companies with a full range of CAD, software, and manufacturing capabilities will have an advantage in penetrating the Indian market.

- Microprocessor and digital signal processor design—The Indian government considers the development of microprocessors and digital signal processors essential for advanced system architectures. Companies with expertise in these areas have an opportunity for licensing their technology and developing a low-cost manufacturing source for their products.

- Microwave IC design—Domestic design capability development for GaAs microwave ICs for satellite communications is a priority. Opportunities exist for design and CAD collaboration. The devices will be manufactured by relevant partners at foundries in either Japan or the United States.

- Advanced printed circuit boards and VLSI packaging—The Indian government has emphasized the need for multilayer board technology and high-pin-count VLSI packaging using surface-mount and TAB techniques. Opportunities exist for semiconductor and board-assembly companies to expand in India.

DATAQUEST CONCLUSIONS

Dataquest believes that India offers exciting opportunities for high-technology companies to expand their markets. With its newly liberalized industrial policies, its tremendous technical resources, and its huge domestic markets, India could well be the next Asian economic miracle.

Krishna Shankar

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Research *Bulletin*

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MANUFACTURING: LOW VOLUME, MILITARY, AND EFFICIENT TOO?

Texas Instruments recently won a $112 million award from the United States Air Force for a five-year contract with the Microelectronics Manufacturing Science and Technology (MMST) program. The program is a cooperative effort by the Air Force Wright Aeronautical Laboratory's Manufacturing Technology Directorate and Electronic Technology Laboratory and the Defense Advanced Research Project Agency (DARPA).

Under the contract, Texas Instruments will develop the equipment and systems for cost-effective manufacturing of low-volume military integrated circuits, microwave devices, and sensors. The program will include the development of advanced processes, process equipment (such as dry chemical cleaning systems), process sensors, process control expert systems, and an integrated factory control system that can be scaled and adapted to a variety of fabrication facilities. These elements will be integrated into a pilot fabrication facility that will feature sub-0.5-micron line geometries, more than 1,000 designs per year with 800 wafers per month throughput, and a minimum cycle time of less than three days.

Texas Instruments hopes to push the state of the art in computer-integrated manufacturing (CIM) by research in processing and in-situ sensors, VHDL-compatible simulation, modeling, symbolic computing, and artificial intelligence computer-integrated processing.

Techniques and equipment developed under this program will be equally applicable to silicon, gallium arsenide, and mercury-cadmium-telluride-based process technologies.

To achieve maximum flexibility for minimum lot sizes, Texas Instruments is planning to replace traditional batch processing equipment with single-wafer processing systems. Diffusion furnaces, for example, might be replaced by single-wafer equipment. With single-wafer processing systems, equipment footprints will shrink dramatically--the entire manufacturing facility might take up no more than 2,500 square feet and cost just a fraction of what conventional facilities cost.

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Dataquest notes that this program has some broad implications. If Texas Instruments and the Air Force are successful at achieving the technical goals of this project, it could help solve crucial technology sourcing problems for future and ongoing defense programs. Because of the typically small order quantities, unique technologies (e.g., radiation hardening), and long life cycles of military semiconductor requirements, it has been difficult for the Department of Defense to secure a cost-effective, stable supply of ICs and sensors. The resulting fabrication technology from this project could be used to lower the overhead of operating a small-volume fabrication operation, thus preserving and even enhancing the supply base of companies that serve the military market.

Additionally, a recent report by the Japanese Technology Evaluation Program points out that Japanese semiconductor manufacturers are ahead of their U.S. counterparts in the implementation of CIM, especially for volume production such as that used for DRAMs. The authors of the report point out that experience in implementation of CIM in volume production could be transferred to nonvolume production such as that used for ASICs, and thus represent a strategic threat to the U.S. semiconductor industry in an area where it has traditionally been in the lead. However, techniques developed for low-volume military manufacturing in the MMST program are applicable to nonmilitary low volume production, and therefore, we believe, will help the U.S. industry maintain its leadership position in low-volume, flexible manufacturing.

Much has been said and written about the need for the U.S. industry and government to work together to keep the U.S. competitive in an increasingly competitive world. Dataquest believes that programs such as MMST's could be part of a successful strategy by government and industry to keep the U.S. semiconductor industry competitive on the world's shop floors.

George Burns
Greg Sheppard

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Research *Bulletin*

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COMPUTER-INTEGRATED SEMICONDUCTOR MANUFACTURING IN JAPAN: A LOOK AT TOSHIBA'S 1Mb DRAM PLANT

SUMMARY

At a recent U.S.-Japan Forum seminar at Stanford University, Dr. Bevan Wu, IBM's manager of Manufacturing Research, summarized the findings of a U.S. tour of Japanese manufacturing plants. The six-person study team was sponsored by the National Science Foundation (NSF) and the Defense Area Research Project Agency (DARPA). The goal was to understand state-of-the-art computer-integrated manufacturing (CIM) in Japanese companies. This bulletin focuses on CIM efforts in semiconductor plants.

SYSTEM INTEGRATION, NOT TOTAL AUTOMATION

Dr. Wu observed that the Japanese manufacturing managers surveyed introduce automation systematically into their plants, beginning with their customers and bookings, through design and process, and finally, back to the customer. They analyze the need for plant automation, asking such questions as: Are robots needed? If so, how will they be used? What is the ideal mix with human workers? By contrast, according to Dr. Wu, some U.S. companies invest heavily in automation without asking these questions or improving the efficiency of their existing operations. The DARPA team found that Japanese managers emphasized several key manufacturing principles: design for easy manufacturing, maintain control over the process, keep the process as simple as possible, and automate only where necessary. To avoid building rigidity into the manufacturing process, they employ human workers for small-lot, quick-turnaround products.

TOSHIBA'S 1Mb DRAM PLANT

Toshiba's 1Mb DRAM plant is an example of highly efficient manufacturing. Dr. Wu observed that Toshiba, like other Japanese chipmakers, has installed a global value-added network (VAN)--or "yellow brick road"--that links design, manufacturing, marketing, and distribution. The system enables anyone in the system to monitor the status of orders, production, and shipments. It was developed by 100 software programmers over a period of five years. At the manufacturing level, a linked data base integrates the various wafer processing steps: diffusion, chemical vapor deposition, dry etch, lithography, and ion implantation.

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Toshiba and other Japanese chipmakers have also introduced three-dimensional wafer maps showing yield variations to an accuracy of 3 to 4 percent. Graphs showing the turnaround time (TAT) to solve yield problems are constantly printed out to increase quality awareness and speed response time. Toshiba has reduced its TAT to 7 to 10 days from 7 to 25 days. By spotting yield problems quickly, Toshiba is able to produce higher-quality wafers.

Dr. Wu estimated that Toshiba's 1Mb DRAM plant has a monthly throughput of 50,000 wafers. Its process involves 550 manufacturing steps, 120 types of equipment, and about 400 pieces of equipment. Toshiba's CIM system has achieved stunning results, including the following:

- An estimated wafer yield of 80 percent (50 percent higher than before installing the CIM system)
- An average turnaround time (TAT) of 5 times the raw process time (RPT) at 100 percent loading—42 percent less than previously—compared with 10 times for the average U.S. semiconductor plants (Toshiba managers are aiming to reduce TAT to twice the RPT.)
- Only 15 minutes to calculate wafer probe yields and correlate its process data
- A 32 percent increase in the effective manufacturing time
- A 25 percent reduction in labor costs

Assuming a new 1Mb DRAM plant cost of $300 million, Toshiba could recover its total plant investment in three or four months by shipping 600 million units per year at current market prices, Dr. Wu estimated. As a result, he concluded that memory chip production is a huge cash generator for Japanese companies using CIM systems. At their peak, Japanese memory plants could efficiently process 1,000 wafer starts per day involving a total staff of 2,500 people, including all support. His most discouraging observation: "Even if the Japanese let us see everything in their plants, we could probably not duplicate it because of cultural and management differences." On the other hand, he believes that Japanese managers are not invincible.

DATAQUEST OBSERVATIONS

Dataquest believes that Dr. Wu's observations merit serious consideration because of his in-depth knowledge of IBM's memory production capabilities. Although his revenue calculations were conducted independent of actual market demand and industry capacity analyses, his insights into Toshiba's productivity gains and yield improvements are worth noting. However, Toshiba is using a proven planar process, while other Japanese are encountering difficulties with the more complex trench capacitor and stacked cell processes. Dr. Wu's discussion did not address how Japanese companies are addressing the dual problem of introducing new submicron processes and CIM systems.

For more information, the DARPA report entitled "CAD/CIM in Japan" can be obtained from Science Application International Corporation, 1710 Goodridge, McLean, Virginia 22102.

George Burns
Mark Reagan
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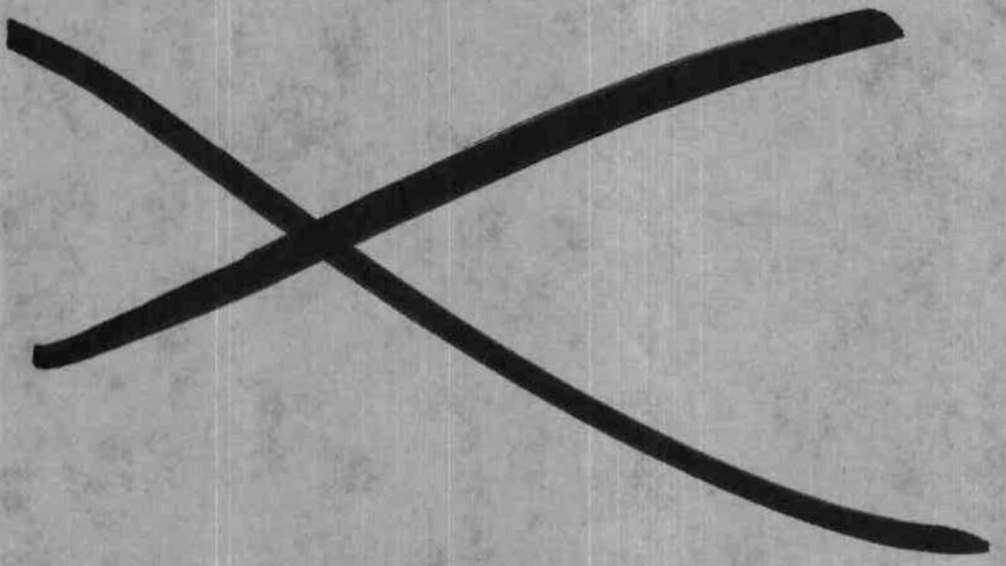

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February 5, 1990

SEMICONDUCTOR EQUIPMENT AND MATERIALS SERVICE

ERRATA

Dear Client:

In the SEMS December 1989 forecast newsletter entitled " Wafer Fabrication Equipment Forecast: The Near-Term Outlook," the line item for the CVD equipment forecast was inadvertantly omitted in Table 2. Please use the following information for the CVD equipment market forecast:

Worldwide CVD Equipment Market Forecast
(Millions of Dollars)

	1989	1990	1991	1992	1993	1994	CAGR (1989-1994)
CVD	540	530	675	875	1050	1150	16.3 %

We apologize for any inconvenience that this omission may have caused you. Please file this errata with the newsletter that is behind the Forecast tab in your binder.

Sincerely,

K Shankar

Krishna Shankar
Industry Analyst
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Research Newsletter

WAFER FABRICATION EQUIPMENT FORECAST: THE NEAR-TERM OUTLOOK

The growth of the economy has slowed visibly in the last few months, and the big question is will the economy begin a descent into a recession or will it "soft land?" Semiconductor equipment and materials suppliers are at the end of the electronic industry food chain, and changes in the general economy ripple down to their level with increasing effects. Thus, equipment and materials companies are very concerned about the near-term outlook.

Although government economic indicators are giving a muddled picture of the economy, a recent Dun & Bradstreet business conditions survey helps to clarify the situation. The D&B Business Expectations Survey, which sampled 1,500 executives in the manufacturing, wholesaling, and retailing sectors, indicates that although current economic lethargy will continue, the economy is not expected to descend into a recession, but will soft land. In addition, other surveys in the electronic sector by Dataquest point to the same conclusion.

This newsletter contains Dataquest's forecast for the wafer fab equipment industry. Our view is consistent in that we expect the near-term outlook for the wafer fab equipment industry to be lethargic as well, but no recession is predicted. In brief, we forecast that 1990 will be a year of zero growth but should be followed by several years of healthy activity.

SEMICONDUCTOR PRODUCTION AND CAPITAL SPENDING

Dataquest's estimates of worldwide semiconductor production, including merchant and captive production, for the 1989-1994 period are presented in Table 1. Note that semiconductor production doubles over this time period from $60.5 billion in 1989 to nearly $121.4 billion in 1994. Also shown is the capital spending required to support that production, and it more than doubles over the same period. Capital spending refers to outlays for wafer

TABLE 1
Worldwide Semiconductor Production, Capital Spending, and Wafer Fabrication Equipment Forecast, 1989-1994 (Millions of Dollars)

	1989	1990	1991	1992	1993	1994	CAGR 1989-1994
Semiconductor Production	$60,506	$61,460	$70,678	$85,130	$111,830	$121,386	14.9%
Growth	11.0%	1.6%	15.0%	20.4%	31.4%	8.5%	
Capital Spending	$12,245	$11,998	$15,119	$19,951	$ 24,876	$ 26,284	16.5%
Growth	21.4%	(2.0%)	26.0%	32.0%	24.7%	5.7%	
Wafer Fabrication Equipment	$ 5,779	$ 5,785	$ 7,170	$ 9,299	$ 11,330	$ 12,280	16.3%
Growth	18.4%	0.1%	24.0%	29.7%	21.8%	8.4%	

Source: Dataquest
December 1989

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fabrication equipment (front end), assembly and test equipment (back end), property, and plant.

FORECAST FOR WAFER FAB EQUIPMENT

Also included in Table 1 is Dataquest's forecast for the worldwide wafer fab equipment market. For the forecast years of 1990 to 1992, there is no significant difference between this year's wafer fab equipment forecast and the one that was presented last year. Then, we said that 1990 would be a slow year with 4 percent growth and that 1991 and 1992 will grow at 26 and 27 percent respectively. Now, we are predicting that 1990 will be essentially a flat year, but that 1991 and 1992 will grow at 24 and 30 percent. Essentially, then, our view of the 1990-1992 period is unchanged.

Dataquest segments the front-end equipment market into ten major categories that are discussed in the following sections. Our discussion is focused on the near-term market outlook and the trends for each equipment segment that will drive the wafer fab equipment market to the high growth years that are expected beyond the mediocrity of 1990. A five-year forecast by equipment segment is presented in Table 2.

TABLE 2
Worldwide Wafer Fab Equipment Market Forecast (Millions of Dollars)

	1989	1990	1991	1992	1993	1994	CAGR 1989-1994
Lithography							
Proximity/Contact	$ 20	$ 20	$ 22	$ 23	$ 24	$ 25	4.6%
Projection Aligners	152	148	180	235	287	303	14.8%
Steppers	1,084	1,142	1,421	1,858	2,335	2,516	18.3%
Direct-Write E-Beam	70	75	83	100	125	140	14.9%
Maskmaking E-Beam	70	78	91	116	143	150	16.5%
X-Ray	12	20	30	40	55	70	42.3%
Total Lithography	$1,408	$1,483	$1,827	$2,372	$ 2,969	$ 3,204	17.9%
Automatic Photoresist Processing Equipment	$ 282	$ 289	$ 356	$ 463	$ 564	$ 609	16.7%
Etch and Clean							
Wet Process	$ 289	$ 278	$ 350	$ 450	$ 560	$ 600	15.7%
Dry Strip	110	110	140	190	220	240	16.9%
Dry Etch	650	640	800	1,050	1,250	1,350	15.7%
Ion Milling	9	10	12	14	16	16	12.2%
Total Etch and Clean	$1,058	$1,038	$1,302	$1,704	$ 2,046	$ 2,206	15.8%
Deposition							
Physical Vapor Dep.	$ 400	$ 390	$ 490	$ 650	$ 750	$ 820	15.4%
Silicon Epitaxy	60	55	61	85	104	112	13.3%
Metalorganic CVD	52	62	74	90	108	128	19.7%
Molecular Beam Epitaxy	100	108	123	140	150	165	10.5%
Total Deposition	$1,152	$1,145	$1,423	$1,840	$ 2,162	$ 2,375	15.6%
Diffusion	$ 330	$ 300	$ 375	$ 480	$ 575	$ 625	13.6%
Rapid Thermal Processing	$ 27	$ 26	$ 34	$ 45	$ 60	$ 70	21.0%

(Continued)

TABLE 2 (Continued)
Worldwide Wafer Fab Equipment Market Forecast (Millions of Dollars)

	1989	1990	1991	1992	1993	1994	CAGR 1989-1994
Ion Implantation							
Medium Current	$ 153	$ 136	$ 168	$ 223	$ 272	$ 259	11.1%
High Current	302	262	320	412	484	470	9.2%
High Voltage	22	29	40	56	72	85	31.0%
Total Implantation	$ 477	$ 427	$ 528	$ 691	$ 828	$ 814	11.3%
CD/Wafer Inspection	$ 221	$ 257	$ 328	$ 426	$ 522	$ 587	21.6%
Other Process Control	$ 469	$ 459	$ 540	$ 685	$ 847	$ 868	13.1%
Factory Automation	$ 153	$ 158	$ 206	$ 268	$ 360	$ 492	26.3%
Other Equipment	$ 202	$ 202	$ 251	$ 325	$ 397	$ 430	16.3%
Total World Fab Equipment Market	$5,779	$5,785	$7,170	$9,299	$11,330	$12,280	16.3%
Percentage Growth	18.4%	0.1%	24.0%	29.7%	21.8%	8.4%	

Source: Dataquest
December 1989

Lithography

The category of lithography equipment includes contact/proximity aligners, projection aligners, steppers, e-beam maskmaking and direct-write systems, laser scanning maskmaking systems, and X-ray aligners. The market for lithography equipment in 1990 is expected to be $1,483 million, up 5.3 percent from its 1989 level.

G-line steppers have been the predominant lithography tool for advanced device processing in the 1980s. Stepper manufacturers have continued to keep pace in providing improvements in stepper alignment systems, as well as developing lenses with higher numerical apertures and smaller resolutions. Recently, new wide-field g-line lenses have been introduced to accommodate more devices in the image field. These new lenses will have a significant impact on system throughput.

As semiconductor manufacturers look ahead to the ever-smaller submicron geometry requirements, several strategies for lithographic processing have been developed. Many manufacturers felt that they would be able to push g-line steppers to their limit, make a transition to excimer laser steppers for processing in the 0.5-micron to 0.35-micron range, and then make the next processing transition to X-ray lithography. The prevailing wisdom has been that i-line steppers would only represent an interim technology.

Recently, however, there has been a significant spurt of interest in i-line technology, and g-line steppers may fade faster than was originally expected. Another surprise is that there may be a resurgence in mix-and-match lithography in which 5X steppers are used to image the critical mask levels while projection aligners or 1X steppers are used for the noncritical processing steps. With the ever-escalating prices of advanced 5X steppers, and the fact that even on 16Mb DRAMs there are a large number of noncritical mask layers, mix-and-match makes economic sense.

With the fervor of activity that is now surrounding i-line technology, it still remains to be seen what the dominant lithography scheme will be below 0.5 micron. If i-line continues to advance, will it push excimer laser stepper technology further out in a similar fashion to what has happened to X-ray technology?

X-ray development continues to proceed. There are several compact synchrotron orbital radiation (SOR) systems that will soon see first light with an X-ray beam. In the area of e-beam lithography, new systems for both maskmaking and direct write are being introduced, and in maskmaking, the new laser scanning systems are making their

appearance at maskmaking houses. However, we still expect that e-beam technology will remain a niche market and will only account for about 10 percent or so of lithography sales.

Automatic Photoresist Processing Equipment

The market for track equipment in 1990 is expected to be $289 million, up 2.5 percent from its 1989 level. The driving force in track equipment continues to be unchanged: reduce contamination and improve process results. As a consequence, the market has seen the introduction of new track equipment in which the traditional belts used to transport the wafers have been replaced by small robots and wafer handlers that move the wafers to the process modules. These new systems are expensive, and because wafer throughput is not necessarily improved, equipment productivity is likely to fall. This phenomenon is not unique to track equipment, but is occurring throughout the fab.

Etch and Clean

The etch and clean market includes dry etch, dry strip, ion milling, and wet processing equipment. As shown in Table 2, the near-term outlook for dry etch equipment is a market of $640 million in 1990, down 1.5 percent from its 1989 level. The forecast for dry strip and ion milling equipment in 1990, at $110 million and $10 million, respectively, shows essentially no growth over 1989 levels. Wet processing equipment is expected to be $278 million in 1990, down 3.8 percent from its 1989 level.

We believe that the dry etch equipment market will grow in synergy with the CVD and PVD equipment markets over the next five years, due to the increasing demand for high-quality, production-worthy, multilayer thin-film deposition and etch processes. The move to 200mm wafers and precisely controlled submicron processing will lead to growing market share for single-wafer reactive ion etch (RIE) systems at the expense of single-wafer plasma etch systems and batch RIE systems. Concerns regarding device damage due to ion bombardment and plasma radiation will be solved by adopting low damage, magnetically enhanced reactive ion etchers (MERIEs) or electron cyclotron resonance (ECR) etchers.

Single-wafer, downstream strippers will be used to improve 200mm wafer process capability while minimizing device degradation due to plasma exposure. Both RF and microwave upstream plasma sources will be used. Ozone-based dry chemical stripping will also be used to avoid the effects of plasma radiation damage. Highly automated barrel strippers with elaborate particle-control measures will continue to be used for non-critical masking layers. As processes become more reproducible, dry strip modules will be integrated with dry etch modules into flexible cluster tools for in-situ processing.

The category of wet processing equipment includes integrated and manual wet benches, rinser/dryers, spray processors, and megasonic cleaners. Automation and chemical reprocessing continue to be important trends in the wet processing area. The emphasis is on reduction of contaminant, lower chemical consumption, and the environmental/safety impact of new system designs. There is also an emerging market for vapor phase systems used in the dry cleaning of wafers. This market will grow at the expense of conventional wet processing equipment, in our opinion.

Deposition

The deposition segment comprises the three technologies of chemical vapor deposition (CVD), physical vapor deposition (PVD), and epitaxy.

The CVD equipment market is forecast to be $530 million in 1990, down 1.9 percent from its 1989 level. However, we believe that the CVD equipment market will enjoy substantial growth over the next five years as submicron devices become more interconnect intensive. Tube CVD will give way to new generations of dedicated CVD reactors for applications such as interlayer dielectrics, silicides, tungsten plugs, and interconnects. ECR CVD processes will find applications in low temperature deposition. CVD technology will drive the emergence of flexible cluster tools that integrate various processes such as dry clean, CVD, PVD, dry etch, dry strip, RTP, and epitaxy. Cluster tool standards such as the SEMI/MESA specifications will benefit equipment companies and device manufacturers equally by offering flexibility, low cost, and retrofit capability to new process modules.

The PVD market, which includes sputtering and evaporation equipment, is forecast to be $390 million in 1990, down 2.5 percent from its 1989 level. The PVD market should enjoy healthy growth over the next five years as 4Mb and

16Mb DRAMs migrate toward double-level metallization, while ASICs and VLSI microprocessor/logic devices move toward three and even four levels of metallization. The cost of the interconnect process will continue to be an increasing proportion of total fabrication cost. Sputtered aluminum will be supplemented with barrier metals such as titanium nitride or titanium-tungsten alloys in order to improve chip reliability. Blanket tungsten and selective tungsten CVD films will be used to planarize submicron contacts and vias. Blanket tungsten CVD films will supplement sputtered aluminum for reliable submicron interconnect applications. Multilayer interconnect films will be deposited in integrated process equipment using a combination of PVD and CVD modules attached to flexible cluster platforms.

The category of epitaxy equipment includes silicon epitaxial reactors, molecular beam epitaxy systems, and metalorganic CVD equipment. The combined market for these three categories of equipment in 1990 is expected to be $225 million, up 6.1 percent from its 1989 level.

The silicon epi reactor market in 1988 was $85 million, reflecting significant growth over the 1987 market of $36 million. The strong performance for this equipment segment was attributable to the scramble to install epi capacity after several years of reduced equipment shipments. An important factor in the 1988 market growth in epi equipment was the increased demand for CMOS epi wafers for latch-up prevention in high-performance microprocessor, ASIC, and logic device applications. However, as the additional epi capacity came on-line, the demand for equipment dropped off significantly in 1989, and is expected to be down slightly in 1990 as well.

The long-term prospects for silicon epi are brighter than the current sluggish market environment would indicate. The demand for epitaxial wafers is expected to surge as more semiconductor manufacturers design epi into their CMOS and BiCMOS processes. In addition, new generations of epi reactor technology are being developed for single-wafer processing. Even the Japanese semiconductor manufacturers, which so far have avoided the high cost of epi wafers for DRAMs, are expected to consider epi processing to solve the latch-up problems for the 16Mb DRAM generation.

Diffusion

The diffusion equipment market is expected to be $300 million in 1990, down 9.1 percent from its 1989 market level. Even though tube unit shipments are forecast to decline in the future, the average selling price of these systems will climb steeply in response to increased automation, process control, and defect reduction measures. By 1994, the majority of tube shipments are expected to be vertical tube reactors, which have the advantages of smaller footprint, easier automation, and better uniformity.

Rapid Thermal Processing (RTP)

The RTP equipment market is expected to be $26 million in 1990, essentially flat with its 1989 market level. RTP technology is on the verge of being implemented in production for a variety of process applications. Dataquest expects RTP equipment to be incorporated as a process module in flexible cluster tools for applications such as silicides, thin oxides, BPSG reflow, and annealing. RTP will complement the diffusion tube market rather than replace it. Dataquest believes that the RTP market will experience healthy growth over the next five years as device manufacturers gain more experience with RTP modules in integrated process applications.

Ion Implantation

Ion implantation equipment includes medium-current, high-current, and high-voltage machines. The market for ion implantation equipment in 1990 is expected to be $427 million, down 10.5 percent from its 1989 level.

In the medium-current implanter market, several companies recently introduced parallel beam systems that have the capability for programmable tilt angle. This provides excellent flexibility in controlling channeling and shadowing effects. The parallel-beam design of these systems is particularly important when processing large wafers or device structures with large aspect ratios because it can provide excellent dose uniformity across the entire wafer surface. In the area of high-current implanters, applications include heavy source-drain implants, as well as the ability to tailor poly gates separately with n+ and p+ dopants.

One important issue for semiconductor manufacturers regarding medium- and high-current implanters is the balance between equipment productivity and capital investment. High-current systems have higher productivity levels than medium-current implanters. At the same time,

however, they also are more expensive. Therefore, to achieve a balance between productivity and capital investment, a fab typically will contain a mix of both medium- and high-current systems.

Japanese manufacturers continue to be the leading buyers of high-voltage implanters. These tools are being used for the formation of retrograde wells, a process alternative to epitaxy for the prevention of latch-up in advanced CMOS devices such as 16/64Mb DRAMs and 1/4Mb SRAMs.

While new technology developments are often the focus of discussion in the semiconductor equipment industry, many believe that the critical issues facing implanters in the future will be more nontechnical in nature, i.e., system reliability, tool automation, and particulate control.

Process Control

Process control is a broad category that includes equipment for mask and wafer inspection, as well as for metrology, process monitoring, surface analysis, and analytical quality control. The market for this equipment is highly specialized with dozen of companies, mostly small, selling into many noncompetitive market niches. The market for process control equipment (including CD/wafer inspection equipment) in 1990 is expected to be $716 million, up 3.8 percent from its 1989 level.

Although the worldwide critical dimension and wafer inspection equipment markets have been experiencing healthy growth the last several years, not all companies have participated in the market expansion to the same extent. The success of a company in optical CD and wafer inspection is more and more dependent on its ability to provide advanced technology for submicron measurement and automatic defect detection. This in turn is tied directly to the company's ability to generate a sufficient income stream from its existing products to fund next-generation technology development, which does not come cheap. At the same time, the number of companies capable of maintaining the flow of R&D dollars continues to shrink.

Although several companies recently have entered the market, several recent acquisitions also are very significant as these signal the beginning of consolidation within this part of the industry. For many companies, consolidation may be the only path available to reach the critical mass required to fund technology development and support an increasingly demanding client base in the future.

Factory Automation/Other Equipment

This category segment includes factory automation equipment and a catch-all category that encompasses all of the various pieces of equipment used in a fab that do not fall into any of the major fab equipment areas described above. These include such items as tube cleaners, storage systems, and gas analyzers. Expenditures for factory automation are still quite small relative to the amount of money that is spent on equipping a fab. For instance, factory automation expenditures in 1990 will represent only about 3 percent of the total wafer fab equipment market. Collective expenditures for the equipment in the catch-all category grow with front-end equipment spending.

DATAQUEST CONCLUSIONS

Sales of wafer fab equipment grew very rapidly in the three-year period of 1987 through 1989, and the wafer fab equipment industry more than doubled over this time period. A significant amount of wafer production capacity was added during this period, and the industry is now absorbing this capacity as new fabs are brought on-line. We expect 1990 will be a flat year as the industry predictably pauses to catch its breath before the next round of new semiconductor devices, new fabs, and added capacity begins anew.

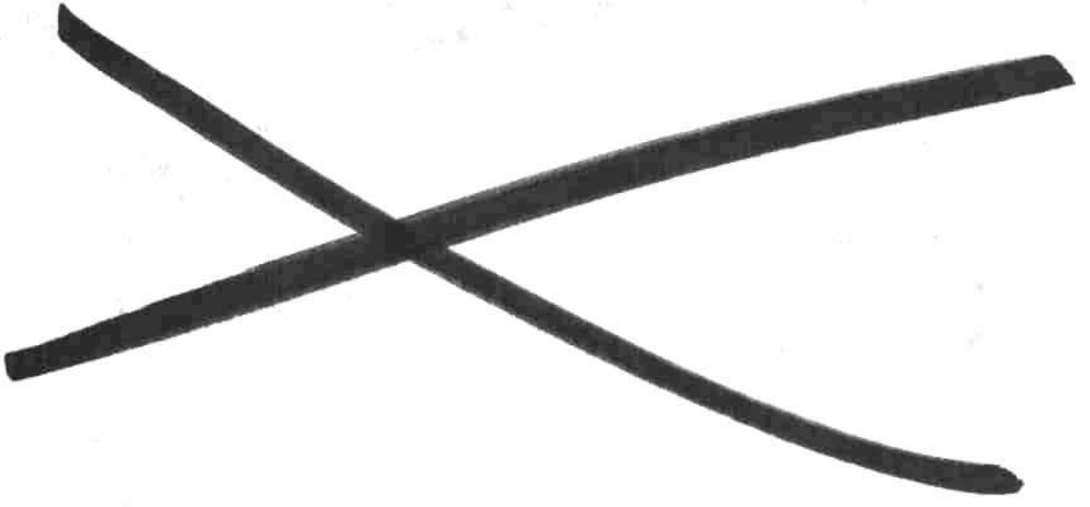
This time the pause will not be as severe as in the past. We are predicting a flat 1990, but very healthy growth starting again in 1991 and continuing until 1994, when we expect another pause in wafer fab equipment spending. One reason the pause in equipment spending will be brief and shallow in 1990 is that the electronic equipment industry, which is at the top of the electronic industry food chain and ultimately provides the demand for all semiconductor equipment and materials, is expected to continue to grow as the world demands advanced electronics of all types.

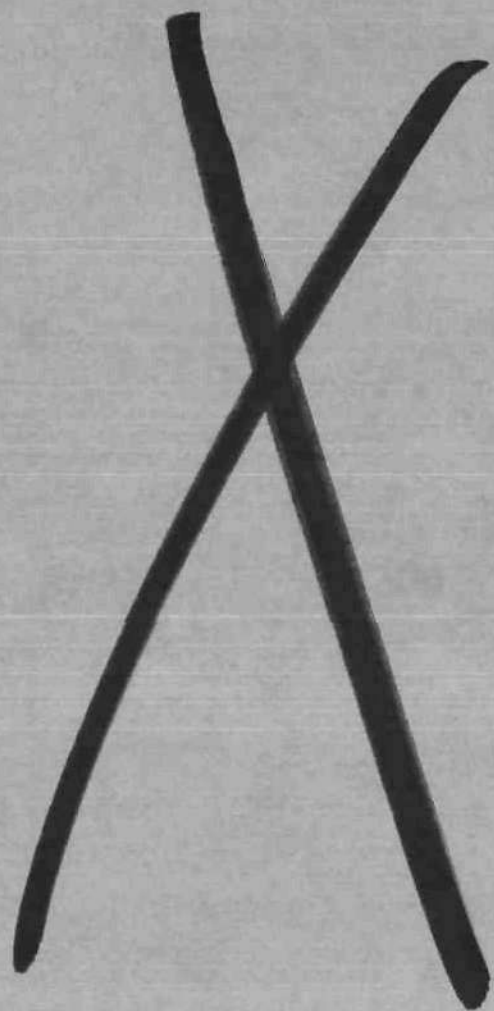
Another reason for the soft landing in 1990 is that the demand for semiconductors is broad-based; the industry is not strongly tied to a single product that can bring the semiconductor industry to its knees, as in the past. A third reason is that the electronic equipment companies have very tightly managed their semiconductor inventories so that changes in their electronic system sales ripple immediately through to the semiconductor manufacturers. All in all, the electronics industry is in fairly good shape; it seems to have learned from its past inventory excesses.

In addition, the view of 1990 by all participants in the electronic industry food chain—the electronic equipment companies, the semiconductor manufacturers, and the equipment and materials companies—is remarkably uniform. This is encouraging, because it indicates that everybody is reading the signs in the same way.

On the negative side, the coming no-growth year will be one in which budgets will be watched closely and attention will be turned toward increasing operational efficiency. It is a time when industry consolidation generally accelerates. However, it is also a time when increasing attention toward customers pays dividends during the next upturn, which we expect to be in a year's time.

Mark FitzGerald
Joseph Grenier
Krishna Shankar
Peggy Marie Wood





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Research Newsletter

SEMS Code: Newsletters 1989
Equipment Data Base
0004354

CLOSING THE GAP: WILL JAPAN BECOME THE WORLD'S LARGEST PRODUCER OF FAB EQUIPMENT?

INTRODUCTION

Dataquest's Semiconductor Equipment and Materials Service (SEMS) has completed its 1988 worldwide wafer fabrication equipment data base. This newsletter is the second in a series of newsletters that will discuss various aspects of the 1988 data base. We will discuss the worldwide wafer fab equipment market and how it is supplied by European, Japanese, and U.S. equipment vendors. The intent is to provide a high-level view of this subject.

The information in this newsletter is drawn from Table 1 of the "Wafer Fab Equipment—Import/Export Data" section behind the Equipment Data Base tab in the SEMS Equipment and Materials notebook. Please refer to that table for more details on the subject discussed in this newsletter.

WORLDWIDE WAFER FAB EQUIPMENT MARKET

Table 1 presents the front-end or wafer fab equipment market for the years 1984 through 1988. The first line in the table gives the total worldwide market for all wafer fab equipment. The subtotal fab equipment market, given on the second line, includes all lithography, etch and clean, deposition, diffusion, ion implantation, and CD/wafer inspection equipment. For these equipment categories, detailed company-by-company sales are determined, and it is this detailed company analysis that forms the basis for the information presented in this newsletter. Not included in the subtotal are other process control equipment, factory automation, and other miscellaneous equipment used in the front end. For these categories, Dataquest estimates the size of the market but does not perform a detailed company-by-company survey.

Table 1

Worldwide Wafer Fab Equipment Market
(Millions of Dollars)

	1984	1985	1986	1987	1988
Total Wafer Fab Equipment Market	$3,520	$3,356	$2,713	$3,148	$4,894
Subtotal Fab Equipment Market	$2,812	$2,740	$2,228	$2,600	$4,162
Subtotal Percent	80%	82%	82%	83%	85%

Source: Dataquest
July 1989

In 1988, detailed company data, represented by the subtotal fab equipment market, accounted for $4,162 million of the total $4,894 million fab equipment market. This represents 85 percent of the total market and includes virtually all of the major equipment used in IC manufacture. Henceforth in this newsletter, the terminology "wafer fab equipment market" refers to the detailed company data. The reason that this discussion is included here is to maintain data integrity across the equipment data base and all of the publications based on the data base.

WORLDWIDE FAB EQUIPMENT MARKET BY REGIONAL OWNERSHIP OF EQUIPMENT COMPANY

Table 2 shows the worldwide wafer fab equipment market broken down by regional ownership of equipment companies for the years 1984 through 1988. In 1984, combined sales by European and Japanese equipment companies were $1,129 million, while U.S. equipment company sales were 49 percent more at $1,683 million. By 1988, combined European and Japanese company sales were $2,238 million, but U.S. company sales grew to only $1,924 million, 14 percent less than combined European and Japanese company sales. From 1984 to 1988, European and Japanese company sales doubled, while sales by U.S. companies increased by only 14 percent. Or, looking at sales growth in another way, U.S. company sales had a compound annual growth rate (CAGR) of only 3.4 percent during the 1984 to 1988 period, while European and Japanese companies each had CAGRs in excess of 18 percent.

Figure 1 graphically shows the shift in market share among the three international suppliers. In 1984, U.S. equipment companies had 60 percent of the world equipment market, but by 1988, their share had slipped to 46 percent. Meanwhile, Japanese company share, which was 33 percent in 1984, grew to 44 percent in 1988. U.S. equipment companies, which in early years pioneered the wafer fab equipment industry and then rose to dominate the world market, are now essentially at parity with their Japanese counterparts.

Table 2

Worldwide Wafer Fab Equipment Market
by Regional Ownership of Equipment Company
(Millions of Dollars)

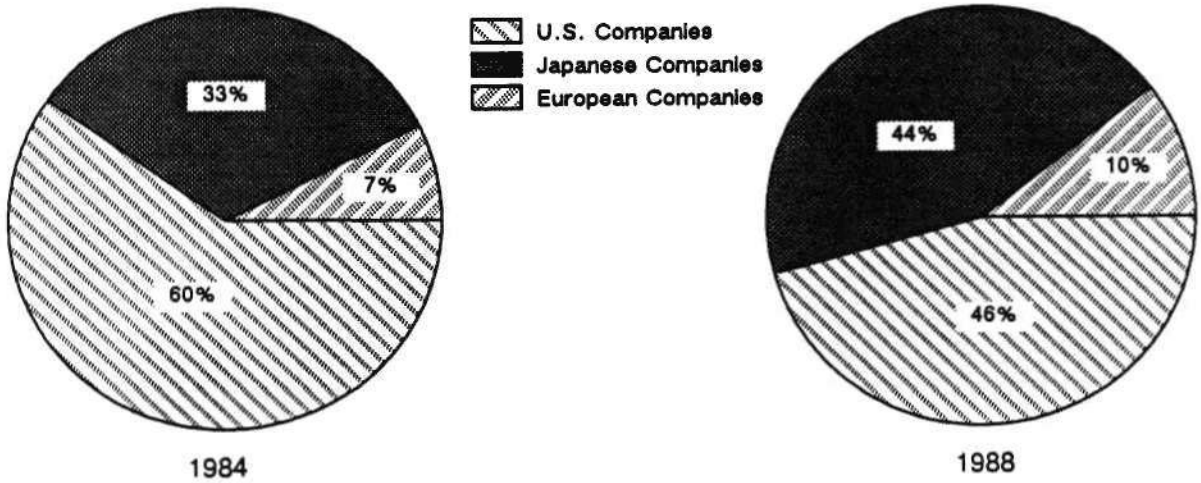
	1984	1985	1986	1987	1988	Percent Share 1988	CAGR 1984-1988
European Companies	$ 204	$ 240	$ 260	$ 315	$ 401	9.6%	18.4%
Japanese Companies	925	967	814	1,076	1,837	44.1	18.7%
U.S. Companies	1,683	1,533	1,154	1,209	1,924	46.2	3.4%
Total	$2,812	$2,740	$2,228	$2,600	$4,162	100.0%	10.3%

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
July 1989

Figure 1

Worldwide Wafer Fab Equipment Market
Shares by Regional Ownership of Equipment Company



0004354-1

Source: Dataquest
July 1989

REGIONAL FAB EQUIPMENT MARKET BY REGIONAL OWNERSHIP OF EQUIPMENT COMPANY

Table 3 lists the percentage of market share for European, Japanese, and U.S. fab equipment companies by region for 1984 and 1988. Note that in 1988 U.S. equipment companies had a 76 percent share of the U.S. market, and Japanese companies had a 78 percent share of the Japanese market. Thus, Japanese and U.S. companies each have comparable shares of their home markets. In the European and Rest of World (ROW) markets, U.S companies have the dominant market share. Table 3 also compares 1984 and 1988 market shares for the three international suppliers for the regions.

Table 3

Regional Wafer Fab Equipment Markets by Regional Ownership of Equipment Company (Percent Share)

	1984	1988	Change 1984-1988
United States			
European Companies	7%	11%	4%
Japanese Companies	6	13	7%
U.S. Companies	87	76	(11%)
	100%	100%	
Japan			
European Companies	2%	3%	1%
Japanese Companies	68	78	10%
U.S. Companies	30	20	(10%)
	100%	100%	
Europe			
European Companies	26%	32%	6%
Japanese Companies	6	13	7%
U.S. Companies	68	55	(13%)
	100%	100%	
Rest of World (ROW)			
European Companies	11%	7%	(4%)
Japanese Companies	20	35	15%
U.S. Companies	69	58	(9%)
	100%	100%	
Worldwide			
European Companies	7%	10%	3%
Japanese Companies	33	44	11%
U.S. Companies	60	46	(14%)
	100%	100%	

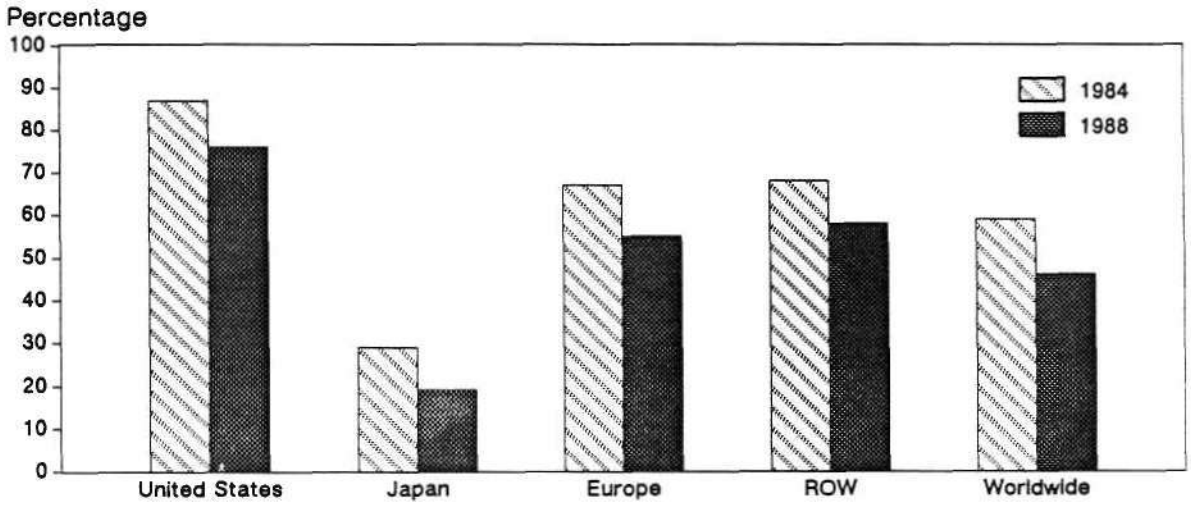
Note: Columns may not add to totals shown because of rounding.

Source: Dataquest July 1989

Figure 2 looks at the same data in another way and compares the 1984 and 1988 market shares for U.S. equipment companies in each of the regions and worldwide. Note that both in every region and worldwide, U.S. companies have lost market share since 1984. For instance, U.S. companies had 30 percent share of the Japanese equipment market in 1984, but by 1988, their share had fallen to 20 percent. Even in the European and ROW markets, where U.S. companies still dominate, they are losing share to European and Japanese companies. Likewise, Figures 3 and 4 show the market share trend for Japanese and European companies. Japanese companies have gained market share in every region and worldwide since 1984; European companies have gained share in every region except ROW, but they still have managed to gain share worldwide.

Figure 2

U.S. Equipment Company Sales
Percent Share of Regional Market



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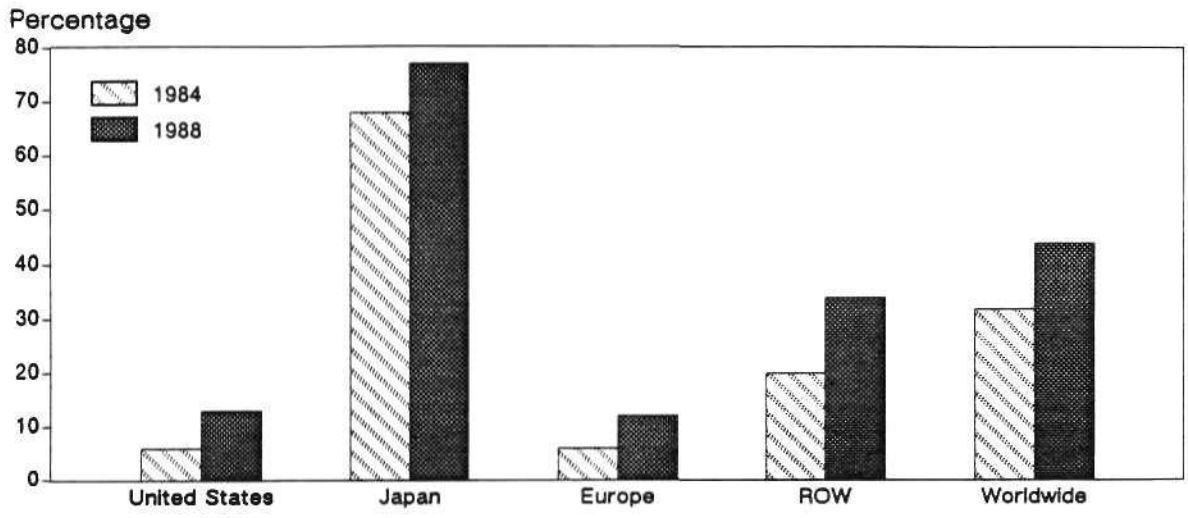
Source: Dataquest July 1989

Figure 3

Japanese Equipment Company Sales
Percent Share of Regional Market



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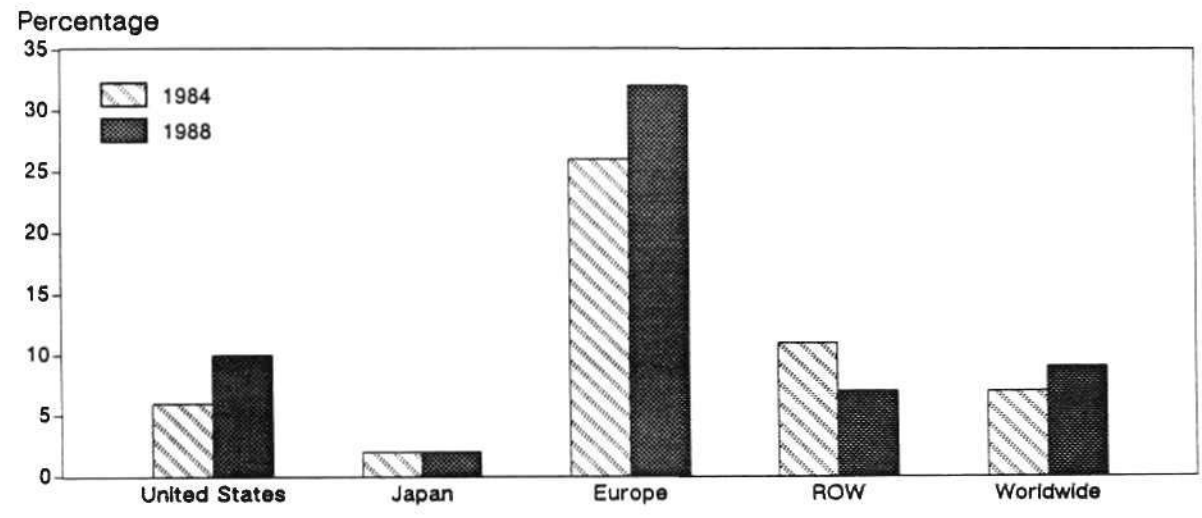
Source: Dataquest
July 1989

Figure 4

European Equipment Company Sales
Percent Share of Regional Market



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Source: Dataquest
July 1989

SUMMARY

The message of this newsletter is that U.S. equipment companies, which once dominated the fab equipment industry, no longer do so. On the other hand, the Japanese equipment industry has grown very rapidly to become essentially at parity with the U.S. companies in 1988. Also, the shift in relative market share between the U.S. companies and the Japanese companies has been rapid: U.S. company share has slipped 14 percentage points since 1984, while the Japanese companies have gained 11 points.

In addition, U.S. companies are losing their international competitiveness as they have lost market share in all regions, while their Japanese counterparts have gained market share in all regions. Japanese companies have made particularly rapid gains in ROW, a region where the U.S. companies historically have been strong.

Japan has become the world's largest producer of semiconductors, and this has provided the impetus to build a strong Japanese equipment industry to support that production. As the Japanese equipment industry matures, it will seek overseas markets, particularly as Japanese semiconductor producers establish overseas facilities. Thus, U.S. and European equipment companies face increasing competition not only in Japan, the world's largest equipment market, but also in their respective home markets as the Japanese semiconductor producers expand worldwide production.

Noteworthy also are the gains being made by the European equipment companies. Although they accounted for only 10 percent of the total market in 1988, this is up from 7 percent in 1984. This gain is largely because of the European companies' increased penetration into their home market and in the United States as well.

Japan is the world's largest producer of semiconductors. Japan is the world's largest market for semiconductor equipment. Will Japan also become the world's largest producer of wafer fab equipment?

Joe Grenier

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Research Newsletter

SEMS Code: Newsletters 1989
Equipment Data Base
0004285

1988 WAFER FAB EQUIPMENT REGIONAL MARKET SHARES

INTRODUCTION

The Semiconductor Equipment and Materials Service (SEMS) has completed its 1988 worldwide wafer fabrication equipment data base. This newsletter is the first in a series of newsletters that will discuss various aspects of the 1988 data base. Here we will discuss the overall wafer fab equipment market by region and by equipment category. The intent is to provide a high-level view of the world fab equipment market; it is not intended to include detailed information on the market, although such information is available in the data base.

The information discussed herein is drawn from Table 1 of the "Wafer Fab Equipment—Summary Data by Category" section behind the "Equipment Data Base" tab in the SEMS Equipment and Materials notebook. Please refer to that table for more details on the subject discussed in this newsletter.

Table 1

Wafer Fab Equipment Market by Region (Millions of Dollars)

	1984	1985	1986	1987	1988	Share 1988	CAGR 1984-1988
United States	$1,461	$1,258	$1,077	$1,105	$1,570	32%	1.8%
Japan	1,526	1,423	1,021	1,288	2,210	45	9.7%
Europe	398	467	453	524	669	14	13.9%
Rest of World	135	209	162	230	446	9	34.7%
Total	$3,520	$3,357	$2,713	$3,147	$4,895	100%	8.6%
Year-to-Year Growth	65.5%	(4.6%)	(19.2%)	16.0%	55.5%		

Source: Dataquest
June 1989

WAFER FAB EQUIPMENT MARKET BY REGION

Table 1 shows that the worldwide front-end, or wafer fab, equipment market in 1988 reached an all-time high of $4,895 million. The 1988 market should be compared with the previous high of $3,520 million, which occurred in the record-breaking year of 1984. Market growth from 1987 to 1988 was a hefty 55.5 percent, nearly matching the 65.5 percent growth achieved in 1984.

Clearly, the U.S. market is stagnating while the Japanese market has grown impressively. Japan now is the largest wafer fab equipment market in the world. Table 1 shows that in the United States, the 1988 wafer fab equipment market of $1,570 million was only 7 percent larger than the 1984 market of $1,461 million; in Japan, the 1988 market of $2,210 million was 45 percent larger than the $1,526 million recorded in 1984.

The high growth rate of the rest of world (ROW) equipment market also is impressive, growing from $135 million in 1984 to $446 million in 1988. It is interesting to note that the ROW market is about one-third the size, and the European market is about one-half the size of the U.S. equipment market.

To summarize Table 1, the United States accounted for only 32 percent of the worldwide wafer fab equipment market, while the Japanese market reached 45 percent and the European and ROW markets combined accounted for 23 percent. From another point of view, the Far East (Japan and ROW) accounted for 54 percent of the worldwide wafer fab equipment market. Wafer fabrication equipment is the bottom tier, or foundation, of the electronics industry food chain. The shift of the fab equipment market to the Far East is just another of the many indications of the increasing amount of electronic production activity occurring there.

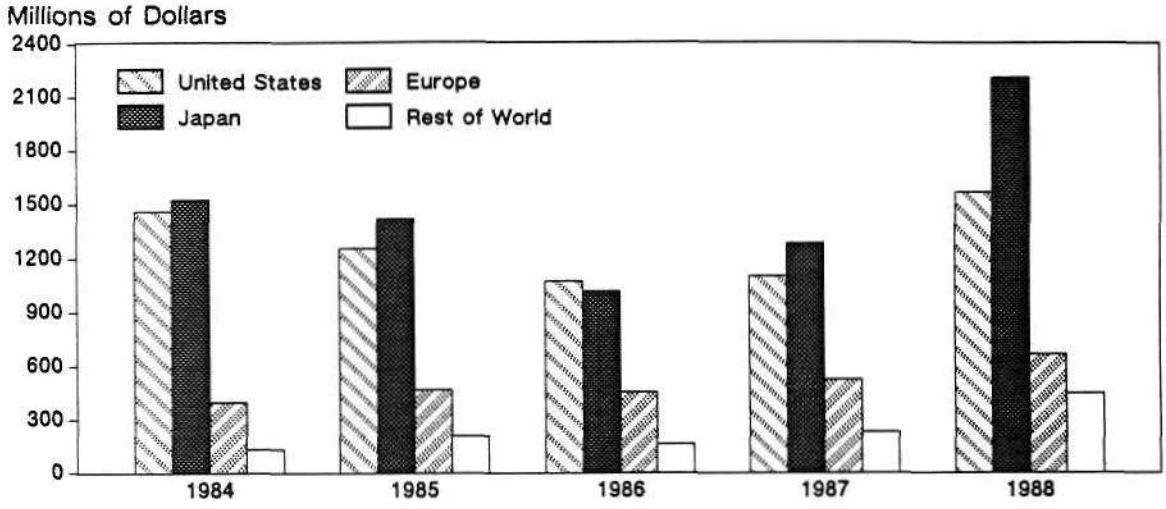
Figure 1 graphically shows the regional data described in Table 1. Every year from 1984 through 1988, with the exception of 1986, when the U.S. and Japanese equipment markets were about the same, the Japanese market exceeded the U.S. market. In 1988, the Japanese market was 41 percent larger than the U.S. market.

Figure 2 shows the regional shift in the wafer fab equipment markets from 1982 through 1988. In 1982, Japan, Europe, and ROW accounted for 54 percent of the world market, while in 1988, these regions accounted for 68 percent. Capital spending in the ROW countries is expected to be very robust and even to exceed that in Europe during the next few years, so we should see this part of the "pie" increase even more.

Table 2 indicates that regional wafer fab equipment market growth was uneven from 1987 to 1988; the highest growth, approximately 94 percent, occurred in the ROW region, particularly Korea and Taiwan. Japan also experienced a very high growth rate of nearly 72 percent, as Japanese semiconductor manufacturers ramped up their DRAM capacity. Europe had the lowest growth rate, about 28 percent, which is still very healthy. How many other industries would be happy with this sort of growth?

Figure 1

Wafer Fab Equipment by Region



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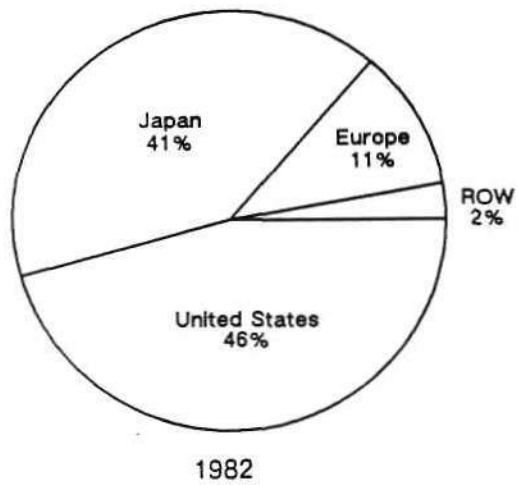
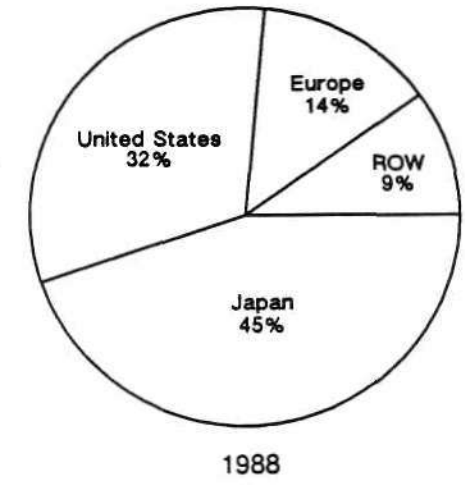
Source: Dataquest June 1989

Figure 2

Wafer Fab Equipment Market 1982 versus 1988





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Source: Dataquest June 1989

Table 2

Wafer Fab Equipment Market
Regional Growth and Regional Shares
(Millions of Dollars)

	1988	Growth 1987-1988
United States	$1,570	42.1%
Japan	2,210	71.6%
Europe	669	27.7%
Rest of World	446	93.9%
Total	$4,895	55.5%

Source: Dataquest
June 1989

WAFER FAB EQUIPMENT MARKET BY CATEGORY

Table 3 shows the 1988 worldwide sales and growth rate from 1987 to 1988 for each of the wafer fab equipment categories that compose the front-end equipment market. Many of these categories had a worldwide growth rate in excess of 50 percent; the regional data for these categories are given in Table 4. In this table, except for silicon epitaxy and optical/CD wafer inspection equipment, the largest markets were in Japan. For the remaining categories in Table 4, the Japanese market for several equipment categories exceeded the U.S. market by 50 percent or more, including steppers (52 percent), automatic photoresist processing equipment (54 percent), dry strip (176 percent), and diffusion (49 percent). Particularly noteworthy was the Japanese implant market, which exceeded the U.S. market by 207 percent. For the ROW region, note that the $113 million spent on steppers exceeded the $85 million spent on steppers in Europe.

As mentioned previously, the world fab equipment market grew by 55.5 percent from 1987 to 1988, but growth rates across the regions were uneven, with the highest growth occurring in the Japan and ROW regions. For several equipment categories listed in Table 4, the regional differences are emphasized even more. Figures 3 and 4 show the 1987 to 1988 growth rates for the nine equipment categories listed in Table 4. Japan and ROW clearly have growth rates for steppers, automatic photoresist processing equipment, dry etch, chemical vapor deposition, and implant equipment that far exceed the other regions (see Figure 3). The equipment categories in Figure 4 show that Japan and ROW, although having high growth rates, do not stand out as clearly as they do in the equipment categories shown in Figure 3.

Table 3

1988 Worldwide Wafer Fab Equipment Market by Category (Millions of Dollars)

	1988	Growth 1987-1988
Lithography	$1,219	54.3%
Automatic Photoresist Processing Equipment	250	52.2%
Wet Process	235	42.5%
Dry Strip	90	73.1%
Dry Etch	547	77.9%
Chemical Vapor Deposition	455	78.9%
Physical Vapor Deposition	315	26.4%
Silicon Epitaxy	85	138.0%
Metalorganic CVD	43	19.4%
Molecular Beam Epitaxy	85	19.8%
Diffusion	266	53.5%
Rapid Thermal Processing	22	18.9%
Ion Implantation	379	103.8%
Optical CD/Wafer Inspection	173	75.9%
Other Process Control	427	28.6%
Factory Automation	130	31.3%
Other Equipment	174	50.5%
Total	$4,895	55.5%

Table 4

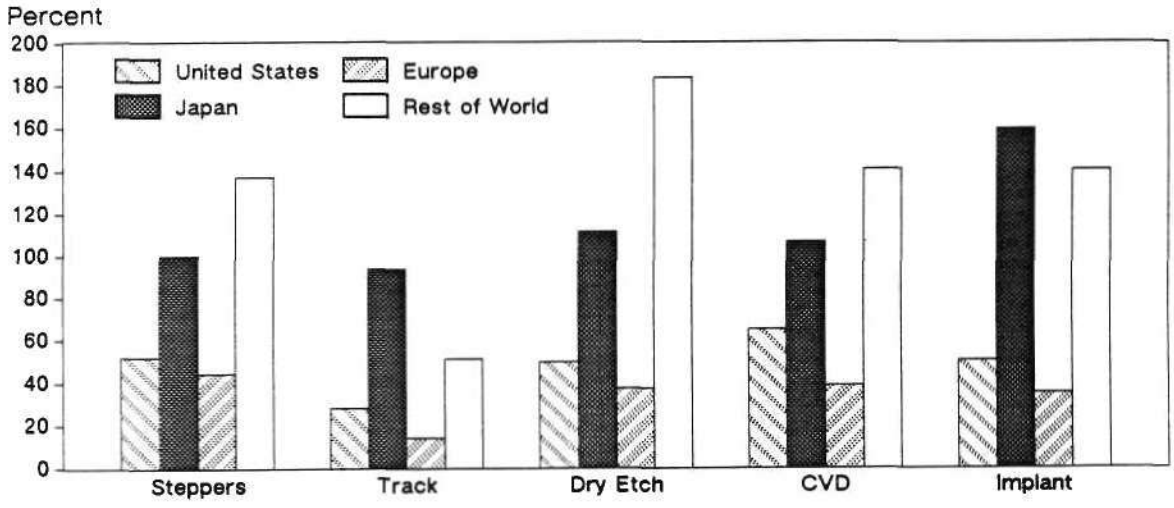
1988 Wafer Fab Equipment Market High-Growth Equipment Categories by Region (Millions of Dollars)

	United States	Japan	Europe	ROW	Total
Steppers	$280	$425	$85	$113	$903
Automatic Photoresist Processing Equipment	$ 78	$120	$32	$ 20	$250
Dry Strip	$ 21	$ 58	$ 4	$ 7	$ 90
Dry Etch	$177	$239	$80	$ 51	$547
Chemical Vapor Deposition	$152	$189	$77	$ 37	$455
Silicon Epitaxy	$ 42	$ 24	$15	$ 4	$ 85
Diffusion	$ 81	$121	$49	$ 15	$266
Implant	$ 69	$212	$55	$ 43	$379
Optical/CD Wafer Inspection	$ 69	$ 61	$25	$ 18	$173

Source: Dataquest
June 1989

Figure 3

1988 Wafer Fab Equipment
High–Growth Equipment Categories
Percent Growth 1987–1988



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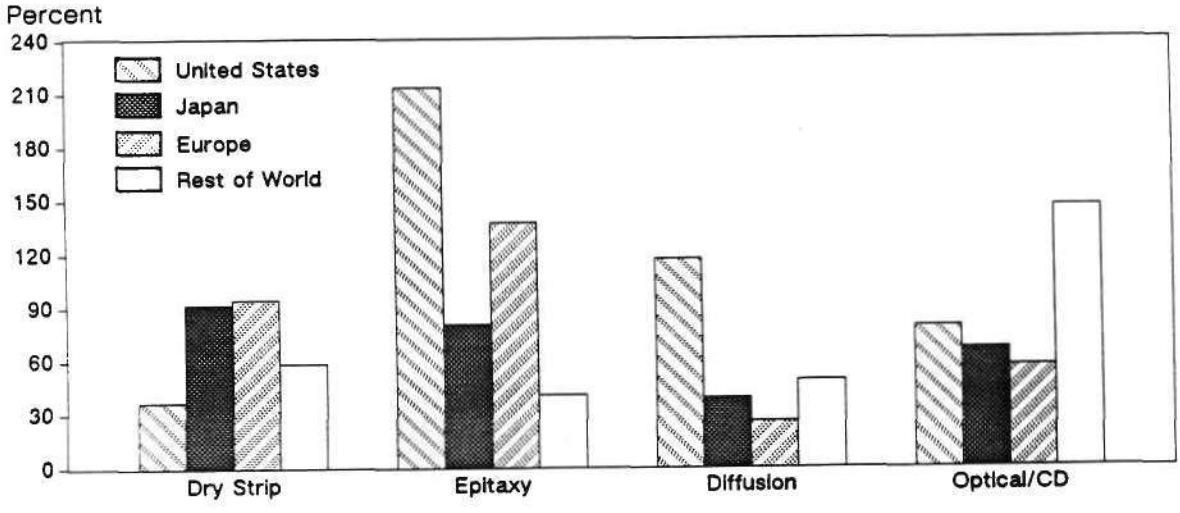
Source: Dataquest
June 1989

Figure 4

1988 Wafer Fab Equipment
High–Growth Equipment Categories
Percent Growth 1987–1988



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Source: Dataquest
June 1989

SUMMARY

This newsletter's message is that the largest wafer fab equipment market, by far, is in Japan; the United States is declining as a fab equipment market; and the ROW countries are becoming major equipment markets. In 1988, very high growth for the equipment market occurred in the Japan and ROW regions. The Japan, Europe, and ROW regions together accounted for 68 percent of the worldwide fab equipment market in 1988, with the United States accounting for only 32 percent.

Japanese equipment companies and large U.S. or European equipment companies with an international presence are in a favorable position. However, small U.S. companies with no overseas connections have less favorable prospects because they are participating in a piece of the market pie that is getting smaller each year. Basically, the fab equipment market action is shifting away from the United States to overseas markets.

Joe Grenier

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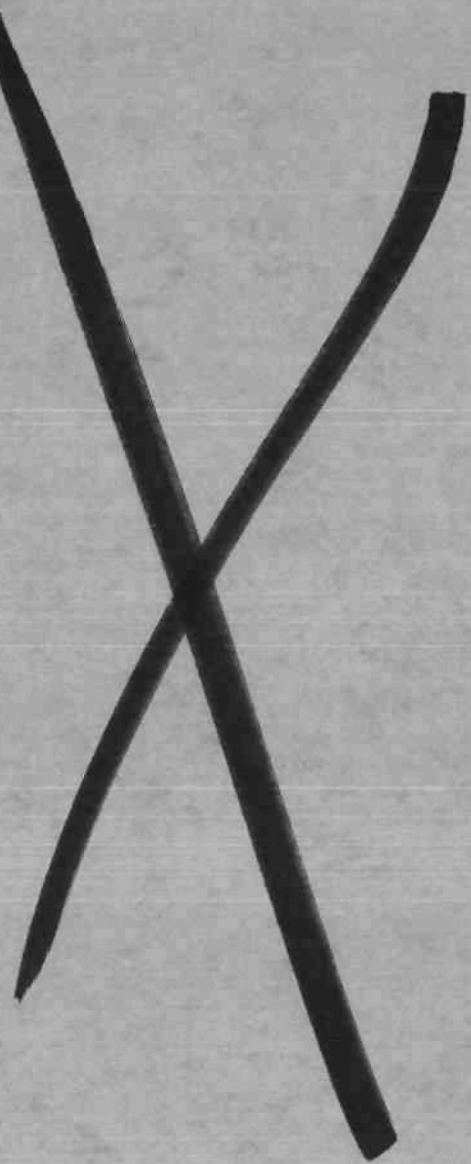

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Research Newsletter

SEMS Code: Newsletters 1989
Lithography
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THE SPIE 1989 SYMPOSIUM ON MICROLITHOGRAPHY

INTRODUCTION

SPIE (Society of Photo-Optical Instrumentation Engineers) held its 1989 Symposium on Microlithography from February 26 through March 3, 1989, in San Jose, California. This annual event is an important international conference on advances in lithography, including optical, excimer laser, e-beam, X-ray, and ion-beam technologies; in IC metrology, inspection, and process control; and in resist technology and processing.

This newsletter presents an overview of the most significant papers given at the conference; the intention is to provide the reader with a glimpse into the future of production lithography technologies. Perhaps the conference can best be summed up by the following observation: At the 1987 conference, the excimer laser people said that excimer laser steppers probably could push optical technology down to 0.5 micron. In 1988, they said that excimer steppers would be used at 0.5 micron, and probably could be pushed to 0.35 micron. This year, the g-line and i-line people said that these optical technologies probably will be used at the 0.5-micron level. The same scenario is revisited each year—the g-line and i-line people continue to advance their technologies beyond expectation. In the past, they have pushed out the market windows for e-beam and X-ray; now they may push out the window for excimer laser steppers also.

G-LINE AND I-LINE STEPPERS

Nikon discussed its new NSR-1505 G6E stepper that features field-by-field leveling, auto focus, new g-line and i-line lenses, and an alignment accuracy of 0.13 micron in the enhanced global alignment mode.

The g-line lens has a numerical aperture (NA) of 0.54, a resolution of 0.65 micron, and a field size of 15mm x 15mm. Total depth of focus is 1.2 microns with the depth of focus (DOF) decreasing as one moves to the corners of the field. Nikon said that this lens is capable of 0.5-micron lithography. The new i-line lens has a numerical aperture of 0.45, a 0.65-micron resolution, a 15mm x 15mm field size, and a greater total depth of focus of 1.8 microns. Bandwidth for the g-line lens is plus or minus 5nm, while for the i-line lens, it is plus or minus 3nm.

Nikon noted some trade-offs between g-line and i-line lenses. The advantages of g-line include the large amount of accumulated experience on g-line systems and higher throughput. (I-line systems have less illumination at the wafer because of absorption of the i-line wavelength in the lens glass.)

Canon discussed its two new g-line lenses. The first is a large field lens that has a 0.45 NA, a 20mm x 20mm field size, a resolution of 0.75 micron, a distortion of less than 0.1 micron, and a DOF of 2 microns. The second lens has a 0.55 NA, a resolution of 0.65 micron, and a DOF greater than 1 micron. Canon said that it would be possible to resolve 0.5-micron lines and spaces with this lens, and that a 0.55 NA lens with an image field larger than 17mm x 17mm could be developed.

GCA discussed its two new i-line lenses that are designed and built by Tropel. The 2040i lens has an NA of 0.40, a resolution of 0.73 micron, and a 20mm circular field size. The 2145i lens has an NA of 0.45, a resolution of 0.65 micron, and a 21mm circular field size. The 2040i was available in 1988, while the 2145i will be available later in 1989. The DOF on the 2040i is 1.5 microns for 10 percent CD control. The maximum distortion measured for four 2040i lenses was less than 0.06 micron. GCA said that these lenses could be matched routinely to within 100nm. No DOF specification has yet been set for the 2145i lens, nor has any distortion data been obtained.

GCA also discussed the i-line resists that are available on the market; its comment was that most of the resists are so new that full characterization is not yet available.

ASM Lithography discussed the progress that it is making in i-line stepper technology. ASM said that whereas today, for 0.7-micron resolution, single-machine and matched-machine overlay requirements are 150nm and 250nm, respectively, they would need to be decreased to 100nm and 160nm for 0.5-micron resolution. In order to meet these future goals, ASM has an overlay improvement program that focuses on improvements in the alignment system, the X-Y stage, and improvements in lens distortion.

ASM also discussed ways of increasing DOF by considering the stepper and i-line resist together as a lithography system, and then looking at opportunities for increasing DOF by examining such factors as postexposure bake, image reversal, top surface imaging, contrast enhancement, and high-contrast resists. In fact, it was a common theme among the talks at the conference to consider the entire lithography system (tool plus the photoresist) rather than the tool alone, as in the past.

ASM's conclusions were that i-line is capable of 0.5-micron resolution and will meet the overlay requirements of 0.5-micron lithography with the planned improvements.

EXCIMER LASER STEPPERS

Nikon discussed the changes that it has made in the design of the excimer laser stepper lens. In 1986, Nikon discussed an achromatic lens made from fused silica (SiO_2) and calcium fluoride (CaF_2). The lens had an NA of 0.37 and a field size of 5mm x 5mm. However, high-quality CaF_2 raw material is hard to obtain, and it is also difficult to fabricate a lens from this material. In addition, because of the large expansion differences between the silica and CaF_2, no material could be found to cement

the lens elements together. Thus, Nikon has switched to a single-material, fused-silica, chromatic 5X lens that has an NA of 0.42 and a 15mm x 15mm field size. Resolution is less than 0.5 micron.

The off-axis alignment system uses a helium-neon (He-Ne) laser to obtain an overlay accuracy of 0.18 micron (3 sigma) in the enhanced global alignment mode. Nikon said that the alignment accuracy is approaching g-line steppers, and estimated that with a 100mJ/cm^2 resist that throughput would be about one-quarter of that of a g-line stepper. Nikon mentioned that availability of excimer laser resists in Japan is limited, and was also careful to say that the excimer stepper was suitable for 0.5-micron lithography in the lab.

Ultratech discussed its broadband deep-UV lens that can use either an unnarrowed krypton fluoride (KrF) laser or a mercury arc source. The lens is the same in concept as the normal Ultratech 1:1 lens; this deep-UV lens differs only in material and construction. The larger elements are made from SiO_2, the prisms of CaF_2, and the other elements of lithium fluoride (LiF). The interfaces between the different elements are in oil, as it is not possible to cement the elements. The lens has an NA of 0.35, a field size of 3.0 cm^2, and a bandwidth of 6nm.

The mercury arc lamp is a 200-watt lamp pulsed to 500 watts. Exposure times are a bit longer than desired; with a 60mW/cm^2 illumination intensity at the wafer, and a 100mJ/cm^2 resist, an exposure time of 1670 msec is required.

EXCIMER LASER SOURCES

One of the key components in the successful development of excimer laser lithography is the laser source itself, and accordingly, three laser companies—Cymer Technologies, Lambda Physik, and Lumonics—presented papers on the KrF 248nm laser systems that they have developed for lithography applications.

General requirements for the laser source include:

- Narrow bandwidth, typically <= 3 picometers (3pm or 0.003nm) as measured at full width half maximum (FWHM)
- Wavelength stability of approximately +/- 0.5-1.0pm
- Average power of 2-10 watts
- Typical repetition rates of 200-500Hz

It is also essential that the excimer laser be stable and well-behaved with regard to transient operation. This means that when the stepper is not exposing the wafer, the line-narrowing optics, as well as other optical elements, must remain stable.

The range in available laser power was a topic addressed by all three papers. Lambda Physik emphasized the modifications it had made in its 248 L laser to increase the power from 2W to 5W operation. The company optimized the discharge unit by improving the laser pumping, modified the line-narrowing optics to improve optical efficiency, and enhanced the gas flow to increase the repetition rate from 200Hz to 400Hz. Even with these adjustments in operating parameters, the laser still exhibited stable beam quality. Cymers' system, the CX-2LS, already operates at 3W of power and a repetition rate of 200Hz. Lumonics' Index 300 KrF laser is rated at 2W power, and 200Hz repetition rate, although the company commented that it has achieved 6W operation at 300Hz, and that it may be possible to achieve power of 5W at 500Hz with the current system.

Because of the current, relatively low, photoresist sensitivity to the 248nm excimer laser wavelength, increasing the power of the laser translates to a higher wafer throughput. As photoresists are developed with higher sensitivity at the 248nm wavelength, there will be less need to optimize laser operation at higher power. Until that time, the laser companies are improving the operation of their components to balance the deficiencies in current photoresist.

STEP AND SCAN: PERKIN-ELMER'S MICRASCAN 1

Without doubt, the most significant event at this year's symposium was the unveiling of the long-awaited step-and-scan system from Perkin-Elmer. This system, which costs $4 million, is a combination projection aligner and stepper that PE has been developing since about 1983 or 1984. The Micrascan 1 is a production tool capable of 0.5-micron resolution and a throughput of 35 to 50 200mm wafers per hour. It will clearly have a major impact on the lithography market in general and steppers in particular. Because of the possible impact of this tool, a separate newsletter has been written entitled "Step and Scan: Perkin-Elmer's Micrascan 1," which will be sent to our clients in April.

TRENDS IN E-BEAM TECHNOLOGY

Several papers commented that conventional raster-scan e-beam systems are slow and not suitable for maskmaking of 16Mb DRAMs or direct-write applications involving large chips with submicron features. Instead, variable-shaped, vector-scan e-beam systems will be used in the future for making 16Mb DRAM reticles, and also for direct-write "system-on-a-chip" ASICs. Variable-shaped systems have the advantages of smaller address unit size, which enables better pattern placement accuracy for submicron devices, and higher writing speed. However, data preparation and formatting is more complicated for the variable-shaped systems, and sophisticated, hierarchical computers are being used to ensure maximum productivity of these e-beams.

Mitsubishi reported the fabrication of 16Mb DRAM 5X reticles using JEOL's JBX-6AIII vector-scanned, variable-shape e-beam system. Using high-quality Molysilicide reticle blanks, Mitsubishi was able to fabricate the 16Mb DRAM reticles with a throughput time of one hour per layer, compared to three hours per layer using conventional raster-scan e-beam systems.

TRENDS IN X-RAY LITHOGRAPHY

Steady progress continues to be made in the area of compact synchrotron orbital radiation (SOR) X-ray sources such as the Fraunhofer Institute COSY project and NTT's super-ALIS ring. Other than the IBM effort, most of the SOR X-ray lithography work is being carried out in Japan and Europe. U.S. merchant semiconductor manufacturers are not investing in this long-term, potentially rewarding research effort. Instead, their efforts are more short-term, and focused on migrating down the optical lithography scale through high NA g-line, i-line, and then excimer laser steppers to obtain resolution limits of about 0.3 micron.

Meanwhile, the goal of an SOR ring with 10 to 15 stepper beam ports with beam energies of 500 to 600 Mev and currents of 10mA seems achievable, notwithstanding the high cost--in the tens of millions of dollars. SOR problems remaining to be solved include reduction of the SOR footprint and cost, selection of an appropriate gas-environment to prevent reticle heating due to radiation, and expansion of the exposure area while maintaining the energy flux to ensure alignment accuracy and high throughput.

Positive and negative single-layer X-ray resist processes under development look promising. The Fraunhofer Institute, in conjunction with Karl Suss, is developing the XRS 200 stepper, which has a resolution of 0.15 to 0.20 micron, while maintaining an alignment accuracy of 0.070 micron. Low throughput of five 100mm wafers per hour is constrained by the alignment system. NTT is also developing a prototype exposure system, and Nikon has fabricated 1Mb DRAMs using its SX-5 X-ray stepper, which has a high-brightness X-ray tube source (10kW) with a rotating palladium target.

The main problem with X-ray lithography is the difficulty in fabricating high-quality, 1X X-ray masks with the pattern placement, resolution, and low defects required for nanometer processing. Advancements continue to be made in X-ray mask materials such as silicon nitride (SiN) and silicon carbide (SiC) membranes layered with high-quality X-ray absorbers such as tantalum or tungsten alloys. The masks have to be fabricated with high accuracy using e-beam techniques with spot sizes of 300 angstroms. Substantial advances are still needed in the areas of X-ray mask inspection and defect repair to enable X-ray maskmaking techniques to be implemented in production.

Hampshire Instruments is booking orders for its laser-plasma-based soft X-ray stepper that has a 1.4nm peak source wavelength. Hampshire's system is capable of 0.5-micron production resolution with 0.25 micron expected in the future. Alignment accuracy is 0.06 micron using single-layer novolac resists. The relatively low cost of this system (compared to SOR-based X-ray lithography) coupled with its small footprint (25 ft^2) makes this system attractive to merchant semiconductor companies who do not have the deep pockets to invest in long-term SOR technologies but still need to begin research in X-ray lithography.

TRENDS IN ION BEAM LITHOGRAPHY

As device-features become submicron, focused ion-beam (FIB) technologies are finding new areas of applications:

- Toshiba reported the feasibility of gallium-ion FIB technology for fuse-blowing in redundancy applications for 16Mb/64Mb DRAMs. Laser-beam technology, which is currently used for 1Mb and 4Mb DRAMs, does not have the narrow, focused spot sizes needed for the 2-micron size fuses expected to be used in the future for 16Mb/64Mb DRAMs.

- FIB technology is being used for local deposition and repair of interconnect lines in integrated circuits. Micrion Corporation reported a FIB system for local deposition of tungsten using tungsten carbonyl as the source gas. Use of these FIB deposition techniques gives the circuit designer an economical tool for rapid failure analysis and debugging of prototype products.

- FIB techniques are being explored for the repair of clear defects in X-ray masks. In combination with focused ion-beam milling, FIB deposition enables a single-system solution for the repair of clear and opaque defects in X-ray masks. The Fraunhofer Institute reported the use of a Micrion 800 FIB system for localized deposition of high-quality tungsten absorber material in clear-defect areas on X-ray masks using tungsten carbonyl as the source gas.

TRENDS IN RESIST TECHNOLOGY

Developments in resist technology were strongly coupled with the efforts in optical lithography to push deep UV lithography into the 0.5-micron regime. More than ever before, the development of stepper technology and resist chemistry have to proceed in a synergistic fashion to provide semiconductor manufacturers with submicron processes that have sufficient process latitude. Large, vertically integrated companies, such as AT&T, Hitachi, IBM, and Toshiba, have substantial in-house development efforts in complementary technology areas such as resist chemistry, stepper/e-beam imaging optics, and dry etch processing. Such broadbased research efforts enable systematic evaluation of an array of technological alternatives in order to choose the most effective technology path.

Semiconductor manufacturers would like to use their long experience with g-line lithography as long as possible, and there is a wide consensus on using high-performance, optimized, single-layer, g-line resists in combination with high NA g-line steppers to push as far as possible into the submicron regime. However, the steep topographies associated with trench structures and multilevel interconnect processes increase the required depth of focus. I-line steppers have the advantage that DOF can be increased over g-line, but i-line resists are still new and not fully characterized.

In an attempt to prolong the life of g-line resists, many techniques, such as surface imaging and dry develop, image reversal, resist pretreatment before exposure, postexposure bake, and UV flood expose, are being extensively explored.

Silylation–based surface imaging processes, such as the DESIRE process developed by UCB Electronics, were discussed extensively at the symposium. Texas Instruments is examining the feasibility of implementing such a process in production for 0.5–micron g–line and i–line lithography. Silylated resists also are being developed to solve some of the pattern definition and focus stability problems associated with 248nm excimer lasers.

IC METROLOGY, INSPECTION, AND PROCESS CONTROL

In this area, a total of 55 papers were presented, including 34 regular papers and 21 poster session presentations. Although many topics were discussed, this section will focus only on developments in automated wafer inspection systems. This is an exciting, high–growth market segment within the equipment categories of wafer inspection and joint CD/inspection systems. In 1988, sales of automated wafer inspection systems with automatic defect detection grew 94 percent over 1987 levels and accounted for approximately 60 percent of the $100 million combined market for wafer inspection and joint CD/inspection systems. Two companies alone—Insystems and KLA Instruments—accounted for this market growth in automated defect detection systems.

Insystems manufactures an automated wafer inspection system that relies on a marriage of technologies—spatial frequency filtering and holography—to detect defects across the entire wafer automatically. An important feature of the holographic application is the ability to capture three–dimensional information. This means that no defect is ever out of focus.

Insystems discussed a technique for defect partitioning that allows the user to pinpoint the source of each defect and determine if a defect results in permanent damage to the device and ultimate yield loss. In this procedure, wafers are inspected at several critical process steps. The defect maps obtained at each process step are stacked, and special algorithms are used to process the data at each level. The defect partitioning analysis includes subtracting defects from previous levels in order to identify those defects unique to each layer. The defect information is correlated with electrical test in order to evaluate the impact of specific defects on yield loss. This type of defect partitioning study provides a methodology to study even those defects that do not directly affect yield. These nuisance defects of today might well be the killer defects of tomorrow's advanced devices.

In 1984, KLA Instruments introduced the KLA–2020, the industry's first fully automated wafer inspection system with automatic defect detection. Subsequent products, the 2028 and the 2030, provide enhanced defect detection capability. At this year's meeting, two papers were presented that discussed KLA's automated inspection systems.

KLA itself discussed the necessity for users of automatic wafer inspection equipment to establish regular characterization routines. For example, KLA emphasized the need to perform regular checks on standard wafers and to generate capture rate curves to establish a confidence measure for a given system's performance. In addition, KLA discussed the importance to the user of understanding false alarms—alpha errors, when a defect exists but is missed by the system, and beta errors, when a defect does not exist but "something" is detected.

In the second paper, Intel discussed a technique for combining electrical defect monitors with automated wafer inspection (a KLA–2028) in order to evaluate large sample sizes on the wafer efficiently. As defect densities decrease, larger and larger sample sizes are required in order to establish statistically valid information. Essentially, the electrical defect monitor is used to locate killer defects while the KLA–2028 is used to obtain defect information on those dead die. By combining both of these tools, large areas can be analyzed with detailed defect analysis applied only where it is required.

Joseph Grenier
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Conference Schedule

1989

Semiconductor User/ Semiconductor Application Markets	February 27–28	Le Meridien Hotel San Francisco, California
Japanese Components	April 20–21	Tokyo Bay Hilton International Tokyo, Japan
Computer Storage	April 26–28	The Doubletree Hotel Santa Clara, California
Document Processing	May 16–18	Monterey Sheraton Hotel Monterey, California
Copiers	May 16–17	
Printers	May 16–17	
Electronic Publishing	May 18	
Imaging Supplies	May 18	
Color	May 18	
SEMICON/West Seminar	May 24	The Dunfey Hotel San Mateo, California
Telecommunications	June 5–7	Silverado Country Club Napa, California
European Components	June 7–9	Park Hilton Munich, West Germany
Asian Semiconductor and Electronics Technology Seminar	June 28	Radisson Hotel San Jose, California
Financial Services	August 22–23	The Doubletree Hotel Santa Clara, California
Technical Computing and Applications	September 11–13	The Doubletree Hotel Santa Clara, California
European Copying and Duplicating	September 18–19	Majestic Hotel Cannes, France
Western European Printer	September 20–22	Majestic Hotel Cannes, France
Taiwan Conference	September 25–26	Grand Hotel Taipei, Taiwan
Distributed Processing	September 26–28	The Doubletree Hotel Santa Clara, California
SIA/Dataquest Joint Conference	September 27	Santa Clara Marriott Santa Clara, California
Information Systems	October 2–6	Tokyo American Club Tokyo, Japan
Semiconductor	October 16–18	Monterey Sheraton Hotel Monterey, California
Asian Semiconductor and Electronics Technology	November 2–3	Kunlun Hotel Beijing, China
European Telecommunications	November 8–10	Grand Hotel Paris, France
European Personal Computer	December 6–8	Athens, Greece

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STEP AND SCAN: PERKIN-ELMER'S MICRASCAN 1

INTRODUCTION

Perkin-Elmer recently introduced its long-awaited step-and-scan lithography tool, which it has been working on since 1982 or 1983. This tool is a major technological development and may have a very significant impact on the future lithography market. In addition, the new Micrascan 1 will give Perkin-Elmer a very much needed boost to help the company reverse its current trend in sales and help recover the technological and market momentum that it enjoyed in the past.

The following is a discussion of the goals of lithography in general and the Perkin-Elmer Micrascan 1 as it pertains to these goals.

BALANCING THE LITHOGRAPHY GOALS

One goal of semiconductor manufacturers is to maximize lithography system resolution, depth of focus, and the associated critical dimension (CD) control. Simultaneously, they strive to increase the usable image field size in order to accommodate larger, more powerful integrated circuits; to reduce the reticle sensitivity to defects; and to aid in tooling inspection. The problem, however, is that the goals of large image field and high resolution are mutually exclusive.

For a reduction stepper system, increasing the lens image field size for a given numerical aperture requires the use of larger diameter internal lens elements and/or more individual elements in the lens design. However, lens aberrations are a function of both the lens element diameter and the image field diameter. Therefore, the process of increasing image field diameter introduces lens complexity and usually reduces image fidelity via increased levels of aberration. To increase resolution at this point by increasing the numerical aperture (NA) compounds the dilemma by again increasing the lens diameter, which drives aberrations up again. The well-publicized Rayleigh relationship between NA, imaging wavelength (λ), and depth of focus (DOF) is:

$$DOF \propto \frac{\lambda}{NA^2}$$

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This relationship further depicts the negative aspect of increasing NA to achieve higher resolution: higher numerical aperture directly reduces lens depth of focus and process latitude.

Several new g-line and i-line lenses have recently been introduced by the stepper manufacturers for 4Mb and 16Mb DRAM production. The g-line lenses have numerical apertures as high as 0.54 to obtain 0.65-micron resolution. However, the total depth of focus for these 15mm x 15mm image field size lenses is about 1.2 microns, thus requiring planarization schemes. New i-line lenses also offer high resolution, a 15mm x 15mm field size, and provide a slightly larger depth of focus, but must be used in conjunction with relatively new and not fully characterized i-line optimized photoresists.

Excimer laser steppers also are being developed to push optical lithography to the 0.5-micron level and below, but improvements still need to made in excimer laser sources, lens design, and photoresists.

This brings us to the Perkin-Elmer Micrascan 1. This tool employs a unique scanning technology pioneered in the early '70s that balances the lithography goals by breaking down the long-standing barrier to simultaneously achieving high resolution, depth of focus, and large image field size. Moreover, Perkin-Elmer claims that it has achieved these goals with a design that results in radically lower color and geometric aberrations as compared to the best g-line lens design.

The Micrascan 1 System

The Micrascan 1 system is a 4:1 reduction, step-and scan projection aligner. It uses a reduction lens design involving both mirrors and lenses to achieve 0.5-micron resolution, large field size, and a compatible depth focus. Table 1 presents some of the Micrascan 1's performance specifications.

Table 1

Micrascan 1 Performance Specifications

Specification	Value
Resolution	0.5 micron
Depth of Focus	+/-0.75 micron for +/-10% CD control at rated resolution.
Exposure Wavelength	240-255 nanometers
Image Field Size	20 x 32.5mm for 6 x 6-inch reticles
Numerical Aperture	0.357
Reduction Ratio	4:1
Distortion	+/-0.07 microns; full field
Machine-to-Machine Overlay	+/-0.15 microns (98% of data)
Throughput (10mJ/cm^2 dose)	35-50 200mm wafers per hour
Reticle Change Time	6 seconds
Reticle Capacity	12

Source: Perkin-Elmer Corporation
Dataquest
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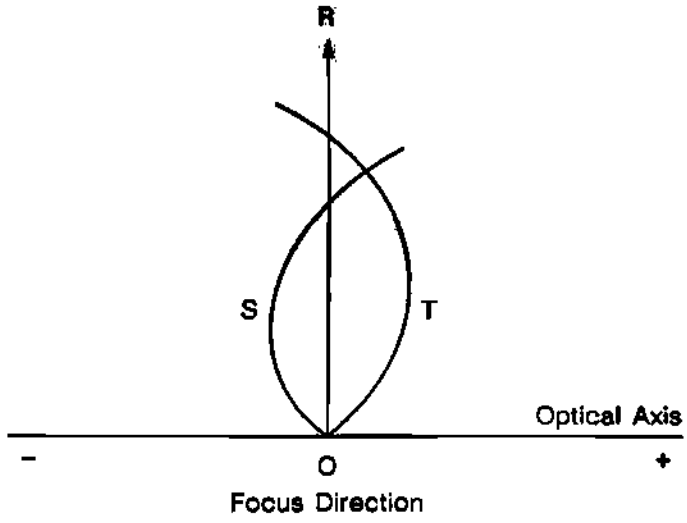
Theory of Operation

The image field shape of the reduction lens can be depicted by the field curves shown in Figure 1. The generalized field curves indicate the radially symmetric shape of the best image surface for reticle information lining up in the radial and transverse directions.

Figure 1

Image Field Curves



R = Maximum Image Field Radius

T = Tangential Information Direction

S = Sagittal or Radial Direction Information

0003647-1

Source: Perkin-Elmer

Astigmatism is commonly defined as the distance in microns between the S and T best focus positions for a given radial image field location, and is, therefore, an image field-dependent aberration. Astigmatism is generally at a minimum near the optical axis (the sweet spot) and worst at the edge of the image field. All refractive, full-field, reduction lenses (g-line, i-line, excimer, etc.) have astigmatism, which reduces image fidelity and depth of focus.

The Micrascan 1 uses only that portion of the image field corresponding to the point where the S and T best image surfaces intersect, which is the zero astigmatism zone. Since the field curves are radially symmetric, the zone of zero astigmatism is a radial slit. This slit imaging system is scanned in relationship to the reticle and wafer to expose a large chip area. In this way, the previously mutually exclusive goals of high resolution (high NA, tight aberration control) and large chip size can now be simultaneously accomplished.

The Micrascan 1 system's slit-shaped, instantaneous image field is 20mm high by 1.3mm wide. During exposure, the reticle and wafer stages are synchronously scanned to expose a full 20mm x 32.5mm rectangular chip area. To maintain alignment during the scanning process to better than +/- 0.04 micron, two separate alignment systems continuously monitor and lock together the reticle and wafer pattern positions via closed-loop servo control and high-resolution laser interferometer techniques.

For illumination, the Micrascan 1 uses a high-pressure mercury-xenon arc lamp for its source of deep UV light, as contrasted with the complex, wavelength-narrowed and stabilized excimer lasers used in excimer steppers.

Perkin-Elmer's customer/development partner has developed a proprietary resist in order to maximize the performance of the system in the deep UV region. Perkin-Elmer, however, reports that commercial resists will soon be available. In a recent presentation at the 1989 SPIE Symposium on Microlithography held in March, Perkin-Elmer stated that the Micrascan 1 could resolve 0.5 micron in 0.9 micron of resist, and 0.4 micron in 0.6 micron of resist. The light intensity and large field size allows from 35 to 50 200mm wafers per hour throughput.

DATAQUEST ANALYSIS

For nearly a decade now, we have watched the resolution limits of semiconductor fabrication processes decrease according to a very stable rule of thumb; that is, line geometries decrease by the square root of two for each new device generation (or about 12 percent a year). Since a new generation is introduced about every one-third of a decade, 0.5-micron production is due by 1993. The major semiconductor processes, such as lithography, deposition, etching, and doping, are all on this schedule. The lithography process has been setting the pace of the schedule and has provided the line geometry target that the other processes use as a goal. With the new Micrascan 1, Perkin-Elmer has jumped ahead in the lithography process, and the effects on the industry will be significant.

For example, stepper manufacturers are now forced to react and move ahead with projects which, before the Micrascan 1, may have been done on a more leisurely schedule. In order to cope with a larger field size, stepper vendors must develop the technique of stitching for very large reticles. They must also work more diligently with their customers and with other equipment vendors in order to perfect planarization schemes. The advent of excimer laser steppers or high numerical aperture lenses does not circumvent the dilemma regarding field size versus depth of focus.

Stepper customers may repeat the scenario that they followed with the transition from projection aligners to steppers. Then, they chose to bring in the newer-technology steppers with their advanced capability, even through the projection aligners were more cost effective and could do the job. Steppers gave the semiconductor manufacturers more process flexibility and pointed the way for other, no less important processes to be developed. We believe that semiconductor manufacturers will be tempted to bring the Perkin-Elmer technology into their fabs as soon as possible, preempting the steppers for 16Mb DRAM production. In addition, there may be significant 4Mb production on the Micrascan 1.

MARKET IMPACT

Perkin-Elmer shipped the first beta system in mid-1988, and at least the entire first year's production has been allocated to the beta site customer. There are more than a dozen Micrascans on the Perkin-Elmer production floor, and more are in the build schedule. At $4 million per system, the Micrascan will significantly affect the lithography market share picture.

If this is indeed a superior technology, it certainly represents a competitive advantage for Perkin–Elmer with respect to the other lithography vendors. In addition, it could represent a significant competitive advantage to those semiconductor companies who choose this technology. We will be watching with great interest to see if Perkin–Elmer can implement this technology. We also will be monitoring SEMATECH's attitude toward this technology as a possible way to recapture some of the schedule delays that the manufacturing consortium has experienced since its inception.

One final comment on the possible impact of this technology. At the conclusion of Perkin–Elmer's paper on the Micrascan 1 on March 3, 1989, at the SPIE Microlithography symposium, a question was directed to the Perkin–Elmer speaker on what the company had in mind for the future for the Micrascan. The speaker, with a broad smile, said simply, "The tool has a great deal of growth potential."

Joseph Grenier
Robert McGeary

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Lithography
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SYNCHROTRON ORBITAL RADIATION UPDATE: JAPANESE PROJECTS UNDER WAY

SUMMARY

Japanese research on synchrotron orbital radiation (SOR) rings for 64Mb and higher memories is building momentum rapidly. Currently, there are 5 new SOR facilities and 19 more being planned. SOR is viewed by Japanese semiconductor makers as the strategic tool to develop 64Mb and higher RAMs and will be one of the future applications for superconducting magnets. Excimer lasers and electron beam equipment are also under consideration, but technical obstacles make them inadequate for mass production of DRAMs. This newsletter provides an update to our previous newsletter (see JSIS Research Newsletter number 1987-30, entitled "Synchrotron Orbital Radiation: Japan's Push into Ultradense Megabit Memories") and focuses on the SOR projects listed in Table 1.

Table 1

Japanese SOR Research Activity

Company/Ministry	Location	Project Status
Ishikawajima-Harima	Tokyo	SOR research center from late 1988
Ministry of Education (MOE)/ Fujitsu/Hitachi/NEC/NTT	Tsukuba	Working on 64Mb memories
NTT/Hitachi/Toshiba	Atsugi	64Mb DRAM being developed on 5m-diameter ring
Ministry of Education (MOE)/ Sanyo	Tsukuba	3-micron mask pattern reduced to 0.75 micron at MOE's SOR ring

(Continued)

Table 1 (Continued)

Japanese SOR Research Activity

Company/Ministry	Location	Project Status
Science and Technology Agency (STA)	West Harima	Detailed planning in 1989; begin construction in mid-1990; operations from 1995
Sortech	Tsukuba	Purchase of Mitsubishi's SOR equipment
Sumitomo Electric/ MITI Electrotechnical	Tsukuba	Developing ultrasmall 50cm-diameter ring with more than 3m diameter

Source: Dataquest
March 1989

WHY SYNCHROTRON RESEARCH?

In the United States, considerable debate exists over the relative merits of SOR because of the installed base of optical steppers and competition from excimer lasers and electron beam equipment. However, Japanese manufacturers note that the mass production capabilities of these competing technologies are limited for the following reasons:

- SOR masks are still difficult to make, limiting their short-term feasibility (for 16Mb DRAMs), but Japanese companies believe that this problem can be solved.
- Optical stepper resolution is limited to 0.25 micron, but uncertainties exist for mass production below 0.5 micron.
- Direct-write electron beam is good for fast-turnaround ASICs, but its low wafer throughput makes it unsuitable for DRAMs.
- Excimer lasers offer high resolution and wafer throughput, but laser source stability and photoresist are limiting factors. (Even if resolution is resolved at 16Mb, the same issue arises at 64Mb.)

Although optical steppers could be used to manufacture large-die 64Mb DRAMs on 8-inch wafers, high defect levels and low yield ratios will ultimately force Japanese manufacturers to move to the 0.30- to 0.35-micron range, as shown in Figure 1. While 0.35-micron patterns have been drawn using optical steppers, their reliability for high-volume manufacturing is still uncertain. Since NTT, Toshiba, and other Japanese manufacturers have already developed prototype 16Mb DRAMs on optical steppers, their most likely strategy will be two-pronged: to push optical steppers as far as possible and to begin developing SOR technology. Excimer lasers could be used as a backup technology.

Figure 1

Lithography Technology Trends

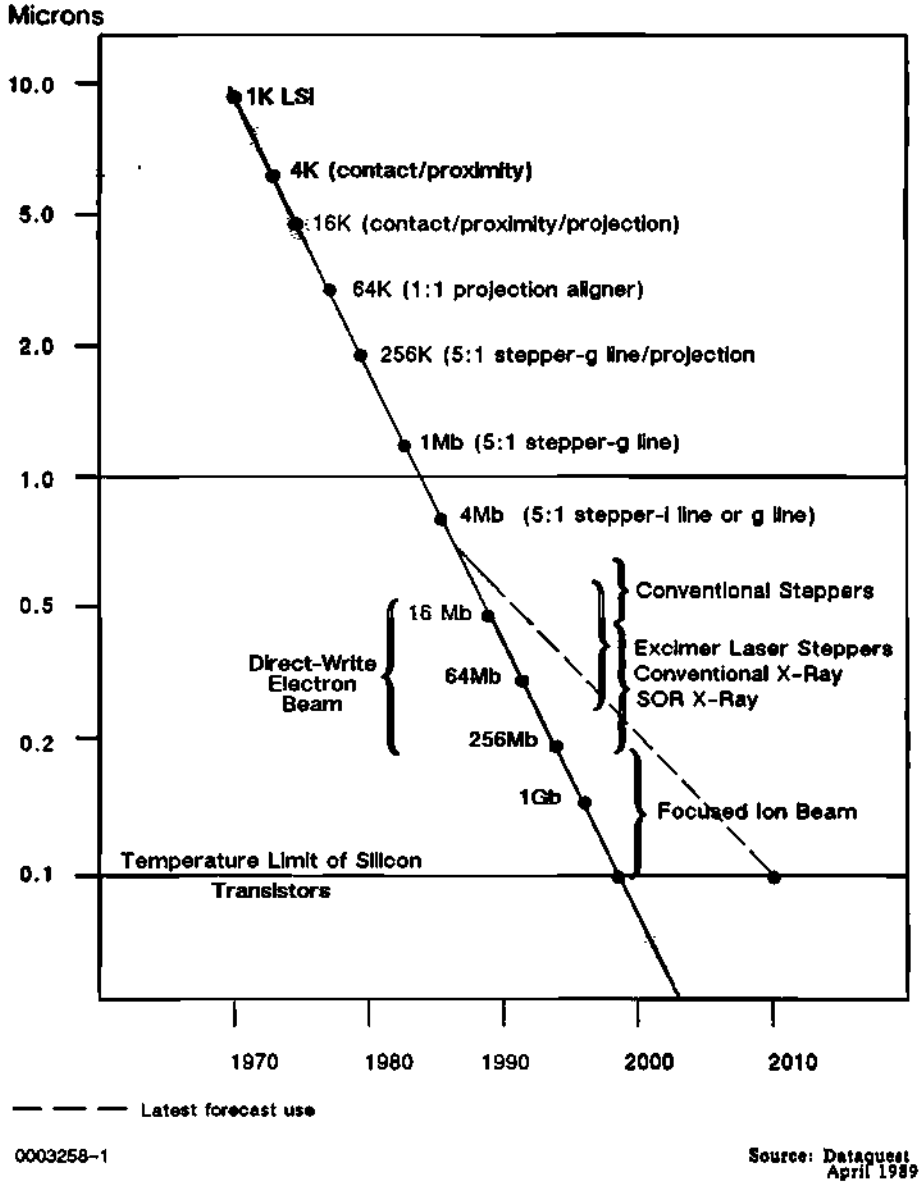

Table 2 lists the major industrial facilities for SOR rings currently being used and planned in Japan.

Table 2

Major SOR Facilities in Japan

Organization	Completion Date	Name	GeV	Magnet Type
Hiroshima University	1992	Hi-SOR	1.50	N/A
Ishikawajima-Harima	1989	N/A		Conventional
Kyushu University	N/A	SOR Center	1.30	N/A
MITI Electrotechnical	1981	TERAS	0.80	Conventional
MITI Electrotechnical	1988	NIJI II	0.50	Conventional
MITI Electrotechnical	1990	NIJI III	0.62	N/A
MOE High-Energy Physics	1982	Photon Factory	2.50	Conventional
MOE High-Energy Physics	1985	TRISTAN-AR	6.00	Conventional
MOE High-Energy Physics	TBD	Super Photon Factory	10.00	N/A
Molecular Science Lab	1984	UV-SOR	0.60	N/A
NTT Corp. (Atsugi Lab)	N/A	N/A	N/A	Conventional
NTT Corp. (Atsugi)	1988	SOR Light	0.80	Superconducting
Riken	1995	Compact SOR	6.00	N/A
Sortech (Mitsubishi Electric)	1988	Compact SOR	1.00	Conventional
Sumitomo Electric	1988	N/A		Conventional
Sumitomo Electric	1989	N/A		Superconducting
Sumitomo Heavy	1988	Aurora	0.65	Superconducting
Tohoku University	N/A	Stretcher	1.50	N/A
Tokyo University	1975	INS-SOR II	0.40	Conventional
Tokyo University	N/A	VUV-SOR	1.00	N/A
West Harima Technopolis	Late 1990s	SOR Research Center	8.00	N/A

N/A = Not Available

Source: Japan Industrial Journal
Japan Industrial Daily

STATUS OF SOR PROJECTS

The following paragraphs are short descriptions of the current status of Japanese SOR research activities listed in Table 1.

Ishikawajima–Harima

Ishikawajima–Harima, a Japanese shipbuilder, announced plans to enter the SOR field by opening an R&D center in the Tokyo region at the end of 1989.

MOE High–Energy Physics Lab/Fujitsu/Hitachi/NEC/NTT

Fujitsu, Hitachi, NEC, and NTT Corp. are developing 64Mb and higher memories on a 28–meter–diameter, 2.5–GeV SOR ring and, more recently, on a 10–meter–diameter, 645–MeV SOR ring. The four companies are using the SOR ring at the Ministry of Education's (MOE's) High–Energy Physics Laboratory in the Tsukuba Science City.

NTT Corp./Hitachi/Toshiba

In early 1988, NTT Corp. began testing a 15–meter–diameter, doughnut–shaped synchrotron at its LSI Laboratory in Atsugi, Kanagawa Prefecture. The ¥20 billion ($166 million) machine, which was funded jointly with Hitachi and Toshiba, radiates 5– to 10–angstrom soft X–ray beams capable of drawing 0.35– to 0.20–micron lines. The electron energy is accelerated to 15 MeV by a 16.8–meter–long linear accelerator, further accelerated to 800 MeV by a 15 x 15–meter accelerator ring, then stored in a 2 x 8–meter storage ring. The ring uses powerful superconductor electromagnets to produce the magnetic fields. In July 1988, NTT Corp. successfully tested a 0.35–micron MOS prototype device with a 20ps gate speed. The goal is to develop a 64Mb DRAM in the 1990s and a 100Mb DRAM by the year 2000.

NTT Corp. is also developing 64Mb DRAMs with Fujitsu, Hitachi, and NEC on a 10–meter–diameter SOR ring operated by the MOE's High–Energy Physics Laboratory in Tsukuba. In March, NTT produced the world's first chemical vapor deposition (CVD) thin film using SOR equipment, which can be used for 64Mb and 256Mb DRAMs. Two methods are used. In the first, gas is pumped over the substrate, triggering an electrical discharge; then the gas molecules are analyzed as the layers are formed. In the second, gas is pumped onto the substrate in the center of the furnace, which is heated to 1,000 degrees Celsius.

Sanyo Electric/MOE High–Energy Physics Lab

In August 1988, Sanyo Electric announced that it had drawn a 0.75–micron line using a 3–micron mask using a pattern–reduction transfer method. The experiments were conducted at the SOR ring at MOE's High–Energy Physics Laboratory in Tsukuba. Sanyo used a 3.5–angstrom wavelength light to direct X–ray beams onto a single–crystal silicon wafer. However, Sanyo encountered problems with a weak contrast below a 2.5–micron mask pattern. Exposure time was from 30 to 60 minutes.

Science and Technology Agency (STA)

The STA selected the West Harima Technopolis site in Hyogo Prefecture for its 6-GeV SOR storage ring. The ¥100 billion ($833 million) storage ring will have a diameter of 300 to 450 meters, a circumference of 1 kilometer, and 100 beam-emitter locations. Detailed plans will be developed in 1989, with construction beginning in mid-1990. Operations are scheduled from 1995. The SOR ring will be used for submicron analysis, VLSI research, and biological topics.

Sortech

In June 1986, the Japan Key Technology Center and 13 Japanese semiconductor device and equipment makers formed Sortech to develop compact SOR equipment for manufacturing 64Mb DRAMs and higher. Current 10-meter-diameter SOR systems are too large for existing wafer plants. Capitalized at ¥214.3 million ($1.8 million), the joint venture company plans to spend ¥14.3 billion ($119.2 million) during its 10-year R&D program (ending March 1996). The Key Technology Center is providing 70 percent of the funding and the companies, the remaining 30 percent. Members include Canon, Fujitsu, Hitachi, Matsushita, Mitsubishi, NEC, Nikon, Oki Electric, Sanyo, Sharp, Sony, Sumitomo, and Toshiba.

As of mid-1988, the 13 participating Japanese companies had assigned 34 researchers to Sortech. Their initial goal is to quickly develop large-SOR-ring technology, then focus on developing compact SOR rings. Currently, Sortech is conducting basic research on lithography, instrumentation for research uses, and device maker requirements.

The following is a chronology of Sortech's activities:

- July 1987—Sortech R&D began with discussions with Hitachi, Mitsubishi Electric, Sumitomo Heavy, and Toshiba to allocate SOR equipment design and manufacturing.

- January 1988—Sortech placed a ¥2.7 billion ($22.5 million) order with Mitsubishi Electric for design of 1-GeV SOR equipment by late 1988. The equipment will feature a 200mA electron beam, 15.5-angstrom wavelength, 46-meter circumference, and 40-MeV injector. Hitachi and Toshiba are also involved, but Mitsubishi received the largest order.

- September 1988—Sortech opened Tsukuba research center. The center has two buildings: a 1,200-square-meter research building and a 3,300-square-meter laboratory. Construction cost approximately ¥2.5 billion ($20 million).

Sumitomo Electric/MITI Electrotechnical Laboratory

With MITI's Electrotechnical Laboratory in Tsukuba, Sumitomo Electric is developing an ultrasmall 50-centimeter-diameter SOR ring with an overall .3-meter diameter. A prototype ring was completed and recently began test operations at Sumitomo's plant in Tokyo.

DATAQUEST OBSERVATIONS

Although the Japanese are starting behind the West Germans, who were planning on a commercialized compact SOR ring, Dataquest believes that the Japanese are rapidly catching up because the Germans' compact ring project has been put on hold. Sumitomo Heavy has already developed a compact SOR ring, and Mitsubishi Electric will provide one to Sortech in 1989. By the early 1990s, at least half a dozen Japanese companies will have compact SOR prototypes for in-house research.

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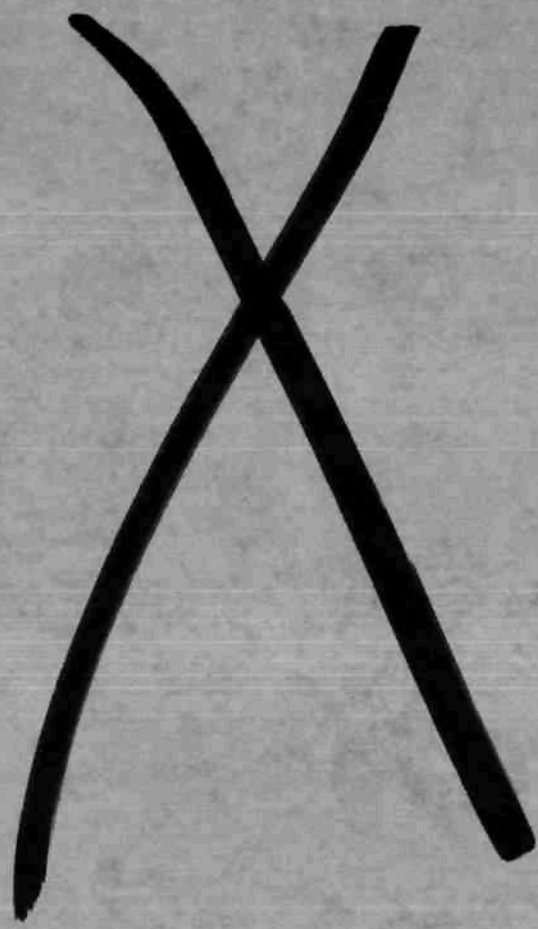

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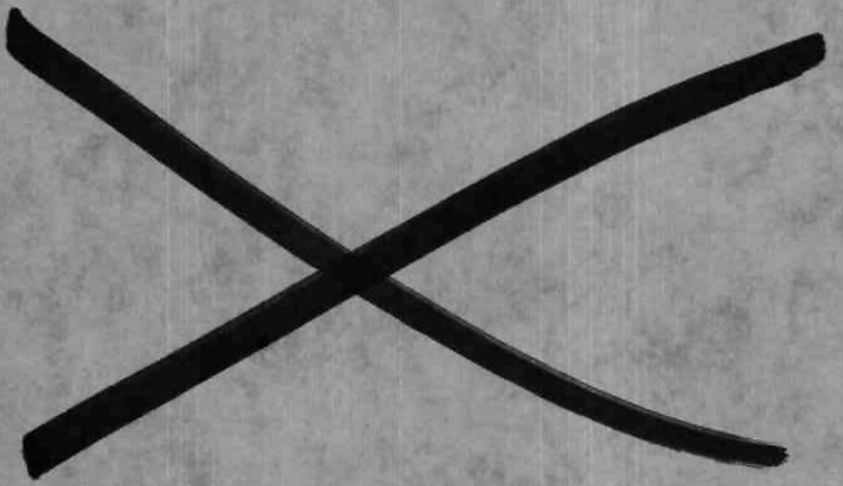

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Research Newsletter

1989 VLSI MULTILEVEL INTERCONNECT CONFERENCE: HOW DO THE TECHNOLOGIES STACK UP?

INTRODUCTION

This newsletter presents key technology trends from the June 1989 VLSI Multilevel Interconnect Conference (VMIC 1989) held in Santa Clara, California. Multilevel interconnect technology is rapidly emerging as one of the cornerstone technologies in submicron devices. Dataquest believes that an optimum choice of the interconnect process largely determines semiconductor manufacturing costs, production yields, and product reliability. Each year the VMIC forum serves as a barometer of trends in multilevel interconnect processing; this year was no exception. Semiconductor equipment, materials, and device companies presented a variety of stacked interconnect schemes to manufacture reliable, high-performance devices. This newsletter describes trends in interconnect process integration, dielectrics, metallization, and planarization that were presented at VMIC 1989. Dataquest believes that the trends presented here are indicative of important advances in mainstream interconnect technology.

INTERCONNECT PROCESS INTEGRATION TRENDS

Table 1 lists the key features of multilevel interconnect processes described by major worldwide semiconductor companies at VMIC 1989. Dataquest observes a wide variety of interconnect processes currently being developed by semiconductor manufacturers for submicron applications. As the number of metal levels increases, chip manufacturing cost is dominated by the interconnect process. Processes are being developed with emphasis on manufacturability and reliability. Semiconductor companies are leveraging their research efforts by developing common interconnect modules applicable to a broad spectrum of products such as memories, standard logic, and ASICs.

TABLE 1
Key Features of Multilevel Interconnect Processes Developed by Major Worldwide Semiconductor Companies

	AT&T	Hitachi	IBM	Motorola	NEC	SGS-Thomson
Products	ASIC	1Mb SRAM 32-bit CPU ASIC	64K SRAM	ASIC	R&D	ASIC
Technology	CMOS	CMOS BiCMOS	CMOS Bipolar	CMOS	R&D	CMOS
Minimum Design Rule	1.0	0.8	0.8	1.0	N/A	1.2
Maximum Levels of Interconnects	2	4	2	3	2	3

(Continued)

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TABLE 1 (Continued)
Key Features of Multilevel Interconnect Processes Developed by Major Worldwide Semiconductor Companies

	AT&T	Hitachi	IBM	Motorola	NEC	SGS-Thomson
ILD between Poly and First Metal	BPSG	BPSG	Oxide/nitride	BPSG	Oxide	PSG/SOG/BPSG
Barrier Metal	None	None	Ti/TiN	Ti/TiN	TiW	Ti/TiN
Contact Plug	None	None	Blanket tungsten	None	None	None
First Metal	Al-Si-Cu	Sputter tungsten	Ti/Al-Cu	Blanket tungsten	Gold/selective tungsten	Al-Si-Cu
ILD between First and Second Metal	PETEOS oxide	PSG/SOG/PSG	Oxide/nitride	BPSG	Organic polysiloxane	Oxide/SOG/ oxide
First Via Plug	None	None	Blanket tungsten	None	Selective tungsten	None
Second Metal	Al-Si-Cu	TiN/Al	Ti/Al-Cu	Al-Si-Cu	TiW/Gold	Al-Si-Cu
ILD between Second and Third Metal		PSG/SOG/PSG		PETEOS oxide		Oxide/SOG/ oxide
Third Metal		TiN/Al		Al-Si-Cu		Al-Si-Cu
Fourth Metal		TiN/Al				

N/A = Not Available

Source: VMIC 1989
Dataquest
September 1989

Hitachi's submicron interconnect process is capable of being extended to four levels of interconnects for applications such as 1Mb SRAMs and ASICs. Companies such as IBM and Motorola are investigating the use of blanket tungsten chemical vapor deposition (CVD) as a contact/via plug and first-level metal. CVD tungsten has the benefits of better step coverage, reliability, and current-carrying capability compared with sputtered aluminum; however, tungsten has the disadvantages of higher resistance and more complex processing when compared with aluminum. Other companies such as SGS-Thomson are developing sputtered barrier alloys such as titanium nitride (TiN) or titanium-tungsten (TiW) to ensure reliable interconnect performance.

New materials such as tetraethylorthosilicate (TEOS) oxide precursors, spin-on-glass (SOG), polysiloxanes, and polyimides are being developed for submicron multilevel interconnect processes. Organic-source oxides such as TEOS are expected to be more conformal and easier to use in production compared with conventional silane-based oxides.

Borophosphosilicate glasses (BPSG) continue to be popular as the dielectric of choice for low-temperature reflow applications between poly and first-level metal. Plasma-enhanced CVD oxide is preferred for dielectric applications between metal levels due to its low deposition temperature. High temperatures during interlayer dielectric CVD deposition can otherwise cause hillocks and low fabrication yields due to electrical shorts.

INTERLAYER DIELECTRICS AND PLANARIZATION TRENDS

Interlayer dielectric film deposition and planarization is one of the most challenging problems in submicron multilevel processing. Previous ILD processes such as resist etchback or SOG planarization were adequate for processes with a metal space design rule greater than 1 micron. However, semiconductor manufacturers are evaluating new processes with better uniformity, lower defects, and more cost-effective ILD films for submicron applications. Dataquest believes that the following ILD deposition and planarization trends are illustrative of various submicron interconnect technologies.

In Situ ILD Deposition and Planarization in Integrated Process Equipment

Integrated cluster tools have the advantages of flexibility and in situ deposition/etchback processing capability. IBM and Cypress Semiconductor presented ILD planarization processes using Applied Materials' PE5000 integrated, multichamber CVD system. The process sequence includes plasma-enhanced TEOS oxide (PETEOS), TEOS/ozone-based thermal CVD oxide (ThCVD), argon sputter etching, and carbon tetrafluoride-based reactive ion etch (RIE). All deposition and etchback planarization steps are carried out in situ under vacuum. Throughputs of 8 to 10 wafers per hour are obtained with this process. IBM and Cypress Semiconductor claim lower defects, higher yields, and higher effective throughputs compared with SOG or resist etchback planarization processes.

Applied Materials discussed experimental results from its new boron oxide ILD planarization process using its PE5000 CVD system in a three-chamber configuration. The process uses trimethylborate and oxygen for depositing boron oxide as a sacrificial planarizing layer over PETEOS oxide films. Boron oxide flows during deposition at wafer temperatures above 450°C. Most of the boron oxide film is etched back in the RIE chamber to form a planarized layer. The remaining boron oxide fills narrow topology gaps to smooth the surface in a manner similar to SOG. A subsequent PETEOS deposition completes the ILD planarization process.

Electron Cyclotron Resonance CVD and Planarization

MIT's Lincoln Laboratories discussed its room temperature electron cyclotron resonance (ECR) deposition and planarization process for oxide films. ECR CVD processes take advantage of the angle-dependent deposition and etchback mechanism that can effectively planarize the device topology. ECR CVD planarization has the following advantages over conventional bias sputtered quartz (BSQ): lower temperatures, better ability to planarize submicron topologies with varying aspect ratios, absence of voids, and higher throughputs due to enhanced ECR ionization efficiencies. A wide range of ILD materials such as oxides, nitrides, and amorphous carbon can be deposited by ECR CVD. Dataquest believes that ECR CVD equipment and processes may find increasing applications in submicron ILD planarization schemes. Multichamber systems may solve the throughput limitation of ECR CVD planarization processes.

SOG Planarization Processes

Research papers on SOG planarization technology were in abundance at VMIC 1989. Both phosphosilicate-based SOG and silanol-based SOG films are being used in multilevel interconnect processes with design rules greater than 1 micron. SOG films are used in combination with CVD oxides for planarization below first-level metal and also between metal levels. Advantages of SOG planarization processes include simplicity, wide process latitude, low temperature process, and good production throughputs. However, for submicron processes, Dataquest believes that SOG planarization has the disadvantages of narrow process latitude and complexity due to multiple deposition and etchback cycles.

Low-Temperature Atmospheric CVD Dielectrics Using TEOS and Ozone

Semiconductor Process Laboratory Co. of Japan described a low-temperature APCVD oxide process using TEOS/ozone chemistry together with organometallic doping sources. The process apparently has the advantages of excellent conformality, low stress, moisture resistance, and low-temperature reflow characteristics. The process was implemented on Canon's new APCVD reactor. Potential applications for these films include DRAM trench refill and ILD planarization. Ozone addition lowers the deposition temperature without lowering the deposition rate.

Toshiba's Composite ILD Using Bias Sputtered Quartz and PECVD Oxide

Toshiba presented a new ILD for double- and triple-metal bipolar and BiCMOS processes using BSQ and PECVD oxide. These sandwich ILD films were found to have good electrical stability and reliability. Toshiba has successfully demonstrated the ILD's use in a BiCMOS test device. Previous BSQ films sustained high defects, severe device degradation, and low throughput limitations.

Toshiba solved these problems by depositing 0.6-micron BSQ film in two steps: 0.1-micron film is deposited with zero bias and is followed by 0.5-micron film deposited with bias. The BSQ film smooths the topology due to its angle-dependent deposition characteristics. Following the BSQ film, Toshiba deposited PECVD oxide and achieved good planarization by reactive ion etchback. Dataquest anticipates that such synergistic processes using BSQ, PECVD, and RIE etchback may be automated in multichamber integrated tools to achieve low defects while maximizing throughputs.

CONTACT AND VIA PLUG TECHNOLOGY TRENDS

Several plug CVD processes that may solve the submicron contact and via metal step coverage problem were presented at VMIC 1989. Plug CVD technology described at the conference included selective and blanket tungsten, aluminum, selective silicide, and polysilicon.

Selective and Blanket Tungsten CVD

Representatives of IBM's T.J. Watson Research Center discussed their experiments on improving tungsten-aluminum interfacial contact resistance in submicron vias between metal levels. IBM performed these experiments in a Genus coldwall batch system. Reactor turret temperatures of 550°C combined with phosphoric-chromic and buffered hydrofluoric acid wet cleans gave the lowest contact resistance for selective tungsten CVD based on silane reduction chemistry. The low contact resistances are attributed to the breakup of the high resistance aluminum fluoride film by intermixing with the selective tungsten CVD.

In the blanket tungsten plug scheme, the CVD tungsten is deposited and etched back to form the plugs. However, the plugs often are recessed below the top of the contact hole due to loading effects and nonuniformity in the etch process. The recessed plugs and exposed contacts can result in poor metal step coverage. Philips Research Laboratories of Eindhoven, the Netherlands, has developed a new process to solve this problem by using a sacrificial PECVD nitride layer. The nitride layer is deposited over the oxide ILD to form a sandwich film prior to contact-hole patterning. Loading effects and plug recession into the contacts are minimized because the fluorine etchant species etches tungsten and nitride at comparable rates after the tungsten in the field areas is cleared.

Sharp Corporation reported that plasma pretreatment with sulfur hexafluoride prior to tungsten deposition is helpful in lowering the contact resistance of selective tungsten plugs to device junctions. The Sharp researchers confirmed that the silane selective tungsten process is preferable over the hydrogen reduction process because of its higher throughput and absence of wormholes and encroachment at the silicon interface. The sulfur hexafluoride plasma treatment etches the silicon surface slightly and enables better tungsten adhesion and electrical stability.

Texas Instruments (TI) presented results from its evaluation of selective tungsten CVD for process control, manufacturability, defect density, and yield. TI used 256K DRAM test wafers and deposited selective CVD tungsten plugs using equipment from three major U.S. vendors. Six recipes representing the best of the hydrogen and silane reduction processes from the three vendors were tested. TI observed that the visual defects did not correlate with the electrical shorts on the wafers. The predominant failure mechanism appeared to be isolated bits of contamination or leakage failures. The contact resistance parameter appeared to be the most strongly degraded due to the selective tungsten process. TI's results indicate that much progress needs to be made before selective tungsten contact plugs are implemented in production. Dataquest believes that selective tungsten may be implemented first as via plugs between metal levels due to its relative process simplicity and the absence of silicon interface reactions that are encountered in contact plugs.

Polysilicon Plug Technology

Polysilicon (poly) plug technology utilizes the advantages of LPCVD poly, such as excellent conformality, good adhesion to oxide, good dry etchability, and good interfacial characteristics, to planarize submicron contacts. Motorola used a composite CVD and sputtered titanium nitride (TiN) barrier in the contacts before depositing polysilicon. The TiN barrier enables good shallow junction integrity, low contact resistance, and reliability. The poly plugs are formed by RIE etchback of the poly film.

In contrast, Sony used the barrier TiN above the poly plug. Sony directly deposited poly in the contacts and etched it back by RIE to form the

plugs. The plugs were doped by separate N+ and P+ ion implants. Rapid thermal processing was used to activate the plug dopants. Sputtered Ti/TiN/Al was deposited and patterned to form the interconnect. Sony reported good electrical characteristics for 0.6-micron contacts using this technology.

Selective Epi Growth and Silicide Plug Technology

Applied Materials and Intel reported a novel silicide plug technology. The scheme combines selective epi growth (SEG) and silicide formation to form silicide contact plugs. Plugs with good planarity and electrical characteristics were reported for 1.1-micron-size contacts. The epi was deposited in an Applied Materials AMC 7810RP reactor. The SEG plug was converted to silicide by rapid thermal processing of sputtered titanium or cobalt films in a nitrogen ambient. Junction leakage and high contact resistance problems remain to be solved before this process can be used in production.

Aluminum CVD Technology

CVD aluminum has the advantages of good step coverage, low resistivity, good interfacial characteristics, and well-characterized patterning ability. ASM International of Bilthoven presented results from its batch, loadlocked hot-wall LPCVD aluminum reactor. ASM was able to achieve growth rates of 200 angstroms per minute at 250°C by tetraisobutylaluminum (TIBA) pyrolysis. ASM claims that its LPCVD aluminum process can be reliably used to form submicron contacts/via plugs and deposit interconnect films sequentially in the same process chamber.

ASM has configured its aluminum LPCVD reactor to be compatible with its Advance 600 series multichamber cluster platform. This platform is capable of integrating vacuum preheat, soft presputter clean, sputter, CVD, and dry etch into an integrated processing tool for interconnect film deposition. The sputter module can be used to deposit barrier films such as TiW and TiN and capping films such as copper-doped aluminum to enhance the interconnect reliability. For a 1-micron aluminum film, ASM claims a throughput of 40 150mm wafers per hour with two batch aluminum CVD reactors attached to the Advance 600 system.

INTERCONNECT FILM TRENDS

Sputtered aluminum alloy films doped with copper, titanium, and silicon are commonly used in multilevel interconnect applications. However, for submicron applications, these films face numerous challenges such as low electromigration resistance, low current-carrying capability, poor step coverage, poor patterning abilities, junction degradation, and silicon nodule formation. Semiconductor companies are exploring a variety of conductor films for improved performance and reliability.

Copper Interconnects for ULSI Applications

Copper's low resistivity and high electromigration resistance makes it an attractive candidate for submicron interconnect applications. However, copper is easily oxidized, difficult to etch, and prone to corrosion. It also affects device characteristics adversely. Hence, copper needs to be coated with a protective skin.

Fujitsu reported a TiN-encapsulated copper interconnect for future ultralarge-scale integration application. The interconnect was formed by sputtering copper-titanium alloy (Cu-Ti) onto a TiN barrier layer. A glue layer of tungsten (W) was used below the barrier for adhesion purposes. The sandwich Cu-Ti/TiN/W film is nitrided at 800°C to encapsulate the outer interconnect skin with TiN. The nitrided copper was etched using ion milling techniques. Fujitsu reported that the nitrided copper interconnect had better oxidation and electromigration resistance compared with pure copper interconnects.

Intel discussed a selective electrodeless wet technique for depositing copper interconnect lines directly on patterned titanium. Advantages of selective electrodeless copper deposition include elimination of the difficult copper etch process, good chemical control of the process, and a low operating temperature of below 80°C. Intel demonstrated 1-micron metal lines and spaces with this process at deposition rates of 1.5 micron per hour using a "homemade" wet solution. Intel used a wet nickel coating technique in an electrodeless bath to encapsulate the copper for preventing corrosion.

Salicide Technology

Intel Corporation presented a comprehensive comparison between titanium silicide ($TiSi_2$) and

cobalt silicide ($CoSi_2$) for self-aligned silicide (salicide) applications. Both silicides were formed by rapid thermal processing in a nitrogen ambient. The film comparisons included parameters such as formation kinetics, process integration issues, and electrical properties. Intel concluded that $CoSi_2$ is a better candidate for the salicide process for the following major reasons: lower lateral encroachment, lower sensitivity to oxygen, higher etch resistance, lower film stress, and better compatibility with submicron shallow junctions. However, Intel cautioned that wafer surface preparation should ensure the complete removal of native oxide from silicon surfaces prior to sputtering the cobalt film.

Excimer Laser Planarization of Sputtered Aluminum Interconnect Films

Sputtered aluminum films have step coverage limitations in submicron applications. Pulsed excimer laser irradiation (xenon chloride laser, 308nm wavelength) is being evaluated as a technique to reflow and planarize sputtered aluminum. During the irradiation, the aluminum melts and reflows due to high surface tension and low viscosity. The underlying device topology is not heated, thus making this technique ideal for ULSI processes with tight thermal budgets. Problems with excimer laser aluminum planarization include excessive local heating and metal evaporation resulting in film ablation and pitting.

Siemens AG reported that aluminum-silicon-titanium (Al-Si-Ti) alloy films are best suited for excimer laser planarization because they can be reflowed without ablation or pitting. Al-Si-Ti alloy films arrest the formation of silicon precipitates that otherwise would absorb excessive radiation and locally melt the film. Excimer laser aluminum planarization processes typically use a barrier metal such as TiW or Ti/TiN to protect the shallow junctions. Semiconductor manufacturers are examining the feasibility of integrating planarization modules such as XMR's Model 7100 excimer laser system with sputtering modules into multichamber cluster tools.

DATAQUEST CONCLUSIONS

VMIC 1989 illustrated the synergistic coupling between multilevel interconnect technology, fabrication equipment, and semiconductor materials. The choice of the optimum interconnect scheme, together with the appropriate processing equipment and materials, will be crucial to cost-effective submicron manufacturing. Semiconductor manufacturers and their equipment and materials vendors will need to forge close strategic relationships in order to develop next-generation multilevel interconnect technologies cooperatively. Dataquest urges its semiconductor industry clients to develop well-defined road maps for submicron manufacturing using the mainstream technology advances from VMIC 1989 reported in this newsletter.

Krishna Shankar

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Research Newsletter

TECHNOLOGY-DRIVEN EXPANSION OF THE CVD EQUIPMENT MARKET

INTRODUCTION

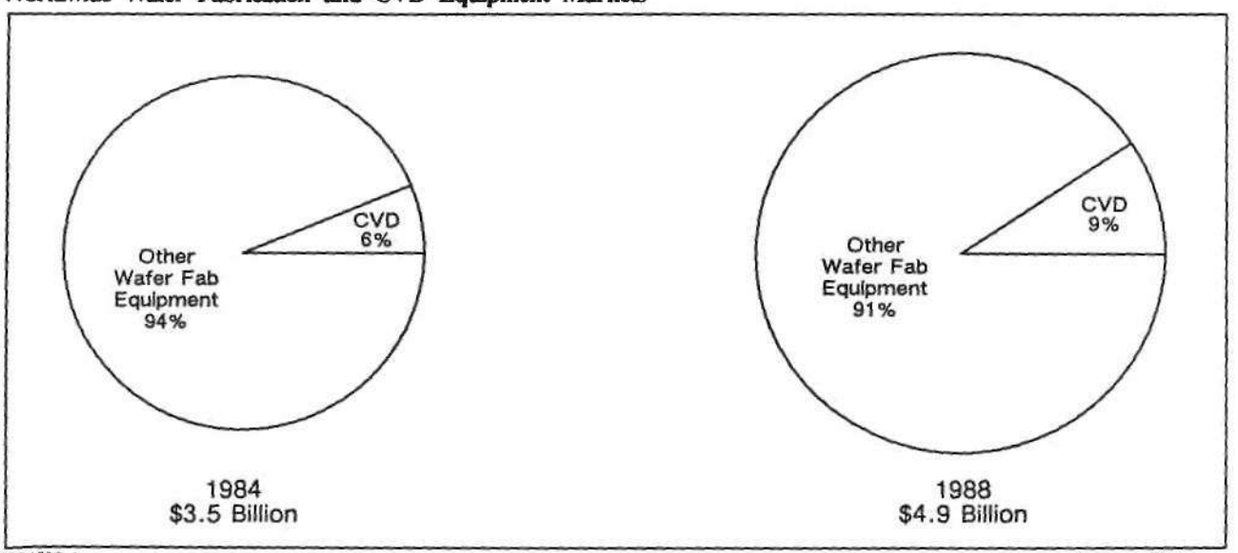
High-quality chemical vapor deposition (CVD) films are becoming increasingly crucial for submicron processes. Fueled by demanding technology requirements, the CVD market grew from $254 million in 1987 to $455 million in 1988—a phenomenal 79 percent increase. Japan, as well as being the largest wafer fab equipment market, now is the largest CVD equipment market, a result of its evolution as an advanced manufacturing powerhouse. However, U.S. CVD equipment companies had the largest share of the worldwide CVD market in 1988 because of their lead in dedicated low-pressure and plasma-enhanced CVD technology.

This newsletter presents an executive-oriented, high-level overview of the worldwide CVD market, competition, products, and applications. This analysis is based on the comprehensive 1988 wafer fab equipment data base of Dataquest's Semiconductor Equipment and Materials Service (SEMS). A more detailed analysis of regional markets, product segments, and technology trends will follow in succeeding newsletters.

WORLD CVD EQUIPMENT MARKET–A BIGGER PIECE OF A BIGGER PIE

Good business conditions in 1988, coupled with the move to submicron processing, prompted semiconductor manufacturers to invest heavily in advanced fabs and equipment. Figure 1 shows the world CVD market growth in relation to the total front-end wafer fabrication equipment market. In 1988, the $455.0 million CVD market made up

FIGURE 1
Worldwide Wafer Fabrication and CVD Equipment Markets



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9 percent of the $4.9 billion wafer-fab equipment market total.

The trend toward three-dimensional 1Mb DRAM cell structures and multilevel interconnect technology for submicron ASICs is driving the CVD market. The tremendous fab capacity expansion for 1Mb DRAMs created a large demand for conformal CVD oxides and low-temperature reflow borophosphosilicate glasses (BPSGs). ASICs with multiple levels of interconnect require production-worthy planarization processes using high-quality interlayer CVD films.

TABLE 1
Regional CVD Markets (Millions of Dollars)

	1987	1988	Percent Growth
United States	$ 92.1	$152.0	65%
Japan	91.4	188.8	107%
Europe	55.3	76.6	39%
ROW	15.6	37.6	141%
World Total	$254.4	$455.0	79%

Source: Dataquest
July 1989

REGIONAL CVD MARKETS–"DRAM"-ATIC GROWTH IN JAPAN AND REST OF WORLD (ROW)

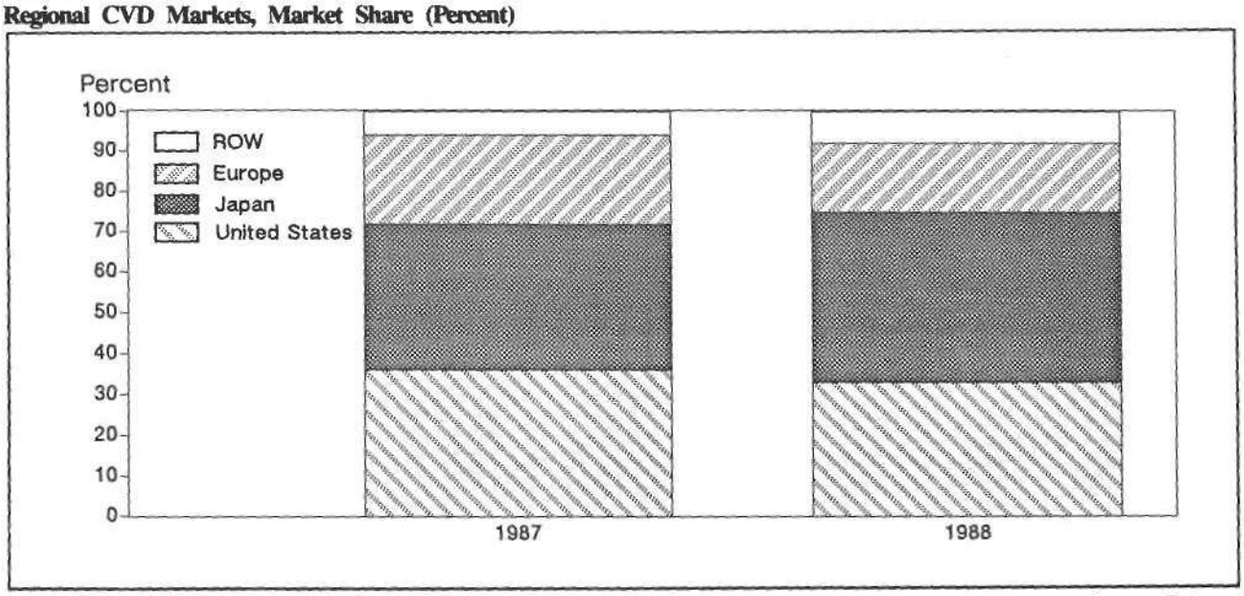
Table 1 displays the regional CVD markets and their growth rates between 1987 and 1988.

Significant 1Mb DRAM capacity expansion caused the Japanese CVD market to more than double during 1988. In their efforts to shrink chip size and improve performance and production yields, second- and third-generation Japanese 1Mb DRAM manufacturers invested heavily in CVD equipment as they migrated from single-level metal planar processes to double-level metal trench or stacked capacitor processes. Also, Japanese semiconductor companies such as Fujitsu, Hitachi, NEC, and Toshiba bought new-generation CVD equipment for ASIC fabs that manufacture sub-micron multilevel gate arrays. Dataquest expects 4Mb DRAM manufacturers to use double-level metal technology widely. Thus, the Japanese CVD market will enlarge substantially with the advent of the 4Mb DRAM.

The ROW CVD market also showed phenomenal growth, more than doubling in 1988. This was mainly because of extensive capital spending for equipping 1Mb DRAM and ASIC fabs in Korea and Taiwan.

Figure 2 presents regional CVD markets for 1987 and 1988 as a percentage of the world CVD market. In 1987, U.S. and Japanese companies each had 36 percent of the world CVD market. In 1988, Japan became the world's largest CVD market with 42 percent, while U.S. share declined to 33 percent of the world market. This trend toward a declining U.S. equipment market and expanding Japanese

FIGURE 2
Regional CVD Markets, Market Share (Percent)



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Source: Dataquest
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and ROW equipment market indicates the Pacific Rim countries' emergence as the regional leaders in semiconductor manufacturing.

TREND TOWARD NONTUBE CVD REACTORS

Figure 3 indicates the shift toward nontube (dedicated) CVD applications from 1984 through 1988.

In 1984, tube CVD was the mainstream dielectric technology, with 54 percent of the $228 million CVD market. By 1988, however, tube CVD had slipped to 37 percent as nontube CVD captured 63 percent of the $455 million world CVD market. For submicron applications, Dataquest expects the trend toward dedicated CVD reactors to continue. Nontube reactors have the advantages of better 6- and 8-inch process uniformity, lower defects, and integrated processing capability for multilayer CVD films.

CVD EQUIPMENT MARKET SHARE: U.S. COMPANIES DOMINATE

Figure 4 shows the worldwide CVD market by regional ownership of CVD equipment companies. U.S companies increased their world CVD market share from 50 percent in 1987 to 58 percent in 1988. Japanese companies maintained 1988 market share at 20 percent, while European companies saw a market share decline, from 31 percent in 1987 to 22 percent in 1988.

CVD is one of the few equipment categories in which U.S. companies have increased 1988 market share, as a result of their lead in developing nontube low pressure CVD (LPCVD) and plasma-enhanced CVD (PECVD) reactors. In contrast, European and Japanese companies dominate the traditional tube CVD market. Nontube reactors are expected to replace tube CVD processes for submicron device applications. Companies that focus on developing nontube CVD reactors for submicron processes will continue to gain market share in the future.

Table 2 lists the top vendors in the tube CVD and nontube CVD market.

In 1988, four of the top five nontube CVD equipment vendors were based in the United States. Applied Materials dominated the nontube CVD area with its successful PE 5000 CVD series. The nontube CVD market is driven by stringent interlayer planarization requirements for submicron multilevel processes.

Watkins-Johnson continued its leadership position in atmospheric CVD applications with its BPSG process for reflow before first-layer metal. Genus was the dominant player in the tungsten and refractory silicide CVD arena, with sales representing 12 percent of the nontube CVD market. The

FIGURE 3
World Markets for Tube and Nontube CVD

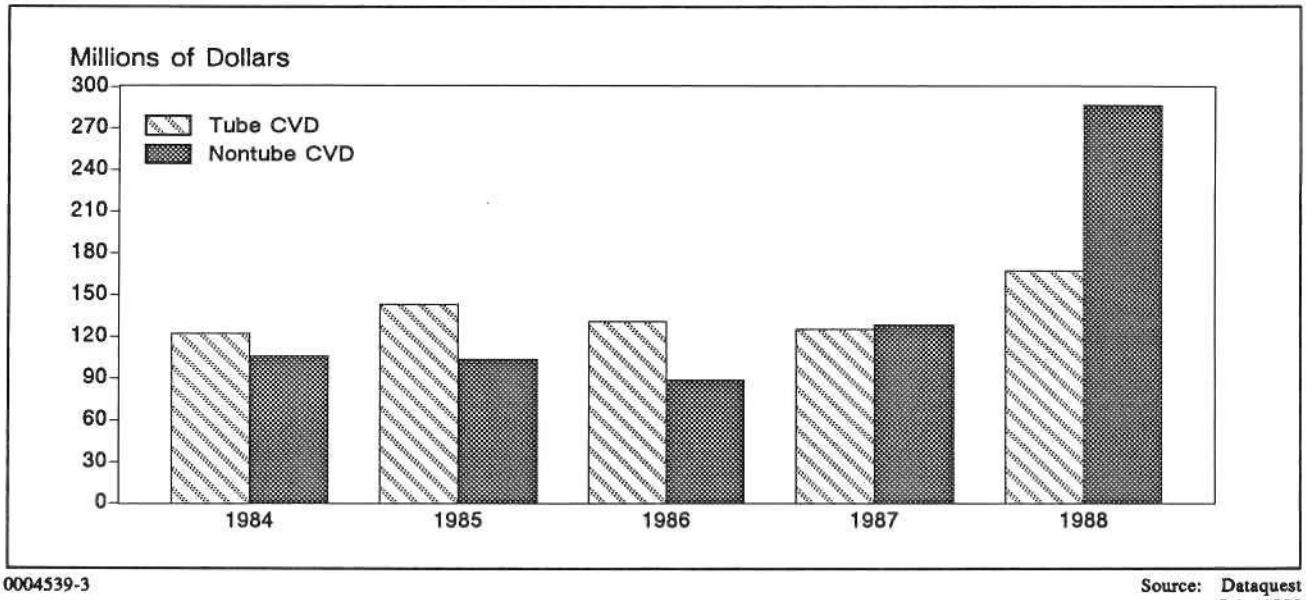

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FIGURE 4
World CVD Market by Regional Ownership of CVD Equipment Companies

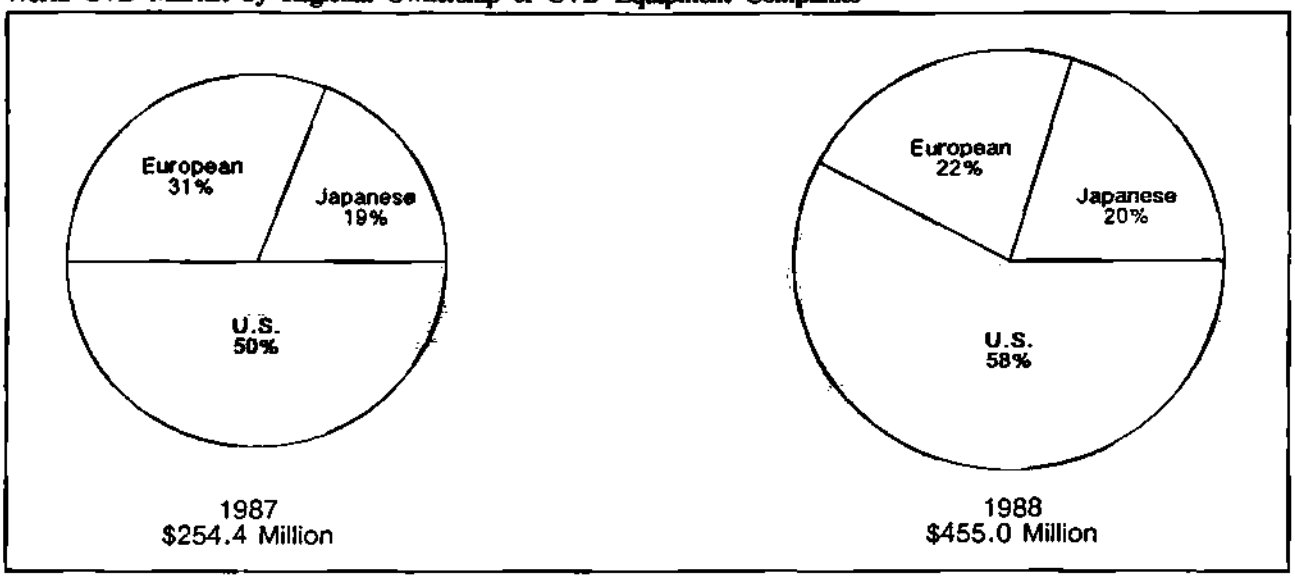

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TABLE 2
1988 Major CVD Equipment Vendor World Sales (Millions of Dollars)

Tube CVD			Nontube CVD		
Company	Sales	Market Share	Company	Sales	Market Share
ASM International	$ 77.4	46%	Applied Materials	$ 91.1	32%
Tokyo Electron Ltd.	16.8	10	Watkins-Johnson	36.0	13
BTU/Bruce	14.5	9	Genus	33.4	12
Kokusai	14.2	8	Novellus	23.7	8
Thermco/SVG	10.1	6	ElectroTech	20.3	7
Others	34.9	21	Others	82.6	28
Total	$167.9	100%	Total	$287.1	100%

Source: Dataquest
July 1989

need for high-performance, high-reliability interconnect technology for submicron applications will drive the tungsten and tungsten silicide CVD market toward vigorous future growth.

ASM International is by far the largest vendor in the tube CVD segment, with sales of $77.4 million representing 46 percent of the total tube CVD market. ASM's tube LPCVD and PECVD products are widely used for interlayer and passivation applications in 1Mb DRAM and ASIC products with 1.0- to 1.2-micron minimum design rules. However, for submicron processes, Dataquest expects dedicated PECVD reactors to be used for dielectric applications. ASM's introduction of its Advance 600 multichamber PECVD system is a recognition of the trend toward integrated CVD processes.

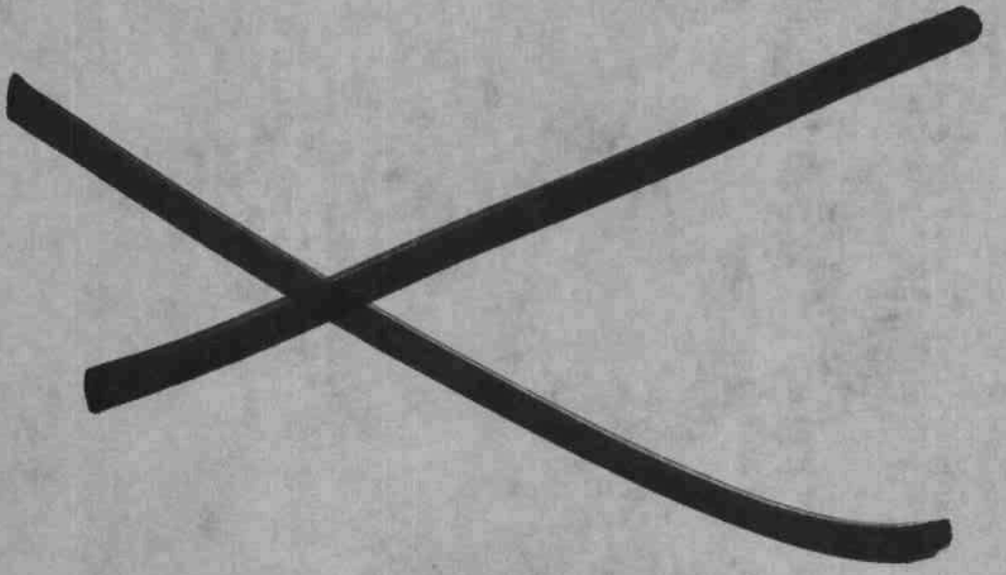
DATAQUEST CONCLUSIONS

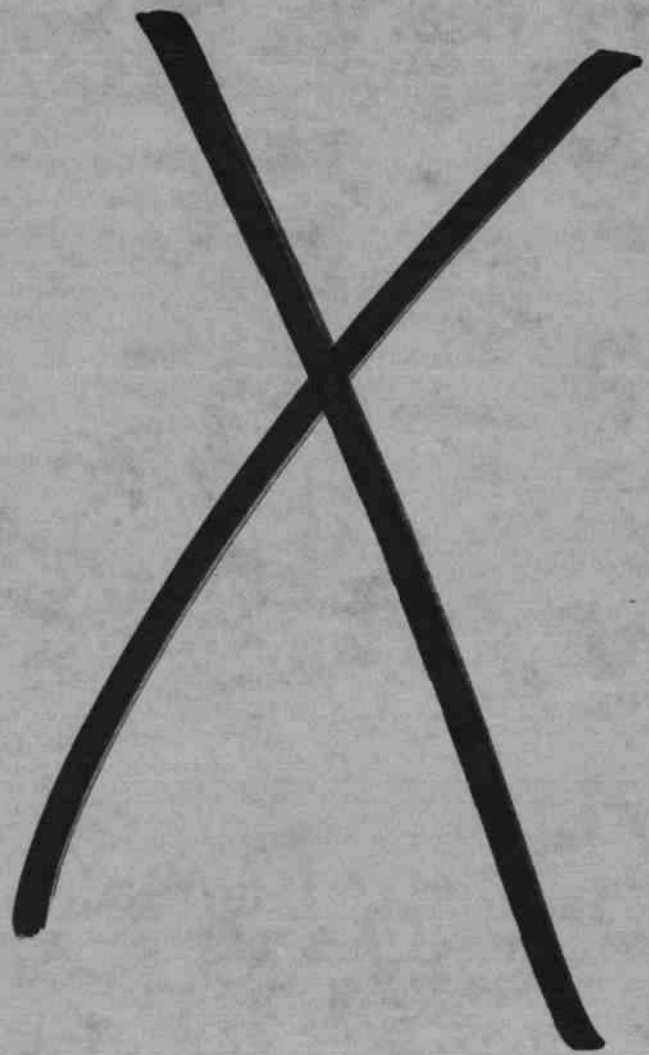
Dataquest believes that the CVD market will continue to gain importance as one of the technology drivers for submicron processing. Three-dimensional DRAM cell structures and ASICs with multiple interconnect levels will catalyze the development of new CVD equipment for demanding dielectric and conductor applications. With the

advantages of low defects and high uniformity, multichamber PECVD systems will continue to gain market share at the expense of traditional tube CVD systems.

Although U.S. companies dominate in selling CVD equipment, their single biggest market is in Japan, which is the leading submicron manufacturing region. CVD market competition will heat up in the next few years as European and Japanese companies challenge the lead of U.S. companies in dedicated CVD reactor technology. Substantial commitments to process development, together with a global, service-oriented presence will be the keys to leadership in the CVD markets of the 1990s.

Krishna Shankar





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CD AND WAFER INSPECTION EQUIPMENT: 1988 WAS A VERY GOOD YEAR

Last year marked robust market growth for optical critical dimension (CD) and wafer inspection equipment. As the world semiconductor industry increased its overall wafer fabrication equipment spending by 55.5 percent, the categories of optical CD, wafer inspection, and joint CD/inspection systems grew at a significantly faster pace of 75.9 percent. These equipment segments benefited not only from the industry's overall capacity expansion but from semiconductor manufacturers' needs for systems with submicron measurement and automated defect detection capability. This newsletter will review the 1988 market, examine the success factors of several companies with strong growth in 1988, profile several new companies and their products, and conclude with a discussion of two recent acquisitions that Dataquest believes signal the beginning of consolidation within this industry segment.

MARKET OVERVIEW

In 1988, the total market for optical CD and wafer inspection equipment was $173.4 million. As shown in Figure 1, the 1988 market for dedicated wafer inspection stations was particularly strong at $71.5 million, up 170.8 percent from its 1987 level of $26.4 million. Also experiencing healthy growth was the optical CD equipment market at $73.8 million, up 74.5 percent from its $42.3 million 1987 level. The market for joint CD/inspection stations was $27.8 million, down slightly from its 1987 level of $29.9 million. Capital spending dollars were readily available in 1988, so semiconductor manufacturers chose to buy systems for dedicated applications rather than invest in equipment with both CD and wafer inspection capability.

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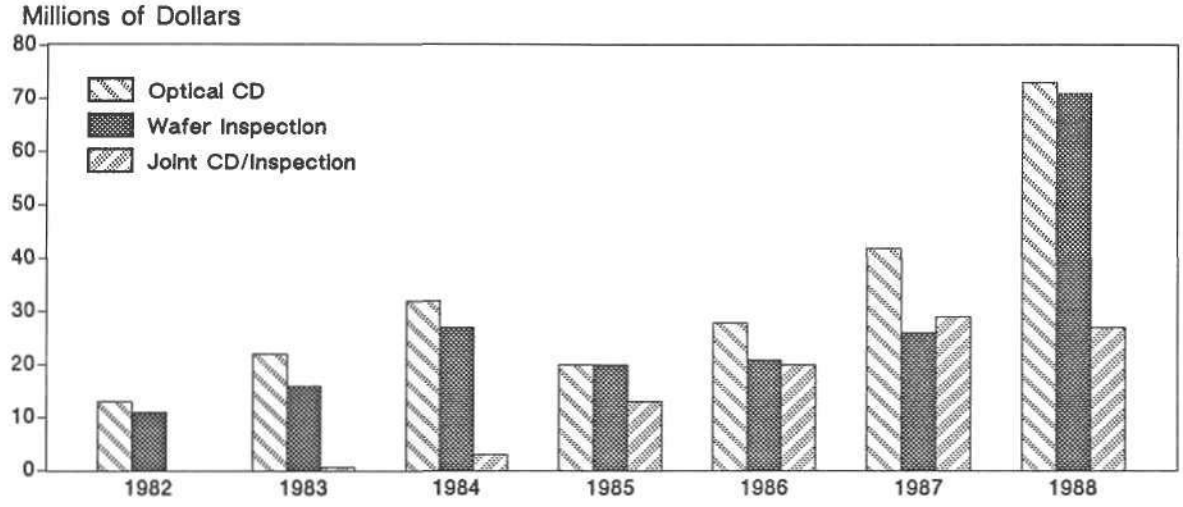
Figure 1

Worldwide Optical CD Equipment, Wafer Inspection Stations, and Joint CD/Inspection Systems Market, 1982–1988



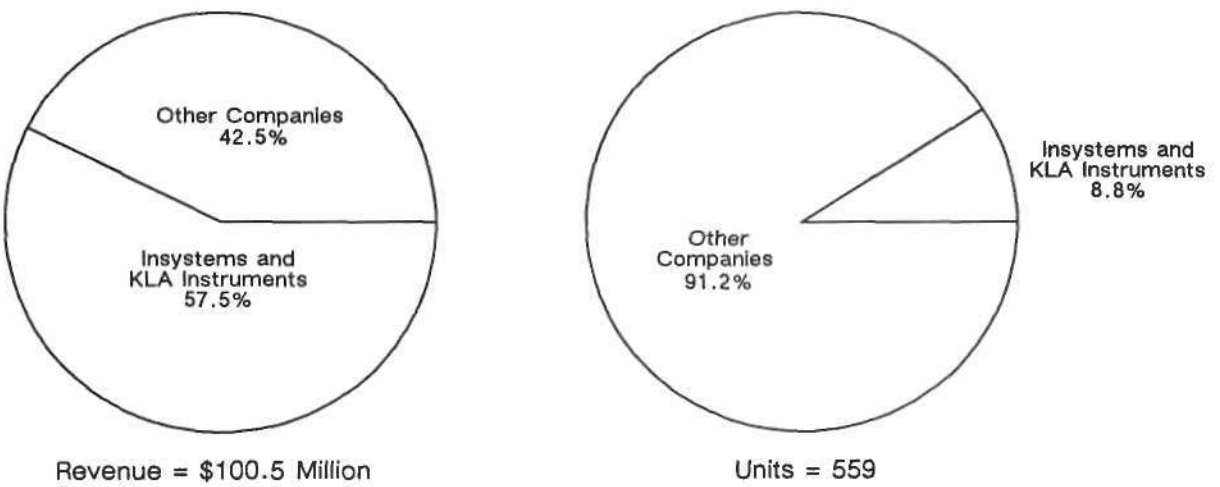
Average Selling Price—Up, Up, and Away

The average selling price (ASP) of optical CD and wafer inspection equipment has risen considerably over the last several years. This increase has been driven by the advent of new measurement and inspection technologies and higher levels of equipment automation. The impact of increasing ASPs on market growth can be illustrated by looking at 1988 revenue and unit estimates. Revenue growth in CD and wafer inspection equipment in 1988 was 75.9 percent. Units grew only 25.5 percent, from 781 systems in 1987 to 980 in 1988. The increase in ASP, however, was a substantial 40.3 percent, from $126,000 in 1987 to $177,000 in 1988. This means that the increase in ASP of CD and wafer inspection systems accounted for 66.7 percent, or two thirds, of total revenue growth in 1988.

Although the overall ASP has been increasing over the last several years, there is still a significant range in the price of CD and wafer inspection equipment. This means that a company with relatively few units that is incorporating advanced technology still can have a strong market presence because the ASP of its equipment is much higher than average. In the wafer inspection and joint CD/inspection equipment categories, there is a significant difference in ASP for systems that rely on an operator to perform visual defect detection (ASP approximately $80,000) compared with systems that automatically detect defects on a wafer (ASP about $1.1 million to $1.2 million). In 1988, only two companies—Insystems and KLA Instruments—provided systems with automated defect detection capability. As shown in Figure 2, their combined sales accounted for almost 60 percent of the market for wafer inspection and joint CD/inspection equipment, while their units accounted for less than 9 percent of total shipments.

Figure 2

Wafer Inspection and Joint CD/Inspection Systems
1988 Revenue and Units



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COMPANY PERFORMANCE—THE SUCCESS STORIES OF 1988

Table 1 presents worldwide sales for companies participating in the optical CD, wafer inspection, and joint CD/inspection equipment markets in 1987 and 1988. Dataquest believes that five companies in particular stand out in the 1988 market environment because of their strong growth and/or dominating market presence. These five companies, in order of 1988 sales, were KLA Instruments, Nikon, Wild Leitz, Insystems, and IVS, Inc. This part of our newsletter will briefly examine some of the factors that contributed to the success of these companies in the 1988 CD and wafer inspection equipment market.

Table 1

Worldwide Company Sales
Optical CD Equipment, Wafer Inspection Stations,
and Joint CD/Inspection Systems, 1987 and 1988
(Millions of Dollars)

	1987	1988
Canon	$ 2.0	$ 3.0
Heidelberg Instruments	1.6	3.4
Hitachi	6.0	1.7
Insystems	2.2	9.8
IVS, Inc.	1.5	6.4
KLA Instruments	27.6	54.2
Nanometrics	1.7	2.3
Nidek	3.1	6.7
Nikon	13.3	29.1
Optical Specialties, Inc.	5.3	4.8
Perkin-Elmer	0	2.9
Ryokosha	1.4	2.5
SiSCAN Systems	3.0	4.9
Vickers Instruments	8.3	9.0
Wild Leitz	11.1	20.2
Zeiss	1.8	1.8
Other Companies	8.7	10.7
Total	$98.6	$173.4
Percent of Growth	39.3%	75.9%

Source: Dataquest
July 1989

KLA Instruments

KLA dominated the CD and wafer inspection equipment market with a 31.3 percent market share in 1988. The company's strength in this equipment segment relies on several factors, including a diverse product line, innovative technology, and a strong presence in all regional markets. In particular, KLA is one of relatively few U.S. companies to be successful in Japan. This region accounted for 36.7 percent of KLA's 1988 CD and wafer inspection equipment sales.

Most important has been the company's ability to provide systems with automated defect detection capability. KLA pioneered this technology and introduced the industry's first automated defect detection system, the KLA-2020, in 1984. The year 1988 marked the first year of sales for KLA's dedicated wafer inspection station, the 2028, as well as for its new joint CD/inspection system, the 2030. In addition to inspection systems, KLA offered two products in the area of optical CD measurement in 1988: the KLA-2005, a high-throughput system that is a metrology-only version of the 2020; and the recently introduced KLA-5000, which relies on a proprietary submicron measurement technology known as coherence probe imaging that was developed by KLA.

Nikon

Nikon was the second-largest supplier of optical CD and wafer inspection equipment in 1988, with 16.8 percent of the market. Nikon's success in this equipment segment in 1988 was tied to its strong presence in its home market, Japan, which represented almost 75 percent of its total optical CD and wafer inspection sales. Nikon manufactures a fully automated, laser-source CD measurement system, the LAMPAS-HD. This tool alone accounted for an approximately 58 percent share of the Japanese optical CD equipment market in 1988. The company also manufactures the Optistation family of wafer inspection systems. These systems represented approximately 30 percent of the Japanese market for wafer inspection equipment and almost 50 percent of unit shipments. In 1988, Nikon's sales of optical CD and wafer inspection equipment were almost evenly split between these two categories of equipment. Dataquest believes that the company's reputation as a manufacturer of optical components, as well as its dominance of the stepper lithography market, also contributed to its success in the optical CD and wafer inspection markets.

Wild Leitz

Wild Leitz, with 11.6 percent of the market, ranked third after KLA and Nikon in the 1988 world optical CD and wafer inspection equipment market. Wild Leitz's strength in this market segment was based in part on a strong regional presence in both Europe and the United States, which accounted for 50.5 percent and 43.6 percent, respectively, of its 1988 sales. Wild Leitz provides a diverse product line, including optical CD equipment (based on its MPV-CD-2 product offering) and wafer inspection stations (the LTS and LIS systems). Like Nikon, the company's 1988 worldwide sales were almost evenly split between optical CD and wafer inspection equipment. Dataquest believes that Wild Leitz's product line and broad regional presence, as well as its ability to manufacture its own optical components, continues to contribute to its success in the optical CD and wafer inspection equipment markets.

Insystems

Insystems experienced a more than fourfold increase in sales in 1988. The company manufactures a fully automated, full-wafer, defect detection system that utilizes holography and spatial frequency filtering technology. The system's success is tied to its innovative technology for automated defect detection. The Model 8600 can inspect the entire surface of a patterned wafer for defects in less than 30 minutes. This should be compared with the several hours required for inspection by conventional optical- or SEM-based inspection tools. This reduction in measurement time is accomplished because the Model 8600 relies on parallel optical processing rather than a serial analysis of the wafer on a die-by-die basis. In 1988, the company had sales in both the United States and Japan.

IVS, Inc.

Like Insystems, IVS experienced a more than fourfold increase in sales in 1988. This small U.S. company manufactures an automated CD measurement system, the Accuvision–4, that incorporates digital image processing, proprietary software algorithms, and an optical microscope system to provide submicron measurement capability. IVS's sales activity was focused on the U.S. market in 1988. That regional focus, along with a gain in the acceptance of its technology, provided the company with an increase in U.S. market share from 8.8 percent in 1987 to 19.2 percent in 1988.

Confocal Technology—Still A Question

One area of advanced CD measurement equipment that has yet to experience any significant growth is confocal scanning laser microscopy (CSLM). Only two companies—Heidelberg Instruments and SiSCAN Systems—currently are providing automated CD measurement tools based on CSLM technology. While the combined sales of these two companies represented 10.9 percent of the 1987 world optical CD market, this figure grew only slightly in 1988 to 11.2 percent.

Much attention and expectation has been directed toward CSLM systems because of their ability to provide submicron measurement capability as well as z–axis profilometry. This technology, however, has developed at a slower pace than was originally expected. Factors that slowed development were a change in laser sources from argon ion (488nm) to helium cadmium (325nm), and the subsequent work required to recharacterize the system's measurement performance. A 325nm source reduces the amount of reflected and scattered light that makes linewidth measurement more difficult at 488nm. This is because many photoresists have lower transmission profiles at shorter wavelengths and, thus, appear more opaque at 325nm than at 488nm. Therefore, interference effects will be attenuated significantly with a 325nm source. In addition, helium cadmium's shorter wavelength offers several other advantages over 488nm illumination, including improved resolution and depth of focus. Both Heidelberg and SiSCAN originally developed their systems with argon ion laser sources (488nm), but SiSCAN has since moved exclusively to a helium cadmium laser source (325nm), while Heidelberg now offers both helium cadmium and argon ion sources.

NEW PLAYERS ENTER THE GAME

In the last 12 to 18 months, three new companies have entered the optical CD and wafer inspection equipment market. This part of our newsletter briefly examines the new products being offered by these companies.

Micro–Controle

At SEMICON/Europa in March 1989, Micro–Controle of France introduced its new Automatic Linewidth and Registration Measurement (ALARM) system and its new Imaging Defect Inspection System (IDIS). Historically, the company's business activities have been focused on precision positioning devices such as micrometers and air–bearing tables. In 1982, Micro–Controle decided to diversify into the semiconductor industry. The ALARM and IDIS products represent Micro–Controle's entry into the front–end semiconductor equipment market.

The ALARM system is an optical CD measurement tool with minimum linewidth measurement capability down to 0.5-micron, 10-nanometer (3 sigma) precision for thick film patterns. System throughput for linewidth measurement is reported to be 60 wafers per hour at five sites per wafer, two measurements per site. This is significantly faster than the standard 25 wafers per hour for most other optical CD systems. The company believes that its fast and accurate stage contributes to this impressive throughput rate.

The IDIS wafer inspection system uses image processing and software algorithms to detect wafer defects on a die-to-die basis. The company hopes to introduce die-to-data base inspection capability by the end of 1989. The IDIS system can be purchased as a separate system or as part of the ALARM. The ALARM is priced between $550,000 and $650,000, while the IDIS is priced at $300,000. A joint CD/inspection version of the ALARM and IDIS systems is priced at approximately $900,000. System shipments began in March 1989 to European customers, while U.S. customers are expected to take delivery later this year.

Olympus

Olympus entered the wafer inspection equipment market when it announced its Cue 2000 Wafer Inspection Station at SEMICON/West in 1988. The Cue 2000 utilizes image recognition software and a user-defined defect library to perform operatorless defect inspection based on the automatic identification of 15 different defect types. Since the defect types are preprogrammed, the Cue 2000 can, in a sense, perform both automatic defect detection and classification. Olympus, a major Japanese manufacturer of optical components, undertook all system development for the Cue 2000 in the United States. Although Olympus has been a long-time supplier of standalone microscope products to the semiconductor industry, the Cue 2000 is the company's first systems-level offering for the semiconductor production environment. The Cue 2000, currently in beta site, is expected to be available by the end of 1989 and will be priced at approximately $150,000.

Perkin-Elmer

Perkin-Elmer introduced the OMS 1 Overlay Measurement System at SEMICON/West in May 1987. This system provides fast, precise overlay measurements that are used to optimize the performance of the company's Micralign and Micrastep lithography tools. At SEMICON/Europa 1989, the company exhibited the OMS 10, which incorporates a wafer-handling robot, a wafer prealigner, and dedicated electronics into the existing OMS 1 system. Perkin-Elmer had sales of $2.9 million for the OMS in 1988, its first year of sales. The ASP of the system is approximately $180,000. The recent announcement of Perkin-Elmer's plan to sell its semiconductor division has created some uncertainty regarding this product's future, as well as that of other semiconductor equipment manufactured by the company.

RECENT ACQUISITIONS

Wild Leitz Steps In to Buy Heidelberg's Technology

In January 1989, Wild Leitz acquired Heidelberg Instruments' laser scanning technology and linewidth measurement equipment business and established a new wholly owned subsidiary, Wild Leitz Instruments. Wild Leitz, formerly an investor in Heidelberg Instruments, states that the new company will be concerned exclusively with laser scanning technology and will focus on applications in semiconductor technology, as well as in life and material sciences.

Wild Leitz has been a major supplier of optical CD and wafer inspection equipment since the early 1980s, and ranked third overall in the 1988 market. The company's traditional optical CD measurement systems rely on reflective white light microscopy, which is limited in its ability to measure device features in the submicron processing regime. The acquisition of Heidelberg's laser technology allows Wild Leitz to complement its existing product line with an advanced submicron measurement system. The new subsidiary benefits from a large corporate parent that is dedicated to expanding its semiconductor markets, able to provide an extensive sales and support network, and better able to support the necessary capital investment that will be necessary for next-generation technology development.

After the acquisition, Heidelberg Instruments still remains as a separate company. It is involved in the development of an automatic wafer inspection system for the semiconductor industry. In addition, the company has developed a laser tomography system for opthamalic applications.

Bio-Rad Acquires Vickers Instruments

In January 1989, Bio-Rad Laboratories acquired Vickers Instruments, the English-based manufacturer of optical and electron beam metrology equipment. (The acquisition also included the Canadian and U.S. operations of Vickers Instruments.) Bio-Rad is a leader in life sciences research products, clinical diagnostics, and analytical instruments. The acquisition of Vickers Instruments provides Bio-Rad with an entry into the front-end semiconductor manufacturing environment with a well-established vendor. Vickers Instruments' optical CD system, the Quaestor CD-07A, placed first in Dataquest's 1987 company rankings in optical CD equipment, with sales of $8.3 million. To complement its optical-based CD measurement equipment, Vickers Instruments also manufactures the Nanolab SR, a SEM-based metrology tool for the semiconductor production environment.

Dataquest believes that Vickers Instruments also will benefit from this acquisition. Its new corporate parent is interested in increasing its presence in the semiconductor industry and has the ability to support Vickers Instruments in its future development of advanced measurement systems. As part of the acquisition, Vickers Instruments (formerly part of Vickers plc) has been renamed Nanoquest, Ltd.

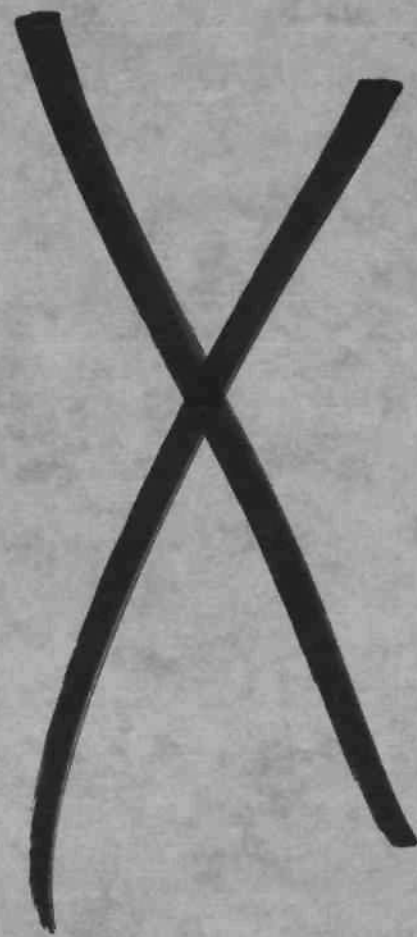
DATAQUEST ANALYSIS

Although the worldwide optical CD, wafer inspection, and joint CD/inspection equipment markets experienced healthy growth in 1988, not all companies participated in the market expansion to the same extent. A handful of companies enjoyed strong growth and/or dominating market presence. These companies were successful for several reasons, including having diverse product lines, advanced technology, and strong presence in one or more regions of the world. However, Dataquest believes that the success of a company in optical CD and wafer inspection will be more and more dependent on its ability to provide advanced technology for submicron measurement and automatic defect detection. This in turn is tied directly to the company's ability to generate a sufficient income stream from its existing products to fund such technology development; such next-generation technology developments are not cheap. At the same time, the number of companies capable of maintaining the flow of R&D dollars continues to shrink. Although several companies recently have entered the market, Dataquest believes that the two recent acquisitions have far more significance. We believe that these acquisitions signal the beginning of consolidation within this part of the industry.

For many companies, consolidation may be the only path available to reach the critical mass required to fund technology development and to support an increasingly demanding client base. While several larger players with diverse product lines already are well positioned, small companies with one or relatively few products and an income trickle rather than a stream have relatively few alternatives to obtain a source of R&D funds, other than being acquired.

One alternative is to turn to the venture capital community. However, this group of investors is becoming increasingly reluctant to participate in the semiconductor equipment industry. Another alternative would be to establish an alliance between a small vendor and a large corporation as an investment partner. This type of partner, while probably more difficult to find, may be more patient than the venture capitalist in waiting for the return on its investment. One final scenario for survival may be for several smaller companies with complementary products and technologies to merge, in a sense creating a "super" metrology and inspection company. Dataquest believes that whatever scenario evolves, the reality is that the shakeout of the optical CD and wafer inspection equipment markets has begun.

Peggy Marie Wood



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Research Newsletter

TUNGSTEN HEXAFLUORIDE: A MARKET IN TRANSITION

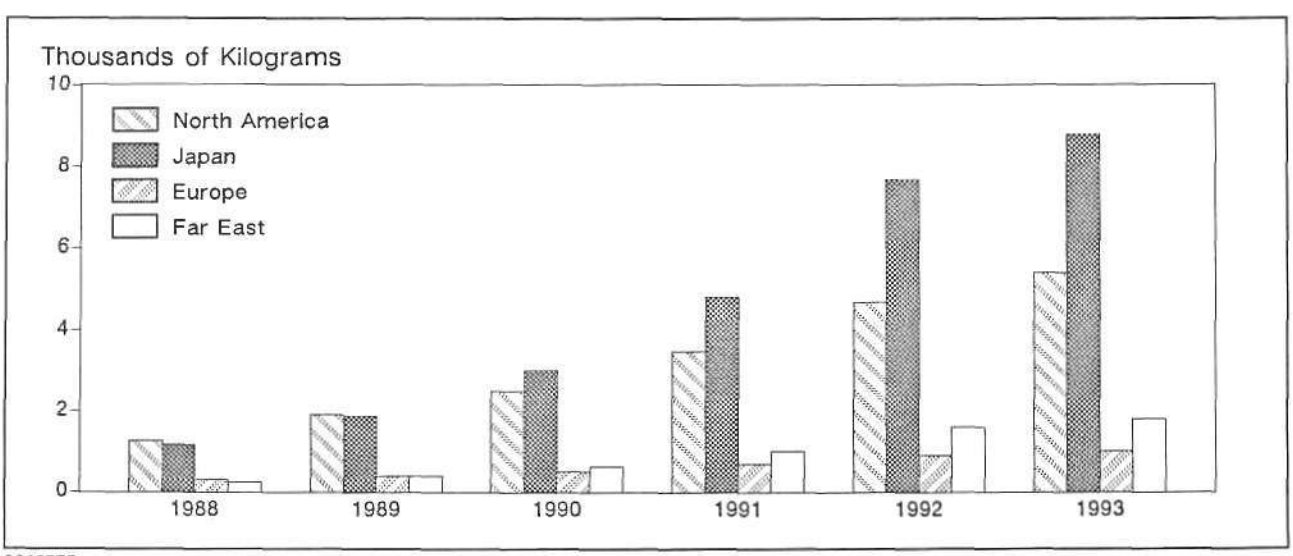
The market for high-purity tungsten hexafluoride (WF_6) used in silicide, blanket, and selective tungsten applications is moving into a transitional period. It can be characterized by a strong expansion in demand coupled with falling prices in most regional markets.

DEMAND

The growth in demand, which Dataquest forecasts at 39.1 percent compound annual growth rate (CAGR) through 1993, will be spurred on by the use of the blanket tungsten process to increase device density in 4Mb and 16Mb DRAMs. Until now, silicides of tungsten used as high-conductivity, low-resistance interconnect materials have been the primary driving application for WF_6 demand. This usage is a low-volume WF_6 consumer compared with the blanket application.

We expect the demand to be especially strong in Japan, South Korea, and Taiwan because of the emphasis on DRAM manufacturing in these regions. In fact, the Far East and Japan are forecast to account for 60 percent of the worldwide consumption by 1993. We believe that demand in Europe and North America will be strong, but will grow at one-half the rate of Japan and the Far East. Figure 1 shows the regional WF_6 demand forecast for 1988 through 1993.

FIGURE 1
Regional WF_6 Demand Forecast



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PRICE

The pricing pressures for WF_6 are due to the worldwide capacity that suppliers are installing and the strategy of new suppliers to cut prices in order to earn market share. (See Table 1 for a list of WF_6 manufacturers by region.) The current installed capacity is estimated to be 40,000 to 50,000 kilograms, while the current demand is 4,500 kilograms or roughly one-tenth of production capacity.

This overcapacity is most pronounced in Japan, which has four primary manufacturers serving a market that is roughly the same size as the U.S. market. The result is that the average selling price for WF_6 has fallen to ¥60,000/kilogram in Japan. The U.S. market has three suppliers, with a fourth expected to enter in the near future. Prices in North America have drifted lower over the past two years and currently are in the $1,100/kilogram range.

Prices in Japan are expected to stay relatively stable as demand grows because of the growing blanket process requirements. In the North American market, prices are expected to fall further as the two market share leaders, Airco and Air Products, come under pressure from recent entrants to the market. Pricing in the Far East and Europe are expected to trend lower, but not as quickly as the other regional markets because of the lack of local competition.

HISTORY

The tungsten process was pioneered by Genus Corporation as a solution to the reliability issues surrounding aluminum in sub-1.5-micron production. When the company was founded in 1983, there were no commercial sources of WF_6 that met the stringent purity requirements for semiconductor manufacturing. Consequently, Genus was forced to set up a materials division to purify the low-grade tungsten hexafluoride that was available commercially.

Genus supplied strong application support for the product from its introduction and tied the end users to Genus with an equipment guarantee that was contingent on the use of Genus' WF_6. The price of $2,645/kilogram reflected the company's sole-source position and its market development cost for setting up the materials division.

The market price for Genus-grade WF_6 inevitably attracted the attention of large industrial gas and chemical companies, which were the primary manufacturers of the material in the United States, Japan, and France. Since 1986, these companies have added columns to clean up their low-grade WF_6 streams and equipment to analyze the high-purity product. In addition, they have installed high-purity cylinder facilities to package the material.

As each new vendor has entered the market, their strategy for penetrating the market has been to undercut price in order to grab market share. The resultant price erosion has occurred more quickly in Japan, where the competition among suppliers has been more fierce. However, the same market dynamics are at work in the United States and are expected to spread to Europe and the Far East.

TABLE 1
Primary Manufacturers of WF_6 by Region

Japan	North America	Europe
Asahi Glass	Air Products	L'Air Liquide
Central Glass	Airco (BOC)	
Kanto Denka	Bandgap (Amax)	
Mitsui Toatsu		

Source: Dataquest
December 1989

DATAQUEST CONCLUSIONS

These trends of lower material cost and growing production capacity firmly establish tungsten CVD films as the refractory metal of choice to supplement sputtered aluminum for primary metallization processing in VLSI manufacturing. Consequently, as more semiconductor manufacturers move the blanket tungsten process to production, they will have a reasonably priced, stable supply of WF_6.

We foresee that WF_6 vendors can expect very strong growth in volume demand. Although margins will be lower, the growth in demand will more than compensate both on a total revenue and profit basis. Moreover, strong demand in the Far East, which has no regional production, should provide a strategic opportunity for Japanese and U.S. suppliers.

Mark FitzGerald

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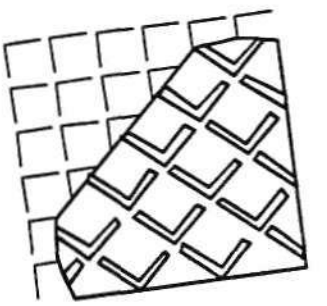


SILICON WAFERS: EXISTING MARKETS AND FUTURE OPPORTUNITIES

PEGGY MARIE WOOD, Ph.D.
Industry Analyst
Semiconductor Equipment and Materials Service
Dataquest Incorporated

At Dataquest's SEMICON/West Annual Seminar on May 24, SEMS Industry Analyst Peggy Wood gave a presentation on the silicon wafer industry. Her speech covered the existing merchant silicon and epitaxial wafer market and the emerging market segment of silicon–on–insulator materials.

EXISTING MARKETS -- SILICON AND EPITAXIAL WAFERS

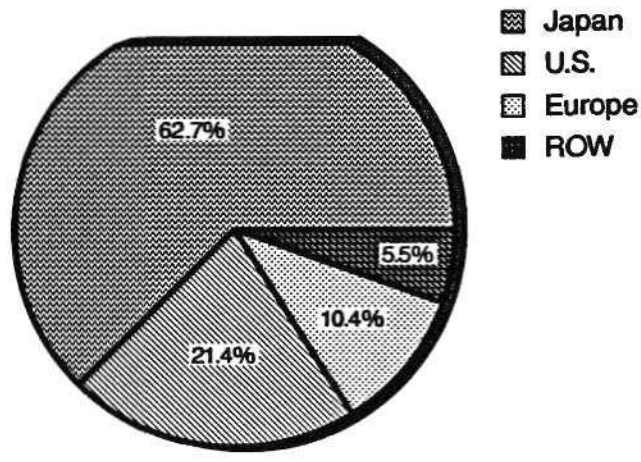
Agenda

- Market overview
- Wafer pricing update
- Looking ahead at 8"
- Acquisitions revisited

Key points to note:

- This is the agenda slide for the first half of the presentation. This portion focuses on the $2.16 billion silicon and epitaxial wafer market in 1988.

1988 MERCHANT SILICON AND EPITAXIAL WAFER MARKET BY REGION



Total = $2.16 Billion

Source: Dataquest

Key points to note:

- At first glance, it may seem that the U.S. market, at approximately $460 million or 21 percent, is unusually small relative to the Japanese market, which accounted for approximately $1.35 billion, or 62.7 percent of the world merchant market.

- Several factors account for this apparent difference:

  - Japan is the largest wafer market in the world, measured not only on a revenue basis but also on a unit basis of million square inches.

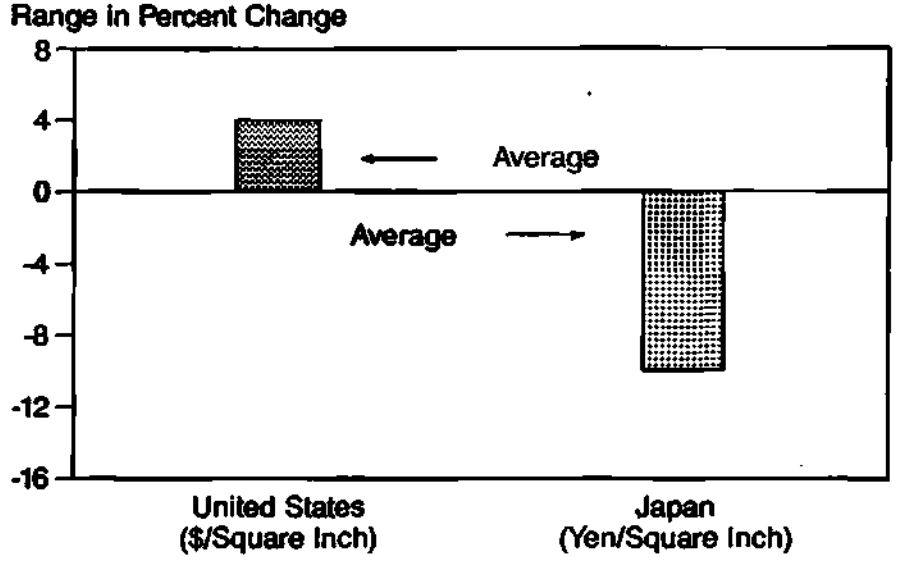
  - There has been significant yen appreciation during the last several years. Since the Japanese wafer suppliers dominate their home market, currency appreciation has affected the size of the Japanese market substantially when measured on a dollar revenue basis.

  - Several semiconductor manufacturers in the United States have internal captive silicon production that is not reflected in our estimates of the merchant wafer market.

- The merchant silicon and epitaxial wafer industry of $2.16 billion corresponded to approximately 1.43 billion square inches. An additional 130 million square inches of captive silicon production brings total world silicon consumption to 1.56 billion square inches in 1988.

WAFER PRICING UPDATE

Polished CZ Wafers



Source: Dataquest

Key points to note:

- During the healthy market environment of 1988, merchant silicon companies experienced some relief from the downward pricing pressures of previous years.
- In the United States, the increase in the average selling prices (ASPs) of polished Czochralski (CZ) wafers ranged from flat to 4 percent growth in dollar-per-square-inch prices from their 1987 levels. The amount of increase was dependent on wafer size. The overall average increase was approximately 3 percent.
- In contrast with the United States, the ASPs for polished CZ wafers in Japan generally ranged from flat to a negative 10 percent on a yen-per-square-inch basis relative to their 1987 levels. This also was dependent on wafer size. The overall average decline, however, was only 2 to 3 percent—a decided improvement compared with the 6 to 10 percent price declines of earlier years.
- Unlike the competitive and customer-induced pricing pressures on mature wafer products, we expect wafer prices for 8-inch wafers to continue to decline during the next several years as 8-inch wafers move from being curiosities to becoming mainstream products.

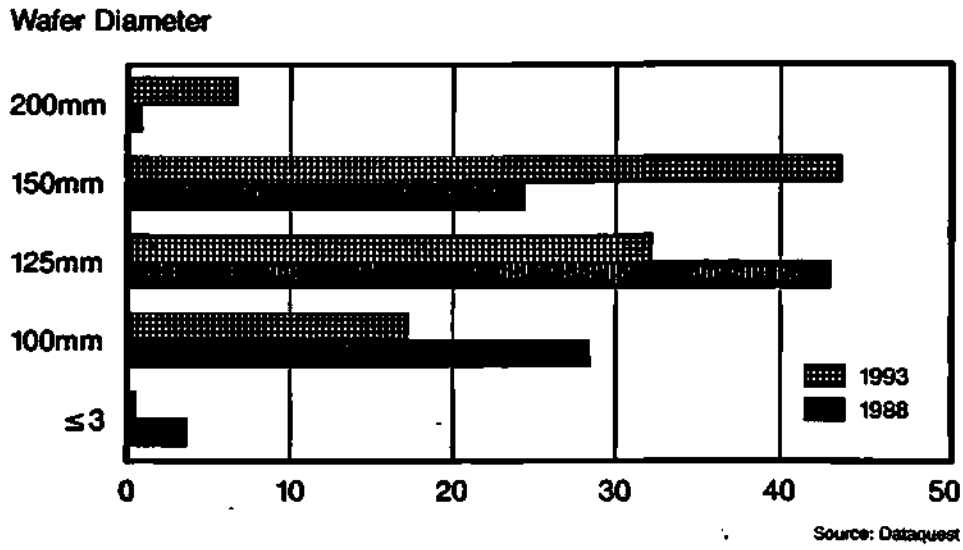
LOOKING AHEAD TO 8"

- 8" fab activity
- Wafer size forecast

Key points to note:

- Clearly, 8–inch fab activities are fueling the demand for 8–inch wafers. In another SEMICON/West talk, SEMS Industry Analyst Mark Reagan reviewed a number of new 8–inch fabs we expect to come on line during the next five years.
- The products we expect to be targeted for 8–inch wafer production in these new fabs are 1M and 4M DRAMs.
- Manufacturing focused on the high–volume commodity products is particularly well–suited for 8–inch wafer processing because of the significant increase in size. One 8–inch wafer has almost twice the area of a 6–inch wafer and approximately four times the area of a 4–inch wafer.

WORLDWIDE WAFER SIZE DEMAND



Key points to note:

- This slide illustrates the worldwide silicon wafer demand in 1988 by wafer size and Dataquest's forecast for 1993. Please keep in mind that this wafer size distribution is measured on the basis of percent million square inches.

- In 1988, 5-inch (125mm) wafers dominated the world's wafer size distribution, representing approximately 43 percent of all square inches. In 1993, we expect the positioning between 5- and 6-inch (150mm) wafers to essentially switch, with 6-inch wafers representing the major share of the size distribution.

- Even with all of the new 8-inch (200mm) fab activity coming on-line, we still expect 8-inch wafers to represent approximately 6.5 percent of the square inch distribution in 1993. Using the conversion factor between square inches and wafer slices, 8-inch wafers drop to approximately 3.5 percent of the actual number of wafers to be processed through the world's fab lines in 1993.

SILICON ACQUISITIONS REVISITED

Year	Company		Acquired By
1988	Monsanto Electonic Materials Company	←	Huels AG
1988	Cincinnati Milacron	←	Osaka Titanium Company
1987	Dynamit Nobel Silicon	←	Huels AG
1986	U.S. Semiconductor	←	Osaka Titanium Company
1986	Siltec Corporation	←	Mitsubishi Metal
1985	NBK Corporation	←	Kawasaki Steel

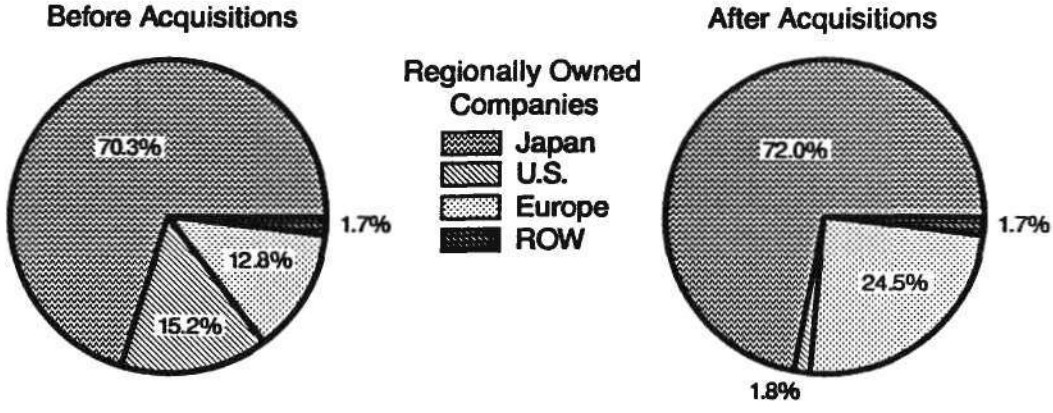
Source: Dataquest

Key points to note:

- In early 1989, Osaka Titanium's acquisition of Cincinnati Milacron and Huels AG's acquisition of Monsanto's wafer operations were finalized. These two acquisitions represent the latest in a series of acquisitions in the silicon wafer industry spanning the last four years.

SHIFTING SHARE
IMPACT OF RECENT ACQUISITIONS

1988 = $2.16 Billion



Source: Dataquest

Key points to note:

- These two acquisitions have significant impact on the world market share of U.S.–based silicon suppliers by reducing their share to less than 2 percent of the world market.

- Interestingly enough, we now are observing the emergence of a domestic silicon supplier base in Asia/Pacific (Rest of World), most notably in Korea. Dataquest anticipates that this year, the Asia/Pacific silicon suppliers will surpass their U.S. counterparts in the sale of merchant wafers.

- Based on our 1988 estimates, Monsanto's acquisition by Huels AG boosts European supplier share from about 13 percent to almost 25 percent. In particular, Huels AG now emerges as the second–largest merchant silicon supplier in the world after SEH of Japan. This is a particularly interesting distinction, considering that it was just two years ago that Huels AG first entered the silicon wafer industry.

Summary (first half)

- The world's silicon wafer industry was an active participant in the robust market environment of 1988.
- Million-square-inch consumption of wafers increased 15 percent over 1987 levels. At the same time, relief in wafer pricing pressures provided some assistance in the return to profitability for several silicon companies.
- The merchant wafer industry continues to be an extremely competitive market, and as with any mature industry, consolidation through acquisitions has been one of the major growth strategies adopted in recent years.

FUTURE OPPORTUNITIES -- SILICON ON INSULATOR

Agenda

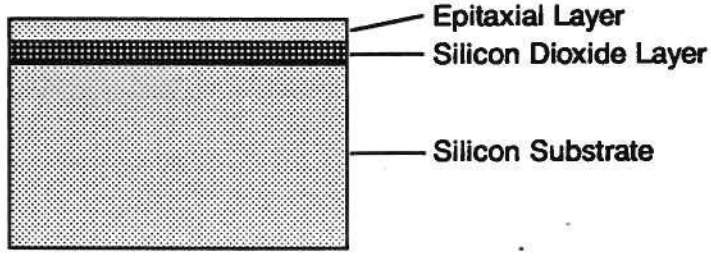
- Advantages and applications
- SOI suppliers
- Technology overview
- Outlook

Key points to note:

- This is the agenda slide for the second half of the presentation. It focuses on the emerging market of silicon–on–insulator (SOI) wafers. During the past 12 to 18 months, we have observed several new start–up companies pursuing opportunities in this market niche.

WHAT IS SOI?

SOI (silicon on insulator) wafers consist of a thin epitaxial layer of silicon on an insulating layer of silicon dioxide over a silicon substrate.



Key points to note:

- What exactly is SOI?
- SOI is a generic term for single-crystal silicon over any insulating material—oxide or otherwise. Most people in the industry are familiar with another SOI technology, known as SOS (silicon on sapphire).
- SOS was the process that RCA developed in the 1960s and 1970s for high-speed and rad-hard applications. However, problems inherent with SOS processing have led to the development of an alternative SOI technology based on silicon dioxide as the insulating material. This material will be the focus of the remainder of this presentation.

SOI ADVANTAGES

- High packing density/freedom from latch-up
- High-speed operation
- Inherent radiation hardness
- High-temperature operation
- High-voltage capability
- Standard silicon processing

Key points to note:

- The simplest reason for these many advantages is that the active device area is built in a very thin layer of single-crystal silicon, which in turn, is isolated from interactions with the bulk silicon substrate by the insulating oxide layer.
- With SOI, CMOS devices may be packed more closely, because there is no need to devote silicon real estate to the insulating oxide trenches now used to prevent parasitic latchup between nearby devices.
- According to one supplier, the properties of SOI wafers allow for devices to be fabricated with a 30 percent improvement in density and a twofold increase in speed without a decrease in device geometry.
- The radiation hardness of SOI devices probably has been the most important driving force in the development of the technology. Although gallium arsenide historically has been the material of choice for rad-hard military applications, the inability to boost circuit densities and drive yields to silicon-like levels has led the military to explore rad-hard alternatives based on silicon technologies such as SOI.
- A particularly attractive advantage of SOI is that, unlike SOS, these wafers can be fabricated on standard silicon processing equipment. Since SOI may well provide a marked increase in device performance with essentially no change in process, it is believed that the useful life of some silicon fabs can be extended.

SOI APPLICATIONS

Military, aerospace, automotive, and telecommunications

- **Fabricated devices include:**
  - **3-GHz ring oscillator (Hughes)**
  - **Linear ICs (Silicon General)**
  - **16K/64K CMOS SRAMs (TI)**

Key points to note:

- SOI's radiation hardness is particularly attractive for military applications, while its high-speed operation is of interest in telecommunications applications.
- SOI holds interesting promise for automotive applications because of its high-temperature capability. In the future, SOI might well provide the means for directly monitoring auto engine performance in a high-temperature environment without the use of remote sensing devices.
- The slide presents a partial list of devices that have already been fabricated using SOI materials. Bipolar, CMOS, and BiCMOS technologies are all being pursued.

SOI WAFER SUPPLIERS

Company	SOI Wafer Technology	Initial Technology Development
Applied Electron Corporation	EBZMR	Colorado State Univ., Fort Collins
Kopin Corporation	ISE/ZMR	MIT Lincoln Labs
Ibis Technology Corporation	SIMOX	Eaton Corporation
Spire Corporation	SIMOX	Spire, Texas Instruments

EBZMR = Electron-Beam Zone Melt Recrystallization
ISE/ZMR = Isolated Silicon Epitaxy/Zone Melt Recrystallization
SIMOX = Separation by IMplantation of OXygen

Source: Dataquest

Key points to note:

- Several companies currently are active in the area of SOI wafer development and manufacturing. All four companies mentioned are located in the United States; however, we are aware of SOI programs in other regions as well.

- Applied Electron Corporation is a three-year-old start-up company located in the Silicon Valley. Its proprietary e-beam technology for SOI wafer processing was developed at Colorado State University.

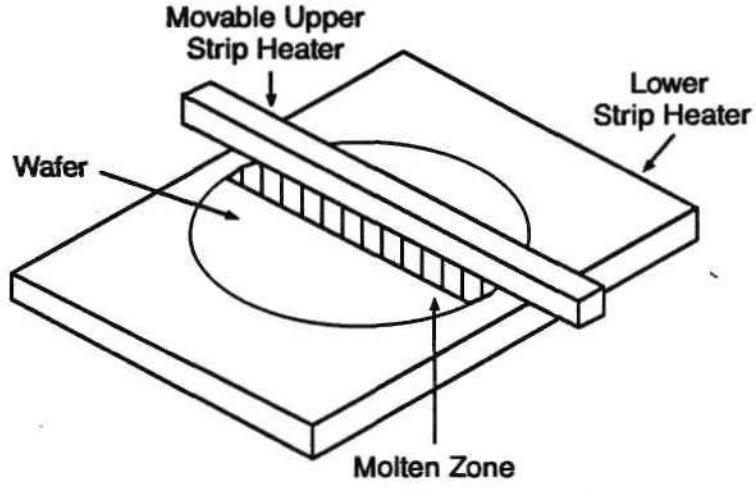
- Kopin Corporation, founded in 1984, is involved in the development and manufacture of advanced semiconductor wafer materials such as GaAs epitaxial wafers, GaAs-on-silicon, and most recently, SOI. Kopin was established as an outgrowth of R&D activities from MIT's Lincoln Laboratory. In particular, Kopin benefits from more than 10 years of SOI wafer development at Lincoln Lab, and the company holds exclusive license to many patents from MIT.

- Ibis Technology Corporation, founded in 1987, has its origins in an Eaton Corporation project to develop an oxygen implanter. The designers of the Eaton oxygen implanter purchased a machine and Eaton's SOI wafer business and left the company to found Ibis.

- Spire Corporation, like Ibis, offers SOI wafers based on the SIMOX technology. The company first began its efforts in this area in 1985. In the fall of 1988, Texas Instruments signed an agreement with Spire that will enable Spire to market 4-inch SOI wafers produced by TI.

SOI TECHNOLOGY OVERVIEW

Isolated Silicon Epitaxy (ZMR)



Source: Kopin Corporation
Dataquest

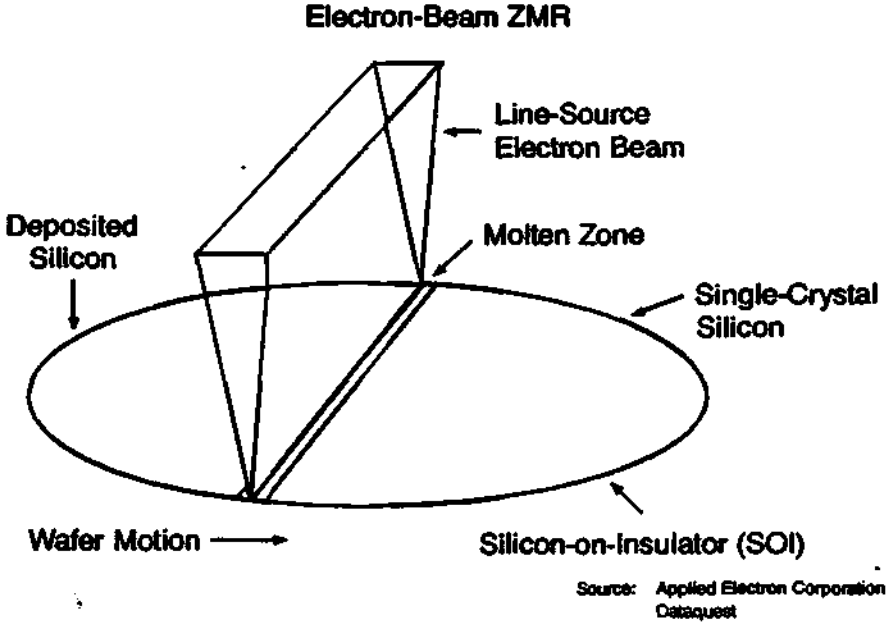
Key points to note:

- Kopin Corporation has developed a proprietary SOI manufacturing process called isolated silicon epitaxy. This process is derived from ZMR (zone melt recrystallization).

- By a thermal process, Kopin grows a layer of silicon dioxide on a wafer. In a different furnace, a layer of polysilicon is deposited over the oxide. This is followed by a second protective layer of oxide that caps the polysilicon.

- In the next stage of processing, a seed of single-crystal silicon comes in contact with the polysilicon layer at the side of the wafer. Single-crystal growth is drawn across the wafer with a movable strip heater. The polysilicon layer turns to single-crystal silicon in the process. The oxide cap is removed later.

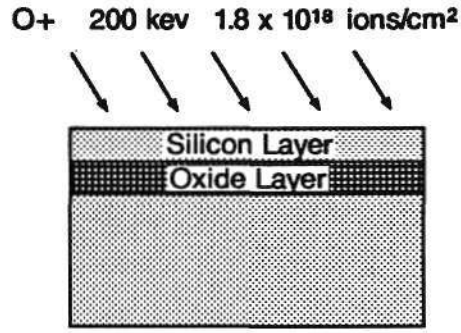
SOI TECHNOLOGY OVERVIEW



Key points to note:

- Electron-beam zone melt recrystallization, or EBZMR, is the SOI technology being pursued by Applied Electron Corporation. In this technique, the graphite strip heater in conventional ZMR has been replaced with a line-source electron beam.
- First, a thermal oxide is grown on a silicon wafer. This is followed by a poly deposition. Oxide is then deposited, forming a cap over the polysilicon layer.
- The wafer is exposed to a high-power linear-source electron beam to produce a narrow molten zone within the poly layer. As the line source is scanned across the wafer, the molten zone recrystallizes into a layer of single-crystal silicon.
- After recrystallization, the top oxide layer is etched away, either by the company or the customer, leaving single-crystal silicon on an insulating oxide layer.

SOI TECHNOLOGY OVERVIEW
SIMOX



Source: Ibis Technology Corporation
Dataquest

Key points to note:

- SIMOX, or separation by implantation of oxygen, is the SOI technique being pursued by both Ibis Technology Corporation and Spire. The specifications indicated on this slide for SIMOX processing come from Ibis, which uses an Eaton NV 200 high-current oxygen implanter in its SOI wafer processing.
- In SIMOX processing, wafers are implanted with a heavy dose of oxygen to create a buried layer of silicon dioxide. The wafers subsequently are annealed at high temperature to remove any damage from the implant.
- Technically speaking, the silicon layer on top of the oxide in SIMOX processing is not an epitaxial layer as it is in the ZMR techniques previously mentioned.

SOI OUTLOOK

Moving Down the Learning Curve

- Lower defect densities
- Lower wafer prices

Key points to note:

- Defect densities and wafer costs are two factors to monitor as SOI technology comes down the learning curve. These will dictate if SOI will one day be accepted in other than niche-market applications.

- The typical defect densities for SOI materials today are about 10^5 to 10^6 per square centimeter, with the best material on the order of 10^4. Reduced defect densities will be necessary if SOI eventually is to compete against conventional CZ and silicon epitaxial wafers. Note: Silicon-on-sapphire defect densities are on the order of 10^8 to 10^9 per square centimeter.

- Current SOI wafers are available in 4- to 6-inch diameters and have a significant range in price depending on the size of the order. Four-inch SOI wafers are priced from $500 per wafer for just a handful of wafers, to $225 per wafer for a 1,000-piece order, to as low as $150 per wafer for a 5,000-wafer lot order over the period of a year. At $150 for a 4-inch wafer, SOI material costs approximately 15 times more than conventional CZ wafers and about 5 times more than conventional silicon epi.

- Wafer costs, particularly for the oxygen implanters used in SIMOX processing, currently are dominated by machine utilization. Prices for SOI wafers are expected to drop dramatically when wafer volumes increase. The development of next-generation systems with higher throughput will also bring down the cost of wafers.

SOI OUTLOOK

Moving Down the Learning Curve

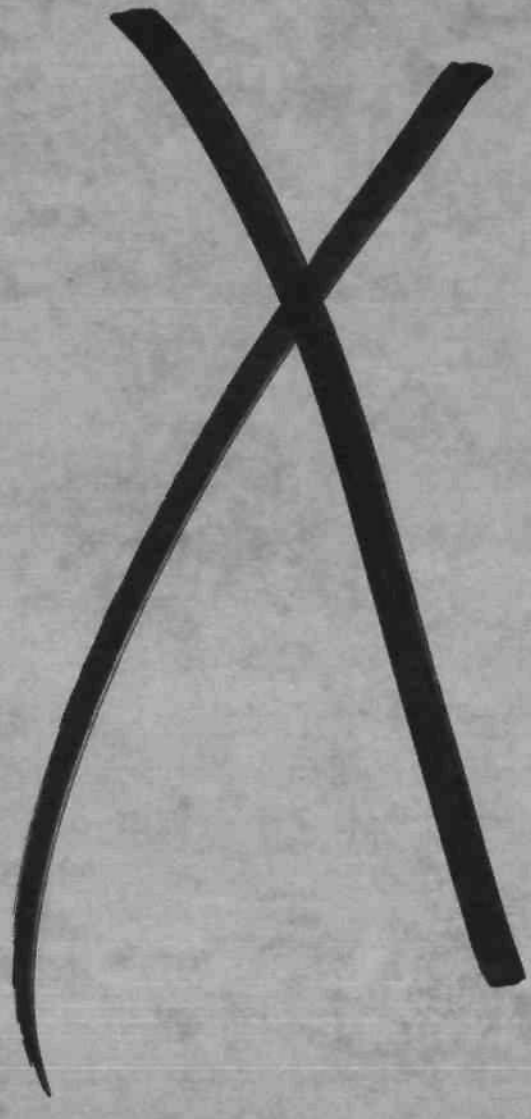
- Lower defect densities
- Lower wafer prices

New Market Opportunities

Key points to note:

- Although SOI has existed for a number of years, we now are observing the emergence of a merchant wafer supplier base. This means that a larger pool of semiconductor manufacturers has access to these materials, which in turn should drive future SOI device development. Dataquest believes that SOI's initial market opportunities will be niche oriented, but that if defect densities and wafer prices continue to come down, it holds significant promise for wider, more mainstream applications in the years to come.

Peggy Marie Wood



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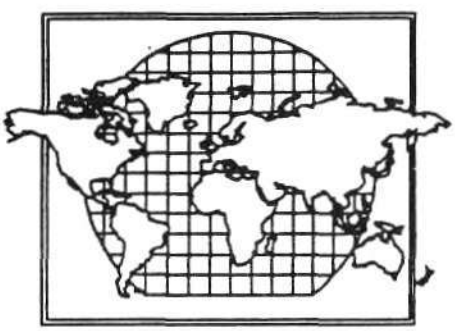

The Globalization of the Semiconductor Industry

GLOBALIZATION AND CONCENTRATION OF THE WAFER FAB EQUIPMENT INDUSTRY

Joseph Grenier
Director
Semiconductor Equipment and Materials Service
Dataquest Incorporated

At Dataquest's annual Semiconductor Industry Conference, held October 16 through 18 in Monterey, California, SEMS Director Joseph Grenier gave a presentation on globalization and concentration of the wafer fab equipment industry. This newsletter provides that presentation for our Semiconductor Equipment and Materials clients, along with some additional material not included at the conference.

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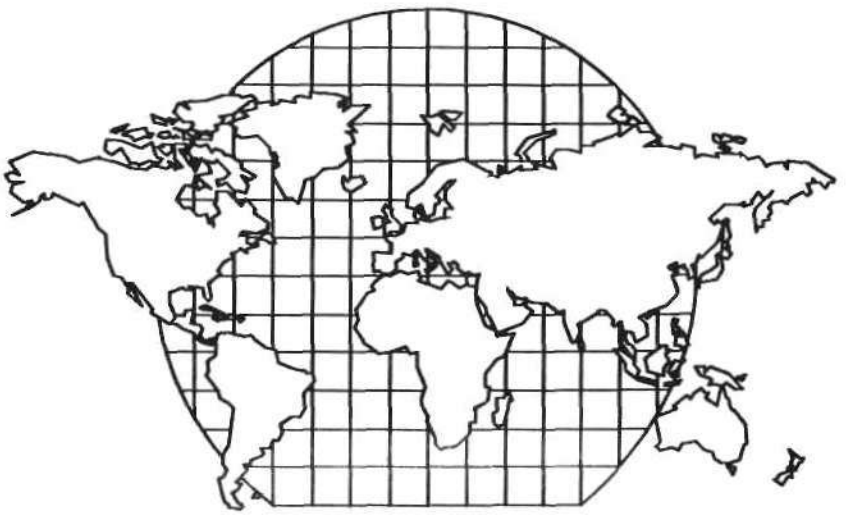
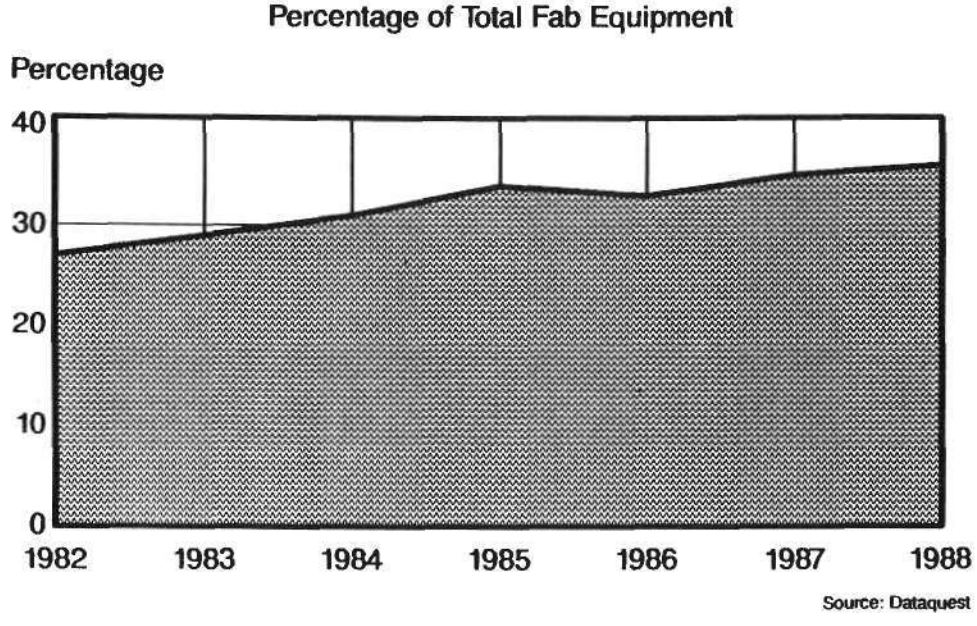


GLOBALIZATION

The theme of this conference is "The Globalization of the Semiconductor Industry." We are all aware of the fact that semiconductor manufacturing, or the chip industry, is becoming more and more globalized, but what do we know about how this applies to the semiconductor equipment industry? What is happening in this semiconductor industry segment regarding globalization?

The semiconductor equipment industry--in particular, the front-end or wafer fab equipment industry--is, in fact, becoming more globalized. Moreover, a concentration of power is occurring within this industry. The link between the two ideas is that globalization is an important cause, although not the only one, of this power concentration.

WAFER FAB EQUIPMENT WORLD TRADE

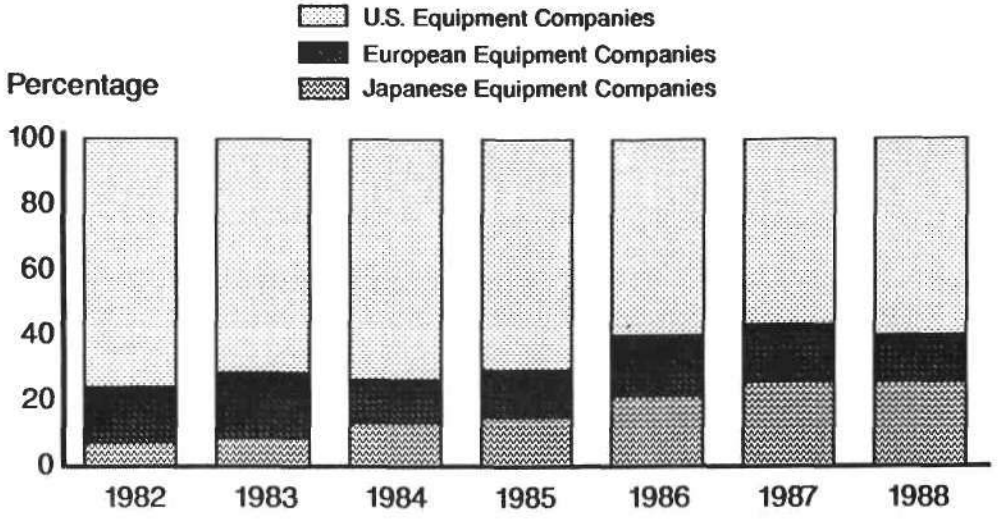


One indication of globalization is the amount of world trade that is occurring in wafer fab equipment. Dataquest defines world trade as the aggregate sum of each country's wafer fab equipment exports. I am also including in world trade the value of overseas production of wafer fab equipment by the companies that produce overseas, but that is a relatively small amount of the total. In other words, world trade by this definition is the total value of the fab equipment that enters the international market.

This slide shows the percentage of all wafer fab equipment produced worldwide that is exported. It is apparent that world trade in fab equipment is increasing. In 1982, it accounted for about 27 percent of total fab equipment and rose to more than 35 percent in 1988. Thus, about one-third of all fab equipment produced worldwide is sold in international markets or produced overseas.

WAFER FAB EQUIPMENT WORLD TRADE

Who Supplies It?



As this slide shows, in 1982, approximately 75 percent of the exports were provided by U.S. fab equipment companies and about 7 percent by Japanese companies. By 1988, exports by the Japanese equipment companies had risen 18 percentage points to about 25 percent, whereas exports by U.S. companies had fallen by 15 percent to about 60 percent. During this same time period, the proportion of overseas sales by European equipment companies fluctuated between 15 and 20 percent.

Several factors have caused the relative percentage change between U.S. and Japanese equipment companies during this period. Back in 1982, the Japanese equipment industry was still maturing, and one-third of the Japanese equipment market was supplied by imported equipment. By 1988, the Japanese equipment industry had matured and grown so that less than one-quarter of the Japanese fab equipment market was supplied by imports.

On the other hand, less than 10 percent of the U.S. equipment market was supplied by imports in 1982, whereas in 1988, one-quarter of the market was provided by imported fab equipment. In both Japan and the United States, then, about 25 percent of the domestic fab equipment market is supplied by imported equipment.

These factors taken together give some indication of why the U.S. percentage of fab equipment world trade has fallen while the Japanese percentage has risen.

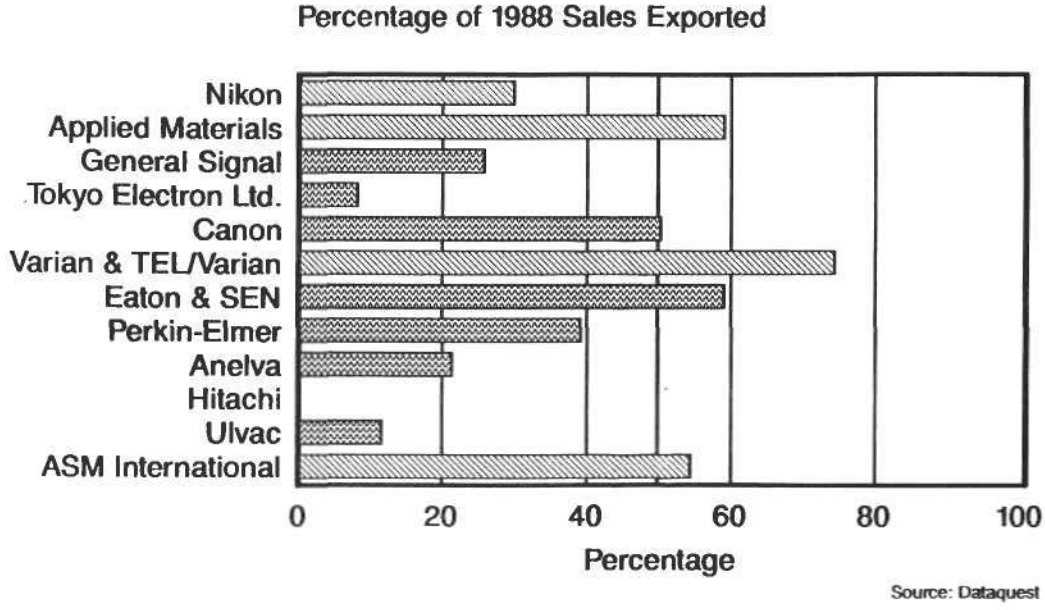
Another reason is that the Asia/Pacific region fab equipment market has grown very nicely in the last few years, and U.S., Japanese, and European equipment companies are competing hotly for this lucrative market. In fact, the Asia/Pacific equipment market currently is larger than the European equipment market. Capital spending for GoldStar and Samsung will amount to $600 million apiece this year. In the mid-70s, capital spending by the entire worldwide semiconductor industry was $600 million!

In addition, one-half the total output of U.S. fab equipment companies is exported, making the health of the U.S. equipment industry heavily dependent on export markets. One can postulate that the very viability of the U.S. equipment industry depends upon the maintenance of the export markets. This is the responsibility of both individual companies and government policymakers. For instance, equipment companies, at the very minimum, must establish strong support bases in overseas markets if they hope to stay in these markets. And the U.S. government must ensure that its export control regulations for fab equipment encourage increasing export markets rather than shackle U.S. equipment companies in their attempts to do business in emerging overseas markets.

The Japanese equipment industry, on the other hand, exports only about one-fifth of its output. Thus, the Japanese equipment industry is much less dependent upon export markets than is the U.S. equipment industry, as 80 percent of its output is absorbed by its own domestic market over which it has some control. In addition, the Japanese fab equipment industry is in a good position to grow its export markets because of a relatively low starting base of exports and because the Japanese semiconductor companies will be establishing overseas fabs.

Thus, U.S. and European fab equipment companies can expect increased competition in both their international and domestic markets.

TOP 12 WAFER FAB EQUIPMENT COMPANIES



We've been talking about the overseas sales of the Japanese, U.S., and European equipment companies, but who are these companies? This slide shows the top 12 wafer fab equipment companies ranked according to their 1988 sales. These are the only companies that had fab equipment sales exceeding $100 million in 1988. Nikon, the leader, had sales of nearly $500 million.

The horizontal bar in the chart above shows the percentage of each company's 1988 sales to overseas markets. Except for three Japanese companies, the companies all had very substantial business in international markets; in fact, a number of companies did 50 percent or more of their business in international markets.

These 12 companies provide almost two–thirds of the world market in wafer fab equipment and almost two–thirds of the world trade in fab equipment as well. Clearly, these companies are intimately involved in the globalization of the wafer fab equipment industry, and clearly, globalization is being done by the larger companies, which is to be expected.

The four asterisked companies are represented by speakers here at the conference. Speakers include Mr. Bagley of Applied Materials, Mr. del Prado of ASM, Mr. Yoshida of Nikon, and Mr. Jurvetson, representing Varian. In addition, Mr. VanLuvanee of Kulicke and Soffa, a world leader in assembly equipment that sells 75 percent of its products overseas, will be speaking. All of these men represent companies that have substantial overseas revenue, and thus, are eminently qualified to be participate in the global theme of this conference.

FACTORS AFFECTING GLOBALIZATION

- Growing international markets
- Offshore fabs
- Europe 1992
- Governmental factors

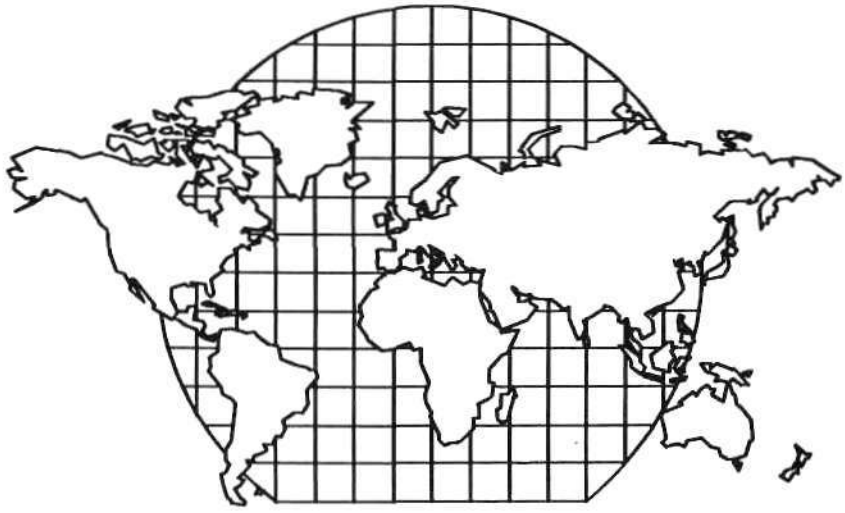
To conclude our discussion of globalization, some of the major factors promoting world trade of wafer fab equipment are the following:

- Growing international markets—Japan is now the largest equipment market in the world. Two-thirds of the world's fab equipment market is in Japan and the rapidly growing Asia/Pacific markets. In addition, the People's Republic of China is a potential growth market.

- Offshore fabs—More than 40 offshore fabs have been established by worldwide semiconductor manufacturers. When a semiconductor manufacturer establishes an offshore fab, the manufacturer generally brings the process and equipment from its domestic fabs. This forces the equipment companies supplying the offshore fab to establish overseas facilities in order to support the fab.

- Europe 1992—Two–thirds of the European fab equipment market is supplied by imported equipment. How will the unified European market in 1992 affect the current wafer fab equipment companies supplying the imports? Will companies need to manufacture in Europe in some cases? Will they need to restructure their European organizations? What about unified equipment safety standards? What steps will companies have to take to continue selling into Europe? These are some of the questions being asked, but the impact of 1992 on the European fab equipment market is not yet clear.

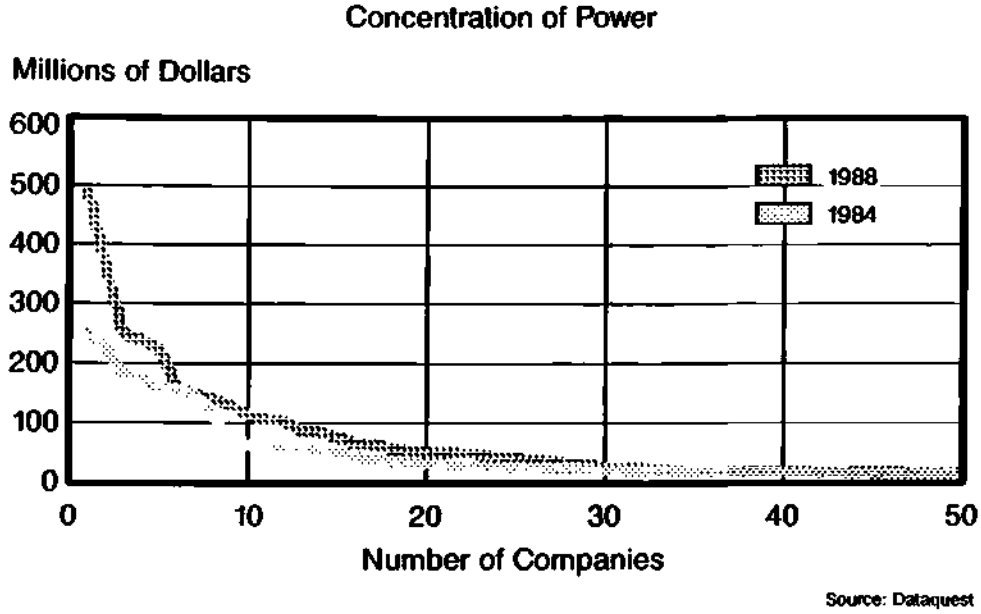
- Government roles—Trade policies, export control regulations, and government spending to develop equipment and processes are a few factors promoting globalization. Joint development programs and consortia, such as Sematech, JESSI, the various X–ray programs in Japan and Europe, and university programs in the United States, play a role in strengthening domestic industry, which provides the base for globalization. In other words, how proactive are governments in promoting the health of domestic fab equipment industries?



CONCENTRATION

A concentration of power is occurring in the wafer fab equipment industry as mentioned earlier, and globalization is a prime causal factor.

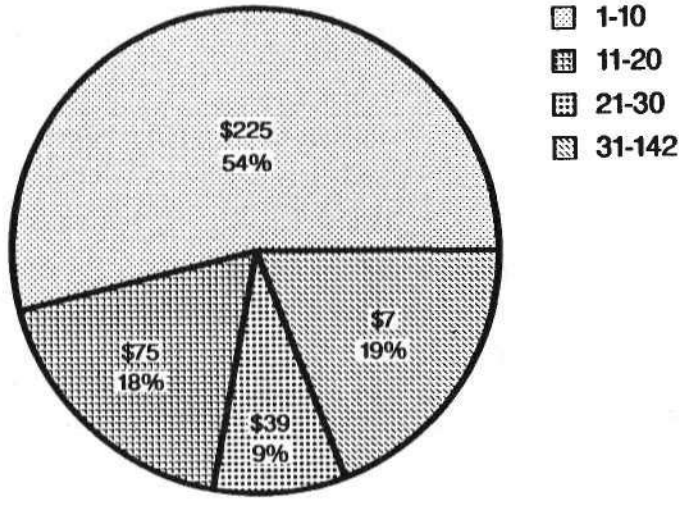
WAFER FAB EQUIPMENT



Shown above are the sales of the top 50 companies for 1984 and 1988. Clearly, the sales of the top 30 companies have grown larger from 1984 to 1988, while the sales of the smaller companies have remained the same. In other words, the big are getting bigger, and the small are staying small. There are certain exceptions to this rule--many excellent smaller companies are exhibiting growth. I think the general conclusion is valid, however, that a concentration of power is occurring in the wafer fab equipment industry.

WAFER EQUIPMENT COMPANIES

1988 Revenue Breakdown

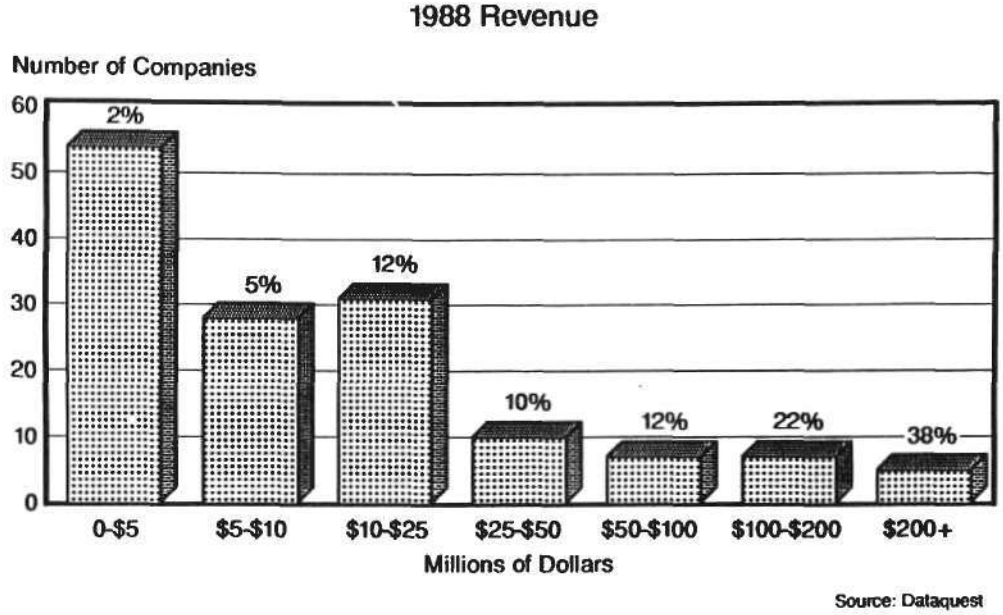


Source: Dataquest

Looking at concentration another way, the top 10 wafer fab equipment companies accounted for 54 percent of the 1988 world revenue for the key fab equipment areas. The top 20 companies accounted for 72 percent of the world revenue, and the top 30 companies accounted for more than 80 percent. The remaining 112 companies accounted for only about 20 percent. This is a textbook example of the 80–20 rule: 20 percent of the companies captured 80 percent of the revenue.

The dollar amounts shown above are the average sales for each group of companies. As you can see, average sales fall off very quickly for each group, from $225 million for the top 10 to $75 million for the 11 to 20 group to $39 million for the 21 to 30 group, all the way down to $7 million for the bottom 112 companies.

WAFER FAB EQUIPMENT COMPANIES



Shown above are the 142 wafer fab equipment companies broken down into revenue groups. Most of the companies are small. In fact, 54 companies had revenue of $5 million or less, and these 54 companies accounted for only 2 percent of the world revenue for key fab equipment in 1988. In the $0 to $10 million range, 82 companies collectively accounted for only 7 percent of the revenue.

At the high end are 12 companies that had 1988 fab equipment revenue of $100 million or more, and these 12 companies accounted for 60 percent of the world revenue.

FACTORS AFFECTING CONCENTRATION

- Globalization
- Need to provide equipment and process
- Increasing R&D costs
- Lack of sources of capital
- Financial strength

To wind up the discussion of concentration, some of the major factors encouraging it are:

- Globalization—As globalization proceeds, equipment companies must establish, at the bare minimum, overseas facilities to support their customers. This requires an investment that favors larger, more financially strong equipment companies.

- Need to provide equipment and process—Gone are the days when equipment companies provided only the equipment; now the companies must provide a guaranteed process as well. In order to provide the process, equipment companies must make investments in a clean room with its associated capital equipment, as well as additional process engineers and support people. Again, this favors larger companies.

- Increasing R&D costs—Small companies are finding it harder and harder to fund the leading-edge R&D that is required to stay competitive. If they cannot stay competitive, sales fall, less funds are available for R&D, and they become less competitive. Thus, the downward spiral continues.

- Lack of sources of capital—Small companies are having an increasingly difficult time raising capital. The financial community, in general, is not as enamored with the high-technology industry as it was a few years ago. In addition, success stories for start-up companies in the wafer fab equipment industry have been few, with very few examples of companies whose sales have skyrocketed in a short time.

- Financial strength—Building a state-of-the-art fab costs as much as $500 million, and the semiconductor manufacturer is staking its success on the equipment that it buys. Besides technical performance as an important buying criterion, the semiconductor manufacturer wants to be assured that the equipment vendor will be able to support the equipment fully into the future. Here too, the larger company is favored.

IMPACT OF GLOBALIZATION AND CONCENTRATION

- On large equipment companies
- On small equipment companies
- On entreprenurial activity

To summarize, both globalization and concentration favor large equipment companies and make it a lot tougher on smaller companies. We are now seeing consolidation and the formation of alliances between large and small companies in the industry as smaller companies look for ways of growing or even surviving.

Perhaps this is part of the natural process of the maturation of an industry. Another characteristic of a maturing industry is the erection of entry barriers to the industry, and in many of the key equipment areas, entry barriers are getting higher.

However, a caveat: smaller companies are a major source of entrepreneurial activity and innovative ideas. We all intuitively know this. However, a very interesting study was recently done that supports our idea. It found that compared with larger companies, smaller companies tend to have more creative new product ideas and higher success rates for these ideas, with shorter development times, and at less cost. Without viable small companies, will the industry's creativeness be stunted?

This concludes my remarks. I hope that I have left you with a few ideas to keep in mind.

Joe Grenier

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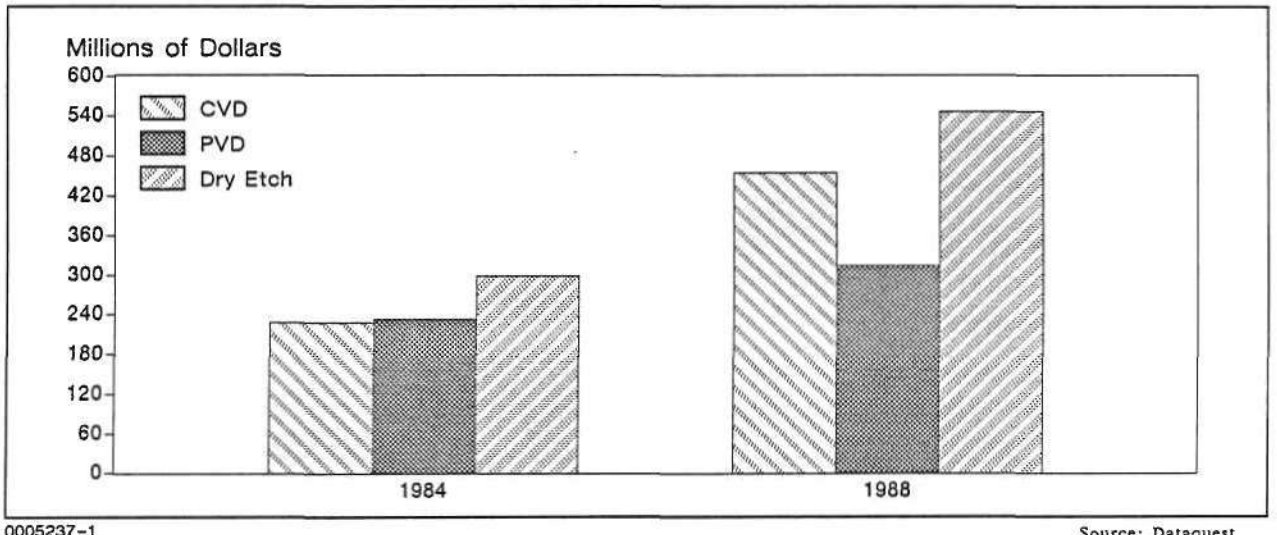
INTEGRATED PROCESSING TECHNOLOGY IN A STANDARDIZED MARKET ENVIRONMENT

THE PROBLEM: AVAILABILITY OF HIGH-QUALITY THIN-FILM PROCESS EQUIPMENT

The availability of high-quality thin-film deposition and etch technologies is crucial to cost-effective submicron manufacturing. Chemical vapor deposition (CVD), physical vapor deposition (PVD), and dry-etch equipment and processes are the cornerstones of high-quality thin films. Figure 1 illustrates the dramatic growth of the worldwide CVD, PVD, and dry-etch equipment markets between 1984 and 1988. These technology-driven markets are fueled by the relentless upward march toward higher chip integration and performance on an increasingly tortuous road marked by ever-finer geometries and killer defects that could cause steep plunges to zero device yields. Dataquest observes considerable synergy and interdependence between the thin-film deposition and etch markets as device geometries head into the submicron regime.

Figure 1

Worldwide CVD, PVD, Dry-Etch Equipment Markets



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Source: Dataquest
October 1989

THE SOLUTION: INTEGRATED PROCESSING EQUIPMENT

Integrated process equipment development has been driven by the trend toward in-situ film deposition and etch processes to minimize defects and simplify increasingly complex technologies. Integrated processing equipment offers the advantages of in-situ multilayer film deposition and etching, lower defects, simplicity, flexibility, and progressive automation in semiconductor manufacturing.

Dataquest defines two broad types of integrated processing equipment: rigid multichamber tools (RMTs), which have the traditional fixed configuration for specific processes, and flexible cluster tools (FCTs), which are truly modular and reconfigurable for a broad range of future processes.

A typical FCT consists of a central, highly reliable, automated wafer-handling platform equipped with a robot for transferring wafers between the input/output (IO) loadlock chamber and any given process chamber module. FCTs are highly modular and made of detachable subsystems, each with its own computer, utilities, and communications capabilities. The central wafer-handling chamber has a series of standard wafer-transfer interface ports to which the process module chambers or the input/output chambers may be bolted.

Ideally, each bolt-on process chamber is a "smart," fully functional reactor with its own vacuum pumps, utilities such as electricity and process gases, plasma power supply, gas distribution, computer, and communication units. The process chamber should be capable of being unbolted and wheeled away for preventive maintenance and standalone process development without interrupting the operation of the mainframe cluster tool. The mainframe platform has a supervisory computer, utilities, and communications systems for coordinating the process sequence through the bolted process modules.

Each of the FCT modules attached to the central platform must be compatible with the overall system throughput, process sequence, film interface, and temperature cycles. The cluster configuration should be carefully optimized with regard to throughput, chamber type, and process flow for any given application. The process chamber has to deliver superior process results by itself and in synergy with the other elements of the cluster tool.

Dataquest expects FCTs to integrate areas such as dry clean, CVD, PVD, etch, and rapid thermal processing (RTP) around a central wafer-handling chamber. The emergence of industry standards for mechanical, wafer-handling, utilities, communications, and software interfaces should spur the acceptance of FCTs.

MODULAR, STANDARDIZED EQUIPMENT CONFIGURATION

Semiconductor manufacturers welcome the move to integrated processing; it enables them to configure flexible manufacturing systems using industry-standard components from multiple equipment vendors. A high degree of reliability and compatibility will be needed from different components of integrated processing

systems. Any weak, incompatible link in the integrated process chain will make the entire system unusable and thus escalate operating costs tremendously. Open architecture and industry standards probably will lead to increased competition among equipment companies. Customer service and advanced process capabilities will be the differentiating factors in an otherwise standardized hardware environment.

MAJOR WORLDWIDE INTEGRATED PROCESSING EQUIPMENT COMPANIES

Numerous companies based in different regions of the world participate in the integrated processing equipment market. Table 1 lists some of the worldwide companies that offer integrated processing equipment. Most of the integrated process equipment products currently available in the market are precursor tools and can be classified as RMTs with the traditional fixed, multichamber configuration. Only a few currently available products are flexible and modular enough to be considered as true FCTs. An ideal FCT enables any arbitrary sequence of operations and random access to any of the process modules. Each of the process modules may be a single-wafer chamber or a multiwafer batch chamber. The FCT system should have the capability of being reconfigured rapidly for varying process needs by quickly changing process chambers.

Table 1

Worldwide Integrated Processing Equipment Companies

U.S. Companies	Japanese Companies	European Companies
Advantage Production	Anelva	Alcatel/Comptech
Applied Materials	Hitachi	ASM International
Branson/IPC	Kokusai Electric	Balzers
BTU International	Sumitomo Metals	Electrotech
Eaton	Tokyo Electron	Plasma Technology
General Signal/Drytek	Ulvac	
Lam Research		
Machine Technology Inc.		
Materials Research Corporation		
Plasma Therm		
Rapro Technology		
Spectrum CVD		
Tegal		
Varian		

Source: Dataquest
October 1989

APPLICATIONS FOR INTEGRATED PROCESSING TECHNOLOGY

Many applications are emerging for integrated processing technology because of the versatility of the cluster tool concept. Table 2 lists a sampling of integrated process applications that may be implemented with the currently available cluster tools. Dataquest believes that the limited RMT applications available today will expand into truly flexible applications in the future, including more challenging fabrication process modules such as lithography and process monitoring. The emergence of cluster tools together with integrated process applications is likely to be a barometer of automation trends in the semiconductor manufacturing business.

Table 2

Potential Integrated Processing Equipment Applications

Application	Dry Clean	CVD	PVD	Dry Etch	Dry Strip	RTP
Blanket/Selective Epi Growth	X	X				X
In-Situ Gate Oxide and Poly Deposition	X	X				X
Self-Aligned Source/ Drain Silicides	X		X			X
Tungsten Contact/Via Plugs	X	X		X		X
Multilayer Interconnect Film Deposition	X	X	X			
Multilayer Interconnect Film Patterning				X	X	
Interlayer Dielectric and Passivation Film Deposition		X				
In-Situ Interlayer Dielectric Planarization		X		X		

Source: Dataquest
October 1989

DATAQUEST CONCLUSIONS

Dataquest believes that integrated cluster tools will be the enabling technology for cost-effective submicron manufacturing. Such tools will allow progressive fab automation to integrate increasingly complex process technologies in order to achieve good production throughputs and yields. The availability of modular, standardized cluster components will allow the semiconductor manufacturer to mix and match optimum tools for specific applications. Conversely, industry-standard components and interfaces will allow small equipment companies to devote scarce development resources to what they do best—i.e., new process development. Large equipment companies can leverage off common integrated architectures by quickly penetrating a wide range of thin-film equipment markets.

The recently announced strategic alliance between Applied Materials and Peak Systems signals the evolution of a new equipment industry structure. Under the terms of this alliance, Peak Systems will develop an OEM rapid thermal processor module for Applied Materials' popular PE5000 platform. In return, Applied Materials will make an investment equal to a 10 percent equity position in Peak Systems. Standardized equipment architecture will enable small equipment companies to focus on reactor-module and process development using industry-standard hardware platforms. Large equipment companies can quicken time-to-market on multiple application fronts by integrating specialized reactor modules from small equipment companies on an OEM basis.

New equipment industry companies such as wafer-handling system manufacturers, CIM software vendors, and system integrators possibly will emerge as a result of the ease of porting their products to industry-standard interfaces. Dataquest believes that integrated processing equipment with industry-standard architecture and interfaces is a win-win situation for both equipment companies and semiconductor manufacturing companies.

Krishna Shankar

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THE ASIC PACKAGE PROLIFERATION

SUMMARY

Surface-mount technology is now mainstream. Dataquest believes that surface-mount devices (SMDs) will continue to grow at a pace that exceeds traditional packaging and assembly techniques. As ASICs continue to grow in usage, many new surface-mount package families will be developed. This will cause multiple package choices for the same IC, resulting in difficulties for design engineers, assembly engineers, and purchasing agents (i.e., nonstandard packages for second-sourcing). It could make it more costly for semiconductor manufacturers to compete.

This newsletter will discuss the packages currently being used or under development for ASICs. It will also review the issues and choices pertaining to standards involved in ASIC packaging.

INDUSTRY ANALYSIS

Dataquest expects the worldwide integrated circuit package market to grow at a 10 percent compound annual growth rate (CAGR) from 1987 to 1992. We expect surface-mount devices to continue to show the greatest gain. They are expected to grow from the current level of 20 percent (year-end 1988) to almost one-half of all IC packages (48.4 percent) by 1992. These statistics are shown in Tables 1a and 1b.

The forecast shows the fastest growth area to be the quad flat package (76.3 percent CAGR). This is directly related to the worldwide increase in ASIC production.

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Table 1a

Estimated Worldwide Shipments by Package Type (Millions of Units)

Package	1987	1988	1989	1990	1991	1992	CAGR 1987-1992
Plastic DIP	23,194	26,282	25,292	21,741	21,103	20,625	(2.4%)
CERDIP	3,346	3,738	3,274	2,778	2,783	2,727	(4.2%)
Ceramic DIP	270	277	250	231	225	203	(5.9%)
Quad/Ceramic and Plastic	284	805	1,357	1,640	2,785	4,833	76.3%
Ceramic Chip Carrier	207	315	374	383	430	562	22.1%
Plastic Chip Carrier	508	1,024	1,412	1,513	1,987	2,792	40.6%
SO	3,092	4,954	6,202	7,167	9,396	12,881	33.0%
PGA/Ceramic and Plastic	234	614	983	1,118	1,583	2,339	58.5%
Other (TAB/COB/ FCHIP)	470	860	1,224	1,480	2,249	3,817	52.0%
Others	479	657	684	596	612	608	4.9%
Total	32,084	39,526	41,051	38,647	43,153	51,386	9.9%
Total of SMT	4,561	7,958	10,569	12,183	16,847	24,885	40.4%
Percent of SMT	14.2%	20.1%	25.7%	31.5%	39.0%	48.4%	

Table 1b

Estimated Worldwide Shipments by Package Type (Percent)

Package	1987	1988	1989	1990	1991	1992
Plastic DIP	72.3%	66.5%	61.6%	56.3%	48.9%	40.1%
CERDIP	10.4	9.5	8.0	7.2	6.5	5.3
Ceramic DIP	0.8	0.7	0.6	0.6	0.5	0.4
Quad/Ceramic and Plastic	0.8	2.0	3.3	4.2	6.5	9.4
Ceramic Chip Carrier	0.7	0.8	0.9	1.0	1.0	1.1
Plastic Chip Carrier	1.6	2.6	3.4	3.9	4.6	5.4
SO	9.6	12.5	15.1	18.6	21.8	25.1
PGA/Ceramic and Plastic	0.7	1.6	2.4	2.9	3.7	4.6
Other (TAB/COB/ FCHIP)	1.4	2.2	3.0	3.8	5.2	7.4
Others	1.4	1.6	1.7	1.5	1.4	1.2
Total	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%

Note: Percentages may not add to 100.0% because of rounding.

Source: Dataquest
July 1989

PACKAGE TYPES

Quad Flat Packs—Old and New

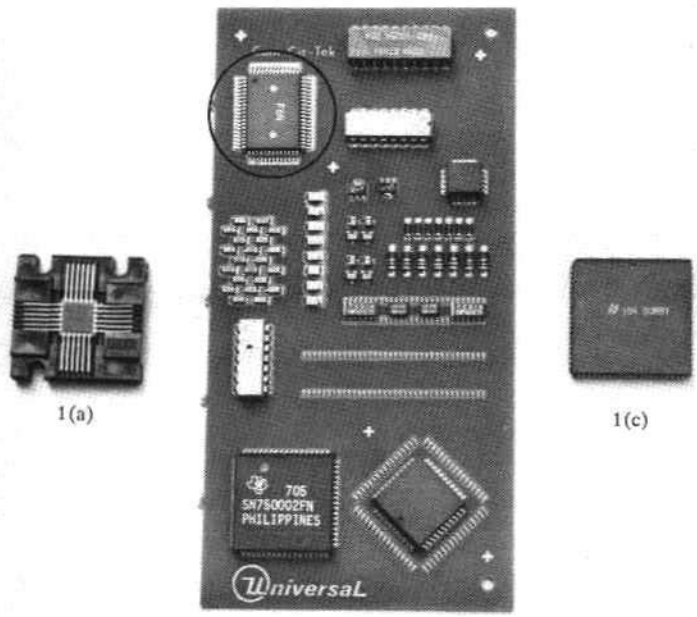
The true, original flat package is not new. Based on 50-mil lead spacing and ceramic technology, it has been and still is used primarily in military applications. The quads are mostly flat, retangular packages with bodies constructed of alumina or beryllia, with glass-to-metal seals. The long leads are splayed out away from the package body on all sides, in a gull-wing-style lead form. Lead counts generally range from 12 to 28 leads. Figure 1(a) shows a photograph of a ceramic quad flat package.

As commercial development of surface mount became prevalent in the early 1980s, the Electronic Industries Association of Japan (EIAJ) began to develop its own plastic versions of the quad flat package. These packages were based on the premise of keeping package body sizes the same and varying the lead pitch, thus increasing lead count density. Pitches of 1.0mm (39.4 mils), 0.8mm (31.5 mils), and 0.65mm (25.6 mils) form standards that define packages from 20 to 240 leads, depending upon body size. This package is also called the quad flat pack (QFP), as seen in Figure 1(b).

Expanding on this, the U.S. manufacturers agreed that placing leads on all four sides of a package was beneficial. But bending the leads underneath the package would increase density even further, and it also could be compatible with the ceramic leadless chip carrier board footprint. Thus the J-bend plastic leaded chip carrier (PLCC) was developed, with lead counts ranging from 18 to 100 leads on 50-mil center lead spacing (see Figure 1(c)).

Figure 1

Ceramic Quad Flat Package



1(a) 1(b) 1(c)

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Source: Dataquest
July 1989

However, the PLCC on 50-mil spacing did not address the increasing demand of ASIC products for higher lead counts (more than 100 pins). So, the United States through the Joint Electronics Device Engineering Council (JEDEC) developed the plastic quad flat package (PQFP) for this requirement. It uses the same plastic body sizes as the PLCC, but has leads on 25-mil centers and a molded "bumper" protruding from each corner for lead protection during handling. Lead counts for this package family range from 44 to 244 leads, and the gull wing is the preferred lead form (see Figure 2).

Figure 2

Plastic Quad Flat Package

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Source: Dataquest
July 1989

Finer Pitch Packages

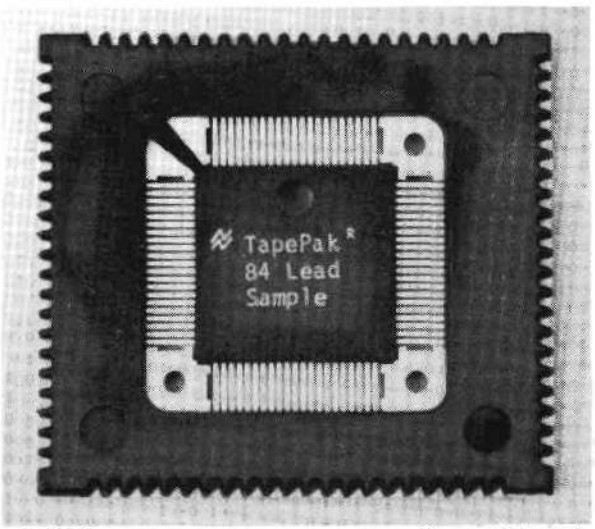
With the consumer market driving for smaller, less costly electronic gadgets and the ASIC market needing higher lead count packages, the Japanese have developed yet another package family: The shrink quad flat package (sometimes called the very small quad flat package (VQFP)). In some ways, this family is an extension of the EIAJ quad flat package (QFP). It also uses standard body sizes, but the package is one-half the thickness, and the lead pitches are reduced to 0.5mm (19.7 mils), 0.4mm (15.7 mils), and 0.3mm (11.8 mils). Lead counts range from 32 to 520 leads.

Besides those mentioned, two more surface-mount package families have recently been introduced into the market for ASIC packaging. One is TapePak developed by National Semiconductor; the other is the TQFP, a TAB quad flat pack developed by LSI Logic.

TapePak uses tape automated bonding (TAB) tape as the lead frame that is attached directly to the die. No wire bonding is used. This die–on–tape combination is then molded in plastic so that an outside ring is formed apart from the inside encapsulated die. This outside ring provides for lead protection and test capabilities. The package body is excised from the carrier ring by the pick–and–place machine and is subsequently attached to the printed circuit board. Like the Japanese quad flat pack, the TapePak family uses standard body sizes with lead counts from 40 to more than 460 leads on 20–, 15–, and 10–mil pitch. This package is shown in Figure 3.

Figure 3

TapePak



0004588–3 Source: Dataquest July 1989

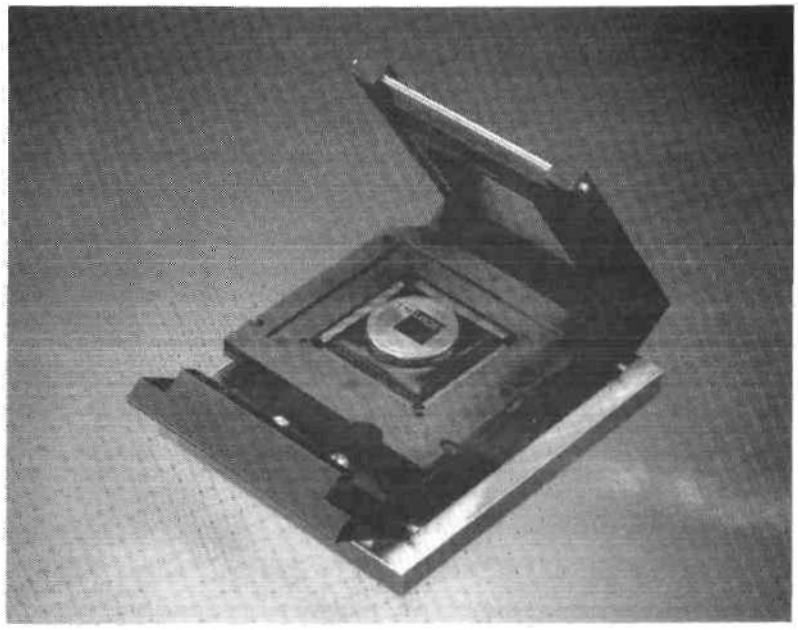
The TQFP is similar to TapePak, except for the following:

- It uses wire bonding for lead counts up to 300 and TAB from 300 to 524 leads.
- The die is encapsulated, using a liquid epoxy "blob."
- A two–piece plastic disposable slide carrier is used for lead protection and test.
- Pin counts range from 164 to 524 leads.

A picture of the TQFP is shown in Figure 4.

Figure 4

TAB Quad Flat Pack



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Source: Dataquest July 1989

Higher Lead Counts and the No-Package Package

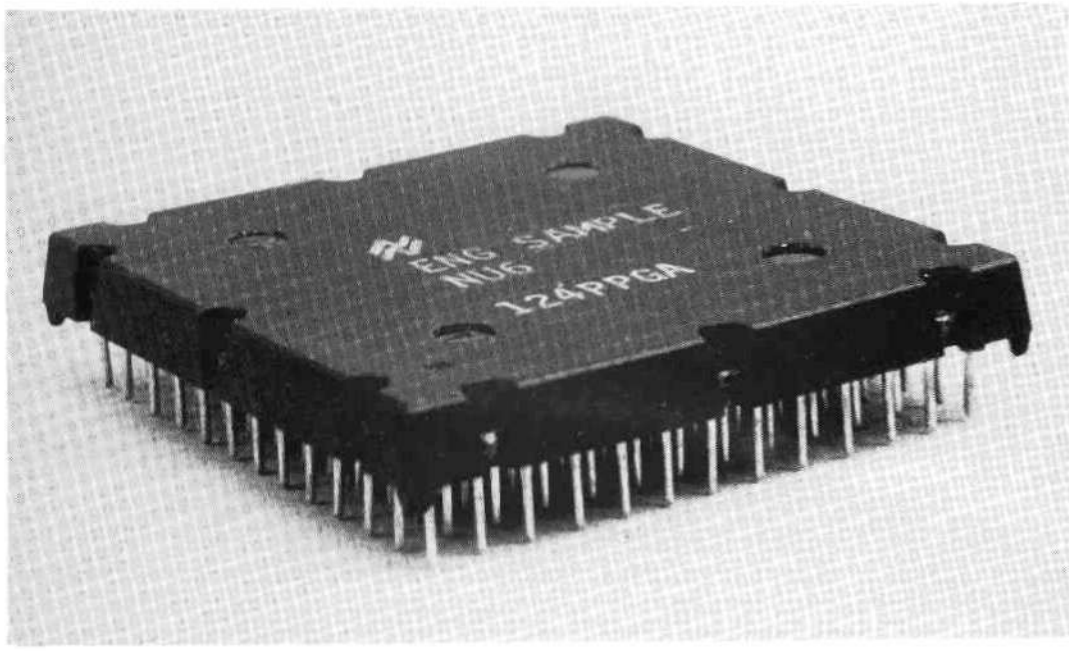
Another packaging solution to ASICs is the pin grid array. Although not assembled to the board using surface-mount technology, it does provide high-density capability to 1,000 leads and beyond. Rows of pins on 100-mil spacing (and more recently 50 mil) are arranged in a grid format to form the PGA (see Figure 5). It is available in both ceramic and plastic and is capable of dissipating more heat than most surface-mount packages.

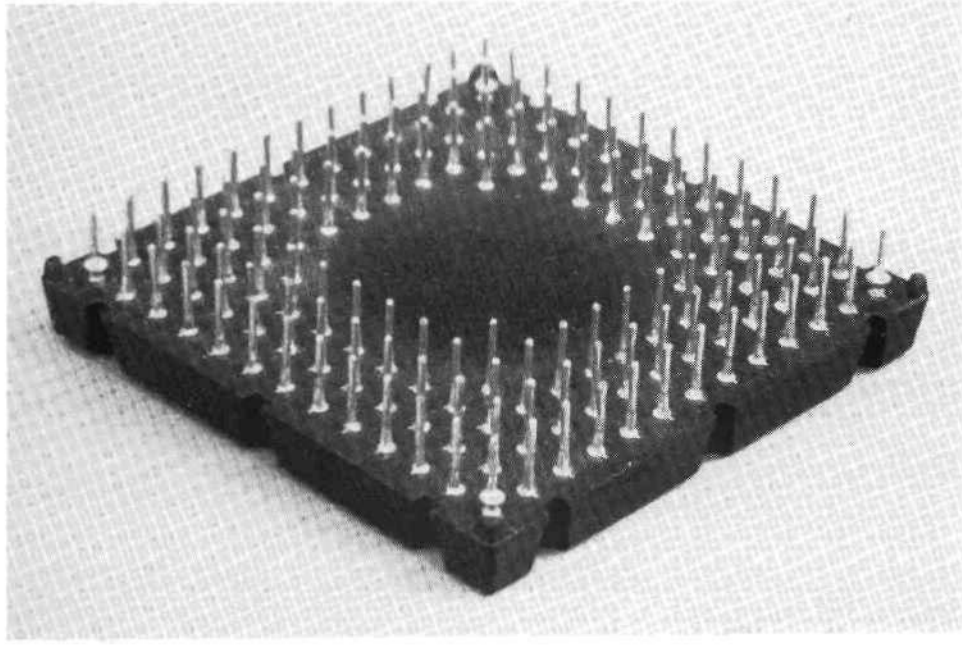
There is one more approach to ASIC packaging that does not really use a package in the traditional sense. Chip-on-board (COB) technology enables the bare die to be attached directly to the printed circuit board. The die is attached to the board via an adhesive (usually epoxy) and wire-bonded directly to the pads or traces on the PCB. After bonding, the die is usually coated with a blob of plastic material to provide for mechanical and environmental protection.

Variations of the COB approach include TAB-on-board (TOB). Component leads are etched on single-layer or multilayer copper/copper-polyimide tape. The tape is etched to form patterns that correspond to the die pad layout. These patterned leads then make the connection between the die and the printed circuit board. Whereas wire-bonded COB is done on a chip-by-chip basis, TOB can be done via an automated, reel-to-reel process. The die-on-tape can then be attached to the board and encapsulated, as in the COB process. An example of TOB is Siemens' Micropak. A basic flow of the TOB process is shown in Figure 6.

Figure 5

Rows of Pins Forming the PGA





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Source: Dataquest
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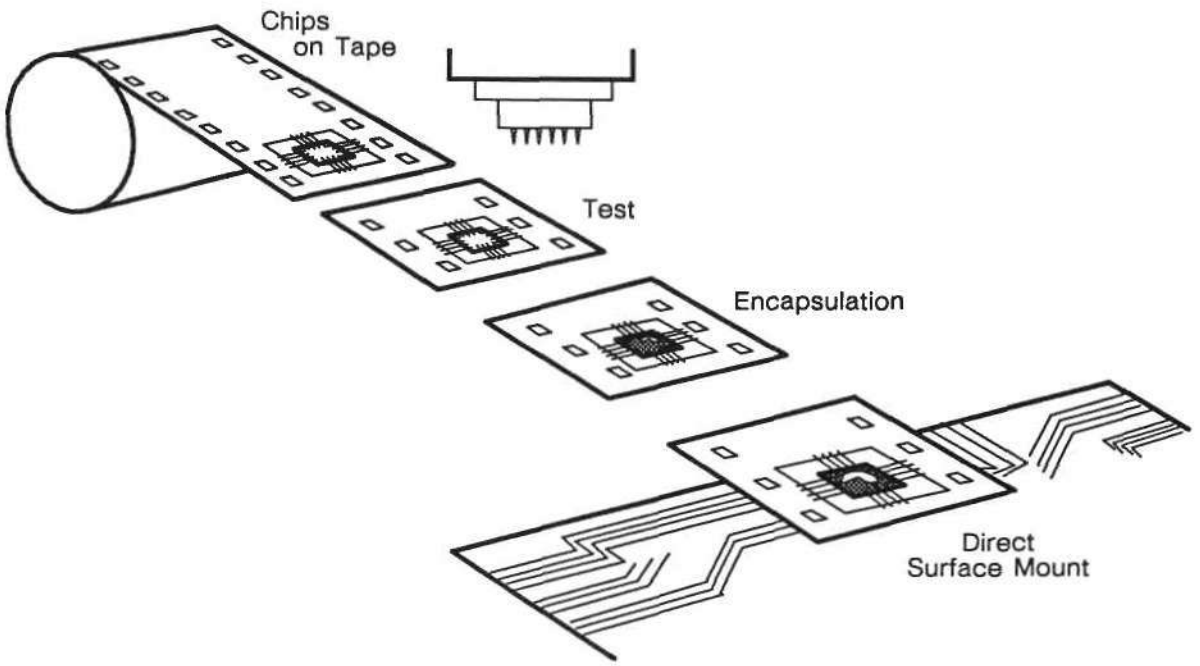
Figure 6

TOB Process (Basic Flow)



0004588-6

Source: MESA Technology

Finally, flip chip is one other assembly process that can be used in ASIC packaging. This process was developed by IBM in the late 1960s and is known as C-4, for controlled-collapse chip connection. It is basically a process in which the chip is designed for facedown reflow soldering. The bond pads are bumped with solder while in wafer form. Passivation (silicon nitride) is added, and the wafer is tested via the solder bumps. After testing, the dice are placed facedown, or flipped, on the ceramic substrate, and the assembly is heated in a furnace to reflow the solder. The surface tension of the solder aligns the dice properly to the substrate. This is the maximum use of interconnect density, as no lead frame, wires, or tape are used.

A DESIGNER'S NIGHTMARE

What package should an ASIC design engineer choose? Assuming that it is an ASIC requiring 68 leads, the following choices can be made if a plastic package is desired:

- 68-lead PLCC (JEDEC)
- 68-lead PQFP (JEDEC)
- 68-lead QFP (EIAJ)
- 68-lead VQFP (EIAJ)
- 68-lead TapePak (JEDEC)
- 68-lead PPGA (JEDEC)
- 68-lead COB (No standard)
- 68-lead TOB (EIA/IPC/ASTM)
- 68-lead Micropak (Europe/DIN)

The following section discusses the above listing in more detail. Table 2 lists some common specifications for each package.

Table 2

68-Lead Package Options*

	Lead Pitch	Lead Width	Package Size	Package Height
PLCC	0.050"	0.028"	0.950" sq.	0.180"
PQFP	0.025"	0.012"	0.550" sq.	0.102"
QFP	0.0256"	0.0118"	0.394" x 0.551"	0.100"
VQFP	0.0118"	0.004"	0.197" x 0.276"	0.050"
TapePak	0.020"	0.010"	0.505" sq.	0.072"
PPGA	0.100"	0.018"	1.14" sq.	0.180"
COB	0.008"	0.0014"	0.378" sq.	0.032"
TOB	0.020"	0.010"	0.378" sq.	0.032"
Micropak	0.0197"	0.009"	0.386" sq.	0.025"

*See Appendix A attached to this newsletter.

Source: Dataquest
July 1989

One can readily see that little, if any, compatibility exists among the various packaging styles, except possibly COB versus TOB. This means that designing with an ASIC from supplier A in PQFP (JEDEC) may not be compatible with the ASIC from supplier B in QFP (EIAJ), even if the silicon function is the same. The possible result is a sole–source supplier based primarily on package offering, not silicon.

STANDARDS ACTIVITY

There has been criticism of industry organizations for their lack of leadership in setting surface–mount standards. Some is justified, as it is difficult to get everyone to agree on one of anything, whether it be process, part, or package. There are major differences between the U.S. and Japanese styles of packages. Work needs to continue to bring commonality to this area.

Package standardization is proceeding within the United States at a faster rate as surface mount becomes a proven technology. To address industry awareness and the need for areas of standardization in surface–mount technology, representatives from EIA, IPC, JEDEC, and ASTM have joined together to form the Surface Mount Council. In January 1989, they issued a document entitled "Survey Report: Surface–Mount Standards, Requirements, and Issues."

This report surveyed responses regarding the awareness and usage of 14 typical standards currently available to the industry. In the case of integrated circuit components, the survey found that only 61 percent of the respondents used all or part of the EIA JEP–95 specification (JEDEC Registered and Standard Outlines for Semiconductor Devices). Eighteen percent were aware of this standard but did not choose to use it, and 16 percent were not aware of the standard. Highlights from this report related to component standards are shown in Table 3.

Table 3

Surface–Mount Component Standards

	Use Standard	Use Part of Standard	Do Not Use	Unaware of Standard
EIA RS 481A--Taping of SM Components for Automatic Placement	30.6%	18.8%	17.6%	20.0%
EIA PDP 100--Mechanical Outline for Registered and Standard Electronic Parts	14.1%	29.4%	16.5%	27.1%
EIA JEP 95-JEDEC--Registered and Standard Outlines for Semiconductor Devices	24.7%	36.5%	17.6%	16.5%
EIA JESD 11--Chip Carrier Pinouts for CMOS 4000HC and HCT Circuits	9.4%	17.6%	16.5%	44.7%

Source: EIA/IPC Surface Mount Council

In addition, many organizations worldwide have established committees to discuss issues related to surface-mount technology. A list of these is shown as follows:

- ACPI (Automated Component Placement and Insertion Group)—c/o AMP, 1000 AMP Drive, Harrisburg, PA 17112
- ANSI (American National Standards Institute)—1430 Broadway, New York, NY 10018
- ASTM (American Society of Testing and Materials)—1916 Race Street, Philadelphia, PA 19103
- BSI (British Standards Institute)—2 Park Street, London, W1A 12BS, United Kingdom
- CSA (Canadian Standards Association)—178 Rexsdale Boulevard, Rexsdale, Ontario, Canada
- DOD (U.S. Department of Defense, Naval Publications Center)—5801 Tabor Road, Philadelphia, PA 19120
- EIA (Electronic Industries Association)—2001 Eye Street N.W., Washington, D.C. 20006
- EIAJ (Electronic Industries Association of Japan)—250 West 34th Street, New York, NY 10119
- EMPF (Electronics Manufacturing Productivity Facility)—1417 North Norma Street, Ridgecrest, CA 93555
- IEC (International Electrotechnical Commission)—3 Rue de Varembe, 1211 Geneva 20, Switzerland
- IEPS (International Electronic Packaging Society)—114 North Hale Street, Wheaton, IL 60187
- IPC (The Institute for Interconnecting and Packaging Electronic Circuits)—7380 N. Lincoln Ave. Lincolnwood, IL 60646
- ISHM-I/SMT (International Society of Hybrid, and Microelectronics, Interconnect and SMT Division)—Box 2698, Reston, VA 22090
- SEMI (Semiconductor Equipment and Materials—International)—805 E. Middlefield Road, Mountain View, CA 94043
- SMART (Surface-Mount and Related Technologies Group)—3 Lattimore Rd., Wheathampstead, Herts AL4 8QF, United Kingdom
- SMC (Surface-Mount Club)—British Overseas Trade Board, 1 Victoria St., London SW1H 0ET

- SMC (Surface-Mount Council—Joint ASTM/IPC/EIA/JEDEC Committee)—c/o IPC, 7380 Lincolnwood Ave., Lincolnwood, IL 60646
- SMEMA (Surface-Mount Equipment Manufacturers Association)—71 West St., Medfield, MA 02052
- SMTA (Surface-Mount Technology Association)—5200 Wilson Road, Suite 107, Edina, MN 55424
- STACK (Standard Computer Komoponenten GmbH)—5775 Wayzata Blvd #700, Minneapolis, MN 55416
- VRCI (Variable Resistive Component Institute)—c/o Bourns, Inc., 1200 Columbia Avenue, Riverside, CA 92507

DATAQUEST CONCLUSIONS

We believe that package proliferation will continue as the ASIC market develops. Many new packaging schemes will arise to meet the speed, thermal, and density requirements needed. Custom and semicustom packaging, including multichip modules using COB and TOB, will become more prevalent. Procurement of semiconductor integrated circuits will depend upon package needs and functions in addition to the basic electrical parameters of the chip. As a result, purchasers will need to specify even more details when ordering.

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Peggy Wood
Mark Giudici

Appendix A

Package Standards

PLCC	JEDEC Publication 95, MO-047AA-AH
PQFP	JEDEC Publication 95, MS-069
QFP	EIAJ Specification IC-74-4, 1986
VQPF	EIAJ Specification IC-74-4-I, 1988
TapePak	JEDEC Publication 95, MO-071
TQFP	JEDEC Publication 95, under consideration
PGA	JEDEC Publication 95, MO-083
COB	Standards not available. Use TOB guidelines.
TOB	JEDEC UO-017 and Surface Mount Council--IPC/EIA/ASTM Publication SMC-TR-001, Guideline Introduction to Tape Automated Bonding Fine Pitch Technology
Micropak	Based on DIN 15851

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Research *Newsletter*

SEMS Code: Newsletters 1989
Industry and Technology Trends
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DRAMs AND ASICs AS TECHNOLOGY DRIVERS

The topic of "DRAMs and ASICs as technology drivers" was presented at Dataquest's annual SEMICON/West'89 seminar. This newsletter presents the highlights of the presentation, which are as follows:

- Memory and ASIC markets
- Industry structure
- Semiconductor technology drivers
- DRAM technology and process equipment
- ASIC technology and process equipment
- Special ASIC process innovations
- Fab configuration
- Synergy and convergence

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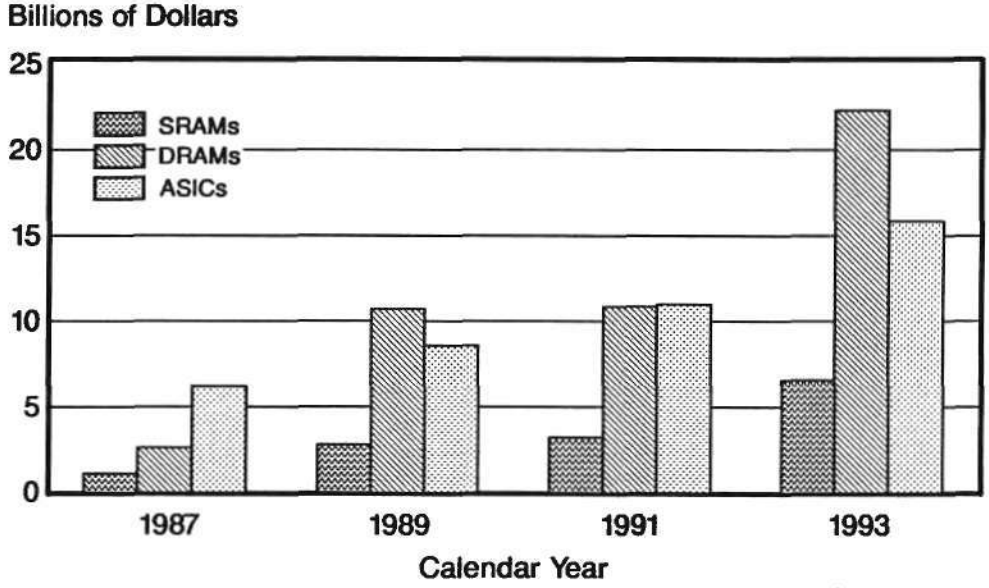
World Memory and ASIC Markets



Source: Dataquest
June 1989

Key Points:

- The world markets for DRAM, SRAM, and ASIC products are substantial and are expected to grow rapidly.

- The worldwide DRAM market is expected to grow to $22.3 billion by 1993. It is fueled by high-performance computers' insatiable demand for memory. Also, new applications for DRAMs such as fax machines, laser printers, copiers, and high-definition television (HDTV) are expected to broaden the use of DRAMs.

- Because of their ability to reduce system cost and improve system performance, ASICs will continue to gain broad acceptance in various industry segments such as computers, telecommunications, transportation, industrial, and consumer applications. The worldwide ASIC market is projected to grow to $15.9 billion by 1993.

Industry Structure

DRAMs	ASICs
Capital intensive	Customer-service intensive
Oligopolistic structure	Numerous competitors
Low product differentiation	High product differentiation
Vertically integrated companies	Small merchant companies and large captive companies
One product per technology generation	Hundreds of low-volume products for each technology generation

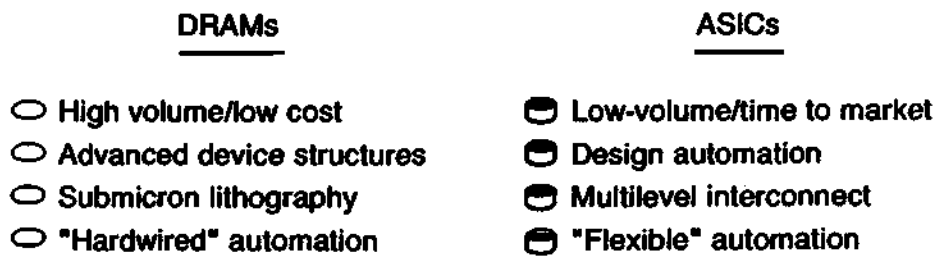
Source: Dataquest
June 1989

Key Points:

- The DRAM industry is characterized by high capital costs, which pose formidable barriers to entry for small, new companies. Only vertically integrated companies with deep pockets can absorb the huge development and plant set-up costs associated with megascale DRAM factories. DRAM manufacturers need to ramp up production quickly to gain market share and recoup their investments, so that they can migrate to the next generation of DRAM technology.

- In contrast, the ASIC industry is characterized by small to medium-size merchant companies that focus on products that are driven by time-to-market and customer-service considerations. Low entry barriers imply a proliferation of ASIC vendors that are geographically dispersed in order to be close to the customers.

Technology Drivers

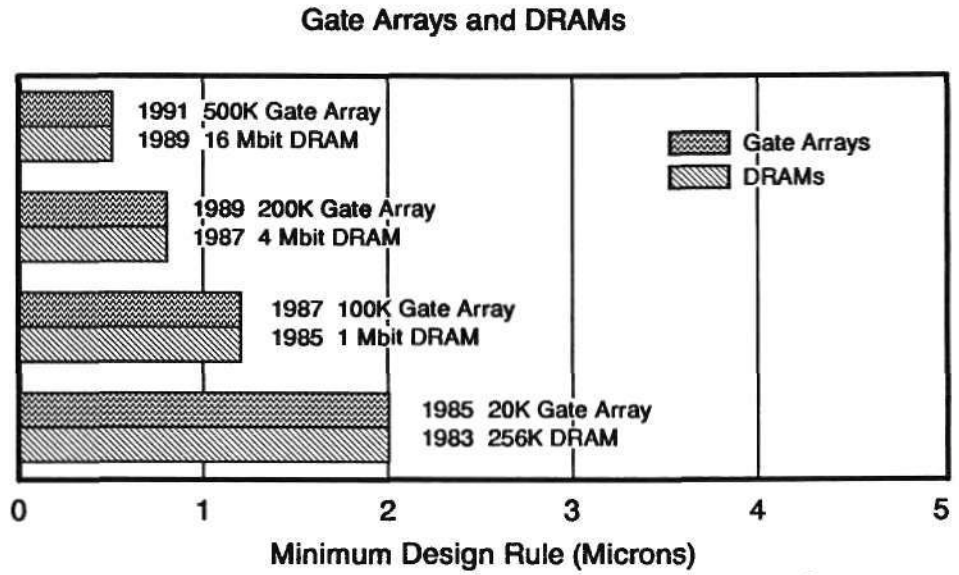


Source: Dataquest
June 1989

Key Points:

- DRAM technology drives the development of silicon device structures such as trench and stacked capacitors and submicron gate transistors with high packing density.
- ASIC technology drives multilevel interconnect technology because of the intensive random logic routing requirements of system-on-a-chip products.

Minimum Design Rules and Metal Levels



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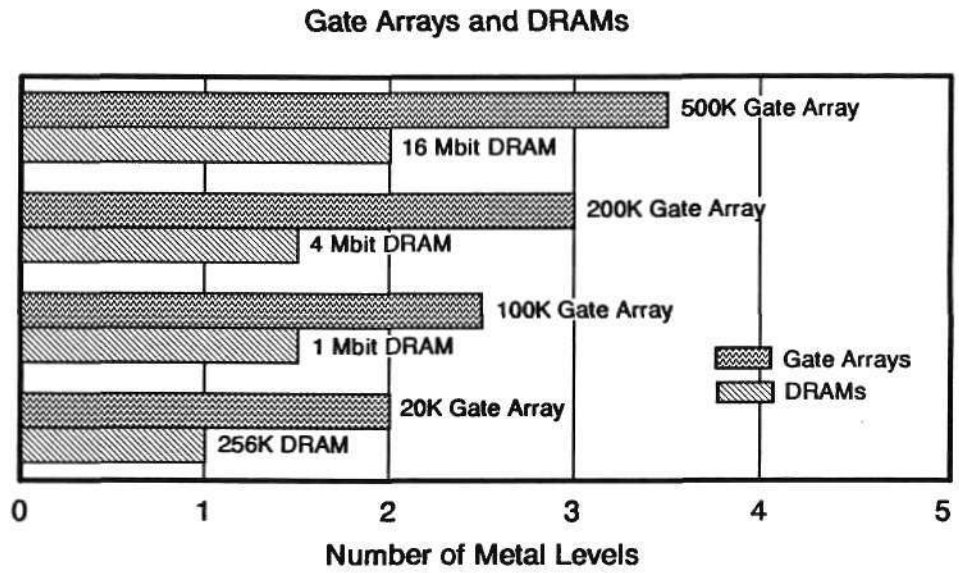

Source: Dataquest
June 1989

Key Points:

- DRAMs continue to have a two–year lead over ASICs in minimum feature size. Submicron lithography processes are first applied to DRAMs and then transferred to ASICs.

- Even though ASICs lag behind DRAMs in minimum feature size, they lead in the use of multiple levels of interconnect. ASIC technology drives advances in planarization, CVD oxides, and refractory metals such as tungsten plugs.

Typical 4Mb DRAM Technology and IBM's 4Mb DRAM

Features	Process/Equipment Needs
○ High-quality EPI	Economical EPI process?
○ Retrograde wells	High-dose/high-energy implants
○ Deep capacitor trenches	High throughput, low RIE damage
○ Stacked capacitor	Conventional etch process
○ Oxide-nitride-oxide dielectric	Vertical furnace or RTP
○ Trench refill CVD oxide	TEOS conformal CVD reactors
○ 0.8-micron gate length	Submicron capability steppers

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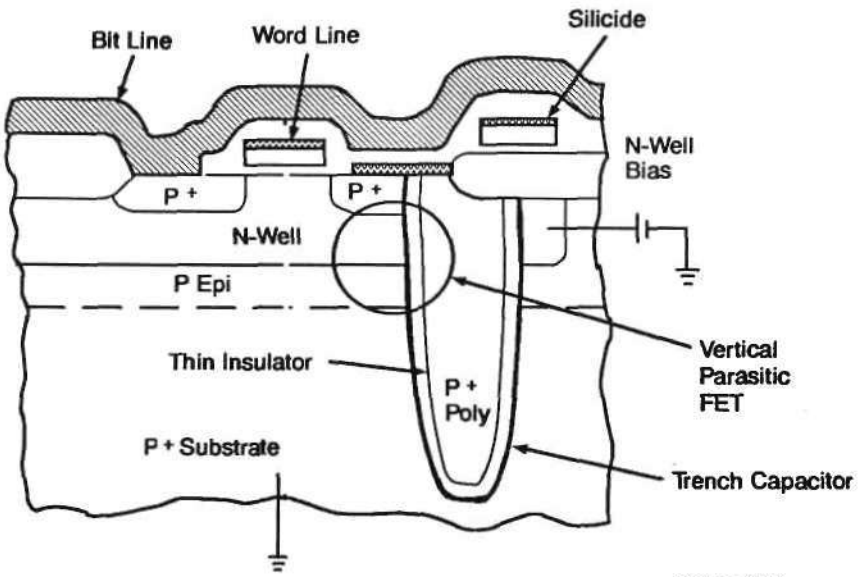
June 1989



Source: IEDM

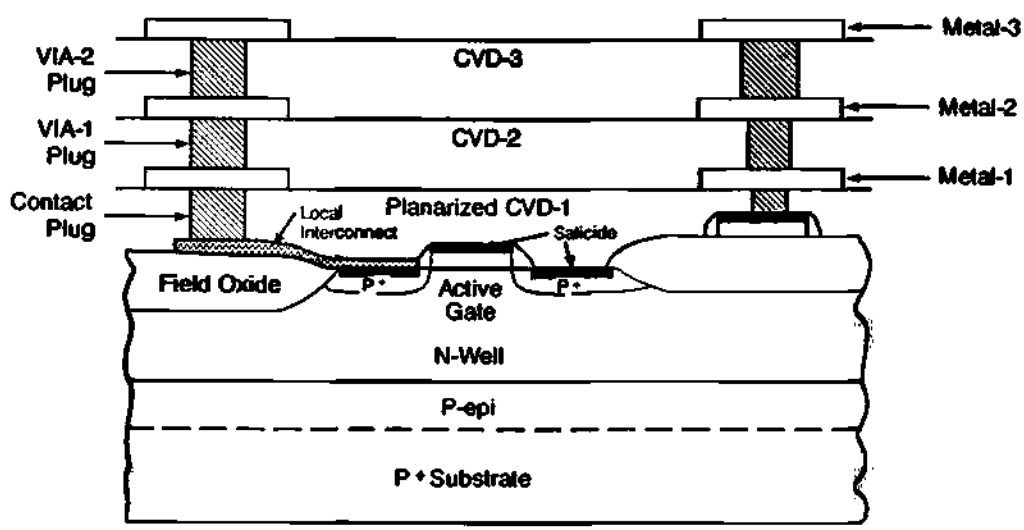
Key Points:

- DRAM technology has spurred the development of 3–D silicon structures such as trench capacitors and stacked capacitors. The etch and deposition technologies for trench formation and refill are unique to DRAM processes.
- The 4Mb and 16Mb DRAM technologies will lead in the use of high numerical aperture (NA) g–line and i–line steppers. Submicron imaging techniques, resist technology, and metrology tools will be paced by DRAM technology.

Technology for 200K Triple–Metal Gate Array

Feature	Process/Equipment Need
Salicide	RTP titanium silicide
Local interconnect	RTP titanium nitride
Planarized CVD between metals	Spin-on-glass planarization or in-situ PECVD planarization
Contact and VIA plugs	Tungsten CVD
Triple-metal interconnect	High-resolution, defect-free interconnect patterning
Custom metallization option	Flexible photoetch process
Many product configurations	Quick-turn maskmaking; good reticle management

Source: Dataquest
June 1989



Source: Dataquest
June 1989

Key Points:

- ASIC technology will lead in the use of local interconnects such as titanium nitride and self–aligned silicides such as titanium silicide. The need for multiple levels of interconnect in ASICs will drive advancements in planarization technology and new CVD processes.

- The trend toward hundreds of low–volume ASICs for each technology generation will demand quick–turn maskmaking and flexible steppers with low setup times.

ASIC Process and Equipment Innovations

- Laser-based interconnect patterning; quick-turn ASICs
- Focused ion beam tungsten direct-write interconnects
- E-beam lithography for maskless, direct-write ASICs
- Single-wafer etching and deposition systems
- Steppers with elaborate reticle management
- Multiproduct, computer-integrated manufacturing

Source: Dataquest
June 1989

Key Points:

- Companies such as LASA Industries and LASARRAY are pioneering the use of laser beams for low-volume prototype ASIC manufacturing.
- Hitachi, JEOL, Micrion, and Seiko Instruments are marketing systems for prototype ASIC repair using focused ion beams to selectively deposit and etch local interconnect patterns.
- To improve throughput time and reduce costs for low-volume products, ASIC companies such as European Silicon Structures and United Silicon Structures are using e-beam systems for direct-write patterning.

Fab Configuration

4Mb DRAM Fabs	ASIC Fabs
Maxifabs ($150M-$200M)	Minifabs ($20M-$50M)
High-volume, single product	Low-volume, multiproduct
Dedicated automation	Programmable automation
Serial "assembly line"	Autonomous lines in parallel
Fab organized by function	Fab organized by product
High throughput, dedicated steppers for each layer	Flexible steppers with low setup time
Mix of batch and single-wafer processing	Single-wafer processing equipment
	Portable/desktop fabs?

Source: Dataquest
June 1989

Key Points:

- DRAM fabs use hardwired automation to produce huge volumes of a single product economically, whereas ASIC fabs use programmable automation to respond to the needs of a dynamic, low-volume, multiproduct market.

Synergy and Convergence

- ASIC products with increasing on-chip SRAM memory
- Custom DRAMs and SRAMs for video, graphics applications
- Universal BiCMOS process for ASICs and high-speed SRAMs
- DRAM process trend toward 3-D silicon structure
- Multilevel interconnect technology now standard for ASIC and memory products
- Memory producers getting into ASIC manufacturing to balance fab capacity and offer one-stop shops
- Modular, reliable, flexible architecture equipment needed

Source: Dataquest
June 1989

Key Points:

- Several major U.S. and Japanese memory producers are setting up multipurpose fabrication plants for manufacturing DRAMs and ASICs in the same location. The objective is to balance capacity utilization by responding rapidly to changing market needs. It is important that process and equipment designs be modular and reliable so that the semiconductor manufacturer can mix and match standard modules for varying applications.

Conclusions

- DRAMs drive silicon device innovations and low-cost/high volume manufacturing
- ASICs drive design automation, multilevel interconnect technology, and flexible manufacturing
- Evolving synergy between memory (especially SRAMs) and ASIC processes
- Equipment design needs to be modular, highly reliable, and offer a "systems solution" to IC manufacturing
- Equipment and processes need to offer "open systems architecture"

Source: Dataquest
June 1989

Krishna Shankar

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Equipment and Materials
0004224

WILL THE EQUIPMENT INDUSTRY MOVE TO OPEN ARCHITECTURE?

SUMMARY

The semiconductor manufacturing equipment industry is in a state of transition. Nowhere was this more evident than at the industry's premier trade show, SEMICON/West '89, held in May. A great deal of debate occurred at the show regarding the standards for future equipment architecture. The stakes are high: participation and growth in a fast-growing capital equipment industry that fuels the bottom of the electronics industry food chain. The choice for the standard is between the rapidly growing Modular Equipment Standards Architecture (MESA) group, the Applied Materials Precision 5000 (PE5000) system, or a combination of the two. Semiconductor Equipment and Materials International (SEMI), the industry trade organization responsible for setting equipment standards, must reach a consensus among its members regarding the multichamber architecture. Dataquest believes that open and modular equipment architecture is desirable for future submicron manufacturing. Otherwise, the equipment industry will continue to offer custom solutions that do not integrate into device manufacturers' long-term strategies.

BACKGROUND

As device geometries continue their submicron push, the trend is toward using multichamber, in situ processing to minimize defects and simplify complex processes implementation. Anelva, Applied Materials, General Signal, Materials Research Corporation, Ulvac, and Varian already are shipping such multichamber systems while other companies including ASM, Electrotech, and Tegal announced similar systems at SEMICON/West '89.

Sematech recently held a workshop with SEMI/Sematech members in Dallas, Texas, to discuss multichamber system architectures. One of Sematech's goals is to foster the development of a healthy, leading-edge U.S. semiconductor equipment industry. Toward this end, it has set up the Tool Applications Shop (TAPS) facility in Austin, Texas, to develop and cooperatively evaluate new equipment. Any multichamber processes developed at Sematech for its Phase II 0.5-micron program are expected to be

reproduced by participating member companies. Two principal multichamber architectures were proposed at the Dallas workshop: Applied Materials offered to open up the PE 5000 CVD system's mechanical and wafer-handling architecture, and a group of 10 other equipment companies offered the MESA. At SEMICON/West, Sematech announced some high-level specifications for multichamber systems, but it stated unequivocally that it was not endorsing any particular architecture. Sematech defined nominal specifications for such parameters as the dimensions of the slot at the wafer-transfer interface plane, the reach of the handler into the process chamber, X-Y handler movement with a Z-option, and detachable process chamber. Details of the equipment configuration, such as batch or single-wafer process, clustered, or linear chamber access, were left to the vendor. Sematech has effectively put the ball into SEMI's court.

ANALYSIS

Just as in other high-technology industries such as personal computers and workstations, the semiconductor equipment industry is headed toward open architecture and modular components. It remains to be seen if the MESA or the Applied Materials PE5000 architecture or a combination thereof can achieve critical mass and evolve into an industry standard. Dataquest estimates that Applied Materials has an installed base of 300 PE 5000 systems. It is the market leader in CVD, etch, and epi equipment. Including ion-implant equipment, Dataquest estimated Applied's front-end equipment sales to be $360 million dollars in calendar year 1988.

Collectively, members of the MESA group wield a powerful influence. The MESA group thus far has 25 confirmed members representing $1.2 billion in sales of front-end equipment during 1988. A list of MESA group members follows.

- AG Associates
- ASM
- Balzers
- Branson/IPC
- Drytek
- Eaton
- Gasonics
- General Signal
- Genus
- Lam Research
- Materials Research
- Matrix
- Nanosil
- Novellus
- Peak Systems
- Process Products
- Prometrix
- Semiconductor Systems
- Spectrum CVD
- SVG/Thermco
- Tegal
- Varian
- Watkins-Johnson
- Xinix
- XMR

The MESA group appears to be strong, with very diversified product offerings. The MESA specification appears to conform to high-level Sematech guidelines. However, the degree of compatibility between Applied's PE 5000 and Sematech's guidelines is not clear at the present time.

DATAQUEST CONCLUSIONS

Dataquest believes that modular, open architecture is a positive benefit for the highly fragmented equipment industry. It will lower entry barriers for the small companies, which now can focus on developing and marketing process equipment modules rather than entire systems. For instance, it has been estimated that the cost of developing the I/O portions of the system (wafer handling, software) can be one-third to one-half of the total development cost. Open system architectures will allow smaller companies to use scarce R&D resources to do what they do best—develop process modules. Meanwhile, big equipment companies can leverage off a common architecture by offering integrated solutions to market areas including CVD, sputter, and etch applications. New industry players such as system-integrators, wafer-handling system manufacturers, CIM, and software vendors will emerge because of the ease of porting their offerings to the industry standard. Device manufacturers that are no longer locked into risky, capital-intensive, proprietary equipment architectures stand to reap substantial benefits from an open, competitive market environment. A device manufacturer will be free to mix and match the best systems for its unique application. Equipment vendors must reach a consensus on open architecture quickly, so that it can be standardized by SEMI for adoption by the industry and Sematech.

Krishna Shankar

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Industry & Technology Trends
0003119

HITACHI AND TI SHARE THE RISK: THE 16Mb DRAM AGREEMENT

SUMMARY

On December 22, Texas Instruments (TI) and Hitachi Ltd. announced that they had entered into an agreement to jointly develop DRAMs. Under the terms of the agreement, the two companies will create a common 16Mb DRAM technology. Implementation of the agreement will allow each company to have access to the other's DRAM technology as it relates to the development of the 16Mb device.

AN INDUSTRY FIRST

The Hitachi/TI agreement marks the first time that leading U.S. and Japanese semiconductor companies have come together to develop a future-generation memory product. The Motorola/Toshiba agreement, although equally significant, involves joint manufacturing and technology exchange related to existing products. In this sense, then, the Hitachi/TI deal has its counterpart more in the "MegaProject" agreement between Philips and Siemens, in which the two European chip manufacturers shared the development costs and technology in producing the 4Mb DRAM (Siemens) and 1Mb fast SRAM (Philips).

The semiconductor industry is certainly familiar with technology exchange as the raison d'etre of alliances. To understand the Hitachi/TI agreement, however, one must also appreciate the risks associated with the increasing capital intensiveness of leading-edge memory development. These risks are probably as great, if not greater, a factor in bringing the two companies together as is any mutual benefit to be obtained through technology swapping.

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RISK SHARING

The issue of risk concerning the 16Mb DRAM has to do with cost and timing. From the standpoint of cost, future participants in the high-density memory business face incredible investments in development and production. Equipment and clean room technology required to produce devices based on 0.5-micron linewidths is enormously expensive. At a recent meeting of a semiconductor task force hosted by the American Electronics Association (AEA), a representative of one major U.S. semiconductor manufacturer introduced a cost model that estimated a $250 million capital investment to build a 0.8-micron, 1Mb DRAM factory with throughput capability of 5,000 6-inch wafers a week. This is probably a conservative estimate to begin with.

To Dataquest's knowledge, construction of a prototype 16Mb fab will be started by NEC in Sagamihara, Japan, in the third quarter of 1989. This facility, with a probable capacity of about 5,000 6-inch wafers per four-week period, alone will cost an estimated $160 million. Eventually, companies will have to consider building the next-generation factory—a 0.8- to 0.5-micron, 8-inch wafer fab—that can produce 4Mb as well as 16Mb DRAMs. The cost of such fabs is currently estimated to be about $400 million.

Whatever reductions in development costs their agreement may achieve, both Hitachi and TI will have to build expensive fabs. By working together, however, the two companies have a better chance of coming up with a winning formula for product manufacture and, thereby, overcoming the other demon of DRAM development: timing. Any company that plans to participate in the 16Mb market, which Dataquest believes will reach approximately 2 million units in 1992, must make massive capacity investments during an industry cycle that we have forecast to be weak. If a company stumbles badly in bringing up its 16Mb DRAM production, the penalties will be serious. From this standpoint, then, the Hitachi/TI deal is not so much about sharing costs as it is about sharing expertise and resources and about minimizing individual exposure. Given the stakes in entering the 16Mb DRAM market, failure could be disastrous.

WHAT TI GETS

While risk sharing can be seen as the most powerful common denominator of the alliance, each company has some unique advantages to gain from its partner. In the case of TI, the advantages seem obvious. Hitachi is an acknowledged leader in memory technology, was the first company to introduce the 256K DRAM, and was in the top two in 1Mb DRAM introductions. Furthermore, Dataquest believes that Hitachi is a major contender, along with Toshiba, for the lead in 4Mb DRAMs. As a result of its agreement with Hitachi, TI—the seventh largest producer of 1Mb DRAMs (in units) in 1987—could be one of the leaders in the future DRAM market.

Hitachi is also a leader in BICMOS, which is a critical process for fast SRAMs as well as high-speed DRAMs. In 1987, Hitachi presented a paper at the ISSCC (International Solid State Circuit Conference) on a 35-nanosecond 1Mb DRAM utilizing BICMOS. Dataquest expects to see samples of such a device in 1989, and we further believe that this technology will be a very important process at the 16Mb DRAM density.

In addition to its expertise in memory technology, Hitachi now manufactures in TI's backyard. Hitachi has just finished equipping its Irving, Texas, fab, which is capable of producing 1.3-micron SRAMs. Future production is planned for ASIC devices and microprocessors. Although the Hitachi/TI agreement does not entail joint manufacturing, as is the case with the Motorola/Toshiba alliance, the proximity of the companies' manufacturing sites would at least make such an arrangement logistically convenient.

WHAT HITACHI GETS

With Hitachi's leading position in DRAMs, substantial capital resources, and existing manufacturing presence in the United States, the Hitachi/TI agreement raises the logical question, "What's in it for Hitachi?" Once again, the issue of risk sharing is paramount; but aside from this factor, some other possible motives are worth speculation. These include the following:

- TI's hold on fundamental DRAM patents may be a factor in the joint development effort—Hitachi was one of the Japanese memory manufacturers sued by TI in 1986 over DRAM patent violations. The companies settled out of court in 1987.

- Although the press release from the companies mentions product development beyond DRAMs, a technology swap involving TI DSP (digital signal processing) circuits could certainly be attractive to Hitachi in view of DSP's relevance to the high-definition TV market and Hitachi's growing emphasis on microdevices.

- Not knowing which way the "trade winds" will blow in the future, having a U.S. partner as well as a domestic manufacturing presence certainly cannot hurt Hitachi from a political standpoint.

HITACHI IN TRANSITION

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1983 versus 1987
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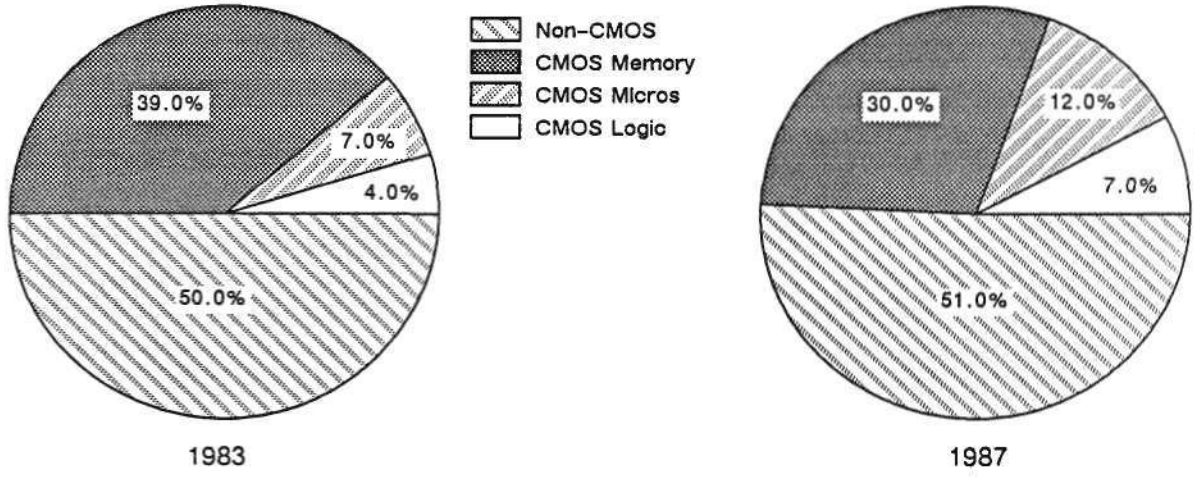

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Source: Dataquest
February 1989

Contrasted with NEC, one senses the path Hitachi must follow. In 1987, combined microdevice and logic revenue accounted for approximately 19 percent of Hitachi's semiconductor business, compared with 35 percent for NEC. Obviously, Hitachi has no plans to abdicate the memory market. Nevertheless, it will be increasingly difficult for Hitachi to continue along its present path in logic and micros while committing ever greater resources to the MOS memory side of its business.

DATAQUEST CONCLUSIONS

Dataquest has long maintained that the complexities of product mix and the escalating costs of development and manufacture at the leading edge will make it difficult for even the largest broad-based semiconductor suppliers to afford a "go it alone" attitude. Certainly, the Hitachi/TI agreement underscores this point of view. Given the costs and risks of participating in the commodity memory business of the future, it is hard to believe that this agreement will be unique.

For the U.S. electronics systems industry, the Hitachi/TI deal should send a message that the U.S. semiconductor industry is committed to the DRAM market for the long term. While the merits of having a domestic (i.e., U.S.-owned) supplier base may be debated, it must certainly be reassuring to U.S. computer manufacturers to know that at least one DRAM vendor is not a systems-level competitor.

One issue that may confront the Hitachi/TI agreement is TI's involvement with Sematech, the U.S. manufacturing consortium. There is likely to be some concern about Hitachi's possible access to Sematech-related technology. Inasmuch as the consortium is a beneficiary of its members' intellectual capital as well as a benefactor, it is possible that the technologies developed through the Hitachi/TI agreement could make a positive contribution to the U.S. semiconductor industry as a whole.

As evidenced by the deliberations of U.S. semiconductor companies over reentering the DRAM business, such a commitment cannot be made on the basis of short-term opportunism. Participation in the DRAM market must be a fundamental part of a semiconductor company's long-term strategy. Although the benefits of developing a 0.5-micron manufacturing capability will accrue to other areas of chipmaking beyond the DRAM business, investments in DRAMs cannot preclude the development of other key component areas.

As the cost of capital investment continues to rise, participation in both leading-edge commodity products and higher-margin businesses such as microdevices and ASICs will be more difficult to support. A major reason for this is that these product development paths are becoming increasingly divergent—while future DRAM generations will depend on trench and other 3-D technologies, ASICs will continue to stress CAD technology and multiple metal deposition. In spite of their differing demands, companies will have to have their feet in both worlds if they intend to be major suppliers to the data processing arena. The Hitachi/TI agreement suggests one way of meeting this challenge; and, as such, it follows a direction already indicated by the Motorola/Toshiba alliance.

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HITACHI AND TI SHARE THE RISK: THE 16Mb DRAM AGREEMENT

SUMMARY

On December 22, Texas Instruments (TI) and Hitachi Ltd. announced that they had entered into an agreement to jointly develop DRAMs. Under the terms of the agreement, the two companies will create a common 16Mb DRAM technology. Implementation of the agreement will allow each company to have access to the other's DRAM technology as it relates to the development of the 16Mb device.

AN INDUSTRY FIRST

The Hitachi/TI agreement marks the first time that leading U.S. and Japanese semiconductor companies have come together to develop a future-generation memory product. The Motorola/Toshiba agreement, although equally significant, involves joint manufacturing and technology exchange related to existing products. In this sense, then, the Hitachi/TI deal has its counterpart more in the "MegaProject" agreement between Philips and Siemens, in which the two European chip manufacturers shared the development costs and technology in producing the 4Mb DRAM (Siemens) and 1Mb fast SRAM (Philips).

The semiconductor industry is certainly familiar with technology exchange as the raison d'etre of alliances. To understand the Hitachi/TI agreement, however, one must also appreciate the risks associated with the increasing capital intensiveness of leading-edge memory development. These risks are probably as great, if not greater, a factor in bringing the two companies together as is any mutual benefit to be obtained through technology swapping.

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RISK SHARING

The issue of risk concerning the 16Mb DRAM has to do with cost and timing. From the standpoint of cost, future participants in the high-density memory business face incredible investments in development and production. Equipment and clean room technology required to produce devices based on 0.5-micron linewidths is enormously expensive. At a recent meeting of a semiconductor task force hosted by the American Electronics Association (AEA), a representative of one major U.S. semiconductor manufacturer introduced a cost model that estimated a $250 million capital investment to build a 0.8-micron, 1Mb DRAM factory with throughput capability of 5,000 6-inch wafers a week. This is probably a conservative estimate to begin with.

To Dataquest's knowledge, construction of a prototype 16Mb fab will be started by NEC in Sagamihara, Japan, in the third quarter of 1989. This facility, with a probable capacity of about 5,000 6-inch wafers per four-week period, alone will cost an estimated $160 million. Eventually, companies will have to consider building the next-generation factory—a 0.8- to 0.5-micron, 8-inch wafer fab—that can produce 4Mb as well as 16Mb DRAMs. The cost of such fabs is currently estimated to be about $400 million.

Whatever reductions in development costs their agreement may achieve, both Hitachi and TI will have to build expensive fabs. By working together, however, the two companies have a better chance of coming up with a winning formula for product manufacture and, thereby, overcoming the other demon of DRAM development: timing. Any company that plans to participate in the 16Mb market, which Dataquest believes will reach approximately 2 million units in 1992, must make massive capacity investments during an industry cycle that we have forecast to be weak. If a company stumbles badly in bringing up its 16Mb DRAM production, the penalties will be serious. From this standpoint, then, the Hitachi/TI deal is not so much about sharing costs as it is about sharing expertise and resources and about minimizing individual exposure. Given the stakes in entering the 16Mb DRAM market, failure could be disastrous.

WHAT TI GETS

While risk sharing can be seen as the most powerful common denominator of the alliance, each company has some unique advantages to gain from its partner. In the case of TI, the advantages seem obvious. Hitachi is an acknowledged leader in memory technology, was the first company to introduce the 256K DRAM, and was in the top two in 1Mb DRAM introductions. Furthermore, Dataquest believes that Hitachi is a major contender, along with Toshiba, for the lead in 4Mb DRAMs. As a result of its agreement with Hitachi, TI—the seventh largest producer of 1Mb DRAMs (in units) in 1987—could be one of the leaders in the future DRAM market.

Hitachi is also a leader in BICMOS, which is a critical process for fast SRAMs as well as high-speed DRAMs. In 1987, Hitachi presented a paper at the ISSCC (International Solid State Circuit Conference) on a 35-nanosecond 1Mb DRAM utilizing BICMOS. Dataquest expects to see samples of such a device in 1989, and we further believe that this technology will be a very important process at the 16Mb DRAM density.

In addition to its expertise in memory technology, Hitachi now manufactures in TI's backyard. Hitachi has just finished equipping its Irving, Texas, fab, which is capable of producing 1.3–micron SRAMs. Future production is planned for ASIC devices and microprocessors. Although the Hitachi/TI agreement does not entail joint manufacturing, as is the case with the Motorola/Toshiba alliance, the proximity of the companies' manufacturing sites would at least make such an arrangement logistically convenient.

WHAT HITACHI GETS

With Hitachi's leading position in DRAMs, substantial capital resources, and existing manufacturing presence in the United States, the Hitachi/TI agreement raises the logical question, "What's in it for Hitachi?" Once again, the issue of risk sharing is paramount; but aside from this factor, some other possible motives are worth speculation. These include the following:

- TI's hold on fundamental DRAM patents may be a factor in the joint development effort—Hitachi was one of the Japanese memory manufacturers sued by TI in 1986 over DRAM patent violations. The companies settled out of court in 1987.

- Although the press release from the companies mentions product development beyond DRAMs, a technology swap involving TI DSP (digital signal processing) circuits could certainly be attractive to Hitachi in view of DSP's relevance to the high–definition TV market and Hitachi's growing emphasis on microdevices.

- Not knowing which way the "trade winds" will blow in the future, having a U.S. partner as well as a domestic manufacturing presence certainly cannot hurt Hitachi from a political standpoint.

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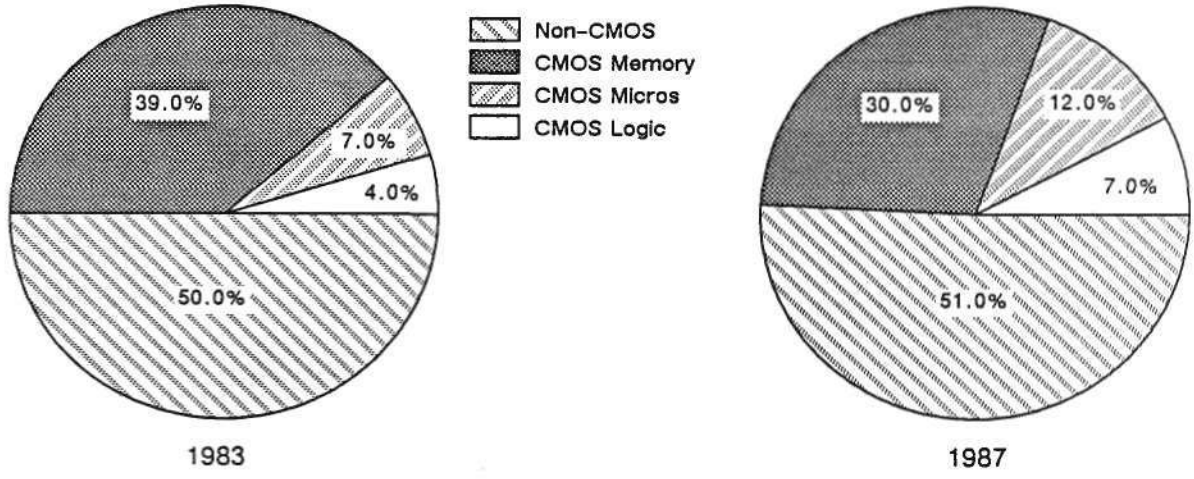

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A SAMPLING OF SUB–1.5–MICRON DEVICES JULY THROUGH DECEMBER 1988

INTRODUCTION

This newsletter lists the new commercial products with line geometries of 1.5 microns or below that were announced from July through December 1988. For the most part, the products are either being sampled or in production. (Although the list is not the result of a thorough literature search, Dataquest believes that it represents a fair cross section of sub–1.5–micron products introduced during the six–month period.) The intent of this newsletter is to provide our clients with a barometer of the changes occurring in fabrication technology, along with an idea of the types of leading–edge products entering production.

Table 1 summarizes the number of new product introductions by linewidth. (A product family, such as an ASIC family, is considered a single product.) Of the 99 new products listed in this newsletter, 37 percent are (or will be) fabricated with 1.5–micron linewidths, while 63 percent are fabricated with 1.3 microns or less. Thirty–eight percent of the new products are fabricated with 1–micron or lower linewidths, and 16 percent are fabricated with submicron geometries. Figure 1 illustrates the breakdown by linewidth and category of the 99 new products.

Figure 2 shows how the number of new products for July through December 1988 compares with the number for March through June 1988. (See SEMS Newsletter 1988–23, entitled "A Sampling of Sub–1.5–Micron Devices, March Through June 1988.") Note that for both periods, 37 percent of the products introduced are fabricated with 1.5–micron linewidths; however, there is a definite shift toward smaller geometries in the later period. In the previous period, 29 percent of the products were introduced at 1.1–micron geometries or below, while in the latest period, the figure has grown to 38 percent.

Table 2 lists the 38 new products that have linewidths of 1 micron or lower and the companies that will manufacture the products.

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Table 1

Number of New Products by Linewidth (Microns)

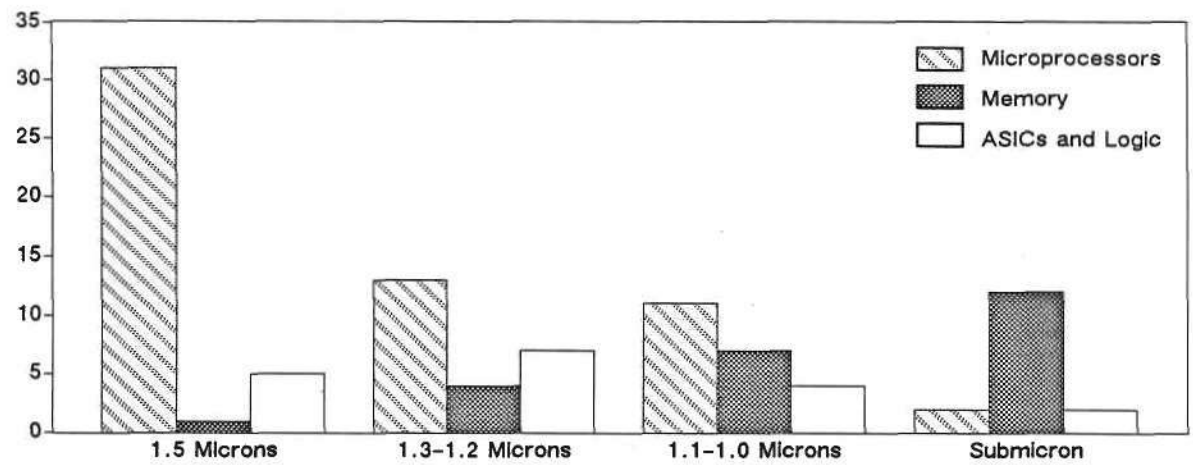
Product Category	1.5	1.3-1.2	1.0	Submicron	Total
Microprocessor Products	31	13	11	2	57
Memory Products	1	4	7	12	24
ASIC and Logic Products	5	7	4	2	18
Total	37	24	22	16	99
Percent of Total	37%	24%	22%	16%	100%

Note: Columns may not add to totals shown because of rounding.

Source: Dataquest
February 1989

Figure 1

Number of New Products by Linewidth and Product Category (July–December 1988)



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Source: Dataquest
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Figure 2

Number of New Products by Linewidth and Time Period

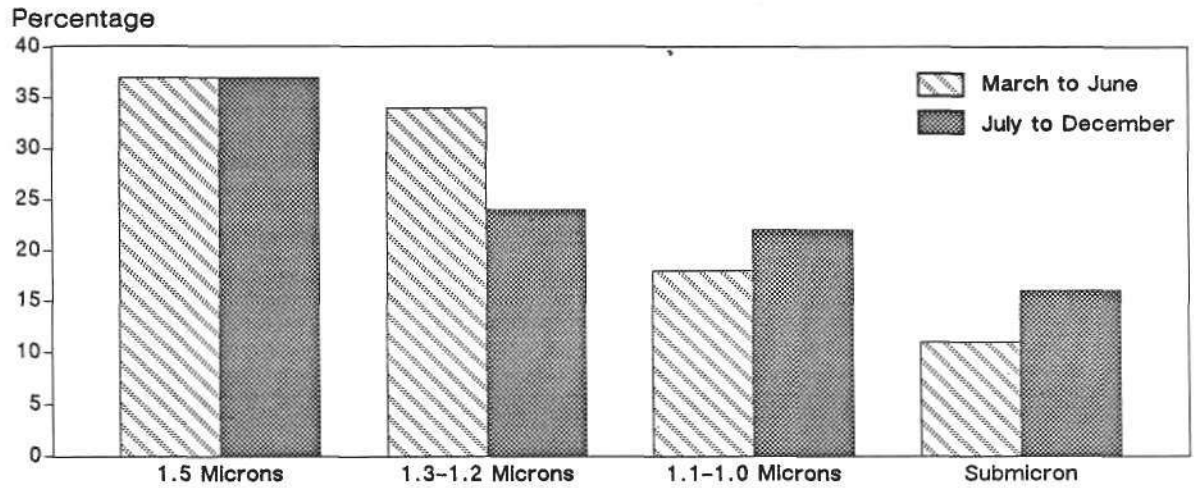

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Table 2

1–Micron and Submicron Devices

Company	Linewidth (Microns)	Device Type
Microprocessors		
Fujitsu	1.0	32-bit TRON MPU
Hitachi	1.0	32-bit TRON MPU
LSI Logic	1.0	RISC MPU
Mitsubishi	1.0	32-bit TRON MPU
Texas Instruments	1.0	Communications coprocessor
Texas Instruments	1.0	RISC DSP
Texas Instruments	1.0	32-bit interface controller
Texas Instruments	1.0	Palette-DAC
Toshiba	1.0	32-bit TRON MPU
TRW	1.0	Integer divider
Weitek	1.0	64-bit FPUs
AT&T	0.75	16-bit DSP
AT&T	0.75	DSP

(Continued)

Table 2 (Continued)

1–Micron and Submicron Devices

Company	Linewidth (Microns)	Device Type
Memory		
Intel	1.0	256K EPROMs
Mitsubishi	1.0	Fast 256K SRAMs
NEC	1.0	4-Mbit EPROM
Siemens	1.0	1-Mbit DRAM
S-MOS	1.0	Fast 256K SRAMs
Toshiba	1.0	Fast 64K SRAMs
Toshiba	1.0	Fast 8K x 9 SRAM
Cypress Semiconductor	0.8	Fast 64K SRAMs
Cypress Semiconductor	0.8	Fast 4K SRAM
Cypress Semiconductor	0.8	Fast 128K SRAM
Hitachi	0.8	4-Mbit DRAM
NEC	0.8	16-Mbit ROM
Waferscale Integration	0.8	1-Mbit EPROM
Waferscale Integration	0.8	512K EPROM
Waferscale Integration	0.8	256K EPROM
Performance Semiconductor	0.7	Fast 4K SRAMs
Performance Semiconductor	0.7	Fast 16K SRAMs
Performance Semiconductor	0.7	Fast 64K SRAMs
NEC	0.55	16-Mbit DRAM
ASIC/Logic		
Altera	1.0	EPLD
LSI Logic	1.0	Gate arrays
VLSI Technology	1.0	Gate arrays
VLSI Technology	1.0	Standard cells
Altera	0.8	EPLD
Vitesse	0.8	GaAs gate array

Source: Dataquest
February 1989

NEW PRODUCTS

Microprocessor, Microcontroller, and Peripheral Products

The following microprocessor, microcontroller, and peripheral products were introduced between July and December 1988:

- Japan's 32-bit Gmicro TRON microprocessors are beginning to hit the market. Hitachi is sampling its Gmicro 200 (700,000 transistors); Fujitsu will began sampling its 900,000-transistor chip, the Gmicro 300 in the spring of 1989; and Mitsubishi is scheduled to begin sampling its 300,000-transistor Gmicro 100 chip, also in the spring of 1989. In addition, Toshiba is working on a 400,000-transistor chip called the TX1. All four devices are fabricated with a 1-micron CMOS process. (12/26/88)

- AT&T has available the DSP32C intended for use in graphics, telecommunications, and speech recognition systems. The device has more than 400,000 transistors and is fabricated with a 0.75-micron, double-metal CMOS process. (12/12/88)

- Hitachi is sampling the H8 532 8-bit microcontroller, which has 32K of EPROM and a 200ns instruction execution time. The device, the first in Hitachi's H8 family, is fabricated with a 1.3-micron CMOS process and is scheduled to be in full production by April 1989. (12/12/88)

- TRW has introduced an integer divider for use in radar systems, workstations, and imaging systems. The TMC3211 performs at 20 million operations per second; it is fabricated with TRW's 1-micron CMOS Omnicron process. (12/12/88)

- Data Translation has entered the chip business with its MicroChannel interface chip designed for use in its line of add-in boards for IBM's PS/2 computers. The device, manufactured by LSI Logic, is fabricated with a 1.5-micron CMOS process. (12/12/88)

- SGS-Thomson Microelectronics has introduced two families of 8-bit microcontrollors, the ST62XX and ST63XX. The devices are fabricated with a 1.5-micron CMOS process. (12/5/88)

- NSI Logic has introduced an advanced video controller, the EVC-415A, and a companion video palette DAC, the PS00004, for implementing VGA-compatible subsystems. Both devices are fabricated with a 1.5-micron CMOS process. (12/5/88)

- Advanced Micro Devices has introduced a single-chip 32-bit floating-point processor. The Am29C325 device is fabricated with a 1.2-micron CMOS process. (12/5/88)

- Texas Instruments (TI) has introduced its single-chip communications coprocessor for implementing a 16-Mbps token-ring local area network (LAN). The TMS380C16 chip is fabricated with TI's 1-micron CMOS EPIC process. The chip is sampling now, with full production expected in mid-1989. (12/5/88)

- Austek Microsystems is sampling the A41102 frequency domain processor, capable of real-time fast Fourier transforms for spectral analysis of speech, radar, and sonar signals. The device is fabricated with a 1.5-micron CMOS process. (11/28/88)

- LSI Logic has begun shipping its new RISC chip set, which consists of the LR3000 32-bit microprocessor, LR3010 floating-point accelerator, and LR3020 write buffer. Available in 16.7 MHz and 25 MHz, the LR3000 CPU is fabricated with a 1-micron CMOS process. (11/21/88)

- Fujitsu has introduced a 25-MHz memory management unit (MMU) for its S-25 Sparc RISC microprocessor. The MB86920 MMU is fabricated with a 1.2-micron CMOS technology. The device is available in sample quantities with production volumes expected in January 1989. (11/21/88)

- Weitek has introduced faster versions of its WTL3164 and WTL3364 64-bit floating-point processors that were originally introduced earlier this year. The devices, previously fabricated with a 1.25-micron process that allowed 100ns speeds, will now be fabricated with a 1-micron process to obtain speeds as fast as 50ns. (11/14/88)

- G-2 Inc. has introduced a 80386SX-compatible chip set, the GCK101SX, which allows designers to build a 80386SX system with nine chips. The GCK101SX, a three-chip set fabricated with a 1.5-micron HCMOS process, is being sampled currently; production is scheduled for the first quarter of 1989. (11/7/88)

- NCR has introduced its 90C98 Arcnet LAN chip, which combines the functions that were previously contained on the 90C26 and 90C32 chips. The device is fabricated with a 1.5-micron CMOS process. Samples will be available in December, with production scheduled for February 1989. (11/7/88)

- Fujitsu is beginning production volume on its second-generation version of the SPARC RISC microprocessor. The S-25 is a standard cell implementation of the SPARC architecture and is fabricated with a 1.2-micron CMOS process. (10/10/88)

- Oki Semiconductor is offering the MSM699210 DSP, a 1.5-micron upgraded version of the 2-micron MSM6992 DSP. The MSM699210 will eventually shrink to a 1.2-micron process and then to a 1-micron process by the end of 1989. (10/17/88)

- AT&T is sampling the WE DSP16A 16-bit DSP device that AT&T claims is the fastest 16-bit DSP on the market, with an instruction execution time of 33ns and a 30-mips performance. The chip is fabricated with a 0.75-micron, double-metal CMOS process. (10/10/88)

- Edsun Laboratories will sample early in 1989 an improved color palette DAC that will make a standard PC monitor look like a high-resolution graphics screen. Production is scheduled for the second quarter of 1989, and the chip will be fabricated with a 1.5-micron, double-metal CMOS process. (10/3/88)

- Chips and Technologies has introduced a six-device chip set intended for the 80286- and 80386SX-based laptop computers. This chip set is offered in two versions for the different microprocessors, and all devices are fabricated with a 1.5-micron CMOS process. (9/26/88)

- Texas Instruments is now sampling the TMS320C30 digital signal processor. Employing RISC architecture, it is capable of 33 Mflops and can execute instructions in 60ns. The chip integrates 700,000 transistors and is fabricated with TI's 1.0-micron EPIC CMOS process. (9/19/88)

- Vadem will sample in November the VG-501 and VG-502 chip set that was developed in conjunction with Intel. The two chips consolidate peripheral functions for the 80C186-based PC XT and PS/2 Model 30 compatible systems. VLSI Technology will manufacture the chip set using a 1.5-micron, double-metal CMOS process. (9/19/88)

- NEC will begin sample shipments of a 122ns DSP in October. The uPD77220 will be fabricated with a 1.2-micron CMOS process; volume shipments will begin in the spring of 1989. (9/13/88)

- Advanced Hardware Architectures has developed a codec chip that can operate at 15 Mbytes per second. The company was spun off last March from the University of Idaho's Microelectronic Research Center, which conducted research on the chip. The AHA4510 chip is fabricated with a 1.2-micron CMOS process, and shipments will begin in October. (9/12/88)

- Matsushita has developed the MN8605, a modem chip for 9,600-bps facsimile transmission. The chip will be fabricated with a 1.5-micron, double-poly, double-metal CMOS process. Volume production will start in the fall of 1988. (9/1/88)

- Texas Instruments is sampling a standard NuBus interface chip set designed to be used in add-in boards for Apple's Macintosh II system and other 32-bit computers using NuBus. The chip set includes the SN74ACT2440 32-bit interface controller and the SN74BCT2420 16-bit address/data transceiver. The 2440 device is fabricated with TI's 1-micron CMOS EPIC process; the 2420 is fabricated with a BICMOS process. Volume production is scheduled for October. (8/29/88)

- Toshiba will sample a 32-bit MPU in December. The TX1 microprocessor, based on the Tron architecture, is its first development in the Tron project. The TX1 is fabricated with a 1-micron process and has 450,000 transistors on a 10.89mm x 10.27mm chip. Average operating speed is 5 mips; at maximum speed, it can perform 12.5 mips at a clock speed of 25 MHz. (8/29/88)

- Samsung has introduced two CMOS DRAM controllers, the KS84C21 and KS84C22. Each controls both 256K and 1-Mbit DRAMs; in addition, the KS84C22 can control 4-Mbit DRAMs. The chips will be fabricated with a 1.2-micron process at Samsung's San Jose, California, facility. (8/15/88)

- Advanced Micro Devices has introduced its first family of CMOS graphics peripheral circuits. The Am81C458 color palette chip (or P-DAC) is fabricated with a 1.2-micron process, which is the same process that AMD uses on its Am29000 family. The chip can support displays up to 1,280 x 1,024 pixels and run at pixel rates up to 125 MHz. The device is being sampled now with volume production scheduled for September. (8/15/88)

- Yamaha has introduced the YM7109 modem chip, which is designed for use with 9,600-baud fax systems. The device is fabricated with a 1.2-micron CMOS process, and sampling will begin in September. (8/15/88)

- Texas Instruments is designing a P-DAC, that will run from 37.5 MHz to 125 MHz. The chip will be fabricated with a 1-micron CMOS process. (8/8/88)

- Intel is sampling the 87C75PF Port Expander device, which is used with 16-MHz 8-bit microcontrollers such as the 8051 and 80C51 series. The Port Expander is for use with embedded controllers that have tight constraints on board space; consequently, it combines on one chip several functions such as two microcontroller I/O ports, interface and logic circuitry, and 32-Kbits of EPROM memory. The device is fabricated with a 1.2-micron CHMOS process and will be in volume production in October. (8/8/88)

- Cypress is shipping the first two members of a family of 16-bit microprocessors, the CYC9116-45JC and CYC9116-45DC, that have been optimized for peripheral controller applications such as disk controllers, graphics controllers, communications controllers, and modems. The devices are fabricated with a 1.2-micron CMOS process. (7/25/88)

- LSI Logic's affiliate, G-2, has entered into an agreement with Groupe Bull of France to manufacture an IBM PS/2 compatible chip set. The chip set includes the GC181 CPU bus controller, the GC182 memory controller, the GC183 DMA controller, the GC184 address-data buffer, and the GC186 peripheral controller. The 20-MHz chip set, which will be sampled in the third quarter of 1988, will be fabricated with a 1.5-micron (1.2-micron effective) CMOS process. (7/25/88)

- NEC is offering five ISDN devices fabricated with a 1.5-micron CMOS process. The uPD72305, uPD72107, and uPD98001 devices are now in production; samples of the uPD72307 and uPD98201 are available with full production scheduled for the third quarter of 1988. (7/11/88)

Memory Products

Memory products introduced between July and December 1988 include the following:

- NEC has a prototype 16-Mbit DRAM with an access time of 55ns and measurement of 8.2mm x 15.9mm. The chip is fabricated with a 0.55-micron CMOS process. (12/26/88)

- NMB Semiconductor has introduced fast 1-Mbit DRAM with access times as low as 60ns. The devices, offered in 1Mx1 and 256Kx4 configurations, will be fabricated with a 1.2-micron process. Volume production is scheduled for the second quarter of 1989. (12/19/88)

- Logic Devices has entered the static RAM market with a family of seven fast 64K SRAMs with access speeds down to 20ns. The parts are fabricated with a 1.5-micron CMOS process and will be produced at the company's foundries in the United States and Japan. (12/19/88)

- Hitachi has begun sampling its 4-Mbit DRAM to a select group of worldwide customers. The chip is fabricated with a 0.8-micron CMOS process using stacked capacitor cells. Large volume availability is expected by 1990. (12/12/88)

- Intel is offering two new 256K EPROMs, the 27C202 and 27C203 devices, which provide zero wait state performance for 32-bit microprocessors. The 27C202 has a 70ns access time, while the 27C203 has a 45ns address setup time. The devices are fabricated with Intel's 1-micron CHMOS III-E process. Samples are available now, with volume production set for the first quarter of 1989. (12/12/88)

- Performance Semiconductor has available a series of fast 4K, 16K, and 64K CMOS SRAMs fabricated with its 0.7-micron gate length, double-metal PACE II process. Performance claims that, at 10ns for the 4K and 64K (64Kx1) parts and 15ns for the 16K and 64K (8Kx8, 16Kx4) parts, they are the world's fastest SRAMs. (12/5/88)

- Xicor is sampling a 1-Mbit EEPROM device, which Xicor claims is the industry's first monolithic 1-Mbit EEPROM. The X28C010 is fabricated with a 1.2-micron CMOS process and measures 359 mm^2. Volume production is scheduled for mid-1989. (11/28/88)

- Toshiba has introduced three fast 64K SRAMs (TC5588, TC55416, and TC55417) and an 8Kx9 memory chip with parity (TC5589). All four chips have access times as low as 15ns. The devices are fabricated with a 1-micron CMOS process with different aluminum masks added to the base die to create the final memories. (11/28/88)

- Siemens has upgraded its 1-Mbit DRAM technology from a 1.2-micron N-well process to a 1.0-micron double-well process, allowing a 15 percent reduction in chip size. Chip size has been reduced from 55 mm^2 to 47 mm^2. The devices are manufactured in Siemens' Mega facility at Regensburg, West Germany. Siemens also has begun sampling 4-Mbit DRAM devices based on a 1.0-micron process as well. The 4-Mbit devices will be manufactured at Perlach, West Germany. (11/21/88)

- Cypress Semiconductor will have available in mid-1989 samples of the CY7C184 128K cache RAM that it is designing in conjunction with Compaq Computer. The CY7C184 will have speeds of 25ns and will be fabricated with a 0.8-micron CMOS process. (10/31/88)

- Cypress Semiconductor is offering a 12ns 4K SRAM intended for cache tag applications. The CY7C150 is fabricated with a 0.8-micron CMOS process. (10/17/88)

- S-MOS is offering the SRM21256 and SRM22256 256K SRAMs that range in speed from 35ns to 70ns. The devices are fabricated with a 1-micron CMOS process. (10/17/88)

- Mitsubishi has introduced three fast 256K SRAMS that have access times of 25ns, which Mitsubishi claims is the fastest in the industry. The M5M5257A, M5M5258A, and the M5M5260A are designed with CMOS peripheral logic technology and an NMOS memory array. The devices are fabricated with a 1-micron process that will be shrunk to 0.8 micron to gain even faster access times. (10/3/88)

- NEC has introduced the uPD23C16000CZ 16-Mbit ROM chip that has an access time of 200ns. The chip, which is fabricated with a 0.8-micron CMOS process, measures 8.49mm x 17.09mm. Production is scheduled for the fourth quarter of 1988. (9/14/88)

- Cypress has introduced a lineup of 20ns 64K SRAMs fabricated with a 0.8-micron CMOS process. The lineup includes the CY7161, CY7162, CY7164, CY7166, CY7185, CY7186, and CY7187 64K SRAMs. (8/22/88)

- NEC will begin sampling a 150ns 4-Mbit EPROM this month. The device, which is the first 4-Mbit EPROM to be sampled, is configured 512Kx8 and will be produced with a 1.0-micron CMOS process. Volume production is scheduled for January 1989. (8/1/88)

- Waferscale Integration is sampling a new family of EPROMs that includes the WS27C010L 1-Mbit device with an access time of 100ns, the WS27C512L 512K device, and the WS27C256L 256K device; the latter two devices both have access speeds of 90ns. The devices are fabricated with a 0.8-micron, split-gate CMOS process that uses a single transistor cell. (7/25/88)

- Integrated Device Technologies has introduced a new family of dedicated FIFO memories. The IDT72131 and IDT72141 FIFOs are for bidirectional serial data communications applications and read in parallel data and read out serial data. The IDT72142 and IDT72132 FIFOs are for serial-to-parallel applications and are intended for tape-drive controllers, hard-disk controllers, and CD-ROM drive controllers. All devices have a shift rate of 50 MHz and an access time of 35ns. They will be fabricated with a 1.2-micron CMOS process. Depending on the part number, sampling will begin either in August or September. (7/25/88)

- Atmel is offering a 70ns 256K EEPROM fabricated with a 1.25-micron (previously reported in SEMS Newsletter 1988-23 as a 1-micron process), double-metal CMOS process. The device, called the AT28HC256, is produced at a Japanese facility. (7/11/88)

ASIC and Logic Products

ASIC and logic products introduced between July and December 1988 include the following:

- Altera is sampling the EP1810, a new version of its EP1800 erasable programmable logic device (EPLD) that operates 50 percent faster than the EP1800. The chip is manufactured with a 1-micron CMOS process. Volume production is scheduled for the first quarter of 1989. (12/26/88)

- United Technologies Microelectronics Center has a new series of gate arrays with gate counts of up to 11,000 usable gates and typical gate delays of 630ps. The devices are fabricated with a 1.5-micron (1.2-micron effective channel length) CMOS process. (12/26/88)

- Plessey Semiconductors is offering a 50,000-gate MEGACELL, which is fabricated with a 1.5-micron CMOS process. (12/12/88)

- Altera is sampling the EPM5032 EPLD logic device, which is the first of many devices that will be based on Altera's MAX (multiple array matrix) architecture. Altera says that the EPM5032 packs more logic than any other programmable logic device (PLD), as it achieves nearly six times the density of popular PLDs. The chip is fabricated with a 0.8-micron CMOS EPROM technology. (11/21/88)

- Vitesse has introduced the VSC10000 gallium arsenide gate array that is intended to compete with ECL gate arrays. The VSC10000 operates at speeds up to 1.2 GHz at one-half to one-third the power of ECL devices; typical gate delays are 100ps. The device is manufactured with an 11-mask process that features 0.8-micron gate length with four layers of metal. Device size is 335 mils x 280 mils; ECL gate arrays are about 20 to 30 percent larger. Power consumption of the VSC10000 is 5 to 12 watts compared with 10 to 30 watts for ECL devices. (11/21/88)

- LSI Logic has introduced a new cell-based ASIC CMOS technology, the LCB007, that is capable of integrating 200,000 equivalent gates on a single chip. The LCB007 will be fabricated with a 1-micron gate length (0.7-micron effective channel length). LCB007 wafers will be manufactured at LSI Logic's facilities in California, Japan, and England. The design library will be made available by the end of 1988, and first customer samples will be shipped by mid-1989. The LCB007 technology will allow the incorporation of up to 144 Kbits of fast SRAM and 1 Mbit of ROM on the chip. (11/14/88)

- VLSI Technology is now accepting orders for its new VGT300 gate array family and VSC300 standard cell family. The VGT300 series has gate counts ranging from 28,090 to 243,360 available gates, with estimated gate utilization of between 30 and 40 percent, and the VSC300 series has usable gate counts of up to 150,000. Both families are fabricated with a 1-micron (effective channel length of 0.85 micron), double-metal CMOS process. The 1-micron process is presently being used at VLSI's San Jose, California, facility and will be transferred to the San Antonio, Texas, facility by mid-1989. VLSI is developing the next family of ASIC products, which will be 0.8-micron, triple-metal devices. (10/31/88)

- Oki Semiconductor is offering a new channeled gate array family with densities up to 30,000 usable gates and a new standard cell family with densities up to 60,000 gates and speeds of 600ps. Both families are fabricated with a 1.2-micron CMOS process. (10/24/88)

- Sony has introduced a fast ECL 200-gate-array chip that rivals similar gallium arsenide chips in speed and power. The E3G200 has toggle frequencies on the order of 2.5 GHz, a typical gate delay of 150ps, and a power dissipation of less than 1 watt. The chip is fabricated with a 1.2-micron, double-metal bipolar process. Sony plans to release 1,000-gate and 2,000-gate versions in July 1989. (9/19/88)

- Motorola is designing gate-array-based interface chips for use in laser printers. The chips will contain a core of the 68000 microprocessor and the dedicated laser printer functions. The LPC-1 will have 5,000 gates and will be fabricated with a 2-micron CMOS technology, while the ALPC-1 will have 16,000 gates and will be the first commercial application of Motorola's HDC series of 1-micron CMOS channelless architecture gate arrays. The LPC-1 is currently available in sample quantities; samples of the ALPC-1 will be available in December, with volume production scheduled for February 1989. (9/5/88)

- Toshiba is offering the TC23SC series standard cell library available from 700 to 50,000 gates and with typical gate delays of 1.0ns. The family is fabricated with a 1.5-micron, double-metal HC^2MOS process. (8/29/88)

- General Electric Solid State has added the CGA10 and CG100 series of continuous-gate arrays to its ASIC offerings. The CGA10 series, ranging from 1,590 gates to 10,648 gates, is fabricated with a 2-micron CMOS process; the CG100 series, ranging from 12,149 gates to 66,550 gates, is fabricated with a 1.5-micron CMOS process. The two families are alternate sources for VLSI Technology's VGT10 and VGT100 families. (8/8/88)

- General Electric's Microelectronics Center is offering a 1.25-micron CMOS gate array family fabricated with a VHSIC I process. The AGC40000 family consists of arrays of 1,750 gates, 6,246 gates, and 13,600 gates. The family, which will also be available in rad-hard CMOS, has a typical gate delay of 0.685ns for a two-input NAND gate. (8/1/88)

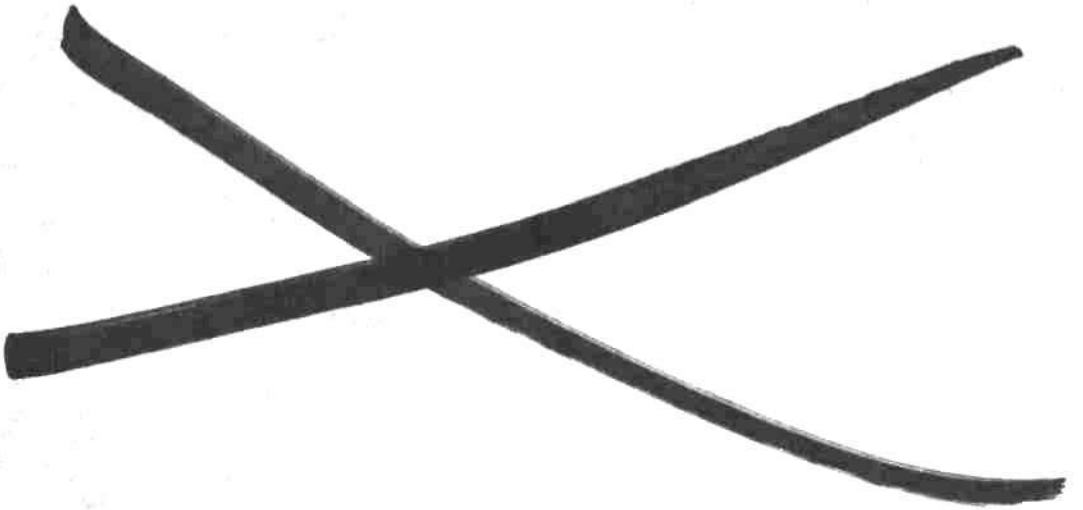
- Atmel has introduced the AT2500, a 2500-gate EPROM-based PLD that can run at 40 MHz. The device, fabricated with a 1.2-micron CMOS process, is being sampled now; full production is scheduled for August. (7/25/88)

- Advanced Micro Devices and Seeq are shipping a jointly developed electrically erasable PAL device. The PALC20RA10Z is built with a double-poly, single-metal 1.2-micron CMOS process. Initially, it will be fabricated only by Seeq, with assembly and test being done by AMD. This is also the first E^2 CMOS product that AMD will be shipping. (7/25/88)

- NEC is taking designs on the uPD65000 series of gate arrays, which range from 858 gates to 5,632 gates. Gate utilization is about 95 percent, and propagation delays average 10ns. The family is fabricated with NEC's 1.5-micron CMOS 4L process. (7/11/88)

- Samsung has begun shipping four parts of its CPL20 PLD family, which has a propagation delay of 25ns. The CPL24 family, which has a delay of 35ns, will begin shipping in August. Both families are manufactured with a 1.2-micron CMOS process at Samsung's Santa Clara, California, facility. (7/4/88)

Joseph Grenier



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Research Newsletter

SEMICON/WEST 1989: TAKING THE PULSE OF THE EQUIPMENT INDUSTRY

INTRODUCTION

The SEMICON/West Equipment and Materials Exposition is held annually in San Mateo, California. This industry trade show is sponsored by the Semiconductor Equipment and Materials Institute (SEMI) and is a yearly milestone for the semiconductor equipment and materials vendors. Each year, Dataquest surveys the wafer fabrication equipment vendors and reports on significant new products and enhancements introduced at the show.

The format of this year's newsletter differs from our previous SEMICON/West newsletters. Part of the reason for this new format is due to the types of questions asked by the staff of the Semiconductor Equipment and Materials Service (SEMS) regarding the current state of the market and technology drivers. The major reason, however, for the new reporting format lies in the unique nature of this year's show compared with previous years. Relatively few new product or technology offerings were introduced at this year's show. Dataquest attributes this relative paucity to the fact that there were many such offerings at the last two SEMICON/West shows, and new products need time to be absorbed and integrated by the industry. Technological change, like other business variables, must be managed properly in order to achieve its maximum potential.

Market Trends

Dataquest's capital spending forecast calls for moderate growth in 1989. This forecast expects spending to fall off at the end of 1989 and the beginning of 1990, coincident with a general downturn in the semiconductor industry. We do, however, expect this slowdown to be less severe in the Asia/Pacific region and Japan. Our survey of equipment vendors at SEMICON/West is consistent with our forecast.

Each of the companies the SEMS staff surveyed was asked, "Do you expect your business to be down, flat, or up in the remainder of 1989?" The results of this survey by equipment category (listed alphabetically) are shown in Table 1.

One market trend that was evident at this show, as it has been for many years running, is the skyrocketing cost of the equipment. Semiconductor manufacturers have responded to these high

TABLE 1
Market Expectations for the Remainder of 1989

Flat Market	Up Market
CVD (U.S. and Europe)	CVD (Japan and Asia/Pacific)
Dry etch (U.S. and Europe)	Dry etch (Japan and Asia/Pacific)
Ion implant	Process control
Steppers	Sputtering
Track	Wet processing

Source: Dataquest
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prices by putting pressure on equipment vendors to increase net throughput (wafers per hour times the percent of time the equipment is available for processing) and/or by increasing yields. In an interesting symbiotic development, some vendors now advertise their equipment as a complement to the more expensive equipment: Use the expensive equipment for critical applications, the less expensive equipment for noncritical applications.

Equipment and Technology Trends

There are two related trends that are driving technology across all equipment categories. One is submicron processing capability. The other is manufacturing productivity.

Submicron processing refers to the ability to do the job at ever-smaller geometries. The job could be imaging or etching small line widths (steppers or etchers), or depositing dielectric or metal on tougher wafer topographies (CVD and sputtering), or perhaps identifying ever-smaller defects and particles (process control). This is a trend that has been with the industry since the invention of the IC. It is continuously challenging, and it is a challenge that is continuously being met: equipment vendors improve their resolution; get better step coverage; and reduce film thickness, particle sizes, and counts.

Manufacturing productivity, on the other hand, is a relatively new challenge facing the equipment industry. It has come into worldwide prominence only in the 1980s. Manufacturing efficiency is now one of the battlegrounds on which semiconductor manufacturers fight their battles for profitability—and for their customers' trust.

As equipment has become more expensive (to be capable of submicron capability), semiconductor manufacturers have demanded that the equipment be more reliable so that net throughput will increase (net throughput is throughput per period, discounted for scheduled and unscheduled downtime). As customers of semiconductor manufacturers have begun to expect zero defect quality control, sole-source suppliers, and just-in-time (JIT) delivery, equipment vendors have had to guarantee repeatability of the process and design their equipment to interface with other processing equipment and production control systems. This demand has led to large increases in automation, process control, and multichamber processing.

As we shall see in the following review, all equipment categories that the SEMS staff reviewed at SEMICON/West were affected by, and responding to, the challenges of submicron processing. Many of the more successful companies also addressed the issues of manufacturing productivity.

LITHOGRAPHY

Market Trends

The worldwide stepper market, which represents approximately 75 percent of the total lithography market, went from 520 steppers in 1987 to 818 in 1988, representing growth of 57 percent. With the additional capacity of the 818 steppers added in 1988, what will be the prospect for 1989? With reference to the U.S. market, some stepper vendors expect their 1989 sales to exceed 1988 sales, while some expect sales to be lower. In general, the consensus indicates that the 1989 U.S. stepper market will be down somewhat from 1988. On the other hand, the consensus expects sales to be up in both Japan and Asia/Pacific. Worldwide, Dataquest anticipates that the increase in business in the Asia/Pacific region and Japan will about balance with the negative growth in the United States and Europe, and that the market for steppers in 1989 will be about equal to the market in 1988.

Equipment and Technology Trends

In general, there were not many new lithography product introductions and product enhancements at this year's SEMICON/West. Perhaps the most significant recent announcement was the Perkin-Elmer Micrascan I, which was introduced prior to SEMICON and described in the SEMS April newsletter, "Step and Scan: Perkin-Elmer's Micrascan I."

Over the last year or so, new advanced submicron systems and lenses have been introduced by the various stepper vendors. It is apparent that the semiconductor industry is now in the digestion phase of these advanced steppers, and this is the reason there was such a low incidence of new products at this year's show.

Interestingly, mix-and-match using projection aligners and 5:1 steppers seems to be making a resurgence, and even mix-and-match using

1:1 steppers with 5:1 steppers is being proposed. With the rising costs of 5:1 steppers, the economic benefits of using mix-and-match for noncritical layers is becoming increasingly attractive. Discussions of the new developments in steppers follow.

Canon introduced a new lens for its FPA-1550 stepper that has a numerical aperture (NA) of 0.55 and a field size of 20mm x 20mm. Deliveries for this lens, which will be installed on a stepper model called the FPA-1550 Mark IVW (wide field), were scheduled to begin in July 1989. Price of the Mark IVW stepper will be about $1.9 million.

Canon also discussed its excimer laser stepper, the FPA-4500. This system uses an all-quartz lens with an NA of 0.37, a resolution of 0.55 micron, and a field size of 15mm x 15mm. The field eventually will be upgraded to 20mm x 20mm. The stepper uses an off-axis alignment system and a laser made by Cymer Laser Technologies (San Diego, California). Price of the FPA-4500 is $2.0 million. Canon said that several of these systems have already been shipped to Japan, the United States, and Europe.

Canon says that it expects 0.5-micron production-worthy excimer laser steppers with 0.45 NA lenses by 1991, and that the industry will push g-line to its limits and then switch to excimer lasers. For 16Mb DRAMs, prototyping and preproduction could be done on g-line steppers with a lens with 0.6 NA, 0.5-micron resolution, and a field size of 17mm x 17mm or 20mm x 20 mm. Production would take place on excimer laser steppers in the 1992 through 1994 time frame.

Ultratech is promoting an intermix philosophy with its 990 series of steppers. In intermix operation, 990 series 1:1 steppers with 1.4-micron resolution are mixed and matched with 5:1 steppers. To more effectively accomplish intermix, Ultratech introduced the Model 990HTI (high throughput and intermix), which is an upgraded version of the Model 990. The 990HTI has a throughput of 95 100.0mm wafers per hour versus 85 for the 990. In addition, the field size can be altered so that multiple 5:1 fields can be accommodated. In one specific case, two 16.5mm x 13.0mm 5:1 fields were accommodated in the 990HTI field that had been changed to 34.0mm x 13.3mm. (The 990 field size is 30.0mm x 15.0mm.) Thus, half the number of steps are required on the 990HTI as are required on a 5:1 stepper, leading to obvious throughput and cost benefits. The 990HTI pre-alignment system also has been adapted for mix-and-match operation.

Ultratech said that intermix is being done at several fabs, and that for one 12-mask-level device, nine levels were done on Ultratech 1:1 steppers, while the remaining three levels were done on 5:1 reduction steppers.

TRACK

Market Trends

Track vendors report that their market has been fairly flat during the last year. They also report that both their bookings and backlogs have been fairly flat, or, at best, only slightly up during the past year. They expect the second half of 1989 to be no better. Business activity in 1990, however, is anticipated with some optimism. While track vendors were unable to identify any particular region as standing head and shoulders above all others in volume of sales, they did agree that Korea was the fastest-growing market in the world. This is consistent with Dataquest's most recent capital spending forecast.

Even though track vendors have seen a flat market this year, customer demands on track vendors have grown. Most of these customer demands fall into the general categories of reliability, process control, contamination control, automation, and flexibility.

Equipment and Technology Trends

Quite a few semiconductor manufacturers are interested in interfacing track systems to lithography tools while maintaining process flexibility. These manufacturers want to develop efficient and flexible track/lithography cells that would be managed by an automated cell controller. In order for an interfaced track/lithography system to be cost efficient, semiconductor manufacturers want track equipment to achieve higher mean time between failure (MTBF) rates of 250 to 500 hours. When track systems can provide a higher MTBF than lithography systems, the linked track/lithography concept will become much more prevalent. Japanese semiconductor manufacturers are said to be achieving close to 1,000 hours MTBF with their track systems. Linked track/lithography systems are more common in Japan due to the reliability of these systems.

Semiconductor manufacturers also are implementing statistical process control into track equipment and want to achieve resist thickness

consistency within 50 angstroms. Temperature control and ambient temperature control is expected to fall within ±0.1°C and humidity control to ±1 percent. Random and flexible (wafer-to-wafer) processing capability as opposed to serial processing also is being requested more frequently.

WET PROCESSING

Wet processing (the stripping, cleaning, and drying of wafers) is made up of several very different equipment segments: manual wet benches, integrated wet stations, acid processors, rinser/dryers, and megasonic units. Each of these segments marches to the drumbeats of different market and technical imperatives.

Manual Wet Benches

Market Trends

Manual wet benches consist of acid baths and rinser/dryers or megasonic units integrated into one unit. The chief feature of a manual wet bench is that cassettes of wafers are moved manually from acid bath to acid bath to a rinser/dryer or a megasonic unit. The market for manual wet benches has declined during the last several years. Most manual wet bench vendors at SEMICON/West were not able to report any news contrary to this trend. However, some vendors did report that their sales were flat, which, in a declining market, is relatively good news.

There was one strong exception to the rule of flat or declining markets for manual wet processing systems: Some vendors reported that, before the recent disturbances, sales of manual wet benches to the People's Republic of China were up strongly.

Integrated Wet Stations

Market Trends

Integrated wet stations are similar to manual wet benches in that they integrate acid bath, rinser/dryers and/or megasonic units. They differ from manual benches in one important way—the movement and transfer of wafers from station to station is automated. Integrated wet stations have grown at a compound annual growth rate (CAGR) of 13 percent since 1984. Many companies, especially those that have established reputations in integrated wet stations, reported that orders and shipments were up strongly in the first half of this year. These same companies are also optimistic about the next six months. Consistent with Dataquest's capital spending forecast, Asia/Pacific was mentioned as a fast-growth area by several vendors.

Equipment and Technology Trends

No new breakthroughs in integrated wet station technology were evident at the show. Many companies, however, featured refinements and improvements that increased safety, reliability, and reduced particulates and breakage of existing systems.

Acid Processors

Acid processor and reprocessor vendors report that orders and shipments for the first half of the year were up substantially over the year-ago period. Some U.S. vendors reported that there was increasing Japanese interest in their products. Acid processors differ from manual or automated wet bench technology in that with acid processors, wafers are placed in a processing chamber, rather than a tub or sink, and acid is sprayed across the wafers in a controlled fashion, instead of being immersed in an acid solution. No major technological innovations in this area were introduced at SEMICON/West.

We also include acid reprocessing in our category of acid processing. Acid reprocessing vendors indicated a growing interest on the part of semiconductor manufacturers in their process. Acid reprocessing removes particulates from the acid and thus sharply cuts chemical consumption while delivering a chemical of a uniform and measurable purity.

Rinser/Dryers

Market Trends

Rinser/dryers typically rinse cleaning chemicals from the wafers and then dry the wafers. Traditional methods have relied on mechanical movement of the wafer for the drying action. For smaller geometries, this has led to particulate generation. Several wet processing companies have responded to this need by moving to isopropyl

alcohol (IPA) vapor drying techniques. IPA vapor drying has shown solid growth in recent years. Vendors of IPA vapor dryers reported that bookings and shipments were strong for the first part of 1989 and that they are confident business will increase in the second half of this year.

Equipment and Technology Trends

Trebor, Inc., demonstrated the Hydro-Dry 5000 System, which had an interesting technique for rinsing and drying wafers. The system combines a hot deionized (DI) water rinse and a slow water lift into a clean laminar flow air atmosphere. By slowly removing the wafer and cassette with a patented dual-lift mechanism, the capillary action of the water tension draws off the water from the wet surfaces. To ensure that the drying process is complete, the hot wafer and laminar air drive off any residual moisture, leaving a completely dry wafer. Several major semiconductor manufacturers are reported to be studying this system.

Megasonic

Market Trends

Megasonic equipment is a category of cleaning equipment that uses sonic pressure waves to clean the wafer. Megasonic equipment is growing faster than any other equipment segment, although it represents only 3 percent of the total wet processing market. Megasonic vendors reported strong bookings and billings in the first half of 1989, and they are confident that growth will continue in the second half of 1989.

DRY ETCH

Market Trends

The mood at SEMICON/West 1989 was cautiously optimistic with regard to market trends. Bookings and shipments had been very strong for the first half of 1989. Most equipment vendors indicated that they expected the second half of 1989 to be somewhat weak in bookings compared with the first half. In general, vendors reported that business continued to be strong in the Pacific Rim markets, especially Japan, Korea, and Taiwan. In comparison, the U.S. and European markets are expected to be flat or "somewhat down" with regard to bookings for the rest of the year. Dataquest expects the backlog of orders for dry etch equipment to decline for the rest of the year. In 1990, Dataquest expects relatively flat growth for the dry-etch business segments, with most of the activity occurring in the Pacific Rim region.

Dry Strip

Equipment and Technology Trends

Dry-strip technology continues its trend toward downstream, single-wafer strippers. Concerns regarding defects, plasma radiation damage, uniformity, repeatability, and efficient resist removal are best addressed by single-wafer, downstream strippers. Microwave sources are gaining popularity for efficient creation of reactive oxygen species.

Gasonics introduced its AURA microwave downstream stripper. The system offers a modular, automated approach to resist stripping with capability extending to 150mm wafers without any system modification.

Branson/IPC expanded on products based on its L3200 dual-chamber, single-wafer, downstream resist stripper. These products use an external rf source in order to shield the wafer from plasma radiation damage. The L2200 system (based on the L3200) is a single-wafer isotropic, downstream etcher for noncritical etch applications.

Dry Etch

Equipment and Technology Trends

From $307 million in 1987, the dry-etch market grew explosively to $547 million in 1988. The growth was fueled by capacity expansion for the burgeoning 1Mb DRAM and ASIC markets. Also, the trend toward submicron design rules and multilevel interconnect created an enormous need for technologically advanced dry-etch equipment.

Single-wafer processing is gaining momentum for applications in the submicron regime. The advantages of uniformity, low defects, repeatability and multistep processing for single-wafer systems will become even more evident as manufacturers move from 150mm to 200mm wafers.

A variety of solutions are being offered to solve the problem of ion-bombardment damage to thin oxides during reactive ion etch (RIE) processing. In the United States, several equipment

vendors are using magnetically enhanced reactive-ion etching (MERIE) to achieve high ionization efficiencies and anisotropy without excessive ion-energies.

Applied Materials introduced a submicron oxide etch process using the PE5000 MERIE etch system. For submicron applications, it appears that Applied will migrate its customers from the 8000 series batch etchers toward the modular PE5000 single-wafer, multichamber architecture.

Tegal introduced the 2000 series of etchers, which combines magnetic confinement with RIE for low-damage applications. The system uses a dual-frequency, tri-electrode configuration to enable maximum flexibility in the processing.

Lam Research announced a new submicron oxide etch process for its successful Rainbow 4000 series etchers. The process used a 400-kHz low-frequency rf discharge for creating etching species with high selectivity and split-phase rf power for enhanced plasma confinement.

The Varian/TEL relationship continued to expand with Varian's introduction of the TEL K-series etchers in the United States and Europe. The systems are anisotropic etchers with 200mm capability targeted toward 1Mb and 4Mb DRAM applications. The VE 4000, 5000, and 6000 models in the K-series are targeted at the polysilicon and silicon trench, oxide, and metal etch markets, respectively.

Materials Research Corporation has been selected by Texas Instruments to market its 150 series plasma-etching systems for nitride, oxide, and polysilicon applications.

Electron cyclotron resonance (ECR) systems are being developed in Japan and Europe for low-damage etching. In Europe, Alcatel and Electrotech have developed distributed multipolar ECR systems for submicron etch applications. In contrast, Sumitomo Metals has developed a single-pole ECR etch and CVD system in Japan. This system will be marketed by its partner Lam Research in the United States.

ECR schemes offer the advantages of very low ion energies, high selectivity, and anisotropic profiles. High-density ECR plasmas are created by achieving resonance between a 2.45 GHz microwave source and an 875-gauss magnetic field. The electrons created in this environment undergo accelerated circular motion, which leads to high ionization efficiencies. Using a divergent magnetic field, these ions can be extracted from the plasma chamber for etching and deposition. The wafer is located downstream from the plasma and hence is not exposed to radiation damage. By independently biasing the wafer stage with a 13.56-MHz rf source, varying degrees of anisotropy can be achieved.

CHEMICAL VAPOR DEPOSITION (CVD)

Market Trends

Market expectations for the CVD market mirrored the comments of the dry-etch equipment manufacturers. This was not surprising, as the move to submicron processes and multilevel interconnect technology affects the associated deposition and etch markets in identical ways. (Please refer to the "Dry Etch" section of this newsletter for a summary of vendor comments regarding market expectations in CVD.)

Equipment and Technology Trends

CVD had a banner year in 1988. The CVD market grew an astounding 79 percent from $254 million in 1987 to $455 million in 1988. The trend toward dedicated nontube reactors for high-quality CVD films was very evident at SEMICON/West. Dedicated reactors offer the benefits of low defects, low-temperature processing, high uniformity, and integrated processing for submicron devices.

CVD films are becoming the technology drivers for the development of clustered process equipment for integrated processing. All the major CVD equipment vendors are now offering their versions of multichamber systems.

CVD Dielectrics

ASM introduced a significant new CVD product: the Advance 600 multichamber, integrated processing system. ASM has positioned the 600 series as its platform for future integrated system offerings. Initially, its system is targeted toward the demanding market for interlayer dielectrics. The system integrates two eight-position batch PECVD chambers with two single-wafer etch chambers. These four process chambers are configured around a central loadlock system (CLS) architecture. The Advance 600 is capable of 150mm wafer processing (upgradable to 200mm in the future). ASM currently offers silane- and TEOS-based PECVD oxide and nitride films on

this system. Throughputs of 100 wafers per hour (without planarization) or 25 wafers per hour (with planarization) are being claimed.

Electrotech introduced the single-chamber 201 version of its Delta 200 series multichamber PECVD oxide system. The Delta PECVD series, together with the Omega etch series and the Sigma sputter system, enables Electrotech to offer one-stop shopping capability for integrating etch, sputter, and CVD into a multichamber platform.

Applied Materials continued to offer more applications for its PE5000 CVD multichamber, integrated process system. In addition to silane- and TEOS-based oxide and nitride films, Applied announced preliminary results from a process for in-situ planarization using boron oxide as a sacrificial oxide. Even though boron oxide is hygroscopic and flows as deposited, Applied uses it as an etchback coating analogous to the spin-on-glass process.

Watkins Johnson continues as the successful "lone ranger" that offers atmospheric oxide, PSG, and BPSG films for production applications. Its system is widely used for BPSG smoothing before first-level metal in 1Mb DRAM applications.

CVD Metals and Silicides

Genus prevails as the market leader for production tungsten silicide films. It continued to highlight the Genus 8720 system for blanket and selective tungsten films using hydrogen or silane chemistry. Genus claims that its system overcomes the problem of tungsten deposition on the edges and backside of the wafer during processing.

BTU International has formed a joint venture with Ulvac in the United States, which is known as BTU-Ulvac. This joint venture will manufacture and market the ERA 1000 coldwall, single-wafer system for selective tungsten in the United States and Europe. The system is a flexible dual-chamber reactor with 200mm capability.

Although selective tungsten is not yet in widespread production, blanket tungsten is gaining popularity for contact/via plugs and first-level interconnect. Equipment companies and semiconductor manufacturers are still struggling with the problems of selectivity, adhesion, uniformity, and reliability of the selective tungsten process. Silane-based processes are beginning to overcome some of the problems such as wormholes, tunnels, adhesion, and uniformity that plagued the earlier hydrogen-reduction selective tungsten processes.

SPUTTERING

Market Trends

Sputtering equipment vendors were optimistic about the second half of this year. Only 1 of the 10 sputtering companies that Dataquest spoke with reported a downward trend for bookings and backlog during the past year. Another reported bookings and backlog as being flat, albeit at very high levels. The rest of the companies, however, reported bookings and backlog as up significantly during the last year. Expectations by the majority of the vendors call for business to remain flat or improve during the second half of 1989 and into 1990. Nearly all sputtering vendors identified Korea and Taiwan as their hottest growth areas.

Equipment and Technology Trends

Step coverage, uniformity, reliability, and throughput continue to be cited by sputtering manufacturers as the major technology drivers for the sputtering market. New film applications are emerging in response to new customer demands. Some of the new film applications that were mentioned include the following:

- Layered films involving metal CVD and sputtered aluminum
- Reactively sputtered TiN and sputtered aluminum
- Excimer laser reflow techniques for planarization
- Barrier structures
- Other TiN applications

Cluster tool (multichamber processing) activity is another major technology driver for sputtering equipment. Electrotech introduced a new cluster tool, marking the sixth cluster tool introduction for sputtering applications along with Anelva, Balzers, Eaton, Leybold-Heraeus, and Varian.

Complete chamber isolation, contamination control, process flexibility, and off-line module maintenance were mentioned as the main drivers for the cluster concept. Along with this concept has come the desire to set up a cluster system with process chambers or modules from different vendors.

Eight-inch wafer capability and low damage processing were also mentioned as technology

drivers for sputtering equipment. Low damage processes generally involve lower power requirements, less energy, low temperature processing, or the use of ECR technology for low-power etch cleaning.

DIFFUSION FURNACES

Market Trends

The vendors of both horizontal and vertical tube systems were an upbeat group who look forward confidently toward the second half of this year. Horizontal tube vendors are seeing healthy activity that is being driven by capacity expansion in the mainstream technologies.

Vendors also are seeing more acceptance of vertical tube reactors (VTR) for advanced processes that require lower levels of contamination, better uniformity, and 200mm wafer capability. The established vendors of VTRs have seen their orders move from one or two systems at a given semiconductor company to multiple systems in an integrated environment.

Bookings have been up for the horizontal tube vendors. Backlogs were reported as either flat and solid, or up during the last year, with more of the same expected during the remainder of 1989 and into 1990.

VTR vendors reported that they expect their bookings and backlogs to continue to be very strong, not only for the remainder of this year, but also for 1990. Japan has the largest installed base of VTRs and is the region that is experiencing the strongest growth. Most of the demand for VTRs is coming from advanced DRAM fabs, 200mm fabs, and fabs that intend to run 200mm wafers in the future.

Equipment and Technology Trends

The demand driver for VTRs was succinctly stated by one company as "DRAMs by default," indicating that DRAM factories are ordering VTRs to ease robotic and 200mm wafer-handling issues. Manufacturers are finding that VTRs are better suited for the task of handling heavy quartz boats full of 200mm wafers.

Reportedly, VTR vendors and their customers have had a lot of discussion about how to link several of the VTRs as an integrated (cluster) system. Two of the world's largest semiconductor manufacturers reportedly are interested in developing a loadlocked cluster system that, while under a loadlocked vacuum, is capable of taking the wafer from the cleaning step to the diffusion step and on to the deposition step. This loadlocked cluster VTR system is being sought for improvements in contamination control, better chamber characteristics, and uniformity.

Other VTR techniques for improved contamination control that are reportedly under consideration are nitrogen-purged loadlocks and an oxygen exclusion system. This last technique is being jointly developed by a large equipment vendor and a large semiconductor manufacturer.

SILICON EPITAXY

Market Trends

In 1987, the epi equipment market totaled $36 million and it grew to $85 million in 1988, representing boisterous growth of 138 percent. Thus, a significant amount of capacity was added in 1988. The consensus at the show was that the growth in 1988 was perhaps too boisterous and now the industry may have to pay for its 1988 excesses in the form of dampened sales in 1989. On the positive side, the advent of single-wafer systems is something that epi vendors think will put a little perk into their 1989 sales.

Overall, the consensus of epi vendors was that the perk from technology buys for single-wafer epi systems will not quite match the hangover from excess capacity: The epi market will be down, or at the very best, flat, in 1989.

Regionally, the United States is the largest market for epi equipment, as it accounted for 50 percent of 1988 sales.

Equipment and Technology Trends

In equipment technology, the competition between the traditional batch reactors and the new single-wafer reactors is becoming more interesting. Applied Materials continued its traditional batch approach by introducing a new model; Lam Research showed the previously introduced Tetron I, also a batch system; and ASM Epitaxy upgraded its new single-wafer Epsilon One to 200mm capability. Although the Epsilon One was the only single-wafer system at the show, another single-wafer system is being developed by Rapro, in Fremont, California. The need for higher-quality epi films will drive the single-wafer epi market.

In process technology, there was emphasis on selective silicon epitaxy. Although selective epi has been around for a while, it has not found its way into production. However, with the push to submicron geometries, selective epi may find its initial production applications in contact buffers, particularly as the selective epi process temperature decreases. Other potential applications include trench refill and device isolation.

Applied Materials introduced the Precision Epi 7700, a batch epi reactor. Applied's previous model, the Precision Epi 7010, which was a disappointment, was a combination induction and passive radiant machine. With the new 7700 system, Applied has reverted to its traditional quartz-lamp radiant approach. The 7700 can process 15 150mm and 8 200mm wafers per batch for gross throughputs of 20 and 10 wafers per hour, respectively. Net throughput, which takes into account the downtime associated with periodic system clean, however, would be less. Thickness and resistivity uniformities are ±5 percent for the 7700.

The 7700 is also fully automated, as is the 7010, except that the 7700 uses only one susceptor instead of the two used on the 7010. The system can do atmospheric or reduced-pressure processing and can deposit silicon epi or selective poly or single-crystal films.

A beta system was installed at AT&T in February, and first shipments of the 7700 are expected to occur in the third quarter of 1989. Price is $1.1 million.

ASM Epitaxy announced the availability of 200mm wafer processing on the Epsilon One single-wafer epitaxial reactor. This system was originally introduced (but not exhibited) at last year's SEMICON/West with 100mm and 125mm capability, and is described more fully in last year's newsletter.

The Epsilon One is the first commercially available, single-wafer epi production system. It features fully automatic, dual load-locked, rapid thermal atmospheric processing with growth rates of 5 microns per minute. Typical run-to-run performance is ±1 percent thickness and ±3 percent resistivity uniformity. Wafer rotation occurs during processing, and chamber etch occurs after every wafer. Net throughput is 7 to 8 200mm wafers per hour. The system also will deposit selective epi. Other features of the Epsilon One include particulate control, low power consumption, and a small footprint. Price is $750,000 to $850,000, depending on options.

RAPID THERMAL PROCESSING (RTP)

Market Trends

The RTP market grew from $18.5 million in 1987 to $22.0 million in 1988. Dataquest believes that 1989 will be a year of healthy growth as several RTP processes move into production for submicron devices.

Equipment and Technology Trends

Titanium silicide and reactive titanium nitride processes are the leading production applications for RTP technology. Dataquest believes that RTP will continue to make inroads into tube processing for demanding submicron applications such as thin oxide/nitride dielectrics, shallow junction implant annealing, and BPSG reflow. AG Associates and Peak Systems continue to dominate the production RTP market both companies introduced products offering 200mm process capability.

ION IMPLANTATION

Market Trends

Dataquest discussed the general business outlook for ion implantation equipment with several vendors at SEMICON/West. In general, both bookings and backlog were basically flat.

Equipment and Technology Trends

No new ion implantation systems were introduced at the show, although one system, because of a recent acquisition, was in a new booth location. Varian exhibited the EXTRION 220, the advanced medium current ion implanter it acquired from ASM International last year. As reported in our previous SEMICON/West newsletters, the 220 uses a unique parallel-beam scanning technique that, combined with the capability of 0 to 89 degrees programmable tilt angles, provides excellent flexibility in controlling channeling and shadowing effects. The parallel-beam design of the system is particularly important when processing large wafers or device structures with large aspect ratios because it can provide excellent dose uniformity across the entire wafer surface.

Although no new implantation systems were introduced at the show, two companies—Applied

Materials and Eaton—introduced system options for modifying the tilt angle of their implanters. Typically, the implant angle of a system is set at 0 degrees or tilted to 7 degrees. At 0 degrees, the ions bombard the wafer perpendicular to the wafer surface. However, this can cause the problem known as channeling, in which the implanted atoms travel along specific directions (open channels) in the single-crystal silicon where the ions do not encounter any target nuclei. Because channeling is difficult to control precisely, it can lead to an inconsistency in implant depth, which results in nonuniformity. One widely accepted technique used to minimize channeling is to tilt the wafer surface relative to the incident beam direction (typically by 7 degrees) so that the silicon lattice presents a dense orientation to the incident beam. This technique, however, may create a new problem known as shadowing, which causes asymmetry of the implant around the device features. In particular, shadowing is unacceptable for many advanced devices such as 4Mb and 16Mb DRAMs. A programmable tilt angle on an implanter provides flexibility in dealing with both channeling and shadowing effects.

Applied Materials introduced its new "Automatic Implant Angle Selection" option for its high-current implanter, the Precision Implant 9200. This option provides flexibility during operation by allowing the implant angle to be changed between 0 degrees and 7 degrees, in 0.5 degree increments. This step can be performed in less than 10 seconds using system process recipes. No mechanical change is required to change the angle of implant.

Eaton introduced a new end station for use on its NV-6200A medium current implanter. The end station can be programmed for wafer tilt angles between 0 and 60 degrees. In addition, the end station can provide rotation of the wafers during processing in a continuous mode or in discrete intervals. The new end station can be retrofitted to existing 6200A implanters and is a no-cost option on new systems.

PROCESS CONTROL

Market Trends

In this year's review of SEMICON/West, Dataquest discusses the general business mood of a diverse group of process control equipment vendors, including perspectives from manufacturers of critical dimension (CD) measurement equipment, wafer inspection systems, film thickness measurement systems, and surface particle detectors.

The majority of process control equipment vendors surveyed at SEMICON/West commented that their bookings activity was relatively healthy and on the rise. Backlog was relatively flat for most vendors but was expected to increase slightly because of an increase in bookings activity. Several vendors remarked that a large backlog from 1988 had been worked off by increasing their production levels and that, as a result, their current backlog was relatively flat. While most companies reported that the first half of 1989 had been good, a number of vendors expressed concern regarding the health of the equipment industry for the latter part of this year and into 1990.

Critical Dimension Measurement

Equipment and Technology Trends

At this year's show, much of the activity in CD measurement systems was focused on system and software enhancements, pick-and-place robotics, and 200mm wafer capability. Two companies introduced new optical CD systems. Micro-Controle of France, a newcomer to the market, exhibited its ALARM optical CD metrology system. This tool was introduced at SEMICON/Europa earlier this year. (In addition to optical CD, Micro-Controle also offers an automatic wafer inspection system.) Optical Specialties, Inc., of Fremont, California, exhibited the alpha unit of its new OSI-2000 fully automatic CD measurement system. One of the important new system features is pattern recognition capability. Like its predecessor, the MV-500, the OSI-2000 utilizes the Laser-Line autofocusing technology developed by OSI.

Wafer Inspection

Equipment and Technology Trends

In the area of wafer inspection, three companies introduced new models of equipment that represent an extension of the current product line for each vendor. Nikon introduced the Optistation 3, which emphasizes improved contamination control, while the Wild Leitz MIS is that company's first system for 200mm wafer inspection. KLA Instruments introduced its new 2029 system, an automatic defect detection tool that has improved

defect-detection sensitivity. The KLA-2029 is capable of detecting 0.35-micron defects on the 0.7-micron design rules used by producers of 4Mb DRAMs.

Insystems introduced a defect review station for its automatic defect detection system. This station allows an operator to perform wafer defect classification as a function separate from the operation of the Model 8600. This translates to enhanced throughput because the time-consuming task of operator defect classification now can be performed essentially off-line. KLA introduced a defect review station for its family of 20xx products at last year's show.

Currently, KLA and Insystems are the major suppliers of automated defect detection equipment; these systems automatically inspect the wafer surface for process-induced defects. At this year's show, two newcomers to this market segment exhibited equipment that they claim can also perform automated defect detection without the need for operator visual inspection. Olympus exhibited its Cue 2000 system, first shown at last year's SEMICON/West. In addition, Micro-Controle exhibited its new Image Defect Inspection System (IDIS). Similar to KLA's approach, both companies are pursuing advanced software and signal processing capability to automatically detect process defects. Insystems relies on a distinctly different technology known as spatial frequency filtering holography to automatically detect defects on a wafer.

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SEMICON/JAPAN 1988: A JUGGERNAUT STRUTS ITS STUFF

INTRODUCTION

The Semiconductor Equipment and Materials International (SEMI) trade organization sponsored its annual SEMICON/Japan exhibition at the Tokyo International Trade Fairgrounds (Harumi) in Tokyo on November 24 through 26, 1988. It should come as no surprise that this show was a blow-out. Attendance was nearly 58,000, showing the tremendous strength of the Japanese semiconductor industry's business environment. Even as the final bell rang at 5:00 on the last day, the booths were still vibrant with activity.

In this newsletter, we will report on some of the interesting new products and process developments that were introduced at the show. We will also examine some of the pertinent issues affecting the industry.

LITHOGRAPHY

Japan is the world leader in DRAM manufacturing; therefore, it is vital to understand the strategies being adopted in Japan for advanced lithography tools for this device category. At SEMICON/Japan this year, Dataquest surveyed a number of lithography experts regarding the progression of g-line, i-line, and excimer laser steppers for high-density DRAM fabrication in Japan. While opinions vary from manufacturer to manufacturer, there was a strong consensus that high numerical aperture (NA) g-line lenses will be used in 4Mb DRAM production and for first-generation 16Mb DRAMs. Final shrink of the 16Mb DRAM is expected to be accomplished with i-line steppers, while significant use of i-line lithography is anticipated for 64Mb DRAM production. (Mix-and-match lithography of e-beam and optical steppers is also being considered for the 0.5-micron processing regime.) Although some experts surveyed felt that excimer laser steppers might be used in production as early as the final shrink of the 16Mb DRAM, most believed that it will be the 64Mb DRAM manufacturing processes that will utilize excimer stepper lithography.

At this year's SEMICON show, Japanese stepper manufacturers announced new g-line and i-line lenses, primarily for 1Mb and 4Mb DRAM manufacturing. In this part of the newsletter, we will report on these new announcements; present a status update of the Aurora X-ray lithography project; and conclude with a brief look at several manufacturers of excimer laser sources, an essential component in the development of next-generation optical lithography.

Canon

Canon exhibited its new FPA-1550 Mark III stepper. This g-line stepper, introduced at SEMICON/West in May 1988, incorporates a new high-speed reticle changer and a new pick-and-place wafer-handling system (also available as options on the 1550 Mark II system). The lens of the 1550 Mark III is designated as UL-11; it is a 5X, g-line lens with a 21.2mm-diameter field. In addition, the lens has switch-selectable numerical apertures of 0.48 and 0.43. At the 0.48 NA setting, it has a production resolution of 0.7 micron, with a 1.5-micron depth of focus at 0.7-micron lines and spaces.

At SEMICON/Japan this year, Canon introduced a wide-angle lens version of the Mark III, known as the Mark IIIW. The Mark IIIW utilizes a 0.45 NA lens with 0.75-micron resolution and provides a 28.3mm-diameter field (20mm by 20mm). This corresponds to an increase in area of 78 percent over the standard field size of 21.2mm diameter, translating to a significant increase in throughput. For example, in 4Mb DRAM production, four to five chips can be imaged in a single field with the wide-angle lens option as compared with two to three chips in the standard lens configuration. The list price of the 1550 Mark III is ¥215 million, and the 1550 Mark IIIW is ¥230 million. Shipments to customers in Japan began in the autumn of 1988.

Hitachi

Hitachi displayed its LD-5010 i-line stepper; this system was first introduced at SEMICON/Japan in December 1987. The LD-5010i utilizes a 5X, i-line lens with an NA of 0.40; a field size of 21.2mm in diameter; and a resolution of 0.6 micron. In last year's SEMICON/Japan newsletter, Dataquest reported that Hitachi was making its own lens for this system. This year, however, an i-line lens manufactured by Minolta for the LD-5010i was on exhibit in the Hitachi booth. Hitachi expects this i-line stepper to be used in 4Mb DRAM pilot lines as well as for final shrink on 1Mb DRAM production lines. The price of the LD-1510i stepper is ¥200 million. Dataquest believes that approximately 15 systems have been installed through the end of 1988.

Nikon

At this year's show, Nikon introduced a new member in its family of NSR 1505 steppers. The new 5X stepper has three lens options: two new g-line lenses (the 1505G6E and the 1505G6D) and a new i-line lens (the 1505i6A). The new stepper has been designed with a larger system chassis in order to accommodate larger lenses with higher numerical apertures, including Nikon's excimer stepper lens. For the two new g-line lenses, the 1505G6E has 0.54 NA and 0.65-micron resolution, and the 1505G6D lens has 0.45 NA and 0.75-micron resolution. The i-line lens, the 1505i6A, also has 0.45 NA but with a finer resolution at 0.65 micron. Field size for all three lenses

is 21.2mm in diameter. Nikon quotes a specification of 0.13 micron (3 sigma) in global alignment and site-by-site alignment modes for all three lens options. This alignment accuracy specification is achieved through the implementation of a new alignment system design.

Other new system enhancements include an individual field-leveling option (for improving process latitude when working with high NA lenses with small depths of focus), an extended reticle library, 200mm wafer capability, on-line host computer control, and improved SECS II implementation. The new stepper system with g-line lens options was available for sale in December 1988 with a delivery schedule of six months; the new i-line lens option will be available for sale after June 1, 1989.

Sumitomo Heavy Industries

A year ago at SEMICON/Japan, Sumitomo Heavy Industries announced its Aurora compact synchrotron orbital radiation (SOR) ring for use in X-ray lithography. Since then, construction has been completed on the injector system; the storage ring itself is expected to be completed during first quarter 1989. At that time, preliminary operation of the Aurora will commence with the injection of electrons into the storage ring. Sumitomo Heavy Industries expects to begin full characterization and operation of the system by summer 1989. The system initially will have three beam lines, but eventually the system will be expandable to 16 ports. The price of the Aurora will be approximately $15 million.

Excimer Laser Sources

In last year's SEMICON/Japan newsletter, we reported that three companies—Canon, GCA, and Nikon—were developing excimer laser steppers for advanced optical lithography. A number of factors still need to be addressed in the development of this technology. These include laser source stability, the extension of laser operation cycle time, the availability of appropriate photoresist with reliable batch-to-batch consistency, and the process engineering know-how within the semiconductor companies themselves to work at line geometries produced by excimer laser steppers. This part of our newsletter highlights two manufacturers of excimer laser sources exhibiting at SEMICON/Japan this year: Admon Science and Lumonics.

Admon Science

Admon Science exhibited its MBK-400TL krypton fluoride excimer laser in the Mitsui booth at SEMICON/Japan. Admon Science, 40 percent owned by Mitsui, has been involved in research on excimer lasers for six to seven years. The MBK-400TL laser has specifically been designed for stepper lithography. It relies on a combination of etalons and other proprietary technology to maintain a line-narrowed output. The company also has designed an automatic partial gas replacement system in order to extend tube lifetime such that the time-limiting factor for extended operation of the laser is cleaning the windows of the discharge unit rather than refilling the gas tube. With the MBK-400TL, the window-cleaning procedure is necessary after approximately 7×10^8 shots. Admon Science already has delivered several lasers with reduction optics to semiconductor manufacturers, including Matsushita Electric. The price of the MBK-400TL laser with reduction optics is ¥44 million. The company has shipped several experimental laser systems to stepper manufacturers as well.

Lumonics

At the show this year, Lumonics exhibited its Index 300 excimer laser, a line-narrowed krypton fluoride excimer laser designed specifically for applications in stepper lithography. The Index 300 utilizes a line-locked resonant absorption cell rather than the traditional etalons in order to keep the laser wavelength locked on a specific absorption line. Lumonics has received a U.S. patent for this design feature and has recently applied for a patent in Japan. The Index 300 has a fully automatic, cryogenically controlled gas handling system. Lumonics has a specification of eight hours of continuous operation per single gas filling, though in-house tests have shown the system to operate well in excess of this limit. Lumonics is a Canadian corporation with manufacturing facilities in Canada, the United States, and England.

PHYSICAL VAPOR DEPOSITION (PVD)

At this year's SEMICON/Japan show, three companies—Anelva, Ulvac, and Varian—exhibited equipment or displayed information on their new multichamber vacuum processing systems. The Anelva and Varian systems have been discussed or exhibited at previous SEMICON shows, but the introduction of a new system from Ulvac illustrates the growing trend in the development of integrated vacuum processing equipment. The strategy being pursued by a number of companies is to provide a variety of vacuum process capabilities on a single system, such as sputter, CVD, etch, and RTP.

Anelva

Anelva exhibited the ILC-1051 and ILC-1551 single-wafer, in-line multichamber systems at SEMICON/Japan this year. These systems were first introduced at SEMICON/Japan one year ago; however, at that show and at SEMICON/West in May, only poster descriptions of the equipment were presented. The ILC-1551 has three processing chambers arranged horizontally around a central wafer-handling chamber. Process chambers that can be used include aluminum sputtering, metal CVD, and ECR deposition of a silicon dioxide interlayer dielectric. Deliveries of the ILC-1551 to Japanese customers began in March 1988; Dataquest believes, however, that shipments to date have been only single-chamber sputter systems (typically with rf bias) rather than the full three-chamber system. The price of the ILC-1551 with a single processing chamber can vary from ¥90 million for a sputter chamber, to ¥100 million for selective tungsten deposition, to ¥140 million for ECR processing capability. The price of the ILC-1551 with all three chambers is ¥150 million. The ILC-1551 is intended for R&D and small-volume production.

The ILC-1051 is a four-chamber system that can be used either in series for multistep processing or in parallel for higher throughput. The ILC-1051 and ILC-1551 have both been designed with the same concept so that new processes developed on the ILC-1551 can be used in volume production on the four-chamber ILC-1051. The ILC-1051 is priced at approximately ¥200 million.

Ulvac

Ulvac threw its hat into the multichamber processing arena at SEMICON/Japan this year with the introduction of its new C-2111 Stellar Multi-Process System. The C-2111 can accommodate from four to eight individually pumped, vacuum-isolated processing chambers. Four chambers are oriented as satellites around each of two central wafer-handling chambers equipped with its own loadlock. In addition, the two central wafer-handling chambers are connected via a wafer transport system. The strategy in this product design is to provide complete metallization processes on one machine. The four chambers include sputter etch for cleaning the wafer, selective tungsten CVD, sputter (including optional rf bias and heating for planarization), and infrared lamp anneal. The price of a four-chamber version of the C-2111 is approximately ¥300 million. The C-2111 system will be available in autumn 1989.

Ulvac also introduced the MCH 4500, a two-chamber sputter system similar in design to its MCH 9000 four-chamber system. The MCH 4500 was developed in response to customer feedback for a smaller version of the MCH 9000 for dedicated processing. Each of the two chambers of the MCH 4500 is individually loadlocked so the system can be run in series or parallel mode. Price of the MCH 4500 is ¥140 million. Several systems have been shipped to Japanese semiconductor manufacturers.

Varian

At this year's show, Varian presented a videotape describing its M2000 single-wafer sputtering system. The system was introduced at last year's show and introduced to the U.S. market at SEMICON/West in May 1988. One system already has been shipped to the demonstration lab of TEL/Varian. Dataquest believes that a second system was shipped to a customer in Japan in December 1988. The price of the M2000 in Japan is between ¥250 million and ¥350 million, depending on options that include number of chambers and rf bias. The M2000 is currently targeted at multistep metal processes, but it is also Varian's entry into the multiprocessing vacuum systems that are just beginning to emerge in the marketplace. When configured for multiprocessing, one or more of the sputter modules can be replaced with rapid thermal processing or CVD modules.

DRY ETCH

Dataquest saw a number of new product introductions this year. Most of the new activity is for the development of integrated vacuum processing. The hex-etcher was the last, and most productive, of the batch. Dataquest believes that the industry is moving inexorably to a single-wafer etching environment, particularly in Japan.

Alcan Tech

This joint venture between CIT/Alcatel and Canon featured its GIR 260, which has three single-wafer chambers. Alcan Tech has targeted aluminum etching and has installed 60 systems in Japan. The system sells for ¥70 million.

The company also featured its microwave stripper, which sells for ¥25 million. Dataquest estimates an installed base of 130 of these systems in Japan.

Anelva

Anelva introduced its Model 4051, a single wafer, multichamber etcher. This etcher uses three chambers—two with magnetic coils and one for downstream stripping. The magnetic coils employ a rotating magnetic field to create a very high ionization ratio in the plasma, thus enabling single-crystal silicon etching to proceed at high etch rates and very low pressures. This system is targeted at the aluminum etching market. It is priced at ¥180 million.

The Model 4051 comes on the heels of last year's MERIE (magnetically enhanced RIE) system. This single wafer system was investigated for use in trench, aluminum, and GaAs etching; about 10 MERIE systems have been sold. The advantage of increasing the magnetic field strength for aluminum etching is that the selectivity over photoresist increases by a factor of 4. The rate at which Japanese semiconductor manufacturers will move into single-crystal, trench processes for DRAMs is still uncertain; therefore, Anelva will use the MERIE technology to penetrate the aluminum market and try to make a dent in Applied Materials' dominant position.

Anelva is still developing and selling batch RIE systems such as its new Model 4015. Anelva introduced and shipped 20 systems in 1988. The 4015 sells for ¥130 million.

Applied Materials Japan (AMJ)

Applied Materials introduced the Precision Etch 5000 in 1988. AMJ reported that eight of these systems were sold in Japan in 1988 for single-crystal applications. The price of the system ranges from ¥150 million for a two-chamber system to ¥200 million for a four-chamber system. This multichamber system uses a rotating magnetic field to create a very high ionization ratio in the plasma. In this way, the etching of single-crystal silicon can proceed at high etch rates and at very low pressures. The same technology had been introduced at Anelva previously.

General Signal/Drytek

Drytek introduced the Model 380 single-wafer etcher for poly and oxide, a single-chamber version of the Quad system previously introduced by Drytek. It sells for ¥60 million. Dataquest believes that no systems have been sold in Japan.

Since the acquisition of GCA by General Signal and the incorporation of the triode etcher into the Drytek division, Drytek now has an installed base in Japan. However, there are less than 10 triode etchers in Japan. It is still unclear as to whether or not Sumisho, a subsidiary of Sumitomo Electric (which has been GCA's representative in Japan), would represent Drytek. Sumisho continues to handle the triode.

Hitachi

Hitachi showed a new product, Model M-308AT, targeted primarily for etching Al-Cu. The system employs the same microwave antenna, magnetic coils, and quartz bell jar as introduced previously in its microwave etcher. The system is priced at ¥180 million. The company shipped approximately 30 systems in 1988, all in Japan. Approximately 50 percent of shipments are outside of Hitachi.

The company also featured its UA-3150 Ozone Stripper. The system is priced at ¥25 million. It employs lamps and ozone to eliminate the drive-in associated with plasma-related stripping processes.

Sumitomo Metals, Inc. (SMI)

Much interest has been generated by the NTT-developed electron-cyclotron-resonance (ECR) process for deposition and etching. Sumitomo licensed the technology and introduced a system three years ago. It has since formed a partnership with Lam Research to market the system in the United States and Europe. The system sells for ¥125 million.

Dataquest believes that Sumitomo has built 60 of these systems and sold approximately 45. (Fifteen systems are being used internally by SMI.) The majority of these 45 systems have been sold to semiconductor manufacturers; however, approximately 5 systems have been purchased for broader industrial applications. In 1988, 16 systems were sold in Japan—10 for etching and 6 for deposition. Before 1988, most of the interest was for deposition. The current interest in ECR is for development of polycide and single-crystal silicon processes.

Tokuda

Tokuda announced its HIR-200 single-wafer etcher. This is a refinement of Tokuda's HIR-100 etchers and employs a permanent magnet below the wafer in order to increase the ionization ratio in the plasma. The system sells for ¥72 million. Shipments of the system will begin in mid-1989. In 1988, 7 units of the older model, the HIR-100, were shipped. The HIR-100 sells for ¥60 million.

The company also featured its CDE (chemical dry etch) system. Dataquest estimates that Tokuda has shipped nearly 400 of these systems since introduction in the early 1980s. They are used primarily for finish etch after RIE, for polysilicon etching of static RAMs, for nitride etching, and for cleaning contact holes in BPSG applications. About 13 of these systems were sold in 1988. The average selling price of the system is ¥41 million.

Tokyo Electron Laboratories (TEL)

TEL/Lam introduced two new single-wafer systems: the Model 4000 for silicon and the Model 5000 for oxide. The Model 4000 is priced at ¥65 million, and the Model 5000 sells for ¥75 million.

The 4000 uses a 13.5–MHz power supply, and the 5000 uses 380 KHz. Both use a clamp ring and helium cooling behind the wafer. These systems represent a departure from the Lam Research models 480 and 580, which TEL/Lam still sells in Japan. Dataquest estimates that 300 of these older systems are installed in Japan, divided equally between the two systems. Although 70 percent of the demand was for polysilicon applications before 1988, most of the interest was for oxide in 1988.

The new systems are part of a strategy to compete against Lam Research's Rainbow etcher in Japan, while continuing to sell the older etchers into Lam's installed base when capacity expansions are necessary. Dataquest estimates that five of the new systems had been sold at the time of the show.

Tokyo Ohka Kogyo (TOK)

TOK has horizontally integrated the major photoresist processes, from spinner/coaters to downstream etching. It is also one of the largest photoresist suppliers in the world. This year, TOK featured two of its new products: the TUE–111 single–wafer, oxide etcher and the TCA–2400 single–wafer, downstream stripper. The TUE–111 sells for ¥60 million, and the TCA–2400 is priced at ¥24 million.

Although there had been no shipments of the TUE–111 as of November 1988, Dataquest believes that 50 of the TCA–2400 systems were shipped in 1988.

Ulvac Japan Ltd. (UJL)

UJL is part of the Ulvac Group, which includes 26 affiliates. It was founded in 1952 as Ulvac Corporation. In the fiscal year ending June 30, 1987, the Ulvac Group had sales of ¥75 billion ($510 million at ¥147/$), of which ¥34 billion ($233 million) were attributable to UJL. Approximately ¥25 billion ($170 million) or 74 percent were for sales of vacuum systems.

Ulvac is one of the licensees of the NTT ECR technology. The company featured its Model MEX–9200 microwave plasma etching system employing that license. The system is configurable to 200mm wafers. Price and shipment information for the system was not available.

Of considerable interest was the strategy represented by the Model C–2111, a multichamber processing system discussed in the PVD section. Ulvac has formed a joint venture with Emergent Technologies to develop a downstream, single–wafer stripper for inclusion into the multichamber system. This will bring sputter etch, selective tungsten CVD, sputtering (including optional rf bias and heating for planarization), infrared lamp anneal, and downstream stripping into the system.

IMPLANT

Ion implantation systems have undergone a tremendous recovery from the low sales levels of the last three years. The following paragraphs describe some interesting new products in medium–current and high–voltage implanters.

Applied Materials

Applied Materials featured its Precision 9003 high–current implanter. The success of this relatively new product has been slow, possibly due to the economic conditions and overcapacity in implantation systems that existed at the time of introduction. The product is picking up speed, particularly in Europe and North America. The company had four systems installed in Japan at the time of the show.

Genus/Ionex

Genus' IX–1500 was featured at Innotech's booth this year. The interest in this system suggests that Japan will begin moving into high–voltage processing for the 4Mb and 16Mb era devices. The system is a tandem accelerator capable of 1.5–MeV beam energies for singly charged ions. The company installed three systems in Japan in 1988 and has orders for several more.

Nissin Electric

Nissin featured two new products at the show this year: the 200–SR medium–current implanter and a 1.5–MeV tandem high–voltage implanter. The 200–SR follows the pattern of the ASM Implant (recently acquired by Varian) medium–current implanter in bringing innovation to an older product line. The system rotates the single–wafer platen, which has a programmable implant angle. This offers better uniformity and allows better process versatility with respect to implant channeling. The system sells for ¥130 million. The company shipped approximately 10 systems in 1988.

Nissin also introduced its new high–voltage implanter, the Model NT–1000. The energy of the beam for singly charged ions is 2.0 MeV. The system features programmable control of implant angle and orientation angle. The energy of the accelerator is 1,000 KeV. This differs from the tandem accelerator being produced by Genus/Ionex, which has voltage of 750 KeV. The price of the system is ¥250 million. None had been shipped at the time of the show.

Sumitomo–Eaton

Sumitomo–Eaton also experienced profound growth in sales of high–current systems. The company exhibited its products but introduced no new products. There were no medium–current or high–voltage system sales in Japan in 1988.

TEL/Varian Ltd. (TVL)

TVL experienced profound growth in implanter sales in 1988, in both medium-current and high-current implanters. No high-voltage systems were sold in 1988. Although TVL did not exhibit any new products at the show this year, it did feature Varian's new Model 1000. The company does not have any installations of the new high-current system, but it will install a system at its applications center at Nirasake in the spring.

Ulvac

Ulvac also introduced its Model IPX-7000 medium-current implanter. The Ulvac system and the Nissin system both employ innovations that will target the 4Mb and 16Mb DRAM device processes. This new system also can rotate the platen at 10 to 60 rpm. The platen angle is programmable from 0 to 45 degrees. The system sells for ¥190 million, and the company shipped five systems in 1988.

PROCESS CONTROL

Two significant introductions in the area of process control occurred at SEMICON/Japan this year, both in the area of critical dimension (CD) SEM measurement systems. Akashi Beam Technology (ABT) and Hitachi, two of the leaders in CD SEM measurement systems, exhibited their newest systems. What makes these newest introductions significant is the clean and simplified design of the systems' control panels. The operating console of a typical SEM system has a multitude of dials and knobs in order to provide maximum system flexibility for measurement and analysis in the analytical lab environment. This level of complexity, however, often requires an operator with advanced training in order to run the system. The simplified control panel of the newer systems provides easy operation and is one of the essential features distinguishing the newest generation of CD SEM measurement systems being developed for the semiconductor production environment.

Akashi Beam Technology (ABT)

ABT exhibited a new critical dimension (CD) measurement system based on SEM technology at SEMICON/Japan. First announced at SEMICON/East in September 1988, the MEA-4000 is a low-voltage SEM system with measurement capability from 0.1 micron to 28.0 microns with 0.01 (3 sigma) reliability. The system has through-the-wall mounting and can handle 125mm, 150mm, and 200mm wafers. Throughput is greater than 15 wafers per hour at three measurement sites per wafer. In addition, the system has a simplified control panel as compared with its predecessor, MEA-3500F, and other typical SEM systems. The price of MEA-4000 is ¥120 million. Several systems were shipped to Japanese semiconductor manufacturers during 1988.

Hitachi

Hitachi introduced a new CD SEM measurement system, the S–7000, which is a new and enhanced version of its popular S–6000 CD SEM. One new major design feature of the S–7000 is that it provides five–axis control (x, y, z, tilt, and rotation), whereas the S–6000 provides only x–y control. Measurement capability of the system is down to 0.1 micron with 0.02–micron measurement reliability. Wafer throughput is five wafers per hour at five measurement sites per wafer. The S–7000 can handle wafers of 100mm, 125mm, and 150mm diameter. Shipment of the S–7000, priced at ¥120 million, began in September 1988. Dataquest believes that five systems were shipped to customers in Japan by the end of 1988.

In addition to the S–7000, Hitachi is still selling its popular S–6000 CD SEM measurement system. Dataquest estimates that Hitachi has sold in excess of 150 systems since it was first introduced at SEMICON/West in 1985. The Hitachi S–6000 is considered by many to be the first CD SEM measurement system specifically designed for the front–end production environment. The S–7000, like its predecessor, has a simplified control panel for easy operation in the fab environment.

EQUIPMENT REPRESENTATIVE: INNOTECH CORPORATION

Innotech, founded in 1985, is a relatively new equipment representative in Japan. In the short time it has been in existence, the company has attracted many new and promising companies as clients. Table 1 presents a list of the companies and products represented by Innotech.

Table 1

Equipment Companies Represented by Innotech

Company Name	Products
Cadence	A full spectrum of IC design solutions
Schlumberger	IDS-5000 CAD/CAE system Sentry S-50 VLSI tester
AOT Corporation	Model OT-2000/4000
TMA Corporation	Process/device simulator
Optical Specialties	MV-500 CD wafer inspection
UTI	Qualitorr 221
Genus Incorporated	Model-8710 CVD system for tungsten and tungsten silicide films Model IX-1500 high-voltage implanter
FSI Corporation	Excalibur gaseous nitrous oxide film removal Megasonic Cleaning System Saturn and Mercury acid processing systems
Matrix	System I Stripper single-wafer, downstream stripper

Source: Dataquest
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DRAM CAPACITY

One pressing issue not only for the semiconductor industry but also for the electronics industry is that of DRAM availability. The shortages caused by the trade sanctions, which were imposed by the U.S. government on DRAMs, caused an increase in memory prices that put the non–Japanese systems manufacturers at a disadvantage with respect to their Japanese competitors. For the last two years, however, semiconductor manufacturers, especially Japanese companies, have been adding DRAM capacity.

We estimate that memory capacity as measured in total bits will increase approximately 60 percent in 1989 over 1988. This includes both the new 1Mb DRAM capacity and the conversion of 256Kb DRAM capacity to 1Mb DRAM capacity. However, because 1Mb devices are very difficult to make and because they employ new manufacturing techniques, their yields may not come up the learning curve as quickly. The actual increase in bit capacity may, therefore, be much lower than 60 percent. This situation would provide an advantage for the Japanese systems manufacturers, allowing them to wrest more market share from their offshore competitors.

One consequence of a reduced capacity for DRAMs would be to soften the impact of an industry recession on the semiconductor equipment industry. The demand would continue for advanced equipment in order to meet the demand for memory devices. It would also increase the incentive for non–Japanese semiconductor manufacturers to reenter the DRAM and SRAM arenas. From this analysis, we can understand that Sematech, and its focus on memories, is important from a semiconductor manufacturing standpoint. When viewed in the context of a worldwide electronics industry strategy, however, it looms in significance.

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