Multichip Modules

Dataquest

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Foreword

Multichip modules are a major new trend in component packaging technology. MCM user's can take advantage of this technology to build more competitive products -- products that use less power or are faster or smaller. MCM user's can optimize their product design and procurement of various MCM technologies based on the information available in this study.

The objective of the *Multichip Modules: Issues and Trends* study is to provide participants with comprehensive information that is qualitative as well as quantitative on the critical trends and major opportunities for multichip module products in the global electronics market.

The written analysis and data assembled in the study were accomplished by Howard Z. Bogert and Mary A. Olsson. The semiconductor component and application forecasts were provided by Jerry Banks, Gary Grandbois, Jim Handy, Brian Lewis, Ken Lowe, Lane Mason and Greg Sheppard of Dataquest.

Chapter 1 — Executive Summary

Multichip module (MCM) technology in production today offers reduced interconnect line width over traditional board technologies in density efficiencies and less area of silicon per package. The advantages of using MCM technology are that high lead count die, on a high interconnect density substrate, require less than 1 mil pitch, and offer 50% to 60% package efficiencies over single chip packages on a PCB which require 4 mil to 8 mil geometries. The disadvantages of MCM technology are that it is a new technology, it is in the prototyping stage for most suppliers to the merchant market, and there is a lack of general consensus on how to handle MCM test issues.

The types of MCM technology that will be covered in this study will be referenced by the acronyms MCM-L (L = laminated), MCM-C (C = cofired), and MCM-D (D = deposited), as defined by IPC-MC-790 classifications. Dataquest's market definition for a multichip module is as follows:

- A module interconnects two or more chips on a single substrate.
- A module achieves higher computation clock rates by reducing propagation delays between chips.
- A module has the potential to be less expensive than conventional technology for highly interconnected digital circuits.
- It doesn't matter how the module is constructed so long as it fills the market need.

The goal of this study is to answer the following questions:

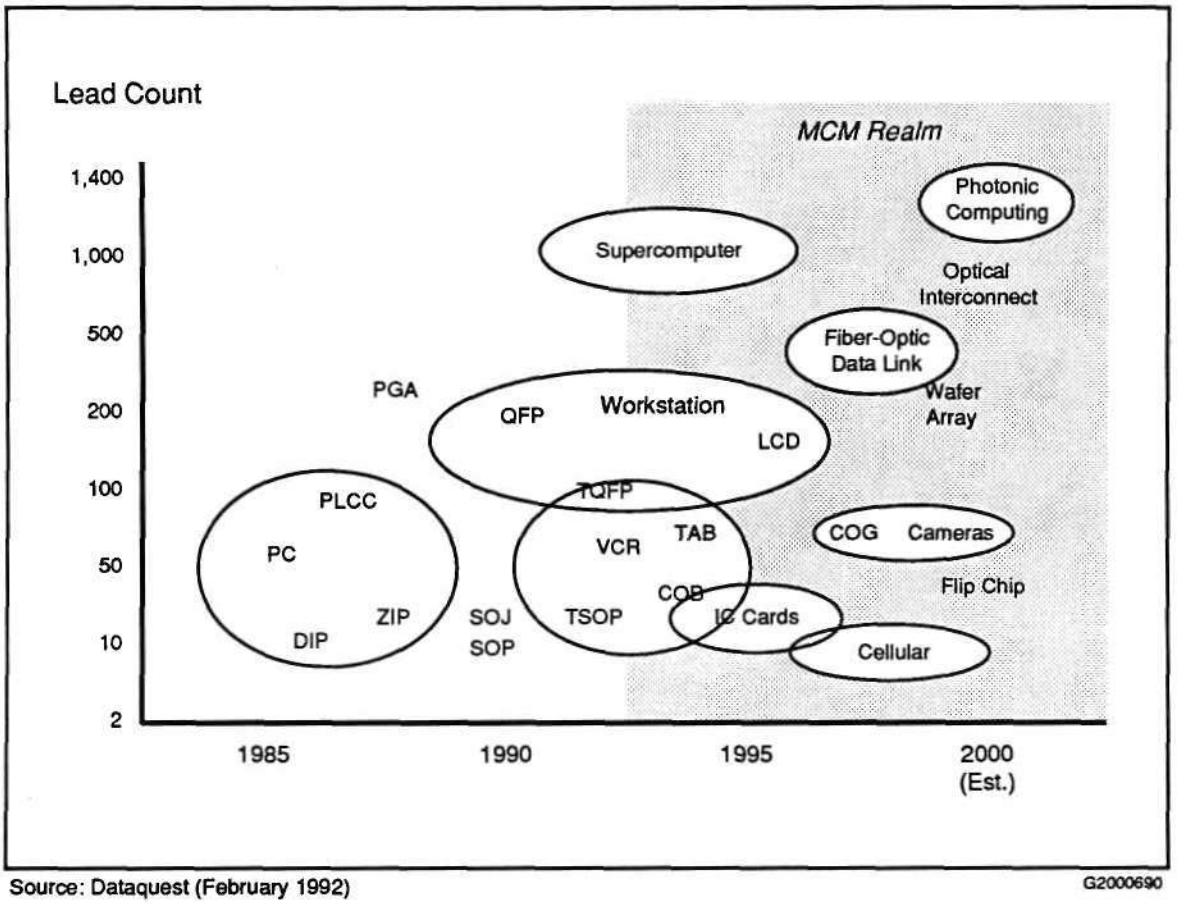
- What performance improvements can be achieved now and in the future through MCM technology?
- What are the current and future MCM costs likely to be?
- What problems stand in the way of more complete MCM implementation?
- What are the capabilities and costs of the different MCM technologies?
- Who are the major MCM vendors and what services do they supply?

Methodology

To set the full business context of the MCM market from 1990 through 2000, Dataquest provides the following:

- Estimated share of available bare die that could be configured in a MCM design.
- Estimated share of electronic equipment that has one or more MCMs.
- Estimated percentage of the semiconductors in that equipment that are designed in a MCM configuration.
- Estimated MCM value in electronic equipment.

Figure 1.4.1
MCM Application Drivers



Source: Dataquest (February 1992) G2000690

General Assumptions

After surveying suppliers and users of MCM technology, Dataquest has concluded the following:

- MCMs will only be designed into new products.
- The majority of MCM designs will be consumed in the dataprocessing, consumer, and communication application markets by 1995.
- The propensity for designers to switch to MCMs for various types of applications will be driven basically by the performance application segments, all other segments are cost driven.
- Captive share of the MCM market is approximately 80 percent of total MCM revenue in 1992.

Multichip Module Drivers

As shown on Figure 1.4.1, the application drivers for MCM technology will continue to flow from the computer sector. The premier metric of computer economics is price/performance, essentially, the dollar cost of one performance unit. As one of the fundamentals of buyer decision making, a low price/performance ratio has one compelling benefit: volume sales.

In terms of price/compute performance, the average 1991 workstation will remain over six times superior to the average supercomputer and over thirty-one times that of the average mainframe. This gap will widen substantially over the next five years. By 1997, the average workstation price/performance should be thirteen times lower than that of a supercomputer and seventy-three times lower than for a mainframe. The primary drivers widening this gap for the workstation are shortened design cycles allowing rapidly accelerating performance improvements, coupled with rapidly accelerating shipment volumes, and hence, price declines. Significantly, Dataquest anticipates that workstation price/performance will even that of personal computers by 1993.

However, in terms of absolute compute power, the highest performance product segment in the computer industry remains the supercomputer. Dataquest anticipates that the average mainframe will reach today's average supercomputer performance level in the 1994-1995 timeframe and the average workstation this same performance in the 1999-2000 timeframe.

The workstation segment is progressing at a relatively fast rate compared to other segments because of the design time for systems development and hence new technology incorporation. Mainframes and supercomputers typically take 3-7 years for design compared to 9 months to two years for a workstation. While both supercomputers and workstations today often incorporate similar CPUs (eg. RISC), several key differences remain which add to the system design time for the larger systems. The most significant ones contributing to the complexity of the supercomputer and mainframe hardware and software design include the following:

- Prevalence of multiprocessor technology.
- Specialized vector processors.
- More advanced and complex I/O subsystem and communications requirements.

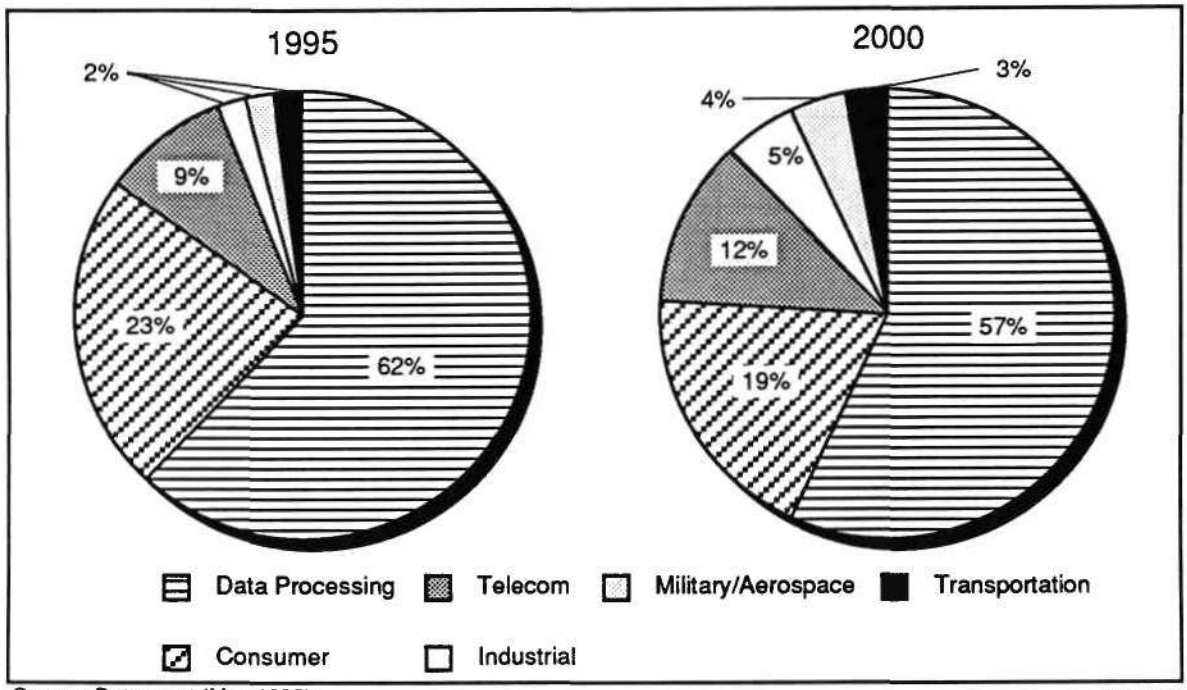
In the 1995 timeframe, the dataprocessing segments are expected to represent 62 percent of MCM revenue worldwide. MCM-C and MCM-D will be the prevalent MCM technologies of this share of market.

Overall, workstation performance and MCM market development are keyed to the continued market dominance of five chip technologies: HP PA, MIPs, Motorola 68000, IBM POWERchip, and SPARC. Within the workstation technology arena, the HP PA architecture provides the industry's leading RISC performance. This combined superscalar/superpipelined architecture is capable of up to 66 MHz in CMOS. In 1991, HP PA represented approximately 3.6 percent of the total workstations shipped. However, by 1995, PA RISC is expected to represent 11 percent of the total workstation shipments.

Dataquest assumes that the MIPs RISC architecture will allow more agressive performance enhancements since the superpipeline design will allow comparable performance to a superscalar implementation with less silicon. Moreover, we assume caches will initially be larger with such pipelined architectures.

Our workstation forecast assumes an agressive increase in the IBM's RISC shipments, rising from 8.1 percent of the 1990 workstation total units to 20 percent of the 1997 workstation shipment total. In the final analysis, we believe that it is more likely that architectures dependent on clock speed will achieve leading performance (eg. superpipelined) than those dependent on complex logic (eg. superscalar).

Figure 1.4.2
Worldwide MCM Revenue Share by Applications



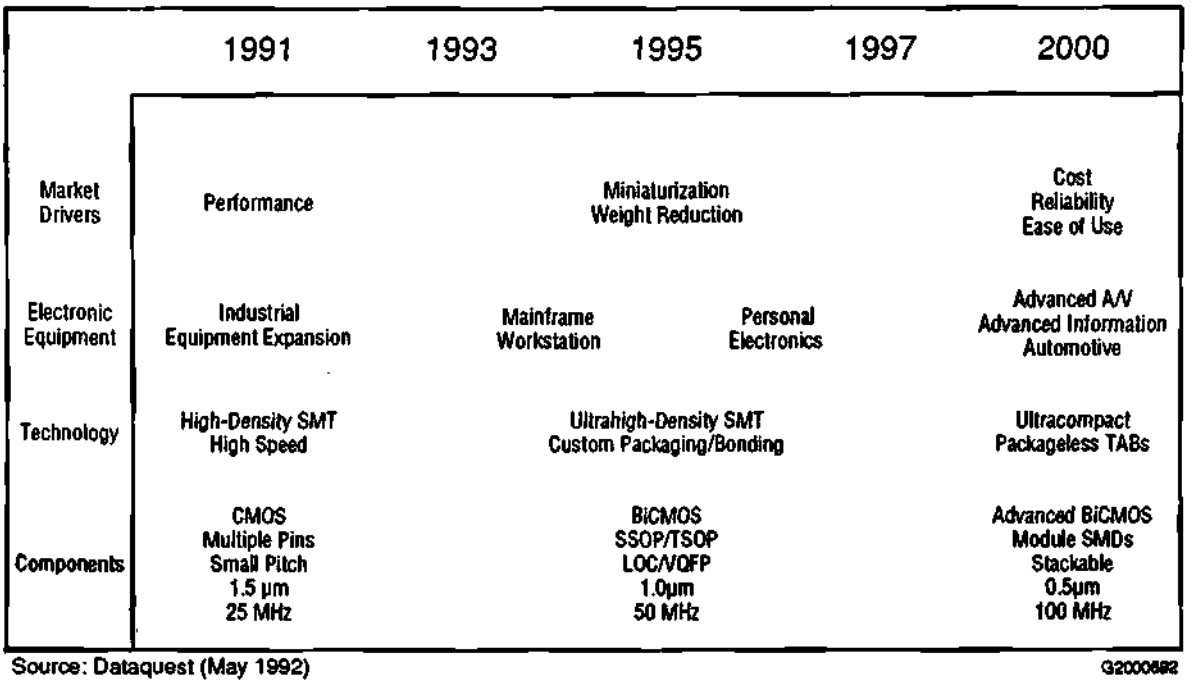
Source: Dataquest (May 1992) G2000691

Overall, due to intense marketshare competition among workstation participants, Dataquest forecasts that over 60 percent of the total systems shipped in the 1992 timeframe will be entry level systems, consisting of 1 to 2 generation-mature RISC technology. In the 1993-1995 timeframe, the average desktop workstation performance will be fueled by the following key factors:

- Emergence of BICMOS technology.
- Superscalar floating point.
- Branch prediction.
- Full 64-bit RISC implementations.
- MCM packaging efficiences.
- Enhanced memory performance due to volume availability of 4Mb SIMMs.
- Larger on-chip caches for superpipelined architectures.

As shown on Figure 1.4.2, the consumer market will represent the second largest share of MCM revenue by 1995, while communications is expected to represent a 9 percent share. MCM-L will be the prevalent technology of these two markets.

Figure 1.4.3
Emerging Package Trends



Source: Dataquest (May 1992)

As part of the continuing review of emerging package trends as illustrated on Figure 1.4.3, other markets and technology drivers that will promote the MCM market will be analyzed extensively in Chapters 2 and 3 of this study.

Chapter 2 — Multichip Module Forecast

Introduction

The worldwide packaging forecast is an evaluation of the single-chip package production for active integrated circuit (IC) devices as well as the available bare die shipped from 1990 through 1996, with projections to 2000. The estimated share of available bare die that potentially could be absorbed into varying MCM configurations are projected by region. This data has been provided to illustrate the potential development of new interconnect technology as well as potential displacement or erosion of other competing package technologies.

Package Forecast

The worldwide forecast shown in Table 2.2.1 represents the total number of single-chip packaged active ICs produced in the four major regions tracked by Dataquest. The forecast is based on the most recent Dataquest IC forecast. The number for bare die represents unpackaged ICs.

Of the total ICs projected to be shipped in 1992, an estimated 40 percent will still be housed in through-hole (TH) packages, as shown on Figure 2.2.1. TH share will continue its decline dropping to approximately 16 percent of the total share by 1995.

Regionally, as shown in Tables 2.2.2 through 2.2.5, Japan is expected to remain the dominant supplier of both SMT packages as well as bare die to the worldwide markets.

Semiconducctor Component Forecasts

During the last two years a major divergence in packaging and interconnect technologies has taken place within the Small Outline (SO) and QUAD. Driven by steady increases in microprocessor operating frequencies and bus widths, and reduction in line width geometries, along with the evolution of 3.3 volt systems, whole new families of Thin Small Outline (TSOP), Thin Shrink Small Outline (TSSOP), Thin Quad (TQFP) and Shrink QUAD (SQFP) packages have emerged. For the CMOS and advanced BICMOS logic circuits, as shown in Tables 2.3.1 through 2.3.5 the 25 mil fine pitch package offers the smallest footprint available.

ASIC

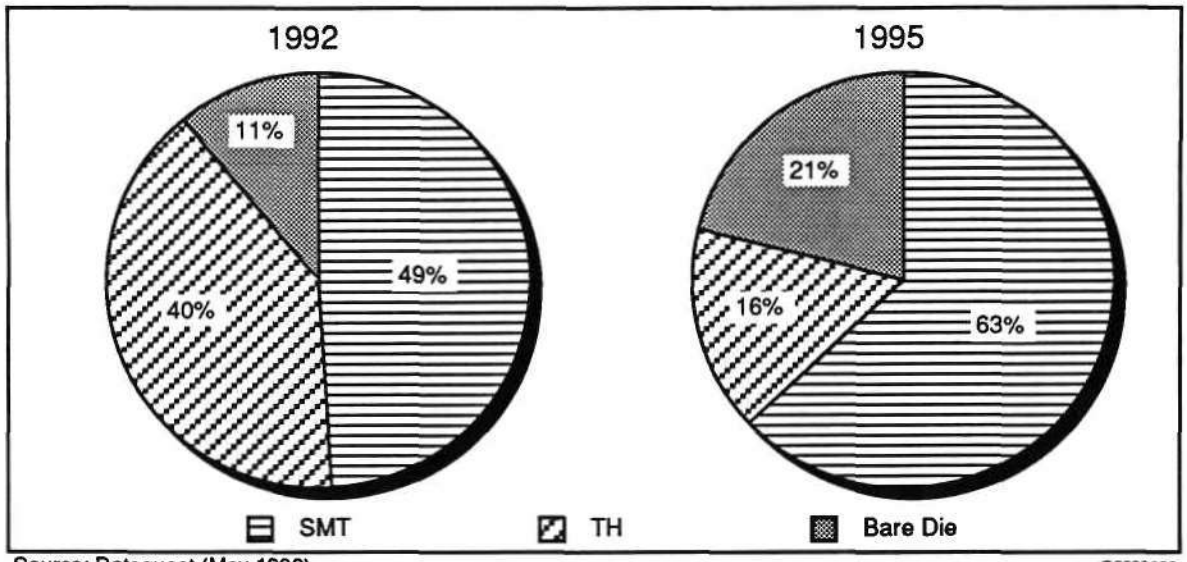
CMOS continues to be the mainstream technology accounting for over 72 percent of the total market revenue in 1992. The BICMOS gate array forecast has been downgraded from original estimates. Future robust growth is questionable as suppliers of CMOS continue to extend the limits of CMOS and interconnect technology. Challenges for ASIC technology during the next five years will come from 100 MHz clock rates and 600 pin counts. Table 2.4.1 shows the estimated worldwide gate array forecast by region and technology. Tables 2.4.2 through 2.4.5 show the collective gate array package production by region.

Table 2.2.1
Estimated Worldwide Package Production

	1990	1991	1992	1993	1994	1995	1996	2000
Plastic DIP	20575	17549	14264	11056	8120	5818	4350	1880
Ceramic DIP	3169	2801	2616	2304	2142	1922	1770	1238
QUAD	4068	5169	7024	10140	14399	16781	18550	24400
Ceramic Chip Carrier	260	271	292	312	350	325	292	140
Plastic Chip Carrier	431	579	724	834	767	663	613	270
SO	10602	12053	13576	14809	16860	19058	20811	32700
Ceramic PGA	265	395	602	762	795	742	660	458
Plastic PGA	147	248	512	744	865	850	801	512
Bare Chip	2878	4153	4905	6604	9409	12011	16053	39691
Total	42395	43218	44515	47565	53707	58170	63900	79329

Source: Dataquest, May, 1992

Figure 2.2.1
Worldwide Package Share



Source: Dataquest (May 1992)

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Table 2.2.2
North America-Estimated Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Plastic DIP	9500	9109	8400	7500	6300	5100	3700	2509	1840	780
Ceramic DIP	1487	1453	1450	1322	1220	1040	983	872	818	638
QUAD	181	450	844	1355	2149	3340	4700	5300	5600	6700
Ceramic Chip Carrier	112	170	188	200	221	245	288	270	244	120
Plastic Chip Carrier	166	222	240	400	530	645	603	511	470	220
SO	1100	1219	1600	1595	1800	2100	2920	3738	3727	6800
Ceramic PGA	78	96	124	185	285	365	335	290	244	159
Plastic PGA	22	50	65	115	245	340	396	380	360	210
Bare Die	700	750	900	1029	1120	1461	2504	3800	5867	13600
Total	13346	13519	13811	13701	13870	14636	16429	17670	19170	29227

Percent of Total	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Plastic DIP	71.2%	67.4%	60.8%	54.7%	45.4%	34.8%	22.5%	14.2%	9.6%	2.7%
Ceramic DIP	11.1%	10.7%	10.5%	9.6%	8.8%	7.1%	6.0%	4.9%	4.3%	2.2%
QUAD	1.4%	3.3%	6.1%	9.9%	15.5%	22.8%	28.6%	30.0%	29.2%	22.9%
Ceramic Chip Carrier	.8%	1.3%	1.4%	1.5%	1.6%	1.7%	1.8%	1.5%	1.3%	.4%
Plastic Chip Carrier	1.2%	1.6%	1.7%	2.9%	3.8%	4.4%	3.7%	2.9%	2.5%	.8%
SO	8.2%	9.0%	11.6%	11.6%	13.0%	14.3%	17.8%	21.2%	19.4%	23.3%
Ceramic PGA	.6%	.7%	.9%	1.4%	2.1%	2.5%	2.0%	1.6%	1.3%	.5%
Plastic PGA	.2%	.4%	.5%	.8%	1.8%	2.3%	2.4%	2.2%	1.9%	.7%
Bare Die	5.2%	5.5%	6.5%	7.5%	8.1%	10.0%	15.2%	21.5%	30.6%	46.5%
Total	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%

Source: Dataquest, May, 1992

Table 2.2.3
Japan-Estimated Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Plastic DIP	7450	6723	6000	4805	3650	2300	1250	950	800	200
Ceramic DIP	1745	1333	980	840	800	705	645	588	500	265
Quad	1800	2100	2402	2700	3100	3800	4900	5500	5840	5600
Ceramic Chip Carrier	42	38	30	28	26	21	19	14	10	0
Plastic Chip Carrier	132	144	122	100	89	70	54	32	27	0
SO	3414	3723	4334	5013	5935	6290	7140	7920	9060	15900
Ceramic PGA	44	59	85	120	195	255	298	300	280	198
Plastic PGA	7	22	60	90	180	300	365	370	342	220
Bare Die	894	1059	1550	2620	3174	4226	5492	6051	6912	14726
Total (Single Chip)	15528	15201	15563	16316	17149	17967	20163	21725	23771	37109
Percent of Total	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Plastic DIP	48.0%	44.2%	38.6%	29.4%	21.3%	12.8%	6.2%	4.4%	3.4%	.5%
Ceramic DIP	11.2%	8.8%	6.3%	5.1%	4.7%	3.9%	3.2%	2.7%	2.1%	.7%
Quad	11.6%	13.8%	15.4%	16.5%	18.1%	21.1%	24.3%	25.3%	24.6%	15.1%
Ceramic Chip Carrier	.3%	.2%	.2%	.2%	.2%	.1%	.1%	.1%	.0%	.0%
Plastic Chip Carrier	.9%	.9%	.8%	.6%	.5%	.4%	.3%	.1%	.1%	.0%
SO	22.0%	24.5%	27.8%	30.7%	34.6%	35.0%	35.4%	36.5%	38.1%	42.8%
Ceramic PGA	.3%	.4%	.5%	.7%	1.1%	1.4%	1.5%	1.4%	1.2%	.5%
Plastic PGA	.0%	.1%	.4%	.6%	1.0%	1.7%	1.8%	1.7%	1.4%	.6%
Bare Die	5.8%	7.0%	10.0%	16.1%	18.5%	23.5%	27.2%	27.9%	29.1%	39.7%
Total	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%

Source: Dataquest, May, 1992

Table 2.2.4
Europe-Estimated Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Plastic DIP	3900	3780	3600	3100	2600	2245	2070	1570	1210	800
Ceramic DIP	777	638	588	510	494	481	466	430	424	318
QUAD	198	278	710	880	1020	1500	2100	2600	3100	5600
Ceramic Chip Carrier	36	37	41	42	44	45	42	40	37	19
Plastic Chip Carrier	40	42	46	48	51	62	60	57	54	31
SO	1300	1600	2090	2180	2230	2550	2700	2800	2774	3500
Ceramic PGA	14	22	52	85	115	132	150	140	122	90
Plastic PGA	6	11	20	40	82	95	92	88	85	70
Bare Die	172	228	306	367	451	703	1079	1634	2405	5275
Total	6443	6636	7453	7252	7087	7813	8759	9359	10211	15703
Percent of Total	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Plastic DIP	60.5%	57.0%	48.3%	42.7%	36.7%	28.7%	23.6%	16.8%	11.8%	5.1%
Ceramic DIP	12.1%	9.6%	7.9%	7.0%	7.0%	6.2%	5.3%	4.6%	4.2%	2.0%
QUAD	3.1%	4.2%	9.5%	12.1%	14.4%	19.2%	24.0%	27.8%	30.4%	35.7%
Ceramic Chip Carrier	.6%	.6%	.6%	.6%	.6%	.6%	.5%	.4%	.4%	.1%
Plastic Chip Carrier	.6%	.6%	.6%	.7%	.7%	.8%	.7%	.6%	.5%	.2%
SO	20.2%	24.1%	28.0%	30.1%	31.5%	32.6%	30.8%	29.9%	27.2%	22.3%
Ceramic PGA	.2%	.3%	.7%	1.2%	1.6%	1.7%	1.7%	1.5%	1.2%	.6%
Plastic PGA	.1%	.2%	.3%	.6%	1.2%	1.2%	1.1%	.9%	.8%	.4%
Bare Die	2.7%	3.4%	4.1%	5.1%	6.4%	9.0%	12.3%	17.5%	23.6%	33.6%
Total	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%

Source: Dataquest, May, 1992

Table 2.2.5
Asia Pacific - Estimated Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Plastic DIP	2790	2654	2575	2144	1714	1411	1100	789	500	100
Ceramic DIP	148	155	151	129	102	78	48	32	28	17
QUAD	4	18	112	234	755	1500	2699	3381	4010	6500
Ceramic Chip Carrier	1	1	1	1	1	1	1	1	1	1
Plastic Chip Carrier	14	17	23	31	54	57	50	63	62	19
SO	1285	1559	2578	3265	3611	3869	4100	4600	5250	6500
Ceramic PGA	3	4	4	5	7	10	12	12	14	11
Plastic PGA	1	2	2	3	5	9	12	12	14	12
Bare Chip	60	72	122	137	160	214	334	526	869	6090
Total	4306	4482	5568	5949	6409	7149	8356	9416	10748	19250
Plastic DIP	64.8%	59.2%	46.2%	36.0%	26.7%	19.7%	13.2%	8.4%	4.7%	.5%
Ceramic DIP	3.4%	3.5%	2.7%	2.2%	1.6%	1.1%	.6%	.3%	.3%	.1%
QUAD	.1%	.4%	2.0%	3.9%	11.8%	21.0%	32.3%	35.9%	37.3%	33.8%
Ceramic Chip Carrier	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
Plastic Chip Carrier	.3%	.4%	.4%	.5%	.8%	.8%	.6%	.7%	.6%	.1%
SO	29.8%	34.8%	46.3%	54.9%	56.3%	54.1%	49.1%	48.9%	48.8%	33.8%
Ceramic PGA	.1%	.1%	.1%	.1%	.1%	.1%	.1%	.1%	.1%	.1%
Plastic PGA	.0%	.0%	.0%	.1%	.1%	.1%	.1%	.1%	.1%	.1%
Bare Chip	1.4%	1.6%	2.2%	2.3%	2.5%	3.0%	4.0%	5.6%	8.1%	31.6%
Total	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%

Source: Dataquest, May, 1992

Table 2.3.1
Estimated Worldwide Standard Logic Package Production
(Millions of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Worldwide Total	3061.2	3055.2	3242.5	3530.4	3739.9	3923.85	4045.8	4117.55	4202	4148.9
DIP	578.3	547.7	349.3	337.3	303.0	247.7	237.3	233.4	229.3	201.2
Plastic	404.2	379.9	215.3	205.6	186.1	155.2	147.5	142.8	139.6	117.3
Ceramic	147.8	142.5	112.0	110.5	98.6	78.9	76.5	76.8	76.1	70.8
Side Brazed	26.3	25.3	22.0	21.2	18.3	13.6	13.3	13.8	13.6	13.2
Flatpack	46.4	45.0	39.9	38.7	38.4	36.6	36.4	36.4	35.7	33.2
Ceramic	41.9	40.7	36.1	35.0	34.8	33.2	33.0	33.0	32.4	30.3
Side Brazed	4.5	4.3	3.8	3.7	3.6	3.4	3.4	3.4	3.3	2.9
Chip Carrier	23.0	25.2	29.3	48.3	62.8	81.6	101.5	129.5	166.4	422.4
Plastic	6.8	6.7	5.0	5.1	5.2	5.2	5.1	5.1	5.2	4.9
Ceramic	16.2	18.5	24.3	43.2	57.6	76.4	96.4	124.3	161.2	417.5
SO	2413.4	2437.3	2404.2	2561.9	2736.1	2922.2	3036.7	3103.0	3173.5	3044.2
QUAD/SQFP	0.0	0.0	419.7	544.2	599.6	635.8	633.9	615.3	597.1	447.9
CMOS	844.5	892.7	694.2	715.0	709.1	720.6	737.4	743.6	742.2	663.6
DIP	4.3	4.6	3.2	3.1	3.0	3.0	3.1	3.1	3.1	2.8
Plastic	3.5	3.6	2.4	2.2	2.1	2.1	2.1	2.1	2.1	1.8
Ceramic	0.6	0.7	0.6	0.7	0.7	0.7	0.7	0.7	0.7	0.7
Side Brazed	0.2	0.3	0.2	0.3	0.3	0.3	0.3	0.3	0.3	0.3
Flatpack	3.3	3.5	3.3	3.5	3.6	3.7	3.8	3.9	3.9	3.6
Ceramic	3.1	3.3	3.2	3.3	3.4	3.5	3.6	3.7	3.7	3.5
Side Brazed	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Chip Carrier	1.9	2.0	1.8	1.9	2.0	2.0	2.1	2.1	2.1	1.9
Plastic	1.0	1.1	0.9	0.9	1.0	1.0	1.0	1.0	1.0	0.9
Ceramic	0.9	1.0	0.9	1.0	1.0	1.0	1.0	1.1	1.1	1.0
SO	835.0	882.6	685.9	706.5	700.5	711.8	728.4	734.5	733.1	655.3
Bipolar	2203.6	2131.3	1374.1	1316.1	1307.7	1277.2	1246.4	1237.5	1238.9	1122.9
DIP	573.9	543.0	345.7	333.7	299.3	244.1	233.9	230.0	226.2	198.4
Plastic	400.7	376.1	212.6	203.0	183.3	152.6	145.1	140.5	137.5	115.4
Ceramic	147.2	141.9	111.4	109.8	97.9	78.2	75.8	76.1	75.4	70.1
Side Brazed	26.0	25.0	21.7	20.9	18.0	13.3	13.0	13.5	13.3	12.9
Flatpack	43.1	41.4	36.4	35.0	34.5	32.6	32.2	32.0	31.0	27.6
Ceramic	38.8	37.2	32.8	31.5	31.1	29.3	29.0	28.8	27.9	24.9
Side Brazed	4.3	4.1	3.6	3.5	3.5	3.3	3.2	3.2	3.1	2.8
Chip Carrier	12.1	11.7	9.3	9.1	9.3	9.3	9.2	9.4	9.6	9.4
Plastic	5.8	5.6	4.1	4.1	4.2	4.2	4.1	4.1	4.1	4.0
Ceramic	6.3	6.1	5.1	5.0	5.1	5.1	5.1	5.3	5.4	5.4
SO	1574.5	1535.3	982.6	938.3	964.6	991.2	971.1	966.0	972.1	887.5

Source: Dataquest, May, 1992

Table 2.3.1 (cont.)
Estimated Worldwide Standard Logic Package Production
(Millions of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
BICMOS	4.0	19.6	36.8	60.8	111.3	196.5	298.4	399.0	514.4	823.4
DIP	0.1	0.2	0.3	0.4	0.7	0.6	0.3	0.2	0.0	0.0
Plastic	0.1	0.2	0.3	0.4	0.7	0.6	0.3	0.2	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
SO	3.9	19.4	36.1	59.8	109.6	193.4	293.8	392.9	506.8	811.7
QUAD/SQFP	0.0	0.0	0.3	0.6	1.1	2.5	4.3	5.8	7.6	11.7
GaAs	9.1	11.6	18.4	37.5	51.8	70.6	90.6	118.5	155.5	413.0
DIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.1	0.1	0.1	0.2	0.3	0.3	0.4	0.5	0.7	2.0
Ceramic	0.1	0.1	0.1	0.2	0.3	0.3	0.4	0.5	0.7	2.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	9.0	11.5	18.3	37.3	51.5	70.3	90.2	118.0	154.8	411.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	9.0	11.5	18.3	37.3	51.5	70.3	90.2	118.0	154.8	411.0
SO	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Other MOS	0.0	0.0	1119.0	1401.0	1560.0	1659.0	1673.0	1619.0	1551.0	1126.0
SO	0.0	0.0	699.6	857.4	961.4	1025.7	1043.4	1009.6	961.6	689.8
QUAD/SQFP	0.0	0.0	419.4	543.6	598.6	633.3	629.6	609.4	589.5	436.2

Source: Dataquest, May, 1992

Table 2.3.2
North America-Estimated Standard Logic Package Production
(Millions of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
North America Total	1034.5	1029.7	1264.9	1294.2	1373.9	1470.0	1510.6	1552.3	1595.6	1688.1
DIP	251.7	241.8	213.3	205.2	176.6	129.1	126.6	131.7	130.0	126.5
Plastic	125.8	121.0	106.8	102.8	88.6	64.8	63.4	65.9	64.9	63.2
Ceramic	100.6	96.6	85.1	81.8	70.3	51.3	50.4	52.5	51.9	50.6
Side Brazed	25.2	24.2	21.4	20.6	17.7	12.9	12.7	13.2	13.1	12.7
Flatpack	46.4	45.0	39.9	38.7	38.4	36.6	36.4	36.4	35.7	33.2
Ceramic	41.9	40.7	36.1	35.0	34.8	33.2	33.0	33.0	32.4	30.3
Side Brazed	4.5	4.3	3.8	3.7	3.6	3.4	3.4	3.4	3.3	2.9
Chip Carrier	16.2	18.3	21.1	28.1	34.2	41.6	48.4	61.8	81.0	202.8
Plastic	3.8	3.7	3.3	3.2	3.3	3.4	3.4	3.5	3.6	3.6
Ceramic	12.4	14.6	17.8	24.8	30.9	38.2	45.0	58.3	77.4	199.2
SO	720.2	724.6	820.8	833.7	917.7	1034.4	1085.6	1130.3	1170.9	1225.4
QUAD/SQFP	0.0	0.0	169.8	188.6	206.9	228.3	213.7	192.1	178.1	100.2
CMOS	163.0	176.3	166.2	176.0	180.3	185.9	190.8	194.5	195.4	181.9
DIP	1.6	1.8	1.7	1.8	1.8	1.9	1.9	1.9	2.0	1.8
Plastic	0.8	0.8	0.8	0.8	0.9	0.9	0.9	0.9	0.9	0.9
Ceramic	0.6	0.7	0.6	0.7	0.7	0.7	0.7	0.7	0.7	0.7
Side Brazed	0.2	0.3	0.2	0.3	0.3	0.3	0.3	0.3	0.3	0.3
Flatpack	3.3	3.5	3.3	3.5	3.6	3.7	3.8	3.9	3.9	3.6
Ceramic	3.1	3.3	3.2	3.3	3.4	3.5	3.6	3.7	3.7	3.5
Side Brazed	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Chip Carrier	1.6	1.8	1.7	1.8	1.8	1.9	1.9	1.9	2.0	1.8
Plastic	0.7	0.8	0.7	0.8	0.8	0.8	0.9	0.9	0.9	0.8
Ceramic	0.9	1.0	0.9	1.0	1.0	1.0	1.0	1.1	1.1	1.0
SO	156.5	169.2	159.6	169.0	173.1	178.5	183.2	186.7	187.6	174.6
Bipolar	862.0	827.1	728.7	699.9	719.6	723.7	731.2	762.0	775.8	789.2
DIP	250.0	239.9	211.3	203.0	174.1	126.6	124.3	129.5	128.0	124.7
Plastic	125.0	119.9	105.7	101.5	87.1	63.3	62.2	64.8	64.0	62.3
Ceramic	100.0	95.9	84.5	81.2	69.7	50.7	49.7	51.8	51.2	49.9
Side Brazed	25.0	24.0	21.1	20.3	17.4	12.7	12.4	13.0	12.8	12.5
Flatpack	43.1	41.4	36.4	35.0	34.5	32.6	32.2	32.0	31.0	27.6
Ceramic	38.8	37.2	32.8	31.5	31.1	29.0	28.8	28.8	27.9	24.9
Side Brazed	4.3	4.1	3.6	3.5	3.5	3.3	3.2	3.2	3.1	2.8
Chip Carrier	8.6	8.3	7.3	7.0	7.2	7.2	7.3	7.6	7.8	7.9
Plastic	3.0	2.9	2.6	2.4	2.5	2.5	2.6	2.7	2.7	2.8
Ceramic	5.6	5.4	4.7	4.5	4.7	4.7	4.8	5.0	5.0	5.1
SO	560.3	537.6	473.7	454.9	503.7	557.2	567.4	592.8	609.0	629.0

Table 2.3.2. (cont.)
North America-Estimated Standard Logic Package Production
(Millions of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
BICMOS	3.5	18.0	31.7	43.8	66.5	115.6	173.0	219.0	264.4	390.0
DIP	0.1	0.2	0.3	0.4	0.7	0.6	0.3	0.2	0.0	0.0
Plastic	0.1	0.2	0.3	0.4	0.7	0.6	0.3	0.2	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
SO	3.4	17.8	31.1	42.9	65.2	113.3	169.5	214.6	259.1	382.2
QUAD/SQFP	0.0	0.0	0.3	0.4	0.7	1.7	3.1	4.2	5.3	7.8
GaAs	6.0	8.3	12.3	19.5	25.5	32.8	39.6	52.8	72.0	195.0
DIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.1	0.1	0.1	0.2	0.3	0.3	0.4	0.5	0.7	2.0
Ceramic	0.1	0.1	0.1	0.2	0.3	0.3	0.4	0.5	0.7	2.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	5.9	8.2	12.2	19.3	25.2	32.5	39.2	52.3	71.3	193.1
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	5.9	8.2	12.2	19.3	25.2	32.5	39.2	52.3	71.3	193.1
SO	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Other MOS	0.0	0.0	326.0	355.0	382.0	412.0	376.0	324.0	288.0	132.0
SO	0.0	0.0	156.5	166.9	175.7	185.4	165.4	136.1	115.2	39.6
QUAD/SQFP	0.0	0.0	169.5	188.2	206.3	226.6	210.6	187.9	172.8	92.4

Source: Dataquest, May, 1992

Table 2.3.3
Japan-Estimated Standard Logic Package Production
(Millions of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Japan Total	1084.0	1083.6	1341.9	1520.8	1607.7	1657.4	1708.2	1745.9	1769.7	1697.5
DIP	114.0	111.1	62.6	57.1	53.9	50.5	46.7	43.4	41.9	27.2
Plastic	114.0	111.1	62.6	57.1	53.9	50.5	46.7	43.4	41.9	27.2
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	3.0	3.2	6.0	14.7	21.8	28.5	35.9	48.0	63.3	187.3
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	3.0	3.2	6.0	14.7	21.8	28.5	35.9	48.0	63.3	187.3
SO	966.9	969.3	1045.6	1117.2	1163.5	1196.1	1231.2	1257.1	1270.9	1155.6
QUAD/SQFP	0.0	0.0	227.6	331.8	368.5	382.3	394.3	397.4	393.5	327.4
CMOS	322.6	341.0	347.0	376.0	371.8	379.7	387.5	393.1	395.0	363.7
DIP	0.3	0.3	0.3	0.4	0.4	0.4	0.4	0.4	0.4	0.4
Plastic	0.3	0.3	0.3	0.4	0.4	0.4	0.4	0.4	0.4	0.4
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
SO	322.3	340.7	346.7	375.6	371.4	379.3	387.1	392.7	394.6	363.3
Bipolar	757.9	738.1	415.3	378.1	356.6	334.3	308.8	286.8	276.4	179.1
DIP	113.7	110.7	62.3	56.7	53.5	50.1	46.3	43.0	41.5	26.9
Plastic	113.7	110.7	62.3	56.7	53.5	50.1	46.3	43.0	41.5	26.9
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
SO	644.2	627.3	353.0	321.4	303.1	284.2	262.5	243.8	234.9	152.2

Table 2.3.3 (cont.)
Japan-Estimated Standard Logic Package Production
(Millions of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
BICMOS	0.5	1.3	4.6	15.0	39.5	66.9	102.0	138.0	164.0	245.4
DIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
SO	0.5	1.3	4.6	14.9	39.1	66.2	100.9	136.6	162.4	242.9
QUAD/SQFP	0.0	0.0	0.0	0.2	0.4	0.7	1.0	1.4	1.6	2.5
GaAs	3.0	3.2	6.0	14.7	21.8	28.5	35.9	48.0	63.3	187.3
DIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	3.0	3.2	6.0	14.7	21.8	28.5	35.9	48.0	63.3	187.3
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	3.0	3.2	6.0	14.7	21.8	28.5	35.9	48.0	63.3	187.3
SO	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Other MOS	0.0	0.0	569.0	737.0	818.0	848.0	874.0	880.0	871.0	722.0
SO	0.0	0.0	341.4	405.4	449.9	466.4	480.7	484.0	479.0	397.1
QUAD/SQFP	0.0	0.0	227.6	331.6	368.1	381.6	393.3	396.0	392.0	324.9

Source: Dataquest, May, 1992

Table 2.3.4
Europe-Estimated Standard Logic Package Production
(Millions of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Europe Total	592.7	597.6	539.4	590.2	606.7	621.5	632.9	626.9	624.0	569.6
DIP	106.0	103.4	60.3	64.3	63.5	61.9	58.7	54.7	54.5	45.5
Plastic	57.8	56.4	32.8	35.0	34.6	33.8	32.1	29.9	29.8	24.8
Ceramic	47.2	46.0	26.9	28.6	28.3	27.5	26.1	24.3	24.2	20.2
Side Brazed	1.0	1.0	0.6	0.6	0.6	0.6	0.6	0.5	0.5	0.4
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	3.8	3.8	2.2	5.5	6.6	9.3	13.9	15.0	17.1	24.6
Plastic	3.0	3.0	1.7	1.8	1.8	1.8	1.7	1.6	1.6	1.3
Ceramic	0.8	0.8	0.5	3.6	4.8	7.5	12.2	13.4	15.5	23.3
SO	482.8	490.5	454.6	496.7	512.3	525.1	534.5	531.5	527.5	480.2
QUAD/SQFP	0.0	0.0	22.3	23.8	24.2	25.1	25.8	25.6	24.9	19.4
CMOS	243.2	257.1	117.0	136.0	148.0	151.0	157.0	155.0	151.5	118.0
DIP	1.2	1.3	0.6	0.7	0.7	0.8	0.8	0.8	0.8	0.6
Plastic	1.2	1.3	0.6	0.7	0.7	0.7	0.8	0.8	0.7	0.6
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	0.2	0.3	0.1	0.1	0.1	0.2	0.2	0.2	0.2	0.1
Plastic	0.2	0.3	0.1	0.1	0.1	0.2	0.2	0.2	0.2	0.1
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
SO	241.7	255.6	116.3	135.2	147.1	150.1	156.1	154.1	150.6	117.3
Bipolar	349.4	340.3	199.1	212.0	209.3	203.9	193.1	179.8	179.3	149.6
DIP	104.8	102.1	59.7	63.6	62.8	61.2	57.9	53.9	53.8	44.9
Plastic	56.6	55.1	32.3	34.3	33.9	33.0	31.3	29.1	29.0	24.2
Ceramic	47.2	45.9	26.9	28.6	28.3	27.5	26.1	24.3	24.2	20.2
Side Brazed	1.0	1.0	0.6	0.6	0.6	0.6	0.6	0.5	0.5	0.4
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	3.5	3.4	2.0	2.1	2.1	2.0	1.9	1.8	1.8	1.5
Plastic	2.8	2.7	1.6	1.7	1.7	1.6	1.5	1.4	1.4	1.2
Ceramic	0.7	0.7	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.3
SO	241.1	234.8	137.4	146.3	144.4	140.7	133.2	124.1	123.7	103.2

Table 2.3.4 (cont.)
Europe-Estimated Standard Logic Package Production
(Millions of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
BICMOS	0.0	0.1	0.2	1.0	3.0	8.5	14.0	24.0	31.0	90.0
DIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
SO	0.0	0.1	0.2	1.0	3.0	8.5	13.9	23.9	30.8	89.6
QUAD/SQFP	0.0	0.0	0.0	0.0	0.0	0.0	0.1	0.1	0.2	0.5
GaAs	0.1	0.1	0.1	3.2	4.4	7.1	11.8	13.1	15.2	23.0
DIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	0.1	0.1	0.1	3.2	4.4	7.1	11.8	13.1	15.2	23.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.1	0.1	0.1	3.2	4.4	7.1	11.8	13.1	15.2	23.0
SO	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Other MOS	0.0	0.0	223.0	238.0	242.0	251.0	257.0	255.0	247.0	189.0
SO	0.0	0.0	200.7	214.2	217.8	225.9	231.3	229.5	222.3	170.1
QUAD/SQFP	0.0	0.0	22.3	23.8	24.2	25.1	25.7	25.5	24.7	18.9

Source: Dataquest, May, 1992

Table 2.3.5
Asia/Pacific-Estimated Standard Logic Package Production
(Millions of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Asia/Pacific Total	350.0	344.3	96.3	125.2	151.6	175.0	194.1	192.5	212.7	193.7
DIP	106.6	91.5	13.0	10.7	9.0	6.1	5.3	3.6	3.0	2.0
Plastic	106.6	91.5	13.0	10.7	9.0	6.1	5.3	3.6	3.0	2.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	0.0	0.0	0.0	0.1	0.1	2.2	3.3	4.6	5.0	7.7
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.1	0.1	2.2	3.3	4.6	5.0	7.7
SO	243.4	252.8	83.3	114.4	142.5	166.6	185.4	184.1	204.2	183.0
QUAD/SQFP	0.0	0.0	0.0	0.0	0.0	0.1	0.1	0.2	0.6	1.0
CMOS	115.7	118.3	64.0	27.0	9.0	4.0	2.1	1.0	0.3	0.0
DIP	1.2	1.2	0.6	0.3	0.1	0.0	0.0	0.0	0.0	0.0
Plastic	1.2	1.2	0.6	0.3	0.1	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
SO	114.5	117.1	63.4	26.7	8.9	4.0	2.1	1.0	0.3	0.0
Bipolar	234.3	225.8	31.0	26.1	22.2	15.3	13.3	8.9	7.4	5.0
DIP	105.4	90.3	12.4	10.4	8.9	6.1	5.3	3.5	3.0	2.0
Plastic	105.4	90.3	12.4	10.4	8.9	6.1	5.3	3.5	3.0	2.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
SO	128.9	135.5	18.6	15.7	13.3	9.2	8.0	5.3	4.4	3.0

Table 2.3.5 (cont.)
Asia/Pacific-Estimated Standard Logic Package Production
(Millions of Dollars)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
BICMOS	0.0	0.2	0.3	1.0	2.3	5.5	9.4	18.0	55.0	98.0
DIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
SO	0.0	0.2	0.3	1.0	2.3	5.4	9.3	17.8	54.5	97.0
QUAD/SQFP	0.0	0.0	0.0	0.0	0.0	0.1	0.1	0.2	0.6	1.0
GaAs	0.0	0.0	0.0	0.1	0.1	2.2	3.3	4.6	5.0	7.7
DIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Flatpack	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Side Brazed	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	0.0	0.0	0.0	0.1	0.1	2.2	3.3	4.6	5.0	7.7
Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	0.0	0.0	0.0	0.1	0.1	2.2	3.3	4.6	5.0	7.7
SO	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.00	0.0	0.0
Other MOS	0.0	0.0	1.0	71.0	118.0	148.0	166.0	160.0	145.0	83.0
SO	0.0	0.0	1.0	71.0	118.0	148.0	166.0	160.0	145.0	83.0
QUAD/SQFP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0

Table 2.4.1
Estimated Worldwide Gate Array Pin Count Production
Percent of Units

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Technology	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%
MOS	64.9%	65.5%	66.2%	69.7%	72.1%	74.6%	75.9%	75.6%	73.8%	60.0%
Bipolar	32.3%	31.8%	30.4%	26.3%	22.6%	18.6%	14.8%	11.7%	9.2%	6.4%
BICMOS	2.8%	2.7%	3.5%	4.0%	5.2%	6.8%	9.3%	12.8%	16.9%	33.5%
Package Type	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%	100.0%
DIP	12.2%	9.4%	6.2%	3.6%	2.0%	1.0%	.0%	.0%	.0%	.0%
QUAD	28.0%	31.3%	31.8%	35.7%	39.3%	44.5%	44.4%	40.8%	37.0%	23.7%
Chip Carrier	39.2%	34.1%	33.0%	28.3%	24.8%	20.1%	15.9%	13.5%	9.9%	.5%
PGA	18.7%	22.3%	23.5%	22.2%	20.2%	17.6%	19.2%	20.6%	21.6%	20.0%
TAB	.4%	1.4%	2.4%	5.5%	7.2%	7.8%	9.2%	11.1%	14.0%	23.5%
Flip Chip	1.5%	1.5%	2.6%	3.7%	4.5%	6.0%	7.3%	9.0%	10.5%	19.0%
Bare Die	.0%	.0%	.5%	1.0%	2.0%	3.0%	4.0%	5.0%	7.0%	13.3%
Pin Count										
<44	10.6%	6.0%	3.0%	1.0%	.0%	.0%	.0%	.0%	.0%	.0%
44-83	36.2%	33.8%	25.7%	18.0%	10.5%	5.0%	1.5%	.6%	.0%	.0%
84-132	44.0%	41.8%	43.1%	40.5%	35.9%	33.6%	30.0%	27.2%	22.4%	7.3%
133-195	4.9%	10.1%	15.9%	22.8%	28.7%	31.5%	30.6%	27.2%	23.7%	11.7%
196-244	2.2%	4.8%	6.3%	7.8%	10.8%	12.1%	14.3%	15.5%	17.0%	19.3%
244-360	.6%	1.7%	2.3%	3.8%	5.4%	5.9%	7.5%	8.6%	10.5%	13.1%
361-524	.0%	.3%	.6%	1.2%	2.0%	2.5%	4.0%	5.2%	6.2%	9.7%
525-600	.0%	.0%	.0%	.2%	.2%	.3%	.6%	1.2%	1.7%	3.7%
600	.0%	.0%	.0%	.0%	.0%	.1%	.2%	.5%	1.0%	2.9%
DIP	12.2%	9.4%	6.2%	3.6%	2.0%	1.0%	.0%	.0%	.0%	.0%
Plastic	8.1%	7.0%	5.0%	3.5%	2.0%	1.0%	.0%	.0%	.0%	.0%
<44	7.0%	4.0%	2.0%	1.0%	.0%	.0%	.0%	.0%	.0%	.0%
44-83	1.1%	3.0%	3.0%	2.5%	2.0%	1.0%	.0%	.0%	.0%	.0%
Ceramic	4.1%	2.4%	1.2%	.1%	.0%	.0%	.0%	.0%	.0%	.0%
<44	3.5%	2.0%	1.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
44-83	.6%	.4%	.2%	.1%	.0%	.0%	.0%	.0%	.0%	.0%

Table 2.4.1 (cont.)
Estimated Worldwide Gate Array Pin Count Production
Percent of Units

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
QUAD										
Plastic	23.8%	27.0%	27.7%	31.3%	34.1%	38.4%	36.6%	32.5	27.7%	15.6%
<44	.1%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
44-83	8.5%	8.0%	4.8%	3.0%	1.0%	.5%	.5%	.1%	.0%	.0%
84-132	12.8%	13.0%	13.0%	11.0%	10.0%	9.5%	8.5%	7.3%	5.0%	.3%
133-195	1.1%	3.5%	7.0%	13.5%	17.4%	21.9%	20.5%	17.4%	14.0%	2.6%
196-244	1.1%	1.8%	2.2%	2.8%	4.0%	4.4%	4.5%	4.5%	5.0%	6.1%
244-360	.2%	.7%	.7%	.9%	1.5%	1.8%	2.1%	2.5%	2.7%	4.1%
361-524	.0%	.0%	.0%	.1%	.2%	.3%	.5%	.7%	1.0%	2.5%
Ceramic	4.2%	4.3%	3.9%	3.3%	2.6%	2.3%	1.8%	1.3%	1.0%	.0%
<44	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
44-83	1.5%	1.1%	1.0%	.8%	.0%	.0%	.0%	.0%	.0%	.0%
84-132	1.3%	1.5%	1.0%	.5%	.5%	.5%	.2%	.0%	.0%	.0%
133-195	1.0%	1.1%	1.0%	1.0%	1.0%	.5%	.3%	.1%	.0%	.0%
196-244	.3%	.5%	.8%	.9%	1.0%	1.2%	1.3%	1.2%	1.0%	.0%
244-360	.1%	.1%	.1%	.1%	.1%	.1%	.0%	.0%	.0%	.0%
361-524	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
Metal QUAD	.0%	.0%	.2%	1.1%	2.6%	3.8%	6.0%	7.0%	8.3%	8.1%
84-132	.0%	.0%	.1%	.5%	1.0%	1.3%	2.0%	2.3%	3.0%	2.5%
133-195	.0%	.0%	.1%	.5%	1.1%	1.5%	2.3%	2.7%	3.2%	3.1%
196-244	.0%	.0%	.0%	.1%	.5%	1.0%	1.7%	2.0%	2.1%	2.5%
Chip Carrier										
Plastic	36.6%	31.5%	30.4%	25.9%	22.4%	18.0%	14.0%	12.5%	9.0%	.5%
44-83	13.6%	11.5%	11.0%	8.8%	6.0%	3.0%	1.0%	.5%	.0%	.0%
84-132	23.0%	20.0%	19.4%	17.1%	16.4%	15.0%	13.0%	12.0%	9.0%	.5%
Ceramic	2.6%	2.6%	2.6%	2.4%	2.4%	2.1%	1.9%	1.0%	.9%	.0%
44-83	2.1%	2.0%	1.8%	1.0%	.5%	.2%	.0%	.0%	.0%	.0%
84-132	.5%	.6%	.8%	1.4%	1.9%	1.9%	1.9%	1.0%	.9%	.0%

Table 2.4.1 (cont.)
Estimated Worldwide Gate Array Pin Count Production
Percent of Units

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
PGA										
Plastic	3.1%	5.7%	8.2%	10.2%	9.5%	9.0%	9.8%	9.8%	9.4%	8.1%
<44	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
44-83	.6%	.2%	.1%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
84-132	2.0%	2.5%	3.2%	3.5%	1.0%	1.0%	.8%	.6%	.4%	.0%
133-195	.3%	1.1%	2.0%	3.0%	4.0%	3.3%	3.1%	2.3%	1.3%	.0%
196-244	.1%	1.5%	2.1%	2.5%	3.0%	3.0%	3.5%	3.8%	4.0%	3.3%
244-360	.1%	.3%	.5%	.8%	1.0%	1.0%	1.4%	1.7%	2.0%	2.5%
361-524	.0%	.1%	.3%	.3%	.4%	.5%	.7%	.9%	1.0%	1.6%
525-600	.0%	.0%	.0%	.1%	.1%	.2%	.3%	.5%	.7%	.7%
Ceramic	15.6%	16.6%	15.1%	11.1%	8.8%	6.1%	6.1%	5.9%	5.6%	3.9%
<44	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
44-83	8.2%	7.6%	3.8%	1.8%	1.0%	.3%	.0%	.0%	.0%	.0%
84-132	4.3%	4.0%	5.0%	4.0%	2.0%	1.0%	.3%	.1%	.0%	.0%
133-195	2.4%	4.0%	5.0%	3.2%	2.7%	1.6%	1.2%	.6%	.1%	.0%
196-244	.6%	.6%	.6%	.6%	.5%	.5%	.4%	.3%	.2%	.1%
244-360	.1%	.3%	.5%	1.0%	1.5%	1.5%	2.1%	2.3%	2.3%	1.5%
361-524	.0%	1%	.2%	.5%	1.1%	1.2%	2.1%	2.6%	3.0%	2.3%
524	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
Land Grid Array	.0%	.0%	.2%	.9%	1.9%	2.5%	3.3%	4.9%	6.6%	8.0%
84-132	.0%	.0%	.1%	.5%	.8%	1.0%	1.1%	1.7%	2.0%	2.0%
133-195	.0%	.0%	.1%	.3%	.8%	1.0%	1.2%	1.8%	2.4%	3.0%
196-244	.0%	.0%	.0%	.1%	.3%	.5%	1.0%	1.4%	2.2%	3.0%
TAB	.4%	1.4%	2.4%	5.5%	7.2%	7.8%	9.2%	11.1%	14.0%	23.5%
<44	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
44-83	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
84-132	.1%	.2%	.5%	2.0%	2.3%	2.4%	2.2%	2.2%	2.1%	2.0%
133-195	.1%	.4%	.7%	1.3%	1.7%	1.7%	2.0%	2.3%	2.7%	3.0%
196-244	.1%	.4%	.6%	.8%	1.5%	1.5%	1.9%	2.3%	2.5%	4.3%
244-360	.1%	.3%	.5%	1.0%	1.3%	1.5%	1.9%	2.1%	3.5%	5.0%
361-524	.0%	.1%	.1%	.3%	.3%	.5%	.7%	1.0%	1.2%	3.3%
525-600	.0%	.0%	.0%	.1%	.1%	.1%	.3%	.7%	1.0%	3.0%
>600	.0%	.0%	.0%	.0%	.0%	.1%	.2%	.5%	1.0%	2.9%

Source: Dataquest, May, 1992

Table 2.4.2
North America-Estimated Gate Array Package Production
(Percent of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
North America										
Share of Production	38.4%	37.0%	35.5%	33.3%	32.5%	31.6%	30.8%	30.2%	29.7%	30.0%
Share by Package Type										
DIP	18.0%	13.0%	5.0%	1.0%	.0%	.0%	.0%	.0%	.0%	.0%
QUAD	21.0%	26.0%	36.1%	46.1%	50.7%	54.9%	58.8%	59.2%	54.5%	39.4%
Ceramic	4.0%	3.0%	2.0%	1.7%	1.0%	.7%	.3%	.0%	.0%	.0%
Plastic	17.0%	23.0%	34.0%	44.0%	49.0%	52.5%	56.0%	56.2%	50.0%	28.4%
Metal QUAD	.0%	.0%	.1%	.4%	.7%	1.7%	2.5%	3.0%	4.5%	11.0%
Chip Carrier	44.0%	43.7%	39.5%	30.0%	24.6%	17.5%	9.6%	3.0%	.0%	.0%
Ceramic	4.0%	4.4%	4.2%	3.5%	3.0%	2.5%	1.5%	.5%	.0%	.0%
Plastic	40.0%	39.3%	35.3%	26.5%	21.6%	15.0%	8.1%	2.5%	.0%	.0%
PGA	15.4%	15.4%	15.4%	15.4%	15.2%	14.8%	16.0%	17.3%	16.9%	9.5%
Ceramic	11.1%	10.9%	10.5%	10.1%	9.5%	8.5%	8.1%	6.3%	5.0%	.0%
Plastic	4.3%	4.5%	4.8%	5.0%	5.2%	5.4%	6.6%	8.0%	7.8%	1.5%
Land Grid Array	.0%	.0%	.1%	.3%	.5%	.9%	1.3%	3.0%	4.1%	8.0%
TAB	.1%	.4%	.5%	1.0%	1.5%	2.1%	2.6%	3.7%	5.6%	9.0%
Flip Chip	1.5%	1.5%	3.0%	5.5%	6.3%	7.8%	8.3%	9.7%	12.0%	23.0%
Bare Die	.0%	.0%	.5%	1.0%	1.7%	2.9%	4.7%	7.1%	11.0%	19.1%

Source: Dataquest, May, 1992

Table 2.4.3
Japan-Estimated Gate Array Package Production
(Percent of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Japan										
Share of Production	45.0%	47.7%	48.5%	50.5%	50.2%	50.4%	51.0%	51.7%	52.5%	49.0%
Share by Package Type										
DIP	16.0%	8.0%	5.0%	1.0%	.0%	.0%	.0%	.0%	.0%	.0%
QUAD	39.2%	49.0%	53.7%	59.9%	63.7%	67.0%	65.9%	63.5%	58.3%	45.0%
Ceramic	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
Plastic	39.2%	49.0%	53.6%	59.6%	63.2%	66.0%	64.4%	61.0%	55.3%	39.5%
Metal QUAD	.0%	.0%	.1%	.3%	.5%	1.0%	1.5%	2.5%	3.0%	5.5%
Chip Carrier	33.5%	30.7%	27.0%	23.0%	19.0%	10.0%	3.0%	.5%	.0%	.0%
Ceramic	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
Plastic	33.5%	30.7%	27.0%	23.0%	19.0%	10.0%	3.0%	.5%	.0%	.0%
PGA	10.6%	10.9%	11.5%	12.1%	12.3%	14.3%	16.0%	15.0%	14.0%	7.0%
Ceramic	8.2%	7.1%	5.8%	4.6%	3.0%	1.0%	.5%	.0%	.0%	.0%
Plastic	2.4%	3.8%	5.7%	7.4%	9.0%	12.3%	14.0%	13.0%	11.0%	1.0%
Land Grid Array	.0%	.0%	.0%	.1%	.3%	1.0%	1.5%	2.0%	3.0%	6.0%
TAB	.7%	1.4%	2.6%	3.5%	4.1%	5.7%	6.6%	8.0%	10.0%	16.0%
Flip Chip	.0%	.0%	.1%	.3%	.5%	1.6%	4.5%	6.0%	7.7%	15.0%
Bare Die	.0%	.0%	.1%	.2%	.4%	1.4%	4.0%	7.0%	10.0%	17.0%

Source: Dataquest, May, 1992

Table 2.4.4
Europe-Estimated Gate Array Package Production
(Percent of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
European										
Share of Production	12.7%	11.8%	12.3%	11.9%	12.2%	12.3%	12.1%	11.7%	11.2%	12.0%
Share by Package Type										
DIP	13.0%	8.6%	3.7%	1.5%	.0%	.0%	.0%	.0%	.0%	.0%
QUAD	17.6%	26.9%	36.0%	42.5%	49.3%	52.2%	52.9%	62.2%	65.9%	60.8%
Ceramic	8.1%	7.4%	6.1%	5.3%	4.0%	3.0%	1.0%	.0%	.0%	.0%
Plastic	9.5%	19.5%	29.9%	37.2%	45.2%	49.1%	51.6%	61.7%	65.2%	57.8%
Metal Quad	.0%	.0%	.0%	.0%	.1%	.1%	.3%	.5%	.7%	3.0%
Chip Carrier	43.8%	38.4%	35.0%	30.0%	24.0%	18.0%	13.0%	9.0%	.0%	.1%
Ceramic	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
Plastic	43.8%	38.4%	35.0%	30.0%	24.0%	18.0%	13.0%	9.0%	6.0%	.1%
PGA	25.6%	26.0%	24.8%	25.0%	24.8%	25.8%	28.0%	19.2%	13.6%	4.1%
Ceramic	20.6%	17.0%	12.8%	10.0%	8.8%	6.5%	5.0%	4.1%	3.2%	.5%
Plastic	5.0%	9.0%	12.0%	15.0%	16.0%	19.2%	22.8%	14.8%	9.8%	1.0%
Land Grid Array	.0%	.0%	.0%	.0%	.0%	.1%	.2%	.3%	.6%	2.6%
TAB	.0%	.1%	.3%	.5%	.8%	1.4%	3.3%	4.5%	6.0%	12.0%
Flip Chip	.0%	.0%	.1%	.3%	.6%	1.1%	1.4%	2.1%	3.5%	11.0%
Bare Die	.0%	.0%	.1%	.2%	.5%	1.5%	1.4%	3.0%	5.0%	12.0%

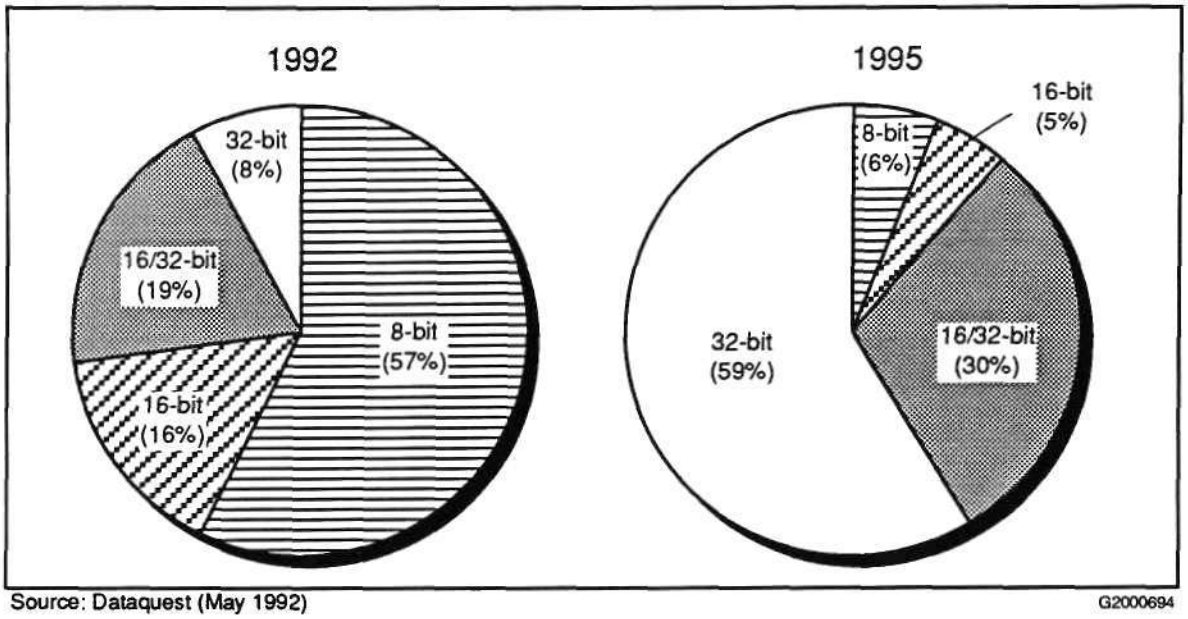
Source: Dataquest, May, 1992

Table 2.4.5
Asia/Pacific-Estimated Gate Array Package Production
(Percent of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Asia/Pacific										
Share of Production	3.9%	3.5%	3.7%	4.3%	5.0%	5.7%	6.1%	6.3%	6.5%	9.0%
Share by Package Type										
DIP	85.0%	63.0%	42.0%	28.9%	9.7%	1.0%	.0%	.0%	.0%	.0%
QUAD	5.0%	15.0%	28.0%	41.0%	58.0%	64.0%	68.6%	69.0%	73.0%	69.0%
Ceramic	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
Plastic	5.0%	15.0%	28.0%	41.0%	58.0%	64.0%	67.6%	64.0%	62.0%	53.0%
Metal QUAD	.0%	.0%	.0%	.0%	.0%	.0%	1.0%	5.0%	11.0%	16.0%
Chip Carrier	5.0%	12.0%	10.0%	10.0%	8.0%	8.0%	7.0%	6.0%	2.0%	.0%
Ceramic	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
Plastic	5.0%	12.0%	10.0%	10.0%	8.0%	8.0%	7.0%	6.0%	2.0%	.0%
PGA	5.0%	10.0%	20.0%	20.0%	24.0%	26.0%	22.0%	21.0%	18.0%	12.0%
Ceramic	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
Plastic	5.0%	10.0%	20.0%	20.0%	24.0%	26.0%	22.0%	21.0%	18.0%	12.0%
Land Grid Array	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
TAB	.0%	.0%	.0%	.0%	.1%	.6%	1.7%	3.0%	5.0%	9.0%
Flip Chip	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%	.0%
Bare Die	.0%	.0%	.0%	.1%	.2%	.4%	.7%	1.0%	2.0%	10.0%

Source: Dataquest, May, 1992

Figure 2.5.1
1991 Worldwide Microcomponent Shipments
(Percent by Bit)



Source: Dataquest (May 1992)

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Microprocessors

The activity level in the 32-bit MPU products represented the largest revenue base in 1991, while the 8-bit market continued to control the unit share as shown in Figure 2.5.1. Table 2.5.1 presents the collective regional data for packaged Microprocessors, and Tables 2.5.2 through 2.5.5 contain the regional microprocessor forecasts.

Table 2.5.1
Estimated Worldwide Microprocessor Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Worldwide Total	98.0	111.0	127.4	141.0	154.2	168.2	183.4	193.7	205.0	216.0
Package Total	98.0	111.0	127.4	141.0	154.2	168.2	183.4	193.7	205.0	216.0
DIP	41.6	36.0	22.0	12.0	6.0	4.0	2.4	1.0	0.3	0.0
QUAD	1.0	2.0	2.8	4.0	5.4	5.7	6.1	6.2	7.0	4.7
Chip Carrier	20.4	23.4	27.2	27.3	24.1	18.5	15.0	8.4	5.3	1.4
PGA	35.0	49.6	75.3	96.6	116.8	136.3	152.5	158.2	160.1	134.9
Bare Die	0.0	0.0	0.1	1.1	1.9	3.7	7.4	19.9	32.3	75.0
Pin Count Total	98.0	111.0	127.3	139.9	152.3	164.5	176.0	173.8	172.7	141.0
40-48	42.0	36.4	22.2	12.2	6.1	4.1	2.4	1.0	0.3	0.0
52-68	45.5	55.0	65.6	68.2	61.7	47.9	36.3	19.8	10.4	4.7
72-84	3.5	10.7	21.2	29.8	38.3	42.5	49.7	44.0	35.8	26.5
114-128	4.5	5.5	11.6	21.2	32.8	46.7	48.8	53.0	48.6	35.2
132-175	2.5	3.4	6.6	8.0	11.4	17.0	27.8	38.0	47.9	40.0
179	0.0	0.0	0.1	0.5	2.0	6.3	11.0	18.0	29.7	34.6
DIP										
Plastic	17.6	16.0	10.0	5.0	2.0	1.0	0.0	0.0	0.0	0.0
40-48	17.6	16.0	10.0	5.0	2.0	1.0	0.0	0.0	0.0	0.0
52-68										
Ceramic	24.0	20.0	12.0	7.0	4.0	3.0	2.4	1.0	0.3	0.0
40-48	24.0	20.0	12.0	7.0	4.0	3.0	2.4	1.0	0.3	0.0
52-68										
QUAD										
Plastic	1.0	2.0	2.8	4.0	5.4	5.7	6.1	6.2	7.0	4.7
52-68	1.0	1.0	0.8	0.7	0.6	0.5	0.3	0.2	0.1	0.0
72-84		1.0	1.8	3.1	4.3	4.5	5.0	5.0	4.9	4.5
114-128			0.2	0.2	0.5	0.7	0.8	1.0	2.0	0.2
Chip Carrier										
Plastic	6.4	6.4	7.2	9.3	8.1	7.5	7.0	4.4	3.0	0.4
40-48	0.4	0.4	0.2	0.2	0.1	0.1	0.0	0.0	0.0	0.0
52-68	6.0	6.0	7.0	9.1	8.0	7.4	7.0	4.4	3.0	0.4
Ceramic	14.0	17.0	20.0	18.0	16.0	11.0	8.0	4.0	2.3	1.0
40-48										
52-68	14.0	17.0	20.0	18.0	16.0	11.0	8.0	4.0	2.3	1.0
PGA										
Plastic										
52-68	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
72-84	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
114-128	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
132-175	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Ceramic	35.0	49.6	75.3	96.6	116.8	136.3	152.5	158.2	160.1	134.9
52-68	24.5	31.0	37.8	40.4	37.1	29.0	21.0	11.2	5.0	3.3
72-84	3.5	9.7	19.4	26.7	34.0	38.0	44.7	39.0	30.9	22.0
114-128	4.5	5.5	11.4	21.0	32.3	46.0	48.0	52.0	46.6	35.0
132-175	2.5	3.4	6.6	8.0	11.4	17.0	27.8	38.0	47.9	40.0
179	0.0	0.0	0.1	0.5	2.0	6.3	11.0	18.0	29.7	34.6

Table 2.5.2
North America-Estimated Microprocessor Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
North America Total	78.6	86.2	102.4	115.2	124.9	134.3	151.9	154.3	159.5	168.4
Package Total	78.6	86.2	102.4	115.2	124.9	134.3	151.9	154.3	159.5	168.4
DIP	39.5	33.7	19.8	10.9	4.9	3.0	2.0	0.7	0.3	0.0
QUAD	1.0	1.5	2.4	3.6	4.4	4.7	5.1	5.2	6.0	3.7
Chip Carrier	16.4	19.1	23.7	23.9	21.8	16.4	14.3	7.8	5.2	1.3
PGA	21.7	31.9	56.4	75.8	92.5	108.6	127.1	131.7	134.4	115.0
Other	0.0	0.0	0.1	1.0	1.3	1.6	3.4	8.9	13.6	48.4

Source: Dataquest, May, 1992

Table 2.5.3
Japan-Estimated Microprocessor Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Japan Total	14.7	17.7	18.0	18.3	20.9	24.2	23.8	29.0	32.8	34.8
Package Total	14.7	17.7	18.0	18.3	20.9	24.2	23.8	29.1	32.8	34.8
DIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
QUAD	0.5	0.5	0.4	0.4	1.0	1.0	1.0	1.0	1.0	1.0
Chip Carrier	2.5	2.5	1.7	1.5	0.5	0.4	0.1	0.0	0.0	0.0
PGA	11.7	14.7	15.9	16.3	18.9	21.2	19.2	18.7	15.4	9.8
Other	0.0	0.0	0.0	0.1	0.5	1.6	3.5	9.4	16.4	24.0

Source: Dataquest, May, 1992

Table 2.5.4
Europe-Estimated Microprocessor Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Europe Total	4.5	6.8	6.8	7.1	8.0	9.2	7.4	9.9	12.1	11.9
Package Total	4.4	6.8	6.8	7.1	8.0	9.2	7.4	9.9	12.1	11.9
DIP	1.9	2.1	2.1	1.0	1.0	1.0	0.4	0.3	0.0	0.0
QUAD	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	1.0	1.8	1.8	1.7	1.6	1.5	0.5	0.5	0.0	0.0
PGA	1.5	2.9	2.9	4.4	5.3	6.2	6.0	7.5	9.8	9.3
Other	0.0	0.0	0.0	0.0	0.1	0.5	0.5	1.6	2.3	2.6

Source: Dataquest, May, 1992

Table 2.5.5
Asia/Pacific-Estimated Microprocessor Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Asia/Pacific Total	0.2	0.3	0.2	0.4	0.4	0.5	0.3	0.4	0.6	0.9
Package Total	0.2	0.3	0.2	0.4	0.4	0.5	0.3	0.4	0.6	0.9
DIP	0.2	0.2	0.1	0.1	0.1	0.0	0.0	0.0	0.0	0.0
QUAD	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Chip Carrier	0.0	0.0	0.0	0.2	0.2	0.2	0.1	0.1	0.1	0.1
PGA	0.0	0.1	0.1	0.1	0.1	0.3	0.2	0.3	0.5	0.8

Source: Dataquest, May, 1992

Memory

Increased demands for high density memory chips in systems designed for miniaturization such as the laptop, notebook and palmtop PCs have resulted in a multitude of memory package and module developments. Although most memory modules continue to be produced by the same semiconductor manufacturer that produces the memory device, the repackaging share for the custom memory module market has grown from 20 percent in 1990, to over 30 percent in 1992. The MOS DRAM, which is the largest product in revenue and unit share of memory products has also continued to maintain the largest growth in memory modules.

Tables 2.6.1 and 2.6.2 list the MOS DRAM package production by density and regions. Table 2.6.3 lists the DRAM module organization and Table 2.6.4 forecasts the development of the emerging DRAM package technologies. Two of the most innovative DRAM packages will be the stackable memory package and the Lead-On-Chip (LOC) package. An example of a stackable memory module is that produced by Irvine Sensors of Costa Mesa, California. Irvine Sensor's product is a thin package of stacked memory chips which are connected at the top by a "cap chip" which allows a variety of conventional manufacturing techniques such as wire bonding, tape automated bonding or solder bumps to be used to interconnect the stack with higher levels of assembly. IBM introduced a stackable memory technology called the Caribou into their systems during the 1980s. Mitsui High Tech Incorporated has designed and assembled a stackable memory TSOP package for memory card applications. The LOC package was patented by IBM (Patent 4,862,245 1989). IBM is currently licensing their LOC design. The package was invented to effectively dissipate heat and improve the performance of higher density devices. Hitachi and Texas Instruments have licensed the LOC package from IBM for their higher density DRAM products. Hitachi tested the package with their 4M DRAM device family. The packaged chip has a plurality of lead frame conductors extending through the encapsulating material which are adhesively joined to the chip. The conductors cover a substantial portion of the chip and thereby serve as conduits for the dissipation of heat from the chip. Wires are bonded to the conductors and extend from the conductors to the terminals on the chip. The chip terminals are designed along the center line of the chip, allowing for short connecting wires which in turn contributes to faster chip response.

The worldwide SRAM package development is summarized in Tables 2.6.5 through Tables 2.6.7. Tables 2.6.8 through Tables 2.6.10 summarize the package data for the EPROM, ROM, and EEPROM families.

Analog

Linear and mixed signal circuits continue to be a fast growing segment of the semiconductor market. A large portion of this growth is driven by microcontroller driven end-use in the consumer and automotive segments. The analog product has been the largest market for SMT. In 1991, demand for SMD outstripped supply in most cases. The linear and mixed-signal products are expected to experience increased growth from compact disk, automotive engine control, air-bag systems, anti-lock brake systems, graphics workstations, electronic test equipment and data acquisition systems. The worldwide and regional data by package types are listed in Table 2.7.1.

Table 2.6.1
Estimated Worldwide MOS DRAM Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
256K Units DRAM	947.3	797.2	590.9	275.4	185.0	125.0	81.0	45.0	20.0	1.0
DIP	729.4	590.7	437.3	198.3	126.7	81.9	49.4	21.6	7.1	0.0
ZIP	75.8	79.7	59.1	30.3	23.1	16.3	10.9	5.9	2.5	0.0
PLCC	113.7	102.8	76.8	38.6	26.8	19.4	13.0	10.8	6.0	0.9
Others	15.2	15.1	11.8	5.5	6.5	6.3	6.9	6.3	4.2	0.1
Die	13.3	8.8	5.9	2.8	1.9	1.3	0.8	0.5	0.2	0.0
SIP/SIMM	56.8	51.4	38.4	19.3	13.4	9.7	6.5	5.4	3.0	0.5
1M Units DRAM	211.6	493.5	706.7	833.7	660.0	370.0	200.0	115.0	85.0	21.0
DIP	88.7	177.2	169.6	125.1	62.0	29.2	6.4	0.0	0.0	0.0
ZIP	23.3	59.2	94.0	116.7	93.1	50.0	25.4	13.9	10.2	1.9
SOJ/SOP	95.2	246.8	424.0	566.9	481.8	277.5	160.0	95.9	70.6	17.6
Others	2.1	4.9	10.6	12.5	9.9	4.8	2.2	1.2	0.9	0.2
Die	2.3	5.4	8.5	12.5	13.2	8.5	6.0	4.0	3.4	1.3
SIP/SIMM	52.4	135.7	254.4	340.1	289.1	180.4	104.0	62.3	45.9	11.5
4M Units DRAM	0.0	1.9	31.4	155.0	412.0	805.0	945.0	775.0	525.0	50.0
DIP	0.0	0.7	4.4	2.8	4.1	0.0	0.0	0.0	0.0	0.0
ZIP	0.0	0.2	4.1	20.2	45.3	64.4	70.9	54.3	36.8	3.5
SOJ/SOP	0.0	1.0	22.0	124.0	342.0	703.6	831.6	682.0	459.4	42.8
Others	0.0	0.0	0.8	7.0	16.5	28.2	28.4	23.3	15.8	1.5
Die	0.0	0.0	0.2	1.1	4.1	8.9	14.2	15.5	13.1	2.2
SIP/SIMM	0.0	0.6	13.2	74.4	205.2	457.3	540.5	477.4	321.6	34.2

Table 2.6.1 (cont.)
Estimated Worldwide MOS DRAM Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
16M Units DRAM	0.0	0.0	0.0	0.3	5.0	35.0	165.0	475.0	750.0	600.0
DIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
ZIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
SOJ/SOP	0.0	0.0	0.0	0.2	4.0	27.5	120.5	344.4	502.5	360.0
Others	0.0	0.0	0.0	0.1	1.0	7.0	41.3	118.8	225.0	210.0
Die	0.0	0.0	0.0	0.0	0.1	0.5	3.3	11.9	22.5	30.0
SIP/SIMM	0.0	0.0	0.0	0.0	0.8	13.7	72.3	206.6	326.6	252.0
64M Units DRAM	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	3.0	425.0
DIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
ZIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
SOJ/SOP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	2.7	307.7
Others	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.3	106.3
Die	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	11.1
SIP/SIMM	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	21.0
256M Units DRAM	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	1.7	230.8
DIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	60.0
ZIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
SOJ/SOP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Others	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	36.6
Die	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	2.4
SIP/SIMM	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	25.4

Source: Dataquest, April, 1992

Table 2.6.2
Estimated Regional MOS DRAM Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Worldwide Total	1158.9	1292.6	1329.0	1264.4	1262.0	1335.0	1391.0	1410.0	1383.0	1157.0
Package Type	1158.9	1292.6	1329.0	1264.4	1262.0	1335.0	1391.0	1410.0	1383.0	1157.0
DIP	818.1	768.6	611.3	326.1	192.9	111.1	55.8	21.6	7.1	0.0
ZIP	99.1	139.1	157.2	167.2	161.5	130.6	107.2	74.0	49.5	5.4
PLCC	113.7	102.8	76.8	38.6	26.8	19.4	13.0	10.8	6.0	0.9
SOJ/SOP	95.2	247.8	446.0	691.2	827.7	1008.5	1112.1	1122.3	1035.1	764.7
Others	17.3	20.1	23.2	25.0	33.9	46.2	78.7	149.5	246.1	339.1
Die	15.6	14.2	14.5	16.3	19.2	19.1	24.3	31.9	39.3	46.9
SIP/SIMM	109.2	187.7	306.0	433.8	508.5	661.1	723.3	751.8	698.8	554.3
Japan	852.0	934.5	955.1	931.2	907.2	934.1	974.4	994.9	963.2	737.4
Package Type										
DIP	564.5	507.3	372.9	176.1	86.8	35.6	11.2	2.2	0.0	0.0
ZIP	99.1	139.1	157.2	167.2	161.5	130.6	107.2	74.0	49.5	5.4
PLCC	78.9	64.7	38.1	12.0	5.0	1.9	0.1	0.0	0.0	0.0
SOJ/SOP	83.5	196.0	356.8	542.8	611.9	717.9	778.1	782.2	694.0	457.6
Others	13.5	16.1	18.6	20.0	26.6	32.8	58.4	111.0	188.3	236.4
Die	12.5	11.4	11.6	13.1	15.4	15.3	19.4	25.5	31.4	38.0
SIP/SIMM	92.7	145.9	219.6	315.0	342.9	389.0	407.5	411.8	363.8	277.0
United States	196.0	216.1	227.5	209.8	205.7	218.5	222.7	230.4	239.3	231.2
Package Type										
DIP	163.6	146.0	122.3	68.5	44.4	27.8	15.1	6.5	2.5	0.0
ZIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
PLCC	16.3	21.0	25.5	18.6	16.9	14.0	9.9	9.8	6.0	0.9
SOJ/SOP	11.0	44.0	74.1	116.8	137.4	167.4	183.5	188.5	190.0	175.0
Others	3.5	3.6	4.2	4.3	5.1	7.4	11.8	22.4	36.9	50.9
Die	1.6	1.4	1.5	1.6	1.9	1.9	2.4	3.2	3.9	4.4
SIP/SIMM	9.1	29.6	45.0	55.0	82.5	124.6	139.8	148.0	144.0	121.0
Western Europe	38.7	56.6	59.8	47.7	53.2	59.9	57.6	59.9	65.8	54.7
Package Type										
DIP	32.7	46.1	48.9	32.6	23.1	17.8	10.6	5.4	2.1	0.0
ZIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
PLCC	5.5	7.1	5.5	4.0	1.9	1.5	1.0	1.0	0.0	0.0
SOJ/SOP	0.1	3.0	5.0	10.6	27.4	39.2	44.0	50.0	58.0	47.1
Others	0.1	0.1	0.1	0.2	0.4	1.0	1.5	2.9	4.9	6.8
Die	0.3	0.3	0.3	0.3	0.4	0.4	0.5	0.6	0.8	0.8
SIP/SIMM	2.0	5.0	10.3	15.0	18.0	22.0	31.0	37.0	41.0	27.6
Asia Pacific	72.3	85.4	86.6	75.7	95.9	122.5	136.4	124.9	114.7	133.7
Package Type										
DIP	57.3	69.2	67.2	48.9	38.6	30.0	19.0	7.6	2.5	0.0
ZIP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
PLCC	13.0	10.0	7.7	4.0	3.0	2.0	2.0	0.0	0.0	0.0
SOJ/SOP	0.6	4.8	10.1	21.0	51.0	84.0	106.5	101.6	93.1	85.0
Others	0.2	0.3	0.4	0.5	1.8	5.0	7.0	13.2	16.0	45.0
Die	1.2	1.1	1.2	1.3	1.5	1.5	1.9	2.5	3.1	3.7
SIP/SIMM	5.4	7.2	31.1	48.8	65.1	125.5	145.0	155.0	150.0	128.7

Source: Dataquest, April, 1992

Table 2.6.3
Estimated MOS DRAM Module Organization
Millions of Units

	1990	1991	1992	1993	1994	1995	1996	2000
256K SIP/SIMM DRAM Units	38.4	19.3	13.4	9.7	6.5	5.4	3.0	0.5
x8	8.4	4.0	2.7	1.7	1.0	0.8	0.5	0.1
x9	30.0	15.2	10.7	7.9	5.4	4.6	2.6	0.4
x32	0.0	0 0	0.0	0.0	0.0	0.0	0.0	0.0
x36	0.0	0 0	0.0	0.0	0.0	0.0	0.0	0.0
x40	0.0	0 0	0.0	0.0	0.0	0.0	0.0	0.0
1M SIP/SIMM DRAM Units	254.4	340.1	289.1	180.4	104.0	62.3	45.9	11.5
x8	109.4	139.5	109.9	63.1	31.2	18.7	13.8	3.4
x9	127.2	176.9	159.0	104.6	65.5	39.3	28.9	7.2
x32	2.5	3.4	2.9	1.8	1.0	0.6	0.5	0.1
x36	10.2	13.6	11.6	7.2	4.2	2.5	1.8	0.5
x40	5.1	6.8	5.8	3.6	2.1	1.2	0.9	0.2
4M SIP/SIMM DRAM Units	13.2	74.4	205.2	457.3	540.5	477.4	321.6	34.2
x8	2.1	11.9	30.8	68.6	81.1	71.6	48.2	5.1
x9	9.2	52.8	143.6	311.0	351.4	296.0	192.9	20.5
x32	0.1	0.7	2.1	4.6	5.4	4.8	3.2	0.3
x36	1.1	6.0	18.5	50.3	70.3	71.6	51.5	5.5
x40	0.7	3.0	10.3	22.9	32.4	33.4	25.7	2.7
16M SIP/SIMM DRAM Units	0.0	0.0	0.8	13.7	72.3	206.6	326.6	252.0
x8	0.0	0.0	0.3	5.5	28.2	78.5	117.6	90.7
x9	0.0	0.0	0.4	8.0	41.2	115.7	173.1	123.5
x32	0.0	0.0	0.0	0.0	0.7	2.1	3.3	2.5
x36	0.0	0.0	0.0	0.3	2.2	10.3	32.7	35.3
x40	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
64M SIP/SIMM DRAM Units	0.0	0.0	0.0	0.0	0.0	0.0	1.7	230.8
x8	0.0	0 0	0.0	0.0	0.0	0.0	0.5	76.2
x9	0.0	0 0	0.0	0.0	0.0	0.0	0.6	80.8
x32	0.0	0 0	0.0	0.0	0.0	0.0	0.0	4.6
x36	0.0	0 0	0.0	0.0	0.0	0.0	0.1	11.5
x40	0.0	0 0	0.0	0.0	0.0	0.0	0.4	57.7
256M SIP/SIMM DRAM Units	0.0	0.0	0.0	0.0	0.0	0.0	0.0	25.4
x8	0.0	0.0	0.0	0.0	0.0	0.0	0.0	7.6
x9	0.0	0.0	0.0	0.0	0.0	0.0	0.0	12.7
x32	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.8
x36	0.0	0.0	0.0	0.0	0.0	0.0	0.0	1.3
x40	0.0	0.0	0.0	0.0	0.0	0.0	0.0	3.0

Source: Dataquest, April, 1992

Table 2.6.4
MOS DRAM Emerging Package Technologies
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Worldwide Total										
SO	95.2	247.8	446.0	691.2	827.7	1008.5	1112.1	1122.3	1035.1	764.7
SOJ	95.2	247.8	437.1	622.0	662.2	706.0	667.2	448.9	414.0	229.4
TSOP			8.9	69.1	165.5	302.6	444.8	673.4	724.6	535.3
Others	17.3	20.1	23.2	25.0	33.9	46.2	78.7	149.5	246.1	339.1
LOC*			0.7	1.8	5.1	9.2	19.7	44.8	98.4	203.4
TAB			0.2	0.3	0.7	0.9	2.4	4.5	7.4	10.2
Stacked LOC			0.0	0.0	0.3	0.9	3.9	7.5	17.2	33.9
Die	15.6	14.2	14.5	16.3	19.2	19.1	24.3	31.9	39.3	46.9

*LOC = Lead on chip

Source: Dataquest, April, 1992

Table 2.6.5
Estimated Slow SRAM Packaging Forecast
(Millions of Units)

		1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
16K	DIP	107.5	102.9	53.8	47.7	20.8	9.3	5.9	2.1	0.6	0.0
	SOG/SOP	46.4	55.8	36.1	39.4	21.0	11.6	9.0	4.8	2.1	0.0
	Bare Die	0.8	0.8	0.5	0.4	0.2	0.1	0.2	0.1	0.0	0.0
	Total	154.7	159.5	90.4	87.6	42.0	21.0	15.0	7.0	3.0	0.0
64K	DIP	80.7	70.8	66.2	63.7	34.1	23.8	16.8	9.5	4.9	0.0
	SOG/SOP	82.3	88.6	121.0	127.4	74.8	60.4	51.8	39.5	29.4	0.0
	Bare Die	1.6	1.6	1.9	1.9	1.1	0.9	1.4	1.0	0.7	0.0
	Total	164.6	161.0	189.0	193.0	110.0	85.0	70.0	50.0	35.0	0.0
256K	DIP	33.8	42.2	55.8	57.4	50.4	32.0	12.8	1.8	0.0	0.0
	SOG/SOP	53.4	83.1	146.6	158.9	164.3	160.0	137.6	75.7	35.0	4.0
	Bare Die	1.8	2.6	4.1	4.4	4.4	8.0	9.6	10.6	15.0	20.0
	Total	89.0	127.9	206.5	220.7	219.0	200.0	160.0	88.0	50.0	26.0
1Mb	DIP	0.0	0.5	3.3	6.4	15.7	21.1	18.9	4.2	0.0	0.0
	SOG/SOP	0.1	1.4	12.7	27.9	78.4	146.1	174.3	172.6	149.4	60.0
	Bare Die	0.0	0.1	0.7	1.4	3.9	8.8	16.8	31.2	14.4	40.0
	Total	0.1	2.0	16.7	35.8	98.0	176.0	210.0	208.0	180.0	100.0
4Mb	DIP				0.0	0.0	0.1	0.4	0.0	0.0	0.0
	SOG/SOP				0.6	1.8	10.1	33.2	75.8	108.5	146.4
	Bare Die				0.1	0.2	1.8	8.4	25.3	46.5	97.6
	Total				0.7	2.1	12.0	42.0	101.0	155.0	244.0

Note: At the 1Mb and 4Mb densities the Pseudo-Static RAMs are not included

Source: Dataquest, May, 1992

Table 2.6.6
Estimated Fast SRAM Packaging Forecast
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
16K DIP	38.9	35.6	27.4	21.7	17.5	15.6	13.1	9.8	7.4	0.0
CLCC	6.6	5.5	3.8	2.8	2.0	1.7	1.3	1.0	0.7	0.0
Bare Die	2.7	2.7	2.3	2.0	1.7	1.7	1.6	1.2	0.9	0.0
Total	48.2	43.8	33.5	26.4	21.3	19.0	16.0	12.0	9.0	0.0
64K DIP	31.5	49.2	51.4	47.1	26.1	18.1	12.4	5.4	2.1	0.0
CLCC	3.7	3.3	2.2	3.1	2.1	1.5	1.2	0.8	0.4	0.0
SOJ	0.3	1.0	9.4	33.5	29.5	25.3	24.8	27.9	24.2	18.9
Bare Die	4.2	6.6	9.4	20.9	21.3	22.1	23.6	20.0	14.4	8.1
Total	39.8	60.1	72.4	104.7	79.0	67.0	62.0	54.0	41.0	27.0
256K DIP	2.0	6.8	10.4	16.2	25.9	24.8	24.2	19.8	12.3	0.0
SOJ	1.4	5.2	11.4	20.5	37.0	52.0	58.6	58.4	62.5	44.0
Bare Die	0.4	1.5	3.0	6.0	11.1	15.2	18.2	20.8	13.2	11.0
Total	3.7	13.5	24.9	42.7	74.0	92.0	101.0	99.0	88.0	55.0
1Mb DIP	0.0	0.0	0.8	1.9	4.8	11.8	14.1	13.6	9.4	0.0
SOJ	0.0	0.0	1.1	3.5	9.2	26.8	39.8	53.6	63.0	60.6
Bare Die	0.0	0.0	0.3	1.0	3.0	8.7	13.1	17.9	21.6	40.4
Total	0.0	0.1	2.2	6.5	17.0	47.3	67.0	85.0	94.0	101.0
4Mb DIP	0.0	0.0	0.0	0.0	0.0	0.1	0.3	0.8	1.3	0.0
SOJ	0.0	0.0	0.0	0.0	0.1	0.4	2.4	7.2	19.8	56.7
Bare Die	0.0	0.0	0.0	0.0	0.0	0.1	0.7	3.1	11.9	48.3
Total	0.0	0.0	0.0	0.0	0.1	0.5	3.4	11.0	33.0	105.0

Source: Dataquest, May, 1992

Table 2.6.7
Estimated Worldwide MOS SRAM Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Worldwide Total	500.1	567.9	635.5	718.0	662.5	719.8	746.4	715.0	671.5	656.0
Package Type										
DIP	182.2	228.9	316.4	354.2	340.3	388.1	405.9	368.4	38.0	0.0
SOG	182.2	228.9	316.4	354.4	340.3	388.1	405.9	368.4	324.4	210.4
SOJ	1.7	6.3	21.9	57.5	75.8	104.4	125.6	147.0	169.5	180.2
CLCC	10.3	8.8	6.0	5.9	4.2	3.1	2.5	1.7	1.1	0.0
Bare Die	11.4	15.8	22.1	38.2	47.0	67.4	93.5	131.0	138.6	265.4
Pin Count	500.1	567.9	635.5	718.0	662.5	719.8	746.4	715.0	671.5	656.0
20-pin	42.1	35.0	30.0	27.0	20.3	15.0	12.0	9	7.0	0.0
22-pin	70.0	96.1	92.0	81.0	64.0	35.0	30.0	26	22.0	9.0
24-pin	97.0	115.0	110.0	101.0	91.0	84.0	64.0	35	18.0	0.0
28-pin	279.6	305.0	369.4	439.8	372.2	370.0	368.9	326	287.9	144.6
32-pin	0.0	1.0	12.0	31.0	68.0	148.4	178.0	188	198.0	237.0
Bare Die	11.4	15.8	22.1	38.2	47.0	67.4	93.5	131.0	138.6	265.4
Japan	401.0	432.7	472.4	515.1	465.8	495.4	505.2	470.0	433.4	410.5
Package Type	401.0	432.7	472.4	515.1	465.8	495.4	505.2	470.0	433.4	410.5
DIP	223.6	211.6	170.1	160.5	128.0	113.8	84.9	46.4	24.4	0.0
SOG	171.6	211.7	276.9	290.6	262.8	288.8	299.8	265.2	237.3	159.3
SOJ	0.7	2.3	15.2	39.3	44.9	47.0	55.5	74.2	94.6	85.2
CLCC	0.1	0.1	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Other	5.0	7.0	10.2	24.9	30.1	45.7	65.0	84.2	77.2	166.0
United States	46.3	56.9	64.7	83.5	85.5	98.8	108.1	110.1	109.6	116.0
Package Type	46.3	56.9	64.7	83.5	85.5	98.8	108.1	110.1	109.6	116.0
DIP	22.7	26.3	23.7	21.0	10.0	9.0	7.0	3	1.4	0.0
SOG	9.0	14.0	23.0	32.9	35.5	25.0	20.0	18	16.0	10.0
SOJ	0.7	2.7	4.8	16.0	25.6	48.8	58.9	56	54.0	54.0
CLCC	9.0	7.0	4.8	4.8	3.3	2.2	1.7	1.3	0.8	0.0
Other	4.9	6.9	8.4	8.8	11.1	13.8	20.5	31.8	37.4	52.0
Western Europe	19.3	24.1	27.2	34.9	35.3	40.5	43.9	44.7	44.4	46.9
Package Type	19.3	24.1	27.2	34.9	35.3	40.5	43.9	44.7	44.4	46.9
DIP	14.8	16.5	16.1	14.8	10.0	9.0	7.0	3	1.5	0.0
SOG	1.5	3.0	5.4	13.2	14.6	15.8	19.4	18	13.8	9.0
SOJ	0.3	1.3	1.5	2.0	5.0	8.0	10.0	12.5	13.0	17.0
CLCC	1.2	1.5	1.0	0.9	0.7	0.7	0.5	0.2	0.1	0.0
Other	1.5	1.8	3.2	4.0	5.0	7.0	7.0	11.0	16.0	20.9
Asia Pacific	33.5	54.2	71.1	84.4	76.0	85.2	89.2	90.2	84.1	82.6
Package Type	33.5	54.2	71.1	84.4	76.0	85.2	89.2	90.2	84.1	82.6
DIP	33.4	53.6	59.1	65.9	47.3	25.0	20.0	14.5	10.7	0.0
SOG	0.1	0.3	11.1	17.5	27.4	58.5	66.7	67.2	57.3	32.1
SOJ	0.0	0.0	0.4	0.2	0.3	0.6	1.2	4.3	7.9	24.0
CLCC	0.0	0.2	0.2	0.2	0.2	0.2	0.3	0.2	0.2	0.0
Other	0.0	0.1	0.3	0.6	0.8	0.9	1.0	4	8.0	26.5

Source: Dataquest, May, 1992

Table 2.6.8
Estimated Worldwide MOS EPROM Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Worldwide Total	350.7	402.1	424.0	425.2	396.9	391.2	363.0	352.5	329.5	226.0
Total by Package Type	350.7	402.1	424.0	425.2	396.9	391.2	363.0	352.5	329.5	226.0
DIP	315.9	352.3	345.8	332.2	297.5	275.5	244.3	221.8	202.3	83.7
Chip Carrier	31.4	42.5	65.5	76.5	75.5	73.7	69.0	65.2	60.1	32.4
SO	3.5	7.2	11.4	12.8	18.2	31.0	32.6	41.0	37.9	30.6
TSOP	0.0	0.0	1.3	3.8	5.7	10.9	17.1	24.4	29.3	79.2
Total by Pin Count	350.7	402.1	424.0	425.2	396.9	391.2	363.0	352.5	329.5	226.0
24-pin	24.5	20.1	17.0	12.8	11.9	7.8	3.6	1.8	0.3	0.0
28-pin	305.8	357.9	379.0	378.9	351.2	346.2	321.2	310.2	291.3	200.0
32-pin	17.5	20.1	21.2	21.3	19.8	19.6	18.1	17.6	16.5	11.3
40-pin	1.8	2.0	2.5	3.8	4.0	7.8	10.9	14.1	13.2	9.0
44-pin	1.1	2.0	4.2	8.5	9.9	9.8	9.1	8.8	8.2	5.6
Japanese Total	115.0	120.6	127.2	127.6	116.7	113.4	101.6	102.2	95.6	65.5
Package Type	115.0	120.6	127.2	127.6	116.7	113.4	101.6	102.2	95.6	65.5
DIP	107.0	106.2	105.6	102.1	92.2	87.4	76.2	74.6	66.9	6.6
Chip Carrier	4.6	7.2	8.9	8.9	8.2	7.9	7.1	6.1	5.7	0.0
SO	3.5	7.2	11.4	12.8	11.7	11.3	11.2	11.2	10.5	7.2
TSOP	0.0	0.0	1.3	3.8	4.7	6.8	7.1	10.2	12.4	51.8
North American Total	180.3	217.1	227.7	225.4	210.4	205.4	199.7	183.3	168.0	106.2
Package Type	180.3	217.1	227.7	225.4	210.4	205.4	199.7	183.3	168.0	106.2
DIP	162.2	191.1	182.1	169.0	147.2	127.3	115.8	91.7	82.3	34.0
Chip Carrier	18.0	26.1	45.5	56.3	56.8	55.5	53.9	51.3	47.1	29.7
SO	0.0	0.0	0.0	0.0	5.3	18.5	20.0	27.5	25.2	22.3
TSOP	0.0	0.0	0.0	0.0	1.1	4.1	10.0	12.8	13.4	20.2
European Total	54.7	61.5	64.9	65.9	61.9	60.6	47.2	45.8	42.8	15.8
Package Type	54.7	61.5	64.9	65.9	61.9	60.6	47.2	45.8	42.8	15.8
DIP	46.0	52.3	53.8	54.7	50.2	49.1	37.8	34.4	30.0	4.7
Chip Carrier	8.8	9.2	11.0	11.2	10.5	10.3	8.0	7.8	7.3	2.7
SO	0.0	0.0	0.0	0.0	1.2	1.2	1.4	2.3	2.1	1.1
TSOP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	1.4	3.4	7.3
Asia/Pacific Total	0.7	2.8	4.2	6.4	7.9	11.7	14.5	21.2	23.1	38.4
Package Type	0.7	2.8	4.2	6.4	7.9	11.7	14.5	21.2	23.1	38.4
DIP	0.7	2.8	4.2	6.4	7.9	11.7	14.5	21.2	23.1	38.4
Chip Carrier	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
SO	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
TSOP	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0

Source: Dataquest, May, 1992

Table 2.6.9
Estimated Worldwide MOS ROM Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Worldwide	250.3	259.3	399.0	481.9	446.2	371.3	319.6	303.5	285.0	240.0
Package Type	248.9	259.3	399.0	481.9	446.2	371.3	319.6	303.5	285.0	240.0
DIP	167.0	138.1	128.4	97.3	54.6	26.5	11.5	5.8	2.5	0.2
SO	76.7	108.9	237.9	335.1	326.0	269.6	224.7	209.9	199.8	171.0
QUAD	0.0	0.2	0.3	0.4	0.4	0.3	0.3	0.2	0.2	0.2
Bare Die	6.6	12.1	32.5	49.0	65.2	74.9	83.1	87.6	82.5	68.6
Pin Count	250.3	259.3	399.0	481.9	446.2	371.3	319.6	303.5	285.0	240.0
24-pin	8.5	3.5	3.4	1.2	0.0	0.0	0.0	0.0	0.0	0.0
28-pin	225.3	227.9	330.4	382.6	325.9	241.6	168.7	143.7	125.6	89.9
32-pin	10.0	15.6	31.9	48.2	53.1	52.0	63.9	66.8	68.4	62.4
40-pin	0.0	0.3	0.4	0.5	1.3	1.9	2.9	3.0	5.7	12.0
44-pin	0.0	0.0	0.4	0.5	0.7	0.9	1.0	2.4	2.9	7.2
Bare Die	6.6	12.1	32.5	49.0	65.2	74.9	83.1	87.6	82.5	68.6
Japan	140.2	168.5	279.3	361.4	357.0	297.0	255.7	242.8	228.0	192.0
Package Type	140.2	168.5	279.3	361.4	357.0	297.0	255.7	242.8	228.0	192.0
DIP	70.1	67.4	55.9	36.1	17.8	3.0	0.0	0.0	0.0	0.0
SO	65.9	92.5	198.0	288.7	288.8	234.4	191.5	177.0	166.2	141.9
QUAD	0.0	0.2	0.3	0.4	0.4	0.3	0.3	0.2	0.2	0.2
Bare Die	4.2	8.4	25.1	36.1	50.0	59.4	63.9	65.6	61.6	49.9
United States	92.6	72.6	91.8	84.3	53.5	42.7	35.2	30.4	28.5	24.0
Package Type	92.6	72.6	91.8	84.3	53.5	42.7	35.2	30.4	28.5	24.0
DIP	83.3	58.1	55.1	42.2	21.4	12.8	5.3	1.8	0.9	0.0
SO	8.3	12.3	32.1	33.7	21.4	19.2	15.8	13.4	13.4	12.0
QUAD	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Bare Die	0.9	2.2	4.6	8.4	10.7	10.7	14.1	15.2	14.3	12.0
Europe	3.8	3.9	6.0	7.2	6.7	5.6	4.8	4.6	4.3	3.6
Package Type	3.8	3.9	6.0	7.2	6.7	5.6	4.8	4.6	4.3	3.6
DIP	2.6	2.6	3.8	4.6	4.0	2.9	1.9	1.4	0.4	0.0
SO	1.1	1.2	2.1	2.5	2.5	2.5	2.5	2.7	3.2	2.9
QUAD	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Bare Die	0.1	0.1	0.1	0.1	0.1	0.2	0.4	0.5	0.6	0.7
Asia Pacific	13.8	14.3	21.9	28.9	29.0	26.0	24.0	25.8	24.2	20.4
Package Type	13.8	14.3	21.9	28.9	29.0	26.0	24.0	25.8	24.2	20.4
DIP	11.0	10.0	13.6	14.5	11.3	7.8	4.3	2.6	1.2	0.2
SO	1.4	2.9	5.7	10.1	13.3	13.6	14.9	16.8	17.0	14.3
QUAD	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Bare Die	1.4	1.4	2.6	4.3	4.4	4.7	4.8	6.4	6.0	5.9

Source: Dataquest, May, 1992

Table 2.6.10
Estimated Worldwide MOS EEPROM Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Worldwide	100.5	118.3	143.0	184.0	188.6	169.1	167.6	170.6	174.1	160.0
Package Type	100.5	118.3	143.0	184.0	188.6	169.1	167.6	170.6	174.1	160.0
DIP	90.5	91.6	91.5	88.3	75.4	50.7	33.5	18.8	8.7	1.6
Chip Carrier	6.0	16.1	24.9	42.3	45.1	38.9	37.7	35.8	33.1	28.8
SO	3.8	9.8	23.6	44.0	49.0	55.6	67.0	80.0	87.1	87.8
PGA	0.1	0.1	0.1	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Bare Die	0.1	0.6	2.9	9.2	18.9	23.7	29.2	35.8	45.1	41.6
Pin Count	100.5	118.3	143.0	184.0	188.6	169.1	167.6	170.6	174.1	160.0
8-pin	65.9	64.0	61.0	61.0	56.6	51.0	49.0	49.0	47.0	35.0
14-pin	5.0	7.5	11.0	19.0	21.0	14.0	13.2	12.5	12.0	4.3
24-pin	5.5	11.1	20.5	31.0	32.0	28.0	26.0	26.0	24.0	16.0
28-pin	14.0	24.0	35.0	46.0	44.0	35.0	32.0	29.0	28.1	21.7
32-pin	10.0	11.0	14.0	22.0	27.0	30.1	31.4	32.0	33.0	28.0
Bare Die	0.1	0.7	1.5	5.0	8.0	11.0	16.0	22.1	30.0	55.0
United States	58.3	69.5	82.3	102.5	103.4	87.2	83.0	81.9	86.3	94.4
Package Type	58.3	69.5	82.3	102.5	103.4	87.2	83.0	81.9	86.3	94.4
IP	51.9	52.6	53.4	53.0	48.1	32.1	23.5	13.2	6.0	1.6
Chip Carrier	5.4	14.5	22.7	38.7	40.5	34.9	33.3	31.5	29.1	25.5
SO	0.8	2.0	5.4	8.0	10.4	14.0	18.0	24.0	30.0	47.1
PGA	0.1	0.1	0.1	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Bare Die	0.1	0.3	0.7	2.6	4.2	6.0	8.0	13.0	21.0	20.0
Japan	37.2	42.6	53.4	72.1	75.6	73.2	74.5	76.6	75.6	57.6
Package Type	37.2	42.6	53.4	72.1	75.6	73.2	74.5	76.6	75.6	57.6
DIP	34.2	34.5	33.3	30.0	23.0	15.0	7.0	3.0	0.5	0.0
Chip Carrier	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
SO	3.0	7.8	17.9	35.6	38.0	40.7	46.9	51.7	51.8	37.0
PGA	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Bare Die	0.0	0.3	2.2	6.5	14.6	17.5	20.6	21.9	23.3	20.6
Western Europe	4.9	5.9	7.0	9.2	9.4	8.5	8.4	10.2	10.4	6.4
Package Type	4.9	5.9	7.0	9.2	9.4	8.5	8.4	10.2	10.4	6.4
DIP	4.3	4.3	4.5	5.2	4.2	3.5	2.9	2.6	2.2	0.0
Chip Carrier	0.6	1.6	2.2	3.5	4.5	3.9	3.8	3.6	3.3	2.9
SO	0.0	0.0	0.3	0.4	0.6	0.9	1.4	3.5	4.5	3.0
PGA	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Bare Die	0.0	0.0	0.0	0.1	0.1	0.2	0.3	0.5	0.4	0.5
Asia Pacific	0.1	0.2	0.2	0.2	0.2	0.2	1.7	1.9	1.9	1.6
Package Type	0.1	0.2	0.2	0.2	0.2	0.2	1.7	1.9	1.9	1.6
DIP	0.1	0.2	0.2	0.1	0.1	0.1	0.1	0.0	0.0	0.0
Chip Carrier	0.0	0.0	0.0	0.1	0.1	0.1	0.6	0.7	0.7	0.4
SO	0.0	0.0	0.0	0.0	0.0	0.0	0.7	0.8	0.8	0.7
PGA	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Bare Die	0.0	0.0	0.0	0.0	0.0	0.0	0.3	0.4	0.4	0.5

Source: Dataquest, May, 1992

Table 2.7.1
Estimated Regional Analog Market Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Worldwide										
Mixed-Signal	1490	1780	2100	2450	2900	3400	4000	4580	5170	8400
Linear	9010	9660	10930	12050	13600	15700	17700	18920	19487	17800
Total	10500	11440	13030	14500	16500	19100	21700	23500	24657	26200
Plastic DIP	5849	5582	5049	4272	3447	2773	2476	1887	1528	838
Ceramic DIP	260	198	123	65	46	26	14	5	0	0
QUAD	242	342	552	807	1151	1556	1937	2227	2524	3055
Plastic Chip Carrier	265	291	315	324	347	377	355	272	195	7
Ceramic Chip Carrier	40	37	23	9	4	0	0	0	0	0
SO	3126	4119	5637	7161	9055	11259	13232	14686	15721	16963
Other	354	388	524	609	669	788	806	753	689	260
Bare Die	364	483	807	1253	1783	2322	2880	3670	3999	5078
North America										
Mixed Signal	580	670	760	865	998	1155	1355	1560	1740	2680
Linear	1838	1961	2202	2325	2700	3100	3294	3595	3664	3204
Total	2418	2631	2962	3190	3698	4255	4649	5155	5404	5890
Plastic DIP	1572	1434	1185	1021	1017	1021	1000	1005	1000	825
Ceramic DIP	133	105	59	32	30	21	14	5	0	0
QUAD	12	26	89	128	185	255	325	412	540	942
Plastic Chip Carrier	48	66	77	64	55	51	46	26	16	0
Ceramic Chip Carrier	24	26	15	6	4	0	0	0	0	0
SO	484	789	1271	1557	1853	2183	2380	2624	2659	2533
Other	48	53	59	64	74	85	93	103	108	118
Bare Die	97	132	207	319	481	638	790	979	1081	1473
Total	2418	2631	2962	3190	3698	4255	4649	5155	5404	5890
Japan										
Mixed Signal	298	370	453	570	714	835	965	1060	1220	1920
Linear	3441	3622	3993	4487	4724	5289	5901	6181	6236	5319
Total	3739	3992	4446	5057	5438	6124	6866	7241	7456	7239
Plastic DIP	1671	1557	1334	1011	544	306	69	0	0	0
Ceramic DIP	4	4	0	0	0	0	0	0	0	0
QUAD	187	240	311	455	598	735	893	941	969	869
Plastic Chip Carrier	75	40	22	20	5	0	0	0	0	0
Ceramic Chip Carrier	4	0	0	0	0	0	0	0	0	0
SO	1499	1796	2223	2837	3317	3938	4532	4844	4988	4989
Other	75	80	133	177	196	227	247	253	246	109
Bare Die	224	275	422	556	778	919	1126	1202	1253	1267
Total	3739	3992	4446	5057	5438	6124	6866	7241	7456	7233

Table 2.7.1 (cont.)
Estimated Regional Analog Market Package Production
(Millions of Units)

	1988	1989	1990	1991	1992	1993	1994	1995	1996	2000
Europe										
Mixed Signal	408	490	570	640	710	820	945	1100	1244	2100
Linear	2109	2300	2678	3000	3420	3591	4000	4300	4424	4400
Total	2517	2790	3248	3640	4130	4411	4945	5400	5668	6500
Plastic DIP	1510	1476	1462	1456	1239	1015	989	540	283	7
Ceramic DIP	50	28	16	7	0	0	0	0	0	0
QUAD	25	56	97	146	207	221	247	302	340	455
Plastic Chip Carrier	50	84	97	109	124	110	99	76	57	7
Ceramic Chip Carrier	3	3	3	0	0	0	0	0	0	0
SO	778	1004	1312	1529	2106	2492	2967	3510	3968	4745
Other	76	84	130	146	124	110	99	54	28	1
Bare Die	25	56	130	248	330	463	544	918	992	1286
Total	2517	2790	3248	3640	4130	4411	4945	5400	5668	6500
Asia/Pacific										
Mixed Signal	204	250	317	375	478	590	735	860	966	1700
Linear	1622	1777	2057	2238	2756	3720	4505	4844	5164	4877
Total	1826	2027	2374	2613	3234	4310	5240	5704	6130	6577
Plastic DIP	1096	1115	1068	784	647	431	419	342	245	7
Ceramic DIP	73	61	47	26	16	4	0	0	0	0
QUAD	18	20	55	78	162	345	472	570	674	789
Plastic Chip Carrier	91	101	119	131	162	216	210	171	123	0
Ceramic Chip Carrier	9	8	5	3	0	0	0	0	0	0
SO	365	529	831	1239	1779	2646	3354	3708	4107	4696
Other	155	172	202	222	275	366	367	342	307	33
Bare Die	18	20	47	131	194	302	419	570	674	1052
Total	1826	2027	2374	2613	3234	4310	5240	5704	6130	6577

Source: Dataquest, May, 1992

Chapter 3 — MCM Applications

Introduction

The electronic equipment forecast shown in Table 3.1.1 provides detailed information on the total worldwide production, both captive and merchant, of electronic equipment by region and by application from 1990 through 1996, with a projected forecast out to 2000. This overview presents a condensed version of the six application segments covered by Dataquest's Worldwide Application Services. Electronic equipment revenue is assigned to the region in which the equipment is manufactured. The major equipment and application categories are defined in Appendix B.

Regional Overview

In reviewing the worldwide market demand for MCM technology, Dataquest has concluded that electronic equipment companies will most likely favor the MCM manufacturers that have established themselves as volume producers, whether they are captive or merchant. Thus suppliers of MCMs will have to be successful in the largest MCM markets which will be computer, communications, and consumer, as shown on Figure 3.2.1.

The major assumptions behind this forecast and that of each region to substantiate Dataquest's conclusions are as follows:

Dataprocessing

- Dataprocessing will continue to consume the largest share of MCM technology. MCM technology is key to further advances in dataprocessing clock rates.
- The conversion to MCM will be greater in the high performance equipment segments that are not cost driven.
- The dataprocessing market will offer the captive suppliers of MCM technology, their greatest opportunity to enter as a merchant supplier.

Communications

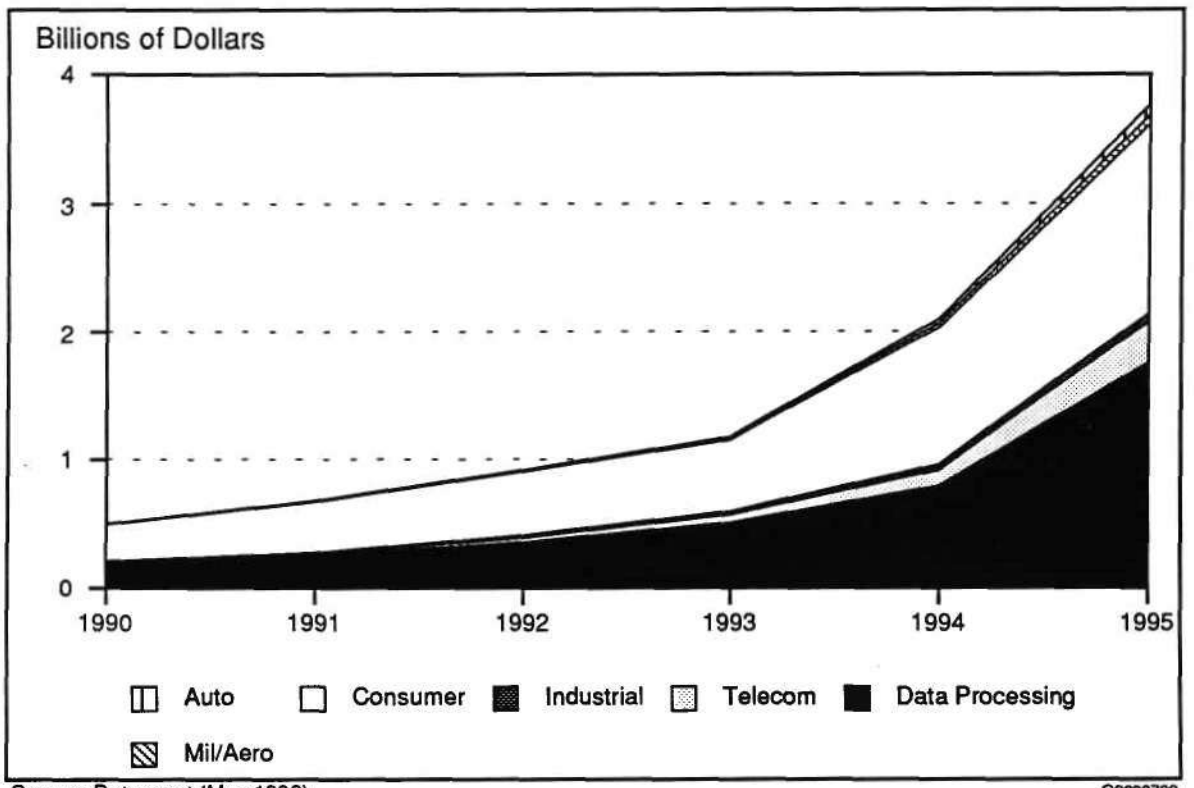
- Few products containing MCMs are now in the communications sector.
- Most telecommunication segments are cost and size driven and not performance driven.
- MCMs will penetrate the modem market at 9600bps and above.
- MCMs will make small inroads to the PBX and call accounting segments in the 1995 through 2000 time frame.
- The highest growth rates for MCM in the communications segments will commence after 1995.

Table 3.1.1
Electronic Equipment Production Forecast
(Factory Revenue in Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000	CAGR 90-95
North America								
Dataprocessing	83028	84112	87654	92167	96089	99749	136665	6.5%
Communications	30188	32520	35408	37972	40184	42614	60048	7.1%
Industrial	33690	35233	37834	40704	43254	46062	63109	6.5%
Consumer	17005	17396	18370	19236	20145	20974	25888	4.3%
Military	60569	56476	59934	62275	64419	67195	74553	2.1%
Transportation	4115	4024	4535	4996	5424	5721	7949	6.8%
Total	228595	229761	243735	257350	269515	282315	368212	5.3%
Japan								
Dataprocessing	46625	54197	59485	64817	68021	72913	114259	9.4%
Communications	20826	24070	25952	27894	29186	31232	46746	8.4%
Industrial	22507	25459	27954	30351	32076	34235	52193	8.8%
Consumer	54007	60202	63854	64249	64824	66736	82372	4.3%
Military	1356	1468	1616	1785	1971	2169	3462	9.8%
Transportation	5596	5900	6407	6768	7061	7429	9848	5.8%
Total	150917	171296	185268	195864	203139	214714	308881	7.3%
Europe								
Dataprocessing	28151	32959	38167	43055	48029	54182	104323	14.0%
Communications	34515	38074	41587	45366	48607	53490	83059	9.2%
Industrial	33920	36282	38874	41717	44125	47184	65562	6.8%
Consumer	37282	40341	43661	47327	51707	57355	88248	9.0%
Military	22112	21847	22327	22863	23549	24350	26753	1.9%
Transportation	4061	4747	5523	6670	8219	9551	22506	18.7%
Total	160041	174250	190139	206998	224236	246112	390450	9.0%
Asia/Pacific								
Dataprocessing	27356	31934	36428	41155	46424	52122	99479	13.8%
Communications	10455	11813	13535	15371	17111	19417	36092	13.2%
Industrial	2920	3369	3855	4313	4800	5236	9394	12.4%
Consumer	27773	29992	35413	39349	43196	47649	81748	11.4%
Military	3583	3907	4318	5000	5507	5989	10001	10.8%
Transportation	1852	2124	2451	2856	3296	3780	7703	15.3%
Total	73939	83139	96000	108044	120334	134193	244417	12.7%
Worldwide								
Dataprocessing	185160	203202	221734	241194	258563	278966	454726	9.6%
Communications	95984	106477	116482	126603	135088	146753	225945	8.9%
Industrial	93037	100343	108517	117085	124255	132717	190258	7.4%
Consumer	136067	147931	161298	170161	179872	192714	278257	7.2%
Military	87620	83698	88195	91923	95446	99703	114769	2.6%
Transportation	15624	16795	18916	21290	24000	26481	48006	11.1%
Grand Total	613492	658446	715142	768256	817224	877334	1311961	7.8%

Source: Dataquest, May, 1992

Figure 3.2.1
Worldwide MCM Revenue by Application
(Millions of Dollars)



Source: Dataquest (May 1992)

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Industrial

- Industrial consumption of MCM technology is expected to be slightly half that of the communications market since it is typically a slow growth market and served by many small companies. Revenue from MCMs will be small and competition will be fierce.

Consumer

- Consumer penetration of MCM technology is expected to be the second largest market behind dataprocessing.
- The MCM-L technology and other COB configurations will represent the largest MCM technology used in the consumer segment. Since COB and MCM-L capacity has already been put in place for production in 1992, in Japan, it is assumed that Japan will maintain control of this market.

Military/Aerospace

- The military/aerospace market caters to the most expensive MCM technology. Since its demand is custom and not based on volume, consumption of MCM technology will not be extensive.
- Commercial aerospace applications are performance sensitive, but the design cycles of new technology do not indicate a near future acceptance of MCM technology in volumes.
- In the wake of economic spending cuts, the U.S. military/commercial aerospace R&D base is shrinking, while Europe's financially subsidized military/commercial aerospace Airbus Industrie consortia continues to expand. European companies that have designed MCM-C and MCM-D technologies for their advanced military programs, are transfering their technology into the commercial application side, posing definite threats to U.S. companies such as Boeing, McDonnell Douglas, and Hughes, that are in a continuous stage of downsizing.

Transportation

- TH is currently the dominant technology in automotive applications. MCM technology is under very close scrutiny in automotive R&D houses, in Europe, Japan and the United States, but there is no detectable use of any form in automotive applications.
- Automotive represents the largest consumer of hybrid interconnect. Most of the hybrid applications are analog and have low interconnect density.
- Interest in low temperature cofired ceramic (LTCC) modules is due to the ability of this technology to fabricate passive components between interconnect layers.
- The passenger compartment area will offer the largest opportunity for multilayer ceramic MCM's and COB configurations. A very small portion of the passenger compartment functions will migrate to under the hood as ceramic MCMs become less expensive.

Regionally, North America remains the largest and most influential electronic equipment market for consumption of electronic devices. Since the level of MCM-C and MCM-D is expected to maintain a higher level of usage and represent a higher level of revenue in the North American region than MCM-L, the level of detail for MCM penetration will be analyzed to a greater extent than for Japan, Europe, and Asia/Pacific.

Tables 3.2.1 through 3.2.6 reflect the value of the equipment in each segment in North America which are expected to contain one or more high density modules. Table 3.2.7 is the roll-up of these tables.

Table 3.2.8 lists the value of semiconductors used in MCM's in the equipment segment for this region. By multiplying an estimated ratio of MCM value to semiconductor value in each system Dataquest has arrived at a total estimated value for MCM revenue in North America in Table 3.2.9.

Tables 3.2.10 through 3.2.21 provide the collective value of electronic equipment using MCM, the value of semiconductors used in MCM for each equipment segment, as well as the total MCM revenue by equipment segment for Japan, Europe and Asia/Pacific regions.

Table 3.2.1
Computers and Data Storage
North America Electronics Equipment Using MCM
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Dataprocessing							
Supercomputers	185	225	267	342	459	590	1890
Mainframe	1239	1253	1332	1320	1692	2738	8190
Midrange	608	1102	1616	2145	3045	4477	10517
Workstation	91	172	344	859	1871	3082	11929
Personal Computer	8	34	81	182	439	924	2299
Computers	2131	2786	3639	4848	7506	11810	44824
Rigid Disk Drives	9	32	63	133	281	688	3960
Optical Drives	0	1	1	4	11	24	133
Tape Drives	0	0	0	0	0	0	0
Flexible Drives	0	0	0	0	0	1	14
Data Storage/Subsystems	9	33	64	137	292	714	4107
Graphics Terminals	25	57	132	278	487	779	3596
Printers	13	44	83	205	429	925	10551
Copiers and Duplicators	0	3	5	10	23	68	745
Other Dedicated Systems	0	3	10	18	42	126	1403
Terminals/Dedicated Systems	38	107	230	511	981	1898	16296

Source: Dataquest, May, 1992

Table 3.2.2
Communications
North America Electronics Equipment Using MCM
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Communications							
Image & Text Equipment	0	1	1	3	6	14	200
Data Communication Equipment	9	19	33	83	110	383	6884
Premise Switching Equipment	0	3	6	9	21	41	605
Call Processing Equipment	2	5	9	17	46	104	2069
Desktop Terminal	0	0	0	0	0	0	0
Transmission Equipment	5	5	23	32	98	227	4671
Central Office	0	2	5	8	16	37	603
Mobile Communications	3	6	9	17	49	124	2173
Broadcast & Studio Telecom	0	0	0	0	0	0	0
Other Telecom	0	0	0	0	0	0	0
Communications	19	41	86	168	346	930	17204

Source: Dataquest, May, 1992

Table 3.2.3
Industrial
North America Electronics Equipment Using MCM
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Industrial							
Manufacturing Systems	0	16	17	55	97	143	4986
Instrumentation	8	9	19	30	53	79	3840
Diagnostics	0	0	4	9	15	38	863
Therapeut	0	0	0	0	0	0	0
Other	0	4	8	13	19	35	807
Total	8	28	48	107	184	295	10495

Source: Dataquest, May, 1992

Table 3.2.4
Consumer
North America Electronics Equipment Using MCM
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Consumer							
Audio	1	1	3	4	5	7	86
Video	3	10	18	26	39	60	611
Personal Electronics	0	1	2	3	4	6	97
Appliances	0	0	0	0	0	0	0
Other Consumer	0	0	0	0	0	0	0
Total	5	13	23	33	48	73	794

Source: Dataquest, May, 1992

Table 3.2.5
Military/Aerospace
North America Electronics Equipment Using MCM
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Military/Aerospace							
Military	15	37	96	244	491	999	11227
Civilian	9	11	24	41	123	259	3525
Total	25	47	120	284	614	1258	14752

Source: Dataquest, May, 1992

Table 3.2.6
Transportation
North America Electronics Equipment Using MCM
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Transportation							
Entertainment	0	0	0	0	1	2	69
Vehicle Controls	0	0	0	0	1	1	150
Body Controls	0	0	0	0	0	0	13
Driver Information	0	0	0	8	25	60	233
Powertrain	0	0	0	2	4	11	613
Safety & Convenience	0	0	0	0	0	0	0
Total	0	0	0	10	31	74	1078

Source: Dataquest, May, 1992

Table 3.2.7
North America-Electronics Equipment Using MCM
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
North America							
Dataprocessing	2178	2926	3933	5496	8779	14422	65226
Communications	19	41	86	168	346	930	17204
Industrial	8	28	48	107	184	295	10495
Consumer	5	13	23	33	48	73	794
Military	25	47	120	284	614	1258	14752
Transportation	0	0	0	10	31	74	1078
Total	2234	3055	4210	6099	10001	17052	109550

Source: Dataquest, May, 1992

Table 3.2.8
North America-Value of Semiconductors Used in MCMs
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
North America							
Dataprocessing	33	50	79	126	219	433	5218
Communications	0	1	2	5	11	28	516
Industrial	0	1	1	3	6	9	315
Consumer	0	0	1	1	2	2	40
Military	0	1	2	7	15	33	708
Transportation	0	0	0	0	1	2	52
Total	34	53	85	143	254	507	6849

Source: Dataquest, May, 1992

Table 3.2.9
Estimated MCM Revenue in North America
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
North America							
Dataprocessing	145	178	236	307	452	865	8192
Communications	2	4	7	13	23	56	810
Industrial	1	2	4	8	12	18	494
Consumer	0	1	2	2	3	5	62
Military	2	3	7	16	32	65	1112
Transportation	0	0	0	1	2	4	81
Total	149	187	256	347	523	1014	10752

Source: Dataquest, May, 1992

Table 3.2.10
Japan Electronics Equipment Production
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Dataprocessing	46625	54197	59485	64817	68021	72913	114259
Supercomputers	211	252	315	370	445	527	877
Mainframe	6061	6164	6321	6237	6153	6027	5000
Midrange	5387	5814	6300	6825	7056	7287	8900
Workstation	809	1041	1528	2297	3171	3676	5400
Personal Computer	9972	9012	9031	9165	9198	10374	15466
Computers	22440	22283	23495	24894	26023	27891	35643
Other Dataprocessing	24185	31914	35990	39923	41998	45022	78616
Communications	20826	24070	25952	27894	29186	31232	46746
Industrial	22507	25459	27954	30351	32076	34235	52193
Consumer	54007	60202	63854	64249	64824	66736	82372
Military	1356	1468	1616	1785	1971	2169	3462
Transportation	5596	5900	6407	6768	7061	7429	9848
Total	150917	171296	185268	195864	203139	214714	308881

Source: Dataquest, May, 1992

Table 3.2.11
Japan Electronics Equipment Using MCM
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Supercomputers	22	28	37	45	80	132	526
Mainframe	315	327	348	349	677	1145	3000
Midrange	119	233	441	819	1200	1858	5518
Workstation	16	31	76	230	539	956	3510
Personal Computer	10	18	45	183	368	830	7733
Other Dataprocessing	24	32	108	200	462	945	20440
Total Dataprocessing	506	668	1055	1826	3325	5866	40727
Communications	21	48	130	251	584	1562	18698
Industrial	11	51	84	121	257	342	11483
Consumer	4321	6020	8940	10280	12965	14682	32949
Military/Aerospace	1	3	5	9	16	22	415
Transportation	6	24	51	68	282	446	3250
Total	4866	6814	10264	12555	17429	22920	107523

Source: Dataquest, May, 1992

Table 3.2.12
Japan Semiconductors Used in MCMs
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Dataprocessing	9	13	27	55	100	264	3055
Communications	0	1	3	8	19	53	748
Industrial	0	1	2	4	8	10	344
Consumer	60	90	134	175	389	514	1812
Military	0	0	0	0	0	1	12
Transportation	0	0	1	2	7	18	162
Total	70	106	168	243	523	860	6134

Source: Dataquest, May, 1992

Table 3.2.13
MCM Revenue in Japan
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Dataprocessing	40	48	82	133	206	528	4796
Communications	2	4	10	19	38	106	1174
Industrial	1	4	7	9	17	21	541
Consumer	268	322	402	425	801	1028	2845
Military	0	0	0	0	1	1	20
Transportation	0	1	3	4	15	36	255
Total	312	380	504	590	1077	1719	9631

Source: Dataquest, May, 1992

Table 3.2.14
Europe Electronics Equipment Production
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Dataprocessing	28151	32959	38167	43055	48029	54182	104323
Supercomputers	123	136	158	197	250	279	600
Mainframe	5152	5283	6020	6534	7032	7462	11200
Midrange	5985	6426	7245	7800	8736	9716	16000
Workstation	1251	1562	1964	2757	3568	3893	7800
Personal Computer	11468	10364	10386	10998	11497	12350	21000
Computers	23979	23771	25773	28286	31083	33700	56600
Other Dataprocessing	4172	9188	12394	14769	16946	20482	47723
Communications	34515	38074	41587	45366	48607	53490	83059
Industrial	33920	36282	38874	41717	44125	47184	65562
Consumer	37282	40341	43661	47327	51707	57355	88248
Military	22112	21847	22327	22863	23549	24350	26753
Transportation	4061	4747	5523	6670	8219	9551	22506
Total	160041	174250	190139	206998	224236	246112	390450

Source: Dataquest, May, 1992

Table 3.2.15
Europe Electronics Equipment Using MCM
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Supercomputers	13	15	18	24	45	70	360
Mainframe	268	280	331	366	774	1418	6720
Midrange	132	257	507	936	1485	2478	9920
Workstation	25	47	98	276	607	1012	5070
Personal Computer	11	21	52	220	460	988	10500
Other Dataprocessing	4	9	37	74	186	430	12408
Total Dataprocessing	453	629	1044	1895	3556	6395	44978
Communications	35	76	208	408	972	2675	33224
Industrial	17	68	117	167	353	472	14424
Consumer	2983	4034	6113	7572	10341	12618	35299
Military/Aerospace	22	44	67	114	188	244	3210
Transportation	4	19	44	67	329	573	7427
Total	3513	4870	7592	10224	15740	22976	138562

Source: Dataquest, May, 1992

Table 3.2.16
Europe Semiconductors Used in MCMs
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Dataprocessing	4	6	13	25	50	128	1349
Communications	1	2	5	11	29	80	997
Industrial	0	2	3	4	8	11	346
Consumer	3	20	31	45	93	139	882
Military	0	0	1	1	3	4	80
Transportation	0	0	1	1	8	19	356
Total	8	31	53	88	191	381	4011

Source: Dataquest, May, 1992

Table 3.2.17
MCM Revenue in Europe
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Dataprocessing	16	22	38	60	103	256	2118
Communications	3	7	16	28	60	160	1565
Industrial	2	6	8	10	17	23	543
Consumer	13	72	92	110	192	278	1385
Military	1	2	2	3	6	8	126
Transportation	0	1	3	3	16	38	560
Total	35	110	158	214	393	763	6298

Source: Dataquest, May, 1992

Table 3.2.18
Asia/Pacific Electronics Equipment Production
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Dataprocessing	27356	31934	36428	41155	46424	52122	99479
Supercomputers	0	0	0	0	0	0	0
Mainframe	0	0	0	0	0	0	0
Midrange	0	0	0	0	0	0	0
Workstation	294	347	546	919	1387	1946	3500
Personal Computer	16453	14419	13999	14206	14257	15314	20000
Computers	16747	14766	14545	15125	15644	17260	23500
Other Dataprocessing	10609	17168	21883	26030	30780	34862	75979
Communications	10455	11813	13535	15371	17111	19417	36092
Industrial	2920	3369	3855	4313	4800	5236	9394
Consumer	27773	29992	35413	39349	43196	47649	81748
Military	3583	3907	4318	5000	5507	5989	10001
Transportation	1852	2124	2451	2856	3296	3780	7703
Total	73939	83139	96000	108044	120334	134193	244417

Source: Dataquest, May, 1992

Table 3.2.19
Asia/Pacific Electronics Equipment Using MCM
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Supercomputers	0	0	0	0	0	0	0
Mainframe	0	0	0	0	0	0	0
Midrange	0	0	0	0	0	0	0
Workstation	6	10	27	92	236	506	2275
Personal Computer	16	29	70	284	570	1225	10000
Other Dataprocessing	11	17	66	130	339	732	19755
Total Dataprocessing	33	56	163	506	1145	2463	32030
Communications	10	24	68	138	342	971	14437
Industrial	1	6	12	17	38	52	2067
Consumer	2222	2999	4958	6296	8639	10483	32699
Military/Aerospace	4	8	13	25	44	60	1200
Transportation	2	8	20	29	132	227	2542
Total	2272	3101	5233	7011	10340	14256	84975

Source: Dataquest, May, 1992

Table 3.2.20
Asia/Pacific Semiconductors Used in MCMs
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Dataprocessing	0	0	1	3	16	49	961
Communications	0	0	0	0	0	1	14
Industrial	0	0	0	0	0	0	0
Consumer	0	0	0	6	35	84	817
Military	0	0	0	0	0	0	0
Transportation	0	0	0	0	0	0	3
Total	0	0	1	9	51	134	1795

Source: Dataquest, May, 1992

Table 3.2.21
MCM Revenue in Asia/Pacific
(Millions of Dollars)

	1990	1991	1992	1993	1994	1995	2000
Dataprocessing	0	0	2	7	33	99	1509
Communications	0	0	0	0	1	2	23
Industrial	0	0	0	0	0	0	0
Consumer	1	1	1	15	71	168	1283
Military	0	0	0	0	0	0	0
Transportation	0	0	0	0	0	0	4
Total	1	1	4	23	105	269	2819

Source: Dataquest, May, 1992

Table 3.3.1
MCM Design Technology

Substrates	Width Min./Max.	Space Min./Max.	Via Pitch	Layers in Cost $/sq.inch <4	4-6	7-8	10-14	28
Ceramic	100µm-150µm	75µm-125µm				$7-10	$7-50	$30-40
Laminate	75µm-100µm	75µm-100µm	300µm	$.50	$1-2	$3-4	$4-7	---
Thin Film	20µm-50µm	25µm-75µm	10µm-200µm	$10-50	$20-100	---	$50-200	---

Source: Dataquest, May, 1992

Technology Design Tradeoffs

The data listed in Table 3.3.1 is a tabulation of the data provided by companies participating in the MCM survey conducted by Dataquest during 1991 and 1992 to evaluate the level of activity in the MCM market. The data was provided by companies both merchant and captive that are currently supplying substrates and finished modules to both merchant and captive end use markets.

In summary, Dataquest has concluded that the entry level to MCM production in volume will be at a higher cost than any interconnect technology available at this time. Because of this higher entry cost, the first firms that are able to produce the most cost efficient module in volume will have the greatest chance to become dominant in the market. The real issue for any MCM producer will be its ability to control the market situation early in implementation of its technology.

Chapter 4—MCM Issues

4.0 MCM Issues

This chapter discusses MCM design software, chip procurement, the MCM vendor community, consortium activities, the need for standards, and the tradeoff between "superchips" and MCM's.

MCM design software is needed that will make it possible to design the entire module using current top-down design methodologies. This need is described in some detail in the software section of this chapter.

Chip procurement is an issue that is closely linked to test and repairability. Test is discussed in some length in Chapter 7, and the conclusion is that the most economically efficient place to test and burn in chips is before they are assembled into a module. This means that the MCM market will require chips that are tested to the same quality levels as today's packaged units. The lack of such units is currently a market impediment.

Semiconductor manufacturers fear loss of value added if they supply bare chips rather than packaged units. Dataquest believes that chip value will be considerably enhanced when chips are thoroughly tested and that this will mitigate the loss of added value.

The structure of the current MCM vendor community is examined and some ideas about the structure of the future MCM vendor community are presented. Dataquest believes that it has already proven difficult for a vendor to survive as a substrate supplier. Vendors in the cofired ceramic part of the market seem to survive as module assemblers with most of the design being done by their customers. Interestingly, there seems to be a trend in the MCM-L and MCM-D segments of the market towards MCM's that are really application specific standard products.

Many consortiums are working with MCM's in one way or another. This section of the chapter reviews the activities of MCC, Sematech, SRC, and others.

Some standardization activity is being pursued with regard to MCM. This section of the chapter reviews the various agencies involved and describes their efforts.

Some semiconductor chip designers feel that MCM's will become unnecessary because everything will eventually be integrated onto one big chip. Dataquest believes that there are situations where this is likely and situations where it is not. These situations are described in some detail.

4.1 MCM Design Software

The ideal of MCM design software is that it will provide a capability so that the entire MCM module can be designed using current top down design methodologies.

Functional partitioning is an ultimate goal for a suite of MCM design tools. This concept assumes that both the chip and substrate are to be designed. The tool suite should therefore assign functions to the various chips in an optimum way and should be capable of handling both the chip design and the substrate design. Currently, most MCM projects assume that the chips are already designed; in this case the tool suite just works with the interconnect between chips.

Dataquest believes that most of the large computers that use MCM are the result of design methodologies that start at the functional partitioning level. Nevertheless, most of the projects in the merchant MCM world work with chips that are already designed. Dataquest believes that it will be some time before partitioning is part of MCM design in the merchant world.

MCM design today is being approached with tools that come from the ASIC world and with tools that come from the PCB design world. Neither type of tool is ideal for MCM's, but the PCB oriented tools may have an advantage because they represent a methodology that is closer to the MCM methodology than do the ASIC oriented tools.

All of the broad line EDA vendors are currently offering design tools, including Cadence, Mentor Graphics Corporation, Dazix, Racal-Redac Group Limited, Intergraph, and Scientific Calculations. In spite of the large vendor base addressing this application, much improvement in tools is needed and the number of tools sold so far is relatively modest.

One basic problem with MCM's is that prototype devices cannot be tested and modified in the same way as PCBs. It is no longer possible to make prototype design changes by manually cutting traces and soldering on blue wires by hand. This means that more up-front analysis is needed to achieve a design that is right the first time. In this sense, MCM design more closely resembles IC design.

MCM design requires knowledge of a number of different technical disciplines—the software suite can reduce the need for this knowledge by the extent to which it deals with technical details. Accordingly, the software must provide for thermal design, transmission line analysis, routing, simulation, and testing. It is also helpful to have available software that helps the designer estimate the performance of the MCM before the detailed design is complete.

MCC (Microelectronics Computer Technology Corporation) has a software package known as the "Design Advisor." This package provides an estimate of cost, thermal performance, signal delay and size for various substrate options. These estimates are based on a description of the chips to be put in the module and on the way these chips are interconnected. They allow the designer to choose a substrate technology before completing the actual design.

Thermal design is likely to become more important in the future. The projections of Chapter 6 indicate that CMOS power densities may grow in the next decade to the point where they exceed the power densities of the ECL chips of today. This means that thermal design will be critical if designers are to obtain the ultimate in performance. Quick, convenient thermal analysis tools will be needed and these tools will have to deal with heat flows in three dimensions.

Transmission line analysis tools are needed when chips work at higher frequencies. The frequencies that require transmission line analysis depend upon the dielectric constant of the material surrounding the line and the size of the MCM substrate. Table 6.2.1 indicates that for substrates (except silicon carbide) smaller than one inch square, frequency limit may be anything from 96 MHz to 150 MHz or more.

Since some MCM designers are using unterminated lossy lines to avoid reflections, the transmission line software must deal with lossy transmission lines as well as lines that only have inductance and capacitance. In addition, the software must provide information concerning power and ground transients and crosstalk from signal line to signal line. Some have used SPICE models to simulate transmission lines, but the computer time required for solutions of any reasonable interconnect is too high. Some current vendors of transmission line software include Quantic Laboratories, Quad Design Technology Inc, and Swiftlogic.

Various kinds of routing packages have been available for a number of years, and the routing of MCM wiring should provide no theoretical difficulties. At the practical level, the current lack of standards is a problem. There is no standard on the location of pads on MCM substrates, and it is difficult to obtain chip images from the chip manufacturer. In addition, chip manufacturers reserve the right to change their chip images from time to time as design rules allow silicon chips to shrink. Needless to say, this causes problems in MCM assembly.

Simulation can be architectural, behavioral, or gate level. Simulators should provide information on the behavior of the whole MCM module, including any transmission line effects. Sometimes this can be difficult if chip manufacturers are unwilling to provide detailed information on the behavior of proprietary chips.

The software must insure that the testing methodology is adequate. Module testing is discussed in Chapter 7, with the conclusion that testing is much simpler and less expensive if KGD (Known Good Die) are available. All that is required is that semiconductor manufacturers test their die as thoroughly as they test packaged units. Accordingly, the problem is more one of making good high frequency electrical contact to the die rather than one of devising new test procedures.

With KGD, module test just requires that the module be tested to ensure that the substrate is properly constructed and that all chips are connected to it without any opens or shorts. This can be accomplished easily if the chips are constructed with boundary scan circuitry as described in IEEE 1149.

If the chips in the module do not have boundary scan, the problem becomes more difficult. A simple functional test at the module level may be sufficient to ensure shipment of good modules, but it will be difficult for this test to provide repair information in the case of bad modules. Module test software could have a difficult time of coping with this problem, especially if chip behavioral models are not available.

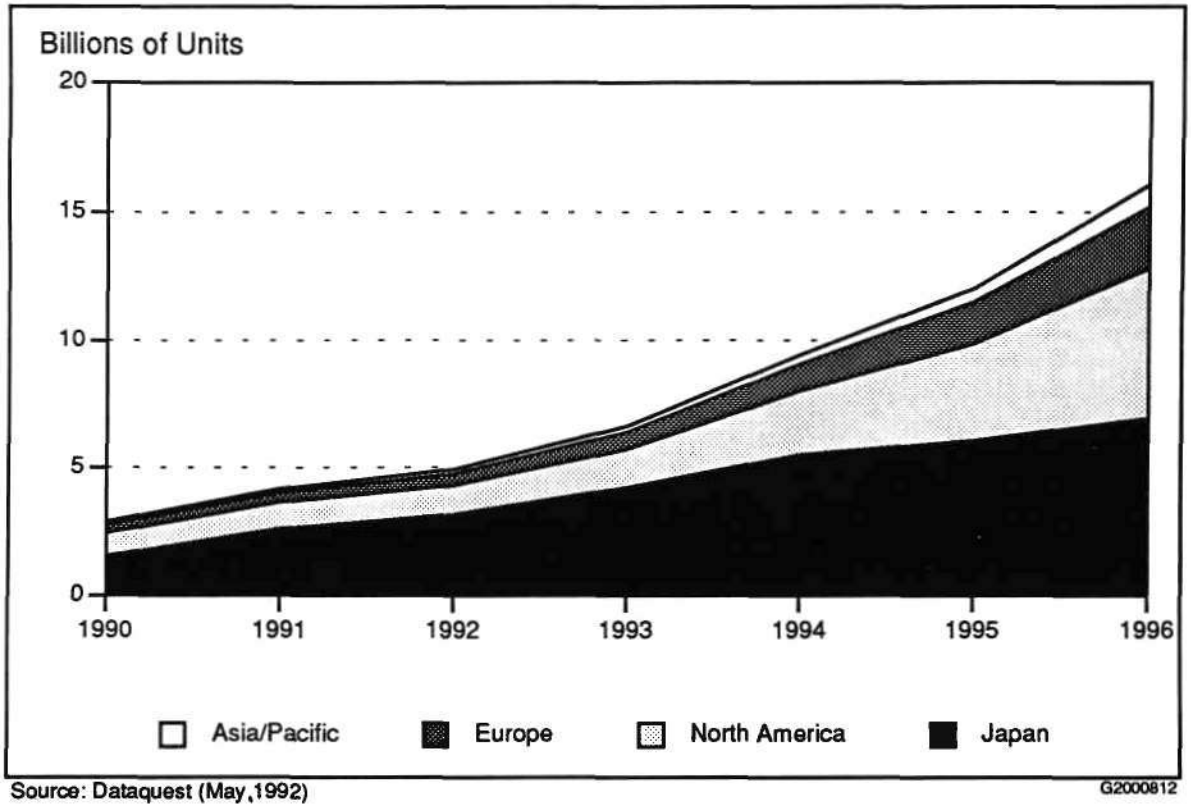
Unfortunately, KGD are not available today. This means that the module test vectors must test both the substrates and the chips. Software to solve this problem is likely to be extremely difficult. In the meantime, MCM manufacturers are likely to rely on a number of ad-hoc solutions. Easy replacement of bad chips is a help, and so is the fact that simple modules with five or less chips have low (less than 10%) rework rates.

4.2 Chip Procurement

S. Leonard Spitz, an East Coast magazine editor wisely stated in the early 1980's that for want of a chip, the package was lost; for want of a package, the board was lost; and for want of a board, the workstation, tester, handler, robot, assembly systems were lost – lost to the offshore makers.

Chip-on-board (COB) assembly of bare die onto an organic substrate was introducced into electronic calculator and watch applications in the 1960s and 1970s. Initially, the largest barriers to COB assembly were from semiconductor manufacturers that were reluctant to supply wafers and lose the value-added revenue generated by packaging assembly. The system users were reluctant to incorporate COB into high-level-systems because of the impression that COB offered less reliability at the chip-level pressure-pot test. As such COB assembly was relegated to "other low-cost expendable products." COB assembly expanded beyond PCB wire bonding into chip on tape, chip on flex, and flip chip on flex. Bare die in a COB configuration has been used extensively in video game cartridges, and low cost watches. COB eventually proved its worth in the calculator, portable phone and pocket PC markets.

Figure 4.2.1
Worldwide Bare Die Market



Source: Dataquest (May,1992)

Dataquest believes that if the MCM market is to grow to its projected size by 2000, then the supply of good or "known" good die must be made available to the market. Of the total ICs produced in 1990, more than 6.8 percent were shipped as bare die, as shown on Figure 4.2.1. Of the total bare die shipped as shown on the regional data in Tables 4.2.1 through 4.2.4, the percent assembled in a nonhybrid COB configuration of either single bare die or multichip module on laminate (MCM-L) will experience the most significant growth during the next five years.

As momentum builds in consumption of MCM-C and MCM-D designs, the competitive pressures on IC manufacturers is expected to increase the availability of known good die. Suppliers or distributors of bare die will profit from the value-added revenue generated from their ability to offer 100% temperature-tested, speed-sorted and burned-in components.

Table 4.2.1
North America
Bare Die Consumption

	1990	1991	1992	1993	1994	1995	1996	2000
Hybrid	795	892	920	1100	1680	2100	2580	1400
COB	75	98	146	272	638	1252	2201	4500
Chip on Glass MCM-C	5	7	12	18	31	76	234	2200
Ceramic MCM-C	17	21	27	46	90	186	422	2700
Thin-Film MCM-D	8	11	15	25	65	186	430	2800
Total Bare Die	900	1029	1120	1461	2504	3800	5867	13600

Source: Dataquest, May, 1992

Table 4.2.2
Japan
Bare Die Consumption

	1990	1991	1992	1993	1994	1995	1996	2000
Hybrid	629	674	720	768	825	870	893	830
COB	820	1618	1820	2050	2153	1948	1740	1200
Chip on Glass MCM-C	64	160	220	598	1080	1200	1633	4726
Ceramic MCM-C	34	144	320	510	974	1300	1700	4300
Thin-Film MCM-D	3	24	94	300	460	733	946	3670
Total Bare Die	1550	2620	3174	4226	5492	6051	6912	14726

Source: Dataquest, May, 1992

Table 4.2.3
Europe
Bare Die Consumption
(Millions of Die)

	1990	1991	1992	1993	1994	1995	1996	2000
Hybrid	161	177	200	301	420	600	800	1075
COB	137	175	223	346	503	746	1113	1800
Chip on Glass MCM-C	1	2	5	9	38	61	119	600
Ceramic MCM-C	7	13	22	43	100	211	325	900
Thin-Film MCM-D	0	0	1	4	18	16	48	900
Total Bare Die	306	367	451	703	1079	1634	2405	5275

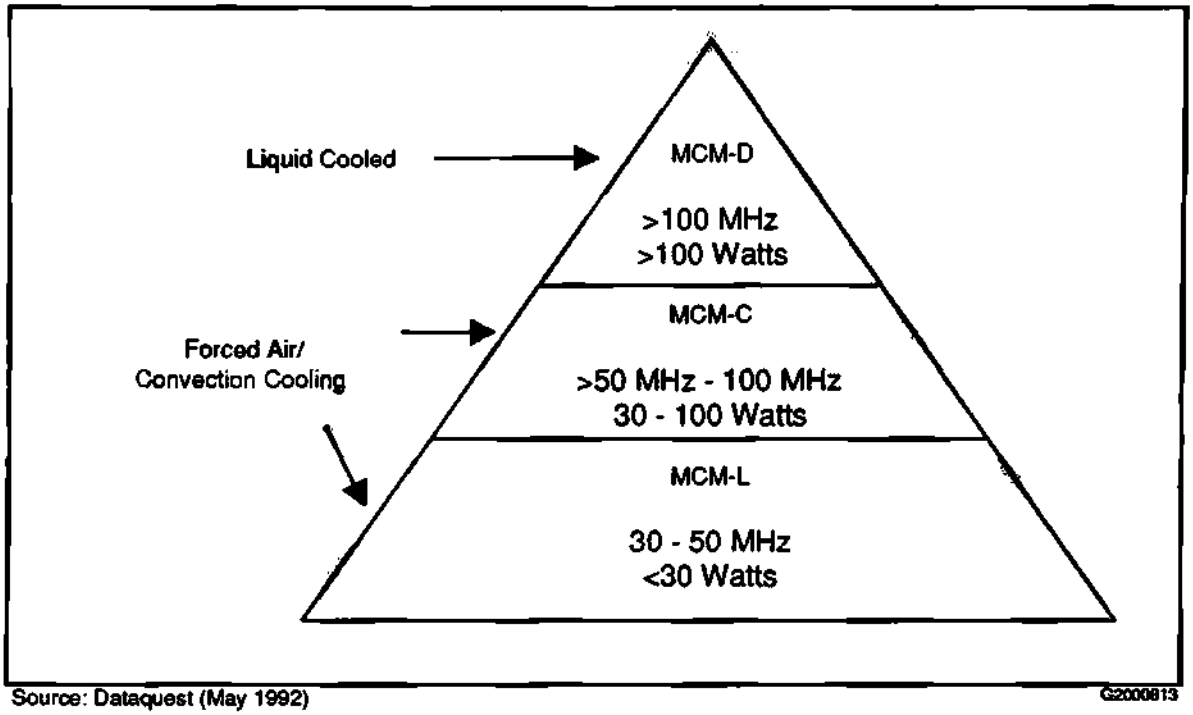
Source: Dataquest, May, 1992

Table 4.2.4
Asia/Pacific
Bare Die Consumption

	1990	1991	1992	1993	1994	1995	1996	2000
Hybrid	108	117	130	166	240	355	533	2000
COB	14	20	30	47	91	164	324	4006
Chip on Glass/MCM-C	0	0	0	0	1	2	4	22
Ceramic/MCM-C	0	0	0	1	2	4	7	34
Thin-Film/MCM-D	0	0	0	0	0	1	1	28
Total Bare Die	122	137	160	214	334	526	869	6090

Source: Dataquest, May, 1992

Figure 4.3.1
MCM Domain



Source: Dataquest (May 1992)

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4.3 Profile of the Vendor Community

Within the MCM domain, as illustrated on Figure 4.3.1, the largest investment and assembly of MCMs is being made by captive systems houses, subcontract assembly houses and bare die distributors. The greatest challenge to the captive MCM vendors such as AT&T, DEC, Motorola and IBM is not to prove the viabilitiy of their MCM technology but to move into the merchant arena and market their technology as an off-the-shelf product to the 60MHz to 100MHz domain. Dataquest believes that these MCM vendors will achieve market dominance because of their ability to understand the role of packaging in the system. Their strength will also provide the direction for standardization. Most of the subcontract assembly houses and bare die distributors listed in Table 4.3.1 function like machine shops. They will dominate the general COB/MCM-L market, providing low-cost volume MCM-L products. They will be the largest contributors to MCM designs in high-growth end equipment such as:

Table 4.3.1
Bare Die Contractors

COB Subcontract Assemblers	Bare Die Distributors
Anam Industrial Corporation	Chip Supply
Chinteik Electronics	Elmo Semiconductor
Dyne-Sem Electronics	Minco Technology Labs
Fine Products Microelectronics Corporation	
Filipinas Micro-Circuits	
Hana Semiconductor	
Hycomp Limited	
Hyundai Electronics	
IMI	
Iteq	
Lingsen Precision	
Pantronix	
Semiconductor Devices Ltd.	
SMOS/Seiko Epson	
Swire Technologies	
TEAM	
Vermont Semiconductor	
VLSI Packaging Corporation	

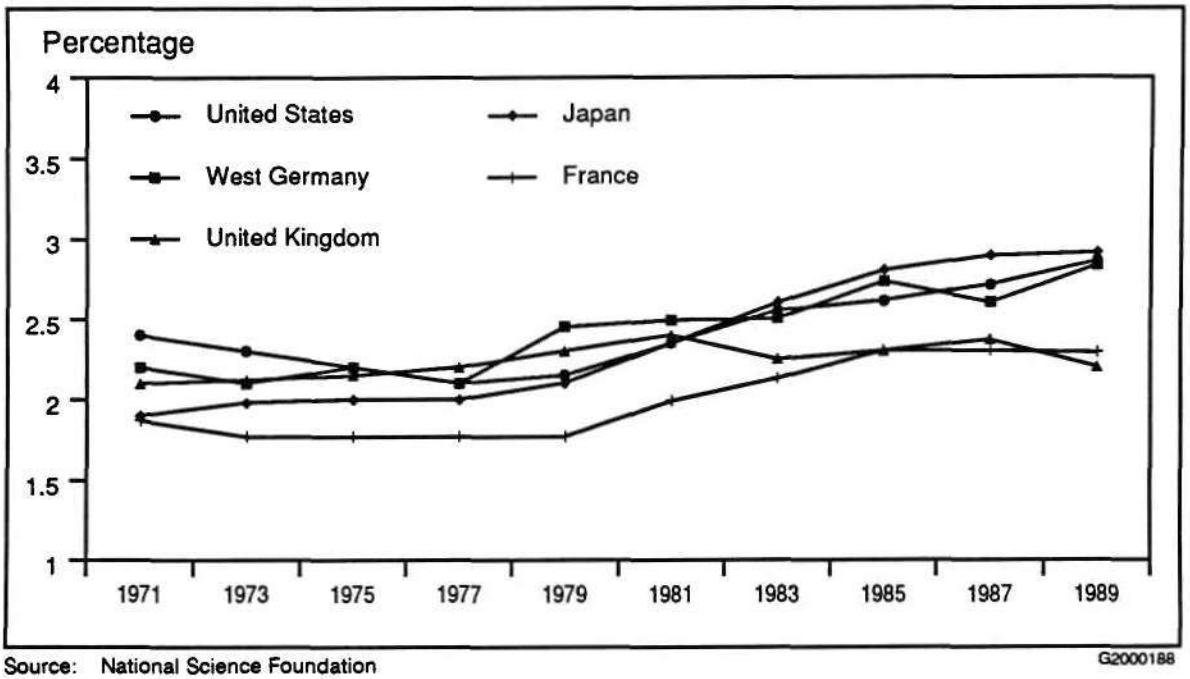
Source: Dataquest May 1992

- Laser printers.
- Laptop computers.
- LCD panels.
- Watches.
- Calculators.
- Smart Cards.
- Memory cards.
- Palmtops.
- Video games.

As cost efficiencies are proven in the MCM-C and MCM-D markets the systems houses and IC manufacturers will either participate in collaborative efforts offering proprietary packaging services or compete with each other in a global arena for the high frequency MCM domain.

The market for the 60 MHz and above thin-film MCMs did not achieve its original expected growth in 1991. As referenced in Chapter 3, the worldwide market for MCM was valued at $ 678 million dollars. Japan and North America each experienced a sluggish market environment in 1991, delaying MCM market growth by one year. Even with its declining market environment in 1991, Japan still accounted for the largest share of bare die consumed worldwide.

Figure 4.4.1
R&D/GNP Ratios by Country
1971-1988



Source: National Science Foundation
OECD, 1991
Dataquest, April, 1992

4.4 Consortium Activities

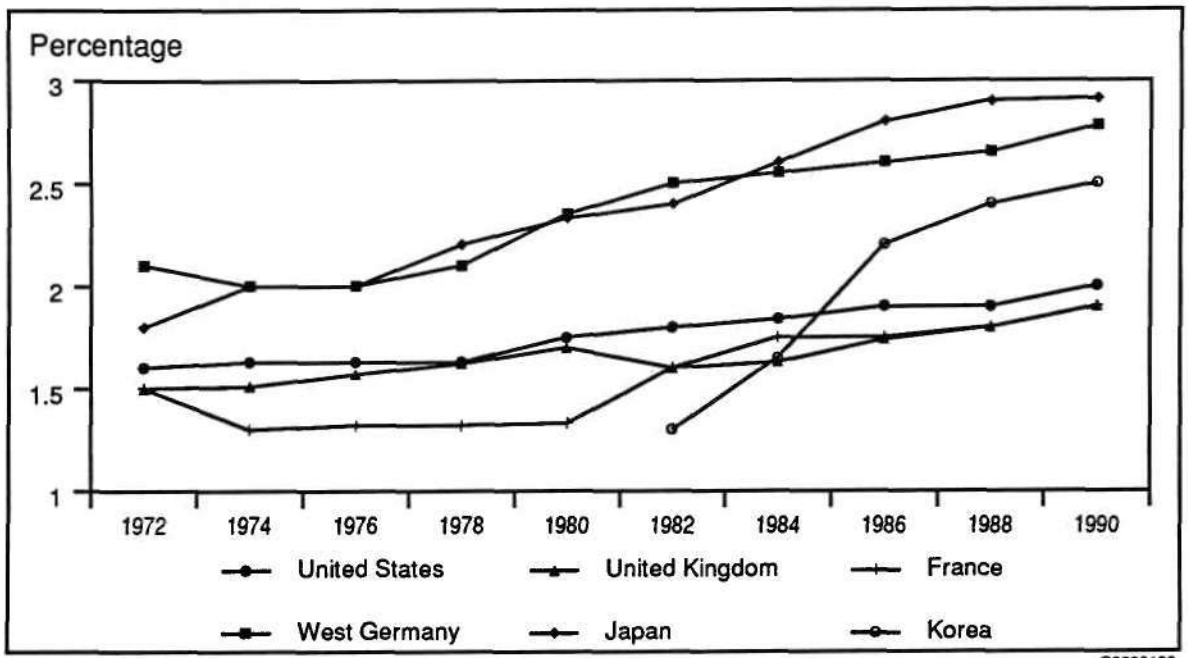
Worldwide, R&D investment, whether it filters from private investment, industry and/or government agencies, has played a major role in facilitating the improvement of existing technologies and the application of new process technologies in the semiconductor industry.

High risk technologies and the cost issues associated with these technologies resulted in the formation of national research consortia during the last decade. Research programs in Europe, Japan, and the United States, that focus on packaging interconnect projects, will be dealt with in the following section.

Worldwide R&D Spending

Historically, the United States had the highest R&D spending per gross national product (GNP) ratio, as shown in Figure 4.4.1. This figure includes defense related R&D. From 1987, the R&D per GNP ratio of Japan has continued to grow, while R&D/GNP ratios of the U.S., West Germany, and France have remained flat, and the U.K. has declined. As a nation, Korea upgraded its technical infrastructure at phenominal rates. By 1988, Korea was spending 2% of its GNP on R&D, with three quarters of that burden carried by the private sector. Korean research spending is expected to reach 5% of GNP by 2001. Although it is not shown on the figure, Taiwan's R&D spending was 1% of its GNP in 1986 and it is expected to grow to 2% of the GNP by 1996.

Figure 4.4.2
Nondefense R&D/GNP Ratios by Country
1971-1988



Source: National Science Foundation
OECD, 1991
National Science Board
Korean Ministry of Science
Dataquest, April, 1992

A comparison of non-defense related R&D/GNP ratio is shown in Figure 4.4.2. Since West Germany and Japan are legally restricted in their defense related R&D spending, most of their investment is geared to industry related efforts. In 1990, 40 % of the total expenditure for U.S. R&D was from the Federal Government, with defense being the largest area of funding. Of the $58.5 billion allocated to R&D, $35.9 was budgeted for Defense Agencies.

United States

During the first two decades of the semiconductor industry in the United States, federally subsidized R&D programs were typically aimed at defense applications, with a large portion of U.S. manufactured semiconductor ICs consummed in the military sector.

Constrained by anti-trust laws, U.S. companies catering to merchant/commercial application markets were fiercely independent in supporting their internal R&D programs.

Table 4.4.1
United States Research Consortia

Consortium	Established	1991 Funding
MCC	1982	$ 55 million
Sematech*	1987	$190 million
SRC	1982	$ 29.1 million

*All members of Sematech are required to be members of SRC.

Source: Dataquest, April, 1992

Increased technological complexity, design, manufacturing, marketing and wafer fab costs, as well as fierce foreign competition, resulted in a restructure of the antitrust laws. During the 1977 through 1980 time frame, the Justice Department's adjustments in antitrust guidelines concerning research joint ventures, opened the doors to consortia development as shown in Table 4.4.1.

SRC has contracted more than $11 million for packaging research since inception of its packaging program in 1983. MCC's packaging interconnect program is a continuation of the original six year, $30 million packaging program initiated in 1983. Through its cooperative efforts with SRC, Sematech has indirectly supported a packaging interconnect research infrastructure.

As part of a continuing effort to follow emerging technologies for the purpose of developing new and/or improved products by the year 2000, members of these research consortia as well as academia, and government agencies and labs have developed a National R&D Plan for Electronic Packaging. Formed in January, 1992, this National Packaging Program will focus on the following technologies:

- Signal transmission and interconnect.
- Design and simulation of packages and assemblies.
- Environmental protection of ICs.
- Multichip module design for test and test methods.
- Power/thermal technologies and analysis.

From the Government sector, DARPA continues to subsidize multichip module research in both industry and academia. DARPAs 1990 $20 million contract was awarded to two industry teams:

Team 1: Texas Instruments and General Electric.

Team 2: E-Systems, nChip, National Semmiconductor, Cypress, Multichip Technology, General Dynamics, and Fairchild Defense.

Under this three year contract both teams will focus their R&D efforts on establishing a merchant foundry for MCM development. Table 4.4.2 lists advanced packaging funded programs in universities and labs during 1990 and 1991. DARPA, along with other federal agencies, consortia and industry allocated over $300 million for these programs.

Table 4.4.2
University Packaging Interconnect Research
1990 - 1991

University	Project Support	Project Focus
Auburn University	N/A	BCB Interlayer Dielectrics 3D Simulation/ High Speed Interconnect
Carleton University	N/A	Interconnect Delay & Crosstalk in MCMs
Carnegie Mellon University	DEC IBM Rockwell SRC	Asymtotic Waveform Evaluation
Cornell University	SRC	Packaging Design Thermal Management
Florida Atlantic University	NSF	MCM Testing
Lehigh University	SRC	Packaging Design, Fundamental Materials Packaging Integrity and Engineering
Massachusetts Institute of Tech	USAF	Coplanar Packaging Techniques for MCMs
Purdue University	SRC	Thermal, Physical Electrical & Mechanical Properties of Package Materials
Rensselaer Polytechnic Institute	N/A	Capacitance Extraction for MCM Interconnect
Sandia National Labs	US Dept. of Energy	MCM Assembly Test Chips
Stanford University	FBI	Field Programmable MCM Systems
	DASH	Scalable Parallel Machines
	SRC	Membrane Probe
	NASA ATT	MCM Environments
University of Arizona	SRC	MCM Switching Noise CAD Tools for MCMs Electrical/Thermal Simulation System

Table 4.4.2 (cont.)

University	Project Support	Project Focus
University of California Berkeley	SRC NSF SRC	MCM System Partitioning Transient Simulation of Lossy Coupled Transmission Lines
	N/A	MCM Interconnecting Circuit & Fluxo Electronics
University of Cinncinati	USAF Wright Labs	Boundary Scan Test Structures
University of Colorado	NSF	MCM & Flip Chip Thermal Compression Bonding
University of Maryland	CALCE Research Ctr	HDI Overlay
University of Michigan	DARPA Seattle Silicon Mentor Graphics	MCM Interconnect Delay MCM & System Performance
University of California Santa Cruz	NSF SRC State of California NSF SRC	RISC in the MCM Environment Thin Film Substrates Bus-based Packet Switch/MCM
University of Southern Calif	Samsung Sandia Labs ISI,GE,Micron DARPA	MCM for Cellular Mobile Telephone Sys. Membrane Probe for Bare Die Test High Density Systems Module
University of South Florida	DARPA FHTIC Honeywell Gigatest	Bare Die/Membrane Probe Test 3-D MCMs
University of Wisconsin/ Milwaukee	Mayo Foundation	Lossy Transmission Lines

Source: Dataquest, April, 1992

Table 4.4.3
Package Related R&D Program Structures in Japan

AIST-Agency of Industrial Science & Technology

R&D Projects of Basic Technology for Future Industries

1. Superconducting Materials
2. New Materials
   - High Performance Ceramics
   - High Performance Plastics
   - Photonic Materials
   - High Performance Materials for Severe Environments
   - Silicon-based Polymers
3. New Electron Devices
   - Superlattices
   - 3-D ICs

Source: MITI, 1991

State Funded R&D

State funded R&D totaled more than $13.3 billion in the U.S. in 1983. By 1990 there were over 160 state funded programs nationwide for high technology programs. State funded programs were instituted to encourage:

- job training.
- technical trade/foreign investment.
- favorable tax policies.
- strong industrial bonds.
- industry development.
- modernization of industry through electronics.

An example of a state funded program that emphasizes packaging is the Alabama Microelectronics Science and Technology Center. This program was established at Auburn University in January, 1984, through a special legislative appropriation with continuing state support. The charter of the center is "to advance microelectronics education and technology." Multichip module research has been ongoing in the center since September 1984. Research activities include material characterization, process development, and MCM-L, MCM-C, and MCM-D module designs. In addition, prototype MCMs have been fabricated under contract. Facilities exist for CAD, artwork generation, thick film substrate processing, multilayer thin film substrate processing, printed wiring board processing, chip and wire assembly and surface mount assembly.

Table 4.4.4
European Packaging R&D Projects

Company Projects	Collaborative Projects
Siemens	ESPRIT - Phase 1
Contraves	ESPRIT - Phase 2
RISH	EUREKA
MCM Consortium	RACE
Thomson 3-D Package	

Source: Dataquest, April, 1992

Japan

Within the framework of their massive technopolis programs of 1980, MITI, in close collaboration with universities and industries, provided significant funding for R&D projects that would have long range benefits to packaging and interconnect applications. The programs listed on Table 4.4.3 are being subsidized through 2000.

The focus of Japanese industry on packaging technology is now directed at the following market trends and applications:

- IC Card packaging technology.
- Bare chip packaging technology.
  TAB/Flip Chip.
- Chip on Glass (COG) high density packaging for driving LSI.
- Advanced fine-pitch SMT.

Europe

In Western Europe there are two main sources of government funding for research and development in semiconductor technology and its applications: a European Community (EC) budget administered by the Commission in Brussels; and funding at national government level.

In Europe, the primary semiconductor research programs are ESPRIT and JESSI. ESPRIT is an EC program; JESSI is not. JESSI is part of EUREKA, which was developed from a French-German initiative started in 1985 and relies on national government money. It has developed in parallel to EC research, but coordinates with EC programs. Whereas EC research is mainly concerned with pre-competitive and basic research, EUREKA projects are nearer to the market. In the case of JESSI (now the biggest EUREKA program) there is considerable synergy with many of the ESPRIT projects. This coordination centralizes funds, enabling both EC and national government money to be used on the same projects.

In addition to ESPRIT, there are three other EC programs that directly benefit the European semiconductor industry. These are RACE, DRIVE, and BRITE/EURAM. RACE and DRIVE have subprograms that involve applications for semiconductors. RACE is involved in telecommunications, and DRIVE in transportation. BRITE/EURAM is concerned with research into basic raw and advanced materials.

Table 4.4.5
European Collaborative Packaging R&D Projects

ESPRIT	EUREKA	RACE
Phase 1	Optoelectronics	Optoelectronics
300+ I/O TAB	Telecom MCMs	Low cost MCM
Optical Interconnect		ISDN
Phase 2		
APACHIP		
MCM-L		
MCM-D		

Source: MCC International Liason Office

Table 4.4.4 lists the packaging/interconnect-related projects separated by company independent research as well as collaborative research.

Siemens high pin count TAB "Mikropak" technology is now used in the Siemens 7500H90 water cooled mainframe system. Contraves "Polystrate/Ultrastrate" MCM technology is aimed at workstation, mainframe and telecommunications systems. The RISH consortium formed by Bristish Aerospace, GEC Plessey, Lucas Automotive, Mars Electronics and the Ministry of Defense investigated the use of silicon substrates for the development of MCMs. Achievements under the RISH program were:

- examination of thermal and electrical characteristics of silicon hybrids.
- evaluation of flip chip, TAB, and wire bonding as chip attach methods.
- construction of prototypes for silicon hybrids.

The MCM consortium is an extension of the RISH project. Under this program, the RISH technology will be transferred to the fabrication stage. The project aims to establish the overall integrity of the silicon MCM method.

The Thomson-CSF 3-D packaging technology is an 8-layer stackable SRAM module, incorporating wire bond assembly in a leadless carrier or ceramic package.

Table 4.4.5 lists the packaging developments achieved via the collaborative projects shown in Table 4.4.4.

4.5 Standardization

Since the majority of captive systems houses engaged in either the computer and/or telecommunication industries are the largest producers and consumers of MCM technology, it would be reasonable to assume that MCM standards would best be driven by this same group. This has not proven to be true in the development of single chip package standards. Historically, standards set have often been de facto standards, strongly influenced by the component market leaders. Heretofore, the fabrication practices that

prevailed in the merchant market segments during the last decade are seen as having influenced over 90% of the single chip package standardization process.

The worldwide merchant semiconductor industry currently lacks the infrastructure and the education in the use of MCM technology for volume ramp up. Thus, the ultimate acceptance of MCM technology will greatly depend on a vendor's ability to create a demand for products by designing the system using the module technology. The success of MCM vendors will not derive from their ability to supply only substrates/modules and design services.

Standardization processes for MCM will occur when and if large-scale producers such as AT&T, IBM, Motorola, PMC and Toshiba ramp-up into full scale production and force standardization through volume produced and consumed. By selling standard off-the-shelf commodity products that use MCM technology they can

- select products that are high volume.
- have direct control over the majority of the chips, as well as the test programs.
- offer a product of value and function knowing the true benefits of the technology.
- offer product at low cost with little or no risk.

Knowledge of linewidths, cost/square inch, substrates and electrical test and repair issues are complicated tools and unwanted risks to the majority of potential MCM users. Proponents of single chip view MCM technology as a very complex, custom, and costly investment. System designers view MCM as a power tool to improve system speed and performance. The economist George Stigler once remarked that a business firm is a collection of devices to overcome obstacles to profit. Although the standardization structure within which companies have operated has created obstacles to profit, MCM complexities viewed as obstacles by the inexperienced could provide opportunity to the MCM experts. The MCM impetus will not be driven by complex standards. MCM standards don't have to be the best; any standard that works will satisfy the user.

Traditionally, industry standardized electronic package outlines have been defined and ratified by one of several committees. Japan has its Electronic Industry Association (EIAJ). The U.S. has its Joint Electronic Device Engineering Council (JEDEC), JC-11 committee. Although the standards process cycle varies between the U.S. and Japan, the normal standard lifecycle from the time that the standard is submitted through its final acceptance averages 1.5 to 2 years. For the company submitting the package outline for ballot approval, the process has become an endless and costly maze of ballots and redesigns as shown in Figure 4.5.1.

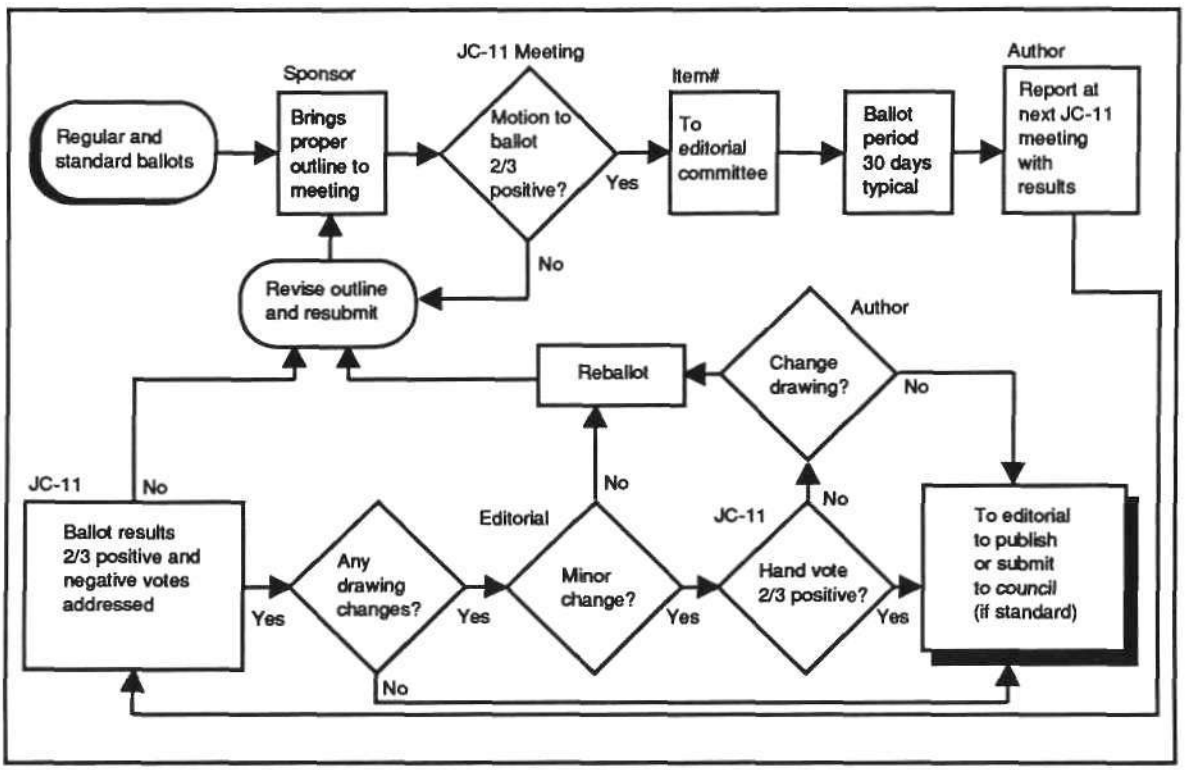
For the systems house, the effect of standardization on the typical assembly process is shown in Figure 4.5.2. As package standards continue to evolve, the cost in upgrade and design time to the system designer are significant. As a case study, Hewlett Packard tracked the typical process development lifecycle for a QFP designed into their palmtop and workstation equipment. The entire six step process from proposal of design through PCB assembly involved 1 year and approximately 4 to 6 people.

Package standard outlines typically include pincounts, mechanical dimensions and tolerances as well as gauges or overlays for verifying critical features. Standard outlines typically do not include specification of materials, specification of material handling or electrical performance requirements.

Through the efforts of MCC, representatives from consortia, industry and government agencies are working together to develop MCM standards for the following reasons:

- to reduce the cost of prototyping/low volume.
- to reduce turnaround time.
- to stimulate vendors to invest.

Figure 4.5.1
JEDEC JC-11
Registration and Standards Ballot Flowchart



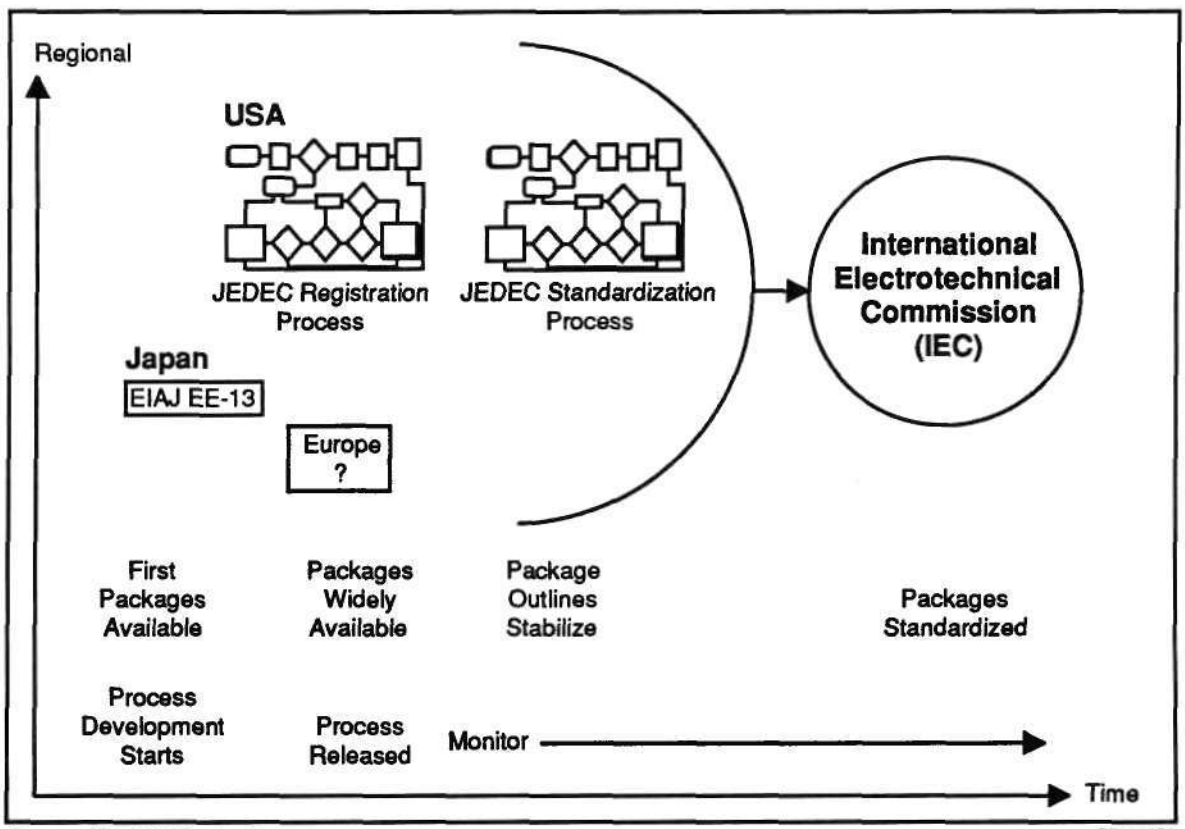
Source: JEDEC G2000190

- to promote dual use for commercial and government markets.
- to accelerate manufacturing by consolidating volume.

The areas that they have designated for standardization include the following:

- substrate size/package connectors.
- device size/footprint.
- electrical interfaces.
- customer/vendor data transfer interfaces.
- device pin-out/performance models.
- QC/reliability specs and test.
- device mountings and module attachment techniques and materials.

Figure 4.5.2
Impact of Package Standardization
On System House Assembly Process Development



The following groups are participating in the development of MCM standards:

Committees	Agencies	Ad Hoc Committees
JEDEC	RADC	HDPUG/Europe
ISHM	NWSC	(High Density
IEPS	NIST	Packaging Group)
IPC/Japan		
ASTM		
IEEE		
SEMI		
SMTA		

Table 4.6.1
Chip-Level Comparison of Single and Multi-Chip Implementations of the Same System Function

	Multi-Chip (Each Chip)	Single Chip
Relative Complexity of Single Chip	----	4 X
Edge Dimension* (mils)	380	730
Max. Peripheral I/O Pins**	152	292
Wafer Cost ($/sq.in.)	$40	$40
Gross Die Cost	$5.78	$21.32
Yield (Murphy)	35.2%	5.3%
Yielded Die Cost	$16.43	$398.56
Yielded Test Cost	$1.64	$24.77
Net Die Cost	$18.07	$423.33

*Assumes square chip. Allowance for bonding pads is a 15 mil border on all sides of the chip.

**Assumes one pin every 10 mils.

Source: Dataquest, April, 1992

4.6 Superchips vs MCM

Two schools of thought have emerged in the semiconductor industry. One school believes that VLSI chips will ultimately be so complex that almost any conceivable function can be built on a single chip; the other believes that multichip modules offer advantages over single chips in many cases.

Multichip modules (MCM's), especially those with high density interconnect (MCM-D), make it possible to hook up many chips and get single chip performance. This report shows when it makes sense to do this.

The multiple chip option provides big cost savings where the single chip version would be difficult to make – savings which decline with time if yields are improved through product shrinks and redesigns.

Another advantage of the multiple chip option is that it may have shorter development time at lower risk.

Single chip is the low cost option if the chip is not too complex. For semiconductor users, this option avoids the need to deal with separate chip and module vendors.

Economic Issues

The economic benefit of the multiple chip option depends on the market situation. There are three cases:

- Product shipments limited by wafer fab capacity.
- Product prices set by the single chip option.
- Product shipments set by the market.

Table 4.6.1 assumes that four single chips of 380 mils on a side can be replaced by a single chip of 730 mils on a side. This larger chip is a little less than four times the area of the single chips because less area is required for input/output pins. The yields are computed using Murphy statistics, and the resultant costs are computed.

When product shipments are limited by wafer fab capacity it is important to note that the MCM solution of Table 4.6.1 will ship 25 modules per 8 inch wafer while the single chip solution will ship 3 units per 8 inch wafer. If the available wafer capacity is 1000 units per month, the MCM solution will ship an extra 17,000 units per month. This will result in extra product sales which should generate significant extra revenue and market share.

If product prices are set by the single chip solution, the module might sell for $1075 (50% gross margin from the costs of Table 4.6.3) and the cost savings is $320 each. If the MCM vendor wished to gain market share instead of maintaining high margins, the MCM could be priced to make the single chip unprofitable.

Product shipments are set by the market if the MCM is of the customer-specific type. Saying it another way, the demand for the chip depends only on the demand for the product in which the chip is used. If the product in question ships 1000 units per month, monthly savings of $320,000 are generated.

Single chip costs decrease more rapidly with time than MCM costs, so these savings illustrated above do not persist. Then, neither does anything else in the electronics business. The timing of the relative costs between the MCM and single chip options is described later in this section.

Other Advantages of MCM's

MCM's may offer shorter time to market

- Some new products can be developed simply by using a new combination of standard chips.
- Chip design times are shorter because design software is readily available.
- Prototype runs are shorter because chip yield is high and chips can be debugged in parallel.

MCM's make it possible to work with more wafer vendors since acceptable yields can be achieved with wafers of lower quality.

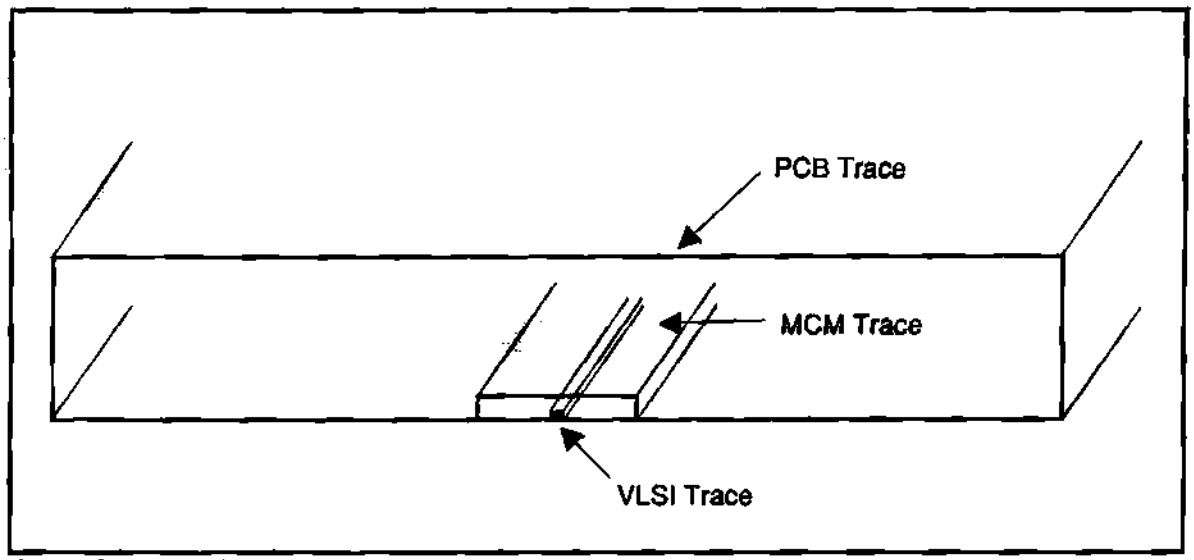
MCM's can mix products made with optimized CMOS processes, like SRAMs and DRAMs.

MCM's can handle mixed technologies like GAAS, ECL and CMOS.

MCM's can have higher clock rates because MCM interconnect has less series resistance than on-chip interconnect.*

* "Electrical Characteristics of Digital Circuit Interconnects: Printed Circuit Boards, Multichip Modules, Monolithic Integrated Circuits," William Henredon, Wescon, 1992

Figure 4.6.1
Cross Sectional View of Typical Metal Traces
on a VLSI Chip, an MCM-D Substrate, and a PCB



Source: Dataquest (May 1992) G2000253

Figure 4.6.1 gives a cross sectional view of typical metal traces on a VLSI chip, an MCM-D substrate and a PCB. Since series resistance depends on the cross sectional area, the PCB will have much less resistance than the MCM which will have much less resistance than the VLSI trace. In the case illustrated here, the area of the MCM trace is 88 times larger than the area of the VLSI trace. The PCB cross sectional area is 38 times larger than the area of the MCM trace.

Signals on the VLSI chip tend to be slowed by the high series resistance of the chip traces. The traces on the MCM offer shorter delays because of their lower resistance. PCB traces are so low in resistance that they require termination to eliminate overshoot and ringing. In addition, the distances to be travelled on the PCB are longer, so delay times on the PCB are longer than on the MCM. The delay times for these three alternatives are given in Table 4.6.2. This table assumes that a 4 chip system is implemented in the MCM and PCB.

Cost Timing Scenario

In the long run yields improve and single chip costs become less than MCM costs. But, as Lord Keynes observed: "In the long run we are all dead." This section deals with the timing issue that is so critical in the fast paced electronics industry.

Table 4.6.1 gives costs for a 4 chip design and for the single chip that replaces it. In this example, four chips at a total of $72 are much less expensive than the single chip at $423.

Table 4.6.2
Computed Delays for a 4 Chip System
As a Single Chip, MCM, and PCB

Single Chip	MCM	PCB
1.5 ns	1.2 ns	2.6 ns

Source: Dataquest, April, 1992

In this table, wafer costs of $40 per square inch assume an advanced CMOS process. The chip yields are typical of microprocessors; gate arrays of the same chip size have higher yields. For comparison with current microprocessor designs, the DEC Alpha and MIPS R-4000 chips would have edge dimensions of 601 mils and 550 mils, respectively, if they were square chips. Both these chips are leading edge, and Dataquest believes that their yields are in the range shown for the single chip in Table 4.6.1.

The larger chip is not four times the area of the single chip because some of the I/O lines needed for the four chip solution are internal to the single chip.

Murphy yield statistics are assumed in extrapolating the yield from the smaller to larger chips.

The costs of Table 4.6.1 are accurate, but not comparable. The four chips need to be hooked together to function like the single chip. This adds cost to the MCM solution as illustrated in Table 4.6.3. Here the single chip solution costs about 2.5 times as much as the 4 chip one.

The rework cost in Table 4.6.3 is low because 95% of the chips work correctly after assembly and, as a result, 81% of the modules do not need rework.

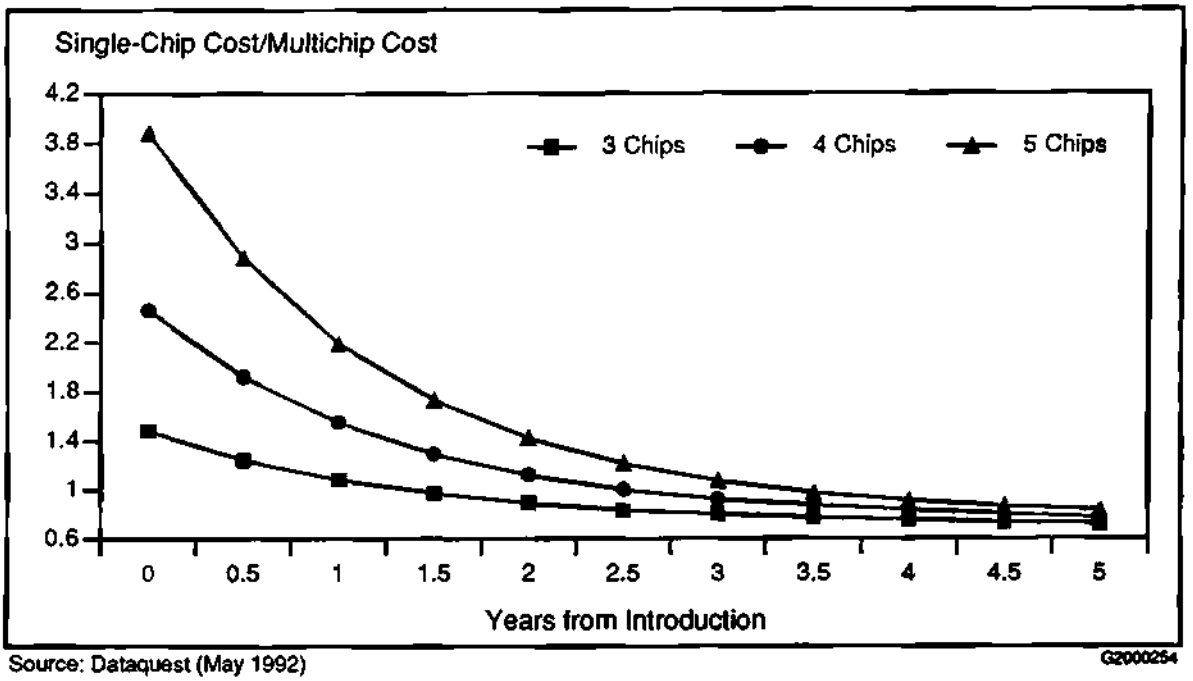
Table 4.6.3 illustrates costs for a single moment in time, but, as we all know, chip yields improve with time. Moreover, the single chip option has more possibility for yield improvement since its yield is so low to begin with. The result of this is that the single chip version will, in time be the least expensive option.

In Figure 4.6.2, the timing of yield improvement is computed by decreasing manufacturing defect densities and chip area by 15% and 23% per year, respectively. Dataquest believes these yield improvements can be obtained for chips that are made in high enough volumes so that it makes sense to fund many shrinks and redesigns. These yield improvements are optimistic for low volume chips – in this case, the MCM advantage would persist for a longer time.

Figure 4.6.2 shows the impact of these yield improvements on the costs of Table 4.6.3. It plots the ratio of single chip cost to multiple chip cost. When this ratio becomes 1, the two options have the same cost. At zero years this ratio is 2.5 (for the four chip curve), indicating that the single chip option is 2.5 times as expensive as the Multi-Chip option. This corresponds to the situation of Table 4.6.3. Cost parity (a ratio of 1) is reached at 2.5 years – this means that the 4 chip solution would be lowest cost for 2.5 years, while a single chip solution would be lower in cost thereafter.

Figure 4.6.2 also gives curves for 3 to 1 and 5 to 1 complexity ratios. In the 3 to 1 case, cost parity is reached in 1.5 years; in the 5 to 1 case, parity is reached in 3.5 years.

Fig. 4.6.2
Relative Module Cost



Source: Dataquest (May 1992)

G2000254

Strategic Considerations

The key advantage of MCM's is that their performance can equal or exceed that of a single chip of equivalent complexity. Other packaging technologies do not offer this advantage.

If single chip designs do not have a performance advantage over MCM's, then the only reason to implement a single chip design is to obtain a cost advantage.

The single chip option has a cost advantage only when yields are high enough to offset the extra packaging cost of the MCM. Thus, the new development strategy is to implement complex functions as an MCM until cost parity is reached and then convert to a single chip version.

Multiple designs and shrinks are assumed in both the single and multichip case because these drive yield improvements. Dataquest believes that the redesign cost is similar for both the single and multi chip options. Low volume chips are not redesigned so frequently—in this case the MCM advantage may persist for a longer time.

Chip designers will have to give some thought to the transition from multi to single ship in the early design stages if this transition is to be graceful.

Table 4.6.3
Assembly-Level Comparison of Single and Multi-Chip Implementations of the Same System Function

	Multi-Chip (Four Chips)	Single Chip
Net Die Cost	$72.28	$423.33
External Package Cost (Including Heat Sink)	$87.60	$87.60
MCM-D Substrate Area (60% Coverage)	0.96 sq.in	------
MCM-D Substrate Cost (at $35/sq.in.)	$33.69	------
Assembly (at $.012/Wire)	$7.30	
Test	$13.14	$13.14
Rework*	$16.89	
Gross Cost	$217.75	$510.93
Final Yield	100.0%	95.0%
Net Module Cost	$217.75	$537.82

*Assumes probability of a good chip is 95%. Rework labor is 10X assembly labor. Single Chip is repaired.

Source: Dataquest, April, 1992

In the past, chip designers have been balanced on a knife edge of uncertainty: if their chip was too complex, yields would not improve in time to capture the volume market – if the chip was not complex enough, some competitor would provide a more cost effective chip. Today, the MCM option offers a two step approach to chip design that lessens risks and makes introduction of complex functions more predictable.

Chapter 5 – Interconnect Trends

5.1 Driving Forces in Single Chip Packaging

Single chip packaging competes with multi-chip packaging so the acceptance of MCM's will partly depend on the progress that is achieved in single chip packaging. Both technologies share the same market driving forces: package delay in high performance applications, physical size of the package, and cost.

Memory and logic make different demands of packaging technology. The pin out of memory chips increases only slowly as the number of bits on a chip increases. In fact, if the memory structure does not change, a doubling of the bit capacity requires only one extra address pin. If a memory has 28 pins, one twice as large would require only 29 pins. Thus, the pin count increases only 3% as the memory size doubles.

By contrast, the pin count of logic devices follows the rule that the number of pins required is roughly proportional to the square root of the number of gates. Thus, if the number of gates were to double, the pin count would need to increase by about 40%. This relationship is known as Rent's rule – depending on the system architecture, the pin count can be proportional to the number of gates raised to a power somewhat greater or less than the square root. Regardless, the number of pins on a logic chip will increase much more rapidly with chip complexity than the number of pins on a memory chip.

Figure 5.5.1 illustrates graphically the trends in single chip packaging. Chip complexity increases every year, and the result is only a slight increase in memory chip lead count. Since most systems have lots of memory, there is a market demand for more dense memory packaging. This has led to thinner memory packaging such as the TSOP. Lead on chip makes memory packaging more dense because it allows a wider chip to be put in the same memory package. Other dense packaging techniques include memory cards and stacked memory.

By contrast, logic chips increase rapidly in pin count with time. Increases in package pin count are being accommodated through either the Quad Flat Pack (QFP) approach or the array grid approach. The difference between these two approaches is that the QFP approach places the package pins on the periphery of the package while the Grid Array approach places the pins or pads all over the bottom of the package. This latter approach offers a higher pin count capability because all of the package area is utilized for pins.

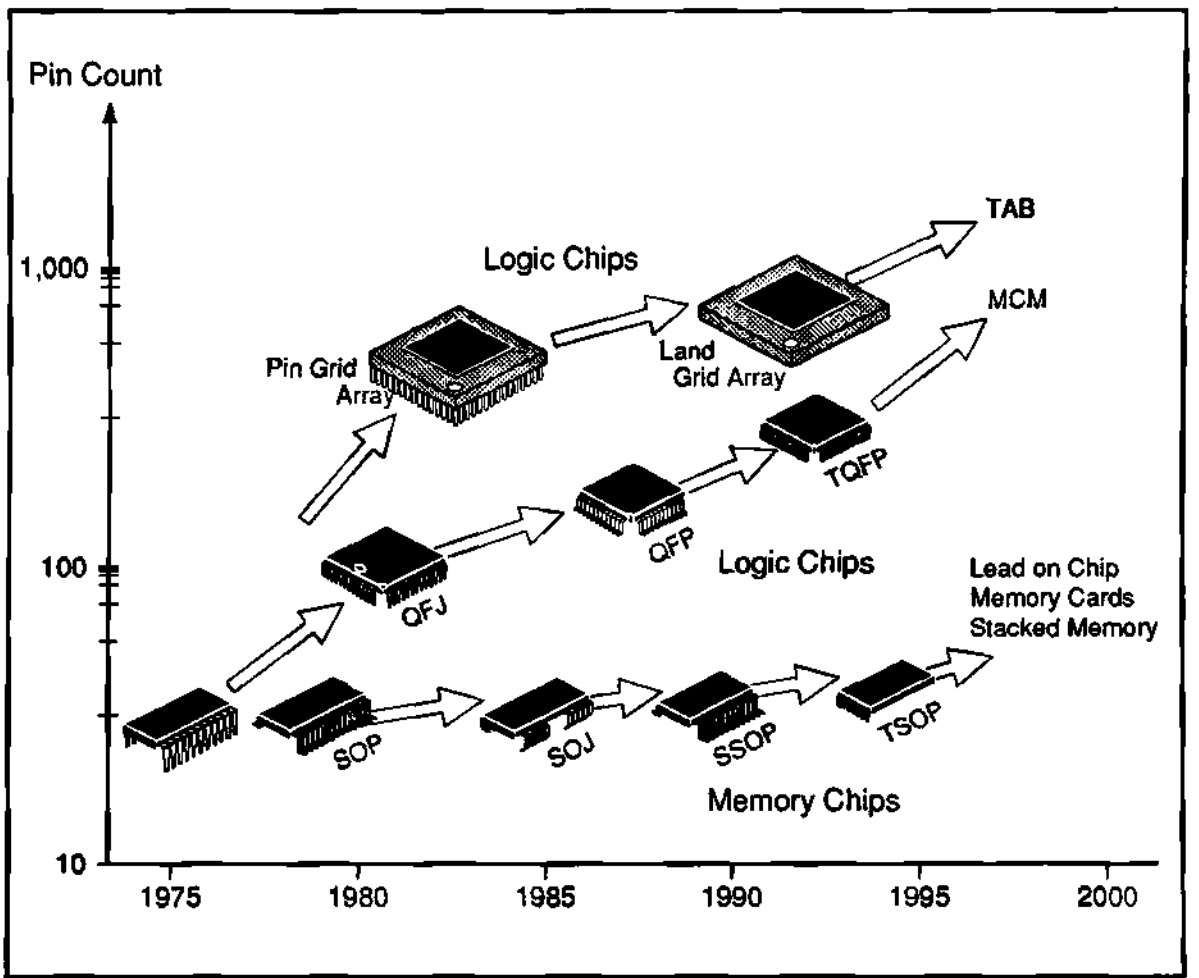
The land grid array is a surface mount version of the Pin Grid Array (PGA). It is much easier to interconnect than the PGA because it does not have pins that go all the way through the printed circuit board. Thus it is possible to run unrestricted wiring beneath the land grid array without concern for the pad locations. This makes board layout much simpler.

Logic packaging will continue to migrate towards higher pin counts. TAB has been used in some applications to obtain high packing densities, sometimes in conjunction with MCM's. Other interconnects being evaluated for MCM include wire bond and flip chip.

QFP's are evolving towards closer pin to pin spacing so that more leads can be put on the same size package. The original spacing was 50 mils, but now packages are being constructed with .65mm (25 mil, approximately) spacing and predictions are that the pin spacing will fall to .3mm (12 mil, approximately). The .65mm packages will go to 256 pins or more, while it is anticipated that the .3mm packages will have 500 pins or more.

The pin spacing on PGA's is traditionally 100 mils. Such packages may contain up to 720 pins. There is also a trend towards 50 mil pin spacing. The land grid array is forecast to have 1000 pins.

Figure 5.1.1
Evolution of Single Chip Packages



Source: Dataquest (April 1992)

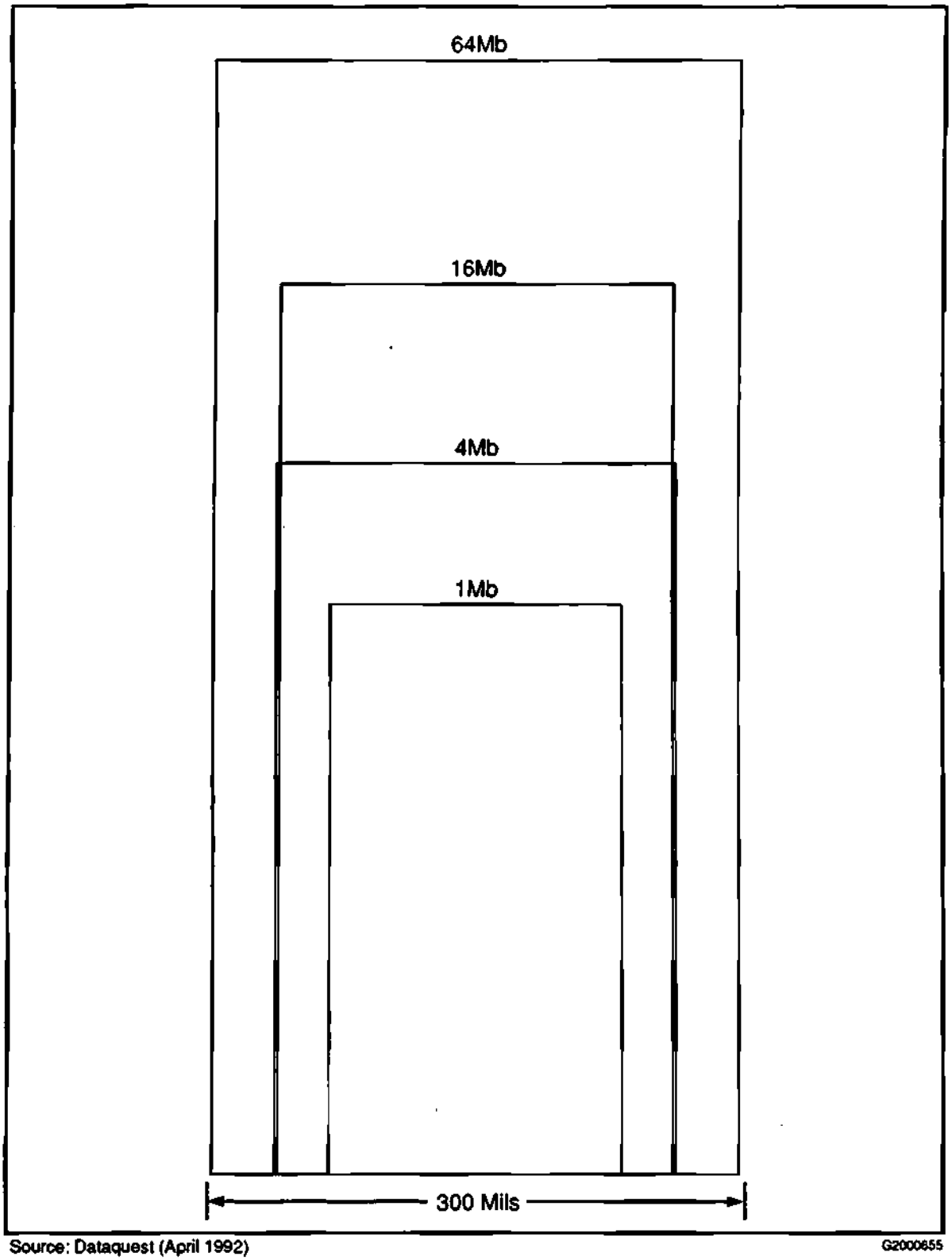
The limit on pin or pad spacing is solderability; if the pins or pads are too close together, the solder may bridge two adjacent pins or pads, leading to unwanted short circuits and an inoperative PCB. Most feel that it will be difficult to solder pins that are more closely spaced than 10 mils, though some TAB devices have been reported with 8 mil spacing.

Memory Packaging

Usually, memory chips are mounted side by side on a PCB. Since most systems use a lot of memory chips, there is a need to package these chips as close together as possible. Thus, users will favor a memory chip that is in a narrow package over one that is in a wide package. For this reason, the 300 mil wide package is favored over one that is 400 or 500 mils wide.

Figure 5.1.2 shows some average sizes for DRAM chips are reported at the International Solid State Circuits conference. Notice how memory manufacturers have chosen high length to width ratios so that they can fit their chips into the 300 mil package width.

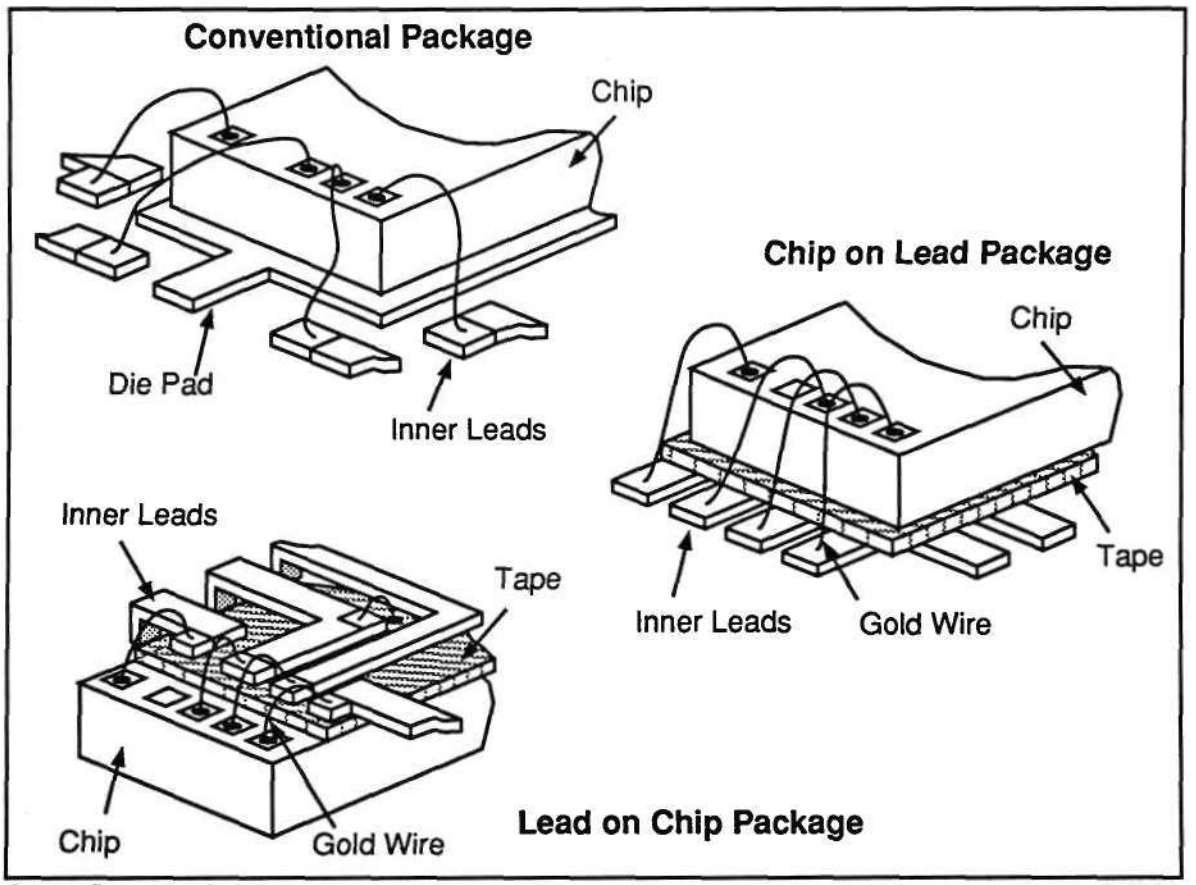
Figure 5.1.2
DRAM Chip Aspect Ratios



Source: Dataquest (April 1992)

G2000655

Figure 5.1.3
Conventional and Advanced Memory Packaging



Source: Dataquest (April 1992) G2000656

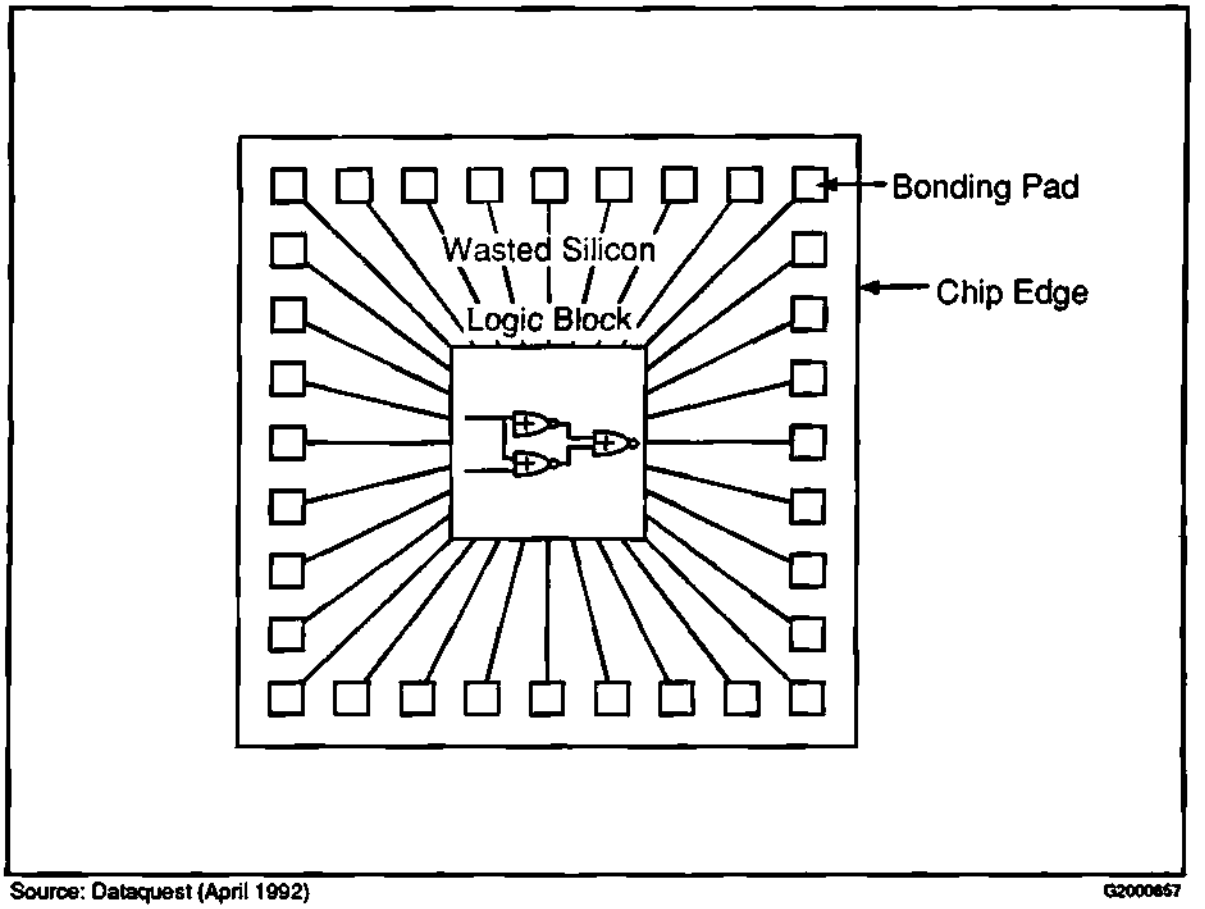
Memory chips have continued to get wider in spite of the increase in aspect ratio. This has led to a demand for a memory package that can accommodate a smaller space between the edge of the memory chip and the outer edge of the package pins.

Figure 5.1.3 shows some packaging techniques that decrease the chip to pin spacing. Conventional packaging is shown where the lead bonds are made from the edge of the the chip to the inner leads. The Chip On Lead (COL) technique does away with the die pad and runs the leads directly under the chip. This reduces chip to lead spacing by eliminating the space required by the conventional package between the die pad and the inner lead.

The Lead On Chip (LOC) approach puts the leads on top of the chip. Here, spacing is reduced again because all the space required for wire bonding is within the periphery of the chip rather than outside it. It is claimed that the LOC approach can lead to packages where the memory chip is 90% of the package area. This approach may also offer a lower impedance connection between the power supply and the chip, resulting in improved memory performance.

There is development work in stacked memories, both in packaged form and as MCM's. Stacked memories are possible because the I/O pin or pins and the address pins are normally wired in parallel. If one memory

Figure 5.1.4
Pad Limited Gate Array



Source: Dataquest (April 1992) G2000857

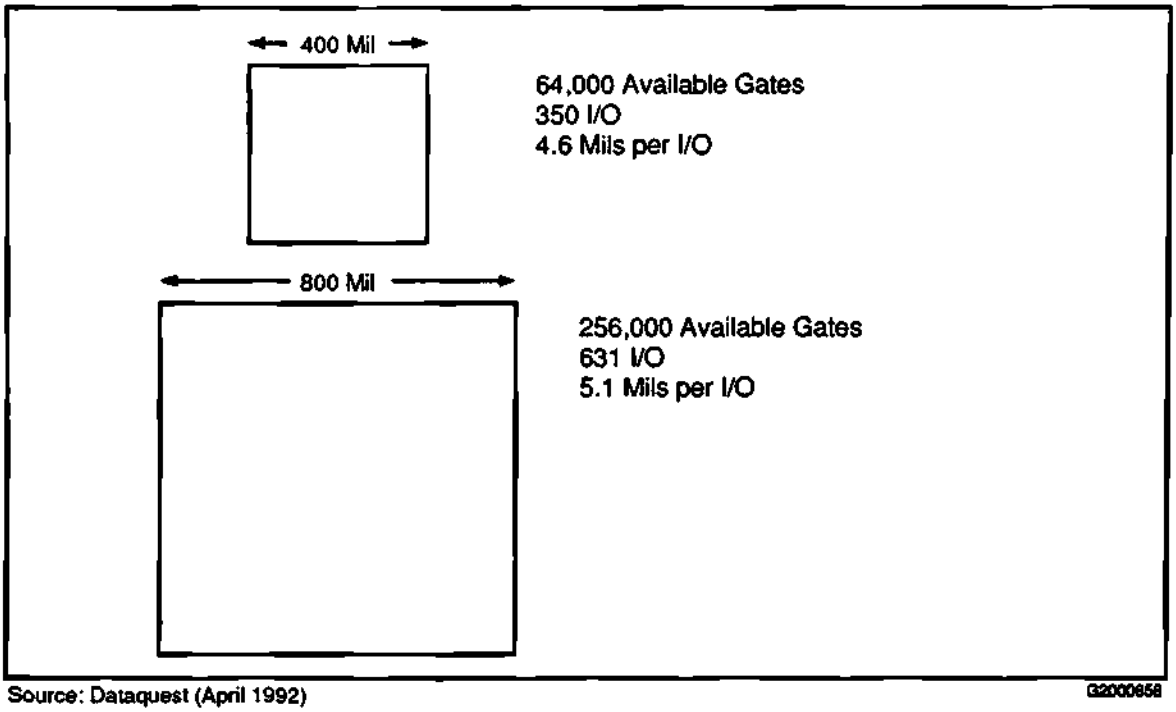
chip is placed on top of another, the address pins of one chip are directly above the address pins of another chip and it is easy to short them together.

The two high stack can be easily accomplished with surface mount technology. In this case, one memory chip is mounted on top of the board while the other is mounted on the bottom of the board. Both chips have the same side up, so the top chip must have its leads formed down to the board while the bottom chip has its leads formed up to the board. This approach requires that half the memory chips have their leads formed in one direction while the other half have their leads formed in the opposite direction. Very high packing densities can be achieved with this technique, rivaling what can be accomplished in an MCM.

Logic Packaging

Logic chips typically have many pins. Indeed, some logic chips are what we describe as pin limited. This situation is illustrated in Figure 5.1.4. Here, bonding pads have been placed at the minimum allowable spacing, but the situation is such that the chip area required to implement the logic is less than the area available within the outline of the peripheral bonding pads. As a result, much of the silicon is "wasted".

Figure 5.1.5
Chip Size Impact on Available I/O



Source: Dataquest (April 1992)

This wasted silicon contributes to the cost of the chip without providing any useful function. It is common for smaller gate arrays to be pin limited in this manner.

The number of bonding pads in Figure 5.1.4 could be increased by staggering the pads. In this technique, the pads are put in two rows with the second row of pads aligned with the space between the first row of pads. This allows an increase in density without breaking any layout rules. The density of pads is also a function of the attachment method – TAB pads can be more dense than wire bonded pads. TAB pads have been reported at 4 mil spacing as compared to a typical minimum of 6 mils for wire bonding.

Many smaller gate arrays are still pin limited, even when staggered pads or TAB frames are used. Larger gate arrays are less likely to be pin limited because the chip periphery increases more rapidly than the pin count as more logic gates are implemented.

Bonding pads perform the role of a "space transformer." That is, they provide the interface between the dense metal lines on the chip and the much less dense metal lines on the PCB or MCM substrate to which the chip will be attached. Today, the pitch of metal lines on the chip is typically 0.1 mils (2-3 microns) while the metal lines on an MCM may be spaced at 1 to 2 mils and the metal lines on a PCB may be spaced at 4 to 6 mils or more. In the PCB case, the bonding pads have to transform the pitch of metal lines by a factor of 20:1 while in the case of the PCB, the transformation is 60:1.

Some of this transformation may occur between the chip and the MCM or PCB substrate. For instance, if TAB is used to connect the chip to the substrate, the inner lead spacing may be 4 mils while the outer lead spacing may be 8 or 10 mils. In this case, the outer lead spacing is driven by a desire for repairability through soldering. If this requirement did not exist, the outer lead pitch could be the same as the inner lead pitch.

One way to avoid the pad limited situation is to put something on the gate array chip that takes up lots of silicon without requiring more pins. Memory is an ideal candidate for this role – it is common today to embed memory and other dense, low pin count functions in gate arrays. If the array is pad limited without the embedded function and it is not pad limited with the embedded function; then the embedded function is almost free.

New technology does not help a pad limited chip – it just makes matters worse. Suppose Figure 5.1.4 illustrates a gate array with 1 micron design rules. When design rules shrink to 0.8 microns, the area to implement the same logic decreases in proportion to the square of the design rule and only 64% as much logic block area is required. If the pad spacing remains the same, the only result is that more silicon is wasted.

The pad limitation for gate arrays improves somewhat for larger arrays. Figure 5.1.5 illustrates a 400 mil gate array that is scaled up to 800 mils. The larger chip should have roughly four times as many gates. If Rent's rule is applied, the 350 input/output connections assumed for the smaller chip increase to 631 connections for the larger chip. The amount of chip periphery per input/output accordingly increases from 4.6 mils to 5.1 mils.

Rent's rule has the form:

$$\text{Pins} = B(\text{Gates})^A$$

Here B and A are constants. Figure 5.1.5 assumes that the value of A is 0.4254. This value of A was developed by fitting a Rent's rule curve to pin out data from two different gate array families (see Figure 5.2.1). If a value of A of 0.5 had been used, the pin count would have been proportional to the square root of the number of gates and the larger gate array would have had the same periphery per input/output as the smaller gate array.

5.2 Chip Interconnect Density Trends

This section of the report develops the Rent's rule constants for both gate arrays and microprocessors by fitting a curve to pin count vs complexity data on gate arrays and microprocessors.

Pin count vs complexity is converted to pin count vs year by using a forecast of maximum microprocessor complexity for a given year. With suitable adjustments, this methodology provides a forecast of gate array pin count as well. This forecast predicts the pin counts that will be required for the most complex devices that will be sold in any given year.

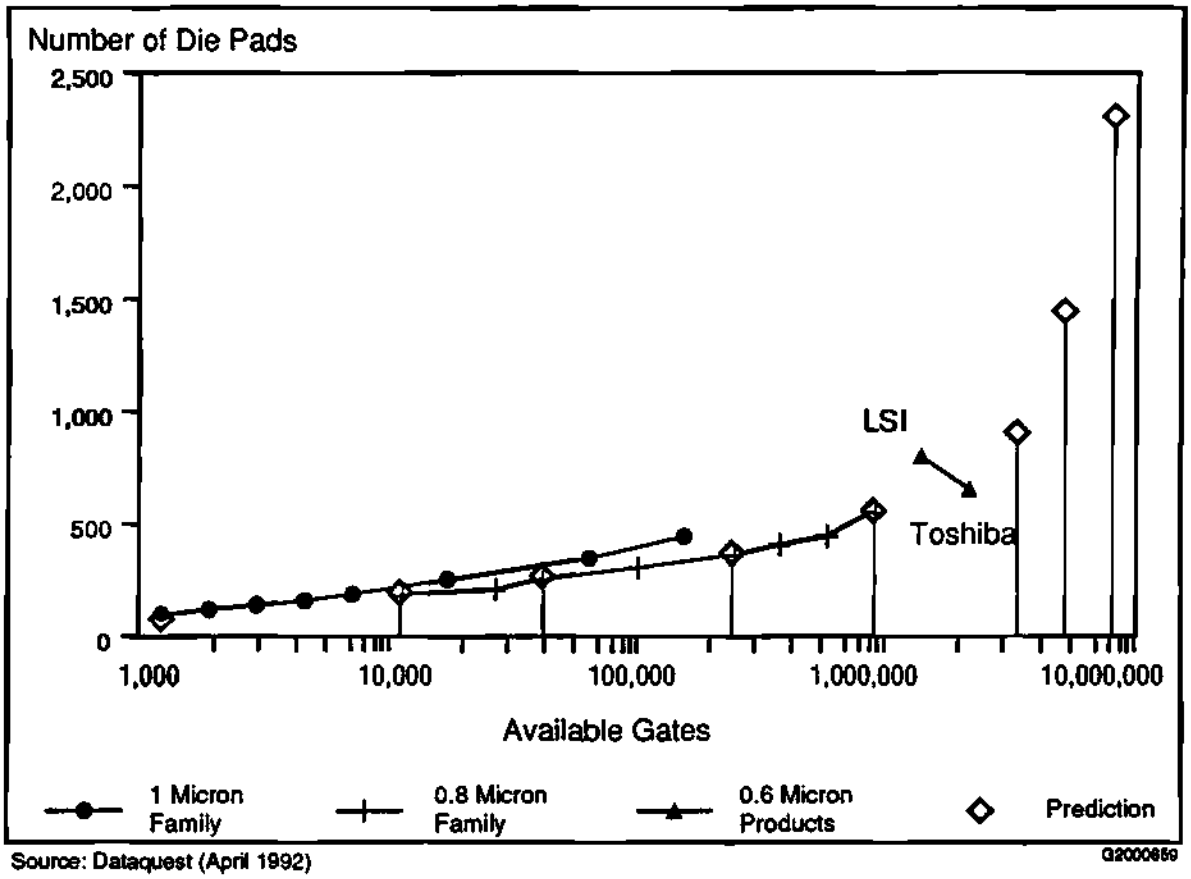
The next step is to forecast the pin counts that can be provided by VLSI chips that are not pad limited. This forecast is provided for both peripheral bonding pads and area bonding pads.

When required pin counts are compared to the pin counts that can be provided, it appears that peripheral connection to gate arrays (and to a lessor degree microprocessors) will not provide the required pin count. This dilemma can be solved by using area connections.

Gate Array Pincount

Figure 5.2.1 shows pin count data for two families of gate arrays: a 1 micron family and a 0.8 micron family. This data shows the highest pin count package provided by the vendor for various sized gate arrays as measured by the number of available gates. This is therefore the maximum number of available input/output pins – a given array may be put in a package with less pins, but no package with more pins is available.

Figure 5.2.1
Available Gate Array Pinout



Source: Dataquest (April 1992)

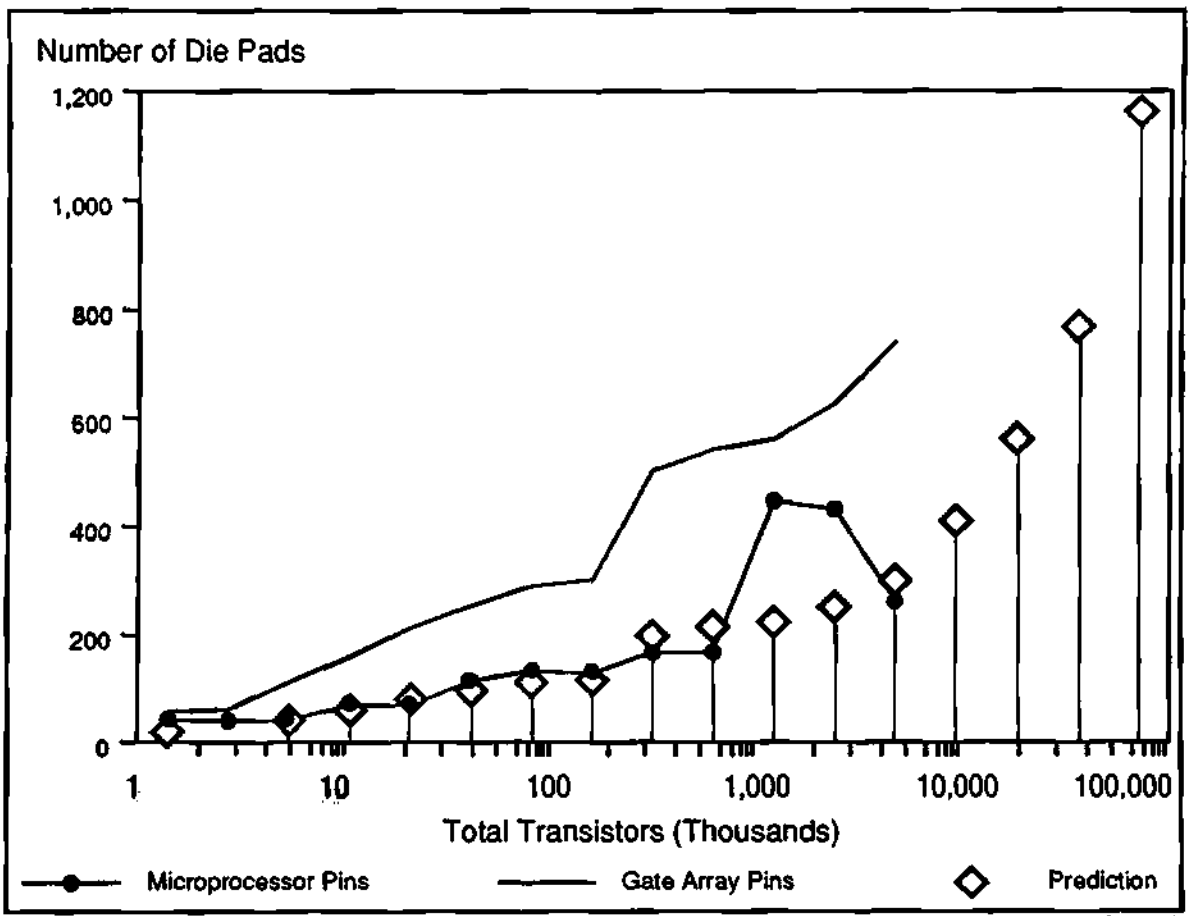
G2000659

The two 0.6 micron arrays are leading edge products announced recently. The 600,000 available gate array has a maximum pin count of 800+ (and is actually a 0.65 micron product) and the 800,000 available gate array has a maximum pin count of 652 (and is actually a 0.5 micron product).

The predicted data points are plotted using Rent's rule. In this case the constant A = 0.4254 and the constant B = 2.536. This curve fits the available data fairly well and forecasts that gate arrays will require more than 1000 pins when the available gate count is slightly in excess of 1 million gates. If each gate has four transistors, this corresponds to 4 million transistors.

For a complexity comparison, current microprocessors approach or exceed this transistor count; the Intel I860XP microprocessor has over 2 million transistors and it is anticipated that the Intel I80586 microprocessor will have more than 4 million transistors.

Figure 5.2.2
Microprocessor Pin Count



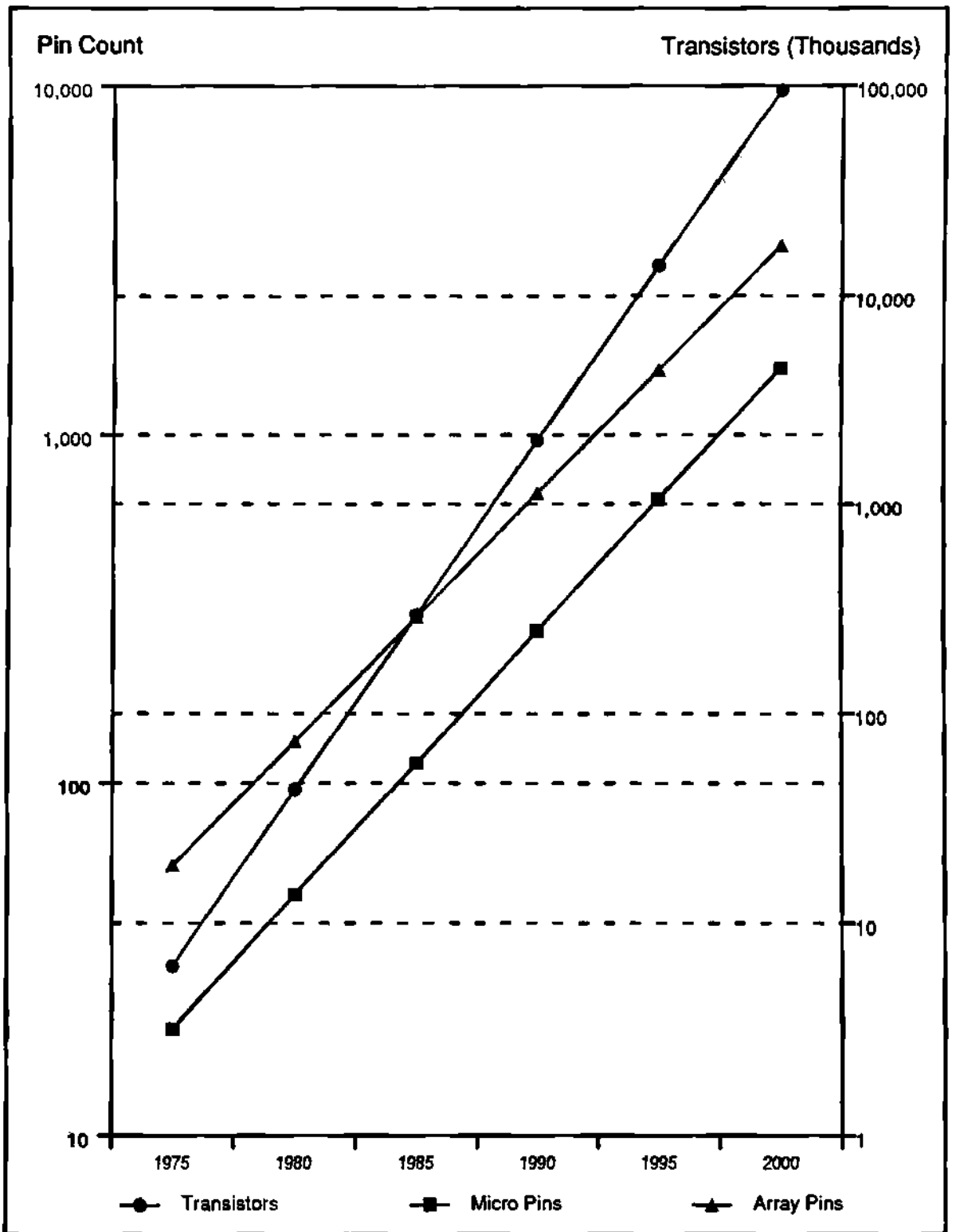
Source: Dataquest (April 1992)

Microprocessor Pin Count

Figure 5.2.2 shows microprocessor pin count. Here the trend line is not so regular and two different chips are plotted with more than 400 die pads, which is considerably above the forecast trend line. It is not unexpected that the microprocessor data is more variable since every part represented on the chart is a different design and possibly a different design philosophy. The gate arrays, by contrast, represent no design philosophy at all since the data shown is for arrays that have not as yet been interconnected.

Two microprocessors have over 400 die pads. These devices are 64 bit units. Possibly, the higher pin count can be ascribed to the fact that they have a 64 bit data buss rather than a data buss of 32 bits or less. However, the 400 pin units are at least 130 pins over the trend line. It seems unlikely that the extra 32 bits of data buss alone could account for this difference. Also, the other data in Figure 5.2.2 covers 8, 16, and 32 bit microprocessors and in these cases the extra word length does not cause a pin count anomaly.

Figure 5.2.3
Pin Count Forecast



Source: Dataquest (April 1992)

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Once again, predicted pin counts are developed using Rent's rule. In this case, the two 400+ pin data points are given relatively little weight. Rents rule in Figure 5.2.2 is of the form:

$$\text{Pins} = B(\text{transistors})^A$$

where A = 0.4521 and B = .3842. The constant B is a lot smaller because the formula relates to transistors rather than gates. The constant A is a little larger than in the gate array case. This indicates that microprocessor pin count should increase slightly faster with chip complexity than gate array pin count.

The gate array trend line of Figure 5.2.1 is also plotted in Figure 5.2.2. It assumes that each gate is four transistors. Notice that, for a given transistor count, gate arrays tend to have many more pins than microprocessors. This is probably because microprocessors have buss oriented architectures and may contain significant memory. Both these factors tend to reduce pin count.

Pin Count Forecast

Figure 5.2.3 plots the trend lines of figures 5.2.1 and 5.2.2 as a function of time rather than of transistor count. It assumes that in any given year, the most complex gate array will have about the same transistor count as the most complex microprocessor. This is borne out by today's situation – the recently announced 600,000 and 800,000 gate arrays have 2.4 and 3.2 million transistors respectively. By comparison, a 2.5 million transistor microprocessor is in production (I860XP), and a 4.5 million transistor microprocessor (I80586) is expected in the near future.

The trend line for microprocessor and gate array pin count vs year is developed by applying the Rent's rule formulae derived earlier to a curve of microprocessor transistor count vs year. This transistor count line indicates that the most complex microprocessor in the year 1975 had about 30,000 transistors and predicts that the most complex microprocessors of the year 2000 will have 100 million transistors.

Figure 5.2.3 indicates that in 1995 microprocessors will need packages which have 600 pins or more and gate arrays will need packages which have over 1,500 pins. In the year 2000 microprocessors will require over 1500 pins and gate arrays will require over 3,400 pins.

Pins Needed and Available

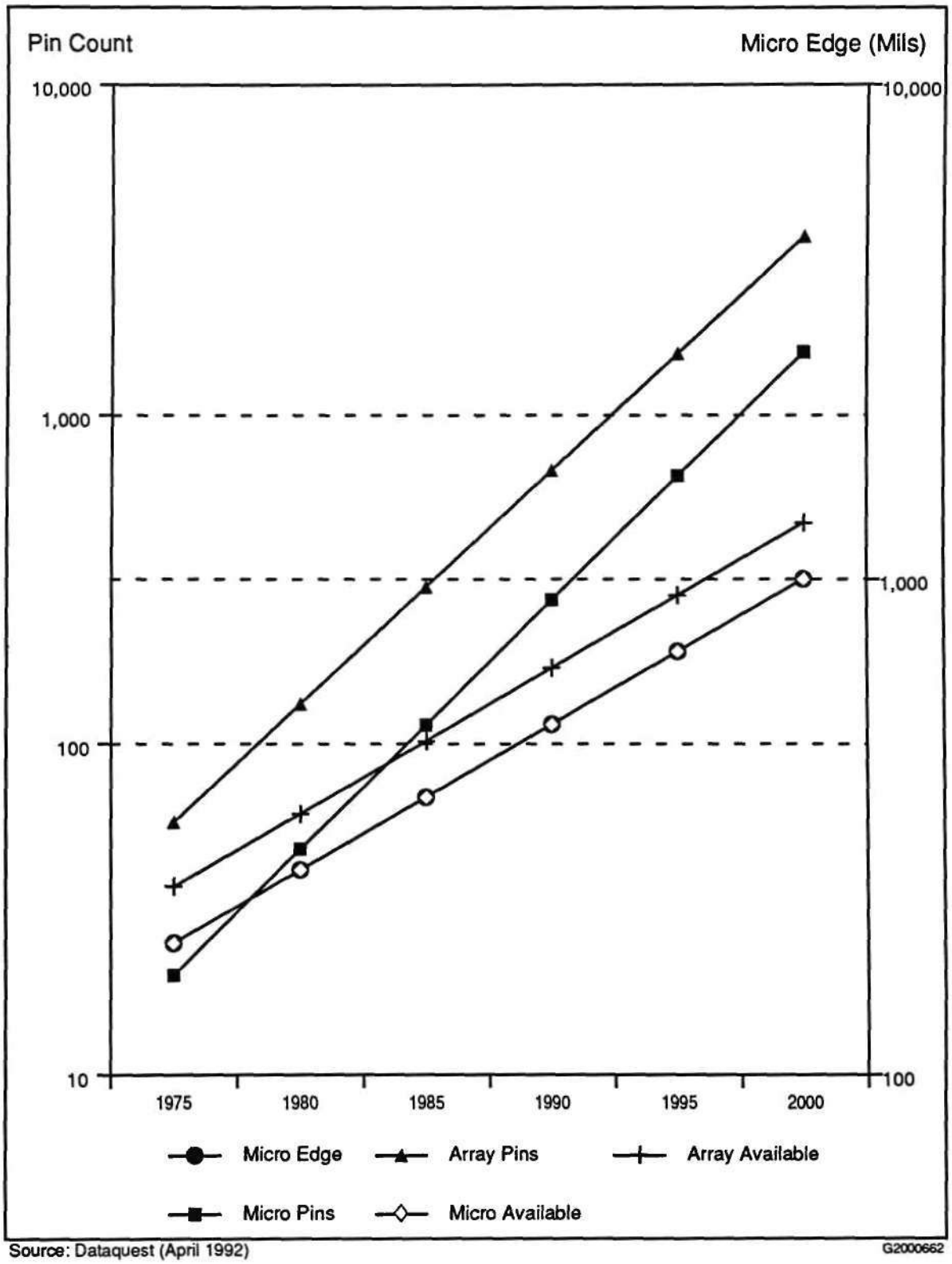
Now that a forecast of future required pin counts is available, it is interesting to compare these with an estimate of the pin counts that can be made available, taking into consideration expected packaging constraints.

Available pins are forecast for both peripheral bonding pads and area pads. These forecasts assume that the gate array or microprocessor chips are not pin limited – that is, the available pin out is computed assuming that the pins are fit onto the chip without any need to enlarge it to accommodate more pins.

The edge dimension of the most complex microprocessor available in any given year is shown in Figure 5.2.4. This edge dimension corresponds to the transistor counts of Figure 5.2.3. In the period of 1975 to 2000, the edge dimension of microprocessors increases from 184 mils on a side to 1000 mils (one inch on a side!).

An earlier assumption was that, in any given year, the most complex gate arrays have the same number of transistors as the most complex microprocessors. This is a good assumption, but this does not mean that gate arrays of equal transistor count can be built on the same size chip. As a matter of fact, a gate array will typically have an edge dimension that is 30% larger than the edge dimension of a microprocessor of the same transistor count. Because of this, gate array chips are able to accomodate more bonding pads than microprocessor chips of the same transistor count.

Figure 5.2.4
Pins Needed and Available
(4 mil Peripheral Pads)



Source: Dataquest (April 1992)

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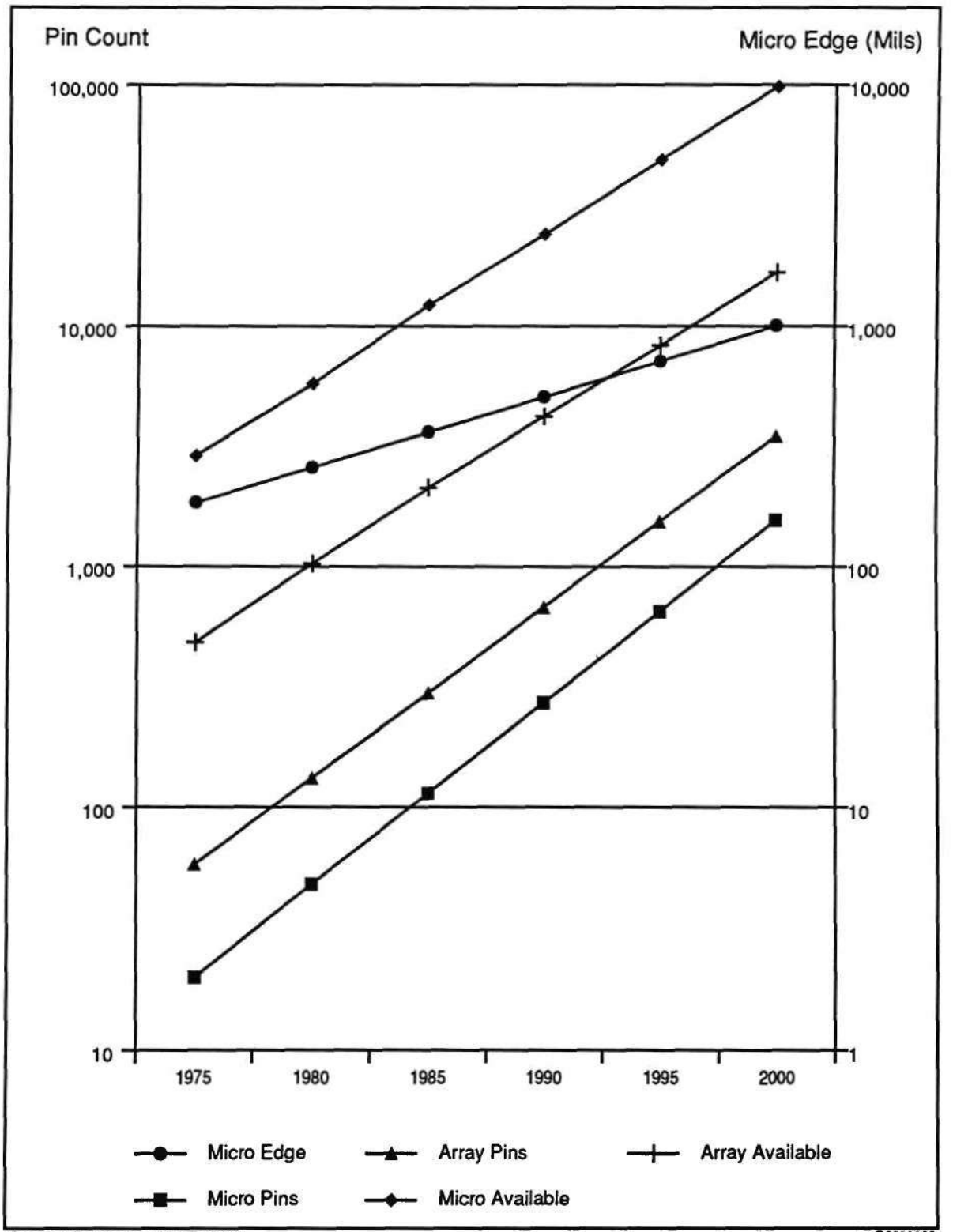
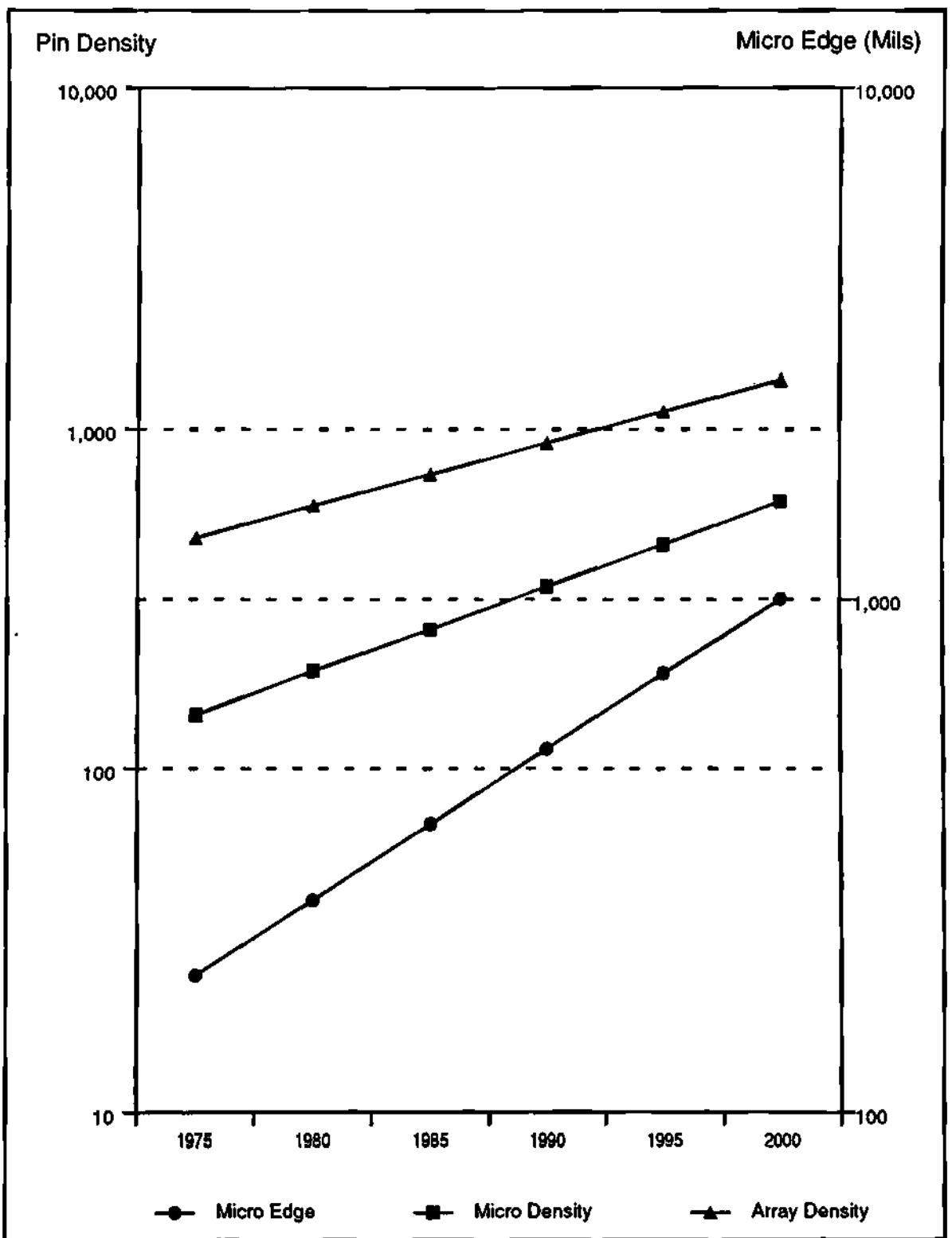
Figure 5.2.5
Pins Needed and Available
(10 mil Area Pads)



Source: Dataquest (April 1992)

G2000663

Figure 5.2.6
Pin Densities Needed
(Pins per Sq. In.)



Source: Dataquest (April 1992)

Figure 5.2.4 shows pads needed and available for chips with peripheral bonding pads on 4 mil centers. This figure indicates that the most complex gate arrays were already pad limited in 1990 and that microprocessors will become pad limited in 1996.

It is possible that the bonding pad spacing can be reduced below 4 mils. This will impact on the crossover dates in Figure 5.2.4. If pad spacing is reduced to 3 mils, the crossover dates are delayed by 2 to 3 years.

Figure 5.2.5 gives pins needed and available for 10 mil area pads. This 10 mil spacing is typical of the spacing that IBM uses in their controlled collapse solder ball flip chip process. This technology is well proven and has been in production for a number of years. As the figure shows, it should be able to provide more pads than are required by either gate arrays or microprocessors for the foreseeable future. The current maximum pad count at IBM is 729 pads. Most likely this upper limit is due to the fact that current chip complexities at IBM do not require a higher pad count.

The curves of Figure 5.2.5 assumes that chip circuitry can run under the solder bumps. This should be possible, but if it is not, the chip area will increase in proportion to the number of solder bumps required.

Technologies in development in Japan aim to put the flip chip connection pads on 10 micron centers (see Chapter 7.5). This pad spacing is twenty times less than is assumed in Figure 5.2.5 and would lead to 400 times as many pads as are illustrated in Figure 5.2.5.

It may appear that the Japanese are seeking to provide more interconnect capability than is required. This is not the case since the Japanese are working to provide signals to LED arrays and LCD panels. Both of these applications require pad densities well in excess of what is required for either gate arrays or microprocessors.

Pin Density

Figure 5.2.6 shows required pin densities. Here, the pin counts of Figure 5.2.5 are divided by the chip area to obtain a measure of pin density.

The required pin density increases slowly:

- 3.2% per year for microprocessors.
- 2.8% per year for gate arrays.

This slow increase in MCM pin density may indicate that the demand for more dense substrates will not increase rapidly.

It may seem odd that the required pin density does not increase more rapidly. Actually, the reason for the slow increase is that pin count increases slowly as transistor count increases; at the same time chip area is also increasing, so the area to place the pins also increases, causing a lowering of pin density.

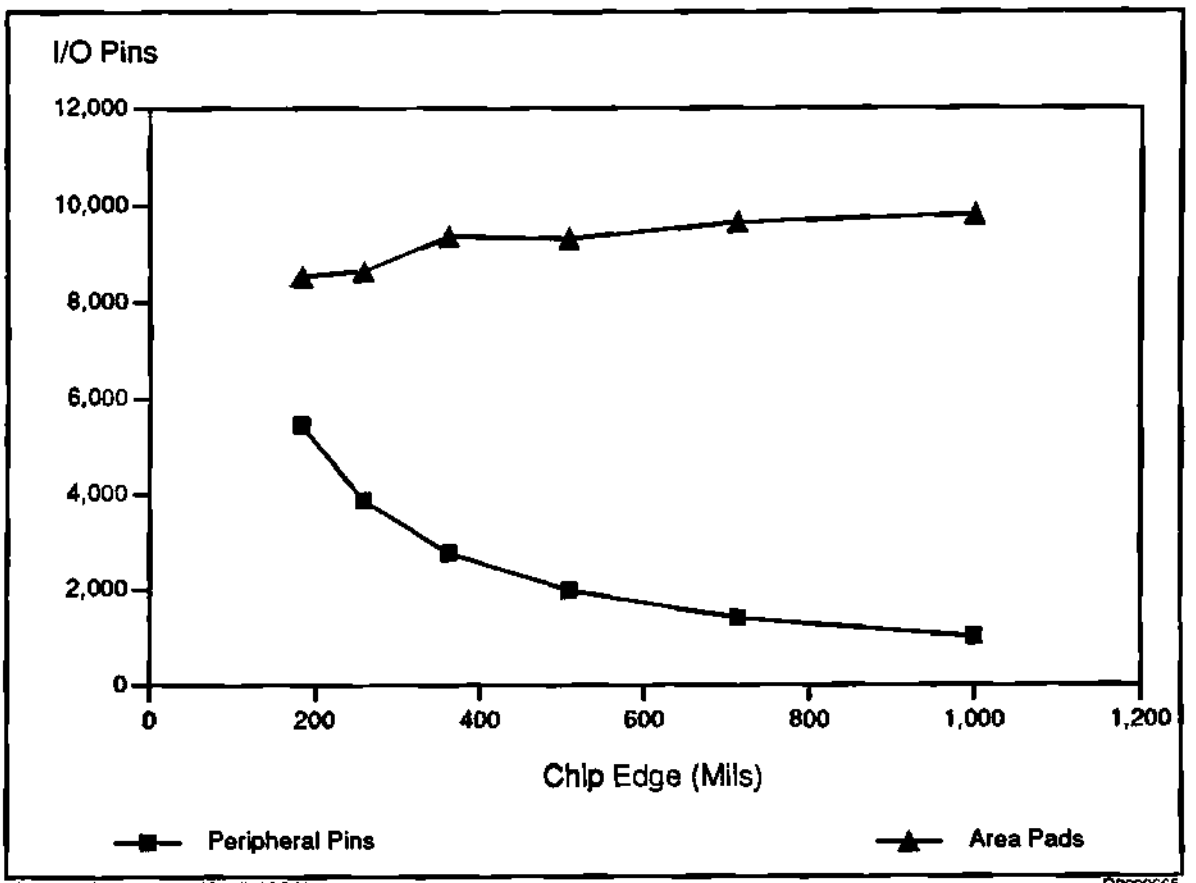
To do a numerical example, note that transistor count in microprocessors has been increasing at a rate of 44.5% per year. The required pin out will then increase at a rate governed by Rent's rule:

$$\text{Rate of pin out increase} = (1.445)^{0.4521} = 1.1811.$$

Chip edge dimensions are increasing at 7% per year, so the increase in chip area is the square of this increase:

$$\text{Rate of chip area increase} = (1.07)^2 = 1.1449.$$

Figure 5.2.7
Pin Density vs Die Size
(I/O Pins per Sq. In.)



Source: Dataquest (April 1992)

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The rate of increase of pin density is just the rate of pin out increase divided by the rate of chip area increase:

Pin density increase rate = 1.1811/1.1449 = 1.0316.

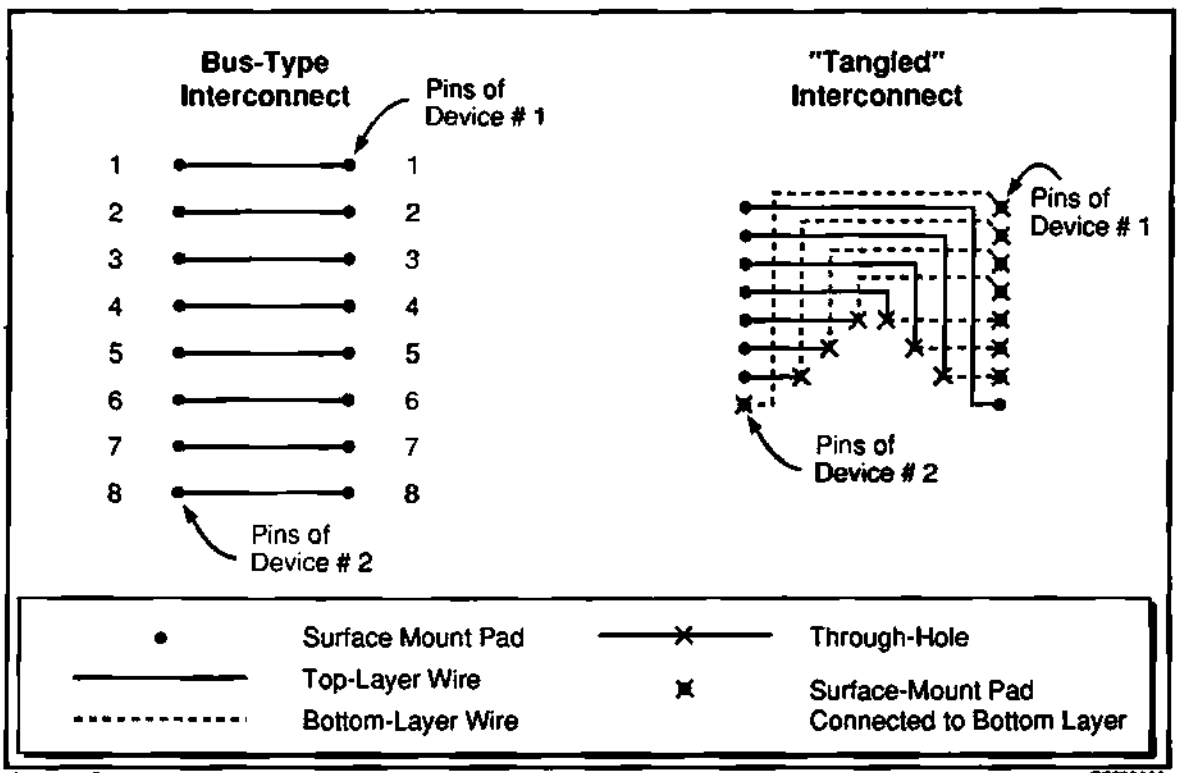
Pin density increase rate = 3.2% per year.

Figure 5.2.7 gives a graph of pin density vs die size for both peripheral pins (on 4 mil centers) and area pins (on 10 mil centers). Note that with peripheral pinning, pin density is much lower for large chips than it is for small chips. This underscores the advantage of area pads.

5.3 Comparison of Substrate Interconnect Capability and Chip Requirements

The claim of advanced substrate technologies used in MCM-D is that they provide denser wiring. There are many factors which determine whether this density is required in a given application. These factors can be:

Figure 5.3.1
Interconnect "Tangledness"



Source: Dataquest (April 1992)

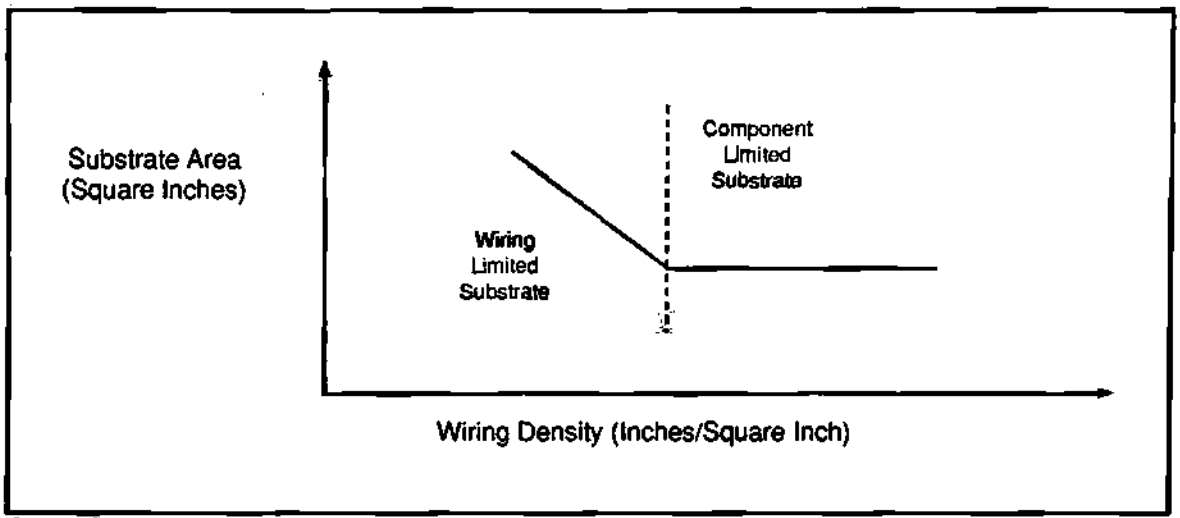
- Geometric – size, weight, volume.
- Electrical – signal delay, noise.
- Thermal – power, temperature rise.
- Cost.

The requirement for MCM-D depends in a complex way on the exact combination of these factors.

Different applications will also require different substrate wiring densities to interconnect components within the required area. The discussion of the previous section suggests that the percentage of applications that require MCM-D wiring densities to achieve minimum module size will not increase rapidly with time. Stated another way, many minimum sized modules will be built without resort to MCM-D.

The required substrate wiring density depends not only on the pin density of the VLSI components, but also on something that Dataquest calls wiring "tangledness." This concept is illustrated in Figure 5.3.1. This figure gives a simplified two dimensional illustration; for simplicity it shows only one row of pins for each VLSI device when most products have either two rows of pins arranged in parallel lines or four rows of pins arranged in a square.

Figure 5.3.2
Wiring and Component Limited Substrates



Source: Dataquest (April 1992) G2000667

The left part of the figure illustrates a "buss-type" connection. Here each pin of the first device is wired directly to the same pin of the second device. Clearly, for this structure, the two rows of pins can be placed as close together as the design rule for pin to pin spacing will allow.

The right part of Figure 5.3.1 shows a situation of maximum "tangledness." Here there is a total reversal of pin connections: pin 1 of the first device is connected to pin 8 of the second device; pin 2 of the first device is connected to pin 7 of the second device and so on.

The "tangled" interconnect requires wires on both the top and bottom of the PCB as well as one through hole for each wire to connect the top wiring with the bottom wiring. A second through hole is required at the device pin itself (for all but one pin) because the device is surface mounted and it is necessary to reconnect the bottom wire with the pin.

The layout for the "tangled" interconnect shows a requirement for eight wiring channels. These wiring channels will require much more interconnect area than is required in the "buss-type" case. In the "tangled" case, some substrate area could be saved if a denser interconnect technology were used.

In a real layout situation, the components themselves would take up substrate area even if they were all laid side to side. If the wiring is dense enough, it will always be possible to completely wire all components by only using the space beneath the components.

This situation is illustrated in Figure 5.3.2 which shows the way substrate area behaves as wiring density increases. At some wiring density, a point is reach where all the wiring is under the components and the substrate does not get any smaller even as the wiring density is increased further. Clearly, it makes no sense to employ a wiring density that is to the right of the dashed line in Figure 5.3.2.

Unfortunately, "tangledness" is a factor that is difficult to evaluate since it does not depend on the number of pins to be interconnected. Possibly, the only way to evaluate it is by making a computer layout of the actual wiring.

Table 5.3.1
Minimum Interconnect Density for
Component Limited Substrates*

Name	Approach	Minimum Interconnect Density (in./in.^{2}) SMT	MCM (Tab or Wire)	MCM (Flip Chip)
FDDI	Buss-Type	63	175	250
Complex RISC	Mixed	225	500	650
RISC	Tangled	500	3250	3750

*Wiring Density assumes that only 40% of the available interconnect wiring can be used due to non-optimum routing, floor planning and congestion.

Source: Dataquest, April, 1992

MCC has developed a software tool called SPEC that makes this analysis. In a recent paper, it was used to determine the area and density requirements for three different modules*:

- A three chip FDDI module that is heavily buss oriented.
- A complex RISC module that has two VLSI chips, 20 SRAMS and up to 48 discrete devices.
- A RISC processor that has four VLSI and two ASIC chips.

Table 5.3.1 shows the minimum interconnect density (in inches per square inch) for component limited substrates. These densities correspond to substrates that are at the wiring density indicated by the dashed line of Figure 5.3.2.

Three interconnect densities are listed for each module. The SMT density is for individual components mounted on a PCB and corresponds to the density where all the wiring is under the SMT devices. Similarly, the MCM (tab or wire), and MCM (flip chip) are for the case where all interconnect wiring is under these components. A somewhat higher wiring density is required for flip chip as compared to TAB or wire because of the fact that TAB or wire requires area outside the chip area for attachment to the substrate.

The FDDI module seems to be heavily buss oriented, so it requires the lowest wiring density. Even in the case of MCM flip chip, the required density is only 250 inches per square inch. This could easily be handled by a two layer PCB with traces on 8 mil centers. Presumably, memory modules consisting of DRAMs, SRAMs, or FLASH devices could easily be wired on a PCB of this wiring density.

The complex RISC requires somewhat denser wiring than the FDDI module, but a point of diminishing returns is soon reached, probably because of the large substrate area required by the discrete devices. In this case, the most dense application requires a wiring density of 650 inches per square inch. This wiring density requires either a multilayer PCB or ceramic substrate or an MCM-D substrate.

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*"Technology Application Tradeoff Studies in Multichip Systems," Peter Sandborn, MCC, Austin, Texas. Published by ISHM in the 1992 Proceedings of the International Conference on Multichip Modules

The six chip RISC must have a tangled interconnect, because a high wiring density is required. The densest requirement of 3750 inches per square inch could not be met by an MCM-D with a pitch of 25 microns (1 mil) if only two layers were used. Four signal layers of 1 mil pitch would be needed to meet this requirement; this is a denser interconnect than is standard with most MCM suppliers. The densest solution shown by MCC was 1016 inches per square inch. This solution must have been to the left of the dashed line in Figure 5.3.2. In spite of this it was the densest alternative shown.

MCC also computed cost (not including the cost of the chips), size, and the package time of flight delay for each module, as summarized below:

- For the FDDI application the lowest cost solution is with a PCB interconnect, the lowest delay is thin film and the smallest substrate is thin film. The size of the PCB was limited by via spacing and not by wiring density.
- For the complex RISC application the lowest cost solution is with individually packaged devices using SMT mounting, the lowest delay is with thin film interconnect and the smallest size is also with thin film interconnect.
- For the RISC processor the lowest cost, least delay, and smallest size are all achieved with thin film interconnect.

Chapter 6 — Substrates for Multi-Chip Modules

This chapter focuses on substrates. Here, the substrate is defined to be the completed interconnecting device. As such it consists of the wiring that interconnects the chips together with a means of mechanically supporting that wiring and a means of dissipating the heat generated by the chips.

The next chapter, Chapter 7 deals with the completed MCM. The data from Chapter 6 serves as an input to Chapter 7.

6.1 Introduction

This chapter develops patterned substrate costs and deals with the pros and cons of the various available substrate options. Dataquest classifies MCM's by technology: hybrid, ceramic cofired (MCM-C), laminate (MCM-L), and high density (MCM-D). Within each of these classes, there are a number of substrate possibilities and this chapter deals with the more popular ones.

This chapter does not discuss hybrid circuits in detail. It is Dataquest's opinion that hybrid technology is reasonably mature and not subject to the rapid evolution that other substrate technologies are experiencing. Here, a hybrid circuit is defined as one using separately fired substrates and pastes. Of course, nothing prevents a hybrid manufacturer from making an MCM using cofired, laminate or high density techniques. These circuits would simply be classified under one of the other three MCM categories. It may well be that hybrid manufacturers will be able to transfer their skills in handling and testing bare die and unencapsulated modules to segments of the MCM market outside the hybrid segment

Dataquest has chosen its MCM classifications in the belief that each category of MCM is attempting to "Piggyback" on a mature production technology. Each of the major technologies has been in production for a number of years. Cofired ceramic technology has been used since the late 1960's to build both individual packages and MCM's (mostly at IBM). Laminate technology has been used mainly in printed circuit boards to interconnect packaged devices. High density interconnect technology is an outgrowth of the semiconductor industry. In the past, this technology has been used to interconnect the transistors within a VLSI circuit; it is now being adapted to interconnect multiple chips.

Though each class of MCM is evolving from a mature production technology, none of the current technologies are perfectly tailored to the needs of the current and future MCM market. Relative market share among these technologies will be determined by which is most suitable and which can adapt to changing needs most readily.

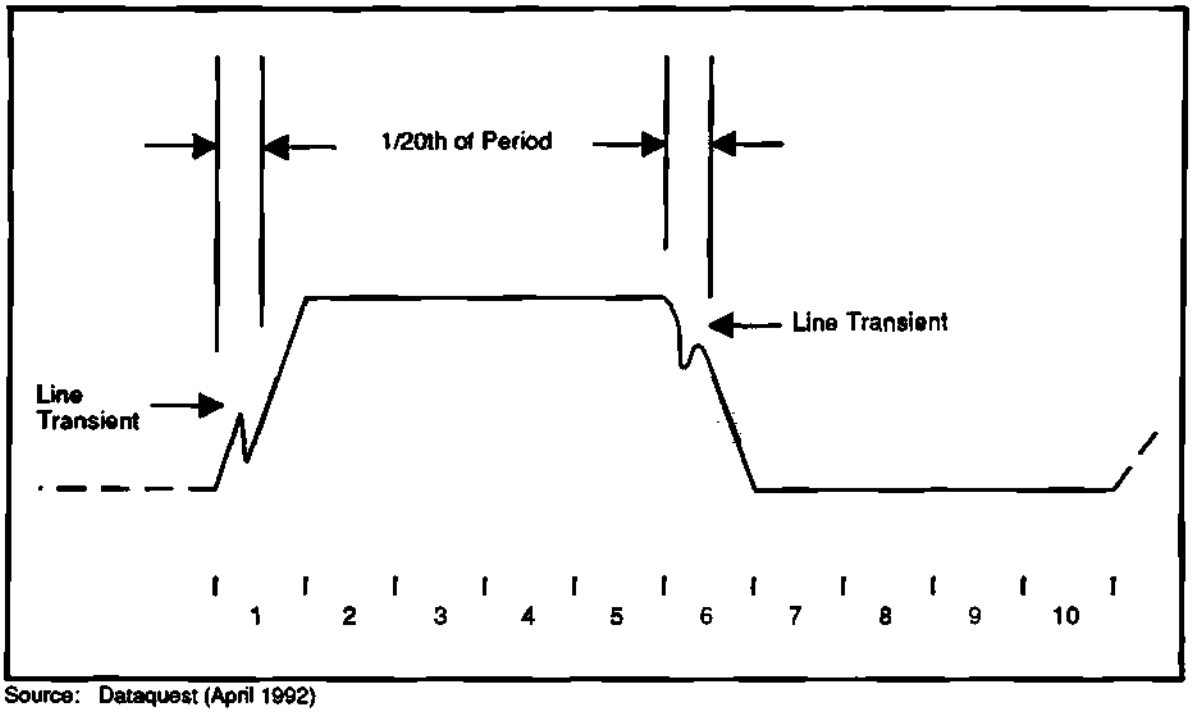
The classes of MCM-C and MCM-L are named for the substrate used in manufacture of MCM's. By contrast, the class of MCM-D is so named because it offers high density interconnect. In an MCM-D, the functions of interconnect wiring and mechanical support are somewhat separated. A silicon substrate provides interconnect wiring, but it is so fragile it must be mounted on a more mechanically robust substrate; popular choices include ceramics and various metals such as copper and aluminum. In a similar way, wiring implemented in copper and polyimide can be mounted on an array of different substrates which provide the functions of mechanical protection and power dissipation.

6.2 Substrate Pros and Cons

This section discusses maximum clock rate, which is related to insulator dielectric constant. It considers the problems of simultaneous switching noise and thermal fatigue. It also summarizes the discussion of

Figure 6.2.1

Waveform Illustrating Maximum Clock Rate For Which Transmission Line Effects Can Be Ignored



Source: Dataquest (April 1992)

later sections which deal with substrate interconnect density, cost, chip power requirements and MCM power handling capability.

Maximum Clock Rate

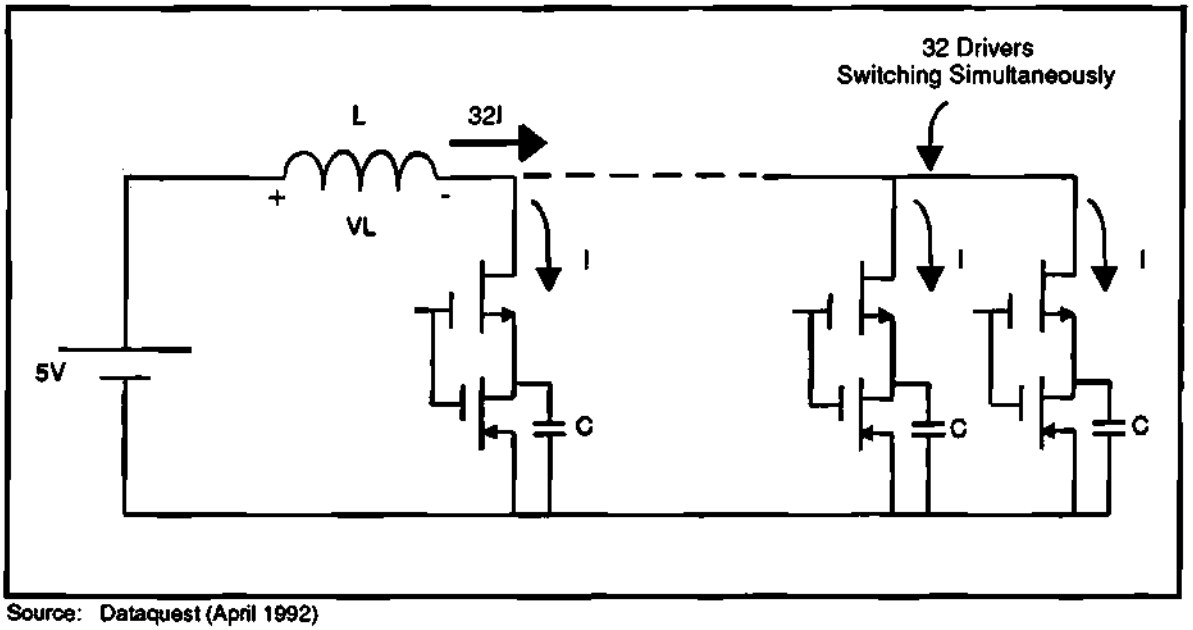
The velocity of light in a vacuum is 30 centimeters per nanosecond. In other media, the velocity is inversely proportional to the square root of the relative dielectric constant (which is the dielectric constant of the material in question divided by the dielectric constant in vacuum).

Electrical signals, like light, are electromagnetic waves, and they follow the same rules as light. Electrical signals typically travel down a wire or transmission line, and the velocity at which these signals travel is determined by the dielectric constant of the material around the wire. In many materials, signals travel at one half to one sixth the speed of light in a vacuum. For a relative dielectric constant of four, this means the electrical signal will travel 15 centimeters or approximately 6 inches in a nanosecond.

When an electrical signal reaches the end of a transmission line that is not terminated, there is a reflection which causes the signal to be distorted. This situation is illustrated in Figure 6.2.1 which illustrates the case in which the clock period is 20 times as long as the time for the signal to travel from one end of the transmission line to the other. This waveform is viewed at the receiving end and is for the case in which the transmission line does not have significant series resistance.

As a rule of thumb, it is possible to largely ignore transmission line effects when the situation of Figure 6.2.2 prevails. If transmission lines cannot be terminated in their characteristic impedance, the situation of Figure 6.2.2 normally prevails.

Figure 6.2.2
Simultaneous Switching Noise



Source: Dataquest (April 1992)

It is particularly difficult to terminate transmission lines in CMOS circuits. CMOS circuits have a 5 volt swing and terminating resistors are usually about 50 ohms. This means that an output driver would dissipate half a watt in its terminating resistor when it is on. If a chip has 100 outputs, each of which is on half the time, 25 watts would be dissipated in the terminating resistors which would normally be fabricated on the MCM substrate.

Table 6.2.1 gives maximum clock rates at which transmission line effects can be ignored. The following comments on this table are pertinent:

- The transmission line is two inches long. This corresponds to the longest line on a 1 inch by 1 inch substrate.
- Line delay is equal to 1/20th of the clock period.
- Many materials support frequencies well over 100 MHz.
- Glass-Ceramic is the material of choice among the cofired ceramic materials.
- FR-4 and Teflon both offer good performance among laminates.
- All of the high density dielectric materials offer good performance.
- Large monolithic chips may have even slower clock rates than indicated here beacuse of the long RC time constant of the interconnect.
- Note that a high dielectric constant is desirable for the power and ground interconnect layers. It increases the capacitance between these layers and damps out unwanted transients. This is why some MCM manufacturers interconnect the power and ground in cofired ceramic and interconnect signal wires using high density interconnect.

Table 6.2.1
Maximum Clock Rates At Which
Transmission Line Effects Can Be Ignored

MCM Category	Dielectric Material	Maximum Clock Rate* (MHz)	Relative Dielectric Constant
Ceramic Cofired	Alumina	96	9.4
	Glass-Ceramic	126-129	5.2-5.5
	Aluminum Nitride	99	8.8
	Silicon Carbide	46	42.0
Laminate	Fr-4	136	4.7
	Teflon	199	2.2
High Density	Silicon Dioxide	149	3.9
	Polyimide	170-158	3-3.5
	Benzocyclobutene	183	2.6
----	Vacuum	295	1.0

*Assumes that module delay is less than 1/20th of the clock period. Transmission line is two inches long.

Source: Microelectronics Packaging Handbook
Dataquest, April 1992

Simultaneous Switching Noise

Simultaneous switching noise is another problem that limits clock rate. The situation is illustrated in Figure 6.2.2. Here 32 output drivers are switching simultaneously into a capacitive load. There is an inductance L in the power supply line between the supply and the output drivers. The following comments are important:

- At a clock frequency of 50 MHz and a capacitive load of 100 picofarads, the current in each driver will rise at 100 milliamperes per nanosecond.
- The current transient in the common inductance is roughly 3200 milliamperes per nanosecond.
- If the inductive voltage must be kept below a quarter of a volt, the maximum common inductance is .08 nanohenries.
- A typical bonding wire is about 2 nanohenries. It would take about 25 bonding wires in parallel to achieve this value. This explains why many chips have multiple bonding wires for power and ground.
- In the case illustrated here, at least one bonding wire would have to be added each time an output is added, depending on the desired frequency of operation.
- Loading is reduced for output drivers that go to only another chip within the same MCM. In this case the capacitance is likely to be much less than 100 picofarads.

Thermal Fatigue

Silicon substrates are too fragile to use directly as a packaging material and need a rigid mounting material to provide mechanical stability. If the mounting material has a coefficient of linear expansion that does not match that of silicon, cracking of the silicon can result, and the substrate becomes inoperative. In Japan, aluminum nitride is a favored mounting material because its coefficient of linear thermal expansion is close to that of silicon.

In North America, MCM manufacturers tend to use mounting materials that have a poor thermal coefficient match and instead prefer to solve the problem by attaching the silicon to its substrate with a compliant (rubbery or stretchy) material that allows the silicon to expand at a rate different than the substrate.

The situation is aggravated in the case of flip chip. If controlled collapse reflow solder balls are used, the attachment between the chip and the substrate is rigid and the solder ball is more likely to crack. IBM has flipped chips onto alumina for many years, but it is believed that a half inch chip is the maximum that can be tolerated in this situation. Significantly, The IBM RISC 6000 uses a silicon substrate and interconnects the individual chip using controlled collapse reflow solder. Clearly, the thermal expansion of the substrate matches that of the chips since both are silicon. In this case thermal expansion considerations limit neither the chip nor the substrate size.

Other flip-chip technologies exist. The BIP process of Raychem's APS division uses wire bonding to provide a short lead at each bonding pad on the chip. These leads are then soldered to the substrate. Since the leads can bend as the chip expands, the cracking problem is eliminated.

Another technique uses gold balls on the chips which are held in contact with the substrate pads by an organic compound that maintains contact pressure through shrinkage of the compound. In this technique, the balls can slide back and forth as the chip and substrate expand at different rates and continuity is theoretically maintained without cracking of either the die or the wafer.

Toshiba reports cracking of silicon substrates on alumina after less than 100 thermal cycles (-55° C to 125° C).[1] If the silicon substrate is mounted on aluminum nitride, more than 2000 cycles can be tolerated.

As indicated earlier, cracking problems become more severe as the thermal coefficient mismatch becomes greater. For illustration, some mismatch coefficients are illustrated below:

silicon on silicon	no mismatch
silicon on ALN	1.1 x 10-6 per degree C
silicon on alumina	3.6 x 10-6 per degree C
silicon on copper	13.5 x 10-6 per degree C
silicon on FR4	12.5 X 10-6 per degree C

North American firms claim to have successfully mounted silicon substrates on copper and FR4, both of which have a high thermal coefficient mismatch with silicon. This is accomplished with a compliant die attach material. Japanese suppliers use a more rigid die attach and prefer to work with aluminum nitride. A disadvantage of the North American approach may be that the die attach materials used exhibit a higher thermal resistance.

In summary, silicon substrates need to be be mounted on a more rigid packaging material. Many different materials may be used if the mounting is compliant enough. Rigid mounting, however, will tend to favor ALN or some other material offering a good thermal match such as a copper invar copper sandwich. If chip power dissipation is high, the thermal performance of the die attach material is important.

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[1] *A Silicon-Based Multichip Module with Co-Fired Aluminum Nitride Package*, Sudo et al, IEIEC Transactions Vol. E74 No. 8, August,1991

Table 6.2.2
Lithography Tool Resolution Requirements for
Printed Circuit Boards, Cofired Ceramic, and High Density Substrates

Substrate	Substrate Size	Line Pitch	Lines/ Substrate
P.C.B.	18" x 24"	4 mils	6000
Cofired	8" x 8"	8 mils	1000
High Density	6"(round)	1 mil	6000
LCD Panel	12" x 16"	0.1 mil	160,000

Source: Dataquest, April 1992

Flip-chip using controlled collapse solder balls will require a good thermal match between the chip and the substrate. Silicon substrates will offer the optimum thermal match to silicon chips.

Substrate Interconnect Density

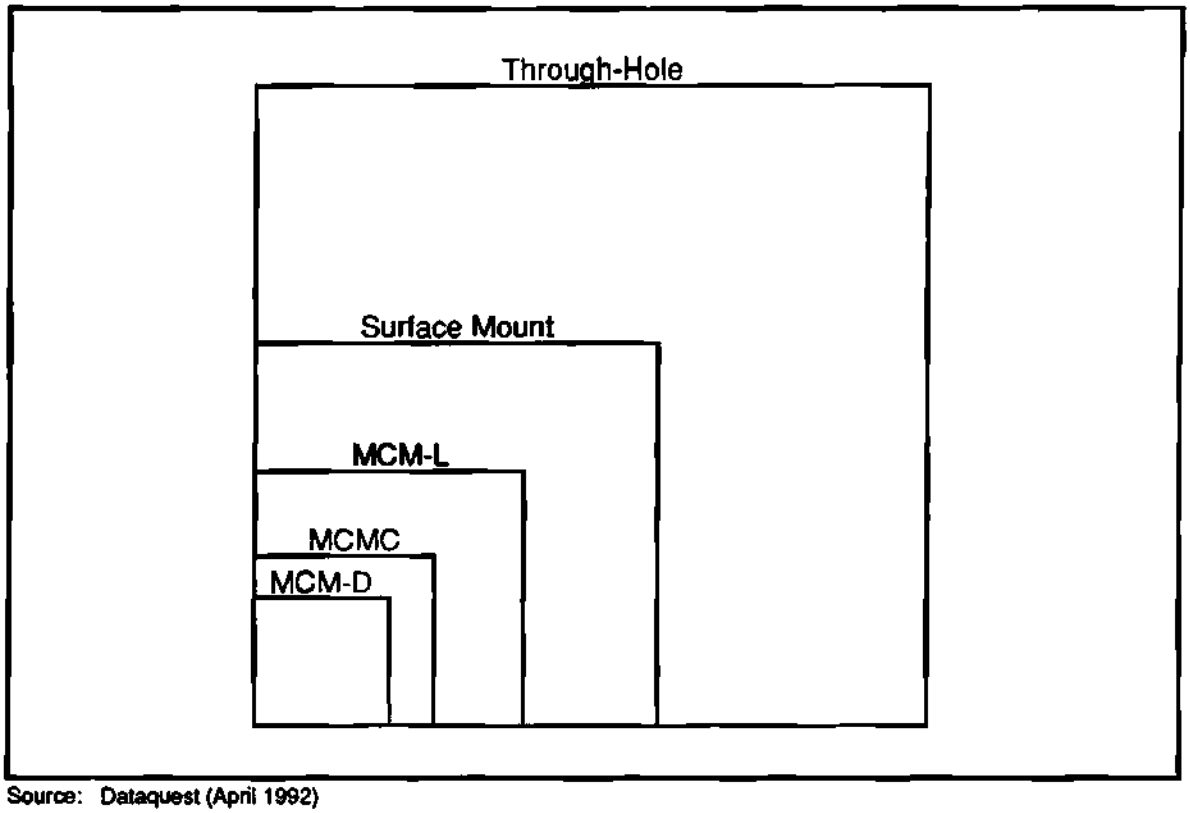
Denser interconnect wires are better than less dense wires. Dense wires make the interconnect substrate more compact and they allow the chips to be placed closer together so that they can run at a higher frequency. Thus, denser interconnect leads to size reduction and performance improvement, both of which are valuable in certain applications.

Since denser interconnect leads to size reduction, it also makes it possible to build MCM substrates which use less raw material. Dataquest believes that approaches that use less raw material have the possibility of becoming the lowest cost alternatives.

Interconnection density is determined by the lithography tool used in substrate manufacture. In turn, the productivity of the tool depends on the number of lines imaged on one substrate. Table 6.2.2 compares the number of lines imaged in the manufacture of typical MCM substrates:

- The column "substrate size" indicates the largest substrate commonly imaged.
- A single substrate may contain many individual MCM substrates.
- The number of lines per substrate increases as the number of lines increases and the pitch decreases.
- Substrates with the highest number of lines are likely to be the least expensive to manufacture per line.
- Cofired substrates have the least lines per substrate.
- PCB's and High Density substrates are comparable.
- LCD panels offer a line per substrate count almost three times that of any other technology. LCD manufacturing equipment may offer significant MCM substrate cost savings.

Figure 6.2.3
Size Comparison of Five Different Substrate Alternatives



Source: Dataquest (April 1992)

Figure 6.2.3 offers a graphic example of the size savings that occur as the line density is increased. This figure compares the area required by the same 5 chip set packaged using the different technologies. The assumptions for each technology are as follows:

- Through-hole: 12 mil line pitch, four layers.
- Surface mount: 10 mil line pitch, 6 layers.
- MCM-L: 6 mil line pitch, 6 layers.
- MCM-C: 10 mil line pitch, 20 layers.
- MCM-D: 1.5 mil line pitch, 4 layers.

The surface mount, MCM-L, and MCM-D areas in Figure 6.2.3 were obtained from actual layouts. The rest of the areas were estimated using industry thumb rules. The five chip set consists of a RISC CPU, an FPU (Floating Point Unit), an ASIC chip and two cache SRAMs. The chips have 670 pins all together and the module offers 256 connections to the outside world.

Table 6.2.3
Comparison of Substrate Costs for
Four Different Alternatives

Alternative	PCB/SMT	MCM-L	MCM-C	MCM-D
No. of Layers	6	6	20	4
Substrate Size:	10.5 sq. in.	5.25 sq. in.	2.00 sq. in.	1.08 sq. in.
Substrate Price	$.65/sq.in.	$2.00/sq. in.	$.70/sq.in./layer	$30/sq in.
Substrate cost	$6.53	$10.50	$28	$32

Source: Dataquest, April 1992

Cost

Table 6.2.3 takes the area of the substrates illustrated in Figure 6.2.3 and converts it to cost using current market costs per square inch. The following comments apply:

- Although the cost per square inch is higher for the more advanced technologies, cost per substrate increases less rapidly because these technologies require less substrate area.
- Printed circuit board technologies, both SMT and MCM-L, offer the most competitive substrate cost.
- MCM-C and MCM-D are roughly comparable in cost.
- MCM-D prices are believed to be in the range of $20 to $60 per square inch. Prices should firm as production volumes increase.
- Dataquest believes that MCM-D prices will decrease substantially as market volume grows, reaching $11 per square inch or less (See sections 6.4 and 6.5 for further discussion).

Chip Power Requirements

Chip power requirements tend to increase as VLSI chips become more complex. The concern is that chip power will increase to such an extent that systems can no longer be built economically.

Dataquest extrapolates chip power requirements in section 6.6. The results are as follows:

- Current memory (DRAM and SRAM) power requirements are in the range of .3 to .6 watts.
- Current CMOS microprocessor power requirements are in the range of 2.5 to 25 watts.
- If nothing changes, CMOS microprocessors of 1995 will require 10 to 100 watts and microprocessors of 2000 will typically require 290 watts.
- ECL chips require 10 to 15 times as much power as CMOS chips of the same gate count.

Dataquest believes that semiconductor engineers will find ways to develop lower power chips in order to avoid excessive packaging costs. Some likely occurrences are:

- Output capacitive loads will be reduced in MCM modules. Power savings of 20% to 30% are likely.

- Power supply voltages will be reduced from the current 5 volts to 3 volts or less. Power savings of 50% to 60% are possible.
- Engineers will design their logic in such a way that switching power is minimized by minimizing the number of nodes that switch in any clock cycle (In CMOS, only nodes that switch from a binary 1 to a binary 0 (or vice versa) dissipate power).
- Dataquest estimates that these techniques will be able to reduce CMOS chip power to 33% of the extrapolated 290 watts that would otherwise be required in 2000.

Dataquest believes that CMOS designers will be able to trade power for clock rate and that they will scale chip power to avoid packaging requirements that are exorbitant in cost.

ECL chips are a different matter. Already, power requirements of 15 to 40 watts are common. The cost to package and cool these chips leads to costs per gate that are 10 times as high as CMOS. Since more chips are required for a given application and the packing density of chips is power limited, clock rates begin to be limited by the physical size of the module. For this reason, ECL tends to be limited to only relatively specialized applications.

Many sophisticated packaging techniques have been developed to handle ECL power. If needed, these techniques or some modification of them can be used to handle CMOS power requirements if and when these requirements approach those of today's ECL chips.

MCM Power Handling Capability

CMOS microprocessor power requirements increase in proportion to CMOS chip area and chip complexity (See discussion of section 6.6). The trend line of section 6.6 indicates that chip power increases by a factor of 7.2 to 1 every time chip complexity increases 10 times. Dataquest estimates that CMOS power density for most CMOS microprocessor chips should be in the range of 12 to 45 watts per sq. cm. in the year 2000.

Can this power be handled by today's packaging technology? Certainly it can – the DEC Alpha chip is an existance proof. It dissipates 20 to 30 watts and the chip has a power density of 10.7 watts per sq. cm., close to the bottom end of the forecast power density for the year 2000. However, this packaging has the problem that chip density (the ratio of chip area to board area) is low. If it were necessary to package chips of this type with 50% of the packaging area occupied by the chips, power densities in the year 2000 would be in the range of 6 to 22.5 watts.

Section 6.6 gives power densities for several ECL systems, including the IBM thermal conduction module. These systems handle power densities in the range of 0.9 to 3.7 watts/sq. cm., considerably less than the year 2000 requirements above. One experimental system, however, does handle power densities of 790 watts per sq. cm. Although this technique is experimental, it offers hope that thermal problems can be solved.

Certainly, solutions to the CMOS packaging problems of ten years from now exist today, though they do not necessarily provide high packing density at low cost. Dataquest believes that better packaging solutions will be found as they become necessary.

Dataquest believes that chip designers can reduce chip power through design to almost any level that the packaging technology can handle. However the market will seek the highest performance available without undue increase in cost. Thus, chip designers will opt for higher power if economical thermal management systems can be developed.

Table 6.3.1
Typical Minimum Line Pitches of
Printed Circuit Boards, Cofired Ceramic, and
High Density Substrates
(Dimensions in mils)

	1970	1975	1980	1985	1990	Est 1995	Annual Change
PCB	15	10	10	8	6	4	-5%
Cofired	15	15	14	10	8	8	-3%
High Density	–	–	–	–	1-2	1-2	–

Source: Microelectronics Packaging Handbook
Dataquest, April, 1992

6.3 Interconnect Density

High interconnect density is good: it leads to higher frequency performance and significant size reduction of electronic equipment. The key economic issue is to make as much interconnect as possible each time the substrate is imaged. For this reason, imaging technology (or photolithography) is key to the usefulness of the technology.

This section reviews historical trends in interconnect density for printed circuit boards, cofired ceramic substrates and high density interconnect.

The manufacture of printed circuit boards usually starts with an epoxy fiberglass material (FR4, typically) which has been laminated with copper. The copper is covered with photoresist, usually a dry film resist, and the appropriate pattern is exposed using an image (or mask) of the circuitry that has been printed on a large sheet of flexible plastic material. The photoresist is removed (or developed) in areas defined by the mask. A subsequent etching step removes any unwanted copper and leaves the desired wiring pattern. The remaining photoresist is then washed away. This process is called photolithography.

A layer of laminate is etched for each layer of circuitry that is desired in the final printed circuit board. These layers are then stacked and laminated in a high pressure press that squeezes them together. Layer to layer connections or vias are then made by drilling holes through all the layers and plating the sides of the holes to that connection is made to the copper traces on the different layers of the board.

Most PCB vias go all the way through the board whether there is a connection to be made at all levels or not. Holes all the way through the board are certainly required in those cases where the lead of a component is to be inserted through the board. It is possible to make vias that do not go all the way through the board as well but in this case the drilling and layer to layer connection occurs before the lamination is completed.

The fabrication of cofired ceramic modules is similar to PCB fabrication except that the starting material is a green or unfired ceramic. Unlike the PCB, this ceramic has no conductive material on it at the onset of the process. Via holes are punched in each layer and conductors are applied by squeeging a conductive paste through a silk screen constructed (usually) of fine stainless steel wires. The pattern on the silk

Table 6.3.2
Typical Minimum Via Pitches of
Printed Circuit Boards, Cofired Ceramic, and
High Density Substrates
(Dimensions in mils)

	1970	1975	1980	1985	1990	1995	Annual Change
PCB	66	36	36	36	28	25	-4%
Cofired	20	15	10	10	10	10	-3%
High Density	–	–	–	–	2-3	2-3	–

Source: Dataquest Microelectronics Packaging Handbook
Dataquest, April, 1992

screen is usually developed through photolithography. The individual layers are stacked and laminated and then the stack is fired in a ceramic furnace. The term "cofired" comes from the fact that all layers are fired concurrently. Usually, pins are brazed on the finished ceramic to provide input and output connections.

MCM-D substrates are produced using an outgrowth of semiconductor manufacturing technology. Often, the starting material is silicon, but other materials such as copper and ceramic have been used. The process begins by deposition of an insulating layer, usually polyimide or silicon dioxide. Holes are etched if layer to layer connections are required and metal, usually copper or aluminum, is applied on top of the insulator and through the holes. The undesired metal is then removed using photolithography. Subsequent layers are added by depositing and patterning more insulating and conductive layers.

Table 6.3.1 shows the trends for typical minum line pitches of printed circuit boards, cofired ceramic substrates and MCM-D substrates. The following comments apply to this table:

- In the 1970's and early 1980's, most PCB's implemented through hole technology. Dip packages with 100 mil pin spacing predominated. As a result line pitches finer than 10 to 12 mils were not needed.
- More recently, surface mount components were introduced. The 50 mil grid used on these packages helped drive line width down to the 8 to 10 mil range.
- Surface mount components are evolving to 12 mil pin spacings, increasing the need for finer line pitches.
- PCB line pitches of 4 mils should be possible in the 1995 time frame.
- Line pitches of 2 to 3 mils may become widely available in the future.
- The current PCB line pitch of 6 mils seems to be adequate for many MCM-L applications.
- Cofired ceramic line pitches are limited by the size of the silk screen mesh. Little future improvement is expected.
- The high density pitch of 1 to 2 mils or 25 to 50 microns is well within the capability of most semiconductor lithography equipment which commonly can image 1 to 2 microns or less. The larger 1 to 2 mil pitch adequately satisfies today's density requirements.

Table 6.3.3
Typical Patterning Tool Capabilities

Tool Type	Minimum Image (mils)	Maximum Substrate Size (inches)	Comments
Screen Printer	8	8 x 8	Minimum image limited by screen mesh
Proximity	0.1	24 x 24	Maximum patttern size limited by registration errors
Scanning Projection	0.1	6 x 6	Image limited to 60,000 lines
LCD Panel Stepper	0.1	12 x 16	Achieves 160,000 lines by making multiple images

Source: Dataquest, April, 1992

Table 6.3.2 shows the trend in via pitches for PCB's, cofired ceramic and high density substrates. The following comments apply:

- Wiring density depends on the via pitch as well as the line pitch.
- PCB vias are typically drilled. Via pitches have shrunk as wiring pitches have decreased.
- Drilling technology is evolving, leading to tighter via pitches. Some believe via pitches well below 10 mils could become routine.
- Laser drilling is another means of producting vias with a tight pitch.
- Cofired vias are gang-punched in the green ceramic.
- Dataquest expects that cofired vias will stay around a 10 mil pitch for the forseeable future.
- High density vias usually have pitches in the 2 to 3 mil range. Much smaller pitches could be achieved, but current applications do not require this.

Table 6.3.3 summarizes typical patterning tool capabilities:

- Screen printer image size is limited by the silk screen mesh. An 8 mil pitch is about the smallest that can be achieved in production quantities.
- The size of substrate that can be silk screened is also limited to about 8 inches by 8 inches because of the tendency of the screen to stretch in a non-uniform manner.
- Proximity printers in semiconductor applications can image lines smaller than 1 micron. Image size in PCB applications is limited by errors in registration between one layer and another. Registration errors also limit the maximum substrate size.

- Scanning projection aligners have the advantage that the mask does not contact the photoresist being printed, as in the case of proximity aligners. This leads to higher yields because masks do not pick up defects by being put in contact with the substrate being imaged. The maximum substrate size is limited by the number of lines that a lens can image.
- The LCD panel stepper was developed to image LCD panels. It achieves larger maximum substrate sizes by making multiple images. The images are formed by a lens, as in the case of the scanning projection aligner, so no mask damage occurs and high yields can be achieved.
- The 12 inch by 16 inch panel size for the LCD panel stepper is dictated by the requirement for a 10 inch diagonal display for laptop PC and TV use. Four displays can be imaged on a single panel of this size.
- If LCD's can be produced for current cost goals, the LCD panel stepper will become the most effective means of imaging MCM-D substrates.

6.4 Summary of Finished Substrate Cost Models

Silicon based MCM-D costs are estimated in some detail in Section 6.5. These estimates assume a 6 inch wafer and semiconductor manufacturing equipment that is purchased at current prices.

The result of the estimates of Section 6.5 is that MCM-D substrates can be built for $11 per square inch, assuming a 6 layer process. For a sanity check, compare this with the price of a 6 inch 1 to 1.5 micron foundry wafer which can be purchased today for $500 to $600 or $18 to $21 per square inch. The foundry CMOS wafer requires 13 mask layers, and if production cost is roughly proportional to the number of mask layers, this wafer should sell for $9 to $11. This comparison confirms that the estimates of section 6.5 are in the right ballpark.

The $11 substrate price of Section 6.5 does assume that the factory is large enough to produce substrates at a competitive cost and that the factory is running at capacity. Since the output of a factory this large is considerably larger than the 1991 MCM-D merchant market, it is likely that the $11 price will not be achieved in the near future.

If a substrate price of $11 per square inch is substituted into Table 6.2.3, the cost of the MCM-D substrate becomes $11.73. This is close to the cost of the SMT PCB at $6.53 and the MCM-L PCB at $10.50. Since a finished module of 5 chips is likely to sell for several hundred dollars when chip costs are included, a price difference this small is likely to be almost negligible.

Table 6.4.1 extends the thin film cost data derived in Section 6.5 by estimating plan investment in facilities and equipment and the revenue that a full capacity plant should produce. The unit size is the maximum substrate that the plant can handle and is available from industry data. In most cases, the substrates produced are smaller than the unit size, so many can be produced in one unit just as many semiconductor chips are produced on one wafer. Units per period are estimated from industry data and from equipment productivity. Once these are available, plant revenue and revenue per square inch can be calculated.

The following comments apply to Table 6.4.1:

- Unit size is a key parameter. The larger the unit size, the smaller the revenue (or price) per square inch.
- The cofired ceramic and laminate technologies are shown for comparison purposes.
- The prices per square inch will be realized only when the market is large enough to fully load one high volume plant. Cofired ceramic and PCB plants have an advantage because the plants can be filled today by products which are not MCM's.

Table 6.4.1
Comparison of Important MCM Substrate Manufacturing Technologies

Manufacturing Technology	Thin Film[1]	LCD Panel	Cofired Ceramic[2]	Laminate[3]
Equipment $ Facility Inv	$56 million	$60 million	$40 million	$15 million
Plant Revenue	$48 million	$50 million	$40 million	$25 million
Unit Size	6 in x 6 in	12 in x 16 in	8 in x 8 in	18 in x 24 in
Units per Period	10,000	10,000	7600	5000
Annual Sq. In.	4.3 million	49.9 million	6.3 million	28 million
Revenue per Gross Sq. In.	$11.00	$2.00	$6.30	$.89

[1] Data is From Section 6.5
[2] Assumes 8 metal layers
[3] Assumes 6 metal layers

Source: Dataquest, April, 1992

- The thin film plant shown in the table generates $48 million of revenue at full capacity. If the largest supplier in the market has a 30% market share, then the MCM-D substrate market must reach $160 million before this plant is fully loaded.
- A substrate market of $160 million translates to a module market of $500 to $600 million. This is about equal to today's captive market and much larger than the current merchant market.
- If LCD panel manufacturing technology is used to make MCM-D substrates, then this technology will become the most competitive in both price and performance. If a substrate price of $2 per square inch is used in Table 6.2.3, the cost of a 1.08 sq. in. substrate becomes $2.16. This is much less than the $6.53 cost of an equivalent SMT PCB or the equivalent $10.50 cost of a MCM-L PCB.
- The target cost of a 10 inch diagonal (6 inch by 8 inch) LCD panel is $200 or $4.17 per sq. in. This panel consists of the glass panel itself, a color filter and several chips which implement the row and column drivers.
- Dataquest estimates that the cost for a panel without drivers and color filter is about $100 or $2 per square inch. This tends to confirm the estimates of Table 6.4.1.
- Dataquest believes it will be some years before LCD manufacturing efficiencies are achieved. Nevertheless, the cost possibilities are highly attractive if LCD manufacturing technology can be applied to MCM-D substrates.

Table 6.5.1
Facilities Improvements for Substrate Fabrication Facility
(500 Wafers per Period, 2 Shift 5 Day Operation)

System	Requirements	Cost
Clean Room	4880 sq.ft.@ $1000/sq.ft.	$4,880,000
Chase Area	4514 sq.ft.@ $400/sq.ft.	1,805,600
Shell	10,000 sq.ft.@ $100/sq.ft	1,000,000
Total		$7,685,000

Source: Dataquest, April, 1992

6.5 Silicon Substrate Cost Model

This section presents budgetary estimates for a prototype sized MCM-D substrate production facility. This cost model is presented in some detail and includes estimates of capital, manpower and materials consumption. Substrate production costs in this facility are then compared with production costs in a larger facility that produces substrates at a lower cost per square inch. Graphs of wafer production cost vs. factory loading and factory size show the impact of manufacturing in a factory that is operating below capacity or one that is too small to be economically competitive.

The issue of substrate yield is dealt with and the advantage of square substrates over round substrates is discussed. Finally, estimated selling prices for substrates of different sizes are presented.

Dataquest believes that modified semiconductor technology has been the impetus behind MCM-D and that MCM-D will be one of the significant substrate technologies five to ten years in the future. Accordingly, these cost estimates should be pertinent.

This MCM-D facility is capable of producing five hundred six-inch substrates per four week period. Each of these is assumed to have six layers of masking, and the level of technology is adequate to support high yields of substrates with metal pitches as small as one mil.

Facilities Improvements

Although substrates are much less complex than semiconductor wafers and employ much looser geometries, each individual substrate is likely to be much larger than a typical semiconductor chip. While the looser geometries tend to improve the yields of individual substrates, the larger substrate sizes will tend to reduce yields.

Table 6.5.2
Manufacturing Equipment for Substrate Manufacturing Area
(500 wafers per Period, 2 Shift 5 Day Operation)

Equipment Type	Amount*
Process Monitoring Equipment	$ 895,000
Deposition and Plating Equipment	2,240,000
Etching Equipment	2,260,000
Photomasking Equipment	885,000
Subtotal	$6,280,000
Fit Up and Hook Up (15%)	$ 942,000
Total	$7,222,000

Source: Dataquest, April, 1992

Dataquest believes these factors tend to offset one another with the result that clean room requirements for the production of substrates are likely to be as stringent as those currently required in semiconductor facilities. Some MCM vendors have assumed that the facilities requirements of five years ago would be adequate for the manufacture of MCM-D substrates since these substrates only require the line widths of five years ago. This has not proven to be the case, since the size of the finished substrates is much larger than the VLSI chips of five years ago. Larger substrates are more likely to be rendered inoperative by defects caused by airborne particles. It is virtually impossible to produce these substrates in a facility that is not clean enough.

Table 6.5.1 shows facilities improvements for substrate fabrication. Here, the clean room requirements have been upgraded to class 10 from those of five years ago (Class 1000) to reflect today's tighter requirements. The other facilities in the chase area reflect a similar upgrading. The shell area reflects the size of the building before implementation of facilities improvements; the cost is typical of standard commercial construction. The total capital required for facilities is $7.7 million.

Equipment Expenditures

A summary of the expenditures for manufacturing equipment is shown in Table 6.5.2. Process monitoring equipment includes items such as probe stations, thin film measurement equipment, a SEM, chemical sinks and cleaning equipment.

Deposition and plating equipment includes a sputtering system, plating tanks and chemical benches as required.

Table 6.5.3
Labor Requirement for Substrate Manufacturing Facility
(500 Wafers per Period, 2 Shift, 5 Day Operation)
Head Function Count

Function	Head Count
Direct Labor	5
Indirect Labor	
Factory Indirect (Maintenance, Process Engineering, MIS, Ops)	9
QC and QA	6
Production, Materials, Facilities	11
Total Indirect	26
Total Head Count	31

Source: Dataquest, April, 1992

Etching equipment includes wet and dry etch equipment, a photoresist asher, microscopes and chemical sinks as required.

Photomasking equipment includes a scanning projection aligner (Perkin-Elmer, now owned by SVG, and Canon are major suppliers). This aligner is used rather than the more expensive 5:1 steppers popular today. This aligner should be able to resolve line widths to less than 2 microns. Since the substrates will have only one mil (25.4 micron) lines, this equipment is more than adequate. It is also much more productive than stepper equipment in terms of the wafer throughput that one unit can handle.

Some firms are planning to use proximity aligners for their MCM-D substrate fabrication facilities. Dataquest believes this is a poor decision since these devices are likely to produce high levels of defect density, which in turn will lead to lower substrate yields. In a proximity aligner, the defects are caused by the mask coming into contact with the substrate during the imaging portion of the manufacturing process. When this happens, the mask is likely to pick up small particles at one mask step and transfer them to another substrate the next time the same mask is used. A single particle can cause a bad substrate.

By contrast, the scanning projection equipment forms an image of the mask on the substrate and avoids direct contact. The mask can be more easily kept free of particles and, as a result, yields are much improved.

Labor Requirement

Table 6.5.3 gives the labor requirement for the small substrate manufacturing facility described here. Notice that direct labor headcount is small since much of the manufacturing equipment is semi-automatic. The indirect labor is aimed at keeping the equipment and factory running either through equipment maintenance or process engineering. QC and QA workers monitor the process quality and the production,

Table 6.5.4
Wafer Cost Analysis for Two Different
Substrate Manufacturing Facilities

	Cost per wafer	
	500 wafers per period 2 shift, 5 days	20,000 wafers per period 3 shift, 7 days
Variable Cost		
Materials	$69.80	$69.80
Direct Labor	23.60	15.50
Total	$93.40	$85.30
Fixed Cost		
Indirect Labor	$237.00	$37.60
Overheads*	61.50	25.20
Depreciation	301.80	69.00
Total	$600.30	$131.80
Total Wafer Cost	$693.70	$217.10
Capital Investment		
Facilities	$7.7 million	$31.2 million
Equipment	7.5 million	78.5 million
Total	$15.2 million	$109.7 million

Source: Dataquest, April, 1992

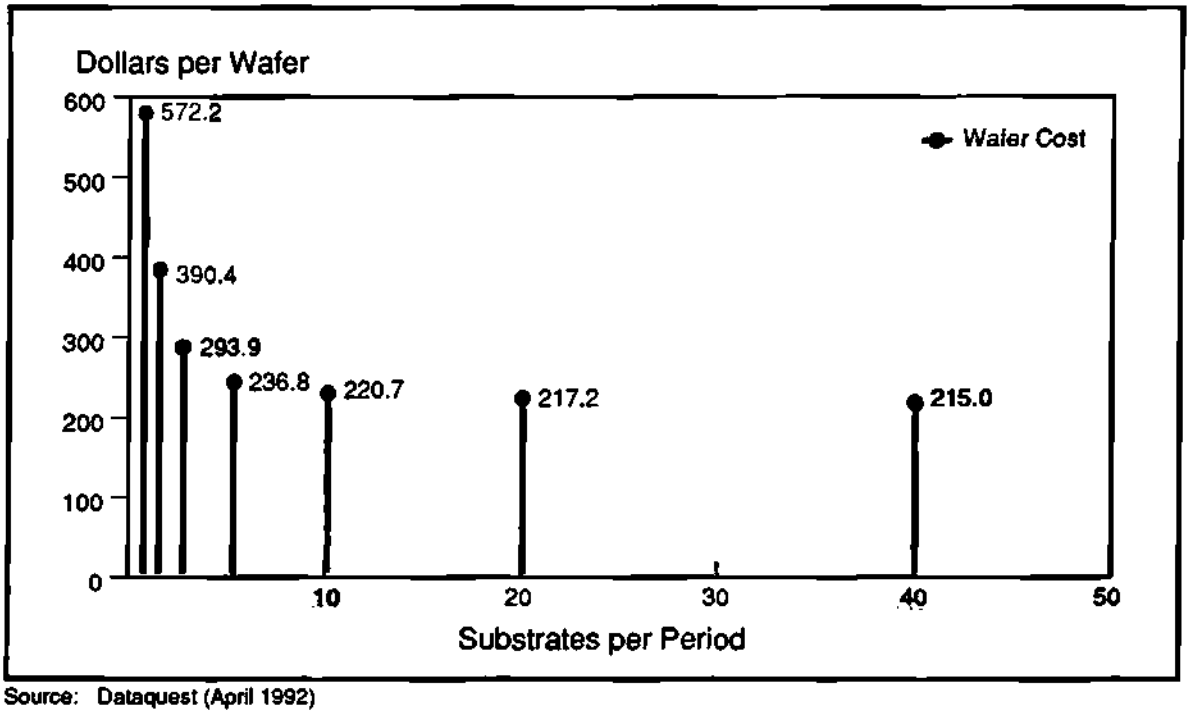
materials and facilities groups respectively determine the allocation of wafers to different products, procure the necessary incoming materials, and keep the major facilities running.

Impact of Production Volume on Cost

Table 6.5.4 gives a wafer cost analysis for two different substrate manufacturing facilities. The first column gives the costs for the prototype facility described in this section while the second column gives manufacturing costs for a much larger 20,000 substrate per period manufacturing facility. Notice that while the larger facility has a much higher capital investment ($109.7 million compared with $15.2 million) it produces substrates at a much lower cost ($217 per wafer compared with $694 per wafer).

The example of Table 6.5.4 illustrates that a larger substrate production facility can produce substrates at a lower cost than a smaller facility. An important question that arises is: "How large does a substrate production facility have to be to be competitive?"

Figure 6.5.1
Substrate Cost versus Factory Size
(6 Inch, 3 Shift, 7 Day)



Source: Dataquest (April 1992)

Figure 6.5.1 gives the answer to this question. The data in this figure was developed by designing substrate production factories of different sizes and plotting the the substrate production cost of each factory as a function of the factory size. In every case the plant was assumed to be operating at full capacity.

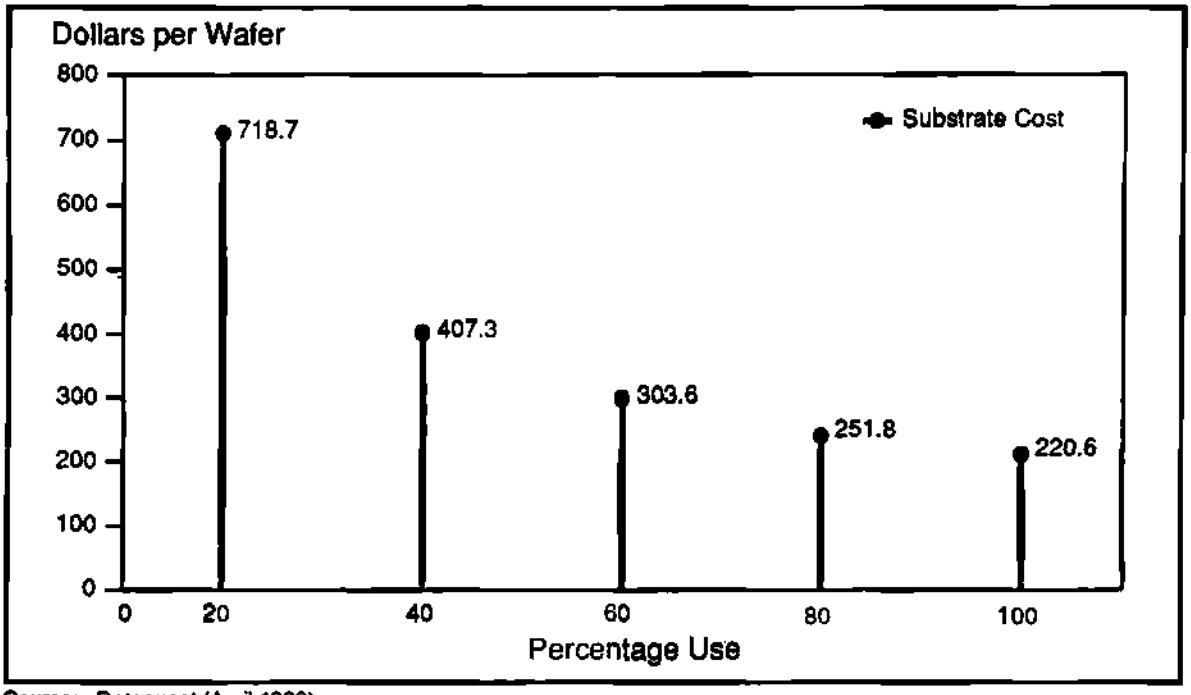
From Figure 6.5.1, it can be seen that a 10,000 substrate per period factory produced substrates at a cost that is almost as low as the substrate cost in a 40,000 wafer per period factory. It would make no sense to construct the larger factory unless it was highly likely that the market was large enough to utilize the output of the factory.

Substrate factories have very high production costs when they are below capacity. Figure 6.5.2 shows this effect. Here it can be seen that a 10,000 substrate per period factory running at 40% of capacity produces substrates at almost twice what they would cost if the factory were running at capacity. In this case, substrates could be produced less expensively in a factory that was designed to operate at 4,000 wafers per period.

The question of optimum factory size is of strategic importance. If a substrate producer builds a factory that is too small (less than 10,000 substrates out per period) then this producer is always vulnerable to a competitor that has the larger factory. If the market is large enough, this competitor can cut prices to gain market share from the smaller vendor. Once the market share is gained, the larger vendor will be profitable while the smaller vendor is not.

If a substrate vendor builds a factory that is too large for the market, then this factory will operate below capacity and will produce substrates at a very high cost. A vendor with a smaller plant that is able to operate at capacity will be able to produce substrates at a more competitive price.

Figure 6.5.2
Substrate Cost versus Factory Utilization
(Plant Size: 10,000 Substrates per Period)



Source: Dataquest (April 1992)

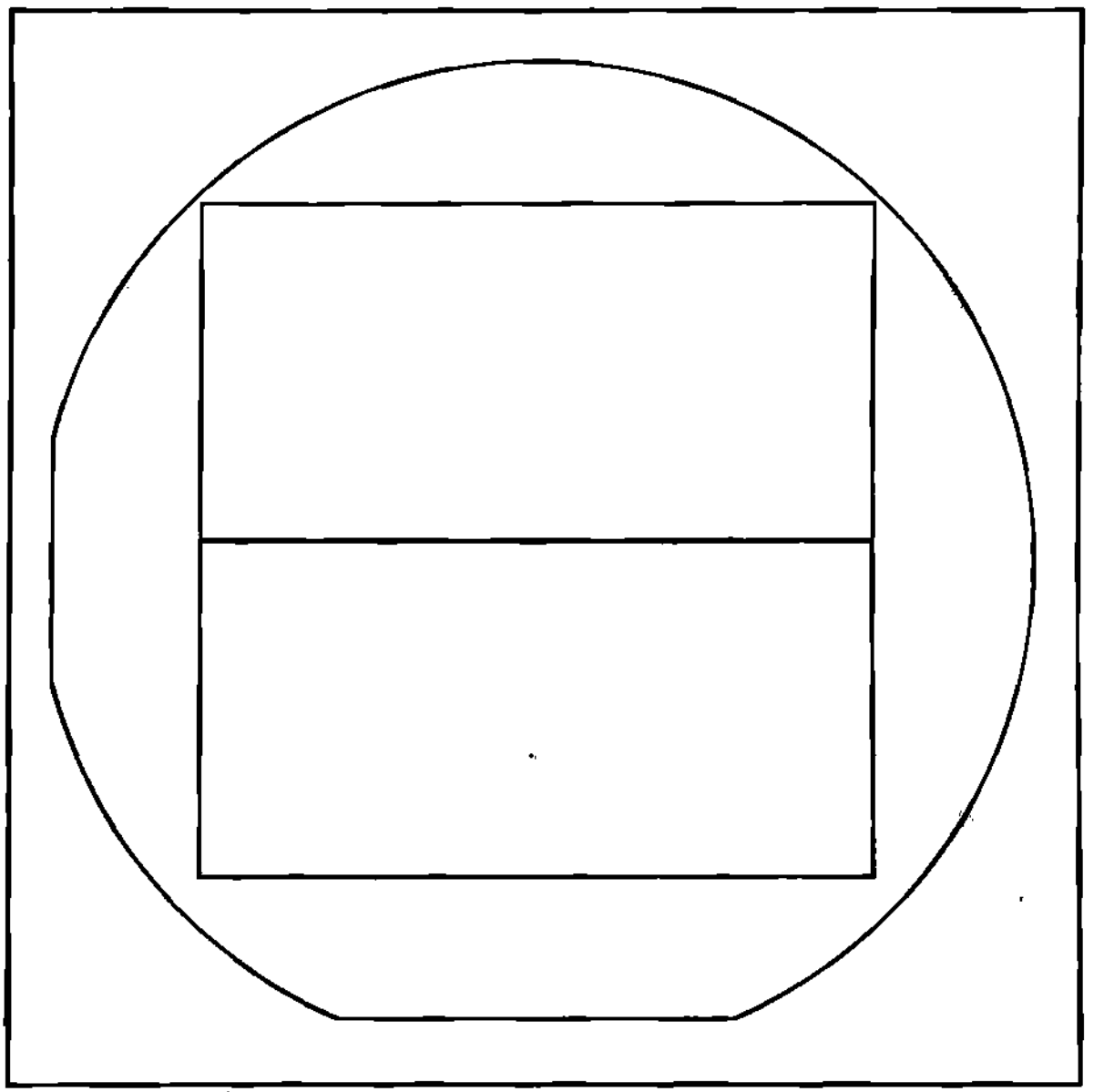
For example, assume the larger vendor has a 40,000 substrate per period plant while the market will only take 10,000 wafers per period from any plant. In this case, the vendor with the 40,000 substrate per period plant is operating at 25% of capacity. Wafer costs in this plant will be more than three times as high as they would be at capacity (See Figure 6.5.2. The relative substrate cost for a 40,000 substrate per period plant operation at 25% of capacity is roughly the same as in a 10,000 substrate per period plant). Meanwhile (See Figure 6.5.1) the vendor with the 10,000 substrate per period plant is producing substrates at $220 or only about a 3% premium.

Round vs. Square Substrates

Most of today's MCM producers plan to use semiconductor manufacturing equipment to produce their substrates. Traditionally, this equipment has been designed to work with round silicon wafers; silicon wafers are naturally round because of the way they are fabricated from a melt of liquid silicon. Although most semiconductor manufacturing equipment has been designed to work with round wafers, Dataquest believes it can be modified to work with square substrates. At least one substrate manufacturer has built a line that works with square material. This line used ceramic material because square silicon material is not readily available.

Until now, we have referred to the entire wafer as a substrate. In actual practice, most MCM substrates are much smaller than a wafer and it is common to build a multiplicity of individual substrates on a single wafer.

Figure 6.5.3
Layout of 8-Square-Inch Substrates (2x x 4 Inches) on a 6-Inch Wafer



Source: Dataquest (April 1992)

Figure 6.5.3 illustrates the situation in which two 8 square inch substrates (4 inches x 2 inches) are fabricated on a single round six inch wafer. Notice that the two individual substrates barely fit and that a significant part of the round wafer is wasted in the attempt to put a square individual substrate on a round wafer. If the wafer were 6 inches square, three individual 8 square inch substrates could be accomodated. This represents a 50% productivity increase.

Table 6.5.5
Gross Available Substrates
On Round and Square Material

Membrane/ Substrate Size* (Sq. In.)	1/4	1/2	1	2	4	8
Gross Number on Round 6 Inch Material	89	40	19	9	4	2
Gross Number on Square 6 Inch Material	144	64	36	18	6	3
Cost Reduction For Square Material	46%	38%	47%	50%	33%	33%

*All individual membrane/substrates are square except the 2 sq. in. one is 1 in. x 2 in., the 4 sq. in. one is 1.6 in. x 2.5 in. and the 8 sq. in one is 4 in. x 2 in.

Source: Dataquest, April, 1992

Square wafers are more productive for two reasons: they use the available area more effectively because it is easier to fit square individual substrates onto square material, and they have more square inches of substrate available. A round wafer is approximately 28 square inches while a square 6 inch substrate is 36 square inches, a 28% increase.

Dataquest believes that there should be little or no increase in manufacturing costs for square substrates as compared to round substrates. This means that the extra eight square inches of substrate should be virtually free. As a result, individual substrates made on square material should cost less than substrates made on round material.

Table 6.5.5 shows the number of substrates that can be fabricated on round and square material, respectively. As indicated, the relative advantage of square material depends somewhat on the size of the individual substrate because there is a significant loss of individual substrates at the edge of the round material. Depending on size, the cost reduction for individual substrates varies anywhere from 33% to 50%.

Substrate Yield

It has often been said that substrate producers can easily make a product using the semiconductor equipment of a decade ago. This is true if only line width is considered – in fact, semiconductor manufacturers were routinely building IC's with 10 micron (1/2 mil) lines and spaces in the early 1970's.

Table 6.5.6
Yield of Membrane/Substrates

Substrate Size (Sq. In.)	1.4	1/2	1	2	4	8
Yield	97%	95	90%	81%	66%	45%

Source: Dataquest, April, 1992

However, the chips that were built in those days were normally less than 200 mils on a side with a total area less than 1/25th of a square inch. This is a far cry from the four and eight square inch individual substrates being contemplated today. The yields on those chips of the 1970's were also in the 10% range, even though they consisted of only six to eight mask layers. If that technology were applied to building today's larger MCM substrates, the yields would be vanishing small.

To make money, a substrate production facility needs to combine the line-width capability of a decade ago with the cleanliness technology of the 1990's. If that can be accomplished, yields of individual substrates can approach levels that make the production process economical.

This section presents a yield model which extrapolates the yield of a modern semiconductor factory into the yield that might be expected from a substrate factory which employs 1990 cleanliness technology.

The yield model scales yields from the yields of today's 4 megabit DRAMs by making the following observations:

- Yield is decreased substantially because of the larger size of the individual substrate.
- Yield is increased by the fact that the metal pitch of an MCM-D substrate is much larger than a DRAM.

The model assumes a standard yield model and also that the defect density decreases as the square of the metal pitch. Dataquest views this calculation method as one that is only approximate. It is always dangerous to extrapolate yield from one factory situation to another, and the extrapolation to larger line widths is especially subject to error. In addition, substrate manufacture may employ one or more process steps that are not production-ready and as a result exhibit low yields. Still, Dataquest believes that the calculations illustrate the types of yield issues that need to be considered.

Table 6.5.6 gives the results of the yield calculations described above for individual substrates ranging in size from a quarter of a square inch to 8 square inches. The smaller substrates have almost perfect yields while the larger substrate has only 45% yield.

Table 6.5.7
Factory Revenue at 10,000 Wafers Per Period*

Wafers out	10,000
Wafer Cost*	$222
Gross Margin	40%
Revenue/Wafer (222/0.6)	$370
Plant Revenue	$3.7 million/period
	$48.1 million/year

*Assumes 3 shift, 7 day operation

Source: Dataquest, April, 1992

Price and Factory Revenue

Table 6.5.7 computes factory revenue for the "minimum economical sized" plant producing 10,000 substrates per period. Here the wafer cost is taken at $222 and the gross margin is assumed to be 40% of sales. The result is that the plant has revenue per wafer of $370 and that annual production is almost $50 million per year. If such a plant had 33% market share, this would imply that the total market of about $150 million would be adequate to fill one "minimum sized" plant to full capacity. If all other producers had smaller market share, this producer would also be the low priced producer and would be able to set the market prices at a level that maintained its profitability while all other producers operated at a loss.

Substrate Selling Prices

Table 6.5.8 takes the yield assumptions of table 6.5.6 and the pricing assumptions of table 6.5.7 to develop estimates of minimum substrate selling prices for both round and square substrates. Referring to the price per square inch for square substrates it can be seen that this price is as low as $11.56 for a 1 inch square individual substrate fabricated on a square six inch starting material.

In Table 6.2.3, the MCM-D substrate cost was assumed to be $30 per square inch, with the result that MCM-D substrates were about the same price as the equivalent MCM-C substrates. At $11.56 per square inch, the MCM-D substrate becomes the low cost option for high frequency applications. In addition, the MCM-D substrate will cost $12.33 or only about 17% more than the competitive MCM-L substrate ($10.50). This result is achieved through economies of scale and should occur when the market grows to the appropriate size.

Table 6.5.8
High-Volume Membrane/Substrate
Yielded Selling Prices*

Substrate Size (sq. in.)	1/4	1/2	1	2	4	8
Net Substrates						
Round Substrate	86	38	17	7	2.6	.9
Square Substrate	139	60	32	14	3.9	1.3
Selling Price						
Round Substrate	$4.30	$9.74	$21.76	$52.86	$142.30	$411.11
Square Substrate	$2.66	$6.17	$11.56	$26.42	$94.87	$284.62
Selling Price per Square Inch						
Round Substrate	$17.20	$19.48	$21.76	$26.43	$35.57	$51.38
Square Substrate	$10.64	$12.34	$11.56	$13.21	$23.71	$35.57

*Assumes revenue of $370 per wafer for either a round or square wafer.

Source: Dataquest, April, 1992

6.6 Power Handling in MCM's

This section deals with power handling in MCM's, particularly in regard to future trends. It begins with a discussion of power scaling theory. This theory deals with the way chip power should increase as chips get more complex. It is followed by discussion of microprocessor power trends. Memory power is then related to chip complexity and ECL power trends are discussed.

Microprocessor power trends are then related to time as well as complexity. This analysis indicates chip power could reach 75 to 300 watts by the end of the century, if current trends continue. Dataquest believes that cost and battery life considerations will drive chip designers to seek ways of reducing chip power. Some of these possibilities are presented and the current status of 3 volt power is discussed.

Some existing thermal management systems are examined to see how their power handling capability relates to the estimated future chip requirements discussed earlier. It seems that these systems will be inadequate for the needs of future microprocessors. Fortunately, at least one experimental cooling system has been developed which looks like it might satisfy future needs.

The various substrates used by different types of MCM's are examined to see what kind of temperature drop they cause in a 5 watt thermal path.

Finally, a scenario for a system of the future is presented.

Table 6.6.1
Power Dissemination of
Microprocessor Chips

Part	Transistor Count	Power (Watts)	Power/Transistor (Microwatts)
80086	29,000	0.4	13.8
80286	134,000	0.5	3.7
80386	275,000	2.5	9.1
80486	1,200,000	3.5	2.9
I860	2,500,000	3.3	1.3
68020	200,000	1.75	8.8
68030	300,000	2.25	7.5
R4000	1,300,000	10.0	7.7
DEC Alpha	1,700,000	25.0	14.7

Source: Dataquest, April, 1992

Power Scaling Theory

Chip complexity is continuously increasing due to shrinkage of the line width dimension. Scaling theory has been developed to relate chip performance factors to the scaling factor or percent shrinkage in line width. In the case of chip power, scaling theory says that chip power density should be constant if the power supply voltage is reduced in proportion to the reduction in line width.* This means that, in theory, the power required by VLSI chips should not increase as chips became more complex, so long as the chip area did not increase.

Saying it another way, if line widths shrink from 1 micron to half a micron, then the power supply voltage should be reduced from 5 volts to 2.5 volts to keep the chip power constant, assuming that the chip size does not increase. Of course, the size of each transistor in the chip will shrink by the square of the line width, so the half micron chip will have four times as many transistors. Since power is constant, the power per transistor (or gate) should fall by a factor of four.

If the power supply voltage is not scaled, then the power required by the chip will increase as the line width shrinks. In addition, chip sizes increase with time as yields improve, and the additional chip area also consumes additional power. Other issues also complicate the trends in microprocessor power consumption. The next section provides power consumption data on actual microprocessor chips so that trends can be examined directly.

* Bakaglu, "Circuits, Interconnection, and Packaging for VLSI," Pages 26 to 27

Microprocessor Power Trends

Table 6.6.1 gives some power consumption figures for microprocessors of different complexities and figure 6.6.1 presents a plot of the same data. All of these devices have a 5 volt power supply except for the DEC Alpha which runs at 3.3 volts.

Most microprocessors have power dissipation per transistor in the range of 1 to 10 microwatts. Among the Intel chips (80086 through I860) there seems to be a downward trend in the power dissipation per transistor. The DEC Alpha has exceptionally high power dissipation, especially since its lower power supply voltage should have reduced the power. This chip runs at 200 megahertz—most likely the designers focused on improving the clock rate rather than reducing the power.

The plot of microprocessor power in Figure 6.6.1 shows that power increases rapidly with transistor count. There is considerable dispersion in the data, indicating that chip power can vary over a wide range for chips of the same complexity. Some possible reasons for this variation are discussed in the section called "Ways to Save Power." The trend line is drawn through the middle of the cluster of data points, so it is probably optimistic for some chips. Even so, the trend line indicates that future chips of ten million transistor complexity will typically consume 40 watts.

Memory Power Trends

Table 6.6.2 gives power dissipation for some typical memory chips, and Figure 6.6.2 gives a plot of the same data. The power figures given here assume the memory chip is being continuously addressed. Many memory chips consume negligible power when they are not being addressed.

Memory chips are not like microprocessors insofar as power consumption is concerned. When a memory chip is addressed, only one or a few locations on the chip are accessed—the locations which are not addressed draw negligible power. As an example, consider a "times one" megabit DRAM. When this chip is addressed, only one of the million memory cells is accessed; the rest of the memory cells are on standby status. Most of the power in the chip is consumed by the addressing logic and the amplifier which reads the signal from the single cell being addressed.

When the number of bits in a memory increase, the same situation still applies: if the memory is in the "times one" configuration, only one bit is addressed and most of the power is consumed in the address logic and the address decoders. The address decoder is slightly more complex for a 4 megabit part than a 1 megabit part, so this part of the chip will draw a little more power in a larger memory.

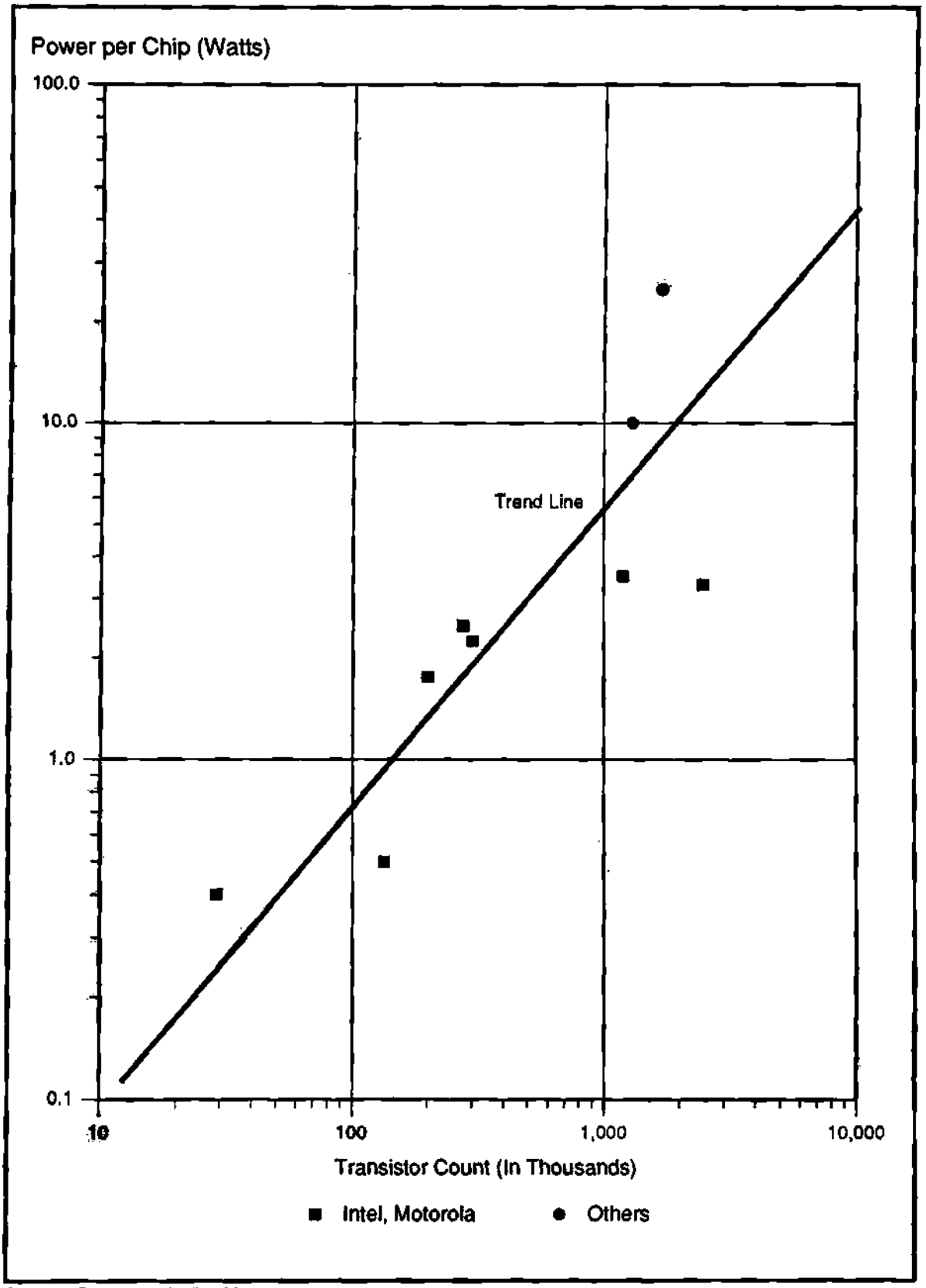
Figure 6.6.2 illustrates the situation. Here, both the DRAM and SRAM trends indicate that chip power increases only slowly as memory chip complexity increases. This trend is much slower than the microprocessor trend. It does not appear that memory power dissipation will be of concern for the foreseeable future since SRAM's will be about 1 watt and DRAMs should be below a watt, even at the 10 million transistor level.

ECL Power Trends

Figure 6.6.3 shows some ECL power trends. ECL chips use bipolar technology and tend to be much higher in power than CMOS chips of the same complexity.

ECL gates draw more power because current is flowing continuously in the gate, whether it is switching or not. CMOS gates draw power only when they are actually switching. ECL gates also tend to be higher in power than CMOS gates. This is somewhat compensated for by the fact that they can run at very high frequencies. Many CMOS gates operate at frequencies well over 200 megahertz.

Figure 6.6.1
Microprocessor Chip Power versus Transistor Count



Source: Dataquest (April 1992)

Table 6.6.2
Power Dissipation of Memory Chips

Part	Transistor Count	Power (Watts)
DRAM:		
64K x 1	64,000	0.15
256K x 1	256,000	0.28
256K x 4	1,000,000	0.30
1M x 1	1,000,000	0.30
4M x 1	4,000,000	0.25
SRAM:		
16K	64,000	0.35
64K	256,000	0.60
256K	1,000,000	0.65

Source: Dataquest, April, 1992

The performance of ECL systems has been limited by power and cost considerations, in spite of the inherent performance of ECL technology. This comes about because the high power density of ECL requires costly and bulky packaging in practical systems. Typically, ECL chips are less complex than CMOS chips, and the result is that complex systems tend to be physically large. The performance of these systems tends to be limited by the long transit time effects which are due to large physical size. Today, an increasing number of system engineers feel that future complex, high performance computer systems will be built with CMOS rather than ECL.

In spite of the above, there are applications in areas like telecom that require high frequency performance without undue complexity. ECL is a good choice in these applications.

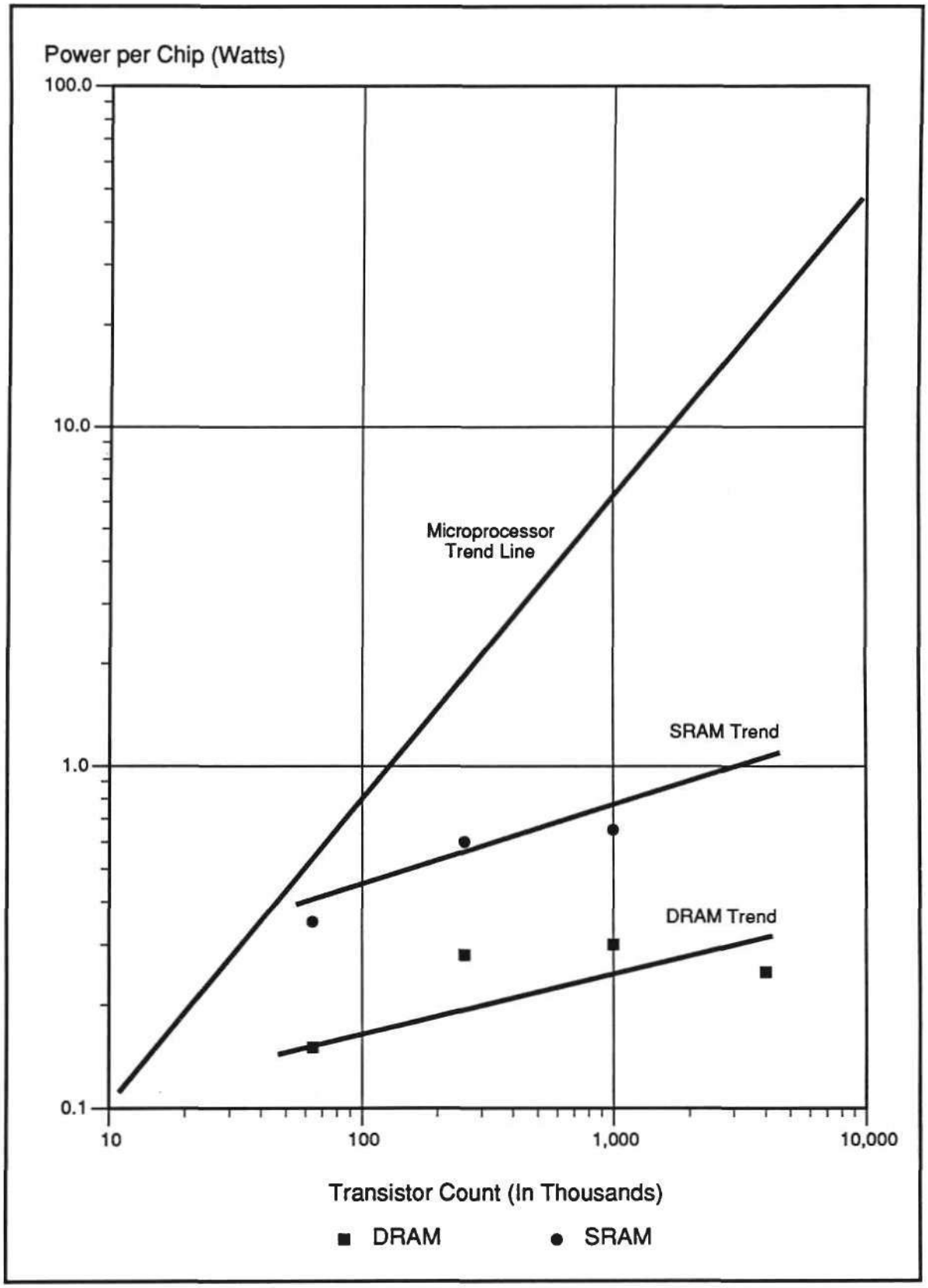
Microprocessor Power Trends With Time

Figure 6.6.4 shows the way in which microprocessor transistor count increases with time. It indicates that microprocessors with 100 million transistors should be available by the end of the century if current trends continue. The right axis of Figure 6.6.4 has been labelled with the power level indicated by the trend line of Figure 6.6.1. To illustrate, this trend line crosses the 10 million transistor level at 40 watts so the 10 million transistor line in Figure 6.6.4 is labelled as being 40 watts.

As it stands, the trend line of Figure 6.6.4 indicates that microprocessor power could reach 290 watts or more in the year 2000. It is forecast that this chip will be about 1 inch on a side, so the power dissipation for such a chip is 45 watts per square centimeter. Typical microprocessors today dissipate power in the range of 2 to 12 watts per square centimeter.

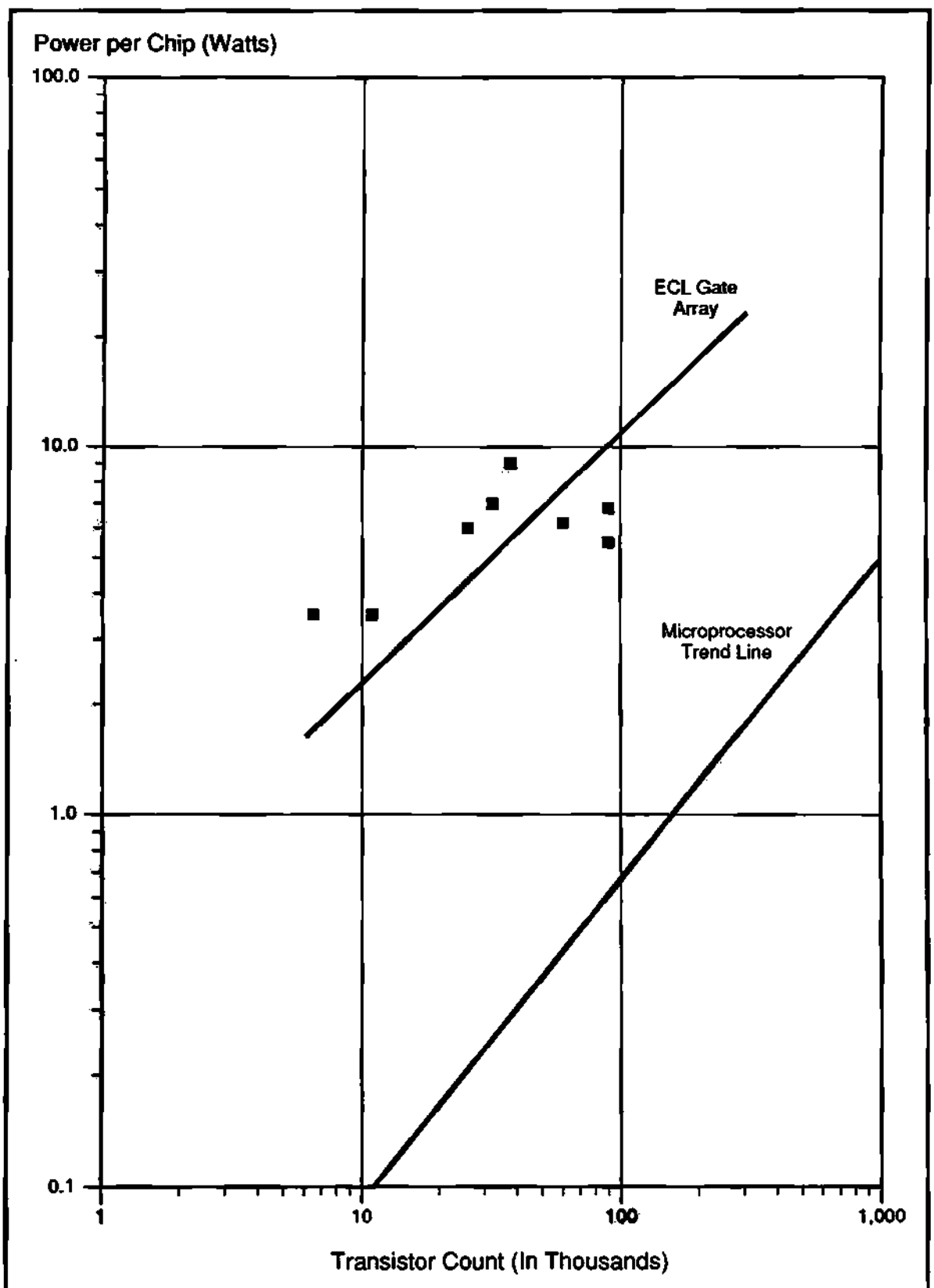
If you recall the discussion of scaling theory, it stated that if the power supply voltage was reduced in proportion to the shrinkage in line width, the power density of chips should remain constant. If this were accomplished, the 1 square inch chip of the year 2000 would dissipate only 77 watts.

Figure 6.6.2
Memory Chip Power versus Transistor Count



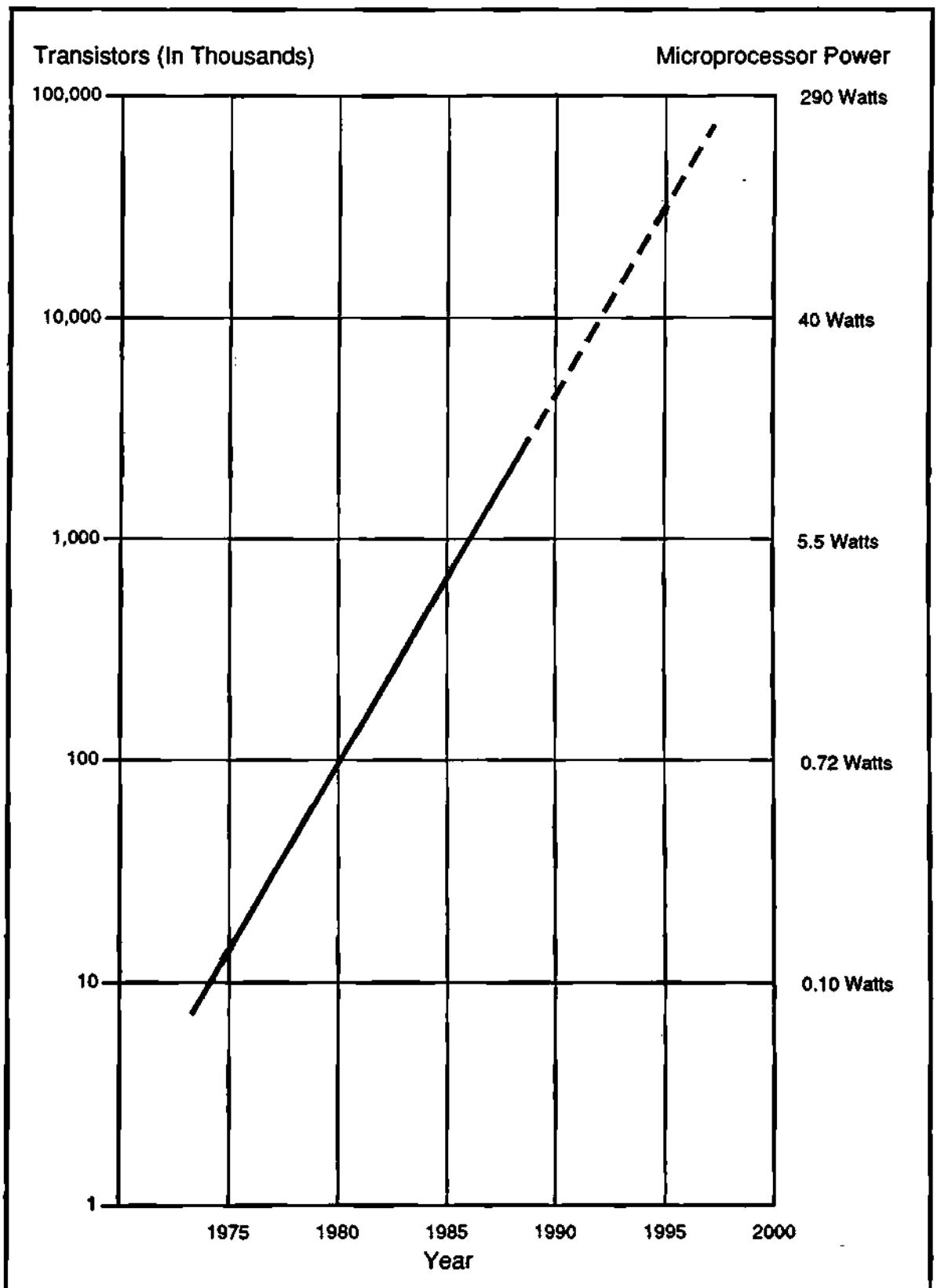
Source: Dataquest (April 1992)

Figure 6.6.3
ECL Gate Array versus Transistor Count



Source: Dataquest (April 1992)

Figure 6.6.4
Microprocessor Chip Power versus Time



Source: Dataquest (April 1992)

Scaling theory also says that clock rate can improve in proportion to the shrinkage of line width, even if the power supply voltage is also proportionately reduced. However, if supply voltage is not reduced, performance improves even more rapidly. Thus, it seems that chip designers will have the option of trading some of the available increase in clock rate for power dissipation.

Saving Power in CMOS Chips

Microprocessor chip power depends on many things besides the number of transistors on the chip and the power supply voltage. Among these are:

- The average number of nodes switched.
- The two transistor conduction effect.
- Average wire length.
- Number of output drivers.
- Capacitive loading on the outputs.

As stated earlier, CMOS logic only dissipates power when it switches—nodes that do not change state dissipate negligible power. Chip designers can therefore reduce power by designing their logic so that as few nodes as possible are switched during commonly used operations.

A CMOS node can function in one of two ways: The pull up transistor can turn off before the pull down transistor turns on, or the transistors can be designed so that both are on for part of the switching cycle. The former case corresponds to slower operation because there is a period of time during which nothing is happening because the output is connected to neither transistor. In the latter case, both transistors are conducting and the power supply is dumping current into ground. This improves performance at the expense of power. Chip engineers can control the degree to which two transistor conduction occurs and, once again trade power for speed.

The dissipation of a CMOS gate depends on the capacitance which it drives—the more capacitance, the more power dissipation. Capacitance is in turn a function of the average wire length on a CMOS chip. If the design can shorten the average wire length, average capacitance and power are reduced.

On many microprocessors, the output drivers account for half the power. Accordingly, power can be reduced by reducing the number of output drivers. This might be accomplished, for instance, by reconstructing some signals on the receiving chip so that they will not have to be transmitted through the output driver.

Some engineers feel that as chips become more complex, the number of drivers required per internal gate will be reduced drastically. In the extreme example, a personal computer has only a few wires entering and leaving the system: two 110 volt AC power wires, a twisted pair to connect to the telephone system or a network, and a ground. If microprocessor output pins are reduced in this manner, power will be saved.

Today's microprocessors are typically designed for capacitive loads of 50 to 100 picofarads on the output drivers. If these driver signals are confined within an MCM, the average capacitive load is much reduced and power is saved accordingly.

Future microprocessor chips may include a much larger percentage of memory. Since memory draws a lot less power than logic, the power dissipation of microprocessors would be reduced accordingly.

Finally, it may be that all portions of a chip are not designed to run at the same speed. Power could be reduced on the low speed portions of a chip by reducing the power supply voltage in these areas or by employing gates that did not exhibit two transistor conduction in these parts of the chip.

Table 6.6.3
Some Examples of Thermal Management Systems

System	Power (Watts)	Size	Watts/ Sq. Cm.
IBM Thermal Conduction Module	300	90 x 90mm	3.7
Mitsubishi High Thermal Conduction Module	36	65 x 65mm (est)	0.9
IBM 4381 Air Cooled Module	90	64 x 64mm	2.2
Tuckerman and Pease Microchannels (experimental)	790	1cm x 1cm	790

*Data is from "Microelectronics Packaging Handbook," Tummala and Rumaszewske, pages 211 through 219.

Source: Dataquest Electronics Packaging Handbook
Dataquest, April, 1992

Three Volt Power Trends

Many in the semiconductor industry are predicting a massive conversion of CMOS to 3.3 volt power by 1993. As indicated earlier, the DEC Alpha microprocessor already employs 3.3 volt power.

Three volt conversion is driven by the need to reduce power and increase battery life of portable computing devices. Power savings of over 50% are possible.

Three volt conversion is also driven by the need for a reduced power supply voltage in 16 megabit DRAMs. The 0.5 micron transistors required for this product do not work well with a 5 volt power supply.

Some factors which may impede the conversion to three volts include:

- The fact that many part types are not available in a three volt version. Some near-term systems may have to be built with a mixture of three and five volt parts.
- The incompatibility of input/output level specifications between three and five volt parts and between three volt parts from different manufacturers.

Some manufacturers today are handling the conversion from three to five volt parts by recharacterization rather than redesign. Recharacterization is easier, but may result in input/output specification incompatibilities.

JEDEC is working to establish standards, but Dataquest has found that many vendors do not follow the current standards.

Example of Thermal Management Systems

ECL chips commonly have had power dissipations in the range of 4 to 10 watts or more, and several systems have been designed to package a multiplicity of these parts. Some of these systems are tabulated in Table 6.6.3.

Table 6.6.4
Thermal Performance of Various Substrate and Dielectric Materials

Material	Thickness (mm)	Thermal Conductivity W(cm-deg.K)	Temp Rise* (deg. C)
Ceramic Cofired			
Alumina	2.54	0.2	6.4
Glass Ceramic	2.54	0.05	25.4
Aluminum Nitride	2.54	2.3	0.55
Silicon Carbide	2.54	2.2	0.57
Laminate			
FR4	2.54	0.002	635.0
Teflon	2.54	0.1	12.7
High Density			
Copper	2.54	4.0	0.31
Aluminum	2.54	2.3	0.55
Diamond	2.54	20.0	0.06
Silicon	0.25	.84	0.15
Silicon Dioxide	0.02	.01	1.00
Polyimide	0.02	.002	5.00
Benzocyclobutane	0.02	.002	5.00

*Assumed power density is 5 watts per square centimeter.

Source: Electronics Packaging Handbook
Dataquest, April, 1992

Our earlier examination of microprocessor power dissipation indicated that required power dissipation densities in the range of 12 to 45 watts per square centimeter of chip may be required by the end of the century.

The thermal management systems of Table 6.6.3 have been characterized by the power density that they are able to handle. Notice that for the first three examples these densities are in the range of .9 to 3.7 watts per square centimeter.

As a minimum, it seems logical to package VLSI chips so that at least half the area of the thermal management system is occupied by the chip. This means that the power density the system has to handle should be in the range of 6 to 22.5 watts. Clearly, the first three packaging systems of Table 6.6.3 are inadequate. This is in spite of the fact that they represent very sophisticated and expensive solutions to the thermal management problem.

The Tuckerman and Pease microchannel system is an interesting one. In this system a silicon die is cooled by a liquid that flows through microchannels etched in the back of the die itself. In this way, the path between the cooling liquid and the source of power is shortened to the ultimate degree. The result is a spectacular increase in power handling capability. This system is still highly experimental, so it will be some time before it reaches production. Still, it gives hope that at least one potential solution to future power handling problems does exist.

Substrate Power Handling

Different substrates are in use in MCM's. This section looks at the power handling capability of these substrates.

The temperature rise data in Table 6.6.4 assumes that power density is 5 watts per square centimeter and that, for structural substrates, the material is one tenth of an inch thick (2.54mm). The thickness of other materials such as silicon, silicon dioxide, polyimide and benzocyclobutane is taken at smaller values typical of their applications. It is also assumed that all the heat flows at right angles through the substrate with no fringing. This makes the computed temperature rise 10% to 20% higher than it might be in actual practice.

Of the ceramic cofired materials, aluminum nitride and silicon carbide have excellent performance with a temperature rise of less than one degree centigrade. Alumina has a manageable temperature rise and the glass ceramic material has an excessive rise at 25.4 degrees centigrade. If this material is used as an interconnect media for high power devices, heat will have to be removed through a path that does not go through the substrate.

Among the laminates, teflon is superior to FR-4. It is common in FR-4 substrates to put copper posts underneath the chip or to mount the chip on a slug of copper that is attached to the PCB. Even if the copper only occupies 25% of the area under the chip the temperature rise will be about 1.2 degrees (four times the 0.31 degrees shown in the table).

In the high density regime, any of the structural materials can be used to support the interconnect. These include the ceramic materials as well as copper and aluminum. Diamond is shown for reference; it is one of the best heat conductors known and is in demand in military applications where cost is no object.

Silicon wafers are normally about 10 mils (.25mm) thick and must be mounted on some other more rigid material. If the thermal resistance of the mounting material is neglected, the temperature rise will be the sum of the temperature rises of the two materials. Thus if silicon is mounted on aluminum nitride, the temperature rise caused by the two substrate materials will be 0.15 plus 0.57 or 0.72 degrees.

The silicon dioxide, polyimide and benzocyclobutane layers are taken at .02mm (20 microns). At these thicknesses, the temperature rise is minimal.

In most applications, a temperature rise of 60 degrees centigrade can be tolerated. Since most of the temperature rise is attributed to other factors such as the size of the heat sink, many of the materials in Table 6.6.4 can be inserted in the thermal path without adding significantly to the temperature rise. Some materials such as the glass ceramic and the PCB laminates are inadequate and alternative thermal paths must be provided if they are to be used.

The System of the Future

We have seen that chip designers can scale the power supply voltage and other aspects of chips to keep them within the constraints imposed by the thermal management system. It is also true that the market will seek the highest performance possible without undue increase in cost. It follows then designers will opt for higher power chips if low price thermal management systems can be developed.

The constraints outlined in this chapter lead to the following scenario for a moderately high powered system of the year 2000:

- Chip transistor count: 110 million.
- Number of chips in system: 9.
- System transistor count: 1 billion.

- Chip power: 110 watts.
- System power: 1 kilowatt.
- Clock rate: 400 megahertz.
- Equivalent complexity: 364 times as complex as an Intel 80386.
- Computing power: 51,000 MIPS.
- Physical size: approximately 5 inches by 5 inches.

It may seem that system power of 1 kilowatt is high, but this is only about 2/3 the amount of power consumed by the little electric heaters that plug into the wall. This computer module should be good for keeping your feet warm in the winter, if nothing else.

Chapter 7 – MCM Test and Assembly

The purpose of this chapter is to provide an overview of MCM test and assembly. MCM assembly involves interconnecting component parts into a working module; the component parts include the substrate, the chips themselves, a package to hold the substrate, if necessary, and any materials that may be required. Upon completion of assembly, the finished module is tested to assure that it is working properly.

Testing is discussed in some detail, and a tutorial discussion of chip test is provided for those who are not familiar with this field.

A major conclusion of this chapter is that thorough testing at the chip level is absolutely mandatory if high volume module production is to become a reality. This arises from the fact that it is virtually impossible to find all defects when testing at the module level.

Consider the consequences of a requirement that module test must be as thorough as chip test. In this case, the module is equivalent to a very complex chip – five, ten or twenty times as complex as a typical chip if there are five, ten or twenty chips in the module. New test programs have to be developed to test this monster chip, and the tester itself becomes more complex. VLSI testers cost roughly $10,000 per pin, and the module may have two to three times as many pins as the individual chips. It is easy to conceive of a 1000 pin tester – such a machine would cost $10 million dollars or more.

If the chips going into an MCM are known to be good, then the module level test need only detect errors in the assembly process itself – errors like open or shorted wiring connections. This test problem is much simpler.

Traditionally, testing of assembled PCB's has been with the assumption that the individual components are known to be good. These PCB's have high quality because of the high quality of the components going into them. Today it is common to have component incoming quality rates of 200 parts per million (ppm) or better.

There has been much discussion concerning the IEEE 1149 test specification spearheaded by the JTAG group. While it is true that chips designed to this specification can be more easily tested after they are assembled, Dataquest does not believe that IEEE 1149 makes it possible to build high quality MCM's with chips that are not known to be good.

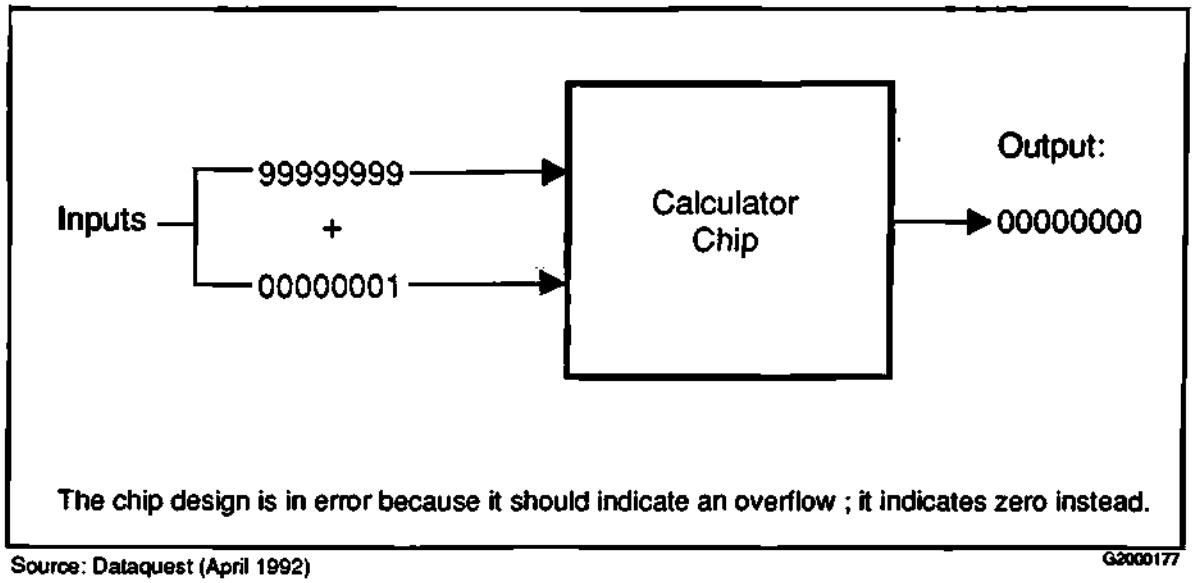
Basically, this specification was developed as an electronic equivalent to the traditional "bed of nails" tester that has long been used by PCB assemblers. The basic function of this tester has always been to catch opens, shorts and other problems caused by the assembly process; the function has never been to implement thorough chip test after board assembly. For this reason, Dataquest does not believe that IEEE 1149 makes it possible to build high quality MCM's without known good chips.

7.1 Component Test

A general rule of thumb is that it costs ten times as much to catch a mistake at the next level of assembly as it does to test it at the lower level. Thus, it is less expensive to test a chip than it is to test a chip once it is in the module. Similarly, it is ten times more expensive to find a bad module in the next assembly than it is to catch the mistake before the module is shipped.

Thus the key to low cost modules is thorough component test. This section discusses testing of the two components that go into an MCM: the chips and the substrate.

Figure 7.2.1
Incorrect Function of 8 Digit Calculator



Source: Dataquest (April 1992) G2000177

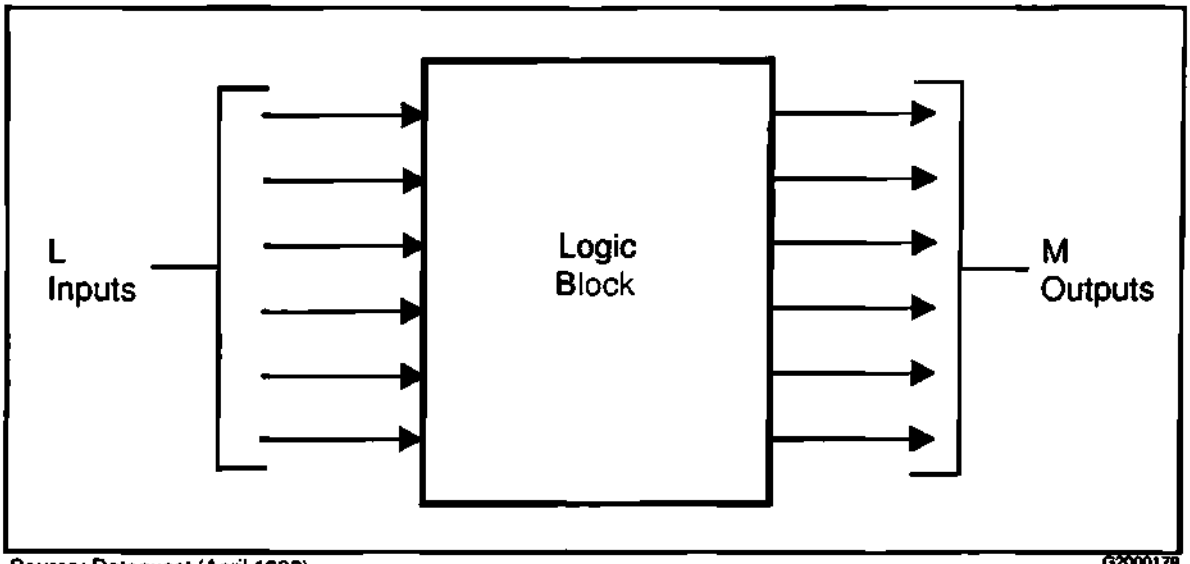
7.2 Chip Test

The theory of chip test is complex and has evolved over a period of 30 years. The next section discusses the theory of VLSI chip test and is intended for those who have no knowledge of the subject. Those who are well versed in the subject can skip this section.

The discussion of the next section includes:

- Testing a Complex Logic Function.
- Test Vectors.
- Stuck Faults.
- Storage Elements Complicate VLSI Test.
- Scan Logic.
- Built in Self Test (BIST).
- Test Generation Software.
- Summary.

Figure 7.2.2
Generalized Logic Function



Source: Dataquest (April 1992) G2000178

7.2.1 Theory of VLSI Test

It is important to know what VLSI test does not do: It (generally) does not catch design errors. Consider Figure 7.2.1 which shows a calculator adding 1 to a number consisting of eight nines. What the calculator should do in this case is to show an overflow. However, the design engineer forgot to include this case in his overflow criteria, so the calculator tries to carry the sum into the ninth digit. Since this digit does not exist, the calculator ends up displaying all zeroes -- clearly this is a long way from the right answer.

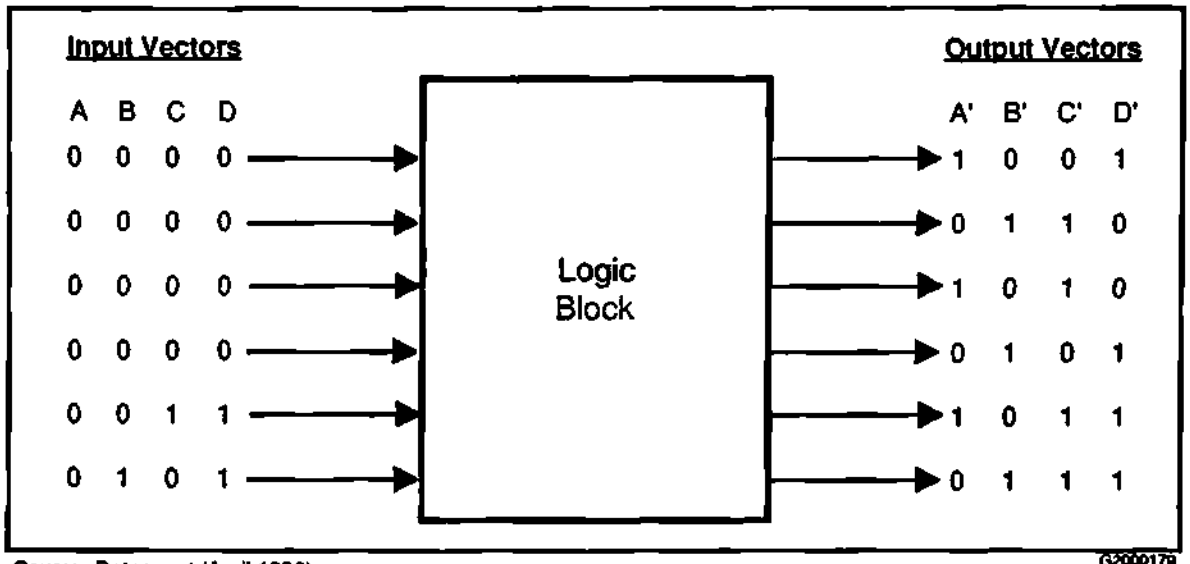
What the test generation will do is to develop test waveforms which, when applied to the calculator chip, assure that the chip is doing what it was designed to do: display all zeroes when it should display an overflow. The test generation methodology does not know what the chip is supposed to do, it only knows what logic gates should be on the chip and how they are hooked together.

While the situation in Figure 7.2.1 may look like a trivial case, it is common for chips to have design errors of this kind. This kind of error occurs commonly in microprocessors; some have several pages of design errors. Normally these errors are caught by running system level checks or test programs. Eventually, the logic is redesigned to eliminate the error and the chip test vectors are revised to verify that the new design is faithfully reproduced on all chips that are shipped.

Testing a Complex Logic Function

Figure 7.2.2 shows a complex logic block with L input pins and M output pins. This logic block has no storage elements, so the output is always the same for the same input, after a suitable propagation delay.

Figure 7.2.3
Illustration of Test Vectors



Source: Dataquest (April 1992)

One way to test this block would be to apply all possible input patterns to the input and then check to see that the output is correct for each input pattern. If the logic block has a lot of input pins, this procedure quickly becomes prohibitive. For instance, if the block had 50 input pins, and if we ran the input patterns in at a 100 megahertz rate, it would take 130 days to test this logic block.

Some knowledge of what is inside the block can simplify the test pattern considerably. For instance, suppose the logic block were broken into five unconnected logic blocks, each with ten inputs. In this case we could apply the same input pattern to each block and it would take only 512 nanoseconds to test the logic. Clearly, knowledge of what is in the logic block simplifies testing considerably.

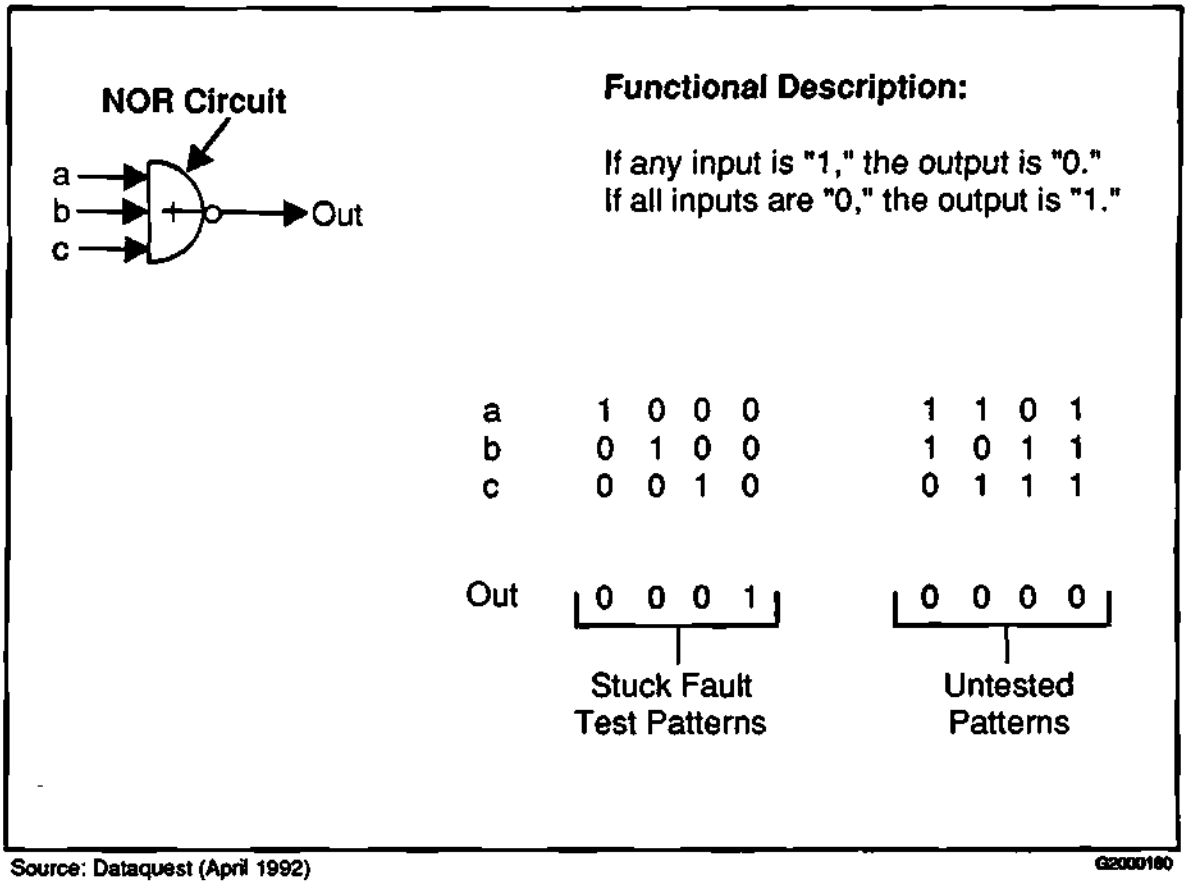
Today, test engineers have complete knowledge of the contents of the logic block and fashion their tests accordingly. Accordingly, generating tests for a pure logic block with no storage is relatively straightforward.

Test Vectors

Figure 7.2.3 shows a logic block with test vectors applied. In the figure the input test vectors A, B, C, and D are applied in sequence, and they give rise to the output vectors A', B', C', and D'. If the output test vectors appear when the appropriate input vectors are applied, the part is said to be good. The sequence of the vectors does not matter so long as there is no storage in the logic block.

Modern VLSI testers have vector files that are hundreds of megabytes. Typically these vectors are stored on hard disks. Each tester pin drives one pin of the VLSI part being tested and the pin electronics may have 32 megabytes of vector storage behind each pin. For high frequency testers, these vectors are able to follow one another at 50 to 100 megahertz.

Figure 7.2.4
Testing for Stuck Faults



Source: Dataquest (April 1992) G2000180

This amount of vector storage may seem excessive for testing pure logic, but when memory is added to the logic, the situation becomes much more complex. The reason for this is discussed in more detail in the following sections.

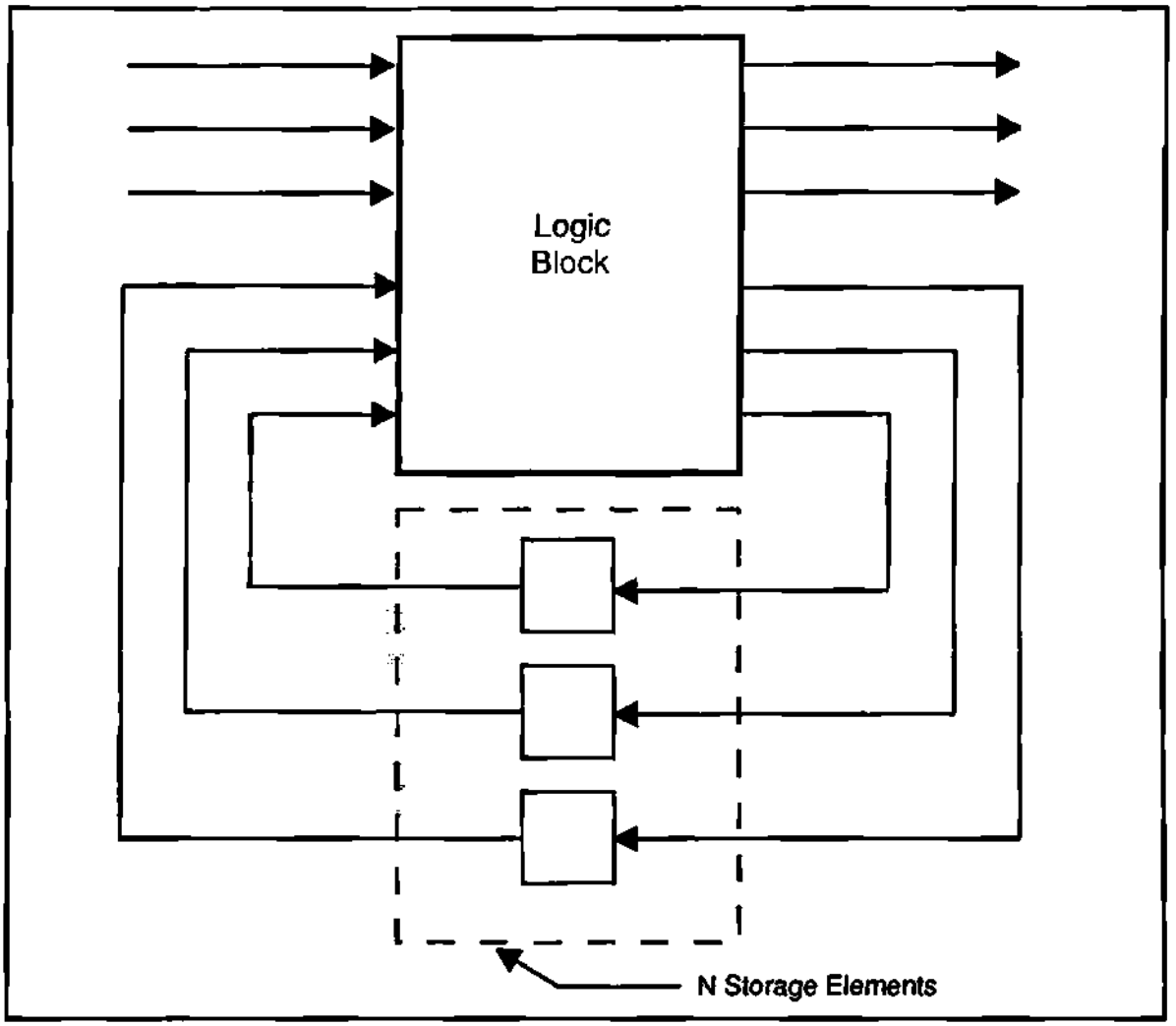
Stuck Faults

The idea of stuck faults is that the most common form of failure is to have a point in the logic shorted either to the power supply or to ground. For positive logic, a short to the power supply is regarded as "stuck at 1" and a short to ground is regarded as "stuck at 0."

The stuck fault tests for a three input "nor" gate are illustrated in Figure 7.2.4. A properly functioning gate will produce a "0" output if any input is at "1" and a "1" output if all inputs are at "0."

The stuck fault test patterns are shown in the figure. What they do is to apply a "1" to each input in turn to verify that the input is not stuck at "0" and that the input is able to pull the output to "0." Then "0" is applied to all inputs. If the output goes to "1" this indicates that the output is not shorted to ground.

Figure 7.2.5
Generalized Logic Function With Storage



Source: Dataquest (April 1992)

G2000181

This particular stuck fault test does not apply all possible patterns to the "nor" gate. In particular, it does not check to see that the output goes to "0" when two or more inputs are at "1." In this way, half the patterns for this particular gate do not have to be applied.

The savings in test vectors becomes more pronounced for larger gates. If an attempt was made to apply all possible patterns to a 50 input nor gate, test time would be 130 days as mentioned in the discussion of Figure 7.7.2. If only the stuck fault patterns were applied, all that would be required is that a "1" would be applied to each of the inputs in turn and finally, all "0's" would be applied to check that the output is not stuck at "0." In this way the test could be completed in only 51 vectors.

Fault Coverage

Once test vectors are generated, usually with the help of computer software, it is common practice to compute fault coverage. This is accomplished in the manner described below.

First, the test vectors are simulated on a computer which also simulates the logic being tested. If the input vectors produce the expected output vectors, the vectors are considered correct.

Next, a stuck fault is simulated in the logic to which the simulated test vectors are applied. If this stuck fault causes one of the output vectors to change, it means that that stuck fault is detected by the vector suite. If no output vector is changed, then that stuck fault is not detected.

In a complex logic network, it is possible that a stuck fault produces some vector change within the network but that vector change cannot be observed at the output because it feeds into some other logic element that has vectors applied that make it insensitive to that particular signal at that particular time.

The computer simulates every stuck fault, one by one. It counts the number of faults detected and computes the fault coverage as follows:

$$\text{Fault coverage} = (\text{Detected faults})/(\text{Total faults})$$

A test vector suite is usually considered complete only when the fault coverage is in the range of 95% to 100%.

Note that our 50 input "nor" gate would have to be simulated 52 times to compute the fault coverage. The first time it would be simulated with no faults to be sure that a good part actually tests good. Then it would be simulated with its 51 stuck faults – once for each input and once to see that the output is not stuck at "0."

Storage Elements Complicate VLSI Test

Figure 7.2.5 shows a logic block that has been modified to include storage elements. Here some of the logic outputs are fed into the storage elements and the outputs of the storage elements are fed back into the logic block. These storage elements are simple "D" type flip-flops. Their outputs take on their input values once every clock cycle.

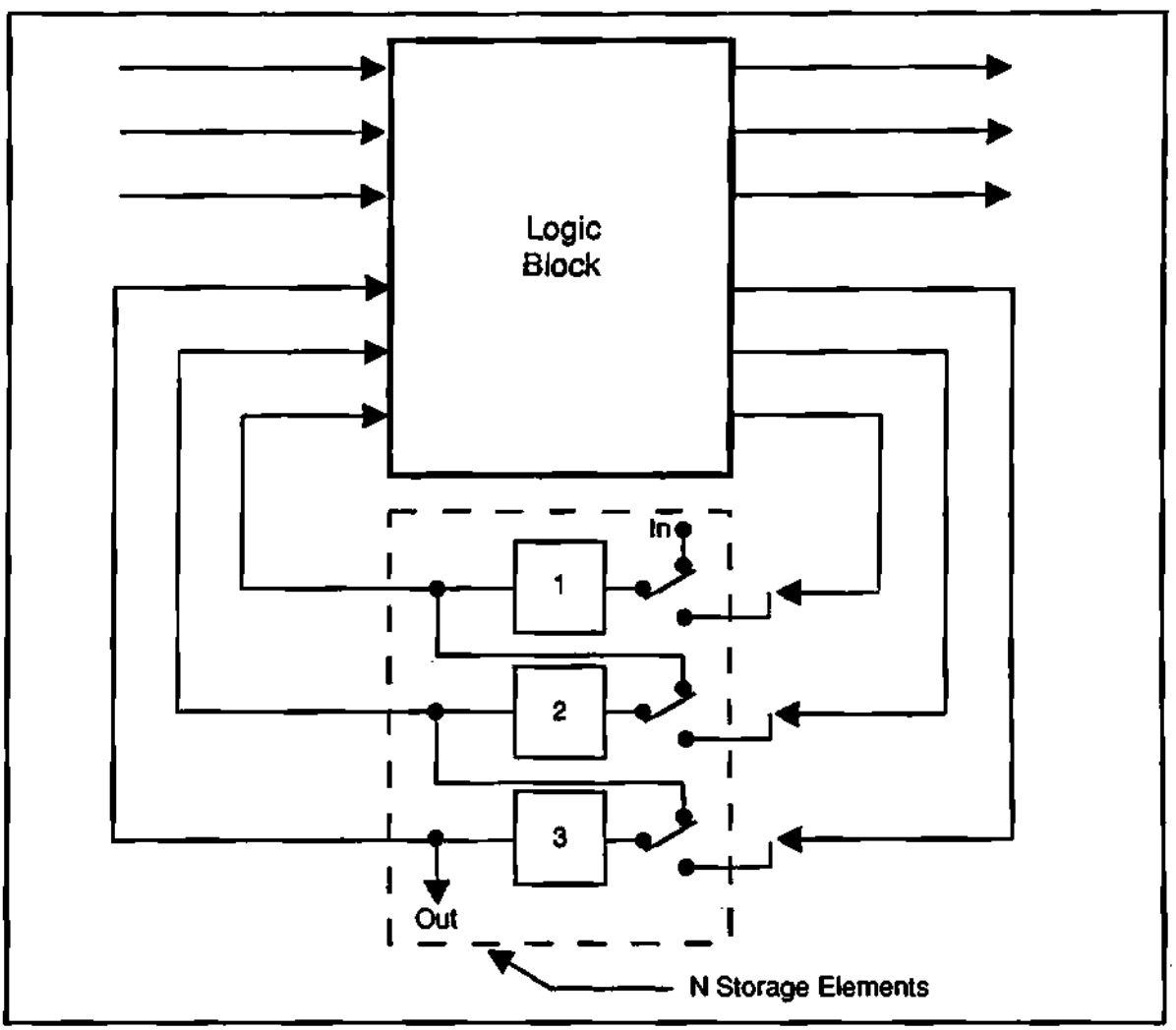
The addition of storage elements complicates the test problem considerably. First, some method of initializing these elements must be provided, for if there is no way to start them off in a known state, it is not possible to predict what will happen next.

Second, the storage elements act as input to the logic block. Their outputs are not a direct function of the signals going into the logic at this clock time. Instead their outputs depend on what was going into the logic a clock time ago and what vectors were being input to the logic at that time.

Depending on how the logic is designed, it may be very difficult to cause the storage elements to take on a desired pattern. If there are three storage elements, they can store up to eight patterns. If the elements are storing a given pattern, it may be necessary to step sequentially through all eight patterns to get from the current pattern to the one that is needed.

This situation gets considerably more complex when there are tens or even hundreds of flip-flops. Sometimes it is virtually impossible for software to generate the needed test vectors.

Figure 7.2.6
Generalized Logic Function with Scan Logic



Source: Dataquest (April 1992) G2000182

Scan Logic

Scan logic breaks the feedback path between the storage elements in the manner illustrated in Figure 7.2.6. Here a single pole double through switch has been put in front of each flip-flop (In a logic chip, the logical equivalent of this switch will be used). As shown in the figure, the first flip-flop is tied to an external input and the output of that flip-flop feeds the next flip-flop.

As illustrated in the figure, the flip-flop inputs are disconnected from the logic and connected to one another. It is a simple matter to sequentially feed in any desired pattern of "1"s and "0"s. In this manner,

the chip can be easily tested. Another advantage is that it is easy to use software to generate chip test vectors when scan logic is used.

The switches in Figure 7.2.6 are shown in the "test" position. When the chip is to be operated, the switches are thrown to the opposite position and the circuit of Figure 7.2.6 becomes identical to that of Figure 7.2.5.

A disadvantage of scan logic is that it requires extra logic to implement the switches. This logic may also slow the maximum clock rate at which the chip can run. Dataquest believes that as chips become more complex and as silicon becomes less expensive scan logic will become more common. Scan logic was originated at IBM and is used widely by them.

Scan logic should not be confused with boundary scan as specified in the IEEE 1149 specification. Boundary scan uses flip-flops that can be connected as a shift register like those of Figure 7.2.6. The difference is that the boundary scan flip-flops are at the input and output terminals of the chip while the scan logic flip flops are embedded in the chip logic. Boundary scan makes it possible to electronically disconnect the chip from its environment. If boundary scan is implemented but scan logic is not, the chip itself does not become easier to test.

Built In Self Test (BIST)

The idea of BIST is to store the chip test vectors (or some subset of them) in the chip itself. One way to do this is to store the vectors in a ROM. Another way might be to construct a specialized shift register that generates a sequence of test vectors that test the part fairly well. Some companies embed BIST circuitry in their macrocells so that when a chip is constructed out of an array of macrocells, it can be tested simply by enabling the built in BIST programs. Depending on the logic and the cleverness of the designer, BIST circuitry can be a lot simpler and require less extra silicon than scan logic.

Test Software

Software programs that help the designer develop test vectors are in common use. Verification software (discussed earlier) identifies stuck faults that are not detected by a test vector suite. Engineers can redesign their vectors to increase fault coverage as necessary.

Test generation software exists that can generate test vectors automatically for scan logic chips.

Software to generate test vectors for logic networks that include storage does not work in all situations. In fact, there are designs (such as uninitiallized storage elements) for which it can be shown that it is not possible to generate test vectors either by hand or by computer. Because of difficulties like these, most software is in use as a design aid.

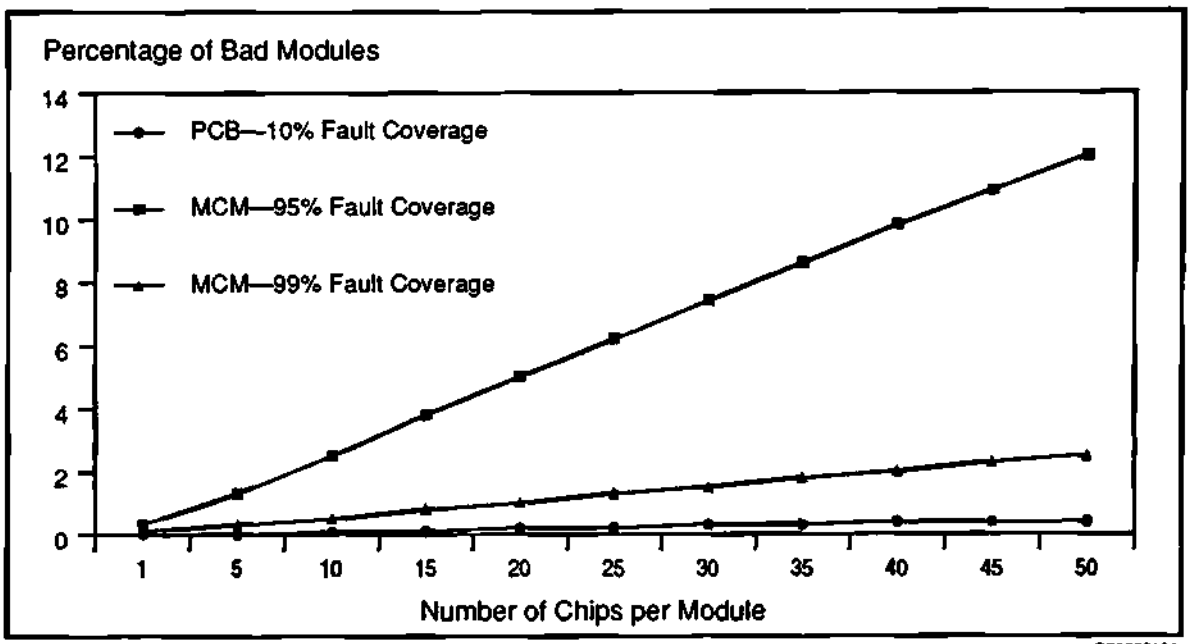
It is important that some thought be given to test before the design of a chip is frozen. If there is a part of the chip that is designed in such a way that it is difficult or impossible to test, it will be necessary to revise the design and serious schedule delays may result.

Summary

Chip test techniques have developed over a 30 year period. The current technique is to generate test vectors which detect stuck faults in the chip logic, with 95% to 100% fault coverage as the goal. If scan logic is used, software exists that can automatically generate chip test vectors. If scan logic is not used, available software may not be able to generate the chip test vectors which reach the desired fault coverage; in fact, chips can be designed in such a way that it is not possible to test them. In this case neither the test engineer or the software will be successful.

Test considerations should be made before the chip design is frozen to avoid possible redesign and schedule slips.

Figure 7.2.7
Module Defects vs Chip Count for PCB & MCM



Source: Dataquest (April 1992)

G20000183

BIST is used by some and is a substitute for scan logic.

Boundary scan is specified in IEEE 1149. This technique makes it possible to electronically disconnect the chip from its surroundings but does not necessarily make the chip easier to test. However, IEEE 1149 does support BIST and scan logic so that these test features can be activated using the extra pins specified in the standard.

7.2.2 Chip Test Problems

VLSI chips can be tested in package form to very high quality levels. However, the semiconductor industry does not attempt this level of quality for testing of unpackaged chips. Unpackaged chips are tested at wafer probe, and the criteria is that the test has to be good enough so that only a few packaged units are thrown away when the chips are tested again at final test.

Final test yields for mature chips are typically in the 95% to 99+% range, indicating that the wafer test quality is typically in this range. For packaged units, the quality level can reach 99.99%.

The difference between 99.99% quality and 95% quality is significant. As we will see, the lower of these quality levels complicates module testing considerably.

Impact of Chip Quality on Module Quality

The chips on a printed circuit board are not tested once they are put on the board since the incoming quality level is high enough that this is not necessary. An assembled PCB is usually given a simple functional test to see if it works, but this test is not exhaustive and may not be at speed. This test checks to see that the board was assembled correctly and not to see that the chips are working correctly.

If the board is not working, a "bed of nails" test may be used to find the component that is not correctly connected or is not working correctly. PCB board assemblers find that most of their inoperative boards are due to assembly errors: solder bridges, open wires, missing vias, or components in upside down.

If chips are of low quality, the quality of the MCM module or assembled PCB is impacted significantly. The formula below* relates module defect level to chip quality:

- DL = $[1-Y^{N(1-F)}]$.
- DL = Percentage of shipped MCM modules which may actually be bad.
- Y = Fraction of chips assembled which are actually good.
- N = Number of chips on module.
- F = Fault coverage of module test.

A graph of this formula is plotted in Figure 7.2.7. The graph for the assembled PCB case assumes that the PCB is constructed from Y = 99.99% good chips and that the fault coverage, F, is only 10%. As can be seen, this results in an assembled PCB defect level, DL, well below 1% even if there are 50 chips on the board.

The curves for MCM assume Y = 95% good chips (typical of today's wafer probed parts). As can be seen, the fault coverage at module test has to be much higher than 95% if the module quality is to be equal to that of today's assembled PCB's. This parity is reached when the fault coverage at module test reaches 99.9%

The implication of Figure 7.2.7 is that if chips are not tested thoroughly, then assembled modules will have to be tested in the same way that chips are now tested. This means a tester that works at high speed and is capable of handling five to fifty times the test complexity of today's VLSI testers. This is a specification for the VLSI tester of the year 2000 or maybe even 2010. Such a tester is not currently available, and if it were it could be prohibitively expensive. Current testers cost roughly $10,000 a pin and a MCM tester might be required to handle 1000 pins or more. Such a tester would cost at least $10 million.

The more feasible solution is to find a means of testing unpackaged chips to the same quality level that is achieved with today's packaged chips. The acronym for this level of chip testing is KGD, which stands for "known good die." The problem here is mechanical and not electrical. It has already been demonstrated that packaged units can be tested to very high quality levels. Unpackaged units will be tested to those same quality levels as soon as a means of making good electrical contact to the bare die is found.

It might seem that the IEEE 1149 test standard offers some help in improving the fault coverage of chips when testing at the module level. However, this standard was not developed to improve chip fault coverage. Instead, it was developed to implement an electronic "bed of nails" test as discussed in the next section.

IEEE 1149 will not ensure good chip fault coverage at the module level unless steps have been taken to go beyond the minimum test circuitry in the specification.

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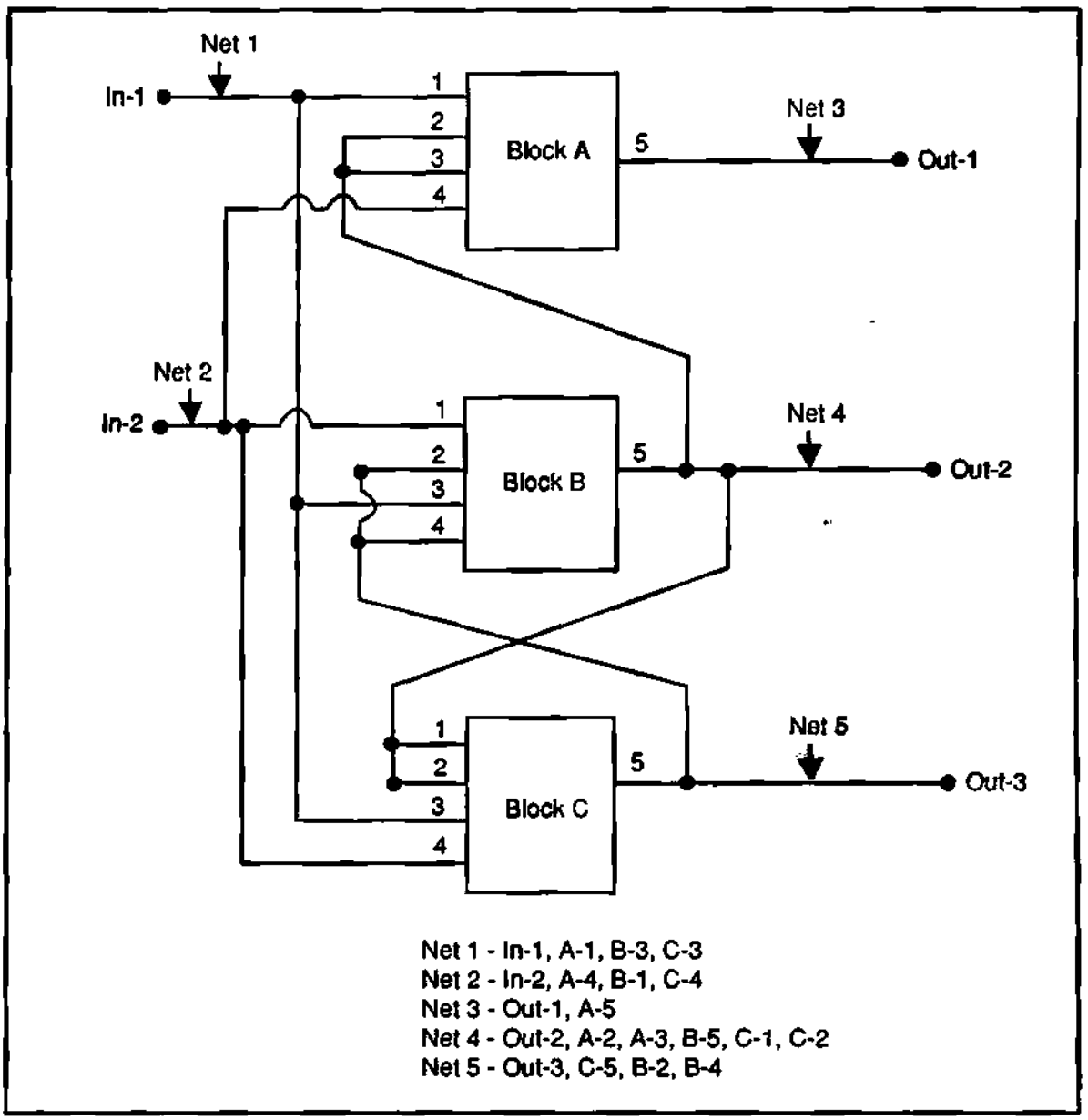
*"Thin Film Multichip Modules," Messner, Turlick, Balde, Garrou et al. ISHM 1992, page 506.

Figure 7.2.8
Logic Network with 5 Nets



Source: Dataquest (April 1992) G2000184

IEEE 1149 supports BIST and scan logic and where these extras have been implemented. If the chip has been specifically designed to be tested through the IEEE 1149 ports it is possible to achieve reasonably high fault coverage at the module level. Some have reported fault coverage as high as 95%. However, as Figure 7.2.7 shows, even 99% fault coverage may not be adequate for complex modules with more than 20 chips.

The IEEE 1149 Test Standard

Surface mount technology was the impetus behind the generation of the IEEE 1149 test standard. As surface mount was implemented, the traces on PCB's became smaller and it became more difficult to probe the PCB with a "bed of nails" tester. The IEEE 1149 specification provides for an electronic substitute for the "bed of nails" tester.

The "bed of nails" tester is used both for testing bare printed circuit boards and for testing boards on which components have been mounted. In the latter case it is used as a diagnostic tool and only tests boards which fail functional test. In both cases, the "bed of nails" tester checks to see that all nets are properly connected.

Figure 7.2.8 illustrates the concept of nets. Here, four logic devices are connected into five nets. A net is a wire that connects any or all of the following:

- An input pin which takes input from the outside world; for example IN-1.
- An input to a logic block; for example A-1 (pin one of block A).
- An output from a logic block; for example A-5 (pin 5 of block 1).
- An output pin which leaves the logic block to go to the outside world; for example OUT-1.

A "bed of nails" tester has a separate spring mounted metal pin for each connection point on each logic net. For the circuit of Figure 7.2.8, 20 such spring loaded pins would be required. The tester would then check to see that all the specified points were shorted together and that no net was shorted to any other net.

So far, we have described the "bed of nails" tests that might be performed on an unpopulated PCB. If the PCB is populated, the same tests are performed, but at a voltage low enough so that no diodes are driven into conduction. If there is a solder bridge that was caused between A-1 and A-2 when logic block A was soldered to the board, the "bed of nails" tester would quickly detect it.

Waveforms may also be applied through the bed of nails tester to check the parts functionally. These are at a higher voltage, and care must be taken when driving signals into one logic block not to destroy another logic block to which the first block is connected. For instance, when driving a signal into pins A-2 and A-3, care must be taken not to put excessive current into B-5, the output of logic block 5 to which this net is also connected.

IEEE 1149 calls for scan registers to be added to every input and output pin of every logic block. In Figure 7.2.8, this would make it possible for the tester to scan data into the register which drives B-5. The scan logic on pins A-3 and A-4 could then check to see that what is going into those pins is the same thing that is coming out of B-5. In this way the continuity of the net can be checked.

IEEE 1149 also calls for four pins to be added to each logic block. One of these is the input to the scan register, one of these is the output from the scan register, and the other two pins are used to control the scan logic. Scan logic is added to the chip so that the state of the input and output scan registers can be controlled.

The added silicon to implement IEEE 1149 is said to increase chip area from 5% to 25%. Clearly, the latter case may be viewed by some as an excessive penalty.

Scan logic can be used to test chips at the wafer level. The advantage is that only four connections need to be made to achieve a fairly thorough test. Such a test probably cannot reach 99.99% because it does not check the unprobed connection between the input bonding pad and the scan flip-flop. Such a test might, however, reach the 95% level needed for testing chips that are later to be packaged individually. This type of test would avoid the need to tool an expensive probe card of several hundred pins.

Requirements for Chip Test

Packaged chips can be tested to high quality levels. The test methods that are applied to packaged chips can easily be used for bare chips as soon as a reliable means of making contact to the bare chips is found.

Mature packaged chips can be shipped to high quality levels even without burn-in once the processes with which they are manufactured are stabilized. However, MCM's will employ leading edge chips that have not reached this level of maturity. It is likely that such chips will have to be burned in before they are put on an MCM.

The methods of contacting chips include various kinds of high frequency probes, TAB, ceramic carriers and various socket approaches.

7.2.3 Burn-In Test

Burn-in test is used to weed out chips subject to "infant mortality." These are the chips that would fail early when put into an operational environment. Burn-in catches these early failures by subjecting all the chips to accelerated environmental conditions. This may include a high temperature bake at 125° C together with some sort of electrical stimulation of the part. The electrical stimulation typically includes operation with applied supply voltages and some sort of waveform stimulation of the chip input pins.

Some burn-in requirements call for measurement of chip parameters before and after test. Chips may be rejected even though they are still working if these parameters change too greatly during burn-in.

If the process is new, it may be necessary to burn-in all chips before they are shipped. Clearly, this is expensive because of the labor required to put the chips in the burn-in sockets, the cost of the burn-in socket, the cost of the burn-in oven and the need for testing after burn-in.

As processes mature, burn-in is done on a sampling basis. In this case, a small percentage of the production is burned in to make sure that the basic process is not changed in a way detrimental to chip reliability.

Power dissipation in burn-in is not normally a problem for CMOS circuits since it is generally acceptable to burn in circuits at low clock rates where power dissipation is minimal.

Several firms are working on wafer level burn-in. Dataquest believes that the individual die on the wafer might be interconnected by metal traces in the scribe line that would automatically be eliminated when the chip is scribed. If wafer burn-in can be achieved it would be less expensive than a socket based burn in.

If chips are not burned in in wafer form, they will have to be burned in individually. This means that some kind of socket will be needed. One promising socket idea is to connect to the semiconductor die using gold bump contacts on a flexible membrane material. This sort of technology has been used in the DEC 9000 to connect MCM modules to the next level of packaging, and appears to have promise.

7.2.4 Chip Power Handling

As chip power increases, handling chip power during test will become increasingly critical, since, unlike the case of burn-in, chips must be tested at full clock rates. Currently, as indicated in the last chapter, many CMOS chips operate with power dissipations in the 5 to 10 watt range, and there is at least one microprocessor chip operating at 25 watts (the DEC Alpha). In the future, even higher power dissipation is expected.

Motorola has described a thermal chuck used in testing TAB mounted ECL devices.* This chuck has a thermal resistance of about 1.2° C per watt. As a result, the chip temperature is about 30° C above the temperature of the chuck. If the thermal resistance of the final package was the same, then the chip would also operate 30° C above its ambient environment in the final application.

Thermal chucks can also be used for testing at high and low temperatures such as -55° C and 125° C. It is relatively straightforward to heat or cool the chuck above and below room temperature. When testing at low temperature, care must be taken to avoid moisture condensation on the chuck as this can interfere with the thermal contact and the moisture can be detrimental to the chip in other ways.

If the chip is higher power, the same thermal chuck can still be used for testing. Suppose that the chip is 50 watts, and the the thermal resistance of its final package is 0.5° C per watt. In its final package, the chip will therefore operate at 25° C above ambient temperature. If room temperature testing is to be simulated, then the chip needs to operate at 25° C above room temperature (25° C) or 50° C.

Since the thermal resistance of the chuck is 1.2° C per watt, this means that the chuck will have to be 60° C (1.2° C per watt times 50 watts) below the desired chip temperature. Thus, operating the chuck at -10° C will compensate for the fact that the chuck has a higher thermal resistance than the final package.

The methodology described above will have some error which comes about from the fact that not all chips will have the same thermal resistance when mounted on the chuck, and not all chips will have the same thermal resistance when mounted in the package. If these errors are small, the temperature of the chip during test will be similar to the temperature of the chip when it is operating.

7.2.5 Chip Contact Techniques

As mentioned earlier, good chip testing can be accomplished only if there is a good way of making electrical contact between the bare chip and the tester. For the high frequency testing that will be required for most MCMs, this means that it will be necessary to maintain a transmission line up to within close proximity of the chip. Many solutions to this problem are being worked on including:

- High frequency probes.
- TAB.
- Ceramic carriers.
- Sockets.

High Frequency Probes

IBM has routinely been testing at speeds approaching 50 to 100 MHz for about a decade. Their probes use hybrid buckling beam probe points and are said to cost about $1000. The maximum number of probe points is a 27 by 27 matrix or 729 probe points. These probes make contact with the solder bumps used for IBM's C4 flip chip interconnect. Some damage occurs during probing, but this is eliminated by reflowing the solder bumps in a hydrogen reducing oven.

Cerprobe makes a ceramic probe that maintains a transmission line to within a fraction of an inch of the probe tip. This probe is said to have an inductance of 2 to 4 nanohenries. This is about the range that might

*"Production Test Fixture for 360 lead TAB Devices," Westbrook and Nelson, Proceedings of the 1992 International Conference on Multi-Chip Modules. Page 118

be expected for a wire bonded chip, so this probe should be adequate for any chips that are destined to be wire bonded. If the final package will have significantly lower inductance than the probe, the chip can still be tested if the test vectors are arranged to avoid simultaneous switching of a large number of outputs.

An epoxy ring probe card is also available. This is one of the most popular cards, but is not useful for high frequency applications.

Membrane probe cards have been developed by Tektronix and HP and licensed by HP to Probe Technology and Cascade Microtech. These cards use a flexible dielectric membrane which incorporates a printed transmission line together with bumps of gold or other metal which make contact with the pads on the wafer. The membrane might be actuated pneumatically or it might be backed by a rubbery material and brought into contact with the wafer by a vertical mechanical motion.

It is said that a transmission line can be maintained right up to the contact bump and that these membrane probes are capable of operating at frequencies over 2 Ghz. The membrane probes are more expensive than the epoxy ring card and may cost $5000 to $10,000 depending on the number of pins. The extra cost may be somewhat offset by the fact that maintenance on the membrane card is lower because it does not have to be planarized frequently.

The high frequency probes promise to solve the problem of bare die test, but they do not solve the problem of burn-in since they only make contact to the die for a short time during test. Some other means of contact will have to be achieved for burn in. This problem may be solved by wafer burn-in, or bare die test sockets may be used.

Tab

Tab is another way of making contact with semiconductor die. Here the tab frame is bonded to the chip and the chip is typically excised from the tab tape and mounted in a carrier or interposer. It is kept in the interposer through burn-in and test. Usually, the tab leads fan out so the lead pitch at the outside of the tape is 12 to 50 mils even though the pitch at the die may be in the range of 4 to 8 mile. Once the tabbed die is tested, it is often mounted on the substrate by hot bar soldering which reflows all the leads on one side of the tape at once.

The tooling for TAB can be expensive. Each new pattern of pads on a chip will require a tooling charge in the range of $5000. Other tooling items include the head for the tab bonders (both inner and outer leads), the bump mask set, the tool which excises the tab from the tape, the interposer and the test socket. All told, the tooling costs can run $15,000 to $25,000 or more.

Ceramic Carriers

The firm Chip Supply has suggested a chip on substrate technique for handling dice.* Here the chip is die attached and wire bonded to an inexpensive ceramic substrate. The substrate in turn is mounted in and wire bonded to a sacrificial package. The package is then tested. After test, the bond wires are pulled off both the package and the chip carrier. The combination of chip carrier and die is then considered to be a known good die (KGD). It in turn can be mounted on the final module. The bonding areas on the ceramic carrier are large enough so that they can reliably be bonded a second time.

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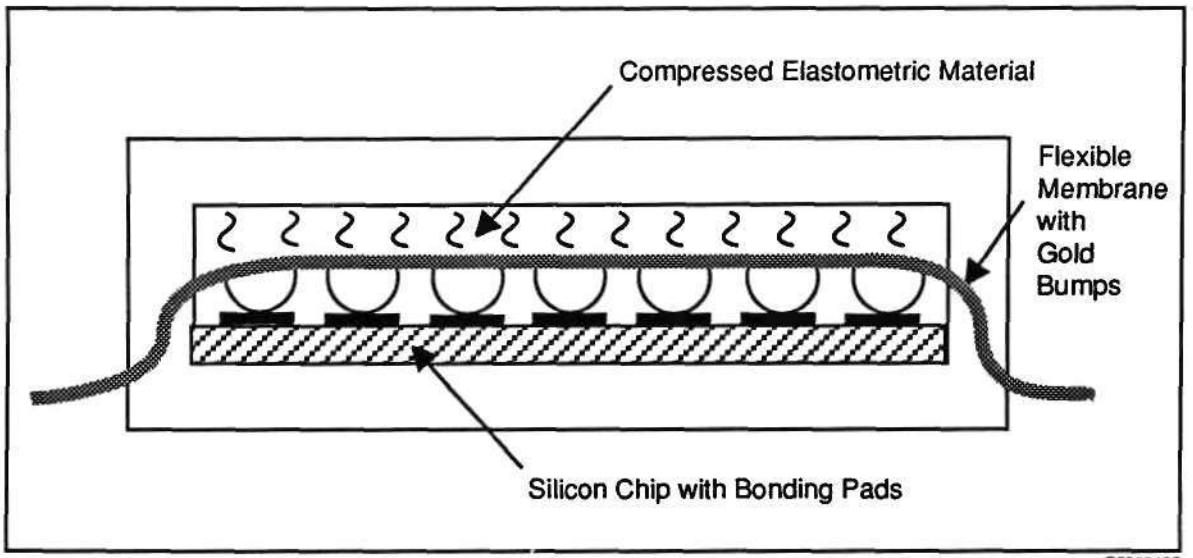
*"Methods for Processing Known Good Die," Smitherman and Rates, 1992 Proceedings of the International Conference on Multichip Modules. ISHM, 1992.

Figure 7.2.9
Membrane Socket for Chip Test



Source: Dataquest (April 1992)
G2000185

The advantage of this technique is that tooling is relatively cheap. The ceramic carrier can be designed so that it accommodates the chip bonding pads but fans out to pads that are standardized to fit a standard test socket. Thus the ceramic carrier is the only thing that has to be tooled. It is expensive and easy to tool because it can be implemented with only one layer of interconnect.

The disadvantage is that the sacrificial package adds cost. In addition, the ceramic carrier is in the thermal path and may add significant thermal resistance in some cases. There is also one extra bond wire in each lead. This wire may add enough inductance to impact performance significantly.

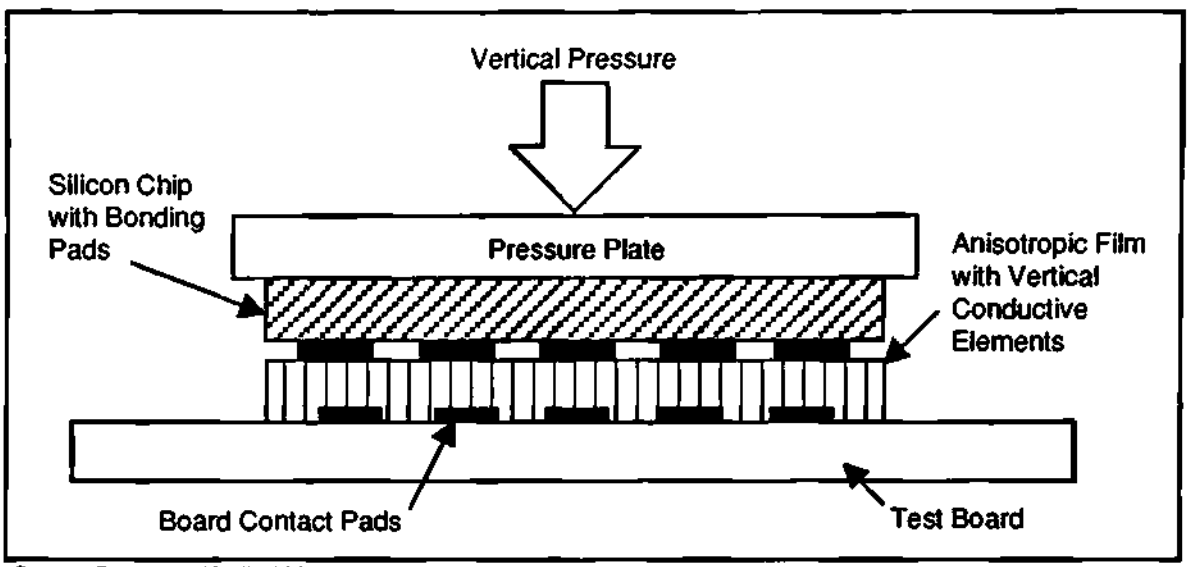
Socket Approaches

Gold bumps on a flexible printed circuit have been shown to be a reliable connection technique. This socket approach is illustrated in Figure 7.2.9. Basically, this concept is a variant of the membrane probe card described earlier. Unfortunately, the current high cost of the membrane probe card suggests that this socket technique may be quite expensive. If tooling is similar to that of the membrane card, tooling charges may be $5,000 to $10,000.

Socket cost will be much less than the tooling cost, and socket expense is justifiable if the socket is used only during test. If that is the case, only one (or possibly a few) socket is required and socket cost is spread over many chips.

Alternatively, the socket may be used for burn-in. In this case, each chip is in a socket for many hours and a great many sockets will be required to avoid bottlenecking the production flow. Burn-in sockets may be somewhat less than test sockets since they do not need to operate at high frequency.

Figure 7.2.10
Anisotropic Conductive Film for Chip Connection



Source: Dataquest (April 1992) G2000186

Anisotropic films offer another solution to the socket problem as illustrated in Figure 7.2.10. The idea of the anisotropic film is that it allows current to flow in the vertical but not the horizontal direction. The film is made up of an elastomeric material in which vertical conductive rods are embedded. Since these rods do not touch each other, they do not allow horizontal current flow. If the rods are close enough together, one or more rods will contact each chip bonding pad, with the result that low resistance is achieved.

The main advantage of the anisotropic film is that they allow for some degree of misalignment between the board and the chip. The disadvantage is that they may not be able to work with the smaller bonding pads. Adhesive anisotropic conductive films are also available for more permanent applications.

7.2.6 Other Chip Handling Issues

Since there is currently no market for KGD, there is no consensus or standard as to how to describe a device that is to be sold as a KGD:

- There is no agreement as to what a KGD data sheet should contain.
- There is no documentation of the chip size and location of the bonding pads.
- There is no description of the function of any bonding pads that are not specified in the product data sheet.

- There is no guarantee of quality.
- There is no assurance that the chip size and thickness will not change.

Prospective users of KGD also complain that vendors are reluctant to provide test vectors so that users can test the chips themselves. Dataquest believes that incoming inspection of packaged units is uncommon today, and for that reason most vendors do not have to provide test vectors. If a specification standard could be developed for KGD that included a guarantee of quality, it is likely that users would not need test vectors from their vendors.

Most microprocessors enjoy a product lifetime of eight years or more. During that time they fall rapidly in price and at the end of the period they may sell for 5% to 10% of their original selling price. This price reduction is achieved mostly through reductions in chip size. These reductions occur in several stages and ultimately result in an area reduction of 2:1.

Accordingly, if a product uses a microprocessor KGD, some provision must be made to accommodate chip shrinks. Depending on the means of contacting the chip at test, this may require retooling of probe cards and test sockets. Since this retooling would be done by the chip vendor, it can be spread over a great many die.

The user will also have to retool since the die may shrink two or more times during the product life. If the chip is wire bonded, some die revisions may be accommodated by the bonder itself – other times it may be more desirable to retool the substrate.

User product lifetimes are normally shorter than the lifetimes of microprocessors. If these lifetimes are on the order of 12 to 24 months, retooling may occur due to product enhancements and may represent no problem.

Manufacturers that make both semiconductors and MCM's seem to have no problems with bare die procurement since they control the chip design directly. Similarly, users of wafer foundries usually control the topology of the chips they design and are able to procure chips in wafer form with little difficulty.

7.3 Substrate Test

The purpose of substrate test is to verify net continuity and to verify that no net is shorted to any other net. Figure 7.2.8 shows a 5 net circuit. A substrate tester would probe each point in every net to make sure they are shorted together. It would then probe one point in every net to make sure no net is short to any other net.

Substrate test is usually done at DC rather than high frequency. It occurs before the chips are put on the substrate.

The techniques under consideration or being used for substrate test include:

- "Bed of nails."
- Glow discharge.
- E-Beam.
- Automatic Optical Inspection.

"Bed of Nails"

The "bed of nails" tester was so named because the test fixture is full of pins and looks just like the bed of nails that one sees an Indian fakir sleeping on in many cartoons. In these testers, there is one "nail" for each point on each net and they all make contact with the PCB under test simultaneously. The circuitry in the tester then tests for the appropriate opens and shorts as described above.

A single "bed of nails" fixture may have hundreds or even thousands of test points. This technique of contacting printed circuit boards has become impractical as surface mount technology has caused boards to shrink. The IEEE 1149 specification was developed to provide an electronic equivalent of "bed of nails" test.

Dataquest does not believe that the "bed of nails" test technique is a viable solution for MCM substrate test.

Two Point Probe

The two point probe tester has two "nails" or probe points that can be moved vertically or in any horizontal direction. Since there are only two probe points, these can be positioned very accurately if they are each driven by precision positioning mechanisms. The idea is to move the points around to sequentially test what the "bed of nails" tester does in parallel.

Accordingly, one probe will be positioned at some point in the first net. The second probe will sequentially probe all other points in that net to see that they are shorted to the first point. Then this procedure will be repeated for all other nets.

Once it has been verified that all points in each net are shorted together, the prober will then check to see that no net is shorted to any other net. First, one probe will be put on Net 1, then all other nets will be probed to be sure that none are short to Net 1. Then the probe will be put on Net 2 and all other nets will be probed to be sure that no other net is short to Net 2. This will be repeated until is is verified that no net is short to any other net.

The procedure of the previous paragraph can take a long time since the number of probes that must be made is proportional to the number of nets squared. Since 200 milliseconds may be required for each probe movement, testing can take a long time. For example, this test would require almost 8.9 hours on a 400 net circuit that could be implemented on a square inch of MCM-D substrate.

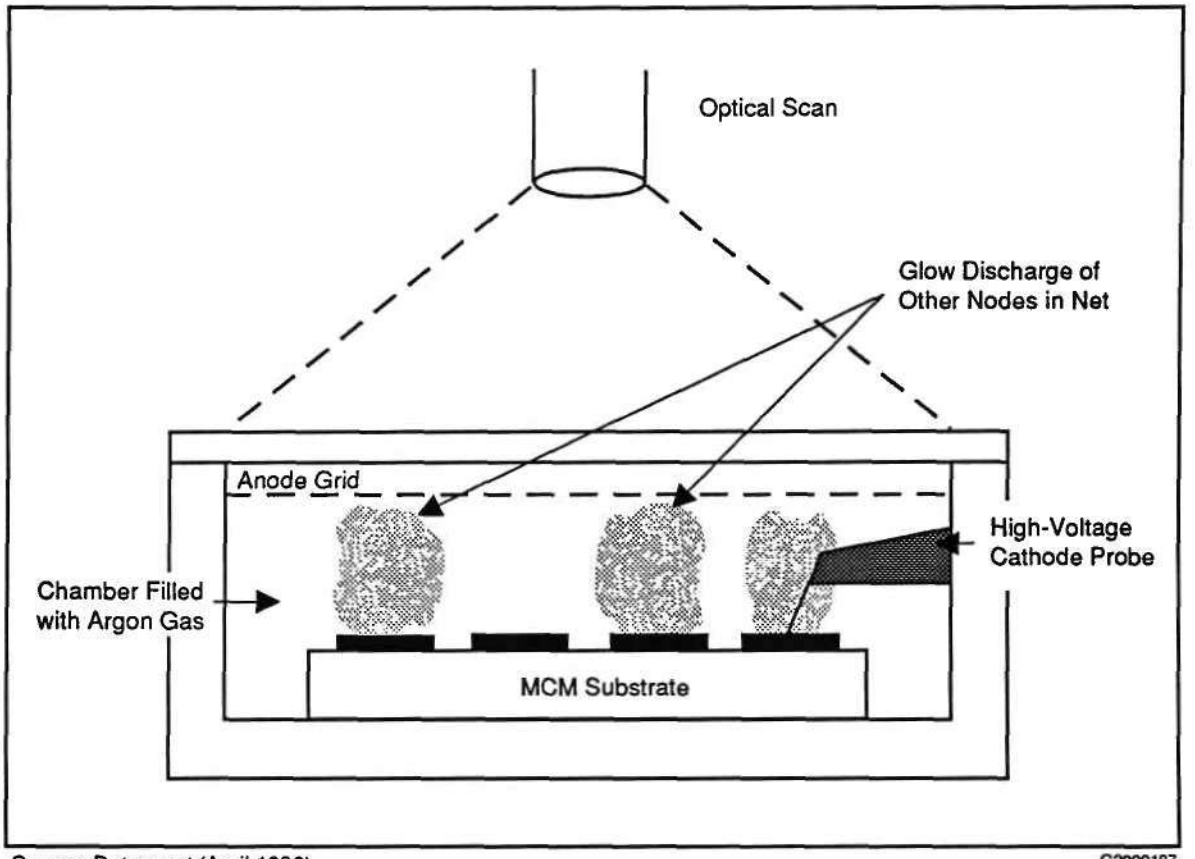
Since the test time is so long, manufacturers have sought other means of verifying that no net is short to any other net. It turns out that this can be accomplished through either rise time testing or capacitance testing.

The idea of capacitance testing is that each net has a certain capacitance. If two nets are shorted, they will both have the same capacitance, and this capacitance will differ from the capacitance of each net. Thus, nets shorted together can easily be detected by measuring capacitance. Since each net needs to be probed only once to measure capacitance, the time to probe will be proportional only to the number of nets rather than to the square of the number of nets. If this technique is used, test time for the 400 net circuit above can be reduced from 8.9 hours to 1.33 minutes.

Rise time testing measures the rise time of each net as it is charged through a known resistor. Since the rise time depends on the net capacitance, this method is equivalent to the one described above.

Two point probes cost about $150,000. They are suitable for low volume applications. Two manufacturers of these devices are Bath Scientific Limited of the U.K. and DIT-MCO of Kansas City.

Figure 7.2.11
Glow Discharge Testing of MCM Substrate



Source: Dataquest (April 1992)

G2000187

Glow Discharge

The glow discharge tester works on the same principal as the familiar orange colored night light. In this device, a voltage is applied to some point on each net and and opposite voltage is applied to a see-through screen in the manner indicated in Figure 7.2.11. An argon gas surrounds the substrate and this gas will glow at all points that are at the substrate voltage. It is an easy matter to check the continuity of a net because all points on that net will glow. It is also easy to check that no net is shorted to another net, because if the short did exist, both nets would glow.

An automatic optical sensing technique is used to check that the proper nodes are glowing as each net is indexed.

The probe still must be mechanically indexed from net to net in turn, but is is no longer necessary to check the continuity of each net in a separate series of probings.

Table 7.2.1
Comparison of Substrate Test Equipment Test Timed

Test System	Setup Time	Test Time*	
		1000 Nodes	4000 Nodes
Two Point Probe	5 min.	3.33 min	13.33 min.
Glow Dishcarge	2 min.	1.34 min.	5.35 min.
E-Beam	1 min.	.08 min.	0.8 min.

* The 1000 node application is similar to a 5-chip computer consisting of a CPU, 2 memories, one floating point unit, and an ASK. It can be wired on approximately one square inch of MCM-D.

Source: Dataquest, April, 1992

This technique was developed by testmatic. The rights to the product were acquired by MCC and in turn MCC licensed them to Alcedo of Sunnyvale, CA. This type of tester is currently in prototype form. Additional work with this concept is being done at Renssalear Polytechnic Institute.

E-Beam

The E-Beam tester makes use of the idea that an electron beam can be used either to charge or discharge a net. If the electron beam is of a certain energy, the electrons will stay on the net and it will charge to a voltage. If the electrons are of another energy, more than one electron will be emitted from the net for every electron that hits the net and the net will be discharged.

Once a net is charged, the voltage on the net can be detected by using the electron beam in voltage contrast mode. The procedure is to first discharge all nets. Then a single net is charged and an electron beam scans the substrate to be sure that only the right nodes are charged. This is repeated until all nets are checked. Test times are very fast using this method because the electron beam is not a mechanical device like the probe in the glow discharge tester. Because it is not mechanical, the electron beam can be very rapidly deflected from node to node.

A disadvantage of the E-beam test method is that the substrate must be tested in a hard vacuum. It takes 20 minutes to pump down the test chamber so the substrate can be tested and this pump-down can be the factor which governs test time. An alternative to this is to have a vacuum load station so that one substrate can be pumping down while another is being tested. In this way it should be possible to reduce the load time to one minute.

Developmental work on E-beam testers is underway at Hughes and MCC.

Table 7.2.2
Estimated Test Costs for
Substrate Test Equipment

Test System	Equipment Cost ($1000)	Hourly Rate[1]	Units/Hour[2] 1000 Node	Units/Hour[2] 4000 Node	Cost/Unit 1000 Node	Cost/Unit 4000 Node
Two Point Probe	$150	$45	3.60	1.64	$12.50	$27.50
Glow Discharge	$180	$48	19.48	4.08	$2.46	$11.76
E-Beam	$350	$65	27.78	16.67	$2.34	$3.90

[1]Assumes 5 year depreciation on 1 shift, plus $30/hour for operation, maintenance, and materials.
[2]Assumes 50% equipment utilization.

Source: Dataquest, April, 1992

Automatic Optical Inspection

Automatic optical inspection (AOI) is in common use in PCB manufacture today. In this application it is used more for in-process inspection than it is for final inspection. It is used to scan the individual layers of the PCB before they are laminated so that opens and shorts will not be buried on an inner layer of the PCB where they cannot be fixed.

Most likely, AOI will be used in the same way in the manufacture of MCM substrates. For this reason it is not a test technique that is competitive with the other substrate test methods described above.

Optrotec is one of the major suppliers of AOI equipment to the PCB industry. Employees of this firm have been in attendance at several MCM conferences. It appears that Optrotec is giving serious attention to this market.

A typical price for an AOI tester for PCB's is $500,000. It is unlikely that an AOI designed for inspecting MCM substrates will be identical to one used for inspecting PCB's. Possibly the MCM AOI inspection machine will be more expensive.

Summary

A comparison of the three important methods for testing MCM substrates is given in Table 7.2.1. Here the test times of the two point probe, the glow discharge and the E-beam testers are compared. Times are given for a 1000 node circuit and for a 4000 node circuit. As indicated, the 1000 node circuit could probably be fabricated on a square inch of silicon. All of these figures assume that the 1000 node circuit has 400 nets and the 4000 node circuit has 1600 nets.

Table 7.7.2 gives an estimate of the comparative test costs for each of the three tester types. Here the hourly rate for the tester is computed by assuming a five year, one shift depreciation schedule and adding $30 per hour for operator time, maintenance time and materials. The throughput calculations assume that the tester is in actual use only 50% of the time. The rest of the time it is being repaired or maintained or is sitting idle because no substrates are available for test. This usage percentage is typical of semiconductor manufacturing equipment.

Table 7.7.2 indicates that the two point probe tester is relatively expensive when compared to the other two methods. Glow discharge is competitive with E-beam for the relatively simple 1000 node circuit, but considerably more expensive for the 4000 node circuit.

As it stands today, the two point probe is operational, the glow discharge equipment is developmental and the E-beam is experimental. Stated succinctly, the two point probe is currently the only game in town.

If it is assumed that the 1000 node circuit is a square inch, then the two point probe test cost for that circuit is $12.50. Clearly, it will be difficult to build this circuit for $11.00 a square inch if the test cost alone is more than that. Things get a little better if the tester is used on three shifts. In this case the hourly rate is reduced to $35 an hour and the substrate can be tested for $9.72.

The E-beam tester benefits much more from being used on three shifts. In this case the hourly rate is reduced to $42.00 and the test cost for the 1000 node circuit falls from $2.34 to $1.51. If MCM-D is to meet the target cost of $11 per square inch something like the E-Beam tester will have to be implemented for substrate test.

Of course, it doesn't do any good to run any of these testers on three shifts if there is not enough business available to fill the tester on one shift. The number of substrates it takes to fill each tester on one shift is indicated below (The lower number assumes the larger substrate while the larger number is for the larger substrate):

Two Point tester	3,200 to 7,200 substrates/yr.
Glow Discharge	8,000 to 39,000 substrates/yr.
E-beam tester	32,000 to 56,000 substrates/yr.

7.4 Module Test

Most assembled PCBs work the first time. It is common to find 95% to 98% of the assembled PCB's to be good. Rework problems can often be detected by manual or X-Ray inspection. Where necessary, a "bed of nails" test can be used on the finished PCB. If only a continuity check is to be done, this test can be run at a low voltage to avoid damaging any components.

The final test of the assembled PCB is usually a simple functional test. For instance, if the PCB were to be used in a calculator, the board might be checked by inserting it in a finished unit and trying a few add, subtract, multiply and divide examples to see that the unit works. This sort of test is not thorough, but is adequate since most of the components have been stringently tested by the vendors which supply them.

Shrinking PCB line widths have made it difficult to construct "bed of nails" testers that can successfully contact all the nodes on a typical PCB. The IEEE 1149 specification was specifically constructed to provide a substitute for "bed of nails" testing.

7.4.1 Test Requirements

The discussion of Figure 7.2.7 explains why it is almost mandatory to have known good die (KGD) before assembly of die to an MCM substrate. Basically, if the chips are known to be good, high MCM quality levels can be assured even though only a simple pass/fail functional test is implemented after MCM assembly.

Failed modules may need to be repaired. However, the percentage of failed modules will be small if KGD are used in MCM manufacture. If module failure rates are in the 3% range it may be simpler just to discard the bad modules.

Repair of bad modules requires first that the module be repairable and second, that there is some way of finding the assembly mistake or bad component that caused the module to be inoperative.

Repairability places an additional constraint on module design. If wire bonding is used, larger bonding pads may be required so that after one wire is removed there is still enough room to put down a second wire. If TAB is used, there may be a requirement that the outer lead bond be soldered rather than thermocompression. The requirement for solder may require that the outer lead spacing be larger than it would otherwise need to be.

IEEE 1149 will make it possible to do fault location on modules that fail functional test. This is discussed in the next section.

7.4.2 IEEE 1149

IEEE 1149 specifies scan shift registers at every input and output of a VLSI chip. It also provides for four extra pins on the chip that make it possible to load data in, take data out and control where the data goes.

If all the chips on an MCM implement IEEE 1149, it is a simple matter to find the fault or faults that cause the module to fail functional test. Continuity of interconnect can be verified by putting a known pattern on all the chip outputs and checking to see that they reach the appropriate chip inputs. If some outputs go the module connector, they can be easily checked at that point. In this way, a failure of the interconnection between chips can be detected.

Scan registers can also be used to check chip function. In this case, Input patterns are applied to the chip and the chip outputs are stored in the output scan registers. These can be shifted out and compared to the specified test vectors to see that the chip is working properly. If chips have been thoroughly pretested before assembly, this test does not need to be exhaustive. As indicated in Figure 7.2.7, even 10% fault coverage may be adequate.

Several firms have developed personal computer based testers that are adequate for exercising an assembled module in the manner described above. These testers may not operate at the full clock rate of the module, but they are acceptable for running the types of tests described above. High frequency testing should not be necessary if the components themselves are tested at high clock rates.

Identification of assembly errors or faulty components becomes much more difficult when some or all of the chips on the MCM are not constructed according to IEEE 1149.

If only a few chips do not meet the IEEE 1149 specification, it may be possible to partially test these chips by exercising them through the output scan registers of chips that do implement IEEE 1149. Alternatively, optical, X-Ray or E-Beam inspection may be used to find assembly errors like open or bridged traces.

Table 7.5.1
Intraconnect Issues

Intraconnect	Advantages	Disadvantages
Wire Bond	Little tooling expense Adapts to different chips Accomodates chip changes Cost about 1/2¢ per lead	Chip replacement difficult Probing for chip test not developed High lead inductance Pad spacing less than 4 mils difficult
TAB	Test sockets available Repairable soldered outer leads Low lead inductance Lead pitch down to 2 mils	Tooling & fixtures $10-25 K New chips need new tooling Chip shrinks need new tooling Cost/pin 1-2¢ for high pin counts
Solder Flip-Chip	Proven Process Area array contacts Low lead inductance Repariable Chip test demonstrated Cost per bump wire bond	8-10 mil bump pitch Tooling & fixtures $1-5K New chips need new tooling Chip shrinks need new tolling
Resin Flip-Chip	1-3 mil bump pitch Area array contacts Low lead inductance Repairable	Developmental New chips need new tooling Chip test not demonstrated

Source: Dataquest, April, 1992

TI offers a line of buffer chips that implement the IEEE 1149 specification. If every chip on the module that does not implement IEEE 1149 has one of these buffers on every input and output line, the module will be as easy to test as if every chip implemented the specification directly. The disadvantage is that the addition of the buffer chips adds cost and increases delay. In some cases, buffer chips may be required for other reasons, and it should be an easy decision to make these IEEE 1149 type buffers. In other cases, the addition of a few buffer chips with scan logic may simplify testing so much that the extra cost is justified.

7.5 MCM Interconnect

The four major categories of chip to MCM substrate connection shown in Table 7.5.1 are wire bond, TAB, solder flip-chip, and resin flip chip.

Wire bond is the most mature technology. Current wire bonders are able to visually sense the chip location and can compensate for any misplacement of the chip on the substrate. They can be "taught" the location of substrate and chip pads by simply bonding one device. This makes it possible to rapidly adapt the

bonder to new bonding patterns and to changes in bonding patterns due to design modifications. A major disadvantage of wire bond is that there is currently no accepted method for testing bare die to find KGD.

TAB has the advantage that test and burn in can be accomplished through use of the appropriate sockets. It suffers from the disadvantage that costs per lead are higher and significant tooling costs may be required.

Solder flip-chip was developed by IBM many years ago. This is a proven process for which the problem of KGD has been solved. By all reports it is a proven process with a very high rate of good connection. Reportedly, it is less expensive than wire bond and the tooling and fixturing requirements for new designs are modest.

Various resin flip-chip processes are in development, many of them in Japan. The idea of these processes is that gold bumps with a very fine pitch are put on the chip. The chip is then flipped and connected to the substrate with a resin. In some cases this resin is an anisotropic conductor (see the discussion of Figure 7.2.1) and in other cases the gold bumps are brought into contact with the substrate by a combination of pressure and shrinkage of the resin.

7.6 MCM Packaging

The three ways to seal an MCM module are hermetic, glob top, and by transfer molding.

Hermetic sealing is often accomplished with MCM-C or through use of a ceramic package in which the MCM module is mounted. Usually, dry nitrogen is sealed inside the hermetic package and the lid which seals the package is solder sealed. These packages are tested for leaks after sealing. They are often preferred for military applications. Hermetic packages are avoided in commercial applications because they tend to be expensive.

Glob-top encapsulants (GTE) are most often used with MCM-L modules. Typically, the GTE material consists of epoxies or silicon gels. Normally, each individual chip is separately encapsulated. Sometimes there is a circular ring or dam around each chip to keep the encapsulant from flowing in an unpredictable manner. The GTE material is normally liquid when it is applied and is hardened during curing at some elevated temperature.

GTE materials have been used for many years. They have been quite common in electronic watches since the late 1970's. Needless to say, the environment seen by a watch is not as severe as some of the industrial environments that are seen by other chips. For this reason, the reliability requirements for GTE parts were not as high as for other VLSI chips.

The original GTE materials did not offer the reliabiltiy of transfer molded epoxy packages. More recently, GTE materials have been improved. Many feel that they will be competitive with transfer molded epoxy in the next several years.

Transfer molded epoxies have been used for many years to encapsulate LSI and VLSI devices. Originally, this technology was regarded as a low cost, low reliability alternative to hermetic sealing. Steady reliability improvements have been made over the years until, today, transfer molded epoxies have well over 80% of the encapsulation market. Their reliability is well documented and they are the standard by which GTE will be judged.

One MCM package technique that is gaining in popularity is the Multi-Chip Package (MCP). The idea here is that several chips can be mounted on a small printed circuit board which is in turn attached to the lead frame of a standard plastic package such as a quad flat pack (QFP). The whole assembly is then put into the QFP transfer mold and epoxy is injected in the normal manner.

The positive features of the MCP are that, for the most part it uses the same tooling as the QFP it is mounted in. In addition, it is encapsulated using tried and true transfer molded epoxy so that reliability considerations are minimized as compared with GTE. Dataquest believes that MCP is gaining rapidly in popularity.

7.7 MCM Reliability

In theory, MCM reliability should be higher than the reliability of a functionally equivalent module constructed with standard chip-per-package technology. This arises from the fact that a high percentage of device failures arise from the interface between levels of interconnect. Since the MCM eliminates a level of interconnect, it should be more reliable.

Some factors that would lead to a lower reliability for MCM include the following:

- Power densities are higher, leading to higher chip temperatures.
- Bonding pads are smaller and closer together, leading to problems with interconnect reliability.
- New, unproven materials are being used in MCMs.
- Mismatches in thermal expansion coefficients may cause warping and cracking.

A fair amount of work, both military and commercial, is being done to verify the reliability of MCMs. Dataquest believes that a user of MCMs today can expect them to be as reliable as the PCBs they replace. Users should work closely with their vendors to assure themselves that the MCM technology being used has had enough testing to reasonably assure them that the part will be reliable in its operating environment.

7.8 MCM Costs

The purpose of this section is to show relative costs for a typical simple MCM module. The module in question is the same one that is illustrated in Figure 6.2.3 and Table 6.2.3. It is a five chip module consisting of a CPU, a floating point unit, an ASIC and two SRAM chips. In its MCM-D version, the substrate is approximately 1 inch by 1 inch.

The PCB "board stuffing" business offers an interesting analogy to MCM assembly. In this business, the margin between the selling price of the finished module and the cost of the components and the bare PCB is normally in the range of 15% to 25% of the selling price. Margins are narrow, and some PCB assemblers make their profit by procuring components at a lower price than their customers.

Table 7.8.1 provides estimated comparative costs for three types of MCMs: MCM-L, MCM-C and MCM-D. In this table the die costs are estimated by assuming a wafer cost and yields that would be typical of a VLSI component that is about a third of the way through its life cycle. For a microprocessor with an eight year life, these chips might be in their second year of production.

The test cost of $9.00 for the five chips is taken at 15% of the chip cost. This is typical of final test costs which are usually 10% to 15% of the selling price for reasonably mature products. A basic assumption here is that that some method has been found to make contact with the chip so that the final test can be run on the bare die. As discussed earlier in this chapter, the probe cards or sockets to accomplish this are still developmental.

Package cost assumes a simple GTE for the MCM-L, a soldered lid for the MCM-C and a 160 pin transfer molded QFP for the MCM-L.

Table 7.8.1
CPU Module Cost Comparison for
Three Substrate Types

Item	Substrate Type MCM-L	MCM-C	MCM-D
Net die cost (Total for 5 Die)	$60.00	$60.00	$60.00
Die Test Cost (15%)	9.00	9.00	9.00
Known Good Die Cost	$69.00	$69.00	$69.00
Substrate Cost[1]	10.50	28.00	32.00
Package Cost[2]	.50	1.00	8.00
Direct Material	$80.00	$98.00	$109.00
Assembly Labor	10.00	10.00	14.00
Functional Test	2.00	2.00	2.00
Rework	5.00	5.00	5.00
	$97.00	$115.00	$130.00
Markup on value-added (100%)	17.00	17.00	21.00
Minimum selling price	$114.0	$132.00	$151.00

[1]From Table 6.2.3

[2]Assumes 1000 plus on the 5 chips, 400 pins on the module. Labor is 1¢ per pin.

[3]Assumes 99.99% good chips, 5% rework rate for assembly errors. Rework cost is $100.00.

Source: Dataquest, April, 1992

Functional test is done on a personal computer based tester that costs $50 per hour, including the operator. The tester throughput is 25 units per hour. The rework rate is assumed to be 5% and rework costs are estimated at ten times the cost of direct assembly labor.

It is interesting to note in Table 7.8.1 that MCM-L is the least expensive method. The cost of the other two options is not too far from MCM-L considering how much more expensive the substrates are.

Table 7.8.2
CPU Module Cost Comparison for
Packaged Units on a PCB

Item	Cost
Net Die Cost (total for 5 die)	$60.00
Die Test	-------
Die Package(1¢/lead)	10.00
Die Assembly (1¢/lead)	10.00
	$80.00
Packaged Test Cost	9.00
	$89.00
Final test Yield	95%
Yielded Cost	$93.68
Markup on Value Added (100%)	13.68
Minimum Component Selling Price	$107.36
PCB Cost (Table 6.2.3)	6.53
Labor to Assemble	5.00
Rework (5%; 10x)	2.50
Total	$121.39
Markup on value added (100%)	14.03
Minimum Selling Price	$135.42

Source: Dataquest, April, 1992

For comparison purposes, Table 7.8.2 estimates the cost of single chip packages packaged on a printed circuit board. Notice that the packaged chips at $107.36 are more expensive than the bare die of the previous table at $69.00. Today, semiconductor manufacturers are not willing to sell bare die at all, much less that cheaply. However, a manufacturer that makes both die and MCMs presumably would see the kinds of costs illustrated in Table 7.8.2.

Dataquest believes that a high volume MCM manufacturer would be able to procure bare die at costs similar to those of Table 7.8.1. This is somewhat similar to the situation of the PCB assembler that is able to buy components cheaper than its customer.

Table 7.8.3
CPU Module Comparisons

Item	PCB	MCM-L	MCM-C	MCM-D
Relative Cost	118%	100%	116%	132%
Relative Size	200%	100%	38%	19%
Relative Clock Rate	80%	100%	118%	130%

Source: Dataquest, April, 1992

It is assumed that the PCB assembly labor is somewhat less than the MCM assembly labor – $5.00 as compared to $10.00. Even so, the total cost for the fully assembled PCB comes to $135.42. This is comparable to the price of MCM-C and considerably more expensive than MCM-L.

The pricing of MCM-L parts in the market today seems to verify the conclusions of Tables 7.8.1 and 7.8.2. Some MCM-L manufacturers will sell their modules in high volume for the same price as the chips individually packaged. This means that the user can buy the chips already hooked together for the same price as individually. Since the user will have to pay to hook the chips together, the MCM-L is a less expensive alternative.

Table 7.8.3 makes some comparisons for the four different module types. These include relative cost, relative size, and relative clock rate. In all cases, the MCM-L option is the standard by which the other techniques are judged.

MCM-L is the lowest cost. The PCB and cofired ceramic options are 18% and 16% more expensive, respectively. The high density option is much more costly and commands a 32% premium. In spite of this it should be attractive in some applications because the clock rate is 30% higher and the module is less than one fifth the size of the MCM-L option.

The MCM-C option should also enjoy some popularity, despite its higher price, because it offers a 63% size reduction and a 118% clock rate improvement as compared to MCM-L.

Appendix A

Introduction

Dataquest has gathered qualitative data from major electronic systems, semiconductor, materials, and contract assembly companies worldwide to determine their multichip module capabilities. The list of companies and the services offered are shown in Tables A1 and A2. The vendor profiles highlight the product lines of companies that participate in the multichip module market.

Table A-1
MCM Vendor Services

Company	Headquarters	Design	Fab	Test	Burn-in	MCM Status MCM-L	MCM-C	MCM-D	MCM Consumption Merchant	Captive
Alcoa	United States	x	x	x	x		x	x	x	
Amkor/Anam	Korea	x			x	x			x	
AT&T	United States	x	x	x	x		x	x	x	x
Boeing	United States		x	x	x		x			x
Burr-Brown	United States	x	x	x		x	x		x	
CNET	Europe	x	x	x	x		x			x
Coors Elec. Packages	United States	x		x	x		x	x	x	
Dassault Electronique	Europe	x	x	x	x		x	x		x
DEC	United States	x	x	x	x		x	x	x	x
Dense-Pac	United States	x		x		x	x		x	
Fujitsu	Japan	x	x	x	x		x	x	x	x
GEC Plessey	Europe	x	x	x			x			x
Hestia Technologies	United States	x		x		x			x	
Hewlett-Packard	United States	x	x	x	x		x	x		x
Hitachi	Japan	x	x			x			x	x
Hughes	United States	x	x	x	x		x	x	x	x
Ibiden	Japan	x		x		x			x	
IBM	United States	x	x	x	x		x	x	x	x
IMI	United States	x		x		x	x		x	
Irvine Sensors	United States			x	x		x		x	
Kyocera	Japan	x	x	x			x	x	x	
LSI Logic	United States	x	x	x	x		x		x	
Mitsubishi	Japan	x	x	x	x	x	x		x	
McDonnell Douglas Corp	United States	x	x	x	x			x		x
Motorola	United States	x	x	x	x	x	x	x	x	x
Multichip Technology	United States	x		x		x			x	
nChip	United States	x	x	x			x	x	x	
NEC	Japan		x	x	x		x	x	x	x
Northern Telecom	Canada	x	x	x	x	x	x	x		x
NTK	Japan	x		x			x	x	x	
NTT	Japan	x					x	x		x
Oki	Japan	x	x			x			x	
PMC	Canada	x		x			x			x
Polycon	United States	x		x			x		x	
Printron	United States	x		x				x	x	
Rockwell	United States	x	x	x	x		x	x		x
Samsung Corning	Korea	x	x	x		x	x		x	
Siemens	Europe		x	x			x			x
Silicon Connections	United States	x					x		x	
SMI Ceramics	Japan	x					x		x	
SMOS/Seiko Epson	Japan	x	x	x		x				
Staktek	United States	x		x		x			x	
Tektronix	United States	x		x			x		x	
Texas Instruments	United States	x	x	x	x		x		x	x
Thorn-EMI	Europe	x		x			x	x		x
Toshiba	Japan	x	x	x		x	x	x	x	x
Unisys	United States	x	x	x	x		x	x		x

Source: Dataquest, April, 1992

Table A-2
Substrate Suppliers - 1992

Company	Headquarters	Alumina	Aluminum Nitride	Beryllium	Glass-Bonded Ceramics	Diamond	Mullite	Sapphire	Silicon Carbide	Silicon
Abar Ipsen Industries/ TI Group PLC	Europe	x					x			
Abrasive Finishing Inc.	United States								x	
Advanced Refractor Technology, Inc	United States		x							
Alcan	United States		x	x						
Aremco Products Inc.	United States	x					x			
Ashai	Japan				x					
Boride Products Inc/ Dow Chemical	United States								x	
Brush Wellman	United States			x						
Carborundum/BP	Europe		x						x	
Ceramatec Inc.	United States	x								
Ceramtek	United States						x			
Ceradyne Inc.	United States			x						
Ceratronics	United States		x							
Chichibu Cement Company	Japan						x			
Colorado Refractories Corp	United States	x								
Coors Ceramics Company	United States	x	x						x	
Cordec Corporation	United States								x	
Corning, Inc.	United States				x					
CPS	United States	x	x							
Crystallume	United States					x				
Denka	Japan		x							
Diamond Materials Institute	United States					x				
Du-Co Ceramics Corp	United States	x					x			
Duramic Products, Inc.	United States	x								
Enprotech Corp	United States	x								
Exolon-ESK Company	United States								x	
Ferro Corporation	United States	x	x				x		x	
Form Physics Corp	United States	x								
Frank & Schulte GmbH	Europe			x						
Fujitsu	Japan				x					
GBC Materials Corp	United States								x	
General Signal	United States	x								
GTE Electrical Products	United States	x								
Harbison-Walker Refractories	United States	x					x		x	
Heany Industries, Inc.	United States	x								
Hi-Purity Materials, Inc.	United States	x								
Hitachi	Japan		x				x			
Hi-Tech Ceramics, Inc.	United States	x					x		x	
Hoechst	Europe		x							
Ibiden	Japan		x							
International Advanced Materials	United States	x		x						

Table A-2 (continued)
Substrate Suppliers - 1992

Company	Headquarters	Alumina	Aluminum Nitride	Beryllium	Glass-Bonded Ceramics	Diamond	Mullite	Sapphire	Silicon Carbide	Silicon
Keramont Italia S.p.A.	Europe	x	x							
Komatsu	Japan									x
Kyocera	Japan	x					x	x	x	
Laing Ceramics Corp	United States									
Lanxide/DuPont	United States		x						x	
Matsushita	Japan		x		x					
McDanel Refractory Co	United States						x			
Micro Materials	United States	x								
Mitsubishi	Japan	x								x
3M/Ceramic Materials	United States	x							x	
Morton International	United States	x								
Murata	Japan		x		x					
National Ceramics Inc.	United States	x					x			
NEC	Japan		x		x					
New Jersey Porcelain Co.	United States						x			
Nippon Mining	Japan	x								
Nitto	Japan				x					
Noritake	Japan		x							
NTK	Japan	x	x		x					
OTC	Japan									x
Particle Technology	United States						x		x	
Pure Industries Inc./Stackpole	United States	x					x			
akco Industrial/Alcoa	United States	x								
Pure Carbon Company/Stackpole	United States								x	
Rhone-Poulenc, Inc.	Europe	x								
R&W Products	United States	x								
Samsung Corning	Korea	x								
Saxonburg Ceramics Inc.	United States	x								
Shinetsu	Japan									x
Shinko	Japan		x				x			
SMI Ceramics	Japan		x			x				
Southtec	United States								x	
Sumitomo Metal	Japan		x						x	
Sumitomo Chemical	Japan	x	x							
Superior Technical Ceramics	United States	x					x			
Toshiba	Japan		x							x
Tokuyama Soda	Japan		x							
Versar	United States								x	
Wilbanks International/ Adolph Coors Co.	United States	x								
W.C. Heraeus	United States		x							
W.R. Grace	United States	x	x							

Source: Dataquest, April, 1992

International Micro Industries, Inc.
8000 Commerce Parkway
Mount Laurel, New Jersey 08054-2227

For product information call: Thomas L. Angelucci, Sr.
(609) 273-0200

MCM overview:

Products:	Design and development services for multiple MCMs
Employees:	50
Factory Size:	5000 square fee
Revenues:	$5 million

Corporate Description:

IMI is engaged in the research, design, assembly, test, sales, and service of ceramic and silicon substrates and modules. IMI's MCM program began in 1987. IMI has developed a gold-to-gold thermocompression TAB lead interconnect process for very high density, high speed MCMs. The lead interconnect assembly process includes IMI designs, tooling and materials including a 400 mil, 360 I/O VLSI test chip with 2 mil square gold bumps on a 4 mil pitch, and a matching 35mm TAB flexcircuit lead pattern.

IMI was founded in October 1971. IMI's products and services are used to lead interconnect, assemble, and package semiconductor devices. The company also provides contract development and production assembly services to the industry. The company concentrates its resources on TAB and Flip Chip technologies.

nChip
1971 North Capitol Avenue
San Jose, California 95132

For product information call: Stan Drobec
Director of Marketing
(408) 945-9991

MCM Overview:

Products:	High density MCM substrates and modules
Employees:	50
Factory size:	30,000 square feet with 6,000 square feet of clean room
Revenues:	$5 to $15 million

Corporate Profile:

nChip is a supplier of silicon based MCM substrates and modules. nChip offers a complete solution to MCM design and fabrication. Services include consulting, design services, substrate manufacture and MCM assembly and test. nChip provides a complete technology roadmap to applications up to and beyond 200 MHz.

nChip uses silicon dioxide as an interlayer dielectric rather than polyimide. nChip believes that silicon

dioxide provides the best combination of low cost, high reliability and performance, and excellent manufacturability. nChip's basic technology utilizes aluminum as a conductor and provides two signal interconnect layers and two power and ground layers. The advanced nC2000 process substitutes copper interconnect with thicker conductors to reduce signal line resistance by 75 percent without increasing capacitance. An optional resistance layer is available for transmission line terminating resistors.

nChip was founded in March of 1989. Total capital raised to date is $15 million from a combination of investors. nChip signed a joint development license agreement with Sumitomo Metal Mining (SMM) Electronics in May 1991. Under the terms of the agreement, the two companies will work together on techniques for lowering the cost and improving the volume manufacturability of core technologies employed in MCMs, including substrate, packaging, and interconnect technologies. The agreement also includes a multi-million dollar equity investment in nChip by SMM.

Brush Wellman Inc.
6100 South Tucson Boulevard
Tucson, Arizona 85706

For product information call: Michael Anderson
(216) 486-4200

MCM Overview:

Products:	High density cofired ceramic (MCM-C) substrates
Employees:	10
Revenues:	$5 million

Corporate Profile:

Brush Wellman is a supplier of Beryllia ceramic substrates for packaging including MCM's. Metallizations include cofired tungsten, single and multilayer, as well as direct bonded copper.

Beryllia ceramic substrates from Brush Wellman were selected by Hughes Aircraft Company for the AMRAAM air-to-air missile. Beryllia was selected over other ceramic substrates as it insulates the electronics to prevent grounding to surrounding metal. The thermal conductivity of BeO is 8 to 10 times that of more commonly used alumina.

Burr-Brown Corporation
P.O. Box 11400 M/S 122
Tucson, Arizona 85734-1400

For product information call: Michael M. Pawlik
Vice President
(602) 746-7180

MCM Overview:

Products:	Supplier of cofired ceramic (MCM-C) and chip-on-board (MCM-L) modules.
Employees:	< 100
Factory Size:	< 5,000 square feet
Revenue:	$15 to $50 million

Corporate Profile:

Burr-Brown Corporation is a leading designer and manufacturer of precision microcircuits and microelectronic based systems for use in data acquisition, signal conditioning, and control applications throughout the world.

Burr-Brown was founded in 1956. Its corporate headquarters are located in Tucson, Arizona. The company employs over 1,650 people and manufactures over 1,000 products.

The Carborundum Company
Microelectronics Division
10409 S. 50th Place
Phoenix, Arizona 85044

Carborundum Company
Substrates Division
2050 Cory Road
Sanborn, New York

For product information call: Robert W. Lashway
(602) 496-5000
Carol Hewett
(716) 731-9244

MCM Overview:

Products:	Cofired ceramic substrates and design services for (MCM-C) modules
Employees:	40
Factory Size:	37,691 square feet
Revenue:	$5 million

Corporate Profile:

The Carborundum Company started sample shipping of ceramic casings in 1990. The New York facility produces aluminum nitride substrates, while the Phoenix, Arizona facility concentrates on the development of aluminum nitride packages for the microelectronics market. The combined operational capabilities includes extrusion, dry pressing, isopressing, green machining, grinding and lapping, tape casting, thick film and refractory metallization.

The Carborundum Company, formerly Standard Oil Engineered Materials Company, is a subsidiary of BP America Inc. The ultimate parent is The BP Company p.l.c., of the United Kingdom.

Advanced Packaging Systems
3099 Orchard Drive
San Jose, California 95134

For product information call: Richard F. Otte
Raychem Corporation
Menlo Park, California
(415) 361-4180

MCM Overview:

Products:	High density thin film modules
Employees:	Facility closed 1992
Factory Size:	1,000 square feet of class 1000 clean room
	Class 100 under the laminar flow hood
	Canon proximity aligners
	5 inch material (1x4 inch substrate)
	100 wafers per week
Revenue:	$5 million to $10 million

Corporate Profile:

Advanced Packaging Systems (APS) was originally a joint venture between Raychem Corporation and Corning. Raychem began work on packaging technology in 1983. Raychem acquired Interamics of San Diego in 1984, and APS became a subsidiary of Raychem in 1988. In January 1991, Raychem completed the sale of the San Diego based Interamics component division of APS to Coors Electronics Package Company, of Colorado. Raychem has closed the APS division. During its operations, APS produced over 100 module prototypes for aerospace, mainframe and workstation applications.

APS built the thin film module interconnects on both silicon and alumina. The layers were built up of polyimide and copper/chrome. The copper was 5 microns thick and the chrome was 1000 Angstroms.

APS also developed a Bonded Interconnect Pin (BIP) process technology. The process consisted of wire bonded pins to a chip, but the pin height was fixed at 15 mils. The substrate consisted of solder puddles in positions matching the chip bonding pads. The chip was flipped and positioned with gold wires in the solder puddles. The advantage of such a process is that the compliance of the wires takes up any differential thermal expansion between the chip and substrate. The disadvantage is that the BIP process cannot withstand acceleration above 1500 G's for military applications. The height of the chip was uniform to allow placement of a cooling plate on the backside of the chips.

APS also developed an optical waveguide technology. The technology consisted of 8 micron waveguides that route infrared energy on the substrate with electrical interconnects. The optical polymer used in the technology was developed by Raychem. While still developmental, its performance was attractive for gigahertz range applications.

Raychem currently holds the licenses for all APS technology.

Alcoa Electronic Packaging, Inc.
16750 Via Del Campo Court
San Diego, California 92127

For product information call: Leonard W. Schaper
(619) 451-7100

MCM Overview:

Products:	High density MCM technology using copper polyimide on a silicon substrate
Employees:	500
Factory Size:	Not available
Revenues:	$5 million

Corporate Profile:

Alcoa Electronics Packaging, Inc., (AEP), signed an agreement with AT&T in 1990, licensing the Polyhic technology patented by AT&T. The original agreement included substrate test, chip/wafer test and module test. Alcoa has also developed prototype test modules utilizing co-fired multilayer alumina-tungsten substrates in a cavity-down arrangement.

AEP is a business division of the Materials Science sector of Aluminum Company of America. The Materials Science sector represents 5% share of the parent company business. The conglomerate's venture into the world of electronic ceramics began in 1986 with the purchase of Pakco Industrial Ceramics, and the formation of Intercon-X, now AEP, in San Diego.

Implex PLC
Elm Road
West Chirton Industrial Estate
North SHields
Tyne & Wear
NE25 8SE
UK

For product information call: William E. Guthrie
Highland Associates
(408) 247-2926

MCM Overview:

Products:	Thin film interconnect of chrome-clad copper conductors imbedded in a polyimide dielectric medium

Corporate Profile:

Implex acquired the Polylithic invented MCM technology in 1991. Polylithics, formerly located in Santa Clara, California was founded in 1988. Their MCM prototype was available in 1989. Implex discontinued the development work conducted by Polylithics and is now licensing the process. Included in the license agreement will be patent rights, manufacturing and marketing rights, documented process and design methodologies and the process recipe itself.

The interconnect film comprises three layers of metal, two for signals and one for power and ground. Fine line widths of 10μm are achieved on 25μm tracks, so routing densities near 2,000 in/in2 are realized with the two signal layers.

AT&T Network Systems
North Andover, Massachusetts

AT&T Bell Labs
Murray Hill, New Jersey

Corporate Profile:

AT&T Network Systems and Bell Laboratories have made multiple developments of MCM products based on their patented (U.S. patent 4,554,229) POLYHIC (Polymer Hybrid Integrated Circuit) technology. POLYHIC was initially introduced in AT&Ts switching and transmission equipment. POLYHIC is an extension of AT&Ts thin film hybrid circuit technology utilizing copper-based metallization, and TaN resistors fabricated on alumina substrates. AT&Ts MCM technology combines copper thin film with a polymer process developed for dielectric and thermal stability. The polymer is a photosensitive formulation that cures at a temperature low enough to prevent degradation of the thin film resistors and conductors. Technology size is 2 mil lines, 3 mil spaces and 4 mil polymer vias.

AT&T has signed a license agreement with Alcoa Electronic Packaging, San Diego to implement the POLYHIC technology in their module development. AT&T is currently evaluating a silicon-on-silicon MCM that incorporates linear Bipolar and digital CMOS circuits. Operating samples will be available in April 1992. This test module replaces 174 separate components in a small module size of 9.3mm x 11mm. This module results in a packaging density of more than 3,000 component terminations per square inch.

References: A. V. Shah, E. Sweetman, C. K. Hoppes, "A Review Of AT&T's POLYHIC Multichip Module Technology," Proceedings of the Technical Program, NEPCON West 1991, pp 850-862.

IBM Corporation
Packaging Applications Marketing
IBM East Fishkill
Hopewell Junction, New York 12533

For product information call: Ed Chang
(914) 892-9712

MCM Overview:

Products: Crystallized glass-ceramic thin film thermal Conduction Module (TCM)

Corporate Profile:

IBM first announced marketing of its semiconductor packaging technology to the merchant market early 1991. IBM now offers a full service packaging capability in design, development, fab, chip bonding, and test of both single chip substrates and thin film modules.

IBM first introduced TCM substrates into their mainframe systems in the 1970s. The C-4 flip-chip and Direct Chip Attach technologies are also available to the merchant market.

In June 1991, IBM, Yasu, Japan, introduced a MCM designed on thin silicon PCB for the RISC 6000 workstation. The module substrate is aluminum polyimide mounted on an aluminum heat spreader. Silicon thermal grease is spread between the substrate and heat spreader to provide compliance and prevent cracking of the substrate during temperature cycling. The module is flipped onto an FR4 board. IBM has been working on high frequency applications from 60 MHz to 200 MHz.

Pacific Microelectronics Centre
8999 Nelson Way
Burnaby, British Columbia
Canada V5A4B5

For product information call: Al Kozak
(604) 293-5755

MCM Overview:

Products:	High density thin film modules
Employees:	45
Revenues:	$5 million

Corporate Profile:

PMC has their own fab capability for both standard and custom MCM solutions. PMC has the capacity to produce 25,000 substrates per year. PMC's MCM technology is marketed into telecom, medical and defense applications.

PMC was founded in May 1988 as a division of MPR Teltech, Ltd. PMC announced its SONET Line Interface Module in July 1991. This module integrates Bipolar, CMOS and GaAs component technology.

Northern Telecom
Electronics Limited
PO Box 3511, Station C
Ottawa, Ontario
CANADA K1Y 4H7

MCM Overview:

Products:	High density MCM technology for MCM-L, MCM-C, MCM-D as well as hybrid circuits

Corporate Profile:

Northern Telecom's MCM operations are completely captive. Northern Telecom's current internal con-

sumption of MCM includes MCM on laminate, ceramic and thin-film, as well as hybrid and traditional single chip packaging.

Ceramics Process Systems Corporation
155 Fortune Boulevard
Milford, Massachusetts 01757

For product information call: Peter R. Loconto
(508) 634-3422

MCM Overview:

Products:	High density cofired ceramic substrates
Factory Size:	36,000 square feet
Revenues:	$5 million

Corporate Profile:

CPS began targeting the MCM market in 1990 concentrating on aluminum nitride and 99.6% aluminum oxide material for their multilayer co-fired and molding processes. CPS has designed high performance multicavity ceramic modules for the Cray Y-MP C90 supercomputer.

CPS was founded in 1984 and operates solely in the development, manufacture, and sale of advanced ceramic products.

Coors Electronic Package Company
511 Manufacturers Road
Chattanooga, Tennessee 37405

For product information call: Jim F. Wade
(615) 755-5400

W.R. Grace & Company
7379 Route 32
Columbia, Maryland 21044

For product information call: James E. Gado
(301) 531-4124

MCM Overview:

Products: High density multilayer, co-fired aluminum nitride MCMs

Corporate Profile:

Grace Research Division and Coors Ceramics Company announced joint development of ceramic MCMs for commercial production in 1990. This MCM program is based on patented Grace technology for hot pressing of electronic ceramic components with emphasis on advanced materials, including aluminum nitride and low k dielectrics. Prototype capacity is located at Grace's corporate research center in Colum-

bia, Maryland with a capacity press of 1,000 square inches per month.

Multichip Technology Incorporated
3901 N. First Street
San Jose, California 95134-1599

For product information call: Andrew J. Paul
President
(408) 943-2600

MCM Overview:

Products: High performance standard and custom memory modules and MCM-L designs
Revenues: $5 million

Corporate Profile:

Multichip Technology Incorporated, a subsidiary of Cypress Semiconductor Corporation, was founded in 1988 to design memory modules and low cost MCMs for SPARC-based workstation designs. Multichip has designed a 10 chip 50 MHz module that incorporates TAB on a PCB/polyimide substrate.

Digital Equipment Corporation
10500 Ridgeview Court
Cupertino, California 95014

For product information call: Michael Grove
(408) 973-1521

MCM Overview:

Product: High density polyimide and copper MCM on aluminum substrate

Corporate Profile:

Digital Equipment Corporation announced development of their High Density Signal Carrier (HDSC) multichip module unit in 1989. The HDSC module was designed for the advanced VAX 9000 system. The DEC MCM technology effort began in 1983. The total R&D effort was $1.5 billion by 1988. The DEC 9000 process was a polyimide and copper design on aluminum substrate. Two separate polyimide layers were used. They were separated from the aluminum by etching, laminated together and then glued to a copper substrate. The chips were die attached onto the polyimide. Thermal vias were configured under the chip for power dissipation. Clock speed on the VAX 9000 reaches 550 MHz. The VAX 9000 module incorporates TAB with 4 mil inner lead and 8 mil outer lead bond pitch.

Hestia Technologies, Incorporated
224 North Wolfe Road
Sunnyvale, California 94086

For product information call: Kevin J. Surace
(408) 737-1212

MCM Overview:

Products:	Low cost MCM designs on multilayer polyimide glass epoxy material
Employees:	35
Revenues:	$5 million

Corporate Profile:

Established in 1983, Hestia Technologies, Incorporated is a privately held U.S. owned operation. Hestia's substrates are manufactured offshore while module assembly takes place at the Sunnyvale, California facility.

Hestia offers complete turnkey services for both single chip and multichip designs.

Kyocera Corporation
Kyocera America, Incorporated
8611 Balboa Avenue
San Diego, California 92123

For product information call: Richard Sigliano
(619) 576-2600

MCM Overview:

Products:	High density cofired ceramic based multilayer substrates

Corporate Profile:

Kyocera provides a full service MCM approach. Their MCM ceramic designs include metallized MCM, thin-film metal brazed MCM, thick film copper MCM, high density mulitlayer aluminum MCM, Mullite MCM, and ultra high speed multilayer copper polyimide MCM.

Kyocera America is a wholly owned subsidiary of Kyocera Corporation of Japan. Kyocera is the largest manufacturer of technical ceramics, and is also the largest supplier of ceramic single chip packages and substrates to the semiconductor industry. Kyocera was established in 1959.

Motorola Incorporated
3501 Ed Bluestein Boulevard
Austin, Texas 78721

MCM Overview:

Products: High density module (HDM) of thin film copper polyimide on ceramic substrate using flip chip bonding

Corporate Profile:

Motorola's MCM R&D organizations reside in Austin, Texas, as well as Chandler and Phoenix, Arizona. Motorola's MCM designs range from low cost 10 chip to high performance 100 chip module designs. Motorola has targeted the CMOS based MCM market for EDP, telecom, automotive and cellular applications.

Motorola's new HDM consists of six simultaneous switching output (SSO) die using Motorola's ASIC technology. Two of the HDM prototype were developed using surface mount Pad Array Carrier (PAC) or Land Grid Array (LGA) technology. Heat was removed from the back of the die through a thermal gel to the lid.

References: J. Trent, G. Westbrook, "Fine Pitch Pad Array Carrier Sockets For Multichip Modules," IEEE 1992 pp 40-43.

NTK Technical Ceramics
Division of NGK Spark Plugs Co., Ltd.
Headquarters: Nagoya, Japan
Substrates Divsion: Takenami, Japan

For product information call: Kay Yamasaki
Howard Ushkow
(619) 487-9310

MCM Overview:

Products: High density cofired mulitlayered ceramic substrates

Corporate Profile:

NTK was established in 1949 as a division of NGK which was founded in 1936. NTK is the second largest supplier of ceramic substrates and packages to the semiconductor industry. NTKs MCM designs incorporate alumina as the base substrate with cofired multilayered metallizations for the power and ground planes. A copper and polyimide multilayer structure is formed on the alumina surface.

Texas Instruments
13532 N. Central Expressway
PO Box 655012
Dallas, Texas 75265

For product information call: Robert Gilbert
(214) 995-5592

MCM Overview:
Products: Offers MCM design and production services

Corporate Profile:

Texas Instruments' built their multichip module technology capability through their defense electronics division. Texas Instruments participates in the DARPA MCM program and has developed an ultra GHz module with General Electric. Texas Instruments has also developed a stackable 9M bit DRAM module with TAB interconnect. Texas Instruments will be offering their module technology for commercial applications.

The Dow Chemical Company
Central Research
Charlotte, North Carolina 28210

For product information call: Philip Garrou, PhD.

MCM Overview:
Products: Substrate materials for fabrication of thin film cofired ceramic modules

Corporate Profile:

The Dow Company in conjunction with Polycon Corporation of Arizona, developed high density MCMs fabricated on silicon wafers with a flexible process using bisbenzocyclobutene (BCB) derived dielectric layers and aluminum interconnect. The Dow Chemical Ceramics and Advanced Materials Division of Dow is also a supplier of aluminum nitride powder to the MCM market.

References: D. Burdeaux, P. Townsend, J. Carr, P. Garrou, "BCB Dielectrics For The Fabrication of High Density Thin Film Multichip Modules," Journal of Electronic Materials, Vol. 19, No. 12, 1990, pp 1357-1366.

J. Reche, P. Garrou, J. Carr, P. Townsend, "High Density Multichip Module Fabrication," The International Journal For Hybrid Microelectronics, Vol. 13, No. 4, December, 1990 pp 91-99.

Polycon
2495 S. Industrial Park Avenue
Tempe, Arizona 85282

For product information call: Robert DeVellis
(602) 731-9544

MCM Overview:

Products:	Supplier of multilayer thin film polyimide and BCB substrates for MCMs
Employees:	20
Revenues:	$5 million

Corporate Profile:

Polycon, previously located in Ventura, California, has been manufacturing low volume high density MCMs since 1984 for military applications. Polycon is essentially a startup to the commercial market for MCMs and has investment funding from the Dow Chemical Company.

Sumitomo Metal Industries, LTD
28-5, Nishigotanda 2
Chome Shinagawa-Ku
Tokyo, JAPAN 141

SMI Ceramics America, Inc.
2953 Bunker Hill Lane
Suite 203
Santa Clara, California 95054

For product information call: Tsuneki Orita
Vice President/Sales Manager
(408) 982-0990

MCM Overview:

Products:	Cofired ceramics substrates

Corporate Profile: SMI Ceramics America Inc., is the U.S. subsidiary of Sumitomo Metal Industries, Ltd., of Japan. Sumitomo Metal Industries of Japan purchased the Narumi Technical Ceramics division from Narumi China of Japan in 1991.

SMI Ceramics is the third largest producer of ceramics packages to the semiconductor industry. SMI has built a $19 million ceramics development center in Yamaguichi, Japan.

Rogers Corporation
PO Box 700
2001 West Chandler Boulevard
Chandler, Arizona 85244

For product information call: Dennis G. Sheehan
(602) 786-8239

MCM Overview:
Products: Fluoropolymer substrate materials

Corporate Profile:

Rogers is offering their proprietary thin film substrate technology for license agreements. Rogers has developed MCM prototypes using their material but they do not intend to scale up for production.

The fluoropolymer material utilized in the MCM prototype reportedly allows faster signal speeds and less cross talk, lower moisture sensitivity and lower TCE than polyimide products. The trademarked material developed by Rogers was part of a $8 million R&D program with investment from Paine Webber R&D Partners II.

Lanxide Electronic Components, L.P.
1300 Marrows Road
PO Box 6077
Newark, Delaware 19714-6077

For product information call: Aris K. Silzars, Ph.D.
President
(302) 456-6311

MCM Overview:
Products: Supplies reinforced ceramic substrates
Facility Size: 37,000 square feet

Corporate Profile:

Lanxide Corporation was founded in 1983 to develop and commercialize reinforced ceramic and metallic products. Lanxide Electronic Components (LEC) is a limited partnership between Lanxide Corporation and E.I. du Pont de Nemours & Company. Lanxide Corporation provides LEC with its materials technology base while DuPont has committed up to $35 million to bring the technology to the electronics industry.

LSI Logic Corporation
1551 McCarthy Boulevard
Milpitas, California 95035

For product information call: Ed Fulcher
(408) 933-6818

MCM Overview:
Products: Low cost MCM-L modules

Corporate Profile:

LSI Logic offers a 40 MHz module incorporating a MIPs R3000, two companion ASICs and six SRAMs. The bare die are mounted on copper slugs into slots on a six layer PCB of 3.5x3.5 inches. LSI Logic has qualified both PGA and Olin's MQuad packages for their modules.

Samsung Corning Company, Ltd.
8th Floor
Joong-Ang Daily News Building
7, Soon Wha-Dong
Chung-Ku, Seoul
KOREA

For product information call: S.H. Hong
756-9988 (532)

MCM Overview:
Products: Low cost MCM-L and high density MCM-C modules and ceramic substrates

Corporate Profile:

Samsung Corning was founded in 1973 as a joint venture between Samsung and Corning. The Samsung Corning ceramic division is located in Kumi, Korea. It supplies both single chip and multichip designs and assembly services as well as substrates to the semiconductor industry. It is currently establishing license agreements with companies in the United States for volume production of low cost 8 to 10 chip modules.

Electro Ceramics Thailand (ECT)

MCM Overview:
Products: Cofired ceramic substrates

Corporate Profile:

ECT is a subsidiary of Nippon Carbide and Hokuriku Ceramics of Japan. The Japan Asia Investment Corporation (JAIC) has also invested $22 million in this subsidiary. The plant was established to supply ceramic substrates to Japanese plants located in Asia.

Printron, Incorporated
8917 Adams NE
Albuquerque, New Mexico 87113

For product information call: David Best
(505) 823-1990

MCM Overview:

Products:	Low cost multilayer substrates
Employees:	10
Facilities:	6,500 square feet

Corporate Profile:

Printron, Inc., was established in 1987. It has developed an advanced manufacturing process for printed circuits. Printron has a joint development agreement with BDM International, Incorporated of McLean, Virginia. The Printron process consists of rapid direct printing with metallurgical inks on multiple substrates followed by a fusing process which results in conductive circuit pathways. Printron and BDM will use this technology to develop systems for military and commercial markets.

Staktek
8900 Shoal Creek Boulevard
Austin, Texas 78758

For product information call: Bob Campbell
(512) 454-9531

MCM Overview:

Products:	Memory modules for disk emulator and high frequency thin film MCM
Facility Size:	4,000 square feet

Corporate Profile:

Established in 1990, Staktek originally developed a thin film MCM technology for space satellite operations. TRW Corporation has made an investment in Staktek. Staktek has developed a hard disk emulator for a memory card application with a 20 to 80 MB capacity.

Intel Corporation
5200 NE Elam Young Parkway
Hillsboro, Oregon 97124

5000 W. Williams Field Road
Chandler, Arizona 85224

Corporate Profile:

Intel Corporation has designed multichip modules and memory modules for defense contracts. While Intel has announced that they will not be producing MCMs in 1992, R&D efforts on a 586 design are underway for availability in 1993. The 1993 design is expected to incorporate the Intel 586 processor, a C5 (cache controller) and ten C8s (SRAMs).

Delco Electronics Division
GMC
Kokomo, Indiana

Corporate Profile:

Delco is currently not producing MCMs. Delco is the largest North American supplier of hybrid circuit designs. MCMs are currently in an R&D phase for their automotive designs. Since cost is the most important concept in automotive electronic consumption, Delco does not expect to manufacture MCMs for another two to three years.

General Electric
Corporate Research & Development
Schenectady, New York 12301

For product information call: Jim E. Sabatini
(518) 387-5905

MCM Overview:

Products: High density interconnect overlay process technology for MCM on laminate or silicon substrates

Corporate Profile:

The HDI overlay process was developed by GE in conjunction with DARPA, the Air Force, Texas Instruments and Lawrence Livermore National Laboratories. In the HDI process the interconnect is built over the top of the bare die. The substrate is not the finished interconnect structure as in other technologies, but rather the heat sink and support structure for the die and interconnect.

References: Dr. W. Daum, L. E. Roszel, "MCM Prototyping Using Overlay Interconnect Process," Proceedings of the 1992, IEEE MCM Conference, pp 36-39.

Toshiba Corporation
1-1-1, Shibaura, Minato-ku
Tokyo 105, JAPAN

Toshiba America, Incorporated
Sunnyvale, California

For product information call: Frank Ramsey
(408) 733-3223

Corporate Profile:

Toshiba's original MCM development was implemented in their GaAs Parallel Processing System mainframe application. Toshiba has also developed a silicon on silicon 1 inch square, 1,000 pinout CMOS MCM technology. Toshiba offers design services, and supplies cofired ceramics and thin film substrates for MCMs. The Toshiba Corporation was founded in 1875.

References: T. Sudo, "Silicon-on-Silicon Technology for CMOS-based Computer Systems," Proceedings of the 1992, IEEE MCM Conference, pp 8-11.

Fujitsu, Ltd.
1015 Kamikodanaka, Nakahara-ku
Kawasaki-shi
Kanagawa 211, JAPAN

Fujitsu Microelectronics, Inc.
IC Division
3545 N. First Street
San Jose, California 95134-1804

Corporate Profile:

Fujitsu's initial development of MCM technology was for their M-780 mainframe and VP2000 Supercomputer. Fujitsu's watercooled module utilizes carrier technology of 144 chips on multilayered ceramic. The module has an aluminum nitride base with tungsten vias. Gold bump TAB technology connects copper polyimide to the metal cap. The module has a soft solder seal with an aluminum nitride heatsink.

Fujitsu also offers a high density thick-film wired MCM on a ceramic substrate housed in a 168-pin PQFP. The module measures 1.5" x 1.5". Height of the package mounted is 0.173 inches.

Crystallume
125 Constitution Drive
Menlo Park, California 94025

For product information call: Laurie C. Conner
(415) 324-2958

MCM Overview:
Products: CVD Diamond thin film substrates
Employees: 30

Corporate Profile:

Crystallume was founded in 1984. Crystallume currently produces 4 inch silicon wafers with 1 micron diamond coating. Crystallume supplies substrates for laser diodes, fiber optic coupled diodes, high speed high power GaAs, silicon and hybrid circuits, and MCMs. Crystallume is developing diamond ceramic substrates.

Irvine Sensors Corporation
3001 Redhill Avenue
Costa Mesa, California 92626

For product information call: Myles F. Suer
(714) 549-8211

MCM Overview:
Products: Silicon-on-silicon 3 dimensional memory structures

Corporate Profile:

Irvine Sensors supplies its stacking package technology design under contract to customers. Most of the company's contract work has been for military applications. ISC has 27 United States patents on its basic technology. The company's revenues result pricipally from prototype development on research and development contracts which are usually cost-plus-fixed-fee or fixed price.

Ibiden Company, Ltd.
Technology & Development Department
300, Aoyanagi-cho, Ogaki
Gifu 603, JAPAN

Ibiden U.S.A. Corporation
1270 Oakmead Parkway #208
Sunnyvale, California 94086

For product information call: Motoji Kato
(408) 735-7755

MCM Overview:

Products: Supplies fine-line PCB modules

Corporate Profile:

Technical marketing and sales of the Ibiden products is done from the Sunnyvale location of Ibiden, while all manufacturing is done in Japan. Ibiden provides design services as well as substrates to the merchant market.

Appendix B

Application Market Definitions

The electronic equipment segments discussed in Chapter 3 are defined in the following paragraphs.

Data Processing

The Data Processing segment is structured to include any equipment with the primary purpose of processing information. This includes add-on and peripheral devices that are used to reproduce computer data for such things as storage and hard-copy output.

The Data Processing segment is further subdivided into Computer, Data Storage/Subsystems, Terminals, Input/Output, and Dedicated Systems. The last subsegment includes equipment with a more or less specifically defined operation, such as electronic typewriters, word processors, and automated banking/teller machines.

All personal computers (PCs) are placed within the Data Processing segment rather than in the Consumer segment because they are products with the primary function of flexible data processing. The majority of products listed in the Consumer segment are electrical or electromechanical equipment designed primarily for home or personal use, to which increasingly integrated semiconductor circuitry is being added. Overall, in the cases of appliances and home entertainment systems, the primary function of such consumer equipment is generally not flexible information processing, in spite of the fact that limited dedicated intelligence may be added as features.

Furthermore, the objective of reporting PC production, as well with all equipment, is for the purpose of estimating the semiconductor demand engendered by that type of equipment. It is not our objective to report the PC market by application segments such as home, scientific, technical, or business. Such a segmentation would represent a PC market phenomenon that is software based and has little to do with the hardware application of semiconductors. The same can be said for all electronic calculators since they too are primarily tools for information processing. Electronic games are designed with the primary objective of use in the home and, as such, are counted in the Consumer segment.

Communications

The Communications segment is subdivided into Premise Telecom, Public Telecommunications, Mobile, Broadcast and Studio, and Other Miscellaneous Equipment. These equipment designations have been developed by Dataquest's Telecommunications Service's format and the Standard Industrial Classification (SIC) codes used in the U.S. Commerce Department's Current Industrial Reports.

Industrial

The Industrial segment comprises all manufacturing-related equipment, and it includes some scientific and dedicated systems.

Consumer

The Consumer segment is subdivided into Audio, Video, Personal Electronics, Appliances and Other Miscellaneous Consumer Equipment. Personal electronics includes products carried or used by individuals, such as games, cameras, or watches. Overall, because much consumer equipment production stems from Japan, the consumer segment's definition was comprised to complement that region's perspective on the market.

Military/Civilian

This segment includes Radar, Space, Navigation/Communication, Aircraft Flight Systems, Simulation and Training equipment for both the Military and Civil (i.e. commercial) purposes.

Transportation

The Transportation segment forecasts the demand for electronic equipment based on auto and light truck production. Transportation also incorporates future analysis and growth of different vehicle electronics. The market has been segmented into equipment types that belong in different vehicle functional areas, such as Entertainment, Powertrain, Body Control, Safety and Convenience, and Driver Information.