1993 SUBSCRIPTION RESEARCH SERVICE

ASICS WORLDWIDE

What you'll need to know in 1993.

What type of ASICs are needed in Japan and North America for current and future generation system design?

While the average gate complexity of ASICs in Japan is lower than that of North America for today's current generation system design (18,000 gates versus 28,000 gates), average gate complexity for ASICs in next generation system designs is expected to dramatically increase in both countries to about 50,000 gates. In Dataquest's 1993 *User Wants and Needs* study, system designers will detail their future ASIC requirements as well as applications driving these higher gate counts. In addition, our focus report, *Regional Gate Array Trends*, will compare and contrast gate array trends in North America, Europe, and Japan.

What impact will BiCMOS have on the ASIC Market?

There continues to be ongoing debates on how much of an advantage BiCMOS has over CMOS, especially below 0.5 micron and with 3-volt power supplies. We will explore the issues surrounding BiCMOS in our 1993 *MarketTrends* report and future *Dataquest Perspective* issues.

What are the future packaging requirements for ASIC devices?

Because ASICs lead the industry in terms of having the most complex packaging and pin count requirements, suppliers are faced with the challenge of offering a wide range of packages that cost a lot of money to develop. To help ASIC suppliers focus their packaging effort, Dataquest will examine today's most popular ASIC packages as well as future packaging requirements in our *MarketTrends* report and future *Dataquest Perspective* issues.

How will VHDL /HDL impact the ASIC market?

Today's system designers are only reusing 35 percent of the functional units from previous designs in their current generation system designs. With the aid of hardware description languages (HDL) or top-down design methodologies, system designers can be more productive by reusing a higher portion of their previous designs. Dataquest will look at the impact of top-down ASIC design methodology in future *Dataquest Perspective* newsletters.

PRODUCT COVERAGE

ASICS
MOS/BiCMOS/Bipolar ASICs
Mixed Signal ASICs
...
GATE ARRAYS
MOS/BiCMOS/Bipolar Gate Arrays
Embedded Gate Arrays
...
CELL-BASED ICS
MOS/BiCMOS/Bipolar CBICs
...
PLDS
MOS/Bipolar PLDs
FPGAs
Simple/Complex PLDs

1993 RESEARCH HIGHLIGHTS

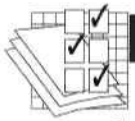
Electronic system design issues for 1993
...
New regional gate array trend data from Europe and Japan
...
Design starts by complexity, by application, by function, by process, by package type
...
Profiles of Actel and Toshiba
...
Key supplier success factors

Dataquest

Worldwide

Semiconductor Group

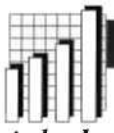
ASICS WORLDWIDE: What you'll need to know in 1993.



USER WANTS AND NEEDS

Key trends in electronic system design exposed through comprehensive surveys of worldwide system designers.

- Surveys will poll electronic system designers to identify significant trends in worldwide electronic system design and to explore potential new target markets for ASIC devices.
- Users will be surveyed on critical electronic system design issues for 1993, ASIC products being designed in specific applications, user perceptions on future ASIC products, and user perceptions on emerging technologies.



MARKETTRENDS REPORT

Comprehensive product and technology forecasts and application market trends in the global ASIC market with detailed quantitative data.

- This report focuses on the products, markets, companies, trends, and technologies of the global ASIC industry. The industry will be examined from a supply side as well as a demand side, and from a regional market as well as a global market perspective. Special attention will be paid to regional market and technology trends for gate arrays and cell-based ICs.
- ***Design starts by:*** complexity (utilized gates), by application (DP, Military, Industrial), by function (RAM, Micro, Analog), by memory size (2K, 4K, 16K), by process line width (1.0, 0.8 micron), by metal interconnect (2-layer vs. 3-layer), by unit volumes (<5K, 20K, >100K), by package type (PQFP vs. PPGA), and by pin count (<44, 44-84, 85-132) are provided for gate arrays and cell-based ICs.

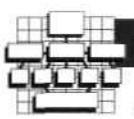
MARKET STATISTICS

- ***ASIC Consumption Forecast*** Five-year revenue forecasts by region for MOS ASICs, bipolar ASICs, BiCMOS ASICs, mixed-signal ASICs, MOS gate arrays, BiCMOS gate arrays, bipolar gate arrays, embedded gate arrays, MOS cell-based ICs, bipolar cell-based ICs, BiCMOS cell-based ICs, MOS PLDs, bipolar PLDs, FPGAs, simple PLDs, and complex PLDs.
- ***Worldwide ASIC Market Share*** Market share by company for MOS ASICs, bipolar ASICs, BiCMOS ASICs, MOS gate arrays, BiCMOS gate arrays, bipolar gate arrays, MOS cell-based ICs, bipolar cell-based ICs, BiCMOS cell-based ICs, MOS PLDs, and bipolar PLDs.

FOCUS REPORT

Regional Gate Array Trends

Over the next two to three years, electronic system manufacturers will encounter significantly greater competitive pressures stemming from the globalization of the industries and the markets. As a result, these system vendors will place greater high-end technology demands on their gate array suppliers.



VENDOR PROFILES

Detail of organizational structure, product portfolio strengths and weaknesses, and strategic directions of major ASICs manufacturers.

Companies scheduled to be profiled:

- Actel
- Toshiba

ADDITIONAL RESEARCH RESOURCES

INQUIRY SUPPORT AND MONTHLY SUMMARIES: year-long direct access to semiconductor analysts and monthly summaries of representative inquiries.

DATAQUEST ALERTS: news and analysis delivered by fax and *Dataquest Online* for fast breaking developments.

DATAQUEST PERSPECTIVES: timely analysis and commentary on industry events and issues.

DATAQUEST ONLINE: access to semiconductor service databases and publications. Clients will be billed separately by CompuServe for connect time.

INFORMATION RESOURCE CENTERS: access to extensive printed and on-line data in San Jose, Boston, UK, France, Germany, and Japan.

SEMICONDUCTOR CONFERENCES: the industry's preeminent semiconductor conferences held in the U.S., Europe, Japan, and Asia.

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User Wants and Needs
...
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...
Market Statistics
...
Focus Reports
...
Vendor Profiles
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Inquiry Support and Monthly Summaries
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Market Statistics (Tab)		_____
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ASIC Consumption Forecast ✓	08/10/92	_____
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December 1992

Dear Client:

Enclosed you will find a new 1992 binder for your ASICs Worldwide Service.

Please move the 1992 Market Statistics, Vendor Profiles, Dataquest Perspectives, and User Wants and Needs into the new binder behind the appropriate tab.

Attached you will find a checklist of what should be included in the new 1992 binders after the documents have been filed.

You will soon be receiving your 1993 Dataquest binders for storage of all 1993 deliverables.

If you have any questions please contact me at (408) 437-8320.

Sincerely,

Kimberlie C. Southern
Operations Coordinator

ASICs *Worldwide*

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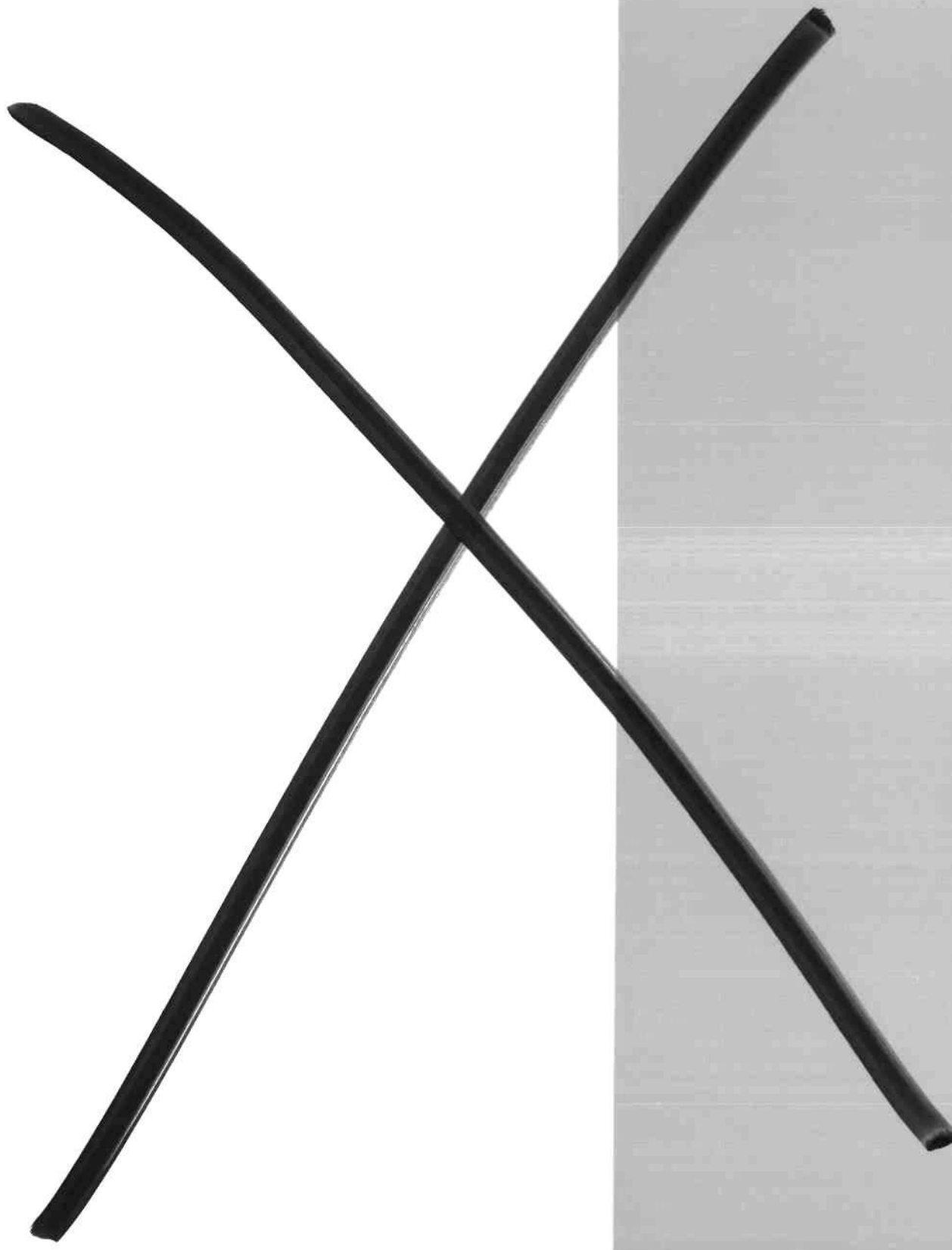

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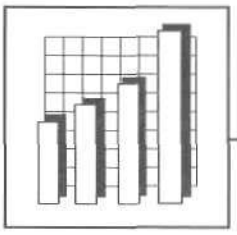
ASICs Worldwide



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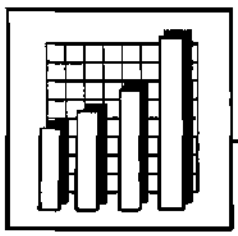
ASICs Worldwide



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Chapter 1
Executive Summary

Introduction and Report Structure

This report contains detailed information on Dataquest's view of the application-specific integrated circuit (ASIC) market and has a focus on gate array and cell-based IC (CBIC) product trends. It is intended to be used by ASIC suppliers and ASIC users to spot significant trends in the ASIC market and to aid in development of effective business planning and targeted product development. The core of this report was generated by Dataquest's ASIC supplier surveys—a MOS gate array survey (see Appendix A) and a MOS CBIC survey. The supply-side data generated from these surveys were then cross-checked with demand-side data for accuracy. Indeed, the trends from ASIC suppliers were consistent with the trends from the ASIC end users. For further detail on ASIC demand-side trends, see *ASIC User Wants and Needs: System Designers Vote on Future ASICs.*

This report is broken into seven chapters. It begins with an executive summary. Chapter 2 explains the research methodology employed in gathering the information as well as the definitions used in the report. Chapter 3 gives a background on gate array and cell-based IC product evolution. In Chapter 4, Dataquest forecasts the ASIC market by product, technology, and region. In Chapter 5, Dataquest examines the size of the North American application markets, then sheds light on the applications driving the ASIC market. Chapter 6 examines the leading ASIC supplier in each product area, then explores the challenges facing the different types of ASIC suppliers. In Chapter 7, the core of this report, Dataquest examines in detail the 1992 gate array and CBIC product trends. In this chapter, Dataquest delves into design starts by gate count (current and future projections), design starts by function (for example, the percentage of designs that had on-chip SRAM, microprocessors, microperipherals, and scan test), and design starts by line width. Furthermore, based on 1992 product trends, Dataquest projects the future product mix.

Major Findings

CBICs have been in a design war with gate arrays since their inception in the late 1960s. Gate arrays entered the electronic system design market a few years prior to CBICs and were quick to establish a dominant position. CBIC product designers continue to search for new weapons in the form of unique cell libraries to attack the well-entrenched gate array product. Gate array product designers have a battle plan of their own and a new weapon, called an "embedded gate

array." An embedded gate array is a traditional gate array (sea-of-gates architecture) that also includes megacells such as a large static RAM block that are diffused into the gate array base wafer.

Embedded gate arrays are making inroads in the ASIC market and now account for 11.3 percent of the 1992 MOS North American gate array design starts; this figure is up from 1 percent in 1990 and 3.7 percent in 1991. Embedded gate arrays offer the reduced risk and turnaround times associated with gate arrays, along with increased functionality and performance associated with CBICs.

The average North American gate array design start was 28,000 utilized gates during 1992, up from 21,000 gates in 1991. This large jump in gate complexity was because of the increasing use of on-chip SRAM and other large functional blocks. During 1992, 37.3 percent of North American gate array designs and 45.2 percent of CBIC designs had on-chip SRAM blocks. There is a strong need for large on-chip SRAM blocks (128K and 256K) in data processing applications that will be used for cache memory. Embedded gate arrays are very efficient in implementing SRAM and large functional blocks.

Traditional gate arrays and embedded gate arrays are also becoming more cost-competitive with CBICs because of the cost savings associated with using of three-layer metal interconnect. Three-layer metal designs now account for 36 percent of the 1992 MOS North American gate array design starts; this figure is up from 8.9 percent in 1990 and 20.5 percent in 1991. This rapid increase in three-layer metal interconnect designs is because of the major cost savings associated with three-layer metal versus two-layer metal in high-density designs. Gate utilization for a sea-of-gates gate array architecture using two-layer metal is about 40 to 45 percent; with three-layer metal interconnect, gate utilization jumps to 70 to 75 percent. Increased gate utilization means that the die required for a given application can be shrunk, which translates to higher yields and a significant cost savings. Furthermore, Dataquest projects that by mid-1995 gate array suppliers will be introducing 0.3- to 0.4-micron products, four-layer metal interconnect, with 1 million usable gates.

What product will win the war? In this report, Dataquest examines in detail the current and future product trends, supplier trends, and application trends, then forecasts the future of the ASIC market.

Project Analyst: Bryan Lewis

Chapter 2
Methodology and Definitions

Methodology

Dataquest uses both primary and secondary sources of information to produce market statistics, forecasts, and market trends. We use measures of both demand-side and supply-side data in the forms of surveys and audits. In addition, Dataquest analysts have many years of experience applying this information—in conjunction with opinions developed through industry contacts—to get the most accurate information possible.

Demand-Side Data

Dataquest demand-side (end-user) data are gathered using extensive survey techniques. End users are identified through the registered user and prospect lists of ASIC and EDA companies. Surveys were distributed throughout North America, Europe, and Japan, enabling Dataquest to gather a snapshot from a user point of view of the current and future system design requirements and the applications driving ASIC usage. Dataquest's international expertise was used: The surveys distributed in Japan were translated into kanji, the Japanese character set, in order to improve their accuracy. Dataquest received statistically significant numbers of responses in all areas and bases current and future end-user system trends upon these data.

Supply-Side Data

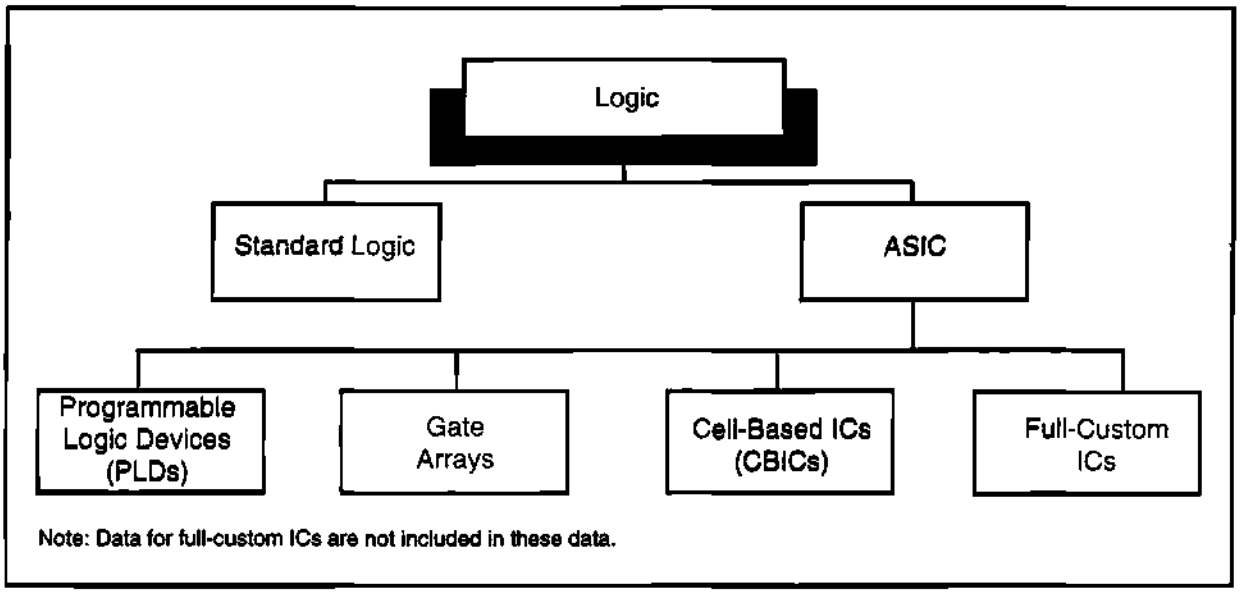
Dataquest supply-side data are gathered by surveying ASIC suppliers with highly detailed questionnaires (see Appendix A for a sample survey). Dataquest personally delivered supplier surveys to both gate array suppliers and cell-based IC suppliers during the third and fourth quarters of 1992. Dataquest received input from most of the leading ASIC suppliers accounting for more than 70 percent of the ASIC market. The information was then compiled and audited on a company basis. The aggregate trends were then cross-checked for accuracy with ASIC demand-side information as well as with system information derived from other Dataquest services.

We believe that the information presented in this report is the most accurate information available today.

Definitions

Dataquest defines the ASIC market according to the segmentation scheme shown in Figure 2-1.

Figure 2-1
ASIC Family Tree



Source: Dataquest (December 1992) G2001436

Dataquest segments logic into two main categories: standard logic and ASIC. The ASIC family tree breaks out ASICs as follows: programmable logic devices (PLDs), gate arrays, CBICs, and full-custom ICs. CBICs and full-custom ICs are personalized by altering the full set of masks, whereas PLDs and gate arrays are personalized by electrically programming the devices or by altering only the final layers of interconnect.

Product Definitions

The term ASIC is used to describe all IC products customized for a single user. ASIC products are a combination of digital, mixed-signal, and analog products. Customized ICs purchased by more than one user become standard products and are no longer counted as ASICs.

PLDs are defined as ICs programmed after assembly. Memory devices such as PROMs and ROMs are not included in this market segment.

Gate arrays are ASICs that contain a configuration of uncommitted elements in a prefabricated base wafer. They are *customized by interconnecting these elements with one or more routing layers*. Included in this category are traditional gate arrays (channeled and sea-of-gates architecture) and embedded gate arrays (channeled or sea-of-gates architecture that *also* include megacells such as SRAM diffused into the gate array base wafer).

CBICs are ASICs that are *customized using a full set of masks* and use automatic place and route tools. Included in this category are tradition standard cells (fixed-height/fixed-width cells) and megacells (variable-height/variable-width cells) and compiled cells.

Full-custom ICs are defined as ASICs customized using a full set of masks and using manual place and route.

Consumption and Revenue Definitions

Because systems may be fabricated, assembled, and sold in several different locations, Dataquest's regional device consumption is defined as the region where the device is assembled on the printed circuit board.

Consumption and revenue estimates include the following five sources of revenue:

- Intracompany revenue (sales to internal divisions)
- Nonrecurring engineering (NRE) revenue
- ASIC software revenue
- PLD development kit revenue
- Device production revenue

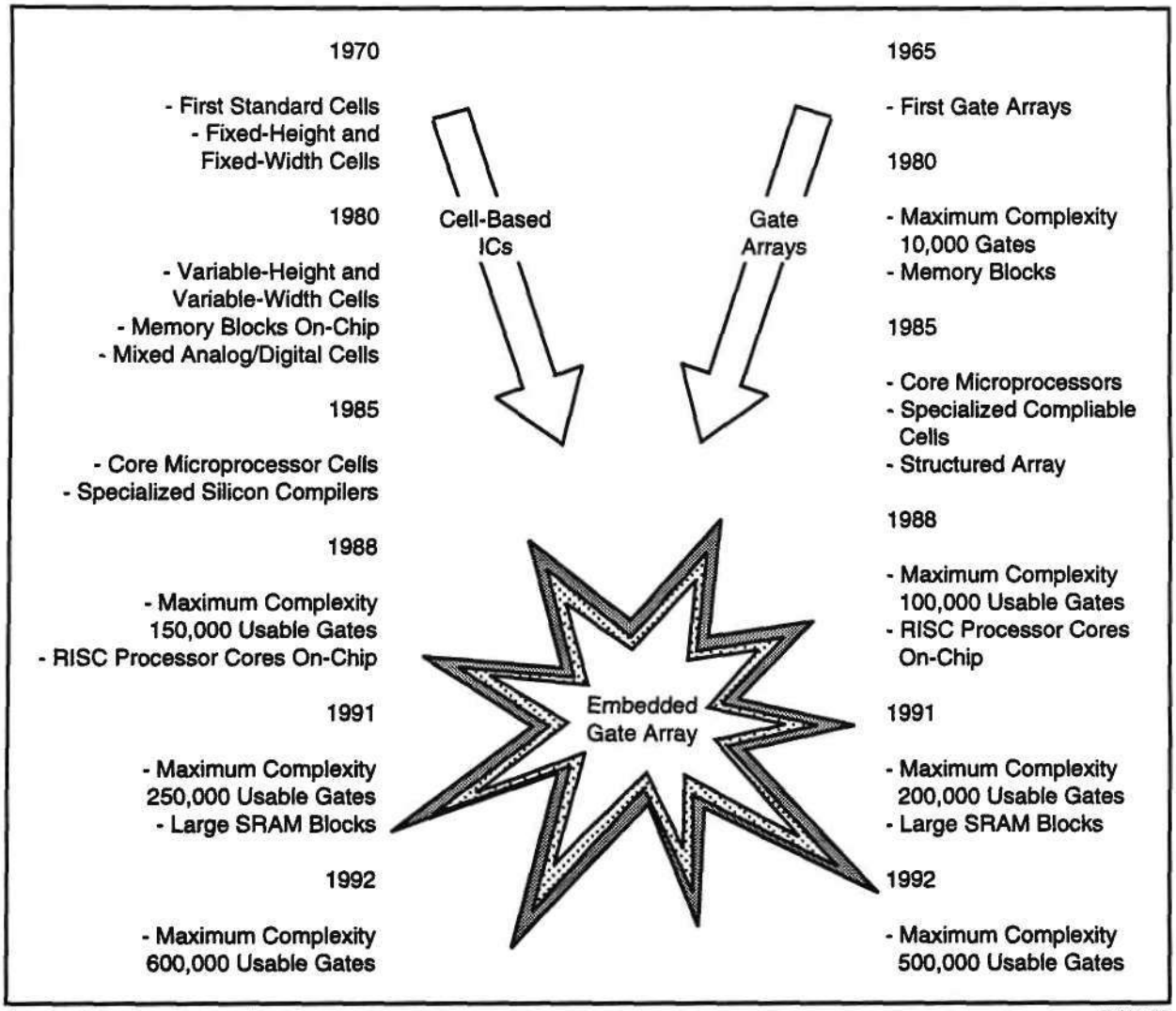
Dataquest includes all revenue, both merchant and captive, for semiconductor suppliers selling to the merchant market. Dataquest's consumption estimates do not include captive-only manufacturing companies represented by companies such as Digital Equipment Corporation, IBM, or Unisys that do not sell semiconductor products in the merchant market.

Despite the care taken in gathering, analyzing, and categorizing the data in a meaningful way, careful attention must be paid to the definitions and assumptions used herein when interpreting the estimates presented in this report. Various companies, government agencies, and trade associations may use slightly different definitions of product categories and regional groupings, or they may include different companies in their summaries. These differences should be kept in mind when making comparisons between data and numbers provided by Dataquest and those provided by other suppliers.

Chapter 3
Gate Array and Cell-Based IC Product Evolution

To get a better understanding of ASIC products, it is helpful to examine gate array and cell-based IC product evolution (see Figure 3-1).

Figure 3-1
Gate Array and CBIC Production Evolution



Source: Dataquest (December 1992)

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The first gate arrays were introduced to the industry in the mid-1960s by companies such as IBM and Fujitsu. They comprised a configuration of uncommitted logic elements (32 gates) on a prefabricated base wafer that were then customized by applying one final mask layer of interconnect. Most gate arrays were used for replacement of standard logic until the early 1980s, when higher-gate-count devices emerged and made single-chip systems practical. Memory blocks were brought on-chip in 1984. Complex cells such as processor cores emerged in 1985. By 1988, RISC on-chip microprocessor cores were announced and maximum densities had reached 100,000 usable gates. Today, large SRAM blocks and microprocessors are available, and maximum chip complexities are reaching 500,000 usable gates.

CBICs or standard cells did not emerge until a few years after the first gate arrays. IBM again was a leader in this area. It followed its master slice approach, which used generic gate arrays, with what IBM called the "open part number set" consisting of a library of cells. Early standard cells started with fixed-height and fixed-width cells, which were implemented through the late 1970s. After several years of development, the area inefficiency of fixed-height/fixed-width cells led to the addition of fixed-height/variable-width cell libraries. This was an interim stop on the way to today's variable-height/variable-width cell libraries. Megacells evolved as an aid to further improve efficiency in CBIC design, eliminating the need to reinvent the wheel every time a complex cell is needed. Memory blocks were brought on-chip in 1982, mixed analog/digital cells in 1984, and core microprocessors in 1985. Today, microprocessor cores and large SRAM blocks are available, and maximum chip complexities are reaching 600,000 gates.

During 1985, the embedded gate arrays concept was started by LSI Logic with a product called "structured arrays," which offered metal-configurable memory and large dedicated building blocks called megacells added to a logic array. The product was unsuccessful because new technology was needed to implement the product strategy. It was five years ahead of its time. During 1990, ASIC suppliers throughout the world began announcing products that utilized a similar concept with new technology and a new name—it is now called an embedded gate array. Instead of using metal-configurable memory and metal-configurable dedicated building blocks, these cells are now diffused in an embedded gate array base wafer that is more efficient than structured arrays. Embedded gate arrays offer reduced die size and increased performance, when compared with structured arrays and traditional gate arrays. In short, embedded gate arrays offer the reduced risk and turnaround time associated with gate arrays, along with increased functionality and performance associated with the CBICs. Embedded gate arrays are included in the gate array category because they are built from a prefabricated base wafer and the random logic is customized using the final routing layers.

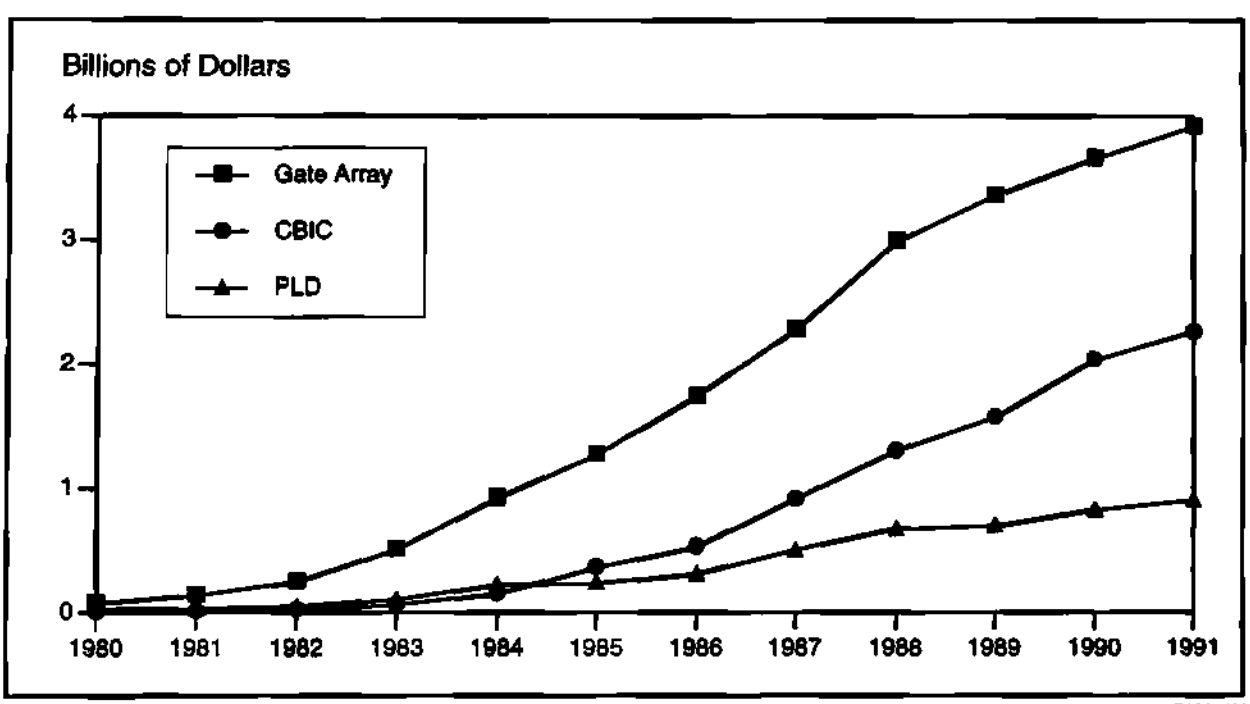
Chapter 4
ASIC Consumption Forecast

ASIC Forecast

The ASIC market without full-custom ICs has grown from less than $200 million to more than $7 billion during the past 10 years. The gate array market alone grew from $137 million in 1981 to more than $3.9 billion in 1991 (see Figure 4-1). CBICs and PLDs also experienced outstanding growth rates over the same period, with compounded annual growth rates of 81 percent and 41 percent, respectively.

Although Dataquest does not believe that growth rates in ASIC market will reach the same levels as in the past, the ASIC market is still expected to return to respectable growth rates after 1992 (see Figure 4-2). Table 4-1 shows Dataquest worldwide ASIC forecast by product and technology.

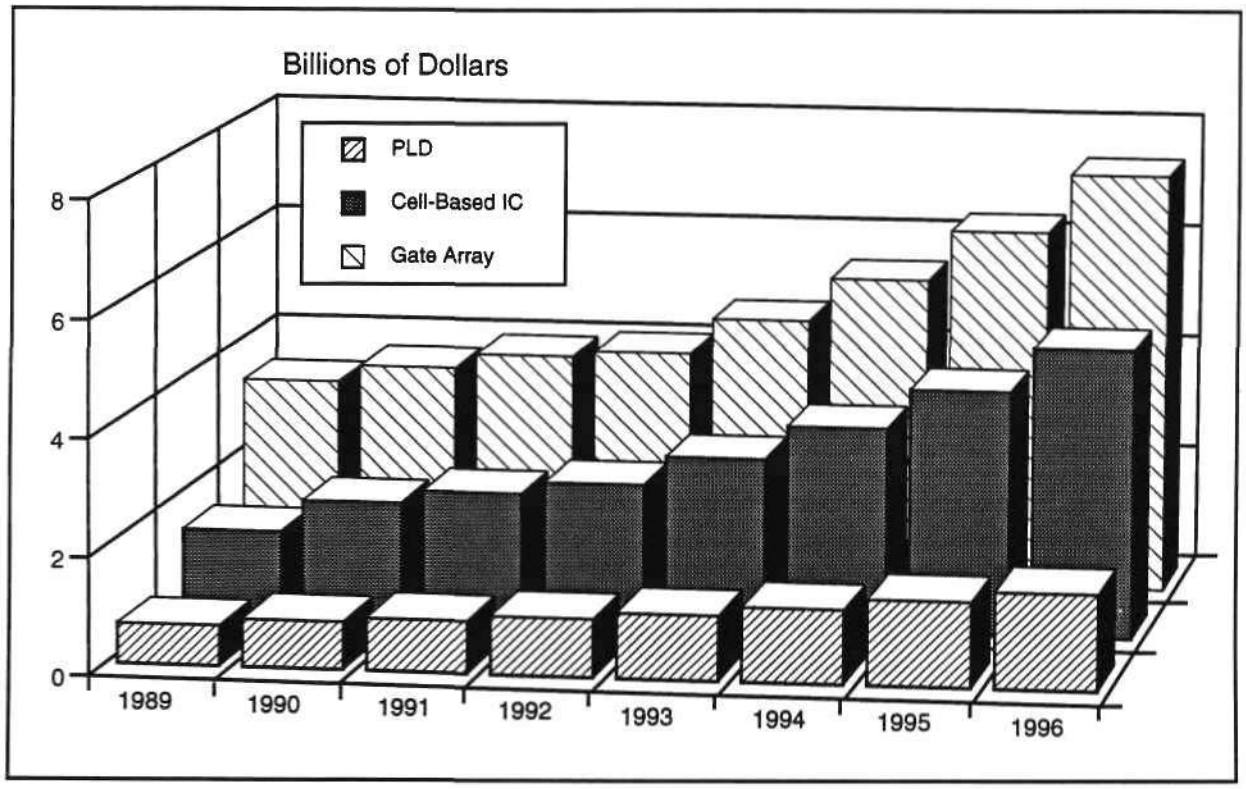
Figure 4-1
Estimated Worldwide ASIC Consumption History



Source: Dataquest (December 1992)

G2001439

Figure 4-2
Worldwide ASIC Consumption Forecast



Source: Dataquest (December 1992) G2001439

Key assumptions incorporated in the 1992 ASIC forecast include the following:

- The 1992 worldwide ASIC market is expected to experience the lowest growth rate in history at 3.5 percent (including full-custom ICs). This is primarily because Japan, a country that accounts for more than 40 percent of the worldwide ASIC market, has entered a recession.
- The Japanese economy will return to typical positive growth rates in the third and fourth quarters of 1992. Furthermore, we assume that the North American economy will pull out of its recession in the fourth quarter of 1992. This forecast should be considered overly optimistic if these assumptions on Japan and North America do not materialize.
- The 1992 European ASIC market is expected to experience growth similar to that of 1991.
- The personal computer clone market experienced severe price erosion during 1991, which caused the 1991 Asia/Pacific-Rest of World ASIC market to stall. The 1992 Asia/Pacific-Rest of World growth rate is expected to return to a more typical 20 percent as companies in this region diversify into other application markets, such as the consumer market.

Table 4-1
Revenue from ASICs, by Technology Shipped to the World (Millions of U.S. Dollars)

	1989	1990	1991	1992	1993	1994	1995	1996	CAGR (%) 1991-1996
Total ASIC	8,123	8,997	9,519	9,839	11,016	12,413	14,042	15,878	10.8
MOS ASIC	5,930	6,765	7,363	7,723	8,818	10,029	11,337	12,696	11.5
Bipolar ASIC	2,071	2,061	1,924	1,772	1,665	1,542	1,416	1,280	-7.8
BiCMOS ASIC	122	171	232	344	533	842	1,289	1,902	52.3
Total Gate Array	3,355	3,654	3,914	4,016	4,649	5,418	6,301	7,334	13.4
MOS Gate Array	2,150	2,405	2,671	2,773	3,313	3,919	4,551	5,239	14.4
Bipolar Gate Array	1,110	1,117	1,074	998	961	907	844	768	-6.5
BiCMOS Gate Array	95	132	169	245	375	592	906	1,327	51.0
Total PLD	695	824	902	1,003	1,118	1,274	1,462	1,643	12.7
MOS PLD	263	401	559	722	890	1,093	1,320	1,535	22.4
Bipolar PLD	432	423	343	281	228	181	142	108	-20.6
Total Cell-Based IC	1,469	2,033	2,258	2,470	2,969	3,549	4,231	4,990	17.2
MOS Cell-Based IC	1,364	1,893	2,103	2,281	2,722	3,212	3,762	4,331	15.5
Bipolar Cell-Based IC	78	101	92	90	89	87	86	84	-1.8
BiCMOS Cell-Based IC	27	39	63	99	158	250	383	575	55.6
Full Custom IC	2,604	2,486	2,445	2,350	2,280	2,172	2,048	1,911	-4.8

Source: Dataquest (December 1992)

- Application-specific standard products (ASSPs) will continue to experience rapid proliferation and will further reduce the growth of the ASIC market.
- Full-custom ICs are being replaced by gate arrays and CBICs, both of which offer reduced NRE charges and a quicker time-to-market when compared with full-custom ICs.

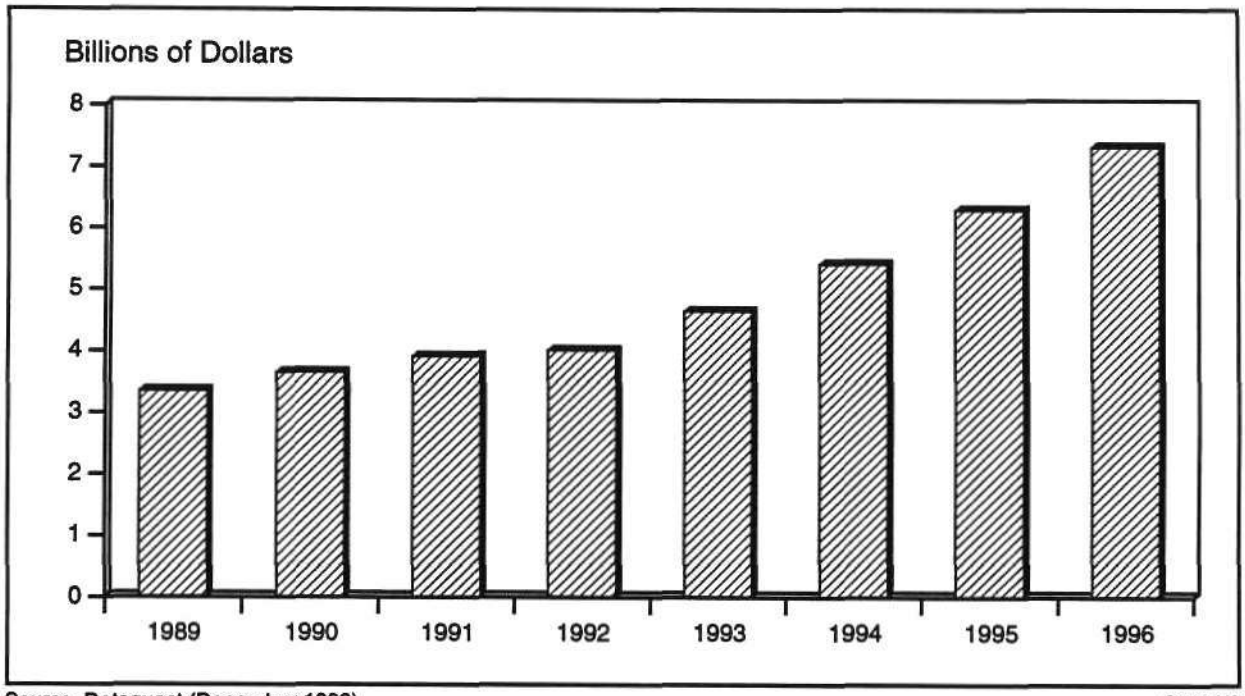
Gate Array Forecast

The gate array market is expected to grow from $3.9 billion in 1991 to more than $7.3 billion by 1996 (see Figure 4-3). MOS gate arrays are expected to continue to dominate the gate array market, while BiCMOS gate arrays are expected to gain market share (see Figure 4-4). Figure 4-5 shows that Japan is the largest consumer of gate arrays in the world.

Assumptions incorporated in the gate array forecast by technology are as follows:

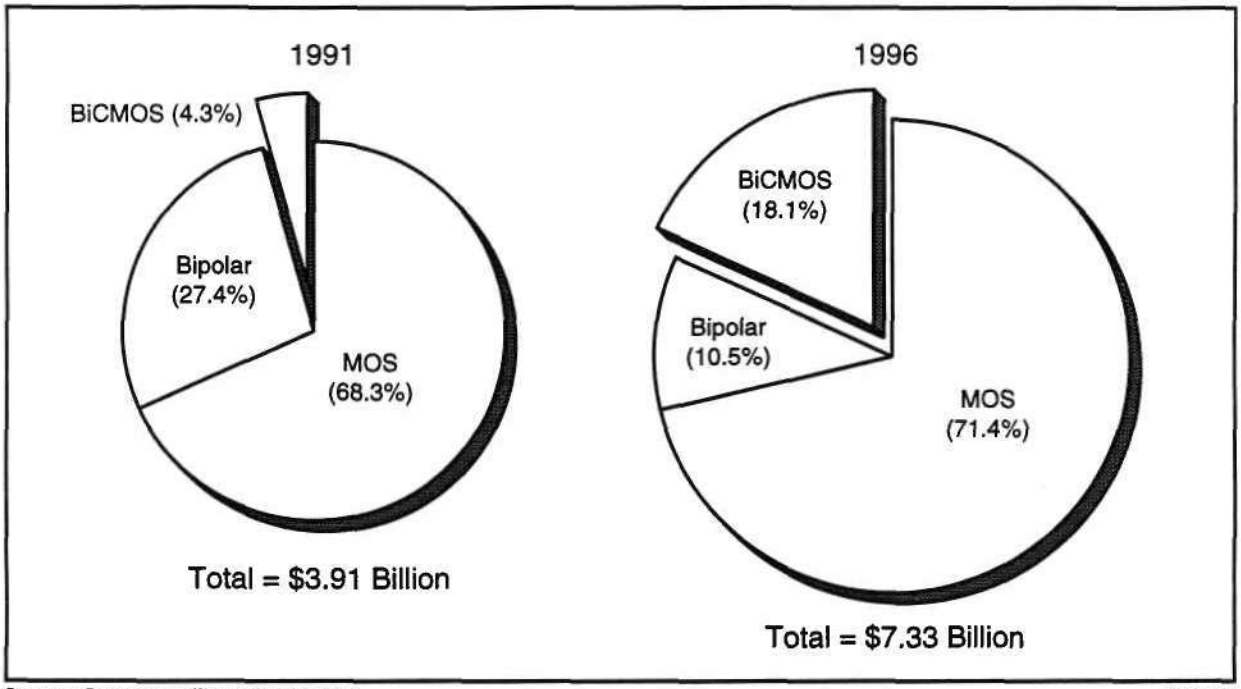
- MOS gate arrays
  - CMOS continues to be the dominant gate array technology for the foreseeable future because of its low cost, low power consumption, and high integration.
  - The North American CMOS gate array market will closely track the computer market because more than 60 percent of all gate arrays are consumed in data processing applications.

Figure 4-3
Estimated Worldwide Gate Array Consumption Forecast



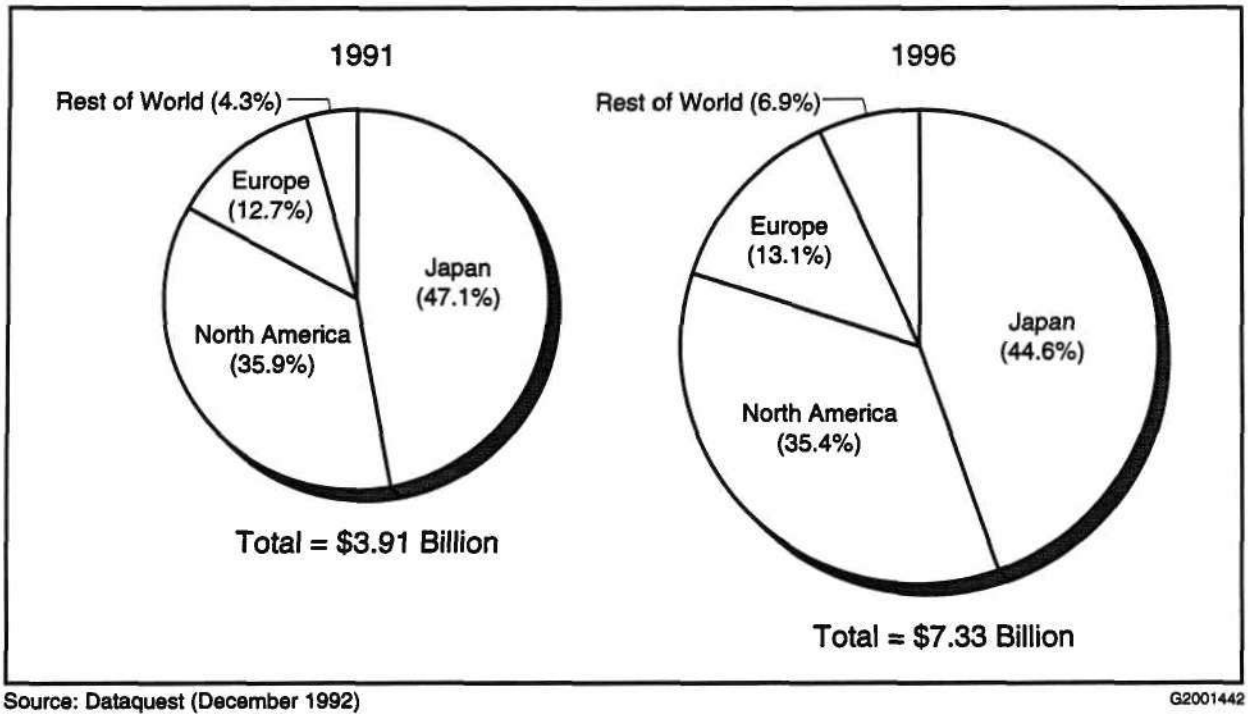
Source: Dataquest (December 1992) G2001440

Figure 4-4
Estimated Worldwide Gate Array Consumption, by Technology



Source: Dataquest (December 1992) G2001441

Figure 4-5
Estimated Worldwide Gate Array Consumption, by Region



Source: Dataquest (December 1992) G2001442

- The low-end CMOS market (less than 20,000 gates) will continue to be adversely impacted by field-programmable gate arrays (FPGAs).
- Embedded gate arrays (that is, megacells such as SRAMs that are diffused in the array base wafer) are included in the gate array category and are expected to fuel gate array growth by the mid-1990s.
- Although we believe that the price-per-gate will continue to drop, average selling prices are still expected to increase because of the increasing use of on-chip functions such as SRAM, arithmetic logic units (ALUs), multiplier, multiplier-accumulator, first in/first out (FIFO), direct memory access (DMA) controller, cache controller, and 82xx microperipherals.

■ Bipolar gate arrays

- Bipolar gate arrays are being replaced by CMOS, BiCMOS, and GaAs ASICs because of their high cost and high power consumption.
- The TTL gate array market is declining, primarily because there have been no new TTL arrays designed in the past three years, and production of these devices is accordingly winding down.
- The ECL gate array market is declining in all regions because most ECL arrays are consumed in large mainframe and supercomputers, which are both declining markets.

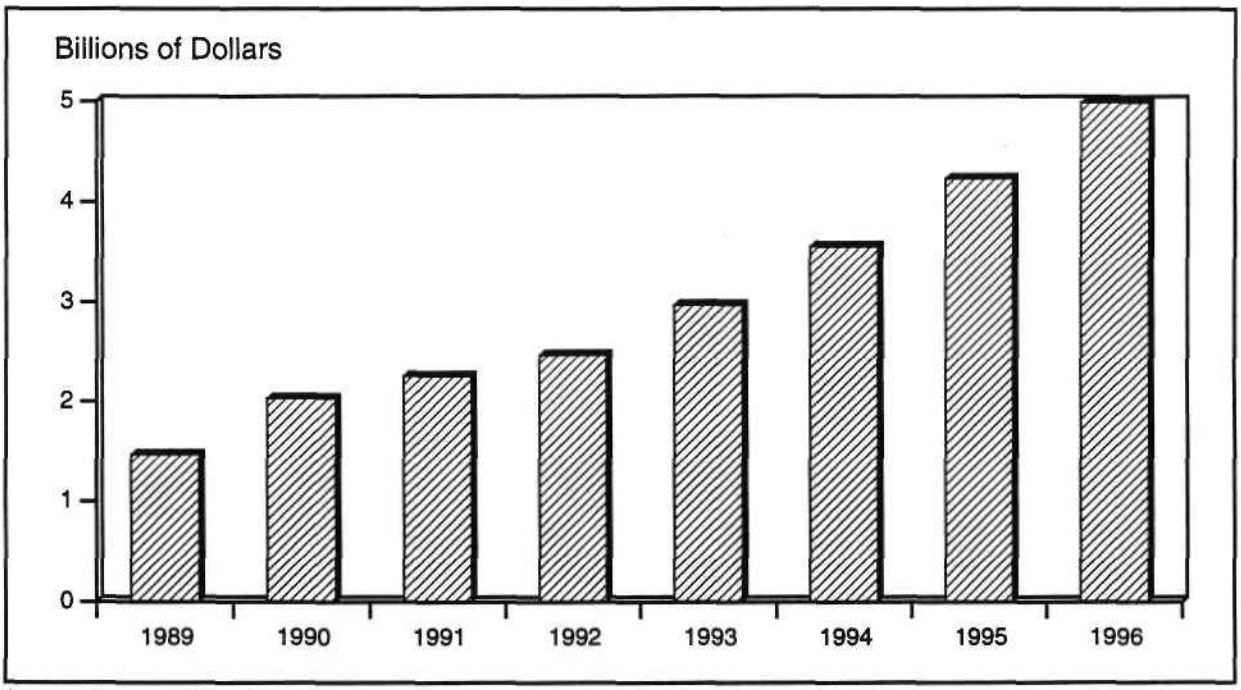
■ BiCMOS gate arrays

- BiCMOS gate array growth has been pushed out one to two years from our previous forecast because of the lack of high-volume production from vertically integrated companies such as Fujitsu, NEC, and AT&T. At this point, the costs of these BiCMOS devices do not outweigh the benefits from BiCMOS, in comparison to CMOS.
- According to Dataquest's worldwide end-user survey of more than 500 system designers, we observed that there is strong interest in using BiCMOS ASICs in next-generation system design.

CBIC Forecast

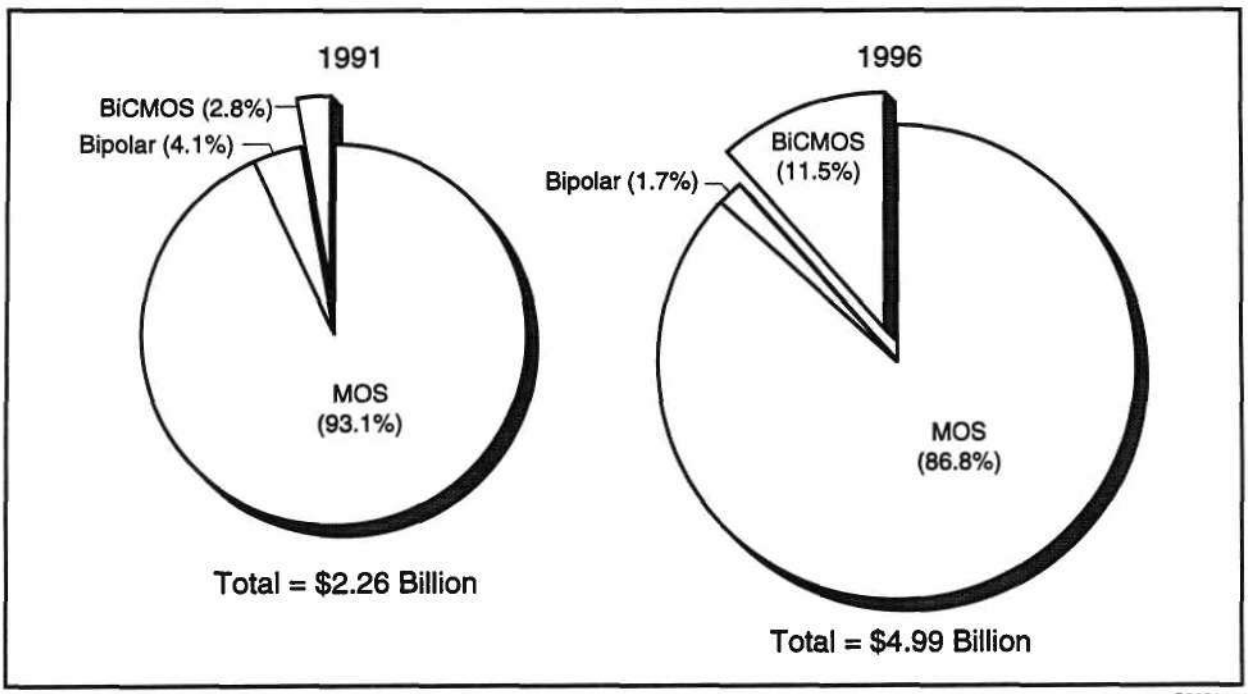
The CBIC market is expected to grow from $2.3 billion in 1991 to about $5 billion by 1996 (see Figure 4-6). As in the gate array market, MOS will be the dominant technology, with BiCMOS gaining market share (see Figure 4-7). Contrary to the gate array market, North America is the largest consumer of CBICs; however, Japan is gaining market share (see Figure 4-8).

Figure 4-6
Estimated Worldwide CBIC Consumption Forecast



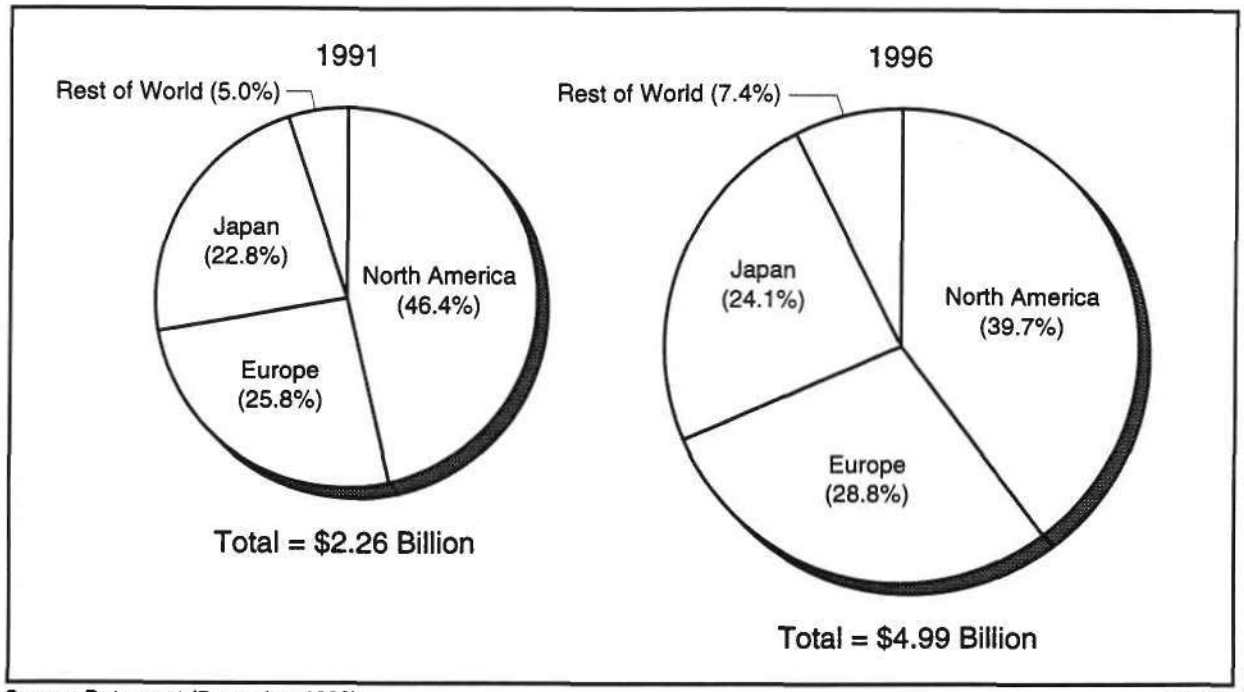
Source: Dataquest (December 1992) G2001443

Figure 4-7
Estimated Worldwide CBIC Consumption, by Technology



Source: Dataquest (December 1992) G2001444

Figure 4-8
Estimated Worldwide CBIC Consumption, by Region



Source: Dataquest (December 1992) G2001445

Key assumptions used in the CBIC forecast are as follows:

- MOS CBICs
  - Gate arrays will continue to penetrate many CBIC applications because of their low pricing attributed to the vast number of suppliers as well as their increasing functionality and performance associated with the emerging embedded gate array.
  - CBIC use in Japan will increase (at the expense of gate arrays) in high-volume applications such as video games, printers, and disk drives, mainly because of the smaller die size of CBICs.
  - Telecommunications applications are driving the CBIC growth in Europe.
- Bipolar CBICs
  - Bipolar CBIC growth stems from two product types: ECL CBICs and analog CBICs.
  - ECL CBICs are expected to experience negative growth, primarily because system designers do not want macros supplied by ASIC vendors; system designers want to design their own macros on the transistor level to optimize their designs for their unique applications.

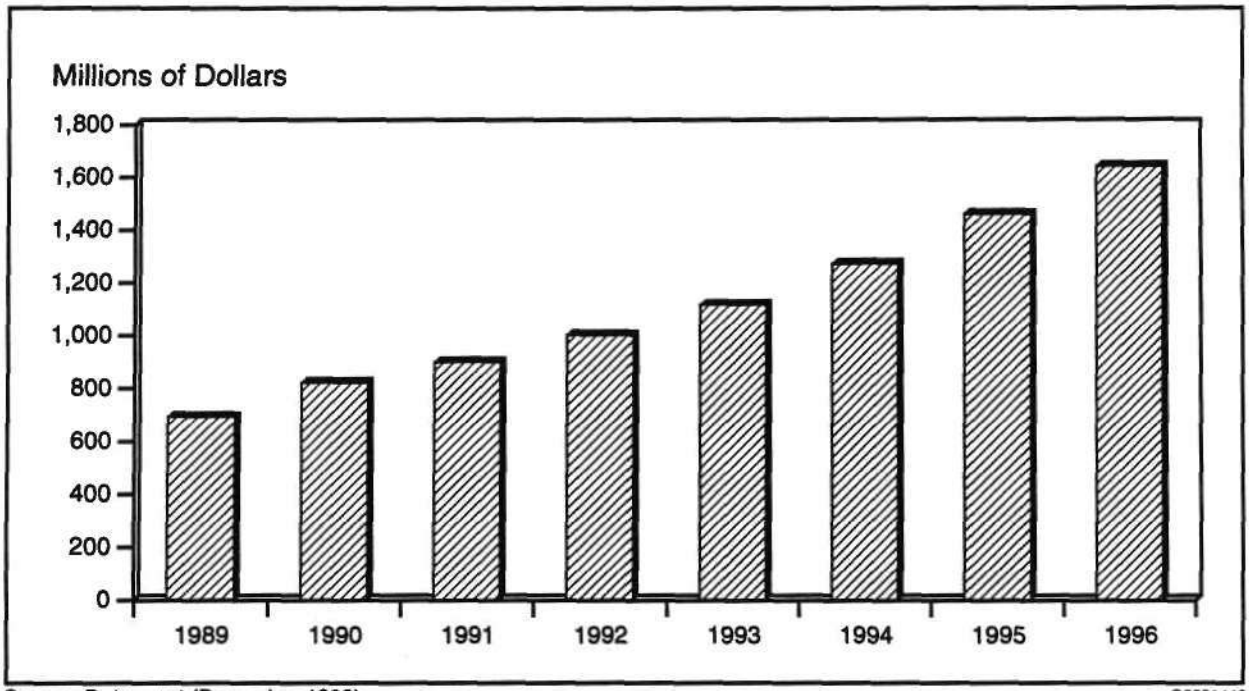
- Analog CBICs such as National's "Classic" line are expected to experience modest growth.

- BiCMOS CBICs
  - BiCMOS CBICs are a good solution for mixed analog/digital applications. The analog portion can be implemented using bipolar technology and the digital portion with CMOS technology.
  - BiCMOS CBICs are expected to be used in many telecom applications.

PLD Forecast

Although the PLD market is not as large as the gate array or CBIC market, it is expected to see solid growth from $900 million in 1991 to $1.6 billion by 1996 (see Figure 4-9). The MOS portion of the PLD market is experiencing rapid growth at the expense of bipolar PLDs (see Figure 4-10). FPGAs are the fastest growing MOS PLD market (see Figure 4-11). Japan is the fastest growing region for PLDs; however, North America is the largest market (see Figure 4-12).

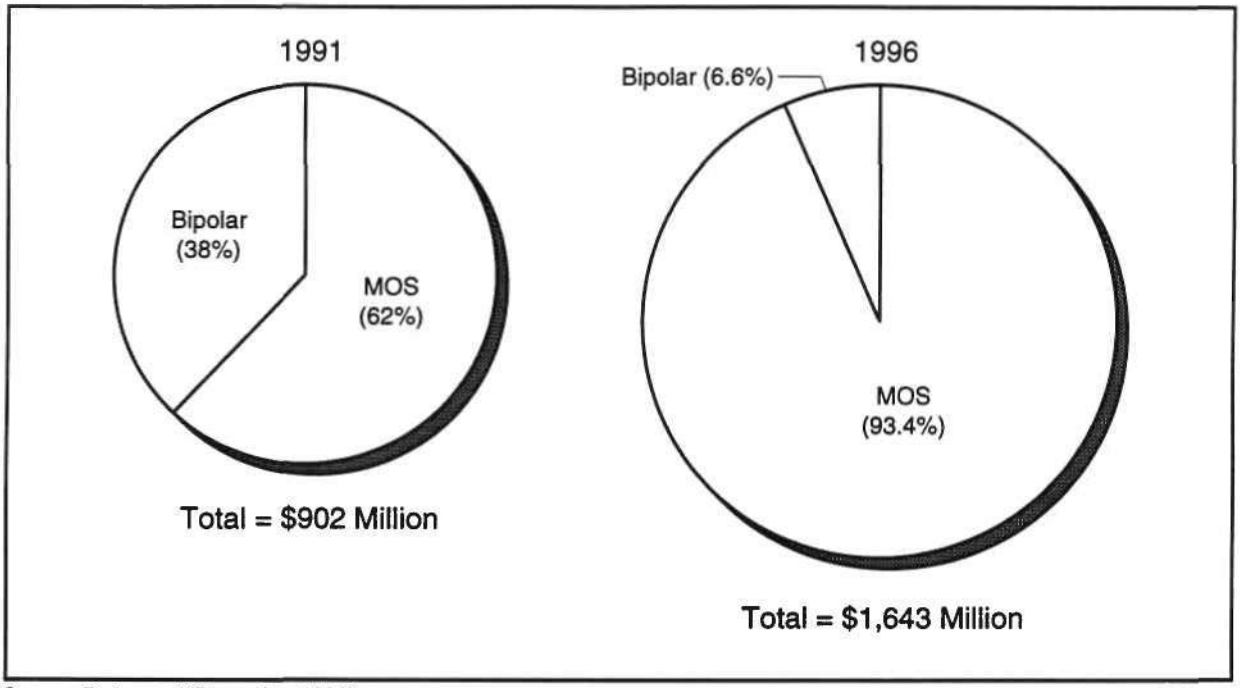
Figure 4-9
Estimated Worldwide PLD Consumption Forecast



Source: Dataquest (December 1992)

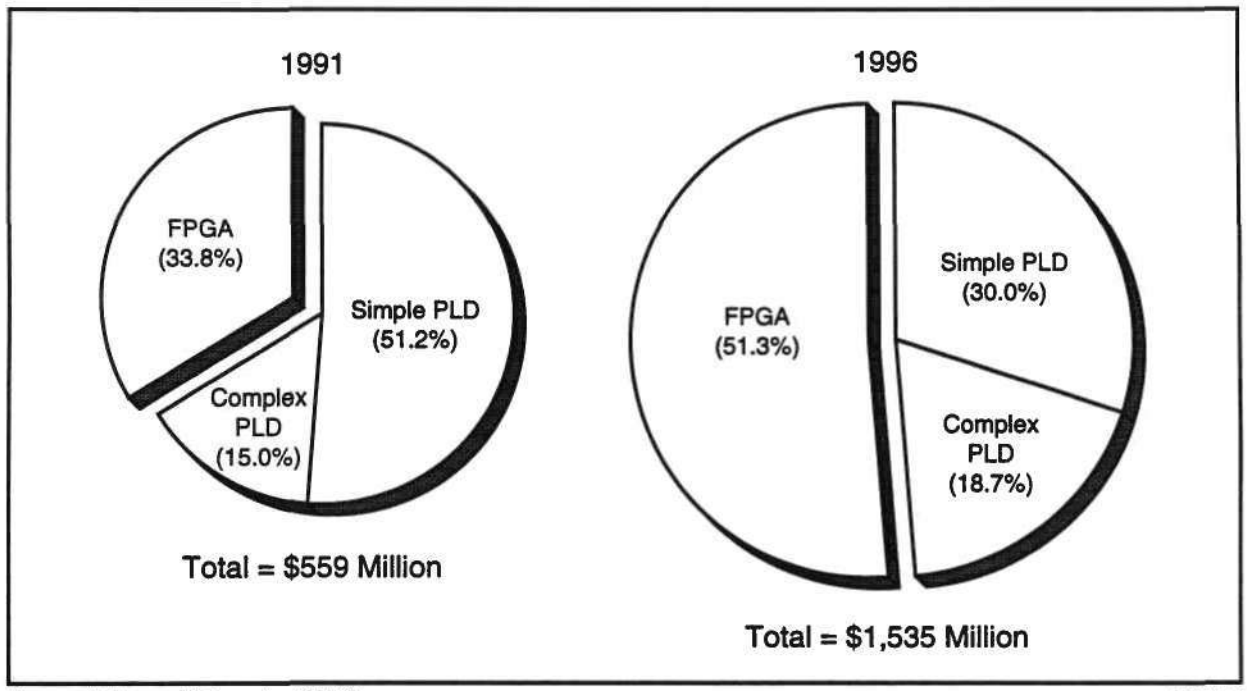
G2001446

Figure 4-10
Estimated Worldwide PLD Consumption, by Technology



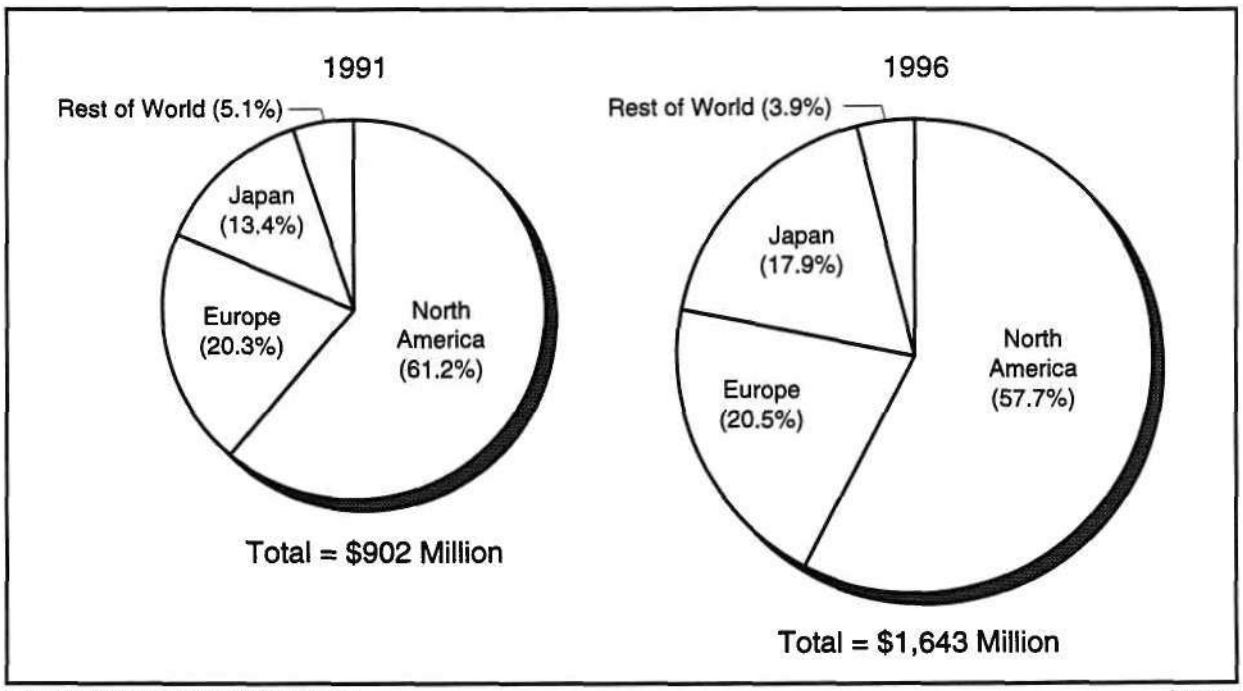
Source: Dataquest (December 1992) G2001447

Figure 4-11
Estimated Worldwide CMOS PLD Consumption, by Logic Complexity



Source: Dataquest (December 1992) G2001448

Figure 4-12
Estimated Worldwide PLD Consumption, by Region



Source: Dataquest (December 1992) G2001449

Key assumptions in the PLD forecast include the following:

- CMOS PLDs
  - CMOS PLD growth stems from three types of devices: simple PLDs (SPLDs), complex PLDs (CPLDs), and FPGAs.
  - The SPLD market is expected to track just above overall semiconductor growth over the next few years. However, growth rates will continue to fall as these small devices are replaced with higher-density CPLDs and FPGAs.
  - Dataquest believes that CPLDs will continue to show robust growth. However, short-term growth has been stunted for the following reasons:
    - Pricing pressure between Altera and second-source Cypress
    - Lack of other significant entrants besides AMD and Lattice
    - Continued competition with higher-density FPGAs
  - CPLDs will continue to hold slight ease-of-use and speed advantages over FPGAs.

- The FPGA market is expected to show excellent growth over the next five years for the following reasons:
  - There continues to be a shift from TTL- and PAL-based designs toward FPGA usage.
  - FPGAs will attack not only the low-end gate array market (less than 10,000 gates), but also the 10,000- to 20,000-gate array market in the 1993 to 1995 time frame as gate array vendors migrate to high-complexity devices.
  - Additional market impetus will come from the large number of new entrants into the market, including hot start-up companies and the Japanese companies.

- Bipolar PLDs
  - The bipolar PLDs market is clearly declining because of a shift in consumption from bipolar PLDs to CMOS PLDs.
  - This market will continue to decline until only a few high-speed ECL devices and specialty high-drive PLDs remain.

For further ASIC forecast information, please see the worldwide ASIC forecast document, *ASIC Consumption Forecast*.

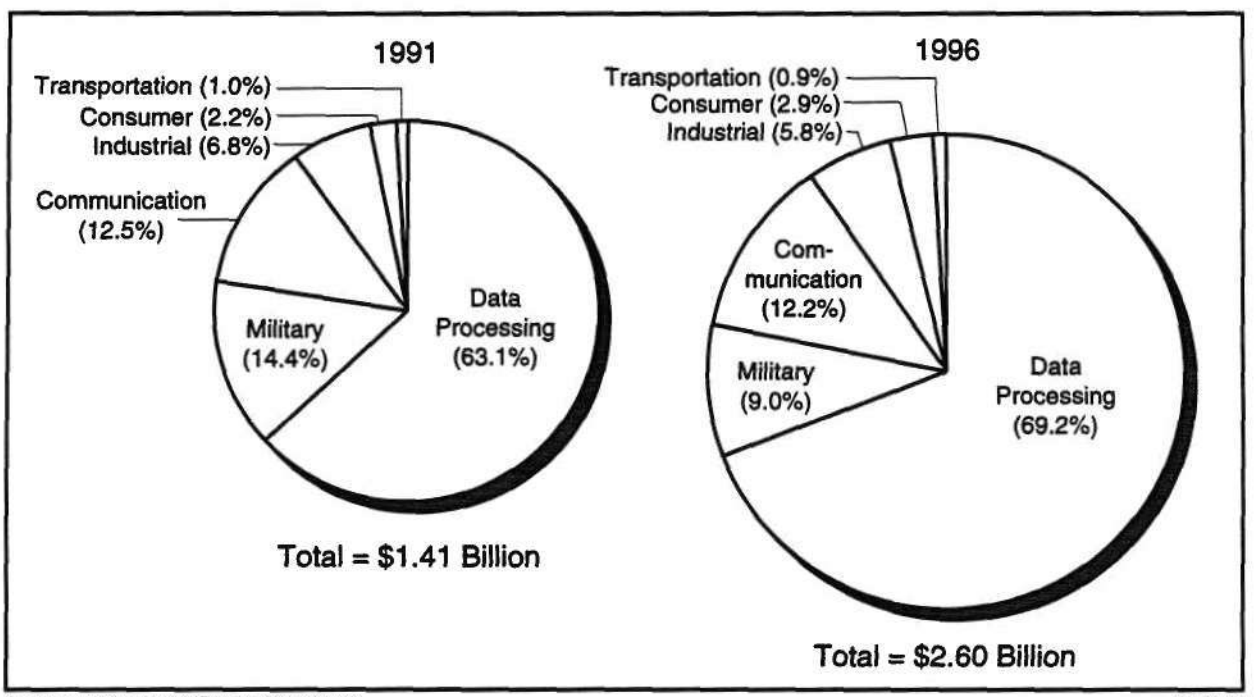
Chapter 5
Application Trends

ASICs are pervasive in today's electronic system design. ASIC applications range from simple speak-and-spell toys to the fastest computers in the world. In this chapter, we will compare and contrast the North American gate array and CBIC application markets and then explore applications driving the ASIC market.

North American Application Markets

The largest use of gate arrays is in data processing application (see Figure 5-1). Although the gate array military market is still growing, it is declining as a percentage of the total gate array revenue market because of federal budget cuts. Data processing applications are also the largest market for CBIC products; however, communication is a much larger market for CBICs than for gate arrays (see Figure 5-2 and Figure 5-3).

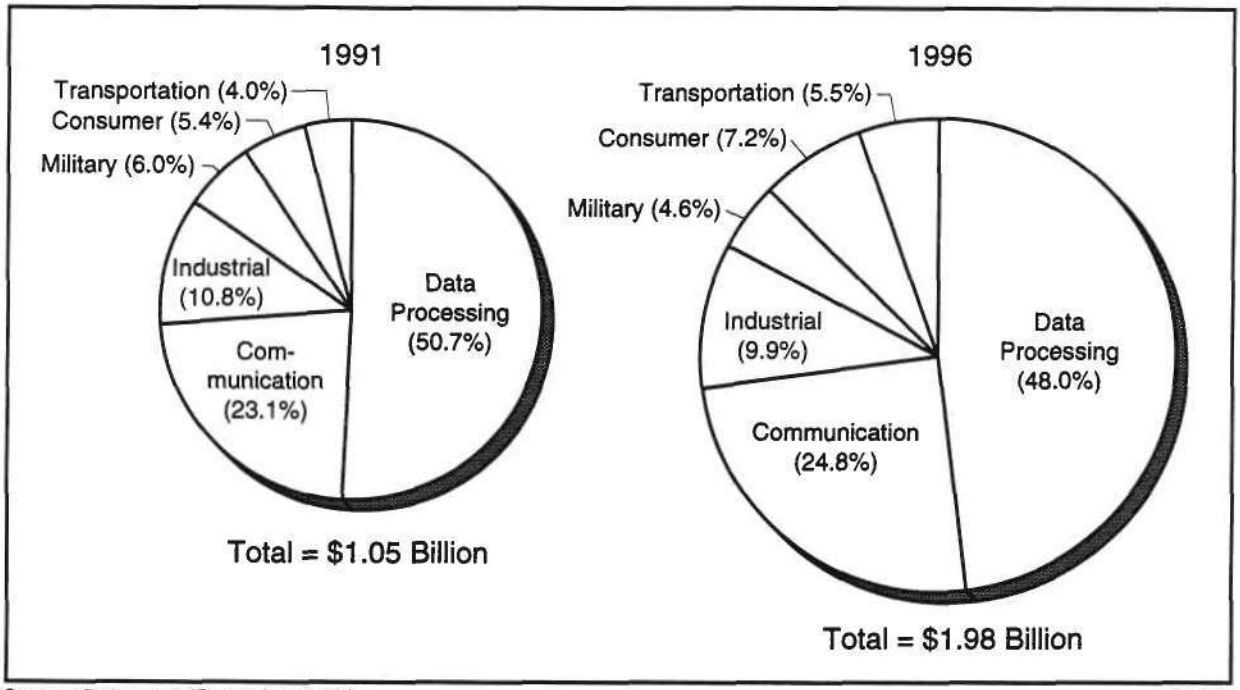
Figure 5-1
Estimated North American Gate Array Consumption, by Application Market



Source: Dataquest (December 1992)

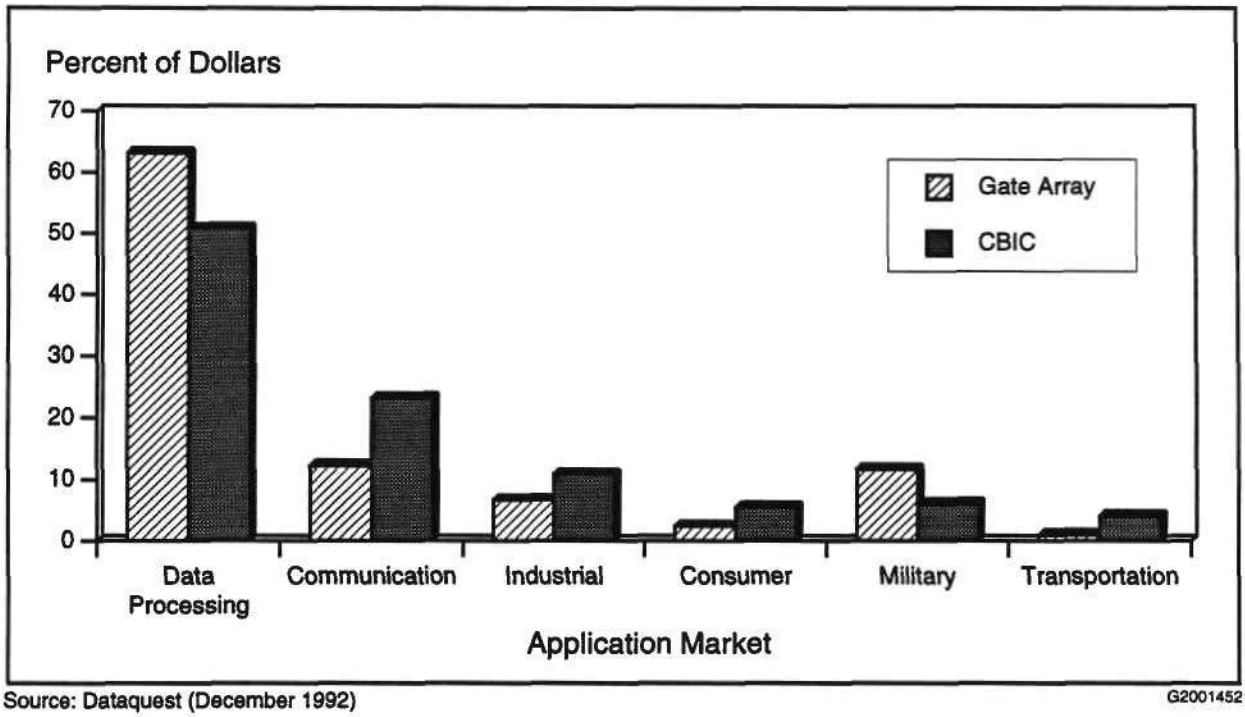
G2001450

Figure 5-2
Estimated North American CBIC Consumption, by Application Market



Source: Dataquest (December 1992)
G2001451

Figure 5-3
Estimated 1991 North American ASIC Consumption, by Application Market



Source: Dataquest (December 1992)
G2001452

ASIC Applications Drive Growth

Data Processing

Data processing is defined as computer systems, data storage devices, input/output devices (that is, media-to-media data conversion, scanning equipment, plotters, and voice recognition/synthesizer equipment), electronic printers, and office equipment (that is copiers, duplicators, and electronic calculators).

Key data processing products that consume large quantities of ASICs include the following:

- Workstations and PCs
- Midrange computers, mainframes, and supercomputers
- Disk drives
- Electronic printers
- Copiers

Emerging data processing products with ASIC opportunity include the following:

- Portable computers
- 2.5-inch and 1.8-inch disk drives
- Video compression and decompression
- Digital video (color space conversion, image digitizing)

Subsystems within data processing products often implemented in ASICs include the following:

- Glue logic consolidation
- Central processing unit
- Graphic processor
- Memory manager
- I/O manager
- Disk drive controller
- Floating-point register
- Network controller
- Bus interface
- Cache controller

Communication

Communication is defined as personal communication, networking, image communication, and voice communication.

Applications for ASICs in the communications segment include the following:

- PBX
- Central office switching systems
- T1-multiplexing
- Modems
- LANs
- ISDN
- Line cards
- Fiber-optic transmission
- Encryption

Industrial

Industrial is defined as test equipment, manufacturing systems, process control equipment, instrumentation, medical equipment, and robotics.

Applications for ASICs in the industrial segment include the following:

- Automated test equipment
- Medical CAT scanners
- Logic analyzers
- Motor control
- Robotics

Military

Military is defined as military electronic equipment.

Applications for ASICs in the military segment include the following:

- Radar
- Sonar
- Missile guidance and control
- Navigation
- Reconnaissance
- Flight simulators

Transportation

Transportation is defined as in-car entertainment systems, body control electronics, driver information, power train electronics, safety electronics, and convenience electronics.

Applications for ASICs in the transportation segment include the following:

- Automatic braking systems
- Active suspension
- Collision avoidance systems
- Multiplex systems such as driver door and steering wheel
- Electronic instrument clusters
- Power train controls
- Engine management

Dataquest Perspective

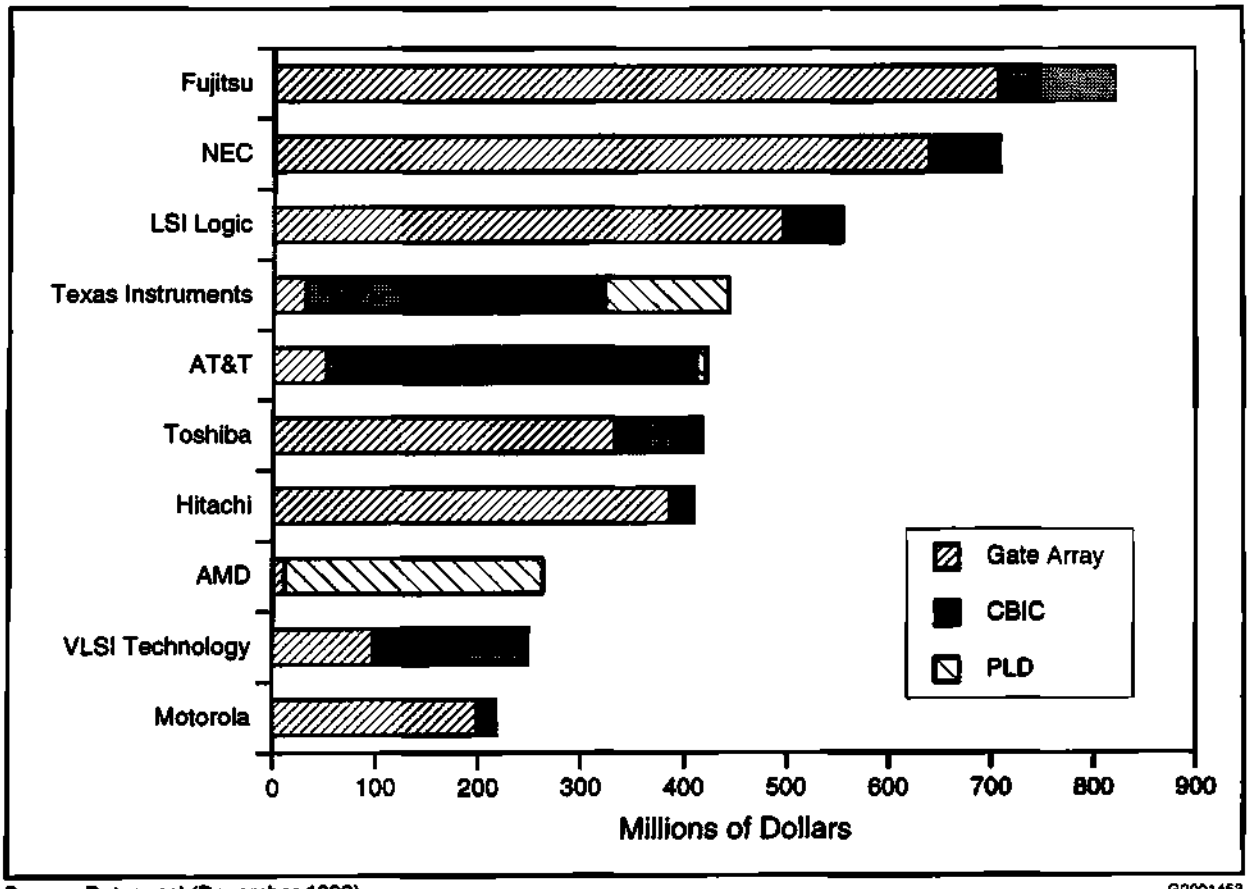
As can be seen from the list of ASIC applications, there is a broad market for ASIC technology. Strong market pull for ASIC technology translates to a healthy revenue opportunity, but, of course, this does not necessarily equate to sustainable profitability.

Chapter 6
Supplier Trends

ASIC Supplier Trends

Of the top 10 1991 worldwide ASIC suppliers (excluding full-custom ICs), 4 are Japanese companies and 6 are North American companies (see Figure 6-1). The four Japanese companies are vertically integrated system suppliers; only one of the North American suppliers is. Three of the North American suppliers are broad-based semiconductor suppliers; only two are focused ASIC suppliers.

Figure 6-1
Top 10 1991 Worldwide ASIC Suppliers



Source: Dataquest (December 1992)

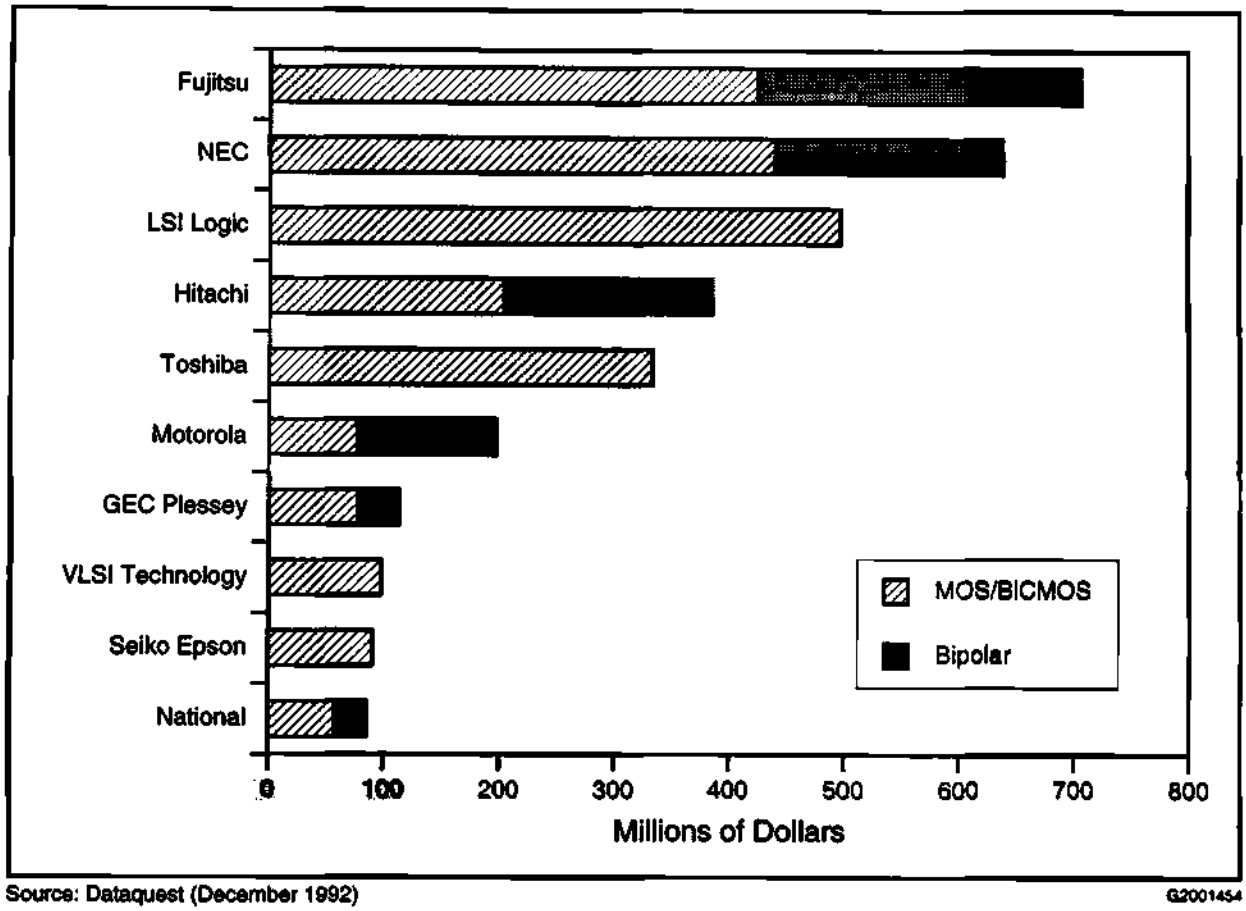
G2001453

In this chapter, Dataquest will first look at the leading suppliers in each product area and then explore the challenges facing different types of ASIC suppliers.

Gate Array Supplier Trends

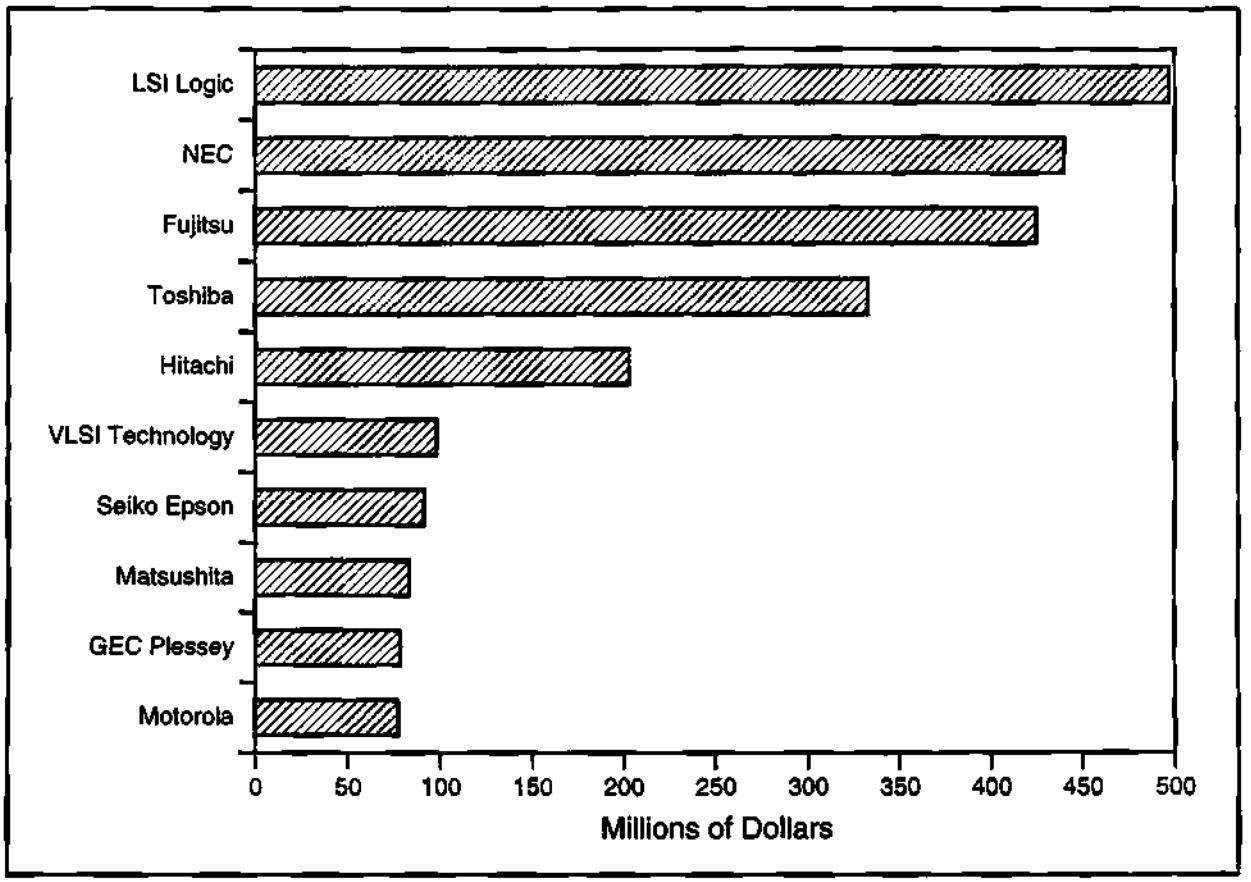
Of the top 10 1991 worldwide gate array suppliers, 5 are Japanese companies, 4 are North American, and 1 is European (see Figure 6-2). Although LSI Logic is ranked third behind Fujitsu and NEC in total gate array sales, it is the largest merchant gate array supplier because Fujitsu and NEC sell 40 to 50 percent of their gate arrays to internal divisions. Not only is LSI Logic the largest merchant gate array supplier, it is also the largest worldwide MOS gate array supplier (see Figure 6-3). NEC was ranked ahead of LSI Logic in preliminary 1991 MOS gate array market share rankings. NEC was subsequently revised downward in the final market share rankings, along with many Japanese companies, because Dataquest believed that the preliminary estimates were too high.

Figure 6-2
Top 10 1991 Worldwide Gate Array Suppliers



Source: Dataquest (December 1992) G2001454

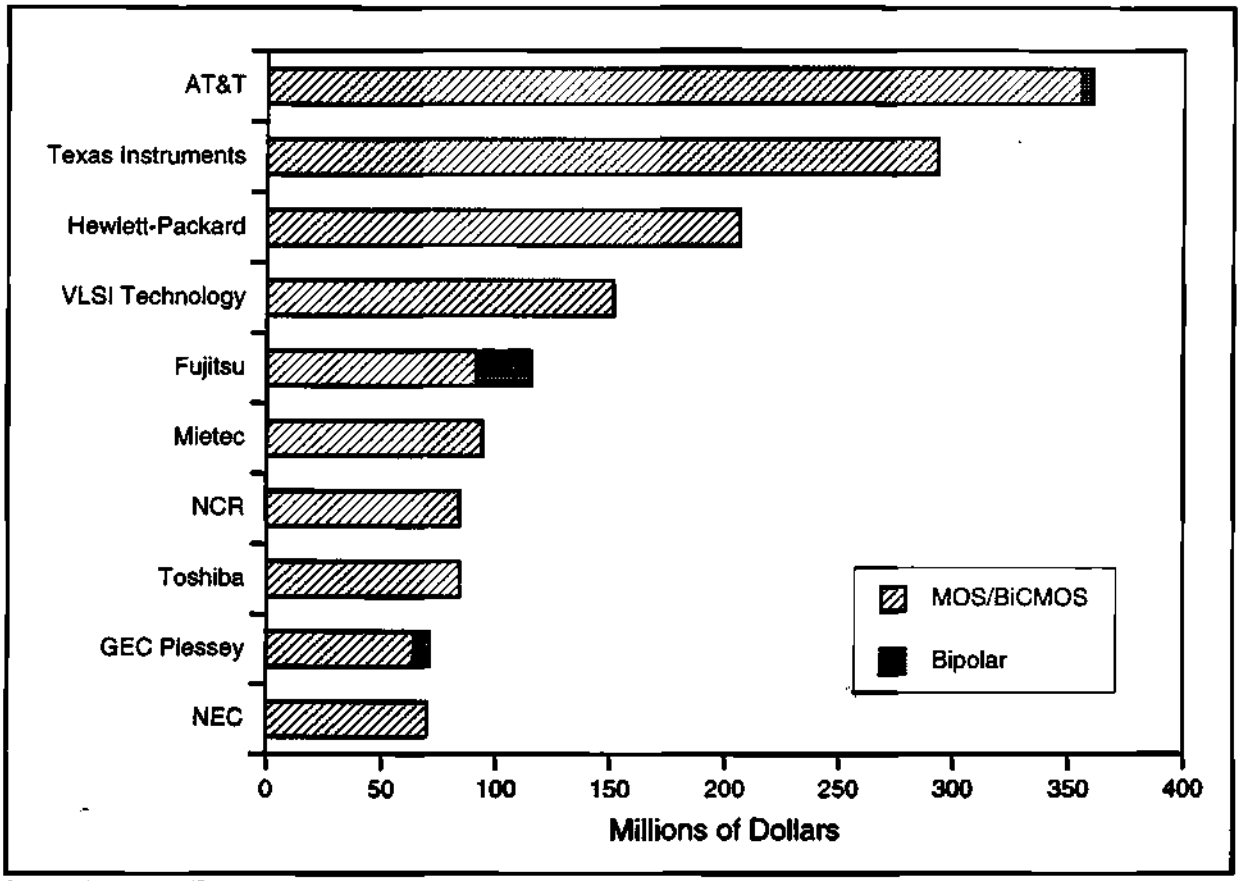
Figure 6-3
Top 10 1991 Worldwide MOS/BiCMOS Gate Array Suppliers



Source: Dataquest (December 1992) G2001455

The top 10 1991 worldwide gate array suppliers lost market share, compared with the top 10 1990 suppliers: 80.4 percent of the total market in 1991 versus 81.3 percent in 1990.

Figure 6-4
Top 10 1991 Worldwide CBIC Suppliers

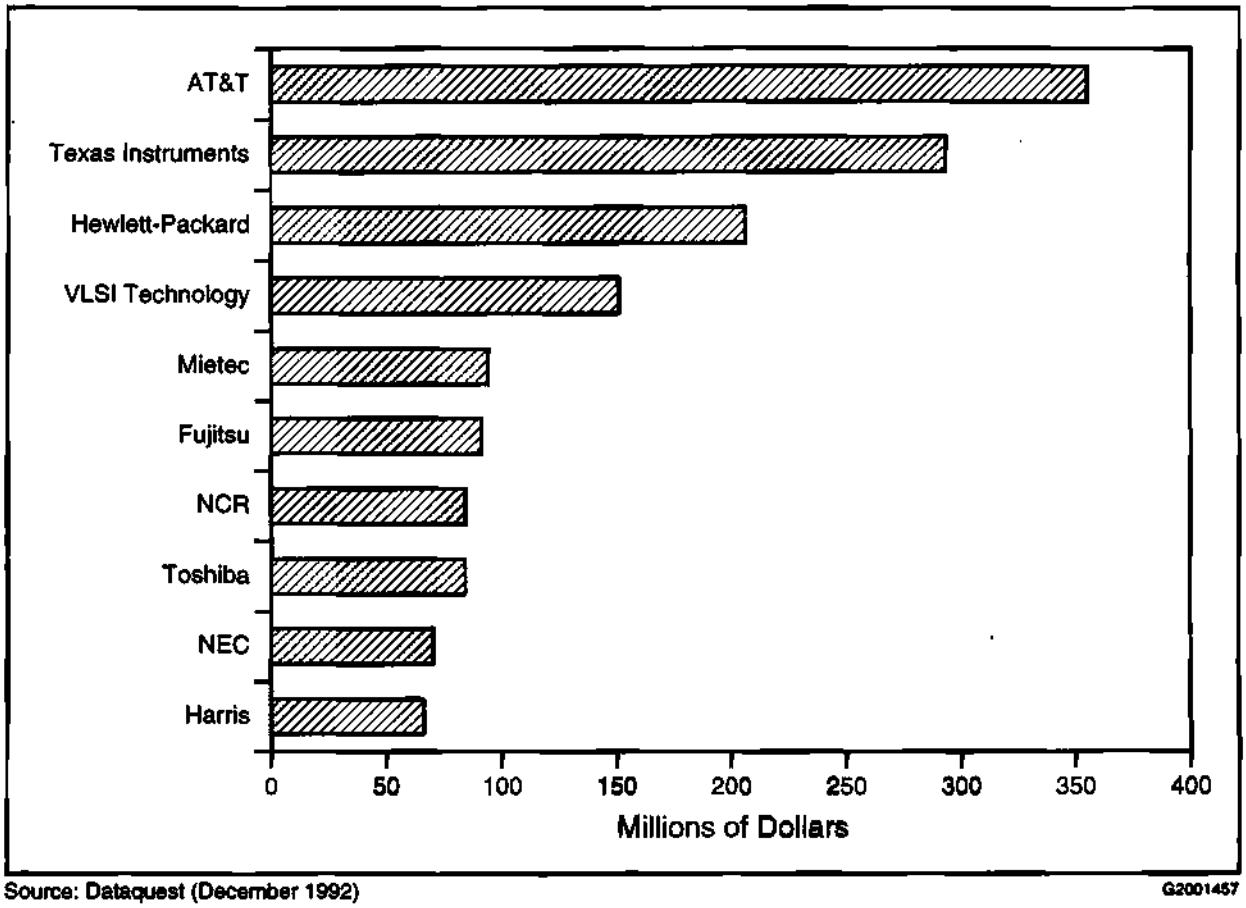


Source: Dataquest (December 1992) G2001456

CBIC Supplier Trends

Contrary to the gate array market, 5 of the top 10 worldwide 1991 CBIC suppliers were North American companies, 3 are Japanese, and 2 are European (see Figure 6-4). North American companies pioneered the CBIC market and still retain a substantial lead over the Japanese. Although AT&T is the largest 1991 CBIC supplier, Texas Instruments is the largest merchant CBIC supplier because 40 to 50 percent of AT&T CBIC sales are to internal divisions. The majority of Hewlett-Packard sales are also to internal divisions. Figure 6-5 shows that the ranking for the top 10 MOS/BiCMOS suppliers remains relatively unchanged from the total CBIC ranking because there was only a small portion of bipolar sales. Mietec is the only top 10 CBIC company to capture a significant portion of its sales using BiCMOS technology.

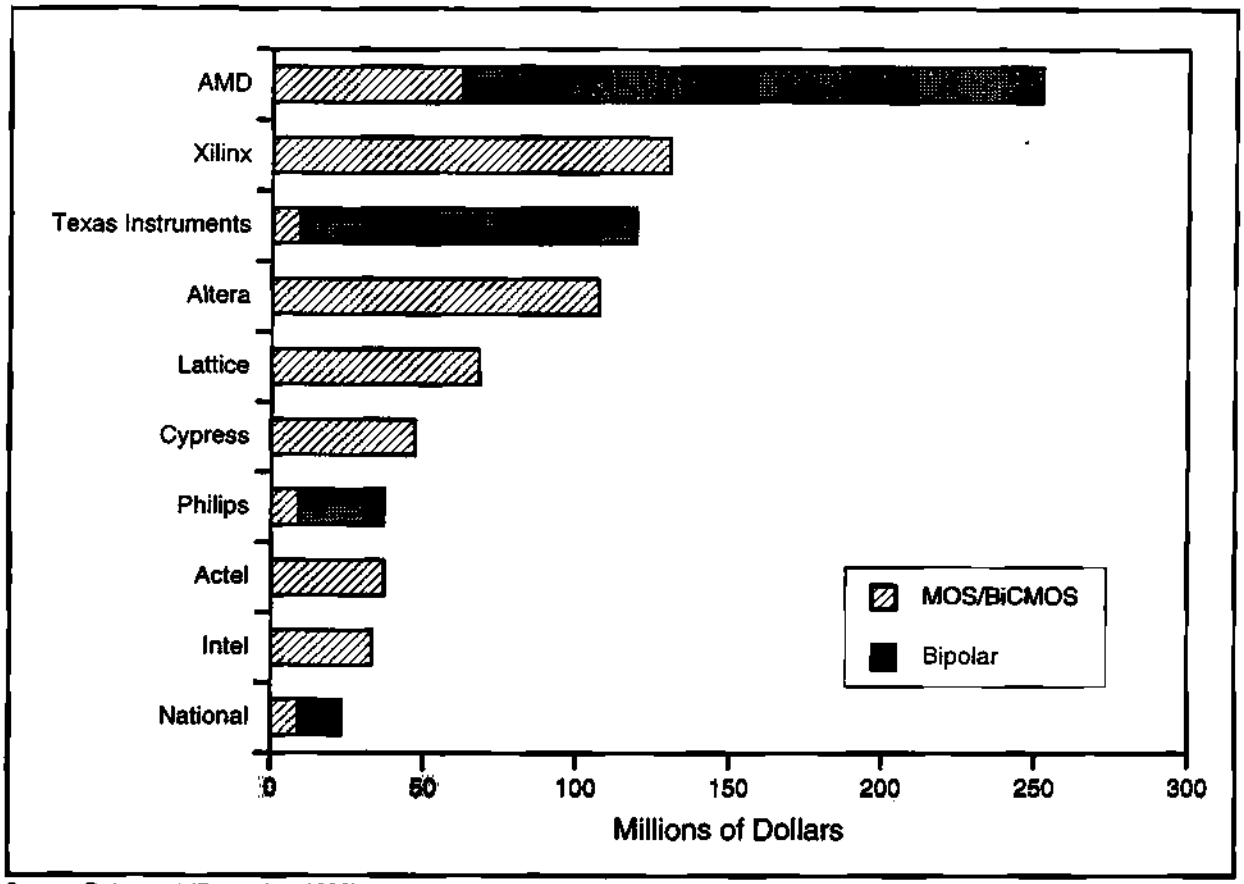
Figure 6-5
Top 10 1991 Worldwide MOS/BiCMOS CBIC Suppliers



Source: Dataquest (December 1992) G2001457

The top 10 1991 worldwide CBIC suppliers gained a small amount of market share, compared with the top 10 1990 suppliers: 67.8 percent of the total market in 1991 versus 67.5 percent in 1990.

Figure 6-6
Top 10 1991 Worldwide PLD Suppliers



Source: Dataquest (December 1992) G2001458

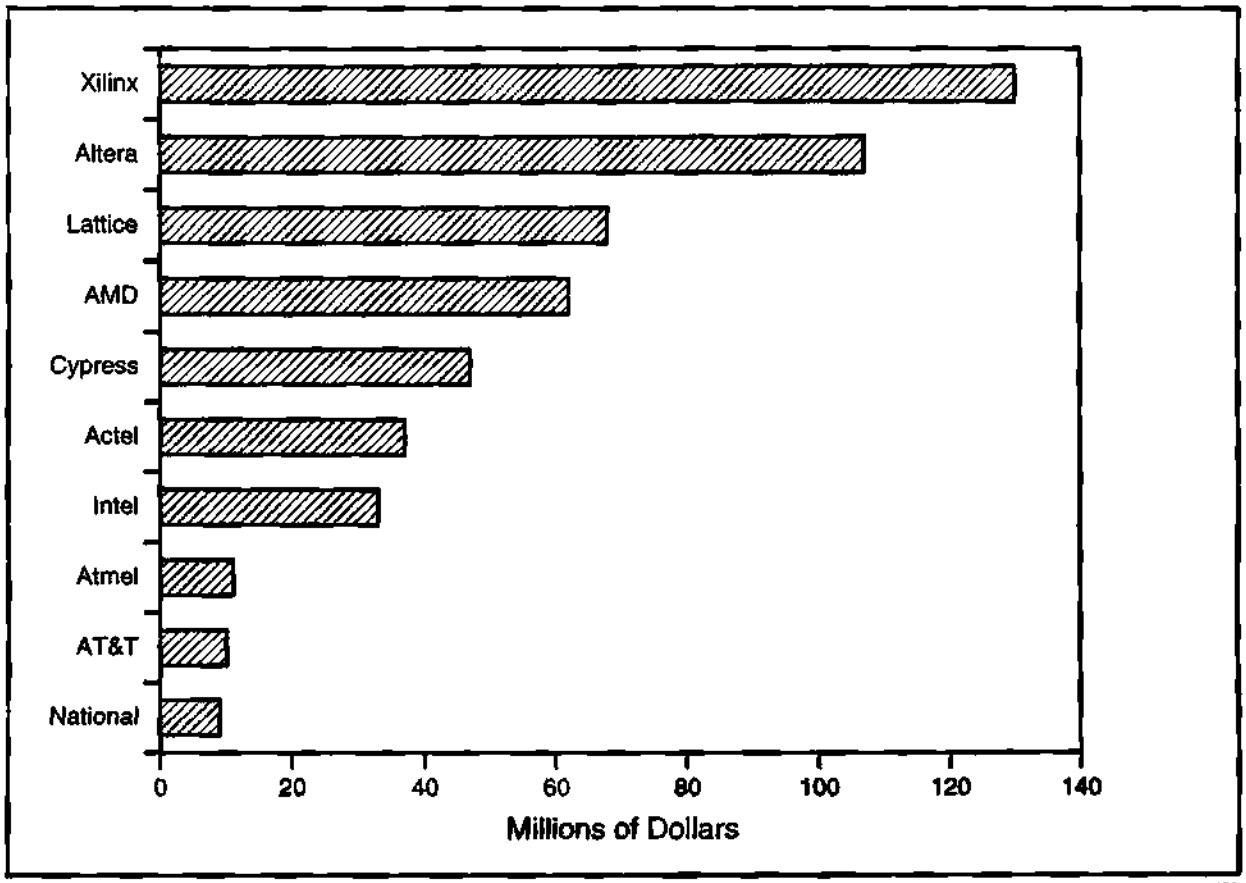
PLD Supplier Trends

The top 10 suppliers in the 1991 PLD market were all North American suppliers (see Figure 6-6). Japanese companies are just entering this market; their success in penetrating this market remains to be seen. Although AMD is the top 1991 PLD supplier, Xilinx is the largest 1991 MOS PLD supplier (see Figure 6-7). AMD, Texas Instruments, Philips, and National all derived a substantial portion of their revenue from bipolar PLDs, which is a declining market.

The top 10 1991 worldwide PLD suppliers lost market share, compared with the top 10 1990 suppliers: 94.6 percent of the total market in 1991 versus 96.4 percent in 1990.

For further information regarding market share rankings, please see the *Worldwide ASIC Market Share* document.

Figure 6-7
Top 10 1991 Worldwide MOS/BiCMOS PLD Suppliers



Source: Dataquest (December 1992)
G2001459

Dataquest Perspective

Shifts in market share can be predicted by examining the strengths and weaknesses of the different types of ASIC suppliers. It will be increasingly difficult for many suppliers to compete given today's industry structure.

ASIC suppliers can be grouped into the following four basic categories:

- Vertically integrated system suppliers that supply ASICs
- Broad-based semiconductor suppliers that supply ASICs
- Focused ASIC suppliers with fabs
- Focused ASIC supplier without fabs

As mentioned earlier, 5 of the top 10 1991 ASIC suppliers are vertically integrated system suppliers that sell ASICs, 3 are broad-based semiconductor suppliers that supply ASICs, and 2 are focused ASIC suppliers with fabs.

Vertically integrated system suppliers use ASIC technology as a competitive weapon for internal system design. This type of ASIC supplier wields a powerful advantage over all other ASIC suppliers in the merchant ASIC market for two reasons. First, these suppliers typically boast the most efficient manufacturing, which stems from economies to scale of high-volume manufacturing. In short, they have both large internal and merchant consumption, which enables greater amortization of development costs. Furthermore, they are often broad-based semiconductor suppliers, which provides an added advantage of amortizing their manufacturing costs across standard products as well as ASICs. This clearly gives them a highly competitive cost structure. Second, they have a large amount of in-house system expertise available to develop advanced ASIC cell libraries. In our view, these suppliers are well positioned to capitalize on the merchant ASIC market.

Broad-based semiconductor suppliers, however, develop ASICs to defend their semiconductor business. They have a cost structure that is somewhat less imposing because manufacturing costs can be amortized across both standard products (for example, DRAMS) as well as ASICs. However, they do not have the internal consumption necessary to reduce their merchant manufacturing cost structure. Therefore, their cost structure is less favorable than vertically integrated suppliers, but more favorable than the focused ASIC suppliers with fabs.

Broad-based semiconductor suppliers have another obstacle to hurdle—limited system expertise. Typically, they are forced to rely on partnerships with customers to acquire the system expertise. The challenge for these suppliers is finding the right partners to aid in development of specialized macrocell libraries dedicated to specific application markets.

Focused ASIC companies with fabs find themselves in the most difficult position. They must find ways to maintain fab capacity to achieve a profitable cost structure as well as invest in the following areas:

- Development of next-generation manufacturing processes
- Development of next-generation products
- Development of dedicated macrocell libraries
- Development of a competitive EDA environment

In our view, partnerships are extremely critical for focused ASIC suppliers that have fabs. They typically do not have the R&D budgets required to develop all the areas of concern, such as the next-generation processes. Even more problematic, the cost of a state-of-the-art fab continues to rise, and at an increasing rate. A complete 0.8-micron diffusion ASIC fab costs about $200 million, requiring very high volume production to support it. One way that some manufacturers will be able to avoid the high-diffusion fab cost is by purchasing preprocessed gate array base wafers and simply performing metallization to customize the base arrays. A metallization fab is significantly less expensive than a full diffusion fab. This clearly reduces

factory overhead and relieves the concern over maintaining fab capacity while achieving reduced turnaround time requirements.

Focused ASIC suppliers without fabs appear to be in a better position to maintain profitability. Today, most of these suppliers are PLD companies. They are not burdened with maintaining fab capacity or developing the next-generation manufacturing processes. They can use the majority of their R&D budgets for developing next-generation devices. However, alliances are also critical for these companies. They must rely on partnering for fab capacity as well as for the system expertise. Choosing the right partners is crucial in meeting today's increasingly demanding time-to-market pressure.

In our view, ASIC suppliers should evaluate their manufacturing costs in light of today's environment and quickly establish the alliances required to compete in the 1990s. System knowledge and dedicated unique macrocell libraries are of great trading value when forming these alliances. The ASIC market will reward those suppliers that offer low-cost manufacturing coupled with high-value intellectual property.

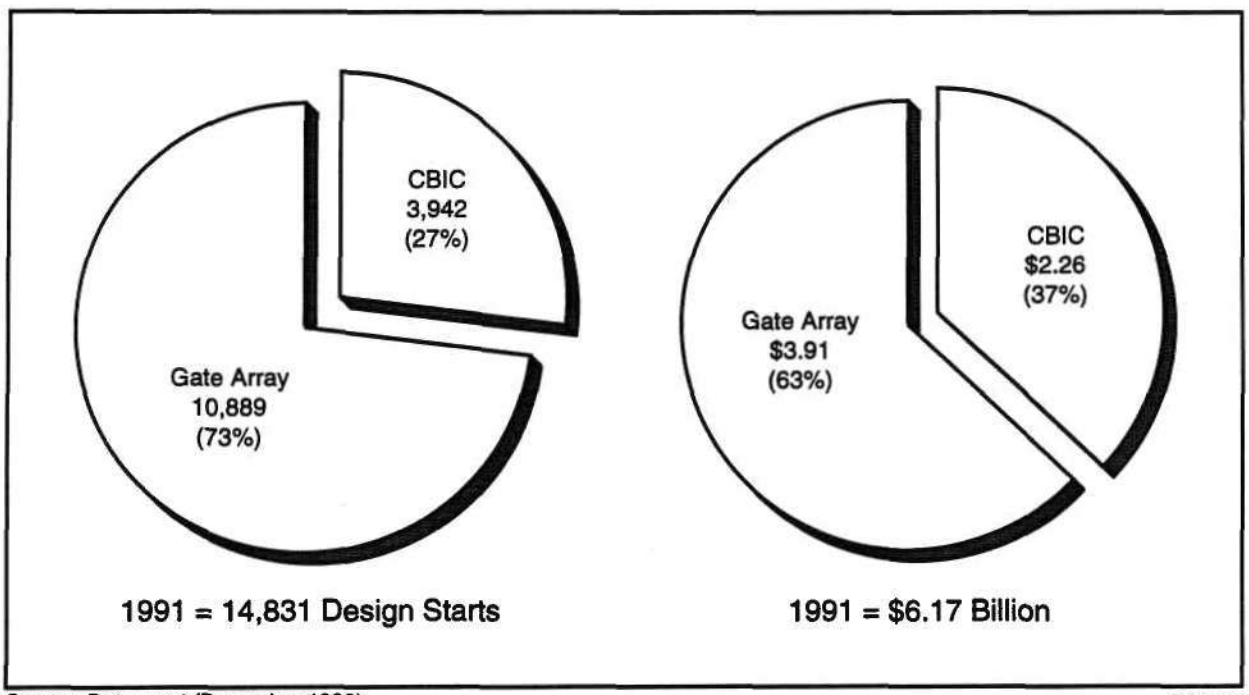
Chapter 7
Gate Array and CBIC Product Trends

Since their inception in the late 1960s, CBICs have been in a design war with gate arrays, which entered the electronic system design market a few years prior to CBICs and quickly established dominance. To attack the well-entrenched gate array product, CBIC product designers continue to search for new weapons in the form of unique cell libraries. The battle plan for gate array product designers includes a new weapon, previously identified, the embedded gate array.

What product is winning the war?

Figure 7-1 shows the percentage of 1991 worldwide design starts and dollars captured by gate arrays and CBICs. CBICs have higher unit volumes per design than do gate arrays, but fewer designs were implemented with CBIC technology. Indeed, by capturing 27 percent

Figure 7-1
Preliminary Estimates of 1991 Worldwide Gate Array and CBIC Design Starts and Dollar Consumption



Source: Dataquest (December 1992)

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of the designs, CBICs managed to capture a higher percentage of ASIC revenue. However, gate arrays are winning the war in both design starts and revenue.

In this chapter, Dataquest delves into design starts by gate count (current and future projections), design starts by function (for example, the percentage of designs that had on-chip SRAM, microprocessors, microperipherals, and scan test), and design starts by line width.

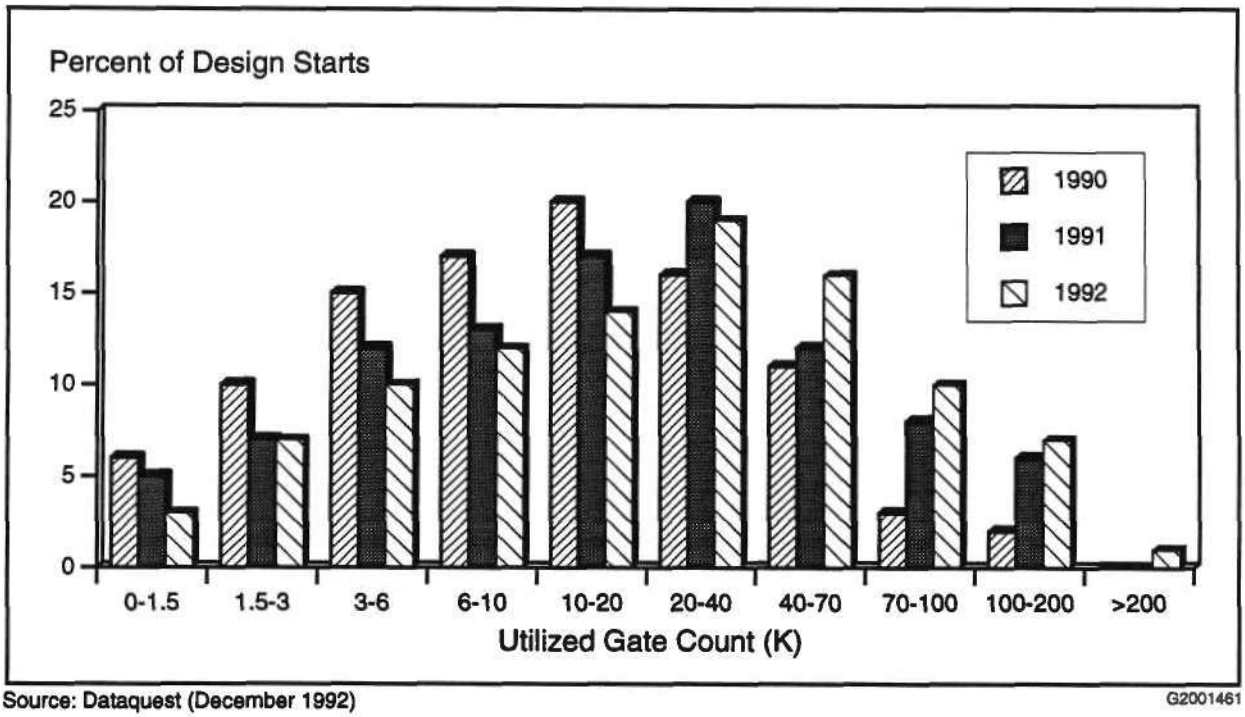
It should be noted while examining the following product trends that about 4,000 MOS gate array designs and about 2,000 CBIC designs will be captured in North America during 1992.

Design Starts, by Gate Count

Current Gate Counts

As gate array design starts continue to rise in complexity every year, the distribution of products by gate count remains in a bell-shaped curve (see Figure 7-2). CBICs also retain the same curve as gate arrays as gate counts rise (see Figure 7-3). Figure 7-4 contrasts the 1992 MOS North American gate array and CBIC design starts by gate count.

Figure 7-2
Estimated North American MOS Gate Array Design Starts, by Gate Count



Source: Dataquest (December 1992)

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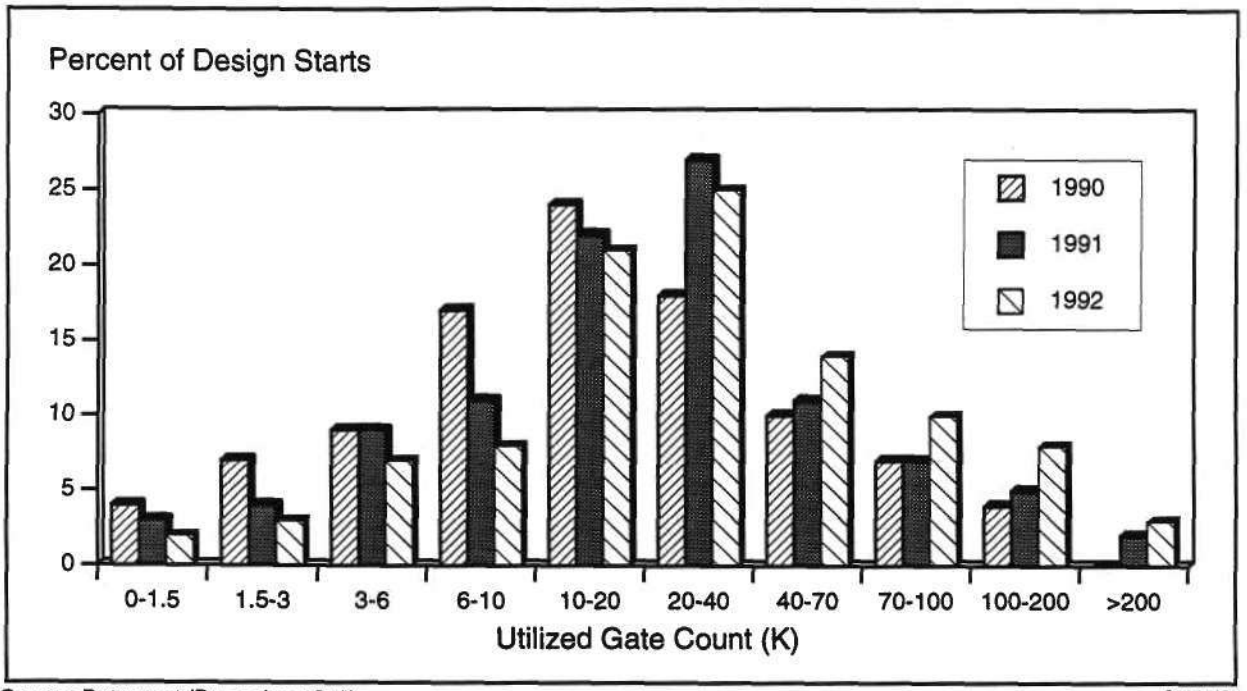
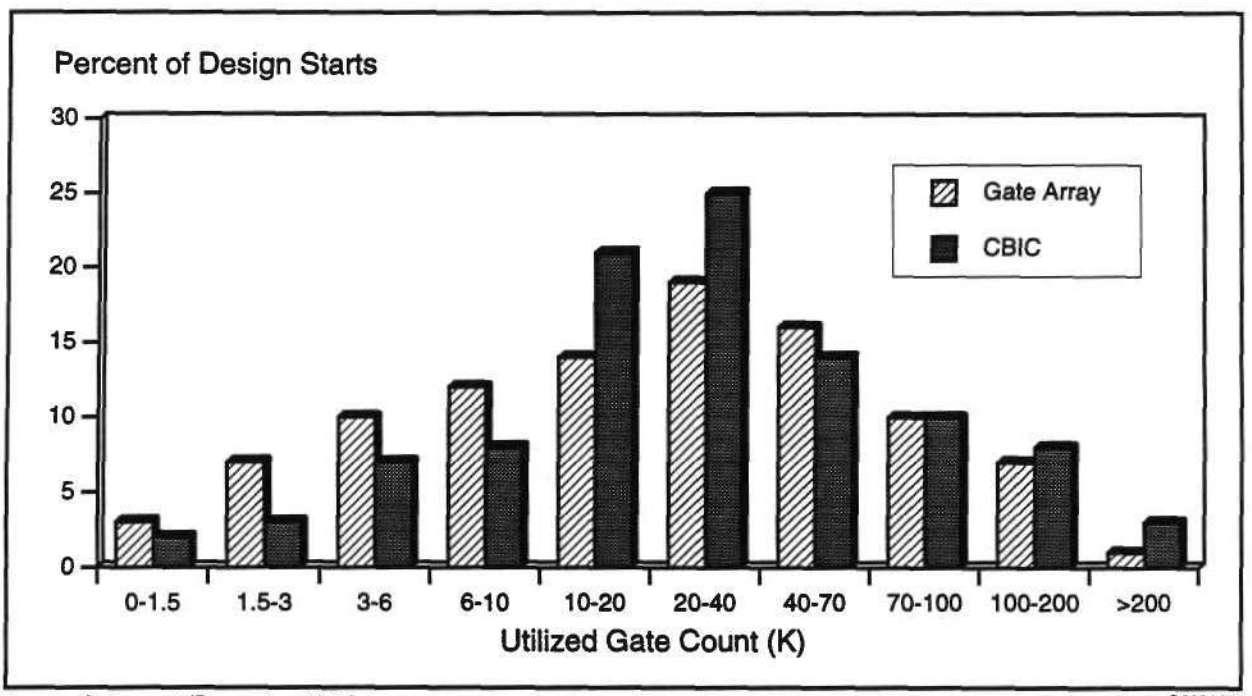
Figure 7-3
Estimated North American MOS CBIC Design Starts, by Gate Count



Source: Dataquest (December 1992) G2001462

Figure 7-4
Estimated 1992 North American MOS ASIC Design Starts, by Gate Count



Source: Dataquest (December 1992) G2001463

Dataquest's analysis of these figures reveals the following important points:

- The most cost-effective gate count in 1992 for both gate arrays and CBICs was in the 20,000- to 40,000-gate range.
- Gate arrays have traditionally been the low-cost vehicle for consolidating random logic and PLDs, thus they dominated CBICs below 10,000 gates.
- CBICs traditionally have been used in applications requiring large functional blocks such as a 128K SRAM or microprocessors/microperipherals; hence, CBICs captured a high percentage of designs above 100,000 gates.
- Today's high-end ASIC market (greater than 100,000 gates) is much smaller than most suppliers would like to believe.
- Gate arrays are narrowing the gap on CBICs in the ability to capture high-density designs because of the increasing efficiency of embedded gate arrays.

Future Gate Count Trends

Looking forward, Dataquest believes that there will be an increasing trend toward design reusability, which will push gate counts significantly higher than they have been in the past. ASIC designers will describe logic functions in VHDL or Verilog HDL, and the HDL functions then will be archived. Designers will retrieve these functions and reuse them on subsequent designs. We believe that functions will include both LSI and VLSI functions.

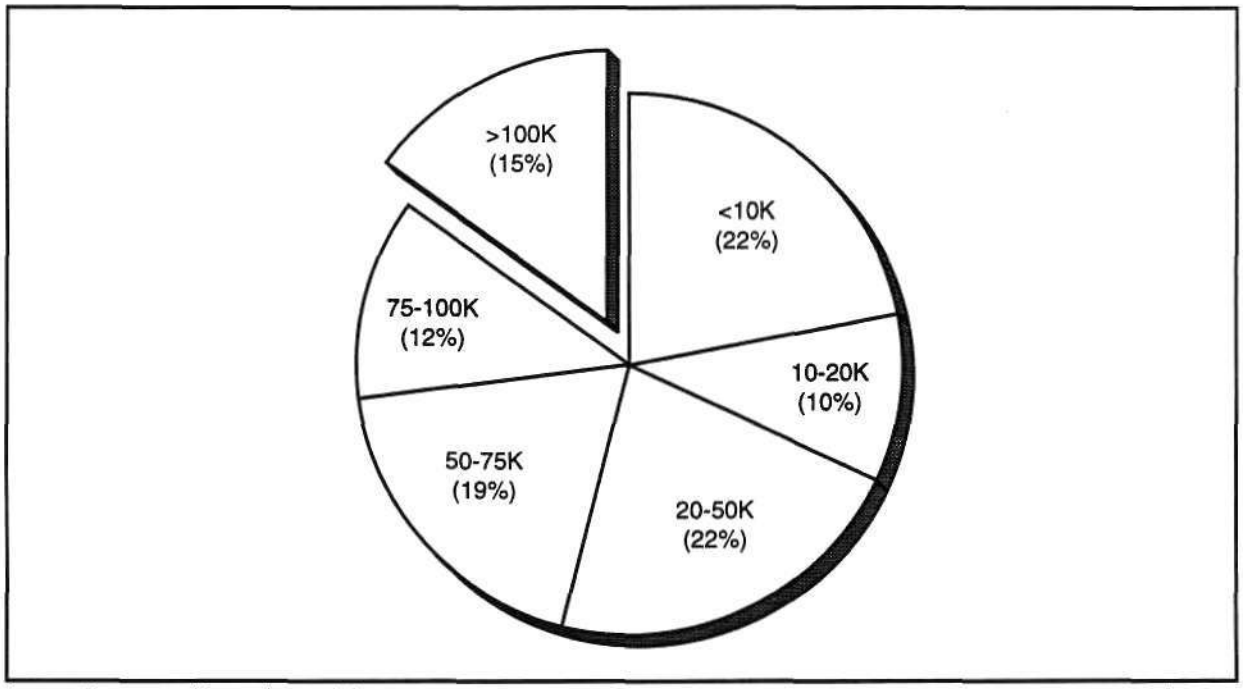
Dataquest also believes that large SRAMs (128Kb and 256Kb) will be diffused in the gate array base wafers and used for cache memory. Other functions such as SCSI, ALU, multiplier, multiplier-accumulator, FIFO, DMA controller, cache controller, and 82XX microperipherals will also be diffused in the gate array and will drive the average gate counts upward.

Figure 7-5 shows that 15 percent of the 1994 North American MOS gate array design starts will have more than 100,000 utilized gates, compared with only 8.2 percent in 1992. Furthermore, Dataquest projects that 17 percent of the 1994 North American MOS CBIC design starts will have more than 100,000 gates (see Figure 7-6).

Although average MOS gate array design starts were only 21,000 in 1991 and 28,000 in 1992, Dataquest projects the average gate count in the year 2000 to be 100,000 utilized gates (see Figure 7-7).

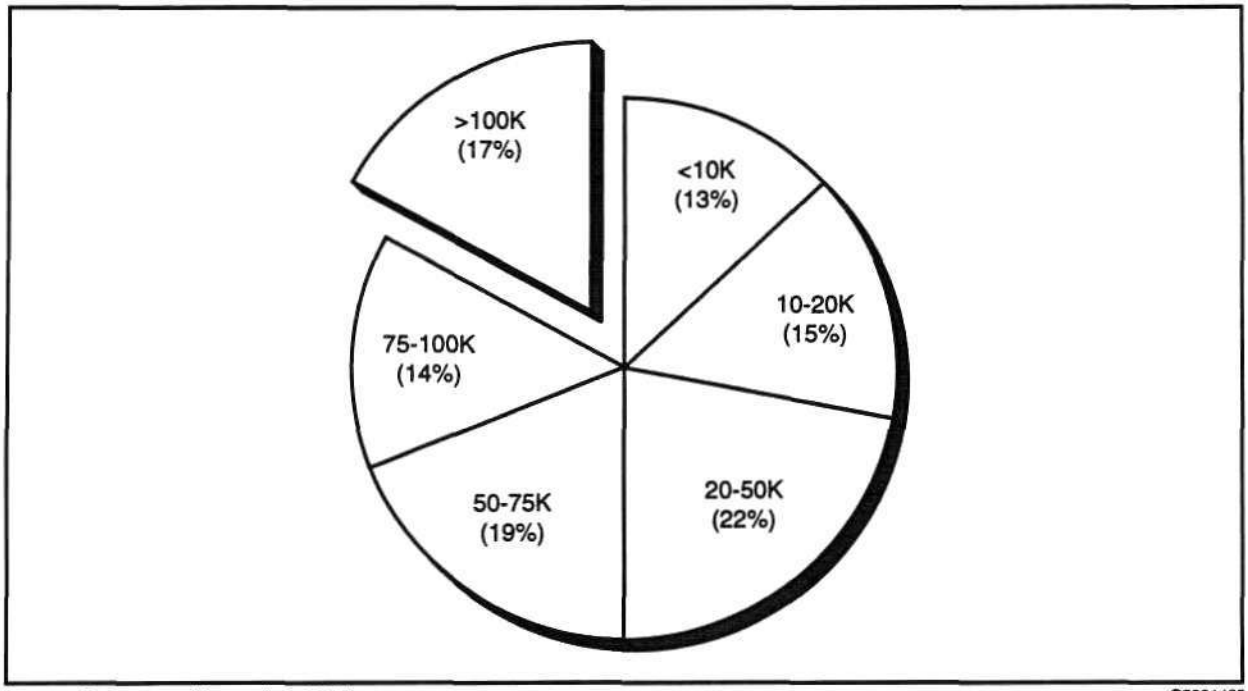
Dataquest expects multichip modules (MCMs) to temporarily stall average gate counts in the 1995 time frame. In Dataquest's view, MCMs will be moving quickly down the price learning curve by 1995, and thus are expected to become attractive for a wide range of applications. For many applications, it will be more cost-effective, for example, to put four 50,000-gate chips in an MCM, compared to one 200,000-gate chip, without losing much system performance.

Figure 7-5
Estimated 1994 North American MOS Gate Array Design Starts, by Utilized Gate Count



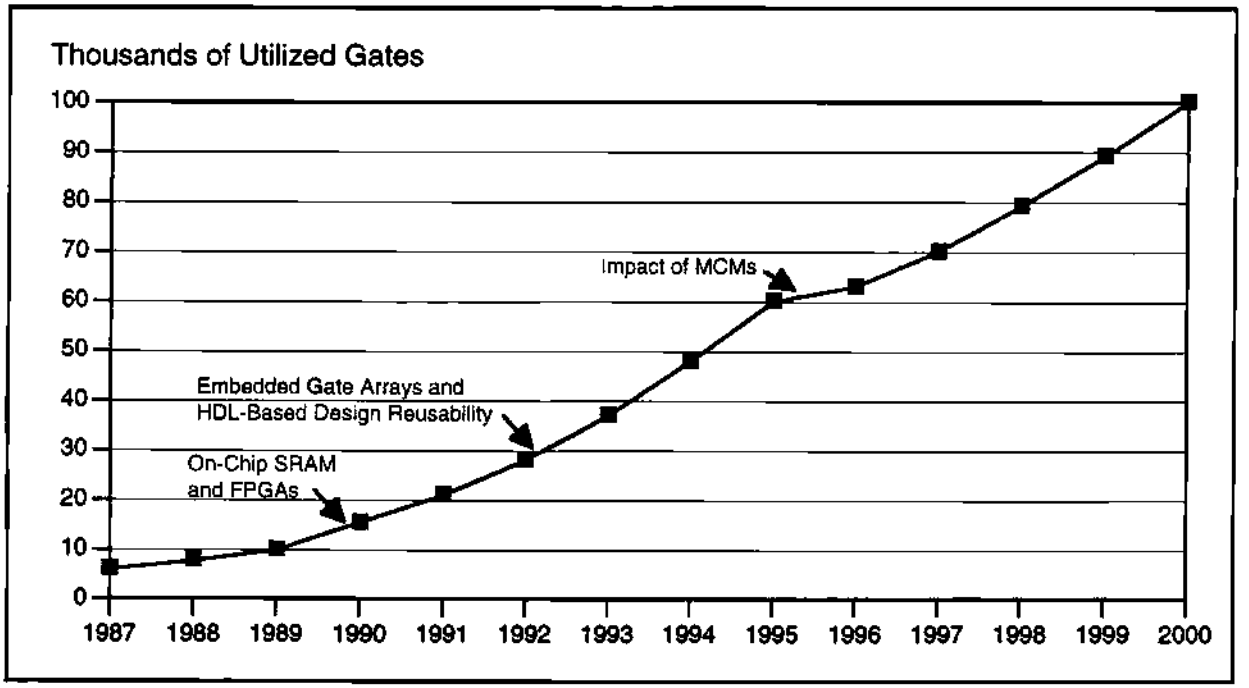
Source: Dataquest (December 1992) G2001464

Figure 7-6
Estimated 1994 North American MOS CBIC Design Starts, by Utilized Gate Count



Source: Dataquest (December 1992) G2001465

Figure 7-7
Estimated North American Average MOS Gate Array Design Starts, by Utilized Gate Count



Source: Dataquest (December 1992) G2001466

MCMs also offer a solution to the problem of high-gate-count ASICs having a limited number on bonding pads. With an MCM, a high-gate-count ASIC can be divided into multiple ASICs to more closely match individual device gate counts to I/O requirements. We expect the I/O problem to intensify over the next five years. Our belief stems from the fact that fabrication process technology developments (that is, feature size reductions) are drastically outpacing corresponding reductions in pad pitch.

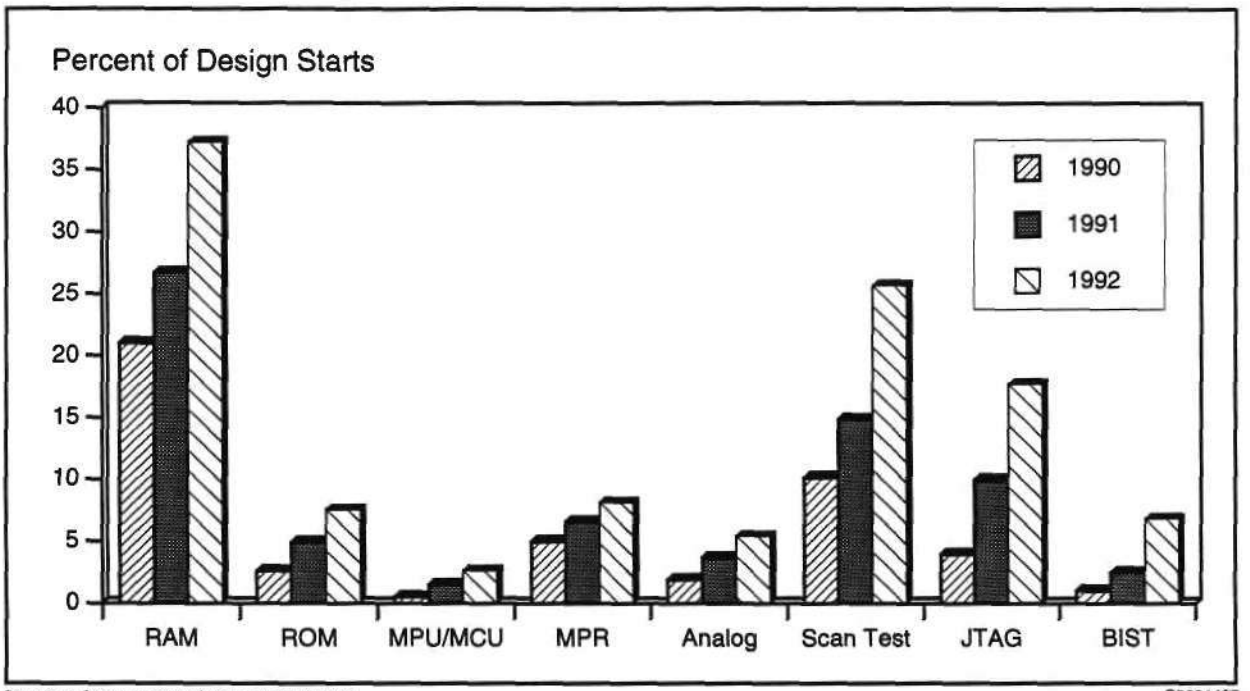
Design Starts, by Function

One primary reason for the big jump in 1992 gate array gate counts is the increasing use of on-chip SRAM and on-chip scan test (see Figure 7-8). As for CBIC design starts, we are not seeing the dramatic shifts in on-chip functionality (see Figure 7-9). Figure 7-10 contrasts the 1992 MOS North American gate array and CBIC design starts, by function.

Figures 7-11, 7-12, and 7-13 show the percentage of North American MOS gate array designs, MOS CBIC designs, and the contracted 1992 MOS gate array and MOS CBIC design starts that incorporated memory, by size of memory.

The remainder of this section contains Dataquest's analysis from these figures.

Figure 7-8
Estimated North American MOS Gate Array Design Starts, by Function



Source: Dataquest (December 1992)

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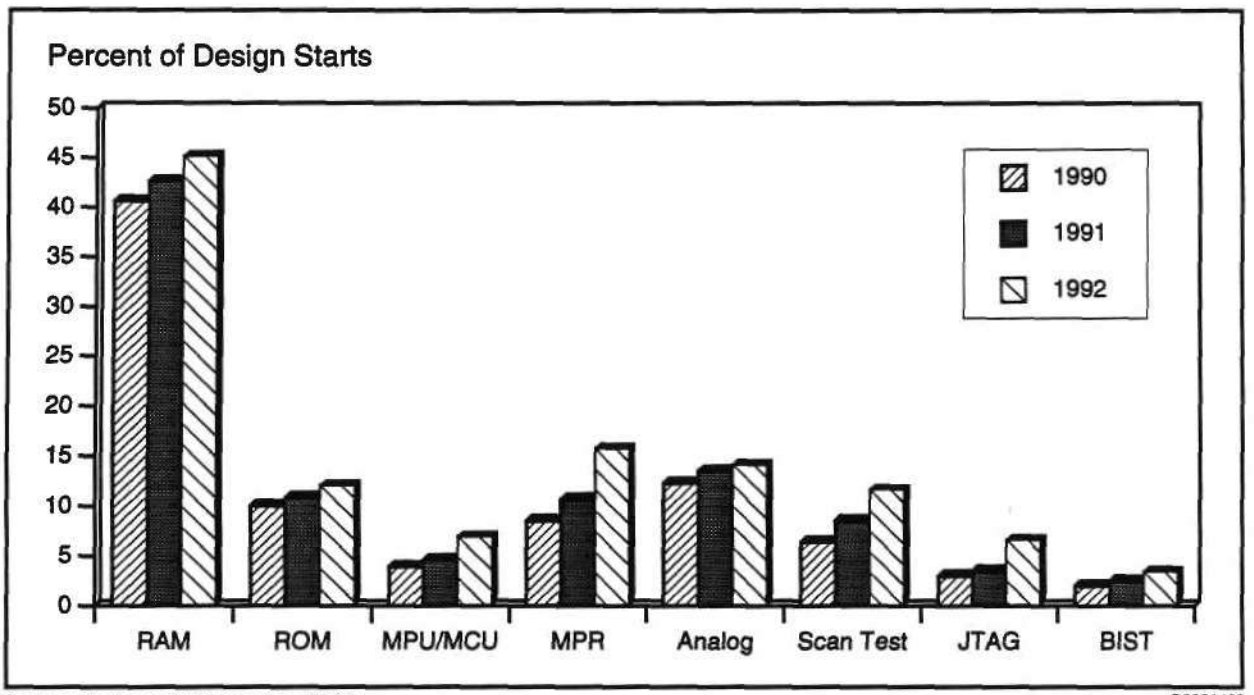
Figure 7-9
Estimated North American MOS CBIC Design Starts, by Function



Source: Dataquest (December 1992)

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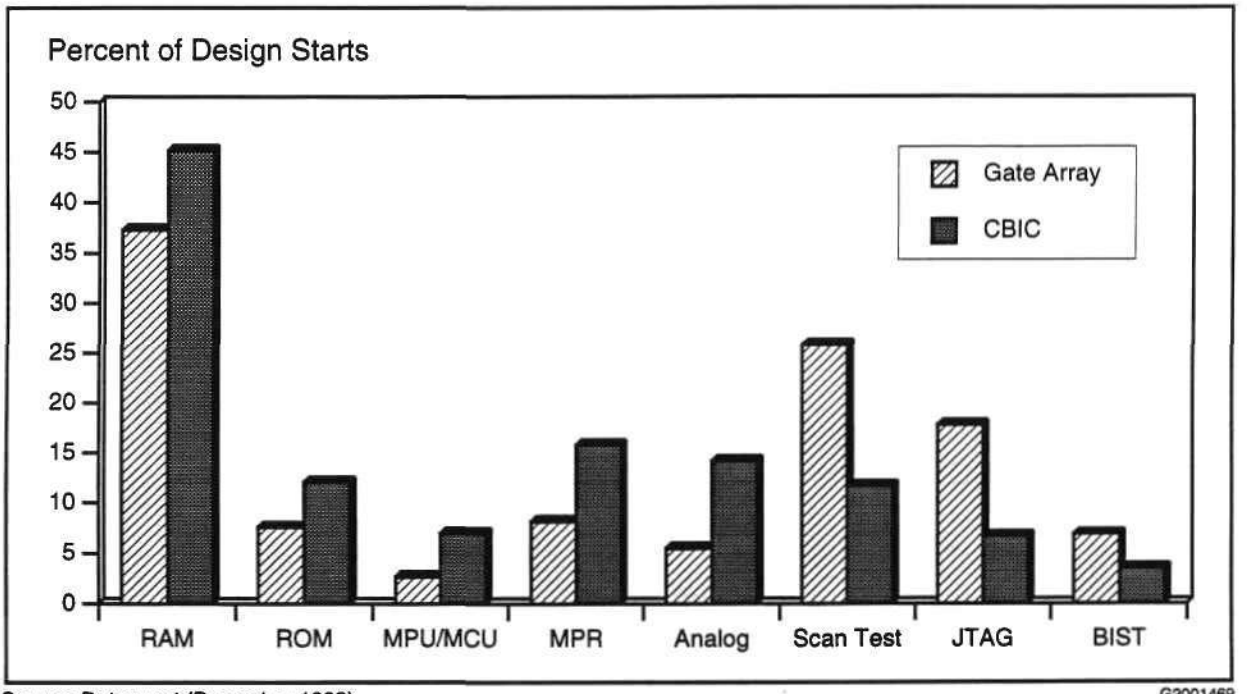
Figure 7-10
Estimated 1992 North American MOS ASIC Design Starts, by Function



Source: Dataquest (December 1992)

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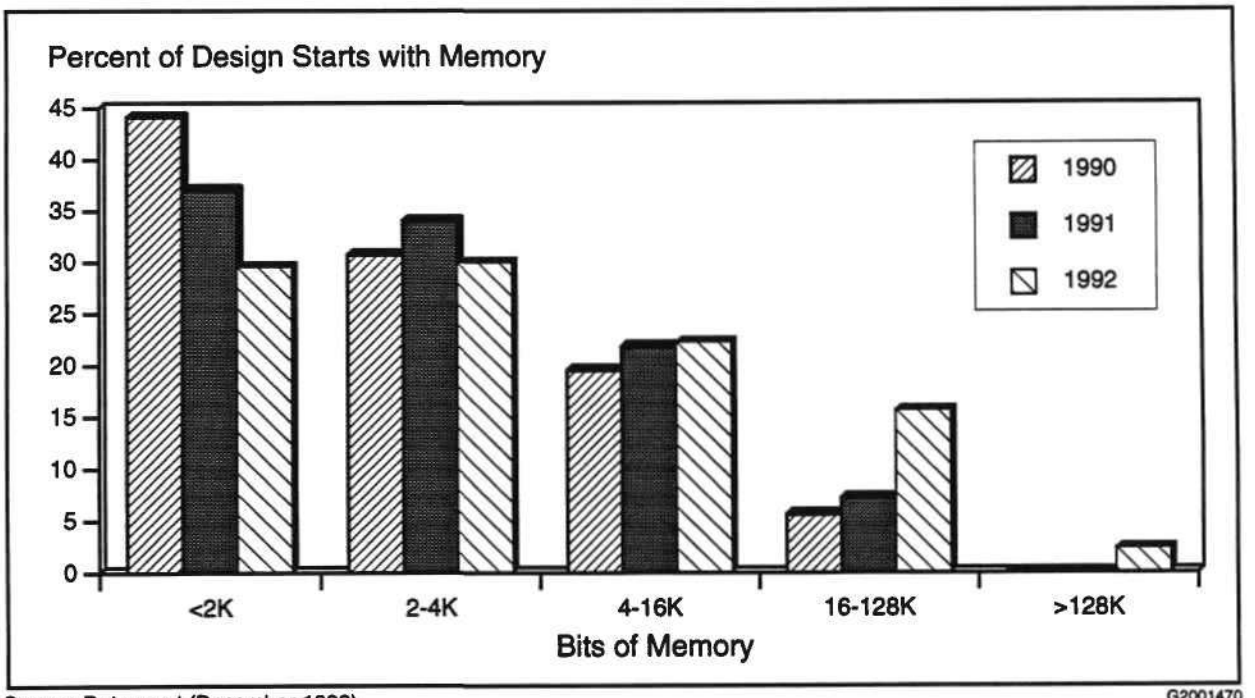
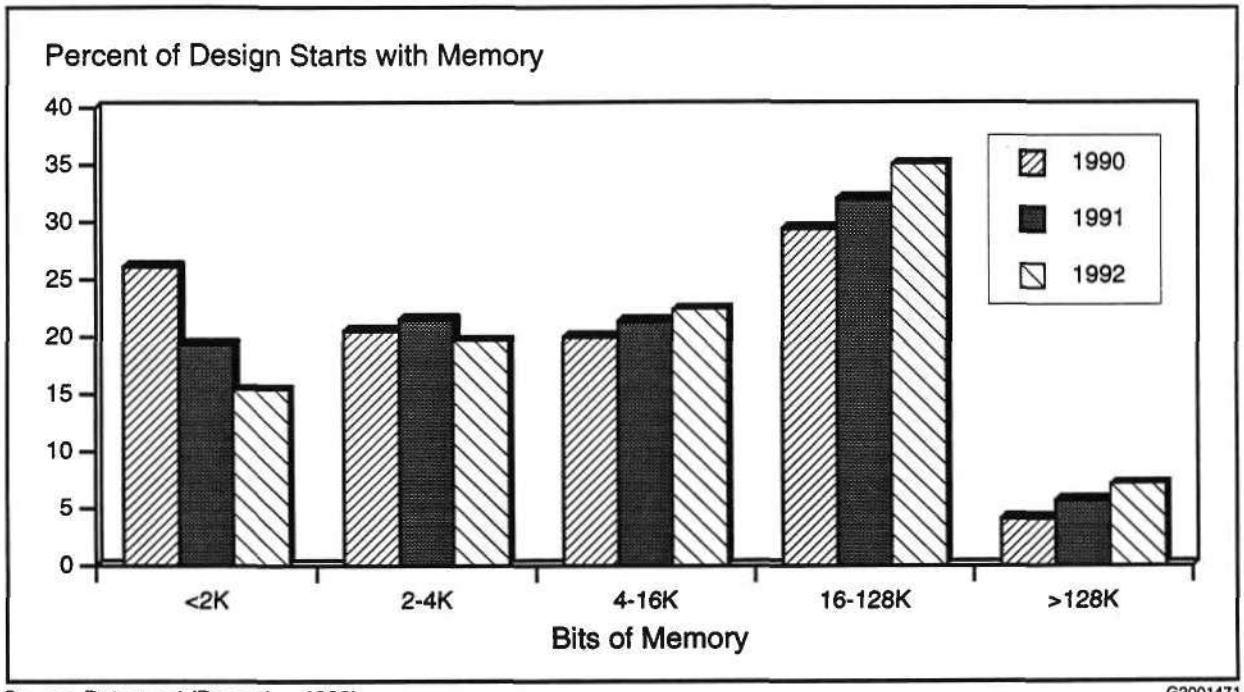
Figure 7-11
Estimated North American MOS Gate Array Design Starts, by Size of Memory



Source: Dataquest (December 1992)

G2001470

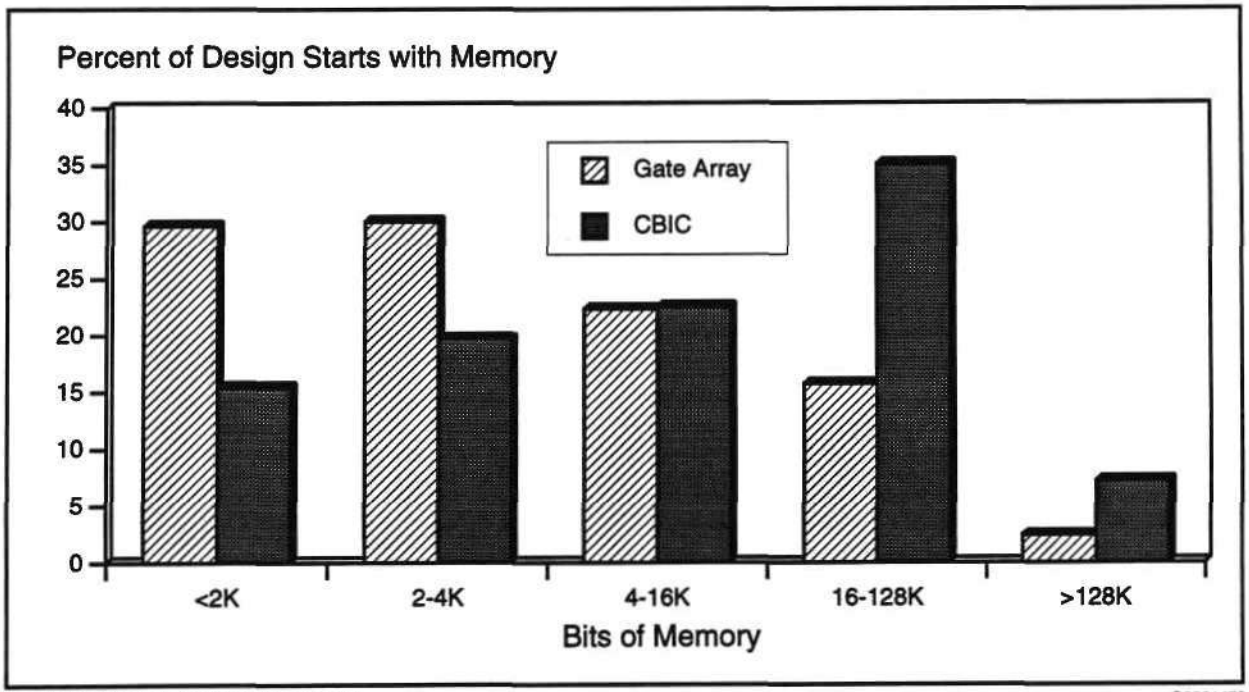
Figure 7-12
Estimated North American MOS CBIC Design Starts, by Size of Memory



Source: Dataquest (December 1992)

G2001471

Figure 7-13
Estimated North American MOS ASIC Design Starts, by Size of Memory



Source: Dataquest (December 1992)

G2001472

Although SRAM is the most popular on-chip function in both gate arrays and CBICs, the rate of change in the percentage of designs that had on-chip SRAM is much higher for gate arrays than for CBICs. Gate arrays went from 26.7 percent of the 1991 designs having on-chip SRAM to 37.3 percent in 1992, while CBIC design starts grew from 42.6 percent in 1991 to only 45.2 percent in 1992. SRAMs implemented with CBICs have traditionally been five to seven times more silicon-efficient than metal-configured SRAMs in gate arrays. The dramatic increase of on-chip gate array SRAM is because of suppliers offering much higher raw gate counts than before (more gates to utilize for metal-configured SRAMs) as well as the availability of embedded gate arrays that have large SRAM blocks. Gate arrays with diffused SRAMs blocks are just as silicon-efficient as implementing SRAMs in CBICs and are now emerging in applications that are SRAM-intensive.

Because CBICs have traditionally been more silicon-efficient for implementing SRAM, not only were there more 1992 CBIC designs with on-chip SRAM, CBIC designs also had larger memories. However, the size of gate array memories is increasing faster than that of CBIC because of the efficiency of embedded gate arrays.

ROM is more cost-effective in a CBIC than in a traditional gate array; therefore, 12.1 percent of the 1992 CBIC designs had on-chip ROM, compared to only 4.9 percent of gate array designs.

Despite the myriad of announcements of on-chip microprocessor units/microcontroller units (MPUs/MCUs), less than 2 percent of the gate array designs and less than 7 percent of the CBIC designs had on-chip MPUs/MCUs in 1992. As the numbers indicate, there has been slow user acceptance of on-chip ASIC microprocessors because of their high design cost, high device cost, and difficult testing issues.

Most on-chip microperipherals in gate array and CBICs during 1992 were 82xx peripherals.

Analog functions are difficult to implement with transistors within gate arrays. Therefore, in 1992, about 90 percent of the gate array designs that had analog functions were pure analog arrays (no digital); only 10 percent were mixed analog/digital arrays. On the other hand, CBICs are well-suited to optimize the analog functions and mix them with digital functions. Therefore, about 90 percent of CBIC designs were mixed analog/digital designs and only 10 percent were pure analog CBICs. Common analog functions being implemented in ASICs include comparators, amplifiers, voltage regulators, interface drivers, data converters, and phase-locked loops.

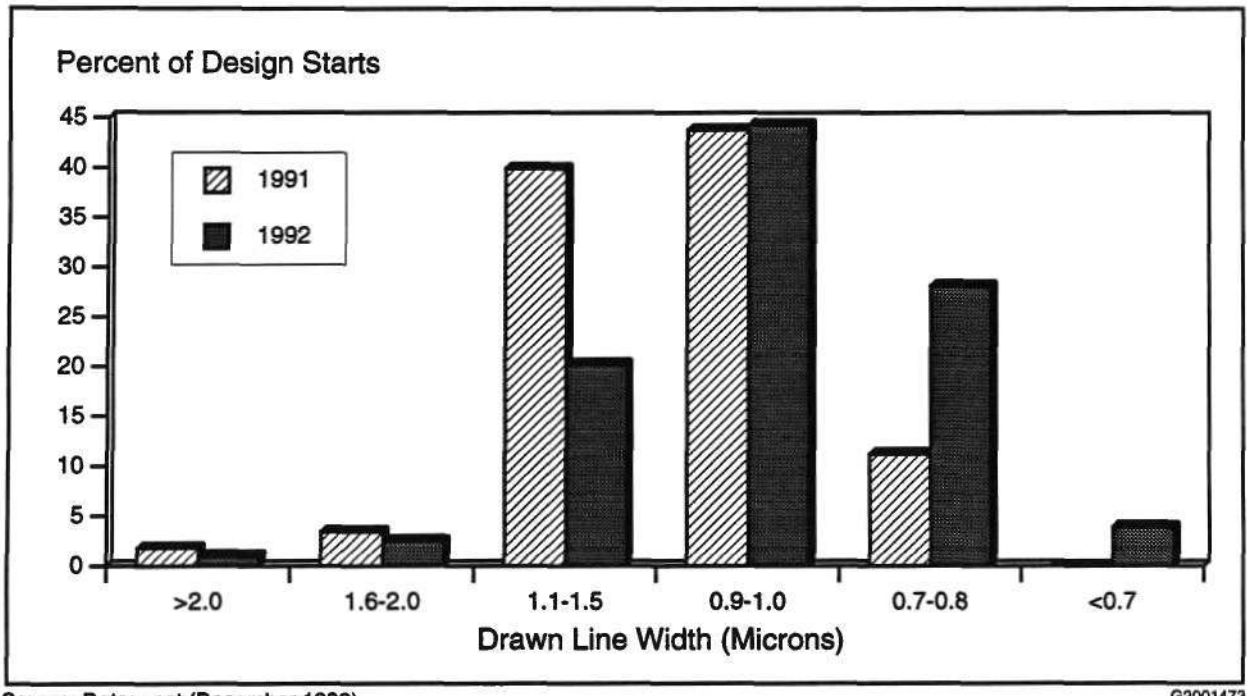
As gate densities continue to rise at a rapid rate, on-chip test has become critical for both gate arrays and CBICs. JTAG compatibility is emerging as the industry standard for board-level testing. There was only a small use of BIST being designed in for memory testing.

Design Starts, by Line Width

Although all the leading MOS gate array suppliers have announced 0.7- to 0.8-micron products (drawn line width) and some have announced sub-0.7-micron products, the bulk of the 1992 North American gate array designs are still in the 0.9- to 1.0-micron range (see Figure 7-14). The vast majority of 1992 North American CBIC design starts are also in the 0.9- to 1.0-micron range (see Figure 7-15). When comparing 1992 gate array and CBIC designs by line width (see Figure 7-16), it is quite apparent that gate arrays are leading CBICs in aggressive process geometries.

Figure 7-17 shows Dataquest's technology road map and design-in window for CMOS gate array design starts over time, by drawn line width and maximum total available gates. On average, two-layer metal interconnect achieves about 40 to 45 percent gate utilization, while three-layer metal interconnect achieves about 70 to 75 percent gate utilization. Dataquest believes that gate array suppliers will be introducing 0.3- to 0.4-micron products with 1 million usable gates by mid-1995.

Figure 7-14
Estimated North American MOS Gate Array Design Starts, by Line Width



Source: Dataquest (December 1992)

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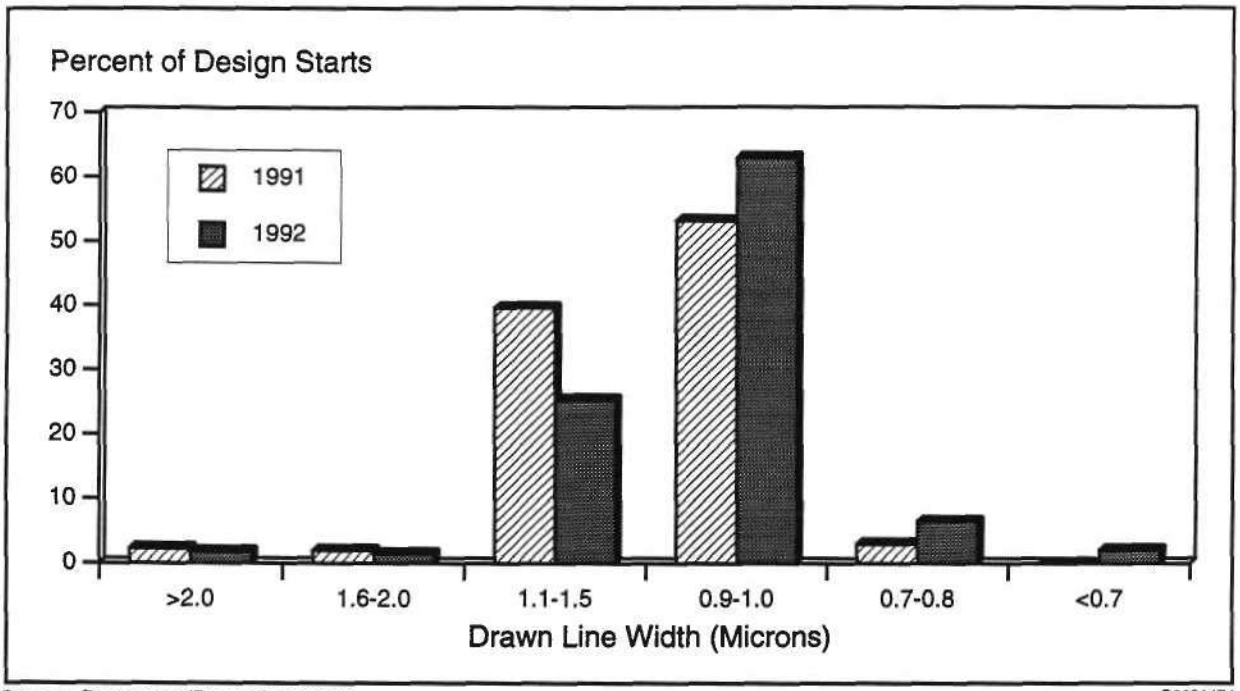
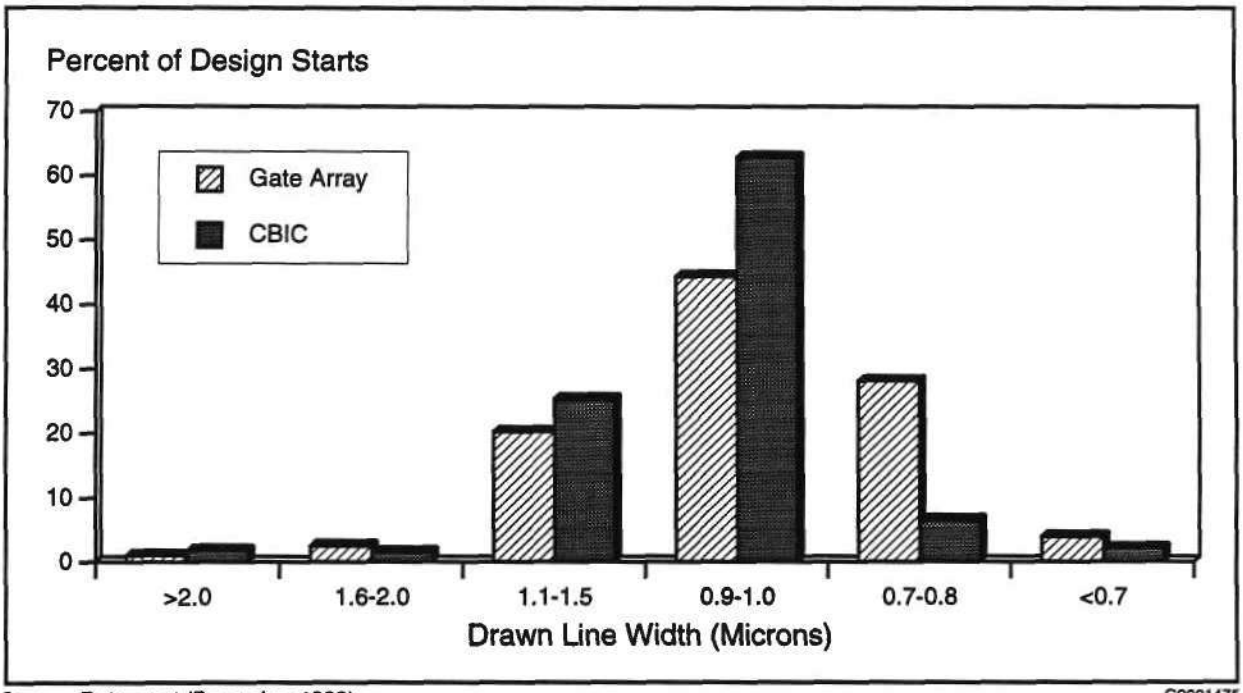
Figure 7-15
Estimated North American MOS CBIC Design Starts, by Line Width



Source: Dataquest (December 1992)

G2001474

Figure 7-16
Estimated North American MOS ASIC Design Starts, by Line Width



Source: Dataquest (December 1992)

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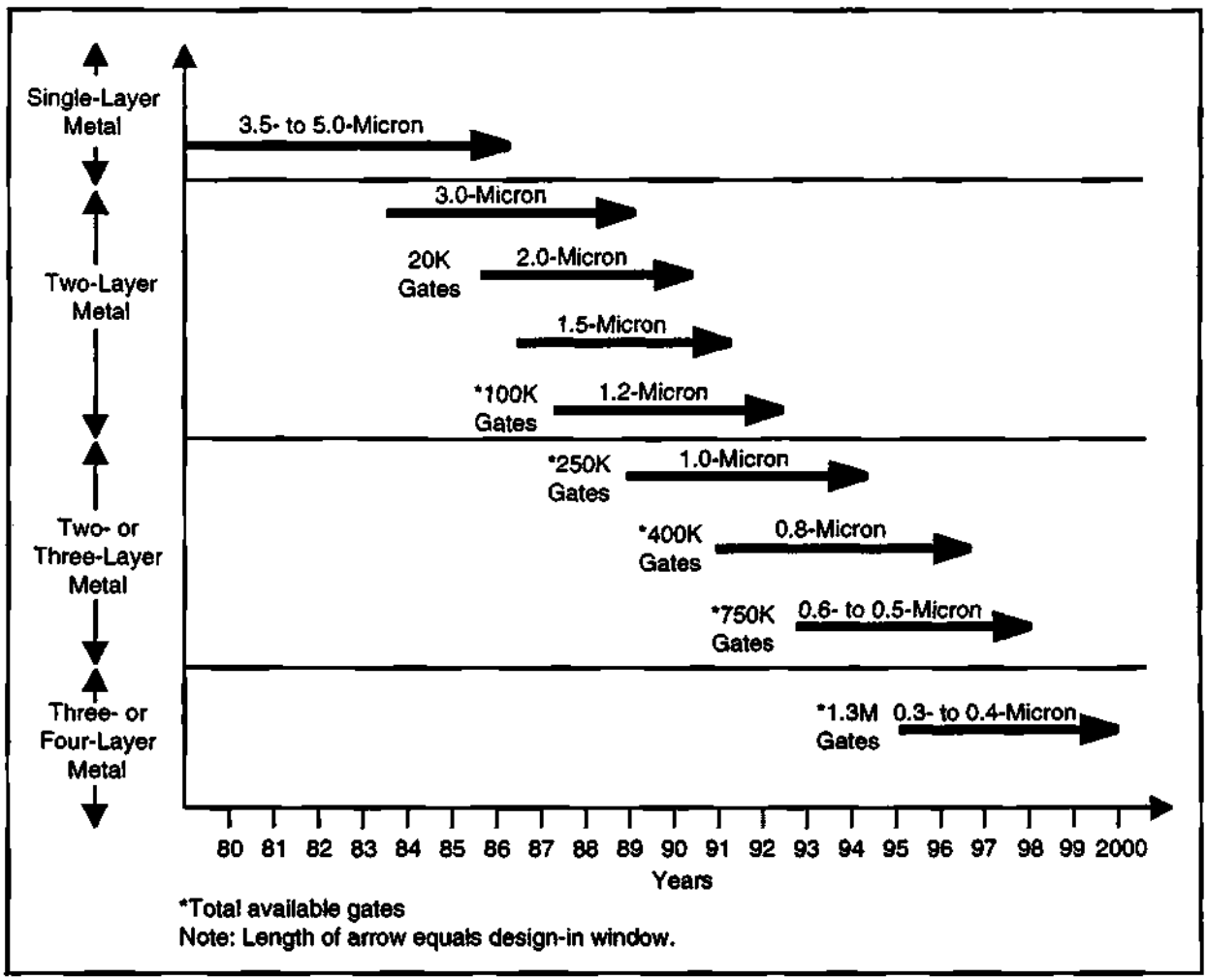
Figure 7-17
CMOS Gate Array Design Start Technology Road Map



Source: Dataquest (December 1992) G2001476

Dataquest Perspective

The dividing line between gate array applications and CBIC applications is in a state of flux. CBICs historically have been used in high-volume applications as well as in applications that need increased functionality such as large SRAM blocks. Gate arrays, when compared to CBICs, offer quicker time to market, lower risk, and lower design cost. Embedded gate arrays have now emerged as a crossbreed and are a viable option to CBICs and traditional gate arrays.

Table 7-1 summarizes the feature trade-offs associated with each type of product.

Embedded gate arrays and CBICs are the most efficient technologies for implementing memory and other large functional blocks. Embedded gate arrays still retain a portion of the chip area available for random logic gates, so the die size and device cost will not be quite as

Table 7-1
ASIC Feature Trade-Off Matrix

Feature	Traditional Gate Array	Embedded Gate Array	CBIC
Memory Efficiency	Low	High	High
Die Size	Large	Medium	Small
Device Cost	Highest	Low	Lowest
NRE Cost	Low	High	High
Retooling Cost	Low	Low	High
Retooling Time	Short	Short	Long
Performance	Medium	Medium-High	High
Risk	Lowest	Low	Highest

Source: Dataquest (December 1992)

good as with CBICs but will be far better than with traditional gate arrays. Although the first embedded gate array design cost or NRE charge is the same as for CBIC, the big savings occur when the design is retooled. Most high-density gate array designs are retooled two to three times because they do not meet system requirements. With embedded gate arrays, only the random logic will need to be reconfigured with the final layers of interconnect; therefore, the retooling turnaround time and cost are far less than for CBICs. With reduced turnaround time and cost comes embedded gate arrays' reduced risk.

Embedded gate arrays are penetrating the ASIC market and now account for 11.3 percent of the 1992 MOS North American gate array designs; the figure was 1 percent in 1990 and 3.7 percent in 1991. As noted earlier, embedded gate arrays are efficient and satisfy the strong need for on-chip SRAM. Dataquest believes that larger SRAMs (128K and 256K) will be diffused in gate array base wafers and used for cache memory. Furthermore, we believe that other functions such as SCSI, ALUs, multiplier-accumulators, FIFO memories, DMA controllers, cache controllers, and 82xx microperipherals will also be diffused in the gate array, fueling the growth of the embedded gate array market.

Because of the rapid increase in designs using three-layer metal interconnect, traditional gate arrays and embedded gate arrays are also becoming more cost-competitive with CBICs. Three-layer metal designs now make up 36 percent of the 1992 MOS North American gate array designs; the figure was 8.9 percent in 1990 and 20.5 percent in 1991. The major cost savings associated with three-layer metal versus two-layer metal in high-density designs have led to this rapid increase. Gate utilization for a sea-of-gates gate array architecture using two-layer metal is about 40 to 45 percent; it jumps to 70 to 75 percent with three-layer metal interconnect. Increased gate utilization allows the die required for a given application to be shrunk, which in turn means higher yields and a significant cost savings.

In conclusion, Dataquest believes that gate arrays (including traditional gate arrays and embedded gate arrays) will continue to remain the dominant technology throughout the decade. Furthermore, we believe that embedded gate arrays will wrestle market share from the CBIC market because they increasingly will be capable of matching the functionality and performance of CBICs, with reduced cost and risk. However, Dataquest does not believe that embedded gate arrays will replace traditional gate arrays or CBICs in the foreseeable future. Each product brings value to the market. Hence, we believe that they will coexist and system designers will select the products that best suit their unique applications.

Appendix A
Survey Questionnaire

Company _____
Date _____

Dataquest's Gate Array Supplier Questionnaire - MOS

1. What percentage of your worldwide gate array revenue was in each technology?

	1991	1992(e)
MOS	_____%	_____%
BiCMOS	_____%	_____%
Total	100%	100%

2. What percentage of your worldwide MOS gate array revenue will be Intracompany? (Sales to internal divisions)

	1991	1992(e)
Intracompany	_____%	_____%

3. What percentage of your worldwide MOS gate array revenue will be NRE?

	1991	1992(e)
NRE	_____%	_____%

4. What percentage of your 1991 and 1992 MOS gate array sales will be consumed in each region?

	1991	1992(e)
North America	_____%	_____%
Japan	_____%	_____%
Europe	_____%	_____%
Asia - Pacific	_____%	_____%
ROW	_____%	_____%
Total	100%	100%

5. What percentage of your 1991 and 1992 North American MOS gate array sales (NRE + Production) will be in each end-use market segment?

	1991	1992(e)
DP	_____%	_____%
Communications	_____%	_____%
Industrial	_____%	_____%
Military	_____%	_____%
Transportation	_____%	_____%
Consumer	_____%	_____%
Total	100%	100%

6. What percentage of your 1991 and 1992 North American MOS gate array dataprocessing sales were in each market?

	1991	1992(e)
Personal computers	_____%	_____%
Workstations	_____%	_____%
Mid-range, Mainframe, Super computers	_____%	_____%
Other _____	_____%	_____%
Total	100%	100%

7. How many MOS gate array design starts did your company capture? (includes respins, design starts are where a prototype was shipped)

North America		Worldwide	
1991	1992(e)	1991	1992(e)
_____#	_____#	_____#	_____#

8. What percentage of your 1991 and 1992 North American MOS gate array design starts are in each gate range? What do you expect for 1996? (Utilized gates including RAM, 1 Bit = 3 gates for metal RAM, 1 Bit = 1 gate for diffused RAM)

	1991	1992(e)	1996(e)
Less than 1,500	_____%	_____%	_____%
1,501 to 3,000	_____%	_____%	_____%
3,001 to 6,000	_____%	_____%	_____%
6,001 to 10,000	_____%	_____%	_____%
10,001 to 20,000	_____%	_____%	_____%
20,001 to 40,000	_____%	_____%	_____%
40,001 to 70,000	_____%	_____%	_____%
70,001 to 100,000	_____%	_____%	_____%
100,001 to 200,000	_____%	_____%	_____%
greater than 200,000	_____%	_____%	_____%
Total	100%	100%	100%

9. What percentage of your 1991 and 1992 North American MOS gate array design starts contain the following on-chip functions? (does not have to total 100%)

	1991	1992(e)
RAM	_____%	_____%
ROM	_____%	_____%
Microprocessor/Controller	_____%	_____%
Micro Peripherals	_____%	_____%
Analog	_____%	_____%
Scan Path Test	_____%	_____%
JTAG Boundary Scan Test	_____%	_____%
BIST	_____%	_____%
Other _____	_____%	_____%

10. Of your 1991 and 1992 North American MOS gate array design starts that had RAM on board, what percentage of the designs had the following number of bits?

	1991	1992(e)
Up to 2K bits?	_____%	_____%
Greater than 2K to 4K bits?	_____%	_____%
Greater than 4K to 16K bits?	_____%	_____%
Greater than 16K to 128K bits?	_____%	_____%
Greater than 128K Bits?	_____%	_____%
Total	100%	100%

11. What percentage of your 1991 and 1992 North American MOS gate array design starts have the following line widths (drawn)?

	1991	1992(e)
Greater than 2.0 micron	_____%	_____%
1.6 to 2.0 micron	_____%	_____%
1.1 to 1.5 micron	_____%	_____%
0.9 to 1.0 micron	_____%	_____%
0.7 to 0.8 micron	_____%	_____%
Less than .7 micron	_____%	_____%
Total	100%	100%

12. What percentage of your 1991 and 1992 North American MOS gate array design starts had the following features?
(Does not have to total 100%)

	1991	1992(e)
Sea of gates architecture?	_____%	_____%
Megacells such as RAM embedded in the base wafer?	_____%	_____%
Double metal interconnect?	_____%	_____%
Triple metal interconnect?	_____%	_____%
Mixed 3V/5V	_____%	_____%
3V only	_____%	_____%
Designed using top-down methodology (Top-down methodology = VHDL,HDL,etc.)	_____%	_____%

13. What percentage or actual number of your 1991 and 1992 MOS gate array design starts will be in each region?

	1991	1992(e)
North America	_____%	_____%
Japan	_____%	_____%
Europe	_____%	_____%
Asia - Pacific	_____%	_____%
ROW	_____%	_____%
Total	100%	100%

14. Of your North American MOS gate array designs in production during 1991, what percentage of your designs will have the following total unit volumes for the life of the design? What do you expect for 1992?

	1991	1992(e)
Less than 5,000	_____%	_____%
5,000 to 10,000	_____%	_____%
10,000 to 20,000	_____%	_____%
20,000 to 100,000	_____%	_____%
greater than 100,000	_____%	_____%
Total	100%	100%

15. Of your North American MOS gate array designs captured during 1991 and 1992, how long do you expect the average production life of a design to last? What do you expect for designs captured in 1993 and 1994? (Commercial only - no not include military designs)

1991	1992(e)	1993(e)	1994(e)
_____years	_____years	_____years	_____years

16. What percentage of your 1991 and 1992 North American MOS gate array designs starts are in the following package types?

	Design Starts 1991	Design Starts 1992(e)
Dual in-line (DIP)	_____%	_____%
Leadless chip carrier (LLCC)	_____%	_____%
Plastic leaded chip carrier (PLCC)	_____%	_____%
Ceramic quad flat pack (CQFP)	_____%	_____%
Metal quad flat pack (MQFP)	_____%	_____%
Plastic quad flat pack (PQFP)	_____%	_____%
Ceramic pin grid array (CPGA)	_____%	_____%
Metal pin grid array (MPGA)	_____%	_____%
Plastic pin grid array (PPGA)	_____%	_____%
Land grid arrays or Pad grid arrays	_____%	_____%
Chip on Board (COB/TAB to board)	_____%	_____%
Multi-chip module	_____%	_____%
Other _____	_____%	_____%
Total	100%	100%

17. What percentage of your 1991 and 1992 North American MOS gate array design starts were in packages in the following pin ranges?

	Design Starts 1991	Design Starts 1992(e)
Less than 44	_____%	_____%
44 to 84	_____%	_____%
85 to 132	_____%	_____%
133 to 195	_____%	_____%
196 to 244	_____%	_____%
greater than 244	_____%	_____%
Total	100%	100%

18. What are the total North America MOS gate array sales for your company during 1991 and 1992 calendar years?
(NRE + CAD software + Intracompany + Production)

1991 $_____ 1992(e) $_____

19. What are the total Worldwide MOS gate array sales for your company during 1991 and 1992 calendar years?
(NRE + CAD software + Intracompany + Production)

1991 $_____ 1992(e) $_____

Thank you for your help!!!!!!!

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• Market Statistics

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ASIC Consumption Forecast

August 10, 1992

Source: Dataquest

Market Statistics

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ASICs *Worldwide*

ASIC-SEG-MS-9202

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ASIC Consumption Forecast

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Note: All tables show estimated data.

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ASIC Consumption Forecast

Introduction

This document contains detailed information on Dataquest's view of the application-specific integrated circuit (ASIC) market. Included in this document are:

- 1992-1996 ASIC consumption forecast
- 1992-1996 gate array consumption forecast
- 1992-1996 cell-based IC (CBIC) consumption forecast
- 1992-1996 programmable logic device (PLD) consumption forecast

More detailed data on this market may be requested through Dataquest's client inquiry service. Qualitative analysis of these data is provided in the *Dataquest Perspectives* located in the binder of the same name.

Segmentation

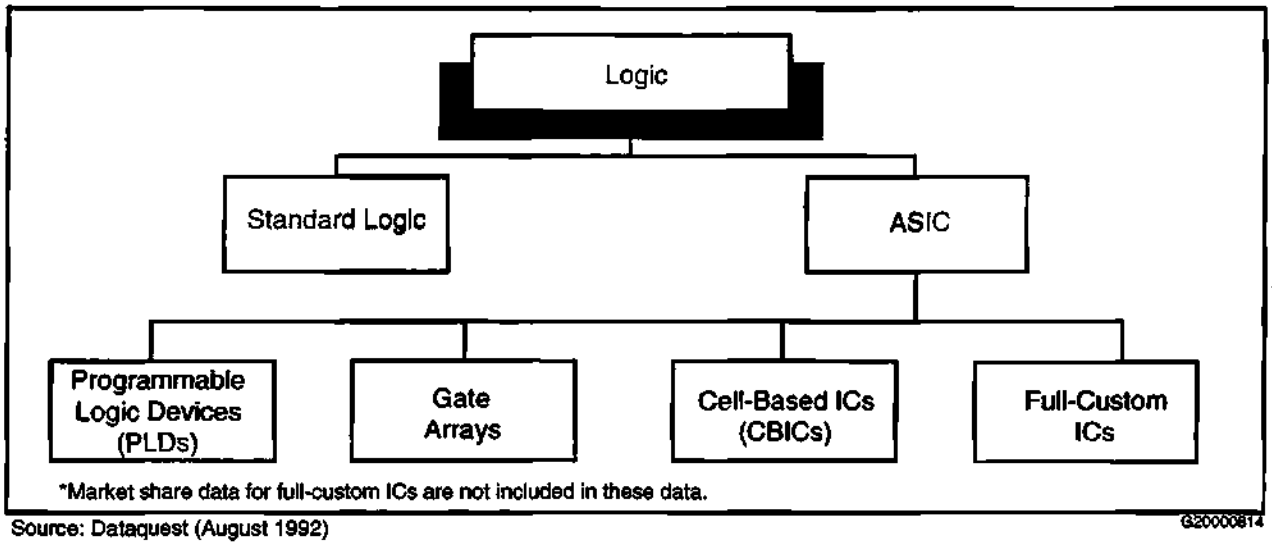
This section outlines the market segments that are specific to this document. Dataquest's objective is to provide data along lines of segmentation that are logical, appropriate to the industry in question, and immediately useful to clients.

For a detailed explanation of Dataquest's market segmentation, refer to the *Dataquest Research and Forecast Methodology* document located in the Source: Dataquest binder. For a complete listing of all market segments tracked by Dataquest, please refer to the *Dataquest High-Technology Guide: Segmentation and Glossary*.

Dataquest defines the ASIC market according to the segmentation scheme in Figure 1.

Figure 1 shows Dataquest's segmentation into the two main categories of standard logic and ASIC. The ASIC family tree breaks out ASICs as follows: PLDs, gate arrays, CBICs, and full-custom ICs. CBICs and full-custom ICs are personalized by altering the full set of masks, whereas PLDs and gate arrays are personalized by electrically programming the devices or by altering only the final layers of interconnect.

Figure 1
ASIC Family Tree



Source: Dataquest (August 1992)

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Definitions

This section lists the definitions used by Dataquest to present the data in this document. Complete definitions for all terms associated with Dataquest's segmentation of the high-technology marketplace can be found in the *Dataquest High-Technology Guide: Segmentation and Glossary.*

Product Definitions

Application-Specific Integrated Circuits (ASICs). This term is used to describe all IC products customized for a single user. ASIC products are a combination of digital, mixed-signal, and analog products. Customized ICs purchased by more than one user become standard products and are no longer counted as ASICs.

Programmable Logic Devices (PLDs). PLDs are defined as ICs programmed after assembly. Memory devices such as PROMs and ROMs are not included in this market segment.

Gate Arrays. Gate arrays are defined as ICs that contain a configuration of uncommitted elements. They are customized by interconnecting these elements with one or more routing layers. Included in this category are generic or custom-base wafers, which include embedded functions such as static RAM.

Cell-Based ICs (CBICs). Cell-based ICs are defined as ICs customized by using a full set of masks and using automatic place and route.

Full-Custom ICs. Full-Custom ICs are defined as ASICs customized using a full set of masks and using manual place and route.

Revenue Classification

Because systems may be fabricated, assembled, and sold in several different locations, Dataquest regional device consumption is defined according to the shipping destination.

Consumption estimates include the following five sources of revenue:

- Intracompany revenue (sales to internal divisions)
- Nonrecurring engineering (NRE) revenue
- ASIC software revenue
- PLD development kit revenue
- Device production revenue

Despite the care taken in gathering, analyzing, and categorizing the data in a meaningful way, careful attention must be paid to the definitions and assumptions used herein when interpreting the estimates presented in this document. Various companies, government agencies, and trade associations may use slightly different definitions of product categories and regional groupings, or they may include different companies in their summaries. These differences should be kept in mind when making comparisons between data and numbers provided by Dataquest and those provided by other suppliers.

Merchant versus Captive Consumption

Dataquest includes all revenue, both merchant and captive, for semiconductor suppliers selling to the merchant market. Dataquest's consumption estimates do not include captive-only manufacturing companies represented by companies such as Digital Equipment Corporation, IBM, or Unisys that do not sell semiconductor products in the merchant market.

Regional Definitions

North America: Includes United States and Canada

Europe: Western Europe

Japan: Japan

Asia/Pacific-Rest of World: All other countries

Forecast Methodology and Assumptions

Dataquest publishes five-year factory revenue forecasts for the ASIC market during the second quarter of each year. In doing so, Dataquest utilizes a variety of forecasting techniques (both qualitative and quantitative) that

vary by technology area. An overview of Dataquest forecasting techniques can be found in the *Dataquest Research and Forecast Methodology* document.

ASIC Forecast Methodology

Dataquest's forecast methodology includes the following steps:

- Formally and informally survey the leading ASIC vendors (in gate arrays, CBICs, and PLDs) throughout the year for their expectations, as well as for their views of the application markets they participate in.
- Formally survey ASIC users for their expected buying patterns, in addition to their views on the growth of the application markets they participate in.
- Examine statistics provided by a number of industry organizations (such as WSTS, MITI, and DOC) for up-to-date monthly trends.
- Perform time-series analysis as well as apply judgmental industry knowledge to product and application trends.

ASIC Forecast Assumptions

ASICs

The 1992 worldwide ASIC market is expected to experience the lowest growth rate in history at 3.5 percent (including full-custom ICs), primarily because Japan, which accounts for more than 40 percent of the worldwide ASIC market, has entered a recession.

Dataquest's ASIC forecast is based on the assumption that the Japanese economy will return to typical positive growth rates in the third and fourth quarters of 1992. Furthermore, we assume that the North American economy will pull out of its recession in the third quarter of 1992. This forecast should be considered overly optimistic if these assumptions on Japan and North American do not materialize.

The 1992 European ASIC market is expected to experience similar growth to that of 1991.

The personal computer clone market experienced severe price erosion during 1991, which caused the 1991 Asia/Pacific-Rest of World (ROW) ASIC market to stall. The 1992 Asia/Pacific-ROW growth rate is expected to return to a more typical 20 percent rate as companies in this region diversify into other application markets, such as the consumer market.

Application-specific standard products (ASSPs) will continue to experience rapid proliferation and will further reduce the growth of the ASIC market.

Full-custom ICs are being replaced by gate arrays and cell-based ICs, both of which offer reduced NRE charges and a quicker time-to-market when compared with full-custom ICs.

Gate Arrays

MOS Gate Arrays

CMOS continues to be the dominant gate array technology for the foreseeable future because of its low cost, low power consumption, and high integration.

The North American CMOS gate array market will closely track the computer market because more than 60 percent of all gate arrays are consumed in data processing applications.

The low-end CMOS market (less than 20,000 gates) will continue to be adversely impacted by field-programmable gate arrays (FPGAs).

Embedded gate arrays (that is, megacells such as SRAMs that are diffused in the array base wafer) are included in the gate array category and are expected to fuel gate array growth by the mid-1990s.

Although we believe that the price-per-gate will continue to drop, average selling prices (ASPs) still are expected to rise because of the increasing use of on-chip functions such as SRAM, ALU, multiplier, multiplier-accumulator, FIFO, DMA controller, cache controller, and 82XX microperipherals.

Bipolar Gate Arrays

Bipolar gate arrays are being replaced by CMOS, BiCMOS, and GaAs ASICs because of their high cost and high power consumption.

The TTL gate array market is declining, primarily because there have been no new TTL arrays designed in the past three years, and production of these devices is accordingly winding down.

The ECL gate array market is declining in all regions because most ECL arrays are consumed in large mainframe and supercomputers, which are declining markets.

BiCMOS Gate Arrays

BiCMOS gate array growth has been pushed out one to two years from our previous forecast because of the lack of high-volume production from vertically integrated companies such as Fujitsu, NEC, and AT&T. At this point, the costs of these BiCMOS devices do not outweigh the benefits from BiCMOS in comparison to CMOS.

According to Dataquest's worldwide end-user survey of more than 500 systems designers, there is strong interest in using BiCMOS ASICs in their next-generation systems design.

Cell-Based ICs

MOS CBICs

Gate arrays will continue to penetrate many CBIC applications because of their low pricing and the vast number of suppliers, as well as because of the increasing functionality and performance associated with the emerging embedded gate array.

There will be an increasing use of CBICs in Japan (at the expense of gate arrays) in high-volume applications such as video games, printers, and disk drives, mainly because of the smaller die size of CBICs.

Telecom applications are driving the CBIC growth in Europe.

Bipolar CBICs

Bipolar CBIC growth stems from two product types: ECL CBICs and analog CBICs.

ECL CBICs are expected to experience negative growth, primarily because system designers do not want macros supplied by ASIC vendors, they want to design their own macros on the transistor level in order to optimize their designs for their unique applications.

Analog CBICs such as National's "Classic" line are expected to experience modest growth.

BiCMOS CBICs

BiCMOS CBICs are a good solution for mixed analog/digital applications. The analog portion can be implemented using bipolar technology and the digital portion with CMOS technology.

BiCMOS CBICs are expected to be used in many telecom applications.

PLDs

CMOS PLDs

CMOS PLD growth stems from three types of devices: simple PLDs (SPLDs), complex PLDs (CPLDs), and field-programmable gate arrays (FPGAs).

The SPLD market is expected to track just above overall semiconductor growth over the next few years. However, growth rates will continue to fall as these small devices are replaced with higher-density CPLDs and FPGAs.

Dataquest believes that CPLDs will continue to show robust growth. However, short-term growth has been stunted for the following reasons:

- Pricing pressure between Altera and second source Cypress
- Lack of other significant entrants besides AMD and Lattice
- Continued competition with higher-density FPGAs

It is our assumption that CPLDs will continue to hold slight ease-of-use and speed advantages over FPGAs.

The FPGA market is expected to show excellent growth over the next five years for the following reasons:

- The shift continues from TTL- and PAL-based designs toward FPGA usage.

- FPGAs will not only attack the low-end gate array market (<10,000 gates), they will also attack the 10,000- to 20,000-gate array market in the 1993 to 1995 time frame as gate array vendors migrate to high-complexity devices.
- Additional market impetus will come from the large number of new entrants into the market, including hot start-up companies and the Japanese companies.

Bipolar PLDs

The bipolar PLDs market is clearly declining because of a shift in consumption from bipolar PLDs to CMOS PLDs. This market will continue to decline until only a few high-speed ECL devices and specialty high-drive PLDs remain.

Exchange Rates

Dataquest used an average annual exchange rate in converting revenue to U.S. dollar amounts. The following outlines these rates for 1989 through 1991.

	1989	1990	1991
Japan (Yen/U.S.$)	138	144	136
France (Franc/U.S.$)	6.39	5.44	5.64
Germany (Deutsche Mark/U.S.$)	1.88	1.62	1.66
United Kingdom (U.S.$/Pound Sterling)	1.50	1.79	1.77

Table 1-1
Revenue from ASICs by Technology Shipped to the World
(Millions of U.S. Dollars)

	1989	1990	1991	1992	1993	1994	1995	1996	CAGR (%) 1991-1996
Total ASIC	8,123	8,997	9,519	9,839	11,016	12,413	14,042	15,878	10.8
MOS ASIC	5,930	6,765	7,363	7,723	8,818	10,029	11,337	12,696	11.5
Bipolar ASIC	2,071	2,061	1,924	1,772	1,665	1,542	1,416	1,280	-7.8
BiCMOS ASIC	122	171	232	344	533	842	1,289	1,902	52.3
Total Gate Array	3,355	3,654	3,914	4,016	4,649	5,418	6,301	7,334	13.4
MOS Gate Array	2,150	2,405	2,671	2,773	3,313	3,919	4,551	5,239	14.4
Bipolar Gate Array	1,110	1,117	1,074	998	961	907	844	768	-6.5
BiCMOS Gate Array	95	132	169	245	375	592	906	1,327	51.0
Total PLD	695	824	902	1,003	1,118	1,274	1,462	1,643	12.7
MOS PLD	263	401	559	722	890	1,093	1,320	1,535	22.4
Bipolar PLD	432	423	343	281	228	181	142	108	-20.6
Total Cell-Based IC	1,469	2,033	2,258	2,470	2,969	3,549	4,231	4,990	17.2
MOS Cell-Based IC	1,364	1,893	2,103	2,281	2,722	3,212	3,762	4,331	15.5
Bipolar Cell-Based IC	78	101	92	90	89	87	86	84	-1.8
BiCMOS Cell-Based IC	27	39	63	99	158	250	383	575	55.6
Full Custom IC	2,604	2,486	2,445	2,350	2,280	2,172	2,048	1,911	-4.8

Source: Dataquest (August 1992)

Table 1-2
Revenue (Millions of U.S. Dollars) and Percentage of ASICs by Technology Shipped to the World

	1989	1990	1991	1992	1993	1994	1995	1996	CAGR (%) 1991-1996
Total ASIC	8,123	8,997	9,519	9,839	11,016	12,413	14,042	15,878	10.8
MOS ASIC	5,930	6,765	7,363	7,723	8,818	10,029	11,337	12,696	11.5
Bipolar ASIC	2,071	2,061	1,924	1,772	1,665	1,542	1,416	1,280	-7.8
BiCMOS ASIC	122	171	232	344	533	842	1,289	1,902	52.3
Total ASIC (%)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	
MOS ASIC (%)	73.0	75.2	77.3	78.5	80.0	80.8	80.7	80.0	
Bipolar ASIC (%)	25.5	22.9	20.2	18.0	15.1	12.4	10.1	8.1	
BiCMOS ASIC (%)	1.5	1.9	2.4	3.5	4.8	6.8	9.2	12.0	

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (August 1992)

Table 1-3
Revenue from ASICs by Technology Shipped by Region
(Millions of U.S. Dollars)

	1989	1990	1991	1992	1993	1994	1995	1996
Worldwide	5,519	6,511	7,074	7,490	8,736	10,241	11,994	13,967
MOS ASIC	3,777	4,699	5,333	5,777	6,925	8,224	9,633	11,105
Bipolar ASIC	1,620	1,641	1,509	1,369	1,278	1,175	1,072	960
BiCMOS ASIC	122	171	232	344	533	842	1,289	1,902
North America	2,540	2,905	3,005	3,276	3,732	4,258	4,878	5,531
MOS ASIC	1,765	2,128	2,274	2,557	3,022	3,528	4,083	4,629
Bipolar ASIC	749	739	679	642	589	531	478	424
BiCMOS ASIC	26	38	52	77	121	199	317	478
Japan	1,879	2,193	2,478	2,357	2,769	3,325	3,993	4,767
MOS ASIC	1,166	1,415	1,712	1,625	1,973	2,412	2,909	3,438
Bipolar ASIC	641	682	648	566	542	510	471	425
BiCMOS ASIC	72	96	118	166	254	403	613	904
Europe	853	1,086	1,263	1,464	1,754	2,052	2,368	2,735
MOS ASIC	650	875	1,043	1,223	1,475	1,720	1,955	2,212
Bipolar ASIC	179	175	161	148	138	128	119	109
BiCMOS ASIC	24	36	59	93	141	204	294	414
Asia/Pacific-Rest of World	247	327	328	393	481	606	755	934
MOS ASIC	196	281	304	372	455	564	686	826
Bipolar ASIC	51	45	21	13	9	6	4	2
BiCMOS ASIC	0	1	3	8	17	36	65	106

Note: Full Custom ICs are excluded from this table.
Source: Dataquest (August 1992)

Table 1-4
Revenue from ASICs by Technology Shipped by Region
(Percentage Growth)

	1989	1990	1991	1992	1993	1994	1995	1996	CAGR (%) 1991-1996
Worldwide ASIC	11.3	18.0	8.6	5.9	16.6	17.2	17.1	16.4	14.6
North America	6.0	14.4	3.5	9.0	13.9	14.1	14.6	13.4	13.0
Japan	15.0	16.7	13.0	-4.9	17.5	20.1	20.1	19.4	14.0
Europe	19.6	27.3	16.3	15.9	19.8	17.0	15.4	15.5	16.7
Asia/Pacific-Rest of World	14.4	32.50	0.2	19.7	22.6	25.8	24.6	23.7	23.3
Worldwide MOS ASIC	12.7	24.4	13.5	8.3	19.9	18.8	17.1	15.3	15.8
North America	10.3	20.6	6.9	12.5	18.2	16.8	15.7	13.4	15.3
Japan	6.4	21.4	21.0	-5.1	21.4	22.3	20.6	18.2	15.0
Europe	31.6	34.6	19.2	17.3	20.6	16.6	13.7	13.1	16.2
Asia/Pacific-Rest of World	22.4	43.4	8.2	22.2	22.6	23.8	21.6	20.4	22.1
Worldwide Bipolar ASIC	7.3	1.3	-8.0	-9.3	-6.6	-8.1	-8.8	-10.4	-8.6
North America	-3.6	-1.3	-8.1	-5.5	-8.3	-9.7	-10.1	-11.3	-9.0
Japan	36.3	6.4	-4.9	-12.7	-4.2	-5.8	-7.7	-9.7	-8.1
Europe	-13.5	-2.2	-8.0	-8.1	-6.8	-7.2	-7.0	-8.4	-7.5
Asia/Pacific-Rest of World	-9.6	-10.3	-53.7	-38.1	-30.8	-33.3	-33.3	-50.0	-37.5
Worldwide BiCMOS ASIC	24.1	40.6	35.7	48.3	55.1	57.9	53.0	47.5	52.3
North America	35.5	46.0	38.3	47.3	57.8	64.3	59.6	50.8	55.8
Japan	7.2	34.2	22.4	41.0	52.7	58.7	52.0	47.5	50.3
Europe	100.0	50.0	63.9	57.6	52.1	44.4	44.0	40.7	47.7
Asia/Pacific-Rest of World	NM	NM	200.0	166.7	112.5	111.8	80.6	63.1	104.0

Note: Full Custom ICs are excluded from this table.
NM = Not meaningful
Source: Dataquest (August 1992)

Table 1-5
Revenue from ASICs by Technology Shipped by Region
(Percentage of Dollars)

	1989	1990	1991	1992	1993	1994	1995	1996
Worldwide ASIC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	46.0	44.6	42.5	43.7	42.7	41.6	40.7	39.6
Japan	34.0	33.7	35.0	31.5	31.7	32.5	33.3	34.1
Europe	15.5	16.7	17.9	19.6	20.1	20.0	19.7	19.6
Asia/Pacific-Rest of World	4.5	5.0	4.6	5.2	5.5	5.9	6.3	6.7
Worldwide MOS ASIC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	46.7	45.3	42.6	44.3	43.6	42.9	42.4	41.7
Japan	30.9	30.1	32.1	28.1	28.5	29.3	30.2	31.0
Europe	17.2	18.6	19.6	21.2	21.3	20.9	20.3	19.9
Asia/Pacific-Rest of World	5.2	6.0	5.7	6.4	6.6	6.9	7.1	7.4
Worldwide Bipolar ASIC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	46.2	45.0	45.0	46.9	46.1	45.2	44.6	44.2
Japan	39.6	41.5	42.9	41.3	42.4	43.4	43.9	44.2
Europe	11.0	10.7	10.7	10.8	10.8	10.9	11.1	11.3
Asia/Pacific-Rest of World	3.1	2.8	1.4	0.9	0.7	0.5	0.4	0.2
Worldwide BiCMOS ASIC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	21.2	22.0	22.4	22.3	22.7	23.6	24.6	25.1
Japan	59.1	56.4	50.9	48.4	47.6	47.9	47.6	47.5
Europe	19.7	21.2	25.4	27.0	26.5	24.3	22.8	21.8
Asia/Pacific-Rest of World	0	0.6	1.3	2.3	3.2	4.3	5.0	5.6

Notes: Full Custom ICs are excluded from this table.
Columns may not add to totals shown because of rounding.
Source: Dataquest (August 1992)

Table 2-1
Revenue from Gate Arrays by Technology Shipped to the World
(Millions of U.S. Dollars)

	1989	1990	1991	1992	1993	1994	1995	1996	CAGR (%) 1991-1996
Total ASIC	8,123	8,997	9,519	9,839	11,016	12,413	14,042	15,878	10.8
Total Gate Array	3,355	3,654	3,914	4,016	4,649	5,418	6,301	7,334	13.4
MOS Gate Array	2,150	2,405	2,671	2,773	3,313	3,919	4,551	5,239	14.4
Bipolar Gate Array	1,110	1,117	1,074	998	961	907	844	768	-6.5
BiCMOS Gate Array	95	132	169	245	375	592	906	1,327	51.0
Total Gate Array (%)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	
MOS Gate Array (%)	64.1	65.8	68.2	69.0	71.3	72.3	72.2	71.4	
Bipolar Gate Array (%)	33.1	30.6	27.4	24.9	20.7	16.7	13.4	10.5	
BiCMOS Gate Array (%)	2.8	3.6	4.3	6.1	8.1	10.9	14.4	18.1	

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (August 1992)

Table 2-2
Revenue from Gate Arrays by Technology Shipped by Region
(Millions of U.S. Dollars)

	1989	1990	1991	1992	1993	1994	1995	1996
Worldwide	3,355	3,654	3,914	4,016	4,649	5,418	6,301	7,334
MOS Gate Array	2,150	2,405	2,671	2,773	3,313	3,919	4,551	5,239
Bipolar Gate Array	1,110	1,117	1,074	998	961	907	844	768
BiCMOS Gate Array	95	132	169	245	375	592	906	1,327
North America	1,280	1,339	1,405	1,527	1,738	1,990	2,277	2,600
MOS Gate Array	808	873	947	1,051	1,240	1,451	1,669	1,902
Bipolar Gate Array	448	431	410	406	390	366	341	310
BiCMOS Gate Array	24	35	48	70	108	173	267	388
Japan	1,546	1,706	1,843	1,726	2,003	2,350	2,774	3,268
MOS Gate Array	918	1,029	1,163	1,070	1,284	1,528	1,803	2,092
Bipolar Gate Array	560	586	569	501	486	461	429	390
BiCMOS Gate Array	68	91	111	155	233	361	542	786
Europe	407	467	498	557	652	754	845	962
MOS Gate Array	308	367	400	456	547	640	717	810
Bipolar Gate Array	96	95	91	88	84	80	74	68
BiCMOS Gate Array	3	5	7	13	21	34	54	84
Asia/Pacific-Rest of World	122	142	168	206	256	324	405	504
MOS Gate Array	116	136	161	196	242	300	362	435
Bipolar Gate Array	6	5	4	3	1	0	0	0
BiCMOS Gate Array	0	1	3	7	13	24	43	69

Source: Dataquest (August 1992)

Table 2-3
Revenue from Gate Arrays by Technology Shipped by Region
(Percentage Growth)

	1989	1990	1991	1992	1993	1994	1995	1996	CAGR (%) 1991-1996
Worldwide Gate Array	12.4	8.9	7.1	2.6	15.8	16.5	16.3	16.4	13.4
North America	11.1	4.6	5.0	8.7	13.8	14.5	14.4	14.2	13.1
Japan	15.6	10.4	8.0	-6.3	16.0	17.4	18.0	17.8	12.1
Europe	8.0	14.7	6.6	11.8	17.2	15.5	12.2	13.8	14.1
Asia/Pacific-Rest of World	2.4	16.9	18.0	22.9	23.8	26.6	25.3	24.3	24.6
Worldwide MOS Gate Array	11.2	11.9	11.1	3.8	19.5	18.3	16.1	15.1	14.4
North America	14.6	8.1	8.5	11.0	18.0	17.0	15.0	14.0	15.0
Japan	6.9	12.1	13.0	-8.0	20.0	19.0	18.0	16.0	12.5
Europe	19.8	19.2	9.0	14.0	20.0	17.0	12.0	13.0	15.2
Asia/Pacific-Rest of World	3.8	17.0	18.4	22.0	23.0	24.0	21.0	20.0	22.0
Worldwide Bipolar Gate Array	15.0	0.6	-3.8	-7.1	-3.7	-5.6	-6.9	-8.9	-6.5
North America	4.9	-4.0	-4.9	-1.0	-4.0	-6.0	-7.0	-9.0	-5.4
Japan	35.8	4.6	-2.8	-12.0	-3.0	-5.0	-7.0	-9.0	-7.3
Europe	-18.6	-1.0	-4.2	-3.3	-4.5	-6.0	-6.3	-8.1	-5.7
Asia/Pacific-Rest of World	-20.0	-3.6	-25.9	-25.0	-66.7	-100.0	NM	NM	NM
Worldwide BiCMOS Gate Array	8.7	39.5	28.0	45.0	53.2	57.7	53.1	46.3	51.0
North America	25.0	45.6	38.8	45.0	55.0	60.0	55.0	45.0	51.9
Japan	2.8	34.7	21.4	40.0	50.0	55.0	50.0	45.0	47.9
Europe	50.0	66.7	40.0	85.7	65.0	60.0	58.0	55.0	64.4
Asia/Pacific-Rest of World	NM	NM	200.0	133.3	85.7	84.6	79.2	60.5	87.2

NM = Not meaningful

Source: Dataquest (August 1992)

Table 2-4
Revenue from Gate Arrays by Technology Shipped by Region
(Percentage of Dollars)

	1989	1990	1991	1992	1993	1994	1995	1996
Worldwide Gate Array	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	38.2	36.6	35.9	38.0	37.4	36.7	36.1	35.5
Japan	46.1	46.7	47.1	43.0	43.1	43.4	44.0	44.6
Europe	12.1	12.8	12.7	13.9	14.0	13.9	13.4	13.1
Asia/Pacific-Rest of World	3.6	3.9	4.3	5.1	5.5	6.0	6.4	6.9
Worldwide MOS Gate Array	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	37.6	36.3	35.5	37.9	37.4	37.0	36.7	36.3
Japan	42.7	42.8	43.5	38.6	38.8	39.0	39.6	39.9
Europe	14.3	15.3	15.0	16.4	16.5	16.3	15.8	15.5
Asia/Pacific-Rest of World	5.4	5.7	6.0	7.1	7.3	7.6	8.0	8.3
Worldwide Bipolar Gate Array	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	40.4	38.6	38.2	40.7	40.6	40.4	40.4	40.3
Japan	50.4	52.4	53.0	50.2	50.6	50.9	50.9	50.8
Europe	8.6	8.5	8.5	8.8	8.7	8.7	8.8	8.8
Asia/Pacific-Rest of World	0.5	0.5	0.4	0.3	0.1	0	0	0
Worldwide BiCMOS Gate Array	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	25.1	26.2	28.4	28.4	28.7	29.1	29.5	29.2
Japan	71.7	69.3	65.7	63.4	62.1	61.0	59.8	59.2
Europe	3.2	3.8	4.1	5.3	5.7	5.8	6.0	6.3
Asia/Pacific-Rest of World	0	0.8	1.8	2.9	3.5	4.1	4.7	5.2

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (August 1992)

Table 3-1
Revenue from Cell-Based ICs by Technology Shipped to the World
(Millions of U.S. Dollars)

	1989	1990	1991	1992	1993	1994	1995	1996	CAGR (%) 1991-1996
Total ASIC	8,123	8,997	9,519	9,839	11,016	12,413	14,042	15,878	10.8
Total Cell-Based IC	1,469	2,033	2,258	2,470	2,969	3,549	4,231	4,990	17.2
MOS Cell-Based IC	1,364	1,893	2,103	2,281	2,722	3,212	3,762	4,331	15.5
Bipolar Cell-Based IC	78	101	92	90	89	87	86	84	-1.8
BiCMOS Cell-Based IC	27	39	63	99	158	250	383	575	55.6
Total Cell-Based IC (%)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	
MOS Cell-Based IC (%)	92.9	93.1	93.1	92.3	91.7	90.5	88.9	86.8	
Bipolar Cell-Based IC (%)	5.3	5.0	4.1	3.6	3.0	2.5	2.0	1.7	
BiCMOS Cell-Based IC (%)	1.8	1.9	2.8	4.0	5.3	7.0	9.1	11.5	

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (August 1992)

Table 3-2
Revenue from Cell-Based ICs by Technology Shipped by Region
(Millions of U.S. Dollars)

	1989	1990	1991	1992	1993	1994	1995	1996
Worldwide	1,469	2,033	2,258	2,470	2,969	3,549	4,231	4,990
MOS Cell-Based IC	1,364	1,893	2,103	2,281	2,722	3,212	3,762	4,331
Bipolar Cell-Based IC	78	101	92	90	89	87	86	84
BiCMOS Cell-Based IC	27	39	63	99	158	250	383	575
North America	843	1,078	1,048	1,119	1,303	1,512	1,747	1,983
MOS Cell-Based IC	790	1,018	990	1,059	1,239	1,438	1,653	1,852
Bipolar Cell-Based IC	51	57	54	53	51	48	44	41
BiCMOS Cell-Based IC	2	3	4	7	13	26	50	90
Japan	243	369	514	510	623	781	974	1,205
MOS Cell-Based IC	216	327	479	474	579	717	882	1,068
Bipolar Cell-Based IC	23	37	28	25	23	22	21	19
BiCMOS Cell-Based IC	4	5	7	11	21	42	71	118
Europe	319	469	582	700	865	1,027	1,218	1,436
MOS Cell-Based IC	294	431	520	608	730	840	957	1,082
Bipolar Cell-Based IC	4	7	10	12	15	17	21	24
BiCMOS Cell-Based IC	21	31	52	80	120	170	240	330
Asia/Pacific-Rest of World	64	117	114	141	178	229	292	366
MOS Cell-Based IC	64	117	114	140	174	217	270	329
Bipolar Cell-Based IC	0	0	0	0	0	0	0	0
BiCMOS Cell-Based IC	0	0	0	1	4	12	22	37

Source: Dataquest (August 1992)

Table 3-3
Revenue from Cell-Based ICs by Technology Shipped by Region
(Percentage Growth)

	1989	1990	1991	1992	1993	1994	1995	1996	CAGR (%) 1991-1996
Worldwide Cell-Based IC	13.0	38.4	11.1	9.4	20.1	19.6	19.2	17.9	17.2
North America	4.7	27.9	-2.8	6.8	16.4	16.0	15.6	13.5	13.6
Japan	3.8	51.9	39.3	-0.7	21.9	25.6	24.7	23.7	18.6
Europe	45.0	47.0	24.1	20.3	23.5	18.7	18.7	17.8	19.8
Asia/Pacific-Rest of World	56.5	82.0	-2.6	23.9	26.0	28.9	27.1	25.5	26.3
Worldwide MOS Cell-Based IC	9.6	38.8	11.1	8.5	19.3	18.0	17.1	15.1	15.5
North America	2.6	28.9	-2.8	7.0	17.0	16.0	15.0	12.0	13.3
Japan	-3.6	51.6	46.5	-1.0	22.0	24.0	23.0	21.0	17.4
Europe	40.0	46.6	20.6	17.0	20.0	15.0	14.0	13.0	15.8
Asia/Pacific-Rest of World	56.5	82.0	-2.6	23.0	24.0	25.0	24.0	22.0	23.6
Worldwide Bipolar Cell-Based IC	77.3	29.5	-8.9	-2.2	-1.5	-1.9	-1.4	-2.1	-1.8
North America	45.7	12.4	-5.3	-1.9	-3.8	-5.9	-8.3	-7.0	-100.0
Japan	153.4	58.8	-24.3	-10.7	-9.4	-3.1	-5.4	-8.2	-7.4
Europe	NM	75.0	42.9	20.0	25.0	13.3	23.5	14.3	19.1
Asia/Pacific-Rest of World	NM	NM	NM	NM	NM	NM	NM	NM	NM
Worldwide BiCMOS Cell-Based IC	145.5	44.4	61.5	57.1	59.6	58.2	53.2	50.1	55.6
North America	NM	50.0	33.3	75.0	85.7	100.0	92.3	80.0	86.4
Japan	300.0	25.0	40.0	57.1	90.9	100.0	69.0	66.2	75.9
Europe	110.0	47.6	67.7	53.8	50.0	41.7	41.2	37.5	44.7
Asia/Pacific-Rest of World	NM	NM	NM	NM	300.0	200.0	83.3	68.2	146.6

NM = Not meaningful
Source: Dataquest (August 1992)

Table 3-4
Revenue from Cell-Based ICs by Technology Shipped by Region
(Percentage of Dollars)

	1989	1990	1991	1992	1993	1994	1995	1996
Worldwide Cell-Based IC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	57.4	53.0	46.4	45.3	43.9	42.6	41.3	39.7
Japan	16.5	18.2	22.8	20.6	21.0	22.0	23.0	24.1
Europe	21.7	23.1	25.8	28.3	29.1	28.9	28.8	28.8
Asia/Pacific-Rest of World	4.4	5.8	5.0	5.7	6.0	6.5	6.9	7.3
Worldwide MOS Cell-Based IC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	57.9	53.8	47.1	46.4	45.5	44.8	43.9	42.8
Japan	15.8	17.3	22.8	20.8	21.3	22.3	23.5	24.7
Europe	21.6	22.8	24.7	26.7	26.8	26.1	25.4	25.0
Asia/Pacific-Rest of World	4.7	6.2	5.4	6.1	6.4	6.8	7.2	7.6
Worldwide Bipolar Cell-Based IC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	65.0	56.4	58.7	58.9	57.3	55.2	51.2	48.7
Japan	29.9	36.6	30.4	27.8	25.8	25.3	24.4	22.7
Europe	5.1	6.9	10.9	13.3	16.9	19.5	24.4	28.6
Asia/Pacific-Rest of World	0	0	0	0	0	0	0	0
Worldwide BiCMOS Cell-Based IC	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	7.4	7.7	6.3	7.1	8.2	10.4	13.1	15.7
Japan	14.8	12.8	11.1	11.1	13.3	16.8	18.5	20.5
Europe	77.8	79.5	82.5	80.8	75.9	68.0	62.7	57.4
Asia/Pacific-Rest of World	0	0	0	1.0	2.5	4.8	5.7	6.4

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (August 1992)

Table 4-1
Revenue from PLD ICs by Technology Shipped to the World
(Millions of U.S. Dollars)

	1989	1990	1991	1992	1993	1994	1995	1996	CAGR (%) 1991-1996
Total ASIC	8,123	8,997	9,519	9,839	11,016	12,413	14,042	15,878	10.8
Total PLD	695	824	902	1,003	1,118	1,274	1,462	1,643	12.7
MOS PLD	263	401	559	722	890	1,093	1,320	1,535	22.4
Bipolar PLD	432	423	343	281	228	181	142	108	-20.6
Total PLD (%)	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	
MOS PLD (%)	37.8	48.7	62.0	72.0	79.6	85.8	90.3	93.4	
Bipolar PLD (%)	62.2	51.3	38.0	28.0	20.4	14.2	9.7	6.6	

Source: Dataquest (August 1992)

Table 4-2
Revenue from PLD ICs by Technology Shipped by Region
(Millions of U.S. Dollars)

	1989	1990	1991	1992	1993	1994	1995	1996
Worldwide	695	824	902	1,003	1,118	1,274	1,462	1,643
MOS PLD	263	401	559	722	890	1,093	1,320	1,535
Bipolar PLD	432	423	343	281	228	181	142	108
North America	417	488	552	630	690	756	854	948
MOS PLD	167	237	337	447	542	639	761	875
Bipolar PLD	250	251	215	183	148	117	93	73
Japan	90	118	121	121	143	194	245	294
MOS PLD	32	59	70	81	110	167	224	278
Bipolar PLD	58	59	51	40	33	27	21	16
Europe	127	150	183	207	237	271	305	337
MOS PLD	48	77	123	159	198	240	281	320
Bipolar PLD	79	73	60	48	39	31	24	17
Asia/Pacific-Rest of World	61	68	46	45	48	53	58	64
MOS PLD	16	28	29	35	40	47	54	62
Bipolar PLD	45	40	17	10	8	6	4	2

Source: Dataquest (August 1992)

Table 4-3
Revenue from PLD ICs by Technology Shipped by Region
(Percentage Growth)

	1989	1990	1991	1992	1993	1994	1995	1996	CAGR (%) 1991-1996
Worldwide PLD	3.3	18.6	9.5	11.2	11.5	14.0	14.8	12.4	12.7
North America	-5.0	17.0	13.1	14.1	9.5	9.6	13.0	11.0	11.4
Japan	45.2	31.1	2.5	0	18.2	35.7	26.3	20.0	19.4
Europe	9.5	18.1	22.0	13.1	14.5	14.3	12.5	10.5	13.0
Asia/Pacific-Rest of World	8.9	11.5	-32.4	-2.2	6.7	10.4	9.4	10.3	6.8
Worldwide MOS PLD	52.9	52.5	39.4	29.2	23.3	22.8	20.8	16.3	22.4
North America	33.6	41.9	42.2	32.6	21.3	17.9	19.1	15.0	21.0
Japan	146.2	84.4	18.6	15.7	35.8	51.8	34.1	24.1	31.8
Europe	77.8	60.4	59.7	29.3	24.5	21.2	17.1	13.9	21.1
Asia/Pacific-Rest of World	128.6	75.0	3.6	20.7	14.3	17.5	14.9	14.8	16.4
Worldwide Bipolar PLD	-13.8	-2.1	-18.9	-18.1	-18.9	-20.6	-21.5	-23.9	-20.6
North America	-20.4	0.4	-14.3	-14.9	-19.1	-20.9	-20.5	-21.5	-19.4
Japan	18.4	1.7	-13.6	-21.6	-17.5	-18.2	-22.2	-23.8	-20.7
Europe	-11.2	-7.6	-17.8	-20.0	-18.8	-20.5	-22.6	-29.2	-22.3
Asia/Pacific-Rest of World	-8.2	-11.1	-57.5	-41.2	-20.0	-25.0	-33.3	-50.0	-34.8

Source: Dataquest (August 1992)

Table 4-4
Revenue from PLD ICs by Technology Shipped by Region
(Percentage of Dollars)

	1989	1990	1991	1992	1993	1994	1995	1996
Worldwide PLD	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	60.0	59.2	61.2	62.8	61.7	59.3	58.4	57.7
Japan	12.9	14.3	13.4	12.1	12.8	15.2	16.8	17.9
Europe	18.3	18.2	20.3	20.6	21.2	21.3	20.9	20.5
Asia/Pacific-Rest of World	8.8	8.3	5.1	4.5	4.3	4.2	4.0	3.9
Worldwide MOS PLD	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	63.5	59.1	60.3	61.9	60.9	58.5	57.7	57.0
Japan	12.2	14.7	12.5	11.2	12.4	15.3	17.0	18.1
Europe	18.3	19.2	22.0	22.0	22.2	22.0	21.3	20.8
Asia/Pacific-Rest of World	6.1	7.0	5.2	4.8	4.5	4.3	4.1	4.0
Worldwide Bipolar PLD	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	57.9	59.3	62.7	65.1	64.9	64.6	65.5	67.6
Japan	13.4	13.9	14.9	14.2	14.5	14.9	14.8	14.8
Europe	18.3	17.3	17.5	17.1	17.1	17.1	16.9	15.7
Asia/Pacific-Rest of World	10.4	9.5	5.0	3.6	3.5	3.3	2.8	1.9

Note: Columns may not add to totals shown because of rounding.
Source: Dataquest (August 1992)

Table 4-5
Revenue from PLD ICs by Logic Complexity Shipped to the World
(Millions of U.S. Dollars)

	1989	1990	1991	1992	1993	1994	1995	1996	CAGR (%) 1991-1996
Total PLD	695	824	902	1,003	1,118	1,274	1,462	1,643	12.7
Total Simple PLD	629	672	629	613	611	607	591	569	-2.0
Total Complex PLD and FPGA	66	152	273	390	507	667	871	1,074	31.5
Total CMOS PLD	263	401	559	722	890	1,093	1,320	1,535	22.4
Simple PLD	197	249	286	332	383	426	449	461	10.0
Complex PLD	5	35	84	116	149	194	246	287	27.9
FPGA	61	117	189	274	358	473	625	787	33.0
Total Bipolar PLD	432	423	343	281	228	181	142	108	-20.6
Simple PLD	432	423	343	281	228	181	142	108	-20.6

Source: Dataquest (August 1992)

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ASIC Consumption Forecast

May 1991

Source:
Dataquest

Semiconductors *Worldwide*

ASICs

Dataquest

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Semiconductors *Worldwide*
ASICs

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Table of Contents

This booklet is divided into five major sections.

Chapter 1

Introduction

This booklet presents forecasts for the application-specific integrated circuit (ASIC) market. Data will be presented in chapters according to the ASIC product groupings listed below (with the exception of the full-custom IC category, for which detailed data are not available). ASIC revenue from standard products groups is not included in these data.

Organization

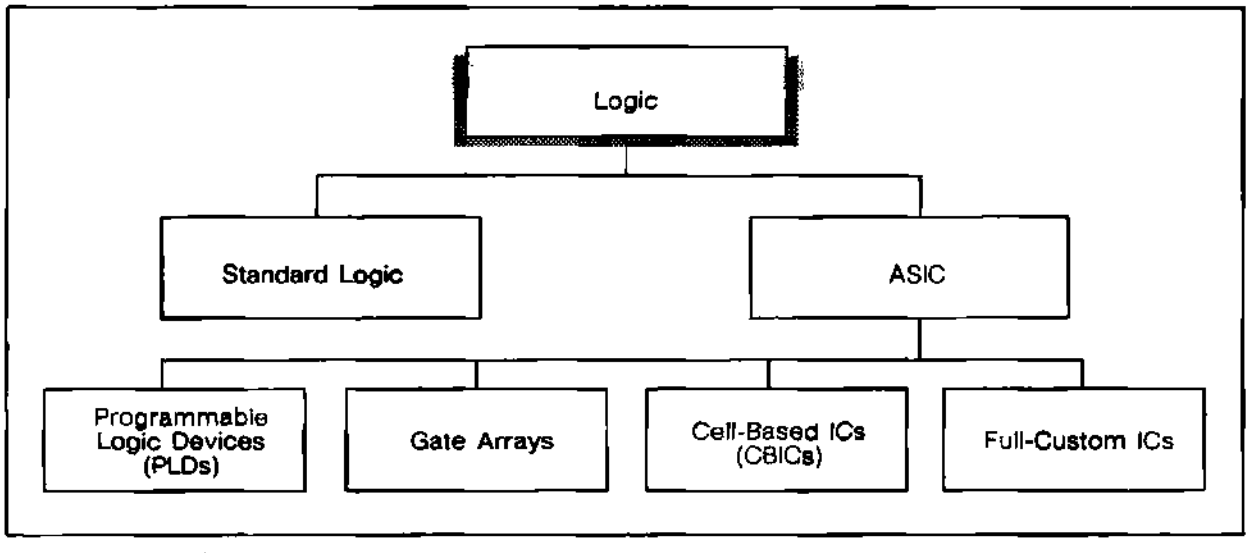
Product Segmentation

Figure 1.1 depicts Dataquest's segmentation of the ASIC category. The ASIC family tree breaks out ASICs as programmable logic devices (PLDs), gate arrays, cell-based ICs (CBICs), and full-custom ICs. CBICs and full-custom ICs are personalized by altering the full set of masks, and PLDs and gate arrays are personalized by electrically programming the devices or by altering only the final layers of interconnect.

Dataquest employs the following criteria to define products within the ASIC segmentation scheme:

- ASICs—This term is used to describe all IC products that are customized for a single user. Customized ICs that are purchased by more than one user become standard products and are no longer counted as ASICs.
- PLDs—PLDs are ICs that are programmed after assembly. Memory devices such as programmable read-only memories (PROMs) and read-only memories (ROMs) are not included in this market segment.
- Gate Arrays—Gate arrays are ICs that contain a configuration of uncommitted elements. They are customized by interconnecting these elements with one or more routing layers. Included in this category are generic or custom base wafers that include embedded functions such as static RAM.

Figure 1.1
ASIC Family Tree



Source: Dataquest (May 1991)

- CBICs—CBICs are ICs that are customized by using a full set of masks and use automatic place and route.
- Full-Custom ICs—Full-custom ICs are ASICs that are customized using a full set of masks and use manual place and route.

Revenue Classification

Because ASICs may be fabricated, assembled, and sold in several different locations, Dataquest uses country of origin as the basis for classifying suppliers. Therefore, for multinational companies the home office (that is, where the balance sheets are consolidated) is considered the country of origin. For example, a company such as Toshiba America selling in North America is considered a Japanese company, whereas a company such as Motorola selling in Japan is counted as a North American company.

Estimates for each company comprise, as applicable, the following four sources of revenue:

- Intracompany revenue
- Sales of electronic design automation (EDA) software
- Nonrecurring engineering (NRE) charges
- Device production

Dataquest's consumption forecasts do not include production by manufacturers that produce ASICs solely for captive use. Examples include Digital Equipment Corporation, IBM, and Unisys.

ASIC Trade-Off Matrix

A basic understanding of the relative merits of the various product approaches within ASICs is an essential prerequisite to the discussion of the forecast material herein. Table 1.1 provides a comparative summary matrix of the various design methodologies in terms of design time, design cost, price per gate, and efficiency.

Table 1.1
ASIC Trade-Off Matrix

Methodology	Design Time	Design Cost	Price Per Gate	Efficiency
Programmable Logic Devices	Shortest	Lowest	Highest	Lowest
Gate Arrays	Short	Low	Low	Medium
Cell-Based ICs	Long	High	Lower	High
Full-Custom Devices	Longest	Highest	Lowest	Highest

Source: Dataquest (May 1991)

Chapter 2

Worldwide ASIC Consumption Forecast—1988-1995

Index of Table Titles—Chapter 2

Table 2.1
ASIC Consumption Forecast by Technology
(Factory Revenue in Millions of U.S. Dollars)

Company: All
Product: Each
Region of Consumption: Worldwide
Distribution Channel: Not Meaningful
Application: All
Specification: All

	1988	1989	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-95
Total ASIC	7,483	8,284	9,269	10,285	11,891	14,042	16,117	18,104	14.3
MOS ASIC	5,400	6,125	7,013	7,877	9,256	11,094	12,660	14,075	14.9
Bipolar ASIC	1,985	2,037	2,085	2,145	2,197	2,184	2,144	2,086	.0
BiCMOS ASIC	98	122	171	263	438	764	1,313	1,943	62.6
Total Gate Array	2,985	3,460	3,861	4,324	5,169	6,352	7,631	8,912	18.2
MOS Gate Array	1,933	2,265	2,559	2,892	3,557	4,481	5,333	6,133	19.1
Bipolar Gate Array	965	1,100	1,170	1,228	1,265	1,252	1,215	1,154	-.3
BiCMOS Gate Array	87	95	132	204	347	619	1,083	1,625	65.2
Total PLD	673	693	828	1,027	1,306	1,660	1,964	2,281	22.5
CMOS PLD	172	258	405	620	911	1,289	1,618	1,971	37.2
Bipolar PLD	501	435	423	407	395	371	346	310	-6.0
Total Cell-Based IC	1,300	1,527	2,094	2,473	3,028	3,738	4,345	4,824	18.2
MOS Cell-Based IC	1,245	1,450	1,982	2,319	2,804	3,421	3,900	4,251	16.5
Bipolar Cell-Based IC	44	50	73	95	133	172	215	255	28.4
BiCMOS Cell-Based IC	11	27	39	59	91	145	230	318	52.2
Full-Custom IC	2,525	2,604	2,486	2,461	2,388	2,292	2,177	2,087	-3.4

Note: Some columns do not add to totals shown because of rounding.

Source: Dataquest (May 1991)

Table 2.2
ASIC Consumption Forecast by Region
(Factory Revenue in Millions of U.S. Dollars)

Company: All
Product: Total ASIC Excluding Full Custom
Region of Consumption: Each
Distribution Channel: Not Meaningful
Application: All
Specification: All

	1988	1989	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-95
Worldwide	4,958	5,680	6,783	7,824	9,503	11,750	13,940	16,017	18.7
MOS ASIC	3,350	3,973	4,946	5,831	7,272	9,191	10,851	12,355	20.1
Bipolar ASIC	1,510	1,585	1,666	1,730	1,793	1,795	1,776	1,719	.6
BiCMOS ASIC	98	122	171	263	438	764	1,313	1,943	62.6
North America	2,396	2,547	2,983	3,351	3,976	4,809	5,583	6,300	16.1
MOS ASIC	1,600	1,784	2,219	2,569	3,151	3,911	4,527	5,070	18.0
Bipolar ASIC	777	737	726	719	711	687	672	644	-2.4
BiCMOS ASIC	19	26	38	63	114	211	384	586	72.8
Japan	1,633	2,033	2,421	2,839	3,455	4,278	5,156	6,061	20.1
MOS ASIC	1,096	1,343	1,606	1,895	2,353	2,972	3,547	4,107	20.7
Bipolar ASIC	470	618	719	801	869	896	898	877	4.1
BiCMOS ASIC	67	72	96	143	233	410	711	1,077	62.2
Europe	713	853	1,051	1,218	1,534	1,941	2,295	2,571	19.6
MOS ASIC	494	650	839	1,000	1,283	1,645	1,944	2,185	21.1
Bipolar ASIC	207	179	176	164	168	170	169	165	-1.3
BiCMOS ASIC	12	24	36	54	83	126	182	221	43.8
Asia/Pacific-Rest of World	216	247	328	416	538	722	906	1,085	27.0
MOS ASIC	160	196	282	367	485	663	833	993	28.6
Bipolar ASIC	56	51	45	46	45	42	37	33	-6.0
BiCMOS ASIC	0	0	1	3	8	17	36	59	126.0

Note: Some columns do not add to totals shown because of rounding.

Source: Dataquest (May 1991)

Table 2.3
ASIC Consumption Forecast by Region
(Percentage of Dollars)

Company:	All
Product:	Total ASIC Excluding Full Custom
Region of Consumption:	Each
Distribution Channel:	Not Meaningful
Application:	All
Specification:	All

	1988	1989	1990	1991	1992	1993	1994	1995
Worldwide Total	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	48.3	44.8	44.0	42.8	41.8	40.9	40.1	39.3
Japan	32.9	35.8	35.7	36.3	36.4	36.4	37.0	37.8
Europe	14.4	15.0	15.5	15.6	16.1	16.5	16.5	16.1
Asia/Pacific-Rest of World	4.4	4.3	4.8	5.3	5.7	6.1	6.5	6.8
Worldwide MOS	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	47.8	44.9	44.9	44.1	43.3	42.6	41.7	41.0
Japan	32.7	33.8	32.5	32.5	32.4	32.3	32.7	33.2
Europe	14.7	16.4	17.0	17.1	17.6	17.9	17.9	17.7
Asia/Pacific-Rest of World	4.8	4.9	5.7	6.3	6.7	7.2	7.7	8.0
Worldwide Bipolar	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	51.5	46.5	43.6	41.6	39.7	38.3	37.8	37.5
Japan	31.1	39.0	43.2	46.3	48.5	49.9	50.6	51.0
Europe	13.7	11.3	10.6	9.5	9.4	9.5	9.5	9.6
Asia/Pacific-Rest of World	3.7	3.2	2.7	2.7	2.5	2.3	2.1	1.9
Worldwide BiCMOS	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	19.4	21.3	22.2	24.0	26.0	27.6	29.2	30.2
Japan	68.4	59.0	56.1	54.4	53.2	53.7	54.2	55.4
Europe	12.2	19.7	21.1	20.5	18.9	16.5	13.9	11.4
Asia/Pacific-Rest of World	.0	.0	.6	1.1	1.8	2.2	2.7	3.0

Note: Some columns do not add to totals shown because of rounding.

Source: Dataquest (May 1991)

Chapter 3

Worldwide Gate Array Consumption Forecast—1988-1995

Index of Table Titles—Chapter 3

Table 3.1
Gate Array Consumption Forecast by Technology
(Factory Revenue in Millions of U.S. Dollars)

Company:	All
Product:	Gate Array
Region of Consumption:	Worldwide
Distribution Channel:	Not Meaningful
Application:	All
Specification:	All

	1988	1989	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-95
Total ASIC	7,483	8,284	9,269	10,285	11,891	14,042	16,117	18,104	14.3
Total Gate Array	2,985	3,460	3,861	4,324	5,169	6,352	7,631	8,912	18.2
MOS Gate Array	1,933	2,265	2,559	2,892	3,557	4,481	5,333	6,133	19.1
Bipolar Gate Array	965	1,100	1,170	1,228	1,265	1,252	1,215	1,154	-.3
BiCMOS Gate Array	87	95	132	204	347	619	1,083	1,625	65.2
Total Gate Array (%)	100	100	100	100	100	100	100	100	
MOS Gate Array (%)	65	65	66	67	69	71	70	69	
Bipolar Gate Array (%)	32	32	30	28	24	20	16	13	
BiCMOS Gate Array (%)	3	3	3	5	7	10	14	18	

Note: Some columns do not add to totals shown because of rounding.

Source: Dataquest (May 1991)

Table 3.2
Gate Array Consumption Forecast by Region
(Factory Revenue in Millions of U.S. Dollars)

Company: All
Product: Gate Array
Region of Consumption: Each
Distribution Channel: Not Meaningful
Application: All
Specification: All

	1988	1989	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-95
Worldwide	2,985	3,460	3,861	4,324	5,169	6,352	7,631	8,912	18.2
MOS Gate Array	1,933	2,265	2,559	2,892	3,557	4,481	5,333	6,133	19.1
Bipolar Gate Array	965	1,100	1,170	1,228	1,265	1,252	1,215	1,154	-.3
BiCMOS Gate Array	87	95	132	204	347	619	1,083	1,625	65.2
North America	1,152	1,281	1,357	1,453	1,676	2,016	2,427	2,815	15.7
MOS Gate Array	705	808	891	972	1,160	1,434	1,701	1,938	16.8
Bipolar Gate Array	428	449	431	423	411	388	372	346	-4.3
BiCMOS Gate Array	19	24	35	58	105	194	354	531	72.3
Japan	1,337	1,650	1,901	2,216	2,677	3,305	3,979	4,707	19.9
MOS Gate Array	859	1,033	1,171	1,368	1,694	2,141	2,554	2,978	20.5
Bipolar Gate Array	412	549	639	712	761	775	756	723	2.5
BiCMOS Gate Array	66	68	91	136	222	389	669	1,006	61.7
Europe	377	407	461	488	599	743	867	960	15.8
MOS Gate Array	257	308	361	393	498	636	748	828	18.1
Bipolar Gate Array	118	96	95	88	88	84	83	81	-3.1
BiCMOS Gate Array	2	3	5	7	13	23	36	51	59.1
Asia/Pacific-Rest of World	119	122	142	167	217	288	358	430	24.8
MOS Gate Array	112	116	136	159	205	270	330	389	23.4
Bipolar Gate Array	7	6	5	5	5	5	4	4	-4.4
BiCMOS Gate Array	0	0	1	3	7	13	24	37	105.9

Note: Some columns do not add to totals shown because of rounding.

Source: Dataquest (May 1991)

Table 3.3
Gate Array Consumption Forecast by Region
(Percentage of Dollars)

Company:	All
Product:	Gate Array
Region of Consumption:	Each
Distribution Channel:	Not Meaningful
Application:	All
Specification:	All

	1988	1989	1990	1991	1992	1993	1994	1995
Worldwide Total	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	38.6	37.0	35.1	33.6	32.4	31.7	31.8	31.6
Japan	44.8	47.7	49.2	51.2	51.8	52.0	52.1	52.8
Europe	12.6	11.8	11.9	11.3	11.6	11.7	11.4	10.8
Asia/Pacific-Rest of World	4.0	3.5	3.7	3.9	4.2	4.5	4.7	4.8
Worldwide MOS	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	36.5	35.7	34.8	33.6	32.6	32.0	31.9	31.6
Japan	44.4	45.6	45.8	47.3	47.6	47.8	47.9	48.6
Europe	13.3	13.6	14.1	13.6	14.0	14.2	14.0	13.5
Asia/Pacific-Rest of World	5.8	5.1	5.3	5.5	5.8	6.0	6.2	6.3
Worldwide Bipolar	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	44.4	40.8	36.8	34.4	32.5	31.0	30.6	30.0
Japan	42.7	49.9	54.6	58.0	60.2	61.9	62.2	62.7
Europe	12.2	8.7	8.1	7.2	7.0	6.7	6.8	7.0
Asia/Pacific-Rest of World	.7	.5	.4	.4	.4	.4	.3	.3
Worldwide BiCMOS	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	21.8	25.3	26.5	28.4	30.3	31.3	32.7	32.7
Japan	75.9	71.6	68.9	66.7	64.0	62.8	61.8	61.9
Europe	2.3	3.2	3.8	3.4	3.7	3.7	3.3	3.1
Asia/Pacific-Rest of World	.0	.0	.8	1.5	2.0	2.1	2.2	2.3

Note: Some columns do not add to totals shown because of rounding.

Source: Dataquest (May 1991)

Chapter 4

Worldwide Cell-Based IC Consumption Forecast—1988-1995

Index of Table Titles—Chapter 4

Table 4.1
Cell-Based IC Consumption Forecast by Technology
(Factory Revenue in Millions of U.S. Dollars)

Company:	All
Product:	Cell-Based IC
Region of Consumption:	Worldwide
Distribution Channel:	Not Meaningful
Application:	All
Specification:	All

	1988	1989	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-95
Total ASIC	7,483	8,284	9,269	10,285	11,891	14,042	16,117	18,104	14.3
Total Cell-Based IC	1,300	1,527	2,094	2,473	3,028	3,738	4,345	4,824	18.2
MOS Cell-Based IC	1,245	1,450	1,982	2,319	2,804	3,421	3,900	4,251	16.5
Bipolar Cell-Based IC	44	50	73	95	133	172	215	255	28.4
BiCMOS Cell-Based IC	11	27	39	59	91	145	230	318	52.2
Total Cell-Based IC (%)	100	100	100	100	100	100	100	100	
MOS Cell-Based IC (%)	96	95	95	94	93	92	90	88	
Bipolar Cell-Based IC (%)	3	3	3	4	4	5	5	5	
BiCMOS Cell-Based IC (%)	1	2	2	2	3	4	5	7	

Note: Some columns do not add to totals shown because of rounding.

Source: Dataquest (May 1991)

Table 4.2
Cell-Based IC Consumption Forecast by Region
(Factory Revenue in Millions of U.S. Dollars)

Company:	All
Product:	Cell-Based IC
Region of Consumption:	Each
Distribution Channel:	Not Meaningful
Application:	All
Specification:	All

	1988	1989	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-95
Worldwide	1,300	1,527	2,094	2,473	3,028	3,738	4,345	4,824	18.2
MOS Cell-Based IC	1,245	1,450	1,982	2,319	2,804	3,421	3,900	4,251	16.5
Bipolar Cell-Based IC	44	50	73	95	133	172	215	255	28.4
BiCMOS Cell-Based IC	11	27	39	59	91	145	230	318	52.2
North America	805	851	1,134	1,312	1,585	1,927	2,176	2,384	16.0
MOS Cell-Based IC	770	814	1,087	1,252	1,503	1,817	2,032	2,194	15.1
Bipolar Cell-Based IC	35	35	44	55	73	93	114	135	25.1
BiCMOS Cell-Based IC	0	2	3	5	9	17	30	55	78.9
Japan	234	293	402	465	569	701	833	955	18.9
MOS Cell-Based IC	224	278	376	428	509	615	703	778	15.7
Bipolar Cell-Based IC	9	11	21	30	49	65	88	106	38.2
BiCMOS Cell-Based IC	1	4	5	7	11	21	42	71	70.0
Europe	220	319	440	538	671	829	973	1,051	19.0
MOS Cell-Based IC	210	294	401	481	590	712	814	867	16.7
Bipolar Cell-Based IC	0	4	8	10	11	14	13	14	11.8
BiCMOS Cell-Based IC	10	21	31	47	70	103	146	170	40.5
Asia/Pacific-Rest of World	41	64	118	158	203	281	363	434	29.8
MOS Cell-Based IC	41	64	118	158	202	277	351	412	28.4
Bipolar Cell-Based IC	0	0	0	0	0	0	0	0	NM
BiCMOS Cell-Based IC	0	0	0	0	1	4	12	22	NM

Note: Some columns do not add to totals shown because of rounding.

NM = Not meaningful

Source: Dataquest (May 1991)

Table 4.3
Cell-Based IC Consumption Forecast by Region
(Percentage of Dollars)

Company:	All
Product:	Cell-Based IC
Region of Consumption:	Each
Distribution Channel:	Not Meaningful
Application:	All
Specification:	All

	1988	1989	1990	1991	1992	1993	1994	1995
Worldwide Total	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	61.9	55.7	54.2	53.1	52.3	51.6	50.1	49.4
Japan	18.0	19.2	19.2	18.8	18.8	18.8	19.2	19.8
Europe	16.9	20.9	21.0	21.8	22.2	22.2	22.4	21.8
Asia/Pacific-Rest of World	3.2	4.2	5.6	6.4	6.7	7.5	8.4	9.0
Worldwide MOS	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	61.8	56.1	54.8	54.0	53.6	53.1	52.1	51.6
Japan	18.0	19.2	19.0	18.5	18.2	18.0	18.0	18.3
Europe	16.9	20.3	20.2	20.7	21.0	20.8	20.9	20.4
Asia/Pacific-Rest of World	3.3	4.4	6.0	6.8	7.2	8.1	9.0	9.7
Worldwide Bipolar	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	79.5	70.0	60.3	57.9	54.9	54.1	53.0	52.9
Japan	20.5	22.0	28.8	31.6	36.8	37.8	40.9	41.6
Europe	.0	8.0	11.0	10.5	8.3	8.1	6.0	5.5
Asia/Pacific-Rest of World	.0	.0	.0	.0	.0	.0	.0	.0
Worldwide BiCMOS	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	.0	7.4	7.7	8.5	9.9	11.7	13.0	17.3
Japan	9.1	14.8	12.8	11.9	12.1	14.5	18.3	22.3
Europe	90.9	77.8	79.5	79.7	76.9	71.0	63.5	53.5
Asia/Pacific-Rest of World	.0	.0	.0	.0	1.1	2.8	5.2	6.9

Note: Some columns do not add to totals shown because of rounding.

Source: Dataquest (May 1991)

Chapter 5

Worldwide Programmable Logic Device Consumption Forecast—1988-1995

Index of Table Titles—Chapter 5

Table 5.1
PLD Consumption Forecast by Technology
(Factory Revenue in Millions of U.S. Dollars)

Company:	All
Product:	PLD
Region of Consumption:	Worldwide
Distribution Channel:	Not Meaningful
Application:	All
Specification:	All

	1988	1989	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-95
Total ASIC	7,483	8,284	9,269	10,285	11,891	14,042	16,117	18,104	14.3
Total PLD	673	693	828	923 1,027	1,306	1,660	1,964	2,281	22.5
CMOS PLD	172	258	405	620	911	1,289	1,618	1,971	37.2
Bipolar PLD	501	435	423	407	395	371	346	310	-6.0
Total PLD (%)	100	100	100	100	100	100	100	100	
CMOS PLD (%)	26	37	49	60	70	78	82	86	
Bipolar PLD (%)	74	63	51	40	30	22	18	14	

Note: Some columns do not add to totals shown because of rounding.

Source: Dataquest (May 1991)

$ 563
-360
923

Table 5.2
PLD Consumption Forecast by Logic Complexity
(Factory Revenue in Millions of U.S. Dollars)

Company:	All
Product:	Each
Region of Consumption:	Worldwide
Distribution Channel:	Not Meaningful
Application:	All
Specification:	All

	1988	1989	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-95
Total PLD	673	693	828	1,027	1,306	1,660	1,964	2,281	22.5
Total SPLD	644	627	676	737	820	929	1,034	1,132	10.9
Total CPLD	29	66	152	290	486	731	930	1,149	49.9
CMOS PLD	172	258	405	620	911	1,289	1,618	1,971	37.2
CMOS SPLD	143	192	253	330	425	558	688	822	26.6
CMOS CPLD	29	66	152	290	486	731	930	1,149	49.9
Bipolar PLD	501	435	423	407	395	371	346	310	-6.0
Bipolar SPLD	501	435	423	407	395	371	346	310	-6.0

Note: Some columns do not add to totals shown because of rounding.

Source: Dataquest (May 1991)

Table 5.3
PLD Consumption Forecast by Region
(Factory Revenue in Millions of U.S. Dollars)

Company:	All
Product:	PLD
Region of Consumption:	Each
Distribution Channel:	Not Meaningful
Application:	All
Specification:	All

	1988	1989	1990	1991	1992	1993	1994	1995	CAGR (%) 1990-95
Worldwide	673	693	828	1,027	1,306	1,660	1,964	2,281	22.5
CMOS PLD	172	258	405	620	911	1,289	1,618	1,971	37.2
Bipolar PLD	501	435	423	407	395	371	346	310	-6.0
North America	439	415	492	586	715	866	980	1,101	17.5
CMOS PLD	125	162	241	345	488	660	794	938	31.2
Bipolar PLD	314	253	251	241	227	206	186	163	-8.3
Japan	62	90	118	158	209	272	344	399	27.6
CMOS PLD	13	32	59	99	150	216	290	351	42.9
Bipolar PLD	49	58	59	59	59	56	54	48	-4.0
Europe	116	127	150	192	264	369	455	560	30.1
CMOS PLD	27	48	77	126	195	297	382	490	44.8
Bipolar PLD	89	79	73	66	69	72	73	70	-.8
Asia/Pacific-Rest of World	56	61	68	91	118	153	185	221	26.6
CMOS PLD	7	16	28	50	78	116	152	192	47.0
Bipolar PLD	49	45	40	41	40	37	33	29	-6.2

Note: Some columns do not add to totals shown because of rounding.

Source: Dataquest (May 1991)

Table 5.4
PLD Consumption Forecast by Region
(Percentage of Dollars)

Company:	All
Product:	PLD
Region of Consumption:	Each
Distribution Channel:	Not Meaningful
Application:	All
Specification:	All

	1988	1989	1990	1991	1992	1993	1994	1995
Worldwide Total	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	65.2	59.9	59.4	57.1	54.7	52.2	49.9	48.3
Japan	9.2	13.0	14.3	15.4	16.0	16.4	17.5	17.5
Europe	17.2	18.3	18.1	18.7	20.2	22.2	23.2	24.6
Asia/Pacific-Rest of World	8.3	8.8	8.2	8.9	9.0	9.2	9.4	9.7
Worldwide CMOS	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	72.7	62.8	59.5	55.6	53.6	51.2	49.1	47.6
Japan	7.6	12.4	14.6	16.0	16.5	16.8	17.9	17.8
Europe	15.7	18.6	19.0	20.3	21.4	23.0	23.6	24.9
Asia/Pacific-Rest of World	4.1	6.2	6.9	8.1	8.6	9.0	9.4	9.7
Worldwide Bipolar	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
North America	62.7	58.2	59.3	59.2	57.5	55.5	53.8	52.6
Japan	9.8	13.3	13.9	14.5	14.9	15.1	15.6	15.5
Europe	17.8	18.2	17.3	16.2	17.5	19.4	21.1	22.6
Asia/Pacific-Rest of World	9.8	10.3	9.5	10.1	10.1	10.0	9.5	9.4

Note: Some columns do not add to totals shown because of rounding.

Source: Dataquest (May 1991)

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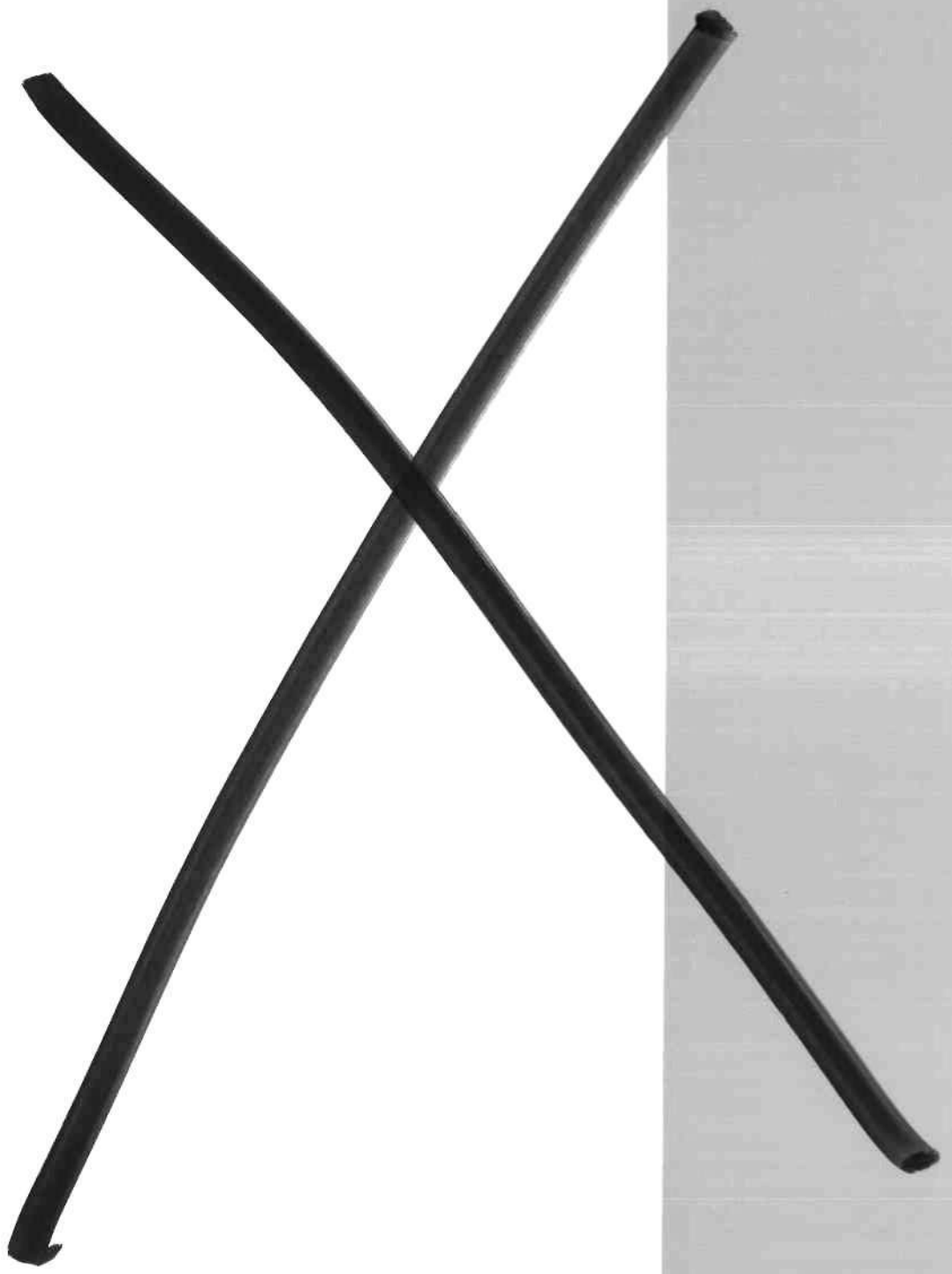

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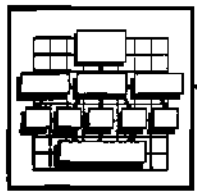

Dataquest Vendor Profile

ASICs *Worldwide*

August 31, 1992

LSI Logic Corporation

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Location	Milpitas, California
Chairman and CEO	Wilfred Corrigan
Number of Employees	4,000
1991 Revenue	$697.8 Million
1991 Net Income	$8.3 Million
Founded	1981
Telephone	(408) 433-8000
Fax	(408) 434-6457

LSI Logic designs, develops, manufactures, and markets integrated circuits (ICs) based on application-specific integrated circuit (ASIC) technology. The company's key product lines are ASICs, which include gate arrays and cell-based ICs; 32-bit SPARC and MIPS RISC microprocessors and peripherals; and application-specific standard products (ASSPs) consisting of PC logic chip sets and graphics products used in IBM-compatible computers. LSI Logic's products and services are marketed primarily to manufacturers in the electronic data processing, military/aerospace, telecommunications, and consumer electronic industries.

Profitability: The Key to Success

Chairman and Chief Executive Officer Wilfred Corrigan states in the 1991 LSI Logic annual report that improving profitability is the company's No. 1 goal. Although LSI Logic has consistently increased annual revenue and has been a driving force in high-performance electronic system design, it has not achieved consistent profitability. Profits have been especially elusive over the last three years. There were net losses of $31.2 million in 1989 and $30.3 million in 1990, and a marginal gain of $8.3 million in 1991. See Tables 1 and 2 for corporate financial highlights and quarterly revenue and earnings history.

Mr. Corrigan is a man of action and is no stranger to solving tough problems. As 1991 progressed, Mr. Corrigan stated, "...it became increasingly clear that we needed to reshape our long-term financial

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ASIC-SEG-VP-9201

Table 1
Five-Year Corporate Highlights
(Thousands of U.S. Dollars)

	1987	1988	1989	1990	1991
Five-Year Revenue	262,131	378,908	546,870	655,491	697,838
Percentage Change	-	44.55	44.33	19.86	6.46
Capital Expenditure	138,993	100,961	114,494	61,998	73,650
Percentage of Revenue	53.02	26.65	20.94	9.46	10.55
R&D Expenditure	28,919	36,964	52,457	60,196	80,802
Percentage of Revenue	11.03	9.76	0.01	9.18	11.58
Number of Employees	2,322	3,329	3,700	4,400	4,000
Revenue ($K)/Employee	112.89	113.82	147.80	148.98	174.46
Net Income	11,340	19,362	-31,254	-30,316	8341
Percentage Change	-	70.74	-261.42	3.00	127.51

Source: Dataquest (August 1992)

Table 2
Quarterly Revenue and Earnings History
(Thousands of U.S. Dollars)

1991/1992 Calendar Years	Q1/91	Q2/91	Q3/91	Q4/91	Q1/92	Q2/92
Revenue	180,243	180,961	172,352	164,282	150,521	151,836
Net Income	2,074	5,654	5,600	-43,654	309	-5,854

Source: Dataquest (August 1992)

model to be more consistent with changing trends in the industry. The computer industry spent much of 1991 adjusting to lower process and tighter cost controls. We had to make adjustments ourselves. We had to be leaner, more productive, more responsive, and consistently profitable. There were no alternatives."

LSI Logic took action—of both short- and long-term nature—during 1991 to improve profitability. Such action lowered the company's break-even point by about 15 percent. Cost-cutting measures taken included the following:

- Reducing the work force
- Forcing vacations during slow periods
- Delaying pay increases
- Delaying the opening of a factory in Japan by one year

- Closing a noncompetitive factory in the United Kingdom
- Discontinuing wafer manufacturing in Canada
- Dropping membership in Sematech

Then, on August 21, 1992, LSI Logic management announced that it will take a restructuring charge in the range of $95 million to $110 million that it estimates will result in a net loss of more than $100 million, or more than $2 per share, in the third quarter ended September 27, 1992. These charges include costs associated with the following:

- The phaseout of the company's Braun-schweig, Germany assembly and test operation
- The write-down of certain U.S. manufacturing assets
- The inventory related to certain discontinued commodity products
- The write-off of certain U.S. manufacturing assets made redundant through a strategic consolidation of the company's manufacturing operations
- Severance costs
- Miscellaneous other costs

If executed properly, these timely actions will position the company to compete more profitably in the very competitive ASIC business.

Further, LSI Logic is another in the long list of ASIC manufacturers to realize that it must depend more on its Japanese facilities for high volume and utilize foundry services to fill voids in its capacity requirements. Also, the company has elected to use its U.S. fab for more specialty devices and technologies to meet the more diversified needs of the U.S. market and its customers.

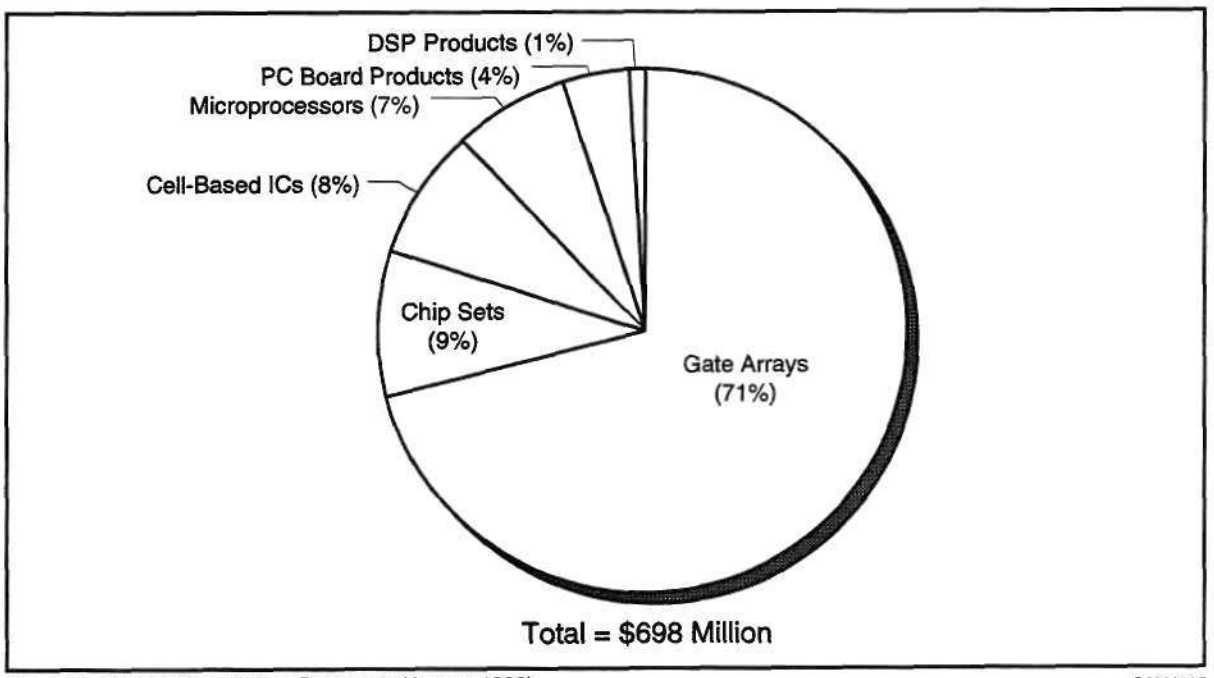
In making this move, Headland Technology, a subsidiary that makes PC chip sets, will be pulled into the corporation and treated as a product line instead of a standalone company. This is a wise and overdue move because of the cost-competitive nature of this business. Chips & Technologies and VLSI Technology have also suffered financially from the cost-cutting nature of this PC chip set market.

Product Strategy

LSI Logic's product strategy is aimed at helping system designers define, modify, and differentiate their products. ASICs including gate arrays and cell-based ICs (CBICs) are a key element of this strategy. Figure 1 shows LSI Logic's 1991 product mix; Table 3 shows its five-year revenue history, by product.

This profile will look at gate arrays, cell-based ICs, and chip sets. LSI Logic also manufactures 32-bit MIPS and SPARC RISC microprocessors. These devices will be covered in a later publication.

Figure 1
LSI Logic 1991 Sales by Product



Source: LSI Logic Corporation, Dataquest (August 1992) G2000465

Table 3
Five-Year Revenue by Product (Millions of Dollars)

Product	1987	1988	1989	1990	1991
MOS/BiCMOS Gate Array	251	332	420	464	497
MOS/BiCMOS Cell-Based ICs	11	24	37	43	58
Microprocessors	0	0	19	34	45
Microperipherals	0	18	45	55	60
DSP Products	0	0	3	4	10
Others	0	5	23	55	28
Total	262	379	547	655	698

Source: Dataquest (August 1992)

Gate Array

LSI Logic is focusing on high-density/high-performance gate arrays targeted primarily toward the electronic data processing, telecommunications, consumer, and military/aerospace industries. LSI Logic was the first ASIC supplier to introduce a new generation of gate arrays based on a 0.60-micron drawn (0.45-micron effective) CMOS process with up to 500,000 usable gates.

Low-density CMOS gate arrays (less than 10,000 gates) during the past eight years took a sharp price drop from 1 cent a gate in 1984 to today's 0.06 cents a gate. Thus margins are very thin. Over the years, LSI Logic has managed to shift the bulk of its design-wins from the low-complexity devices to higher-density devices where margins are much higher because of less competition.

Table 4 shows key gate array products offered by LSI Logic.

Cell-Based ICs

LSI Logic was founded as a gate array company but has since established itself as a viable supplier of cell-based IC products. When comparing cell-based ICs to gate arrays, cell-based ICs offer higher integration and higher performance. LSI Logic recognized the importance of such a product in the high-performance application markets it participates in and quickly developed a competitive cell-based product line.

In April 1992, LSI Logic announced the industry's first cell-based IC product line based on a 0.6-micron drawn CMOS process with up to 600,000 gates. Table 5 shows a summary of LSI Logic's cell-based IC product offering.

Table 4
LSI Logic Gate Arrays

Product	Drawn Gate Length	Usable Gate Count
LCA 300K Embedded Array	0.6-Micron	500,000
LCA 300K Compacted Array	0.6-Micron	500,000
LCA 200K Compacted Array Turbo	0.7-Micron	200,000
LFT 150K Fastest Array	1.0-Micron	80,000
LCA 100K Embedded Array	1.0-Micron	150,000
LCA 100K Compacted Array	1.0-Micron	100,000

Source: LSI Logic Corporation

Table 5
LSI Logic Cell-Based ICs

Product	Drawn Gate Length	Usable Gate Count
LCB 300K Series	0.6-Micron	600,000
LCB007 Series	1.0-Micron	200,000
LCB15 Series	1.5-Micron	100,000

Source: LSI Logic Corporation

Chip Sets

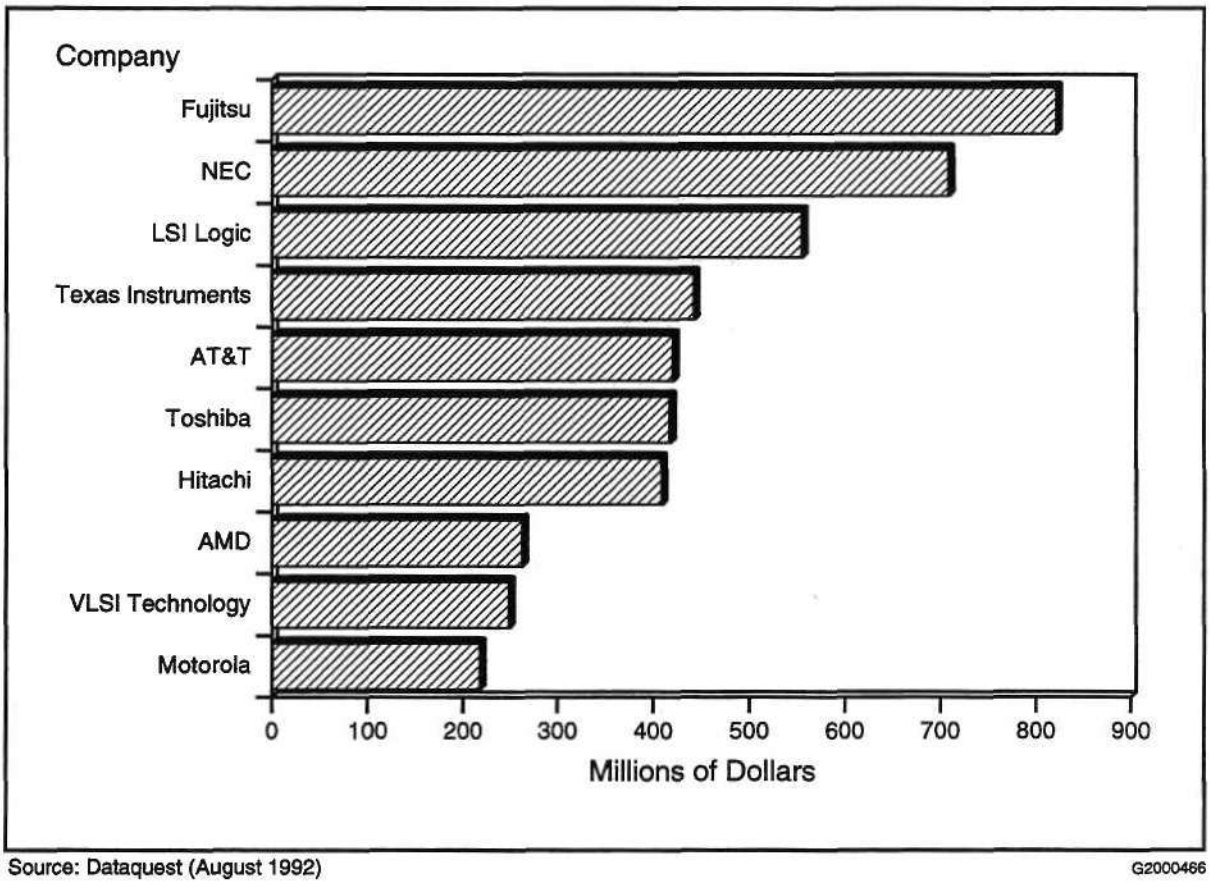
Through its Headland Technology subsidiary, LSI Logic has been supplying PC chip sets and graphics boards to the market. Its position in PC chip sets has been a weak one, with VLSI Technology the leading manufacturer. It is our estimate that Headland Technology in 1991 had about 5 percent of this market and VLSI Technology had 21 percent or four times Headland's position. LSI Logic's Video Seven subsidiary manufactured and sold the graphics boards, and its revenue in 1991 was an estimated $30 million.

Market Position

LSI Logic was the No. 3 worldwide ASIC supplier (trailing Fujitsu and NEC) and the No. 1 MOS gate array supplier in 1991. However, a large portion of Fujitsu and NEC sales are to internal divisions. Excluding sales to internal divisions, LSI Logic is the No. 1 worldwide merchant ASIC supplier.

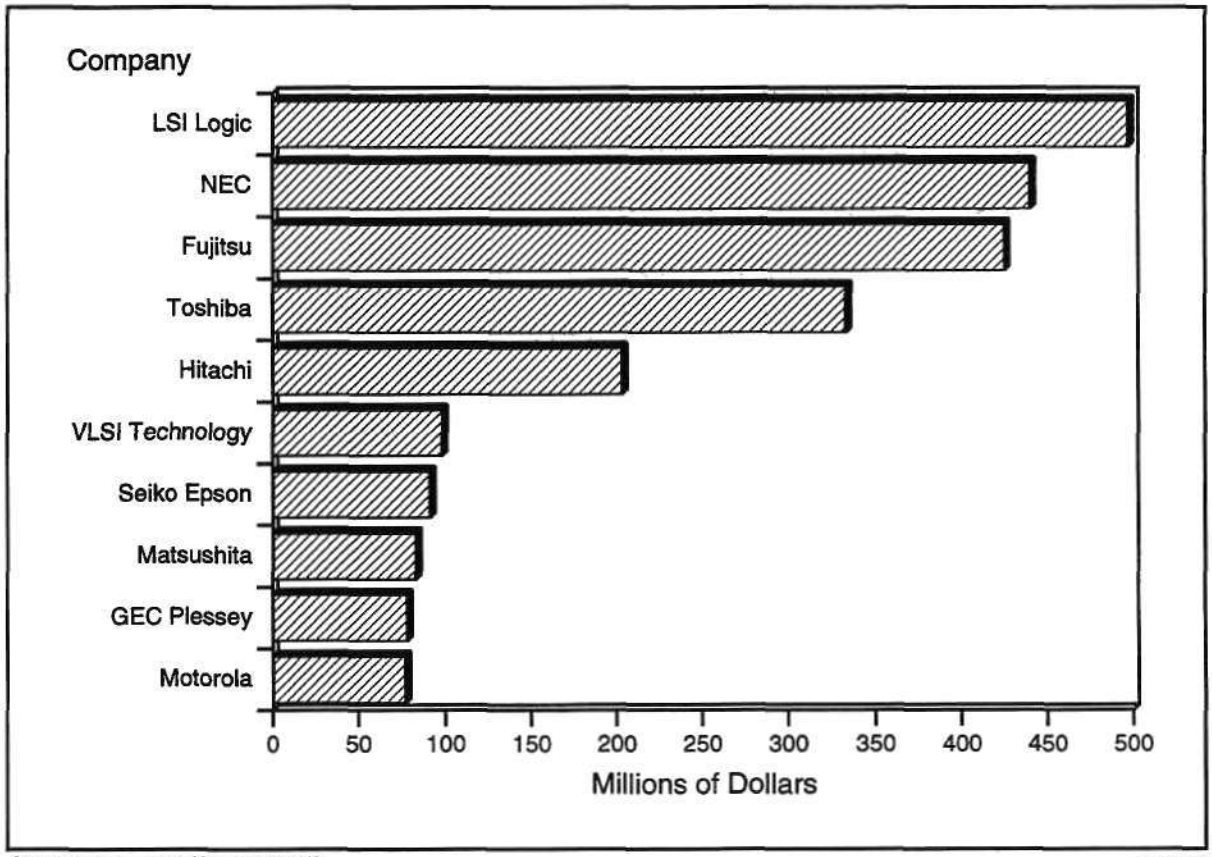
Figure 2 shows the 1991 top 10 worldwide ASIC suppliers. Figure 3 shows the hotly contested top 10 MOS gate array suppliers and their 1991 final revenue estimates.

Figure 2
Final 1991 Top 10 Worldwide ASIC Suppliers



Source: Dataquest (August 1992) G2000466

Figure 3
Final 1991 Top Worldwide MOS/BiCMOS Gate Array Suppliers



Source: Dataquest (August 1992) G2000467

Competition

The leading ASIC suppliers shown in Figure 2 and Figure 3 can be grouped into three basic categories, as follows:

- Vertically integrated system suppliers that manufacture ASICs (that is, Fujitsu, NEC, Toshiba, and AT&T)
- Broad-based semiconductor suppliers that manufacture ASICs (that is, Texas Instruments and Motorola)
- Focused ASIC manufacturers with fabs (that is, LSI Logic and VLSI Technology)

Vertically integrated system suppliers use ASIC technology as a competitive weapon for internal system design. This type of supplier wields a powerful advantage over other ASIC suppliers in the merchant ASIC market for two reasons. First, large vertically integrated system suppliers typically boast the most efficient manufacturing, which stems from economies of scale in manufacturing. In short, they have both large internal and merchant consumption, which enables

greater amortization of development costs. Furthermore, they are often broad-based semiconductor suppliers, which provides an added advantage in allowing them to amortize their manufacturing costs across standard products as well as ASICs. This clearly gives them a highly competitive cost structure. Second, they have a large amount of in-house system expertise available to develop advanced ASIC cell libraries. In our view, these suppliers are well positioned to capitalize on the merchant ASIC market.

Broad-based semiconductor suppliers, however, develop ASICs to defend their semiconductor business. They have a cost structure that is somewhat less imposing because manufacturing costs can be amortized across both standard products (for example, DRAMs) and ASICs. However, they do not have the internal consumption necessary to reduce their merchant manufacturing cost structure. Therefore, their cost structure is typically less favorable than that of vertically integrated suppliers, but more favorable than that of focused ASIC suppliers with fabs.

Focused ASIC suppliers with fabs are in the most difficult position. They must find ways to maintain fab capacity to achieve a profitable cost structure as well as invest in the following areas:

- Development of next-generation manufacturing processes
- Development of next-generation products
- Development of dedicated macrocell libraries
- Development of a competitive EDA environment

As with ASICs or any other device of the semiconductor industry, the main goal in having a manufacturing facility with fab, assemble, and test is to keep all parts of the process running at full capacity. Concerning LSI Logic's assembly and test (A&T) operation in Germany, this has surely not been the case. It was originally planned to support the computer industry in Europe, and the goal was for it to reach high levels of efficiency. The hard reality is that the computer market in Germany and other parts of Europe has been in a recession for two years and this facility became a very expensive operation. This will not be an easy one to unload, because there is significant excess A&T capacity in Europe and the Asians have far lower cost structures.

LSI Logic's new fab strategy of exercising its soon-to-be-completed joint venture fab with Kawasaki Steel is a smart one, but it will test the communications and planning skills of the senior production management based in Milpitas. Also, LSI Logic now plans to utilize foundries and other partnerships to fill gaps in capacity.

In our view, partnerships are extremely critical for focused ASIC suppliers that have fabs. They typically do not have the R&D budgets required to develop all the areas of concern, such as the next-generation processes. Even more problematic, the cost of a state-of-the-art fab continues to rise at an increasing rate. A complete 0.8-micron diffusion ASIC fab costs about $200 million, requiring very high volume production to support it.

Dataquest Perspective

Consistent profitability is clearly a challenging goal for LSI Logic. With the U.S. economy struggling through a slow recovery and the Japan economy in a severe recession, the challenge is even greater.

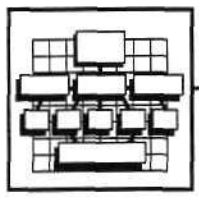
In our view, the No. 1 problem that LSI Logic must solve to achieve consistent profitability is reshaping its long-term manufacturing cost model. Clearly it has taken some bold steps with its August 21 release. Although LSI Logic has a strong product offering, it does not have the economies of scale required to remain cost-competitive considering the competition and the rising costs associated with state-of-the-art fabs.

Even though management has taken significant steps to reduct costs and redirect its strategic direction, we believe that LSI Logic still has to drive costs lower until it has its new joint venture fab completed in 1993. But in the meantime current costs are too high and geometries are too large to successfully compete with the likes of NEC and Fujitsu.

LSI Logic must move quickly to establish the other partnerships required to compete in the future. LSI Logic has a strong bargaining position when forming these alliances because it has much to offer, including the following:

- Competitive proprietary CAD tools
- Robust dedicated cell libraries
- Solid test and packaging capabilities
- Large customer base
- Very experienced fab partner in Kawasaki Steel

Dataquest believes that LSI Logic has a good understanding of the issues it faces and has made short- and long-term moves toward improving profitability. Wilf Corrigan's track record demonstrates that once he sets his sights on an objective and becomes personally involved—and stays involved—success is achieved.



Dataquest Vendor Profile

ASICs *Worldwide*

August 31, 1992

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(Thousands of U.S. Dollars)

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Percentage of Revenue	11.03	9.76	0.01	9.18	11.58
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Quarterly Revenue and Earnings History
(Thousands of U.S. Dollars)

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- Closing a noncompetitive factory in the United Kingdom
- Discontinuing wafer manufacturing in Canada
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Then, on August 21, 1992, LSI Logic management announced that it will take a restructuring charge in the range of $95 million to $110 million that it estimates will result in a net loss of more than $100 million, or more than $2 per share, in the third quarter ended September 27, 1992. These charges include costs associated with the following:

- The phaseout of the company's Braun-schweig, Germany assembly and test operation
- The write-down of certain U.S. manufacturing assets
- The inventory related to certain discontinued commodity products
- The write-off of certain U.S. manufacturing assets made redundant through a strategic consolidation of the company's manufacturing operations
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- Miscellaneous other costs

If executed properly, these timely actions will position the company to compete more profitably in the very competitive ASIC business.

Further, LSI Logic is another in the long list of ASIC manufacturers to realize that it must depend more on its Japanese facilities for high volume and utilize foundry services to fill voids in its capacity requirements. Also, the company has elected to use its U.S. fab for more specialty devices and technologies to meet the more diversified needs of the U.S. market and its customers.

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Product Strategy

LSI Logic's product strategy is aimed at helping system designers define, modify, and differentiate their products. ASICs including gate arrays and cell-based ICs (CBICs) are a key element of this strategy. Figure 1 shows LSI Logic's 1991 product mix; Table 3 shows its five-year revenue history, by product.

This profile will look at gate arrays, cell-based ICs, and chip sets. LSI Logic also manufactures 32-bit MIPS and SPARC RISC microprocessors. These devices will be covered in a later publication.

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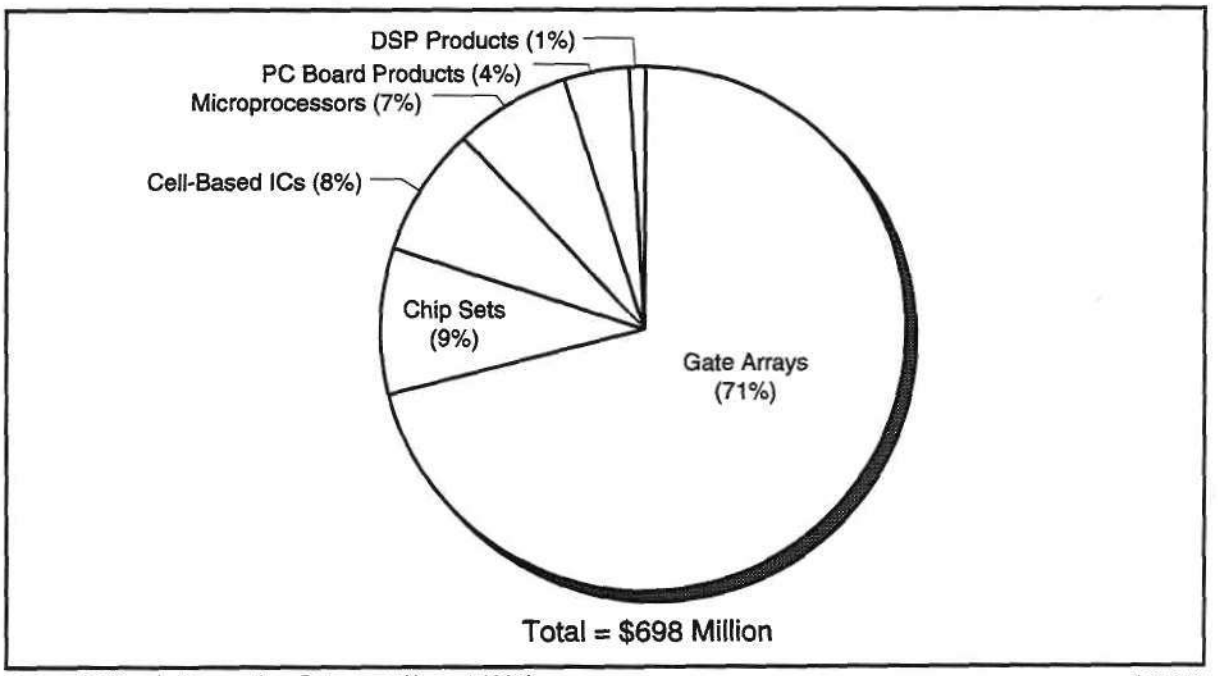

Source: LSI Logic Corporation, Dataquest (August 1992) G2000465

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Microprocessors	0	0	19	34	45
Microperipherals	0	18	45	55	60
DSP Products	0	0	3	4	10
Others	0	5	23	55	28
Total	262	379	547	655	698

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Gate Array

LSI Logic is focusing on high-density/high-performance gate arrays targeted primarily toward the electronic data processing, telecommunications, consumer, and military/aerospace industries. LSI Logic was the first ASIC supplier to introduce a new generation of gate arrays based on a 0.60-micron drawn (0.45-micron effective) CMOS process with up to 500,000 usable gates.

Low-density CMOS gate arrays (less than 10,000 gates) during the past eight years took a sharp price drop from 1 cent a gate in 1984 to today's 0.06 cents a gate. Thus margins are very thin. Over the years, LSI Logic has managed to shift the bulk of its design-wins from the low-complexity devices to higher-density devices where margins are much higher because of less competition.

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Cell-Based ICs

LSI Logic was founded as a gate array company but has since established itself as a viable supplier of cell-based IC products. When comparing cell-based ICs to gate arrays, cell-based ICs offer higher integration and higher performance. LSI Logic recognized the importance of such a product in the high-performance application markets it participates in and quickly developed a competitive cell-based product line.

In April 1992, LSI Logic announced the industry's first cell-based IC product line based on a 0.6-micron drawn CMOS process with up to 600,000 gates. Table 5 shows a summary of LSI Logic's cell-based IC product offering.

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Chip Sets

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Market Position

LSI Logic was the No. 3 worldwide ASIC supplier (trailing Fujitsu and NEC) and the No. 1 MOS gate array supplier in 1991. However, a large portion of Fujitsu and NEC sales are to internal divisions. Excluding sales to internal divisions, LSI Logic is the No. 1 worldwide merchant ASIC supplier.

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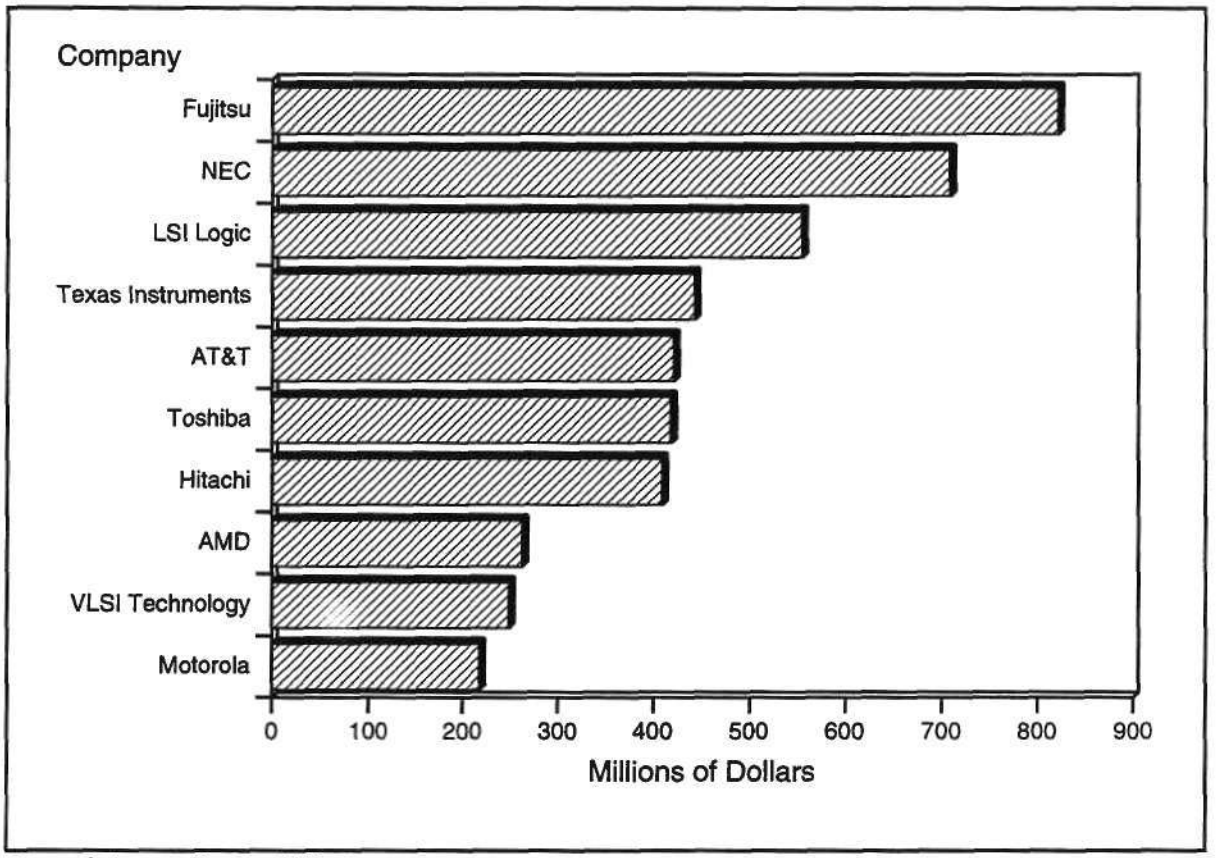
Final 1991 Top 10 Worldwide ASIC Suppliers



Source: Dataquest (August 1992)

G2000466

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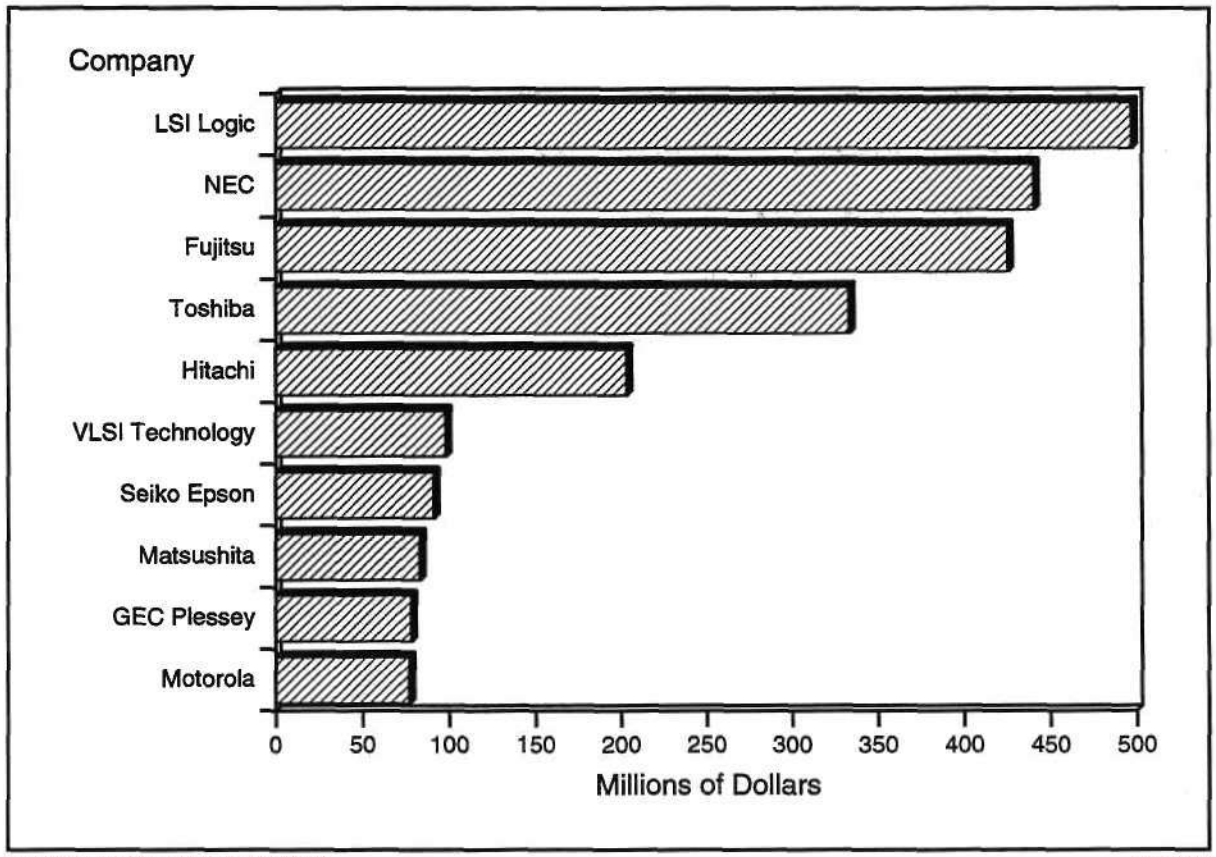

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Competition

The leading ASIC suppliers shown in Figure 2 and Figure 3 can be grouped into three basic categories, as follows:

- Vertically integrated system suppliers that manufacture ASICs (that is, Fujitsu, NEC, Toshiba, and AT&T)
- Broad-based semiconductor suppliers that manufacture ASICs (that is, Texas Instruments and Motorola)
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Vertically integrated system suppliers use ASIC technology as a competitive weapon for internal system design. This type of supplier wields a powerful advantage over other ASIC suppliers in the merchant ASIC market for two reasons. First, large vertically integrated system suppliers typically boast the most efficient manufacturing, which stems from economies of scale in manufacturing. In short, they have both large internal and merchant consumption, which enables

greater amortization of development costs. Furthermore, they are often broad-based semiconductor suppliers, which provides an added advantage in allowing them to amortize their manufacturing costs across standard products as well as ASICs. This clearly gives them a highly competitive cost structure. Second, they have a large amount of in-house system expertise available to develop advanced ASIC cell libraries. In our view, these suppliers are well positioned to capitalize on the merchant ASIC market.

Broad-based semiconductor suppliers, however, develop ASICs to defend their semiconductor business. They have a cost structure that is somewhat less imposing because manufacturing costs can be amortized across both standard products (for example, DRAMs) and ASICs. However, they do not have the internal consumption necessary to reduce their merchant manufacturing cost structure. Therefore, their cost structure is typically less favorable than that of vertically integrated suppliers, but more favorable than that of focused ASIC suppliers with fabs.

Focused ASIC suppliers with fabs are in the most difficult position. They must find ways to maintain fab capacity to achieve a profitable cost structure as well as invest in the following areas:

- Development of next-generation manufacturing processes
- Development of next-generation products
- Development of dedicated macrocell libraries
- Development of a competitive EDA environment

As with ASICs or any other device of the semiconductor industry, the main goal in having a manufacturing facility with fab, assemble, and test is to keep all parts of the process running at full capacity. Concerning LSI Logic's assembly and test (A&T) operation in Germany, this has surely not been the case. It was originally planned to support the computer industry in Europe, and the goal was for it to reach high levels of efficiency. The hard reality is that the computer market in Germany and other parts of Europe has been in a recession for two years and this facility became a very expensive operation. This will not be an easy one to unload, because there is significant excess A&T capacity in Europe and the Asians have far lower cost structures.

LSI Logic's new fab strategy of exercising its soon-to-be-completed joint venture fab with Kawasaki Steel is a smart one, but it will test the communications and planning skills of the senior production management based in Milpitas. Also, LSI Logic now plans to utilize foundries and other partnerships to fill gaps in capacity.

In our view, partnerships are extremely critical for focused ASIC suppliers that have fabs. They typically do not have the R&D budgets required to develop all the areas of concern, such as the next-generation processes. Even more problematic, the cost of a state-of-the-art fab continues to rise at an increasing rate. A complete 0.8-micron diffusion ASIC fab costs about $200 million, requiring very high volume production to support it.

Dataquest Perspective

Consistent profitability is clearly a challenging goal for LSI Logic. With the U.S. economy struggling through a slow recovery and the Japan economy in a severe recession, the challenge is even greater.

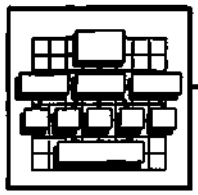
In our view, the No. 1 problem that LSI Logic must solve to achieve consistent profitability is reshaping its long-term manufacturing cost model. Clearly it has taken some bold steps with its August 21 release. Although LSI Logic has a strong product offering, it does not have the economies of scale required to remain cost-competitive considering the competition and the rising costs associated with state-of-the-art fabs.

Even though management has taken significant steps to reduct costs and redirect its strategic direction, we believe that LSI Logic still has to drive costs lower until it has its new joint venture fab completed in 1993. But in the meantime current costs are too high and geometries are too large to successfully compete with the likes of NEC and Fujitsu.

LSI Logic must move quickly to establish the other partnerships required to compete in the future. LSI Logic has a strong bargaining position when forming these alliances because it has much to offer, including the following:

- Competitive proprietary CAD tools
- Robust dedicated cell libraries
- Solid test and packaging capabilities
- Large customer base
- Very experienced fab partner in Kawasaki Steel

Dataquest believes that LSI Logic has a good understanding of the issues it faces and has made short- and long-term moves toward improving profitability. Wilf Corrigan's track record demonstrates that once he sets his sights on an objective and becomes personally involved—and stays involved—success is achieved.



Dataquest Vendor Profile

ASICs *Worldwide*

August 31, 1992

LSI Logic Corporation

Corporate Statistics

Location	Milpitas, California
Chairman and CEO	Wilfred Corrigan
Number of Employees	4,000
1991 Revenue	$697.8 Million
1991 Net Income	$8.3 Million
Founded	1981
Telephone	(408) 433-8000
Fax	(408) 434-6457

LSI Logic designs, develops, manufactures, and markets integrated circuits (ICs) based on application-specific integrated circuit (ASIC) technology. The company's key product lines are ASICs, which include gate arrays and cell-based ICs; 32-bit SPARC and MIPS RISC microprocessors and peripherals; and application-specific standard products (ASSPs) consisting of PC logic chip sets and graphics products used in IBM-compatible computers. LSI Logic's products and services are marketed primarily to manufacturers in the electronic data processing, military/aerospace, telecommunications, and consumer electronic industries.

Profitability: The Key to Success

Chairman and Chief Executive Officer Wilfred Corrigan states in the 1991 LSI Logic annual report that improving profitability is the company's No. 1 goal. Although LSI Logic has consistently increased annual revenue and has been a driving force in high-performance electronic system design, it has not achieved consistent profitability. Profits have been especially elusive over the last three years. There were net losses of $31.2 million in 1989 and $30.3 million in 1990, and a marginal gain of $8.3 million in 1991. See Tables 1 and 2 for corporate financial highlights and quarterly revenue and earnings history.

Mr. Corrigan is a man of action and is no stranger to solving tough problems. As 1991 progressed, Mr. Corrigan stated, "...it became increasingly clear that we needed to reshape our long-term financial

For more information on LSI Logic Corporation or the ASICs industry, call Bryan Lewis at (408) 437-8668

Dataquest
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ASIC-SEG-VP-9201

Table 1
Five-Year Corporate Highlights
(Thousands of U.S. Dollars)

	1987	1988	1989	1990	1991
Five-Year Revenue	262,131	378,908	546,870	655,491	697,838
Percentage Change	-	44.55	44.33	19.86	6.46
Capital Expenditure	138,993	100,961	114,494	61,998	73,650
Percentage of Revenue	53.02	26.65	20.94	9.46	10.55
R&D Expenditure	28,919	36,964	52,457	60,196	80,802
Percentage of Revenue	11.03	9.76	0.01	9.18	11.58
Number of Employees	2,322	3,329	3,700	4,400	4,000
Revenue ($K)/Employee	112.89	113.82	147.80	148.98	174.46
Net Income	11,340	19,362	-31,254	-30,316	8341
Percentage Change	-	70.74	-261.42	3.00	127.51

Source: Dataquest (August 1992)

Table 2
Quarterly Revenue and Earnings History
(Thousands of U.S. Dollars)

1991/1992 Calendar Years	Q1/91	Q2/91	Q3/91	Q4/91	Q1/92	Q2/92
Revenue	180,243	180,961	172,352	164,282	150,521	151,836
Net Income	2,074	5,654	5,600	-43,654	309	-5,854

Source: Dataquest (August 1992)

model to be more consistent with changing trends in the industry. The computer industry spent much of 1991 adjusting to lower process and tighter cost controls. We had to make adjustments ourselves. We had to be leaner, more productive, more responsive, and consistently profitable. There were no alternatives."

LSI Logic took action—of both short- and long-term nature—during 1991 to improve profitability. Such action lowered the company's break-even point by about 15 percent. Cost-cutting measures taken included the following:

- Reducing the work force
- Forcing vacations during slow periods
- Delaying pay increases
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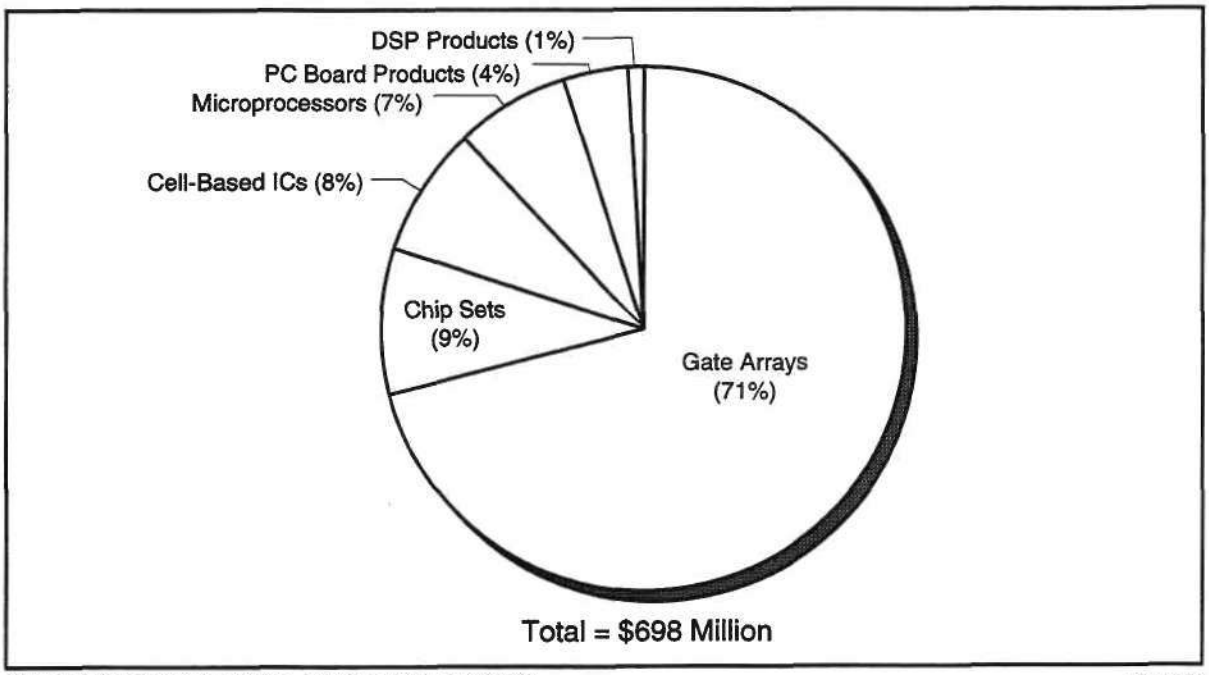

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Cell-Based ICs

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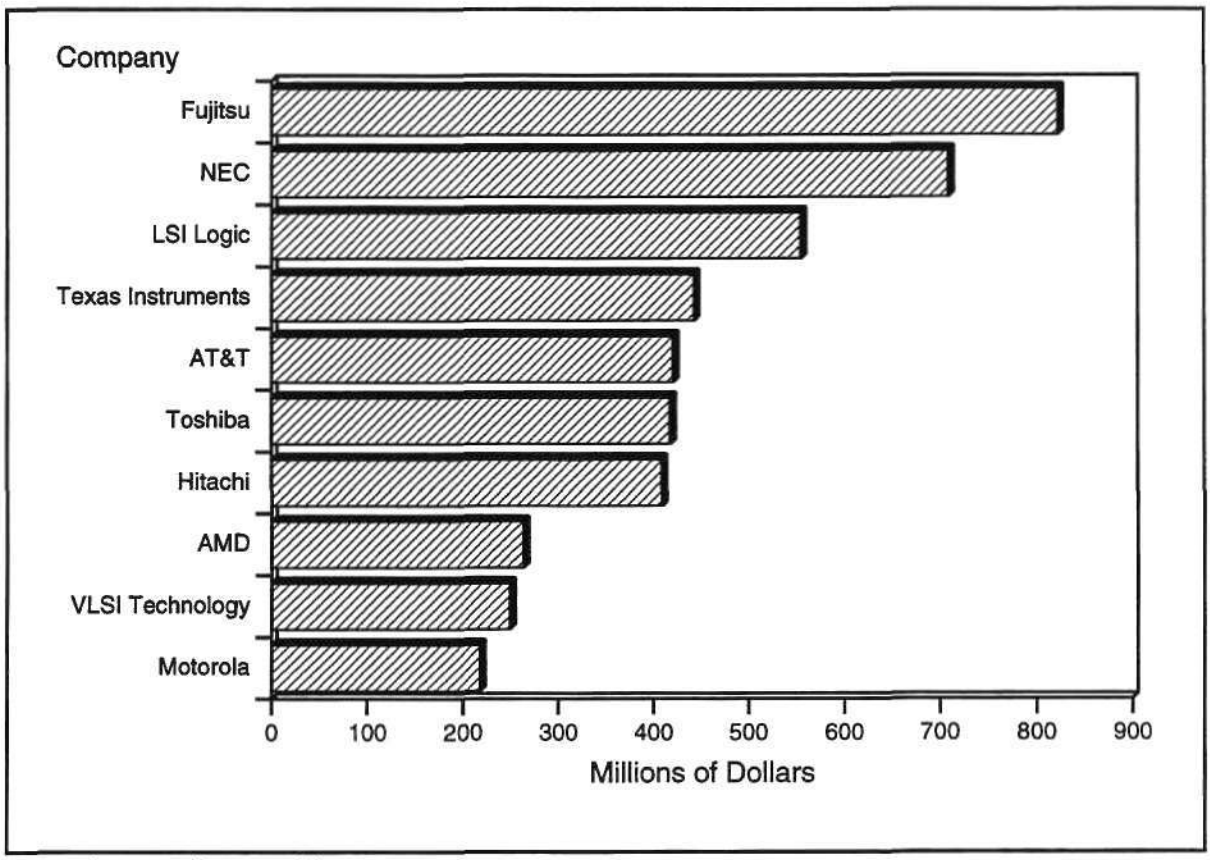

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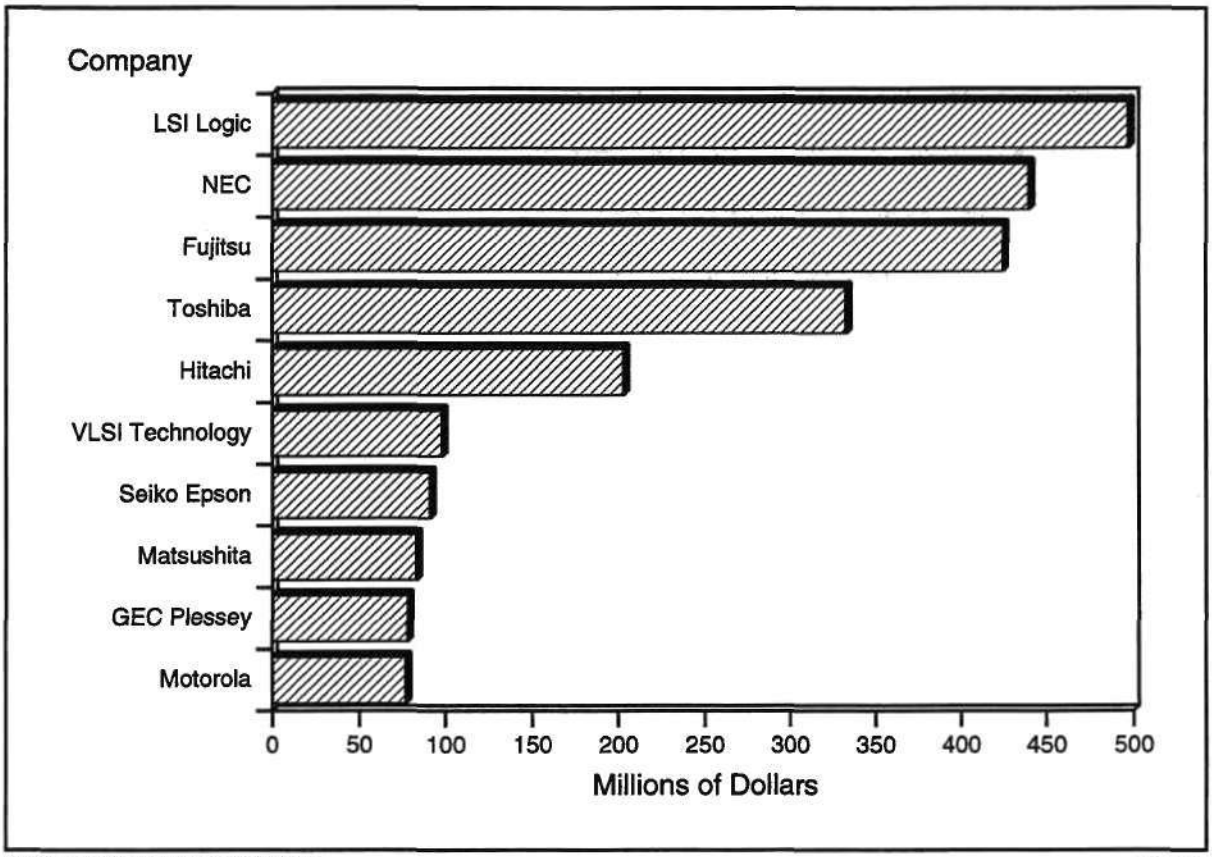

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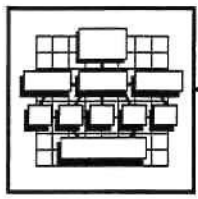

Dataquest Vendor Profile

ASICs *Worldwide*

December 21, 1992

Cadence Design Systems Inc.

Corporate Statistics

Location	San Jose, California
President and CEO	Joseph B. Costello
Number of Employees	2,500
1991 Software Revenue*	$292.8 million
1991 Corporate Revenue*	$392.3 million
Founded	1988
EDA Software Market Share*	24.2 percent
Strongest Competitor	Mentor Graphics

*Adjusted to include Valid revenue

Corporate Overview

Vision is the art of seeing things invisible.
—Cover of Cadence Annual Report, 1991

Cadence Design Systems Inc. develops, markets, and supports electronic design automation (EDA) software products for a variety of technical workstations. The company has a diverse offering of tools, consistent with its history as a company based upon merger and acquisition. It currently enjoys the privilege of being the largest provider of EDA software to the world.

Corporate Organization

Formed as a result of a merger between SDA Systems Inc. and ECAD in May 1988, the management structure at Cadence has been fluid over the past four years, with change being the norm. The company is currently organized along four main product thrusts: IC design, analog design, system design, and CAE tools. Yet through it all, Joseph B. Costello, President and CEO, has provided a very strong leadership presence. Figure 1 outlines the Cadence organizational structure.

Cadence is a company formed by mergers, as shown in Figure 2. While retaining the Cadence name since 1988, the company is in fact an amalgamation of diverse EDA companies formed in the early

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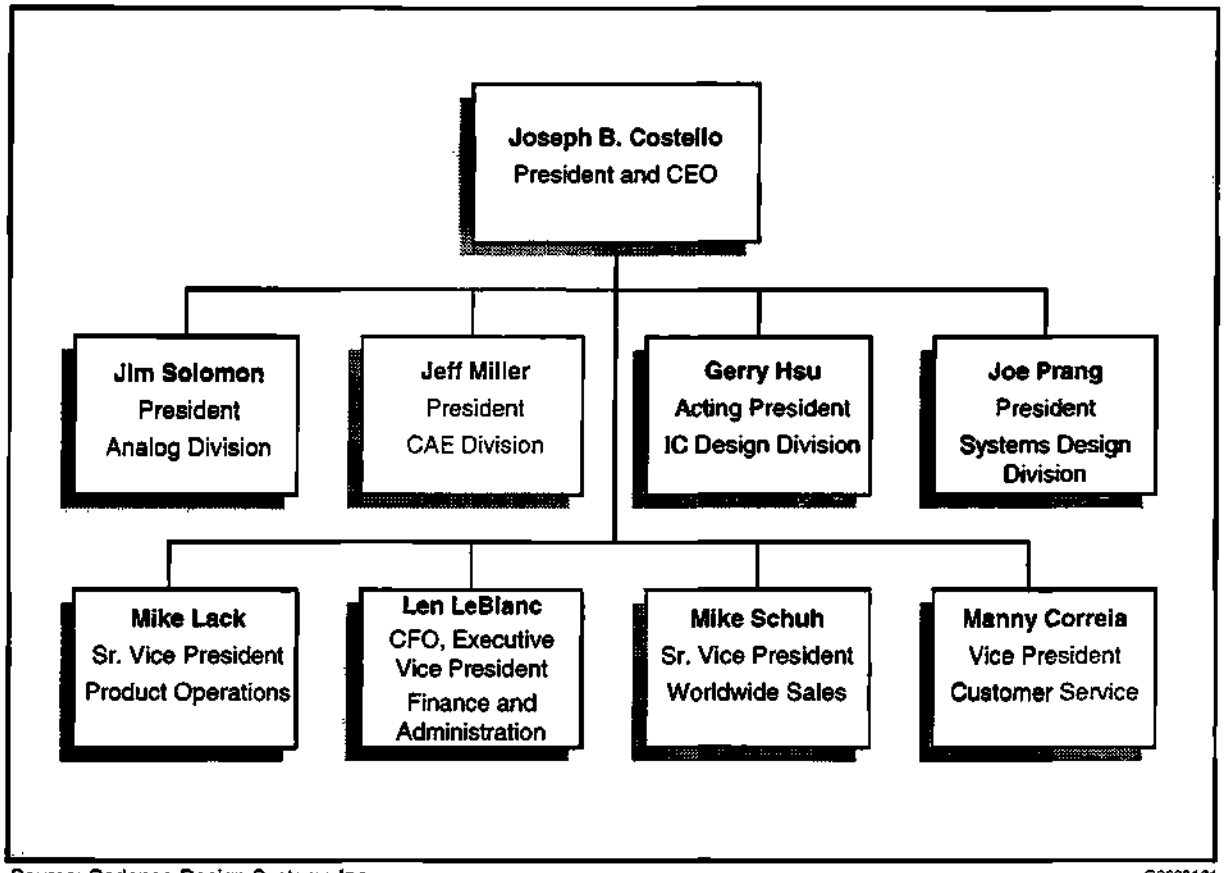
ASIC-SEG-VP-9202

Figure 1
Cadence Corporate Organization



Source: Cadence Design Systems Inc. G2002161

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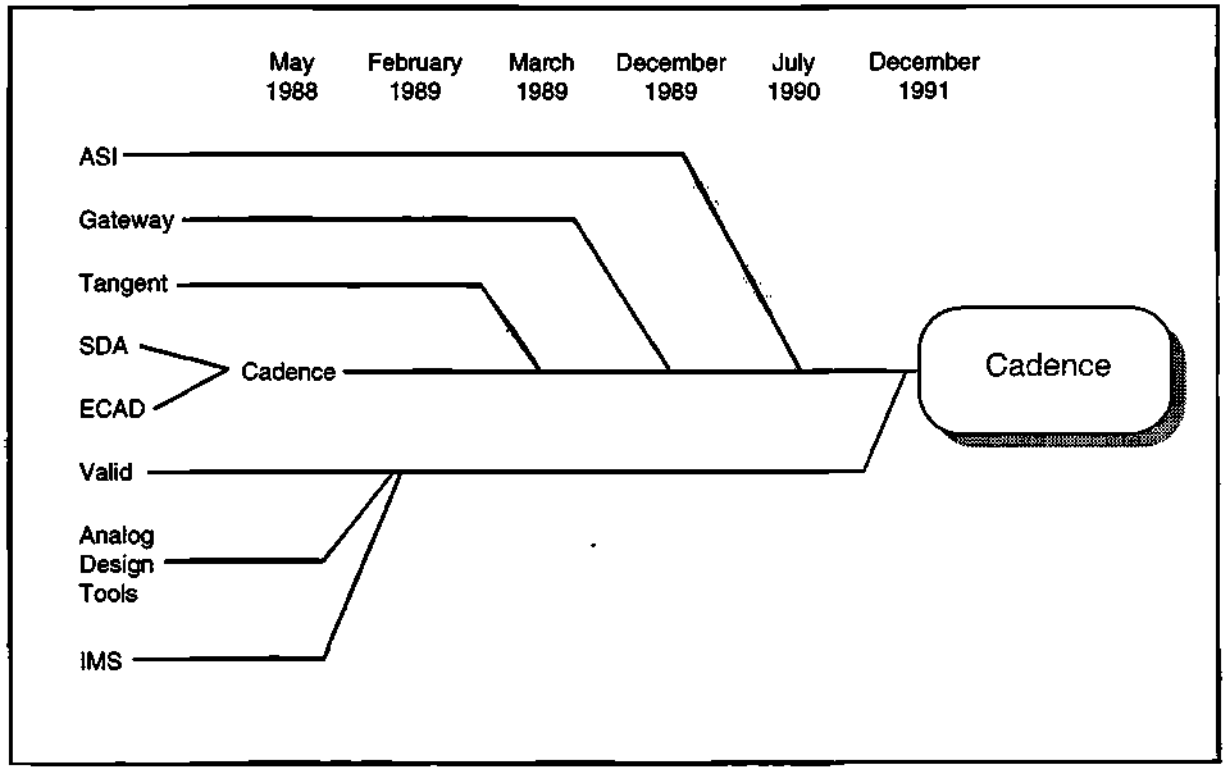

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Jeffrey A. Miller is the president of the Computer-Aided Engineering (CAE) Division. With a classic combination of B.S.E.E. and M.B.A. credentials, Miller arrived at Cadence shortly before the merger with Valid. He previously had been general manager of storage products at computer subsystem supplier Adaptec.

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Source: Dataquest (December 1992)

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Verilog-XL	Mixed-level simulation
VHDL-XL	Mixed-level simulation
Veritime-XL	Static timing analysis
Verifault-XL	Fault Simulation

Source: Dataquest (December 1992)

Table 3
Cadence's PCB Design Products

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SigNoise	PCB/MCM signal integrity analysis
Viable	PCB/MCM reliability analysis
Prance-XL	PCB/MCM autorouting
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Cadence is currently the largest supplier of electronic design automation tools. Dataquest estimates that its 1991 software revenue was $184.3 million, as shown in Table 4. However, this figure is based upon premerger conditions. With the addition of Valid's $108.5 million, Cadence's total software revenue is $292.8 million.

By becoming the largest supplier of EDA tools, Cadence has unseated its strongest rival, Mentor Graphics. Mentor Graphics was one of the pioneering companies of EDA, and the only standalone entity left from the boom years of the big three: Daisy, Mentor, and Valid. Table 5 depicts the "tale of the tape" for these two EDA giants. In 1991, both Cadence and Mentor Graphics lost money. Cadence's loss was because of write-downs from merger costs, and Mentor Graphics' problems stemmed from layoffs and restructuring. However, 1992 has seen Cadence's profits improve compared to last year, and the company seems to be on track to break its revenue number of last year. Mentor Graphics, conversely, is still struggling with product transitions, downsizing, and loss of revenue due to its dwindling hardware sales.

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1991 EDA Software Market Share

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1991 Profit	-21.7	-61.6
1991 Software Revenue	292.8	146.4
1991 Service Revenue	88.1	135.9
1991 Hardware Revenue	5.1	113.8
Q1 1992 Corporate Revenue	101.3	100.1
Q2 1992 Corporate Revenue	105.9	89.0

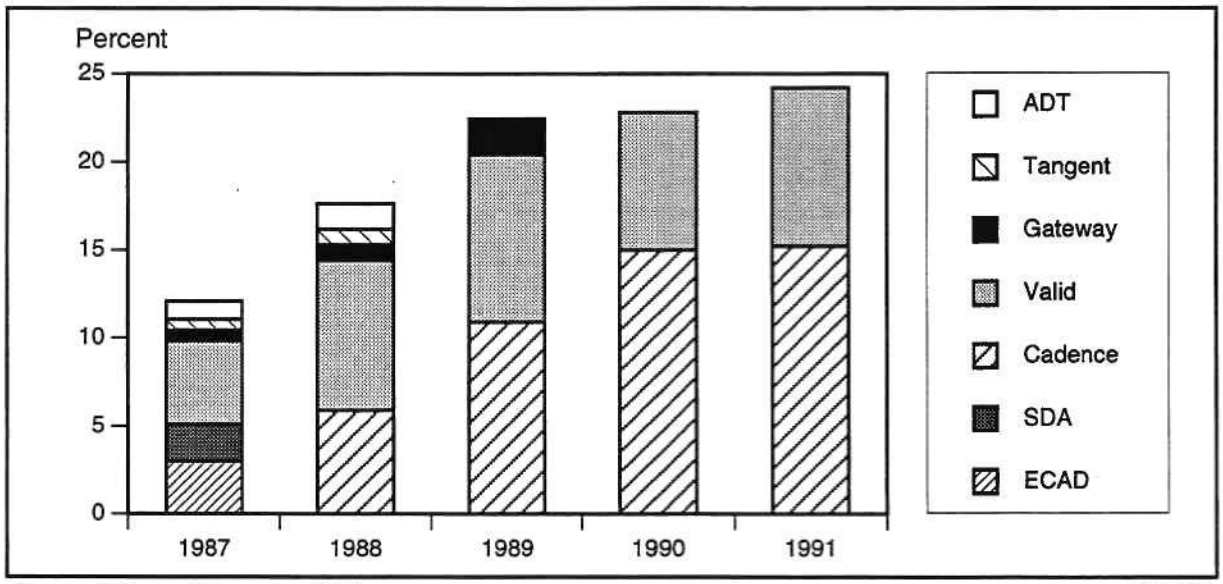
Source: Cadence, Mentor Graphics, and Dataquest (December 1992)

IC Design Drove Cadence's Rise to Prominence

IC design was the base that Cadence worked from to penetrate the EDA market. By 1991, the combined Cadence and Valid entity garnered a whopping 62 percent of the IC layout market (see Figure 6). Cadence has very little competition in this market, with Mentor Graphics trailing Cadence/Valid by almost $87 million. It is from this position of strength in the IC layout market that Cadence had set its sights on total EDA domination.

On the downside, the IC design market has reached a saturation point. Slowing worldwide semiconductor growth, as well as the economic downturn in Japan, will further stagnate this market. However, there are shifts in the methodologies used in custom and semicustom IC design, and Cadence is well positioned to migrate with the changing user needs.

Figure 3
Worldwide EDA Software Market Share of Companies Forming Cadence



Source: Dataquest (December 1992)

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Figure 4
Cadence 1991 Worldwide Software Revenue Percent by Market

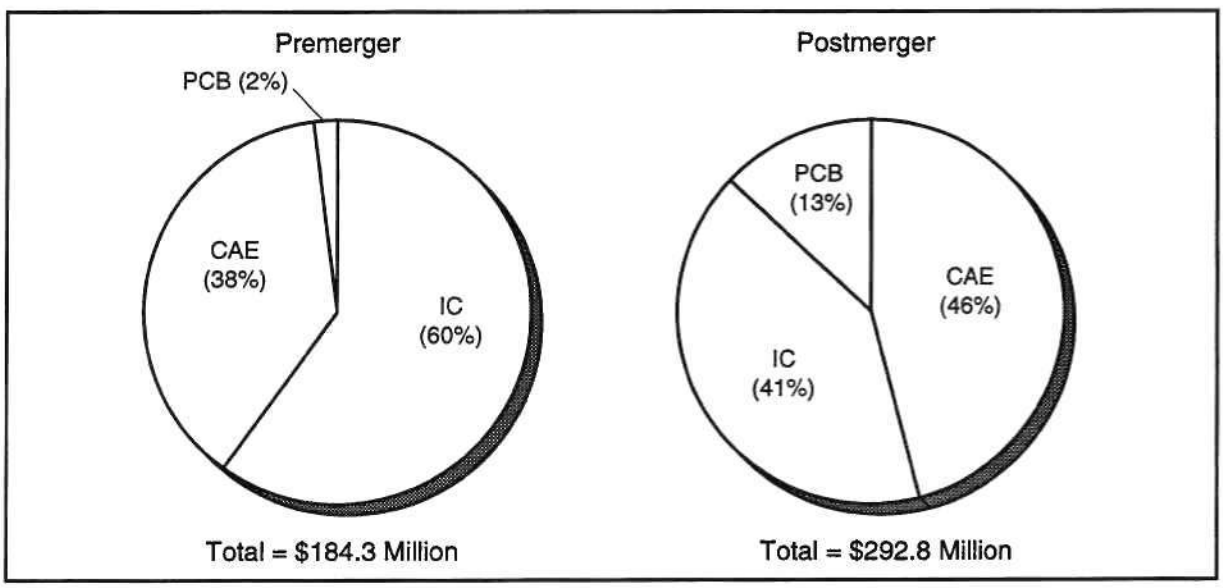

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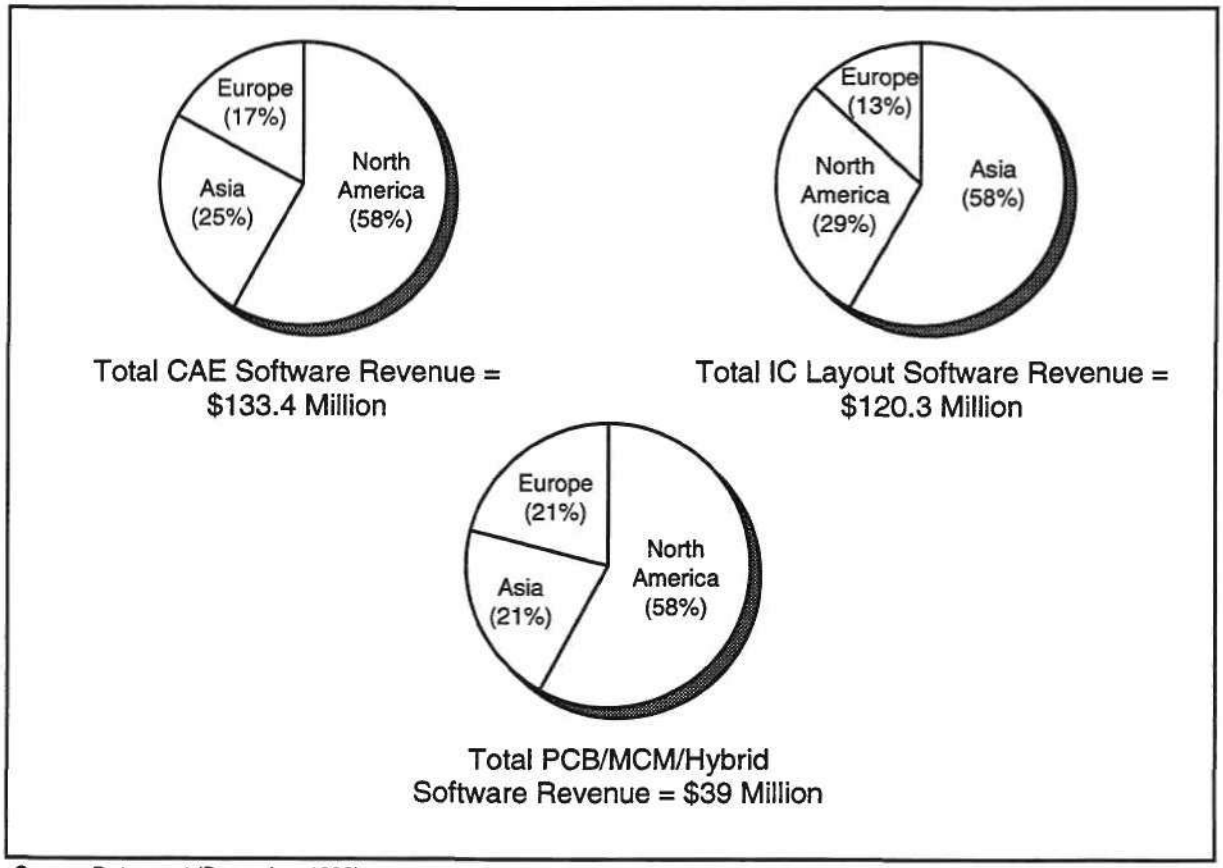
Figure 5
Combined Cadence/Valid 1991 Software Revenue by Market and Region



Source: Dataquest (December 1992) G2002165

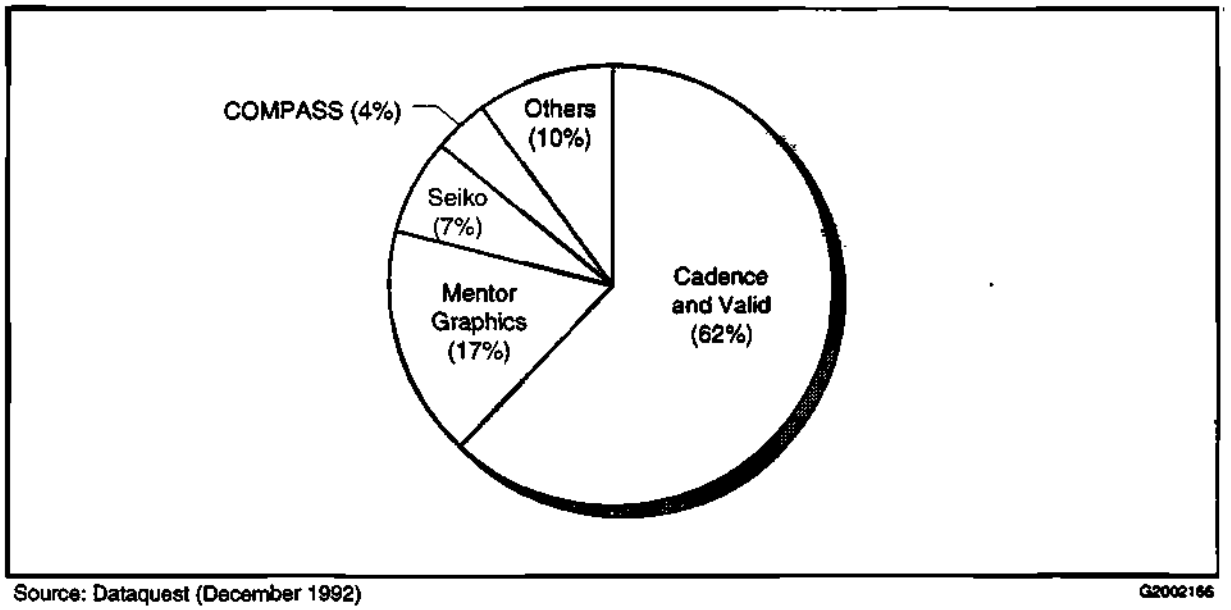
CAE Penetration Has Highs and Lows, with Verilog Leading the Way

Cadence made its big leap into the CAE market with its 1989 acquisition of Gateway Design Automation. The jewel Cadence was after was the Verilog-XL simulator, a simulator that today still is the de facto standard in mixed-level simulation. However, this powerful weapon in the Cadence arsenal has come under attack in two areas.

The first area is the emergence of the VHSIC hardware description language (VHDL). This rival hardware description language (HDL) and mixed-level simulators based upon its use have begun to erode Verilog's market share.

The second factor that will affect Verilog sales is the birth of the Verilog-clone simulation market. As part of Cadence's battle plan against VHDL, it created Open Verilog International (OVI) as an industry body to evolve the Verilog HDL into a true industry standard, as opposed to a proprietary, de facto standard. As a by-product of this effort, we are now beginning to see Verilog-based

Figure 6
1991 Worldwide IC Layout Software Market Share



Source: Dataquest (December 1992) G2002166

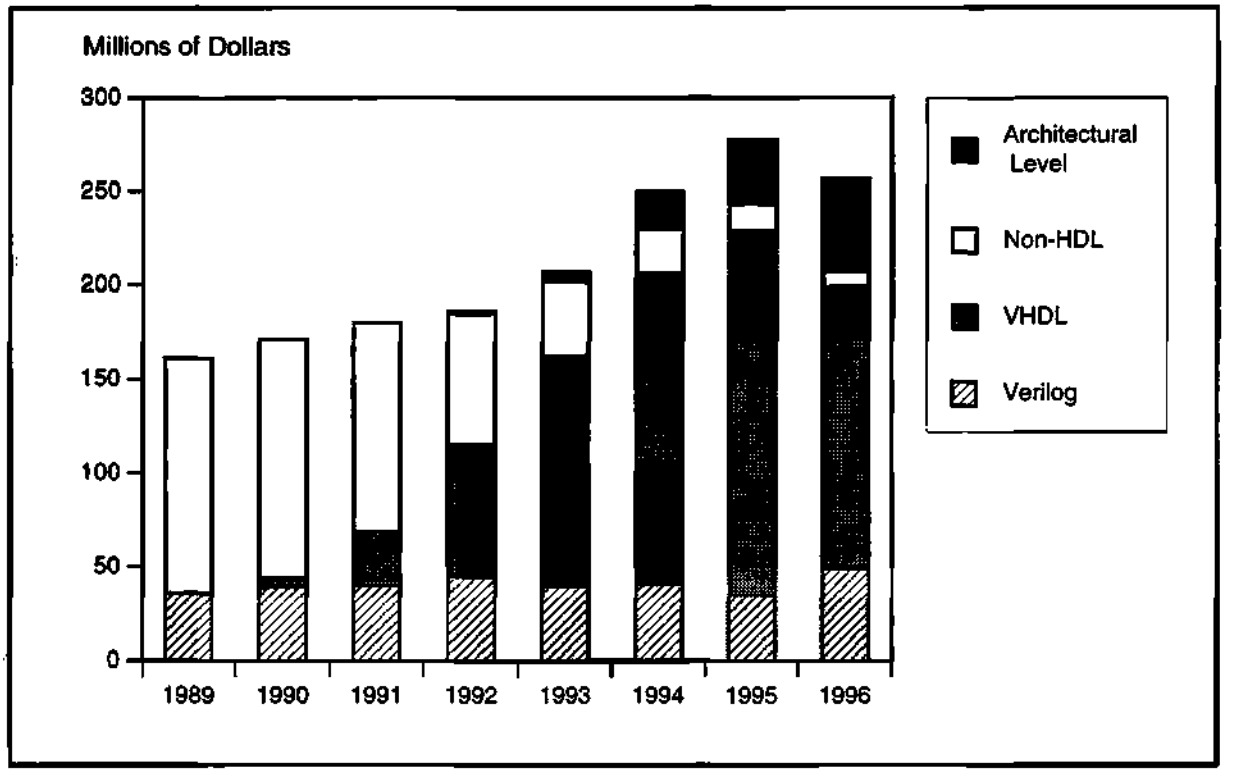
simulators from other companies. Dataquest believes that these new simulators will provide a mid-life extension to the Verilog market; however, it may also decrease the average selling prices (ASPs) of Verilog-based simulators. Based upon these factors and end-user research showing a coming tide of VHDL use, Dataquest anticipates that sales of Verilog-based simulators will stagnate over the coming years, whereas VHDL-based simulators will be more broadly accepted by the mainstream designer (see Figure 7).

Other design verification tools are critical to Cadence's future success. The company has not ignored the VHDL phenomenon and has recently announced a VHDL initiative to help standardize VHDL models for use in a variety of VHDL-based simulators—a vexing problem facing ASIC suppliers. While Cadence has had a VHDL simulator—the VHDL-XL—the product has not received the same attention that its Verilog-XL counterpart has. Look for this to change as Cadence adopts to user's demands and more fully supports VHDL.

Synthesis May Be a Weak Chink in the Cadence Armor

Logic synthesis is the pivotal point tool in the top-down design methodology that is being adopted by the mainstream electronic designer. Synopsys is the one company that has pioneered this productivity-enhancing technology. The combination of the Synopsys synthesis tool with Cadence's Verilog-XL simulator has been a favorite for ASIC designers for some time now. But Synopsys is distancing itself from Cadence, and these once-symbiotic partners now treat each other as competitors. Cadence introduced its own synthesis tools, Synergy, while Synopsys acquired a VHDL simulator from ZYCAD and is now focusing on a VHDL-based top-down

Figure 7
Historical and Projected Growth of Worldwide Software Simulation Market



Source: Dataquest (December 1992) G2002167

design to further differentiate itself from Cadence. It may be quite difficult for Cadence to gain market share in this technically demanding area of logic synthesis.

Attempting to build upon its Verilog strength, Cadence has generated its own front-end design entry system called Composer. In addition, Cadence has generated PLD design tools and other design verification tools. These products are not necessarily "lead" products that drive sales; rather they are "drag" products that are brought along to fill out the solution for the electronic designer. Cadence will look to its strength in Verilog simulation to evolve into a more potent VHDL-based CAE product offering.

PCB Design Tools Complete the Circle

To become the largest supplier of EDA tools, Cadence had the vision to seek out new areas of expansion. While it never had a presence in the printed circuit board (PCB) design area, it sought to acquire this expertise. Its first attempt was to purchase ASI, a PCB production house that had its own internal set of PCB design tools. Unfortunately this strategy proved to be unsuccessful, and after this misstep, Cadence set its sights on larger game. Cadence's weakness in PCB design tools led to its merger with Valid, which had a growing business in PCB design with its Allegro tool set. Cadence's challenge is to keep the momentum of the Allegro tool set while integrating it into the Cadence set of framework and entry tools.

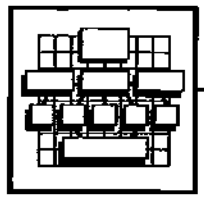
Dataquest Perspective

Cadence is now clearly a master of its own destiny. The vision of becoming the largest supplier of EDA tools has been successfully accomplished by external acquisition and skillful integration and sales. However, Dataquest believes that Cadence's largest challenge is still before it. The EDA market is littered with those who had been No. 1 but who had failed to stay on top due to missed execution or lack of forward thinking. Cadence must base its coming evolution upon the following strengths:

- Technology holding, with a superb portfolio of point tools
- IC design dominance
- Strong field sales and support organization

Software technology has a short shelf life, and Cadence must successfully integrate outstanding point tools into integrated solutions for its customers. It must do so while avoiding the pitfalls of its largest competitor and last year's EDA king-of-the-hill, Mentor Graphics. Cadence's continued success is based upon its ability to do the following:

- Evolve an integration strategy without causing widespread customer disruption
- Use selected technology partnerships to further enhance point tools
- Avoid focusing on internal structural and political battles
- Develop, partner with, and/or acquire new best-of-breed technology to keep the coming generation of start-up companies at bay
- Articulate its vision of the next generation of EDA



Dataquest Vendor Profile

ASICs *Worldwide*

December 21, 1992

Cadence Design Systems Inc.

Corporate Statistics

Location	San Jose, California
President and CEO	Joseph B. Costello
Number of Employees	2,500
1991 Software Revenue*	$292.8 million
1991 Corporate Revenue*	$392.3 million
Founded	1988
EDA Software Market Share*	24.2 percent
Strongest Competitor	Mentor Graphics

*Adjusted to include Valid revenue

Corporate Overview

Vision is the art of seeing things invisible.
—Cover of Cadence Annual Report, 1991

Cadence Design Systems Inc. develops, markets, and supports electronic design automation (EDA) software products for a variety of technical workstations. The company has a diverse offering of tools, consistent with its history as a company based upon merger and acquisition. It currently enjoys the privilege of being the largest provider of EDA software to the world.

Corporate Organization

Formed as a result of a merger between SDA Systems Inc. and ECAD in May 1988, the management structure at Cadence has been fluid over the past four years, with change being the norm. The company is currently organized along four main product thrusts: IC design, analog design, system design, and CAE tools. Yet through it all, Joseph B. Costello, President and CEO, has provided a very strong leadership presence. Figure 1 outlines the Cadence organizational structure.

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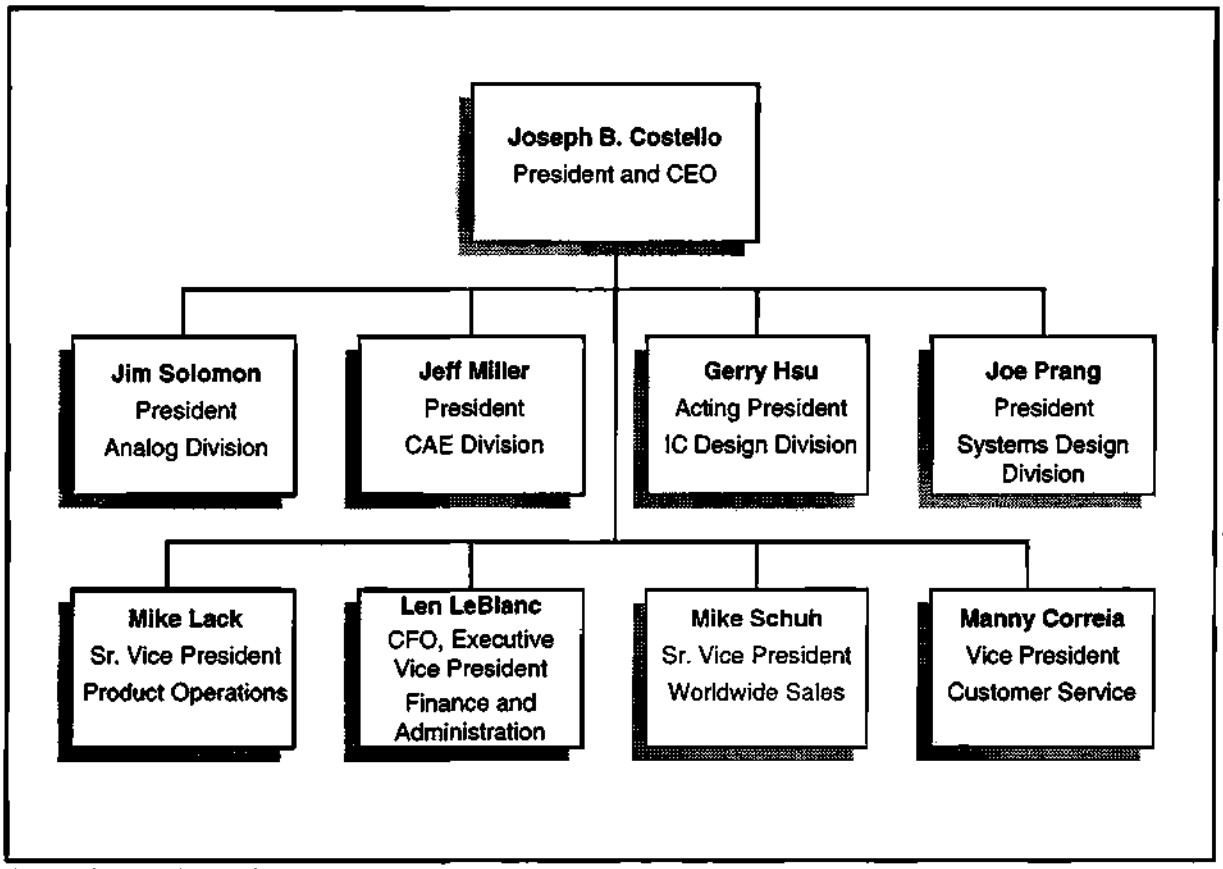

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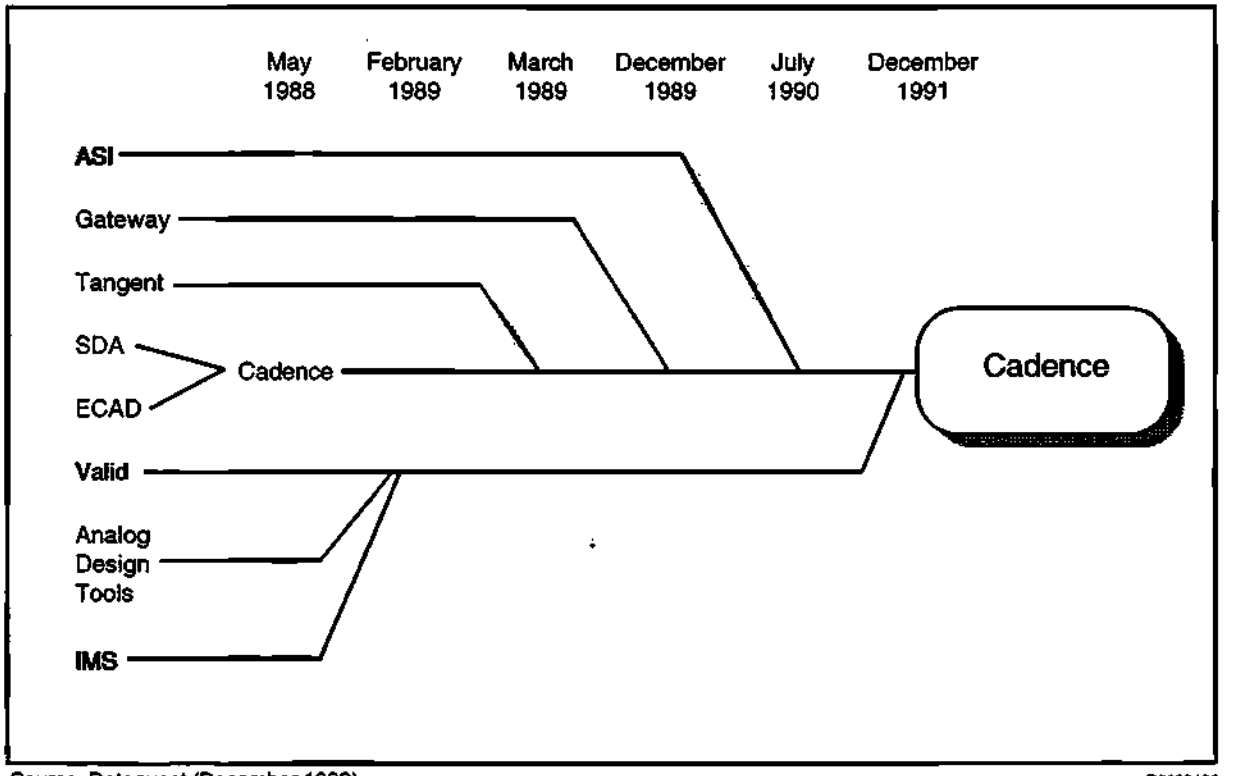

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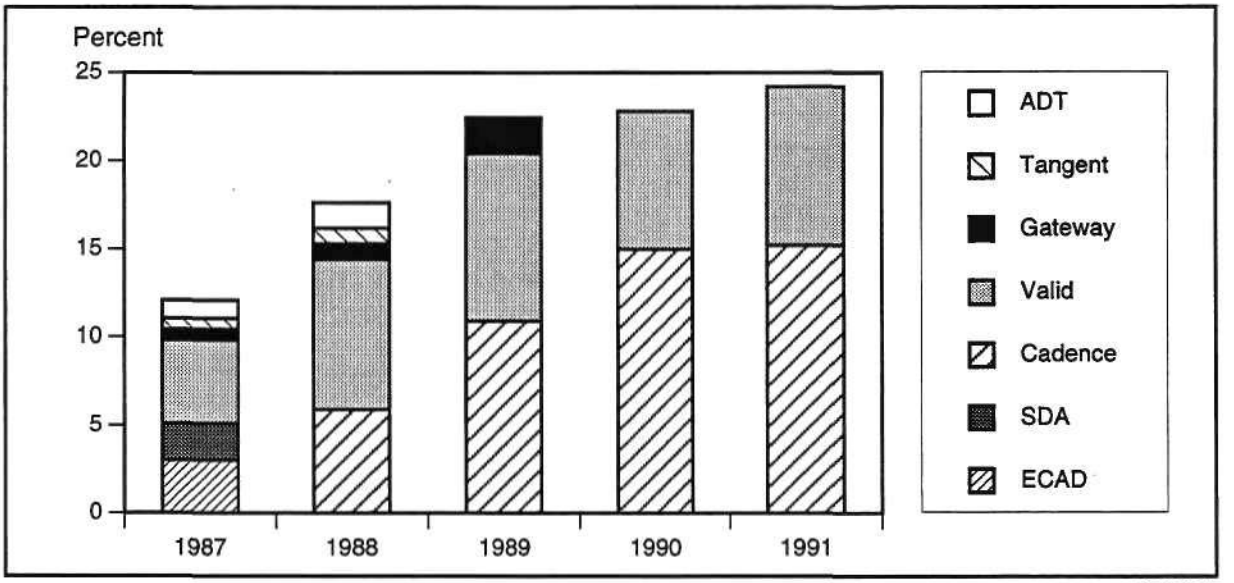

Source: Dataquest (December 1992)

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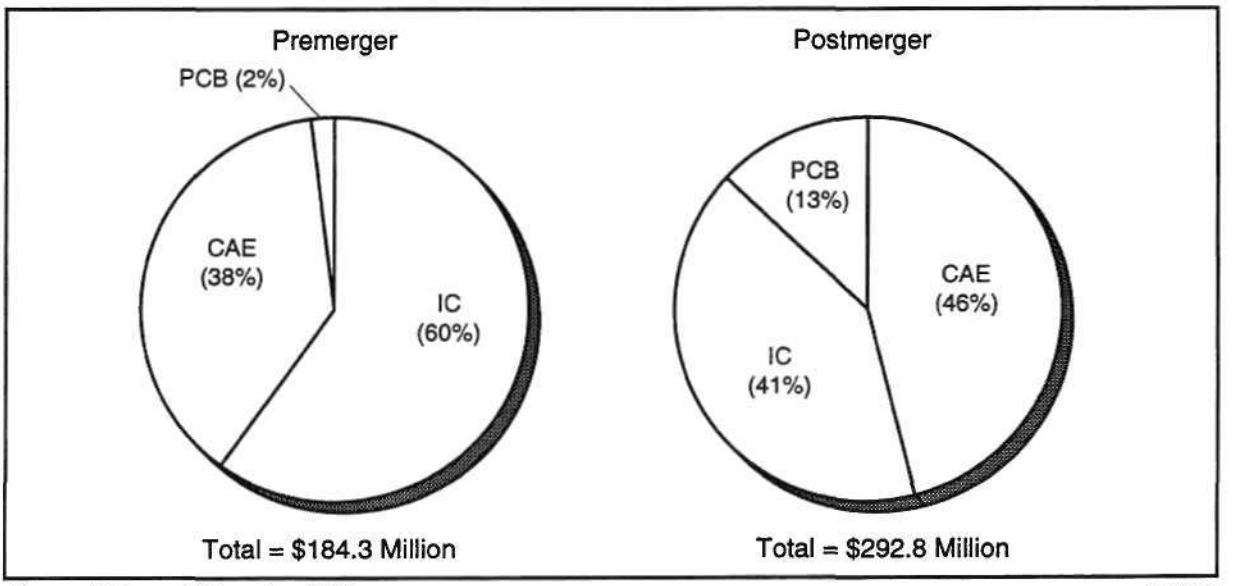
Figure 4
Cadence 1991 Worldwide Software Revenue Percent by Market



Source: Dataquest (December 1992)

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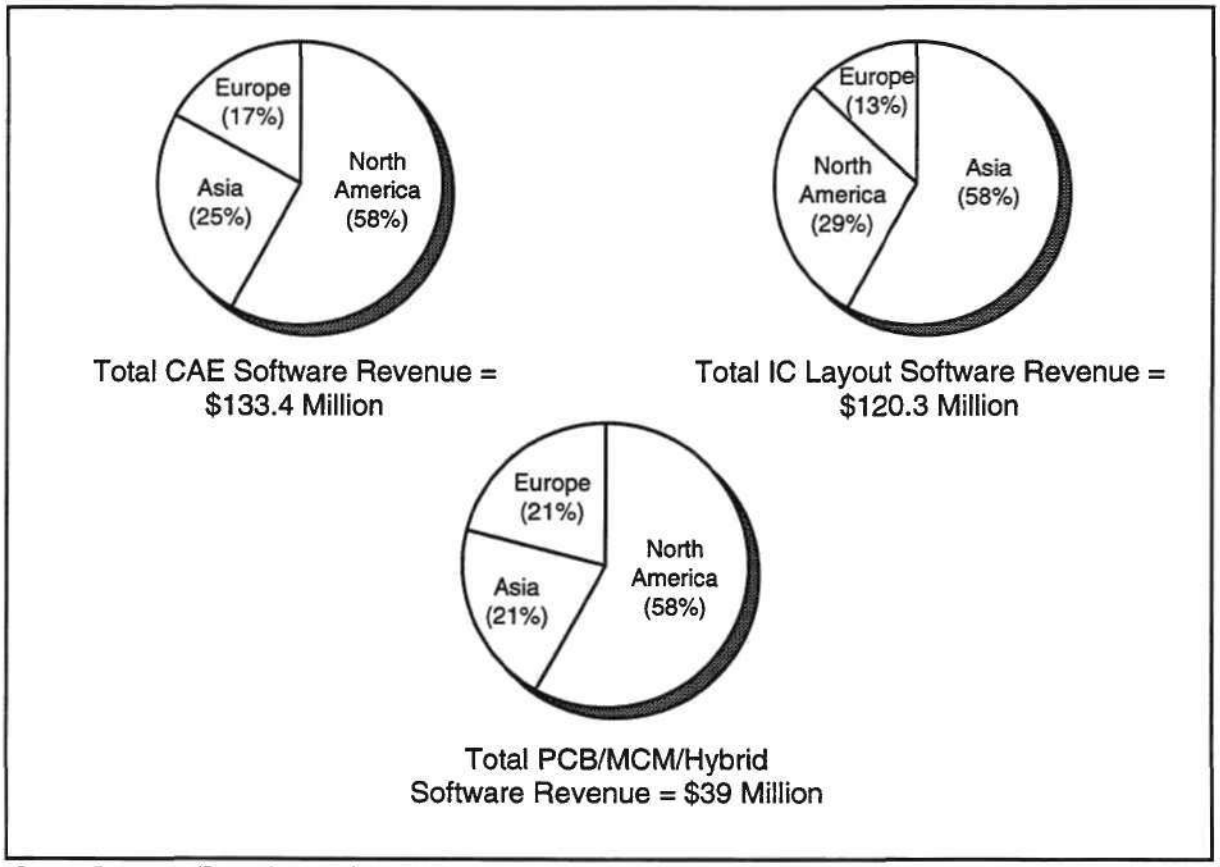
Figure 5
Combined Cadence/Valid 1991 Software Revenue by Market and Region



Source: Dataquest (December 1992) G2002165

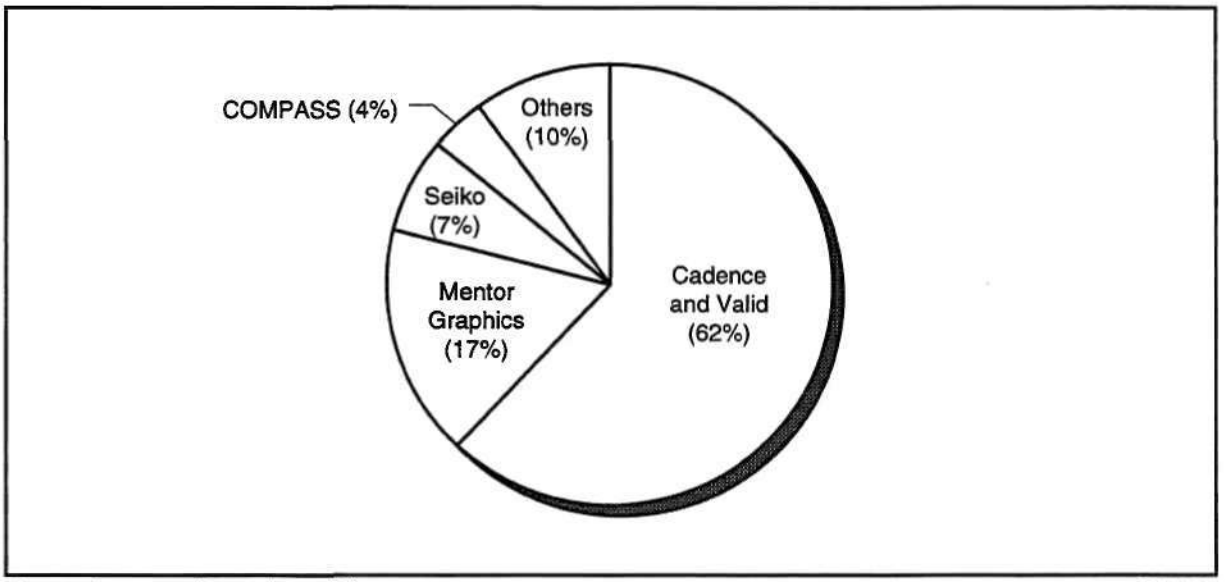
CAE Penetration Has Highs and Lows, with Verilog Leading the Way

Cadence made its big leap into the CAE market with its 1989 acquisition of Gateway Design Automation. The jewel Cadence was after was the Verilog-XL simulator, a simulator that today still is the de facto standard in mixed-level simulation. However, this powerful weapon in the Cadence arsenal has come under attack in two areas.

The first area is the emergence of the VHSIC hardware description language (VHDL). This rival hardware description language (HDL) and mixed-level simulators based upon its use have begun to erode Verilog's market share.

The second factor that will affect Verilog sales is the birth of the Verilog-clone simulation market. As part of Cadence's battle plan against VHDL, it created Open Verilog International (OVI) as an industry body to evolve the Verilog HDL into a true industry standard, as opposed to a proprietary, de facto standard. As a by-product of this effort, we are now beginning to see Verilog-based

Figure 6
1991 Worldwide IC Layout Software Market Share



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Synthesis May Be a Weak Chink in the Cadence Armor

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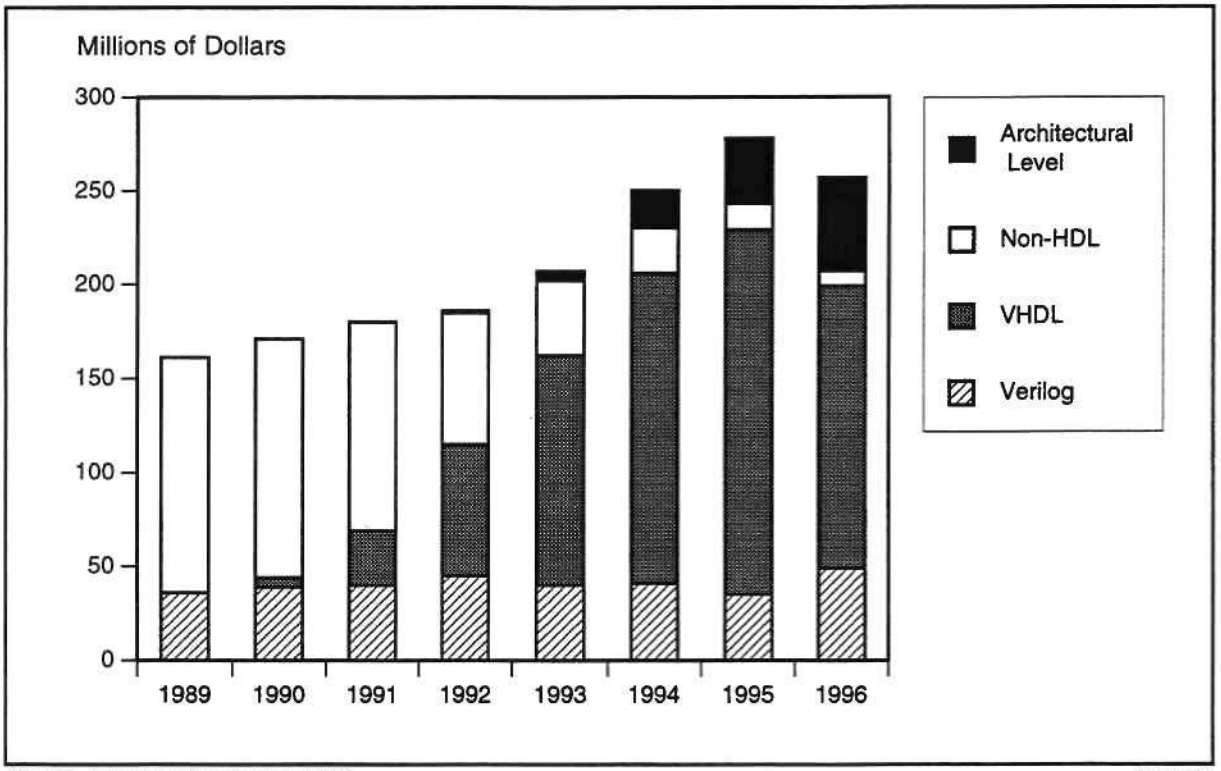
Figure 7
Historical and Projected Growth of Worldwide Software Simulation Market



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Attempting to build upon its Verilog strength, Cadence has generated its own front-end design entry system called Composer. In addition, Cadence has generated PLD design tools and other design verification tools. These products are not necessarily "lead" products that drive sales; rather they are "drag" products that are brought along to fill out the solution for the electronic designer. Cadence will look to its strength in Verilog simulation to evolve into a more potent VHDL-based CAE product offering.

PCB Design Tools Complete the Circle

To become the largest supplier of EDA tools, Cadence had the vision to seek out new areas of expansion. While it never had a presence in the printed circuit board (PCB) design area, it sought to acquire this expertise. Its first attempt was to purchase ASI, a PCB production house that had its own internal set of PCB design tools. Unfortunately this strategy proved to be unsuccessful, and after this misstep, Cadence set its sights on larger game. Cadence's weakness in PCB design tools led to its merger with Valid, which had a growing business in PCB design with its Allegro tool set. Cadence's challenge is to keep the momentum of the Allegro tool set while integrating it into the Cadence set of framework and entry tools.

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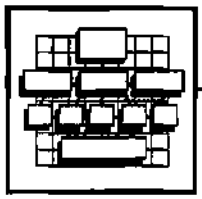
Cadence is now clearly a master of its own destiny. The vision of becoming the largest supplier of EDA tools has been successfully accomplished by external acquisition and skillful integration and sales. However, Dataquest believes that Cadence's largest challenge is still before it. The EDA market is littered with those who had been No. 1 but who had failed to stay on top due to missed execution or lack of forward thinking. Cadence must base its coming evolution upon the following strengths:

- Technology holding, with a superb portfolio of point tools
- IC design dominance
- Strong field sales and support organization

Software technology has a short shelf life, and Cadence must successfully integrate outstanding point tools into integrated solutions for its customers. It must do so while avoiding the pitfalls of its largest competitor and last year's EDA king-of-the-hill, Mentor Graphics. Cadence's continued success is based upon its ability to do the following:

- Evolve an integration strategy without causing widespread customer disruption
- Use selected technology partnerships to further enhance point tools
- Avoid focusing on internal structural and political battles
- Develop, partner with, and/or acquire new best-of-breed technology to keep the coming generation of start-up companies at bay
- Articulate its vision of the next generation of EDA



Dataquest Vendor Profile

ASICs *Worldwide*

December 21, 1992

Cadence Design Systems Inc.

Corporate Statistics

Location	San Jose, California
President and CEO	Joseph B. Costello
Number of Employees	2,500
1991 Software Revenue*	$292.8 million
1991 Corporate Revenue*	$392.3 million
Founded	1988
EDA Software Market Share*	24.2 percent
Strongest Competitor	Mentor Graphics

*Adjusted to include Valid revenue

Corporate Overview

Vision is the art of seeing things invisible.
—Cover of Cadence Annual Report, 1991

Cadence Design Systems Inc. develops, markets, and supports electronic design automation (EDA) software products for a variety of technical workstations. The company has a diverse offering of tools, consistent with its history as a company based upon merger and acquisition. It currently enjoys the privilege of being the largest provider of EDA software to the world.

Corporate Organization

Formed as a result of a merger between SDA Systems Inc. and ECAD in May 1988, the management structure at Cadence has been fluid over the past four years, with change being the norm. The company is currently organized along four main product thrusts: IC design, analog design, system design, and CAE tools. Yet through it all, Joseph B. Costello, President and CEO, has provided a very strong leadership presence. Figure 1 outlines the Cadence organizational structure.

Cadence is a company formed by mergers, as shown in Figure 2. While retaining the Cadence name since 1988, the company is in fact an amalgamation of diverse EDA companies formed in the early

For more information on Cadence Design Systems Inc. or the ASICs industry, call Bryan Lewis at (408) 437-8668.

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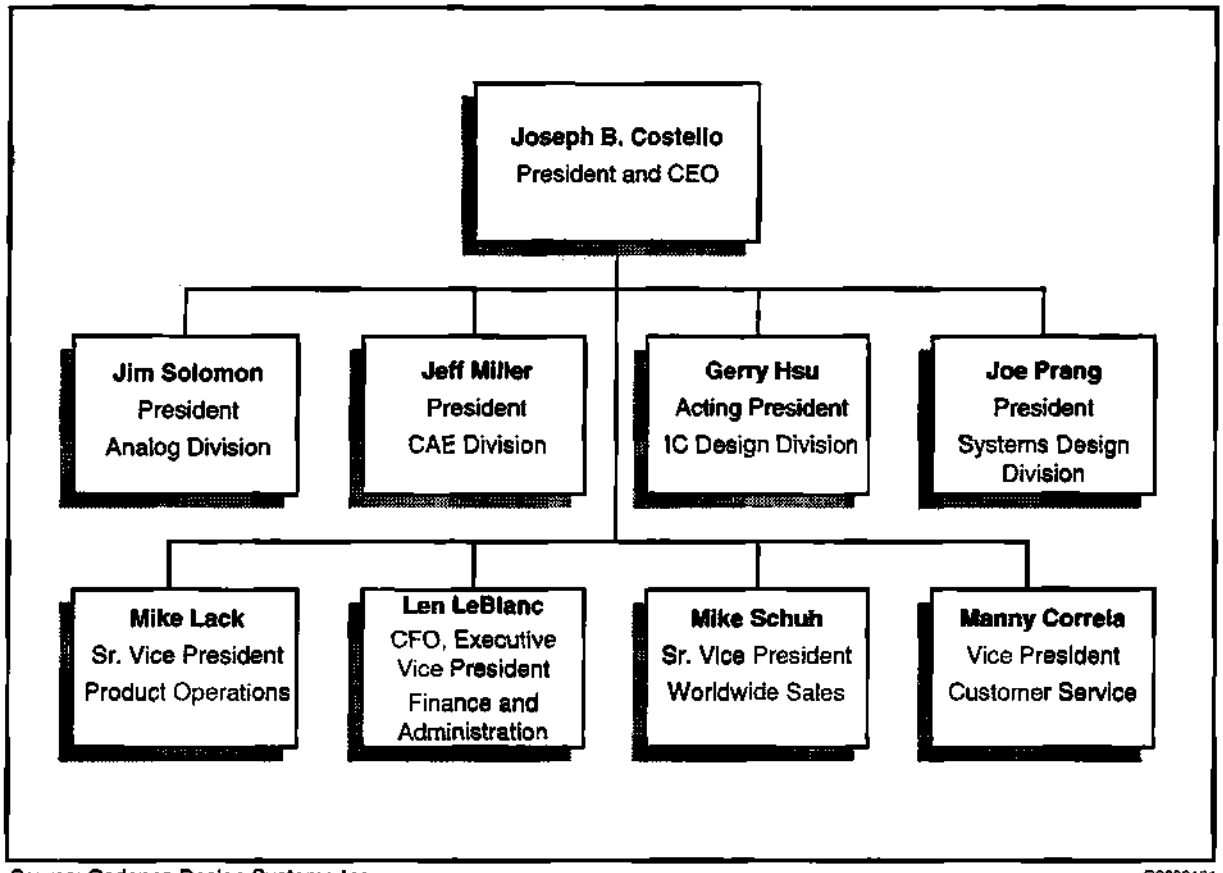
ASIC-SEG-VP-9202

Figure 1
Cadence Corporate Organization



Source: Cadence Design Systems Inc. G2002161

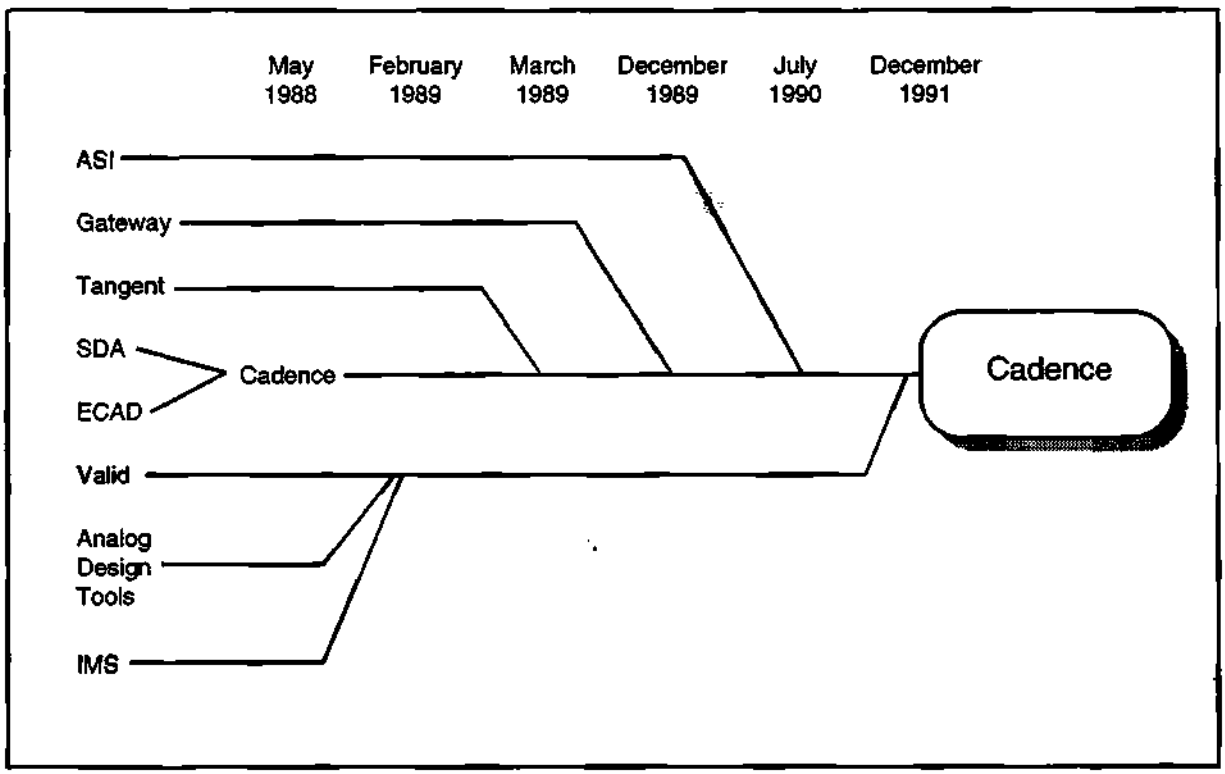
1980s. As such, the key management team is composed of aggressive individuals gleaned from these mergers and other electronics-related companies. Cadence's strength has been its corporate vision and shrewd acquisition of technology.

Key Personnel

Joseph Costello is the embodiment of Cadence. A scientist by training, he holds an impressive list of academic credentials. A B.S. in math and physics from Harvey Mudd, an M.S. in physics from Yale, and a master of science in physics from UC Berkeley round out his collegiate history. This scientific bent has not hindered his ability to make bold, decisive strokes in piloting the Cadence ship through the turbulent EDA waters. He has surrounded himself with a strong, experienced, management team, adding stability to a potentially chaotic ride.

Manny Correia, vice president of Customer Service, recently assumed this position from his previous post as vice president of Operations. Correia came along for the ride when Cadence purchased Gateway

Figure 2
Cadence Merger History



Source: Dataquest (December 1992) G2002162

Design Automation in 1989. He used his B.S.E.E. and M.S. in management science at IBM for 31 years before joining Gateway.

Aki Fujimura, vice president of Central Engineering and Information Services, is responsible for the infrastructure that Cadence's application tools run upon. He rose up through the engineering ranks at Cadence and holds both a bachelor's and master's degree in electrical engineering and computer science from MIT.

Michael D. Lack, senior vice president of Product Operations, had previously been president of Cadence's IC Division. His move into his current position shows top management's renewed focus at delivering quality products in a timely manner.

Leonard J. LeBlanc is the executive vice president of Finance and Administration and chief financial officer. He has the daunting task of making fiscal sense of the continuing saga of mergers and acquisitions at Cadence.

Jeffrey A. Miller is the president of the Computer-Aided Engineering (CAE) Division. With a classic combination of B.S.E.E. and M.B.A. credentials, Miller arrived at Cadence shortly before the merger with Valid. He previously had been general manager of storage products at computer subsystem supplier Adaptec.

Joseph Prang, president of the Systems Design Division, had been vice president of Marketing at Valid prior to the merger. Prang was one of the top executives at Valid that remained a part of the integral functioning of Cadence's day-to-day operations. Prang also has a combination B.S.E.E. and M.B.A. from Purdue University.

James E. Solomon, president of the Analog Division, has been with Cadence since its inception. He had been a founder of SDA, which he created after a tenure at National Semiconductor.

Michael N. Schuh is the senior vice president of Worldwide Sales. An alumni of EDA suppliers Daisy and Computervision, Schuh rides herd on some 60 sales offices worldwide.

EDA Products

Cadence carries a complete portfolio of strong point tools that address the broad range of electronic designer's design problems. This section outlines the major products, segmented by the area they address. Tables 1 through 3 outline Cadence's design products.

Table 1
Cadence's IC Design Products

Product	Application
ASIC Workbench	Front-to-back ASIC design
Dracula	Design verification
Diva	Design verification
Gate Ensemble	Gate Array place and route
Cell Ensemble	Cell-based IC place and route
Cell3 Ensemble	3-layer metal cell-based IC place and route
Preview	ASIC floorplanner
Analog Artist	Analog IC design and simulation
Dantes	Analog design for test

Source: Dataquest (December 1992)

Table 2
Cadence's CAE Design Products

Product	Application
Composer	Design entry
Synergy	ASIC logic synthesis
Verilog-XL	Mixed-level simulation
VHDL-XL	Mixed-level simulation
Veritime-XL	Static timing analysis
Verifault-XL	Fault Simulation

Source: Dataquest (December 1992)

Table 3
Cadence's PCB Design Products

Product	Application
System Workbench	Front-to-back PCB/MCM design
Allegro	PCB/MCM place and route
Thermax	PCB/MCM thermal analysis
SigNoise	PCB/MCM signal integrity analysis
Viable	PCB/MCM reliability analysis
Prance-XL	PCB/MCM autorouting
Analog Workbench	Analog PCB design simulation

Source: Dataquest (December 1992)

Market Position

Cadence is currently the largest supplier of electronic design automation tools. Dataquest estimates that its 1991 software revenue was $184.3 million, as shown in Table 4. However, this figure is based upon premerger conditions. With the addition of Valid's $108.5 million, Cadence's total software revenue is $292.8 million.

By becoming the largest supplier of EDA tools, Cadence has unseated its strongest rival, Mentor Graphics. Mentor Graphics was one of the pioneering companies of EDA, and the only standalone entity left from the boom years of the big three: Daisy, Mentor, and Valid. Table 5 depicts the "tale of the tape" for these two EDA giants. In 1991, both Cadence and Mentor Graphics lost money. Cadence's loss was because of write-downs from merger costs, and Mentor Graphics' problems stemmed from layoffs and restructuring. However, 1992 has seen Cadence's profits improve compared to last year, and the company seems to be on track to break its revenue number of last year. Mentor Graphics, conversely, is still struggling with product transitions, downsizing, and loss of revenue due to its dwindling hardware sales.

While it may seem that Cadence's rise to prominence has been led by purchasing market share, this is not the case. Dataquest has analyzed the market share of the smaller entities that have merged to form the Cadence of today (see Figure 3). The combined market share has continued to rise consistently over the past five years, which shows the telltale signs of excellent management. In this case, the team is definitely greater than the sum of its players. Additionally, the Cadence/Valid merger balanced the software revenue of the company to a more even distribution, which reflects Cadence's vision of becoming a broad range supplier of EDA tools (see Figure 4). Geographic distribution of Cadence's software revenue is outlined in Figure 5.

Table 4
1991 EDA Software Market Share

Company	Software Revenue ($M)	Market Share (%)
Cadence	184.3	15.2
Mentor Graphics	146.4	12.1
Valid	108.5	9.0
Racal-Redac	70.6	5.8
Zuken	62.3	5.1
Intergraph	44.7	3.7
Viewlogic	32.0	2.6
Synopsys	30.1	2.5
Wacom	25.5	2.1
Compass Design	23.9	2.0
All EDA Companies	1,210.0	100.0

Source: Dataquest (December 1992)

Table 5
Tale of the Tape for Cadence/Mentor Graphics Fight (Millions of Dollars)

	Cadence	Mentor Graphics
1991 Corporate Revenue	392.3	400.1
1991 Profit	-21.7	-61.6
1991 Software Revenue	292.8	146.4
1991 Service Revenue	88.1	135.9
1991 Hardware Revenue	5.1	113.8
Q1 1992 Corporate Revenue	101.3	100.1
Q2 1992 Corporate Revenue	105.9	89.0

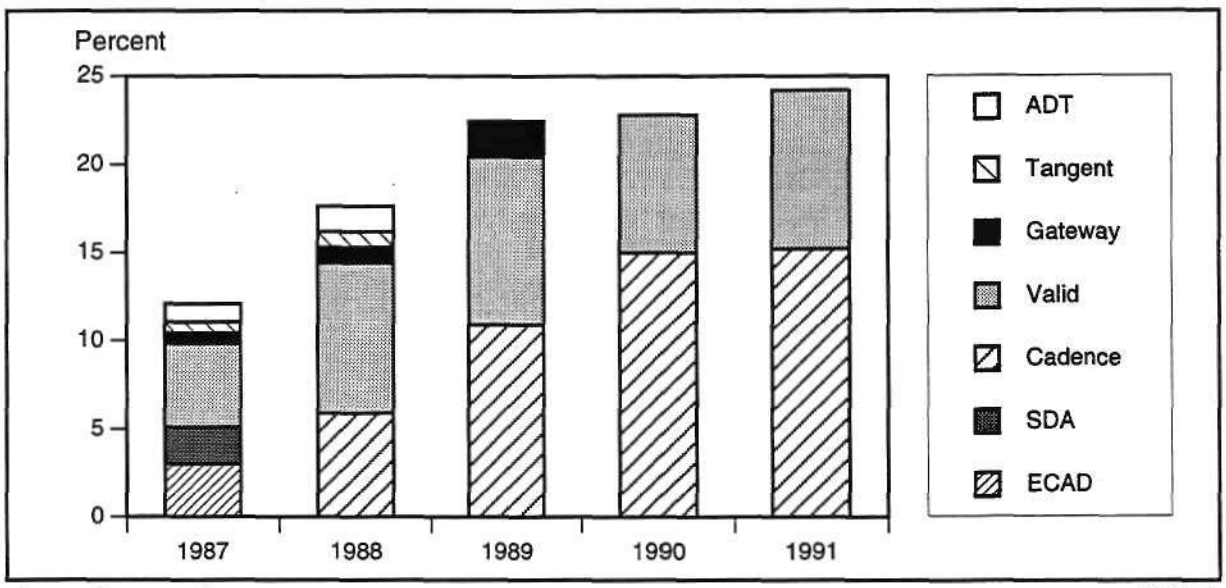
Source: Cadence, Mentor Graphics, and Dataquest (December 1992)

IC Design Drove Cadence's Rise to Prominence

IC design was the base that Cadence worked from to penetrate the EDA market. By 1991, the combined Cadence and Valid entity garnered a whopping 62 percent of the IC layout market (see Figure 6). Cadence has very little competition in this market, with Mentor Graphics trailing Cadence/Valid by almost $87 million. It is from this position of strength in the IC layout market that Cadence had set its sights on total EDA domination.

On the downside, the IC design market has reached a saturation point. Slowing worldwide semiconductor growth, as well as the economic downturn in Japan, will further stagnate this market. However, there are shifts in the methodologies used in custom and semicustom IC design, and Cadence is well positioned to migrate with the changing user needs.

Figure 3
Worldwide EDA Software Market Share of Companies Forming Cadence



Source: Dataquest (December 1992)

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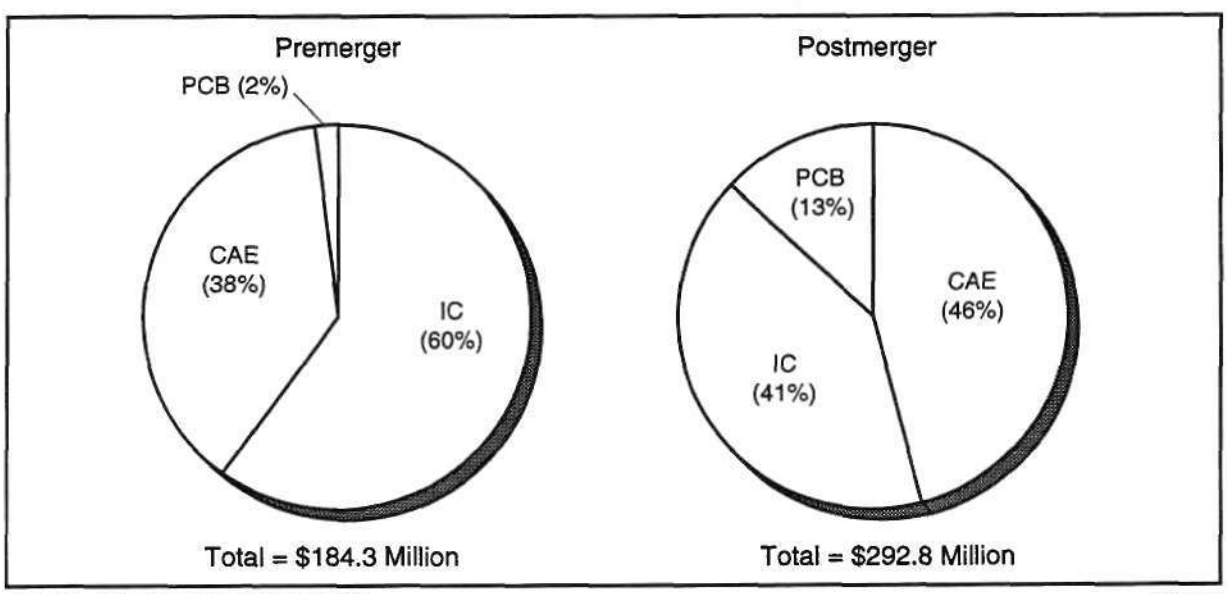
Figure 4
Cadence 1991 Worldwide Software Revenue Percent by Market



Source: Dataquest (December 1992)

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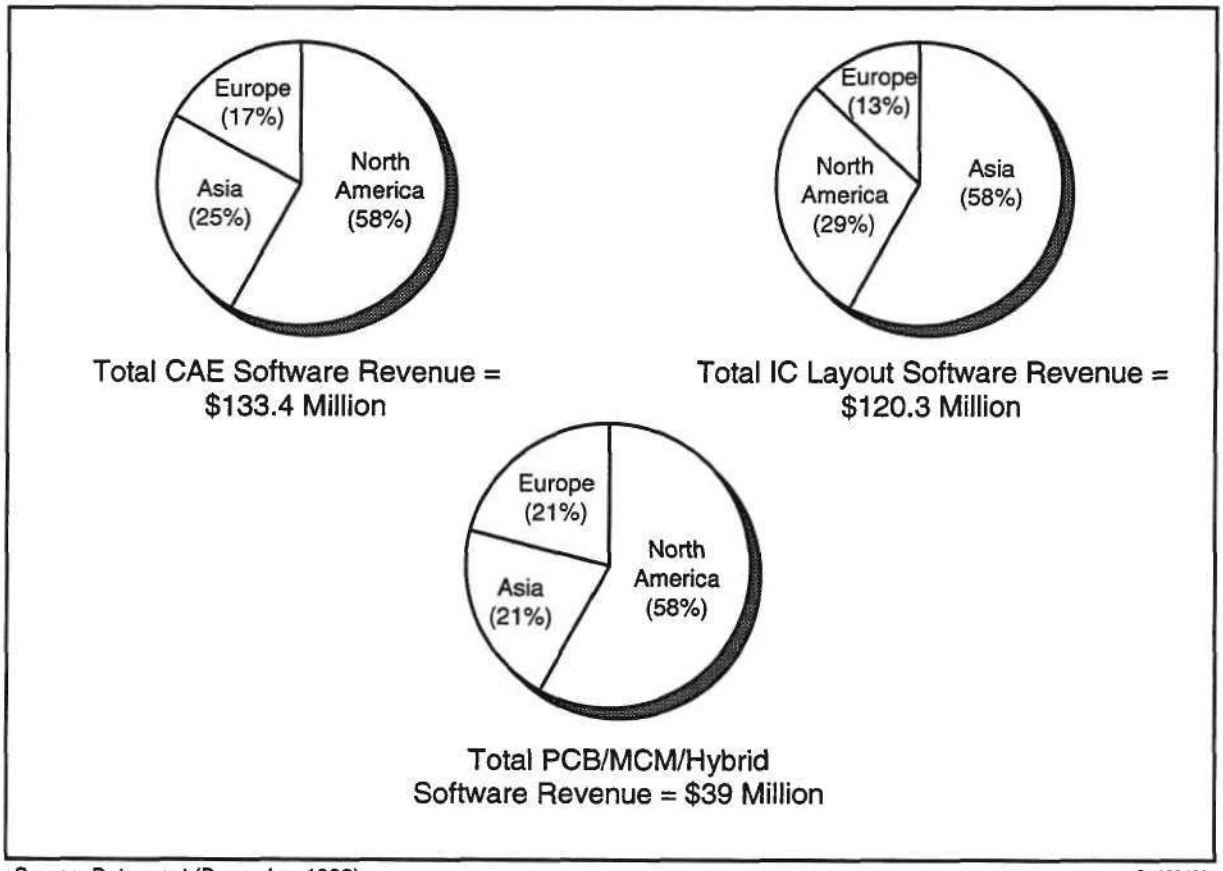
Figure 5
Combined Cadence/Valid 1991 Software Revenue by Market and Region



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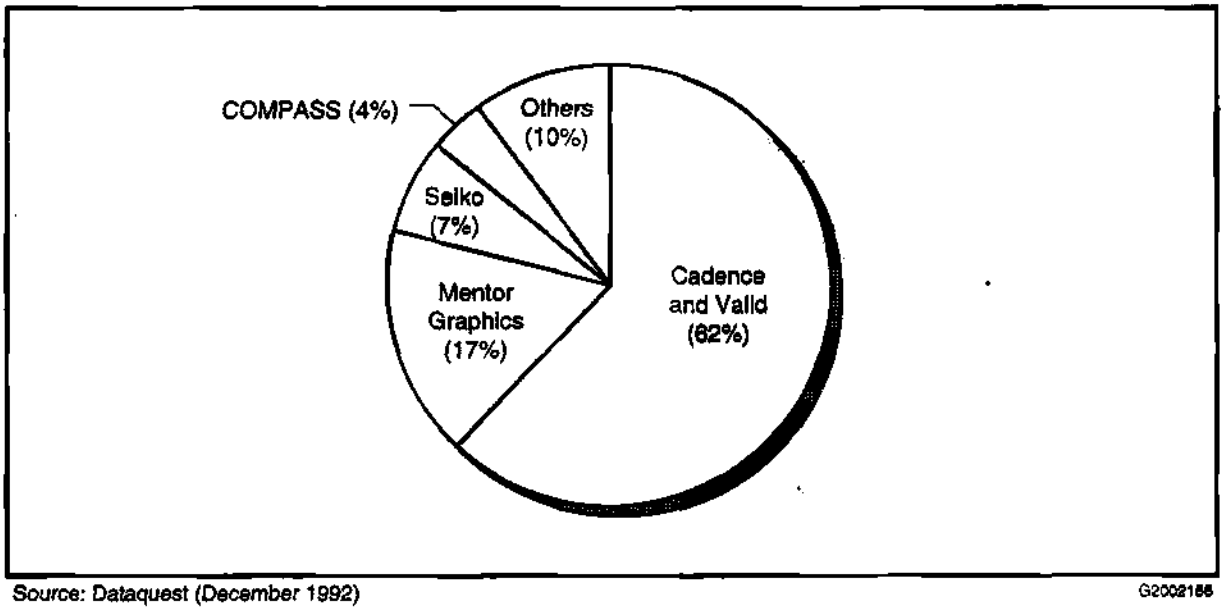

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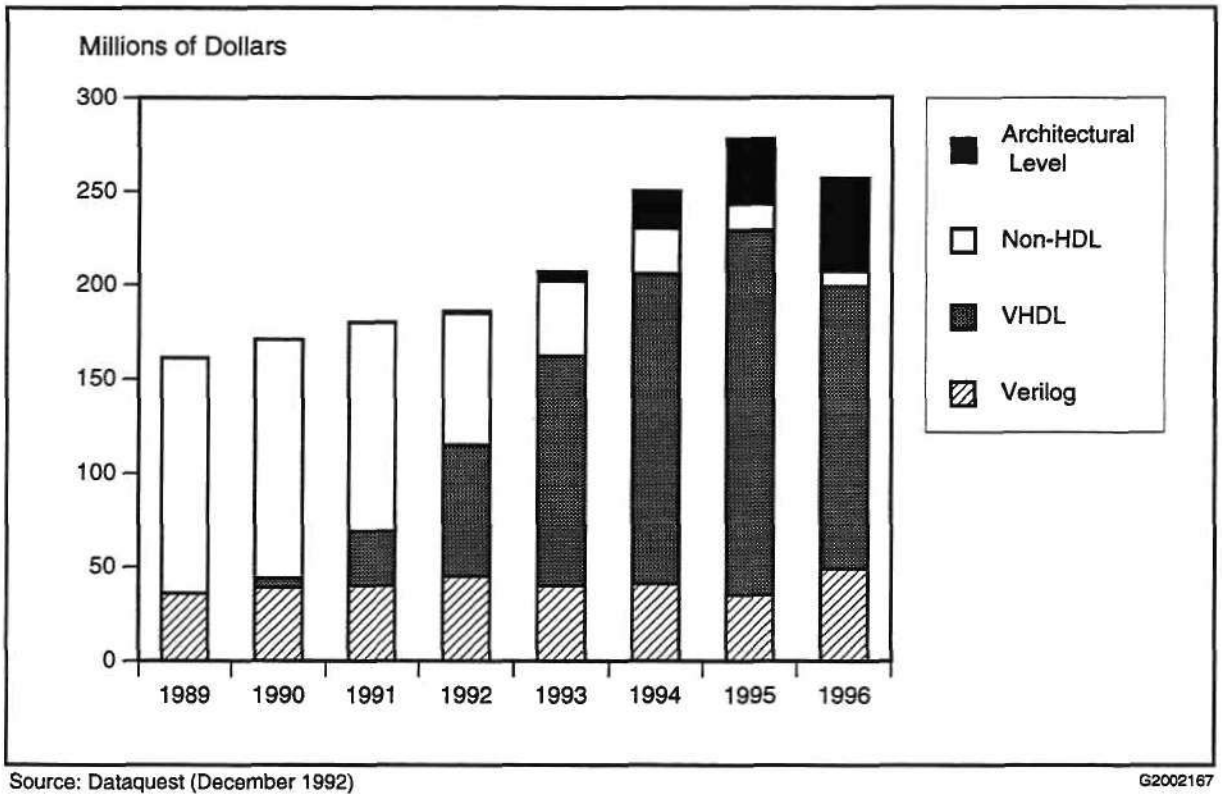

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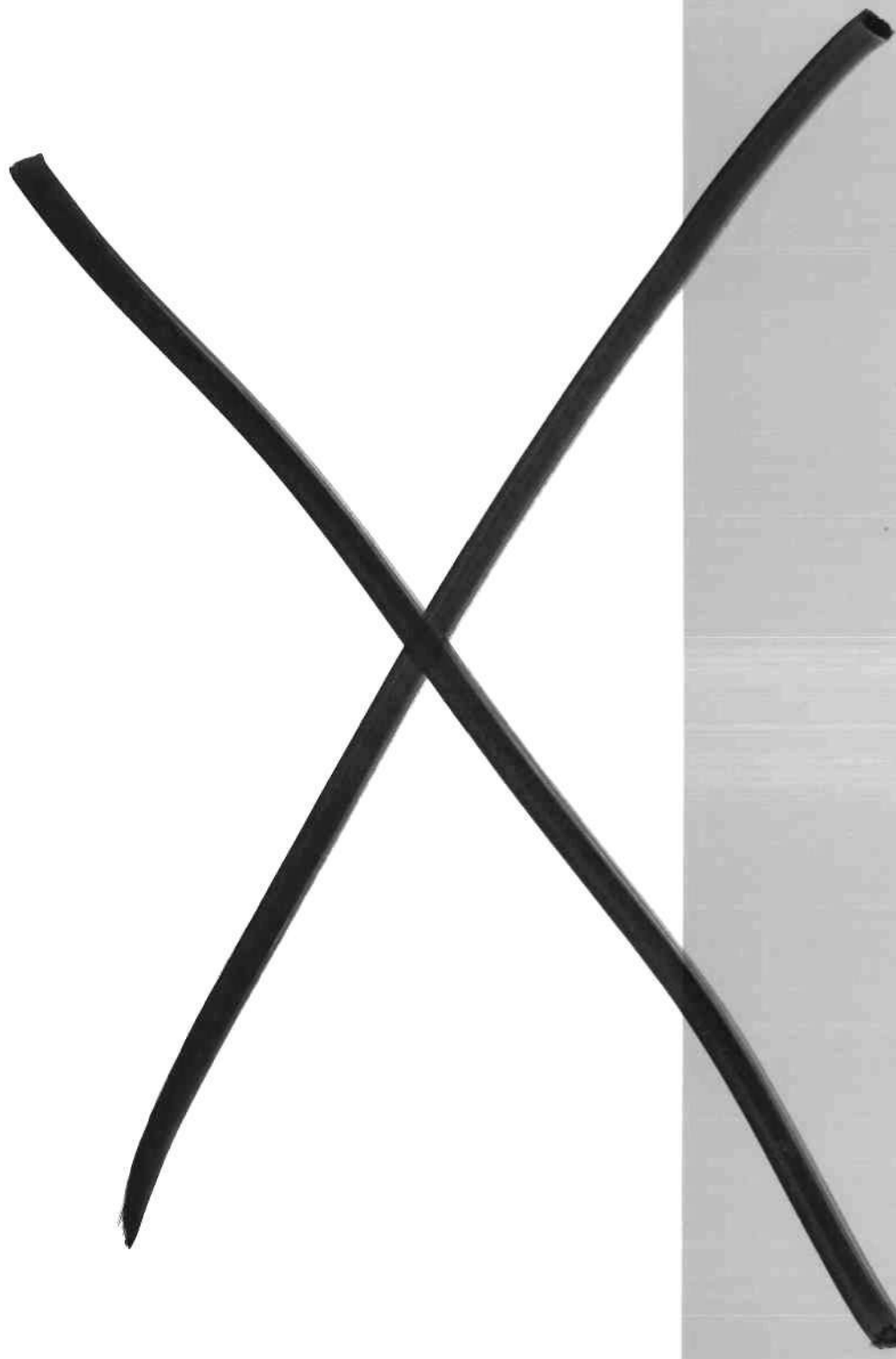

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Dataquest Perspective

ASICs *Worldwide*

ASIC-SEG-DP-9204 July 27, 1992

In This Issue...

Technology Analysis

Function-Specific Programmable Logic Devices—No More Mr. Niche Guy

The name "function-specific programmable logic devices" is itself an oxymoron. Programmable logic devices (PLDs) were created so that they may implement a wide variety of logic functions. Yet a penalty must be paid for such flexibility. Inherent to general-purpose programmable devices is a programming and test overhead that manifests itself as additional silicon area for programming elements and test structures. Because of this limitation, a programmable device will never implement any function faster or cheaper than a standard part. Yet users have shown a preference for using a more flexible programmable solution, and they are willing to pay a premium for it. Now, as users continue to demand more density and performance from their programmable solutions, PLD vendors should examine new ways to add incremental speed and functionality with minimal die-size impact. One avenue of possibility is with function-specific programmable logic devices.

Function-specific PLDs provide standard, nonprogrammable functions, optimized for speed and die size, in conjunction with general-purpose programmable logic. They may be classified in two ways: highly programmable and slightly programmable. Highly programmable devices are characterized by having large amounts of programmable logic with a small portion of standard functionality. Examples of this type of device include PLDs with diffused SRAM, ALUs, storage registers, and bus interface logic adjacent to large amounts of CPLD, or FPGA-based logic. Slightly programmable devices, on the other hand, have large amounts of standard logic in relation to a small amount of programmability. Examples of this type of device include a graphics processor with programmable bus interface logic, or a standard

bus interface device with programmable address selection or programmable self-decoding.

Some companies have made tentative steps in this direction. Historically, attempts have been made with slightly programmable devices, and the standard logic contained in the programmable device was targeted to a specific application. Example applications include bus interfacing, microsequencing, and waveform generation. Devices from such companies as Altera (EPB1400, EPS448, and EPB2001), Intel (5CBIC) and Cypress (7C330 and 7C361) have all failed in generating significant revenue for these companies.

Enter at Your Own Risk

Function-specific PLDs, more than other device types, are fraught with peril. These devices are prone to market failure for the following reasons:

- The end application market never materializes
- The device does not meet application's speed or density needs
- A production delay causes missing critical design-in window
- A standard part with the same functionality is introduced to the market
- The function-specific logic section is too segmented for broader use

Rules for Success

In order to avoid the potential pitfalls of function-specific PLDs, companies should follow the basic rules for success in creating a function-specific programmable logic device discussed in the following paragraphs.

Target Emerging Applications Where Standards Are in Flux

It is important for function-specific PLD vendors to target markets that take full advantage of the flexibility a programmable solution provides. Any large-volume application will mature to a point where a standard part can solve the problem. The challenge for the PLD vendor is to stay one step ahead of chip set and standard logic vendors by recognizing areas of opportunity for a semiprogrammable solution. Current application areas that should be investigated include imaging, digital image compression and communication, mobile data collection, and GPS.

Target Applications with Limited Price Sensitivity

There will continue to be a cost premium for function-specific PLDs because of their programmable nature. PLD vendors should therefore target applications with run rates less than 10,000 units per year. This effectively rules out high-volume areas such as consumer goods.

Partner with a Technology Leader in an Emerging Market

It is critical to gain a thorough understanding of the end application when creating a function-specific device. ASIC vendors have the ability to scrutinize every design that they produce. PLD vendors do not have the same luxury because the design is programmed into the part at the customer site. This limited insight into the end application makes it imperative that the PLD vendor foster a close development partnership with a technology leader in the end application market.

Check for Broad Acceptance

After agreeing upon specifications for the new device, it behooves the PLD vendor to show a mock-up of the device to other potential users, which in most cases will be competitors of the chosen partner. A function-specific programmable device must have a broad acceptance in the target application market in order to generate sufficient revenue.

Market to Specific End Users

Particularly in the case of slightly programmable solutions, it is important to guide the sales effort of these devices toward specific end users. The user who has no need for the nonprogrammable area on the function-specific PLD will no doubt purchase a device that provides a lower-cost solution. The user will not pay for the extra, nonusable die area consumed by the nonprogrammable function.

Embedded Cell Paradigm

The development of function-specific PLDs is analogous to the emergence of the embedded gate array in the gate array market. The embedded gate array merges the cost efficiency of cell-based ICs with the reduced turnaround time of gate arrays. Embedded gate array vendors have

tried to target either high-volume applications where the cost savings of diffused cells would be beneficial (such as RISC cores and micro-peripherals) or choose embedded cells that have a broad appeal across many companies (SRAMS, FIFOs, and ALUs). These approaches are similar to slightly programmable and highly programmable function-specific PLDs, respectively. At this point in the maturity of the ASIC market, Dataquest believes that there is a place for properly chosen embedded cells, and these devices will continue to coexist with CBICs and standard gate arrays. The combination of cost savings and rapid turnaround will carve a significant niche between CBICs and gate arrays.

Dataquest Perspective

The viability for function-specific PLDs is less clear than for its embedded cell brethren. Although the gate array and CBIC market totaled almost $7 billion in 1991, programmable logic has yet to reach the $1 billion mark. It is obvious that any highly programmable function-specific programmable device will be able to address a subset of the total PLD market. A 5 percent niche of the $7 billion gate array market is a significant niche, whereas 5 percent of the PLD market is only $4.5 million. It is also questionable whether PLD-only suppliers can penetrate other markets with a slightly programmable solution. Horizontally diverse companies with insight to many areas of semiconductor consumption should look to leverage that knowledge into the creation of slightly programmable devices, while smaller PLD-only companies should focus on creating function-specific devices that have a broad range of uses.

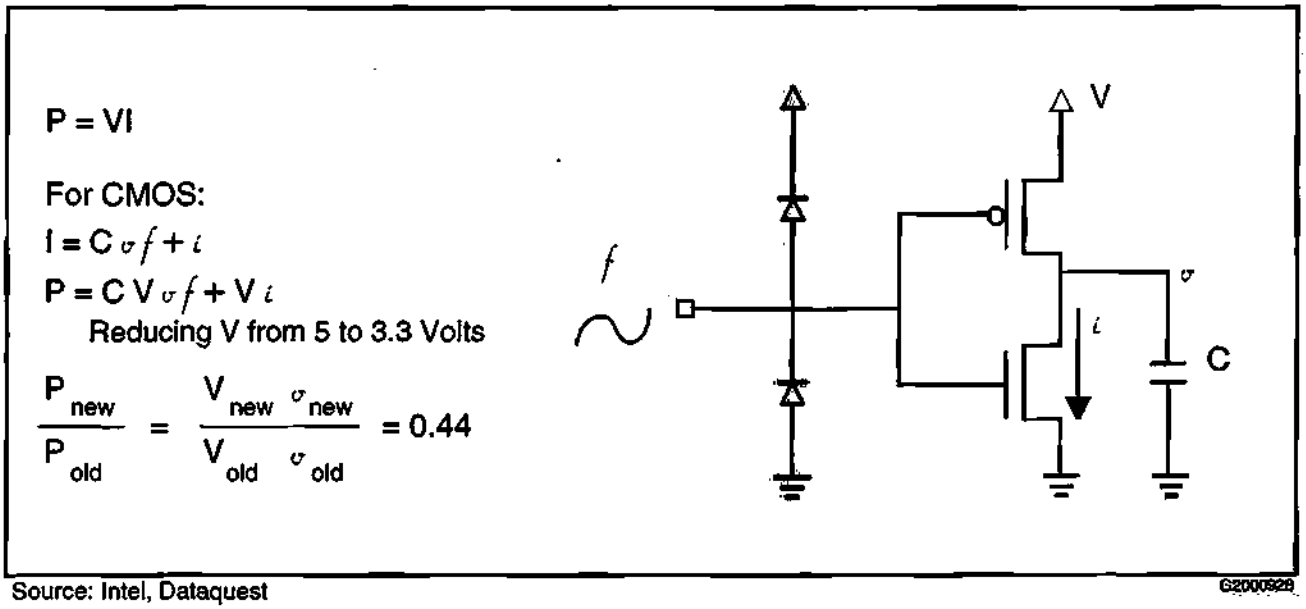
By Robert K. Beachler

3-Volt Rules

The rapid migration to a low-voltage power supply standard is being driven by the need to extend the battery life of hand-held or portable systems. Notable applications driving the migration include laptop, notebook, and palmtop computers; cellular phones; and memory cards. When operation voltage is reduced from 5 volts to 3.3 volts, component power consumption theoretically declines by 44 percent (see Figure 1). Figure 2 applies this same thinking to a laptop system and shows how total system power consumption is affected.

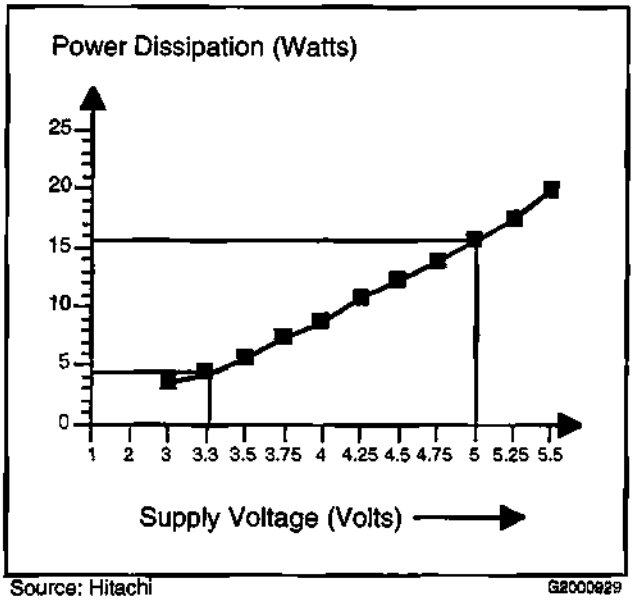
An equally important driver toward 3-volt components is not power related, but technology driven. Process technologies on the bleeding edge of performance and density have extreme difficulty supporting 5-volt operation. Placing 5 volts across a 0.5-micron transistor can cause a permanent drain turn-on, or "punch-through," which is effectively a short circuit rendering the transistor useless. Other reliability problems

Figure 1
CMOS Transistor Power Savings



Source: Intel, Dataquest

Figure 2
Supply Voltages versus Power Dissipation (40-MHz 386 PCMB with 64KB Cache)



Source: Hitachi G2000929

include hot electron effects, where electrons stick in the oxide, and gate oxide breakdown, which causes the CMOS gate to draw current. To eliminate these effects, the voltage across the transistor must be reduced.

The sheer number of transistors that may be packed on a die with sub-0.8-micron processes also contributes toward the shift to 3-volt supplies. It is difficult to dissipate the power consumed by more than 500,000 gates of logic running at 5 volts without using expensive packaging and/or cooling techniques. Although it is still open for debate as to the lithography pitch at which a 5-volt chip becomes impractical, the trend clearly is toward 3 volts. As an example, Toshiba's recently announced 0.5-micron gate array family currently has a 3-volt-only library, but LSI Logic's 0.60-micron family has both a 3-volt and a 5-volt library offering.

Are PLDs Missing in Action?

Clearly, process technology limitations and application needs have combined to create a critical mass of semiconductors necessary for creation of 3-volt systems. Current 3-volt parts are available to designers in the following flavors:

- Microprocessors
- Embedded processors
- DRAMS
- Voltage regulators
- Gate arrays
- CBICs
- EPROMs
- Standard logic
- SRAMs
- VGA controllers

These devices are either redesigned from the ground up to operate optimally at 3 volts, or, more likely, 5-volt devices that have been recharacterized or derated to operate at 3 volts. Conspicuous by their absence are programmable logic devices. At present only one 3-volt PLD has been announced to be available in 1992.

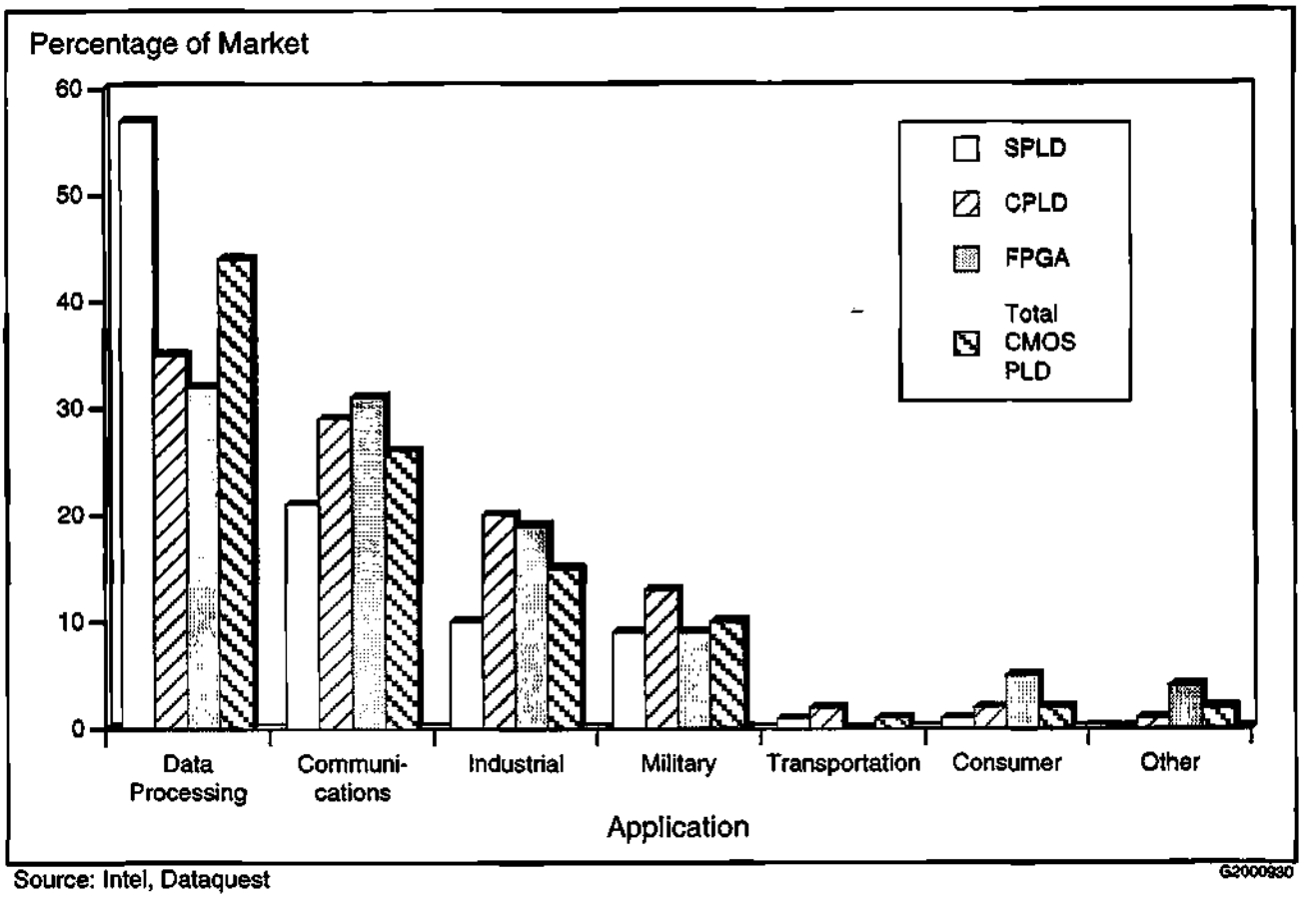
The primary reason explaining the lack of 3-volt PLDs is the age-old supply and demand rule. There is no demand, therefore there is no supply. Currently the 3-volt components listed earlier have been going into large-volume portable computer and consumer markets. Because of their high-volume nature, these applications effectively rule out programmable devices. However, in rare instances where a PLD is used, today's portables are either 5-volt or mixed 5-volt/3-volt systems, so they are capable of accommodating 5-volt PLDs. Indeed, examining the application split of programmable logic, almost 50 percent of the total PLD market is in data processing and less than 3 percent in consumer (see Figure 3). The data processing percentage is predominantly larger, nonportable systems.

However, with the coming of total 3-volt systems, portable suppliers will begin to demand 3-volt PLDs. Dataquest believes that the portable computer market will continue to be small for the PLD vendor. However, the power-savings techniques pioneered in this area will cross industries and fuel growth for 3-volt-only systems in military, instrumentation, and portable data acquisition and logistics applications, which have historically been users of programmable solutions.

3-Volt PLD Power Savings

Because of the lack of demand for 3-volt PLDs, the benefits a 3-volt PLD may bring have not

Figure 3
1991 CMOS PLD Application Markets



Source: Intel, Dataquest

been examined. Dependent on the programming technology, 3-volt PLDs will have different characteristics.

The simplest case is SRAM or antifuse-based PLDs. These devices behave as CMOS devices, with their power consumption based upon capacitive loading and frequency. The power savings this type of device realizes is a straightforward 44 percent reduction in power consumption over a 5-volt counterpart. Because they behave as true CMOS components, these devices have a low power consumption rating at low frequencies, and the drop to a 3-volt rail has a small impact on overall system power consumption.

For EPROM- or EEPROM-based devices, however, the power savings may be more significant at lower frequencies. As shown in Figure 4, these devices have a very heavy DC current component, caused by leakage current in the EPROM array. In fact, for a 22V10-type device, the DC power is as much as 0.5 watts. Applying a 3.3-volt rail can considerably decrease the amount of power consumed by these power-hungry devices.

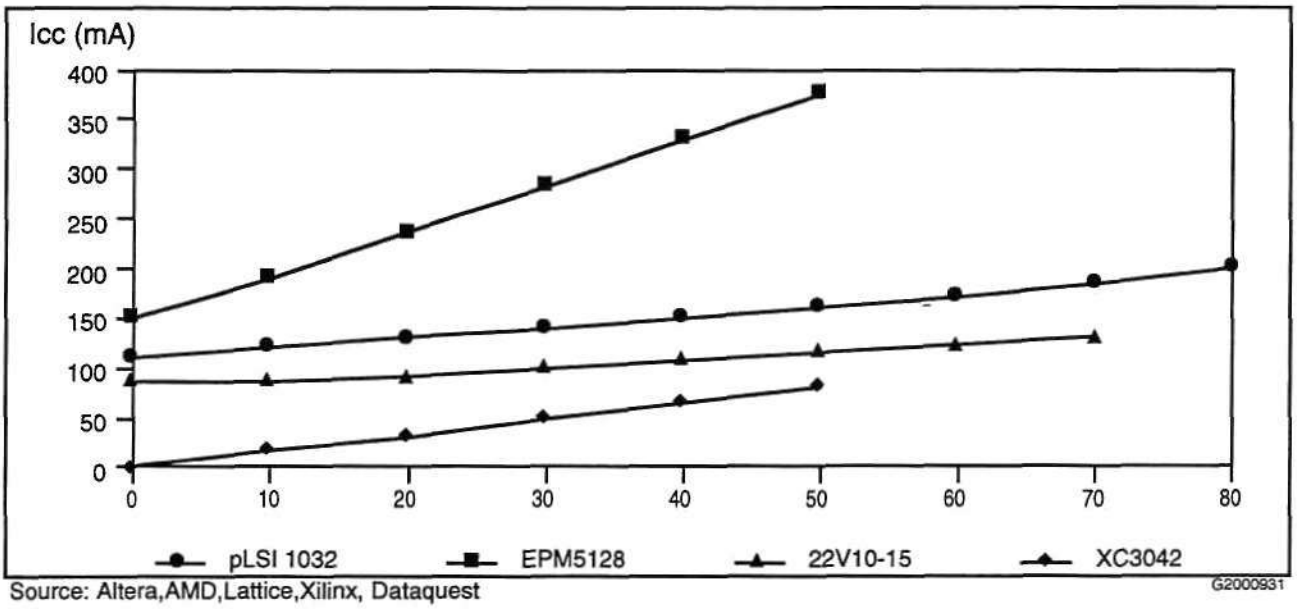
Technology Limitations

Unlike many memory and ASIC cells, product-term-based PLDs cannot be derated to operate at a 3-volt power supply. These devices are based on internal sense amps, and the amplifiers must be retuned to operate at lower voltages. Additionally, some PLDs have internal power-on reset circuitry designed to reset all flip-flops to a logical 0 state upon application of power. This is triggered at a certain point as Vcc makes its way toward 5 volts. This type of circuitry will need to be redesigned for 3.3-volt operation.

Speed Degradation

Creating a 3-volt device utilizing a 5-volt technology process will significantly decrease the

Figure 4
Typical Power Consumption of CMOS PLDs



Source: Altera,AMD,Lattice,Xilinx, Dataquest

performance of the device. By migrating to smaller channel widths and tuning the process with thinner oxides, ASIC vendors have recouped some of the lost performance. An unfortunate by-product of this shrinkage is the inability to support 5-volt operation. PLD vendors must be able to support a range of programming voltages, in some cases up to 15 volts, and it is unclear whether this may be supported with the finer geometry processes. Dataquest expects the first 3-volt devices to continue to use larger transistor widths in the programming path.

Dataquest Perspective

The combination of technology issues and slowly emerging low-volume portable applications will result in a slow emergence of the 3-volt PLD market. It is not until 3-volt-only systems become a reality that we believe there will be a significant 3-volt PLD market. We can begin to estimate the opportunity for 3-volt PLDs by examining a leading indicator market, such as microprocessors. Dataquest estimates that 35 percent of the microprocessor revenue will be based upon 3-volt devices by 1995 (see Figure 5). It is obvious that the 3-volt PLD market will be significantly less than 35 percent of the total PLD market. Dataquest believes that once 3-volt-only systems become a reality, 3-volt PLDs could garner up to 10 percent of the CMOS PLD market by 1997. As channel widths of all ICs reach about 0.5-microns, 3-volt design will become a necessity regardless of the system power requirements, and PLD vendors will need to be in position to provide 3-volt products.

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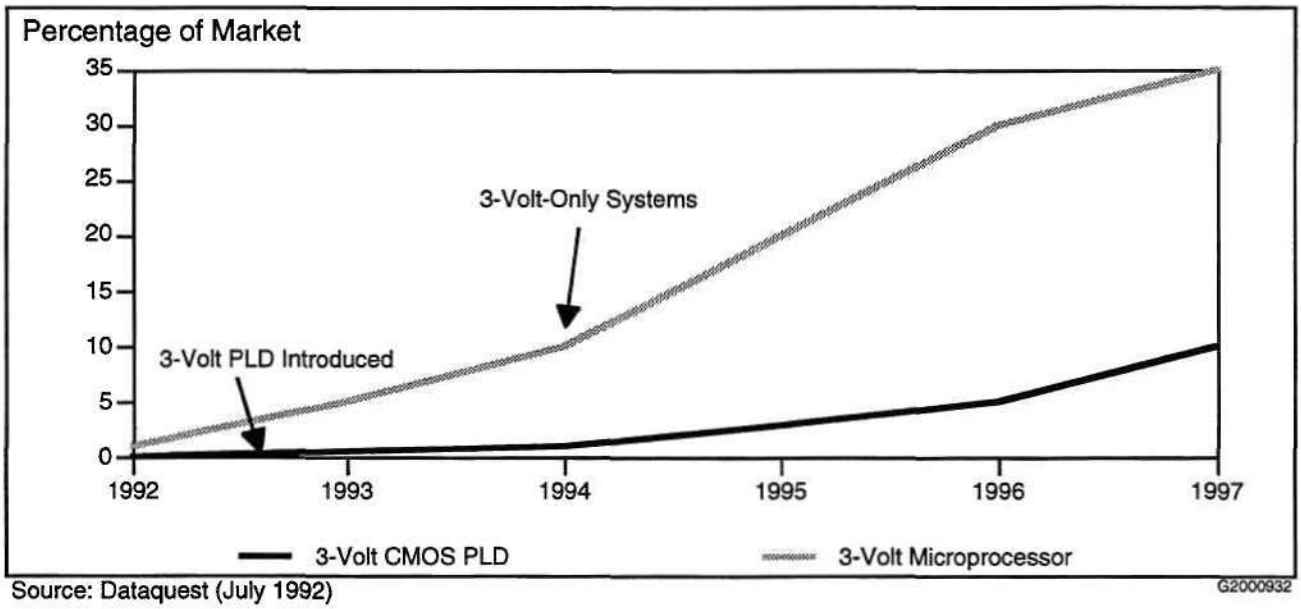
By Robert K. Beachler

Figure 5
3-Volt PLD Percentage of Total Market



Source: Dataquest (July 1992)

In Future Issues

Watch for reports on the following topics in future issues of *Dataquest Perspective:*

- PLD market analysis
- Final ASIC market share and forecast

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Dataquest Perspective

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ASICs *Worldwide*

ASIC-SEG-DP-9203 May 25, 1992

In This Issue...

Market Analysis

ASIC Design Kits: The Necessary Evil

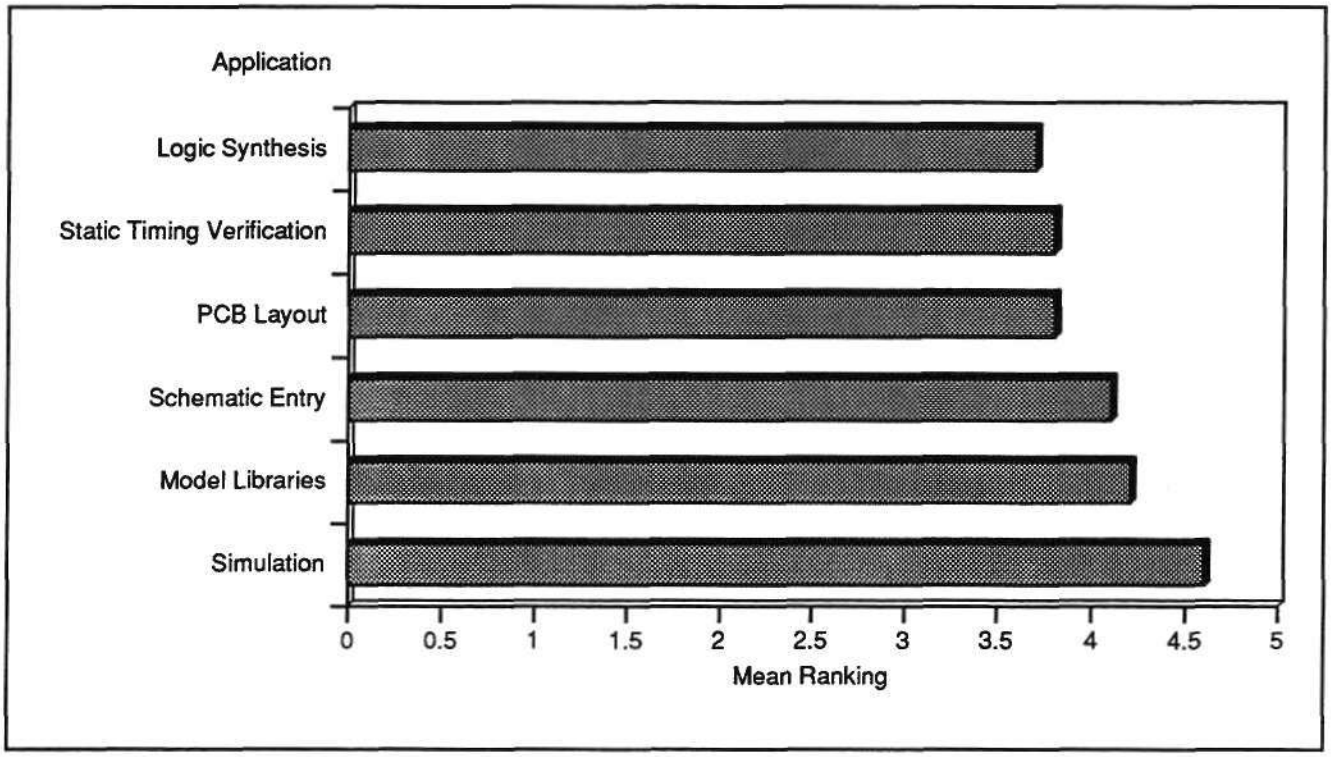
When application-specific integrated circuits (ASICs) were first introduced, ASIC vendors supplied proprietary CAE tools to enable designers to implement gate array or cell-based design. However, expensive proprietary tools were not the best solution for the end user. When third-party tools were introduced, ASIC users recognized the value in having a generic toolset that may be used to capture and analyze designs for multiple-ASIC vendors. ASIC vendors fought this trend, and it was only the combination of customer demand and third-party tool pressure that pushed the reluctant ASIC vendors into supplying library information to third-party CAE tool providers.

Gradually, third-party CAE tools supplied by Daisy, Mentor Graphics, and Valid Logic Systems became the standard tools used to implement ASIC designs, and the burden of creation of the ASIC libraries shifted from the CAE tool vendor to the ASIC supplier. Today, the ASIC vendor is spending its software development dollar, in some cases to the tune of over $1 million a year, supplying design kits and support for third-party EDA tools. This type of spending is motivated by a need in the user community. Figure 1 shows North American users' ranking of EDA applications (note that users recognize the importance of model libraries, ranking them second out of all EDA tools).

User's Perspective

Over the course of years, the ASIC user's goals have not radically changed. Dataquest research shows that the top three goals of the electronic designer are to reduce the cost of the design, increase the functionality of the design, and decrease the time it takes to implement the design. As a cost-reduction measure in these recessionary times, ASIC designers demand the flexibility of using general-purpose EDA tools to

Figure 1
EDA Tool Importance, User's Perspective



Source: Dataquest (May 1992) G2000671

create designs, and then choose the appropriate silicon vendor.

The key to shortening the design cycle is for the EDA vendor to provide more accurate simulation and timing analysis tools, and have the ASIC vendors support them. Our research into the North American electronic design cycle leads us to believe that in 48 percent of ASIC designs more time is spent tracking down timing problems than evaluating functional problems. After the ASIC prototype is received, 45 percent of ASIC designs require more timing-related debug.

EDA Vendor Perspective

The EDA vendor relies upon the existence of the ASIC library in order to sell its products. The total serviceable market for an EDA vendor correlates directly with the breadth of its ASIC library. Without the underlying cell information containing delay and area information, synthesis and simulation tools have no value.

To this end, EDA vendors have large sales and support organizations whose sole purpose is to persuade ASIC vendors to support their tools.

Yet it is only in conjunction with customer pressure that the ASIC vendor will choose to support an EDA vendor's tools. For second-tier EDA vendors, whose voice is not loud enough and whose customer base is not large enough, it means that they must resort to creating ASIC design kits themselves and submitting the finished work to the ASIC vendor for certification.

Certification, in some cases, may take as long as the actual creation of the ASIC library. Although the actual work involved to certify an ASIC library is typically three man-weeks, the total amount of time is significantly longer. Political battles, priority conflicts, and scheduling all combine to delay the actual certification of an ASIC library to up to six months.

This is not to imply that there is a dearth of ASIC design kits. Counting the ASIC support supplied by the top six EDA vendors, more than 700 ASIC libraries are supported.

ASIC Vendor Perspective

The dilemma for the ASIC vendor is an expensive one. It must provide as many design kits

for third-party tools as possible. The sole limitation is one of cost. Dataquest estimates that a simple design kit with a small number of library elements costs $50,000 to $60,000 to create. And for larger, more complex kits, the cost quickly skyrockets to hundreds of thousands of dollars.

The total cost quickly climbs as one analyzes the multiplicity of demands upon the ASIC vendor. A typical ASIC vendor on average will have at any one time 12 different technology libraries. The reasons for the multiplicity include different line widths (typically 1.5, 1.0, and 0.8µM), cell-based versus gate array, process technologies (CMOS, BiCMOS, Bipolar, and GaAs), and voltage levels (3V or 5V). On average, the ASIC vendor supports six different EDA vendors. Therefore each technology library must be re-created for six different modeling languages. It then follows that the average ASIC vendor is supporting 72 different libraries. Further complicating the picture is the fact that each EDA tool executes on a multiplicity of platforms. Not including the platform factor, this conservative model implies that the typical ASIC vendor has spent at least $4 million on ASIC libraries.

Other factors that affect the cost of ASIC library development include process geometry shrinkage and embedded cell support. As process line widths decrease, the complexity of accurately modeling the delay increases. Interconnect delays are becoming a much larger percentage of the overall path delay, and are beginning to affect the intrinsic cell delay. ASIC vendors are moving toward more sophisticated input slew modeling and more complex delay equations to improve the accuracy of simulation and timing analysis. These measures add cost to the overall library creation process. Embedded cells and supermacros also add to the library cost. In 1992, only 3 percent of gate array designs have embedded cells, but we believe this will grow to 10 percent in 1994. Additionally, almost all designs of more than 25,000 gates are using some type of megacell, either a metallized memory or datapath macro.

Future Perspective

ASIC and EDA vendors need a solution to the design kit dilemma. ASIC vendors are looking for any way to reduce their cost of doing business as competitive pressures continue to erode profit margins. EDA vendors want more ASIC vendors to support their applications so that they may expand their total serviceable market. Many have looked toward VHDL as a potential answer to the problem of supporting multiple EDA tools with just one library, but at this point VHDL only exacerbates the problem.

VHDL, or IEEE standard 1076, is supported, to some degree, by more than seven different simulators. Yet each simulator is not common in its treatment of VHDL. Some tools accept only a subset, while others tout that they support the entire standard. Additionally, there exists ambiguity in the standard itself, in terms of the logic state value set and backannotation. Each simulator supports a different set of logic values. Backannotation of delay information into VHDL code is not uniform among VHDL tools. VHDL International is working hard at trying to bring some standardization to VHDL, but it may be a few years until VHDL is at a point that it will provide a potential cost savings to the ASIC vendor.

In the short term, VHDL causes an additional support burden for the ASIC vendor. Not only must the ASIC vendor support the native language simulator of the EDA vendor, but it must now also support the VHDL language simulator. Dataquest estimates that this costs the ASIC vendor an added expense of $25,000 to $30,000 per VHDL simulator supported.

Assuming that VHDL reaches a point of true standardization, the true cost saving to the ASIC vendor is significant. Dataquest estimates that for a basic design kit, cost reduction of about 50 percent could be realized by using VHDL as the simulation modeling language for all its ASIC design kits. However, for a more extensive design kit, including software utilities such as delay calculators and design rule checkers, the cost saving is more like 20 percent. For an increasingly margin-sensitive business, ASIC vendors should consider the substantial cost savings that migrating to an all-VHDL modeling method would provide, once the technical barriers are overcome.

Dataquest Perspective

Dataquest believes that the recent consolidation in the EDA market will have a limited impact on the cost of supporting ASIC design kits. While the number of broad-based EDA vendors

is decreasing, the number of new tools being brought to bear upon the ASIC design problem is increasing, and ASIC vendors are being pressured by users to support them. The added need for increased accuracy, in combination with the market pressure to differentiate ASIC products with margin-improving embedded cells and megacells, is driving up the cost of developing ASIC libraries.

VHDL holds promise as a long-term cost reducer, but current technical limitations will not allow it to be used in a way to solve the ASIC vendor's cost problem. However, ASIC manufacturers should continue to periodically evaluate VHDL in terms of technical capability and market mass in order to determine the best time to move to a VHDL-based modeling scheme.

By Robert K. Beachler

In Future Issues

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- PLD market analysis

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Dataquest Perspective

ASICs *Worldwide*

ASIC-SEG-DP-9202 April 27, 1992

In This Issue...

Market Analysis

An Update from the HDL Front

Dataquest's research of the electronic design market indicates that the momentum behind the VHSIC Hardware Description Language (VHDL) is accelerating. Not only is this the case in North America, but Japan-based electronics suppliers have also begun throwing greater support behind the IEEE standard. As a result, we continue to stand by our projection that VHDL's market share will increase dramatically during the next three years.

While VHDL is gaining strength, the Verilog hardware description language (HDL), which is the primary alternative to VHDL, is showing signs of weakness. Despite the efforts of both Cadence and the Open Verilog International (OVI) consortium to strengthen the language's market position, it is clear that Verilog HDL has been able to expand its market perception (as a long-term standard) only marginally over the past six to nine months. This conclusion is based on Dataquest research showing that although Verilog will retain a significant portion of its current user base over the next few years, VHDL will capture most new users adopting the top-down design methodology, *provided that the VHDL-based products meet the market's performance expectations*. Nonetheless, in our view, Verilog HDL will remain a force in the marketplace for *at least* the next two to three years, especially in light of Cadence's recent acquisition of the Valid Logic installed base.

Whether OVI and other Verilog HDL champions are able to arrest, or at least slow, the VHDL tide remains to be seen. This research examines the current and projected market dynamics impacting the various HDLs.

HDL Market Dynamics

With HDL-based top-down design moving steadily into the mainstream electronic design

arena, electronics manufacturers are increasingly selecting VHDL as the language of choice. Selection of VHDL over Verilog HDL stems not from any particularly superior capabilities of the language—in fact it is somewhat inferior in many ways—but rather because VHDL is perceived by the market to be fully endorsed and heavily supported by most electronic design automation (EDA) and ASIC suppliers. The upshot is that the collective market power of the EDA and ASIC suppliers promoting VHDL has overshadowed the attempts initiated by Verilog HDL proponents to sustain its momentum. Furthermore, we believe that Cadence failed to seize upon a window of opportunity in 1991 to significantly bolster Verilog HDL's market position. The company's seemingly laissez-faire attitude toward Verilog HDL standardization during that time has been a boon to most opponents of Verilog HDL. In our view, this is somewhat unfortunate, given Verilog HDL's ease of use, production-proven status, growing third-party support, ASIC library support, and general popularity among users.

Despite the trend toward VHDL, many electronics manufacturers continue adopting Verilog HDL. We estimate that Cadence sold an additional 1,500 to 1,800 Verilog-XL simulator licenses in 1991. This brings the installed base to approximately 5,500 single- and multiple-user licenses, which translates to 10,000 to 15,000 users of the Verilog-XL simulator. It is important to note, however, that only a portion of the Verilog-XL user base can be viewed as "sophisticated" users of the Verilog HDL. In this context, we estimate that only 30 percent to 35 percent of the 10,000 to 15,000 Verilog-XL users can be considered familiar enough with the language to use it as a design entry vehicle for a top-down design.

Furthering the Verilog HDL cause, several small EDA vendors, including both established companies and start-up ventures, are developing EDA products based on Verilog HDL. Yet to date, none of the larger EDA vendors has announced support for Verilog HDL. Lack of endorsement by the bigger players remains a significant impediment to Verilog HDL standardization, although less so than it did six months ago. Since then Cadence acquired Valid Logic, which significantly boosted the company's market power in the HDL arena. Many users of the Valid Logic CAE system that at one time would have migrated directly to VHDL are now likely to evaluate and perhaps adopt Verilog HDL.

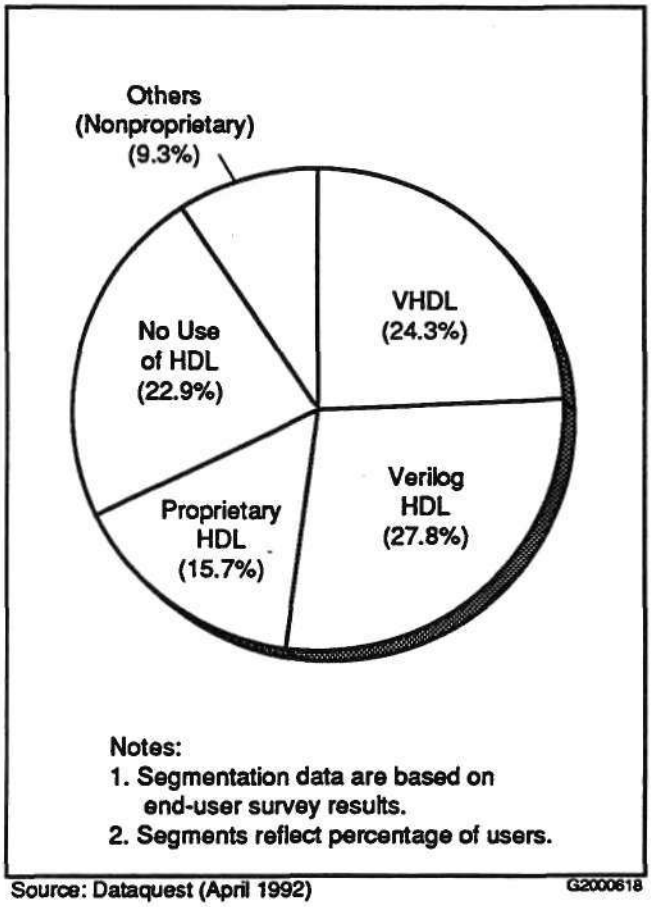
Still, companies such as Dazix, Mentor Graphics, Racal-Redac, and Viewlogic have not endorsed Verilog HDL. To do so would bolster Verilog HDL's market position, which ostensibly would also strengthen Cadence. Thus, most of Cadence's competitors are loath to support Verilog HDL. In addition, Synopsys, an early and strong advocate of Verilog HDL, has been vigorously promoting VHDL since its acquisition of the Zycad VHDL-based simulation product line in October 1990. Not surprisingly, the company has been gradually distancing itself from the Verilog HDL. Although Synopsys is dwarfed by Cadence and Mentor Graphics, the company has played a central role on the HDL battlefield. Indeed, Synopsys can be credited with helping to establish Verilog HDL as a de facto standard in the marketplace. In our view, Synopsys' market power and its ability to influence the direction of the HDL trends will continue to expand as a result of its nearly unfettered penetration of the logic synthesis market.

HDL Market Share in North America and Japan

Dataquest's most recent research in North America and Japan (conducted in the second half of 1991) shows the market share of the various HDLs currently in use. The research was conducted by surveying managers and engineers at several hundred electronic design sites, most of which have 500 employees or more. The survey sample consisted of current users of EDA tools that run on both technical workstations and personal computers. The pie chart in Figure 1 indicates that the percentages of Verilog HDL users and VHDL users in North America are approximately equal. Figure 2 illustrates the current HDL market share in Japan and shows that Verilog HDL currently holds the leadership position in the Japanese market.

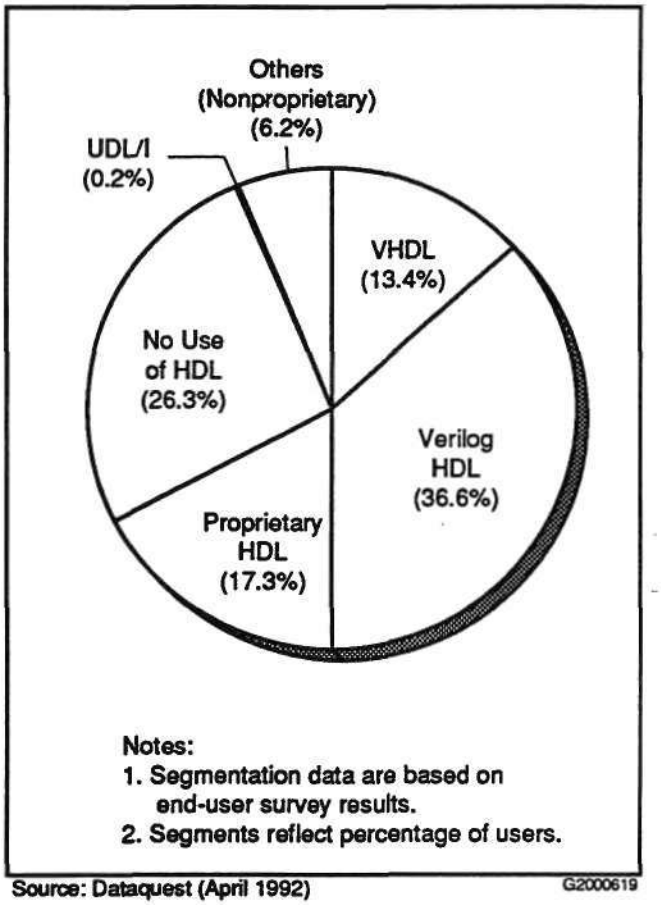
It is important to note that the data in Figures 1 and 2 were not captured using a bottom-up approach and, thus, may be somewhat less accurate than a survey of VHDL product suppliers. However, the data correlate well with our bottom-up market share analysis conducted in early 1991 (see the CAD/CAM newsletter entitled "The HDL Showdown: VHDL versus Verilog HDL," April 1991), which shows approximate parity between VHDL and Verilog HDL.

Figure 1
1991 North American HDL Market Segmentation



Source: Dataquest (April 1992) G2000618

Figure 2
1991 Japanese HDL Market Segmentation



Source: Dataquest (April 1992) G2000619

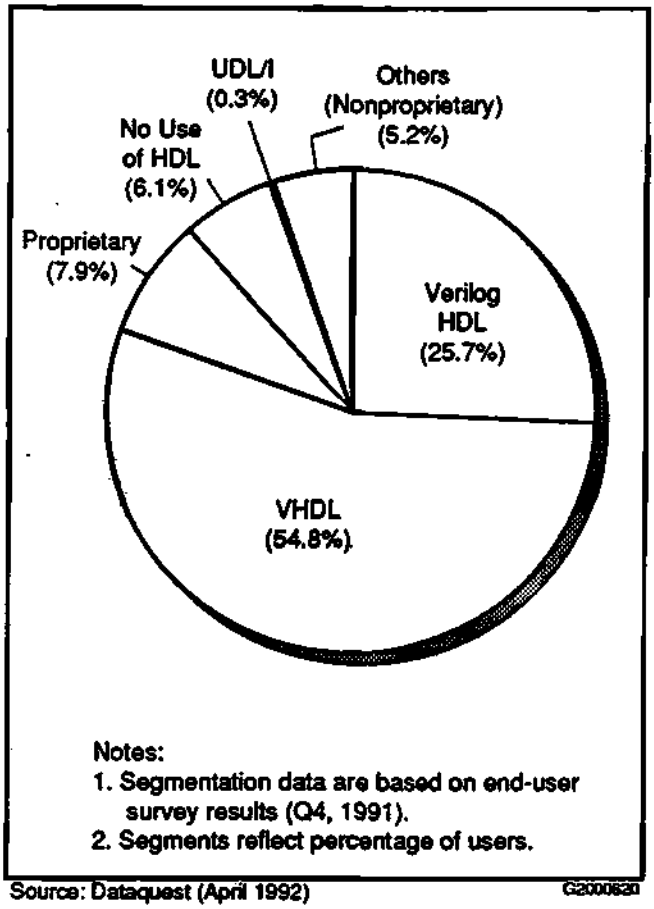
Historical and projected market share figures published in April 1991 show worldwide figures, as opposed to a regional segmentation. At the worldwide level, our figures show that the market shares of Verilog HDL and VHDL were nearly equivalent. This is based on our estimate that Verilog HDL and VHDL's North American market shares were approximately equal, whereas in Japan, Verilog HDL held a significant edge; in Europe, a less exhaustive study indicated that VHDL held a significant advantage over Verilog HDL.

North American Outlook

Among the most significant issues facing EDA software vendors and ASIC suppliers is determining how the HDL landscape will shift over the next three years. Dataquest's most recent studies shed light on the subject. Figure 3 shows the projected market share of the various HDLs in North America. The chart was generated by surveying electronic design groups at over 250 different sites throughout North America. Engineers and managers were asked which HDL they planned to use for their next-generation design. The results show that an overwhelming percentage plan to adopt VHDL.

Despite the strong response favoring VHDL, it is important to recognize that VHDL-based tools will realize their market share potential only if they fulfill the market's performance requirements. The data in Figure 3 is simply a reflection of the market's current thinking. Our assumption underlying the data is that VHDL's performance problems will be resolved and that the ASIC libraries will be available for VHDL tools. Most EDA vendors maintain that VHDL-based tools will deliver the necessary performance requirements, but users still complain about VHDL's slow simulation speed and excessive memory requirements. We believe that these performance issues will be resolved, given the

Figure 3
Projected 1995 North American HDL Market Segmentation



Source: Dataquest (April 1992) G2000820

enormous research and development efforts being put forth by VHDL advocates. Moreover, even if these efforts produce less-than-satisfactory results, skyrocketing compute performance and dramatic improvements in price/performance of compute platforms will substantially mitigate the problems.

As an indication of the market's desire to hedge its bet on VHDL, our research confirms that much of the Verilog HDL installed base plans to adopt VHDL without disposing of Verilog HDL. Indeed, approximately 82 percent of the Verilog HDL-only installed base in North America (those that are using Verilog HDL and have not adopted VHDL) will continue using Verilog HDL over the next two to three years, if not longer. Only 18 percent plan to replace it with VHDL. Indicative of an emerging trend toward coexistence between Verilog HDL and VHDL, 27 percent of the Verilog HDL-only installed base plans to adopt VHDL and use both Verilog HDL and VHDL for at least the next two years. However, 55 percent of the Verilog-only users will continue using the language in the absence of VHDL. In sum, about half of the the Verilog HDL-only installed base will continue to cast its loyalty exclusively toward Verilog HDL. The other half will either forsake Verilog HDL for VHDL or adopt both languages.

Among the current base of VHDL-only users in North America (those that are using VHDL and have not adopted Verilog HDL), less than 2 percent plan to replace VHDL with Verilog HDL. However, approximately 6 percent of the VHDL-only user base will also adopt Verilog HDL and use both languages.

In the North American electronic design market, adoption rates of VHDL will be fastest in the military and aerospace industries, which is not surprising given that VHDL development was funded and later mandated by the U.S. Department of Defense. What is perhaps surprising, however, is that the computer industry, which is a Verilog HDL stronghold, will also begin to aggressively adopt VHDL. Today, only 10 percent of the computer industry is using VHDL. We expect this figure to reach at least 40 percent during the next 18 to 24 months.

Widespread adoption of VHDL is also expected among North American semiconductor manufacturers. Approximately one-third of the industry has already begun using VHDL. Our research indicates that at least 50 percent to 60 percent of the semiconductor sector will be using it by the end of 1994.

VHDL will also make significant inroads into the communications equipment design arena. Approximately 25 percent of the communications industry has adopted VHDL, but this figure will more than double over the next two years.

Japanese Outlook

From 1989 through 1991, the Japanese market wavered in its support of any particular HDL, although the tendency was moving toward Verilog HDL during that period. We believe that the bias favoring Verilog HDL was (and is) a by-product of the ubiquitous presence of the Verilog

HDL-based simulator, Verilog-XL, which expanded significantly once Cadence put its distribution muscle behind it (after acquiring the technology from Gateway Design Automation). It was natural for users of the Verilog-XL simulator to favor adoption of the complementary Verilog HDL. Current HDL market share reflects Cadence's overall strength in the Japanese market—strength that is rooted in Cadence's stronghold on the IC design market.

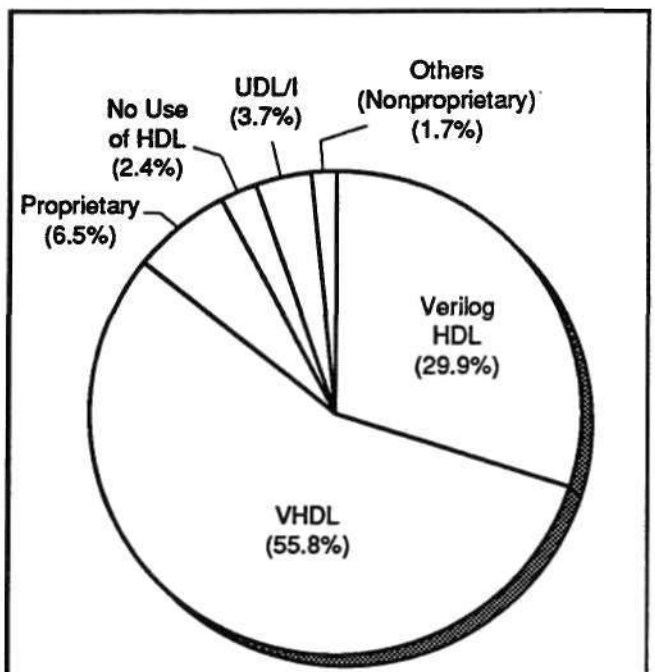
Our studies conclude that approximately 34 percent of the Verilog HDL-only installed base will replace the language with VHDL. Thus, coexistence between VHDL and Verilog HDL is projected to be widespread in Japan, with 53 percent of the Verilog HDL-only user base planning to use both Verilog HDL and VHDL. Only 13 percent will continue to use Verilog HDL exclusively—that is, without adopting VHDL.

The number of VHDL-only users in Japan is currently too small to draw any solid conclusions, but early indications suggest that 10 percent to 20 percent may displace it with Verilog HDL, and another 15 percent to 25 percent will end up using both Verilog HDL and VHDL. The upshot is that we expect approximately 60 percent of the VHDL-only base to use VHDL exclusive of Verilog HDL.

Reaction to VHDL among most Japanese manufacturers over the past few years has been less than positive. Negative perceptions about the language among Japanese manufacturers have been shaped by a number of factors. For instance, VHDL's DoD roots were viewed somewhat negatively. Electronics manufacturers believed that the language did not meet the needs of the commercial sector. Indeed, because VHDL was initially developed as a documentation language, many of its constructs did not lend themselves to either simulation or logic synthesis. Furthermore, VHDL was more difficult to use than other languages: Its gate-level simulation speed was slow; the standard itself was open to interpretation; and applications were being developed for unique subsets of the language, which potentially precluded the mixing and matching of VHDL-based tools from different vendors. Moreover, early widespread endorsement of VHDL among EDA vendors was viewed by Japan-based electronics manufacturers as a preemptive response aimed at curbing the expanding presence of Cadence's Verilog HDL. In sum, VHDL was perceived as language unable to meet the needs of the customer, but nonetheless was being forced upon the market by the U.S. government and an array of EDA suppliers determined to weaken Verilog HDL's market position.

Many of the problems and stumbling blocks surrounding VHDL persist today. Yet, the collective market power of the VHDL camp, which consists not only of EDA vendors but also of ASIC suppliers, has eclipsed much of the momentum previously garnered by the Verilog HDL. Figure 4, which shows the projected market share of the various HDLs in Japan, serves as a clear indicator of the collective mind-set of the Japanese electronics industry. This figure reflects the survey responses from electronic design groups at over 100 different sites throughout Japan. Engineers and managers

Figure 4
Projected 1995 Japanese HDL Market Segmentation



Notes:
1. Segmentation data are based on end-user survey results (Q4, 1991).
2. Segments reflect percentage of users.

Source: Dataquest (April 1992) G2000621

were asked which HDL they planned to use for their next-generation design. The results show that an overwhelming percentage plan to adopt VHDL. Conversely, although the Verilog HDL base will grow by 15 percent to 20 percent, its market share vis-a-vis VHDL in Japan will decline significantly.

Recent shifts toward VHDL within the Japanese market stem from widespread EDA industry support of the language, as well as a large number of VHDL products being introduced into the market. Acquiescence toward VHDL and its projected coexistence with Verilog HDL is also a reflection of the fact that Japanese manufacturers are willing to accept VHDL on a trial basis but are unwilling to replace Verilog HDL with VHDL at this point. Our research shows that adoption of VHDL will be strongest in the automotive, computer, and semiconductor industries. Coexistence between Verilog HDL and VHDL will be widespread in the semiconductor industry, a current stronghold of Verilog HDL.

UDL/I HDL, which was injected into the public domain but was originally developed as a proprietary language primarily by NTT Laboratories in Japan, has yet to capture the market's attention. We stand by our projection that the earliest possible opening of a significant market window for UDL/I will be in 1995 or 1996.

Dataquest Perspective

Although Verilog HDL's market position has been bolstered by both its injection into the public domain and the creation of the OVI consortium, Dataquest believes that Cadence has not applied the necessary marketing, promotion, or support over the past nine months to emerge from the shadow cast by VHDL. Were it not for the fact that Cadence acquired Valid Logic, we would be inclined to believe that Verilog HDL's market position would erode even faster as a result of Cadence's limited efforts. However, the acquisition has the potential to significantly expand both the life span and market size of Verilog HDL. Even before the acquisition, usage of Verilog HDL within the Valid Logic installed base was widespread. With direct access to non-Verilog HDL customers in the Valid Logic base, Cadence is in a better position to persuade a significant percentage to adopt Verilog HDL. Of course, it should be pointed out that Cadence offers both Verilog HDL and VHDL-based products.

OVI has also been stepping up its efforts to strengthen Verilog HDL's position, as follows:

- OVI has become a distributor of a restricted version (protected against reverse engineering) of the Verilog simulator that can be used to validate third-party Verilog HDL-based tools.
- Several Verilog HDL manuals have also been created, including a language reference manual and a programming language interface manual.
- A recently held user group meeting attracted several hundred attendees and approximately 20 vendors on the exhibition floor.
- OVI's membership has burgeoned to nearly 50 members.
- A test technical subcommittee has been established to identify and address test requirements as they pertain to Verilog HDL.
- Several discussions are under way within the various technical subcommittees to determine what, if any, extensions should be incorporated into the language.

Even more significant is OVI's recent decision to begin pressing the IEEE to accept the Verilog HDL as a standard hardware description language.

Finally, an increasing number of start-up ventures have begun investigating and/or developing EDA products based on the Verilog HDL. Fledgling companies in this camp are motivated by the prospect of penetrating the large Verilog-XL simulation installed base. With all of the activity surrounding both Verilog HDL and VHDL, Dataquest believes that the two languages will coexist over the next several years, if not longer. We estimate that by 1996 there will be over 30,000 users of Verilog HDL and VHDL (see Figures 5 and 6).

The opportunity for EDA vendors is to offer the market tools and environments that support this paradigm. Indeed, the market opportunity for language-independent tools portends to be rich.

By Ron Collett

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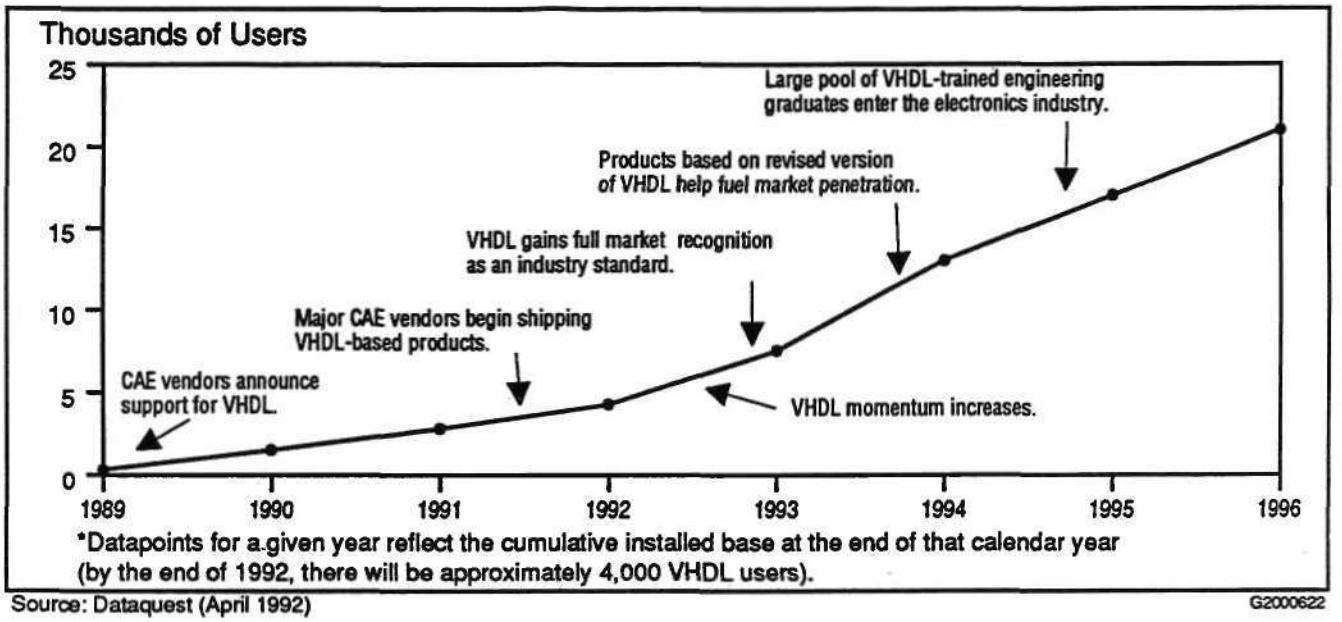
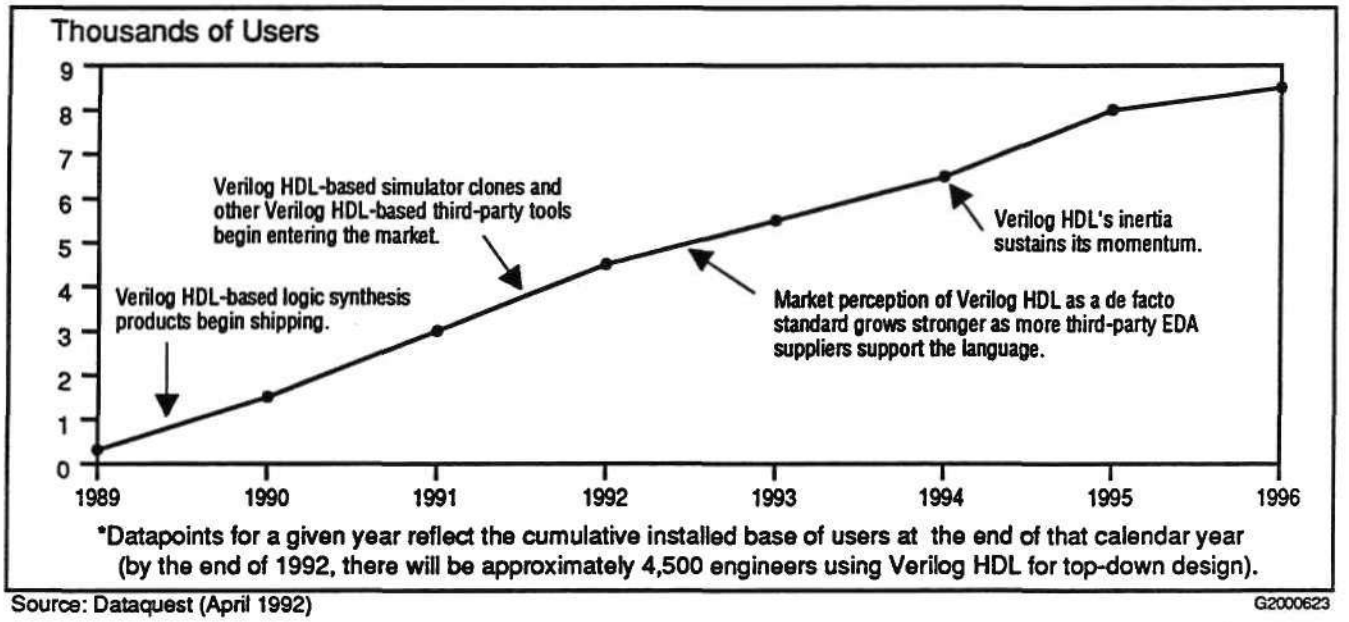
Figure 5
Projected Installed Base of VHDL Users*



Source: Dataquest (April 1992) G2000622

Figure 6
Projected Installed Base of Verilog HDL Users*



Source: Dataquest (April 1992) G2000623

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Dataquest Perspective

ASICs *Worldwide*

ASIC-SEG-DP-9201 February 10, 1992

In This Issue...

Market Analysis

1991 ASIC Market Share Estimates Show Domination by Vertically Integrated System Suppliers

Dataquest's preliminary market share estimates of the 1991 top 10 total worldwide ASIC suppliers shows that the top five suppliers derived the majority of their revenue from gate array sales (see Figure 1). Again, market estimates reveal that users prefer gate arrays over the highly touted cell-based ICs (CBICs). Fujitsu continues its reign as the No. 1 ASIC supplier; however, NEC, Toshiba, and Hitachi all gained significant market share during 1991. AT&T and Hewlett-Packard focused on the CBIC market and did not have the success experienced by the gate array suppliers. AMD, which derives the majority of its revenue from programmable logic devices (PLDs), was the only top 10 ASIC supplier to experience a decline in total ASIC revenue.

This article first analyzes the 1991 market share data by product, then examines the market potential of the different types of ASIC suppliers.

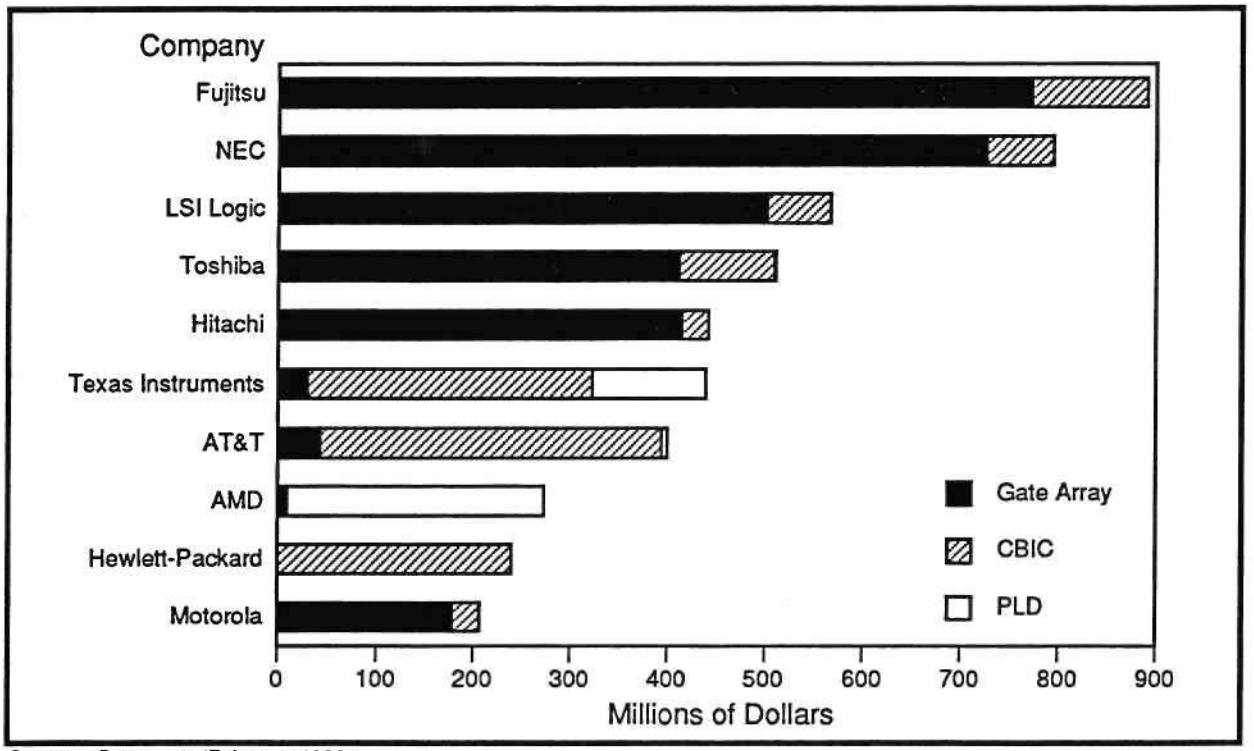
1991 Market Share Rankings

Table 1 shows Dataquest's preliminary 1991 estimates of the top 20 worldwide total ASIC suppliers with their respective revenue and market shares.

Important points regarding ASIC market share rankings include the following:

- On average, Japanese companies grew faster than most North American companies in 1991 for the following reasons:
  - The yen appreciated against the U.S. dollar.
  - Japanese companies increased intracompany sales.
  - Consumer product sales flourished in Japan.

Figure 1
1991 Top 10 Worldwide ASIC Suppliers



Source: Dataquest (February 1992)

- The 1991 North American ASIC market experienced little growth in comparision with Japan and Europe. Japan experienced high consumer spending for the first three quarters of 1991.
- The recession in North America negatively impacted the growth of most ASIC suppliers.
- Saturation of the PC and disk drive markets hurt many gate array and CBIC suppliers.
- Many ASIC suppliers have shifted focus from revenue growth to increasing profitability.

The following are footnotes to the ASIC market share estimates:

- Rankings are based on dollar shipments, which include the following five sources of revenue:
  - Intracompany revenue (sales to internal divisions)
  - Nonrecurring engineering (NRE) revenue
  - ASIC software revenue
  - PLD development kit revenue
  - Device production revenue
  - Note: Compass Design Automation's software sales are excluded from VLSI Technology's 1991 ASIC revenue estimates.
- Full custom IC revenue is excluded from ASIC market share.
- ASIC product revenue is based on the combined revenue from digital, mixed analog/digital, and analog products.
- MOS rankings include the sales of CMOS, NMOS, and BiCMOS.
- Total rankings include the sales of CMOS, NMOS, BiCMOS, and bipolar.
- The U.S. dollar appreciated 2.9 percent against the European currency unit (ECU) during 1991. Dataquest's exchange rates are U.S.$1 = 0.79 ECU in 1990 and U.S.$1 = 0.81 ECU in 1991.
- The yen appreciated 5.6 percent against the U.S. dollar during 1991. Dataquest's exchange rates are U.S.$1 = ¥144 in 1990 and U.S.$1 = ¥136 in 1991.

Table 1
Preliminary Estimated Market Share Ranking: Worldwide Total ASIC (Millions of Dollars)

1991 Rank	1990 Rank		1990 Revenue	1991 Revenue	Percent Change	1991 Market Share (%)
1	1	Fujitsu	884	891	1	12.0
2	2	NEC	668	795	19	10.7
3	3	LSI Logic	507	567	12	7.6
4	4	Toshiba	419	511	22	6.9
5	6	Hitachi	372	442	19	6.0
6	5	Texas Instruments	378	439	16	5.9
7	7	AT&T	366	400	9	5.4
8	8	Advanced Micro Devices	306	273	-11	3.7
9	9	Hewlett-Packard	230	239	4	3.2
10	11	Motorola	196	207	6	2.8
11	10	VLSI Technology	211	203	-4	2.7
12	12	GEC Plessey	156	178	14	2.4
13	14	Oki	117	136	16	1.8
14	22	Matsushita	70	132	89	1.8
15	17	Xilinx	84	130	55	1.8
16	13	National Semiconductor	141	127	-10	1.7
17	15	Seiko Epson	115	124	8	1.7
18	20	Altera	78	108	38	1.5
19	16	NCR	104	100	-4	1.3
19	18	SGS-Thomson	80	100	25	1.3

Source: Dataquest (February 1992)

Product Overview

The worldwide ASIC market (excluding full custom revenue) grew 11 percent over 1990 to $7.42 billion. Figure 2 presents the composition of the ASIC market by product and shows that gate arrays continue to dominate the market.

Gate Arrays

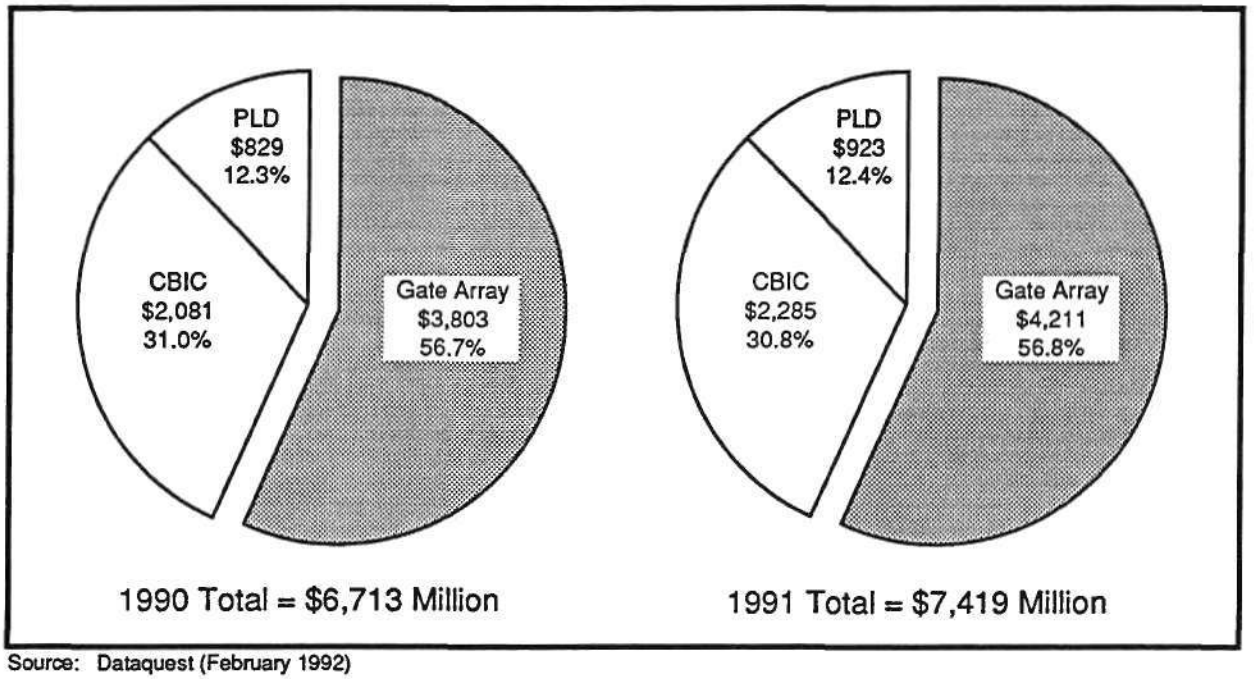
The year 1991 was one of change for the gate array industry. NEC surpassed LSI Logic and is now the largest worldwide MOS gate array supplier. VLSI Technology revenue growth shifted from CBICs to gate arrays. The 1991 worldwide bipolar gate array market declined (4 percent) for the first time because of the sluggish mainframe computer market. One market dynamic that did not change was that the MOS gate array market continued to outpace the semiconductor market with 17 percent growth in 1991.

Figure 3 shows the top 10 1991 worldwide gate array supplier revenue by technology. Table 2 shows the hotly contested top 20 1991 worldwide MOS gate array suppliers and their respective revenue and market shares.

Noteworthy points regarding the 1991 gate array rankings include the following:

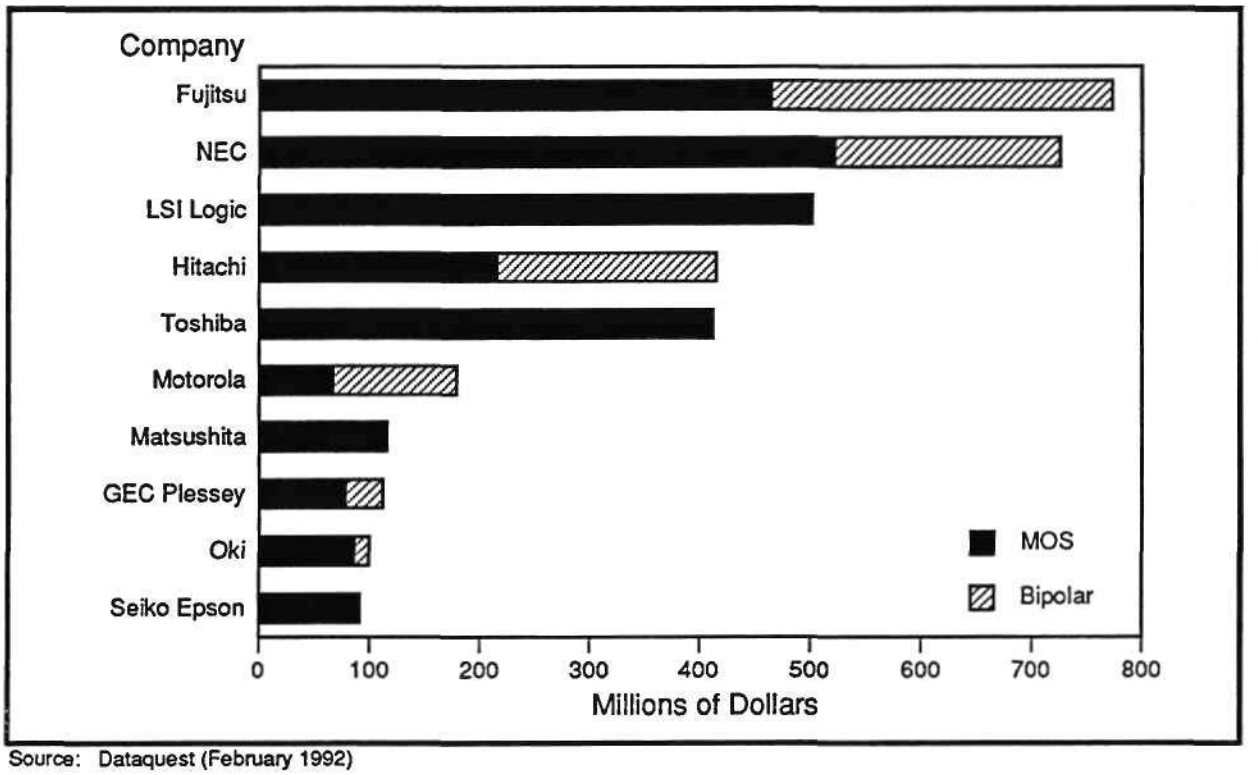
- While Fujitsu maintained its No. 1 position in total gate arrays, NEC (the No. 2 supplier) closed the the gap, growing 15 percent in 1991 total gate array sales compared with Fujitsu's zero growth. Fujitsu's low 1991 growth can be attributed to the company's poor year in bipolar gate arrays. Its bipolar gate array revenue declined 19 percent from 1990. NEC BiCMOS gate array revenue was reported incorrectly in 1990 and was corrected for 1991 market share rankings.

Figure 2
Preliminary Estimated 1991 Worldwide ASIC Consumption, by Product (Millions of Dollars)



Source: Dataquest (February 1992)

Figure 3
1991 Top 10 Worldwide Gate Array Suppliers



Source: Dataquest (February 1992)

Table 2
Preliminary Estimated Market Share Ranking: Worldwide MOS Gate Array (Millions of Dollars)

1991 Rank	1990 Rank		1990 Revenue	1991 Revenue	Percent Change	1991 Market Share (%)
1	2	NEC	445	522	17	16.8
2	1	LSI Logic	464	502	8	16.2
3	3	Fujitsu	397	465	17	15.0
4	4	Toshiba	332	412	24	13.3
5	5	Hitachi	185	216	17	7.0
6	9	Matsushita	66	115	74	3.7
7	11	VLSI Technology	54	91	69	2.9
7	7	Seiko Epson	80	91	14	2.9
9	6	Oki	86	86	0	2.8
10	8	GEC Plessey	69	78	13	2.5
11	12	Motorola	41	67	63	2.2
12	9	National Semiconductor	66	59	-11	1.9
13	13	Sharp	38	45	18	1.5
14	13	Mitsubishi	38	43	13	1.4
15	15	SGS-Thomson	35	38	9	1.2
16	16	Texas Instruments	23	28	22	0.9
17	17	Matra MHS	20	22	10	0.7
18	18	Rohm	15	19	27	0.6
19	21	NCR	12	15	25	0.5
19	30	Samsung	5	15	200	0.5

Source: Dataquest (February 1992)

- LSI Logic lost market share in worldwide MOS gate arrays, falling from 17.5 percent market share in 1990 to 16.2 percent in 1991. LSI Logic continued to focus on profitability rather than just revenue growth.
- Motorola had a healthy 63 percent gain in 1991 MOS gate array revenue. However, the company also experienced a 14 percent decline in 1991 bipolar gate array revenue.
- A significant increase in high-volume consumer products accounted for Matsushita's dramatic increase in MOS gate array revenue.
- VLSI Technology jumped to the No. 7 position in the 1991 MOS gate array ranking, up from its No. 11 spot in 1990. This rise in ranking is because the company introduced a new gate array product as well as converted some CBIC business to gate arrays.
- Texas Instruments' BiCMOS gate arrays are fueling its MOS gate array growth.
- Samsung is the first Korean supplier to rank in the top 20 of MOS gate array suppliers. Korean suppliers have targeted the gate array market for future growth.

Cell-Based ICs

The year 1991 was unexpectedly slow for the overall cell-based IC market, with only 10 percent growth over 1990. MOS CBICs accounted for 98 percent of the total 1991 CBIC market. The 1991 worldwide MOS CBIC experienced a modest 11.5 percent growth over 1990, whereas bipolar CBICs declined by 37 percent. Saturation of the PC and disk drive markets contributed to this slow year.

Figure 4 shows the top 10 1991 worldwide CBIC supplier revenue by technology. Table 3 shows the top 20 1991 worldwide MOS CBIC suppliers by their respective revenue and market shares.

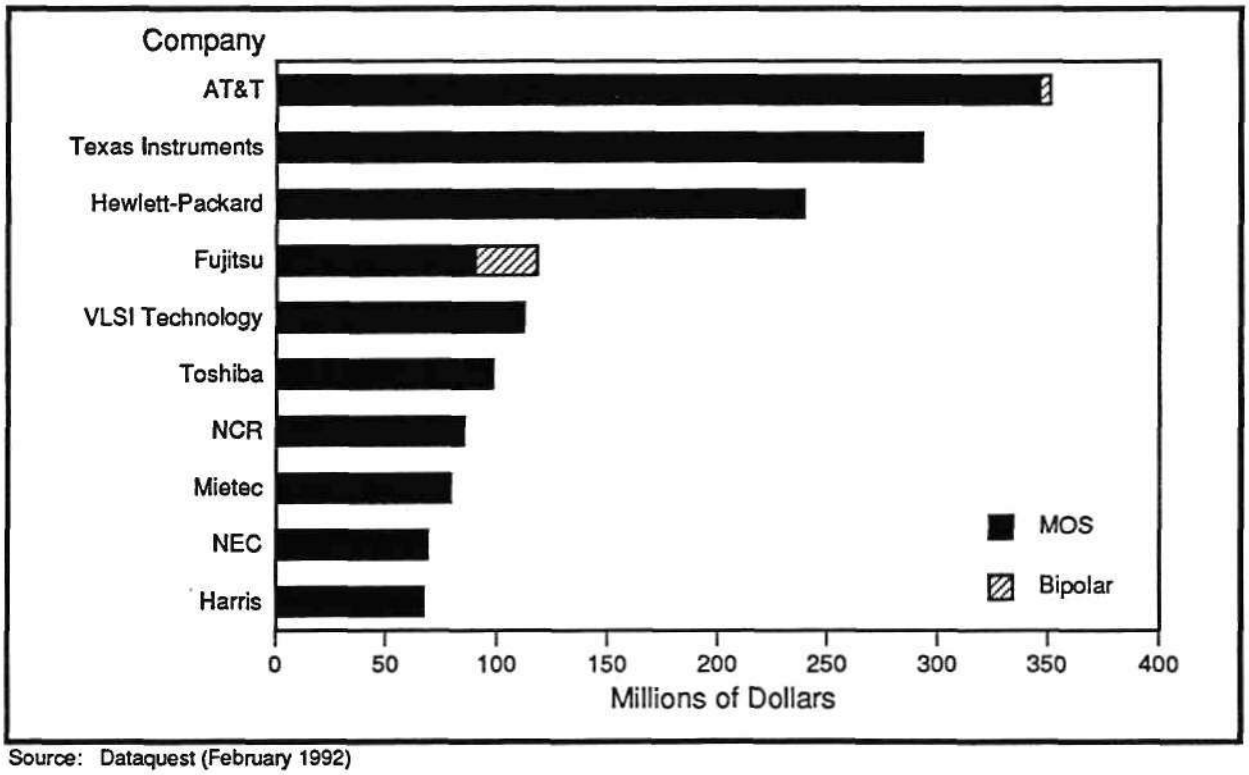
Noteworthy points regarding the 1991 CBIC rankings include the following:

- AT&T remained the leader in worldwide CBIC revenue. However, saturation of the PC and disk drive markets limited its growth.
- Texas Instruments' growth surpassed that of the worldwide CBIC market because the company increased its penetration in the rapidly expanding Japanese market.
- VLSI Technology's CBIC revenue decline stems not only from the conversion of some of its CBIC business to gate array sales, but also from Compass Design Automation's revenue being excluded from its CBIC revenue for the first time. If Compass' revenue had been included in the 1991 CBIC estimate, the company's CBIC growth would have been relatively flat.
- Toshiba and Fujitsu outpaced the CBIC market by increasing their market share in Japan. Increased market share was achieved by focusing on high-volume applications including video games, printers, and disk drives.
- Mietec's high CBIC growth is because of BiCMOS product sales primarily to European telecom equipment suppliers.
- NEC's high CBIC growth is being fueled by internal consumption and by increases in its merchant sales.

PLDs

Some segments of the PLD market were vibrant while others were sluggish during 1991. Although the MOS PLD market outpaced the entire semiconductor industry with a robust 39 percent growth over 1990, revenue from the bipolar PLD market fell 15 percent. Most PLD suppliers experienced a slowdown in the fourth quarter because of the recession and product transitions that reduced their 1991 annual growth rate. The 1991 worldwide PLD

Figure 4
1991 Top 10 Worldwide CBIC Suppliers



Source: Dataquest (February 1992)

Table 3
Preliminary Estimated Market Share Ranking: Worldwide MOS Cell-Based IC (Millions of Dollars)

1991 Rank	1990 Rank		1990 Revenue	1991 Revenue	Percent Change	1991 Market Share (%)
1	1	AT&T	316	346	9	15.5
2	2	Texas Instruments	230	293	27	13.1
3	3	Hewlett-Packard	230	239	4	10.7
4	4	VLSI Technology	157	112	-29	5.0
5	6	Toshiba	86	98	14	4.4
6	7	Fujitsu	78	90	15	4.0
7	5	NCR	92	85	-8	3.8
8	9	Mietec	50	79	58	3.5
9	14	NEC	35	69	97	3.1
10	8	Harris	69	67	-3	3.0
11	11	LSI Logic	43	65	51	2.9
12	13	GEC Plessey	38	64	68	2.9
13	12	SGS-Thomson	40	55	38	2.5
14	10	Int'l Microelectronic Products	48	38	-21	1.7
15	26	Oki	19	37	95	1.7
16	18	European Silicon Structures	27	34	26	1.5
17	16	Seiko Epson	31	33	6	1.5
18	17	Gould AMI	27	33	22	1.5
19	15	Austria Mikro Systeme	33	31	-6	1.4
20	20	Sierra Semiconductor	24	29	21	1.3

Note: Compass Design Automation's software sales are excluded from VLSI Technology's 1991 cell-based IC revenue estimate.
Source: Dataquest (February 1992)

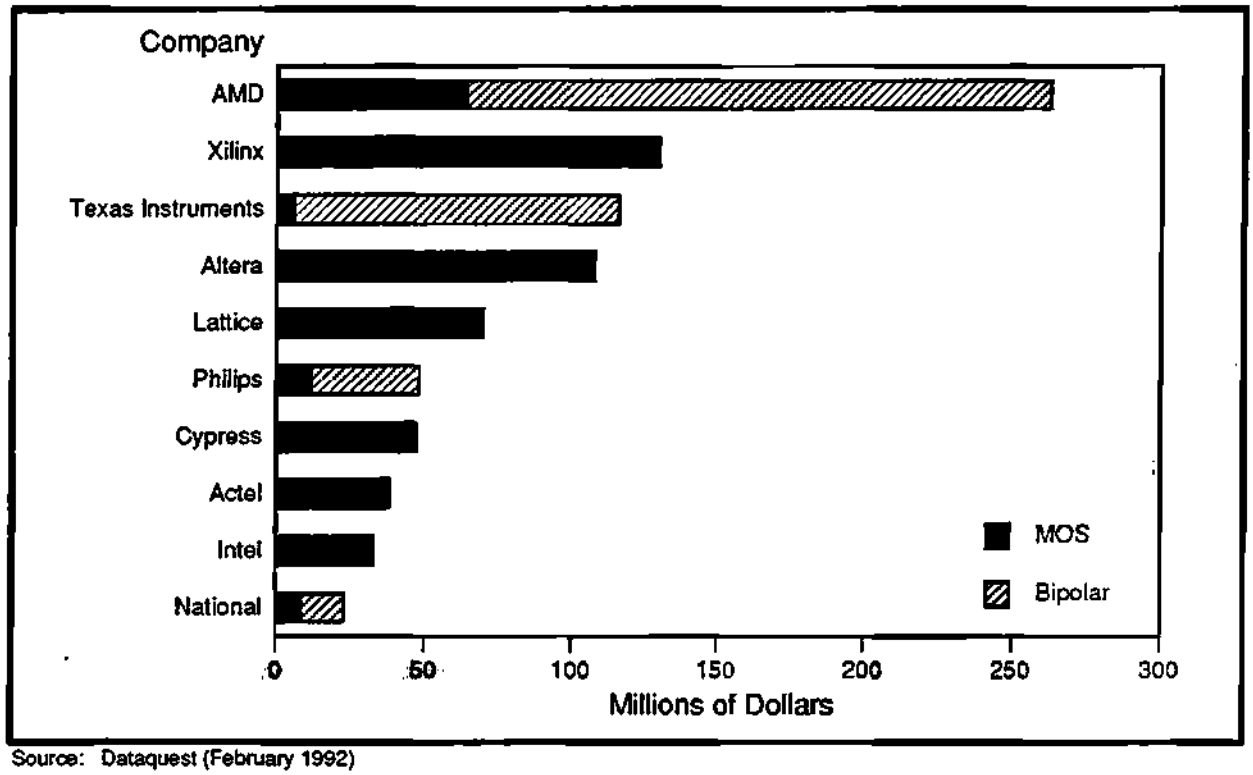
market grew a modest 11 percent over 1990, equal to growth of the 1991 worldwide ASIC market. However, PLDs on average had the highest profit margins of any ASIC product.

Figure 5 shows the top 10 1991 worldwide PLD supplier revenue by technology. Table 4 shows the emerging top 15 1991 worldwide MOS PLD suppliers and their respective revenue and market shares.

Noteworthy points regarding the 1991 PLD rankings include the following:

- AMD's total 1991 PLD revenue declined 10 percent over 1990. The company experienced a 20 percent decline in 1991 bipolar PLD revenue and a 52 percent increase in 1991 MOS PLD revenue. AMD is clearly sacrificing its bipolar PLD revenue.
- Xilinx surpassed Texas Instruments in total PLD sales. The company also extended its lead in worldwide MOS PLDs, growing sales by 55 percent. Texas Instruments' 6 percent decline in 1991 bipolar PLD sales cost it the No. 2 slot in total PLDs.
- Lattice experienced a below-average 1991 MOS PLD growth rate because, in our view, it lacks a high-density PLD product line.
- Philips captured the No. 6 spot in the 1991 PLD market. However, its 1991 MOS PLD revenue estimate appears high and will likely be revised downward in the final market share estimates.
- Actel has demonstrated that antifuse technology is viable, posting an 81 percent increase in 1991 MOS PLD revenue.

Figure 5
1991 Top 10 Worldwide PLD Suppliers



Source: Dataquest (February 1992)

Table 4
Preliminary Estimated Market Share Ranking: Worldwide MOS PLD (Millions of Dollars)

1991 Rank	1990 Rank		1990 Revenue	1991 Revenue	Percent Change	1991 Market Share (%)
1	1	Xilinx	84	130	55	23.1
2	2	Altera	78	108	38	19.2
3	3	Lattice	62	70	13	12.4
4	4	Advanced Micro Devices	42	64	52	11.4
5	4	Cypress Semiconductor	42	47	12	8.3
6	7	Actel	21	38	81	6.7
7	6	Intel	30	33	10	5.9
8	8	Atmel	7	13	86	2.3
9	15	Philips	2	12	500	2.1
10	8	National Semiconductor	7	9	29	1.6
11	10	SGS-Thomson	5	7	40	1.2
12	13	Texas Instruments	3	6	100	1.1
12	19	AT&T	1	6	500	1.1
14	11	Gould AMI	5	5	0	0.9
15	14	GEC Plessey	3	3	0	0.5

Source: Dataquest (February 1992)

Dataquest Perspective

Shifts in market share can be predicted by examining the strengths and weaknesses of the different types of ASIC suppliers. It will be increasingly difficult for many suppliers to compete, given today's industry structure.

ASIC suppliers can be grouped into four basic categories, as follows:

- Vertically integrated system suppliers that supply ASICs
- Broad-based semiconductor suppliers that supply ASICs
- Focused ASIC suppliers with fabs
- Focused ASIC suppliers without fabs

Vertically integrated system suppliers use ASIC technology as a competitive weapon for internal system design. This type of ASIC supplier wields a powerful advantage over all other ASIC suppliers in the merchant ASIC market for two reasons. First, vertically integrated system suppliers typically boast the most efficient manufacturing, which stems from economies to scale of high-volume manufacturing. In short, they have both large internal and merchant consumption, which enables greater amortization of development costs. Furthermore, they are often broad-based semiconductor suppliers, which provides an added advantage of amortizing their manufacturing costs across standard products as well as ASICs. This clearly gives them a highly competitive cost structure. Second, they have a large amount of in-house system expertise available to develop advanced ASIC cell libraries. In our view, these suppliers are well positioned to capitalize on the merchant ASIC market.

Broad-based semiconductor suppliers, however, develop ASICs to defend their semiconductor business. They have a cost structure that is somewhat less imposing because manufacturing costs can be amortized across both standard products (for example, DRAMs) and ASICs. However, they do not have the internal consumption necessary to reduce their merchant manufacturing cost structure. Therefore, their cost structure is less favorable than that of vertically integrated suppliers, but more favorable than the focused ASIC suppliers with fabs.

Broad-based semiconductor suppliers have another hurdle—limited system expertise. Typically, they are forced to rely on partnerships with customers to acquire the system expertise. The challenge for these suppliers is finding the right partners to aid them in the development of specialized macrocell libraries dedicated to specific application markets.

One way that some manufacturers will be able to avoid the high diffusion fab cost is by purchasing preprocessed gate array base wafers and simply performing metalization to customize the base arrays.

Focused ASIC companies with fabs find themselves in the most difficult position. They must find ways to maintain fab capacity to achieve a profitable cost structure as well as invest in the following areas:

- Development of next-generation manufacturing processes
- Development of the next-generation products
- Development of dedicated macrocell libraries
- Development of a competitive EDA environment

In our view, partnerships are extremely critical for focused ASIC suppliers that have fabs. They typically do not have the R&D budget required to develop all the areas of concern, such as the next-generation processes. Even more problematic, the cost of a state-of-the-art fab continues to rise and at an increasing rate. A complete 0.8-micron diffusion ASIC fab costs about $200 million, requiring very high volume production to support it. One way that some manufacturers will be able to avoid the high diffusion fab cost is by purchasing preprocessed

gate array base wafers and simply performing metalization to customize the base arrays. A metalization fab is significantly less expensive than is a full diffusion fab. This clearly reduces factory overhead and relieves the concern over maintaining fab capacity while achieving reduced turnaround time requirements.

Focused ASIC suppliers without fabs appear to be in a better position to maintain profitability. Today, most of these suppliers are PLD companies. They are not burdened with maintaining fab capacity or developing the next-generation manufacturing processes. They can use the majority of their R&D budget for developing next-generation products. However, alliances are also critical for these companies. They must rely on partnering for fab capacity as well as for the system expertise. Choosing the right partners is crucial in meeting today's increasingly demanding time-to-market pressure.

In our view, ASIC suppliers should evaluate their manufacturing costs in light of today's environment and quickly establish the alliances required to compete in the 1990s. System knowledge and dedicated unique macrocell libraries are of great trading value when forming these alliances. The ASIC market will reward those suppliers that offer low-cost manufacturing coupled with high-value intellectual property.

By Bryan Lewis

ASIC Testability—Finding the Demon Within

Within every one of the millions of ASICs shipped per month is a potential demon, one that could bring the most powerful of systems to its knees. This, of course, is the stuck-at fault. The guns of technology have been leveled at this target for the past 10 years. And with the renewed push to improve the quality and reliability of products, even more emphasis has been placed upon ASIC testability.

A host of new technologies and methodologies have been developed by both ASIC vendors and EDA suppliers. Yet even with the increased sophistication of test methods and the amount of attention testability has received, the growth of the ASIC and EDA test market certainly has been disappointing. However, Dataquest believes that this market is at a crux, and that ASIC suppliers must position themselves properly in order to capitalize on the coming test needs of the ASIC designer. This article examines the current climate of ASIC test and the promise for new ASIC test growth.

So Many Tools, So Little Revenue

Over the past three years, a plethora of design tools have been introduced to help ASIC designers improve testability. Table 1 lists a sample of the companies and their respective products.

Yet with all of these product offerings from the EDA camp, ASIC test automation software, which includes automatic test pattern generation (ATPG), fault simulation, and test logic synthesis, added up to only $21.9 million in 1990. Preliminary estimates for 1991 show little improvement, to a total perhaps of $25 million. This lackluster performance serves as a signpost that ASIC designers are not migrating to the more advanced design for test and ATPG tools.

Why Didn't Testing Take Off?

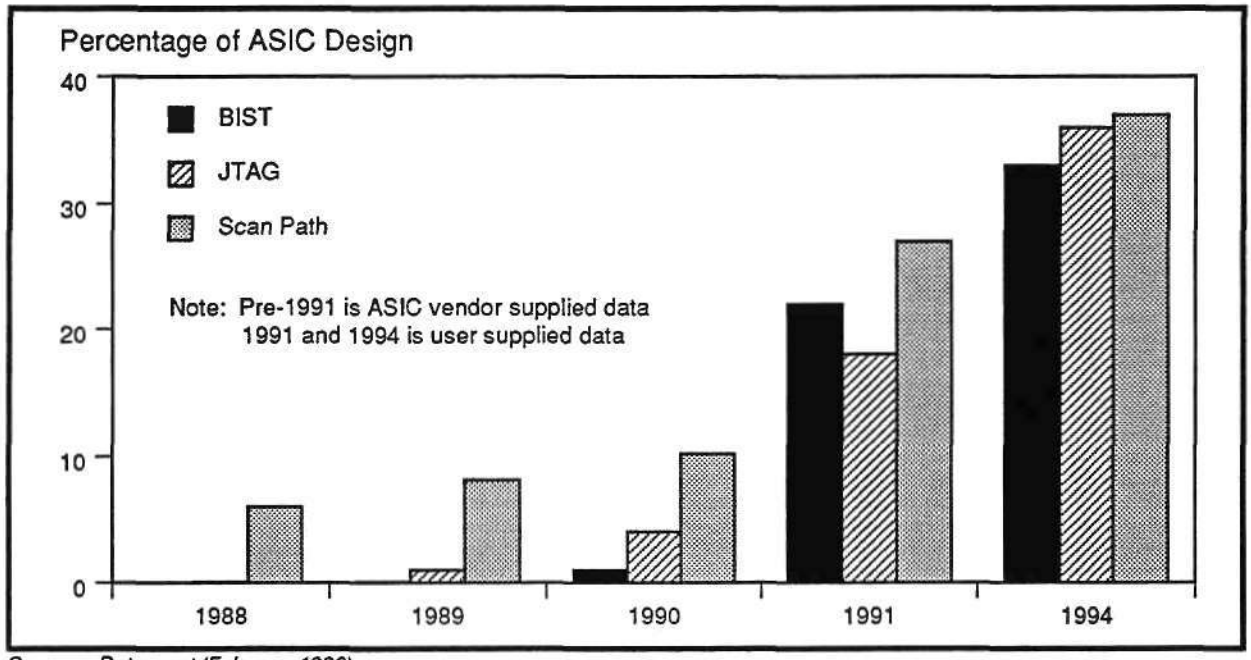
Test has traditionally taken a back seat to design, much like documentation. Logic designers have often ignored it, passing the responsibility of ensuring that the design meets test specifications to test engineering or manufacturing, because it was not a design problem. In fact, only 10 percent of CMOS gate array designs had any scan path logic (see Figure 1). With ASIC and EDA vendors proclaiming the dire need of this capability, why hasn't there

Table 1
Design Tool Products

Company	Product
AT&T	Test Scan System
Compass Design Automation	Test Assistant
Expertest	Test Design Expert
GenRad	HiDesignA
Motorola	Mustang
Racal Redac	Intelligen
Seimens Nixdorf	TENcheck, TENsocrates
Synopsys	Test Compiler
Teradyne	AIDA Testability Tools
TSSI	Test Development Software

Source: Dataquest (February 1992)

Figure 1
North American ASIC Test Use, by Year



Source: Dataquest (February 1992)

been a greater acceptance of design for test and scan-based logic design?

Dataquest believes that the primary reason behind the sluggish growth is that the typical ASIC design has not been large enough to warrant a rigid test methodology. For example, in 1991 the average gate array design start was still in the 20,000-gate range, up from 15,000 in 1990 and 9,000 in 1989. Designs in the 10,000- to 15,000-gate range typically allow engineers to forgo the use of dedicated test structures. Instead they use an ad hoc method for testing that usually yields adequate test coverage. A second reason is that the additional die size and performance penalty for test structures also makes design-for-test less attractive to ASIC designers.

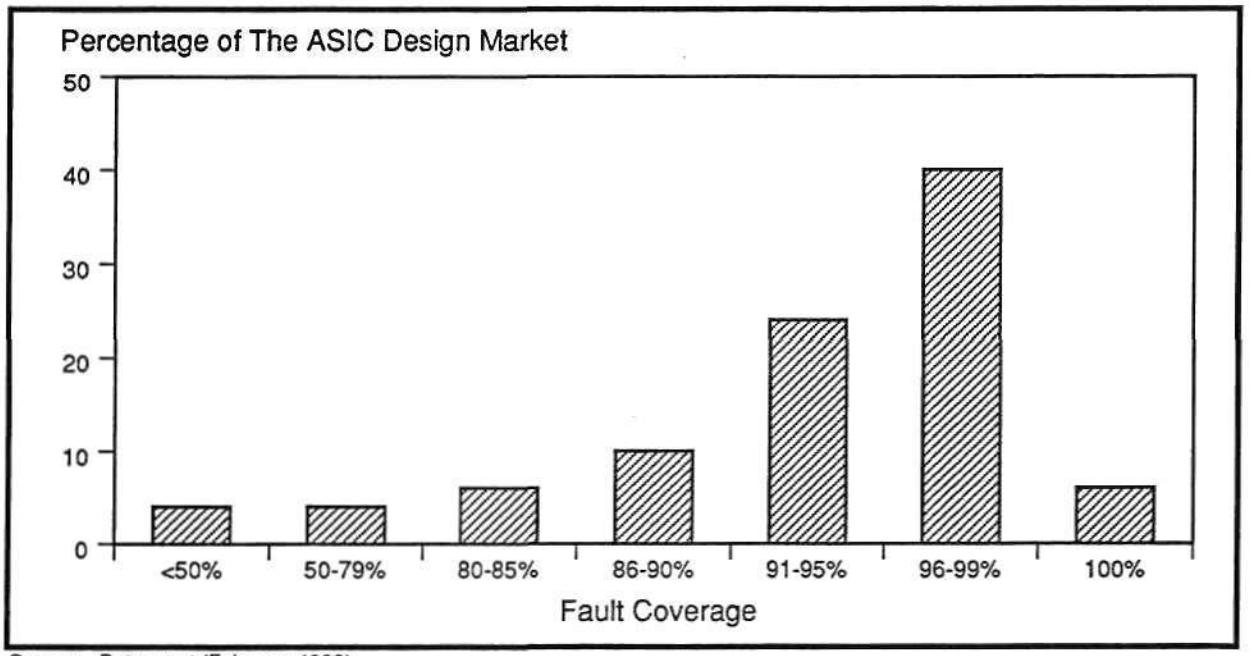
Corporate Mandates Should Spur Growth

Dataquest expects greater importance to be placed on quality and reliability at a corporate level. Quality and reliability currently ranks fourth in importance by North American electronic design companies, well behind time to market, cost, and design functionality. However, as ASIC designs become more complex, the testing difficulties grow at an exponential rate and rigorous test methods will be enforced at the corporate level to ensure a controllable defect rate. Dataquest believes that ASIC designers, no matter how hard they struggle against it, will have to start taking testability into account. In our view, it is important for ASIC and EDA vendors to note that market acceptance of the need for test technology demands a corporate sell and not an engineering sell.

Testability Acceptance Criteria: Speed and Coverage

The requirements for a successful test methodology should come as no surprise: high coverage, low-speed impact, and minimal cost. Figure 2 shows the distribution of acceptable test coverage, with more than 40 percent of the market demanding 96 percent or better fault coverage. But high fault coverage comes with a performance and die size penalty that many designers refuse to pay. For example, Dataquest research shows that only 29 percent of the ASIC design market would allow a 6 to 10 percent speed impact on their design in order to allow a desired level of testability. Although designers will not sacrifice the performance of their design, they are a little more willing to suffer

Figure 2
Acceptable Fault Coverage



Source: Dataquest (February 1992)

increased die size to achieve testability goals. Indeed, our research indicates that 66 percent of the market would bear a 6 to 10 percent chip cost increase in order to obtain the highest possible testability level.

The Future Is Finally Here

Dataquest believes that the use of test methods will begin to show substantial growth. Figure 1 shows the projected increase in use of test methodologies for 1991 and beyond. The number of designs expected to use scan methodologies will grow by more than 200 percent in the next three to five years, from 10 percent to 35 percent.

Although at this point there is no clear-cut winner in the upcoming test methodology wars, Dataquest believes that there is room for two or perhaps three solutions.

The emergence of JTAG for board-level design will also require ASIC vendors to supply this capability as a matter of course in order to remain competitive. The use of JTAG will double between the current generation of design and the next.

Test Methods

Dataquest sees two primary methods of ASIC test automation: design with test, and after-design test. Design with test means bringing the test issue up front in the logic designer's mind and creating the logic design with testability structures so that speed and silicon efficiency are weighed against the need for increased fault coverage. This includes performing ATPG and fault coverage verification for every module of the design during conception and implementation phases of the design process. The second method, after-design test, consists solely of automatic test pattern generation and some limited test logic synthesis (that is, scan insertion after the complete design has been integrated).

While design with test and after-design test focus on improving software tools and design methodology, one company has chosen to tackle the ASIC test problem from a hardware perspective. Crosscheck Technologies' novel architecture is imprinted upon ASIC masterslices. Seven companies have embraced the technology: Fujitsu, Harris, LSI Logic, NEC, Oki, Raytheon, and

Sony. This list captured almost 50 percent of the CMOS gate array market in 1991. However this promising technology has yet to reach the market in a broad sense; only three of the suppliers have announced products. The Crosscheck technology offers the potential to solve more than just the classic stuck-at fault failures. Failure modes including opens, shorts, and bridging faults are also detectable with this technology. However, this capability must be weighed against the increased die cost associated with it.

Dataquest Perspective

In order to successfully compete in high-density gate array and standard cell markets, ASIC vendors must help tackle the growing test problem. Although at this point there is no clear-cut winner in the upcoming test methodology wars, Dataquest believes that there is room for two or perhaps three solutions. Each ASIC designer will approach the test demon in his or her own way, trading off the cost, speed, and ease of use of the existing test solutions.

At the very minimum, ASIC vendors must foster design with test and after-design test methodologies, supplying the needed macros and support for the upcoming testability crunch.

The high cost of underused testability tools will require the ASIC vendor to undertake more of the test burden, amortizing the cost and using guaranteed quality as a product differentiator. At the very minimum, ASIC vendors must foster design with test and after-design test methodologies, supplying the needed macros and support for the upcoming testability crunch. Test solution suppliers must keep design performance and design time impacts to almost nothing in order to be successful.

By Robert K. Beachler

High-End ASIC Opportunity Shifting to Mainstream

Electronic systems manufacturers will encounter significantly greater competitive pressures over the next two to three years stemming from the globalization of the industries and markets in which they participate. As a result, these systems vendors will place greater technology demands on the semiconductor manufacturers supplying them with ASIC products. In short, as the competitive pressures mount, electronics suppliers will look toward ASIC vendors to deliver ASIC technologies that offer even faster speeds, have higher density, and consume less power. Moreover, the ASIC market will gravitate toward those suppliers that embed this technology in a suite of design tools that supports an unfettered design methodology.

An objective view of the ASIC arena reveals that the ASIC has become a commodity. Indeed, computers themselves are becoming commodities, so it is not surprising that the technology comprising computers is becoming a commodity. Ostensibly, the ASIC will continue its march into the world of the commodity, with a myriad of undifferentiated suppliers from different corners of the globe vying even more aggressively for ASIC sockets. Thus, differentiation among competitors must be both the unwavering strategy and focus of all vendors that wish to be successful in the ASIC business.

ASIC vendor strategies centering around technology differentiation have been less effective than anticipated over the past few years. For example, numerous suppliers offer high-density gate arrays, yet the market's needs have remained below 20,000 gates on average. Similarly, many ASIC suppliers can manufacture CMOS gate arrays and cell-based ICs that yield system clock frequencies exceeding 60 MHz, but two-thirds of the market still builds systems running at less than 51 MHz. In sum, the market's technology needs have lagged the advanced products offered by ASIC manufacturers. Dataquest believes that this situation is about to change.

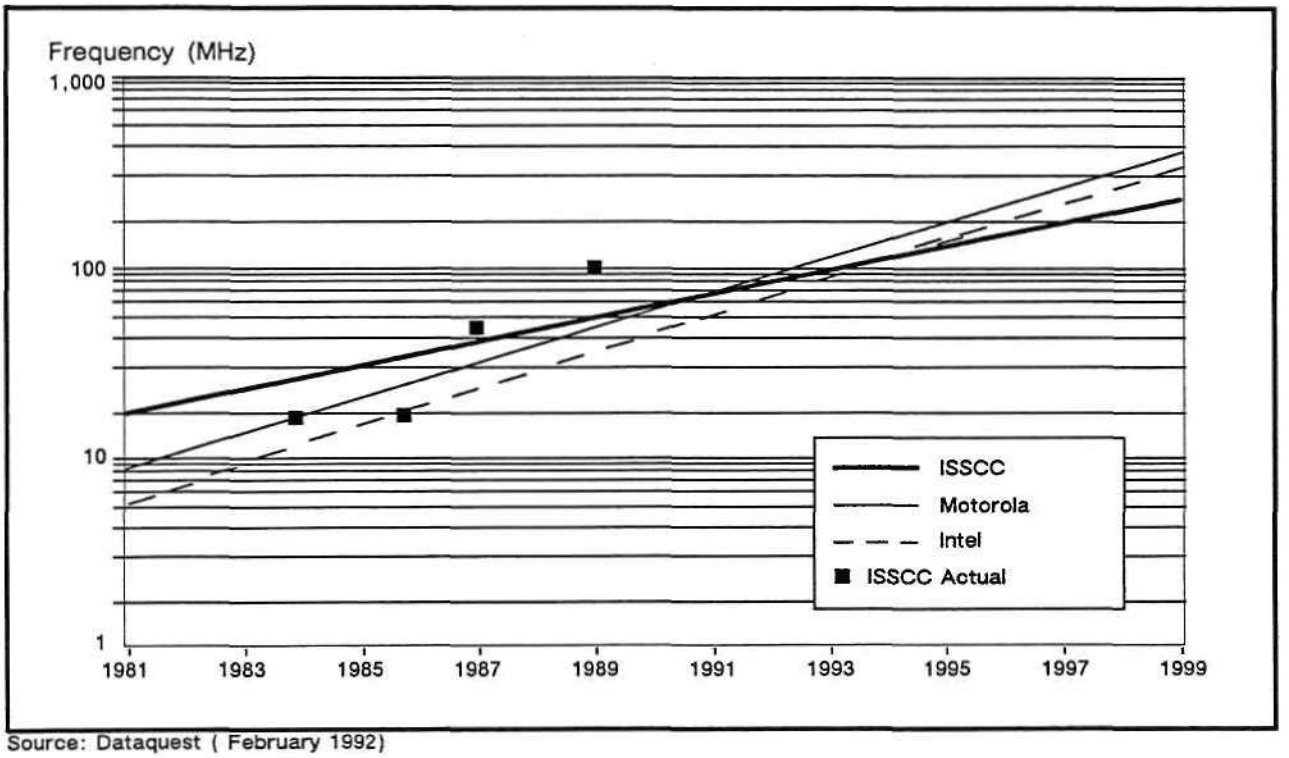
In our view, the combination of improved design tools, a more skilled ASIC design community, and intensifying competitive pressures in the systems design marketplace will translate to more widespread use of the high-end ASIC technologies. Furthermore, we believe that ASIC suppliers that can deliver the right combination of high-end capabilities will move to center stage over the next three years. This article profiles the emerging high-speed ASIC design market.

Forces Driving the High-Speed ASIC Market

Clock frequencies for MOS microprocessors have been increasing at a rate of about 15 percent annually. Figure 1 illustrates historical and projected (based on extrapolation) microprocessor clock frequency rates. The graph is derived from product introductions from Intel and Motorola, as well as from research presented at various ISSCC symposia. Although the Motorola and Intel trend lines show future clock rates of 300 MHz to 400 MHz, such frequencies are not likely in the time frame shown. In our view, the physical limitations of silicon do not support indefinite extension of the current trends. A more realistic projection calls for the introduction of 100-MHz microprocessors by early 1994 and 200-MHz devices by the end of the decade.

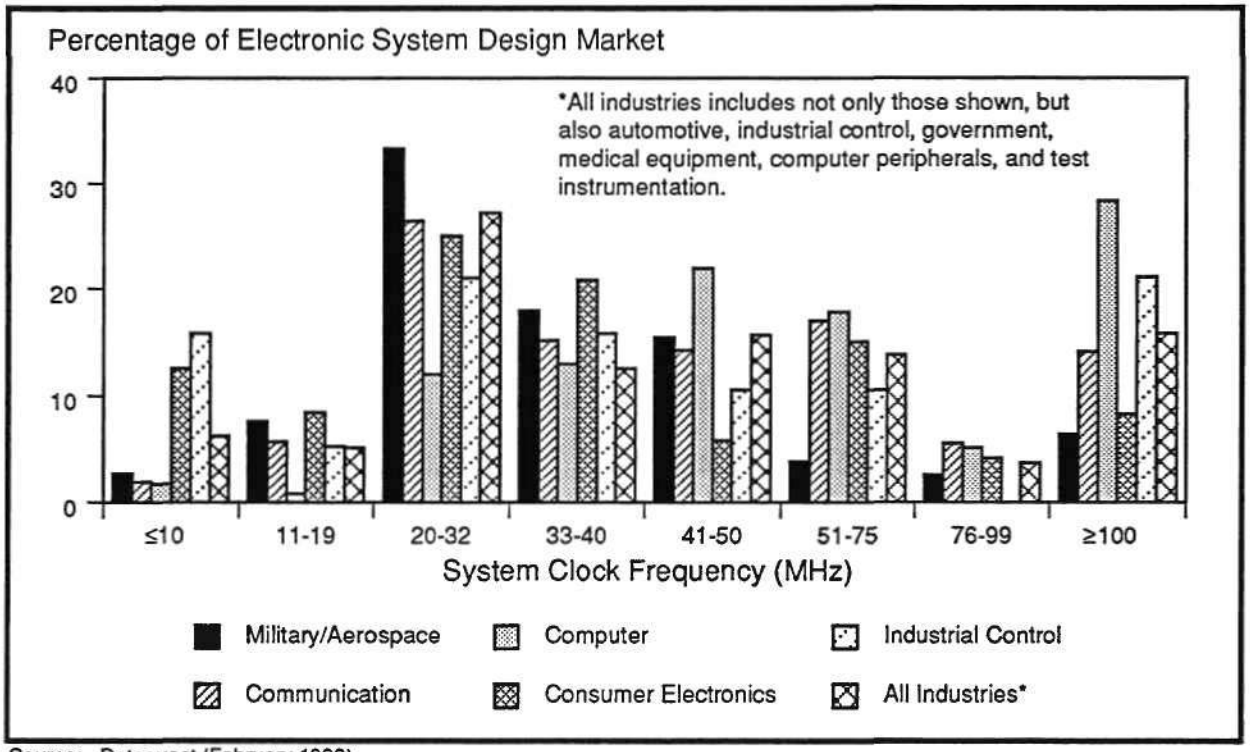
Figure 2 shows the clock frequency distributions of the current generation of electronic system designs in North America, segmented by industry. The data clearly show that only one-third of the overall market is designing systems that run above 50 MHz. Dataquest believes that increases in clock rates of systems designed by the mainstream electronic design market will be in approximate lockstep with the rate of increase of microprocessor speeds (12 to 15 percent per year). In the more performance-driven industries such as the workstation sector, manufacturers will push the performance of semiconductor technology to its limit, using proprietary design and manufacturing technologies (where available) to boost the rate of advancement to 15 to 20 percent annually. In the less performance-concerned markets such as automotive, the move toward higher speeds will be more restrained.

Figure 1
Clock Frequency Trends for MOS Microprocessors



Source: Dataquest (February 1992)

Figure 2
North American Electronic System Clock Frequencies, by Industry



Source: Dataquest (February 1992)

Nearly all major ASIC manufacturers have begun (or will soon be) offering technologies to address the needs of this new class of design problem. These technologies include macrocells such as phase-lock loops that minimize on-chip and interchip clock skew, high-drive buffers that handle large numbers of simultaneously switching outputs to mitigate ground bounce, slew rate control circuits that ensure linear slew rates in output buffers, and circuitry that compensates for variations in temperature, voltage, and fabrication processes. In addition, several ASIC manufacturers have begun aggressively marketing 3.3V libraries to meet the market's low-power, high-performance demands. With the stream of products and technologies that suppliers have begun announcing, the battle lines among vendors targeting the high-speed design market are being drawn quickly.

Differentiation within the Expanding High-Speed ASIC Market

Dataquest believes that the traditional technology and market strategies followed by most ASIC manufacturers have focused primarily on intrachip design issues, with only marginal attention paid to interchip, or system, problems. In our view, manufacturers that direct equal attention toward both and position themselves in the market with technology that addresses both will emerge as industry leaders over the next two to three years. Providing technology, support, and service (such as consulting and design courses) for high-speed design will be perceived by the market as added value. Moreover, it will provide much needed differentiation among ASIC competitors.

Our view is based on the fact that clock speeds of 33 MHz and above aggressively challenge the limits of printed circuit board (PCB) interconnect technology. At these speeds, PCB traces adopt characteristics of circuit elements, introducing potentially crippling signal delay and distortion to the signals they carry. In short, some traces must be treated as transmission lines and/or be isolated from other traces to prevent capacitive coupling (crosstalk).

Interchip design issues will become increasingly important not only because of the rise in clock

frequencies, but also because the size of printed circuit boards is remaining relatively constant. Dataquest's most recent end-user research shows that PCBs are shrinking by less than 3 percent annually. Meanwhile, clock frequencies are rising by 12 to 15 percent yearly. Thus, the length of PCB traces will remain fairly constant while clock frequencies continue increasing, further exacerbating the impending design problems.

Modest reductions in PCB size indicate that most of the systems market is not using semiconductor integration advancements to reduce form factor but rather is packing more functionality into the same given area. Our view correlates well with the fact that reducing form factor is a very low priority among systems manufacturers. Not surprisingly, the market plans to take advantage of semiconductor integration progress by reducing the average number of components per board by about 10 percent between its current generation and next generation of designs. Indeed, this is the approximate rate of integration advancement of semiconductor manufacturing.

Without the proper design tools, technologies, and support, high-speed design will become unwieldy. Such compelling evidence should act as a mandate for ASIC manufacturers to appropriately address the market's interchip design needs. (The rate of increase of clock frequencies taken together with slow size reductions projected for PCBs also serves as an indicator of the impending importance of and need for multichip modules.)

ASIC manufacturers that aggressively attack and deliver value to the emerging high-speed market segment stand to gain considerable market position. In our view, systems built around high-speed logic will be more subject to spurious and intermittent signal degradation problems than will systems running at lower frequencies. As a result, an increasing number of electronic products will intermittently fail, and for no apparent reason to the user. Buyers of these electronic products will become more sensitive to quality issues, which in turn will make quality a more important issue for electronic systems designers. Quality currently ranks fourth on the priority list of most electronics manufacturers. Indeed, quality (based on a comprehensive survey of North American electronics manufacturers) currently falls well behind reducing time to market, reducing cost, and increasing functionality, in terms of what manufacturers believe are the most important factors contributing to their products' future ability to achieve market success. In sum, we believe that improving design quality will climb up the importance chart as system clock frequencies rise.

We can draw a useful parallel between a traditional ASIC design problem and what we believe is the impending high-speed design problem. It is well known that a significant percentage of ASIC designs have not worked correctly when plugged into the sockets of their respective target systems. Figures range from a low of 10 percent to a high of 50 percent. (Designers argue over the source of these problems, in terms of whether they are rooted most in timing violations or in functional problems. Dataquest's research of North American manufacturers has found that about 45 percent of the problems stem from timing errors and about 55 percent result from functional violations.) This has caused many ASIC customers to lose confidence in both their ASIC suppliers and the technology (and methodology) itself.

...those that offer technology and support not only for high-speed ASIC design but also for high-speed system design will significantly differentiate themselves in the ASIC market.

In our view, once the mainstream ASIC market begins boosting system clock rates above the 33-MHz mark, timing problems will overshadow functional problems. It goes almost without saying that ASIC vendors delivering chips with timing requirements that meet the customer's expectation will garner a solid reputation in the market. Conversely, those ASIC suppliers that do not meet the customer's expectations should observe what happened to ASIC vendors whose silicon regularly failed when plugged into the target system—a continuous loss of market share.

The Relationship between Silicon Advancements and Design Cycle Length

It is interesting to note that the average length of today's printed circuit board design cycle (from design concept to prototype) is about nine months. As discussed earlier, manufacturers are increasing the clock rates of their products by about 12 to 15 percent annually. In our view, it is reasonable to use the rate of advancements being made in semiconductor manufacturing as a rough proxy to predict the percentage by which systems manufacturers will reduce the average design cycle's length. Clock frequency improvement rate can be used as a surrogate for measuring semiconductor manufacturing advancements. Semiconductor manufacturing is at the beginning of the electronics food chain, and its rate of advancement should translate downstream to the rate at which new chip, board, and ultimately system design products are developed. This conclusion stems from our belief that downstream semiconductor users will adopt new and faster chip technology as quickly as it becomes available. Our analyses correlate with recently captured market data. A survey of North American electronic systems manufacturers shows that they plan to reduce next-generation PCB design cycle time on average by 22.5 percent.

Dataquest Perspective

Most ASIC vendors have offered MOS gate arrays and cell-based ICs that can run up to 60 MHz. Yet the performance of most ASIC and system designs developed by the market fall into the low-end category, which Dataquest defines at this juncture as designs running below 25 MHz. The upshot has been a relatively low number of high-speed ASIC design starts and hence few high-speed system designs. In our view, this portends to be a liability for some ASIC suppliers, whereas for others it is an opportunity. For suppliers that can deliver *only* leading-edge chip fabrication technology, it will be a liability. On the other hand, we believe that ASIC vendors also offering value-added technology and support services that target the design problems associated with high clock rates will be most successful in the expanding high-speed market. Moreover, those that offer technology and support not only for high-speed ASIC design but also for high-speed system design will significantly differentiate themselves in the ASIC market.

By Ron Collett

In Future Issues

The following topics will be addressed in future issues of ASICs Worldwide *Dataquest Perspective:*

- ASIC forecast
- BiCMOS ASICs

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• User Wants and Needs

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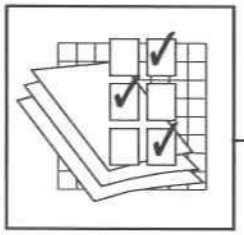

User Wants and Needs

System Designers Vote on Future ASICs
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ASICs *Worldwide*
ASIC-SEG-UW-9201
November 23, 1992

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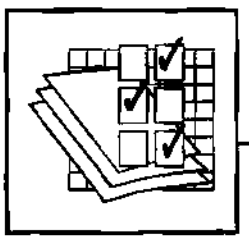

User Wants and Needs

System Designers Vote on Future ASICs
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ASIC-SEG-UW-9201
November 23, 1992

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Chapter 1
Executive Summary

Introduction and Report Structure

This report represents the results of Dataquest's research into worldwide electronic system design. It is intended to be used by business executives to spot significant trends in electronic system design and explore potential target markets for ASIC devices. The basis for this report, an end-user survey, is in Appendix A. This same survey is also the basis for a similar report on worldwide electronic design automation user wants and needs, which is available to subscribers of Dataquest's Electronic Design Automation service.

This report is broken into five main chapters. It begins with an executive summary. Chapter 2 explains the research process Dataquest employed in gathering the information and the demographics of the respondents of the survey. Chapter 3 delves into the critical factors that determine success for system designers and the characteristics of the systems being designed, and also provides valuable insight into the ASIC design cycle. Chapter 4 sheds light on the ASIC products being designed in systems on a regional and application basis. ASIC users vote on the gate counts they will need for each type of application for their next-generation system design. In Chapter 5, Dataquest measures the perceived demand from system designers for BiCMOS ASICs and GaAs ASICs. Potential applications for these emerging technologies are examined on a product and regional basis. In the final chapter, Dataquest explores the major findings from this research and makes recommendations to both ASIC suppliers and ASIC users.

Major Findings

An overriding theme echoed by system designers throughout the world is that they want to dramatically increase their system integration levels for their next-generation system designs, but not at the expense of increasing their time to market or raising the system cost. Reducing time to market is the No. 1 goal of today's system designers. Reducing the ASIC design cycle is important in meeting this goal. System designers in Japan lead designers in North America and Europe with the shortest ASIC design cycle. Japan system designers were able to achieve the reduced ASIC design cycles for their current-generation system design by using lower-complexity ASICs than North American designers. The average ASIC complexity of current-generation system design in Japan is about 18,000 gates, compared with 28,000 gates in North America. However, one of the biggest

surprises from our survey results is that the average ASIC gate count in Japan for next-generation system design is expected to be higher than the average gate count in North America (57,000 gates in Japan, compared with 54,000 in North America). Applications slated for high-density ASICs in Japan include RISC-based computers, industrial control, medical equipment, telecommunication, data communication, and consumer electronics. Dataquest believes that HDTV will play a major role in the development of high-density ASICs in Japan.

Another major finding from our end-user research is the strong perceived demand for BiCMOS ASICs in next-generation system design. Survey results showed that about 10 percent of the system designers in North America and Japan said they were using at least one BiCMOS ASIC in their current-generation system design. As for next-generation system design, 36 percent of designers in North America and 31 percent of designers in Japan said they would be using BiCMOS ASICs. Although Dataquest believes that these estimates are high, clearly ASIC users believe that there is a strong need for BiCMOS ASICs in their next-generation system designs.

In this report, Dataquest takes a long, hard look at the applications driving the ASIC industry.

Chapter 2
Survey Methodology

Dataquest demand-side, or end-user, data are gathered using extensive survey techniques. End users are identified through the registered user and prospect lists of ASIC and EDA companies. Surveys were distributed throughout North America, Europe, and Japan, enabling Dataquest to gather a snapshot from a user point of view of the current and future system design requirements and the applications driving ASIC usage. Relying upon Dataquest's international expertise, surveys distributed in Japan were translated into kanji, the Japanese character set, to improve their accuracy. The survey is in Appendix A.

Surveys were mailed in the second half of 1991 to North American sites. The responses were examined for integrity and entered into a database to allow manipulation and cross-cutting of the data. Japanese surveys were distributed at the end of 1991, and the responses were similarly processed and entered in early 1992. European surveys were completed in the spring of 1992. Although some of the surveys were mailed in late 1991, Dataquest believes that the responses for today's system design and next-generation system design are still valid because the length of the design cycle and the survey respondents were somewhat optimistic when the surveys were originally filled out.

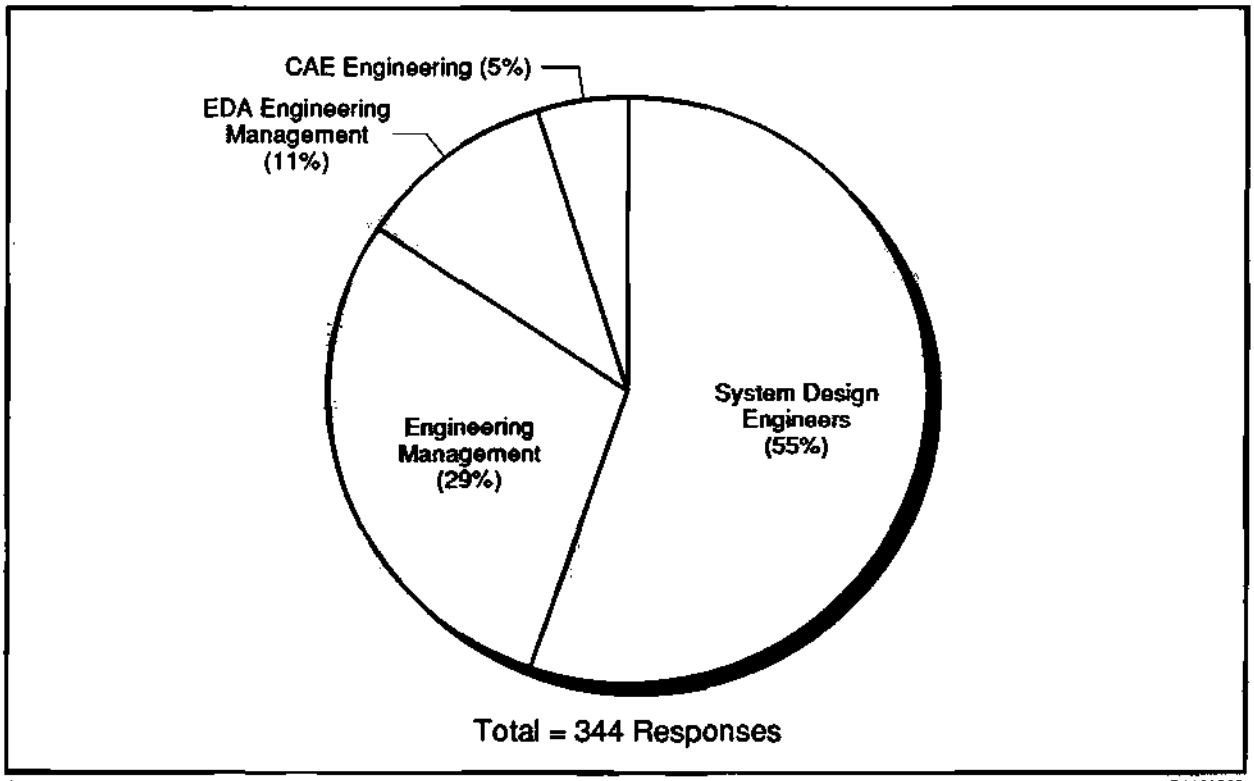
Respondent Demographics

North America

Data collected in North America are predominantly from system design engineers and engineering managers, with a 16 percent contribution from CAE engineers and EDA engineering management (see Figure 2-1). Dataquest believes that these data represent a statistically significant sample to gauge the needs and trends of electronic system design.

There were 344 total survey responses, and the mean employee count of the company was 27,335. Figure 2-2 denotes the primary line of business of the respondent's company. Dataquest believes that more significant information may be ascertained by examining the trends for the project team's primary line of business, which is shown in Figure 2-3. Dataquest's reasoning is that ASIC usage is dependent on the applications they are used in, which is better represented by the project team's responses.

Figure 2-1
North American Respondents, by Job Title



Source: Dataquest (November 1992)

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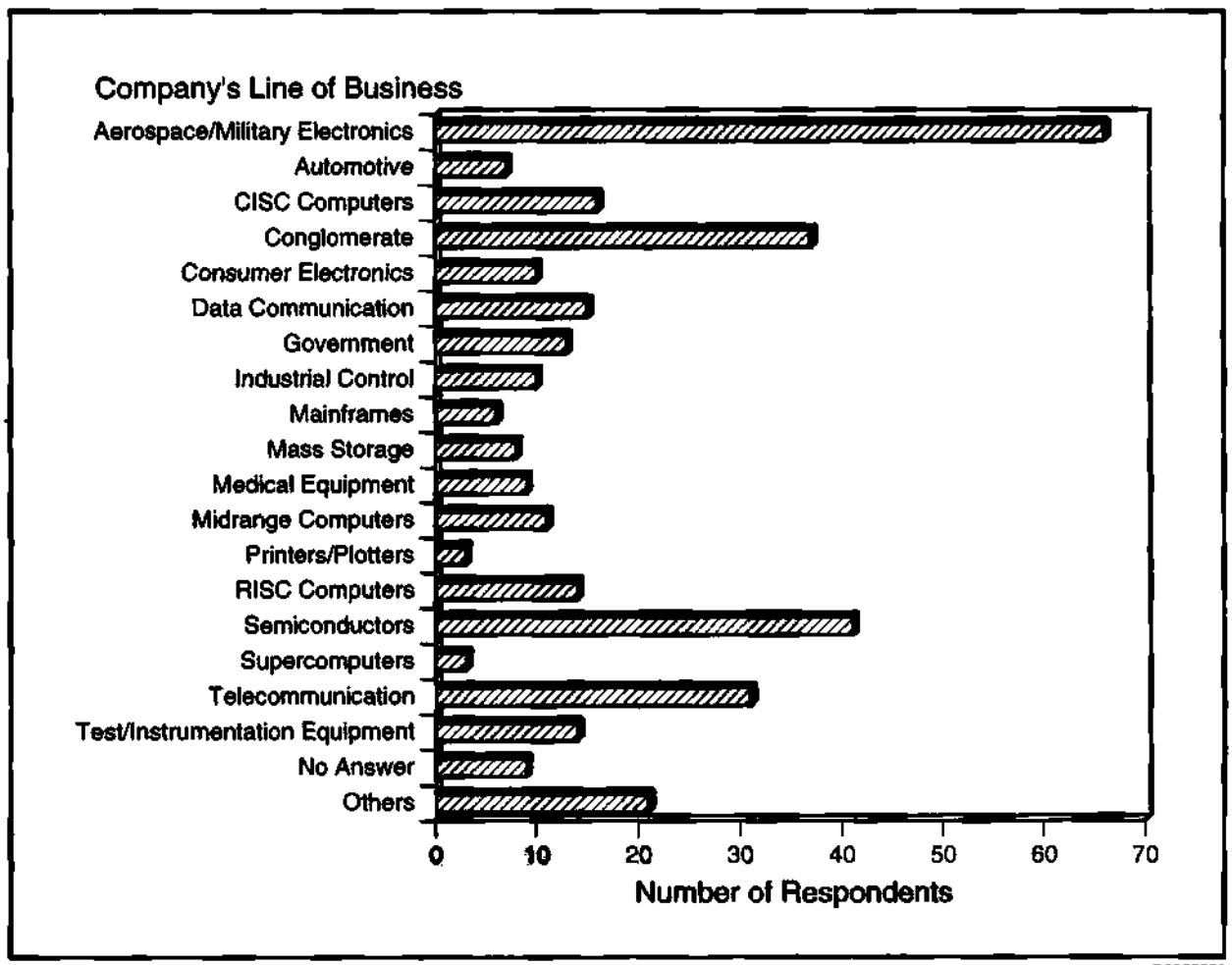
Figure 2-2
North American Respondents' Primary Line of Business



Source: Dataquest (November 1992)

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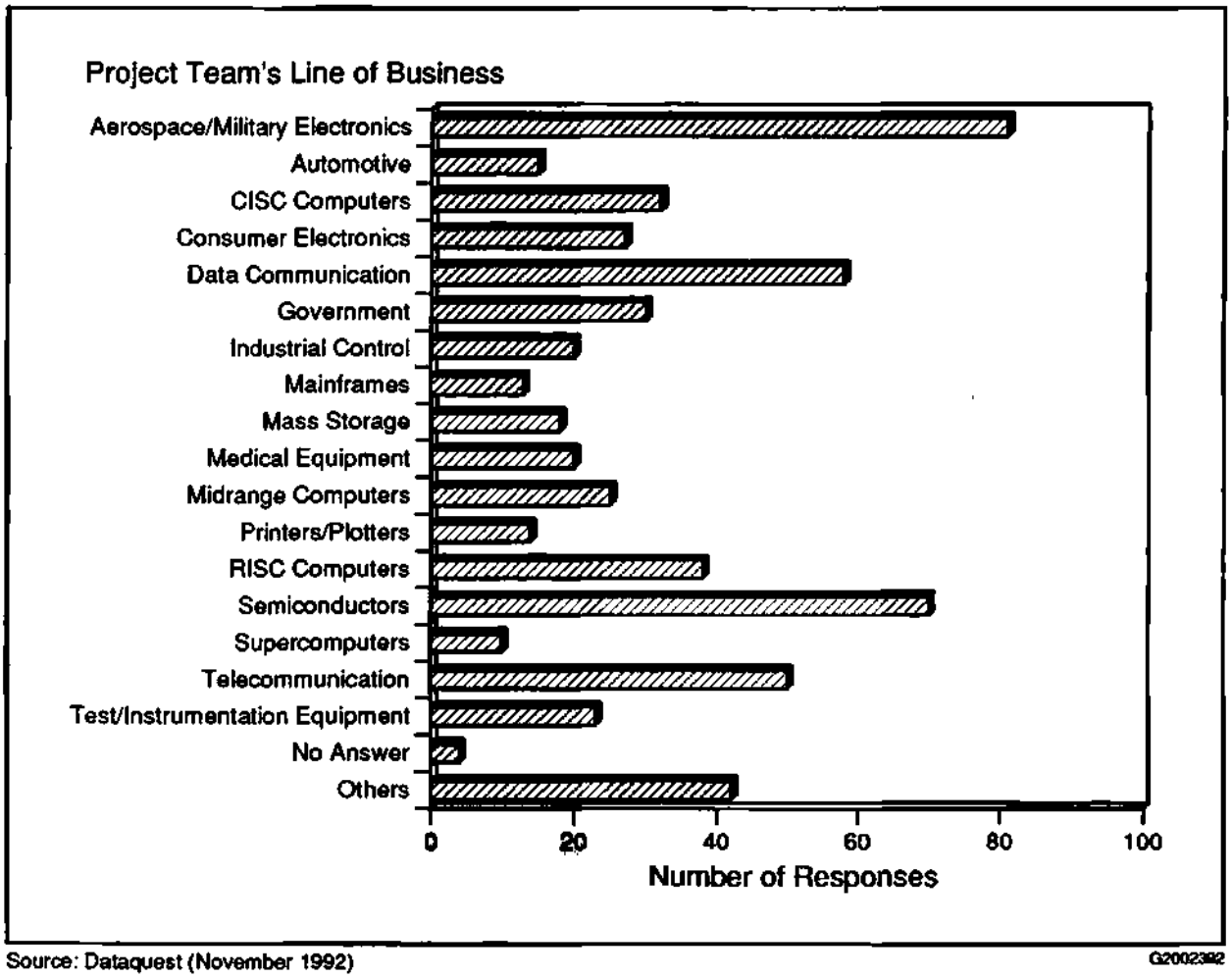
Figure 2-3
North American Respondents' Project Team's Primary Line of Business



Source: Dataquest (November 1992)

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It is important to note that *survey respondents were allowed to check more than one box for their project team's primary line of business. Because of this, certain responses have been classified for more than one application area.*

To provide a more statistically correct view of end-application markets, Dataquest grouped respondent answers into broader categories in certain situations. Figure 2-4 and Table 2-1 show the North American responses by application project team.

Japan

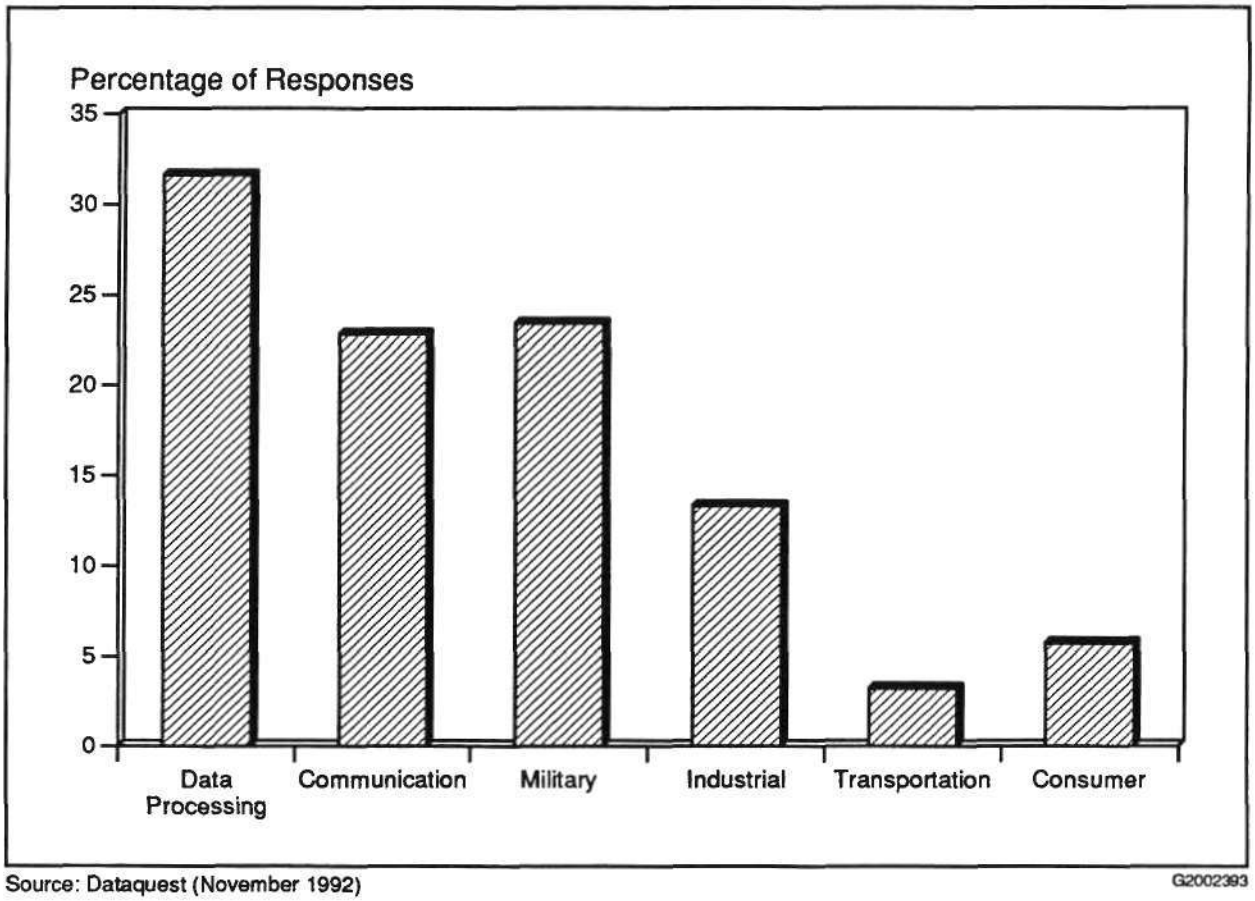
Dataquest's Japanese survey results show that the majority of respondents are also system design engineers or engineering managers (see Figure 2-5). There were 260 total survey responses, and the mean employee count of the company was 18,560. Figure 2-6 shows Japanese respondents' by the company's primary line of business. Figure 2-7 shows Japanese respondents by the project team's primary line of business. Again, the data presented in this report are based on the project team's impute. Figure 2-8 and Table 2-2 show the Japanese responses by application project team.

Europe

Because of language and intercountry mailing difficulties, results from Dataquest's survey of European designers were relatively small, with only 59 responses. Although no single industry recorded more than 20 responses, Dataquest included the results of European data for completeness. Indeed, the results from Europe are consistent with North American and Japanese data.

European respondents show again that they are predominantly system design engineers or engineering managers (see Figure 2-9). There were 59 total responses, and the mean employee count of the company was 11,440. Figure 2-10 shows European respondents by the company's primary line of business; Figure 2-11 shows European respondents by the project team's primary line of business. The data presented in this report are based on the project team's input. Figure 2-12 shows the European response by application project team.

Figure 2-4
North American Respondents, by Application Project Team



Source: Dataquest (November 1992)

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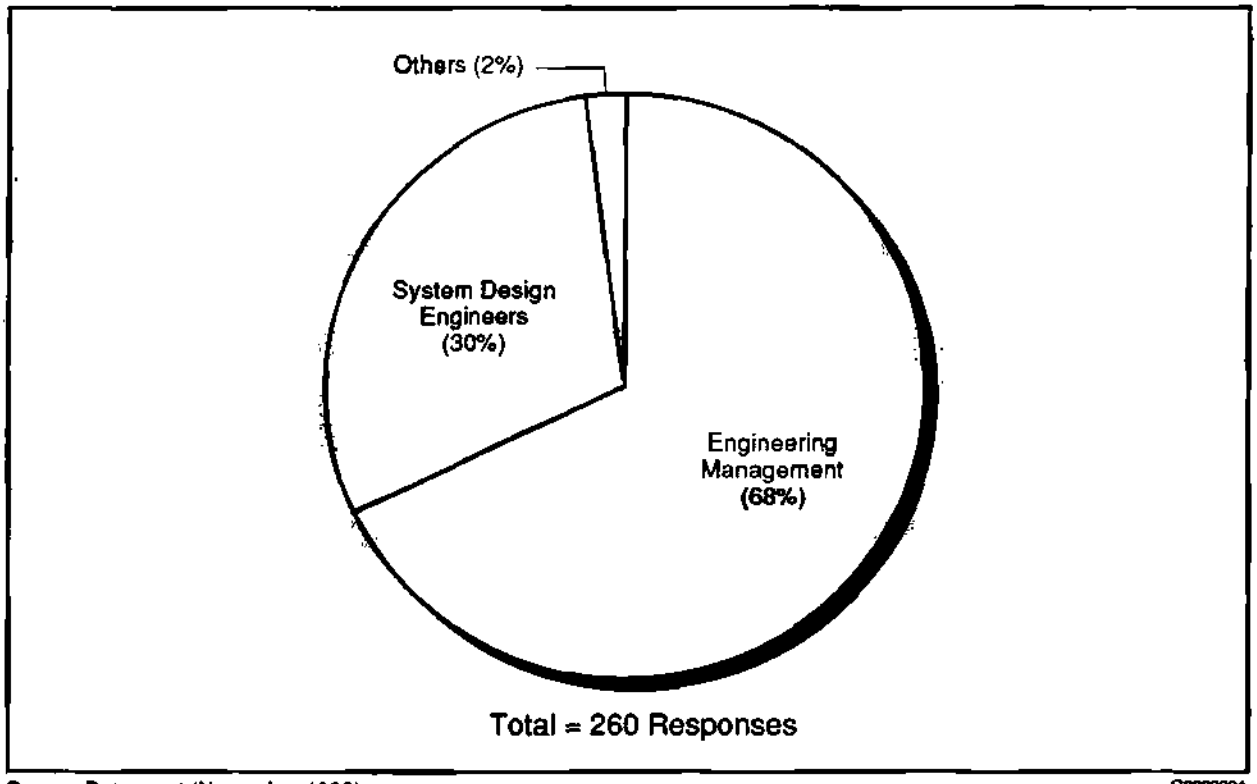
Table 2-1
North American Respondents, by Application Project Team (Number of Responses)

Project Team Responses	
Data Processing	
RISC Computers	38
CISC Computers	32
Midrange Computers	25
Mainframe Computers	13
Supercomputers	10
Printers/Plotters	14
Mass Storage	18
Total Data Processing	150
Communication	
Telecom	50
Datacom	58
Total Communication	108
Military	
Aerospace/Military	81
Government	30
Total Military	111
Industrial	
Industrial Control	20
Medical Equipment	20
Test/Instrumentation	23
Total Industrial	63
Transportation	
Automotive	15
Total Transportation	15
Consumer	
Consumer	27
Total Consumer	27
Total All Applications	474

Source: Dataquest (November 1992)

Figure 2-5
Japanese Respondents, by Job Title



Source: Dataquest (November 1992)

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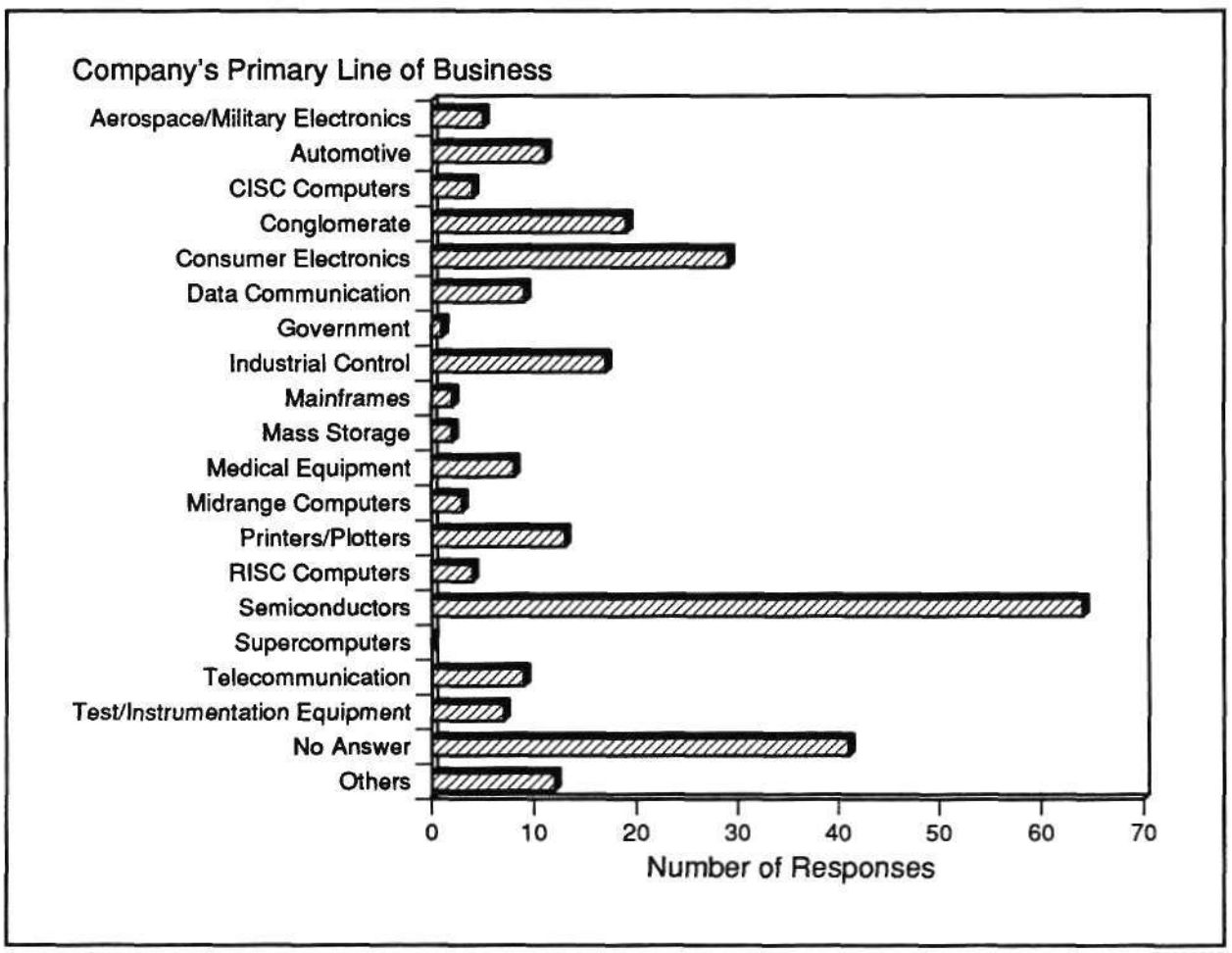
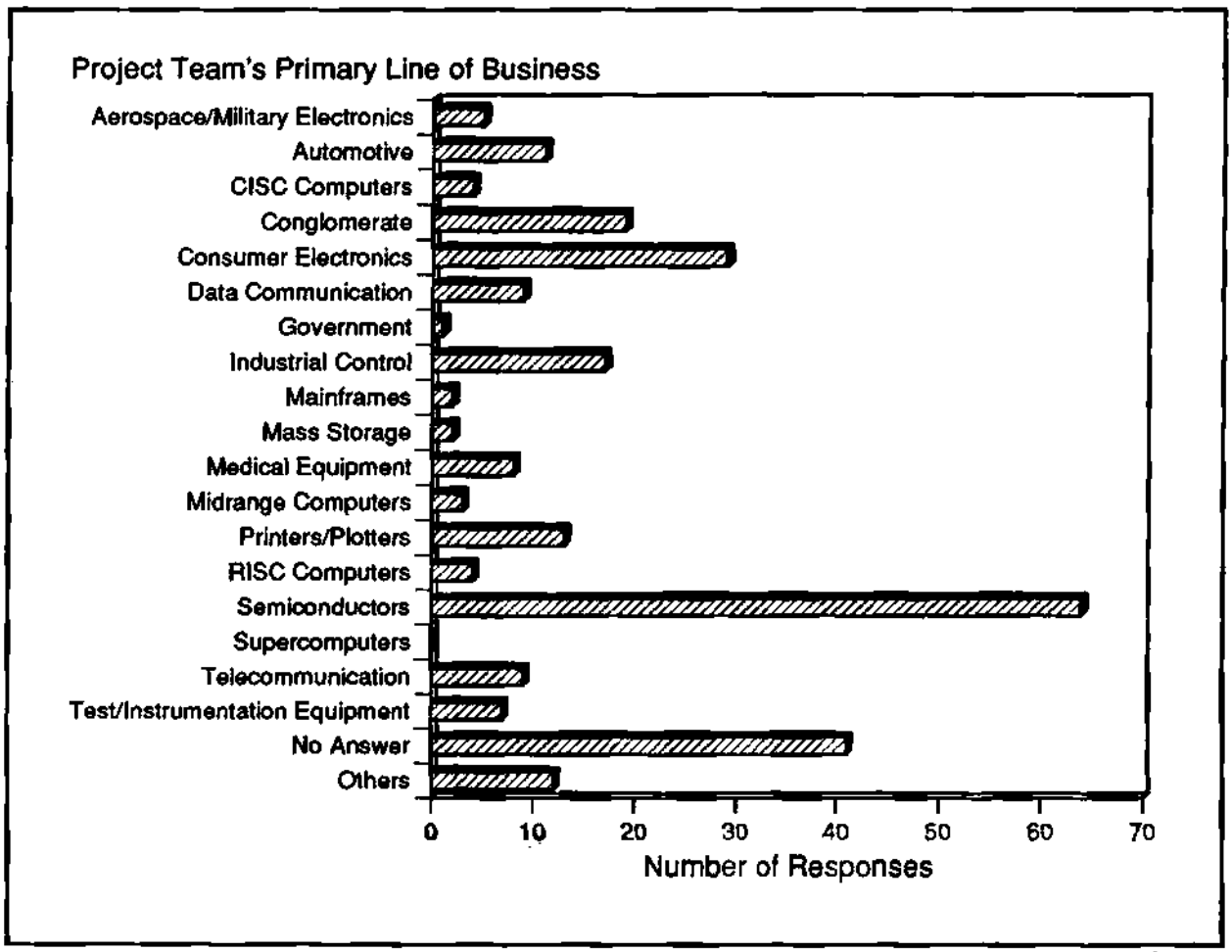
Figure 2-6
Japanese Respondents' Primary Line of Business



Source: Dataquest (November 1992)

G2002395

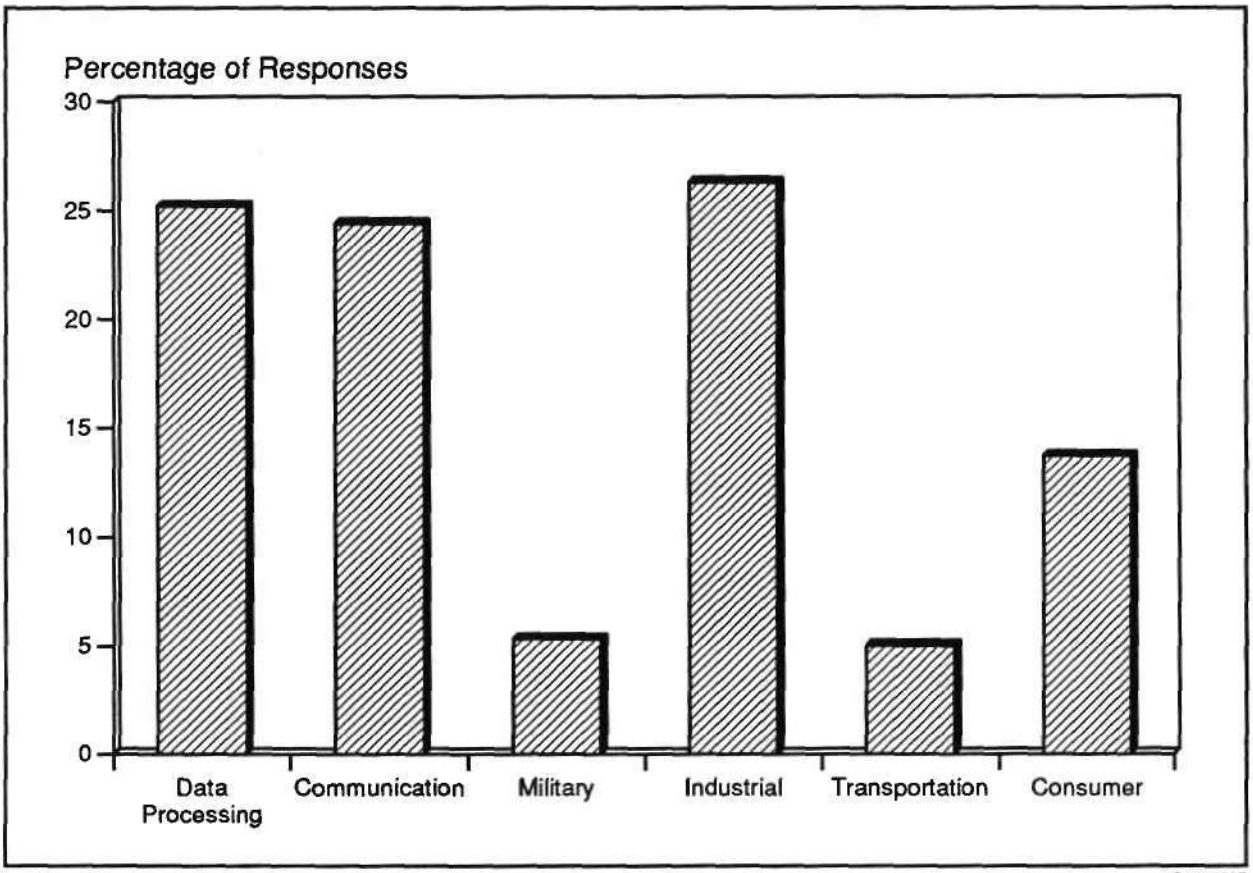
Figure 2-7
Japanese Respondents' Project Team's Primary Line of Business



Source: Dataquest (November 1992)

G2002396

Figure 2-8
Japanese Respondents, by Application Project Team



Source: Dataquest (November 1992)

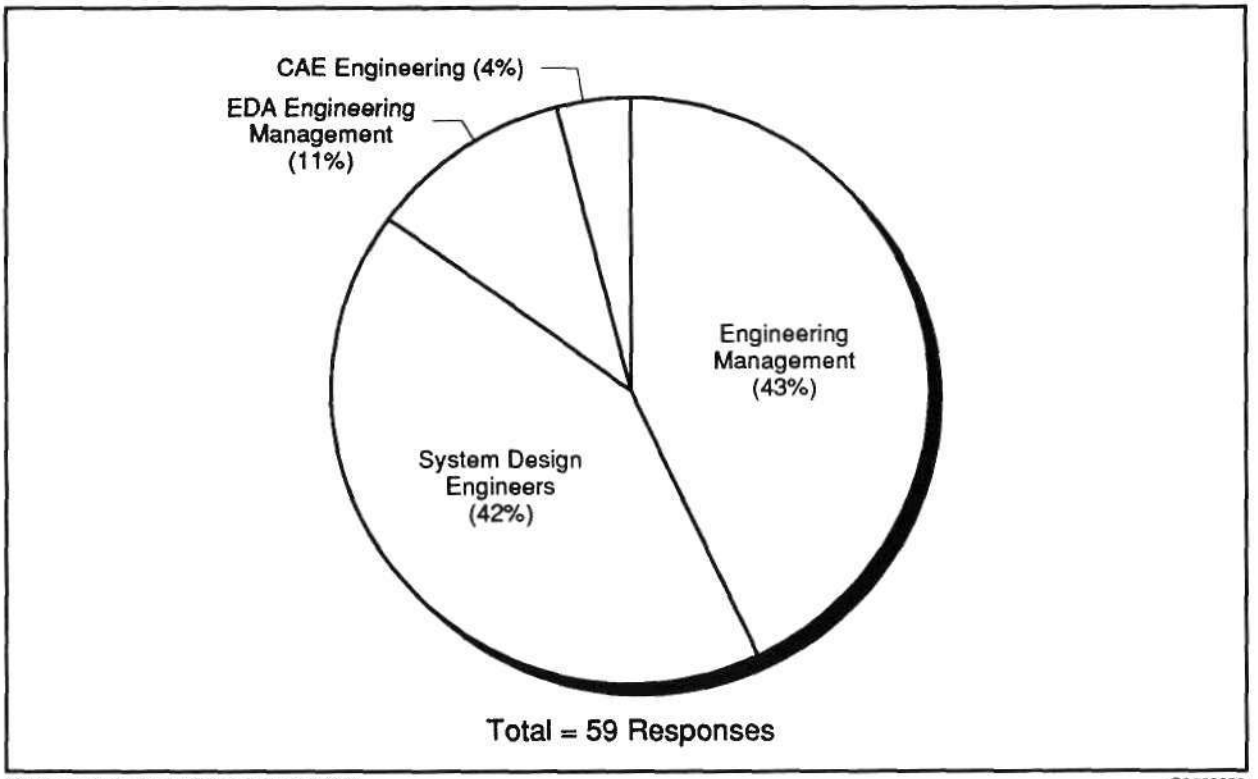
G2002397

Table 2-2
Japanese Respondents, by Application Project Team (Number of Responses)

	Project Team Responses
Data Processing	
RISC Computers	14
CISC Computers	21
Midrange Computers	10
Mainframe Computers	1
Supercomputers	1
Printers/Plotters	33
Mass Storage	10
Total Data Processing	90
Communication	
Telecom	43
Datacom	44
Total Communication	87
Military	
Aerospace/Military	12
Government	7
Total Military	19
Industrial	
Industrial Control	49
Medical Equipment	18
Test/Instrumentation	27
Total Industrial	94
Transportation	
Automotive	18
Total Transportation	18
Consumer	
Consumer	49
Total Consumer	49
Total All Applications	357

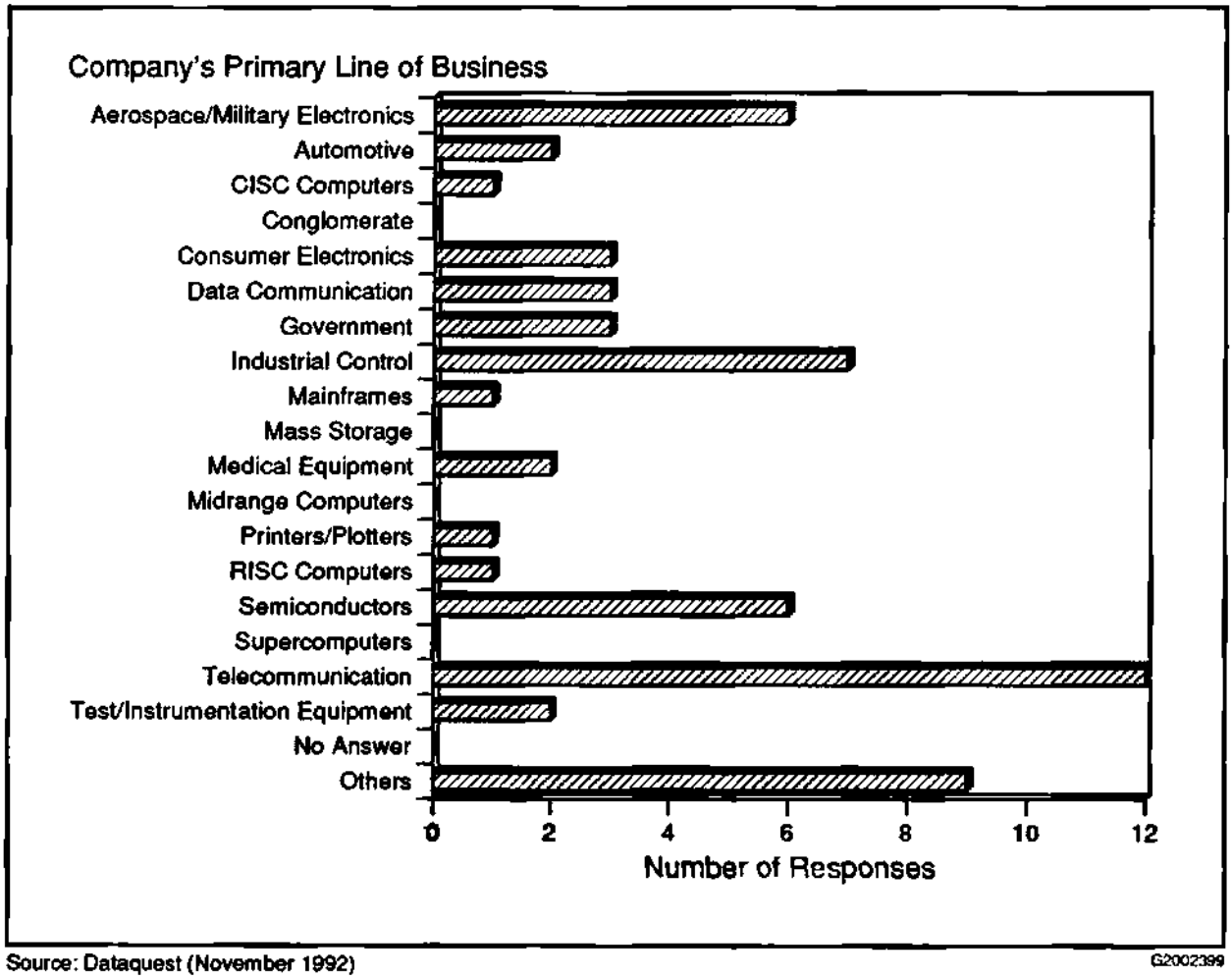
Source: Dataquest (November 1992)

Figure 2-9
European Respondents, by Job Title



Source: Dataquest (November 1992)

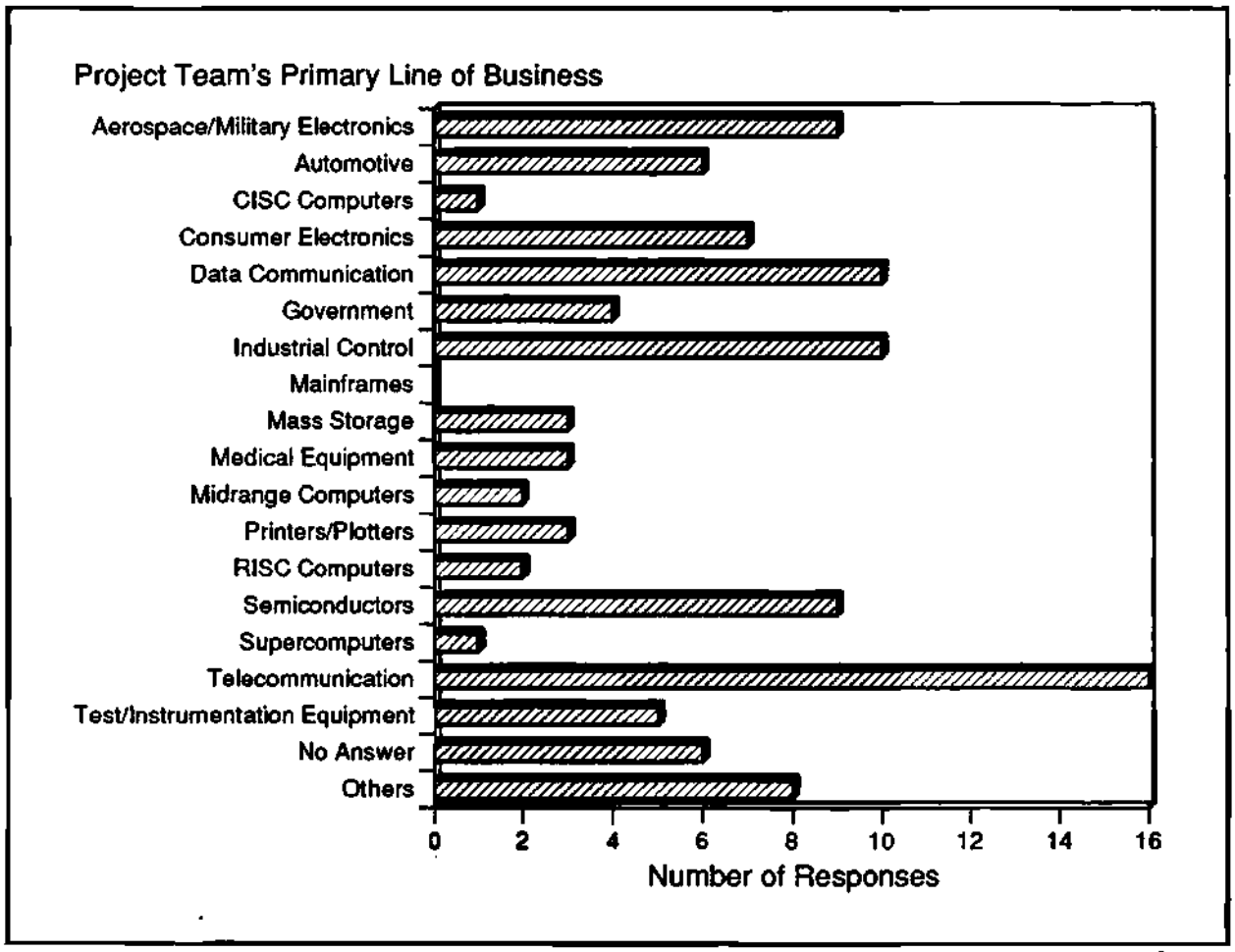
Figure 2-10
European Respondents' Primary Line of Business



Source: Dataquest (November 1992)

G2002399

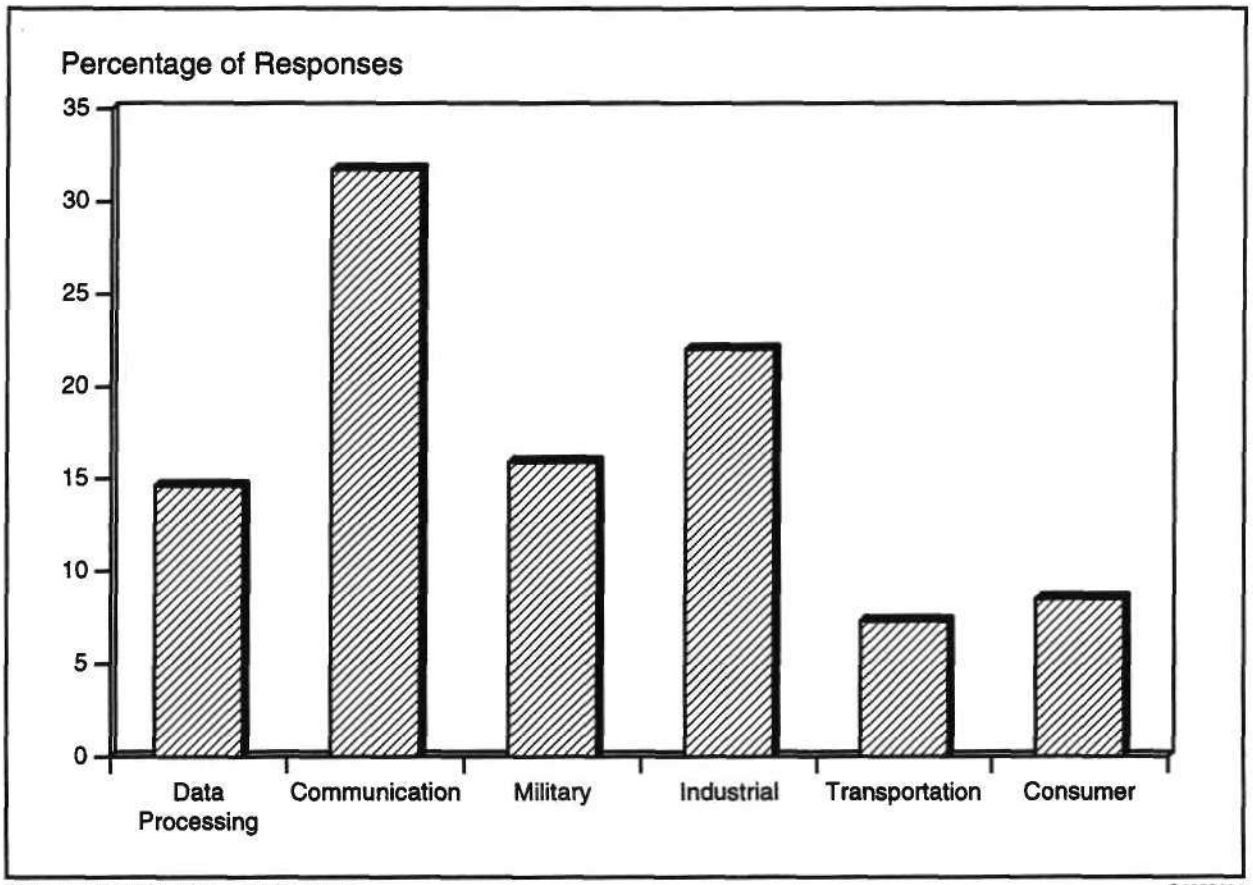
Figure 2-11
European Respondents' Project Team's Primary Line of Business



Source: Dataquest (November 1992)

G2002400

Figure 2-12
European Respondents, by Application Project Team



Source: Dataquest (November 1992)

G2002401

Chapter 3
Design Trends and Issues

The key to successfully opening the door to the ASIC market is in understanding how system designers think and how they build their products. With a better understanding of system designers' requirements on a regional basis and a product basis, specific markets can be targeted and penetrated more effectively.

In this chapter, Dataquest analyzes the critical factors that determine success for system designers, the ASIC design cycle, and the characteristics of the systems designed.

Determining Market Success for System Designers

Quantifying the factors that lead to successful products is of critical importance to all companies involved in the fast-paced electronic industry. Not surprisingly, electronic designers are cognizant of the attributes necessary for developing successful systems. Dataquest requested that each respondent select the three attributes most important to their product's future ability to achieve market success. Figures 3-1, 3-2, and 3-3 show the most important attributes that lead to market success for North America, Japan, and Europe, respectively. Figure 3-4 shows the worldwide view of the most important factors leading to market success.

While the magnitude of the response rate varied on a regional basis, the overall results were consistent. The three most important factors were as follows:

- Reducing time to market
- Reducing cost
- Increasing functionality

Increasing the reliability of the system and increasing the system speed are of secondary importance to system designers. Improving reliability of systems is less of an issue today because of the shortening product life cycles and because today's standards for quality and reliability are already high. Although increasing system speed is important and a way to differentiate product, it is not as important as getting to the market first. In short, it is more important to be quicker to the market with a cost-effective solution than to have a faster product that is late to the market.

Reducing the Design Cycle

Reducing the ASIC design cycle is of paramount importance for system designers in their never-ending battle to reduce time to market. There are two parts to the ASIC design cycle: concept to prototype, and prototype to production. Major strides are being made to reduce the ASIC design cycle in all regions of the world. Japan leads the race with the lowest time to market in both concept to prototype and prototype to production.

Japan has more than a two-month lead on Europe and a three-month lead on North America in terms of today's concept-to-prototype design cycle (see Figure 3-5). Japan also has a significant lead over Europe and especially North America in today's prototype-to-production design cycle (see Figure 3-6). As for next-generation designs, one- to two-month improvements can be seen in each region in both phases of the design cycle, with the rankings unchanged.

How is it that Japan is consistently ahead of Europe and North America in reducing the ASIC design cycle? To answer this question, Dataquest explored and contrasted Japan and North America in the following areas:

- Application mix and selected applications
- Number of engineers on a project team
- Size of ASICs being designed
- Number of signal layers on the printed circuit board
- Size of a typical board design

While it is true that the survey response in Japan comprised a different application mix than in North America (see Figure 3-7), this does not account for difference in turnaround times. Careful examination of ASIC design cycles for selected application in both regions showed that Japan had shorter design times within each application (see Figure 3-8).

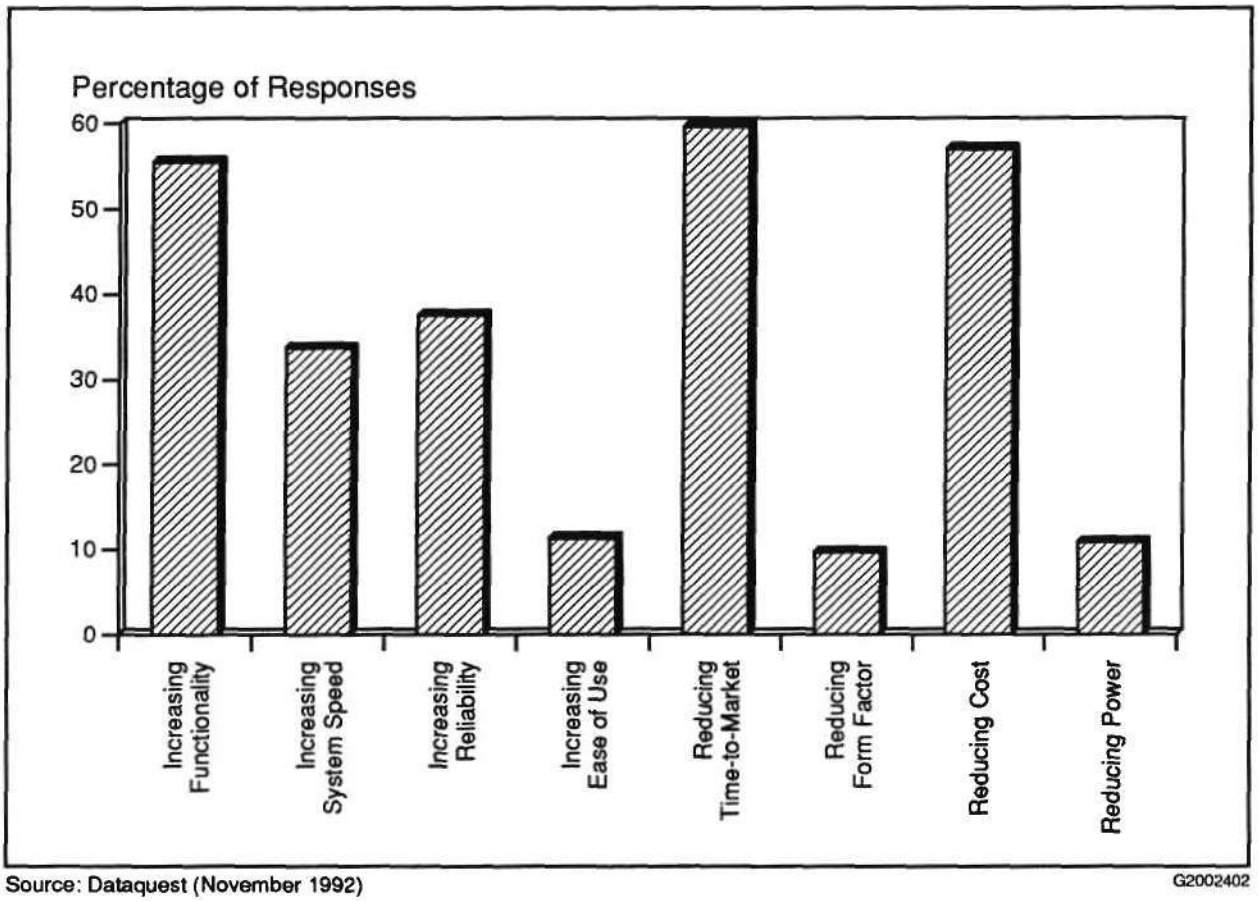
Another theory is that there may be a higher number of engineers on a design team in Japan versus North America, thus the reduced design cycle time for Japan. The data did not support this theory, and in fact, the contrary was true. The average number of engineers on a project team in North America was 14, while the average number in Japan was only 8.4. In each specific application, a consistently higher number of engineers in North America worked on a design team than in Japan. This theory did not explain the difference in design cycle times.

After further examination of the data, the answers became clear on how Japan had reduced ASIC design cycles compared with North America. First, the design cycle times for Japan are based on ASIC designs of much lower complexity than the designs in North America. The average complexity of current-generation ASIC designs in Japan is

about 18,000 gates, compared with 28,000 for designs in North America. Second, the average number of signal layers on a printed circuit board design is also substantially lower in Japan than in North America (5.7 versus 8.6 layers). Furthermore, the average number of signal layers on a printed circuit board for each application is also much lower in Japan than in North America (see Figure 3-9). If the number of signal layers on a printed circuit board is lower in Japan than in North America, the expected average size of the printed circuit board would be larger in Japan than in North America; the data supported this theory. Figure 3-10 shows the relative size of typical board designs in Japan and North America for selected applications.

In summary, system designers in Japan achieved reduced ASIC design cycle times compared with designers in North America by reducing the complexity of their ASIC designs and reducing the complexity of their printed circuit board designs. This further supports the point made in the discussion on critical factors for market success that it is more important to be quicker to the market with a cost-effective solution than to have technologically superior product late to market.

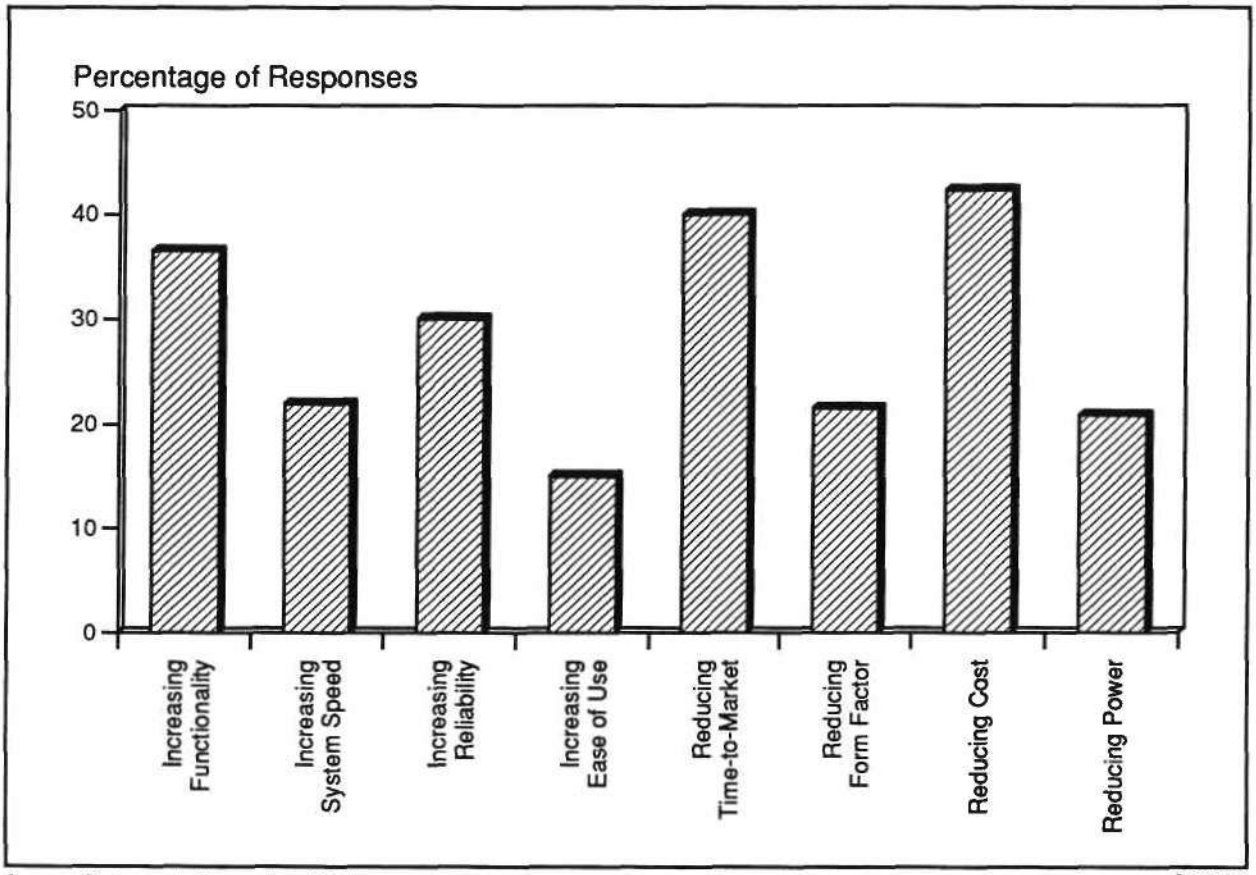
Figure 3-1
Factors Critical to Market Success: North America



Source: Dataquest (November 1992)

G2002402

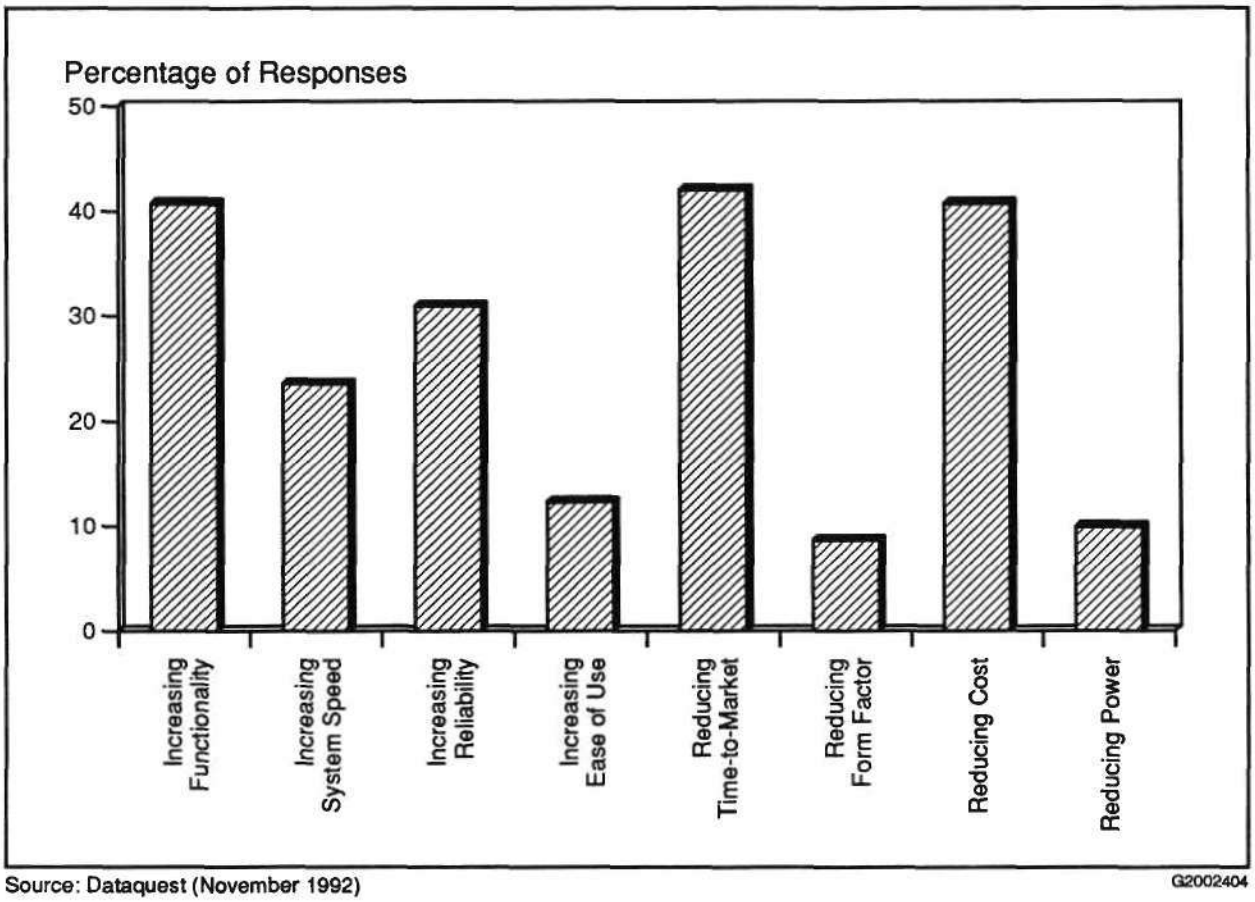
Figure 3-2
Factors Critical to Market Success: Japan



Source: Dataquest (November 1992)

G2002403

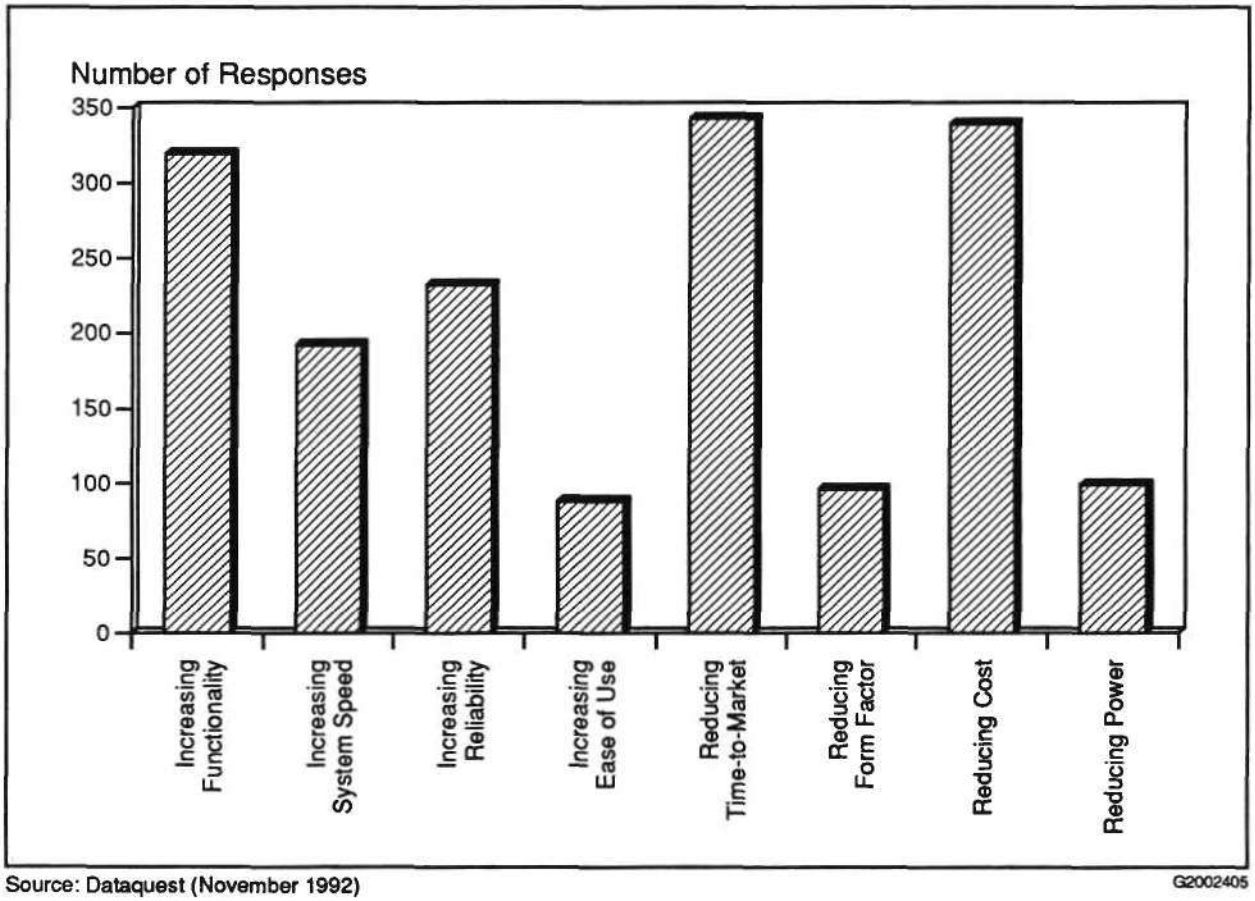
Figure 3-3
Factors Critical to Market Success: Europe



Source: Dataquest (November 1992)

G2002404

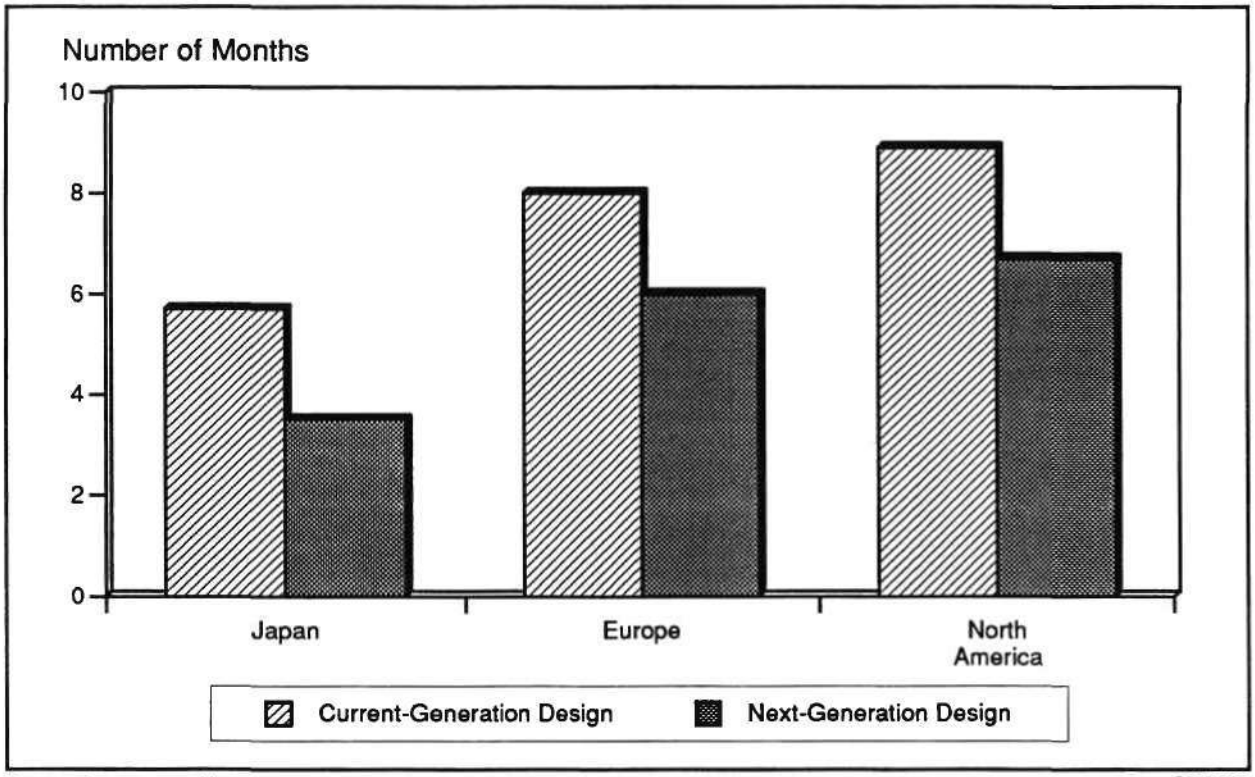
Figure 3-4
Factors Critical to Market Success: Worldwide



Source: Dataquest (November 1992)

G2002405

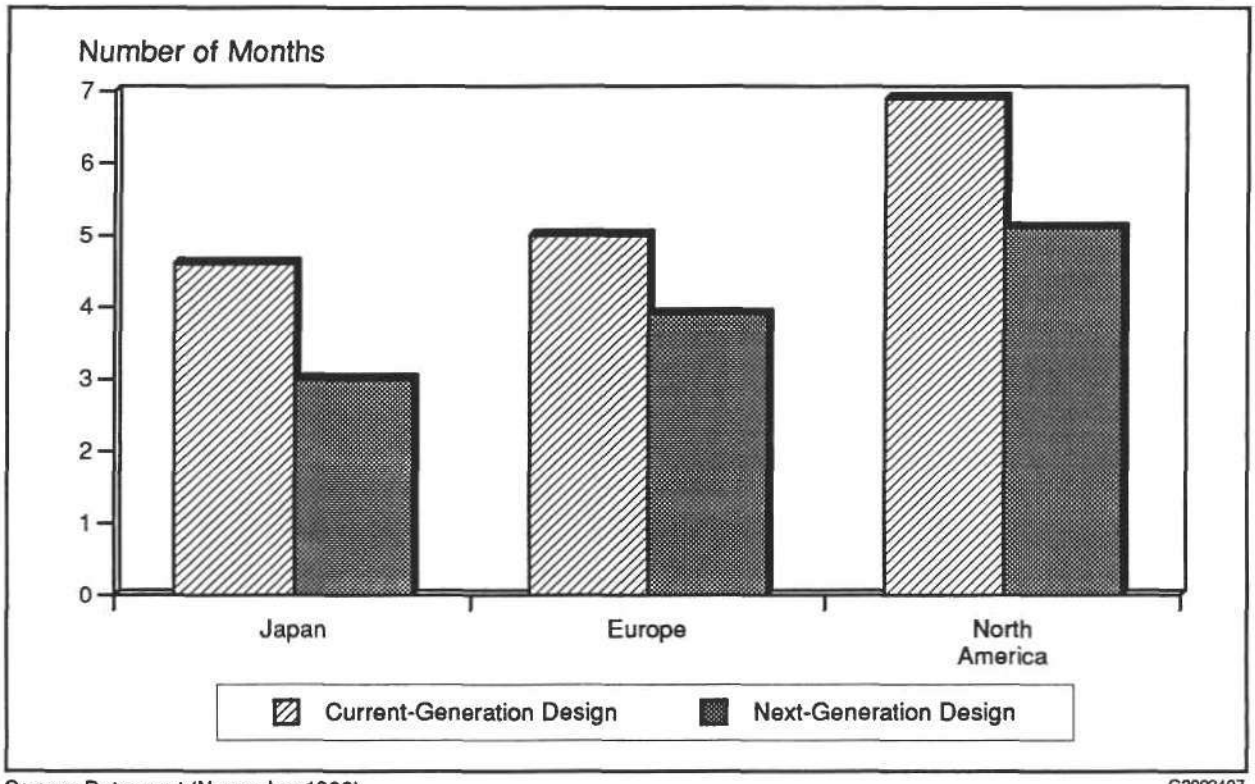
Figure 3-5
ASIC Design Cycle: Concept to Prototype



Source: Dataquest (November 1992)

G2002406

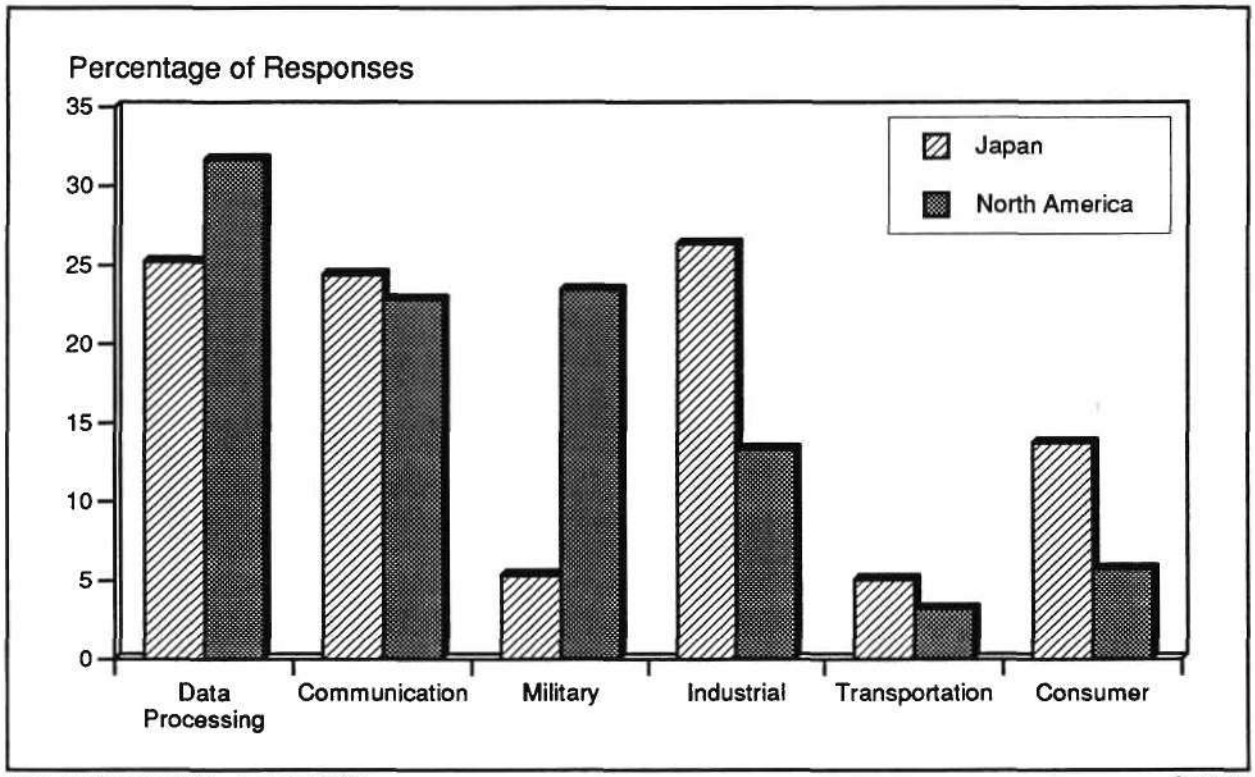
Figure 3-6
ASIC Design Cycle: Prototype to Production



Source: Dataquest (November 1992)

G2002407

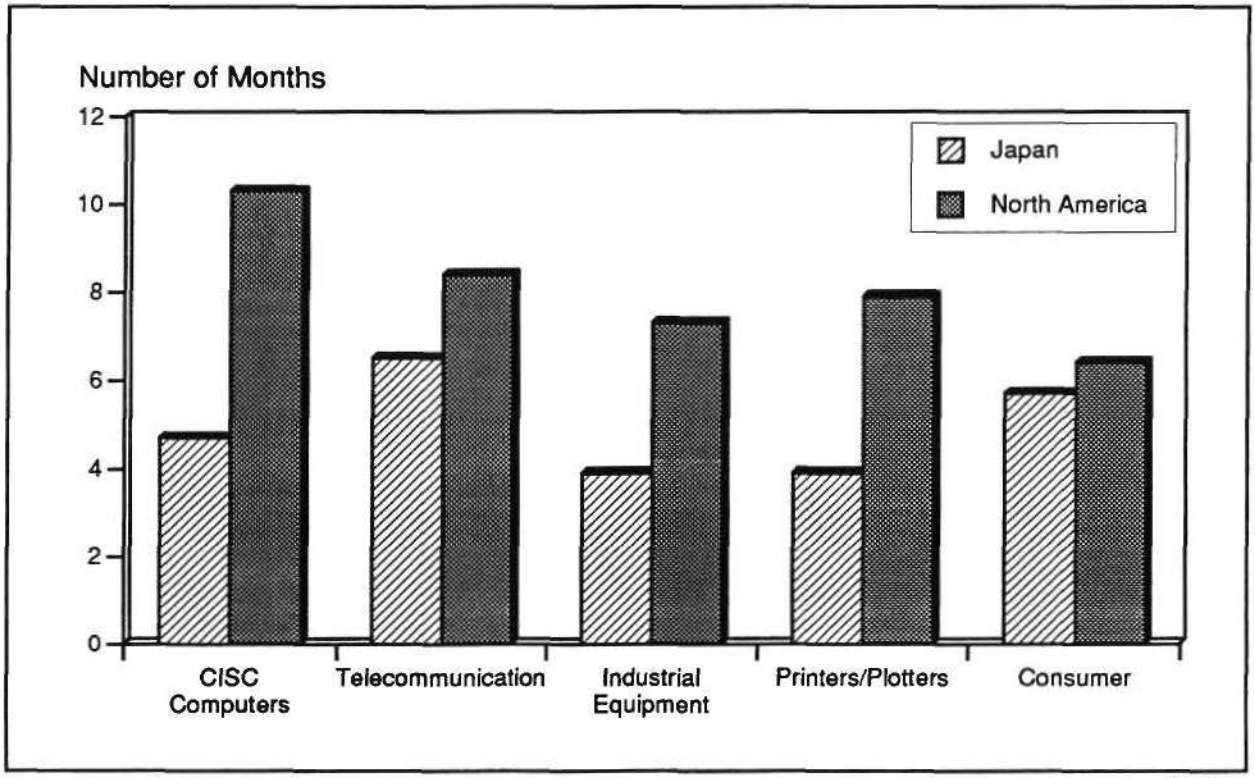
Figure 3-7
Survey Responses, by Application Project Team



Source: Dataquest (November 1992)

G2002408

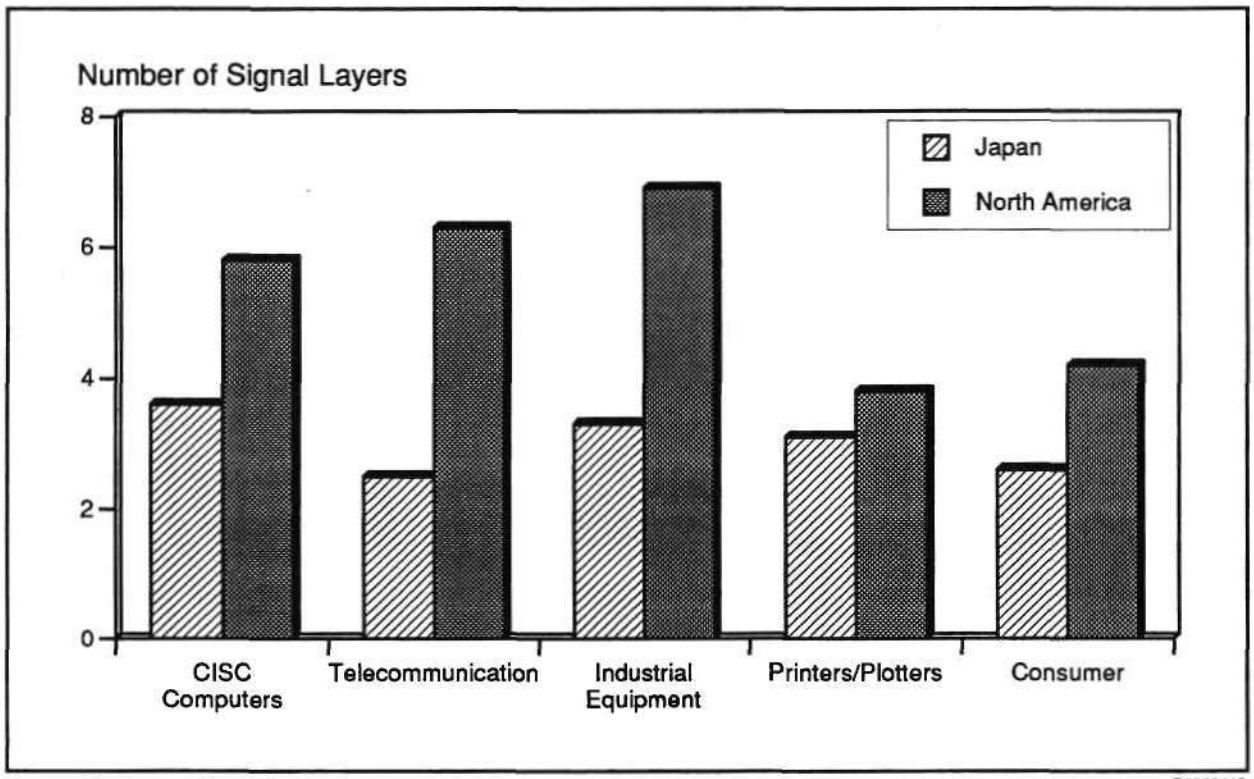
Figure 3-8
ASIC Design Cycle, by Application: Concept to Prototype



Source: Dataquest (November 1992)

G2002409

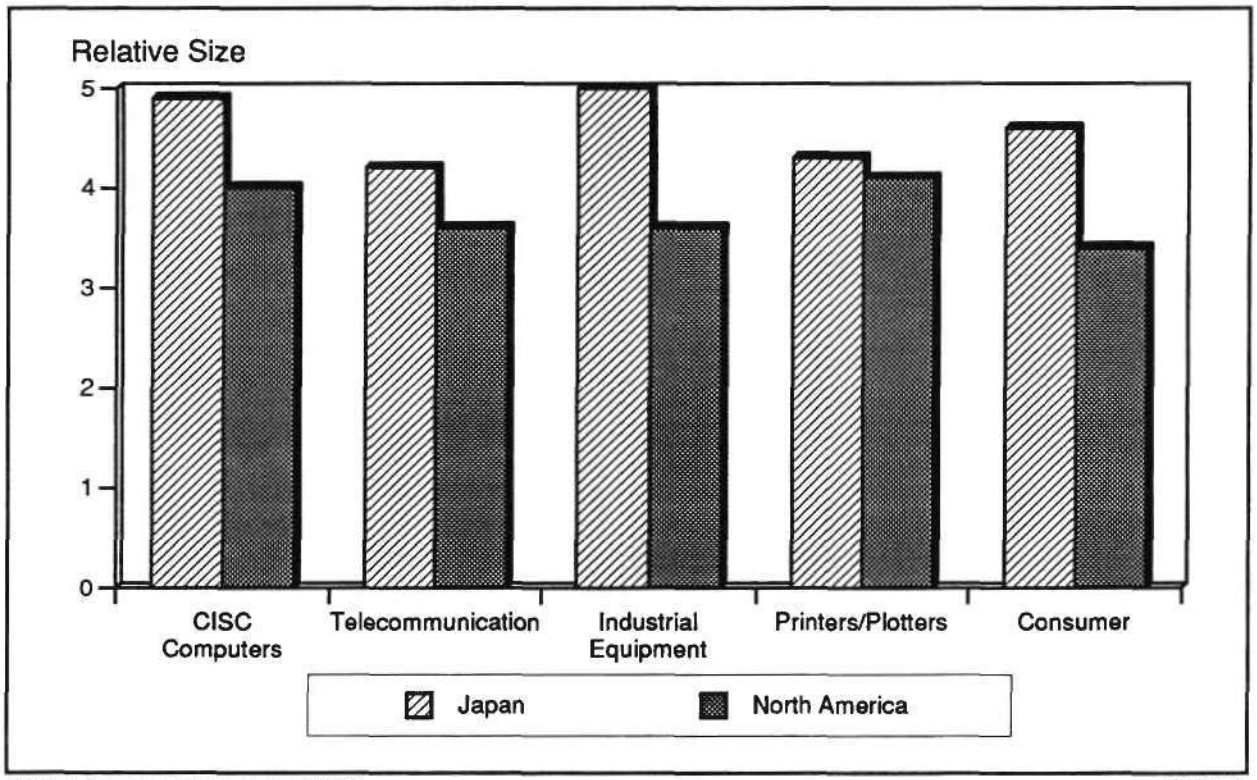
Figure 3-9
Average Number of Signal Layers per Board Design



Source: Dataquest (November 1992)

G2002410

Figure 3-10
Average Size of a Typical Board Design



Source: Dataquest (November 1992)

G2002411

Chapter 4
Product Trends

To develop and market ASIC products that are competitive in each region of the world, it is important to examine the integration levels used in ASIC design for current-generation systems and plans for next-generation system designs.

In this chapter, Dataquest explores the ASIC product trends by region and by applications, in terms of gate counts and system clock speeds.

Gate Counts, by Region

The average gate count of ASIC devices used in system designs varies widely on a regional basis. According to Dataquest's survey, the average gate count of ASICs used in Japan's current-generation system designs was 18,000; averages were 20,000 in Europe and 28,000 in North America. Figure 4-1 shows the distribution of average gate counts for the current-generation system design by region. It is important to note that FPGAs are included in the ASIC gate count distribution, thus there are high percentages of ASIC designs below 5,000 gates.

As for designs in North America, the peak of designs captured today and for the next-generation system design is in the 20,000-to-50,000-gate range (see Figure 4-2). In Japan, the peak usage of ASIC designs for the current-generation of system designs is in the 5,000-to-20,000-gate range and will move up to the 20,000-to 50,000-gate range for the next-generation system design (see Figure 4-3). Europe has a very even distribution of ASIC designs below 20,000 gates for the current-generation design. However, its peak also shifts to the 20,000-to-50,000-gate range for next-generation system design (see Figure 4-4).

The most important point that came out of examining the regional trends is that Japan system designers plan to use ASICs with much higher gate counts in their next-generation system designs, in many cases higher than North American system designers. While North American system designers will lead Japanese designers in the use of greater-than-100,000-gate devices for data processing applications, Japanese designers will lead in communication and consumer applications (see Figures 4-5, 4-6, and 4-7). Even more surprising, Japan's overall average ASIC gate count is expected to be higher than that of North America for the next-generation system design. According to Dataquest's survey, the average ASIC gate count in Japan for the

next-generation system design is expected to be 57,000 gates, compared with 54,000 for North America.

Gate Counts, by Applications

Great opportunity lies within the data processing market for high-density ASICs. Fifty percent of the RISC computer designers in North America said that their average ASIC gate counts will exceed 100,000 gates on their next-generation computer design. While most of the CISC computer designers said their next-generation ASIC designs will be in the 20,000-to-50,000-gate range, a large portion of the midrange, mainframe, and supercomputer designers will use ASICs with an excess of 100,000 gates. Figures 4-8 and 4-9 show the distribution of average ASIC gate counts for data processing applications in North America and Japan, respectively.

The communications market has a need for a wide variety of ASICs. While the peak usage of today's ASICs for communications applications in Japan is in the 10,000-to-20,000-gate range (20,000 to 50,000 in North America), much higher density ASICs will be employed in the next-generation systems (see Figures 4-10 and 4-11). Telecommunication and data communication show comparable gate count distributions for both current- and next-generation system design.

Today's industrial market can be characterized as a low-gate-count business (see Figures 4-12 and 4-13). However, there is opportunity for midrange ASICs in next-generation industrial control systems and test/instrumentation equipment. Japan is expected to use high-end ASICs in industrial control systems and medical equipment.

While military applications represent only a small portion of the ASIC designs in Japan, they represent more than 15 percent of all ASIC designs in North America. Military designers use a wide variety of ASIC (see Figure 4-14). Although this market traditionally has been closed to non-North American suppliers, many military designers are now evaluating ASICs manufactured outside North America. The military offers high profit margins to its ASIC suppliers, although it is a low-volume business.

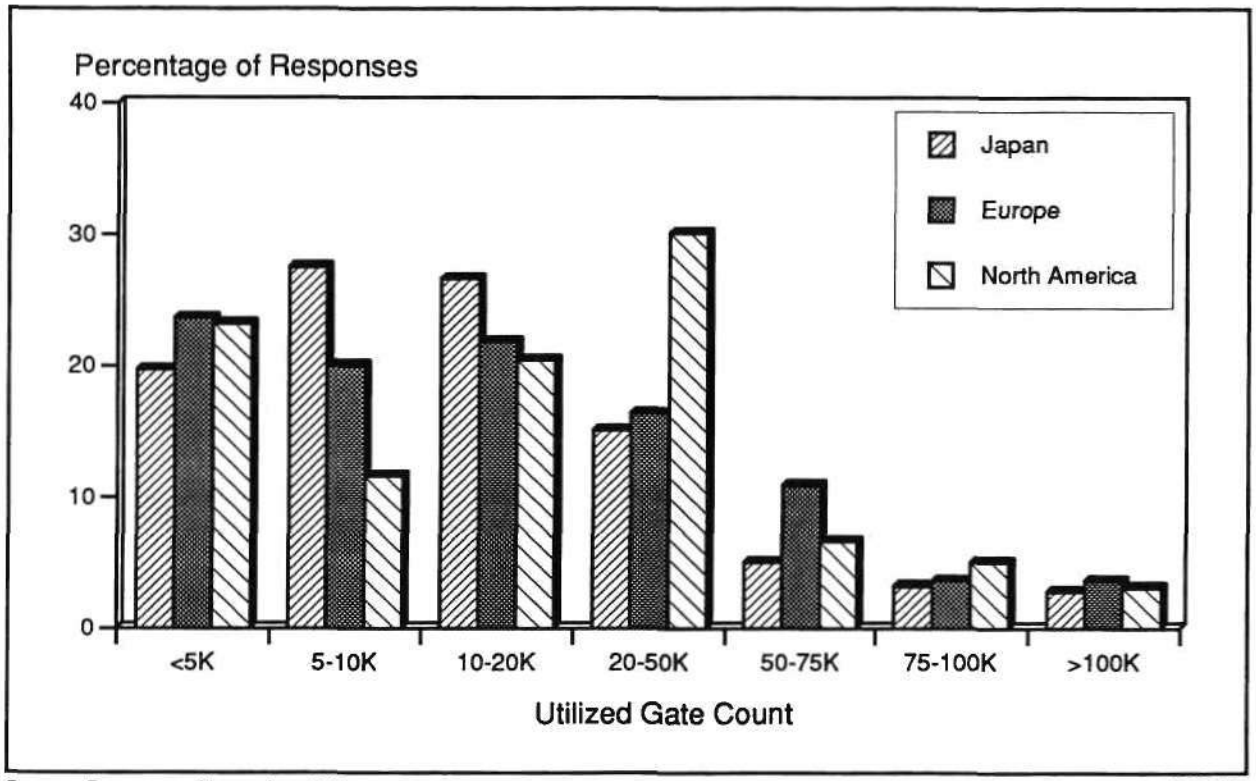
Consumer is a large market in Japan and a growing market in North America. Japan has been using low-to-midrange ASICs for most of its current-generation consumer systems. However, we see a strong demand for high-density ASICs in the next-generation products (see Figure 4-15). Dataquest believes that HDTV will play a major role in developing high-density ASICs in Japan.

Transportation is a small market for ASICs in both North America and Japan. The European survey had a small sample in many application areas. Tables 4-1 and 4-2 show average North American ASIC design starts for current-generation and next-generation designs by application markets. Tables 4-3 and 4-4 show average Japan ASIC design starts by applications.

System Clock Speeds

Just as the opportunity for high-density ASICs continues to accelerate, so does the need for high-speed ASICs. Figure 4-16 shows the highest digital clock frequencies used in today's North American system designs. Figure 4-17 shows the distribution of the digital clock frequencies in Japan. The distribution for North America and Japan is similar; both curves peak at the 20-to-25-MHz range and both curves have a large distribution over 33 MHz. Products that drove the peak in the 20-to-25-MHz range were printers, plotters, telecommunication, data communication, military, and medical equipment. RISC computers, CISC computers, mass storage, telecommunication, data communication, and test equipment were major contributors to the 41-to-99-MHz range. Figure 4-18 shows the opportunity for applications with digital clock frequencies of 100 MHz and greater.

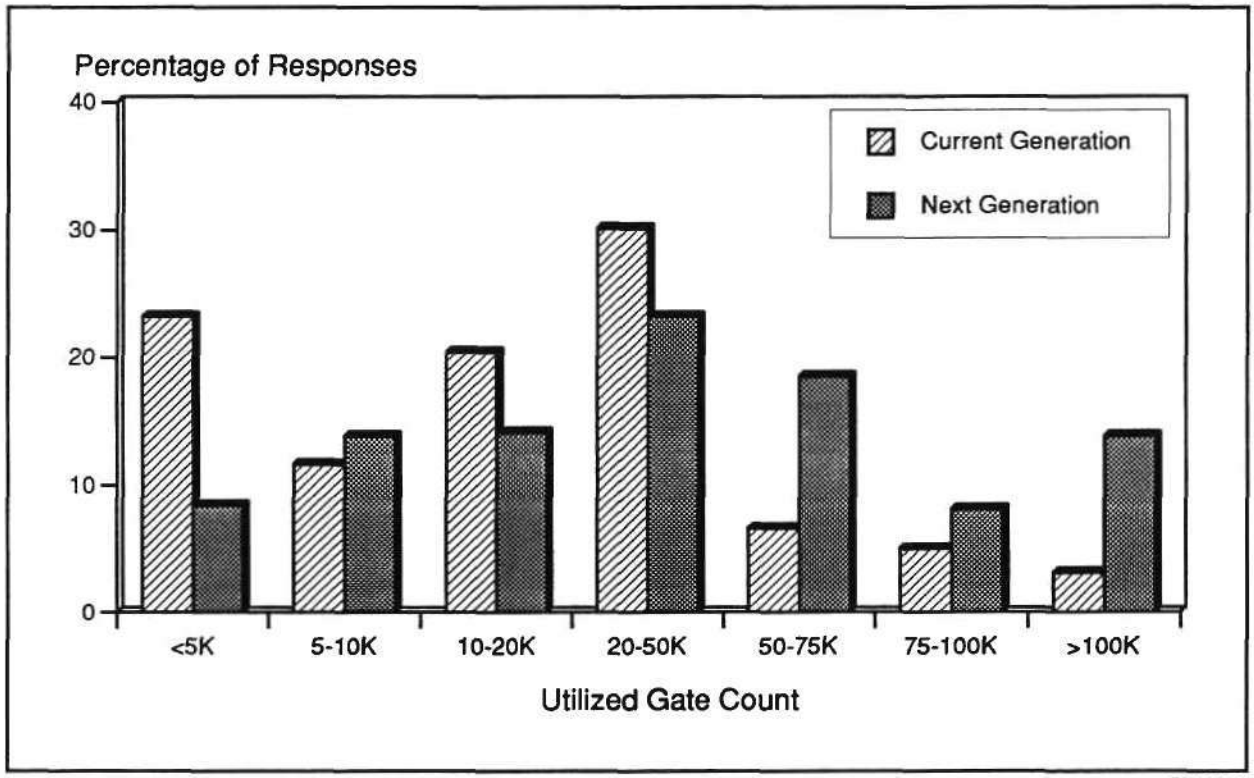
Figure 4-1
ASIC Design Starts, by Average Gate Count: Current-Generation Design



Source: Dataquest (November 1992)

G2002412

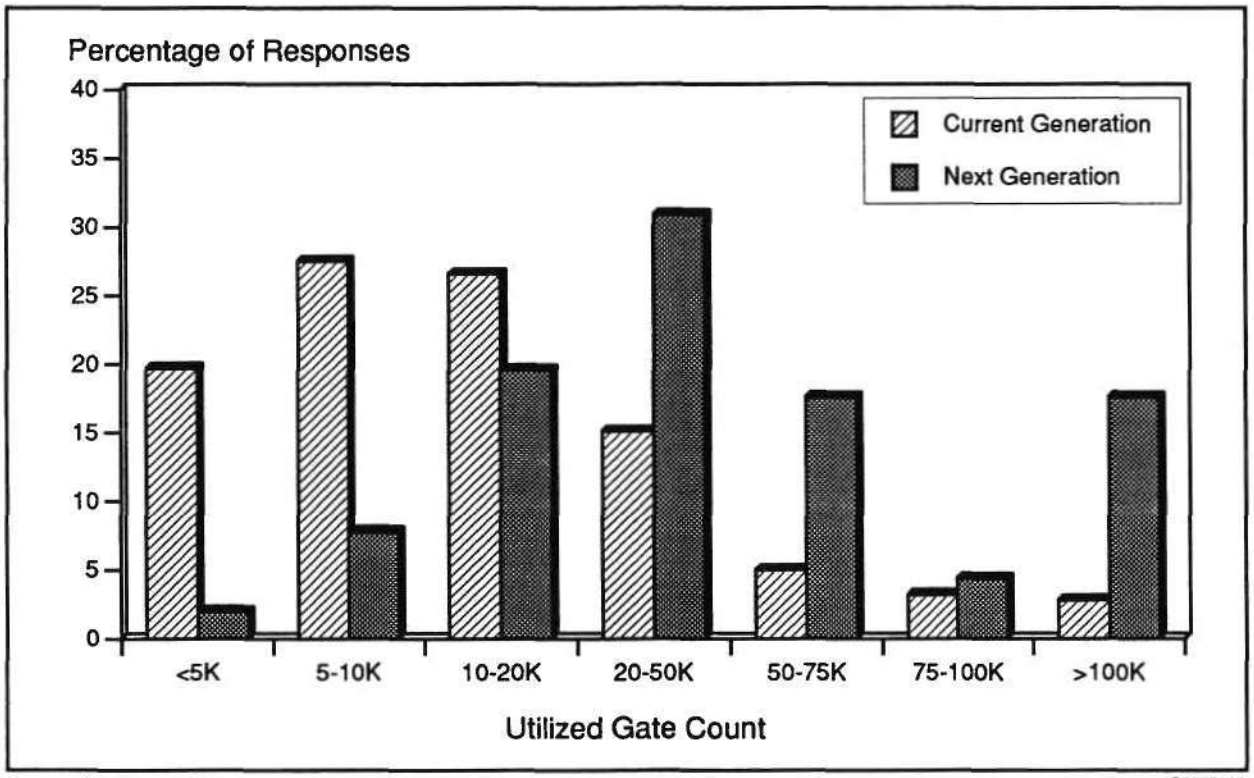
Figure 4-2
ASIC Design Starts, by Average Gate Count: North America



Source: Dataquest (November 1992)

G2002413

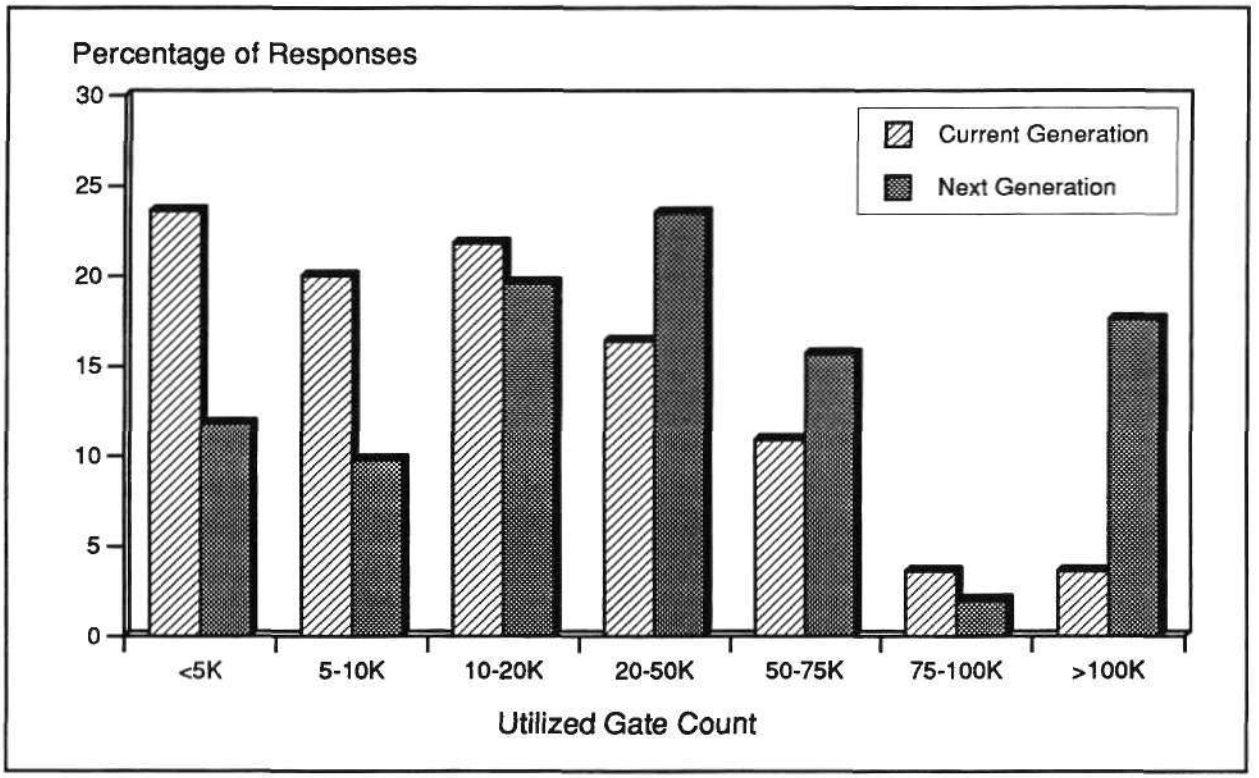
Figure 4-3
ASIC Design Starts, by Average Gate Count: Japan



Source: Dataquest (November 1992)

G2002414

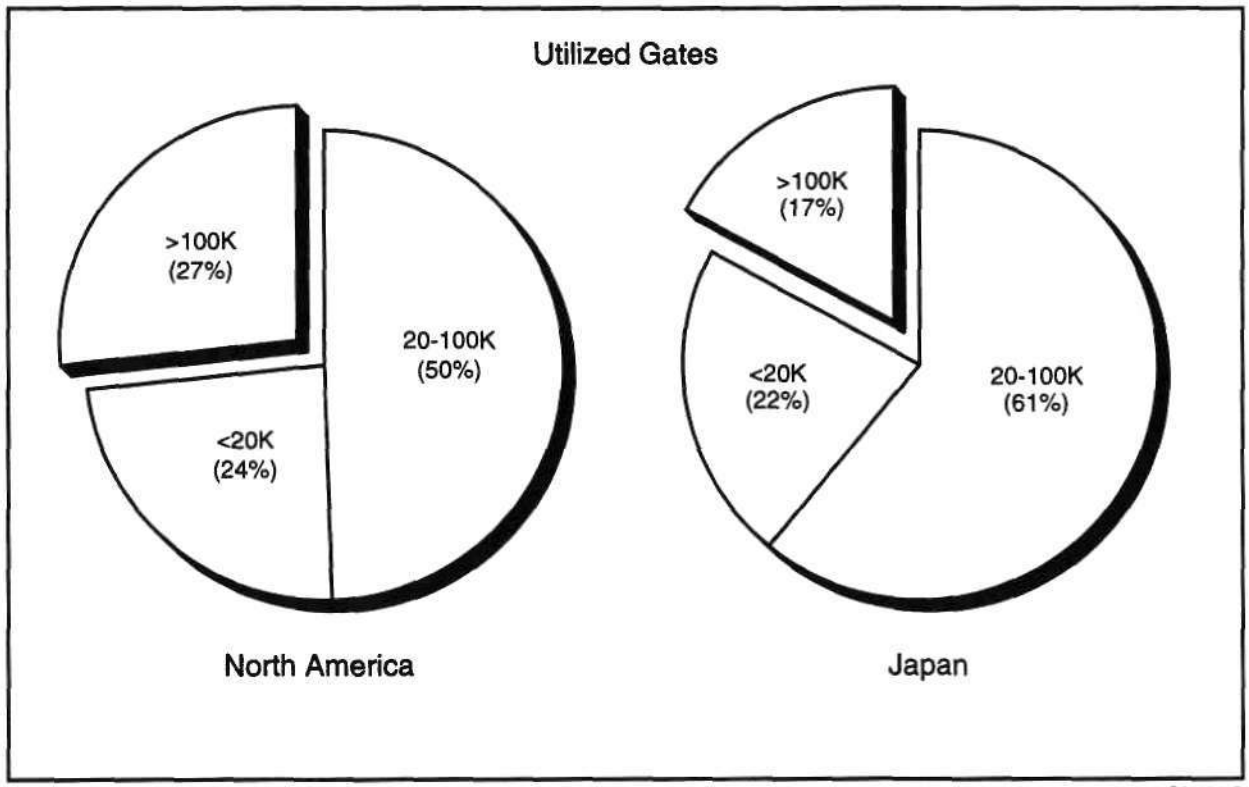
Figure 4-4
ASIC Design Starts, by Average Gate Count: Europe



Source: Dataquest (November 1992)

G2002415

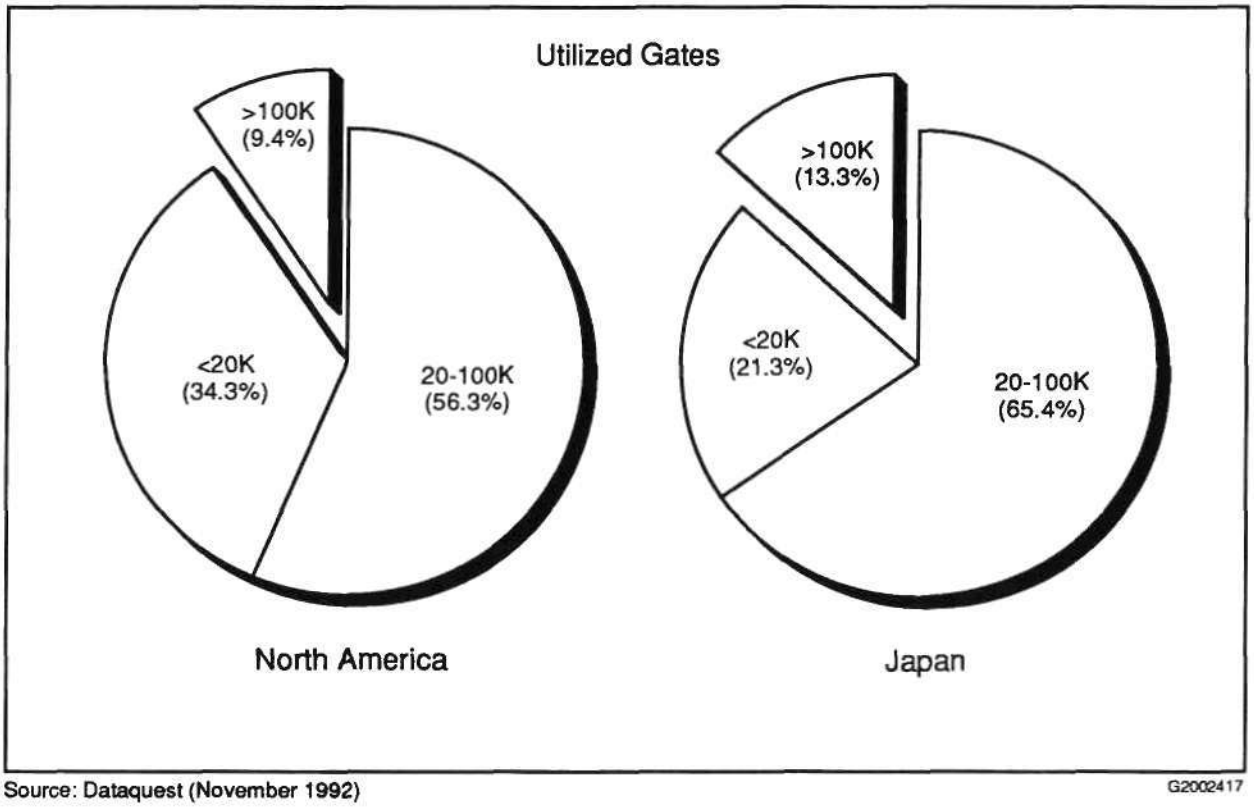
Figure 4-5
Next-Generation ASIC Design Starts: Data Processing



Source: Dataquest (November 1992)

G2002416

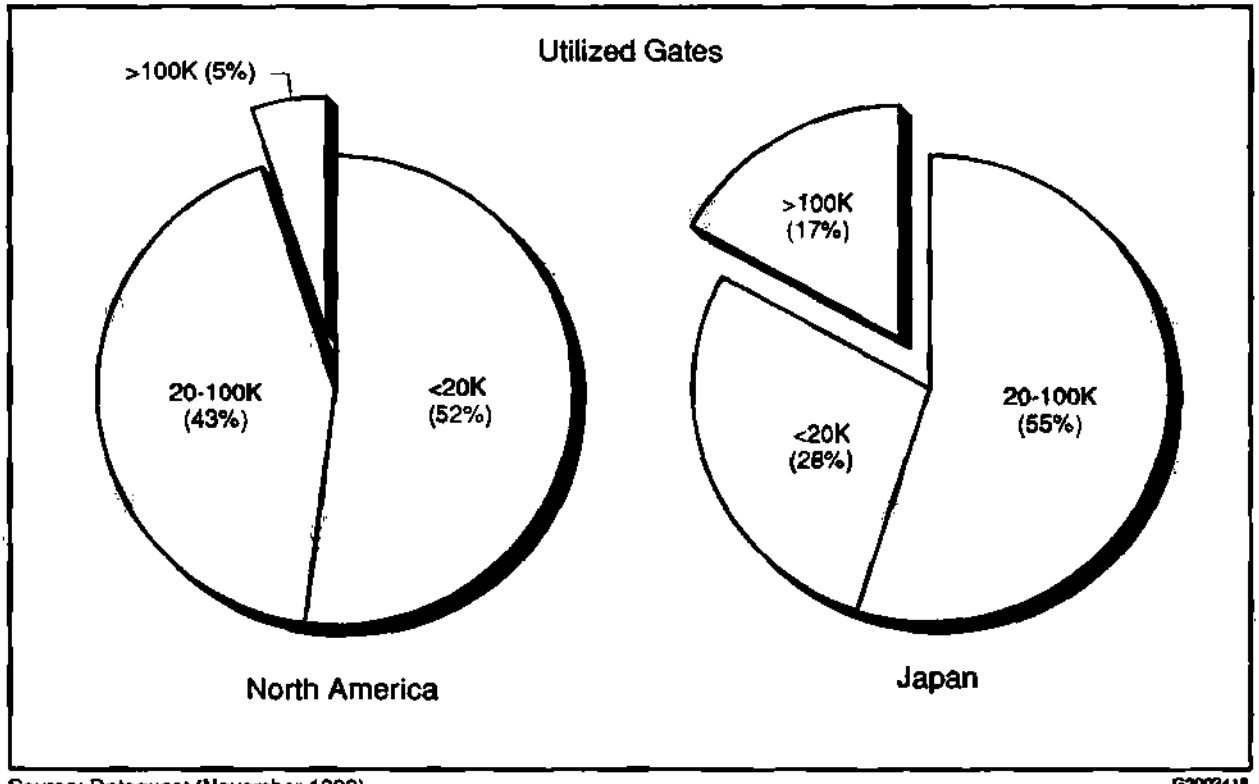
Figure 4-6
Next-Generation ASIC Design Starts: Communication



Source: Dataquest (November 1992)

G2002417

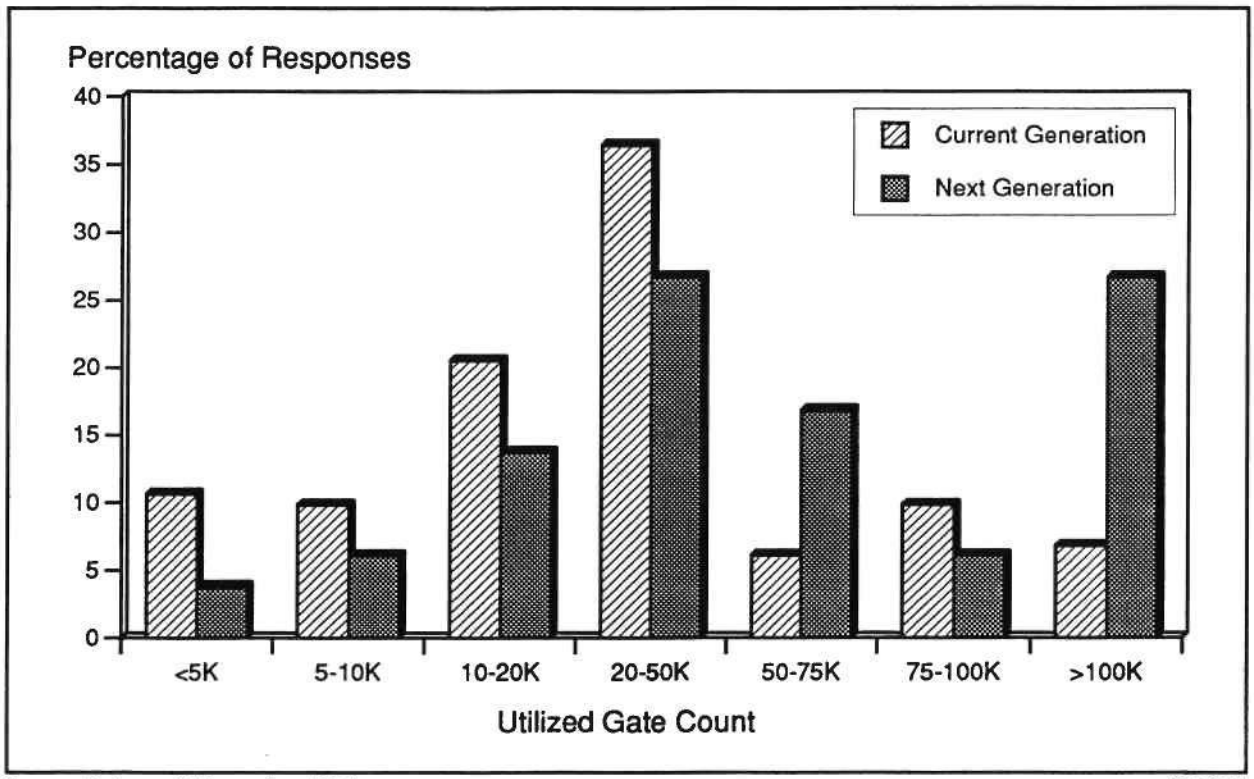
Figure 4-7
Next-Generation ASIC Design Starts: Consumer



Source: Dataquest (November 1992)

G2002418

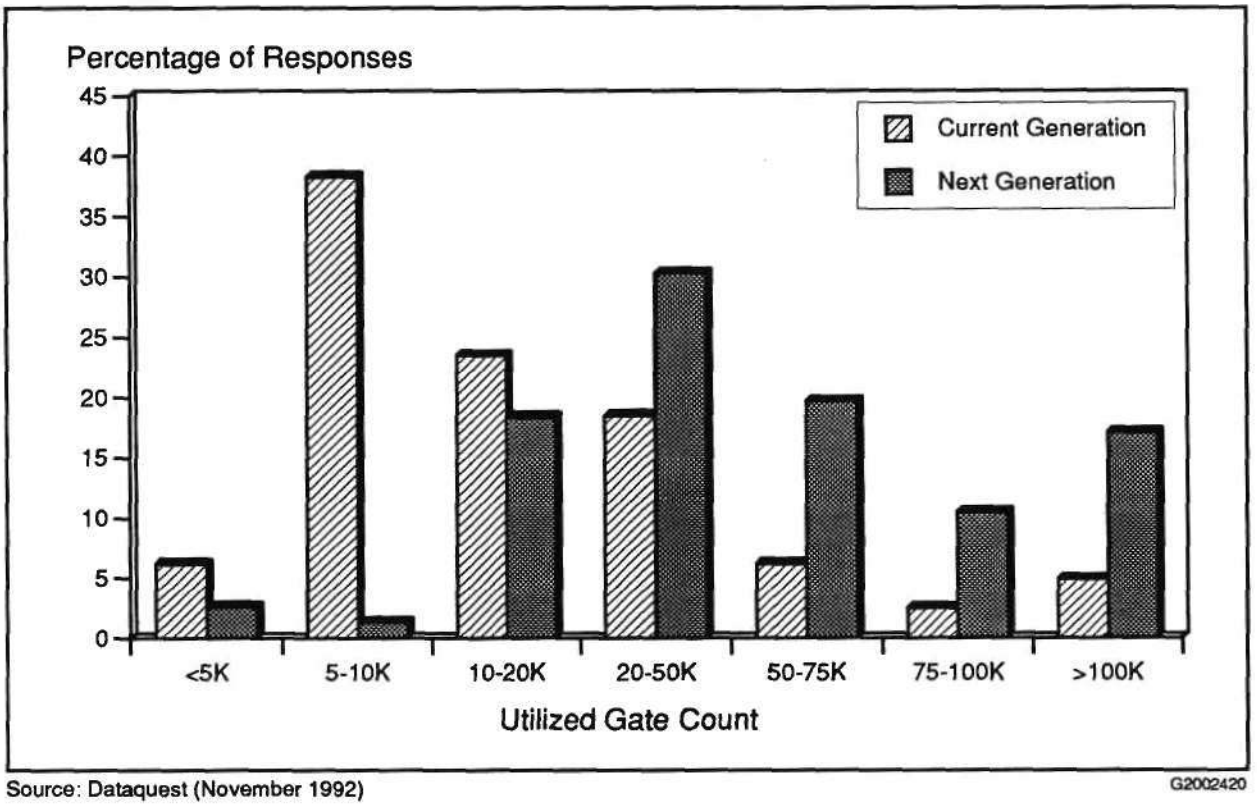
Figure 4-8
North American ASIC Design Starts: Data Processing



Source: Dataquest (November 1992)

G2002419

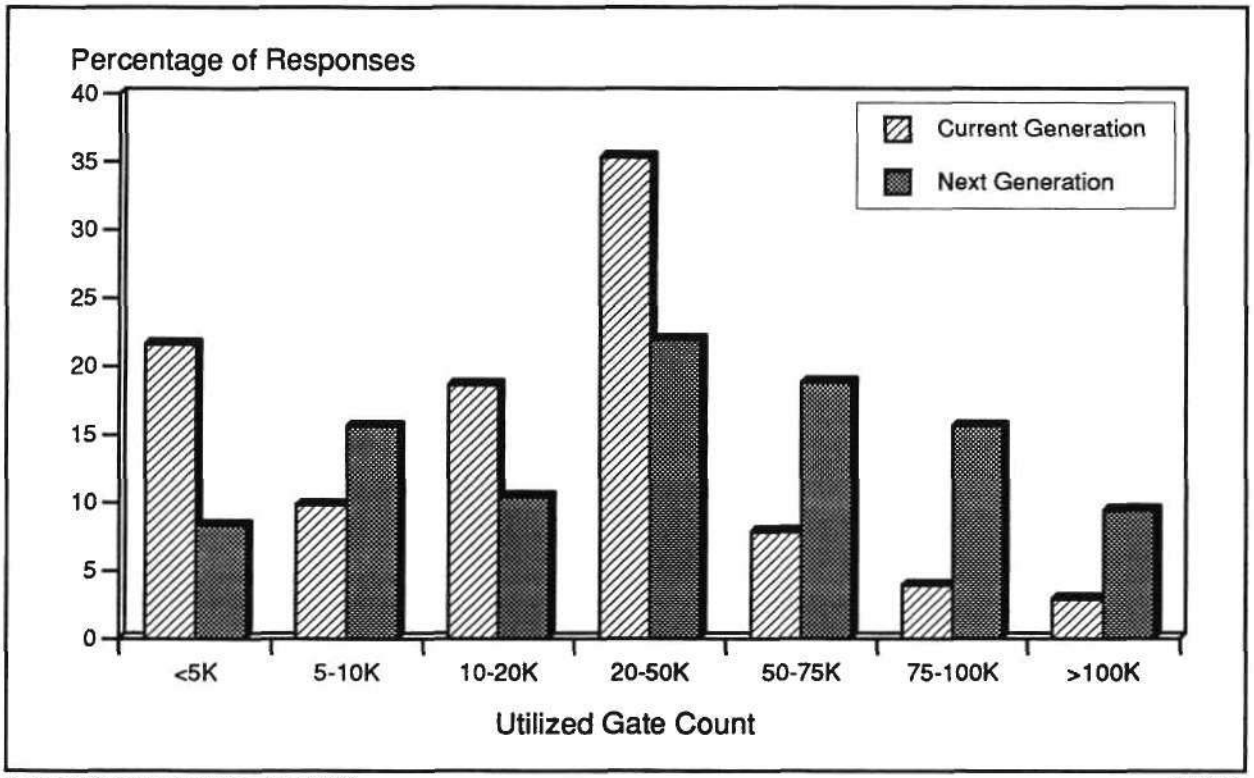
Figure 4-9
Japanese ASIC Design Starts: Data Processing



Source: Dataquest (November 1992)

G2002420

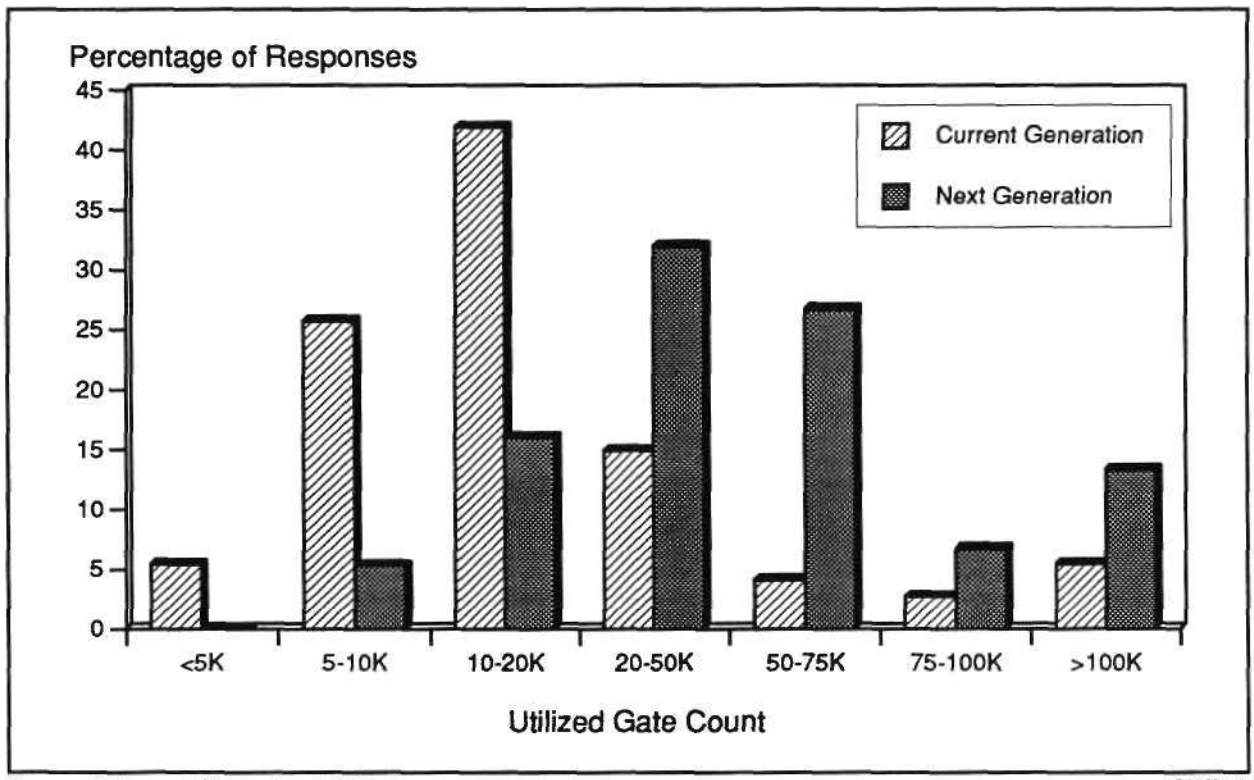
Figure 4-10
North American ASIC Design Starts: Communication



Source: Dataquest (November 1992)

G2002421

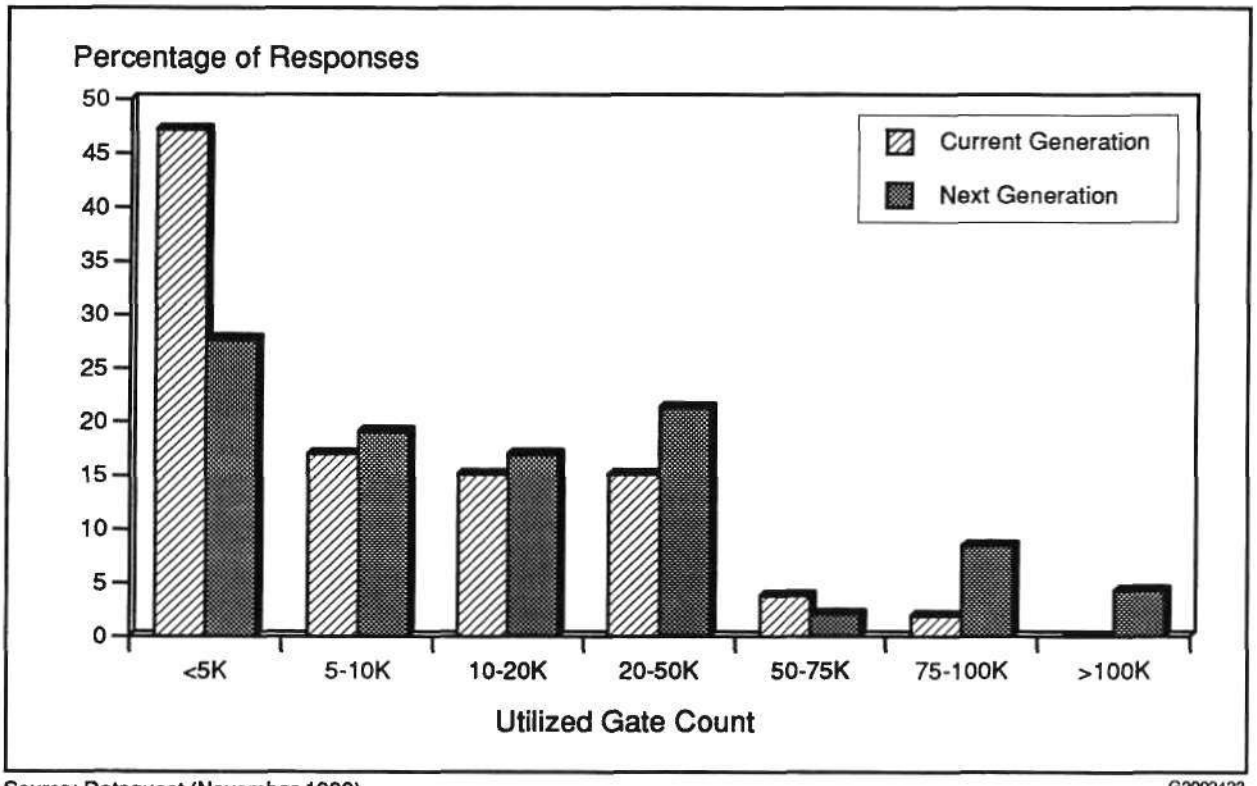
Figure 4-11
Japanese ASIC Design Starts: Communication



Source: Dataquest (November 1992)

G2002422

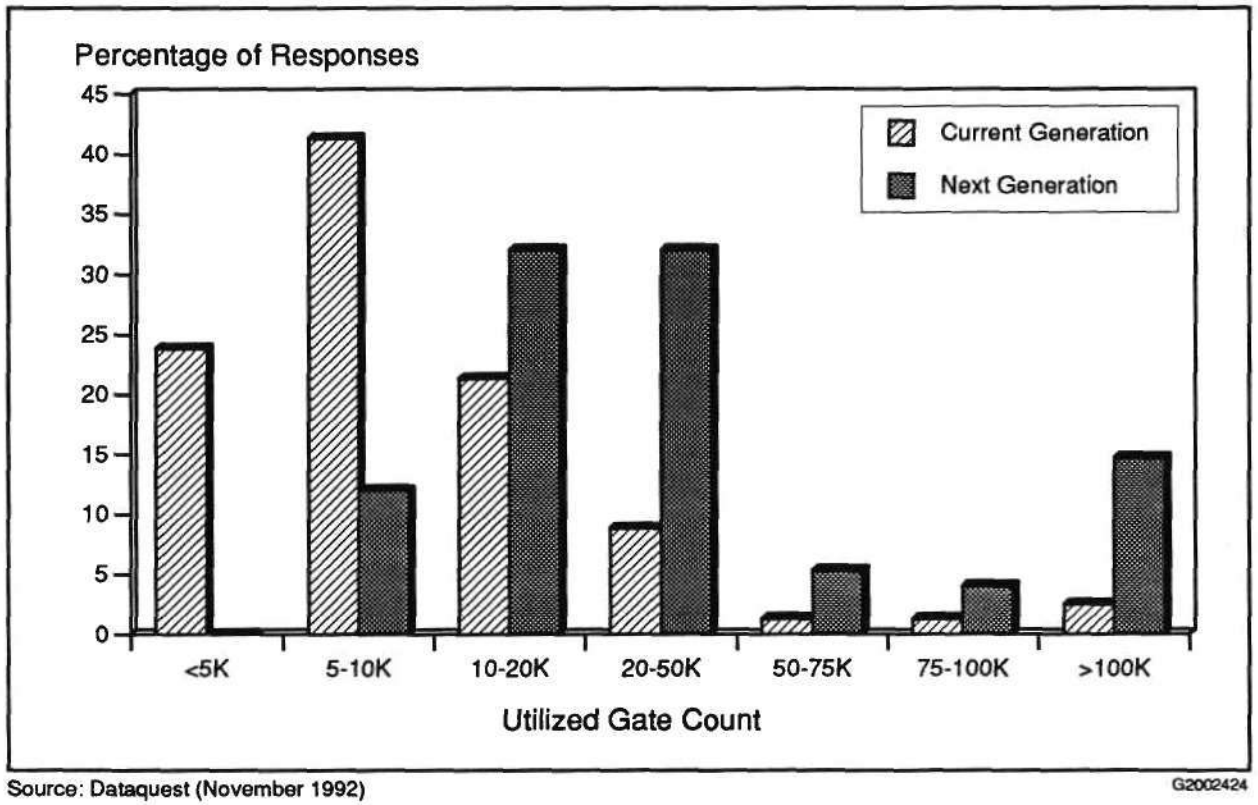
Figure 4-12
North American ASIC Design Starts: Industrial



Source: Dataquest (November 1992)

G2002423

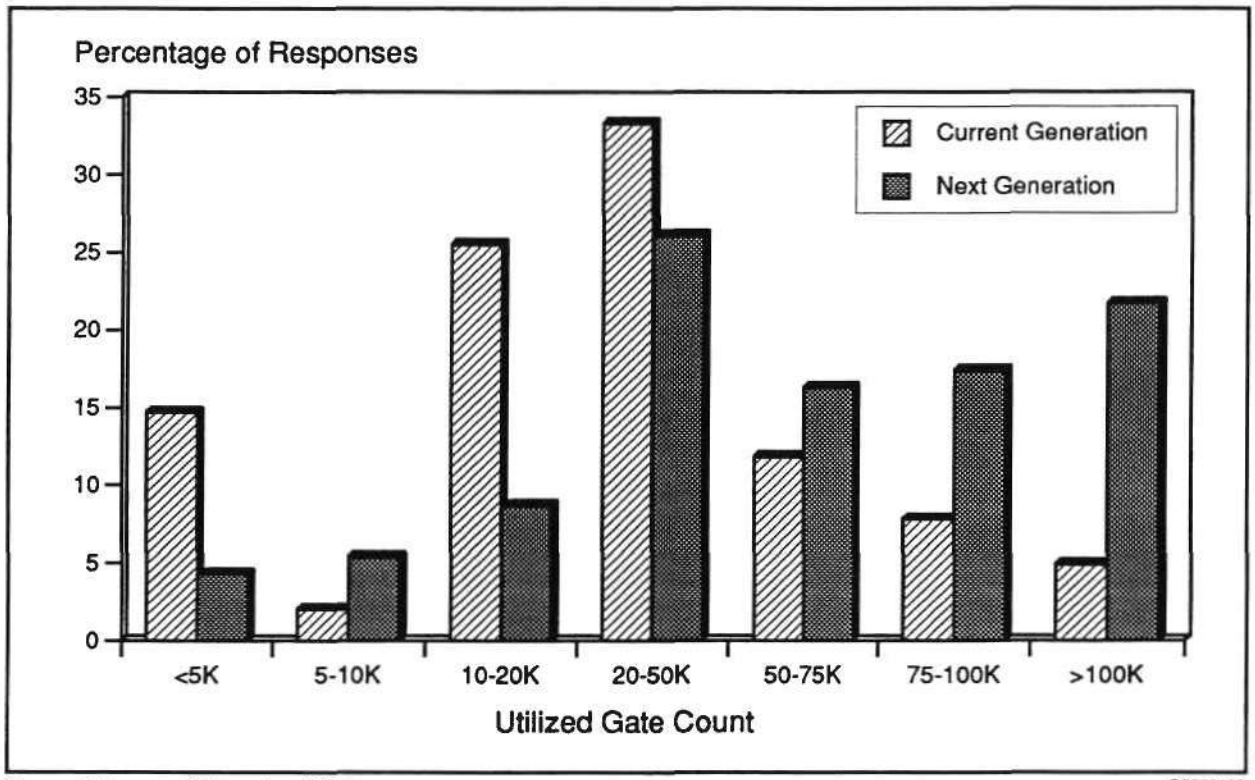
Figure 4-13
Japanese ASIC Design Starts: Industrial



Source: Dataquest (November 1992)

G2002424

Figure 4-14
North American ASIC Design Starts: Military



Source: Dataquest (November 1992)

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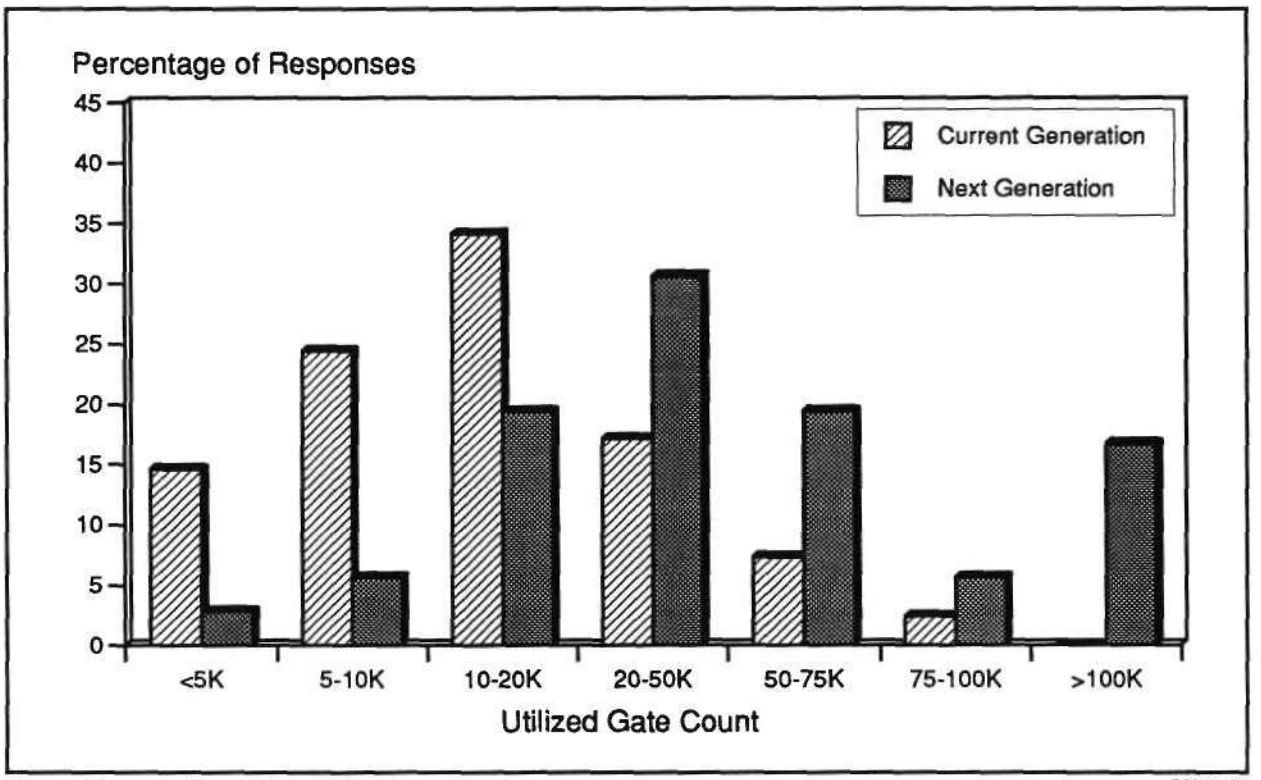
Figure 4-15
Japanese ASIC Design Starts: Consumer



Source: Dataquest (November 1992)

G2002426

Table 4-1
North American ASIC Design Starts, by Application: Average Size of Current-Generation Design (Percentage of Respondents)

Utilized Gates	Data Processing	Communication	Military	Industrial	Transportation	Consumer
4,999 or Fewer	10.6	21.6	14.7	47.2	28.6	52.2
5,000 to 9,999	9.8	9.8	2.0	17.0	7.1	4.3
10,000 to 19,999	20.5	18.6	25.5	15.1	28.6	17.4
20,000 to 49,999	36.4	35.3	33.3	15.1	28.6	17.4
50,000 to 74,999	6.1	7.8	11.8	3.8	7.1	0
75,000 to 99,999	9.8	3.9	7.8	1.9	0	4.3
100,000 and Greater	6.8	2.9	4.9	0	0	4.3
Total	100.0	100.0	100.0	100.0	100.0	100.0

Note: Columns may not add to 100 percent because of rounding.
Source: Dataquest (November 1992)

Table 4-2
North American ASIC Design Starts, by Application: Average Size of Next-Generation Design
(Percentage of Respondents)

Utilized Gates	Data Processing	Communication	Military	Industrial	Transportation	Consumer
4,999 or Fewer	3.8	8.3	4.3	27.7	0	19.0
5,000 to 9,999	6.1	15.6	5.4	19.1	23.1	14.3
10,000 to 19,999	13.7	10.4	8.7	17.0	30.8	19.0
20,000 to 49,999	26.7	21.9	26.1	21.3	15.4	14.3
50,000 to 74,999	16.8	18.8	16.3	2.1	7.7	9.5
75,000 to 99,999	6.1	15.6	17.4	8.5	7.7	19.0
100,000 and Greater	26.7	9.4	21.7	4.3	15.4	4.8
Total	100.0	100.0	100.0	100.0	100.0	100.0

Note: Columns may not add to 100 percent because of rounding.
Source: Dataquest (November 1992)

Table 4-3
Japanese ASIC Design Starts, by Application: Average Size of Current-Generation Design
(Percentage of Respondents)

Utilized Gates	Data Processing	Communication	Military	Industrial	Transportation	Consumer
4,999 or Fewer	6.2	5.4	27.8	23.8	31.3	14.6
5,000 to 9,999	38.3	25.7	33.3	41.3	37.5	24.4
10,000 to 19,999	23.5	41.9	22.2	21.3	31.3	34.1
20,000 to 49,999	18.5	14.9	5.6	8.8	0	17.1
50,000 to 74,999	6.2	4.1	5.6	1.3	0	7.3
75,000 to 99,999	2.5	2.7	5.6	1.3	0	2.4
100,000 and Greater	4.9	5.4	0	2.5	0	0
Total	100.0	100.0	100.0	100.0	100.0	100.0

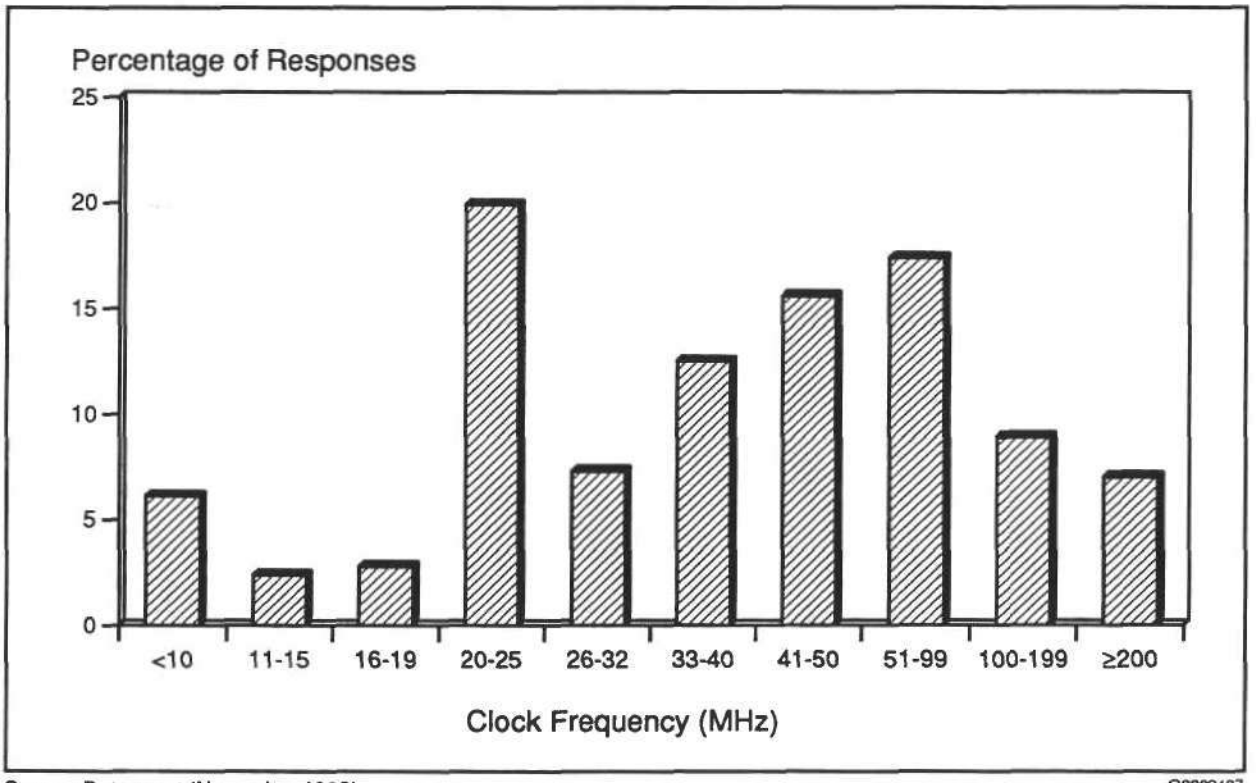
Note: Columns may not add to 100 percent because of rounding.
Source: Dataquest (November 1992)

Table 4-4
Japanese ASIC Design Starts, by Application: Average Size of Next-Generation Design
(Percentage of Respondents)

Utilized Gates	Data Processing	Communication	Military	Industrial	Transportation	Consumer
4,999 or Fewer	2.6	0	0	0	0	2.8
5,000 to 9,999	1.3	5.3	0	12.0	14.3	5.6
10,000 to 19,999	18.4	16.0	37.5	32.0	50.0	19.4
20,000 to 49,999	30.3	32.0	31.3	32.0	28.6	30.6
50,000 to 74,999	19.7	26.7	6.3	5.3	7.1	19.4
75,000 to 99,999	10.5	6.7	0	4.0	0	5.6
100,000 and Greater	17.1	13.3	25.0	14.7	0	16.7
Total	100.0	100.0	100.0	100.0	100.0	100.0

Note: Columns may not add to 100 percent because of rounding.
Source: Dataquest (November 1992)

Figure 4-16
Highest Digital Clock Frequency Used in Design: North America



Source: Dataquest (November 1992)

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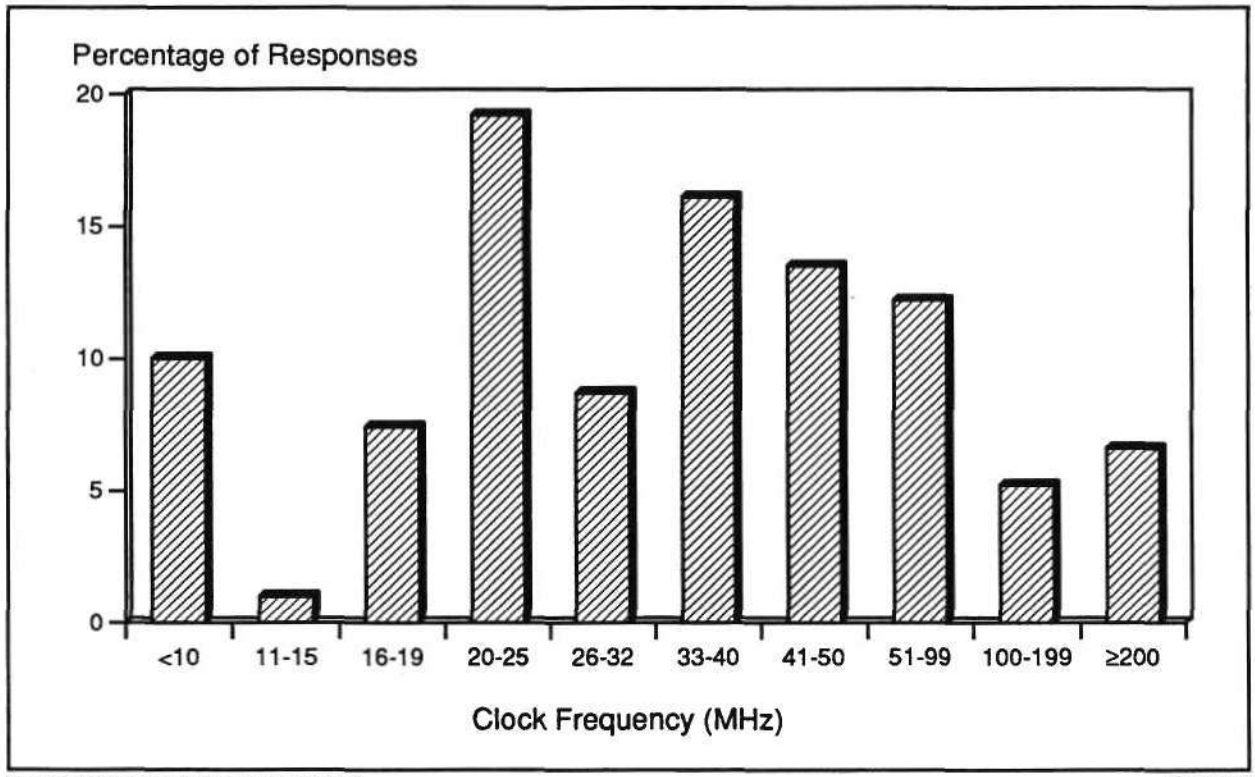
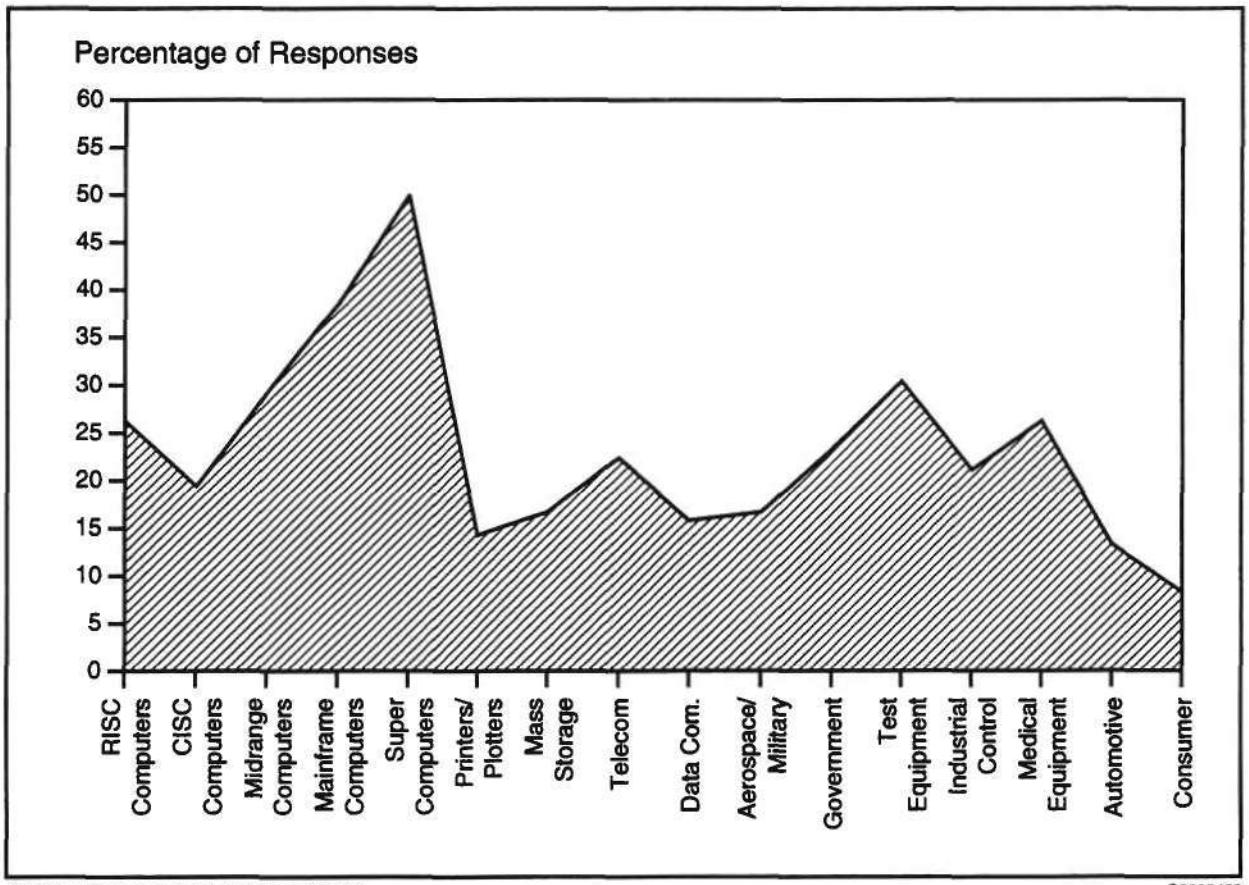
Figure 4-17
Highest Digital Clock Frequency Used in Design: Japan



Source: Dataquest (November 1992)

G2002428

Figure 4-18
Applications with Highest Digital Clock Frequency ≥100 MHz: North America



Source: Dataquest (November 1992)

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Chapter 5
Emerging Technology

Long-standing questions have faced the ASIC industry regarding emerging technologies. What impact will BiCMOS and GaAs have on the ASIC market? What applications will these technologies be used in? While there continues to be ongoing debate on how much value BiCMOS and GaAs have over CMOS from ASIC suppliers, Dataquest solicited opinions on these technologies from system designers, whose perceptions, after all, can make or break a market.

In this chapter, Dataquest measures the perceived demand of BiCMOS, ECL, and GaAs from system designers in both North America and Japan. We explore the impact that BiCMOS and GaAs ASICs will have in selected applications.

Two important notes concern the data presented in this chapter. First, Dataquest asked system designers to check a box for the ASIC technologies they currently use in their system design and for which technologies they plan to use in their next-generation systems. It is much easier to check a box than actually buy the product. Second, system designers do not state how much of the system is a given technology; it could be 98 percent CMOS and 2 percent BiCMOS and they would check the box regarding BiCMOS use. Both points lead to the same conclusion: The results are good for measuring a trend, but the magnitude of the results should be considered optimistic.

Technology Perception Comparison

There is clearly a strong perceived value of BiCMOS ASICs in next-generation system designs. When comparing BiCMOS, ECL, and GaAs ASICs in North America and Japan, the results showed an outstanding interest in BiCMOS ASICs and a secondary interest in GaAs ASICs (see Figure 5-1). While ECL ASICs showed some potential growth from current-generation design to next-generation design, the growth is small when compared with BiCMOS and GaAs ASICs, as one would expect.

BiCMOS ASICs

As mentioned earlier, there was an overwhelmingly positive statement from system designers that they plan to use BiCMOS ASICs in their next-generation system designs. Nearly 40 percent of system designers in all applications believe that they will need at least one BiCMOS ASIC in their next-generation system. This high use of

BiCMOS ASICs in all types of next-generation system design holds true in both North America and Japan (see Figures 5-2 and 5-3).

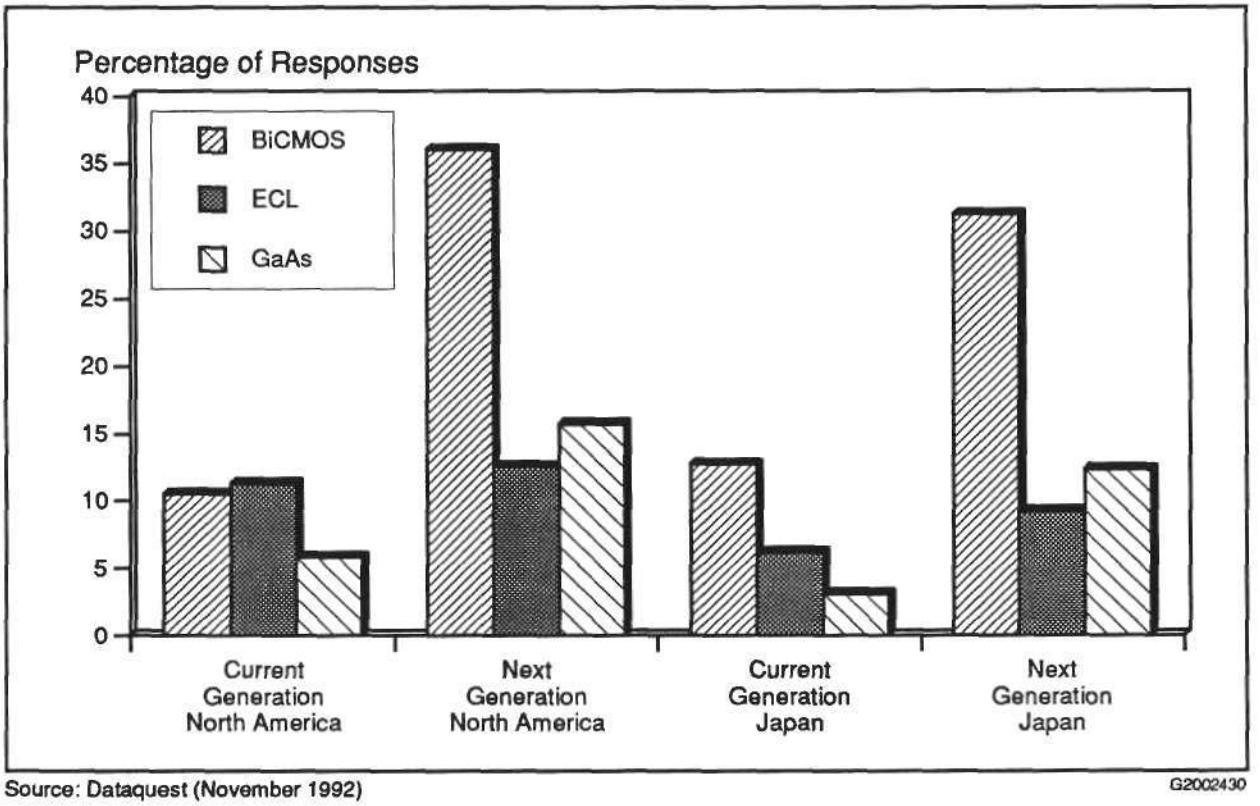
Forty-five percent of the data processing system designers in North America said they would use at least one BiCMOS ASIC in the next-generation system design. This is a powerful statement, considering that data processing is the largest ASIC market in North America and accounts for more than 50 percent of the dollar market. RISC system designers are the largest users of BiCMOS ASICs today. However, the survey results showed that BiCMOS ASICs will be used in more than 40 percent of all types of next-generation computer design, from CISC computers to supercomputers (see Figure 5-4).

GaAs ASICs

Users perceive GaAs ASICs as more of a niche product than BiCMOS ASICs. Military and computer system designers are expected to be among the larger users of GaAs ASICs in both North America and Japan (see Figures 5-5 and 5-6). Transportation showed high use of GaAs ASICs in North America, but this should be discounted because of the small survey response rate in this area.

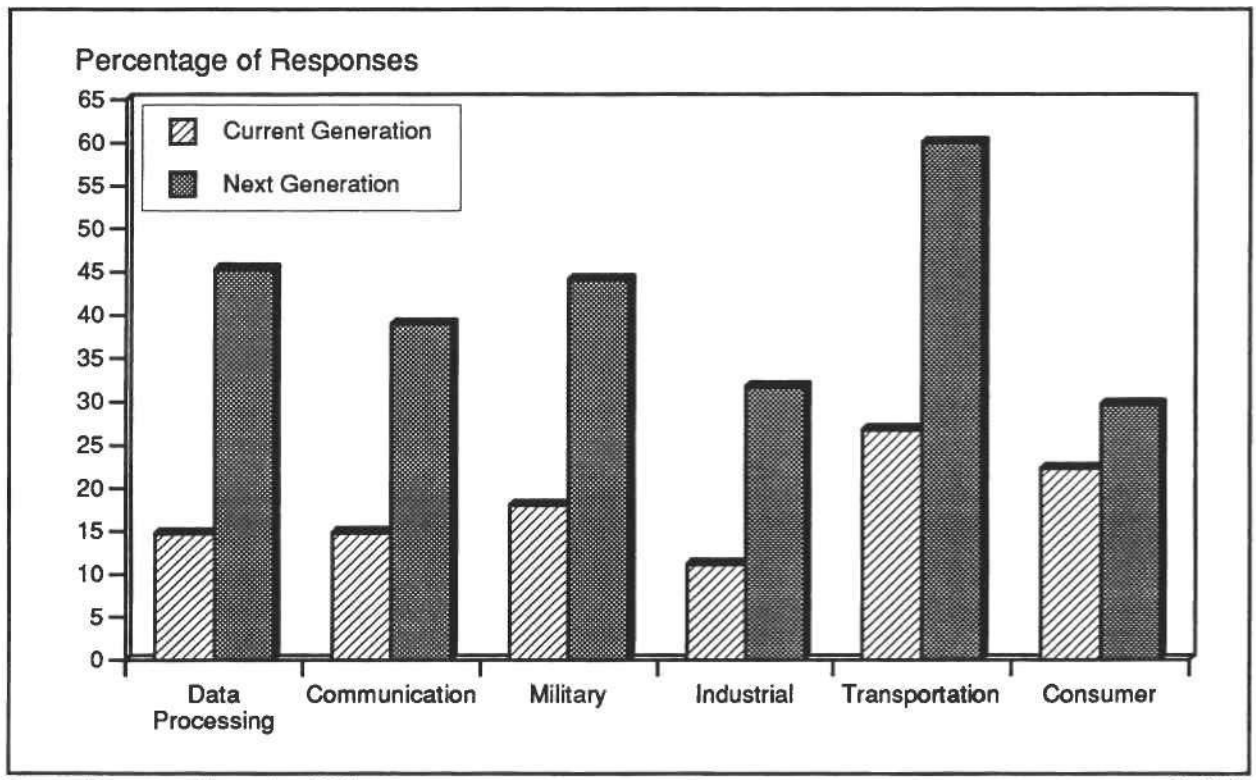
Further examination of the types of computers that will be using GaAs ASICs showed that CISC computers came up surprisingly high in the results for North America (see Figure 5-7). As expected, mainframe and supercomputers are expected to be the largest users of GaAs ASICs in the next-generation system designs.

Figure 5-1
ASIC Users, by Process Technology



Source: Dataquest (November 1992)

Figure 5-2
BiCMOS ASIC Users, by Application: North America



Source: Dataquest (November 1992)

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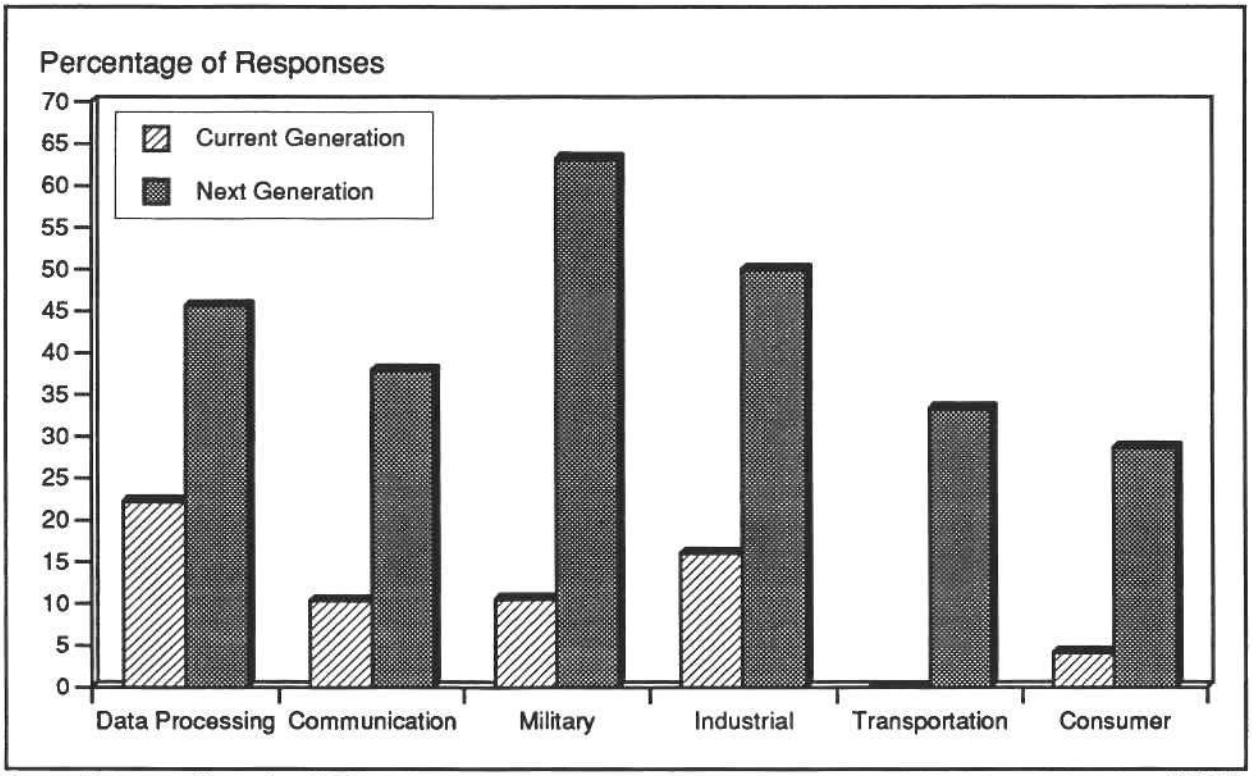
Figure 5-3
BiCMOS ASIC Users, by Application: Japan



Source: Dataquest (November 1992)

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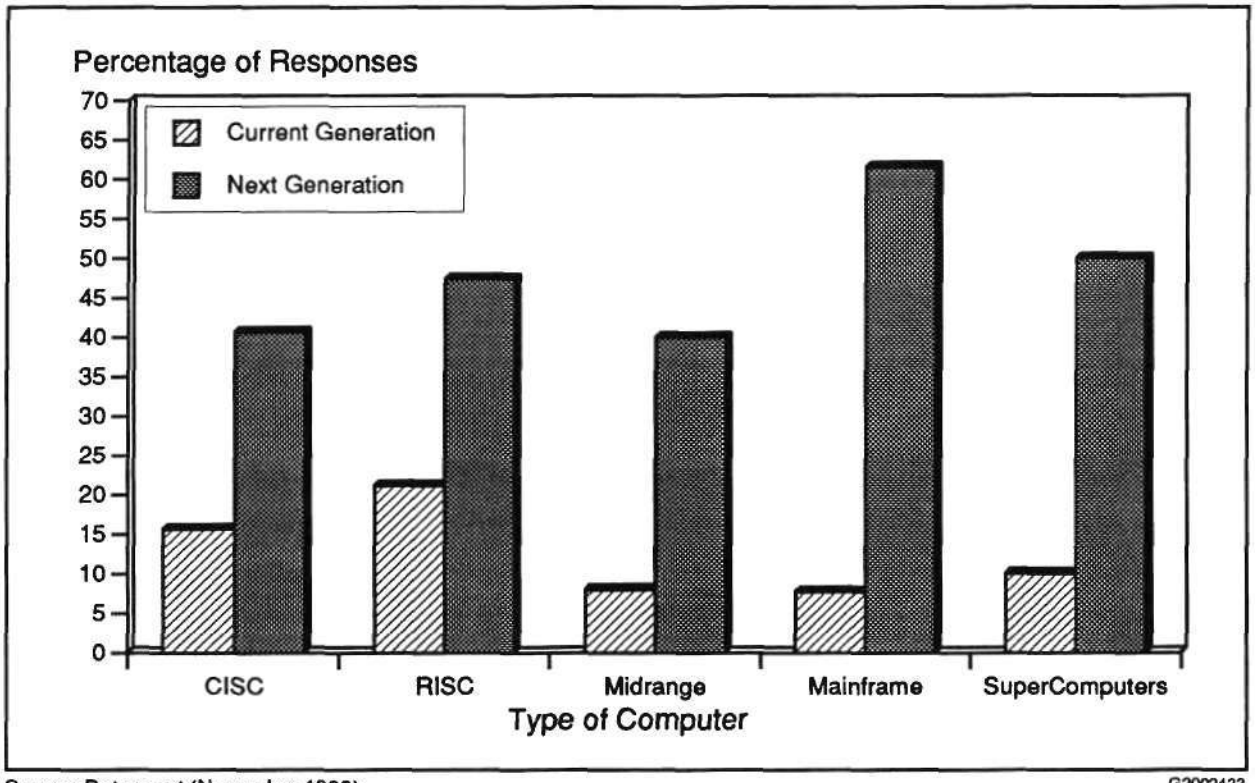
Figure 5-4
North American BiCMOS ASIC Users: Computers



Source: Dataquest (November 1992)

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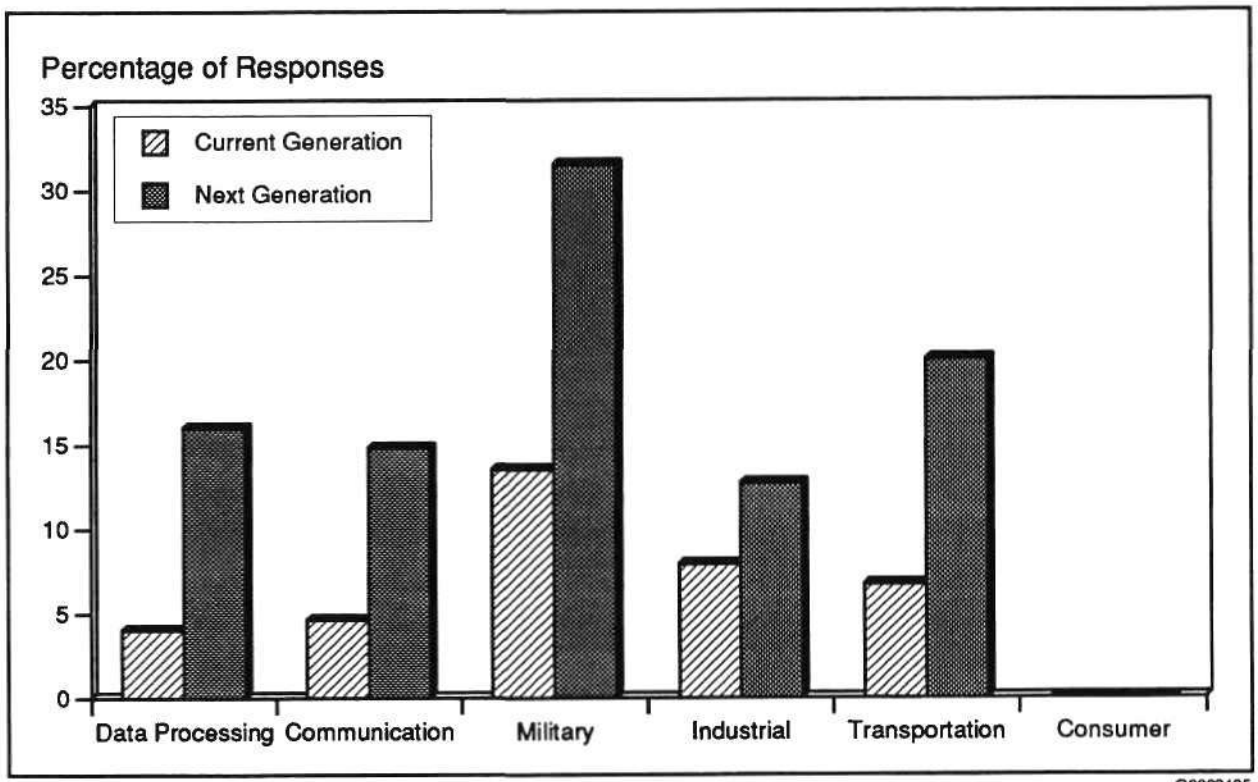
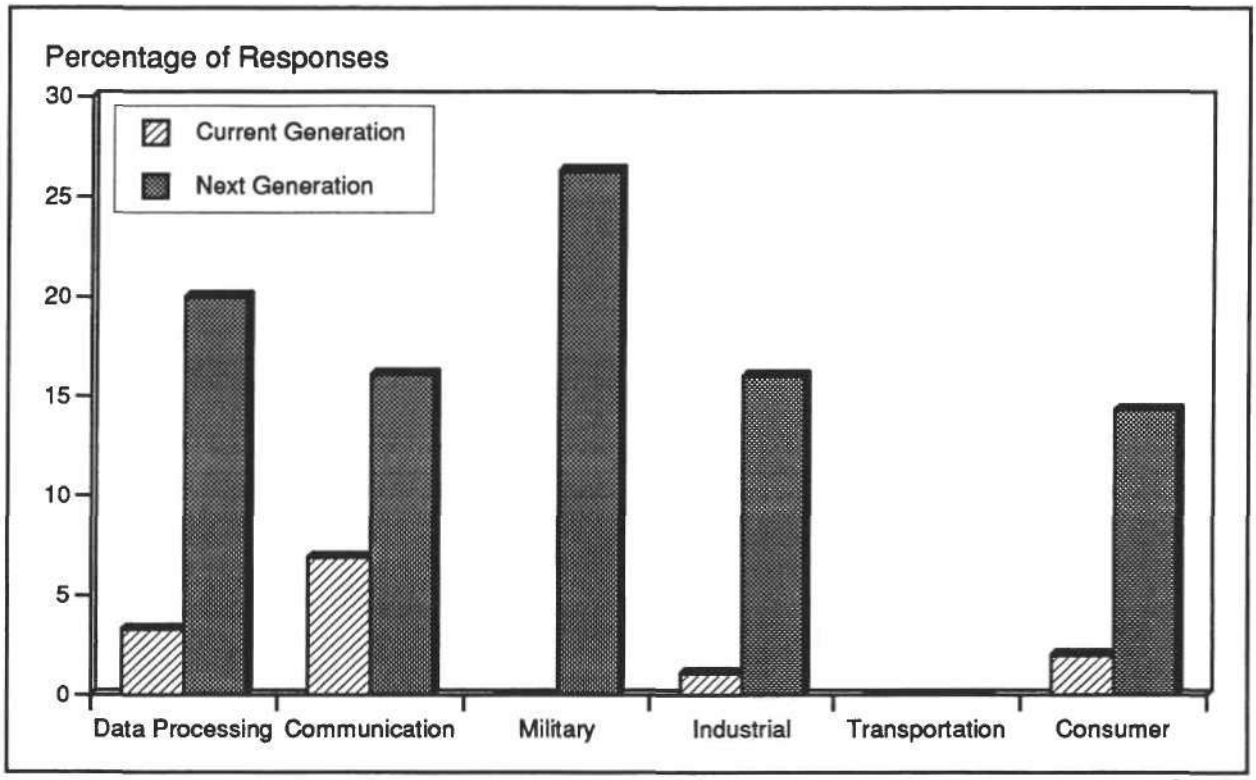
Figure 5-5
GaAs ASIC Users, by Application: North America



Source: Dataquest (November 1992)

Figure 5-6
GaAs ASIC Users, by Application: Japan



Source: Dataquest (November 1992)

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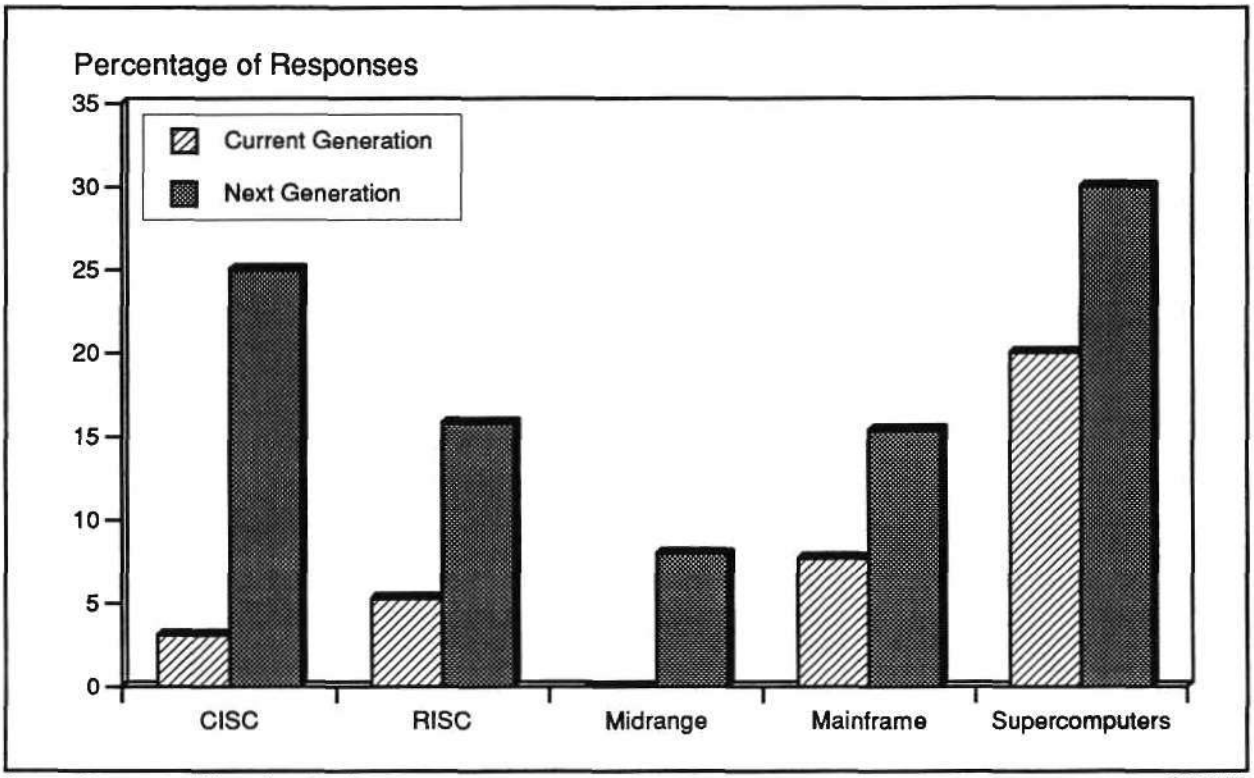
Figure 5-7
North American GaAs ASIC Users: Computers



Source: Dataquest (November 1992)

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Chapter 6
Dataquest Conclusions

The two most surprising conclusions that can be made from the survey results are as follows:

- The average gate count of ASIC devices used in Japan for next-generation system design is expected to be higher than in North America.
- System designers perceive great value in BiCMOS ASICs for their next-generation system designs.

According to Dataquest's user survey results, the average gate count of ASICs used in Japan's current-generation system design was 18,000, and was 20,000 in North America. These gate counts are consistent with the average gate counts compiled from ASIC suppliers. The big surprise came when comparing the results of average gate counts for next-generation system designs. System designers in Japan said that the average ASIC gate count for next-generation system design will be nearly 57,000 gates, compared with 54,000 in North America. Although Dataquest believes that the averages for both countries will probably be closer to 50,000 gates, this is quite a change from the gate counts in current-generation system design. With the aid of third-party design tools from companies such as Cadence and Mentor, system designers in Japan are able to design-in complexity levels much higher than when they used proprietary design tools based on mainframe computers. Potential applications slated for high-density ASICs in Japan include RISC-based computers, industrial control, medical equipment, telecommunication and data communication, and consumer electronics. Dataquest believes that HDTV will play a major role in the development of high-density ASICs in Japan.

The second most surprising result from the survey results was the high usage of BiCMOS ASICs planned for next-generation system design. About 10 percent of the system designers in North America and Japan said they were using at least one BiCMOS ASIC in their current-generation system design. As for next-generation system design, 36 percent of designers in North America and 31 percent of system designers in Japan said they would be using BiCMOS ASICs. Although Dataquest believes that these percentages are high, ASIC users clearly see a perceived value in BiCMOS ASICs for their next-generation system design. RISC computers, telecommunication, data communication, mainframe computers, mass storage, printers/plotters, and test/instrumentation equipment are potential applications for which system designers plan to use BiCMOS ASICs. Examination of

the applications slated for BiCMOS ASICs suggests that designers must believe that BiCMOS ASICs offer a major drive or speed advantage over CMOS ASICs. Although today's BiCMOS ASICs may have some slight advantages, compared with CMOS ASICs, it is not clear how much of an advantage BiCMOS ASICs will have over CMOS ASICs when process geometries are below 0.5 microns and 3V power supplies are used. A larger question that remains is how much users are willing to pay for BiCMOS ASICs, compared with CMOS ASICs. Dataquest believes that CMOS will remain the mainstream ASIC technology for the foreseeable future and that BiCMOS ASICs will be more of a niche product.

Supplier Recommendations

ASIC users want and need high-density ASICs for their next-generation system design. This presents great opportunity for ASIC suppliers.

The first step that ASIC suppliers must take to capitalize on this opportunity is to target specific applications in specific regions. Survey results showed that the wants and needs of system designers vary widely on an application and a regional basis. Suppliers should analyze the data presented in this report to determine the requirements of the different target markets.

Next, ASIC suppliers must develop a plan for how they will differentiate their products from their competitors. This is easier said than done. Most ASIC suppliers offer competitive process technology, solid design tools, and ASIC products with an excess of 100,000 gates. Cell libraries and system knowledge are important ways of differentiating ASIC suppliers. ASIC users will seek the suppliers that understand their system design and have invested in library development targeted for their specific applications. Although there are other ways to differentiate ASIC products such as by offering unique packaging or extensive test capabilities, system knowledge and dedicated cell libraries are of primary importance to ASIC users.

Alliances and partnerships also are critical to the success of future ASIC suppliers. ASIC suppliers can no longer develop all the areas needed to be competitive in the ASIC market. For example, many suppliers will need to form alliances to enhance their test capabilities or broaden their packaging offering. A close partnership with ASIC users or system designers is also crucial. Library development costs can be substantially reduced if suppliers and users work together to jointly develop cells that can be reused in future ASIC designs. No supplier will be able to go it alone in the future.

User Recommendations

Dataquest believes that users should take a long, hard look at the perceived advantages of BiCMOS ASICs, compared with CMOS ASICs. There are many ways to solve a problem. Clever system designers are finding new ways to design using CMOS that elevate the need for

BiCMOS in future system designs. There will always be a pricing premium associated with BiCMOS ASICs, and system designers need to contrast the advantages they receive with the premium they pay.

Dataquest also advises ASIC users to compare the cost of using multichip modules versus using extremely high-gate-count ASICs. In many cases, it will be less expensive and quicker to market to use four 100,000-gate devices in a multichip module, versus one 400,000-gate device, for example. The golden rule should be kept in mind: It is far better to get to the market quicker with a low-cost product than to get to the market late with a technologically superior product.

Appendix A
Dataquest Electronic Design Survey

1. Please check the organization for which you will be responding in answering this survey (check only one):

   Company ❑ Project Team ❑

2. What is the average size of your ASIC designs (in gates)?

	Current Design* (check one)	Next Generation Design (check one)
4,999 or fewer	❑	❑
5,000—9,999	❑	❑
10,000—19,999	❑	❑
20,000—49,999	❑	❑
50,000—74,999	❑	❑
75,000—99,999	❑	❑
100,000 and greater	❑	❑
Don't know	❑	❑

**Current design means the design that you are currently working on. This usage is consistent throughout this survey.*

3. Please estimate the average annual unit volume production per board design:_____

4. What is the average number of signal layers per board design?

   Current Design _____ Next Generation Design _____

5. What is the size of your typical board design?

	Current Design (Check one)	Next Generation Design (Check one)
Less than 10 square inches (25.4 cm^2)	❑	❑
10-19 square inches (25.4-50.7 cm^2)	❑	❑
20-49 square inches (50.8-126.9 cm^2)	❑	❑
50-99 square inches (127-253.9 cm^2)	❑	❑
100-249 square inches (254-634.9 cm^2)	❑	❑
250-499 square inches (635-1,269.9 cm^2)	❑	❑
500 square inches or greater (1,270 cm^2)	❑	❑

6. How many different boards does your company and project team design annually?

   Company _____ Project Team _____

7. Please estimate the average number of IC packages per typical board design:

   Current Design _____ Next Generation Design _____

8. What is the highest frequency used in your design?

   Digital Clock Frequency _____MHz Analog Signal Frequency _____MHz

9. What percentage of your design's functionality is reused circuitry from a previous design? _____%

10. Are you using, or do you plan to use, EDIF in your design process for the following (check all that apply)?

	Current Design	Next Generation Design
Design Data Translation	❑	❑
Library Data Translation	❑	❑
Other (please specify)	_____	_____

11. On average, how many of the following devices do/will you have on each board design?

	Current Design	Next Generation Design
Microprocessors	____	____
Microcontrollers	____	____
DSPs	____	____
PALs, PLAs	____	____
Complex PLDs (e.g., Altera's MAX, Plus Logic)	____	____
Field Programmable Gate Arrays (e.g., Xilinx, Actel ICs)	____	____
Gate Arrays (Mask Programmable)	____	____
Cell-Based ICs	____	____
Handcrafted, Full-Custom ICs	____	____
Analog ASICs	____	____
Mixed Signal ASICs	____	____

12. Please check the process technologies of the standard ICs and ASICs used in your board design (check all that apply):

	Standard ICs		ASICs	
	Current Design	Next Generation Design	Current Design	Next Generation Design
NMOS	❑	❑	❑	❑
CMOS	❑	❑	❑	❑
BiCMOS	❑	❑	❑	❑
TTL	❑	❑	❑	❑
ECL	❑	❑	❑	❑
GaAs	❑	❑	❑	❑
Don't Know	❑	❑	❑	❑
Other (please specify)	❑	❑	❑	❑
	_____ (Specify)		_____ (Specify)	

13. a) For a typical electronic system design project, how many total engineers are assigned? _____

b) Of the total engineers, which of the following categories apply (check as many as applicable)?

System Architects ❑	PCB Layout Specialists ❑
Digital Designers ❑	IC Layout Specialists ❑
Analog Designers ❑	Software Development Engineers ❑
Mixed-Signal Designers ❑	Packaging Engineers ❑
Simulation and Verification Support Engineers ❑	Reliability Engineers ❑
Test Engineers ❑	Manufacturing Engineers ❑

Other (please specify)_____

14. Please estimate the number of licenses/copies of the following EDA tools that you have, and how many you need:

	Currently Have	Currently Need
Schematic Entry	____	____
Logic Synthesis	____	____
Logic Simulation	____	____
Timing Verification	____	____
Analog Simulation	____	____
Automatic Test Vector Generation	____	____
PCB Layout	____	____
IC Layout	____	____
Thermal Analysis	____	____
Data Management	____	____

15. Please check the three most important factors to your product's future ability to achieve market success (check only three):

- Increasing Functionality ❑
- Increasing System Speed ❑
- Increasing Quality/Reliability ❑
- Increasing Ease of Use ❑
- Reducing Time-to-Market ❑
- Reducing Form Factor ❑
- Reducing Cost ❑
- Reducing Power Dissipation ❑
- Reducing EMI ❑
- Other (please specify) _____

16. Please estimate the percentage investment (i.e., resources) in developing the hardware portion of your system versus the software portion:

	Current Design	Next Generation Design
Hardware Portion	____	____
Software Portion	____	____
	Total = 100%	Total = 100%

17. If you use or plan to use the following devices, what do you plan to use them for (check all that apply)?

	Prototyping	Production	ASIC Emulation
PALs, PLAs	❑	❑	❑
Complex PLDs/FPGAs	❑	❑	❑

18. For a typical board design, what percentage of its functionality is digital versus analog?

	Current Design	Next Generation Design
Digital	____	____
Analog	____	____
	Total = 100%	Total = 100%

19. Please estimate the percentage of the packages on your current board design according to the following categories:

Surface Mount _____

Through-Hole Packages _____

Total = 100%

20. Which of the following package technologies do you currently use or are you planning to use (check all that apply)?

	Current Design	Next Generation Design
Chip on Board (CoB)	❑	❑
Tape Automated Bonding (TAB)	❑	❑
Multi Chip Modules (MCM)	❑	❑
Flip Chip	❑	❑
Hybrid	❑	❑

21. For your board designs, how long (in months) would you estimate the design cycle to be?

	Board Designs	
	Current Design	Next Generation Design
From concept to prototype	____	____
From prototype to volume production	____	____

22. For your ASIC designs, how long (in months) would you estimate the design cycle to be?

	ASIC Designs	
	Current Design	Next Generation Design
From concept to prototype	____	____
From prototype to volume production	____	____

23. What percentage of fault coverage is acceptable in your ASIC designs (check only one)?

Less than 50%	❑
50-79%	❑
80-85%	❑
86-90%	❑
91-95%	❑
96-99%	❑
100%	❑

24. In order for your ASIC design to achieve the highest possible testability level acceptable, what percentage of increased component cost and reduced speed are you willing to accept?

Penalty	0	1-5%	6-10%	11-15%	16-20%	>20%
Component cost (Check one)	❑	❑	❑	❑	❑	❑
Reduced speed (Check one)	❑	❑	❑	❑	❑	❑

25. Please indicate whether any of your designs implement the following test capabilities (check all that apply):

	Current Design	Next Generation Design
Full SCAN (ASIC)	❑	❑
Partial SCAN (ASIC)	❑	❑
BIST (ASIC)	❑	❑
BIST (board)	❑	❑
JTAG (board)	❑	❑
Other (please specify)	_____	_____

26. a) During the design cycle, which of the following design problems consumes more time?

	ASIC Design (Check One)	Board Design (Check One)
Timing violations	❑	❑
Functional violations	❑	❑

b) After the prototype is received, which of the following design problems consumes more time?

	ASIC Design (Check One)	Board Design (Check One)
Timing violations	❑	❑
Functional violations	❑	❑

27. Please indicate the percentage of system design cycle time spent on the following tasks:

	% of System Design Cycle Time Spent on Task
Definition of design specification and system partitioning	_____
Logic/circuit design and logic verification	_____
Design for testability and test vector development	_____
System integration and verification	_____
Prototype debug	_____
Other (please specify) _____	_____
	Total = 100%

28. During the design cycle, what methods do you use to verify your system designs (check all that apply)?

	Current Design	Next Generation Design
Full system level simulation	❑	❑
Simulate critical parts only	❑	❑
Breadboard (or directly to prototype)	❑	❑

29. a) What is your EDA budget (in dollars if possible)?

1991	_____
1992 (estimate)	_____

b) What percentage of your 1991 EDA budget is spent on purchasing tools from outside vendors versus *developing* tools internally?

Outside Vendors	_____%
Internal Development	_____%
	Total = 100%

30. On a per-seat basis, how much would you be willing to spend for a framework license that supports the following (check only one per column)?

	Tool Integration & Data Translation	Data & Library Management	User Interface Customization
Less than $2,500	❑	❑	❑
$2,500-$4,999	❑	❑	❑
$5,000-$9,999	❑	❑	❑
$10,000-$14,999	❑	❑	❑
$15,000 or more	❑	❑	❑

31. From the following list, please check all the vendors whose platforms you currently use or plan to use for EDA:

	Current	Future
Apple Computer	❑	❑
DEC	❑	❑
Fujitsu	❑	❑
HP/Apollo	❑	❑
Hitachi	❑	❑
IBM	❑	❑
MIPS	❑	❑
NEC	❑	❑
Silicon Graphics	❑	❑
Sony	❑	❑
Sun Microsystems	❑	❑
IBM Clone Vendor	❑	❑
SPARC Clone Vendor	❑	❑
Other (please specify)_____		

32. Do you plan to use X terminals that do not provide any local processing power in your EDA environment?

Yes ❑
No ❑

33. Please rate the importance of each of the following design automation tools (rate on a scale of 1 to 5, with 1 = Least Important and 5 = Most Important):

	Least Important				Most Important
DIGITAL DESIGN	1	2	3	4	5
Design Entry:					
Schematic entry (graphical)	❑	❑	❑	❑	❑
High level entry (e.g., HDL)	❑	❑	❑	❑	❑
Model libraries	❑	❑	❑	❑	❑
Design Verification:					
Simulation	❑	❑	❑	❑	❑
Static timing verification	❑	❑	❑	❑	❑
Signal noise analysis	❑	❑	❑	❑	❑
Transmission line simulation	❑	❑	❑	❑	❑
Crosstalk analysis	❑	❑	❑	❑	❑
Power consumption analysis	❑	❑	❑	❑	❑
EMI simulation	❑	❑	❑	❑	❑
Simulation acceleration (e.g., Zycad, IKOS)	❑	❑	❑	❑	❑
Hardware modeling (e.g., Logic Modeling Systems)	❑	❑	❑	❑	❑
Rapid prototyping (e.g., ASIC emulators)	❑	❑	❑	❑	❑
Logic Synthesis	❑	❑	❑	❑	❑
Test Automation:					
Automatic test vector generation	❑	❑	❑	❑	❑
Design for testability/test logic synthesis	❑	❑	❑	❑	❑
Fault simulation/grading	❑	❑	❑	❑	❑
Documentation	❑	❑	❑	❑	❑
Data management	❑	❑	❑	❑	❑
OTHER					
IC Layout	❑	❑	❑	❑	❑
PCB Layout	❑	❑	❑	❑	❑
Thermal Analysis	❑	❑	❑	❑	❑
Electromechanical Design Automation Tools	❑	❑	❑	❑	❑
Manufacturing Interfaces	❑	❑	❑	❑	❑

34. Which of the following design and manufacturing tasks do you currently perform, or will you perform, internally within your company (check all that apply):

	Current Design	Next Generation Design
IC floor planning	❑	❑
IC manual place and route	❑	❑
IC automatic place and route	❑	❑
IC design rule checking	❑	❑
IC electrical rule checking	❑	❑
IC logic-to-layout checking	❑	❑
PCB bareboard fabrication	❑	❑
PCB assembly	❑	❑

35. Please check which of the following hardware description languages (HDLs) you use or plan to use (check all that apply):

	Current Design	Next Generation Design
VHDL	❑	❑
Verilog HDL	❑	❑
UDL/I	❑	❑
Proprietary	❑	❑
Other (please specify)_____	❑	❑
No use of HDL	❑	❑

36. What is the total employee count of your company?_____

37. What is your title? _____

38. Which one of the following best describes your primary line of business in each category?

Company (Check only one)	Project Team (Check all that apply)	
❑	❑	Aerospace/military electronics
❑	❑	Automotive
		Communications equipment
❑	❑	Telecommunications
❑	❑	Data Communications
		Computer Systems (Desktop computers & servers):
❑	❑	RISC
❑	❑	CISC
		Host-based systems
❑	❑	Midrange computers
❑	❑	Supercomputers
❑	❑	Mainframes
❑	❑	Consumer electronics
❑	❑	Government
❑	❑	Industrial control
❑	❑	Medical equipment
❑	❑	Semiconductors
		Peripherals:
❑	❑	Printers/plotters
❑	❑	Mass storage
❑	❑	Test/instrumentation equipment
❑	❑	Other (please specify)

_____

Name/Title: _____ Telephone:_____

Company: _____

Address: _____

_____

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