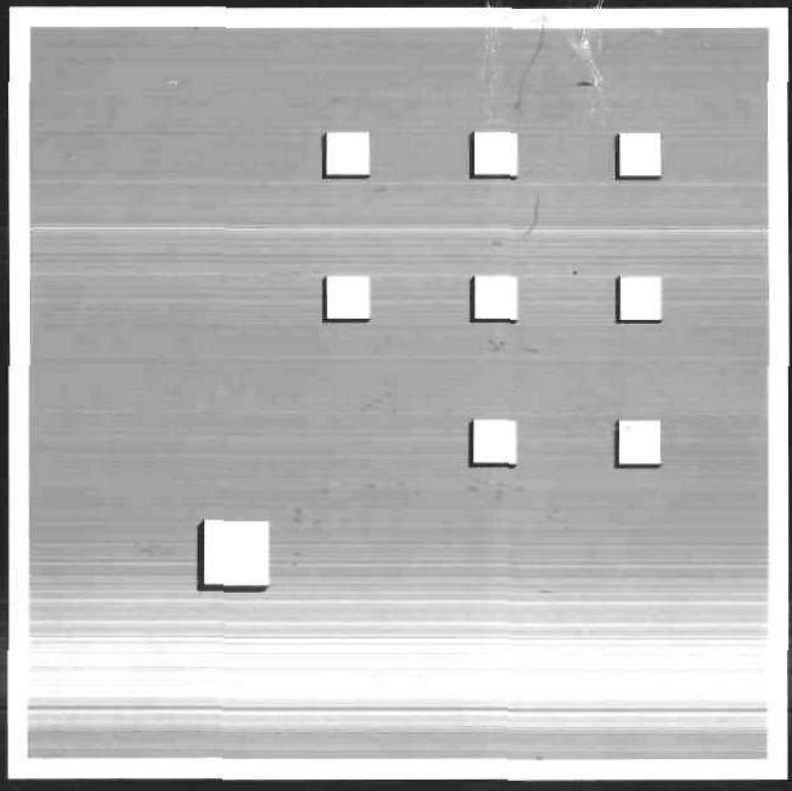
IC Outlook '87



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IC Outlook '87

Paris, France — September 15
Milan, Italy — September 16
Munich, West Germany — September 17
Frankfurt, West Germany — September 18
Stockholm, Sweden — September 19
London, England — September 22
Edinburgh, Scotland — September 23

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Presented
By

European Semiconductor Industry Service
Semiconductor User Information Service

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IC Outlook '87

Paris, France — September 15
Milan, Italy — September 16
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8:30 a.m. Registration

9:00 a.m. Introduction

9:15 a.m. Worldwide Business and Technology Trends
- World market trends and business climate
- 1986–1987 outlook
- Price and availability trends
- Status of start-ups
- Current and emerging technology trends

9:45 a.m. European Industry Update
- Economic analysis
- Regional market update and outlook
- Integrated circuit industry in Europe
- Market share analysis

10:30 a.m. Break

11:00 a.m. ASICs and Logic
- Standard logic
  - Market status and trends
  - CMOS or bipolar?
  - Impact of ASICs
  - New family review
- Application-specific ICs
  - Market growth continuing
  - Price trends
  - Selecting the right product and source
  - New opportunities

Noon Lunch (provided with the seminar)

1:30 p.m. Memory and Microprocessor Update
- Memory review
  - Market overview
  - Impact of U.S.-Japan trade issues
  - DRAM trends
  - SRAM trends
  - Nonvolatile memories
- Microprocessors
  - Market update and outlook
  - The emerging 32-bit market
  - OTPs and microcontroller overview
  - Market share analysis
  - Digital signal processing

2:30 p.m. Packaging Review
- Industry overview
  - Trends
  - Technology
  - Forecast
- Surface mount
  - Where is it going?
  - Impact on board densities
  - End-user production issues

3:00 p.m. Break

3:30 p.m. Vendor-Customer Relationships
- Strategic partnering
  - Objectives
  - Obstacles
  - Vendor motivation

4:15 p.m. Wrap-up

4:30 p.m. Meeting Adjourns

NOTE: Where appropriate, we will present our current market forecast, price and lead time trends, capacity versus demand, supplier review, and sourcing considerations.

Speaker Biographies

James W.M. Beveridge

Mr. Beveridge is an Associate Director of Dataquest's European Semiconductor Division, based in London. He has more than nine years of experience in the electronics industry.

Before joining Dataquest, he was European Product Marketing Manager for CMOS Logic and Telecommunications Circuits at Motorola Semiconductors Ltd. His experience prior to this was gained in a range of marketing and engineering positions for the Motorola microcomponent, memory, and custom IC product lines. Mr. Beveridge spent two years working at Motorola GmbH Munich, where he had responsibility for CMOS marketing in Central Europe.

Mr. Beveridge received a B.Sc. (Eng.) degree in Electronics and a specialization in Business Studies from the University of Glasgow, United Kingdom.

Mark A. Giudici

Mr. Giudici is an Industry Analyst for Dataquest's Semiconductor User Information Service.
He is responsible for worldwide research of semiconductor costs, pricing, and industry trends.

Prior to joining Dataquest, Mr. Giudici spent eight years in the computer and semiconductor industries, where he held a variety of financial and marketing positions. Most recently, Mr. Giudici was a Product Marketing Engineer with Gould-American Microsystems Inc., where he was responsible for cost modeling and marketing semicustom and custom semiconductor components.

Mr. Giudici received a B.S. degree in Business Administration from California State University at Chico and an M.B.A. degree in Business Management from the University of Oregon.

Peter Savage

Mr. Savage is an Associate Director of Dataquest's European Semiconductor Division, based in London. He has more than 19 years of experience in the electronics industry, the last 11 of which were spent in the semiconductor sector.

Prior to joining Dataquest, he was the North European Marketing Manager for the LSI Products Division of TRW. Previously, he was with SGS (U.K.) Ltd., where he held a variety of marketing and engineering positions including Marketing and Market Development Manager and overall Product Marketing Manager.

Mr. Savage studied Electronic and Radio Engineering at two Polytechnics of London University and, with postgraduate studies, received the equivalent of an M.S.E.E. degree.

IC Outlook '87

- Introduction
- Worldwide Business and Technology Trends
- European Industry Update
- ASICs and Logic
- Memory and Microprocessor Update
- Packaging Review
- Vendor-Customer Relationships

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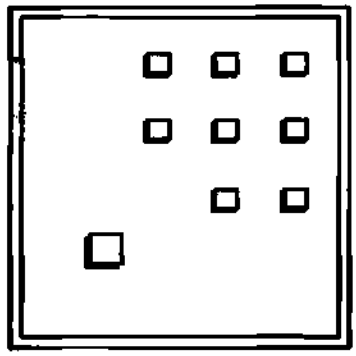

Dataquest
IC Outlook '87

September 15–23, 1986

INTRODUCTION

PETER SAVAGE
Dataquest UK Limited

Good morning ladies and gentlemen. My name is Peter Savage, and I'd like to take this opportunity to welcome you to Dataquest's third annual European integrated circuit seminar, IC Outlook '87. Before we start the formal program, I'd like to take a few minutes to tell you a little about Dataquest.

Dataquest, since May 1984, has been part of the Dun & Bradstreet corporation, the world's largest information company, with over 58,000 employees worldwide. We are very proud of our association with such an outstanding organization. Listed here are some of our corporate affiliates--altogether it adds up to an incredibly extensive information resource.

Dataquest was established in 1971 and has achieved, since that time, a 20 per cent per annum growth both in size and revenue. We currently serve over 2,200 clients and our research activities presently cover 27 separate strategic and tactical industry services spanning a wide spectrum of high technology business areas. Through its wide coverage of high-technology industries, ranging from semiconductors and CAD/CAM to peripheral systems, we believe Dataquest is uniquely qualified to analyze the impact of industry developments across this wide spectrum of markets. All of the analysts have access to, and interaction with, these 27 separate services which are, themselves, tied together via a worldwide integrated data base. We are an international operation with 11 offices, and representatives on all four continents.

Within Dataquest's semiconductor activities there are now six services relating specifically to the semiconductor industry.

The original Semiconductor Industry Service (SIS) offers a global and U.S. perspective; the European Semiconductor Industry Service (ESIS), which is headquartered in London, focuses on in-depth analysis of the European marketplace; the Japanese Semiconductor Industry Service (JSIS) has its major research capability in Tokyo; the Semiconductor User Industry Service (SUIS) gives subscribers access to data on pricing, lead times, product and cost analyses, product quality and reliability, and vendor-related information; the Semiconductor Equipment and Materials Service (SEMS) is designed to fulfill the needs of vendors to the semiconductor manufacturing community; and finally the latest addition, Semiconductor Application Markets (SAM), tracks the equipment end-use consumption of semiconductor products by the industry segments of Transportation, Consumer, Data Processing, Military, Communications, and Industrial.

Each Dataquest service consists of four elements: the industry data bases, newsletters, conferences, and direct access to analysts. The data base, which is supplied in loose-leaf binders, gives basic industry statistics and information. It is updated regularly and can answer many of your questions.

Each group publishes several newsletters each month. These newsletters help you keep abreast of developments in the industry and offer timely information on hot topics.

The annual conferences offered by each service give attendees an opportunity to hear experts from their industry speak in a formal program. An equally important function of each conference is the chance to meet your peers in the industry and discuss shared concerns in an informal setting.

We have a wealth of unpublished information and individual expertise in our research offices. Direct access to analysts within the group enables you to obtain more detailed information on topics discussed in the data bases and newsletters, or to ask questions on topics of immediate interest.

In addition to these specific services, Dataquest publishes a series of Focus Reports providing in-depth analysis on topical aspects of the industry. Some recent and upcoming publications deal with the Korean semiconductor industry, the gallium arsenide market, and the digital signal processing market.

There are specific newsletters published regularly reporting on the marketplace in the Far East entitled I.C. Asia, for the United States entitled I.C. U.S.A., and for Europe there is the European Monthly Report. Dataquest On-line Service has recently been launched, allowing fast, easy, and timely access to the data bases of the respective services.

Specifically in this area, the Semiconductor Industry Association through its World Trade Statistics arm has given Dataquest the exclusive marketing rights for its monthly flash reports containing book-to-bill ratio data and the blue book of trade statistics. This particular service is also available to non-Dataquest clients.

In today's seminar, we will be analyzing the current market for integrated circuits, giving an overview of product and technology trends, and discussing the many factors affecting semiconductor selection and procurement now and in the future. We welcome any questions throughout the presentation.

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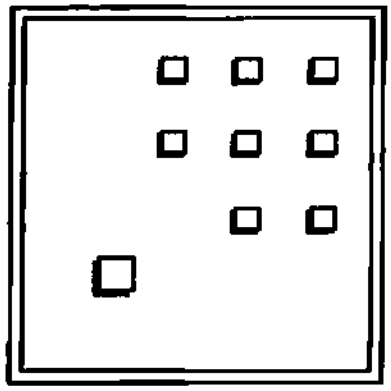

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IC Outlook '87

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WORLDWIDE BUSINESS AND TECHNOLOGY TRENDS

MARK A. GIUDICI
Dataquest Incorporated

(Slide 1)

Good morning. Clearly, the electronics industry is in a state of transition. Now that we have hopefully left the worst recession that the industry has ever seen, many aspects are different. Business conditions, market conditions, and technology itself are all changing. And very rapidly at that.

(Slide 2)

Competition has increased dramatically on a worldwide basis. This is not only true for semiconductor suppliers, but also for equipment manufacturers.

(Slide 3)

Additionally, the current economic situation in the United States and in most other countries has a pronounced impact upon the electronics industry. An example is the current tax reform in the United States, which is affecting capital purchases.

(Slide 4)

Today, more than ever, technology moves at a pace that is unyielding. This accelerating change forces users to stay abreast of the latest developments or face being uncompetitive. Shorter product life cycles, a variety of new design solutions, and increased competition all complicate product definition and affect an end product's viability, with an immediate effect on profit margins.

(Slide 5)

The semiconductor business is certainly known for its volatility, making it very cyclical in nature. A short time ago it was thought that the industry's size would not permit these types of swings. Yet we have just experienced the worst recession in its history.

(Slide 6)

Designing the right type of product and manufacturing it effectively has always been important to being competitive. And as the high-growth electronics segments become even more competitive, achieving real success will come from the application market focus. This is certainly a long-term goal.

(Slide 7)

A "blanket" marketing technique will not suffice in the future. Semiconductor companies will have to meld with the needs of the smaller customers. Obviously this requires an investment. But being successful at serving the needs of those niche market customers means a somewhat tailored approach in helping to service the high-growth segment players.

(Slide 8)

Markets tend to evolve in all product areas. We have identified three stages that we will call class, mass, and mass-class. This evolution in semiconductors has parallels in other industries such as automobiles.

The class stage defines a market for expensive products supplied by potentially many vendors--probably in medium to low volume and very targeted.

In the mass market, high-volume, low-cost products from several suppliers fulfill many needs, as in standard logic devices for instance.

The mass-class market defines those suppliers that are targeting specific product areas and customers' requirements, but in some volume such as ASICs, DSP, and similar devices.

(Slide 9)

The mass-class market also means that a semiconductor supplier understands the needs of the very end customer, perhaps an average consumer. This person is the IC customer's customer, who may not be concerned about the technology of the end product.

(Slide 10)

I believe that everybody will agree that the current electronics market has an impact on purchasing and operations as well as on marketing in an organization. Today's buying decisions are clearly not simple, and they likely will not become simpler in the future.

(Slide 11)

Product marketing has always been an important part of a competitive strategy. However, operational issues, including procurement, have become equally as important in a company's strategy to stay at the forefront of its marketplace. Included in that strategy is the effect that quality has on everything performed, in order to remain highly competitive. This should be the highest consideration.

(Slide 12)

The buyer's view has become an increasingly important aspect of daily operations for the industry. As we move further into a changing industry, more companies are becoming aware of the need to emphasize these items or concepts. I will highlight a couple of these points.

(Slide 13)

Within the last five years, the issue of pricing has risen to a global level. Monitoring worldwide pricing has allowed equipment manufacturers to formulate programs to deal with the regional differences. This suggests different manufacturing programs.

(Slide 14)

The Far East leads the United States in lower materials cost. This 20 to 40 percent difference indicates the importance of buying materials effectively, as labor costs are a lesser portion of manufacturing from increased efficiency.

(Slide 15)

The worldwide semiconductor consumption forecast indicates reasonably strong growth through 1987. We are forecasting a return of growth to about 23 percent from being negative in 1985. The same is true in 1987, when we expect consumption to be about 27 percent above 1986. Much of this growth comes from yen-to-dollar difference, the dumping situation, and simply gradual overall growth.

From a regional point of view, the United States, Japan, and Europe should all return at about the same rate. The yen-to-dollar difference accounts for some inflation in growth over last year. When that inflation is removed, these three regions are close at about 8 to 10 percent. The exception to this is ROW, which indicates a strong market growth but from a relatively small consumption base.

(Slide 16)

A worldwide product view shows that ICs alone track with the expected growth of overall semiconductors. Within this is the clear impact that MOS technology is having on the industry. It should average 25 percent for this year and be closer to 45 percent in 1987. The biggest portion of MOS for 1986 is logic, driven primarily by ASIC consumption. In 1987, we expect memory products to be the clear leader in dollar growth. The return of higher, more stabilized prices certainly contributes to most of that growth.

(Slide 17)

This slide shows our average selling price estimates for a sample of representative devices. Logic should remain fairly constant over time as demand picks up. Pricing could escalate dramatically if a very abrupt demand occurred that resulted in immediate shortages. This could occur if an end product driver would begin to be produced in volume, such as the personal computer boom of a couple of years ago.

Memory products, specifically dynamic RAMs and EPROMs are experiencing the direct results of the semiconductor trade agreement. As a result of the last-minute negotiations, the 1986 ASPs should be affected by a factor of about two times, resulting in an approximate $5 ASP for 256K dynamic RAMS.

(Slide 18)

Microprocessor prices should continue to decline along the experience curve. This is especially true for the high-end devices including 32-bit parts. Application-specific ICs such as gate arrays should remain fairly stable over time, partly due to the monitoring of ASPs from Japan.

(Slide 19)

The electronic equipment outlook is important in understanding where the growth is and why. The computer industry in the United States, for example, is expected to grow at only about one-half of its normal rate. But other segments, such as the communications, industrial, and transportation sectors, could display higher-than-normal growth. The next slide will detail seven product areas in North America that are expected to reach about $1 billion by 1990 and have higher-than-normal growth.

(Slide 20)

These seven product areas have been identified as being potential high-growth areas and therefore substantial semiconductor consumption possibilities. These segments have annual growth ranging from 13 percent to more than 30 percent and higher-than-average I/O ratios.

(Slide 21)

From this list it becomes obvious that consumer products are still the leading end product for semiconductors in Japan. This permits the Japanese to build ICs in mass volume and drive the costs down quickly.

(Slide 22)

This slide shows that the Japanese market is moving quickly toward leading-edge products for personal and office use. Telecommunications and office automation are becoming larger portions of the end market in Japan. This will continue as more efficiency and productivity are stressed in the job environment.

(Slide 23)

A quick look at the status of start-ups indicates that even while the recession continued, several new ventures were created. We believe that at least 12 new companies were started, and possibly more who will announce themselves in the near future. There continues to be a proliferation in Santa Clara Valley due to the presence of venture capital. This could, however, change somewhat since the venture capital people are somewhat more cautious about investing than they were a few years ago.

Of these start-ups, it is interesting to note that almost half of them are involved with ASICs, digital signal processing, or some type of niche system-solution product.

A last point here is that these same companies will eventually require their own fab facilities to maintain control over leading-edge processes. This is apparent since the capacity that does exist is not in the 1- to 1.5-micron range.

(Slide 24)

In discussing leading-edge technologies, I need to show you what the Japanese are currently doing in their funded projects. There are many more than these eight shown here, but these programs represent the most publicized ones at this point. As you can see, this ranges anywhere from the next-generation computers with very advanced architectures to projects to create new materials for a variety of applications. This of course indicates the commitment the Japanese government has toward supporting advanced research in areas they believe will take them into the next century.

(Slide 25)

The Technopolis concept is becoming an important topic when people discuss the direction the Japanese are taking in becoming a world force in technology. This program focuses on a complete strategy from the facilities to the actual R&D.

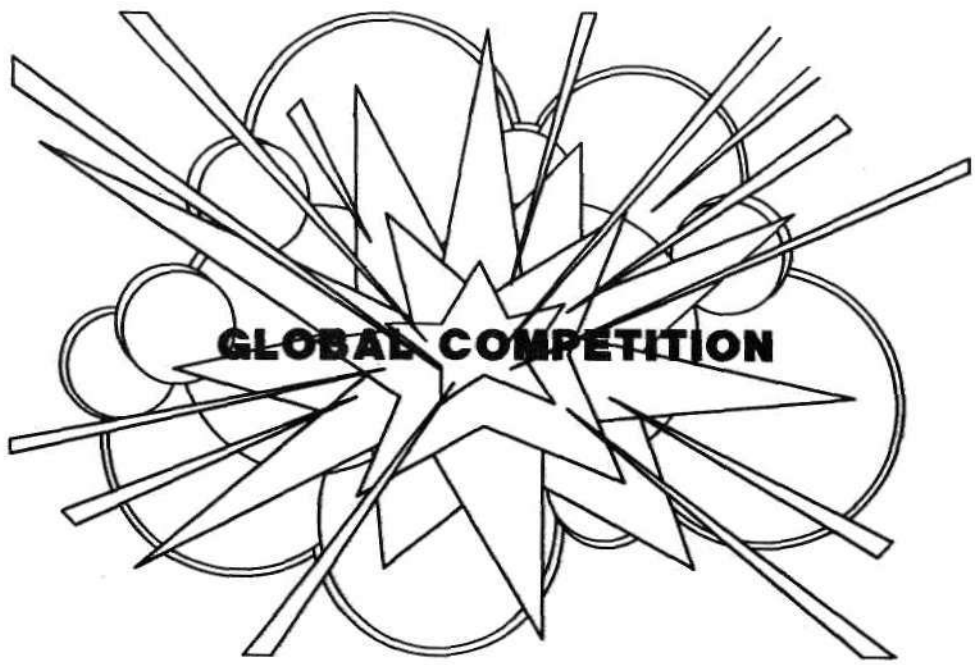
(Slide 26)

The synthesis for this is created by putting together the technology and the environment. This is to be performed in each of the prefectures where there are major technology centers.

(Slide 27)

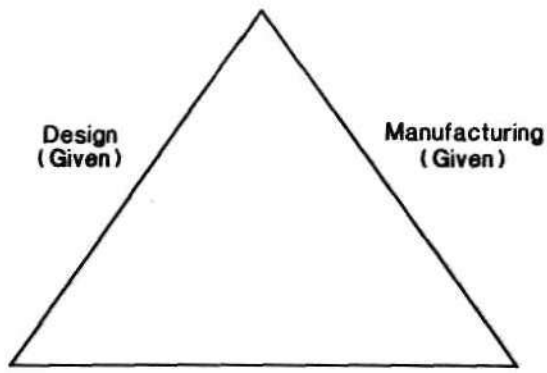
As you can see from this schedule, the program is fairly aggressive. While they do not wish to clone Silicone Valley, the Japanese want to extract the best parts and also inject some culture to make it complete from their point of view.

WORLDWIDE BUSINESS / TECHNOLOGY UPDATE



AN INDUSTRY TRANSITION —→1986 AND BEYOND

Three Technologies For Success



Marketing – An Application Market Focus

Source: Dataquest

THE CONCEPT OF TAILORED SERVICE

- Association with "the little guy"
- Customer service
- Niche market orientation
- Specialization
  - Financial
  - Retail

CLASS→MASS→MASS-CLASS EVOLUTION

A Class Market: Expensive cars	Devices for DP and military
A Mass Market: Basic transportation at low prices	Jelly beans
A Mass-class Market: Better cars, more diversity	Niche markets, ASICs, ASSPs

THE CUSTOMER'S CUSTOMER

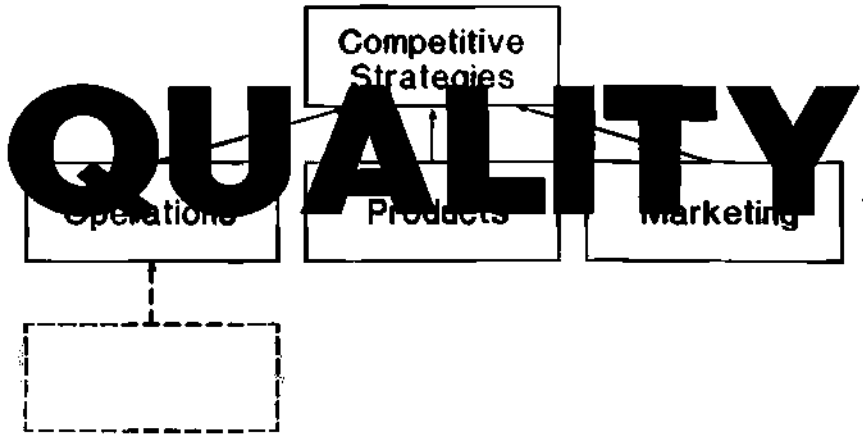
- Every boom → technology in the consumer's hands

- Semiconductors invisible
  - User doesn't know about technical benefits
  - Consumers care about results (What they see)

THE BUYER'S PERSPECTIVE

Focus on Operations

COMPETITIVE IMPACT ON OPERATIONS



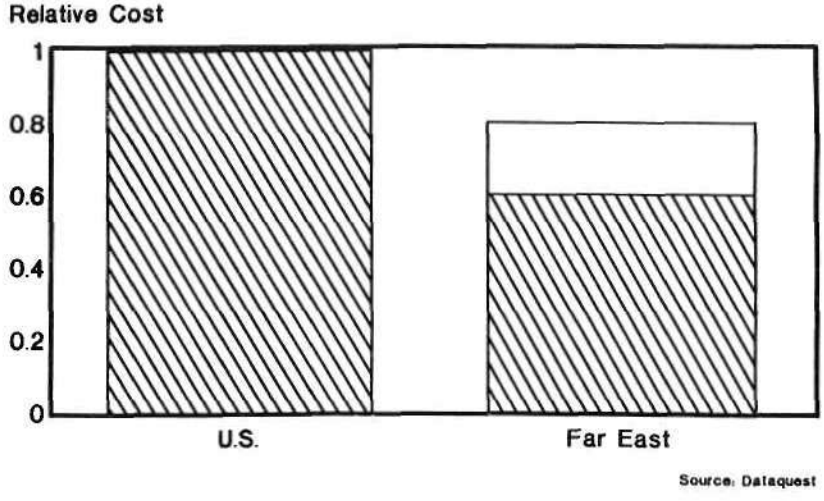
BUYER'S PERSPECTIVE

- Pricing – a global issue
- Impact of inventory management
- Partnering for success
- Streamlining operations
- Summary

PRICING

A global issue

COST OF MATERIALS



WORLDWIDE SEMICONDUCTOR DIRECTION FORECAST

(Billions of Dollars)

	1985	1986	1987
Worldwide	$24.8	$30.3	$38.5
North America	$ 9.6	$10.5	$13.3
Japan	$ 8.6	$11.9	$14.9
Europe	$ 4.7	$ 5.1	$ 6.4
ROW	$ 1.9	$ 2.8	$ 3.9

1986 and 1987: North America, Europe, Japan similar in growth
ROW displays greatest potential for consumption

Source: Dataquest

A WORLD PRODUCT OUTLOOK

- 1986 total IC consumption expected to reach 24% growth
  - Significant return from negative growth in 1985
- MOS technology demonstrates strongest overall growth
- MOS memories forecast to grow at 47% in 1987 - leads all others
- Logic strongest in 1986 MOS technology - driven by ASICs

ESTIMATED PRICING TRENDS

	1985	1986	1987
74LS00	$0.16–$0.18	$0.13–$0.18	$0.13–$0.18
74LS244	$0.58–$0.64	$0.31–$0.39	$0.32–$0.42
74HC00	$0.20–$0.25	$0.12–$0.19	$0.14–$0.19
74HC244	$0.62–$0.70	$0.36–$0.45	$0.38–$0.50
256K DRAM	$5.50	$2.35	$2.00
128K EPROM	$6.25	$3.11	$2.89

Source: Dataquest

ESTIMATED PRICING TRENDS

	1985	1986	1987
Z80 MPU	$ 1.75	$0.93	$1.13
8086 MPU	$10.25	$7.85	$6.81
68000 MPU	$ 9.70	$9.00	$7.50
Gate Array			
(2-micron CMOS)	--	$0.0020	$0.0019

Source: Dataquest

ESTIMATED NORTH AMERICAN ELECTRONIC EQUIPMENT OUTLOOK

(Billions of Dollars)

	1985	1986	1987	1990	CAGR 1986-1990
Data Processing	$ 80.4	$ 88.3	$ 97.2	$118.0	7.5%
Communications	28.6	31.8	35.4	49.7	11.9%
Industrial	34.9	38.8	44.0	57.2	10.2%
Consumer	16.2	17.0	18.4	21.6	6.2%
Military	49.2	54.8	61.4	72.7	7.3%
Transportation	8.5	9.6	10.8	15.1	12.0%
Total	$217.8	$240.3	$267.2	$334.3	8.6%

Source: Dataquest

FAST-GROWING NORTH AMERICAN EQUIPMENT MARKETS

(Estimated in Millions of Dollars)

	1985	1987	1990
Integrated Voice/Data Workstations	$ 203	$ 331	$ 789
Local Area Networks	$ 540	$ 740	$ 1,000
Cellular Mobile Radio	$ 802	$ 1,990	$ 4,434
Robotics	$ 552	$ 786	$ 1,637
Nonimpact Printers	$ 363	$ 1,652	$ 2,972
Personal Computers	$21,616	$25,646	$31,458
Sub-5.25-inch Rigid Disk Drives	$ 2,591	$ 3,544	$ 5,187

Source: Dataquest

RANKING OF MAJOR END PRODUCTS BY SEMICONDUCTOR CONSUMPTION IN DOLLARS

	1982	Percent of Total	1984	Percent of Total	1985	Percent of Total
VCRs	1	16.3%	1	18.0%	1	14.9%
General-purpose Computers	2	9.3%	3	10.1%	2	9.5%
Office Computers	15	2.0%	8	3.0%	3	9.1%
Personal Computers	8	3.5%	2	10.9%	4	8.3%
Tape Recorders	4	7.5%	5	5.6%	5	7.0%
Color TVs	3	8.9%	4	6.8%	6	5.9%
Copying Machines	9	3.4%	6	4.1%	7	4.9%
Peripherals	-	3.1%	9	2.8%	8	3.1%
Automobiles	6	3.5%	7	3.2%	9	3.0%
PBXs	7	3.5%	10	2.7%	10	2.3%

Source: Dataquest

HOTTEST END MARKETS FOR SEMICONDUCTORS RANKINGS IN TOP 100

	1982	1984	1985
Digital Audio Disk Players	47	33	18
Word Processors	31	17	12
Facsimile	21	14	13

Source: Dataquest

START-UPS

- 1985
  - Minimum of 12 new companies
  - Most in Santa Clara Valley
- 1986-1987
  - Several have not announced themselves yet
- About 50% in ASICs
- Emphasis on system-level solutions
- Must build their own fabs to survive

JAPANESE TECHNOLOGY PROGRAMS

- Optoelectronics project - optical computer/control
- Supercomputer project - high-speed computer
- Fifth-generation computer - nonalphanumeric data
- Next-generation industries - accelerated development
- Future electron devices - VLSI for the 1980s
- New materials project - new alloys
- Bioelectronics project - for many uses
- Advanced robotics project - mobile robotic systems

WHY TECHNOPOLIS?

JAPANESE SYNTHESIS

Technology
+
City Building =
TECHNOPOLIS

TECHNOPOLIS CONSTRUCTION SCHEDULE

1980	MITI "Visions for the 1980s"
1981	Technopolis '90 committee report
1982	Technopolis law
1983	Development concept hearings
1984	Formal designation (16 sites)
1985	Construction/technomart concept
1986	New media community program
1990	Complete basic infrastructure
2000	Complete Technopolis program

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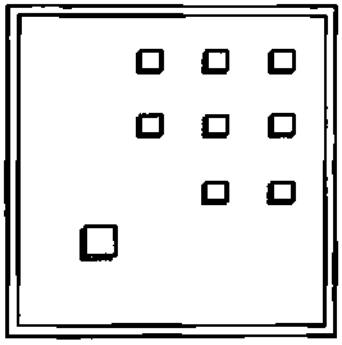


Dataquest
IC Outlook '87

September 15-23, 1986

EUROPEAN INDUSTRY UPDATE

JIM BEVERIDGE
Dataquest UK Limited

Good morning, ladies and gentlemen.

Before looking specifically at the European market status and market estimates for 1986 through 1991, I believe it is worthwhile, in order to view the outlook more clearly, to recap the past very briefly.

As Brand has stated, the '85 downturn produced the worst recession that the semiconductor industry has ever experienced. In the United States, consumption dropped a staggering 27 percent. In Europe and Japan, the decline was more moderate at 4 percent and 3 percent, respectively. In the rest of the world, a decline of 17 percent was experienced.

The outlook is dependent upon the relative importance of the economic forces shaping demand. Fiscal policies in North America are less expansionary and moving in the direction of less restriction elsewhere. Interest rates have fallen and show signs of falling further. Oil prices have declined dramatically and now seem to have stabilized. With the assumption that there will be no change in monetary or fiscal policies, the resulting effect could be higher domestic demand growth with net exports dependent upon currency exchange rates. However, it is expected that positive net exports will make negligible contributions to GNP growth.

While expectations are therefore for a more modest recovery, it will seemingly be more soundly based and less likely to terminate abruptly as has been the case in the past.

Recently there have been signs that the earlier optimistic announcements concerning the positive effect the fall in the price of oil would have on the general economy have been somewhat premature. What almost all the economists overlooked was the way in which the oil fall would affect the losers. The Texas oil magnates and the Arab sheiks have reacted by cutting back their spending quickly in order to stop themselves from running into debt. The gainers by contrast have been savoring their real incomes rising in the bank before rushing out to spend. In essence, this has inserted a time lag into the economic growth time scale. This has been taken into account in our forecast to which I shall now turn.

The criteria and assumptions made in the generation of our estimated European quarterly shipment forecast still hold. Nothing substantial has transpired which would lead us to revise the forecast.

Four major assumptions were made in producing our forecast involving:

- Distribution
- The book-to-bill ratio
- The acceleration of recovery
- Underestimation of market swings

We assumed that distribution inventory would come under control and that there would be less back-to-back ordering on principles. This has happened. We further assumed that the book-to-bill ratio would continue to move upwards through 1986 and into 1987. This is happening, and although there has been a slowdown in the rate of change very recently, the trend is still positive.

Indications now exist that the general recovery which is going through a period of stabilization in the second half of 1986 will continue through 1987.

The final assumption that was introduced into the equation was that the magnitude of the market swings are always underestimated. With the tight coupling between production and demand that exists in the industry today, the concern is that an unexpected rise in demand could trigger a shock wave resulting in the demand outstripping manned capacity. We are of the opinion, because of the relatively low levels of capital investment in the late 1985-early 1986 time frame, that 1988 will be a year of capacity shortage and should be a year of strong profitability for the industry.

Looking now at the end-user consumption split for Europe, it can be seen that the market is dominated by four major segments: telecommunications, industrial, consumer, and computer. It is the existence of this balanced market that has helped Europe to weather the storms of the industry a little better than the United States.

In terms of the growth pattern, the telecommunications segment has consistently increased its importance, from a 19.6 percent market share in 1984 to a projected 25.7 percent of the total market in 1986. We expect this trend to continue and that by 1991 telecommunications will represent 26 percent. The consumer segment, however, continues to show some decline in market share, shrinking from 24.7 percent in 1984 to 19.3 percent in 1986, with a continuing downward trend through 1991.

A higher than industry average growth rate is expected in both the computer segment and automotive segment as the resurgence in professional minicomputer and office automation manufacturers continues and as exhaust emission regulations yet to be introduced impact on the level of electronic control systems adopted by motor vehicle manufacturers.

This slide shows the individual dynamics within these growth trends and at the same time shows an industry slowdown in the 1989 time frame, very much in keeping with the industry cycles we have come to love and hate.

The regional breakdown shows the continuing trend of higher than average growth in the United Kingdom. Although West Germany is still ahead of the United Kingdom and Eire, we estimate that in terms of integrated circuit consumption the United Kingdom and Eire will continue to represent the largest market in Western Europe.

France is predicted to grow at a much higher rate than any other West European country, recovering to pre-1984 levels. Higher than average growth is also expected in Scandinavia as more and more of the major users in this region expand still further their worldwide horizons, particular in the telecommunications, office automation, and data processing industry segments.

Marginal declines in market share are expected in the remaining European countries, their growth being limited primarily by the weakening European consumer electronics market, despite strengths in automotive, telecommunications, data processing, and office automation.

I would like to look now at the changes occurring in integrated circuit consumption. The trends we are seeing are very much in line with world trends and you can see here the impact that the increasing consumption of MOS and in particular CMOS integrated circuits are expected to have.

I stated earlier that by 1991 integrated circuit consumption will account for nearly 86 percent of total semiconductor consumption, growing at a CAGR of 22.8 percent. Within this we expect total MOS integrated circuits to grow at a much faster rate of 27.9 percent, being driven specifically by the very high growth in CMOS.

The relative importance of this dramatic swing to CMOS on the three major product categories--Logic, Memory, and Microprocessor--can more readily be seen here.

In 1986, we estimate that the combined MOS and bipolar logic market will reach $1.44 billion, of which 42.2 percent will be bipolar. Of the estimated $0.90 billion total memory market, only 14.5 percent will be bipolar.

By 1991, partly because of the rapid growth in ASIC products and the continuing shift to high-speed CMOS standard logic, MOS logic products will represent 67 percent of a combined MOS and bipolar market of $3.7 billion.

The consumption of memory products is expected to grow from $0.90 billion in 1986 to $2.7 billion by 1991, with bipolar devices declining to 8.4 percent of this total.

The microprocessor market is one in which bipolar products never really gained a significant portion of the market. We anticipate that in 1986 the MOS microprocessor market will grow by 15.7 percent to $0.55 billion and that by 1991 this will have grown at a CAGR of 32.0 percent to $2.2 billion. I will deal with a more in-depth analysis of the MOS micro and memory market this afternoon. I would now like to turn my attention to the critical period leading into the third millennium: 1991 and beyond.

I say "critical" because the seeds for success in this period are being sown today. Decisions affecting investment in people, plants, and systems are already starting to shape the European semiconductor industry of the 1990s. I therefore wish to act as a catalyst for thought and provide you with our perspective of what we see happening to the European industry in the 1990s. The elements of my speech are depicted as follows:

- The marketplace
- The technology
- The vendor base
- The users

The Marketplace

Ten years ago, the European semiconductor marketplace was worth $1.6 billion. Since then, despite the negative impact of exchange rates, it has grown to an estimated $5.1 billion, 17 percent of the total world marketplace. We project the European market growth rate over the next ten years to exceed that of the world's, at a CAGR in excess of 18 percent, ending up at $25 billion by 1996. This tells us that in the 1990s we will be participating in a highly dynamic, world-class marketplace.

This dynamism is further reinforced when we consider the growth of the integrated circuit sector of the marketplace. As Peter pointed out, since 1982, IC consumption in Europe has been the fastest-growing semiconductor market worldwide. This performance has been achieved despite the low pricing in commodity families due to the European "battleground" effect. Let me explain what I mean by this term. In the late 1970s and early 1980s, multinational corporations saw the European market as a battle zone. The companies understood that by winning European market share and thereby increasing their global production volumes they could ramp their costs down faster than their competitors, forcing weaker companies to exit the market. During the 1970s, the product was Standard Logic, the combatants the American multinationals. In the early 1980s this changed, and open season in the MOS memory market was declared as Japanese and American companies strove to maximize their global market share. Despite the low average selling prices that resulted from these confrontations, IC consumption grew. The growth of the strategically important IC sector gives us every confidence that the marketplace can achieve the growth rates projected. Let us turn now to technology.

The Technology

Over the last few years, European technologists have succeeded in maximizing Europe's prominence on the world technology map with state-of-the-art production processes. This was not always the case, although we in Europe never lacked the basic resource--innovation. Indeed, creativity and inventiveness are skills which have been and are still in plentiful supply. We lacked, however, the vision, the drive to take our products to market.

We have to thank our North American friends for the example they set the European semiconductor industry in the late 1960s and early 1970s. Texas Instruments, Motorola, National Semiconductor, and others investing heavily in Europe, taught by example how to market products effectively, how to apply a global rather than regional perspective to business, and in essence how to grow and apply technology for profit.

Whatever our weaknesses, "not invented here" (NIH) has never been a European trait and we continue to learn from both our North American and Far Eastern counterparts.

Today, we believe our home-grown technology, like our marketplace, is world class. If you divide silicon technology into the elements of material science, processing, systems architecture, and packaging you will find that in the 1990s Europeans will major in every category.

Let me give you some specific examples of where we are today.

In materials, we have Wacker Chemitronic supplying industry standard 6-inch wafers, and planning for the mid-1990s 8-inch and 10-inch dinner plate slices of silicon.

In processing, we have state-of-the-art high-voltage processes from SGS and production smart-card technology from Thomson and Bull.

In architecture, Siemens is leading the world with its advanced telecommunications ISDN concepts, and Inmos with its parallel processing transputer.

In packaging, Philips was the pioneer of surface-mount technology and the miniature SOIC--and is a leading producer of production equipment.

How does this expertise benefit you and I in the 1990s?

It is important to realize that processed silicon is today the raw material of the electronics industry. A strong presence in silicon is fundamental in keeping Europe's component, electronic, and equipment industries cost competitive, and thereby successful in the international marketplace.

Processed silicon has served to buffer the industry and consumer from the ravages of inflation. In more traditional industries this has not been the case. By way of illustration, consider an example of the automotive industry versus the electronics industry. In 1960, a small car would have set you back approximately $800. Today that car's equivalent price lies in the region of $6,000. Contrast that with the black-and-white television receiver, which because of its use of increasingly sophisticated semiconductors, has held its cost of manufacture, for all intents and purposes, constant in the past 26 years.

To summarize, a healthy semiconductor technology base is fundamental to a healthy European industrial economy. We believe that European companies are successfully building that base for the 1990s.

Let us turn our attention now to the people servicing the component demand--the suppliers.

The Vendor Base

Interestingly enough, the solid European technological base has the additional knock on benefit in that it makes it increasingly attractive for suppliers to invest in Europe. The rate of investment in Europe has been steadily increasing since the early 1980s fueled by a creeping realization by European governments' heads of the strategically significant role electronics will play in the struggle to create wealth and employment for their citizens in the 1990s. This has led to a regional marketing drive to increase inward investment in high technology.

There are currently more than 130 merchant manufacturing sites in Europe distributed so. Specific centers of excellence have sprung up, characterized by local concentrations of manufacturers and suppliers, healthy input from quality technical universities, and efficient global communications links.

We will soon be at the stage where each country has its own local Silicon Valley. This pattern of resource distribution has advantages for both vendor and user. The vendor covering a number of sites has greater flexibility in determining where to produce products that will match the local market's needs. The user benefits by increased local service at both technical and commercial levels.

As I have previously mentioned, the European semiconductor marketplace of the early 1980s was considered to be the battleground between the American and Japanese suppliers for commodity products. European suppliers who today supply over a third of the total European consumption, have for the past few years been investing heavily in plant and equipment with the intent of becoming world market forces. For example, SGS now has over 50 percent of its output running off 5-inch and 6-inch wafers, which is twice the industry average. Philips and Siemens

are working together on the development and production of megabit static and dynamic RAMs. Thomson has boosted its international presence through the acquisition of Mostek's assets. In the United Kingdom, Plessey has brought in a new breed of innovative, goal-oriented management to capitalize on its advanced semicustom products and to manage its sub-1.5 micron facility in Roborough. We believe that many European companies have moved up the league into the premier division and are well positioned to regain lost market share internationally.

Meanwhile, the by-products of the industry achieving critical mass are coming into view: European start-ups! Surprisingly, an ever-increasing number of brave, intrepid engineers are setting up companies to innovate the technology and systems of the future. I say surprisingly because stock options and stock ownership laws are very difficult and the rules concerning taxation of investment are burdensome. In addition, raising venture capital across Europe is time-consuming because each country has its own system and large syndicates are the exception rather than the rule. Nevertheless, the pioneers are winning, and making life easier for their followers.

Thus, we have in a nutshell the European supplier's scenario of the 1990s. American and Japanese suppliers will continue to play a major role in the marketplace, the first division of European companies will move into the world league, and the start-ups will work their way up to the first division. It's going to be an interesting game, both home and away.

The Users

Last, and by no means least, let us turn to the European user in the 1990s.

As Jerry Sanders pointed out at this conference last year, the bigger companies are growing larger at the expense of the smaller companies. Thus it is in general industry, where the oligopoly of large corporations is growing stronger.

This, combined with the increasing number of semiconductor purchasing outlets driven by the pervasion of semiconductors into all sectors of industry, leads to a stretching of the consumption distribution profile. Concurrently with this, we see a blurring of the edges of the traditional industry, with segments of the computer, telecommunications, and consumer industries merging to form an information technology sector.

Here we have the classic dilemma for the semiconductor supplier: how to organize? If he structures his organization to take account of these changes, then he will be rewarded with client satisfaction, the good identification of business opportunities, and a motivated sales force. Get the formula wrong, and he could end up with an organization that

spends an inappropriate percentage of its time discussing internal issues such as responsibility and compensation. This results in a decrease in business visibility and client service. To fit the needs of the user means that all sections of the organization must be in harmony with the user's desires, not only those of the local sales office.

Now let us consider what we perceive to be the needs of the user of the 1990s. Let us start by considering what he doesn't want:

- Hundreds of semiconductor salesmen pounding on his door
- Inaccurate leadtimes
- To deal with opportunistic pricing policies
- To invest money in incoming test equipment
- To hold inventory
- Incorrect shipments
- To be bound hand and foot to the services of one ASIC manufacturer (although a number of manufacturers would have you believe otherwise)

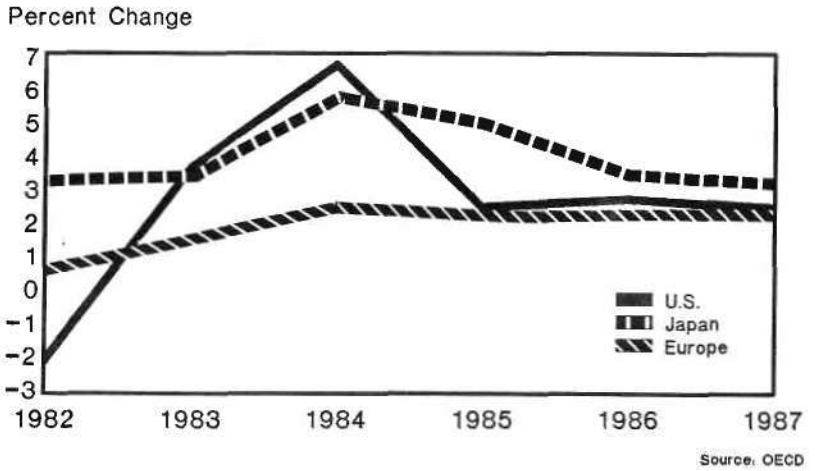
It's very easy to expand this list and it's also very easy to state what the user does want in one word: service. The development of an organizational service culture is a key criterion which will allow suppliers to mold themselves to the user's fast-changing demands in the 1990s. Ultimately, it will be instrumental in determining the survivors in the ongoing evolution of the industry.

In the last few minutes I have demonstrated our perception of the European marketplace, of European technology and of the future of European suppliers. One common theme links all of these projections of the 1990s: we can achieve our forecasts, we can achieve our goals, we can achieve success, but we will only achieve them if we service our clients. It pays to remember that the customer is our only source of income and that serving him is the key to success and survival.

Thank you.

WORLDWIDE ECONOMIC SUMMARY

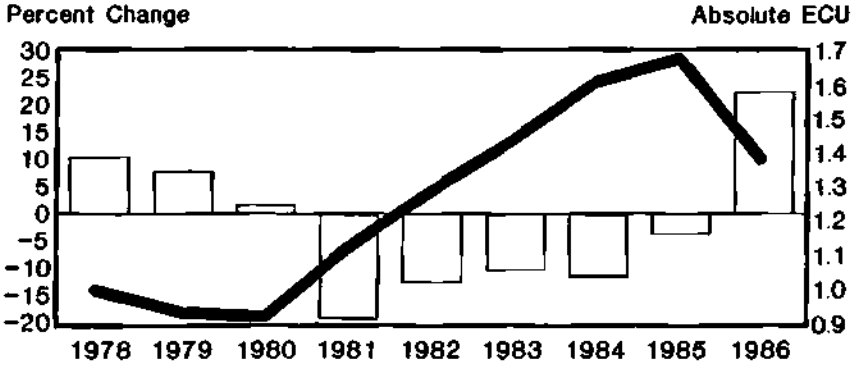
Estimated Growth of Real GNP



Source: OECD

ESTIMATED YEARLY AVERAGE WEIGHTED EUROPEAN CURRENCIES VERSUS U.S. DOLLAR

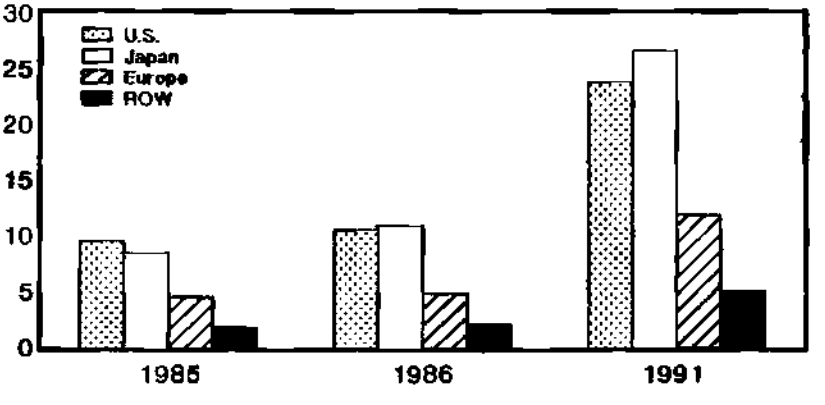
1978 Through 1986 YTD



Source: DATAQUEST

ESTIMATED WORLD SEMICONDUCTOR CONSUMPTION PROFILE

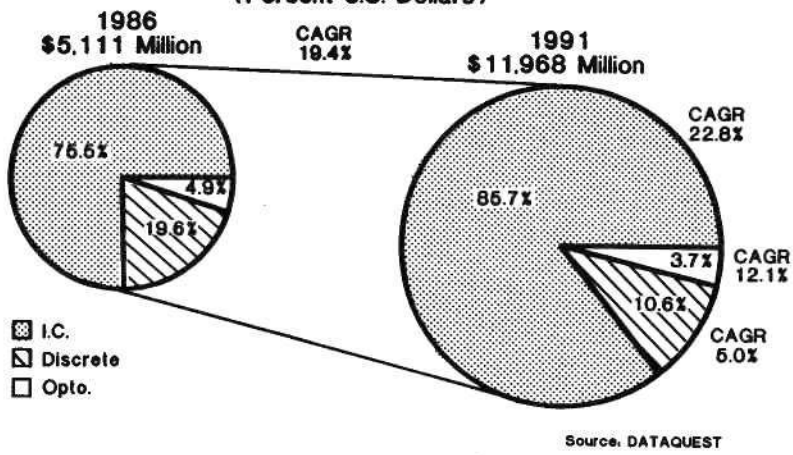
Billions of U.S. Dollars



Source: DATAQUEST

ESTIMATED EUROPEAN SEMICONDUCTOR CONSUMPTION

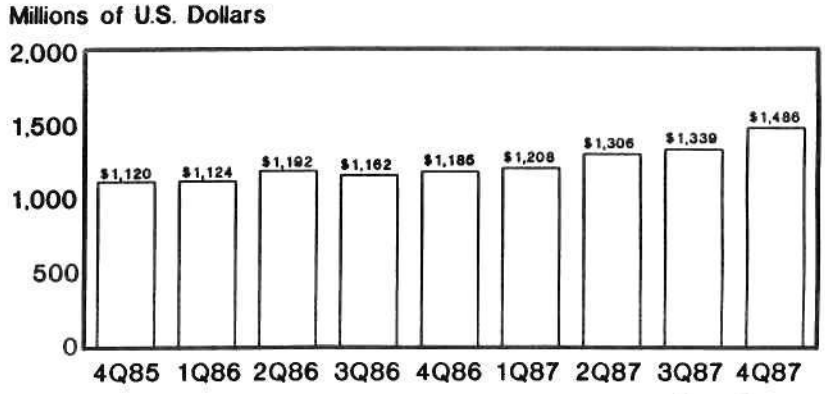
(Percent U.S. Dollars)



Source: DATAQUEST

ESTIMATED EUROPEAN SEMICONDUCTOR QUARTERLY SHIPMENTS

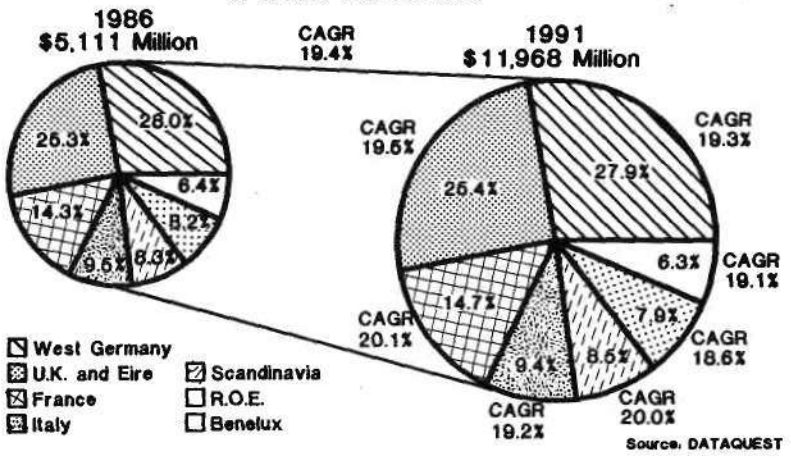
1986-1987



Source: Dataquest

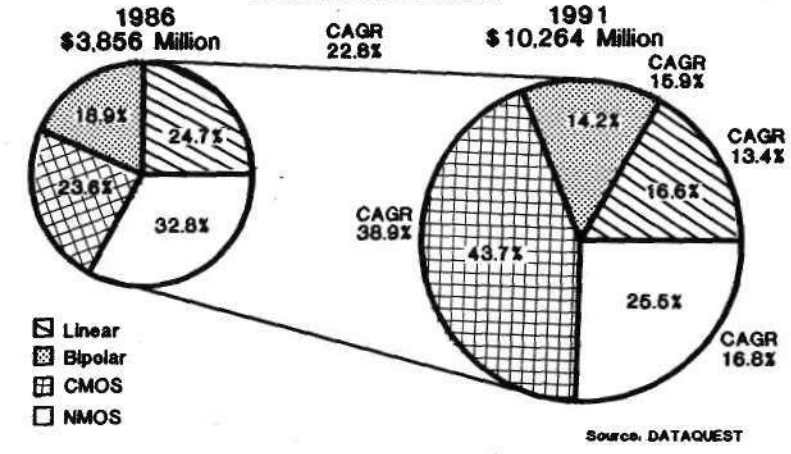
ESTIMATED SEMICONDUCTOR CONSUMPTION - BY REGION

(Percent U.S. Dollars)



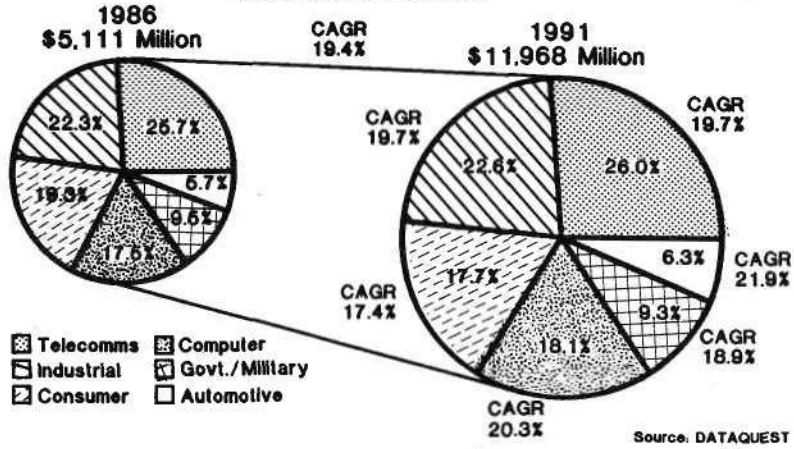
ESTIMATED EUROPEAN INTEGRATED CIRCUIT CONSUMPTION - BY TECHNOLOGY

(Percent U.S. Dollars)

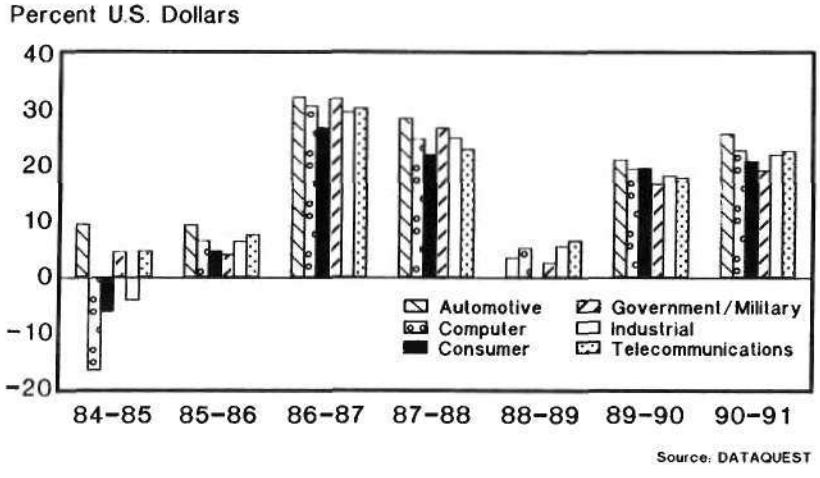


ESTIMATED EUROPEAN SEMICONDUCTOR CONSUMPTION - BY END USE

(Percent U.S. Dollars)

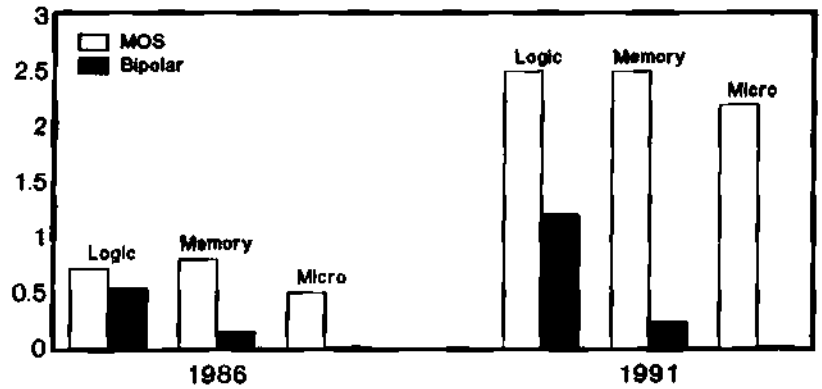


ESTIMATED EUROPEAN SEMICONDUCTOR CONSUMPTION GROWTH BY END USE

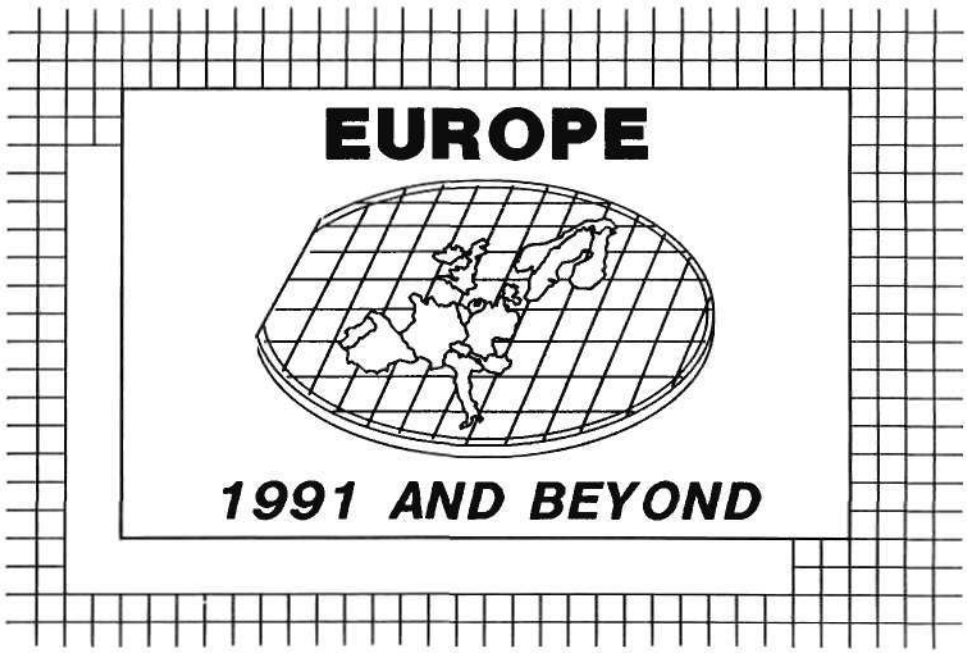


ESTIMATED EUROPEAN LOGIC, MEMORY, AND MICROPROCESSOR CONSUMPTION

Billions of U.S. Dollars



Source: DATAQUEST

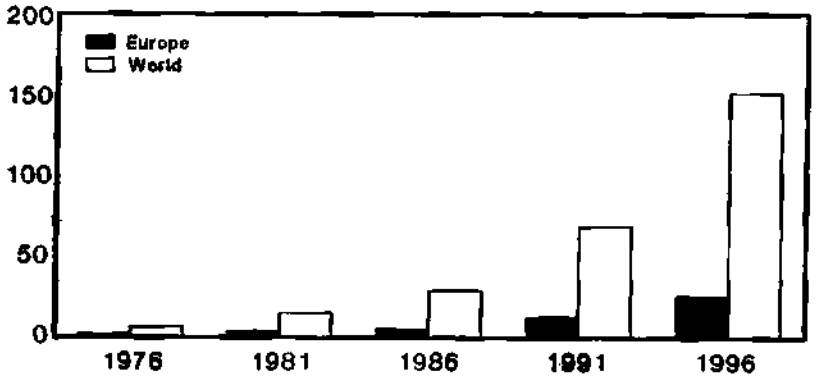


1991 AND BEYOND

- The market
- The technology
- The vendor base
- The users

ESTIMATED WORLD AND EUROPEAN SEMICONDUCTOR MARKETS

Billions of U.S. Dollars

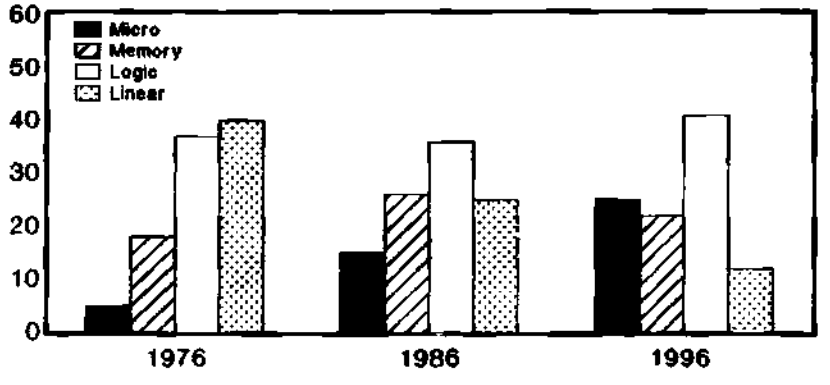


Source: DATAQUEST

ESTIMATED EUROPEAN IC MARKET

Micro, Memory, Logic, Linear

Percent (Based on Dollars)



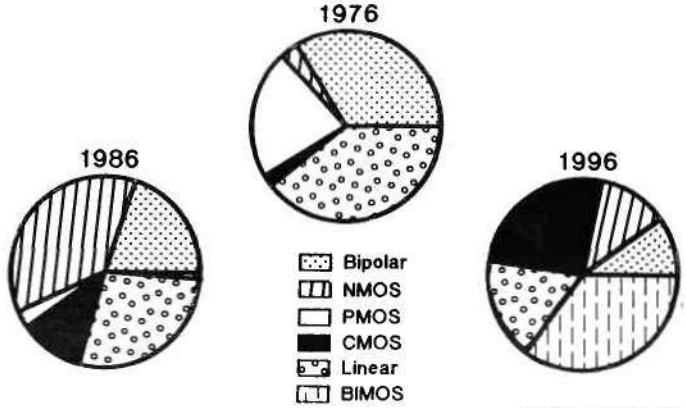
Source: DATAQUEST

1991 AND BEYOND

- The market
- The technology
- The vendor base
- The users

ESTIMATED EUROPEAN PRODUCTION AND SHIPMENTS BY TECHNOLOGY

(Percent)



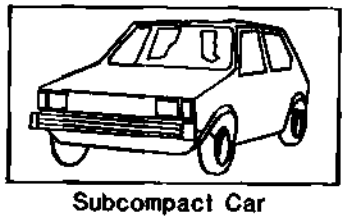
Source: DATAQUEST

EUROPEAN TECHNOLOGY

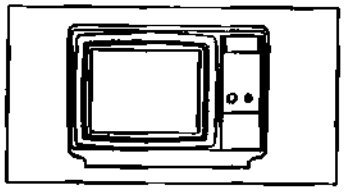
Materials:	Wacker, B.O.C.
Processing:	SGS, Thomson, Bull
Architecture:	Siemens, Inmos
Packaging:	Philips

Source: DATAQUEST

SEMICONDUCTOR TECHNOLOGY
BEATING INFLATION



Subcompact Car



Black and White TV

	1960	1986
Subcompact Car	$800	$6,000
Black and White TV	$100	$100

Source: DATAQUEST

1991 AND BEYOND

- The market
- The technology
- The vendor base
- The users

EUROPEAN PLANT LOCATIONS

100+ Existing Facilities
57 Operating Locations

Source: DATAQUEST

PLANNED NEW PRODUCTION LINES?

Source: DATAQUEST

EUROPEAN START-UPS

Company	Location	Product
ES2	Munich, Germany	Fast Turnaround ICs
Langenden	Eindhoven, Holland	ASICs
Inmos	Bristol, England	Memory, Micro
IPS	Livingstone, Scotland	Power ICs
Micron Semiconductor	Lensing, England	Detectors
Mietec	Brussels, Belgium	Telecom Custom
Wolfson Microelectronics	Edinburgh, Scotland	Custom ICs
Qudos	Cambridge, England	ASICs

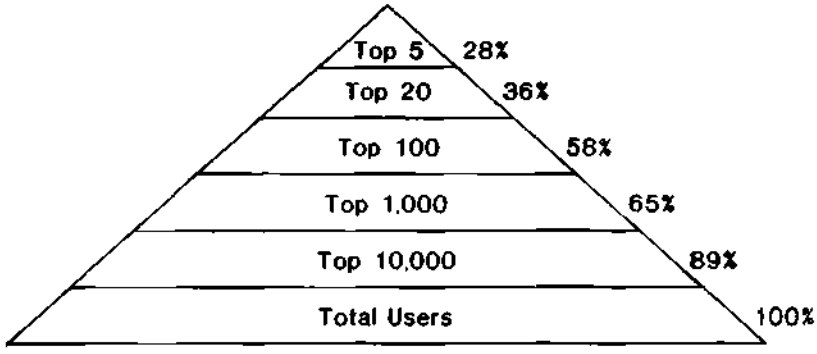
Source: DATAQUEST

1991 AND BEYOND

- The market
- The technology
- The vendor base
- The users

ESTIMATED EUROPEAN SEMICONDUCTOR PURCHASING - 1996

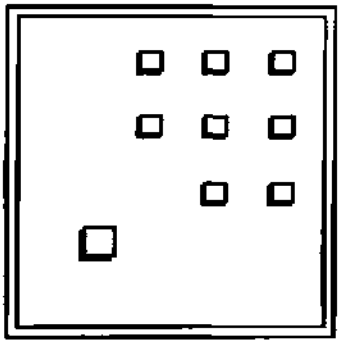
(Percent of Total Consumption)



Estimated Number of Users = 90,000

Source: DATAQUEST

Dataquest
a company of
The Dun & Bradstreet Corporation



Dataquest
IC Outlook '87

September 15–23, 1986

ASICs AND LOGIC

PETER SAVAGE
Dataquest UK Limited

We have grouped these two product categories together here because they are used in much the same way. Application-specific ICs, or ASICs as we call them, are primarily gate array and/or cell-based products that are replacing standard logic integrated circuits in many different applications.

The interrelationships can be seen more clearly when looking at the integrated circuit family tree. Within the major top level category of logic integrated circuits there are three subcategories: standard logic, application-specific, and a new category, recently created, application-specific logic products (ASLPs). This new third category has been created as a result of the synergism of application-specific integrated circuits (ASICs) and the demands of certain end-markets, creating a whole new breed of products and business opportunities. These products are aimed at unique applications, such as in telecommunication and digital signal processing. Effectively, dedicated products fall into this category. Typical devices would be single-chip modem integrated circuits, multiplier accumulator integrated circuits, and fuel injection controllers. There are many different types of products.

It is not the intent here today, though, to cover within this ASIC and Logic presentation the category of application-specific standard logic products (ASLPs) since it is an area that is particularly diverse and end-use dependent. I wish to mention, however, that we are in the early planning stages for a Focus Conference on telecommunications to be held early in 1987, which will cover in detail the semiconductor activity and trends in this market sector.

Let us move on now to look at standard logic.

Standard logic has been with us for more than 20 years. Although the early logic families, RTL and DTL, have long since ceased to be of any significance, the 7400 series TTL products have evolved into new families since their introduction in 1965, and continue to evolve.

We are of the opinion that the revenue in Europe derived from standard logic will peak by the end of this decade and begin to go into a slow decline. There are some thoughts in the industry that the peak may occur before 1990, but with new families being introduced and new process technologies replacing others, we see continued growth throughout this decade.

The driving force with all standard logic is technology, and as wafer fabrication and microlithography have advanced there have been corresponding advances in the performance of product families. This slide, courtesy of Texas Instruments, shows how the speed/power product advances of various TTL and CMOS families have improved as technology has advanced. Each shift in technology has brought more suppliers to the market and this evolutionary process is still continuing.

At the present time, system designers and machine architects make their design choices based on the speed/power criteria from the spectrum of standard logic components available to them.

The design choices are illustrated here and as one would expect, the design boundaries are not sharp. Overlap occurs with all product families. We expect by the end of the decade that the speed/power performance of AS-TTL and ALS-TTL will improve signficantly and that the propagation delay of the CMOS families will decrease substantially. The trend then, is for the present relatively large differences in technical performance, speed, and power, for each of the families to become smaller. Our firm belief is that gate propagation delays of HC/HCT CMOS and TTL will tend towards the delays of ECL and that the difference in power dissipation between CMOS, TTL, and ECL will decrease. As this occurs, a more meaningful system parameter, system throughput, will emerge and be used to compare the different standard logic families.

Looking now at the life cycle of standard logic, we can see here the relative position of the standard logic families on the life curve. The early 74 series logic families are mature or declining, as new system designs make use of products in the growth stage, such as 74 ALS and CMOS 74HC/HCT. Lower gate propogation delays, lower power consumption, and increasing price parity at some complexity levels have made these devices more attractive. This is especially true for the more advanced CMOS families.

The original 4000/74C parts are very mature as a technology but are useful in specific higher-voltage applications. The newer CMOS logic (HC, HCT) is still growing but is likely to be replaced by low-cost CMOS gate arrays, a situation which has been exacerbated by eroding per-gate prices in mature technology gate arrays. The newest ACT CMOS logic families appear to be a longer-term replacement alternative, and as such are attracting more vendors as the family expands.

The standard ECL families are mature in technology. High-performance ECL gate arrays are a natural replacement for ECL standard logic, due not only to the increased performance in gate speed, but also to the reduction of package interconnect delays associated with discrete logic devices.

Standard logic pricing has substantially stabilized from the levels experienced in 1984 and early 1985. Most spot prices of standard logic devices are at or below the contract prices shown here. Leadtimes are lengthening relative to 1985, but are still approximately half the time span experienced in 1984. We expect the pricing of more mature product lines (74S and 74LS) to slowly increase in 1986 and on out into 1987. Increased competition coming from Japan on the 74HC and 74ALS families is exerting strong pressure on prices. Price parity currently exists in the low gate count devices. By mid- to late-1987, we expect total price parity to be reached. A point worth noting, however, is that many of the larger users that have vendor assessment programs in place are ranking quality and service before price, and awarding business to top-performing vendors in quality and service.

So what are our medium-term European consumption estimates for standard logic ?

In 1986 we expect total bipolar standard logic consumption to grow by 2.7 percent, compared to 1985, reaching $377 million. Within this growth, however, LS TTL, by far the largest portion of bipolar standard logic, will decline 4.2 percent to $204 million. A decline of 16.3 percent compared to 1985 will be seen in standard TTL, as revenue derived from this family continues to follow the life curve presented earlier into the phaseout stage. It will be the remaining families of ALS, AS/FAST, and ECL that will fuel the modest growth in bipolar standard logic in 1986. ALS will grow by nearly 26 percent to $34 million; AS/FAST will grow by 35.5 percent to $61 million; and ECL will grow by 10.8 percent to $10.8 million. For 1987, in keeping with our total semiconductor and particular total integrated circuit forecast, we are predicting a more robust growth for bipolar standard logic, compared to 1986, of 16.7 percent.

Within this growth, the highest increase will be seen in ALS, with revenue rising to $58 million, a growth of 70.6 percent compared to 1986. LS TTL will recover slightly to $229 million, representing a growth of 12.2 percent compared to 1986, before following the decline into maturity and phaseout.

By 1990 total bipolar standard logic will have grown at a CAGR of 8.0 percent, compared to 1985, reaching $540 million. CAGRs of 36.1 percent and 26.4 percent will be experienced in ALS and AS/FAST, compared to 1985, with revenue reaching $126 million and $145 million, respectively. LS TTL on the other hand will have declined to $121 million, a CAGR of negative 2.2 percent compared to 1985.

Looking now at CMOS standard logic, in 1986 we expect consumption revenue to reach $113 million, or 23 percent of the consumption of total standard logic. This represents a growth of 10.8 percent compared to 1985, four times greater than bipolar standard logic, but not achieving the level seen in 1984, after the significant decline in 1985. By 1987 CMOS

standard logic is expected to grow by 51.3 percent, compared to 1986, to reach $171 million. This slide, apart from showing absolute values for the 4000 series and 74HC series of CMOS standard logic, also shows the changeover from 4000 series to 74HC occurring from 1988 to 1989 to the point when consumption of 74HC in 1989 will reach $122 million, greater than ALS TTL and within $2 million of AS/FAST in the same year. By 1990, CMOS standard logic is forecast to grow at a CAGR of 19.7 percent, compared to 1985, to $251 million. The 4000 series family, having peaked in 1987, is projected to grow at a CAGR of 2.3 percent by 1990 compared to 1985, revenue declining to $84 million. In contrast, the 74HC family is expected to grow at a CAGR of 44.0 percent during the next five years such that consumption will reach $167 million in 1990.

Now while we expect total standard logic to grow in absolute terms, the growth will be less than the market growth for total integrated circuits. Consequently, standard logic will decline as a percentage of the total integrated circuit market, having peaked as a percentage in 1984.

This is clearly the result of the impact that application-specific integrated circuits is having and will continue to have on standard logic shipments.

Gate arrays are being more and more widely used in systems as a lower-cost alternative to standard logic, soaking up the numerous "glue" logic elements in a system and integrating into a single device. As a result of these changes, we expect the number of functions (gates) in the form of gate arrays to exceed those delivered in the form of SSI/MSI standard logic devices in 1987. This ASIC impact can more readily be seen here where the growth of standard logic is almost flat in comparison to application-specific integrated circuits.

In 1985, the consumption of application-specific integrated circuits exceeded that of total standard logic by 12.8 percent. By 1990 ASIC consumption will be greater than two times that of total standard logic.

So, what is an ASIC?

There has been and, I think there will continue to be, a considerable amount of discussion throughout all sectors of industry, semiconductor manufacturers and users alike, on this very question.

To make this next section of the presentation on application-specific integrated circuits (ASICs) clearer and to ensure that at least some commonality is achieved here, I feel it worthwhile to spend just a few minutes looking at the ASIC family tree and considering the definitions of the various ASIC subcategories.

Custom, as you can see, has the subcategories of Full Custom and Cell-Based Design (CBD). Full Custom products are hand-crafted, unique designs implemented without the use of precharacterized cells or macro cells. Cell-Based Designs, on the other hand, are defined to include integrated circuits, either digital or mixed linear/digital, that are customized using a full set of masks and that comprise precharacterized cells or macros. This includes standard cells, megacells, and compilable cells. On the semicustom side of the tree, the subcategories of programmable logic and gate array exist. Gate arrays are defined as either digital or mixed linear/digital integrated circuits containing a configuration of uncommitted elements. These uncommitted elements can be as small as a single two-input gate in the case of a standard gate array, or a core cell such as a microprocessor or 16K DRAM combined with an expanse of the smaller elements in the case of a structured array.

Customization is implemented by interconnecting these elements with one or more routing layers. In the final category, programmable logic, are logic or gate arrays that can be programmed by the end user and not at any stage during the device manufacturing process.

With these definitions in mind then, let us move on to review the ASIC market. The application-specific device has actually existed since the mid-1960s, coming into being at approximately the same time as standard logic. Widespread acceptance of ASICs however did not occur until the early 1980s. The devices introduced in the 1960s were the forerunners of today's gate array-type products. Further evolutions of the various ASIC technologies have resulted in significant increases in circuit density and a dramatic increase in cost effectiveness. Continued acceptance of ASICs in almost all end-product designs will aid in the decline of standard logic.

System designers have four distinct ways to design ASICs. Each offers a trade-off in development cost and prototype device lead time. The major benefits, however, are at the system manufacturing level. ASICs offer:

- Lower manufacturing costs
- Lower power consumption
- Smaller system size
- Higher system reliability
- Design security
- Shorter time to market
- Increased functionality

It is these benefits that have helped fuel the ASIC explosion.

Looking at the ASIC life cycle, while gate arrays themselves are not at a specific point on the life cycle curve, the various process and technology levels tend to follow the movement of the curve. Of all the ASIC product families, it is gate arrays that are having the most pervasive impact on the electronic equipment industry. The Cell-Based Design segment of ASIC is expected to grow steadily through to the end of the decade. But growth will be dependent upon the further evolution of gate arrays, which are competing with cell-based designs as a result of increased performance from technology improvements. CMOS is the predominant process technology in cell-based designs, with average gate delays of 3ns or 5ns with typical toggle frequencies of 20 MHz to 50 MHz. The geometry trend is from 3 microns down to about 1.5 to 1 micron. The keys to the long-term acceptance of these products are the design tools and development software that are still emerging. Electronic design automation (EDA) tools play a very important role in making the growing cell library functionality readily usable. As an alternative design solution, programmable logic has already replaced standard logic in many applications, overlapping the very low gate count end of gate arrays. Functionality and pure speed are the two key issues with PLDs. Some of the newer products offer tremendous functionality but may not have quite the speed required for throughput-intensive applications. We expect to see the newer CMOS PLD designs reach typical bipolar propagation delays while ECL products will maintain the edge in ultimate operating speed.

In Europe in 1985 the ASIC sector grew substantially despite the industry downturn. While total standard logic declined by 22.2 percent compared to 1984, total ASIC grew by slightly more than 20 percent. We see this high growth rate continuing through into 1986 at a level of 22.5 percent. The largest portion of the ASIC market in 1986 will be full custom, and by that I mean hand-crafted, with a value of $279 million. The gate array market, the second-largest sector of the ASIC arena at $219 million, will be nearly four times larger than the standard cell market.

The situation is expected to change significantly by 1991. We expect the ASIC market to grow at a CAGR of 28 percent to the point where it will represent nearly 22 percent of the total integrated circuit market. By that time gate array products will become the dominant portion of the market despite the high growth rate of standard cells. As one would expect, the hand-crafted sector will decline in proportion as design resource is placed more and more in the hands of the user. This slide shows the individual dynamics year on year within the growth trends.

Looking at the regional breakdown for ASIC in Europe, it can be seen that the United Kingdom and Eire represent the largest market in 1986 although by 1991 we expect West Germany, with its slightly higher CAGR of 28.8 percent, to overtake the United Kingdom and Eire.

Slightly higher growth than the market average is expected in Italy, Scandinavia, and Benelux as major users take advantage of the proliferation of design resources, and as the trend towards design center implants continues.

The lack of substantial design center resources in France and the ROE countries, we believe, is likely to impact the growth in these respective markets and we are therefore projecting a slightly lower than average growth in these regions.

The ASIC end-use breakdown looks slightly different than that for total semiconductor but is still balanced on the four major market segments and therefore offers the same level of stability. We expect the telecommunications segment to grow at a slightly higher rate than the market and by 1991 to represent a market size of $481 million.

The industrial sector is projected to grow at a slightly lower rate than the total market and this we feel is primarily due to the high degree of fragmentation that exists and the large number of small users. But this in itself has brought about a new opportunity--Quick ASIC.

As one would expect, high growth rates will be experienced in the automotive and military sectors, although from a small base in absolute terms, while we expect the consumer sector to follow the pattern of declining market share.

I stated earlier that gate arrays were having the most pervasive impact on the electronic equipment industry and that by 1991 they will be the dominant product of the ASIC categories. I would therefore like to spend a little more time discussing in more detail the trends in gate arrays and their interrelationship with standard cell.

Why is the gate array market larger than any other sector of the ASIC market, other than full custom? And why will gate arrays eventually become the largest sector?

Gate arrays are cost effective in sweeping up numerous standard logic functions onto a single chip. In 1985 it was estimated that the majority of the revenue in CMOS gate arrays was derived from devices with less than 2,500 gates, being driven by gate arrays replacing standard logic.

On a worldwide basis, Dataquest is currently tracking more than 67 CMOS gate array suppliers that offer these low gate count devices. In Europe in 1985, of the top 15 CMOS gate array manufacturers, nine were European; six of them in the top ten. It is interesting to note that the combined revenue of the three Japanese companies in the top 15 was still less than that achieved by the market leader LSI Logic. We believe, however, that in 1986 the Japanese companies will become far more active, pursuing this rapidly growing market. It is these Japanese companies that have experienced the highest growth rates in the market sector in the past two years.

With the large vendor base growing with new market entrants, all with comparable products, there have been considerable price erosions. These price erosions have been more dramatic in Europe as pricing pressure from Japanese market entrants has severely impacted pricing levels on a per-gate basis seen two years ago. The most popular gate array, a 3-micron, 2,000-gate CMOS device in a plastic package, in quantities of 5,000 to 10,000 pieces, took a sharp price-per-gate drop from between $0.010 and $0.012 in 1984, to between $0.002 and $0.004 in 1985. This decline in pricing is still occurring and has increased signficantly the cost effectiveness of gate arrays at the expense of cell-based ICs. Present pricing trends by technology and gate count are shown here for the three major CMOS gate array technologies.

Between the two volume CMOS technologies (3- and 2-micron), the price-per-gate crossover point is 2,000 gates. As the more efficient 2-micron process comes down the experience curve, the gate count for this crossover point will continually decline. Due to the scarcity of volume manufacturers and its state-of-the-art nature, the 1.5-micron CMOS cost per gate currently commands a premium price. But, as the process matures, its speed and density attributes will become more affordable. The crossover points for the relative process technologies can be seen here. The latest European CMOS gate array market estimates by geometry size indicate that already the 3.5- and 3.0-micron process technologies are in decline and that in 1987, the 2- and 2.5 micron products will dominate. This dominance will, however, be short-lived as what is clearly seen as the most cost- and performance-effective process technology, 1.5-micron, takes over in 1988. Clearly, any new market entrants must demonstrate the capability of providing this process technology today if they are to become accepted and achieve design captures now for production volumes in the 1987 to 1988 timeframe.

Nonrecurring engineering charges for cell-based ICs are inherently more expensive than those for gate arrays. Since cell-based ICs are customized using a full set of masks, average NRE charges range from $60,000 to $250,000, including 12 to 14 masks at between $4,000 to $6,000 per mask, plus computer time. Gate arrays are customized using only the final layers for interconnect, so the NRE charges are much less, in the range of $20,000 to $80,000. The role of NRE charges as a market indicator are noteworthy. In 1985, the total NRE gate array revenue grew 44.4 percent compared to the $47.2 million base in 1984. The MOS NRE revenue increased to a dramatic 54.1 percent, while bipolar NRE revenue was more modest at 29.7 percent. An important measurement in determining design captures is the average NRE charge per design. Despite better CAD tools and the users' increased capabilities, the average NRE charge per design is increasing due to the increasing complexity per design. While per design charges have increased, better performance of the CAD tools and experience curve cost reductions have lowered the average NRE per gate. Thus the cost of designing a given array over time has dropped, increasing their overall cost effectiveness. NRE as a percentage of total gate array revenue is decreasing and we expect it to continue to do so. The MOS NRE as a percent of total MOS

gate array revenue is declining 1 percent to 2 percent per year and is expected to stabilize at 20 percent in seven to ten years, when market maturity is reached. The bipolar market, however, appears to have reached maturity and is holding constant with 20 percent NRE.

The preceding gate array advantages of competitive pricing, low NRE charges, coupled with user-friendly software and fast turnaround times, have pushed cell-based IC suppliers to compete with higher gate count devices and in higher production volumes.

In 1985 in Europe, the number one supplier of cell-based ICs was VTI with revenue two and a half times greater than the nearest competitor Zymos. Of the top 15 shown here, the U.S. companies dominate but particularly interesting is the almost complete absence of Japanese manufacturers. The indicators are, however, that this situation is likely to be short lived. Over the past few months we have seen a spate of activity from Japanese vendors in the introduction of megacells and design automation systems, particularly from companies such as Fujitsu, Matsushita, Mitsubishi, and NEC.

In the early 1980s, cell-based ICs were more economic than gate arrays when production volumes reached 8,000 to 10,000 units a year. Today, the crossover point is very dependent upon gate count and device functionality. If unit production volumes are less than 15,000 units a year, gate arrays will undoubtedly capture the design. This slide shows the current relationship between unit volume and gate count for each of the ASIC design methodologies.

In 1986, the total number of design captures for standard cell and gate array combined is expected to reach 2,479. Of this, 85.7 percent, or 2,125, is anticipated to be for gate arrays. Within this, 1,026 design starts are expected to be for CMOS gate arrays with greater than 1,000 gates.

By 1990, the number of design captures is expected to grow at a CAGR of 38.5 percent to a combined gate array and standard cell total of 9,126, of which 4,572, slightly more than half, will be for CMOS gate arrays with greater than 1,000 gates. This represents a CAGR of 45.3 percent in this time frame. In contrast, standard cell design captures for products with greater than 1,000 equivalent gates are expected to grow from 196 in 1986 to 1,387 in 1990, a CAGR of 63.0 percent and a higher growth rate than gate arrays. Clearly, not all of the design captures will enter production. Our analysis of designs captured in 1985 have shown that on average it takes six months to one year for a device to reach the production phase. The percentage of designs that ultimately reach the production phase vary widely, ranging from 40 percent in a depressed semiconductor economy to slightly more than 70 percent in a thriving semiconductor economy. One clear reason for the rising number of design starts is the decreasing end equipment product life cycles, from the average of four to five years seen in the early 1980s to the current average of three to four years.

Another aspect that has influenced, and is a fundamental requirement of, the ASIC sector is the establishment of design resource. In May 1986, there were 91 fully operational merchant design centers spread across Europe. Of these, 46 had been established by U.S. semiconductor companies, 27 by indigenous European semiconductor companies, and 18 by semiconductor companies from Japan. The trend we see in the short term is for more and more design centers to be established and for Japanese semiconductor manufacturers in particular to establish the majority of these new centers in the next 12 to 18 months.

The regional split in Europe of these design centers effectively supports the regional ASIC consumption split shown earlier, the greatest concentration of design centers being in the United Kingdom and Eire, and West Germany.

This analysis, however, does not take into account the growing tendency toward design center implants. The implants arise from strategic agreements between semiconductor manufacturers and users, effectively providing for the user a captive facility and for the vendor an almost captive source of revenue.

The design centers that exist today and for the short to medium term are only an interim solution to the continuing need to provide design resources and tools. In the long term, the objective of the ASIC vendors must be to provide every design engineer with the best possible design tools. Then and only then will the ASIC explosion occur. It will occur when silicon compilation really comes of age.

True silicon compilation provides the major benefits of:

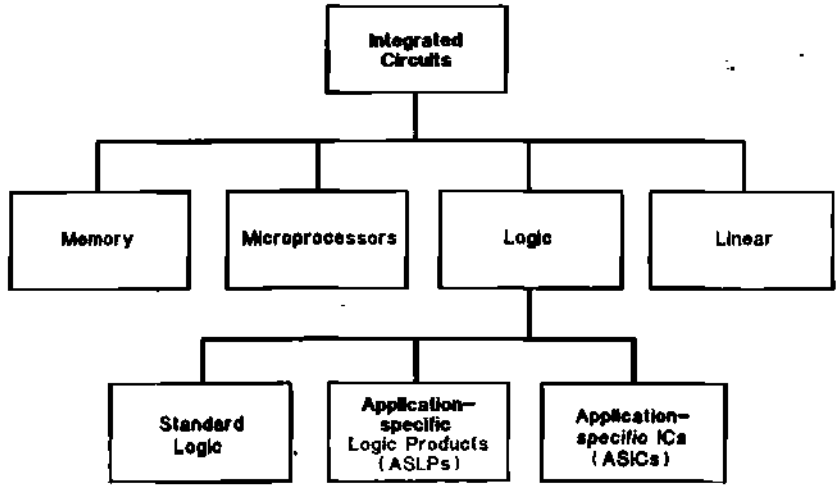
- Reduced design turnaround and cost compared with other methodologies, by-passing the time-intensive and error-prone schematic entry phase
- A complete integrated design solution
- Greater design exploration and creativity by freeing system or non-IC design engineers from the time constraints of schematic entry
- Enforcing standard design practices be they generalized or highly specific
- Provision of fully automated layout

The overriding advantage that silicon compilation has over the present design methodologies is that it provides a shared method of satisfying the design demands of both system engineers and IC designers, providing the means of communicating IC design methodology in terms understood by each class of user. This then will allow the user to choose the

appropriate design methodology on a per design, rather than on a per workstation, basis. We are not expecting widespread user acceptance of silicon compilation until the end of this decade. IC suppliers, silicon compiler companies, and workstation vendors are all trying to position themselves for long-term lucrative growth, each experimenting with a variety of silicon compiler products and marketing strategies, in the race for single-chip system solutions.

What is apparent today is the trend towards specialized compilable cells. Today, device complexity and functionality are far ahead of the designers' abilities to find applications. For example, what are the appliations for a 50,000-gate array? It is the vendor of such a product that must provide the insight to answer this question. We believe that anticipating these future applications and directing the use of IC design tools and ASIC products in the end-use markets will be critical in determining success. The right alliances between compiler companies, ASIC manufacturers, and users will make the difference between the leaders and the followers.

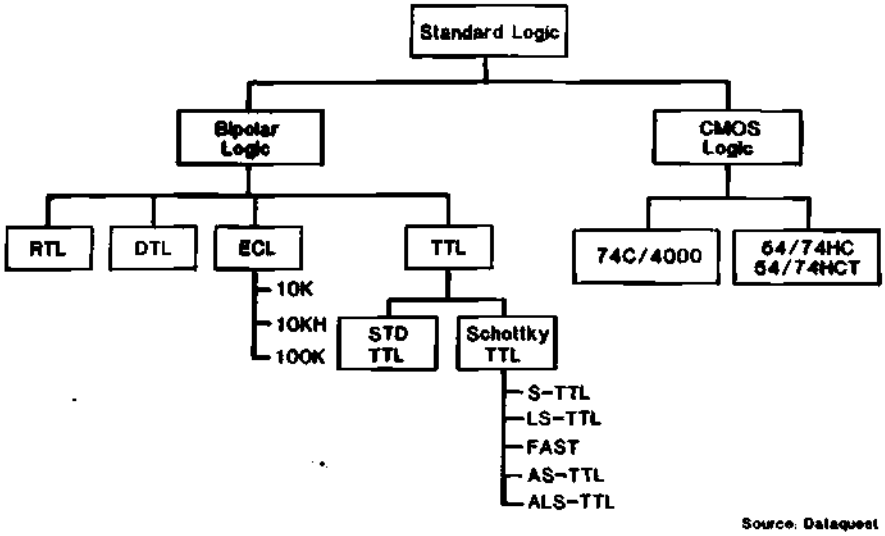
INTEGRATED CIRCUIT FAMILY TREE



Source: Dataquest

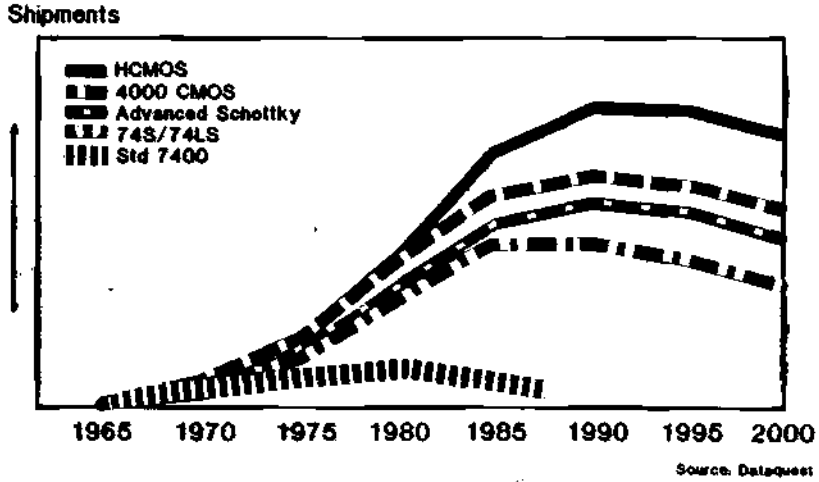
STANDARD LOGIC

STANDARD LOGIC FAMILY TREE



Source: Dataquest

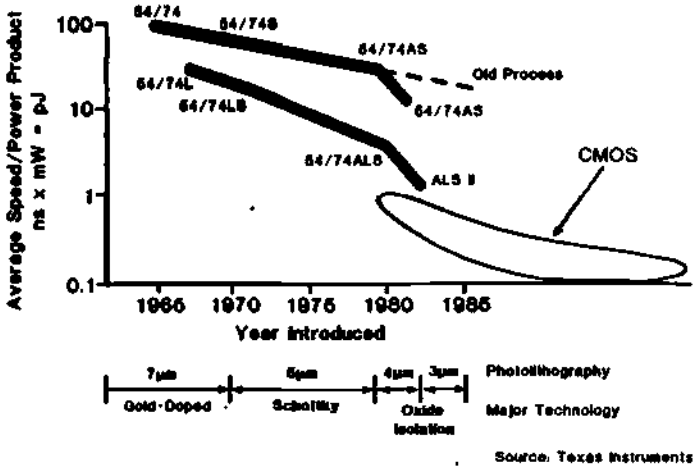
ESTIMATED
STANDARD LOGIC LIFE CYCLE



Source: Dataquest

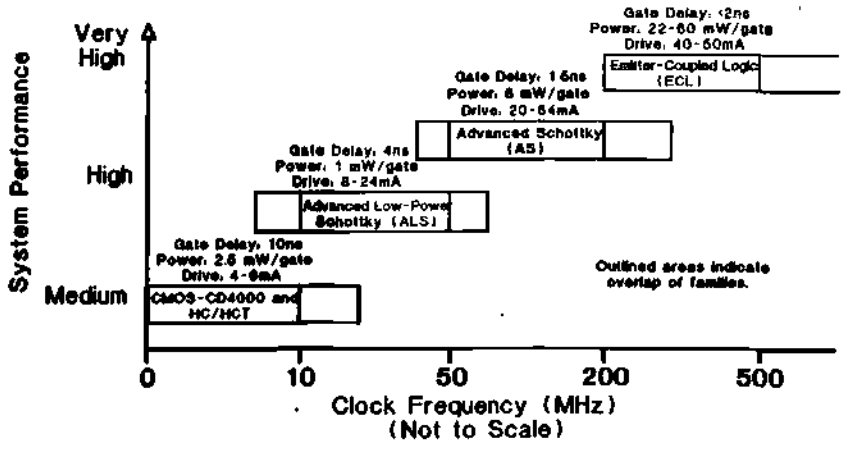
SPEED/POWER PRODUCT OF TTL AND CMOS STANDARD LOGIC

(1965–1985 and Beyond)



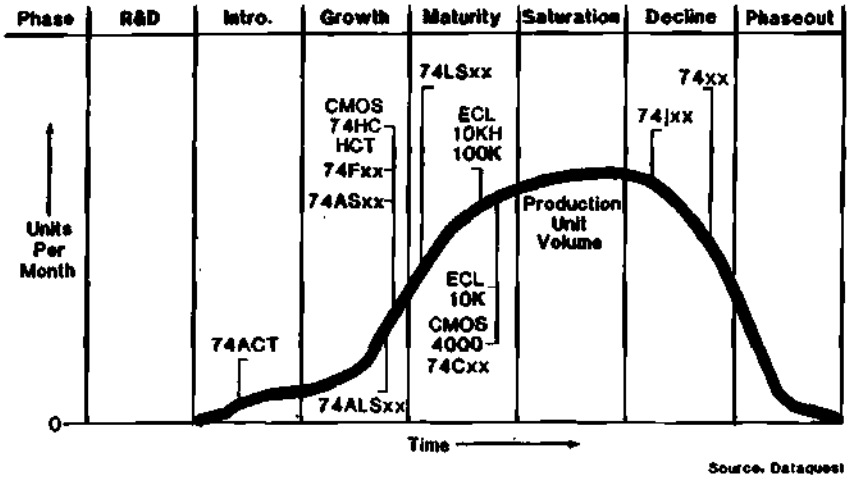
Source: Texas Instruments

STANDARD LOGIC COMPONENTS SPECTRUM OF USE BASED ON SYSTEM PERFORMANCE AND FREQUENCY



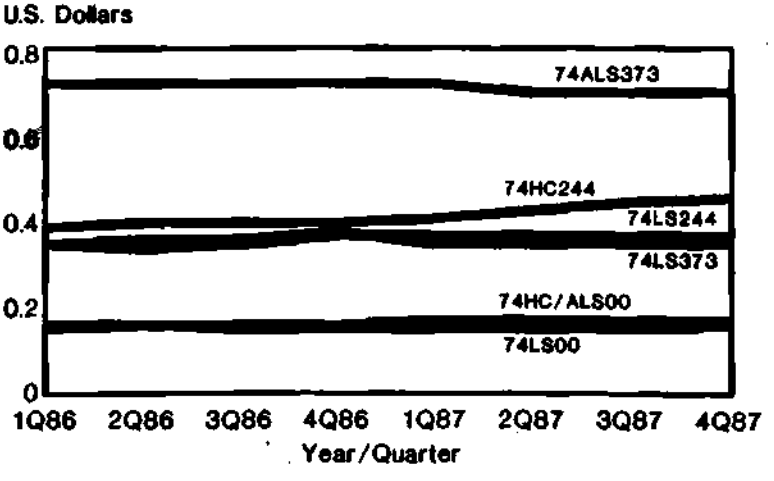
Source: Dataquest

TTL SHIPMENTS
SSI/MSI STANDARD LOGIC LIFE CYCLE



Source: Dataquest

ESTIMATED AVERAGE PRICE TRENDS

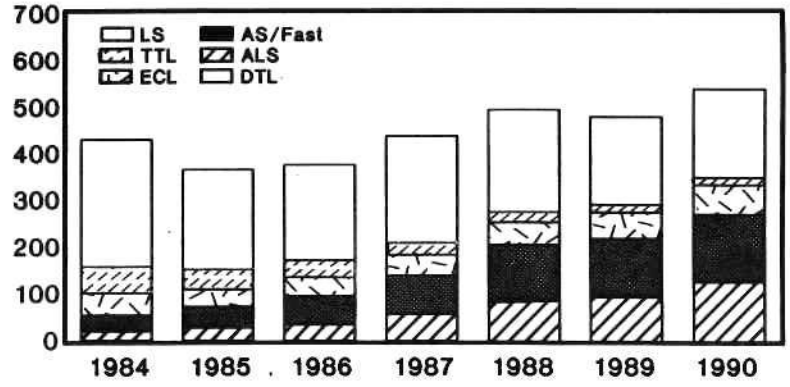


Source: Dataquest

ESTIMATED EUROPEAN CONSUMPTION

Bipolar Standard Logic

Millions of U.S. Dollars

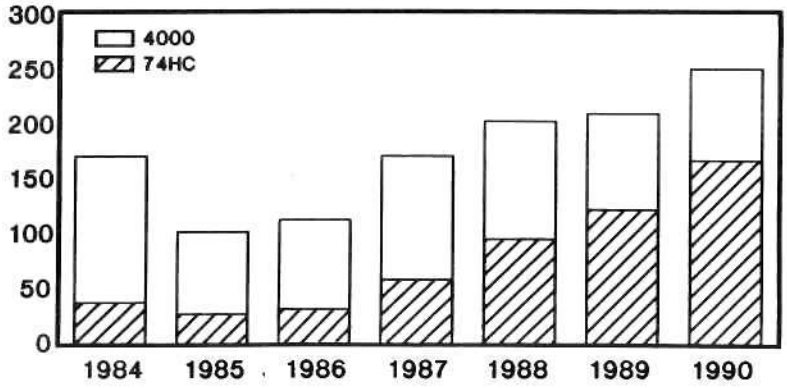


Source: Dataquest

ESTIMATED EUROPEAN CONSUMPTION

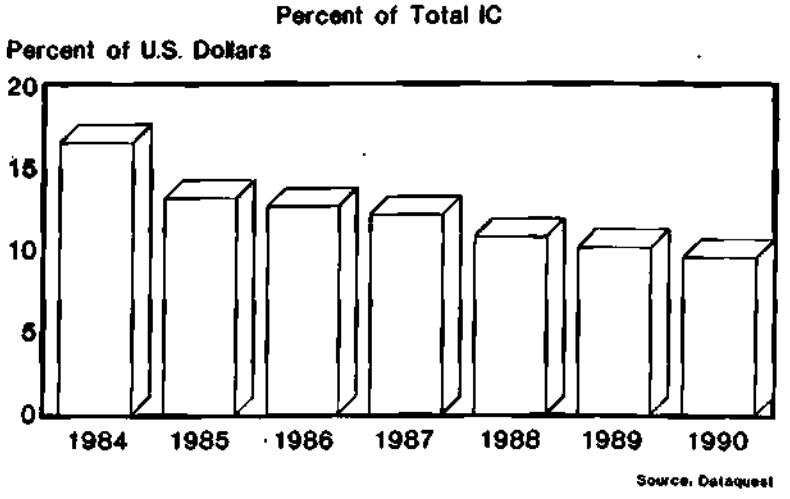
CMOS Standard Logic

Millions of U.S. Dollars

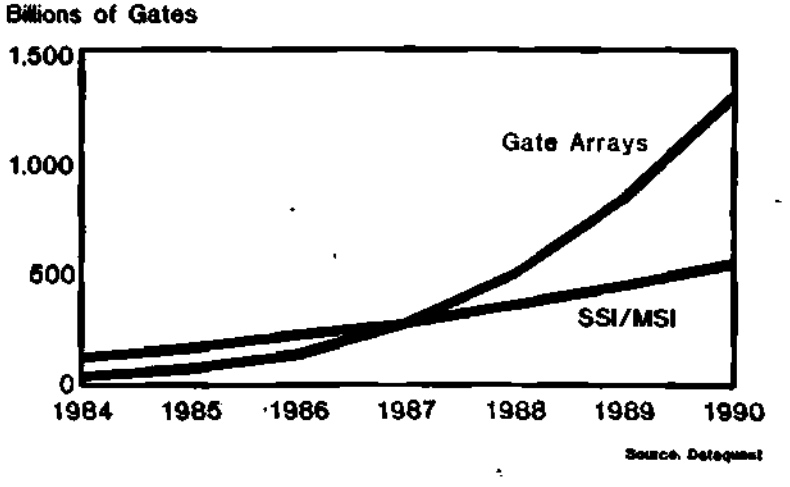


Source: Dataquest

ESTIMATED EUROPEAN CONSUMPTION

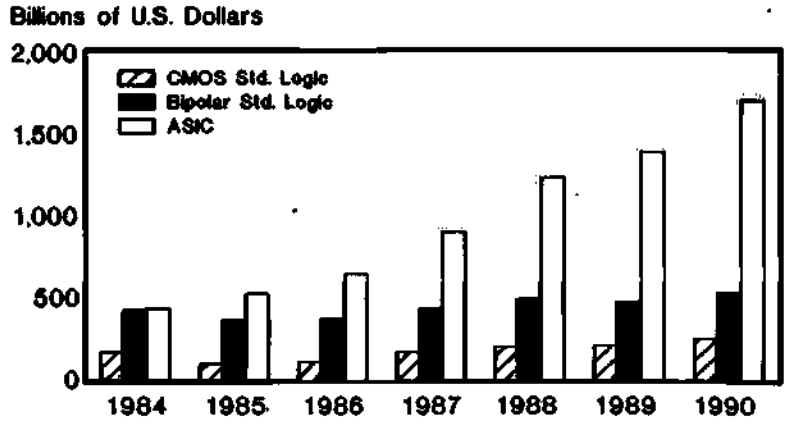


EXPECTED IMPACT OF GATE ARRAYS ON SEMICONDUCTOR LOGIC FUNCTION SHIPMENTS



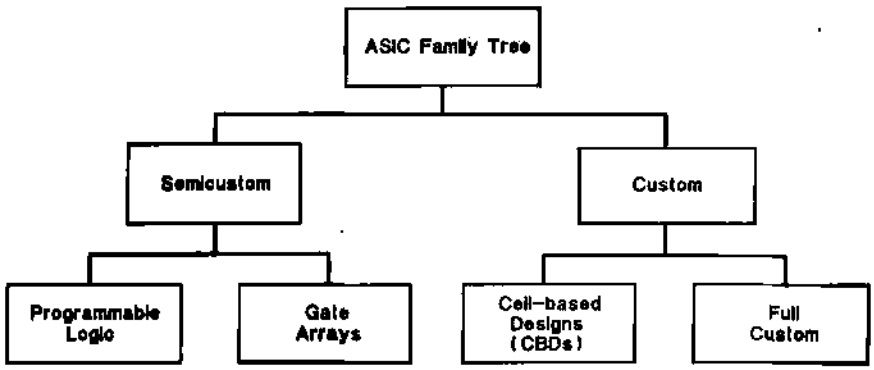
ESTIMATED EUROPEAN CONSUMPTION

Standard Logic and ASICs



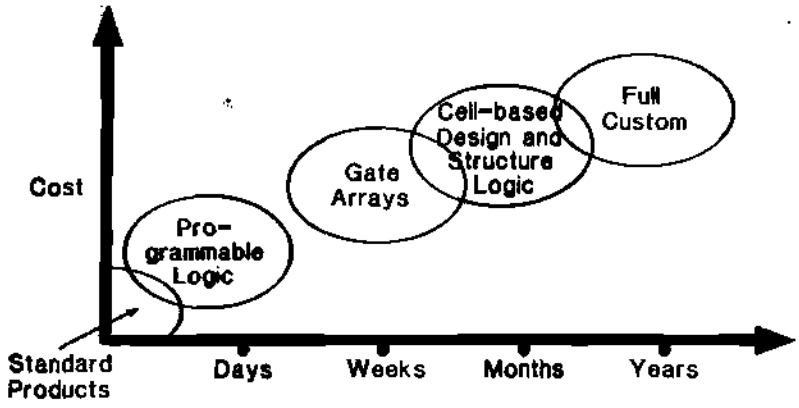
Source: Dataquest

ASIC FAMILY TREE



Source: Dataquest

IMPLEMENTATION ALTERNATIVES

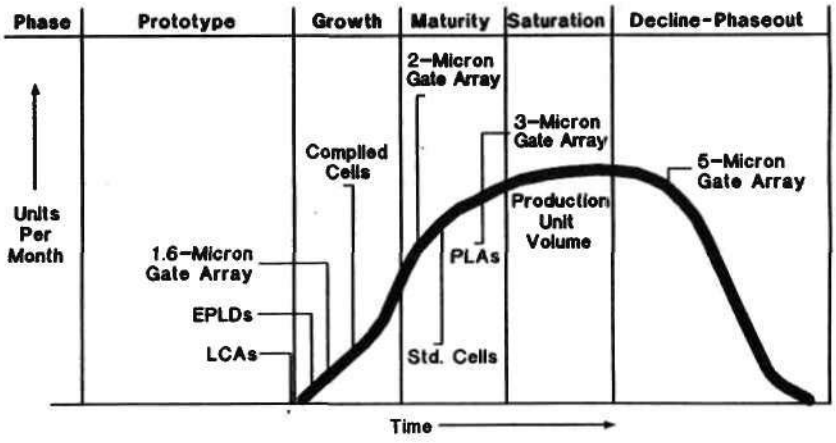


Source: Dataquest

APPLICATION-SPECIFIC ICs

- Manufacturing cost
- Power consumption
- System size
- System reliability
- Security
- Time to market
- Functionality

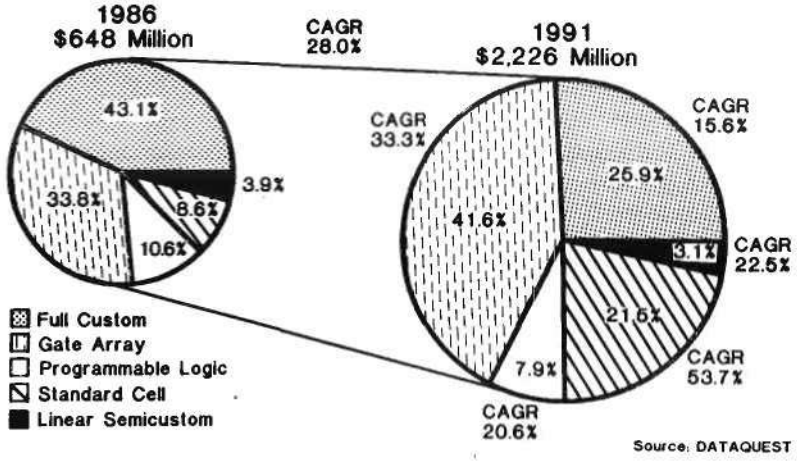
APPLICATION-SPECIFIC INTEGRATED CIRCUIT LIFE CYCLE



Source: Dataquest

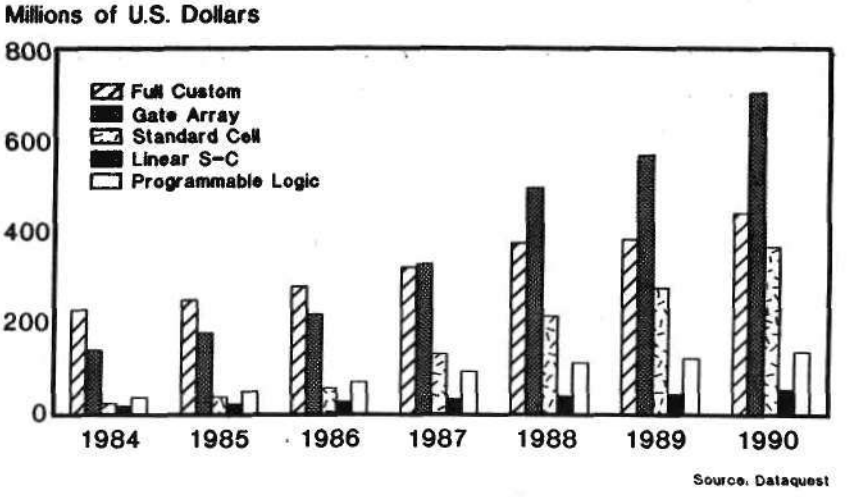
ESTIMATED EUROPEAN ASIC CONSUMPTION

(Percent U.S. Dollars)

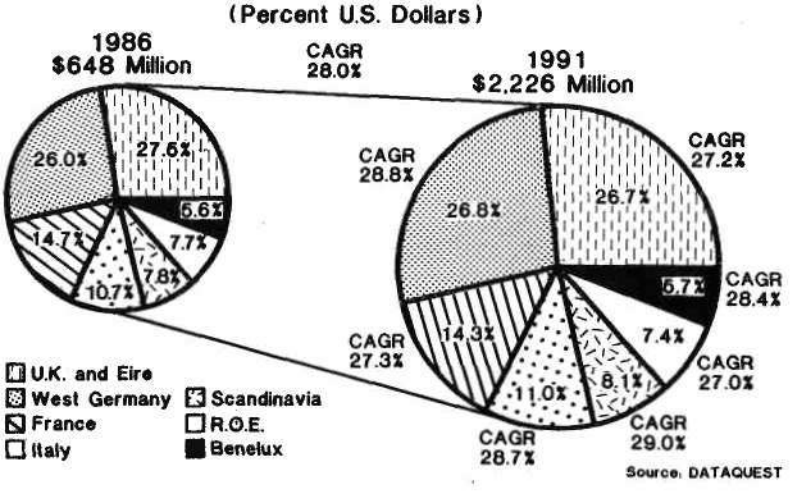


Source: DATAQUEST

ESTIMATED EUROPEAN ASIC CONSUMPTION

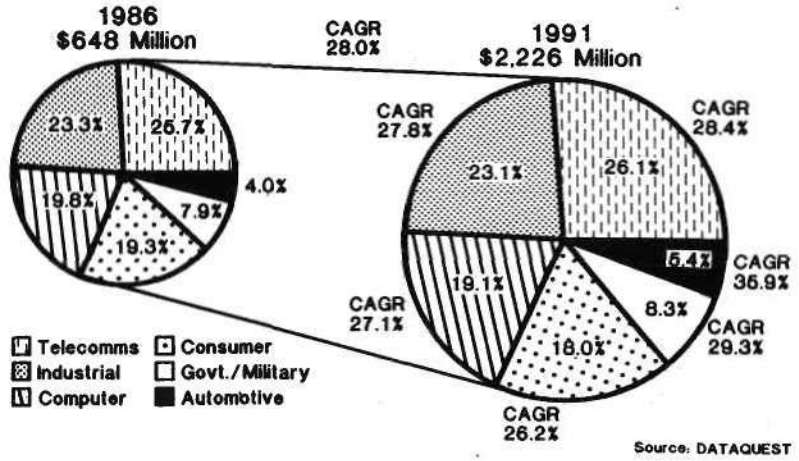


ESTIMATED EUROPEAN ASIC CONSUMPTION - BY REGION



ESTIMATED EUROPEAN ASIC CONSUMPTION - BY END USE

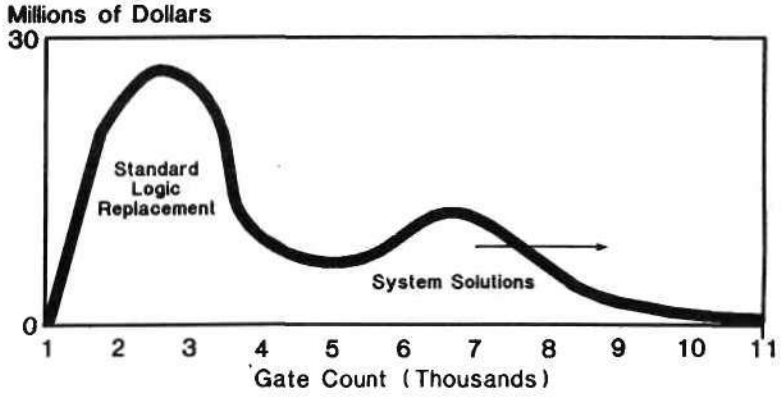
(Percent U.S. Dollars)



Source: DATAQUEST

ESTIMATED EUROPEAN 1985 CMOS GATE ARRAY CONSUMPTION

(Revenue by Gate Count)



Source: Dataquest

EUROPEAN MOS GATE ARRAY
MARKET SHARE ESTIMATES - TOP FIFTEEN

(Millions of U.S. Dollars)

Rank	Company	1984	1985	Growth %
1	LSI Logic	8.4	12.5	48.8
2	Thomson	7.2	8.6	19.4
3	Plessey	5.2	6.9	32.7
4	Nat. Semi.	4.0	6.8	70.0
5	Medl	5.0	5.5	10.0
6	Smiths	4.0	5.4	35.0
7	SGS	3.7	5.1	37.8
8	Philips	2.4	5.0	108.3

(Continued)

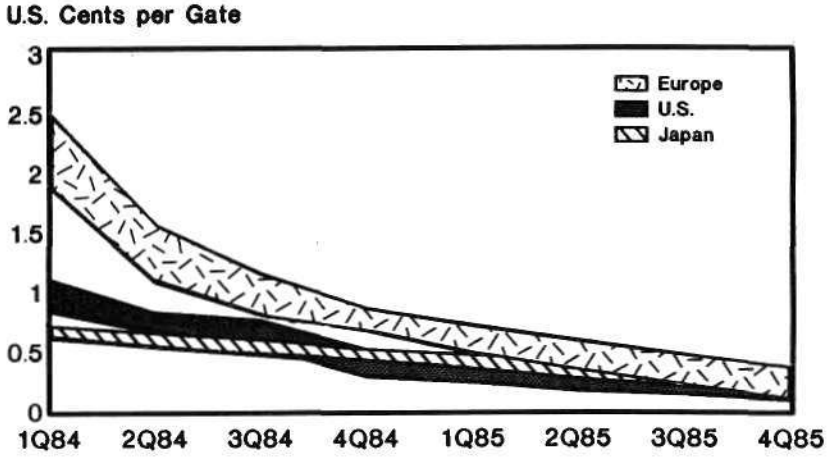
EUROPEAN MOS GATE ARRAY
MARKET SHARE ESTIMATES - TOP FIFTEEN

(Millions of U.S. Dollars)

Rank	Company	1984	1985	Growth %
9	Fujitsu	2.4	4.9	104.2
10	RCA	3.3	4.5	36.4
11	Matra-Harris	3.0	3.7	23.3
12	MCE	3.0	3.3	10.0
13	NEC	2.1	3.0	42.9
14	Hitachi	1.9	2.9	52.6
15	Racal	2.0	2.5	25.0

Source: Dataquest

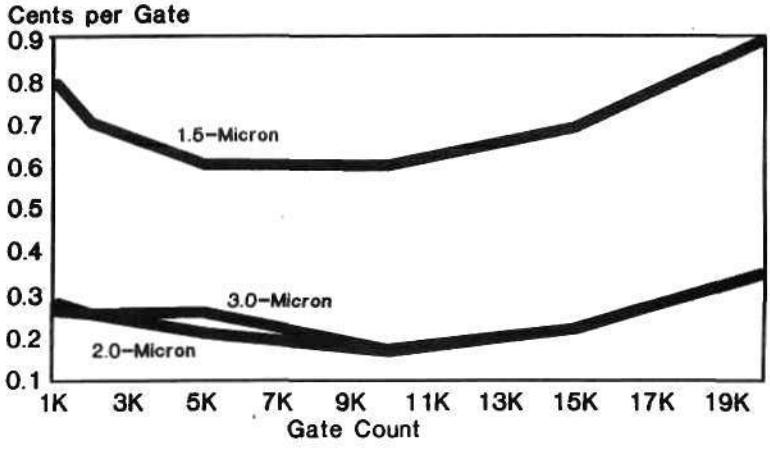
CMOS GATE ARRAY PRICE TRENDS



Source: Dataquest

CMOS GATE ARRAY PRICE PER GATE

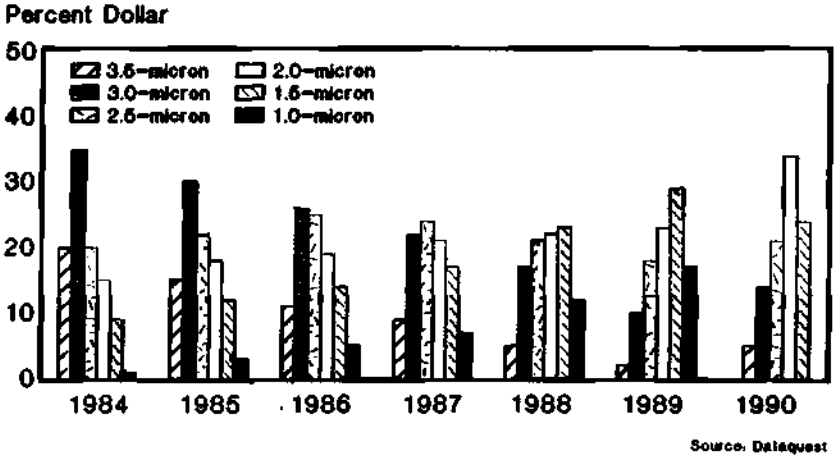
By Technology



Source: Dataquest

EUROPEAN GATE ARRAY MARKET ESTIMATES

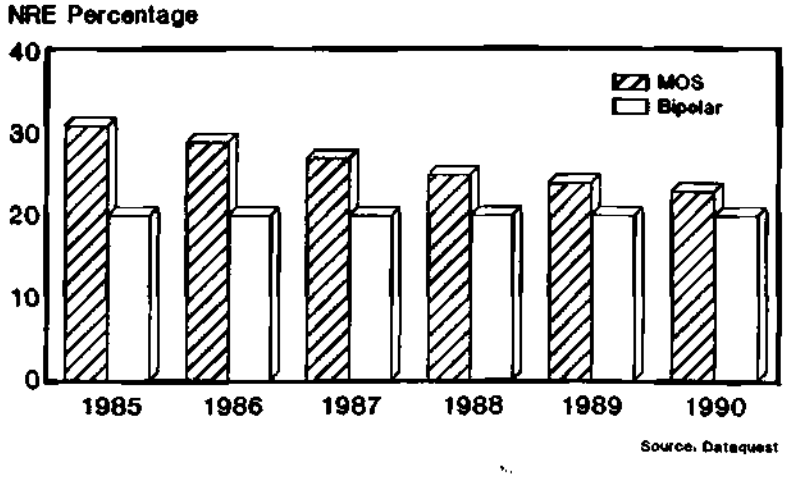
CMOS - By Geometry Size



Source: Dataquest

ESTIMATED EUROPEAN NRE REVENUE

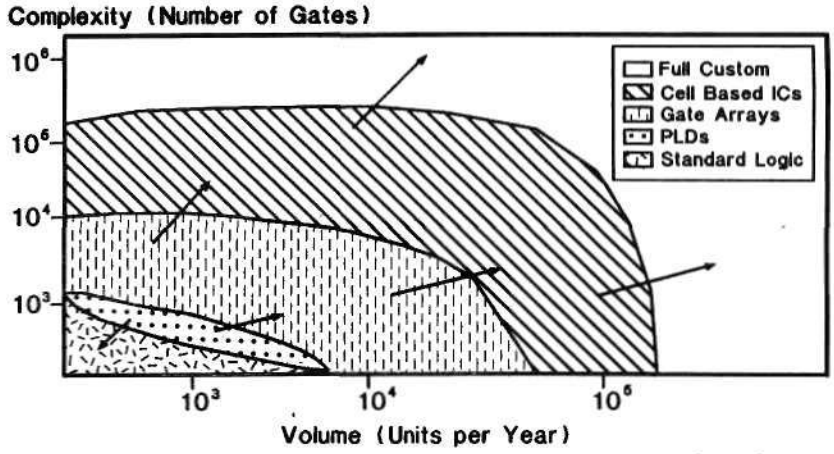
Percent of Gate Array Revenue



Source: Dataquest

ESTIMATED 1985 ASIC PRODUCTION VOLUME

Units by Gate Count



Source: Dataquest

EUROPEAN MOS STANDARD CELL MARKET SHARE ESTIMATES - TOP FIFTEEN

(Millions of U.S. Dollars)

Rank	Company	1984	1985	Growth %
1	VLSI Technology	4.2	10.5	150.0
2	Zymos	3.2	4.2	31.3
3	IMP	2.6	3.3	26.9
4	Thomson	1.8	2.4	33.3
5	Medl	1.3	1.9	46.2
6	AMI	1.3	1.8	38.5
7	Texas Inst.	1.4	1.7	21.4
8	RCA	1.2	1.6	33.3

(Continued)

EUROPEAN MOS STANDARD CELL MARKET SHARE ESTIMATES - TOP FIFTEEN

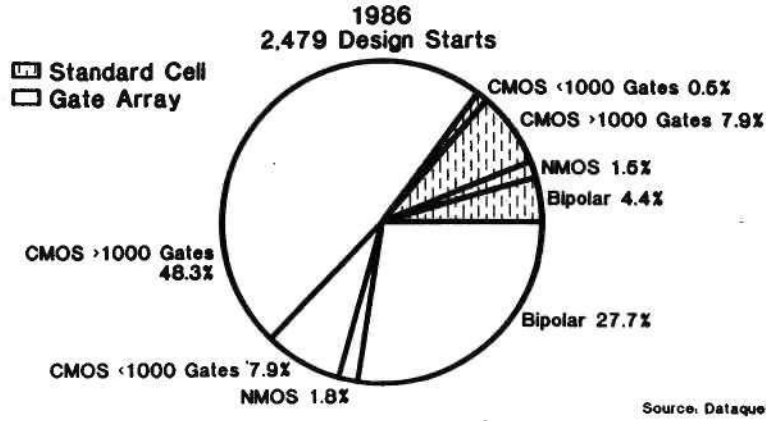
(Millions of U.S. Dollars)

Rank	Company	1984	1985	Growth %
9	SGS	0.9	1.2	33.3
10	Fujitsu	0.7	1.1	57.1
11	Siemens	0.4	1.1	175.0
12	Nat. Semi.	0.8	1.1	37.5
13	NCR	0.4	0.6	50.0
14	Plessey	0.3	0.6	100.0
15	Motorola	0.3	0.5	66.7

Source: Dataquest

ESTIMATED EUROPEAN APPLICATION-SPECIFIC IC DESIGN STARTS

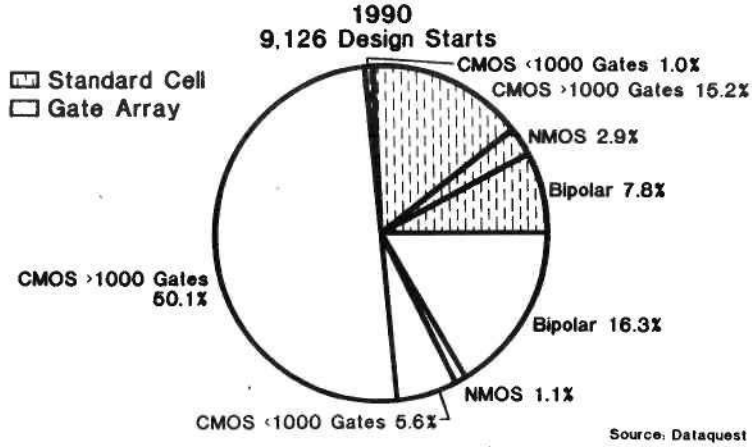
Standard Cell and Gate Array



Source: Dataquest

ESTIMATED EUROPEAN APPLICATION-SPECIFIC IC DESIGN STARTS

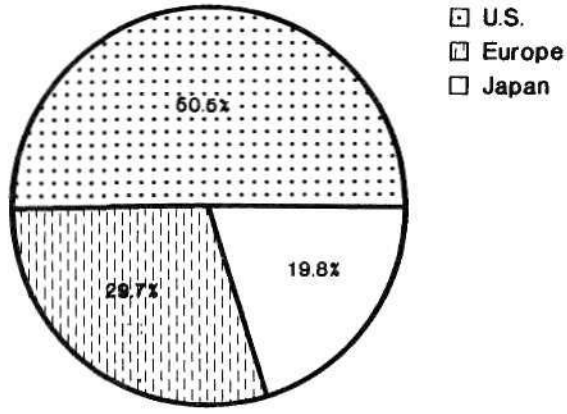
Standard Cell and Gate Array



Source: Dataquest

ESTIMATED GATE ARRAY DESIGN CENTERS

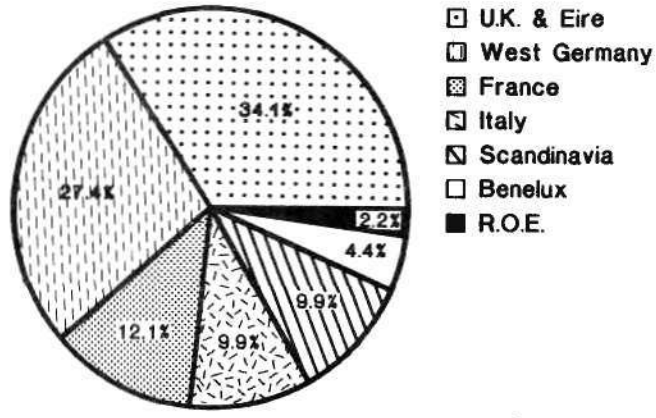
Merchant - 1986 - By Vendor Source



Source: Dataquest

EUROPEAN GATE ARRAY DESIGN CENTERS

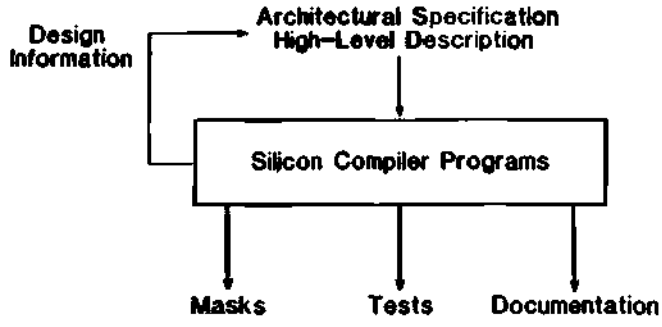
Merchant - 1986 - By Region



Source: Dataquest

APPLICATION-SPECIFIC ICs

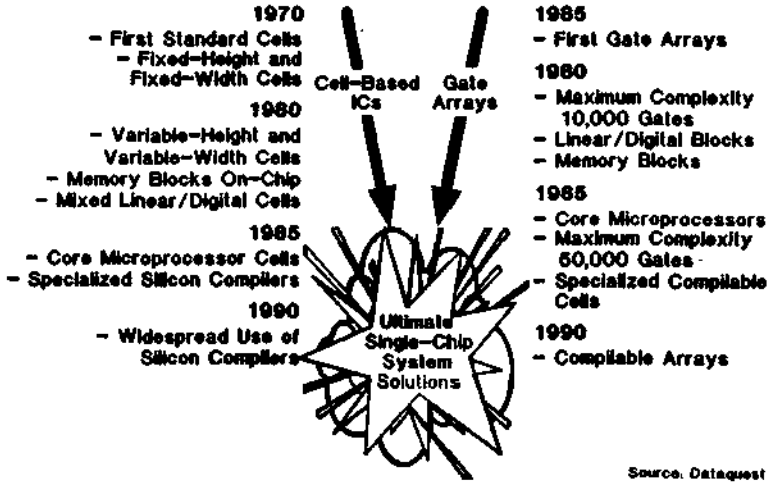
True Silicon Compilation



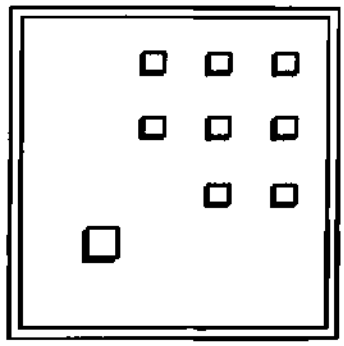
Source: Dataquest

APPLICATION-SPECIFIC ICs

The Race for Single-chip System Solutions



Source: Dataquest



Dataquest
IC Outlook '87

September 15–23, 1986

MEMORY AND MICROPROCESSOR UPDATE

JIM BEVERIDGE
Dataquest UK Limited

Good morning ladies and gentlemen, and welcome to the MOS sector of today's seminar. Before I start, let me very briefly give you an overview of the sections I shall be covering during today's session.

The presentation is divided into two sections: MOS Memories and MOS Microcomponents.

(Slide 2)

Within the memory portion, I will be dealing with the overall market situation, the current discussion on U.S.-Japan trade issues, dynamic RAMs, static RAMs, and nonvolatile memories. During the microcomponent market overview, I will consider microprocessors, microcomponents, and microperipherals, as well as the digital signal processing marketplace.

(Slide 3)

The worldwide MOS memory market declined by an estimated 39 percent from 1984 to 1985, dropping from $6.53 billion to $3.97 billion. This slide gives details of the revenue drop by product category. Demand stagnation and severe price erosion in the DRAM market resulted in a reduction in revenue by more than 50 percent, the greatest decline among any major MOS memory product area. Slow SRAMs suffered much the same fate, dropping by 36 percent as a result of a supply-demand imbalance. This was made worse by the failure of the portable computer market to materialize as expected. Fast SRAMs fared much better, increasing by 3 percent due to both a steadiness in demand from a more stable user base and to the emergence of newer 64K devices. The EPROM market dropped an estimated 26 percent from 1984 to 1985, with the most severe price competition coming in the second half of the year. The mask ROM market declined by 28 percent, but the fall was cushioned by the emergence of the modest video games business in Japan in the second half of the year. The market for EPROMs combined with NVRAMs was only down 7 percent to $135 million, although price declines were severe.

(Slide 4)

Since its inception in about 1970, MOS memory market growth has been truly outstanding. Over the last 15 years, the bit growth rate shown in this slide has averaged nearly 100 percent per year. This means that in any given year, as many memory bits were shipped as were shipped in the entire previous history of the product. The market has been driven by products like home and personal computers, mainframe and mini computers, a little splash in video games in the United States in 1981 and 1982, and a little bit in Japan in the last year or so. All of these contributed to a growth of about 100 percent per year. In 1985, the total MOS memory bits shipped were about 145×10^{12}, so it is a pretty phenomenal achievement from a dead start 15 years ago. Even in the disaster year of 1985, bits shipped exceeded those shipped in 1984 by about 40 percent, which was the lowest growth that the market had experienced in all of

these 15 years. No manufactured item has ever experienced a growth rate sustained over such a long period of time as MOS memory bits have. Standing and looking from the vantage point of a couple of recessions ago in 1975, I suspect that few could have imagined that we would be shipping 1,000 times as many bits a decade later and that market revenue would be 15 times larger.

(Slide 5)

Looking out for the next decade, Dataquest believes that the outlook is no less outstanding from both a bit growth and bits shipped level; for the rest of the decade we can look at an annual bit growth rate of around 80 percent or perhaps a little more. In the first half of the decade of the 90s, we are looking at somewhere in the 50 to 60 percent growth rate year to year. Some of the markets that we expect to be the key drivers during this next decade are bit map graphics that show up on digital TVs, video recorders, imaging applications, and signal processing applications. We expect to see another wave of personal computers and equipment for office automation applications, IC cards, and applications in simulation. All of this on top of the basic core amount into mainframes, minicomputers, and business computers. In certain applications today, the cost of semiconductor memory compares favorably with magnetic media, which could in turn open up a market that is 100 times bigger in terms of total bits than the semiconductor memory market is today.

Turning now to trade issues.

(Slides 6/7)

This slide demonstrates the worldwide MOS memory market shares by home base of producer. U.S. manufacturers' revenue declined by 46 percent and Japanese manufacturers, despite their strong presence in the commodity static dynamic DRAM and EPROM markets, declined by 35 percent. Asia Pacific companies--Korea, Taiwan, and Hong Kong--managed to increase their revenue by 50 percent over their small 1984 bases.

(Slide 8)

This slide represents the MOS memory market shares by home base of producer as a percentage of the worldwide marketplace. Clearly it demonstrates how Japan now has the premier position in the MOS memory marketplace. Japan's steady worldwide gain in market share is the basis of its present dispute with the United States. American companies claim that Japanese manufacturers have been dumping products, i.e., selling products below cost in the domestic marketplace, and at the same time they feel that they have been excluded from the fast-growing Japanese home market.

(Slide 9)

The situation was brought to a head during 1985 when the marketplace dramatically declined and heavy losses were reported by the majority of companies in the volume memory marketplace. The following companies--Mostek, Inmos, National Semiconductor, Motorola, and Intel--withdrew from the DRAM marketplace, and UTC closed down its Mostek subsidiary, the assets being sold to Thomson. The North American multinationals reacted, bringing dumping allegations against Japanese companies. After many months of investigation, the U.S. Department of Commerce found Japanese suppliers of EPROMs and 256K DRAMs guilty of price dumping.

(Slide 10)

These margins represent the percentage by which each company's price was judged to have undercut its fully loaded cost of manufacturing plus an 8 percent profit margin. Effective from March 13, 1986, some makers of EPROMs and 256K DRAMs were required to post bonds to cover dumping duties on all EPROMs and 256K DRAMs imported from Japan. The 64K DRAM penalties that were decided on December 9, 1985, as well as general economic trends, have already impacted the current 64K DRAM ASPs at the beginning of the year. Current agreement between Japanese and American companies means that the bonds posted have now been refunded; however, the actual duty has only been suspended and can be reactivated at any point in the future.

(Slide 11)

The U.S./Japanese agreement covers the following four points:

- Japan agrees to increase the purchase of semiconductors to more than 20 percent of its own marketplace over the next five years.
- Japanese prices will be monitored on an ongoing basis by MITI.
- The U.S. Department of Commerce will check this monitoring by undertaking its own investigation of costs and prices of Japanese chips.
- In return for the increased market penetration, the United States has decided to suspend dumping suits against Japanese companies.

In Europe there is concern on two fronts:

- First, that the increased penetration of the Japanese marketplace by North American companies might be at the expense of the European semicondutor manufacturers.

- Second, there is concern in the European user community that local price increases in memory components will result in our telecommunications and computer end-equipment manufacturers suffering a cost disadvantage vis-a-vis their Japanese competitors.

At the time of this writing, the European Economic Community was considering taking action against Japanese companies dumping products within the EEC.

(Slides 12/13)

The combination of economic trends and dumping negotiations raised the overall prices for DRAMs from their third-quarter 1985 low point. The U.S./Japanese agreement has caused the prices of the 64K and 256K DRAMs to stabilize, but the 256K is expected to renew its cost-related price decline by the end of the year. As a point of interest, it should be noted that the 1Mb DRAM prices are included in the 256K dumping suit. As 256K DRAM prices decline, the tradeoff point of the 256K to 1Mb DRAM is now expected to occur no sooner than the second half of 1987. Due to the dollar/yen exchange rate situation and fear of dumping penalties, prices for Japanese parts stay generally higher than prices for the U.S. and Korean products. Current lead times for the DRAMs are 64K--3 to 5 weeks, 256K--4 to 8 weeks, and 1Mb--8 to 12 weeks.

(Slide 14)

When considering the technology used for 256K DRAMs, 96 percent of the designs were in NMOS and 4 percent in CMOS. CMOS was only used when high performance in terms of speed was required. For the 1Mb DRAM, Fujitsu, Mitsubishi, NEC, and Toshiba started with NMOS designs, whereas AT&T, Hitachi, Micro Technology, Mostek, TI, and Vitelic started with CMOS designs. All companies have now announced that they will have CMOS variants by early 1987. CMOS is not only being used for the performance memories such as static column and ripple mode variants, but also for the mainstream page and nibble types. At the time of this writing, 12 companies had announced designs, with AMD, Motorola, Philips, Sanyo, Sharp, and Thomson as possible contenders. Inmos, Intel, Mostek, and National Semiconductor have declined to participate in the marketplace.

(Slide 15)

Almost 2 million units were shipped in the first half of 1986, the majority being supplied by Fujitsu, Hitachi, and Toshiba. AT&T and Texas Instruments were the major North American participants.

(Slide 16)

Finally, we can take a look at some of the characteristics of the DRAM industry. Investment in DRAMs today is very much a rich company's prerogative. There is an extremely high fixed cost associated with it, often running in excess of $100 million per facility. This commitment has to be made years in advance, despite our inability to see exactly what the market is going to look like when the facility comes on-stream. Operating at the leading edge of technology means that the facility is obsolete very rapidly, with typically a three- to five-year life cycle for the equipment. The fixed cost of plant and equipment is a major part of the product cost. This is compounded by the fact that there are inherent instabilities in the way users and vendors currently do business. The contract and forward pricing, the letter of intent which doesn't protect either the user or vendor against price rises or price declines very well, those factors make it difficult to forecast one's business. As we have seen in both the up cycle and the down cycle, if pricing is rising, lead times go out because everyone has to order further in advance. This makes lead times go out more and prices go up more. When on the down side in a market of declining prices, users will stay out of the market hoping for a lower price later on. If, as a result, the demand isn't there, the price is sure to decline until a new equilibrium point is achieved.

(Slide 18)

Here, we are moving on to SRAMs, which have gone through the same recession as DRAMs, although not as seriously. In 1985, the SRAM marketplace declined by 25 percent from $1,203 million to $906 million. Slow SRAMs are much more a commodity product than fast SRAMs. In 1985, the slow SRAM market declined by an estimated 36 percent from 1984 to $541 million. The state-of-the-art products at the 16K and 64K density suffered tremendous price erosion throughout the year, and the 256K devices were not sufficiently close to production to make up the difference. The fast SRAM marketplace grew by $11 million (or 3 percent) from an estimated $354 million in 1984 to $365 million in 1985. Faster SRAMs have a high presence in the military market, which has remained more stable throughout the year. They also tend to be sold into high-end system markets and not into the consumer areas. The market is highly specialized and highly differentiated in terms of density, performance, organization, and special features, thereby offering opportunities for greater price stability.

(Slide 19)

Once again, Japanese companies dominate the fast SRAM marketplace. The major players are Hitachi, NEC, Seiko-Epson, and Toshiba. The North American companies are stronger in the fast marketplace. Companies such as AMD, IDT, and Motorola have a strong presence. Most of the European production is accounted for by Inmos in England, although Matra-Harris, Siemens, STC, and Thomson also participate in this market.

(Slide 20)

This slide shows the position of both slow and fast SRAMs on the life cycle curve. Specialty or secondary types of SRAM devices are emerging, but only for specific applications. These are dual-port devices, resettable SRAMs, and x9 organizations (providing an extra bit for parity). These specialty parts are all CMOS fast SRAMs and will probably have longer life cycles as they cater to particular niche applications. Most early NMOS SRAMs are either in a decline or a phase-out stage; the exceptions would be the fast 2Kx8 part and 4Kx4 part. The NMOS 16Kx1 and CMOS 1K and 4K devices are also declining or being replaced. The CMOS fast 16K (i.e., 4Kx4, 16Kx1, and 2Kx8) are still production workhorses. The slow 16K part (2Kx8) is declining as the CMOS slow 64K part is the mainstream production unit now. The fast reaction of CMOS 64K is building up production volume to be a mainstream part from now through 1988. Though placement at this level will occur in 1988 and 1989 with the 256K as a production mainstay. CMOS slow 256K SRAMs are currently in the early design phase. The CMOS fast 256K part is in the sampling stage and will be ready for system design production in 1987.

(Slide 21)

There are certain important trends that one should take note of in the SRAM marketplace. First, more participants. The marketplace is becoming more and more crowded as the established producers AMD, Fujitsu, Hitachi, Inmos, Intel, Mitsubishi, NEC, and Toshiba are joined by new start-ups or new programs from established producers. Among these companies are Alliance Semiconductor, Cypress, IDT, Lattice Semiconductor, Mosel (Taiwanese company), Motorola, Triad (a new start-up out of Inmos Corporation), Vitelic, and VLSI Technology; and via licensing agreements, MMB Semiconductor, Seiko, Sharp, and Sony. This increased participation is expected to accelerate the price erosion in the marketplace. In addition to this, there is a demand for more complex, faster parts. Manufacturers are operating at the leading edge of the technology and are managing to improve their total kit price by offsetting price reductions in the more mature parts against the premiums of paying for products such as very high-speed devices (e.g., 25ns) and special feature parts such as dual-port RAMs or RAMs with separate I/Os.

NONVOLATILE MEMORIES--EPROMS

(Slides 22/23)

The worldwide market for MOS EPROMs closed with revenue of $878 million in 1985, down 26 percent from 1984 revenue of $1,179 million. In a year that saw the entire MOS memory market shrink by 39 percent in dollars, MOS EPROMs held up well in revenue, although profits for all participants were impacted dramatically, especially in the second half of the year. For example, Intel's EPROM revenue dropped only 2 percent while its market share increased by 5 percent from 17 percent to 22 percent of the

worldwide total, reversing the company's loss of share of 1984. In September, AMD, Intel, and National Semiconductor jointly accused Japanese EPROM manufacturers of dumping. On March 10, 1986, the Department of Commerce's preliminary ruling assigned dumping penalties averaging 63 percent on Japanese suppliers.

(Slide 24)

Like all MOS memory markets, the product is slowly becoming more varied as users offer several package options and special application parts. Enough of the technical and manufacturing foundation is now in place to point to stronger increases in the EPROM's already broad range of applicability. The foundation not only includes significant reductions in cost and cost per bit, but, very importantly, in ease of use, inventoriability, and adaptability to an automated, high-volume, production line environment. In Europe, the use of mask ROMs has been reduced drastically, as the EPROM's steeper leaning curve has eroded the price advantage that ROMs have had historically. Drastic swings in market pricing and product line profitability plus technical difficulty in mastering the OTP package have again slowed adoption and use of plastic package EPROMs. With high cerdip prices in 1984, vendors had little incentive to move to plastic. With low cerdip prices in 1985, users had little incentive to adapt to what was viewed as an uncertain technology. On top of all this, manufacturers continued to have difficulty in achieving a speed sort for the plastic package that is comparable to that of cerdip parts and guaranteeing long-term reliability of OTP plastic packages.

(Slides 25/26)

Finally, before we leave MOS memory, licensing agreements and joint ventures pertaining to MOS memory products are increasing. There were 7 exchanges in 1982, 14 in 1983, 17 in 1984 and 18 in 1985. There have been 9 agreements just in the first few months of 1986, but there are many reasons for this increase in licensing agreements and joint ventures. One of the most evident is the need for capital. In 1985, many semiconductor companies experienced deep financial losses. The selling of technology was a means of creating revenue in a very depressed market. Venture capital has been tight over the last few years, and many start-up companies were not able to attract additional rounds of financing needed to sustain their growth. These companies sold their designs as a means of survival. Other companies were rich in manufacturing capabilities but in need of technology and products to fill their factories; these companies sold fab space to create revenue. Nearly all MOS memory agreements used technology from U.S. companies. One reason for this primarily one-directional flow is that the United States is still the largest innovator of new technology. Another, and perhaps more significant reason, is that the Japanese are very reluctant to sell their technology for short-term gains in revenue and market share. Overall, companies in the United States have been less successful

at semiconductor production than those in Japan and Korea. Japanese and Korean companies often have fab capacity that is subsidized by larger parent corporations, allowing them to run very efficient fab facilities. This has encouraged a large number of U.S. companies to trade technology for Japanese and Korean fab capacity. Some of the European joint ventures have been Vitelic and Philips for CMOS SRAMs, Dallas and Thomson Mostek for multiport memories and FIFOs, Cypress and Matra-Harris for 4K/16K fast SRAMs, Intel and Philips for 256K EPROMs, and Siemens and Toshiba for 1Mb DRAMs. Finally this slide notes how Dataquest estimates European MOS memory revenue of the 11 leading suppliers.

MOS Microcomponents

This shows the Dataquest family tree.

(Slide 28)

Microcomponents are divided into three areas; processors, microcontrollers, and microperipherals.

(Slide 29)

In Europe in 1985, the number one company in revenue was Intel with $114 million. The top five companies comprised three American, one Japanese and one European. Despite the overall market slowdown, MOS microcomponents fared well, increasing from $465 million to $485 million in 1985.

(Slide 30)

This chart shows the relative size of the marketplaces for the given categories.

Dataquest estimates that in Europe, the MOS microcomponent marketplace will grow from $485 million in 1985 to $2,190 million by 1991, with controllers and microprocessors demonstrating higher-than-average growth over this time span. Worldwide microcomponent consumption is demonstrated in the next slide.

(Slide 31)

Over the past few years, the North American microcomponent consumption as a percentage of the world market has declined, and in Western Europe and Japan it has increased. Dataquest expects this trend to continue, and expects that the North American marketplace will account for 34 percent of consumption by 1991 compared with 42 percent today.

(Slide 32)

Today we see the microprocessor industry being driven by the data processing sector. In terms of design-in, 16-bit microprocessors are dominating; four 16-bit microprocessor architectures account for 84 percent of the marketplace. Increasingly the trend is toward higher levels of integration on the microprocessor. Examples of this are the Philips 68070 with DMA and MMU and the Hitachi Z80-based 64180. Increased bus width, coupled with the demand for extended I/O functions, has resulted in higher pin counts and a variety of packages available now on the marketplace. Tomorrow is the 32-bit world, as the large chip area and lower power consumption demanded by market considerations make CMOS processing a prerequisite. The up-and-coming ASIC revolution does not mean that microprocessors will lose out in growth rate; in fact, it implies the opposite. Microprocessors today are forming the core of the most complex standard cell/gate array offerings.

(Slide 33)

In 1985, worldwide shipments of 8-bit processors accounted for 60.4 million units; 16-bit were 7.9 million units; and 32-bit were 100,000 units. Intel and Motorola architects are the market leaders at 16-bits; Zilog, Intel, and Motorola architects dominate the 8-bit market. The 32-bit microprocessor marketplace is still very much in its infancy. In 1985, Dataquest estimates that 92,000 units were shipped. Eighty percent of these units went into engineering and scientific workstations, 8 percent went into industrial factory automation (robotics), 4 percent were dedicated to telecom applications, office automation accounted for 1 percent, and others such as military and parallel processing totaled 7 percent. In 1990 we expect this picture to change dramatically. The office automation marketplace is forecast to grow from 1 percent of consumption to 76 percent of consumption, the engineering/scientific workstation market to fall from 80 percent to 9 percent, robotics and telecom are expected to account for 9 percent between them, and other categories 6 percent.

(Slide 34)

Manufacturers of 32-bit microprocessors have entered into an eager price competition. During the next two years we can expect price reductions of approximately 50 percent. Most 32-bit MPUs will be priced at less than $100 in a few years. In 1990, we believe that 32-bit prices could be close to those of today's 16-bit microprocessors. The average selling price will be affected by factors such as new product introductions, processor clock rates, manufacturing volume, and package complexity. The 32-bit market is expected to grow by a factor of 12 between 1985 and 1990; the total market revenue for 32-bit microprocessors and peripheral device development tools and software is expected to reach $1 billion in 1990.

(Slide 35)

One key philosophy accompanying merging the 32-bit world is whether a microprocessor should be a complex instruction set computer (CSIC) or a reduced instruction set computer (RISC). The RISC architecture stems from the desire to create a much faster and more efficient computing engine rather than a general-purpose mainstream with all the bells and whistles used in CISC architecture. Examining current product offerings, designers will notice that the majority of the units are more general-purpose types. RISC devices are still a minority, though notable. RISC philosophy has resulted in micro designs such as Fairchild's Clipper, Inmos' IMST414, and MIP's (a California start-up's) R2000. These devices will likely find their way into particular market niches where the issues of speed and software simplicity will prevail.

Hewlett-Packard is backing RISC technology with its HP 3000 series model 930 and Nixdorf with its 128-user Targon/35 SUPERMINI it gets from Pyramid.

The RISC idea was that if you wired in a few basic instructions so that they executed very quickly, you could do complex instructions by making them out of simpler ones. A good analogy can be drawn between writing in Chinese and English. Chinese has a few thousand copier characters that make it hard to learn and slow to write, although it is superficially efficient. English, on the other hand, gets by with a few characters, but these can be formed into many tens of thousands of words and written or typed very quickly indeed. The uphill struggle the RISC chips face is lack of available software and lack of people who know how to write code for them.

(Slide 36)

Sixteen-bit MPU sales to the PC sector are dominated by the Intel architecture. This is due to the 8086-MS DOS connection, which when adopted by IBM, spawned a tremendous number and variety of application packages.

In the 32-bit stakes, the direct software-processor links are weakening. Most software today is not written in Assembler language, which is tied to the machine code of the processor, but in high-level languages such as C, Pascal, and Modula-2. It is therefore relatively easy to port or transfer to machines that use different processors.

What can be guaranteed is that one processor will not win. The competition between users of the elegant, easy-to-program 68000 and 68020, the bolt-on, upward compatibility of the 8080-803086, and the new raw power of the RISC designs, will ensure that users continue to be offered even more powerful engines every year for less cash.

(Slides 37/38)

The industrial, data processing, and transportation marketplaces accounted for 87 percent of microcomponent consumption in 1985. The data processing marketplace is characterized by an on-going requirement for low-power systems; the industrial and transportation sectors by harsh operating environments due to electrical noise and high temperatures. A typical example would be in an automotive application with the microcontroller positioned under the bonnet of a car. Auto makers are being forced, both by cost reduction pressures and by legislation on exhaust emissions and fuel efficiency, to incorporate more and more high-technology electronics. Engine controls, electronic fuel injection emission monitors, automatic transmission controls, and oil service reminders are just some of the typical applications that microcontrollers are performing in the transportation sector.

(Slide 39)

The harsh environments experienced in the transportation and industrial sectors make the use of CMOS technology increasingly popular. CMOS technology, higher noise immunity, and low power supply requirements have resulted in us forecasting its rise in consumption from 24 percent today to 82 percent by 1991.

(Slide 40)

Microprocessors designed specifically for digital signal processing (DSP) are about to take off in a dynamic way. Dataquest estimates that the DSP world market will grow from $225 million in 1985 to $769 million in 1990.

The 1985 DSP consumption was made up of building blocks (49 percent), gate arrays (21 percent), DSP processors (15 percent), and custom circuits (15 percent).

The boom now starting is being fueled by two developments that have dramatically increased processing speeds, up to an order of magnitude, at costs that mean the chips can be used in areas as price sensitive as consumer electronics.

The first is VLSI technology. A typical state-of-the-art DSP chip, Analog Devices' 2100, is currently made in 1.5-micron CMOS and will be shrunk to 1 micron within a year. It has a 125ns cycle time and a capacity of 8 MIPS. The first single chip devices were made with 5-micron geometries, cycle times two to five times slower, and corresponding lower MIPS rates.

The second development is parallel processing. This has become one of the glamorous topics of the computer and electronics industry in the form of products such as the Inmos transputer and concurrent processors from companies such as Intel. Parallel processing allows complex algorithms to be processed in real time.

(Slide 41)

Dataquest views the greatest potential for DSP applications to be in telecoms, data processing, speech processing, defense, image processing, and consumer electronics.

Up to the present, the single greatest market for DSP circuits has been modems. Two up-and-coming markets are speech and image processing. In the former, that means store-and-forward systems, analysis, synthesis, and recognition; and in the latter, machine vision, medical, CAD/CAM, and graphic arts.

As a final note I would say that DSP processors are the most successful exponents of RISC architecture, being designed around two operations--multiply and accumulate. There is nothing that you can do with a DSP that you cannot do with a standard microprocessor. But with DSP you can do it in real time, and that's what the applications are demanding.

MOS MEMORY

- Market overview
- Trade issues
- DRAMs
- SRAMs
- Nonvolatile memories

MOS MEMORY

- Market overview

WORLDWIDE MOS MEMORY MARKET SIZE

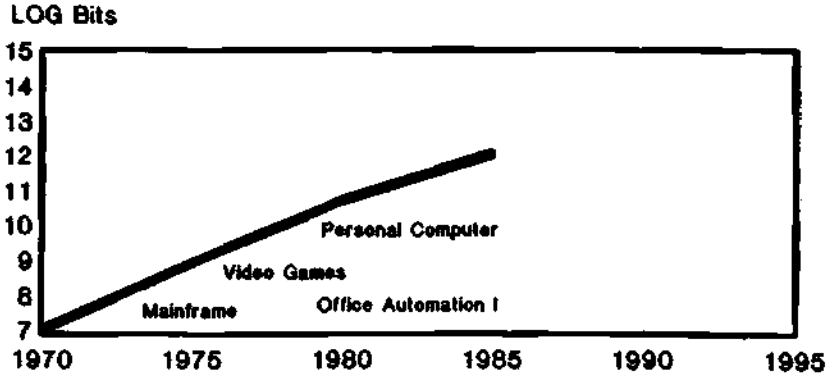
Millions of Dollars

	1984	1985	Percent Change
DRAM	$3,472	$1,653	(52%)
Total SRAM	1,203	906	(25%)
Fast SRAM	354	365	3%
Slow SRAM	849	541	(36%)
EPROM	1,179	878	(26%)
EEPROM	123	117	(5%)
NVRAM	24	20	(17%)
ROM	513	367	(28%)
Other MOS Memory	19	26	37%
Total Market	$6,533	$3,967	(39%)

Source: Dataquest

MARKET OUTLOOK: YESTERDAY AND TOMORROW

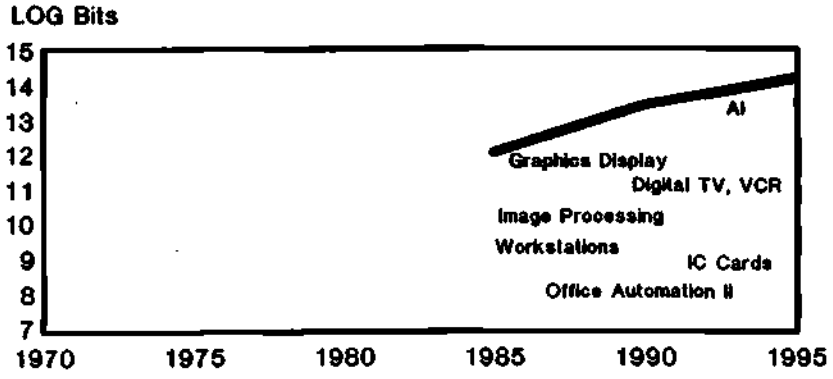
MOS Memory Bits Shipped



Source: Dataquest

MARKET OUTLOOK: YESTERDAY AND TOMORROW

MOS Memory Bits Shipped



Source: DATAQUEST

MOS MEMORY

- Market overview
- Trade issues

MOS MEMORY MARKET SHARES BY HOME BASE OF PRODUCER

Millions of Dollars

	1984	1985	Percent Change
United States	$2,695	$1,453	(46%)
Japan	3,540	2,285	(35%)
Europe	291	190	(35%)
ROW	26	39	50%
Total	$6,533	$3,967	(39%)

Source: Dataquest

MOS MEMORY MARKET SHARES BY HOME BASE OF PRODUCER

Percent of Worldwide Market

	1984	1985
United States	41%	37%
Japan	54	58
Europe	4	5
ROW	0	1
Total	100%	100%

Note: Totals may not add due to rounding.

Source: Dataquest

TRADE ISSUES

Casualties of RAM wars . . .

- Mostek – DRAMs
- Inmos – DRAMs
- NSC – DRAMs
- Motorola – NMOS DRAMs
- Intel – DRAMs
- (Mostek Corporation)

DUMPING PENALTIES

Company	64K DRAM	EPROM	256K DRAM
Hitachi	18.49%	30.0%	20.0%
Toshiba	38.83%*	21.7%	50.0%
Fujitsu	38.83%*	145.0%	75.0%
NEC	8.93%	188.0%	108.0%
Mitsubishi	94.00%	63.1%*	40.0%*
Oki	12.52%	63.1%*	40.0%*
Overall	38.83%	63.1%	40.0%

*General levy against all Japanese manufacturers other than the companies specifically named

Source: Dataquest

U.S.-JAPAN AGREEMENT

- Japan to increase purchase of semiconductors above 20% of market over next five years
- Japanese prices monitored by MITI
- Department of Commerce will monitor production costs/prices of Japanese chips
- U.S. to suspend dumping suits

MOS MEMORY

- Market overview
- Trade issues
- DRAMs

CONTRACT DRAM PRICE TRENDS

Product/Family	1987 Q1	Q2	Q3	Q4	Year
64K DRAM (150ns)	$1.00	$1.00	$1.00	$1.00	$1.00
256K DRAM (150ns)	$2.15	$2.10	$2.05	$2.00	$2.00
1Mb DRAM	$15.00	$11.50	$8.40	$7.75	$10.54

Source: Dataquest

1Mb DRAM

Announced Designs:	12
CMOS:	All (By '87)
Chip Size = K(mils)^2:	70–108
Design Rules:	1.2–1.5
H1 1986 Shipments (K):	1,490

Source: Dataquest

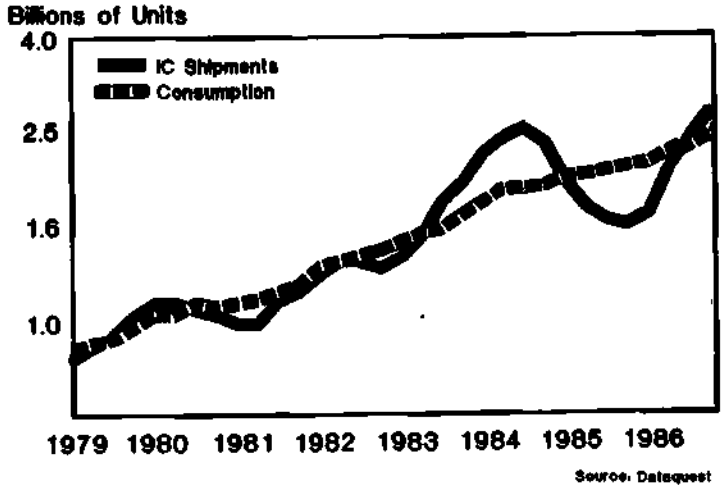
1Mb DRAM
ESTIMATED SHIPMENTS

Company	Technology	K Units (H1 1986)
ATT	CMOS	17
Fujitsu	NMOS	350
Hitachi	CMOS	235
Mitsubishi	NMOS	7
NEC	NMOS	7
TI	CMOS	7
(256x4)	CMOS	7
Toshiba	CMOS	850
	NMOS	10
	Total	1,490

Source: Dataquest

ESTIMATED MEMORY UNIT SHIPMENTS

U.S. IC Units



MOS MEMORY

- Market overview
- Trade issues
- DRAMs
- SRAMs

WORLDWIDE STATIC RAM SHIPMENTS

	1984	1985	Percent Change
Slow SRAM	849	541	(36%)
Fast SRAM	354	365	3%
Total	1,203	906	(25%)

Source: Dataquest

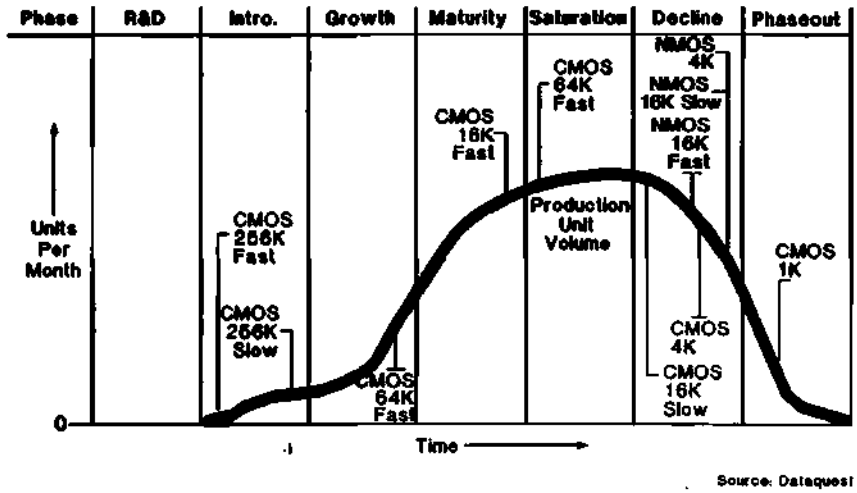
STATIC RAM MARKET SHARES BY HOME BASE OF PRODUCER

(Millions of Dollars)

	1985	Fast	Slow
United States	250	126	124
Japan	565	170	395
Europe	86	70	16
ROW	5	1	4
Total	906	367	539

Source: Dataquest

STATIC RAM PRODUCT LIFE CYCLE



Source: Dataquest

STATIC RAM - TRENDS

- More participants
- Demand for more complex parts
- Outlook becoming more application specific

MOS MEMORY

- Market overview
- Trade issues
- DRAMs
- SRAMs
- Nonvolatile memories

ESTIMATED WORLDWIDE EPROM REVENUES

(Millions of Dollars)

Company	1983	1984	1985
Intel	$184	$ 202	$197
Fujitsu	99	158	118
AMD	75	155	117
Hitachi	124	145	113
Mitsubishi	83	155	66
Texas Instruments	83	128	65
NEC	64	70	55
Toshiba	18	38	55
National	39	45	22
Others	60	83	70
Total	$829	$1,179	$878

Source: Dataquest

EPROM - QUARTERLY MARKET MAKEUP BY DENSITY

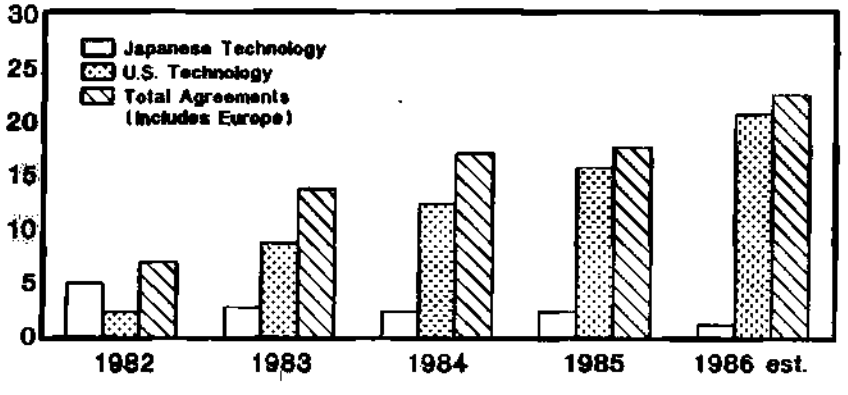
(Millions of Dollars)

		1985				
Density	1984	1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Year
2K-8K	$ 6	$ 1	$ 1	$ 1	$ 0	$ 3
16K	115	19	18	17	16	70
32K	190	35	27	22	18	102
64K	450	100	70	65	55	290
128K	330	80	55	46	43	224
256K	87	44	52	38	41	175
512K	1	2	4	3	5	14
1Mb	0	0	0	0	0	0
Total	$1,179	$281	$227	$192	$178	$878

Source: Dataquest

MOS MEMORY JOINT VENTURE AND LICENSING AGREEMENTS

By Source of Technology



Source: Dataquest

ESTIMATED EUROPEAN MOS MEMORY REVENUES OF 11 LEADING SUPPLIERS

(Millions of U.S. Dollars)

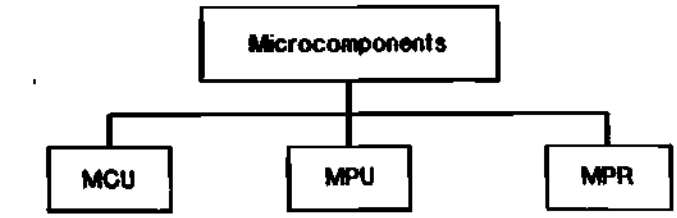
Company	1984	1985	Annual Growth
Texas Instruments	$136	$115	(15.44%)
Hitachi	$143	$109	(23.78%)
NEC	$111	$ 91	(18.02%)
Intel	$ 95	$ 85	(10.53%)
Fujitsu	$ 49	$ 53	8.16%
Toshiba	$ 59	$ 39	(33.90%)
AMD	$ 56	$ 35	(37.50%)
Siemens*	$ 38	$ 24	(36.84%)
Mostek	$ 74	$ 23	(68.92%)
Mitsubishi	$ 16	$ 21	31.25%
Thomson Semiconductors	$ 24	$ 21	(12.50%)

*Includes Litronix

Source: Dataquest

MICROPROCESSORS

MICROCOMPONENTS FAMILY TREE



Microcontrollers	Microprocessors	Microperipherals
4-bit	8-bit	Communication
8-bit	16-bit	Mass Storage
16-bit	32-bit	System Support
		Keyboard/Display
		General Purpose
		Special Purpose

Source: Dataquest

ESTIMATED EUROPEAN MOS MICROPROCESSOR REVENUES OF 12 LEADING SUPPLIERS

(Millions of U.S. Dollars)

Company	1984	1985	Annual Growth
Intel	$96	$114	18.75%
NEC	$60	$ 59	(1.67%)
Motorola	$38	$ 49	28.95%
AMD	$43	$ 47	9.30%
Philips-Signetics	$30	$ 35	16.67%
Signetics	$ 4	$ 8	100.00%
Hitachi	$27	$ 29	7.41%
National Semiconductor	$30	$ 29	(3.33%)
Thomson Semiconductors	$15	$ 28	86.67%
RCA	$16	$ 16	0.00%
SGS	$16	$ 13	(18.75%)
Siemens*	$14	$ 13	(7.14%)
Texas Instruments	$15	$ 13	(13.33%)

*Includes Litronix

Source: Dataquest

ESTIMATED EUROPEAN MOS MICROCOMPONENT MARKET

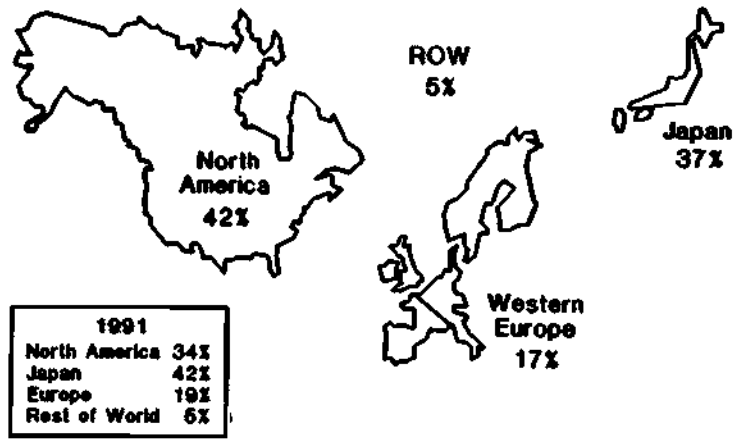
(Millions of Dollars)

	1985	1991
Microcontroller	214	1,024
Microprocessor	69	339
Microperipheral	202	827
Total MOS Micro	485	2,190

Source: Dataquest

1986 MICROCOMPONENT CONSUMPTION

North America, Europe, and Jaapan



Source: Dataquest

MICROPROCESSORS

Today	Tomorrow
• 16 bits dominate	• 32 bits dominate
• Four 16-bit = 84% of market	• CMOS comes of age
• Integration – Virtual memory – Peripherals	• Higher integration
	• Higher pin count
	• Voice I/O displaces keyboard
• Packaging proliferation	• Shift toward core processor technology
• Standards – UNIX, MS/DOS	

Source: Dataquest

1985 MICROPROCESSOR SUPPLIERS

(Millions of Units)

	8-bit	16-bit	32-bit
Shipments	60.4	7.9	0.1
Major Suppliers	NEC Toshiba Intel Zilog Motorola	Intel Motorola	Motorola National Inmos
Major Products	Z80 8085 6802 8088 6809	8086 68000 80286 80186	68020 32032 T414

Source: Dataquest

ESTIMATED WORLDWIDE 32-BIT MPU SHIPMENTS

(Millions of Units and Dollars)

	1986	1987	1988	1989	1990	1991
Units	0.29	0.71	1.42	2.63	4.73	8.52
Dollars	36.12	59.60	92.38	138.57	200.92	321.47
ASP	$124.55	$83.88	$65.01	$52.71	$42.46	$37.74

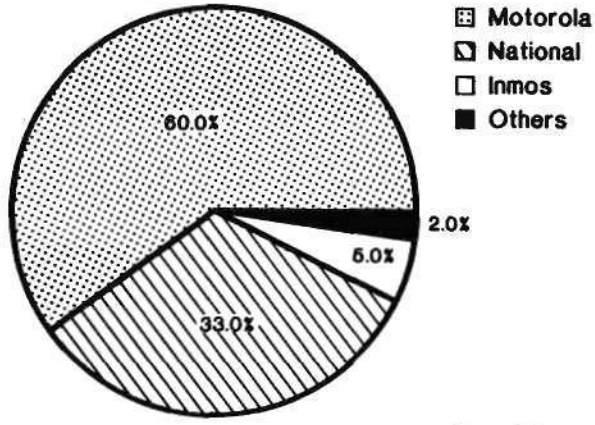
Source: Dataquest

32-BIT MPU FEATURES

Announced Designs:	18
NMOS/CMOS:	4/14
Std. Clock Frequency:	12-16 MHz Now
Chip Size:	375 x 375mm
Package Type:	PGA
Design Rule:	1.5 Micron

Source: Dataquest

32-BIT MPU
1985 MARKET SHARE BY MANUFACTURER



Source: Dataquest

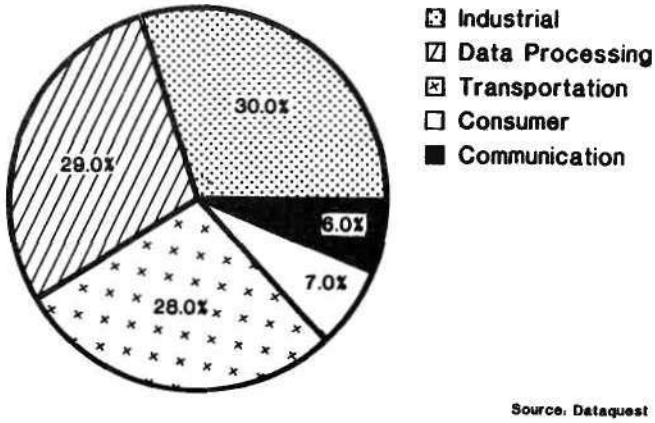
MICROCONTROLLERS

MICROCONTROLLERS

Today	Tomorrow
• 8-bit dominates the 1980s	• 16 bits
• Four 8-bit architectures - 53% of the market	• I/O intensive
• CMOS conversion at full speed - 24% today - 82% by 1991	• EEPROM on-chip • OTP

Source: Dataquest

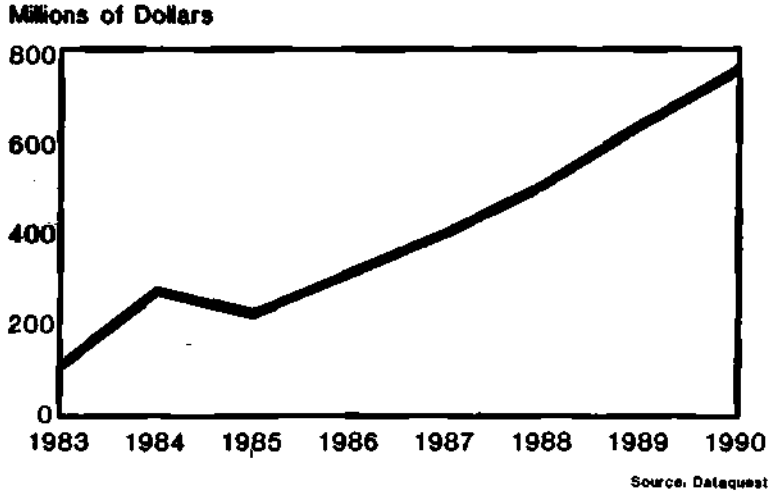
8-BIT MICROCONTROLLER WORLDWIDE CONSUMPTION BY APPLICATION MARKETS IN 1985



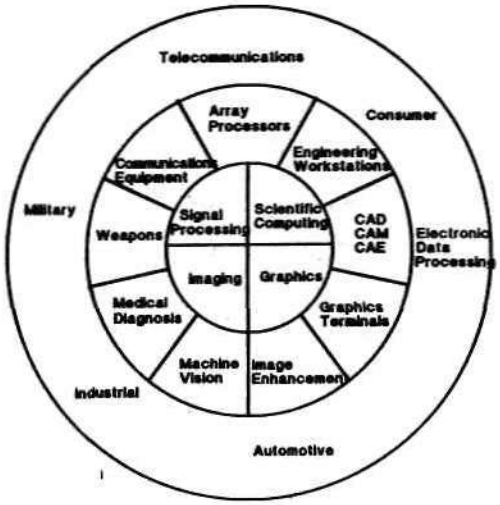
Source: Dataquest

DSP

DIGITAL SIGNAL PROCESSING REVENUES



USES FOR DSP ICs



Source: Dataquest

Dataquest
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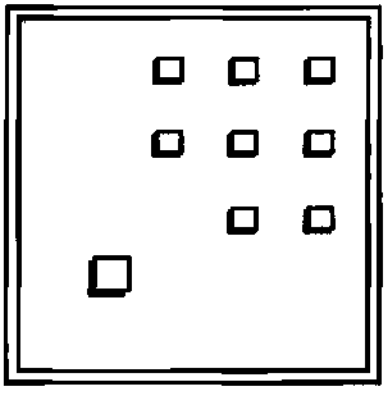
The Dun & Bradstreet Corporation



Dataquest
IC Outlook '87

September 15–23, 1986

PACKAGING REVIEW

MARK A. GIUDICI
Dataquest Incorporated

(Slide 1)

Packaging has become an increasingly important issue for both the user and the semiconductor supplier. There are trends on both sides that are impacting the direction that IC packaging is taking. In the following presentation, I will discuss the current trends and present data that indicates where we believe packaging is headed as a technology.

(Slide 2)

As I said, there are trends for both users and suppliers. A very clear trend is that equipment manufacturers are using more and more VLSI devices. There is a sweeping desire to reduce space and cost through more condensed packaging and to automate as much as possible. This, of course, forces users to evaluate their needs carefully.

(Slide 3)

IC suppliers are maintaining standard dual-in-line packages and some small outline packages for low-end volume products. This is especially true for commodity logic devices. It has also been projected that about 35 percent of microprocessor products will be in some form of surface-mount package by the end of this year.

Over the last couple of years, memory devices have been on the leading edge of packaging technology due to density requirements. The next slide will show how functional density has been changing over time. It is interesting to note that concurrent with this, the pitch of various packages has been decreasing.

(Slide 4)

We believe that by 1990, IC packages will exhibit an increase of 20 to 30 percent in functional density, which is defined as die area per package footprint area.

(Slide 5)

Looking out a few years, these trends are apparent. OEM companies will be close to 50 percent in their use of surface-mount devices in end products. Again, small outline will probably stay at the low pin count range while plastic DIP remains a viable technology for most of the devices produced. At that point, chip carriers should become a volume technology, filling the midrange pin count requirements. Lastly, pin grid arrays will fill the upper end of high-pin density parts. Even though this is a through-hole technology, it is still considered reliable for those applications.

(Slide 6)

Currently, there is some overlap of pin count with the newer package technologies. Small outline is still relegated primarily to the lower pin density range for mainstream products, along with DIPs, such as logic parts. This appears logical since the package shape and lead spacing are similar to DIP technology.

PGA packages are being used for the higher pin density products since the package footprint can be kept in a manageable range. Concurrent with this is the role that tape-automated bonding plays. Presently, lower pin count devices such as logic can be found in TAB as well as in SO.

(Slide 7)

This slide depicts the number of pins per square inch possible with the different technologies. As we move on toward the next century, you can see that TAB becomes the only technology that is currently known for maximum use of board space.

(Slide 8)

Here is a good indication of where pin counts are by product type for the higher pin density products. These areas represent ranges. Gate arrays specifically have the broadest spread of pin-outs, since internal logic structures can vary quite a bit.

(Slide 9)

The next three graphs show total package consumption by region. This information is based on IC consumption, and therefore shows consumption of all IC package types. It is interesting to note that in 1985, the United States had the majority, but as the next slide indicates, that will change.

(Slide 10)

In 1988, the Japanese begin to be the majority consumer by virtue of the consumer business, while Europe and the United States lose a little of the share.

(Slide 11)

By the beginning of the next decade, the Japanese are expected to lead the world, primarily because of automated assembly. There already exists quite an effort among many equipment suppliers in Japan to make it easy to go the automated processes necessary for those packages.

(Slide 12)

For many years, no specific product type led the move in any one direction of packaging. However, within about the last two years, DRAMs, for reasons of density, have become an indicator. In 1986, plastic and ceramic DIPs will still be the leading packages.

(Slide 13)

By 1989, DIPs are forecast to shrink by more than 20 percent, and ZIP and small outline J-lead to grow dramatically.

(Slide 14)

As we move into the 1990s with much higher memory densities, the SOJ package becomes the leader, with DIP still second in volume. Here is a clear example where board space coupled with the highest possible functional density becomes the overriding issue.

(Slide 15)

These last graphs take us into the issue of surface mount as a whole. To reiterate, high-density device architectures led by smaller geometries and line widths, the desire to bring costs down maintaining while price competitiveness, and as always, building a better and faster machine, will require the increased use of SMT. Users have an idea of what they must do to achieve these goals; now the decisions must be made to execute them.

(Slide 16)

I believe that some people are unsure about where surface mount is being used, and are naturally cautious about the unknown. This list represents several already existing applications for this technology. Consumer and military has always been a given, but these others are newer uses for SMT.

(Slide 17)

The reasoning behind using surface mount is fairly straightforward. At today's technological pace, reducing size and therefore cost is a major goal. But surface mount also allows for less weight. This may be significant to certain users, especially in automotive, consumer, and avionic/space-oriented systems. Regionally, here is a primary breakout.

(Slide 18)

This slide shows the primary end applications for 1985. The computer segment was actually the leader in the United States in that year but automotive has grown significantly. Once again, the same issues come up regarding size and cost. Additionally, reliability is playing a greater role as thermal coefficients are reduced and certain package types handle stress better than through-hole technology.

(Slide 19)

A quick comparison shows the benefits and advantages of SMT over through-hole assembly for a typical board example. The results indicated here affect not only cost, but also reliability and the cost of rework later.

(Slide 20)

The impact on the design of boards for a system using surface mount is going to vary. The one clear benefit, though, is the reduction in board size and most probably, board cost. As the earlier example showed, a six-layer board was reduced to four layers and the cost was halved. This also results in the increased reliability and overall system performance improvements. Inductance, capacitance, and resistance parameters can be reduced on the order of 55 percent using SMT.

The drawbacks tend to be the cost of assembly equipment, since most of what is required is still new to the industry, and some offset in reliability different from the reliability benefits.

(Slide 22)

A few points worth indicating here are:

- Various standards for the packages are emerging, but support is slow. By this I mean handling equipment, assembly equipment, and fixturing.

- New developments are continuing to come from the supplier base as these companies strive to perfect the best solutions to the issue of reliable, cost-effective packaging for next-generation products.

The more advanced packaging techniques of tape-automated bonding and flip-chip will have the greatest impact on the user for system packaging. These methods will provide lower-cost, higher-reliability products when performed in volume.

(Slide 23)

In conclusion, the complete packaging issue has a pronounced effect upon the user. This has never been more true than now. The decisions that companies must make in selection and implementation are critical. Remaining competitive is becoming harder to accomplish, since costs and product quality are keys to success.

As users consider the transition to more advanced packaging for their purposes, it is vital to examine carefully all of the possible options. Things will continue to change for the user as IC vendors move more mature devices and new devices into a wider range of package options.

PACKAGING UPDATE

THE IC PACKAGING DILEMMA

User Trends

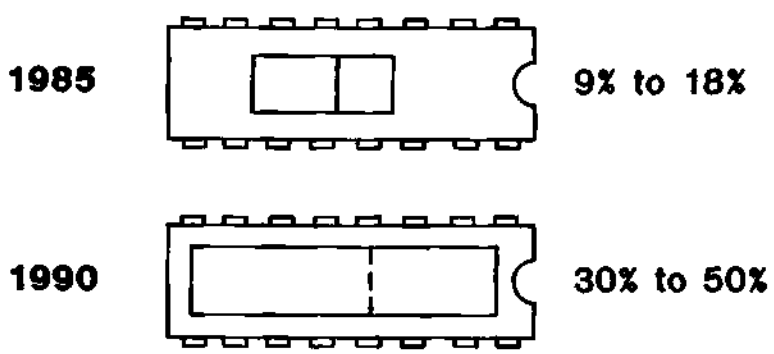
- Increased use of VLSI
- Smaller packages – less space
- Reduced board/module costs
- Automated assembly process

THE IC PACKAGING DILEMMA

Supplier Trends

- DIP & SO are low-end mainstream types
- 1986: 35 percent of MPUs will be SMD
- Memory devices leading package trend
- Functional density increasing
  - Package pitch decreasing

PACKAGE FUNCTIONAL DENSITY



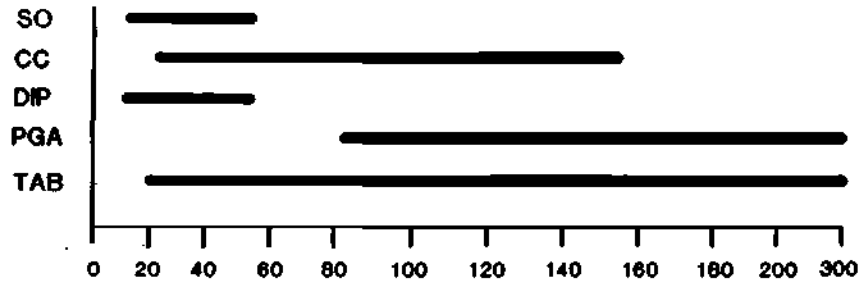
Source: Dataquest

A VIEW TOWARD 1990

Dataquest Forecasts

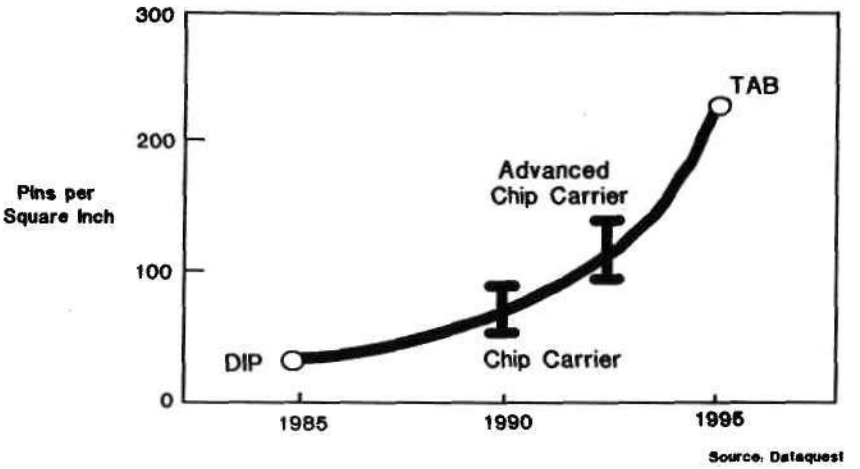
- Worldwide presence of SMT in OEMs will be 50%
- SO relegated to 28 pins or less
- Plastic DIP will be majority type until 1990
- Chip carrier growing now – volume technology in the 1990s
- Pin grid arrays are solution at 84 pins and above

ESTIMATED PACKAGE CONSUMPTION AS A FUNCTION OF PIN COUNT



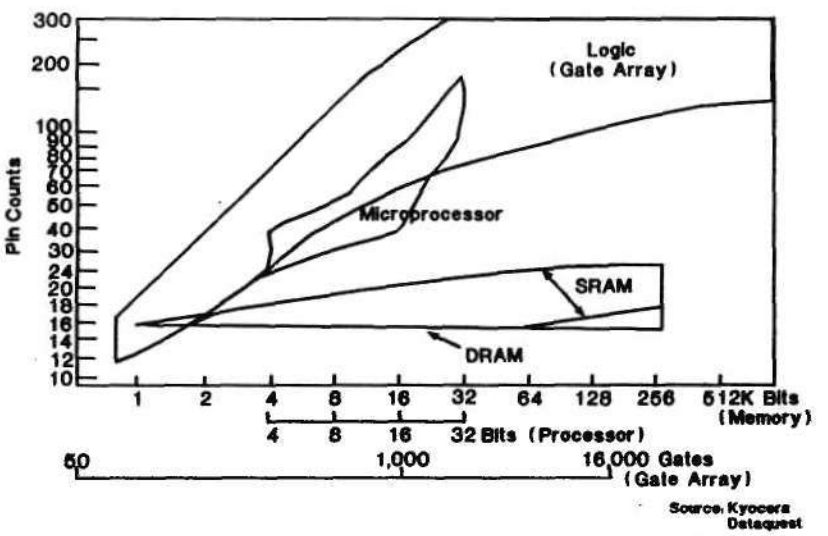
Source: Dataquest

ACHIEVABLE BOARD DENSITIES BY PACKAGING TECHNOLOGY



Source: Dataquest

IC PACKAGING



Source: Kyocera
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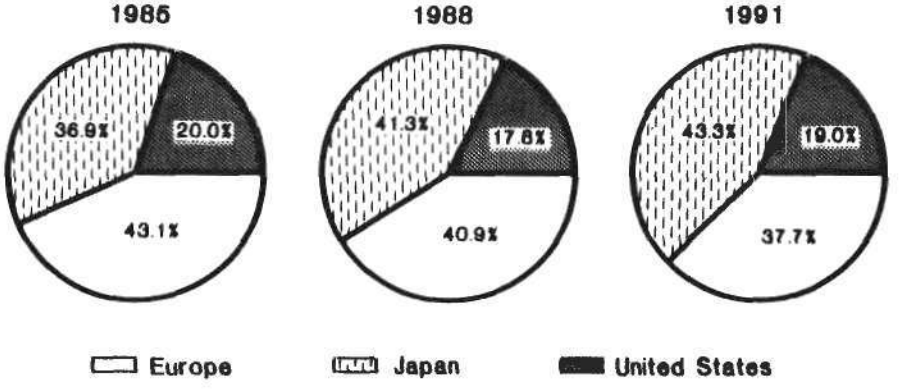
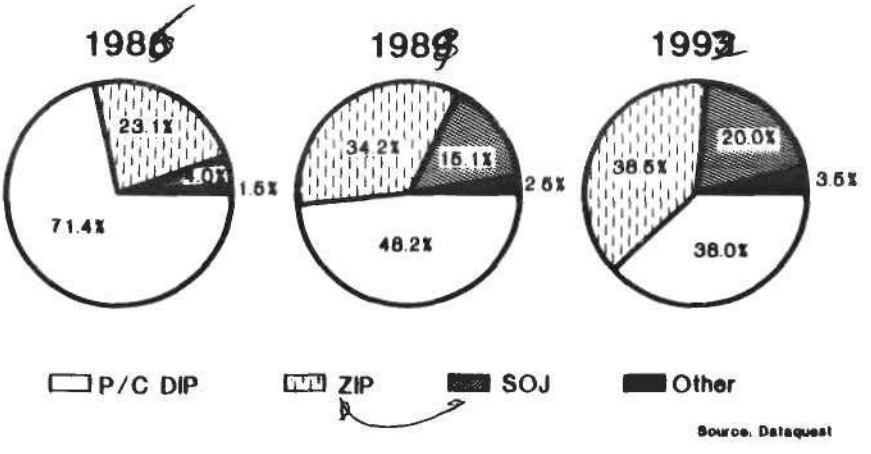
ESTIMATED 1985 WORLDWIDE PACKAGING TRENDS



Source: Dataquest

ESTIMATED 1Mb DRAM PACKAGES



Source: Dataquest

BASIC DRIVING FORCES

- Submicron device geometries
- Reduced overall system cost
- Continued system performance improvements

These forces are promoting the requirement for surface-mount technology.

SURFACE-MOUNT TECHNOLOGY

Where?

- Consumer
- Automotive
- Disk storage
- Avionics, missiles and space
- High-density memories
- Power supplies

SURFACE-MOUNT TECHNOLOGY

Why?

- Principally due to:
  - Small size
  - Weight considerations

Uses

- U.S. – automotive
- Japan – consumer
- Europe – telecommunications

SURFACE-MOUNT TECHNOLOGY END-USE SEGMENTS - 1985

	Japan	Europe	United States
End Use	Consumer	Telecom-munications	Computers
Driving Force	Small size	Reliability	Cost reduction
Percent of ICs Consumed Worldwide	35%	18%	41%
Percent of ICs in SMT	16.7%	1.8%	1.6%
Dominant SMT Approach	TAB/COB	SO	COB/SO/CC/TAB

Source: Rose Associates

ASSEMBLY TECHNIQUE COMPARISON

	Through-Hole	Surface-Mount	% Reduction
Board Size	11" x 14" (154 sq. in.)	6.5" x 9.6" (64 sq. in.)	58%
No. of Layers	6	4	33%
Board Cost	$150	$75	50%

Source: Texas Instruments

SURFACE MOUNT

Board Design Impact

- 30% to 70% board size reduction
- Enhanced reliability
- Improved performance characteristics

Negative aspects include:

- Equipment costs
- Some reliability offset

ESTIMATED SURFACE-MOUNT PRODUCTION LINE COSTS

Equipment	Cost
Solder screener	$ 60,000
Pick and place	200,000
Soldering system	90,000
Board cleaning	60,000
Visual inspection (automated)	120,000
Board tester (manual)	100,000
Miscellaneous (repair, etc.)	100,000
Total	$730,000

Source: Tektronix, Inc.

ANALYSIS

- Standards are appearing – but the world is not fully prepared.
- More developments are in process – suppliers are examining various solutions.
- TAB, flip–chip types will result in greatest change.

CONCLUSIONS

- Packaging has dramatic effect
  - Results in significant decisions
- Clearly a transitional time for users
  - Look at all options carefully

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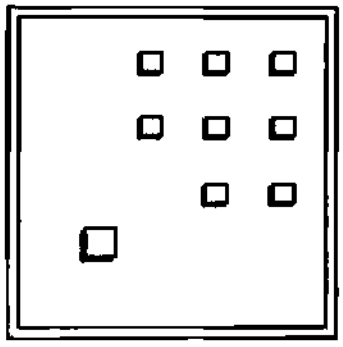


Dataquest
IC Outlook '87

September 15-23, 1986

VENDOR-CUSTOMER RELATIONSHIPS

PETER SAVAGE
Dataquest UK Limited

In this last session of today's proceedings, Vendor-Customer Relationships, I intend to address the live issue of strategic partnering. This is strategic partnering between supplier and user and is all about risk management, which is no easy task. Alliances are critical.

The increasing costs of R&D and capital investment more and more demand a sharing of the risks (and rewards). Correctly applied, alliances will provide cost-effective innovative systems and market leadership. There are many issues here, but perhaps the most crucial is that each party should want the other--alliances are a two-way affair. Success can only be achieved by first defining the objective of a given relationship. Overall is the need to develop an environment that supports the necessary change, encourages participation, and brings about a deeper commitment to the semiconductor supplier/user relationship. Clearly, there are substantial obstacles to overcome, and the ability to take the longer-term view is often hampered by overriding short-term considerations. Those companies that successfully make the best use of technology will have the strategic edge. Productivity and quality are fundamental prerequisites for successful participation in the increasingly competitive high-technology environment. The more obvious elements include zero defects, zero delinquency, ship to stock, and just-in-time, but it is the potential impact of these, together with a greater accuracy to the planning cycles, that will, in turn, make an enormous impact on helping to dampen the peaks and troughs of the "traditional" semiconductor business cycles. With that goal in sight, what better motivation in an alliance can exist for the semiconductor manufacturer.

You have heard today how rapidly the industry is changing. The very character of the devices purchased has changed. In 1975, we estimated that slightly more than 50 percent of semiconductor consumption was discrete circuits and that prior to that time we were living in a discrete world. In 1986, we estimate that 77 percent of semiconductor consumption will be integrated circuits. By 1996, we will be living in an almost totally integrated world, with ICs representing almost 90 percent of semiconductor consumption. Within this shift to integrated circuits are the corresponding growths in the consumption of high-technology memory, microprocessor, and ASIC products, all having been fueled by major advances in technology. It is the advances in process technology that have been the underlying reason for the growth of both the semiconductor industry and the industries in which semiconductors are used, bringing about a rapidly falling price per function. We estimate that in 1996 the average price per function will be 0.5 millicents, down 1,100 percent from the present estimated 6.0 millicents per function. The trend to CMOS technology, which we expect to be the dominant technology of the early 1990s, has helped fuel increased device complexity, but as you heard in the packaging review earlier, it is also fueling important changes in packaging technology. There is now a marked shift toward surface-mounted devices.

So what of the future business climate? The data that my colleagues and I have presented suggest that users will be buying more and more complex devices in the future. Equipment manufacturers will be participating more and more in the design of the semiconductors used. CMOS will be the dominant IC manufacturing process and learning-curve pricing will continue for the foreseeable future. Surface-mount packaging will account for an increasing share of ICs shipped. And the problems of trying to limit the number of vendors worked with from an increasing number of potential suppliers--all are aspects that must be dealt with simultaneously. Many more companies will be buying semiconductors--and that means users competing for parts when a seller's market exists.

Given that the business environment is changing, how will the component procurement role adapt? There are many critical issues here but clearly the old-style adversarial relationships, so typical of the past, have no place in this progressive high-technology world.

Let us now look at what could and should be some of the major objectives of a strategic partnership.

During the recent Dataquest European Semiconductor Industry Service Conference held in Venice, Italy, a workshop entitled Semiconductor User Requirements was included in the proceedings. This workshop dealt with the topics of vendor motivation and practical steps for improved inventory management. Two important aspects of vendor-customer relationships, and the basis on which to build sound strategic alliances, emerged.

From the user's perspective, the most important objective was cost reduction. But there were many ways highlighted by which cost reductions could be achieved. Quality, leadtime, delivery performance, flexibility, and unit price are the key elements in reducing the cost of ownership. This would then achieve another important objective for the procurement role in being perceived as making a valuable contribution to company profitability, perhaps the single biggest motivator at the individual level in any organization. Of course other objectives exist, but the overriding factor in these is communications, both internal and external, since all concerned must buy into the objective if there is any chance at all of it being met.

In contrast, the objectives of the vendors are fundamental, interrelated, and essential for an alliance to be successful.

It would seem on the surface that the objectives from both sides are ones that can easily be achieved. And I think they are, if a real desire and willingness for them to succeed exists. There are a considerable number of obstacles that must be overcome before a meaningful series of programs can be implemented, but when the major ones, which are few in number, are addressed those remaining will effectively become nonissues.

Clearly the objectives of both parties must be effectively communicated and understood. And this includes feedback of the results, positive or negative, of any agreed programs that have been implemented. This in turn will help overcome concerns and potential disputes arising from performance measurement of vendors and the methods employed in such measurements. To define the cost of ownership requires a completely open-minded approach from both sides to ensure that all factors are taken into consideration and, once the methodology has been established, can be fundamental in the process of continuous improvement.

A joint responsibility exists in the education and training of employees to ensure that the increasing product complexity produced by vendor and user are fully exploited and to the best advantage. Essential are high levels of openness and confidence between participants to improve the quality and accuracy of forecasts and orders both in terms of the total needs and the profile of those needs. But fundamental and crucial to the success of an alliance is not only the acceptance of the intent behind such an alliance by corporate management but the active support of it--driving it from the top down.

With the obstacles removed, a collective set of second-order objectives arise. A mutually agreed-upon process of continuous monitoring of performance by both parties can and will lead to the accomplishment of continuous improvement based upon collaborative, goal-oriented action plans implemented with key suppliers. The encouragement of candor, risk taking, and honesty at all levels can only contribute to further success in the achievement of superordinate goals. Complacency cannot find any refuge within the existence of a dynamic environment.

Clearly a number of programs addressing the fundamental issues of quality, manufacturing, and zero defects should be implemented, the key elements of which I would now like to address.

QUALITY PROGRAMS

The key here is specification congruence, but if a problem does exist, then the mechanism for closed-loop corrective action to fix the problem once and once only must be implementable. For this to happen, however, vendors must have in place effective process control programs that ultimately will lead to 100 percent performance. This is 100 percent performance over a sustained period of time, which can only be achieved by the process of continuous improvement and shifting of the original goals. Clearly essential is the existence of common quality programs for all plant locations. With the required elements of quality achieved, the result will then translate to the elimination of incoming inspection/testing, impacting on related manufacturing processes.

MANUFACTURING PROGRAMS

The key element here, having met the quality goals, is that of just-in-time. This ultimately leads to the elimination of waste and hence reduction in costs. Only after progressive steps in reducing manufacturing cycle times can the crutch of large safety stocks in inventory be removed. Success is dependent upon continuous improvement, performance rewards to suppliers, and employee involvement at all levels, and is further dependant upon fast, effective communication and feedback--key factors in achieving manufacturing excellence.

ZERO DEFECTS PROGRAM

The final program is that of zero defects, but as you can see, this has a lot to do with the interrelationship of quality and manufacturing. The points I wish to stress, however, are those of commitment, the attitude of prevention rather than cure, and above all cooperation and teamwork. If these are in place, then permanent fixes will follow.

The three programs that have just been outlined clearly cannot be applied to a large vendor base. Essential in their success is the reduction in the number of suppliers and restricting the implementation of the programs to those key vendors crucial to long-term success.

They are programs that place a performance and responsibility demand on a vendor and, as with any marriage, give and take must exist. The vendor must be motivated to comply with the program requirements. Vendor motivation can be achieved simply and easily by early involvement in helping to define the programs themselves as well as in the product development and design phase. The supplier contribution in the design phase must be considered essential to assure quality, cost, and delivery targets. And, the involvement can only be complete if free and open sharing of both business and technical information prevails. The final point of performance reward is perhaps the most important. Performance rewards must be continuous and forthcoming. Broken promises for whatever reason are the biggest demotivator.

In closing, the final issue is that of vendor selection. How do you limit the number of world-class suppliers you buy from and at the same time open the door to innovative start-ups that can perhaps provide that competitive edge? The list of criteria here is by no means exhaustive, but represents what we at Dataquest consider to be some of the most important.

In the selection of large companies, consideration must be given to whether they:

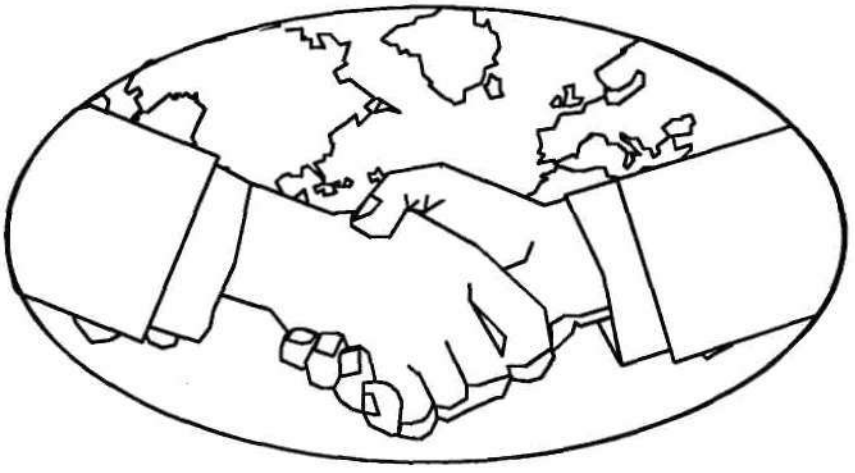
- Cover all or most of the product categories needed
- Serve the geographic areas in which you plan to buy

- Have already made alliances with your competitors
- Can provide product design support

For the small company, the emphasis is slightly different. Consideration must be given to:

- What kind of backing exists?
- What is quality of their management team?
- Do they have an international outlook?
- What was the founder's motivation for starting the company? Get-rich-quick or founding a dynasty?

However, the most important of all in choosing a suitable vendor for a strategic alliance is: make sure he chooses you.



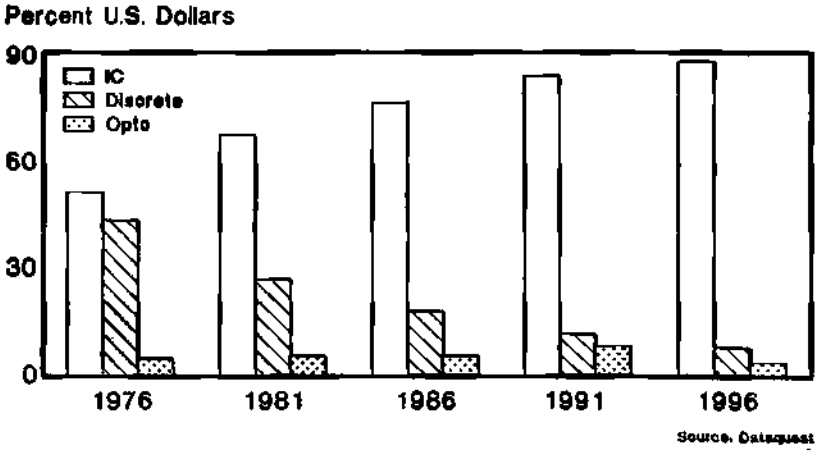
STRATEGIC PARTNERING

VENDOR-CUSTOMER RELATIONSHIPS

- Strategic partnering
- Objectives
- Obstacles
- Vendor motivation

AN INDUSTRY IN TRANSITION

ESTIMATED WORLDWIDE SEMICONDUCTOR CONSUMPTION



THE FUTURE BUSINESS CLIMATE

- More complex devices
- In-house design
- Dominant technology - CMOS
- Learning curve pricing
- Surface-mount packaging
- Alliances with fewer vendors, but . . .
- Many more vendors to choose from
- More companies buying semiconductors

THE OBJECTIVES

PROCUREMENT OBJECTIVES

- Cost reduction by improving:
  - Quality
  - Lead time
  - Delivery
  - Flexibility
  - Price

PROCUREMENT OBJECTIVES

- Cost reduction
- Make a contribution to profits
- Manage supplier relationships
- Communicate expectations and performance results
- Assume a leadership role:
  - Internal/external communications
  - Sourcing of new technology
  - Influencing supplier selection
  - Assuring accurate specifications

VENDOR OBJECTIVES

- Early participation in product development and design
- Performance reward (sole source)

THE OBSTACLES

- Communication of objectives
- Measurement of performance
- Methodology to define cost of ownership
- Product complexity
- Visibility
- Corporate acceptance/support

COLLECTIVE OBJECTIVES

- Development of monitoring process
- Continuous improvement
- Collaborative action plans
- Development of superordinate goals

KEY ELEMENTS OF PROGRAMS

- Quality programs
  - Specification agreement
  - Closed-loop corrective action
  - Statistical process control
  - 100% performance to specification goal
  - Continuous improvement
  - Ship-to-stock
  - Common quality program for all plant locations

KEY ELEMENTS OF PROGRAMS

- Manufacturing programs
  - Just-in-time
  - Inventory goals
  - Performance rewards
  - Employee involvement

KEY ELEMENTS OF PROGRAMS

- Zero defects programs
  - 100% conformance
  - 100% lot acceptance
  - 100% on-time delivery
  - Commitment
  - Prevention orientation
  - Cooperation/teamwork
  - Permanent fixes

VENDOR MOTIVATION

- Participation in product development and design
- Free and open sharing of information
- Performance rewards

VENDOR SELECTION CRITERIA

Large companies

- Product portfolio
- Geographic representation
- Other alliances
- Support

VENDOR SELECTION CRITERIA

Small companies

- Financial backing
- Management
- International perspective
- Founders' motivation

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1986 EUROPEAN INTEGRATED CIRCUIT SEMINAR--IC OUTLOOK '87

September 15 ☐ 16 ☐ 17 ☐ 18 ☐ 19 ☐ 22 ☐ 23 ☐
(Check today's date)

Evaluation Questionnaire

Thank you for attending IC Outlook '87. Please assist us in planning our next seminar by completing and returning the questionnaire.

1. How would you rate the seminar on a scale of 1 to 10 (where 10 is the highest in terms of your approval)?
   Content _____ Delivery _____ Format _____ Location _____
   Comments _____

2. How would you rate the seminar facilities (1 to 10)?
   Location _____ Meals _____ Meeting Room _____

3. How would you rate the following sessions (1 to 10)?
   Worldwide Business and Technology Trends _____
   European Industry Update _____ ASICs and Logic _____
   Memory Review _____ Microprocessors _____
   Packaging Review _____ Vendor-Customer Relationships _____

4. How did you find out about this seminar? _____

5. What were your objectives in attending? _____
   _____

6. To what extent were your objectives met (1 to 5) (1 = not at all, 5 = completely)? _____

7. What other topics would be of interest to you in future seminars of this type? _____

8. Would you prefer a seminar that is longer ☐, shorter ☐, or same length ☐ ?

9. Would you attend IC Outlook '88? Yes ☐ No ☐

10. Are there others in your company who would be interested in attending this type of seminar, or who should receive information about Dataquest services to the electronics industry?
    Name _____ Title _____ Phone _____
    Name _____ Title _____ Phone _____
    Address _____
    _____

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