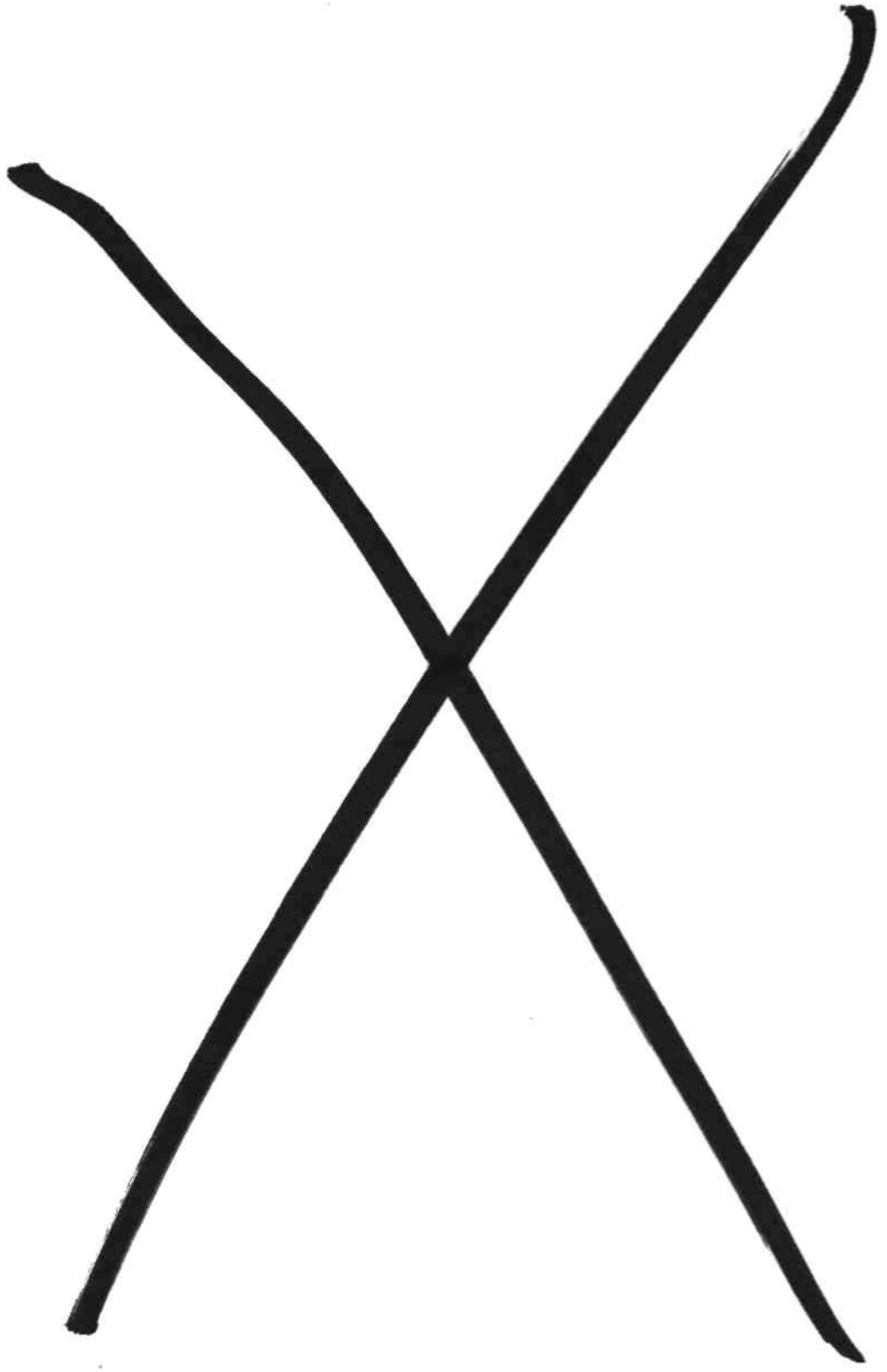

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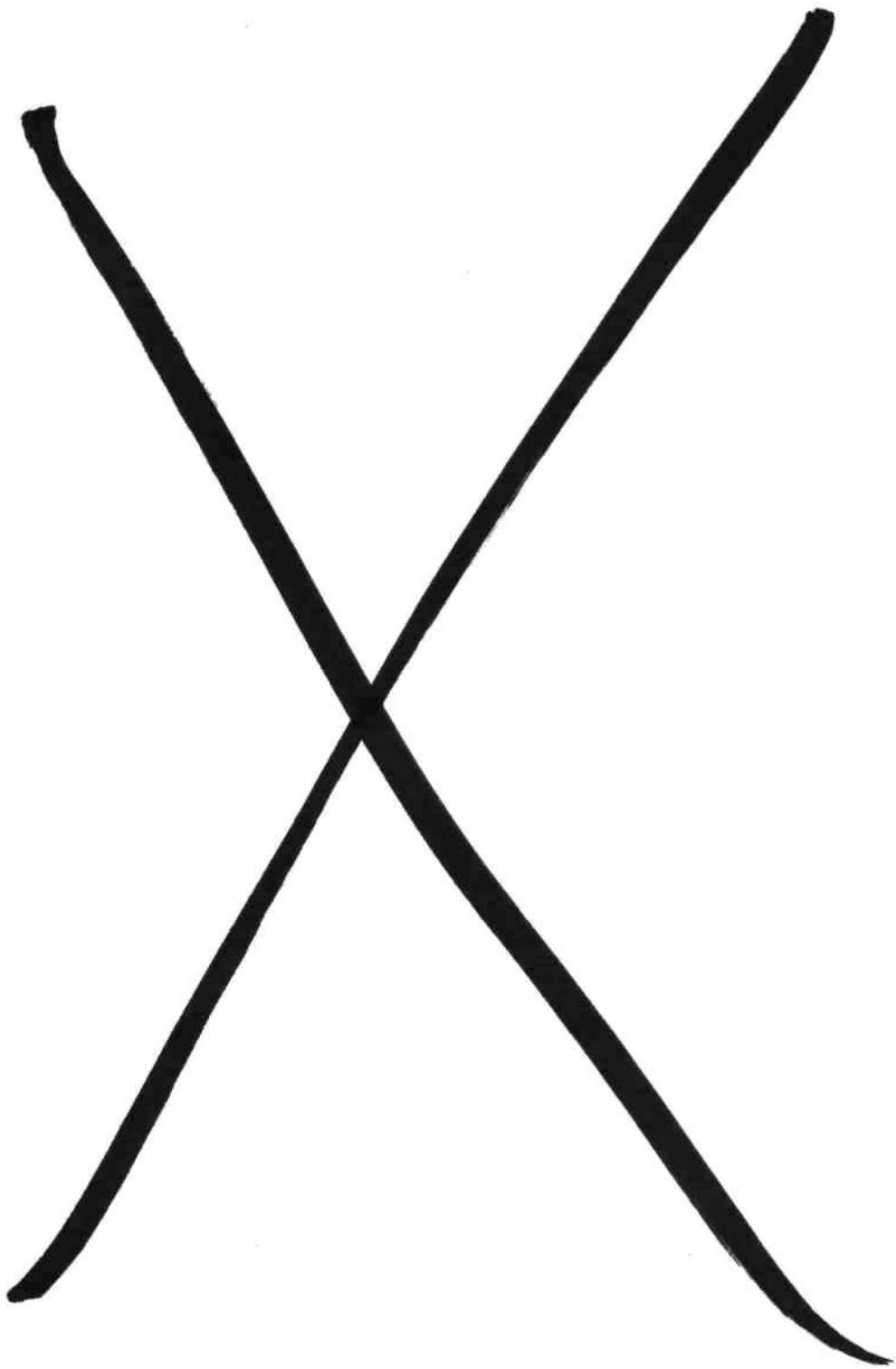


Introduction to the Service

The Semiconductor Industry Service is a comprehensive, worldwide information service that documents and analyzes all important aspects of the semiconductor industry. The service consists of:

- Three, three-inch looseleaf binders containing sections that are continually revised and updated as developments occur or additional information becomes available
- Newsletters reporting on significant industry developments in a timely manner
- Unlimited free inquiry privileges for answering questions and obtaining back-up information
- An annual three-day conference with industry experts discussing developments of current interest and importance

The Service analyzes and reports on the products, markets, and major companies in the semiconductor industry on a worldwide basis and assesses the effects of developments in products and processes, new competitors, and other changes in the market. To answer questions on the industry, the Service will:

- Identify and quantify market trends
- Analyze growth-stimulating and growth-restricting factors
- Provide detailed perspectives on new technologies
- Evaluate relative company positions
- Compare and analyze pricing policies
- Discuss marketing channels, strategies, and related operational aspects
- Discuss semiconductor manufacturing technologies and trends
- Provide perspective on electronic distribution
- Estimate market shares for all participants
- Describe relevant aspects of all major industry participants, including: research and development and marketing activities; product lines; competitive strengths and weaknesses; financial capabilities; international operations
- Assess the impact on the industry from such external influences as materials and energy shortages, economic and monetary trends, tariffs, and competing technologies

Introduction to the Service

NEED FOR THE SERVICE

The rapid growth that has occurred in the semiconductor industry has not been matched by a growth in detailed, comprehensive, and timely analytical and reporting services. No official body in the United States--government organization, industry association, or trade publication--maintains complete or even near-complete statistics on the semiconductor industry. Thus, industry data must be gathered from a wide variety of sources and carefully assembled to make them as meaningful and accurate as possible. Similarly, although certain other countries have either active trade or detailed government statistics, adequate data in a usable form are not generally available. The Service seeks to fill this gap through publication of information—in a convenient format—collected during DATAQUEST's continuous industry coverage. The size and capabilities of our staff and other resources permit us to publish analyses never before available, and to expand and update them as the industry evolves.

We believe that the Semiconductor Industry Service will serve as the industry standard for classifying products and markets into a usable reference structure. We have made every possible effort to organize the Service in a manner useful to a broad range of industry participants and analysts. Furthermore, we have endeavored to select and consistently use popularly accepted terminology whenever possible. Finally, we have attempted to make the service a "living," working entity through: (1) the flexibility of the updated, looseleaf binders; (2) very detailed market breakdowns that permit easy recombination or customized analyses by subscribers; (3) complete and precise definitions of all categories treated so that the exact scopes are clear; (4) careful statement of assumptions and forecasting approaches; and (5) maximum attention to format, graphics, and topic organization to ensure rapid search, easy reading, and clear interpretation.

SERVICE STRUCTURE AND TERMINOLOGY

Detailed discussions of technologies, products, markets, competition, and companies have been broken down in three separate ways:

- By product type (also used as the basis for market segmentation)
  - Discrete
    - Optoelectronic
  - Integrated Circuit
    - Digital
    - Linear
    - MOS

- By geographical region
  - North America
  - Western Europe
  - Japan
  - Rest of World
- By time period
  - Individual years 1970, 1971, . . . , 1985

An alternate to market segmentation by product type is a breakdown according to typical user need. This breakdown is referred to as a classification by "user application area." It comprises the following major areas with some typical smaller segments:

- Industrial
  - Communications
  - Instrumentation
  - Process Control & Data Acquisition
  - Office Equipment
- Computer
  - Memories
  - Microprocessors
- Consumer
  - Audio
  - Video
  - Automotive
  - Calculators
  - Appliances
  - Games
  - Cameras
  - Watches
- Government and Military

We will refer to this breakdown when describing markets from the user's viewpoint, but will not use it for detailed numerical estimates.

In order to provide a basis for correlating our market data that is maintained in terms of consumption with historical data gathered by industry associations—such as the Semiconductor Industry Association (SIA)—and government agencies, we have segmented worldwide production (factory shipments) by geographical region. This data is presented in the Service primarily to assure overall consistency rather than to serve as a basis for market projections.

Introduction to the Service

SERVICE ORGANIZATION AND CODING

To minimize difficulties in updating and reference search, DATAQUEST has developed a fairly rigid organizational hierarchy and associated coding for the individual components that make up the entire set of binders. As shown in Table 0.1-1, we will consistently refer to the largest components of the Service as Chapters, Chapters are divided into Sections, and Sections are divided into Subsections.

Numerical codes have been used down the hierarchy only through the section level. A typical code to designate a section is A.B, where A represents the chapter and B represents the section. For most of the sections, the letters A and B can be replaced by a single digit, because ten categories are usually sufficient to cover all the possibilities at that level. The coding structure permits the letters A and B to stand for two or more digits, however, because the period serves as an absolute delimiter.

For referring to pages, tables, and figures, we have used references of the form A.B-pp, A.B-tt, and A.B-ff. The designations pp, tt, and ff represent the serially numbered pages, tables, and figures, respectively, within a section.

SERVICE FEATURES AND PROCEDURES

Because of the large quantity of printed information that will be available for insertion, the binders are actually a multivolume set. A volume number appears on the spine of each volume. Section dividers are included for easy reference, with new ones added as new material is added to the notebook.

The date of preparation is noted on the bottom of each page. When there are major revisions, entire sections or subsections will be updated. Each new version replaces the earlier one in its entirety, and is entered into the book according to the codes appearing within the page numbers. (Actually, with the numerical design of the codes, if the entire notebook of material somehow becomes completely scrambled, it can be rearranged in ascending numerical order.) With minor changes or corrections, only the page or pages affected are changed. If the additions or replacements are not obvious, they are accompanied by an instruction sheet.

Newsletters take two forms--reports and analyses. Those newsletters that contain information of a general reporting nature such as trade show reviews, meeting summaries, mergers, shifts of personnel, etc., are intended for current news and will be utilized in later analysis and updating of sections or subsections. Newsletters are coded for filing in accordance with the basic service organization until complete updates of the affected section are prepared.

Introduction to the Service

The inquiry privilege permits subscribers to contact DATAQUEST by mail, telegram, telephone, TWX, or in person, to ask for copies of printed material, data, or opinions on topics covered in the Service. With the exception of confidential or proprietary material, DATAQUEST's complete files on the semiconductor industry—as well as its entire staff of electronics specialists—are available to subscribers.

Our annual three-day conference covers topics of timely interest and importance. Programs include outside speakers, panel discussions, and demonstrations. Participants have the opportunity to mingle with skilled industry specialists.

Because we wish the Service to be responsive to industry needs, we welcome suggestions for changes. We will periodically poll all subscribers to determine the topics that should be given priority, or new ones that should be added.

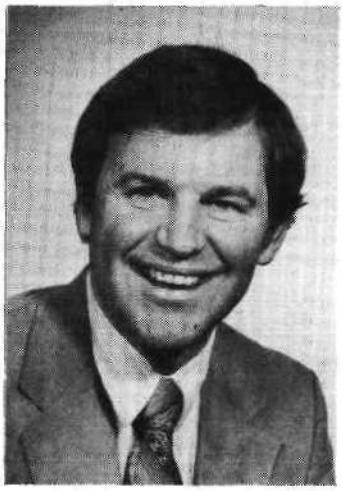
Table 0.1-1

SERVICE ORGANIZATION AND CODING STRUCTURE

Component Name	Component Code	Component Heading Format	
		Description	Example
Chapter	A	Divider only or running head, centered at top of page	**3 Manufacturing** or **3 Manufacturing**
Section	A.B	Running head, centered at top of page	**3.4 Plant Construction**
Subsection (Level 1)		Upper case, flush left, underscored	FLOOR PLAN
Subsection (Level 2)		Upper/lower case, flush left, underscored	United States
Subsection (Level 3)		Upper/lower case, indented 5 spaces, underscored	North America
Subsection (Level 4)		Upper/lower case, indented 5 spaces, underscored, space, hyphen, space, followed by text on the same line	Market Estimates - Text

Introduction to the Service

SERVICE STAFF



Howard Z. Bogert

Mr. Bogert is responsible for assessing the impact of new technologies on the semiconductor, equipment, and product markets. Mr. Bogert has been with DATAQUEST for more than three years. During his 23 years in electronics, he has held management positions in market research, product planning, long-range planning, research and development, and engineering. Most recently, he was a divisional vice president of engineering for Rockwell International. Earlier he was director of MOS development for Siliconix. Mr. Bogert holds a B.S. degree in Electrical Engineering from Stanford University, an M.S. degree from the University of Maryland, and an M.B.A. degree from the University of Santa Clara.

Mary Ellen Hrouda

Ms. Hrouda has been a Research Associate for DATAQUEST's Semiconductor Industry Service for three years. She is responsible for computerized database maintenance of market share data, client inquiries, and research newsletter writing. Ms. Hrouda received a B.S. in Natural Science from Johns Hopkins University.

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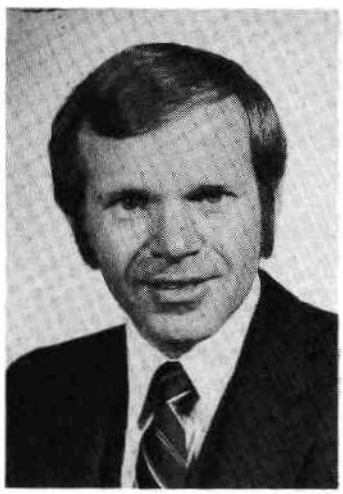


Daniel L. Klesken

Dr. Klesken is Director of DATAQUEST's Semiconductor Industry Service. He specializes in the areas of semiconductor memory, microprocessors, major users of semiconductors, applications, and strategic planning. Prior to joining DATAQUEST in July 1976, he was with Texas Instruments for nine years as a member of the technical staff. At TI he was in the Central Research Laboratories where he did corporate strategic planning and market research as well as system applications for magnetic bubbles and charge coupled devices. His earlier research was in the area of computers and digital communications systems. Dr. Klesken received his B.S. and M.S. degrees in electrical engineering from Lehigh University and a Ph.D. in electrical engineering from Carnegie-Mellon University.

F. Lane Mason

Mr. Mason is a Research Analyst for DATAQUEST's Semiconductor Industry Service. He has been with DATAQUEST for three years, during which time he has gained increased responsibility for coverage of MOS memory and microprocessor markets, company analyses, and capital spending, as well as general research support. Mr. Mason's experience lies outside the semiconductor industry, having worked formerly for Hughes Aircraft and Raychem Corporation. He has a B.S. in physics from the California Institute of Technology, and has done graduate work at UCLA in the Department of Economics.

Introduction to the Service

Kenneth V. McKenzie

Mr. McKenzie is a Senior Research Analyst for DATAQUEST's Semiconductor Industry Service. He is responsible for all research in the microprocessor and microcomputer component markets. His other duties include the Semiconductor Industry Service internal data processing coordination and research into specific end-user markets. During Mr. McKenzie's 14 years in the electronics industry, he has held management positions in both design engineering and marketing. His last position was as Component Marketing Manager at Zilog, Inc. Prior to that, Mr. McKenzie was Marketing Manager for 8-bit microprocessor families at Intel Corporation. His educational background is in electrical engineering, computer science, and business administration.

Jean C. Page

Mrs. Page is a Research Assistant for DATAQUEST's Semiconductor Industry Service. She provides general research support for the Service, focusing on the West European semiconductor market. Before joining DATAQUEST, Mrs. Page worked for ten years in libraries and in the formation of research departments and spent one year in Switzerland as a technical translator. Mrs. Page studied library science at the North-Western Polytechnic in England and holds a B.A. in English from the Open University, also in England.

Introduction to the Service

Susan A. Thomas

Ms. Thomas is a Research Assistant for DATAQUEST's Semiconductor Industry Service. She provides general research support, focusing on the equipment and materials industry. Ms. Thomas' previous experience is in publishing. Most recently, she was a reporter for the San Francisco Business Journal. Ms. Thomas was graduated with an A.B. degree in English from Occidental College, where she was elected to Phi Beta Kappa.

Frederick L. Zieber

Mr. Zieber is Director of DATAQUEST's Semiconductor Industry Service. He has ten years of experience in market research and consulting to the semiconductor industry. Previously, Mr. Zieber had nine years' experience in the semiconductor industry at Siliconix where he was product line manager for MOS Analog Switches. He has experience in integrated circuit and discrete device processing, design, manufacture, and testing. He holds two patents in semiconductor processing. Mr. Zieber has a B.S. degree in Electrical Engineering from Stanford University and an M.B.A. degree from the Graduate School of Business at Stanford University.

Introduction to the Service

Semiconductor Industry Staff Capabilities

The DATAQUEST Semiconductor Industry Service staff has a continuing, long-term commitment to the semiconductor and related electronic industries. The staff has in-depth expertise in all facets of the electronics industry and represents more than 80 years of industry and consulting experience within the industry.

Members of the DATAQUEST professional staff are frequent speakers at industry seminars and symposia. We participate in the leading professional societies related to the electronics industry. We maintain contact with a large user base through sophisticated sampling and interviewing techniques. Our staff regularly reviews all important publications related to the semiconductor industry and associated user industries.

Consulting Studies

Members of DATAQUEST's Semiconductor Industry service staff are consultants to many of the major semiconductor and related industries companies in the United States and abroad. Primary engagements have involved manufacturing cost and facility evaluation, market forecasting, and product potential evaluations. Other engagements have included acquisition studies and competitive analyses.

DATAQUEST will respond to requests for proposals that involve those areas of semiconductors and related electronics in which the staff has expertise.

SUBSCRIPTION TERMS

Basic Terms

The Service begins on the date of the first billing. At that time, the subscriber receives three, three-inch binders containing complete, up-to-date material and copies of all recent newsletters. For the duration of the subscription, the subscriber receives a copy of each additional or replacement section of the notebook and each newsletter published. The inquiry privilege may be utilized as often as desired. Subscribers are invited to send one participant to the annual seminar. (Additional participants may be sent for a moderate fee.)

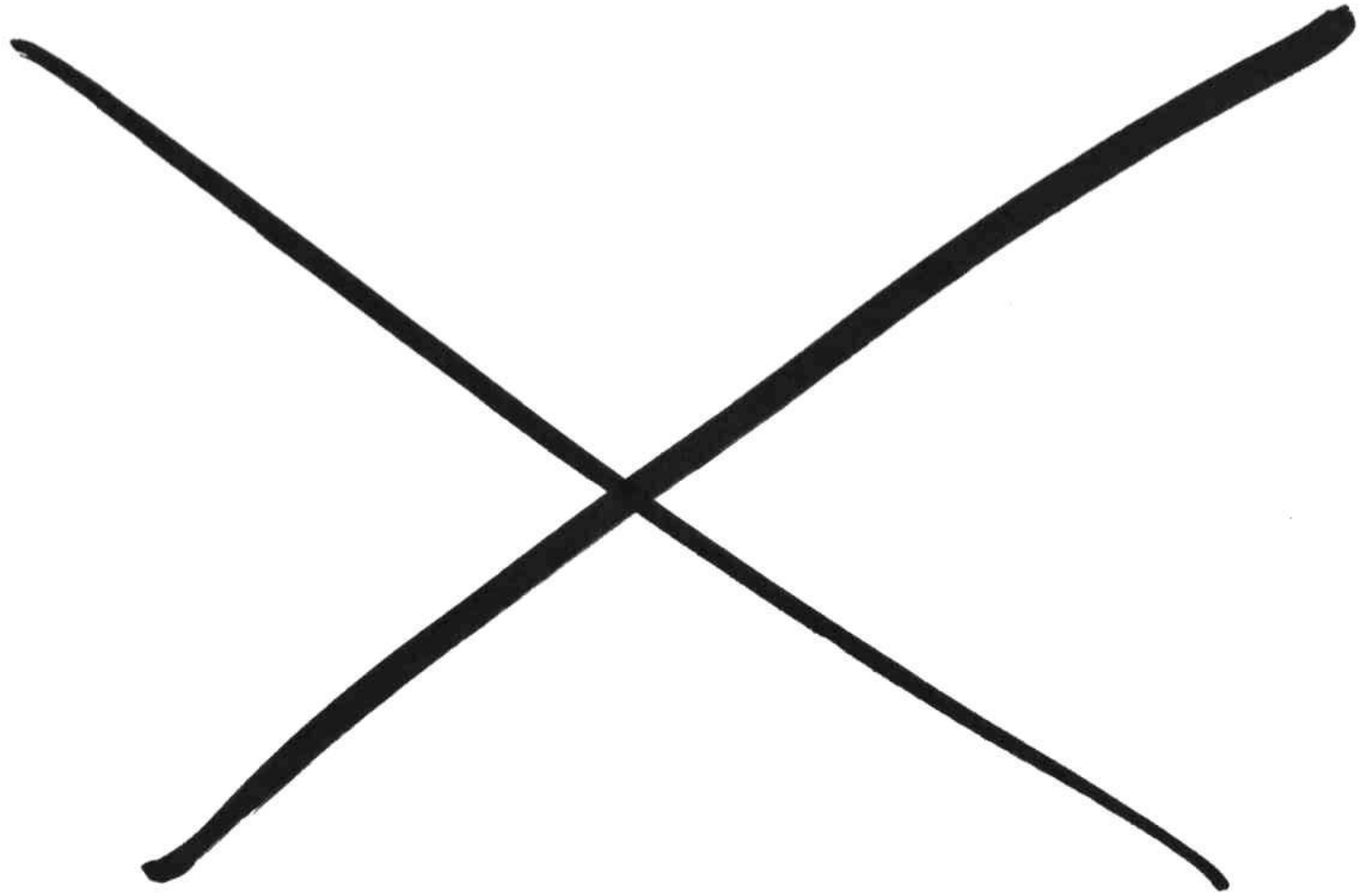
Add-On Subscriptions

Subsidiaries, divisions, regional offices, majority owned affiliates, and parent companies of the subscribing organization are eligible for "add-on" subscriptions

at a low percentage of the base price for each additional subscription. These add-on subscriptions include complete copies of all published material, full inquiry privileges, and seminar attendance.

Base Price and Payment Terms

Industrial clients will be billed for the full price of the service on an annual basis. DATAQUEST reserves the right to raise its subscription prices to reflect broadened scope or increased costs. Subscribers will be notified in advance of any such price increase.



1.0 Scope

The semiconductor industry is one of the cornerstones of modern industrial society. Semiconductor devices are the basic components of computers and other data processing equipment, telecommunications, industrial automation, television and radio, defense electronics, and other important products. Both directly and indirectly, semiconductor devices are important in nearly every facet of our lives.

In 1979, the worldwide market for semiconductor devices, including captive suppliers, exceeded $10 billion. The industry supplied literally billions of devices consisting of thousands of types of individual products—including diodes, transistors, integrated circuits, and optoelectronic devices. Despite their wide diversity, these products share the common bond that their basic electronic functions are performed by semiconducting materials. This commonality provides a clear definition for the industry.

More than 160 companies actively compete in the semiconductor industry worldwide. Many of these companies are small, and production of semiconductors is not yet highly concentrated among a few companies. However, at least 20 concerns manufacture in excess of $100 million in semiconductors annually. Major U.S., European, and Japanese manufacturers of semiconductors are shown in Table 1.0-1.

The purpose of this chapter is to provide a basic description of the semiconductor industry, including its structure, special characteristics, important trends, and special problems the industry faces.

1.0 Scope

Table 1.0-1

MAJOR WORLD SEMICONDUCTOR MANUFACTURERS

United States

- AMD
- General Electric
- General Instrument
- Honeywell
- IBM
- Intel
- ITT
- Mostek
- Motorola
- National Semiconductor
- RCA
- Signetics
- Texas Instruments
- Western Electric

Europe

- AEG-Telefunken
- Philips
- SGS-ATES
- Siemens
- Thomson-CSF

Japan

- Fujitsu
- Hitachi
- Matsushita
- Mitsubishi
- Nippon Electric
- Toshiba

Source: DATAQUEST, Inc.
June 1980

1.1 History

The semiconductor industry is less than 30 years old. Although some simple diodes had been manufactured earlier, the first transistor was produced by Bell Laboratories on December 23, 1947. Technical breakthroughs in the manufacture of transistors followed rapidly, and by 1952 a number of companies were producing devices commercially. These devices, however, were made using germanium as the semiconductor material.

In 1954, Texas Instruments (TI) began to manufacture silicon transistors on a commercial scale. (Prior to that time, TI had not been a factor in the semiconductor industry.) In the late 1950s, the industry was still in its infancy with sales just beginning to pass the $100 million mark. The major market for semiconductor devices was provided by the military, which had seen the potential of semiconductors and actively supported the industry's development. Another large market, of course, was for transistor radios.

In 1959, Fairchild Camera and Instrument developed the planar technology for making transistors, which later became the basic technology for the manufacture of integrated circuits (ICs). Integrated circuits themselves were not commercially produced until 1961, when they were first marketed by Texas Instruments. About the same time, a wider proliferation of many different types of semiconductor devices began, including the development of MOS devices, junction field effect transistors, and Schottky diodes. At this time, several improvements in manufacturing technology also occurred, providing rapid increases in productivity and device reliability.

In the late 1960s, the use of integrated circuits grew rapidly and by 1965 worldwide industry sales had passed the $1 billion mark. This period also marked a proliferation in uses for semiconductor devices, including many markets for industrial products, data processing devices, and communications equipment. During this time, MOS devices also began to be sold on a commercial scale. U.S. companies began to assemble their products overseas and both the European and Japanese markets became important. In 1968, the first light-emitting diodes were sold commerically by Hewlett-Packard following their development by Bell Labs four years earlier.

The late 1960s and early 1970s marked some major changes to the semiconductor industry. During this span, over 36 new merchant companies were begun. At the same time, many captive semiconductor facilities emerged. These new companies added technical and competitive impetus to an already fast-moving industry. This period also saw the rapid rise of MOS integrated circuits as a major product area in the semiconductor industry. Major products to emerge included semiconductor memory, custom devices, complex linear circuits including operational amplifiers, voltage regulators, A to D and D to A convertors, and others. The early 1970s marked the advent of large scale integration (LSI) devices, and uses for consumer devices such as calculators and watches. An era of low-cost electronics was emerging.

The late 1970s saw the emergence of a large worldwide semiconductor industry, with competition on an international scale. The emergence of very large scale integration (VLSI) devices brought important new products, including microprocessors. Other major new devices included various types of customizeable semiconductors such as ROMs and EPROMs. A history of technical milestones in the semiconductor industry is given in Chapter 4, Technology; Section 4.16, Impact of Technological Change, of the Semiconductor Industry Service notebooks.

1.1 History

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1.2 Structure

PRODUCTS

The semiconductor industry has a wide diversity of products. The most basic breakdown consists of integrated circuits (ICs), discrete devices, and optoelectronics. An integrated circuit is a single chip that has more than one active device on it. For example, it may have a number of transistors, diodes, resistors, or capacitors as part of the electronic circuit. Integrated circuits vary widely according to the functions that they perform and the technologies used in their manufacture. Circuits can perform digital or linear electronic functions and be based on a number of basic technologies, such as that for bipolar transistors or MOS transistors. ICs can be configured to an almost limitless number of different types of circuits.

Discrete devices have an even wider diversity. They consist of many types of transistors, diodes, and switching devices such as SCRs and triacs. Again, the wide diversity of product applications requires tens of thousands of types of discrete devices. This product diversity requires many variations in manufacturing.

A description of many of these products is provided in Chapter 4, Technology, of the Semiconductor Industry Service notebooks.

Products fall into three general classifications:

- Custom
- Standard
- Commodity

A custom device is basically designed and manufactured for a single customer. In general, only a limited quantity is manufactured, the price is relatively high, and the technical attributes are specifically designed to meet the customer's needs.

A standard device is a semiconductor that is offered to the general marketplace. These devices are intended by the manufacturer to meet the application requirements of many users. The quantities of standard devices manufactured depend on their acceptance in the markets for which they are intended.

A commodity device is a semiconductor that has been universally accepted and is produced in high volume by more than one manufacturer. This type of device is usually characterized by high volume, low cost, and relatively low margins.

Only within the past few years have a significant number of integrated circuits become commodity products. The emergence of commodity devices marks a major advance in the maturity of semiconductor markets. In general, these products are manufactured by the larger companies which have a competitive edge in volume efficiency. Custom devices, on the other hand, are often produced by small manufacturers that are competitive within a niche for a particular product or technology.

In recent years, a number of customizeable, or user-programmable, devices have emerged, including PROMs, EPROMs, EAROMs, programmable microprocessors, gate

arrays, and field programmable logic arrays. These devices can be programmed electrically or by design of the last interconnect stage of wafer fabrication. In general, they reduce the design time and effort needed to customize a semiconductor product.

MARKETS

The semiconductor industry has four major end-user markets:

- Consumer
- Industrial
- Computers
- Government and military

Although each of these markets is separate, the division should not be overemphasized, because most products are useful in more than one market, and manufacturers rarely specialize in a single market.

The consumer market includes entertainment items (such as radios and televisions), cameras, watches, automobiles, calculators, appliances, electronic organs, games, toys, and video games. Most applications in this market are fairly recent developments, with the exception of radios which supplied one of the first markets for semiconductors.

The industrial market consists of a wide variety of industrial applications, including noncomputer electronic data processing (EDP) applications, office equipment, industrial process control equipment, communication equipment, test and instrumentation equipment, various power or current switching applications.

The computer market includes devices used for computers, minicomputers, peripheral devices such as terminals, and associated memory storage. Microcomputers are a new and growing segment of this market.

The government and military market is the oldest of the semiconductor markets. Prior to the mid-1960s, this market accounted for the majority of semiconductor sales. Devices for this market generally require special handling and testing, special packaging, and unusually high reliability. Moreover, demand is often limited and prices are generally considerably higher than those of other markets.

WORLD MARKET SHARES

United States companies have always supplied a majority of the semiconductor devices produced in the world, and this dominance is increasing. For several years, U.S. companies gradually lost market share to European and Japanese manufacturers and, in 1970, the share of the world semiconductor market controlled by U.S.

companies reached its lowest point. Since that time, the market share of U.S. companies has been relatively stable, despite devaluation of the dollar. In 1974, U.S. companies controlled an estimated 62 percent of the total world semiconductor market and about 75 percent of the total world integrated circuit market (more than 80 percent including captive manufacturers). Table 1.2-1 shows the percentage of the world's semiconductor market that is supplied by U.S., European, and Japanese companies.

Table 1.2-1

ESTIMATED SEMICONDUCTOR MARKET SUPPLIED BY U.S., EUROPEAN, AND JAPANESE COMPANIES

(Percent)

Year	U.S.	European	Japanese
1970	56.5%	16.1%	27.1%
1974	62.3%	16.3%	20.7%
1975	63.9%	16.7%	19.3%
1976	60.4%	14.9%	24.5%
1977	60.0%	14.2%	25.6%
1978	58.6%	12.9%	28.4%
1979	60.9%	13.2%	25.6%

Source: DATAQUEST, Inc.
June 1980

United States companies are positioned in the fastest growing semiconductor market segments. They have a much larger share of the integrated circuit market than they do of the discrete market. United States companies have their largest integrated circuit sales in MOS devices, and nearly as large a market in bipolar digital devices. Since the integrated circuit market is growing faster than the discrete market, the market segments now served by U.S. companies will ensure that their current share of the total world semiconductor market will not rapidly diminish.

However, as U.S. companies have transferred more and more manufacturing to foreign plants, the transfer of technology has been more rapid and the technical superiority held by U.S. companies has been diminishing. In addition, a number of

factors mitigate against the market advantages of U.S. companies. These factors are often cultural or political, spurred by nationalistic feelings. Foreign governments have attempted to set up strong barriers to increased market dominance by U.S. companies and to provide advantages to local companies. Such barriers include strong pressure on users to purchase from domestically owned companies (especially in the military market), direct and indirect subsidies, high tariffs and duties, import quotas and restrictions, and other forms of government control. Because of these strong pressures, it is unlikely that U.S. companies will increase the share of the world integrated circuit market that they now hold.

It should be noted that the data mentioned above include only noncaptive manufacturers. IBM and Western Electric, which have a combined estimated output of more than $800 million in semiconductors, are not included. If the production of captive companies is included, the market controlled by U.S. companies becomes significantly higher.

The major markets supplied by the semiconductor manufacturers have a large number of different applications which result in an extremely large number of smaller market segments. The smaller markets often require special types of devices with unique technologies or specialized applications. This situation creates opportunities for many small companies to be both competitive and profitable.

With a few exceptions, semiconductor devices are sold to manufacturers that design, assemble, and market the end products. Thus, the vast majority of semiconductors are sold to other industrial manufacturing corporations rather than used internally.

Major users of semiconductors are given in Appendix C of the Semiconductor Industry Service notebooks. A quantitative analysis of major semiconductor markets is given in Appendix D.

MANUFACTURING

The central focus in manufacturing in the semiconductor industry is the fabrication of the semiconductor device from an extremely thin, raw silicon wafer, about four inches in diameter. This process entails hundreds of individual manufacturing steps, each requiring complex technology and high precision. The manufacture of the semiconductor device can be divided into three major operations: wafer fabrication, testing, and assembly. A complete description of semiconductor fabrication is found in Chapter 3, Manufacturing, of the Semiconductor Industry Service notebooks. Process variations among the different types of semiconductors are included in Chapter 4, Technology.

In the semiconductor industry, all manufacturing steps are usually performed by a single company, which also markets the devices. As a result, the industry is structurally simple. Differences occur from company to company, however, in the amount of integration of support functions. Integration includes fabrication of the

package in which the devices are assembled, manufacture of the semiconductor wafers on which the devices are made, manufacture of the masks involved in the photolithographic process, and other functions. Larger (or older) companies, such as IBM or Texas Instruments, operate on this greater level of backward integration. Smaller (or newer) companies, in general, do not perform these manufacturing functions. For example, Intel purchases masks, wafers, and packages. The unified manufacturing structure of the industry—from wafer to final product—results from the close interrelationship of the technology of the various manufacturing steps.

In recent years, there has been a proliferation of companies offering various semiconductor manufacturing services. These services include semiconductor device design, mask making, semiconductor wafer fabrication (wafer foundries), assembly and packaging services, and testing services. This vertical disintegration has made it possible to control design, manufacture, and market semiconductors without a significant investment in manufacturing or engineering manpower. These companies serve the needs of manufacturers and users alike to design and make various custom devices.

DISTRIBUTION AND MARKETING

Semiconductor devices are sold and distributed in three basic ways:

- Through a direct sales force, with shipment from the manufacturing company
- Through a sales representative organization with shipment from the manufacturing company
- Through a distributor with shipment from its own stocks

Historically, semiconductor companies have preferred to market directly whenever possible, especially to larger users. However, a direct sales force cannot market economically to smaller users or in areas where sales volumes are low, so that direct selling represents a large fixed cost. As a result, many companies have turned increasingly to manufacturers' representatives (Reps). These organizations may handle several companies with nonconflicting product lines. Generally, a representative organization receives a higher commission than does the direct sales force. However, for small companies that cannot economically maintain a direct sales force, this approach is a viable alternative.

Distributors generally buy semiconductor devices from companies in large quantities, under agreements with those companies, and resell them in smaller quantities at higher prices. Distributors also often market actively to many companies. They relieve the semiconductor companies of the problems associated with handling many small orders and perform a valuable inventory function for the industry, as well as some marketing functions. A detailed description of this facet of the industry is provided in Chapter 7, Distribution, of the Semiconductor Industry Service notebooks.

1.2 Structure

VERTICAL INTEGRATION

In the past, vertical integration has rarely played a role in the structure of the industry. Semiconductor companies, in general, have not integrated into the complete manufacture of an end product. Notable exceptions have been the Delco Division, which supplies General Motors, IBM, and Western Electric, which is the manufacturing arm of AT&T. Recently, there has been a trend toward increased vertical integration with more higher level products (such as board products) being offered by semiconductor manufacturers, and more captive semiconductor facilities making some devices for electronic systems manufacturers. However, the separation of semiconductor manufacturing and end-product manufacturing still prevails in the majority of cases. The variety of semiconductor devices used for most end products requires a greater diversity than a single semiconductor facility can offer.

OWNERSHIP

The ownership of semiconductor manufacturing can be divided into three broad categories: independent manufacturers, divisions of major corporations, and captive manufacturers. These distinctions are not always entirely clear, but they serve generally to identify the various types of companies. The first two groups actively compete in the merchant market, and the latter does not.

Independent Manufacturers

Most semiconductor manufacturing (about 80 percent in the United States) is performed by independent manufacturers. By definition, the semiconductor operations of these manufacturers constitute a major portion of their businesses. Companies in this category include Advanced Micro Devices (AMD), Intel, Motorola, National Semiconductor, and Texas Instruments. There are a very large number of smaller companies, both publicly and privately owned, in this category. Between 1968 and 1971, more than 30 new semiconductor companies were formed.

A basic characteristic of these companies is that their survival depends on their performance in the semiconductor industry. As independent companies, they do not have either guaranteed markets or financing. In general, they are competitive, aggressive, and leaders in bringing new technologies to the marketplace. Moreover, they have been leaders in expanding the international scope of the industry, both in manufacturing and in marketing.

Divisions of Major Corporations

Many major corporations in the United States, Europe, and Japan have divisions that manufacture semiconductor devices. These divisions are distinct from totally captive manufacturing in that they actively market their semiconductor products. In some cases, they do not supply products directly to the parent corporation, although many of them do. Most such organizations, however, derive only a minority of their

sales from captive markets. Companies with large semiconductor divisions include General Electric, Hitachi, ITT, Nippon Electric, Philips, Raytheon, RCA, Siemens, and Westinghouse.

Structurally, these organizations may be treated as a division of the parent corporation or may be organized as semiautonomous companies. For example, Mostek is set up as an independent company from United Technology Company, its parent.

These companies vary greatly in (1) their outlook toward the semiconductor industry, (2) their treatment by the parent company, and (3) their competitiveness in the industry. They may be slightly less competitive and aggressive than the independent companies, but it is difficult to generalize. All of these companies, however, can benefit from the financial resources of the parent. With the increasingly high capitalization requirements in the industry, that is a distinct advantage. Also, large parent corporations often have a sheltered market that the semiconductor division can take advantage of. On the other hand, such companies can have problems attracting talented individuals from the industry because the fast pace of the semiconductor industry frequently is at odds with slower decision-making processes of a large corporation. Furthermore, the senior officers of the parent corporations generally have little or no experience with the semiconductor industry.

Captive Manufacturers

Several companies have totally captive semiconductor facilities and make semiconductor devices for their own use, but do not market devices to industry. Major manufacturers with captive lines include Burroughs, General Motors, Hewlett-Packard, Honeywell, IBM, NCR, and Western Electric (AT&T). The existence of such captive facilities tends to decrease the market available to the companies competing in the semiconductor industry. However, many captive facilities provide services and special devices not available in the marketplace, i.e., companies make what they cannot buy.

As semiconductors have become more important to major manufacturing companies, and semiconductor technology more critical to the end product, interest in captive facilities has increased. Captive facilities provide advantages to many companies in integrating semiconductor design with final product design. Moreover, there are often planning and control advantages. The ability of a captive facility to know both the future quantity and product mix of its output, and the lack of marketing costs are strong advantages.

Captive facilities have many of the same problems with which divisions of major corporations are faced: difficulty in attracting top grade technical personnel, slow decision-making processes, and changes in the technology that may outmode facilities. In the past, only a few manufacturers (e.g., AT&T and IBM) have had sufficient in-house requirements for semiconductors to support the necessary efficiencies of scale for cost-effective semiconductor manufacturing. However, this situation is rapidly changing with both the increasing scale of equipment manufacturers and the increasing solid-state content of their products. The number of companies with semiconductor purchases in excess of $100 million was 2 in 1975, 7 in 1979, and is expected to be around 50 in 1985.

1.2 Structure

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1.3 International Aspects

The semiconductor industry is highly international. Devices are manufactured and marketed throughout the industrialized world. The European market and Japanese market for semiconductors are each about one-half the size of the U.S. market, but differ from it in many important respects.

EUROPE

The European market for semiconductors amounted to an estimated $2.9 billion in 1979. About 46 percent of that market is accounted for by discrete devices, a larger percentage than for the world market as a whole. The use of semiconductor devices in Europe is heavily weighted toward industrial and TV uses with smaller markets for computer, other consumer, and military applications.

Manufacturing in Europe is performed both by European and U.S. companies. The U.S. concerns, with more than half of the market, dominate integrated circuit manufacturing. Unlike the United States, there are only a limited number of small companies in Europe and few companies in which semiconductor manufacture is the major focus. Most large semiconductor manufacturers in Europe are divisions of large industrial electronic systems manufacturers.

For a number of political reasons, many European semiconductor companies are heavily subsidized by the governments of their countries, which allows them to compete against larger U.S. companies that have lower manufacturing costs. However, the largest European companies are very effective, viable competitors. Most European companies, with the exception of Philips and Siemens, have not fully developed their international manufacturing and marketing capabilities. This limitation, together with the greater market strength and advanced technology of U.S. manufacturers, has weakened the competitive position of many European companies.

JAPAN

The use and manufacture of semiconductor devices developed very rapidly in Japan in the late 1960s, but since 1970 the Japanese market has grown at an equal pace with the world market. Japanese consumption of semiconductor devices is estimated at about $2.8 billion in 1979. In Japan, semiconductor devices are used primarily for consumer applications, with over 50 percent of all devices applied to that market. However, industrial applications have been growing rapidly in recent years.

In the past, the Japanese market for semiconductor devices has been highly protected by the Japanese government through a variety of means, including high tariffs, import restrictions, subsidies, and cultural barriers. This situation has allowed the Japanese semiconductor industry to develop successfully to maturity and viability. As a result, Japanese companies can manufacture a high percentage (estimated at about 85 percent) of the semiconductor devices consumed in the country. Japanese semiconductor technology, at all levels, is now at a par with the best in the United

1.3 International Aspects

States. A small group of five companies dominates Japanese semiconductor manufacture, although there are also many smaller companies.

In the past, foreign companies have been restricted to a minority interest in semiconductor manufacturing in Japan. Several U.S. companies established manufacturing facilities on a minority ownership basis with little success. Only Texas Instruments has been allowed to have a wholly-owned facility. Recently, however, many import and capital investment restrictions have been lifted, and foreign companies are now allowed to have wholly-owned manufacturing plants in Japan. Several major U.S. companies are now planning to establish facilities in Japan. Among European companies, Philips holds a 30 percent interest in Matsushita Electronics, and Siemens has a smaller interest in Fujitsu.

1.4 Special Industry Characteristics

The semiconductor industry has many characteristics that set it apart from other industries. For the most part, these characteristics arise from the industry's high technological dependence, intense competitiveness, and broad variety of products. These special characteristics include:

- Intense competition
- Product diversity
- High technology
- Rapid rate of change
- Cost and price reductions
- Short product life cycles
- Maturity with change

COMPETITION

The semiconductor industry has always been intensely competitive and should remain so in the foreseeable future. The effects of this competition are to make the industry aggressive, to make it readily adaptive to any change or competitive advantage, and to limit profit margins.

There are several reasons for this intense competitive situation:

- A lack of any major barriers to competition
- Low barriers to entry
- Market share advantages
- A wide range of products
- A very large number of companies
- A continual influx of new products and new markets

More than 160 companies worldwide make semiconductor products of one kind or another, although many of these companies produce only specialized products or manufacture limited lines for their parent companies. More than 90 U.S. companies actively compete in the mainstream of the industry. In addition to these companies, more than 30 European and 30 Japanese companies make and sell semiconductor devices.

In any given semiconductor market segment, there are usually many competitors from which a buyer may choose. The large number of companies may be reduced in the future, but they can exist at present because of the wide range of products in the industry. A company can specialize in a given area and have a particular advantage in manufacturing a few products. Although any competitive advantage in a product line is temporary, the diversity of products is sufficient to allow all companies in the industry to be competitive in at least some areas.

New products are continually being developed by the industry at a very high rate. Since a new product, by definition, does not have established suppliers, the company producing it can gain a short-term advantage. Thus, many small companies compete

effectively in the semiconductor industry by continually advancing the state-of-the-art technology. The same advantage of new products also applies to new markets created by these products. Nevertheless, since market share and the resulting volume production is important in the industry, particularly as markets become mature, competition is intense for market share. This situation leads to recurrent price competition which can be extremely severe.

Another reason for the large number of competitors in the industry and the severity of competition is that barriers to entry into the semiconductor industry have, in the past, been relatively low. Although such barriers as start-up costs, technology, and market entry are rising, they nevertheless remain low in comparison with many other industries. Between 1968 and 1971, more than 36 new companies were formed in the United States to compete in the semiconductor industry. Despite declining semiconductor demand in 1970 and 1971, at least 80 percent of these companies survived in one form or another and some, such as AMD, Intel, Mostek, and National Semiconductor, have been eminently successful. Increasing manufacturing and design costs have rapidly reduced the number of start-up companies for mainstream competition. However, wafer foundries and other special service areas continue to see the creation of new companies. Furthermore, increased international competition by Japanese and European companies is providing more market competitors.

A corollary to the low entry barriers to the semiconductor industry is the lack of any artificial market or manufacturing barriers that might serve to lessen competition, such as government regulation, price controls or supports, or labor union policies.

PRODUCT DIVERSITY

The semiconductor industry is characterized by an extremely wide range of products. There are several different types of transistors or other semiconductor devices whose operation is based on different physical laws. Each type of product has a large number of operating characteristics, including power-handling capability, speed, amplification level, and rated voltage. The possible design value chosen for each of these characteristics for a given product can vary over an extremely wide range, and the possible combination of product characteristics is nearly infinite. Integrated circuits have even wider diversity than discrete devices because of variations in circuit designs.

Product diversity occurs because semiconductor products have been specialized to perform distinct functions, and their design and manufacture have been optimized for those functions. Thus, there are literally tens of thousands of different products in the industry.

The extremely wide diversity of products has many important consequences for the industry. Because it allows a larger number of competitors to exist by forming a large number of specialized markets, it paradoxically increases the competition in the industry. Product diversity also decreases volume manufacture of any single product, thus inhibiting increased industry automation.

1.4 Special Industry Characteristics

TECHNOLOGY

It is important to underscore the role that technology plays in the industry. The primary products—discrete devices and integrated circuits—are, of course, technological in nature. Their concept, design, and function are the very basis of sophisticated electronics. It is also important, however, to note that the manufacture of the devices is also highly technical in all its aspects—the processes employed, the sophisticated equipment used to manufacture and test the devices, and the skill levels of all personnel concerned with the operation. Furthermore, the products in which most semiconductors are used are also highly technological.

A large scale integration (LSI) semiconductor memory is an example of this technological complexity. To be competitive in this field, a company must have a thorough understanding of the device's complex end use. Moreover, it must have the design capability and the processing technology to make the device. It must also be able to choose successfully among the trade-offs available in the various technologies to produce a successful cost-competitive product (see Chapter 3, Manufacturing, of the Semiconductor Industry Service notebooks). This understanding is fundamental to being a competitive supplier with state-of-the-art design, state-of-the-art manufacturing, and products that are useful and cost effective for the user.

Furthermore, the technological nature of the business makes timing critical. Every facet of a product—its design, its process, and its market—is viable and competitive for only a short period of time. Before that time, manufacture is too difficult, too costly, or simply not viable. After that time, the product may be obsolete.

Because of the technological intensity of the industry, research and development expenses are always unusually high compared with those in many other industries—up to 10 percent of revenues. Extensive research and development is a necessary investment for any company that wishes to remain competitive.

Nearly everyone who works in the industry must be highly trained in one phase or another of semiconductor technology. This requirement includes a large cadre of engineering specialists; managers who are trained not only in management but have a thorough understanding of the general aspects of the technology, and the technicians, supervisors, and workers who must have a thorough understanding of the equipment they operate.

A recurring problem for all companies is the threat of technological obsolescence of their products. This threat occurs not only over time, as new and improved products displace old ones, but also because at any time a completely different semiconductor technology could obsolete the products they manufacture. For example, silicon transistors replaced germanium transistors, TTL logic replaced DTL logic for integrated circuits, and NMOS replaced PMOS for low-cost memory.

1.4 Special Industry Characteristics

RATE OF CHANGE

The semiconductor industry is very dynamic; it truly suffers from "future shock." It has very rapidly changing technology, processes, products, manufacturing methods, and markets. This characteristic is perhaps the least understood and the most underrated by observers of the industry.

Improvements in the capability of semiconductors come at breathtaking speed. For example, in 14 years (1962 to 1976), the products of the industry progressed from a simple transistor, to an IC performing a simple logic function (such as a gate), to an IC performing an entire functional block of a system (such as an adder), to a one-chip calculator circuit, to a one-chip computer processor. Processing technology has changed from alloy junctions to bipolar planar technology to MOS technology—all with many alternative variations. (See Chapter 4, Technology, of the Semiconductor Industry Service notebooks for further information about past technological milestones.) Markets have changed from primarily military applications to include a wide range of industrial equipment, EDP applications, and consumer products.

The dynamic nature of the semiconductor industry is both exciting and profoundly unsettling. Products, technologies, and even companies are based on the shifting sands of technological progress. Past benchmarks are not applicable to the future. It is important to understand that this rapid rate of change is not a transitory phenomenon. Rather, it is a built-in characteristic of the industry. That is, the industry is one that is geared to change. Indeed, its dynamic nature is a more fundamental element of the industry than are the semiconductors that the industry manufactures.

Three main factors acount for the dynamic nature of the industry:

- Technological progress
- A large number of talented people
- Heavy competitive pressure

None of these factors are independent, but they work together in constant reinforcement. Because the industry is highly competitive, companies strive for improvements in technology to gain a competitive advantage, even if it is only temporary. The industry seeks large numbers of individuals with technological expertise, creative ability, and drive. These people must have the special ability to manage under the constant change that is occurring in the industry—circumstances that bewilder competent managers in other industries. However, it is the excitement and change that attract these people to the industry. In turn, their abilities add to the competitive crush and the high rate of technological progress.

Not all of the effects of this environment are positive. The change takes its toll both in people and companies, through technological obsolescence. Although the industry has made laudable progress, adaptation to the rapid change keeps industry profits low and tends to undermine any basic strength that a single company may have, so that any competitive advantage may be short-lived. Moreover, both the change and the growth in the industry create a continual financial strain for most companies.

1.4 Special Industry Characteristics

COST AND PRICE DEFLATION

One of the most remarkable characteristics of the semiconductor industry is the rapid and continual price decreases that occur. Prices of an average function in an integrated circuit have declined an average of over 40 percent per year since 1962, as shown in Figure 1.4-1. If these price changes over the past 20 years had been matched by the automobile industry, one could buy a car today for $1.00. In 1960, the average price of one transistor was over $5.00. In 1980, the cost of more than 50 transistors can be less than a penny when purchased as part of an integrated circuit. In the semiconductor industry, the high-volume markets for commodity devices have been called "jelly bean" markets, but today the nomenclature is no longer germane since transistors are considerably less expensive than jelly beans. The price of a semiconductor is effectively decreased in four ways:

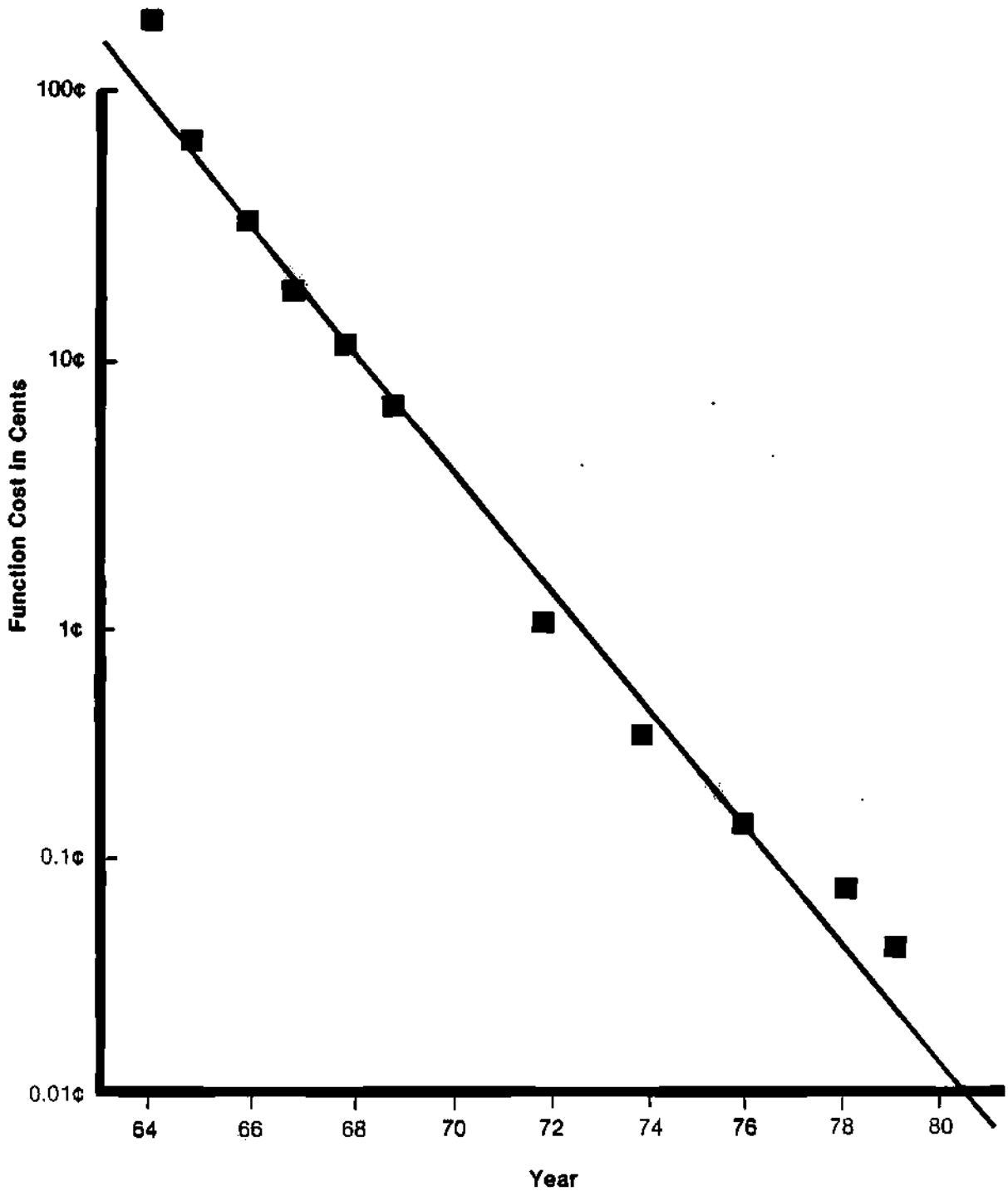
- Decreased unit price
- Increased functions per device
- Improved device parameters
- Greater sophistication or complexity per device

Average unit price deflation has been the most visible indication of price decreases in the industry, although it is possibly the least significant. Unit price decreases for a discrete device, the silicon transistor, are shown in Table 1.4-1 for the years 1962 to 1979. Unit price decreases for integrated circuits from 1963 to 1979 are shown in Table 1.4-2. The average price for discrete devices has fallen even though many lower cost devices are no longer sold, having been replaced by integrated circuits. Integrated circuit prices have fallen slowly although the complexity of the circuits themselves has increased. It should be noted that for both discrete devices and integrated circuits, the price per unit is not decreasing as fast on a percentage basis as it has in the past.

The greatest change in semiconductor prices comes from the increasing number of functions performed by a single device. In 1962, each unit sold performed essentially a single function because nearly all devices were discrete units such as transistors or diodes. With the advent of integrated circuits, the average number of functions of a single unit began to increase. In 1969, the estimated average was 3 functions per unit and, by 1972, the average was about 16 functions per unit. The increasing market penetration of LSI integrated circuits ensures that the average number of functions per unit will continue to increase. Since a 64K RAM may contain up to 75,000 transistors, relatively small unit sales of these devices can have a dramatic effect on the average number of functions per unit for the overall industry. DATAQUEST estimates that by late 1980 the average number of functions per device will be more than 500 and will continue to climb as shown in Figure 1.4-2.

1.4 Special Industry Characteristics

Figure 1.4-1
AVERAGE PRICE PER FUNCTION (ICs)



Source: DATAQUEST, Inc.

1.4 Special Industry Characteristics

Table 1.4-1

PRICE HISTORY OF SILICON TRANSISTORS

(Noncaptive U.S. Factory Sales)

Year	Unit Volume (In Millions)	Average Unit Price
1962	26.6	$4.39
1963	50.6	$2.54
1964	118.1	$1.46
1965	274.5	$0.86
1966	487.2	$0.64
1967	489.5	$0.58
1968	684.1	$0.44
1969	934.5	$0.37
1970	786.9	$0.38
1971	803.0	$0.33
1972	1,208.4	$0.27
1973	1,466.7	$0.30
1974	1,733.3	$0.27
1975	1,472.0	$0.25
1976	1,900.0	$0.22
1977	2,081.0	$0.21
1978	2,375.0	$0.20
1979	2,786.0	$0.21

Source: SIA, EIA
DATAQUEST, Inc.
June 1980

1.4 Special Industry Characteristics

Table 1.4-2

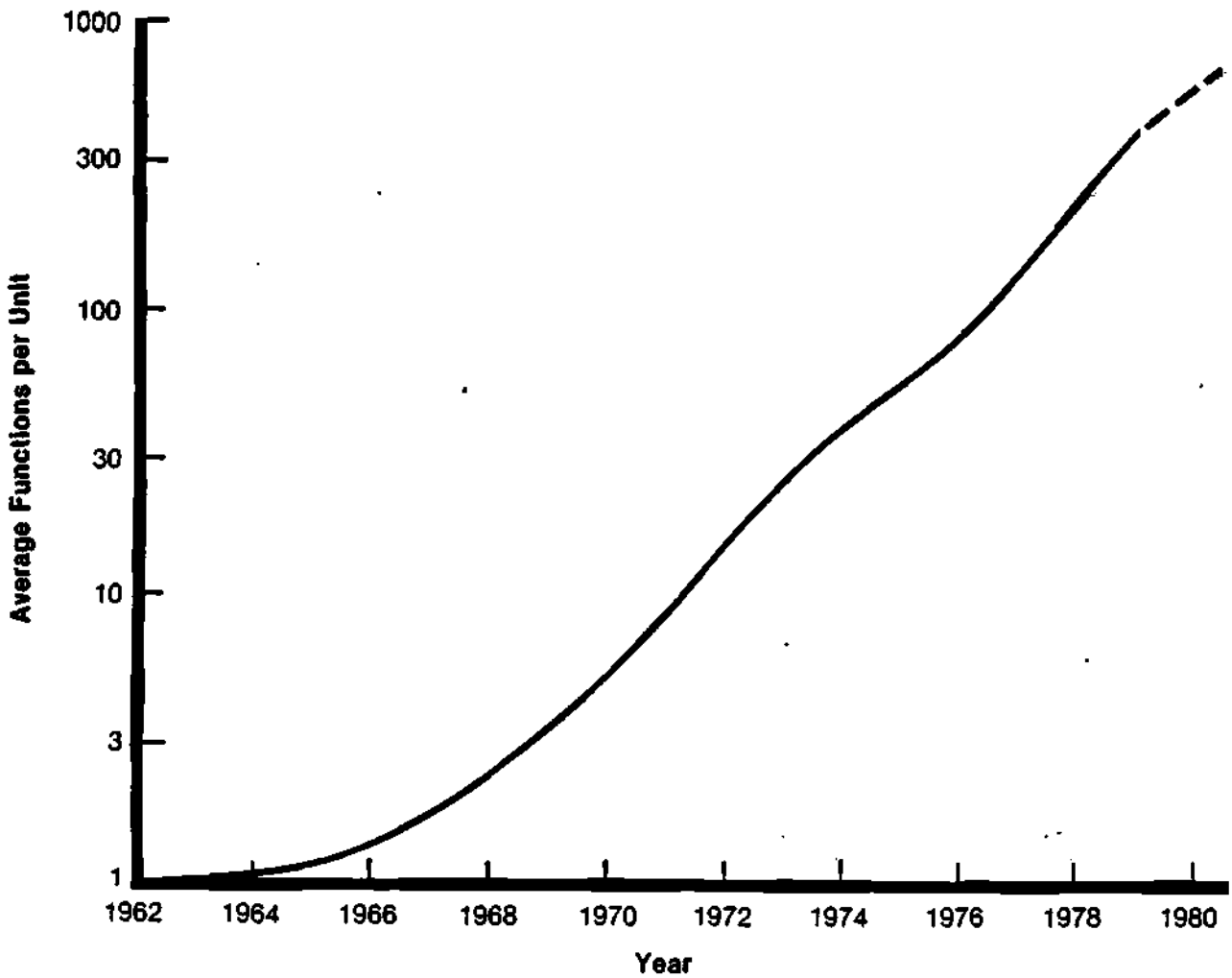
PRICE HISTORY OF INTEGRATED CIRCUITS
(Noncaptive U.S. Factory Sales)

Year	Unit Volume (In Millions)	Average Unit Price
1963	0.5	$31.60
1964	2.2	$18.50
1965	9.5	$ 8.33
1966	29.4	$ 5.05
1967	68.1	$ 3.24
1968	133.2	$ 2.28
1969	252.9	$ 1.63
1970	298.8	$ 1.45
1971	361.5	$ 1.23
1972	603.5	$ 1.01
1973	1,093.6	$ 1.09
1974	1,441.4	$ 1.04
1975	1,228.3	$ 0.99
1976	1,612.0	$ 1.00
1977	1,989.2	$ 1.02
1978	2,922.0	$ 0.91
1979	3,884.0	$ 0.98

Source: SIA, EIA
DATAQUEST, Inc.
June 1980

1.4 Special Industry Characteristics

Figure 1.4-2
NUMBER OF FUNCTIONS PER UNIT
FOR THE AVERAGE SEMICONDUCTOR DEVICE



Source: DATAQUEST, Inc.

1.4 Special Industry Characteristics

Unit pricing has also been affected by the great increase that has occurred in device performance, as defined by technical parameters, such as greater power handling capability, increased speed, greater reliability, lower power consumption, and longer life. For example, one of the greatest factors in the growth of the power semiconductor transistor market in the last few years was not lower prices per se, but the ability of these devices to handle either higher power or higher voltages and to do so with much greater reliability. Higher speeds of integrated circuits have allowed computers to have much greater computational power using the same amount of electronics.

Although the list of device improvements is long, the net effect is that the user of semiconductors has had an effective price decrease either because he can obtain greater performance using the same devices, or he can use improved device performance to decrease the number of devices needed. It is not possible to quantify effectively the price deflation of improved device performance.

Besides being larger (more functions) and better (improved parameters), ICs can also be more complex, i.e., more sophisticated. An example will clarify this concept. A one-chip microprocessor is not larger nor more difficult to manufacture than many memory devices that were earlier introduced by semiconductor manufacturers. However, it employs sophisticated systems design concepts. It is a complicated interplay between logic design, random access memories, read-only memories, and input-output circuits. Many different logic and memory designs are on the same chip and complicated computer organization concepts are used. In other words, it is more sophisticated. This type of improvement takes time to evolve, and it is important as a means of greater performance at a given price. Even if current process technology did not change for the industry, it would be many years before this type of improvement in device capability ceased.

The reasons underlying the four types of price reduction discussed above are several. The highly competitive nature of the industry has spurred technological improvement as a means of gaining competitive advantages or opening new markets. Price decreases have come from the continuing improvement of old technologies and the development of new technologies, manufacturing improvements, the use of new materials (especially in packaging), the move to overseas assembly to take advantage of lower labor costs, and a large increase in unit volume.

For new products, improvements in device yields, combined with larger batch fabrication, have been the most significant factor in reducing the costs of semiconductor chips and, therefore, prices. As a technology becomes more refined, the yields should improve for more complex or more sophisticated devices. (See Chapter 3, Manufacturing, for a discussion of yields.)

An important concept in evaluating prices for semiconductor devices is the learning curve. The theory behind this curve, of course, holds that as accumulated unit volume for a product increases, the price will decline, and that this relationship will appear as a straight line when graphed logarithmically. On an industry-wide basis, this learning curve has held true for major market segments in the semiconductor

industry. Each time the accumulated industry volume doubles, the cost per unit declines by a predictable percentage. Integrated circuits have shown a 25 to 30 percent price decline for each doubling of accumulated volume. As the volume of integrated circuits has increased, the price has rapidly declined, in spite of increasing complexity.

It is expected that prices will continue to decrease in the future. However, these decreases are expected to come less from changes in average unit price and more from increases in the number of functions per unit and increased sophistication of the unit. This increased density and sophistication will result from reduced dimensional tolerances (see Very Large Scale Integration, Section 1.5 of this Chapter).

Major new technological changes in the industry, such as the development of planar technology or MOS transistors in the past, are not expected in the next few years. However, the current state of the art in semiconductor fabrication allows for considerable evolutionary improvement. It takes several years for many small technological improvements to have an effect on the industry as a whole. We believe that the current rate of technological progress and the eventual possibilities indicate that there will be no foreseeable change in the rate of price decreases over the next few years.

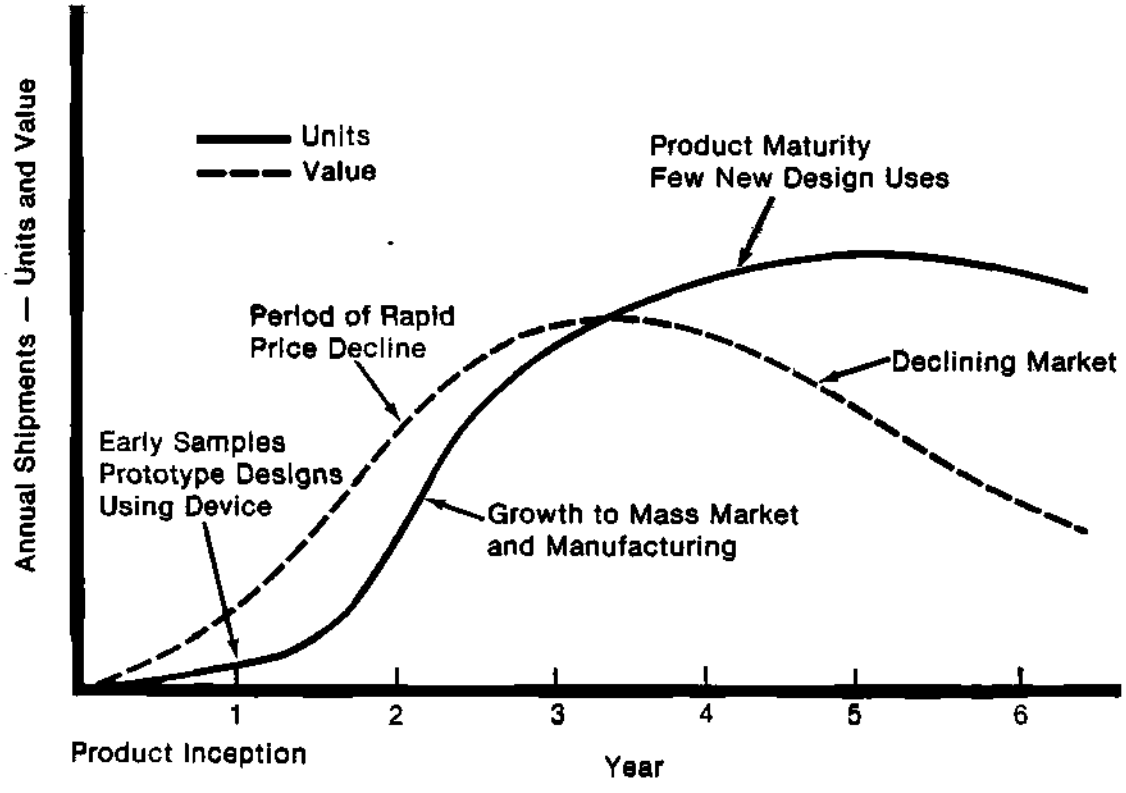
PRODUCT LIFE CYCLES

Short product life cycles are a basic consequence of the rapid change in the semiconductor industry. Any product is useful in the marketplace for only a certain period of time after its inception, but in the semiconductor industry that time can be extremely short. It is important to differentiate between the single product and the product family (in which the actual products themselves change). A product family has a somewhat longer lifetime, usually three to five years. A technology's life cycle may be even longer since it may be used for a number of successive product families.

Figure 1.4-3 shows a typical product life cycle for the semiconductor industry. After its introduction, a product rapidly increases its market—both in units and in dollars. Because initial prices are high, and decline thereafter, unit volume always increases somewhat faster than dollar volume. Initial growth may be slow, until the product is accepted, and understood, and equipment designed to include it. After that, unit volume grows very fast. Then several things happen—the market for the equipment using the product becomes saturated, new equipment is designed using new improved products, and price continues to decline. Subsequently, the dollar volume of the market for the product reaches its highest point. However, if equipment using that product has a relatively long life cycle, unit volume of a particular product may remain fairly stable (or even grow somewhat) for a longer period of time, but it eventually will begin a gradual decline.

1.4 Special Industry Characteristics

Figure 1.4-3
TYPICAL SEMICONDUCTOR PRODUCT LIFE CYCLE



Source: DATAQUEST, Inc.

1.4 Special Industry Characteristics

DTL integrated circuits are an excellent example of product life cycles in the semiconductor industry. The market for these circuits grew very rapidly between 1966 and 1969. After that time, new logic designs generally employed TTL circuits. However, because of the use of older equipment designs, the DTL market kept growing in unit volume through 1973. The dollar value, however, peaked in 1969 and has declined since then as the average unit selling price continued to decline.

INDUSTRY MATURITY

The fact that the semiconductor industry is both young and rapidly changing is often misinterpreted for it has some of the characteristics of both a growth industry and a mature industry. The semiconductor industry aggressively seeks new and growing markets. This, in turn, leads to rapid change and growth. Thus, the dynamic nature of the industry in its management of technology and technological change is probably more characteristic of industries of the future than a symptom of immaturity. However, there is currently no reason to believe that the industry will change this basic characteristic and start to resemble older, more stable industries in the United States.

The industry can be characterized as being highly sophisticated, especially in its use of technology, research and development, and its international marketing and manufacturing approaches. Management in the industry is exceptionally competent, even though rapid change and competitive pressures often present very challenging problems. Some of the best managed corporations in the United States have been blatant failures in the semiconductor industry.

1.4 Special Industry Characteristics

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1.5 Industry Trends

The semiconductor industry has always been characterized by change. Several important trends are now occurring within the industry, including:

- Low-cost electronics
- Market pervasiveness and new markets
- Very large scale integration (VLSI)
- Market crowding
  - Fewer suppliers
  - Increase in very large users
- Mergers and acquisitions
- Internationality
- Vertical integration
- Continuing rapid technical change
- Captive semiconductor manufacturing
- Increasing automation

LOW-COST ELECTRONICS

A principal feature of the semiconductor industry is the continual reduction in costs and prices, resulting in the emergence of even lower cost electronics. Previous concepts of electronics as being expensive must be discarded. Cost, of course, must refer to the function that a semiconductor performs and not simply unit price. Costs can be expected to decrease in the future for several reasons:

- An increasing number of functions on integrated circuit chips
- Improvements in yields through larger wafers, better equipment, and improved processing
- Greater unit volume and, therefore, greater efficiencies of scale

The results of lower cost electronics are expected to become even more visible in the future. Some of these capabilities, such as in low-cost, hand-held, personal calculators, are clearly visible already. In discrete devices, much of the effect is yet to be seen, but capability has increased and cost decreased to the point where discrete devices such as triacs and SCRs are cost competitive with a wide range of electromechanical and electromagnetic components. Because these components have

a definite requirement for raw materials, their costs have set lower limits. Moreover, many of them cannot be batch fabricated, allowing semiconductor devices to be more cost competitive. In the future, semiconductors are expected to become substantially less expensive than electromechanical and electromagnetic devices.

Market Elasticity

In general, decreasing semiconductor prices have opened up enough new areas of market growth to allow growth in the dollar value of the total market. In other words, the semiconductor market has a basic elasticity greater than one. Precise determination of this elasticity, however, is extremely difficult. In the first place, the effective change in semiconductor prices, as discussed previously, is difficult to measure. Second, there is a question of timing. It is apparent that changes in semiconductor prices or capability—which is the same thing—lead to the opening of new markets. However, it may take several years for these markets to develop because in many electronic systems the complexity is such that there is a long learning experience in employing new devices, designing them into systems, and developing the market for those systems. Thus, even if semiconductor prices did not change in the future, the market can be expected to expand at current prices for several years. Such items as telecom applications, large computers, and military systems have life cycles lasting many years. With the very high rate of price decline for electronic functions, ignoring timing differences might lead one to believe that the average 15 percent rate of growth in the semiconductor industry indicated that elasticity was a little greater than one. But in many cases, current markets reflect the devices developed several years ago. Today's products ensure market growth for several more years at current long-term growth rates.

MARKET PERVASIVENESS AND NEW MARKETS

Market growth, particularly resulting from the penetration of new markets, should be a continuing trend in the industry. Growth in the semiconductor market comes from either expansion of established markets or creation of new markets. Nevertheless, in established markets, changing products that use more semiconductors occasionally make the difference between these two markets purely definitional. Established markets, such as those for radios or minicomputers, grow in two different ways:

- Growth in the end market. For example, the basic market for minicomputers has grown rapidly, spurring a demand for the semiconductor devices used in them. However, because of the declining prices of semiconductors, market growth must be rapid enough to overcome the effect of declining prices if the dollar market is to grow.

- Introduction of new or changed products that employ more semiconductor devices. For example, a new computer may use more electronics to make it faster or more powerful. In a number of semiconductor markets, it is

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common for product designers to take advantage of falling semiconductor prices to increase instrument or product capability. As a result, these markets grow through higher semiconductor content.

The largest market growth in semiconductors still comes from the creation of new markets. These markets develop because of the increasing capabilities of semiconductor devices and their decreasing costs. There are three basic types of new markets:

- Component replacement
- Creation of completely new products
- Replacement of labor with capital

Component replacement has recently opened up vast new markets for semiconductor devices. This market is of two basic types—individual component replacement and replacement of small systems. Individual components are replaced by semiconductors in three areas:

- Electronic components
- Electromechanical devices
- Electromagnetic devices

Basic electronic component replacement includes such items as the replacement of lights with LEDs or the substitution of semiconductors for tubes in products such as television or high-fidelity equipment. The switch from electronic tubes to solid state in color television has created a strong area of growth for the semiconductor industry in the past few years.

Large areas of future growth are expected to come from the replacement of electromechanical and electromagnetic devices, including solid-state engine controls; solid-state relays and SCRs replacing electromagnetic relays; semiconductor memories replacing ferrite cores; disk and drum memories; and semiconductor timing circuits replacing electromechanical devices in appliances. These new markets open up vast areas of growth for semiconductors.

At the systems level, semiconductors are replacing basic electromechanical or mechanical systems. For example, semiconductor controllers are replacing electromechanical devices in industrial control applications. Occasionally, as in watches, semiconductors replace a fully mechanical system.

In some instances, the greater capability of integrated circuits and their rapidly falling prices have created totally new markets. The best known of these is the personal calculator market. In this case, semiconductors have resulted in the creation of a market that never existed before. Numerous small markets of this type are being created in industrial applications.

A basic factor in the growth of the semiconductor market has been the ability of semiconductors to be applied to equipment to replace labor with capital. In some instances, this approach also encompasses mature markets. Integrated circuits have

opened up many new market possibilities in such areas as computers, industrial automation, office equipment, and industrial control. These new products are primarily aimed at replacing labor or increasing productivity or both. Basic decisions by business to use capital equipment (containing semiconductors) is still a major factor in semiconductor industry growth.

VERY LARGE SCALE INTEGRATION (VLSI)

Integrated circuit devices are increasing extremely rapidly in complexity, and performance. The complexity of devices, already severe, is expected to increase a hundredfold over the next ten years. A current LSI device has interconnections that approach the complexity of a road map of Los Angeles. Devices in 1983 or 1984 will have an interconnection complexity equivalent to a road map of the entire North American continent. In 1978, a memory bit cost approximately 50 millicents. That is expected to decline by a factor of 50 over the next ten years. Memory costs will be paralleled by similar changes in the thrust of logic and other semiconductor functions. At the same time, the performance of semiconductor devices as measured by their speed, power, or other parameters, will increase steadily and significantly. These estimates are based on current semiconductor research.

The Effect of Dimension

One of the overriding engineering concerns of semiconductor manufacturers is to reduce the minimum dimension of the devices which they make. Minimum line widths for semiconductor devices decreased from about ten microns to about five microns between 1965 and 1978. Most of the increase in complexity of LSI devices (and the reduction in cost per function) came from other factors. These factors are best described by Dr. Gordon Moore of Intel as "cleverness," such as the ability to reduce memory cells from six devices to one device. Table 1.5-1 gives estimates of the contribution of various factors to the annual growth of component cost per LSI device. The first two columns are estimates by Dr. Moore. The last column is future estimates by DATAQUEST. Once a cell reaches one transistor, further improvements become difficult. As a result, reduced dimension tolerance is now the critical factor in increasing component count.

The yield of semiconductor devices is directly related to the size of the semiconductor chip. If component dimensions are reduced, chip size declines and yield increases significantly. A decrease from five microns to three microns (HMOS dimensions) can result in a yield increase of a factor of ten for a device of equivalent complexity. This can result in a decrease in die cost and, ultimately price, by the same amount. Conversely, if die size remains constant, the complexity can increase by a factor of two and a half. It is easy to see why the semiconductor industry is striving to reduce dimension. Those manufacturers who first achieve this reduction will have a significant competitive advantage. This direction ensures that device complexity will increase and device cost per function will decline significantly in the future. Essentially, electronics are inexpensive and will continue to get cheaper.

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Table 1.5-1

CONTRIBUTION OF VARIOUS FACTORS TO ANNUAL GROWTH OF COMPONENT COUNT PER LSI DEVICE

	1968-1972	1973-1977	1978-1983
Dimension	26%	26%	67%
Die Area	7	13	15
Cleverness	67	61	18
Compound Growth	100%	100%	100%

Source: DATAQUEST, Inc.
June 1980

System Considerations

The increasing complexity and lower cost of semiconductor devices have resulted, and will continue to result, in semiconductors performing more and more systems tasks. Semiconductor design is now concerned not only with circuit design and logic blocks, but very often with system architecture. New devices, such as some microprocessor peripherals, need to take system application and system software into account during the design of the device. For the electronic system manufacturer, some important consequences are:

- In the future, system design and semiconductor design can no longer be organizationally separated.
- System design and semiconductor design must be performed concurrently.
- If the semiconductor manufacturer does the semiconductor design, it will de facto gain system knowledge and expertise.
- Those system manufacturers who effectively use semiconductors to speed system design will gain an advantage.
- Those system manufacturers who effectively use semiconductors to enhance performance or reduce system costs will gain an advantage.

The latter point is not entirely obvious, but there are many functions that now can be more cheaply performed by employing silicon "real estate," e.g., the tradeoff between software costs and memory costs will continue to favor memory more and more. It may be cost saving to reduce wire harnesses by employing more sophisticated digital electronic methods. Only those companies with semiconductor design knowledge can effectively choose the most appropriate tradeoffs for any given point in time.

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Design Considerations

In the future, a major emphasis will likely be on system design and system integration. The reason is that the complexity of semiconductor devices is increasing so rapidly that the ability to put logic on silicon will outpace the conceptualization of what that logic should be. In the past, the transition from device-to-logic gates to logic blocks to small processors has been fairly steady and reasonably obvious.

Cost of Design

The rapidly increasing complexity of LSI devices shows up most dramatically in the cost and time it takes to do the device engineering and design. Prior to 1970, the cost to design a state-of-the-art semiconductor device was in the tens of thousands of dollars. Currently, the cost for a state-of-the-art device can be in the millions of dollars. For example, state-of-the-art memory devices, such as 16K dynamic RAMs, cost semiconductor manufacturers an estimated $2 million to $4 million to design, including special processing work. The recent cost of design and development for 16-bit microprocessors is estimated to be approximately $30 million. Those costs include the design of peripheral chips, software aids, and other considerations associated with chips of this complexity.

It is important to note that these costs are a function of system complexity, whether one or more chips is involved. It is estimated that within five years the entire circuitry of today's 16-bit (or 32-bit) microprocessor chips, peripheral chips, and some memory will be included on a single device. While these costs are not growing quite as fast as complexity, they are escalating rapidly. Design aids, including computer-aided design (CAD), redundancy on the chip, modularization of functions, and some other methods of cutting and pasting, help to reduce costs.

Time of Design

In a few years, the capability of putting a million transistors on a chip will be a reality. The time required to design is going to become extremely critical in the near future. Those companies that learn to reduce those times will have a definite advantage.

IC Complexity--The Consequences

The implications of the preceding discussion are important to captive manufacturers and systems houses. The complexity potential of integrated circuits has increased from single-chip, four-function calculators to 16-bit microprocessors in slightly under eight years. There are some important consequences:

- Potential chip performance will outpace system design capability.
- The major constraints on implementing or designing VLSI devices will not come from wafer fabrication or yield considerations.

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- Chip capability will be increasingly important in defining the system, and conversely, the system will be important in defining the semiconductor device.

Thus, the sensitive technical areas that define state-of-the-art limitations will shift. DATAQUEST believes the following factors will be future constraints on either advancing the state of the art or implementing a new (VLSI) semiconductor device:

- Semiconductor design, including conceptualization, cost, and time
- Cost, time, and engineering of testing procedures
- Software costs
- System definition, design, and architecture

Chip yield will be a major constraint only for a limited number of high-volume products. The problems mentioned above apply particularly to custom devices. They are an indication of where a systems company could be concerned about future allocation of resources—dollars, equipment, and labor. DATAQUEST feels these factors are especially important because they will be of limited future supply. Systems houses must effectively shift their software and design capability to the semiconductor level.

MARKET CROWDING

Fewer Suppliers

In a period of very rapidly increasing semiconductor demand, the number of worldwide merchant suppliers of semiconductor devices is declining. As shown in Table 1.5-2 the number of merchant semiconductor manufacturers has declined to 95 at present from the peak of 105 in 1975. This decline results from the increasing maturity of the industry, the larger manufacturing scale to remain competitive, the increasing financial requirements, and the decline of available venture capital. In the United States, about 35 semiconductor manufacturers were established between 1967 and 1971. Currently, there are virtually no new semiconductor companies being established except for specialty shops. This situation is not expected to change. Several factors are influential here:

- Minimum facility costs rose from under $2 million to over $10 million in the late 1970s.

- The minimum sales level for a manufacturer to achieve the full economies of scale has risen above $100 million of annual revenue and is rapidly approaching $250 million.

- Changes in government tax laws have decreased available investment dollars and reduced incentives available to entrepreneurs.

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Table 1.5-2

TOTAL NUMBER OF SEMICONDUCTOR MANUFACTURERS - WORLDWIDE

Year	Merchant	Captive
1955	8	3
1960	22	8
1965	36	14
1970	87	23
1975	105	36
1980	95	60

Source: DATAQUEST, Inc.
June 1980

Table 1.5-3

SEMICONDUCTOR USERS PURCHASING MORE THAN $100 MILLION

Year	Number of Companies	Total Semiconductor Consumption (Billions of Dollars)	Percent of Total Semiconductor Consumption
1976	1	$0.11	2%
1977	1	$0.13	3%
1978	5	$0.69	8%
1979	7	$0.93	10%
1980	12	$1.80	17%
1981	17	$2.80	22%
1982	23	$3.90	26%
1983	25	$4.80	27%
1984	27	$5.80	28%
1985	31	$7.10	31%

Source: DATAQUEST, Inc.
June 1980

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Rise in Major Users

The number of major users of semiconductors is increasing rapidly as shown in Table 1.5-3. This increase is spurred by the growing pervasiveness of semiconductors and their importance in end-user electronics markets. As recently as 1977, only one company purchased more than $100 million in semiconductors. This number is expected to rise to 31 (or more) companies by 1985, accounting for more than 31 percent of all semiconductor consumption. The larger users, each individually representing hundreds of millions of dollars of purchases, will be powerful market forces and the extent of their needs is likely to alter the structure of semiconductor purchasing. However, the large number of major users probably indicates that any single company will not command undue attention of the suppliers.

MERGERS AND ACQUISITIONS

The reduction of U.S. merchant semiconductor companies in recent years has come because of both merger and acquisition. The following points are pertinent:

- Since 1975, the number of U.S. semiconductor companies has declined by ten.
- 21 U.S. merchant companies now have major foreign ownership, mostly acquired since 1976.
- 17 U.S. merchant semiconductor companies now are owned by non-semiconductor U.S. conglomerates with primary revenues outside semiconductors.
- Of 36 U.S. semiconductor companies started between 1966 and 1975, only 7 remain independent.

Recent acquisitions include the purchase of Fairchild by Schlumberger, the purchase of Mostek by United Technology Corporation, and the purchase of Synertek by Honeywell.

Many companies still existing have been acquired by foreign interests. All these companies currently are merchant vendors of semiconductors and all of them now have absentee ownership. The acquisition of U.S. semiconductor companies was primarily motivated by desires to acquire semiconductor technology or to ensure semiconductor supply. In many cases, such acquisition has been done with the encouragement and/or financing of foreign governments. Only in limited instances, such as with Supertex, have business or entrepreneurial interests been the motivator.

Foreign ownership per se is not undesirable, and the capital infusions are certainly welcome. Since the U.S. merchant semiconductor industry controls more than 50 percent of the European semiconductor market, purchase of U.S. semiconductor companies by European interests is not entirely unexpected. However, the

possibility that these companies will become less competitive and aggressive, and the possibility that their resources or production will be allocated by other than market forces, must be taken into account.

In addition to total ownership, several U.S. companies have major blocks of stock owned by other companies or individuals. Of significance are the following: 20 percent ownership of AMD by Siemens, 10.4 percent ownership of Intel by Fayez Sarofim, approximately 20 percent ownership of Analog Devices by Standard Oil of Indiana, 25 percent ownership of AMI by Borg Warner and Robert Bosch, 22 percent ownership of Siliconix by Lucas, and 24 percent ownership of Intersil by Northern Telecom (Canada).

Acquired semiconductor companies do, usually, remain as suppliers to the merchant market but historically those companies have become less aggressive competitors in the market and they often slip from the mainstream of product development and production.

INTERNATIONALITY

The semiconductor industry is highly international in scope and outlook, and this characteristic is expected to increase even further in the future. The international character of the industry is present both in marketing and in manufacturing. Most U.S. companies derive about 20 to 35 percent of their revenues from foreign sales with the average above 23 percent. As foreign markets increase, these percentages are expected to increase. International marketing is a necessity, because marketing on a worldwide scale provides additional sales to support efficiencies in manufacturing. Thus, even modest foreign sales can increase profits markedly.

European and Japanese companies have been reluctant in the past to market outside their own geographical areas, but currently are becoming much more aggressive in foreign markets. All semiconductor manufacturers today are aggressively pursuing expansion of their international marketing, most noticeably in Japanese companies. Japan has lifted restrictive import quotas on semiconductors, and a large potential market has been opened to non-Japanese manufacturers. Thus, many companies are actively increasing their marketing efforts in Japan. At the same time, Japanese companies, with less domestic protection, are expanding in U.S. and European markets, especially in memory devices, where the Japanese companies have gained a significant share of the memory market. Imports of semiconductors both to the United States and to Japan increased over 50 percent in 1979, and constituted a larger share of each region's consumption than ever before.

Foreign manufacturing is increasing for three reasons. First, the manufacture of semiconductor devices has areas that are capital and technology intensive and areas that are labor intensive. As a result, it is generally cost effective to do the capital- and technology-intensive manufacture in areas such as the United States where technical personnel and equipment are more available and to do the highly labor-intensive manufacturing, i.e., assembly, in areas where labor costs are low, as in Asia.

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It is not unusual for wafers to be fabricated in one country, devices assembled in a second country, and final testing and shipping performed in a third country. This highly mobile means of manufacturing is made possible, of course, by the small size and low weight per dollar value of semiconductor devices. Searches to seek out the most cost-efficient allocation of manufacturing has led more and more companies to invest in overseas assembly plants. This trend is expected to continue even though it may be slowed eventually by increased automation in assembly processes.

The second reason for international manufacturing is for market access—the consuming country desires to have the manufacturing process peformed locally. This approach is encouraged in a number of ways, especially through import quotas and high tariffs and duties. These nationalistic attitudes place a strong pressure on U.S. companies to achieve even greater internationality. There are approximately 98 foreign manufacturing plants owned by U.S. companies. The number of foreign operations of European and Japanese companies is small but increasing rapidly. Competitive pressures will ensure that the number of such operations increases.

The third reason is access to technology. Excellent semiconductor technology now exists not only in the United States, but also in Europe and Japan. Limited access to that technology is a competitive handicap. An excellent way to ensure access to foreign technology is through design, fabrication, and other manufacturing functions in overseas locations.

VERTICAL INTEGRATION

An important trend in the semiconductor industry is toward vertical integration. In the past few years, the thrust toward this approach has increased significantly. By vertical integration, we mean the manufacture of semiconductors by a company for the assembly of systems by that company. Although vertical integration has always existed to some extent, the manufacture of semiconductors and the manufacture of systems have usually remained relatively independent. Even though semiconductor manufacturers have had divisions that produce systems, as at Texas Instruments, these divisions have generally operated independently of semiconductor manufacture and true integration has not taken place. Integration must be considered in two ways—the first section discusses captive manufacturers' upward integration of semiconductor manufacturers into the manufacture of systems. Captive manufacturing, or the downward integration of systems companies into the manufacture of semiconductor devices for their internal use, is discussed in the following section.

Upward Integration

The benefits of greater vertical integration have always been a controversial subject in the semiconductor industry. In the past, attempts at more vertical integration have not been particularly successful for several reasons. First, until recently, the semiconductor content of most electronic systems was relatively small, averaging about 5 percent of the manufacturing cost of the system. Thus, to enter

into a system business, a semiconductor manufacturer would have to learn the remaining 95 percent of the business. Second, an entirely new marketing organization might be required, new marketing techniques would have to be learned, and the costs of market penetration would be a major problem. Generally, early attempts at upward integration were unsuccessful, especially in consumer devices.

Recently, however, upward integration has become much more widespread and has been fairly successful. Besides systems, board products and other sub-assemblies, such as memory boards and microcomputer products, have become primary means of vertical integration. Many of these products are marketed to the same customer base as semiconductor devices. Other areas being expanded with upward integration include memory systems, minicomputers, point-of-sale systems, and a number of component devices such as transducer systems and solid-state switches. DATAQUEST believes that the number of items being manufactured by the semiconductor companies will increase and that the resulting dollar volume will expand rapidly over the next five years.

There are a number of reasons why the trend toward vertical integration has become more successful:

- Increased portion of system design performed at the semiconductor (IC) level
- Standardization of many board products
- Greater dollar percentage of semiconductors in systems
- Lower assembly costs
- System design expertise has shifted to the designer of initial semiconductor components

The rapidly increasing complexity of integrated circuits, typified by large-scale integration (LSI), has meant that an ever-increasing portion of the engineering design must be performed prior to manufacture of the semiconductor device. Consequently, there has been a major shift in the value of systems design from the systems manufacturer to the semiconductor manufacturer.

The decreasing cost and increasing performance of semiconductors have made it cost effective to add an increasing number of performance features to most systems. These same capabilities have allowed semiconductors to perform more tasks in a system by eliminating other components, resulting in a vastly increasing number of semiconductor devices in a system relative to other components. For some systems, the value of semiconductors is running as high as 20 percent of the total final manufacturing cost of the system.

The effect of greater complexity of integrated circuits has been that a much smaller number of devices is being used for any given system—even though their dollar value may be greater. Consequently, the assembly cost of the system, especially

labor, has come down significantly. Many system costs are relatively fixed. Those costs that are truly variable determine the competitive position of the manufacturer. For many products, variable costs are now controlled by the semiconductor manufacturer. Therefore, vertical integration is not only feasible and profitable for many products, but in some cases almost mandatory for company survival.

Several semiconductor companies have recently been improving their capabilities for manufacturing memory boards and systems. Production of add-on memory systems was pioneered primarily by Advanced Memory Systems (now Intersil), but other companies, such as Intel and National Semiconductor now compete in this area. Most memory manufacturers now make and market board products.

Very small computers will very likely be another fertile area for vertical integration by the semiconductor companies in the future. The advent of the microprocessor, i.e., a computer processor on a single chip, began a transfer of the systems capability to semiconductor companies. Microcomputer chip systems, including the processor and associated memory chips, are becoming more common, and semiconductor companies are marketing chip sets assembled on a single PC board, or in some cases, the entire microcomputer. Generally, these products are marketed to OEMs who then market the complete systems to the end user. This capability will mark a significant step in vertical integration for some semiconductor companies because of the addition of systems and software expertise. As levels of chip integration increase, the processes will become more and more complex, and chip systems should rapidly approach the performance of today's computers. As a result, the assembly of small computers will rapidly become a domain of semiconductor manufacturers.

Semiconductor manufacturers are beginning to make more and more components that are primarily functional blocks which are entirely electronic and cannot be fully integrated into a single chip. Typical of these products are such items as solid-state switches, simple transducer systems, LED displays, watch modules, and automotive electronic modules. Slightly higher levels of integration, such as amplifiers or A-D converters, still require significant custom engineering and, as a result, these components are still primarily the domain of specialized manufacturers. As some of these devices become increasingly standardized, however, it is possible that the manufacture of these devices will also shift to semiconductor companies.

Today's trends imply that vertical integration by the semiconductor manufacturers will increase rapidly in dollar volume. These manufacturers will produce a growing percentage of semiconductors for their own use and supplement their internal supplies with outside purchases as needed to support their board businesses. However, DATAQUEST expects that the majority of semiconductor devices will still be marketed competitively.

Vertical integration is not without hazards, nonetheless. Many U.S. semiconductor companies had disastrous experiences manufacturing calculators and watches. In particular, semiconductor companies that integrate vertically face problems of manufacturing and marketing in areas with which they are unfamiliar. They also face greater exposure to the risk that changes in technology may undermine their competitive position.

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Furthermore, these potential areas for integration require financial support to penetrate. Most semiconductor companies have limited capitalization, and the relatively high growth rate of the semiconductor industry requires considerable capital to finance continued growth. Companies integrating vertically may be expected to limit themselves to areas that do not require excessive financing.

Captive Semiconductor Manufacturing

Systems companies which integrate backward with the purpose of producing their own semiconductor components, and that produce solely for their own needs are captive manufacturers. In spite of their predicted demise, captive semiconductor manufacturers have been a fixture of the industry for many years. The number of captive suppliers is growing rapidly, as shown in Table 1.5-2. Our research into silicon wafer usage and semiconductor manufacturing equipment indicates that captive manufacturers constitute an estimated 20 percent of the markets for these products.

Successful captive suppliers tend to be those that supply services to their parent organizations and that the merchant semiconductor industry is unwilling, or unable, to supply. Some of these services are listed below:

- Special Processes. Some captive semiconductor suppliers have developed special processes that are not available elsewhere. These processes make possible products that could not be made in any other way.

- Special Designs. This class includes custom LSI designs that are made in such small volume that they are not of interest to semiconductor firms. Usually, these designs are justified through cost savings and by the fact that they tend to protect proprietary systems concepts.

- Education. It is desirable to educate design engineers in LSI technology to allow them to develop more competitive systems concepts—concepts which optimize the application of semiconductor technology.

- Second Source. A captive facility may be justified as a second or back-up source, i.e., as an insurance premium.

- Purchasing Support. The captive manufacturing facility can provide vendor evaluation, cost analysis, and may even help vendors with problems.

- Public Relations. Customers of major equipment companies may feel that their supplier is more capable if they have their own semiconductor facility.

- Design Integration. A captive facility allows integration of semiconductor and systems design yielding several benefits:

  - Faster design turnaround

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  - Optimization in cost/performance through design control of the entire vertical chain
  - More efficient, faster handling of engineering change orders
- Reliability
- Production control and assured delivery

AUTOMATION

Automation of semiconductor manufacturing is increasing in the semiconductor industry, continuing a trend followed over the past few years. However, the level of automation has always been a subject of controversy in the semiconductor industry because automation has both advantages and disadvantages. Several factors currently work toward increased automation in the industry. They include:

- A current low level of automation
- Increasing labor costs, tariffs, and freight rates
- Larger volume
- Greater standardization

In spite of the large amounts of sophisticated capital equipment required to manufacture semiconductors, the industry is still highly labor intensive. Labor costs amount to at least ten times amortized capital costs—building and equipment depreciation or rent. As a result, productivity in the industry is low. The semiconductor industry as a whole has one of the lowest ratios of revenues per employee, or assets per employee, of any U.S. industry. Company estimates are shown in Table 1.5-4. Variations in company growth rates, and company revenues from other product lines distort these ratios somewhat.

Some areas of semiconductor manufacturing, especially assembly, are performed overseas where low labor costs can substitute for the capital costs that would be incurred using more automated assembly operations in the United States. However, this area is becoming more expensive because of rapid wage inflation in many parts of Asia. Wages have increased by as much as four times in the past year and one half. Additionally, there has been increasing concern over tariffs and duties, particularly Sections 806/807 of the Customs Code (which deal with the rates applied to foreign assembly) as interpreted by the Commerce Department. Regulated freight rates are also an important cost factor for Asian assembly. A recent FCC decision has allowed a 60 percent increase in freight rates charged to some semiconductor companies. These high rates may be circumvented in the future by companies that purchase and operate their own airplanes.

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Table 1.5-4

ASSETS AND REVENUES PER EMPLOYEE 1978

Company	Assets Per Employee	Revenue Per Employee
AMD	$24,205	$29,184
AMI	$17,999	$25,253
Analog Devices	$37,732	$41,787
Electronic Arrays	$16,255	$19,739
Fairchild	$16,333	$21,204
Intel	$18,020	$36,789
Intersil	$23,500	$37,815
Monolithic Memories	$10,491	$19,944
Mostek	$22,526	$26,566
Motorola	$24,361	$32,632
National Semiconductor	$10,432	$22,332
Siliconix	$17,432	$21,665
Texas Instruments	$19,322	$32,455
Unitrode	$25,687	$32,119

Source: DATAQUEST, Inc.
June 1980

Between 1967 and 1974, the unit volume of integrated circuits increased over 20 times and should increase further in the future. In addition to this volume increase, more devices are becoming industry standards and are manufactured in extremely high quantities. Greater volume makes automation more economically feasible. All of these factors argue for increased automation. On the other hand, some factors will slow automation, including:

- Lack of capital in the industry
- Continuing technical changes
- Lack of availability of adequate equipment

Since the industry generally is underfinanced, it cannot afford a great deal of capital equipment without a large infusion of equity. The continuing evolution of the technology and the consequent rapid obsolescence of products and equipment tend to lower the expected return on investment for equipment. In the past, many companies have been severely affected by the rapid obsolescence of capital equipment.

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Finally, and perhaps most important, has been the lack of adequate automated equipment. Equipment for the semiconductor industry has very special requirements and, in many cases, effective design has not yet been evolved.

Two areas that are highly labor intensive are likely to become more automated: mask alignment and lead bonding. Operation repeatability and improved process tolerances are principal motivations to automate these areas. Mask alignment is done primarily in the United States because it is an integral part of wafer fabrication. Automatic aligners are beginning to appear and should see greater acceptance in the future. Lead bonding is performed mainly in the Asian assembly facilities. Whether this step should be automated has recently become a very controversial subject. We believe that increased automation will occur eventually. Adequate automated bonding machines have not been designed at this time, but they are certainly technically feasible. Both Motorola and Texas Instruments have major in-house programs to develop improved bonding equipment.

In general, newer, more automated equipment will have four major capabilities:

- The ability to handle larger batches
- Repeatable process capability
- Faster throughput or higher productivity
- Greater adaptability to different devices

There are important consequences of the shift toward increased automation. First, more production will be performed in the consuming nation—that is, manufacturing will be performed wherever the market exists. Increased automation should make the higher labor costs of these market areas less important. Second, the industry will become less labor intensive, with higher fixed costs. Finally, underfinanced companies that cannot afford automated equipment will be at a competitive disadvantage.

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1.6 Industry Problem Areas

ECONOMIC CYCLES

A major problem in the semiconductor industry is the effect of cycles in the general economy on semiconductor markets. Small changes up or down in the general economy are magnified several times in the semiconductor industry. This problem arises because the basic market for semiconductors—about two-thirds of the U.S. semiconductor market—is accounted for by capital equipment. These items, in general, are purchased for expansion of industrial capacity or productivity. When the economy is expanding, industry expands its capacity and there is a good market for equipment using semiconductors, but, when the economy is not doing well, the market for such items as computers is diminished considerably. Table 1.6-1 shows this effect quantitatively.

Table 1.6-1

SEMICONDUCTOR INDUSTRY GROWTH

(U.S. Consumption)

Year	Percentage Real Growth In GNP	Percentage Industry Growth
1967	2.7%	-4.2%
1968	4.4%	4.7%
1969	2.6%	16.3%
1970	-0.3%	-9.6%
1971	3.0%	-6.9%
1972	5.7%	29.6%
1973	5.5%	49.4%
1974	-1.4%	13.6%
1975	-1.3%	-20.1%
1976	5.7%	30.0%
1977	4.9%	15.2%
1978	4.4%	22.6%
1979	2.3%	39.2%

Source: DATAQUEST, Inc.
June 1980

1.6 Industry Problem Areas

In good years such as 1966 and 1973 when the economy was doing well, the semiconductor industry had high market growth. However, in years when the economy was in a slowdown, such as 1967, 1970, and 1975, the semiconductor market has been very poor. The large swing in market growth, over a range from minus 20 percent to plus 45 percent, shows the extreme sensitivity of the industry to the economy. The retaliation of the industry to the economy is discussed in more detail in Chapter 2, Markets; Section 2.2, Econometric Model, of the Semiconductor Industry Service notebooks.

Such rapid changes in the semiconductor market, of course, pose some difficult problems for the industry. In very good times, it is difficult for companies in the industry to adjust to the rapid growth—such as in 1973 and 1979. In difficult times, these companies face the task of cutting production. In such times, individual companies must make hard decisions on prices. They must choose, in essence, between profit margins or retaining market share. A company often faces the dilemma that if it tries to retain its profits, its market share will shrink so drastically that its efficiencies of scale will disappear and its profits with them. Because the industry is highly competitive, this decision generally means that profits suffer. In 1970 and 1971, when semiconductor demand decreased, the semiconductor industry was grossly unprofitable, with only six companies out of about 70 remaining profitable. In 1975—a much more severe downturn—only a limited number of companies were unprofitable.

Because the semiconductor industry is basically labor intensive, the industry has only one prime method of cutting costs—by reducing employment. Laying off employees is painful, of course, not only for personal reasons, but also because any employee represents a considerable investment in training. Severe reductions in employment can reduce the ability and speed with which a company can return to normal levels. Product development can also be slowed if engineers are laid off. It is clear that down cycles in the economy have been a major factor in the high mobility of employees in the industry. However, since the more experienced and more productive workers are usually retained, initial reductions in employment in a semiconductor company have little effect on production. In general, it takes a 20 to 25 percent reduction in employment to decrease unit output by 10 percent. As a result, employment reduction must be very severe to obtain measurable results.

AVAILABILITY OF ENGINEERS AND OTHER PERSONNEL

The rapid growth of the semiconductor industry and other related electronics and EDP industries from 1976 through 1979 has placed severe demands on the available pool of engineering talent in the United States. Since the early 1950s, the engineering graduates in the United States have grown very slowly, while companies in electronic and other technical disciplines have grown very rapidly. This condition is further aggravated by a temporary decline of engineering graduates in the early 1970s.

Table 1.6-2 shows the declining proportion of engineering graduates to total graduates between 1950 and 1978. As a result, available technical talent in all areas is severely limited, especially in semiconductor design and processing, and computer

software programming. This general industry problem does not have an immediate solution, and may be amplified by increased government expenditures in military electronics. Some moves to alleviate this situation include increased automation, use of computer-aided design, increased use of standard products, and overseas expansion.

The manpower shortage is worsened further by the limitation of location to areas preferred by technical professionals, such as the Santa Clara Valley (Silicon Valley), California. Increasingly, site locations for the new semiconductor facilities are predicated on the available work force, the pool of technical talent, and the desirability of a location to engineering professionals.

Table 1.6-2

ENGINEERING GRADUATES

Year	Engineering Graduates	Percent of Total Graduates
1950	58,086	11.6%
1960	45,624	9.5%
1970	63,753	5.9%
1975	65,308	5.0%
1978	74,858	5.9%

Source: National Center for Education Statistics (Department of Education)

UNIONIZATION

As the semiconductor industry grows, it is increasingly the target of union organizers. It is generally accepted (by those in the industry) that unionization of a company would be highly undesirable to its competitive position in the semiconductor industry.

The semiconductor industry requires a highly motivated, conscientious workforce. Secondly, the fast pace of change in the industry requires considerable flexibility among the workforce. Furthermore, it is desirable to promote based on merit and ability. None of these important considerations are generally of top concern to unions; a union shop is generally perceived to have rules stifling flexibility with workers' tasks, limitations to motivation, limited or structured communication with supervisors in management, limits on productivity improvement, and other traits undesirable to the rigorous demands of the semiconductor industry.

1.6 Industry Problem Areas

In the past, the semiconductor industry has generally treated its workers well, providing them with competitive pay, excellent benefits, good working conditions, and upward mobility. It is necessary that the industry continue to do so, or companies may face severe problems in the future.

HEALTH AND SAFETY

Because the semiconductor industry is a light industry, working in a semiconductor plant is generally safe from both injury and illness assuming adequate precautions have been taken by the company. Nevertheless, the semiconductor industry is essentially a chemical factory with a number of various potential problems if precautions are relaxed. Potential problems could come from toxic gases, dangerous acids, toxic cleansing chemicals, employee sensitivity to various chemicals, high temperatures, high voltages, and microscope work. These various potential problems are currently undergoing a close scrutiny by unions, the radical left, government bureaus, newspapers, and other organizations. Overreaction by them could blow minor problems out of proportion. The issue could be an explosive problem for the industry if not handled properly.

SHORTAGES

The semiconductor industry uses a wide range of materials. As a result, it often finds that one or more of these materials are in short supply, especially in times of general world economic expansion. In the past, there have been shortages in copper and some chemicals such as hydrofluoric acid. Rapid semiconductor industry expansion creates shortages of its own. In 1973, for example, there were shortages of silicon, glass quartz diffusion tubes, and packaging. The suppliers of these items had difficulty expanding fast enough to meet industry demands.

Similarly, in 1979, many materials were in short, if not critical, supply. In particular, various acids and silicon wafers were difficult to obtain at times. Other materials, especially gold, had rapid increases in price.

A future potential problem affecting the industry is a shortage of poly (polycrystaline silicon) to manufacture silicon wafers. No new major poly processing plants have been built worldwide for some time. A tremendous over-capacity in the early 1970s is now being absorbed. Because of the time required to build a plant and bring it to capacity—two years or more—there may be only limited increases in poly capacity through 1982. DATAQUEST believes that under conditions of heavy semiconductor demand, adequate wafer supply could be a problem.

A particular problem that concerns the semiconductor industry is the possibility of a shortage of electric power. Electricity is necessary for the production of diffusion tubes and the powering of depositions, epitaxial reactors, as well as all other types of testing and assembly equipment. Other power sources cannot be substituted.

1.6 Industry Problem Areas

Needless to say, a shortage of electric power could shut down the industry. Although that is highly unlikely, the imposition of quotas during a general power shortage could halt industry expansion and penalize fast-growing companies. Shortages may not be avoided, but they can be alleviated if they are detected early and the problem is communicated both to industry and to suppliers.

CAPITALIZATION

Undercapitalization will most probably be a severe problem for the industry. Historically, the industry has been somewhat underfinanced, partially because of the rapid growth in the industry. In the future, the semiconductor industry will need financing for two major reasons—to grow and to automate.

Assuming normal growth in the general economy, the semiconductor industry should grow at an average annual rate of about 15 percent. This growth will require considerable expansion in buildings, equipment, inventories, and receivables. A larger financial need, however, will come from the requirement for increased automation. The industry has always been labor intensive. For several measures of worker productivity—such as assets per employee, sales revenues per employee, and the cost of buildings and equipment as a percentage of revenues—the semiconductor industry is at one of the lowest levels of any industry in the United States. Large increases in expensive equipment will be required to increase worker productivity.

The basic need for capital within the industry could have three major effects. First, companies with cash will have an advantage. Texas Instruments is the only independent semiconductor company with a large cash inflow. The importance of financing may also be a benefit to semiconductor manufacturers that operate as divisions of large corporations that can supply the necessary financing. Second, if the stock market improves, many companies will go to the equity market to obtain financing. At this time, however, most companies' stocks are selling at market prices well below book value (which has always been low anyway) and, thus, are extremely reluctant to sell new issues of stock. Finally, the lack of cash in the industry is apt to slow automation. Companies will continue to turn to overseas operations or to utilize three shifts a day to obtain the greatest benefit from their existing equipment.

OTHERS

Many other lesser problems arise in the semiconductor industry. These problems are caused primarily by the rapid changes in the industry, the high technological content of the products, and the relative immaturity of the market that the industry serves. For example, the industry serves markets that can grow, or disappear, overnight. This rapid change has been true in the calculator market which has had several major shifts in only a few years. Managers in the industry have to anticipate changes both in prices and technology to be effective. Short product lifetimes, which

1.6 Industry Problem Areas

are characteristic of the industry, mean that a high proportion of funds must be committed to the research and development of new products. Rapid changes in markets and in products mean rapid changes in market shares. This condition lends a high degree of instability to the industry and the companies in it.

12 COMPANIES — DISTRIBUTORS

1 Industry

1 SCOPE H1

The semiconductor industry is one of the cornerstones of modern industrial society. Semiconductor devices are the basic components of computers and other data processing equipment, telecommunications, industrial automation, television and radio, defense electronics, and other important products. Both directly and indirectly, semiconductor devices are important in nearly every facet of our lives.

In 1974 the worldwide market for semiconductor devices exceeded $5 billion, including captive suppliers. The industry supplied literally billions of devices consisting of thousands of types of individual products—including diodes, transistors, integrated circuits, and optoelectronic devices. Despite their wide diversity, these products share the common bond that their basic electronic functions are performed by semiconducting materials. This commonality provides a clear definition for the industry.

More than 100 companies actively compete in the semiconductor industry worldwide. Many of these companies are small, and production of semiconductors is not yet highly concentrated among only a few companies. However, at least 16 concerns manufacture in excess of $100 million in semiconductors annually. Major U.S., European, and Japanese manufacturers of semiconductors are shown in Table 1.0-1.

The purpose of this chapter is to provide a basic description of the semiconductor industry including its structure, special characteristics, important trends now occurring in the industry, and special problems that the industry faces.

Table 1.0-1

MAJOR WORLD SEMICONDUCTOR MANUFACTURERS (Includes Captive Manufacturers)

United States

- Fairchild Camera and Instrument
- IBM
- Intel
- ITT
- Motorola
- National Semiconductor
- RCA
- Signetics
- Texas Instruments
- Western Electric

Europe

- AEG-Telefunken
- Philips
- Sescosem
- SGS
- Siemens

Japan

- Hitachi
- Matsushita Electric
- Mitsubishi
- Nippon Electric
- Toshiba

Source: DATAQUEST, Inc.

1.1 History

The semiconductor industry is less than 30 years old. Although some simple diodes had been manufactured earlier, the first transistor was produced by Bell Laboratories on December 23, 1947. Technical breakthroughs in the manufacture of transistors followed rapidly, and by 1952 a number of companies were producing devices commercially. These devices, however, were made using germanium as the semiconductor material.

In 1954, Texas Instruments began to manufacture silicon transistors on a commercial scale. (Prior to that time, TI had not been a factor in the semiconductor industry.) In the late 1950s, the industry was still in its infancy with sales just beginning to pass the $100 million mark. The major market for semiconductor devices was provided by the military, which had seen the potential of semiconductors and actively supported the industry's development. Another large market, of course, was for transistor radios.

In 1959, Fairchild Camera and Instrument developed the planar technology for manufacturing transistors, which later became the basic technology for the manufacture of integrated circuits. Integrated circuits themselves were not commercially manufactured until 1961, when they were first marketed by Texas Instruments. About the same time, a wider proliferation of many different types of semiconductor devices began, including the development of MOS devices, junction field effect transistors, and Schottky diodes. At this time several improvements in manufacturing technology also occurred, providing rapid increases in productivity and device reliability.

In the late 1960s the use of integrated circuits grew rapidly, and by 1965, worldwide industry sales had passed the $1 billion mark. This period also marked a proliferation in uses for semiconductor devices, including many markets for industrial products, data processing devices, and communications equipment. During this time MOS devices also began to be sold on a commercial scale. U.S. companies began to assemble their products overseas, and both the European and Japanese markets became important. In 1968, the first light emitting diodes were sold commercially by Hewlett-Packard, following their development by Bell Labs four years earlier.

1.2 Structure

PRODUCTS

The semiconductor industry has a wide diversity of products. The most basic breakdown consists of integrated circuits, discrete devices, and optoelectronics. An integrated circuit is a single chip that has more than one active device on it. For example, it may have a number of transistors, diodes, resistors, or capacitors as part of the electronic circuit. Integrated circuits (ICs) vary widely according to the functions that they perform and the technologies used in their manufacture. Circuits can perform digital or linear electronic functions and be based on a number of basic technologies, such as that for bipolar transistors or MOS transistors. ICs can perform almost a limitless number of different types of circuits.

Discrete devices have an even wider diversity. They consist of many types of transistors, diodes, and switching devices such as SCRs and triacs. Again, the wide diversity of product applications requires tens of thousands of types of discrete devices. This product diversity requires many variations in manufacturing.

Products fall into three general classifications:

- Custom
- Standard
- Commodity

A custom device basically is designed and manufactured for a single customer. In general, only a limited quantity is manufactured, the price is relatively high, and the technical attributes are specifically designed to meet the customer's needs.

A standard device is a semiconductor that is offered to the general marketplace. These devices are intended by the manufacturer to meet the application requirements of many users. The quantities of standard devices demanded depend not only on the market for which they are intended, but also on their acceptance in those markets.

A commodity device is a semiconductor that has been universally accepted, and it is produced in high volume by more than one manufacturer. This type of device is usually characterized by high volume, low cost, and relatively low margins.

Only within the past few years have a significant number of integrated circuits become commodity products. The emergence of commodity devices marks a major advance in the maturity of semiconductor markets. In general, these products are manufactured by the larger companies which have a competitive edge in volume efficiency. Custom devices, on the other hand, are often produced by small manufacturers that are competitive within a niche for a particular product or technology.

MARKETS

The semiconductor industry has four major end-user markets:

- Consumer
- Industrial
- Computers
- Government and Military

Although each of these markets is separate, the division should not be overemphasized, because most products are useful in more than one market, and manufacturers rarely specialize in a single market.

The consumer market includes entertainment items (such as radios and televisions), cameras, watches, automobiles, calculators, and appliances. Most applications in this market are fairly recent developments, with the exception of radios which supplied one of the first markets for semiconductors.

The industrial market consists of a wide variety of industrial applications, including noncomputer EDP applications, process control equipment, communication equipment, test and

1.2 Structure

instrumentation equipment, and various current switching applications.

The computer market includes devices used for computers, minicomputers, and associated memory storage. Microprocessors are a new and growing segment of this market.

The government and military market is the oldest of the semiconductor markets. Prior to the mid-1960s, this market accounted for the majority of semiconductor sales. Devices for this market generally require special handling and testing, special packaging, and unusually high reliability. Moreover, demand is often limited and prices are generally considerably higher than those of other markets.

The major markets supplied by the semiconductor manufacturers have a large number of different applications, which result in an extremely large number of smaller market segments. The smaller markets often require special types of devices with unique technologies or specialized applications. This situation creates opportunities for many small companies to be both competitive and profitable.

With a few exceptions, semiconductor devices are sold to manufacturers that design, assemble, and market the end products. Thus, the vast majority of semiconductors are sold to other industrial manufacturing corporations rather than used internally.

MANUFACTURING

The central focus in manufacturing in the semiconductor industry is the fabrication of the semiconductor device from an extremely thin, raw silicon wafer, which is about three inches in diameter. This process entails hundreds of individual manufacturing steps, each requiring complex technology and high precision. The manufacture of the semiconductor device can be divided into three major operations—wafer fabrication, testing, and assembly. A complete description of semiconductor fabrication is found in the manufacturing chapter of the Semiconductor Industry Service. Process variations among the different types of semiconductors are included in the Technology Chapter.

In the semiconductor industry, all manufacturing steps are usually performed by one company. The company also markets the devices. As a result, the industry is structurally simple. Differences occur from company to company, however, in the amount of integration of support functions. Integration includes fabrication of the package in which the devices are assembled, manufacture of the semiconductor wafers on which the devices are made, manufacture of the masks involved in the photolithographic process, and other functions. Larger companies, such as Texas Instruments, operate on this level of integration. Smaller companies, in general, do not perform these manufacturing functions.

The unified manufacturing structure of the industry—from wafer to final product—results from the close interrelationship of the technology of the various manufacturing steps. It is not likely that this structure will change in the future.

DISTRIBUTION AND MARKETING

Semiconductor devices are sold and distributed in three basic ways:

- Through a direct sales force, with shipment from the company.
- Through a representative organization with shipment from the company.
- Through a distributor with shipment from its own stocks.

Historically, semiconductor companies have preferred to market directly whenever possible. However, a direct sales force cannot market economically to smaller users or in areas where sales volumes are low so that direct selling rep-

1.2 Structure

resents a large fixed cost. During the current downturn, many of the larger manufacturers—such as Fairchild and Rockwell—have turned increasingly to manufacturers' representatives. These organizations may handle several companies with nonconflicting product lines. Generally, a representative organization receives a higher commission than a does the direct sales force. However, for small companies that cannot economically maintain a direct sales force, this approach is a viable alternative.

Distributors generally buy semiconductor devices from companies in large quantities, under agreements with those companies, and resell them in smaller quantities at higher prices. Distributors also often market actively to many companies. They relieve the semiconductor companies of the problems associated with handling many small orders and perform a valuable inventory function for the industry, as well as some marketing functions.

VERTICAL INTEGRATION

In the past, vertical integration has rarely played a role in the structure of the industry. Semiconductor companies, in general, have not integrated into the complete manufacture of an end-product. Notable exceptions have been the Delco Division of General Motors, IBM, and Western Electric. There has been a gradual trend toward vertical integration, which has been highly visible, because of calculators and digital watches. However, the separation of semiconductor manufacturing and end-product manufacturing still prevails in the majority of manufacturers. This is because the semiconductors required for most products require a greater diversity in semiconductor manufacturing than a single semiconductor facility can offer.

OWNERSHIP

The ownership of semiconductor manufacturing can be divided into three broad categories: independent manufacturers, divisions of major corporations, and captive manufacturers. These distinctions are not always entirely clear, but they serve generally to identify the various types of companies.

Independent Manufacturers

Most semiconductor manufacturing in the United States is performed by independent manufacturers. By definition, the semiconductor operations of these manufacturers constitute a major portion of their businesses. Companies in this category include American Microsystems, Fairchild, Intel, Motorola, and National Semiconductor. There are a very large number of smaller companies, both publicly and privately owned, in this category. Between 1968 and 1971, more than 30 new semiconductor companies were formed.

A basic characteristic of these companies is that their survival depends on their performance in the semiconductor industry. As independent companies, they do not have either guaranteed markets or financing. In general, they are competitive, aggressive, and leaders in bringing new technologies to the marketplace. Moreover, they have been leaders in expanding the international scope of the industry, both in manufacturing and in marketing.

Divisions of Major Corporations

Many major corporations in the United States, Europe, and Japan have divisions that manufacture semiconductor devices. These divisions are distinct from totally captive manufacturing in that they actively market their semiconductor products. In some cases, they do not supply products directly to the parent corpora-

1.2 Structure

tion, although many of them do. Most such organizations, however, derive only a fraction of their sales from captive markets. Companies with large semiconductor divisions include General Electric, Hitachi, ITT, Nippon Electric, Philips, RCA, Raytheon, Siemens, and Westinghouse.

Structurally, these organizations may be treated as a division of the parent corporation or may be organized as a semiautonomous company. For example, Signetics was set up as a completely independent company by Corning.

These companies vary greatly in (1) their outlook toward the semiconductor industry, (2) their treatment by the parent company, and (3) their competitiveness in the industry. Although, in general, they may be slightly less competitive and aggressive than the independent companies, it is difficult to generalize. All of these companies, however, can benefit from the financial resources of the parent company. With the increasingly high capitalization requirements in the industry, that is a distinct advantage. Large parent companies also often have a sheltered market that the semiconductor division can take advantage of. On the other hand, such companies often have problems attracting talented individuals from the industry because the fast pace of the semiconductor industry often is at odds with slower decision-making processes of a large corporation. Furthermore, the senior officers of such corporations generally have little or no experience with the semiconductor industry.

Captive Manufacturers

Several companies have totally captive semiconductor facilities and make semiconductor devices for their own use, but do not market devices to industry. Major manufacturers with captive lines include Burroughs, IBM, NCR, Hewlett-Packard, Honeywell, and Western Electric (AT&T). The existence of such captive facilities tends to decrease the market available to the companies competing in the semiconductor industry.

As semiconductors have become more important to major manufacturing companies, interest in captive facilities has increased. Captive facilities provide advantages to many companies in integrating semiconductor design with final product design. Moreover, there are often planning and control advantages. The ability of a captive facility to know both the future quantity and product mix of its output and its lack of marketing costs are strong advantages. On the other hand, captive facilities have many of the same problems that divisions of major corporations are faced with—difficulty in attracting top grade technical personnel, slow decision making processes, and changes in the technology that may outmode facilities. In the past, only a few manufacturers (e.g., AT&T and IBM) have had sufficient in-house requirements for semiconductors to support the necessary efficiencies of scale for cost-effective semiconductor manufacturing. However, this situation is changing with both the increasing scale of equipment manufacturers and the increasing solid-state content of the products so that companies like Burroughs and NCR now are cost-effective.

1.3 International Aspects

The semiconductor industry is highly international. Devices are manufactured and marketed throughout the world. The European market and Japanese market for semiconductors are each about one-half the size of the U.S. market, but differ from it in many important respects.

EUROPE

The European market for semiconductors amounted to an estimated $1.2 billion in 1974. About 60 percent of the market is accounted for by discrete devices, a larger percentage than the world market as a whole. The use of semiconductor devices in Europe is heavily weighted toward industrial uses with smaller markets for computer, consumer, and military applications.

Manufacturing in Europe is performed both by European and U.S. companies. The U.S. concerns, with more than half of the market, dominate integrated circuit manufacturing. Unlike the United States, there is only a limited number of small companies in Europe and few companies in which semiconductor manufacture is the major focus. Most large semiconductor manufacturers in Europe are divisions of large industrial manufacturers.

For a number of political reasons, many European semiconductor companies are heavily subsidized by the governments of their countries, which allow them to compete effectively against larger U.S. companies that have lower manufacturing costs. However, the largest European companies—especially Philips and Siemens— are very effective, viable competitors, particularly in discrete devices. Most European companies, with the exception of Philips, have not fully developed their international manufacturing and marketing capabilities. This limitation, together with the greater market strength and advanced technology of U.S. manufacturers, has weakened the competitve position of many European companies.

JAPAN

The use and manufacture of semiconductor devices developed very rapidly in Japan in the late 1960s, but since 1970 the Japanese market has grown more slowly than the world market. Japanese consumption of semiconductor devices is estimated at about $1.1 billion in 1974. In Japan, semiconductor devices are used primarily for consumer applications, with nearly two-thirds of all integrated circuits applied to that market. However, industrial applications have been growing rapidly.

In the past, the Japanese market for semiconductor devices has been highly protected by the Japanese government through a variety of means including high tariffs, import restrictions, and subsidies. This situation has allowed the Japanese semiconductor industry to develop successfully to maturity and viability. As a result, Japanese companies can manufacture a high percentage (estimated at about 85 percent) of the semiconductor devices consumed in the country. A small group of five companies dominate Japanese semiconductor manufacture, although there are also many smaller companies.

In the past, foreign companies have been restricted to a minority interest in semiconductor manufacturing in Japan. Several U.S. companies—including American Microsystems, General Electric, ITT, International Recitifier, Motorola, and Raytheon—have established manufacturing facilities on a minority ownership basis. Only Texas Instruments has been allowed to have a wholly owned facility. Among European companies, Philips holds a 30 percent interest in Matsushita Electronics.

Recently, however, many import restrictions have been lifted, and foreign companies are now allowed to have wholly owned manufacturing plants in Japan. U.S. manufacturers

have long felt that they could increase their share of the Japanese market if restrictions were lifted. Indications now are that such an increase may occur. For example, in 1974, U.S. companies greatly increased their share of the Japanese IC market—to about 30 percent.

Rising Japanese wages, limited facilities for off-shore labor, severe declines in the Japanese market for many consumer items, such as calculators and color televisions, and lack of technological leadership have hurt the competitive position of the Japanese semiconductor manufacturers.

SYMBOLIC CAPABILITIES IN THE EMERGING NATIONS

In the past, semiconductor devices have been manufactured primarily by European, Japanese, and U.S. companies. However, many developing nations are expressing a keen interest in establishing semiconductor manufacturing facilities. The same national pride that has led to the establishment of national airlines in many developing countries is expected to lead to the establishment of semiconductor facilities. These nations feel that many benefits will accrue from establishing a facility, including:

- National pride
- Defense capability
- Industrial autonomy
- Symbolic technological capability
- Support for local electronic assembly
- A core industry leading to further development in other industries
- Improved balance of trade

Different nations place different emphasis on various of these benefits. Nevertheless, an expansion of facilities in many countries seems likely. Nations showing particular interest include the Arab nations, Canada, India, Iran, Israel, Korea, the Philippines, Singapore, Spain, and Taiwan.

In establishing a semiconductor facility, however, these countries face some severe problems. Major problems include the lack of adequate support technologies in industry and difficulity in attracting qualified technical personnel. Ongoing facilities may face a lack of markets for their product and will very likely have difficulty being competitive. It can be expected that these facilities will be highly subsidized. Nevertheless, the cost of establishing a facility is small compared with that for airlines, steel mills, or other industries.

Diffusion facilities are in place now in Korea and Taiwan. Within a year, plants will begin operations in the Philippines and the Mid-East. The impact of these facilities on U.S. companies will be mixed. On the positve side, a number of profitable cross-licensing arrangements will quite likely be made and the equipment will probably be ordered primarily from U.S. manufacturers. On the negative side, nationalistic practices may limit exploitation of these markets by U.S. companies in a manner similar to the restrictive tactics previously used by the Japanese to protect local manufacturing. Futhermore, as nationals return home a reverse "brain drain" may siphon technical talent from the United States.

1.4 Special Industry Characteristics

The semiconductor industry has many characteristics that set it apart from other industries. For the most part, these characteristics arise from the industry's high technological dependence, intense competitiveness, and broad variety of products. These special characteristics include:

- Intense competition
- Product diversity
- High technology
- Rapid rate of change
- Cost and price reductions
- Short product life cycles
- Maturity with change

COMPETITION

The semiconductor industry has always been intensely competitive and should remain so in the foreseeable future. The effects of this competition are to make the industry aggressive, to make it readily adaptive to any change or competitive advantage, and to lower profit margins.

There are several reasons for this intense competitive situation.

- A lack of any major barriers to competition
- Low barriers to entry into the industry
- Market share advantages
- A wide range of products
- A very large number of companies
- A continual influx of new products and new markets

More than 100 companies in the United States make semiconductor products of one kind or another. Although many of these companies produce only specialized products or manufacture limited lines for their parent companies, more than 70 companies actively compete in the mainstream of the industry. In addition to these U.S. companies, more than 30 European companies and 10 Japanese companies are actively competing in the world market.

In any given semiconductor market segment, there are ususally many competitors from which a buyer may choose. Although the large number of companies will almost surely be reduced in the future, they can exist at present because of the wide range of products in the industry. A company can specialize in a given area and have a particular advantage in manufacturing a few products. Although any competitive advantage in a product line is temporary, the diversity of products is sufficient to allow all companies in the industry to be competitive in at least some areas.

New products are continually being developed by the industry at a very high rate. Since a new product, by definition, does not have established suppliers, the company producing it can gain a short-term advantage. Thus, many small companies compete effectively in the semiconductor industry by continually advancing the state-of-the-art technology. The same advantage of new products also applies to new markets created by these products. Nevertheless, since market share and the resulting volume production is extremely important in the industry, particularly as markets become mature, competition is intense for market share. This situation leads to recurrent price competition which can be extremely severe.

Another reason for the large number of competitors in the industry and the severity of competition is that barriers to entry into the semiconductor industry have, in the past, been relatively low. Although such barriers as start-up costs, technology, and the cost of obtaining a competitive market share are rising, they nevertheless remain low in comparison with many other industries. Between 1968 and 1971, more than 30 new companies were formed in the United States to compete in the semiconductor industry. Despite declining semiconductor demand in 1970 and 1971, at least 80 percent of

1.4 Special Industry Characteristics

these companies survived in one form or another and some, such as Intel, have been eminently successful.

A corollary to the low barriers of entry to the semiconductor industry is the lack of any artificial market or manufacturing barriers that might serve to lessen competition, such as government regulation, price controls or supports, or union policies.

PRODUCT DIVERSITY

The semiconductor industry is characterized by an extremely wide range of products. There are several different theoretical types of transistors or other semiconductor devices, each with its own special characteristics. Each type of product has a large number of operating characteristics including power-handling capability, speed, amplification level, and rated voltage. The possible design value chosen for each of these characteristics for a given product can vary over an extremely wide range, and the possible combination of product characteristics is nearly infinite. Integrated circuits have even wider diversity than discrete devices because of variations in circuit designs.

Product diversity occurs because semiconductor products have been specialized to perform distinct functions, and their design and manufacture have been optimized for those functions. Thus, there are literally tens of thousands of different products in the industry.

The extremely wide diversity of products has many important consequences for the industry. Because it allows a larger number of competitors to exist by forming a large number of specialized markets, it parodoxically increases the competition in the industry. Product diversity also decreases volume manufacture of any single products, thus inhibiting increased industry automation.

TECHNOLOGY

Since the semiconductor industry is highly technologically oriented, it is important to underscore the role that technology plays in the industry. The primary products—discrete devices and integrated circuits—are, of course, technological in nature. Their concept, design, and function are the very basis of sophisticated electronics. It is also important, however, to note that the manufacture of the devices is also highly technical. This includes the processes employed, the sophisticated equipment used to manufacture and test the devices, and the skill levels of all personnel concerned with the operation. Furthermore, the products in which most semiconductors are used are also highly technologically oriented.

An LSI semiconductor memory is an example of this technological complexity. To be competitive in this field a company must have a thorough understanding of the device's complex end-use. Moreover, it must have the design capability and the processing technology to make the device. It must also be able to choose successfully among the trade-offs available in the various technologies to produce a successful cost-competitive product (See Chapter 3, Manufacturing). This understanding is fundamental to being a competitive supplier with state-of-the-art design, state-of-the-art manufacturing, and products that are useful and cost-effective for the user.

Furthermore, the technological nature of the business makes timing critical. Every facet of a product—its design, its process, and its market—is viable and competitive for only a short period of time. Before that time manufacture is too difficult, too costly, or simply not viable. After that time the product may be obsolete.

Because of the technological intensity of the industry, R&D expenses are always unusually high compared with those in many other

1.4 Special Industry Characteristics

industries—often over 10 percent of revenues. Extensive R&D is a necessary investment for any company that wishes to remain competitive.

Nearly everyone who works in the industry must be highly trained in one phase or another of semiconductor technology. This requirement includes a large cadre of engineering specialists; managers who are trained not only in management but have a thorough understanding of the general aspects of the technology; and the technicians, supervisors, and workers who must have a thorough understanding of the equipment they operate.

A recurring problem for all companies is the threat of technological obsolescence of their products. This threat occurs not only over time, as new and improved products displace old ones, but also because at any time a completely different semiconductor technology could obsolete the products they manufacture. For example, silicon transistors have replaced germanium transistors and TTL logic has replaced DTL logic for integrated circuits.

RATE OF CHANGE

The semiconductor industry is very dynamic; it truly suffers from "future shock." It has very rapidly changing technology, processes, products, manufacturing methods, and markets. This characteristic is perhaps the least understood and the most underrated by observers of the industry.

Improvements in the capability of semiconductors come at breathtaking speed. For example, in a little more than ten years the products of the industry have progressed from a simple transistor to an IC performing a simple logic function (such as a gate), to an IC performing an entire functional block of a system (such as an adder), to a one-chip calculator circuit, to a one-chip computer processor. Processing technology has changed from alloy junctions to bipolar planar technology to MOS technology—all with many alternative variations. (See Chapter 4, Technology, for futher information about past technological breakthroughs.) Markets have changed from mainly military to include a wide range of industrial equipment, EDP applications, and consumer products, such as calculators, automobiles, and watches.

The dynamic nature of the semiconductor industry is both exciting and profoundly unsettling. Products, technologies, and even companies are based on the shifting sands of technological progress. Past benchmarks are not applicable to the future. It is important to understand that this rapid rate of change is not a transitory phenomenon. Rather, it is a built-in characteristic of the industry. That is, the industry is one that is geared to change. Indeed, its dynamic nature is a more fundamental product of the industry than are the semiconductors that the industry manufactures.

Three main factors account for the dynamic nature of the industry:

- Technological progress
- A large number of talented people
- Heavy competitve pressure

None of these factors is independent, but works together in constant reinforcement. Because the industry is highly competitive, companies strive for improvements in technology to gain a competitive advantage, even if it is only temporary. This leads the industry to seek large numbers of individuals with technological expertise, creative ability, and drive. These people must have the special ability to manage under the constant change that is occurring in the industry—circumstances that bewilder competent managers in other industries. However, it is the excitement and change that attract these people to the industry. In turn, their abilities add to the competitive crush and the high rate of technological progress.

Not all of the effects of this environment

1.4 Special Industry Characteristics

are positive. The change takes its toll both in people and companies, through technological obsolescence. Although the industry has made laudable progress, adaptation to the rapid change keeps industry profits low and tends to undermine any basic strength that a single company may have so that any competitive advantage may be short-lived. Moreover, both the change and the growth in the industry create a continual financial strain for most companies.

COST AND PRICE DEFLATION

One of the most remarkable characteristics of the semiconductor industry is the rapid and continual price decreases that occur. If these price changes over the past 15 years had been matched by the automobile industry, one could buy a car today for $2.50. In 1960, the average price of one transistor was over $5.00. In 1975 the cost of more than 20 transistors is less than a penny when purchased as part of an integrated circuit. In the semiconductor industry, the high volume markets for commodity devices have been called "jelly bean" markets, but today the nomenclature is no longer germane since transistors are considerably less expensive than jelly beans. The price of a semiconductor is effectively decreased in four ways:

- Unit price decreases
- Increased functions per device
- Improved device parameters
- Greater sophistication or complexity per device

Average unit price deflation has been the most visible indication of price decreases in the industry, although it is possibly the least significant. Unit price decreases for discrete devices from 1962 to 1972 are shown in Table 1.4-1, and unit price decreases for integrated circuits from 1964 to 1972 are shown in Table 1.4-2. The average price for discrete devices has fallen

Table 1.4-1

PRICE HISTORY OF SILICON TRANSISTORS (U.S. Factory Sales)

Year	Unit Volume[1] (in Millions)	Average Unit Price
1962	26.6	$4.39
1963	50.6	2.54
1964	118.1	1.46
1965	274.5	.86
1966	487.2	.64
1967	489.5	.58
1968	684.1	.44
1969	934.5	.37
1970	786.9	.38
1971	803.0	.33
1972	1,208.4	.27

[1] U.S. Factory – noncaptive

Source: EIA

Table 1.4-2

PRICE HISTORY OF INTEGRATED CIRCUITS (U.S. Factory Sales)

Year	Unit Volume[1] (in Millions)	Average Unit Price
1963	0.5	$31.60
1964	2.2	18.50
1965	9.5	8.33
1966	29.4	5.05
1967	68.1	3.24
1968	133.2	2.28
1969	252.9	1.63
1970	298.8	1.45
1971	361.5	1.23
1972	603.5	1.01
1973 (Est.)	1,200.6	.86
1974 (Est.)	1,582.0	.82

[1] U.S. Factory – noncaptive

Source: EIA
DATAQUEST, Inc.

1.4 Special Industry Characteristics

even though many lower cost devices are no longer sold, having been replaced by integrated circuits. Integrated circuit prices have fallen although the complexity of the circuits themselves has increased. It should be noted that for both discrete devices and integrated circuits the price per unit is not decreasing as fast on a percentage basis as it has in the past. This situation results from absolute limitations imposed by the cost of the material for packaging the device and the absence of any recent radical change in packaging material.

The greatest change in semiconductor prices comes from the increasing number of functions performed by a single device. In 1962 each unit sold essentially performed a single function because nearly all devices were discrete units, such as transistors or diodes. With the advent of integrated circuits, the average number of functions of a single unit began to increase. In 1969 the estimated average was three functions per unit, and by 1972 the average was about 16 functions per unit. The increasing market penetration of LSI integrated circuits ensures that the average number of functions per unit will continue to increase. Since a 4K RAM may contain up to 14,000 transistors, relatively small unit sales of these devices can have a dramatic effect on the average number of functions per unit for the overall industry. Dataquest estimates that by late 1975 the average number of functions per device will be more than 50 and will continue to climb, as shown in Figure 1.4-1.

Unit pricing has also been affected by the great increase that has occurred in device performance, as defined by technical parameters, such as greater power-handling capability, increased speed, greater reliability, lower power consumption, and longer life. For example, one of the greatest factors in the growth of the power transistor market in the last few years was not lower prices per se, but the ability of these devices to handle either higher power or higher voltages and to do so with much greater reliability. A typical use for these devices that has not been feasible until the last few years has been in automobile ignition units. Higher speeds of integrated circuits have allowed computers to have much greater computational power using the same amount of electronics.

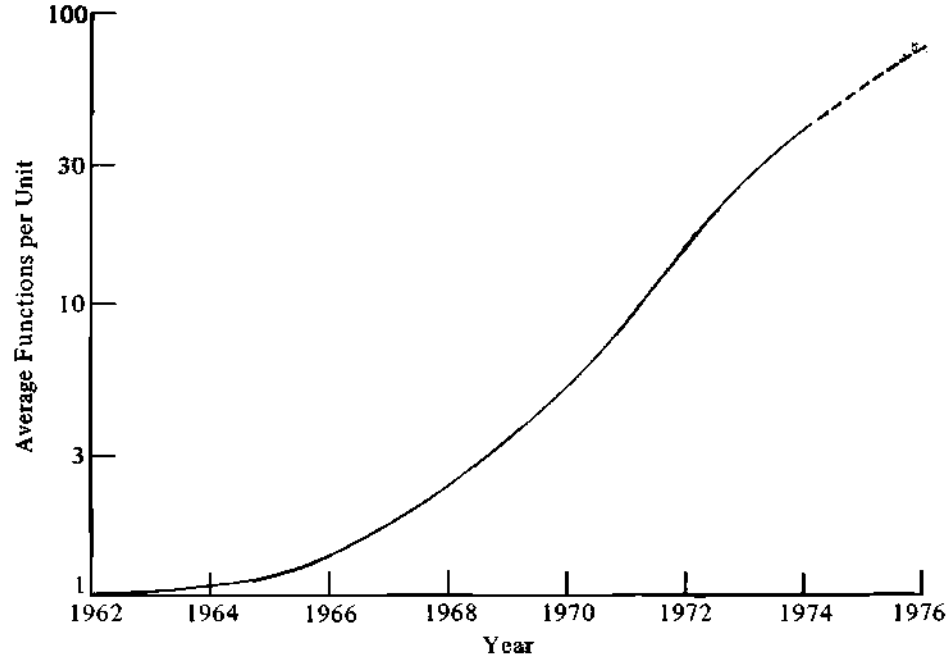
Although the list of device improvements is long, the net effect is that the user of semiconductors has had an effective price decrease either because he can obtain greater performance using the same devices, or he can use improved device performance to decrease the number of devices needed. It is not possible to quantify effectively the price deflation of improved device performance. However, in many cases, the increase in performance has been several orders of magnitude and the factor is significant.

Besides being larger (more functions) and better (improved parameters), ICs can also be more complex, i.e., more sophisticated. An example will clarify this concept. A one-chip calculator is not larger nor more difficult to manufacture than many memory devices that were earlier introduced by semiconductor manufacturers. However, it employs sophisticated systems design concepts. It is a complicated interplay between logic design, random access memories, read only memories, keyboard inputs, and display drive. Many different logic and memory designs are on the same chip, and complicated computer organization concepts are used. In other words, it is more sophisticated. This type of improvement takes time to evolve. However, it is no less important as a means of greater performance at a given price. Even if current process technology did not change for the industry, it would be many years before this type of improvement in device capability ceased.

The reasons underlying the four types of price reduction discussed above are several. The highly competitive nature of the industry

1.4 Special Industry Characteristics

Figure 1.4-1
NUMBER OF FUNCTIONS PER UNIT FOR THE AVERAGE SEMICONDUCTOR DEVICE–1962-1976



Source: DATAQUEST, Inc.

has spurred technological improvement as a means of gaining competitive advantages or opening new markets. Price decreases have come from the continuing development of old technologies and the development of new technologies, manufacturing improvements, the use of new materials (especially in packaging), the move to overseas assembly, and a large increase in unit volume.

For new products improvements in device yields, combined with larger batch fabrication have been the most significant factor in reducing the costs of semiconductor chips, and therefore prices. As a technology becomes more refined, the yields should improve for more complex or more sophisticated devices. (See the Manufacturing Chapter for a discussion of yields.)

An important concept in evaluating prices for semiconductor devices is the learning curve. The theory behind this curve, of course, holds that as accumulated unit volume for a product

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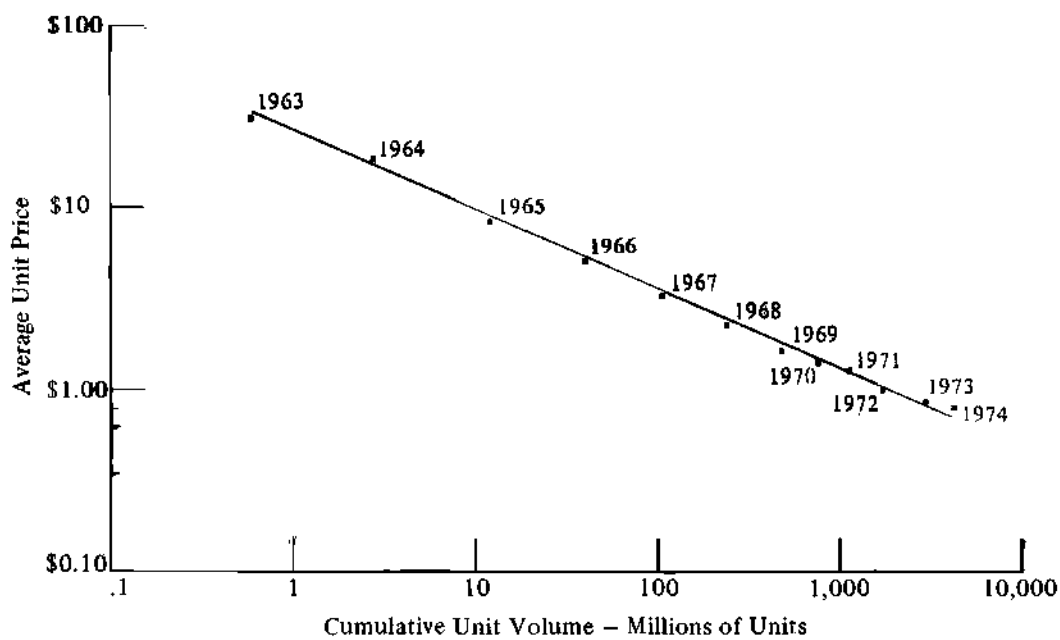
Figure 1.4-2
CIRCUIT LEARNING CURVE[1]



[1] U.S. Factory–non-Captive

Source: EIA
DATAQUEST, Inc.

increases the price will decline and that this relationship will appear as a straight line when graphed logarithmically. On an industry-wide basis, this learning curve has held true for major market segments in the semiconductor industry. Each time the accumulated industry volume doubles, the cost per unit declines by a predictable percentage. Integrated circuits have shown a 25 to 30 percent price decline for each doubling of accumulated volume, as shown in Figure 1.4-2. As the volume of integrated circuits has dramatically increased, the price has rapidly declined, in spite of increasing complexity.

It is expected that prices will continue to decrease in the future. However, these decreases are expected to come less from changes in average unit price and more from increases in the number of functions per unit and increased sophistication of the unit. Major new technological changes in the industry, such as the development of planar technology or MOS

1.4 Special Industry Characteristics

transistors in the past, are not expected in the next few years. However, the current state-of-the-art in semiconductor fabrication allows for considerable evolutionary improvement. It takes several years for many small technological improvements to have an effect on the industry as a whole. We believe that the current rate of technological progress and the eventual possibilities indicate that there will be no foreseeable change in the rate of price decreases over the next few years.

PRODUCT LIFE CYCLES

Short product life cycles are a basic consequence of the rapid change in the semiconductor industry. Any product is useful in the marketplace for only a certain period of time after its inception, but in the semiconductor industry that time can be extremely short. It is important to differentiate between the single product and the product family (in which the actual products themselves change). A product family has a somewhat longer lifetime, usually three to five years. A technology's life cycle may be even longer, since it may used for a number of successive product families.

Figure 1.4-3 shows a typical product life cycle for the semiconductor industry. After its introduction, a product rapidly increases its market—both in units and in dollars. Because initial prices are high, and decline thereafter, unit volume always increases somewhat faster than dollar volume. Initial growth may be slow, until the product is accepted, understood, and equipment designed to include it After that, unit volume grows very fast. Then, several things happen—the market for the equipment using the product becomes saturated, new equipment is designed using new improved products, and price continues to decline. Subsequently, the dollar volume of the market for the product reaches its highest point. However, if equipment using that product has a relatively long life cycle, unit volume of a particular product may remain fairly stable (or even grow somewhat) for a longer period of time, but it eventually will begin a gradual decline.

DTL integrated circuits are an excellent example of product life cycles in the semiconductor industry. The market for these circuits grew very rapidly between 1966 and 1969. After that time, new logic designs generally employed TTL circuits. However, because of the use of older equipment designs, the DTL market kept growing in unit volume through 1973. The dollar value, however, peaked in 1969 and has declined since then as the average unit selling price continued to decline.

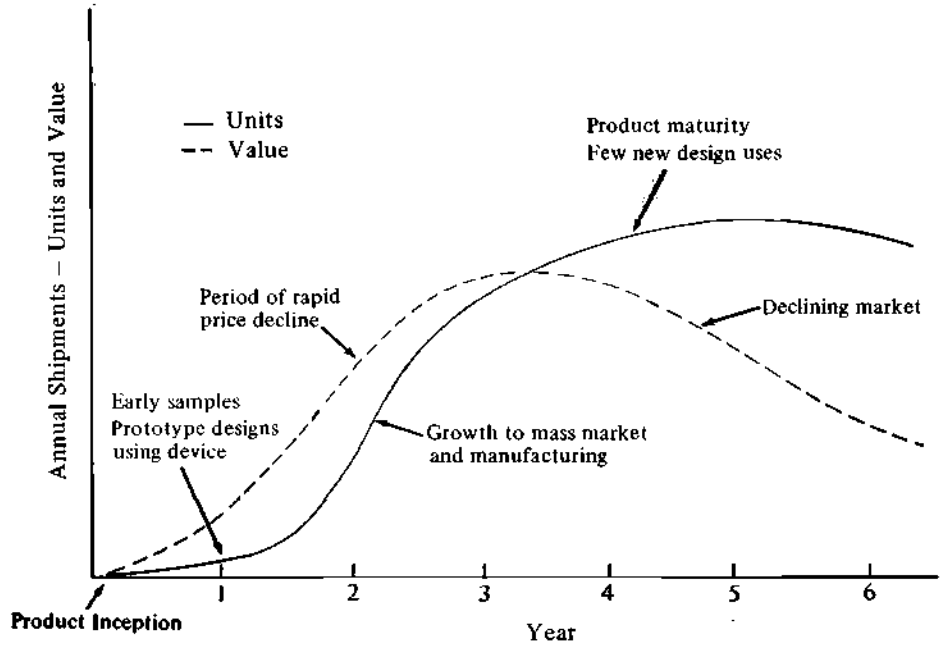
INDUSTRY MATURITY

The fact that the semiconductor industry is both young and rapidly changing is often misinterpreted, for it has some of the characteristics of both a growth industry and a mature industry. The semiconductor industry aggressively seeks new and growing markets. This, in turn, leads to rapid change and growth. Thus, the dynamic nature of the industry is probably more characteristic of industries of the future in its management of technology and technological change than a symptom of immaturity. However, there is currently no reason to believe that the industry will change this basic characteristic and start to resemble older, more stable, industries in the United States.

The industry can be characterized as being highly sophisticated especially in its use of technology, R&D, and its international marketing and manufacturing approaches. We believe that management in the industry is exceptionally competent, even though rapid change and competitive pressures often make them appear less so. It should be pointed out that some of the best managed corporations in the United States have been blatant failures in the semiconductor industry. Yet, they have often been

1.4 Special Industry Characteristics

Figure 1.4-3
TYPICAL SEMICONDUCTOR PRODUCT LIFE CYCLE



Source: DATAQUEST, Inc.

the first to condemn the successful companies in the semiconductor industry for their practices.

examples

1.5 Industry Trends

The semiconductor industry has always been characterized by change. Several important trends are now occurring within the industry, including:

- Lower cost electronics
- Market growth and penetration of new markets
- Increasing consumer products
- Greater internationality
- Increasing U.S. market dominance
- The advent of new trading partners
- An increasing number of mergers and acquisitions
- More successful vertical integration
- Continuing rapid technical change
- Increasing automation

LOWER COST ELECTRONICS

A major trend in the semiconductor industry is the continual reduction in costs and prices, resulting in the emergence of even lower cost electronics. Previous concepts of electronics as being expensive must be discarded. Cost, of course, must refer to the function that a semiconductor performs and not simply unit price. Costs can be expected to decrease in the future for several reasons:

- An increasing number of funtions on integrated circuit chips.
- Improvements in yields through larger wafers, better equipment, and improved processing.
- Greater unit volume and therefore greater efficiencies of scale.

The results of lower cost electronics are expected to become even more visible in the future. Some of these capabilities, such as in low-cost, hand-held, personal calculators, are clearly visible already. In discrete devices, much of the effect is yet to be seen, but capability has increased and cost decreased to the point where discrete devices such as triacs and SCRs are cost competitive with a wide range of electromechanical and electromagnetic components. Because these components have a definite requirement for raw materials, their costs have set lower limits. Moreover, many of them cannot be batch fabricated, allowing semiconductor devices to be more cost competitive. In the future, semiconductors are expected to become substantially less expensive than electromechanical and electromagnetic devices.

Market Elasticity

In general, decreasing semiconductor prices have opened up enough new areas of market growth to allow growth in the dollar value of the total market. In other words, the semiconductor market has a basic elasticity greater than one. Precise determination of this elasticity, however, is extremely difficult. In the first place; the effective change in semiconductor prices, as discussed previously, is difficult to measure. Second, there is a question of timing. It is apparent that changes in semiconductor prices or capability—which is the same thing—lead to the opening of new markets. However, it may take several years for these markets to develop because in many electronic systems the complexity is such that there is a long learning experience in employing new devices, designing them into systems, and developing the market for those systems. Thus, even if semiconductor prices did not change in the future, the market can be expected to expand at current prices for several years. Such items as large computers or military systems have life cycles lasting many years. With the very high rate of price declines for electronic functions, ignoring timing differences might lead one to believe that the average 15 percent rate of growth in the semiconductor industry indicated that elasticity was a little greater than one. But in many cases cur-

1.5 Industry Trends

rent markets reflect the devices developed several years ago. Today's products ensure market growth for several more years at current long-term growth rates.

MARKET GROWTH AND PENETRATION OF NEW MARKETS

Market growth, particularly resulting from the pentration of new markets, should be a continuing trend in the industry. Growth in the semiconductor market comes from either expansion of established markets or creation of new markets. However, in established markets, changing products that use more semiconductors occasionally make the difference between the two markets purely definitional. Established markets, such as those for radios or minicomputers, grow in two different ways.

- Growth in the end market. For example, the basic market for minicomputers has grown rapidly, spurring a demand for the semiconductor devices used in them. However, because of the declining prices of semiconductors, market growth must be rapid enough to overcome the effect of declining prices if the dollar market is to grow.

- Introduction of new or changed products that employ more semiconductor devices. For example, a new computer may use more electronics to make it faster or more powerful. In a number of semiconductor markets, it is common for product designers to take advantage of falling semiconductor prices to increase instrument or product capability. As a result, these markets grow through higher semiconductor content.

The largest market growth in semiconductors, however, comes from the creation of new markets. These markets exist, or come into existence, because of the increasing capabilities of semiconductor devices and their decreasing costs. There are three basic types of new markets:

- Component replacement
- Creation of completely new products
- Replacement of labor with capital

Component replacement has recently opened up some vast new markets for semiconductor devices. This market is of two basic types—individual component replacement and replacement of small systems. Individual components are replaced by semiconductors in three areas:

- Electronic components
- Electromechanical devices
- Electromagnetic devices

Basic electronic component replacement includes such items as the replacement of lights with LEDs or the substitution of semiconductors for tubes in products such as television or high fidelity equipment. The switch from electronic tubes to solid-state in color television has created a strong area of growth for the semiconductor industry in the past few years.

Large areas of future growth are expected to come from the replacement of electromechanical and electromagnetic devices, including solid-state ignition replacing traditional points, solid-state relays and SCRs replacing electromagnetic relays, semiconductor memories replacing ferrite cores, CCD devices replacing disc and drum memories, and semiconductor timing circuits replacing electromechanical devices in appliances. These new markets, especially the replacement of core memories, open up vast areas of growth for semiconductors.

At the systems level, semiconductors are replacing basic electromechanical or mechanical systems. For example, semiconductor controllers are replacing electromechanical devices in industrial control applications. Occasionally, as in watches, semiconductors replace a fully mechanical system.

In some instances, the greater capability of

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integrated circuits and their rapidly falling prices have created totally new markets. The best known of these is the personal calculator market. In this case, semiconductors have resulted in the creation of a market that never existed before. Numerous small markets of this type are being created in industrial applications.

A basic factor in the growth of the semiconductor market has been the ability of semiconductors to be applied to equipment to replace labor with capital. In some instances, this approach also encompasses mature markets. Integrated circuits have opened up many new market possibilities in such areas as computers, industrial automation, office equipement, and industrial control. These new products are primarily aimed at replacing labor or increasing productivity or both. Basic decisions by business to use capital equipment (containing semiconductors) is still a major factor in semiconductor industry growth.

CONSUMER PRODUCTS

In the past, semiconductors for use in consumer products did not represent a major market. In the last five years, however, this use has grown tremendously and this growth trend will almost certainly continue. It is a major area for future industry growth. The dollar value of semiconductor devices in consumer items in the U.S. market increased from under $100 million in 1970 to more than $450 million in 1974. As a percentage of total U.S. semiconductor sales, semiconductor devices in consumer items increased from about 8 percent in 1970 to about 20 percent in 1974.

The primary reason for this growth has been the emergence of new markets, which were spurred by the increasingly low costs of semiconductors. Current major uses for semiconductor devices in consumer items include calculators, television sets, automobiles, and cameras. The use of semiconductor devices in such consumer entertainment items as radios is a declining and less important segment of the market.

In 1973 and during the first half of 1974, the consumer market grew extremely rapidly. Much of this growth resulted from a combination of factors. First, this period marked the introduction of hand-held calculators, which represented an extremely large, new market for semiconductor devices. Hand-held calculators grew from a very small market in 1972 to more than 25 million units worldwide in 1974.

Second, this period marked the conversion of color television to solid state. Prior to this time, the majority of active components in color television sets were tubes. But rapid improvement in semiconductor devices, higher reliability, and lower prices led to a nearly complete conversion of new television sets to solid state by the end of 1974.

Third, the combination of environmental and safety considerations in automobiles, spurred by new legislation, led automotive engineers to look more closely at electronics for automobiles. This situation opened markets for solid-state ignition, seat belt interlocks, and other items. Moreover, during 1973 and the first half of 1974 there was a general boom period for all semiconductors, both in numbers of units and in prices. Price stability helped the consumer market to grow more rapidly, in dollars, than it might otherwise have.

Finally, in 1974 a considerable market for consumer devices was transferred from Japanese producers to U.S. producers, especially in calculators and television sets. For example, prior to 1973 the Japanese held over 80 percent of the U.S. market for calculators, but by the end of 1974 this market was well below 50 percent. Similarly, in 1973 the market for television sets in the United States grew rapidly at a time when Japanese production was actually decreasing. Increased automation in the assem-

bly of television sets led to greater competitiveness among U.S.-based manufacturers.

The use of semiconductor devices in consumer items is expected to continue to grow in the future, but growth is expected to be slower than in the past. Since the current market base is larger, a high percentage growth rate will be more difficult to attain, even though growth in dollar volume is considerable. Moreover, growth in the markets for semiconductors for calculators, television sets, and automobiles will very likely be slow. The calculator market is expected to saturate in 1975 or 1976 in terms of numbers of units. Meanwhile, the dollar value of semiconductor devices used for the handheld calculators has been decreasing. As a result, this market should show little growth in dollars. The conversion of television to solid-state devices has been completed. Therefore, this market can only grow if existing markets are expanded or new ones are developed. This market is fairly mature in the United States; thus, relatively little additional growth in dollars is expected for semiconductors in this application. The automobile market holds great potential for vast uses of semiconductor devices, and automotive uses for semiconductors are expected to keep increasing in the future. However, this market has been slowed by decreased automobile sales in 1974 and the first part of 1975, extremely conservative approaches by automobile manufacturers, and greater realization of the economic impact of environmental and saftey legislation. The overall result is a slowing of the introduction of electronic devices in automobiles. Ultimately, however, the use of microprocessors in automobiles holds the promise of a vast improvement in engine performance.

In addition to automotive uses, several other new markets for consumer items, including appliances, cameras, and watches and clocks, are growing rapidly. Appliances include a number of timing and control functions that could be performed by semiconductors. This market competes primarily on a cost basis. Although the market is expected to be very large, it may take some years to reach fruition. Cameras use semiconductor devices for timing, light measurement, and motor control. Although limited, this market is expected to grow. The largest new market for semiconductor devices is in electronic watches. About 5 million watches are sold each year in the United States at prices over $50 per watch, representing an excellent market opportunity for electronic watches. There are other very exciting possibilities for wrist electronics, such as body monitors, which bode well for this marketplace. The market for electronic watches is expected to grow very rapidly in 1975 and 1976. Its ultimate growth, of course, will be determined by three major factors: cost, performance, and consumer acceptance.

These markets, together with a very wide range of many smaller markets that may open in the future, promise that the trend toward increased use of semiconductor devices in consumer items will continue. It is also possible that large new markets, such as the calculator market, may appear.

INTERNATIONALITY

The semiconductor industry is highly international in scope and outlook, and this characteristic is expected to increase even further in the future. The international character of the industry is present both in marketing and in manufacturing. Most U.S. companies derive about 15 to 30 percent of their revenues from foreign sales, with the average probably above 20 percent. As foreign markets increase, these percentages are expected to increase. International marketing is a necessity, because marketing on a worldwide scale provides additional sales to support efficiencies in manufacturing. Thus, even modest foreign sales can increase

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profits markedly.

Japanese and European companies have been reluctant in the past to market outside their own geographical areas, but are expected to become much more aggressive in foreign markets in the future. All semiconductor manufacturers today are aggressively pursuing expansion of their international marketing, most noticeably in Japan. Japan has recently lifted restrictive import quotas on semiconductors, and a large potential market has been opened to non-Japanese manufacturers. Thus, many companies are actively increasing their marketing efforts in Japan. At the same time, Japanese companies, with less domestic protection, are looking at U.S. and European markets.

Foreign manufacturing is increasing for two reasons. First, the manufacture of semiconductor devices has areas that are capital and technology intensive and areas that are labor intensive. As a result, it is generally cost-effective to do the capital- and technology-intensive manufacture in areas such as the United States where technical personnel and equipment are more available and to do the highly labor-intensive manufacturing, i.e., assembly, in areas where labor costs are low, such as Asia. It is not unusual for wafers to be fabricated in one country, devices assembled in a second country, and final testing and shipping to be performed in a third country. This highly mobile means of manufacturing is made possible, of course, by the small size and low weight per dollar value of semiconductor devices. Searches to seek out the most cost-efficient allocation of manufacturing has led more and more companies to invest in overseas assembly plants. This trend is expected to continue, even though it may be slowed eventually by increased automation.

The second reason for international manufacturing is the desire of the consuming country to have the manufacturing process performed locally. This approach is encouraged in a number of ways, especially through import quotas and high tariffs and duties. These nationalistic attitudes place a strong pressure on U.S. companies to achieve even greater internationality.

Table 1.5-1
ESTIMATED
SEMICONDUCTOR MARKET
SUPPLIED BY U.S. COMPANIES

Year	Percent of Market
1970	55.0%
1971	57.3%
1972	58.4%
1973	59.1%
1974	62.1%

Source: DATAQUEST, Inc.

U.S. companies now have an estimated 95 foreign manufacturing plants. The number of foreign operations of European and Japanese companies, however, is very small. Competitive pressures will ensure that the number of such operations increases.

U.S. DOMINANCE

U.S. companies have always supplied a majority of the semiconductor devices produced in the world, and this dominance is increasing. For several years, U.S. companies gradually lost market share to European and Japanese manufacturers and in 1970 the share of the world semiconductor market controlled by U.S. companies was at its lowest point. Since that time, the market share of U.S. companies has been increasing. In 1974 U.S. companies controlled an estimated 62 percent of the total world semiconductor market and about 75 percent of the total world integrated circuit market (more than 80 percent including captive manufacturers). Table 1.5-1 shows the percentage of the world's semiconductor market that is supplied by U.S. companies.

1.5 Industry Trends

The short-term advantage of U.S. companies results from:

- Structural market position
- Changing end markets
- Easing of Japanese import restrictions

United States companies are positioned in the fastest growing semiconductor market segments. They have a much larger share of the integrated circuit market than they do of the discrete market. U.S. companies have their largest integrated circuit sales in MOS devices, and nearly as large a market in bipolar digital devices. Their lowest market saturation is in linear devices. Since the integrated circuit market is growing faster than the discrete market, the market segments now served by U.S. companies will ensure that their current share of the total world semiconductor market will increase. Similarly, because the MOS market is the fastest growing integrated circuit market and the linear market is the slowest growing, U.S. companies should increase their share of the integrated circuit market. Paradoxically, U.S. companies could lose market share in every market segment, yet still increase their total market share in integrated circuits or all semiconductors.

The manufacture of number of items using semiconductors has been returned to the United States, or will be in the near future. This change makes those semiconductor markets more accessible to U.S. companies. For example, calculators resulted in about a $50 million shift in semiconductor use from Japan to the United States between 1973 and 1974—more than a 1 percent shift in total semiconductor market share. Another significant change has been an increase in the U.S. manufacture of television sets. Since 1972, U.S. consumption of semiconductors has been growing faster than either Japanese or European semiconductor consumption.

In the past, Japan has restricted total semiconductor imports to about 15 percent of the total Japanese market. The majority of these imports were of integrated circuits. In December 1974, the Japanese government discontinued its import quotas on semiconductors and its restrictions on the manufacture of semiconductors in Japan by U.S. companies. This move allowed U.S. companies to penetrate the Japanese market more fully. In the past 12 months, imports of integrated circuits into Japan have increased from less than 25 percent to more than 30 percent of Japanese integrated circuit consumption.

U.S. companies have traditonally had, and should continue to have, three major advantages:

- Technical superiority
- Market strength
- Weak foreign competition

However, as U.S. companies transfer more and more manufacturing to foreign plants, the transfer of technology has been more rapid and the technical superiority held by U.S. companies has been diminishing.

Few foreign companies have gained a strong foothold in the manufacture of integrated circuits. Severe price competition in some foreign markets has tended to keep U.S. suppliers dominant. With greater market share, that position can be maintained. A number of factors, however, mitigate against the market advantages of U.S. companies. These factors are primarily political, spurred by nationalistic feelings. Foreign governments have attempted to set up strong barriers to increased market dominance by U.S. companies and to provide advantages to local companies. Such barriers include strong pressure on users to purchase from domestically owned companies (especially in the military market), direct and indirect subsidies, high tariffs and duties, import quotas and restrictions, and other forms of government control. Because of these strong pressures, it is unlikely that U.S. companies will ever be able to increase by more than a few percent the

share of the world integrated circuit market that they now hold. Any higher increase would only invoke a stronger reaction from foreign governments. It should be noted, that the data mentioned above include only noncaptive manufacturers. Both IBM and Western Electric, which have a combined estimated output of more than $800 million in semiconductors, are not included. If their production companies are included, the market share controlled by U.S. companies becomes significantly higher.

NEW TRADING PARTNERS

The traditional markets for semiconductors have been the United States, Europe, and Japan. Increasingly, however, new markets are being developed in the rest of the world. Although these markets today are small, Dataquest expects them to grow very rapidly in the future. The development of these markets is occurring for several reasons.

- Rapidly increasing worldwide industrialization
- Increasing world use of technology
- Increasing world trade
- Fewer defense restrictions on semiconductor sales
- Increasing assembly of devices employing semiconductors in low labor cost areas

These factors tend to nurture market formation and growth outside the traditional markets.

As a consequence, the semiconductor manufacturers are seeing the development of many new trading partners. We believe that in the future the foremost among major areas concerned will be:

- China
- The Middle East
- The Eastern Bloc

China has had rapid industrial growth, albeit from an extremely small base. In the past, it has had little need for semiconductor devices and the market has been small. This has been further compounded by political implications, lack of foreign capital, and a decision by China to try to develop its own industry. Nevertheless, China is attractive because of the vast potential market that it represents. As its industry grows, it will need an increasing quantity of semiconductors and it will not be able to supply many of these needs on its own.

The vast influx of petrodollars into the Middle East has drastically changed the potential market in this area. Although at this time there are few primary markets for semiconductor devices in the Middle East, recent purchases of equipment (especially military equipment) by these countries have had significant semiconductor content. The drive of these countries to industrialize eventually will almost surely include technological areas. Recently, several of these countries have expressed a keen interest in acquiring such capabilities. How large these markets become depends on the continued influx of petrodollars into these countries. But the Middle East can no longer be ignored by the semiconductor industry.

Eastern Europe supplies much of the electronics technology available to the Communist world. But, despite the capabilities of the Eastern Bloc in technology, their semiconductor manufacturing capability is low. With the lowering of political trade barriers and restrictions on exports of semiconductors, these countries will provide a large and growing market for the semiconductor industry. The potential annual market in this area is probably several hundred million dollars.

As the world becomes more industrialized, other markets will also open. Brazil is an example of such a potential market.

MERGERS AND ACQUISITIONS

There have been relatively few mergers or

acquisitions in the semiconductor industry in the past. However, Dataquest believes that this trend will change and that mergers and acquisitions will increase in the future. Several basic conditions support this belief. First, currently there are a very large number of semiconductor companies, about 70 companies are active in the United States and an equal number in the rest of the world. Even with the wide product diversity in the industry, the world market probably cannot support more than a fraction of those companies on a competitive basis as the industry matures. For this reason, many companies will either have to sacrifice growth and remain in specialized markets or merge with other companies.

The need for financial resources will also tend to foster mergers. In general, companies in the semiconductor industry are limited in their financial resources, and as the market grows these financial resources will be strained. This problem will be exacerbated by increasing automation within the industry. Whereas equity financing by the public has been a possibility in the past, stock prices for semiconductor companies are currently near their lowest historical point. In the last two years, the equity market for small companies has been essentially nonexistent. As a result, many companies cannot look to equity for financial resources.

On the other hand, many systems companies have been actively seeking in-house semiconductor capabilities. They realize both the difficulty of starting up a capability themselves and their limitations in understanding the semiconductor industry. These considerations lead them to seek acquisition of an ongoing company.

The combination of these factors should lead to more acquisitions or mergers of semiconductor companies. Two or more companies combined can provide broader product diversity and broader worldwide marketing capability. As in the past, one major deterrent to mergers and acquisitions has been that the management of many semiconductor companies strongly value their independence.

VERTICAL INTEGRATION

Possibly the most important trend in the semiconductor industry is toward vertical integration. In the past two years, the thrust toward this approach has increased tremendously. By vertical integration, we mean the manufacture of semiconductors by a company for the assembly of systems by that company. Although vertical integration has always existed to some extent, the manufacture of semiconductors and the manufacture of systems have usually remained relatively independent. Even though semiconductor manufacturers have had divisions that produce systems, as at Texas Instruments, these divisions have generally operated independently of the semiconductor manufacture and true integration has not taken place. Integration must be considered in two ways—the upward integration of semiconductor manufacturers into the manufacture of systems and the downward integration of systems companies into the manufacture of semiconductor devices for their internal use.

Upward Integration

The benefits of greater vertical integration have always been a controversial subject in the semiconductor industry. In the past, attempts at more vertical integration have not been particularly successful for several reasons. First, until recently the semiconductor content of most electronic systems was relative small, averaging about 5 percent of the manufacturing cost of the system. Thus, to enter into the system business, a semiconductor manufacturer would have to learn the remaining 95 percent of the business. Second, an entirely new marketing organization would be required, new marketing

techniques would have to be learned, and the costs of market pentration would be a major problem. Generally, early attempts at upward integration were unsuccessful.

Recently, however, upward integration has become much more widespread and has been fairly successful. The manufacture of calculators has been the primary means of entry. Entering this field has added significant dollar volume to the semiconductor groups of Litronix, National Semiconductor, Rockwell International, and Texas Instruments. Other areas being expanded with upward integration include memory systems, minicomputers, point-of-sale systems, watches, and a number of components devices such as transducer systems and solid-state switches. Dataquest believes that the number of items being manufactured by the semiconductor companies will increase and that the resulting dollar volume will expand rapidly over the next five years.

There are a number of reasons why the trend toward vertical integration has become more successful, including:

- Increased portion of system design performed at the semiconductor (IC) level
- Greater dollar percentage of semiconductors in systems
- Lower assembly costs

The rapidly increasing complexity of integrated circuits, typified by large-scale integration (LSI), has meant that an ever-increasing portion of the engineering design must be performed prior to manufacture of the semiconductor device. Consequently, there has been a major shift in the value of systems design from the systems manufacturer to the semiconductor manufacturer.

The decreasing cost and increasing performance of semiconductors has made it cost-effective to add an increasing number of performance features to most systems. These same capabilities have allowed semiconductors to perform more tasks in a system by eliminating other components, resulting in a vastly increasing number of semiconductor devices in a system relative to other components. For some systems, the value of semiconductors is running as high as 20 percent of the total final manufacturing cost of the system.

The effect of greater complexity of integrated circuits has been that a much smaller number of devices are being used for any given system—even though their dollar value may be greater. Consequently, the assembly cost of the system, especially labor, has come down very significantly. Of more significance, is the fact that many costs (e.g., packaging) are relatively fixed. But those costs that are truly variable and determine the competitive position of the manufacturer, for many products, are now controlled mainly by the semiconductor manufacturer. Therefore, vertical integration is not only feasible and profitable for many products, but in some cases (such as calculators) almost mandatory for company survival.

Although marketing of a final product is still a major problem for semiconductor manufacturers, there are a number of products that can be marketed relatively easily. These products include items, such as calculators, or products, such as memory systems, that can be merchandized to OEM customers. Semiconductor companies have been rapidly improving their competence in marketing non-semiconductor products and systems. Recently, semiconductor companies have been creative in forming new types of marketing or distribution approaches to make their entry into new product areas easier, particularly with respect to calculators and watches, where tie-ins with mass merchandisers have been instrumental in easing their market entry.

The manufacture of calculators has been the greatest success in upward integration recently experienced by the semiconductor manu-

1.5 Industry Trends

facturers. For low cost, hand-held calculators, the semiconductor manufacturer has had a distinct cost advantange over the assembler. In 1974, a large percentage of the manufacturers of calculators switched from assembling calculators to manufacturing semiconductors. This trend should continue during 1975 and 1976 until virtually all small calculators are manufactured by semiconductor companies. Current large calculator manufacturers that produce semiconductors include Texas Instruments, National Semiconductor, Rockwell International, and Litronix. Hewlett-Packard is also a major calculator manufacturer, but has not been a large integrated cirucit manufacturer. However, it is believed that this company will manufacture an increasing number of the semiconductors used in its calculators. The recent problems of Bowmar have been an example of the problems calculator assemblers face. Many Japanese calculator assemblers have also lost significant market share.

Recent interest has focused on electronic watches as another major area where vertical integration is promising. Although there are some questions as to the size of the market for electronic watches, the semiconductor companies have a distinct technical and cost advantage in the manufacture of the basic modules for these watches. Marketing electronic watches is difficult, which may prove to be a problem for the semiconductor companies. Nevertheless, Dataquest believes that the basic module will be manufactured by current semiconductor manufacturers. Semiconductor manufacturers now making watch modules include Hughes Aircraft Corporation, National Semiconductor, American Microsystems, Intel, and Litronix.

Several semiconductor companies have recently been improving their capabilities for manufacturing memory systems, especially add-on memory systems for IBM computers. Production of these systems was pioneered primarily by Advanced Memory Systems, but other companies, such as Intel and National have been growing more aggressive in this area. Entry into this segment will give them the capability to sell semiconductor memory components, memory boards, or memory systems. Since a very high percentage of the cost of add-on memory systems is accounted for by semiconductors, these systems are a natural area for vertical integration.

Very small computers will very likely be another fertile area for vertical integration by the semiconductor companies in the future. The recent advent of the microprocessor—i.e., a computer processor on a single chip—is a precursor of the transfer of the systems capability to the semiconductor companies and the continuing increase of the level and complexity of integration in LSI devices. Microcomputer chip systems, including the processor and associated memory chips, are becoming more common. It seems clear that semiconductor companies will market chip sets, sets assembled on a single PC board, or in some cases the entire microcomputer. Generally, these products will be marketed to OEMs who will then market the complete systems to the end user. This capability will mark a significant step in vertical integration for some semiconductor companies. As levels of chip integration increase, the processes will become more and more complex, and chip systems should rapidly approach the systems performance of today's minicomputers. As a result, the assembly of small computers will rapidly become the domain of semiconductor manufacturers.

Semiconductor manufacturers are beginning to make more and more components that are primarily functional blocks which are entirely electric and cannot be fully integrated into a single chip. Typical of such products are such items as solid-state switches, simple transducer systems, and LED displays. Slightly higher levels of integration, such as amplifiers or A-D converters, still require significant cus-

tom engineering input and, as a result, these components are still primarily the domain of specialized manufacturers. As some of these devices become increasingly standardized, however, it is possible that the manufacture of these devices will shift steadily to the semiconductor companies.

Today's trends imply that vertical integration by the semiconductor manufacturers will rapidly increase in dollar volume. These manufacturers will produce a growing number of semiconductors for captive sources. However, Dataquest expects that the majority of semiconductor devices will still be marketed competitively.

Vertical integration is not without hazards, however. In particular, semiconductor companies that integrate vertically face problems of manufacturing and marketing in areas with which they are unfamiliar. They also face greater exposure to the risk that changes in technology may undermine their competitive position.

However, these potential areas for integration require financial support to penetrate them. Most semiconductor companies have limited capitalization, and the relatively high growth rate of the semiconductor industry requires considerable capital to finance that growth. Companies integrating vertically may be expected to limit themselves to areas that do not require excessive financing.

Downward Integration

Historically, integration downward toward the manufacture of semiconductor devices has been less than successful. A very large number of major corporations have, at one time or another, attempted the manufacture of semiconductors. Corporations that were unsuccessful in this venture include Ford, General Telephone, Union Carbide, Lockheed, Boeing, Westinghouse, and General Electric in integrated circuits. The major large corporations today with captive semiconductor facilities are IBM, Western Electric, and General Motors. It is not clear whether or not the semiconductor facilities of these companies are totally competitive. Nevertheless, it has been the policy of these companies to perform as much of the manufacturing of their products as feasible. These three corporations also have one major advantage—each company is sufficiently large that its internal demand for semiconductors allows its semiconductor facility to have required economies of scale. Few other corporations have this advantage.

Other companies have had many problems integrating downward into semiconductors including:

- Inability to attract qualified semiconductor personnel, either because of low pay scales, poor locations, inability to offer stock options, or other considerations.
- Lack of full understanding of the semiconductor industry, especially the dynamic rate of change, the decreasing costs and prices, and the interplay of technology in the marketplace.
- Lack of management attention since the prime business of the company is in other areas.
- Insufficient in-house demand.

Currently, systems companies have taken a new approach to downward integration. Some companies are opting to establish small semiconductor facilities that can be used for other than the large scale manufacture of in-house needs. The small facility allows manufacture of small quantities of proprietary devices, the design and testing of devices to be manufactured by others in larger quantities, and a facility

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where systems engineers can interface more closely with the manufacture and design of ICs.

Such capabilities can provide strong advantages for the systems companies. Moreover, the company always has the option to expand production later. This type of small facility has been most fully exploited by Hewlett-Packard, which uses its semiconductor facilities to produce many small quantity proprietary devices used in Hewlett-Packard's instruments and EDP systems. An additional incentive for systems companies to integrate downward is the potential for achieving fuller control over the manufacture of components for systems produced internally.

Semiconductors hold a unique fascination for many people. Because of this fascination, there is strong pressure in many companies to establish semiconductor facilities. Both real and fancied advantages of in-house facilities indicate that increasingly more systems companies will establish semiconductor production operations. Currently, many EDP systems manufacturers are investigating the outlook for establishing facilities to manufacture semiconductors. For standard items, it is clear that many of these companies may not be competitive. Nevertheless, by their very existence they will add competitive pressure to the market. The total volume produced by these companies, at least in the foreseeable future, is not expected to be significant.

AUTOMATION

Automation of semiconductor manufacturing is increasing in the semiconductor industry, continuing a trend followed over the past few years. However, the level of automation has always been a subject of controversy in the semiconductor industry because automation has both advantages and disadvantages. Several factors currently work toward increased automation in the industry. They include:

- A current low level of automation
- Increasing labor costs, tariffs, and freight rates
- Larger volume
- Greater standardization

In spite of the large amounts of sophisticated capital equipment required to manufacture semiconductors, the industry is still highly labor-intensive. Labor costs amount to at least ten times amortized capital costs—building and equipment depreciation or rent. As a result, productivity in the industry is low. The semiconductor industry as a whole has one of the lowest ratios of revenues per employee or assets per employee of any U.S. industry. Company estimates are shown in Table 1.5-2. Variations in company growth rates, layoffs at the end of 1974, and company revenues from other product lines distort these ratios somewhat.

Some areas of semiconductor manufacturing, especially assembly, are performed overseas where low labor costs can substitute for the capital costs that would be incurred using more automated assembly operations in the United States. However, this area is becoming more expensive because of rapid wage inflation in many parts of Asia. Wages have increased

Table 1.5-2

ASSETS AND REVENUES PER EMPLOYEE—1974

	Assets Per Employee	Revenues Per Employee
Fairchild	$16,414	$21,276
Intel	23,940	42,684
Motorola	14,262	26,807
National[1]	5,700	12,118
Texas Instruments	14,731	23,998
Fortune 500	33,688	46,200

[1] Year Ending May 31, 1974

Source: DATAQUEST, Inc.

by as much as four times in the past year and one-half. Additionally, there has been increasing concern over tariffs and duties particularly sections 806/807 (which deal with the rates applied to the industry) as intrepreted by the Commerce Department. Regulated freight rates are also an important cost factor for Asian assembly. A recent FCC decision has allowed a 60 percent increase in freight rates charged to some semiconductor companies. These artificially high rates may be circumvented in the future by companies that purchase and operate their own airplanes.

Between 1967 and 1974, the volume of integrated circuits increased over 20 times and volume should increase further in the future. In addition to this volume increase, several devices are becoming industry standards and are manufactured in extremely high quantities. Greater volume makes automation more economically feasible. All of these factors argue for increased automation. On the other hand, some factors will slow automation, including:

- Lack of capital in the industry
- Continuing technical changes
- Availability of adequate equipment

Since the industry, in general, is underfinanced, it cannot afford a great deal of capital equipment without a large infusion of equity. The continuing evolution of the technology and consequent rapid obsolescence of products and equipment tends to lower the expected return on investment for equipment. In the past many companies have been severely affected by the rapid obsolescence of capital equipment.

Finally, and perhaps most important, has been the lack of adequate automated equipment. Equipment for the semiconductor industry has very special requirements, and in many cases effective design has not yet been evolved.

Two areas that are highly labor-intensive could stand more automation; they are mask alignment and lead bonding. Mask alignment is primarily done in the United States because it is an integral part of wafer fabrication. Automatic aligners are beginning to appear and they should see greater acceptance in the future. Lead bonding is performed mainly in the Asian assembly facilities. Whether this step should be automated recently became a very controversial subject. We believe that increased automation will occur eventually. Adequate automated bonding machines have not been designed at this time, however, but they are certainly technically feasible. Both Texas Instruments and Motorola have major in-house programs to develop improved bonding equipment.

Other potential areas of automation are less dramatic but equally important and costly, including equipment that does not deal with new tasks but upgrades current equipment. In general, newer, more automated equipment will have three major capabilities:

- The ability to handle larger batches
- Faster throughput or higher productivity
- Greater adaptability to different devices

There are important consequences of the shift toward increased automation. First, more production will be performed in the consuming nation—that is, manufacturing will be performed wherever the market exists. Increased automation should make the higher labor costs of these market areas less important. Second, the industry will become less labor-intensive, with higher fixed costs. Finally, underfinanced companies that cannot afford automated equipment will be at a competitive disadvantage.

Although automation will continue to increase in the future, the countervailing problems associated with it indicate that current rates of increasing automation will not accelerate greatly. In general, the ratio of labor costs to capital costs are expected to decrease slowly.

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ECONOMIC CYCLES

A major problem in the semiconductor industry is the effect of cycles in the general economy on semiconductor markets. Small changes up or down in the general economy are magnified several times in the semiconductor industry. This problem arises because the basic market for semiconductors—about two-thirds of the U.S. semiconductor market—is accounted for by capital equipment. These items, in general, are purchased for expansion of industrial capacity or productivity. When the economy is expanding, industry expands its capacity and there is a good market for equipment using semiconductors, but when the economy is not doing well the market for such items as computers is diminished considerably. Table 1.6-1 shows this effect quantitatively.

In good years such as 1966 and 1973 when the economy was doing well, the semiconductor industry had high market growth. However, in years when the economy was in a slowdown, such as 1967, 1970, and 1975, the semiconductor market has been very poor. The large swing in market growth, over a range from minus 15 percent to plus 45 percent, shows the extreme sensitivity of the industry to the economy. The retaliation of the industry to the economy is discussed in more detail in Section 2.1, Econometric Model.

Such rapid changes in the semiconductor market, of course, pose some difficult problems for the industry. In very good times it is difficult for companies in the industry to adjust to the rapid growth—such as in 1973. In difficult times, these companies face the task of cutting production. In such times, individual companies must make hard decisions on prices. They must choose, in essence, between profit margins or retaining market share. A company often faces the dilemma that if it tries to retain its profits, its market share will shrink so drastically that its efficiencies of scale will disappear and its profits with them. Because the industry is highly competitve, this decision generally means that profits suffer. In 1970 and 1971, when semiconductor demand decreased, the semiconductor industry was grossly unprofitable, with only six companies out of about 70 remaining profitable.

Because the semiconductor industry is basically labor intensive, the industry has only one prime method of cutting costs—and that is by reducing employment. Laying off of employees is painful, of course, not only for personal reasons, but also because any employee represents a considerable investment in training. Severe reductions in employment can reduce the ability and speed with which a company can return to normal levels. Product development can also be slowed if engineers are laid off. It is clear that down cycles in the economy have been a major factor in the high mobility of employees in the industry. Moreover, since the more experienced and more productive workers are usually retained, initial reductions in employment in a semiconductor company have little effect on production. In general, it takes about a 20 to 25 percent reduction in employment to decrease unit output by 10 percent. As a result, employment reduction must be very severe to obtain measurable results.

CAPACITY

Industry overcapacity has always been a particular problem in the semiconductor industry. This results from several factors.

- The ability to expand rapidly
- A desire to gain market share
- Preparation for rapid market expansion
- Too many companies operating in the industry

Under favorable market conditions, the industry can expand very rapidly. Because de-

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mand was in excess of supply in 1973, the year provided a good measure of how fast the industry can expand. In that year, the industry expanded at the rate of about 10 percent per quarter. None of this expansion was due to price increases. In most instances the semiconductor industry can expand fast enough so that the limited capacity situation rarely ever occurs.

Table 1.6-1
SEMICONDUCTOR INDUSTRY GROWTH

Year	Real GNP Growth	Industry Growth
1973	5.9%	39.2%
1966	6.5%	30.3%
1975	Down	-17.2% est.
1970	-0.4%	-8.7%
1967	-2.6%	-2.5%

Source: DATAQUEST, Inc.

Market share can be extremely important in the industry. Companies often expand capacity in anticipation of securing an increased market share, even in poor markets. Generally, however, expectations exceed reality, leading to overcapacity.

The sensitivity of the semiconductor industry to the economy means that when the economy is on the upgrade semiconductor demand can expand very rapidly, especially in selected market segments. Therefore, companies are ill-advised to operate too close to capacity when the market turns up or they may not be able to grow with the market. In particular, companies should try to make sure that long lead time items in capacity expansion never become a limiting factor.

There are probably too many companies, with too much capacity, in the semiconductor industry. This situation results primarily because starting a semiconductor facility has become a consuming fascination for many.

Since the semiconductor industry is highly competitive, the effect of excess capacity is twofold: prices are always under extreme pressure and profits are rarely very high. Some manufacturers, such as those mentioned above, can withstand large losses and prices below cost for long periods. But this is a continual problem for the legitimate companies in the business, since it erodes their profits and markets. The problem of capacity will probably not disappear. However, as technology evolves more slowly, competition for market share may become less severe.

SHORTAGES

The semiconductor industry uses a wide range of materials. As a result it often finds that one or more of these materials are in short supply, especially in times of general world economic expansion. In the past, there have been shortages in copper and some chemicals such as hydrochloric acid. Rapid semiconductor industry expansion creates shortages of its own. In 1973, for example, there were shortages of silicon, glass quartz diffusion tubes, and packaging. The suppliers of these items had difficulty expanding fast enough to meet industry demands. Glass diffusion tubes, for example, are produced from a special type of quartz. Much of this quartz is mined in Brazil, shipped to France where the tubes are made, and then shipped to the United States. Not only is there a long lead time, but the manufacturers of the quartz glass are not inclined to make rapid expansions to meet short-term demands.

A particular problem that concerns the semiconductor industry is the possiblity of a shortage of electric power. Electricity is necessary for the production of diffusion tubes and the powering of depositions, epitaxial reactors, as well as all other types of testing and assembly equipment. Other power sources cannot be substituted. Needless to say, a shortage of electric power could shut the industry down. Al-

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though that is highly unlikely, the imposition of quotas during a general power shortage could halt industry expansion and penalize fast growing companies. Shortages may not be avoided, but they can be alleviated if they are detected early and the problem is communicated both to industry and to suppliers and steps are taken to minimize problems.

CAPITALIZATION

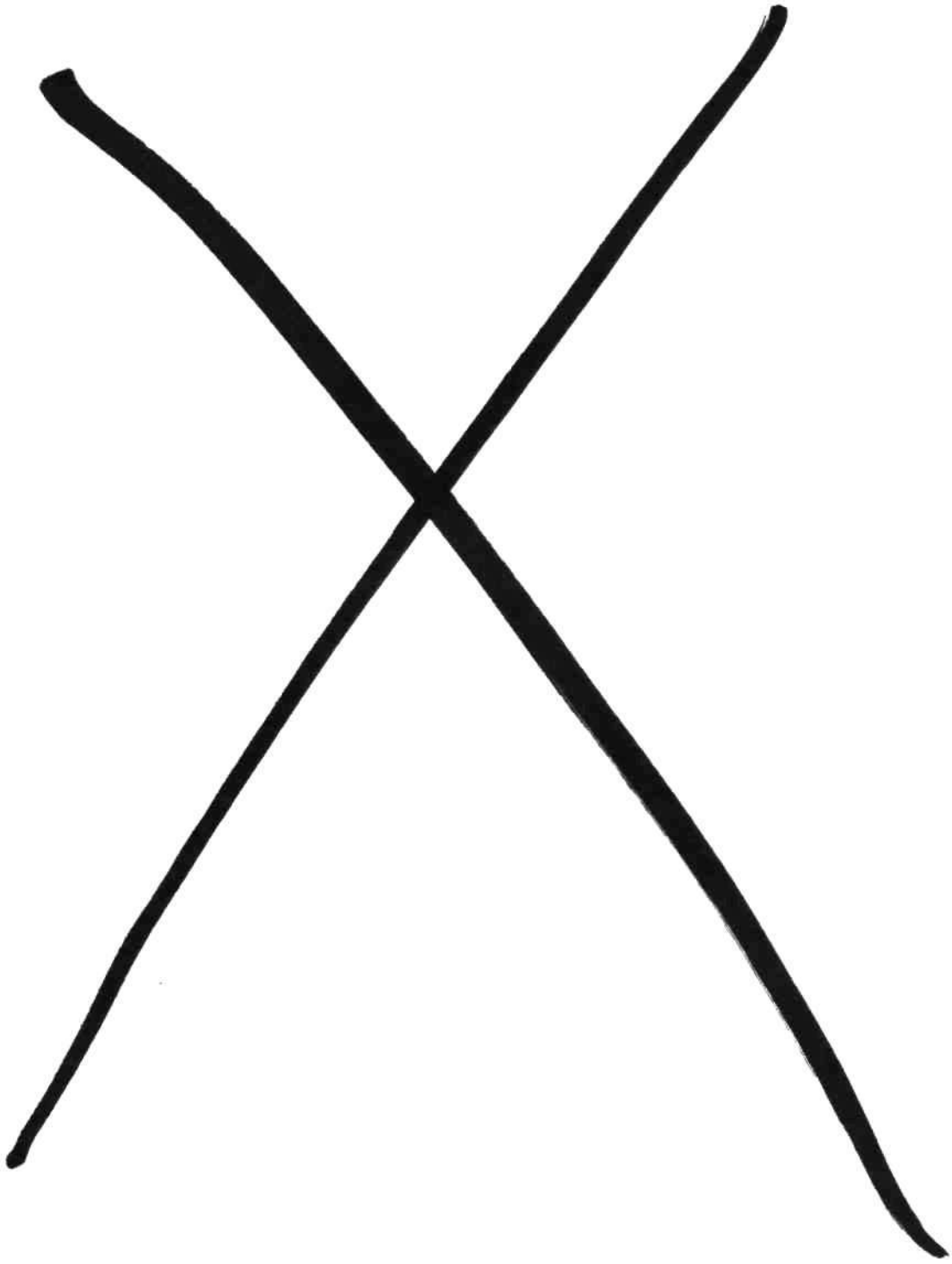
Undercapitalization will most probably be a severe problem for the industry in the future. Historically, the industry has been somewhat underfinanced, partially because of the rapid growth in the industry. In the future, the semiconductor industry will need financing for two major reasons—to grow and to automate.

Assuming normal growth in the general economy, the semiconductor industry should grow at an average annual rate of about 15 percent. This growth will require considerable expansion in buildings, equipment, inventories, and receivables. A larger financial need, however, will come from the requirement for increased automation. The industry has always been labor-intensive. For several measures of worker productivity—such as assets per employee, sales revenues per employee, and the cost of buildings and equipment as a percentage of revenues—the semiconductor industry is at one of the lowest levels of any industry in the United States. Large increases in expensive equipment will be required to increase worker productivity.

The basic need for capital within the industry could have three major effects. First, companies with cash will have an advantage. Texas Instruments is the only independent semiconductor company with a large cash inflow. The importance of financing may also be a benefit to semiconductor manufacturers that operate as divisions of large corporations which can supply the necessary financing. Second, if the stock market improves many companies will go to the equity market to obtain financing. At this time, however, most companies are selling at market prices well below book value (which has always been low anyway) and, thus, are extremely reluctant to sell stock. Finally, the lack of cash in the industry is apt to slow automation. Companies will continue to turn to overseas operations or to utilize three shifts a day to obtain the greatest benefit from their existing equipment.

OTHERS

Many other lesser problems arise in the semiconductor industry. These problems are caused primarily by the rapid changes in the industry, the high technological content of the products, and the relative immaturity in the market that the industry serves. For example, the industry serves markets that can grow, or disappear, overnight. This has been true to a large extent in the calculator market which has had several major shifts in only a few years. Managers in the industry have to anticipate changes both in prices and technology to be effective. Short product lifetimes, which are characteristic of the industry, mean that a high proportion of funds must be committed to the research and development of new products. Rapid changes in markets and in products mean rapid changes in market shares. This condition lends a high degree of instability to the industry and the companies in it.



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GENERAL INDUSTRY FORECAST

The basic outlook for 1978 U.S. semiconductor shipments remains relatively unchanged from the presentations made at our October 21, 1977, SIS Conference. U.S. factory shipments in 1977 are expected to be about 12 to 13 percent above 1976 levels, and U.S. factory shipments in 1978 are expected to increase about 15 percent over 1977. Quarter-to-quarter growth is still expected to be erratic.

Our general industry forecast has been delayed for two reasons: first, both our forecast in July and our forecast at our October Semiconductor Industry Conference contained an error overstating discrete device shipments and market growth, which is now corrected; second, for timing considerations, our forecast will now be put out at the end of each quarter, i.e., December, March, August, and September.

This is the last industry forecast in which we will estimate U.S. factory shipments. In future forecasts, we will employ U.S. consumption figures. Because consumption does not include devices shipped overseas, it is more closely related to the U.S. economy. In addition, data will be comparable to that reported by the SIA. The cooperation of several industry market researchers has now made adequate historical data available for our regression models.

Given the performance of the U.S. economy, semiconductor shipments in 1977 have been below expectations. Nearly all models of industry demand indicated increases of shipments in 1977 over 1976 considerably higher than the 12 to 13 percent that will actually result. There appear to be several reasons for this:

- The major reason is the lack of economic growth in Europe and Japan. Year-to-year growth in industrial production in Western Europe is flat to slightly down. Industrial growth in Japan this year has been about 2 percent, with rapidly increasing inventories and higher exports. Because these markets are very poor, they affect the decisions of all companies, particularly the large U.S. multinationals having excess capacity abroad. They tend to decrease their worldwide purchases, especially for capital equipment.
- Capital equipment sales have been lower than expected because of the reason cited above, and because of a lack of confidence in U.S. and world economies. At comparable points in past economic cycles, capital spending has been considerably stronger. Apart from the general lack of confidence in future expansion, many companies have postponed investments because of the lack of clear-cut investment payoff due to the regulatory and tax environments.
- The consumer electronics market has been weak all year. Although the TV and automotive markets performed satisfactorily, CB radios and watches have performed extremely poorly. The calculator market also has been sluggish. Overall, semiconductor shipments to the consumer area probably declined in 1977 when compared to 1976.
- For the first time during a period of economic expansion, the pervasiveness of semiconductors in the EDP industry has declined. Computer industry shipments grew faster than shipments of semiconductors to the EDP industry. The reasons for this are not entirely clear, and this trend is not expected to continue. Indeed, recent strong order rates from computer companies have buoyed semiconductor bookings since September.
- There has been a heavy conversion to LSI in 1977, at the expense of small-scale integrated circuits and discrete devices. LSI devices are tremendously lower in cost per function. This indicates that industry use of electronics has increased greatly, but dollar

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volumes may not have adjusted sufficiently.

Price is one factor that we feel has not affected semiconductor shipments in 1977. Prices, at least for integrated circuits, have been relatively stable—i.e., price declines have been the same as under normal conditions. Increased industry earnings confirm that price erosion has not been excessive, and that costs have declined commensurately.

The U.S. economy continues to remain sound, with growth at a measured pace. The economy certainly is not in a 'runaway' situation, nor does it appear to be entering a downturn. The erratic behavior of the economy during the third quarter of 1977 appears to be ended.

- Industrial production has grown steadily, if slowly, for the past few months.
- The GNP grew at about a 5.1 percent annual rate in the third quarter.
- The FRB Index of Leading Indicators has continued to increase rapidly since July, after being flat throughout the second quarter.
- Retail sales continue to be strong.
- The money supply continues to grow slowly in terms of real dollars.

These developments indicate a beneficial climate for the economy and the semiconductor industry in the first half of 1978. The slower growth of the worldwide economy increases the probability that we are breaking out of the recent trend of four-year economic cycles. Indeed, it has been more than four years since industrial production turned down in December 1973, and more than eight years since the downturn of economic growth during the 1960s. The economy remains self-regenerative. In 1978, we expect the economy to be stimulated by increased capital spending and renewed confidence in general.

The economies of Japan and Western Europe, both of which have been performing poorly, remain as major question marks. Industrial production in Western Europe is virtually the same as one year ago and is up no more than 2 percent in Japan. If the governments of Japan and West Germany do not take measures to stimulate their economies, a period of slower U.S. economic growth may occur. We believe these governments will take more stimulative actions.

Semiconductor industry bookings in October and November appear to have been strong, with book-to-bill ratios between 1.1 and 1.2. After a poor summer, bookings picked up at the end of September and have remained strong. Particular strength has come from the computer industry, which is reaping the benefits of price reductions earlier in 1977. The strong bookings have increased optimism for good semiconductor shipments during the fourth quarter of 1977 and the first quarter of 1978. This is in line with the continued improvement of the economy in general. However, the real strength in semiconductor bookings from increased industrial capital equipment expenditures may not occur until foreign economies improve. The worldwide economic situation is maintaining capital expenditures at a level below what might be expected at this point in the economic recovery. Inventories of end products, which had been increasing in the second quarter of 1977, have now been worked off and should not further affect semiconductor demand. Component inventory also remains at very low levels.

Our current forecast is shown in Tables 2.1 and 2.2. Semiconductor shipments are expected to continue improving on a quarterly basis throughout 1978. Total industry shipments (U.S. factory sales) are expected to increase in 1978 to about 15.4 percent over 1977. Our econometric model does not give clear indications of quarterly growth rates in 1978, although we expect somewhat greater growth in the fourth quarter of 1977 and the second quar-

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ter of 1978, and slower growth in the first and third quarters of 1978. Seasonal factors may accentuate this growth. It is entirely possible that 1978 may be similar to the previous two years, with stronger growth in the first half of the year and slower growth in the second half. In short, good but not great growth is expected.

The limited growth of semiconductor demand has fostered an environment in which the semiconductor industry is not exhibiting extremes:

- Prices remain relatively firm; i.e., they are not declining exceptionally fast, although some specific products have shown weakness due to excessive competition.
- Excess capacity in the semiconductor industry has remained fairly constant, with industry productivity increasing at a rate similar to shipment increases. However, this capacity shows increasing variance among different product lines, with shortages occurring in some MOS LSI products.
- Semiconductor inventories have remained at low levels.
- The industry is at nearly full employment.

As foreseen, heavy capital expenditures by the semiconductor industry this year have not resulted in excess industry capacity. Most expenditures were related to increased automation, cost control, or new technical capability (especially for VLSI), rather than to an increase of overall capacity. Furthermore, many new processes are increasingly wafer fabrication intensive. These wafers require more work to produce, and consequently use up a greater proportion of equipment and capacity. Relative to other industries, the semiconductor industry is still labor intensive, and the ratio of capital costs to labor costs is increasing very slowly.

Yields in the industry, particularly for LSI, have risen very rapidly over the last year. This has caused prices to decline somewhat rapidly for many products. The potential for short-term

Table 2.1

ESTIMATED U.S. FACTORY SALES OF SEMICONDUCTORS
(Dollars in Millions)

	1976	1977	Percent 76 - 77	1978	Percent 77 - 78
Discrete Devices	$1,076	$1,092	1.5%	$1,230	12.6%
Integrated Circuits	1,637	1,969	20.3%	2,302	16.9%
Total	$2,713	$3,061	12.8%	$3,532	15.4%

Source: DATAQUEST, Inc.
December 25, 1977

2 Markets

Table 2.2

ESTIMATED QUARTERLY U.S. FACTORY SEMICONDUCTOR SALES
(Dollars in Millions)

	1977				
	1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Total Year
Discrete Devices	$264	$274	$272	$282	$1,092
Integrated Circuits	460	491	497	521	1,969
Total	$724	$765	$769	$803	$3,061
Percent Change From Previous Quarter	2.7%	5.7%	0.5%	4.4%	-

	1978				
	1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Total Year
Decrete Devices	$289	$302	$311	$328	$1,230
Integrated Circuits	541	569	584	608	2,302
Total	$830	$871	$895	$936	$3,532
Percent Change From Previous Quarter	3.4%	4.9%	2.8%	4.6%	-

Source: DATAQUEST, Inc.
December 25, 1977

problems in industry growth before market elasticities take effect should be watched closely. The semiconductor industry is increasingly adept at managing its technical progress, but users of semiconductors often have system restraints that impede their ability to react quickly to that progress.

2 Markets

GENERAL INDUSTRY FORECAST

Our forecast remains relatively unchanged from the previous one (January 21, 1977); 1977 U.S. factory shipments are expected to be about 20 percent over those of 1976. We believe the largest quarter-to-quarter growth in the industry will occur in the second quarter, with slower growth during the last two quarters of the year.

The U.S. and world economies continued to remain strong during the last quarter. Strength is concentrated in the U.S. economy, with somewhat weaker economic recoveries abroad. Continued buildup of the U.S. economy was interrupted by the cold weather during January and February. Although production interruptions during the winter freeze had a definite effect on the economy, the consensus is that long-term effects were relatively negligible as a full recovery occurred in March. In March, industrial production jumped 1.4 percent over February. Several favorable economic developments have continued:

- Record months of industrial production in February and March
- Continued increasing high levels of consumer spending in March
- Decreasing unemployment
- Lessened over-stimulative economic measures by the government
- Continued increases in real GNP
- Increasing capital spending, particularly for electronic equipment

These factors indicate continued strengthening in both the U.S. economy and semiconductor demand throughout 1977. Nevertheless, a major concern at this time is the possibility of renewed inflation. However, increased housing sales, auto production, inventory accumulation, capital goods production, and consumer spending should give the economy a sufficient push throughout the year. Additional stimulus is expected to result from greater confidence in the economy as the year progresses. With these developments, the economy is currently self-regenerative and stimulative measures by the government would only be counterproductive.

Current levels of industrial production and the expected future increases are rapidly beginning to deplete excess industrial capacity. This is expected to stimulate capital spending, although spending has been much more cautious than in past economic upturns. However, there is less reluctance to spend for electronic equipment (which more directly benefits the semiconductor industry) than capital equipment in general. Due to the decreasing cost per function of semiconductor devices, equipment using semiconductors continues to become more cost-effective than other forms of capital equip-

Table 2.1

ESTIMATED U.S. FACTORY SALES OF SEMICONDUCTORS
(Dollars in Millions)

	1975	1976	Percent 75-76	1977	Percent 76-77
Discrete Devices	$ 901	$1,087	20.6%	$1,258	15.7%
Integrated Circuits	1,195	1,571	31.5%	1,934	23.1%
Total	$2,096	$2,658	26.8%	$3,192	20.1%

Source: DATAQUEST, Inc.

2 Markets

Table 2.2

ESTIMATED QUARTERLY U.S. FACTORY SEMICONDUCTOR SALES
(Dollars in Millions)

	1976				
	1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Total Year
Discrete Devices	$255	$272	$275	$285	$1,087
Integrated Circuits	356	396	403	416	1,571
Total	$611	$668	$678	$701	$2,658
Percent Change From Previous Quarter	11.1%	9.3%	1.5%	3.4%	—

	1977				
	1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Total Year
Discrete Devices	$295	$311	$325	$327	$1,258
Integrated Circuits	430	476	501	527	1,934
Total	$725	$787	$826	$854	$3,192
Percent Change From Previous Quarter	3.4%	8.6%	5.0%	3.4%	—

	1978				
	1st Qtr.	2nd Qtr.	3rd Qtr.	4th Qtr.	Total Year
Discrete Devices	$332				
Integrated Circuits	533				
Total	$865				
Percent Change From Previous Quarter	1.3%				

Source: DATAQUEST, Inc.

ment (where prices have generally inflated). Furthermore, there appears to be more inclination to utilize capital spending for increases in productivity and efficiency of existing plants rather than construction of new facilities.

We expect capital equipment markets to be a primary force in 1977 in increasing total semiconductor demand. The above considerations have been reflected in improved sales for related electronic equipment: production control, data processing (mainframes), office equipment, communications, and instruments. Recently, sales for these items have been showing increasing strength, and these market segments should join minicomputers in providing a major impetus during 1977 for increased semiconductor sales.

Semiconductor bookings and semiconductor shipments, which were essentially flat in the third and fourth quarters of 1976, have begun to increase and were especially strong in March. Bookings increased only slightly in January

2 Markets

and February, which we believe was partially due to weather conditions—both directly and indirectly. The freeze made buyers extremely cautious and reluctant to either add inventory or make long-term commitments. This attitude apparently reversed in March as every major company showed excellent booking increases. Most companies had record bookings during either the first quarter of 1977 or in March; however, because of low bookings in the fourth quarter, shipment increases in the first quarter were relatively modest. Nevertheless, these order improvements should result in a major increase in semiconductor shipments during the second quarter. Worldwide, the U.S. lead has not been closely followed. European demand has been increasing steadily, if slowly, but orders and production declined in Japan in the first quarter.

Our current forecast is shown in Tables 2.1 and 2.2. Semiconductor shipments are expected to continue quarter-to-quarter improvements throughout 1977. Total industry shipments (U.S. factory sales are expected to be about 20.1 percent above those of 1976. The current quarter is expected to show a major increase in semiconductor shipments over the first quarter; it should be over 8 percent, as shown in Table 2.2. This increase is expected to slow considerably during the third and fourth quarters of this year. The forecast for the first quarter of 1978 shows essentially no change from the previous quarter. However, this flatness may only reflect erratic statistics that resulted from the winter freeze rather than underlying economic trends and a possible cooling of the U.S. economy in the second half of 1977.

As bookings increase and the U.S. economy improves, confidence in the future should rapidly increase. Although the outlook is favorable, excessive optimism is also similarly unwarranted in the near future. The following major world economic problems still exist:

- Weak national economies
- Inflation
- Excessive deficit spending
- High unemployment

These problems will probably maintain worldwide economic improvements at a modest pace. The fear of inflation or possible shortages should act as a strong incentive to maintain problems that will prevent overheated world economies. During the next year, do not expect a "runaway" situation like the one that developed in 1973.

Semiconductor bookings can increase much faster than industry production. This can occur when users, with increased orders of their own, order both for increased production and inventory building. It is generally the case that buyers place longer-term orders at the same time, which further swells bookings. This can cause short-term effects on lead times for semiconductor devices that give the false appearance of developing shortages. A situation such as this occurred in TTL devices in 1976, and may currently develop in some markets. However, increases in semiconductor production should be sufficient to meet increases in end demand for electronic equipment. We do not foresee industry shortages in the next six months; but increased bookings are expected to increase backlogs and extend delivery times. Accordingly, this should keep price erosion at manageable levels and maintain or increase industry profit margins.

The increase in semiconductor production throughout this year should create increased demands for employees and equipment in the industry. Consequently, some strains should develop as the year progresses. Semiconductor companies in recent months have been reticent in both building capacity and in ordering equipment. Increased bookings may cause excess capacity to rapidly decrease; and this, in turn, could cause a rapid increase in equipment orders.

2.2 Econometric Model

INTRODUCTION

Dataquest believes that econometric modeling of the semiconductor industry gives valuable insight into the direction of future industry shipments, the size of those shipments, and the timing of shipment peaks and troughs. The semiconductor industry experiences wide variation in its rates of shipments, with annual industry shipment growth rates varying from minus 15 percent to plus 50 percent. Changes in the short-term outlook of the industry can be extremely rapid and of major consequence. Our model shows that the economy provided a clear indication of industry shipment downturns in 1967, 1970, and 1974, and industry upturns in 1968 and 1972. Econometric modeling also indicated the very high growth rate experienced by the semiconductor industry in 1973.

A well-prepared model also gives insight into the prime economic forces that determine industry sales. This information helps bring into focus the long-term changes occurring throughout the industry and provides a basic indication of long term growth.

Industry Sensitivity to Modeling

Two factors make modeling of the semiconductor industry particularly important:

- High sensitivity to the economy
- Low sensitivity to noneconomic factors

Semiconductor industry shipments are clearly governed more by the general economy than any other factor. The major markets for semiconductor devices are in industrial applications, which are primarily determined by the health of the economy.

Because the uses of semiconductors are directly related to industrial expansion, the demand for these devices is generally high when industry is expanding and low when the economy is in recession. Figure 2.2-1 shows U.S. semiconductor industry shipments and U.S. investment in producers' durable equipment (IPDE) over a period of years. Although the scales have been selected to show clearly the correlation between the variables, no modeling or other adjustments have been made. The figure graphically demonstrates the correlation of the semiconductor industry on the general economy.

Not only is the industry tied to the economy, but shipments are very sensitive to changes in economic activity. This sensitivity to the economy accounts for the wide variations that occur in the demand for semiconductors and means that a small change in the economy can have a very large change in semiconductor industry shipments. For this reason, econometric modeling of the industry is all the more important.

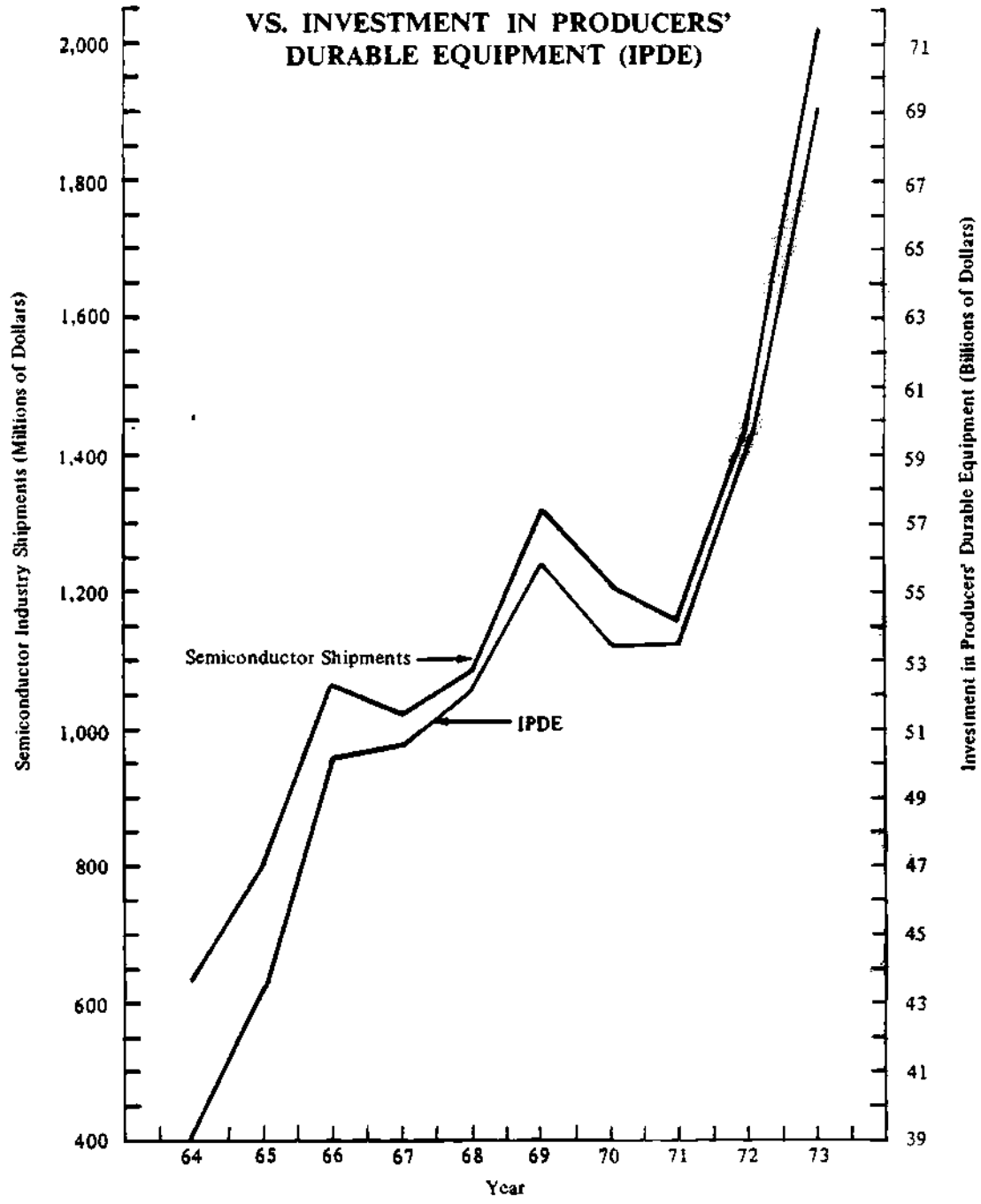
The model has been evolved over time and combines the benefits of Dataquest's staff's long experience within the semiconductor industry, a complete data base, and extensive experience in econometric modeling. Further, monitoring of day-to-day changes in the industry through a wide range of industry contacts provides a continued check on results from the model.

The model is uncomplicated. Its main focus is to provide forecasts of the future directions of the semiconductor industry, for the short and long term, and to do so in a manner that provides both flexibility and a short response time. A number of checks and balances have been built into the model, which help to avoid gross forecasting errors resulting from usual perturbations in the economy or individual indicators. These checks and balances also provide a statistical method for assessing the confidence in a forecast and allow realistic limits to be assigned to the forecast range.

2.2 Econometric Model

Figure 2.2-1

SEMICONDUCTOR SHIPMENTS VS. INVESTMENT IN PRODUCERS' DURABLE EQUIPMENT (IPDE)



[1] Simple scaling without modeling. U.S. Factory noncaptive semiconductor shipments

Source: DATAQUEST, Inc.

2.2 Econometric Model

MARKET SEGMENTS

For modeling purposes the semiconductor industry has three major user segments:

- Government sales for military and space applications
- Consumer uses
- Industrial applications including EDP

Government

Military and space uses of semiconductors are the most stable segment in the industry. This segment of the market peaked in the late 1960s and has only recently begun to grow again. Its overall growth rate has been far slower than that of the other segments.

The sale of semiconductor devices is determined primarily by the use of semiconductors in the defense hardware and aerospace vehicles being procured. However, semiconductor use is not a direct function of total spending for defense and aerospace or spending for electronics in this area. That is partially because the semiconductor content of military electronics is a very small percentage of the total system value and because semiconductor content varies widely with the type of equipment procured. Moreover, procurements tend to be somewhat erratic and are often strongly influenced by a few large dollar contracts which further complicates modeling. To correct for this lack of correlation military and space programs must be monitored closely to assess the extent of semiconductor sales in these areas.

Defense and NASA procurements for hardware are nevertheless reasonable indications of future semiconductor sales although correlation is not high. Government obligations for military and NASA procurement are well documented in advance and such documentation can assist the forecasting of short term changes in this segment. Of course, longer term government spending in these areas depends on political and other considerations. For modeling purposes, total industry demand must also be considered a factor because it affects prices in this segment and therefore dollar volume. Since variations in this market segment are less abrupt than in other segments, potential forecasing errors are smaller.

Consumer

In the past, the consumer market segment for semiconductors was extremely small. But in recent years this area has grown rapidly. Because of the infancy of this segment it is not, by itself, amenable to econometric modeling since a historical basis has not been established. To date, consumer uses are primarily for durable goods items, including automobiles, televisions, and calculators. Sales of these items tend to correlate rather closely with the sales of industrial durable goods because they can be delayed in poor economic times. For forecasting purposes, the consumer segment has been lumped with the industrial segment.

Unlike the military segment, which has its own pricing structure, the consumer segment is subject to the same price elasticities as the industrial segment. In other words, decreasing prices for semiconductors tend to open new markets in both segments. Thus, there is little difference, for example, between the replacement of distributor points in an automobile by semiconductor ignition devices and the substitution of semiconductors for electromechanical switches in industrial applications. Both are a function of the same price elasticity. At this stage of development, we have identified the consumer segment for tracking but not for separate forecasting in our model. As more data are accumulated on this segment, however, it may become more meaningful to forecast independently and at that time we will make the necessary revisions in our model. In the mean-

2.2 Econometric Model

while we will continue to include it with the industrial sector.

Industrial

The largest and most important segment of the semiconductor industry is the industrial market, which accounts for about 65 to 70 percent of the total market. Semiconductors are used widely in computers, office equipment, other data handling and communications equipment, process control, and instruments. Thus, semiconductors are used pervasively in industrial durable goods and these uses all share the common denominator that they are important to business when it needs to expand capacity or increase productivity. Most of the following discussion applies to the industrial segment.

RELATION TO THE ECONOMY

The semiconductor industry exhibits three important relations to the economy:

- Industry shipments depend almost totally on the demand for durable equipment.
- Shipments are highly sensitive to the economy.
- Semiconductor shipments lag the general economy.

Semiconductor sales are strongly affected by changes in spending for durable equipment, reflecting the fact that most uses for semiconductors are in some type of durable equipment.

The market for semiconductors is dominated by economic cycles. Demand is great when industry is expanding and low during a recession. Consequently, variations in shipments are greater than variations in the general economy. Further, the equipment using semiconductors can be produced more rapidly than can much durable equipment and, therefore, is more sensitive to short run changes in the economy than is durable equipment as a whole. The approximate sensitivity of the semiconductor industry to various economic indicators is shown in Table 2.2-1. This table shows that a small percentage change in one of the variables would generally signal a much larger percentage change in semiconductor industry shipments. For example, a 1 percent change in the Federal Reserve Board index of industrial production would usually be matched by a 4 percent change in semiconductor sales.

Semiconductor sales lag the economy because commitments to spending for industrial expansion generally occur when industry is expanding. Actual expenditures can occur somewhat after general economic expansion has been halted. On the other hand, following a recession, commitments do not begin until after the economy has started to improve and production approaches capacity. This cycle leads to the general observation that those factors that

Table 2.2-1

SENSITIVITY OF SEMICONDUCTOR DEMAND TO THE ECONOMY

Economic Variable	Relative Multiplier to Semiconductor Demand[1]
IPDE	2.7
GNP	7.5
Money Supply	5.0
FRB Index	4.0
12 Leading Indicators	2.9

[1] i.e., if the variable changed p%, and multiplier is y, then change in semiconductor demand would be (p x y)%.

Source: DATAQUEST, Inc.

2.2 Econometric Model

influence the demand for semiconductors lag the general economy both in upturns and downturns. Semiconductor shipments can lag general economic indicators anywhere from six months to one year, depending on those used. This relation has held true in all past changes in direction in semiconductor demand—i.e., all peaks and troughs.

Price also plays a very important role in the value of semiconductor shipments. Purchases of semiconductors made during a period of expansion generally carry higher prices. These prices carry-over into the initial period of a downturn because companies ship from backlogged orders. After demand has been weak for some time, price competition typically causes a radical drop in semiconductor prices. This price decline, in turn, will affect the total dollar value of the market in the early periods of an upturn in demand. Thus, semiconductor shipments in dollars may remain low even though unit demand has increased. As a result, pricing actions tend to reinforce the lag in the industry relative to the general economy and to amplify the sensitivity.

Because the semiconductor industry lags the economy as a whole, those economic variables that either lead or are coincident with the general economy can be considered in forecasting industry performance. The typical time lag between the various economic indicators and semiconductor industry shipments are shown in Table 2.2-2.

Although these lags have generally held true, it is not clear that they always will. Of particular importance, is the two-step recession in 1974-75. Industrial production showed a downturn in the last few months of 1973 and January of 1974. This situation was reflected by the semiconductor industry when demand turned down in the summer of 1974. However, these same variables showed a much greater downturn between October 1974 and February of 1975. There are indications that, in this case, the corresponding reaction in semiconductor demand might be more coincident. Further, the behavior of semiconductor demand in a long downturn or recession of the economy is unknown. During the brief history of the industry, upturns and downturns in the economy have not been long lived.

Table 2.2-2

TYPICAL LEADING INDICATORS OF SEMICONDUCTOR DEMAND

Economic Variable	Approximate Months the Variable Leads the Semiconductor Industry
IPDE	0
GNP	9
Money Supply	12
FRB Index	7
12 Leading Indicators	12

Source: DATAQUEST, Inc.

Economic Variables

Major economic variables that show strong correlation with the semiconductor industry include:

- Investment in producers' durable equipment (IPDE)
- Gross National Product
- Money supply
- Federal Reserve Board index of industrial production
- Index of 12 leading indicators

These are the major variables used by Dataquest. A wide range of other variables may be used, including total purchases of durable goods, orders for durable goods, changes in business inventories, and gross private domestic

2.2 Econometric Model

investment. In general, however, all economic variables are somewhat interrelated. A number of more specific economic indicators are also of importance as they apply to specific market segments of the industry. However, these variables suffer occasionally from inaccuracies in reporting, short term fluctuations, availability, and difficulties in forecasting. No variable is without its faults, and dependence on any single economic indicator can be dangerous. Investment in producers' durable equipment is by far the most important economic indicator in modeling semiconductor demand because the major markets for semiconductors are in those items that make up much of the durable equipment purchased by manufacturers. Correlations between this variable and semiconductor shipments are extremely high (see Figure 2.2-1). IPDE is directly coincident with changes in the semiconductor industry, i.e., both react to the economy at the same time.

An extremely simple model of the semiconductor industry would include only IPDE. However, to forecast semiconductor industry shipments with this variable, it is necessary to forecast IPDE. Forecasting attempts by econometricians have never been entirely successful. Moreover, a small error in forecasting IPDE is increased by a multiplier (refer to Table 2.2-1) when applied to semiconductor demand. Thus, a small error in IPDE results in a substantial error in forecasting semiconductor sales.

An alternative approach is to forecast with leading economic variables because actual data on these variables are already available. However, although correlations can be extremely high, another source of error is possible because the relation of these economic indicators to the semiconductor industry is more indirect. Dataquest believes that forecasting in this manner is most accurate for the near term. Historically, Gross National Product (GNP) has been an excellent leading indicator of semiconductor demand. But recently, that has not been true, probably because of the problem of measuring inflation. Another problem associated with GNP is the very high multiplier between GNP and semiconductor sales (refer again to Table 2.2-1), which increases the chance of error substantially.

Measures of industrial production, especially the FRB index, avoid the problem of inflation. However, this index in some ways may be less accurate than a measurement of GNP. It also can be questioned because of its high dependence on automobile production (which has only a minimal relation to the semiconductor industry). The FRB index does not measure services, which, of course, have no bearing on semiconductor sales. In this respect it may be less indicative of the health of the entire economy.

Both the Commerce Department index of 12 leading indicators and money supply are the leading indicators of the economy. As such, they also exhibit a high correlation with the semiconductor industry. The validity of this correlation may be questioned, however, because the relationship between these indicators and the semiconductor industry is more indirect than is the case with indicators such as IPDE. Further, these variables have problems both in measurement and in adjusting for inflation.

Other Variables

A number of other variables are important in semiconductor demand, including:

- Inventory accumulation
- Price fluctuations
- Introduction of major new product lines
- Major new markets
- Measures of consumer spending

By far the most important is the effect of changes in inventory. Generally, a high growth rate in semiconductor demand invariably leads

to shortages followed by overordering and hoarding. When the economy turns down, this situation leads to rather drastic readjustments. Inventory bulges have happened in 1966, 1969, and early 1974, and readjustments have come respectively in 1967, 1970, and late 1974 and are coming in 1975. The problem of inventory adjustments is difficult to model for two reasons: it is not directly related to general inventory accumulation in the economy and it is almost wholly psychological in nature. In the past, the amount of extra inventory accumulation above normal levels has been up to 10 percent of the total annual industrial sales for the year. A rough rule of thumb is that inventory accumulation adds 5 to 10 percent to total industry sales in the second year of two consecutive years of high growth. Readjustments occur throughout the 12 months following a downturn in demand. Dataquest monitors the inventory situation in the semiconductor industry very carefully through contacts with manufacturers, distributors, and users.

Rapid changes in prices can cause fluctuations in semiconductor sales. Because these price changes are directly related to demand, however, this effect is often overstated. In fact, price changes generally serve to emphasize shifts in semiconductor demand because prices rise in times of high demand and fall in times of low demand.

Broad new markets can also have an important effect. New markets are an inherent characteristic of the growth of the industry. However, a large market—such as that for minicomputers—can have a positive effect that is slightly greater than normal. In the next few years, semiconductor devices will most likely penetrate a wide range of new markets. Although these new markets should allow the long term growth of the industry to continue, they are not expected to cause the industry to grow at an abnormal rate.

THE DATAQUEST MODEL

Derivation of Coefficients

A flow chart of the derivation of model coefficients is shown in Figure 2.2-2. First, a wide range of historical, economic, and other data must be collected. Since semiconductor industry data is divided into two major segments—the industrial/consumer segment and the military and space segment, the data must be put into a form that is mathematically useful for statisitcal modeling. It must be adjusted for time series problems, colinearity, seasonal variations, inflation, and other factors that may arise. An intuitive judgment must then be made concerning which variables should be used.

Dataquest uses broad economic indicators (discussed above) for three reasons:

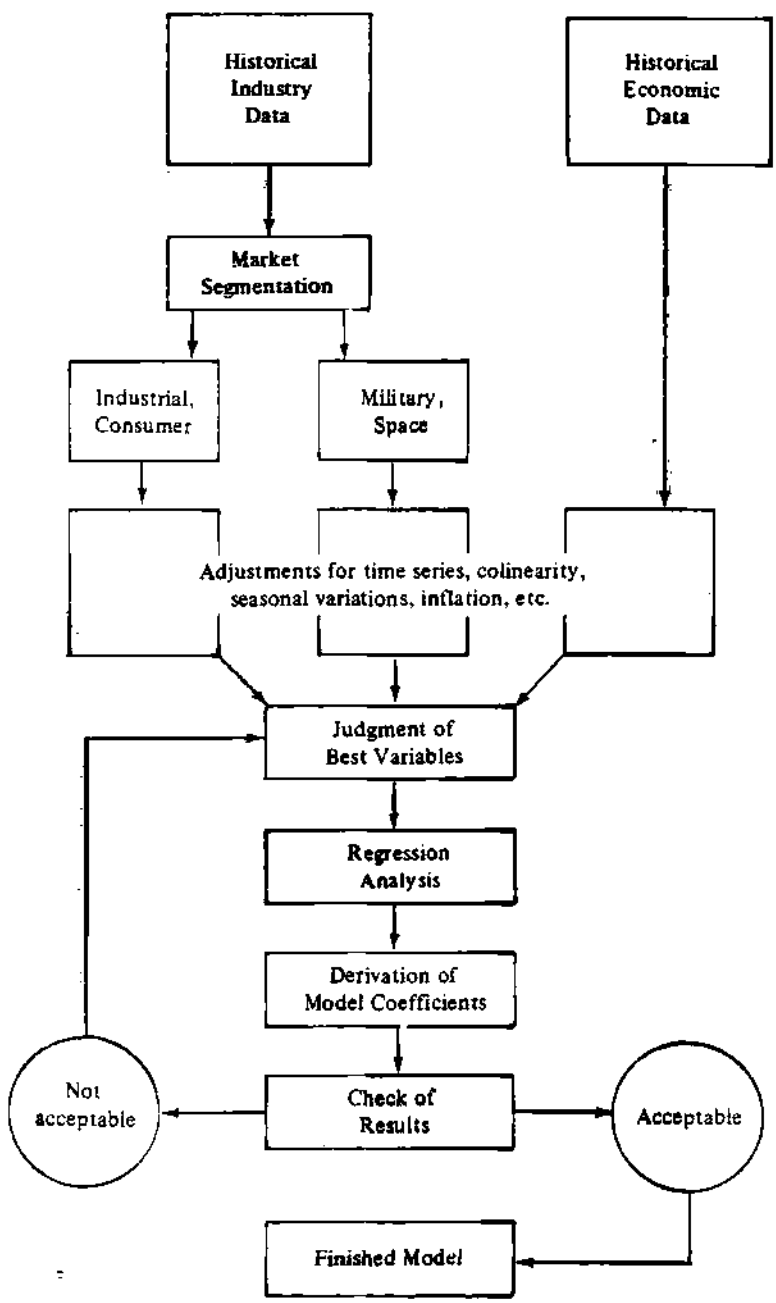
- The general economic health affects the industry more than any other factor.
- Specific indicators are less accurate.
- Specific indicators are subject to wider short-term fluctuations, which distort short-term forecasts.

Dataquest has found that the most accurate forecasts use variables that lead semiconductor shipments. By employing leading economic indicators, we can use actual current data rather than relying on forecast values for coincident indicators such as IPDE. However, because many macroeconomic models, such as the Chase Econometric Model or the DRI Model, forecast coincident variables, Dataquest also maintains a model of the semiconductor industry using coincident variables for our clients' use. The results obtained from either leading variables or coincident variables usually do not differ greatly.

Once the independent variables are determined, multiple linear regression analysis can

2.2 Econometric Model

Figure 2.2-2
DERIVATION OF MODEL COEFFICIENTS



Source: DATAQUEST, Inc.

2.2 Econometric Model

determine the coefficients for these variables. These coefficients are then applied to the proposed model equations, and values for historical shipments are derived. The results are then checked against actual past data. If the results are not satisfactory, then new or altered variables must be chosen. Ultimately, both the form and the coefficients for the equations in the model will be chosen.

Form of Model

The Dataquest model forecasts U.S. factory shipments of semiconductors, i.e., those devices tested, marked, and packed in the United States. Shipments of totally captive manufacturers—principally IBM and Western Electric—are not included. Intracompany shipments by manufacturers such as Texas Insturments are included.

In its simplest form, the model takes the format of a basic linear equation, as shown in Table 2.2-3. In this case, S is a derived or dependent variable that represents semiconductor shipments. The K values are coefficients and the X values represent the independent variables used in the model.

Actually, we use a number of equations. There are several reasons for the approach. First, one equation represents a single time period, i.e., a year or a quarter. For example, the next four quarters would be represented by four different equations.

Second, some of the economic variables used are so highly correlated that they cannot be employed together. We have found it useful in this case to use several different equations where each equation employs one of the variables. As a result, for any single time period, a number of different values of S are derived and an ultimate value is determined by a method of weighted averages. This approach has proven useful for giving both a confidence level and range of possible variation in forecasts. It also dampens errors resulting from short term perturbations in a single indicator.

Last, two forms of the equation may be used. Logarithmic values of the variables are employed to avoid nonlinearity problems. Dataquest has found this approach to be accurate, especially where there are wide ranges or values of time. However, the calculations and adjustment are time consuming. For rapid estimates, rates of change of the variables (i.e., percentages) are employed.

The steps in the process of determining a forecast value include:

- Identifying the variables to be used and obtaining correct data.
- Adjusting the variables to the format of the equation, including adjustments for time series, inflation, seasonal variations, and the proper mathematical transformation.
- Applying the adjusted variables to the model's equations, using the coefficients derived from historical data, and calculating the dependent variables.
- Readjusting the derived dependent variables to real values or percentage changes.
- Separating the results to obtain individual values for discrete and integrated circuit shipments. These values are historically a function of the rate of change of total shipments, as well as time. This can be checked, it necessary, by individual models for either discrete or integrated circuits.
- Determining quarterly values. These values are calculated by two methods. If logarithms are used, the final data are in an annual rate form. The data must be divided by four and seasonally adjusted for quarterly values. If percentages are used, it is inadvisable, because of the smaller changes, to figure percentage changes quarter to quarter. Therefore, annual changes between the quarters in consecutive years are calculated. Annual data in quarterly steps can

2.2 Econometric Model

Table 2.2-3

FORECASTING MODEL FORMAT

Basic Equation: $S = k_1x_1 + k_2x_2 + k_3x_3 \ldots + k_n$

where: S = dependent variable

$k_1, k_2 \ldots k_n$ = constant coefficients

$x_1, x_2 \ldots x_{n-1}$ = independent variables

Equation Matrix:

for time period 1: $S(a,t_1), S(b,t_1), \ldots$

time period 2: $S(a,t_2), S(b,t_2), \ldots$

.

.

.

time period n: $S(a,t_n), S(b,t_n) \ldots$

where: $t_1, t_2, t_3 \ldots t_n$ = different time periods

$a, b, c \ldots$ = use of multiple equations

Final Value of S(t): $S(t_1) = W_a S(a,t_1) + W_b S(b,t_1) \ldots$

(Same equation for other time periods.)

where: $W_a, W_b, \ldots$ are weighted values

Steps in Process:

1] Obtain data on independent variables
2] Adjust data to proper format
3] Apply data to equations
4] Readjust derived data to original form
5] Determine final value for S
6] Derive Quarterly values
7] Derive statistical variation $\Delta S = [(|S_a - S|)^2 + |S_b - S|^2 + \ldots.]^{1/2}$
8] Determine forecast values of market segments

Source: DATAQUEST, Inc.

then be easily calculated.

- Calculating the amount of statistical variation that might be expected in the forecast. This information is obtained from the range of the several different equations employed for one time period. This procedure has some pragmatic applications. First, if a major economic variable is distorted, it should become apparent. This seems true in 1974, for example, with GNP. In 1975, it is possible that variations resulting from the severe drop in automobile industry production may affect some values. Second, if a large number of these variables are very close together, it gives a high degree of certainty to the forecasted result. This was true in 1972. If the range is very wide, as it appears to be for forecasts in 1975, then those forecasts are less certain.

2.2 Econometric Model

Results

Results for the Dataquest model are shown in Table 2.2-4. In general, the results show good correlation with the actual values. The table shows two sets of results, one derived using coincident indicators and one using 12-month leading indicators, and compares them with estimates of actual shipments. The results using data derived a year before actual shipments, that is, with 12-month leading variables and other data available in December of the previous year, are nearly as accurate as the data from coincident variables.

Table 2.2-5 shows annual percentage changes in U.S. factory semiconductor shipments. This table clearly illustrates the high degree of variability in the industry from year to year. The values derived from the econometric models show the ability to obtain an effective indication of both the direction and magnitude of annual changes in the industry. The average error is about 2 percent of annual shipments. This degree of error is well within the accuracy of the historical data on U.S. factory shipments as well as the economic data used in the forecast.

1974 and 1975

The year 1974 was not used in the derivation of Dataquest's model for two reasons: First, complete data were not available at that time, and, second, the year could be used as a test case. For 1974, the model predicted a growth of 11.3 percent in U.S. factory semiconductor shipments. Uncertainty gives a range for this forecast from 9 to 15 percent. Real growth estimated by Dataquest subsequent to model development for 1974 was 13.7 percent (total shipments of $2.3 billion). Therefore, the error in the forecast was about 2.4 percent of total shipments, and the model gave a reasonable forecast for the year.

Negative growth is expected in the semiconductor industry for 1975, with a decline of shipments in excess of 10 percent. Because of the rapidly changing economy between October 1974 and February 1975 and rapidly changing rates of inflation, there is a high degree of uncertainty in our forecast values. All values derived by our model are highly negative, i.e., a 10 to 30 percent decrease in shipments. It is possible that overadjustment for inflation in 1974 may be causing one or more segments of the model to underestimate shipments. Further, a rapid V-shaped recovery in the economy could blunt the effect on the semiconductor industry of the very bad economic figures of January 1975 and shipments might be greater than a historically based model would forecast.

Long Term Industry Growth Rate

The long term growth of the semiconductor industry has resulted primarily from the elasticity of the market to decreasing semiconductor prices. Since the price per function is expected to continue to decline, long-term growth rates of the past should be maintained. Some different methods of calculating this long-term growth are shown in Table 2.2-6. If all U.S. factory semiconductor sales are included, the past growth rate over the last 10 years is considerably lower than if the government sector is excluded. The nearly zero growth rate of the government segment has masked the higher growth rate of the other segments. Since these other segments now constitute a larger percentage of industry sales than in the past, future growth for the industry should be higher even though all segments maintain the same growth rates.

Measurement of compound annual growth rates is questionable because of the high peaks and deep troughs in sales. It is difficult to pick representative base years. Similar problems exist if a simple least-squares trend line is used.

2.2 Econometric Model

Table 2.2-4

ESTIMATED SEMICONDUCTOR INDUSTRY SHIPMENTS

Year	U. S. Factory Shipments (Dollars in Millions)	Model with Coincident Variables Derived Value (Dollars in Millions)	Model with Coincident Variables Percent Error	Model with 12 Month Leading Variables Derived Value (Dollars in Millions)	Model with 12 Month Leading Variables Percent Error
1973	$2,040	$2,003	-1.8%	$2,035	-0.2%
1972	1,466	1,470	+0.3	1,430	-2.5
1971	1,156	1,148	-0.7	1,128	-2.9
1970	1,211	1,166	-3.9	1,227	+1.3
1969	1,327	1,339	+0.9	1,339	+0.9
1968	1,102	1,120	+1.6	1,149	+4.1
1967	1,023	1,054	+2.9	981	+4.3
1966	1,049	1,046	-0.3	1,034	-1.5
1965	805	800	-0.6	824	+2.5
1964	670	663	-1.1	666	-0.6
R^2		.996		.994	
Average Error			1.4%		2.1%

Source: DATAQUEST, Inc.

In the latter case, the very high growth in 1973 would be discounted.

A more accurate measurement results from using values derived with linear regression analysis. The values in Table 2.2-6 indicate that average future growth of the semiconductor industry might be fairly high, i.e., 14 to 18 percent. That assumes, of course, that past market and economy growth rates are maintained. Past average annual growth for IPDE, GNP, and the FRB index of industrial production are 6.5, 4.2, and 4.7 percent, respectively.

MODELING PROBLEMS

A number of problems are associated with econometric modeling and in modeling the semiconductor industry specifically. These problems do not alter the basic value in modeling the industry, but an understanding of them is necessary to place the modeling in perspective. These factors include:

- Data accuracy
- Inflation
- Colinearity
- Nonlinearity
- Price variations
- World market effects
- Long-term market changes
- Time series effects

2.2 Econometric Model

Table 2.2-5

SEMICONDUCTOR INDUSTRY SHIPMENTS PERCENT CHANGE–YEAR TO YEAR

Year	U. S. Factory Shipments	Derived – Model with Coincident Variables	Derived – Model with 12 Month Leading Variables
1973	39.2%	36.6%	38.8%
1972	26.8	27.2	23.7
1971	–4.5	–5.2	–6.9
1970	–8.7	–12.1	–7.5
1969	20.4	21.5	21.5
1968	7.7	9.5	12.3
1967	–2.5	0.5	–6.5
1966	30.3	29.9	28.4
1965	20.1	19.4	23.0
R^2	–	0.986	0.972

Source: DATAQUEST, Inc.

Table 2.2-6

LONG TERM INDUSTRY GROWTH RATE

Method of Calculation	Derived Annual Industry Growth (Percent)[1]
Total Industry	
Compound Growth	13.2%
Compound Growth (segmented and adjusted for 1973 market sizes)	14.6
Logarithmic Trend Line (least squares)	9.6
Linear Regression Analysis	14.5
Industrial-Consumer Segments	
Compound Growth	17.2%
Logarithmic Trend Line (least squares)	13.0
Linear Regression Analysis using:	
IPDE (1964–1973 growth, 6.5%)	17.4
GNP (1964–1973 growth, 4.2%)	19.2
FRB Index of Industrial Production (1964–1973 growth, 4.7%)	17.9

[1]Non-captive, U. S. Factory Shipments

Source: DATAQUEST, Inc.

2.2 Econometric Model

Data Accuracy

Usable data on the semiconductor industry are not always available. Although the Electronics Industry Association (EIA) collected data on the semiconductor industry through 1972, the data suffer somewhat from inaccuracies in reporting, changes in the basis of reporting over time, changes in the companies that reported over time, and an emphasis on production rather than sales. Nevertheless, gross U.S. factory shipments can be derived fairly accurately from the data. Although data are available on market segmentation and on segmentation by product, their accuracy is often questionable. Since 1972, the semiconductor industry has not reported to the EIA. For that period, Dataquest has derived its own market estimates, but the nonavailability of real industry data makes accuracy impossible to check. Thus, complete accuracy simply is not possible. Market estimates will do well to be expected to be accurate within a few percent.

The increasing in-house use of semiconductors, such as at Texas Instruments, National Semiconductor, or Rockwell for calculators, pose additional problems. Errors can be substantial.

Similar inaccuracies, although possibly less severe, exist for most of the economic variables. In general, as the market or variable becomes more specific or more detailed the accuracy becomes less sure. As a result, it is fallacious to attempt to become too detailed or too precise in modeling the industry.

A number of other variables that are important to the semiconductor industry can only be estimated grossly. These include: prices, inventory accumulation, capacity, and productivity changes. Nevertheless, some of them are important, and it is necessary to estimate them to monitor current and future changes in the industry.

Inflation

Generally, specialized econometric models derive their coefficients from historical data. Historical relationships may change if there is a major change in the underlying economy. Thus, any major disruption can have unforeseen consequences, either directly or indirectly. For example, major perturbations can be caused by the unforeseen consequences of such factors as war, the energy crisis, and inflation, which change past interrelationships.

In the past 18 months, there has been double digit inflation for the first time in the history of the semiconductor industry. The effect of this inflation on the industry is not well known. Inflation causes major types of problems in modeling the semiconductor industry:

- Inflation distorts all economic variables.
- Inflation affects the market for semiconductors.

In the past, the effects of inflation on economic data collected by the U.S. government were minimal. However, that is no longer the case and the accuracy of basic data, including GNP, can be questioned. For example, in 1974 current GNP increased greatly, but with the very large inflation adjustments real GNP decreased by about 3 percent. On the other hand, the Federal Reserve Board index of industrial production showed very little decrease through most of 1974. This 3 percent difference between the FRB index and GNP statistics is highly unusual, and has led many economists to question the possible overstatement of inflation adjustments to GNP.

Such problems are not minor when modeling the semiconductor industry. With the high degree of sensitivity of the industry to the economy, the differences become multiplied (see Table 2.2-1). As a result, potential inaccuracies in inflation adjustment can have major effects

in modeling and forecasting the industry. Thus, inflation gives some doubts as to the continued accuracy of econometric forecasting.

A second problem of inflation is that a high rate of inflation may have a major effect on the decision to buy or not buy semiconductors. On the demand side, inflation changes the basic balance between labor and capital and high wages may spur increased automation. That, in turn, has a very positive effect on the market for semiconductors, provided that corporations have the liquidity to make investments in capital equipment. On the supply side, however, the semiconductor industry has been characterized by decreasing prices. These price decreases have been one of the major factors in the growth rate of the industry, and higher wages will ultimately have an effect on prices. The net long term effect of inflation on the semiconductor industry will probably be beneficial but there are no historical data to substantiate this opinion.

Colinearity

Colinearity is a major problem in an econometric model. The problem arises because the industry is almost wholly sensitive to economic factors except for some military and aerospace sales. Since all economic variables are closely tied together, they exhibit a high degree of colinearity. One approach to this problem is to transform the variables into a form that will remove the colinerity. However, this approach is not particularly fruitful if the basic causal relationships in economic variables remain unchanged.

If two colinear factors are employed in a linear regression model, colinearity will manifest itself by a distortion in the coefficients derived for each of those factors. Effects can be extremely pronounced in models of the semiconductor industry and can lead to major problems. For example, in a period of rapid change in the economy when two previously colinear variables do not remain colinear, a model can be very much in error in spite of extremely high past accuracy. Dataquest has made major adjustments in the structure of its model to avoid the problems of colinearity.

Nonlinearity

The standard econometric model, using regression analysis, is built on the assumption that the relationships that exist among the various factors are linear. However, that may not necessarily be true for the semiconductor industry. The primary problem is the large swings in demands for semiconductor devices. The semiconductor industry cannot respond immediately in filling demand, and there are definite limits to the speed at which it can increase production. But demand can and has increased faster than these limits. As a result, there can be distortions in the market that do not occur under normal conditions. In particular, prices can remain higher than normal. This effect is pronounced if there are two or more good years in a row for the industry. In the second or third year, the rate of price decline will be lower and the market (in dollars) may be inflated.

Price Variations

Prices also pose a dilemma in modeling the semiconductor industry. The basic question hinges on whether or not the market is more truly described by unit volume or by dollar volume and on whether or not econometric models of the industry should be based on units or dollars. If the market is described in terms of units, then average prices must be calculated to convert back to dollars. If the market is modeled in terms of dollars, then average prices are not as important. However, such a model avoids the question of elasticity and the effect that prices may have on future market demand.

2.2 Econometric Model

A number of markets for semiconductors, particularly for many integrated circuits, may be best characterized by a demand for units regardless of price. In these markets, a particular function must be performed and the cost of the semiconductors has only a minor effect on the final system price. In essence, these markets can be considered to have very low price elasticity.

On the other hand, the generation of most new markets and new uses for semiconductors is directly attributable to changes in their prices. If the cost for semiconductor functions had not decreased, these markets would have never developed. Electronic calculators are a typical example. Due primarily to how cost large scale integration (LSI) devices prices have dropped from hundreds of dollars to tens of dollars in the last few years. Sales have risen from almost zero to nearly thirty million units forecasted for 1975.

The biggest problem with prices, of course, is that average prices are difficult to calculate. First, prices of each of the tens of thousands of different products are not well know. Second, price per unit is a somewhat meaningless figure for semiconductor devices, because of the changing number of functions per unit in integrated circuits and the continual improvement in device parameters. Thus, unit costs—even if they were known—would not provide a true measure of changes in prices. For example, in some markets for MOS devices, the price per unit has actually increased in some years, but the device complexity increased even faster, thus decreasing the cost per function. Nevertheless, in those years, the dollar value of the market continued a steady curve upward.

Generally, Dataquest feels it is more accurate to model the industry on a dollar volume basis. Since the industry is competitive, prices are highly elastic. Aside from the long-term trend of overall price decreases, prices will tend to be firmer in periods of high demand and much weaker in periods of low demand. Since prices tend to follow demand, a dollar volume model tends to differ from a unit demand model mainly by having larger coefficients. In other words, there are greater variations in the semiconductor market on a dollar basis than there are on a unit basis. These variations, nonetheless, are very highly correlated. However, if the industry is modeled on a dollar basis, prices must, nevertheless, be closely followed so that any abnormalities from normal pricing trends can be noted. For example, if prices did not follow their normal rate of decrease, it might signify a long term change in the industry. For this reason, Dataquest monitors prices both on a per unit and a per function basis. Trends in productivity among semiconductor manufacturers also are closely watched. Since is also possible to model the integrated circuit industry on a unit basis, a rapid check on modeling can be performed using a dollar basis.

World Market Effects

Some error is inherent in modeling U.S. factory shipments for an industry that is so international in scope. Although there is a high correlation between the movements of the different economies and foreign semiconductor markets, there can be important variations in the magnitude of economic ups and downs and in timing differences of economic cycles among nations. Changes in the European and Japanese markets for semiconductors may either lead or lag those in the U.S. market. These variations affect the overall demand of the U.S. semiconductor companies. For example, in 1970 the European market slowed down less rapidly than did the U.S. market. As a result, companies, such as Texas Instruments, which had a high percentage of European sales, were less affected in 1970 than those companies that had nearly all of their sales in the United States.

2.2 Econometric Model

Long Term Market Changes

If regression analysis is used to determine the coefficients in an econometric model, there is an implicit assumption that the historical basis of the market is unchanging. That is never entirely true, and it is definitely not true for the semiconductor industry. Over the past ten years, the semiconductor industry has had a major trend away from a reliance on the military and aerospace market. Consequently, it is necessary to separate this market segment from the remainder of the industry in performing an analysis. More recently, the industry has seen the emergence of a consumer market segment that includes such items as automobile electronics, television, and calculators. This market lacks historical data and, at any rate, is too immature for econometric analysis. However, because, as previously described, the present consumer market is for products that appear to behave similarly to industrial products, it is not yet necessary to separate the consumer market segment from the rest of the industry.

In time, other long-term changes should affect the industry as it matures. Most important will be a decreasing rate of technological innovation, which will slow the very rapid rise in the cost-effectiveness of using semiconductors. But these changes will not be rapid, and there should be no major effect on the industry over the next few years.

Dataquest continually reviews its model to evaluate the impact of such items as consumer markets and technological progress on the model.

Time Series Effects

An important statistical problem in modeling the semiconductor industry is the problem of time series. The semiconductor market has a long-term growth trend and will therefore show correlation with any other series that has a long-term growth trend. This situation causes two problems. First, there is the danger of a mathematical correlation that is not supported by a functional relation. Second, there may be true correlation with a series that grows at a different rate, a fact that will be obscured unless some adjustments are made. Therefore, it is necessary in all series used to elimate long-term trends prior to modeling.

DATAQUEST INCORPORATED

RESEARCH NEWSLETTER

SIS Code 2.2 Markets

March 21, 1975

MOS MARKET SHARE ESTIMATES

Recently, the fastest growing segment of the semiconductor industry has been MOS Integrated Circuits. Table 1 gives our estimates of market share in 1974. The values include internal use of MOS at current market prices by partially captive suppliers, such as Texas Instruments, but totally captive suppliers, such as IBM, are excluded. This table is a small portion of an extensive breakdown of market share by year, product category, and manufacturer currently being prepared for the Markets Chapter of Dataquest's Semiconductor Industry Service.

With about 50 market participants and rapidly changing technology, neither present nor future market share is easily estimated. Most of the MOS market leaders still have the majority of their sales in a single market segment or process technology. Most of Intel's sales are in memory devices, and it dominates that market. Texas Instruments, Rockwell, and Hitachi derive a majority of their sales from calculator chips. American Microsystems (AMI) is the largest custom device manufacturer and custom sales still account for a majority of its sales. RCA and Motorola derive most of their MOS sales from CMOS technology.

We believe the depressed market in 1975 is intensifying the competition in many markets, resulting in severe price competition in CMOS, memories, and calculators. This competition should cause difficulties for the independent chip manufacturers, with market share accruing to the vertically integrated calculator manufacturers. Hitachi has been badly hurt in the calculator market and Rockwell should experience slower growth due to calculator chip price erosion. RCA will likely be pressed to defend its CMOS market leadership against National and Motorola. Mostek has apparently had difficulties with NMOS production compounded by difficulties in the calculator market.

480 California Ave. / Palo Alto, California 94306 / (415) 327-8210

Product positioning is currently very important in the market. The only major manufacturer with wide product diversity is National Semiconductor. Dataquest feels its MOS revenues will experience faster growth in 1975 than those of many other market leaders. We feel that by 1976 the top four MOS manufacturers will be Intel, TI, AMI, and National.

James F. Riley
Fredrick L. Zieber
Denny K. Paul

Table 1

ESTIMATED 1974 COMPANY REVENUES
FROM MOS DEVICES

(Dollars in Millions)

COMPANY	MOS REVENUES[1]
Intel	$100
Texas Instruments	90[2]
Rockwell	75
American Microsystems	74
RCA	53
Hitachi	50
Mostek	48
National Semiconductor	40
General Instrument	35
Motorola	23
Fairchild	20
Electronic Arrays	17
Western Digital	12
Solid State Scientific	12
Signetics	10
Siliconix	6
Others	130
Total Worldwide Consumption	$795

[1]Includes all open market sales and internal sales of partially captive suppliers but excludes sales of totally captive suppliers.

Source: DATAQUEST, Inc. (March 21, 1975)

[2]Internal sales about $40 million

2.6.8 Games

SUMMARY

In the last few years, a new market for sophisticated semiconductor electronics—games—has been going through its formative stages. In the next five years, and especially in the next two years, this fascinating market should experience dynamic growth. In Table 2.6.8-1, we have outlined our estimate of the worldwide electronic games market for 1975, 1976, and 1980. Additionally, we have provided our estimates of semiconductor shipments into this market.

In two segments of this market—pinball machines and slot machines—current equipment is presently mechanical and electromechanical. In these segments, the opportunity for electronics is in replacing existing mechanical components because of lower cost, improved reliability, and lower maintenance. The primary objective in these markets will be to retain the feel of the mechanical pinball and slot machine; however, in some cases electronics may provide improved displays and user interaction. Almost all 1975 sales of pinball machines and slot machines were fully mechanical or electromechanical units. As our table shows, we are expecting little growth in the basic market; but we do foresee significant growth in their electronic content.

The other three market segments—home video games utilizing in-home television sets, coin-operated video games such as Pong for use in amusement centers, and other electronic games—are new markets which are developing because of the capability of semiconductor electronics. In these markets there are opportunities for semiconductor companies to provide not only semiconductor devices or electronic modules but the whole retail item, especially in home video games. This is an opportunity for semiconductor manufacturers—similar to the experience in calculators and watches—to provide added value, and consequently gain significant revenue. In this light, the games market represents an opportunity for semiconductor companies in excess of one-half billion dollars by 1980. The $100 million market opportunity in semiconductors would be supplemented by an opportunity of over $400 million in retail products sales.

Because of the extreme importance of marketing channels, high tooling cost, and low value added, we expect the pinball and slot

Table 2.6.8-1

ESTIMATED WORLDWIDE ELECTRONIC GAMES MARKET
(Dollars in Millions)

	1975	1976	1980
Pinball Machines	$127	$132	$ 160
Coin-Operated Video Games	59	90	190
Home Video Games	39	240	630
Slot Machines	50	53	65
Other	25	40	80
Total	$300	$555	$1,125
Semiconductor Content	$ 15	$ 44	$ 111

Source: DATAQUEST, Inc.

2.6.8 Games

machine market to continue to be strongly controlled by existing operators such as Bally Corporation, Williams Electronics, and Gottlieb, Inc. However, new companies such as Atari can find a market in the specialized segments that develop from technological innovation, e.g., the coin-operated video game.

Magnavox led the development of the home video game market, and Atari became a major factor in this market in 1975. We expect several semiconductor companies, including Fairchild, Motorola, National, and Texas Instruments to announce products in 1976. The television manufacturers are likely to develop the market by featuring new sets with games built-in, rather than the current add-on approach. Thus, the most interesting segments of games, home entertainment video-based devices, will have competitors from three industry segments-semiconductor manufacturers, television manufacturers, and independent producers.

1976 should be an important year for game manufacturers. Leading this growth will be home video games, where we expect retail sales to move from about $39 million to about $240 million. The market will move rapidly to penetrate the home entertainment field, prices will fall rapidly, and competition—always the banner word in the semiconductor industry—should be keen. We are forecasting semiconductor shipments for use in all electronic games to almost triple to the $44 million level.

INTRODUCTION AND BACKGROUND

This subsection discusses the opportunities and markets for electronic games. Presently, this business encompasses a wide variety of sophisticated electronic devices for entertaining one to four-players.

There are five major segments to the game market:

- Coin-operated pinball machines, which have formerly been electromechanical but are presently being converted to semiconductor based electronics.

- Coin-operated video games which are essentially a computer driven TV screen display.

- Home video games are units for the retail consumer which can be simply connected to a home television set. They work on either black and white or color television sets.

- Slot machines, which are presently mechanical or electromechanical, are viewed as another opportunity for semiconductor electronics to enter the game field.

- An additional segment which we presently define as "other". This segment includes a potpourri of games such as intellectual mind-tickler units, childrens games like the Novus Whiz Kid, or a reflex testing device. The products in this market are not well defined. As these products are developed, they may create several new market segments. Although this last category is the least developed, we might note that it may become the most interesting market in the long run.

History

The oldest market segment is the coin-operated pinball machine industry which began during the depression. Many of today's competitors in this industry have survived the last 40 years unchanged and are manufacturing essentially the same product developed in the 30s. Product tooling is in place (and fully depreciated), channels of distribution are established, and several of the businesses are family-owned companies with good control over the trade secrets of success. The opportunity is to

2.6.8 Games

introduce modern electronics into this existing business.

The video game was developed during the 1970s. There were two geographic centers of research for this product. Ralph Baer and William Rusch of Sanders Associates in Nashua, NH did pioneering circuit design work on radar displays for the government and for airline reservation terminals. Patents 3659284, 3659285, 3728480, and others resulted from this research. They described a television gaming and training apparatus composed of a control unit that could be added to a standard television receiver. During the same period of time in California Nolan Bushnell developed a technique (covered by Patent 3793483) for a game with a CRT display using digital circuit techniques.

Magnavox acquired an exclusive license for Sanders Associates' patents and developed a product called Odyssey which could be connected to a home TV set. The Odyssey game—the industry's first consumer home video game—was announced in 1972 and by the end of 1975 the original Odyssey had sold in the neighborhood of 340,000 units. One problem with Odyssey, the requirement for expert in-home installation, was inconvenient and costly.

At the same time, Mr. Bushnell licensed Nutting Associates, a manufacturer of coin-operated machines, to manufacture a game called Computer Space. Mr. Bushnell joined Nutting as Vice President of Engineering. However, he soon left this position and invented the video ping pong game—trademarked Pong—and formed a firm named Syzygy (later incorporated as Atari). Today Atari is the leader in coin-operated video games. Many of the coin video games in place today bear the manufacturing names of either Syzygy, Atari, or Kee Games, a subsidiary of Atari. From the original Computer Space, which had moderate success, to Atari's Pong, which had tremendous market acceptance, the coin-operated video game market grew to a level of roughly $59 million in 1975.

During the middle of 1975, Atari introduced to the marketplace (through Sears) a consumer video game called "Telegame"—a ping pong game featuring sound and automatic scoring on the TV screen. Telegame is a one chip MOS/LSI logic design and one analog chip to control signalling and facilitate connection to the TV set. In November 1975, Magnavox introduced the Odyssey 100, which was originally designed with four I^2L chips from Texas Instruments and played two games—tennis and hockey. In December of 1975, the Odyssey 200 was announced with tennis, hockey, and smash. Both Telegame and the new Odyssey can be connected to the TV by the user—an advantage over the original Odyssey.

Consumer video games were also offered by First Dimension and Executive Games. Thus, by Christmas 1975, the consumer had a variety of home games from which to choose.

FCC Regulations

Games must meet stringent FCC requirements because they operate in the TV frequency band. Recent FCC regulations have limited the number of competitors in the home video game market to the following four—companies that have obtained FCC approval: Atari, Executive Games, First Dimension, and Magnavox. Some potential competitors are currently either removing their games from the marketplace because of failure to meet the FCC regulations, or are in the throes of qualifying their devices with the FCC prior to their public announcement.

Legal Issues

A significant issue surrounding patents and litigation clouds the future of the coin-operated and home video game manufacturers. As part of the licensing arrangement on the Sanders

Associates' patents, Magnavox is obliged to pursue patent infringement actively. It has initiated suit against Atari. With the success of video consumer games in 1975 and anticipated revenues in 1976, Magnavox is beginning to accelerate legal action against other manufacturers. Atari, in turn, is countersuing Magnavox while also suggesting a settlement to be mutually negotiated which would involve both home video games and coin-operated video games. The outcome of these discussions will affect the other manufacturers that may attempt to participate in this marketplace.

POSITION OF SEMICONDUCTOR MANUFACTURERS

Semiconductor manufacturers may play several roles in the games market. They may provide semiconductor chips, supply complex electronic modules or subsystems, or sell end products, especially in the consumer markets.

A semiconductor manufacturer has a significant contribution to make in terms of the logic design, system understanding, and integration of the various LSI devices. To exploit the market fully, the industry feels the video consumer game must have additional variety and interest for the player. The future high-end or "Cadillac" version of the video game, which could be announced in 1976, will likely include features that will add a number of new games to the same installation. Techniques to achieve this require LSI understanding, circuit design experience, and system architectural capabilities. Semiconductor firms can meet each of these requirements. The bulk of the technology in this area involves computer techniques which are currently well understood by those semiconductor manufacturers participating in the memory, microprocessor, and interface component marketplace.

MARKETS AND COMPETITION

Pinball Market

The pinball industry has been reasonably stable for the last 40 years. It is estimated that in excess of 150,000 pinball machines were manufactured in 1975. The four major manufacturers of pinball machines are Bally, Chicago Coin, Gottlieb, and Williams Electronics. As shown in Table 2.6.8-2, these four manufacturers produce the bulk of the mechanical pinball machine installations.

Gottlieb, Inc., Williams Electronics, and Bally Corp. are all well established. However, Chicago Coin has been losing market share steadily over the last few years and was impacted significantly during the 1975 recession. It is believed that Chicago Coin will relinquish market share to new entries or to the existing competitors as the pinball machine converts to more reliable solid state circuity.

Present pinball machine technology utilizes cabling, mechanical relays, and other electromechanical devices extensively. These devices cause units to be unreliable in the field and require constant maintenance. Downtime on the machine is costly in terms of revenue generation for the operator. In addition, the field maintenance costs have increased substantially with inflation; as a result, repair of the machine in the field becomes extremely costly to the manufacturer or owner.

Solid state electronics can replace 700 cables, over 30 electronic mechanical relays, 7 to 9 rotary score wheels, and 7 to 9 driving motors. The circuitry will probably be microprocessor or even common TTL/MSI logic. Rotary score wheel displays will likely be replaced initially by gas discharge displays and eventually by LED devices. The semiconductor content for a new solid state pinball machine is estimated to be about $35 per machine.

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Table 2.6.8-2
ESTIMATED 1975 PINBALL MACHINE PRODUCTION

Manufacturer	Gottlieb	Williams	Bally	Chicago Coin
Average Daily Production (Units)	175	165	100	70
Average Selling Prices (Dollars)	$700	$653	$687	N/A
Single Player	$800	$703	$750	N/A
Two Player	$900	$850[1]	$865	N/A

[1] A recent increase from $793

Source: DATAQUEST, Inc.

Table 2.6.8-3 summarizes our forecast of the pinball machine market. Currently, the pinball machine market is basically static except for growth that either comes from general population growth, affluence, and/or inflation.

The growth of electronic pinball machines will come from two areas. First, an increasing incursion into the existing market so that by 1980—perhaps sooner—all pinball machines will be semiconductor based. This could result in semiconductor sales of $6.3 million by 1980. Second, another growth opportunity exists by placement of these machines into new locations where they are pulled in by coin-operated video games. The electronic machines will look like their mechanical predecessors. Although retaining the mechanical "feel" seems to be important, underneath the cabinet will be solid state circuitry rather than electromechanical components.

The average selling prices of pinball machines depends upon the mix of products sold;

Table 2.6.8-3
ESTIMATED WORLDWIDE PINBALL MACHINE MARKET

	1975	1976	1980
Units (Thousands)	150	155	180
Retail Revenue (Millions)	$127	$132	$160
Electronic Units (Thousands)	9	31	180
Semiconductor Content (Millions)	$ 0.3	$ 1.1	$ 6.3

Source: DATAQUEST, Inc.

that is, the mix among four-player units, two-player units, and single-player units. Product mix in the classic pinball market has been 55 percent four-player, 25 to 30 percent two-player, and the balance in single-player pinball machines. Single-player pinball machines are not generally profitable. This unprofitability, coupled with the low reliability of the electromechanical system, indicates that the solid state pinball machines will make rapid entry into the single-player segment on the basis of reliability and into the four-player segment because of profitability.

Mirco, Meadows Games, and Atari, have announced solid state pinball machines. Bally Corporation is testing a pinball machine using solid state devices (the 8080 microprocessor) and has been working extensively with Intel in this area, as well as on slot machine applications. Bally will probably pioneer the introduction of the solid state pinball machine, with Gottlieb and Williams maintaining a wait and see attitude. A few new entries may gain some market share. It is conceivable that, in addition to Mirco, Allied Leisure, Atari, and Meadows Games, others will compete by virtue of a distribution system established by their video game installations. Significant revenues from the sale of pinball machines is anticipated for these new entries. Meadows Games had an electronic video pinball game which was announced and then taken off the market because of lack of customer acceptance. The new players in 1980, therefore, could be Bally Corp., Williams and/or Gottlieb, and Atari, Mirco, Allied Leisure, or Meadows Games.

It is not anticipated that any of the semiconductor companies which supply chips to these participants will move into the end market itself. The nature of established channels of distribution, coupled with the relatively low percent of semiconductor content to end system price precludes semiconductor industry marketing or manufacturing leverage.

The pinball machine manufacturers feel that the costs for tooling of the various units will prohibit entry to the market of a semiconductor manufacturer or other game manufacturer. It is thought that tooling costs are in the neighborhood of $700,000. This could be financed by Atari, but not by other smaller companies which are in the video coin-operated market.

Coin-Operated Video Game Market

Early coin-operated video games (1972-74 vintage) were made possible by their large computing power—comparable to a medium sized computer—and the low cost of the integrated circuits.

Table 2.6.8-4 gives our forecast of the coin-operated video game market. The 1976 market should exceed $90 million.

Major competitors in the coin-operated video game market are Atari, Midway Manufacturing, Allied Leisure, Meadows, Games, Micro, Ramtak, and Fun Games. We estimate almost half of the market is controlled by Atari with $24 million in sales in 1975. Many of the competitors in the industry are located in Sunnyvale, Calif., Santa Clara, Calif., or in the immediate vicinity and to a great extent copy products that are innovated by Atari or another company.

Midway Manufacturing is a subsidiary of Bally Corporation and is estimated to have shipped $12 million in 1975 (many of these games were originally developed for Midway by Atari). Allied Leisure had 1975 sales of about $8 million. We estimate that in 1975 Meadows Games shipped $4 million, Ramtek $2 million, Fun Games $1 million, Exidy $250,000, and JRW Electronics $200,000. In addition, Innovative Coin Corporation, Project Support Engineering, Inc., Electronics Design and Assembly, Inc., and others announced new products in 1975 for shipment in 1976.

2.6.8 Games

Table 2.6.8-4
ESTIMATED WORLDWIDE COIN OPERATED VIDEO GAME MARKET

	1975	1976	1980
Units (Thousands)	39	60	127
Retail Revenue (Millions)	$ 59	$ 90	$ 190
Semiconductor Content (Millions)	$7.7	$12.6	$28.5 250 400

Source: DATAQUEST, Inc.

Mirco's sales are presently estimated to be somewhere in the $2-3 million range. Mirco's new video game—PT109—uses a Fairchild F8 microprocessor. This may have led to the recent announcement that Mirco and Fairchild would jointly develop semiconductor circuits for home games. It is interesting to note that Mirco is run by Tom Connors—the ex-Semiconductor Division General Manager of Motorola.

Market Characteristics

The average price of a coin-operated game has increased with the complexity of the game. It is our estimate that the current average selling price of the games shipped in 1975 is approximately $1,500. The low-end games are selling close to $750 while the high-end games, as characterized by the Atari eight-player Indy 800 color video game, sells in the neighborhood of $8,000.

The life cycle of a coin-operated game is numbered in months rather than years. The average life of video games in the field is relatively short—six to nine months. They then either become unprofitable because of lack of player interest and are dismantled, or they move down in the distribution channel to a different level of installations. Although this is a very short life, the original owner generally will receive his investment back in the first three to six weeks of installation, making even such a short life economically attractive.

The requirements for constant research on the behavior patterns of the consumer and also the demands on rapid buildup of machines creates enormous cash flow needs and tremendous pressures on the manufacturing operation. Many of the games that have been announced have not been well received and were subsequently abandonded. On the other hand, Atari's Tank, which was scheduled to run only 2,000 machines, should exceed 20,000 installations.

One of the significant factors in the growth of the coin-operated video game is the deviation from the traditional arcade. In fact, in 1971-72, the product originally appeared at airports, shopping centers, pizza parlors, and singles bars, where people spend leisure time.

However, as the games caught on, the stigma of the traditional arcade has been removed. The bulk of the coin-operated game installations is occurring in different environ-

ments than those formerly associated with the arcade. Complete mobile arcades built into large trucks are being brought to state fairs. Covered shopping centers are now including large game rooms to produce revenue and also to occupy children, which allows mother to spend her time shopping more effectively. With the advent of more dating and couples bars for the young population, the video game has been widely accepted in the more sophisticated taverns, social clubs, and ski resorts. This dramatic development has also accelerated the use of pinball machines in outlets that were pioneered by video coin-operated games. We are likely to find the installation of coin-operated video games in cafeterias of major manufacturing plants, in schools, other recreational facilities, and even in homes of the wealthy. There is no stigma associated with the games as there has been with pinball machines.

There are three levels to the industry structure—manufacturer, distributor, and operator. The distributor buys machines from the manufacturer and sells them to the operator. The operator places the machines at various locations and splits the revenue with the owner of the location. Also, the distributor provides necessary repair service.

If a machine stays in a particular location too long, regular players invariably become bored with it and receipts start to fall off. When this happens, the operator moves the machine to another location. After a particular model has made the rounds of all his locations, the operator either returns it to the distributor for a trade-in allowance on a new game, or sells it to the location owner. To the operator, the four most important qualities of an amusement game are: machine revenues, how quickly the revenues fall off, resale value, and minimum down-time. These four combined with initial cost determine his rate of return.

If revenues are low, the operator can make more money by investing in a different machine. If the revenues are good initially but fall off quickly, he must spend an inordinate amount of time moving machines around. If a machine has a reputation as a poor or short-time earner, its resale value falls. Finally, when a game is inoperative, both operator and location owner lose.

Semiconductor content in a video game is estimated at 12-15 percent. Many of the video games that have currently been designed use microprocessor techniques, although the TTL approach continues to be cost effective. (Early units used roughly 125 TTL/MSI integrated circuits.) Because the lifetime of a game is short, the low cost and ease of implementation of a TTL/MSI approach can be used to develop a test model rapidly and build into a large volume manufacturing without the concern of using state-of-the-art and limited availability LSI devices. Recent video games have utilized dramatic quantities of read only memory for micro instructions and random access memories, and are beginning to use microprocessors. We anticipate that this trend will continue. We do not see new coin-operated video games requiring the custom MOS/LSI techniques being used in the consumer video game because of lower volume.

Home Video Game Market

Magnavox was the first company to produce a game for this market; it introduced Odyssey in 1972. We estimate that in that year, 21,000 Odyssey's were sold; in 1973, about 125,000-150,000 units; and in 1974, 125,000 units. At that point, the product became obsolete and was subsequently removed from the marketplace in 1975. Total estimated shipments in calendar 1975 were 70,000 units; thus, the original Odyssey sold about 340,000 units in four years at an average price of $100 to represent a total market of $34 million.

It is estimated that about $8 million was

2.6.8 Games

spent to promote the game from 1972 on. Therefore, $8 million was spent in advertising to obtain the $34 million revenue—not exactly an advertising success. This is thought today to be the result of two factors—the lack of sound and automatic scoring on the original Odyssey and its difficulty of installation. A third factor might be that the game itself became uninteresting after it had been played repeatedly.

Subsequent products have sold much better even though the price is still $100. Newer games can be installed by the user, feature more than one game per unit, and score automatically, thus overcoming the limitations of Odyssey. It is thought that these newer games can penetrate a much larger marketplace, particularly as price reductions occur that will open the low end of the market.

Table 2.6.8-5 shows our estimate of the market for consumer video games. We estimate 385,000 units were shipped in 1975. The new Odyssey game—that is, the 100 and the 200—had limited volume due to poor performance by Texas Instruments on shipping the I^2L circuits. Our estimate is that 30,000 units were shipped in calendar 1975. Atari's shipments, which began in August 1975 and slowed for a period of time because of a technical problem, accelerated rapidly in November and December, and we estimate the calendar 1975 shipments of Atari's Telegame at 260,000 units. It is thought that Executive Games and First Dimension, the other two suppliers, had limited volume; total sales of the two companies combined are probably less than 25,000 games.

In 1976, we expect strong growth in shipments of video consumer games. One key factor in this growth should be substantially reduced prices. It is estimated that at the retail price of $100, the video consumer market is limited to roughly 1 million games in 1976. It is the intent of Atari, and we believe Magnavox, to significantly reduce the retail selling prices—to the neighborhood of $50. It is believed that at this level about four times as many units can be sold, thus almost doubling the market in dollars.

Novus, National's Consumer division, is expected to announce a video consumer game in 1976 priced under the $50 level. We estimate that its introductory price should be in the area of $35-39. At this level the market potential is thought to exceed 6 million units in 1976.

Table 2.6.8-5

ESTIMATED WORLDWIDE HOME VIDEO GAME MARKET

	1975	1976	1980
Units (Thousands)	385	300	21,000
Retail Revenue (Millions)	$ 39	$ 240	$ 630
Manufacturers Revenue (Millions)	$ 27	$ 168	$ 441
Semiconductor Content (Millions)	$4.7	$28.0	$71.0

Source: DATAQUEST, Inc.

2.6.8 Games

Another key factor in success will probably be the variety of games available on one unit. A magnetic tape or cassette may be used to obtain this variety. However, the limit on the quantity of games that can be included in one unit is probably the man/machine interface. Different games require different human inputs such as push buttons, levers, or dials; thus, the ability to provide variety at low prices may be determined by the human engineering on future systems.

Market Analysis

The home video game market is the only segment of the electronic game industry that lends itself to the use of demographic data for analysis. The worldwide television market is basically mature and has been well documented. Using this information, we can estimate the potential for home video game installations with a reasonable degree of confidence.

Table 2.6.8-6 summarizes our market analysis. It is estimated that there were over 200 million television sets installed worldwide at the end of 1975, excluding Communist Bloc countries. There are a large number of two-set homes, especially in the United States, and it is our belief that second sets should be eliminated to obtain an estimate of homes with at least one TV set. We feel that in the next five years the likelihood of multiple games installed in a single home will be small. After correcting for two-set homes, we arrived at an estimate of over 150 million homes with at least one television set. Of these, 71 million were located in the United States. We might note that this represents almost 100 percent penetration in the U.S. market. Because of this, growth in TV households in the United States will be limited to household formations. We believe, however, on a worldwide basis that recent increases of approximately 15 million sets per year can continue for the next five years. This yields estimated installations in 1980 of 235 million with 76 million located in the United States.

We believe that by 1980, close to 20 percent of the worldwide sets, including about a third of the U.S. sets, will have games installed; this would represent 45 million games. Our estimate of 21 million games shipped in 1980 implies cumulative shipments since game introduction in 1972 of 55 to 60 million units. We believe 10 to 12 million of these units will be obsoleted, especially the first Odyssey units and the early units of other manufacturers which are presently being produced. Thus, we arrive at an estimated sales value of 21 million units, or $630 million, in 1980 as shown in Table 2.6.8-6.

Home Video Game Manufacturers

In the longer term we expect to see three groups of competitors in the home video market.

- The semiconductor companies are entering rapidly. They will sell complete machines as well as selling electronic modules and semiconductor devices to other manufacturers.

- The television manufacturers should become more aggressive soon, introducing television sets with built-in game features. By eliminating some duplicate electronics, their costs should be lower than the combined price of a TV plus a game.

- The independents, with the possible exception of Atari, will probably feel the competitive pressure from the other two groups and many will likely drop from the market.

As we previously outlined, Magnavox initiated the home video game market in 1972 with Odyssey and introduced the Odyssey 100 and 200 in 1975. All of the Odyssey games have re-

2.6.8 Games

Table 2.6.8-6
MARKET ANALYSIS OF HOME VIDEO GAMES
(Units in Millions)

	1970	1975	1976	1980
Worldwide Television Sets Installed	135	210	228	300
Worldwide Households with at least 1 Television Set	90	157	172	235
U.S. Households with at least 1 Television Set	63	71	72	76
Percent of Worldwide Households with a Video Game	0	<1	3	20
Percent of U.S. Households with a Video Game	0	<1	4	33
Installed Games Worldwide	0	0.6	4.5	45
Installed Games U.S.	0	0.5	3	25
Annual Game Sales Worldwide	0	0.385	4	21

Source: DATAQUEST, Inc.

tailed at about $100.

Atari began with coin-operated games and introduced a game called Telegame to the home market in 1975. The Atari game retails through Sears at $99, and the FOB factory price is $70.85. We believe the Sears purchase order is for a volume of 1 million units starting in June of 1975 and ending in June 1976. The agreement provides that $5.00 per unit shall be discounted from the $70.85 price as an advertising allowance to be spent by Sears to promote Telegames. This amounts to roughly $5 million in advertising and is in line with the promotional costs associated with the original Odyssey campaign. In 1976, we expect Atari to announce a new top-of-the-line game. Its approach will probably use a magnetic tape or cassette for multiple game use. We believe the price will be in the area of $129.95 FOB factory and $149.95 retail.

Two other competitors who have obtained FCC approval are Executive Games, a small organization consisting of some design people from MIT, and First Dimension. Executive Games' Television Tennis uses 23 integrated circuits—TTL and low power Schottky—and is not considered reliable enough to compete long-term because of the high device count. It also appears to be under threat of cost competitiveness by the Atari one chip MOS/LSI unit and the Odyssey four chip I^2L unit. The current price FOB factory is $47, and it retails for $69.

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There was no significant volume production in 1975.

First Dimension Corporation's game, First Dimension TV, uses 51 chips—primarily TTL and CMOS. The price FOB factory is $99.95 and its retail price is $119.95. It has three games—tennis, hockey, and a play-the-robot game. Other competitors—National Computer Systems, Cromemco and Universal Research Laboratories—are awaiting FCC approval and finalization of arrangements with marketing and distribution systems.

The first semiconductor manufacturer to enter the field will probably be National's Novus Division. The Novus TV video game is thought to use a cassette technique which would require advanced LSI buffer memories to facilitate changing the number of games for each of the installations.

It is our belief that National has also approached Magnavox to act as a supplier of a one chip PMOS device to replace the four TI I^2L chips in Odyssey 100 and 200. In turn, National wishes to have Magnavox indemnify it against the results of any patent litigation.

In addition, Fairchild, Motorola, and TI are expected to announce home video games in the next 12 months. Other semiconductor manufacturers are also moving to gain sales of semiconductor chips to the rapidly growing consumer video game market. General Instrument has announced a 24 pin MOS TV game chip as an add-on for TV sets. Six games—tennis, squash, football, soccer, pelota, and rifle shooting—are provided. The device also includes automatic scoring (displayed on TV screen), and realistic sounds. General Instrument already produces modules and subsystems for many offshore TV set manufacturers. Other semiconductor manufacturers—Electronic Arrays, Motorola, Synertec, and AMI—are currently supplying TV game chips to existing system manufacturers.

Slot Machines

Sales of slot machines in 1975 are estimated at $50 million. The present market is dominated by Bally Corporation's slot machine division located in Sparks, Nevada. Slot machines represent a substantial opportunity for solid state electronics since there are significant reliability problems with the electromechanical portions of existing slot machines. These parts would be replaced by electronics. Semiconductor content on some prototypes is estimated at $25. Completely electronic slot machines have been made, but have not received strong market acceptance. Reasons such as the lack of "feel" and machine interaction are presently believed to contribute to this poor acceptance.

There are two major factors prohibiting entry of new competitors—Bally's. Bally's strong position (estimated at 85 percent of the worldwide market), combined with a market that demands custom made items tailored to each individual location. Bally has a strong rapport with the major buyers and meets their individual needs. The slot machine market is approached by financing both the slot machines themselves and the leasehold improvements of the gaming parlor as part of the sale.

Bally's strong position in the video game business and the pinball business allows it access to the semiconductor technology as well as a generally strong distribution system in the gaming market. It is believed that Bally is working with Intel on microprocessor-based slot machines and pinball machines, but that electrical noise problems have prohibited introduction.

Gamex Industires, a subsidiary of Centronics is also known to be working on a solid state slot machine; some of its financing has come from Caesars Palace. Also, the initial development of the Centronics mechanical printer drive was intended for slot machines and some of its work is still applicable in this market.

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We are not aware of any activity on the part of the coin-operated machine manufacturers—video or mechanical—in this market.

Table 2.6.8-7 summarizes our estimate of the market for slot machine games. We believe semiconductor sales to this application could reach $400,000 by 1980. This market appears to be open to significant sales of semiconductors to Bally, but successful new entries are unlikely.

Others

This is the category of the future. New products will probably be aimed at both other types of coin-operated games and the lower-priced end of the consumer market.

Atari is one manufacturer that is introducing games outside of the video CRT category. Last year it introduced a game called "Touch Me" using integrated circuits with various displays on a panel. This is a computer game that challenges hand-eye coordination as well as how quickly the mind can repeat the thinking patterns presented. Additional devices will probably be announced in 1976; these will probably include IQ testers and mind scramblers. Displays may also be used to generate astrological output for coin-operated astrological games.

There are already a number of companies that manufacture low-priced consumer games: Ideal, Marx, Mattel, and Creative Play Things. These companies are likely to become significant competitors in this segment because of their knowledge of the marketing channels, merchandising techniques, and the customer buying profile. We understand that Creative Play Things, a subsidiary of CBS, will announce five new electronic games this summer. These games are reported to be microprocessor based and use extensive MOS/LSI technology. However, we must not overlook the lesson learned in calculators and watches: if the traditional competitors cannot move rapidly to develop industries made possible by semiconductor electronic technology, others will.

At present, the Novus Whiz Kid, an MOS/LSI based teaching game, is the only product offered by a semiconductor manufacturer. It is the calculator and watch manufacturing operations of semiconductor and other companies that may represent the significant new suppliers to the low-priced consumer game segment.

Table 2.6.8-7

ESTIMATED WORLDWIDE SLOT MACHINE MARKET

	1975	1976	1980
Total Units (Thousands)	10	11	13
Retail Revenue (Millions)	$50	$53	$ 65
Electronic Units (Thousands)	0	0	12
Semiconductor Revenues (Millions)	$ 0	$ 0	$0.4

Source: DATAQUEST, Inc.

These companies are accustomed to relatively low-priced, high-volume production and already have facilities and personnel in place. Most of these companies also have distribution networks in retail stores through which the new game products can be sold.

The significant investments in production and marketing are likely to inhibit new innovator companies from entering this segment. It is our estimate that a commitment in advertising funds of $3.0 to $5.0 million is necessary to obtain large retail chain buyer commitments for a new product; yet these products are considered tremendous successes if they sell one million units. Obviously, in the $10 to $20 price range the portion of sales devoted to marketing, and the dollar investment required to tool for that length of run, are tremendous. We believe innovators of new games in the low-priced category are likely to license their ideas to traditional game manufacturers or possibly to the calculator companies for market development.

The concept of educational games along with hand or lap held electronic games is only now being explored. It is highly probable that a success like Monopoly could be developed in an electronic game. This potential is likely to generate intense competition in the future.

COMPANIES

Throughout this report we have mentioned a number of companies that are present or likely future participants in the electronic game business. In this subsection we have provided the names and addresses of the non-semiconductor companies, and the game category in which they participate or in which we anticipate their participation.

Company	Game Category
Allied Leisure Industries Inc. 245 W. 74th Pl. Hialeah, FL 33014 (305) 558-5200	Coin-Operated Video Slot Machines
Atari, Inc. Executive Offices 14600 Winchester Blvd. Los Gatos, CA 95030 (408) 374-2440	Pinball Coin-Operated Video Home Video
Bally Distributing Co. Subsid. of Bally Man. Corp. 390 E. 6th Street Reno, NV 89502 (702) 333-6157	Slot Machines
Bally Manufacturing Corp. 2640 W. Belmont Ave. Chicago, IL 60618 (312) 267-6060	Pinball

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Chicago Coin Corporation
Machine Div. Chicago Dynamic Ind.
1725 W. Diversey Blvd.
Chicago, IL 60614
(312) 935-4600

Pinball

Corrobilt Fun Games
8410 Amelia St.
Oakland, CA 94621
(415) 568-5225

Coin-Operated Video

Cromemco
1 First St.
Los Altos, CA 94022
(415) 941-2967

Home Video
Other Games

Electronic Design & Assembly Inc.
2210 S. Priest Dr.
Tempe, AZ 85282
(602) 967-3393

Coin-Operated Video
Home Video

Executive Games
1200 Adams
Dorchester, MA 02124
(617) 296-1420

Home Video

Exidy
166 San Lazaro St.
Sunnyvale, CA 94086
(408) 733-1104

Coin-Operated Video

First Dimension
1234 Lewis St.
Nashville, TN 37210
(615) 256-4392

Home Video

Gamex Industries
Subsid. of Centronics Data Computer Corp.
P. O. Box 14517
Las Vegas, NV 89104
(702) 732-9526

Slot Machines

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Gottlieb, D. & Co. 165 W. Lake St. Northlake, IL 60164 (312) 562-7400	Pinball
Innovation Coin Corp. 1755 Comstock St. Santa Clara, CA 95050 (408) 247-7701	Coin-Operated Video
JRW Electronics Inc. 285 Sobrante Way Sunnyvale, CA 94086 (408) 733-3373	Coin-Operated Video
Magnavox Co. 1700 Magnavox Way Ft. Wayne, IN 46804 (219) 432-6511	Home Video
Meadows Games, Inc. 181 Commercial Sunnyvale, CA 94086 (408) 732-8110	Pinball Coin-Operated Video
Midway Manufacturing Co. Subsid. of Bally Mfg. Corp. 10750 Grand, Franklin Park Chicago, IL 60610 (312) 451-1360	Coin-Operated Video
Mirco, Inc. 1951 W. North Lane Phoenix, AZ 85029 (602) 997-7141	Pinball Coin-Operated Video Home Video
Nutting Associates 500 Logue Ave. Mountain View, CA 94043 (415) 961-9373	Coin-Operated Video
Project Support Engineering, Inc. 525 Del Rey Ave. Sunnyvale, CA 94086 (408) 739-8550	Coin-Operated Video

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Ramtek
292 Commercial
Sunnyvale, CA 94086
(408) 735-8400

Coin-Operated Video

filed for Chpt. XI 7/77

Universal Research Labs
2501 United Lane
Elk Grove Village, IL 62407
(312) 766-6900

Coin-Operated Video
Home Video

Williams Electronics Div.
Seeburg Industries, Inc.
767 Fifth Ave.
New York, N.Y. 10022
(212) 751-5300

Pinball
Slot Machines

2.8.2 Charge Coupled Devices

SUMMARY

This subsection contrasts Charge Coupled Devices with other memory technologies, especially Magnetic Bubble Devices, and discusses their potential applications, markets, prices, technology, and the competitive environment.

Charge Coupled Devices (CCDs) for memory applications were first introduced in 1975 by Fairchild and Intel. We expect Texas Instruments to sample its first CCD product—a 64K device—in the first half of 1977. Another six to eight firms are working on CCDs; consequently, active competition among CCD manufacturers should occur by 1978.

The largest market for CCDs is mass storage systems, where memory size ranges from one-half to 20 megabits; the secondary market is a variety of other applications. The market for CCDs in mass storage systems is estimated to grow from $4 million in 1977 to $75 million in 1981. For CCDs in other applications, the market is expected to grow from $2 million in 1977 to $55 million in 1981. Therefore, the total market for CCDs should grow from $6 million in 1977 to $130 million in 1981.

In 1977, the first Magnetic Bubble Devices (MBDs) will become available on the merchant market. MBDs and CCDs will compete for some of the same markets, particularly the mass storage systems. Actual shipments growth of CCDs will depend upon their availability, existence of second sources, price, performance, acceptance by designers, and competition within the industry.

INTRODUCTION

Overview

Charge coupled devices are generating considerable interest as new, low-cost semiconductor memory devices. CCDs and MBDs are often referred to as "gap filler technologies" because they fill the price and performance gap between semiconductor main memory (bipolar and MOS RAMs) and auxiliary storage (discs and tapes). It is anticipated that CCDs and MBDs will offer a price advantage of 2.5 or 3.0 to 1 over MOS RAMs. With a performance advantage over auxiliary storage and a cost advantage over MOS RAMs, CCDs are well-suited for use in both existing and new applications.

History

Charge coupled devices rely upon the phenomenon of charge coupling in semiconductor materials, which was discovered in 1970 by Willard Boyle at Bell Telephone Laboratories. During the early 1970s, CCD research and development was pursued by a number of companies including Bell Laboratories, Fairchild, Hughes Aircraft, Intel, and Texas Instruments.

In 1975, the first CCD memory product introductions finally occurred. A substantial development effort has also been devoted to CCDs for use in imaging and signal processing applications. These efforts are now yielding CCD cameras and signal processing filters, but these markets are not estimated in this subsection.

The development effort in CCD memories resulted in Fairchild's introducing its 9K CCD in early 1975 and its 16K CCD in late 1975. The 9K device has an unusual architecture that has nine input/output lines accessing synchronized 1024-bit shift registers. Intel introduced its 16K CCD in February 1975. Fairchild and Intel are expected to introduce 64K CCDs in 1977. Texas Instruments is expected to introduce its first CCD device in 1977— a 64K CCD. Besides these companies, another half dozen companies are known to be working on CCDs. As CCD memories find acceptance, product introductions and applications should gain momentum.

2.8.2 Charge Coupled Devices

THE MARKET

CCD Characteristics

To appreciate the applications for CCDs, it is worthwhile to evaluate their characteristics and then compare them with the capabilities of competing technologies. Table 2.8.2-1 lists the projected memory characteristics of CCDs, MOS RAMs, MBDs, and floppy discs for 1977. Figure 2.8.2-1 shows the price/performance characteristics of CCDs and MBDs compared with main memory MOS, bipolar and core technologies, and mass storage disc technology. Figure 2.8.2-2 shows the capacity/performance characteristics of the same memory technologies.

Both the reason for the name "gap filler technology," and the advantages of CCDs are obvious in Table 2.8.2-1. Their access time fills the void between the access times of main memory technologies (roughly 100 to 400 nanoseconds), and mass memory technologies (roughly 100 to 400 milliseconds). The transfer rate for CCDs is 1 to 5 megabits/second per chip, which compares favorably with MOS RAMs and far exceeds magnetic bubbles and floppy discs.

The storage capacity of currently available CCD memory products is 9K and 16K, but 64K CCD chips are expected in 1977. This places the capacity of CCD chips between that of MOS RAMs and MBDs. The read error rate and reliability of CCD memories is expected to be comparable with that of MOS RAMs and MBDs. CCD memories are not removable like the floppy discs, but this is not considered a major disadvantage. Although CCDs are volatile, a CCD memory system can be made nonvolatile by using a battery backup system. CCDs rank second to MOS RAMs in terms of their ease of software and hardware interfacing into a computer mass memory system. This is an important factor, especially considering today's high cost of software.

Since CCDs and MBDs are both new technologies seeking widespread acceptance and applications in the memory field, it is timely and worthwhile to compare these technologies in more detail. Table 2.8.2-2 lists the major characteristics of these technologies. The volatility of CCDs and the non-volatility of MBDs is a major difference, but as noted previously, there are ways around this. Some designers may find batteries inconvenient or undesirable; yet it is a solution if non-volatility is a system requirement. The fact that both CCDs and MBDs are nonmechanical memory technologies enhances their potential as replacements for failure-prone mechanical memory systems.

The small physical size of both CCDs and MBDs further supports both technologies, since mass memories can be implemented on PC boards in the CPU. For example, a 256 Kbyte (2.048 megabits) CCD memory can be implemented with 32 64K CCD devices plus interface and control electronics on a single PC board that can be installed in the minicomputer chassis. This eliminates the need for a separate disc unit and its attendant cabling.

Furthermore, current price comparisons between a CCD memory and a floppy disc are promising. At a price of 40 millicents per bit, 256 Kbyte of CCD memory costs the manufacturer $820. Control and interface circuitry, labor, and the PC board should cost approximately $300. After a 100 percent markup, the selling price for a 2 megabit CCD memory board is $2,240. A floppy disc that can store 2 to 4 megabits sells for $2,000 to $3,000 including drive and controller interface.

CCDs and MBDs have a further advantage—memory modularity. In applications where a smaller mass memory—such as 48 Kbytes—is required, one small PC board in the

2.8.2 Charge Coupled Devices

Table 2.8.2-2

A COMPARISON OF CCD AND MBD CHARACTERISTICS

Charge Coupled Devices	Magnetic Bubble Devices
• Serial Access Memory	• Serial Access Memory
• Shift Register Organization	• Shift Register Organization
• Block Organized	• Block Organized
• Word Addressable	• Word Addressable
• Volatile	• Nonvolatile
• Nondestructive Read	• Nondestructive Read
• Nonmechanical	• Nonmechanical
• Small Physical Size	• Small Physical Size
• Low Power Consumption	• Low Power Consumption
• High Reliability	• High Reliability
• Unidirectional Shifting	• Bidirectional Shifting
• Continuous Shifting	• Stoppable Shifting
• High Serial Transfer Rate	• Low Serial Transfer Rate
• Variable Transfer Rate	• Variable Transfer Rate
• Modular Storage Capacities	• Modular Storage Capacities
• Semiconductor Manufacturing Compatibility	• Few Manufacturing Steps
• Six to Eight Mask Levels	• One or Two Mask Levels

Source: DATAQUEST, Inc.

1981. Thus, the total market for CCDs is $6 million in 1977 and $130 million in 1981. It should be emphasized that any one of these markets could rapidly develop and become an even more attractive market than estimated. This is especially true in the area of other applications. As designers begin using CCDs, they will discover more attractive opportunities for the devices.

Selling Price of CCD Memory

The estimated average selling price of CCD memory over the next five years is shown in Table 2.8.2-4. Also included in the table are the estimated average selling prices of MBDs and MOS RAMs. As shown, the CCDs are expected to be selling at 40 millicents per bit in 1977 and to decrease to 9 millicents per bit by 1981. MBD prices are expected to be very competitive with CCD prices over this period. Hence, the price advantage of CCD and MBD memory over MOS RAM is in the 2.5 or 3.0 to 1.0 range over the next five years.

Earlier, it was thought that there could be a tenfold price advantage of CCDs over MOS RAMs. Unfortunately, this has not occurred, nor is it likely to occur. If CCDs could offer a tenfold price advantage over MOS RAMs, their development and application would likely be much further advanced.

Because the price advantage is not as sig-

2.8.2 Charge Coupled Devices

Table 2.8.2-3

ESTIMATED WORLDWIDE MARKET FOR CHARGE COUPLED DEVICES
(Dollars in Millions)

	Charge Coupled Devices[1]		
Mass Storage Systems	**1977**	**1978**	**1981**
Fixed and Moving Head Disc	2	7	35
Floppy Disc and Cassette	2	11	40
Subtotal	4	18	75
Other Applications			
Microcomputer Systems	1	2	15
Military Systems	-	2	12
Intelligent Terminals	-	-	2
Programmable Calculators	-	-	1
Games	-	3	15
Automotive	-	-	3
Other	1	1	7
Subtotal	2	8	55
Total Market	6	26	130

[1] Non-memory applications for CCDs are not included in these estimates

Source: DATAQUEST, Inc.

nificant as had been hoped for, application of CCDs will not always be obvious. In some main memory extensions where a very low-priced CCD might have been used, the CCD at expected prices might be less attractive than the MOS RAM. On the other hand, while CCDs are more expensive on a per-bit basis than some disc systems, they may find applications due to their reliability, modularity, access speed, and transfer rate.

As in all new markets, it is difficult to foresee all the applications that innovative designers will find for the device. It is expected that CCDs will appear in some applications not currently discussed.

Impact of Other Technologies

One of the most frequently asked questions regarding CCD applications is what effect MBDs will have upon CCD markets. The answer is not clear at this early stage of market development, but market segments exist where one or the other has a clear advantage. The military prefers MBDs because of their non-volatility, while in games and video refresh memories CCDs have the advantage over MBDs because of their higher transfer rate. In intelligent terminals and programmable calculators, magnetic bubbles are preferred because they are non-volatile.

The mass storage market is available to penetration by both CCDs and MBDs. In fact, our estimates reflect an equal market in mass memories for each technology, since currently neither technology has a clear advantage. Such factors as availability of memory devices and interface chips, availability of second sources, price, reliability, and user acceptance will eventually determine the market share that CCDs realize.

CCD OPERATION

Device Operation for Memory Applications

(A detailed description of the basic physical operation of CCDs can be found in Section 4.3 of this notebook.)

A CCD memory chip can be organized in any one of several ways, but the Series-Parallel-Series (SPS) shift register organization shown in Figure 2.8.2-3 is the most common for large capacity chips because it minimizes chip size

2.8.2 Charge Coupled Devices

Table 2.8.2-4

ESTIMATED AVERAGE SELLING PRICE OF CCD MEMORY
(Millicents per Bit)

	1977	1978	1979	1980	1981
Charge Coupled Devices (CCDs)					
9K CCD	60	-	-	-	-
16K CCD	50	30	-	-	-
64K CCD	40[1]	25	15	10	9
256K CCD	-	-	18	12	9
Magnetic Bubble Devices (MBDs)					
20K MBD	50	35	20	-	-
92K MBD	40[2]	26	15	10	9
256K MBD	-	35	18	12	9
1M MBD	-	-	-	15	12
MOS RAMs (ASP for Standard Device)					
1K RAM (Static)	220	190	160	140	125
4K RAM (16-Pin, Dynamic)	113	88	75	63	50
4K RAM (Static)	200	160	140	125	110
16K RAM (16-Pin, Dynamic)	106	69	44	31	25
64K RAM	-	78	47	28	22

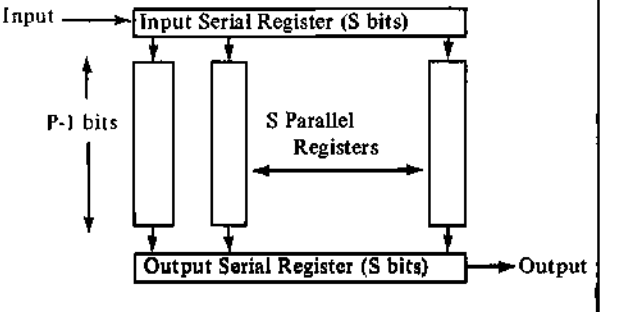
[1] Samples--1st quarter 1977
[2] Samples--4th quarter 1976

Source: DATAQUEST, Inc.

and power. A serial bit sequence enters the input gate and is shifted into the S bit input serial register until it is filled. All S bits are then simultaneously transferred into the parallel shift registers. The data bits are shifted through the parallel section until they move into the output serial register out of which they are serially shifted. Since the bits are shifted S times in the serial register before each shift into the parallel section, the parallel registers are clocked at frequency f/S. The advantage of this structure is that all bits move in the same direction; thus, clocking is easier, and each bit traverses a fewer number of memory cells, which requires less refreshing. A drawback is the fact that two clocks are required.

Figure 2.8.2-3

SERIAL-PARALLEL-SERIAL
(SPS) REGISTER



Source: DATAQUEST, Inc.

Other CCD memory structures include a serial register, a serpentine register, a line addressable random access memory (LARAM), a time phase multiplexed SPS register, and a time phase multiplexed electrode-per-bit organization. These formats are not as widely used for CCD memory chip organization.

Device Operation for Other Applications

The ability to generate, shift, and detect many separate charge packets in a small piece of semiconductor material suggests that CCDs can serve a number of information processing applications. CCDs are especially well-suited for imaging and signal processing applications.

When light falls on the CCD substrate, the radiation is absorbed, resulting in the generation of electrons in a quantity proportional to the amount of incident light. The CCD array of potential wells will contain differing levels of charge concentration corresponding to the different amounts of light focused on them. The charge packets in each row of the CCD array can then be shifted out serially to a detector, and converted to an electrical signal that is representative of a horizontal row of the optical image of the signal displayed on a video screen.

The advantage of CCD devices over conventional television cameras is that the majority of the signal processing can be done on one, small silicon chip. This eliminates the need for an electron scanning beam, high voltages, and the associated circuitry required by conventional television cameras to convert optical images to electrical signals. Furthermore, the CCD chip is small, operates at high speed, has low power dissipation, and offers solid-state reliability. CCD images are exceptionally sensitive at very low light levels and can be fabricated to be sensitive to infrared light, which would make them applicable for special military and security requirements. CCDs are already being used in hand-held black and white TV cameras. Their color response is not currently adequate for use in color TV cameras.

The CCD can also function as a delay line for digital or analog signals. Any signal placed at the input of a CCD serial shift register will appear at its output after an interval required for the charge packets to be shifted through the shift register. The delay can be varied by varying the clock rate applied to the CCD shift register and by varying the length of the shift register. Two variations of delay lines are possible with CCDs. The first is a simple delay in which the signal is simply delayed. In the second, data that appear in bursts can be loaded into the CCD during the burst, retained for the desired delay, and then read out at a slower rate; this is referred to as a buffer function. Delay lines with such flexibility should be of considerable value in radar, communications, and television applications and will simplify existing methods of producing controlled delays.

A simple extension of the delay line concept leads to filters for signal processing applications. If a delay line is fabricated with interim taps where the signal can be sensed, weighted, and fed back to earlier stages in such a way as to impact the signal transmission, the structure can serve as a signal processing filter. A variety of band pass and matched filters have been fabricated from CCDs for signal processing applications in such areas as radar and sonar.

PROCESSING TECHNOLOGY FOR CCDs

A CCD is a MOS device; it therefore uses the silicon processing technology that has been extensively developed. Producing a CCD involves eight mask levels, which requires a high degree of alignment accuracy. The 64K CCDs forthcoming in 1977 are expected to occupy approximately 40,000 square mils. This implies a cell size of approximately 0.4 square mils and

line widths of 0.1 to 0.2 mils. These requirements are well within the limits of conventional photo lithography and processing technology. The next CCD device will probably be a 256K CCD, with a cell area of 0.2 to 0.3 square mils and line widths of 0.1 mils. These dimensions place more stringent requirements on the lithography and processing, but are still within the limits of conventional photo lithography.

The most important point is that CCDs use existing MOS technology. Any company manufacturing MOS is a potential manufacturer of CCDs, since it can use the same processing equipment that it has in place for MOS processing. This contrasts with MBD manufacturing, which uses equipment unique to the garnet technology of magnetic bubbles. Few MOS engineers understand magnetic technology in the depth required to design and fabricate MBDs. Consequently, a semiconductor firm interested in pursuing MBDs must make an investment in personnel and capital equipment not required for CCDs. If an MOS manufacturer were to begin CCD and MBD development and manufacture simultaneously, the MBD team would be at a disadvantage to the CCD team in terms of both lead time (12 to 18 months) and investment cost ($3-5 million).

COMPETITION

Only Fairchild and Intel currently offer CCD products. Texas Instruments is expected to join the race in 1977 when it begins delivery of its 64K CCD. Other firms known to be working on CCDs include AMD, AMS, Hitachi, Motorola, National, Signetics, and Toshiba; we expect product introductions from these firms in 1977 and 1978. We estimate that Intel has 60 percent of the current market. However, the market is still in its infancy, and it is too early to forecast market shares of all the potential competitors.

2.8.3 Magnetic Bubble Devices

SUMMARY

This subsection contrasts Magnetic Bubble Devices with other memory technologies, especially Charge Coupled Devices, and discusses their potential applications, markets, prices, technology, and the competitive environment.

Recently there has been increasing interest in Magnetic Bubble Devices (MBDs) and their potential markets. Since the discovery of MBDs in 1967, considerable research activity has occurred, and several product announcements have been made recently. Hitachi has announced a 20-kilobit chip and Texas Instruments has announced a 92-kilobit chip. Both firms began sampling devices in 1976 and should be shipping them in larger quantities in 1977.

The market for MBDs is expected to grow from $6 million in 1977 to $141 million in 1981. Magnetic bubbles should find their largest market in mass storage systems for minicomputers and larger computer systems. This market is expected to grow from $4 million in 1977 to $75 million in 1981. Secondary markets for MBDs should be a variety of other applications, including microcomputer systems, military systems, terminals, programmable calculators, entertainment systems, and automotive systems. The market for these other applications is expected to grow from $2 million in 1977 to $66 million in 1981.

An interesting confrontation is likely to occur between MBDs and Charge Coupled Devices (CCDs) in those markets that both technologies can serve equally well. Mass storage systems is one market in which keen competition is expected between MBDs and CCDs, and it is too early to predict which technology will win. The acceptance of magnetic bubbles and CCDs will depend upon their availability, performance, price, and the competitive moves made by the respective manufacturers.

INTRODUCTION

Overview

Magnetic bubble devices have generated substantial interest as a "gap filler technology." They will fill the performance gap between the access times of main memory and mass storage, and the price gap between high cost main memory and low cost mass storage systems. Magnetic bubble devices are expected to have a price advantage of 2.5 or 3 to 1 over that of MOS random access memory (RAM). With a performance advantage over mass storage systems and a price advantage over main memory, MBDs should find their way into many existing and new applications.

History

MBDs were discovered in 1967 at Bell Telephone Laboratories, and most of the early research on magnetic bubbles was conducted there. Within a few years, however, research was conducted at IBM, Rockwell, and Texas Instruments, and more recently at several foreign laboratories, namely Fujitsu, Hitachi, Nippon Electric, Plessey, Philips, and Siemens. MBD development has been stimulated by government funding which is intended to expedite the availability of magnetic bubble memories for military and NASA programs.

Because magnetic bubbles depend upon magnetics technology rather than silicon technology, most semiconductor firms are not actively pursuing magnetic bubble devices. However, some of the larger minicomputer and mainframe companies are pursuing device development and system applications of magnetic bubbles; these include Burroughs, CDC, Hewlett-Packard, IBM, and Univac. Further discussion of their competitive positions appears in a later section.

2.8.3 Magnetic Bubble Devices

THE MARKET

MBD Characteristics

To appreciate the applications for magnetic bubbles, it is helpful to first consider their characteristics. In Table 2.8.3-1, the characteristics of MBDs are listed together with those of CCDs, MOS RAMs, and floppy discs. In Figure 2.8.3-1, the price/performance of MBDs and CCDs is contrasted with that of main memory and mass storage technologies. Figure 2.8.3-2 shows the capacity/performance of these memory technologies. The access time of magnetic bubbles falls between that of main memory (roughly 100 to 400 nanoseconds) and that of mass storage systems (roughly 100 to 400 milliseconds). The price of magnetic bubbles is also between that of higher cost main memory (generally greater than 100 millicents per bit) and lower cost mass storage (generally less than 10 millicents per bit).

Table 2.8.3-1 shows that the time to access the first word in magnetic bubble devices is in the range of one to three milliseconds. Transfer rates for magnetic bubbles are on the order of 100 kilobits per second per chip. Magnetic bubbles have a slower transfer rate and a longer access time that that of CCDs; they are presently approximately one-tenth as fast. However, this disadvantage can be overcome by paralleling bits, and by advances in the magnetic bubble technology, which is anticipated for the 1978 to 1980 era.

Based upon presently announced magnetic bubble products, the current storage capacity per chip is in the range of 20 kilobits to 92 kilobits. In some applications, several chips are being packaged in a single module to produce a high-capacity module. Magnetic bubbles are more reliable and incur fewer read errors than mass storage systems, which incorporate rotating magnetic media. Magnetic bubble devices incorporate solid state phenomenon, and the inherent reliability is one of their most important advantages in terms of eventually displacing rotating mass storage systems.

Since magnetic bubbles and charge coupled devices are coming to market at roughly the same time, it is important to compare their characteristics. Table 2.8.3-2 lists the major characteristics of both technologies. Like other mass storage media, both are serial access memories; this is in contrast with main memory technology, which is random access. Both are organized as shift registers, and the data are generally block-oriented. Furthermore, the technologies have the important features of being nonmechanical, small, low-power, and highly reliable, which makes them attractive candidates for mass storage systems.

Magnetic bubble devices are non-volatile, which means they do not lose their stored information when the power has been removed. Because they are non-volatile, the bubbles can be stopped when the memory is quiescent, which saves power and can improve the access time. This is in contrast to CCDs, where the shifting and charge regeneration must be continuous to maintain the memory contents. Many potential users believe that non-volatility is a very important characteristic of magnetic bubbles, but it is difficult to assess its eventual impact on the markets that magnetic bubbles serve. Certainly, the military is interested in having non-volatile memories; yet in commercial markets, properties other than volatility alone are expected to affect the preference for magnetic bubbles.

The ease with which magnetic bubbles can be interfaced into a system is very important to the designer and affects the memory price. The hardware and software interfacing of magnetic bubble devices is more difficult than that for CCD and MOS RAM main memory, yet easier than that for disc and tape mass storage technologies.

2.8.3 Magnetic Bubble Devices

Table 2.8.3-2

A COMPARISON OF CCD AND MBD CHARACTERISTICS

Magnetic Bubble Devices	Charge Coupled Devices
• Serial Access Memory	• Serial Access Memory
• Shift Register Organization	• Shift Register Organization
• Block Organized	• Block Organized
• Word Addressable	• Word Addressable
• Nonvolatile	• Volatile
• Nondestructive Read	• Nondestructive Read
• Nonmechanical	• Nonmechanical
• Small Physical Size	• Small Physical Size
• Low Power Consumption	• Low Power Consumption
• High Reliability	• High Reliability
• Bidirectional Shifting	• Unidirectional Shifting
• Stoppable Shifting	• Continuous Shifting
• Low Serial Transfer Rate	• High Serial Transfer Rate
• Variable Transfer Rate	• Variable Transfer Rate
• Modular Storage Capacities	• Modular Storage Capacities
• Few Manufacturing Steps	• Semiconductor Manufacturing Compatibility
• One or Two Mask Levels	• Six to Eight Mask Levels

Source: DATAQUEST, Inc.

that range from one-half to 20-megabit capacity. Magnetic bubbles are expected to partially displace fixed- and moving-head discs, floppy discs, and cassette storage media. Penetration into these markets is expected for three reasons: higher reliability of the magnetic bubbles, the convenience of mass storage packaged within the minicomputer, and competitive prices.

Secondary markets for magnetic bubbles are expected in an array of other applications. These include microcomputer systems in which small to moderate amounts of mass storage are required for some applications. Bubble memory systems, with their modular storage capability, can easily handle these requirements. The military and NASA generally prefer MBDs over CCDs because they are non-volatile and radiation resistant. Computer terminals and programmable calculators are another application where the non-volatility of MBDs is very important. A single 20-kilobit bubble chip can easily store several programs for a programmable calculator. A 92-kilobit bubble chip could store a salesman's records for use in a portable computer terminal that he carries with him. Other market areas for magnetic bubbles include games, radio, TV, CB, automobiles, typewriters, office equipment, point of sale terminals, and displays. The amount of memory used in entertainment and automotive applications is often only a few hundred bits, but the number of devices per application can run into

2.8.3 Magnetic Bubble Devices

the millions. However, in applications requiring a few hundred to a few thousand bits of non-volatile storage the floating-gate avalanche-injection metal-oxide-semiconductor (FAMOS) types and the metal-nitride-oxide-semiconductor (MNOS) types will likely be more competitive than MBDs because they are available in smaller memory sizes (2K and 8K) and their cost of interfacing is relatively lower.

Table 2.8.3-3 lists the estimated markets for magnetic bubbles for the period 1977 to 1981. The market in mass storage systems is expected to grow from $4 million in 1977 to $75 million in 1981. The market for other applications is expected to grow from $2 million in 1977 to $66 million in 1981. Thus, the total magnetic bubble market is estimated at $6 million in 1977 growing to $141 million in 1981. It is difficult to anticipate every application that can develop as this new technology comes to market; consequently, large markets currently unforeseen could develop. A few major new applications could significantly expand the total market for magnetic bubbles.

Table 2.8.3-3

ESTIMATED WORLDWIDE MARKET FOR MAGNETIC BUBBLE DEVICES (Dollars in Millions)

	Magnetic Bubble Devices		
Mass Storage Systems	**1977**	**1978**	**1981**
Fixed and Moving Head Disc	2	7	35
Floppy Disc and Cassette	2	11	40
Subtotal	4	18	75
Other Applications			
Microcomputer Systems	1	2	18
Military Systems	-	2	20
Intelligent Terminals	-	1	5
Programmable Calculators	-	1	4
Games	-	-	1
Automotive	-	-	8
Other	1	1	10
Subtotal	2	5	66
Total Market	6	23	141

Source: DATAQUEST, Inc.

Average Selling Price of MBDs

The estimated average selling price of MBDs over the period 1977 to 1981 is shown in Table 2.8.3-4. Also included are the estimated average selling prices of CCDs and MOS RAMs. As indicated in Table 2.8.3-4, magnetic bubble prices are expected to decline from 40 millicents per bit in 1977 to 9 millicents per bit by 1981; CCDs should follow a similar decline over the same time period. Thus, the cost advantage of magnetic bubbles and CCDs over MOS RAMs is expected to be in the range of 2.5 or 3.0 to 1.0 over the next five years.

When one considers the cost of the memory devices plus the cost of interfaces and controls, the cost advantage of MBDs over MOS RAMs is closer to 2.0 to 1.0 than 3.0 to 1.0. Hence, there will be some applications where the choice between MBDs and MOS RAMs is not clear. However, magnetic bubbles do have the advantages over MOS RAMs of high density and non-volatility, which makes them attractive for many applications. The important point is that MBDs must be sold on the basis of price and performance rather than on price alone.

2.8.3 Magnetic Bubble Devices

Table 2.8.3-4

ESTIMATED AVERAGE SELLING PRICE OF MBD MEMORY
(Millicents per Bit)

	1977	1978	1979	1980	1981
Magnetic Bubble Devices (MBDs)					
20K MBD	50	35	20	-	-
92K MBD	40[1]	26	15	10	9
256K MBD	-	35	18	12	9
1M MBD	-	-	-	15	12
Charge Coupled Devices (CCDs)					
9K CCD	60	-	-	-	-
16K CCD	50	30	-	-	-
64K CCD	40[2]	25	15	10	9
256K CCD	-	-	18	12	9
MOS RAMs (ASP for Standard Device)					
1K RAM (Static)	220	190	160	140	125
4K RAM (16-Pin, Dynamic)	113	88	75	63	50
4K RAM (Static)	200	160	140	125	110
16K RAM (16-Pin, Dynamic)	106	69	44	31	25
64K RAM	-	78	47	28	22

[1] Samples–4th quarter 1976
[2] Samples–1st quarter 1977

Source: DATAQUEST, Inc.

Impact of Other Technologies

Since MBD, CCD, and electron beam addressed memories all occupy the price/performance gap between main memory and mass storage in Figure 2.8.3-1, they are technologies competing for the same markets. The electron beam addressed memory (EBAM) is a CRT tube on the face of which bits of information are stored in an MOS matrix structure. The matrix is written and read under the control of a finely focused electron beam, and information is stored in the MOS patterns as the presence or absence of charge. Writing or reading information from the matrix is accomplished by the electron beam, together with gating circuitry which gates information into or out of the individual storage locations. The minimum size of an EBAM memory is approximately 16 million bits, which places the EBAM memory into a class by itself where it must serve special markets with fairly large storage requirements.

Currently, the military is the major proponent of EBAM memory. General Electric in Schenectady, New York has been funded for several years to develop the EBAM. Because the EBAM memory has a large minimum size and because it is not expected to be as reliable as MBD and CCD memories, it is not foreseen as a major threat to MBDs in the applications discussed in Table 2.8.3-3. Furthermore, the electron tube and its electromagnetic focusing

are not readily adaptable to batch fabrication in the same sense that magnetic bubble and other semiconductor memories are; hence, the cost experience curve cannot be fully applied to the manufacture of the EBAM memory.

CCDs are a more immediate threat to MBDs in jointly served markets; this is especially true in mass storage. Our estimates reflect an equal market in mass memories for MBDs and CCDs, since a well-defined winning technology does not exist at this early stage. CCDs should compete effectively in the other applications areas, such as games and video terminals, because of their higher transfer rate. In military applications and microcomputer systems, magnetic bubbles have the advantage of their non-volatility. In the home entertainment and automotive areas, magnetic bubbles hold an advantage because of their non-volatility. Time and user acceptance will eventually determine the winners in these areas.

Volatility and speed are the major differences between MBDs and CCDs, and they could dictate the use of one or the other technology in a particular application. However, design innovations exist that can be used to minimize the impact of these differences, and a company advocating one technology or the other will certainly use these design innovations to gain advantages for its chosen technology.

Aside from the physical differences between magnetic bubbles and CCDs, major differences will most likely be generated by the competitive strategies of the companies making MBDs and CCDs. Such developments as availability of memory chips, presence of second sources, availability of interface chips, reliability, price, and user experience will eventually be factors that will determine the market shares of MBDs and CCDs.

For applications requiring fewer than 10 kilobits of non-volatile storage, FAMOS and MNOS memories are less expensive than MBD memories. FAMOS devices are erasable by the application of ultraviolet light and are electrically erasable and MNOS devices are electrically erasable. The erase time ranges from one-half minute for the electrically erasable FAMOS device to 30 minutes for the ultraviolet erasable type. On the other hand, MBD devices do not require an erase cycle before writing new information and MNOS devices can be erased in under a second. Therefore, both price and performance must be considered in the trade-off between MBDs, FAMOS, and MNOS devices.

MBD OPERATION

Device Operation for Memory Applications

(A detailed description of the physical operation of magnetic bubble devices can be found in Section 4.5 of this notebook.)

Magnetic bubbles are really cylindrical, magnetic domains whose magnetization is opposite to that in the remainder of the thin magnetic garnet layer in which they exist. These cylindrical domains are visible under polarized light and appear as bubbles—hence the name.

Magnetic bubbles can be generated by applying appropriate current pulses to a "hairpin" loop of wire directly over the thin garnet layer. The presence and absence of bubbles is used to represent the 1s and 0s in a binary data stream. The bubbles are shifted into and stored in long shift registers until they are recalled for readout at a later time. Bubbles are propagated in the garnet film by applying a rotating magnetic field in the plane of the garnet film. When a segment of the data stream is to be read out, these bubbles are shifted to a bubble detector where the presence and absence of bubbles is converted to voltage levels representing 1s and 0s.

The preferred architecture for MBD chips is the major/minor loop shown in Figure 2.8.3-

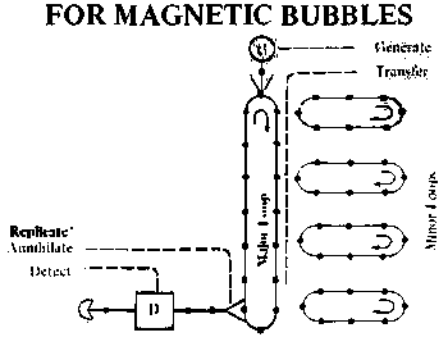
3. This architecture consists of one major loop and multiple minor loops. As bubbles are generated in the major loop, they are shifted around the loop until a block of data lines up with the minor loops. Under external control, the transfer gate enables the transfer of bubbles between the major and minor loops. This process can continue until all the bubble positions in the minor loops are filled. To read the bubble memory contents, an entire block (one bit from each minor loop) is transferred to the major loop. The bubbles in the major loop are then propagated around the loop and detected. Another bubble chip architecture is the serial register that uses one long serial register to store the data. This architecture is not as popular as the major/minor loop structure, because it has an inherently lower yield for the same memory capacity.

Device Operation for Other Applications

Since magnetic bubbles are visible under polarized light, they offer potential for use in displays. By using a series of dots (bubbles) to generate line segments, numeric and alphanumeric characters can be created. This non-memory application of magnetic bubbles is still relatively new and remains more of a laboratory curiosity than a growing application area.

Figure 2.8.3-3

MAJOR-MINOR LOOP ARCHITECTURE FOR MAGNETIC BUBBLES



Source: DATAQUEST, Inc.

PROCESSING TECHNOLOGY FOR MAGNETIC BUBBLES

The manufacture of magnetic bubble devices involves fewer and simpler manufacturing steps than that required for bipolar or MOS integrated circuits. Most magnetic bubble chip designs require only two mask levels—one for the permalloy overlay pattern and one for the conductor pattern. This is simpler than a typical CCD design, which requires seven or eight mask levels and very careful mask alignment.

Magnetic bubbles and CCDs differ in the crystal pulling, in the front end of the wafer fabrication, in testing, and in packaging. The pulling of GGG crystals is a difficult and new process compared to the well-established silicon crystal pulling technology. Once the crystal has been sliced and the wafers have been polished, an epitaxial layer is grown on the wafer. This garnet epitaxial layer is the thin magnetic film in which the magnetic domains shape the stubby cylinders known as magnetic bubbles. Pulling the crystals and growing the epitaxial film are two of the most difficult and exacting processes in fabricating magnetic bubbles. Fortunately, wafers with the garnet film are commercially available from suppliers. The remainder of the processing uses standard photolithography imaging and processing. Testing the complex bubble chip will be one of the major challenges in their manufacture. Packaging the bubble chips between bias magnets and crossed coils is a difficult packaging job. Single magnetic bubble chips are being packaged with bias magnets and crossed coils in a 14-pin dual in-line package.

Although much of the processing for magnetic bubbles resembles that of semiconductors, bubble technology is not a simple extension of

in-house capability for a semiconductor firm. It requires design, process, and applications engineers who are skilled in magnetics. With the dynamic growth of semiconductor technology over the last two decades, there have been comparatively few specialists in magnetic materials. Therefore, a semiconductor firm interested in creating a magnetic bubble effort would have to attract some of the existing talent from companies such as Bell Labs, IBM, Rockwell, and Texas Instruments. We estimate that a semiconductor firm interested in manufacturing MBDs must make at least a $3 to $5 million investment before being able to sample devices 18 months later. For these reasons, we do not expect semiconductor firms to quickly begin developing and manufacturing magnetic bubbles; instead, we expect them to closely watch the market develop before they decide whether or not to actively pursue it.

COMPETITION

Currently, two of the major firms pursuing magnetic bubbles are captive manufacturers; they are Bell Labs and IBM. Bell Labs discovered magnetic bubbles in 1967 and is an important leader in this technology. In 1976, it put a magnetic bubble production line into operation in the Western Electric plant at Reading, Pennsylvania. We understand that Western Electric's first application for magnetic bubbles will be a voice recorder. It will package several 20-kilobit chips into a 272-kilobit module for recording 10 seconds of digitized voice. These modules will be used in its voice announcement system, which plays recorded messages such as, "This is no longer a working number; please check your directory." The high reliability of MBDs make them an ideal replacement for the failure-prone mechanical tape cassette storage system currently in use. Other potential telephone company applications include the use of bubble memories in repertory dialers and in mass storage systems to replace disc storage. Currently, telephone office executive routines are stored on disc files. Since telephone equipment requires extremely high reliability over a 40-year lifetime, bubble memories are an attractive alternative to rotating memories for the Bell System.

IBM is still in a research mode on magnetic bubbles and is working energetically on bubbles at its Watson Research Laboratory in Yorktown Heights, New York as well as at its San Jose, California research laboratory. Although IBM will be a captive manufacturer, it is expected to be a powerful force in the market once it begins putting magnetic bubbles into mass storage systems. With bubbles, IBM could insert a modest amount of data processing into the storage areas and vice versa. While this may not significantly change computer throughput, it would certainly disrupt the markets of plug-compatible disc manufacturers. Furthermore, MBDs promise about a tenfold improvement in access time that would not be easy to duplicate in standard disc technology.

Texas Instruments has an engineering pilot line that began producing MBD chips in the second quarter of 1976. It began shipping sample quantities in the fourth quarter of 1976 and should begin delivery of higher volumes in the first quarter of 1977. TI has an estimated 100 people working on magnetic bubbles including engineers, technicians, and production workers. The company has made a major commitment to make magnetic bubbles a success. In addition to the corporate commitment, it has received substantial government funding in magnetic bubble research and development since the early 1970s. TI plans to sell magnetic bubble chips and associated support circuitry in the merchant market. Currently, it has no announced plans to make and sell magnetic bubble memory systems; however, plans can certainly be developed quickly if TI determines that the memory system business is a worth-

2.8.3 Magnetic Bubble Devices

while opportunity.

Rockwell International has a small bubble pilot line and has been funded by several major government contracts. Its capacity is much less than that of TI, and it has a different marketing plan, which is to make and market magnetic bubble systems rather than to sell the chips. Rockwell has begun sampling memory systems for POS terminals; this 800-kilobit memory will include eight 100-kilobit chips, plus all the necessary control and interface circuits.

In addition to the above, there are several minicomputer and mainframe manufacturers that are actively following magnetic bubbles. However, they are not in a position to be manufacturing them in the near future. These include Burroughs, Hewlett-Packard, and Univac. Typically, they have fewer than ten people; in some cases, fewer than five work on magnetic bubbles for both device and system application aspects. In Japan, Hitachi has announced and begun sampling a 20-kilobit magnetic bubble device. It will likely begin shipments of larger quantities in the first quarter of 1977. Its pilot line capacity is believed to be comparable to that of Texas Instruments. Fujitsu has reportedly made an 80-kilobit chip that is still in the laboratory stages. Nippon Electric has demonstrated 16-kilobit chips and has a 100-megabit system that is still in development. In Europe, Plessey has reportedly made some 8- and 16-kilobit chips, but development is in a laboratory phase. Philips and Siemens are conducting magnetic bubble research.

6.1 Microcomputers

MICROCOMPUTER MARKET CHARACTERISTICS

Introduction

At the low end of the computer price and performance scale, a growing number of products exist that are generally labeled "microcomputers." Although this term is rather ill defined within the computer industry, it generally refers to low-cost computer CPUs supplied on circuit boards and built using some form of semiconductor LSI. System level products, which include power supply and cabinet, adopt the name microcomputer when their price and performance place them clearly at the bottom end of the minicomputer market performance spectrum.

The products included in DATAQUEST's definition of a microcomputer are 8-bit board- and system-level products as well as 12- and 16-bit board-level products. At the system level, 12-bit and 16-bit products are no longer classed as microcomputers and are therefore not included in this discussion. Also excluded from this analysis are microprocessor development systems, custom board products, prototyping boards sold by semiconductor suppliers to familiarize their customers with microprocessors, and dedicated small computer systems that incorporate CPU, keyboards, displays, and peripherals in a single enclosure. The analysis focuses on the general purpose board and systems market at the OEM level and excludes the peripherals, software, and service associated with the end-user system market. Stand-alone microprocessor program development systems are treated separately in Section 6.2.

Within the context of the hardware classification of DATAQUEST's Minicomputer Industry Service (MCIS), this section covers Class I boards and systems and Class II and Class III board-level products only. It also includes all current personal computer kits and boards.

The term microcomputer will be used as a generic term to cover all products specifically included in this analysis. In some cases, the products currently do not use LSI devices in the CPU, but the evolution of the technology and upgrading of product lines by suppliers dictates that in the near future virtually all microcomputer products will be implemented with some form of LSI devices for the CPU function. The use of LSI semiconductor memory is already well accepted in computers of all sizes and dominates microcomputer memory implementation.

Although products for the experimenter/hobbyist market have traditionally been sold in kit form, they are included in this analysis because of the importance of the market and of the major suppliers that have evolved from it. The experimenter/hobbyist market is considered a consumer market and is included in the "other" category of microcomputer applications. For more detailed information on the personal computer market, please refer to Section 6.3.

Industry Structure

The microcomputer market is structured in a unique manner as a result of three diverse types of suppliers to the market. The three supplier groups are: (1) traditional minicomputer manufacturers; (2) a new group of suppliers specializing in microcomputers; and (3) semiconductor suppliers. This combination brings to the market three completely different sets of perspectives, distribution methods, and marketing philosophies.

Although traditional minicomputer companies like Computer Automation have been supplying board-level products for many years, the semiconductor suppliers provided the first really low-cost, general purpose boards and systems when they introduced the 8-bit micro-

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processor chip sets in 1973. A group of small entrepreneurial firms exploited this new technology and began marketing products for industrial control, data acquisition, and hobby applications.

As a result, until recently, the market was structured according to heritage. The minicomputer suppliers were offering low-cost 16-bit machines with upward-compatible instruction sets, such as the DEC LSI-11. The specialized microcomputer suppliers (such as MITS and IMSAI) were supplying 8-bit systems based on the Intel 8080 CPU chip to industrial and hobby customers. The semiconductor firms are now participating in this market with a full range of products based on microprocessor and memory technology. The high semiconductor content of both board- and system-level low-end products makes them attractive to the semiconductor suppliers and provides a competitive edge from a cost standpoint.

The structure of the industry will continue to evolve rapidly as specialized microcomputer firms move away from the experimenter/hobbyist market, which provided their initial customer base, into the more traditional OEM and end-user markets. It is expected that over the long term, the semiconductor suppliers will dominate the OEM market in both 8- and 16-bit board-level products due to their cost advantage and technology position. Although the minicomputer firms will continue to be a factor in the 16-bit board market, it is expected that their low-cost processor capability will increasingly be used to support their own end-user-oriented products where software, system architecture, and customer support are important factors.

Participants

The microcomputer market has brought together a large number of competing suppliers with different sets of strengths and weaknesses for a share of the low-performance board and systems market. Many of the small firms were able to enter the market due to the initial acceptance of kit-type products for the hobby market. The rapid movement of the market no longer makes it possible for a new start-up to gain significant market share in a short period of time. The experimenter/hobbyist market (with its cash-before-delivery method of operation) created the opportunity for a new computer supplier to start and grow. However, this market is undergoing a number of major changes, among which is a transition to preassembled systems that considerably increase the capital requirements for market participation. As a result, the market is already somewhat stabilized in terms of the suppliers that will be important to the future of the OEM board and systems markets.

Major minicomputer firms with a position in the OEM microcomputer market include Computer Automation, Data General, DEC, General Automation, and Interdata. Microdata has chosen to de-emphasize this market. Of those firms committed to this market, only Data General and DEC have a captive semiconductor source. Other suppliers use custom chips purchased from outside vendors. Texas Instruments is a difficult company to categorize. Using the 16-bit processor chip, it has introduced board- and system-level products from the Digital Systems Division and OEM boards and development systems from the Semiconductor Division.

Specialized microcomputer suppliers focusing on system-level products include Control Logic, Cromemco, The Digital Group, IMSAI, MITS, Polymorphic Systems, and Warner and Swasey. These firms are also active in the board-level market. Although many of these suppliers are supplying kits to the experimenter/hobbyist market, the general purpose design of the products and the trend away from the hobby area are permitting these firms to

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move into the more traditional OEM markets in communications, industrial control, and instrument and lab automation.

Since its acquisition by Pertec, MITS has enlarged its dealer organization and expanded its system level offerings in the business systems market. Products for the hobby market now are a small percentage of total sales. This same trend away from the hobby market now characterizes all of the major microcomputer board and system suppliers. As the semiconductor manufacturers move more agressively into the OEM board and box market, the smaller microcomputer suppliers will be forced to move more in the direction of integrated systems for small business use. IMSAI has already started to change its emphasis from the OEM-type CPU products to its new series of integrated desktop systems.

The smaller microcomputer firms tend to be privately held and are growing rapidly. This combination produces financial stresses that have been encountered by all the major firms including IMSAI, MITS and Processor Technology. The Digital Group and TDL/Xitan have recently been through reorganizations and have brought in additional outside funds through private investors.

All the semiconductor companies including Intel, Mostek Motorola, National, TI, and Zilog have made strong entries into the OEM board and box market. Recently AMD, Fairchild, General Instruments, and Synertec have introduced board-level OEM products based on their microprocessor chip sets. The semiconductor suppliers are now approaching the microcomputer market as a separate profit center and as a business diversification rather than a simple extension of their chip business. Zilog, in particular, has introduced a series of OEM microcomputer systems that include intelligent terminals, floppy discs, and printers. National appears to be moving in the same direction.

With their inherently better cost position on microprocessors and memory, the semiconductor manufacturers can be expected to evenutally dominate both the 8- and 16-bit board markets and move aggressively into low end system level products. New microprocessor designs are expected to allow the semiconductor suppliers to market highly competitive products for sophisticated small business systems and low-cost industrial control applications.

The minicomputer manufacturers have for the most part been moving away from the low-cost OEM board market. The major exceptions are, of course, Data General and DEC, both of which have in-house semiconductor facilities that permit manufacture of proprietary CPU chips and necessary peripherals. The small minicomputer firms have elected to move closer to the end-user market with new system level products for both distributed processing and small business applications.

A listing of microcomputer suppliers and their addresses appears in Appendix B.6.1.

Products

Microcomputer products take a variety of forms; however, product structure is built around board- and system-level products. In most cases, they represent two levels of integration by the same supplier. For example, the Intel SBC 80/10 board-level CPU is combined with a chassis, power supply, and front panel to implement the System 80/10. For most suppliers, the product listing is a "hardware store" full of various boards for CPU, RAM, PROM, A/D and D/A converters, interfaces, interrupt controllers, and I/O controllers. They are used in various combinations according to the needs of the specific application. The customer may elect to provide the card cage, power supply, and cabling, or can delve further into the supplier's catalog and buy each part he needs to integrate the computer into his end product at the proper level.

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Both board- and system-level products look very much like the OEM products sold for a number of years by the minicomputer suppliers; however, the prices are much lower and the performance correspondingly less. The vast majority of products are 8-bit processors utilizing one of the popular LSI CPU devices such as the Intel 8080, Motorola 6800, MOS Technology 6502, or Zilog Z80. Much software support associated with the minicomputer market is becoming available for the microcomputers. High-level languages, various types of assemblers, disc operating systems, file management, word processing, and other utility programs are currently available from either the processor supplier or one of the many "micro" software houses that have sprung up around the country.

The specific board-level products offered are largely a function of the availability of LSI CPU devices and have bus characteristics and system architectures that are dictated by the CPU devices. A typical system might consist of a CPU board, which contains the CPU, control ROM, and a limited amount of RAM.. A second board would handle I/O functions; additional ROM and RAM would be on additional boards. Thus, while a CPU board may sell in quantity for under $300, the total price for a system to solve a specific problem generally runs between $700 and $1,500. In process control and machine tool applications, where large numbers of complex I/O ports or A/D converters are required, a set of boards can run as high as $3,000, even in reasonably large quantities.

System-level products are currently dominated by the products sold by the original hobby-oriented manufacturers. A minimal system with CPU, memory, peripheral interface, and power supplies is priced at about $700 in kit form and close to $1,000 assembled. A number of additional boards and accessories must be added to the basic system in order to solve a specific problem for the user. As system-level products are generally used in more memory-intensive applications, the cost of an assembled system without the peripherals can run $2,000 to $5,000 in small quantities.

An important product trend that has emerged is second sourcing of popular microcomputers. National Semiconductor has introduced a second source board for the Intel 80/10 and 80/20 Series of 8-bit CPU boards, starting what could be a trend toward second sourcing at the board level. This is an example of the "component mentality" being extended into the microcomputer board and system markets. As system architecture and bus designs become further standardized due to the widespread use of present and future Intel and Intel-compatible chips, this trend should accelerate.

Another product trend of interest is that of board size and bus specification standards. Since most microcomputers need a number of interface boards which may not be available from the CPU manufacturer, it is essential to the growth of the market that standardization of board sizes and bus specifications becomes a reality. A number of de facto standards have been adopted, primarily due to the marketing strength of the firms originating them. The first such standard was the S100 bus developed by MITS for the early hobby computers. This bus is in wide use today and a preliminary IEEE standard has been released for this popular bus. The Intel SBC bus has been adopted by a number of suppliers that offer bus-compatible CPU, memory, and interface boards. The DEC LSI-11 has established another standard, particularly for memory and interface boards. A number of suppliers such as Heath, Mostek, Motorola, PCS, Prolog, TI, and Zilog have elected to use proprietary bus designs; as the popularity of each manufacturer's product grows, a number of compatible products may be introduced.

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Distribution and Marketing

At the present time, each of the three groups of market suppliers has a different approach to the market and decidedly different marketing and distribution channels. The minicomputer suppliers view the microcomputers as a downward extension of the minicomputer product and technology with lower prices that open up new levels of users. The hobby-oriented suppliers have developed mail order and retail stores as their primary distribution methods. Initially, there was only mail order distribution of computers to the hobby market, but as the popularity of the computer hobby spread, retail stores sprang up to serve local markets for both hardware and software products. The semiconductor suppliers are using the traditional component OEM sales force and the network of distributors to sell chips, boards, and systems. All three levels of products are treated as different forms of the same component and offered to the customer as viable alternatives, depending upon the needs of the customer and his applications.

The semiconductor suppliers and their distributors command a much larger customer base and a greater number of outlets than do the other two types of microcomputer suppliers. Although the minicomputer suppliers are starting to use dealers for distribution of small OEM computers and OEM peripherals, their sales are primarily through system-oriented direct sales forces.

The retail outlets are the really new innovation in computer marketing. At the present time, there are approximately 750 retail stores worldwide selling computers, kits, and associated peripherals and software. Both MITS and IMSAI have established franchised stores, while some independent chains of associated stores such as Byte Shops and Computer Mart handle several manufacturers' equipment. Byte Shops are the largest independent chain, with over 70 stores worldwide. Of the franchised stores under the control of equipment manufacturers, the MITS Computer Stores, Inc., are the largest, with over 70 stores now in operation throughout the United States.. IMSAI has also started franchised outlets under the Computer Land name, with about 50 stores operating at the present time. The retail store is an important part of the end-user marketing strategy of many microcomputer manufacturers, because it is expected to allow entry into the very small business computer market.

Another important distribution trend resulting from the growth and development of the microcomputer market is the entry of the electronics distributors into the OEM equipment markets. Several large distributors (such as Hamilton/Avnet) are starting major efforts to market the OEM board and system products of their semiconductor principals and are moving into peripherals as well. The distributor appears to be on the way to becoming the low-volume OEM computer distribution arm for the semiconductor companies as they move further into the computer market. The wide sales coverage and short delivery times associated with distributors could give the semiconductor suppliers a powerful OEM sales organization.

The minicomputer manufacturers are also developing new channels of distribution for low-volume OEM products. DEC has signed Hamilton/Avnet as a distributor, and Data General has elected to team up with the Schweber organization. Data General has been talking with the Byte Shops about selling its products in the computer stores, while DEC recently opened its own computer store, presumably the first of a nationwide chain. General Automation is selling through the Tandy computer catalog and the single existing Tandy Computer Store.

The entire distribution problem of selling relatively small quantities of OEM hardware to a wide range of new customers is prompting

the microcomputer manufacturers to explore new types of distribution, such as electronics distributors and retail stores. DEC has also experimented with mail order as a way of reaching small customers on an economical basis. This extension of distribution channels is expected to continue for several more years as the manufacturers experiment with new and more effective ways of reaching a broad range of customers with these low-cost computer products.

THE MICROCOMPUTER MARKET

Market Trends

In looking at major trends, both the OEM and end-user markets must be considered. The minicomputer manufacturers are expected to evolve into sales of small packaged systems based on their microcomputers that will take advantage of their strengths in end-user marketing and maximize the sales and profit dollars on each system. The peripherals content of systems directed at small business applications will amount to four or five times the processor cost, making the end-systems market very attractive for the vertically integrated minicomputer manufacturers such as DEC and Data General. The end result would appear to be a combining of the two movements within the minicomputer industry—greater emphasis on end-user markets and systems, and further exploitation of the lower costs of CPU and memory devices in low-priced computer systems.

The specialized microcomputer manufacturers are also expected to move more towards the industrial and business markets with complete product lines and packaged systems. The uniqueness of their retail marketing outlets should allow them to open new markets for business and professional computer systems. Computer retail stores should become a major new factor in the sale, support, and maintenance of very small business-data-processing-oriented computer systems.

The semiconductor suppliers are expected to begin to dominate the OEM hardware business for both 8- and 16-bit processors due to their lower device costs and access to the latest technology. Vertical integration by the semiconductor firms is now an accomplished fact, and the final competitve battleground for all three supplier groups appears to be the packaged systems for business, industrial, and personal use. The high peripheral content of systems and the software dependency should force the semiconductor suppliers to move toward integration beyond boards and systems in order to be able to offer competitive products incorporating CRT/keyboards, floppy discs, printers, and other high-volume peripherals. New memory technologies such as charge-coupled devices (CCD) and magnetic bubble domain (MBD) will be important to the small systems market and therefore could be profitably used by the semiconductor suppliers to further their position in this market. If present trends continue, in several years the products and capabilities of the three competing groups of suppliers are expected to be very comparable, with marketing and support as major competitive factors.

The low prices of board- and systems-level microcomputers have opened up new applications, both with sophisticated and unsophisticated users. To a large extent, these board and system products are starting to be viewed as components in much the same way as microprocessor and memory chips are components. Over time, the technology permits a given amount of computer system to be assembled on fewer boards with fewer semiconductor components. The level of product integration, chips, boards, or systems for a particular application is a matter of the user's ability and economic need to utilize the computer at a particular level of complexity.

Just as with semiconductor LSI, there are

standard and custom board-level products, with the choice based on economics and overall system performance. The system-level product is generally only the packaging necessary to use the computer boards in any given application. Thus, an analogy exists between the LSI chip and its package, and the microcomputer board and its cabinet, card cage, power supply, and cables (the system). This similarity will be further discussed in the following subsection.

In general, the user of a microcomputer has the option of buying the processor and memory and input/output circuitry at either the chip, board, or system level. The semiconductor suppliers started supplying board-level products to their chip customers as an aid to system prototyping and programming. It came as a surprise to many of the chip suppliers (and industry analysts) that their customers would actually start volume production using a board- or system-level product rather than chips. This has occurred because many of the customers for microprocessors are new users of electronic components and certainly not adept at component selection and system design and programming. As a result, the board- or system-level product is a perfect solution, since it is much easier to use and apply than the microprocessor chip.

The choice of chip-, board-, or system-level computer components is a complex set of trade-offs, many of which are subjective in nature. The variables include annual quantity, end-system price, the percentage of the system that is the computer, and the sophistication of the user. For example, a manufacturer of energy management systems for small commercial buildings would, in most cases, elect to buy at the system level since the annual quantity of systems is not likely to exceed a few hundred and the computer, at $2,000, represents somewhere between 5 and 10 percent of the total system cost. Furthermore, the user has his primary expertise in energy systems management and analysis; the related software and computer are simply "components" in the overall system.

At the other extreme would be a manufacturer of intelligent terminals that is already in the electronic systems manufacturing business and has engineers expert in logic and hardware design. In addition, the number of annual units is probably well over 5,000 per year, and the processor and memory account for up to 25 to 30 percent of the hardware cost. In this case, the decision will likely be to build the system using chip-level components and a circuit board design that is optimized for large-volume production of a relatively low-cost product.

In the middle are applications such as medical instruments, data entry systems, and data acquisition systems in which the combination of user sophistication, end-product price, and annual unit volume will lead to a decision to purchase the computer at the board level in many cases. This is particularly true where the nature of the application requires the system manufacturer to design and build one or more custom interface boards in order to integrate the computer effectively into the end product.

The choice of an 8-bit or 16-bit computer is, in general, based on the computational and throughput requirements of the system, but is also based on system expandability, vendor software support, and some subjective factors. In general, 8-bit units are used in control-oriented applications, while 16-bit machines are chosen for higher-throughput, computation-oriented systems. Among the subjective factors is the fact that many designers underestimate the amount of processing power and memory that will be required. If the cost differential is not significant, then the larger, more powerful system will be an "insurance policy" against finding halfway through the project that the processor is too small.

In general, the criteria for determining the choice of chip-, board-, or system-level pro-

ducts include overall system cost, user sophistication, and the annual units required. As a generalization, it can be stated that sophisticated users with production volumes of 5,000 to 10,000 units per year will elect to buy at the chip level. In some cases, this unit volume requirement can be as low as 1,000 units if the design and manufacturing capability are already in place. If the system is to have an annual volume of between 100 and 1,000 units per year, board-level products are generally the choice. For a few to a few hundred units per year, which usually implies that the system is large and complex and the manufacturer's expertise lies in other areas, the system-level products are generally chosen.

Price Trends

At both the board and system levels, there are factors that tend to increase the price of a typical system and those that tend to decrease it. Continued reduction in semiconductor costs should permit reduced prices on existing designs. As the complexity of the devices increases, the same capability can be assembled on fewer circuit boards, providing reduced prices for future generations of systems. On the other hand, the trend toward more memory-intensive applications and the incorporation of complex analog-to-digital preprocessing on system boards is tending to increase the prices of the systems being shipped.

Because of the expected dominance of the board-level business by the semiconductor companies, prices of systems should decline along with device price reductions and density increases. The highly competitive nature of the semiconductor market will likely be extended to the 8-bit board and system business and later to the 16-bit market.

Due to increasing memory content and the availability of a wider range of standard interface and peripheral controller boards, the average price of 8-bit boards is expected to decline at the rate of 11 percent per year through 1982, while 12- and 16-bit boards are forecasted to decline only 12 percent per year.

Prices of systems-level 8-bit machines are expected to rise slightly over the period due to the addition of large amounts of memory for business applications and the trend toward integrating floppy disc drives in the CPU. Much like semiconductor LSI, system-level microcomputer prices tend to be bounded at the low end by testing and packaging cost. The cost of power supplies, cabinets, cables, and front panels is not expected to decrease as quickly as board costs and represents a substantial percent of total system cost. The largest single cost item, the power supply, can be reduced in cost somewhat by circuit innovations, but can be affected more directly by reducing the power requirements of the LSI chips.

Worldwide Market Forecasts

The world market for microcomputer CPU products from U.S.-based suppliers is expected to grow from an estimated $118 million in 1977 to $385 million in 1982. This represents a 27 percent compound annual growth rate. This value of annual shipments is for factory level shipment of 8-bit boards, 8-bit systems (boxes) and 12/16-bit boards. These values do not include the sales of peripherals, software, or service associated with the end-use system. At the board level, the figures given include the value of all types of boards (CPU, memory, interface, etc.) sold by U.S.-based suppliers of microcomputer CPU products. The values do not include sales by board manufacturers that do not offer a CPU product. In the case of 8-bit boxes, the sales figures include the value of those floppy disc drives offered as an integral part of some CPUs. Desktop computers that include keyboard, display, processor, memory, and printer in a single unit are not included in this analysis.

6.1 Microcomputers

Unit shipments of standard microcomputer products are expected to increase from 89,000 units in 1977 to 508,000 units by 1982. Complete forecasts for units and dollars in the 1977 to 1982 period are given in Tables 6.1-1 and 6.1-2. Market shares by product type are given in Tables 6.1-3 and 6.1-4.

The 8-Bit Board Market

The 8-bit board market comprises products directed at both the hobby and industrial control markets. The semiconductor suppliers, as well as a few firms dedicated to the control field such as Control Logic, Process Computer Systems (PCS), and Warner and Swasey, dominate the industrial segment. In the hobby-oriented segment there are a large number of suppliers that exist on a relatively small level of business conducted primarily by mail order and through computer stores.

As shown in Table 6.1-5, an estimated 32,000 8-bit boards were shipped in 1977; approximately 30 percent of the units went to the hobbyist/experimenter. We believe that the real growth in this product segment is not in the hobby market, however, but in the myriad of industrial and commercial applications that are open to low-cost "component" computers. By 1982, the annual shipments are expected to reach 300,000 units per year, a 54 percent average annual growth rate. During this same time, the dollar volume is expected to grow from $32 million to $150 million for a 36 percent annual growth rate.

The prices and functions of the 8-bit boards can be expected to follow that of semiconductors, in terms of more powerful CPU products, and also in terms of simpler, lower-cost processor boards. To a limited extent, the rapid unit growth can be attributed to the use of multiple CPUs in more complex industrial control applications. This implies that the number of systems utilizing 8-bit boards will be somewhat less than the number of board shipments forecasted.

The 8-Bit System Market

Until recently, the 8-bit system market was primarily for kits directed at the hobbyist/experimenter. This market provided a good vehicle for a number of new firms to become well established in the small computer field. Among the more notable examples are Cromemco, IMSAI, and MITS. These companies provide systems based on the 8080 and 2-80 chips and have evolved into reliable, well-documented products with a growing list of industrial and business users.

Over the forecast period the average system price for 8-bit system-level products is actually expected to increase as the transition is made from primarily a kit market to primarily an assembled system market and some manufacturers incorporate more memory and internal floppy disc drives. During 1977, an estimated 35 percent of the CPUs shipped went into the hobbyist/experimenter market. By 1982 the hobby market is expected to account for only 5 percent of the 8-bit system unit shipments. Hobbyists are increasingly tending to purchase complete personal computer systems such as those manufactured by Apple Computer and Tandy Corporation (Radio Shack). As these are dedicated products that incorporate CPU, keyboard, display, etc., in a single cabinet, they are not included in this section but are treated separately in Section 6.3.

As shown in Table 6.1-6, during 1977 an estimated 32,000 processors were shipped by U.S. manufacturers. This figure is forecasted to grow to 78,000 units with a market value of $145 million by 1982. Toward the end of the forecast period, the upper-end products will likely find strong competition from low-cost 16-bit systems in a number of major applications such as small business computers and industrial

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Table 6.1-1
ESTIMATED WORLDWIDE MARKET FOR MICROCOMPUTERS
(Thousands of Units)

	1976	1977	1978	1979	1980	1981	1982	Compound Annual Growth Rate 1977 - 1982
8-bit Boards	17	35	70	120	180	240	300	53.7%
8-bit Systems	14	32	47	60	70	75	78	19.5%
12-bit and 16-bit Boards	10	22	45	65	85	110	130	42.7%
Total	41	89	162	245	335	425	508	41.7%

Source: DATAQUEST, Inc.

Table 6.1-2
ESTIMATED WORLDWIDE MARKET FOR MICROCOMPUTERS
(Millions of Dollars)

	1976	1977	1978	1979	1980	1981	1982	Compound Annual Growth Rate 1977 - 1982
8-bit Boards	$17	$ 32	$ 60	$ 95	$130	$145	$150	36.2%
8-bit Systems	18	57	105	140	155	150	145	20.5%
12-bit and 16-bit Boards	14	29	45	65	75	85	90	25.4%
Total	$49	$118	$210	$300	$360	$380	$385	26.7%

Source: DATAQUEST, Inc.

6.1 Microcomputers

Table 6.1-3
ESTIMATED SHARE OF MARKET
BY MICROCOMPUTER PRODUCT TYPE
(Percent of Units)

	1976	1977	1978	1979
8-bit Boards	41%	39%	43%	49%
8-bit Systems	34	36	29	25
12-bit and 16-bit Boards	25	25	28	26
Total	100%	100%	100%	100%

Source: DATAQUEST, Inc.

Table 6.1-4
ESTIMATED SHARE OF MARKET
BY MICROCOMPUTER PRODUCT TYPE
(Percent of Value)

	1976	1977	1978	1979
8-bit Boards	35%	27%	29%	32%
8-bit Systems	37	48	50	47
12-bit and 16-bit Boards	28	25	21	22
Total	100%	100%	100%	100%

Source: DATAQUEST, Inc.

control, which will tend to reduce the dollar growth rate. The increased shipments of lower performance, lower-priced systems will likely keep the shipments growing. Average prices are expected to decline in the 1979 to 1982 period due to the competition with 16-bit machines and the resultant shift in the product mix to lower-priced systems.

The 12-Bit and 16-Bit Board Market

During 1977, virtually all of the 16-bit board products were being supplied by minicomputer manufacturers. One exception is the PACE board being supplied by National Semiconductor. The minicomputer-derived boards represent downward extensions of well-established product lines of manufacturers such as Data General, DEC, and General Automation. The TI 16-bit board, which is based on the TMS9900 processor chip, is offered as the 990/100 for OEM use. The TI board serves as the basis for the 990/10 and 990/20 minicomputers, just as the DEC LSI-11 serves as the processor board in the PDP-11/03. In the cases of Data General, DEC, and TI, the MOS/LSI processor chips are made in an in-house semiconductor facility.

In late 1978, Intel is expected to make available a series of OEM board and box products based on the new 8086 16-bit CPU chip. Both Data General and DEC have introduced new versions of their board-level microcomputers apparently in response to market experience and the expected competition from Fairchild, Intel, TI, and Zilog.

Due to lower semiconductor costs and a better ability to market processor components, the semiconductor suppliers could move into a strong position in this market. With a large base of customers who are using 8-bit boards, if the semiconductor firms can meet the upward-compatible processor needs of their customers, they could generate a large-volume market for

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Table 6.1-5
ESTIMATED WORLDWIDE MARKET FOR
8-BIT BOARD-LEVEL MICROCOMPUTERS

	1976	1977	1978	1979	1980	1981	1982	Compound Annual Growth Rate 1977 - 1982
Thousands of Annual Units	17	35	70	120	180	240	300	53.7%
Average System Price (Thousands of Dollars)	$ 1.0	$ 0.9	$ 0.9	$ 0.8	$ 0.7	$ 0.6	$ 0.5	(11.4%)
Millions of Dollars	$17	$32	$60	$95	$130	$145	$150	36.2%

Source: DATAQUEST, Inc.

Table 6.1-6
ESTIMATED WORLDWIDE MARKET FOR
8-BIT SYSTEM-LEVEL MICROCOMPUTERS

	1976	1977	1978	1979	1980	1981	1982	Compound Annual Growth Rate 1977 - 1982
Thousands of Annual Units	14	32	47	60	70	75	78	19.5%
Average System Price (Thousands of Dollars)	$ 1.3	$ 1.8	$ 2.2	$ 2.3	$ 2.2	$ 2.0	$ 1.9	0.9%
Millions of Dollars	$18	$57	$105	$140	$155	$150	$145	20.5%

Source: DATAQUEST, Inc.

16-bit boards. Some of this growth will be at the expense of upper-end 8-bit products; however, the 8-bit processors will be mature at both board level and chip level by 1980 and this inherent competition will have little effect on overall sales revenues.

As shown in Table 6.1-7, the 1977 16-bit board market is estimated to have been 22,000 units with a market value of $29 million. By 1982, unit shipments are expected to reach 130,000 units with a value of $90 million. This represents a 43 percent growth rate in units and a 25 percent growth rate in dollar value.

During the forecast period, the minicomputer manufacturers will likely use their 16-bit board-level products increasingly in system products and evolve into some multiprocessor applications. The specialized microcomputer suppliers, such as IMSAI and MITS, are expected to introduce 16-bit CPU chips in order to offer a higher level of performance in their industrial and business system products.

International Markets

During 1977, an estimated 65 percent of the microcomputer shipments were to customers in North America. By 1982 this is expected to shift to a 50 percent shipment rate, with Japan taking 10 percent, Europe, 30 percent, and the Balance of the World, 10 percent. The foreign markets for board-level products are expected to account for a smaller portion of total U.S. output than one might otherwise expect. The major contributed value is in assembly of the board; thus, shipment of semiconductor chips will be a better alternative for many users. The chips would be assembled in the foreign country into boards and systems.

Table 6.1-8 gives estimated regional market shares for all microcomputers.

Table 6.1-7
ESTIMATED WORLDWIDE MARKET FOR
12-BIT AND 16-BIT BOARD-LEVEL MICROCOMPUTERS

	1976	1977	1978	1979	1980	1981	1982	Compound Annual Growth Rate 1977 - 1982
Thousands of Annual Units	10	22	45	65	85	110	130	42.5%
Average System Price (Thousands of Dollars)	$ 1.4	$ 1.3	$ 1.0	$ 1.0	$ 0.9	$ 0.8	$ 0.7	(12.1%)
Millions of Dollars	$14	$29	$45	$65	$75	$ 85	$ 90	25.4%

Source: DATAQUEST, Inc.

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Table 6.1-8
ESTIMATED REGIONAL DISTRIBUTION OF MICROCOMPUTER REVENUES
(Percent)

Region	1976	1977	1982
North America	85%	65%	50%
Japan	5	7	10
Europe	10	25	30
ROW	NIL	3	10
Total	100%	100%	100%

Source: DATAQUEST, Inc.

Market Size by DATAQUEST Performance Class

Tables 6.1-9 and 6.1-10 present the microcomputer market in units and dollars segmented according to DATAQUEST's processor classes. Class I includes products based on MOS 8-bit processor chips. Class II includes all 12-bit processors and the slower 16-bit machines. Class III comprises the low-end minicomputer-derived products such as the LSI-11 and the microNOVA. As a group, the Class II processors form a very small market, most of which is based on systems that emulate the PDP-8. The rapidly falling costs of 16-bit products will probably leave little room for Class II products, except in cases where a software investment in PDP-8 programs justifies using a Class II processor.

Applications

At the present time, Class I boards and systems are used primarily in hobby and industrial control applications. An estimated 30 percent of Class I boards and 35 percent of Class I systems are sold to experimenters/hobbyists. We estimate that by 1982 only 5 percent of the units will be for hobby applications. Tables 6.1-11 through 6.1-14 show our estimates for Class I board and system products.

Class II products find very little usage outside of the industrial control and laboratory automation areas. In the future, the availability of low-cost Class III boards should restrict the growth of the Class II market. Tables 6.1-15 and 6.1-16 show the estimated market for Class II boards by application.

Class III boards tend to follow more closely the distribution of Class II minicomputers in their applications. The higher performance and greater software support permit their use in more EDP-oriented applications and in communications-related systems. Tables 6.1-17 and 6.1-18 show the estimated application distribution for Class III boards.

Major Growth Areas

From an application standpoint, we anticipate that the board-level products will continue to find their major applications in the industrial control, laboratory automation, and specialized data acquisition and control application areas.

During the forecast period, the use of system-level products in business applications should see dramatic growth. The reduction in sales to the hobby segment will be more than offset by the rapid growth in systems directed at the business end-user market. The growth rate of the dollar market in the 1977 to 1979 time period should be accelerated by the changeover from kits to preassembled systems, with correspondingly higher average prices per system. The figures do not include the dollar value of peripherals such as discs and printers, which will be greater with the system-level products than with board-level products.

The rapid growth anticipated for the 16-bit

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Table 6.1-9
ESTIMATED WORLDWIDE MICROCOMPUTER MARKET
BY DATAQUEST PERFORMANCE CLASS
(Thousands of Units)

	1976	1977	1979	1982	Compound Annual Growth Rate 1977 - 1982
Class I Boards	17	35	120	300	53.7%
Class I Systems	14	32	60	78	19.5%
Class II Boards	2	2	5	7	28.5%
Class III Boards	8	20	60	123	43.8%
Total	41	89	245	508	41.7%

Source: DATAQUEST, Inc.

Table 6.1-10
ESTIMATED WORLDWIDE MICROCOMPUTER MARKET
BY DATAQUEST PERFORMANCE CLASS
(Millions of Dollars)

	1976	1977	1979	1982	Compound Annual Growth Rate 1977 - 1982
Class I Boards	$17	$ 32	$ 95	$150	36.2%
Class I Systems	18	57	140	145	20.5%
Class II Boards	2	2	5	6	24.6%
Class III Boards	12	27	60	84	25.5%
Total	$49	$118	$300	$385	26.7%

Source: DATAQUEST, Inc.

Table 6.1-11
ESTIMATED WORLDWIDE CLASS I BOARD-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Units)

	1976	1977	1979	1982
Business Data Processing	—	1%	2%	3%
Communications	2%	3	6	10
Design & Drafting	—	—	1	2
EDP Support	3	3	2	1
Industrial Automation	25	33	35	32
Instructional	5	5	6	7
Laboratory and Computational	10	12	13	15
Specialized Data Acquisition and Control	10	12	13	15
Specialized Data and Word	—	1	2	5
Other (Including Hobby)	45	30	20	10
Total	100%	100%	100%	100%
Annual Unit Shipments (Thousands)	17	35	120	300

Source: DATAQUEST, Inc.

board-level market should provide opportunities for many suppliers; however, we believe it will be dominated by the semiconductor suppliers like the 8-bit board market. We expect the 16-bit boards will find major applications in communications, EDP support, industrial automation, and systems for laboratory automation and data acquisition and control.

The Microcomputer Peripherals Market

The sales of microcomputer systems should "drag" a significant amount of peripheral sales into the market. We anticipate that products such as small printers, floppy disc drives, tape cassette drives, CRT displays, keyboards, hard disc drives, and other, more specialized, I/O peripherals will be the primary products sold with microcomputer systems.

As business-oriented applications become more important in the 1979 to 1982 period, the average peripherals content of microcomputer systems will increase sharply. The average peripherals value at the OEM level was estimated to be $1,400 per system in 1977; this figure is expected to increase to $4,000 per system by 1982. During this same period the value of peripherals is expected to increase from 44 percent of OEM microcomputer system sales to 68 percent (See Table 6.1-19).

The business-oriented systems will increasingly be using faster printers, more disc storage,

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Table 6.1-12
ESTIMATED WORLDWIDE CLASS I BOARD-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Value)

	1976	1977	1979	1982
Business Data Processing	–	2%	3%	4%
Communications	2%	3	6	10
Design & Drafting	–	–	1	2
EDP Support	3	3	2	1
Industrial Automation	35	32	25	23
Instructional	5	4	5	6
Laboratory and Computational	10	15	18	20
Specialized Data Acquisition and Control	15	15	18	20
Specialized Data and Word	–	1	2	5
Other (Including Hobby)	30	25	20	10
Total	100%	100%	100%	100%
Annual Revenues (Millions of Dollars)	$ 17	$ 32	$ 95	$150

Source: DATAQUEST, Inc.

and more operator stations. This reflects the trend towards multiple operator stations systems for business and scientific use. During this time, CPU prices are expected to increase slightly, relfecting greater memory capacity and higher performance. It should be noted that this analysis applies only to Class I microcomputer systems. The Class II and Class III systems are covered elesewhere in the Minicomputer Industry Service.

Peripherals for use with Class I systems are expected to become increasingly intelligent with disc drives, printers, terminals, and memory subsystems containing microprocessors equal in power to that in the CPU, which will result in a form of distributed processing architecture for the resulting systems. This will allow the CPU prices to remain relatively stable. It is expected that the CPU boxes will begin to incorporate multiple processors as a way of increasing throughput and providing efficient processors for business applications.

MICROCOMPUTER TECHNOLOGY

Standards

Due to the commonality of the 8080 instruction set and chips to many of the 8-bit microcomputers, this architecture and software forms a de facto industry standard. In terms of

Table 6.1-13
ESTIMATED WORLDWIDE CLASS I SYSTEM-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Units)

	1976	1977	1979	1982
Business Data Processing	5%	20%	30%	40%
Communications	–	2	5	7
Design & Drafting	–	–	–	–
EDP Support	–	–	–	–
Industrial Automation	15	18	15	10
Instructional	–	5	7	10
Laboratory and Computational	10	10	10	10
Specialized Data Acquisition and Control	5	8	10	13
Specialized Data and Word	–	2	3	5
Other (Including Hobby)	65	35	20	5
Total	100%	100%	100%	100%
Annual Unit Shipments (Thousands)	14	32	60	78

Source: DATAQUEST, Inc.

interfacing at the bus level, two standards have evolved—the S100 bus originated by MITS for the hobby market, and the Intel SBC bus introduced with that company's line of products. These bus configurations have the same universality in the 8-bit world that the DEC Unibus and Data General Nova bus have in the 16-bit minicomputers. This standardization at the 8-bit level, with bus configurations that are essentially "public domain," makes possible a large number of memory and interface boards for use with the available CPUs. The CPU board suppliers such as Intel are encouraging suppliers to enter this market, since it broadens the range of applications available to the CPU products. This has happened to some extent at the 16-bit level with, for example, the products introduced for use with the DEC LSI-11. The LSI-11 bus is not a Unibus, but by virtue of its use in the popular board-level computer, it is a de facto standard for 16-bit microcomputers. It is to be expected, however, that upward extensions of the S100 and SBC bus will also provide a widely accepted standard for future 16-bit machines. Bus standards are far less important in business applications and with large OEM users.

Semiconductor LSI

Microcomputer performance and prices are driven primarily by semiconductor LSI technol-

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Table 6.1-14

ESTIMATED WORLDWIDE CLASS I SYSTEM-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Value)

	1976	1977	1979	1982
Business Data Processing	7%	22%	35%	45%
Communications	–	2	5	7
Design & Drafting	–	–	–	–
EDP Support	–	–	–	–
Industrial Automation	20	16	10	5
Instructional	–	5	7	10
Laboratory and Computational	12	10	10	10
Specialized Data Acquisition and Control	6	8	10	13
Specialized Data and Word	–	2	3	5
Other (Including Hobby)	55	35	20	5
Total	100%	100%	100%	100%
Annual Revenues (Millions of Dollars)	$18	$57	$140	$145

Source: DATAQUEST, Inc.

ogy. Since costs are a function of the number of boards required to build a system and the number of components per board, the costs of the microcomputers can be expected to continue to decline with increasing levels of semiconductor integration. However, advances in LSI technology are expected to provide greater system performance on the order of larger memory and more peripheral controllers on the chip. The expected result is that the average price for both board- and system-level systems will not decline as rapidly as semiconductor device costs.

The economics of the LSI technology made the 4-bit general-purpose microprocessor replaceable by a more powerful 8-bit system at only a nominal increase in cost; the prices of 8-bit and 16-bit CPU devices can also be expected to converge. During the forecast period, we expect LSI technology—either MOS or bipolar—to be capable of placing a 16-bit processor, writable control store, ROM, and an effective cache memory on a single chip. Such devices, when coupled with a hierarchy of solid state memory products and processor-based interface controllers, will provide extremely powerful single-board computers that can be used in single or multiple processor systems. High-level language operation of the processor is expected to be readily available by selecting a companion interpreter chip. Special languages for control and communications applications also should be available in ROM.

Table 6.1-15

ESTIMATED WORLDWIDE CLASS II BOARD-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Units)

	1976	1977	1979	1982
Business Data Processing	5%	5%	6%	7%
Communications	10	10	7	5
Design & Drafting	–	–	–	–
EDP Support	–	–	–	–
Industrial Automation	50	50	50	48
Instructional	–	–	–	–
Laboratory and Computational	20	20	20	20
Specialized Data Acquisition and Control	15	15	17	20
Specialized Data and Word	–	–	–	–
Other (Including Hobby)	–	–	–	–
Total	100%	100%	100%	100%
Annual Unit Shipments (Thousands)	2	2	5	7

Source: DATAQUEST, Inc.

Table 6.1-16

ESTIMATED WORLDWIDE CLASS II BOARD-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Value)

	1976	1977	1979	1982
Business Data Processing	6%	6%	8%	10%
Communications	10	10	7	5
Design & Drafting	–	–	–	–
EDP Support	–	–	–	–
Industrial Automation	49	49	48	45
Instructional	–	–	–	–
Laboratory and Computational	20	20	20	20
Specialized Data Acquisition and Control	15	15	17	20
Specialized Data and Word	–	–	–	–
Other (Including Hobby)	–	–	–	–
Total	100%	100%	100%	100%
Annual Revenues (Millions of Dollars)	$ 2	$ 2	$ 5	$ 6

Source: DATAQUEST, Inc.

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Table 6.1-17

ESTIMATED WORLDWIDE CLASS III BOARD-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Units)

	1976	1977	1979	1982
Business Data Processing	5%	7%	9%	10%
Communications	15	12	10	5
Design & Drafting	2	3	3	4
EDP Support	10	10	12	15
Industrial Automation	25	28	27	26
Instructional	3	5	6	7
Laboratory and Computational	20	15	12	10
Specialized Data Acquisition and Control	10	10	12	15
Specialized Data and Word	5	5	5	5
Other (Including Hobby)	5	5	4	3
Total	100%	100%	100%	100%
Annual Unit Shipments (Thousands)	8	20	60	123

Source: DATAQUEST, Inc.

Table 6.1-18

ESTIMATED WORLDWIDE CLASS III BOARD-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Value)

	1976	1977	1979	1982
Business Data Processing	8%	10%	16%	16%
Communications	10	12	10	5
Design & Drafting	2	3	3	4
EDP Support	10	10	12	15
Industrial Automation	27	25	20	20
Instructional	3	5	6	7
Laboratory and Computational	20	15	12	10
Specialized Data Acquisition and Control	8	10	12	15
Specialized Data and Word	7	5	5	5
Other (Including Hobby)	5	5	4	3
Total	100%	100%	100%	100%
Annual Revenues (Millions of Dollars)	$ 12	$ 27	$ 60	$ 84

Source: DATAQUEST, Inc.

6.1 Microcomputers

Table 6.1-19
PERIPHERALS CONTENT OF CLASS I MICROCOMPUTER SYSTEMS
(Millions of Dollars at OEM Level)

	1977	1979	1982	Compound Annual Growth Rate 1977 - 1982
Class I CPUs	$ 57	$140	$145	20.5%
Peripherals				
Business Systems	$ 20	$ 72	$220	61.5%
Hobby Systems	10	11	3	(21.4%)
Other	15	45	81	42.1%
Subtotal	$ 45	$128	$310	47.1%
Total Class I Systems	$102	$268	$455	34.9%
Peripherals Share	44%	48%	68%	9.1%

Source: DATAQUEST, Inc.

By the end of 1979, it is expected that 32-bit microprocessor chips will have been announced by at least one vendor. Thus, it is likely that 32-bit board level products will become available in 1980 or 1981 and a significant market could develop by the end of the forecast period. However, without definitive information on the nature of the product and the competitive environment in the 32-bit area, DATAQUEST is reluctant to attempt a specific forecast at the present time.

Microcomputer Hardware

No major changes in microcomputer hardware are anticipated during the forecast period. The assembly of semiconductor chips on circuit boards is a manual operation for all but the largest of manufacturers. The trend toward fewer packages per computer works to defeat the cost justification of automatic assembly. Innovations in semiconductor packaging will be required in order to place devices of greater complexity and heat dissipation in plastic packages. It is expected that 48-, 64-, and 100-pin packages will be in widespread use by 1981. For high-volume systems, specialized input/output devices can be expected to reduce chip and board count and make the system easier to use.

6.1 Microcomputers

Microcomputer Software and Support

As the prices of chips, boards, and boxes continue to fall, the economic limitations on the expansion to new applications are continually being removed. The major cost to the user and the seller of the microcomputer system is expected to be software and support. In this regard, a number of technology-related trends appear to be emerging.

The first is a trend toward the sale of major software products in the form of "firmware" included on the processor board. High-level language compilers and interpreters, communications protocols, I/O device drivers, and other software products that lend themselves to standardization are expected to be sold in "chip" form. The semiconductor ROM could become a major medium for the packaging and sale of selected standard software products.

The second major trend is toward the use of packaged software development systems as expanded system design and documentation centers. The limitation on new applications imposed by the lack of machine-level programmers and systems analysts should be greatly alleviated by the increasing sophistication of "system development" systems. These interactive design and programming systems will provide the unsophisticated user with the "hand-holding," system interaction, and understanding that should enable many new applications to be generated without the great overhead support expense normally associated with the sale and use of products of this complexity. In effect, the customer will be buying a packaged applications specialist in a $5,000 to $10,000 desktop computer. The system would also handle software documentation. The evolution of current program development systems into products of this type is a natural upgrading of existing products. The technology permits, and even enhances, the "component computer" marketing approach, that is expected to characterize the strong position of the semiconductor suppliers in this market.

MICROCOMPUTER PRODUCTS

Table 6.1-20 lists the leading 8-bit board products and their major characteristics. Table 6.1-21 gives similar information for 8-bit systems. Table 6.1-22 lists the leading 12-bit and 16-bit board-level microcomputers.

MICROCOMPUTER COMPETITION

Competitive Environment

The emerging microcomputer market is highly competitive within a given supplier or application segment. However, the three groups of suppliers—the semiconductor suppliers, the specialized microcomputer manufacturers, and the minicomputer suppliers—all currently have different customer bases and marketing approaches. As a result, competition for a given customer is somewhat limited at this time. This is expected to change, however, as the semiconductor suppliers expand their product lines, support, and market objectives.

DATAQUEST believes that over the long term the semiconductor suppliers will dominate the OEM board market for Class I, II, and III products. This will force the minicomputer and microcomputer suppliers to move farther into end-user markets and offer packaged systems including peripherals and applications software. National Semiconductor, with its position in the large CPU and memory end markets, has chosen to participate only at the OEM level, leaving end-user sales and service to the OEM customer. Intel is building an end-user sales force in the IBM add-on memory division that could, in the future, be used to market computer systems into the IBM environment.

The greatest product limitation on any

Table 6.1-20
LEADING 8-BIT BOARD-LEVEL MICROCOMPUTER PRODUCTS

Supplier	Model	Microprocessor Used	DATAQUEST Performance Class
Advanced Micro Computers	80 - 10	8080	I
Apple Computer	Apple I	6502	I
	Apple II	6502	I
Applied Data Communications	Series 70 - 100	8080A	I
Control Logic	L-Series	8008	I
	M-Series	8080A	I
	MM1	8080A	I
	CCS-1025	8080	I
Cromemco	ZPU	Z80	I
Data Numerics	DL-8A	8080A	I
Digital Equipment Corp.	MPS	8008	I
Digital Group, The	Z80-CPU	Z80	I
	8080-CPU	8080	I
	6800-CPU	6800	I
	6502-CPU	6502	I
Fairchild	F-8 One Card Microcomputer	F-8	I
Gnat	Gnat 8080	8080	I
IMSAI	MPU A	8080	I
	MPU B	8085	I
Intel	SBC 80/10	8080A	I
	SBC 80/20	8080A	I
	SBC 85/10	8085	I
Martin Research	AT471-3	8008-1	I
	AT441-5	8080A	I

(Continued on following page)

Table 6.1-20 (Continued)
LEADING 8-BIT BOARD-LEVEL MICROCOMPUTER PRODUCTS

Supplier	Model	Microprocessor Used	DATAQUEST Performance Class
MITS/Pertec	Altair 680b	6800	I
	Altair 8800a	8080A	I
	Altair 8800b	8080A	I
Monolithic Systems	MSC Z80	Z80	I
Mostek	SD Series	Z80	I
Motorola	Microcomputer I	6800	I
	Microcomputer 1A	6800	I
Mycro-Tek	MT 8080PB	8080	I
National Semiconductor	ISP-8C	SC/MP	I
	BLC-8010	8080A	I
Polymorphic Systems	Poly 88 CPU	8080	I
Process Computer Systems	PCS 1806	8080A	I
	CM 4400	8080	I
Process Technology Corp.	SOL-PC	8080	I
Pro-Log	PLS-881	8080A	I
	8811A	8080A	I
	8821	8080A	I
	PLS-881	8080A	I
	8111	8008	I
	8611	6800	I
		9002	I
		900C	I
Synertek Systems	Jolt CP 100	6502	I
	KIM	6502	I
Systems Integration Associates	SIA-3000	8080	I
Warner & Swasey	M-8A	Discrete	I
Wintek Corp.	Wince	6800	I
Xitan, Inc.	ZPU	Z80	I
Zilog	Z80-MCB	Z80	I

Source: DATAQUEST, Inc.

6.1 Microcomputers

Table 6.1-21

LEADING 8-BIT SYSTEM-LEVEL MICROCOMPUTER PRODUCT CHARACTERISTICS

Supplier	Model	Microprocessor Used	DATAQUEST Performance Class
Astral Computer Company	Astral 2000	6800	I
Cromemco	Z-2	Z80	I
	Z-3	Z80	I
Digital Electronics	DE 68	6800	I
Digital Group, The	System 1 System	Z80	I
ECD Corp.	7X	6512A	I
Electronic Product Associates	Micro-68	6800	I
Gnat	Gnat 8080	8080	I
IMSAI	I-8080	8080	I
	I-8048	8048	I
Intel	System 80/10	8080A	I
	System 80/20	8080A	I
MITS/Pertec	8800	8080	I
	6800	6800	I
Monolithic Systems, Inc.	Z80 +	Z80	I
Multisonics	808A	8080	I
Northstar Computer	Horizon	Z80	I
Ohio Scientific Instruments	Challenger 65	6500	I
	Challenger 68	6800	I
Polymorphic Systems	Poly 88/System 16	8080	I
	8810/8813	8080	I
Process Computer Systems	MicroPac 80/A	8080A	I
	SuperPac 180	8080A	I
	MicroPac 180	8080A	I
Processor Technology	SOL	8080	I
Sphere Corp.	300 Series	6800	I
Vector Graphics	Vector 1	Z80	I
Veras Systems	F-8	F-8	I
Wave Mate	Jupiter II - CPU-125A	6800	I
Xitan, Inc.	Alpha	Z80	I
Zilog	Z80-MCS	Z80	I

Source: DATAQUEST, Inc.

Table 6.1-22
LEADING 12-BIT AND 16-BIT LEVEL BOARD PRODUCT CHARACTERISTICS

Supplier	Model	Microprocessor Used	Word Length	DATAQUEST Performance Class
Computer Automation	LSI-3105	Discrete	16	II
	Naked Mini LSI/2	Discrete	16	III
	Naked Mini 4	Custom	16	III
Data General	microNOVA Board	microNOVA	16	III
Digital Equipment Corp.	PDP-8/A	Discrete	12	II
	LSI-11	LSI-11	16	III
Fairchild	Flame	9440	16	III
General Automation, Inc.	GA-16/110	Custom	16	III
	GA-16/220	Custom	16	III
Intel	SBC 86	8086	16	III
Interdata	5/16	2900 AMD	16	III
Intersil	Intercept	IN6100	12	II
National Semiconductor	1PC-16C	PACE	16	III
	IMP-16L	IMP-16	16	III
	IMP-16P	IMP-16	16	III
Texas Instruments	990/100	TMS 9900	16	III
	990/180	TMS 9980	16	III

Source: DATAQUEST, Inc.

type of supplier attempting to enter the end-user market will be the high peripherals content and the need to have a vertically integrated operation in order to ensure lowest costs and continuity of peripherals supply. The high cost of establishing an end-user sales and support organization places the end-user market outside the reach of most small microcomputer suppliers.

Market Share

Tables 6.1-23 through 6.1-28 present market share estimates for each product segment during 1977. In the 8-bit board market, it is expected that the semiconductor suppliers such as Intel, Mostek, Motorola, National, and Zilog, will move into positions of market dominance during 1979 and 1980. A number of smaller suppliers with a dedication to the hobby market will likely survive, but they are not expected to become major factors in the market. We expect companies with specialized expertise in the industrial control market, such as PCS and Control Logic, to continue to grow, but to be limited by their marketing resources in comparison with semiconductor suppliers having large sales forces and distributor networks.

Although MITS and IMSAI are expected to continue to hold major market shares in the 8-bit system market, Intel, Zilog, and National are expected to make strong inroads into this market during 1979 and 1980. Because of the end-user business system orientation of MITS and IMSAI, there will probably not be a high degree of direct competition between these two groups of competitors.

We expect the 16-bit board market to continue to be dominated by DEC and the other minicomputer suppliers during 1978 and 1979. By 1980 the semiconductor suppliers are quite likely to have well-established 16-bit microprocessor product lines available in both board- and system-level products. Therefore, by 1980 the semiconductor suppliers can also be expected to have achieved a market position comparable to that held in 8-bit boards during 1977. The large customer base of 8-bit board and system users should provide a natural upgrade market for 16-bit machines.

6.1 Microcomputers

Table 6.1-23

ESTIMATED SUPPLIER UNIT SHARE OF WORLDWIDE MARKET
8-BIT BOARD-LEVEL MICROCOMPUTERS

Supplier	Units Shipped 1976	Units Shipped 1977	Share of Units 1976	Share of Units 1977
Intel	6,000	10,000	35%	29%
National	500	3,000	3	9
Pro-Log	1,000	2,000	6	6
Motorola	500	2,000	3	6
PCS	1,000	1,500	6	4
Others	8,000	16,500	47	46
Total	17,000	35,000	100%	100%

Source: DATAQUEST, Inc.

Table 6.1-24

ESTIMATED SUPPLIER VALUE SHARE OF WORLDWIDE MARKET
8-BIT BOARD-LEVEL MICROCOMPUTERS

Supplier	Value ($ Millions) 1976	Value ($ Millions) 1977	Share of Value 1976	Share of Value 1977
Intel	$ 4.8	$10.0	28%	31%
National	0.3	3.0	2	9
Motorola	0.4	2.0	2	6
Pro-Log	1.0	1.8	6	6
PCS	1.5	1.5	9	5
Others	9.0	13.7	53	43
Total	$17.0	$32.0	100%	100%

Source: DATAQUEST, Inc.

6.1 Microcomputers

Table 6.1-25

ESTIMATED SUPPLIER UNIT SHARE OF WORLDWIDE MARKET
8-BIT SYSTEMS-LEVEL MICROCOMPUTERS

Supplier	Units Shipped		Share of Units	
	1976	1977	1976	1977
IMSAI	3,000	5,000	21%	15%
MITS/Pertec	6,000	4,000	43	12
Cromemco	*	3,500	*	10
Processor Technology	*	3,000	*	9
Heath	*	3,000	*	9
Intel	500	2,500	4	7
Southwest Technical	*	2,500	*	7
Digital Group	1,000	2,000	7	6
Ohio Scientific	*	2,000	*	6
Others	3,500	6,000	25	19
Total	14,000	33,500	100%	100%

*Included in "Others."

Source: DATAQUEST, Inc.

Table 6.1-26

ESTIMATED SUPPLIER VALUE SHARE OF WORLDWIDE MARKET
8-BIT SYSTEM-LEVEL MICROCOMPUTERS

Supplier	Value ($ Millions) 1976	Value ($ Millions) 1977	Share of Value 1976	Share of Value 1977
MITS/Pertec	$ 5.4	$ 8.0	31%	14%
IMSAI	2.4	7.0	14	12
Processor Technology	*	5.0	*	9
Intel	1.3	5.0	7	9
Cromemco	*	4.5	*	8
Digital Group	1.2	3.5	7	6
Heath	*	3.0	*	5
Ohio Scientific	*	3.0	*	5
Southwest Technical	*	3.0	*	5
Others	7.2	14.5	41	27
Total	$17.5	$56.5	100%	100%

*Included in "Others."

Source: DATAQUEST, Inc.

6.1 Microcomputers

Table 6.1-27

ESTIMATED SUPPLIER UNIT SHARE OF WORLDWIDE MARKET
12-BIT AND 16-BIT BOARD-LEVEL MICROCOMPUTERS

Supplier	Units Shipped 1976	Units Shipped 1977	Share of Units 1976	Share of Units 1977
DEC	6,000	9,000	57%	41%
Data General	200	3,000	2	13
Texas Instruments	1,000	3,000	10	13
Computer Automation	1,000	2,000	10	10
Interdata	500	1,000	5	5
General Automation	500	1,000	5	5
Others	1,100	3,000	11	13
Total	10,300	22,000	100%	100%

Source: DATAQUEST, Inc.

Table 6.1-28

ESTIMATED SUPPLIER VALUE SHARE OF WORLDWIDE MARKET
12-BIT AND 16-BIT BOARD-LEVEL MICROCOMPUTERS

Supplier	Value ($ Millions) 1976	Value ($ Millions) 1977	Share of Value 1976	Share of Value 1977
DEC	$ 7.2	$12.0	61%	41%
Data General	0.2	4.5	2	16
Texas Instruments	.1.2	4.5	10	16
Computer Automation	1.0	2.4	9	8
Interdata	0.6	1.2	5	4
General Automation	0.6	1.0	5	3
Others	0.9	3.4	8	12
Total	$11.7	$29.0	100%	100%

Source: DATAQUEST, Inc.

2.8.5 Program Development Systems

INDUSTRY

Introduction

Introducing microprocessors to the circuit and logic designers of the electronics industry was initially a difficult undertaking. The concept of programmable logic was foreign to most designers; consequently, for the microprocessor to achieve its potential in the electronics industry, a number of education and design aids were introduced. In addition to seminars to introduce engineers to the concepts of microprocessors and to each manufacturer's products, it was necessary to provide a number of tools that designers could use to evaluate various devices, build prototype systems, and write programs for the systems. Furthermore, since the programs were to be stored in Programmable Read Only Memory (PROM) for use by the microprocessor, simple PROM programmers were also introduced.

The evolution of this early system evaluation and development activity has been toward a series of integrated products that enable a supplier to (1) effectively communicate the virtues of his particular processor to the design engineer; and (2) provide a degree of design automation in the writing, debugging, and modifying of microprocessor programs.

Early microprocessors were simple 4-bit units that could be readily programmed in mnemonics or machine language. As processors became more powerful and were used in applications requiring thousands of bytes of program, using high-level languages became popular. As the problems of programmer productivity, program documentation, and program maintenance became more apparent, users evolved more sophisticated system and program development aids.

With the widespread use of microprocessors and microcomputer boards by equipment designers with little or no computer background, the need for comprehensive system design and programming aids has become an important factor in market growth. A broad line of support products, including development systems, software, debugging and troubleshooting aids, and documentation, are now considered an important and integral part of any microprocessor product line.

Development systems are being extended to include capabilities for in-circuit emulation (ICE) of the processor chip and many functions formerly available only in test equipment such as logic analyzers. The new second generation development systems incorporate CRT displays, disk drives, and sophisticated software. Typical system prices range from $5,000 to more than $20,000.

Initially, the semiconductor manufacturers offered development systems as an aid to selling chips. The size and growth rate of the market for such products, however, has attracted instrument makers and a few independent suppliers of development systems. Thus, the development systems market has taken on an identity of its own, separate from the related market for microprocessor chip sets. It appears that program development aids are the beginning of a series of sophisticated, processor-based, design, test, and service aids to be offered by the semiconductor manufacturers as well as by the independent suppliers.

As a result of the hardware and software development aspects of microprocessor system development activity, development aids have evolved in two different ways. The initial products, directed at the hardware development lab environment, took the form of a ready-made breadboard that the engineer or technician could use in conjunction with his existing equipment and work methods. Thus, prototype boards or low-cost design aids priced from $200 to $3,000 comprised the early products offered by the microprocessor suppliers.

2.8.5 Program Development Systems

As the size of microprocessor-based systems increased, and as they were applied to more complex applications, software became the primary cost factor and programmers began using traditional software development tools. Initially, this took the form of simulators and cross-assemblers that could be used on commercial time-sharing or a large in-house computer. These techniques became expensive and cumbersome for large projects; as a result, users were soon building systems based on the processor being used for the end product, and providing each programmer with his own stand-alone programming station. The sophistication of the programming tools has grown to the point where the development systems of today are interactive, provide a wide range of software aids, and are very cost-effective—even at a price of $15,000 to $20,000 per station. The complexity of the program development system can now be tailored to the complexity of the processor being used and to the specific application.

A number of development aids are currently available to the microprocessor chip or board user. These are:

- *Time-sharing*—Initial use of assemblers and simulators for various devices was made available to users on the national time-sharing networks such as GE, McAuto, NCSS, and UBC. Terminals consist of Teletypes or other printing terminals. The cost of programming is approximately $20 per hour of connect time.

- *Stand-alone Development Systems*—These processor-based systems permit the user to interactively write, edit, and debug programs for microprocessors. In most cases, the input is by means of a CRT with printers available for program lisiting. Prices run from $5,000 to $15,000 depending upon sophistication and peripherals used.

- *Multi-station Development Systems*—Similar to time-sharing systems, these multi-station development systems offer a centralized processor and program library to a number of users. Systems of this type are particularly attractive to large computer system manufacturers that are designing large numbers of new systems and peripherals that incorporate a variety of microprocessors. The benefits of such a system to the user are sharing of utility programs, standardization of documentation and high level languages, and the economies of sharing dedicated computer system resources among a number of users. As yet, only limited multi-station program development systems have been introduced; however, more sophisticated systems are expected to be available in late 1978 or early 1979.

- *PROM Programmers*—This is a specialized area with Data I/O and ProLog supplying virtually all of the programmers used. These systems are priced at about $2,000 and usually contain a microprocessor for control. Some stand-alone development systems also have a provision for PROM programming—either integral or as an option.

- *Evaluation Kits*—To meet the need for a low-cost method for prospective customers to evaluate their products, chip suppliers provide kits including all necessary semiconductor devices to build a system. Products vary from very simple boards selling for $150 up to sophisticated prototyping systems with assembled and tested boards for $950.

- *System Analyzers*—These products were introduced by the test equipment suppliers as specialized tools for analysis of complex

logic circuits such as microprocessor systems. These logic analyzers permit the designer to view the interaction of program and system by displaying memory locations and register activity. They are helpful in troubleshooting systems during development and in manufacture, and can enable the designer/programmer to be more efficient in program design. Major suppliers are Biomation and Hewlett-Packard. Prices are in the $5,000 range.

- *Educational Products*—To meet the needs of microprocessor education seminars and classes at universities, a number of chip suppliers have introduced education systems that are somewhere between prototyping boards and development systems in terms of complexity and cost. A typical system has a number of boards including the CPU, a power supply, simple keyboard and display, and instruction books with a sequence of experiments and projects that enable the user to become familiar with the microprocessor and to write simple programs for it. Prices are in the $300 to $1,000 range for assembled products.

The focus of this analysis is on stand-alone development systems; however, some information will be provided on the multi-station systems as well as PROM programmers. Stand-alone systems currently dominate the development aids market, and are expected to remain the primary means of microprocessor program development. The systems covered here are dedicated by their design and software to the program development function. In some cases, general purpose microcomputers, such as those manufactured by MITS or IMSAI, are adapted to the program development for the 8080 chip. Generally, such systems are used to develop software at the system level rather than at the chip level. These systems are not covered in this analysis.

Participants

With few exceptions, the suppliers of development systems are semiconductor manufacturers that view this product as a necessary sales tool to promote use of their particular chip sets and provide a high level of customer support.

The leader in the microprocessor market, Intel, is also the leader in development systems. The early Intellec systems have evolved into extremely well-supported CRT-based systems with floppy disc operating systems, printers, and other peripherals, and include high-level language support. An added feature is in-circuit emulation (ICE), which permits the development system to simulate the microprocessor for program development, and then to insert the microprocessor in the system for prototype troubleshooting, program debugging, and system checkout. In addition to Intel, AMI, Fairchild, Mostek, Motorola, National, Signetics, Texas Instruments, and Zilog offer interactive program and system development aids of this type.

In addition to the semiconductor chip suppliers, there are two other groups of manufacturers that have entered the development systems market. These are the test instrument manufacturers, such as Tektronix, and a small group of independent suppliers. The general trend among the independent suppliers, as well as Tektronix, is to supply a "universal" development aid that can support a number of popular microprocessors. The chips that are currently supported are the Intel 8080 and 8085, the Zilog Z-80, the TI 9900, and the Motorola 6800. Support for other devices will obviously be added to the systems as the demand justifies supplier investment.

Because of the estimated 20,000 development systems installed worldwide, there is an

emerging market for independent manufacturers to offer add-on products for systems such as the Intel MDS. One example is Relational Memory Systems of San Jose, California, which offers the circuit board and accessories to permit the Intel MDS series of development systems to be used with the Z-80 microprocessor. The entry of Tektronix and the expected introduction of a program development system by Hewlett-Packard indicate the emergence of the development system as much more than just a microprocessor sales aid. The impact of the microprocessor on the traditional circuit and system design process in the electronics industry has prompted the need for a series of new types of test equipment for logic state analysis, data signature analysis, and system trouble shooting. Apparently the other test equipment suppliers, such as Biomation, E-H Research, and Systron-Donner, are waiting to see the impact of the Tektronix and H-P moves before making plans to enter the market.

Distribution

Since the primary purpose of development systems is to aid the customer in the use of semiconductor suppliers' chips and boards, the development aids are generally sold through the same channels as chips. Although direct factory salesmen also sell the development systems and prototype boards, the primary outlet is through distributors that have ready access to the large number of small and first-time microprocessor users and account for a high percentage of units shipped.

Some distributors have set up elaborate "design centers" at their facilities to make the system development tools available to local engineers. In most cases, these centers have not been successful, primarily because the engineer is out of his own environment working in someone else's facilities. As a result, most development systems are sold or rented.

Equipment rental firms—such as Electro Rents—have established nationwide rental of development systems, particularly the Intel line. This permits microprocessor users with only occasional or project-related design activities to use systems on an as-needed basis. As would be expected, after a rental "trial period" a number of the rental units are purchased; the user has been able to understand the savings in cost and time afforded by the system, which convinces his management of its value.

International Aspects

Sales of development systems and other design aids are closely tied to the sales and distribution of microprocessor devices. Widespread use of English and commonality of computer programming methods throughout the world make the program development system applicable on a worldwide basis.

The larger microprocessor suppliers, such as Intel, Motorola, Texas Instruments, use their worldwide marketing and distibution systems for sales of programming and design aids. Distribution by world area follows the sales levels of microprocessor devices throughout the world. In general, microprocessor suppliers have between 30 and 40 percent of their microprocessor-related sales in foreign markets, with development systems following the same pattern.

Special Industry Characteristics

The microprocessor or microcomputer program development system is a new approach to computer assisted product design, and it is fostering a new design and service aids industry that is still in its infancy. The semiconductor manufacturers are now aware that the way to create customer loyalty and product differentiation in their chip- and board-level products is to provide increased amounts of product sup-

port. Beginning with simple prototyping aids, the support aids have moved to interactive program development aids and are now expanding into related systems for use in production testing and field service, as well as the development of micro-codes for sophisticated systems.

The microcomputer systems support aid market is the result of market forces from the semiconductor, computer, and test equipment industries and will result in a major new business opportunity that is directly related to the seemingly endless number of new applications for microprocessors at both the chip and board level.

Trends

Development systems are most cost-effective in more complex applications where the size of the program and the complexity of the systems benefit directly from the in-circuit emulation and system debug capabilities. These are inherently the lowest unit volume markets and therefore less attractive to a chip supplier. If a semiconductor supplier is to provide only the support that enhances his market position and contributes to large volume microprocessor chip sales, then the high-end, disc-based development systems are of diminishing value.

Furthermore, sophisticated users are not expected to want to invest $15,000 in a system that will work with only one vendor's chips. Thus, a trend towards universal development systems is emerging and is being promoted by the independents. The users want universal systems, but the semiconductor suppliers only benefit from supplying a system for their own products. Therefore, it is likely that only a semiconductor firm with the market share and product popularity of Intel and Motorola, or a commitment to systems such as National and TI, can afford to continue to support the complex upper-end systems dedicated to a range of products.

This trend creates a dilemma for the semiconductor suppliers. If they choose to support their customers with better and more universal systems, they partially defeat the "marketing support" role of the development system. With or without the chip suppliers, it appears that system development aids will evolve into a sizable market served by independents, the major test instrument manufacturers.

Another trend in the program development systems market is towards multi-terminal or multi-station systems. Such systems are similiar to time-sharing, except that they are dedicated to microprocessor program development. Although only limited products have as yet been introduced to the market, Hewlett-Packard is expected to introduce a more sophisticated product of this type in late 1978 or early 1979. Such a product is expected to be based on a minicomputer such as the HP3000 and have provisions for a number of specially configured terminals providing for a range of program and system design and development tasks. These large systems are expected to sell for $200,000 to $300,000 and will be particularly attractive to large electronics systems manufacturers that need microprocessor system and program development in a number of separate locations. Centralized program storage, high level languages, support of all popular chips, libraries of utility programs, and standard formats for program documentation and field test procedures would do much to "rationalize" the current product design situation in many large companies.

A large electronics or computer manufacturer could have as many as 50 stand-alone development systems. At an average price of $10,000 each, this represents an investment of $500,000, not including training and installation costs. In large companies, these systems are vulnerable to replacement at the end of their economic life by a multi-terminal system.

Other trends in the development aids mar-

ket are affecting both prototyping boards and PROM programmers. In the case of prototyping boards, the unique or dedicated boards that the semiconductor chip manufacturers offer are being replaced by standard OEM boards as the chip suppliers further integrate into the board-level microcomputer market. This means that the potential chip user now purchases a set of standard OEM boards with support hardware and power supply in order to engage in hardware development. This has benefits for both suppliers and users in that the supplier can now manufacture a standard set of boards and the user has the option, after the prototype is completed, of buying chips for assembly onto boards or buying standard pre-tested boards from the chip supplier. The program development system that supports the chip-level products will also support the board- and box-level products, giving the user the make-or-buy option for any product under development.

PROM programmers are moving out of the development lab and into both the production facility and the field service shop. As the cost of PROM chips continues to decline, the use of these electrically programmable devices in production systems continues to increase. This creates the need for PROM "duplicators" in production and a capability for inserting program changes in PROMs in the field. In addition, the newer program development systems are incorporating on-line PROM programmers, eliminating the need for separate program development and PROM programmer units.

MARKETS

The stand-alone development systems market reached $74 million in 1977, representing a total of 8,900 units delivered by U.S. manufacturers. This brings the total of units delivered to date to 20,800. The semiconductor chip suppliers accounted for slightly over 90 percent of the market. Intel, the largest single supplier of development systems, had an estimated 54 percent of 1977 dollar shipments. In 1976 Intel had an estimated 46 percent of the total shipments of $41.8 million.

Table 2.8.5-1 gives the forecast of the stand-alone development systems market from 1977 to 1982. During this period the market is expected to grow from $74 million to $285 million, a 31 percent compound annual growth rate. The growth rate is expected to moderate after 1980 as the upward trend in average system prices slows due to increased competition, and the demand for stand-alone systems is impacted by sales of multi-terminal systems.

By 1982, the total number of stand-alone development systems in use is expected to approach 100,000 units. Assuming that there are approximately 400,000 engineers and programmers developing programs for microprocessor-based systems by that time, there will be one development system for every four potential users.

Unit shipments of stand-alone systems are expected to increase from 8,900 in 1977 to 21,800 in 1982 (see Table 2.8.5-2), a compound annual growth rate of 20 percent over the forecast period. Average system prices are expected to continue to increase as users find that there is a clear return on the development system investment and additional options are added to new units to increase their productivity. In 1977, the estimated average price of systems shipped was $8,300. This is expected to increase to $11,200 by 1980, and to $13,000 by 1982. This indicates an average system price increase of 9 percent per year. This increase takes into account the effects of moderate inflation and, more significantly, the increase in the memory, disc storage, software, and printers shipped with new development systems.

Other development aids such as PROM programmers and prototyping boards also experienced rapid growth in 1977. PROM pro-

2.8.5 Program Development Systems

Table 2.8.5-1
ESTIMATED STAND-ALONE DEVELOPMENT SYSTEMS MARKET
(Dollars in Millions)

Supplier Type	1976	1977	1978	1979	1980	1981	1982	Compound Annual Growth Rate 1977 - 1982
Semiconductor	$40	$67	$ 95	$120	$160	$200	$240	29.1%
Test Instruments	–	4	8	12	15	18	20	38.0%
Others	2	3	7	11	15	20	25	52.8%
Total	$42	$74	$110	$143	$190	$238	$285	31.0%

Source: DATAQUEST, Inc.

Table 2.8.5-2
ESTIMATED STAND-ALONE DEVELOPMENT SYSTEMS MARKET
(Thousands of Units)

Supplier Type	1976	1977	1978	1979	1980	1981	1982	Compound Annual Growth Rate 1977 - 1982
Semiconductor	7.2	8.3	10.4	12.0	14.5	16.7	18.5	17.4%
Test Instruments	–	0.3	0.7	0.8	1.0	1.2	1.4	36.1%
Others	0.2	0.3	0.7	1.1	1.4	1.7	1.9	44.7%
Total Annual Units	7.4	8.9	11.8	13.9	16.9	19.6	21.8	19.6%
Cumulative Units Shipped	11.9	20.8	32.6	46.5	63.4	83.0	104.8	

Source: DATAQUEST, Inc.

grammers grew from an estimated $7 million in 1976 to $12 million in 1977, and in 1978 are expected to achieve $18 million in sales by U.S.-based suppliers. It is extremely difficult to separate those PROM programmers that are used with development systems from those which go into production and field service applications.

Prototyping boards are also losing their identity of being unique to product develop-

ment activity as an increasing number of chip suppliers move into the OEM microcomputer board market and use these standard boards to support their customers' prototyping needs. Since many of these boards are sold to users through distributors, it is impossible to track the actual use of OEM boards in product development activities. The OEM microcomputer board market is analyzed in the Microcomputer Chapter of this Service.

TECHNOLOGY

The major distinguishing technological characteristics of the stand-alone development system are related to the software and in-circuit emulation features available. The actual hardware used in these systems is very similar to any small minicomputer and includes a microprocessor-based memory system (usually a floppy disc or cassettes). Typical peripherals include keyboard-CRTs for data input and programming development. The larger configurations require an operating system to manage the flow of data, and some of the systems have file managers associated with the auxiliary storage medium.

Flexibility and ease of use of any development system is closely related to software offered. Standard packages include compiler or assembler that allows translation of the programming code into machine instructions, an editor that traps and flags programming errors, and a program debugging routine that allows the system to step through the control sequence and check the logic and operation through software simulation of the target microprocessor. In the universal development systems, the use of software routines or "personality boards" allows a change in the target microprocessor for which the system can be used. Suppliers such as Microkit sell cassettes with the required programs to adapt the system for different microprocessors.

One of the most important features of stand-alone development systems is the ability to perform in-circuit emulation (ICE). This technique allows a program that has been developed using the simulation facilities of the system to be systematically transferred to the actual target microprocessor. The microprocessor is actually attached to the system and the programmer then transfers portions of the control program to the microprocessor's RAM, checking each step of the logic as he proceeds. Once the program is totally transferred and debugged, it can be used with confidence on production models of the system.

An interesting feature expected to be added to some development systems in the near future is the ability to develop multiprocessor systems. The inherent suitability of microprocessors for interconnection to form complex systems is difficult for designers to exploit using current development systems. Software is similar to uniprocessor systems but must be able to accommodate the interaction of multiple microprocessors. Furthermore, the ICE capability must allow interconnection of multiple microprocessors for final program checkout. The availability of this new feature will be important to the proliferation of multi-microprocessor systems and could be a key stimulant to the continuation of increased microprocessor chip sales.

The stand-alone program development system is expected to evolve to include at least limited multi-terminal capability. Tektronix is moving in that direction and the expected introduction of a time-shared, multi-terminal system by H-P would accelerate this trend. As stated earlier, a number of significant benefits to large users of development systems are inherent in the multi-user concept.

It will be interesting to see how Intel, with over half of the current installed base of stand-alone systems, reacts to the introduction of multi-terminal systems. Certainly, one option is

to offer a communications capability for existing MDS systems that would permit connection to a time-sharing service or a dedicated time-shared minicomputer. Given the need to maintain its current market position, the possibility of a new, multi-terminal, multi-microprocessor development system from Intel should not be ruled out. Other suppliers, such as National, are already headed in this direction.

The major suppliers of development systems are now offering high-level language support including BASIC, FORTRAN, and proprietary languages such as the Intel PL/M and Zilog PLZ. This capability extends the use of the systems to a greater number of engineers and reduces the time necessary to develop and test programs. As the size and complexity of programs increases, high-level languages offer easier programming and documentation at some expense in the amount of final code that must be put in the system ROM. It is expected that the use of high-level languages will increase rapidly.

PRODUCTS

The use of microprocessor design aids is relatively new to most logic and circuit (hardware) designers; however, among computer programmers the use of a "development system" (i.e., a computer system for software development) is widely accepted. In the case of large mainframes, the use of a time-sharing option (TSO) on the host computer permits interactive program development while the main system is performing its productive role. In minicomputer-based system development, it is normal to have a system of the type being used in the end-product dedicated to the software development job. Minicomputer manufacturers supply a wide variety of software tools for use in this interactive programming and debugging environment.

Hardware designers, on the other hand, are accustomed to working with logic diagrams and breadboards along with power supplies, signal generators, oscilloscopes, and other test equipment to deal with the electrical signals in the system. In the past, the hardware development tools have been less expensive and less sophisticated than the software development tools. It should be noted, however, that some sophisticated large system manufacturers have been using computer-aided circuit design systems for a number of years. These systems permit simulation of logic and circuit designs for worst-case power, temperature, and voltage levels. To a large extent, this function has now been taken over by the semiconductor manufacturers, with the system designer interconnecting selected logic building blocks. The large-scale circuit simulations are now being performed at the time of chip design, which lessens the need for chip users to have elaborate design systems at the circuit level.

Table 2.8.5-3 lists the scope of design aid products offered by leading suppliers. Time-shared and non-resident aids refer to simulators, assemblers, and other software available on a commercial time-sharing system or another host computer. More details about stand-alone systems are given in Table 2.8.5-2. Evaluation kits and boards are offered by most microprocessor suppliers. PROM programmers are offered as dedicated products and in some cases as options on stand-alone development systems. Other design aids include educational products and circuit analyzers.

Table 2.8.5-4 lists the leading stand-alone development systems available. These sophisticated design aids combine hardware and software development tools typically including high-level languages, disc memory, CRT displays, and output printers. The table indicates the supplier, model, applicable microprocessors, hardware configuration of the system, and unit base price. All stand-alone systems listed offer software, which includes a system monitor or

2.8.5 Program Development Systems

Table 2.8.5-3
MICROPROCESSOR DESIGN AIDS OFFERED BY LEADING SUPPLIERS

Supplier	Time-Shared/ Non-Resident Software Aids	Stand-Alone Development Systems	Evaluation Kits and Boards	PROM Programmer	Other Development Aids
Advanced Micro Devices		X			
American Microsystems	X	X	X	X	
Data I/O				X	
Fairchild	X	X	X	X	
Future Data		X			
General Instrument	X	X	X		
Information Control		X			
Intel Corporation	X	X	X	X	X
Intersil, Inc.		X	X		X
MOS Technology, Inc.	X	X	X	X	
Mostek	X	X	X		
Motorola	X	X	X	X	X
MuPro		X		X	
National Semiconductor	X	X	X		
NEC Microcomputer	X	X	X		
Prolog				X	
RCA	X	X	X		X
Rockwell Microelectronics	X	X	X		X
Signetics	X	X	X	X	
Synertek	X	X	X		
Tektronix		X		X	X
Texas Instruments	X	X	X		X
Zilog	X	X	X	X	X

Source: DATAQUEST, Inc.

operating system, an assembler, and a debugging package. Some systems also offer high-level languages for program development and more sophisticated file management systems.

The real value of the development system lies in its ability to greatly reduce the time (and therefore the cost) associated with the development and programming of a microprocessor-based system. The savings are the greatest in more complex systems where considerable amounts of time-sharing time, engineering time, and programmer effort would be required for successful system development. Thus, the development system and other system design aids are moving toward a universal system approach that is designed according to the specific development task by software and customized boards ("personality boards"). Some systems also offer the ability to design with several different microprocessors using cassettes or software changes to accommodate the desired microprocessor.

2.8.5 Program Development Systems

Table 2.8.5-4

LEADING STAND-ALONE DEVELOPMENT SYSTEMS

Supplier	Model	Applicable Microprocessors	Configuration: CPU	CRT	Keyboard	Cassette	Floppy	In-Circuit Emulator	PROM Programmer	Base Price	High Level Languages
Advanced MicroDevices	System 29	2901	X	X	X	NA	X	X	X	$25,000	NA
American Microsystems	6800 MDS	S6800, S2000, S3000	X	X	X	NA[1]	X	NA	X	$ 9,600	BASIC
Fairchild	Formulator-Mark I	F8, 3870	X	Opt[2]	X	Opt.	NA	NA	X	$ 595	NA
	Formulator-Mark II	F8, 3870	X	Opt.	X	Opt.	NA	NA	X	$ 1,695	NA
	Formulator-Mark III	F8, 3870	X	Opt	X	Opt.	NA	NA	X	$ 4,995	NA
Futuredata	Microsystem	6800, 8080, Z-80, 8085	X	X	X	Opt.	Opt.	Opt.	Opt.	$ 3,850	BASIC
General Instrument	Gimini	CP-1600, PIC-1650	X	X	X	NA	NA	X	NA	$ 3,500	NA
Information Control	Micro Command	Z-80, 8080	X	X	X	Opt.	Opt.	NA	NA	$ 4,875	NA
Intel Corporation	Intellec MDS-800 II	8080, 8048, 3000, 8086	X	X	X	NA	X	Opt.	Opt.	$ 3,950	PL/M, FORTRAN
	PROMPT 48	8048, 8748, 8035	X	NA	NA	NA	NA	NA	Opt.	$ 1,750	
	PROMPT 80	8080	X	NA	NA	NA	NA	NA	Opt.	$ 1,495	
Intersil, Inc.	Intercept	IM6100	X	Opt.	Opt.	NA	Opt	Dev.[3]	Dev.	$ 2,850	NA
MOS Technology, Inc.	MDT 650	6502	X	NA	X	Opt.	NA	NA	NA	$ 245	NA
Mostek	A10-80F	Z-80, 3870	X	NA	NA	NA	X	Opt.	Opt.	$ 1,295	#5995 FORTRAN
Motorola	Exorcisor II	6800, 3870	X	X	X	Opt.	X	NA	Opt.	$ 7,950	
MuPro, Inc.	MuPRO-80	8080, 8085	X	Opt.	Opt.	NA	Opt.	X	X	$ 3,950	NA
National Semiconductor	IPC-16P[4] (PACE-P)	PACE-SC/MP	X	Opt.	Opt.	NA	Opt.	Dev.	Opt	$ 4,115	NA
	ISP-8P/301 (LCDS)	SC/MP	X	Opt.	X	Opt.	NA	X	X	$ 499	NA
	SPX 80/40 (STARPLEX)	8080A	X	X	X	NA	X	Opt.	Opt.	$13,800	BASIC, FORTRAN
NEC Microcomputer	PDA-80	μCOM-8	X	Opt.	Opt.	Opt.	Opt.	Opt.	X	$ 4,000[5]	NA
RCA	COSMAC Dev. System	CDP-1800 Family	X	Opt.	Opt.	NA	Opt.	NA	NA	$ 3,000[5]	NA
Rockwell	Assemulator	PPS-4, PPS-8	X	Opt.	X	NA	Opt.	X	X	$ 3,450	NA
	R6500	6500	X	Opt.	Opt.	NA	X	X	X	$ 5,900	NA
Signetics	Twin[6]	2650	X	Opt.	Opt.	NA	X	X	Opt.	$ 9,625	NA
Synertek	MDT-650	6500	X	NA	X	X	Opt.	X	–	$ 5,000[5]	NA
Tektronix	8002[6]	8080, 6800, Z-80, 9900, 8085	X	X	X	NA	X	Opt.	X	$ 9,950	NA
Texas Instruments	FS990 Prototyping Sys	TMS 9900	X	X	X	X	NA	NA	Opt.	$ 5,000[8]	FORTRAN
	FS 990/X	TMS 9900	X	X	X	Opt.	HD[7]	Opt.	Opt.	$10,600[5]	
	990/10 DS	TMS 9900	X	X	X	Opt.	HD	Opt.	Opt.	$25,000[5]	
	HE-2	TMS 1000	X	NA	NA	NA	NA	NA	NA	$ 6,000[5]	
	990/40 DS	TMS 9940									
Zilog	ZOS-1/40	Z-80	X	X	X	NA	X	X	X	$11,690	BASIC, FORTRAN
	ZOS-1/25	Z-80	X	X	X	NA	X	X	X	$ 7,740	PL-Z

[1] NA – Indicates feature not available.
[2] Opt – Indicates feature optionally available.
[3] Dev. – Indicates feature in development.
[4] The IPC-16P is the same as National's IMP-16P except for the CPU.
[5] Indicates approximate base price.
[6] Built by Millenium Information Systems.
[7] HD – Indicates hard disc
[8] Bundled in hardware price.

Source: DATAQUEST, Inc.

The general purpose systems are particularly applicable in the higher performance bit/slice product area where the ability to effectively manipulate microcode and macro instructions is essential. It can be expected that suppliers such as AMD and Raytheon, who have pioneered the microprogrammable bit/slice products (along with the National IMP) and developed micro-level assembly languages (RAYASM and AMDASM), will offer program development systems for working with microcode in addition to high-level program development and system simulation.

On another front, the single-chip 16-bit processor with on-chip microprogram ROM is currently limited to either a proprietary instruction set or an emulation mode. With a development system that was adapted to the microcode structure of the chip, the user could optimize the instruction set during the system design and order chips with the proper ROM pattern. This would effectively avoid the problems of out-

board microprogram storage ROMs and reduce the system chip count. It also permits the customer to have a "custom" processor chip for only a slight additional cost.

The minicomputer industry has already established the approach of using a general purpose processor and peripherals with appropriate software for "system program development." The systems being supplied by some of the semiconductor firms such as Intel, National, and Zilog are already in this category. For the board- and box-level customer, these are ready-made development systems. It is the chip-level customer, who does not want to be committed to a single chip type or vendor, who desires the general purpose development system.

COMPETITION

The most vigorous exponents of development systems are the prime sources of the chip sets such as the Fairchild F-8, the Intel 8080, the Motorola 6800, the National SC/MP, the Signetics 2650, and the Zilog Z-80. Second sources of the 8080 include AMD, National, NEC, and TI, all of which offer only limited development support compared with Intel. Of course, one of the presumed advantages of second sourcing is that much of the product support and software costs can be avoided as this burden is being borne by the prime source. However, until recently, it appeared that the market position and support provided by Intel for the 8080 prevented a significant penetration of the chip market by alternate suppliers.

Tables 2.8.5-5 and 2.8.5-6 provide estimates of 1976 and 1977 shipments of development systems by primary suppliers. It should be noted that Millenium Information Systems (recently acquired by AMI) does not appear in the table because the company sells its development systems on an OEM basis only. Thus, its systems are counted under the share of the resellers such as Signetics and, in 1977, Tektronix. Until recently, there has been little competition in the stand-alone development systems market. The semiconductor suppliers have been competing primarily for chip sales, with the development systems used as their sales aid and marketing support product. Therefore, competition in the "development system market" as such did not exist among chip suppliers.

The recent entry of Tektronix indicates a new dimension of the market, with the traditional suppliers of test equipment and logic analyzers becoming suppliers of systems. The competition that is developing is between the general purpose development systems from the independent suppliers and the dedicated systems from the semiconductor suppliers. The market share held by the semiconductor suppliers is expected to drop from 91 percent in 1977 to 84 percent in 1982. Although the major microprocessor suppliers such as AMD, Intel, Mostek, Motorola, National, TI, and Zilog will lose shares to the independents, they will continue to make the investments necessary to provide a high level of customer support.

These estimates are based on a scenario in which the new, first-time, or small user would prefer to obtain both his support and his chips from the same vendor. The more experienced user, with more complex projects and a continuing product design effort, would opt for a general purpose system with the full support and service of the independent supplier. This would eventually push the semiconductor suppliers to the lower end of the market, which generates the most chip unit volume. The upper end would then consist of independents and those chip suppliers that choose to look at development systems and related systems as a separate market opportunity not directly related to sales of specific chip products.

Another aspect of the competitive situation in this market is that, as the instrument suppliers such as Tektronix enter the development systems market, the semiconductor suppliers

2.8.5 Program Development Systems

Table 2.8.5-5

ESTIMATED SUPPLIER UNIT SHARE OF WORLDWIDE MARKET
STAND-ALONE DEVELOPMENT SYSTEMS

Supplier	Units Shipped		Share of Units	
	1976	1977	1976	1977
Intel	4,000	5,000	54%	56%
National	900	1,000	12	11
Motorola	700	800	9	9
Zilog	*	300	*	3
Tektronix	–	250	–	3
Texas Instruments	*	250	*	3
AMI	*	200	*	2
Fairchild	*	200	*	2
Mostek	*	150	*	2
Signetics	*	150	*	2
Others	1,800	600	25	7
Total	7,400	8,900	100%	100%

*Included in "Others."

Source: DATAQUEST, Inc.

are moving to provide a broad range of microprocessor-oriented test and service products. Intel has introduced the Microscope 820 for field testing and troubleshooting of systems based on the 8080 and 8085. National has introduced the ICE BOX emulation system. AMI has recently acquired Millenium Information Systems, the leading private label manufacturer of development systems. Millenium has also introduced a Microsystem Analyzer for use with microprocessor-based systems.

Given that both the semiconductor and test instrument suppliers can build the hardware and provide the software necessary for microprocessor program development, the competitive edge must then go to the firms having the advantage in distribution and sales coverage. In this case, the semiconductor manufacturers apparently have a clear advantage in that they have much broader direct and distributor sales organizations than do the instrument manufacturers. In addition, the instrument manufacturers must train their sales people to operate in the fast-paced and aggressive microprocessor environment—an area in which the semiconductor manufacturers write the rules. As a result, the test equipment manufacturers are not expected to make a major change in the market structure for the stand-alone development systems.

Likewise, the other independents are not expected to achieve a market position in com-

2.8.5 Program Development Systems

Table 2.8.5-6
ESTIMATED SUPPLIER VALUE SHARE OF WORLDWIDE MARKET
STAND-ALONE DEVELOPMENT SYSTEMS

Supplier	Value ($ Millions) 1976	Value ($ Millions) 1977	Share of Value 1976	Share of Value 1977
Intel	$20	$40	40%	54%
Motorola	6	8	14	11
National	4	5	10	7
Tektronix	—	4	—	5
Texas Instruments	*	3	*	4
Zilog	*	3	*	4
AMI	*	2	*	3
Fairchild	*	2	*	3
Signetics	*	2	*	3
Mostek	*	1	*	1
Others	12	4	28	5
Total	$42	$74	100%	100%

*Included in "Others."

Source: DATAQUEST, Inc.

petition with both the semiconductor and test instrument manufacturers. Although there will be good growth opportunities for the relatively small number of independents in this market, their combined market share is expected to be less than 10 percent of the total 1982 market for stand-alone development systems.

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STAND-ALONE MICROPROCESSOR DEVELOPMENT SYSTEM SUPPLIERS

American Microsystems, Inc. (AMI)
3800 Homestead Road
Santa Clara, CA 95051
(408)246-0330

Fairchild Camera & Instrument Corporation
464 Ellis Street
Mountain View, CA 94042
(408)998-0123

General Instrument Corporation
Microelectronics Division
600 West John Street
Hicksville, NY 11802
(516)773-3107

Intel Corporation
3065 Bowers Avenue
Santa Clara, CA 95051
(408)246-8501

Intersil, Inc.
10900 Tantau Avenue
Cupertino, CA 95014
(408)996-5000

Futuredata
2180 Colorado Avenue
Santa Monica, CA 90404
(213)828-8539

Millenium Information Systems
19020 Pruneridge Avenue
Cupertino, CA 95014
(408)996-9109

MOS Technology, Inc.
950 Rittenhouse Road
Norristown, PA 19401
(215)666-7950

Mostek Corporation
1215 W. Crosby Road
Carrollton, TX 75006
(214)242-0444

Motorola Semiconductor Products, Inc.
Box 20912
Phoenix, AZ
(602)991-0733

muPro, Inc.
10340 Bubb Road
Cupertino, CA 95014
(408)996-1137

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, CA 95051
(408)737-5000

NEC Microcomputers, Inc.
Five Militia Drive
Lexington, MA 02173
(617)862-6410

Ramtek
292 Commercial Street
Sunnyvale, CA 94086
(408)735-8400

RCA Corporation
Solid State Division
Route 202
Somerville, NJ 08876
(201)685-6000

Rockwell International
Microelectronic Device Division
3430 Miraloma
Anaheim, CA 92803
(714)632-8111

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Signetics Corporation
811 East Arques Avenue
Sunnyvale, CA 94086
(408)739-7700

Synertek
3050 Coronado Drive
Santa Clara, CA 95051
(408)241-4300

Texas Instruments, Inc.
Digital Systems Division
P.O. Box 2909
Austin, TX 78767
(512)258-5121

Tranti Systems, Inc.
1 Chelmsford Road
N. Billerica, MA 01862
(617)667-8321

Zilog, Inc.
170 State Street
Suite 260A
Los Altos, CA 94022
(415)941-5055

PROM PROGRAMMER SUPPLIERS

Data I/O Corporation
Box 308
Issaquah, WA 98027
(206)455-3990

ProLog Corporation
2411 Garden Road
Monterey, CA 93940
(408)372-4593

2.8.8 Redundancy

SUMMARY

Redundancy is receiving increasing attention in the design and manufacture of semiconductor memory because it combats the problems of reduced yield and reliability that result from today's larger and more complex chips. IBM, INMOS, and Intel have already announced devices that employ redundancy, and DATAQUEST expects that other companies will soon follow. In addition, Bell Laboratories, NEC, and NTT have designed research devices that employ redundancy.

DATAQUEST believes that the use of redundancy will become increasingly popular. In particular, we believe that redundancy offers strong economic advantages over chips that do not employ redundant techniques. The following factors are of extreme importance:

- 64K MOS RAMs without redundancy will have difficulty competing economically with 16K RAMs.
- The use of redundancy can dramatically increase yields of large complex memory arrays. Redundant storage can be justified, even considering improved wafer processing.
- A device with redundancy can cost significantly less than a device of equal size without redundancy that has undergone equivalent processing.
- DATAQUEST believes that customers will readily accept devices employing redundancy.

Use of redundancy, fault tolerance, and fault correction will markedly alter design, manufacture, and testing of future semiconductor memory. The development of these new factors in semiconductor technology should be closely followed. This section deals with one method of employing redundancy to improve yield in large memory devices. We will discuss other methods of fault correction in future sections.

REDUNDANCY—WHAT IS IT?

Many schemes have been advanced in the past to employ fault-tolerant or fault-correcting methods in semiconductor manufacture, beginning as far back as 1964 at IBM and 1965 at Texas Instruments.

For large memory arrays, the majority of the chip is the array. This part is the area that can be corrected by redundant techniques. At this time, redundant techniques apply only to the large complex arrays.

In current technology, redundancy is achieved through the use of a few spare rows and/or columns in memory arrays combined with the associated sense amplifiers and row and column decoders. The defective row or column is replaced by a spare row or column through the use of polysilicon fuses or by cutting

2.8.8 Redundancy

interconnections with lasers. The advantages of redundancy are clear: if a bit on a nonredundant dynamic RAM is defective, the chip is rejected. On a redundant chip, the row and column that contains the defective bit is replaced. Furthermore, redundancy is transparent to the user because the memory supplier "blows" the polysilicon fuses or cuts the interconnections. Also, the cost of redundancy is small since the additional rows, columns, and logic add a small percentage to the array—usually only 5 to 10 percent—and because redundancy can improve yields by a factor of five or six.

The polysilicon fuse approach has two basic advantages: polysilicon fuses require only a moderate amount of wafer processing, and they can be blown when the die undergoes testing. The laser method is not so convenient because of the time it takes to position the laser on the die.

THEORY

Semiconductor device defects are of two types—spot defects and area defects. Improvements in semiconductor processing over the last several years have reduced the number of area defects. The major concern today is with spot defects. Spot defects may affect only one memory cell. They are often (but not always) distributed randomly over a wafer and are related to the general processing cleanliness of wafer fabrication. If the average defect density is known, yield results can be mathematically calculated. Yield curves have been used for a long time and are considered relatively reliable. Given chip area (and knowing the defect density for that particular process) the percent of perfect devices (yield) can be calculated. Additionally, the percent of devices with one defect, two defects, three defects, etc., can also be calculated using a Poisson distribution. For example, Table 2.8.8-1 presents the distribution of defects where the average defect density is 3.38 defects per chip. Devices with different defect densities—due, for example, to improved processing—or with different chip sizes would give different figures. Two things are clear:

- There is a significant penalty for increased chip size.
- For low-yielding semiconductor devices, there is an additional large percentage of devices with only a few defects per chip.

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Table 2.8.8-1

AN EXAMPLE OF THE POISSON DISTRIBUTION OF
RANDOMLY DISTRIBUTED DEFECTS
(Average Defect Density per Chip = 3.38)

Number of Defects on Chip	Percent of Chips
0	3.4%
1	11.5%
2	19.4%
3	21.9%
4	18.5%
5	12.5%
6	7.0%
7	3.3%
8	1.3%

Source: DATAQUEST, Inc.
February 1981

In Table 2.8.8-2, DATAQUEST calculated the potential yield of a hypothetical chip using redundancy. We compared examples of the same array by using a chip not employing redundancy, and a somewhat larger chip employing redundancy. Some important assumptions were made:

- Only up to two defects per chip can be corrected
- Half of all defects cannot be corrected

Nevertheless, the yield improvements are startling and significant. It is DATAQUEST's understanding that actual results from devices employing redundancy bear out this significance. It should be noted that the level of yields here—one percent to 15 percent—is on the order of those used for large memory arrays, including 64K dynamic RAMs, 16K static RAMs, and 64K EPROMs.

2.8.8 Redundancy

Table 2.8.8-2

THEORETICAL YIELDS USING REDUNDANCY
(Percent)

Chips Without Redundancy (Range of Typical Yields) No Correction	Chips With Redundancy		
	No Correction	One Defect Correction	Two Defect Correction
1.0%	0.8%	3.0%	7.9%
3.0%	1.9%	5.6%	13.0%
5.0%	3.4%	9.1%	18.8%
10.0%	7.7%	17.5%	30.1%
15.0%	11.0%	22.8%	36.5%

Assumptions:

1. Chip with redundancy is 15 percent larger than the corresponding chip without redundancy. (Chip without redundancy = 38,250 sq. mil)

2. Only (up to) two defects per chip can be corrected.

3. 50 percent of all defects cannot be corrected.

4. Standard yield equations, statistical (defect) distribution, and Poisson distribution have been used.

Source: DATAQUEST, Inc.
February 1981

To see what this means in terms of device economics, devices chosen from the center row of Table 2.8.8-2 were used to calculate approximate device cost and prices (see Table 2.8.8-3). Specifically, we used a hypothetical 64K RAM without redundancy, with a chip area of approximately 38.3 thousand square mils. No additional wafer fabrication cost for the redundant chip was used. The redundant devices have significantly higher testing costs. Chips at die sort have to be tested, defective bits identified, redundant rows and columns activated, and devices retested. DATAQUEST estimates that testing costs can be up to five times greater with a redundant device than a non-redundant device. However, catastrophically bad devices and others need not go through the full testing routine. A testing cost at die sort of 2-1/2 times is assumed. While other costs (such as improved visual sort) might come into play, the two major additional costs of devices using redundancy come from additional testing and larger die size.

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Table 2.8.8-3

ESTIMATED HYPOTHETICAL DEVICE COSTS

	Chip Without Redundancy	Chip With Redundancy[1]
Device	64K RAM	64K RAM
Chip Area (Sq. Mils)	38,250	44,000
Total Chips Per Wafer	267	223
Yield	5.0%	18.8%
Yield without Redundancy	5.0%	3.4%
Wafer Cost	$80	$80
Gross Die Cost	$ 0.30	$ 0.36
Wafer Sort Cost (Per Die)	0.088	0.22
	$ 0.388	$ 0.58
Yielded Die Cost (5%)	$ 7.76	$ 3.08
Assembly Cost	0.18	0.18
	$ 7.94	$ 3.26
Yielded Assembled Devices (85%)	$ 9.34	$ 3.83
Final Test Cost	0.80	0.80
	$10.14	$ 4.63
Yielded Good Devices (70%)	$14.49	$ 6.62
Selling Price (40% Margin)	$24.14	$11.04

[1] Up to two defects corrected, see Table 2.8.8-2

Source: DATAQUEST, Inc.
February 1981

In making these assumptions, we have been conservative in several important areas:

- We assumed an increase in chip size of 15 percent, almost twice the reported actual values.
- Only devices with two or less defects are corrected via redundancy. Significantly higher yields might be possible if devices with three or four defects were similarly corrected.
- We assumed that only half of the devices with one or two defects could be actually corrected, although we estimate the actual percentage is considerably higher.

The improvement in cost and price can be significant.

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PROS AND CONS

The arguments for and against redundancy in memory arrays have several important points. They can be summarized as follows:

- For redundancy:
  - Higher yield
  - Lower cost
  - Lower facility and equipment cost
  - Equipment availability
  - Lower sensitivity to alpha particles
- Against redundancy:
  - Larger chips
  - Increased processing costs
  - Much greater testing costs
  - Slower speed
  - Some questions on reliability

We believe that the economic benefits of redundancy significantly outweigh the costs. Increased chip size can pay an important penalty in yield. However, reducing minimum line widths to reduce chip size has its own penalties in terms of yield. Redundancy techniques offer a possibility to increase yield for larger chips and make yield less sensitive to chip area. This result means facilities that have been employed to make 16K RAMs with four to five micron minimum dimensions can make 64K RAMs with redundancy. More expensive facilities, with a higher degree of cleanliness, will be required for three micron 64K RAMs. Thus, the user of redundancy can allow facilities and equipment that are lower in cost. New equipment required to make 64K RAMs is expected to be in short supply as the new generation of RAMs, microprocessors, telecom devices, automotive control devices, etc., are brought into production. It is possible that the availability of proper equipment will play an important role in determining market share in many semiconductor markets. The ability to use older, more proven equipment for some production can be a significant advantage.

Larger chips, with larger cell sizes, would be less sensitive to alpha particle radiation—a definite marketing benefit in some instances. However, larger cell sizes, and the additional circuitry employed for redundancy, does affect the speed performance of devices. We do not believe that this is significant, but it may be a marginal factor in the market.

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The sale of chips with defects has raised the question of reliability. There are some defects that with aging could cause failures in adjacent bits. However, inspection, testing, and burn-in have proven effective in eliminating problem devices. The use of partial 16K devices has had excellent results. DATAQUEST believes that most users will quickly come to accept redundant devices.

64K RAMS VERSUS 16K RAMS

With the reinstatement of competitive pricing in the semiconductor MOS memory market, a special problem has been generated for 64K RAMs. These devices will soon have to sell (in quantity) at under $10 to compete with 16K RAMs selling for around $2 each. Is this possible? In all previous generations of semiconductor memory, there has been little change in chip size. Today's 16K RAMs are not markedly different in chip size from the 256-bit dynamic RAMs of 10 years ago. In each new generation, there was an abundance of "cleverness" to provide significant cost improvements. These included a variety of process improvements, cell design improvements, and circuity improvements. Major improvements in succeeding generations included the advent of silicon gates, the switch to NMOS, and the use of double layers of polysilicon.

For the 64K RAM, however, no such dramatic improvements are envisioned. Indeed, most 64K RAM chips are significantly larger than 16K RAM chips. What is important is the total number of good bits that a wafer can provide. The 64K RAMs must get one fourth of the yield (having four times the bits) of 16K RAMs. In terms of die area, this means that a 64K RAM chip must be approximately 33,000 square mils in area to compete with a 20,000 square mil, 16K device.

Some hypothetical costs, as estimated by DATAQUEST, are shown in Table 2.8.8-4. The table highlights an important marketing problem for 64K RAMs: it is extremely difficult for 64K RAMs, with minimum design dimensions of 3.5 microns, to compete with 16K RAMs with minimum dimensions of 5 microns. Even if that were possible, the smaller dimensions could be applied to new 16K RAM designs and provide significantly lower costs.

2.8.8 Redundancy

Table 2.8.8-4

HYPOTHETICAL ESTIMATED COST COMPARISON

RAM Density	16K	16K	64K	64K
Minimum Dimension (Microns)	5	4.0	3.5	3
Die Area (Sq. Mil.)	20,000	14,000	40,000	30,000
Die Per Wafer	600	850	300	400
Yield[1]	25%	43%	8.83%	13.6%
Good Die	150	360	26	54
Die Cost	$0.48	$0.21	$3.54	$1.70
Final Selling Price	$2.11	$1.40	$12.50	$7.00

[1] Assumes (falsely) that there is no yield penalty for reduced dimensions, and that 64K RAMs are at the 16K point on the learning curve

Source: DATAQUEST, Inc.
February 1981

Most importantly, these calculations assume that there is no yield penalty for reduced dimensions, but this is not the case. Devices with smaller dimensional tolerances have defects caused by proportionally smaller particles. The number of particles increases with the cube of the inverse of their size. For example, there are eight times as many 3 micron diameter particles as there are 6 micron diameter particles. This means that to get equivalent yields for 64K RAMs, significant improvements have to be made in facilities, equipment, and processing techniques. The cost penalties of those improvements and the associated yield penalties are not well defined. However, the conclusion is important: It is extremely difficult for 64K RAMs to compete economically with 16K RAMs unless the chip size is extremely small or redundancy is employed.

WHAT'S DIFFERENT NOW

The idea of redundancy has been around a long time and has never proven to be the winning technological approach in the past. As a result, it has a poor reputation in the technical community. This reputation has perhaps slowed the attention

given to redundancy recently. We believe that there are several major factors now that change the relative advantages of employing redundancy. They are:

- The process of manufacturing polysilicon fuses has advanced in recent years.
- Larger arrays employ redundancy more efficiently.
- Significantly lower packaging costs—as more memory is packaged in plastic—have taken away the major cost improvement (4 to 1) found in higher density chips.
- Further improvements in facility cleanliness and equipment precision are becoming extremely expensive.
- Lack of major new process, cell design, and circuitry improvements (cleverness) do not provide immediate cost improvements.
- General processing improvements have increased the percentage of small spot defects (i.e., correctible defects) to total defects.

CONCLUSION

The arguments for redundancy appear fairly compelling while the arguments against redundancy are increasingly weak. The most consistent argument against redundancy is, "Our yields are O.K. With our processing capability we don't need it." But that argument begs the question. If yields are adequate without redundancy, they can be still better with it. It's that simple. Redundancy should not be regarded as a "fix"—we believe that it will be an inherent part of future large memory arrays.

2.10 Integrated Circuit Packaging

SUMMARY

Historical forces have influenced the choice of package technology and the choice of pin configuration and spacing. The increasing requirement for packages with more than 40 pins is creating demand for more compact packages than can be achieved with the traditional DIP (dual in-line package) configuration. This has led to the QUIP (quad in-line package), developed by Intel and 3M, and to the chip carrier. Sometimes these packages are leadless; often a socket is used to facilitate interconnection at the next level.

The interconnection of integrated circuit packages is required if useful electronic equipment is to be constructed. Popular mounting techniques include flow-soldered printed circuit boards, electronic watch assembly, hybrid assembly, and flip-chip assembly.

The key package technologies are discussed in detail, including TO header, flatpack, ceramic DIP, CERDIP, plastic DIP and chip carriers. Demand for CERDIP and chip carriers is seen as growing faster than total package requirements. Plastic DIPs now account for 80.7 percent of integrated circuit packages, though this share is forecast to fall to 79.5 percent in 1982; plastic technology is believed to be very active and subject to significant future technological change. In particular, copper alloy lead frames with interdigitation and silver plating are seen as cost-reduction measures. (Interdigitated lead frames use less metal because the leads of one package occupy the space between the leads of the next package.) In addition, it is possible that thermoplastics will be substituted for thermosetting plastics in some applications.

Current 1979 prices for the 14-pin configuration are about 6.3¢ for plastic DIPs, 9.9¢ for the CERDIP, 82¢ for ceramic DIPs, and 51¢ for the chip carrier. These prices help to explain the popularity of plastic DIPs in low-cost applications. These prices are for 500,000 units and up, but price adders for lower quantities are provided later in the report. In addition, the effect of variations in gold prices on package prices is given for CERDIP and ceramic packages.

We estimate that IC package consumption by U.S. companies accounts for roughly 73 percent of worldwide ~~IC manufacture~~ on a dollar volume basis. The figures provided in this report include packages that are consumed by U.S. companies, but because of assembly yield losses, are less than the amounts shipped as finished IC units.

IC package consumption

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INTRODUCTION

The package technology for integrated circuits has been driven by three historical forces: complexity, reliability-cost considerations, and power. Integrated circuits were first introduced in the early 1960s as simple gates and flip-flops. The low complexity of these devices allowed them to be packaged in 8- or 12-lead TO-type headers (transistor outline metal can package). As more complex small scale integrated (SSI) and medium scale integrated (MSI) circuits were introduced, it became necessary to seek packages with a greater number of leads. To a large extent, this need for higher lead count was met by the DIP.

The DIP package has two rows of leads. These rows of leads are normally 0.3 inches apart on packages with 20 or fewer leads, 0.4 inches apart on packages with 22 leads, and 0.6 inches apart on packages with 24 or more leads. DIP packages are currently available with up to 64 leads. The leads themselves are separated from each other by a space of 0.1 inches. As an option, some manufacturers form the DIP leads in such a fashion that each of the two rows of leads is staggered by 0.2 inches; allowing more flexibility in printed circuit board layout. DIP packages may be manufactured using ceramic, plastic, or CERDIP technology. Ceramic packages are constructed from a ceramic material and generally feature brazed-on leads and a die-mounting cavity that is sealed with a metal lid by a soldering technique. The integrated circuit manufacturer assembles the CERDIP package using a glass sealing method from separately supplied ceramic parts and a lead frame. The manufacturer also assembles the plastic package by a transfer molding process from separately supplied epoxy and lead frames. While the outer dimensions of the DIP package are standardized, the dimensions of the die mounting area are not and these tend to vary from one integrated circuit manufacturer to another, depending on the requirements for the size of the die mounting area, height of the die, and location of the bonding pads. Typically a given DIP configuration (e.g., 14 pins) may be tooled in 10 or more configurations.

Reliability and cost considerations may dictate the choice of a package technology. Hermetic packages are usually preferred in situations where the lowest cost is not required. A hermetic package encloses the semiconductor chip in an air-tight cavity; usually, the cavity is filled with dry nitrogen at the time of closure. Since only dry nitrogen is in contact with the die, there is little chance of a chemical reaction between the die and the packaging material. Usually a hermetic package is checked, at least on a sampling basis, to see that it has no holes that would allow the dry nitrogen to leak out. Both gross and fine leak tests are used. The gross leak test may simply consist of a system for immersing the package in a fluid to look for bubbles; the fine leak test may make use of a radioactive tracer gas. Plastic packages, though lower in cost, are not hermetic since the plastic material directly contacts the semiconductor die. As a result, there are more possibilities for varying chemical reactions between the die and the packaging material or between the die and any moisture or other liquid that might infiltrate the package material. Although these possible chemical reactions may create additional failure modes, proper quality

control procedures can maintain the reliability of plastic packages at a level comparable with that of hermetic packages.

As LSI devices become more complex, they tend to dissipate more power. If this power is not dissipated by the package, the temperature of the semiconductor die can increase to the point where performance or reliability is degraded. Ceramic packages are good power dissipators because the ceramic material readily conducts heat from the die to the surface of the package. Plastic is more of a thermal insulator and, as a result, plastic packages have lower power-handling capabilities. Currently, some work is being done to add materials to the plastic which will improve the power-handling capacity of this package. Electronic equipment manufacturers have used various means to improve package power-handling capability, including everything from forced air cooling to mounting the package on a metal plate. As lead counts increase to 64 pins and beyond, there is a need for a new package configuration to replace the DIP. With its 0.1-inch pin centers, a 64-lead DIP package must be at least 3.2 inches long (actually, a little longer when allowance is made for the fact that the package must extend beyond the last pin). This large package tends to make printed circuit boards larger, a situation that, in turn, makes electronic equipment larger. Two solutions to this problem are currently being offered.

Intel and 3M have jointly developed what is called a QUIP. This package places 32 leads on each side of the package in two staggered rows with 0.1-inch spacing; it is intended for use with a socket that can be automatically mounted on a printed circuit board. This package and socket combination is said to use 40 percent less printed circuit board area than a conventional 64-pin DIP.

Another new package configuration is the so-called chip carrier, which features terminals on all four sides of a basically square package. Kyoto Ceramic, Kyocera, and 3M are suppliers of ceramic chip carriers. AMP supplies a low-cost injection molded plastic chip carrier. These terminals are on 0.050-inch centers—half that of a conventional DIP. The terminals may have leads attached or may be leadless; in the latter case, they are simply metallized regions in the package itself. Fundamentally, this package type offers great space savings over current technology, but requires that new techniques be developed for assembling the package into electronic equipment. A JEDEC (Joint Electron Device Engineering Council) committee is currently meeting to set standards for this package.

MARKETS

This section deals with integrated circuit package consumption by U.S. companies and accounts for yield losses in the assembly process. Since much assembly is accomplished outside the United States, these figures of necessity include packages and package materials that are consumed overseas. Once assembly is complete, many of the finished integrated circuits are sold into foreign markets as well. Although consumption of the packaged integrated circuits and package materials may occur overseas, most of the purchase commitments are made in the continental United States. Most companies selling packages or package materials to U.S. companies have representation in the United States.

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Table 2.10-1 gives estimated integrated circuit package consumption by U.S. companies for 1978. On a unit-count basis, most package requirements are presently being met by the plastic DIP. Nevertheless, some of the other package types offer lucrative markets to suppliers of packages and materials because of the higher unit selling prices.

Table 2.10-1

ESTIMATED 1978 INTEGRATED
CIRCUIT PACKAGE CONSUMPTION
BY U.S. COMPANIES

Package Type	Millions of Units	Unit Share (Percent)
Plastic DIP	4,020	80.7%
CERDIP	710	14.2
Ceramic DIP	120	2.4
Flatpack	60	1.3
TO Header	50	1.0
Chip Carrier	20	0.4
Total	4,980	100.0%

Source: DATAQUEST, Inc.
July 1979

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Table 2.10-2 shows the way in which package shipments are distributed by pin count among the various package technologies. It is interesting to note that the CERDIP and plastic DIP show a heavier concentration in the lower pin counts. This is probably due to the fact that most low-cost integrated circuits have low pin counts. Due to their low cost, these circuits generally employ the low-cost CERDIP and plastic technologies. The concentration of high pin counts for the ceramic DIP reflects the use of this package in LSI applications where pin count and circuit prices tend to be higher.

Table 2.10-2

ESTIMATED 1978 INTEGRATED CIRCUIT PACKAGE CONSUMPTION BY U.S. COMPANIES

(Percent Share of Units by Pin Count)

Pin Count	Chip Carrier	TO Header	Flat-pack	Ceramic DIP	CERDIP	Plastic DIP
8	-	55%	-	5%	3%	12%
10	-	30	20%	-	-	1
12	-	15	-	-	-	-
14	5%	-	28	9	31	33
16	24	-	19	11	45	24
18	36	-	-	20	6	8
20	-	-	-	-	1	1
22	-	-	9	21	5	8
24	32	-	17	12	7	9
28	2	-	-	12	1	4
36	1	-	7	-	-	-
40	-	-	-	10	1	-
Total	100%	100%	100%	100%	100%	100%

Source: DATAQUEST, Inc
July 1979

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Table 2.10-3 presents forecasted unit IC package consumption by U.S. companies for 1978 through 1982. Unit consumption is expected to show a 15.2 percent compound annual growth rate through this period. A slightly greater growth rate is anticipated for both the CERDIP and chip carrier, as indicated by their increasing share of unit consumption.

Table 2.10-3

ESTIMATED U.S. INTEGRATED CIRCUIT
PACKAGE CONSUMPTION BY YEAR

	1978	1979	1980	1981	1982	Compound Annual Growth in Units
Plastic DIP	80.7%	80.9%	79.7%	79.8%	79.5%	14.2%
CERDIP	14.2	14.5	15.5	15.8	16.1	18.2%
Ceramic DIP	2.4	2.0	1.9	1.7	1.6	2.8%
Flatpack	1.3	1.0	0.8	0.6	0.6	(3.5%)
TO Header	1.0	0.9	0.9	0.7	0.6	0.9%
Chip Carrier	0.4	0.7	1.2	1.4	1.6	62.1%
Total	100.0%	100.0%	100.0%	100.0%	100.0%	14.6%
#	5084	6348	7199	8755	10444	12310 (14509) (17103
4	5117	5936	6571	7654	8828	10101 11900 ~~14485~~ 13000
Units (Millions)	4,980	5,781	6,400	7,454	8,598	
	.974	.974	.974			
				9487	12085	15197 18290 21615
New #		6961	8521		Source: DATAQUEST, Inc.	
New 4		6509	7778	8731	10209	July 1979 12470 14370 16430
X.974 (=45)		6340	7575	8504	9944	12146 13996 16003

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MOUNTING OF INTEGRATED CIRCUIT PACKAGES

Traditionally, integrated circuit packages have been mounted on printed circuit boards. These boards are usually made of an epoxy fiber glass material and have their conductive copper wiring defined by a chemical etching process. They may be made of single layers or they may be multilayered. Package mounting is accomplished by providing holes in the printed circuit board through which the leads of the integrated circuit are inserted. This insertion may be performed manually, but it is possible to use automatic insertion equipment, at least for a DIP with 24 or fewer pins. Once all packages are inserted on a board, it is passed through a wave soldering machine that creates a standing wave of molten solder by pumping it through a rectangular opening. The solder serves to complete both the electrical and mechanical connections between the package and the printed circuit board.

Multilead packages are difficult to remove from a printed circuit board once they have been soldered, a situation that makes troubleshooting more difficult and expensive. Consequently, many electronic equipment manufacturers have begun using sockets. These sockets, rather than the package, are soldered to the printed circuit board, allowing the package to be easily removed from the socket for troubleshooting.

The addition of leads in ceramic packages requires an extra manufacturing step. Most sockets have a springy metal contact that is similar in form and cost to a lead. Thus, it is possible to provide a combination of socket and leadless package for approximately the price of a package with leads. Both the Intel/3M QUIP and some versions of the chip carrier are intended for use with an accompanying socket.

Manufacturers of electronic watches have extremely tight space requirements; as a result, they have developed a new assembly technology. Typically, an integrated circuit chip is mounted on a printed circuit board using an epoxy die attach. Leads are then bonded from the chip to the board using an ultrasonic bonder, and the chip and wires are covered with a drop of epoxy. Sometimes the chip is protected by a small plastic cup before the epoxy is applied.

Hybrid circuit technology offers another means of interconnecting integrated circuits. The starting material is a ceramic substrate. Both resistors and interconnect wires can be silk-screened onto this substrate; subsequently, they are fired in a high-temperature furnace. Necessary integrated circuits and capacitors are then mounted to the substrate by conventional die attach and lead bonding. After this step, the entire ceramic substrate is packaged to prevent damage to the semiconductor parts. This technique is similar to watch manufacture inasmuch as no package at all is used for the integrated circuit chip. Instead, the necessary mechanical protection is provided at the next level of interconnect.

Unpackaged integrated circuits are difficult to handle and test. As a result, there is a high probability that defective chips will be incorporated in the assembly and then removed after testing shows them to be bad. These repair costs may more

than offset the savings obtained by eliminating one level of packaging. Various techniques are used to alleviate this problem, including flip chips and chip carriers.

Flip chips have raised solder bumps applied in regions where it is intended that the chip be bonded to a ceramic substrate. The chip is then placed on the substrate upside down and aligned with the substrate interconnect points. Substrate and chips are passed through a high-temperature furnace, which causes the solder to melt (reflow). A certain amount of self-alignment occurs since the chip floats on the solder balls and is drawn into near-perfect alignment by surface tension. IBM uses this method for mounting semiconductor die to ceramic substrates. Flip chips can generally be probe tested more reliably because the solder ball enhances electrical contact between chip and probe card.

Chip carriers were originally developed to make it easier to handle chips. Semiconductor chips are mounted to the chip carrier by conventional die attach and wire bonding techniques and the carrier is often mounted to a ceramic substrate by reflow soldering. Mostek's 32K RAM uses two chip carriers containing 16K RAMs that are then mounted on an 18-pin carrier "Mother Board" configured like an 18-pin DIP.

TECHNOLOGIES

Several technologies, described below, are used to package integrated circuits. These technologies vary in cost and also in the degree of effort required of the semiconductor manufacturer. Some packages, such as the ceramic DIP and TO header, are available in virtually finished form while others, like the plastic and CERDIP, require a certain amount of package manufacture performed as part of the process of packaging or assembling the integrated circuit.

In all cases, the integrated circuit manufacturer must perform the functions of die attach and lead bond. Die attach refers to the process of attaching the integrated circuit to the package, which may be accomplished at high temperature with a solder preform, or may be at room temperature using an epoxy material. Leads are generally attached by bonding to interconnection pads on the integrated circuit itself. The common methods are thermocompression, ultrasonic, and thermosonic bonding. Bonders may be operated manually or automatically. Thermocompression and thermosonic bonds generally use gold wire; ultrasonic bonds use aluminum wire.

TO Header

TO headers are purchased separately as a base and cap. The metal base of the package contains cylindrical leads which are arranged in a circle that is normally .4 inch or .2 inch in diameter. The leads are passed through individual, hermetic glass to metal seals. Typically, the leads and base are gold plated. Die attach is made to the base and, after wire bonding, the cap is hermetically attached to the package by welding. This package is available in 8, 10, and 12 leads. The technology used to make this package is mature and has been in use since the early 1960s. When DIP packages became available the TO package lost favor because it is difficult to insert and remove from printed circuit boards and awkward to use for lead counts above eight.

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Table 2.10-4 lists manufacturers that supply TO headers and caps to U.S. companies. Primary suppliers are believed to have somewhat greater market share than other suppliers.

Table 2.10-4

TO HEADER AND CAP SUPPLIERS TO U.S. SEMICONDUCTOR COMPANIES

Primary Header Suppliers	Location
Isotronics	Bedford, Massachusetts
Motorola, Inc.	Phoenix, Arizona
Plessey Chatsworth	Chatsworth, California
Shinko Denki	Nagano, Japan
Texas Instruments	Dallas, Texas
Other Header Suppliers	
Hermetic Seal	Rosemead, California
Hermetite Corp.	Avon, Massachusetts
Koto Denshi Co., Ltd.	Tokyo, Japan
Primary Cap Suppliers	
Texas Instruments	Attleboro, Massachusetts
Truelove and McLean	Waterbury, Connecticut

Source: DATAQUEST, Inc.
July 1979

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Flatpack

Flatpacks are distinguished by their extremely compact dimensions, which allow construction of compact, lightweight electronic equipment. This characteristic, together with the fact that flatpacks represent a mature technology offering true hermetic seals, accounts for their popularity in military applications. Assembly of flatpacks to printed circuit boards is expensive and is often done by welding or RF (Radio Frequency) soldering the leads to the top traces of a printed circuit board. In other cases, the leads are formed and fed through holes in the printed circuit board to be soldered by more conventional techniques. In satellite and airborne applications, the high cost of equipment construction using this package is more than offset by savings in space and weight. Usage of this package in military applications is expected to decline somewhat as the chip carrier becomes more popular.

Flatpacks have typical body thicknesses of .050 inch to .080 inch. The leads are thin (.004 to .006 inch) ribbon-like sheets of metal .015 to .019 inch wide, spaced on .050-inch centers. Flatpacks are available in 10, 14, 16, 22, and 24-pin versions. Flatpacks are typically of multilayer ceramic construction but glass-ceramic construction (CERPAC) and glass-ceramic-metal construction are also used. Usually, the package is sealed by soldering a metal lid to the top. Normally, this is accomplished by placing a solder preform between the lid and package, and passing the whole assembly through a belt furnace that heats both lid and package to the point where the solder reflows. Recently, this lid has also been attached with a glass seal. The flatpack is supplied as a finished unit ready for sealing with lid and preform. Package suppliers are listed in Table 2.10-5; lid and preform suppliers are listed in Table 2.10-6.

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Table 2.10-5

CERAMIC PACKAGE SUPPLIERS TO U.S. SEMICONDUCTOR COMPANIES

Company	Chip Carrier	Flat Pack	Ceramic DIP	Glass Ceramic DIP	CERDIP
AMP, Inc., Harrisburg, Pennsylvania[1]	S[2]	-	-	-	-
Ceramic Systems, San Diego, California	S	-	-	-	-
Coors Porcelain, Golden, Colorado	S	PS[3]	-	-	PS
Diacon, San Diego, California	S	S	-	PS	S
Hermetic Seal, Rosemead, California	-	S	-	S	-
Hermotite Corp., Avon, Massachusetts	-	S	-	S	-
Isotronics, Bedford, Massachusetts	-	-	-	PS	-
Kyocera Intl., San Diego, California	PS	PS	PS	-	PS
Kyoto Ceramic Ltd., Kyoto, Japan	PS	PS	PS	-	PS
3M Company, St. Paul, Minnesota	PS	PS	PS	-	-
Metceram, Rosenthal, Providence, Rhode Island	S	PS	PS	-	-
National Beryllia, Haskell, New Jersey	-	-	S	-	-
Narumi Co., Ltd., Nagoya, Japan	-	S	S	-	PS
NGK Spark Plug, Inc., Nagoya, Japan	-	S	PS	-	S
Plessey Frenchtown, Frenchtown, New Jersey	-	PS	-	-	PS
Plessey Chatsworth, Chatsworth, California	-	-	-	S	-
Space Ordnance Systems, Saugus, California	-	-	-	PS	-
Shinko Denki, Nagano, Japan	-	-	-	-	S
Siltec, Inc., San Diego, California	-	-	-	-	PS
Tekform Products, Anaheim, California	-	-	-	PS	-
Texas Instruments, Dallas, Texas	-	PS	-	-	-

[1] Supplies plastic chip carriers
[2] S = Supplier
[3] PS = Primary Supplier

Source: DATAQUEST, Inc.
July 1979

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Table 2.10-6

LID AND PREFORM SUPPLIERS TO U.S. SEMICONDUCTOR COMPANIES

Company	Location
Alpha Metals	Jersey City, New Jersey
Cominco American	Spokane, Washington
Consolidated Refining Co.	Mamoroneck, New York
Plessey, Inc.	Melville, New York
Semi Alloys	Mt. Vernon, New York
Williams Precious Metals	Buffalo, New York

Source: DATAQUEST, Inc.
July 1979

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Ceramic DIP

The ceramic DIP is available in DIP configurations of 8, 14, 16, 18, 20, 22, 24, 28, and 40 pins. It may be of multilayer ceramic construction (with top-brazed, bottom-brazed, or side-brazed leads), glass-ceramic construction, or glass-ceramic-metal construction. The major sealing technique uses a gold-plated metal lid and a gold-tin eutectic sealing preform. A low-temperature glass seal is also available. A 64-pin configuration is expected to enter production in 1979. Efforts are being made to reduce package costs and it is expected that gold content will be reduced by limiting gold to the die and wire bonding areas only. When this occurs, the lead frame will be tin plated or solder coated. Suppliers for the ceramic DIP and the glass-ceramic-metal DIP are listed in Table 2.10-5; lid and preform suppliers are listed in Table 2.10-6.

CERDIP

CERDIP is a term probably coined from the words "ceramic DIP". However, construction of the CERDIP is quite different from that of the ceramic DIP described in the previous paragraph. CERDIPs are typically available in the DIP configuration with available pin counts of 8, 14, 16, 18, 22, 24, 28, and 40 pins. CERDIP packages offer the least expensive hermetic technology available and, as a result, demand for this package is continuing to grow.

The semiconductor manufacturer who assembles integrated circuits with the CERDIP also performs part of the package assembly. The ceramic base and cap are purchased from suppliers listed in Table 2.10-5. The ceramic base has a metallized gold spot to provide a means of die attach. Lead frames for this package are purchased separately from the suppliers listed in Table 2.10-7. Generally, the lead tips on these frames are aluminized so that aluminum bonding wire can be used. The integrated circuit manufacturer performs the functions of attaching the lead frames to the base, die attach, lead bond, and package seal. Sealing can be accomplished with either vitreous or nonvitreous glass. When this package was first developed, it was not considered suitable for MOS applications because contaminants released from the glass during sealing could cause degradation of the MOS die. Improvements in die passivation and sealing techniques have now largely eliminated this problem.

A "bull's eye lid" for the CERDIP is being developed for use in MOS EPROM applications. This lid incorporates a special glass that will transmit the ultraviolet light used for erasing the PROMs and is less expensive than the sapphire lids currently used. This development appears to be a significant one for the CERDIP; costs are lower than the ceramic DIP package used for EPROMs and it does not seem to be possible to make a plastic package that will transmit ultraviolet light needed by EPROMs.

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Table 2.10-7

STAMPED LEAD FRAME SUPPLIERS TO U.S. SEMICONDUCTOR COMPANIES

Company	For CERDIP Packages	For Plastic Packages
Advalloy, Palo Alto, California	PS[1]	S[2]
Arnold Engineering, Fullerton, California	S	PS
Buckbee-Mears, St. Paul, Minnesota	-	-
Caribidex, Southgate, Michigan	-	S
Dynacraft, Santa Clara, California	-	PS
Jade Corp., Huntington Valley, Pennsylvania	-	S
Mitsui Co., Ltd., Yokahama, Japan	S	PS
Oberg Mfg., Freeport, Pennsylvania	S	PS
Plessey Montvale, Montvale, New Jersey	PS	PS
Stamping Technology, Santa Clara, California	PS	S
Sylvania, Warren, Pennsylvania	-	PS
Texas Instruments, Attleboro, Massachusetts	-	PS
U.G.M. Co., Ltd., Tokyo, Japan	-	PS
Youngwood Metals, Murraysville, Pennsylvania	S	S

[1]PS = Primary Supplier
[2]S = Supplier

Source: DATAQUEST, Inc.
July 1979

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Plastic DIP

Plastic DIPs offer the lowest cost technology currently available for integrated circuits. These packages are available in 8- and 10-lead, 14- through 28-lead, and 40-pin versions. The integrated circuit manufacturer purchases plastic and lead frames separately and manufactures the completed package as part of the assembly process. Lead frames are available from the suppliers listed in Table 2.10-7 and plastics are available from the suppliers listed in Table 2.10-8.

Table 2.10-8

PLASTIC SUPPLIERS TO U.S. SEMICONDUCTOR COMPANIES

Primary	Location
Allied Chemical	Toledo, Ohio
Dow Corning Corp.	Midland, Michigan
Hysol Division, Dexter Corp.	Industry, California
Morton Chemical	Chicago, Illinois
Other	
Dynacraft, Inc.	Santa Clara, California
Emerson and Cumming	Canton, Massachusetts
General Electric	Waterford, New York

Source: DATAQUEST, Inc.
July 1979

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The integrated circuit manufacturer attaches die directly to the lead frame. Typically, a number of lead frames are joined together in a strip with the number of package sites depending on the lead count. Commonly the frame is alloy 42 (42 percent nickel and the balance iron) with spot gold plating in the die attach and bonding areas; however, some manufacturers have used the lower cost silver plating since the early 1970s. Copper alloy lead frames with silver plating are being considered as an additional cost-reduction measure. Interdigitation of the lead frames may also serve as a material- and cost-saving technique. Gold wires are used in all plastic packages to bond from the die to the lead frame and lead tin solder is the standard coating for the external leads.

Tape bonding has been used as a substitute for wire bonding. In this technique a metal tape is produced that has patterns configured to match the locations of the pads on the die and the leads on the package. Since every die has its bonding pads in a different location, this approach requires that a separate tape be tooled for each die configuration. Either the die or the tape has solder bumps applied and all leads of the tape are simultaneously attached to the die by a machine called an "inner lead bonder." The outer leads are attached to the frame by an "outer lead bonder." This technique is used for a significant fraction of current SSI assembly. Some logistical problems have been caused because a separate tape must be inventoried for each different die type. Automatic lead bonders are programmed to bond to the pads on the die; accordingly, the need to inventory separate tapes for each die configuration is eliminated. Since the advent of automatic lead bonders offering cost savings comparable to those of tape bonders, tape bonding has not been popular for new designs.

Once die attach and bonding are complete, the lead frame is placed in a transfer mold where a plastic material is formed around each die site. The packages are subsequently detached from the frame and leads are formed to the desired configuration. The plastic is shipped in refrigerated form and is a thermosetting plastic. Under heat and pressure the plastic permanently takes the desired form; reheating the plastic does not permit it to be reformed. Phenolic was an early material used in plastic packages, but is now virtually phased out. Silicones then became popular, but since 1974 have been superseded by Novolac epoxies.

Plastic packages generally have lower power ratings than CERDIP or ceramic packages, but new packages with copper lead frames and molded-in heat sinks may alleviate this problem. Some suppliers are also changing filler loadings to improve the dissipation of the plastic material.

Thermoplastics may offer savings over thermosetting plastics because they can be reheated and reused. Since 40 to 60 percent of the epoxy material is now wasted in the transfer molding process and cannot be reused, thermoplastics could offer significant savings. In addition, they may be less expensive and need not be refrigerated during shipment. Riton, a development of Phillips Petroleum, is being considered for this use.

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Chip Carrier

The chip carrier was originally developed for use in hybrid applications; it is now being considered for broader application in electronic equipment. It can have leads or be leadless with terminals available on all four sides of the square package; terminals are on .050-inch centers. Multilayer ceramic construction is used predominantly today and the processes of assembly and hermetic sealing are similar to those used in the ceramic DIP. Chip carrier suppliers are listed in Table 2.10-5. Leadless packages are often used with a mating socket, but may be soldered to a ceramic substrate or printed circuit board. We believe the reliability of printed circuit board assembly is questionable because of the mismatch of thermal coefficients of expansion between the package and the printed circuit board. If no socket is used, compliant leads can be added to the chip carrier to alleviate the mismatch problem. Chip carriers are available with 14, 16, 18, 24, 28, 36, 40, and 64 leads. A JEDEC specification is currently being written for this package in its various versions.

Wright-Patterson Air Force Base has sponsored a Manufacturing Technology program (MAN-TECH) to develop chip carriers with six different pin counts between 14 and 84 pins. This contract was awarded to Hughes, RCA, and Texas Instruments, and has attracted considerable industry attention. IBM's use of high lead count leadless ceramic carriers in its new computer systems should also stimulate use of this technology.

AMP, Incorporated, of Harrisburg, Pennsylvania, is working on a low-cost chip carrier. This device is made of injection molded plastic, and should be considerably less expensive than the ceramic chip carriers.

ALPHA PARTICLE PROBLEM

An alpha particle consists of two protons and two neutrons (identical to the nucleus of a helium atom). In typical packages, these particles are usually emitted by the elements uranium and thorium, which occur in trace amounts in most packaging materials, including the alumina used in ceramic packages, the glass used for sealing CERDIP packages, the gold-plated lids used on ceramic packages, and the epoxy or silicone used in plastic packages. (Recently, Ferro Corporation, working with Coors Porcelain, claims to have developed a CERDIP sealing glass with lower alpha emission.) When an alpha particle strikes a semiconductor chip, it creates hole-electron pairs; these neutralize stored charges or cause currents to flow. The net effect is that a random noise signal is injected into the part—a signal that can cause a spontaneous error to be generated. These errors are referred to as "soft errors" because there is no permanent damage to the chip.

The severity of the alpha particle problem depends on the sensitivity of the chip. So far, it appears that CCDs and MOS dynamic RAMs have exhibited the greatest sensitivity, but alpha-induced errors have been detected in static RAMs designed with polysilicon load resistors as well. It is likely that the alpha particle problem will confront package manufacturers for some time. Although measures are being taken to

reduce device sensitivity, the trend toward a smaller device dimension acts to increase device sensitivity. Alternate solutions to the alpha particle problem are as follows:

- Packaging. Thus far, it has been established that the glass used to seal CERDIP packages may produce more than 10 times the alpha radiation of the ceramic material itself. Package vendors are now working to screen incoming materials more carefully and semiconductor vendors are beginning to specify tolerable levels of alpha radiation in packages.

- Coatings. Alpha particles can be stopped by the presence of such simple things as Scotch Tape or masking tape. Accordingly, most manufacturers are experimenting with various compounds to coat the chip. It is likely that some time will elapse before a suitable coating is found, since every coating must be evaluated for its effect on the long-term reliability of the semiconductor part.

- Design and Processing Changes. Some designs have been found to be less sensitive to alpha particle problems than others. Accordingly, semiconductor manufacturers are taking such steps as modifying oxide thicknesses and providing aluminum layers over portions of the die that are alpha particle sensitive.

2.10 Integrated Circuit Packaging

PRICES

The prices of integrated circuit packages depend on quantity, technology, and the amount of precious metal used in the package. Most packages are sold directly to integrated circuit manufacturers, and in large quantities. In this report, our prices assume procurement in lots of 500,000 pieces or more. Table 2.10-9 shows how prices might be adjusted for lower-quantity purchases. This information is intended as a guideline only; pricing by specific manufacturers may vary considerably. There is little consumption of packages in less than 10,000 piece lots and distribution channels are not well developed; therefore, prices may vary even more.

Table 2.10-9

ESTIMATED QUANTITY PRICE BREAKS
FOR INTEGRATED CIRCUIT PACKAGES

Units Purchased	Normalized Price
500,000	Unity
250,000-500,000	Add 11%
100,000-250,000	Add 15%
50,000-100,000	Add 50%
25,000-50,000	Add 70%
10,000-25,000	Add 100%

Source: DATAQUEST, Inc.
July 1979

2.10 Integrated Circuit Packaging

Table 2.10-10 gives a comparison of 14-pin package costs to the integrated circuit manufacturer. It is industry convention to include labor costs for the plastic package since at least part of the labor is concerned with package assembly rather than die assembly. Labor costs are not included for the other package types since, with the exception of the CERDIP, the package is supplied as a complete unit. Multilayer ceramic construction is assumed for the ceramic DIP and chip carrier. Note the relatively high cost of the solder preform that is used to attach the lid.

Table 2.10-10

ESTIMATED INTEGRATED CIRCUIT PACKAGE COST ELEMENTS FOR 14-PIN PACKAGES[1]

(Quantities of 500,000)

Plastic	0.600¢	Epoxy, Handling, and Refrigeration
	3.000¢	Lead Frame
	0.005¢	Die Attach, Epoxy
	0.400¢	Gold Wire
	4.005¢	Total Material
	2.300¢	Yield Factor, Labor and Overhead
	6.305¢	Total
CERDIP	3.90¢	Ceramic Base
	1.50¢	Tinning
	3.00¢	Frame
	1.50¢	Tinning
	9.90¢	Total
Ceramic DIP	66¢	Side Brazed Package
	3¢	Lid
	13¢	Solder Preform for Lid
	82¢	Total
Cerpac	31¢	Package and Frame
	4¢	Lid
	35¢	Total
Chip Carrier	35¢	Multilayer Ceramic Package
	3¢	Lid
	13¢	Solder Preform for Lid
	51¢	Total

[1]Prices assume gold adder at $200 per ounce

Source: DATAQUEST, Inc.
July 1979

2.10 Integrated Circuit Packaging

Table 2.10-11 extends the costs of Table 2.10-10 to packages with pin counts other than 14. Package prices today conventionally include a "gold adder." This is a factor that is used to adjust the price of the package as the price of gold increases and decreases. For competitive reasons, most package quotes are made with the assumption that gold is $105 an ounce. When the package is shipped, the invoice to the buyer reflects a new price that accounts for cost increases due to increases in the price of gold. The costs given here reflect a gold price of $200 per ounce. Table 2.10-12 shows how the prices of 14-lead ceramic and CERDIP packages might have changed as gold increased from $105 to $200 per ounce. In July 1979, the price of gold is $305 an ounce.

Table 2.10-11

ESTIMATED 1978 INTEGRATED CIRCUIT PACKAGE COSTS
(Quantities of 500,000)

Pin Count	Normal DIP Row Spacing (inches)	Chip Carrier	TO Header and CAP	Cerpac	Ceramic DIP	CERDIP	Plastic DIP
8	.3	-	$.18	-	-	$.072	$.077
10	.3	-	$.20	$ .28	-		$.058
12	.3	-	$.24	-	-	-	-
14	.3	$ .51	-	$ .35	$ .82	$.099	$.063 ← 7.8-8.1
16	.3	$ .56	-	$ .36	$ .84	$.129	$.065
18	.3	$ .61	-	-	$ .91	$.239	$.073
20	.4	-	-	-	$ .93	-	$.086
22	.6	-	-	$ .65	$1.01	$.333	$.099
24	.6	$ .78	-	$ .83	$1.23	$.408	$.118
28	.6	$ .82	-	-	$1.61	$.643	$.143
36	.6	$ .95	-	$1.45	-	-	-
40	.6	$1.00	-	-	$2.89	$.940	$.232 — 35-40

Source: DATAQUEST, Inc.
July 1979

2.10 Integrated Circuit Packaging

Table 2.10-12

ESTIMATED EFFECT OF GOLD ADDER ON PACKAGED PRICE
(Quantities of 500,000)

	Gold At $105 Per Ounce	Gold At $200 Per Ounce
14 Lead Side-Brazed Ceramic (Excluding lid and preform)	55.0¢	66.0¢
14 Lead CERDIP	4.7¢	5.4¢

Source: DATAQUEST, Inc.
July 1979

6.1 Board-Level Microcomputers

INDUSTRY CHARACTERISTICS

Introduction

At the low end of the computer price and performance scale there are a growing number of new classes of products labeled "microcomputers." These exciting, "new generation" products are creating new markets and causing changes and redefinitions in the prior generation minicomputer markets. Although the term "microcomputer" has been broadly defined, products and markets are becoming more established and segmented. The term "microcomputer" refers to board-level CPUs that are sold individually or incorporated in system-level products. System- or box-level hardware products include boards, cabinet, power supply, and, increasingly, some form of tape or rotating memory.

This section focuses solely on board-level products as a separate subsegment of the microcomputer marketplace. The board-level microcomputer market has experienced explosive growth, which we believe should continue during the five year forecast period. Board-level products often also represent the first leading edge of applied technology. Furthermore, as microprocessor chips become denser and faster, and as more software is encoded in microcode or logic arrays, DATAQUEST expects that board-level products will acquire more systems orientation and move up into the minicomputer domain.

Software — including operating systems, real-time executives, and development utilities — is now increasingly important as microcomputer products are introduced into wider, more user-oriented markets; as the creation, expansion, and maintenance of totally debugged software becomes critical; as programmer efficiency becomes a more important factor; and as manufacturers try to differentiate among themselves in the marketplace.

The present board market has evolved from at least three distinct areas as follows:

- Experimenter and Hobbyist
- Scientific and Lab Control
- Industrial Automation and Control

Experimenter and Hobbyist

The experimenter and hobbyist market started in 1974 with the introduction of inexpensive 8-bit microcomputer chips. This market was originally served by small, entry-level companies that first offered printed circuit board kits and later marketed assembled and tested boards. This type of board-level product soon became a system box with front-panel switches. Its switches were later replaced with a small monitor program so a CRT could be used for input and output. Most of

the early participants in this market are now in the "systems" business with board products providing only incidental revenues.

Scientific and Lab Control

The scientific and lab control market was originally addressed by Digital Equipment Corporation with the PDP-8 minicomputer in the early 1960s. Digital still dominates the market with its PDP-11 minicomputer and LSI-11 family of boards. Its continued domination is largely a function of the large installed base of PDP equipment in this market and the reliability of the large amount of associated software with which users are already familiar.

Industrial Automation and Control

The industrial automation and control market began in the 1960s as minicomputers were used with numerical control (N/C) machines and process automation systems. By 1978, the power of the minis was contained on a board and direct digital control (DDC) had taken over. Microcomputer chips on low-cost boards were also replacing logic relays. But the end-user engineers who were forced to design low-volume applications with chips were becoming frustrated by circuit timing and coordination problems and with manufacturers' specifications. When the semiconductor manufacturers initially designed a few demonstration boards, they were surprised at the user interest in board-level products. Up to that point they had not realized that many users, especially in industrial automation, would pay for highly reliable functions that were precoordinated on a board. The customers did not want to solve the rather artificial problem of interfacing the latest set of chips. Reliability was essential and a board-level product was an insurance policy that the chip set would actually work.

Products included in DATAQUEST's definition of board-level microcomputers are:

- 8-bit Small Bus Boards - STD Bus, KIM Bus, SYM Bus
- 8-bit Large Bus Boards - EXORbus, Multibus, Versabus, S-100 Bus
- 12- and 16-bit Boards - Multibus, S-100 Bus, Q-bus

Excluded from this analysis are:

- Custom board products
- Prototyping boards sold by semiconductor suppliers to familiarize potential customers with microprocessors
- Microprocessor development systems

6.1 Board-Level Microcomputers

For more detailed information on microprocessor development systems or personal computers, please refer to Vol I - Section 6.2, or Vol II - Section 6.1, respectively. DATAQUEST also publishes a separate Test Instrument Industry Service (TIIS), which includes microprocessor development systems data.

The analysis in this section focuses on the general purpose board market at the OEM level, rather than on resale or end-user markets. Within the context of the hardware classifications of DATAQUEST's Small Computer Industry Service (SCIS), this section covers:

- Class I boards - Basically all 8-bit products (small and large bus)
- Class II boards - Basically PDP-8 12-bit boards
- Class III boards - Basically 16-bit medium performance boards

Participants

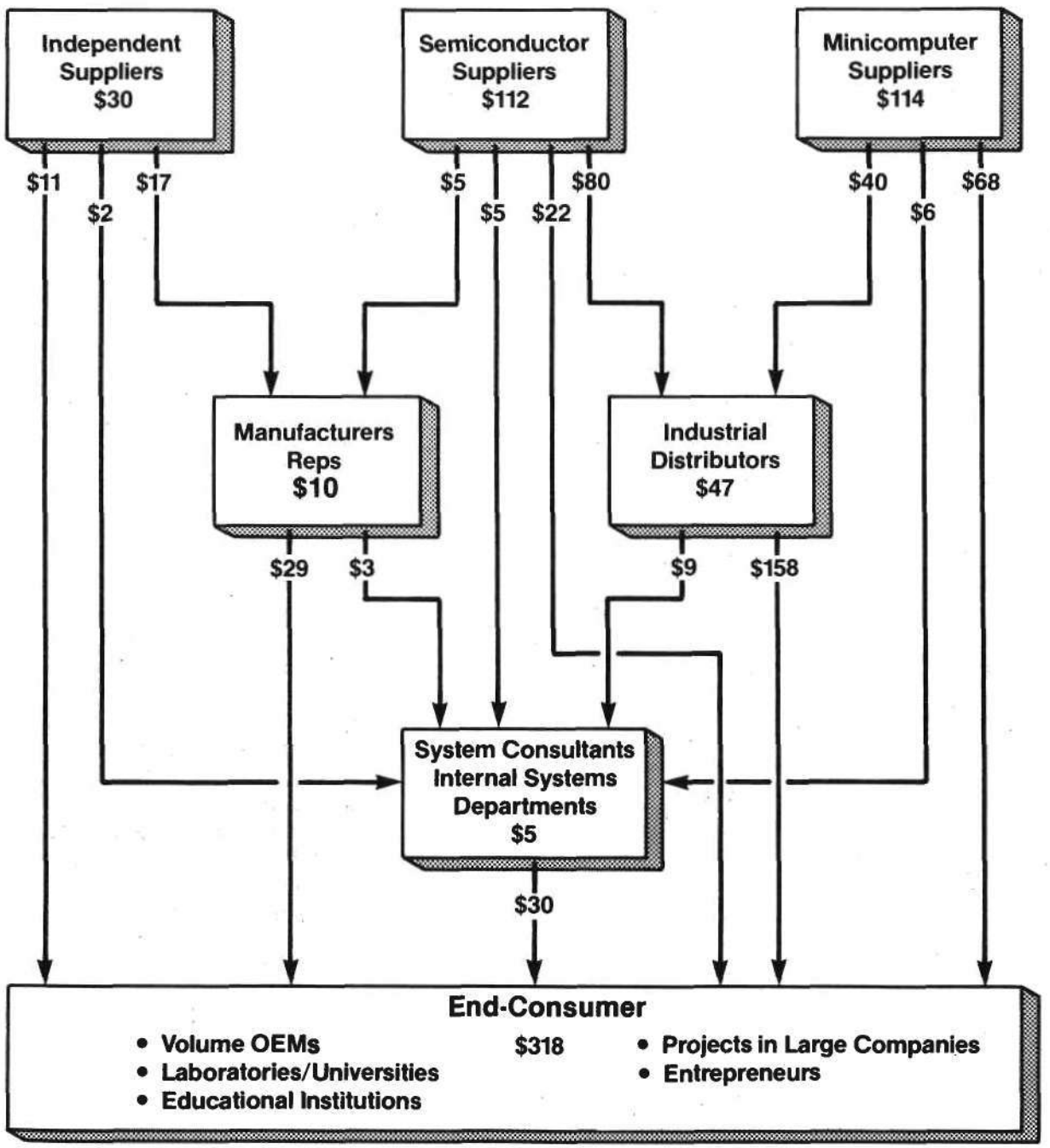
The board-level microcomputer market is structured in a unique manner as a result of three diverse types of suppliers to the market. The three supplier groups are: traditional minicomputer manufacturers, semiconductor suppliers, and independent suppliers. These suppliers bring to the market three different sets of perspectives, distribution methods, and marketing philosophies. Figure 6.1-1 outlines the board-level microcomputer industry structure with estimated 1980 shipments shown on the interconnecting lines and the participant's value added shown within the boxes.

In addition to the suppliers of boards, related participants in this market include: systems integrators, software development organizations and consultants, in-house engineering teams, independent sales representatives, large national or regional distributors, and suppliers of components (power supplies, frames, cabinets, sensors). The system integrator companies, in particular, span a large range of sizes and focuses. In size they range from small enterprises with one or two projects to large organizations with multiple projects and well-staffed engineering and software departments. In focus, system integrators range from a narrow vertical market orientation such as medical instrumentation or numerical machine control to a broad range of projects for many clients. Currently there is a trend in large companies toward internal systems integration departments to provide for industrial control needs; these departments represent a significant share of the board market. Even within large organizations, dispersed local engineering teams often develop their own smaller-scale projects for boards, chips, or systems.

6.1 Board-Level Microcomputers

Figure 6.1-1

BOARD-LEVEL MICROCOMPUTER INDUSTRY STRUCTURE
1980 SHIPMENTS AND VALUE-ADDED
(Millions of Dollars)



Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

Major minicomputer companies with a position in the board-level market include Computer Automation, Data General, Digital Equipment, General Automation, and Hewlett-Packard. Of the companies committed to this market, Data General, Digital, and Hewlett-Packard have captive semiconductor sources. Other suppliers use custom chips purchased from outside vendors. Texas Instruments (TI) is a difficult company to categorize. It has introduced board-level products using the 16-bit processor chip, both through its Digital Systems Division and through its Semiconductor Division. Honeywell, with its rapidly expanding chip-level technology and instrumentation background, can be expected to enter the board market eventually, probably through its Synertek subsidiary.

All the major semiconductor companies—including Intel, Mostek, Motorola, National, Texas Instruments, and Zilog—have made strong entries into the board-level market. In recent years, AMD, Fairchild, Intersil, and Synertek have also introduced board-level OEM products based on microprocessor chip sets. Intersil recently introduced a set of STD-bus boards to be sold through selected industrial distributors. The semiconducter suppliers approach the board market as a separate profit center and as a business diversification rather than as a simple extension of their chip business. Zilog, one of the first companies to introduce a line of boards, recently dropped its board-level product line in a consolidation move forced by its parent company, Exxon Enterprises, Inc., a subsidiary of Exxon. Fairchild previously sold board products based on its NOVA-compatible FLAME microprocessors, but is presently offering only custom-designed boards.

The semiconductor manufacturers now dominate the 8-bit board markets due to a better cost position on microprocessors and memory, and wide distribution channels. Although the 16-bit board market has shown substantial growth, semiconductor suppliers have not yet penetrated it as previously expected by some observers. This lower penetration is due to the delayed introduction of many of the new 16-bit chips, but also is a result of the need for the more sophisticated software required to take advantage of the higher microprocessor performance now available. The independent suppliers of board-level products generally provide specialty boards such as analog-to-digital converters or specialized controllers. These independent supplier boards often interface to standard industry bus structures. These suppliers also use well-accepted chip sets, thus most are based on 8-bit microprocessors. Independent suppliers produce boards primarily for the industrial marketplace, but a few specialize in commercial and hobbyist systems, mostly using the S-100 bus.

There are a large number of independent board suppliers. Some of the suppliers in the industrial area are Analog Devices, Applied Micro Technology, Data Translation, Heurikon, Micro-link, Micro/Sys, and Prolog. In the commercial S-100 area, most independent suppliers of very small business computers such as Cromemco, North Star, and Vector Graphic still sell boards, although the emphasis is on systems. Independent suppliers of commercial S-100 boards include California Computer Systems, Godbaut, and Systems Group.

6.1 Board-Level Microcomputers

Hardware Products

Board-level microcomputer products consist of boards, card cages with power supplies and cabinetry, and input/output interconnections and sensors. Boards can be categorized first by the type of interconnect bus structure used and second by the type of function performed. Interconnect bus structure need not be standardized between manufacturers or even models, but bus standards initially set by industry leaders have often been accepted in the industry to allow for multiple sourcing and the convenience of developing specialty boards. Bus standards themselves fall into three catagories: physical standards, electrical standards, and logic standards. The Euro-card standard, for example, is only a physical standard. Even with physical and electrical standards, the buyer must still beware of incompatible logical standards, even on so-called second-sourced boards.

Given these precautions on "standardized" buses, DATAQUEST divides bus-structures into two generic types:

- Small-bus - Characterized by a data bus of 8-bits or less and an address bus of 16-bits or less; usually also characterized by small format, single-function boards; includes STD-bus, KIM-bus, SYM-bus

- Large-bus - Characterized by a data bus of 12- to 16-bits and an address bus of 16 to 32 bits; usually, but not always, large-format multifunction boards; includes Multi-bus, Versabus, Q-bus, S-100 bus

Boards may also be catagorized by function. Most industry participants divide boards into three generic functions: CPU boards, memory, and input/output/controller boards. But, as chip-level logic becomes denser and as interfaces become more standardized, more functions are being implemented on a single board. This category is epitomized by the "single-board computer." The following insert is a nonexclusive list of many common functions implemented on boards. The small-bus type boards are often designed with only one function per board. It is possible, for example, to implement each of the following functions on separate small-bus boards: CPU, memory, serial ports, parallel ports, floating point, and DMA-controller. On the other hand, all these functions are often on a single large-bus board. It is also important to determine how a specific function is implemented. It can be implemented as simple software subroutines using up cycles of the main CPU, or it can be implemented with its own separate CPU-intelligence, buffer-memory, interrupt, and/or DMA capabilities for passing parameters and data back and forth. Math routines, for example, can be software sub-routines or can be implemented in hardware as a separate math chip. The same software-hardware trade-off is true for disk controllers, network communication schemes, and most other functions.

6.1 Board-Level Microcomputers

Representative Board-Level Functions

Input/Output Ports (Serial, and Parallel)

RS232, Current-Loop, TTL
IEEE 488, Triac, Opto-isolated, SPST Relay
Parallel: # lines

Peripheral Controllers

Keyboard and Display
Graphics: Color, B/W, Resolution (pixels)
Cassette, Diskette, Winchester Disk, Paper-Tape
Stepper Motor, Servo Motor
Printers

On-Board Functions

Memory: ROM, PROM, RAM-Dynamic, Static (speed, power consumption)
DMA, Priority Interrupt
Counter/Timer, Time/Calendar
Debug, Diagnostic
Math Hardware: Fixed/Floating Point, Scientific Functions

Other

Communications: Synchronous Data Link Controller (SDLC), Network Interface
Modem Controller: SR, ASR
A/D and D/A Converter: Channels, Accuracy (8-, 12-, 16-bit)
Keypad, Display

Another method of obtaining more flexibility of functions while still using standardized boards is to use plug-in piggy-back board modules, a recent innovation introduced on the Multibus by Intel. Market acceptance of this approach has yet to be determined. A standard single-board computer could, for example, be configured with various input/output port configurations, or with various mass-storage controllers (cassette, diskette, Winchester) by plugging different types of piggy-back boards into an internal bus slot. Furthermore, an engineering team could concentrate on the specialized plug-in board to fit the requirements of its particular application and avoid having to re-design the standardized functional and interconnect hardware and software. The advantages to the designers would be decreased engineering costs, faster time to market, more proven reliability, and greater future flexibility while still maintaining proprietary products and added-value. The disadvantages would be higher overall unit costs, greater board real estate usage, and a less elegant solution to the specific initial design criteria.

Software and Support

Reliable, preconfigured software and training go hand-in-hand with reliable, preconfigured board-level hardware. Time to market and development costs are critical for users in choosing board-level hardware, and software development tools for these boards are very important ingredients. Although initial software development costs and time to market are still primary, the modification, enhancement, and maintenance of software over the life of the product or project are becoming increasingly important factors for users choosing among vendors.

Initial software packages tend to get more complex over time. Users of 8-bit boards for industrial controllers have found that over a few years' span, simple 4K ROM software projects develop into complex patched 16K and 32K projects. Many large-volume users of early 8-bit processors have developed their own real-time executive software and are now living with a lack of system flexibility. But now, as the 8-bit users look to reprogramming for the 16- and 32-bit systems, they are also looking for software development tools that will allow them maximum flexibility to add new functions and maximum portability to move up to newer processor chips. With 8-bit systems, executive software was primarily developed either by customers or third-party software suppliers. With the new 16-bit systems, the semiconductor suppliers themselves are taking a more active role in utility software development, thus putting themselves squarely in the minicomputer skills domain.

The semiconductor companies are in the process of developing multifunction real-time executives for their respective 16-bit CPU chips. Several versions of these basic nucleus executives will probably evolve. One will be a stripped-down version for those who put maximum performance and minimum memory requirements ahead of flexibility. The other will be designed for maximum flexibility and programming ease at the expense of raw speeds and minimum memory requirements. The semiconductor companies may eventually implement much of the systems software in on-chip hardware or firmware, thus increasing the efficiency of the more flexible, full-function executive software and lowering its cost.

6.1 Board-Level Microcomputers

On the other hand, the minicomputer companies, led by Digital Equipment, are emphasizing their well-established, well-proven, thoroughly debugged executive software and are designing Read-Only-Memory versions of these packages. . .

A third software development approach is presented by the small-bus, 8-bit board vendors using popular 8-bit CPU chips. They emphasize the value of assembly or low-level computer programming languages. Their boards are often used for single-function logic replacement that can be handled with fairly simple programs. Even here, the trend is toward using efficient compilers such as "FORTH" or a PROM-based BASIC to ease programming efforts and provide portability. A good set of industrial control subroutines written in a language such as FORTH or a library of routines in various assemblers is needed and being developed to make this alternative more practical. CP/M, a well known 8-bit microcomputer operating system, is being implemented on several small-bus products.

In addition to ease of programming, flexibility, portability, upward mobility, speed, low memory requirements, and low price, the reliability of executive software is critical and is too often taken for granted by the unaware user. Some software projects can tolerate occasional problems, but when controlling a continuous process or when a large discrete manufacturing machine is involved, malfunctioning costs are high.

Today, most board-level products are used in single-function or single-machine control and there is little emphasis on communications among controllers, except in process control environments. As users become more confident in single-use implementation, and as inexpensive local network architectures become available through office-of-the-future developments, down-loading software and communicating real-time results among separate processor stations should begin to receive more emphasis.

The most common higher-level computer language used with board-level projects is still FORTRAN. The tendency is toward using structured languages that allow a more top-down programming approach for those organizations with the discipline to consistently use it. Certainly, most colleges are teaching this approach. Several types of "structured" FORTRAN are available. Pascal, like BASIC, is often too slow for use in real-time systems, unless the Pascal P-code is implemented in microcode. Alternatively, source statements from Pascal and other interpretive languages can be compiled into an intermediate code that is then translated into an assembler language for a specific microprocessor, finally ending up as machine code with no interpreter needed. Much work is being done by universities and independent language developers to enhance Pascal.

The Ada language, promoted by the Department of Defense (DOD), is likely to be an important product in the next decade. It is the first language to be completely specified before a compiler was written, and it has substantial extensions for

real-time processing. The specification process has taken 10 years and all compilers must be tested by the DOD before they can use the Ada name. Western Digital has developed a P-code (Pascal) type Ada chip set, and Intel has implemented Ada as the chip language for the upcoming i432 microprocessor. In addition to languages, the single most important software tool that a programmer will use is the editor, followed by the debugger utility. By now, functions needed in editor software are fairly well standardized, although it still takes a programmer a week or so to familiarize himself with the specific commands of a new editor. The range of capabilities in debugger software, however, is still not standardized and many different levels of functions parade under the same "debugger" title.

A major difference between vendors currently exists with respect to the type of machine that will be used for software development. In the first approach, software can be developed on the actual boards to be used in the final product—the target system—with perhaps an optional PROM burn-in kit. This approach is used by the minicomputer board-level participants. Of course, this system tends to stay a development system rather than being used in final products. In a second approach, software can be developed on a specially constructed "development system" that contains the editor, linker, debugger, and file software for storage of programs on tape, diskette, or hard disk. The software is then down-loaded directly to the RAM of the target boards or is burned into PROM, which is then inserted into the boards. This approach has been pioneered by the semiconductor companies.

With in-circuit emulation (ICE), which comes with most development systems, the CPU chip is removed from the target board and the ICE is plugged in instead. This technique allows the programmer to step through the program and display registers, flags, pin conditions, and even timing signals/diagrams. ICE is useful for designing and debugging boards made in-house from chips, but it is less useful for board-level users.

In a third approach, many large software operations develop software on a larger time-sharing system with efficient editors and compilers, cross-compile the software to the target CPU, and then down-load to a development system, which in turn loads the target boards. Although this approach saves compile-time and allows the use of mainframe-type utilities such as libraries, it does take a great deal of time going from machine to machine in the reiterative program-debug phase. The desire to eliminate steps has resulted in the current emphasis on multiuser, hard disk development systems.

Development systems for board-level products tend to be more highly priced than small commercial systems that can be programmed to do the same tasks. Development systems are available from semiconductor vendors usually for use only with the vendors' chip sets. Systems are also available from independent suppliers. The independents tend to emphasize software for chips from multiple vendors and better price/performance. Development systems are now primarily designed for those users who are designing their own boards from chips, and secondarily for the programming of the assembled boards. Over the next few years, we believe that there will be a tendency to offer lower-priced development systems that are used to

program board-level products primarily. The boards in these new development systems will probably be versions of the target boards themselves. This development will allow the small-sized system integrator or the remote engineering team to develop software for standard board products with entry-level development system costs in line with the size of their initial projects.

Marketing and Distribution

As the board-level market itself has become more structured and mature, the marketing of boards has evolved from simply taking orders and following up advertising inquiries to actively pursuing "design-wins" and searching for potential new projects. A design-win is made when a specific vendor's board or board-family is specified by engineering design and the bid is actually attained from the purchasing department. In early 1980, for example, Intel launched a program titled CRUSH with a goal of at least 4,000 design-wins for its 16-bit 8086 chip family over a two-year period, with many of these design-wins forecast initially from board products. The "CRUSH" program included presentations at 59 customer locations, 38 seminars with a total of 7,000 attendees worldwide, 3 press tours, 12 major articles, and 35 different sales presentations. From the 59 accounts, Intel won 39 designs, lost 7, and registered 15 as undecided.

A board-level sale usually starts with the identification of a new engineering project either by a vendor's sales force, the distributor, or by a direct response to advertising. The vendor's sales force or representatives will often attempt to uncover potential new projects and begin working with the project engineers before the information becomes public. Most leads still come directly to the board vendors from their national advertising, although large distributors are becoming more active because of their own local contacts and their own advertising campaigns. It is important to note that 80 percent of all boards are purchased or funneled through distributors, even though the sale sometimes is handled totally by the vendor's sales representatives.

Typically, a new lead is coordinated by a vendor's regional sales manager who turns it over to one of several distributors in a local area. The distributor salesman contacts the project engineers to determine project specifications and the potential size of the project. The distributors are required, under agreement with their semiconductor suppliers, to also have technical application support personnel available to work with project engineers. These distributor Field Application Engineers (FAEs) and the factory FAEs are a key ingredient in the technical board-level sales. The distributor FAE coordinates the contacts with the customer's engineering team, and the factory FAE almost always is involved at some point in each sale. The distributor FAE ostensibly helps the customer's engineers choose between vendors and types of solutions such as chips, types of boards, or systems. In most cases, though, the customer already has a strong inclination toward one solution or the distributor is working under leads from one vendor.

6.1 Board-Level Microcomputers

Besides working with the engineer or engineering managers, the local salesman often checks in with the purchasing department after engineering evaluation. Small quantities for boards are then purchased, along with a software development system, if needed. This design phase lasts for 6 to 18 months, after which production quantities of boards are finally purchased. Although the clients are looking for a great deal of support during the design phase, the purchasing department sometimes buys production quantities from another source.

The factory development of FAEs is a long-term investment and is a key to gaining long-term market share. The number of FAEs varies greatly among suppliers, as do the method of selection, length of training, and support infrastructure. Direct factory FAE contact is backed up by training programs for both distributor personnel and customer engineers as well as by a consistent and clear long-term product strategy. The emphasis is still on leading edge chip technology at ever-lower prices but the key to product differentiation and design-wins will increasingly rely on FAE and infrastructure support.

Somewhere between the factory or distributor FAE and the OEM is the small independent systems consulting company. These skilled, hardware and software integrators work with end-consumer companies such as manufacturers, the microcomputer systems department, or in conjunction with internal systems integration departments. Several board-based suppliers are making concerted efforts to find and support these mostly young, highly skilled, technical developers.

The customer's decision to buy boards rather than to make them from chips is partly economical, partly psychological, and partly political. The customer tends to buy boards when the cost of electronic components is a small portion (less than 20 percent) of the total cost of the end product, when the volume is low or uncertain, when the primary value added is not electronics, or when the customer does not have established board-level engineering or production resources. The customer's economic decision needs to be based on realistic appraisals of both the investment costs of board development and the complete unit costs of production, testing, and warranty. One of the salesman's main jobs is to be sure the customer is in fact making a realistic appraisal, which sometimes means even looking at unique cost allocating methods within the customer's accounting system.

A few years ago the customer was better off making boards when his volume reached 250 units per year. Now, with increased development costs and decreased unit costs from major suppliers, the crossover point is closer to 1,000 boards per year. Proforma engineering project plans tend to underestimate development costs, difficulty, and time. Plans usually do not factor in the opportunity costs from delayed schedules. Time to market and incorporation of new chip technology are increasingly important factors since most products are introduced in a fast-moving, competitive environment. Many board customers are finding that, with limited engineering resources, their primary value added should be focused in the management of software teams rather than in hardware design.

6.1 Board-Level Microcomputers

Psychological and political factors relate to the "not invented here" syndrome, the desire of engineers to design from basic components, and the concern for job security or departmental influence. For these reasons, board-level make or buy decisions need to be made at the appropriate level in the organization, usually by upper engineering management.

Over the past few years, several approaches to organizing the sales responsibility for board-level products have been tried by different semiconductor suppliers. Since it is mostly an engineer-to-engineer sale, best results have been achieved by sales forces concentrating on selling intelligent components. The salesmen are encouraged to view the board product simply as another component, a chip with more leads or functions. Results are not as good when board products are represented by either salesmen of three-pronged, discrete components or systems-level salesmen, neither of which usually call on engineers. Some companies have tried hiring a separate salesforce for board products, but using an existing salesforce with separate board product quotas has proven less costly and more successful. Smaller suppliers use independent sales representatives and also work with OEMs that develop products for specific vertical markets. Using representatives creates a totally variable direct cost of sales, although the successful companies also have staff and a well-designed plan for continually selling and training their sales representatives. This strategy is coupled with advertising or communication campaigns to the end user.

The 80/20 rule applies to board products as it does elsewhere in business; 20 percent of the accounts create 80 percent of the unit sales. Because of this, some companies have created sales and support teams to focus on specific large accounts. These accounts include internal systems integration departments within large organizations and accounts in specific industries such as automotive, consumer electronics, universities, research labs, petrochemical, and telecommunications.

Some minicomputer companies, such as Computer Automation, use their own salesforces to sell board-level products, but in recent years most of the sales of minicomputer board-level products have gone through industrial distributors. Two years ago Digital began working with Hamilton/Avnet as its exclusive distributor. Recently, Digital began signing up other distributors with strengths in specific local markets. Data General teamed up with the Schweber organization, but has not put much emphasis on board-level products. In early 1980, Data General broke out board-level system and peripheral sales as a separate marketing group and is pursuing OEM accounts.

The three methods of distributing board-level products are through electronic distributors, independent sales representatives, and internal sales organizations. For all three, the primary need is to find, train, and motivate qualified personnel with the required technical, sales, and time management skills needed in this fast-moving market.

6.1 Board-Level Microcomputers

MICROCOMPUTER MARKETS

Market Trends

The major market trends are:

- Introduction of microprocessor intelligence into a seemingly unlimited number of new applications
- Much wider use of microprocessors in discrete and continuous industrial process control
- Interconnection of individual industrial controllers over local networks to monitor and control complete processes
- Shift from buying straight boards to buying packaged hardware/software systems
- Tendency of users to view themselves as software systems developers rather than hardware integrators
- Development of reliable higher-level software systems that remain constant over time but become implemented on increasingly efficient microprocessor systems
- Development of several classes of real time executives from bare bones, low memory requirement executives to full function, high-overhead systems
- Desire for minimal cost entry-level development systems specifically designed for programming board-level products only
- Strong market niche for highly reliable (self-testing, self-correcting, Tandem-type redundancy) board-level controllers for use in critical applications

The introduction of microcomputer intelligence into the industrial environment (production of goods and services) should accelerate over the next few years. The ever lower prices of board- and system-level microcomputers, the increased reliability and performance of microcomputer products, and the greater ease of application programming are combining with the competitive need for increased productivity and faster communications to accelerate the microprocessor growth trends. Microprocessor-based industrial automation is just beginning. Where only a few processes in a factory or laboratory are currently monitored and/or controlled with microprocessors, in a few years we expect microprocessor usage to extend from individual logic replacement to whole processes and interprocess coordination.

6.1 Board-Level Microcomputers

Whereas the majority of the data processing market will continue to use computer systems and the consumer market will design with chips, the industrial market will be the province of boards.

The data processing end-user market has always used integrated hardware and software system-level products. Furthermore, because of the high volume, the high microprocessor value in the products, the desire for proprietary value added, and the competitive price pressures, system-integrator vendors have always manufactured these systems by making their own boards from custom or standardized chips. Recently, though, board-level products, especially new 16-bit products, are being used by smaller system integrator vendors, especially larger OEMs, who see their major value added as software, rather than board design.

The choice of an 8- or 16-bit computer is, in general, based on the computational and throughput requirements of the system. In addition, the availability of software executive systems is critical. Eight-bit units are used in control-oriented applications where only a few functions or processes are to be monitored or controlled, with results sometimes being sent to a 16-bit minicomputer. Sixteen-bit machines are used in more complex multitasking designs or where higher sampling rate, higher-throughput, or computation-oriented tasks are needed.

Sometimes a 16-bit machine is used to provide marketing with a "latest technology" advantage when an advanced 8-bit solution normally would be adequate. Among subjective factors, many designers underestimate the amount of processing power and memory that will be required. If the cost differential is insignificant with respect to the total project, then a larger, more powerful system will be an "insurance policy" against finding, partway through the project, that the initial requirements were underestimated. Equally important is the ability to use proven sophisticated software systems such as those available from the 16-bit minicomputer vendors.

Over the past five years, a significant amount of microprocessor integration and application development has come from small entrepreneurial activities—whether from individuals or from small groups within larger organizations. For these activities, minimal entry costs are very important. For example, by keeping board costs under $500, the small-bus suppliers have made requisition approval much easier for innovative engineering teams. Microcomputer development systems for 8-bit systems have decreased in price, and board-only application development systems without in-circuit emulation and upgradable to 16-bit systems are being introduced for this segment. During 1981, Rockwell, for example, is planning to introduce a new line of small-bus, 8-bit boards that can be programmed with AIM-65 for under $500, complete with keyboard and calculator-style printer. Furthermore, Mostek is introducing CP/M, the most widely used microcomputer disk operating system, for its line of STD-bus boards.

6.1 Board-Level Microcomputers

Price Trends

The continued reduction in semiconductor costs will permit reduced prices on existing board-level designs. As the density of memory and processor chip-devices increases, the same capabilities and memory can be assembled on a board with fewer chips. Since the production and test costs of board products are generally directly related to the number of interconnects, and since fewer interconnects also result in greater reliability, the lower chip count should provide reduced prices and maintenance costs for future generations of systems. Of course, minimal chip counts would either take customers out of the board-level market altogether, as they could easily manufacture boards from chips themselves, or would encourage mass produced, component-type board-level products.

Eight-bit chip families are already far along the learning curve for higher yields and are thus relatively inexpensive. Future 8-bit board price decreases will come from incorporating more functions on one chip, thus decreasing the chip count. Once a board is designed into an end product, however, an unusual amount of inertia is usually encountered in changing boards, especially in high-volume uses. Thus, the initial 8-bit single-board computer products, such as the Intel 80/10, are still sold in high volumes. The 80/10 became a "standard" type product and is sold, like a chip component, in large quantities with a low price that is based more on competitive production costs than on the market price of replacement products or the need to amortize development expenses. The small bus boards are also designed as a standard product. Mostek, for example, recently announced an average 30 percent price reduction on its STD-bus boards.

The standard memory chip presently in use is the 16-Kbit dynamic RAM. This chip should be supplemented by the 64-Kbit RAM chip within the next two years, and that device should be supplanted by the 256-Kbit chip some time after 1985. Thus, memory costs per byte can be expected to decrease by about 18 percent per year over the next five years. The decreased price per byte will be offset by greater usage of memory per system because of the lower prices; furthermore, the newer 16-bit microprocessors will offer direct addressing capacity up to 16 Mbytes.

With 16-bit boards, the anticipated price trends are more complex. Price decreases for memory components will be the same as for 8-bit boards. Production and test costs for 16-bit boards, although higher than those for 8-bit systems, will often not be significantly different because many 8-bit systems already use an extended 16- to 22-bit address bus. The difference will be in the data bus that will be extended to the full 16 bits; the small bus 8-bit system will, however, keep the less expensive 8-bit data bus. In the 16-bit systems, the microprocessor devices are still early in the learning curve and thus significant price decreases per chip can be expected over the next five years. The newer, extended addressing 16-bit chips are currently priced at about $75 each; we expect the price to drop to about $16 by 1985. Even with the greater inherent complexity per chip, the non-memory chip count per board should also decrease over the forecast period as more functions are incorporated per chip.

6.1 Board-Level Microcomputers

In 16-bit board products, both price and chip count decreases should be mitigated by the policy of introducing new chip components with systems "software on silicon" for greater end-system throughput and ease of programming. This technology will introduce another factor into new product innovations along with both more functions per chip and greater bandwidth (16- to 32-bit systems). Thus, one family of 16-bit boards would follow the same trend as 8-bit systems with decreasing costs and chips per system and an efficient, low-memory requirement operating system. Another family would implement a full-function operating system on increasingly more efficient chip sets, keeping pricing per system more constant while performance increases.

Prices of systems made up of 8-bit boards are expected to decline at the rate of nine percent per year through 1985. Decreased component and production costs will be offset by greater memory content, a wider range of standard interface and controller boards, and more software charges. Price-competitive 16-bit board systems are expected to decrease by 11 percent per year and full-performance 16-bit systems by about six percent per year over the forecast period.

Worldwide Market Forecasts

The world market for board-level microcomputer products is expected to grow from an estimated $256 million in 1980 to $837 million in 1985. This figure represents a 27 percent compound annual growth rate. This growth includes the value of annual shipments on a calendar year basis for factory-level shipments of all 8- and 12/16-bit boards. These dollar figures include all board-level hardware; card-cages (and power supplies or cabinetry); and system software offered by the suppliers. The figures do not include sales of peripherals, software, or services associated with the application-oriented, end-use system. The figures also do not include sales by board manufacturers that do not offer a CPU product.

Unit figures for board-level products are derived from the number of CPU boards shipped each year, which is a reasonably accurate estimate of the number of board-level systems installed, since the vast majority of applications have only one CPU board per system.

The average selling prices (ASPs) are thus dollars per CPU board, which is a reasonable estimate of dollars per installed system of board-level products. This method allows a calculation of ASP per system regardless of whether the functions are implemented on one board or six boards.

Unit shipments of board-level products are expected to increase from 234 thousand units in 1980 to 1.2 million units by 1985, a compound annual growth rate of 39 percent. Complete historical figures of units, dollars, and ASPs, and forecasts for the 1981 to 1985 period are given in Tables 6.1-1 through 6.1-3. Tables 6.1-4 and 6.1-5 show estimated market share for units and value by board level product type. Table 6.1-6 gives the estimated percentage distribution of board-level microcomputer revenues by region of the world. Figures 6.1-2 and 6.1-3 graphically show these market share figures for CPU-units and revenues, respectively.

6.1 Board-Level Microcomputers

Table 6.1-1

ESTIMATED WORLDWIDE MARKET FOR BOARD-LEVEL PRODUCTS
(Thousands of CPU Units)

	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	Compound Annual Growth Rate 1980-85
8-Bit Small Bus	-	5	19	40	57	90	130	180	250	340	42.9%
8-Bit Large Bus	17	30	40	78	110	160	220	290	380	490	34.8%
8-Bit Sub-Total	17	35	59	118	167	250	350	470	630	830	37.8%
16-Bit Limited Function	10	22	31	48	58	98	162	215	275	343	42.7%
16-Bit Full Function	-	-	2	3	9	15	22	32	44	58	45.2%
16-Bit Sub-Total	10	22	33	51	67	113	184	247	319	401	43.0%
Total CPU-Board Units	27	57	90	169	234	363	534	717	949	1,231	39.4%

Source: DATAQUEST, Inc.

Table 6.1-2

ESTIMATED WORLDWIDE MARKET FOR BOARD-LEVEL PRODUCTS
(Millions of Dollars)

	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	Compound Annual Growth Rate 1980-85
8-Bit Small Bus	$ -	$ 2	$ 3	$ 17	$ 25	$ 35	$ 47	$ 59	$ 75	$ 90	29.2%
8-Bit Large Bus	17	30	46	66	90	130	161	191	230	270	24.6%
8-Bit Sub-Total	$ 17	$ 32	$ 49	$ 83	$115	$165	$208	$250	$305	$ 360	25.6%
16-Bit Limited Function	$ 12	$ 29	$ 46	$ 73	$ 95	$130	$180	$225	$260	$ 268	23.0%
16-Bit Full Function	-	-	8	11	46	67	92	128	167	209	35.4%
16-Bit Sub-Total	$ 12	$ 29	$ 54	$ 84	$141	$197	$272	$353	$427	$ 477	27.6%
Total Factory Revenues	$ 29	$ 61	$103	$167	$256	$362	$480	$603	$732	$ 837	26.7%
Trade Discount Dollars	7	14	25	40	62	87	115	145	176	201	
Total Market Revenue	$ 36	$ 75	$128	$207	$318	$449	$595	$748	$907	$ 1,038	

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

Table 6.1-3

ESTIMATED WORLDWIDE MARKET AVERAGE SYSTEM PRICE
FOR BOARD-LEVEL PRODUCTS

	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	Compound Annual Growth Rate 1980-85
8-Bit Small Bus	-	$ 400	$ 160	$ 420	$ 440	$ 390	$ 360	$ 330	$ 300	$ 270	(9.3%)
8-Bit Large Bus	$ 1,000	$ 1,000	$ 1,150	$ 850	$ 820	$ 810	$ 730	$ 660	$ 600	$ 550	(7.5%)
8-Bit Average	$ 1,000	$ 910	$ 830	$ 700	$ 690	$ 660	$ 590	$ 530	$ 480	$ 430	(9.0%)
16-Bit Limited Function	$ 1,200	$ 1,320	$ 1,480	$ 1,520	$ 1,640	$ 1,350	$ 1,200	$ 1,050	$ 950	$ 780	(11.5%)
16-Bit Full Function	-	-	$ 4,000	$ 3,700	$ 5,100	$ 4,500	$ 4,200	$ 4,000	$ 3,800	$ 3,600	(6.0%)
16-Bit Average ASP	$ 1,200	$ 1,320	$ 1,640	$ 1,650	$ 2,100	$ 1,740	$ 1,480	$ 1,350	$ 1,230	$ 1,190	(10.7%)
All Board Level Products ASP	$ 1,070	$ 1,070	$ 1,140	$ 990	$ 1,090	$ 1,000	$ 900	$ 840	$ 770	$ 680	(9.0%)

Source: DATAQUEST, Inc.

Table 6.1-4

ESTIMATED SHARE OF MARKET
BY BOARD-LEVEL PRODUCT TYPE
(Percent of Units)

Market Segment	1978	1979	1980	1981	1985
8-bit Small Bus	21 %	24 %	24 %	25 %	28 %
8-bit Large Bus	43	46	47	44	39
8-bit Subtotal	64 %	70 %	71 %	69 %	67 %
16-bit Limited Function	34 %	28 %	25 %	27 %	28 %
16-bit Full Function	2	2	4	4	5
16-bit Subtotal	36 %	30 %	29 %	31 %	33 %
Total	100 %	100 %	100 %	100 %	100 %

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

Table 6.1-5

ESTIMATED SHARE OF MARKET
BY BOARD-LEVEL PRODUCT TYPE
(Percent of Value)

Market Segment	1978	1979	1980	1981	1985
8-bit Small Bus	3 %	10 %	10 %	10 %	11 %
8-bit Large Bus	45	40	35	37	32
8-bit Subtotal	48 %	50 %	45 %	47 %	43 %
16-bit Limited Function	45 %	43 %	37 %	34 %	32 %
16-bit Full Function	7	7	18	19	25
16-bit Subtotal	52 %	50 %	55 %	53 %	57 %
Total	100 %	100 %	100 %	100 %	100 %

Source: DATAQUEST, Inc.

Table 6.1-6

BOARD-LEVEL MICROCOMPUTER MARKET
ESTIMATED REGIONAL DISTRIBUTION
(Percent)

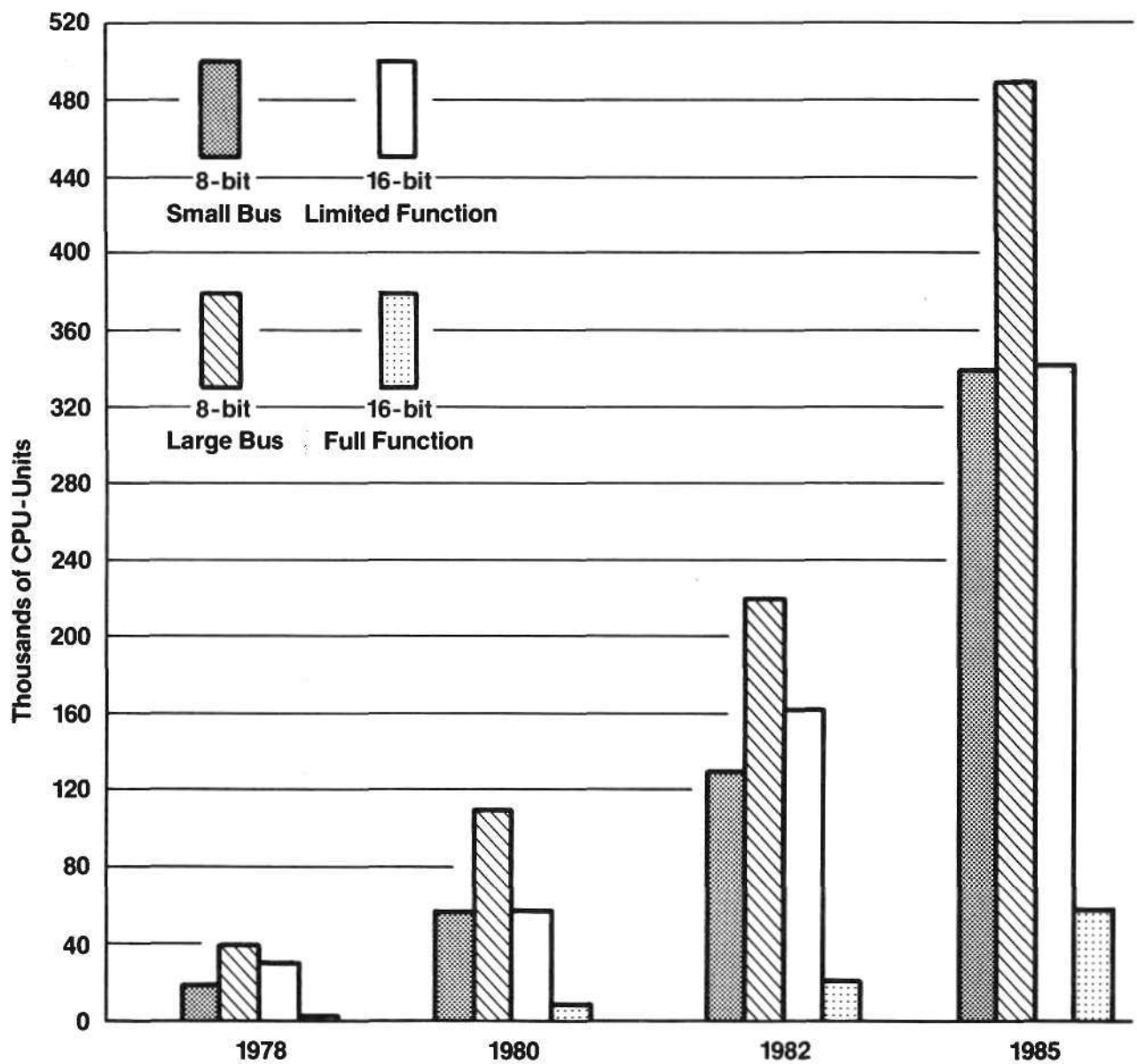
Region	1978	1980	1982	1985
United States	62 %	56 %	51 %	48 %
Canada	3 %	3 %	3 %	3 %
Western Europe	25 %	29 %	31 %	33 %
Japan	7 %	8 %	10 %	11 %
ROW	3 %	4 %	5 %	5 %
Total	100 %	100 %	100 %	100 %

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

Figure 6.1-2

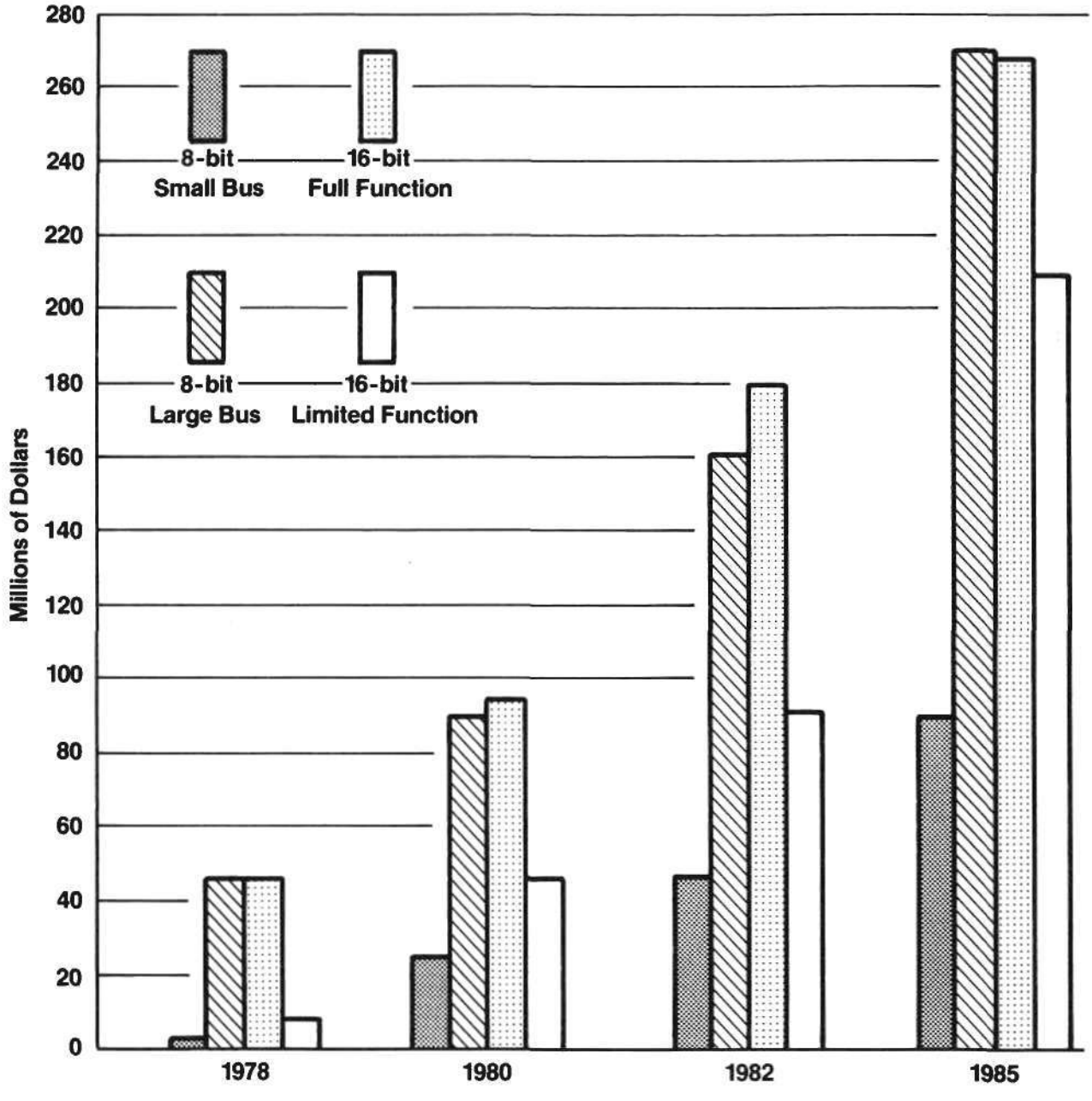
ESTIMATED WORLDWIDE MARKET FOR BOARD-LEVEL PRODUCTS
(Thousands of CPU-Units)



Source: DATAQUEST, Inc.

Figure 6.1-3

ESTIMATED WORLDWIDE MARKET FOR BOARD-LEVEL PRODUCTS
(Millions of Dollars)



Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

The 8-Bit Board Market

The 8-bit board market is expected to grow from approximately 167,000 units in 1980 to 830,000 units in 1985, a compound annual growth rate of 38 percent. The 8-bit small bus boards have been increasing dramatically from a very small base over the past two years. The unit growth rate in the next five years for small-bus boards is forecasted to be only slightly more than for large-bus boards. This similar growth rate is due to similar rates of price decreases as well as recently introduced piggy-back flexibility, and operating system software available with large-bus boards. But, as the lowest price board-level system, the small-bus products should still do very well, especially for single-function logic replacement.

The percent unit and revenue breakdowns of the 8-bit market by application are is given in Table 6.1-7 and 6.1-8. The 8-bit market will be driven by the industrial automation application segments that will require nearly half the systems by 1985. All segments will show increases in absolute number of units due to the rapid growth rate. Because of large untapped potential applications, communications, specialized data acquisition and control, and industrial automation are expected to grow faster than the overall market, reducing market share of the instructional and laboratory control areas. The average selling price for systems in the industrial automation area is expected to drop more than for other applications—since this a very price-sensitive area—thus keeping the percent of value fairly constant for industrial control. Also, this area is expected to see a relatively greater amount of lower-priced small-bus boards than other segments.

6.1 Board-Level Microcomputers

Table 6.1-7

ESTIMATED WORLDWIDE 8-BIT BOARD-LEVEL
MICROCOMPUTER MARKET BY APPLICATION
(Percent of Units)

Application Area	1978	1980	1982	1985
Business Data Processing	4 %	5 %	5 %	5 %
Communications	5	6	7	9
Design and Drafting	1	1	1	1
EDP Support	2	2	2	2
Industrial Automation	37	44	45	47
Instructional	10	10	9	7
Laboratory and Computational	17	12	9	9
Specialized Data Acquisition and Control	8	8	19	13
Specialized Data and Word	2	2	2	2
Other	14	8	7	5
Total	100 %	100 %	100 %	100 %
Annual Shipments (Thousands of CPU Units)	59	167	350	830

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

Table 6.1-8

ESTIMATED WORLDWIDE 8-BIT BOARD-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Value)

Application Area	1978	1980	1982	1985
Business Data Processing	5 %	6 %	6 %	6 %
Communications	6	7	8	11
Design and Drafting	1	1	1	1
EDP Support	2	2	2	2
Industrial Automation	34	40	40	41
Instruction	5	5	5	4
Laboratory & Computational	25	22	20	16
Specialized Data Acquisition and Control	8	8	10	13
Specialized Data and Word	2	2	2	2
Other	12	7	6	4
Total	100 %	100 %	100 %	100 %
Annual Revenues (Millions of Dollars)	$ 49	$115	$208	$360

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

The 16-Bit Board Market

The 16-bit board market is expected to grow from an estimated 67,000 units in 1980 to approximately 400,000 units in 1985, a compound annual growth rate of 43 percent. DATAQUEST has divided the 16-bit board market into two subsegments, the "limited-function" boards and the "full-function" boards.

The "full-function," 16-bit board market segment is defined as including boards that offer a full-function, high-overhead operating system and executive along with a full complement of coprocessor functions and an expanded addressing capability. The actual definition will change over time as more capability is introduced at the high end and as more standard functions are incorporated into the definitions of "limited" function. At present, the full-function definition includes: a minimum 18-bit address bus; memory management or input/output processing for relocation, segmentation, and level-protection; and numeric processing to include at least hardware multiply and divide. In 1980, the full-function boards included the LSI-11/23 with memory management and the Hewlett-Packard 1000-L series boards. Intel's iSBC 86/12 board, although meeting some of the criteria, has not been included because of limited memory protection and numeric processing, the evolving executive software during 1980, and the announced plans to introduce higher-function boards.

The full-function, 16-bit board market, starting from a very small base in 1980, is expected to grow at the fastest rate of all board segments over the forecast period. In addition, price decreases are expected to be lowest for this market segment because of the continued introduction of new "software-on-silicon" and advanced functionality. Thus, the revenue for the full-function, 16-bit board segment is expected to grow from approximately $46 million in 1980 to $209 million in 1985, a compound annual growth rate of 35 percent.

The "limited-function" segment of the 16-bit board market will emphasize lean, efficient, executive software and the incorporation of more functions per chip rather than full-functionality per board. This segment will be the higher-volume, lower-cost board area with performance and functionality closely matched to specific design needs. Because of the recent introduction of new 16-bit chips, the prices of limited-function systems are still early on the learning-curve and thus prices for this segment are expected to decline more than for other board markets, with an annual compound rate of 11 percent. The revenue for the limited-function, 16-bit board segment is expected to grow from $95 million in 1980 to $268 million in 1985, a compound annual growth rate of 23 percent.

The percent unit and revenue breakdown of the 16-bit market by application area are given in Tables 6.1-9 and 6.1-10. During 1980, the laboratory segment was the major influence, mostly due to the large historical influence of Digital's PDP-11 family. By 1985, however, the industrial automation segment is expected to be the major influence, although not as much as for the 8-bit market. The communications,

specialized data acquisition and control, and laboratory segments should all have about equal influence in the 16-bit markets. Communications and laboratory control are expected to use more of the full-function boards, with data acquisition and industrial automation using more of the limited-function systems.

During 1980, the minicomputer companies supplied most of the 16-bit board products. Although many products were introduced, the semiconductor companies were not a strong influence in the 1980 16-bit market. But with many successful design-wins during 1980, the die is already cast for codominance of this board market by semiconductor and minicomputer companies over the forecast period. Minicomputer companies have a competitive advantage with executive software systems, and upward compatibility with existing minicomputer sytems. Semiconductor companies offer the latest technology, chip-level products, and a strong software development effort.

International Markets

During 1980, an estimated 59 percent of board-level microcomputer products were shipped to customers in North America (see Table 6.1-6). By 1985, this is expected to shift to a 51 percent shipment rate, with Western Europe taking 33 percent and Japan 11 percent. The West European market has been especially strong for board products. The customers tend to be larger companies and the team sales approach is used—a supplier will often send a four-person team to spend several weeks with a customer. The customer's decision-making process is thus usually technically very complete with a resultant tendency to use more conservative, established technology.

Siemens AG, in conjunction with the West German postal authority, has defined a pin interface for boards called the Euro-Card standard. It is more expensive, but intrinsically more reliable than the traditional gold-edge card connector. Siemens has had an aggressive pricing and marketing program for its boards and as a result dramatically increased sales in 1980. In addition, several U.S.-based suppliers, including Mostek, Motorola, Rockwell, and Zilog (later withdrawn) have introduced Euro-Card boards. Motorola, for example, recently introduced West European versions of its Exorbus and Versabus (on a double-sized card) at the Electronika show in Munich, West Germany.

6.1 Board-Level Microcomputers

Table 6.1-9

ESTIMATED WORLDWIDE 16-BIT BOARD-LEVEL
MICROCOMPUTER MARKET BY APPLICATION
(Percent of Units)

Application Area	1978	1980	1982	1985
Business Data Processing	8 %	10 %	8 %	6 %
Communications	10	10	12	14
Design and Drafting	-	-	1	2
EDP Support	9	5	5	4
Industrial Automation	25	20	27	36
Instructional	4	3	2	2
Laboratory and Computational	32	40	29	15
Specialized Data Acquisition and Control	6	6	10	15
Specialized Data and Word	1	1	1	2
Other	5	5	5	4
Total	100 %	100 %	100 %	100 %
Annual Revenues (Thousands CPU Units))	33	67	184	401

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

Table 6.1-10

ESTIMATED WORLDWIDE 16-BIT BOARD-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Revenue)

Application Area	1978	1980	1982	1985
Business Data Processing	8 %	9 %	8 %	7 %
Communications	10	11	13	17
Design & Drafting	-	-	1	2
EDP Support	9	5	4	3
Industrial Automation	23	17	24	32
Instructional	3	2	2	1
Laboratory and Computational	35	46	34	19
Specialized Data Acquisition and Control	6	5	9	13
Specialized Data and Word	1	1	1	2
Other	5	4	4	3
Total	100 %	100 %	100 %	100 %
Annual Revenues (Millions of Dollars)	$ 54	$141	$272	$477

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

MICROCOMPUTER TECHNOLOGY

Microcomputer performance and prices are driven primarily by semiconductor LSI technology. Since direct costs are a function of the number of board interconnections needed to configure a given set of functions, the costs of microcomputer boards can be expected to continue to decline. But total costs of a board project must also include development costs and opportunity costs from a longer time to market. These lost opportunity costs usually interact with other marketing and product decisions to result in a smaller long-term share of market.

The advances in semiconductor technology can be used in three ways: to increase the number of functions integrated on a chip while keeping the performance constant; to increase the performance through wider band width or faster cycle time while keeping the functions constant; or to provide a higher level of functional integration through software-on-silicon to make application programming easier. The first way results in lower direct costs, while the others result in greater value added by the semiconductor suppliers. For many applications, greater throughput is not really needed; instead increased reliability and ease of programming through the use of standardized routines has more incremental value to the customer and is a better application of technology.

The trend toward software-on-silicon means that the semiconductor companies have had to hire and manage a new type of professional, the system software integrator. In the 8-bit world, and up to now with 16-bit chips, system software has been left up to third-party participants. These skills, of course, are already the forte of the minicomputer vendors and they have been quickly integrating backwards into semiconductor technology.

Another important trend in semiconductor technology is the rapid reduction of lead times for developing new iterations of microprocessor chips. This trend is due primarily to the use of computers to aid in the logic and design of new microprocessors. These are the CAD/CAM techniques (for computer-aided-design and computer-aided-manufacturing).

Besides CAD/CAM, gate array technology is helping to decrease chip development time. In gate-array chips, the first six layers of transistor-level deposits on silicon are identical in all chips. Thus, an inventory of known good wafers can be built up. The wafers are then customized by unique interconnections of the basic transistor levels through the remaining five or more layers of deposits.

The savings in development time is dramatic using both CAD/CAM and gate arrays. Design turnaround time in the industry has typically been six months to two years. IBM recently made major investments in three automated, quick turnaround fab lines that are reported to have reduced turnaround time from months to between eight hours and two weeks.

6.1 Board-Level Microcomputers

The rapid reduction in microprocessor chip development time means that there will be an eventual move from standardized microprocessor chips to chips much more customized to specific applications. Thus, the chip designer will become more of a hardware integrator, leaving to third parties the higher and higher levels of application programming.

In chip packaging, the familiar dual in-line (DIP) pin package is beginning to face more competition from the leadless chip-carriers. The improved board densities the leadless chip-carriers offer have encouraged their use with very large-scale integrated circuits, usually with the help of sockets or a small motherboard. New types of PC boards are presently being designed that should allow reliable direct soldering of leadless chip-carriers onto the board. The large amount of equipment now installed for chip fabrication, automatic chip insertion, and wave soldering will keep the DIP package as the predominant packaging mode over the next few years.

There is recent increased interest in low-power boards and memories using CMOS technology. National Semiconductor recently started shipping quantities of a low-power, 8-bit chip with a Z80 instruction set and an 8085-like multplexed address bus. The interest is for uses where portability, battery power, or minimal power supplies are important and will be especially useful with the small bus 8-bit boards because of their small size.

COMPETITION

Competitive Environment

The total board-level microcomputer market of $240 million in 1980 is rather small, only 1.5 percent of the $16 billion total for the small computer industry. DATAQUEST's projected compound annual growth rate, based on historical trends, of 27 percent in dollar volume over the next five years is also not spectacular. The real importance of this market lies first in its unrealized potential, and second in its strategic positioning as the major battleground between semiconductor and minicomputer suppliers.

Unrealized potential revolves primarily around the need for increased industrial productivity for the 15 million productive employees working in manufacturing companies in the United States today. Based on present trends, DATAQUEST projects a cumulative board-level market of $3.2 billion over the next five years from 1981 to 1985. But, if each productive user were given the microprocessor intelligence equivalent to a $2,000 personal computer over the next five years, the total market for manufacturing automation alone would be $30 billion. Realizing this potential requires designing products and marketing programs that meet the needs and attitudes of users in the manufacturing environment. There is obviously a great need, but also a great deal of attitudinal inertia and adherence to existing technologies. Of course, competition in this market already exists from

programmable controllers sold by companies such as Allen-Bradley, Foxboro, General Electric, Honeywell, Leeds & Northrup, and Texas Instruments. The 1980 programmable controller market is estimated at $200 million.

Another area of unrealized potential is that of selling boards to be used in very small business computers (VSBC). Up to now, VSBC suppliers have manufactured their own boards from chips. This market is very price-competitive and thus product cost savings are very important. There is a tendency, though, for larger OEMs to integrate their own systems at the board level, especially with stand-alone specialized CRT workstations. They can integrate standard boards from several sources with prefabricated CRTs and third-party software systems. As a result, system integration tends to migrate from the supplier level to the OEM, who is closer to the end user. The board supplier and the OEM can then share the extra margin made available by eliminating the independent system integrator.

As chips become more powerful, board-level products will be able to develop into the traditional minicomputer realms. In the competitive environment, the semiconductor company's strengths are in the advanced technology expressing itself with 16- and 32-bit microcomputer chips, in the engineer-oriented salesforce, and in the control of industrial distribution. Semiconductor company weaknesses are in limited operating system software, limited field service force, and limited end-user knowledge or orientation. Minicomputer company strengths are in their well-proven system software, boards that are minicomputer compatible, strong field service support, established OEMs, and a strong end-user orientation. Minicomputer company weaknesses are in limited semiconductor technology, generally unavailable microprocessor chips for users to build their own boards, limited influence with industrial distributors, a salesforce that is generally not engineering-oriented, and the need to preserve their minicomputer bases.

Of course, semiconductor companies that wish to be leaders in the board-level marketplace are now investing heavily in developing operating system software. The minicomputer companies, on the other hand, have been committing resources in capital and talent to building their semiconductor technology and manufacturing bases.

A few years ago, competition for a given customer was rather limited. This status has changed as semiconductor companies have expanded their product lines, support, and market objectives. Competition for large, traditional OEM customers is now fierce.

DATAQUEST believes that over the long term, semiconductor suppliers will dominate the bus-compatible board market sold through industrial OEMs and system integration. The semiconductor companies can also be expected to offer board-level systems packaged as boxes and integrated systems with appropriate software utilities. The minicomputer suppliers will move farther toward end-user markets and offer packaged systems including peripherals and application software. Boards will be offered to large end-user and system integrators, but will be bundled with software and allow upward compatibility with minicomputer and super mini systems.

6.1 Board-Level Microcomputers

Market Share

Tables 6.1-11 through 6.1-18 present market share estimates for the 8-bit board-level and 16-bit board-level markets through 1980. These tables list the vendors in sequence by their estimated 1980 share of market. As expected, the semiconductor companies dominate the market in the 8-bit area. Mostek, with a Z80 system on the STD bus, showed surprising growth through the past year while the rest of the 8-bit market brought in a sluggish performance. The large bus 8-bit market slowed dramatically in the fourth quarter of 1980 due to the overall economic outlook. The West European market continued strong, especially with the forceful entry of Siemens. The slowing of the U.S. market resulted in intense bidding and price cutting "on the street" to be sure inventory was off the shelf by the end of the year, so distribution returns would not be a problem. Rockwell continued to do well with the AIM-65, complete with keyboard, display, and printer, and should do well in 1981 with its new line of compatible microflex small-bus boards that are available either with edge-card or Euro-card connectors. Intel licensed their production of 8- and 16-bit boards to EMM Sesco to produce military, ruggedized versions of their multibus products. MOS-Technology, a subsidiary of Commodore, stopped production of its KIM-bus boards. Although Zilog announced it was out of the board business and let some field people go, residual orders for their existing boards were surprisingly strong.

In the 16-bit area, Digital did very well in 1980. DATAQUEST estimates that it shipped 9,000 LSI 11/23 boards in calendar 1980. Intel also showed excellent growth from the results of its concentrated push on the 8086. The resultant design wins should also mean a good year for 1981. Although Motorola introduced the M68000 Versabus board, quantity shipments did not start in 1980.

This year, 1981, should see the introduction of the 32-bit i432 chips and prototype boards from Intel with some of the promised software-on-silicon. Western Digital is readying the microcoded Ada chip set. We expect that both Hewlett-Packard and Digital will announce a 32-bit chip. Surprisingly, both units may first be used in desk-top personal, business-oriented computers, most likely with sophisticated graphics.

The year 1981 should see the delayed 16-bit boards from semiconductor companies begin to grab market share. The big question is how this increased microprocessor power, due to the shift from an 8-bit into a 16/32-bit world, will be applied and exactly what new applications will begin to open up in the market.

6.1 Board-Level Microcomputers

Table 6.1-11

8-BIT BOARD-LEVEL MICROCOMPUTERS
ESTIMATED WORLDWIDE SHIPMENTS

Supplier**	CPU Units Shipped (Thousands) 1976	1977	1978	1979	1980
Intel	6.0	10.0	20.0	38.0	48.0
National Semiconductor	0.5	3.0	5.7	11.6	15.1
Motorola	0.5	2.0	4.2	7.2	10.0
Mostek	*	*	1.0	2.9	10.0
Siemens	*	*	*	*	17.0
Rockwell	*	*	1.0	15.0	19.0
Prolog	1.0	1.5	2.5	4.0	7.1
Zilog	*	*	2.4	4.7	3.3
Synertek	*	*	3.0	9.0	12.0
MOS-Technology	*	*	10.0	8.0	3.0
Other	9.0	18.5	9.2	17.6	22.5
Total	17.0	35.0	59.0	118.0	167.0

*Included in other
**Ranked in order by 1980 revenues

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

Table 6.1-12

8-BIT BOARD-LEVEL MICROCOMPUTERS
ESTIMATED WORLDWIDE REVENUES

Supplier**	Revenue (All Boards) (Millions of Dollars) 1976	1977	1978	1979	1980
Intel	$ 4.8	$ 10.0	$ 18.5	$ 33.0	$ 40.0
National Semiconductor	0.3	3.0	5.1	9.6	11.2
Motorola	0.4	2.0	5.0	5.5	9.1
Mostek	*	*	0.4	3.6	9.1
Siemens	*	*	*	*	8.1
Rockwell	*	*	0.4	5.3	7.1
Prolog	1.0	1.4	2.7	3.7	5.3
Zilog	*	*	2.5	4.3	3.6
Synertek	*	*	1.3	1.7	2.3
MOS-Technology	*		2.0	1.6	0.6
Other	10.5	15.6	11.1	14.7	18.6
Total	$ 17.0	$ 32.0	$ 49.0	$ 83.0	$115.0

*Included in other
**Ranked in order by 1980 revenues

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

Table 6.1-13

8-BIT BOARD-LEVEL MICROCOMPUTERS
ESTIMATED WORLDWIDE SHARE OF MARKET

Supplier**	Share of Units (Percent) 1976	1977	1978	1979	1980
Intel	35 %	29 %	34 %	32 %	29 %
National Semiconductor	3	9	10	10	9
Motorola	3	6	7	6	6
Mostek	*	*	2	3	6
Siemens	*	*	*	*	10
Rockwell	*	*	2	13	11
Prolog	6	6	4	3	4
Zilog	*	*	4	4	2
Synertek	*	*	5	8	7
MOS-Technology	*	*	17	7	2
Other	53	50	15	14	14
Total	100 %	100 %	100 %	100 %	100 %

*Included in other
**Ranked in order by 1980 revenues

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

Table 6.1-14

8-BIT BOARD-LEVEL MICROCOMPUTERS
ESTIMATED WORLDWIDE SHARE OF MARKET

Supplier**	Share of Revenue (Percent) 1976	1977	1978	1979	1980
Intel	28 %	31 %	38 %	40 %	35 %
National Semiconductor	2	9	10	12	10
Motorola	2	6	10	7	8
Mostek	*	*	1	4	8
Siemens	*	*	*	*	7
Rockwell	*	*	1	6	6
Prolog	6	4	6	5	5
Zilog	*	*	5	5	3
Synertek	*	*	3	2	2
MOS-Technology	*	*	4	2	-
Other	62	50	22	17	16
Total	100 %	100 %	100 %	100 %	100 %

*Included in other
**Ranked in order by 1980 revenues

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

Table 6.1-15

16-BIT BOARD-LEVEL MICROCOMPUTERS
ESTIMATED WORLDWIDE SHIPMENTS AND REVENUES
U.S.-BASED SUPPLIERS

	CPU Units Shipped (Thousands)				
Supplier*	1976	1977	1978	1979	1980
Digital Equipment	6.0	9.0	15.0	28.0	38.0
Hewlett-Packard	-	-	2.0	2.5	3.0
Intel	-	-	-	1.5	4.5
Texas Instruments	1.0	3.0	6.0	7.0	7.5
Intel	-	-	-	1.5	4.5
Data General	0.2	1.3	2.0	2.5	3.0
Computer Automation	0.5	1.0	1.2	1.5	1.6
Other	2.3	4.7	6.8	8.0	9.4
Total	10.0	19.0	33.0	51.0	67.0

*Ranked in order by 1980 revenues

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

Table 6.1-16

16-BIT BOARD-LEVEL MICROCOMPUTERS
ESTIMATED WORLDWIDE SHIPMENTS AND REVENUES
U.S. BASED SUPPLIERS

Supplier*	Revenue (All Boards) (Millions) 1976	1977	1978	1979	1980
Digital Equipment	$ 7.2	$12.0	$25.0	$46.0	$ 90.0
Hewlett-Packard	-	-	8.0	9.8	12.0
Intel	-	-	-	3.9	12.0
Texas Instruments	1.2	4.5	8.5	9.8	10.2
Data General	0.2	2.0	3.0	3.5	4.2
Computer Automation	0.7	1.2	2.0	2.2	2.5
Other	2.7	5.3	7.5	8.8	10.1
Total	$12.0	$25.0	$54.0	$84.0	$141.0

*Ranked in order by 1980 revenues

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

Table 6.1-17

16-BIT BOARD-LEVEL MICROCOMPUTERS
ESTIMATED WORLDWIDE SHARE OF MARKET

Supplier*	Share of Units (Percent) 1976	1977	1978	1979	1980
Digital	60 %	47 %	45 %	55 %	57 %
Hewlett-Packard	-	-	6	5	4
Intel	-	-	-	3	7
Texas Instruments	10	16	18	14	11
Data General	2	7	6	5	4
Computer Automation	5	5	4	3	2
Other	23	25	21	15	15
Total	100 %	100 %	100 %	100 %	100 %

*Ranked in order by 1980 revenues

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

Table 6.1-18

16-BIT BOARD-LEVEL MICROCOMPUTERS
ESTIMATED WORLDWIDE SHARE OF MARKET

	Share of Revenue (Percent)				
Supplier*	1976	1977	1978	1979	1980
Digital	60 %	48 %	46 %	55 %	64 %
Hewlett-Packard	-	-	15	12	8
Intel	-	-	-	5	8
Texas Instruments	10	18	16	12	7
Data General	2	8	6	4	3
Computer Automation	6	5	4	3	2
Other	22	21	13	9	8
Total	100 %	100 %	100 %	100 %	100 %

*Ranked in order by 1980 revenues

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

MICROCOMPUTER PRODUCTS

Table 6.1-19 lists the 8-bit board-level CPU products and vendors. Since 1978, 17 vendors have left this marketplace. Most notable among these are: Apple Computer, Fairchild, IMSAI, MITS, and Warner & Swasey. On the other hand, 18 vendors have entered the market. Most notable of these are: RCA, Rockwell, and the System Group. This high turnover is indicative of the rapidly changing market and the resources needed in finance, marketing, and product planning.

Table 6.1-20 lists the 16-bit board-level CPU products and vendors. Since 1978, only two vendors, Fairchild and Perkin-Elmer, have withdrawn from this market; however, mostly due to the availability of new 16-bit chips from their own semiconductor facilities, seven new vendors have joined the group. These recent 16-bit board-level vendors include Advanced Micro Computer, Hewlett-Packard, Motorola, Plessey Microsystems, and Western Digital. So far, mostly major technology-oriented vendors have entered the 16-bit market. Standard 16-bit chips are now available and as soon as standardized 16-bit operating systems and languages also become available, we expect that many more independent board suppliers will enter this market.

Table 6.1-21 lists the descriptions of the abbreviations used in the options column for Tables 6.1-19 and 6.1-20. Not all the options listed in this table are actually used, but they are included as possible future categories. It should also be noted that most of these options can themselves be subdivided into finer levels of resolution. For example, serial ports can be RS232 and/or current-loop among others, while parallel lines can be grouped into ports and programmed with on-board ROM. Some option categories such as the memory management unit need further clarification in the future because different sets of features are included under this heading by various suppliers. As these features become more standardized and implemented with on-chip logic, future classification should become easier.

6.1 Board-Level Microcomputers

Table 6.1-19

8-BIT BOARD-LEVEL MICROCOMPUTER PRODUCTS

Supplier	Model	Bus Structure	CPU Used	Clock Rate MHz	RAM	ROM	Maximum On Board Options
Advanced Micro Computers	95/4006	Multi -	8080	4.0	4K	16K	1S, 48P, 5T, 8I, APU
	95/4010	Multi -	AM 8085A-2	4.0	-	4K	2S, 24P, 5T, 8I, MMU, 20A
Analog Devices	MAC-4000	None	8085A	2.0	2K	-	1S, 16P, 0T, 0I, 12AN
California Computer Systems	2810A	S-100	Z80A	2.0-4.0	-	2K	1S, 0P, 0T, 0I
Control Logic	CCS-1143	none	Z80	2.0	1K	16K	1S, 50P, 1T, 0I
	MMI-MSC	Poly	Z80	2.0	1K	2K	4S, 0P, 0T, 0I
Creative Micro Systems	9609	Exor-	6809	2.0	1K	6K	2S, 40P, 3T, 8I
	9600-A	Exor-	6802	2.0	1K	6K	2S, 40P, 3T, 8I
Cromemco	SCC	S-100	Z80	4.0	1K	8K	1S, 24P, 5T, 0I
	ZPU	S-100	Z80	4.0	-	-	0S, 0P, 0T, 0I
Digicomp Research	PASCAL - 100	S-100	Z80/WD 9000	2.5	-	-	0S, 0P, 0T, 0I
Diversified Technology, Inc.	CBC 800/216S	C-Bus	NSC 800	4.00	16K	32K	1S, 44P, 4T, 20I, LP, TMP
	CBC 800/216T	Multi-	NSC 800	4.00	16K	32K	1S, 44P, 4T, 20I, LP, TMP
EMM Seseo	SECS 80/101	Multi-	8080A	2.05	1K	8K	1S, 48P, 0T, 1I, RGD
General Micro Systems	GMS-6506	Exor-	6502	1.0	8K	16K	1S, 16P, 2T, 8I
	GMS-6525	Exor-	6802	4.0	8K	16K	1S, 16P, 2T, 8I
	GMS-6526	Exor-	6809	4.0	8K	16K	1S, 16P, 2T, 8I
	GMS-6527	Exor-	Z80	1.0	8K	16K	1S, 16P, 2T, 8I
Godbout Electronics	CPU-Z	S-100	Z80A	2.0-6.0	4K	4K	0S, 0P, 0T, 8I, 24A
	CPU-8085/8088	S-100	8085-8080	2.0-5.0	-	-	0S, 0P, 0T, 8I, 24A
	System Supported	S-100	Support-Bd	N/A	4K	4K	1S, 0P, 2T, 8I, APU
Heurikon Corporation	MLZ-80	Multi-	Z80	2.00	73K	8K	2S, 32P, 4T, 8I, 20A, F, APU
	MLZ-80A	Multi-	Z80	4.00	73K	8K	2S, 32P, 4T, 8I, 20A, F, APU
	MLZ-DAQ	Multi-	Z80	2.0-4.0	2K	8K	2S, 32P, 4T, 8I, AN
	MLZ-91	Multi-	Z80	4.00	64K	8K	2S, 0P, 0T, 8I, P, HD, ST, F, APU
Intel	iSBC 80/04	None	8085A	1.97	256	4K	1S, 22P, 1T, 4I
	iSBC 80/05	Multi-	8085A	1.97	512	4K	1S, 22P, 1T, 4I
	iSBC 80/10A	Multi-	8080A	2.05	1K	8K	1S, 48P, 0T, 1T
	iSBC 80/20-4	Multi-	8080A	2.15	4K	8K	1S, 48P, 2T, 8I
	iSBC 80/30	Multi-	8085A	2.76	16K	8K	1S, 24P, 2T, 12I, DP, 2PB
Intersil	ISB-3100	STD-	Z80A	2.5-4.0	4K	4K	0S, 0P, 4T, 0I
	ISB-3110	STD-	8085	3.0-4.0	4K	4K	0S, 0P, 4T, 0I
	Concept-48	None	8048	3.0	2K	2K	1S, 24P, 1T, 0I, RPD, DSP, LP
Monolithic Systems	MSC 8001	Multi-	Z80A	4.0	8K	16K	1S, 48P, 2T, 8I
	MSC 8004	Multi-	Z80A	4.0	32K	32K	1S, 48P, 2T, 8I, DP, APU, MMU
	MSC 8007	Multi-	Z80A	4.0	32K	32K	3S, 24P, 2T, 8I, DP, APU, MMU
	MSC 8009	Multi-	Z80A	4.0	32K	16K	2S, 0P, 2T, 8I, F, APU
Morrow Designs	Decision 1	S-100	Z80	4.0	-	4K	0S, 0P, 0T, 12I, APU, 20A
Mostek	MDX-CPU 1	STD-	Z80	2.5-4.0	256	4K	0S, 0P, 4T, 3I
	MDX-CPU 2	STD-	Z80	2.5-4.0	12K	12K	0S, 0P, 4T, 3I
	SDE-OEM 80E	Euro	Z80	2.5	16K	20K	2S, 32P, 4T, 10I

6.1 Board-Level Microcomputers

Table 6.1-19 (Cont'd.)

8-BIT BOARD-LEVEL MICROCOMPUTER PRODUCTS

Supplier	Model	Bus Structure	CPU Used	Clock Rate MHz	RAM	ROM	Maximum On Board Options
Motorola	M68 MM 01	Exor-	MC6800	1.0	1K	4K	0S, 60P, 0T, 0I
	M68 MM 01A2	Exro-	MC6800	1.0	1K	4K	1S, 40P, 0T, 0I
	M68 MM 01B	Exor-	MC6802	1.0	128	2K	0S, 20P, 3T, 0I
	M68 MM 0131A	Exor-	MC6802	1.0	384	4K	2S, 20P, 3T, 0I, CAS
	M68 MM 01D	Exor-	MC6800	1.0	-	10K	1S, 20P, 1T, 0I
	M68 MM 19	Exor-	MC6809	1.0-2.0	2K	32K	1S, 20P, 3T, 0I
Multi-User Microsystems	Net/80	S-100	Z80	4.0	64K	-	1S, 0P, 0T, 0I
	EXP/80	S-100	EXPANSION	-	-	4K	1S, 8P, 2T, 8I
National Semiconductor	BLC-80/05	Multi-	8085A	2.00	512	8K	1S, 22P, 1T, 4I
	BLC-80/07	Multi-	8080A	2.04	512	4K	0S, 24P, 0T, 1T
	BLC-80/10	Multi-	8080A	2.04	1K	4K	1S, 48P, 0T, 1I
	BLC-80/11	Multi-	8080A	2.04	1K	8K	1S, 48P, 0T, 1I
	BLC-80/11T	Multi-	8080A	2.04	1K	8K	1S, 48P, 0T, 1I, TMP
	BLC-80/12	Multi-	8080A	2.04	2K	8K	1S, 48P, 0T, 1T
	BLC-80/12T	Multi-	8080A	2.04	2K	8K	1S, 48P, 0T, 1T, TMP
	BLC-80/14	Multi-	8080A	2.04	4K	8K	1S, 48P, 0T, 1T
	BLC-80/14T	Multi-	8080A	2.04	4K	8K	1S, 48P, 0T, 1I, TMP
	BLC-80/204	Multi-	8080A	2.15	4K	8K	1S, 48P, 2T, 9I
	BLC-80/11A	Multi-	8080A	2.04	4K	32K	1S, 48P, 0T, 1T, 2Pb
	BLC-80/116	Multi-	8080A	2.04	16K	32K	1S, 48P, 0T, 1T, 2PB
	BLC-80/316	Multi-	Z80A	3.69	16K	8K	1S, 48P, 2T, 9I
NEC Microcomputers, Inc.	TK-80A	None	8080A	2.0	4K	8K	0S, 24P, 0T, 0I, KPD, DSP, CAS
ProLog	7801	STD-	8085A	3.1	4K	8K	0S, 0P, 0T, 1I
	7802	STD-	6800	1.0	4K	8K	0S, 0P, 0T, 1I
	7803	STD	Z80	2.5	4K	8K	0S, 0P, 0T, 1I
	PLS-881	Custom	8080A	2.0	4K	1K	0S, 40P, 0T, 1I
	PLS-888	Custom	8080A	2.0	8K	2K	0S, 40P, 0T, 1I
	PLS-888A	Custom	8080A	2.0	8K	2K	0S, 40P, 0T, 1I
	PLS-858	Custom	8080A	3.1	8K	2K	0S, 40P, 0T, 1I
	PLS-868	Custom	6800	1.0	8K	2K	0S, 40P, 0T, 1I
	PLS-898	Custom	Z80	2.5	8K	2K	0S, 40P, 0T, 1I
RCA	CPD18 S601	COSMAC	1802	2.0	4K	8K	1S, 25P, 0T, 0I, LP
	CPD18 S602	COSMAC	1802	2.5	2K	4K	1S, 21P, 0T, 0I, LP
	CPD18 S603	COSMAC	1802	2.0	512	8K	1S, 25P, 0T, 0I, LP
	CPD18 S604	COSMAC	1802	2.0	512	2K	1S, 21P, 0T, 0I, LP
Rockwell	RM65-1000	MicroFlex	R6502	1.0	2K	16K	0S, 0P, 0T, 0I
	RM65-1000E	Euro-MicroFlex	R6502	1.0	2K	16K	0S, 0P, 0T, 0I
	A65-100	AIM-65	R6502	1.0	4K	20K	1S, 44P, 1T, 0I, CAS, KBD, DSP, PTR
SSM Microcomputer Products	CB1A	S-100	8080A	2.0	1K	2K	0S, 8P, 0T, 0I
	CB2	S-100	Z80	2.0-4.0	2K	4K	0S, 8P, 0T, 0I
Synertek Systems	SYM-1	KIM-1	Sy6502	1.0	4K	28K	1S, 71P, 5T, 0I, KPD, DSP, CAS
	CP110	None	SY6502	1.0	1K	-	3S, 28P, 1T, 0I
	MBC020-65	Exor-	6512	1.0	3K	16K	1S, 20P, 2T, 0I, VDO
	MBC020-68	Exor-	6800	1.0	3K	16K	1S, 20P, 2T, 0I, VDO

6.1 Board-Level Microcomputers

Table 6.1-19 (Cont'd.)

8-BIT BOARD-LEVEL MICROCOMPUTER PRODUCTS

Supplier	Model	Bus Structure	CPU Used	Clock Rate MHz	RAM	ROM	Maximum On Board Options
Systems Group Division, Measurement Systems & Control	CPD-2800	S-100	Z80	4.0	-	-	2S, 16P, 1T, 8I
	CPD-2810	S-100	Z80	4.0	-	4K	4S, 16P, 1T, 8I
Tarbell Electronics	Z80-CPU	S-100	Z80	2.0-4.0	-	-	2S, 0P, 1T, 0I
Wintek Corporation	WINCE	Custom	6800	1.0	512	4K	1S, 32P, 0T, 0I
Xycom	1880+B	Custom	Z80A	2.2	1K	8K	2S, 0P, 0T, 0I, APU, RGD
	1862+B	Custom	Z80A	2.2	8K	8K	2S, 0P, 0T, 0I, APU, RGD
Zilog	Z80-MCB	Z-Bus	Z80A	2.5	16K	4K	1S, 16P, 3T, 4I

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

Table 6.1-20

16-BIT BOARD-LEVEL MICROCOMPUTER PRODUCTS

Supplier	Model	Bus Structure	CPU Used	Clock Rate MHz	RAM	ROM	Maximum On Board Options
Advanced Micro Computers	96/4116	Multi-	Z8000-2	4.0	32KB	8KB	2S, 24P, 5T, 10I, DP, 20A
Contral Data Corporation	B1017	Multi-	Z800-1	4.0	-	4K	0S, 0P, 3T, 9I, MMU, APU
Computer Automation	LSI 2/20	Maxi-	Custom	6.6	-	-	0S, 0P, 0T, 1I, APU, 1PB
	LSI 2/40	Maxi-	Custom	10.0	-	-	1S, 0P, 1T, 1I, APU, MMU
	Scout 4/04	Scout-	Custom	1.5	-	-	0S, 0P, 1T, 6I, APU
	NM 4/10	Maxi-	Custom	1.5	4K	4K	4S/4P, 1T, 6I, APU
	NM 4/30	Maxxi-	Custom	5.0	-	-	0S, 0P, 1T, 6I, APU
	NM 4/90	Maxi-	Custom	5.0	-	-	0S, 0P, 1T, 6I, APU
	NM 4/95	Maxi-	Custom	5.0	-	-	0S, 0P, 1T, 6I, APU, MMU, 24A, CM
Data General	MBC/1	Custom	MN602	8.3	2K	4K	1S, 32P, 1T, 16I
	MBC/2	Custom	MN602	8.3	8K	32K	2S, 32P, 1T, 16I
	MBC/3	Custom	MN602	8.3	32K	32K	2S, 32P, 1T, 16I
Desert Micro Systems	DM-8800	STD	8088	5.0	-	4K	0S, 0P, 0T, 2I, 20A
Digital Equipment Corporation	KD11-	Q-Bus	LSI-11/2	2.63	-	-	0S, 0P, 0T, 1I
	KD11-	Q-Bus	LSI-11/2	2.63	-	-	0S, 0P, 0T, 1I, APU
	KDF11-	Q-Bus	LSI-11/23	3.45	-	-	0S, 0P,0T, 4I, APU
	KDF11-	Q-Bus	LSI-11/23	3.45	-	-	0S, 0P, 0T, 4I, APU, MMU, 18A
EMM-SESCO	SECS 86/05	Multi-	8086	5.0	16K	32K	1S, 24P, 2T, 9-65I, APU, Rgd
General Automation	GA 16/110	Custom	GA-Micro	20.0	-	-	0S, 0P, 0T, 64I, ECC, PM
	GA 16/220	Custom	GA-Micro	20.0	-	-	1S, 0P, 0T, 64I, ECC, PM
Hewlett-Packard	HP 1000-L	Custom	1000-L set	28.2	-	4K	0S, 0P, 1T, 64I, MMU, PM
Intel	iSBC 86/12A	Multi-	8086	5.00	32K	16K	1S, 24P, 2T, 9-65I, DP, 20A
	iSBC 86/05	Multi-	8086-2	8.00	8K	32K	1S, 24P, 2T, 9-65I, 20A, 2PB
Intersil	Intecept-JR	12-Bit	IN6100	2.5	384	3K	0S, 12P, 0T, 1I, KPD, DSP, LP
	Intercept-CPU	12-Bit	IN6100	3.3	384	3K	2S, 12P, 1T, 1I, LP
Motorola	M68KVM01A-1	Versa-	68000	8.0	32K	64K	2S, 40P, 3T, 7I, BAL, 24A, PM, TST
	M68KVM01A-2	Versa-	68000	8.0	64K	64K	2S, 40P, 3T, 7I, BAL, 24A, PM, TST
National Semiconductor	BLC-86/12B	Multi-	8086	5.00	64K	32K	1S, 24P, 2T, 9-65I, DP, 2A, 2PB
Plessy Microsystems	MPC-515	MiPROC-16	MSI Components	4.0*	-	-	0S, 0P, 0T, 8I, Rgd
	MPC-175	MiPROC-16	MSI Components	2.6*	-	-	0S, 0P, 0T, 8I, Rgd
Texas Instruments	TM990/100M	TM990	TMS9900	3.0-4.0	4K	8K	1S, 16P, 2T, 15I
	TM990/101M	TM990	TMS9900	3.0-4.0	4K	8K	2S, 16P, 3T, 15I
	TM990/180M	TM990	TMS9980	2.5	1K	4K	1S, 16P, 2T, 6I
	TM990/1481	TM990	Bit-Slice	5.0	-	-	1S, 0P, 0T, 16I, APU
	TM990/189	TM990	TMS9980	2.5	2K	6K	0S, 16P, 0T, 6I, KBD, CAS
Western Digital	WD/900	None	WD9000	2.5	64K	-	2S, 16P, 0T, 4I
	ME/1600	Sentinal-	WD9000	2.5	-	-	0S, 0P, 0T, 4I

*Most instructions execute in a single machine cycle.

Source: DATAQUEST, Inc.

6.1 Board-Level Microcomputers

Table 6.1-21

DESCRIPTION OF BOARD-LEVEL OPTION ABBREVIATIONS*

A	=	Address Lines Used (if other than 16)
F	=	Floppy Disk Controller
I	=	Interrupt Levels
P	=	Parallel Lines
S	=	Serial Ports
T	=	Timers Available for Applications
AN	=	Analogue Input/Output
CM	=	Cache Memory
DP	=	Dual-Ported Memory
LP	=	Low-Power (CMOS)
HD	=	Hard-Disk Controller
PB	=	Piggy-Back Boards
PF	=	Power Fail Interrupt Logic on Board
PM	=	Parity Memory
ST	=	Streamer Tape Controller
APU	=	Arithmetic Processing Unit
BAL	=	Bus Arbitration Logic
CAS	=	Cassette Controller
DSP	=	Display on Board
ECM	=	Error Correcting Memory
KBD	=	Keyboard on Board
KPD	=	Keypad on Board
MMU	=	Memory Management Unit
PTR	=	Printer on Board
RGD	=	Ruggedized Board
SFT	=	Software License Included
TMP	=	Extended Operating Temperature
TST	=	Self-Test Features
VDO	=	Video Interface

*NOTE: Some abbreviations are preceded by digits in Tables; i.e.: OP means zero parallel lines.

Source: DATAQUEST, Inc.

6.1 Microcomputers

MICROCOMPUTER MARKET CHARACTERISTICS

Introduction

At the low end of the computer price and performance scale, a growing number of products exist that are generally labeled "microcomputers." Although this term is rather ill-defined within the computer industry, it generally refers to low-cost computer CPUs supplied on circuit boards and built using some form of semiconductor LSI technology. System level products, which include power supply and cabinet, adopt the name microcomputer when their price and performance place them clearly at the bottom end of the minicomputer market performance spectrum. The purpose of this section is to explore and forecast this dynamic and fast-growing portion of the small computer market.

The products to be included in DATAQUEST's definition of a microcomputer are 8-bit board- and system-level products as well as 12- and 16-bit board-level products. Specifically excluded from this analysis are microprocessor development systems, custom board products, prototyping boards sold by semiconductor suppliers to familiarize their customers with microprocessors, and dedicated small computer systems that incorporate CPU, keyboards, displays, and peripherals in a single package. The analysis focuses on the general purpose board and systems market at the OEM level and excludes the peripherals, software, and service associated with the end-user system market. Stand-alone microprocessor program development systems are treated separately in Section 6.2.

Within the context of the hardware classification of the DATAQUEST Minicomputer Industry Service (MCIS), this section covers Class I boards and systems and Class II and Class III board-level products only. It also includes all current hobby computer kits, boards, and systems. The market has thus been defined to include a subset of general purpose minicomputers that compete with one another.

The term microcomputer will be used as a generic term to cover all of the products specifically included in this analysis. In some cases, the products currently do not use LSI devices in the CPU, but the evolution of the technology and upgrading of product lines by suppliers dictates that in the near future virtually all microcomputer products will be implemented with some form of LSI devices for the CPU function. The use of LSI semiconductor memory is already well-accepted in computers of all sizes and dominates microcomputer memory implementation.

Although products for the experimenter/hobbyist market have traditionally been sold in kit form, they are included in this analysis due to the importance of the market and of the major suppliers which have evolved from it. The experimenter/hobbyist market is considered a consumer market and is included in the "other" category of microcomputer applications. For more detailed information on the hobby market, please refer to Section 6.3.

Industry Structure

The microcomputer market is structured in a unique manner as a result of the three diverse types of suppliers to the market. The three supplier groups are: (1) the traditional minicomputer manufacturers; (2) a new group of suppliers specializing in microcomputers; and (3) the semiconductor suppliers. This combination brings to the market three completely different sets of perspectives, distribution methods, and marketing philosophies.

Although traditional minicomputer companies like Computer Automation have been supplying board-level products for many years, the

semiconductor suppliers provided the first really low-cost, general purpose boards and systems when they introduced the 8-bit microprocessor chip sets in 1973. A group of small entrepreneurial firms exploited this new technology and began marketing products for industrial control, data acquisition, and hobby applications.

As a result, until recently, the market was structured according to heritage. The minicomputer suppliers were offering low-cost 16-bit machines with upward-compatible instruction sets, such as the DEC LSI-11. The specialized microcomputer suppliers (such as MITS and IMSAI) were supplying 8-bit systems based on the Intel 8080 CPU chip to industrial and hobby customers. The semiconductor firms have made it clear within the past year that they intend to participate in this market with a full range of products based on microprocessor and memory technology. The high semiconductor content of both board- and system-level products makes them attractive to the semiconductor suppliers and provides a competitive edge from a cost standpoint.

We believe that the structure of the industry will continue to evolve rapidly as specialized microcomputer firms move away from the experimenter/hobbyist market, which provided their initial customer base, into the more traditional OEM and end-user markets. It is expected that over the long term, the semiconductor suppliers will dominate the OEM market in both 8- and 16-bit board-level products due to their cost advantage and technology position. Although the minicomputer firms will continue to be a factor in the 16-bit board market, it is expected that their low-cost processor capability will increasingly be used to support their own end-user-oriented products where software, system architecture, and customer support are important factors.

Participants

The microcomputer market has brought together a large number of competing suppliers with different sets of strengths and weaknesses for a share of the low-performance board and systems market. Many of the small firms were able to enter the market due to the initial acceptance of kit-type products for the hobby market. The rapid movement of the market no longer makes it possible for a new start-up to gain significant market share in a short period of time. The experimenter/hobbyist market (with its cash-before-delivery method of operation) created the opportunity for a new computer supplier to start and grow. However, this market is undergoing a number of major changes, among which is a transition to preassembled systems that considerably increases the capital requirements for market participation. As a result, the market is already somewhat stabilized in terms of the suppliers that will be important to the future of the OEM board and systems markets.

Major minicomputer firms with a position in the OEM microcomputer market include Computer Automation, Data General, DEC, General Automation, and Interdata. Microdata has chosen to de-emphasize this market. Of those firms committed to this market, only Data General and DEC have a captive semiconductor source. Other suppliers use custom chips purchased from outside vendors. Texas Instruments is a difficult company to categorize. Using the 16-bit processor chip, it has introduced board- and system- level products from the Digital Systems Division and board and development systems from the Semiconductor Division.

Specialized microcomputer suppliers focusing on system-level products include Control Logic, The Digital Group, IMSAI, MITS, PCS, Inc., Polymorphic Systems, and Warner and Swasey. These firms are also active in the

board-level market. Although many of these suppliers are supplying only kits to the experimenter/hobbyist market, the general purpose design of the products and the trend away from kits in the hobby area are permitting these firms to move into the more traditional OEM markets in communications, industrial control, and instrument and lab automation.

MITS has been acquired by Pertec and has indicated its intention to move rapidly into end-user markets in the business data processing area in addition to maintaining its thrusts in the hobby and industrial markets. The smaller independent firms are having difficulties growing and making the transition from kits to assembled products. Those firms that have specialized in board-level kits for the experimenter/hobbyist market may have to be content with a small share of the hobby market, or face severe competition from newer, more aggressive suppliers of assembled boards. Small firms also lack the high-volume semiconductor purchasing power, and therefore have a cost disadvantage by comparison with larger suppliers.

The semiconductor suppliers have avoided the experimenter/hobbyist market except to the extent that their prototype board kits were bought by hobbyists in addition to potential chip customers. Their entry into the OEM board and systems market is the initial phase of the implementation of an overall vertical integration strategy aimed at deriving greater sales volumes from LSI memory and processor devices. The products related to microcomputers that are supplied by semiconductor manufacturers include microprocessor development systems, prototype boards, custom CPU and memory boards, add-on memory boards and systems, and OEM CPU boards and systems. With the exception of the true OEM products, the semiconductor suppliers have backed into supplying high-level products as a means of supporting and enhancing the sale of LSI chips. Even custom CPU boards for large-volume users are primarily aimed at creating a large market for their microprocessor devices and the associated interface and memory products. Due to their agressive marketing and inherently better device cost position, the semiconductor suppliers can be expected to move into a dominant position in the OEM board- and systems-level markets—initially, with 8-bit products and later with advanced 16-bit processors.

A listing of microcomputer suppliers and their addresses appears in Appendix B.9.1.

Products

Microcomputer products take a variety of forms; however, product structure is built around board- and system-level products. In most cases, they represent two levels of integration by the same supplier. For example, the Intel SBC 80/10 board-level CPU is combined with a chassis, power supply, and front panel to implement the System 80/10. For most suppliers, the product listing is a "hardware store" full of various boards for CPU, RAM, PROM, A/D and D/A converters, interfaces, interrupt controllers, and I/O controllers. They are used in various combinations according to the needs of the specific application. The customer may elect to provide the card cage, power supply, and cabling, or can delve further into the supplier's catalog and buy each part he needs to integrate the computer into his end product at the proper level.

Both board- and system-level products look very much like the OEM products sold for a number of years by the minicomputer suppliers, except the prices are much lower and the performance correspondingly less. The vast majority of products are 8-bit processors utilizing one of the popular LSI CPU devices such as the Intel 8080, the Motorola 6800, MOS Technology 6502, or the Zilog Z80. Much of the software support associated with the minicomputer

market is becoming available for the microcomputers. High-level languages, various types of assemblers, disc operating systems, file management, word processing, and other utility programs are currently available from either the processor supplier or one of the many "micro" software houses which have sprung up around the country.

The specific board-level products offered are largely a function of the availability of LSI CPU devices and have bus characteristics and system architectures that are dictated by the CPU devices. A typical system might consist of a CPU board which contains the CPU, control ROM, and a limited amount of RAM. A second board would handle I/O functions; additional ROM and RAM would be on additional boards. Thus, while a CPU board may sell in quantity for under $300, the total price for a system to solve a specific problem generally runs between $700 and $1,500. In process control and machine tool applications, where large numbers of complex I/O ports or A/D converters are required, a set of boards can run as high as $3,000, even in reasonably large quantities.

System-level products are currently dominated by the kits sold by the hobby-oriented manufacturers. A minimal system with CPU, memory, peripheral interface, and power supplies is priced at about $700 in kit form and close to $1,000 assembled. A number of additional boards and accessories must be added to the basic system in order to solve a specific problem for the user. As system-level products are generally used in more memory-intensive applications, the cost of an assembled system without the peripherals can run $2,000 to $3,000 in small quantities.

An important product trend that may emerge is second sourcing of popular microcomputers. National Semiconductor has introduced a second source board for the Intel 80/10 and 80/20 Series of 8-bit CPU boards, starting what could be a trend toward second sourcing at the board level. This is just another example of the "component mentality" being extended into the microcomputer board and system markets. As system architecture and bus designs become further standardized due to the widespread use of present and future Intel and Intel-compatible chips, this trend should accelerate.

Distribution and Marketing

At the present time, each of the three groups of market suppliers has a different approach to the market and decidedly different marketing and distribution channels. The minicomputer suppliers view the microcomputers as a downward extension of the minicomputer product and technology with lower prices that open up new levels of users. The hobby-oriented suppliers have developed mail order and retail stores as their primary distribution methods. Initially, there was only mail order distribution of computers to the hobby market, but as the popularity of the computer hobby spread, retail stores sprang up to serve local markets for both hardware and software products. The semiconductor suppliers are using the traditional component OEM sales force and the network of distributors to sell chips, boards, and systems. All three levels of products are treated as different forms of the same component and offered to the customer as viable alternatives, depending upon the needs of the customer and his applications.

The semiconductor suppliers and their distributors command a much larger customer base and number of outlets than do the other two types of microcomputer suppliers. Although the minicomputer suppliers are starting to use dealers for distribution of small OEM computers and OEM peripherals, their sales are primarily through system-oriented direct sales forces.

The retail outlets are the really new inno-

vation in computer marketing. At the present time, there are approximately 350 retail stores worldwide selling computers, kits, and associated peripherals and software. Both MITS and IMSAI have established franchised stores, while some independent chains of associated stores such as Byte Shops and Computer Mart handle several manufacturers' equipment. Byte Shops are the largest independent chain, with over 70 stores worldwide. Of the franchised stores under the control of equipment manufacturers, the MITS Computer Stores, Inc. are the largest, with over 25 stores now in operation throughout the United States. IMSAI has also started franchised outlets under the Computer Store name with about ten stores operating at the present time. Retail stores are an important part of the end-user marketing strategies of many microcomputer manufacturers, because it is expected to allow entry into the very small business computer market.

Another important distribution trend resulting from the growth and development of the microcomputer market is the entry of the electronics distributors into the hobby and OEM equipment markets. Several large distributors (such as Hamilton/Avnet) are starting major efforts to market the OEM board and system products of their semiconductor principals and are moving into peripherals as well. The distributor appears to be on the way to becoming the low-volume OEM computer distribution arm for the semiconductor companies as they move further into the computer market. The wide sales coverage and short delivery times associated with distributors could give the semiconductor suppliers a powerful OEM sales organization.

THE MICROCOMPUTER MARKET

Market Trends

In looking at major trends, both the OEM and end-user markets must be considered. The minicomputer manufacturers are expected to evolve into the sales of small packaged systems based on their microcomputers to take advantage of their strengths in end-user marketing and to maximize the sales and profit dollars on each system. The peripherals content of systems directed at small business applications will amount to four or five times the processor cost, making the end-systems market very attractive for the vertically integrated minicomputer manufacturers such as DEC and Data General. The end result would appear to be a combining of the two movements within the minicomputer industry—greater emphasis on end-user markets and systems and further exploitation of the lower costs of CPU and memory devices in low-priced computer systems.

The specialized microcomputer manufacturers are also expected to move more towards the industrial and business markets with complete product lines and packaged systems. The uniqueness of their retail marketing outlets should allow them to open new markets for business and professional computer systems. Computer retail stores should become a major new factor in the sales, support, and maintenance of very small business-data-processing-oriented computer systems.

The semiconductor suppliers are expected to begin to dominate the OEM hardware business for both 8- and 16-bit processors due to their lower device costs and access to the latest technology. Further vertical integration by the semiconductor firms seems inevitable, in which case the final competitive battleground for all three supplier groups appears to be the packaged systems for business, industrial, and per-

sonal use. The high peripheral content of systems and the software dependency should force the semiconductor suppliers to move toward integration beyond boards and systems in order to be able to offer competitive products incorporating CRT/keyboards, floppy discs, printers, and other high-volume peripherals. New memory technologies (such as charge-coupled devices (CCD) and magnetic bubble domain (MBD)) will be important to the small systems market and therefore could be profitably used by the semiconductor suppliers to further their position in this market. It is expected that if present trends continue, in five years the products and capabilities of the three competing groups of suppliers will be very comparable, with marketing and support as major competitive factors.

The low prices of board- and systems-level microcomputers have opened up new applications, both with sophisticated and unsophisticated users. To a large extent, these board and system products are starting to be viewed as components in much the same way as microprocessor and memory chips are components. Over time, the technology permits a given amount of computer system to be assembled on fewer boards with fewer semiconductor components. The level of product integration, chips, boards, or systems for a particular application is a matter of the user's ability and economic need to utilize the computer at a particular level of complexity.

Just as with semiconductor LSI, there are standard and custom board-level products. As with chips, the choice is one of economics and overall system performance. The system-level product is nothing more than the packaging necessary to use the computer boards in any given application. Thus, an analogy exists between the LSI chip and its package, and the microcomputer board and its cabinet, card cage, power supply, and cables (the system). This similarity will be further discussed in the following subsection.

In general, the user of a microcomputer has the option of buying the processor and memory and input/output circuitry at either the chip, board, or system level. The semiconductor suppliers started supplying board- level products to their chip customers as an aid to system prototyping and programming. It came as a surprise to many of the chip suppliers (and industry analysts) that their customers would actually start volume production using board- or system-level components rather than chips. This has occurred because many of the customers for microprocessors are new users of electronic components and certainly not adept at microcomputer selection and programming. As a result, the board- or system-level component is a perfect solution, since it is much easier to use and apply than the bare microprocessor chip.

The choice of chip-, board-, or system-level computer components is a complex set of tradeoffs, many of which are subjective in nature. The variables include annual quantity, end-system price, the percentage of the system which is the computer, and the sophistication of the user. For example, a manufacturer of energy management systems for small commercial buildings would, in most cases, elect to buy at the system level since the annual quantity of systems is not likely to exceed a few hundred and the computer, at $3,000, represents somewhere between 5 and 10 percent of the total system cost. Further, the user has his primary expertise in energy systems management and analysis; the related software and computer are simply "components" in the overall system.

At the other extreme would be a manufacturer of intelligent terminals who is already in the electronic systems manufacturing business and has engineers who are expert in logic and hardware design. In addition, the number of annual units is probably well over 5,000 per year, and the processor and memory account

for up to 25 to 30 percent of the hardware cost. In this case, the decision will likely be to build the system using chip-level components and a circuit board design that is optimized for large-volume production of a relatively low-cost product.

In the middle are applications such as medical instruments, data entry systems, and data acquisition systems in which the combination of user sophistication, end-product price, and annual unit volume will lead to a decision to purchase the computer at the board level in many cases. This is particularly true where the nature of the application requires the system manufacturer to design and build one or more custom interface boards in order to integrate the computer effectively into the end product.

The choice of 8-bit or 16-bit computer is, in general, based on the computational and throughput requirements of the system, but is also based on system expandability, vendor software support, and some subjective factors. In general, the 8-bit units are used in control-oriented applications, while 16-bit machines are chosen for higher-throughput, computation-oriented systems. Among the subjective factors is the fact that many designers underestimate the amount of processing power and memory that will be required. If the cost differential is not significant, then the larger, more powerful system will be an "insurance policy" against finding halfway through the project that the processor is too small.

In general, the criteria for determining the choice of chip-, board-, or system-level products include overall system cost, user sophistication, and the annual units required. As a generalization, it can be stated that sophisticated users with production volumes of 5,000 to 10,000 units per year will elect to buy at the chip level. In some cases, this unit volume requirement can be as low as 1,000 units if the design and manufacturing capability are already in place. If the system is to have an annual volume between 100 and 1,000 units per year, board-level products are generally the choice. From a few up to a few hundred units per year, which usually implies that the system is large and complex and the manufacturers' expertise lies in other areas, the system-level products are generally chosen.

Price Trends

At both the board and system levels, there are factors that tend to increase and those that tend to decrease the price of a typical system. Continued reduction in semiconductor costs should permit reduced prices on existing designs. As the complexity of the devices increases, the same capability can be assembled on fewer circuit boards, providing reduced prices for future generations of systems. On the other hand, the trend toward more memory-intensive applications and the incorporation of complex analog-to-digital preprocessing on system boards is tending to increase the prices of the systems being shipped.

Because of the expected dominance of the board-level business by the semiconductor companies, prices of systems should decline along with device price reductions and density increases. The highly competitive nature of the semiconductor market will likely be extended to the 8-bit board and system business and later to the 16-bit market.

Due to increasing memory content and the availability of a wider range of standard interface and peripheral controller boards, the average price of 8-bit boards is expected to decline at the rate of 14 percent per year through 1981, while 12- and 16-bit boards are forecasted to decline only 10 percent per year.

Systems-level 8-bit machines are expected to drop by slightly over 12 percent per year due to the reduced cost of the boards and more intense competition with 12- and 16-bit systems in the 1979 to 1981 time period. Much like

semiconductor LSI, system-level microcomputer prices tend to be bounded at the low end by testing and packaging cost. The cost of power supplies, cabinets, cables, and front panels is not expected to decrease as quickly as board costs and represents a substantial percent of the total system cost. The largest single cost item, the power supply, can be reduced in cost somewhat by circuit innovations, but can be affected more directly by reducing the power requirements of the LSI chips. Toward the end of the forecast period, it is expected that the 8-bit systems will be of minimal complexity and power drain, contributing to the reduction of power supply cost.

Worldwide Market Forecasts

The world market for microcomputer CPU products from U.S.-based suppliers is expected to grow from an estimated $49 million in 1976 to $370 million by 1981. This represents a 49.8 percent compound annual growth rate. The value of shipments is for manufacturers' factory sales of 8-bit, 12-bit, and 16-bit CPU boards and 8-bit systems and does not include the peripherals, software, or service associated with the final end-user application. In some cases, the microcomputer suppliers will derive additional value from the shipment of peripherals--primarily with system-level products--and service and software. Appendix A treats the total CPU and peripheral market for Class I, II, and III systems in more detail. During this time, annual unit volume is forecasted to increase from 41,000 units in 1976 to 456,000 units in 1981 for an 81.6 percent annual rate of growth. Figures for units and value for the 1975 to 1981 period are given in tables 6.1-1 and 6.1-2.

Market shares by product type for 1976, 1978, and 1981 are given in tables 6.1-3 and 6.1-4. As can be seen, price declines and the resulting high unit volumes combine to give 8-bit boards 35 percent of the 1976 dollar market and 41 percent of the unit market, growing to 37 percent of the units and dollars and 60 percent of the units by 1981.

The 8-Bit Board Market

The 8-bit board market comprises products directed at both the hobby and industrial control markets. The semiconductor suppliers, as well as a few firms dedicated to the control field such as Control Logic, Process Computer Systems (PCS), and Warner and Swasey, dominate the industrial segment. In the hobby-oriented segment there are a large number of suppliers that exist on a relatively small level of business which is conducted primarily by mail order.

As shown in Table 6.1-5, in 1976 an estimated 17,000 8-bit boards were shipped, of which approximately 45 percent of the units went to the hobbyist/experimenter. We believe that the real growth in this product segment is not in the hobby market, however, but in the myriad of industrial and commercial applications which are open to low-cost "component" computers. By 1981, the annual shipments are expected to reach 275,000 units per year, a 102 percent average annual growth rate. During this same time, the dollar volume is expected to grow from $17 million to $138 million for a 75 percent annual growth rate.

The prices and functions of the 8-bit boards can be expected to follow that of semiconductors, in terms of more powerful CPU products, and also in terms of simpler, lower-cost processor boards. During 1977, we expect a number of firms will introduce boards based on the Intel 8048 one-chip computer. These low-cost boards will be popular with the hobbyist, but will also find a number of relatively large-volume applications in areas such as data acquisition systems. To a limited extent, the rapid unit growth can be attributed to the use

6.1 Microcomputers

Table 6.1-1

ESTIMATED WORLDWIDE MARKET FOR MICROCOMPUTERS
(Thousands of Units)

	1976	1977	1978	1979	1980	1981	Annual Growth Rate 1975 - 1981
8-bit Boards	17	45	85	145	220	275	74.5%
8-bit Systems	14	29	45	57	67	73	39.1%
12-bit and 16-bit Boards	10	25	42	63	85	108	60.9%
Total	41	99	172	265	372	456	61.9%

Source: DATAQUEST, Inc.

Table 6.1-2

ESTIMATED WORLDWIDE MARKET FOR MICROCOMPUTERS
(Millions of Dollars)

	1976	1977	1978	1979	1980	1981	Annual Growth Rate 1975 - 1981
8-bit Boards	$ 17	$ 40	$ 68	$102	$132	$138	52.0%
8-bit Systems	$ 18	$ 55	$104	$137	$154	$146	52.0%
12-bit and 16-bit Boards	$ 14	$ 30	$ 46	$ 63	$ 76	$ 86	43.8%
Total	$ 49	$125	$218	$302	$362	$370	49.8%

Source: DATAQUEST, Inc.

Table 6.1-3

ESTIMATED SHARE OF MARKET BY MICROCOMPUTER PRODUCT TYPE (Percent of Units)

	1976	1977	1978
8-bit Boards	41%	49%	60%
8-bit Systems	34	26	16
12-bit and 16-bit Boards	25	25	24
Total	100%	100%	100%

Source: DATAQUEST, Inc.

Table 6.1-4

ESTIMATED SHARE OF MARKET BY MICROCOMPUTER PRODUCT TYPE (Percent of Value)

	1976	1977	1978
8-bit Boards	35%	31%	37%
8-bit Systems	37	48	39
12-bit and 16-bit Boards	28	21	24
Total	100%	100%	100%

Source: DATAQUEST, Inc.

of multiple CPUs in more complex industrial control applications. This implies correctly that the number of systems utilizing 8-bit boards will be less than the number of board shipments forecasted.

The 8-Bit System Market

Until recently, the 8-bit system market was primarily for kits directed at the hobbyist/experimenter. This market provided a good vehicle for a number of new firms to become well established in the small computer field. Among the more notable examples are MITS and IMSAI. Both companies provide systems based on the Intel 8080 chip and have evolved into reliable, well-documented products with a growing list of industrial and business users.

Over the forecast period the average system price for 8-bit system- level products is actually expected to increase as the transition is made from primarily a kit market to primarily an assembled system market. During 1976 an estimated 65 percent of the CPUs shipped went into the hobbyist/experimenter market. By 1981 the hobby market is expected to account for only 15 percent of the 8-bit system unit shipments.

As shown in Table 6.1-6, during 1976 an estimated 14,000 processors were shipped by U.S. manufacturers. This figure is forecasted to grow to 73,000 units with a market value of $146 million by 1981. Toward the end of the forecast period, the upper-end products will likely find strong competition from low-cost 16-bit systems in a number of major applications such as small business computers and industrial control, which will tend to reduce the dollar growth rate. The increased shipments of lower performance, lower-priced systems will likely keep the shipments growing. Average prices are expected to decline in the 1979 to 1981 period due to the competition with 16-bit machines and the resultant shift in the product mix to lower-priced systems.

The 12-Bit and 16-Bit Board Market

At the present time, virtually all of the 16-bit board products are being supplied by minicomputer manufacturers. One exception is the PACE board being supplied by National Semiconductor. The minicomputer-derived boards represent downward extensions of well-established product lines of manufacturers such as

6.1 Microcomputers

Table 6.1-5

ESTIMATED WORLDWIDE MARKET FOR
8-BIT BOARD-LEVEL MICROCOMPUTERS

	1976	1977	1978	1979	1980	1981	Annual Growth Rate 1976 - 1981
Thousands of Annual Units	17.0	45.0	85.0	145.0	220.0	275.0	74.5%
Average System Price (Thousands of Dollars)	$ 1.0	$ 0.9	$ 0.8	$ 0.7	$ 0.6	$ 0.5	-12.9%
Millions of Dollars	$17.0	$40.0	$68.0	$102.0	$132.0	$138.0	52.0%

Source: DATAQUEST, Inc.

Table 6.1-6

ESTIMATED WORLDWIDE MARKET FOR
8-BIT SYSTEM-LEVEL MICROCOMPUTERS

	1976	1977	1978	1979	1980	1981	Annual Growth Rate 1976 - 1981
Thousands of Annual Units	13.7	29.0	45.0	57.0	67.0	73.0	39.7%
Average System Price (Thousands of Dollars)	$ 1.3	$ 1.9	$ 2.3	$ 2.4	$ 2.3	$ 2.0	9.0%
Millions of Dollars	$17.5	$55.4	$104.0	$137.0	$154.0	$146.0	52.8%

Source: DATAQUEST, Inc.

Data General, DEC, and General Automation. The TI 16-bit board, which is based on the TMS9900 processor chip, is offered as the 990/4 for OEM use. The TI board serves as the basis for the 990/10 and 990/20 minicomputers, just as the DEC LSI-11 serves as the processor board in the PDP-11/03. In the cases of DEC, Data General, and TI, the MOS/LSI processor chips are made in an in-house semiconductor facility. DEC is the one exception insofar as it does not actively sell the processor chip set to outside customers.

The 16-bit boards tend to be used in true computer applications where the availability of vendor software or a large user base such as PDP-11 or Data General Nova programs exist. During the latter half of 1977 it is expected that Intel, Mostek, and Zilog will introduce 16-bit processor chips and a line of supported board- and system-level products. Although this should greatly increase the competitive pressures in the market, average selling prices should only see a 10 percent decline due to increasing memory, interface, and peripheral controller boards being shipped as part of the system mix.

Due to lower semiconductor costs and a better ability to market processor components, the semiconductor suppliers could move into a strong position in this market. With a large base of customers who are using 8-bit boards, if the semiconductor firms can meet the upward-compatible processor needs of their customers, they could generate a large-volume market for 16-bit boards. Some of this growth will be at the expense of upper-end 8-bit products; however, the 8-bit processors will be mature at both the board and chip level by 1980 and this inherent competition will have little effect on overall sales revenues.

As shown in Table 6.1-7, the 16-bit board market is estimated to have been 10,000 units with a market value of $14 million in 1976. By 1981 the unit shipments are expected to reach 108,000 units with a value of $86 million. This represents an 87 percent growth rate for units and a 69 percent growth rate for dollars.

During the forecast period, the minicomputer manufacturers will likely use their 16-bit board-level products increasingly in system products and evolve into some multiprocessor applications. The specialized microcomputer suppliers, such as MITS and IMSAI, are expected to introduce 16-bit CPU chips in order to offer a higher level of performance in their industrial and business system products.

International Markets

During 1976, an estimated 85 percent of the microcomputer shipments were to customers in North America. By 1981 this is expected to shift to a 65 percent shipment rate to North America, with Japan taking 10 percent; Europe, 20 percent; and the remainder of the world, 5 percent. The foreign markets for board-level products in particular are expected to be a smaller percentage of U.S. output than for finished systems, since the major contributed value is in assembly of the board; thus, shipment of semiconductor chips will be a better alternative for many users. The chips would be assembled in the foreign country into boards and systems.

Table 6.1-8 gives the estimated regional market shares for all microcomputers.

Market Size by DATAQUEST Performance Class

Tables 6.1-9 and 6.1-10 present the microcomputer market in units and dollars segmented according to DATAQUEST's processor classes. Class I includes products based on MOS 8-bit processor chips. Class II includes all 12-bit processors and the slower 16-bit machines. Class III comprises the low-end minicomputer-based products such as the LSI-11

6.1 Microcomputers

Table 6.1-7

ESTIMATED WORLDWIDE MARKET FOR
12-BIT AND 16-BIT BOARD-LEVEL MICROCOMPUTERS

	1976	1977	1978	1979	1980	1981	Annual Growth Rate 1976 - 1981
Thousands of Annual Units	10.0	25.0	42.0	63.0	85.0	108.	60.9%
Average System Price (Thousands of Dollars)	$ 1.4	$ 1.2	$ 1.1	$ 1.0	$ 0.9	$ 0.8	-10.6%
Millions of Dollars	$14.0	$30.0	$46.0	$63.0	$76.0	$ 86.0	43.8%

Source: DATAQUEST, Inc.

Table 6.1-8

ESTIMATED REGIONAL DISTRIBUTION
OF MICROCOMPUTER REVENUES
(Percent)

Region	1976	1981
North America	85%	65%
Japan	5	10
Europe	10	20
ROW	NIL	5
Total	100%	100%

Source: DATAQUEST, Inc.

and the microNOVA. As a group, the Class II processors form a very small market, the majority of which is based on PDP-8 products and systems that emulate the PDP-8. The rapidly falling costs of the 16-bit products will probably leave little room for the Class II products, except in cases where a software investment in PDP-8 programs justifies using a Class II processor.

Applications

Class I boards and systems are used primarily in hobby and industrial control applications at the present time. An estimated 45 percent of the Class I boards and 65 percent of the Class I systems are sold to experimenters/hobbyists. By 1981 we estimate only 15 percent of the units will be for hobby applications. Tables 6.1-11 through 6.1-14 show our estimates for Class I board and system products.

Class II products find very little usage outside of the industrial control and laboratory automation areas. In the future, the availability of low-cost Class III boards should restrict the growth of the Class II market. Tables 6.1-15 and 6.1-16 show the estimated market for Class

6.1 Microcomputers

Table 6.1-9

ESTIMATED WORLDWIDE MICROCOMPUTER MARKET
BY DATAQUEST PERFORMANCE CLASS
(Thousands of Units)

	1976	1978	1981	Annual Growth Rate 1976 - 1981
Class I Boards	17	85	275	74.5%
Class I Systems	14	45	73	39.1%
Class II Boards	2	5	8	32.0%
Class III Boards	8	37	100	65.7%
Total	41	172	456	61.9%

Source: DATAQUEST, Inc.

Table 6.1-10

ESTIMATED WORLDWIDE MICROCOMPUTER MARKET
BY DATAQUEST PERFORMANCE CLASS
(Millions of Dollars)

	1976	1978	1981	Annual Growth Rate 1976 - 1981
Class I Boards	$17	$ 68	$138	52.0%
Class I Systems	18	104	146	52.0%
Class II Boards	2	6	6	24.6%
Class III Boards	12	40	80	46.1%
Total	$49	$218	$370	49.8%

Source: DATAQUEST, Inc.

Table 6.1-11

ESTIMATED WORLDWIDE CLASS I BOARD-LEVEL MICROCOMPUTER MARKET BY APPLICATION (Percent of Units)

	1976	1978	1981
Business Data Processing	–	1%	3%
Communications	2%	5	10
Design & Drafting	–	1	2
EDP Support	3	2	1
Industrial Automation	25	30	27
Instructional	5	5	7
Laboratory and Computational	10	12	12
Specialized Data Acquisition and Control	10	12	15
Specialized Data and Word	–	2	8
Other (Including Hobby)	45	30	15
Total	100%	100%	100%
Annual Unit Shipments (Thousands)	17	85	275

Source: DATAQUEST, Inc.

Table 6.1-12

ESTIMATED WORLDWIDE CLASS I BOARD-LEVEL MICROCOMPUTER MARKET BY APPLICATION (Percent of Value)

	1976	1978	1981
Business Data Processing	–	2%	5%
Communications	2%	7	12
Design & Drafting	–	1	2
EDP Support	3	2	1
Industrial Automation	35	32	22
Instructional	5	6	8
Laboratory and Computational	10	12	15
Specialized Data Acquisition and Control	15	15	15
Specialized Data and Word	–	3	10
Other (Including Hobby)	30	20	10
Total	100%	100%	100%
Annual Revenues ($ Millions)	$ 17	$ 68	$138

Source: DATAQUEST, Inc.

II boards by application.

Class III boards tend to follow more closely the distribution of Class II minicomputers in their applications. The higher performance and greater software support permit their use in more EDP-oriented applications and in communications-related systems. Tables 6.1-17 and 6.1-18 show the estimated application distribution for Class III boards.

Major Growth Areas

From an application standpoint, we anticipate that the board-level products will continue to find their major applications in the industrial control, laboratory automation, and specialized data acquisition and control application areas.

During the forecast period, the use of system-level products in business applications should see dramatic growth. The reduction in sales to the hobby segment will probably be more than offset by the rapid growth in systems directed at the business end-user market. The growth rate of the dollar market in the 1976 to 1979 time period should be accelerated by the changeover from kits to preassembled systems, with correspondingly higher average prices per system. The figures do not include the dollar value of peripherals such as discs and printers, which will be greater with the system-level products than with board-level products.

The rapid growth anticipated for the 16-

Table 6.1-13

ESTIMATED WORLDWIDE CLASS I SYSTEM-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Units)

	1976	1978	1981
Business Data Processing	5%	18%	25%
Communications	–	2	5
Design & Drafting	–	–	–
EDP Support	–	–	–
Industrial Automation	15	25	20
Instructional	–	3	5
Laboratory and Computational	10	12	15
Specialized Data Acquisition and Control	5	8	10
Specialized Data and Word	–	2	5
Other (Including Hobby)	65	30	15
Total	100%	100%	100%
Annual Unit Shipments (Thousands)	14	45	73

Source: DATAQUEST, Inc.

Table 6.1-14

ESTIMATED WORLDWIDE CLASS I SYSTEM-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Value)

	1976	1978	1981
Business Data Processing	7%	20%	27%
Communications	–	2	5
Design & Drafting	–	–	–
EDP Support	–	–	–
Industrial Automation	20	25	20
Instructional	–	4	5
Laboratory and Computational	12	13	15
Specialized Data Acquisition and Control	6	8	10
Specialized Data and Word	–	2	5
Other (Including Hobby)	55	26	13
Total	100%	100%	100%
Annual Revenues ($ Millions)	$ 18	$104	$146

Source: DATAQUEST, Inc.

bit board-level market should provide opportunities for many suppliers; however, like the 8-bit board market, we believe it will be dominated by the semiconductor suppliers. The 16-bit boards will find major applications in communications, EDP support, industrial automation, and systems for laboratory automation and data acquisition and control.

MICROCOMPUTER TECHNOLOGY

Standards

Due to the commonality of the 8080 instruction set and chips to many of the 8-bit microcomputers, this architecture and software forms a *de facto* industry standard. In terms of interfacing at the bus level, two standards have evolved—the S100 bus originated by MITS for the hobby market, and the Intel 80/10 bus introduced with that company's line of products. These bus configurations have the same universality in the 8-bit world that the DEC Unibus and Data General Nova bus have in the 16-bit minicomputers. This standardization at the 8-bit level with bus configurations that are essentially "public domain" makes possible a large number of memory and interface boards for use with the available CPUs. The CPU board suppliers such as Intel are encouraging suppliers to enter this market since it broadens the range of applications available to the CPU

Table 6.1-15

ESTIMATED WORLDWIDE CLASS II BOARD-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Units)

	1976	1978	1981
Business Data Processing	5%	6%	7%
Communications	10	7	5
Design & Drafting	–	–	–
EDP Support	–	–	–
Industrial Automation	50	50	48
Instructional	–	–	–
Laboratory and Computational	20	20	20
Specialized Data Acquisition and Control	15	17	20
Specialized Data and Word	–	–	–
Other (Including Hobby)	–	–	–
Total	100%	100%	100%
Annual Unit Shipments (Thousands)	2	5	8

Source: DATAQUEST, Inc.

Table 6.1-16

ESTIMATED WORLDWIDE CLASS II BOARD-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Value)

	1976	1978	1981
Business Data Processing	6%	8%	10%
Communications	10	7	5
Design & Drafting	–	–	–
EDP Support	–	–	–
Industrial Automation	49	48	45
Instructional	–	–	–
Laboratory and Computational	20	20	20
Specialized Data Acquisition and Control	15	17	20
Specialized Data and Word	–	–	–
Other (Including Hobby)	–	–	–
Total	100%	100%	100%
Annual Revenues ($ Millions)	$ 2	$ 6	$ 6

Source: DATAQUEST, Inc.

products. This has happened to some extent at the 16-bit level with, for example, the products introduced for use with the DEC LSI-11. The LSI-11 bus is not a Unibus, but by virtue of its use in the popular board-level computer, it is a *de facto* standard for 16-bit microcomputers. It is to expected, however, that upward extensions of the S100 and 80/10 bus will also provide a widely accepted standard for future 16-bit machines.

Semiconductor LSI

Microcomputer products and prices are driven primarily by semiconductor technology. Since costs are a function of the number of boards required to build a system and the number of components per board, the costs of the microcomputers can be expected to continue to decline with increasing levels of semiconductor integration. However, advances in LSI technology are expected to provide greater system performance in the area of larger memory and more peripheral controllers on the chip. The expected result is that the average price for both board- and system-level systems will not decline as rapidly as semiconductor

Table 6.1-17

ESTIMATED WORLDWIDE CLASS III BOARD-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Units)

	1976	1978	1981
Business Data Processing	5%	6%	8%
Communications	15	12	10
Design & Drafting	2	2	3
EDP Support	10	12	15
Industrial Automation	25	24	20
Instructional	3	4	5
Laboratory and Computational	20	18	15
Specialized Data Acquisition and Control	10	10	10
Specialized Data and Word	5	5	6
Other (Including Hobby)	5	7	8
Total	100%	100%	100%
Annual Unit Shipments (Thousands)	8	37	100

Source: DATAQUEST, Inc.

Table 6.1-18

ESTIMATED WORLDWIDE CLASS III BOARD-LEVEL MICROCOMPUTER MARKET BY APPLICATION
(Percent of Value)

	1976	1978	1981
Business Data Processing	8%	10%	12%
Communications	10	8	7
Design & Drafting	2	2	3
EDP Support	10	12	15
Industrial Automation	27	24	19
Instructional	3	4	5
Laboratory and Computational	20	18	15
Specialized Data Acquisition and Control	8	8	8
Specialized Data and Word	7	7	8
Other (Including Hobby)	5	7	8
Total	100%	100%	100%
Annual Revenues ($ Millions)	$ 12	$ 40	$ 80

Source: DATAQUEST, Inc.

device costs.

Just as the economics of the LSI technology made the 4-bit general-purpose microprocessor replaceable by a more powerful 8-bit system at only a nominal increase in cost, so can the difference in 8-bit and 16-bit CPU device prices be expected to converge. During the forecast period, we expect that LSI technology—either MOS or bipolar—will be capable of placing a 16-bit processor, writable control store, ROM, and an effective cache memory on a single chip. Such devices, when coupled with a heirarchy of solid state memory products and processor-based interface controllers, will provide extremely powerful single-board computers which can be used in single or multiple processor systems. High-level language operation of the processor is expected to be readily available by selecting a companion interpreter chip. Special languages for control and communications applications also should be available in ROM.

Microcomputer Hardware

No major changes in microcomputer hardware are seen during the forecast period. The assembly of semiconductor chips on circuit boards is a hand assembly operation for all but the largest of manufacturers. The trend toward fewer packages per computer works to defeat the cost justification of automatic assembly.

6.1 Microcomputers

Innovations in semiconductor packaging will be required in order to place devices of greater complexity and heat dissipation in plastic packages. It is expected that 48-, 64-, and 100-pin packages will be in widespread use by 1981. For high-volume systems, specialized input/output devices can be expected to reduce chip and board count and make the system easier to use.

Microcomputer Software and Support

As the prices of chips, boards, and boxes continue to fall, the economic limitations on the expansion to new applications are continually being removed. The major cost to the user and the seller of the microcomputer system is expected to be software and support. In this regard, a number of technology-related trends appear to be emerging.

The first is a trend toward the sale of major software products in the form of "firmware" included on the processor board. High-level language compilers and interpreters, communications protocols, I/O device drivers, and other software products which lend themselves to standardization are expected to be sold in "chip" form. The semiconductor ROM could become a major medium for the packaging and sale of standard software products.

The second major trend is toward the use of packaged software development systems as expanded system design and documentation centers. The limitation on new applications imposed by the lack of machine-level programmers and systems analysts should be greatly alleviated by the increasing sophistication of "system development" systems. These interactive design and programming systems will provide the unsophisticated user with the "hand-holding," system interaction, and understanding which should enable many new applications to be generated without the great overhead support expense normally associated with the sale and use of products of this complexity. In effect, the customer will be buying a packaged applications specialist in a $5,000 to $10,000 desk-top computer. The system would also handle software documentation. The evolution of current program development systems into products of this type is a natural upgrading of existing products. The technology permits, and even enhances, the "component computer" marketing approach, which is expected to characterize the strong position of the semiconductor suppliers in this market.

MICROCOMPUTER PRODUCTS

Table 6.1-19 lists the leading 8-bit board products and their major characteristics. Table 6.1-20 gives similar information for 8-bit systems. Table 6.1-21 lists the leading 12-bit and 16-bit board-level microcomputers.

MICROCOMPUTER COMPETITION

Competitive Environment

The emerging microcomputer market is highly competitive within a given supplier or application segment. However, the three groups of suppliers—the semiconductor suppliers, the specialized microcomputer manufacturers, and the minicomputer supplier—all currently have different customer bases and marketing approaches. As a result, competition for a given customer is somewhat limited at this time. This is expected to change, however, as the semiconductor suppliers expand their product lines, support, and market objectives.

DATAQUEST believes that over the long term the semiconductor suppliers will dominate the OEM board market for Class I, II, and III products. This will force the minicomputer and microcomputer suppliers to move farther into end-user markets and offer packaged systems

Table 6.1-19

LEADING 8-BIT BOARD LEVEL MICROCOMPUTER PRODUCTS

Supplier	Model	Microprocessor Used		DATAQUEST Performance Class
		Supplier	Model	
Applied Data Communications	Series 70-100	Intel	88080A	I
Control Logic	L-Series	Intel	8008	I
	M-Series	Intel	8080A	I
	MM1	Intel	8080A	I
	CCS-1025	Intel	8080	I
Data Numerics	DL-8A	Intel	8080A	I
Apple Computer	Apple I	MOS Technology	6502	I
	Apple II	MOS Technology	6502	I
Cromemco	ZPU	Zilog	Z80	I
Digital Equipment Corp.	MPS	Intel	8008	I
Digital Group, The	Z80-CPU	Zilog	Z80	I
	8080-CPU	Intel	8080	I
	6800-CPU	Motorola	6800	I
	6502-CPU	MOS Technology	6502	I
Fairchild Camera	F-8 One Card Microcomputer	Fairchild	F-8	I
Gnat	Gnat 8080	Intel	8080	I
Heurikon Corp.	MCP-8080	AMD	8080	I
Intel	SBC 80/10	Intel	8080A	I
	SBC 80/20	Intel	080A	I
Martin Research	AT471-3	Intel	8008-1	I
	AT441-5	Intel	8080A	I
Microcomputer Associates	JOLT CP100	MOS Technology	6502	I
	SuperJOLT CP110	MOS Technology	6502	I
	8080 CPU	Intel AMD	8080	I
Microdata	Micro One	--	TTL/MSI	-

Source: DATAQUEST, Inc.

Table 6.1-19 (Continued)

LEADING 8-BIT BOARD LEVEL MICROCOMPUTER PRODUCTS

Supplier	Model	Microprocessor Used		DATAQUEST Performance Class
		Supplier	Model	
MITS	Altair 680b	Motorola	6800	I
	Altair 8800a	Intel	8080A	I
	Altair 8800b	Intel	8080A	I
Monolothic Systems	MSC 8080	Intel	8080	I
Motorola	Microcomputer I	Motorola	6800	I
	Microcomputer 1A	Motorola	6800	I
Mycron	Mycro I	Intel	8080	I
Mycro-Tek	MT 8080PB	Intel	8080	I
National Semiconductor	ISP-8C	National	SC/MP	I
	BLC-8010	National	8080A	I
Polymorphic Systems	Poly 88 CPU	Intel	8080	I
Process Computer Systems	PCS 1806	Intel	8080A	I
	CM 4400	Intel	8080	I
Process Technology Corp.	SOL-PC	Intel	8080	I
ProLog	PLS-881	Intel	8080A	I
	8811A	Intel	8080A	I
	8821	Intel	8080A	I
	PLS-881	Intel	8080A	I
	8111	Intel	8008	I
	8611	Motorola	6800	I
	8921	Electronic Array	9002	I
	PLS-891	Electronic Array	900C	I
Sphere	Hobbyest	Motorola	6800	I
Systems Integration Associates	SIA-3000	Intel	8080	I
Technical Design Labs	ZPU	Zilog	Z80	I
Warner & Suasey	M-8A			I
Wintex Computer	200ns	Discrete		III
Wintek Corp.	Wince	Motorola	6800	I
Wyle Computer	UP	Intel	8080A	I
Zilog	Z80-MCB	Zilog	Z80	I

Source: DATAQUEST, Inc.

Table 6.1-20
LEADING 8-BIT SYSTEM LEVEL MICROCOMPUTER PRODUCT CHARACTERISTICS

Supplier	Model	Microprocessor Used		DATAQUEST Performance Class
		Supplier	Model	
Data Numerics, Inc.	DL-8A	Intel	8080A	I
American Microprocessors Equipment & Supply	KISS S-100 Jr.	Intel	8080A	I
Apple Computer, Inc.	Apple II	MOS Technology	6502	I
Cromemco	Z-2	Zilog	Z80	I
Digital Electronics	DE 68	Motorola	6800	I
Digital Group, The	System 1 System	Zilog	Z80	I
ECD Corp.	Micromind uM-65	MOS Technology	6512A	I
	Micromind II	MOS Technology	6512A	I
Electronic Product Associates	Micro-68	Motorola	6800	I
Gnat	Gnat 8080	Intel	8080	I
IMSAI	I-8080	Intel	8080	I
	I-8048	Intel	8048	I
Intel	System 80/10	Intel	8080A	I
MBR Enterprises	Astral 2000	Motorola	6800	I
Monolithic Systems, Inc.	8080+	Intel	8080	I
Multisonics	808A	Intel	8080	I
Ohio Scientific Instruments	Challenger 65	MOS Technology	6500	I
	Challenger 68	Motorola	6800	I
Polymorphic Systems	Poly 88/System 16	Intel	8080	I
Process Computer Systems	MicroPac 80/A	Intel	8080A	I
	SuperPac 180	Intel	8080A	I
	MicroPac 180	Intel	8080A	I
Sphere Corp.	300 Series	Motorola	6800	I
Technical Design Labs	Xitan Alpha	Zilog	Z80	I
Veras Systems	F-8	Fairchild	F-8	I
Xecon Associates	XMC-360	Discrete		III
Wave Mate	Jupiter II-CPU-125A	Motorola	6800	I
Zilog	Z80-MCS	Zilog	Z80	I

Source: DATAQUEST, Inc.

Table 6.1-21

LEADING 12-BIT AND 16-BIT LEVEL PRODUCT CHARACTERISTICS

Supplier	Model	Microprocessor Used	Word Length	DATAQUEST Performance Class
Computer Automation	LSI-3105	Discrete	16	II
	Naked Mini LSI/2	Discrete	16	III
	Naked Mini 4	Custom/SI		III
Data General	microNOVA Board	microNOVA	16	III
Digital Equipment Corp.	PDP-8/A	Discrete	12	II
	LSI-11	LSI-11	16	III
General Automation, Inc.	GA-16/110	Custom	16	III
	GA-16/220	Custom	16	III
Interdata	5/16	2900 AMD	16	III
National Semiconductor	1PC-16C	PACE	16	III
	IMP-16L	IMP-16	16	III
	IMP-16P	IMP-16	16	III
Texas Instruments	990/4	TMS 9900	16	III

Source: DATAQUEST, Inc.

including peripherals and applications software. Even National Semiconductor, with its position in the large CPU and memory end markets, only chose to participate at the OEM level, leaving end-user sales and service to the OEM customer. Intel is building an end-user sales force in the IBM add-on memory division which could, in the future, be used to market computer systems into the IBM environment.

The greatest product limitation on any type of supplier attempting to enter the end-user market will be the high peripherals content and the need to have a vertically integrated operation in order to ensure lowest costs and continuity of peripherals supply. The high cost of establishing an end-user sales and support organization places the end-user market outside the reach of most small microcomputer suppliers.

Market Share

Tables 6.1-22 through 6.1-24 present market share estimates for each product segment during 1976. In the 8-bit board market it is expected that during 1977 and 1978 the semiconductor suppliers such as Intel, Motorola, National, Zilog, and Mostek will move into positions of market dominance. A number of smaller suppliers with a dedication to the hobby market will likely survive, but not become major factors in the market. We expect companies with specialized expertise in the industrial control market, such as PCS and Control Logic, to continue to grow, but they will be limited by their marketing resources in comparison with the semiconductor suppliers that have large sales forces and distributor networks.

Although MITS and IMSAI are expected to continue to hold major market shares in the 8-bit system market, Intel, Motorola, and National are expected to make strong inroads into this market during 1977 and 1978. Because of the experimenter/hobbyist and end-user business system orientation of MITS and IMSAI, there will probably not be a high degree of direct competition between these two groups of competitors.

We expect that the 16-bit board market will continue to be dominated by DEC and the other minicomputer suppliers during 1977 and 1978. By 1979 it is expected that the semiconductor suppliers will have well-established 16-bit microprocessor product lines available in both board- and system-level products. Therefore, by 1979 it is expected that the semiconductor suppliers will also have achieved a market position comparable to that held in 8-bit boards during 1977. The large customer base of 8-bit board and system users should provide a natural upgrade market for 16-bit machines.

6.1 Microcomputers

Table 6.1-22

ESTIMATED 1976 MICROCOMPUTER SUPPLIER SHARE
OF WORLDWIDE MARKET
8-BIT BOARD-LEVEL MICROCOMPUTERS

Supplier	Units Shipped	Share of Units	Value ($ Million)	Share of Value
Intel	6,000	35.3%	$ 4.8	28.2%
PCS	1,000	5.9	1.5	8.8
Pro-Log	1,000	5.9	1.0	5.9
Microcomputer Assoc.	700	4.1	0.6	3.5
Electronic Product Assoc.	500	2.9	0.3	1.8
Control Logic	500	2.9	0.8	4.7
Motorola	500	2.9	0.4	2.4
National	500	2.9	0.3	1.8
Other	6,300	37.2	7.3	42.9
Total	17,000	100.0%	$17.0	100.0%

Source: DATAQUEST, Inc.

Table 6.1-23

ESTIMATED 1976 MICROCOMPUTER SUPPLIER SHARE
OF WORLDWIDE MARKET
8-BIT SYSTEMS-LEVEL MICROCOMPUTERS

Supplier	Units Shipped	Share of Units	Value ($ Million)	Share of Value
MITS	6,000	42.9%	$ 5.4	30.9%
IMSAI	3,000	21.4	2.4	13.7
Digital Group	1,000	7.1	1.2	6.9
Intel	500	3.6	1.3	7.4
PCS	500	3.6	1.3	7.4
Other	3,000	21.4	5.9	33.7
Total	14,000	100.0%	$17.5	100.0%

Source: DATAQUEST, Inc.

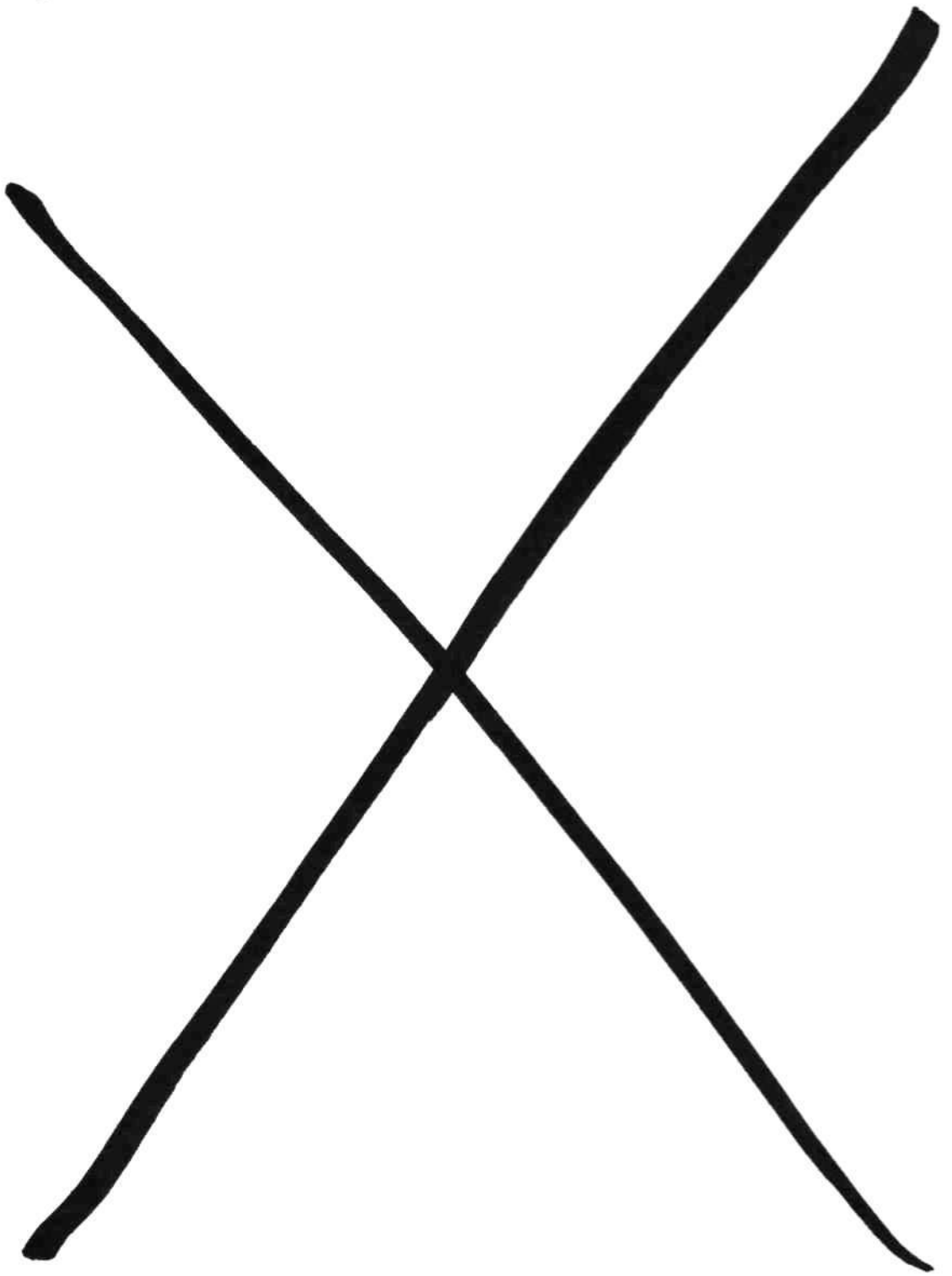
6.1 Microcomputers

Table 6.1-24

ESTIMATED 1976 MICROCOMPUTER SUPPLIER SHARE
OF WORLDWIDE MARKET
12-BIT AND 16-BIT BOARD-LEVEL MICROCOMPUTERS

Supplier	Units Shipped	Share of Units	Value ($ Million)	Share of Value
DEC	6,000	58.2%	$ 7.2	61.5%
Computer Auto.	1,000	9.7	1.0	8.5
TI	1,000	9.7	1.2	10.3
National	1,000	9.7	0.8	6.8
General Auto.	500	4.9	0.6	5.1
Interdata	500	4.9	0.6	5.1
Data General	200	1.9	0.2	1.7
Other	100	1.0	0.1	1.0
Total	10,300	100.0%	$11.7	100.0%

Source: DATAQUEST, Inc.



Semiconductor Manufacturing Model

DATAQUEST
INCORPORATED
480 California Ave.
Palo Alto, California 94306
(415) 327-8210

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This manufacturing chapter consists of two main parts. The first, written in 1975, describes an early 4K RAM production line and is contained in Sections 3.2 to 3.7. In Section 3.8, an update to the original line is presented, which makes use of information on the manufacturing equipment available in 1977. A comparison between the 1975 and 1977 manufacturing lines reveals some dramatic differences, which are highlighted in this section and detailed in Section 3.8.

INTRODUCTION AND PURPOSE

This chapter has two purposes. The first is to familiarize the nontechnical reader with the basic technological and financial implications of operating an integrated circuit manufacturing facility. This purpose is accomplished in Sections 3.2 to 3.7, where the 1975 line is modeled and the manufacturing operations are discussed in some detail. These sections (1) provide the reader with an intimate look into a high-technology manufacturing facility, (2) define the key functions in manufacturing the product, (3) discuss manufacturing costs and the components that have an impact on those costs (such as yield), and (4) survey the capital equipment costs needed to support the business. Included are helpful points in evaluating an IC facility.

The second purpose is to give the reader an understanding of the rapid rate of technological change in the semiconductor industry and an appreciation for the industry's rapid rate of equipment obsolescence. To this end, the line of 1975 is updated in Section 3.8 to a line that we believe is typical of those production lines that are being installed or will be installed in 1977. Process steps and equipment items that have changed during the two-year period are described in detail and a new cost model is constructed for the new line. These old and new cost models are compared in this section and in Section 3.8.

The processes described here are illustrative. Although they summarize some of the variations in NMOS processing, the times, temperatures, and other details are not intended to represent actual working processes. We believe, however, that the equipment throughput rates are accurate enough so that the financial model can be used to draw conclusions about the semiconductor industry.

If the facilities described here were to be constructed from the ground up, it would take at least nine months from initiation of construction to output of the first engineering product runs. Production would commence four months later, and the facility would reach full output 18 months or more after construction had begun. Six months could be saved if an existing, empty building were used. At least two to three months would have to be allowed, however, for the installation of the special facilities required, such as high-purity gas, RF generators, temperature and humidity controls, clean rooms, and a high-purity water system.

NEW PROBLEMS AND OPPORTUNITIES

When the 1975 and 1977 manufacturing lines are compared, it is immediately evident that the new line is much more productive; it has both a higher capacity to process silicon material and a greater product output from a given amount of silicon material. The combined result of these two factors is a new line that can produce more than 10 times as many 4K RAMs as the old line when both are operated the same number of shifts per day.

Our financial model for the new line assumes that it processes no more wafers than the old line; this assumption is believed to be realistic in view of demand and start-up considerations. The capital cost per unit is increased significantly as a result of this assumption. Non-

3.0 Executive Summary

etheless, the product cost is reduced because of the increased product output from a given amount of silicon material. Furthermore, only 40 percent of the capacity of the new line is allocated to the 4K RAM, as compared to 100 percent of the capacity of the old line. We assume that the other 60 percent of the capacity is used for other products. The model line is set up as an 8-mask line even though some products still only require five masks. No effort is made in product costing to account for the different number of mask levels.

To remain competitive, a semiconductor manufacturer must buy new capital equipment when the product output (or yield) from a given amount of silicon material improves. If he is one of the first to install the new equipment, he will be able to amortize it before the product prices fall in the marketplace. If he is late in installing it, he will soon become noncompetitive. Most semiconductor manufacturers do not seek to build excess capacity; instead, the excess capacity that plagues the industry is often the result of a race to improve the yields and thus lower the product costs.

Semiconductor manufacturing equipment does not usually wear out; it merely becomes obsolete in the face of more efficient equipment. Sometimes the rate at which obsolescence occurs can be surprising. Indeed, we estimate that fully 40 percent of the equipment installed in the 1975 line is obsolete or fast becoming so. This situation helps to explain why semiconductor manufacturers tend to use the shortest allowable depreciation schedules.

The fact that the new line offers improved yield suggests that manufacturers will probably consider new product designs with somewhat larger die sizes. These new designs would tend to increase revenue because larger die sizes make it possible to design more complex products that can be sold at higher prices. At the same time, these new products tend to "soak up" excess wafer capacity. More wafers would be required both because there are fewer gross dice per wafer and because yields decrease at larger die sizes—reducing the net dice per wafer as well.

One product of increased complexity that will likely be considered is the 16K RAM. With the yield assumptions contained here, it should be possible to build this product on the new line. However, production would require the development of a "double poly" process, i.e., one using two levels of polysilicon. Since this process was not assumed in our model, it was not possible to assume production of 16K RAMs. Instead, an allocation of 1,000 R&D wafers a month was made to allow development of the "double poly" process.

The new line includes a fully automated line for handling photoresist processing. This new method of handling wafers is beginning to appear in the semiconductor industry. Although it offers advances in yield and process control, it also has the very important effect of reducing the amount of time it takes a wafer to pass through the wafer fabrication portion of the manufacturing process. We estimate that throughput time is reduced by a factor of 2—from three weeks to one-and-a-half weeks. The resultant time savings allows our new line to respond much more rapidly to changes in customer demands and should help to decrease the number of unwanted products that are produced.

COST COMPARISONS

Table 3.0-1 compares the capital equipment costs of the old and new lines. Here it can be seen that the total capital cost has increased by 293 percent—from $720,000 to $2,829,000. Most of the increase was accounted for by the masking area which increased by 635 percent—from $291,000 to $2,140,000. At the same time, the masking room utilized a much larger portion of the capital budget, increasing its

3.0 Executive Summary

share from 41 percent to 76 percent. Most of the increased capital cost in the masking room results from the substitution of projection alignment equipment with associated automated photoresist processing for the older manually-operated contact aligners.

Table 3.0-2 compares the production capacities of the two lines. Here it can be seen that the wafer start capacity increases by 66.7 percent—from 14,300 wafers per month to 23,833 wafers per month. Both the old and new lines have one piece of alignment equipment per mask layer, and both lines are set up so that the wafer-handling capacity of the other process equipment is compatible with that of the aligners; the increased capacity of the new line results therefore from the greater wafer-handling capacity of the projection aligners as compared with the older alignment equipment.

The second line of the table compares the capacities of the two lines when the number of wafers out of fabrication per month is held constant, as it is in our financial model. (Both lines have the same wafer fabrication yield. Thus, the wafer starts are identical if the wafers out of fabrication are identical.) In this case, the new line produces more gross dice because it uses 4-inch wafers rather than the 3-inch wafers assumed for the old line. Even though the projection alignment equipment does not expose the whole wafer, the number of gross die per wafer increases 76 percent—from 250 to 440. For comparison we have assumed the same die size of 150 mils on a side, though today's dice are somewhat smaller.

The fifth line of Table 3.0-2 shows the increase in 4K RAM production capacity, based on 10,000 good wafers a month in each line. The capacity increase is 551 percent (from 0.195 million to 1.27 million RAMs); this increase results partly from the fact that the wafer sort yield has been assumed to increase from 12 percent to 40 percent. This yield increase is attributable to the use of projection aligners, although there is some evidence that masking techniques exist that permit similar yields with conventional aligners. If the added wafer start capacity shown by line 1 of Table 3.0-2 is taken into account, together with the productivity and yield improvements of lines 4 and 5, it will be seen that the new line is capable of producing more than 10 times as many RAMs as the old line. As stated earlier, our financial model has assumed the new line does

Table 3.0-1

CAPITAL COST COMPARISON—
OLD AND NEW PRODUCTION LINE

	Capital Equipment Cost (Dollars in Thousands)			
	Old Product Line		New Product Line	
Area				
Diffusion	$196	27%	$ 308	11%
Masking	291	41	2,140	76
Deposition	233	32	381	13
Total	$720	100%	$2,829	100%

Source: DATAQUEST, Inc.

Table 3.0-2

PRODUCTIVITY COMPARISON

	Monthly Capacity	
	Old Product Line (3 inch wafers)	New Product Line (4 inch wafers)
Wafer Start Capacity (3 shifts)	14,300	23,833
Good Wafers	10,000	10,000
Actual Wafer Starts	14,300	14,300
Gross 4K RAM Die	2,500,000	4,400,000
Net 4K RAM Die	195,000	1,270,000

Source: DATAQUEST, Inc.

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Table 3.0-3

PRODUCT COST COMPARISON

	Manufacturing Cost	
	Old Product Line (3 inch waters)	New Product Line (4 inch waters)
Wafer Fabrication		
Material	$21.70	$22.66
Labor	5.83	7.57
Capital ("Fixed")	1.20	12.25
Total	$28.73	$42.48
Die cost, yielded	$ 1.55	$ .40
Pack and Ship (plastic) yielded	.33	.20
Total	$ 1.88	$ .60

Source: DATAQUEST, Inc.

not produce that many 4K RAMs because of demand and start-up considerations.

Table 3.0-3 compares the manufacturing costs of the old and new lines. Here it can be seen that material costs are under satisfactory control, even though the wafer size has increased from 3 inches to 4 inches. The 4-inch silicon wafer is more expensive, but this cost increase is compensated for by a reduction in mask costs. Projection printing extends mask life almost indefinitely, virtually eliminating the cost of masks.

Wafer fabrication labor increases somewhat, even though labor-saving automated photoresist processing equipment is installed in the alignment room. This rise reflects an increase in manufacturing wages between 1975 and 1977 and an increase in the complexity of the process from five to eight mask levels. Furthermore, higher maintenance costs were assumed because of the more complex manufacturing equipment.

The most dramatic increase in wafer fabrication cost is in the capital cost (or depreciation) per wafer; this cost has increased by 1,021 percent—from $1.20 to $12.25 per wafer. This cost increase reflects the use of very expensive equipment and running rates well below capacity for the new line. If it were to be run at full capacity, the capital cost per wafer would be reduced to $5.14, thus lowering the total cost per wafer by 16.7 percent, and presumably also reducing the product cost.

Table 3.0-3 also shows the reduction in die and package cost. The cost of producing the 4K RAM has been reduced from $1.88 to $0.60, a reduction of 68 percent. This reduction occurs even though the new line is not being operated at full capacity. It is brought about mostly through improvements in wafer sort yield and in die per wafer. It should be pointed out that these figures are cost figures and do not reflect selling prices. Selling prices would typically be two or more times these costs, as determined by the competitive market environment.

3 Manufacturing

INTRODUCTION AND PURPOSE

The semiconductor integrated circuit industry has been characterized by its constant and frequent evolution of new process and product technologies. Because of the technological nature of the changes, it is often difficult for observers outside the industry to fully understand the impact of these technological advances on the performance of a semiconductor company. Part of this difficulty stems from nontechnical observers trying to analyze and relate these changes to their potential financial impact.

The purpose of this report is to familiarize the nontechnical reader with the basic technological and financial considerations and implications of operating an integrated circuit manufacturing facility. To accomplish that, we have developed a manufacturing model of a metal-oxide-semiconductor (MOS) operation, which is described in this chapter. We discuss only the manufacturing operations in detail, while taking a quick look at some of the support activities of the operation. As a result, the other integral parts of a company, such as Marketing, Sales, Product Design, and Administration, and their costs are not covered in this report.

Our objective is to provide an intimate look into a high technology manufacturing facility, define the key functions in manufacturing the product, discuss manufacturing costs and the components that have an impact on those costs—such as yield—and survey the capital equipment costs needed to support the business. Included are helpful points in evaluating an IC facility.

The process described here is illustrative. While it summarizes one of several variations in NMOS processing, the times, temperatures, and other details are not intended to represent an actual working process.

The major manufacturing operations are Wafer Fabrication, Assembly, and Test. Wafer Fabrication consists of chemical and photolithographic processing steps performed on a 3-inch diameter wafer of silicon. The operation forms hundreds of RAM circuits on each wafer. These circuits are tested on the wafer, at wafer sort, with the good circuits being separated from the rejects during the first step of the assembly process. Each good circuit, now called a die, is assembled into a package, encapsulated, and sent on to final test. The assembled units are tested stringently against the guaranteed specifications, and the good units are shipped to customers.

The cost of manufacturing the RAMs is summarized by operation in Table 3.0-1. Wafer fabrication is by far the most expensive operation, at $3,448,000 or 77 percent of total annual expenses. Since the operation generates 30 million dice annually, however, the cost amortizes to $0.115 per die out of wafer fabrication.

Material costs amount to 64 percent of total annual expenditures, with labor accounting for 28 percent. Again, the contribution of wafer fabrication is greatest, amounting to 89 percent of the total cost of materials and 58 percent of the labor costs. In the latter, 105 direct labor operators support the manufacturing operation, 42 of which are in wafer fabrication and 48 in assembly.

Yield fluctuations strongly affect both the material and labor costs. If the wafer fabrication cumulative yield decreases from the 70 percent assumed in our model to 50 percent, the operating costs would rise by $840,000 per year.

The unit cost for the manufacturing model's 4,096 bit RAM is derived to be $1.88 per unit. On an annual basis, this amounts to a manufacturing cost of $4,459,000 per year.

If the facility for the manufacturing model were to be constructed from the ground up, it would take at least nine months from initiation of construction to the output of the first engineering product runs. Production would commence four months later, and the facility would

3 Manufacturing

Table 3.0-1

ANNUAL MANUFACTURING COSTS
(Dollars in Thousands)

	Materials	Labor	Capital	Other	Total
Wafer Fabrication	$2,544	$700	$144	$60	$3,448
Test					
Wafer Sort	–	141	30	6	177
Final Test	71	141	71	6	289
Assembly	230	154	39	74	497
Pack	24	24	–	–	48
Total	$2,869	$1,160	$284	$146	$4,459
Percent of Total	64%	26%	6%	3%	100%

Source: DATAQUEST, Inc.

reach an output of 10,000 wafers per month 18 months or more after construction had begun. Six months could be saved if an existing, empty building were used. At least two to three months would still have to be allowed, however, for the installation of the special facilities required, such as high purity gas, RF generators, temperature and humidity controls, clean rooms, and high purity water.

ASSUMPTIONS

The following assumptions are made for describing this model:

- Output—10,000 3-inch diameter silicon wafers per month.
- Process Technology—Late 1975 state-of-the-art, N-channel, silicon gate, metal-oxide-semiconductor (MOS). A process of medium complexity which is representative of processes currently used by major MOS manufacturers.
- Product—4,096 bit (4K), dynamic random access memory (RAM) similar to those currently entering the marketplace.
- Package—16-pin, dual-in-line package (DIP), plastic.
- High Volume Selling Price—$4.00 per unit
- Unit Shipments Per Month—195,000

In addition to the major assumptions listed above, we are also assuming that all chemicals, materials (such as raw silicon wafers, photomasks, quartzware) complete circuit designs (in the form of ready-to-use photomasks) are already available, and the process is thoroughly proven.

3.0 Executive Summary

This manufacturing chapter consists of two main parts. The first, written in 1975, describes an early 4K RAM production line and is contained in Sections 3.2 to 3.7. In Section 3.8, an update to the original line is presented, which makes use of information on the manufacturing equipment available in 1977. A comparison between the 1975 and 1977 manufacturing lines reveals some dramatic differences, which are highlighted in this section and detailed in Section 3.8.

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When the 1975 and 1977 manufacturing lines are compared, it is immediately evident that the new line is much more productive; it has both a higher capacity to process silicon material and a greater product output from a given amount of silicon material. The combined result of these two factors is a new line that can produce more than 10 times as many 4K RAMs as the old line when both are operated the same number of shifts per day.

Our financial model for the new line assumes that it processes no more wafers than the old line; this assumption is believed to be realistic in view of demand and start-up considerations. The capital cost per unit is increased significantly as a result of this assumption. Non-

3.0 Executive Summary

etheless, the product cost is reduced because of the increased product output from a given amount of silicon material. Furthermore, only 40 percent of the capacity of the new line is allocated to the 4K RAM, as compared to 100 percent of the capacity of the old line. We assume that the other 60 percent of the capacity is used for other products. The model line is set up as an 8-mask line even though some products still only require five masks. No effort is made in product costing to account for the different number of mask levels.

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Semiconductor manufacturing equipment does not usually wear out; it merely becomes obsolete in the face of more efficient equipment. Sometimes the rate at which obsolescence occurs can be surprising. Indeed, we estimate that fully 40 percent of the equipment installed in the 1975 line is obsolete or fast becoming so. This situation helps to explain why semiconductor manufacturers tend to use the shortest allowable depreciation schedules.

The fact that the new line offers improved yield suggests that manufacturers will probably consider new product designs with somewhat larger die sizes. These new designs would tend to increase revenue because larger die sizes make it possible to design more complex products that can be sold at higher prices. At the same time, these new products tend to "soak up" excess wafer capacity. More wafers would be required both because there are fewer gross dice per wafer and because yields decrease at larger die sizes—reducing the net dice per wafer as well.

One product of increased complexity that will likely be considered is the 16K RAM. With the yield assumptions contained here, it should be possible to build this product on the new line. However, production would require the development of a "double poly" process, i.e., one using two levels of polysilicon. Since this process was not assumed in our model, it was not possible to assume production of 16K RAMs. Instead, an allocation of 1,000 R&D wafers a month was made to allow development of the "double poly" process.

The new line includes a fully automated line for handling photoresist processing. This new method of handling wafers is beginning to appear in the semiconductor industry. Although it offers advances in yield and process control, it also has the very important effect of reducing the amount of time it takes a wafer to pass through the wafer fabrication portion of the manufacturing process. We estimate that throughput time is reduced by a factor of 2—from three weeks to one-and-a-half weeks. The resultant time savings allows our new line to respond much more rapidly to changes in customer demands and should help to decrease the number of unwanted products that are produced.

COST COMPARISONS

Table 3.0-1 compares the capital equipment costs of the old and new lines. Here it can be seen that the total capital cost has increased by 293 percent—from $720,000 to $2,829,000. Most of the increase was accounted for by the masking area which increased by 635 percent—from $291,000 to $2,140,000. At the same time, the masking room utilized a much larger portion of the capital budget, increasing its

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share from 41 percent to 76 percent. Most of the increased capital cost in the masking room results from the substitution of projection alignment equipment with associated automated photoresist processing for the older manually-operated contact aligners.

Table 3.0-2 compares the production capacities of the two lines. Here it can be seen that the wafer start capacity increases by 66.7 percent—from 14,300 wafers per month to 23,833 wafers per month. Both the old and new lines have one piece of alignment equipment per mask layer, and both lines are set up so that the wafer-handling capacity of the other process equipment is compatible with that of the aligners; the increased capacity of the new line results therefore from the greater wafer-handling capacity of the projection aligners as compared with the older alignment equipment.

The second line of the table compares the capacities of the two lines when the number of wafers out of fabrication per month is held constant, as it is in our financial model. (Both lines have the same wafer fabrication yield. Thus, the wafer starts are identical if the wafers out of fabrication are identical.) In this case, the new line produces more gross dice because it uses 4-inch wafers rather than the 3-inch wafers assumed for the old line. Even though the projection alignment equipment does not expose the whole wafer, the number of gross die per wafer increases 76 percent—from 250 to 440. For comparison we have assumed the same die size of 150 mils on a side, though today's dice are somewhat smaller.

The fifth line of Table 3.0-2 shows the increase in 4K RAM production capacity, based on 10,000 good wafers a month in each line. The capacity increase is 551 percent (from 0.195 million to 1.27 million RAMs); this increase results partly from the fact that the wafer sort yield has been assumed to increase from 12 percent to 40 percent. This yield increase is attributable to the use of projection aligners, although there is some evidence that masking techniques exist that permit similar yields with conventional aligners. If the added wafer start capacity shown by line 1 of Table 3.0-2 is taken into account, together with the productivity and yield improvements of lines 4 and 5, it will be seen that the new line is capable of producing more than 10 times as many RAMs as the old line. As stated earlier, our financial model has assumed the new line does

Table 3.0-1

CAPITAL COST COMPARISON—
OLD AND NEW PRODUCTION LINE

	Capital Equipment Cost (Dollars in Thousands)			
Area	Old Product Line		New Product Line	
Diffusion	$196	27%	$ 308	11%
Masking	291	41	2,140	76
Deposition	233	32	381	13
Total	$720	100%	$2,829	100%

Source: DATAQUEST, Inc.

Table 3.0-2

PRODUCTIVITY COMPARISON

	Monthly Capacity	
	Old Product Line (3 inch wafers)	New Product Line (4 inch wafers)
Wafer Start Capacity (3 shifts)	14,300	23,833
Good Wafers	10,000	10,000
Actual Wafer Starts	14,300	14,300
Gross 4K RAM Die	2,500,000	4,400,000
Net 4K RAM Die	195,000	1,270,000

Source: DATAQUEST, Inc.

3.0 Executive Summary

Table 3.0-3

PRODUCT COST COMPARISON

	Manufacturing Cost	
	Old Product Line (3 inch waters)	New Product Line (4 inch waters)
Wafer Fabrication		
Material	$21.70	$22.66
Labor	5.83	7.57
Capital ("Fixed")	1.20	12.25
Total	$28.73	$42.48
Die cost, yielded	$ 1.55	$ .40
Pack and Ship (plastic) yielded	.33	.20
Total	$ 1.88	$ .60

Source: DATAQUEST, Inc.

not produce that many 4K RAMs because of demand and start-up considerations.

Table 3.0-3 compares the manufacturing costs of the old and new lines. Here it can be seen that material costs are under satisfactory control, even though the wafer size has increased from 3 inches to 4 inches. The 4-inch silicon wafer is more expensive, but this cost increase is compensated for by a reduction in mask costs. Projection printing extends mask life almost indefinitely, virtually eliminating the cost of masks.

Wafer fabrication labor increases somewhat, even though labor-saving automated photoresist processing equipment is installed in the alignment room. This rise reflects an increase in manufacturing wages between 1975 and 1977 and an increase in the complexity of the process from five to eight mask levels. Furthermore, higher maintenance costs were assumed because of the more complex manufacturing equipment.

The most dramatic increase in wafer fabrication cost is in the capital cost (or depreciation) per wafer; this cost has increased by 1,021 percent—from $1.20 to $12.25 per wafer. This cost increase reflects the use of very expensive equipment and running rates well below capacity for the new line. If it were to be run at full capacity, the capital cost per wafer would be reduced to $5.14, thus lowering the total cost per wafer by 16.7 percent, and presumably also reducing the product cost.

Table 3.0-3 also shows the reduction in die and package cost. The cost of producing the 4K RAM has been reduced from $1.88 to $0.60, a reduction of 68 percent. This reduction occurs even though the new line is not being operated at full capacity. It is brought about mostly through improvements in wafer sort yield and in die per wafer. It should be pointed out that these figures are cost figures and do not reflect selling prices. Selling prices would typically be two or more times these costs, as determined by the competitive market environment.

3.1 Major Manufacturing Operations

An integrated circuit begins with an extremely thin raw silicon wafer about three inches in diameter. Hundreds of individual manufacturing steps later, this silicon wafer is transformed into a number of individual integrated circuits. Manufacture of a 4,096 bit RAM is an extremely complex and highly technical procedure. The purpose of this report is to describe in simple terms the manufacturing procedures used and the costs incurred along the way and to give some insights into the bewildering world of semiconductor manufacturing.

GENERAL DESCRIPTION

The manufacture of an integrated circuit can be divided into three major operations—wafer fabrication, testing, and assembly. An overall flow diagram is shown in Figure 3.1-1. The raw silicon wafer enters the wafer fabrication area for processing. Here, the wafer is transformed into an array of electronic circuits, each of which is made up of a large number of individual transistors interconnected by the processing. A 4K N-channel MOS RAM can have 5,000 to 14,000 transistors in an area roughly 15/100 of an inch square. Each wafer contains an array of about 250 such circuits.

Wafer Fabrication has three main areas of Processing:

- Masking
- Diffusion
- Deposition

The wafer does not transverse a steady path through the wafer fabrication area. Instead, it goes through a sequence of steps that take it several times through each of the three areas in wafer fabrication. In each area, depending on the particular point in the processing sequence, the wafer undergoes a number of processing steps. Defects or processing errors cause many of the wafers to be discarded. However, wafers with complete circuits fabricated on them will eventually reach the end of the processing sequence. It should be pointed out that individual transistors are not fabricated separately but that all of them are fabricated simultaneously.

After wafer fabrication, the wafer then goes to wafer sort, where it is tested. Here each circuit on the wafer is tested individually, and defective circuits are marked. From this point on, the individual circuit on the wafer is called a die (plural, dice). After wafer sort, the tested wafer moves into the assembly area where the dice are packaged into a form that can be used for electronic circuits. First, the dice are separated and the defective circuits are discarded. After this step, the integrated circuits (or dice) are handled individually. Through a number of assembly steps, each good die is placed in a package and the contact electrodes, or pads, on the die are connected to corresponding electrodes extending from the body of the package. The final package is encapsulated in plastic with leads extending from it.

Once packaged the integrated circuits are referred to as units rather than dice. From assembly they go to final test, where they are individually tested to ensure that each part meets the required specifications. After final test, the good units are marked and shipped to customers.

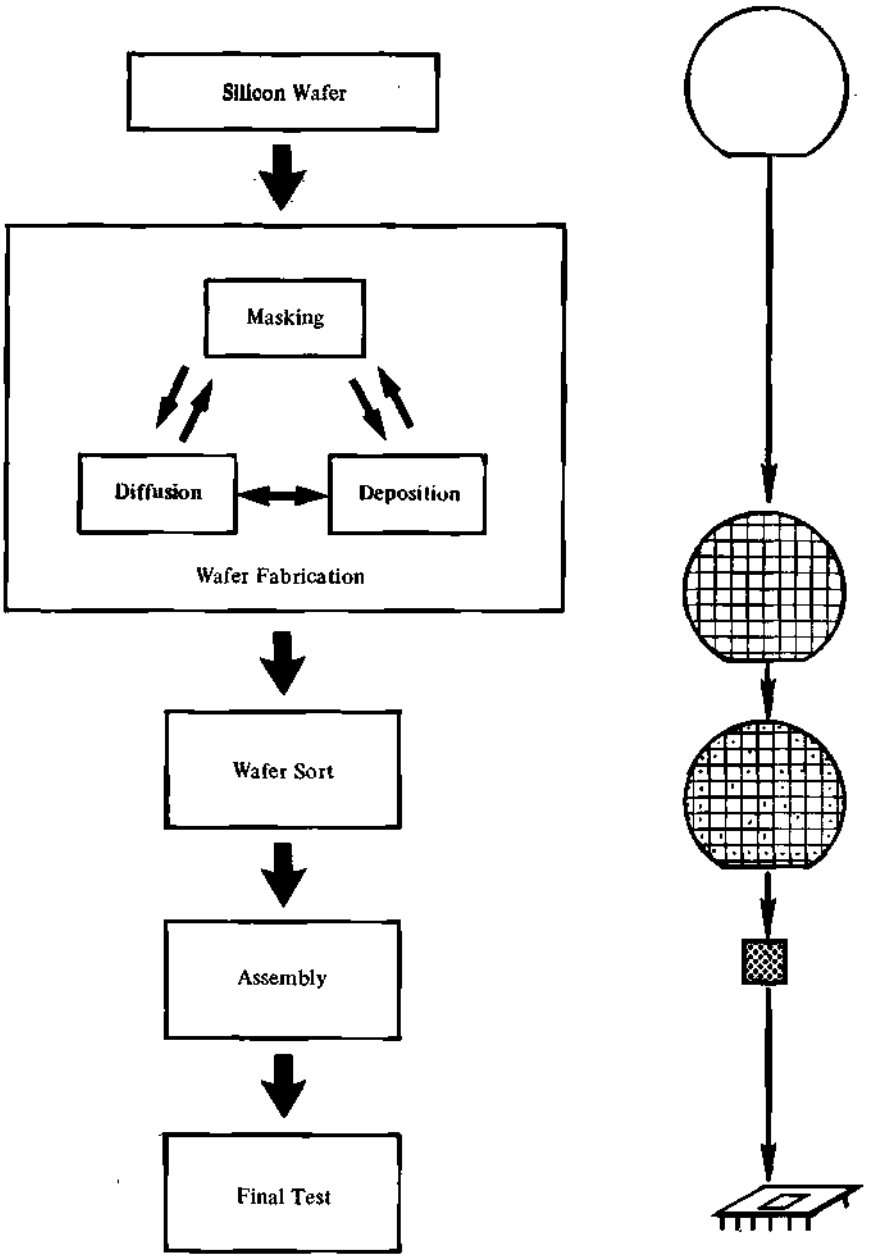
Batch Processing

An important facet of semiconductor manufacturing is its orientation toward batch processing. Wafers are generally processed in wafer fabrication in batches or "runs" containing up to 50 wafers. Since each wafer will be made into up to 250 4K RAM circuits, each batch consists of more than 10,000 potential circuits. These batches are kept together throughout the entire wafer fabrication sequence and are processed simultaneously during each process step. Batches of other types of

3.1 Major Manufacturing Operations

Figure 3.1-1

SEMICONDUCTOR MANUFACTURING WORK FLOW



Source: DATAQUEST, Inc.

3.1 Major Manufacturing Operations

semiconductor devices can contain up to 500,000 individual ICs. The advantage of batch processing, of course, is that a very low labor content can be maintained for single devices. This is the primary reason for the low cost of electronics today.

After wafer fabrication, circuits must be treated individually although they are still processed in groups, with each group corresponding to each batch that was processed through wafer fabrication.

Yield

A second important concept in the manufacture of semiconductor devices is yield. The manufacture of large semiconductor devices, such as the 4K RAM, requires considerable precision and control through a very large number of steps. Throughout processing, a large number of wafers or devices become defective. As a result, only a small fraction of the total number of devices started, or potential devices, eventually become acceptable finished products. The ratio, either for the entire process or for individual steps, is called the yield. If the yield is low, changes in it can have a very significant effect on costs. Changes in yield can vary costs significantly, either up or down. The manufacturers with the most satisfactory yields have the lowest costs and are therefore most competitive.

Process Requirements

To manufacture integrated circuits successfully, the following general needs must be met:

- Extreme cleanliness at all phases of processing
- Very high purity gases, materials, and chemicals
- Manufacturing equipment with very high precision and control
- Sophisticated electronic equipment
- Perfect control of a long and difficult process
- Careful design of the part to be manufactured

These requirements are not discussed individually throughout this report, except for special cases. However, they must be kept in mind for a full understanding of the semiconductor manufacturing process. Some examples will make these needs clear. Transistors in an integrated circuit are nearly microscopic. Any microscopic particle—in the air, cleaning water, or a chemical—can cause a circuit to be defective if the particle falls on a wafer. Sodium contamination as small as a few parts per billion can cause unreliable devices. Water not only must be completely free of contaminating particles, but also free of electrical ions. Alignment equipment must have a precision within a millionth of a meter. Diffusion furnaces must control temperatures over a large area within one degree centigrade at temperatures up to 1,200 degrees centigrade. The number of individual processing steps is so high that yield loss or operator error at one step only once every hundred times could have catastrophic effects on cumulative yields. The challenge to semiconductor manufacturers is to meet these stringent requirements and continually improve the state-of-the-art.

WAFER FABRICATION

In this section, we will discuss the processes used in fabricating MOS silicon gate integrated circuits. This area of manufacturing is commonly referred to as "Wafer Fabrication", "Wafer Fab", "Fab", or "Diffusion". We will refer to it as "Wafer Fab" and will define its major areas as Diffusion, Deposition, and Photomasking (or Masking). Each of the three Wafer Fab areas is discussed in the following sections to give the reader a general understanding of the functions and interrelation-

ships of each.

All of the processing of the silicon wafer occurs in wafer fabriciation area. In this area, the raw wafer is transformed into many integrated circuits through a number of steps described later. During processing, the wafer travels a complicated route through the major areas of wafer fabrication; at several different times during the processing the wafer will be in diffusion, deposition, or masking. The particular process used to produce a finished wafer can vary greatly among different products and for the same product from manufacturer to manufacturer. However, the general nature of the wafer fabrication process is consistent throughout the industry.

Diffusion and Oxidation Processes

The diffusion processes are called such because they characterize processes that take place by the diffusion of atomic elements into the silicon wafers. To visualize what diffusion is, imagine pouring a tablespoon of red food coloring into a glass of clear water. The red coloring "diffuses" into the water, and as time progresses the clear water turns to shades of light pink and then to red. If the coloring were poured into boiling water, the coloration would "diffuse" more rapidly. This concept is the basis for the high temperature diffusion processes used in wafer fab.

Silicon wafers are loaded vertically onto quartz carriers which resemble ladders with slots in their rungs. The carriers or "boats" are 12-24 inches long and, depending on the particular diffusion process, can carry 20-200 wafers.

Once the boats are loaded with wafers, they are pushed into a diffusion furnace, which consists of a horizontal quartz tube heated by coils circumscribing the bulk of its 5 to 7 foot length. The coils heat up the tube, boat, and wafers to temperatures ranging from 450 degrees centigrade to 1,275 degrees centigrade (842-2327 degrees Fahrenheit).

At the rear of each furnace tube is a set of timers and flow meters (commonly referred to as the "jungle"), which control the input of gases into the furnace tube. In newer systems these gases may be 100 percent oxygen or nitrogen. Alternatively, they may be "dopant" gases, consisting of carrier gases such as oxygen and nitrogen mixed with other gases containing boron, phosphorus, or arsenic. The latter dopants are analogous to the red food coloring we previously discussed. All gases are exhausted from the front of the tube, cleansed through gas purifiers or scrubbers, and then passed into the atmosphere.

If pure oxygen is poured into the tube, the silicon is oxidized—i.e., oxygen combines with the silicon to form a glass or oxide of silicon. This process is therefore referred to as the oxidation process. The thickness of the glass or oxide layer is determined by time and temperature: the longer the time and the higher the temperature, the thicker the oxide will be.

If dopant gases are passed down the tube, the elements (boron, phosphorus, arsenic) are deposited onto the wafers and diffuse into the silicon to form conductive regions or junctions in the semiconductor material. The concentration of the dopant in the silicon and the depth to which it diffuses are determined by time and temperature: the longer the time and the higher the temperature, the higher the concentration and the deeper the diffusion. Concentration is also a function of the amount of dopant in the carrier gas.

MOS transistors are formed by a sequential exposure to these diffusion processes, separated by masking steps (discussed later) used to delineate the silicon areas which will or will not be exposed to the diffusion of dopants.

Since the diffusion steps are sequential, each succeeding step modifies the previous steps that have been performed. For example, a

subsequent high temperature process will cause oxides to grow thicker (if oxygen is available) and cause dopants to diffuse deeper. Slight errors, such as leaving the wafers in the furnace too long, can become cumulative and adversely affect yields. As a result, tight process controls and monitors are absolutely necessary to guarantee that all wafers have identical processing.

The number of diffusion and oxidation steps in an N-channel silicon gate MOS process varies greatly between manufacturers, ranging from as low as six to as high as twelve. There are distinct cost and yield reasons for desiring to minimize the number of diffusion steps; these reasons are discussed in Section 3.

Deposition Processes

Some process steps cannot be performed in a diffusion furnace. For example, processes using large amounts of pure hydrogen gas at elevated temperatures can catch fire and explode if accidentally exposed to air. Such processes require closed systems. Other processes must be performed at low temperatures to minimize the impact that these steps would have on previously performed diffusion steps.

Consequently, there is a need for processes that conform to these requirements. The processes utilized are deposition processes, so named because they consist of depositing layers on the silicon wafers versus growing or diffusing them. Two of the deposition processes to be discussed occur by the mixing of reactive gases at temperatures ranging from 380 degrees to 1,000 degrees centigrade. The third deposition process consists of heating a metal until it evaporates, in a closed system. All three types of deposition processes will be discussed. Depending on the manufacturer, three to five total deposition steps are used in manufacturing a silicon gate MOS wafer.

Oxide Deposition

Oxide deposition is also referred to as "Vapox" (from vapor deposited oxides), "topside" glass (when used on top of the metallization), or "field ox" (when used as the intermediate oxide between the poly silicon and metal).

The advantage of this process is that thick glass or oxides can be formed rapidly at a low temperature of 380 degrees to 420 degrees centigrade (716-790 degrees Fahrenheit), in contrast to the greater than 900 degrees centigrade temperatures needed for furnace oxidations. The thickness of the oxide is dependent on time: the longer the time, the thicker the oxide. Because of the low temperature, the growing of oxide with this process will not affect the previous diffusions that have taken place (most dopants begin to move or diffuse significantly at 900 degrees centigrade or higher). Furthermore, unlike the furnace oxidation process, vapox depositions do not consume or require silicon atoms from the wafer itself, which is important for the silicon gate process.

The disadvantages of the deposited oxide process are many: (1) particulate contamination, such as dust or dandruff, on the wafer prior to deposition would be covered by the deposited oxide and possibly negatively affect yields or cause instability problems. In a higher temperature furnace process, these particules would most likely be burned away as soon as the wafers entered the furnace. (2) Virtually all deposition processes require that the wafers lie flat on the carrier, as opposed to the vertical loading used in furnaces. While a furnace tube can typically take 200 3-inch wafers per load, a deposition system can only handle 30 wafers per load. (3) The deposited oxides are not as dense, clean, and defect-free as furnace-grown oxides. (4) Control of the critical parameters is machine and operator sensitive.

As a result of the overriding disadvan-

tages, most manufacturers try to minimize the number of oxide deposition steps in a process.

Poly Deposition

Poly deposition is short for poly-crystalline silicon deposition (hereafter referred to as poly). Unlike the silicon wafer, poly is not a single crystal structure but consists of many small crystals. This deposition process is unique to the silicon gate process, where the poly forms the controlling electrode or "gate" of the silicon gate device.

The poly is deposited at high temperatures (typically 800-1000 degrees centigrade) in a hydrogen gas atmosphere. Because of the reactiveness of hydrogen, the quartz tube is mechanically closed after the carrier of wafers (called a susceptor) is inserted. The susceptor, with the wafers lying flat, is heated by high power radio frequency (RF) electromagnetic waves to the required temperature. In contrast to the standard furnace process, the tube is not heated directly by this process to prevent silicon from depositing on the quartz tubes.

The disadvantages of this process are very similar to those of the deposited oxide processes: particulate contamination, less volume because the wafers must lie flat, and the sensitivity of the critical parameters to machine and operator variations.

In spite of the disadvantages, however, no one has yet been able to develop a furnace-oriented process that is safe and provides the same quality of silicon as that deposited in an RF heated system.

Metallization

Metallization, also referred to as "metal evaporation", "metal", or "evap", is used to deposit a thin layer of metallization (usually aluminum) over the surface of the wafer. A pattern is subsequently delineated in the aluminum, allowing it to connect the individual transistors together to form the circuit function.

The metallization process is performed in a closed system, which is pumped to a vacuum equivalent to that of outer space. The wafers rotate while mounted on holders or dome-shaped "planets" above a source of high purity (99.9999 percent pure) aluminum, which is heated by bombardment from a stream of electrons emitted by an electron gun. Also the wafers are sometimes heated. The thickness of the resulting aluminum layer is a function of the power of the electron beam, time, and the distance of the wafers from the source. This process is relatively straight-forward and is used by virtually every MOS manufacturer.

Photomasking Processes

Also referred to as 'masking", the photomasking processes are used to replicate patterns onto the silicon wafers in much the same manner in which photographs are developed. The patterns, each of which represents an integrated circuit, are arranged in rows and columns, separated by a space or "grid line" 4 mils (0.004 inches) wide. This array of patterns is on the surface of a glass plate, called a photomask or mask. For 3-inch wafer processing, the masks are 4 inch x 4 inch and 60 mils (0.060 inches) thick. The number of patterns on each photomask depends on the pattern size. Our 4K RAM is 150 mils x 150 mils, so each mask has more than 500 repetitive circuit patterns. However, since the 4-inch square mask is larger than the round 3-inch wafer, only about half of the patterns will fall on the wafer.

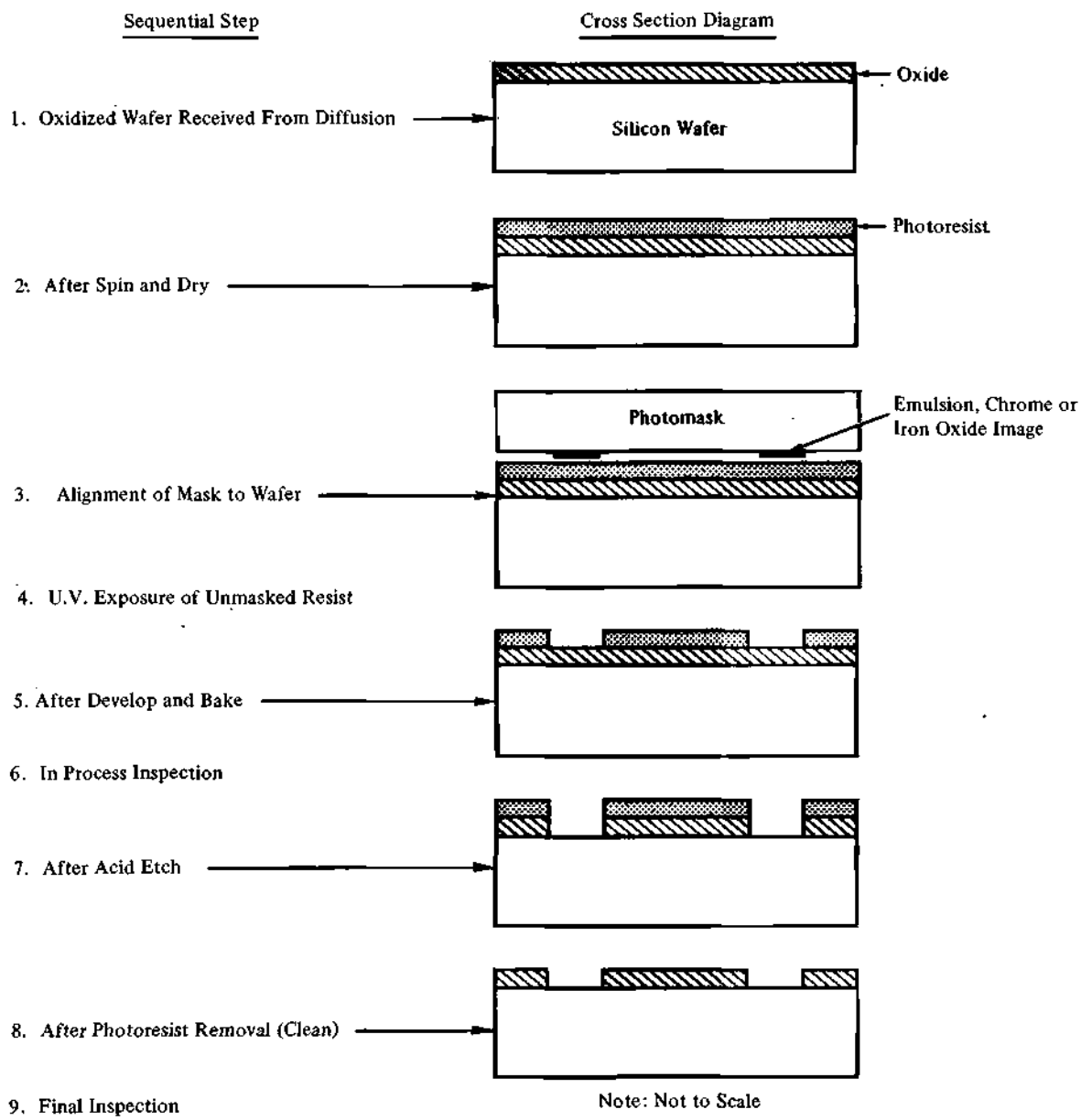
Depending on the manufacturer, a wafer may go through the masking process five to nine times before all wafer processing is completed. As discussed later, the masking process is costly in terms of its effect on productivity, yields, and costs.

Figure 3.1-2 illustrates the sequence of

3.1 Major Manufacturing Operations

Figure 3.1-2

PHOTOMASKING PROCESS STEPS



Source: DATAQUEST, Inc.

events that a wafer goes through at each masking step. In summary, the wafer is received from either a diffusion or deposition process and is coated with a photosensitive material, called photoresist. This step is performed by dispensing a measured amount of photoresist on the surface of the wafer and rapidly accelerating the wafer to 3,000-8,000 rpm. The excess photoresist is immediately thrown off and a thin layer is left on the wafer, the thickness of which stems from the viscosity of the resist and the speed at which the wafer is spun. The wafers are then dried at a low temperature to drive off the excessive solvents from the photoresist. During the next step, an operator aligns the repeated circuit images on the photomask to the corresponding images on the wafer which were generated by the previous masking step. Photomask images can be made of three materials—opaque emulsion, chrome, or semitransparent iron oxide. These materials block ultraviolet light even though some are transparent to incandescent light. When the images are aligned, the mask is brought in contact with the thin layer of photoresist covering the surface of the wafer. Ultraviolet light (UV) is then flashed over the mask. Photoresist under the clear areas of the mask are "exposed" and hardened (polymerized), while that under the nontransmitting areas remains soft. The soft or unexposed photoresist is washed (developed) out at the next step, and then the wafers are baked at a higher temperature to complete the hardening of the remaining photoresist. At in-process inspection, the wafers are inspected to check for quality of the images delineated in the photoresist, at which time those with poor images or a high number of defects are sent back for recycling through the front end of the masking process (called "reworking"). Next, the wafers are dipped in the etching solutions (acids) that attack the underlying oxides, poly, or metal which are unprotected by hardened photoresist. In this manner, holes and patterns are etched through the unprotected layers to duplicate those on the masks. The wafers are then cleaned, inspected (final inspection) to check the quality of the etching processes, and sent on to the next diffusion or deposition step.

If the next step is a diffusion process, the pattern etched in the oxide, for example, will determine where the dopant is diffused into the silicon: it will diffuse into areas where there is no oxide to protect the silicon.

N-CHANNEL SILICON GATE MOS PROCESS

Wafer Fabrication Process

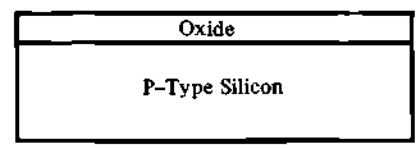
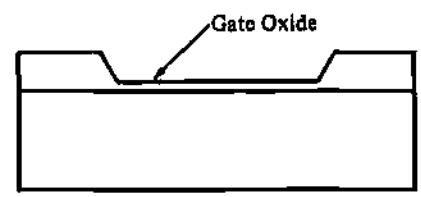
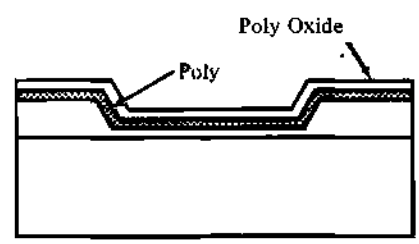
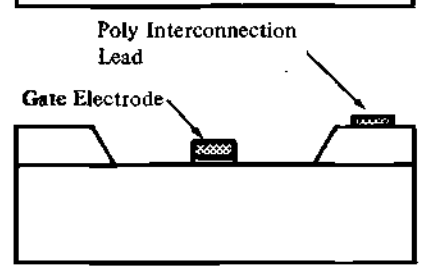
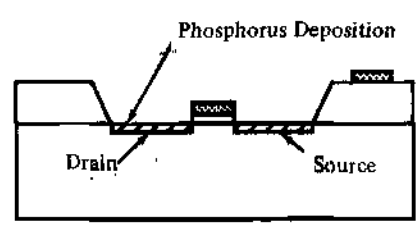
Figure 3.1-3 illustrates and describes the sequence of processing steps followed in wafer fabrication of an N-channel silicon gate MOS. The major transformations that the wafer undergoes are described, and the illustrations show a cross-section of a single MOS device on the wafer. The complete integrated circuit, of course, has thousands of transistors in a complex array of interconnection, while each wafer has several hundred integrated circuits. There are well over 100 individual steps in wafer fabrication. The process shown is the one assumed for our model and gives only the major steps. However, many different processes are currently being used to manufacture N-channel silicon gate MOS. Some of these processes are considerably more complex than the one shown, although the end product is similar. Dataquest feels that ultimately the simpler processes will prevail because of their promise for lower costs and higher yields.

Many processes employ ion implantation, often in conjunction with an additional masking step. Additional capital equipment is required to perform the implantation. We have chosen not to include ion implantation in the process shown, but its application should be

3.1 Major Manufacturing Operations

Figure 3.1-3

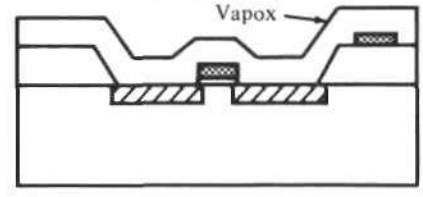
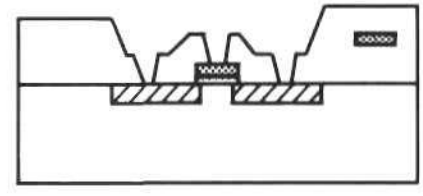
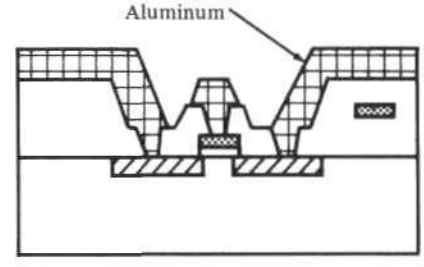
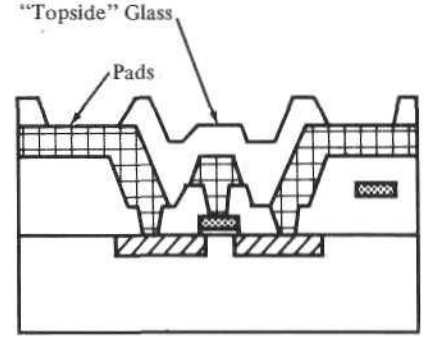
N-CHANNEL SILICON GATE PROCESS

Process Step	Description	Cross Section
1. Initial Clean Initial Oxidation	Silicon wafer is cleaned. Oxide is then grown in a high temperature furnace.	
2. 1st Mask Gate Oxidation	Masking opens the area where the MOS transistor will be formed. A thin (gate) oxide is then grown in the opened area.	
3. Poly Deposition Poly Oxidation	A thin layer of poly-silicon is deposited over the wafer in an RF reactor. A thin oxide layer is then grown on the poly-silicon in a high temperature furnace.	
4. 2nd Mask	Masking delineates the gate electrodes and the poly interconnection leads through a selective etch of the poly-silicon. A further oxide etch opens areas for the next diffusion in areas wherever the thin oxide is not covered by poly.	
5. Phosphorus Deposition	Phosphorus is deposited to form the Drain and Source of the N-MOS transistor as well as any resistors or interconnections in the silicon.	

Source: DATAQUEST, Inc.

Figure 3.1-3

N-CHANNEL SILICON GATE PROCESS

Process Step	Description	Cross-Section
6. Field Oxide Deposition (Vapox) Anneal	A thick layer of glass is deposited (at 400°C). It is annealed in a high temperature furnace which also completes diffusion of the drain and source.	
7. 3rd Mask	Masking opens contacts to gates, drains, sources, and all interconnects.	
8. Aluminum Evaporation 4th Mask	Conductive aluminum is deposited on the wafer. Masking then selectively etches the aluminum to delineate connections.	
9. Glass Deposition 5th Mask Alloy	Low temperature glass is deposited on top of the aluminum to protect it from contamination and scratches. Masking opens holes through glass so that contact can be made to the aluminum pads. A low temperature anneal (alloy) insures that the aluminum makes good contact with the silicon.	

Source: DATAQUEST, Inc.

considered a viable process.

Process Flow Chart

Many manufacturing facilities have a wide range of processes because of the difference in their products. Process flow charts are used to define a particular process. A process flow chart gives the sequence of operations that define the process, references the specifications that define the manner in which the operation is to be performed, and delinates special instructions related to that operation. It is a basic technical document. The special instructions are needed since most operating specifications are used solely to define methods. The specific times, temperatures, gas flow rates (not shown on our example), etc., may vary from process to process even though the methods are the same. As a result, most companies find it expedient to write one general specification on methods and a process flow chart to fill in the specific information for a given process.

Table 3.1-1 illustrates a sample process flow chart of the kind used by many semiconductor companies. This chart summarizes the critical specifications and parameters defining a specific process flow and is necessary for quality control, consistency, and reliability in manufacturing.

The process represented here is called "N" and describes the process for our model N-channel silicon gate 4K RAM. Other NMOS processes may be designated differently. Changes to this document can only occur via a written engineering change notice (ECN) or engineering change order (ECO), signed off and approved by the key engineering and manufacturing personnel.

Traveler

Wafer fabrication is often confusing to those not familiar with semiconductor manufacture because of the large number of processing steps and the fact that the wafer does not travel a clear-cut path through the wafer fabrication area. Indeed, the wafer visits each area in wafer fabrication many times before all wafer fabrication processing is completed. Because a wafer fabrication area may have batches of wafers at different stages in processing, it is necessary to keep close track of each run or batch. For this reason "run travelers" are used. The fab traveler is a card or sheet of paper that travels along with each batch of wafers through the wafer fabrication area. As illustrated in Table 3.1-2, it defines the photomask set and process to be used for a specific product.

There are also columns to log in the number of wafers received at a process step and the number out of the step, the operator's initials, date, and time. Not all companies require that the time be logged. It generally is a good practice, however, since many problems are time-oriented.

Most travelers also force the operator to record specific data related to the process, such as equipment numbers, thicknesses, oxide colors, and critical dimensions (C.D.'s—dimensions that must be held in the photomasking processes to ensure that the circuits will operate properly). These historical data are used to evaluate the consistency of a process and to track down problems that may arise.

In most cases, critical process information is not printed on the travelers for two reasons: (1) times, temperatures, and the like may change over time. It is far easier to change the flow charts and post the ECNs than it is to change each of the individual travelers; (2) one of the numerous travelers could easily get into the hands of a competitor.

TESTING

There are three places in the manufacturing processes where electrical tests are per-

3.1 Major Manufacturing Operations

Table 3.1-1

SAMPLE PROCESS FLOW CHART[1]

Process: N
Technology: N-channel, Silicon Gate

Division: MOS

Revision: A
ECN # : 306
Orig. : J. Doe
Date : 1-1-74

Operation	Spec. Ref.	Special Instructions
1. Raw Wafers	10001	3-4 ohm-cm, (100)-orientation
2. Initial Clean	20001	10 minutes
3. Initial Oxidation	20002	1150°C, 1 hr. 40 min., wet O_2, T_{ox} = 10,000Å
4. Mask: P-Beds	30001-6,9	6 min. Buffered HF
5. Gate Oxidation	20003	1150°C, 40 min. dry O_2 + 15 min. dry N_2, T_{ox} = 1350Å
6. Poly Deposition	20004	Thickness = 5000Å ± 500Å
7. Oxidation	20005	1100°C, 55 min., T_{ox} = 1200Å
8. Mask: Gate	30001-5,7,9	
9. Phosphorus Deposition	20006	V/I = 1.0, 1075°C, $POCl_3$
10. Field Vapox Deposition	20007	9000Å ± 1000Å
11. Anneal	20008	1100°C, 20 min., dry N_2
12. Mask: Contacts	30001-6,9	
13. Aluminum Evaporation	20009	6-9's pure, 12,000Å ± 1000Å
14. Mask: Metal	30001-5,8	
15. Glass Deposition	20010	9000Å ± 1000Å
16. Mask: Pad	30001-6,9	
17. Alloy	20011	450°C, 30 min.
18. Wafer Evaluation	20012	V_{to} = 1.8 – 2.2V, $BV_{DSS} \geq 25V$, $V_{TM} \geq 25V$, $V_{TP} \geq 25V$

[1] For illustration only; not intended to describe a working process

Source: DATAQUEST, Inc.

3.1 Major Manufacturing Operations

Table 3.1-2

SAMPLE TRAVELER[1]

RUN. NO. _____ PROCESS _____

MASK SET NO. _____ PRODUCT _____

Operation	In	Out	Date/Time	Operator	Spec. Instructions
Initial Clean					Standard Clean
Initial Oxidation					Fur.#____, 1150°C, wet O_2, 1 hr. 40 min., Color:_____
Mask: Bed					#____, CD = ____
Gate Oxidation					Fur.#____, 1150°C, 40 min., dry O_2 + 15 min., dry N_2,
Poly Deposition					Reactor #____, Thick.____
Oxidation					Fur.#____, 1100°C, 55 min.
Mask: Gate					#____, CD =_____
Etch Oxide					3 min. BHF
Clean					Sulfuric/Peroxide
Etch Poly					3 min. silicon etch
Etch Oxide					3 min. BHF
Phosphorus Deposition					Fur.#____, V/I =_____ 1075°C
Field Vapox Deposition					Machine #____, Th._____
Anneal					Fur.#____, 1100°C, 20 min.
Mask: Contact					#____, CD =_____
Aluminum Evaporation					Bell jar # _____ Th._____
Mask: Metal					#____, CD =_____
Glass Deposition					Machine #____, Th._____
Mask: Pad					Use Glass etch
Alloy					Fur.#____, 450°C, 30 min.
Wafer Evaluation					V_{to} =____, BV_{DSS} =____, V_{TM} =____, V_{TP} =____

[1] For illustration only; not intended to describe a working process

Source: DATAQUEST, Inc.

3.1 Major Manufacturing Operations

formed. We will discuss each test point individually and discuss their interrelationship.

Wafer Evaluation

The first test is performed immediately after the last wafer fab step, usually in the fab area. This test, called "wafer evaluation" or "wafer mapping", is performed on test devices (MOS transistors, resistors) located either on the periphery of the circuit dice or on three to five special patterns intermixed with the standard circuit patterns. The parameters measured at this step reflect the critical parameters of the process and, by implication, if these parameters meet specification then the processing has been properly performed.

Wafer Sort

The wafer sort test is also referred to as "electrical sort", "E-sort", "wafer probe", or "probe". Here, individual wafers are placed on the platform or "chuck" of a wafer probe machine. Tiny probes, resembling straight pins, are then mechanically aligned over each of the metallized pads which are located along the periphery of the die, as shown in Figure 3.1-4. Each of these probes is electrically wired to a fixture or jig that interfaces with the prober to the computer that exercises and tests the circuits. The probes are automatically "stepped" along the wafer, at each step coming down in contact with the 4 mil x 4 mil wide pads on each die (16 pads for the 16 pin 4K RAM). Every time the probes come down, a set of electrical pulses is applied to the circuit and the responses are measured. If all responses fall within some pre-established criteria, the prober proceeds directly to the next die. If a measurement fails to meet the limits, a small hypodermic needle or pen comes down and places a drop of "ink" (red food coloring) on the rejected die. The inked dice are then discarded at the first inspection (Die Visual) in the assembly process.

The objectives of wafer sort are three-fold:

- To reject potentially bad dice, so that no additional costs (such as assembly) will be incurred by them.
- To subject the die to a stringent enough test that it has a better than 70 percent chance of passing final test when it reaches that point.
- To feed back information to the wafer fab area on potential processing problems, particularly if the wafers have an inordinately high number of unacceptable (rejected) devices.

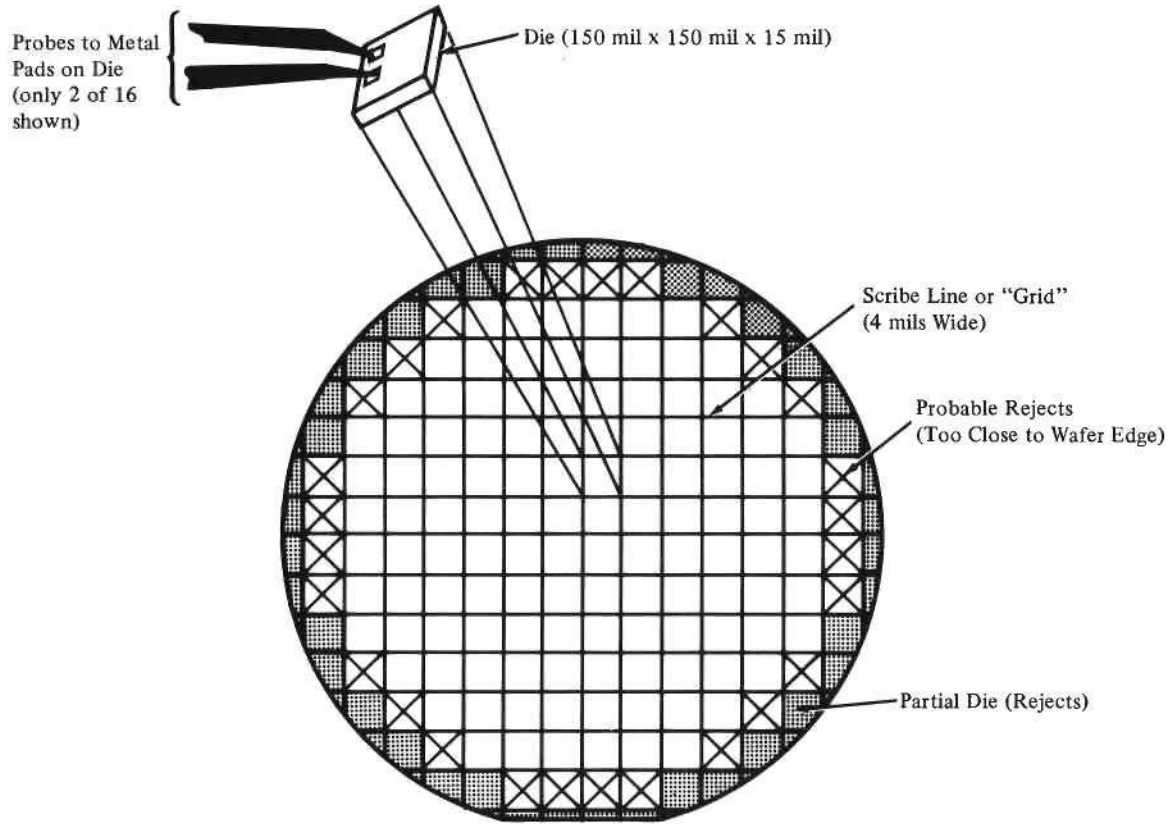
Final Test

The final test is performed after the dice have been packaged. Since the packaged units now have external leads that operators or machines can handle, this process is usually automated. The packages are received from assembly in long metal tubes, with the units stacked end-to-end. Each tube is placed vertically, one end down, in an automatic package handler. The handler, in turn, releases one package at a time, allowing it to slide to a set of contacts that match its leads (16 contacts for the 16-lead package). The contacts are wired to the automatic tester or computer.

Each unit is stringently tested at this step, across all "worst case" conditions. The circuits are exercised for maximum and minimum speeds, power dissipation, for every combination of inputs and outputs—i.e., they are tested to ensure that they will meet all of the manufacturer's specifications and guarantees. Literally thousands of separate tests are performed.

Since most circuits are guaranteed to operate over certain temperature ranges, final test must be stringent enough to ensure that the performance will be met. The environmental conditions are usually assured in either of two

Figure 3.1-4
WAFER SORT



Source: DATAQUEST, Inc.

ways:

- All devices are tested at the high temperature end of the specification or
- The devices are tested at room temperature with wide enough tolerances that operation at the temperature extremes is assured.

The first approach is obviously the safest, but it is also very expensive in terms of labor and the amount and type of test equipment required. As a result, many semiconductor manufacturers will correlate the room temperature characteristics with the characteristics at temperature extremes, add a safety guardband to the room temperature test parameters, and then test at room temperature. Samples are taken regularly from the production lots and tested across the full range of environmental conditions to ensure that the correlation continues to be accurate.

Interrelationship of Wafer Sort and Final Test

There is a very close interplay between wafer sort and final test. In fact, in most opera-

tions both test activities are located in the same room and often the same equipment is used for both, with only the test programs being different.

As we mentioned earlier, one of the functions of wafer sort is to minimize the amount of additional labor and materials that would be assigned in producing bad circuits. This factor is especially important for semiconductors with lower die costs and, therefore, relatively higher assembly costs. However, wafer sort cannot sort out all potentially defective dice for several reasons:

- Most sophisticated circuits, such as the 4K RAM, cannot be completely tested in wafer form, because of the parasitic effects resulting from the probes and wiring, incident room light, etc.
- Some of the dice may be damaged during the assembly processes.
- The dice cannot be tested across the temperature range in wafer form because the wafer (and contact probes) cannot be easily maintained at temperatures other then ambient.

The objective of wafer sort is to ensure that enough of the potentially rejectable circuits have been discarded so that final test yields will be high enough to support the desired level of profitability. Excessively high final test yields are not necessarily acceptable. They may mean that potentially good devices are being thrown away at wafer sort. As a result, most manufacturers will adjust the tightness or severity of their wafer sort tests to allow the final test yields to fall in the range of 70 to 85 percent good units.

ASSEMBLY

This section describes the assembly processes used in packaging the 4K RAM after it has been tested in wafer form. A typical assembly flow is illustrated in Figure 3.1-5 and is described below:

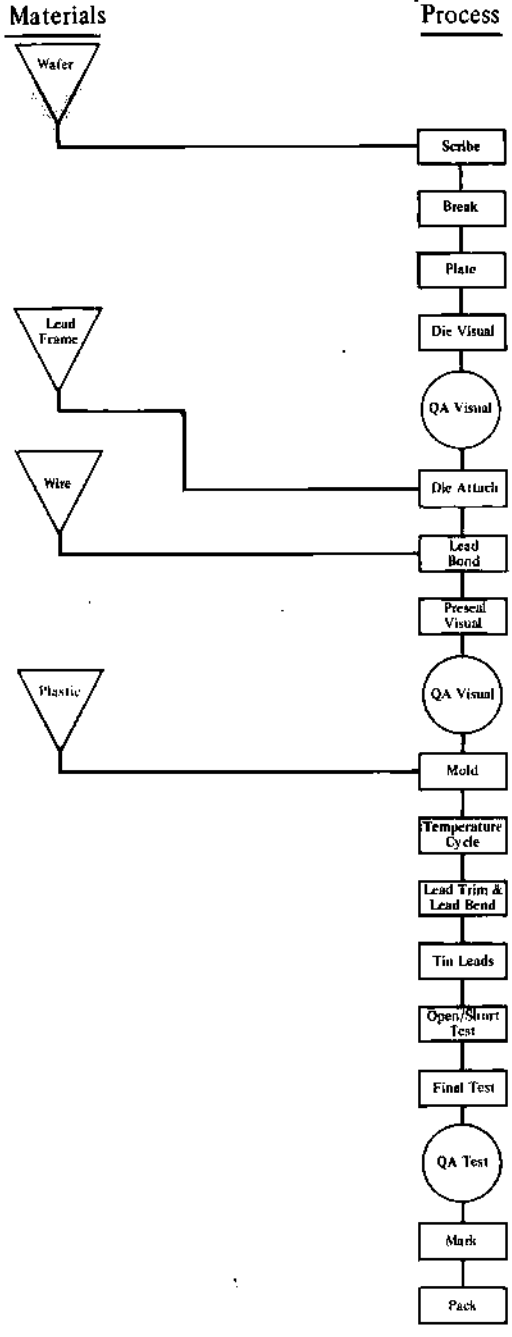
- Scribe—Wafers are received from the wafer sort area, with the bad devices inked. The wafers are placed onto scribers, which are machines that automatically pass a diamond needle along "grids" on the wafers. These grids were outlined in the circuit pattern during the masking operations and delineate the boundaries of the square or rectangular-shaped circuits. The purpose of this process is to lightly score the silicon surface (to a depth of 0.001 to 0.002 inches), so that the wafer may be easily broken along the scored lines. This process is exactly the same as that used by glass workers, when they score flat glass plates with a diamond tip to cut them.
  Recently, laser scribers have been used for many semiconductors, with the laser beam performing the "scribe". They may offer lower breakage loss and greater productivity. However, the heat generated by the laser has caused some reliability problems with N-channel silicon gate devices.

- Break—After scribing, the wafers are placed on flexible holders and aligned such that one set of parallel scribe grids is registered against a fixed calibration mark. The holder and wafer are fed into a machine (wafer breaker) which flexes the holder and wafer around a fixed radius, so that the wafer breaks along one set of grids. The process is similar to running the wafer and holder through the ringers on an old-fashioned washing machine. After the wafer is broken in one direction, the holder is turned perpendicular to the first pass and put through the flexing process again, to break it along the second set of scribe lines. When the wafer comes out of this second pass, all the individual circuits have been separated and

3.1 Major Manufacturing Operations

Figure 3.1-5

ASSEMBLY WORK FLOW



Source: DATAQUEST, Inc.

each circuit is now referred to as a "die".

- Plate—The operator separates the good and reject dice at this point, using a pick-up tool. All rejected dice, with ink dots on them, are discarded and all good dice are placed in orderly rows on a square plate.

- Die Visual—The plate of dice is placed under a microscope and each die is inspected according to preset visual quality criteria. Gross contamination, scratches, and broken dice are reasons for rejection.

- Die Attach or Die Bond—The good dice are now mounted into packages. An empty package frame is placed on a heating block and heated to 400 degrees centigrade. In some cases, a thin square of gold, slightly smaller than the die itself, is then placed on the package where the die is to be attached. Most companies, however, do not use this approach but purchase packages with thicker gold on the die bond area, to save time and labor. The operator picks up the die by its edges, with a pair of tweezers, and gently forces the botton of the die onto the thick-plated gold area. The gold immediately becomes a conductive "glue" which holds the die to the package.

- Lead Bond or Wire Bond—Bonding is accomplished in either of two ways. For plastic packages, gold wire is used due to its superior strength to connect the individual 4 mil x 4 mil aluminum pads on the die to the corresponding leads on the package. For ceramic packages, either gold or aluminum wire is used.
  In gold bonding, the package is heated to 340 degrees centigrade. Looking through a microscope and manipulating a joystick controller, the operator positions the tip of a gold wire directly over a pad on the die.

When the alignment is complete, the gold wire (0.001 to 0.0015 inches in diameter) is forced down on the pad and adheres. The operator then trails out gold wire until reaching the corresponding pad in the package. Again, after alignment, the wire is brought down on the package pad and the excess wire is automatically severed at the pad. This process is repeated until all pads on the die have been bonded to the corresponding package pads.
In aluminum bonding the basic bonding operation is the same except that instead of heating the package ultrasonic agitation of the wire is used to make the contact with the pads by a "scrubbing" action.

- Preseal Visual—This visual is performed to screen out any units that may have been damaged during the previous assembly steps. Unbonded pads, broken wires, chipped dice, and loose dice are reasons for rejection.

- Mold (plastic) or Seal (ceramic)—Plastic packaging is the lowest cost of all methods of semiconductor encapsulation. In plastic packages, the frames holding the die are placed in molds and molten plastic is injected into the mold to form the package body. After removal from the mold, the packages are cured in an oven at around 200 degrees centigrade. Ceramic packages must be sealed with a metal lid to make them airtight. Different methods are used, but all require running the device (with the lid) through a long sealing furnace.

- Temperature Cycle—One hundred percent of the units are cycled at temperatures between -55 degrees centigrade and +150 degrees centigrade, five times, to check for lead bond integrity.

- Centrifuge—This test would not be performed on our plastic package 4K RAM, since the leads are buried in the plastic encapsulant, but is used for ceramic or metal packages. In this test, a centrifuge is used to accelerate the packages to 30,000 g's to stress the leads and bonds. This check not only tests for mechanical integrity, but also serves as a screen to determine whether the wire is too close to the bottom of the lids and therby a potential circuit failure.

- Fine and Gross Leak—Like the centrifuge test, these tests would not be performed on plastic packages, since they have no cavities. The purpose of these leak tests is to ensure that the lids are properly sealed to the package, so that the die is protected from ingression of contaminants.

- Lead Trim and Lead Bend—Up to now, several packages have been connected in strips by additional metal between the leads on the packages. At this step a special lead trimmer cuts off this extra metal separating both the packages and the individual leads on each package. The leads are then bent at right angles (90 degrees) to the bottom of the package.

- Open/Short Test—This is a simple electrical test, usually performed on a homemade test box, which checks package leads to determine whether any are electrically shorted together or open. It is performed primarily by overseas assembly plants as a monitor of assembly quality.

- Electrical Test or Final Test—This step was described previously under testing.

- Mark or Symbol—This step also can be performed prior to final test. It consists of stamping identification information onto the

package: part number, manufacturer, a coded date, and origin of assembly (if overseas). It is usually performed after the final test step because different part types may be derived from the same basic die, simply by defining different performance criteria. For example, a high speed part may be designated with a "-1".

- Pack—Completed units are packed with their leads shorted together, using conductive foam or aluminized containers, labeled, and readied for shipment to the customer.

SUPPORT ACTIVITIES

To this point, no mention has been made of the other support groups that are vitally important to the success of the manufacturing operations. We will briefly discuss the key groups in this section.

Circuit or Product Design

The function of the design group is to take marketing and customer inputs and design the circuits needed to perform the desired electrical functions. The inputs take the form of a specification of a function to be performed. The design group then determines the best circuitry and technology to generate the function. A designer simulates the circuit, section by section, on a computer (computer-aided design or CAD) to determine the optimum design. The circuit is designed using the outputs of these simulations and photomasks are generated for the manufacturing area.

Product Engineering

Product engineering is generally considered to be an integral part of the manufacturing operation, even though circuit design is not. The function of the product engineer is multifaceted and he in many respects is one of the most important individuals in the manufacturing operation.

The product engineer works with the circuit designer as a product is being conceptualized and designed. As the circuit reaches the hardware stage in the form of wafers, the product engineer either writes or aids the designer in writing the electrical test programs for wafer sort and final test. After the first devices are obtained, he is responsible for fully characterizing the circuits over the full performance range to ensure that they meet the specifications.

Once the product has been released to the manufacturing area by the product engineer, it is his responsibilty to ensure that it continues to be manufactured economically, i.e., good yields. Problems that arise at wafer sort and final test are his responsibility. He must be certain that the products leaving those areas meet the specifications. However, he is also responsible for ensuring that the manufacturing personnel can move the product "out the door" and on to the customers.

Since he neither designs nor manufactures the product, the product engineer is in the unique position of coordinating the communication between the two areas. With his sophisticated testers, he can help to isolate whether a reject is process or design oriented. This function is important because most process engineers know little about designing circuits and most designers know little about processing.

Process Engineering

Process engineering is implicitly or explicitly divided up into manufacturing or sustaining engineering and process development.

Sustaining engineering usually is just that—solving the day-to-day problems as they arise so that production can be sustained. It is commonly referred to as "fire fighting". In most companies, the function of sustaining en-

gineering is to "keep production running". Like the product engineer, the process engineer is often faced with the decision of whether to maintain a high level of quality versus "getting products out the door".

Process development, in a manufacturing operation, relates to short term work aimed at desensitizing a particularly troublesome process, improving productivity through a process, and developing other methods of lowering costs (methods for reducing chemical usage, etc.).

Quality Assurance

Quality assurance (QA) is extremely important in any manufacturing process, but probably most important in an MOS manufacturing operation. Since an MOS circuit or transistor cannot be tested until the last step of the process (wafer evaluation), its process controls are implicit. That is, test wafers are run through individual processes to qualify that process as being "in specification". The production wafers are then put through the process based on the observation that the test vehicle met the proper specifications. In other IC processes, it is possible to measure the results of that process step directly on the production wafer as soon as it comes out of the process. In MOS, one assumes or implies that the product is "within specification" because the test vehicle was within the specified tolerances.

Obviously, the interpretation of "in specification" may vary considerably from operator to operator, foreman to foreman, and engineer to engineer. The function of QA is to ensure that documentation is maintained on every process, that controls are established at the critical steps, that the controls are monitored (and meaningful) and that warning flags are raised when out-of-specification conditions occur. Although our initial example related to wafer fab, these same responsibilities hold throughout the manufacturing operations, including assembly and test.

Maintenance

Maintenance and preventive maintenance are becoming important functions in MOS operations. Process and test equipment are becoming more sophisticated all the time. Process equipment is filled with many of the same integrated circuits that it builds, and testers have become small special purpose computers. Each of these must be continually maintained and repaired, so that the manufacturing operation can run smoothly and economically. This is discussed in greater detail in Section 3.

EFFECT OF PRODUCT AND/OR PROCESS CHANGES

Variety of Processes

Throughout the course of the previous discussions, we have indicated that the number of processing steps for an N-channel silicon gate MOS product depends on the particular manufacturer, because an N-channel process can be put together many different ways to fabricate the same product. Some process steps are added by manufacturers to provide performance advantages, some are added to circumvent processing problems, and some are added to increase wafer yield.

Because of the differences in processes, it is difficult for the casual observer to readily determine the capacity of a given wafer fab facility, for instance, without knowing something about the process employed. For example, if a manufacturer has 24 furnace tubes, compared with his competitor's 12, does he really have twice the capacity? It could be that he needs all 24 for his process while his competitor needs only 9.

3.1 Major Manufacturing Operations

We have chosen a relatively short version of the N-channel silicon gate MOS processes currently being used, because in the future economics will favor the shorter processes as the selling price for the 4K RAM drops to $4.00. The cost impact of longer processes is discussed in detail in Section 2.

Interrelationship of Product and Processes

The interrelationship of product and process is becoming more critical as larger, more complex, higher performance circuits are being designed. It is not uncommon for a semiconductor manufacturer to use two or three N-channel silicon gate processes to support specific products. For instance, he might have one process for producing low voltage, slow RAMs, such as the present 1,024 bit static RAMs, another for the high speed, more complex 4,096 bit dynamic RAMs, and still another for high speed microprocessors. Each of the circuits is designed for a specific process, and each of the processes is optimized to allow the circuit to have the best performance possible—at a minimum cost.

This process optimization around a product is often almost accidental. A manufacturer determines that the performance specifications cannot be met with the standard process or that the product cannot be manufactured at low enough costs even though it meets the performance criteria. When these problems arise, either one or both of two things happen: (1) the product is redesigned to optimize its performance or yield at a given process or (2) the process is "modified" to allow the existing product design to meet performance specifications.

In the majority of cases, the processes are modified, because it is faster than redesigning a circuit that might have been six months in the making. Photomask dimensions are skewed (larger or smaller), diffusions are shortened or lengthened, oxide thicknesses are increased or decreased—whatever it takes to achieve the circuit yield. The result is twofold: "tailor-made" processes are generated, and an initial increment of circuits is available for the marketplace. The dangers are obvious: special handling in large volume manufacturing areas can lead to operator errors and inefficiency. So many of the interrelated and interactive processes may have been modified, that the margin of safety for consistently running the process may have been substantially reduced.

3.2 Manufacturing Cost Analysis

The important cost contributions related to the manufacture of N-channel silicon gate MOS 4K RAMs are discussed in this section. Detailed costs are discussed for materials, labor, and capital, and these costs are segmented for each of the major manufacturing steps, that is, wafer fabrication, assembly, and both wafer sort and final test. Total costs are broken down and calculated for either a single chip or a single wafer. However, because there is considerable attrition of devices throughout the assembly process, yield at the various manufacturing steps is an important factor in calculating the final cost of a finished unit. The relationship between the costs of an individual step at any point in the manufacturing process and the yielded cost, which accumulates throughout the manufacturing process, must be kept in mind.

YIELDS

Yields play an important part in determining the final cost of an integrated circuit. For a relatively complex IC, the final number of devices compared with the original number of dice started can be as low as 5 percent. Manufacturing yields can vary tremendously among manufacturers and play a dominant role in determing the cost competitiveness of a manufacturer. To determine the standard cost for a device, its manufacturing yields must be estimated. Typical yields are shown in Table 3.2-1 for wafer fabrication and wafer sort, and in Table 3.2-2 for assembly and test. These represent reasonable yields which one might expect to see in an efficient MOS IC manufacturing operation.

The basic yields used in this model are:

- 70 percent cumulative wafer fab yield
- 7 percent rework rate in wafer fab
- 10,000 good wafers produced per month
- 250 total devices per wafer
- 12 percent wafer sort yield
- 86.8 percent assembly yield
- 75 percent final test yield

Table 3.2-1

TYPICAL WAFER FAB YIELDS

Process Step	Yield	Cumulative Yield
Wafer Fab		
Initial Clean	99.5%	99.5%
Initial Oxidation	99.5	99.0
1st Mask	98	97.0
Gate Oxidation	99	96.1
Poly Silicon Deposition	99	95.1
Oxidation	99	94.1
2nd Mask	95	89.4
Phosphorus Deposition	98	87.7
Field Vapox Deposition	97	85.0
Anneal	99	84.2
3rd Mask	97	81.6
Evaporation	99	80.7
4th Mask	97	78.4
Glass Deposition	98	76.8
5th Mask	99	76.0
Alloy	100	76.0
Wafer Evaluation	92	70.0
Wafer Sort	12	8.4

Source: DATAQUEST, Inc.

The volume of wafers, dice, and packaged units is summarized in Table 3.2-3 for our manufacturing model. These numbers show that about 195,000 4K RAMs per month would be manufactured from the 14,300 wafers started into wafer fab. At a $4.00 average selling price, the projected sales revenue would be $781,000 per month or $9,374,000 per year. The impact of yield on cost is discussed later in this section.

MATERIALS

Materials are an important cost factor, particularly in wafer fabrication. For a complex

3.2 Manufacturing Cost Analysis

Table 3.2-2

TYPICAL ASSEMBLY AND TEST YIELDS

Assembly Step	Yield	Cummulative Yield
Assembly		
Scribe	100%	100%
Break	100	100
Plate	98	98
Die Visual	95	93.1
Die Attach	99	92.2
Lead Bond	98	90.3
Preseal Visual	98	88.5
Mold	99	87.6
Temperature Cycling	100	87.6
Lead Trim & Bend	99	86.8
Test[1]		
Final Test	75	65.1
Mark	100	65.1
Pack	100	65.1

[1]Centrifuge, Gross and Fine Leak Tests are not performed on plastic packages and therefore omitted.

Source: DATAQUEST, Inc.

device, such as the 4K RAM used in this manufacturing model, wafer fabrication costs predominate and silicon wafers and photomasks are an important component of that cost. For simpler devices where assembly costs are a much larger percentage of the final cost of the device, packaging costs are extremely important. Major material cost items are discussed below. A summary of these costs for each manufacturing area, including rent, is shown in Table 3.2-4.

Silicon Wafers

The cost of silicon wafers has continued to rise over the past year. In 1973, a 3-inch diameter MOS wafer could be purchased for under $6.00, but the price for large volumes rose to $7.00 in 1974. The $7.00 figure is assumed in our cost calculations. At a 70 percent fab yield, the yielded raw wafer cost would be $10.00 for each good wafer.

Table 3.2-3

MONTHLY WAFER DIE AND UNIT VOLUMES

Manufacturing Step	Yield (%)	Cumulative Yield (%)	Quantity into Step
Wafer Starts			14,300 wafers
Wafers Out of Fab	70%	70%	10,000 wafers
Wafer Sort	12%	8.4%	10,000 wafers (2.5 million die)
Scribe and Break	100%	8.4%	10,000 wafers (300,000 good die)
Plate	98%	8.2%	300,000 die
Die Visual	95%	7.8%	294,000 die
Die Bond (Attach)	99%	7.7%	279,300 die
Lead Bond	98%	7.6%	276,500 units
Preseal Visual	98%	7.4%	271,000 units
Mold	99%	7.4%	265,600 units
Temperature Cycling	100%	7.4%	262,900 units
Lead Trim and Bend	99%	7.3%	262,900 units
Final Test	75%	5.5%	260,300 units
Mark	100%	5.5%	195,200 units
Pack	100%	5.5%	195,200 units

Source: DATAQUEST, Inc.

3.2 Manufacturing Cost Analysis

Table 3.2-4
UNIT MATERIAL COSTS

Area	Unit Cost[1]
Wafer Fab	$21.70
Wafer Test	$0.0002
Assembly	$0.056
Final Test	$0.0020

[1] Per wafer out, die tested, unit tested, or unit assembled.

Source: DATAQUEST, Inc.

Photomasks

Photomasks are the second most costly material used in manufacturing 4K RAMs. The quality level of these masks must be exceptionally good for reasonable yields to be obtained. Typical quality levels range from 10 to 20 percent of potentially defective dice per good mask. If each of these defects on the mask is translated to a die on a wafer, then for a five mask process about 67 percent of the die would be defective from the 20 percent defective masks, versus 41 percent from the 10 percent defective masks.

As described in Section 1, the photomask is brought into contact with the wafer during the alignment and exposure process steps. The contact aids in the definition of the images, but also causes a rapid degradation of the mask quality. Scratches, photoresist clumps, fractures of the glass plate, and the like, all contribute to an increasingly higher defect density with use.

For a 150 mil x 150 mil die, an emulsion photomask would typically be used for only five exposures (contacts) and would then be discarded. Each of these masks costs approximately $5.00, resulting in a materials cost of $1.00 per alignment. Assuming a 7 percent rework rate, the total mask cost per wafer would be $5.35.

Chemicals

Chemical costs are approximately $2.25 per good wafer for this five-mask process and a volume of 10,000 good wafers per month. Chemicals are used in all phases of wafer fabrication including diffusion, deposition, and masking.

Indirect Supplies

Indirect supplies include quartzware, susceptors, clean room attire, and so forth, and amount to approximately $2.50 per wafer out.

Utilities

Gases used in wafer fabrication run approximately $0.50 per wafer out and DI water is $0.60 per wafer out.

Packages

Packages for the 4K RAM are assumed to be plastic 16-pin dual inline packages (DIPs). Typical material costs for this package, in large volumes, would be $0.050, broken down as follows: lead frame $0.020, gold wire $0.025, and plastic $0.015.

Rent

Space requirements for a manufacturing plant are discussed further in Section 3.4. At 10,000 wafers out per month and a 10,000 square foot wafer fab facility, the rent amounts to about $0.50 per wafer. Assembly rent is about $0.006 per unit in assembly for an Asian facility (or about $0.02 for a U.S. facility). Rent attributable to testing is about $0.0002 per die

tested and about $0.002 per final tested unit.

LABOR COSTS

The manpower requirements for the three manufacturing operations are summarized in Table 3.2-5. Each of the areas is shown with the key personnel broken out by categories, with support groups included. Four supervisory personnel are also required, and their cost is allocated among the major areas.

A total of 105 production operators are required,(using U.S. assembly) of which 93 (89 percent of the total) work for the labor-intensive wafer fab and assembly operations. Asian assembly would require about 22 more operators.

The number of manufacturing personnel required and the allocation of those personnel depend heavily on the efficiency of the manufacturing operation and the yields at various points in the process. Not only is semiconductor manufacturing highly labor-intensive, but the attitudes of the workers, their training, and the organizational efficiency of the plant can vary widely. These variances can have a very marked effect on the cost of the final product and the competitiveness of a manufacturer.

Changes in yield will necessarily alter the number of operators required at any particular manufacturing step. For example, an increase in the number of good dice per wafer (either from improved yields at wafer sort or smaller dice) can decrease the number of personnel required in wafer fabrication relative to the other areas.

Wafer Fab

Within wafer fab itself, 32 of the 45 fabrication production operators (78 percent of fab and 30 percent of the total) are required for masking, indicating that the masking processes are the most labor-intensive of the fab processes (see Table 3.2-6).

The support group labor is derived from costs for maintenance, fab supervision, QA, PC, engineering and indirect fab personnel. The management contribution relates to fab's allocation of costs for salaries of the managers directing those activites.

Test

Labor costs for wafer sort and final test are broken down in Table 3.2-7. Direct labor costs per die into wafer sort (unyielded) are $0.0014/die, and additional overhead labor and benefits costs add another $0.0033 per die, or a total of $0.0047/die into wafer sort.

Final Test labor costs amount to $0.013 per unit for direct labor, $0.025 for overhead-related labor charges, and $0.006 for employee benefits, giving a total of $0.044 per unit into final test (out of assembly).

It should be noted that as a convention for wafer sort, assembly and final test the costs are stated as a function of the number of units into the step. Wafer costs are stated as a function of the number of wafers out.

Assembly

Assembly-related labor costs are summarized in Table 3.2-8. If the assembly is performed in the United States, the total assembly labor per package out is $0.155. This cost is high for a plastic, 16-lead package and reflects the high cost of U.S. labor and the labor intensiveness of the assembly processes.

The labor content for Asian assembly is about $0.043 per package out. However, labor rates can vary considerably from country to country. Some extra expenses are incurred if an Asian facility is used. Nevertheless, the total cost of $0.058 per unit, compared with the U.S. labor cost of $0.155, is still much lower. For devices with lower chip costs, the difference be-

3.2 Manufacturing Cost Analysis

Table 3.2-5

MANPOWER REQUIREMENTS[1]

Area	Production Operators	Quality Assurance Operators	Manufacturing Technicians	Foremen	Process/ Product Engineers	Maintenance	Production Control	Total
Wafer Fab								
Masking	32		2	2				
Deposition	8		4	2				
Diffusion	5							
Sub-Total	45	2	6	4	4	4	2	67
Test								
Wafer Sort	6							
Final Test	6							
Sub-Total	12	2	2	2	1	2	1	22
Assembly (U.S.)	48	2	2	2	1	2	2	59
Grand Total:	105	6	10	8	6	8	5	148

Supervisory Personnel
- 1 Quality Assurance (QA) Supervisor
- 1 Production Control (PC) Supervisor
- 1 Engineering Manager
- 1 Operations Manager

[1] Assumption
- 10,000 3-inch wafers out per month
- 195,000 unit ships per month
- 2 shifts, 20 days per month

Source: DATAQUEST, Inc.

tween Asian and U.S. assembly cost is increasingly important.

CAPITAL COSTS

Table 3.2-9 summarizes the capital costs, by area, for the manufacturing model. Identification, costs, and quantities required are summarized in the Appendix (Section 6). For each piece of equipment the capital costs also reflect a 6 percent sales tax. Monthly depreciation expenses, amortized against the product (wafers, dice, packaged units) are shown in the right-hand column. For purposes of simplicity, a five-year straight line depreciation schedule was assumed, rather than sum-of-digits. Salvage value was assumed to be zero. No attempt was made to estimate capitalized installation costs for which the accounting varies from company to company.

Wafer fab equipment is expensive to install. A rough rule of thumb for installation costs would be 10 percent of the total fab capital purchases, which amortizes to an extra $0.12 per wafer out. The impact of the amortization of installation costs for wafer sort, final test, and assembly would be insignificant against dice in, units in, and assembly out measures.

The following additional observations can be made regarding capital expenditures:

3.2 Manufacturing Cost Analysis

Table 3.2-6
WAFER FAB LABOR COSTS

Process/Task	Annual Salary	Number of Personnel Required	Total Cost (Annual)	Cost per Wafer Out
Direct Labor Costs				
Masking Area				
Coat and Dry		2		
Develop and Bake		2		
Align		10		
In Process Inspection		6		
Etch and Clean		4		
Final Inspection		6		
Mask Dispense		2		
Masking Total	$ 7,000	32	$224,000	$1.87
Deposition Area				
Poly Deposition		2		
Field Oxide Deposition		2		
Metal Deposition		2		
Glass Deposition		2		
Deposition Total	7,000	8	$ 56,000	$0.47
Diffusion Area				
Diffusion Total	7,000	5	$ 35,000	$0.29
Total Direct Labor		45	$315,000	$2.63
Indirect and Support Labor				
QA Operations	7,000	2	14,000	
Technicians	9,000	6	54,000	
Foremen	15,000	4	60,000	
Process Engineers	18,000	4	72,000	
Maintenance	12,000	4	48,000	
Production Control	7,000	2	14,000	
Total		22	$262,000	$2.18
Allocated Labor Overhead				
QA Supervisor	18,000	.33	5,950	
Production Control Supervisor	18,000	.33	5,950	
Engineering Manager	25,000	.33	8,250	
Operations Manager	35,000	.33	11,550	
Total		1.33	$ 31,700	$0.26
			$608,700	$5.07
Employee Benefits (15%)			91,300	0.76
Total Wafer Fab Labor Contributed Cost			$700,000	$5.83

Source: DATAQUEST, Inc.

3.2 Manufacturing Cost Analysis

Table 3.2-7

TESTING LABOR COSTS

Personnel	Annual Salary	Number of Personnel Required	Total Cost (Annual)	Cost per Unit[1]
Wafer Sort				
Direct Labor				
Operators	$ 7,000	6	$ 42,000	$0.0014
Indirect and Support Labor				
Test Supervisor	18,000	.5	9,000	
QA Operator	7,000	1	7,000	
Technician	9,000	1	9,000	
Foreman	15,000	1	15,000	
Engineer	18,000	.5	9,000	
Maintenance	12,000	1	12,000	
Product Control	7,000	.5	3,500	
Total Indirect Labor			$ 64,500	$0.0022
Allocated Labor Overhead				
QA Supervisor	18,000	.166	3,000	
Product Control Supervisor	18,000	.166	3,000	
Engineering Manager	25,000	.166	4,170	
Operations Manager	35,000	.166	5,830	
Total Allocated Labor			$ 16,000	$0.0005
			$122,500	$0.0041
Employee Benefits (15%)			18,400	0.0006
Total Wafer Sort Labor Cost			$140,900	$0.0047
Final Test				
Direct Labor				
Operators	$7,000	6	$42,000	$0.013
Indirect and Support Labor				
QA Operator	7,000	1	7,000	
Technician	9,000	1	9,000	
Foreman	15,000	1	15,000	
Engineer	18,000	.5	9,000	
Maintenance	12,000	1	12,000	
Production Control	7,000	.5	3,500	
Test Supervisor	18,000	.5	9,000	
Total Indirect Labor			$ 64,500	$0.020
Allocated Labor Overhead				
QA Supervisor	18,000	.166	3,000	
Production Control Supervisor	18,000	.166	3,000	
Engineering Manager	25,000	.166	4,170	
Operations Manager	35,000	.166	5,830	
Total Allocated Labor Overhead			$ 16,000	$0.005
			$122,500	$0.038
Employee Benefits (15%)			18,400	0.006
Total Final Test Labor Cost			$140,900	$0.044

[1] Die into wafer sort, or unit into final test.

Source: DATAQUEST, Inc.

3.2 Manufacturing Cost Analysis

Table 3.2-8
ASSEMBLY LABOR COSTS

Personnel	Annual Salary	Number of Personnel Required	Total Cost (Annual)	Cost per Unit[1]
United States				
Direct Labor				
Operators	$ 7,000	48	$336,000	$0.093
Indirect and Support Labor				
QA Operators	7,000	2	14,000	
Technicians	9,000	2	18,000	
Foremen	15,000	2	30,000	
Engineer	18,000	1	18,000	
Maintenance	12,000	2	24,000	
Production Control	7,000	2	14,000	
Total Indirect Labor			$118,000	$0.033
Allocated Labor Overhead				
QA Supervisor	18,000	.33	6,000	
Product Control Supervisor	18,000	.33	6,000	
Engineering Manager	25,000	.33	8,330	
Operations Manager	35,000	.33	11,670	
Total Allocated Labor			$ 32,000	$0.009
			$486,000	$0.135
Employee Benefits (15%)			72,900	0.020
Total U.S. Assembly Labor Cost[1]			$558,900	$0.155
Asia				
Direct Labor				
Operations	$620	72	$ 44,600	$0.012
Indirect and Support Labor				
QA Operator	1,000	5	5,000	
Technicians	1,200	4	4,800	
Foreman	1,200	6	7,200	
Engineer	2,000	1	2,000	
Maintenance	1,200	4	4,800	
Production Control	1,000	4	4,000	
Asst. Plant Managers	2,500	2	5,000	
Plant Manager (American)	35,000	1	35,000	
			$ 67,800	$0.019
Allocated Labor (same as United States)			$ 32,000	$0.009
Employee Benefits[2] (15%)			10,000	0.003
Total Asian Assembly Labor Cost			$154,400	$0.043
Extra Costs of Asian Assembly (Duty, Air Freight, Communication, Transportation)			54,900	0.015
Total Cost of Using Asian Labor			$209,300	$0.058

[1] Costs reflects units into assembly
[2] U.S. labor only, Asian labor rates include benefits

Source: DATAQUEST, Inc.

3.2 Manufacturing Cost Analysis

Table 3.2-9
CAPITAL COSTS

Area	Capital Equipment Cost (Thousands of Dollars)	Unit Depreciation Expense (Dollars)
Diffusion	$ 195.7	$0.325
Masking	291.4	0.486
Deposition	233.2	0.389
Total Wafer Fabrication	$ 720.3	$1.200
Wafer Sort	172.8	0.0012
Final Test	352.5	0.022
Total Testing	$ 525.3	
Assembly (Total)	196.5	0.011
Total, all manufacturing	$1,442.1	

[1] Per wafer out, die tested, unit tested, or unit assembled

Source: DATAQUEST, Inc.

- Wafer fab capital costs of $720,300 represent 50 percent of the total capital equipment requirements for the manufacturing model. If wafer sort were considered to be part of wafer fab, as it is in some companies, the fab-related equipment costs would rise to $893,100 or 62 percent of the total cost. This huge capital investment is one of the reasons why volume is so important to IC manufacturing.

- The deposition process in our manufacturing model consists of only four process steps (poly, field vapox, metal, and glass) out of those major steps listed in Figure 3.1-5. However, the capital-related expense amounts to 31.4 percent ($0.389 of $1.20) of the total capital contributed wafer cost.

- The wafer fab capital costs reflect only the process described for the manufacturing model. A longer process or one with poorer manufacturing yields could greatly increase the equipment requirements. For example, an ion implantation step could require up to $100,000 worth of equipment.

- Final test capital costs are necessarily higher than wafer sort, because of the need for a more sophisticated tester to thoroughly exercise the 4K RAM as well as perform tests not possible at wafer sort.

CUMULATIVE COST

The cumulative manufacturing cost for the plastic packaged, 16-pin, 4K RAM is shown in Table 3.2-10. These costs reflect the manufacturing model and all of the assumptions related to it. Because the assumptions for yields, productivity rates, and the like differ from company to company, the costs in Table 3.2-10 should be used primarily as a guide. The unit costs for each of the manufacturing areas are

3.2 Manufacturing Cost Analysis

summarized in Table 3.2-11 through 3.2-14.

The wafer cost (Table 3.2-11) is within the achievable range, but probably on the low side. Other additional engineering and supervision costs, such as office space, secretarial help, and office supplies, have not been added into this wafer cost figure. Total manufacturing cost of a more fully allocated overhead burdened wafer might be $30 to $35.

Final test costs include some unidentified costs of about $0.02 per unit tested. This addition brings the total cost per unit for final test to about $0.09 per unit. Those units that pass final test, of course, must be packed and shipped. These costs amount to about $0.02 per unit, although for higher volume, lower cost products this cost can be considerably lower.

The outcome of these calculations indicates that a 4K RAM from our manufacturing model can be manufactured for $1.88. With overhead and profit margins, this cost would support a $4.00 selling price.

This manufacturing cost is lower than might be expected for two reasons. First, we have assumed a manufacturing model tailored to run only one process (N-channel silicon gate MOS), one product (4K RAM), and one package type (16 pin plastic). The process is assumed to be running smoothly and the product is assumed to be well designed and capable of being manufactured. Consequently, personnel and equipment are used very efficiently and

Table 3.2-10

PRODUCT COST ANALYSIS

Reference Code	Production Step		Unit Cost ($)
A	Wafer Cost (from Table 3.2-11)	$28.73	
B	Number of die per wafer[1]	250	
C	Cost per die out of Wafer Fabrication (A ÷ B)		$ .115
D	Wafer Sort Costs (from Table 3.2-12)		.006
E	(C + D)		$ .121
F	Wafer Sort Yield	12%	
G	Cost per die out of Wafer Sort (E ÷ F)		$1.008
H	Assembly Costs (from Table 3.2-13)		.125
I	(G + H)		$1.133
J	Assembly Yield (from Table 3.2-2)	86.8%	
K	Cost per unit out of assembly (I ÷ J)		$1.305
L	Final Test Costs (from Table 3.2-14)		.090
M	(K + L)		$1.395
N	Final Test Yield (from Table 3.2-2)	75%	
O	Cost per unit out of Final Test (M ÷ N)		$1.860
P	Packing and Shipping Costs (from Table 3.2-14)		.020
	Total Unit Manufacturing Cost (O + P)		$1.880

[1] Die size 150 mils square, 3 inch wafer with 20% die edge loss.

Source: DATAQUEST, Inc.

3.2 Manufacturing Cost Analysis

Table 3.2-11

WAFER FABRICATION COSTS

Material and Rent	$21.70
Labor	5.83
Capital	1.20
Total Cost per wafer out of Wafer Fabrication	$28.73

Source: DATAQUEST, Inc.

Table 3.2-12

WAFER SORT COSTS

Material and Rent	$0.0002
Labor	0.0047
Capital	0.0012
Total Cost per die into Wafer Sort	$0.0061

Source: DATAQUEST, Inc.

Table 3.2-13

ASSEMBLY COSTS

Material and Rent	$0.056
Labor (Asian assembly)	0.043
Capital	0.011
Extra Costs of Asian assembly	0.015
Total Cost per unit into Assembly	$ .125

Source: DATAQUEST, Inc.

Table 3.2-14

FINAL TEST COSTS

Material and Rent	$0.002
Labor	0.044
Capital	0.022
Nonidentified Costs	0.022
Total Cost per unit into Final Test	$0.090
Packing and Shipping Cost	$0.020

Source: DATAQUEST, Inc.

consistent yields are predictable. Usually a manufacturing operation will run a number of products and package types and as many as 2 to 5 process flows, so that efficiency is less than it is for our model.

Second, the manufacturing volume used in this model and the implied learning curve has not yet been achieved by any manufacturer. Currently, volume manufacture is just beginning for 4K RAMs, and not all manufacturing problems have been solved. Although a manufacturer may have a yield at any given point in the manufacturing process similar to those outlined here, generally there will be some areas in its manufacturing process where yields are not as good or not as consistent. In short, smoothly running 4K manufacturing facilities have yet to be achieved. However, Dataquest expects the yields and costs outlined here to be achieved by the end of 1975.

PROFIT/COST CONSIDERATIONS

Yield

There are many different yield points in each of the manufacturing processes—and many different definitions of each of the yield points. Some of the definitions are interchanged in day-to-day conversation, so that it is difficult for the observer to understand how meaningful the yield number is that has been given to him. In this section, we define the various yield points and discuss their interpretation.

Wafer Fabrication

Most wafer fabrication managers use cumulative wafer fabrication yield or fab yield as a measure of their performance. This yield is defined as the number of wafers into wafer sort (out of wafer fab) divided by the number of wafers started in wafer fab (at initial or wafer

clean), times 100. Hence, if 30 wafers are transferred to wafer sort out of the 50 started, the fab yield is said to be 60 percent. However, this number can be arrived at in two different ways. One way is to tally the wafer fab travelers as the batches or "runs" of wafers are transferred to wafer sort. This would not include a run that might have been completely destroyed earlier in the process and would never have made it to the wafer sort area. A second, and preferred, method is to include all wafers started in fab yield calculations.

"Cumulative" yield is obtained by multiplying the yields at each of the process points within the wafer fab process. This yield may change daily because of the effect of small batches of wafers processed through a given step. That is, if ten wafers are processed at one of the process steps and only five pass, the best the cumulative yield can be is 50 percent. However, this yield smooths out as data are collected over a period of time (one week or more) and better reflects the performance of the wafer fab area.

In this report, we will use the term fab yield in the same context and with the same definition as cumulative yield. The effect of cumulative yield is dramatic. If the fab yield in our manufacturing model dropped from 70 to 50 percent, we would have to start 5,700 additional wafers per month. This translates into the following cost impacts:

- At $7.00/raw wafer, the direct materials cost is increased by $40,000 per month.
- Work-in-process (WIP) wafers (assuming an ideally balanced line) rises by more than 1,100 wafers. The value of these additional wafers depends on the average work-in-process wafer value, typically $15,000.
- The number of alignments increases by 15,500 per month, at a 7 percent rework rate, resulting in the need for two additional alignment operators and one additional alignment jig.
- At $5.00 per emulsion photomask and five alignments per mask, the additional mask costs would be $15,500 per month.

Accounting only for these simple considerations, the increased expense of supporting a 50 versus 70 percent wafer fabrication yield is more than $70,000 per month or more than $7.00 per additional wafer out of fab.

At 10,000 3-inch N-channel silicon gate MOS wafers per month, the fully allocated manufacturing burden was approximately $30 for the process described in the manufacturing model. The extra $7.00 resulting from the 50 versus 70 percent yield would add 23 percent to the finished wafer cost.

Rework yields

Masking reworks arise from the fact that wafers rejected at in-process inspection can be cleaned off and reprocessed through spin and the succeeding processes. Rejection of wafers can be due to misalignment of a mask to the pattern on the wafer, high number of defects (mars in the photoresist), wrong mask used, and the like.

In all of our calculations for the manufacturing model, we have assumed a nominal rework percentage of 7 percent. Although companies try to run at less than 5 percent, 7 percent appears more representative, with some companies running as high as 10 to 20 percent. Since the definition of an in-process reject varies significantly from company to company, comparing percentages arbitrarily may not be meaningful. Our concern here, however, is the effect

of rework rates on productivity.

Looking again at our five-mask process, a 20 percent rework rate on every layer would mean that the process would look like a six-mask process, with the attendant decrease in productivity (200 versus 220, or down 9 percent).

Wafer Sort

Wafer sort yield is defined as the total number of good dice divided by the total number of dice tested. It is expressed as a percentage of good dice on a wafer or in terms of number of good dice per wafer or both. For complex, large die parts such as the 4K RAM of our model, this yield is the most important one we have considered thus far—primarily because it is so low. Compared with increasing yields by one percentage point out of a yield of 95 to 98 percent, in wafer sort we are talking about a percentage point out of 10 to 20 percent.

An increase in wafer sort yield from the 12 percent to 13 percent would generate an additional 25,000 dice. Alternatively, for the same number of good dice, only 9,230 wafers would have to be produced per month. The 770 fewer wafers would result in a labor and material savings of more than $23,000 per month or $277,000 per year, at a wafer cost of $30. Alternately, these die could mean additional revenues of $100,000 per month.

Assembly

Assembly yields are high in comparison with wafer fab yields, ranging from 85-90 percent, not including final test. The highest loss points usually are die visual, preseal visual, and, for nonplastic packages, fine and gross leak.

Die visual yields are affected by three factors:

- Visual defects caused by the wafer fab processes. These defects (narrow metal lines, for example) pass wafer sort because they are not catastrophic. However, they are rejected at die visual because they may present potential long term reliability problems.

- Visual defects caused by wafer sort. Scratches and ink splashes are the more common problems.

- Scribe and break. A dull diamond needle or a scriber improperly set up may cause the die to break nonuniformly.

In our model, an increase in yield of one percentage point at die visual would generate 3,000 additional good dice and $12,000 additional sales revenue per month.

The losses at preseal visual occur from such failures as loose bonds, broken wires, loose die, and incorrect bonding (wrong pads to wrong pins). These losses are costly at this point, since a package has been committed and is not recoverable. A one percentage point increase at this step would generate 2,700 more die and, ultimately, more than $10,000 additional revenue per month.

Final Test

The final test yield is defined as the total number of good units out of test, divided by the total number of units tested. This yield is affected primarily by the severity of the wafer sort test program and should range from 75 to 85 percent. Less than 75 percent indicates that too much labor and material are being put into bad dice. Yields greater than 85 percent indicate that potentially good dice are probably being thrown out at wafer sort.

3.2 Manufacturing Cost Analysis

Impact of Yields

A very important cost consideration results from the interaction of yield and cost as a unit progresses through manufacturing. Costs are more sensitive to yield at steps toward the end of manufacturing than they are at steps near the beginning.

That is because greater accrued costs can be lost at the final steps. For example, a 90 percent yield at a step near the end of manufacturing would increase the unit cost of the remaining devices by about 11 percent. If this same 90 percent yield occurred instead at a point midway in manufacturing, where accrued unit cost is half the final cost, the cost at that point would also be increased 11 percent; however, the final cost of the unit would be increased by only 5.5 percent.

The result is that it is desirable to push low yield to the front of the manufacturing process. Since a lower yield occurs at the front, there will be a higher yield at the end of manufacturing. It is often cost effective to add steps to accomplish this. For example, an added inspection in wafer fabrication might remove wafers that would fail at wafer sort. This lower fabrication yield would be more than offset by higher yield at wafer sort. By increasing yield losses at the front end of the process large costs are not incurred on defective wafers (or devices) toward the end. Similarly, if a cost incurred at the front of manufacturing will increase yields further on, it may be cost effective to do so.

Photomask Cost

The use of hard surface, chrome or iron oxide, photomasks can dramatically decrease their cost. As compared with five alignments per emulsion mask, a hard surface mask can be used for up to 50 alignments per mask and, in non-contact processing, can last up to 250 or more alignments before having to be discarded. Each mask costs $37, giving a mask cost of $0.74 per alignment at 50 and $0.15 per alignment at 250 ($0.17 per alignment, if the masks are cleaned and reinspected every 50 alignments). In our analysis emulsion masks cost $1.00 per alignment.

Even more substantial savings can be realized with proximity exposures (wafer and mask are separated by 1 mil) and projection exposures (wafer and mask are separated by inches). Although the equipment costs are higher, $27,000 for a proximity aligner and $100,000 for a projection aligner, the mask costs can be substantially reduced. Present proximity aligners, using recleanable hard surface masks, give mask lifetimes of up to 1,000 alignments. This reduces mask costs to $0.06 per alignment, including recleaning after every 50 wafers.

Die Size

As die size increases there will be fewer die per wafer. The impact of die size on the gross number of dice on a 3-inch wafer is shown in Figure 3.2-1.

Additionally, as the die size increases the yield (at wafer sort) will decrease because there is a greater area for a defect to occur per die. This is often expressed by the empirical equation:

$$Y = e^{-ks}$$

where Y is yield, s is the length of one side of the (square) die, and k is a constant. This rule applies only to similar products using the same process and is, therefore, not accurate in comparing dissimilar competitive processes. This relationship is shown in Figure 3.2-1 for variations in die size from the 22,500 square mils (and .12 yield) of our model device.

The number of acceptable die per wafer is

additional weighting given to critical steps. Polysilicon deposition (silicon gate MOS) and epitaxial silicon deposition (bipolar) are rated at 1.5. Field vapox deposition is rated at 2.0. All other steps, including topside glass, are rated at 1.0 for MOS. Bipolar masking and diffusion steps are rated at 0.9 for the following reasons: (1) the masking tolerances required for bipolar TTL are more lenient than those required for MOS, (2) the cleanliness and special handling requirements are less, and (3) bipolar TTL processing is well down the learning curve and is running at higher volumes than MOS, resulting in more efficient use of equipment and labor. All processes represent those used for large scale integration (LSI).

Table 3.2-15

PROCESS COST COMPARISON

Process	N MOS Silicon Gate	P MOS Silicon Gate	P MOS Metal Gate	TTL Bipolar	C MOS Metal Gate
Furnace Steps	5	7	5	10	9
Masking Steps	5	6	5	7	7
Depositions					
Poly/Epi	1	1	–	1	–
Field Vapox	1	1	–	–	–
Top Glass	1	1	1	1	1
Metal	1	1	1	1	1
Total Major Steps	14	17	12	20	18
Total Weighted Value	15.5	18.5	12.0	18.8	18.0
Normalized to N Silicon Gate	1.0	1.194	0.774	1.213	1.161
Projected Wafer Cost	$28.73	$34.30	$22.24	$34.85	$33.36

Source: DATAQUEST, Inc.

3.29 Glossary

Bipolar—Having two carriers of electrical current, one positively charged and one negatively charged. This is in contrast to MOS transistors which only have one charge carrier (unipolar or one polarity).

Boat—Quartz wafer holder, 3 inches wide and up to 24 inches long for use in furnace processes. Parallel slots are cut in the quartz so that wafers can sit vertically in the boat.

CAD—Short for Computer Aided Design. In its most common form, a computer memory is filled with a theoretical model of the MOS transistor and the pertinent process and device parameters. The circuit designer can then use the computer to simulate the performance of sections of the circuit he is designing, so that he can optimize the design without building a hardware prototype first. It can also refer to computer aided layout design.

Fabrication Yield—Cumulative wafer fabrication yield—defined as the number of wafers out of the process divided by the number into the process times 100.

Cumulative Yield (Cum. Yield)—The product or multiplication of yields at every manufacturing step. For example, two manufacturing steps with 80 percent (.8) yield would have a cum. yield of 64 percent (.64).

Desiccators—Plexiglass storage boxes purged with a clean dry gas, such as nitrogen. Used to store work-in-process wafers to minimize contamination.

DI Water—Deionized water. High purity water in which all impurities having an electrical charge (ions) associated with them have been removed.

Die (plural,dice)—Individual integrated circuits (or transistors) separated from the original whole silicon wafer but not yet assembled in a package. They vary in size from 20 mils on a side to larger than 250 mils on a side. The number of dice on a 3 inch wafer may vary from tens to thousands.

DIP—Acronym for Dual-In-Line Package; usually referring to a package configuration in which the external pins are aligned in two parallel rows.

Dopant—Atoms such as phosphorus, boron, or arsenic which are diffused into silicon to create resistors, diodes, and transistors.

Fab—Short for wafer fabrication.

FET—Acronym for field effect transistor. The FET is a transistor whose electrical characteristics are varied by the modulation of an applied electric field across its controlling electrode.

I.C. (IC)—Short for Integrated Circuit.

Junction—The boundary formed by the diffusion of a dopant which produces an excess of negative (positive) charges into an area of silicon having a dopant producing an excess of positive (negative) charges. At this boundary, the two dopant concentrations are equal.

Jungle—The gas control units used to regulate the flow and mixture of gases into furnace tubes.

Laminar Flow—Refers to the "clear air" systems (such as laminar flow hoods or benches) in which the filtered air has a streamlined flow, as opposed to turbulent flow.

Masks, Hard Surface—Photomasks whose patterns are made of chrome or iron oxide, both of which are tougher or harder than the standard

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emulsion patterns. These masks are more scratch resistant and last longer, but are more costly.

Micron—One-millionth of a meter, or about forty-millionths of an inch (0.000040 inches).

Mil—One-thousandth of an inch (0.001 inches) or about 25.4 microns.

M.O.S. (MOS)—Acronym for metal-oxide-semiconductor. In present applications, the semiconductor is silicon. The MOS structure forms the controlling electrode of this type of transistor and consists of a sandwich of metal, oxide, and silicon.

MOS Transistor—A device having an MOS controlling electrode, with a total of three electrodes, typically: Source (source of electrical carriers); drain (collects the carriers emitted by the source); and gate (controls or "gates" the amount of carriers flowing from the source to the drain).

N-channel MOS—A device in which carriers of electrical current and the path (channel) in which they flow are negatively charged.

PC—Short for Production Control. This group schedules the flow of raw materials, work-in-process, and finished goods.

P-channel MOS—A device in which carriers of electrical current and the path (channel) in which they flow are positively charged.

Photomasks—2 1/2 x 2 1/2 to 4 x 4 glass plates, 60 mils thick, upon which are repeated patterns of a circuit layer or die. The patterns are of emulsion, chrome, or iron oxide.

Photoresist (resist)—An organic, viscous liquid which polymerizes (hardens) when exposed to ultraviolet light. A thin film is applied to the wafer surface and the images on a photomask are reproduced in the resist.

Probes—Electrically conductive wires, resembling a straight pin in shape, which are used to contact the electrode pad on circuit die during wafer sort.

QA—Short for quality assurance. In a semiconductor operation, the QA group ensures that the product being produced meets the written specifications and guarantees.

QC—Short for quality control. This group is responsible for monitoring the quality of the product at each of the manufacturing steps.

RAM—Acronym for random access memory. A memory circuit which is organized such that any information location is accessible, without disturbing the information contained in any of the other memory locations.

Run—A batch of wafers, numbering from 5 to 50, which are processed through each process step together.

Silicon Gate MOS—MOS transistors which have a controlling electrode (gate) consisting of silicon instead of metal over the oxide.

Susceptor—Graphite or carbon carrier, as large as 10" x 30", sometimes coated with a layer of silicon carbide, used to hold wafers for poly deposition. Wafers lie flat on this carrier, and energy from radio frequency waves heat up the carrier and wafers.

Vapox—Short for vapor deposited oxides, oxides that are deposited onto wafers by the decomposition of reactive gases (vapors) at low temperatures.

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VLF—Vertical Laminar Flow. Refers to hoods in which the filtered air flows downward to the work surface, in a laminar manner.

Wafers—Circular slices of silicon, 2 inches or 3 inches in diameter and 11 to 20 mils thick, used in the fabrication of integrated circuits.

3.3 Plant Management and Productivity

ORGANIZATION

Organizational structures for manufacturing operations vary from company to company and are often a function of the company's size. Larger companies and rapidly growing companies organize functionally to minimize duplication of people and equipment. As an example, most companies prefer to have a central assembly and packaging department to take advantage of the lower cost derived from higher volumes.

Tested wafers are shipped to this central assembly facility from the wafer sort areas. The good dice are assembled in the United States or sent to Mexican or Asian assembly facilities or both. After assembly, they are shipped back to the specific product groups for final test and shipment. With this type of organization, the assembly responsibilities of the operations manager are reduced to that of production control and some amount of assembly engineering aimed at resolving problems unique to his particular product or product line.

As is illustrated in Figures 3.3-1 and 3.3-2, wafer sort may or may not be a part of wafer fab. Many companies prefer to integrate the two, since the function of wafer fab is really to make good dice.

The product and process engineering approach is mixed. Some companies prefer to integrate process engineering with wafer fab to minimize the "we, they" effect. With this integration, the operations manager has the resources to define and resolve the problems. The difficulty with this approach is usually to find an operations manager who has the ability to understand both the nuances of manufacturing and the technical aspects of engineering.

Product engineering often reports directly to the operations manager, since the engineers must cover both wafer sort and final test, and, as we previously discussed, these latter two activities are intimately related,.

YIELDS

The single most important item in controlling costs and improving productivity and operational efficiency is yield. An efficient manufacturing facility not only has high yields, but those yields are consistent, competitive, and used effectively to make plant management decisions. Yields show up most importantly in wafer fab chute yield, wafer sort yield, and final test yield. However, these yields only reflect the cumulative results of a large number of previous production steps. Yields reflect the interplay of many factors. All of these factors—shown below—are important and all should be watched closely to maintain yields.

- Cleanliness
- Precision in processing
- The process
- Device design
- Operator discipline and attitudes
- Production control and information feedback
- Yield interrelationships

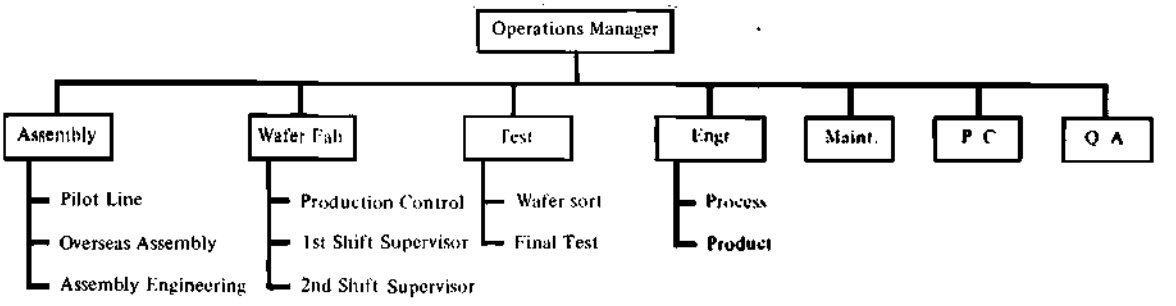
The need for cleanliness and its effect on yields is well known. Purity in gases and water, the presence of sodium, particles of dust in the air, and clean handling procedures are all very important. Uncleanliness not only can drastically cut yields but also can affect the reliability of the product. The latter may only be discovered after the final product is finished. On LSI devices one small particle can cause the entire device to be a reject.

With hundreds of separate processing steps, process variations can become cumulative. Precision and control at each step are extremely important in producing a device which operates properly. The precision required throughout a semiconductor facility is difficult to imagine for those not familiar with semiconductors. As a result, at most operating steps in manufacturing a semiconductor—especially an LSI device—state-of-the-art precision is re-

3.3 Plant Management and Productivity

Figure 3.3-1

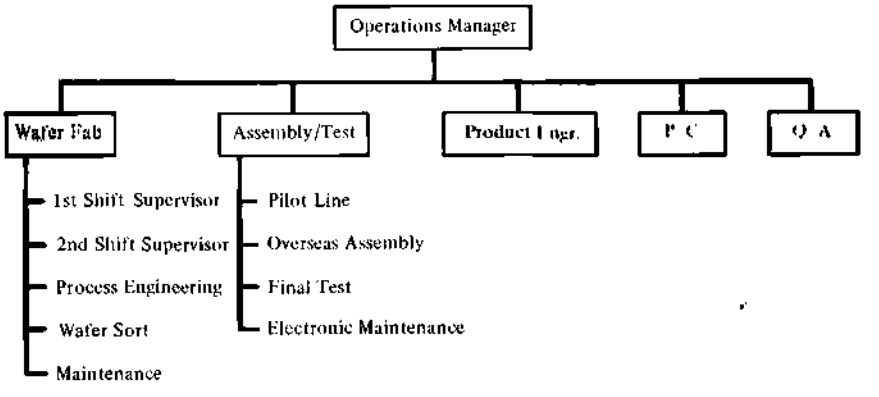
FUNCTIONAL ORGANIZATION CHART



Source: DATAQUEST, Inc.

Figure 3.3-2

TASK ORIENTED ORGANIZATION CHART



Source: DATAQUEST, Inc.

quired to be competitive. That is one important reason why equipment becomes obsolete so rapidly. Lack of precision shows up immediately with variations in the important control parameters on a device, and these variations can often have an enormous affect on yield.

The particular process used and its complexity can have an important effect on yield. The process is also extremely important in affecting the reliability of the device. The design of a process that is simple, workable, and reliable is difficult, and at this time nearly all N-channel silicon gate processes are a compromise. No clear consensus process has arisen.

Integrated circuits must be designed so that the design parameters do not tax the capability of wafer fabrication. If either the process or design has been poorly engineered, greater processing precision will be required. Lack of communication between design engineers, processing engineers, and test personnel during the formative stages of a product can have drastic consequences.

Because of the large number of processing steps in manufacturing a device, the performance at any one step must be almost perfect. Such a state requires disciplined operators with excellent work attitudes. If operators become lax, the cumulative decline in yields over the many different steps can have frightening effects. For example, if errors increase from 1 in 200 to 2 in 200 per step over 20 steps, cumulative yield will drop from 0.91 to 0.82. If a lead bond operator makes an error of one in even 100 bonds, then one-third of the devices will be defective (32 bonds for a 16 pin package).

Controlling yields is a difficult and frustrating process. To be effective requires good production control, a well developed system of information feedback among the different steps in manufacturing, a large number of check and test points in the process, and a high degree of communication and cooperation among all areas of manufacturing and engineering. It is necessary not only to measure yields, but also to pinpoint what is causing yield problems. However, since factors affecting yields result from a combination of diverse situations, teamwork among the manufacturing and support areas is a necessity.

A yield at any given point in manufacturing can be highly interrelated with the yield at another point. For example, there is high degree of inverse correlation between yields at wafer sort and final test. Very often the decision to improve yields at one point may affect the yields adversely at another point. Even though the total cumulative yield will improve, changes such as these can have an important affect on costs. If the cost of a die is extremely high, it may be cost effective to be less particular at die sort. However, if die cost is low, as in small scale integration ICs, then assembly costs should not be incurred on a device that may prove defective, because assembly costs and assembly yields largely determine the final cost of the device. Interrelationships also occur throughout the wafer fabrication area.

DISCIPLINE

The manfacturing of a 4K RAM requires a high degree of precision, extremely complex processing, and a high degree of general awareness on the part of management and engineering on just exactly what is going on at any point in time. Discipline and control in a manufacturing facility is absolutely necessary if the company is to be successful. No matter what amount of investment, talent, or effort there has been, a lax operation will not succeed.

Discipline is most important at the operator level. It requires an operator to be able to perform a complex processing step hundreds of times without error. The operator must also be aware of problems that may have developed at some other step in the process and must alert engineering or production control.

3.3 Plant Management and Productivity

With respect to control, one of the most fruitful effects is the feedback of information. Specific information on yields must be collected at final test, wafer sort, and elsewhere and placed in the hands of the engineering support group. These groups in turn must use that information to spot or monitor potential problems and to correct such problems before they arise.

Since yields cannot be perfect, the operations manager must be extremely careful in the use of his resources—both labor and capital. Thus, he must have a knowledge not only of yields but also of the effect that engineering attention, more operators, or a new piece of equipment might have on those yields. Then he must decide how to use his limited resources most effectively for the good of the facility. This decision is often extremely difficult, especially when the various manufacturing areas and support groups may be more concerned with showing their area in the best light regardless of the benefits to the total facility.

The interrelationships mentioned above make it clear that cooperation is extremely important in a smoothly running facility. Even those familar with semiconductor manufacturing have difficulty grasping the entire process and its interrelationships, and it is always difficult to be objective. For example, suggestions that a device design might be hurting yield can be particularly galling to a design engineer, who might feel that the problem lies in processing. Nevertheless, device design can very often put an unfair burden on processing capability. Thus, cooperation between the two areas is essential.

AUTOMATION

Automation has always been a subject of controversy in the semiconductor industry and for good reason: it has both strong advantages and strong disadvantages. In perspective, the semiconductor industry is not very automated. In spite of high capital costs, the industry is still very highly labor-intensive. Labor costs are at least ten time the cost of depreciation and rent. For this reason, it would seem that more automation is natural and, indeed, the industry may automate slowly. However, because several factors work against automation, the degree of automation in any facility must be a considered decision.

Automation always holds the potential of higher product throughput, lower labor costs, and higher labor productivity. It has the possibility of lowering costs that result in improvements in manufacturing control beyond human capabilities. However, the decision to use a more automated piece of equipment can entail some serious problems:

- High equipment costs
- Possible lower yield
- Trained labor requirements
- Short equipment lifetime

Because of the complexity of semiconductor processing and the precision required, automated equipment can be very expensive. The added expense is an additional burden on an industry that is not, in general, well financed.

The major problem with automated equipment is that the yields possible with this equipment can be lower than with less automated equipment due to factors such as precision, possible device damage, and cleanliness. For this reason, the very labor-intensive bonding steps in assembly have never been automated for LSI devices. Because of the high cost of the chips, a small drop in yield at these steps can be very costly. In the masking area of wafer fabrication, the alignment of the masks has never been automated because human alignment has proved slightly superior in this extremely critical step.

Equipment lifetime, in general, is very short in the semiconductor industry because of the continual need for state-of-the-art precision

to be competitve. As a result, semiconductor manufacturers have often been burdened with automated equipment that has been bypassed by the rapid changes in technology. Consequently, they have hesitated to automate their production line more fully.

PRODUCTIVITY CONSIDERATIONS

Semiconductor processing equipment tends to become obsolete relatively quickly and, as a result, is typically written off over a period of five to seven years. Rapid obsolescence occurs for two reasons. The IC industry is relatively young (15 years) and is still experiencing a period of rapid technological change. New process technologies, such as MOS, have required the evolution of increasingly sophisticated process equipment, with solid state controls and previously unheard-of needs for accuracy, precision, and cleanliness. New products, such as the complex 4K RAM, require computer-type testers with the ability to exercise every permutation and combination of inputs.

In addition, the semiconductor industry has been dedicated to following "the learning curve". As unit volumes have increased, IC prices have continued to fall at a rate of 20 to 35 percent per annum in spite of inflation. Part of the reduction in cost has come through the upgrading of manufacturing equipment. Wafer sizes have increased from 1 to 2 inches and from 2 to 3 inches, with each step requiring a new round of capital equipment. Hand-made electrical test set-ups, which were acceptable for small volumes, have been replaced by fully automatic testers and automatic package handlers. Metal packages which were once individually sealed by hand are now replaced by injected molded high purity plastics.

The equipment listed for the manufacturing model is up-to-date and, barring significant equipment advancements, should be viable through at least 1978.

The Compressed Work Week

One approach to maximize the use of equipment is to use it 24 hours a day, seven days a week, 365 days a year. While we know of no company pushing that hard, there are companies who fully utilize their equipment six days a week, 24 hours a day in periods of high demand. To do so, these companies have gone from the standard 40 hour work week to the compressed work week (CWW).

The CWW consists of four teams of people: foremen, technicians, operators, and, sometimes, engineers. Each team works three days a week, 12 hours a day. The seventh day (6 p.m. Saturday to 6 p.m. Sunday) is used primarily for engineering work and maintenance of equipment. This approach allows every piece of equipment to be manned and operating 144 hours a week, with no overtime. Time is also saved because one less shift is needed.

Although the data are still sparse, the companies report no increase in absenteeism, tardiness, or turnover. In some cases, they claim the numbers are better than that of the standard work week, particularly if a substantial amount of overtime is required for the latter approach.

While this approach makes excellent use of capital resources, the negatives aspects are many:

- Generally, more operators, foremen, and technicians are needed, particularly at lower volumes, to man the four shifts.
- Communications between shifts can become a problem. For example, a unique process problem that is resolved on Shift One at 3 p.m. (Wednesday) may never be explained to the foreman who handles Shift Two, which ended Wednesday morning at 6 a.m. These two foremen will not see each other again until 6 a.m. Monday morning of the following week.
- Cross-training of operators is a necessity, so

that they can do some job rotation during the day to minimize boredom and fatigue.
- One operator absent for a day means a 33-1/3 percent loss of her weekly contribution.
- Generally higher hourly wages.

In lieu of a compressed work week, standard two shift or three shift operation is very common.

Maintenance

Most companies have found that an effective maintenance team is cost effective in the long run when downtime costs are considered. Maintenance is the most often neglected activity and usually occurs only as "reactive" maintenance—i.e., equipment is worked on only when it is giving trouble. The biggest problem is that maintenance personnel usually do not have access to production equipment to accomplish preventive maintenance, because the equipment is always in use.

A second problem is that equipment downtime is typically longer now because of the complexity of the machines and the extent to which solid state components, including ICs, are used. The self-taught mechanic, who was the expert on past machines, often finds it impossible to pinpoint rapidly the failure of an IC. On the other hand, the electronics technician, very few of whom want to be mechanics, are "all thumbs" when it comes to fixing the mechanical problems.

Back-up Equipment

It is not uncommon for some equipment, particularly in wafer fab, to be down for four hours or even an entire shift. Since the fab processes are sequential, the failure of one key piece of equipment affects succeeding processes and can enormously affect productivity. For this reason, it is often wise to have "back-up" equipment. As an example, one coater is assumed for our manufacturing model. If, however, that machine was found to be subject to an exceptional amount of problems on a continuing basis, it might be desirable to purchase a small machine (2 tracks versus 4 tracks) for back-up. That is because shut down of all 4-tracks of the single coater would also shut down activity of five aligners, two developers, and ultimately, the succeeding diffusion and deposition processes.

Judicious placement of back-up equipment is paramount to the running of a successful manufacturing operation. The extra capacity allows preventive maintenance to be more consistently performed and allows manufacturing to continue to operate, although at a slower rate, when the primary equipment fails.

Wafer Fabrication

Wafer fabrication productivity is an important measure of the efficiency of an LSI facility. Although productivity can vary, there are two good measures of an efficient operation:
- 180 to 220 wafers out per operator per month.
- 1.25 to 3.0 wafers out per square foot of fabrication area.

The number of wafers out per month, of course, depends on both the general productivity of the operation and the yield in wafer fabrication. If the wafers out per month can be estimated and the number of operators in wafer fabrication can be estimated, then a good measure of the facility's efficiency can be calculated. It should be noted that "wafers out" refers to good wafers on which a reasonable wafer sort yield can be obtained. A poorly managed operation, on the other hand, may produce carloads of wafers, but if the process is not well controlled the wafers may yield only a negligible amount of good devices.

If the size of the facility is known and the number of wafers out can be estimated, then

3.3 Plant Management and Productivity

productivity can be calculated. The values noted above (1.25 to 3.0) apply for a standard three-shift work week. If two shifts or one shift are used, the measure of good productivity must be adjusted correspondingly. Similarly, if a compressed work week is used, the measure of productivity must be adjusted upward by about one-third.

Of the three major fabrication areas, masking is the most labor-intensive. Consequently, the bulk of our remarks on productivity relate to the effects of masking. The key forces impacting fabrication productivity are:

- Complexity of the process
- Operator turnover
- Scheduling
- Yields
- Degree of automation

Complexity of the Process

In any manufacturing operation, process complexity is an important factor contributing to productivity, particularly for MOS wafer fabrication. The simpler the process the better. The N-channel silicon gate process described in our manufacturing model has only five masking steps. Each additional mask layer, at the 10,000 wafer output per month rate, would require an additional 13,300 alignments per month. If the process had nine masks (and some do) an extra 53,000 alignments per month would be needed. This translates into the need for four additional alignment jigs and eight additional operators. When the additional in-process and final inspection operators are added (ten more operators and five additional microscopes), productivity drops further. Up to five more operators would also be needed for deposition and diffusion. A summary of the impact of the number of masks is shown below, assuming 10,000 wafers out per month and two shifts:

Number of Masks	Extra Operators Required	Productivity (wafers per operator per month)
5	0	220
6	5	200
7	10	181
8	16	164
9	21	152

Using a productivity level of 220 wafers per operator for five masks, the right-hand column in the tabulation summarizes the effective productivities as additional masks are added. The nine-mask process results in an output per operator that is 31 percent less (152 versus 220) than the five-mask process. In short, labor costs (and mask costs) rise rapidly as the number of masking operations increases.

It is apparent that to maximize the use of operators, a manufacturing process should be designed that minimizes the number of masking steps. This, in turn, will minimize the capital equipment and space needs as well.

Operator Training and Turnover

Turnover rates are generally high in the mobile semiconductor industry. Although it varies with location, 1 to 2 percent per week turnover is not unusual. The consequences of turnover are most serious in the masking operations, particularly at align. It usually takes an inexperienced person approximately five weeks to reach 450 alignments per shift, with a reject rate of less than 5 percent. In our model, the operator could probably reach 450 within four weeks because she would only have to align one mask set for the 4K RAM.

During the five-week time frame, the new align operator would average 235 aligns per shift or about half of the standard productivity rate. From an output standpoint, it takes two new inexperienced operators to perform the work of one seasoned operator. There would

also be a need for additional equipment and space.

All other operators in the three fabrication activities can be trained relatively quickly (two to three weeks). However, the experience of most manufacturers is that the newer operators make the most mistakes and that these mistakes lower yields and productivity. Minimizing operator turnover and improving training, particularly at align, must be a constant concern to fab managers.

Scheduling

Since the MOS fabrication processes are sequential, it is essential to keep the work-in-process (WIP) inventories properly distributed—i.e., keep the production line "balanced." In spite of backup equipment, most fabrication areas do not have the capability for making up much lost ground. The shutdown of one station can cause others to shut down. An interactive, responsive Production Control group is essential to a good fabrication operation. It must schedule the work to make the most effective use of people and equipment.

Equipment For Increased Productivity

The diffusion and deposition processes have, to a great extent, been automated. But cleaning, dipping, loading, and unloading batches of wafers still tend to be labor-intensive. These are being simplified, however, by the use of "cassettes", which look much like the old 35 mm rectangular slide trays. These carriers allow "flip transfer" of wafers—simply by placing an empty carrier upside-down on the top of a full one and flipping the combination. This approach eliminates the tedious, time-consuming effort that many companies still use: moving each wafer individually from one carrier to the next with a pair of tweezers.

A fully automatic mask aligner would be a boon to the semiconductor industry. Alignments per operation could at least double if a machine assumed the tedious role of aligning the pattern on the mask to that on the wafer. Training time for new operators would be reduced to less than a week. Reworks for misalignments would be nil. Unfortunately, however, none of the automatic aligners on the market has proven its worth (or expense). Electrical and mechanical problems are numerous, and increased productivity has yet to be realized.

Assembly

The measures of productivity within the assembly area are difficult to define. A rule of thumb for our 16-pin, plastic packaged 4K RAM would be: Units out of assembly (not including final test) should average at least 5,000 per operator per month. Our model runs at 5,700 per operator per month.

Of the three major components of our manufacturing model, assembly is the most difficult in which to increase productivity. In spite of a number of automated systems that have been tried, none has been successful enough to gain general acceptance and the basic approach to assembly has changed very little over the past five years. The most significant change has been the conversion of many products to injection molded plastic (silicon or epoxy) packages, where frames holding ten units at a time can be assembled and cut apart after molding. Plastic packages have been successful because the material costs are significantly lower than those for ceramic packages. All other innovative assembly techniques have served to reduce some of the labor content, but have not lowered the cost of the finished unit significantly. In some examples, the labor content decreased in assembly, but the labor and

materials cost rose in wafer fabrication.

In some respects, the ready availability of low cost Mexican and Asian assembly labor five to ten years ago has hindered the development of lower cost packaging. Assembly can still be performed in some countries for as little as $0.10 per hour. However, this is changing and overseas assembly costs are on the rise. Labor costs are increasing (pay raises of 30 to 300 percent were granted in some countries during 1974) and inflation is rapidly forcing up the cost of packaging materials.

Consequently, the present emphasis in assembly is being placed on plastic packages, low cost hermetic packages (Cerdip), higher speed bonders, and the elimination of some 100 percent yield process steps. In the last case, a close look is being taken at process steps in which the yield is consistently 100 percent and in which 100 percent of all units are tested. Examples would be temperature cycle and centrifuge. In place of the 100 percent test, the companies could implement a statistically based sample plan.

Although the new high speed bonders are running at 100 16-lead units per hour (optimally), bonding is still the slowest assembly step. Productivity in the assembly area could be significantly improved if bonding rates could be increased or an alternative assembly method were developed. Most of the innovative techniques have reduced the labor at lead bond, only to have moved the costs into wafer fab or the packaging materials.

Another area that should be scrutinized are the two key inspection steps which are very labor-intensive. In our model, more than 575,000 dice must be individually inspected every month at die and preseal visuals. For the larger 4K RAM die, a reasonable inspection rate would be 1,350 per shift for die visual and 3,000 for shift for preseal visual, or a requirement of 16 operators.

Test

The RAM testers on the market today are basically computers. They have a tremendous amount of sophisticated integrated circuitry, compounded with the need to interface with electromechanical probers and handlers. Because of the complexity of the test system, subtle problems frequently arise that are difficult to track down and resolve. Testers of this complexity are frequently down for hours at a time, and tester downtime is a serious problem. Most manufacturers have a team of electronic maintenance personnel, some with engineering degrees, specializing in troubleshooting on testers. In choosing a test system maintenance many times will override the other productivity considerations.

Wafer Sort

The RAM testers currently available on the market have the capability of running two or four wafer probe machines. Test time per wafer for these machines depends on the complexity of the test program (which depends on the complexity of the product) and the number of dice on each wafer. A wafer with small—40 mil x 40 mil die—may take 30 minutes to test, while a wafer with our 150 mil x 150 mil, 4K RAM with almost 14 times fewer dice may take as little as five minutes, including set-up time.

Productivity can be improved in two ways. An operator can run two probers at a time, rather than operating only one. If the probers are likely to wander, i.e., the probes move off alignment with the pads on the die, it is preferable to have an operator at each station. Moreover, the test program can be written to test the most likely failure mode first and immediately go on to the next die when the first failure is found on a die. This "first fail" approach is fast

Full Test of 10 ?

but sacrifices information that may be achieved by identifying all test failures on the rejected die.

Final Test

Productivity at final test can be most dramatically improved by going to "single insertion" or "single pass" testing. In "single pass" testing, the packaged unit needs to be inserted only once into a test socket. This is contrasted with multiple-pass testing in which the unit is put in one socket for part of the testing and then pulled out and put into other sockets for additional testing. An example would be to test the functionality of the unit first and then to put it into another holder to perform tests at the temperature extremes or dynamic tests. However, single pass testing is often hard to implement because of the complexity in required testing equipment and adequate assurance that the device is being tested to specifications.

A second approach of great impact is the use of automatic package handlers. These handlers take a tube of serially stacked dual-in-line packages and automatically feed a unit at a time into the test head. The output of the machine may be delivered to a number of tubes, each one representing a different performance level part. This type of testing can even be performed at the higher operating temperature limit, and parts can be sorted out to different temperature ranges. Use of these automatic handlers can increase the output per station by more than 30 percent.

3.4 Plant Construction

Integrated circuit and, in particular, MOS integrated circuit manufacturing facilities require a great deal of attention in construction because of the need for extreme cleanliness.

The following sections describe a floor plan of the completed plant, the special needs of the MOS facility, and the timing typical for the construction and start-up of such a facility.

FLOOR PLAN

The floor plan of a typical N-channel silicon gate MOS wafer fabrication facility is shown in Figure 3.4-1. This layout is for illustrative purposes only, the objective being to show the typical location of specific equipment and processes, relative floorspace, and other considerations.

There are four areas that define the important components of wafer fabrication: diffusion, deposition, and align and etch (masking). All furnaces and their associated acid sinks, which are used for cleaning wafers before a furnace operation, are located in the diffusion area.

Because of the similarity in requirements for air conditioning, electrical power, and utilities, the deposition processes are located in the same area as the furnaces. The RF generators are placed in their own rooms as a precautionary measure. Align and etch (which constitute the masking area processes) are located in separate rooms because of their different environmental requirements.

Spaces have been reserved (as outlined by dotted lines) for future expansion of capacity. However, it is likely that much of this space would be filled immediately for either back-up equipment or because the N-channel MOS process used by a company may be more complex than the one described in our manufacturing model.

The total area required for manufacturing operations is summarized in Table 3.4-1.

WORK FLOW

The general work flow in a plant was shown in Figure 3.1-1. In wafer fabrication, the flow of product is from diffusion and deposition to masking and vice versa. Because five masks are used each wafer would travel through masking five times.

After the last step in wafer fabrication—wafer evaluation—the wafers are transferred to wafer sort where they are tested in wafer form. The tested wafers are then moved into assembly, where the individual circuits are packaged. We have assumed that assembly is performed in this same plant, although it is more likely that the assembly operations would be performed in a low cost, offshore plant. From assembly, the packaged circuits are transferred into final test, where each unit is tested by a specific electrical test criterion. The good units are moved into Pack and subsequently shipped out to the customer.

SPECIAL FACILITY REQUIREMENTS

Integrated circuit and, in particular, MOS integrated circuit manufacturing facilities require a great deal of attention in constuction because of their need for extreme cleanliness.

The following section describes some of the special requirements of a MOS facility, including deionized (DI) water, gases (nitrogen, oxygen, and hydrogen), clean rooms, air conditioning, and power.

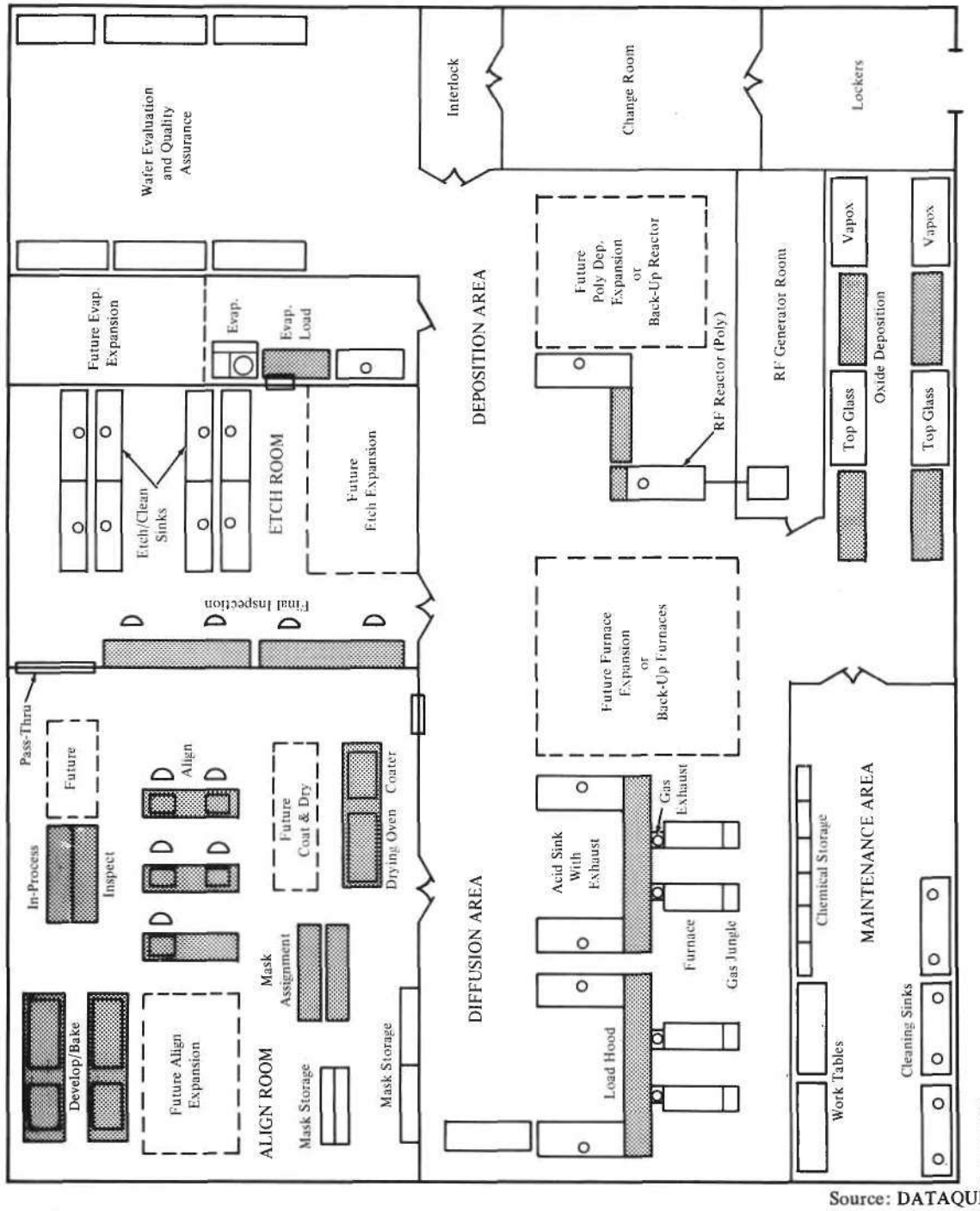
Deionized Water

Water for all integrated circuit facilities is highly purified. It is purified by passing standard tap water into a series of "refining" steps which sequentially remove the minerals, microorganic sludge (via charcoal filters), bacteria, particulates, and ions (particles having an electrical charge).

3.4 Plant Construction

Figure 3.4-1

TYPICAL MANUFACTURING FLOOR PLAN



Source: DATAQUEST, Inc.

3.4 Plant Construction

Table 3.4-1
MANUFACTURING AREA REQUIREMENTS

Manufacturing Area	Space Required (square feet)
Wafer Fabrication	
Masking	3,000
Diffusion	3,000
Deposition	2,500
Support	1,500
Subtotal	10,000
Test	
Wafer Sort	1,500
Final Test	1,200
Subtotal	2,700
Assembly	10,000
Total	22,700

Source: DATAQUEST, Inc.

Since MOS circuits have large areas of thin glass (oxide) which is formed as an integral part of the device structure, particulates can be a serious problem. Each particle can cause a potential failure site in the thin oxides, so the minimization of particle concentration is extremely important. If the water is less than pure, there is a possibility that the MOS products will be contaminated when immersed in it. On the other hand, if it is that pure and the container into which it flows is clean, the water forms an excellent final cleaning and rinsing solution. In fact, if wafers are accidentally contaminated on the surface with ions of sodium, which in quantities as low as two parts per billion can cause MOS devices to be unstable, the clean DI water can be used to leach out the sodium.

DI water is measured in terms of numbers of particles per volume of water and resistivity, an electrical measure of resistance to electrical current flow (the higher the resistivity, the fewer the ionic species). Many bipolar integrated circuit facilities run successfully with more than 200 particles per 100 milliliters of water and one million ohms of resistance. MOS facilities, on the other hand, require fewer than 100 particles per 100 milliliters and greater than 15 million ohms of resistance.

Clean Rooms

Because of the vulnerability of MOS circuits to failures caused by particulates, it is necessary to build clean areas or "clean rooms" for the critical processing steps.

These rooms have solid ceilings, as opposed to "drop" and "hung" ceilings; solid walls versus moveable walls; sealed floors; filtered air input through the air conditioning system; positive air pressure with respect to the access corridors; sealed light fixtures; no ledges, cracks, or open utility holes; change rooms, in which operators don clean room clothing; and double-access doors to each specific area.

Some facilities even go to the extent of having entire ceilings or walls of filtered, "laminar-flow" air (filtered to less than 100 particles/cubic foot, of sizes less than 0.5 micron) flushing through the room. Where laminar-flow ceilings are used, the floor below is commonly ventilated and the air is exhausted through it. However, laminar-flow walls and ceilings are often more expensive than effective. Real improvement in air purity and laminar-flow is often difficult for large areas, and other sources of contamination can thwart the intended air improvement. Personnel movement or opening of doors defy good design.

The majority of the quality MOS houses have built in the characteristics summarized in the second paragraph and then installed laminar-flow clean benches (table with a blower and filter directly over it) at each of the process stations. Work in process is then transferred from one station to another via pass-throughs

or in covered containers. With this approach, the wafers are uncovered only under these clean hoods and the hoods, in turn, also help to continually cleanse the room air through their filters.

To maintain the effectiveness of the clean rooms, manufacturing must institute strict discipline among their personnel with regard to clean room techniques. Clean room personnel clothing never leaves the clean room change area; purses, pencils, noncoated paper, and excessive facial powder are taboo; clean room clothing is changed regularly, as often as every other day. This type of discipline or the lack of it will makes or breaks a clean room facility, regardless of its appearance or its construction expense.

Temperature Humidity Control

Control of temperature and humidity is very important for process control, as well as operator comfort. The diffusion processes generate enormous amounts of heat because of their high operating temperatures (450 degrees centigrade to 1,275 degrees centigrade or 824 degrees Fahrenheit to 2,325 degrees Fahrenheit). Moreover, the potentially toxic gas output of each furnace and its associated acid sink must be exhausted to the outside. Consequently, a tremendous load is placed on the air conditioning system and, for that reason, the diffusion equipment is isolated in a separate room with its own exhaust and air conditioning systems.

The photomasking room must typically be controlled to within plus or minus 2 degrees Fahrenheit and less than 40 percent relative humidity, because of the sensitivity of the photosensitive film (photoresist) to temperature and moisture. Further, most photoresists are sensitive to ozone (found in smog) so that the air into the area must be filtered through activated charcoal filters.

Many facilities separate the first half of their photomasking processes from the last half, because first half (mask align) requires the tight humidity and temperature control, but the second half (etch) does not. The etch area also requires a large amount of air exhausting for its acid sinks. This could place great demands on the dehumidifiers used to control relative humidity levels needed for align. The splitting of the photomasking area saves money and energy.

Temperatures and humidity control are also important for most testing areas. A wide temperature variation can cause marginal devices to pass testing and good devices to be rejected.

Gases

The gases used in MOS processing must be extremely pure, and great precautions are taken to ensure purity. Oxygen, nitrogen, and hydrogen are used throughout the manufacturing plant. Prior to entering the manufacturing area the gases are forced through very fine filters, which have pore sizes of less than 0.2 microns, to ensure that no particles accidentally contaminate the gases as they pass down the pipes.

All piping is either of stainless steel or of vacuum baked high purity copper, to minimize any possible contributions from the pipes themselves. All solders and fluxes used to join pipes are also of high purity, without such contaminants as phosphorus or boron. Finally, a continuous flow of inert gas (nitrogen) is passed through the pipes during the soldering and welding operations to carry away any potential contaminants.

Electrical Power

Semiconductor manufacturing facilities use a great deal of electrical power. Large amounts of power are required for the diffusion furnaces,

the RF generators, much of the support equipment such as air conditioners, and many other pieces of manufacturing equipment.

In addition to the total power requirements, the semiconductor facility has two other special needs. One need is for very high quality electrical power that is free from noise or wide voltage variations. Second, a high quality ground is required for the electrical test equipment. In general, manufacturers have found it fruitful to separate power lines for testing equipment from power lines to other equipment. In particular, equipment that turns on and off by means of switches or relays can be especially troublesome in causing transient surges that result in unreliable testing by the test equipment.

TIME REQUIREMENTS

Because of the special facility needs required for the semiconductor industry, it is usually more effective in the long run to construct a facility rather than to try to adapt an existing building. Prior to construction, particular attention must be given to the design of the facility so that all special requirements are met. Attention must also be given to the time required to install support equipment, plumbing, air conditioners, and other hardware before the facility can be used. Some equipment will also require time to be ordered, manufactured, or shipped and installed—such as large equipment used for gas storage and producing deionized water.

Construction and Equipment Check-Out

The time required to construct, debug, and build-up an N-channel silicon gate MOS facility ranges from nine months to a year. Construction is affected by such factors as strikes, material shortages, late deliveries, and adverse weather.

The time required to debug equipment and processes can vary among companies. Most companies choose to install the latest and best manufacturing equipment in any new facility, for two reasons: (1) the equipment becomes obsolete so rapidly that it is not always economical to install older models, even though they are well proven machines; (2) Most IC companies buy their equipment from the same vendors and, therefore, all have the same basic manufacturing capability. The advantage, however slight, supposedly goes to the company getting the newest, best equipment into production first. More often than not, however, the latest models have "bugs" or problems which may take days or even months to resolve.

In the wafer fabrication area, there is a close interaction among processes, process equipment, and yields. New equipment at a process step often forces a redefinition or redevelopment of that process, sometimes causing it to be subtly different from the earlier one. Then the manufacturers find that, while the new equipment is faster, the process has worse yields than the previous one. The subsequent questions raised are: (1) Is it the equipment, the process, or both? (2) Which process stops are involved? Considerable time may be required to answer these questions and find an acceptable solution.

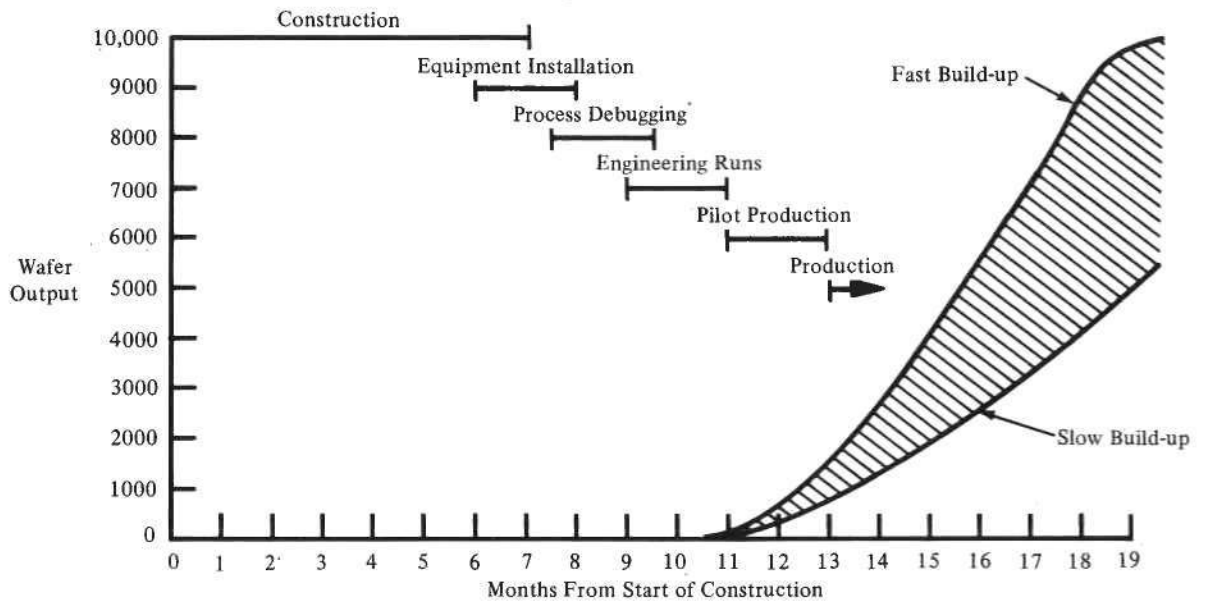
Figure 3.4-2 illustrates the timing for the building of a new MOS manufacturing facility, from construction to volume output. Approximately six months can be saved by moving into an existing adequate facility. The construction time is then limited to the installation of utilities and equipment.

Volume Build Up

If a building is started from scratch, it takes at least nine months (barring any serious disruptions) before the initial engineering runs can be processed through the area. These are wafer batches carefully handled at each process

3.4 Plant Construction

Figure 3.4-2
START UP TIME REQUIREMENTS



Source: DATAQUEST, Inc.

step by highly trained and experienced engineering operators. The objective is to determine whether the equipment and processes are sound and to pinpoint any deficiencies that could arise under ideal processing conditions. When this step is completed, manufacturing operators are brought into the area to begin the processing of larger volumes. The objective of this pilot production step is to determine and correct problems that are volume- and people-sensitive. Volume is increased until the area is able to consistently process around 500 good wafers per week (2,000 per month) without any major problems and at the projected yields.

It should be noted that for a new facility, the slowest area to reach production is almost always the wafer fabrication facility and processes. Test equipment and assembly equipment can usually be debugged and on-line at least four weeks before the wafer fabrication processes are debugged.

Wafer volume build-up is loosely tied to the availability of trained operators. Even experienced operators have to be retrained on new equipment, which lowers their productivity for days or weeks at a time.

During the build-up of volume, output per operator is not necessarily a satisfactory indication of efficiency, since most of the efforts go into the establishment of the work-in-process inventory. Further, operators are hired in advance of the actual growth of volume, for purposes of training and in anticipation of the future need for their services.

3.5 Analyzing an IC Plant

In this section, we have tried to highlight some items that can be beneficial to an observer reviewing an IC operation. The accurate analysis of the performance capabilities of an IC plant is difficult for an observer unfamiliar with the "nitty gritty" details of the technology and products employed. Our objective is to elucidate those factors which will assist in the analysis of a facility to determine its capabilities and competitive position.

PREPARATION

A simple review of any IC manufacturing facility generally consists of a question and answer session and a tour of the manufacturing facility. Preparation is important to reap the maximum benefit.

- Know all you can about the manufacture of semiconductors.
- Know the important details of the product(s) you are interested in: product number, designation, package type, function, process technology, and die size, if possible.
- Know your questions. A long written list of questions will quickly lose the attention of any engineers or manufacturing supervisors and reduce your chances of obtaining accurate information. Memorize the answers—writing them down worries most individuals, because they are usually fearful of divulging proprietary information.
- Know the definitions of the key measures of interest to you. For instance, know the definition of fab yield so that, if necessary, you can define it to the respondent.

EXPERIENCE

Because an integrated circuit manufacturing facility is both complex and highly technological, it is impossible to analyze it effectively without some experience and knowledge of the industry or the manufacturing processes. For this reason, it is necessary to visit a number of different facilities. If some of those facilities are known to be either effective or not effective, it can be helpful in analyzing the data you gather. At any rate, the experience thus obtained will familiarize the observer with what to look for, what is and is not important, and some basic benchmarks to evaluate other facilities. An initial trip through an IC facility can be overpowering, and it is easy for the inexperienced to be misled. Practice will avoid this problem.

COMMENTS ON DATA INTERPRETATION

One of the major problems faced is to ensure that the answers obtained allow an accurate comparison. In discussing yields, for example, there are different ways in which to define fabrication yield, and a high wafer sort yield is meaningless if the final test yield is very low.

A second problem is that the responses you receive may be indicative only of what the respondent wants you to hear—or thinks you want to hear. It is highly probable that someone with a 40 percent fab yield may answer that his yield is running in excess of 70 percent, because that is what he feels a good process would yield. On a tour through the manufacturing areas, do not be surprised to see a large number of batches of your favorite product strategically located for your viewing.

A third problem is you may not be able to obtain any critical data, such as yields, because they are classified as "company proprietary".

Finally, the qualitative data gathered by an observer may be as valuable as the quantitative data. The extent to which the value is recognized depends partially on the experience and knowledge of the observer. We would recommend that some of the most worthwile conclusions may be drawn by comparison of responses within an operation and by a

3.5 Analyzing an IC Plant

company-to-company comparison.

All manufacturing companies tend to show off only their best facility or to give tours through only the prototype or engineering lines. As observer must be careful to make sure that he has seen the main production lines of the product in which he is interested. Not all companies will honor such a request, but it is helpful if you are a stockholder or have some other financial leverage.

QUESTIONS TO ASK

- Wafer fab yields? (70 to 85 percent is good)

- Wafer starts per month?

- Wafer outs per month?

Knowing any two of the above will allow you to calculate the third. This calculation is a bit tricky if the fabrication area is in a rapid build-up mode, since much of the labor of the operators will go into building work-in-process inventory. The wafer outs questions could also be posed to wafer sort personnel, as "How many wafers are tested per month?".

- Wafer sort yield?

To be meaningful, the wafer sort yield must be defined for a specific product. Good die per wafer and percentage good die per wafer are both necessary, because the two pieces of data allow you to calculate back to total potential candidates on a wafer or die size or both. Do not expect a straight answer to this question, however, as wafer sort yields are sensitive numbers and rarely given out.

- Final test yield?

The final test yield should be checked against the wafer sort yield and typically should run in the 70 to 85 percent range. If two vendors are manufacturing the same product, at equivalent die sizes, and one is running 85 percent of final test yields versus the other's 65 percent, a check of wafer sort yields is essential. It is likely that the one with the higher final test yields is running with a lower wafer sort yield. A note of caution, however. In many instances, a very well-designed product, together with a well-controlled process, will result in both excellent wafer sort and final test yields.

- Number of shifts?

- Area of wafer fab (in square feet)?

- Number of operators?

From answers to the above question, a person can calculate wafers out per operator per month and wafers out per month per square feet if the number of wafers out is known. These numbers reflect the productivity considerations. Normal values are 180-220 wafers out per operator per month and 1.25-3.0 wafers out per month per square feet for MOS LSI. Again, be careful in drawing conclusions from these data if the area is in a period of rapid volume build-up.

- Number of photomask steps in process?

- Percentage rework in masking?

As discussed previously, the number of photomasks is an important factor affecting costs and productivity. The large photomasking area you see, filled with mask aligners and operators, may only reflect a many-masked, high rework process and not a high volume production line. A zero percent rework rate, on the other hand, may not be satisfactory and may indicate that potentially bad material is being passed on to wafer sort.

- Number of photomask aligners?

Count the aligners! They will give you the fastest most accurate estimate of a facility's production. Empty alignment stations are also

3.5 Analyzing an IC Plant

an indication of decreased production or unused capacity. The number of aligners needed for a process depends on the volume of wafers, number of masking steps per wafer, fab yield, re-work rate, downtime of the machines, and the number of equivalent shifts per month that the machines are manned. For an efficient facility:

Wafers out per month =
(800 to 1300) x (number of aligners)

This information can be used to calculate the number of wafers produced. If wafer production is known, it can provide an extremely valuable check on wafer fabrication productivity.

- Number of furnace tubes?

- How many diffusion or furnace steps?

Unless the number of diffusion steps in a particular manufacturer's process is known, the answer to this question may not be too meaningful. Manufacturers with half the number of tubes as their competitors may only have half the number of diffusion steps and may actually have a higher potential capacity because of a shorter process throughput time. You must also determine how many of the tubes are used for engineering evaluations and process development.

- In-line process monitors?

Monitoring instruments measure critical parameters in manufacturing. What kind and how many monitors are used, with what frequency? Are the monitors scrutinized by QA? Do the on-line supervisors know what the monitors are?

- Single or multiple-pass testing? Manual or automatic handling?

- Relationship of QA to fab and process engineering?

Is this relationship constructively interactive or is QA considered simply as a "police" force by manufacturing? To what extent does QA become involved when problems arise—will it aid in providing more frequent monitoring of the troublesome process until the problems are resolved?

- Control procedures?

Do process control procedures exist and if so are they followed? The process flow chart and all specification should be accurate, up to date, and followed. All operators should be performing the processes exactly alike. Testing information should be regularly fed back to engineering support groups.

- Number of total employees?

The number of employees can give an indication of the volume of production for a given product line. Annual revenues per employee varies from about $10,000 for high volume standard products (TTL) to over $20,000 for LSI circuits. If revenue is known, the total number of employees can be a check on productivity, and therefore current or future profitability.

3.6 Equipment List

The following is a list, by area, of the equipment used in our manufacturing model. For each item, the rate of production (if applicable), cost, quantity, and a vendor are given. The following considerations were made in compiling this list:

- The production rate depends on the definition of the process for a specific piece of equipment. We have assumed typical processes based on our experience and have accounted for downtime and daily set-up time.
- There are numerous vendors for much of the equipment and materials. We have listed one or two vendors for information only. This in no way implies that they are the only qualified vendors or that we recommend these vendors over others. Vendors listed may not be the largest and may be geographically limited.
- We assumed that QA, Process, and Product Engineering share the monitoring and electrical test equipment with manufacturing.
- The quantities of equipment listed are for the five-mask, 10,000 wafers out per month manufacturing model we have been describing. A second coater, for example, would be needed if a process has the equivalent of seven masks (including rework).

Table 3.6-1

EQUIPMENT LIST FOR MASKING AREA

Item	Cost Each ($Thousands)	Rate of Production	Number Required	Total Cost ($ Thousands)	Manufacturer	Purpose
1. Automatic Coater	$25.0	400/hour	1	$25.0	GCA/IMS (Santa Clara, CA) II Industries (Mt. View, CA)	Automatically coat wafers with thin photoresist layer
2. Automatic Developer	25.0	170/hour	2	50.0	"	Wash out unexposed photoresist
3. IR Oven	3.5	—	3	10.5	"	Dry solvents out of resist
4. Mask Aligner	21.0	60/hour	5	105.0	Kasper (Mt. View, CA) Cobilt (Sunnyvale, CA)	Align photomask to wafer
5. Align Hood, VLF	1.8	—	3	5.4	Envirco (Albequerque, NM) Microaire (Santa Clara, CA)	Provide clean, filtered airflow over aligner
6. Spin Hood, VLF	1.8	—	1	1.8	"	Provide clean air over coater
7. Mask Dispense, VLF	1.8	—	2	3.6	"	Provide clean air
8. In-Process Inspect, VLF	1.8	—	2	3.6	"	"

(Continued)

3.6 Equipment List

Table 3.6-1

EQUIPMENT LIST FOR MASKING AREA (Continued)

Item	Cost Each ($Thousands)	Rate of Production	Number Required	Total Cost ($ Thousands)	Manufacturer	Purpose
9. Final Inspect, VLF	1.8	—	2	3.6	"	"
10. Etch Sink, 6 foot	2.0	—	4	8.0	Harrington Plastics (Los Angeles, CA)	
11. Clean Sink, 6 foot	2.0	—	4	8.0	"	
12. Microscope, Dark Field	2.0	—	1	2.0	Leitz/Opto-Metic (Rockleigh, NJ)	Inspection
13. Measuring Scope	3.0	—	1	3.0	Vickers Instr. (Malden, MA)	Measure critical dimensions
14. Microscope	1.0	—	6	6.0	Olympus (New Hyde Park, NY)	
15. Spray Rinser/Dryer	2.0	—	8	16.0	Corotek (Garden Grove, CA) Fluorocarbon (Anaheim, CA)	Rinse wafers with DI water & dry
16. Align Table	0.5	—	5	2.5	Kasper (Mt. View, CA)	Isolate aligner from vibrations
17. Convection Oven	5.0	—	1	5.0	Blue M Engineering (Blue Island, ILL)	Re-bake photoresist
18. Desiccators	0.2	—	20	4.0	Precision Lab. Prod. (Mt. View, CA)	Clean wafer storage
19. Mask Storage Cabinets	0.2	—	4	0.8	"	Store mask inventory
20. Temp/Humidity Monitor	0.5	—	1	0.5	Van Waters & Rogers (Burlingame, CA)	
21. Misc. cabinets, tables, chairs				7.0		
22. Develop Hoods, VLF	1.8	—	2	3.6	Microaire (Santa Clara, CA)	
Total Masking Area Cost (6% sales tax added)	$291.4					

Source: DATAQUEST, Inc.

3.6 Equipment List

Table 3.6-2

EQUIPMENT LIST FOR DIFFUSION AREA

Item	Cost Each ($ Thousands)	Rate of Production (wafers)	Number Required	Total Cost ($ Thousands)	Manufacturer	Purpose
1. Furnace, 3 tubes per stack	$12.0	300–750 per shift[1]	4	$48.0	Thermco Products (Orange, CA) Lindberg Hevi Duty (Chicago, IL)	Diffusions and oxidations
2. Sinks, 6 foot	2.0	—	4	8.0	Harrington Plastics (Los Angeles, CA)	
3. Furnace Load Stations (VLF)	2.0	—	2	4.0	Envirco (Albequerque, N.M.) Micro-Air (Santa Clara, CA)	
4. Potentiometer	2.0	—	1	2.0	Doric Scientific Leed & Northrup (Los Angeles, CA)	Measure furnace temperature
5. Optical Pyrometer	2.0	—	1	2.0	Leeds & Northrup (Los Angeles, CA)	Measure susceptor temperature
6. Thickness Measuring System, Dektab	9.0	—	1	9.0	Sloan (Santa Barbara, CA)	Alum., Poly, thick oxides
7. Pinhole Detector	2.7	—	1	2.7	Siltec (Menlo Park, CA)	Oxide quality
8. Microscopes, Dark Field	2.0	—	2	4.0	Leitz/Opto-Metric (Rockleigh, N.J.) Nikon B & L	Inspections
9. Automatic Boat Pullers	2.0	—	6	12.0	HLS Industries (Sunnyvale, CA)	Automatic push/pull into furnace
10. Automatic Jungles	1.2	—	12	14.4	HLS Industries (Sunnyvale, CA) CGI (Sunnyvale, CA)	
11. 4-Point Probe	3.5	—	1	3.5	Signatone (Sunnyvale, CA)	Measure dopant concentrations
12. Utility Sink	1.5	—	1	1.5	Harrington Plastics (Los Angeles, CA)	Test sample prep.
13. Wafer Evaluation Tester	12.0	—	1	12.0	Custom	Wafer evaluation
14. Spray Rinser/ Dryer	2.0	—	4	8.0	Corotek (Garden Grove)	Rinse/dry wafers

(Continued)

3.6 Equipment List

Table 3.6-2

EQUIPMENT LIST FOR DIFFUSION AREA (Continued)

Item	Cost Each ($ Thousands)	Rate of Production (wafers)	Number Required	Total Cost ($ Thousands)	Manufacturer	Purpose
15. Wet Oxidation System	3.0	—	2	6.0	HLS Industries (Sunnyvale, CA)	Fast oxide growth
16. C-V Plotter	6.0	—	1	6.0	MDC (Palo Alto, CA)	Measure furn. & evap. cleanliness
17. H_2 Alarm System	5.0	—	1	5.0	Applied Materials (Santa Clara, CA)	Safety warning
18. Ellipsometer	5.0	—	1	5.0	Applied Materials (Santa Clara, CA)	Measure thin oxides
19. Gas Cylinder Storage Cabinets	0.5	—	2	1.0	Unicorp (Sunnyvale, CA)	Safe storage
20. Dessicators	0.3	—	4	1.2	Precision Lab Prod. (Mt. View, CA)	Store WIP wafers
21. Furnace Tube Washer	3.0	—	1	3.0	Harrington Plastics (Los Angeles, CA)	Clean quartz furnace tubes
22. Reactor Tube Washer	3.0	—	1	3.0	Harrington Plastics (Los Angeles, CA)	Clean quartz reactor tube
23. Utility Sink - Quartzware Clean	1.8	—	1	1.8	Harrington Plastics (Los Angeles, CA)	Clean boats
24. Drying Ovens	1.5	—	1	1.5	Blue M Engineering (Blue Island, IL)	Dry quartzware
25. Angle Lap/ Measurement Equipment	3.0	—	1	3.0	Signatone (Sunnyvale, CA)	Measure junction depth
26. Evap Thickness Monitor	7.0	—	1	7.0	Kronos/Varian Ass. (Palo Alto, CA) Sloan (Santa Barbara, CA)	Automatic thickness control
27. Miscellaneous Tables, cabinets, Tools, chairs				10.0		
Total Diffusion Area Cost (6% sales tax added)	$195.7					

[1] Depends on length of operation and number of wafers operation can handle

Source: DATAQUEST, Inc.

3.6 Equipment List

Table 3.6-3

EQUIPMENT LIST FOR DEPOSITION AREA

Item	Cost Each ($ Thousands)	Rate of Production	Number Required	Total Cost ($ Thousands)	Manufacturer	Purpose
1. Poly Deposition System	$95.0	60/hour	1	$95.0	Unicorp (Sunnyvale, CA)	Deposit poly silicon
	$40.0	36/hour	2	80.0	Applied Materials (Santa Clara, CA)	
2. Oxide Deposition System (Field Vapox)	15.0	36/hour	2	30.0	Pacific Western (Mt. View, CA)	Deposit field vapox
	60.0	160/hour	1		Applied Materials (Santa Clara, CA)	
3. Oxide Deposition System (Topside Glass)	15.0	36/hour	2	30.0	Pacific Western (Mt. View, CA)	Deposit topside glass over metal
	60.0	160/hour	1	60.0	Applied Materials (Santa Clara, CA)	
4. Metallization System (Vacuum)	35.0	65/hour	1	35.0	Varian/NCR (Palo Alto, CA)	Deposit aluminum
Induction Heated Source, or	8.0	—	1	8.0	Applied Materials (Santa Clara, CA)	Power supply for metallization system
Electron Gun, E-gun Power Supply	15.0	—	1	15.0	Airco-Temescal (Berkeley, CA)	
5. Pre-metallization Dip Sink	2.0	—	1	2.0	Harrington Plastics (Los Angeles, CA)	
6. Poly Sink	2.0	—	1	2.0	"	
7. Pre-metal Load Hood	1.5	—	1	1.5	Microaire (Santa Clara, CA)	
8. Poly Load Hood	1.5	—	1	1.5	"	
9. Vapox Load Hoods	1.5	—	4	6.0	"	
10. Spray Rinser/Dryer	2.0	—	1	2.0	Corotek (Garden Grove, CA)	
Total-Deposition Area Cost (6% sales tax added)	$233.2					

Source: DATAQUEST, Inc.

3.6 Equipment List

Table 3.6-4
EQUIPMENT LIST FOR ASSEMBLY

Item	Cost Each ($ Thousands)	Rate of Production	Number Required	Total Cost ($ Thousands)	Manufacturer	Purpose
1. Scriber	$ 6.2	20 wafers/ hour	2	$12.4	Tempress (Los Gatos, CA)	Scribe wafers
2. Breaker	5.0	60 wafers/ hour	1	5.0	IC Automation (Santa Cruz, CA)	Break wafers
3. Microscopes (Die Visual)	1.0	180 die/hr	6	6.0	Olympus (New Hyde Park, NY)	Inspection
4. Die Attacher	3.0	450 die/hr	2	6.0	K & S (Santa Clara, CA)	Attach die to lead frame
5. Lead Bonder	5.0	100 units/ hour	10	50.0	Unitek (Monrovia, CA)	Attach wires from die to leads on lead frame
6. Microscopes (Pre-seal)	1.0	400 units/ hour	3	3.0	Olympus (New Hyde Park, NY)	Inspection
7. Press	40.0	2K units/hr	1	40.0	Poly Mold (San Jose, CA)	Encapsulate unit in plastic
8. Mold	20.0	—	1	20.0	"	"
9. Oven	10.0	10K units/hr	2	20.0	Blue M Engineering (Blue Island, ILL)	Temperature cycling, cure
10. Lead Trimmer/ Bender	5.0	5K units/hr	1	5.0	Adcotech (Sunnyvale, CA)	Trim (cut) leads, bend leads
11. Tinner	3.0	4K units/hr	1	3.0	Custom	Coat leads with conductive metal
12. Symbolizer	5.0	1.1K units/hr	1	5.0	Markem	Mark part number, logo, etc. on device
13. Misc. jigging, fixtures	—	—	—	10.0		
Total Assembly Area Cost (6% sales tax added)	$196.5					

Source: DATAQUEST, Inc.

3.6 Equipment List

Table 3.6-5

EQUIPMENT LIST FOR TEST AREA

Item	Cost Each ($ Thousands)	Rate of Production	Number Required	Total Cost ($ Thousands)	Manufacturer	Purpose
Wafer Sort						
1. Probers	$14.0	12 wafers/ hour	3	$ 42.0	Electroglas (Santa Clara, CA) Pacific Western (Mt. View, CA)	Make electrical contact to circuit on the wafer
2. Tester-Wafer Sort-2 Stations	60.0	—	2	120.0	Pacific Western (Mt. View, CA)	Electrically test circuit
3. Microscope	1.0	—	1	1.0	Olympus (New Hyde Park, NY)	Inspection
Total-Wafer Sort Cost (6% sales tax added)	$172.8					
Final Test						
1. Auto. Handlers	7.5	1000/hr/oper.	1	7.5	Contrell (Sunnyvale, CA) IPT Corp. (Sunnyvale, CA)	Provides automatic handling of devices
2. Environmental Chamber	25.0	—	2	50.0	Delta Design (San Diego, CA)	Testing at different temperatures
3. Tester-Final Test	275.0	—	1	275.0	Fairchild Systems (Mt. View, CA) Teradyne (Boston, MASS)	Electrically test circuit
Total-Final Test Cost (6% sales tax added)	$352.5					

Source: DATAQUEST, Inc.

3.7 Materials List

The following is a list of some of the most frequently used materials in the manufacturing operations, along with some potential vendors. Again, other qualified vendors also supply many of these products. Our intent here is to reflect at least one qualified vendor per product.

Table 3.7-1

MATERIALS LIST FOR WAFER FABRICATION

Item	Cost	Vendor
Silicon Wafers	$7.00	Applied Materials (Santa Clara, CA) Monsanto (St. Peters, MO) Siltec (Menlo Park, CA)
Quartz Furnace Tubes	$200 – $300	Berkeley Glass (Emeryville, CA) U.S. Fused Quartz (Fairfield, NJ)
Masks	$4 – $5	Micromask (Mt. View, CA) Transmask (Newport Beach, CA)
Quartz Boats, custom glassware	$40 – $300	Berkeley Glass (Emeryville, CA) M & M Glass (Sunnyvale, CA)
Gas Cylinders	$150 – $450	Matheson Gas Products (Newark, CA) Precision Gas Products (Rahway, NJ)
Solvents, Acids		J. T. Baker (Phillipsburg, NJ) Allied Chemical (Morristown, NJ)
Photoresist	$30 – $80 per quart	Kodak (Rochester, NY) Shipley (Newton, MA)
Clean Room Smocks		Red Star (San Jose, CA) Acme Uniform (San Francisco, CA)
Liquid Dopant Sources	50¢ – 60¢ per gram	Mallinckrodt (St. Louis, MO) Baker and Adams

(Continued)

3.7 Materials List

Table 3.7-1

MATERIALS LIST FOR WAFER FABRICATION

(Continued)

Small, general items (beakers, hot plates, etc.)		Scientific Products (Palo Alto, CA) Van Waters & Rogers (Burlingame, CA)
High Purity Aluminum		MRC (Orangesburg, NY)
Fittings, brass & stainless steel		Van Dyke Valve & Fitting (Sunnyvale, CA)
Pressure Regulators	$35 – $85	Victor Equipment (Santa Clara, CA) Elchem (Saratoga, CA)
Gas Flowmeters	$40 – $70	Brooks Flowmeters (Hatfield, PA) Fisher & Porter (Warminster, PA)
Teflon Wafer Boats, for Acid Etches	$25 – $40	Fluoroware (Chaska, Minn)
Thermocouples	$150 – $200	Calimatic (Santa Clara, CA)
Filters		Millipore (Bedford, MA)
Susceptors	$400	Dow Corning Texas Instruments Ultra Carbon

Source: DATAQUEST, Inc.

3.7 Materials List

Table 3.7-2

MATERIALS LIST FOR TEST AND ASSEMBLY

Item	Cost	Vendor
Probe cards	$60 – $100	Rucker & Kolls (Mt. View, CA)
Conductive Foam		Gillis & Lane (Redwood City, CA)
Diamond Scribe Tips	$10	Tempress (Los Gatos, CA)
Gold Wire		Plessey Incorp. (Melville, NY)
Aluminum Wire		Plessey Incorp. (Melville, NY)
Leadframes	10¢ – 20¢ per frame (of 10)	Sylvania
Epoxy	$2.00/lb.	Allied Chemical (Morristown, NJ)
		Morton
Silicone	$7.00/lb.	Dow Corning Corp. (Midland, MI)

Source: DATAQUEST, Inc.

3.8 Updated Manufacturing Model

This section describes the new, updated manufacturing line, which utilizes current manufacturing equipment available in 1977. The yield trends brought about by equipment changes are discussed, new manufacturing operations instituted since 1975 are described, and a thoroughgoing cost analysis of the new plant is made. The last subsection discusses plant design, describing process flow and line balance. Detailed equipment lists are given to support capital cost totals, and labor estimates are provided for the wafer fabrication and test areas. There is no discussion of new assembly techniques because, although significant changes have occurred in assembly in the last few years, they have generally been implemented on more mature products like TTL. For this reason, it is not practical to discuss them in connection with the 4K RAM line.

YIELD TRENDS

When a semiconductor wafer is fabricated, it contains many potentially good dice. Unfortunately, however, not all the dice are actually good, so it is necessary to test them during wafer sort and to mark the bad dice. The number of good dice divided by the total number of potentially good dice is commonly expressed as a percentage and is known as the wafer sort yield.

Bad dice occur because there is some sort of defect in the silicon material, the mask used to create circuit patterns on the wafer, or weaknesses induced during processing. These defects interfere with the circuit and cause some portion of it to be inoperative. Yield at wafer sort can be related to the number of defects in a given area of the finished silicon wafer—i.e., the more defects per square inch or square centimeter, the lower the yield.

Likewise, if the defect density were fixed, a small die would be much less likely to encompass a defect than would a large die. For instance, if defects were 100 mils apart, a die which measured 10 mils on a side would be unlikely to encompass a defect. On the other hand, a 200-mil die would have a high probability of intercepting a defect. Thus, for a fixed defect density, the yield decreases as the die size becomes larger.

Generally, most defects are associated either with processing or with defects in the mask itself. Since the amount of processing increases with the number of mask levels, it has become the practice to speak of the number of defects for each mask level. Thus, if the defect density per level and die size are fixed, the wafer sort yield will decrease as the number of mask levels increases. Wafer sort yield can be predicted using the formula:

$$\text{Yield} = 1/(1 + DA)^n$$

Where D is defect density, A is die area, and n is the number of mask levels. Note that as A and n become small, the yield approaches 100 percent.

If the die area and the number of mask levels are fixed, the defect density is of crucial importance in determining yield. Table 3.8-1 traces the historical reductions in inferred defect densities from 1965 to 1977. They are inferred because they are obtained by using the above formula to work backward from the wafer sort yield, die size, and number of mask levels to obtain the defect density. They were not obtained by actually counting defects on any actual silicon wafer.

Table 3.8-1 shows that average defect densities in the semiconductor industry have been decreasing dramatically during the past 12 years. Note that between 1975 and 1976, the typical defect densities declined from 3.6 to 2.46 per square centimeter, causing an increase in yield for the 150-mil square 4K RAM from 12 to 22 percent—almost a factor of two. This yield improvement is associated with the

3.8 Updated Manufacturing Model

Table 3.8-1

HISTORY OF INFERRED DEFECT DENSITIES

Year	Typical Wafer Sort Yield	Die Size (Mils)	Number of Mask Layers	Defect Density (Per sq. cm.)	Comment
1965	60%	40	6 (bipolar)	10	–
1967	10%	94	5 (MOS)	10	–
1975	12%[1]	150	5 (MOS)	3.6	From Fig. 3.2-3
1976	22%[2]	150	5 (MOS)	2.5	–
1977	40%[3]	150	5 (MOS)	1.4	–
1977	26%[4]	452	11 (CCD)	0.1	R&D device

[1] 4K RAM with emulsion masks.
[2] 4K RAM with hard surface masks.
[3] 4K RAM with projection printing.
[4] Master masks were optically inspected and the defects eliminated manually with laser "ZAPPER".

Source: DATAQUEST, Inc.

change from emulsion to hard-surface masks. Projection printing has given rise to another average defect density decrease from 2.46 to 1.40 per square centimeter, increasing the wafer sort yield once more—from 22 to 40 percent. (Recently, certain manufacturers have apparently achieved similar or better yields with conventional contact aligners using special photoresist techniques.)

The last device in Table 3.8-1 is a CCD device manufactured in an R&D environment using carefully controlled projection printing. Considering the large 450-mil die size, the yield shown is very large, corresponding to an inferred defect density of only 0.1 per square centimeter. If this defect density could be achieved on the 4K RAM line in a production environment, the predicted wafer sort yield would be an extremely high 93 percent—or more than two-and-one-half times the wafer sort yield assumed in the financial model of this section. The result would be an almost proportionate increase in plant capacity. Therefore, a high financial incentive exists for semiconductor manufacturers to achieve this kind of yield improvement.

Before projection aligners were introduced, images were transferred from the photomask to the wafer by bringing the mask into contact with the silicon wafer itself. This approach resulted in damage to the mask by the silicon wafer even with the use of the so-called proximity printers that supposedly brought the mask close enough to make a good image without actually touching. The contact between wafer and mask eventually caused enough mask defects so that it was necessary to throw the mask away and obtain a new one. Since defect densities increased as the mask was used, the significant defect density is the average between that obtained on new and used masks.

Table 3.8-2 shows typical defect densities obtained with various kinds of masks. (Although the defects were measured on actual

3.8 Updated Manufacturing Model

masks, the numbers quoted may not be strictly accurate because the definition of defects varies somewhat and because human operators are unable to catch all defects accurately. Recently, Bell Laboratories developed an Automatic Mask Inspection System (AMIS) to enable it to monitor defect levels more accurately.) Defect densities are shown for both new and used masks. The average defect density is simply the average of a new and a used working plate or mask. It can be seen that the hard-surface plate had average defect densities somewhat lower than that of the emulsion working plate. This reduction in defects accounts for the improved yield of 4K RAMs between 1975 and 1976.

Table 3.8-2 also shows the defect level obtained on a stepped master mask. Since projection printers do not wear out masks, it is economically feasible to use the more expensive master masks to expose wafers. The lower defect density of the master masks gives rise to the 40 percent wafer sort yield for 4K RAMs in 1977. Master masks have a lower defect density than working plates because working plates are produced from master masks by the contact printing method, which induces defects. First, the master mask is contact-printed onto a submaster, inducing defects, and then the submaster itself is contact-printed onto the working plate, inducing still more defects. This situation accounts for the difference in defect density between the stepped master and the hard-surface

Table 3.8-2

MASK DEFECT DENSITIES

Mask Type	Defect Density (Per sq. cm.)	Defect Density (Per sq. in.)	Cost Per Layer	Comments
Repaired Master	.16	1.0	$600.00	–
Mask Blanks	.2	1.3	–	–
Stepped Master	.5	3.2	$ 75.00	–
Hard-Surface Working Plate	1.25	8.0	$ 37.00	–
Hard-Surface Working Plate, Used	1.86	12.0	–	After 100 soft contact exposures or 50 hard contact exposures.
Average Hard-Surface Defect Level	1.56	10.0	–	–
Emulsion Plate	1.86	12.0	$ 5.50	–
Emulsion Plate, Used	3.54	22.8	–	After 10 hard contact exposures.
Average Emulsion Plate Defect Level	2.70	17.4	–	–

Source: DATAQUEST, Inc.

3.8 Updated Manufacturing Model

or emulsion working plate. The defect level quoted for new emulsion plates is higher than that of new hard-surface plates; because of the lower cost, the mask maker cannot afford so much quality control. Indeed, Table 3.8-2 shows a strong inverse correlation between the defect level and the cost per layer.

If the defect levels of the masks in Table 3.8-2 are subtracted from the inferred defect levels of Table 3.8-1, the result is a constant difference of 0.9 defects per square centimeter. This difference is attributable to defects induced during processing. Interestingly enough, the R&D device shown in Figure 3.8-1 has achieved defect densities of 0.1 per square centimeter, well below the defects resulting from the use of master masks or those that are process-related. The research staff that developed the device actually used master masks in which the defects had been "repaired" by eliminating defects with a laser "zapper." Apparently, they were also successful in significantly reducing process-related defects, but it is not known how that was accomplished.

NEW MANUFACTURING OPERATIONS

This section updates Section 3.1 and describes those operations that have changed since 1975. The equipment changes include:

- The use of low-pressure continuous vapor deposition (LPCVD) for fabricating the polysilicon layer
- The use of a dual electron beam evaporator to deposit an aluminum-silicon layer
- The addition of an ion-implanter
- The change to automatic photoresist processing and projection alignment in photomasking
- The addition of plasma-resist stripping

The new process has eight mask levels rather than the five levels used in the old process. The additional mask levels permit: (1) the addition of a field ion-implant that allows independent control of field thresholds and the thresholds of the active MOS devices; (2) ion-implanting of pull-up devices to make depletion loads, which has the effect of eliminating the second positive power supply formerly needed on LSI devices; and (3) the addition of a direct contact between the polysilicon layer and the silicon layer, which allows an increase of functional packing density. Additional details of new process flow are given in Figure 3.8-3 and in the later subsection, **Process Flow**.

Polysilicon Deposition

The poly deposition process described in Section 3.1 under ***Poly Deposition*** made use of an RF-heated metal plate that transferred heat to the wafers by conduction. This device was expensive, had limited throughput, and was somewhat difficult to control. The control problems came about because the wafers were heated unevenly if they did not lie perfectly flat on the metal plate. Since the deposition rate is a function of temperature, uneven wafers tended to have uneven polysilicon layers.

The new poly deposition process makes use of low-pressure chemical vapor deposition (LPCVD) equipment. This device is a diffusion tube that is operated at less than atmospheric pressure. The wafers are heated by radiation rather than conduction; as a result, heating is more even and the polysilicon layers are more uniform. In addition to offering better uniformity, the LPCVD equipment is somewhat less expensive than the old equipment and has a higher throughput rate. The old poly deposition system cost $95,000 and had a throughput rate of 60 wafers per hour, whereas the new system

costs $30,000 (excluding the furnace tube) and has a throughput rate of 106 wafers per hour.

Alluminum-Silicon Metallization

Since 1975, geometries in N-channel silicon gate devices have become somewhat smaller which, in turn, has led to a desire for shallower diffused N-regions. Since the N-regions spread sideways as they diffuse deeper into the silicon wafer, the sideways spread can only be reduced by diffusing less deeply. When shallower diffused regions are employed, a metallization problem results, which is caused by the fact that aluminum itself is a P-type dopant. Thus, if aluminum is deposited on a shallow N-type diffused region, there is a high probability that the aluminum will penetrate completely through the N-region during the subsequent alloy step, thus shorting out the junction.

The aluminum penetrates into the silicon because there is a preferred mixture of aluminum and silicon at alloy temperatures; silicon migrates into the aluminum, and simultaneously the aluminum dissolves in the silicon. In any event, this migration can be prevented if a small amount of silicon is added to the aluminum as it is being deposited on the wafer. The deposited aluminum will then contain all the silicon that it can accomodate at alloy temperature, and no migration can occur. Some manufacturers deposit more complex materials than aluminum-silicon (e.g., aluminum-silicon-copper or aluminum-copper).

The old N-channel line used an electron beam evaporator to vacuum-deposit aluminum on the silicon wafer. This equipment cannot evaporate a combination of aluminum and silicon, so new equipment was needed for the new line. The new equipment has a dual-electron beam—one beam for the aluminum and one beam for the silicon—and costs $75,000; it replaces the old single-electron beam evaporator that cost $50,000. An alternative to the electron beam evaporator in both the old and new diffusion rooms is an evaporator that heats the source by electromagnetic induction rather than by an electron beam. Both systems are used in practice.

Another method of evaporating materials is through sputtering. This process uses an ion beam rather than an electron beam. The ions hit the target and "knock off" molecules, which deposit themselves on the wafer. One advantage of this process is that the chemical composition of the target material tends to be maintained during evaporation; consequently, it would be a good candidate for silicon-aluminum evaporation. However, sputtering has not always eliminated other methods in spite of the existence of cases where it might be a more effective technique.

Ion-Implant

Ion-implant is analogous to diffusion in some ways inasmuch as it is a means of introducing controlled amounts of "impurities" or dopants into a silicon material. This technique is attractive because it offers much more precise control of the impurity concentrations than does diffusion. Typically, diffusion concentrations can only be controlled within a factor of 2 to 1, whereas ion-implantation allows control of concentrations to less than 5 percent.

In an ion-implanter the desired dopant (i.e., boron) is first ionized by a radio frequency field. Some atoms may have only one electron removed while others may have two or more removed by this process. The atoms with the desired number of missing electrons are selected from the ion stream by passing all ions through a filter. This device removes the unwanted ions, allowing only the desired ones to pass. The desired ions are then allowed to fall through an electric field potential of approximately 300,000 volts, which accelerates the ions

until they move at a high velocity. They then "crash" into the silicon wafer and because of their high velocity penetrate some distance into the silicon material itself.

Generally, the ions are focused into a beam and the entire silicon wafer is covered with ions by sweeping the beam back and forth to "paint" the wafer, much as an electron beam in a television set is swept back and forth to "paint" a television picture. The depth of ion penetration depends on the velocity of impact. The number of ions deposited in a given area can be precisely controlled by controlling the beam current and the sweep rate. In the processes described in this section, about 10 seconds is typically required to implant a wafer. Other processes requiring heavier ion concentrations may have implant times as long as several hours.

Ion implant is used in our process to implant the field region and to implant beneath the gates of the pull-up devices to create "depletion loads." Some MOS processes also use an ion implant beneath the active MOS transistors to allow more precise control of threshold voltage. Ion implant is prevented in regions where it is not desired by masking with photoresist; the ions simply enter the photoresist and are decelerated there.

Photomasking

The photomasking area has two significant changes—the substitution of projection printers for contact or proximity aligners and the addition of an automated photoresist processing line.

The projection printing aligners are responsible for the significant yield improvements discussed in the beginning of this section under the heading **YIELD TRENDS**, although one manufacturer is believed to be obtaining similar yields without projection alignment through improved photoresist techniques. Fundamentally, these aligners project an image of a mask on the wafer in much the same way a slide projector projects an image of a 35 millimeter slide on a viewing screen. This technique requires use of a lens system to create the desired images.

By contrast, older methods of aligning and printing masks used no lenses at all between the mask and the wafer. Consequently, it was necessary to bring the mask very close to or in contact with the wafer so that the image (or shadow) on the wafer would faithfully reproduce the image on the mask. This process gradually destroyed the mask, as it was scratched by the wafer and pieces of photoresist stuck to it. These defects printed onto subsequent wafers, causing devices to be unacceptable.

Projection printing has been a dream of many years; in fact, work was begun on this technique in the mid-1960s. The problem is a complex one, however, because of the difficulty in making a lens of sufficient quality to resolve the images as finely as required by the semiconductor industry. Because of the resolution problem, masks are made by a "step and repeat" process, which creates multiple copies of the same pattern on a master mask through a series of multiple exposures. In this way, the lens that creates the images needs to resolve only a single die pattern and not the entire mask. These lenses, which are fairly expensive and may cost as much as $10,000, still do not have the resolution required for projection printing.

Lenses suffer from a defect known as "chromatic aberration," in which light of different colors is bent at slightly different angles as it passes through the lens, much as in a prism. Although most high-quality lenses are designed for only a narrow range of light colors (or narrow spectrum), they still have difficulty obtaining the desired resolution.

The first successful projection aligner, built by Perkin-Elmer, employed mirrors as lenses,

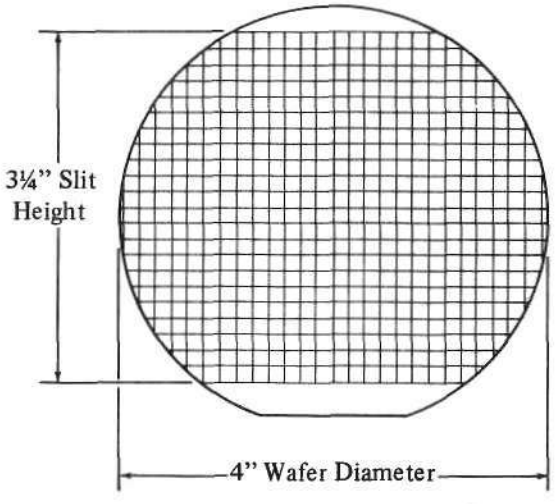
3.8 Updated Manufacturing Model

somewhat like those used in large telescopes. (It is believed that Cobilt has a similar piece of equipment in the final stages of development. This equipment will expose a full 4-inch wafer and has adaptive focus, partial field scanning, potentially higher throughput, and automatic alignment and loading.) Since light never passes through any lens in either of these systems, the problem of chromatic aberration is avoided and very fine lines can be reproduced. Because the mirror-lenses reflect different colors of light equally, it is possible to use a light source containing many colors. Printing of finer lines is also possible because the mirror-lens technique alleviates some of the problems of "standing waves" in the photoresist. These waves are caused by reflections from the boundary between photoresist and silicon. When single-color light is used, the reflected light cancels the incident light in some areas, causing the photoresist to be underexposed. This phenomenon does not occur when light of many colors is used because each color of light has a region of cancellation at a different position in the photoresist. Thus, where one color of light cancels out, another color does not; the result is a more uniform photoresist exposure.

Successful projection aligners make use of spherical mirrors, which produce only a narrow region of perfect focus. The light is made to fall on the mask only in this region by putting a slit between the light source and the mask; therefore, only a narrow portion of the wafer (corresponding to the slit) is exposed at any given time. Because of the lens size, the slit height is 3.25 inches. The entire wafer is exposed in this system by moving the mask and wafer simultaneously past the slit of light. The slit is affixed to the stationary light source, and the mask and wafer are then both mounted to a rigid carriage that sweeps them past the slit of light. Thus, the wafer is totally exposed as the slit of light passes across it. Since the mask and wafer move together past the light slit, there is no theoretical limit to the size of the exposed area in the direction of travel. Figure 3.8-1 shows the exposure pattern that would result on a 4-inch wafer. Although the pattern is only 3.25 inches high, it is 4 inches long. As a result, over 90 percent of the available wafer surface is exposed. For some time many semiconductor manufacturers thought the projection alignment equipment limited them to 3-inch wafers; now it is apparent that there is a compelling reason to work with 4-inch wafers. The wafer in Figure 3.8-1 has 440 potentially good dice as compared with 250 potentially good dice on a 3-inch wafer. The extra dice gained in this manner more than pay for the cost of the additional silicon in a 4-inch wafer.

Figure 3.8-1

PROJECTION ALIGNER EXPOSURE PATTERN ON 4 INCH WAFER



440 Potentially Good 150 Mil Die.

Source: DATAQUEST, Inc.

3.8 Updated Manufacturing Model

The throughput rate on projection alignment equipment is significantly higher than the older alignment fixtures used in the 1975 line—100 wafers per hour as opposed to 60 wafers per hour. This figure, obtained from a Perkin-Elmer customer who uses all negative photoresist, represents the average of his most efficient and least efficient operators. Exposure times with negative resists typically run 6 seconds as compared with 30 seconds for positive resist. Naturally, throughput would be slower if positive resists were used. Some users favor positive resist because they believe it allows them to obtain better resolution. Most believe that the resolution of the Perkin-Elmer system is limited to about 3 microns (a micron is one-millionth of a meter).

In projection alignment equipment, there is a tradeoff between resolution and exposure time. As the slit is made wider, more of the wafer is exposed, and consequently the speed of mechanical slit movement can be increased. Since the slit is appreciably wider than the region of "perfect" focus, resolution suffers. Similarly, resolution can be improved at the expense of throughput rate by narrowing the slit and slowing the rate of mechanical travel.

Early users of projection alignment equipment did not achieve satisfactory results because they did not provide the proper operating environment for the equipment. As one user states, "The equipment only works well in an engineering environment; accordingly, it is necessary to create an engineering environment in the masking room." Among other things, frequent preventive maintenance is required and daily focus checks must be run. Some users did not achieve good results because they continued to buy lower-cost masks with high defect levels. Projection alignment equipment also requires effective control of ambient temperature and humidity. Since the mask and wafer are separated by some distance, a small temperature change can cause the mounting system to expand slightly, changing the mask-to-wafer spacing and throwing the system out of focus. More than a day is required to stabilize the system after control of ambient temperature and humidity is lost. For this reason, special laminar flow hoods with good ambient controls are used with projection alignment equipment.

The 1975 line had five aligners—one for each mask level—costing a total of $105,000. The 1977 line has eight projection aligners—costing a total of $1,316,000. The throughput of the new equipment is somewhat higher—100 wafers per hour compared with 60. The principal justification for this equipment is the dramatic increase in wafer sort yield that it provides. Some users report that they have achieved payoff of their new aligners in periods as short as three to six months. At this time, a majority of the installed projection alignment equipment are Perkin-Elmer units. Canon and Kasper also make projection aligners using lenses rather than mirrors; their equipment has not been as well received to date. Cobilt is believed to be working on a system similar to that of Perkin-Elmer.

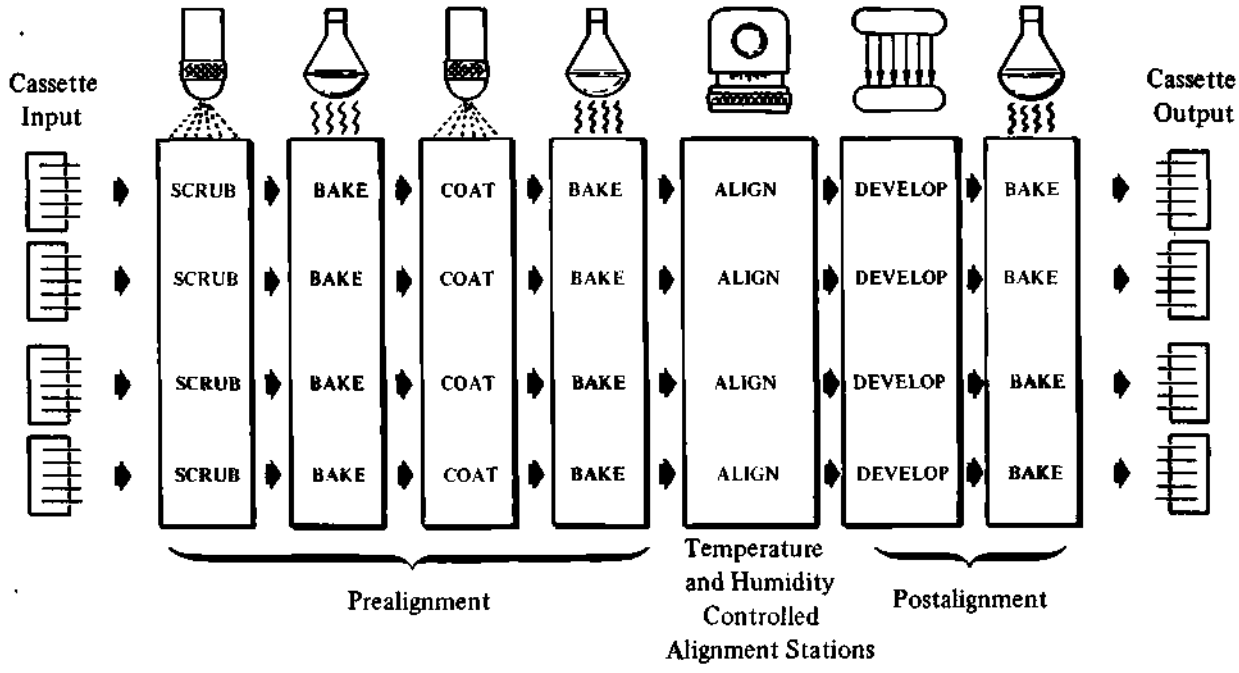
Figure 3.8-2 shows a schematic representation of an automatic photoresist processing line. It is a 4-track line servicing four aligners and contains stations that scrub (or clean), bake (or dry), coat (spin on liquid photoresist), and bake (dry the photoresist) the wafers before presenting them to the aligner. A similar set of stations develops the photoresist after it has been exposed and bakes the photoresist once more. This sequence of steps is merely representative and does not illustrate any particular process.

In the old line, each station in Figure 3.8-2 was represented by a separate piece of equipment to scrub, bake, coat, and develop. Each piece of equipment had a dessicator or drybox that held wafers while they were waiting to be processed. The wait time between process steps was highly variable; in fact, it was 10 times

3.8 Updated Manufacturing Model

Figure 3.8-2

FOUR STATION AUTOMATIC MASKING LINE



Source : DATAQUEST, Inc.

longer than the process time itself.

Photoresist processing requires tight control of parameters. As an example, the optimum bake time depends on how long wafers have been stored after leaving the coat or develop stations. If storage time is variable, then the process cannot be optimized with a fixed bake time. Therefore, some wafers leave photoresist processing, fail to pass a subsequent in-process inspection, and must be sent back for rework. Industry estimates vary, but from 5 to 30 percent of the wafers may have to be reworked. Our old line assumed a relatively optimistic 7 percent rework rate.

The automatic photoresist processing system shown in Figure 3.8-2 eliminates all inventory points between the cassette input and the cassette output by moving the wafers from station to station on a conveyor track. Various means of accomplishing the conveyor are offered by equipment suppliers—some use air jets, others use belt systems, and still others use a vibrating track method.

Conveying wafers automatically results in better control of photoresist processing because the storage time between steps is constant, causing a concurrent reduction in rework rates. Here we have assumed that rework is essentially negligible. Furthermore, the elimination of in-process inventory improves throughput time and reduces investment in work in process. If the times required for every process step of

the new 8-mask process are totaled, the complete process time is 18 hours or 2-1/4 working days. Yet, it is typical for a wafer to spend three or four weeks in the fabrication area; therefore, the wafer must be in inventory (instead of in processing) about 90 percent of the time.

The 8-mask process has 47 separate wafer fabrication process steps when automated photoresist processing is used. If manual photoresist processing were used and each in-process inventory point were counted as a process step, the total number of steps would more than double—to 95. If the wafer spends three to four weeks in fabrication for a 95-step process, it should spend only one-and-a-half to two weeks in fabrication for a 47-step process.

The savings in work-in-process inventory can be computed by assuming a one-and-a-half-week savings in throughput time. If 10,000 wafers a month come out of fabrication at a material cost of $22.66 each (see Table 3.8-5), the savings due to this shorter "pipeline" would be $78,000. This savings would help pay for the difference in cost between an automated handling system and a manual handling system, a difference that is estimated at $132,000.

The automated photoresist processing line allows processing to be accomplished with fewer workers. In our case, we have assumed two workers instead of six workers and the addition of two maintenance technicians, for a net savings in direct labor (exclusive of fringe) of $11,600 annually. Further savings would probably be generated through yield improvements, but such savings are difficult to estimate. Yield improvements result from more efficient control of processing, as mentioned earlier, and from the fact that the equipment in the automated photoresist processing line is microprocessor controlled. This approach allows continuous monitoring of each piece of equipment to determine whether it is working correctly. If the performance of a piece of equipment exceeds specification limits, it is shut down and a maintenance man called before any material can be damaged.

Plasma Resist Stripping

The plasma state is often referred to as "the fourth state of matter"—the other three states being liquid, solid, and gas. When a material is excited into a plasma by the removal of one or more valence electrons, its chemical properties change. Sometimes new properties are encountered that can be used to advantage in semiconductor processing. There is a high interest in plasma chemistry at the present time because researchers believe it will eventually be possible to eliminate "wet" chemistry altogether and substitute "dry" plasma chemistry. The effect would be to permit smaller geometries than can be achieved with wet chemistry. Furthermore, plasma chemistry appears to be more economical in its use of raw material and other resources, such as power. Plasma chemistry has been used to etch SiO_2 and aluminum and strip photoresist. Researchers are actively working to extend the applicability of plasma chemistry still further.

Currently, many wafer fabrication areas limit their plasma chemistry to photoresist stripping, since this application was the first practical one. In this process, oxygen is ionized and passed over the wafer. The oxygen reacts with the photoresist and removes it from the wafer without removing anything else. In our new process, only plasma resist stripping is used. If a high-temperature diffusion step follows plasma stripping, the wafer is first washed in deionized water to ensure removal of any residue left after plasma stripping.

COST ANALYSIS

A cost analysis for the new manufacturing line is given in Tables 3.8-3 through 3.8-8.

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These costs are supported by additional detail in the subsection entitled **PLANT DESIGN** where equipment lists are given to support capital costs, and manpower loadings are given to support labor costs. This section presents cost data that begin with the total product cost and work backward to provide the supporting detail.

	Plastic Package	Ceramic Package
Factory Cost	$.60	$1.21

The table above gives total product cost. Here the factory cost for the 4K RAM is $0.60 in plastic and $1.21 in ceramic. Depending on the gross margin of the particular manufacturer and on market factors, the part should sell for a mark-up of two or more times cost.

The cost analysis in this section gives no detailed breakdown for assembly costs. Instead, it is assumed that assembly is simply purchased in an offshore facility. This practice is common in the industry and even if a company had its own offshore assembly, it would very likely be treated as a separate cost center for accounting purposes.

Table 3.8-3 gives a detailed breakdown of the costs listed above. Here the wafer cost is built up as the sum of "fixed" and "variable" costs. (These terms are put in quotations because it is a matter of judgment as to whether certain costs are fixed or variable. However, since our new line is operating well below capacity, it is important to make the distinction inasmuch as "fixed" costs per wafer could be expected to decrease as wafer volume increased.)

The cost per net die is then obtained by first allocating 40 percent of the "fixed" wafer sort costs to the 4K RAM. Since only 4,000 wafers per month of the 10,000 started are used for the 4K RAM, it is natural that this product bear only 40 percent of the wafer sort cost. The remaining 60 percent is borne by other products. The fixed and variable costs per die are then added to the die cost per unit (obtained by dividing the wafer cost by the gross die per wafer) with a result of 10.28 cents. This number is then divided by the sort yield to obtain the cost per net die of 25.70 cents.

Assembly and final test costs are handled in a similar fashion, except that only one-third of the fixed final test costs are allocated to the 4K RAM because the product mix in finished units is somewhat different from the mix of wafer starts. This situation would occur if the die size and sort yield of other products differed from those of the 4K RAM. In assembly and final test, the package costs are separated from the die costs and added together at the end. These figures show that 67 percent of the cost (39.78 cents out of 59.77 cents) is die cost in the plastic package, whereas only 33 percent of the cost is die cost when a ceramic package is used (39.78 cents out of $1.2066).

Table 3.8-4 gives a breakdown of the volume-insensitive or "fixed" costs for the various areas. Here the recurring expenses, like utilities and property taxes, were allocated somewhat arbitrarily between wafer fabrication, sort, and final test. A certain portion of the indirect labor was assumed to be "fixed" inasmuch as the line would require a skeleton staff to keep it running and to process the sustaining wafers. (These wafers are needed to run tests on the process to ensure that it is still in control.) The line can also be used for a limited amount of process improvement work.

Finally, the capital cost (or depreciation) is added to the monthly fixed costs to arrive at a total monthly cost of $151,264. Most wafer fabrication facilities of this type break even at around $300,000 a month in gross revenue. If our new line were to break even at this point, we would have $148,736 ($300,000 minus $151,264) available to pay the variable cost per wafer. This figure corresponds to $148,736/30.23 or 4,920 wafer starts per month and a

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Table 3.8-3

DETAILED PRODUCT COST ANALYSIS (4K RAM ONLY)

Function	Wafer Cost	Dice Cost	Package Cost	
			Plastic	Ceramic
Wafer Fabrication				
"Fixed" Costs per Month	$122,464	–	–	–
"Fixed" Cost/Wafer at 10,000 Wafers/Month	$12.25	–	–	–
Plus "Variable" Costs	30.23	–	–	–
Total	$42.48	–	–	–
Wafer Sort				
Allocated "Fixed" Costs (40% x $13,337)		$5,335	–	–
"Fixed" Cost/Unit at 1,760,000 Units/Month		0.0030	–	–
Plus "Variable" Costs		0.0033	–	–
Plus Wafer Cost/Unit ($42.48/440/die/wafer)		0.0965	–	–
Total (Cost per Gross Die Wafer Sort)		$0.1028	–	–
(Cost per Net Die - $0.1028/40% Sort Yield)		$0.2570	–	–
Assembly				
Die Cost		$0.2570	–	–
Material and Occupancy		–	$0.0560	$0.5399
Labor		–	0.0430	0.0040
Capital		–	0.0160	0.0060
Extra Costs of Asian Assembly		–	0.0150	0.0200
Total (Cost per Gross Die at assembly)		$0.2570	$0.1300	$0.5699
(Cost per Net Die - divide by 85% assembly yield)		$0.3024	$0.1529	$0.6705
Final Test				
Allocated "Fixed" Costs (1/3 x $15,463)		$5,154	–	–
"Fixed" Cost/Unit (598,400 units)		0.0086	–	–
"Variable" Cost/Unit		0.0271	–	–
Die Cost From Assembly		0.3024	$0.1529	$0.6705
Total (Cost per Gross Die at Final Test)		$0.3381	$0.1529	$0.6705
(Cost per Net Die - divide by 85% final test yield)		$0.3978	$0.1799	$0.7888
Pack and Ship		–	0.0200	0.0200
Total (Cost per Net Die)		$0.3978	$0.1999	$0.8088
Dice and Package Cost		–	$0.5977	$1.2066

Source: DATAQUEST, Inc.

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Table 3.8-4

VOLUME-INSENSITIVE COSTS ("FIXED")
(Monthly Costs)

Type of Expense	Wafer Fabrication	Test		Total
		Sort	Final	
Recurring Expenses				
Utilities	$ 16,000	$ 1,200	$ 800	$ 18,000
Property Tax	10,000	3,600	2,400	16,000
Industrial Gasses	2,300	120	80	2,500
Water and Sewer	1,000	120	80	1,200
Building Rental	6,000	600	400	7,000
Subtotal	$ 35,300	$ 5,640	$ 3,760	$ 44,700
Labor (including fringe)				
Supervision	$ 3,000	$ 1,500	$ 1,000	$ 5,500
Process Sustaining	7,500	–	–	7,500
Test Engineer	–	1,080	720	1,800
Sustaining Labor[1]	5,000	–	–	5,000
Subtotal	$ 15,500	$ 2,580	$ 1,720	$ 19,800
Direct Materials (For 1,000 Sustaining Wafers)	$ 21,520	–	–	$ 21,520
Capital Cost	50,144	5,117	9,983	65,244
Total	$122,464	$13,337	$15,463	$151,264

[1] Labor to process 1,000 test wafers/month

Source: DATAQUEST, Inc.

per wafer cost of $300,000/4,920 or $60.97.

Table 3.8-5 shows the volume-sensitive or "variable" costs for the old and new lines. Here it can be seen that most material costs are roughly comparable. The silicon wafer cost is increased because of the shift from 3-inch to 4-inch wafers. Mask cost becomes almost negligible, even though individual masks are more expensive, because the masks used in projection printers do not wear out. They have to be removed and cleaned occasionally, but otherwise there is no wear. Some users have obtained as many as 100,000 alignments on a given mask set. In practice, most mask sets probably become obsolete because design changes are made before they wear out. We have assumed that the cost of design changes would not be a part of direct product cost. The chemicals cost is increased because the new 8-layer process requires more processing than does the old 5-layer process. All wafers are costed in the same manner even though the 4,000 wafers per

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Table 3.8-5

VOLUME SENSITIVE COSTS ("VARIABLE")

	Old Product Line	New Product Line
Wafer Fabrication (Costs/Wafer)		
Material Costs (Per Good Wafer)		
Silicon Wafer[1]	$10.00	$15.71
Masks	5.35	.05
Chemicals	2.25	4.10
Indirect (Quartz, smocks, etc.)	2.50	2.50
Gas	.50	.10[2]
Water	.60	.20
Rent	.50	Fixed Cost
Subtotal	$21.70	$22.66
Labor	5.83	7.57
Total	$27.53	$30.23
Wafer Sort (costs per unit)		
Material	$.0002	$.0001[3]
Labor	.0047	.0032
Total	$.0049	$.0033
Final Test		
Material	$.002	$.0001[3]
Labor	.043	0.0270
Total	$.045	0.0271

[1] The old line was for 3 inch wafers which cost $7.00 and had 70% fabrication yield. The new wafers cost $11.00 and have 70% fabrication yield.
[2] Part of gas cost has been transferred to recurring expense.
[3] New cost excludes rent.

Source: DATAQUEST, Inc.

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month used for the 4K RAM still only use five mask steps. Gas, water, and rent appear to be reduced because a portion of the cost has been transferred to "fixed" cost. Wafer sort and final test costs are essentially unchanged, except that labor costs have been reduced to reflect reduced test times resulting from improvements in test programs that decrease throughput time.

Table 3.8-6 shows the capital investment in various parts of the new line. These costs are taken from Tables 3.8-13 through 3.8-16 of the next subsection. The depreciation in Table 3.8-6 is on a five-year straight-line basis.

Labor Estimates

Labor estimates for the diffusion and fabrication areas are provided in Tables 3.8-7 and 3.8-8. These labor costs are computed on a per unit basis and used in Table 3.8-5.

PLANT DESIGN

This section describes the new 8-mask process, indicating the area in the wafer fabrication room in which each step is performed as well as the equipment used to accomplish the processing. The throughput rates are then given, and the equipment count is selected so that the line is "balanced" and the equipment cost is then totaled.

Process Flow

The process implemented in our new line is illustrated in Figure 3.8-3. While this process is reasonably up-to-date, it is expected that competitive conditions may force important changes within the year. The first is the addition of a second poly layer so that 16K RAMs can be built. The second is the addition of what is known as a coplanox process. This technique uses silicon nitride deposition in the early

Table 3.8-6

CAPITAL INVESTMENT

Category	Fabrication	Test		Total
		Sort	Final	
Equipment				
Diffusion	$ 307,820	–	–	$ 307,820
Masking	2,139,720	–	–	2,139,720
Deposition	381,070	–	–	381,070
Test	–	$307,000	$599,000	906,000
Subtotal	$2,828,610	$307,000	$599,000	$3,734,610
Leasehold Improvements	180,000	–	–	180,000
Total	$3,008,610	$307,000	$599,000	$3,914,610
Monthly Depreciation (5 years straight line)	$ 50,144	$ 5,117	$ 9,983	$ 65,244

Source: DATAQUEST, Inc.

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Table 3.8-7

WAFER FAB LABOR COSTS
(One Shift - 10,000 Wafers/Mo. Out of Fabrication)

Process/Task	Annual Salary	Number of Personnel Required	Total Cost (Annual)
Direct Labor Costs			
Masking Area			
Coat and Dry		1	
Develop and Bake		1	
Align		8	
In-Process Inspection		6	
Etch and Clean		5	
Final Inspection		6	
Mask Dispense		1	
Subtotal	$ 7,900	28	$221,200
Deposition Area			
Ion Implant		2	
Oxide Deposition		4	
Metal Deposition		2	
Glass Deposition		2	
Subtotal	$ 7,900	10	$ 79,000
Diffusion Area	$ 7,900	7	$ 55,300
Total Direct Labor		45	$355,500
Indirect and Support Labor			
QA Operators	$ 8,000	2	$ 16,000
Technicians	$10,000	10	100,000
Foremen	$18,000	4	72,000
Process Engineers	$25,000	4	100,000
Maintenance	$15,000	6	90,000
Production Control	$12,000	3	36,000
Total Indirect and Support Labor		29	$414,000
Total Labor			$769,500
Fringe Benefits (18%)			$138,510
Total Annual Cost			$908,010
Monthly Cost			$ 75,668
Cost Per Wafer ($75,668÷ 10,000 Wafers)			$ 7.57

Source: DATAQUEST, Inc.

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Table 3.8-8

TESTING LABOR COSTS
(4K RAM Only)

Personnel	Annual Salary	Number of Personnel Required	Total Cost (Annual)
Wafer Sort			
Direct Labor (Operators)	$ 7,900	4.0	$ 31,600
Indirect and Support Labor			
QA Operators	$ 8,000	0.5	$ 4,000
Technicians	$10,000	0.5	5,000
Engineers	$25,000	0.2	5,000
Maintenance	$15,000	0.5	7,500
Production Control	$12,000	0.3	3,600
Total Indirect and Support Labor		2.0	$ 25,100
Total Labor			$ 56,700
Fringe Benefits (18%)			$ 10,200
Total Annual Cost			$ 66,900
Monthly Cost			$ 5,575
Cost Per Unit (5,575 ÷ 1,760,000 Units)			$ 0.0032
Final Test			
Direct Labor (Operators)	$ 7,900	12	$ 94,800
Indirect and Support Labor			
QA Operators	$ 8,000	1.0	$ 8,000
Technicians	$10,000	1.0	10,000
Foremen	$18,000	1.0	18,000
Engineers	$25,000	0.5	12,500
Maintenance	$15,000	0.5	7,500
Production Control	$12,000	1.0	12,000
Total Indirect and Support Labor		5.0	$ 68,000
Total Labor			$162,800
Fringe Benfits (18%)			$ 29,304
Total Annual Cost			$192,104
Monthly Cost			$ 16,008
Cost Per Unit ($16,008 ÷ 598,400 Units)			$ 0.027

Source: DATAQUEST, Inc.

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process stages to help keep the surface of the wafer more even.

Figure 3.8-3 shows cross-sectional drawings for the major steps of an 8-mask N-Channel silicon gate process. This process varies from the older process of Figure 3.1-3 in that steps 2, 5, and 6 are added corresponding to first, third, and fourth mask, respectively. If the older 4K RAM is still produced, the production flow is altered so that steps 2, 5, and 6 are skipped.

Step 1 is somewhat changed in that the initial oxide does not have to be grown so thickly because there is a field implant in step 2. This dopes the surface of the silicon where there is no MOS device. The heavier surface concentration makes it possible to obtain high field thresholds with higher starting resistivities and to work with somewhat thinner field oxides.

Step 5 is a second implant step to allow creation of depletion-type load devices. The use of these devices eliminates one power supply and speeds the circuit up somewhat. Note that the implantation is actually made through the thin gate oxide.

Step 6 removes oxide in regions where contact between polysilicon and silicon is desired. Note in step 6 that this metalless contact is made when the poly is deposited. Note also in step 8 that the phosphorous deposition is made through the poly material, which is possible because the poly material is relatively thin and because phosphorous diffuses more rapidly through polysilicon than through crystalline silicon.

Step 11 varies in that a combination of aluminum and silicon is deposited, rather than aluminum, and step 12 substitutes silicon nitride for the vapox glass used previously. (Silicon nitride offers more protection to the device than vapox and is generally preferred.)

Table 3.8-9 lists each process step and shows in which room it occurs as well as the type of equipment used to perform the step. Here each masking operation is counted as one step, although in reality each masking operation requires the steps of scrub/bake/coat and bake/align/develop/bake illustrated in Figure 3.8-2. There are actually 47 steps when each masking operation is counted as a single step. Here, a step is taken to mean any point in the process flow at which there is an in-process inventory.

Line Balance

Tables 3.8-10 through 3.8-13 show the equipment balance charts for the diffusion, masking, deposition, and test rooms. In all of these charts, the throughput rate has been assumed to be 100 wafers per hour at each process step. This figure corresponds to a reasonable average projection aligner throughput rate. By and large, equipment has been selected to reflect a "straight-through" process flow; in other words, an effort has been made to avoid implementing several process steps on the same piece of equipment. Since there is one preclean station for each set of three diffusion tubes, some sharing of preclean stations between the various process steps is necessary.

Table 3.8-10 shows the diffusion room equipment balance. A separate tube (or tubes) is used for each process step, so there is a "straight" flow. Since diffusion tubes come three to a furnace, a preclean station is positioned in front of each 3-high stack to allow the wafer to move directly from preclean to diffusion without entering the room atmosphere, lowering the possibility of contamination. In the case of batch processes, the equipment throughput is calculated from the process time. It is then multiplied by a factor of 0.8 to allow for equipment downtime. Where cassettes are used, the throughput time cannot be derived from the process time. The number of pieces of equipment required is determined by adding

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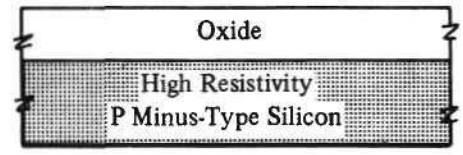
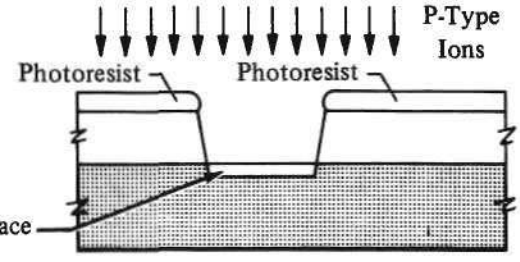
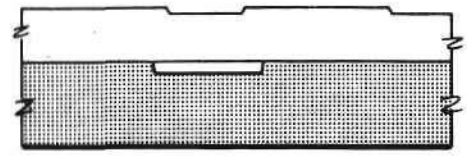
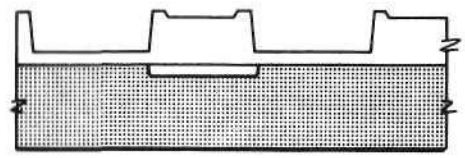
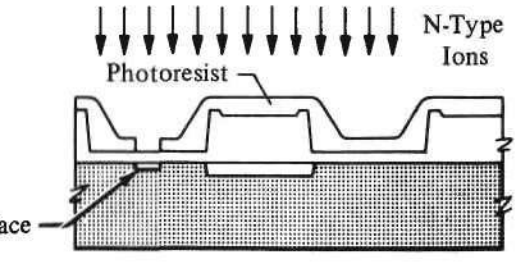
Figure 3.8-3

8 MASK N-CHANNEL SILICON GATE PROCESS

Process Step	Description	Cross-Section
1. Preclean Initial Oxidation	Silicon wafer is cleaned. Oxide is grown in high temperature furnace.	
2. 1st Mask (Field Mask) Oxide Etch Field Implant	Masking defines the area outside of active devices where the surface concentration is to be increased.	
3. Field Reoxidation	Oxide is regrown in a high temperature furnace.	
4. 2nd Mask Oxide Etch Gate Reoxidation	Masking opens the area where the MOS transistor will be formed. A thin gate oxide is then regrown in the area.	
5. 3rd Mask Depletion Implant (Note 1)	Masking defines the regions where depletion type devices are desired.	

Source: DATAQUEST, Inc.

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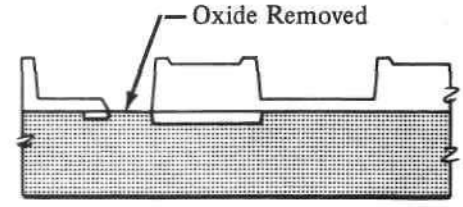
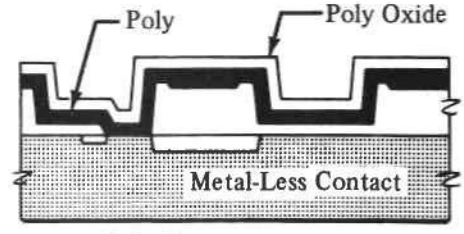
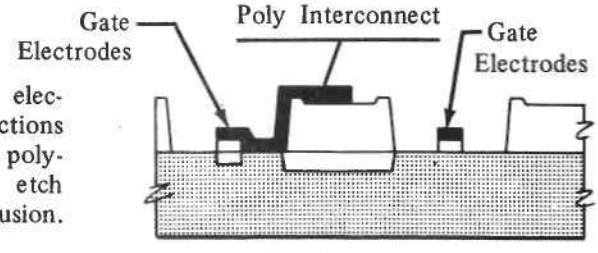
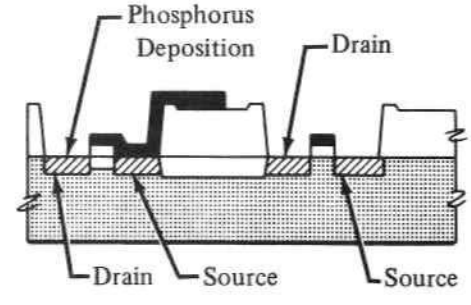
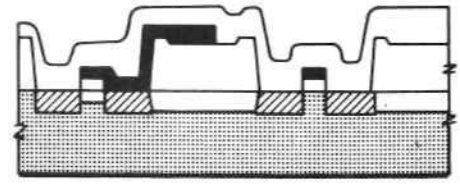
Figure 3.8-3 (Cont.)

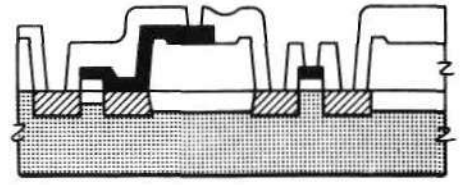
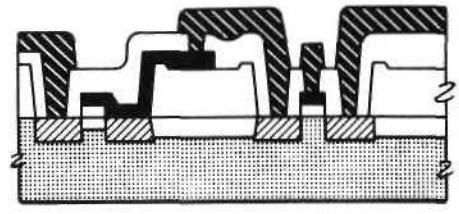
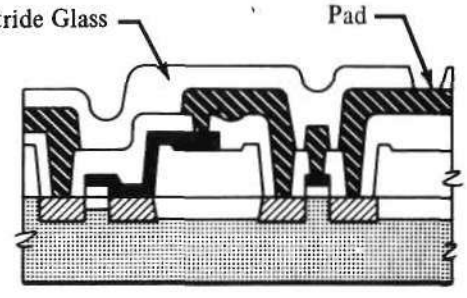
8 MASK N-CHANNEL SILICON GATE PROCESS

Process Step	Description	Cross-Section
6. 4th Mask (Metal-Less Contact) Oxide Etch	Masking defines the regions where contact between poly-silicon and silicon is desired.	
7. Poly Deposition Poly Oxidation	A thin layer of poly is deposited over the wafer in a hot-wall reactor. A thin oxide layer is then grown on the poly silicon in a high temperature furnace.	
8. 5th Mask Poly Oxide Etch Poly Etch Gate Oxide Etch	Masking delineates the gate electrodes and the poly interconnections through a selective etch of poly-silicon. A further oxide etch opens areas for the next diffusion.	
9. Phosphorus Deposition (Note 2)	Phosphorus is deposited to form the drain and source of the MOS transistor as well as any resistors or interconnects in silicon.	
10. Vapox Deposition (Field Oxide) Anneal	A thick layer of glass is deposited. It is annealed in a high temperature furnace which also completes diffusion of drain and source.	

Source: DATAQUEST, Inc.

Figure 3.8-3 (Cont.)

8 MASK N-CHANNEL SILICON GATE PROCESS

Process Step	Description	Cross-Section
11. 6th Mask (Contacts) Oxide Etch	Masking opens contacts to gates, drains sources and all interconnects.	
12. Aluminum-silicon Evaporation 7th Mask Metal Etch, Alloy (Note 3)	Aluminum-silicon is deposited on the wafer. Masking then selectively etches the material to delineate connections. A low temperature anneal (alloy) assures good contact to silicon.	
13. Nitride Deposition 8th Mask Pad Oxide Etch	Silicon nitride is deposited on top of the aluminum to protect it from contamination and scratches. Masking opens holes through the nitride so that contact can be made to the aluminum-silicon pads.	

Note 1: The ion implant for depletion-type devices is made through the thin gate oxide.

Note 2: Phosphorus deposition is made through the poly-silicon which overlies the source electrode. This is possible because of the thinness of the poly layer.

Note 3: Aluminum-silicon is used rather than aluminum to prevent alloying through the shallow N diffusions.

Source: DATAQUEST, Inc.

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Table 3.8-9

PROCESS SEQUENCE CHART

Location of Process Step			
Diffusion	Masking	Deposition	Equipment Used
1. Raw wafers			—
2. Preclean			Chemical sink + spray rinser/dryer
3. Initial oxidation			Diffusion tube + accessories
	4. First mask		Automated masking line
	5. Oxide etch		Chemical sink + spray rinser/dryer
		6. Field implant	ION implanter
	7. Plasma resist strip		Plasma stripper
8. Preclean			Chemical sink + spray rinser/dryer
9. Field reoxidation			Diffusion tube + accessories
	10. Second mask		Automated masking line
	11. Etch oxide		Chemical sink + spray rinser/dryer
	12. Strip photoresist		Chemical sink + spray rinser/dryer
13. Preclean			Chemical sink + spray rinser/dryer
14. Gate reoxidation			Diffusion tube + accessories
15. Pinhole inspection			Pinhole detector
	16. Third mask		Automated masking line
		17. Depletion implant	ION implanter
	18. Plasma resist strip		Plasma stripper
	19. Fourth mask		Automated masking line
	20. Etch oxide		Chemical sink + spray rinser/dryer
	21. Strip photoresist		Chemical sink + spray rinser/dryer
22. Preclean			Chemical sink + spray rinser/dryer
23. Poly deposition			Hot wall CVD system
24. Poly oxidation			Diffusion tube + accessories
	25. Fifth mask		Automated masking line
	26. Poly oxide etch		Chemical sink + spray rinser/dryer
	27. Plasma resist strip		Plasma stripper
	28. Poly etch		Chemical sink + spray rinser/dryer
	29. Gate oxide etch		Chemical sink + spray rinser/dryer
30. Preclean			Chemical sink + spray rinser/dryer
31. Phosporus deposition			Diffusion tube + accessories
		32. Vapox deposition	Oxide deposition system
33. Anneal			Diffusion tube + accessories
	34. Sixth mask		Automated masking line
	35. Oxide etch		Chemical sink + spray rinser/dryer
	36. Photoresist strip		Chemical sink + spray rinser/dryer
		37. Pre-metallization clean	Chemical sink + spray rinser/dryer
		38. Al-Si evaporation	Dual electron beam evaporator
	39. Seventh mask		Automated masking line
	40. Metal etch		Chemical sink + spray rinser/dryer
	41. Photoresist strip		Chemical sink + spray rinser/dryer
42. Preclean			Chemical sink + spray rinser/dryer
43. Alloy			Diffusion tube + accessories
		44. Nitride deposition	Nitride deposition system
	45. Eighth mask		Automated masking line
	46. Nitride etch		Chemical sink + spray rinser/dryer
	47. Plasma resist strip		Plasma stripper

Source: DATAQUEST, Inc.

3.8 Updated Manufacturing Model

Table 3.8-10

DIFFUSION ROOM EQUIPMENT BALANCE

Function	Process Step	Total Throughput Required (wafers/hr.)	Equipment Used	Process Time (Minutes)	Bath Size (Wafers)	Throughput (wafers/hr.)	Number Required
Initial oxidation	3	100	Diffusion tube + accessories	60	96	80	2
Field reoxidation	9	100	Diffusion tube + accessories	180	96	25	4
Gate reoxidation	14	100	Diffusion tube + accessories	45	96	106	1
Phosporous deposition	31	100	Diffusion tube + accessories	20	30	72	2
Poly oxidation	24	100	Diffusion tube + accessories	20	100	240	1
Anneal	33	100	Diffusion tube + accessories	20	100	240	1
Alloy	43	100	Diffusion tube + accessories	20	100	240	1
Poly deposition	23	100	Hot wall CVD system	45	100	106	1
							13
Preclean	2 8 13 22 30 42	480[1]	Chemical sink + spray rinser/dryer	10	100	480	5
Pinhole inspection	15	120	Pinhole detector		(Sample Only)		

[1] One preclean station is used for every 3 furnace tubes. The process steps in the 3 tube associated with a single preclean station are chosen so that the throughput need not exceed 480 wafers/hr.

Source: DATAQUEST, Inc.

3.8 Updated Manufacturing Model

Table 3.8-11

MASKING ROOM EQUIPMENT BALANCE
(120 Wafer per Hour Throughput)

Function	Process Steps	Total Throughput Required (wafers/hr.)	Equipment Used	Process Time (minutes)	Bath Size (wafers)	Throughput (wafers/hr.)	Number Required
Masking	4	100					
	10	100	Automated	5	25	400	1
	16	100	masking line		(cassette)		
	19	100					
	25	100					
	34	100	Automated	5	25	400	1
	39	100	masking line		(cassette)		
	45	100					
Oxide etch	5	100					
	11	100	Chemical sink	10	100	480	1
	20	100	+ spray				
	35	100	rinser/dryer				
Poly oxide etch	26	100	Chemical sink + spray rinser/dryer	10	100	480	1
Gate oxide etch	29	100	Chemical sink + spray rinser/dryer	10	100	480	1
Glass etch	46	100	Chemical sink + spray rinser/dryer	10	100	480	1
Plasma resist strip	7	100					
	18	100	Plasma stripper	10	100	480	1
	27	100					
	47	100					
Strip photoresist	12	100					
	21	100	Chemical sink	10	100	480	1
	36	100	+ spray				
	41	100	rinser/dryer				
Metal etch	40	100	Chemical sink + spray rinser/dryer	10	100	480	1

Source: DATAQUEST, Inc.

3.8 Updated Manufacturing Model

Table 3.8-12

DEPOSITION ROOM EQUIPMENT BALANCE

Function	Process Step	Total Throughput Required (wafers/hr.)	Equipment Used	Process Time (minutes)	Bath Size (wafers)	Throughput (wafers/hr.)	Number Required
Implant							
Field	6	100	ION	0.24	25	250	1
Depletion	17	100	Implanter		(cassette)		
Vapox deposition	32	100	Oxide deposition system	40.0	100	120	1
Plasma nitride	44	100	Plasma nitride deposition system	25.0	65	100	1
Aluminum/Silicon Evaporation	38	100	Dual Electron beam evaporator or induction evaporator	25.0	40	100	1
Pre-metallization clean	37	100	Chemical sink + spray rinser/dryer	10.0	100	480	1

Source: DATAQUEST, Inc.

3.8 Updated Manufacturing Model

Table 3.8-13

TEST AREA EQUIPMENT BALANCE
(Three-Shift Operation Assumed)

Function	Process Step	Total Throughput Required (wafers or units/hr.)	Equipment Used	Process Time (seconds)	Batch Size (wafers)	Throughput (wafers or units/hr.)	Number Required
Wafer Sort: (4,000 4K RAM wafers/mo., 6,000 other wafers/mo.)							
Wafer sort (for RAMs)	–	8.333	Automatic prober	550[1]	–	5.2	2
Wafer sort	–	12.5	Automatic prober	6[2]	–	10	2
Tester, wafer sort	–	–	Automatic tester	–	–	–	10 heads
Final Test: (598,400 4K RAMs/mo., 1,000,000 other products/mo.)							
Final test (2 shifts)	–	1973	Auto handler	10[3]	–	360	5
Final test (other products)	–	2,500	Auto handler	1[4]	–	1,000	3
Tester, final test	–	–	Automatic tester	–	–	–	4 heads

[1] Test time is assumed to be 1 1/4 seconds 1 die.
[2] Test time is assumed to be 1 second per die.
[3] Each 4K RAM is tested an averager of 1.5 times, including burn-in and sampling.
[4] Each other product is tested 1.1 times.

Source: DATAQUEST, Inc.

units until the number required multiplied by the actual throughput exceeds the required throughput. As can easily be seen from the figure, some stations have excess capacity simply because each piece of equipment has a different throughput rate; therefore, it is impossible to balance perfectly.

Table 3.8-11 shows the equipment balance for the masking room. As in the diffusion room, some process steps are shared on chemical sinks and on the plasma stripper. The additional chemical sinks shown are required because each may contain different chemicals, and it is generally not desirable to etch materials from different process steps in the same sink because cross-contamination may result.

Table 3.8-12 shows equipment balance for the deposition room. Here the ion-implanter is shared between two process steps.

Table 3.8-13 shows equipment balance for the test area. Note that a much shorter test time is assumed at wafer sort than final test,

partly because (1) 60 percent of the dice are unacceptable and the test program does not continue after one error is made, and (2) the wafer sort test is somewhat abbreviated. The abbreviated test is permissible because the device will be tested again at final test. The wafer sort test time is a compromise among test cost, packaging cost, and the cost of rejects at final test. In addition, some tests cannot be performed at wafer sort.

A wafer sort tester is no longer used. Formerly, this equipment was used to probe the test transistors to obtain data on process parameters. Now each die has a test pattern incorporated within it. The tester automatically tests the test pattern as it tests the die itself, and the data are automatically logged and analyzed.

Formerly, the wafer fabrication and wafer sort departments were prone to argue about whether a wafer should be accepted into wafer test based on the data obtained on the test transistors. These arguments cease when both tests are made on the same piece of equipment.

Equipment Lists

Equipment lists for the diffusion, masking, deposition, and test areas are given in Tables 3.8-14 through 3.8-17. These tables give the unit price for each piece of equipment. These prices are multiplied by the volume of equipment required as shown in the equipment balance lists of Tables 3.8-10 through 3.8-13. The resulting totals then have tax added and appear in the capital investment analysis of Table 3.8-6. Although we have listed several vendors for each piece of equipment, often other vendors also make the same equipment. Similarly, the costs shown are typical; they can vary considerably depending on the options selected.

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Table 3.8-14

EQUIPMENT LIST FOR DIFFUSION ROOM
(Dollars in Thousands)

Item	Cost Each	Number Required	Total Cost	Manufacturers
1. Furnaces, 3 per stack	$15.0	5	$75.0	Thermco, Lindberg
2. Diffusion tube accessories				
Furnace Load Stations	$ 2.5	8	$20.0	Envirco, Microaire
Automatic Boat Pullers[1]	1.5	15	22.5	HLS, CGI
Automatic Process System	2.5	15	37.5	CGI, HLS, Tylan
3. Hot wall CVD system				
(Excluding furnace tube)	$30.0	1	$30.0	Applied Materials
4. Chemical sink + spray rinser/dryer				
Chemical sink, 6 ft.	$ 3.5			Harrington Plastics
Spray rinser/dryer	2.5			Corotek, Flourocarbon, Kasper
	$ 6.0	5	$30.0	
5. Pinhole detector	$ 2.7	1	$ 2.7	Siltek
6. Laminar Flow Hoods for Chemical sinks	$ 2.5	5	$12.5	Envirco, Microaire, GCA
7. Process Monitoring Equipment				
Potentiometer	$ 2.0	1	$ 2.0	Doric, Leeds & Northrup
Optical Pyrometer	2.0	1	2.0	Leeds & Northrup
Thickness measuring system	9.0	1	9.0	Sloan
Microscopes	2.0	3	6.0	Leitz
4 Point probe	3.5	1	3.5	Signatone
C/V Plotter	6.0	1	6.0	MDC
Ellipsometer	5.0	1	5.0	Applied Materials
Angle Lap/Measurement Equipment	3.0	1	3.0	Signatone
			$36.5	
8. Maintenance Equipment				
Furnace tube washer	$ 3.0	1	$ 3.0	Harrington Plastics
Utility sink	1.8	1	1.8	Harrington Plastics
Drying ovens	1.5	1	1.5	Blue M
			$ 6.3	
9. Miscellaneous				
Dessicators	$ 0.3	8	$ 2.4	Precision Lab Products
Tables, chairs, cabinets			$17.4	
Total			$290.40	
Tax			17.42	
Grand total			$307.82	

[1] Automatic boat pullers are only used on the critical process steps.

Source: DATAQUEST, Inc.

3.8 Updated Manufacturing Model

Table 3.8-15

EQUIPMENT LIST FOR MASKING AREA

(Dollars in Thousands)

Item	Cost Each	Number Required	Total Cost	Manufacturers
1. Automatic Masking Line				
A. Prealignment				
Scrubber, 4 track	$ 19.0			GCA, Kasper, Cobilt
Baker, 4 track	19.0			
Coater, First track	20.0			
3 extra tracks	21.0			
Baker, 4 track	19.0			
Track sections	20.0			
4 track automatic indexer	25.0			
Programmable controller	20.0			
Subtotal	$163.0			
B. Alignment				
4 Projection aligners with 4" wafer capability improved light source and automatic loading @ $167.90	$671.50			Perkin-Elmer Kasper, Cobilt
C. Postalignment				
Developer, first track	$ 20.0			
3 extra tracks	21.0			GCA, Kasper, Cobilt
Baker, 4 track	19.0			Macronetics
4 Track automatic indexer	25.0			
Track sections	20.0			
Postalignment	$105.0			
Total	$939.50	2	$1,879.0	
2. Chemical Sinks				
Chemical sink, 6 ft.	$ 3.5			Harrington Plastics
Spray rinser/dryer	2.5			Corotek, Flourocarbon
Total	$ 6.0	6	$ 36.0	
3. Plasma stripper	$ 10.5	1	$ 10.5	LFE, Intenational Plasma, Tegal
4. Laminar flow hoods				
For Aligners	$ 5.6	8	$ 44.8	Envirco, Microaire, GCA
For Chemical Sinks	2.5	6	15.0	
For Inspection/Storage Stations	2.5	4	10.0	
			$ 69.8	
5. Miscellaneous Equipment				
Microscopes	$ 2.0	2	$ 4.0	Olympus, Leitz
Measuring Scope	5.0	1	5.0	Vickers Instrument
Dessicators	0.2	15	3.0	Precision Lab Products
Mask Storage Cabinets	0.2	4	0.8	Precision Lab Products
Temp/Humidity Monitor	0.1	1	0.5	Van Waters and Rogers
Cabinets, Tables, Chairs			10.0	
			$ 23.3	
Total Masking Area Cost			$2,018.60	
Tax			121.12	
Grand total			$2,139.72	

Source: DATAQUEST, Inc.

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Table 3.8-16

EQUIPMENT LIST FOR DEPOSITION AREA
(Dollars in Thousands)

Item	Cost Each	Number Required	Total Cost	Manufacturers
1. Ion Implanter	$160	1	$160	Varian-Extrion, Accelerators, Inc., GCA, Kasper
2. Oxide Deposition System	$ 34	1	$ 34	Applied Materials, Pacific Western
3. Plasma Nitride Deposition System	$ 60	1	$ 60	Applied Materials, Pacific Western
4. Dual Electron Beam Evaporator or Induction Evaporator	$ 75	1	$ 75	Airco Temescal, Varian/NCR Applied Materials
5. Chemical Sink + Spray Rinser/Dryer				
Chemical Sink, 6 ft.	$ 3.5			Harrington Plastics
Spray Rinser/Dryer	2.5			Coritek, Flourocarbon, Kasper
	$ 6.0	1	$ 6.0	
6. Laminar Flow Hoods				
For Implanter	$ 2.5	1	$ 2.5	Envirco, Microaire, GCA
For Oxide Deposition	2.5	2	5.0	
For Electron Beam Evaporator	2.5	1	2.5	
For Chemical Sink	2.5	1	2.5	
			$ 12.5	
7. Process Monitoring Equipment				
H_2 Alarm System	$ 5.0	1	$ 5.0	
Evaporator Thickness Monitor	7.0	1	7.0	
			$ 12.0	
Total			$359.50	
Tax			21.57	
Grand total			$381.07	

Source: DATAQUEST, Inc.

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Table 3.8-17

EQUIPMENT LIST FOR TEST AREAS
(Dollars in Thousands)

Item	Cost Each	Number Required	Total Cost	Manufacturers
Wafer Sort				
Automatic Prober	$20	4	$ 80	Electroglas, Pacific Western
Tester, Wafer Sort	–	2 heads	210	Xincom (Fairchild), Tektronix, Teradyne, Macrodata
Total, Sort			$290	
Tax			17	
			$307	
Final Test				
Automatic Handler	$25	4	$100	Seimens
Tester, Final Test	–	4 heads	465	Xincom (Fairchild), Tektronix, Teradyne, Macrodata
Total, Final Test			$565	
Tax			34	
			$599	

Source: DATAQUEST, Inc.

3.9 Glossary

Bipolar—Having two carriers of electrical current, one positively charged and one negatively charged. This is in contrast to MOS transistors which only have one charge carrier (unipolar or one polarity).

Boat—Quartz wafer holder, 3 inches wide and up to 24 inches long for use in furnace processes. Parallel slots are cut in the quartz so that wafers can sit vertically in the boat.

CAD—Short for Computer Aided Design. In its most common form, a computer memory is filled with a theoretical model of the MOS transistor and the pertinent process and device parameters. The circuit designer can then use the computer to simulate the performance of sections of the circuit he is designing, so that he can optimize the design without building a hardware prototype first. It can also refer to computer aided layout design.

Fabrication Yield—Cumulative wafer fabrication yield—defined as the number of wafers out of the process divided by the number into the process times 100.

Cumulative Yield (Cum. Yield)—The product or multiplication of yields at every manufacturing step. For example, two manufacturing steps with 80 percent (.8) yield would have a cum. yield of 64 percent (.64).

Desiccators—Plexiglass storage boxes purged with a clean dry gas, such as nitrogen. Used to store work-in-process wafers to minimize contamination.

DI Water—Deionized water. High purity water in which all impurities having an electrical charge (ions) associated with them have been removed.

Die (plural,dice)—Individual integrated circuits (or transistors) separated from the original whole silicon wafer but not yet assembled in a package. They vary in size from 20 mils on a side to larger than 250 mils on a side. The number of dice on a 3 inch wafer may vary from tens to thousands.

DIP—Acronym for Dual-In-Line Package; usually referring to a package configuration in which the external pins are aligned in two parallel rows.

Dopant—Atoms such as phosphorus, boron, or arsenic which are diffused into silicon to create resistors, diodes, and transistors.

Fab—Short for wafer fabrication.

FET—Acronym for field effect transistor. The FET is a transistor whose electrical characteristics are varied by the modulation of an applied electric field across its controlling electrode.

I.C. (IC)—Short for Integrated Circuit.

Junction—The boundary formed by the diffusion of a dopant which produces an excess of negative (positive) charges into an area of silicon having a dopant producing an excess of positive (negative) charges. At this boundary, the two dopant concentrations are equal.

Jungle—The gas control units used to regulate the flow and mixture of gases into furnace tubes.

Laminar Flow—Refers to the "clear air" systems (such as laminar flow hoods or benches) in which the filtered air has a streamlined flow, as opposed to turbulent flow.

Masks, Hard Surface—Photomasks whose patterns are made of chrome or iron oxide, both of which are tougher or harder than the standard

3.9 Glossary

emulsion patterns. These masks are more scratch resistant and last longer, but are more costly.

Micron—One-millionth of a meter, or about forty-millionths of an inch (0.000040 inches).

Mil—One-thousandth of an inch (0.001 inches) or about 25.4 microns.

M.O.S. (MOS)—Acronym for metal-oxide-semiconductor. In present applications, the semiconductor is silicon. The MOS structure forms the controlling electrode of this type of transistor and consists of a sandwich of metal, oxide, and silicon.

MOS Transistor—A device having an MOS controlling electrode, with a total of three electrodes, typically: Source (source of electrical carriers); drain (collects the carriers emitted by the source); and gate (controls or "gates" the amount of carriers flowing from the source to the drain).

N-channel MOS—A device in which carriers of electrical current and the path (channel) in which they flow are negatively charged.

PC—Short for Production Control. This group schedules the flow of raw materials, work-in-process, and finished goods.

P-channel MOS—A device in which carriers of electrical current and the path (channel) in which they flow are positively charged.

Photomasks—2 1/2 x 2 1/2 to 4 x 4 glass plates, 60 mils thick, upon which are repeated patterns of a circuit layer or die. The patterns are of emulsion, chrome, or iron oxide.

Photoresist (resist)—An organic, viscous liquid which polymerizes (hardens) when exposed to ultraviolet light. A thin film is applied to the wafer surface and the images on a photomask are reproduced in the resist.

Probes—Electrically conductive wires, resembling a straight pin in shape, which are used to contact the electrode pad on circuit die during wafer sort.

QA—Short for quality assurance. In a semiconductor operation, the QA group ensures that the product being produced meets the written specifications and guarantees.

QC—Short for quality control. This group is responsible for monitoring the quality of the product at each of the manufacturing steps.

RAM—Acronym for random access memory. A memory circuit which is organized such that any information location is accessible, without disturbing the information contained in any of the other memory locations.

Run—A batch of wafers, numbering from 5 to 50, which are processed through each process step together.

Silicon Gate MOS—MOS transistors which have a controlling electrode (gate) consisting of silicon instead of metal over the oxide.

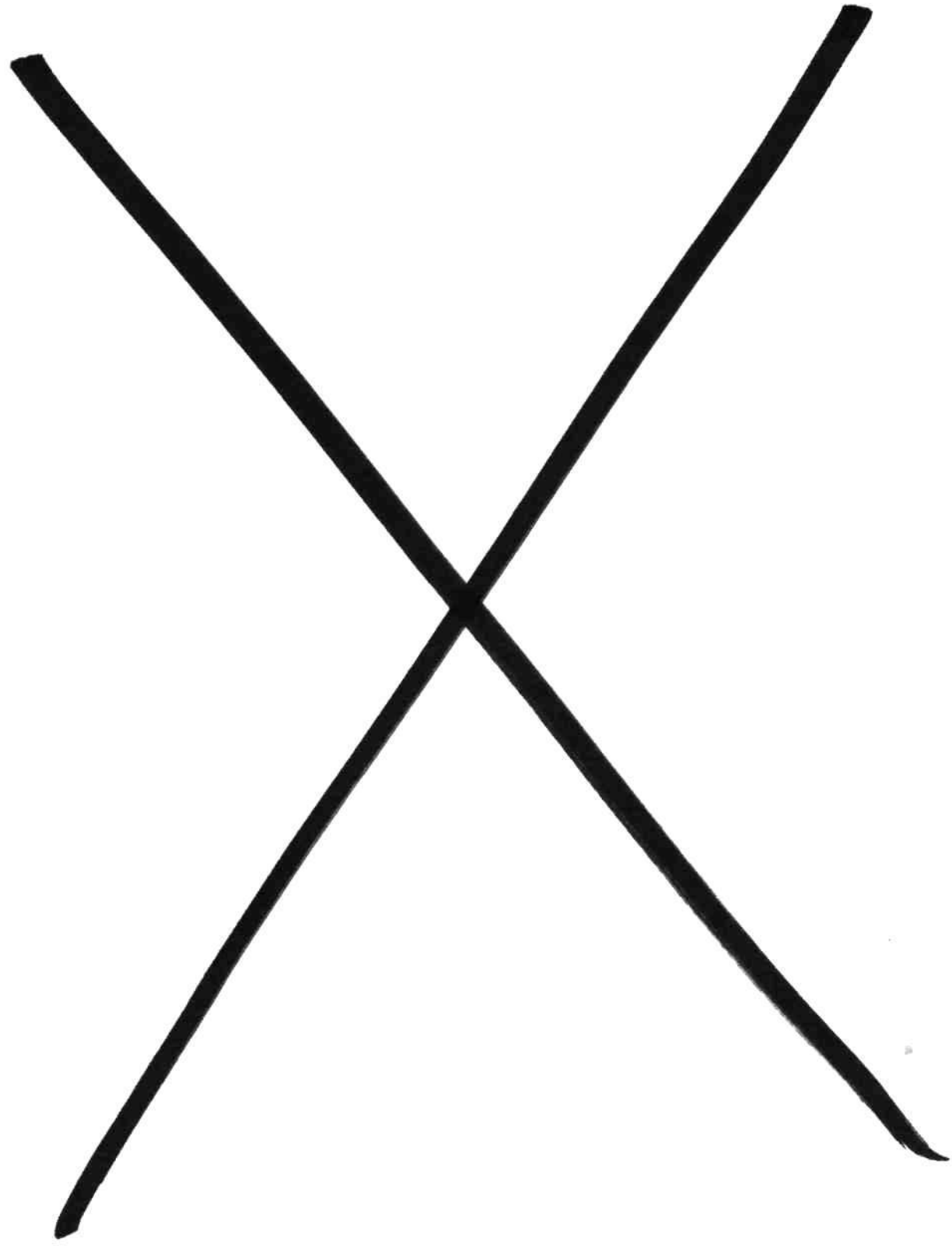
Susceptor—Graphite or carbon carrier, as large as 10" x 30", sometimes coated with a layer of silicon carbide, used to hold wafers for poly deposition. Wafers lie flat on this carrier, and energy from radio frequency waves heat up the carrier and wafers.

Vapox—Short for vapor deposited oxides, oxides that are deposited onto wafers by the decomposition of reactive gases (vapors) at low temperatures.

3.9 Glossary

VLF—Vertical Laminar Flow. Refers to hoods in which the filtered air flows downward to the work surface, in a laminar manner.

Wafers—Circular slices of silicon, 2 inches or 3 inches in diameter and 11 to 20 mils thick, used in the fabrication of integrated circuits.



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MANUFACTURING MODEL

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3.0 Manufacturing

INTRODUCTION

It is difficult to imagine any area of twentieth century life that will remain unaffected by the integrated circuit (IC). Some areas such as space travel, remote sensing, telephony, radio, ballistic missiles, and radar that were impossible without electronics have been made more reliable, faster, cheaper, and more accessible by the integrated circuit.

This chapter deals with the manufacture of integrated circuits; it was first written in 1975 and revised in 1977. This 1980 version will show major changes since then in technology and cost structure. As before, we discuss wafer manufacturing equipment. However, this chapter has a new section that covers plant facilities.

Costs are summarized and ratios given, both of which will offer some guidance. Terms which might be unfamiliar are, for the most part, defined in the text or will be listed in the appended Glossary.

THE SEMICONDUCTOR MARKET

Since the industry downturn in 1975, the demand for semiconductors, especially integrated circuits, has rebounded to a level that is difficult to satisfy with current manufacturing capacity worldwide. Although market segments and total consumption and shipment are fully detailed in Appendix A, some highlights will be mentioned here. The total growth in worldwide consumption for the five years ending in 1979 was 15 percent (compounded) for semiconductors and 23 percent for integrated circuits. Worldwide MOS memory consumption grew even more rapidly, achieving a 49 percent growth rate between 1977 and 1979. The year 1979 was particularly good because the average revenue per MOS wafer start increased an estimated 16 percent. It appears that 1980 will usher in a year in which worldwide semiconductor sales should exceed $12 billion.

North American consumption is between 38 percent and 39 percent of the total semiconductor market and approximately 45 percent of the total integrated circuit (IC) market. It appears that North American manufacturers have recently rapidly increased sales of microprocessors and related memory circuits. New users such as automotive, game, and telecommunications manufacturers have entered the market. The market is expected to show fairly steady growth over the next few years (see Appendix A, Volume II of the Semiconductor Industry Service notebook) while certain market segments will grow spectacularly.

3.0 Manufacturing

The competition has intensified for available manufacturing capacity and more and more independent merchant manufacturers have been purchased by semiconductor users. In addition, the number of captive manufacturers increased from 5 to 56 companies between 1955 and 1979. Since captive manufacturers serve only their internal market, there are many smaller companies with similar needs who have not been served because they cannot afford to build a wafer manufacturing facility. It is fair to say that most manufacturers have been operating at or near peak capacity, while expansion is being paced by long equipment delivery times, shortages of personnel, limited financing and other problems.

CURRENT TRENDS IN SEMICONDUCTOR MANUFACTURING

Significant changes are taking place in the way semiconductor plants are sited, constructed, equipped, and staffed. This section summarizes these changes and highlights important aspects of them.

Site Selection

A significant trend is the move away from the established semiconductor areas such as the Santa Clara Valley in California and the Houston-Dallas areas in Texas. In these areas, although job opportunities are still abundant, the wealth generated by the industry has forced up the price of available housing such that technical staff can ill afford it, limiting the incoming population flow. The price of real estate, for expansion of manufacturing facilities, has also risen sharply.

During the past five years, the established semiconductor manufacturers have looked elsewhere to begin new operations. New locations include Santa Cruz, Sacramento, Lodi, Santa Rosa, and Rancho Bernardo, California; Portland and Corvallis, Oregon; Orem and Salt Lake City, Utah; Austin and Carrollton, Texas; Colorado Springs, Colorado; and Vancouver, Washington.

What makes one location attractive and another not? The factors that enter such an equation are discussed below:

Electrical Power

The semiconductor industry is not tolerant of either brownouts or blackouts in which substantial material and dollar losses can be sustained. It would be intolerable to have to compete for power allocated on a quota system now that the industry is poised for aggressive growth.

Real Estate

Real estate must be available in abundance for present use and growth at reasonable prices. If the location is set in an area of fast economic growth, the expectation of investment appreciation adds to the attraction, both for firms locating in the area and for employees who anticipate appreciation in the value of their homes.

3.0 Manufacturing

Direct Labor Base

A preferred location would border on a large or growing population center. Demographic studies must therefore precede site selection.

Quality of Life

This term, quality of life, encompasses many of those abstract and physical qualities that make life agreeable and give people a feeling of well-being. In such an environment, people are free to pursue their desired lifestyles. Under the heading "quality of life" would come such things as climate, culture and entertainment opportunities (theatres, festivals, etc.), general standard of living, ambience (history, architecture), shopping, and sports (water, winter, traditional). Judicious site selection will result in the work force being attracted to such an area for more than the opportunity to earn a salary. As a corollary, if people are not offered a comparable or superior lifestyle, recruitment for that job market is more difficult. Professional semiconductor personnel are in short supply, and not inclined to move to undesirable locations.

Transportation

Proximity to a major airport and a major highway network is highly desirable. These two modes constitute major support systems for the industry to move products and equipment. Travel time to and from company headquarters is also important.

Housing

Housing has to be affordable and accessible. Lack of affordable housing has been a major drawback in attracting personnel to the Santa Clara Valley. Availability of housing close to the manufacturing site has the added virtues of energy and productivity savings.

City Services

Adequate water, sewage, roads, and other items are necessary.

Legislation

Both local and regional authorities must be sympathetic or at least not unreasonable concerning building codes, taxation, and environmental legislation. The locality must welcome new (light) industry.

Infrastructure

The proper infrastructure will offer tooling, gases, chemicals, and spare parts capabilities as well as maintenance services. Lack of adequate wafer fab equipment maintenance is a serious problem in many areas.

3.0 Manufacturing

A region already possessing some high technology industry will have available a labor force not unfamiliar with sophisticated equipment and processes. Such a labor force will consequently be more amenable to training in the particular disciplines of the semiconductor industry. Indeed, it is highly desirable for a small new company that is not wholly self-sufficient to have a semiconductor neighbor that can help out in emergencies.

Educational Institutions

Traditionally, semiconductor houses have located their operations near universities with topflight engineering and business schools, and all have benefitted from the proximity.

Junior colleges have provided valuable services by training operators and technicians in disciplines related to the industry.

The general labor force is also concerned about the education of their offspring; therefore, a preferred location should offer good elementary and preparatory schools.

Other Services

Motels, hotels, and restaurants provide necessary ancillary services. Mature areas are also able to offer convention facilities and exhibition sites.

Technology and Equipment

The trend toward greater device complexity (in excess of 130 kilobits of memory per device) and larger die size has been spurred on by lowered defect densities. As device geometries approach the 2 micron level and below, processing, environmental and equipment technologies must come together.

Of the many process technologies which have arisen, photolithography has been one of the key factors in determining the pace of Very Large Scale Integration (VLSI) design and manufacture. The trend has been away from contact printing toward proximity and projection printing.

Dry etching techniques are being developed as a necessary concomitant of projection printing in order to etch fine patterns in a variety of materials.

Ion implantation techniques have kept pace in order to achieve, quickly and inexpensively, control of impurity concentrations and junction depths.

Although complex and expensive, with increasing delivery times, related equipment is proving to be cost effective. The equipment is increasingly controlled electronically by the integrated circuits it fabricates. The result is greater automation, control, and reproducibility of results, as well as lower defect levels due to lower operator-wafer interfacing.

3.0 Manufacturing

The clean room facilities in 1980 are geared toward Class 100 rating rather than toward the Class 1000 rating that was acceptable until 1978.

Deionized (DI) water is being elaborately treated and tested to meet the new clean standards. The water is pretreated through activated carbon and diatomaceous earth filters before it goes through reverse osmosis and deionization stages.

Four-inch diameter wafers are expected to be the standard during the mid-1980s; larger wafers may be used for many standard memory lines. Thus, for a facility processing 10,000 wafers out per period, $40-80 per wafer to manufacture, and gross revenues of $300 to $600 per wafer, at least $3.0 million dollars per period can be realized.

At the same time, equipment purchases for today's use must nevertheless be chosen for eventual upgrading to handle 5-inch, and even 6-inch diameter wafers, as long as the particular technology will not be obsolete by the time of the upgrading. It is often possible to adapt machines to suit other products before those machines are no longer serviceable. With the high capital cost of some equipment, care must be taken to obtain maximum utilization of such equipment while it is in service.

Plant Layout and Design

Several factors determine the way in which a particular plant is laid out. The space allocated and the relationships among equipments are determined by:

- The technologies employed and the available equipment to realize them
- Line balance resulting from a particular product mix
- Resulting material and process flow
- The volume of product scheduled out per period
- The particular constraints imposed by city building codes which, in the main, are designed for operator safety

There are, however, other factors which are having a profound effect on the layout of today:

- Cleanliness for VLSI production is influencing what portion of the equipment remains in the clean room. Only the loading end of diffusion furnaces are being allowed in the clean room. The heat and dust generating portions are being separated from the clean room by a fire wall. The same is true for ion implanters and the trend will be continued for other equipment where appropriate.

- Servicing of equipment and work stations in old facility designs meant frequent ingress of personnel into the clean room to deliver bottles of chemicals, replace furnace tubes, and repair plumbing. New layouts obviate the necessity for these entries by pumping chemicals (except photoresist) to other points of use. Plumbing can be done outside the clean room if a service corridor rings the fabrication area. Furnace tubes can be pulled and replaced behind the fire wall and outside the clean room. If gases are pumped overhead through a crawl space, gas lines can often be serviced in these crawl spaces without need for entry into the clean room.

- Philosophies of equipment design have shifted toward single wafer and in-line processing and wafer handling, away from the purely batch-type handling. Thus, there is greater interplay between different processing areas (as opposed to the almost strict quarantine that existed before) as long as cleanliness is maintained, material flow facilitated, and cross-contamination avoided. New demands for material accountability have made production control supervision the heart of the entire operation and this fact has also affected the overall layout. Increased usage of computers and terminals will make this an even more effective approach.

Manufacturing

Increased pressure for production economies, higher productivity, device reliability and yield, and the stringent demands of complex fine geometry devices have resulted in several developing trends in circuits manufacturing.

Automation

Perhaps the most persistent and pervasive trend is that towards automatic sequencing of events. Also popular is the drive toward computer automation for control, reproducibility, data collection and analysis. The benefits to be reaped are legion and include:

- Less wafer handling
- Process monitoring and control
- Correct process sequencing
- Proper routing of material
- System self-diagnostics and self-correction
- Data collection for off-line processing
- Elimination of paper work

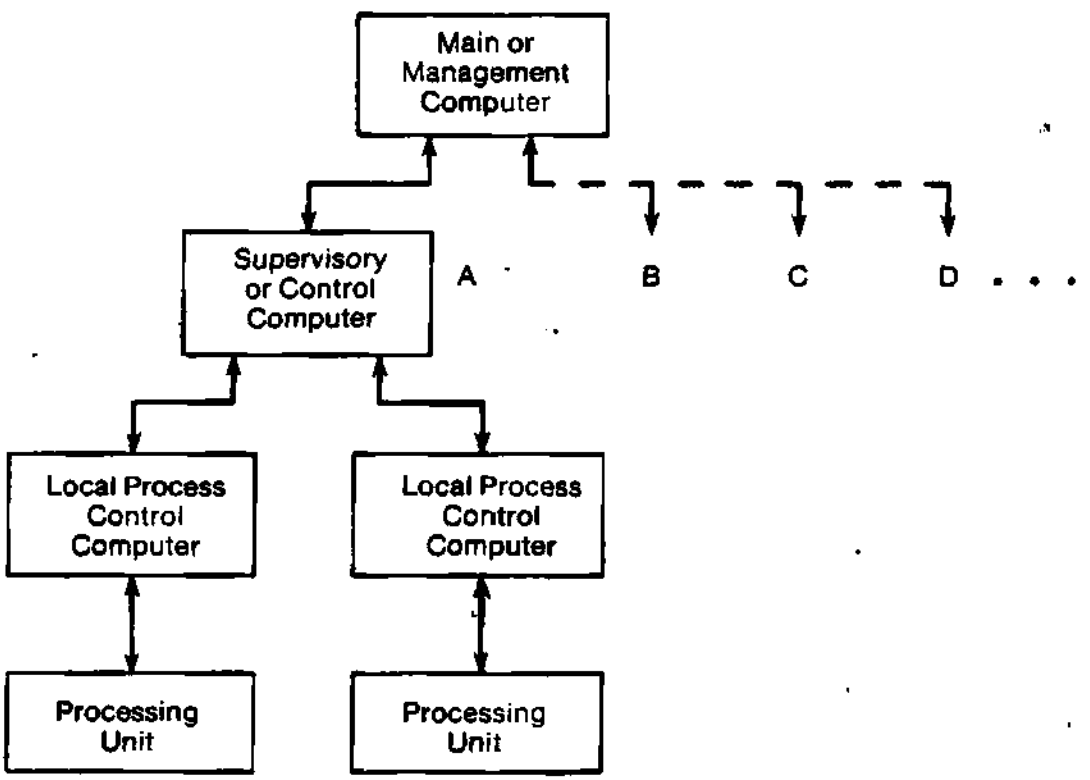
- Material accountability (especially useful since lot sizes vary for different operations in the manufacturing process)

Equipment manufacturers are following the trend toward automated equipment (some with micro and minicomputers) primarily because it is already available and on production lines. Some automation now exists in the areas of diffusion/oxidation, physical and chemical vapor deposition, ion implantation masking, alignment, mask making, mask inspection, testing, plasma etching, DI water, and environmental monitoring.

A fully computerized operation would have the hierarchy shown in Figure 3.0-1. The functions of the elements of such a hierarchy are shown in Figure 3.0-2.

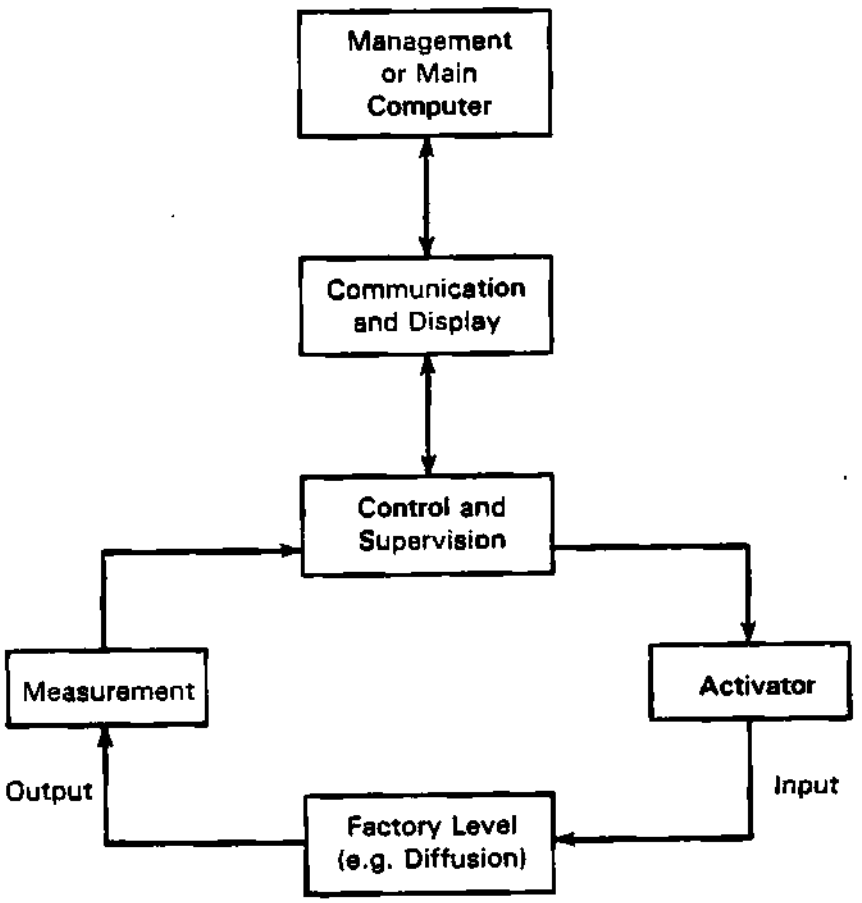
Figure 3.0-1

COMPUTER HIERARCHY



Source: DATAQUEST, Inc.

Figure 3.0-2
CLOSED-LOOP OPERATION



Source: DATAQUEST, Inc.

Variables which constitute the particular process at the factory level are sensed and measured. The supervisory element compares the measured data against set values and adjusts the system to initiate or shut down the process. Communication and display terminals are at the floor or factory level and through them data are transmitted to the highest level, the management computer.

Exciting as it is, the prospect of a fully computerized, semiconductor manufacturing facility is not foreseen before the mid- to late-1980s, even though an experimental automated line has been constructed at Texas Instruments and automated production lines are used by several captive manufacturers. The determining

element is, of course, equipment development. Much of the equipment today is being "updated" by adding microprocessors for sequencing. However, very few pieces of equipment are designed around computer control with adequate supporting software. More and more companies have placed computer terminals in their manufacturing areas but these terminals are almost always to handle data rather than direct and control manufacturing processes.

The development cycle for very sophisticated equipment can range from two to five years. Delivery times of equipment costing above $200,000 often range from nine to eighteen months. Development costs are often high too, as is the rate of obsolescence. Consequently, only the wealthiest semiconductor manufacturers can undertake their own development programs toward full computerization of the factory. The rest must wait for market forces to react.

Cassette-to-Cassette Wafer Handling

Batch processing will probably never disappear in the forseeable future. However, more and more equipment manufacturers are offering cassette-to-cassette wafer systems to eliminate tweezer handling. Tweezers are a well-known cause of damaged patterns, silicon particle generation, and wafer defects. In properly controlled equipment, each wafer is subject to almost the same set of process parameters.

Energy and Resources Conservation

Manufacturers are implementing the following operations to conserve both energy and other resources:

- Diffusion/oxidation furnace temperatures are being ramped down to a lower holding temperature when not in use and at the end of high temperature processing. Not only does this practice conserve electrical energy but it also helps to avoid silicon crystal damage.

- Deionized water is being reclaimed at great savings for the manufacturer and for society. Water for chilling is being stored for re-use.

- Organic chemicals are being collected after use and resold for reclamation.

- Plasma dry etching and stripping result in appreciable savings on chemical usage, estimated at one-half to one-third of net processing costs. The technique also implies fewer process steps and floor space as well as being necessary, in the case of dry etching, to define small geometries in a variety of materials which have to be etched anisotropically to avoid undercutting.

- Projection printing results in considerable economies in mask costs whereas a mask used for contact printing can be used on 50-100 wafers before being discarded. A repaired chrome master, starting out with defect levels of

approximately 1 defect/sq.in., can be used on up to 100,000 wafers with defect levels finally not much above the starting values. Since defects are known to be transmitted back and forth between mask and wafer during contact printing, higher device yields and reliability result from projection printing. Equipment costs are usually justifiable within about a year based on mask cost savings alone at current production levels.

Environmental Control

The manufacturing environment has now become the focus of intense monitoring and control procedures. Some measures have already been discussed under the heading Plant Layout and Design. Clean rooms are now being established as Class 100 and more care is now being taken with the room's ceiling materials, paint, tile composition, material flow, personnel movement, and gear. "Bunny Suits" expose the wearer's face and hands only, and plastic booties are also becoming the standard. Operators (perhaps the primary source of contamination) access the production floor by passing through air showers. Air-handling units must be adequate to provide more positive pressurization in the areas most sensitive to contamination. The return air ducts must be sized and spaced to avoid noise and turbulence and then smoke-tested for assurance.

The logistics of janitorial training and service are being addressed with greater care, while hoods and sinks are being designed consonant with janitorial service. Wafers are stored in clean boxes on wire mesh racks under laminar flow hoods fitted with ion generators.

Much of the new equipment is highly sensitive to temperature, while many processes already sensitive to humidity are becoming more so to particulate contamination. The monitor and control of these aspects of manufacturing are becoming of utmost importance to manufacturing managers concerned about high yields. Sensors are located strategically around the production floor, and readouts are sometimes done on computer terminals.

External to the production area, the normal work environment has been a subject of continuing concern. Social, as well as economic pressures have blended toward a common goal of limiting the amount of chemical effluents, both liquid and gaseous, which are discharged into the environment. Thus, dry processing, computer-controlled dispensers of minimal amounts of chemicals required for a particular process, and energy resources conservation are all part of the continuing program to preserve the living environment.

Human Engineering

This facet of manufacturing addresses operator safety and health. Although some aspects are legislated, optimization often results in higher productivity. More care is being taken to detect and reduce acid and solvent fume levels. Colors of equipment, walls, and floors, are being chosen to keep operators comfortable and productive. Noise levels are difficult to reduce in equipment and air handling units, except by design. High noise levels are known to reduce productivity in the short term and to affect operators adversely in the long term.

Another aspect being more closely studied is the velocity of air flowing past the operator. Too rapid a flow of air is not only unhealthy for the operator, but also results in turbulent dissemination of particulates around the room.

Staffing

The cumulative effects of the recessions of 1970 and 1974 are now evident in the acute shortage of trained engineering staff. The trend of decreased enrollment in engineering colleges since these recessionary periods has not been reversed at rates compatible with industry growth. For those engineers who remained, it has become a sellers' market. In Santa Clara (Silicon) Valley, California, unemployment at 4.7 percent in September 1979 was at a five-year low, unparalleled anywhere in the country. At the lower end of the wage scale, turnover rates ranged from 50-100 percent among operators. (See Assumptions under "Manufacturing Model" for typical salaries and salary ranges). Although mothers of young children have rejoined the work force, the industry still faces severe labor shortages while professional personnel are being wooed by "headhunters," print, skywriting, radio, and television ads. Incentives and bounties are offered to staff already in place to ensure successful recruiting.

Housing costs, already prohibitive for engineering staff, are even more prohibitive for operators (see "Site Selection"). Commuting is only a partial solution to the problem of staffing expanding operations. The trend, therefore, has been to relocate new operations into more favorable labor markets, all other things being equal.

In any direct labor market, the overwhelming majority of labor available consists of women ranging from 18 to 35 years old, that is, in the prime childbearing range. It is not surprising, therefore, to hear of industrial park planners contemplating the establishment of nurseries right in the center of such parks.

3.0 Manufacturing

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3.1 Major Manufacturing Operations

INTRODUCTION

After a circuit designer has completed an integrated circuit design, there remains the challenge of translating these drawings of thousands of transistors, resistors, diodes, and capacitors into reality. This is the manufacturing or wafer fabrication process performed on elemental silicon to produce millions of identical integrated circuits all capable of performing the same complex functions for a given set of conditions. After electrical testing, the good "chips" or circuits are each isolated and packaged as individual units. Chip complexity has now reached the point where it is feasible to create a single chip capable of all the functions of a complete computer.

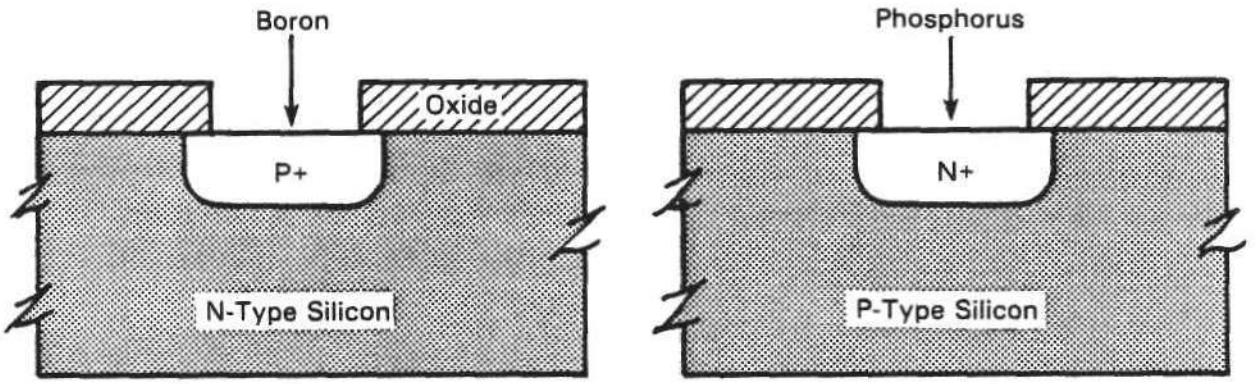
SEMICONDUCTORS, P-N JUNCTIONS, AND TRANSISTORS

To understand the manufacturing process, it is useful to see what materials and devices are being used and why. Materials like wood and glass are insulators (or non-conductors of electricity). On the other hand, metals (e.g., silver or aluminum) are excellent conductors of electricity. Silicon is categorized midway between conductors and insulators, hence, the name semiconductor. The characteristic of paramount interest is the ability of silicon to alter its electrical conductivity. It does so with the introduction into the crystal of impurities ("dopants") of suitable type and in suitable amounts. If boron is introduced, the silicon is doped p-type indicating a region of positive charge due to a deficiency of electrons. Conversely, phosphorus will dope silicon "n-type" by creating a region of negative charge. Thus, if boron is introduced into n-type silicon (or phosphorus into p-type silicon), a p-n junction is formed as illustrated in Figure 3.1-1. (Note: p+ = heavily doped p-type; n+ = heavily doped n-type silicon).

By suitable juxtaposition of p-n junctions and application of appropriate biasing voltages, a transistor can be created. Figure 3.1-2 shows the cross section of an MOS transistor. A positive voltage applied to the gate causes the p-type silicon underneath the gate oxide to form an n-type channel which connects the two n+ regions. A small positive voltage applied to the drain causes a current of electrons to flow or transit from the source to the drain. Hence, the name transi(s)tor;the extra "s" is included for euphony. This transistor is called an n-channel metal-oxide-silicon (MOS) transistor and behaves like a switch. The earlier gates were metal (typically aluminum) but nowadays, heavily doped (n+) polysilicon is used instead.

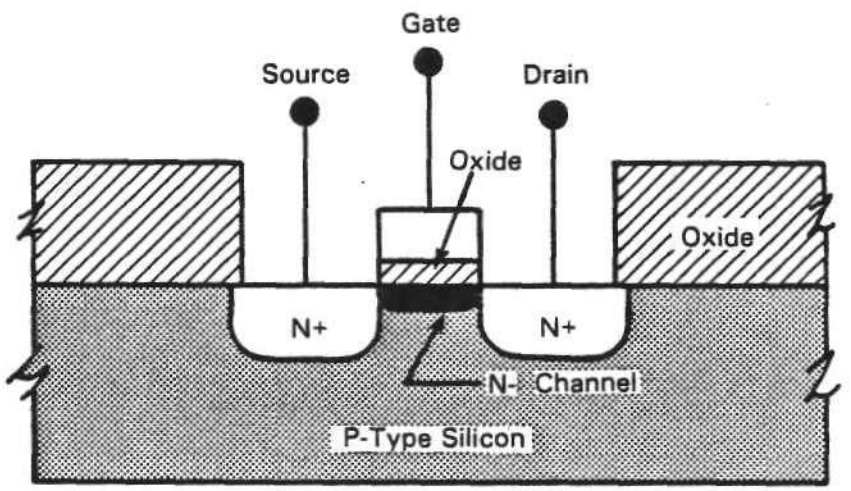
3.1 Major Manufacturing Operations

Figure 3.1-1
P-N JUNCTIONS



Source: DATAQUEST, Inc.

Figure 3.1-2
CROSS SECTION OF AN N-CHANNEL MOS TRANSISTOR



Source: DATAQUEST, Inc.

3.1 Major Manufacturing Operations

Other arrangements of p-n junctions result in bipolar transistors or junction field effect transistors (JFETs), and other types of transistors, diodes, and thyristors.

Oxide sandwiches behave like capacitors; isolated p-n junctions behave like diodes; and transistors themselves are often used as fixed or variable resistors or loads. A clever designer uses this entire arsenal to create very small, but extremely complex, integrated circuits. A chip merely two-tenths of an inch square often has as many as 20,000 transistors executing cycles of functions at speeds faster than one millionth of a second.

THE MANUFACTURING PROCESS (THE PLANAR PROCESS)

General

Almost universally, semiconductor manufacturers use the planar process in which these circuits are fabricated one layer at a time. (The closest parallel one might invoke is the silk screening process.)

Batches of silicon wafers (3 or 4 inches in diameter and 14 to 20 thousandths of an inch thick) are oxidized in long furnace tubes full of dry or wet oxygen. The wafers are then coated with photoresist, a light sensitive liquified rubber which behaves like photographic film. A mask or plate, supporting tiny replicated metal or emulsion patterns on glass, is inserted between the photoresist-coated wafer and a source of (typically) ultraviolet (UV) light. If the mask is in contact with the wafer, this operation is called contact printing. Otherwise, the patterns on the mask may be projected on to the wafer. The resist (short for photoresist) polymerizes those areas of the wafer that actually receive UV light. Treatment of the wafer with a suitable organic solvent removes the unexposed resist by differential solubility. What remains is a "negative" image of the pattern on the mask; hundreds of these patterns are simultaneously etched into the oxide film prepared during the oxidation step described above. The polymerized resist protects the underlying oxide making possible pattern definition during oxide etching. After removal of the resist, the wafer may be implanted (see Ion Implantation) or diffused with dopant ions to create p-n junctions. This occurs only where the oxide has been removed. The patterning process is very grandly called photolithography (Greek: photos = light; lithos = stone (silicon); graphein = to write) and may be repeated nine times to define the required pattern at each layer. The penultimate pattern is usually a metallization or interconnect pattern which establishes the desired electrical relationships among all the elements of the integrated circuit. This method of processing integrated circuits is the "planar process."

After the final scratch protection layer is masked (short for photomasked) and etched, computerized electrical sorting of good and bad dice takes place. The bad dice (or circuits) are dotted with a magnetic ink and are magnetically removed when

the wafer is scribed or sectioned into individual die in the early assembly operations. The good dice are wired and packaged as individual sealed units in ceramic or plastic. Thereafter, these circuits communicate with the external world only through metal leads. After final environmental and electrical testing, the good units are sold to the users.

Process Requirements

A strand of human hair is between 1 and 2 mils thick. One mil is one-thousandth of an inch, or 25.4 microns. The lines and spaces defined routinely today in chip manufacture are between 4 and 5 microns. Some specialized circuits for very high speed devices in very limited production employ 1 micron lines and spaces. In addition, most devices are affected by ionic contamination. Hence, the following general needs must be met:

- Precise environmental control of particulates, temperature, and humidity
- Very high purity deionized (DI) water, gases, and chemicals
- Manufacturing equipment with very high precision and control for reproducibility
- Careful design of the part to be manufactured
- Well-trained labor and engineering to reproduce faithfully and in proper sequence the hundreds of operations that constitute circuit manufacturing

MAJOR FAB OPERATIONS

The terms wafer fabrication area, wafer fab, or fab, will be used interchangeably and will refer to that part of the factory where diffusion/oxidation, ion implantation, thin film deposition, and photomasking operations occur. In general, it is the area in which the raw silicon wafer is transformed into thousands of integrated circuits still on the wafer.

Oxidation

After subjection to hot corrosive acids which clean the wafer surface, particulate and soluble impurities are removed from the wafer surface in a final DI water rinse, and then dried. The wafers are loaded on edge in specially designed boats; the boats are then loaded into the oxidation furnace. The gas or gas mixture which constitutes the ambient are admitted at one end of the furnace tube, flow over the stacked wafers, and are exhausted at the other end. The spent gas(es) escape through a

"scavenger" or flue and are "scrubbed" with water to render the effluent harmless to the environment. Temperatures usually range between 900 to 1200°C. The ambient is either dry oxygen, oxygen and water vapor, nitrogen, or hydrogen burned in oxygen. The combination of time, temperature, and ambient will determine the thickness of the silicon dioxide produced. The oxide formed is the corrosion product of the reaction and is used, among other engineering purposes, to make capacitors, for "passivation" or protection of the underlying silicon and to define device patterns. The versatility of silicon dioxide is one of the major attractions of silicon technology.

Diffusion

What is diffusion? We have commented earlier on the need to make p-n junctions by introducing dopants (e.g., boron, phosphorous) into selected areas in the silicon. Imagine pouring red food coloring into a glass of clear cold water. Given enough time, the water would become uniformly pink. If hot water were used, the coloring would "diffuse" more rapidly. The same principle is used in semiconductor diffusion processes. In general, one establishes a concentration gradient (a local gradation of dopant content) and, given time and high temperatures, the dopant will further disperse itself into the host material (silicon). Usually, p-type dopants are introduced into n-type silicon and vice versa. There are, however, important situations in which p-type silicon needs to be made even more p-type (p+) and n-type silicon more n-type (n+).

The preparation for and the performance of the diffusion operation is almost identical to the oxidation operation. Results and purpose of the ambients, however, are far different. The dopant is introduced as a vapor into the diffusion tube usually with very small amounts of oxygen. Whether phosphorus (n-type dopant) or boron (p-type dopant) is to be introduced, the idea is usually to form a p-n junction.

The characteristics of a p-n junction—characteristics such as forward conductance and breakdown voltage are determined by the surface concentration of the doped silicon and the depth of the junction. Both these factors are controlled by the concentration of the dopant in the ambient gas during diffusion, the temperature, and the time of the diffusion.

Dopants are often introduced into oxides to perform functions such as "gettering" or passivation. This introduction is made possible by the production of a glass which is a combination of the dopant oxide and the silicon oxide. In the process of "gettering," impurities will be more soluble in the glass than in the silicon and, once the impurities have been gettered, they are removed when the glass is etched away.

Since several oxidation and diffusion processes occur during wafer fabrication, engineers have to calculate the cumulative effects of oxidations, diffusions, and etching steps on the final oxide thicknesses, junction depths, dopant profiles (concentration distributions in the vertical), and surface concentrations.

3.1 Major Manufacturing Operations

Ion Implantation

The silicon crystal is a regular array of silicon atoms with a known spatial relationship in an imaginary lattice. Foreign atoms can be introduced into this lattice by diffusion processes but they can also be "shot" in like bullets from a pistol. Like all other atoms, those of phosphorus or boron (the chief dopants) have electrons whizzing around their central core. If a negatively charged electron is stripped away, the atom then has net positive charge. This ion (charged particle) can be accelerated in a properly designed electric field so that it travels at tremendous velocities. Further, if a suitable magnetic field is deployed, that ion could be directed along a well-defined trajectory toward a specific target.

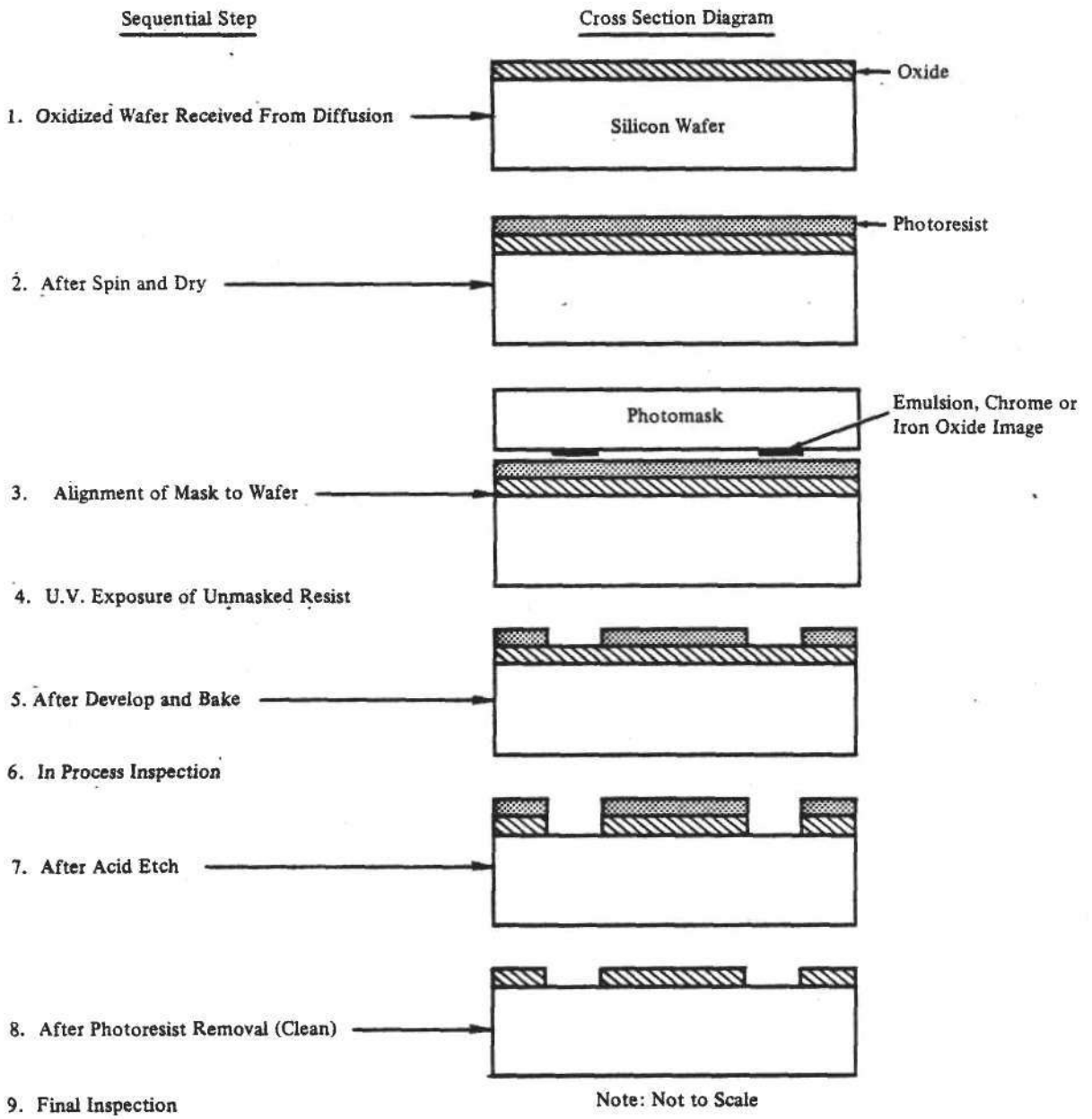
This activity is precisely what an ion implanter is designed to do; ion implantation is yet another technique that the semiconductor industry has developed and now takes for granted. The selected dopant ion is accelerated toward the silicon target and enters the silicon lattice in areas predetermined by photomasking. Among the many factors that determine the dopant profile (how much dopant will go where) in the silicon, the two main considerations seem to be the particular dopant atom and the power used to implant it.

This kind of battering disturbs the regularity of the silicon crystal and a layer of disordered (amorphous) material results. The crystal then has to be annealed to restore the original order to the lattice as well as to activate the implanted ion. Activation causes the dopant to exert its electrical characteristics. Most activation is executed at high temperature in a nitrogen ambient furnace. This process results in disturbance of the implanted dopant profile. In addition, the dopant can diffuse to form a p-n junction that is deeper than desired. A new technique without these disadvantages, employs a pulsed high-energy laser or electron beam. Ion implantation saves time (the process takes minutes, not hours), space, and money. It also offers considerably more control over p-n junction characteristics.

Photomasking (Masking)

The single area of semiconductor manufacturing most determinant of the industry's progress is masking. In the production of an integrated circuit, there may be from five to ten masking steps to define: areas to be implanted or diffused, capacitors, resistors, and metal interconnects. At any particular step in the fabrication of a particular circuit, a unique mask is called for. On 4-inch wafers, a 4-inch x 4-inch x 0.060-inch glass plate or photomask is used. This mask will usually carry a pattern replicated hundreds of times in chrome, iron oxide, or emulsion. These patterns must maintain their integrity throughout the mask making and photomasking processes. Any disruption of almost any portion of a pattern (either from scratching, smudging, or particulate contamination), whether on the mask or the silicon wafer, will render that circuit useless. Photomasking proceeds by this sequence (illustrated in Figure 3.1-3):

Figure 3.1-3
PHOTOMASKING PROCESS STEPS



Source: DATAQUEST, Inc.

3.1 Major Manufacturing Operations

1. Wafer Surface Preparation. This process consists of removing particulates and moisture to promote resist adhesion.

2. Spin-Coating With Resist, and Drying. The resist is nozzle-dispensed onto the wafer as it sits on a vacuum chuck. The resist is spread uniformly over the wafer surface at spin speeds typically between 3000 and 8000 revolutions per minute (rpm). The amount of resist dispersed and the spin speed employed usually determine the resist thickness. The resist is then hardened or "cured" to remove solvents by setting the wafers in a convection or infra-red oven.

3. Mask-to-Wafer Alignment. Since the resist film is light sensitive, the coated wafer is exposed to only filtered yellow light to which most "negative" resists are least sensitive. When the resist is dried (non-tacky), the appropriate photomask is placed between the UV source and the wafer and aligned to the previous patterns. Manufacturers are now beginning to acquire equipment that can perform this step automatically. Yield losses are often due to operator judgmental errors at this step.

   In contact printing, the wafer is actually in contact with the photomask and both wafer and mask may experience some damage in the process. Damaged masks have to be replaced while damaged circuit patterns result in circuit yield losses.

   Projection printing is rapidly replacing contact printing despite the high capital outlay for this equipment. Savings in the cost of mask replacement are tremendous and a single mask set has been known to survive a given product's lifetime in the marketplace. Device yields and reliability have been found to improve since in projection printing the mask is not in contact with the wafer; the image is simply projected onto the wafer.

4. UV Exposure. Once the alignment is deemed accurate, UV light is flashed over the mask for a few seconds, and the chemical processes (described above in The Manufacturing Process) take place.

5. Resist Development and Bake. If a "negative" photoresist is used, those areas of photoresist that were shielded by the mask pattern from the UV source will be soluble in the corresponding developer (solvent). Hence, the term "negative" resist (similar to the use of the word negative in standard photography). With positive resists, the converse is true.

   The developer itself must be rinsed away with another solvent since it would otherwise tend to be absorbed by the resist itself and the resultant swelling would distort the pattern.

   The bake step evaporates any remaining solvent and further hardens the polymerized resist to withstand subsequent etching operations.

6. In-Process Inspection. At this point, wafers are inspected for pattern integrity; at some layers, measurements of critical lines and spaces are taken. In this way, neither time, material, nor labor is further expended on unsuitable wafers. At this point wafers can usually be reprocessed through the masking step.

7. Etching. Up to this point, the required pattern has been defined only in the photoresist. To define the pattern in the underlying material (usually oxide), batches of wafers are immersed in an aqueous acid bath. Since the photoresist very largely protects the areas directly underneath, an almost 1:1 reproduction of the resist pattern is obtained in the underlying material. In this kind of wet etching, a pattern width designed to be 8 microns, for example, might turn out to be 6 or 7 microns at the surface and 8 microns where the film or oxide meets the underlying wafer. Etching proceeds horizontally as well as vertically since the chemical properties of the material are the same in all directions. The material is said to be isotropic (Greek: iso = equal; tropos = affinity for). This behavior in wet etches creates problems in VLSI circuits where designed geometries of 4 microns or less have to be held throughout the process for the circuit to perform predictably.

   A solution is Planar Plasma Etching, an emerging process. The developed wafers are laid face up in an atmosphere of reactant species (plasma). Both the plasma and reaction products are volatile and are drawn off during the process. The walls of etched patterns are straight (instead of sloped as with wet etching) since the etching occurs anisotropically (not isotropically). This, then, is the preferred etch technique for small designed patterns and is rapidly finding acceptance as a manufacturing process. The benefits gained are safety and control as well as savings in processing, time, and chemicals. Some fears remain, however, as to the effect, in some devices, on voltage control and stability.

8. Resist Removal. Hot, corrosive acids have traditionally been used to remove resist. The chosen solution must remove the resist and nothing else. Plasma techniques similar to those used for etching are currently finding favor. The benefits and fears are similar to those for etching.

9. Final Inspection. Before being sent on to the next process step, wafers are inspected again for detail such as pattern integrity, critical dimensions, and complete removal of photoresist. As patterns become smaller, the inspection process will become more significant.

In summary, as the industry seeks to gain more and more functions per unit area of silicon, the photomasking process determines this. In particular, mask making, alignment, pattern definition, and etching constitute the leading edge of technology for very small geometries.

3.1 Major Manufacturing Operations

Deposition Processes

Films may be formed either by chemical or physical vapor deposition. In Low Pressure Chemical Vapor Deposition (LPCVD) one gas may be decomposed or two or more gases made to react to produce the desired film. This film will be chemically different from all of the original or constituent material.

Most hotwall deposition systems are modifications of standard diffusion furnaces that include provisions for introduction of the necessary special deposition gases. They usually have a higher throughput (number of wafers processed in a given time) than other systems. In this type of loading, the wafers are made to stand on edge in slotted boats and are spaced 4 to 6 wafers per inch. Hot wall processes, since they usually occur above 400°C for periods in excess of one hour, are restricted to pre-metallization steps.

In physical vapor deposition (PVD), material is transferred from a source or target onto the wafer surface during the vapor phase. In both cases, the film is quickly grown at relatively low temperatures (350°C to 800°C). It may grow to any thicknesses desired, without affecting either previous dopant profiles (how much dopant is where) or junction depths. With the advent of Plasma-Enhanced Chemical Vapor Deposition (PECVD) techniques, films may be grown at lower temperatures (250°C to 450°C) using far lower volumes of reactant gases. Improved equipment design has tended to reduce hot surface areas (where unwanted films tend to deposit), turbulent gas flow, and deposits of particulates, while allowing for in situ cleaning of the apparatus. More automatic sequencing and minicomputer controls are also used, and there are corresponding increases in capital costs for this newer, more sophisticated equipment.

Chemical Vapor Deposition

Some examples of films deposited from the vapor phase are given below:

Vapox

Vapor deposited Oxide is normally deposited from mixtures of silane and oxygen diluted in nitrogen at about 450°C ± 25°C. In this way, the silicon wafer itself is not consumed to form this silicon oxide film. Typically, these films are used to either increase the oxide thickness in the inactive surface areas or to protect the metal interconnect patterns of the finished device against scratches. In new equipment, wafers are loaded on edge into diffusion-type furnaces to increase the number of wafers processed each cycle.

Vapox is a less dense, open-structure oxide but can be densified by high temperature treatment (900°C) in an inert atmosphere (e.g., nitrogen) to resemble thermally grown silicon dioxide in its physical properties. If the film is deposited in the presence of phosphine, for example, the resulting phosphorous oxide-silicon dioxide network tends to tie up ionic contamination (particularly sodium) which causes undesirable electrical behavior.

3.1 Major Manufacturing Operations

Poly

Polycrystalline silicon is formed by decomposition of silane or its derivatives. Like Vapox, it can be formed by CVD in a furnace tube or by PECVD in a "cookie sheet" type mode. If heavily doped with phosphorous (n+) during or after deposition, its electrical conductivity behaves like that of a metal. Whereas "single crystal" silicon shows the same order in the array of silicon atoms over large volumes of its lattice, poly does not. It behaves like randomly assembled chunks of "single crystal" silicon with an ordered lattice only over very small volumes of material. Hence, the name "polycrystalline" (Greek: poly = many) silicon.

While doped polysilicon is being used extensively as gate and interconnect material, there remains the problem of increasing its electrical conductivity to suitable levels for very small geometry devices.

Silicon Nitride

These films, too, are prepared by CVD and PECVD. The composition varies according to the parameters of the particular process. Its first and continuing use is to reduce the device's step heights over which metal lines run. High steps cause the metal to crack. Areas where active device elements are to be made are defined and protected from oxidation by the deposited nitride film. The exposed silicon in the field or inactive areas is oxidized to form very thick films of field oxide. When the remaining silicon nitride is removed, diodes, capacitors, and transistors are fabricated in those active areas as desired. The result is that, since part of the field oxide is "buried" in the silicon, the step heights from field to device are roughly half of what they would otherwise have been, and metal interconnects are less likely to crack over these steps. Trade names for this process vary from company to company and include COPLAMOS (Standard Microsystems), PLANOX (SGS-ATES), LOCMOS (Philips), and ISOPLANAR (Fairchild).

Silicon nitride is a good barrier against ions and moisture and is also scratch resistant; it is, therefore, used extensively to protect the finished device. PECVD films are prepared at low temperatures ($\sim 400^{\circ}C$) and show very little or no cracking to repeated cycling from $25^{\circ}C$ to $425^{\circ}C$.

EPI (Epitaxial Silicon)

If an ingot of single crystal silicon were sliced at different angles, each exposed face would have varying numbers of silicon atoms per unit of area (varying atomic density). Each face would be said to have a particular orientation. This is a useful, if simplistic, way of understanding silicon crystal orientation. At temperatures between $1000^{\circ}C$ and $1200^{\circ}C$, if silane or its derivatives in the vapor phase are decomposed at or near the surface of silicon with a particular orientation, the crystal grows along that particular axis or orientation. This is the process of epitaxy and the new silicon is called expitaxial silicon. If boron or phosphorous is introduced into the vapor during growth, the new material can be doped either p-type or n-type respectively during epitaxy. Bipolar transistors are made almost exclusively on epitaxial silicon. MOS transistors of very small geometries have been prepared successfully in epitaxial silicon to secure the precise control of dopant distribution required.

3.1 Major Manufacturing Operations

Physical Vapor Deposition

Metallization processes almost always employ physical vapor deposition techniques. The metal target may be converted to the vapor phase by resistance heating, electron beam evaporation, or sputtering. The silicon wafer to be coated is placed suitably in the path of the vapor which subsequently condenses to form the required film.

In resistance-heating processes, the heat is developed by the resistance of the target holder (or filament) to the passage of an electrical current. Where silicon-aluminum films have to be deposited, this technique is unsuitable because of the high melting point of silicon itself. Further, since the film composition is determined by the temperature of deposition, the resulting films would be unsuitable. Ionic content in resistance films has always been intolerably high since material from the walls of the bell-jar and fixturing tend to enter the reaction.

When electron beam (E-beam) techniques are used, a stream of high energy electrons is directed towards the target, commonly aluminum. Energy is given up to the target and, consequently, vaporizes it. Aluminum-silicon films are used for devices with shallow junctions so that the aluminum will not alloy through the device and short out the junction. Commonly, dual E-beam equipment is used for aluminum-silicon deposition.

When sputtering processes are used, a beam of high energy ions is directed at the target. These ions might be the nuclei of argon atoms. When they hit the target, they literally knock loose molecules of the target material. Sputtering processes have proved to be much more versatile since the composition of the target is maintained in the film. Film compositions are highly controllable and, since the target need not see ambient room air, contamination levels in the film and apparatus are low.

Backside Processing

There are several purposes served by processing the backside of wafers on which finished devices have already been fully processed. Among the most important are:

- Removing unwanted p-n junctions
- Thinning of the wafer so that the individual die will fit the cavity of the package
- Increasing the electrical conductivity of the backside of the device using ion implantation

The thinning process, and the removal of unwanted p-n junctions, are accomplished either by sandblasting (high pressure abrasion using "sand" particles) or by grinding on an abrasive pad. The Equipment List included in this report delineates total equipment required for backside processing by grinding. The device side of the wafer is protected in these operations both by the scratch protection films (oxide or

nitride) as well as by the photoresist film from the preceding masking process. "Sand" particles are removed by high pressure DI water scrubbing and photoresist is removed by plasma ashing.

Since too high a resistance to the passage of an electric current at the device backside results in spurious electrical behavior, it is often required to increase its electrical conductivity by increasing the doping level. Because the device has already been processed and the metallization should not undergo temperatures above 400° to 450°C for any appreciable period, the extra doping step is accomplished by ion implantation. This process can be effected at room temperature without disturbing p-n junction depths or profiles. A final alloying step activates the implanted dopant.

Further, a gold film is often required on the device backside to promote electrical conduction between the backside of the finished device and its package. When this gold film is applied to bipolar devices, it sometimes serves the added purpose of altering the electrical properties within the device by diffusion of the applied gold.

Many of the gold processes were introduced into the industry when the price of gold was $35 an ounce. With gold at about $600 an ounce, alternatives are being sought and gold recovery exercises are more important than ever.

PROCESS SPECIFICATION

Process Flow Chart

Many manufacturing facilities have a wide range of processes because of the differences in their products. Process flow charts are used to define a particular process. A process flow chart gives the sequence of operations that defines the process, references the specifications that define the manner in which the operation is to be performed, and delineates special instructions related to that operation. It is a basic technical document. The special instructions are needed since most operating specifications are used solely to define methods. The specific times, temperatures, gas flow rates (not shown on our example), etc., may vary from process to process even though the methods are the same. As a result, most companies find it expedient to write one general specification on methods and a process flow chart to fill in the specific information for a given process.

Table 3.1-1 illustrates a sample process flow chart of the kind used by many semiconductor companies. This chart summarizes the critical specifications and parameters defining a specific process flow and is necessary for quality control, consistency, and reliability in manufacturing.

The process represented here is called "N" and describes the process for an N-channel silicon gate 4K RAM. Other NMOS processes may be designated differently. Changes to this document can only occur by a written engineering change notice (ECN) or engineering change order (ECO), signed off and approved by the key engineering and manufacturing personnel.

3.1 Major Manufacturing Operations

Table 3.1-1
SAMPLE PROCESS FLOW CHART[1]

Process: N
Technology: N-channel, Silicon Gate

Division: MOS

Revision: A
ECN # : 306
Orig. : J. Doe
Date : 1-1-74

Operation	Spec. Ref.	Special Instructions
1. Raw Wafers	10001	3-4 ohm-cm, (100)-orientation
2. Initial Clean	20001	10 minutes
3. Initial Oxidation	20002	1150°C, 1 hr. 40 min., wet O_2, T_{ox} = 10,000A
4. Mask: P-Beds	30001-6,9	6 min. Buffered HF
5. Gate Oxidation	20003	1150°C, 40 min. dry O_2 + 15 min. dry N_2, T_{ox} = 1350A
6. Poly Deposition	20004	Thickness = 5000A ± 500A
7. Oxidation	20005	1100°C, 55 min., T_{ox} = 1200A
8. Mask: Gate	30001-5,7,9	
9. Phosphorus Deposition	20006	V/I = 1.0, 1075°C, $POCl_3$
10. Field Vapox Deposition	20007	9000A ± 1000A
11. Anneal	20008	1100°C, 20 min., dry N_2
12. Mask: Contacts	30001-6,9	
13. Aluminum Evaporation	20009	6-9's pure, 12,000A ± 1000A
14. Mask: Metal	30001-5,8	
15. Glass Deposition	20010	9000A ± 1000A
16. Mask: Pad	30001-6,9	
17. Alloy	20011	450°C, 30 min.
18. Wafer Evaluation	20012	V_{to} = 1.8 – 2.2V, $BV_{DSS} \geq 25V$, $V_{TM} \geq 25V$, $V_{TP} \geq 25V$

[1] For illustration only; not intended to describe a working process

Source: DATAQUEST, Inc.

3.1 Major Manufacturing Operations

Travelers

Wafer fabrication is often confusing to those not familar with semiconductor manufacture because of the large number of processing steps and the fact that the wafer does not travel a clear-cut path through the wafer fabrication area. Indeed, the wafer visits each area in wafer fabrication many times before all wafer fabrication processing is completed. Because a wafer fabrication area may have batches of wafers at different stages in processing, it is necessary to keep close track of each run or batch. For this reason, "run travelers" are used. The fab traveler is a card or sheet of paper that travels along with each batch of wafers through the wafer fabrication area. As illustrated in Table 3.1-2, it defines the photomask set and process to be used for a specific product.

There are also columns to log in the number of wafers received at a process step and the number out of the step, the operator's initials, date, and time. Not all companies require that the time be logged. Generally it is a good practice, however, since many problems are time-oriented.

Most travelers also force the operator to record specific data related to the process, such as equipment numbers, thicknesses, oxide colors, and critical dimensions (C.D.s—dimensions that must be held in the photomasking processes to ensure that the circuits will operate properly). These historical data are used to evaluate the consistency of a process and to track down problems that may arise.

In most cases, critical process information is not printed on the travelers for two reasons: (1) times, temperatures, and other variables may change over time, and it is far easier to change the flow charts and post the ECNs than it is to change each of the individual travelers; (2) one of the numerous travelers could easily get into the hands of a competitor.

3.1 Major Manufacturing Operations

Table 3.1-2
SAMPLE TRAVELER[1]

RUN. NO. _____ PROCESS_____
MASK SET NO._____ PRODUCT_____

Operation	In	Out	Date/Time	Operator	Spec. Instructions
Initial Clean					Standard Clean
Initial Oxidation					Fur.#____, 1150°C, wet O_2, 1 hr. 40 min., Color:_____
Mask: Bed					#____, CD = ____
Gate Oxidation					Fur.#____, 1150°C, 40 min., dry O_2 + 15 min., dry N_2,
Poly Deposition					Reactor #____, Thick.____
Oxidation					Fur.#____, 1100°C, 55 min.
Mask: Gate					#____, CD =_____
Etch Oxide					3 min. BHF
Clean					Sulfuric/Peroxide
Etch Poly					3 min. silicon etch
Etch Oxide					3 min. BHF
Phosphorus Deposition					Fur.#____, V/I =_____ 1075°C
Field Vapox Deposition					Machine #____, Th._____
Anneal					Fur.#____, 1100°C, 20 min.
Mask: Contact					#____, CD =_____
Aluminum Evaporation					Bell jar # _____ Th._____
Mask: Metal					#____, CD =_____
Glass Deposition					Machine #____, Th._____
Mask: Pad					Use Glass etch
Alloy					Fur.#____, 450°C, 30 min.
Wafer Evaluation					V_{to} =_____, BV_{DSS} =_____, V_{TM} =_____, V_{TP} =_____

[1] For illustration only; not intended to describe a working process

Source: DATAQUEST, Inc.

3.1 Major Manufacturing Operations

TESTING

There are three places in the manufacturing processes where electrical tests are performed. We will discuss each test point individually and examine their interrelationships.

Wafer Evaluation

The first test is performed immediately after the last wafer fab step, usually in the fab area. This test, called "wafer evaluation" or "wafer mapping," is performed on test devices (MOS transistors, resistors) located either on the periphery of the circuit dice or on three to five special patterns intermixed with the standard circuit patterns. The parameters measured at this step reflect the critical parameters of the process and, by implication, if these parameters meet specification, then the processing has been properly performed.

Wafer Sort

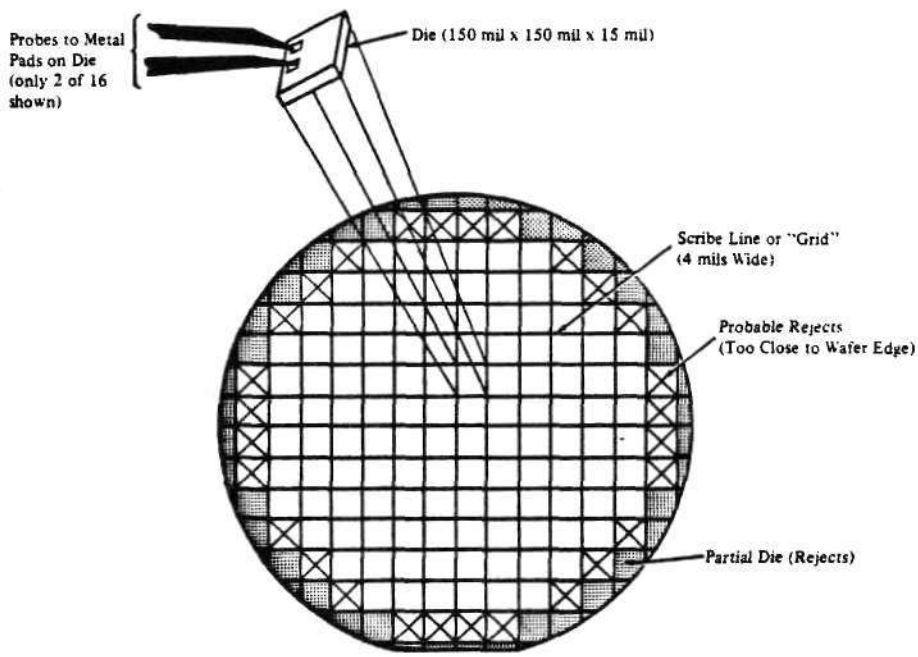
The wafer sort test is also referred to as "electrical sort," "E-sort," "wafer probe," or "probe." Here, individual wafers are placed on the platform or "chuck" of a wafer probe machine. Tiny probes, resembling straight pins, are then mechanically aligned over each of the metallized pads which are located along the periphery of the die, as shown in Figure 3.1-4. Each of these probes is electrically wired to a fixture or jig that interfaces the prober to the computer that exercises and tests the circuits. The probes are automatically "stepped" along the wafer, at each point coming down in contact with the 4-mil x 4-mil wide pads on each die (16 pads for the 16-pin 4K RAM). Every time the probes come down, a set of electrical pulses is applied to the circuit and the responses are measured. If all responses fall within some pre-established criteria, the prober proceeds directly to the next die. If a measurement fails to meet the limits, a small hypodermic needle or pen comes down and places a drop of "ink" (red food coloring) on the rejected die. The inked dice are then discarded at the first inspection (Die Visual) in the assembly process. Sometimes magnetic ink is used so that bad die may be removed magnetically.

The objectives of wafer sort are three fold:

- To reject potentially bad dice, so that no additional costs (such as assembly) will be incurred by them
- To subject each die to a test stringent enough to assure a better than 70 percent chance of passing final test when it reaches that point
- To feed back information to the wafer fab area on potential processing problems, particularly if the wafers have an inordinately high number of unacceptable (rejected) devices

3.1 Major Manufacturing Operations

Figure 3.1-4
WAFER SORT



Source: DATAQUEST, Inc.

Final Test

The final test is performed after the dice have been packaged. Since the packaged units now have external leads that operators or machines can handle, this process is usually automated. The packages are received from assembly in long metal tubes, with the units stacked end-to-end. Each tube is placed vertically, one end down, in an automatic package handler. The handler, in turn, releases one package at a time, allowing it to slide to a set of contacts that match its leads (16 contacts for the 16-lead package). The contacts are wired to the automatic tester or computer.

Each unit is stringently tested at this step, across all "worst case" conditions. The circuits are exercised for maximum and minimum speeds, for power dissipation, and for every combination of inputs and outputs—i.e., they are tested to ensure that they will meet all of the manufacturer's specifications and guarantees. Literally thousands of separate tests are performed.

Since most circuits are guaranteed to operate over certain temperature ranges, final test must be stringent enough to ensure that the performance standard will be met. The environmental conditions are usually assured in either of two ways:

- All devices are tested at the high-temperature end of the specification, or

- The devices are tested at room temperature with wide enough tolerances that operation at the temperature extremes is assured.

The first approach is obviously the safest, but it is also expensive in terms of labor and the amount and type of test equipment required. As a result, many semiconductor manufacturers will correlate the room temperature characteristics with the characteristics at temperature extremes, add a safety guardband to the room temperature test parameters, and then test at room temperature. Samples are taken regularly from the production lots and tested across the full range of environmental conditions to ensure that the correlation continues to be accurate.

Interrelationship of Water Sort and Final Test

There is a very close interplay between wafer sort and final test. In fact, in most operations, both test activities are located in the same room and often the same equipment is used for both; only the test programs are different.

As we mentioned earlier, one of the functions of wafer sort is to minimize the amount of additional labor and materials that would be assigned in producing bad circuits. This factor is especially important for semiconductors with lower die costs and, therefore, relatively higher assembly costs. However, wafer sort cannot eliminate all potentially defective dice for several reasons:

- Most sophisticated circuits, such as the 4K RAM, cannot be completely tested in wafer form because of the parasitic effects resulting from the probes and wiring, incident room light, etc.
- Some of the dice may be damaged during the assembly processes.
- The dice cannot be tested across the temperature range in wafer form because the wafer (and contact probes) cannot be easily maintained at temperatures other than ambient.

The objective of wafer sort is to ensure that enough of the potentially rejectable circuits have been discarded so that final test yields will be high enough to support the desired level of profitability. Excessively high final test yields are not necessarily acceptable. They may mean that potentially good devices are being thrown away at wafer sort. As a result, most manufacturers will adjust the tightness or severity of their wafer sort tests to allow the final test yields to fall in the range of 70 to 85 percent good units.

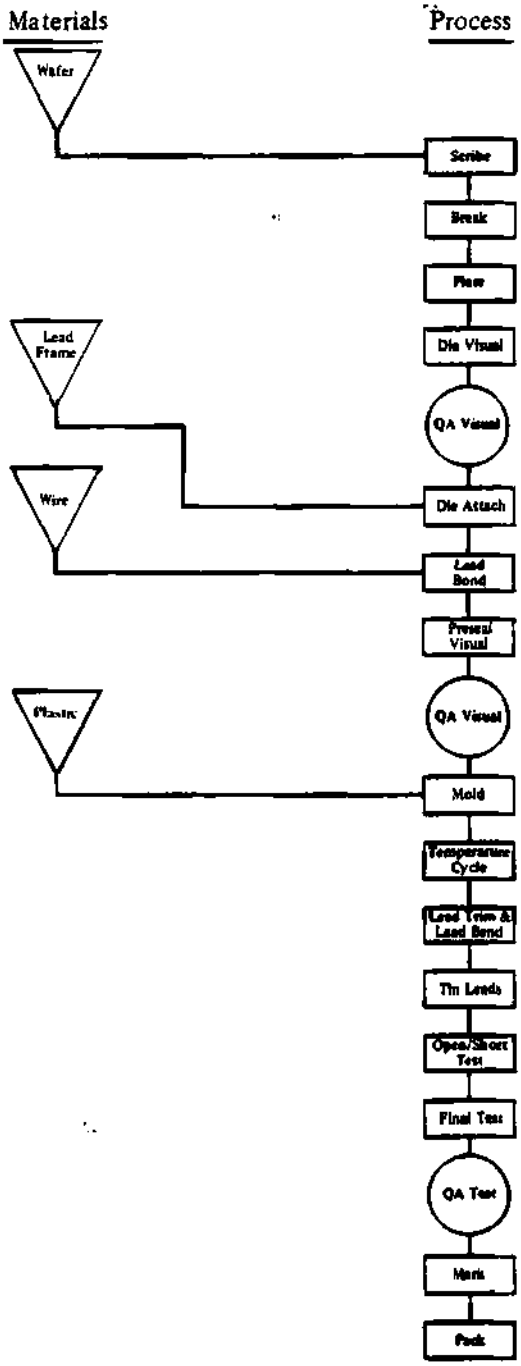
ASSEMBLY

This section describes the assembly processes used in packaging the 4K RAM after it has been tested in wafer form. A typical assembly flow is illustrated in Figure 3.1-5 and is described below:

3.1 Major Manufacturing Operations

Figure 3.1-5

ASSEMBLY WORK FLOW



Source: DATAQUEST, Inc.

- Scribe—Wafers are received from the wafer sort area; the bad devices have already been inked. The wafers are placed onto scribers, which are machines that automatically pass a diamond needle along "grids" on the wafers. These grids were outlined in the circuit pattern during the masking operations and delineate the boundaries of the square or rectangular-shaped circuits. The purpose of this process is to lightly score the silicon surface (to a depth of 0.001 to 0.002 inches), so that the wafer may be easily broken along the scored lines. This process is exactly the same as that used by glass workers when they score flat glass plates with a diamond tip to cut them.

Recently, laser scribers have been used for many semiconductors, with the laser beam performing the "scribe." They offer lower breakage loss and greater productivity. However, the heat generated by the laser has caused some reliability problems with N-channel silicon gate devices.

Even more recently, wafer saws have become popular. These units actually saw the wafer using a diamond encrusted saw blade. Sometimes, the wafer is sawn completely through and sometimes the saw kerf is only partway through the wafer ("scribe mode"). Sawing is popular for thicker wafers that do not scribe and break well. It is also popular for very small dice since the allowance for saw kerf can be much smaller than that for the normal scribe line. This process greatly increases die per wafer for small die since the space between dice is a large percentage of the die area.

3.1 Major Manufacturing Operations

- Break –After scribing, the wafers are placed on flexible holders and aligned such that one set of parallel scribe grids is registered against a fixed calibration mark. The holder and wafer are fed into a machine (wafer breaker) which flexes the holder and wafer around a fixed radius, so that the wafer breaks along one set of grids. The process is similar to running the wafer and holder through the wringers on an old-fashioned washing machine. After the wafer is broken in one direction, the holder is turned perpendicular to the first pass and put through the flexing process again, to break it along the second set of scribe lines. When the wafer comes out of this second pass, all the individual circuits have been separated and each circuit is now referred to as a "die." Sawn dice do not have to be broken, of course.

- Plate—The operator separates the good and reject dice at this point, using a pick-up tool. All rejected dice, with ink dots on them, are discarded and all good dice are placed in orderly rows on a square plate. Plating is not necessary if sawn dice are cut from wafers backed with sticky tape. This tape holds the dice in position.

- Die Visual –The plate of dice is placed under a microscope and each die is inspected according to preset visual quality criteria. Gross contamination, scratches, and broken dice are reasons for rejection.

- Die Attach or Die Bond—The good dice are now mounted into packages. An empty package frame is placed on a heating block and heated to 400°C. In some cases, a thin square of gold, slightly smaller than the die itself, is then placed on the package where the die is to be attached. Most companies, however, do not use this approach but purchase packages with thicker gold on the die bond area to save time and labor. The operator picks up the die by its edges, with a pair of tweezers, and gently forces the bottom of the die onto the thick-plated gold area. The gold immediately becomes a conductive "glue" which holds the die to the package.

- Lead Bond or Wire Bond—Bonding is accomplished in either of two ways. Due to its superior strength, gold wire is used on plastic packages to connect the individual 4-mil x 4-mil aluminum pads on the die to the corresponding leads on the package. For ceramic packages, either gold or aluminum wire is used.

  In gold bonding, the package is heated to 340°C. Looking through a microscope and manipulating a joystick controller, the operator positions the tip of a gold wire directly over a pad on the die. When the alignment is complete, the gold wire (0.001 to 0.0015 inches in diameter) is forced down on the pad and adheres. The operator then trails out gold wire until it reaches the corresponding pad in the package. Again, after alignment, the wire is brought down on the package pad and the excess wire is automatically severed at the pad. This process is repeated until all pads on the die have been bonded to the corresponding package pads.

In aluminum bonding, the basic bonding operation is the same except that, instead of heating the package, ultrasonic agitation of the wire is used to make contact with the pads by a "scrubbing" action.

Recently, microprocessor-controlled automatic bonders have become popular. In these machines, the operator need only bond one unit; after that the machine "remembers" where to place the bonds on subsequent dice and packages. The operator then needs only to establish initial orientation.

- Preseal Visual—This visual is performed to screen out any units that may have been damaged during the previous assembly steps. Unbonded pads, broken wires, chipped dice, and loose dice are reasons for rejection.

- Mold (plastic) or Seal (ceramic) —Plastic packaging is the lowest cost of all methods of semiconductor encapsulation. In plastic packages, the frames holding the die are placed in molds and molten plastic is injected into the mold to form the package body. After removal from the mold, the packages are cured in an oven at around 200°C. Ceramic packages must be sealed with a metal lid to make them airtight. Different methods are used, but all require running the device (with the lid) through a long sealing furnace.

- Temperature Cycle—One hundred percent of the units are cycled five times at temperatures between -55°C and +150°C to check for lead bond integrity.

- Centrifuge—This test would not be performed on plastic packages since the leads are buried in the plastic encapsulant, but is sometimes used for ceramic or metal packages. In this test, a centrifuge is used to accelerate the packages to 30,000 g's to stress the leads and bonds. This check not only tests for mechanical integrity, but also serves as a screen to determine whether the wire is too close to the bottom of the lids and thereby a potential circuit failure.

- Fine and Gross Leak—Like the centrifuge test, these tests would not be performed on plastic packages which have no cavities. The purpose of these leak tests is to ensure that the lids are properly sealed to the package, so that the die is protected from ingression of contaminants.

- Lead Trim and Lead Bend—Until this point in the process, several packages have been connected in strips by additional metal between the leads on the packages. At this step, a special lead trimmer cuts off this extra metal separating both the packages and the individual leads on each package. The leads are then bent at 90 degree angles to the bottom of the package.

- Open/Short Test—This is a simple electrical test, usually performed on a homemade test box, which checks package leads to determine whether any

are electrically shorted together or open. It is performed primarily by assembly plants as a monitor of assembly quality.

- Electrical Test or Final Test—This step was described previously under testing.

- Mark or Symbol—This step also can be performed prior to final test. It consists of stamping identification information onto the package: part number, manufacturer, a coded date, and origin of assembly (if overseas). It is usually performed after the final test step because different part types may be classified into different categories at final test.

- Pack—Completed units are packed with their leads shorted together, using conductive foam or aluminized containers, labeled, and readied for shipment to the customer.

SUPPORT ACTIVITIES

To this point, no mention has been made of the other support groups that are vitally important to the success of the manufacturing operations. We will briefly discuss the key support groups.

Circuit or Product Design

The function of the design group is to take marketing and customer inputs and design the circuits needed to perform the desired electrical functions. The inputs take the form of a specification of a function to be performed. The design group then determines the best circuitry and technology to generate the function. A designer simulates the circuit, section by section, on a computer (Computer-Aided Design or CAD) to determine the optimum design. The circuit is designed using the outputs of these simulations and photomasks are generated for the manufacturing area.

Product Engineering

Product engineering is generally considered to be an integral part of the manufacturing operation, even though circuit design is not. The function of the product engineer is multifaceted and he, in many respects, is one of the most important individuals in the manufacturing operation.

The product engineer works with the circuit designer as a product is being conceptualized and designed. As the circuit reaches the hardware stage in the form of wafers, the product engineer either writes or aids the designer in writing the electrical test programs for wafer sort and final test. After the first devices are obtained, he is

responsible for fully characterizing the circuits over the full performance range to ensure that they meet the specifications.

Once the product has been released to the manufacturing area by the product engineer, it is his responsibility to ensure that it continues to be manufactured economically, and that there are good yields. Problems that arise at wafer sort and final test are his responsibility. He must be certain that the products leaving those areas meet specifications. However, he is also responsible for ensuring that the manufacturing personnel can move the product "out the door" to the customers.

Since he neither designs nor manufactures the product, the product engineer is in the unique position of coordinating the communication between these two areas. It is his responsibility to isolate problems and determine whether a reject is process or design oriented. This function is important because most process engineers know little about designing circuits and most designers know little about processing.

Process Engineering

Process engineering is comprised of manufacturing or sustaining engineering and process development.

Sustaining engineering is usually just that—solving the day-to-day problems as they arise so that production can be sustained. It is commonly referred to as "fire fighting." In most companies, the function of sustaining engineering is to "keep the product running." Like the product engineer, the process engineer is often faced with the decision of whether to maintain a high level of quality versus "getting products out the door."

Process development, in a manufacturing operation, relates to short-term work aimed at desensitizing a particularly troublesome process, improving productivity through a process modification, and developing other methods of lowering costs (methods for reducing chemical usage, etc.).

Quality Assurance

The function of Quality Assurance (QA) is to ensure that documentation is maintained on every process, that controls are established at the critical steps, that the controls are monitored (and meaningful), and that warning flags are raised when out-of-specification conditions occur. These responsibilities hold throughout the manufacturing operations, including assembly and test. Quality Assurance is extremely important in any manufacturing process, especially in MOS manufacturing. Since a MOS circuit or transistor cannot be tested until the last step of the process (wafer evaluation), many process controls are implicit. That is, test wafers are run through individual processes to qualify that process as being "in specification." The production wafers are then put through the process based on the observation that the test vehicle met the proper specifications. In other IC processes, it is often possible to measure the results of that process step directly on the production wafer as soon as

it comes out of the process. In MOS, one assumes or implies that the product is "within specification" because the test vehicle was within the specified tolerances. Obviously, the interpretation of "in specification" may vary considerably from operator to operator, foreman to foreman, and engineer to engineer. It is QA's responsibility to limit that interpretation by maintaining uniform standards, specifications, and tolerances.

Equipment Maintenance

Maintenance and preventive maintenance are becoming important functions in wafer fabrication operations. Process and test equipment are becoming more sophisticated all the time. Process equipment contains many of the same integrated circuits that it builds, and testers have become small special purpose computers. Each of these must be continually maintained and repaired so that the manufacturing operation can run smoothly and economically.

Facilities Maintenance

The Facilities section later in the chapter (Section 3.3) will sensitize the reader to the broad and important range of functions which fall under the aegis of Facilities Engineering. Among the major functions performed are environmental control (temperature, humidity, and particulates), purity of gases, DI water and chemicals delivered to the fab area, regulation of the pressures of gases for pneumatic and processing functions, as well as proper disposal of all wastes. It is evident, therefore, that the preventive and on-going maintenance provided for the facilities is critical.

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3.2 Productivity Analysis

MANAGEMENT--NEW CHALLENGES

The decade of the 1970s has posed severe challenges for management in every industry, but nowhere more so than in the semiconductor industry. Very few of the vacuum tube manufacturers of the 1950s made a successful transition to semiconductors. Of those who started out in semiconductors in the 1970s, only those who have managed to make good and well-timed decisions will successfully survive the 1980s. At the corporate level, some of the most severe problems involve innovations in technology, new products, and new marketing strategies. For example, many U.S. companies that marketed digital watches and calculators were not able to remain in this very competitive business. Other problems of no less severity are inflation, expensive energy, high interest rates, environmental and social legislation as well as fluctuation of the dollar in international markets.

Semiconductor plant management is part of this structure. The management's objective is, of course, to maximize the output of high quality dice for a market characterized by rapidly declining prices. The company will be organized to achieve this objective but no matter how "classical" the organizational structure, the success of the entire operation will depend on the manager's training, style, and sensitivity. The proper balance needs to be struck between productivity and personnel problems; problems and tasks have to be defined; monitoring and feedback mechanisms must be established and used, and a suitable environment must be equipped for the tasks to be performed.

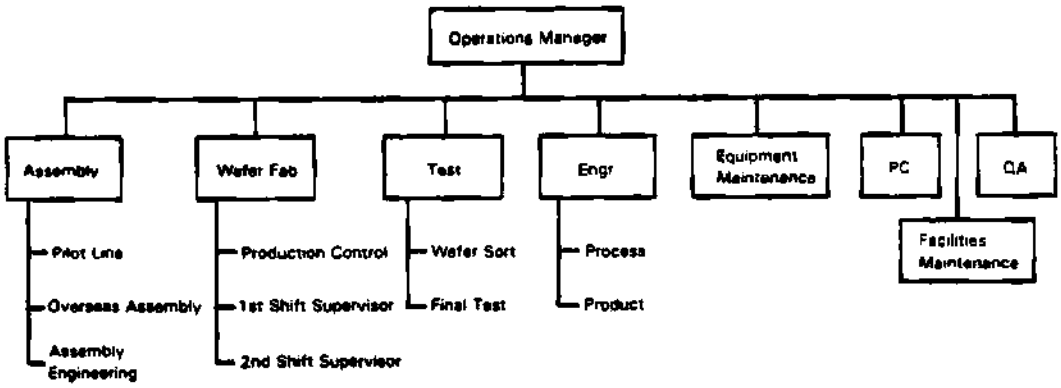
ORGANIZATION

Organizational structures for manufacturing operations vary from company to company and are often determined by the company's size. As shown in Figures 3.2-1 and 3.2-2, organizational structures can be task oriented or functional.

Larger companies and rapidly growing companies organize functionally to minimize duplication of people and equipment. As an example, most companies prefer to have a central assembly and packaging department to take advantage of the lower costS derived from higher volumes. Tested wafers are shipped to this central assembly facility from the wafer sort areas. The good dice are assembled in the United States or sent to Mexican or Asian assembly facilities or both. After assembly, they are shipped back to the specific product groups for final test and shipment. With this type of organization, the assembly responsibilities of the operations manager are reduced to that of production control and some assembly engineering to resolve problems unique to his particular product or product line.

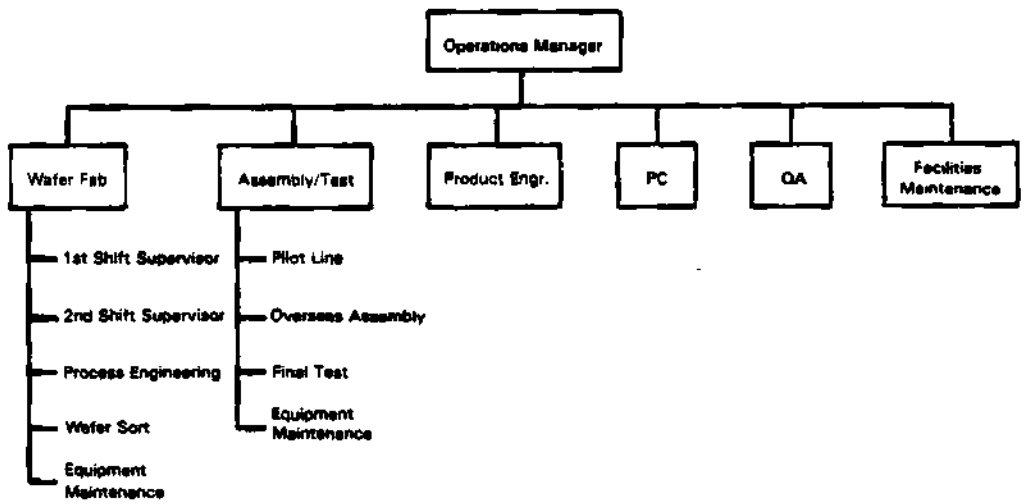
3.2 Productivity Analysis

Figure 3.2-1
FUNCTIONAL ORGANIZATION CHART



Source: DATAQUEST, Inc.

Figure 3.2-2
TASK ORIENTED ORGANIZATION CHART



Source: DATAQUEST, Inc.

3.2 Productivity Analysis

As illustrated in Figures 3.2-1 and 3.2-2, wafer sort may or may not be a part of wafer fab. Many companies prefer to integrate the two since the task of wafer fab is essentially to make good dice.

The approach to product and process engineering is mixed. Some companies prefer to integrate process engineering with wafer fab to minimize the "we, they" effect. With this integration, the operations manager has the resources to define and resolve the problems. The difficulty with this approach is usually in finding an operations manager who has the ability to understand both the nuances of manufacturing and the technical aspects of engineering.

Product engineering often reports directly to the operations manager, since the engineers must cover both wafer sort and final test; as previously discussed, these latter two activities are intimately related.

YIELDS

The single most important item in controlling costs and improving productivity and operational efficiency is yield. An efficient manufacturing facility not only has high yields, but those yields are consistent, competitive, and used effectively to make plant management decisions. Yields show up most importantly in wafer fab yield and wafer sort. However, these yields only reflect the cumulative results of a large number of previous production steps.

For a given operation, or set of operations, the yield is that percentage of good dice or wafers resulting from the operation(s). Although many hundreds of operations are performed in the making of an integrated circuit, the yield is only calculated at selected inventory or evaluation points.

Yields reflect the interplay of the many factors listed below:

- Design
- Process
- Equipment
- Facilities
- Operators
- Supervision
- Defects
- Die Size

Many of these factors, as will be shown in the discussion, also affect productivity.

3.2 Productivity Analysis

Design

Circuits must be designed so that the required parameters do not tax the limit of equipment performance or existing process technology. Hence, collaboration between design and process engineering early in the product development cycle is of the essence.

Process

Well-engineered design tends to simplify processing. Above all, processes must be reproducible within comfortable control limits yielding precise doping profiles, junction depths, critical lines and spaces, as well as reproducible film thicknesses and quality. Good processing is usually concise and elegant and shows up when prescribed electrical parameters are monitored. The result is increased productivity and device yields, savings in time, labor, and materials as well as assurance that devices will not fail prematurely in use.

Equipment

Wafer breakage is the ultimate defect. Apart from poor handling by operators, machines are the greatest causes of wafer breakage and pattern damage. If wafer breakage were observed in UV light, it would be seen that thousands of fine silicon particles are discharged into the ambient. These particles adhere to exposed wafer surfaces by electrostatic attraction and cause unwanted diffusions, damaged mask patterns, and other yield-limiting problems later in the process. Thus, proper equipment can provide faster wafer throughput, lower operator handling, and assure precision and control; but to do so, it must not malfunction. It must also be designed so that machine oils and metal particulates from its rotor brushes and other parts never abuse the product.

Automation has always been a subject of controversy in the semiconductor industry and for good reason—it has both strong advantages and strong disadvantages. In perspective, the semiconductor industry is not very automated. In spite of high capital costs, the industry is still labor-intensive. Burdened labor costs continue to be one to two times the cost of depreciation. For this reason, it would seem that more automation is natural, and, indeed, the industry is automating. However, because several factors work against automation, the degree of automation in any facility must be a considered decision.

Automation holds the potential of higher product throughput, lower labor costs, and higher labor productivity. It has the possibility of lowering costs that result in improvements in manufacturing control beyond human capabilities. However, the decision to use a more automated piece of equipment can entail problems of high equipment costs, possible lower yield, trained labor requirements, less flexibility, and short equipment lifetime.

3.2 Productivity Analysis

Due to the complexity of semiconductor processing and the precision required, automated equipment can be very expensive. The added expense is an additional burden on an industry that is not, in general, well financed.

In the semiconductor industry, equipment depreciation periods are very short (five to seven years) because of the continual need for state-of-the-art precision to be competitive. As a result, semiconductor manufacturers have often been burdened with automated equipment that has been bypassed by the rapid changes in technology. Consequently, they have hesitated to more fully automate their production lines.

Facilities

Facilities engineering must provide process gases, chemicals, and DI water of the highest purity, compatible with the state of the art, at their points of use in the fabrication area. Moreover, throughout the entire process, the area must be maintained at a specified level of cleanliness, temperature, and humidity. Much of the new equipment is sensitive to vibration which also must be minimized. Neglect of these control functions can reduce fab and device yields to levels of unprofitability.

Operators

All things being equal, device and wafer yields can be seen to keep pace with operator progress along the "learning curve." In other words, as operators become familiar with new processing areas, equipment and processes, productivity and yields tend to increase with time. This is why proper and prompt training is so vital in this operation. If one appreciates the "learning curve" problem, it is not difficult to understand the deleterious effect a high operator turnover rate can have on both fab and device yields. No matter how well techniques and processes have been developed, a single untrained operator can reduce yields to a shambles; this is particularly so in the face of inexperienced supervision. Once training has been completed, the remaining factor is one of discipline.

The manufacturing of any integrated circuit requires a high degree of precision, extremely complex processing, and a general awareness by management and engineering of exactly what is going on at any given time. Discipline and control in a manufacturing facility are absolutely necessary if the company is to be successful. No matter what amount of investment, talent or effort there has been, a lax operation will not succeed.

Discipline is most important at the operator level. It requires an operator to be able to perform a complex series of processing steps hundreds of times without error. The operator must also be aware of problems that may have developed at some other step in the process and must alert engineering or production control.

3.2 Productivity Analysis

One of the most fruitful effects of control is the feedback of information. Specific information on yields must be collected at final test, wafer sort, and other points, and then placed in the hands of the engineering support group. These groups, in turn, must use that information to spot or monitor potential problems and to correct such problems before they arise.

Since yields cannot be perfect, the operations manager must be extremely careful in the use of his resources—both labor and capital. Thus, he must have a knowledge not only of yields, but also of the effect that engineering attention, more operators, or a new piece of equipment might have on those yields. Then he must decide how to use his limited resources most effectively for the good of the facility. This decision is often extremely difficult, especially when the various manufacturing areas and support groups may be more concerned with showing their areas in the best light regardless of the benefits to the total facility.

These interrelationships make it clear that cooperation is extremely important to a smoothly running facility. Even those familiar with semiconductor manufacturing have difficulty grasping the entire process and its interrelationships, and it is always difficult to be objective. For example, suggestions that a device design might be hurting yield can be particularly galling to a design engineer, who might feel that the problem lies in processing. Nevertheless, device design very often can put an unfair burden on processing capability. Thus, cooperation between the two areas is essential.

Supervision

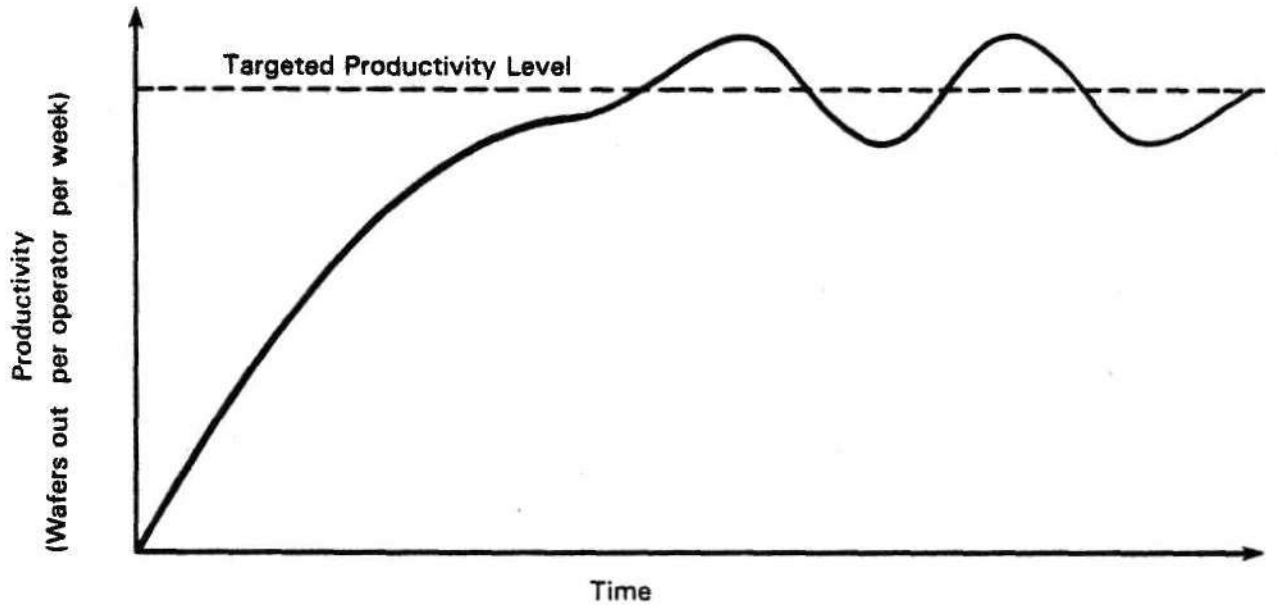
Care must be taken in the appointment of supervisory personnel since their function goes far beyond that of merely directing traffic. The supervisor must, in turn, ensure that operators can and do perform their required functions.

Once weekly and monthly production schedules have been set, it is the production supervisor's job to ensure that the required levels of production are met with regard to performance (productivity) and yields. The supervisor then must be able to identify and solve problems on the floor relating to equipment, process, personnel, and changes in production schedules.

Yields are known to suffer if material remains too long in the line. The precise mechanisms are not totally understood. Hence, fast throughput is a prime requisite of a production line. The actual processing time for most devices ranges from 20 to 40 hours; yet it is not uncommon for production runs to average 2 to 4 weeks in the line.

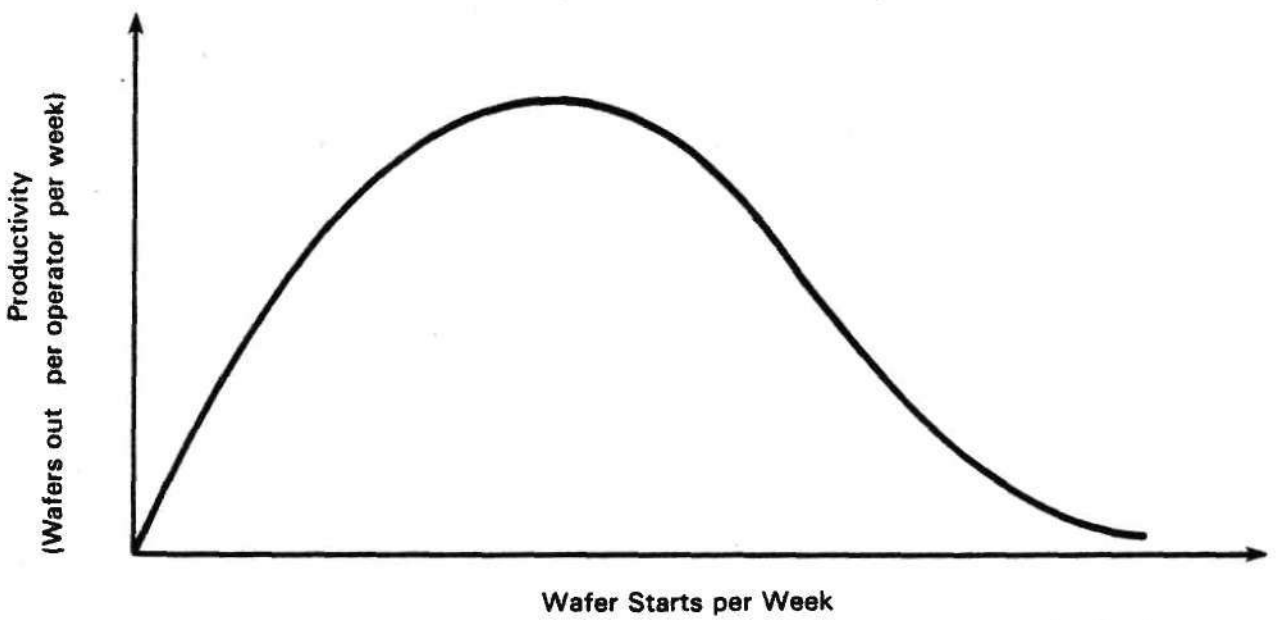
Wafer starts-to-inventory ratios vary from 1:3 to 1:5. Typically, the higher the inventory, the less productive the line. For a given product mix there is an ideal ratio which must be established. Figure 3.2-3 shows the way fab efficiency and productivity vary with time (learning curve) and total wafer starts.

Figure 3.2-3A
THE LEARNING CURVE



Source: DATAQUEST, Inc.

Figure 3.2-3B
FAB EFFICIENCY VS. WAFER STARTS



Source: DATAQUEST, Inc.

3.2 Productivity Analysis

Supervision at the engineering level is no less critical since, not only must the engineering staff monitor inadequacies in the set process most carefully, but also perturbations due to operators, environment, and equipment. The formal disciplines involve physics, chemistry and metallurgy. Since the laws of physics are not known to vary substantially among Dallas, Phoenix, or Santa Clara, for example, the reasons offered at times for processes breaking down or for yields declining are often a tribute to the creativity and inventiveness of the reporting engineers. It is the job, therefore, of their supervisory counterparts to have established key monitoring and reporting mechanisms to make analysis prompt and reasonable. These functions are the sine qua non for maintaining high yields and productivity.

Defects

So much has been written about the effects of defects on yield that we will treat only those aspects of the subject which DATAQUEST feels are important from a management point of view. Before discussing yield models, however, we have listed defect mechanisms that are known to result unquestionably in yield losses.

Any artifact which results in any alteration of the designed pattern, spurious capacitor, voltage or current values, spurious current paths, or premature failure of the device can be considered a defect. These include:

- Wafer Breakage. Wafer breakage is considered the ultimate defect.
- Mask Defects. This defect encompasses printable spots, breaks in pattern geometry, and incorrectly patterned critical lines and spaces. In projection printing, these defect levels are more or less set. In contact printing, further defects are generated and transmitted in the process of alignment.
- Silicon Crystal Defects. No one-to-one relationship has been established between failed devices and the type of defect. The effects also vary from one device type (e.g., MOS, Bipolar) to the other. Nevertheless, the chief culprits are nevertheless thought to be:
  - Diffusion pipes (spurious current paths)
  - Dislocations (disorders in the silicon lattice)
  - Oxygen clusters (high concentrations of oxygen in the silicon lattice)
  - Precipitation (high local concentrations, chiefly of metallic elements and carbon where "holes" and electrons tend to recombine)
  - Fluoride precipitates (heavy metal fluoride precipitates, chiefly on the silicon surface, undetectable as such under a microscope)

3.2 Productivity Analysis

Even if one started with defect-free silicon (a more expensive wafer), the crystal could be full of crystal defects at the end of the process because of differential thermal and mechanical stresses, contamination from chemicals used, and high-energy bombardment of the crystal.

- Pinholes in the photoresist (film too thin)
- Dust particles introduced during the photolithographic and diffusion processes
- Misalignment between the patterns during photolithography
- Incorrectly defined critical lines and spaces
- Hillocks (or "bumps") in metal and vapox films
- Aluminum "spiking" (penetration of aluminum beyond the diffused impurity or dopant layer into the underlying silicon)
- Incorrect impurity profiles
- Incorrect junction depths
- Incorrect film thicknesses
- Chemical contamination

It is at once clear that not all these defects are detectable by the routine microscopic inspections of fab processing. Further, as die sizes increase and device geometrics decrease, the size of particles that can affect circuit yields and performance is also decreasing.

In the years since 1975, we have seen the birth, maturation, and decline of the 4K dynamic RAM. Its yield history is inextricably involved with a history of decline in defect levels. The resulting increase in yields against a background of declining unit prices was responsible for its prolonged life in the marketplace in the face of the burgeoning market for the 16K dynamic RAM.

Table 3.2-1 shows that average defect densities in the semiconductor industry have been decreasing dramatically during the past 12 years. Note that between 1975 and 1976, the typical defect densities declined from 3.6 to 2.5 per square centimeter, causing an increase in yield for the 150-mil square 4K RAM from 12 to 22 percent—almost a factor of two. This yield improvement is associated with the change from emulsion to hard-surface masks. Projection printing (primarily) has given rise to another average defect density decrease from 2.46 to 1.40 per square centimeter, increasing the wafer sort yield once more—from 22 to 40 percent.

3.2 Productivity Analysis

Table 3.2-1
HISTORY OF INFERRED DEFECT DENSITIES

Year	Typical Wafer Sort Yield	Die Size (Mils)	Number of Mask Layers	Defect Density (Per sq. cm.)	Comment
1965	60%	40	6 (bipolar)	10	–
1967	10%	94	5 (MOS)	10	–
1975	12%[1]	150	5 (MOS)	3.6	From Fig. 3.2-3
1976	22%[2]	150	5 (MOS)	2.5	–
1977	40%[3]	150	5 (MOS)	1.4	–
1977	26%[4]	452	11 (CCD)	0.1	R&D device

[1] 4K RAM with emulsion masks.
[2] 4K RAM with hard surface masks.
[3] 4K RAM with projection printing.
[4] Master masks were optically inspected and the defects eliminated manually with laser "ZAPPER".

Source: DATAQUEST, Inc.

The last device in Table 3.2-1 is a CCD device manufactured in an R&D environment using carefully controlled projection printing. Considering the large 450-mil die size, the yield shown is very high, corresponding to an inferred defect density of only 0.1 per square centimeter. If this defect density could be achieved on the 4K RAM line in a production environment, the predicted wafer sort yield would be an extremely high 93 percent. The result would be an almost proportionate increase in plant capacity. Therefore, a high financial incentive exists for semiconductor manufacturers to achieve this kind of yield improvement.

Before projection aligners were introduced, images were transferred from the photomask to the wafer by bringing the mask into contact with the silicon wafer itself. This approach resulted in damage to the mask by the silicon wafer, even with the use of the so-called proximity printers that supposedly brought the mask close enough to make a good image without actually touching the wafer. The contact between wafer and mask eventually caused so many mask defects that it was necessary to throw the mask away and obtain a new one. Since defect densities increased as the mask was used, the significant defect density was the average between that obtained on new and used masks.

3.2 Productivity Analysis

Table 3.2-2 shows typical defect densities obtained with various kinds of masks. Although the defects were measured on actual masks, the numbers quoted may not be strictly accurate because the definition of defects varies somewhat, and because human operators are unable to catch all defects. Recently, Bell Laboratories developed an Automatic Mask Inspection System (AMIS) to monitor defect levels more accurately. Similar systems are available from KLA and Dainippon (Japan). Defect densities are shown for both new and used masks. The average defect density is simply the average of a new and a used working plate or mask. Note that the hard-surface plate had defect densities somewhat lower than that of the emulsion working plate. This reduction in defects accounts for the improved yield of 4K RAMs between 1975 and 1976.

Table 3.2-2
MASK DEFECT DENSITIES

Mask Type	Defect Density (Per sq. cm.)	Defect Density (Per sq. in.)	Cost Per Layer	Comments
Repaired Master	.16	1.0	$600.00	–
Mask Blanks	.2	1.3	–	–
Stepped Master	.5	3.2	$ 75.00	–
Hard-Surface Working Plate	1.25	8.0	$ 37.00	–
Hard-Surface Working Plate, Used	1.86	12.0	–	After 100 soft contact exposures or 50 hard contact exposures.
Average Hard-Surface Defect Level	1.56	10.0	–	–
Emulsion Plate	1.86	12.0	$ 5.50	–
Emulsion Plate, Used	3.54	22.8	–	After 10 hard contact exposures.
Average Emulsion Plate Defect Level	2.70	17.4	–	–

Source: DATAQUEST, Inc.

3.2 Productivity Analysis

Table 3.2-2 also shows the defect level obtained on a stepped master mask. Since projection printers do not wear out masks, it is economically feasible to use the more expensive master masks to expose wafers. The lower defect density of the master masks gave rise to the 40 percent wafer sort yield for 4K RAMs in 1977. Master masks have a lower defect density than working plates because working plates are produced from master masks by the defect-inducing contact-printing method. This situation accounts for the difference in defect density between the stepped master and the hard surface or emulsion working plate. The defect level quoted for new emulsion plates is higher than that of new hard-surface plates; because of the lower cost, the mask maker cannot afford as much quality control. Indeed, Table 3.2-2 shows a strong inverse correlation between the defect level and the cost per layer.

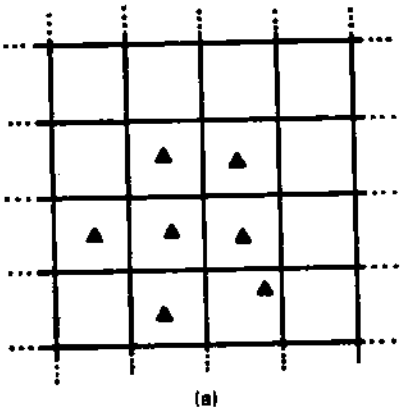
If the defect levels of the masks in Table 3.2-2 are subtracted from the inferred defect levels of Table 3.2-2, the result is a constant difference of 0.9 defects per square centimeter. This difference is attributable to defects induced during processing. Interestingly, the R&D device shown in Figure 3.2-2 has achieved defect densities of 0.1 per square centimeter, well below the defects resulting from the use of master masks or those that are process-related. The research staff that developed the device actually used master masks in which the defects had been repaired by eliminating defects with a laser "zapper." Apparently, they were also successful in significantly reducing process-related defects, but it is not known how that was accomplished.

Die Size

For a given level of particulate defects, the yield is greatly influenced by the die size. Figures (a) through (c) in Figure 3.2-4 illustrate this principle graphically as the die size is doubled from one figure to the next. The assumptions here are that only the visible defects shown will cause the die to fail, and that all areas of the device are equally susceptible to the visible defects. This is, of course, not true in real life. However, if we were to consider all possible yield-limiting defects as "visible" as shown in Figure 3.2-4 (a) through (c), the conclusion would not be altered in any way: yields are lower for larger devices, assuming a given level of random defects. Furthermore, we could conclude that reducing the total level of defects (seen and unseen) will allow devices either of larger area or higher circuit density to be built economically. This conclusion gives an extra dimension to one's perception of the VLSI trend. To optically resolve these smaller geometries requires not only more refined photolithographic techniques, but also a parallel program of reducing defects in all categories discussed above. We are thus defining a materials investigation program encompassing the silicon crystal itself as well as dielectric (oxide, nitride) and metal films used in the wafer fabrication process.

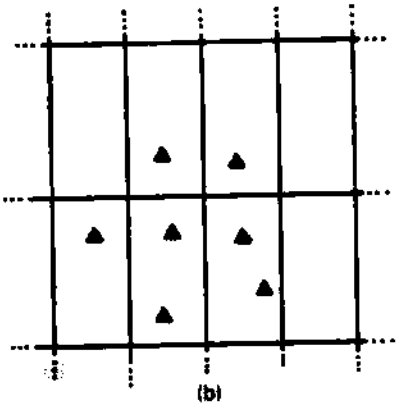
Figure 3.2-4

EFFECT OF DIE SIZE ON YIELD
FOR A GIVEN RANDOM PARTICULATE (DEFECT) LEVEL



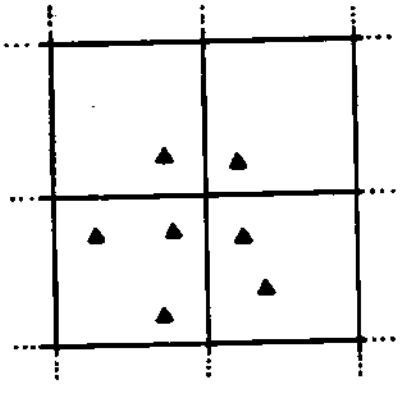
(a)

Yield: 9 Good
Out of 16 = 56%



(b)

Yield: 3 Good
Out of 8=37.5%



(c)

Yield: 0 Good
Out of 4 = 0%

Source: DATAQUEST, Inc.

3.2 Productivity Analysis

DEVICE YIELD MODELS

So far, we have shown only the dependence of device yields on defect densities and die size. Yields are also affected by the length and complexity of processing. Since the number of processing steps tends to be proportionate to the number of photomasking steps, it is common practice to use the number of photomasking steps (or mask layers) in most yield equations. Expressed mathematically,

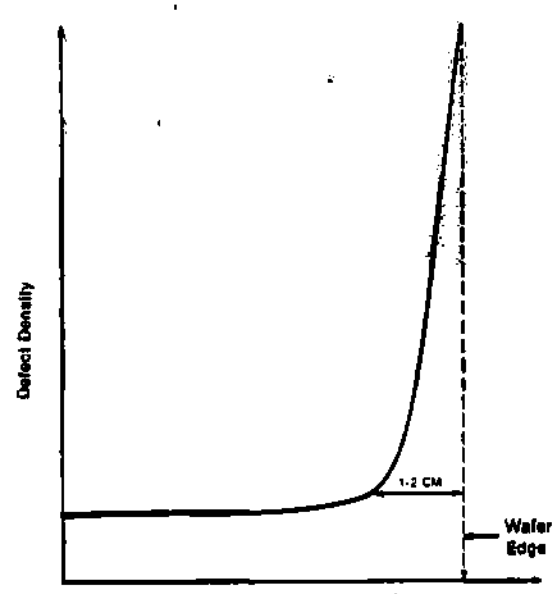
Y = some function of (D,A,n)

where Y = device yield
D = defect density
A = die area
n = number of masking steps

In the following discussion some assumptions are made. Not all areas of any particular chip are equally susceptible to defects. Hence, the area A actually being discussed is not the total chip area but is an effective area. The distribution of defects is often assumed to be random; yet the actual distribution as seen from wafer analysis usually is not. Often clusters of failed dice are seen associated with clusters of defects whose origins are usually difficult to determine. When the defects are not visible microscopically, crystal defects are inferred. Figure 3.2-5 shows the typical radial distribution of defects observed.

Figure 3.2-5

RADIAL DISTRIBUTION OF WAFER DEFECTS



Source: DATAQUEST, Inc.

3.2 Productivity Analysis

The high incidence of defects at the edge is usually attributed to tweezer handling, cracks or chips induced by loading wafers in slotted boats, or from "dump" transfer from cassette to cassette. One other important assumption often used in yield models is a normal distribution of defects from wafer to wafer over the period that device yields are studied.

Purely exponential models relating yield to die size show a more rapid decline of yield with increasing die size than is observed in practice. The choice of yield model depends on whether the defects are really random (in which case Boltzmann statistics might be useful) or whether a finite number of defect producing mechanisms can be isolated. The latter situation is usually assumed, and the Bose-Einstein statistics employed by Price[1] give the relationship:

$$Y = \frac{1}{(1 + DA)^n}$$

where the symbols have the same meanings as before. The photomasking step is offered as the defect-producing mechanism.

Note that as "A" and "n" become small, the yield approaches 100 percent.

If the die area and the number of mask levels are fixed, the defect density is of crucial importance in determining yield. Table 3.2-1 traces the historical reduction in inferred defect densities from 1965 to 1977. They are inferred because to obtain the defect density we use the formula above to work backward from the wafer sort yield, die size, and number of mask levels. The number was not obtained by actually counting defects on any actual silicon wafer.

Although Price's relationship does not give exact results, it can nevertheless generate useful experimental values of (D) over (n) masking steps. This is of some help in predicting device yields (hence cost) for newer, larger circuits. Practical values of (D) reported in 1979 for 10-layer (n = 10) devices, both MOS and bipolar, range from D = 6 per square inch (sq. in.) to a high of D = 10 per sq. in. That is to say, each layer contributes 6 to 10 defects per sq. in. cumulatively over n = 10 layers. These data are derived from contact printing processes where double resist coating techniques were used at critical layers.

As critical dimensions (gates, emitters) decrease, there is an apparent increase in defect densities as these dimensions become more susceptible to smaller defects. Thus, for a given minimum feature size of x microns, the effective defect density D* is related by an equation of the form:

$$D^* = Ae^{Bx} \text{ defects/cm}^2$$

The constants A and B can be evaluated from experimental data. D* will be found to increase as x decreases, hence, B is negative.

[1] J. E. Price, "A New Look at Yield of Integrated Circuits," Proc. IEEE (Lett), Vol. 158, August 1970, pp. 1290-1291.

3.2 Productivity Analysis

EFFECT OF YIELD ON COST

The effect of yield on cost is best illustrated by a simple numerical example. For the sake of illustration, assume the following situation:

(Material + fabrication) costs per wafer = $70
Testing cost at electrical sort (E-sort) per wafer = $30
Gross number of potentially good dice = 250

Then the total cost per circuit up to this point at:

100% E-sort yield =	$0.40
50% E-sort yield =	$0.80
25% E-sort yield =	$1.60
10% E-sort yield =	$4.00

At the fabrication level, yields must be kept high or the $70 figure used for this calculation will rise sharply. The same argument is true for Assembly and Final Test operations which follow the E-sort function.

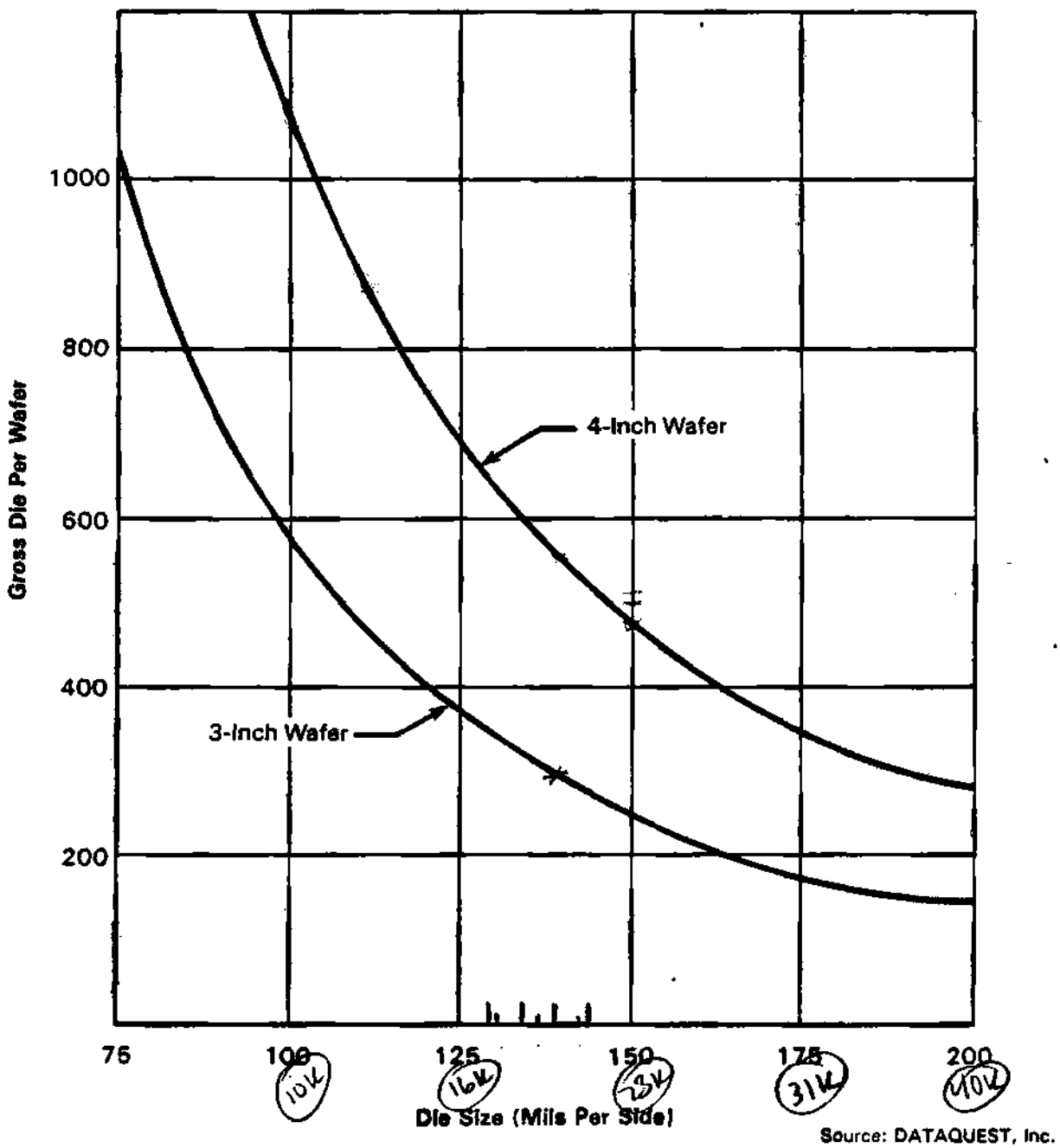
It is common practice to run a "shrink" on established circuit types. In this technique, every dimension on the die is reduced by a given factor. For example, if a 200 x 200 mil die were reduced to 160 x 160 mils (80 percent shrink), the gross dice per wafer would increase by 56 percent. Net dice would increase even more if the percentage yield also increased. However, actual percent yield could even be reduced due to an increase in effective defect density D*. Most manufacturers run various "shrinks" until the maximum number of net die per wafer is obtained. E-beam masks are popular for running these experiments because it is possible to make a mask with different "shrinks" in different die positions on a wafer. This process eliminates the possibility of different processings for different shrinks.

This brief discussion of the effect of yield on cost should in no way mislead the reader as to its importance. Once a manufacturing facility is in operation, the yields of new products must be carefully gauged before committing to production. Once in production, profitability rests on running the highest possible cumulative yields in Fabrication, E-sort, Assembly, and Final Test. Profitability control levels must be set for yields at all points at which they are to be monitored. Increasing wafer throughput to meet dice output schedules when yields are below profitability levels is, for any operations manager, a career-limiting move.

Figure 3.2-6 relates the number of gross dice which can be expected from 3-inch and 4-inch wafers for square dice of a given side. These numbers should be close enough to those for the rectangular dice encountered in practice. For these calculations, the outermost 150 mils of the periphery of the wafer have been neglected.

3.2 Productivity Analysis

Figure 3.2-6
GROSS (POTENTIALLY GOOD) DIE
PER WAFER VS. DIE SIZE



Source: DATAQUEST, Inc.

3.2 Productivity Analysis

PRODUCTIVITY CONSIDERATIONS

Capacity

One obvious way of effectively increasing the output of a given wafer fabrication area is to increase the wafer diameter. Going from 3-inch to 4-inch wafers increases the output of dice by a factor of nearly 1.8, all other things being equal. There is a practical difficulty to this solution: retrofitting the area without disturbing production. Usually a new 4-inch facility is built adjacent to the production area, the new area is started, then the old 3-inch area is shut down for retrofitting. The logistics of this operation must be carefully worked out, especially when both areas will be sharing services (gases, DI water, etc.).

Changing or updating certain processes can also increase the output from a given area. For instance, where ion implantation can replace conventional diffusion (for bases, p-wells, etc.), wafer throughput is increased. Outfitting furnace tubes for LPCVD not only saves floor space, but increases the output for deposition of nitride, polysilicon, and oxide films, often by a factor of two or more.

The Compressed Work Week

One approach to maximize the use of equipment is to operate it 24 hours a day, seven days a week, 365 days a year. While we know of no company pushing that hard, there are companies which fully utilize their equipment six days a week, 24 hours a day, in periods of high demand. To do so, these companies have gone from the standard 40-hour work week to the compressed work week (CWW).

The CWW consists of four teams of people: foremen, technicians, operators, and sometimes, engineers. Each team works three days a week, 12 hours a day. The seventh day (6 p.m. Saturday to 6 p.m. Sunday) is used primarily for engineering work and maintenance of equipment. This approach allows every piece of equipment to be manned and operated 144 hours a week, with no overtime. Time is also saved because one less shift is needed.

Although the data are still sparse, the companies report no increase in absenteeism, tardiness, or turnover. In some cases, they claim the numbers are better than that of the standard work week, particularly if a substantial amount of overtime is required for the latter approach.

While this approach makes excellent use of capital resources, the negative aspects are many:

- Generally, to man the four shifts, more operators, foremen, and technicians are needed, particularly at lower volumes.

- Communication between shifts can become a problem. For example, a unique process problem that is resolved on Shift One at 3 p.m. (Wednesday) may never be explained to the foreman who handles Shift Two, which ended Wednesday morning at 6 a.m. These two foremen will not see each other again until 6 a.m. Monday morning of the following week.

- Cross-training of operators is a necessity, so that they can do some job rotation during the day to minimize boredom and fatigue.

- If one operator is absent for a day, it means a 33-1/3 percent loss of that worker's weekly contribution.

- Generally, hourly wages are higher.

- There are difficulties in maintenance staffing.

In lieu of the compressed work week, standard two-shift or three-shift operation is very common. A further modification of the CWW is the 4-day, 10 hour-per-day approach.

Maintenance

Most companies have found that an effective maintenance team is cost effective in the long run when downtime costs are considered. Maintenance is an often neglected activity occurring only as "reactive" maintenance—when equipment is giving trouble. The biggest problem is that maintenance personnel usually do not have access to production equipment to accomplish preventive maintenance because the equipment is always in use.

A second problem is that equipment downtime is typically longer than previously because of the complexity of the machines and the extent to which electronics are used. The self-taught mechanic who was the expert on past machines often finds it impossible to pinpoint rapidly the failure of an integrated circuit. On the other hand, electronics technicians, very few of whom want to be mechanics, are "all thumbs" when it comes to fixing the mechanical problems.

Back-up Equipment

It is not uncommon for some equipment, particularly in wafer fab, to be down for four hours or even an entire shift. Since the fab processes are sequential, the failure of one key piece of equipment affects succeeding processes and can enormously affect productivity. For this reason, it is often wise to have "back-up" equipment.

Assume that a fab area has a single coater. If that machine was found to be subject to an exceptional number of problems on a continuing basis, it might be desirable to purchase a small machine (two tracks versus four tracks) for back-up. That alternative is desirable because a shut down of all four tracks of the single coater would also shut down activity of five aligners, two developers, and, ultimately, the succeeding diffusion and deposition processes.

3.2 Productivity Analysis

Judicious placement of back-up equipment is paramount to the running of a successful manufacturing operation. The extra capacity allows preventive maintenance to be performed more consistently and allows manufacturing to continue to operate, although at a slower rate, when the primary equipment fails.

Fab Output and Operator Productivity

Wafer fabrication productivity is an important measure of the efficiency of an LSI facility. Although productivity can vary, there are two good measures of an efficient operation:

- There should be 1.0 to 1.5 wafers out per square foot of fabrication area per period (1 period = 4 weeks). The average tends toward 1.2 wafers out per square foot for most product mixes. "Wafers out" refers to good wafers on which a reasonable wafer sort yield can be obtained.

- There should be a minimum of 80 wafers out per operator per period for a 12-mask process and 160 wafers out per operator per period for a 6-mask process.

There are other conditions which affect this set of productivity numbers:

- Device geometries are assumed to be 6 microns and smaller.

- Cumulative fab yields must lie between 70 percent for 12-layer devices and 85 percent for 6-layer devices.

- Rework yields must be 5 to 10 percent or lower at In-Process (Develop) Inspection and 2 to 4 percent at Final Inspection (see Photomasking, above).

- Implant masking steps count as half a manufacturing step in the productivity relationship.

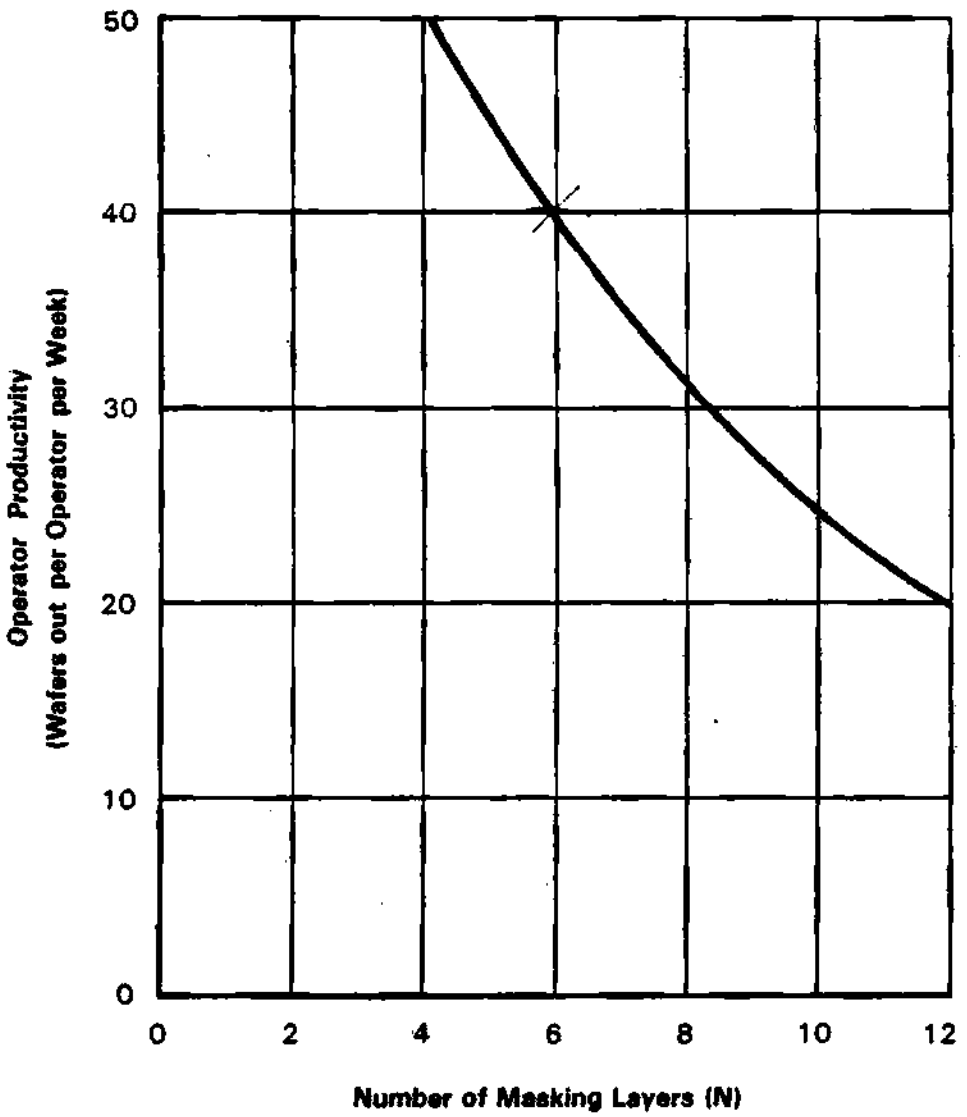
- Within these limits, the variation in the productivity figures is ± 7.5 percent.

- The schedule includes two shifts per day, five days per week (mostly maintenance and calibration on the third shift).

The plot shown in Figure 3.2-7 is the form of a rectangular hyperbola in that the product:

(No. of wafers out per operator-week) x (No. of masking layers) = 250

Figure 3.2-7
VARIATION OF PRODUCTIVITY WITH DEVICE COMPLEXITY



Source: DATAQUEST, Inc.

3.2 Productivity Analysis

By interpolation, a reasonable expectation of operator productivity can be calculated from this curve if there is a known number of masking layers for the devices and if the above-mentioned conditions are met.

The number of wafers out per month depends on both the general productivity of the operation and the yield in wafer fabrication. If the wafers out per month can be estimated and the number of operators in wafer fabrication can be estimated, then a good measure of the facility's efficiency can be calculated. A poorly managed operation, on the other hand, may produce carloads of wafers, but if the process is not well controlled, the wafers may yield only a negligible amount of good devices.

From these two rules of thumb for fab output and operator productivity, many useful inferences can be made.

Of the three major fabrication areas, masking is the most labor-intensive. Consequently, the majority of our remarks on productivity relates to the effects of masking. The key forces impacting fabrication productivity are:

- Complexity of the process
- Operator turnover
- Scheduling
- Yields
- Degree of automation

When cumulative yields are not in the 70 to 80 percent range assumed above, Generally, there is a great deal of material that has to be reworked in the photomasking area. This situation has the effect of increasing the labor per wafer and decreasing wafer output.

There is another productivity tool that is in use because it establishes a useful relationship between the number of moves per good wafer (wafers moved between selected process steps) and cumulative fab yields.

$$\text{Number of moves} = (\text{number of wafers}) \times (\text{number of steps}) \times \left(\frac{1 + Y}{2Y}\right)$$

where Y = cumulative fab yield expressed fractionally. The time base can be either a week or a period. For any particular operation, the process steps selected have to be clearly defined to set the standard for the number of moves. The conditions stated under operator productivity above, also pertain.

3.2 Productivity Analysis

Scheduling

Since the MOS fabrication processes are sequential, it is essential to keep the work-in-process (WIP) inventories properly distributed—i.e., keep the production line "balanced." In spite of back-up equipment, most fabrication areas do not have the capability for making up much lost ground. The shutdown of one station can cause others to shut down. An interactive, responsive Production Control group is essential to a good fabrication operation. It must schedule the work to make the most effective use of people and equipment.

Equipment For Increased Productivity

The diffusion and deposition processes, to a great extent, have been automated. Nevertheless, cleaning, dipping, loading, and unloading batches of wafers still tend to be labor-intensive. These are being simplified, however, by the use of "cassettes" which look much like the old 35 mm rectangular slide trays. These carriers allow "flip transfer" of wafers—simply by placing an empty carrier upside-down on top of a full one and flipping the combination. This approach eliminates the tedious, time-consuming effort that many companies still use: moving each wafer individually from one carrier to the next with a pair of tweezers.

The fully automatic mask aligners now being introduced promise to be a boon to the semiconductor industry. Alignments per operation may increase by a factor of 1.3 to 1.5 as machines assume the tedious role of aligning the pattern on the mask to that on the wafer. Training time for new operators may be reduced to less than a week. Reworks for misalignments should be nil.

Assembly

The measures of productivity within the assembly area are difficult to define. A rule of thumb for a 16-pin, plastic packaged 16K RAM would be: units out of assembly (not including final test) should average at least 5,000 per operator per month.

Of the three major components of our manufacturing model, assembly is the most difficult in which to increase productivity. The most significant recent change is the introduction of automatic lead bonders. Tape or gang bonding is also popular on devices that are produced in very high unit quantities. Another trend is the conversion of products to molded plastic (usually epoxy) packages, where frames holding ten or more units at a time can be assembled and cut apart after molding. Plastic packages have been successful because the material costs are significantly lower than those for ceramic packages. All other innovative assembly techniques have reduced some of the labor content, but have not lowered the cost of the finished unit significantly. In some examples, the labor content decreased in assembly, but the labor and materials cost rose in wafer fabrication.

3.2 Productivity Analysis

In some respects, the ready availability of low-cost Mexican and Asian assembly labor five to ten years ago has hindered the development of lower cost packaging. Assembly still can be performed in some countries for a fraction of a dollar per hour. However, this is changing and overseas assembly costs are on the rise. Labor costs are increasing and inflation is rapidly forcing up the cost of packaging materials.

Consequently, the present emphasis in assembly is being placed on plastic packages, low-cost hermetic packages (CERDIP), automatic and tape bonders, and the elimination of approximately 100 percent yield process steps. In the last case, process steps in which the yield is consistently 100 percent have been eliminated. Examples of such steps include those of temperature cycle and centrifuge. In place of the 100 percent test, the companies implement a statistically based sample plan.

Test

The RAM testers on the market today are basically computers. They have a tremendous amount of sophisticated integrated circuitry compounded with the need to interface with electromechanical probers and handlers. Because of the complexity of the test system, subtle problems frequently arise that are difficult to track down and resolve. Testers of this complexity are sometimes down for hours at a time, and tester downtime is a serious problem. Most manufacturers have a team of electronic maintenance personnel, some with engineering degrees, specializing in troubleshooting on testers. In choosing a test system, maintenance will often override the other productivity considerations.

Wafer Sort

The RAM testers currently available on the market have the capability of running two or four wafer probe machines. Test time per wafer for these machines depends on the complexity of the test program (which depends on the complexity of the product) and the number of dice on each wafer. A wafer with small dice—40 mil x 40 mil—may take 30 minutes to test, while a wafer of 150 mil x 150 mil with almost 14 times fewer dice may take as little as five minutes, including set-up time.

Productivity can be improved in two ways. An operator can run two probers at a time, rather than only one. If the probers are likely to wander, i.e., if the probes move off alignment with the pads on the die, it is preferable to have an operator at each station. Moreover, the test program can be written to test the most likely failure mode first and immediately go on to the next die when the first failure is found on a die. This "first fail" approach is fast, but sacrifices information that may be achieved by identifying all test failures on the rejected die.

3.2 Productivity Analysis

Final Test

Productivity at final test can be most dramatically improved by going to "single insertion" or "single pass" testing. In "single pass" testing, the packaged unit needs to be inserted only once into a test socket. This procedure is contrasted with multiple-pass testing in which the unit is put in one socket for part of the testing and then pulled out and put into other sockets for additional testing. For example, the unit may be tested for functionality first and then put into another holder to perform tests for tolerance of temperature extremes or for dynamics. However, single pass testing is often difficult to implement because it requires complex testing equipment and adequate assurance that the device is being tested to specifications.

A second approach that greatly improves productivity is the use of automatic package handlers. These handlers take a tube of serially stacked dual-in-line packages and automatically feed one unit at a time into the test head. The output of the machine may be delivered to a number of tubes, each one representing a different performance level part. This type of testing can even be performed at the higher operating temperature limit, and parts can be sorted out to different temperature ranges. Use of these automatic handlers can increase the output per station by more than 30 percent.

SPECIFIC EQUIPMENT IMPACT ON PRODUCTIVITY

The four years since 1975 have seen experimental equipment pressed into general service. Two main purposes have been served: higher productivity and increased device reliability stemming from process reproducibility and control. Combinations of techniques provided by some of this new equipment have contributed to productivity by allowing more versatile processing. As a result of this versatility, more functions can be designed and processed per unit area of silicon.

Specific pieces of equipment and related techniques are discussed in this section on the basis of their impacts on productivity. They are:

- LPCVD of Polysilicon
- Sputtering of Aluminum-Silicon
- Ion Implantation
- Photomasking
- Automatic Diffusion Furnaces
- Plasma Resist Stripping

LPCVD of Polysilicon

The technique is not peculiar to polysilicon since oxide and nitride films for various applications are similarly prepared. The old polysilicon deposition process made use of a Radio Frequency-heated susceptor (a susceptor is a flat plate on which the wafers are placed) that transferred heat to the wafers by conduction. This device was expensive, had limited throughput, and was somewhat difficult to control. The control problems came about because the wafers were heated unevenly if they did not lie perfectly flat on the susceptor. Since the deposition rate is a function of temperature, uneven wafers tended to have uneven polysilicon layers.

3.2 Productivity Analysis

The new poly deposition process makes use of low-pressure chemical vapor deposition (LPCVD) equipment. This device is a diffusion tube that is operated at less than atmospheric pressure. The wafers are heated by radiation rather than by conduction; as a result, heating is more even and the polysilicon layers are more uniform. In addition to offering better uniformity, the LPCVD equipment is somewhat less expensive than the old equipment and has a higher throughput rate. The old poly deposition system cost $95,000 and had a throughput rate of 60 wafers per hour, whereas the new system costs $45,000 (excluding the furnace tube) and has a throughput rate of 100 wafers per hour.

Sputtering of Aluminum-Silicon

Since 1975, geometries in N-channel silicon gate devices have become somewhat smaller which, in turn, has led to a desire for shallower diffused N-regions. Since the N-regions spread sideways as they diffuse deeper into the silicon wafer, the sideways spread can only be reduced by diffusing less deeply. When more shallow diffused regions are employed, a metallization problem results, which is caused by the fact that aluminum itself is a P-type dopant. Thus, if aluminum is deposited on a shallow N-type diffused region, there is a high probability that the aluminum will penetrate through the N-region during the subsequent alloy step, thus shorting out the junction.

The aluminum penetrates into the silicon because there is a preferred mixture of aluminum and silicon at alloy temperatures; silicon migrates into the aluminum, and simultaneously the aluminum dissolves in the silicon. In any event, this migration can be prevented if a small amount of silicon is added to the aluminum as it is being deposited on the wafer. The deposited aluminum will then contain all the silicon that it can accommodate at alloy temperature, and no migration can occur. Some manufacturers deposit more complex materials than aluminum-silicon (e.g., aluminum-silicon-copper or aluminum-copper).

Perhaps the best method of depositing compound films is sputtering and, in particular, magnetron sputtering. The sputtering process has been described earlier under Physical Vapor Deposition. Sputtering even lends itself to the deposition of refractory (high melting point) films such as tungsten, often used sequentially with titanium.

Such systems cost approximately $200,000 and are usually microprocessor automated and controlled. The "load-lock" feature usually offered allows wafers to be fed into the system under reduced pressure such that the system need not be opened up to room ambient. This feature minimizes particulate contamination of the work, and oxide inclusions in the film. The films are highly reproducible and, thus, the desired silicon content of the film is well controlled.

These features of control and process versatility are highly desirable and are a giant step towards VLSI goals of more shallow junction devices.

Wafer throughput is about 60 wafers per hour. The addition of cryopumps to these machines eliminates the need for and cost of liquid nitrogen used on diffusion pumps for creating the required vacuum.

3.2 Productivity Analysis

Ion Implantation

This technique offers process versatility and, hence, allows greater packing densities. Because it is a fast, room-temperature process, usually followed by specific or implied high-temperature activation, throughput is high.

Ion implantation is somewhat analogous to diffusion in that it is a means of introducing controlled amounts of "impurities" or dopants into silicon material. This technique is attractive because it offers much more precise control of the impurity concentrations than does diffusion. Typically, diffusion concentrations can only be controlled within a factor of 2 to 1, whereas ion implantation allows control of concentrations to less than 5 percent.

In an ion implanter, the desired dopant (e.g., boron) is first ionized by a radio frequency field. Some atoms may have only one electron removed while others may have two or more removed by this process. The atoms with the desired number of missing electrons are selected from the ion stream by passing all ions through a filter. This device removes the unwanted ions, allowing only the desired ones to pass. The desired ions are then allowed to fall through an electric field potential of approximately 300,000 volts, which accelerates the ions until they move at a high velocity. They then "crash" into the silicon wafer and, because of their high velocity, penetrate some distance into the silicon material itself.

Generally, the ions are focused into a beam and the entire silicon wafer is covered with ions by sweeping the beam back and forth to "paint" the wafer, much as an electron beam in a television set is swept back and forth to "paint" a television picture. The depth of ion penetration depends on the velocity of impact. The number of ions deposited in a given area can be precisely controlled by controlling the beam current and the sweep rate. In typical processes, about 10 seconds are required to implant a wafer. Other processes requiring heavier ion concentrations may have implant times as long as several hours.

Ion implant is often used to implant the field region and to implant beneath the gates of the pull-up devices to create "depletion loads." Some MOS processes also use an ion implant beneath the active MOS transistors to allow more precise control of threshold voltage. Ion implant is prevented in regions where it is not desired by masking with photoresist; the ions simply enter the photoresist and are decelerated there. In bipolar processing, ion implantation is routinely used for doping bases and resistors.

Photomasking

Two significant changes have occurred in the photoresist area in the last three to five years: 1) the substitution of projection printers for contact or proximity aligners, and 2) the addition of an automated photoresist processing line to replace individual pieces of photoresist processing equipment.

The projection printing aligners are responsible for significant yield improvements. These aligners project an image of a mask on the wafer in much the same way a slide projector projects an image of a 35 millimeter slide on a viewing screen. This technique requires use of a lens system to create the desired images.

By contrast, older methods of aligning and printing masks used no lenses at all between the mask and the wafer. Consequently, it was necessary to bring the mask very close to or in contact with the wafer so that the image (or shadow) on the wafer would faithfully reproduce the image on the mask. This process gradually destroyed the mask, as it was scratched by the wafer and pieces of photoresist stuck to it. These defects printed onto subsequent wafers, causing devices to be unacceptable.

Projection printing has been a dream for many years; in fact, work was begun on this technique in the mid-1960s. The problem is a complex one, however, because of the difficulty in making a lens of sufficient quality to resolve the images as finely as required by the semiconductor industry. Because of the resolution problem, masks are made by a "step and repeat" process, which creates multiple copies of the same pattern on a master mask through a series of multiple exposures. In this way, the lens that creates the images needs to resolve only a single die pattern and not the entire mask. These lenses, which are fairly expensive and may cost as much as $10,000, still do not have the resolution required for full wafer projection printing.

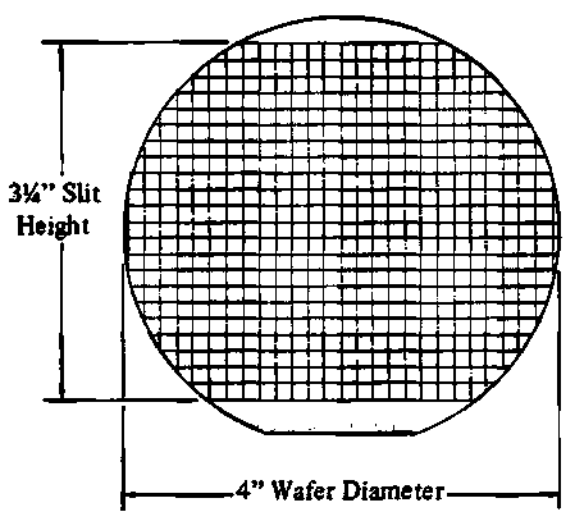
Lenses suffer from a defect known as "chromatic aberration," in which light of different colors is bent at slightly different angles as it passes through the lens, much as in a prism. Although most high-quality lenses are designed for only a narrow range of light colors (or narrow spectrum), they still have difficulty obtaining the desired resolution.

The first successful projection aligner, built by Perkin-Elmer, employed mirrors in place of lenses, somewhat like those used in large telescopes. Cobilt has a similar piece of equipment. This equipment will expose a full 4-inch wafer and has adaptive focus, partial field scanning, potentially higher throughput, and automatic alignment and loading. Since light never passes through any lens in either of these systems, the problem of chromatic aberration is avoided and very fine lines can be reproduced. Because the mirror reflects different colors of light equally, it is possible to use a light source containing many colors. Printing of finer lines is also possible because the mirror-lens technique alleviates some of the problems of "standing waves" in the photoresist. These waves are caused by reflections from the boundary between photoresist and silicon. When single-color light is used, the reflected light cancels the incident light in some areas, causing the photoresist to be underexposed. This phenomenon does not occur when light of many colors is used because each color of light has a region of cancellation at a different position in the photoresist. Thus, where one color of light cancels out, another color does not; the result is a more uniform photoresist exposure.

Successful projection aligners make use of spherical mirrors, which produce only a narrow region of perfect focus. The light is made to fall on the mask only in this region by putting a slit between the light source and the mask; therefore, only a narrow portion of the wafer (corresponding to the slit) is exposed at any given time. Because of the lens size, the slit height is limited. The entire wafer is exposed in this system by moving the mask and wafer simultaneously past the slit of light. The slit is affixed to the stationary light source, and the mask and wafer are then both mounted to a rigid carriage that sweeps them past the slit of light. Thus, the wafer is totally

exposed as the slit of light passes across it. Since the mask and wafer move together past the light slit, there is no theoretical limit to the size of the exposed area in the direction of travel. Figure 3.2-8 shows the exposure pattern that would result on a 4-inch wafer using a 3.25-inch lens. Although the pattern is only 3.25 inches high, it is 4 inches long. As a result, over 90 percent of the available wafer surface is exposed. For some time, many semiconductor manufacturers thought the projection alignment equipment limited them to 3-inch wafers; now it is apparent that there is a compelling reason to work with 4-inch wafers. The wafer in Figure 3.2-8 has 440 potentially good dice on a 3-inch wafer. The extra dice gained in this manner more than pay for the cost of the additional silicon in a 4-inch wafer. Aligners are now becoming available with 4-inch and larger lenses.

Figure 3.2-8
PROJECTION ALIGNER EXPOSURE PATTERN ON 4-INCH WAFER



440 Potentially Good 150 Mil Die.

Source: DATAQUEST, Inc.

3.2 Productivity Analysis

In projection alignment equipment, there is a trade-off between resolution and exposure time. As the slit is made wider, more of the wafer is exposed and, consequently, the speed of mechanical slit movement can be increased. Since the slit is appreciably wider than the region of "perfect" focus, resolution suffers. Similarly, resolution can be improved at the expense of throughput rate by narrowing the slit and slowing the rate of mechanical travel.

Early users of projection alignment equipment did not achieve satisfactory results because they did not provide the proper operating environment for the equipment. As one user states, "The equipment only works well in an engineering environment; accordingly, it is necessary to create an engineering environment in the masking room." Among other things, frequent preventive maintenance was required and daily focus checks had to be run. Some users did not achieve good results because they continued to buy lower cost masks with high defect levels. Projection alignment equipment also requires effective control of ambient temperature and humidity. Since the mask and wafer are separated by some distance, a small temperature change can cause the mounting system to expand slightly, changing the mask-to-wafer spacing and throwing the system out of focus. More than a day is required to stabilize the system after control of ambient temperature and humidity is lost. For this reason, special laminar flow hoods with good ambient controls are used with projection alignment equipment. Some of the new projection aligners have built-in temperature control.

Considerable savings are realized using projection printing. Mask costs per wafer out are well below $1.00 compared with $4.00-$5.00 per wafer out with contact printing. The principal justification for this equipment is the dramatic increase in wafer sort yield that it provides. Some users report that they have achieved payoff of their new aligners in periods as short as three to six months. At this time, most of the installed projection alignment equipment are Perkin-Elmer units. Canon and Cobilt also make projection aligners using mirrors rather than lenses.

Recently, step and repeat projection aligners have been developed. These aligners are similar to the step and repeat equipment used in mask making. They generally image only a portion of the wafer at a time and can achieve finer lines as a result. The wafer is then moved mechanically and as many images as needed to fill the wafer are made. Typically, these systems use lenses rather than mirrors. They are now being evaluated for high resolution work, typically between 1 and 2 microns. Suppliers include Canon, Censor, Electromask, GCA, Optimetrix, and Ultratech.

Even more recently, there has been a resurgence of interest in proximity aligners. When these devices were first introduced, it was not possible to purchase aligners with a peak-to-valley variation much better than 20 microns. Since most fine-line applications require a mask-to-wafer spacing of at least 10 microns, it is clearly necessary for the mask to touch the wafer at least on the peaks. This caused mask wear much like that observed in proximity aligners. Today, wafer flatness of 6 to 10 microns can be achieved and this technology is now viable for line widths in the 3 microns and larger range. It is attractive to users who do not require the most advanced technology because the aligners are about half the price of projection aligners.

3.2 Productivity Analysis

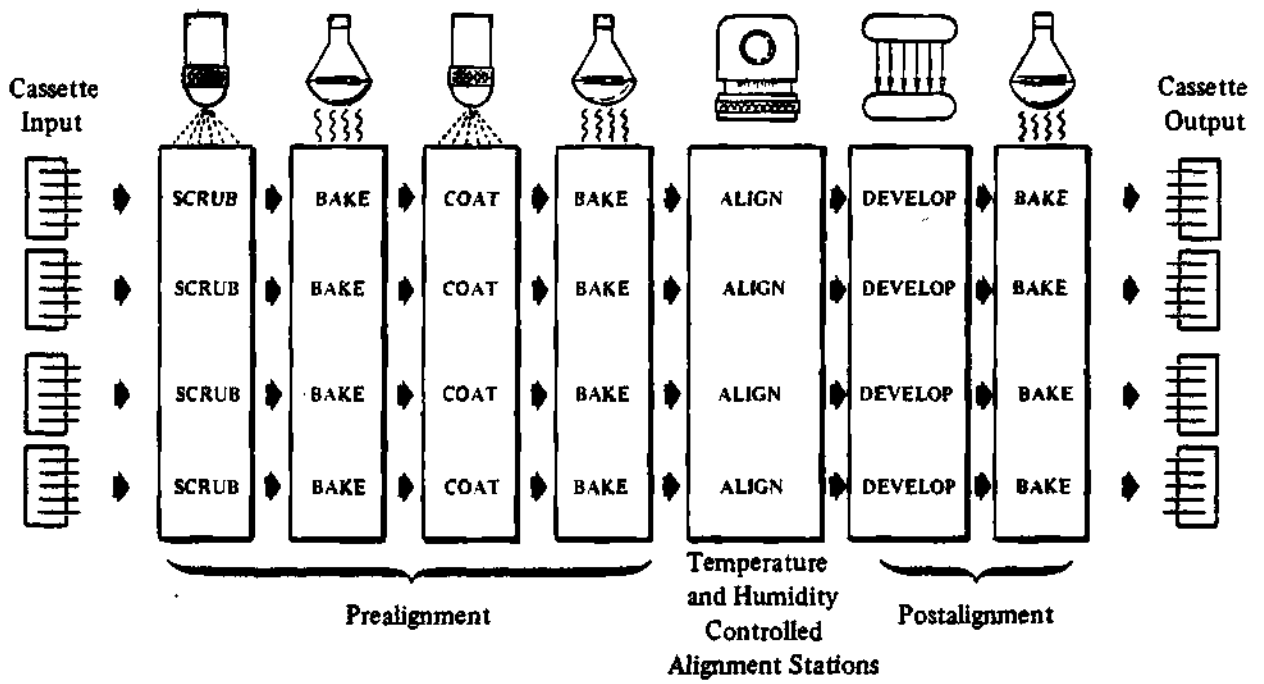
Figure 3.2-9 shows a schematic representation of an automatic photoresist processing line. It is a four-track line servicing four aligners and containing stations that scrub (or clean), bake (or dry), coat (spin on liquid photoresist), and bake (dry the photoresist) the wafers before presenting them to the aligner. A similar set of stations develops the photoresist after it has been exposed and bakes the photoresist once more. This sequence of steps is merely representative and does not illustrate any particular process.

Formerly, each station in Figure 3.2-9 was represented by a separate piece of equipment to scrub, bake, coat, and develop. Each piece of equipment had a dessicator or drybox that held wafers while they were waiting to be processed. The wait time between process steps was highly variable; in fact, it was ten times longer than the process time itself.

Photoresist processing requires tight control of parameters. As an example, the optimum bake time depends on how long wafers have been stored after leaving the coat or develop stations. If storage time is variable, then the process cannot be optimized with a fixed bake time. Therefore, some wafers exit the photoresist processing, fail to pass a subsequent in-process inspection, and must be sent back for rework. Industry estimates vary, but from 5 to 30 percent of the wafers may have to be reworked.

Figure 3.2-9

FOUR STATION AUTOMATIC MASKING LINE



Source: DATAQUEST, Inc.

3.2 Productivity Analysis

The automatic photoresist processing system shown in Figure 3.2-9 eliminates all inventory points between the cassette input and the cassette output by moving the wafers from station to station on a conveyor track. Various conveyors are offered by equipment suppliers—some use air jets, others use belt systems, and still others use a vibrating track method.

Conveying wafers automatically results in better control of photoresist processing because the storage time between steps is constant, causing a concurrent reduction in rework rates. Here we have assumed that rework is essentially negligible. Furthermore, the elimination of in-process inventory improves throughput time and reduces investment in work in process.

An 8- to 10-layer device typically requires three to four days of processing if all process times are added together. This includes long oxidations typical of isoplanar type process steps or long p-well diffusions associated with complementary MOS (CMOS) processing. Yet the fact is that a wafer will spend at least three to four weeks in the fab area. This means that the wafer remains in inventory for 80 to 85 percent of the time. This delay is experienced for both MOS and bipolar processing. The photomasking step, in general, is the single longest interval between inventory points, excluding the long diffusion and oxidation referred to above.

The automatic masking line compresses many little steps into three compact processing steps:

- Prealignment
- Alignment
- Postalignment

Etching and inspection operations are still time-consuming. Nevertheless, the automatic masking line can save two to five days of inventory. The value of this inventory can approach one-fifth the cost of the wafer track equipment. Additional savings may result from yield improvements that accrue from reduced inventory time.

Plasma Resist Stripping

The plasma state is often referred to as "the fourth state of matter"— the other three states being liquid, solid, and gas. When a material is excited into a plasma by the removal of one or more valence electrons, its chemical properties change. Sometimes, new properties are encountered that can be used to advantage in semiconductor processing. There is now a high interest in plasma chemistry because researchers believe it will eventually be possible to eliminate "wet" chemistry altogether and substitute "dry" plasma chemistry. The effect would be to permit smaller geometries than can be achieved with wet chemistry. Furthermore, plasma chemistry appears to be more economical in its use of raw material and other resources, such as power. Plasma chemistry has been used to etch SiO_2, aluminum and polysilicon, and to strip photoresist. Researchers are actively working to extend the applicability of plasma chemistry still further.

3.2 Productivity Analysis

In plasma removal of photoresist, oxygen is converted by radio frequency excitation to a mixture of highly reactive atomic and ionized species or "plasma." As photoresist is almost entirely a hydrocarbon, it reacts very readily with the oxygen plasma. The reaction by-products are carbon dioxide and water vapor which are exhausted to the scrubbers. Nothing but photoresist and any other stray hydrocarbons are removed from the wafer. All residual traces of resist or other impurities are removed finally in subsequent standard pre-diffusion or pre-oxidation cleaning of the wafers. Any electrical charges produced in the wafer during the plasma stripping are removed by annealing the wafers for a few minutes in nitrogen between 600°C and 450°C. The use of a "Faraday cage" also minimizes the amount of positive charge that would otherwise enter areas of silicon dioxide exposed to the plasma.

The economics of plasma resist stripping make this technique attractive as long as no ill effects can be demonstrably attributed to it. For a fab that puts out 10,000 wafers per period about 16 to 20 lineal feet of chemical sinks are allocated to aqueous resist stripping. Fully outfitted chemical sinks cost about $1,600 per lineal foot.

The total cost of chemicals (excluding DI water and process gasses) ranges from 25 to 60 cents per layer of every wafer out each period, depending on fab yields and management. Of this, 5 to 10 cents per layer out per period is for wet resist stripping.

By contrast, the chemicals cost per layer out per period for plasma stripping is much less than 5 cents; this cost is for oxygen, the only chemical used. The tables used for processing cost $425 per lineal foot. No acid or solvent drains need be provided. Hazards in processing are considerably reduced, and throughput for 4-inch wafers exceeds 100 wafers per hour per machine.

Using the above figures for estimating savings, the minimum per period for a 10-layer device would be:

10 layers x 4½¢ x 10,000 wafers = $4,500 per period

if we assumed 100 percent processing and fab yields. Capital cost savings per lineal foot would be $1,175, total savings $1,175 x 20 = $23,500. Additional savings in hood, wafer, and drain hookup, $600. The total would be $24,100. Three plasma ashers to replace the chemical sinks should cost $27,000 each for a total of $81,000. Thus, net capital is $56,900, and payout should occur in 12.6 periods. A similar analysis would apply for plasma etching, except chemical savings per layer would probably be higher.

3.3 Major Facilities Operations

INTRODUCTION

Without a properly functioning Facilities group the entire semiconductor manufacturing operation would collapse. Consideration must be given to the role of this group in the planning, construction, and maintenance of the facilities required to establish and maintain circuits production. Environmental requirements both in-house and externally, the standards of purity for chemicals, gases, and DI water delivered to the manufacturing floor, and safety considerations are more rigorous than they have ever been.

To demonstrate the scope of activities of the Facilities group, the following list shows programs that usually fall under the aegis of this group:

- Site Selection
- Real Estate Acquisition
- Environmental Impact Study
- Architectural and Engineering Systems Designs
- Air Conditioning and Handling
- DI Water Plant
- Acid Waste Treatment
- Exhaust and Scrubbers
- Chemicals: Storage, Distribution, Handling
- Electrical Power Systems
- Gases and Hydrogen Alarms
- Cooling Water and Tower
- Noise and Vibration Control
- Compressed Air and Vacuum
- Clean Rooms
- Fire Protection and Safety
- Security
- Human Engineering
- Plant Construction
- Moving (Equipment, Furniture)
- Energy Conservation
- Equipment Installation
- Process Piping and Trenching

Some of the most important of these functions will be discussed briefly.

3.3 Major Facilities Operations

REAL ESTATE

Although the model adopted for this 1980 presentation of Manufacturing assumes a leased building at $1.00 per square foot per month, the following discussion on real estate is nevertheless relevant. A well run semiconductor manufacturing operation usually considers acquiring its own real estate outright.

Real estate costs vary widely. Current valuations in the Santa Clara Valley are, for the most part, in the range of $100,000 - $400,000 per acre. A fully developed site after its final expansion typically shows a ratio of land space to floor space of 2:1. In the planning stage, a land size recommendation is roughly eight times the size of the proposed initial building. Therefore, a 20,000 square foot building (approximately one-half acre) requires a plot size of 4 acres or 16,000 sq. ft. Land is required for access of public transportation (shipping and receiving), employee parking, landscaping, employee recreation, and expansion. Experience has shown that the average plant will expand its physical facilities to about four times its original size, leaving the land to building ratio of 2:1 already mentioned. The basic shell of a building offered for leasing to prospective semiconductor manufacturers by speculators ("build-to-suit") costs $40 to $85 per square foot to build, and offers little more than the shell itself, comfort facilities, basic power, city water, and sewage. Once leased, this type of building will cost an additional $230 to $250 per square foot when all construction and special services have been added.

ENVIRONMENTAL IMPACT STUDY

Local and county requirements usually demand an impact study delineating the advantages and disadvantages of siting a manufacturing facility within a particular community. A proper study should also anticipate the effect of the community on the facility. The major effects studied will deal with the contribution to air pollution, the strain on municipal services (particularly electrical power, sewage, and water), the effect on traffic patterns, noise and nuisance, housing availability, school population, and other related items. Such a study will also alert the manufacturer to the rate at which needed services will vary in cost and availability, as well as provide a picture of the costs necessary to control and monitor pollution in order to conform with local regulations. The cost of this study is usually close to $10,000 and extends over two man-months.

ARCHITECTURAL AND ENGINEERING SYSTEMS DESIGNS

The architectural design costs are normally based on a flat percentage of construction costs and average between 4 and 6 percent. Our model would require a cost of 4.5 percent of the construction cost. This model includes the design only of interior walls, ceilings, comfort facilities, building modification, seismic analysis, landscaping, investigation of roof loads and design. Mechanical engineering services

are based on either 2-1/2 times the facilities costs (air conditioning, electrical piping and support systems, gases, air and chemicals handling costs) times 6 percent, or else a flat 10 percent of these total costs. These formulae, or variations thereof, depend on whether or not the total project is to be managed entirely by outside services. Our model assumes the use of outside services.

DI WATER PLANT

This plant is one of the most critical aspects of circuits manufacturing (MOS device manufacturing in particular) since DI water quality affects both yield and reliability. The aim of this plant is to process any municipal water supply so as to remove particulates, bacteria, and all ionic contamination in order to obtain water of 18 megohm (million ohms) resistivity. The first stage of city water treatment is through filters of activated charcoal, diatomaceous earth, and cartridge-mounted membranes to remove organic and particulate contamination. In this early stage, chemicals such as chlorine and sulphuric acid are added in controlled amounts to adjust the pH (acidity level) and remove bacteria. The next stage is that of reverse osmosis (RO) in which the water is treated by forcing it through a semi-permeable membrane. In this operation, ionic and organic matter are trapped in the material of the membrane. The degasification step which follows next removes carbon dioxide. Two or more deionization (ion-exchange) stages follow in which cations and anions (positive and negative charge-carrying entities respectively) are removed. In the final stages, the water is subjected to ultraviolet (UV) illumination to destroy bacteria. After a final filtration step which admits particles no larger than one or two tenths of a micron in diameter, the water is allowed into the manufacturing area. Resistivity monitoring to ensure purity is done in-process as well as on the manufacturing floor. The entire DI water processing loop can be designed to reclaim some of the effluent from the manufacturing process back into the DI water processing loop.

DI water is evaluated with respect to the number of particles greater than a given diameter per unit volume of water and its electrical resistivity. This latter term is a measure of the resistance of a given volume (and shape) of water to electrical current flow. The higher the resistivity, the fewer the ions in the sample and the better the water is for semiconductor use.

A set of specifications of ultra high purity water approved by the ASTM (American Society for the Testing of Materials) is shown in Table 3.3-1. These specifications can be met only with very tight discipline and continuous monitoring of the components of the system.

3.3 Major Facilities Operations

Table 3.3-1

ULTRA HIGH PURITY WATER SPECIFICATIONS

1. Resistivity

   Sustained 18 megohms at 25°C as measured with flow-through cell and ohmeter as per ASTM-D-1125 (16 megohm @ 25°C minimum cutoff point).

2. Particulates

   Less than 500 particles held on 0.45 micron test filter, 37mm diameter, per liter of sampled water measured at 100 x magnification.

3. Bacteria

   Less than 1 colony per ml of sample incubated for 24 hours at 35°C in a suitable growth agar.

4. Organics

   Less than 1 part per million (ppm) as determined by Total Oxidizable Carbon (TOC).

5. Oxygen

   Less than 1 ppm dissolved oxygen as determined by Winkler test method.

6. Total Electrolytes

   Less than 5.0 parts per billion (ppb) as sodium determined by flame photometer as per ASTM (Method B) D-1428.

Source: DATAQUEST, Inc.

3.3 Major Facilities Operations

The operation of the DI water plant is critical. Consequently, a full-time engineering specialist is usually assigned sole responsibility for the continuous operation of the plant. For our model, a DI water plant capable of 75 to 80 gallons per minute (gpm) is assumed. This capacity is greater than necessary to facilitate the next stage of physical expansion.

In most municipalities, the cost of raw (city) water has almost doubled in the last two to five years thus making reclaiming of DI water attractive. The resultant disposal of smaller amounts of polluted water into the city sewage system also reduces municipal concern. In many new plants, the amount of water reclaimed ranges from 60 to 70 percent. The result is a corresponding reduction in the purchase of raw water. The greatest savings, however, are in the ultimate cost of processing DI water. Usually, raw water contains about 170 ppm of assorted electrolytes and organics. When the water is processed, the contamination levels fall below 1 ppm. When the cycled materials return, the levels are at or near 15 ppm. If this returned water were reprocessed, savings of nearly 40 percent in operating costs could be achieved. Estimates for initial capital costs for a new DI water plant should include a DI water reclaim system and a study to justify (or not) its extra cost.

The ultimate test of the quality of DI water processing and use in fabrication is in the preparation of MOS circuits. While bipolar circuits manufacturing can be done successfully on significantly reduced quality of DI water, MOS circuits will exhibit spurious behavior evidenced in voltage (particularly threshold voltage) shifts due to ionic sodium. Particulates also tend to reduce the quality of the gate oxide, subjecting the devices to premature breakdown or unwanted electrical conduction. Heavy metal ions will cause insoluble fluorides to be incorporated in thermally grown oxides, thus lowering the quality of the oxide.

ACID WASTE TREATMENT

Wafer fab areas are major potential pollutants. The discharged acids corrode concrete sewer pipes, gates, and pumps in the waste treatment facilities of the municipality. Cyanides and chlorinated solvents are highly toxic to sewer workers. Heavy metal ions attack the bacteria necessary to process waste in biological treatment plants. Hence, semiconductor plants must clean up waste effluents before discharging them into municipal sewage. This waste treatment requires expensive and sophisticated equipment for treatment and monitoring. In addition, the municipality levies fees for monitoring and disposal. Most city ordinances are formulated on the basis of preserving life and safety. Some ordinances require compliance to avoid nuisances, e.g., odors which might be obnoxious yet in themselves not constitute a danger to life.

Similar regulations apply to gaseous waste which must be exhausted, scrubbed, and monitored for compliance to set limits.

3.3 Major Facilities Operations

ELECTRICAL POWER SYSTEMS

Semiconductor manufacturing facilities use a great deal of electrical power. Large amounts of power are required for the diffusion furnaces, the RF generators, much of the support equipment such as air conditioners, and many other pieces of manufacturing equipment.

In addition to the total power requirements, the semiconductor facility has two other special needs. One is for very high quality electrical power that is free from noise or wide voltage variations. Second, a high quality ground is required for the electrical test equipment. In general, manufacturers have found it fruitful to separate power lines to testing equipment from power lines to other equipment. In particular, equipment that turns on and off by switches or relays can be especially troublesome because they may cause transient surges that result in unreliable testing by the test equipment.

Our model assumes 10,000 wafers out per period in 12,160 square feet of fab area. With the equipment listed below, power requirements are about 750 horsepower (HP). The equivalency is approximately 1 kilowatt-hour (KWH) per HP at an average cost of 7.5¢ per KWH. (Although the cost of gas is 16¢ per therm (one therm = 10,000 BTU -British Thermal Unit), if heat losses and inefficiencies are accounted for, the true cost is closer to 24¢ per therm.)

In the light of world events in the opening months of this decade, any costs now given for energy of any sort must be regarded only as tentative. It is reasonable to expect significant price increases and we will need to make adjustments in any calculations based on prices current at the time of writing. It has been mentioned previously that inflation and high energy costs are new challenges to management. Indeed, there is the problem of securing power allocations for startup of a new operation or the expansion of an existing one.

CLEAN ROOMS

In the push toward achieving VLSI capability, both MOS and bipolar devices are becoming increasingly sensitive to inadequately designed clean rooms. Today in 1980, the most general critical dimension being delineated in any feature of an LSI array is 5 microns. (However, by 1985, that dimension may very well be 3 microns and facilities built today will be handling this stringent requirement.)

A 2-micron particle will destroy 40 percent of a designed 5 micron line. The need, therefore, is clearly to control the size and amount of particulates contacting the wafer surface in process. This need has resulted in the development of an entire technology which demands that highly disciplined operators perform the required functions in the clean room environment.

3.3 Major Facilities Operations

Once the environment has been prepared and evaluated as clean, the main problems in keeping it so are personnel, traffic, equipment, and processing. These generate particles which migrate directly to the work or are redistributed by the air handling and ventilation systems into the process fab area.

Particle size is measured in microns (μ). A micron is one ten-thousandth of one centimeter. Otherwise expressed, it is 0.000039 inches. The need today is for a clean room of Class 100 standard. This means, by Federal Standard #209, an atmosphere controlled particle count per cubic foot of air containing not more than 100 particles of 0.5 microns in diameter and larger and not more than 1 particle of 4.0 microns or larger.

In semiconductor manufacturing, two methods using laminar flow principles are generally in use. One is the laminar flow room; the other is the laminar flow work station. Only laminar flow techniques can achieve Class 100 standards. Laminar flow means that air flow is in one direction and is non-turbulent; parallel elements of flow remain parallel in one plane. In a laminar flow clean room either a wall, or preferably the ceiling, is made of of High Efficiency Particulate Air (HEPA) filters and the other wall or floor is the exhaust grille. HEPA filter coverage ranges from 35 to 90 percent. The higher the coverage, the higher the air-handling capacity of the air conditioning system. Vertical laminar flow systems employ the ceiling as the filtered air entry and the floor or sidewall grille as the exit. This design takes advantage of gravity as well as the moving air stream to remove particles. Greater efficiencies are achieved. Such a facility will accommodate more people and more efficient work flow patterns. The principal disadvantages of the vertical flow system is the problem of construction.

These rooms have solid ceilings, as opposed to "drop" and "hung" ceilings; solid walls versus movable walls; sealed floors; filtered air input through the air conditioning system; positive air pressure with respect to the access corridors; sealed light fixtures; no ledges, cracks, or open utility holes; change rooms in which operators don clean room clothing; and double-access doors to each specific area. Entry to the clean room is best effected through an "air shower."

Fab expansion is limited by the ceiling. In general this approach is extremely expensive but absolutely necessary if high clean room standards are to be met. Where cost is a restriction, the difference in standards between room and station must be studied.

Control of temperature and humidity is very important for process control, as well as operator comfort. The diffusion processes generate enormous amounts of heat because of their high operating temperatures (450°C to 1,275°C or 824°F to 2,325°F). Moreover, the potentially toxic gas output of each furnace and its associated acid sink must be exhausted to the outside. Consequently, a tremendous load is placed on the air conditioning system and, for that reason, the diffusion equipment is isolated in a separate room with its own exhaust and air conditioning systems.

3.3 Major Facilities Operations

The photomasking room must typically be controlled to within plus or minus 2°F and less than 40 percent relative humidity because of the sensitivity of the photosensitive film (photoresist) to temperature and moisture. Further, most photoresists are sensitive to ozone (found in smog) so that the air into the area must be filtered through activated charcoal filters.

The laminar flow workstation is used when precise, economical environmental control of a specific area or operation is required. Such workstations usually house one or two operators and are self-contained with HEPA filters providing the cleanliness required. HEPA filters are 99.97 percent efficient by volume in filtering particles larger than 0.3 microns. In laminar flow stations, the air must have a velocity of 90± 20 feet per minute maintained up to one inch from the containment surfaces and the forward edge. If the rate of flow drops below 50 feet per minute, dust tends to settle on the work surface. A balance must be struck between laminar flow efficiency and operator comfort.

The cost of constructing a Class 100 clean room varies with plant location and percentage of HEPA filter coverage. Detailed design procedures will not be treated in this document but the following points are worthy of attention.

In the air handling system, if three-stage filtration is employed, the first filter stage is a roughing filter such as felt or glass wool. This filters out particles larger than 10 microns. The second stage filters are either fiberglass or electrostatic filters rated at 35 to 80 percent for particles above 0.3 microns. The third stage is the HEPA filter rated at 99.97 percent for particles above 0.3 microns. A fourth stage is usually added consisting of activated charcoal to remove hydrocarbons and ozone.

As much as 25 percent of the return air is re-used; it is repolished and its temperature and humidity readjusted.

To maintain the effectiveness of the clean rooms, manufacturing must institute strict discipline among their personnel with regard to clean room techniques. Clean room personnel clothing never leaves the clean room change area; purses, pencils, noncoated paper, and excessive facial powder are taboo; clean room clothing is changed regularly, as often as every day. This type of discipline or the lack of it will make or break a clean room facility, regardless of its appearance or its construction expense.

CHEMICAL WASTE TREATMENT AND CHEMICAL STORAGE

Separate drainage systems for chemical wastes are subject to local municipal codes as well as to compliance with ICBO (International Conference of Building Officials) plumbing and building codes. Since compliance with a code depends on a particular municipality, the following summary of an ordinance will explain the general tenor of such requirements:

3.3 Major Facilities Operations

Industries are prohibited from discharging into sewer systems wastes that would cause or interact with any of the following:

- Fire or explosion
- Interference with waste water systems
- Injury to the sewage facility
- Damage to life or safety of persons
- Strong or offensive odors
- Prevent effective maintenance or operation of the sewage system
- Overload the sewage facility
- Create a rise in treatment costs
- Cause a negative environmental impact
- Discoloration in the effluent from the sewage facility
- Cause a municipality to be in violation of the requirements of law. By July 1983, all cities should be treating wastes to the standards set by the 1972 Water Pollution Control Act (PL-92-500). Section 7509 of the Control Act forbids discharge and waste-water containing any of the following substances in excess of the maximum allowable limits:

0.1 mg/litre	arsenic
0.2 " "	cadmium
2.9 " "	copper
1.0 " "	cyanide
1.0 " "	lead
1.0 " "	mercury
0.2 " "	silver
0.5 " "	total chromium
3.0 " "	zinc

The requirements of the above Act will raise the cost to municipalities of sewage treatment. This, in turn, will add significantly to the cost of plant construction. Most cities are requiring industries to clean up their discharged wastes to help meet the stricter codes. Waste-water discharge permits are required. In addition to permit fees, monthly monitoring charges and sewage disposal charges are levied on the manufacturing facility. These are major expenses. A semiconductor waste treatment facility would cost upwards of $75,000 and would likely be sized for a flow of 30 gallons per minute. The cost includes monitoring, sampling, and metering systems.

Acid and chemicals storage facilities are required and should, if usage is high enough, be located in bulk containers away from the facility according to required (code) distances. For a 10,000 wafers-out per period facility, it is recommended that storage systems be designed and installed based on the following requirements:

Five 300 gallon acid storage tanks
Two 500 gallon chemicals storage tanks

3.3 Major Facilities Operations

Current estimates place the cost (including tanks, pumps, controls, and all piping for 100 foot maximum runs) at:

$20,000 per acid tank
$ 5,000 per chemicals tank

Pads, foundations, retaining walls - $100,000. Hence, the total cost is approximately $220,000.

Small volumes of other acids and chemicals should be stored in containers in well-ventilated enclosures which provide at least a two-hour fire separation from the rest of the building. They should be chained to prevent overturning and grounded to prevent static arcing.

Positive pressure exhaust systems are required and should provide 30 to 60 air changes per minute. Self-contained breathing equipment and protective clothing must be provided in the event of accidental spillage or leakage. Personnel must be trained in handling the chemicals both for normal usage and in the event of emergencies (fire, earthquake).

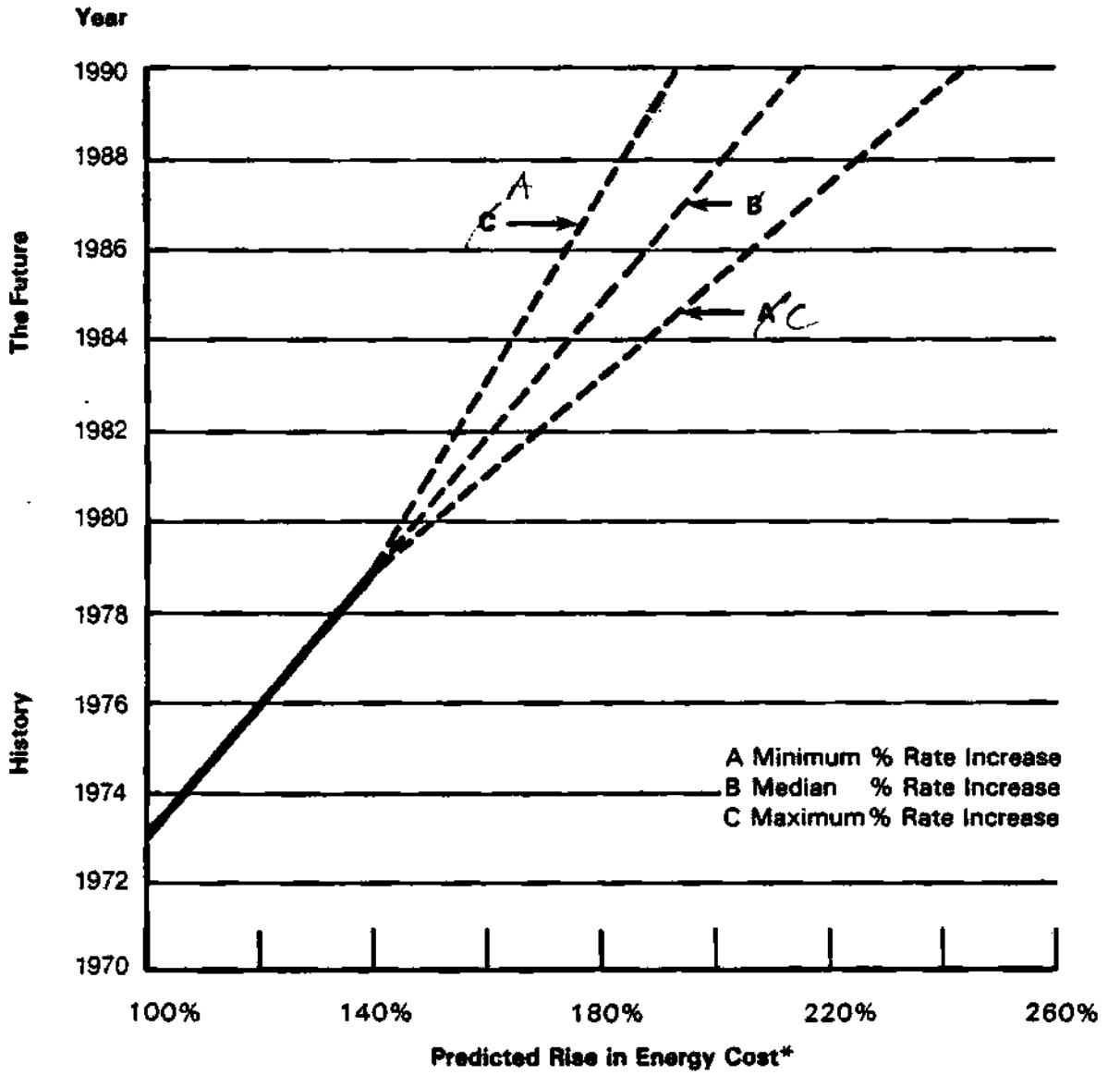
ENERGY CONSERVATION

Energy is increasing in cost at a very rapid rate. Electricity increased 8 percent in 1979 and is expected to increase 10 percent or more in 1980. The price of natural gas is expected to increase by 15 to 20 percent in 1980 having increased by 16 percent in 1979. Unpredictable fuel supplies are forcing new approaches to both business management aimed at conservation as well as to determining the effect on product cost. It has been demonstrated that a well considered energy conservation program can hold down both energy usage and costs. Reductions of 15 to 30 percent or more in usage are not unusual.

Figure 3.3-1 and the accompanying Table 3.3-2 indicate DATAQUEST's most optimistic projections on energy costs over this decade.

3.3 Major Facilities Operations

Figure 3.3-1
PREDICTED RISE IN ENERGY COST



*Relative to 1973 (1973 = 100%)

Source: DATAQUEST, Inc.

3.3 Major Facilities Operations

Table 3.3-2

EXTREMES AND MEDIAN PREDICTED RISE IN ENERGY COSTS

(The ensuing table is based on the Figure 3.3-1 curves, and assumes that a company paid a total of $100,000 for energy in 1973.)

Year	Probable Minimum Curve A	Probable Median Curve B	Probable Maximum Curve C
1973	$100,000	$100,000	$100,000
1979	$140,000	$140,000	$140,000
1980	$146,000	$147,000	$149,000
1985	$174,000	$180,000	$193,000
1990	$196,000	$212,000	$236,000

Source: DATAQUEST, Inc.

Since energy usage is an important and complex problem in the semiconductor industry, consulting services used for conservation programs should be close to the industry. Recent technological advances are responsible for several inexpensive electronically operated demand-control units. These units save power expense by avoiding the simultaneous operation of many major pieces of equipment. Such controllers as Trimax and Xencon are in ever expanding use as opposed to the 24-hour time clock systems. Each unit can be installed either on a demand-limiting or on-off basis for small to medium-sized facilities for $10,000 to $15,000, including the energy tax credit allowed. In situations where electrical power costs more than $1,000 per month, such units are highly desirable and the pay-back period is usually quite short. For larger, more complex installations with energy costs in excess of $1 million yearly, several other computer controlled systems are available.

3.3 Major Facilities Operations

EXHAUST, VENTILATION, AND POLLUTION CONTROL

In general, local Air Pollution District regulations are not formulated on the basis of specific pollutants. Most operate primarily upon whether or not particulate matter or visible plumes are discharged. However, semiconductor facilities discharge toxic chemicals containing oxide or nitrogen as well as flammable waste. The facility in this model is designed to follow the Threshold Limit Values (TLV) and the Lower Explosive Levels (LEL) recommended by the American Conference of Governmental Industrial Hygienists for storing, distribution, and usage of gases.

These toxicity and flammability limits are listed in Table 3.3-3 and have been established to guard against accidental release due to equipment failure, leaky cylinders, or other types of discharge. Piping systems for toxic substances must be constructed with welded fittings. Any other form of joint will leak. Better system reliability is obtained by limiting the number of welded joints. The system design must also make allowance for the possible maximum G-Force that might be experienced in the event of an earthquake. Safety valves proved effective during a recent earthquake at Livermore, CA. Storage areas require at least a 50 percent allowance above seismic design levels established by codes. Ventilation in these areas should provide at least 50 air changes per hour in an enclosure kept under negative pressure.

Table 3.3-3

TOXICITY AND FLAMMABILITY LEVELS

	Toxicity (TLV) in ppm	Flammability (LEL) Percent
Arsine	0.05	-
Phosphene	0.3	-
Diborane	0.1	(Pyrophoric)
Silane	-	(Pyrophoric)
Hydrogen Chloride	5	-
Ammonia	2.5	15.50
Boron Trifluoride	1	-
Hydrogen	-	4.00
Toluene	100	1.27
Xylene	100	1.0
Hydrogen Fluoride	3	-
Hydrogen Peroxide	1	-
Isopropyl Alcohol	400	2.02
Methanol	200	6.72
Acetone	1,000	2.55
Methyl Ethylketone	200	1.81
Trichloroethylene	100	-
Acetic Acid	10	5.4
Nitric Acid	2	-
Phosphoric Acid	1 mg/M^3	-
Sulphuric Acid	1 mg/M^3	-

Source: Milton S. Kiver Publications, Inc.
DATAQUEST, Inc.

3.3 Major Facilities Operations

PLANT CONSTRUCTION, DESIGN, AND LAYOUT

The construction phase of a semiconductor facility is an important and sensitive stage which consumes almost eight months. Although it includes many conventional construction techniques, it is characterized by the multiplicity of highly technical approaches peculiar to this industry.

Our model calls for ten-foot high ceilings above the work area so that the laminar air flow required for the clean rooms will be efficient. Above the ceiling, but below the roof, a six-foot high space is called for. This establishes a very necessary area for gas piping, ducting for air-conditioning, pump location, and controls. Such an area, though expensive to construct, will, in fact, guarantee the integrity of the fab area and allow maintenance personnel to avoid the precincts of the actual manufacturing area.

Trenching, as a construction technique, does at a physically lower level what the existential space does above the ceiling. It saves valuable manufacturing floor space by relegating service corridors to below ground. If the space is properly sealed, contamination of the fab area due to leakage of chemicals is avoided. Trenching tends to avoid wall openings for pipes and control functions which otherwise would have required absolute seals around each opening. Floor drains (required for cleanup) and safety showers are also more easily installed and maintained with floor trenches.

Clean rooms are very expensive. They also require workmanship of the highest caliber. HEPA filter coverage for the ceiling ranges from 35 to 90 percent in most installations. The requirement for an air plenum above the ceiling, in addition to the weight of the filtration apparatus, adds an extra burden of approximately 15 lb. per square foot to the roof load. This requirement almost always exceeds the support capabilities of most roofs and structural strengthening is required.

Flooring materials must be acid-resistant. An example of such material is "Mypolam." When the flooring material is extended 12 inches or more up the side of the walls, it eliminates floor-to-wall seams but adds considerably to the cost of the facility. The costs of such material runs to three or four times that of vinyl.

Chemical storage and supply installations placement off-site is not only highly desirable but in most cases is also a necessity. Better control of chemical usage and employee safety are guaranteed by this construction technique. Federal and state safety requirements for this kind of installation require not only isolation but also "catch-basin" arrangements beneath the storage tanks. In earthquake-prone areas, seismic studies dictate construction requirements. For our model, an installation of five acid tanks and two chemical tanks is required at a cost of $220,000. Though it is difficult to prove, we believe that the added cost of these tanks is recovered through better control of chemical usage and inventory and through improved yields. The improved yields result because it is not necessary to have extra personnel passing through the clean room to deliver chemicals. Every time a new worker enters a clean room, the dust particle count increases. There is also less danger of chemical spillage when chemicals are piped in rather than being delivered in bottles.

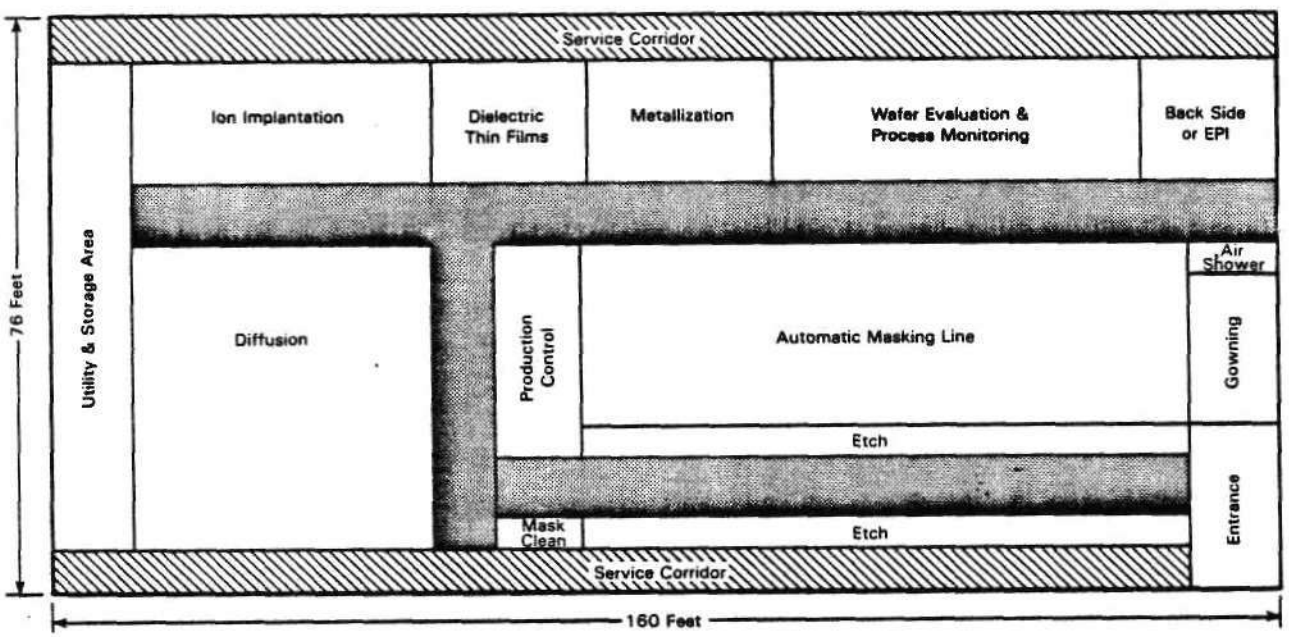
3.3 Major Facilities Operations

Construction of support (i.e., non-Fab) areas such as Wafer Sort and offices conform more to routine construction requirements and are much lower in cost. Standards exist for office size, ceilings, walls, and floors in most industries and these standards are easily applied to this phase of construction.

In Section 3.0 under the heading "Current Trends," some general layout and design philosophies are discussed. These, for the most part, have been adopted in the illustrative block area diagram in Figure 3.3-2 used as our Wafer Fab model.

Figure 3.3-2

MANUFACTURING BLOCK AREA DIAGRAM



Source: DATAQUEST, Inc.

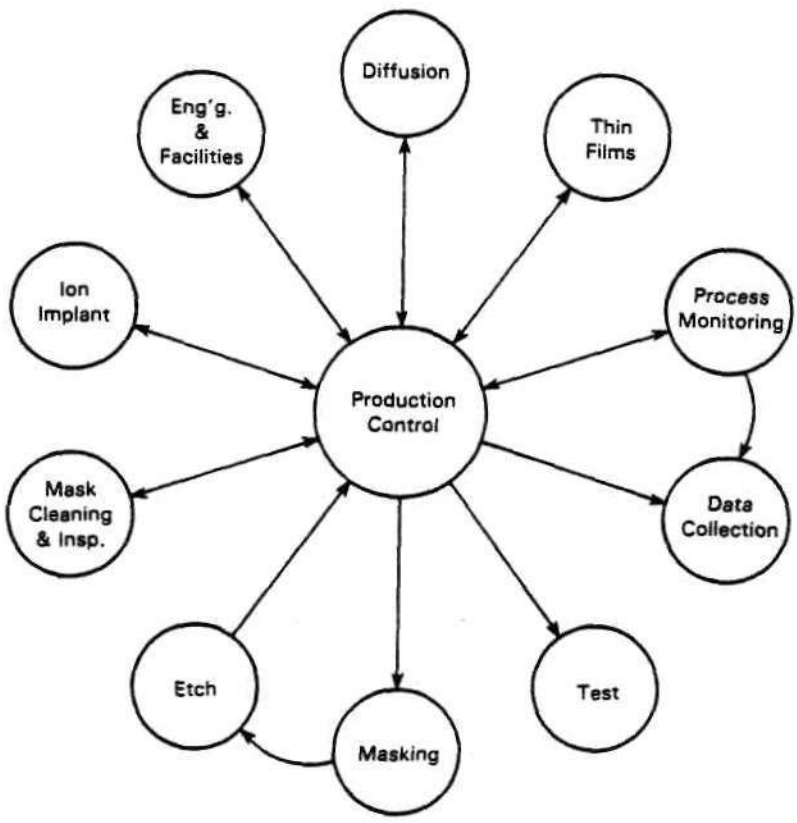
3.3 Major Facilities Operations

The heat and dust generating portions of the diffusion furnaces and ion implanter are sealed off by firewalls from the clean rooms and processing areas. Service corridors ring the Fab so that stations using wet chemicals can be serviced from outside the controlled environment. The result is a lower heat load, better particulate control, and reduced traffic across the manufacturing floor.

Figure 3.3-3 shows schematically the movement of data and material during the manufacturing process. The production or manufacturing control center is the heart of the operation and the block area diagram (Figure 3.3-2) reflects this fact. There is a unidirectional, closed-loop relationship, for instance, among Production Control, Masking, and Etching. Production Control accesses all areas by means of "pass throughs" so that each area can maintain its integrity. Entry to the factory floor is through three stages: primary entrance, gowning room, and air shower. At each stage one becomes progressively cleaner.

Figure 3.3-3

DATA AND MATERIAL FLOW



Source: DATAQUEST, Inc.

3.3 Major Facilities Operations

Table 3.3-4 shows space allocation for the specific manufacturing areas. The Diffusion area is sized to accommodate five banks of 4-stacker diffusion furnaces. This might be useful if the model is to be adapted for 8-layer bipolar or 10-layer CMOS devices. Space allocated for the automatic masking line is enough for eight or more projection aligners. Amost 80 lineal feet have been reserved for etch and inspection stations. The relationship between ion implantation and dielectric thin films areas is such that the dividing wall can be moved so as to accommodate the operation with the greater need. For bipolar processing, epi operations will replace the backside processing required for the 16K DRAM we have adopted for the 1980 model.

The entrance to the Fab area has been deliberately staged to conform with clean room requirements. Data collection has been removed from the manufacturing floor since computer record keeping and data processing still involve paper work that would be intolerable there.

Table 3.3-4

WAFER FAB SPACE ALLOCATION

Function	Space Allocation (Square Feet)
Masking	1,896
Service Corridors	1,848
Diffusion	1,560
Etching	1,264
Wafer Fabrication	768
Utility and Storage	704
Ion Implantation	624
Metallization	384
Dielectric Films	320
Production Control	308
Backside Processing or Epi	288
Gowning and Air Shower	268
Entrance	264
Mask Cleaning and Inspection	132
Subtotal	10,648
Aisles, Walls, etc.	1,512
Total	12,160

Source: DATAQUEST, Inc.

3.3 Major Facilities Operations

COST CUTTING

Perhaps the earliest example of cost cutting was the elimination of windows from the Pyramids. Unfortunately, this is no model to emulate in the semiconductor industry. Earlier, we discussed HEPA filter coverage for clean room ceilings as being between 35 and 90 percent. Considering the need for Class 100 ratings in the production of small geometry devices for VLSI (1.5 to 3.0 micron lines and spaces), one can only regard filter coverage below 75 percent as reckless. Loss of yield over the useful life of the Fab makes cost cutting in construction of a state-of-the-art facility an extremely delicate exercise ("penny wise and pound foolish").

Nevertheless, there are areas in which construction expenses can be reduced or avoided without penalty. Chilled water storage, although desirable, is not considered necessary as long as the chilled capacity lies below 500 tons. Above this limit, however, rapidly increasing energy costs make savings realized by chilled water storage attractive. At least 85 percent efficiency should be achieved to justify this expense.

The existential space between Fab ceiling and roof, as noted above, is expensive to construct. In lieu of this approach, some plants simply install a maze of catwalks above the "dropped" Fab ceiling. However, this approach necessitates, in most cases, that maintenance crews enter this existential space from within the manufacturing area. The resulting contamination problems are severe even if done during off-production periods. Catwalks usually accommodate the piping and ductwork and are not necessarily near the problem area. The entire Fab area is usually shut down to accommodate the maintenance exercise with resulting loss of revenue. The catwalk approach to construction also results in loss of positive pressure in the room below. Finally, this type of construction makes any attempt at expansion impossible without gross contamination in any adjacent manufacturing operation.

The point of this entire section is to sensitize the reader to the ramifications of reducing expenses in high technology manufacturing. With care, a diligent engineer can find many areas in which appreciable savings can be effected without downstream damage. In Facilities Engineering, as in Process Engineering, there is no such thing as a "small engineering change."

TIME REQUIREMENTS

Because of the special facility requirements of the semiconductor industry, it is usually more effective in the long run to construct a facility rather than to try to adapt an existing building. Prior to the construction phase, particular attention must be given to the design of the facility so that all special requirements are met. Attention must also be given to the time required to install support equipment, plumbing, air conditioners, and other hardware before the facility can be used. It will also require time for equipment to be ordered, manufactured, shipped and installed--such as large equipment used for gas storage and deionizing water.

3.3 Major Facilities Operations

The time required to design, construct, debug, and build a facility ranges from one and one-half to two years. Construction time is affected by such factors as strikes, material shortages, late deliveries, adverse weather, and changed orders due to imperfect planning.

Figure 3.3-4 illustrates the timing for the building of a new manufacturing facility. Time can be saved by moving into an existing facility provided extensive modifications are not needed to render it adequate. Very often, however, considerable tradeoffs have to be made, particularly in the areas of working space and material flow.

If a building is started from scratch, it can take (barring any serious disruptions) up to 15 months from the design stage before the initial engineering runs are processed through the area.

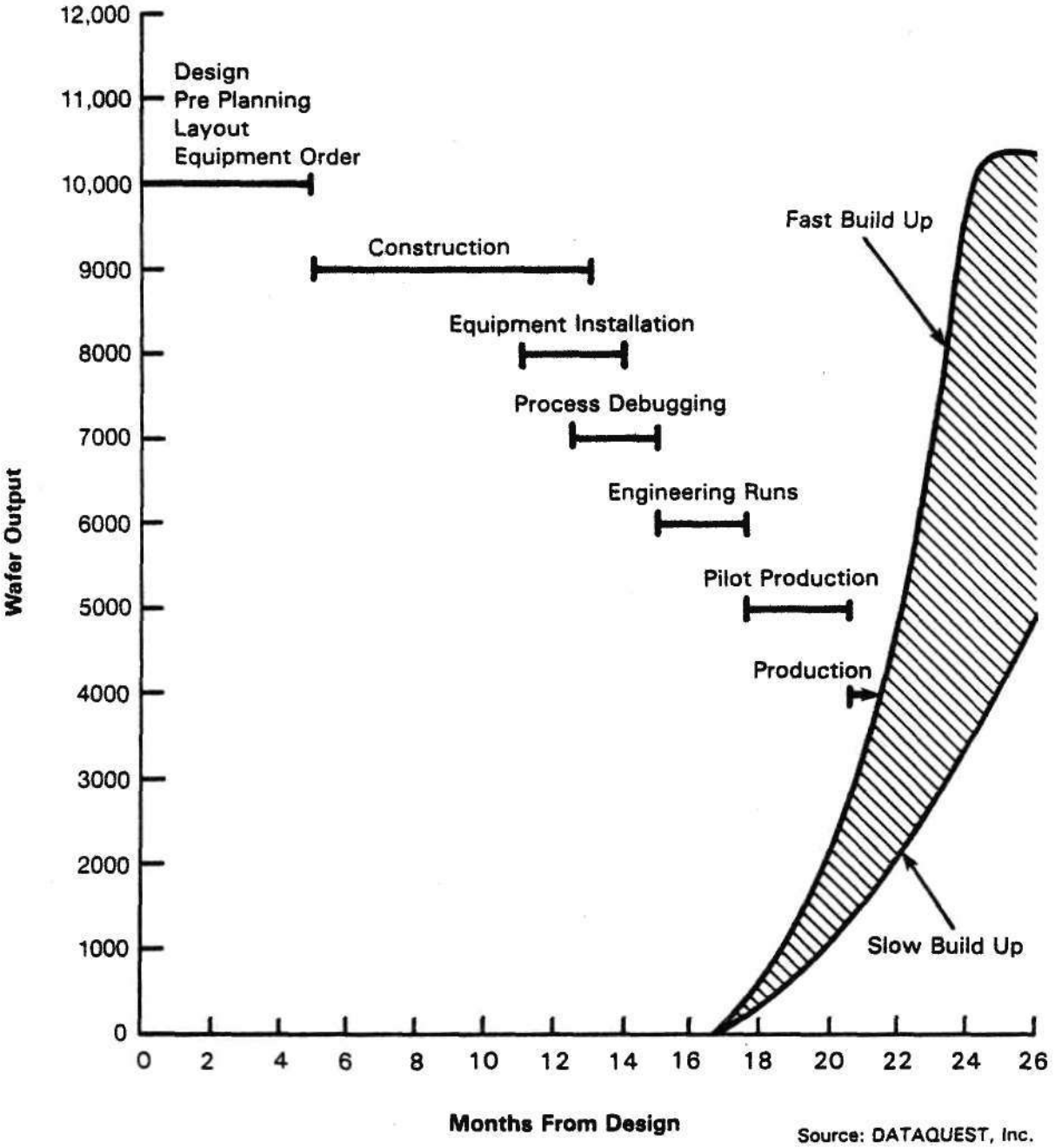
It should be noted that for a new facility, the slowest area to reach production is almost always wafer fabrication and its processes. Test equipment and assembly equipment can usually be debugged and be on-line at least several weeks before wafer fabrication processes. The time required to debug equipment and processes can vary from company to company.

Most companies choose to install the latest and best manufacturing equipment in any new facility for two reasons: (1) the equipment becomes obsolete so rapidly that it is not always economical to install older models, even though they are well proven machines; (2) most IC companies buy their equipment from the same vendors and, therefore, all have the same basic manufacturing capability. The advantage, however slight, supposedly goes to the company getting the newest, best equipment into production first. More often than not, however, the latest models have operating problems which may take days or even months to resolve.

In the wafer fabrication area, there is a close interaction among processes, process equipment, and yields. New equipment at a process step often forces a redefinition or redevelopment of that process, sometimes causing it to be subtly different from the previous process. Manufacturers then find that the process has worse yields than previously. The subsequent questions raised are: (1) is the problem one of equipment, process, or both? (2) which process steps are involved? Considerable time may be required to answer these questions and to find an acceptable solution.

Wafer volume build-up is loosely tied to the availability of trained operators. Even experienced operators have to be retrained on new equipment, which lowers their productivity for days or weeks at a time. During the build-up of volume, output per operator is not necessarily a satisfactory indication of efficiency since most of the efforts go into the establishment of the work-in-process inventory. Further, operators are hired in advance of the actual growth of volume for purposes of training and in anticipation of the future need for their services.

Figure 3.3-4
START UP TIME REQUIREMENTS



Source: DATAQUEST, Inc.

3.4 Manufacturing Cost Analysis

INTRODUCTION

Our 1980 model and cost analysis is based on an MOS device: the sixteen thousand bit dynamic random access memory (16K DRAM). The choice of device has been vindicated by the enormous strides the MOS market has made in recent years. Although both bipolar and MOS markets have expanded significantly, the MOS market has moved at a rapid pace and now exceeds the bipolar market. MOS speeds have increased through clever design and process, and circuit densities have also increased. The future of MOS technology and markets looks even brighter than previously forecast.

For the model a 6-layer process was chosen as the simplest way to fabricate a workable 16K DRAM device. In fact, many companies use an 8-layer process with an isoplanar structure and threshold shifting implantation. The bipolar process shown in this chapter uses 8 layers. It often employs an isoplanar approach involving an extra mask. In both technologies, a deposition of silicon nitride is necessitated and an accompanying long oxidation to grow a thick oxide in the field regions of the device. The 3-inch wafer used in previous DATAQUEST models has been replaced by a 4-inch wafer.

The assumptions made in developing wafer and die costs are listed below. Companies were surveyed and the data analysed for certain cost elements. The standard deviations represent, for the most part, regional, management, and accounting differences.

The Equipment List shows a dramatic increase in dollar costs from the equipment lists of our previous manufacturing models partly because of inflation and partly because of the high cost of developing and marketing sophisticated new equipment with a very short product life cycle, which must work with much finer geometries.

Facilities costs are summarized. These costs, too, have shown a rapid increase due to escalation of labor rates and price inflation of metals (e.g., copper) used for piping and petroleum-based products (e.g., PVC, formica, mypolam). Also included in this section are fab construction and planning schedules.

Assembly is contracted out as a service. E-sort and Final Test costs are predicated on a dollar cost per hour basis which covers labor and materials.

3.4 Manufacturing Cost Analysis

ASSUMPTIONS

The assumptions used to develop the model for this cost analysis have been summarized below for easy reference. Although a 6-layer MOS model has been used, it can readily be adapted to an 8-layer bipolar model, for example, by making adjustments in the equipment list, direct labor rate, and package type. Facilities costs would remain essentially unchanged. Wafer Fab materials can be ratioed to accommodate the extended processing.

Technology

a. 16K DRAM, MOS N-channel
b. 6-layer double-poly process
c. 5 micron geometry
d. 140 mil x 140 mil chip size (= 20,000 mil^2)
e. 16-pin DIP plastic package
f. 4-inch diameter silicon wafer
g. 1:1 projection aligners (UV)
h. Negative photoresist
i. Wet etching
j. Plasma ashing of photoresist

Production

a. Two full shifts per day (skeleton graveyard shift mainly for maintenance)
b. Seven hours effective work per shift
c. Five day week = 20 days per period
d. 12.5 productive periods per year
e. 25 percent benefit package including shift premiums
f. Minimum throughput at any step = 60 wafers per hour
g. 10,000 wafers out per period
h. Productivity at approximately 42 wafers out per operator per week (6 layers)
i. All assembly operations offshore

Salaries (without fringes)

Range	Typical	Average Annual Salary
Operators	$ 8-10,000	$ 8,750
Technicians	$14-18,000	$14,000
Supervisors	$20-24,000	$21,000
Engineers	$28-32,000	$30,000
Operations Manager	$35-45,000	$40,000

(Note: These salaries could differ widely outside the Santa Clara Valley in California.)

3.4 Manufacturing Cost Analysis

Yields

a.	Cumulative Fab yield	75%
b.	E-Sort (16K DRAM)	16%
c.	Assembly yield	90%
d.	Final Test yield	80%

Facilities

a. Building rented as shell at $1.00 per sq. ft. per calendar month
b. Space rented = 25,000 sq. ft
c. Minimum of 15 percent inflation rate on construction, materials, and equipment
d. All facilities and services supplied from scratch
e. All design services contracted to outside engineering firms
f. All chemicals (except photoresist) to be pumped into the Fab Area from storage tanks to points of use
g. Masking can accommodate up to 10 projection aligners
h. Diffusion can accommodate 20 furnaces
i. Fab area = 12,160 sq. ft; E-Sort, Test, Offices = 12,840 sq. ft. total

Some fab allocated.

Equipment

a. Highly automated operation
b. Convertible for use on 5-inch diameter substrates
c. Equipment will be used eventually on 2 to 3 micron gates and shallow junctions (less than 1.0 micron)
d. Need filled for data collection and information management to facilitate trend analysis

FACILITIES COST ANALYSIS

The costs reported here cover those items and projects listed in the Introduction to Section 3.3 above:

Fab Construction	$ 884,000
Wafer Sort, Test Area, Offices, etc., Construction	513,000
DI Water Plant	350,000
Air Conditioning	438,000
Chemical Storage	220,000
Electrical Power Plant	258,000
Equipment Installation	320,000
Cooling Water and Tower	82,000
Architectural and Engineering Designs	493,000
Other Equipment Systems and Alarms for Fab and Test	274,300
Grand Total	$3,832,300

5% Equip cost.

3.4 Manufacturing Cost Analysis

(Note: No allowance has been made in this section for contingencies such as inflation, moving and storage, cost overruns, and other demons of real life. A practical figure ranges from 10 to 15 percent of the above grand total.)

It must be mentioned here that the term "construction" relates to specific items such as which include ceilings, floors, perimeter walls, roof screens, trenching.

WAFER COST ANALYSIS

Fixed Costs

Fixed monthly costs are listed in Table 3.4-1. Equipment costs have established a new plateau for a fab producing 10,000 wafers per period. Depreciation on this equipment exeeds the combined total of all other fixed monthly costs. However, the productive life of most of this equipment is much shorter than the 60 months allowed for its depreciation. The industry would no doubt welcome a depreciation period of 36 months since equipment represents the major capital outlay. As it ages, very little of this equipment can be adapted to challenge competitively the demands of new technology. Consequently, this protracted depreciation period constitutes a major drawback for would-be entrepreneurs.

The cost of electrical power is by no means insignificant and could rise more sharply over the next few years at rates more rapid than indicated in Figure 3.4-1. It would seem that the only answer to the inflationary spiral in which equipment and energy costs are entrapped lies in increased productivity and yields. This fact cannot be repeated too often to planning and production teams.

3.4 Manufacturing Cost Analysis

Table 3.4-1

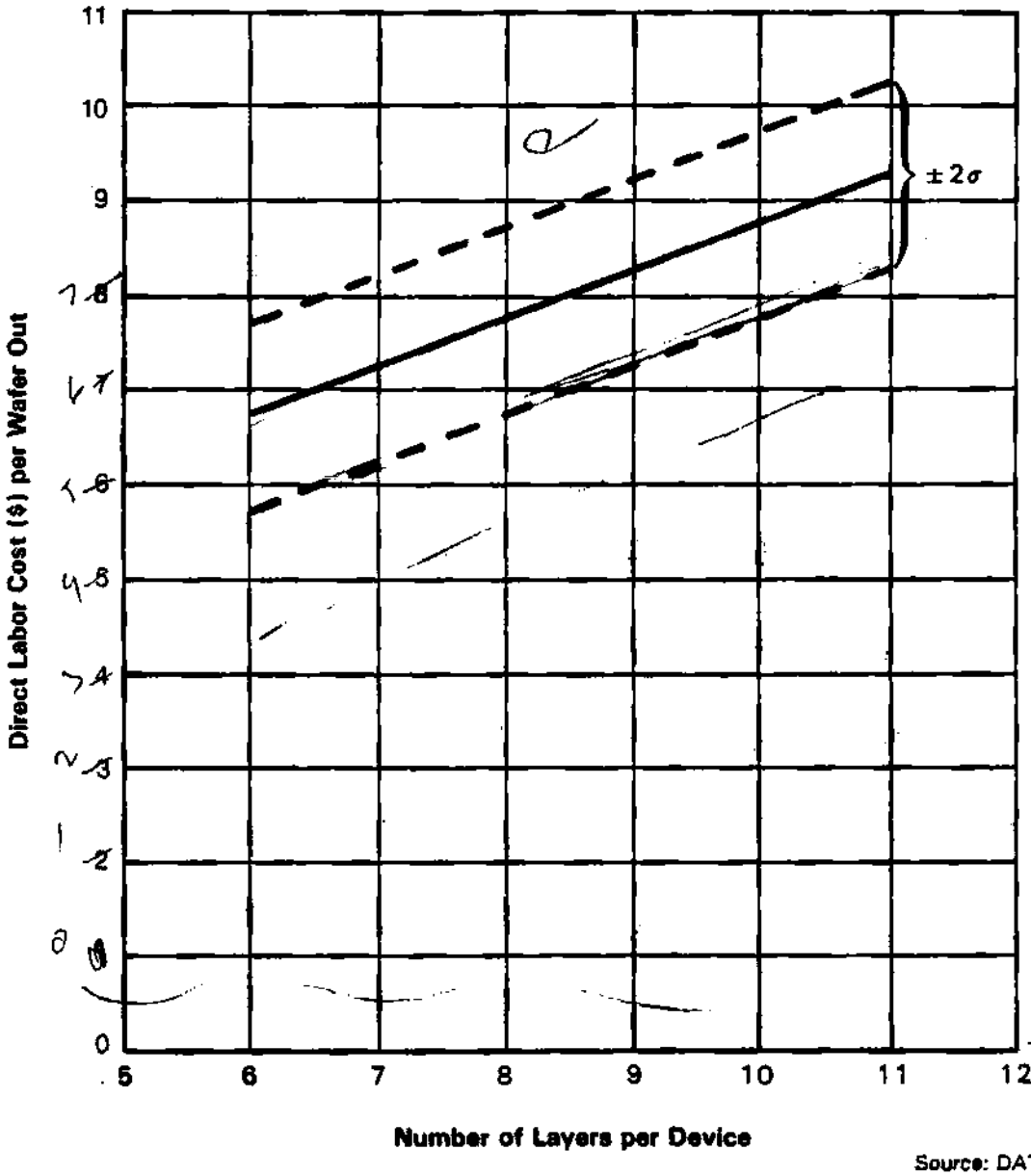
FIXED MONTHLY COSTS

Rent: 25,000 sq.ft. @ $1.00 per sq. ft., per calendar month - taxes and sewage included	$ 25,000
Sewage and Water Monitor: per calendar month	2,000
Electrical Power: 750 HP @ 1 KWH per HP, 75% rating, 7.5¢ per KWH, per calendar month	28,350
Gas: 3300 Therms @ effectively 24¢ per Therm	800
Depreciation:	
- Fab Construction: $884,000; 360 months	2,456
- All other construction: (E-Sort, Test, Offices) and Systems, etc., $2,948,900; 96 months	30,718
- Equipment: $6,364,950; 60 months	106,083
Total per calendar month	$195,407
Total per period	$180,376
For 10,000 yielded wafers out per period, the cost per wafer (Table 3.4-3, Item I)	$ 18.04

Source: DATAQUEST, Inc.

3.4 Manufacturing Cost Analysis

Figure 3.4-1
DIRECT LABOR VS. NUMBER OF DEVICE LAYERS



Source: DATAQUEST, Inc.

3.4 Manufacturing Cost Analysis

Table 3.4-2 displays cost data gathered from manufacturing houses on both coasts and the southern United States. The average number of layers processed by these companies per device was 8.36 with a standard deviation of 1.44. While most companies are still processing 3-inch wafers predominantly, there is considerable expertise in the use of 4-inch material.

Table 3.4-2

VARIABLE (VOLUME SENSITIVE) COSTS

(Data Gathered From Company Surveys)

Wafer Fab (75% Cumulative Yield)		
Materials:		
- Silicon	$13.33	
- Masks	0.25	
- Chemicals	3.00	
- Indirect Materials	2.25	
- Gases	2.00	
- DI Water	0.10	
Cost per wafer out (Table 3.4-3, Item II)		$20.93
Labor:		
- Direct (adjusted for 6-layer process)	$ 5.75	
- Indirect	2.59	
- Allocated	13.53	
Cost per wafer out (Table 3.4-3, Item III)		$21.87

Source: DATAQUEST, Inc.

3.4 Manufacturing Cost Analysis

Materials

In general, there was more variation in costs due to yields rather than to a difference between processing costs of 3-inch and 4-inch substrates. Raw silicon wafer costs varied from $9.00 to $11.00 depending on whether epitaxial material was used or not. Another striking fact was that bipolar and MOS houses showed very close correspondence in wafer costs where photomasking techniques, wafer diameter, and the number of layers per device were similar.

Mask costs varied tremendously depending on the mix between projection and contact printing. For well-established products with a long history in the marketplace, the data isolated showed projection mask costs well below 10¢. Our model loads this cost up to 25¢ to reflect shorter product lifetimes, superseded designs, new development costs, breakage, and yield losses from mask cleaning and inspection. The typical mask costs in contact printing ranged from $4.50 to $5.50 reflecting, again, the differences in yields and wafer diameters. Additional cost variations may have been due to the fact that some manufacturers buy their masks while others produce them in-house.

DI water usage ranged from 80 gallons to 260 gallons per yielded wafer out. Typical was 140 gallons per wafer. DI water costs per gallon ranged from 1.0¢ to .65¢; the typical cost is 0¢ per gallon. No distinction was made between 3-inch and 4-inch wafers. The highest DI water cost per wafer out was $2.60 and this cost included DI plant amortization. In the Santa Clara Valley, DI water costs typically 1.0¢ per gallon. In the South, Southwest, and East, costs tended to be lower. More DI water was used in some cases on 7-layer devices than on 9-layer devices although cumulative yields were similar. In summary, DI water usage was largely uncontrolled though monitored.

Labor

The survey on labor rates was interesting. The data are graphed in Figure 3.4-1 for direct labor costs per wafer out. If Figure 3.4-1 is used in conjunction with Figure 3.2-7 which shows the variation of operator wafer output vs. the number of masking layers per device, it is readily seen that the direct labor cost per wafer out is 25 percent or more above the standard labor cost of $4.20.

Indirect labor costs were very close to the mean value of $2.50 per wafer out.

Allocated labor costs per wafer out averaged $13.23 with a standard deviation of $2.71.

3.4 Manufacturing Cost Analysis

Table 3.4-3 shows the total cost per wafer out for the N-channel MOS model used as being $60.59 per wafer out. The percentage contributions of the various cost elements are also shown.

Table 3.4-3

COST PER WAFER OUT

			Cost		Percent
I.	Fixed monthly costs (From Table 3.4.1)		$18.04		29%
II.	Fab materials		20.93		35%
III.	Fab Labor:				
	Direct	$ 5.75		9.5%	
	Indirect	2.59		4.3%	
	Allocated	13.53		22.2%	
	Subtotal		21.87		36%
	Total		$60.84		100%

Source: DATAQUEST, Inc.

DIE COST ANALYSIS

Analysis of the survey data indicate that isolation of testing costs incurred by specific device types is difficult and unrewarding. The trend is toward consolidating the E-sort and Final Test areas. Costs are then allocated to each product type according to the time each spends on testers. The average tester cost per hour was found to be $48.86 per hour with a standard deviation of $7.97. Device yields on 16K DRAMs tend to lie between 15 and 25 percent at E-sort. This figure is up from the 5 to 15 percent yields seen in 1978. The less bullish figure of 16 percent was adopted for

our model. At this rate, slightly more than five 3-inch wafers can be tested per hour or slightly less than four 4-inch wafers per hour. Paradoxically, but not surprisingly, higher yielding wafers may cost more to test because a good die is tested more completely—testing ceases for a "bad" die at the first failure. A large component of the testing costs is for wafer placement or "setup" during which the wafer is mounted and inspected and the probes set.

Table 3.4-4 details the calculation of costs for the packaged die. Our model assumes assembly operations are done "offshore" (Malaysia, Mexico, Philippines, Southwest Asia), following the established trend within the industry.

An assembly cost of $0.230 is assumed for the 1980 model versus the $0.153 for the 1977 model. Plastic packages are increasing in versatility. Important advances have been made recently in heat dissipation and, at present, they represent a cost advantage over ceramics of three to four times.

3.4 Manufacturing Cost Analysis

Table 3.4-4

PACKAGED DIE COST (16-Pin DIP Plastic)

E-Sort (Wafer Sort)	
• Cost per wafer at E-Sort = (Cost per hour) - (No. of wafers sorted per hour) = $48.86 ÷ 4 =	$12.2200
• E-Sort cost per gross die = $12.22 ÷ 550 =	$0.0222 (a)
• Wafer Fab cost per gross die = $60.59 ÷ 550 =	$0.1102 (b)
• Total cost per gross die	$0.1324 (a+b)
Cost per net die at E-Sort 0.1324 ÷ (16% E-Sort yield)	$0.8275 (c)
Assembly	
• Cost of die from E-Sort =	$0.8275 (c)
• Assembly cost per gross die =	$0.2300 (d)
• Assembly yield =	90%
• Cost per gross die = (c) + (d) =	$1.0575 (e)
Therefore, cost per net die = (e) ÷ 90% =	$1.1750 (f)
Final Test	
• Test time per die =	15 sec.
• Test cost per second = $48.86/3600 =	$0.01357(g)
Therefore, Test cost per gross die = (g) x 15 =	$0.2036 (h)
• Total cost per gross die = (f) + (h) =	$1.3786 (i)
• Final test yield =	80%
Therefore, cost per net die = (i) ÷ 80% =	$1.7233 (j)
Pack and Ship	
• @ 100% yield =	$0.0200 (k)
Therefore, (j + k) = Total Cost Per Net Die =	$1.7433

Source: DATAQUEST, Inc.

3.4 Manufacturing Cost Analysis

EQUIPMENT LIST/COST

The detailed equipment lists for the N-channel MOS are given in Appendix A. A summary of costs by area for the NMOS and bipolar models is given in Tables 3.4-5, -6, and -7.

Table 3.4-5

EQUIPMENT COSTS : N-CHANNEL MODEL

	Capital Cost	Percent of Total
Diffusion Area	$1,339,450	21.0%
Masking Area	2,283,300	35.9
Deposition Area	1,039,700	16.3
Fab Support and Test Areas	1,287,900	20.3
Backside Processing	414,600	6.5
Grand Total (6½% Tax included)	$6,364,950	100.0%

Source: DATAQUEST, Inc.

3.4 Manufacturing Cost Analysis

Table 3.4-6

EQUIPMENT COSTS: BIPOLAR MODEL

Bipolar Model (8 Layers)

N-channel model (above)	$6,205,200
Omit Backside Processing	$ (414,600)
Add to Diffusion Area:	
4 Furnaces and Peripherals @ $35,000 each furnace	140,000
Add to Deposition Area:	
2 Epi Units @ $450,000 each	900,000
Add to Masking Area:	
2 Perkin-Elmer Aligners @ $175,000 each	350,000
Grand Total (6½% Tax Included)	$7,180,600

Source: DATAQUEST, Inc.

Table 3.4-7

COST OF A 1980 NMOS WAFER FAB

	Capital Cost	Percent of Total
Equipment	$ 6,205,200	62%
Facilities	3,832,300	38%
Grand Total	$10,037,500	100%

Source: DATAQUEST, Inc.

3.4 Manufacturing Cost Analysis

DEVICE MODEL

The device model was adopted for illustrative purposes only. Table 3.4-8 shows the N-channel MOS double-poly process flow chart for the 16K DRAM. The steps shown are inventory or accounting points at which in-process yields are monitored. The individual steps highlight the major process operations dealt with in Section 3.1. Figure 3.4-2 shows in schematic cross-section the definitive DRAM memory cell. This new configuration uses a single N+ diffusion thereby allowing economical usage of the silicon wafer. The double-polysilicon structure allows the vertical dimension to be used for switching instead of the horizontal, again saving valuable "real-estate."

Table 3.4-8

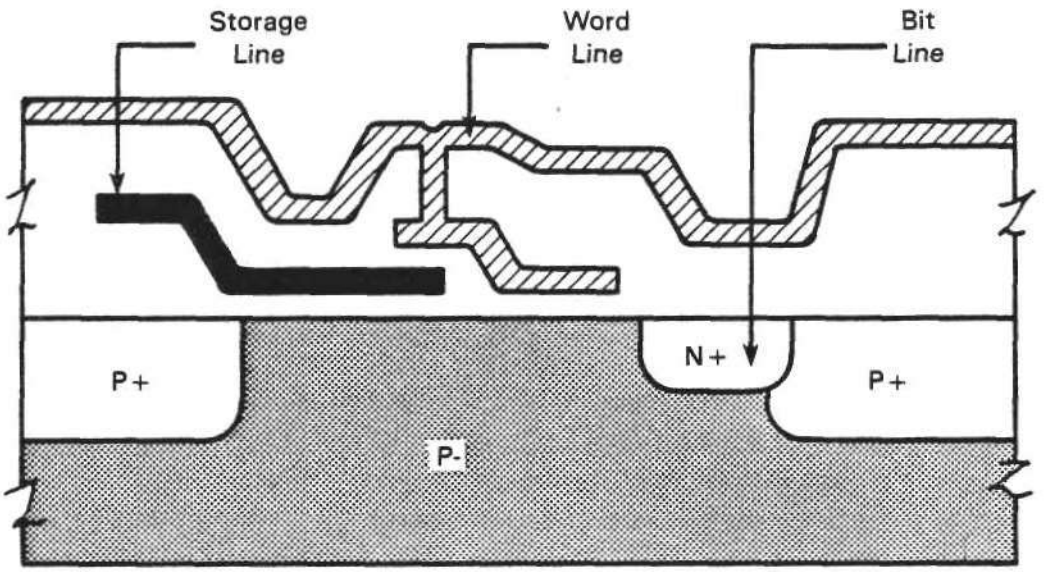
DOUBLE-POLY PROCESS FLOW CHART - 16K DYNAMIC RAM

1. Initial Oxidation
2. Field Implantation
3. 1st Mask
4. Gate Oxidation I
5. Poly Deposition
6. Poly Doping (or Implantation)
7. Poly Oxidation
8. 2nd Mask
9. Ion Implantation
10. Gate Oxidation II
11. Poly Deposition
12. Poly Doping (or Implantation)
13. Poly Oxidation
14. 3rd Mask
15. N+ Predeposition (or Implantation)
16. N+ Diffusion
17. Field Vapox Deposition
18. Vapox Densification
19. 4th Mask
20. Vapox Reflow
21. Al-Si Deposition
22. 5th Mask
23. Alloy I
24. Wafer Evaluation (Electrical)
25. Glass Deposition
26. 6th Mask
27. Backlap
28. Backside Implantation
29. Alloy II
30. Backside Gold Deposition

Note: This process flow is illustrative only.

Source: DATAQUEST, Inc.

Figure 3.4-2
16K DRAM CELL
(Not to Scale)



Source: DATAQUEST, Inc.

3.4 Manufacturing Cost Analysis

Table 3.4-9 shows a bipolar process flow chart for an 8-layer device, again included only for illustrative completeness. The terminology differs a little from MOS processing, but the process is similar: the technology is still planar technology and the major process operations are still oxidation, diffusion, and masking.

Table 3.4-9

TYPICAL BIPOLAR PROCESS

1. Initial Oxidation
2. Collector Mask (First Mask)
3. Collector (Deposition) Pre-Oxidation
4. Collector Diffusion
5. Epitaxy
6. Epi Reoxidation
7. Second Mask (Double Spin, Double Expose)
8. Composite Reoxidation
9. Third Mask
10. Isolation Deposition
11. Base Dip
12. Base Deposition
13. Base Diffusion
14. Sinker Mask (Fourth Mask)
15. Sinker Deposition
16. Emitter Mask (Fifth Mask)
17. Emitter Deposition
18. Emitter Anneal
19. Contact Mask (Double Spin, Double Expose) (Sixth Mask)
20. Platinum (Pt.) Sputter
21. Platinum (Pt.) Sinter
22. Platinum Strip
23. Titanium/Tungsten Sputter
24. Aluminum Evaporation
25. Aluminum Mask (Seventh Mask)
26. Aluminum Alloy
27. Contact Probe
28. Silox Passivation
29. Silox Mask (Eight Mask)

Note: This process flow is illustrative only.

Source: DATAQUEST, Inc.

Appendix

Table A-1

EQUIPMENT LIST FOR WAFER BACKSIDE PROCESSING

Item	Cost Each (Thousands of Dollars)	Required	Total Cost (Thousands of Dollars)	Delivery Weeks	Manufacturers
Abrasive (Backlap) System	$ 85.00	1	$ 85.00	20-30	Spitfire, Lapmaster
Magnetron Sputtering	$200.00	1	200.00	24-36	MRC, Airco
Cryopump	$ 13.00	1	13.00	12	CTI
Gas Analyser	$ 18.00	1	18.00	16	
Chemical Sink	6 ft. @ $1.60/lin.ft.	1	9.60	12-20	Microaire, Protoplastics, Harrington
Spray Rinser/Dryer	$ 2.50	1	2.50	6-10	Fluorocarbon, Fluoroware
High Pressure DI Water Scrubber	$ 22.00	1	22.00	18-20	Kasper, Cobilt, GCA
Plasma Asher (Barrel Type)	$ 27.00	1	27.00	12-26	Tegal, Dionex (IPC)
Laminar Flow Hood	18 ft. @ $0.40/lin.ft.		7.20	6-8	Microaire, Envirco
Miscellaneous Equipment: (Includes target storage, wafer storage, tables, chairs)			5.00		
Total			$389.30		
6½% Tax			25.30		
Grand Total			$414.60		

Source: DATAQUEST, Inc.

Appendix

Table A-2

EQUIPMENT LIST FOR FAB SUPPORT AND TEST AREAS

Item	Cost Each (Thousands of Dollars)	Required	Total Cost (Thousands of Dollars)	Delivery Weeks	Manufacturers
Production Control					
Host Computer (MIS)	$ 50.00	1	$ 50.00		IBM, DEC, Data General
CRT Terminal	$ 1.00	1	1.00		Lear Siegler
Laminar Flow Hood	2x8 ft. @ $0.40/ lin.ft.	2	6.40		Envirco, Microaire
Wafer Storage Cabinets	$ 0.20	2	.40		
Table, Desk, Chairs	$ 1.00		1.00		
Steel Mesh Shelving	$ 1.50		1.50		
Changing Room					
Lockers	$ 0.30	50	1.50		
Benches	$ 0.20	3	0.60		
Shoe Cleaner	$ 0.85	1	0.85		
Wafer Sort					
Automatic Prober	$ 27.00	4	108.00		Pacific Western, Electroglas
Tester (Wafer Sort)	2 heads		230.00	12-24	Xincom, Tektronix, Teradyne, Macrodata
Final Test					
Automatic Handler	$ 27.00	4	108.00		Siemens
Tester	$700.00	1	700.00	24-30	Fairchild, Tektronix, Teradyne, Macrodata
Total			$1,209.25		
6½% Tax			78.60		
Grand Total			$1,287.90		

Source: DATAQUEST, Inc.

Appendix

Table A-3

EQUIPMENT LIST FOR DEPOSITION AREA

Item	Cost Each (Thousands of Dollars)	Required	Total Cost (Thousands of Dollars)	Delivery Weeks	Manufacturers
Ion Implantation (2 ma, 20 to 100 KeV)					
Implanter	$470.00	1	$ 470.00	26-30	Lintot, AI, Extrion
Cryopump	$ 2.50	1	2.50	12	CTI
Laminar Flow Hood	2x6 ft @ $0.04/ lin. ft.	2	4.80	6-8	Envirco, Microaire
Leak Detector	$ 7.80	1	7.80	8-12	Veeco
Metallization					
Magnetron Sputtering Systems	$200.00	2	400.00	24-36	MRC, Airco Ultek
Cryopumps	$ 13.00	2	26.00	12	CTI
Residual Gas Analyser	$ 18.00	2	36.00	16	Inficon, UTI
Laminar Flow Hoods	30 ft. @ $0.40/ lin . ft.		12.00	6-8	Envirco, Microaire
Chemical Sinks	6 ft. @ $1.60/ lin. ft.	1	9.60	12-20	Microaire, Protoplastics, Harrington
Spray Rinser/Dryer	$ 2.50	1	2.50		
Miscellaneous Equipment (Includes target storage, chairs, tables, Dewar flask. Area can be designed to share Diffusion area process monitoring equipment.)			5.00		
Total			$ 976.20		
6½% Tax			63.45		
Grand Total			$1,039.70		

Source: DATAQUEST, Inc.

Appendix

Table A-4

EQUIPMENT LIST FOR MASKING AREA

Item	Cost Each	Required	Total Cost (Thousands of Dollars)	Delivery Weeks	Manufacturers (Thousands of Dollars)
Automatic Masking Line A. (4-Track System) Scrub/Bake Spin/Bake Develop/Bake (Includes controllers, indexers, track sections, buffers, pumps and cabinets)	$400.00	1	$ 400.00	16-24	GCA, Kasper, Cobilt
B. Alignment 1:1 Projection Aligner with automatic load/unload to 6-track system (max. 4" wafer capability) with accessories	$171.00	6	1,026.00	64	Perkin-Elmer, Cobilt
Chemical Sinks for Etching	50 ft. $1.60/ lin. ft.	1	80.00	14-24	Microaire, Protoplastics Harrington Plastics
Ultra-Clean Enclosures for Aligners	$ 10.00	6	60.00	16	Envirco, Integrated Air Systems
Laminar Flow Hoods for Masking Line	44 ft.@ $0.40/ lin. ft.	1	17.60	6-10	Envirco, Microaire
Mask Cleaner	$ 8.00	2	16.00	16	Ultratech
Critical Dimensions Measurement Systems	$ 23.70	1	23.70	26	Nanometrics, ITP
Convection Oven	$ 2.90	1	2.90	10	Blue-M

Table A-4 (Continued)

EQUIPMENT LIST FOR MASKING AREA

Item	Cost Each (Thousands of Dollars)	Required	Total Cost (Thousands of Dollars)	Delivery Weeks	Manufacturers
Particle Counter	$ 1.00	1	$ 1.00	12	Royco
Microscopes	$ 2.60	8	20.80	12	Leitz, Olympus
Camera	$ 0.80	1	0.80	6	Polaroid
Temperature/Humidity Monitor, Controller	$ 1.00	1	1.00		
Tables	$ 0.425	8	3.40	6-8	Microaire, Protoplastics
Chairs	$ 0.125	20	2.50		
Laminar Flow Hoods (for Etch Stations)	128 ft. @ $0.40/ lin.ft.	1	51.20	6-8	Envirco, Microaire
Plasma Ashers (Barrel Type)	$ 27.00	3	81.00	12-26	Tegal, Dionex (IPC)
Plasma Etchers (Planar Type)	$ 80.00	4	320.00	10-26	Dionex (IPC) D&W, ETS, Tegal
Spray Rinser/Dryer	$ 2.50	4	10.00	6-10	Fluorocarbon, Fluoroware
Miscellaneous Equipment (Includes: Solvent Cabinet Desiccators, Acid Storage Specialty Sink)			26.00		
Total			$2,143.90		
6½% Tax			139.40		
Grand Total			$2,283.30		

Source: DATAQUEST, Inc.

Appendix

Table A-5

EQUIPMENT LIST FOR DIFFUSION AREA

Item	Cost Each (Thousands of Dollars)	Required	Total Cost (Thousands of Dollars)	Delivery Weeks	Manufacturers
Furnaces (4 tubes per stack fully automated)	$30.00	12	$360.00	24-30	Thermco, Bruce
Hot Wall LPCVD Systems (fully automated)	$46.00	4	184.00	16-20	AMT, ASM
Chemical Sinks (8 ft. modules)	$ 1.60 (per lin.ft.)	4	51.20	12-20	Microaire, Protoplastics, Harrington Plastics
Spray Rinser/Dryer	$ 2.50	4	10.00	6-10	Fluorocarbon, Fluoroware
High Pressure DI Water Scrubbers	$22.00	1	22.00	18-20	Kasper, Cobilt, GCA
Work Stations (10 ft.)	$ 0.25	4	1.00	6-8	Microaire, Protoplastics
Laminar Flow Hoods for Work Stations (10 ft.)	$ 0.40 (per lin.ft.)	4	16.00	6-8	Envirco, Microaire
Subtotal			$644.20		

Appendix

Table A-5 (Continued)

EQUIPMENT LIST FOR DIFFUSION AREA

Item	Cost Each (Thousands of Dollars)	Required	Total Cost (Thousands of Dollars)	Delivery Weeks	Manufacturers
Process Monitoring Equipment					
Thickness Measuring System	$ 12.00	1	$ 12.00	10-14	Sloan, Siltec
Microscopes	$ 2.60	4	10.40	12	Leitz, Olympus
Pinhole Detector	$ 10.50	1	10.50	8-10	Sloan, Siltek
4-Point Probe	$ 3.50	2	7.00	8-10	Signatone
UV Lamps	$ 1.00	4	4.00		
C-V Plotter	$ 10.00	1	10.00		MDC
Parameter Tester	$135.00	1	135.00	16	Keithley
Metallurgical Microscope	$ 16.00	1	16.00	12	Zeiss, Reichert
SEM	$ 30.00	1	30.00	16-18	ISI (Japan)
Probe Station	$ 18.00	1	18.00	6-12	Micromanipulator, Signatone
Digital Ellipsometer	$ 23.70	1	23.70	26	Nanometrics
Angle Lap Measurement	$ 4.50	1	4.50	6-8	Philtek
Oscilloscope	$ 10.00	1	10.00	2-3	Tektronix
Resistivity Typing Equipment	$ 4.60	1	4.60	8-10	Signatone
Sodium Lamp	$ 2.00	1	2.00		
Microscope	$ 2.60	1	2.60	12	Leitz, Olympus
Camera	$ 0.80	1	0.80	6	Polaroid
Chemical Sink (6 ft.)	$ 1.60/ lin.ft.	1	9.60	12-20	Microaire, Protoplastics
Laminar Flow Hood (6 ft.)	$ 0.40/ lin.ft.	1	2.40	6-8	Microaire, Envirco
Table (6 ft.)	$ 0.425	1	0.43	8-12	Microaire, Protoplastics
Subtotal			$313.53		

Appendix

Table A-5 (Continued)

EQUIPMENT LIST FOR DIFFUSION AREA

(Thousands of Dollars)

Item	Cost Each (Thousands of Dollars)	Required	Total Cost (Thousands of Dollars)	Delivery Weeks	Manufacturers
Maintenance Equipment:					
Tube Washer	$ 11.30	1	$ 11.30	72	Integrated Air Systems
Tube Storage (7 tubes)	$ 1.04	1	1.04	12-14	Integrated Air Systems
Utility Sink (6 ft.)	$ 1.60/ lin. ft.	1	9.60	12-22	Microaire, Protoplastics
Drying Oven	$ 2.90	1	2.90	10	Blue-M
Washing Machine for Wafer Carriers		1	1.00		
Subtotal			$ 25.84		
Miscellaneous Equipment: Includes gas cabinets, gas systems, acid storage, quartzware storage, H_2 alarm systems, desiccators, safety showers, eye baths, thermocouples, tables, chairs			124.13		
Total for diffusion area.			$1,257.70		
6½% Tax			81.75		
Grand Total			$1,339.45		

Source: DATAQUEST, Inc.

3.5 Glossary

Angstrom - 10^{-8}cm.

Bipolar - Having two carriers of electrical current, one positively charged and one negatively charged. This state is in contrast to MOS transistors which only have one charge carrier (unipolar or one polarity).

Bit - Binary digit (see kilobit).

Boat - Quartz wafer holder, 3 inches wide and up to 24 inches long for use in furnace processes. Parallel slots are cut in the quartz so that wafers can sit vertically in the boat.

CAD - Acronym for Computer Aided Design. In its most common form, a computer memory is filled with a theoretical model of the MOS transistor and the pertinent process and device parameters. The circuit designer can then use the computer to simulate the performance of sections of the circuit he is designing, so that he can optimize the design without building a hardware prototype first. It can also refer to computer aided layout design.

Capacitor - A device (e.g., silicon - silcon dioxide - aluminum "sandwich") which can store charge.

Class 100 - An atmosphere controlled particle count per cubic foot of air containing not more than 100 particles of 0.5 microns in diameter or larger and not more than 1 particle of 4.0 microns or larger.

Cumulative Yield - The product or multiplication of yields at every manufacturing step. For example, two manufacturing steps with 80 percent (.8) yield would have a cumulative yield of 64 percent (.64).

Desiccators - Plexiglass storage boxes purged with a clean dry gas, such as nitrogen. Used to store work-in-process wafers to minimize contamination.

DI Water - Deionized water. High purity water in which all impurities having an electrical charge (ions) associated with them have been removed.

Die (plural, dice) - Individual integrated circuits (or transistors) separated from the original whole silicon wafer but not yet assembled in a package. Also known as chips or bars (in Texas). They vary in size from 20 mils on a side to larger than 250 mils on a side. The number of dice on a 3-inch wafer may vary from tens to thousands.

3.5 Glossary

Diode - A device (e.g., p-n junction) which allows large currents to pass when forward biased and very little current when reverse biased.

DIP - Acronym for Dual In-Line Package; usually referring to a package configuration in which the external pins are aligned in two parallel rows.

Dopant - Atoms such as phosphorus, boron, or arsenic which are diffused into silicon to create resistors, diodes, and transistors.

E-Sort - Electrical Sorting area where electrical performance of integrated circuits in wafer form is tested. (Same as Wafer Sort.)

Fab = Wafer Fabrication Area - The area in which the major manufacturing operations are performed.

Fabrication Yield - Cumulative wafer fabrication yield - defined as the number of wafers out of the process divided by the number into the process times 100.

FET - Acronym for Field Effect Transistor. The FET is a transistor whose electrical characteristics are varied by the modulation of an applied electric field across its controlling electrode.

HEPA (filter) - Acronym for High Efficiency Particulate Air filter.

I.C. (IC) - Short for Integrated Circuit.

Ion - Electrically charged particle. (Cations are positively charged; anions are negatively charged.)

JFET - Acronym for Junction Field Effect Transistor (see also FET).

Junction - The boundary formed by the diffusion of a dopant which produces an excess of negative (positive) charges into an area of silicon which itself has a dopant producing an excess of positive (negative) charges. At this boundary, the two dopant concentrations are equal.

Jungle - The gas control units used to regulate the flow and mixture of gases into furnace tubes.

Kilobit - One thousand bits (see bit).

Laminar Flow - Refers to the "clear air" systems (such as laminar flow hoods or benches) in which the filtered air has a streamlined flow, as opposed to turbulent flow.

3.5 Glossary

LPCVD - Acronym for Low Pressure Chemical Vapor Deposition.

LSI - Acronym for Large Scale Integration.

Masks, Hard Surface - Photomasks whose patterns are made of chrome or iron oxide, both of which are tougher or harder than the standard emulsion patterns. These masks are more scratch resistant and last longer, but are more costly.

Micron - One-millionth of a meter, or about forty-millionths of an inch (0.000040 inches).

Mil - One-thousandth of an inch (0.001 inches) or about 25.4 microns.

MOS (M.O.S.) - Acronym for metal-oxide-semiconductor. In present applications, the semiconductor is silicon. The MOS structure forms the controlling electrode of this type of transistor and consists of a sandwich of metal, oxide, and silicon.

MOS Transistor - A device having an MOS controlling electrode, with a total of three electrodes, typically: source (source of electrical carriers); drain (collects the carriers emitted by the source); and gate (controls or "gates" the amount of carriers flowing from the source to the drain). See also Bipolar, Unipolar, FET.

N-channel MOS - A device in which carriers of electrical current and the path (channel) in which they flow are negatively charged.

PC - Short for Production Control. This group in the manufacturing process schedules the flow of raw materials, work-in-process, and finished goods.

P-channel MOS - A device in which carriers of electrical current and the path (channel) in which they flow are positively charged.

PECVD - Acronym for Plasma Enhanced Chemical Vapor Deposition.

PERT - Acronym for Program Evaluation and Review Technique.

Photomasks - 2½" x 2½" to 4" x 4" glass plates, 60 mils thick, upon which are repeated patterns of a circuit layer or die. The patterns are of emulsion, chrome, or iron oxide.

Photoresist (resist) - An organic, viscous liquid which polymerizes (hardens) when exposed to ultraviolet light. A thin film is applied to the wafer surface and the images on a photomask are reproduced in the resist.

Probes - Electrically conductive wires, resembling a straight pin in shape, which are used to contact the electrode pad on circuit die during wafer sort.

PVD - Acronym for Physical Vapor Deposition.

3.5 Glossary

QA - Short for Quality Assurance. This group develops quality standards.

QC - Short for Quality Control. This group is responsible for monitoring the quality of the product at each of the manufacturing steps.

RAM - Acronym for Random Access Memory. A memory circuit which is organized such that any information location is accessible without disturbing the information contained in any of the other memory locations.

Resistor - A device which measurably opposes the passage of an electric current (e.g., "doped" silicon).

Run - A batch of wafers, numbering from 5 to 50, which are processed through each manufacturing step together.

Silicon Gate MOS - MOS transistors which have a controlling electrode (gate) consisting of silicon instead of metal over the oxide.

Unipolar (device) - e.g., MOSFET or JFET devices where the charge carriers have a single polarity.

Vapox - Short for Vapor Deposited Oxides, oxides that are deposited onto wafers by the decomposition of reactive gases (vapors) at low temperatures.

VLF - Acronym for Vertical Laminar Flow. Refers to hoods in which the filtered air flows downward to the work surface, in a laminar manner.

VLSI - Acronym for Very Large Scale Integration.

Wafer Sort - See E-Sort.

Wafers - Circular slices of silicon, 3 inches or 4 inches in diameter and 15 to 20 mils thick, used in the fabrication of integrated circuits.

Fast-Turn CMOS Model

OVERVIEW

This chapter deals with the design and manufacturing cost analysis of a facility dedicated to the prototype production of custom ICs. These ICs incorporate a two-micron complementary MOS (CMOS) process having a double layer of metal for interconnections. The treatment mainly applies to a small-size facility, the so-called pilot line, where initial investment in processing equipment is kept to a minimum, and where the emphasis is placed on fast turnaround time. In such a facility the skill and intelligence of the technical people is more important than their wafer fabrication productivity.

The transition to a higher volume, more productive operation is also briefly discussed.

The emphasis on fast turnaround time (10 to 15 working days) leads to low productivity of labor and extremely low productivity of capital equipment, even though equipment costs are minimized. As a result, wafer costs are about $360 per four-inch wafer; such a wafer would probably be priced in excess of $1,000, if such a facility were to supply wafer processing services on the open market. These prices are well in excess of the current market prices of $120 to $240 for a four-inch CMOS wafer. Some of the price increase can be attributed to the high number of masking levels (13) and to the expensive equipment required for the reproduction of two micron lines. The rest is due to production inefficiency.

We believe that these high manufacturing costs can be justified by the fast turnaround time achieved—two weeks instead of the 6 to 12 weeks normally obtained on a semiconductor manufacturing line. Many engineering managers feel that once a team of engineers and technicians is assigned to a project, money is expended at a more or less constant rate until the project is completed. This rate of spending is often called the "burn" rate; a term analogous to a rocket which, once fired, burns fuel at a constant rate. Since even a small integrated circuit design project with one engineer and a few technicians might "burn" money at the rate of $100,000 per year, it could be argued that a 10-week schedule savings is worth at least $20,000. This savings equals the total cost of two lots of 10 wafers each. In addition, having a product ready 10 weeks earlier might lead to other benefits such as increased market share.

It can also be argued that fast turnaround time can be achieved on a conventional manufacturing line by using the "hot-lot" technique. In this method, a portion of the wafers are processed without having to wait in in-process inventory. This argument is valid until an emergency—such as high yield loss—occurs. At such a time the economics of the situation demand all resources of the line to be applied to returning the line to full production. Any hot-lot runs are delayed for the duration of the emergency. Since emergencies occur frequently on most lines, the availability of this hot-lot service is at best somewhat unpredictable.

Fast-Turn CMOS Model

Most likely, any high volume custom circuits developed on this line will be produced in another higher volume facility, and for this reason the processes must be compatible. This is possible because in the last few years, major developments have taken place in the areas of semiconductor materials, chemicals and gases, and in wafer processing equipment used in the industry. This, together with the availability of accurate computer simulation tools for semiconductor processes and devices, makes it possible for a small-scale wafer fabrication area to approach the type of process control formerly obtainable only on large manufacturing lines.

Clearly, a system house has a strong motivation to set up an IC fabrication facility as a means of implementing proprietary designs into silicon rapidly, and with complete control. Alternatively, this need may be filled by small, efficient companies dedicated to the production of custom ICs.

WHY CMOS?

It is widely recognized that many future designs are going to be implemented in silicon with CMOS technologies; some of the reasons are:

- A CMOS gate dissipates power only during the transition from one state to the other, and has negligible power dissipation during standby conditions. This has the important consequence that, for a given package power dissipation and average gate delay, the maximum number of gates that can be integrated on a chip is orders of magnitude larger for CMOS circuits than for either bipolar or MOS circuits of any other technology.

- Propogation delay for a CMOS gate is only slightly larger than for an NMOS gate. For a 2-micron gate length, sub-nanosecond gate delays are possible.

- The CMOS inverter has a high degree of built-in noise immunity, since the output voltage swings completely from one supply voltage to the other.

- CMOS circuits are easy to design in comparison with other circuit forms.

We chose a double layer of metal for interconnections because of VLSI design considerations. The biggest challenge in complex VLSI designs is not so much the ability to place a very large number of gates on a chip, but the ability to interconnect them without errors and with a short design cycle. Industries and universities are very busy now developing tools for automatic layout of the interconnections. It is generally recognized that more than one level of high conductivity metal is going to be needed to make computer layout possible, while keeping the density of gates on the VLSI chip comparable to that of a completely manual layout with single layer metal.

Fast-Turn CMOS Model

PRODUCTIVITY CONSIDERATIONS

Organization

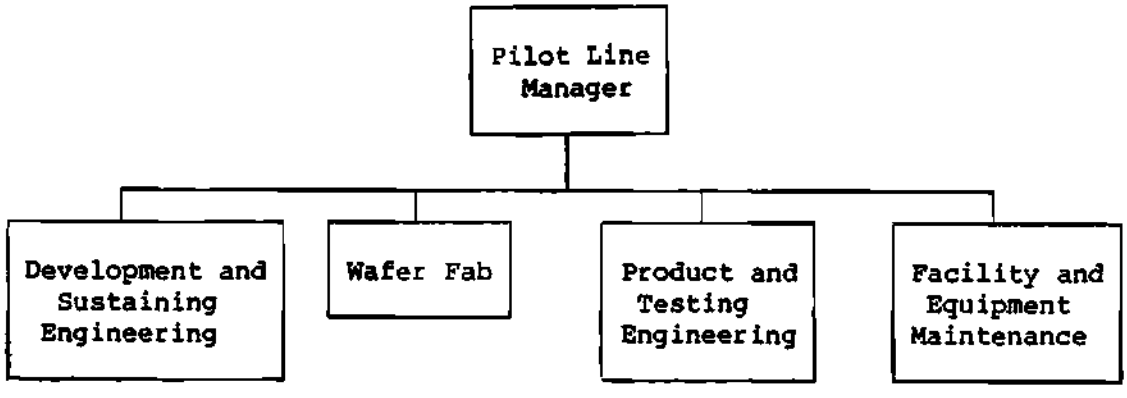
As stated in the beginning, the pilot line is intended to produce a small quantity of wafers using state-of-the-art technologies and with fast turnaround time, and not to be a laboratory dedicated to the development of process technologies. Once the individual pieces that are part of the process flow have been installed and characterized, and a complete process flow defined and specified in detail, the line has to run with the same general organization and discipline as a normal (high volume) production line.

The division of labor and level of experience required for the people of the organization are different. The division of labor in the wafer fab area is different because operators are cross-trained on several pieces of equipment. This allows them to hand-carry a batch of wafers through several sequential process steps, eliminating any inventory delay. In some firms these individuals might be given the title of model maker to distinguish them from more conventional fab operators. A higher level of experience is generally required for most workers in the organization; this arises from the fact that the relatively small number of individuals in the pilot line must have the aggregate experience of the staff of a much larger production line if they are to be technologically competitive.

A typical organization chart is shown in Figure 3.7-1.

Figure 3.7-1

ORGANIZATION CHART



Fast-Turn CMOS Model

The development and sustaining engineering group comprises the engineers who will develop and install the technologies, train the operators to run the various process steps, and who will be responsible for the quality of the material produced, and the correct use and maintenance of all equipment. Each engineer will have responsiblity for more than one process technology, and be very familiar with the equipment used and all the steps of the process. Because of the broad range of responsiblity of the job, he or she must be familiar with the physics of semiconductor devices and have experience in both semiconductor R&D and production environments.

The wafer fab group comprises all the equipment operators, and is directed by one supervisor who is responsible for the scheduling of the movements of the material, and for the line throughput. To enhance turnaround time, the operators (or modelmakers) have to be able to perform several related steps. For example, a diffusion operator will run all the diffusion, LPCVD deposition, and ion implantation operations, together with wafer cleaning and resist stripping operations. An etching operator will be able to use any etching machine, perform all the inspections to check resist pattern quality before committing the wafer to etching, and to check agreement of critical dimensions to the specifications. A masking operator will be able to prepare the wafers for exposure, run the photolithographic equipment and do all the post-processing operations and inspections. He or she must also know how to clean and inspect masks and reticles. Having all operators capable of doing all the processing steps is ideal for reducing turnaround time because it reduces or eliminates problems; this is practically impossible because of the long time required for training, and dangerous because of the lack of doublechecking. However, one or two operators of this kind (senior modelmakers) are invaluable for processing batches of wafers that have priority over the other batches.

The size of the product engineering and testing group depends on how much the customer is going to do in terms of testing of the circuits. Even if all testing at the wafer level and debugging of the circuits is done by the customer, the pilot line needs product engineers who use specifically designed test patterns to constantly monitor the stability of device parameters and the defect level of the wafers. These product engineers can be much more effective if they are also responsible for at least limited device testing, and if they have good communications skills and a good understanding of both processing and circuit design.

Fast turnaround requires that most equipment is performing properly most of the time. Responsive and professional maintenance of the facility infrastructures and processing equipment is key to this goal. Preventive maintenance should be done at specified times, even if the process engineers think that it is not necessary. Whenever possible, maintenance contracts that cover preventive and emergency equipment care should be negotiated at the time of purchase. The availability of such contracts usually directly determines the reliability level of the equipment.

Fast-Turn CMOS Model

Staffing

For a 500-wafer-out operation of this kind, our estimate of requirements in terms of people is shown in Table 3.7-1.

Number of Shifts

For most operations, the presence of all the process engineers is essential. Consequently, the number of shifts cannot exceed two; for example, a large shift from 7:00 a.m. to 3.30 p.m., and a reduced-staff shift from 2:00 p.m. to 10:30 p.m. This small second shift can complete time-consuming operations that take longer than eight hours; these include high dose implants and long diffusions.

The only exception is in the masking area. There, a full staff of experienced operators and sustaining engineers should operate on two shifts because of the limited throughput of the wafer stepper equipment.

Equipment Selection Criteria

For an easy transfer of the technology to a production line, the equipment of the pilot line should be compatible with production-type equipment. The decision whether to use an R&D or production version of the equipment requires a good knowledge of, and familiarity with, the process in question, and a detailed study of all the factors that might affect the duplication of the operation. Such a decision should be made by the development engineer under the guidance of the line manager. Some money can be saved by not requiring many of the equipment options offered for operation by inexperienced and untrained operators, but any automation that saves labor and enhances duplication and safety should be included.

Maximum Output

With only one wafer stepper used on two full shifts, our pilot line production is limited to 500 wafers out per period (one period equals four weeks). For such output, all other equipment is going to be used a maximum of 60 percent of the time it is available. This allows plenty of time for maintenance, and will enhance turnaround time.

To reduce even further the load on heavily utilized equipment (wafer stepper, ion implanter, oxide etcher and one furnace), the equipment might be duplicated. Additional space is provided for that purpose in the layout and design of the facility.

Fast-Turn CMOS Model

Table 3.7-1

STAFFING REQUIREMENTS

Classification	Job Function	Personnel Required	Estimated Wage Rate Per Period* (Thousands of Dollars)
Direct	Wafer Fab Operators (Model Makers)	10	$1.40
Indirect	Line Manager	1	$4.50
	Wafer Fab Supervisor	1	$2.50
Allocated	Development and Sustaining Engineers	5-6	$4.00
	Product and Testing Engineers	2	$3.00
	Facility and Equipment Maintenance Engineers	3-4	$2.80

*Period equals four weeks

Source: DATAQUEST, Inc.
January 1982

Fast-Turn CMOS Model

For photolithography, our pilot line will use one 10:1 wafer stepper for all the masking levels requiring high resolution and/or the smallest registration error to the previous pattern, and a 1:1 scanning projection system for all remaining layers. For a CMOS circuit with double layer metal, the critical masking levels are the same as for an NMOS circuit:

- Field mask
- Gate mask
- Contact mask
- First metal mask
- Via mask
- Second metal mask

All remaining mask levels are oversize masks, and alignment tolerances can be relaxed. One exception is the P-well mask. For some types of circuits where the spacing between P and N channel devices could significantly affect the die size, it may be advantageous to use the wafer stepper for defining the P-wells, but we have not done so in our model.

Because of the high degree of control required for positional accuracy of the patterns and size accuracy of their dimensions, 1:1 masks and 10:1 reticles must be generated with electron-beam maskmaking equipment.

FAB LAYOUT AND FACILITY REQUIREMENTS

Introduction

In this section we describe the main process flow used for producing two-layer metal CMOS circuits, list the needed equipment, show an example of equipment layout in the clean room area, and describe the facility requirements in terms of electric power, gases, DI water, etc.

The layout of the fab area for a pilot line is a very challenging task. It is a compromise between various and often contradicting needs. The requirements are to:

- Ensure a smooth flow of the wafers through the steps of the main process that is going to be used in the facility
- Allocate space and equipment for new technology developments in such a way that this activity is not going to interfere with standard production

Fast-Turn CMOS Model

- Simplify the layout of process piping, air and exhaust ducting, and power distribution for ease of maintenance and cost reduction during construction
- Facilitate equipment maintenance, so that it will not disturb work on all equipment
- Ensure the highest achievable level of cleanliness, particularly in the masking and deposition areas

Process Flow

While the N-channel silicon gate process flow is quite well established, the same is not true for the CMOS process.

The minimum number of masking steps necessary for producing two-layer metal CMOS circuits is ten. Three extra implant protection masks are usually added for better control of device characteristics, and for reducing the spacing between P- and N-channel devices, and they will be added in our process flow.

The number of critical masking steps, in terms of image resolution and layer to layer registration, is the same as required for producing NMOS circuits with two layers of metal. They are as listed in the previous section and are the ones for which the wafer stepper equipment will be used.

A typical process flow is given in Table 3.7-2.

Equipment List and Utilization

The list of equipment necessary for performing all the process steps is given in the appendix at the end of this section, with indicative prices, delivery times and manufacturers. We have also added a list of equipment for a testing area that is not part of the clean room area.

For a more accurate prediction of equipment utilization, one has to know the wafer mechanical yield at every step. Since the throughput limits occur in the masking area, we have assumed that the sorting of good and bad wafers occurs at incoming inspection in the masking area, and not at each processing step. The assumed wafer mechanical yield is shown in Table 3.7-3; equipment utilization, in terms of hours of use for a final production of 500 wafers per period, and in percentage of the total time the equipment is available to the operators, is given in Table 3.7-4 along with the time spent by the operator using the equipment. These numbers are used for predicting the number of operators needed in the processing area and their assignment in the three areas of specialization—diffusion (including ion implantation and thin film deposition), etching and masking.

Table 3.7-2

TWO-LAYER METAL CMOS PROCESS FLOW OUTLINE

Process Step	Comments
Initial Oxidation	
P-well Mask	Defines areas where N-channel transistors are built
Boron (P) Implant	
P-well Drive In	
Oxidation and Nitride Deposition	
Field Mask	Defines all active device areas
N-field Implant	Raises the field inversion voltage of the N-areas
P-field Mask	
P-field Implant	Raises the field inversion voltage of the P-areas
Field Oxidation	
Gate Oxidation	
P-channel Mask	
Phosphorous (N) Implant	Controls punch-through voltage of the P-channel
Boron (P) Implant	Controls P-channel threshold voltage
N-channel Mask	
Boron (P) Implant	Controls punch-through and threshold voltage of N-channel
Polysilicon Deposition	
Polysilicon Doping	
Gate Mask	Defines gate electrodes
Reoxidation	

Table 3.7-2 (Continued)

TWO-LAYER METAL CMOS PROCESS FLOW OUTLINE

Process Step	Comments
N^+ mask	
Phosphorous or Arsenic Implant	Establishes source/drain regions of N-channel
P^+ mask	
Boron Implant	Establishes source/drain regions of P-channel
Anneal	
Phosphorous Glass Deposition	
Anneal	
Contact Mask	
First metal deposition	
First metal mask	
Dielectric deposition	
Via mask	Establishes the areas of contact between the two layers of metal
Second metal deposition	
Second metal mask	
Alloy	
Dielectric deposition	For scratch protection
Pad mask	

Source: DATAQUEST, Inc.
January 1982

Fast-Turn CMOS Model

Table 3.7-3

WAFER MECHANICAL YIELD

Step	Yield (Percent)	Cumulative Yield (Percent)	Number Of Wafers Produced
P-well Mask	95	95.0	776
Field Mask	96	91.2	737
P-field Mask	97	88.5	708
P-channel Mask	98	86.6	686
N-channel Mask	97	83.2	673
Gate Mask	96	79.9	646
N^+ Mask	99	79.1	638
P^+ Mask	97	76.1	614
Contact Mask	96	73.7	595
First Metal Mask	93	68.5	554
Via Mask	96	65.8	532
Second Metal Mask	95	62.5	505
Pad Mask	99	61.8	500

Source: DATAQUEST, Inc.
January 1982

Table 3.7-4

EQUIPMENT UTILIZATION AND OPERATOR TIME PER EQUIPMENT AREA
(500 Wafers Out Per Four-Week Period)

Equipment	Use (Hours)	Number Of Shifts	Utilization (Percent)	Operator Time Per Period (Hours)
Diffusion area				
Sink				
#1	36.87	2	13.2	12.93
#2	73.18	1	52.3	28.33
#3	26.30	1	18.8	9.02
#4	14.12	1	10.9	14.12
#5	78.48	2	28.3	31.62
Furnace				
#1	144.13	2	51.5	17.65
#2	98.29	2	35.1	3.88
#3	44.84	1	32.0	5.90
#4	21.25	1	15.2	14.87
#5	25.20	1	18.0	8.82
#6	12.28	1	8.8	3.07
#7	12.62	1	9.0	3.53
LPCVD				
Poly	8.97	1	6.4	3.73
Nitr.	10.35	1	7.4	4.32
Oxide	33.47	1	23.9	8.37
Metal Deposit	31.32	1	22.4	18.78
Implanter	148.62	2	53.1	25.65
Total diffusion operator time				214.59
Etching Area				
Nitride Etcher	22.11	1	15.8	14.73
Poly Etcher	41.18	1	29.4	38.95
Oxide Etcher	86.67	1	61.9	86.67
Metal Etcher	59.09	1	42.2	59.09
Asher	55.42	1	39.6	19.95
Total etching operator time				219.39
Masking Area				
Wafer Stepper	237.90	2	85.0	237.90
Projec. Align.	113.60	2	40.6	113.60
Resist Proces. Equipment	-	2	25.0	371.80
Total masking operator time				723.30

Source: DATAQUEST, Inc.
January 1982

Fast-Turn CMOS Model

Clean Room Layout

A typical layout for the equipment in the wafer fab area is shown in Figure 3.7-2. We can identify three distinct areas:

- Photolithography area, with the process line for the wafer stepper and the area for the projection aligner; as shown, the process lines can easily accomodate two steppers and two 1:1 projection aligners; the photolithography area is isolated from the rest of the clean room and will use a dedicated air conditioning system
- Etching and metal deposition area, which requires a high degree of cleanliness, but a less stringent climate control than the masking area
- Diffusion, thin film deposition, and ion implantation area

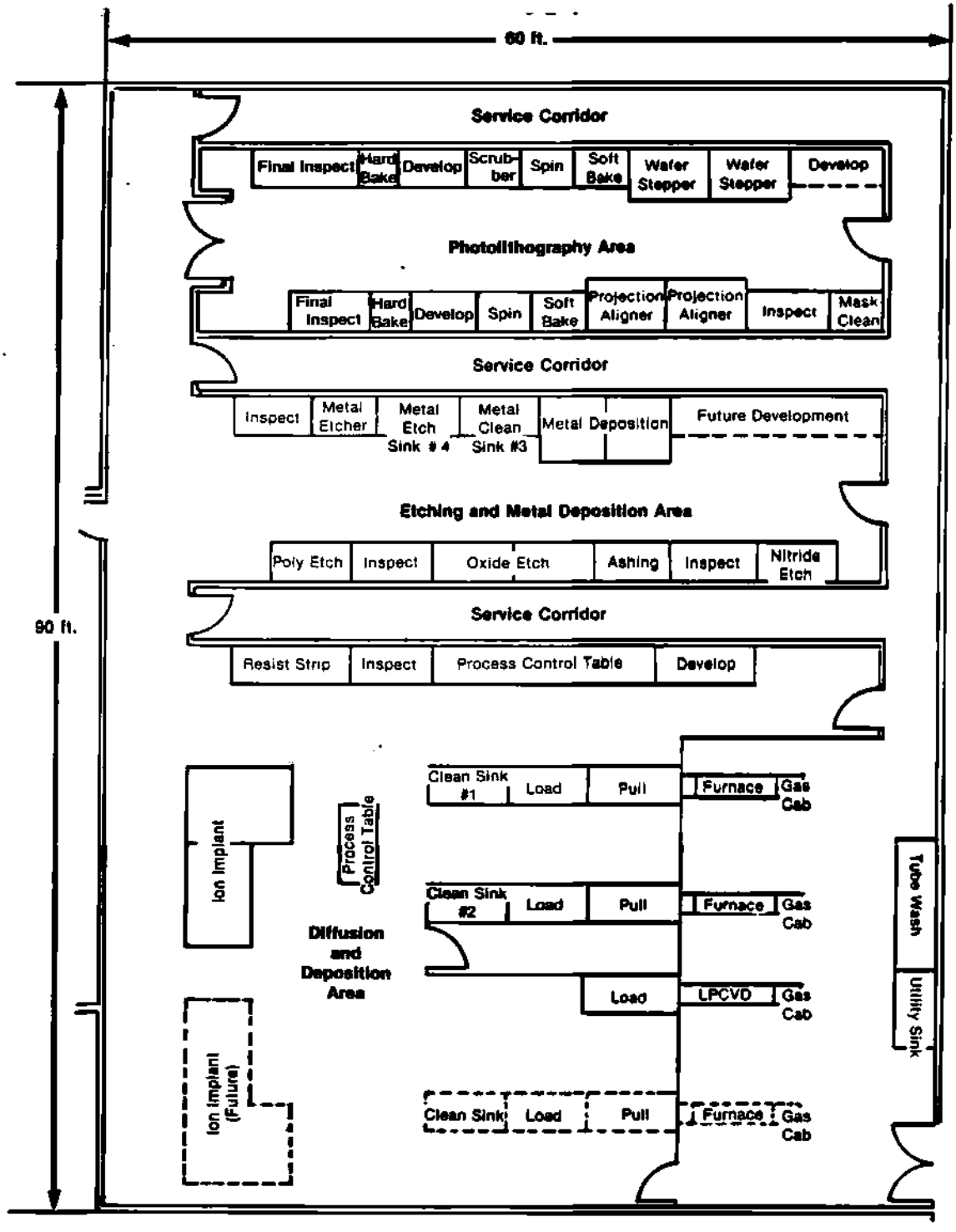
Service aisles are provided behind lithography and etching process lines for locating all the "dirty" equipment (such as pumps, power generators, canisters containing liquids, specialty gas cylinders, etc.), and the gas and liquid pipes, and the electrical wiring. This approach allows most of the maintenance work to be done outside the clean areas; the resulting reduction of traffic makes it easier to keep the clean areas particle free.

The overall wafer fab area is 5,400 square feet. The service aisle area is about 1,300 square feet, leaving a net effective clean area of 4,100 square feet.

Facility Requirements

The major systems and requirements for the wafer fab area are listed in Table 3.7-5. A range of costs for material and installation is given, reflecting differences in the requirements and materials used. Non-recoverable costs indicate the portion of the cost that is due to physical additions to the building, such as process piping or clean room construction. These items generally have a longer depreciation cycle.

Figure 3.7-2
LAYOUT FOR C-MOS WAFER FAB AREA



Source: DATAQUEST, Inc.

Table 3.7-5

FACILITIES IMPROVEMENTS FOR WAFER FABRICATION AREA

System	Requirements	Cost Range (Thousands of Dollars)	Average (Thousands of Dollars)	Nonrecoverable Costs
Fab Construction		$505 - $ 605	$ 555	$360
DI Water system (With 80 percent Reclaimation)	25-50 Gallons per Minute	125 - 200	163	60
Air Conditioning (With Cooling System and Tower)	100-125 Tons	180 - 200	190	60
Chemical and BOH6 Storage		20 - 25	22	22
Electrical		150 - 200	175	125
Totals		$980 - $1,230	$1,105	$627

Source: DATAQUEST, Inc.
January 1982

Fast-Turn CMOS Model

WAFER COST ANALYSIS

Assumptions

The assumptions described in the previous sections are:

- Technology
  - Two-layer metal CMOS
  - Six masking operations with wafer steppers (10:1)
  - Seven masking operations with 1:1 projection aligners
  - Dry etching
  - 100mm-diameter silicon wafers
- Production
  - One fully staffed shift in diffusion and etching areas
  - Small second shift in diffusion area
  - Two fully staffed shifts in the masking area
  - Personnel requirements, wage rates, and labor costs for direct, indirect and allocated personnel as shown in Table 3.7-6
  - 500 finished wafers out per week
- Yield; cumulative fab yield is 61.8 percent

Fast-Turn CMOS Model

Table 3.7-6

LABOR COSTS
(Thousands of Dollars)

Personnel	Number	Wage Rate	Personnel Cost per Period	25 percent Fringe Benefit	Total Personnel Cost
Direct:					
Wafer Fab Operators	10	1.4	$ 14.0	$3.50	$17.50
Indirect:					
Line Manager	1	4.5	$ 4.5		
Wafer Fab Supervisor	1	2.5	2.5		
			$ 7.0	$1.75	8.75
Allocated:					
Development and Sustaining Engineers	5-6	4.0	$22.0		
Production Testing Engineers	2	3.0	6.0		
Facility and Equipment Maintenance Engineers	3-4	2.8	$ 9.8		
			$37.8	$9.45	$47.25
					$73.50

Source: DATAQUEST, Inc.
January 1982

Fast-Turn CMOS Model

Fixed Costs

Tooling

The costs of reticles and masks used for wafer production are not included in the wafer cost analysis. These costs are very high, ranging from $1,000 to $3,500 for 10:1 reticles and masks. These costs are normally included in circuit design costs.

Facilities

We assume that the building is rented as a shell at $1.00 per square foot per period. The total space rented is 12,000 square feet (5,000 square feet for wafer fab, the remainder for offices and service areas). Facility design is contracted to an outside engineering firm and all facilities and services are supplied from scratch.

From Table 3.7-5, the cost of construction and equipment of the systems supporting the fab area is $1,105,000, out of which $627,000 is nonrecoverable. In terms of depreciation, the latter portion of the cost is treated as fab construction cost. Construction cost for office, test area, and service areas is estimated at $40 per square foot, for a total cost of $280,000.

Equipment

From the Appendix, equipment costs are as follow (dollars in thousands):

Diffusion area equipment	$ 751.5
Deposition, implantation equipment	635.5
Etching equipment	628.9
Masking equipment	1,346.2
In-process test equipment	289.0
Total cost for fabrication equipment	$ 3,651.1

Fast-Turn CMOS Model

Wafer Cost Analysis

Fixed Costs Per Period (four weeks)

Rent:	12,000 square feet @ $1.00 per square foot	$ 12,000
Sewage and water maintenance		1,500
Electrical power		18,000
Gas		700
Depreciation		
Fab construction (360 months); $627,000		1,742
All other construction, including office, test area and fab support systems (96 months); $758,000		7,896
Fab equipment, excluding test equipment (60 months); $3,651,100		60,851
Total per calendar month		$ 102,689
Total per period		94,790
Cost per wafer for 500 wafers out		$ 189.58

Variable Costs Per Period

Materials		
Silicon	$ 17.50	
Chemicals	7.80	
Miscellaneous materials	2.90	
Gases	5.20	
DI water	2.50	
Cost per wafer for 500 wafers out		$ 35.90
Labor		
Direct	$ 17,500	35.00
Indirect	8,750	17.50
Allocated	42,250	84.50
Cost per wafer for 500 wafers out		$ 137.00

Fast-Turn CMOS Model

The cost per wafer, based on all fixed costs and variable costs of materials and labor, is shown as a percentage of the total cost:

Fixed costs per period	$	189.58	52.3%
Fab materials		35.90	9.9%
Fab labor		137.00	37.8%
Total cost per wafer for 500 wafers out	$	362.48	100.0%

INCREASING PRODUCTIVITY

Introduction

The productivity of our pilot line in terms of wafers per operator and per square foot of fab area is quite small if one compares these results with those achieved, for instance, in N-channel dynamic RAM production lines. There are several reasons for this:

- We want fast turnaround time and for this reason, keep the equipment utilization low and the batch size small.
- Our CMOS process is more complicated than a conventional N-channel process.
- We have limited the investment in very expensive equipment (e.g., aligners) and created throughput bottlenecks.

A look at Table 3.7-4 shows that much expensive equipment (occupying a very costly floor space) is very much underutilized. Productivity can be raised by duplicating the equipment that has a high degree of utilization. This has the additional benefit of avoiding a complete paralysis of the line in case a heavily utilized piece of equipment is not operational.

In this section we modify our plan to increase wafer throughput from 500 wafers out per period to 1,000 wafers out per period. Substantial cost savings result. While output could be increased still further and give still more cost savings, we do not believe the 10- to 15- working-day turnaround time can be maintained under such conditions.

Fast-Turn CMOS Model

Duplication of Equipment

The line throughput can be doubled by adding:

One wafer stepper, used on two shifts
One furnace (#1), used on two shifts
One ion implanter, used on two shifts
One oxide etcher, used on one shift

The degree of utilization of the wafer steppers still remains at 85 percent, which is very high, but this is assuming a wafer throughput of only 15 wafers per hour. Expected improvements in existing equipment (automatic alignment and automatic reticle exchange), and the introduction of completely new models is going to increase the equipment throughput by at least a factor of two, thus reducing the equipment utilization to levels more acceptable for a fast turnaround time.

Wafer Cost Analysis for Increased Line Throughput

For increased throughput, these cost figures are going to change:

- Fab equipment depreciation
- Labor

All other costs are not going to change significantly. The fab equipment depreciation per month will increase from $60,851 to $76,938. This will add depreciation of $14,850 per period. The direct labor cost per wafer will decrease from $35.00 (10 fab operators), to $26.25 (15 fab operators), and the allocated labor from $84.50 per wafer to $60.75 per wafer (with the addition of two sustaining engineers and one maintenance engineer).

Table 3.7-7 shows the total wafer cost for 1,000 wafers out per period in comparison to the cost for 500 wafers out.

Fast-Turn CMOS Model

Table 3.7-7

COST PER WAFER

	500 Wafers Out Per Period		1,000 Wafers Out Per Period	
	Cost	Percent	Cost	Percent
Fixed Cost Per Period	$189.58	52.3%	$109.69	45.4%
Fab Materials	35.90	9.9	35.90	14.9
Fab Labor				
Direct	35.00		26.25	
Indirect	17.50		8.75	
Allocated	84.50		60.75	
Total Labor	$137.00	37.8	$ 95.75	39.7
Total Cost Per Wafer	$362.48	100.0%	$241.34	100.0%

Source: DATAQUEST, Inc.
January 1982

Fast-Turn CMOS Model

APPENDIX
EQUIPMENT LIST FOR CMOS WAFER FAB AREA

Item	Unit Cost (Thousands of Dollars)	Number Required	Total Cost (Thousands of Dollars)	Delivery (Weeks)	Manufacturers
Diffusion Area Equipment					
Furnaces (4 tubes per stack, fully automatic)	$35.0	8 (tubes)	$280.0	26	Thermco, Bruce
LPCVD System (fully automatic)	$50.0	3	150.0	26	AMT, ASM, ACS
Chemical Sink (6 feet with rinser/ dryer)	$22.0	2	41.5	12-20	Micro Air, Protoplastic, Harrington Plastic
Process Monitoring Equipment					
Step Height Meas. System	$12.0	1	$ 12.0	6-12	Sloan, Tencor, Siltec
4-Point Probe	$ 3.5	3	10.5	4-8	Signatone, Veeco
UV Lamp	$ 1.0	3	3.0	4	
CV Plotter	$11.0	1	11.0	6	MDC
Probe Station	$18.0	1	18.0	6-12	Micromanipulator, R&K, Signatone
Thin Film Meas. Equipment	$30.0	1	30.0	16-20	Nanometrics
Curve Tracer	$10.0	1	10.0	12-16	Tektronix
Angle Lamp Equipment	$ 4.5	1	4.5	6-8	Philtek
Microscope	$ 5.0	1	5.0	4-8	Lietz, Nikon, Olympus
Interferometer	$ 4.0	1	4.0	4-8	Lietz
Camera	$ 1.0	1	1.0	4-8	Polaroid
Maintenance Equipment					
Tube Washer	$ 12	1	$ 12.0	8-10	Integrated Air System
Utility Sink (8 feet)	$ 8	1	$ 8.0	12-20	Micro Air, Protoplastic

(Continued)

APPENDIX
EQUIPMENT LIST FOR CMOS WAFER FAB AREA (Continued)

Item	Unit Cost (Thousands of Dollars)	Number Required	Total Cost (Thousands of Dollars)	Delivery (Weeks)	Manufacturers
Miscellaneous Equipment (gas system, gas cabinets, acid storage, quartzware, TC and temp. meas. systems, tables, chairs)			$105.0		
Subtotal			$705.5		
6.5% Tax			46.0		
Total for Diffusion Area Equipment			$751.5		
Deposition and Implant Equipment					
Ion Implanter (medium current, 200kV)	$350.0	1	$350.0	20-40	Nova, Varian, GCA
Metal Deposit. System (sputter depos.)	$195.0	1	195.0	30-45	Perkin-Elmer, Ultek, MRC Airco, Temescal, CPA
Chemical sink (6 feet with rinser/ dryer)	$ 14.0	1	11.5	12-20	Micro Air, Protoplastic, Harrington Plastic
Wafer Scrubber	$ 20.0	1	20.0	8-12	MTI, Veeco, Macronetics
Leak Detector	$ 8.0	1	8.0	8-12	Veeco, Varian
Miscellaneous Equipment (Dewar flasks, gas systems, tables, chairs)			12.0		

(Continued)

APPENDIX
EQUIPMENT LIST FOR CMOS WAFER FAB AREA (Continued)

Item	Unit Cost (Thousands of Dollars)	Number Required	Total Cost (Thousands of Dollars)	Delivery (Weeks)	Manufacturers
Subtotal			$596.5		
6.5% Tax			39.0		
Total for Deposition and Implant Equipment			$635.50		
Etching Equipment					
Nitride Etcher (barrel type)	$ 34.0	1	$ 34.0	12-16	Branson IPC, Tegal, LFE
Polysilicon Etcher (planar type)	$120.0	1	120.0	18-26	PlasmaTherm, Tegal, Branson IPC
Oxide Etcher (planar type)	$200.0	1	200.0	18-26	Toshiba, Plasmatherm, AMT
Metal Etcher (planar type)	$130.0	1	130.0	20-26	D&W Eaton, Branson IPC AMT, Varian
Asher (barrel type)	$ 20.0	1	20.0	12-16	Branson IPC, Tegal
Resist Strip Sink (6 feet)	$ 22.0	1	22.0	12-20	MicroAir, Protoplastics Harrington Plastic
Chemical Sink (6 feet with rinser/ dryer)	$ 17.5	1	17.5	12-20	MicroAir, Protoplastic Harrington Plastic
Microscope	$ 4.0	3	12.0	4-8	Leitz, Olympus

(Continued)

APPENDIX
EQUIPMENT LIST FOR CMOS WAFER FAB AREA (Continued)

Item	Unit Cost (Thousands of Dollars)	Number Required	Total Cost (Thousands of Dollars)	Delivery (Weeks)	Manufacturers
Miscellaneous Equipment (gas systems, gas cabinets, wafer storage cabinets, tables, chairs)			35.0		
Subtotal			$590.5		
6.5% Tax			38.4		
Total for Etching Equipment			$628.9		
Masking Equipment					
Wafer Stepper	$750.0	1	$ 750.0	40	GCA, Optimetrix, Censor, Electromask
1:1 Projection Aligner (autoload, manual adjustment)	$280.0	1	280.0	13	Perkin-Elmer, Cobilt, Canon
Wafer Scrubber	$20.0	1	20.0	8-10	Veeco Macronetics, Cobilt, Kasper
Single Track Resist Spinner	$16.0	2	32.0	8-10	Veeco Macronetics, Cobilt, Kasper, GCA
Single Track Soft Bake Oven	$15.0	2	30.0	8-10	Veeco Macronetics, Cobilt, Kasper, GCA
Resist Develop Station	$11.5	2	23.0	16	Ultratech
Hard-Bake Oven	$ 5.0	2	10.0	10	Lab-line Instr., Blue-M, Thelco

(Continued)

APPENDIX
EQUIPMENT LIST FOR CMOS WAFER FAB AREA (Continued)

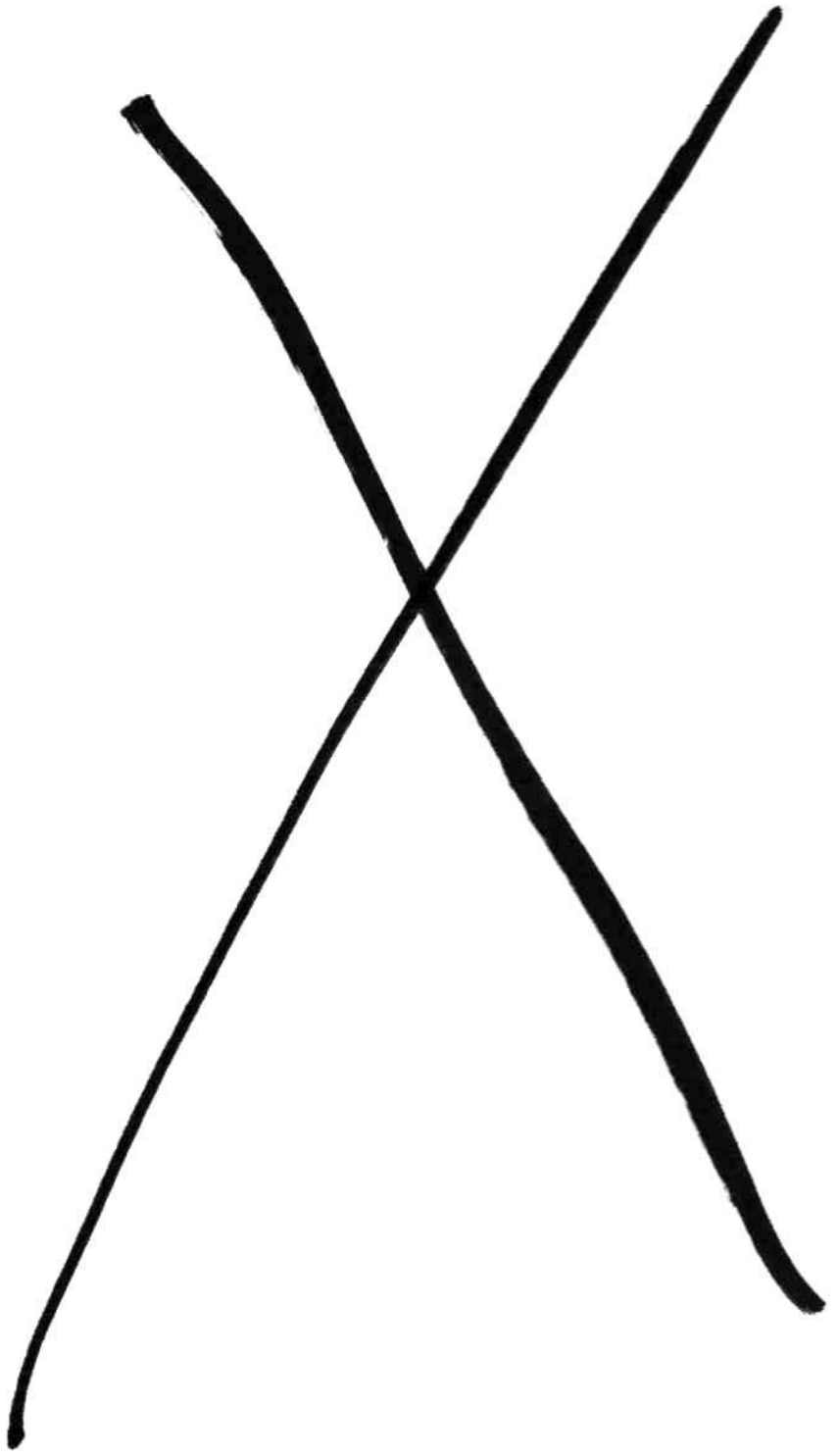
Item	Unit Cost (Thousands of Dollars)	Number Required	Total Cost (Thousands of Dollars)	Delivery (Weeks)	Manufacturers
Mask Cleaner	$ 8.0	1	8.0	16	Ultratech, MTI
Linewidth Meas. System	$40.0	1	40.0	26	Nanometrics, ITP
High Quality Microscope and Camera	$16.0	1	16.0	6-8	Letiz, Zeiss, Reichert
Inspection Microscope	$ 4.0	3	12.0	6-8	Leitz, Nikon, Olympus
Wafer Flatness Tester	$20.0	1	20.0	3	Tropel
Particle Counter	$ 7.0	1	7.0		Royco
Temp./Humidity Monitor	$ 1.0	1	1.0		
Miscellaneous Equipment (solvent, acid storage cabinets, mask, wafer storage cabinets, specialty sink)			15.0		
Subtotal			$1,264.0		
6.5% Tax			82.2		
Total for Masking Equipment			$1,346.2		
In-Process Test Equipment					
Automatic Prober	$ 27	1	$ 27.0		Pacific Western, Electroglass
Parametric Tester	$ 85	1	85.0		Keithley, Lomac, HP
Curve Tracer	$ 5	1	5.0		Tektronix
Oscilloscope	$ 5	1	5.0		Tektronix

(Continued)

APPENDIX
EQUIPMENT LIST FOR CMOS WAFER FAB AREA (Continued)

Item	Unit Cost (Thousands of Dollars)	Number Required	Total Cost (Thousands of Dollars)	Delivery (Weeks)	Manufacturers
Digital Voltmeter	$ 1	2	2.0		Fluke, HP
Frequency Counter	$ 2	1	2.0		HP
Signal Generator	$ 2	2	4.0		HP
SEM (4 inch stage)	$120	1	120.0		Cambridge, Hitachi
Manual Prober	$ 11	1	11.0		Rucker & Kolls
Miscellaneous Equipment (power supplies, ammeters, L-C meter, tables, chairs)			10.0		
Subtotal			$271.0		
6.5% Tax			18.0		
Total for In-process Test Equipment			$289.0		

Source: DATAQUEST, Inc.
January 1982



4 Technology

The many different theoretical types of devices, their circuit functions, the different types of semiconductor materials, and the variations in basic designs generate a large number of semiconductor devices and integrated circuits. This chapter of the DATAQUEST Semiconductor Industry Service provides a brief explanation of the physical phenomena that cause semiconductors to function and the technologies employed in the production of semiconductor devices and explores the past evolutionary growth of semiconductor technology.

The Technology Chapter is divided into two major parts. Sections 4.2 to 4.9 are reserved for in-depth studies on emerging technologies. Three sections have been assigned—Integrated Injection Logic (I^2L), Section 4.2; Charge Coupled Devices (CCDs), Section 4.3; and Silicon-on-Sapphire (SOS), Section 4.4. Sections 4.10- to 4.16 deal generally with semiconductor technology.

The basic assumptions made in writing this chapter are that the reader has little technical background and is only slightly familiar with the technologies basic to the semiconductor industry.

The nontechnical reader should gain some appreciation for both the complex technologies that are required for modern semiconductor devices and the interactions between them. Our objective is to cover technology briefly rather than in depth. The discussion will accomplish the following:

- The nontechnical reader will understand most of the definitions and abbreviations found in the jargon of the industry.
- Basic explanations will utilize heuristic discussions of the physical phenomena.
- Most of the processes utilized in device manufacture will be explained.
- The operation and uses of the various types of devices will also be outlined.

For those readers with a more technical background, the key areas of interest will be the technology trend analyses. The evolutionary growth of device and circuit technology in the past helps us to forecast the future path of technology. Thus, the industry trends that will result in improved devices, circuits, and manufacturing technology will become more apparent.

4.12 Bipolar Technology

INTRODUCTION

The term "bipolar" defines a class of semiconductor devices, integrated circuits, and processes in which the conduction of electrical current is via two oppositely charged carriers. As previously described, one of the carriers is negatively charged (negative polarity) and is called an electron; the other is the positively charged (positive polarity) and is called a hole. Both carriers contribute to the total flow of current.

In contrast to MOS devices, which are discussed later, the critical flow of current in a bipolar device takes place within the bulk silicon substrate rather than at the silicon surface. Consequently, bipolar devices have been relatively insensitive to the surface contamination that degrades MOS yields and reliability.

The low sensitivity of bipolar devices to surface effects enabled bipolar fabrication to become the dominant device technology in the late 1950s. This dominance continued into the 1960s, as bipolar ICs were developed in great profusion. New device and circuit design techniques, coupled with process improvements, produced products of ever-increasing complexity and improved performance.

This section describes bipolar processes, for both discrete devices and integrated circuits. Past and probable future trends are discussed to give the reader a perspective on the changes that continue to occur in bipolar technology.

FABRICATION TECHNOLOGIES– GENERAL

A number of bipolar process technologies are available, producing a multitude of product families. Ultimately, however, the basic fabrication technologies are derived from two processes: multidiffused and epitaxial.

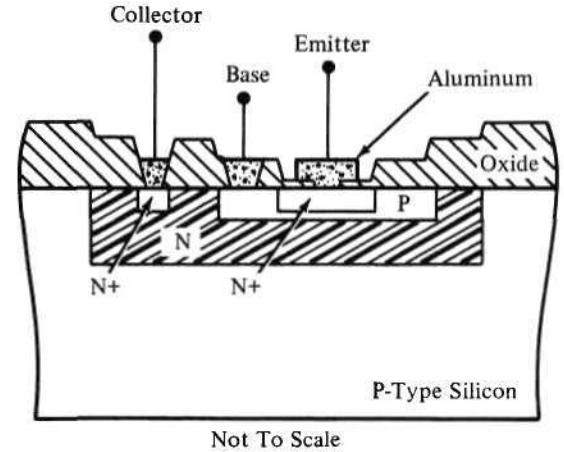
Multidiffused Process

A cross-section of a multidiffused bipolar device is shown in Figure 4.12-1. The particular device shown is called a triple-diffused transistor, because three separate diffusions are needed to form its three electrodes.

The triple-diffused transistor in Figure 4.12-1 is formed sequentially by a series of three vertical diffusions with intermediate photomask steps delineating the appropriate areas to be doped. Each successive diffusion is of higher dopant concentration and of opposite dopant type than the previous layer. It is placed within the previous diffused area or "well." The final N-type diffusion is performed into the P-type diffusion, which was made into the first N diffusion. The final high concentration N+ contains 100 to 1,000 times more dopant than the initial N-type diffusion. In many devices, gold is also diffused into the wafer during the last N+ diffusion to enhance the

Figure 4.12-1

CROSS SECTION OF A TRIPLE-DIFFUSED BIPOLAR TRANSISTOR



Not To Scale

Source: DATAQUEST, Inc.

4.12 Bipolar Technology

speed of the transistors.

The triple-diffused process formed the basis for many bipolar discrete transistors and IC families that are discussed later. Although the process is considered to be simple by today's standards, it represented a radical step forward in process technology when it was introduced in the early 1960s. Multidiffused devices are still being fabricated today, primarily for discrete devices. However, most bipolar integrated circuits now use the epitaxial process because of the improved device performance obtainable.

Epitaxial Process

Around 1962 a number of semiconductor companies announced products utilizing an epitaxial or "epi" process.

The cross-section of an epitaxial transistor is illustrated in Figure 4.12-2. For the structure illustrated, the N-type epi layer serves the same function as the diffused N layer in Figure 4.12-1 and the subsequent processing is similar to that used in the triple-diffused process. We have shown the epi layer deposited on a highly doped N-type substrate for this discussion, as compared with the P-type substrate used in the multidiffused device.

The most significant advantages of the epitaxial approach are:

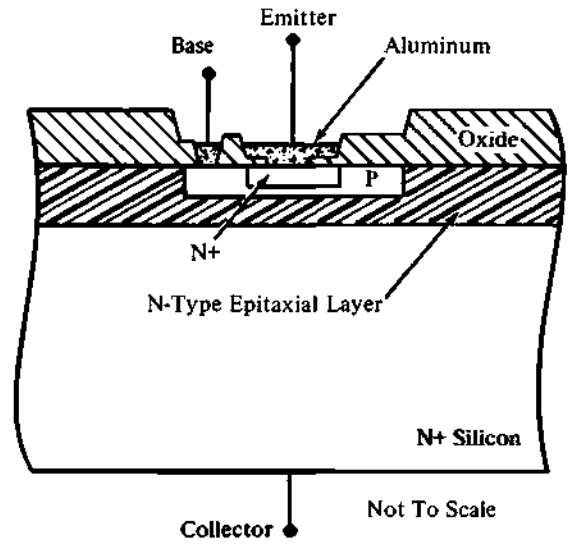
- An epitaxial layer of either polarity, N or P, and of lower dopant concentration than the substrate can be deposited on the silicon wafer. Figure 4.12-2 illustrates the case where a lower concentration N-type epi layer is deposited on an N+ substrate. This combination is not realizable with a triple-diffused process.

- Unlike the triple-diffused process, an epi layer has a uniform dopant concentration throughout. In the triple-diffused process, the concentration of dopant is highest near the surface and lowest where the N diffusion meets the P substrate.

- The P and N+ diffusions can be shallower in an epitaxial process, so that parasitic effects are less (resulting in higher speeds and lower power dissipation) and geometries can be made smaller.

These three advantages allow for the design and fabrication of transistors and circuits having higher voltage, higher current, and higher frequency performance than their triple-diffused counterparts.

Figure 4.12-2
CROSS SECTION OF AN EPITAXIAL BIPOLAR TRANSISTOR



Source: DATAQUEST, Inc.

4.12 Bipolar Technology

DISCRETE DEVICES

Diodes

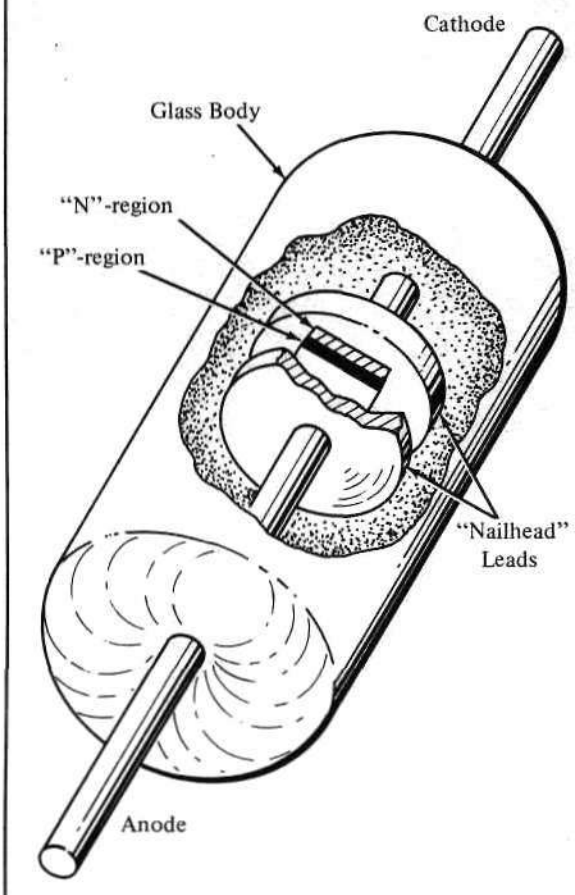
Diodes are two-terminal devices that conduct current in one direction of flow, but not in the other. The two terminals are called anode and cathode—a holdover from vacuum tube technology. As we discussed in Section 4.10, a PN junction forms the diode; the P section of the junction is analagous to the anode of a vacuum tube and the N section is analagous to the cathode.

There are many different types of diodes, each used for various specific applications. The primary types include signal diodes, rectifiers, Schottky barrier diodes, and Zener diodes.

Signal Diodes

Signal diodes, which are defined as those diodes where the forward current is under 100 mA, are manufactured by diffusing a single junction across an entire wafer of silicon and subsequently metallizing both sides of the contacts. The wafer is then sawed into a large number of square diode chips which are encapsulated in tubular glass packages as shown in Figure 4.12-3. The two nail head leads are held in a compression by the glass of the package. Signal diodes are generally smaller than other diodes and are used as rectifiers for low current power supplies, detectors for lower frequency circuits, such as television and radios, and for steering of computer signals where integrated electronics has not been employed.

Figure 4.12-3
GLASS ENCAPSULATED SIGNAL DIODE



Source: DATAQUEST, Inc.

Rectifiers

Rectifiers are large area PN junction diodes. They are manufactured by the same general technology as signal diodes but with more care so that defects will not occur in the large areas. Rectifiers with extremely high current capacity may be as large as 2 or 3 inches in diameter and handle hundreds of amps of current or kilowatts of power. These devices with their contacts are often termed "hockey-puck" diodes. Since rectifiers carry large currents and correspondingly higher power, heat transfer must be a primary consideration in the design of rectifier encapsulation. Some applications of rectifiers sustain high voltages—up to several thousand volts. The peak inverse voltage (PIV)

is determined by the breakdown voltage of the diode; higher voltages can be designed by the appropriate choice of semiconductor doping levels. Care is required to achieve high PIVs since many of the processes will create leakage paths in parallel with the diode, lowering the effective breakdown voltage.

Schottky Barrier Diodes

A Schottky barrier diode is formed by the deposition on a semiconductor surface of a suitable metal, such as platinum, aluminum, or molybdenum, which forms an effective junction with relatively high resistivity semiconductor materials. Early Schottky barrier diodes were manufactured by the use of tungsten whisker contacts on semiconductor material and were known as "point-contact diodes." These devices were employed in radar detectors as early as World War II. The use of photolithography has allowed Schottky barrier diodes to be formed using the metal deposition methods outlined previously. These diodes have somewhat lower barrier voltage and power capabilities compared with regular PN junction diodes.

The lower barrier voltage of Schottky barrier diodes has been used advantageously in TTL integrated circuit logic by paralleling the collector-base junction of transistors. The Schottky diode clamps the transistor; by not allowing it to saturate, faster turn-off times are possible. Thus, the term Schottky-TTL has risen.

Zener Diodes

When a diode is operated with a sufficiently high reverse voltage, it breaks down and allows a large current to flow. The breakdown voltage is determined by the dopant levels and geometry and can be precisely controlled. If the diode is designed to handle the power dissipated in the breakdown condition, this controlled voltage can be used as a reference. Diodes used in this manner are known as "Zener" diodes.

Zener diodes are manufactured much like other semiconductor diodes. They are used in all applications where a current-independent voltage drop is required. Typical applications include voltage references in power supplies, DC level shifting and biasing circuits. Often two diodes that are alike will be placed in series in a back-to-back fashion so that operation of the unit is independent of insertion orientation.

Transistors

The word transistor is derived from a contraction of the term transfer resistor, which describes the basic operation of the device. The input of a transistor appears as a low resistance or impedance circuit to the applied input signal (electrical current). This input signal current is transferred by the device to a high resistance circuit at the output.

There are many different types of bipolar transistors which are dedicated to specific applications, such as power, small signal, audio, radio frequency (RF), and switching. These transistors fall into two primary categories—NPN and PNP.

NPN Transistors

The NPN transistor is generally manufactured with a multidiffused or epitaxial transistor having a vertical cross-section consisting of a P-type layer sandwiched between two N-type layers, as illustrated in Figure 4.12-4. The N+ diffusion in the center of the device is the "emitter," so named because it emits the electrons that carry current. Electrons from the emitter travel down into the P or "base" diffusion. In most transistors, more than 98 percent of the electrons travel through the base and are

Figure 4.12-4

CROSS SECTION OF A TRIPLE-DIFFUSED NPN TRANSISTOR SHOWING ELECTRON FLOW

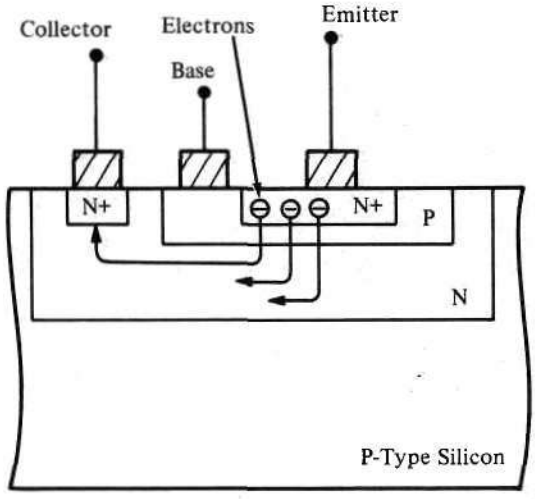
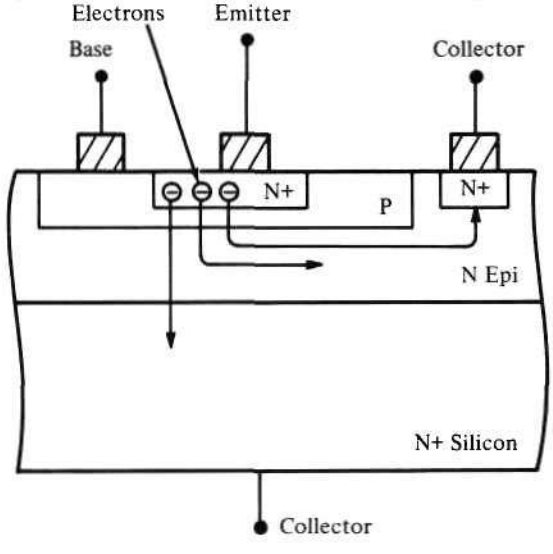


Figure 4.12-5

CROSS SECTION OF AN EPITAXIAL NPN TRANSISTOR SHOWING ELECTRON FLOW



Source: DATAQUEST, Inc.

collected in the N+ "collector." The flow of electrons is illustrated in Figures 4.12-4 and 4.12-5.

In the multidiffused transistor of Figure 4.12-4, the current flows downward through the base, into the collector diffusion, and then back up to the metallized collector contacts. An N+ area is diffused into this collector, where contact is made with the metallization. This approach is used to ensure excess electrons in the region and prevent the aluminum-N interface from behaving like a junction, which would occur since the metal is P-type and diffuses slightly into the N diffusion.

Electron flow in the epitaxial transistor shown in Figure 4.12-5 occurs through the N+ silicon substrate which serves as the collector or through the standard topside collector contact. The N epi on N+ substrate transistor structure is commonly used for discrete devices, but not for integrated circuits where each transistor must be electrically isolated from another. We will discuss a new bipolar integrated circuit technology later, however, which does use NPN transistors fabricated similarly to that shown in Figure 4.12-5.

PNP Transistors

The PNP transistor is defined like the NPN, by its vertical cross-section, as shown in Figures 4.12-6 and 4.12-7. The operation of the PNP is analogous to that of the NPN, except that the carriers of electrical current are now positive "holes" rather than negative electrons. Moreover, the polarity of the current and voltages applied are reversed from positive to negative.

The use of PNP transistors in integrated circuits is limited, since virtually all ICs use the higher speed NPN devices. However, as we discuss later, a lateral version of the PNP transistor, combined with a vertical NPN, is used in many linear integrated circuits.

4.12 Bipolar Technology

Figure 4.12-6
MULTI–DIFFUSED PNP TRANSISTOR

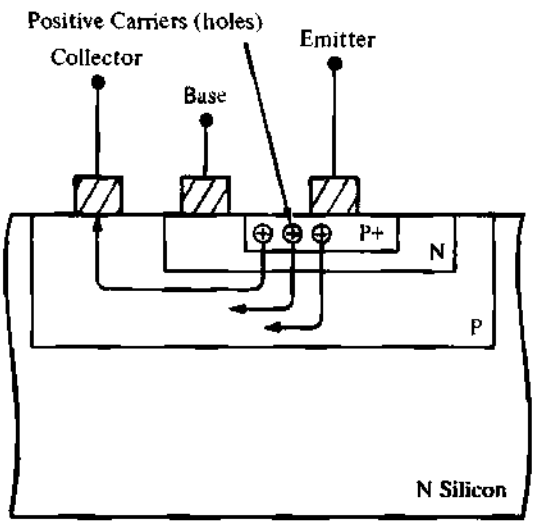
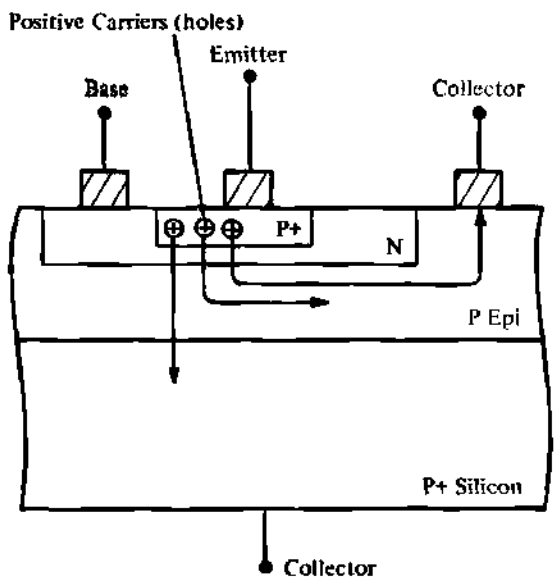


Figure 4.12-7
EPITAXIAL PNP TRANSISTOR



Source: DATAQUEST, Inc.

Unijunction Transistors

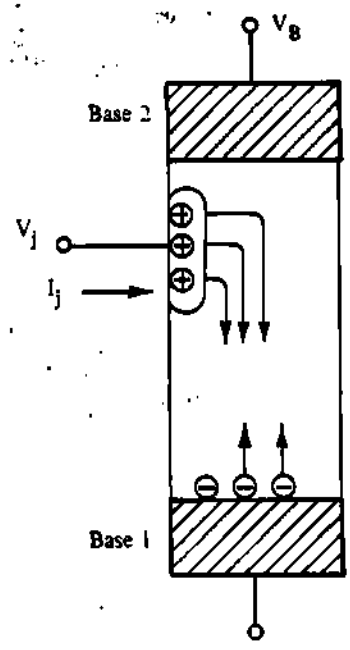
A unijunction transistor has a single PN junction with two (ohmic) base contacts, as shown in Figure 4.12-8. It is used as a switch or relaxation oscillator; its operation depends on resistivity modulation (lowering) caused by large minority-carrier injection. The normal unijunction transistor cannot be used in monolithic integrated circuits because the requirements for a shaped bar, alloy junction, and specific atmosphere are undesirable from the standpoint of compatability. A modified, compatible structure has been designed with essentially similar electronic characteristics.

Junction FET

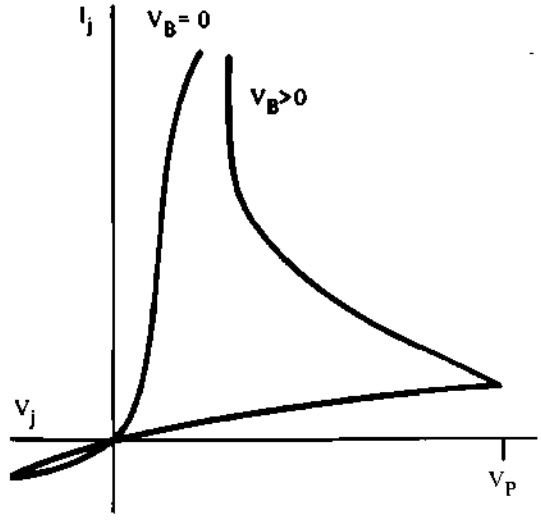
Like the transistor, a field effect transistor (FET) has three terminals. The main terminals are known as the source and the drain, with the gate terminal controlling the current flow between the other two terminals. A junction FET is manufactured by using a PN junction for the gate. As shown in Figure 4.10-10 the PN junction is reverse biased to control the electric field between the source and drain terminals, modulating the resistance between them. The technology utilized to fabricate junction FETs is very similar to that needed to fabricate PNP and NPN transistors.

A junction FET may be a P-channel FET or an N-channel FET depending on the type of doping in the source-drain region. The gate diffusion and the substrate of the device must be of the opposite impurity type from the source and drain. The operation of junction FETs is essentially the same as that of MOS FETs. Junction FETs were manufactured earlier because the control of the surface impurities required in a MOS FET was not possible. MOS devices require less room, however, and as a result have been exploited for integrated circuitry. They are the subject of another sec-

Figure 4.12-8
UNIJUNCTION TRANSISTOR



(a) Cross section showing current and electron flow



(b) Current-Voltage characteristics

Source: DATAQUEST, Inc.

tion in this Technology Chapter.

Thyristors

Thyristors are a class of bipolar devices that act as switches. Unlike transistors, thyristors are turned on with a quick pulse of current and remain on even though the applied current stops. They are generally built to handle high-power and, although they have two stable states, are rarely used to process information.

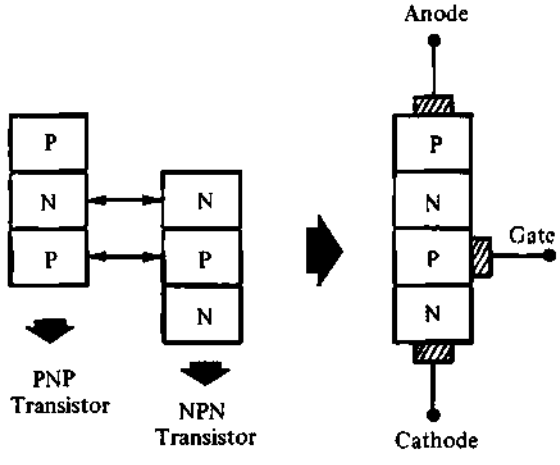
Silicon Controlled Rectifiers (SCR)

The SCR is the most widely known thyristor and is now commonly used in automotive ignition systems (i.e., capacitive discharge (CD) ignition systems), regulated power supplies, automobile alternators, and fluorescent lighting. An SCR is a four-layer semiconductor device, approximated by the superposition of two electrodes of a PNP and a NPN transistor. A visual representation of an SCR is given in Figure 4.12-9.

The SCR is usually nonconducting or "off." A current applied between anode and cathode will cause it to conduct, provided the voltage is above the minimum required to switch the SCR on. This minimum voltage is controlled by the current applied to the gate terminal. The higher the gate current, the lower the turn-on or switching voltage. Once the SCR is on, the main current flow is independent of applied gate current. It remains on until the main current is externally reduced below that needed to sustain the "on" state.

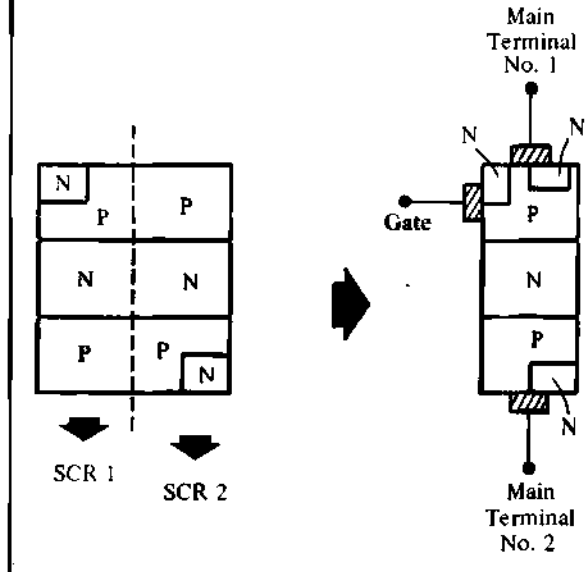
An applied voltage of reverse polarity will not turn on an SCR, so current flow is "blocked" in this direction. Current flow only occurs in the "forward" direction provided a minimum, gate-controlled, switching voltage is exceeded.

Figure 4.12-9
SILICON CONTROLLED RECTIFIER (SCR) CROSS SECTION



Source: DATAQUEST, Inc.

Figure 4.12-10
TRIAC CROSS SECTION



Source: DATAQUEST, Inc.

Triacs

The triac is a three-terminal, five-layer device having two main terminals and a gate electrode. It is used in such applications as motor controls, light dimmers and power switching systems. Its cross-section is represented in Figure 4.12-10, which also illustrates that the device essentially is two parallel SCRs oriented in opposite directions.

Unlike the SCR, a triac is bidirectional and will switch from the "off" state to the "on" state with either polarity of applied voltage, positive or negative. This switching point is controlled by the current applied to the gate terminal. A good triac will require the same magnitude of switching voltage and conduct the same magnitude of current under either polarity of applied voltage.

Diacs

A diac is a two-terminal, three-layer device with a transistor-like structure. Unlike the triac, which is essentially current-dependent, the diac is voltage-dependent. The diac changes from a nonconducting state to a conducting state when a minimum voltage of either polarity is applied. Because of their symmetric characteristics and the fact that the current increases as the voltage decreases once the switching voltage has been surpassed, diacs have been found to be ideal for use in triggering (turning on and off) triacs; that is their principal application.

4.12 Bipolar Technology

INTEGRATED CIRCUITS

General Comments

An IC is an electronic circuit in which all of the normally individual circuits components, such as transistors, diodes, resistors, and capacitors, have been produced and interconnected on a single, monolithic piece of silicon. By using a sequential combination of photolithographic and high temperature chemical processes, thousands of circuits may be produced simultaneously on a single three-inch diameter silicon wafer. Processed in batches through each manufacturing step, these wafers in turn produce tens of thousands of circuits at a time.

The cost of producing these circuits can be low because of the low labor content per device which results from batch processing. Moreover, they occupy very little space and consume minimal amounts of power. This approach is contrasted with previous techniques that required tedious hand soldering of hundreds of individual components onto a printed circuit card. Today, bipolar ICs containing more than 14,000 components are being fabricated on silicon chips that are less than three-sixteenths of an inch per side.

This subsection describes the manufacture of bipolar ICs, defines the functional types that are available, and briefly comments on the important product families.

The Bipolar Integrated Circuit

In integrating transistors, diodes, resistors, and capacitors fabricated on a single piece of silicon, called a die, measures must be taken to ensure that the components will not accidentally interact electrically. Moreover, additional process steps are added to improve specific transistor and circuit performance characteristics.

The fabrication of bipolar circuit components is illustrated in Figure 4.12-11. We have chosen to limit our discussion to this epitaxial approach, since it is the dominant bipolar IC process technology at present.

This transistor structure differs from that of the discrete transistor in two significant ways:

- The transistor now has a highly conductive N+ "buried layer", which is formed prior to deposition of the epi layer. This N+ layer provides a lower resistance path than the thin N layer under the base for electrons to flow to the collector contact. The result is improved electrical performance over that of the triple-diffused transistor.

- A P-type "isolation" wall has been diffused through the epi layer to the P-type substrate surrounding the sites where the components are to be formed. As shown in the figure, the N epi layer and its corresponding N+ buried layer are now completely surrounded by P-type silicon and are "isolated" from other similar N epi islands.

With the exception of the capacitor, the following three components are formed by the standard transistor process:

• Diode—The diode is formed basically as a transistor without the buried layer and with only two electrode connections, as shown in Figure 4.12-11. It is a junction consisting of N+ for one electrode and P for the other.

- Resistor—The resistor is created simultaneously with the formation of the transistor base region. Its value depends on its length, width, and dopant concentration. The longer and narrower its geometry, the higher its value. The lower the dopant concentration, the fewer the carriers available to conduct current and, hence, the higher

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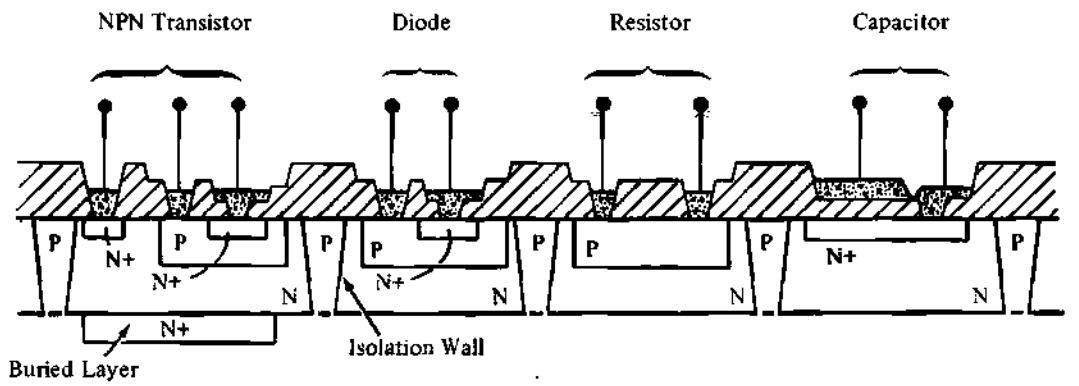
Figure 4.12-11

BIPOLAR INTEGRATED CIRCUIT COMPONENTS



Source: DATAQUEST, Inc.

the resistance to current flow. Resistors are used to limit current flow and to adjust voltage levels.

- Capacitor—A capacitor is formed by sandwiching metal (aluminum), a thin layer of oxide, and an N+ layer formed during the diffusion of the emitters. The oxide does not conduct current when voltage is applied between the metal and the N+ electrodes. Instead, it behaves like a bucket which stores charge, the amount of charge being directly proportional to the applied voltage.

Types of Circuits

Components may be interconnected in a number of combinations, depending on the circuit design and the desired electrical function. Interconnection of the respective electrodes is accomplished by the metallization pattern to form the final circuit function. Most bipolar circuits are divided functionally into two categories—digital integrated circuits and linear circuits; digital ICs can be further broken down into logic devices and memory devices.

Digital Integrated Circuits

Digital ICs operate on a binary number system. The binary system permits only two possible marks or states, "1" or "0." A "1" may be represented by the presence of a voltage and the "0" by the absence of a voltage, or any other present/absent, on/off, or yes/no relationship. For example, a light switch may be considered to be a digital "system." The light is on if the switch is up and off when it is down. Regardless of the physical or electrical process entailed, each "1" or "0" is referred to as an information "bit."

The function of the digital circuit is typically to perform a logic operation, i.e., perform operations on binary signals.

4.12 Bipolar Technology

Returning to our example of the light switch, suppose that the light is controlled by two switches, one upstairs and one downstairs. For the light to go on, both switches must be up simultaneously, i.e., the downstairs switch *AND* the upstairs switch must be up. In other words, if both switches are "on" (1s), then the light is "on" (1). This example serves as an analogy for a very simple digital logic circuit; called a 2-input AND "gate." The circuit works on the same principle: if both applied inputs are "on", the output will be "on."

Bipolar transistors function extremely well as electrical "switches." If no current is applied to the input or base of the transistor, no current flows through the collector and the transistor is "off". Conversely, an excess amount of current applied to the base (over and above that needed to turn it "on") would force both junctions to readily conduct current and the transistor would be fully "on." A transistor operating such that both junctions are fully conducting is said to be in the "saturated" mode and this operation is typical of the bipolar logic families that are available at present.

Obviously, the digital circuits available today are far more sophisticated than our simple light switch example. A digital IC may have hundreds of gates on a chip, interconnected so that the information may be processed through a number of parallel and serial logical operations before the outputs are determined. These operations or calculations can be performed in billionths of a second (nanoseconds), with the small consumption of power measured in thousandths of a watt (milliwatts). Small, high-speed computers are available today because of these digital ICs. To meet the needs of users, semiconductor manufacturers have developed various families of bipolar digital circuits. These families are discussed in a later section.

Digital IC Product and Process Families

The important bipolar product families are described in this subsection. All of these families are digital logic design, because this market is the largest. That is not to imply that advancements have not been made in the linear product and process areas. On the contrary, the linear circuits of today are more sophisticated than ever, employing field effect transistors, lateral PNP transistors, ultra high gain NPN transistors, and even Schottky diodes. These advancements, however, have been used to improve the performance of specific products, such as operational amplifiers, differential amplifiers, comparators, and regulators. They have not generated self-contained families employing a specific technology that are known by their own acronym or trademark.

Two circuit performance measures—speed and power dissipation—are critical and should be observed closely. These two parameters move in the same direction. Thus, as speed increases, so does power dissipation. Most users of ICs would like as much speed as possible for their particular application. However, the increased power dissipation is a problem because the cost of removing the generated heat, say from an enclosed computer cabinet, is very high. Consequently, the user is forced to make a compromise between speed and power dissipation, depending on his application. Figure 4.12-12 shows typical operating speed and power usage of several types of ICs.

The burden of resolving the speed-power dilemma is on the semiconductor manufacturer, who has responded by generating the multiplicity of logic families summarized in the following text.

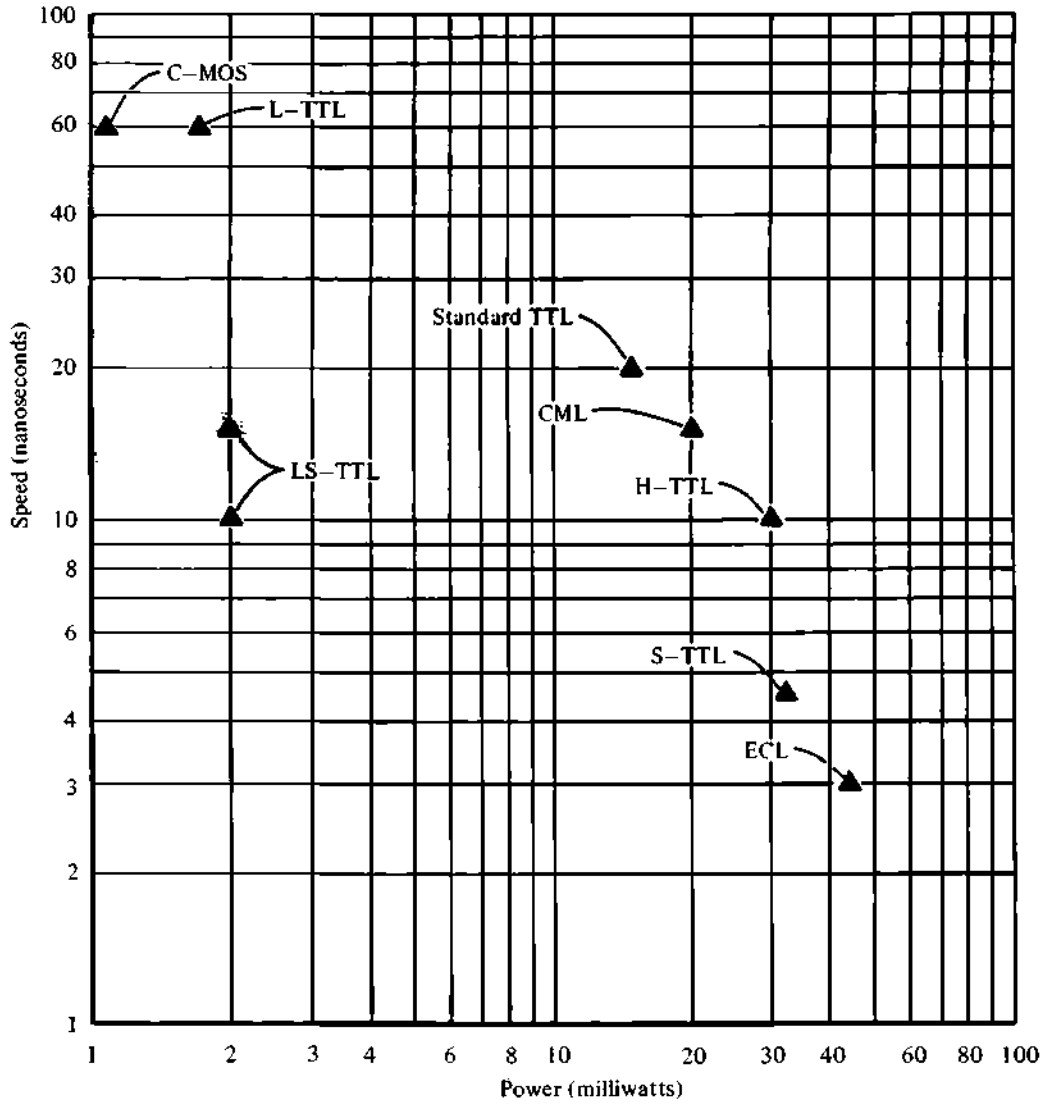
Transistor-Transistor Logic (TTL)

Better known as TTL, transistor-transistor logic is the most popular form of logic circuit

4.12 Bipolar Technology

Figure 4.12-12

OPERATING SPEED AND POWER CONSUMPTION FOR A TYPICAL GATE



Source: DATAQUEST, Inc.

today. Unlike other logic or linear circuit forms, a single transistor with multiple emitters diffused into the base handles the signal inputs to the circuit. Each emitter serves an an input, and the collector of the first transistor transfers the resultant signal to the base of a second transistor; hence, the description transistor-transistor logic.

The multiple emitter structure eliminates the need for the resistors and diodes that are required in other input structures and provides a significant space saving. At the time of its introduction in the early 1960s, TTL offered the significant advantages of higher speed and lower power dissipation over the existing logic families. However, it did not become cost effective until the late 1960s. During the past decade, TTL has become the dominant logic family. Its primary competition has been from variations on the basic TTL concept that improve speed and power dissipation.

Low Power TTL

The low power TTL family has been derived from the standard TTL devices discussed above and has been improved by increasing the resistor values. The increase in resistance reduces current flow and thereby reduces power dissipation to less than one-tenth of standard TTL. Speed is sacrificed, however, so that these circuits are three times slower than conventional TTL. These circuits can be used only in applications where lower power dissipation is essential and speed is less important than power.

Schottky TTL

This family stems from more recent process evolution and represents a significant step forward in achieving higher speeds without the attendant substantial increase in power dissipation. Again, it is a modification of, and is electrically compatible with the standard TTL family.

The Schottky TTL circuit uses a Schottky diode connected between the base and collector of each of its transistors. This special diode prevents excess charge from being forced into the base of the transistor when the transistor is being turned on. Consequently, the transistor is prevented from becoming saturated. Because it is not forced into saturation, less power and time are required to turn it on and off. Furthermore, less power is dissipated while the transistor is on, and there is a threefold increase in speed over standard TTL, with a penalty of only doubling power dissipation.

Low Power Schottky TTL

The low power Schottky TTL is the most recent of the TTL families. This product line succeeds in combining most of the benefits of the two previous families. Once again, power dissipation is reduced by the use of high-valued resistors. However, integration of Schottky diodes prevents the factor-of-three improvement in speed usually observed only in the Low Power family. The result is a family that operates at the speed of standard TTL, with only 20 percent of the TTL's power dissipation.

Emitter-Coupled Logic

Commonly referred to as ECL, the emitter coupled logic family consists of circuits in which the transistors are not driven fully on. ECL circuits are designed for high-speed performance and are more than 30 percent faster than Schottky TTL products. Because of its design, however, each logic gate draws power continuously and this power is increased as each of the inputs is turned on. Consequently, the higher speed is combined with a substantial increase in power dissipation. ECL circuits dissipate 50 percent more energy than Schottky TTL, which limits their use to more specialized applications where speed is of paramount importance.

4.12 Bipolar Technology

Memories

There are three basic types of bipolar memories that are of interest today:

- ROMs (read-only memories)
- PROMs (programmable read-only memories)
- RAMs (random access memories)

Another major type of memory, shift registers, are not generally fabricated with bipolar technology.

Read-Only Memories (ROMs)

ROMs are memories that are preprogrammed or coded to the customers specifications during the wafer manufacturing process. Programming is accomplished by photomask variations that either omit or add a transistor within an array of transistors. The omission of a transistor may specify a binary "0", while the addition of a transistor would define a binary "1." Since the information is preprogrammed and unalterable once the wafer has been manufactured, the information or binary bits within the array can be read out upon command, but cannot be changed.

ROMs are used in many applications, the most common of which is the storage of binary bits that define letters of the alphabet (8 bits per character) or the digits 0 through 9 (4 bits per character). When used in conjunction with other logic and memory circuits, ROM devices can be exercised to produce binary information so that alphanumeric characters are displayed. For example, airline reservation terminals and point-of-sale cash registers use ROMs to generate the letters and numbers displayed on a video screen.

The fact that these memories must be programmed by the semiconductor manufacturer creates a number of problems for the customer. First, each mask variation can cost up to $1,000 and the customer must wait four to eight weeks before he receives a packaged unit. Second, if a correction is needed after the ROM is placed in a machine by the customer, he must go through the entire design cycle again. Consequently, the development of programmable read-only memories has been a significant advancement.

Programmable Read-Only Memories (PROMs)

PROMs are manufactured in such a way that all of the possible transistors in an array are produced on the chip and are accessible. The customer then programs the devices with his specific code in his own factory, either by burning out a special metallized link that goes to each individual transistor or by destroying a diode. If the customer finds his program is in error, he simply removes the defective PROM and replaces it with another that has been properly programmed.

The advantage of this device to both customer and manufacturer is that the customer can maintain a supply of unprogrammed PROMS at his factory and program them as necessary. This approach eliminates the need for an inventory of specialized parts.

The disadvantage of PROMs is cost. In very high volume, most PROMs are more expensive to make and use than their masked ROM counterparts because of the increased number of processing steps, larger die size (fewer potential dice per silicon wafer), and programming requirements. However, this size differential has been narrowed considerably in the past year.

Read/Write or Random Access Memories (RAMs)

4.12 Bipolar Technology

Both of the read-only memories discussed thus far have the disadvantage that their stored information is fixed, which is not the case for read/write or random access memories (RAMs).

RAMs are memories in which each bit of information stored can be accessed independently of the other bits. Information can be written into or read out of any bit location at any time.

Because of their read/write and random access capability, semiconductor RAMs are used in computer memories, where large amounts of data are stored and frequently changed. Bipolar RAMs are limited at present to computer applications where speed is primary and the higher power dissipation and cost associated with these devices can be tolerated. Except for cache, scratchpad, and small virtual memories, RAMs are not being applied to most large, mainframe computer memories where the need for high-speed is overshadowed by memory costs.

Bipolar RAMs operate in a "static" mode, whereas MOS RAMs are available in both static and dynamic versions. A static RAM retains indefinitely, the latest information written into it, provided the basic power is supplied to the circuit. Furthermore, data stored at any bit location is changed only when different information is written into it. When a storage location is accessed to read the stored bit, the data stored at that location is not destroyed—i.e., the bipolar memory has "non-destructive read out." High speed bipolar RAMs both consume more silicon area than ROMs, and are manufactured using a more costly process. Current state-of-the-art is 1,024 bits per device.

Linear Integrated Circuits

The output of a linear circuit is proportional to the input, and this proportionality is constant. An input of one unit, for example, would result in an output of ten units, if the constant were ten. In contrast to digital circuits in which the output is either on or off, conducting or nonconducting, the output of a linear circuit continues to follow the change in the input. Continuing with our light switch example, a linear circuit would be best represented by a dimmer switch or rheostat instead of an on/off switch. The increase in brightness smoothly follows the turn of the dimmer knob and is proportional to the amount that the knob is turned.

Linear circuits display an amplification quality as indicated in the above example, i.e., the input of one unit was amplified ten times at the output. This is in contrast again with digital circuits in which the "1" or "0" displayed at the output is predefined and will always be the same magnitude as long as the inputs are above or below the switching threshold. The design of linear circuits differs substantially from that of digital circuits, since the transistors cannot go into saturation and must operate within their linear performance range.

Virtually all of the linear integrated circuits available today are bipolar. Although the basic NPN transistors used in linear circuits are similar in function to digital circuits, different performance characteristics are obtained by the modification of certain parameters during the manufacture of the circuits. Moreover, many linear circuits utilize lateral PNP as well as NPN transistors on the same chip and omit the gold doping which is usually used to increase the speed of digital circuits.

There are three major classifications of linear circuits.

- General linear circuits such as operational amplifiers (op amps), voltage regulators, and voltage comparators. Operational amplifiers are the most widely used, primarily because of their high voltage gain (output voltage is a high multiple of input voltage)

4.12 Bipolar Technology

and their ability to amplify the difference between the input voltages applied simultaneously at two input terminals. Op amps are the best electronic rendition of a "perfect" amplifier and can be used through complex mathematics, for the simulation of differential equations.

- Consumer and communications—or entertainment—circuits. Consumer products consist of timers, audio and video amplifiers for radios and TV, and automotive applications. Communication circuits are primarily applifiers used in telephone and other communication systems.

- Interface circuits that aid in the coupling of digital subsystems. These circuits amplify information signals going into or coming out of digital systems. The subclasses of interface circuits are memory drivers and sense amplifiers, line drivers and receivers, and peripheral equipment drivers.

Functional Blocks

DATAQUEST defines functional blocks as large scale logic elements that incorporate many circuits which perform a specific task. These monolithic blocks are circuits containing up to 1,000 gates on a single chip. Examples are the bipolar microprocessors and microcontrollers now being introduced commercially, adders, multiplexers, terminal controllers, and the like. These microprocessors perform many of the same calculations done by computers of much greater size and fabricated with hundreds of individual integrated logic circuits.

The advantages of these functional blocks is that ultimately they significantly lower the cost of building sensing, controlling, and computing subsystems. The lower cost will allow the use of these subsystems in applications that are not economical at present. There is a downside risk, however, that these more complex, harder-to-manufacture subsystems will displace existing semiconductor components in many applications. (This potential impact is discussed later in this report.)

BIPOLAR TECHNOLOGY TRENDS

The growth of the semiconductor industry has resulted in large part from the constant product evolutions that have taken place over the past 15 years. Bipolar circuits were the first to be fabricated commercially and since their introduction have steadily progressed through a series of design and process advancements. This trend is continuing with the recent introduction of Integrated Injection Logic (I^2L) circuits, which are bipolar circuits offering many of the advantages that have made MOS popular—i.e., low power dissipation and small size at medium speeds.

In this section, we summarize some of the major milestones that have occurred in the development of bipolar circuits, including density and performance improvements, and discuss the importance of some evolving process techniques.

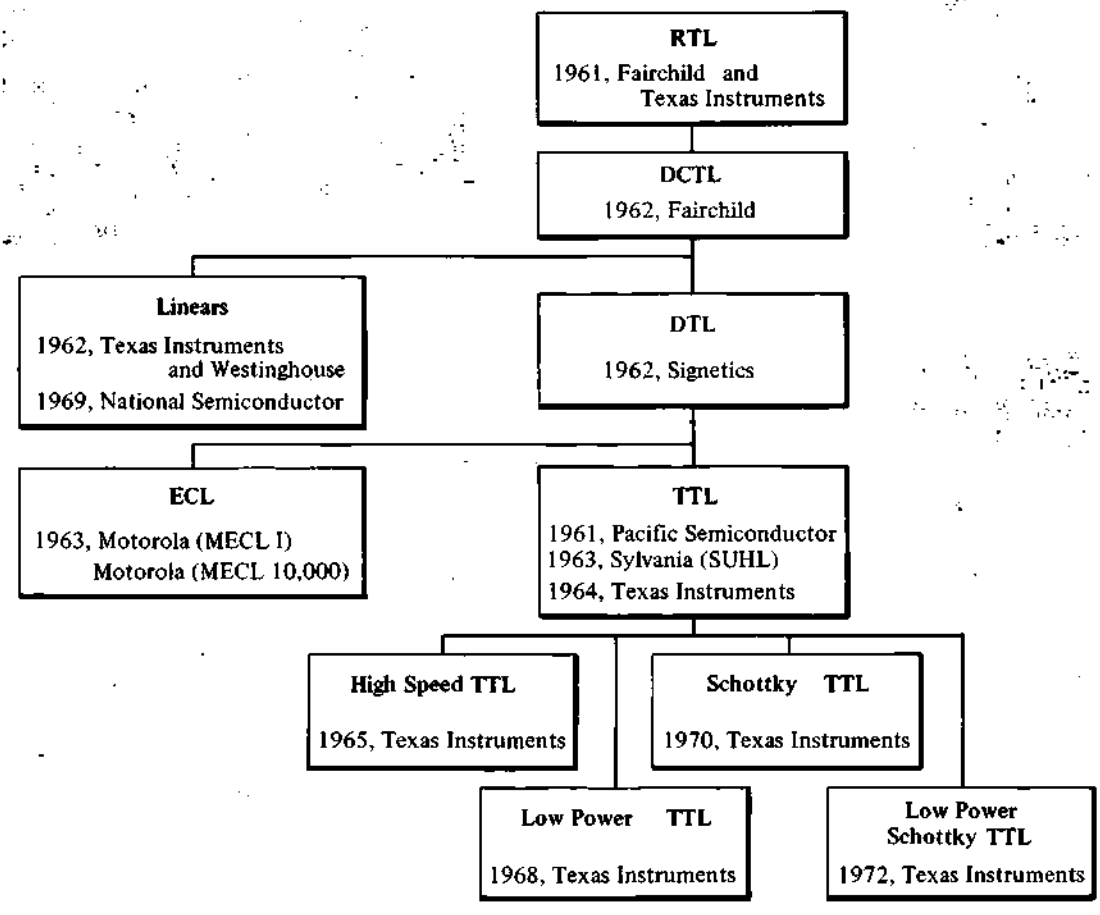
Bipolar Family Tree

The evolution of bipolar product/process families is illustrated in Figure 4.12-13. Listed along with each family is the approximate year it became a production reality and the company that pioneered a commercial product line using the technology. These companies are not necessarily the current leaders.

Bipolar integrated logic circuits began with Direct-Coupled Transistor Logic (DCTL) in 1962. This family had the disadvantage that its operation was affected by slight differences in the characteristics of individual transistors. Consequently, it was rapidly superseded by Resistor-Transistor Logic (RTL).

4.12 Bipolar Technology

Figure 4.12-13
BIPOLAR FAMILY TREE



Source: DATAQUEST, Inc.

RTL was the first family of logic circuits presented as a standard catalog line. This family, introduced in 1962 by Fairchild and Texas Instruments, had low switching speeds and poor immunity to electrical noise. It was supplanted by Diode-Transistor Logic (DTL), introduced by Signetics that same year. Although Signetics has always been a signficant supplier of DTL, its product line was not as successful as Fairchilds popular 930 series, which was introduced in 1964 and became the dominant DTL family.

Also during the early sixties, Texas Instruments and Westinghouse introduced the first commercial linear circuits. These devices were operational amplifiers (op amps) of limited performance capabilities, but nevertheless represented the entrance of ICs into the linear product area. Neither of these companies is a major factor in linear ICs at present (Westinghouse has dropped out of ICs altogether); leadership positions now rest with Fairchild and

National Semiconductor.

A number of companies were active in pioneering TTL products. Among the first to announce a product was Pacific Semiconductor in 1961. However, PSC was not successful in translating its product into a production reality. Two years later, in 1963, Sylvania introduced its SUHL (Sylvania Universal High Level Logic) family and, in 1964, Texas Instruments introduced its now dominant 5400 series. Since that time, the use of DTL has diminished significantly and is currently limited to older, established equipment.

Significant in this illustration is the dominance of T^2L—related families throughout the past decade. TI has introduced four important T^2L product families and has remained the dominant supplier in each, with Fairchild, National Semiconductor, and Signetics occupying the next three positions.

ECL was introduced as a product family by Motorola (MECL I) in 1963, but has never taken a significant share of the IC market. Its applications continue to be limited to high-speed computers and high-power dissipation is still its major drawback.

Future Trends

Component Density

In addition to speed and power performance, advancements have also been made in increasing component density. This situation is best illustrated by the ever-increasing bit density per chip of bipolar RAMs, as shown in Figure 4.12-14.

The data points on this plot represent the approximate time when memory chips became commercially available in volume. Many products were announced before the dates indicated, but volume production did not occur until months (and sometimes years) later.

As indicated on the graph, the first bipolar 16-bit RAMs became available in 1966. Both 8-bit and 16-bit devices were announced, but the latter became the dominant products. Every two and one-half to three years since 1966, the RAM bit density has quadrupled and, in 1974, the first production volumes of 1,024-bit (1K) RAMs were generated. DATAQUEST expects that bipolar RAMs of 4,096 bits (4K) will be available by 1977.

Performance

The two major performance parameters discussed so far are speed and power dissipation. In all cases, as speed increases, so does power dissipation. To blend the effects of these two parameters, designers use a parameter of the switching time (measured in nanoseconds and actually the reverse of speed) multiplied by the power dissipation (measured in milliwatts) of a given gate. Called the speed-power product, it is usually stated in picoJoules ($_pJ$) or trillionths of a Joule and is a measure of the energy required to achieve a certain frequency (or speed). Speed, power dissipation, and the speed-power product for present bipolar logic families are summarized in Table 4.12-1.

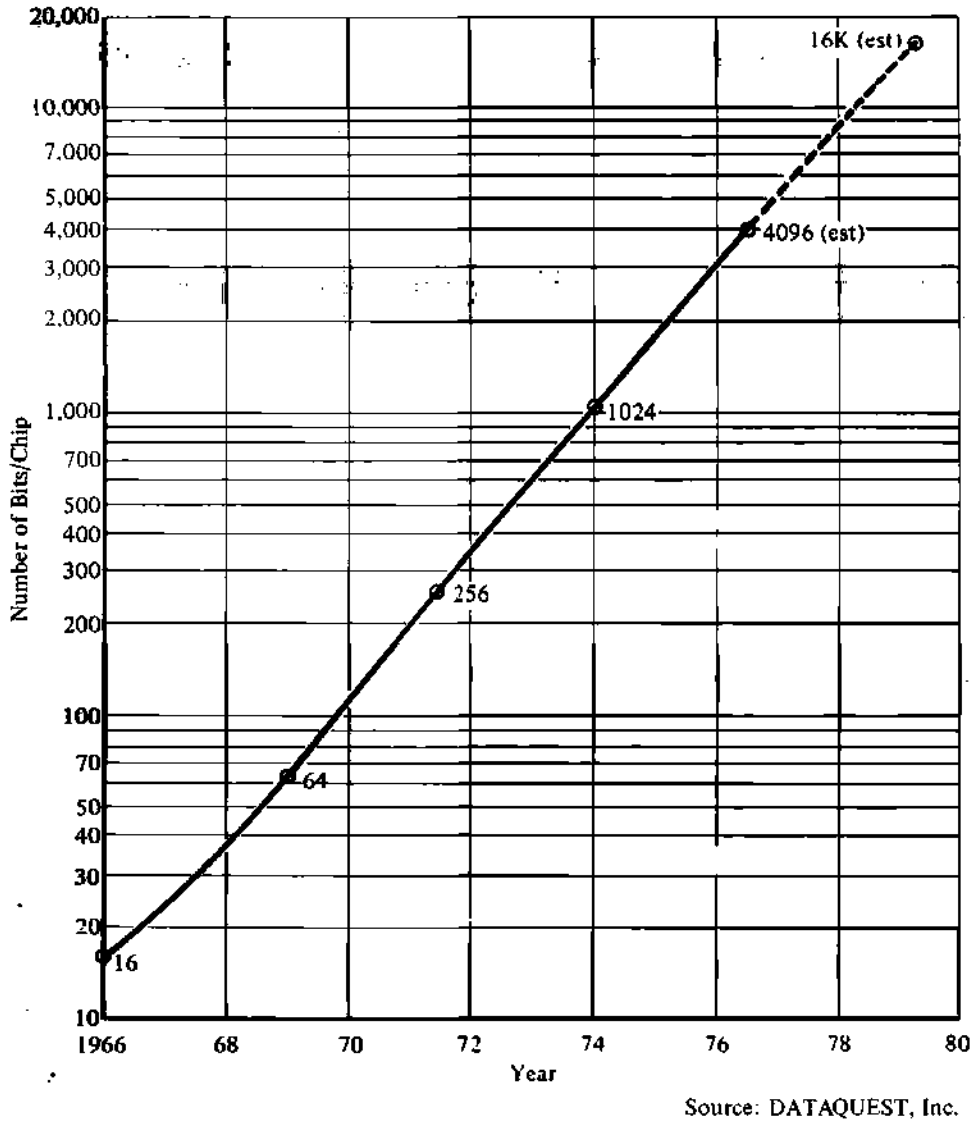
Isoplanar Technique

Planar isolation was originally introduced in the mid-1960s and called "planox" processes. The objective of using this was to minimize the height of the oxide steps that are built up during the manufacture of bipolar and MOS circuits. These steps can create small cracks ("microcracks") in the aluminum metallization lines traversing them, causing yield losses and reliability problems. They also increase the difficulty of resolving narrow metallization lines during the masking processes.

The planox process virtually eliminates the largest of the oxide steps, thus minimizing mic-

4.12 Bipolar Technology

Figure 4.12-14
BIPOLAR RAM BIT DENSITY



Source: DATAQUEST, Inc.

4.12 Bipolar Technology

Table 4.12-1

TYPICAL LOGIC FAMILY PERFORMANCE PARAMETERS

Family	Speed (nanoseconds/gate)	Power (milliwatt/gate)	Speed-Power Product (pico-Joules)
TTL	10	10	100
Low Power TTL	30	1	30
High Speed TTL	6	22	132
Schottky TTL	3	20	60
Low Power Schottky TTL	10	2	20
ECL (MECL 10,000)	2	25	50
I^2L (est.)	20	0.1	2

Source: DATAQUEST, Inc.

rocracking and allowing small metallized line widths and spacings to be realized. The latter provides for the economic manufacture of more complex circuits on the same die size.

The planox process was originally best suited for metal gate MOS products. However, because of the longer processing times required, higher costs, and the evolution of other alternatives, it was never promoted.

A process was finally introduced commercially as "Isoplanox," by Fairchild Semiconductor in 1971. The first product was a small area, high-speed, 256-bit bipolar RAM. Isoplanox-type processes have since been integrated into other bipolar and MOS products by a number of semiconductor manufacturers.

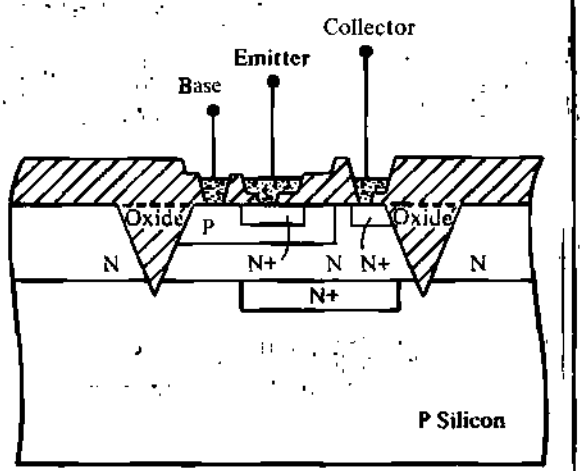
As mentioned previously, each of the transistors in an IC must be isolated from the others. This separation is accomplished in an epitaxial process by the use of an extra P isolation diffusion around each transistor which extends vertically to the P-type substrate.

In the Isoplanox process, the heavy P diffusion (P+) is replaced by oxide as shown in Figure 4.12-15. Since the oxide is an insulator, it isolates more effectively than the P diffusion, which is basically a diode and has the characteristics of one. Adjacent diffusions can be pressed right up against the wall of the oxide isolation, as illustrated, allowing significantly smaller geometries. This approach is not feasible with diffused isolations, since the P diffusion would alter the electrical characteristics of the other diffusions. Moreover, the oxide walls can be narrower (limited primarily by photolithography), so that transistors can be located closer together.

The reduction of other parasitic effects associated with the diffused junction isolation and the smaller device geometries allows isoplanar circuits to perform at higher speeds and lower power than do conventionally isolated circuits.

All of these advantages, however, come at

Figure 4.12-15
ISOPLANAR NPN TRANSISTOR



Source: DATAQUEST, Inc.

a price. The isoplanar processes are considerably longer and the initial process steps are more complex than conventional diffused isolation devices. Consequently, wafer costs are higher and the increased number of process steps makes the process more vulnerable to lower yields for comparable die sizes.

Ion implantation

Ion implantation (II) is a process in which electrically charged atoms of dopants are accelerated in an electric field and impacted on a target. As applied in the semiconductor industry, the typical dopants are boron (P-type), phosphorus (N-type), and arsenic (N-type). The target is the silicon wafer at one or more stages in its process cycle.

Much like its thermal diffusion process counterparts, the source atoms can be directed to specific silicon areas by using oxides to protect areas that will not be doped. However, there are other distinctions that make it substantially different from standard diffusion processes:

- Control of process parameters is substantially better with ion implantation than conventional processes. Since each atom has a charge associated with it, the total flow of charge can be monitored precisely as electrical flow of current. Hence, virtually every dopant atom can be counted.

- Wafers are implanted by having the ion beam sweep back and forth across their area. Dopant concentrations are more uniformly distributed across a wafer.

- All depositions are performed at moderate temperatures. The deposited or implanted dopant concentration is dependent on implantation time, beam energy, and beam current. The longer the time and the higher the energy, the greater the dopant concentration. Control is achieved electronically with high dopant concentrations taking long times. Consequently, semiconductor manufacturers do not use ion implantation except where precise control of other special characteristics are needed.

Furthermore, ion implantation has unique properties compared with diffusion:

- Dopant ions are implanted into the silicon to depths ranging from a few hundred angstroms to almost a micron.

- Dopant atoms can be implanted through thin layers of silicon dioxide (oxide), without degrading the oxide quality. In contrast, diffusion processes usually occur on unprotected silicon regions. Dopants can "melt" through the oxide layers, but this substan-

tially changes the oxide characteristics.

- Very small amounts of dopants can be implanted precisely at concentrations 100-1,000 times lower than for diffusion processes.

Currently, there are two primary applications of ion implantation in bipolar technology, both for resistors. The first application is for low-power TTL, where the resistor values must be high to minimize power dissipation. Using standard diffusion techniques, the higher the resistance, the more the area consumed by the resistor. Since dopant concentrations cannot be well controlled at low levels in diffusion processes, ion implantation offers the advantage of precise dopant control. The use of ion implantation results in two to three times higher resistor values in equivalent areas. Alternatively, ion implantation allows smaller resistor areas for the same resistor values.

The second application is for digital-to-analog and analog-to-digital converters. These products utilize resistors whose values must be precisely controlled. Only ion implantation offers the kind of control needed to manufacture these devices in integrated form.

Discrete Semiconductor Trends

The major technical advances in discrete semiconductor devices will be a continuation of the trend toward higher power and higher frequency applications. These trends are the result of the same technological advances that allow more complex integrated circuitry. Improvements in material technology allow larger devices to be made with economic yields. Continuing improvements in phototechnology for smaller geometry patterns lead to advances in high frequency devices. Darlington power transistors—two transistors attached to give greater amplification—are a result of better technology control in semiconductor processing.

Trends in discrete devices in general are toward:

- High current capabilities—100 amps and up
- High gain power-control devices
- Increased frequency microwave devices
- Tight capacitance/voltage control diodes

The types of applications that favor the choice of designing with discrete devices are (1) power applications, (2) high frequency designs, and (3) precision electronics. Hybrid integrated circuitry is being used in these applications to miniaturize and reduce the costs of the resultant designs. In a growing number of cases, devices and integrated circuits are transferred from the producer to the user as unencapsulated chips. Testing on the individual device is desirable, but there are difficulties and it is generally not done.

4.13 MOS Technology

Like the bipolar transistor described in the previous section, MOS transistors are generally three-terminal devices. The controlling electrode is called a "gate" (not to be confused with the logic circuit) consisting of a sandwich of metal, oxide, and silicon. It is similar to the base of a bipolar transistor in that it controls the flow of current from one electrode to the other. The other two electrodes are the "source" and "drain," which are analogous to the bipolar emitter and collector. The source is the electrode from which carriers flow, and drain is where they are collected.

Unlike bipolar transistors, MOS devices are "unipolar" and bilateral. Current is conducted by either positive or negative carriers, and the source and drains are interchangeable. Moreover, current conduction takes place at the surface of the silicon rather than within its bulk; thus, MOS devices are far more senstive to surface effects. Finally, current flow is modulated by a voltage applied to the control or gate electrode of a MOS transistor, rather than a current.

MOS refers to a general process or technology from which discrete transistors and families of ICs have been derived. This section discusses MOS fabrication technologies, describes the types of devices and IC product families, and outlines the technological trends.

FABRICATION TECHNOLOGIES

There are two basic manufacturing technologies for producing MOS circuits: metal gate and silicon gate.

Metal Gate

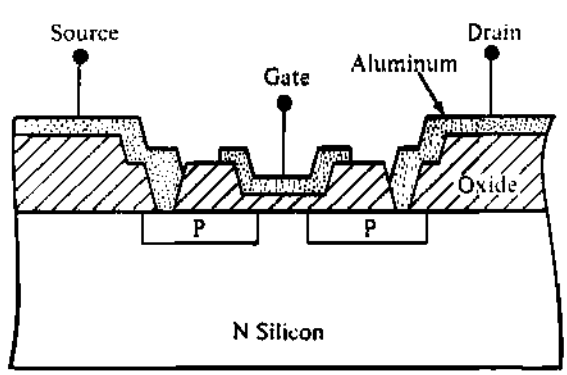
Metal gate is the oldest of the MOS technologies, dating back to 1963 when the first discrete transistors were offered. The controlling electrode of this device consists of metal (typically aluminum) covering a thin oxide layer grown over the silicon. The cross-section illustrated in Figure 4.13-1 is typical of this class of MOS products, although some variations on the structure are added by manufacturers.

The advantage of the initial metal gate process was its process simplicity, particularly when compared with bipolar epitaxial processes. No epitaxial layer, or buried layer of isolation diffusion, was necessary. In fact, only one dopant diffusion and four masking steps were needed to manufacture a device.

The disadvantages of this process were circuit performance and density. The initial P-channel products were very slow, and the density of components was limited by the single metallized interconnection layer.

To overcome performance limitations, many variations on the P-channel process were attempted and recently N-channel metal gate processes were introduced. However, none of these metal gate processes was able to blunt the thrust of the newer silicon gate process.

Figure 4.13-1
P-CHANNEL METAL GATE TRANSISTOR



Source: DATAQUEST . Inc.

4.13 MOS Technology

Silicon Gate

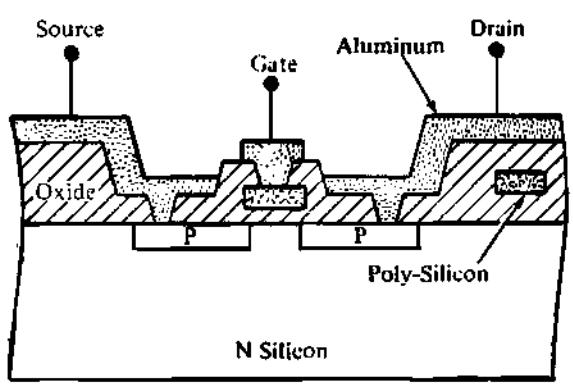
Silicon gate, introduced commercially in 1968, produced the first major significant change in MOS processing. In this device, the metal electrode was replaced by a highly doped layer of polycrystalline silicon, as shown in Figure 4.13-2. (A detailed illustration of the silicon gate process sequence may be found in the Manufacturing Section, pages 3.1-9 and 3.1-10.)

Initially applied to P-channel devices, the silicon gate process generated the following benefits:

- The voltage required to turn on the device (threshold voltage) was halved (from 4 volts to 2 volts), resulting in higher speeds and voltage compatibility with bipolar T^2L circuits.
- The conductive polysilicon could be used as an additional interconnection layer; thus, die sizes were reduced.
- The silicon electrode is self-aligned to the diffused electrodes, since this electrode is formed first in the masking processes and thereby automatically defines the location of the other two electrodes. This self-alignment significantly reduces parasitic capacitances, which increases speed and allows

Figure 4.13-2

P-CHANNEL SILICON GATE TRANSISTOR



Source: DATAQUEST, Inc.

the transistors to be smaller.

TYPES OF DEVICES

Within the metal and silicon gate process technologies, there are three types of transistors: P-channel, N-channel, and complementary. These devices in turn can operate in either of two ways: enhancement-mode or depletion-mode.

Enchancement-Mode Operation

An enchancement-mode transistor is normally off, i.e., it does not conduct current unless voltage is applied to its gate electrode. Referring to the P-channel transistors of Figures 4.13-1 and 4.13-2, this type of device consists of two diffusions (P-type, in this example) separated by a region of opposite polarity (N-type). The latter region is covered by a thin layer of oxide which in turn is covered by metal or silicon.

When a voltage of the same polarity as the substrate (negative for N-type, positive for P-type) is applied to the gate, a thin layer of silicon (a few hundred angstroms thick) under the gate oxide converts to the same polarity as the diffused beds. A "channel" is thus formed connecting the two diffusions. This channel allows current to flow from one diffused bed (electrode) to the other. As the applied input voltage is increased, current flow increases or is "enhanced."

Depletion-Mode operation

The channel of a depletion-mode device is formed during the manufacturing process. Figures 4.13-1 and 4.13-2 would be modified to show a shallow P-type layer under the gate oxide and connecting the two P beds. With no applied gate voltage, these devices are normally "on" or conducting. If a gate voltage of opposite polarity to the substrate is applied, the carriers in the channel are reduced or "depleted" and the current diminishes.

P-Channel (PMOS)

P-channel is the oldest of the three types of MOS devices and was the first MOS technology to become commercially available. The structure of this device is illustrated in Figures 4.13-1 and 4.13-2, where the diffused source and drain electrodes are P-type. A channel formed, either by application of a negative voltage (same polarity as N-type substrate) or during the manufacturing process, would be P-type. Thus, it is designated P-channel.

N-Channel (NMOS)

The N-channel structure is shown in Figure 4.13-3. It consists of two N-type wells diffused into a P-type substrate and separated by the gate electrode. In contrast to P-channel devices, the polarities of the dopants, carriers, and voltages are exactly reversed. The diffusion of a shallow N-type region connecting the two beds (depletion-mode) or the application of a positive voltage to the gate creates an N-type channel.

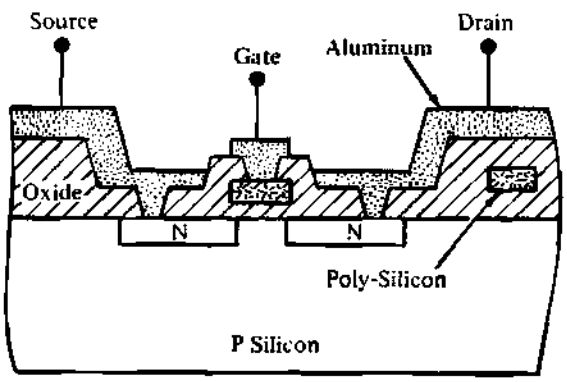
N-channel presents three main advantages over P-channel devices:

- The speed is two to three times greater
- For equivalent speeds, N-channel devices can be made smaller than P-channel devices.
- The polarity of applied and generated voltages and currents are consistent with bipolar devices.

The disadvantage is that N-channel devices are far more sensitive to minute amounts

4.13 MOS Technology

Figure 4.13-3
N-CHANNEL SILICON GATE TRANSISTOR



Source: DATAQUEST, Inc.

of contamination during the manufacturing, test, and assembly processes. This sensitivity can reduce yields and create reliability problems. Most manufacturers, however, have found that the silicon gate process substantially reduces N-channel MOS sensitivity to contamination, as compared with the metal gate process.

Complementary (CMOS)

CMOS transistors consist of one N-channel and one P-channel device connected, as indicated in Figure 4.13-4. The PMOS transistor replaces the diffused or MOS-type resistors usually used with an NMOS and operates such that it is "off" when the NMOS device is "on" and vice versa. Consequently, the CMOS device consumes much less power than a single polarity device, since the two transistors are in series and one is always "off."

Other advantages of CMOS over NMOS and PMOS are:

- The input signal always forces one transistor to turn "off" while forcing the other to turn "on." This active participation of both transistors makes CMOS faster for equivalent functions and processes.
- CMOS is far less sensitive to electrical noise on the input signal.
- CMOS devices can operate over a wider range of power supply voltages.

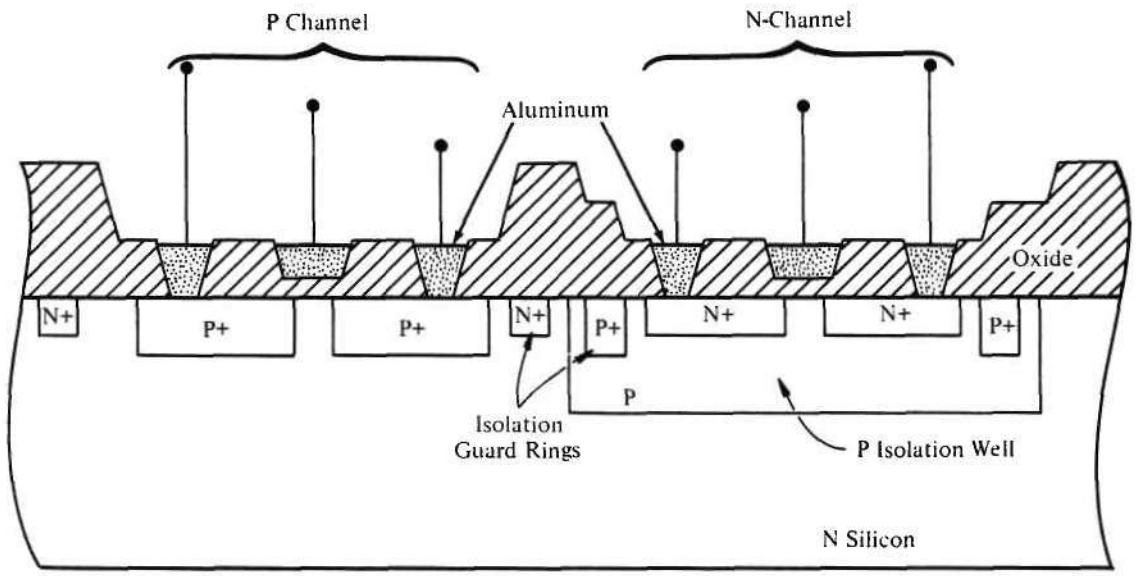
The disadvantages relate predominantly to processing. CMOS processes are substantially more complex than NMOS and PMOS processes because of the need to fabricate both transistors on the same substrate. Second, the use of two transistors causes additional silicon real estate to be consumed to form the P isolation well and the guard rings that protect against parasitic interaction between the two devices. As a result, CMOS devices are more costly.

INTEGRATED CIRCUITS

As defined in the Bipolar Section, ICs are circuits in which all components are produced and interconnected on a single, monolithic piece of silicon called a die. The basic processing principles are the same for bipolar and MOS ICs, although MOS is far more sensitive to minute amounts of contamination and therefore requires more extensive and closer process controls.

In the past, many companies did not exercise the discipline required to enforce these controls, causing them to make unreliable circuits or rendering them incapable of fabricating any parts at all. At present, however, many MOS manufacturers have good control over their processes and are able to produce a multitude

Figure 4.13-4
METAL GATE CMOS TRANSISTOR



Source: DATAQUEST, Inc.

of products with a number of processes.

The MOS Integrated Circuit

MOS transistors can be operated to simulate other components, such as resistors and capacitors. Two methods can be used to form each of these components. Figure 4.13-5 illustrates the MOS transistor used as a resistor. In 5a, the transistor is biased on with a fixed voltage applied to the gate. Since this fixes the current flow between source and drain, the channel basically behaves as a resistor. In 5b, the gate is tied to the drain and its voltage varies as the drain voltage. Current flow is again limited because the voltages to the two electrodes are the same; therefore, the depth of the channel at the drain is always constant.

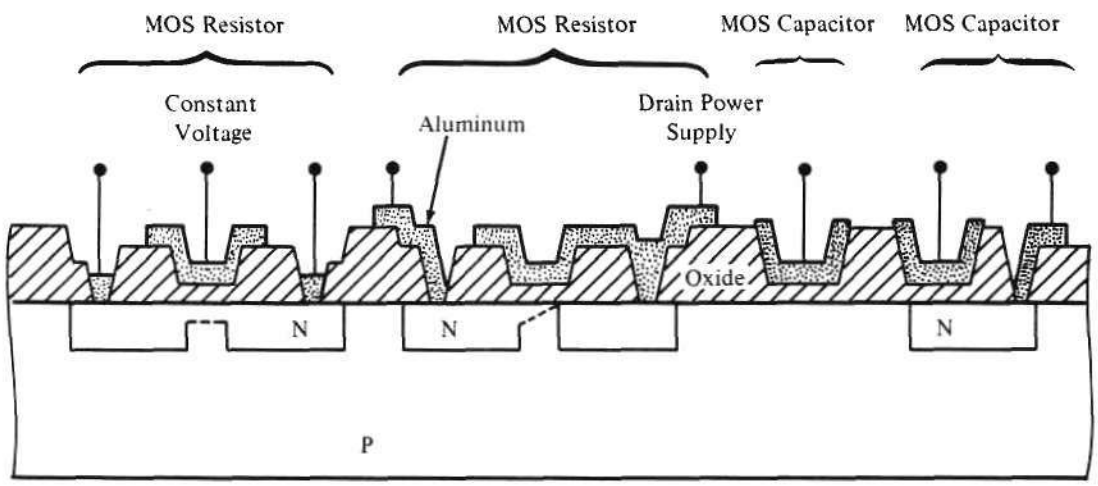
One method of forming a capacitor is shown in 5c and consists simply of an MOS sandwich. The capacitance of this structure varies with applied voltage, however, and therefore the device cannot be used for many applications. In those cases the structure illustrated in 5d is used because its capacitance is more constant.

The use of these structures allows the fabrication of very high-value resistors and capacitors in a small area. This obviously contributes to the smaller die size of MOS functions than equivalent bipolar functions.

However, the resistive components, in par-

4.13 MOS Technology

Figure 4.13-5
MOS INTEGRATED CIRCUIT COMPONENTS



Source: DATAQUEST, Inc.

ticular, are not ideal and in many applications cause the circuits to be slow. To improve the speed of MOS circuits, designers have resorted to a "dynamic" mode of operation versus the static mode used in bipolar. The characteristics of the two modes are discussed in the following paragraphs.

Static Circuits

As with bipolar circuits, a static MOS circuit is one in which the information is retained as long as the primary power supply is on. Moreover, the act of interrogating a specific data storage point within the circuit does not alter the data stored there. The storage element of a static circuit is a circuit based on the "flip-flop." This circuit has two key transistors—one is "on" the other is "off"—which will maintain that state until steered to the other state by an outside disturbance. The state of the flip-flop transistors may be changed by the "write" cycle; however, the state can be read without destruction by the "read" cycle.

Flip-flops were invented by Eccles and Jordan as part of the initial electronic digital computer. The same circuit idea has been implemented using vacuum tubes, relays, bipolar transistors, and MOS transistors. The MOS flip-flop has the advantage of small size, but it has a lower read-write speed than the bipolar flip-flop. Chains of flip-flops are used to implement arithmetic, counting, logic, and storage functions in digital computers and EDP equipment.

Alternative techniques have been explored to provide digital functions more cheaply. One has been the use of storage change on a capacitor. MOS transistors provide nearly ideal switches for this type of circuitry.

Dynamic Circuits

The concept of dynamic storage and operation has been used predominantly with MOS

products. In this approach, a unique feature of an MOS device is utilized. Since the input (gate) to the MOS transistor is a capacitor, it can store energy in the form of an electrical charge. If the quantity of this charge is sufficiently high, the MOS device will turn on and stay on. The charge will not remain indefinitely, however, since there is always some amount of charge that leaks away from this electrode, ultimately reducing it to a level that would turn the transistor off. Before it reaches that low level, the charge must be replaced or "refreshed." Because the charge will not remain even though the primary power supply is on and because the data must be continually refreshed, this type of storage is called "dynamic."

Dynamic storage can be used in all types of MOS circuits, including logic, memory, and functional blocks. Its advantages are that it is substantially faster and consumes less power than do static devices. Furthermore, fewer and smaller transistors are needed to store information for RAMs, so that many more bits of information can be stored in the same silicon area. As an example, the largest static MOS RAMs currently available contain 1,024 bits, whereas the largest dynamic RAMs contain 4,096 bits.

The disadvantages are that the refresh signals must be generated and that the information stored is "volatile," i.e., it will disappear if not properly refreshed. Moreover, the information stored at a bit location is destroyed when that storage point is interrogated. Hence, once the information is read out, it must be written back in again.

Product and Process Families

P-Channel MOS

There are a number of process families within the generic P-channel MOS technology. However, we choose to group them into two major classifications—metal gate and silicon gate.

Metal Gate PMOS

Metal gate P-channel devices have been the backbone of MOS market growth over the past decade, with calculator chips offering the primary growth products. Although the older devices are now being phased out, this portion of the technology still represents the largest market segment. However, it is decreasing or at best flattening. Very few new products are designed around this technology.

Silicon Gate PMOS

Intel introduced the first product family using silicon gate in 1969. It consisted of dynamic shift registers, a 256-bit static RAM, and eventually the now widely used 1103, a 1K dynamic RAM. The advantages of TTL compatibility, higher component density, higher speeds, and greater function complexity were all combined in these products. The products were subsequently second-sourced by a number of other semiconductor houses, thus speeding the shift to silcon gate.

The silicon gate process is far more complex than are metal gate processes, approaching bipolar processes in complexity. However, its performance advantages, coupled with the ability to build complicated products more economically, have helped it to displace metal gate for new designs.

The advantages of the silicon gate IC process over metal gate as one example are summarized in Table 4.13-1, for two dual 100-bit static shift registers. Signetics' S2005 is a P-channel metal gate device and its 2510 is a P-channel silicon gate version.
The silicon gate product offers more options (each is an advantage to the user, but each

4.13 MOS Technology

Table 4.13-1

COMPARISON OF METAL GATE MOS AND SILICON GATE MOS

Product	Area	Features					
		3-State Outputs	Recirculating Logic	TTL Compatibility	On Chip Clock	Speed	Power
S2005 (metal gate)	8,190 square mils	No	No	No	No	1 MHz	225mw
S2510 (silicon gate)	6,970 square mils	Yes	Yes	Yes	Yes	2 MHz	115mw

Source: DATAQUEST, Inc.

consumes silicon wafer area), at twice the typical operating speed and half the power dissipation, on a 15 percent smaller die.

In spite of these advantages, however, most semiconductor companies and users consider P-channel silicon gate as a stepping stone to the technology that is most desirable—N-channel.

N-Channel MOS

The advantages of N-channel MOS discussed earlier still apply when the process is applied to ICs. Higher device speeds translate to higher circuit speeds, and the polarity of currents and voltages make the circuits directly compatible with the bipolar circuits. Metal gate and silicon gate processes are used for fabricating N-channel circuits; both result in products that operate at higher speeds and with lower power consumption than PMOS.

Metal Gate NMOS

The primary metal gate products available today are RAMs aimed at the high-speed computer memory market. These 1,024-bit devices operate at more than twice the speed of silicon gate P-channel RAMs, such as the 1103, and about half the speed of bipolar RAMs. In the latter comparison, the lower MOS speed is offset by lower power dissipation and lower costs.

The density of these RAMs is limited, however, because the single metal interconnection layer does not allow efficient space utilization. For this reason, silicon gate N-channel is now becoming the preferred technology for RAMs.

Silicon Gate NMOS

The silicon gate process offers the same advantages for N-channel as it does for P-channel. Its primary advantages over N-channel

metal gate are:

- Higher component density because of the polysilicon interconnection layer.
- Less sensitivity to manufacturing processes because the gate oxides are protected by a polysilicon layer.

The composite advantages of NMOS over PMOS and silicon gate over metal gate have made silicon gate NMOS the preferred technology.

Few new products are currently being committed to the older PMOS silicon gate products. The new 8-bit microprocessors, 4K dynamic RAMs, 1K static RAMs, and 1K high-speed dynamic RAMs are all N-channel. They should be the growth products of tomorrow.

Complementary MOS

CMOS circuits are available in both metal and silicon gate versions. Use of these parts is limited to applications where power dissipation and tolerance to electrical noise are primary concerns.

Metal Gate CMOS

Unlike single polarity P-channel and N-channel circuits, the process trend in CMOS has been continuing along the metal gate approach. Two significant product lines are being manufactured, the 4000 series by RCA and the 74C series by National Semiconductor, with the former most widely used and second-sourced.

Both product lines are a series of logic circuits, with a few smaller RAMs (64-256 bits) included. The 4000 series was derived from custom programs RCA had completed over a number of years, and the 74C series was a direct attack by National Semiconductor on the 7400 TTL family.

Because of the poor utilization of silicon wafer area by the metal gate CMOS devices and the fact that the process is less mature, the cost of CMOS is not yet competitive with equivalent bipolar products. Its use is therefore limited to those applications that are not adequately served by bipolar and single polarity MOS products.

Silicon Gate CMOS

The application of silicon gate to CMOS has been limited at best. Two major types of products are being manufactured with this process— electronic wrist watch circuits and large (512 bits or greater) static CMOS RAMs. These products are designed to take advantage of the lower power dissipation and increased performance obtained using the silicon gate process. They are premium products, commanding premium prices.

The reluctance to shift to silicon gate stems from the increased process complexity that would result. Since the polysilicon is usually doped N-type for NMOS products and P-type for PMOS products, a simply constructed CMOS process would have poly of both polarities. This is a problem, since the intersection of the two differently doped poly types would be a junction, i.e., it would conduct current in one direction, but not the other. Moreover, the self-aligned gate feature prevents the formation of uninterrupted isolation guard rings around the individual devices. This prevents the convenient fabrication of logic circuits, such as the 4000 series, which operate at higher voltage levels.

Both of the above problems may be avoided, but at the cost of a substantial increase in the number of process steps. Unless some major breakthroughs are forthcoming, it is unlikely that silicon gate CMOS circuits will soon supplant metal gate for CMOS logic circuits. There seems to be little choice in RAMs, however, since die size and performance are

paramount. Silicon gate CMOS will almost undoubtedly be the dominant technology for large CMOS memories.

MOS TECHNOLOGICAL TRENDS

The evolution of MOS technologies has been as rapid as that of bipolar technologies. Originally hailed as a replacement for bipolar, it has now settled into a niche that typically does not compete with that technology. Its advantages are still low power dissipation, high density, and low costs.

However, as indicated earlier, the MOS processes are becoming more complex with each passing year. The original four-mask, single diffusion process is evolving into the complex silicon gate N-channel and CMOS processes we have been discussing. Further refinements, such as ion implantation, are also being integrated to increase circuit performance. At the same time, new bipolar process techniques, such as integrated injection logic, are enabling it to acquire many of the performance features once solely the domain of MOS.

MOS Family Tree

Evolution of the MOS product families is illustrated in Figure 4.13-6. The company pioneering commercial products using the technology and the approximate year it became a production reality are shown on the first line, and the present technology leader is shown on the second line.

The MOS IC industry originally started with the introduction of a metal gate, high threshold, P-channel dynamic shift register by General Microelectronics (GME) in 1964. Unfortunately, most potential users were skeptical and cautious, as GME continued to have serious yield and reliability problems over the ensuing years.

It was not until two years later that the credibility of MOS was re-established. American Microsystems (AMI) quickly became the leader and established itself as a solid supplier of high-quality, custom, metal gate PMOS products. National Semiconductor introduced the first standard product line, using <100> orientation silicon to achieve low turn-on voltages and a limited bipolar compatibility. General Instruments countered with a nitride gate process, but remained the only manufacturer using this process. The rest of the MOS companies followed National's lead and coverted to <100> silicon.

The next major step occurred in 1968 with the announcement of silicon gate P-channel MOS products by Intel and Fairchild. This technology made complex, high performance MOS products available at reasonable prices.

By 1972, the first silicon gate N-channel products were introduced by Intel and metal gate CMOS (first introduced by RCA in 1968) had begun to pick up substantial momentum. Moreover, the silicon-on-sapphire (SOS) products introduced the previous year were starting to reach the marketplace.

The technological evolution continued with introduction of the first silicon gate CMOS product in 1973 and the introduction of the first charge-coupled devices (CCD) for imaging in 1974.

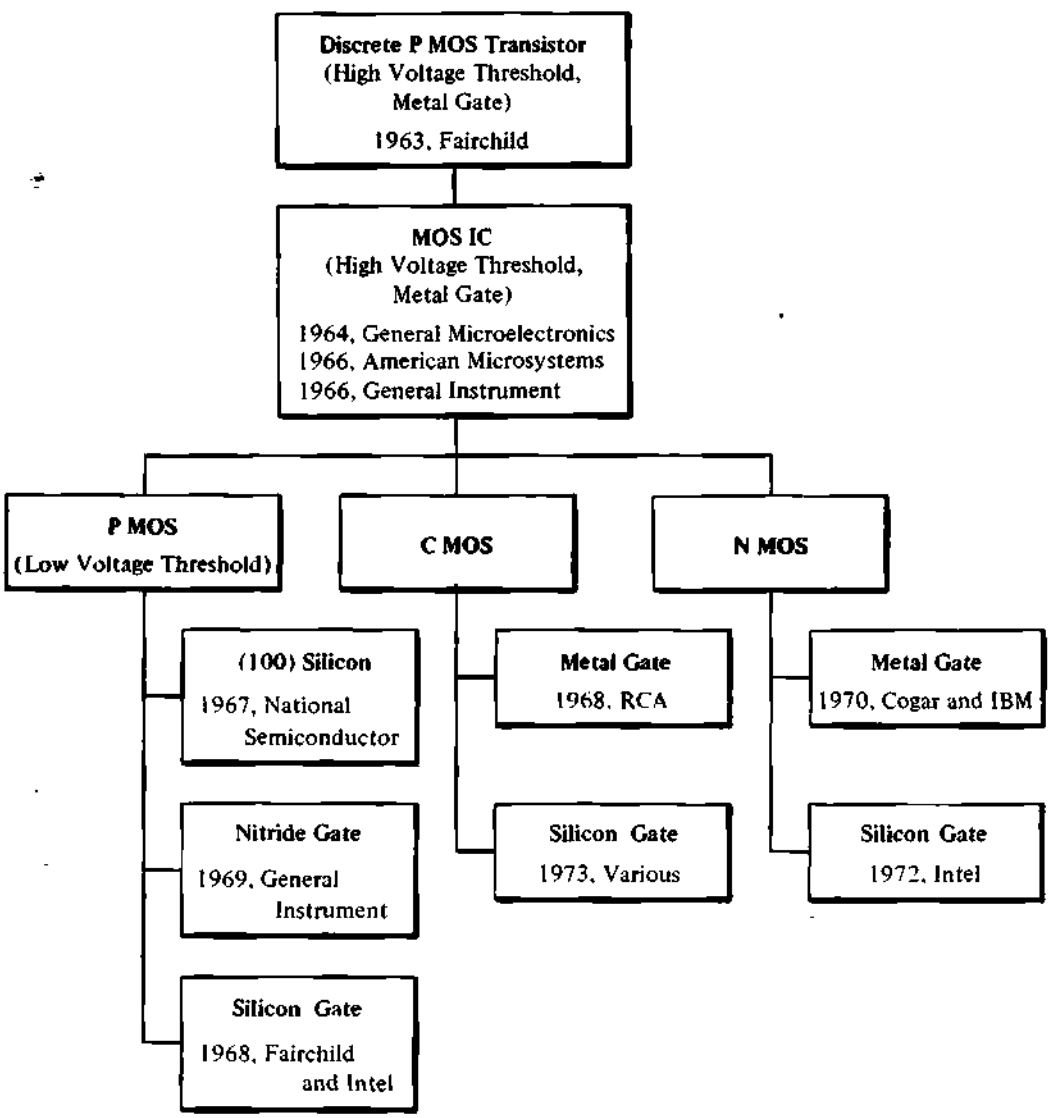
Future Trends

Component Density

As in bipolar integrated circuits, MOS circuits have rapidly increased in circuit density over the past decade. To illustrate the trend, Figure 4.13-7 depicts the growth in memory bits per chip, beginning with the first 256-bit dynamic PMOS RAM in 1969. The 256-bit RAM was initially produced in volume by General Instruments and was used by the com-

4.13 MOS Technology

Figure 4.13-6
MOS FAMILY TREE



Source: DATAQUEST, Inc.

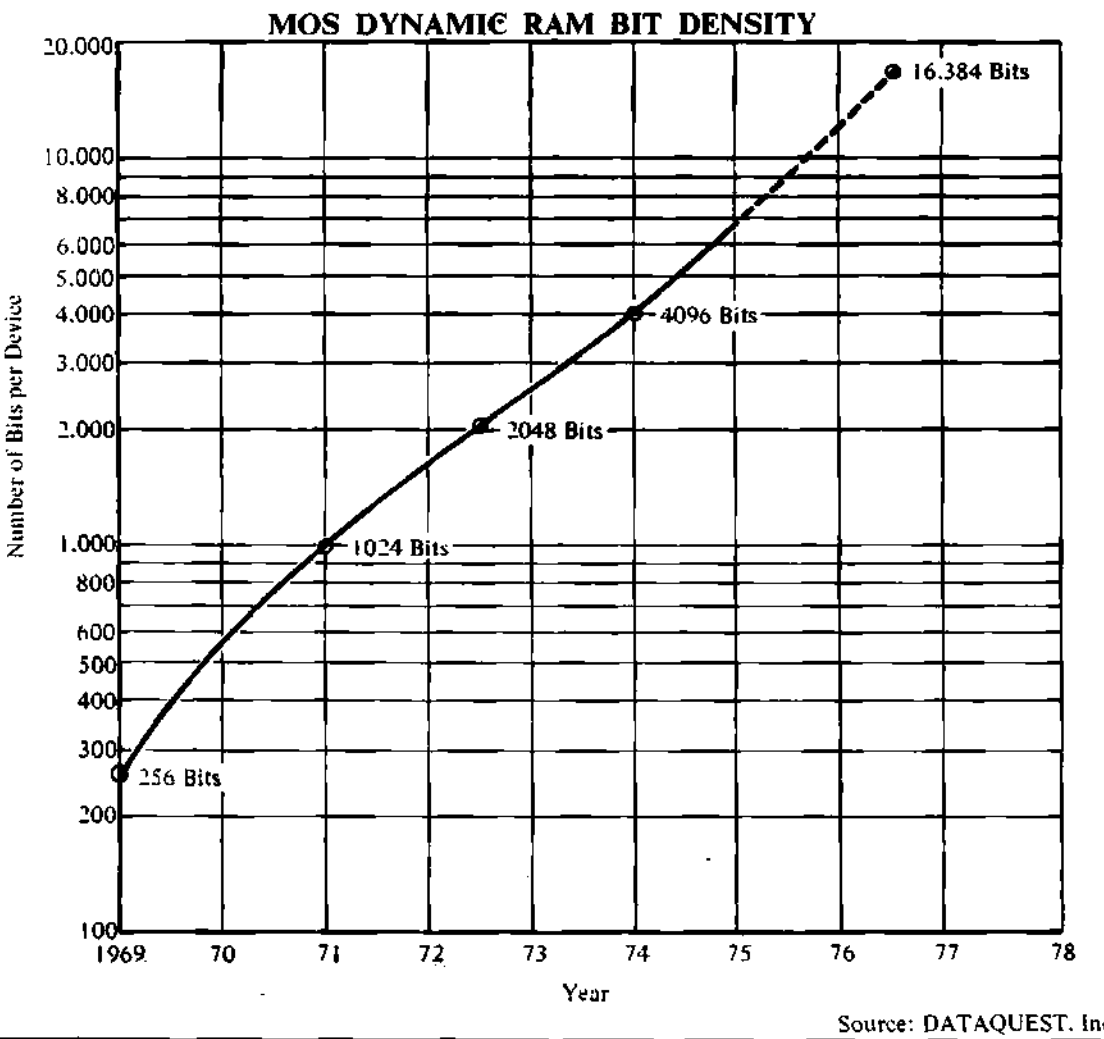
puter group of National Cash Register. It measured approximately 13,000 mills^2 and contained more than 800 transistors.

The 1K RAM was introduced by Intel (1103) and Advanced Memory Systems (6002), with the former becoming the most widely used version. The 1103 RAM measured more than 16,000 mill^2 and consisted of more than 3,100 transistors.

The 2K RAM was an anomaly, since most computer manufacturers prefer progression in bit density by factors of four, beginning with the 256-bit RAM. A 2K RAM was developed on contracts from Honeywell and was used primarily by that company.

Newest on the marketplace is the 4K RAM, most recent versions of which use a single transistor for each memory bit. However, the initial chips were relatively large, at 28,000 mills^2, and contained more than 12,000 transistors. More recent versions are less than 20,000 mills^2 and contain fewer than 5,000 transistors.

Figure 4.13-7



Source: DATAQUEST, Inc.

4.13 MOS Technology

On the basis of historical growth in bit density, DATAQUEST expects that 16K RAMs will become available by mid-1977. Again, the 8K RAM is not expected to become a large factor because of its less than ideal organization.

Performance

The performance of MOS products can be measured in a number of ways. Since speed and power dissipation are intimately related, both are considered here. Speed is characterized as memory bit access time for MOS RAMs and is measured in nanoseconds. Power is measured in milliwatts.

Two speed curves are shown in Figure 4.13-8, one for 1K RAMs and the other for 4K RAMs. The speed of the 1K RAMs has steadily increased, with the present RAMs running at 60 nanoseconds versus 300 nanoseconds in 1971. At the same time, power dissipation has increased from less than 350 milliwatts in 1971 to 400 to 500 milliwatts today. A performance factor relating these two characteristics, called "speed-power product," was discussed in the Bipolar Section. The speed-power product for the original 1970 vintage 1102 was 100 picoJoules/bit. Using this measure, today's circuits at 30 picoJoules/bit are three times better than those of 1970.

The 4K RAMs are still in their embryonic growth stage. Speeds range from 210 to 300 nanoseconds, with the latter more common at present. The speed-power product is a staid 29.3 picoJoules/bit but is acceptable to those users wanting the extra bit density. Most users would like to have a part operating at less than 200 nanoseconds, at a power dissipation of less than 300 milliwatts, thereby yielding a maximum speed-power product of 14.6 picoJoules/bit. We predict the 200 nanoseconds part will be available in volume in the second half of 1975, but that the power dissipation is more likely to be 450 milliwatts (speed-power product = 22 picoJoules/bit). By 1976, 4K RAMs with speed-power of 12 picoJoules/bit (100 nanoseconds access time and 500 milliwatts) should be available.

Isoplanar Techniques

Application of the oxide isolation process to MOS transistors and integrated circuits is shown in Figure 4.13-9. As in bipolar processing, the original intent of this process, when applied to metal gate MOS circuits, was to minimize the height of the oxide steps over which metallization was to traverse.

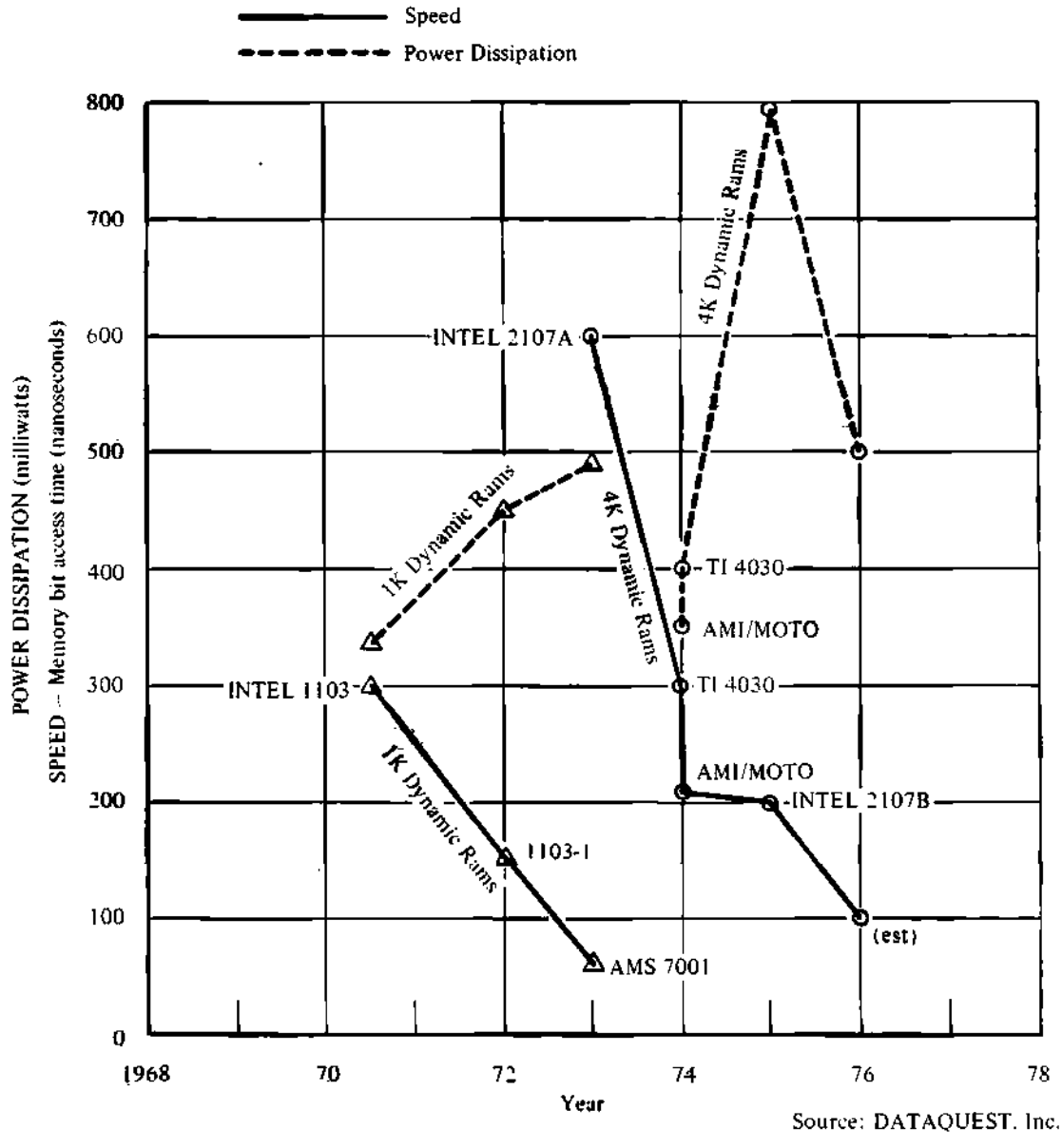
As the process is now applied, the objective is to decrease the size of the components and increase circuit performance. The size decrease is accomplished by allowing diffusions to touch the oxide walls. These walls can be made as thin as photolithography allows (typically 5 microns). This is contrasted with standard processes in which 10 to 15 microns are left between adjacent diffused beds for isolation. Performance is improved, since the oxide isolation removes part of the diffused junction parasitic capacitance that exists at the juncture of P- and N-type materials. The reduction in this parasitic allows the improvement of speed, without the normal increase in power dissipation accompanying it.

The oxide isolation process penalizes the MOS process more than it does the bipolar process, in which the oxide isolation only replaces a diffused isolation, because more complex processes are added at the beginning. As shown in Figure 4.13-10, two major deposition processes and a three-step masking etch process are added even before the processing has begun for the MOS transistors.

The increased number of steps detracts from the original advantage of MOS, which was the potential for higher yields because of process simplicity. Each of the process steps increases potential yield losses which offset poten-

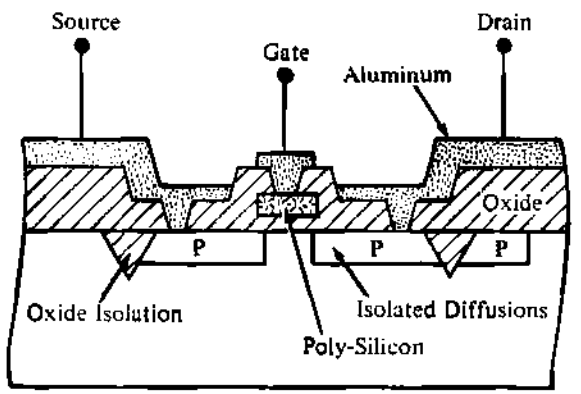
4.13 MOS Technology

Figure 4.13-8
MOS DYNAMIC RAM PERFORMANCE



Source: DATAQUEST, Inc.

Figure 4.13-9
ISOPLANAR SILICON GATE MOS



Source: DATAQUEST, Inc.

tial gains because of the smaller die size.

It remains to be seen how many manufacturers convert to this technique for the manufacture of MOS products. Thus far, three companies (Advanced Micro Devices, Fairchild, and National Semiconductor) are using this process in production of some of their silicon gate MOS circuits.

Ion Implantation

The basic ion implantation process is the same as described in the Bipolar Section. However, the primary applications differ substantially.

Threshold Adjustment

The voltage required to turn on an MOS transistor (threshold voltage) is an important parameter. In the metal gate processes, the use of <100> orientation silicon or silicon nitride dielectric layers under the gate electrode have been used to obtain lower threshold voltages. In silicon gate, the P-type doping of the polysilicon gate automatically lowers thresholds. However, in N-channel, silicon gate, the threshold problem arises again, but in this case it is too low.

The use of ion implantation resolves the threshold problem for all MOS technologies. Since the implantation can take place through thin layers of oxides without damaging them, a convenient time to use ion implantation is immediately after gate oxidation. A light dose of boron (P-type) into the channel of a PMOS device will lower its threshold. Similarly, a light dose of boron into the channel of an NMOS device raises its threshold. Since the concentration of dopant can be monitored accurately, this threshold adjustment is very precise and can easily tailor the threshold to any desired value.

Depletion-Mode Transistors

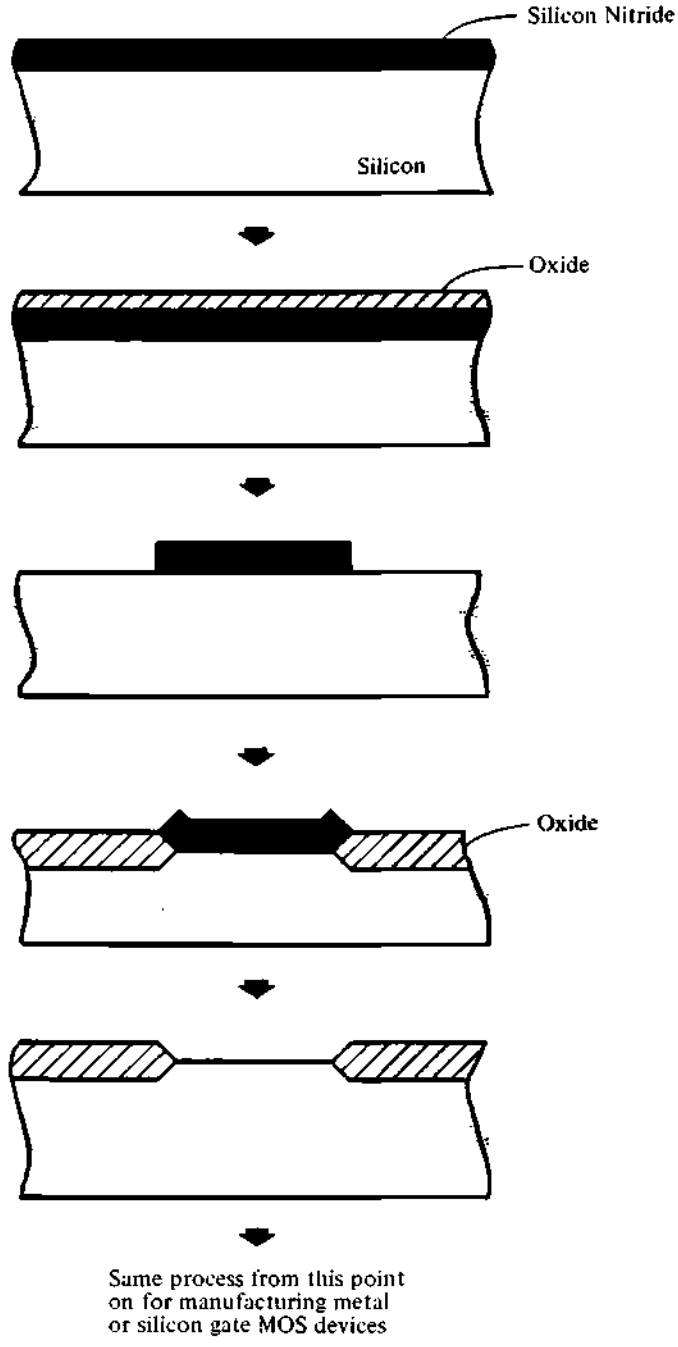
MOS ICs do not use many resistors, but they do use MOS transistors which are electrically operated in their resistive mode. The amount of this resistance can be altered and tailored by higher doping of the channel regions to create normally "on," or depletion-mode, transistors.

The wafer can be masked after the gate oxide is formed so that only certain gate oxide areas would be exposed to the ion beam. The uncovered gates could then be implanted to produce a circuit having both depletion and enhancement mode transistors on the same substrate.

This approach was first used by Mostek to build a metal gate, P-channel, 1K quasi-static RAM operating at speeds higher than standard metal gate products. This RAM is now rapidly being displaced by silicon gate, N-channel products.

Figure 4.13-10

ISOPLANAR PROCESS FOR MOS DEVICES



Source: DATAQUEST, Inc.

Isolation Implants

A controlled implant between the diffusions (masked by oxide) eliminates many of the parasitic effects that have an impact on MOS circuits. The implant, however, does not necessarily reduce parasitic capacitances nor increase circuit speed. The process is, nevertheless, desirable and used by many companies, since it avoids the need to deposit and etch layers of oxide and nitride used in oxide isolation processes.

Diffusions

Ion implantation is useful in one MOS diffusion process—forming the P well in CMOS circuits. The dopant concentration of this well is low (although higher than those used for isolation or threshold adjustment) and is difficult to control using standard diffusion techniques. Doping concentration is also critical, since it determines many of the critical NMOS device characteristics.

The integration of ion implanation into this part the CMOS process has been instrumental in increasing CMOS yields and simplifying the normally lengthy MOS process.

4.3 Charge Coupled Devices

Charge coupled devices (CCDs) were first introduced in 1970 by Willard Boyle of Bell Laboratories. He and his coworkers proposed that this type of device could readily be used for imaging and other applications. Three years later, circuits became commercially available for the first time. In this section we give a brief description of the operations, fabrication, and major applications of charge coupled devices.

DEVICE OPERATION

Figure 4.3-1 illustrates the cross section of a silicon-gate, two-phase, CCD device. A CCD device retains information by storing electronic charges in depletion"wells" created by the voltage on metal or polysilicon near the surface of the wafer. Information is moved by transferring the charge along much like an old time bucket brigade. If the metal or polysilicon has the proper voltage, the well will be created and will disappear when the voltage is removed. Although the well holds the charge, the charge must be introduced into it at the time it is formed. Charges can be introduced either by incident light, as in the case of imaging applications, or by an applied electrical signal.

In Figure 4.3-1a a charge is introduced by a P-type diffusion when it is at the proper voltage. If the P-type material is not at the proper voltage, charges will not be introduced and the well will remain empty. In Figure 4.3-1b the voltage phase is changed so that Phase 2 has a negative voltage and Phase 1 has a positive voltage. When this change occurs, the charge is transferred from the original well to a newly created adjacent one. In the next time period, as shown in Figure 4.3-1c, the voltage on the phase lines changes back to the original levels and the charge is again transferred. Since the P-diffusion no longer has a positive voltage, the first well (on the left) has no charge transferred to it.

In this manner information is moved serially through the CCD bits by alternately changing the magnitudes of the voltages applied to the phase electrodes. Because the amount of charge in a particular well can vary over an entire range and need not be in either one of two states, a CCD device can function as an analog memory; that is, the information stored in a well can be proportional to an input signal.

FABRICATION

As illustrated in Figure 4.3-1, there are no diffusions and no contacts to the substrate under the CCD storage and transfer elements. Consequently, yield losses typically associated with the diffusion process and with substrate contacts are eliminated in those critical areas. Both of these differences also allow the CCD to have a greater bit density than does standard MOS memory. The semiconductor processes used for CCD devices are basically the same as those described for standard N-channel silicon-gate devices in the Manufacturing Model (Chapter 3 of the Semiconductor Industry Service). The diffusions and substrate contacts used for standard N-channel devices are also necessary for CCD devices at the inputs and outputs of the device as well as for any electronic logic included on the device. Some CCD processing includes special ion implanation steps to increase performance.

CCD circuits can operate in many different ways, and each operation mode can affect fabrication in turn. Depending on the fabrication and type of operation, CCD devices can operate with three-phase or four-phase clocking as well as variations of the two-phase circuit described here.

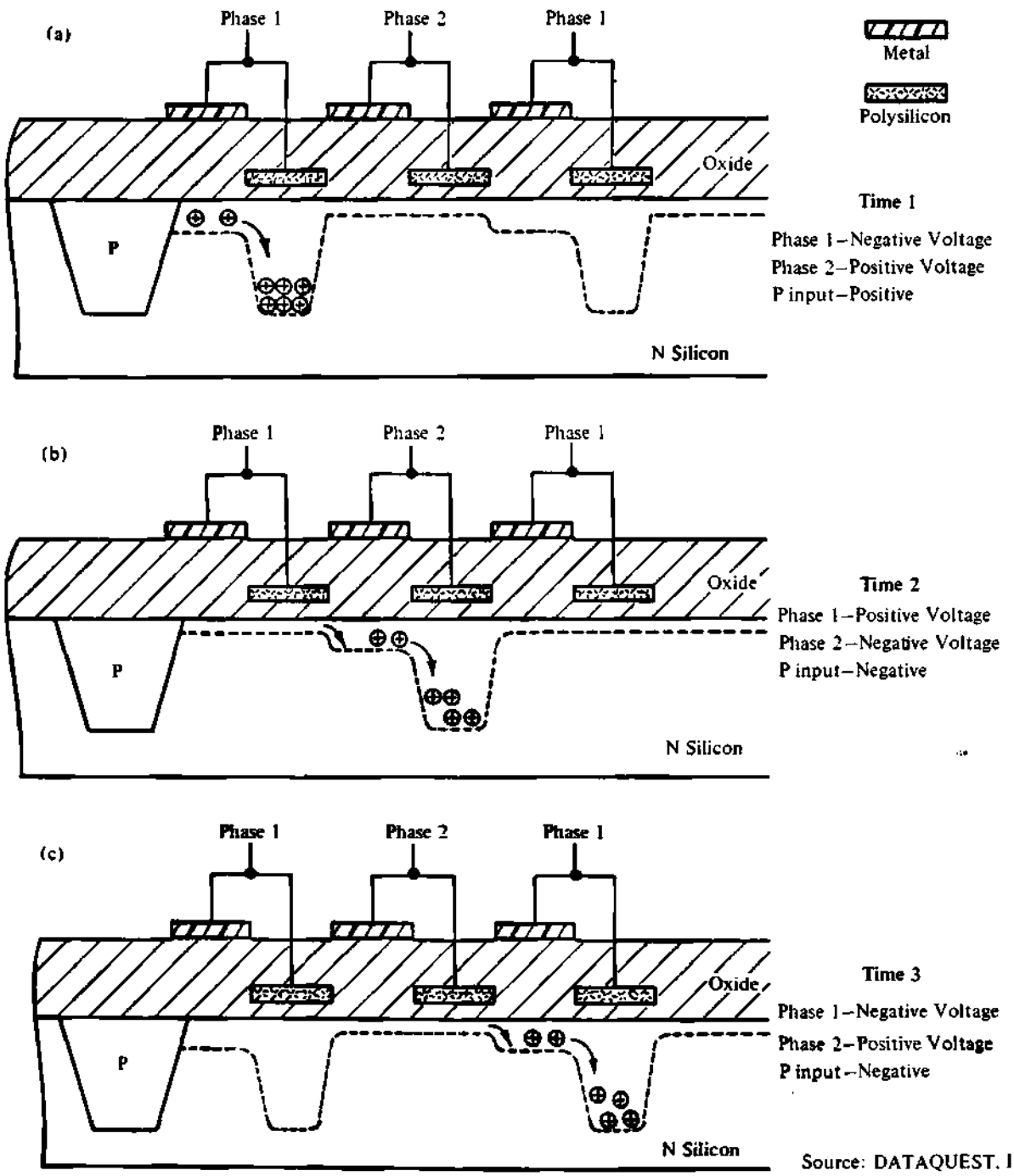
APPLICATIONS

There are four major potential applications

4.3 Charge Coupled Devices

Figure 4.3-1

CHARGE COUPLED DEVICE OPERATION



Source: DATAQUEST, Inc.

4.3 Charge Coupled Devices

for CCD devices:

- Imaging
- Memory
- Delay lines
- Filters

Imaging

In imaging applications, incident light is focused either on the front or back side of the CCD device. This incident light creates electrical charge wells within the silicon close to the electrodes. The amount of charge in a well is proportional to the amount of light. Different wells will have different amounts of charge according to the amount of light focused on them. On electrical command, the wells of charge can be shifted serially out of the CCD sensors. The information, for example, can be redisplayed on a video screen. The advantage of CCD devices over conventional TV cameras is that the bulk of image processing can be performed on a single silicon chip. This approach eliminates the need for an electron scanning beam, high voltages, and the associated circuitry required by conventional TV cameras to convert an optical image into an electrical signal. Moreover, the CCD chip is small, operates at high speed, has low power dissipation, and offers solid-state reliability. One drawback to the use of CCD devices as video sensors is their poor response to blue light, a characteristic of any silicon sensor. Thus color discrimination, for color video, is poor. On the other hand, CCD devices have exceptionally good sensitivity at very low light levels and can be fabricated to be sensitive to infrared light. These advantages make the CCD devices potentially applicable for many special uses such as military applications and security devices.

The impact of CCD on television at present is less certain because of still unresolved problems of resolution and picture quality. Technology is still insufficiently developed to economically produce devices of the complexity of commerical TV cameras. However, industrial quality CCD video cameras are now becoming available. Furthermore, Bell Labs has produced a CCD device capable of full Picturephone resolution. The success of these prototypes and future advancements in CCD technology will determine the impact of this technology on the video market.

Simpler CCD devices have also found use in other optical-sensing applications, such as optical readers. Such usage should become more prevalent in the near future.

Memory

As mentioned earlier, since there are no diffusions for contacts between or to any of the charge storage areas, the density of information storage can be very high for CCD memories. Moreover, the serial nature of the charge storage and shifting in CCD devices makes them adaptable to many serial memory applications, such as picture storage and recycling on CRTs and video screens. High density serial CCD memories can be applied also to some areas now serviced by magnetic disk and drums storage, where information density is important and speeds are only nominal. An example of this application is a CCD equivalent of an 8 million-bit drum memory currently being designed by RCA. Using an RCA designed 16K-bit CCD memory, this memory system would be 1/10 the size and 1/8 the weight of a conventional drum memory and operate four times faster using 1/60 of the power. This level of performance may cause many semiconductor companies to introduce CCD memory products although CCD devices are more expensive than drum or disc memories. CCD memories offer an additional place in the memory hierarchy between semiconductor RAMs and magnetic memory.

4.3 Charge Coupled Devices

Early in 1975, Fairchild and Intel both announced the development of CCD type memories. In small quantities, these memories are priced at between $0.005 per bit and $0.01 per bit. If volume increases along a reasonable curve, however, DATAQUEST expects that such CCD memories will sell for below $0.001 per bit by the beginning of 1976. In general, CCD memory is expected to cost about one-third to one-half the cost of standard semiconductor random access memories.

Delay Lines

One particular application of CCD devices that cannot be readily performed by other semiconductor devices is their use as signal delay lines. The delay can be varied according to the clock rate applied to the electrodes of the device and the number of bits used. An important attribute of these devices is that the delay can be used to accomodate either analog or digital signals. One potential application, for example, would be to correct delay errors in video recording and with video discs. Many applications for acoustical delay lines could be filled by CCD devices.

Filters

The delay line characteristics of CCD devices can also be adapted to make the device function as a filter for electronic signals. This characterstic has several potential applications. CCD devices can perform narrow bandwidth high Q filtering centered around a particular frequency, which is determined by the clock rate of the device. These filters are especially competitive technically at very low frequencies.

CCD filters can also be designed to filter nonsinusoidal signals. This attribute has potential applications in such areas as radar and sonar, although the current operational speeds of the devices are far too slow for radar.

4.5 Magnetic Bubble Devices

Magnetic Bubble Devices (MBDs) were discovered in 1967 by Bell Laboratories engineers who discovered that stable magnetic bubbles could be created, propagated, and detected for use in memory applications. In 1976, the first MBD memory chips became commercially available in sample quantities. In this section, we describe the device operation, fabrication, and major applications of magnetic bubble devices.

DEVICE OPERATION

Magnetic bubbles are mobile cylindrical magnetic domains that can be generated in a thin magnetic layer and moved around within that layer. Magnetic bubbles of 5-micron diameter became commercially available in late 1976 and offer storage densities in excess of 10^6 bits/inch^2. Magnetic materials capable of supporting 0.5-micron diameter bubbles are feasible in the laboratory and promise storage densities in excess of 10^8 bits/inch^2.

The material used to support magnetic bubbles is a thin garnet epitaxial film (a single crystal magnetic material) that has been grown on a non-magnetic substrate (gadolinium gallium garnet or GGG). In this single crystalline thin garnet film, magnetic domains exhibit a preferred axis of magnetization perpendicular to the film surface. In the absence of any external magnetic field, the thin film will break up into magnetic domains in which the magnetization is uniformly "up" or "down." The serpentine magnetic domains arrange themselves in such a way that the garnet film is magnetically neutral, with half of the serpentine domains pointing up and the other half pointing down (Figure 4.5-1a). If a small magnetic field is applied perpendicular to the film, the magnetic domains whose polarity is opposite to that of the applied field shrink (Figure 4.5-1b). As the applied magnetic field is further increased, the serpentine magnetic domains shrink into cylinders (Figure 4.5-1c) whose diameter depends upon the film thickness, the applied field, and certain material parameters. When viewed under a polarized light source, these magnetic cylinders can be seen and appear as bubbles. If the applied magnetic field is further increased, the opposing magnetic domains collapse entirely (Figure 4.5-1d).

If the applied bias field is reduced to a level where magnetic bubbles are stable, magnetic bubble domains can then be generated by passing current pulses through a "hairpin" conductor loop. The resulting bubbles appear in the garnet film under the loop and can be moved around inside the film. Bubble propagation is accomplished by using an overlay permalloy pattern, which determines the bubble propagation path, and an in-plane rotating magnetic field, which moves the bubbles. The rotating in-plane field is generated by a set of orthogonal coils that surround the bubble chip.

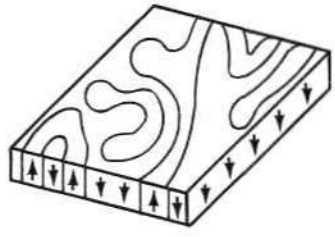
Figure 4.5-2 illustrates the details of magnetic bubble propagation. A common overlay pattern known as a "TI Bar pattern" is processed on the thin garnet film. It consists of magnetically soft permalloy material that polarizes along the in-plane field. Any bubbles under the permalloy overlay move to positions under the appropriate poles. Rotating the in-plane field causes the positioning magnetic poles to move across the TI Bar array, which carries the underlying bubbles along. (See the bubble movements in the successive rows of Figure 4.5-2.) Other overlay patterns that have been successfully demonstrated include the Y-bar, chevron, and contiguous disc. The overlay pattern requires no conductors in the central area of the bubble chip. The only conductors required are for generation, detection, replication, and transfer of bubbles, and these are positioned along the edges of the bubble chip.

The preferred architecture for MBD chips is the major/minor loop shown in Figure 4.5-3. This architecture consists of one major loop

4.5 Magnetic Bubble Devices

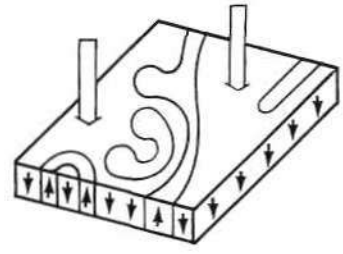
Figure 4.5-1

MAGNETIC DOMAINS
IN A THIN GARNET FILM



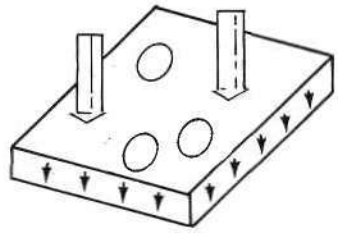
a

Serpentine magnetic domains under no external field. Half of the domains are pointed up and half are pointed down.



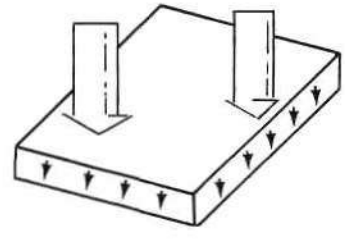
b

Serpentine magnetic domains under applied magnetic field. More than half of domains are oriented with external field.



c

Opposing magnetic domains shrink to cylinders as applied magnetic field increases.



d

Opposing magnetic domains disappear as applied magnetic field is further increased.

Source: DATAQUEST, Inc.

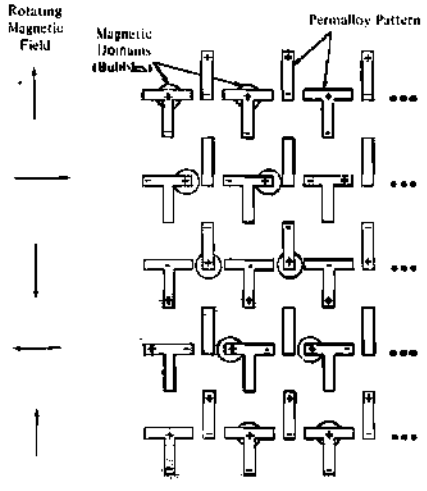
and multiple minor loops. An incoming stream of 1s and 0s is converted by the bubble generator into a serial stream of bubbles and no bubbles. As bubbles are generated in the major loop, they are shifted around the loop until a block of data lines up with the minor loops. Under external control, the transfer gate enables the transfer of bubbles between the major and minor loops. This process can continue until all the bubble positions in the minor loops are filled. To read the bubble memory contents, an entire block (one bit from each minor loop) is transferred to the major loop. Actually, a copy of each bit is transferred to the major loop and the original bit is left behind in the minor loop to preserve the memory contents. The bubbles in the major loop are then propagated around the loop and detected.

The advantage of the major/minor loop architecture is that every bit location in the minor loops does not have to be perfect. Some level of defects can be tolerated. By accepting

4.5 Magnetic Bubble Devices

Figure 4.5-2

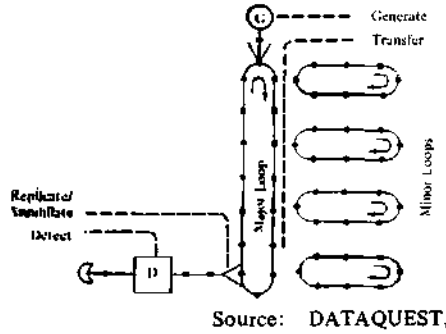
TI-BAR PROPAGATION TECHNIQUE



Source: DATAQUEST, Inc.

Figure 4.5-3

MAJOR-MINOR LOOP ARCHITECTURE FOR MAGNETIC BUBBLES



Source: DATAQUEST, Inc.

all chips that have no more than say 8 percent of the minor loops defective, a higher yield and lower cost can be achieved. The defective loops are noted during testing and are omitted from the address list of good minor loops. Another bubble chip architecture is the serial register that uses one long serial register to store the data. This architecture is not as popular as the major/minor loop structure because it has an inherently lower yield for the same memory capacity.

Since magnetic bubbles are not TTL-compatible, special interface circuits must be used. The interface circuits actually serve two purposes. First, they provide a TTL 8-bit parallel interface which is ideal for minicomputer and microcomputer applications. Second, they format the parallel data into a serial stream for input to the MBD package, and they provide the precise timing and control necessary to operate the magnetic bubble memory.

Texas Instruments is developing a set of interface chips for use with its 92-kilobit package. There are eight different interface chips; six of these chips must accompany each 92-kilobit bubble package to create a 92-kilobit bubble chip set. These six interface chips provide temperature compensation and precise currents for bubble generation and transfer, provide the rotating external drive field, provide return current paths for collapsing fields, provide detector bias, and detect the presence of bubbles. The other two interface chips can serve up to nine 92-kilobit bubble chip sets. They provide precise timing and master control for the above interface circuits. The interface chips and 92-kilobit bubble chip are packaged in dual in-line packages whose pin counts range from 8 to 16. The 92-kilobit bubble package is a 14-pin package, which measures 1 inch by 1.2 inches by 0.4 inches and weighs 20 grams. The 92-kilobit bubble chip set dissipates 1.9 watts during read and write cycles and 0.9 watts during standby.

FABRICATION

The manufacture of magnetic bubble devices involves fewer and simpler manufacturing

4.5 Magnetic Bubble Devices

steps than required for bipolar or MOS integrated circuits. Most magnetic bubble chip designs require only two mask levels—one for the permalloy propagation pattern and one for the conductor pattern. This is simpler than a typical CCD design, which requires as many as eight mask levels and very careful mask alignment.

The processing of MBDs and CCDs differs in the crystal pulling, in the front end of the wafer fabrication, in testing, and in packaging. The pulling of GGG crystals is a difficult and new process compared to the well-established silicon crystal-pulling technology. Once the crystal has been sliced and the wafers have been polished, an epitaxial layer is grown on the wafer. This garnet epitaxial layer is the thin magnetic film in which the magnetic domains shape the stubby cylinders known as magnetic bubbles. Pulling the crystals and growing the epitaxial film are two of the most difficult and exacting processes in fabricating magnetic bubbles. The remainder of the processing uses standard photolithography imaging and processing. Testing the complex bubble chips will be one of the major challenges in their manufacture. Furthermore, packaging them between bias magnets and crossed coils is a difficult task. Single magnetic bubble chips are currently being packaged with bias magnets and crossed coils in a 14-pin dual in-line package.

Manufacturing yields for MBDs are expected to be sufficiently high to produce cost-effective MBD memories. One factor leading to good yields is that the major/minor loop architecture of Figure 4.5-3 can tolerate some defective minor loops. By identifying the defective minor loops and programming the controller to use only good loops, partially defective chips can be used, thereby increasing the effective manufacturing yield. This technique is employed in the 92K MBD manufactured by Texas Instruments.

APPLICATIONS

There are two potential applications for MBDs:

- Memory
- Display

Memory

Memory is the primary application for MBDs. Commercially available 5-micron diameter bubbles achieve bit densities of greater than 10^6 bits/inch^2, and 0.5-micron diameter bubbles feasible in the laboratory promise densities in excess of 10^8 bits/inch^2. These high densities and their expected high reliability make bubbles attractive for many memory applications.

MBDs should find their largest market in mass storage systems where high density and low cost are generally more important than speed. MBDs are expected to displace some fixed- and moving-head discs as well as floppy discs and cassetes. Typical applications include one-half to 20-megabit storage systems for minicomputers.

Secondary markets for MBDs should be an array of other applications, including microcomputer systems, military systems, terminals, programmable calculators, entertainment systems, and automotive systems. In some of these applications—especially military systems and portable terminals—the non-volatility of MBDs will play an important role.

Display

Magnetic bubbles can be seen when illuminated by polarized light. By creating linear segments from a row of dots (bubbles) and using the line segments to generate numeric and alphanumeric characters, a magnetic bubble display becomes possible. MBDs offer the advantages of non-volatility, good color contrast,

4.5 Magnetic Bubble Devices

and low drive voltages in a flat electronic display. Feasibility of such a display has been demonstrated, but economic viability has not yet been demonstrated.

4.10 Semiconductor Materials and Physics

This section discusses the materials used in the semiconductor industry and the importance of single crystal material to the basic conduction mechanisms. The discussion includes the types of impurity dopants and doping techniques and the various types of surface coatings used in device and circuit manufacturing. It should be noted that a primary feature in reducing the cost of semiconductor processing has been the availability of larger diameter silicon wafers. Wafer fabrication is discussed in a subsection on crystal preparation.

MATERIALS

Semiconductors fall midway between conductors and insulators in their ability to conduct electrical current. Electrical current is facilitated in solids because electrons are able to move freely under the influence of an electrical potential. Conductors are characterized by a large number of electrons in the conduction band with many free electronic energy states available to allow the electrons free movement. Insulators have few available free energy states in the valence band so that the electrons are tightly bound and cannot move.

The material used to fabricate semiconductors is more like an insulator than a conductor, but it can have a few valence electrons that move freely. An additional conduction mechanism that is important in semiconductor electronics is that created by a missing electron. This state is called a hole and is created through impurities in the material. These conduction mechanisms result from the basic crystalline qualities of the semiconductor elements.

CRYSTALLINE SEMICONDUCTORS

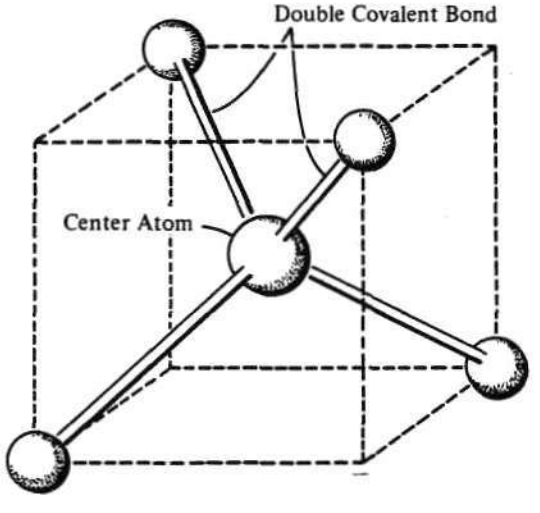
There are many different semiconductor materials. Germanium and silicon are the most common and have the same crystalline structure as diamonds. In the diamond crystalline structure, each atom is symmetrically surrounded by four other atoms. These atoms are situated as if they were in the alternate corners of a cube as shown in Figure 4.10.1. This arrangement has the interesting geometrical property that it is the only way in which four balls can be placed around a fifth so that they are in completely equivalent positions with respect to each other.

This structure arises from the nature of the chemical forces that exist between the atoms. The atoms in most substances are held together largely by electron-pair bonds resulting from the sharing of electrons between atoms. These electron pairs constitute the so-called covalent bonds.

Carbon, silicon, and germanium atoms all have in common the characteristic of four valence electrons which form sets of four bonds with their four neighbors. In a perfect crystal, each covalent bond contains two electrons as shown in Figure 4.10-2. Consequently, every

Figure 4.10-1

SILICON CRYSTAL STRUCTURE



Source: DATAQUEST, Inc.

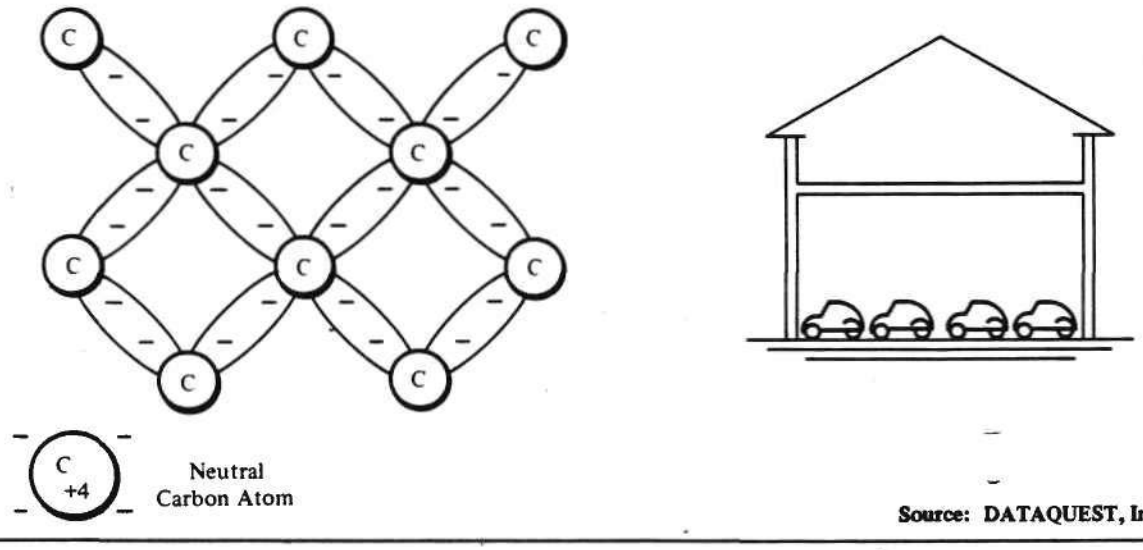
electron is tightly bound and thus unable to enter into the process of electric conduction. This situation may be represented by the analogy of an automobile storage garage, where one floor is completely filled with automobiles so that no flow of traffic is possible.

Conductivity can be produced in crystals of this type in a number of ways, all of which entail destroying the perfection of the covalent bond structure. Toward this end, various types of imperfections can be introduced into a semiconductor. For example, an electronic disturbance can be produced in silicon (Figure 4.10-3) by a light photon. The light photon delivers its energy to an electron, which is then ejected from one of the bonds. The ejected electron constitutes a localized negative charge in the crystal since, before it arrived at its new destination in the crystal, the electron-pair bond structure was electrically neutral. Such an electron represents an excess over and above the number of electrons required to complete the bond structure in its neighborhood. It can move around much like an electron in a metal, since it has been put into a state of higher energy levels, called "the conduction band." Its behavior is represented in our garage analogy by the vehicle on the second floor in Figure 4.10-3 which is now free to move. This process of conduction by excess electrons is referred to simply as conduction by "electrons."

In the automobile analogy, the vacant space now permits traffic to flow on the first floor. A similar conduction process takes place in the crystal through the motion of the "hole" left in the bond when the electron was ejected. This hole constitutes a net, localized, positive charge in the crystal since before it was created that part of the crystal was electrically neutral. Holes move about as easily in semiconductors as do electrons.

Figure 4.10-2

ELECTRON-PAIR BONDS IN A DIAMOND-TYPE CRYSTAL

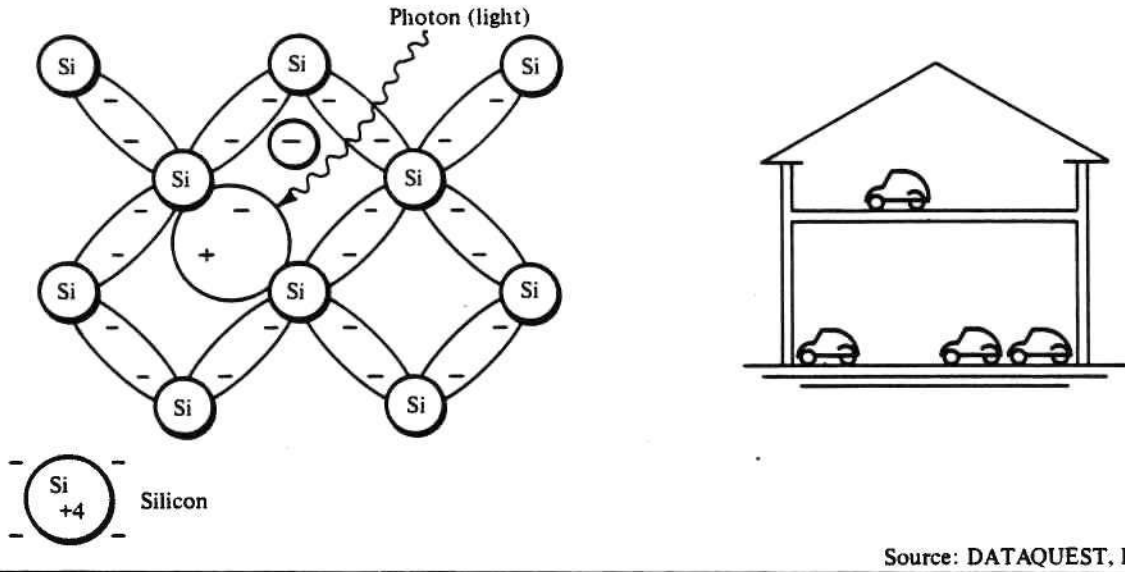


Source: DATAQUEST, Inc.

4.10 Semiconductor Materials and Physics

Figure 4.10-3

INTRINSIC SILICON WITH A FREE ELECTRON AND HOLE PRODUCED BY LIGHT



Source: DATAQUEST, Inc.

SEMICONDUCTOR MATERIALS

The primary semiconductor materials employed today are silicon and germanium, which are elemental semiconductors. Other chemical elements having the same chemical valence, such as carbon and tin, exhibit similar properties, but these elements do not include the desirable physical properties for semiconductor device fabrication.

Certain compounds of materials also exhibit semiconducting properties. One family of such compounds combines elements having three valence electrons (such as gallium) with elements having five valence electrons (such as arsenic). Other gallium compounds in addition to gallium arsenide have also been extensively explored, including gallium phosphide, gallium antimonide, and combinations of three elements, such as gallium arsenide phosphide. Other semiconductor materials include indium antimonide, indium arsenide, silicon carbide, and cadmium sulphide.

Another type of semiconductor material results from the ionic bonding of particular types of molecules. Semiconductors produced by this means are known as ionic semiconductors. Examples of this type of material are lead salts such as lead selenide and lead tellenide.

The use of a semiconductor material for a particular device depends on its physical characteristics, workability, and availability. Early transistors and diodes were made from germanium because devices could be more easily fabricated from this material as compared with silicon. As the industry developed, however, the basic physical advantages of silicon devices led to overcoming the difficulties in fabrication. Thus, silicon is now used predominantly because of its ease of fabrication, reliability, and general availability within high purity. Germanium, on the other hand, is slowly being phased out. Extensive work has been done with gallium arsenide as a material that has ex-

tremely desirable properties for devices. However, basic fabrication problems have relegated gallium arsenide to use only in cases, such as for light emitting devices, where another material would not be as effective. Gallium arsenide is also used extensively for microwave frequency devices because of the high mobility of its electrons. Indium antimonide is being explored for high frequency devices. Cadmium sulphide and the ionic semiconductors are used primarily as photoconductors. Other semiconducting compounds are continuously being explored and will become important as their properties are understood and fabrication problems are overcome.

Theoretically, faster device performance should be available with germanium and gallium arsenide, as well as other compounds, as compared with silicon. But ingenious developments in device design and geometry (such as planar technology) have led to silicon's domination throughout most of the history of the semiconductor industry. It appears that this domination will continue throughout the 1970s, unless some unforeseen technological breakthrough occurs.

TECHNIQUES OF CRYSTAL PREPARATION

Probably the most important scientific development in the semiconductor field following the invention of the transistor was the development of high-quality single crystals. Early work on the growth of these crystals provided a sound basis for later material developments for discrete transistors and diodes, more advanced hybrid and monolithic integrated circuits, and other devices, such as light-emitting diodes, tunnel diodes, and solid-state lasers.

The various techniquies for producing crystals for semiconductor fabrication are discussed below.

Czochralski Crystals

Most of the silicon crystals produced in the world today are grown by the method developed by Czochralski in 1916, who never envisioned the fantastic growth and almost universal application of his technique to the growth of silicon crystals that occurred nearly a half-century later. His interest was in measuring the solidification rates of lead, tin, and zinc. Many features of his original experiment are being rediscovered daily in crystal-pulling systems.

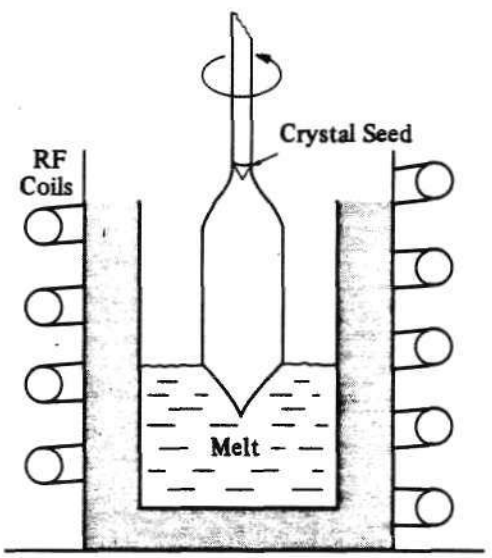
The method—shown in Figure 4.10-4—consists of pulling the solid single crystal material from a molten solution of the desired material. It was first applied to the growth of germanium about 1950 and was improved in 1965 to enable the growth of dislocation-free crystals of up to two inches in diameter. Most crystals grown today are prepared by the Czochralski method.

With the advent of monolithic integrated circuit technology, the Czochralski method has become more widely used mainly because:

- Large diameter crystals are needed for larger wafers
- Lower cost of the processes
- More uniform resistivity in a doped crystal
- High-quality material with a minimum of defects

More stringent crystal quality requirements are being imposed upon material suppliers. Smaller device dimensions are causing microscopic crystal defects to become more critical with respect to the yield, performance, and reliability of semiconductor devices.

Figure 4.10-4
CZOCHRALSKI
CRYSTAL PULLING FURNACE



Source: DATAQUEST, Inc.

Float Zone Crystals

A second technique in preparing large single crystal material is termed "float zone." In this technique, a floating liquid zone is produced through the use of selective heating such as by radio frequency (RF) induction techniques. As the floating liquid zone is passed along the material, the impurities tend to remain in the liquid zone. Under proper conditions, the material solidifies into single crystal material as the liquid zone is passed through it. The float zone method is used primarily for producing silicon crystals with low oxygen impurity concentrations, when low dislocation concentrations and exceptionally large diameters are not required.

Epitaxial Crystal Growth

An important development in crystal growing technology occurred in 1960 when the epitaxial process of producing single crystal material was developed. The word epitaxial is derived from two Greek words: epi, meaning upon, and taxis, meaning arranged. This process consists of depositing a thin layer of silicon, of the same crystalline orientation as the substrate, onto the surface of a bulk silicon wafer. The resultant "epi" layer serves as an extension of the original wafer, but may be of opposite dopant polarity and different dopant concentration.

The epi layer is generally deposited onto the bare silicon wafer by condensation from a gaseous source in a chamber heated by RF or infrared sources. During the deposition process, a controlled amount of gaseous impurity is introduced into the system to produce the proper impurity concentration in the epi layer.

In recent years much of the development work in the area of epitaxial layer growth has been directed toward achieving improved film perfection. Techniques for growing epi layers at lower temperatures are also under development and will be important in achieving precise doping profiles. Additional work has been directed toward achieving silicon epitaxial films on insulating substrates such as sapphire or spinel. These materials have crystalline structures of the appropriate geometry to allow single crystal silicon to form on their crystalline axis structures.

In recent years, a great deal of effort has been directed toward achieving automation in the growth of epitaxial layers. Developments in this area are directed toward (1) controlling thickness, resistivity, and profiles, particularly for thin layers and (2) developing silicon films on insulating substrates.

4.10 Semiconductor Materials and Physics

Trends In Crystal Material Preparation

Progress in the semiconductor industry has depended largely on progress in the technology of single crystal preparation. Technological progress in this field has resulted in improved crystal perfection and crystals of larger diameter. It is clear that with the batch processing philosophy of the semiconductor industry the incorporation of large semiconductor wafers in the process will yield economies of scale. Figure 4.10-5 indicates the increasing diameter of silicon crystals used over time and projects the use of four-inch diameter wafers in the 1976-77 time frame. Although silicon crystals of larger than four inches in diameter were grown as early as the 1950s, they were not of adequate quality for semiconductor processing.

Doping and Dopants

Donors and Acceptors

In addition to introducing conduction electrons and holes into crystal using light, they can also be introduced chemically by substituting a phosphorus atom for a silicon atom as shown in Figure 4.10-6. The phosphorus atom uses four of its five valence electrons to make four covalent bonds. Its fifth electron is free to wander, giving the crystal a conductivity by negative carriers. This type of conduction is called "N-type conduction," the crystal is called "N-type material," and the phosphorus impurity is called a "donor-type" impurity. Similarly, an impurity element with three valence electrons such as boron, can be substituted for a silicon atom in the crystal structure as shown in Figure 4.10-7. It does not have sufficient electrons to form the four covalent bonds. Consequently, a "hole" is formed that is free to move through the the crystal, giving it a conductivity by positive carriers. This type of conduction is called "P-type conduction;" the crystal is called "P-type material," and the impurity is called an "acceptor-type" impurity.

In the semiconductor industry, a material that is highly doped with an acceptor-type impurity is often called a "P±-type" material. Similarly, a material that has a high concentration of donors is called a "N±-type" material. For most purposes, these materials can be thought of as conductors rather than as semiconductors.

In the chemical periodic table of elements, semiconductors fall in the Group IV column, acceptors fall in Group III column; and donors fall in the Group V column. Table 4.10-1 lists several of the donors and acceptors commonly used in the fabrication of silicon and germanium semiconductor devices.

Doping Techniques

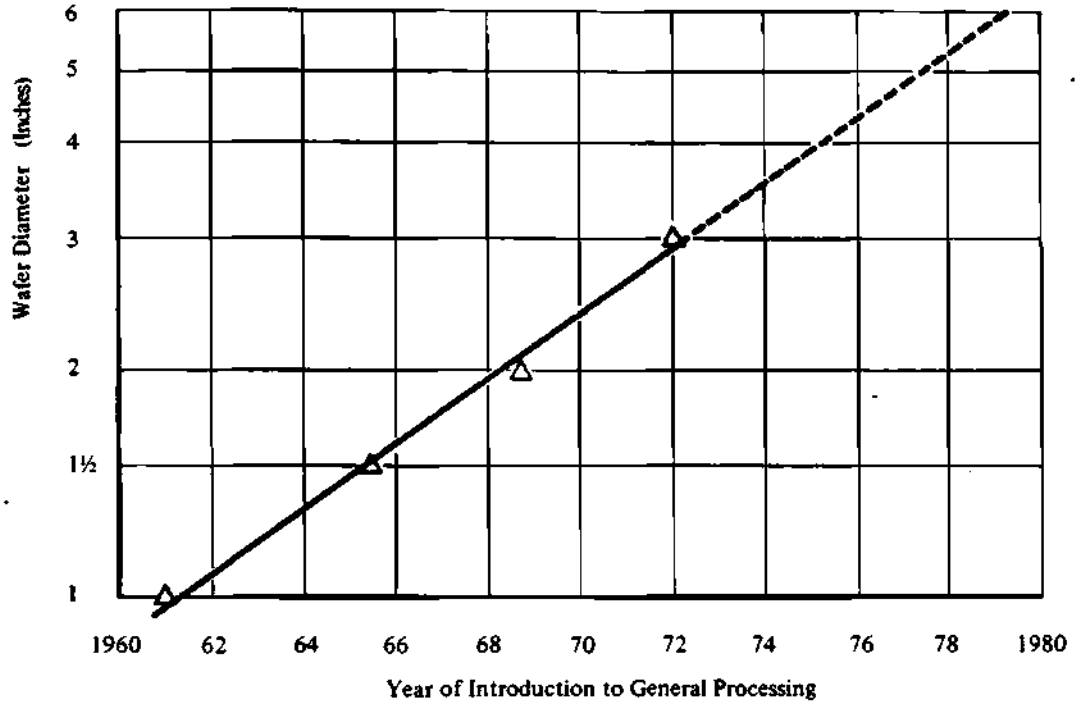
If there is an abrupt change in doping type in a crystalline semiconductor—for instance, from a donor type (or N-type) material to an acceptor (or P-type) material, the resultant transition is called a junction. The electrical behavior of a PN junction is the foundation of semiconductor electronics. A diode can be formed with one junction, and a transistor with two. The fabrication of semiconductor devices consists of selectively placing the proper dopants in the required positions of the semiconductor crystal. The high degree of sophistication in the placement of dopant material is one of the foundations of increasingly sophisticated semiconductor processing.

Grown-Junction

Early in the history of semiconductor fabrication, transistor and diode junction devices were formed by two techniques. The first technique is known as the grown-junction technique and consists of a compositional structure

Figure 4.10-5

SILICON WAFER DIAMETERS USED IN SEMICONDUCTOR PROCESSING



Source: DATAQUEST, Inc.

formed as the crystal is grown from a melt containing one type of dopant. If the dopant is arsenic, then the junction becomes N-type. It is very difficult to remove the arsenic from the melt, but if enough gallium, which is an acceptor, is added part way through the growth to more than compensate for the arsenic, a PN junction is obtained. The crystal is then sliced around the junction and sawed into a number of small slivers which are attached to a package so that a diode can be used. Transistors may also be formed in this manner.

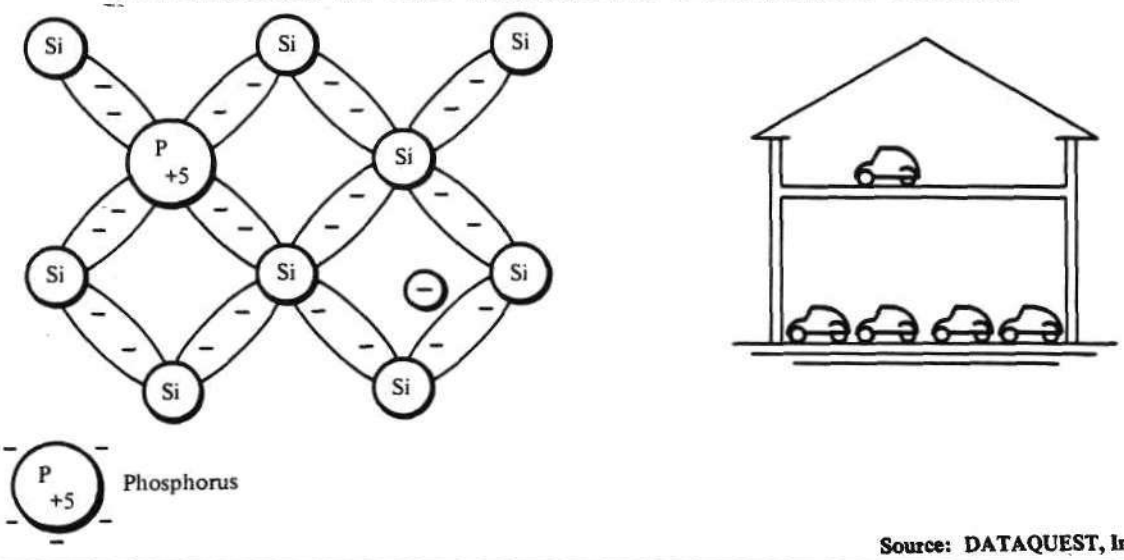
Alloy-Junction

A second early type of transistor is the alloy-junction transistor. In this type of construction, a crystal with the proper impurity concentration is pulled from the melt and subsequently sliced into thin walfer-like slabs. The wafer is then cut into small squares, called dice. Each die (plural dice) is then run through an elevated temperature chamber with a small pellet of the opposite impurity which is alloyed into the thin die. After the first alloy, the assembly is turned and the process repeated for the second junction.

These two techniques of transistor fabrication resulted in devices that were crude by today's standards. Their frequency response, current or power capabilities, and breakdown voltages were low.

Figure 4.10-6

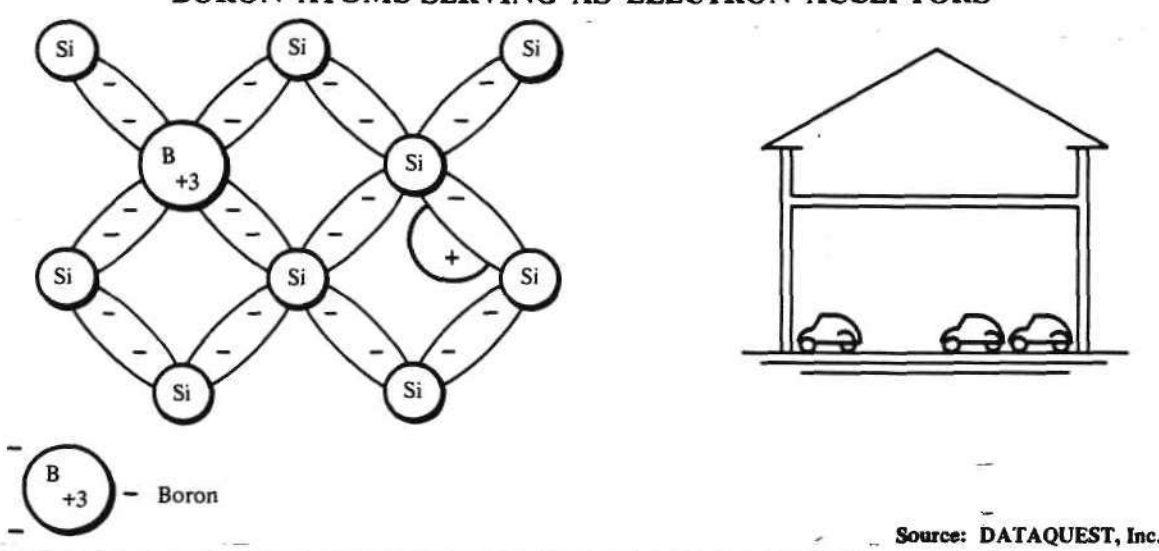
N-TYPE SILICON: ELECTRONIC CONDUCTION DUE TO PHOSPHORUS ATOMS SERVING AS ELECTRONIC DONORS



Source: DATAQUEST, Inc.

Figure 4.10-7

P-TYPE SILICON: ELECTRONIC CONDUCTION DUE TO BORON ATOMS SERVING AS ELECTRON ACCEPTORS



Source: DATAQUEST, Inc.

Table 4.10-1
TYPICAL DOPANT ELEMENTS FOR SEMICONDUCTOR MATERIALS

Element	Chemical Symbol	General Use
Donors (N-Type)		
Phosphorus	P	Emitter doping
Arsenic	As	Collector or Emitter doping
Antimony	Sb	Substrate or Collector doping
Acceptors (P-Type)		
Boron	B	Base or Substrate doping
Aluminum	Al	Contacts or Emitters on PNP
Gallium	Ga	Substrate or Base doping
Indium	In	Emitters or Collectors on Ge PNP

Source: DATAQUEST, Inc.

Diffused Junction

In the middle to late 1950s, it was recognized that thermal diffusion offered an improved technique for the placement of semiconductor impurity atoms. Thermal diffusion takes place when a high concentration of the impurity is placed at the surface of the semiconductor. Thermal diffusion is analogous to the effect of injecting a small amount of dye at the top of a glass of clear liquid. Over a period of time the liquid in the glass becomes colored by the dye. So that the impurities may move with reasonable speed through the semiconductor crystal, the material must be elevated in temperature to about 1,000° centigrade (or about 2,000° Fahrenheit). When the material is returned to room temperature, the impurities no longer move with sufficient velocity to alter their geometrical placement in the crystal structure. This approach may be thought of as quick-freezing the liquid shortly after the dye is injected so that the color pattern remains fixed in the solid material.

One important factor about thermal diffusion is that some dopant materials have a lower diffusion constant in the oxides of silicon than they do in silicon itself. Thus, silicon dioxide can act as a masking agent so that the impurities are selectively diffused over the surface of the wafer. This selective masking of the impurity diffusants is the primary technique used in the fabrication of silicon semiconductor devices and integrated circuits today.

Ion Implantation

A fourth doping technique is known ion implantation. Ion implantation allows precise quantities of ionized, isotropically pure dopants to be injected at high electrical energies into the semiconductor crystal held at low temperatures. This technique is analogous to having the dopant "bullets" shot from the ion implanter

"gun" into the silicon "target." After implantation, annealing at a moderate temperature is often used to remove crystal lattice damage and allow the dopant to achieve its desired depth into the crystal. The main advantage of ion implantation is the preciseness of the junction depth control that can be obtained while holding the silicon crystal at low temperatures. Masking can be achieved through the use of oxide, metal, or photoresist coatings, which are defined on the wafer. Although ion implanation as a doping technique was discovered in the late 1950s, it has only recently been employed as a production process.

In the past five years, several companies have supplied "ion implanters" to the semiconductor industry. These machines offer automatic, precise control of the doping profiles. The precise control of implantation has many advantages over diffusion as a source of dopant impurities, and many integrated circuits now employ ion implanation at some point in the process. A more detailed discussion of ion implantation is found in Section 4.4.

OPERATION OF DISCRETE DEVICES

In this section, the basic operations of the fundamental semiconductor devices—the PN junction and the transistor—are described. A brief picture of the operation of these devices should assist the reader to understand why there are such a large number of these devices.

PN Junction

The PN junction is the basic semiconductor device. In a PN junction the P-type region is populated by holes and the N-type region by electrons. The PN junction can be a light emitter, a solar cell, and also a rectifier or diode.

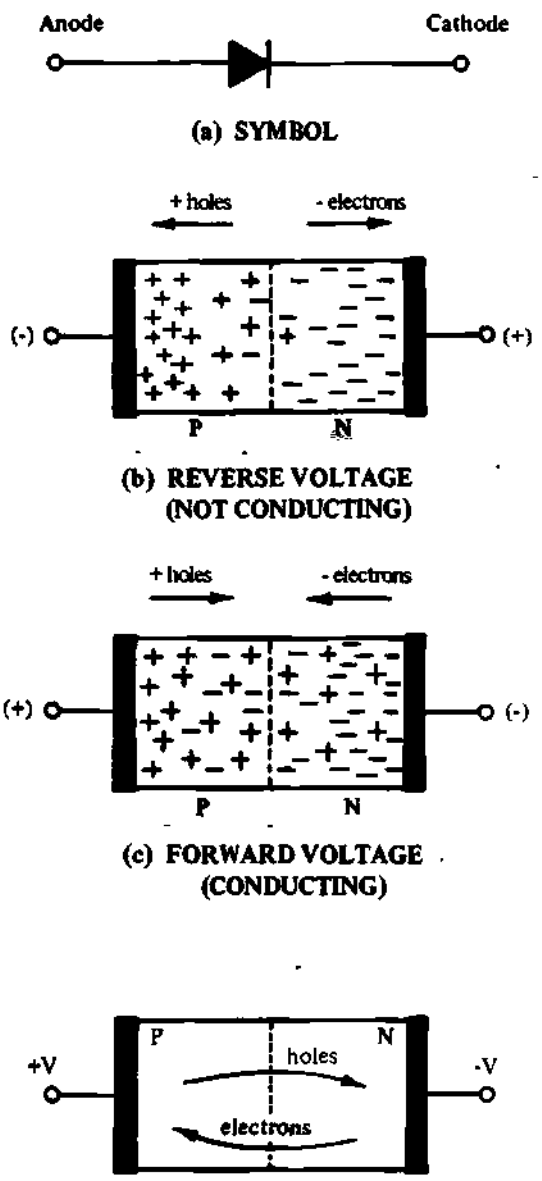
Such a junction is shown in Figure 4.10-8b with the P-type region negatively biased with respected to the N-type region. The holes (+'s) are attracted toward the negative side and the electrons (-'s) toward the positive side. Both types of carriers are pulled away from the junction. Donors and acceptors near the junction are ionized, setting up an electric field. This produces a voltage drop across the junction. Because the carriers are being pulled away from each other very little electric current flows across the junction.

If the polarity of the voltage is changed, as shown in Figure 4.10-8C, the electrons and holes are effectively pushed toward each other by the electrical field. They recombine (one hole neutralizing one electron). This requires more electrons and holes to go to the center (to balance the electrical field) and the device carries a current. It is evident from this type of action that a PN junction conducts current in one direction and thus can be used as a rectifier. Appreciably more current flows with a forward voltage bias (when the holes and electrons are pushed toward one another) than in the reverse bias state. Thus, if an alternating (AC) voltage is applied across the PN junction direct current (DC) flows in the forward direction but not in the reverse. By a suitable design of the area of the junction, such rectification can take place at microwave frequencies.

When the PN junction is reverse biased, the carriers are pulled away from the junction and the "empty" junction acts as a capacitor. By varying the reverse voltage, the carriers move farther from or closer to the junction, thus varying the thickness and hence the capacitance. This voltage sensitive capacitance is used for such applications as voltage tuning of the resonant circuits for TV tuners, voltage tuned oscillators, and other applications requiring an electronically variable capacitance.

When the reverse voltage is sufficiently large that the material can no longer withstand the electric potential, the junction is said to break down. This breakdown voltage can be controlled by the number of acceptors and do-

Figure 4.10-8
A PN JUNCTION



Source: DATAQUEST, Inc.

nors on either side of the junction and the device geometry (i.e., its area and junction shape). PN junctions designed in this manner can be used as voltage references.

Junction Transistor

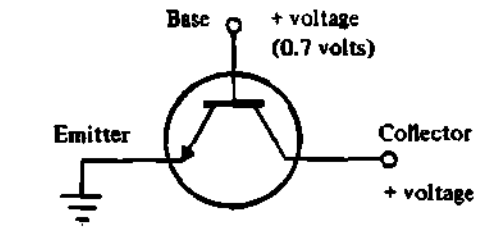
By adding a second junction to our device, as shown in Figure 4.10-9, we can create a transistor. The NPN transistor is a structure having three regions—N, P, and N. Originally, the structures were prepared by first doping a melt with one impurity, then compensating it with the opposite type of impurity, and finally overcompensating with the original type. The structures are now generally built using crystal preparation and diffusion techniques as outlined earlier in this section.

If voltage is applied to the NPN structure as shown in Figure 4.10-9, the function on the right is reverse bias while the junction on the left is forward biased. The reverse biased junction on the right is termed the "collector"; the forward biased junction on the left is termed the "emitter;" the region in the center is the "base." The carriers on the forward biased side of the transistor are pushed toward one another as described earlier for the PN junction. The negative carriers—electrons—are pushed from the emitter into the base where they are attracted by the positive voltage of the collector. Thus, the current can flow from the emitter to the collector.

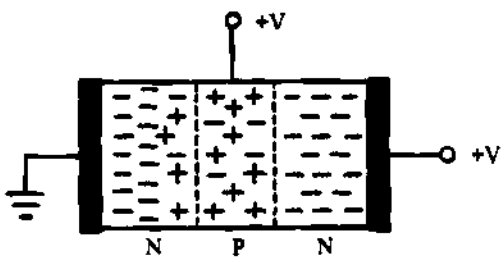
Under suitable dimensions, impurity doping levels, and bias voltages, much more current will flow to the collector than to the base. By varying the forward bias applied to the transistor base, the amount of current flow from emitter to collector can be controlled. Thus, a small current in the base controls a much larger current to the collector. The transistor is then an amplifier.

If the voltage applied to the emitter-base junction is zero or reverse biased, then no cur-

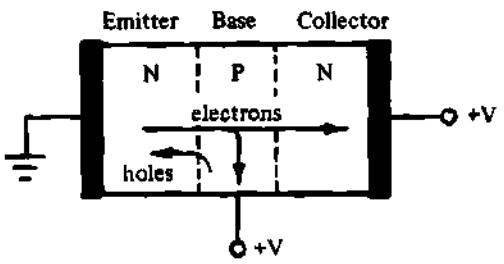
Figure 4.10-9
A NPN JUNCTION TRANSISTOR



(a) SYMBOL



(b) CHARGE CARRIER DISTRIBUTION



(c) ELECTRON FLOW

Source: DATAQUEST, Inc.

rent can flow in either junction and the transistor can be said to be "Off." When the emitter-base voltage is high, a large current flows and the transistor is said to be "On." When used in this manner, the transistor can act as a switch, changing the current from a small, negligible value to one that is fairly large.

The operation of a PNP transistor is essentially the same as that of an NPN transistor except that the types of junctions constructed are the opposite and the voltages used are reversed. The choice of which type of transistor to use depends on the particular circuit under construction and the properties of the particular types of transistors available.

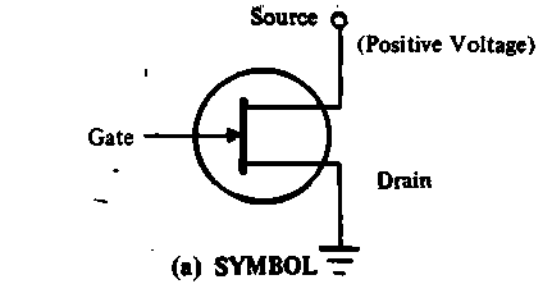
Field Effect Transistor

Figure 4.10-10 diagramatically shows a junction field effect transistor. If the two terminals called gates are left unbiased, the current will flow between the terminals called source and drain much as current flows in a resistor. When negative bias is applied to the gate terminals, the carriers are pushed away from the junctions, constricting the cross sectional area available for current flow and raising the resistance between source and drain. When the reverse bias becomes sufficiently large, the region where the carriers are pushed away from the junctions can touch and the area is termed "depleted." This touching action drops the current flow between the source and drain to a very low value.

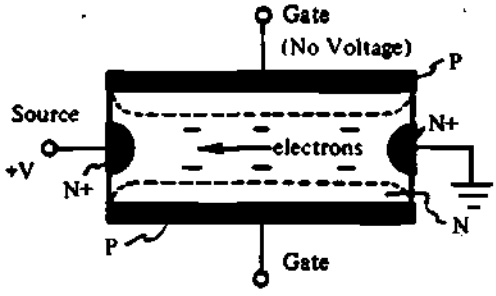
If the junctions creating the two gates are replaced by a metal electrode which is separated by an oxide from the silicon, the basic action of the device remains the same. The metal-oxide-silicon type devices are known as an MOS field effect transistors.

The major advantage of field effect transistors is that the gate electrode is reverse biased with respect to the source and drain electrodes. Very little current flows to the gate electrode,

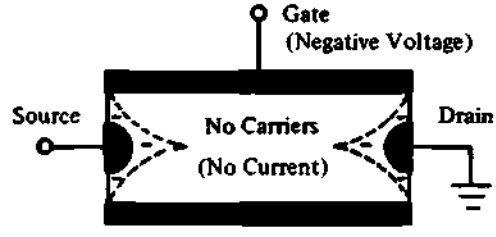
Figure 4.10-10
A JUNCTION FIELD EFFECT TRANSISTOR



(a) SYMBOL



(b) TRANSISTOR ON



(c) TRANSISTOR OFF

Source: DATAQUEST, Inc.

and hence very little power is required to control the source-to-drain current. As in the junction transistor, the field effect device can act as an amplifier or as a switch.

Bipolar and MOS Technologies

The junction transistor has become known as a "bipolar" device. Most field effect transistors are manufactured using MOS technology, especially those fabricated for integrated circuits; thus, these transistors or ICs are called MOS devices. Bipolar and MOS technologies are discussed detail later in the chapter.

SURFACE COATINGS

Surface coatings play an important role in the fabrication of semiconductor devices. These coatings fall into two general categories—insulators and conductors. The coatings are either grown or deposited on the surface of the semiconductor wafer during the processing.

Insulators

One of the reasons for the dominance of silicon as the preferred semiconductor material is the extreme usefulness of its natural oxide which can easily be grown on the wafer. Silicon dioxide may be deposited on wafers as either an insulating layer or masking coating. Silicon dioxide may be thermally grown or deposited by a pyrolytic technique which is similar to the deposition of epitaxial layers. Another insulating coating deposited by the pyrolytic technique is silicon nitride. This coating has proved to be extremely resistant to unwanted impurities and is used as a passivation layer. Devices passivated with silicon nitride have been shown to be reliable even though unencapsulated.

4.10 Semiconductor Materials and Physics

Conductors

The deposition and layout of conductors is an extremely important factor in the advance of integrated circuit technology. Conductors connect the resistors, diodes, and transistors in an integrated circuit. In general, the deposition techniques used for conductor application entail the use of high vacuum apparatus. The conductor is melted and evaporated onto the surface of the wafer through one of the several techniques. The basic conduction metals generally are either aluminum or gold. When gold is used a secondary metal layer is first applied to achieve effective contact resistance and adherence to the semiconductor slice. Polycrystalline silicon (nonsingle crystal) is also used as a conductor (between metal conductors) on some ICs.

4.11 Device Development

EVOLUTION OF NEW PRODUCTS

General

The evolution of new products occurs as a result of a twofold generation process. On the one hand, there is an expression of a particular need, such as logic gate arrangement resulting in a particular logic function, or a particular discrete device application, such as a microwave oscillator transistor. These particular needs will require specific device parameters, such as circuit speed, voltage-current parameters, and transistor noise figure. On the other hand, the semiconductor industry may have a particular technology that has reached a critical development stage. The developers hope to fill some needs or additional applications for the particular type of fabrication technology. Examples of this type of end-product development are CMOS filling the lower power logic requirements, automobile semiconductor electronics applications, consumer watch applications, and MOS memory applications. These applications were filled by new semiconductor fabrication technology and probably would not have been accomplished satisfactorily using older technology.

Once a need is identified and a tentative technology chosen, the development steps for a new product are straightforward. First, a basic process technology is identified. If the process is well established, the problem for new product development is mainly one of circuit design. If a new process must be developed, it is developed with simple circuits that can be compared with existing process familes.

Development Cycle

A circuit is proposed to provide the required performance or, for a discrete device, a geometry is developed which is expected to provide the proper specifications. Extensive computer-aided design techniques are utilized to verify the design principles. The circuit (or device) topology is proposed and checked; computer-aided design checks are used for complex circuits to avoid possible human error. The topology is then drawn at many times the final size for the photo reduction and replication steps to provide the process masks.

The initial wafer runs are processed, using the developed photo masks and compared against the desired results in a test program. The development engineer must iterate the process technology until the product fulfills the original need. This approach may require (1) the development of new masks to avoid some process problems or (2) alterations to the process to provide the proper performance.

As the product nears the end of the development cycle, the process and the photomask tooling are reviewed for production. Changes are proposed for ease of production. Several runs may be processed to develop test data for marketing purposes. If the product is entirely new, the marketing strategy may dictate extensive advertising prior to product introduction to test market the device. The assembly techniques should be well worked out so that the product will be ready when required.

The development process described above is somewhat idealized. Often, development cycle times must be shortened to meet customer demand or the competitive requirements of the marketplace. New devices are often made by the development laboratory and sold as completed devices at the same time that the production group is gearing up. A small company may be able to develop and put a device into production very simply because of the close communication among the personnel responsible. On the other hand, a larger company can offer extensive production capacity should mar-

4.11 Device Development

ket demand warrant it.

Product Design Considerations

After a particular circuit has been chosen and optimized, the specific product design considerations deal with the "topology," or layout of the circuit. Design rules have been developed that relate to the particular process that is envisioned for the circuit. These design rules are chosen by experience to maximize the process yield and optimize the performance of the family of devices undergoing the particular process. Examples of the rules would be in the emitter metallization to the emitter contact opening overlap, line-to-line spacing, base-to-emitter geometry spacing, and the like.

If the circuit is required to have performance superior to that of a standard process, a new process design must be developed. In this event, experience gained with other processes is used as the foundation for the new process design. Often only one or two of the specific processes must be changed. Such parameters as the epitaxial layer thickness, base diffusion depth and concentration, and emitter diffusion parameters are the ones normally varied. Since it is not efficient to vary the process parameters used in production, a separate set of processing equipment is generally required by the development group.

The process parameters and mask tooling are then carefully documented and a teaching process is used to transfer the device to the production facility. Many companies have found that close interaction between the development and production groups is required and have both groups report to the same engineering supervisors.

CIRCUIT DESIGN

In the design of integrated circuits, circuit fabrication technologies must be taken into account. The various technologies and processes (i.e., bipolar, MOS, and variations thereof) introduce design constraints that result from the dimensions of components, how they work physically, electrical parasitics introduced by certain component-isolation techniques, component-tolerance limitations, and various voltage and current limitations.

General Considerations

Three design considerations that are important for integrated circuits are:

- Nonoptimized components
- Component interaction
- Relative component cost

Bipolar and MOS IC fabrication technology can limit circuit performance because all of the components are fabricated at the same time. Thus, no advantage can be taken of process optimization for constructing the various components. By contrast, when discrete circuits are fabricated, each component can be tested and optimum choices can be made.

Monolithic integrated devices also present additional circuit design problems because of the interactions that occur among components within the structure and because of the deviations in component parameters from optimum values available with separate components. Sophisticated device models for the interactions of transistors and components have been developed. These models are used in conjunction with computer-aided design techniques and can account for both first and second order effects that can be critical in determining circuit performance.

Another design consideration is the economics of the silicon monolithic structure; i.e., the transistors and diodes can be much less costly in an IC compared with resistors or capacitors. It is very important to design circuits

with these relative values in mind so that chip size is minimized or device yield is maximized or both.

Logic Circuits

By far the largest number of integrated circuits is fabricated for logic usage—that is, they perform electrically simple logic operations or combinations of operations. Logic devices are used in digital circuit applications to provide gating, level restoring, memory, and so forth. The simplest form of logic circuit available in integrated form is Direct Coupled Transistor Logic (DCTL). The basic circuit configurations of the various logic families are shown in Figure 4.11-1. These families are generally known by their intitials, DCTL, RTL (Resistor Transistor Logic), DTL (Diode Transistor Logic), TTL (Transistor-Transistor Logic), and ECL (Emitter Coupled Logic). The most common type of logic used today is the TTL.

Recent logic family additions are CMOS and I^2L. These logic families are gaining in popularity because of limited power usage coupled with high-speed performance.

Several variations of the basic transistor-transistor logic gate are available; these variations include high-power TTL (HTTL), low-power TTL (LTTL), and Schottky TTL (STTL), and low-power-Schottky TTL (LSTTL). The basic logic gate structure for all of these families is similar; however, the circuit performance is altered slightly for speed or power consumption.

Linear Circuits

Because of the smaller market for specific linear circuits (compared with logic devices) and their more difficult design and fabrication, fewer linear circuits are available in commercial form. Increasing effort is being made to develop the potential market for some linear integrated devices designs by making them more flexible. This includes such standard devices as amplifiers and regulators. Other design options can be to provided extra devices in the structure with a variety of possible interconnection patterns or several components can be left out so that flexibility can be achieved by providing a range of different external components. Additional efforts have been made to partition various types of electronic equipment into circuit structures that can be made in monolithic integrated form. An example of this technique is the partitioning of a television set into five to seven circuit oriented sections.

Circuit Design Techniques

Because DC coupling is easiest in integrated structures, bias point stabilization has been a problem since silicon resistors and junction parameters are highly temperature sensitive. Techniques for avoiding this temperature dependence have been developed using resistance ratios and compensating junctions to avoid voltage shifts with temperature. DC feedback is used to eliminate resistors and provide additional stabilization. In linear structures, wide use has been made of Darlington amplifier connections to provide moderately high input impedances.

Parasitic capacitance effects are an important part of the design of semiconductor integrated circuit parts. The predominant parasitics are generally associated with the isolation junction.

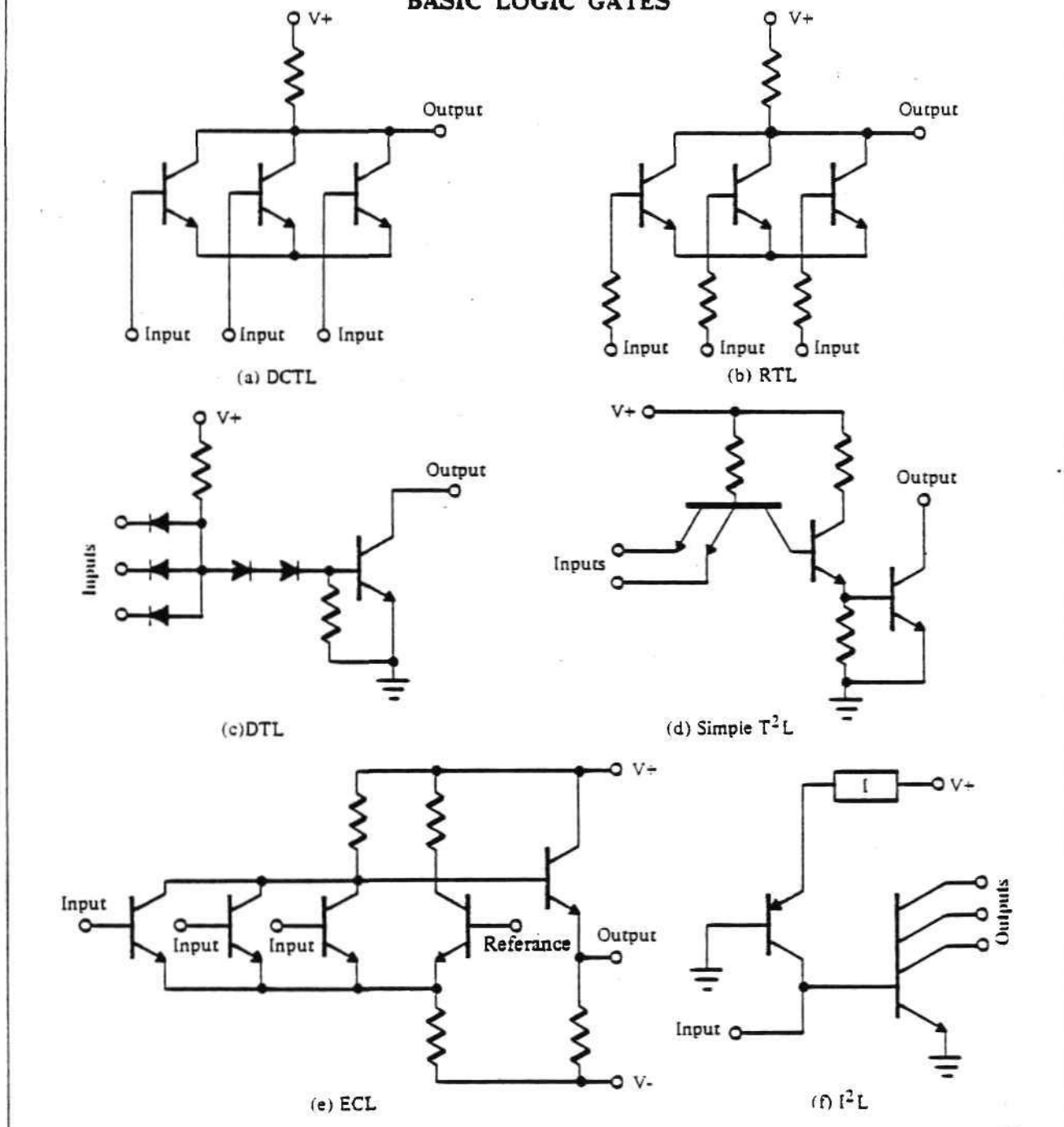
Circuit Layout

A major part of integrated circuit design is concerned with achieving the proper circuit pattern layout for the chip. The results of this process are the drawings of the various diffusion mask, passivation, and interconnection patterns for the circuit. As the patterns for the

4.11 Device Development

Figure 4.11-1

BASIC LOGIC GATES



Source: DATAQUEST, Inc.

photoreplication steps, these drawings, coupled with the process flow and descriptions, form the engineering documentation for the particular circuit manufacture.

The circuit must be arranged in a planar fashion. The number of elements should be minimized, and interconnections should be eliminated. The pattern layout must also attempt to minimize device size. Generally, standardized transistor, diode, and resistor shapes are used, and standardized computer-aided pattern generation is extensively employed. As the circuits for individual chips become increasingly more complex the computer-aided design and layout algorithms become required design tools rather than mere aids. The end results of the layout cycle is a composite scale drawing of the chip process layers that resembles modern art.

The composite drawing is reviewed for potential difficulties—i.e., nearly touching nonconnected diffusion areas, potential bridging faults etc. Since the drawing is idealized, experienced judgment is required to visualize how the completed patterns will appear. This judgment compensates for potential photographic flaws that can occur in an attempt to maximize yield.

The composite drawing is broken into separate drawings of the particular layers, and a pattern is made for each process step. Minimization of the number of steps is one of the design goals since each process step adds cost to the circuit fabrication. The layer drawings are the documentation for the preparation of the photographic tooling required for manufacture described in the next subsection.

PHOTOREPLICATION

The techniques of photoengraving are necessary for planar processes and interconnections in integrated device technology. The photoengraving masks that define the geometry on the silicon wafer are made through the use of high resolution photographic and photoreduction equipment, step and repeat cameras, and precision drafting equipment. Using these and the circuit topology layout provided by the design engineer, a series of photographic masks is prepared which defines the areas diffusion, contacts, and interconnection patterns.

Masking

We have previously discussed that oxides and nitrides can be formed on the surface of the silicon wafer, acting as a mask against the diffused impurity dopants. It follows that diffusions can be defined in specific areas of the wafer if the oxide is preferentially etched away in that area. With the use of photoengraving techniques, preferential oxide etching can be accomplished readily. This process is described in the Manufacturing Chapter on pages 3.1-7 to 3.1-8. Similarly, high conductivity metallic interconnection patterns can be formed on a wafer by photoengraving techniques. If the wafer is coated with a metal, such as aluminum, the use of photolithographic techniques permits exposure of the excess aluminum, so that it can be etched away and leave the wafer with an aluminum interconnection pattern.

The use of the term "mask" in semiconductor integrated circuit technology may prove to be confusing unless careful attention is paid to the context within which the term is used. There are three kinds of "masks": "photographic mask," "photoresist mask," and "oxide mask" have been mentioned. The photographic mask is a positive or negative image of the circuit pattern formed on a photosensitive glass plate. It is used for forming the resist mask. The resist mask is formed on the wafer in the photoresist, a photosensitive lacquer-like film which is applied to the wafer. It is used for selectively protecting areas from etching the oxide or aluminum it covers. The oxide mask is the etched pattern remaining in the oxide when

the resist is removed and is used for selective diffusion.

Figure 4.11-2 shows several of the typical masks used in the fabrication of silicon integrated circuits. To process a particular circuit, a set of precision photomasks is required—one mask for each step in the process. Each mask carries a set or "array" of several hundred identical patterns. The patterns must be reproduced on the mask with exacting precision. Each mask in the set must be precisely registered with all of the others, so that when all of the masks are superimposed, the registration between masks is kept within narrow tolerances. These requirements derive from the small sizes of the finished circuits, and the small dimensions used in their fabrication. For example, an emitter width can vary from 0.1 mil (1/10000 of an inch) to 0.25 mil depending on the type of circuitry and speed performance. The unit-to-unit variation in distance across the array must be smaller than the width of the emitter if the emitter is to be positioned in the same place across the entire wafer.

Photographic Masks

Photographic masks are prepared by reduction techniques. The masks are drawn from 50 to 500 times the actual size on a clear sheet of mylar covered by a red film called "peel coat." The artwork is produced by cutting and peeling the red film where the pattern is desired. In preparing the artwork, the cutting is performed by the use of a precision coordinatograph. Machines are available with an accuracy of 0.1 mil and may be motor driven from a computer prepared tape. Although a number of techniques have been used to produce the array of photographic images on the master patterns, the technique generally used is called the step-and-repeat process. This process, as its name indicates, produces a two-dimensional array of images by a multiplicity of exposures. Each exposure forms a single image. The shifting of the photographic plate between the exposures must be accomplished with great accuracy and is usually performed with an X-Y coordinatograph possessing an accuracy of ±1 micron (1 micron is 1 millionth of a meter). Although this system suffers many disadvantages owing to its mechanical nature, the optical quality of the result is excellent and overcomes the mechanical disadvantages.

New Photoreplication Technologies

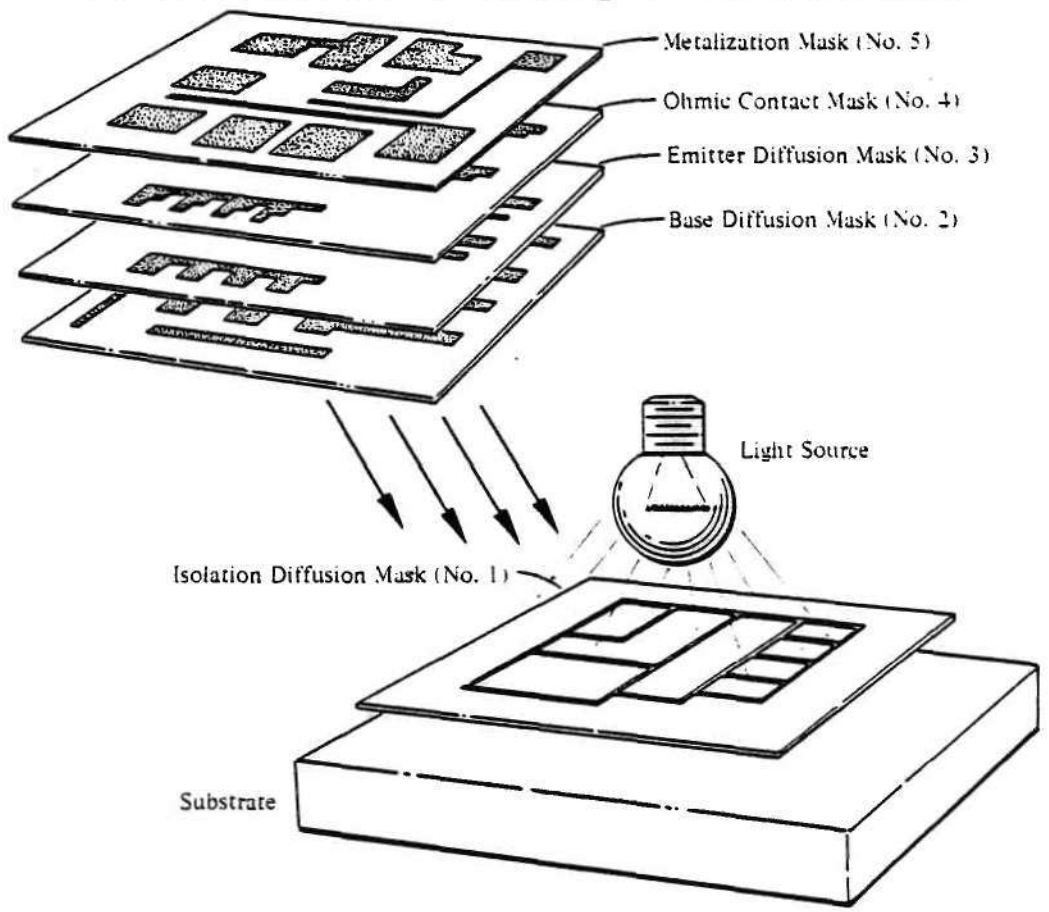
The existing means of photolithographic processing are approaching the difraction limits as a result of the practical clearance problems between the wafer and mask for making device line widths much smaller than 2.5 or 3 microns. With careful photolithographic techniques, devices have been fabricated down to 0.5 micron in resolution, but such techniques are now used only for microwave devices. Figure 4.11-3 shows the history of practical photoreproduction geometries for the minimum microwave transistor emitter widths and practical lines on ICs for good production yield.

Alternative technologies that are now being explored should be ready for commercial application in a few years. The two technologies are X-ray lithography and electron beam lithography. Electron beam lithography consists of employing a fine beam of electrons to expose a pattern on the resist. This resist pattern can be formed directly on the device or can be used in making high-resolution masks for photolithography with either conventional lithography approaches or X-ray lithography. The overall mask making scheme for employing electron beam photolithography is shown in Figure 4.11-4. It is generally agreed that some combination of E-beam lithography with X-ray lithography will be needed to further reduce production IC line width.

Several techniques for electron beam li-

Figure 4.11-2

PHOTOMASKS USED IN SEMICONDUCTOR FABRICATION



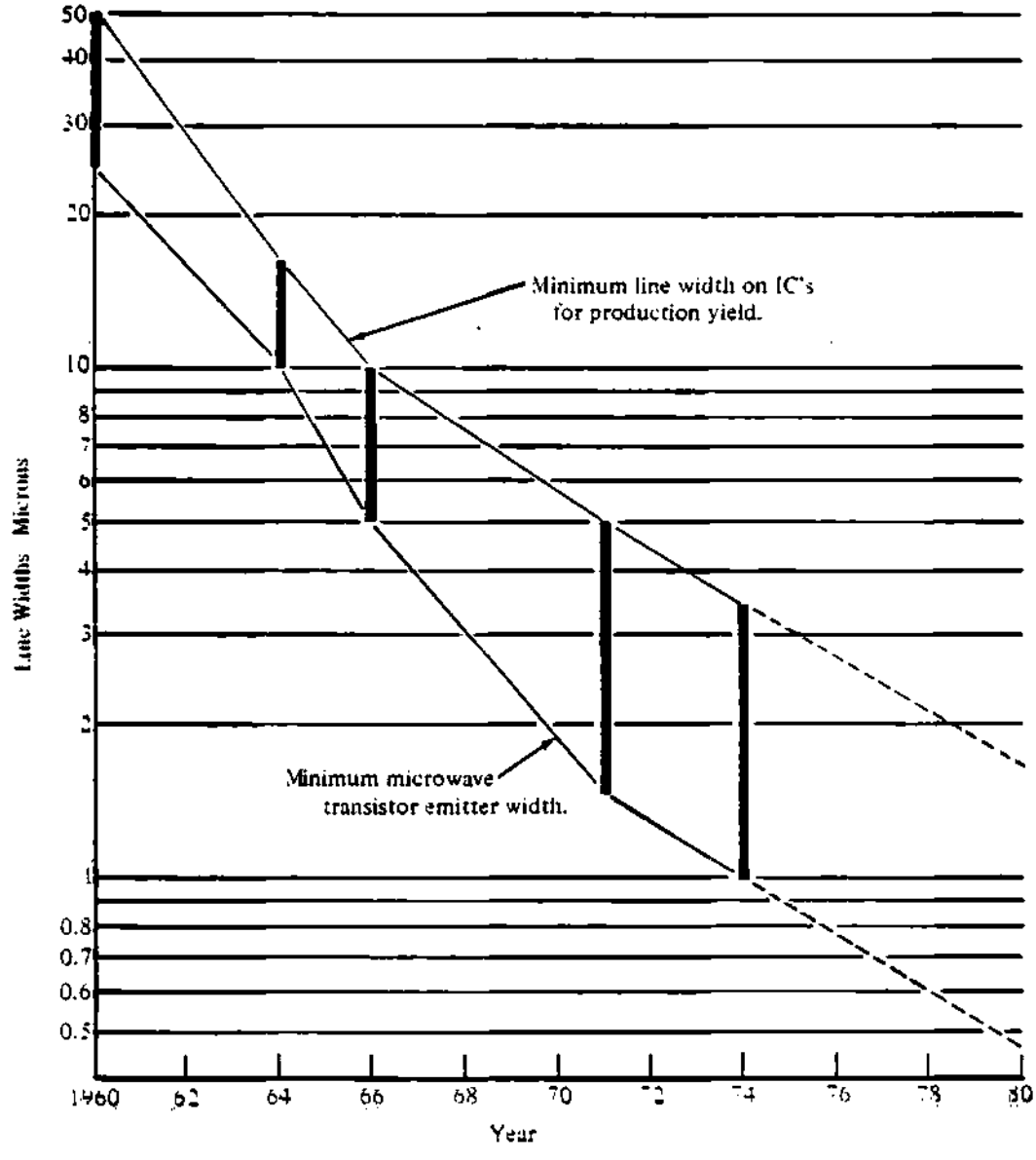
Source: DATAQUEST, Inc.

thography have been explored in recent years. They include flying spot scanner, raster-scan techniques, and vector-scan techniques. The technology required for electron beam sensitive resists have been well developed. Several companies—including Bell Telephone Laboratories, IBM, Texas Instruments, and Western Electric—are leaders in this new technology.

As in all photographic work, it is relatively easy to perform work of fair quality, but extremely difficult to achieve very good or very precise results. Exposure times are critical. Optimum exposure depends on the line width in the circuit pattern, and, therefore, critical dimensions on the same plate should be at the same value, or a compromise exposure may be necessary. Extreme cleanliness is required in the areas where photographic areas are produced. The glass with the photosensitive material must be of extremely high quality and must be optically flat for minimum registration error. The lenses used in the camera systems are of the

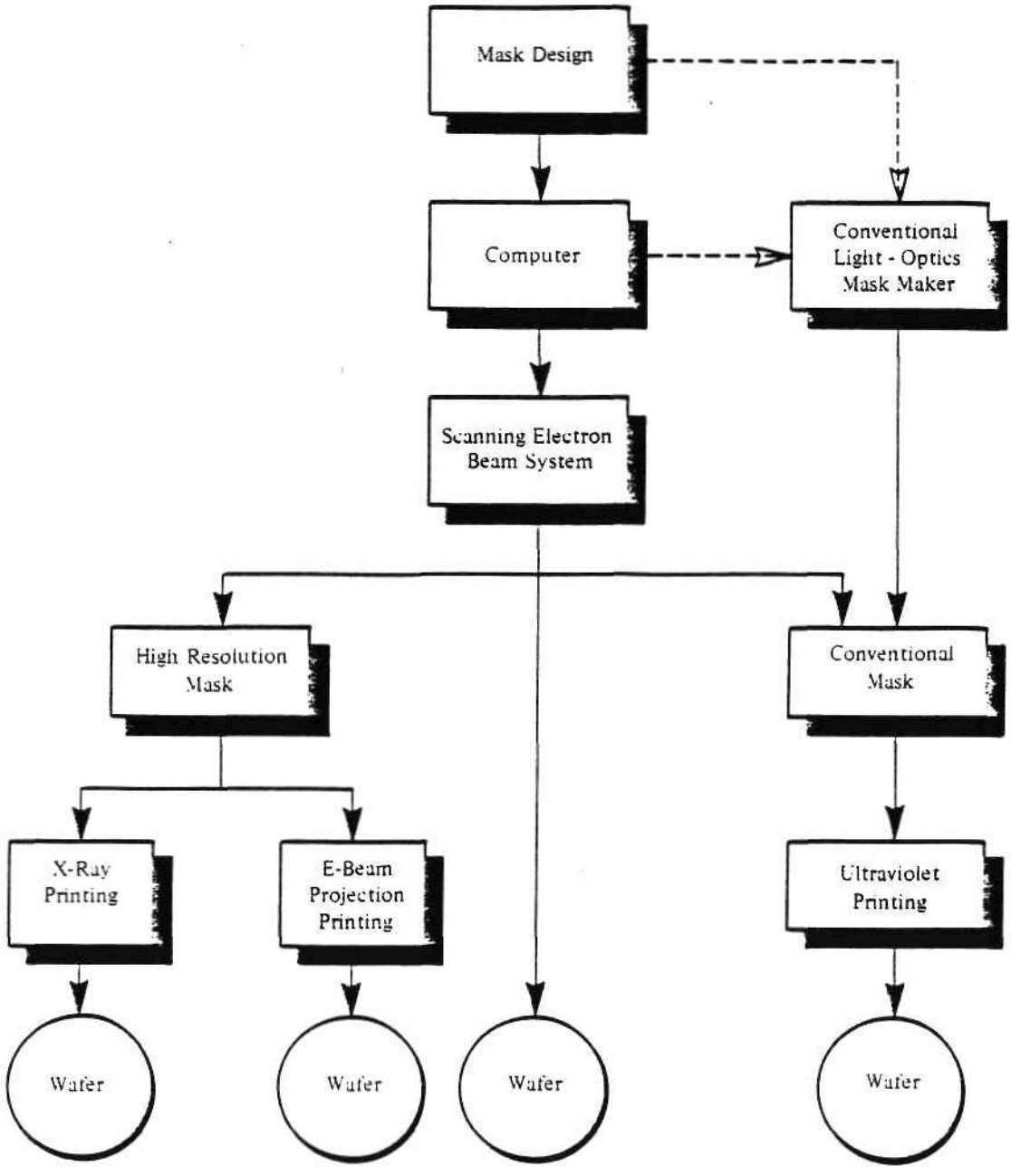
4.11 Device Development

Figure 4.11-3
PRACTICAL PHOTOREPRODUCTION TOLERANCES



Source: DATAQUEST, Inc.

Figure 4.11-4
METHODS OF MASK MAKING AND MASKING



Source: DATAQUEST, Inc.

highest quality and cost several thousand dollars per lens. The trend toward increasingly larger circuits fabricated on larger silicon wafers imposes even more stringent requirements on the critical photomask process. Since defects in the photo images will be reproduced directly on the slice during the processing, a great deal of effort has been expended to produce defect-free photomasks.

PROCESS DEVELOPMENT

The fabrication of semiconductor devices and integrated circuits is an electrochemical process. The development of the particular plan for a specific circuit results from an extensive process development cycle.

This cycle starts with the process design formulated by the development engineer. The process flow designed by the development engineer lists all of the fabrication steps necessary for the wafer to be made. Many of the operations are standard processes that are used for both development and factory processing. There may be more than 100 operations between the initial wafer cleaning step and the final wafer probe. If these operations are performed sequentially with no waiting time the total process time might be 50 hours. Unless a crash development program is under way, the cycle time is two to three times longer because of the queues before each process. Furthermore, several products are usually being developed simultaneously with the same fabrication personnel.

Circuit "Prove-Out"

The development engineer's responsibility is to "prove-out" the projected process flow. In the simplest cases, this may mean the processing of one or two "process firsts" to verify the circuit design, using standard diffusions and contact metallizations. The completed circuit is operated for the first time as a single device. Problems in layout may be discovered as a result of processing difficulties or faulty electrical performance. Improvements in the mask set are usually necessary for ease of alignment or for accounting for second order diffusion effects. If distributed electrical parasitic effects are too great, the circuit may have insufficient speed as fabricated, requiring extensive redevelopment.

Improved performance may be achieved by tailoring the process for the individual circuit. Speed may be increased by changing the transistor diffusion cycles to create a shallower device. If one of the transistor diffusions is used for other types of devices on the circuit, such as resistors or diodes, the performance of these devices will be altered by the change in diffusion processing. Care must be taken, therefore, to consider all of the ramifications of any process change.

New Processes

Another responsibility of the process development group is to implement process improvements to achieve increased yields or lower costs. These developments might include evaluation of the types of photoresists, new fabrication equipment developments, new diffusion sources and techniques, and oxidation and passivation layer depositions.

As an example of this type of development process let us examine the incorporation of boron nitride (BN) as a diffusion source. Prior to 1971 the generally used boron source was liquid boron tri-bromide (BBr_3). The source gas was bubbled through the liquid and then passed over the semiconductor wafers. Precise control of gas flow and wafer placement is required for uniformity throughout the total batch. By contrast, BN is a solid that may be placed adjacent to the silicon slices in the furnace. The precise details of the boron nitride diffusion process entail the activation and stor-

age of the BN slices, gas glow adjustments, BN to silicon slice distance, type of diffusion boat, and so forth. Only an extensive empirical development cycle could be used to completely specify all of the process variables. Although guidelines can be obtained from the technical literature, each manufacturer must verify the particular process for his products.

Similar empirical development programs are undertaken for almost all parts of semiconductor device processing. Processes may be developed for one class of devices and applied to many of the other categories. For instance, shallow diffusion technology developed for microwave transistors resulted in improved diffusion cycles for ECL logic and very low power integrated circuits. The isoplanar process developed for improved metallization techniques has resulted in greatly improved packing densities and has been applied to several technologies. The steady advance of semiconductor technology is largely the result of continued process innovation.

PACKAGING

If semiconductor devices are to be useful and function under various conditions, they must be properly packaged. Packaging offers protection from external and environmental conditions and provides a convenient means of handling. To be useful, proper packaging must minimize the requirments for special tooling. The design of the package depends upon the intended use of the device. Simple packages may be used for equipment intended to operate in normal settings such as a laboratory or home. More complex, rugged packages must be used for hostile environments such as a steel mill and oil well applications or space exploration.

The semiconductor manufacturer is responsible for the performance and reliability of his devices. The manufacturer must consider the characteristics of mechanical design, hermetic seal, stress, and similar factors as part of the device development process. The general considerations fall under the areas of:

- Electromechanical requirements
- Attachment techniques
- Package materials

Although semiconductor devices continue to be assembled individually by hand, development activities aimed at automating the assembly process are beginning to bear fruit. Continued cost improvements in semiconductor and integrated circuit devices will require additional automatic assembly technology. DATAQUEST expects that the efforts to automate the assembly and packaging processes will continue with increasing success.

Electromechancial Requirements

Packages must carry current between the external elements and the device or circuit terminals and provide suitable isolation between the current leads. The package should not degrade the operation of the device by adding additional parasitic elements to the electric circuit. Circuit speed, current-carrying capability, series resistance, and the like are some of the electrical design factors that must be considered.

The package must be strong enough to withstand the handling stresses of device and circuit assembly. The designer must consider bending of leads, dropping, soldering, and so forth, as well as temperature and pressure and other environmental ambient extremes. The package must protect the circuit from these extremes. The configuration of the package for handling, layout, and system assembly must also be carefully reviewed.

Since the devices generate large heat densities, the package must provide a heat path

from the device to the outside. Without a good thermal path, the chip can easily exceed the maximum allowable operating temperatures. Thus, the package must be constructed of materials with good thermal conductivity for efficient heat removal.

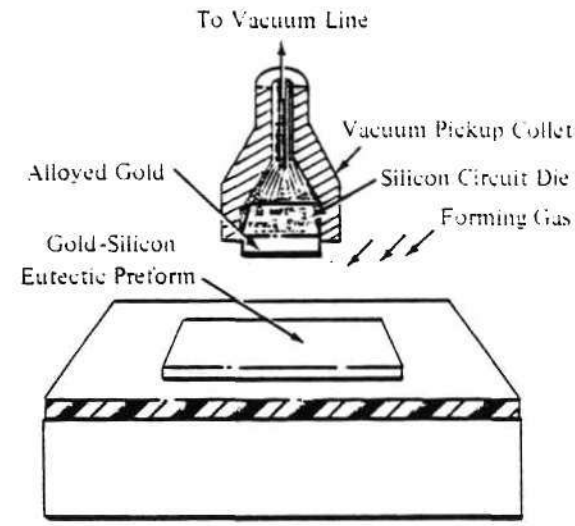
Attachment Techniques

Silicon chips or dice may be mounted in the package by alloying, soldering, or brazing, as well as by the use of cement. If electrical insulation is required, as in high-frequency circuits, the chip is mounted on metallized islands on an insulator adapted to fit into the package. Figure 4.11-5 illustrates a basic alloy die attach operation. All package metals and metallized islands are usually of metals that have mechanical expansion coefficients matching that of silicon. Eutectic alloying preforms are chosen so that the alloying temperature, necessary to secure the chip to the package or land, is lower than the temperature used in making the chip. This is done to prevent shorting the chip by realloying the contacts or other problems. In most cases, gold doped with a trace of germanium or silicon (to slightly lower its solubility in the silicon chip at the alloying temperature) is used for a preform.

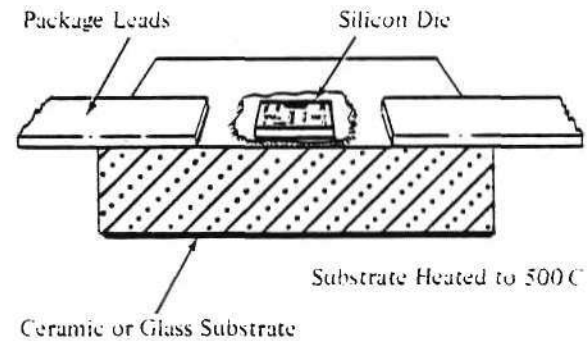
Circuit dice may also be attached to ceramic or glass packages with a low temperature glass frit as shown in Figure 4.11-5. This packaging technique utilizes the fact that the back of the integrated circuit die is generally not used for electrical connection. The electrical connections are brought to the chip through the package leads which are brazed to the ceramic substrate in an earlier operation.

After the integrated circuit die has been attached to the package, it is necessary to make electrical connections between ohmic-contact areas of the circuit and package leads. The most commonly used method today consists of attaching extremely fine wires to the various

Figure 4.11-5
BASIC DIE ATTACH OPERATIONS



(a)



(b)

Source: DATAQUEST, Inc.

areas to be interconnected by thermocompression bonding. This process requires the simultaneous application of heat and stress, leading to the deformation of at least one of the members being joined. A variety of bonding machines, including the so-called wedge bonders, nail head or ball bonders, and stitch bonders, have been developed to accomplish thermocompression bonding. Although ball bonding, illustrated in Figure 4.11-6, requires individual attachment of the bonding wire to each contact pad, it is still the most commonly used technique today because of its reliability and bond strength.

Two alternate approaches for lead connection and die attaching are illustrated in Figure 4.11-6. The first of these, flip chip attachment, shown in Figure 4.11-6b, has been extensively used by IBM in its Solid-Logic-Technology (SLT). It employs the use of plated solder bumps to connect to small raised lands on a ceramic substrate. The chief disadvantage of this approach is the extreme care that must be used during die placement to solidly connect to the circuit or device chip. A second "upside down approach" was developed in the mid-1960s by Bell Telephone Laboratories, and is illustrated in Figure 4.11-6c. Beam lead attachment is utilized for the some integrated circuits used in defense applications but has not been extensively employed elsewhere. The chief disadvantage of this type of attachment is the large amount of the silicon area required for the extended plated-gold beams. This large area of silicon detracts from the useful device area and increases the cost of the die by increasing the number of wafers that must be processed. In the past few years extensive work has been done on approaches to eliminate wire bonding and lower assembly costs. The most successful to date is based on the "mini-mod" process originally developed by General Electric. In this process raised bumps are placed on the contact pads in a second metallization process. The lead frame for the circuit is fabricated on a piece of Kapton film which is slightly transparent. In the process, the objection of die placement is overcome because the operator can see through the lead frame carrier. Once the mini leads are attached to the circuit, the circuit and frame are encapsulated in a plastic resin. Extremely high production rates may be achieved by this technique in the future. Rates in excess of 1,000 to 2,000 units per hour per operator have been quoted. These rates compare with the 100 to 200 units per hour for conventional chip and wire bond technology.

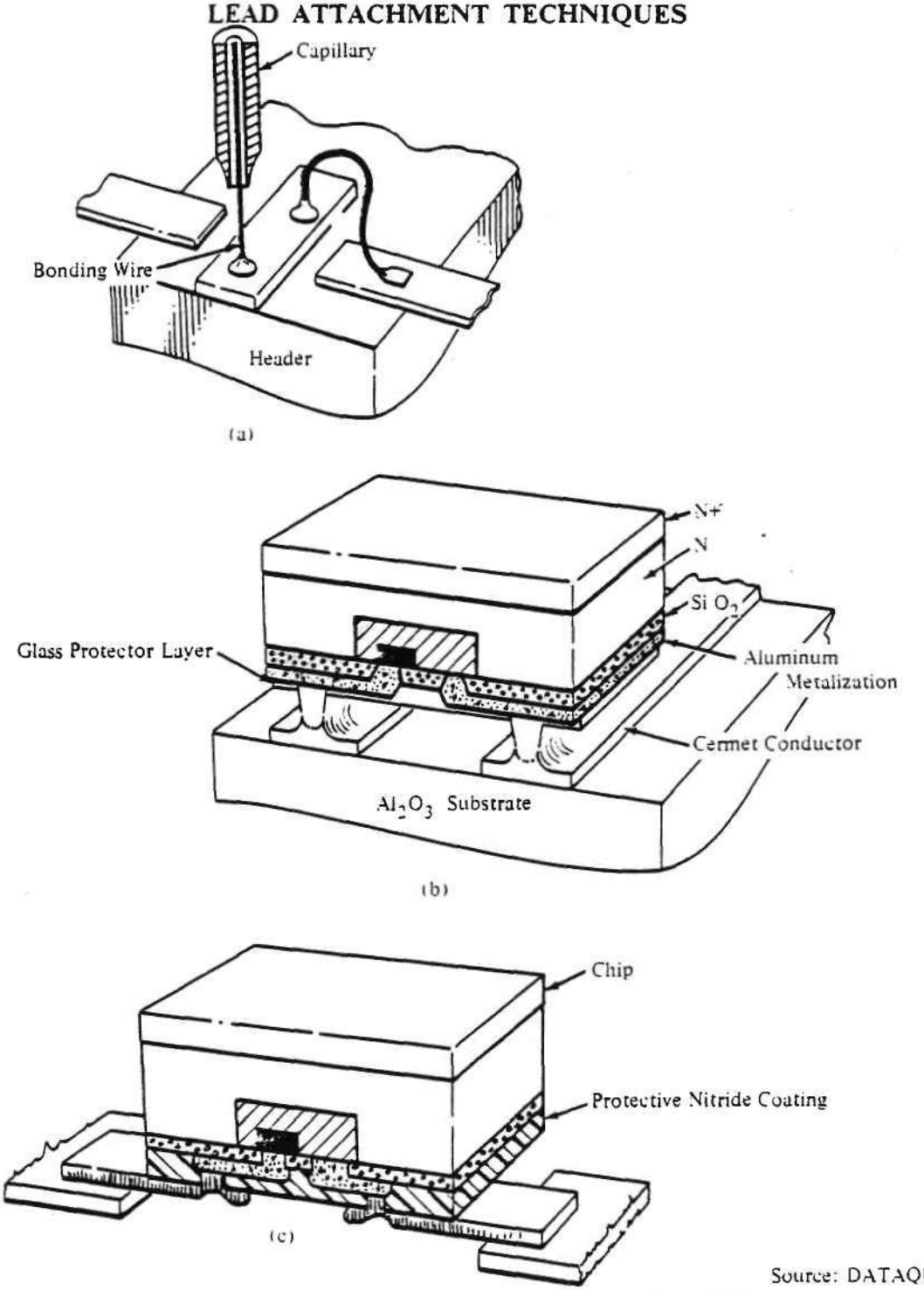
Package Materials

Transistor technology brought about a revision in electronic component packaging. Earlier active devices, such as vacuum tubes, were situated in glass or metal-cased vacuum evacuated tubes. The small size and simplicity of the transistor necessitated the development of a new packaging concept that would be compatible with the device. One approach to transistor packaging was finally standardized through a series of "cans." These cans utilize a header through which the leads protrude and a "top hat" shaped cover, see Figure 4.11-7. After the chip and bond wires are attached, the cover is welded to the header in an inert atmosphere chamber. The glassed metal assures the hermeticity of the package where the leads protrude through the header.

Whereas the cans were designed as a container for transistors and later adapted to integrated circuits, the flat pack was specifically designed as a container for ICs. To minimize the wasted volume of the cans, the flat pack was designed to conform as closely as possible to the geometry of the "chip" that it was to contain. This was accomplished by passing the leads through the walls of the package rather than through the base as in the case of the can.

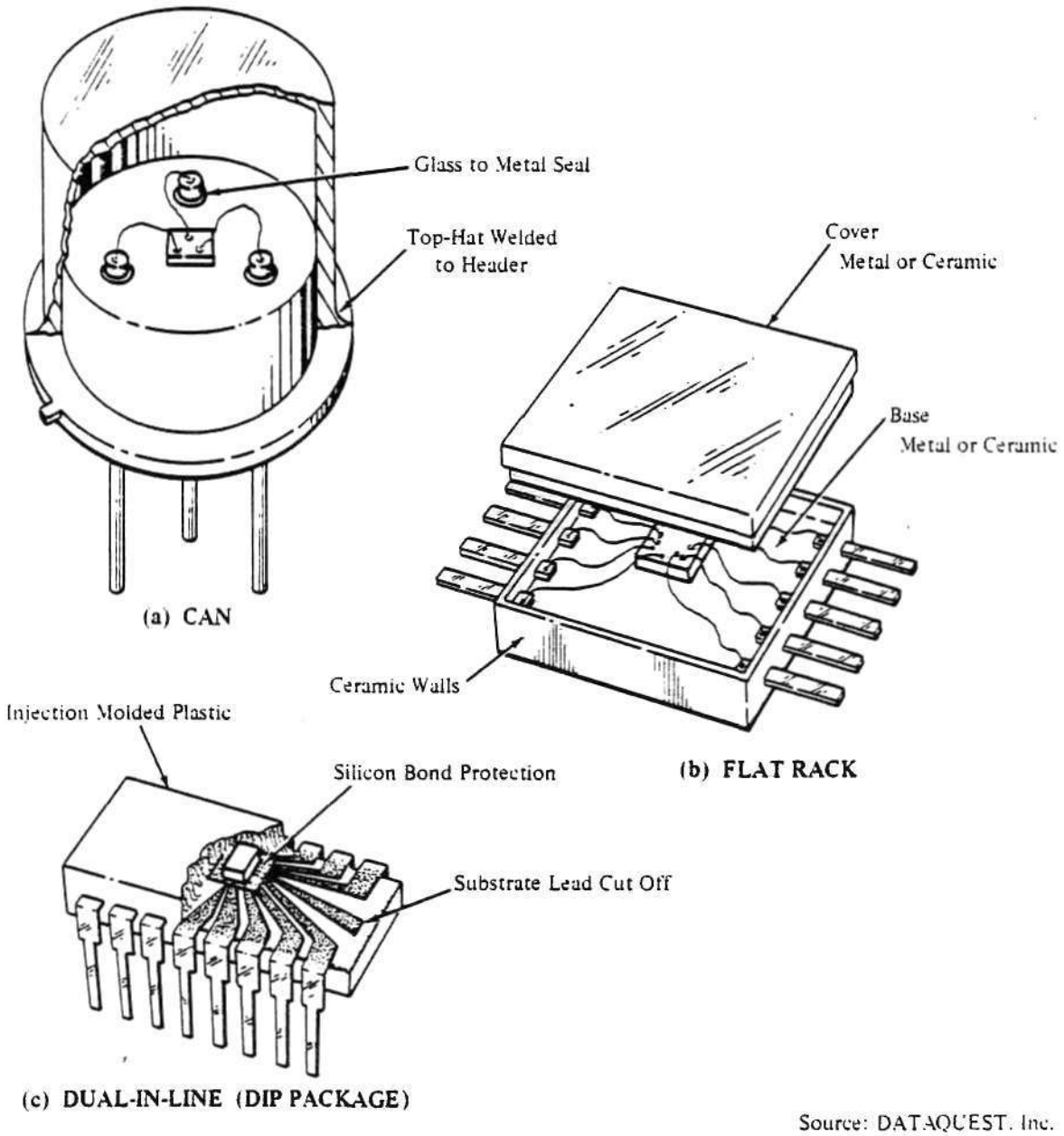
Figure 4.11-6

LEAD ATTACHMENT TECHNIQUES



Source: DATAQUEST, Inc.

Figure 4.11-7
PACKAGING METHODS



Source: DATAQUEST, Inc.

4.11 Device Development

Passing the leads through the side of the package offered several advantages. First, projecting the leads from the sides of the package is more compatible with planar packaging systems. Second, by utilizing the walls, more leads can be brought through the package for a given size and still retain reasonable spacing between them. There are many types of flat pack manufacturing technologies. The initial packages were based on the glass to metal seal technology of the cans. Later packages have been manufactured using ceramic to metal brazing processes and ceramic sandwiching processes. The ceramic sandwich process has proven to be the strongest package and the least expensive to produce.

The most commonly used integrated circuit package is the dual-in-line package (DIP). This package was designed primarily to overcome the difficulty associated with handling packages and inserting them into mounting boards. The DIP package is easily inserted either by hand or by machine. It requires no spreaders, spacers, insulators, or lead forming. This package when made of plastic is finding wide use in commerical applications: a number of military and computer systems utilize a ceramic form of this package.

The most cost effective packaging technology developed to date has been the variety of plastic packaging techniques utilizes epoxy, phenolic, and silicon. These packages employ a stamped or etched lead frame of relatively thick metal on which the chip is attached and the leads bonded. The assembly is subsequently run through a plastic molding process employing specific temperature and pressure conditions. Such devices are usually specified for use over limited temperature ranges in commerical applications.

Although a great deal of reliability testing has been done on plastic packages, controversy surrounds their use. Some users have resisted efforts to allow wide use of plastic encapsulated devices in their equipment. One of the primary reasons for the restriction is the belief that the plastic may not provide the necessary hermeticity for high performance applications. The most serious problems with many plastic devices is the inability to make an effective seal at the lead-plastic interface. This failing allows moisture to penetrate the device at the interface and corrodes the metallization, which causes conversion layer leakage on the chip.

4.14 Optoelectronics

INTRODUCTION

In the past, optical effects of semiconductors have been undesirable characteristics. If a transistor case was somewhat transparent, spurious performance would result because unwanted light impinging on the surface of the crystal generated a charge. Unwanted leakage, current effects, and undesirable signal paths were then created. For this reason, most if not all of the plastic cases used in the semiconductor industry are loaded with black compound to eliminate light. MOS circuits are particularly light-sensitive, and some are actually tested in darkened rooms to allow more optimum testing conditions. Certain optical characteristics have given rise to a new electronics industry: optoelectronics.

Product Division

The optoelectronics products can be divided into a number of categories. Liquid crystal devices are discussed at the end of this section because of their close associations with the semiconductor industry. The division used in the DATAQUEST Semiconductor Industry Service is as follows:

- Light sensing devices
  - Bulk effect
  - Junction
  - Schottky
- Light emitting devices
  - Visible single lamps
  - Displays
  - Infrared emitters
- Optical couplers
- Solid-state lasers

Characteristics of Light

To better understand the characteristics and technology of light-emitting and light-sensing devices, it is necessary to understand something of the nature of light. Light is electromagnetic radiation at a particular wavelength. The wavelength, usually measured in microns, determines the color of the light. Visible light has a wavelength ranging from about 0.38 microns to 0.76 microns. Below the visible spectrum of 0.38 microns light is termed ultraviolet (UV) and immediately above the 0.76 microns it is designated as infrared (IR). Although ultraviolet and infrared light are not visible to the human eye, they are still significant in the field of optoelectronics.

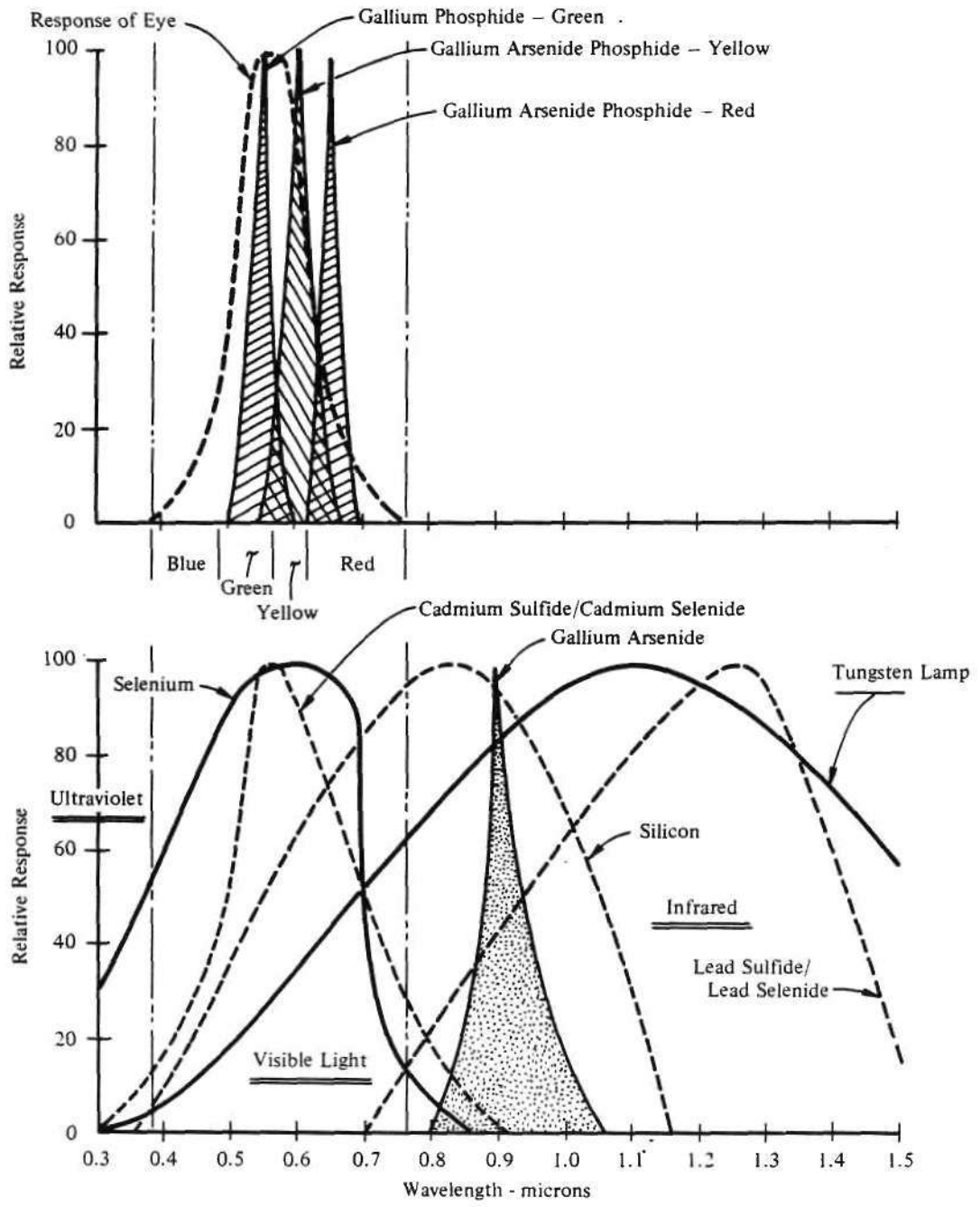
Figure 4.14-1 shows the spectral response curves of the human eye and the various semiconductor materials that are important optoelectronics. They include sensors of silicon, cadmium sulphide, cadmium selenide, and lead sulphide, as well as emitters of gallium arsenide, gallium phosphide, and gallium arsenide phosphide. The curves are normalized so that the peak of each curve represents the most sensitive wavelength for that material.

Several things should be noted about these curves. First of all, the human eye does not see all colors equally well. It is most sensitve to the yellow-green spectrum and is relatively weak in the red spectrum. This limitation is important because it means that a yellow or green light does not have to emit as much energy to appear equally bright. It should be noted that solid-state emitters produce radiation in very narrow—nearly monochromatic—bandwidths whereas a tungsten lamp emits light over a very broad range. Finally, it should be noted that the sensors made of cadmium selenide and cadmium sulphide very closely resemble the response of the human eye and are well suited, therefore, for simulated viewing functions, such as light meters. Similarly, silicon sensors and gallium arsenide sources are well matched in the infrared range and thus are well-suited to control functions where the spectral simulation of the eye is unimportant.

4.14 Optoelectronics

Figure 4.14-1

SPECTRAL RESPONSE OF VARIOUS EMITTERS AND DETECTORS



Source: DATAQUEST, Inc.

4.14 Optoelectronics

LIGHT SENSORS

Bulk Effect Sensors

Photoconductors are materials whose conductivity is sharply increased when they are exposed to light and are bulk effect sensors. They are basically light-sensitive resistors. The absorbed energy releases electrons at the surface, and the electron-hole pairs are produced. In semiconductors, these electrons and holes remain separated sufficiently long enough to enhance current flow when an external electric field is applied, i.e., conductivity is increased. The increasing conductivity depends on the number of electron-hole pairs generated, which is proportional to the intensity of incident light radition. As a result, the current flow is proportional to the light intensity as well as the area of the surface exposed to it.

Photoconductive cells are low-cost photoconductive devices comprised of bulk compounds, such as cadmium sulphide, cadmium selenide, and lead sulphide. These compounds are fabricated by pressing a powder onto a ceramic substrate and sintering it. Contacts are provided at each end of the sensitive area. These photoconductive cells are essentially uniform semiconducting masses with large dark resistance—of several megohms—which drops dramatically when exposed to light.

Bulk photoconductive cells have a relatively low frequency response, in the kilohertz region, whereas the response range of a silicon junction device is in the megahertz region. On the other hand, the operating currents of the junction devices are very low, on the order of microamps or a few milliamps, whereas those of photoconductive cells can range up to 0.5 amp.

Junction Light Sensors

Junction light-sensors are employed to generate power, as in photovoltaic cells, or to sense light for other reasons. In the latter case, photodiodes, transistors, and others are biased by a voltage and operate as active devices.

Photovoltaic Cells

A photovoltaic cell absorbs radiation and produces an output voltage related to the incident radiation, thus converting color energy to electricity, A P-N junction in a semiconductor forms a barrier that separates the hole-electron pairs formed by the breaking of the covalent bonds. The open-circuit voltage of the photovoltaic cell is approximately a logarithmic function of the illumination level. Except for very small cells, the open-circuit voltage is independent of cell area.

Many types of semiconductors have been used for photovoltaic devices. The most common materials being used today are silicon (largely because of its ease of fabrication) and selenium (as a result of its spectral response). Other materials that are occasionally employed for photocells are germanium, cadmium telluride, indium phosphide, indium antimonide, and gallium arsenide.

As a result of the energy crisis, new materials and technologies are being explored for solar cell development. The primary objective for development of effective solar cells is concerned with the conversion efficiencies of the light to electrical energy. Recently, a thin-film solar cell with 12 percent efficiency was announced. It utilizes a hetero-junction (i.e., two different semiconductor materials) composed of a polycrystalline N-type cadmium sulphide deposited on a single-crystal P-type indium-phosphide substrate. Other announcements of improved efficiency have been made using gallium arsenide solar cells.

4.14 Optoelectronics

The construction of a silicon solar cell is shown in Figure 4.14.-2. In this construction, a shallow boron diffusion is made into an N-type silicon substrate. It is important that the junction be fairly shallow so that the light is not absorbed entirely in the P-type region and the hole-electron pairs can be separated. An anti-reflective coating consisting of a silicon oxide or silicon nitride deposition of the proper thickness is applied to the diffused surface. This coating acts as a transmission match between the silicon and the air above it, preventing reflection of light from the surface. A solid metal ohmic contact is fabricated on the N-type side and a grid pattern of contacts, which permits light absorption, is made to the P-type side. In addition to converting solar energy to electricity, photovoltaic components find use in card-readers, cameras, and light-sensitive switches.

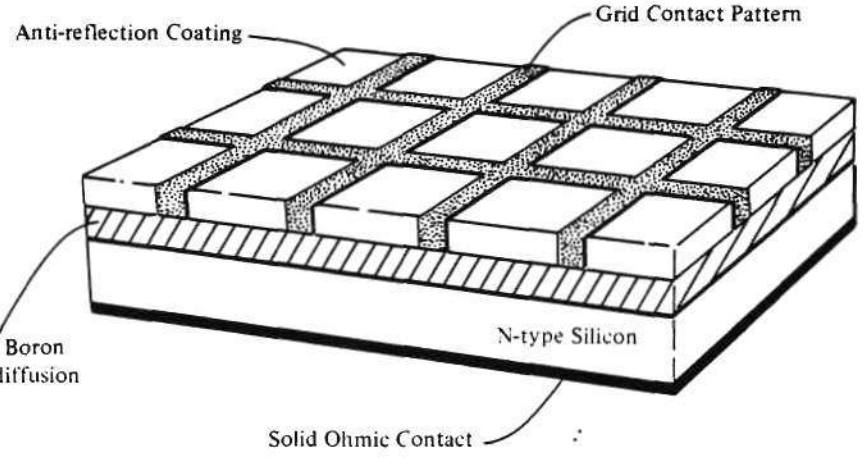
Photodiodes

When a PN junction is operated under reverse bias and light shines on it, the leakage current increases. This light-sensitive current can vary from tens of microamps to hundreds of microamps; it is directly proportional to the light intensity on the diode. Such diodes may be made of silicon or germanium and are generally formulated in the PIN diode format (P-type, Intrinsic, N-type) junctions to decrease the diode capacitance. This decrease in capacitance and corresponding increase in the depletion region allows less recombination of the electron-hole pairs and improved speed response.

By selecting the material characteristics (dopant concentration, lifetime, and mobility) and the diffused impurity type, it is possible to optimize the photodiode for various characteristics such as the speed of response, the dark current, the light wavelength efficiency, and the

Figure 4.14-2

SILICON SOLAR CELL CONSTRUCTION



Source: DATAQUEST, Inc.

electrical parameters of the diode.

Charge-coupled devices (CCDs) employ the charge generated by light much in the same manner as a photodiode. They have the advantage that large arrays may be employed and the generated charge sequentially moved to a detector. A further discussion of CCD devices is given in Section 4.3. Although there are a large number of special photodiodes for certain applications, they are basically PN diodes and behave according to the diode theory.

Phototransistor

A phototransistor is more sensitive than a photodiode. By having the light shine on the reverse biased collector-base junction, electron hole pairs are created and act as a base current. This base current is multiplied by the beta, h_{FE} (current gain), of the transistor, thus increasing the sensitivity of the device. However, the dark current (the leakage current of the device) is also multiplied. Some phototransistors have only the collector and emitter leads while others have a base lead. It has been found that open base optical transistors provide the largest optical gain.

Photo FET

Field effect transistors (FETS) are notably light-sensitive. The gate junction acts as a photodiode, and the drain-to-gate junction is normally reverse-biased through a gate resistor. The mechanical geometry of an FET is not optimum for light-sensitivity. Most of the gate junction region is covered by metal source and drain contacts so that care must be taken not to focus a small light source on the surface where it could be blocked by a contact.

SCR Photo Devices

Photo PNPN devices are similar to standard PNPN designs with one collector junction exposed to light so that triggering by light may be used. The highest current carrying capacity of any of the junction photo devices is found in a light-activated SCR. Both electrical and light signals can be used to activate the device, otherwise it operates as a regular SCR. Once the device is triggered, it conducts until the voltage across it is removed or reversed. Light-activated SCRs can be used to replace relays, to drive higher activity SCRs, or to provide logic switching functions.

Schottky Photodiodes

Schottky photodiodes find special application for very sensitive light-sensing, especially at certain wavelengths. Their operation is similar to that of regular junction photodiodes, but they often can be designed to have a much faster response time.

Applications

New applications for solid-state light-sensing devices are being announced regularly, and this trend will very likely continue. The devices are primarily used for industrial control computers, peripherals, and, to a lesser degree, consumer products. Some uses of bulk effect light-sensing devices are camera exposure meters, automatic light controls, counters, electric eye door openers, and industrial control applications. Junction type light-sensing devices, such as photodiodes and phototransistors, are used for punched card and tape readers in computer operations. New uses have been developed, such as end-of-tape sensors for magnetic tape applications, counters, tachometers, inspection devices, and rotatory shaft indicators. Junction type light-sensing devices in arrays are particularly useful in optical character recognition applications.

4.14 Optoelectronics

LIGHT EMITTERS

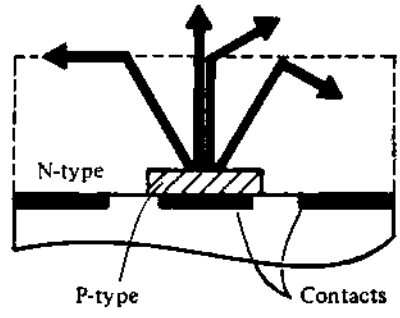
General Comments

When minority carriers recombine with majority carriers (holes and electrons) in a semiconductor, energy is released in the form of light, heat, or kinetic energy to other carriers. Any PN junction under forward bias can emit some light, but before reasonable conversion efficiences can be obtained, many factors must be optimized. For instance, light output can be severely reduced by competing nonradiative recombination processes, as well as by internal absorption and reflection losses. These losses can be minimized by choosing the proper material and by using geometrical structures and other methods to reduce absorption and reflection losses. Nonlight-producing recombination processes predominate over semiconductors, such as silicon and germanium and they are highly inefficient light emitters. On the other hand, materials such as gallium arsenide, have a high probability of radiative recombination, and consequently are used for light emitting diodes.

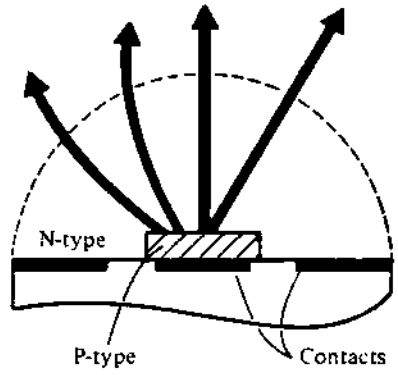
In selecting the semiconductor, the wavelength of light desired must be considered. By growing single crystal mix compounds, such as gallium arsenide phosphide and gallium aluminum arsenide, it is possible to obtain materials for the desired light wavelength by varying the composition. At present, gallium arsenide phosphide (GaAsP) diodes that emit red light are the most widely used for applications requiring visable light. Control applications where visibility is not necessary generally are filled by gallium arsenide emitting in the infrared range. New materials that have been developed are leading to reproducible manufacturing of LEDs of other colors. For example, gallium phosphide for green emission, indium gallium phosphide for yellow, and gallium nitride for blue

Figure 4.14-3

INTERNAL REFLECTION CHARACTERISTICS OF JUNCTION LIGHT EMITTERS



(a) Flat Planar Emitter



(b) High Power, High Efficiency Dome Emitter

Source: DATAQUEST, Inc.

are currently available. The predominant technique for obtaining colors is to change the proportions of arsenic and phosphorus in the GaAsP material. Appropriate doping emphasizes the desired radiation. Other possible light emitting materials are compounds from the second and sixth column of the chemical period table, such as cadmium sulphide and zinc telluride. Silicon carbide, in which yellow, blue, and green emissions have been observed, is a possible material, although it has difficult manufacturing problems.

Single Lamps

In both gallium arsenide and GaAsP diodes, light emits from the junction only. Consequently, the light appears as a thin, flat beam and the packages in which it appears are designed to produce a radiation pattern suitable for visual observation. In a simple planar junction enclosed in the flat wafer, much of the light generated is lost by internal reflection. This loss is caused by the angle at which the light is refracted as it traverses from the gallium arsenide material into the air. A typical flat device is shown in Figure 4.14-3. The light generation takes place almost entirely in the P-region and is of a slightly longer wavelength than the absorption edge of the N-type material. Light can therefore be brought out through the N-region without excessive absorption. Larger efficiencies can be achieved by doping the gallium arsenide with silicon in both the N and P regions. However, this shifts the light emitted further into the infrared.

Internal reflection can be eliminated and the light output can be increased if a hemispherical dome is placed over the junction. However, the ratio of dome-to-junction diameter is at least as great as the index of refraction of gallium arsenide to air; thus, none of the light reaching the surface will exceed the critical angle. Figure 4.14-4 shows a structure with a lens-type shape at the top which gives direction to the emitted radiation. Such a packaging scheme is useful when energy is transferred from the emitter to a small area, which occurs in a silicon detector. Lens-like structures improve the bare-chip external efficiency.

One way of improving the appearance of a visible LED is to increase the contrast. This is done on red emitters by using a red (rather than clear) plastic covering. Transmission properties of the red plastic are such that it transmits the emitted wavelength and absorbs all other visible wavelengths. Thus, the background observed by the viewer is darker than it would be with clear plastic.

An important LED packaging consideration is heat sinking. The efficiency of the devices decreases as the temperature increases. If high reliability is a consideration, then metal packages (for heat sinking) with glass lenses may be required.

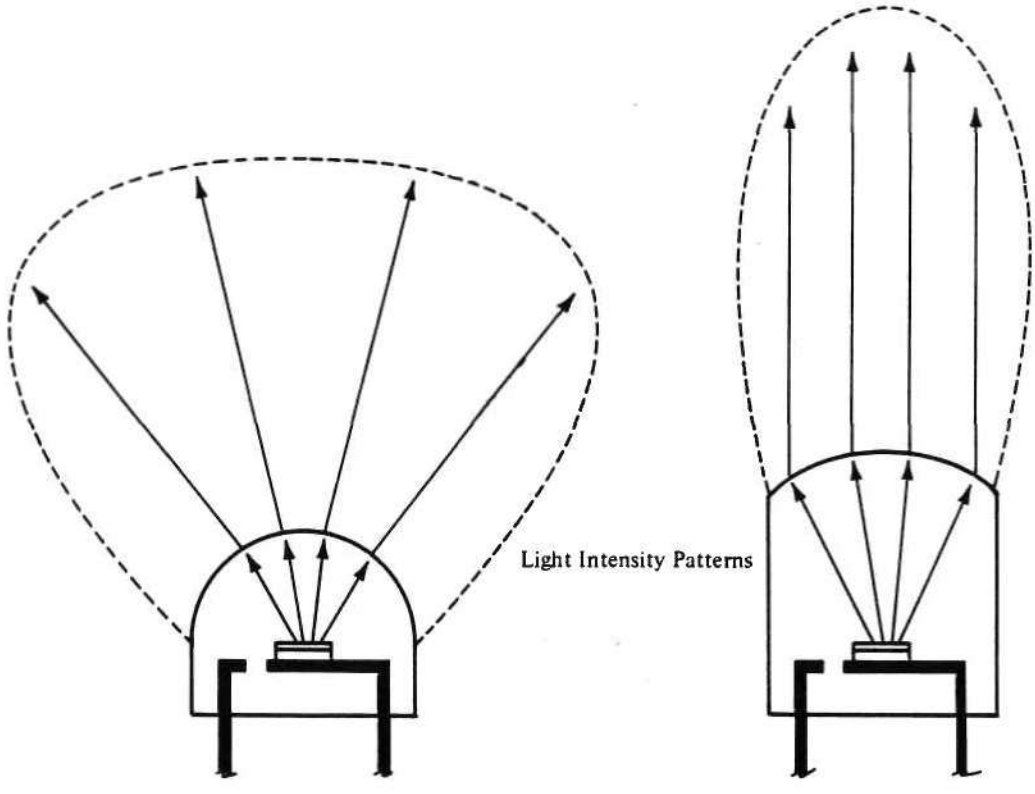
Characteristics

The diodes used for light emitting junctions are generally of small size—approximately 10 to 15 mils (0.005 inch) square. Large light sources are made by paralleling a number of like emitters which must be matched for intensity versus current distribution. Larger size light sources may also be made by placing one or two small chips on a surface and constructing a suitable sized light pipe. This technique is used in the construction of the larger display sizes.

The intensity of LEDs is low compared to that of a small tungsten filament lamp. However, as indicated above, the contrast can be increased by enclosing the LEDs in red plastic. It has also been observed that the apparent intensity to the observer is increased because the emitted light is essentially monochromatic. Some people find the red light emitted by most LEDs objectionable. This is a drawback for use in some displays.

4.14 Optoelectronics

Figure 4.14-4
DIRECTIONAL CHARACTERISTICS OF LENSES



(a) Chip with Dome Lens

(b) Focused Lens

Source: DATAQUEST, Inc.

Applications

Visible LEDs are used for lamps, digits, and displays. One of the principal uses for LEDs is as front panel lights or diagnostic lights on printed circuit boards. Here these lamps have the advantage of being able to operate from the normal integrated circuit logic power supplies.

When used in connection with LEDs, "displays" are 8 to 12 digit displays of 1/8 inch high characters generally constructed for small hand-held calculators, watches, or other instruments. These displays are constructed in hybrid or monolithic fashion with all of the digits of the display assembled on a single printed circuit or ceramic card.

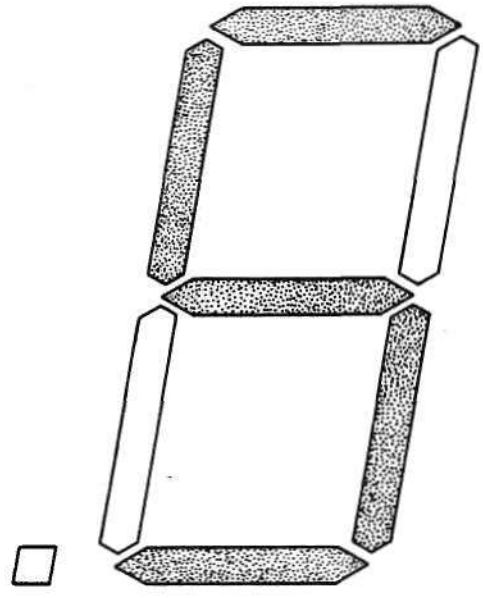
LED Displays

A digit is a single character of an alphanumeric display. Generally speaking, digits are

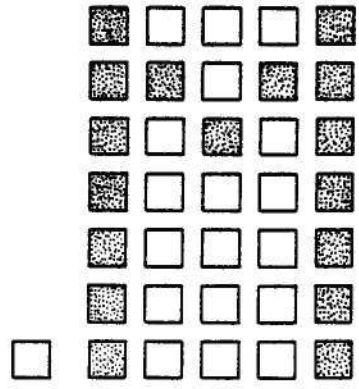
4.14 Optoelectronics

defined as characters that are larger than 1/8 inch high. A multicharacter display can be made of several digits. At present, digital displays utilizing seven-segment, figure eight-shaped characters are available up to 6/10 inch high. These larger sizes are almost always sold as individual characters. Uses include panel indications for almost every type of electronic instrumentation. They compete directly with Nixie, RCA, Numatron, and Gas Discharge devices. In hybrid construction, the digits are seven-segment plus the decimal, as shown in Figure 4.14-5. Some manufacturers have developed small monolithic seven-segment cell digits which may be constructed in a single or three digit formats. Although they are smaller than the 1/8 inch size, a magnifiying lens is used to give the appearance of 1/8 inch digits. As mentioned, these displays are generally used for hand-held calculators. However, Hewlett-Packard has introduced this approach for a hand-held probe digital voltmeter. The user can keep his eyes on both the probe element and the digital display as he checks circuit voltages. This type of display meets the major criteria of personal or portable products that have short viewing distances. An alphanumeric display, which produces the alphabet as well as numbers, generally requires a 5 x 7 matrix of emitters for each character, as shown in Figure 4.14-5. Some of the matrices are equipped with an integrated circuit decoder driver which is placed on the same hybrid substrate.

Figure 4.14-5
LIGHT EMITTING DIODE DISPLAYS



7 Segment
Numeric Display



5X7 Matrix
Alpha-Numeric Display

Source: DATAQUEST, Inc.

Infrared Emitters

Nonvisible LED devices are finding new applications in industrial as well as military/aerospace markets. Industrial uses include intrusion detectors, production line counters, scanners, level and weight controls, special shaft encoders, and alignment systems. Arrays of gallium arsenide LEDs and silicon junction photodetectors are useful in the optical reading

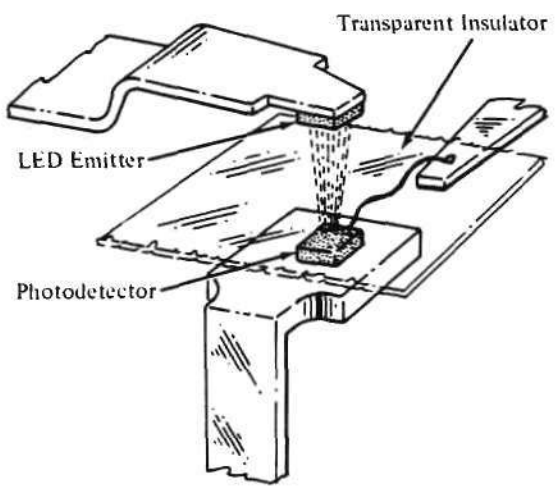
of computer tapes and cards. LEDs coupled with fiber optic bundles are foreseen as a possible replacement for some low level electrical signals and data transmission needs.

OPTICAL COUPLERS

An optical coupler consists of a light source and a light sensor mounted facing each other in an enclosed case. The case is opaque to prevent any other light from entering. These couplers are used where information needs to be transmitted between two circuits that must be electrically isolated. Such isolation was provided in the past by relays, isolation transformers, and the like.

Figure 4.14-6

EXPLODED VIEW OF AN OPTO-ISOLATOR



Source: DATAQUEST, Inc.

The input is applied to the LED terminals. The LED radiation actuates the photosensor, producing an isolated output electrical signal. The light-sensor may be a photoconductive cell, a phototransistor, or a PIN diode.

The coupling between the LED and the photosenor may be fiber optics or a small glass lens, as shown in Figure 4.14-6. The insulation resistance between the input and output terminal is typically 100,000 megaohms. The final product is enclosed in a dual in-line package configuration with the package dyed black for opaqueness.

Design engineers now use optical coupler-isolators to transfer, relay, couple, switch, or isolate electrical signals in critical circuits. They have been widely used by circuit designers, perhaps because no knowledge of optics is required for their application—all external connections are electrical. They provide almost perfect DC isolation and are much faster and more compact than the relays and transformers previously used to achieve isolation. They are used in industrial sensing and controls, feedback applications, or other applications where voltage level translations and isolation are required.

SOLID-STATE LASERS

Solid state lasers are generally made with gallium arsenide. They radiate in much the same manner as other LEDs, but are physically constructed to emit coherent light. Many technical problems currently exist, and most state-of-the-art devices will emit coherent light only at below normal temperatures. However, the problems are being solved rapidly.

LIQUID CRYSTALS

Although liquid crystals (LCDs) are not a semiconductor technology, they do form a prime competitive technology and are generally

4.14 Optoelectronics

classed as electronics. Therefore, we will consider them briefly.

Liquid crystal electro-optic effects are important because they do not require the emission of light. Instead, they modify the passage of light through the liquid crystal either by light scattering, modulation of optical density, or color changes. The displays incorporating liquid crystal technology also feature low-voltage operation, very low power dissipation, and wash-out immunity in high-brightness ambient situations. They can be made with relatively inexpensive materials and techniques in fairly large sizes, leading to the promise of large area flat displays. This section discusses the basic physical phenomena, materials, and manufacturing techniques employed with liquid crystal displays.

Physical Properties of Liquid Crystal Materials

Everyone is familiar with substances that undergo a simple transition from solid to liquid—such as the melting of ice. There are, however, many organic materials that exhibit more than a single transition in passing from solid to liquid. The molecular ordering in these intermediate phases, known as "mesophases," lies between that of a solid and isotropic liquid. Ordered fluid mesophases are commonly called "liquid crystals" In these mesophases, the molecules show some order even though the crystal lattice has been destroyed. The lack of a lattice requires that these mesophases be fluid. It is the simultaneous possession of a liquid and a solid character in a single phase that makes liquid crystals unique and creates many interesting properties.

Organic liquid crystals may be broadly classified as smectic, nematic or cholesteric. In the smectic phase, molecules are constrained to be parallel with their neighbors in layers and translational motion between these layers is of low probability. In the nematic phase, molecules are able to move in any direction with respect to their immediate neighbors, but are still constrained to be parallel with them along the "nematic director." In some materials, a twisting of the nematic director occurs from layer to layer and the resulting structure is termed cholesteric. Figure 4.14-7 illustrates these three types of ordering.

Liquid Crystal Materials

Liquid crystals used for displays are "thermotropic" because the tranistions of these mesophases are most naturally affected by changing temperature. Materials showing thermotropic liquid crystal pahses are usually organic substances with molecular structure typified by those of cholesteryl nonanoate and N-(p-methoxybensildine)-P Prime-N-butylanalyn (MBBA). Actual ratios of four to eight and molecular weights of 200 to 500 gms per mole are typical for thermotropic liquid crystal materials.

Electro-Optic Phenomena

Liquid crystal electro-optic phenomena can be divided into two categories—conduction-induced dynamic scattering and field effect.

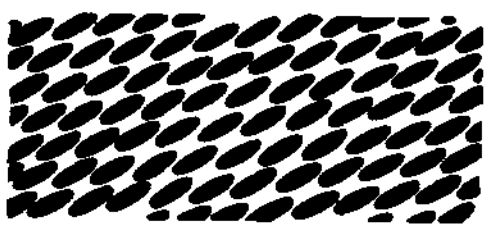
Dynamic Scattering

In some nematic materials conduction-induced fluid flow occurs during the application of an applied voltage. When the voltage exceeds a threshold value, the fluid becomes turbulent and the molecules are disordered. As a result, the light is scattered and the liquid crystals become milky white and opaque. With no applied voltage, the liquid crystals assume their crystalline alignment and are essentially transparent to light. The contrast ratio between the two states can vary greatly.

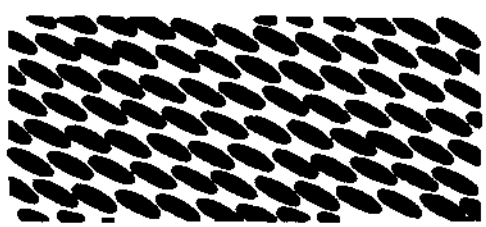
4.14 Optoelectronics

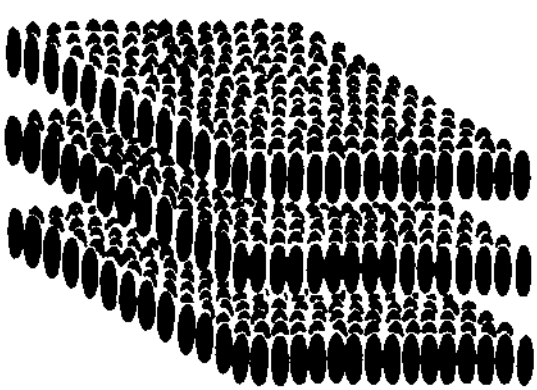
Figure 4.14-7
MOLECULAR ARRANGEMENTS OF LIQUID
AND THREE TYPES OF LIQUID CRYSTALS

Isotropic Liquid

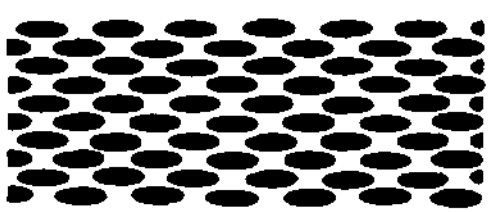


Nematic Liquid Crystal





Smectic Liquid Crystal



Cholesteric Liquid Crystal

Source: DATAQUEST, Inc.

4.14 Optoelectronics

Early displays utilizing dynamic scattering operated from direct current voltages. The lifetime of these displays was relatively short as a result of a time-dependent current variation. The failure mode was traced to the production of an insulating film on the field plates. At present, the displays are driven from AC signals rather than DC, which greatly diminishes the likelihood of failure caused by electrochemical effects. Consequently, most dynamic scattering displays are driven by AC signals. AC operating life can be greater than 10,000 hours.

Field Effect

Field effect LCD devices are proving the most popular, for both technical and other reasons. Under the presence of an electric field, the phases of a nematic liquid crystal may be deformed or twisted. With no applied field, the nematic liquid is aligned in a particular fashion and allows the light to pass through it along one alignment. When the applied voltage exceeds the threshold value, the liquid crystal distorts the light direction. A maximum rotation of 90° is possible, allowing the use of polarized light and a cross polarizer for light analysis. Depending upon the orientation of the polarizer and analyzer, a black on white or white on black display can be obtained.

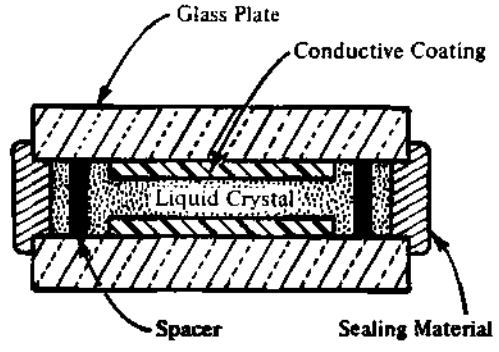
Display Construction

The standard sandwich cell configuration for liquid crystal displays is illustrated in Figure 4.14-8. Usually, low-cost soda-lime soft glass is used. However, more expensive borosilicate and fused silicate substrates can also be utilized. These cells can be made as large as a billboard and as small as a watch face. The great flexibility in size and configuration of liquid crystal displays offers a potential for a wide range of display applications.

At least one of the conductive coatings in a liquid crystal display must be transparent. The most common transparent conductive coating material is a mixture of indium oxide and tin oxide. The optical transmission of this film is excellent, transmitting from 80 to 100 percent of the light incident on the coating. Reflective coatings or electrodes are readily obtained by the evaporation of metals.

The sealing materials are limited by the need for both compatibility with the liquid crystal, and for a hermetic seal since both moisture and oxygen can react with many of the liquid crystal systems deleteriously. Other criteria for selecting sealing materials are the thermal expansion match with the glass plates, bonding strength, sealing temperature, and manufacturing cost. Glass frits, solder glasses, and polymeric materials are suitable sealing materials.

Figure 4.14-8
SIDE VIEW OF A LIQUID CRYSTAL CELL



Source: DATAQUEST, Inc.

4.14 Optoelectronics

Liquid Crystal Display Problems

Temperature Dependence

Until the resurgence in liquid crystal research in the 1960s, most of the mesomorphic materials were solid at room temperature. Today, there are many liquid crystal systems that exhibit the mesophase over a wide temperature range of around 20° centigrade. The operating temperature, however, is limited compared with other display media. Most currently available liquid crystal displays operate from about 0° centigrade (the freezing point of water) to 60° centigrade (140° Fahrenheit).

For applications, such as outdoor displays and automobile dashboard indicators, the inability to operate much below 0° centigrade will be a liability for a liquid crystal display. The prospects for finding new materials with lower operating temperatures and wider ranges are not encouraging. The practical solution is to incorporate a heating element in the liquid crystal display to keep the temperature in the operating temperature range. However, the power dissipated and the cost of the heating element eliminates the low cost advantage of crystal displays.

Operating Life

Operating life has been one of the primary concerns about liquid crystal displays. Manufacturers of these displays are currently quoting lifetimes in excess of 10,000 hours as a typical operating life for the display under AC exitation (a much lower operating life is observed under DC operation.) Although a life of 10,000 hours is an acceptable minimum for many applications, other applications will require considerably longer life—for example, 50,000 hours. Although few manufacturers have performed statistically significant life testing for more than 10,000 to 20,000 hours, the consensus in the industry is that an operational life greater than 50,000 hours is not only feasible but will be obtained in the future.

Contrast and Viewing Angle

Display brightness, or contrast, has been the major criticism of liquid crystal displays. The viewing angle affects the contrast ratio of the liquid crystal display, particularly for reflective displays where at certain angles contrast is very poor. To some extent, this problem can be overcome with a transmissive display where light is also gathered from the back and transmitted through the display. If the ambient light level is too low to allow satisfactory contrast, the transmissive display must be an auxiliary light source for back lighting. Lack of a light source has been a disadvantage for the use of liquid crystal displays where the customer feels that a lighted display is preferred. Auxiliary lighting can be provided for both reflective and transmissive displays. For these displays, some of the advantages of power consumption and size are negated by the addition of the auxiliary light source.

Applications

For the near term, there are three potentially large market areas for crystal displays:

- Watches and clocks
- Pocket size and desk calculators
- Digital panel meters

Other possible areas of digital display equipment include industrial control systems.

Applications have also been proposed for automobile displays. Dashboard indicators could well be liquid crystal displays if the economics are proven.

In the future, a potentially significant mar-

ket for liquid crystal devices could develop in graphic displays. These displays include computer terminal displays, specialized flat panel displays, commercial TV displays, and billboard and advertising displays. Each application would depend on the development of a suitable, common, and inexpensive matrix.

In addition to image displays, liquid crystals can be used to store information, and considerable work is being expended on this technology. Laboratory type situations have been constructed at Xerox and Bell Telephone Laboratories in which displays can retain their images for some period of time. However, a number of problems must be worked out before these memory displays become practical.

TECHNOLOGY TRENDS

To some extent, development in the optoelectronics industry has slowed from the exuberant period of the late 1960s. The characteristics and limitations of semiconductor LEDs are generally well recognized. Material research continues, but most efforts appear to be concentrated on developing new applications for existing materials. New mounting techniques, contrast enhancement, light leveling techniques (such as the built-in regulator) are being explored. Production capacity of existing material is being improved.

The basic advances that can be expected are:

- Increased LED brightness
- Availability of larger displays
- Larger monolithic displays
- Improved optical efficiency

All of these advances will result from step-by-step improvements rather than revolutionary breakthroughs. It can be expected that an increasing amount of integration of the LEDs, displays, and digits will occur as the manufacturers of optoelectronics seek larger markets. This integration will be directed at making the device more convenient to use. Matrix decoding, built-in light levelers, and current regulators are only a few of the potential combinations that will be explored.

Widespread use of liquid crystal displays will await improvements in material technology as well as consumer acceptance. Many companies once thought to be leaders of liquid crystal technology have curtailed their activity. A revolutionary breakthrough in technology may be required for complete acceptance of LCD displays.

4.15 Microwave Semiconductors

GENERAL COMMENTS

Microwave applications are one of the oldest uses of semiconductors. Microwave point contact diodes have been manufactured for nearly 40 years. Many special semiconductor devices have been developed for microwave electronics usage. This section discusses their construction and a few of their special uses.

Transit time effects are the basic difficulty with electronic devices operating at microwave frequencies—i.e., greater than one GHz (1 billion hertz). At these frequencies, the time taken for a carrier, such as an electron or hole, to traverse the required distance is comparable with the period of the signal frequency.

Microwave transistors have become more widely used in the past ten years as they have become competitive with other techniques performing amplification at microwave frequencies. In general, microwave transistors are divided into two categories—low noise or power—depending on their ultimate use.

Most of these devices are two-terminal devices generally classified as diodes. Some of the diodes, such as the tunnel diode, utilize special junction effects, based on particular physical properties.

Hybrid microwave integrated circuits (MICs) are one of the primary reasons for advanced uses of semiconductor microwave devices. The use of hybrid circuit technology eliminates many of the electrical parasitic elements that occur with packaged semiconductors. Full advantage of the capabilities of the semiconductor devices can be taken by utilizing MIC techniques.

MICROWAVE DIODES

Detectors

Point Contact Diodes

Point contact diodes were the earliest semiconductor devices. Many people remember the cat's whisker employed in a crystal radio. This technique was employed in the construction of mixer and detector diodes used in early radars and is still used for some diode construction. Figure 4.15-1 is a sketch of the construction of a point contact diode. A specially formed tungsten "whisker," the point of which is formed by electrolytic etching, is attached to the cap of the package. The whisker is held onto the semiconductor slab using the resultant spring action.

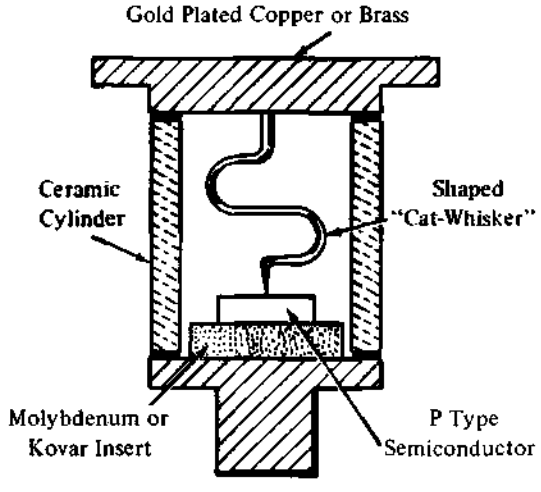
Although modern point contact diodes employ nearly the same technology used in their early development, some point contact diodes are constructed in glass diode packages similar to the one detailed earlier for PN junction diodes (see Figure 4.12-3). Circuit application of these devices at microwave frequencies must take into account package capacitances and the inductance of the whisker. For this reason, it has been difficult to replace diodes in existing circuits and replacement devices must be made in nearly the same manner as the original to reproduce the circuit performance.

Schottky Barrier Diodes

Modern technology has made possible the form of metal-semiconductor barrier diodes which were first theorized by Schottky in the early 1930s. The characteristics of these devices are determined by the purity of the semiconductor and metal employed. Refractory metals such as platinum or molybdenum are often

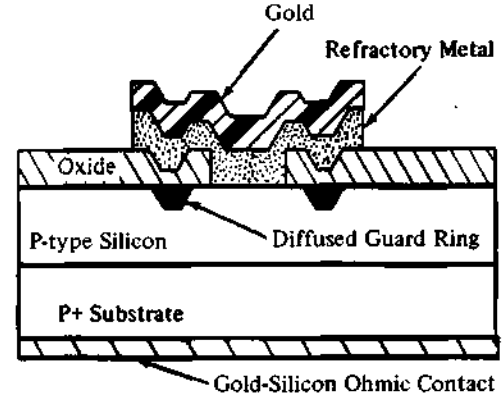
4.15 Microwave Semiconductors

Figure 4.15-1
POINT CONTACT
DIODE CONSTRUCTION



Source: DATAQUEST, Inc.

Figure 4.15-2
SCHOTTKY BARRIER
DIODE CONSTRUCTION



Source: DATAQUEST, Inc.

used for the barrier metal with a gold bonding contact. In nearly all cases, the semiconductor material is silicon because of its highly developed processing technology. Figure 4.15-2 shows the construction of a Schottky barrier diode. The "guard ring" diffusion may not be needed unless a high reverse voltage is required.

The thickness and impurity doping of the P-type layer is extremely important in the construction of Schottky barrier diodes. The overlap of material beyond the desired active region is also important because it causes undesired capacitance. The advantage of a Schottky diode in high-frequency use is that electrons injected from the semiconductor into the metal "disappear" instantaneously. Thus, the device can be switched off very fast.

Schottky barrier diodes can be made in matched sets by dicing the semiconductor wafer in pairs or quads so that they may be packaged for use in bridge-type circuits. Another technique utilizes beam leads for factory connection. This package construction is useful in the development of high-frequency mixer technology because it provides more uniform product characteristics.

Control Diodes

PIN Diodes

In a PIN diode, the semiconductor wafer has a heavily doped P region and a heavily doped N region separated by a layer of high-resistivity material that is nearly intrinsic (I). The thickness of the high-resistivity layer lies in

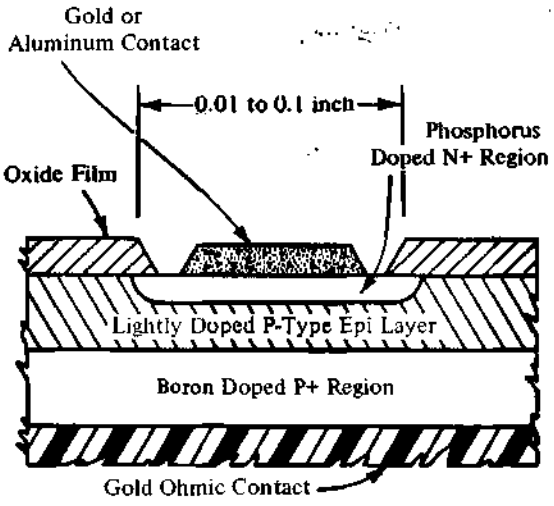
the range between 1/4 and 8 mills. Electrical contact is made to the two heavily doped regions.

The PIN diode was first proposed as a low-frequency power rectifier. Although it becomes a poor rectifier at frequencies above a few megahertz, it can be used for other purposes at microwave frequencies. Under zero or reverse bias, the diode has a very high impedance at microwave frequencies, whereas at moderate forward current it has a very low impedance. This situation permits the use of the PIN diode as a switch in a microwave transmission line. Since the R-F resistance of a PIN diode can be varied continuously from large to small values by changing the diode's bias, it can also be used as a variable attenuator. Finally, a microwave signal can be amplitude-modulated (up to a few megahertz) by shunting a transmission line carrying the microwave signal with a PIN diode and varying the diode forward bias in accordance with the desired modulation.

Figure 4.15-3 shows the details of a PIN diode construction, and Figure 4.15-4 shows a typical mounting in a microwave "pill" package. Packaging of diodes at microwave frequencies is extremely important. The pill package has been designed for high thermal conductivity and low electrical capacitance and inductance parasitics.

Figure 4.15-3

TYPICAL PLANAR MICROWAVE PIN DIODE



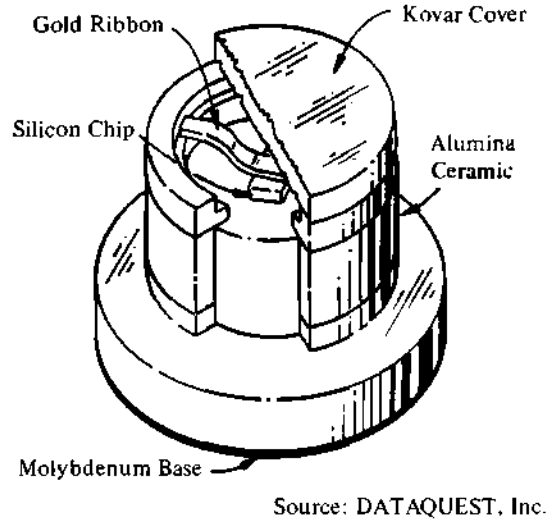
Source: DATAQUEST, Inc.

Step Recovery Diodes

A step recovery diode (snap-back diode) is a special type of PIN diode. In this structure, the intrinsic (I) region is made extremely small and the junction gradients are made very large. This approach allows control of the charge stored in the junction when the device is forward biased. When a device is reverse biased, capacitance is essentially constant. The device can be used to control a current fairly rapidly—a characteristic needed for multiplier circuits. In

Figure 4.15-4

TYPICAL PIN DIODE MOUNTING IN A MICROWAVE "PILL" PACKAGE



Source: DATAQUEST, Inc.

4.15 Microwave Semiconductors

this manner, it is operated essentially the same as a varactor diode (which is explained later).

Step recovery diodes are packaged in a similar manner to the PIN diode pictured in Figure 4.15-4. To ensure that there is no deleterious effect of parasitic capacitance by the package, many circuit designers use beam-leaded devices. The beams can be placed directly on the strip line conductor of a circuit.

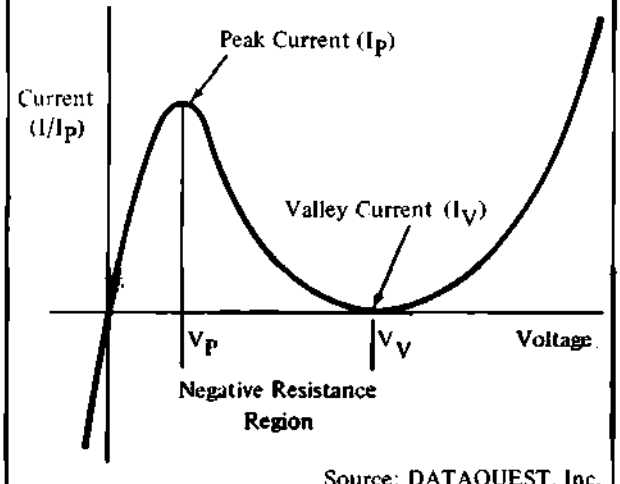
Amplifier Diodes

Tunnel Diodes

A tunnel diode, or Esaki diode, is a PN junction device with extremely heavy doping on both sides of the junction. If the transistion from the P side to the N side is sufficiently abrupt, electrons can "tunnel" through the potential energy barrier at the junction by quantum mechanical means. This tunneling occurs at very low reverse voltages and results in an unusual current-voltage characteristic, as shown in Figure 4.15-5. The device exhibits a negative resistance over part of the forward voltage characteristic and has a large current flow at relatively small reverse voltages. Because the tunneling phenomenon is a majority-carrier effect, it is very fast, enabling the construction of useful devices to very high frequencies.

The tunnel diode has received more interest than acceptance in the microwave semiconductor field. In theory, it has promised medium noise amplifiers, low-noise converters, and low-cost oscillators. In practice, these circuits have never achieved high volume usage, primarily because of their low power handling capability. Tunnel-diode amplifiers overload at inconveniently low power levels, and oscillators based on them have insufficient output power to be of practical use.

Figure 4.15-5
TUNNEL DIODE CURRENT-VOLTAGE CHARACTERISTIC



Source: DATAQUEST, Inc.

Varactor Diodes

The varactor diode is a semiconductor device used as a variable reactance element—i.e., its capacitance varies with applied voltage. The varactor is basically a non-linear circuit element that is used in four different ways:

- Switching of microwave signals by changing the varactors reactance
- Generation of harmonics of the applied microwave signal (a multiplier)
- Parametric amplification of a microwave signal
- Conversion of a microwave signal to a higher frequency

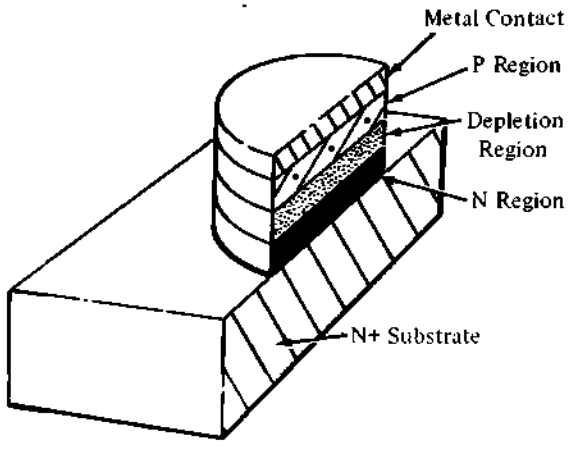
The particular use of the varactor diode is determined by the circuit in which it is employed.

4.15 Microwave Semiconductors

Varactor diodes are made in much the same manner as other semiconductor components, often using "mesa" techniques as shown in Figure 4.15-6. Strict controls are imposed during fabrication to maintain junction capacitance and material resistance tolerances. As in all microwave devices, the package contributes to the electrical parameters, and thus packaging is critical. Varactor diodes are often made in beam-lead form to improve device parasitics. The best varactor diodes are constructed with gallium arsenide material. The process is difficult and hand tailored--resulting in devices that can sell for up to $100. Lower cost varactors, used for most applications, are made of silicon.

Figure 4.15-6

CROSS SECTION OF A TYPICAL MESA VARACTOR DIODE



Source: DATAQUEST, Inc.

Power Conversion Diodes

Gunn Effect Devices

In 1963, J.B. Gunn discovered that a DC voltage applied to the ohmic contacts on the ends of a rectangular bar of N-type gallium arsenide or indium phosphide caused oscillations when voltage exceeded a threshold value. The period of the oscillations observed was close to the transit time of the carriers between the contacts. Experiments revealed that these microwave oscillations were associated with the transit of a moving dipole layer of charge across the device. This is called a "high field domain." This effect was determined to be caused by bulk negative resistance in gallium arsenide which results from field-dependent carriers exitated to a normally unoccupied low-mobility conduction band from a high-mobility band.

This new phenomenon attracted widespread interest, both as a new area for stimulating research and because of its potential usefulness in new solid-state devices. Since the discovery, bulk negative resistance effect devices have been applied to the construction of microwave solid-state oscillators and amplifiers.

The semiconductor materials used for these devices are either bulk-grown or epitaxially grown N-type gallium arsenide. Although the microwave oscillation and amplification are inherently bulk phenomena, the electrical contacts play an important role. It has been determined that the high field domains are nucleated near the cathode; thus, the doping profile near the cathode greatly affects the device characteristics. To achieve suitable oscillation coherency and reasonable frequency, the interface between the contacts and the N-type gallium arsenide must be a well-defined plane, and the cathode and anode must be reasonably parallel to provide a uniform field throughout the entire cross-section near the cathode.

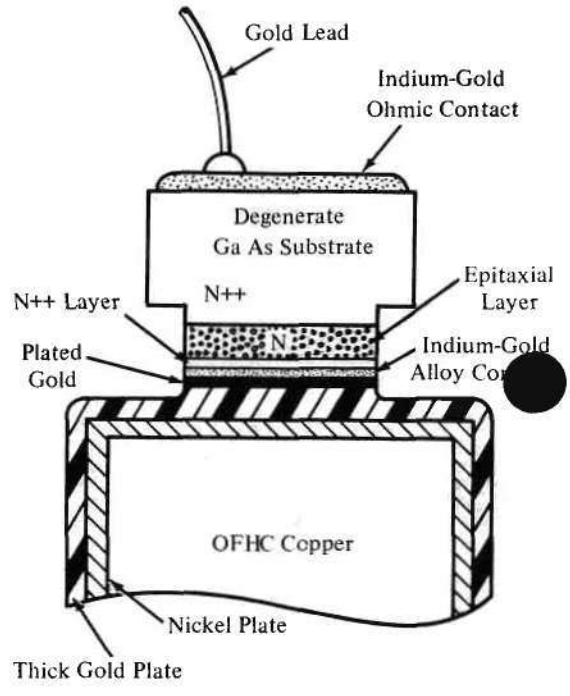
4.15 Microwave Semiconductors

Bulk effect devices often operate at continuous power with dissipation densities as high as 20 billion watts per cubic centimeter. This necessitates mounting the device in a package with extremely low thermal resistance. Mounting must be done carefully to prevent voids between the device and the package. Figure 4.15-7 shows the common technique of flip chip (named because the chip is upside down from the normal position) mounting of the bulk effect device to remove the heat from the near active area. The device is actually thermal compression bonded to its gold contact and the gold plating on the oxygen-free high conductivity (OFHC) heat sink post. The heat sink may be part of a microwave "pill" package or may be a post that allows the device to be mounted directly in a waveguide circuit.

The normal powers and efficiencies lead to the use of bulk effect devices from frequencies of 6 GHz to approximately 40 GHz. The most common use is as single frequency oscillators for receiver local oscillators. Bulk effect devices have been combined with YIG (Yttrium Iron Garnet) tuned circuits for use as sweeping microwave oscillators. Bulk effect devices have been utilized as negative resistance amplifiers in the microwave region above 5 GHz where alternative solid-state approaches do not have sufficient power. The electrical noise characteristics of the Gunn effect device are superior to those of the IMPATT device described in the next section.

Figure 4.15-7

BULK EFFECT DEVICE FLIP MOUNTED ON A COPPER HEAT SINK STUD



Source: DATAQUEST, Inc.

IMPATT Diodes

In 1965, workers at the Bell Telephone Laboratories observed that microwave oscillations could be obtained from reverse biased PN junctions. Additional work has clarified the type of oscillations that were observed and optimized the structures for obtaining these oscillations. These devices are diode-like structures operated near the avalanche breakdown voltage. The oscillations are a function of the transit time across the depleted region of the junction. Carriers are injected during a part of the oscillation cycle, breaking over the avalanche breakdown condition. The term IMPATT is an acronym for IMPact Avalance and Transit Time which describes the operation of these diodes.

The general structures used are either a PIN structure or a modified structure such as PNIN, as shown in Figure 4.15-8. One

junctions is biased at nearly avalanched condition. In the PNIN structure, this junction would be the PN junction. When a small part of the AC signal causes the diode to avalanche, carriers are injected across the PN function and are swept across the depleted intrinsic layer by the electric field. The transit time required for the carriers to be taken across this layer determines the frequency of oscillation. Thus, the length of the intrinsic region is critical in design of the device.

These devices have been successfully used as medium power (10s of watts) oscillators in the lower microwave frequency regions and low power (10s of milliwatts) oscillators in the higher microwave (millimeter wavelength) regions of the spectrum.

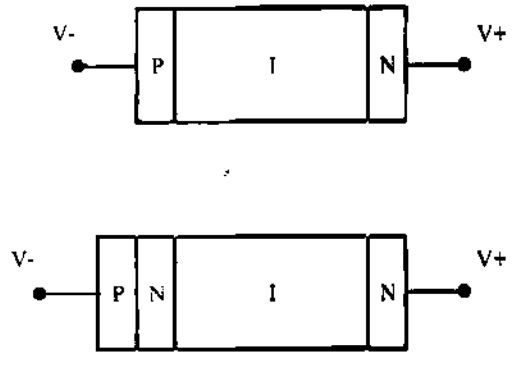
IMPATT devices generate more electrical noise than do Gunn effect devices. Thus they are less useful for local oscillator type applications. However, IMPATT oscillators can be less noisy than a klystron tube that is close to the carrier frequency. This feature is important in systems such as Doppler radar which need a narrow bandwidth source. The IMPATT oscillator noise is also important when the device is used as a source or "pump" for parametric amplifiers.

In addition to the work done in silicon, IMPATT operation in gallium arsenide and germanium diodes have been reported. Both materials show a markedly lower electrical noise performance than is true of silicon devices. The silicon units, however, continue to show the highest power output capabilities.

As with bulk effect devices, thermal considerations in packaging IMPATT diodes are paramount. The techniques of "flip chip mounting" shown for the bulk effect devices (Figure 4.15-7) are also used for IMPATT diodes. When properly mounted, IMPATT devices are the most powerful solid-state sources yet discovered for prime high-frequency microwave signals.

Figure 4.15-8

PIN AND PNIN STRUCTURES USED FOR IMPATT DEVICES



Source: DATAQUEST, Inc.

MICROWAVE TRANSISTORS

General

The design and successful fabrication of microwave transistors is postulated on the careful manipulation of design parameters to achieve useful microwave performance within the constraints imposed by the fundamental limitations that apply to transistors. As the operating frequency approaches the microwave region (1 GHz), factors that are insignificant or of minor importance at lower frequencies assume increasingly major roles. To achieve microwave capability in active regions of the transistors, the dimensions of these regions in the semiconductor must be shrunk to exceedingly small values, and this must be accompanied by extremely low wafer and package parasitic electrical characteristics. Furthermore, even in the

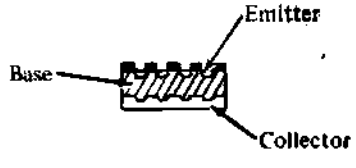
4.15 Microwave Semiconductors

presence of satisfactory microwave performance capability, the proper impedance transformations must be provided to derive useful circuit performance. Figure 4.15-9 compares the size of a microwave transistor cross-section with a 7400 series TTL IC.

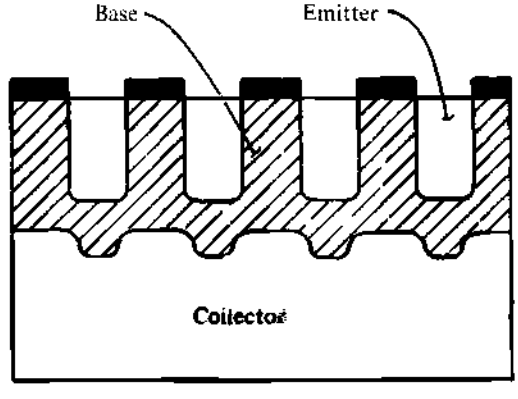
In general, a microwave transistor is designed by extending the technology on several fronts simultaneously. Diffusion, photoengraving, thin-film metallization, etching, and assembly operations are all pushed to the limits of capability to make active regions of the device as small as possible. Specially designed packages are required. Characterization of the device is difficult in a frequency range where well-developed test techniques have only recently become available.

Figure 4.15-9

RELATIVE DIMENSIONS FOR A MICROWAVE TRANSISTOR AND A 7400 SERIES IC



Microwave Transistor



Typical 7400 Series TTL IC

Source: DATAQUEST, Inc.

The material used in most microwave transistors today is silicon. Although germanium and gallium arsenide have theoretically better performance parameters, the advantage of silicon lies in its well-developed process technology. A technology recently available for transistors employs the use of gallium arsenide in a field effect configuration. These so-called "GaAs FETs" appear to offer capabilities that will allow solid-state amplification and oscillation for frequencies of up to 20 GHz.

In general, microwave transistors have two major segments depending upon their application—low-noise and high-power.

Low Noise Transistors

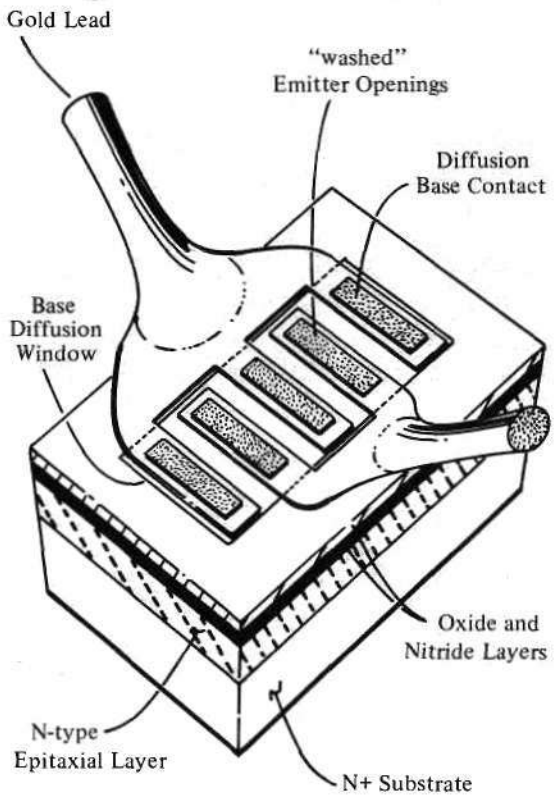
Bipolar

Although field effect transistors are used for low-noise amplification in the UHF region, the bipolar transistor is the device predominantly used for low-noise amplification in the microwave frequency region. Until 1968, germanium bipolar transistors had a performance advantage as a result of superior material characteristics. Since that time the improved process technologies employed on NPN silicon transistors have made the germanium device obsolete. Low-noise microwave transistors employ interdigitated geometry exclusively (like two hands woven together), as shown in Figure 4.15-10. This transistor structure can be thought of as several transistors acting in parallel. The emitters are made narrow and short to eliminate undesirable effects at high-frequencies.

The performance of bipolar microwave

4.15 Microwave Semiconductors

Figure 4.15-10
SMALL SIGNAL INTERDIGITATED MICROWAVE TRANSISTOR



Source: DATAQUEST, Inc.

transistors has improved steadily in the past ten years. The "noise figure"—a figure of merit measuring unwanted electrical noise—has decreased over time, as shown in Figure 4.15-11. Lower frequency performance has recently reached a plateau. The improvement at 4 GHz has also slowed as a result of the development of the gallium arsenide FET devices which show improved performance with less difficult processing. Some improvement of higher frequency performance can be expected as electron beam photolithography technology becomes more prevalent.

Gallium Arsenide FET

The latest device developed for microwave frequency amplification is the gallium arsenide FET. This device utilizes the intrinsic properties of gallium arsenide material to achieve high-frequency operation. The basic structure of the device is shown in Figure 4.15-12. Extremely thin gate lines for Schottky barrier contact are made on a thin epitaxial N layer grown on a semi-insulating substrate. This substrate is oxygen-doped to make it almost an insulator. In general, the gate structure is only one micron long (the length of the gate is the dimension between the source and drain). The source and drain contacts are gold germanium alloy to provide ohmic contact to the N-type gallium arsenide. A small mesa is etched for the active device, allowing the gate bonding pad to be placed on the substrate, and thus lowering parasitic capacitances and improving overall high-frequency performance.

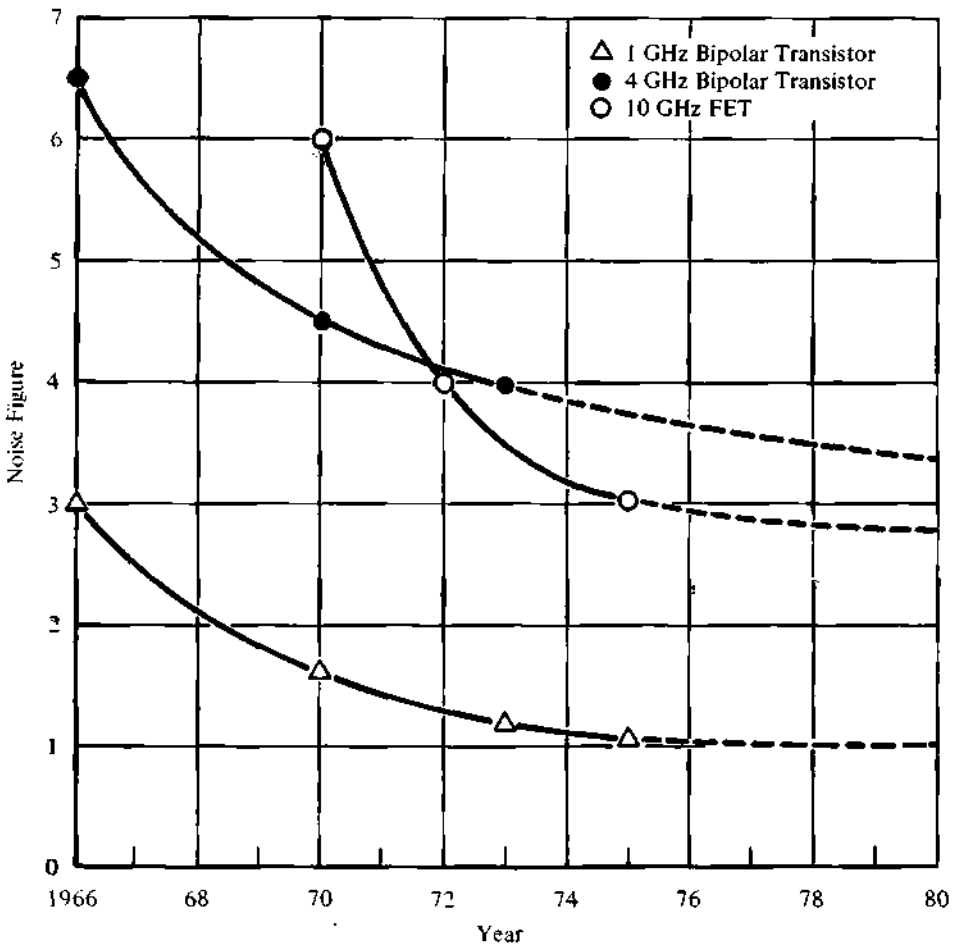
Gallium arsenide FETs are just emerging from the laboratory. Only a few companies have devices available on a production basis. Amplifiers made with these devices have been delivered with performance superior to low-noise traveling wave tubes at frequencies up to 12.4 GHz, and wideband oscillators have been constructed with these devices at frequencies in the 10 GHz region. New devices appearing on the market promise useful amplification at frequencies up to nearly 20 GHz. The performance cross-over between bipolar low-noise transistors and gallium arsenide FET transistors appears to be around 5 GHz.

Power Transistors

Microwave power transistors are not merely enlarged microwave small signal tran-

4.15 Microwave Semiconductors

Figure 4.15-11
MICROWAVE TRANSISTOR NOISE FIGURE

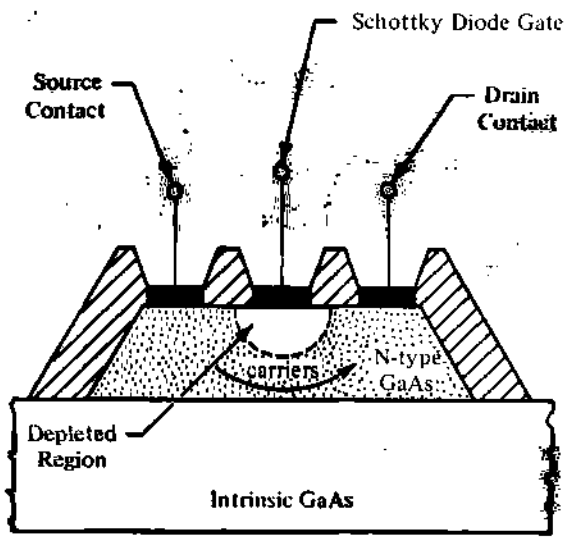


Source: DATAQUEST, Inc.

4.15 Microwave Semiconductors

Figure 4.15-12

GALLIUM ARSENIDE FIELD EFFECT TRANSISTOR



Source: DATAQUEST, Inc.

sistors. Special considerations must be taken to enable the higher power capability. Emitters must be "ballasted"—i.e., a small resistor is in series with each emitter "finger"—and packaging needs for severe thermal and electrical requirements must be met.

The basic goal of the microwave power transistor designer is to pack a very long emitter into a small area collector-base junction. Three technologies have been evolved to accomplish this goal—the mesh or matrix, the overlay, and the interdigitated structure. These terms refer to the different geometrical arrangements used. Although each structure has some advantages over the others, it appears that none has fundamental superiority. The preference of the designer depends on the type of process controls that a particular manufacturer has developed. All three methods use silicon epitaxial diffused structures.

The performance of a microwave silicon transistor is very much a function of the pack-

age in which it is placed. Microwave transistor packages must have good thermal conduction pads combined with electrical isolation. Beryllia, a ceramic material with high thermal conductivity and low electrical conductivity, is used extensively. Innovative designs are employed to reduce unwanted wire lengths and minimize parallel parasitic capacitances.

At present silicon microwave power transistors are available with 50 to 100 watt capabilities at one GHz, dropping to 5 to 10 watts at four GHz. Using electron beam photolithographic technologies, Texas Instruments has reported development of a device with capability of one watt to 10 GHz with reasonable power gain. Other laboratories have reported that with power GaAs FETs one-half to one watt has been obtained in the 10 GHz region. Although the frontier of microwave power transistors is generally established by higher powers at higher frequencies, development work in recent years has been directed toward lower frequencies to obtain higher power efficiencies and higher amplification (for a given power). Improved diffusion technologies and higher resolution photoengraving techniques are employed with close process control to achieve these results.

MICROWAVE INTEGRATED CIRCUITS (MIC)

Integration of microwave circuits has come to mean the techniques used to incorporate solid-state devices into microwave circuitry. The amount of integration technology applied to a particular circuit depends on its function. Overall performance, reliability, potential usage, cost, and size are a few of the factors considered in determining which integrated techniques should be applied.

Types of Microwave Integrated Circuits

Three levels of integration are considered in Table 4.15-1. The highest order of integration shown is monolithic construction; this technique uses the same substrate structure for both active and passive circuit components. Although circuits manufactured in this manner have engineering advantages in terms of reproducibility, production cost, and potential reliability, the difficulties encountered in their development have prevented their widespread use. However, a varied catalog of surface-oriented devices—including PIN diodes, Schottky-barrier diodes, transistors, and Gunn oscillators—has been developed for use in monolithic microwave circuits. Under separate evaluation, these units have shown acceptable performance, but problems such as surface inversion layers and substrate conductivity modulation have prevented the circuits fabricated with these devices from reaching their full performance potential.

The second level of integration, termed Hybrid I, incorporates the passive circuit elements such as capacitors and resistors onto a transmission line substrate. Active devices are connected to the circuit after the completion of the component-forming operations. Many techniques may be used to make the components on the substrate. These approaches include vacuum thin-film deposition and a subsequent photographic definition to build the hybrid circuits. This approach allows flexibility of design since the process steps may be applicable to many circuits simultaneously, thus allowing batch fabrication and control even during the development cycle. These techniques have also been used to make passive components, i.e., filters, signal couplers, and similar circuits.

Four general techniques for attaching the devices to the hybrid circuit substrate are employed. Transistor and diode die attaching has been accomplished by use of the conventional

4.15 Microwave Semiconductors

Table 4.15-1
MIC INTEGRATION TECHNIQUES

Type of Integration	COMPONENTS: Deposited or Formed in or on a Common Substrate	COMPONENTS: Bonded or Attached to a Common Substrate
Monolithic	All components	None
Hybrid I	Transmission lines and all passive components	Semiconductor devices
Hybrid II	Transmission lines and some passive components	Semiconductor devices and remainder of passive components

Source: DATAQUEST, Inc.

alloy and wire bond procedures. Special tooling has been developed that allows selective heating of the substrate in the region of the device attachment only to avoid destructive heating of the thin-film components. Devices requiring low thermal impedance paths are mounted first on carrier packages made of beryllium. These devices can be inserted into the circuits in holes or in spaces in the proper position either by raised pads or by use of beam leads. Beam lead components are now available for PIN diodes, varactor diodes, mixer diodes, capacitors, and thyristors.

The third level of integration, Hybrid II, employs hybrid construction for the transmission lines only. All active devices and resistors and capacitors are attached by techniques that have been discussed above. In this approach, the metallization for the transmission lines may be fabricated by thin or thick film hybrid microcircuit construction.

Applying the integration criteria to various pieces of a microwave system may dictate different integration approaches to the individual circuits. Monolithic construction has been applied with limited success to a few microwave functions such as switches and mixers and is not used commercially. The hybrid construction types have been applied to a much wider variety of circuits with success. Many mixed hybrid construction circuits have been packaged together into microwave subsystems, such as broad band amplifiers, phase shifters, oscillators, and transceivers.

MIC Technology Trends

Technology growth in microwave integrated circuits has definitely slowed in the past five years. The major new revolutionary technology is the employment of GaAs FETs for higher frequency low-noise amplifiers. It is expected within the next year or two these amplifiers will be available, reaching 18 to 20 GHz capability with low-noise figures. One of the primary advantages of MIC use at microwave frequencies is likely to be the achievement of wider frequency band performance stretching over several decades of bandwidth. Low-noise mixers which use beam lead Schottky barrier diodes formed in pairs or quads are another wideband component. These wideband components will continue to develop slowly, showing performances over decade or double decade bandwidths in the near future.

There will most likely be an increasing use of MIC techniques for subassemblies employing more than one microwave component. A microwave component consists of an assembly with one function, such as an amplifier, switch, mixer, etc. These MIC subassemblies will generally be used for receiving applications; however, use of power transistors in the lower microwave region allows construction of complete transceivers (transmitter-receivers).

The increasing use of MIC technology has

4.16 Impact of Technological Change

TIME LAG BETWEEN TECHNOLOGY AND PRODUCTION

Although new technologies and products have evolved rapidly in the semiconductor industry, a significant time lag nevertheless may exist between the inception of an idea and its successful implementation into manufacturing. The duration of this lag varies and is difficult to predict. Moreover, many highly heralded products and ideas never become commercial successes.

As an example of this time lag, the principle of field effect modulation used in MOS devices was patented in 1935, more than 25 years before the first commercial MOS transistor was available in 1963, and the complete theory of operation was described by Shockley in 1954. In this case, the idea was far in advance of the technology available. Significant discoveries and advancements had to occur before the device could be manufactured. Similarly, CMOS circuits, ion implantation, and automated film bonding have all had long gestation periods.

A widely acclaimed technological achievement was the development of the tunnel diode in 1958. The advantages of this device included very high frequency response, negative resistance (current decreases with increasing voltage over part of the voltage range) at low power dissipation, and insensitivity of its electrical characteristics to temperature. More than 15 years later, however, commercial application of tunnel diodes is minimal; it is used primarily as a research tool to study semiconductor properties. Other examples include beam lead devices, unijunction transistors, and junction field effect transistors. All of these were expected to have much larger markets than they currently have.

Processes such as electron beam masking and device processes such as I^2L circuits are examples of technologies with potential for success that are in their early formative stages.

Many semiconductor firms have announced product concepts long before they become production realities. In many instances, the time lag results from problems of transferring a technology from the R&D stage to production, while incorporating it into a suitable product. A process developed during the R&D phase is usually executed with great care by highly trained engineers, scientists, and technicians. Wafers are processed in small batches with great care and very little time pressure. Moreover, the process equipment is usually substantially different from that used in the manufacturing area—smaller (since fewer are processed), older (many are relics disposed of by the production area), and "hand-tweaked" to perform a process.

The process developed under these constraints is usually not production-oriented, and its weaknesses become evident as volume increases and less sophisticated personnel attempt to work with it. Consequently, the yields realized in the R&D phase always fall dramatically when a process and product are transferred to production. The loss in time may be only a few months, but typically has been a year or more in the semiconductor industry. This lag may be several years if other technical improvements need to be made to fully implement the process or product and make it economically feasible. By that time, other approaches may be more attractive. Many processes and products never make the transition from research and development to production.

Once a technology becomes established, several years may be required until it becomes a major market force. This is due to the time required for devices to be designed and implemented into electronic equipment, and for that electronic equipment to be accepted in the market.

4.16 Impact of Technological Change

DISPLACEMENT EFFECT

The remarkable growth and evolution of the semiconductor industry has resulted largely from both the development of new markets, and the displacement of other technologies. For example, the use of transistors instead of vacuum tubes has had a major impact on the manufacture of radios. The transistor displaced vacuum tubes in virtually every new radio design. Low power transistors allowed the manufacture of small, portable, battery-powered radios for the first time. The following discussion considers some examples of the displacement effect with respect to both nonsemiconductor and semicondcutor technologies.

Nonsemiconductor Technologies

Electromechanical

There are a number of notable examples of the displacement effect of semiconductors on electromechanical equipment. One of the most evident today is the electronic calculator. In the early 1960s, all adding and calculating machines were electromechanical. The more the capability of the machine, the more cumbersome it was likely to be.

The electronic calculator, first introduced in 1966, brought compactness, portability, lower power dissipation, and more complex calculating power to a world dominated by the four-function electromechanical machines. Continued advancements allowed all four functions to be integrated onto one MOS chip, costing less than $5.00 by 1970. Electromechanical machines were quickly displaced and a new breed of calculators, the hand-held calculator, was born.

Magnetic Memories

Magnetic cores have long been the dominant memory technology for information storage. The replacement of magnetic core memories has been much slower than originally projected because of the size and cost reductions achieved by core manufacturers. Momentum is gaining, however, as higher performance, higher density semiconductor memories reach the marketplace at competitive prices.

Single package 4096 bit (4K) RAMs, operating at almost twice the speed of core, are now priced at less than 0.2 cents per bit. Within a year, the price should drop to 0.1 cent per bit and be out of reach of core competition. By 1980, core is expected to represent only 4 percent of the memory market compared with the 50 percent it is believed to have had in 1975.

Semiconductor Technologies

Although the semiconductor industry has been able to generate new markets by displacing nonsemiconductor technologies, displacement also occurs among semiconductor products. Newer bipolar and MOS processes rapidly outdate existing devices by providing cheaper or higher performance circuit functions or both.

Product Displacement

One displacement that is currently occurring has resulted from the development of microprocessors. A number of MOS and bipolar microprocessor sets (of about 1 to 15 packages) are now available from semiconductor manufacturers. Depending on the application, from 30 to 300 standard TTL packages may be displaced by each microprocessor set. With microprocessor sales expected to grow to 10 million units by 1980, 300 million to 3 billion potential

4.16 Impact of Technological Change

TTL packages may be replaced.

MOS Versus Bipolar Technology

Until recently, MOS and Bipolar technologies have had relatively little impact on each other. Bipolar technology has concetrated on high speed, relatively high power dissipation (compared with MOS), and medium component density. MOS, on the other hand, has found its niche in medium speed, medium (P and NMOS) and low (CMOS) power dissipation, and high component density. For example, the largest bipolar RAMs are 1,024 bits, operate at speeds of less than 50 nanoseconds, and consume up to 600 milliwatts of power. On the other hand, the largest N-channel MOS RAMs have 4,096 bits, operate at 200 to 300 nanoseconds, and consume 300 to 400 milliwatts.

The advent of bipolar I^2L techniques, however, has brought a new variable into the equation I^2L offers power dissipation, component density, and speeds comparable with N-channel silicon gate MOS. If the design and manufacturing problems are successfully resolved, bipolar and MOS could be in serious competition for the first time.

Displacement Within Technology

As indicated previously, a considerable amount of displacement takes place even within the bipolar and MOS technologies. RTL was displaced by DTL in less than two years and, within the next two years, TTL became the dominant family. MOS has progressed through similar iterations, beginning with metal gate, high threshold P-channel in 1973.

These displacements have occurred because the newer products and processes demonstrated improved performance capabilities, lower costs, or both. Thus, products and technologies in the semiconductor industry exhibit limited lifetimes. Companies must adapt to changes or lose their competitiveness. Unfortunately, many products are often displaced before an adequate return is realized on the investments made to develop them.

HISTORICAL TRENDS

Technological milestones that have occurred in the past are summarized in Table 4.16-1, which shows the year a technology was developed, the pioneering company, and gives pertinent comments on current status. This table shows the constant evolution of semiconductor technology.

The pioneering company is not necessarily the company that was successful with the technology despite introducing the first commercial devices. Four pioneering companies, (Westinghouse, Sylvania, General Microelectronics, and Cogar) are no longer in the IC business. A fifth, Inselek, is currently operating under Chapter XI. Texas Instruments has been the most successful company in retaining a position of leadership in the technology it pioneered, with much of its successes derived from its development of silicon transistors and iterations of the TTL technology.

RCA began its efforts in CMOS in the early 1960s and announced its 4000 series in 1968. Having generated the market and having been virtually the sole source of CMOS logic circuits for many years, RCA has placed itself in a strong leadership position.

Motorola followed much the same path as RCA in developing the ECL products and market. It also maintains the leadership in the technology it pioneered, although the expected ECL volume will be far less than that of CMOS.

The latest company that is still the leader in the technology it pioneered is Intel, with its N-channel silicon gate products.

4.16 Impact of Technological Change

Table 4.16-1
SEMICONDUCTOR INDUSTRY MILESTONES

Year	Technological Advance	Pioneering Company	Comments
1947	Point Contact Transistor invented	Bell Laboratories	by Schokley, Bardeen and Brattain
1948	Junction Transistor proposed	Bell Laboratories	by Shockley
1950	High Purity Germanium developed	Bell Laboratories	Early transistors were Germanium
1950	Junction Transistor	Bell Laboratories	
1951	Zone refining of semiconductors developed	Bell Laboratories	by William Pfann
1951	Junction devices sold commercially	General Electric and others	
1951	Gallium Arsenide Material	Siemens	
1952	Alloy Transistor	Bell Laboratories	
1953	Surface Barrier Transistor	Philco	No longer in competitive market
1953	Unijunction Transistor	General Electric	Not commercially successful
1954	Junction Field Effect Transistor proposed	Bell Laboratories	by Shockley
1954	Diffusion process developed	Bell Laboratories	
1954	Oxide Masking	Bell Laboratories	
1954	Photolithographic Techniques	Bell Laboratories	
1954	Zener Diode	National Semiconductor and others	
1954	Transistor Radio	Texas Instruments, Regency	
1954	Silicon Transistor	Texas Instruments	Development started TI as a major manufacturer
1954	Interdigitated Transistor	Transistor Products	Idea survived, company did not
1955	Diffused Base Transistor	Bell Laboratories	
1956	Silicon Controlled Rectifier	General Electric	Commercially successful
1956	Commercial Unijunction Transistors	General Electric	Not commercially successful

4.16 Impact of Technological Change

Table 4.16-1
SEMICONDUCTOR INDUSTRY MILESTONES (Continued)

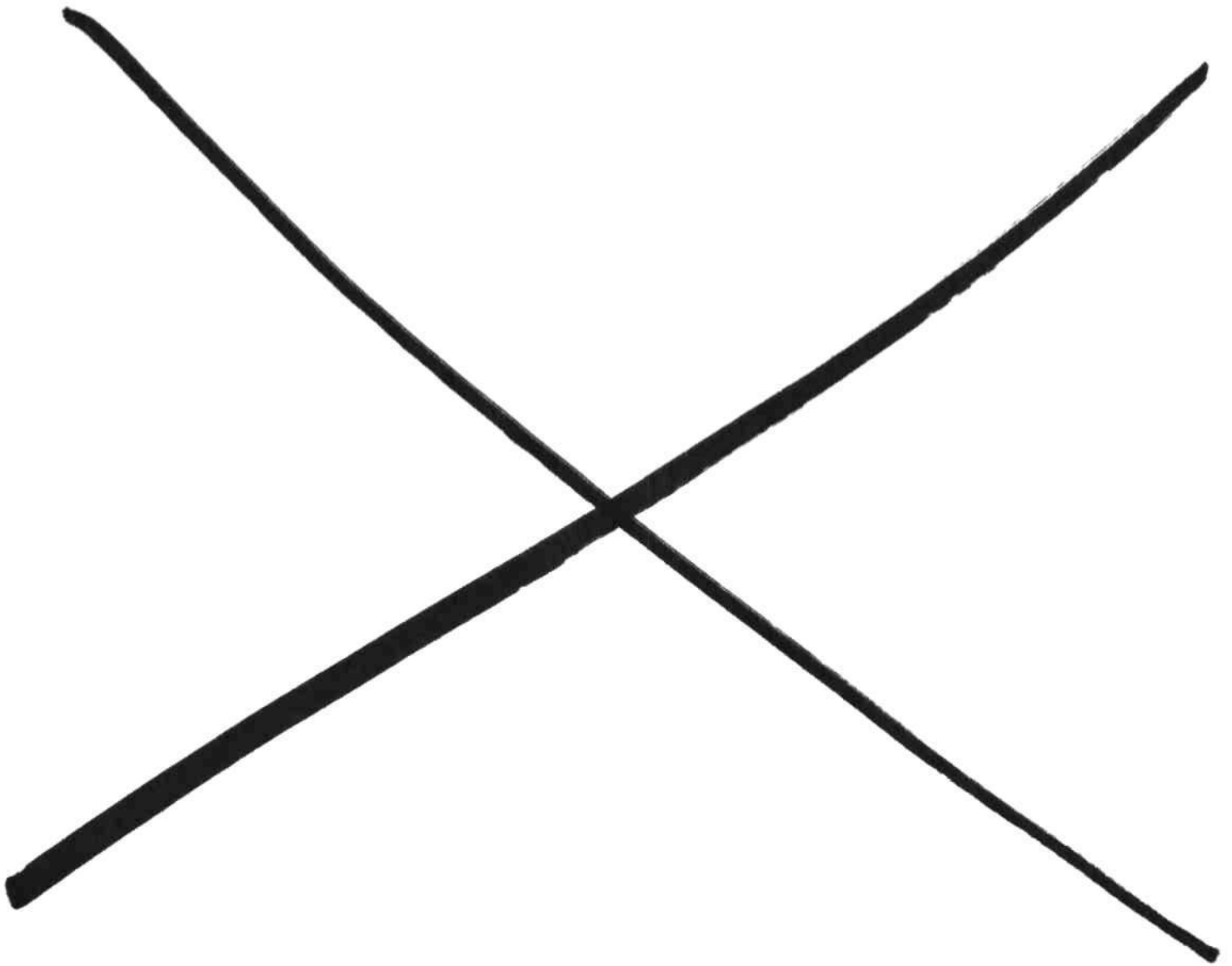
Year	Technological Advance	Pioneering Company	Comments
1957	Mesa Transistor	Motorola	
1958	First Integrated Circuit	Texas Instruments	
1958	Tunnel Diode	Sony	Not commercially successful
1958	Step Recovery Diode	Hewlett-Packard	
1959	Planar Transistor	Fairchild	Invention boosted FCI as a major manufacturer
1960	Epitaxial Transistor	Bell Laboratories	
1960	MOS FET	Bell Laboratories	
1960	Schottky Barrier Diode	Bell Laboratories	
1961	First Commercial IC's	Texas Instruments	Still market leader
1961	First Planar Field Effect Transistors	Amelco	
1961	RTL logic IC's	Fairchild, Texas Instruments	Obsoleted by DTL
1962	Solid State (GaAs) Laser	General Electric, IBM	Parallel inventions, 10 days apart
1962	DCTL logic IC's	Fairchild	Never became popular
1963	Gunn Diode	IBM	
1963	TTL logic IC's	Sylvania	Sylvania left semiconductors in 1970
1963	ECL logic IC's	Motorola	Still leads market
1963	Commercial MOS Discretes	Fairchild	
1963	Linear IC	Fairchild, TI, Westinghouse	Westinghouse dropped out of IC market several years later
1964	Light Emitting Diode	Bell Laboratories	
1964	GaAsP LED	Bell Laboratories	
1964	MOS IC's	General Microelectronics	GMe was purchased by Ford and later dissolved
1964	First Static Flip-flop IC	Fairchild	

4.16 Impact of Technological Change

Table 4.16-1
SEMICONDUCTOR INDUSTRY MILESTONES (Continued)

Year	Technological Advance	Pioneering Company	Comments
1965	IMPATT Diode	Bell Laboratories	
1965	LSA Diode	Bell Laboratories	
1965	High Speed TTL	Texas Instruments	
1966	NMOS	Fairchild	
1968	Commercial Light Emitting Diode	Hewlett-Packard, Monsanto	
1968	Heterojunction Laser	–	
1968	Low Power TTL IC's	Texas Instruments	Obsoleted by Schottky TTL
1968	CMOS IC's	RCA	Still market leader
1969	GaAs Junction FET	IBM	
1970	Charge Coupled Device	Philips	Developed commercially by Intel and Fairchild
1970	Schottky TTL	Texas Instruments	
1971	Isoplanar Process	Fairchild	
1971	Barrit Diode	Bell Laboratories	
1971	Commercial Silicon on Sapphire	Inselek	Went bankrupt
1971	Ion Implantation	–	
1972	Low Power Schottky TTL	Texas Instruments	
1974	I^2L logic circuits	Philips, IBM, Texas Instruments	TI did not invent, but made first commercial devices

Source: DATAQUEST, Inc.



7 Industrial Electronic Components Distribution

7.0 INTRODUCTION

Industrial distribution—the sale of components to equipment manufacturers by intermediaries—is a relatively new phenomenon in electronics. However, the influence of industrial distribution is pervasive and growing; it has been handling an increasing portion of electronic component sales, and now sells 27 percent of all components. It is a complex business and is different in significant ways from its suppliers and the businesses to which it sells. This chapter provides a detailed discussion of the distribution business for all those who are involved or interested in electronics.

The chapter begins with an executive summary that condenses the key issues for corporate management. The discussion of key industry issues dissects the causes of distribution's sales growth, describes competitive factors, considers the problems of technical sales, and presents a discussion of distribution's control problem. In Section 7.3, we describe a stocking location from the perspective of the general manager of that location. The company, "Model Electronics," has been constructed on paper to be a representative outlet of a successful distributor. The emphasis in this section is on assets management, financial analysis, and the traps that one must avoid if one is to be successful. A perspective follows that defines distribution, compares it with other businesses, and places its growth record in an historical framework. The largest distribution customer class—the original equipment manufacturer—is characterized, especially concerning his view of distribution. A distributor profile gives special attention to the sales function and relations with components manufacturers.

The section on companies compares and contrasts the largest distributors. We have selected and discussed in detail a representative subgroup of these companies. We have also run a computerized analysis on balance sheets and income statements going back a number of years. These analyses appear in Chapter 12 of the notebook.

7.1 Executive Summary

Distribution has gained an increasing share of a growing market. During the last ten years, we estimate that the total dollar volume of U.S. component sales grew 30 percent from $5.5 to $7.2 billion, semiconductor sales grew 140 percent from $1.0 to $2.4 billion, and industrial distribution grew 130 percent from $.66 to $1.5 billion. Distribution has increased its share of the components dollar during this period from 12 percent to 21 percent, and it is expected by many that this trend will continue until the share is about 40 percent in 1980.

The explosion of the customer base has been responsible for distribution's growth in share of market. During the same ten-year period, the number of account locations who dealt with one or more distributors has increased from 6,000 to 60,000. (A large company may have several account locations that deal with more than one distributor.) This increase in the customer base has been much more rapid than the growth of distributor sales; in fact, the average sales volume per account location has decreased approximately 77 percent from $110,000 to $25,000. New high-technology, low-cost components such as microprocessors, analog to digital converters, memories, and CMOS have been major influences in this explosion. These components have caused older companies to convert from other technologies to electronics. Furthermore, these high-technology components have encouraged the growth of small electronics firms.

High-technology components are sold through distribution even though the distributor has traditionally been considered a source of local stock and an order-taker. Many small, high-technology accounts can only be reached through distribution and many companies strive to have their products on distributor's shelves at announcement time. Constant pressure is exerted on the distributor to handle high-technology products effectively in the marketplace, both to generate sales of the high-technology parts themselves, and to "drag in" sales of other components.

The big distributors emphasize semiconductor sales. For example, Wyle/Elmar, Hamilton, and Cramer all report that semiconductor component sales approach or exceed half their dollar volume even though these sales are generally 41 percent of all distributors' component sales. DATAQUEST believes that Schweber may have a similar ratio, but because Schweber is privately held, the data are not available. This concentration occurs because semiconductor companies constantly strive to increase volume to compensate for the expected annual price declines of 15 to 25 percent or more, and they pressure their distributors for this volume. The continuous learning involved and the strong sales effort required for semiconductors tends to cause these distributors to neglect their other lines. Consequently, many opportunities for small, new, and profitable distributorships exist outside the area of semiconductor components. Although pricing in semiconductors is extremely competitive, the best distributors have been able to maintain their margins in bad years through contractual price protection.

A restructuring may be underway within the distribution business, since the growth required to maintain market share (9 to 20 percent a year) creates financial strain. We expect that the undercapitalized distributors will not be able to finance this growth and will lose market share. Small distributors will very likely continue to appear, particularly in non-semiconductor components.

Distribution is a people-sensitive business and since there are few economies of scale, the obtaining of business by price cutting is a disastrous competitive strategy for distributors. The key factors are sales penetration through knowledge of the territory and asset control. The best distributors attract entrepreneurial employees and motivate them through incentive programs to provide better service and as-

7.1 Executive Summary

set management. Small distributors can compete effectively with larger ones if they have the motivation, since all buy at similar prices.

7.2 Key Industry Issues

Industrial electronic component distribution is only 20 years old, but has become a significant factor in the components market. Strangely, many in electronics seem to be unaware of distribution's growing market share; even fewer understand its complexities.

This section analyzes some of the changes occurring in distribution and discusses competition among distributors. The last section **"DISTRIBUTION'S CONTROL PROBLEM,"** discusses whether some distributors have outgrown their traditional role and explores some new possibilities.

THE PARADOX OF DISTRIBUTOR GROWTH

The paradox of distributor growth is simply this: high technology causes the growth, but the traditional role of distributors is to sell commodity products. How can this exist and what problems does it cause?

The high-technology products of the semiconductor industry have provided rapidly increasing functional capabilities at rapidly decreasing prices. In addition to reducing the costs of circuit functions, technology has reduced the complexity of the Original Equipment Manufacturers' (OEMs) task of producing and designing equipment. Prior to the advent of the integrated circuit, most OEMs had large design groups to do the circuit design of their logic elements; these groups became unnecessary and were eliminated in the mid-1960s. Similarly, the microprocessor has reduced the complexity of equipment design a second time. An OEM can now change his equipment performance with the mere change of a PROM, and does not need to have as much engineering overhead tied up in PC board design, logic design, mechanical design, document control, and production control.

Overhead is difficult to eliminate once it is on the payroll. Consequently, the advent of LSI technology and microprocessors has tended to favor the companies who are new to electronics—whether they are new start-ups or older companies that have worked primarily with electromechanical components. Indeed, components are now so inexpensive and design is so straightforward that there is a booming market in the hobby microcomputer.

The low cost of electronics and the ease of entry into equipment design has caused a proliferation of new electronic component users and an explosion in the distributor account base. The number of account locations has increased from 6,000 to 60,000 in ten years. At the same time, Hamilton-Avnet alone reported that it had 49,000 accounts in 1976; some of these same accounts also bought from other distributors. While the average annual OEM purchase from distributors was $25,000, the average account at a single distributor was $3,800 annually. This indicates that each OEM account purchases from an average of seven different distributors in a year. Each OEM may represent more than one account, since he could have as many as ten different purchasing locations, each of which is a separate account.

Component manufacturers have been unable to service these new accounts because many of them are too small to be handled economically by the factory; instead, they have relied upon distributors to perform the sales function for them. The number of customers served directly by the components manufacturer has increased during this same time period, but not nearly as fast as the number of distributor accounts. There is also some indication that the average size of the factory direct account is increasing.

Small OEMs see the distributors first, and depend on them for assistance and credit. Distributors provide the only presence in the field for these OEMs to work with. The OEM's needs for technical assistance are mostly satisfied by literature that the distributor obtains

from the manufacturer. Traditionally, the distributor salesman has more buyer rapport than engineering rapport. High-technology component suppliers would like distributors to increase their engineering rapport and contacts. The next section addresses whether this is a paying proposition for the distributor.

CAN DISTRIBUTORS MAKE (AFFORD) TECHNICAL SALES?

Components manufacturers want distributors to make engineering sales contacts because they cannot afford to make these contacts themselves. They frequently do not seem to consider whether the distributor can afford to make the contacts. Distributor margins are small, and this kind of missionary work could rapidly have an adverse effect on them. Clearly, distributors can afford engineering contacts only if they are more productive of margin revenue than buyer contacts.

DATAQUEST suggested to two manufacturers that distributors could be given a rep commission and territorial protection in these situations where the manufacturer desired heavy engineering sales contacts; both indicated they thought this would never happen. Whether this proposal solves the problem or not, we still believe that it is incumbent upon the component manufacturer to give some consideration to protecting the distributor's margin before he proposes a new type of sales activity.

There is some agreement among distributors and manufacturers that the engineering rapport of distributor salesmen is improving. Distributors have been quick to establish this rapport in small OEMs where engineering dominates purchasing, since they are more confident of obtaining the eventual order. They have also invested more sales effort in engineering contacts in those lines where they have a reasonably exclusive position. In these cases, distributors find that training is effective and little correlation exists between the technical knowledge of the salesman and his sales, provided he knows when to obtain help.

Distributors have little incentive to work closely with the engineering department when it is highly likely that they will lose the order at the buyer's desk to another distributor who handles an identical or interchangeable part. In this case, they prefer to depend on the factory for the necessary technical support.

Some products that distributors handle are purchased by engineers for the use of the engineering department; these include microprocessor design systems, panel DVMs, microprocessor kits, and E-PROMs. Since the engineering contact is the only one needed to ensure the sale, this type of product can provide the needed support of distributor technical contacts. These same products can be bought for resale in his equipment by the OEM. Even in this case, engineering contacts can be supported for the product, since the product is not so likely to be a commodity, and is more likely to be sold to an OEM whose purchasing function is engineer-dominated.

The trend is towards increasing participation of distributors in engineering sales contacts. Alert distributors will recognize the situations that allow them to make an adequate return on investment in this activity.

COMPETITION AMONG DISTRIBUTORS

Distribution is an intensely competitive business. Backlogs are relatively small compared to sales volumes, and orders are gained or lost primarily on the basis of personal contacts, or incentive deals.

Following are several reasons for this intensely competitive situation:

- Few economies of scale exist.
- It is difficult to finance the growth needed

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to maintain market share.
- Entry is easy.
- An entrepreneurial attitude is necessary for success.
- Knowledge of the local territory is mandatory.

Few economies of scale exist because distributors' average cost of products varies directly with and is a fixed percentage of sales—approximately 75 percent. Of the distributors' 25 percent, hopefully 5 percent is profit, approximately 10 percent is variable cost, and 10 percent is fixed cost. The result is that only 10 percent of the distributor's costs are subject to reduction with increasing sales volume; the rest vary with sales volume.

Price cutting can be a disastrous strategy. If a distributor cuts prices by 5 percent, then to just break even he must increase sales so that the fixed costs, formerly 10 percent of sales, become 5 percent of sales. This means that sales will have to double to return him to the same profitability; however, return on investment will be decreased because of the extra assets employed. The distributor who cuts prices will find himself constantly struggling just to stay in the same place.

The large distributors may have better buying power. Distributors will periodically take advantage of the semiconductor companies' "end of the month" syndrome to negotiate slightly better prices on specific items. However, the smaller distributors also have special buying opportunities; for example, they may stock their shelves by buying an OEM's surplus. These quantities are significant to them but not large enough to impact the large distributor.

It is difficult to finance the growth needed to maintain market share. The distribution industry as a whole has been growing at a 12 percent a year average rate, with some geographic areas showing more rapid growth. Distribution is a low-margin, high-turn business, and produces the necessary capital for growth only with careful financial management. In recent years, some distributors have become overburdened by debt, and as a result, have lost their position in expanding markets.

Entry into the discrete component distributor/broker business is easy—particularly for an individual or group of individuals who have worked in distribution for some time. Few assets are usually required and the business starts on a brokering basis—the buy and sell order is executed almost simultaneously and no money is tied up. Some of the gross margin is retained in the business, and inventory and other assets are eventually accumulated. Such businesses can grow to a relatively large size in only a few years' time, with possible annual sales of $1 million in five to seven years. A smaller San Francisco Bay Area distributor believes that the 20 distribution businesses in that area will grow to 50 within five years.

Most of the opportunities for small distributors exist outside the area of semiconductor components. Large distributors are narrowing their lines and concentrating their sales in semiconductors; simultaneously, the number of component manufacturers is increasing. Semiconductors are usually bid separately from passive components, and accordingly, a small distributor does not need to stock them to be competitive in breadth of line. Moreover, the price pressure is often less than in semiconductors, which creates the opportunity for higher margins.

An entrepreneurial attitude is necessary for success in distribution, regardless of the size of the organization. The small distributor who has this instinct will prosper, and if he values and rewards the same attitude in others, his business will grow beyond the size that he can personally handle. The distributor or his outside salesmen must be on good personal terms with the people who purchase his products to influence their decisions. The local character of dis-

tribution makes it possible for regional distributors to compete successfully with national distributors. Wyle, now the third largest distributor, is regional and has only a total of six outlets.

COMPARISON: LARGE AND SMALL DISTRIBUTORS

Table 7.2-1 gives a statistical comparison of a large regional distribution center (used for the financial model of Section 7.3), and a small, local specialty distributor. The specialty distributor may have one or two people experienced in distribution as managers who are closely involved in the outside sales function. The specialty distributor has lower sales per employee ($95,000 versus $140,000 annually) and less sales per square foot ($300 versus $780 annually), but has higher inventory turns and a better gross margin. The higher margin more than compensates for any inefficiencies due to smaller size; the higher inventory turns keep down the assets required to run the business.

How can the small specialist outperform the regional or national distributor? In many cases the average professional competence of employees is higher, and the organization is more responsive to change. Certainly, the founder-managers are qualified to run a regional center, and they commonly find the greater risk is compensated by a freedom from corporate constraints and the possibility of greater rewards. Since it is their own business, the gross margin is of highest importance, and they are selective about taking marginal orders. Their own salaries are probably half the payroll; therefore, they can stand larger month-to-month variations in revenue. As this small distributor grows, he will be willing to let the aggregate gross margin fall, since even in this case new employees still cost less than they earn, and his personal returns improve.

Table 7.2-1

ESTIMATED COMPARISON BETWEEN A LARGE DISTRIBUTION CENTER AND A SMALL SPECIALTY DISTRIBUTOR

	Large Regional Distribution Center	Small Specialty Distributor
Net Sales	$14,000,000	$950,000
Warehouse Space (square feet)	10,500	2,000
Office Space (square feet)	7,500	1,000
Manufacturers Stocked	60	12
Items Stocked	20,000	4,000
Employees	100	10
Average Order	$ 150	$ 150
Lines (Items) Per Order	4	3
Number of Accounts	3,700	190
Inventory Turns	4	6
Gross Margin	25%	33%

Source: DATAQUEST, Inc.

This small distributor is a specialist and knows his line of products well. His experience gives him the ability to discern those situations in which he can offer a real service to his customer; moreover, he knows what value to place on this service, which helps improve his gross margin.

THE MISSING MIDDLE

In the early 1960s, distributors handled sales from price lists, and components manufacturers handled everything else. This simple world is illustrated by the left-hand pyramid in Figure 7.2-1.

Motorola introduced their supplementary

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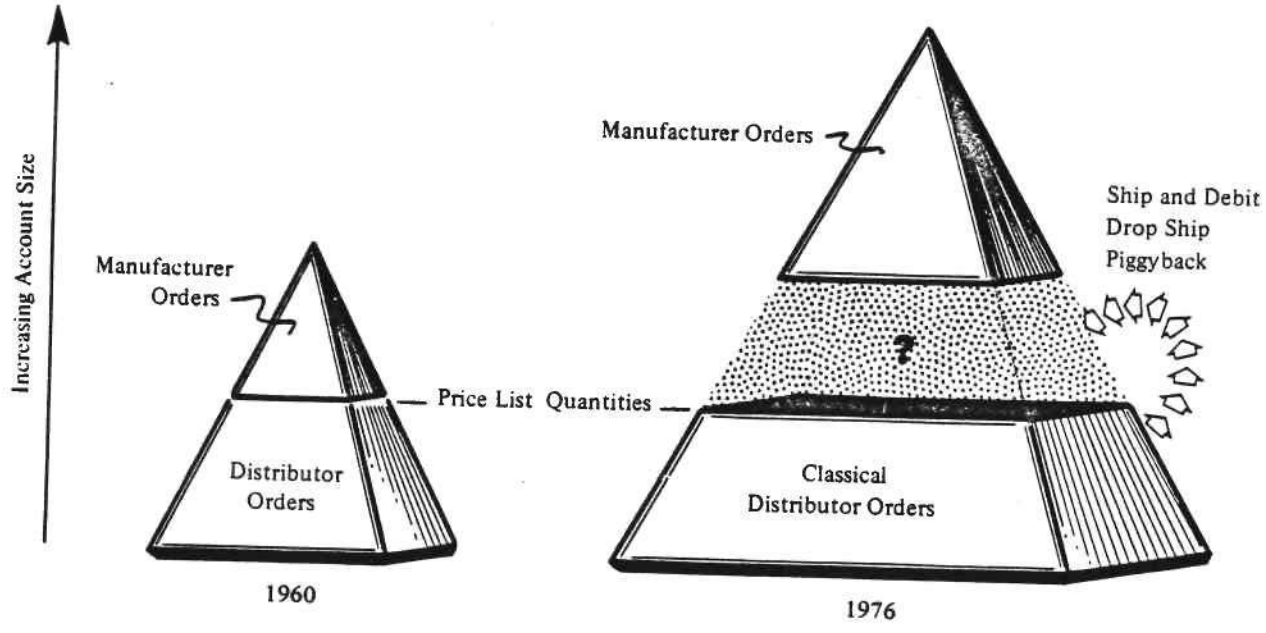
Figure 7.2-1
THE MISSING MIDDLE



program for distribution (SPD) in the mid-1960s so that distributors could participate in above-list price sales. Currently, this type of sale is widespread in distribution and is estimated at 20 to 50 percent of all distributor sales. Some distributors have as much as 50 or 60 percent of their sales in the missing middle category. Gross margins on this type of sale are in the 10 to 15 percent range. The order is frequently drop-shipped to the OEM directly, and never sees the distributor's shelf; sometimes the components manufacturer even carries the receivable.

DATAQUEST refers to this type of sale as the missing middle because it is not the classical price-list-type of distributor business. Furthermore, the distributor often provides no local inventory, so this service is lacking. Finally, the quantities and dollar volumes are possibly high enough so that manufacturers could handle this kind of business economically with their direct sales force, if they had an adequate staff.

The distributor sometimes is able to obtain missing middle business through account control. He will establish contact with a small OEM and work with him through the early growth years. When the company becomes large enough to go factory direct, it may stay with the same distributor. Distributors also participate in missing middle business on a ship-from-stock and debit basis; in this case, the manufacturer may ask the distributor to fill a previous high-volume commitment from his shelf stock. The distributor then debits the manufacturer to recover the reduction in product cost. Piggyback orders occur when a distributor begins to supply a portion of a high-volume purchase order. His local stock buffers the components manufacturer from the small fluctuations in the OEM's month-to-month needs and allows steadier production.

Prices are usually determined through a process of distributor-manufacturer-OEM negotiation in the missing middle. The negotiation is based on a margin spread; the distributor indicates to the manufacturer the sales price and asks for a gross margin. Since the distributor who participates in missing middle business is procuring components at many different prices, there is a tendency for the price protection and returns accounting to become so complex that the components manufacturer may not be able to keep his records completely up to date. Component manufacturers may sometimes believe that returns and inventory procured at "missing middle" prices are being sent back at the higher distributor prices, which is the reason some prefer to drop-ship such orders.

Component manufacturers are reluctant to extend their price lists to higher quantities, which would allow the "missing middle" orders to be covered in a more orderly fashion. This privilege would by law have to be extended to all distributors and would lower the manufacturers' spread on the orders at existing price-list quantities.

Distributors, through participating in missing middle business, are aware that OEMs obtain parts at lower prices than the distributor price. They have long sought to purchase parts on the same terms as OEMs, but have been unable to do so. Recently, one semiconductor manufacturer has allowed distributors to buy selected commodity products on OEM terms. Other components manufacturers are watching this situation carefully, and believe they may have to respond by instituting the same practice. The next section, which deals with distribution's control problems, also addresses the question of whether OEM-like sales to distributors should be on a private label basis.

DISTRIBUTION'S CONTROL PROBLEM

The large industrial distributors, those with sales of $80 million or more, now have a significant portion of their sales volume in the

7.2 Key Industry Issues

missing middle. This particular business differs from the "buy in large quantity and sell in small quantity" business that distribution began with. The margins are lower and distributors provide less service; consequently, they have less control over their market. Furthermore, they have no control over the manufacture of their product. This section discusses some of the various means that distributors might use to improve their control from a third-party perspective and attempts to enumerate their advantages and disadvantages.

No action is always an alternative. Distribution is a growing industry, and there is no evidence to suggest that it will not continue its growth. Perhaps the lack of control will never be evidenced by a substantial crisis, which is unlikely to occur if the majority of a distributor's sales are at price-list quantities.

Additional control can be obtained either through manufacturing or through enhancing the distributor's recognition in the marketplace. Many equipment manufacturers have chosen the manufacturing route and have set up captive or semicaptive manufacturing facilities, with almost uniformly negative results. The captive semiconductor facility has usually provided parts at factory costs in excess of the prevailing market price, even with no administrative overhead assessment. It seems unlikely that distributors would have better results if they attempt to manufacture semiconductor components.

Recognition in the marketplace implies that the distributor will establish some brand or corporate identity. Retailers are able to establish this identity because they have a large customer base; for example, Sears Roebuck puts the Sears label on most products it sells, but manufactures none of them. The company has achieved a certain amount of loyalty from its customers because it supplies products at a competitive, fair price. Furthermore, Sears controls product quality through stringent specification and sample testing, and it backs up its guarantee with nationwide service and spare parts distribution. Electronic companies who have supplied calculators to Sears have discovered that its specifications are more difficult to meet than military specifications. Sears has control of the market, with 1976 sales of $13.6 billion, and it controls many of its manufacturers by buying the bulk of their output.

The metals service industry is a $10 billion segment of industrial distribution. Suppliers like Ryerson and Ducommon achieve some independent corporate identity because 75 percent of all steel orders require some sort of reprocessing. Steel is a standard enough commodity that buyers do not particularly care who the manufacturer was; instead, they depend on their distributor to ensure that the steel meets industry specifications. Ducommon (Kierulff's parent company) is one of the five largest steel reprocessors and distributors, and serves some 30,000 customers in over 700 industries. Since steel is a commodity product, virtually an identical product is available from others. Consequently, competition in the metals service industry, like industrial electronic distribution, is on the basis of service: technical advice, up-to-the-minute product information, the most modern processing equipment, and "on time" performance.

Industrial electronic distributors could obtain brand or corporate identity by private labeling of either commodity components, specialty components, or equipment. Private labeling is discussed here as a potential method of conducting business; DATAQUEST does not believe that there is any private labeling of industrial semiconductor components at the present time.

OEMs have reliability and incoming reject problems with commodity semiconductor components (see the discussion in 7.5, **"THE SIGNIFICANCE OF SEMICONDUCTORS"**). These problems are severe enough that reliabil-

ity and test houses have been created to satisfy them, and some OEMs are willing to pay $.05 to $.10 extra per part to these test houses to have their parts screened. A distributor who provides a product with his name on it that does not have these problems might be able to achieve some brand recognition. It would probably be necessary for him to procure his components from multiple sources and to establish his own procurement specifications.

Component manufacturers are understandably upset when a distributor criticizes the quality of the products to his customers. Private branding would tend to alleviate this situation, because the relative quality between different component suppliers would then become a subject of discussion between the distributor and his manufacturers, rather than the distributor and his customers.

Distributors would have greater motivation to have these commodity products designed in if they were private labeled, since there would be less chance of losing the order to a competitive distributor once it reached purchasing. This would free the component manufacturer to devote sales effort to his specialty products where he has achieved product differentiation. The private label distributor would lose his price protection for these components because they could obviously never be sold by anyone else. Component manufacturers would benefit from this, and both parties should be able to eliminate a certain amount of unnecessary (and expensive) price protection and returns accounting.

If the trend towards component sales to distributors on OEM terms continues, component manufacturers may have no alternative but to become involved. In this case, private labeling offers additional advantages to the components manufacturer; it enables him to preserve the distributor mark-up in those situations where the customer prefers his brand to the distributor brand. If both OEM-like sales and distributor price protected sales are conducted simultaneously through the same marketing channels, private labeling of the OEM-like sales would allow these parts to be kept clearly separate.

The distributor, unprotected by price protection, would need to precisely anticipate the market. It is likely that he would continue to purchase and stock branded products from the components manufacturer, both to compensate for his market estimates and to supply to customers those preferred brands.

The distributor certainly would expect to buy private label parts at a substantial discount from existing distributor list prices. He undoubtedly has an idea of what this discount might be through his participation in above-list price sales. Probably 20 to 50 percent discounts from the distributor list are not uncommon on higher-volume orders. Components manufacturers would obviously be reluctant to lose the mark-up they now make on distributor sales and might retaliate.

"Strike back" by component manufacturers would probably be through denial of specialty products to the distributor who private labels the commodity products. Naturally, the component manufacturer who first agrees to private label would not be the one to employ this strategy. It is also questionable whether a component manufacturer would elect to "strike back" in the case where the private label commodity product is one which he does not manufacture.

"Strike back" is a powerful weapon if it is employed. Not only would the distributor lose the higher margin that he usually obtains on specialty products, but more importantly, he would lose one of the principal product lines he has to attract customers. This effect could be the more substantial of the two, and the net result could be that he loses rather than gains margin.

Distributors could also consider private

labeling specialty components. It is doubtful that a component manufacturer would agree to private brand a component that he had developed with his own R&D funds; thus, the distributor would probably have to fund the product development himself. This would require substantial commitments on the part of the distributor. With the current multiplicity of products and costs of development, it would be an involved process for a distributor to develop enough private label products to encompass even a fraction of his product lines.

Furthermore, distributors could consider private labeling some of the newer equipment products that they are beginning to handle; these include microprocessor design systems, panel DVMs, microprocessor kits, and E-PROMs. Many of these products have been designed by component manufacturers who consider the product development expense as a necessity. Almost any component manufacturer would not object to a distributor who handled a complementary equipment product, and many would welcome the chance to reduce their product development costs in this area.

Some in the industry question whether components manufacturers can continue to recover the costs of software and hardware product development in the price of microprocessor parts. However, OEMs need these support systems to design their product and an effective case can be made for developing these items outside the components manufacturer. Many small companies have already been started to address this market, and distribution might offer an effective way for these companies to reach customers. Private labeling could be an acceptable alternative for them.

7.3 Distributor Model

This section describes in detail a hypothetical distribution center called "Model Electronics." This company has been constructed on paper to represent one of the more successful distribution centers, and has better financial performance than the industry averages. "Model Electronics" is presented from the General Manager's perspective, with an emphasis on assets management, financial analysis, and the traps to avoid to be successful.

SUMMARY

Model Electronics (see Table 7.3-1) was structured to have 100 employees. It has average sales that are comfortably within the industry range of $100,000 to $200,000 per employee. With total sales of $14 million, it is well above the industry averages in sales per location.

Wyle had the highest average sales per location (six locations) in the industry with $9.3 million in 1976 and an estimated $13 million in 1977. Hamilton was second with $7.2 million per location for 32 locations in 1976. However, many distribution centers are larger than these averages and have sales over $20 million, including several operated by Wyle and Hamilton. Of the 20 centers in the San Francisco Bay Area, Bell, Kierulff, Cramer, Hamilton-Avnet, and Wyle-Elmar are all believed to be in excess of $10 million annual sales.

Model's floor space is based on $780 annual sales per square foot and is divided into 40 percent office space/60 percent warehouse space. The number of accounts is derived using average annual sales per account of $3,800 per year. Model stocks lines from 60 manufacturers; this is within the spread of 28 to 100 manufacturers stocked by the 14 largest multi-outlet regional and national distributors. Some of these lines are probably franchised regionally or nationally by the company and may not represent a franchise at this particular location. Model's local branch probably concentrates its efforts on lines that are particularly well understood by its salesmen or especially in demand. Model may make 80 percent of its sales from the lines of 20 manufacturers. The number of items stocked (20,000), items per order, and average order size are all representative.

Model Electronics' 100 employees are functionally organized into 8 groups: Product Management, Outside Sales, Inside Sales, Applications, Credit and Collections, Data Base Management, Warehousing, and Administration. The functions performed by each group and the number of people in each group are given in Table 7.3-2. Head counts are representative but can vary considerably in the industry from those shown here; for example, a distributor might emphasize a hard-to-sell but high gross margin product. Consequently, he would have more people in outside sales and applications and a lower average revenue per employee.

Table 7.3-1

OPERATING PARAMETERS OF "MODEL ELECTRONICS"

Net Sales	$14,000,000
Warehouse Space (square feet)	10,500
Office Space (square feet)	7,500
Manufacturers Stocked	60
Items Stocked	20,000
Employees	100
Average Order	$ 150
Lines (Items) Per Order	4
Number of Accounts	3,700

Source: DATAQUEST, Inc.

7.3 Distributor Model

Table 7.3-2

FUNCTIONAL ORGANIZATION OF "MODEL ELECTRONICS"

Group	Responsibilities	Number of Employees
Product Management	Each product team consists of two persons and handles the products of eight manufacturers. The team is responsible for manufacturer negotiations concerning stocking levels, price protection, quantity prices not on the price list, and returns. They also handle relations with Sales.	10
Outside Sales	Field salesmen call on buyers and engineers to supply information and obtain orders.	20
Inside Sales	This group handles telephone orders. They compare the order with available stock (usually by computer) and advise the customer of availability. Orders are taken but not entered.	20
Applications	This group provides applications support to sales. They also service the design center.	4
Credit and Collections	Credit checks new orders for credit and approves them for entry. Credit also approves new customers and expedites payment on delinquent accounts.	6
Data Base Management	This group is responsible for the data base. They make all order entries, record shipments, and handle exceptions and customer inquiries.	4
Warehousing	This group includes all receipt, unpacking, binning, order make up, and packing for shipment. They also handle the will call function and component subassembly.	28
Administration	This group includes finance and accounting, the switchboard, personnel, and Maintenance (the General Manager's Office).	8
	Total	100

Source: DATAQUEST, Inc.

The sales function is important to distributors. At Model, Outside Sales, Inside Sales, and Product Management occupy half the employees that work for the firm. This total is typical, but often the ratio of outside to inside sales changes from distributor to distributor, depending on whether most sales are made through telephone orders or personal contacts.

Product management has the responsibility to make decisions concerning product lines. Although they make decisions concerning which items to stock, management usually reserves the right to decide which lines to stock and how many inventory dollars should be invested in each line. The reader should note that there is not enough Product Management to handle the number of product lines. Each team has two people and handles eight manufacturers. Model will have Product Management for only 40 lines, and since it stocks 60 lines, 20 of them will be somewhat neglected. The larger distribution centers can afford more Product Man-

7.3 Distributor Model

agement, which results in a more effective job of covering all product lines.

SALES ANALYSIS

This section considers different ways that the sales of Model Electronics can be dissected and analyzed. First, a typical price list is presented, then sales are broken down by product type and discount class, and finally an example is constructed to show why a distributor can inventory components less expensively than an OEM.

Typical Price List

A typical distributor price list is shown in Table 7.3-3. This was taken from an actual price list; only the names of the manufacturers and products were changed. The gross margin ratios are taken for each item and happen to be identical within the *x* series and within the *x-y* series. Gross margin spreads that are believed to be typical of the industry are shown in the same table.

The smaller quantity breaks have higher margins to compensate the distributor for his higher handling costs per item. Similarly, slow-moving items normally carry a higher gross margin to compensate the distributor for his costs of carrying inventory.

A common industry "thumb rule" is that the gross margin times the inventory turns should be 100 percent, which is sometimes referred to as a 100 percent annual gross profit margin. Gross margin is usually computed for each part type with no consideration of the quantity category in which sales are made. The computation of sales is made by totaling the total sales dollars, and the cost is obtained by multiplying the distributor price by the number of units sold. Component manufacturers and distributors both have computer programs that provide listings of gross margin and inventory turn for each part type, as well as summaries of product line performance.

Table 7.3-3

TYPICAL PRICE LIST
XYZ TRANSISTORS, INC.

Part Number	Price to OEM 1-24	25-99	100-999	Price to Distributor
X-100	$ .83	$ .76	$ .66	$ .53
X-200	1.24	1.14	.99	.79
X-300	5.69	5.23	4.55	3.64
X-400	10.46	9.63	8.37	6.70
YZ-100	.49	.41	.34	.27
YZ-200	7.92	6.55	5.46	4.37
Distributor's Gross Margin				
X-series	37%	31%	20%	
YZ-series	45%	33%	21%	
Typical Spread for Various Products:	25-50%	20-40%	15-25%	

Source: DATAQUEST, Inc.

Distribution by Margin Class

The distributor buys his price list items at a fixed price and sells them at different prices that depend on the quantity being ordered by his customer. For this reason, his average gross margin depends on the quantity ranges in which his business falls.

Before proceeding, we must add that not all of the distributor's purchases are at the distributor prices shown in Table 7.3-3. During the last 15 years, it has become common for distributors to sell a portion of their merchan-

7.3 Distributor Model

dise at quantities above those that the price list covers. (See discussion of Section 7.2, "THE MISSING MIDDLE".) The prevailing market prices in these higher quantity ranges are below distributor prices. As a result, the components manufacturer must give the distributor a further discount, which is in the 10 to 15 percent range, from the prevailing market price for him to handle the order. These sales are called "negotiated" sales in Table 7.3-4.

Table 7.3-4 makes two different assumptions about the percentage of Model Electronics' sales that might be occurring in each quantity category. In the first example, it has been assumed that most of the sales are in the higher-quantity ranges; the result is that Model's gross margin averages 25 percent.

In the second example, it is assumed that more of Model's sales occur in the lower-quantity ranges; the result is that the company's gross margin now averages 32 percent. We must add that this probably does not mean

Table 7.3-4

DISTRIBUTION BY MARGIN CLASS
(Dollars in Millions)

High Quantity Sales

Quantity	Percent of Sales	Amount	Average Gross Margin	Gross Profit
1-24	10%	$ 1.4	45%	$ .63
25-99	20	2.8	35%	.98
100-999	30	4.2	25%	1.05
Negotiated	40	5.6	15%	.84
	100%	$14.0		$3.50

$3.50/$14.0 = 25% Gross Margin

Low Quantity Sales

Quantity	Percent of Sales	Amount	Average Gross Margin	Gross Profit
1-24	20%	$ 2.8	45%	$1.26
25-99	40	5.6	35%	1.96
100-999	30	4.2	25%	1.05
Negotiated	10	1.4	15%	.21
	100%	$14.0		$4.48

$4.48/$14.0 = 32% Gross Margin

Source: DATAQUEST, Inc.

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that Model makes a higher *net* profit. The average order size is undoubtedly smaller in the second example; therefore, more staff is required in Inside Sales and Warehousing to process the orders, which increases costs and decreases the extra gross margin.

Shifts like that illustrated in Table 7.3-4 may occur between different geographical regions and during varying periods in the business cycle. Some geographical areas have only the Research and Engineering labs of commercial OEMs or only military electronics OEMs, which both usually buy more products at the lower volumes. Moreover, some OEMs discover they need most of their engineering staff to assist production during prosperous times in the business cycle; consequently, small quantity purchases for laboratory use may actually decline in booms and expand in recessions.

Table 7.3-5
DISTRIBUTION BY PRODUCT TYPE

Semiconductors	50%
Capacitors	11
Resistors	13
Connectors	14
Relays/Switches/Keyboards	5
Other (Inductors, Transformers, Misc.)	7
	100%

Source: DATAQUEST, Inc.

Distribution by Product Type

Table 7.3-5 shows Model's sales distribution by product type. Since Model is a branch of a large national or regional distributor, it has a proportionately higher percentage of its sales in semiconductors. Among larger distributors in 1976, Hamilton reported 62 percent semiconductor sales, Wyle reported 50 percent, Cramer reported 43 percent, and Pioneer 33 percent. Connectors were the second largest sales category, with Hamilton at 24 percent, Wyle 14 percent, and Cramer 13 percent.

Individual branches of any distributor, such as Hamilton, Wyle, or Cramer, might vary considerably from the company's national averages. The numbers in Table 7.3-5 are within the range that would be representative for Model Electronics.

Model might supply other products besides those shown. Tools and expendable materials are sometimes handled by distributors, which include hand tools, soldering irons, solder, wire, and hardware; Marshall Industries is one distributor that specializes in this kind of item. Model might also handle equipment that includes instruments like panel digital voltmeters, power supplies, microprocessor kits, and microprocessor design centers.

Inventory Sharing

One of the functions that distributors perform is to provide a "safety" stock to isolate the components manufacturer from the month-to-month variations in demand from individual OEMs. Distributors usually find several OEMs that use the same part type. When the distributor stocks the part for them, he finds he can support their needs with less "safety" stock as a percent of usage than they would require if they stocked the part themselves. Even with this smaller inventory, the distributor is able to reduce the stock outages below the level the OEMs could achieve for themselves.

If a distributor stocked parts for three manufacturers who had the same average monthly requirements and who each kept the same "safety" stock as a percentage of usage, his average monthly requirements would be three times as great. The significant factor is

7.3 Distributor Model

that his "safety" stock would be a smaller percentage of the combined usage as shown in Table 7.3-6.

Statistically speaking, this phenomena could be explained by determining that when independent random variables with an average deviation from the mean are added together, the resultant distribution is "tighter." It is tighter because the deviations add in an RMS (root mean square) way and the means just add. Suppose a distributor stocked for three manufacturers who each required 1,000 pieces of a given component a month and who each expected their monthly usage to vary by plus or minus 40 percent. The distributor would need to supply an average of 3,000 components a month, but would see monthly variations in usage of only plus or minus 23 percent (.58 times 40 percent equals 23.2 percent). This would allow the distributor to work with a smaller "safety" stock and help him to achieve fewer stock outages.

Table 7.3-6

REDUCTION IN DISTRIBUTOR'S SAFETY STOCK FOR SHARED INVENTORY

Reduction in Percent "Safety" Stock	Number of Identical Manufacturers Served
$\sqrt{2}/2 = 71\%$	2
$\sqrt{3}/3 = 58\%$	3
$\sqrt{4}/4 = 50\%$	4
$\sqrt{5}/5 = 45\%$	5

Source: DATAQUEST, Inc.

FINANCIAL STATEMENTS

The income statements and balance sheets for Model Electronics are given in the next two sections. They are structured to represent a conservatively financed distributor in the business, and also have been constructed so that Model has the financial capacity to grow at the 12 to 15 percent a year rate required if the company is to maintain or improve its existing share of market. While these financial statements are above average, the better companies meet or exceed them in most respects. (Refer to Section 7.7, which gives historical financial statements for selected distributors.)

Income Statement

The income statement for Model Electronics is shown in Table 7.3-7. Model has a profit before interest and taxes that is respectable at 7.36 percent. This is in the range of Pioneer (7.2 percent) and Wyle (7 percent estimated for 1977), approaches Hamilton (10.6 percent), and is significantly above the industry average. Gross profit is average at 25 percent, and expenses are 17.64 percent.

Balance Sheet

Model's balance sheet is shown in Table 7.3-8. Model is fairly heavily leveraged and has a liability to equity ratio of $(2,544,092 plus 500,000)/$2,410,454 equals 1.26, which is not excessive but would be more conservative if lower. The more conservatively financed companies like Pioneer-Standard and Hamilton-Avnet have maintained this ratio below one. Note that Model's liability to equity ratio improved from 1.37 the previous year.

Model has current assets that are 90 percent of assets; $4,915,455/$5,454,456 equals 90 percent. Model's average assets over the last two years are $5 million, which gives a sales to

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Table 7.3-7

MODEL ELECTRONICS, INC.
INCOME STATEMENT

Gross Sales	$14,285,714		102.00%
Cash Discounts	(185,714)		(1.30)
Returns & Allowances	(100,000)		(0.70)
Net Sales		$14,000,000	100.00%
Cost of Sales			
Merchandise	$10,150,000		72.50%
Freight	70,000		0.50
Discounts Earned	140,000		1.00
Inventory Reserve	140,000		1.00
		$10,500,000	75.00%
Gross Profit		$ 3,500,000	25.00%
Operating Costs			
Product Management	$ 274,600		1.96%
Outside Sales	676,000		4.83
Inside Sales	365,200		2.61
Applications	203,200		1.45
Credit & Collections	150,400		1.08
Data Base Management	134,800		0.96
Warehousing	418,800		2.99
Administration	246,600		1.76
		$ 2,469,600	17.64%
Profit Before Interest and Taxes		$ 1,031,063	7.36%
Interest Expense		88,755	0.63%
Profit Before Income Taxes		$ 942,308	6.73%
Taxes		452,308	3.23%
Net Profit		$ 490,000	3.50%

Source: DATAQUEST, Inc.

average asset ratio of 2.8, and a return on average assets of 490,000/5,000,000 equals 9.8 percent. Cost of sales over average inventory (or inventory turn) is computed as 10,150,000/.5(2,913,676 plus 2,428,230) equals 3.8.

Model declares no dividends; therefore, all the earnings are kept in the corporation as retained earnings.

GROWTH—HOW DO YOU FINANCE IT?

Distribution is a growing industry and has been averaging 12 percent a year in the United States. Model's management is ambitious and strives to improve its share of market, and thus targets for 20 percent growth in sales in the next five years. This growth in sales will require a growth in assets that also is 20 percent, which will occur because the accounts receivable and

7.3 Distributor Model

Table 7.3-8

MODEL ELECTRONICS, INC.
BALANCE SHEET

	Current Year	Previous Year
ASSETS		
Current Assets		
Cash	$ 150,000	$ 90,000
Accounts Receivable	1,831,779	1,526,396
Inventory	2,913,676	2,428,230
Prepaid Expenses	20,000	15,000
Total Current Assets	$4,915,455	$4,059,626
Property and Equipment		
Land	$ 100,000	$ 100,000
Buildings	500,000	400,000
Furniture and Equipment	194,091	175,828
Autos and Trucks	15,000	10,000
	$ 809,091	$ 685,828
Less Accumulated Depreciation	270,000	200,000
Net Property and Equipment	$ 539,091	$ 485,828
	$5,454,546	$4,545,454
LIABILITIES AND SHAREHOLDERS' EQUITY		
Current Liabilities		
Notes Payable to Banks (10% Interest)	$ 559,092	$ 400,000
Accounts Payable	1,470,000	1,225,000
Income Taxes	250,000	230,000
Accrued Salaries and Commissions	150,000	140,000
Other Accrued Expenses	115,000	110,000
Total Current Liabilities	$2,544,092	$2,105,000
Long Term Debt Due After One Year		
8% Mortgage Payable	$ 500,000	$ 520,000
Shareholder's Equity		
Common Shares	$ 500,000	$ 500,000
Capital in Excess of Par	500,000	500,000
Retained Earnings	1,410,454	920,454
Total Shareholders' Equity	$2,410,454	$1,920,454
	$5,454,546	$4,545,454

Source: DATAQUEST, Inc.

7.3 Distributor Model

inventory of Model will have to expand as sales expand. Furthermore, there will eventually have to be a new plant and equipment as well. This growth will only partially be offset by the natural growth in Model's accounts payable.

It is obvious that Model's 9.8 percent return on assets is not large enough for all of its increase in assets to come from retained earnings; other sources will be needed. This section explores the use of assets at Model Electronics and discusses some ways assets can be tied up in unproductive uses; we then discuss financing asset growth.

Asset Turns

Asset "turns" is a measure of the efficiency of asset employment; it is simply the ratio of sales to average assets. For Model, this ratio is 2.8. *Turn* is a word that has been historically applied to inventory. If an item is stocked by a distributor who sells all the shelf stock four times a year, then the inventory is said to have a four-times turn. *Turn* in this sense is a misnomer when applied to the total assets of Model—for many of the assets do not turn. Fixed assets are not bought and sold and neither is cash; however, we will show that the asset "turn" ratio is a useful concept. ("Turn" is indicated in quotation marks when it refers to a financial ratio rather than movement of stock from inventory.) In Table 7.3-9, suppose that Model could improve asset turns. The increase in assets for every new dollar of sales is shown.

Table 7.3-9

THE EFFECT OF ASSET TURNS

Asset "Turns"	=	2.5	We need to increase assets $0.40 for every $1 in sales.
	=	3.0	$0.33 for every $1 in sales.
	=	3.5	$0.29 for every $1 in sales.

Source: DATAQUEST, Inc.

Receivables and inventory also have turns. For Model, receivable turns equal 14,000,000/.5(1,831,779 plus 1,526,396) equals 8.33; inventory turns equal 14,000,000/.5(2,913,676 plus 2,428,230) equals 5.24. Improving the turns of these two items will improve asset turns. The other assets—cash, property, and equipment—cannot readily be managed in a turns basis since decisions are only made periodically.

Ship and Debit Lowers Turns

Ship and debit refers to the practice of filling orders from distributor stock when the selling price is below the distributor's price. When the distributor finds a high-volume buyer who wants a discount, he can often obtain permission from the factory to ship shelf stock. He negotiates a new distributor price with the components manufacturer for that order only, and sends a credit memo to the factory for the difference between the old and new distributor price. It appears that this process has worked effectively: the distributor's margin has been maintained and the product was sold; however, inventory turns are affected negatively because the assets are in stock at the higher price. Extra money is tied up even though the components move promptly off the shelf. Moreover, communication is required between the distributor and the factory to negotiate prices. This communication is expensive because it is conducted by the distributor's higher-paid staff members. Furthermore, still more costs are incurred because of the paperwork required to initiate and track debit memos.

An example is a ship and debit deal that Model has just negotiated. Assume:

- The items have been in stock three months.
- 10,000 units cost $.79 each.
- The market price is $.52.
- The new negotiated distributor price is $.42

7.3 Distributor Model

(19 percent gross margin)

- Normally the units sell at an average list price of $1.05 (24 percent gross margin).

The deal appears profitable at this stage. Four turns a year at 19 percent gross margin equals 76 percent gross profit, which is fairly close to the 100 percent target.

However, it is not as effective as it seems. Compute inventory "turns:"

"turns" = $ Sales/$ Inventory, averaged over the year
= 10,000 times $.52/10,000 times $.79 times .25
"turns" = 2.63 (way below the target of four turns)

To emphasize: the *inventory* turned four times a year, but the assets only "turned" 2.63 times.

Actually, the computation above makes the situation look worse than it really is since it fails to take into account the fact that Model has a credit memo in process. We can be more precise if we compare a normal sale at the average list price, the ship and debit sale, and a sale in which the inventory was held at the negotiated distributor price of $.42. Table 7.3-10 compares the way Model's assets are tied up.

Again, "turns" can be computed by dividing sales by assets employed. In the price list case, we had $7,900 tied up for 30 days—the 30 days after we paid for the merchandise but before we sold it; on a quarterly basis, this amounts to average assets of $7,900/3. When the sale is made, the inventory is shipped and the inventory asset is converted into an account receivable asset, which is on the books for 60 days or two-thirds of a quarter. The computation for inventory "turns" is given in Table 7.3-11, including the computation for a high-volume sale without ship and debit.

Table 7.3-11

INVENTORY "TURNS" FOR A HIGH-VOLUME SALE

"Turns" (Price List Sale) =

$$\frac{10{,}500}{(7{,}900 \times 1/3 + 10{,}500 \times 2/3)1/4} = 4.36$$

"Turns" (High-Volume Sale) =

$$\frac{5{,}200}{(4{,}200 \times 1/3 + 5{,}200 \times 2/3)1/4} = 4.27$$

The ship and debit case is similar, except for the existence of the debit memo. This in effect reduces the money tied up in accounts receivable *if* it can be immediately credited

Table 7.3-10

ASSET EMPLOYMENT IN A SHIP AND DEBIT SITUATION

	Price List Sale	High Volume Sale	Ship and Debit
Inventory at	$ .79	$ .42	$ .79
Sell at	$1.05	$ .52	$ .52
Inventory	$7,900 x 90 days	$4,200 x 90 days	$7,900 x 90 days
Less Accounts Payable	7,900 x 60 days	4,200 x 60 days	7,900 x 60 days
	$7,900 x 30 days	$4,200 x 30 days	$7,900 x 30 days
Accounts Receivable	$10,500 x 60 days	$5,200 x 60 days	$5,200 x 60 days
Debit Memo	–	–	$1,000

Source: DATAQUEST, Inc.

7.3 Distributor Model

against the money Model owes the manufacturer. Sometimes this is not possible and the credit may not be available for 60 to 90 days, which would obviously tie up more assets. Computations for "turns" under these circumstances are given in Table 7.3-12. It seems apparent that ship and debit is not an effective way to utilize assets.

Table 7.3-12

INVENTORY "TURNS" IN A SHIP & DEBIT SITUATION

"Turns" (Ship and Debit) =

$$\frac{5{,}200}{(7{,}900 \times 1/3 + 4{,}200 \times 2/3)1/4} = 3.83$$

If the Credit Memo is not available for 60 days we get:

"Turns" (Ship and debit) =

$$\frac{5{,}200}{(7{,}900 \times 1/3 + 5{,}200 \times 2/3)1/4} = 3.41$$

How Does A Distributor Obtain New Assets?

Model will need to raise money to purchase the assets required by its expanding business. To see where these assets derive, look at the liabilities figures in the balance sheet (see Table 7.3-8) as summarized in Table 7.3-13. If sales increase, debt may have to increase. Accounts payable will normally increase in proportion to sales, and is now 10.5 percent of sales. Other liabilities will also normally increase in proportion to sales, provided they are for items that tend to increase with sales—such as salaries. Stockholders' equity will be increased by the net profit after taxes if no dividends are paid.

If Model can maintain its sales to asset ratio, then liabilities and assets will have to increase in proportion to sales. For this to occur (without changing balance sheet ratios), all

Table 7.3-13

SUMMARY OF MODEL ELECTRONIC LIABILITIES

Debt (Notes + Mortgage)	=	$1,059,092	19.4%
Accounts Payable	=	1,470,000	27.0
Other Liabilities (Taxes, Accrued Salaries, & Expenses)	=	515,000	9.4
Shareholders' Equity	=	2,410,454	44.2
		$5,454,546	100.0%

items on the liability side of the balance sheet will have to increase in proportion to sales as well. It is reasonable to expect that this increase will occur naturally for accounts payable and other liabilities. If profits are substantial enough so that shareholders' equity increases in proportion to sales as well, it is likely that it will be possible to borrow the other necessary funds. Banks are likely to part with these funds, provided the debt to equity ratio—currently .44—does not worsen.

Currently, Model has a return on average equity of 23 percent (see Table 7.3-14 for computation); thus, it should be able to pay down its debt slightly when the growth in sales is only 20 percent as it was in the last year. Eventually, shareholders' equity will increase (with constant profits) to the point where the return on shareholders' equity is equal to the rate of growth of sales.

Table 7.3-14

COMPUTATION OF RETURN ON AVERAGE EQUITY

$$\text{Return on Average Equity} = \frac{490{,}000}{(2{,}410{,}454 + 1{,}920{,}454)1/2} = 23\%$$

7.3 Distributor Model

The payment of dividends would not impair return on equity, but would slow the rate of increase in shareholders' equity and thereby reduce the growth rate that could be achieved with given profits and asset turns.

Five-Year Growth Projection

What if Model cannot maintain its profits and asset turns? This subsection presents (in Table 7.3-15) an example of what might happen. A 20 percent sales growth rate is assumed, giving rise to five-year sales shown in the first section of the table. Depending on the asset turns that Model can achieve, varying amounts of new assets will be required. Since we are interested in new assets, we subtract the assets needed in year five from those used in year one.

Some capital is generated internally as shown in section 2 of the table. Part of it is from earnings retained by Model, and part is from the normal growth in payables. It should be noted that we have been conservative here and have assumed that the other liabilities do not grow at all with sales. If the capital generated here is greater than what is needed, then Model will need no new debt and can pay off old loans.

Part 3 of Table 7.3-15 takes the difference between assets required and assets generated internally. Bracketed quantities indicate the amount of funds to be borrowed.

Part 4 examines Model's borrowing capacity; it is assumed that Model can borrow additional funds provided its balance sheet does not degrade. This is an effective assumption if credit markets are stable; however, it would not be effective during a "credit crunch" when bankers tend to ration their loanable funds.

Model could maintain its debt to equity ratio if they borrowed funds equal to their retained earnings. However, this would cause their total liabilities to increase by the amount of increase in accounts payable. Part 3 of the table maintains a constant liability to equity ratio by subtracting out the growth in accounts payable.

In practice, the decision whether or not to borrow and whether or not to strengthen the balance sheet by reducing debt depends on the propensity of the management of Model Electronics to take risk, and on their view of future credit markets.

FINANCIAL EVALUATION OF MODEL ELECTRONICS

Some of the significant financial quantities for Model Electronics are given in Table 7.3-16; most of these have been discussed in the previous subsections, except for the financial ratios. The fact that 90 percent of the asset side of the balance sheet is current assets makes these ratios look conservative. The current ratio is 1.93, and the quick ratio (which measures the percentage of current liabilities that could be paid off by cash and receivables) is also conservative at .79.

Table 7.3-16

FINANCIAL EVALUATION OF MODEL ELECTRONICS

Profitability Ratios	
Operating Earnings	7.36%
Net Income	3.50%
Return on Average Assets	9.80%
Return on Average Equity	22.63%
Utilization of Assets	
Average Asset Turns	2.80%
Average Inventory "Turns"	3.80%
Accounts Receivable (Days[1])	43
Payables (Days[1])	38
Financial Ratios	
Current Ratio	1.93%
Quick Ratio	.79%
Debt to Equity Ratio	.44%
Inventory + Receivables as a percent of assets	87%

[1] 360 day basis

Source: DATAQUEST, Inc.

7.3 Distributor Model

Table 7.3-15

FIVE-YEAR GROWTH PROJECTION FOR MODEL ELECTRONICS
(Assumes 20% Sales Growth)
(Dollars in Thousands)

1. Asset Requirements

	Year 1	2	3	4	5	Total Sales	5-Year Increase
Sales	$14,000	$16,800	$20,160	$24,192	$29,030	$104,182	$15,030
Average Assets Required							
2.4 turns	$ 5,833	–	–	–	$12,096	–	$ 6,263
2.8 turns	5,000	–	–	–	10,368	–	5,368
3.2 turns	4,375	–	–	–	9,072	–	4,697

2. Capital Generated Internally

5-Year Profit	Net After-Tax	+	Capital From Payables[1]	=	Total Capital Generated
0%	–		$1,503		$1,503
2%	$2,084		1,503		3,587
3%	3,125		1,503		4,628
4%	4,167		1,503		5,670
5%	5,209		1,503		6,712
8%	8,335		1,503		9,838

[1] 10% of Sales Increase

3. Asset Increase Not Financed by Profits and Payables

Profit	2.4 Turns	2.8 Turns	3.2 Turns
0%	($4,760)	($3,865)	($3,194)
2%	(2,676)	(1,781)	(1,110)
3%	(1,635)	(740)	(69)
4%	(593)	302	973
5%	449	1,344	2,015
8%	3,575	4,469	5,141

4. Amount That Can Be Borrowed While Maintaining a Constant Liability to Asset Ratio

Profit	Maximum Debt Increase	-	Payables Increase	=	Borrowing Capacity
0%	–		$1,503		($1,503)
2%	$2,084		1,503		581
3%	3,125		1,503		1,622
4%	4,167		1,503		2,664
5%	5,209		1,503		3,706
8%	8,335		1,503		6,832

Source: DATAQUEST, Inc.

7.4 Perspective

This section provides an overview of the distribution business. The various kinds of distribution in the United States are discussed briefly and industrial electronic distribution is placed in this framework. The salient financial and growth ratios of industrial electronic distributors are compared with those of other retailing and manufacturing firms. A short history of electronic distribution is presented and statistics are given on the growth of the electronics components, semiconductor, and distribution businesses.

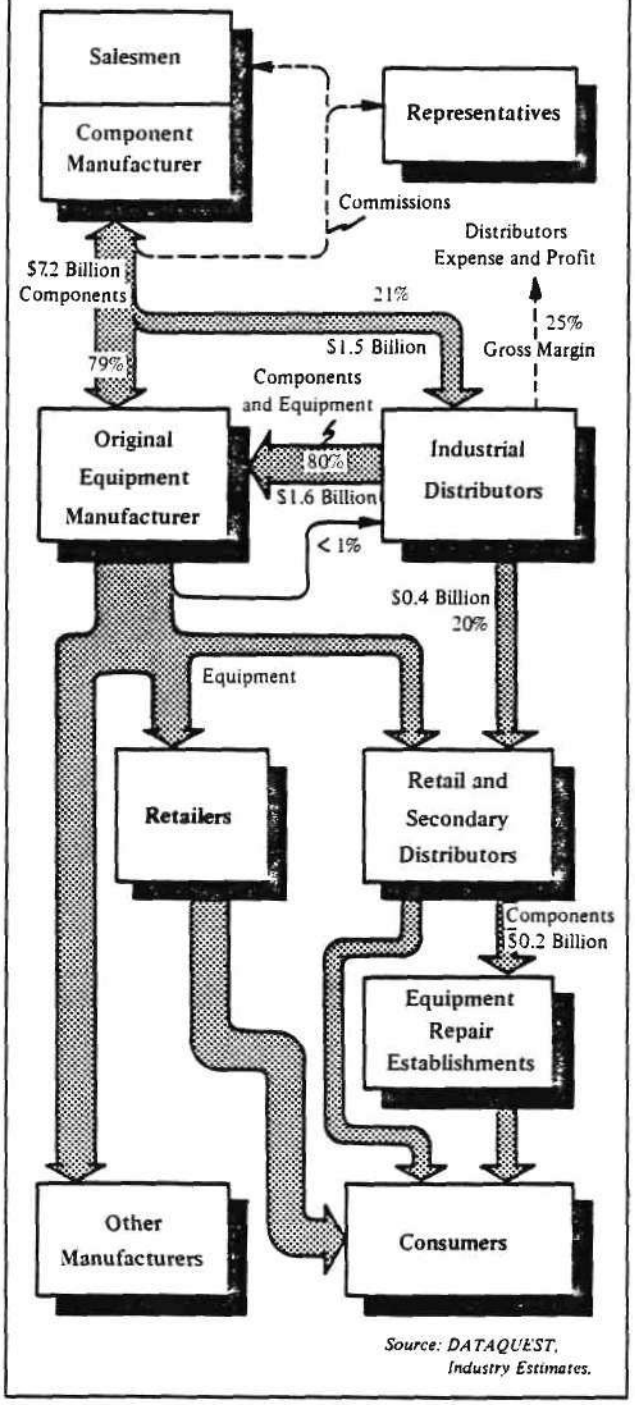
DISTRIBUTION–A DEFINITION

It is difficult for many to perceive why it costs so much to get food from the farm to the supermarket, or goods from the factory to the store. Moreover, the actual role of the "middleman" in this shipment of goods, and American business in general, is frequently misunderstood.

Figure 7.4-1 gives a simplified version of the complexities of industrial electronic distribution. Components' manufacturers sell about 79 percent of their output to equipment manufacturers, and 21 percent to industrial distributors. The diagram, for simplicity, ignores the fact that some components' manufacturers also make equipment; for example, National Semiconductor's memory division buys many components from distributors, even though National is a components manufacturer. The distributors sell an estimated 80 percent of their output to equipment manufacturers and the other 20 percent to retail and secondary distributors. Distributors' total sales are approximately $2.0 billion, accounting for a 25 percent mark-up over their $1.5 billion of component purchases. Again, the diagram ignores the fact that often the retail and secondary distributors may be part of the same company (though usually a separate profit center) as the industrial distributor.

Figure 7.4-1

FLOW CHART FOR INDUSTRIAL ELECTRONIC DISTRIBUTION



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The retail distributor is shown buying his product from the industrial distributor, which is common; however, it is possible that he might buy direct, or more likely on the gray market. Gray market components, for example, can be surplus sales of an equipment manufacturer or components that were obtained by culling and retesting the parts in a manufacturers' reject barrel. Some semiconductor companies routinely sell their rejects, and many of the functionally operable devices eventually become hobbyist kit parts. The original reject is unmarked and the hobbyist part will bear some brand other than that of the manufacturer.

The retail distributor sells to consumers (hobbyists usually) and equipment repair establishments such as television repair shops. This latter business is either stable or declining, since the advent of semiconductors has tended to either make products so reliable that repair is unnecessary, or so inexpensive that they are disposable items. Some distributors have left the secondary business because they see it as either stable or declining.

The consumer side of retail distribution has begun to emphasize the sale of equipment. Most retail distributors handle stereo, public address, ham radio, instruments for hobbyists, calculators, and other equipment, and consider these as their growth area rather than components.

The equipment manufacturer that buys from the industrial distributor may install the components in its own equipment and resell it. A small percentage of these components (8 to 14 percent) are used for the purpose of repairing equipment already in the field, which is called the MRO (maintenance and repair order) market. A small percentage of components are used by its engineering department for prototypes and are never sold again by the manufacturer to construct test equipment. This is called the R&D market.

The equipment manufacturer will frequently organize its purchasing department so that the components purchased for the production line are handled by a different buyer than those purchased for R&D maintenance and repair work. Since the resold components are higher volume, the bidding is more competitive. Moreover, the bulk of these components may be purchased factory direct at the larger accounts. Accordingly, these other equipment manufacturer markets can be lucrative for the alert distributor salesman.

COMPARISON WITH OTHER BUSINESSES

Industrial distributors buy from manufacturers and sell to other manufacturers. Since it is not necessary for them to produce a product, they need only warehouse and office space. Consequently, few of their assets are tied up in plants and equipment; instead, their major assets are in the form of inventory and receivables. These are current assets that have a more readily established value than do the plant and equipment assets of manufacturers. This has made debt financing relatively easy, and some distributors have had a tendency to overextend themselves and carry too heavy a debt burden. Distributors are able to generate more sales per dollar of asset than manufacturers since they have no plant and equipment; as a result, they can generate a reasonable return on assets while operating at a slimmer profit margin.

Distributors are more similar to retailers than manufacturers in terms of their employment of assets and profit margins. Table 7.4-1 compares and contrasts three types of companies and lists three manufacturers—General Motors, Intel, and National Semiconductor; two retailers—Sears and Mervyns (a west coast soft-goods retailer with 1976 sales of $194 million); and four distributors—Pioneer Standard (a regional distributor serving the market between but not including Chicago and New

7.4 Perspective

York), Wyle (a regional distributor serving the Western United States), Avnet (a national distributor), and Model (the paper construct of Section 7.3).

The Sales/Assets column of Table 7.4-1 that compares selected manufacturers, distributors, and retailers indicates distributors and retailers generate more sales per dollar of asset than manufacturers, even when the manufacturers are in such diverse businesses as automobile and semiconductor manufacturing. Sears is an anomaly in this case, since the consolidated sales include the insurance, finance, and savings and loan activities.

The second column—Cost of Sales/Inventory—gives an approximate measure of inventory turnover. Distributors surprisingly tend to have a lower ratio than the other businesses, which indicates that inventory stays on their shelves longer. Perhaps this results from the fact that products and product brands are identified with the manufacturer and not the dis-

Table 7.4-1

STATISTICAL COMPARISON OF SELECTED MANUFACTURERS, RETAILERS, AND DISTRIBUTORS
(From Latest Fiscal Year Data)

Company	Sales/ Average Assets	Cost of Sales/ Average Inventory	Receivables + Inventory/ Assets	Gross Margin	After-Tax Profit	Return on Average Assets	5-Year Compounded Sales Growth	P/E Ratio (Sept. '76)
Manufacturers								
General Motors	$1.72	$5.92	42%	16%	3.5%	6.0%	9%	7
Intel	1.53	3.76	49%	51%	11.8%	18.3%	80%	33
National Semiconductor	2.12	4.47	63%	32%	5.8%	12.3%	50%	23
Retailers								
Sears	1.21	4.42	61%	37%	3.8%	4.6%	8%	16
Mervyns	3.19	5.06	84%	30%	5.1%	16.2%	40%	15
Distributors								
Pioneer-Standard	2.55	3.37	83%	26%	3.8%	9.6%	20%	5
Wyle Labs[1]	3.20	4.30	90%	24%	–	–	19%	–
Avnet[2]	2.07	2.99	78%	31%	5.7%	11.5%	20%	7
Model Electronics	2.80	3.80	87%	25%	3.5%	9.8%	20%	–

[1] About half of Wyle's sales are in distribution. The numbers provided here are for its distribution business. Blank columns are left because these figures are available only for the entire corporation and are not directly comparable.

[2] The quantities entered for Avnet are for the entire corporation. Only 37% of the company is in industrial electronic component distribution.

Source: DATAQUEST, Inc.

tributor. Consequently, the distributor must emphasize its ability to deliver rapidly from stock on the shelf; if it does not have the part, the customer can always obtain it elsewhere.

The third column—Receivables and Inventory—divided by assets measures the fraction of the balance sheet that is tied up in these two current assets; it indicates that distributors have the highest ratio of the three types of companies. Again, they carry a higher stock than the retailer to avoid stock outages. The fact that these are current assets and easily valued gives distributors good borrowing power. Some distributors have overextended their use of debt, and have experienced problems as a result.

The Gross Margin, After-Tax Profit, and Return on Average Asset columns indicate that distributors can generate a greater return on assets with the same profit margin because they have more sales per dollar of assets. For example, Pioneer Standard has an after-tax profit margin equal to Sears, but has twice the return on asset because they have higher sales per assets dollar.

The Compound Sales Growth indicates the manner in which the businesses in Table 7.4-1 have grown in the last five years. Distribution's growth tends to be faster than that of large companies like General Motors and Sears, but somewhat less dramatic than some semiconductor companies.

MAJOR CHANGES OVER THE YEARS

The first electronic distributors entered business in the 1920s. They sprung up in "radio rows" all over the country; Courtland Street in New York is typical. They carried tubes, antennae, and ham gear, and served radio/TV repair shops and the electronic hobbyist or do-it-yourself advocate. Their stock was obtained directly from the manufacturers of components or from industrial or military surplus supplies, which was particularly important after World War II.

The industrial electronic distributor emerged in the 1950s as many original equipment manufacturers discovered that the radio parts stores could supply their small quantity components needs more rapidly than the component manufacturers. Since all radio parts stores did not necessarily cater to industrial accounts, some distributors began to specialize in them. Tony Hamilton was an important pioneer in industrial electronic distribution, and he currently heads Hamilton-Avnet's Electronics Marketing Group—the largest industrial electronic distributor.

Some of the original TV-shop distributors never did branch out into the industrial business and remain as they were in the 1950s; however, others like Pioneer Standard have entered the industrial market very successfully. Today, distributors recognize the differences between the industrial, repair, and consumer markets and will usually organize their efforts in these markets into separate profit centers when they are in more than one activity. Since the widespread introduction of semiconductors in consumer products, the market for components to repair consumer products has been static or declining, and some distributors have decreased their participation or withdrawn. The consumer/hobbyist market has expanded to include the sale of CB radios and stereo equipment as well as components.

Some distributors in the consumer and repair markets are now called secondary distributors because they often buy from industrial distributors. They are represented by an organization called NEDA—the National Electronics Distributors Association. Recently, NEDA has recruited most of the industrial distributors as well. Today, the distribution industry consists of some 1,500 companies at 5,000 locations; it has annual sales of $2.0 billion, with the top 14 companies responsible for 55 percent of these sales when only industrial distribution is con-

sidered.

The large industrial distributors have identified geographical markets and have developed internal market research departments to derive statistics about each purchasing area. They have grown consistently throughout the 1960s and 1970s.

In the 1960s, industrial distributors introduced value-added services. They perform limited testing, component assembly, connector construction, and component lead forming on premises, as well as instrument calibration and repair and PROM programming. This type of service has sometimes added value to the product distributors sell, but has not generally added profits because of competitive pressures. Value-added services are not expected to increase significantly from their approximate level of 5 percent of sales.

In more recent years, distributors have added computer systems, usually with interactive CRT terminals, to assist them in improving the productivity of inside sales and in reducing the costs of inventory control. Moreover, these systems provide accurate and current order status to their customers. This transition has not been painless; some distributors have achieved added profits only after delays in program development and others have only succeeded in mechanizing a system that was originally inadequate.

Recently, distributors have tried to increase their effectiveness in serving their high-technology manufacturers in such areas as microprocessors, optoelectronics, and bit slices. This is an arduous process because most franchises are essentially nonexclusive, and it is difficult to recover the investment made in engineering sales calls. The addition of new products that are sold to engineers and not to buyers should alleviate this problem; these products include panel DVMs, microprocessor design systems boards, and power supplies.

With the concentration of larger industrial distributors on semiconductor products, opportunities have developed for smaller, specialized distributors in passive and electromechanical components. These opportunities are excellent and should proliferate.

GROWTH RECORD

As the components market has grown, the industrial electronic distributors have accounted for a larger share of the components sales dollar. This is illustrated in Table 7.4-2, which shows the distributor's share increasing from 9 percent in 1961 to 21 percent in 1976.

Distributors have increased their share of the components market primarily due to pressure exerted by the component suppliers. Suppliers have regarded distributors as a convenient, low-cost sales outlet for their product; they have taken the initiative in most cases and have even designed products specifically for distribution. Many of the value-added services mentioned in the previous subsection were conceived by component manufacturers to reduce local inventory. For example, a distributor can stock subparts of potentiometers and connectors and build up a multiplicity of part types by assembling various permutations and combinations of the subparts.

In the last 15 years, distributors have increasingly initiated or participated in sales at quantities above those given on distributor price lists. Motorola was one of the early manufacturers who encouraged these sales through VPAs—Volume Purchase Agreements. Some distributors have welcomed the larger volume enthusiastically, and the average order size handled by manufacturers has been increasing as a result.

7.4 Perspective

Table 7.4-2

ESTIMATED DISTRIBUTOR'S SHARE OF U.S. FACTORY SALES
(Dollars in Millions)

Year	Total Component Sales	Distributor Share	U.S. Semiconductor Sales[1]	Distributor Share[1]
1961	$3,100	9%	$ 525	10%
1966	5,500	12%	1,010	12%
1971	4,770	19%	1,160	16%
1976	7,200	21%	2,400	26%

[1] Distributor sales are at distributor resale prices.

Source: EIA, DATAQUEST, Inc.

7.5 Equipment Manufacturer's Profile

Original Equipment Manufacturers (OEMs) are the principal customers of the industrial electronic distributor. These manufacturers of electronic equipment vary considerably, but they also share certain common problems. This section describes equipment manufacturers and the business pressures that motivate them in order to provide better insight into the distributors' principal market.

A considerable lack of empathy sometimes exists between the components manufacturer and the OEM, particularly if the components manufacturer happens to be a semiconductor company. A reason for this communication problem is differing procurement aspects of the two businesses. For example, a semiconductor company typically needs to buy only silicon, packages, and expendable materials (industrial gases and chemicals) to produce its product. The dollar volume of purchases of the semiconductor company may be a smaller portion of net sales than for the OEM, and the mix of items bought may not depend so strongly on the actual products sold. Conversely, the OEM will often have thousands of different parts in a single product; all of these must be obtained in a timely manner if the product is going to be shipped on schedule. The lack of a single part can stop his production line. Furthermore, the mix of parts to be purchased depends on the mix of products to be shipped; thus, a strong linkage between sales and purchasing is evident.

DESCRIPTION

An OEM is in the business of buying, putting together, and selling assemblages of electronic components. Considerable time is spent in procurement, incoming inspection, construction, test of the finished product to eliminate inoperative parts, and analysis of components that fail in the field. To a large extent, any reputation that his product may have in terms of quality will depend on how conservatively he applies the components and how adequately he screens them.

A diverse range of OEMs buy from distributors. An OEM could be a moonlighting engineer working in his garage, or an employee of one of the small, rapidly growing, high-technology companies just completing a new microprocessor-based product. Distributors prefer the rapidly growing companies because their sales are often product limited; therefore, they are more concerned about product availability than price. Furthermore, rapid growth causes them to be more dependent on the services a distributor can provide. Sometimes these small companies mature and no longer have high growth rates, but still represent profitable distributor accounts.

Many companies which are not involved in electronics as their basic business are now beginning to purchase electronic components; these include machine tool manufacturers and makers of knitting machines. This type of company often combines purchasing acumen with a lack of component knowledge and as a result is a good customer for the services distributors provide. The large electronic OEM, on the other hand, is usually professional in both component application and procurement and may limit the amount of his purchases through distributors. However, he will often depend on distributors during times of crises and shortages. He may also represent a good-sized account in the areas where he buys components that do not go into his equipment; these include components for research and engineering, for in-house constructed test equipment, and maintenance and repair (MRO) components.

Finally, there are large military equipment manufacturers such as Lockheed, North American Rockwell, and Hughes; they buy prototype parts from distributors. Production quantity parts are specialized because the parts must be screened to military specifications. There is one

distributor in Los Angeles—Hi-Rel Distributor Sales—that handles military grade components almost exclusively, which are specially marked with JAN and JANTX designations to indicate they have undergone specialized testing for military uses; they command substantially higher prices. Counterfeiting of the special markings has been a recurrent problem in the industry.

Components are procured from a bill of materials. Usually, each product has a separate bill of materials, except at larger OEMs where they may be combined. This bill of materials lists the different items and the quantity required of each to build a given assembly of the OEM's product. In the area of electronic components, the assembly is usually a printed circuit board. The bill of materials will typically contain 50 to 500 types of components, and since each type of component is listed on a separate line, they are sometimes called line items. A single piece of equipment may have several bills of material, and frequently a target cost the buyer must meet will be established for the bill of materials.

The engineering department is responsible for the design accuracy of the bill of materials. Engineers select the components initially and subject prototype equipment to limited testing to verify its performance. The parts are selected to satisfy many criteria: they usually must be manufactured by two or more components suppliers to insure availability; they must be up to date technically to ensure competitive performance of the resultant product; and they should have the lowest possible cost.

The component is almost always specified on the bill of materials by a part numbering system that is unique to the OEM. This is necessary because all his numbers must be structured in the same manner to ensure handling by a common manual or computerized filing system. In many companies the component manufacturer's part number will not appear on the bill of materials; as a result, it is necessary to go to the components file to obtain this information.

The components engineering department is separate from design engineering. Components engineering is responsible for maintaining the OEM's file of approved components. Design engineering cannot use a new component type in a product unless it is first approved by components engineering. The components engineering group is responsible for the availability and reliability of components listed in the components file, but is not so concerned with performance. It maintains the components file that lists the OEM's part number, the component description, and the approved vendors and their part numbers. A well-known vendor will frequently not be approved for certain components because of a real or imagined reliability problem he has with this type of component. Many component vendors use the same part number to help the OEM order from multiple sources. For this reason, OEMs believe it is desirable to keep the vendor part number off the bill of materials so that components will not be inadvertently ordered from a vendor who is not approved.

It had been a common practice for OEMs to procure many of their parts, particularly semiconductors, to special part numbers. The special part might be nothing more than a standard transistor with either tightened or sometimes loosened parameters. This practice allows component manufacturers to charge different prices for what is essentially the same product; it also eliminates the distributor's function. This practice has been less common on integrated circuits and LSI components because it is not as usual to test to different performance limits. OEMs have increasingly favored generic part types because of the procurement flexibility that this practice allows.

Many OEMs find that the least expensive way to maintain the quality and reliability of

their equipment is through use of an approved vendor list. A part must usually undergo qualifications testing to be put on the list; furthermore, the reliability of components in the field will also be monitored. Small manufacturers do not engage in qualification testing and will often rely solely on either field experience, experience in testing prior to shipment, or their knowledge of component reliability gained as a result of previous experience.

Reliability engineering is also concerned with components selection. They will perform qualification testing and are called in to advise when field problems occur. Many commercial companies have no reliability engineering, but simply depend upon their experience with approved vendors. They are more likely to have a components engineering group, although the design engineer may be expected to perform this function. Service companies exist that will do reliability engineering on a contract basis for those who have no internal reliability department.

The OEM's quality assurance department is responsible for testing his product before introduction to ensure its integrity. When the product is in the manufacturing process, they monitor the production line to ensure that incoming inspection, assembly, and pre-ship testing of the product is conducted properly. Incoming components usually will not be 100 percent tested; instead, only a small sample of the product will be tested. Quality assurance will decide what to do with a "lot" of components if a sample taken from that lot does not perform correctly. They may return it to the manufacturer.

The OEM's purchasing department is responsible for negotiating purchases and for obtaining the necessary quantity of the correct components to the assembly floor at the right time. Purchasing is under constant pressure to minimize the investment of the company in raw materials; they are always mindful of the fact that *one* missing component can stop the production line, causing the company to incur losses that offset the money saved through months of careful negotiation. There is usually not a large enough staff in purchasing to enable the OEM to deal directly with each manufacturer. It will tend to favor distributors, especially those who encompass the largest portion of its bill of materials.

Many OEMs are not able to forecast the acceptance of their equipment in the marketplace precisely. They are commonly in a situation with excess product or with unfilled demand, and purchasing must work closely with sales to keep informed. The build and procurement schedules are normally revised every 30 days and run for six months; purchasing agents prefer flexible arrangements that will allow them to make these changes.

The smaller OEMs are underfinanced and may be credit risks, particularly those who are growing rapidly. A local distributor who can determine the viability of the OEM's product is in a good position to make a credit judgment.

THE SIGNIFICANCE OF SEMICONDUCTORS

The semiconductor industry has been the technology leader in electronic components (see Chapter 1 of this notebook for a discussion of the industry). It is an industry characterized by rapid technological advances coupled with rapidly falling prices, which on a given part may be 15 to 20 percent a year. Sometimes price cuts occur in the face of shortages as suppliers bid for business in the hope that they can supply in the future. In recession years, price competition may cause the industry dollar volume to shrink even as the number of parts shipped continues to expand.

Semiconductor parts are selected first when a new piece of electronic equipment is being designed; they are the active component

7.5 Equipment Manufacturer's Profile

and largely determine the performance of the equipment. Other components are selected after the semiconductor devices have been chosen. These components are frequently bought from the same distributor that supplies the semiconductors, if he has done the proper sales work. This type of business is called "drag business" because semiconductor sales "drag in" sales of other components.

Heavy pressure always exists on the price of semiconductor parts, which comes from two sources. First, semiconductor parts comprise 50 to 80 percent of the cost of components mounted on PC boards. The engineer and/or the purchasing agent often have a target cost number for each PC board assembly, and the largest cost item offers them the most fertile ground for cost reductions. Second, purchasing agents have learned from experience that the prices of semiconductor parts are "softer" than those of most other components. Effort in negotiating semiconductor prices is more likely to yield the price reduction that justifies the buyer's function than is effort on any other item.

OEMs often aggregate their semiconductor requirements into a single annual or semi-annual requirement and put it out to bid. Distributors will usually write a contract that allows the purchasing agent to change the quantities of individual parts providing the aggregate dollar amount of the contract is met; these are called "mixing privileges." If the OEM does not purchase the aggregate dollar amount agreed to, then a provision is created that specifies an added amount to be paid at the end of the period; this is called the "bill back" provision. In many cases where the contract quantities are not met (maybe 95 percent of the time), bill back is not exercised; instead, the distributor or supplier settles for another order.

Because of the focus on semiconductors by the OEM's purchasing agent and engineer, there is a tendency to neglect the other components. For example, engineers may not fully understand capacitor voltage ratings, and the purchasing agent may neglect to purchase some of the passive components until shortly before he needs them. Since there is less time for negotiation and since these passive components may be a smaller percentage of system cost, price pressure is less likely, which creates opportunities for the smaller distributor of passive components.

Semiconductor parts have historically caused most of the electronic component availability problems. Semiconductor manufacturers do not create these problems intentionally, but the technological changes are so rapid that they sometimes introduce a product before its performance or reliability is thoroughly tested, or before production problems are solved. These problems then are discovered by OEMs in the field, and could be so severe that the OEM might believe that it was prudent to withdraw the offending component from his product; this could be accomplished only if a second source was available.

Semiconductor problems are sometimes process oriented rather than design oriented. Manufacturers have been known to "lose the process" and be unable to manufacture parts on a given line, e.g., the N-channel silicon gate line. If the process is not completely lost, it may be affected in a manner that could reduce the yield and hence the throughput. Again, the result is an availability problem that the semiconductor manufacturer resolves by allocating his output; the OEM would be in difficulty without a second source.

In the process of defining new products, the integrated circuit or LSI manufacturer may choose a configuration that he believes will be accepted in the marketplace. The product may sell well for the first few months as OEMs buy samples for their breadboards, but it may never "take off" and become a high-volume part. Some 12 to 18 months are required for a new part to be designed in and reach production

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volume; therefore, a relatively long period of uncertainty exists. Again, if two sources supply the product, the OEM designer is at least assured that more than one manufacturer thought there would be a market for the product, which could result in it being produced in volume. If the product is never produced in high volume, it is likely to be much more expensive than similar high-volume parts.

The cost penalties paid by the OEM for choosing the wrong part are high. For purposes of illustration, Table 7.5-1 compares the prices of selected members of the popular low-power schottky TTL family (54 LS) with equivalent members of the less popular low-power TTL family (54L). Note the premium that would be paid by an OEM who committed his design to the 54L series.

Semiconductor availability problems may arise from design weaknesses, loss of process, or simply because the part never becomes popular enough to be high volume. Most of these problems disappear if the OEM carefully selects parts that are multi-sourced. Semiconductor companies strive to meet this demand for multi-sourcing. For example, many manufacturers use the same part numbers to aid in the generic identification of their products. Unfortunately for the semiconductor companies, multi-sourcing also makes procurement more competitive. This helps account for the observed rapid decline in semiconductor prices.

Table 7.5-1

COMPARATIVE PRICES FOR LOW POWER AND LOW POWER SCHOTTKY TTL (100-999 Units, January 1977)

		Low Power Schottky TTL 54LS	Low Power TTL 54L
Quad 2 Input Nand	(00)	$ .55	$1.15
Hex Invertor	(04)	.60	1.25
Dual J-K	(73)	1.25	1.92
Triple 3 Input Nand	(10)	.55	1.15

Source: DATAQUEST, Inc.

Passive component technology advances less rapidly than semiconductor technology. As a result, passive components have fewer availability problems and there is a much weaker demand for multi-sourcing. For example, some capacitors have unique terminal placement or voltage ratings, some switches and keyboards have no second sources that are 100 percent interchangeable mechanically, and almost all cabinets differ among manufacturers. This situation again creates opportunities for the distributor of passive components.

Semiconductor parts have relatively high incoming failure rates. OEMs report failure rates in the 2 to 7 percent range for simple gates and flip-flops. This low-quality level may be due to the pricing pressures in the semiconductor industry, with some manufacturers regarding reduced quality control as a way of reducing cost.

Incoming inspection failures may be due to a lack of correlation between the OEM's test equipment and the component manufacturer's test equipment. Obtaining effective test correlations between OEMs and semiconductor manufacturers has always been a problem. Most distributors do not test semiconductor products and avoid entering discussions of differing test results as much as possible.

The high incoming failure rates of semiconductor parts are costly to OEMS; consider a printed circuit board with a number of integrated circuits on it. Table 7.5-2 gives the number of assembled printed circuit boards that

will not work when they are first turned on and that will therefore have to go to a technician for troubleshooting and rework. Note the dramatic increase in the rework rate as the number of ICs and failure rate increase.

Rework causes the following two problems. First, good technicians are scarce and it takes them considerable time to learn to debug a complex product efficiently. If high production rates are planned, the delay needed for technician staffing and training could slow product introduction by several months. Second, the costs of debugging are high; for example, a technician who debugs eight of the 20-component boards a day might cost $6 an hour direct and $18 an hour when fringe benefits and overhead charges are added to his base salary. Table 7.5-3 gives the cost per component of reworking the printed circuit boards. Although the cost to rework each bad board is fixed, the cost per component is reduced at lower failure rates because fewer boards need to be reworked.

These rework costs have been recognized. In the San Francisco Bay Area, several companies are now established who offer the testing and inspection of semiconductor components as a service. They charge between $.05 and $.10 per part for simple room temperature tests, with the price depending on the complexity of the test. This rate can be economically justified by Table 7.5-3 at failure rates above 1 percent, if direct costs are used.

OEM/DISTRIBUTOR RELATIONS

To some extent, OEM's attitudes towards distributors reflect the popular bias in the United States against middlemen in general. Most consumers seek to buy products at cost and resent the fact that they must pay the Ford dealer more than Ford, and the supermarket more than the farmer. However, consumers patronize the dealer and the supermarket because

Table 7.5-2

REWORK LEVEL OF PRINTED CIRCUIT BOARDS AT VARIOUS INCOMING FAILURE RATES

Number of Integrated Circuits on Printed Circuit Board	Percent of Printed Circuit Boards Reworked at Various Integrated Circuit Reject Levels			
	1% Rejects	2% Rejects	5% Rejects	7% Rejects
5	5%	10%	23%	30.0%
10	10%	18%	40%	52.0%
20	18%	33%	64%	77.0%
50	39%	64%	92%	97.0%
100	63%	87%	99%	99.9%

Source: DATAQUEST, Inc.

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Table 7.5-3

COST PER COMPONENT TO REWORK A 20 INTEGRATED CIRCUIT BOARD AT VARIOUS INCOMING FAILURE RATES

Number of Integrated Circuits on Printed Circuit Board	Cost of Printed Circuit Board Rework Per Incoming Component at Various Incoming Failure Rates			
	1%	2%	5%	7%
20 with overhead:	16.2¢	29.7¢	57.6¢	69.3¢
20 direct cost:	5.4¢	9.9¢	19.2¢	23.1¢

Source: DATAQUEST, Inc.

there is no other choice.

Similarly, smaller OEMs have no choice but to deal with distributors. The components manufacturer will not handle orders below a given annual dollar volume, preferring instead to refer these orders to his distributor. The size of order that will attract the attention of the component manufacturer has been increasing, which cause some accounts that were formerly direct to go through distributors. The OEMs commonly resent being forced to deal with the distributor and pay his additional mark-up; they usually attach little value to the credit, expediting, and local inventory services the distributor provides.

These OEMs find that when a crisis occurs, they receive little or no technical assistance from the distributor and must go to the factory for assistance even though they buy from the distributor. The factory tends to ignore these assistance requests because it has no day-to-day contact with the OEM. This situation can become frustrating, especially when the OEM suspects the distributor has had trouble with the same part at other accounts but did not pass the information on. Distributors, on the other hand, commonly believe that it is unwise to circulate information about faulty components, partly because accuracy is unlikely and partly because they do not wish to offend their suppliers. Instead, they recommend the OEM protect himself by training his engineers to take the necessary safeguards to avoid component problems, as well as making judicious use of independent test houses.

Since most OEMs realize that distributors merely inventory a manufacturer's parts, they do not regard the distributors' decision to stock as an endorsement of component quality. Therefore, they select the distributor primarily for the services and support he can offer; these include, in estimated order of importance:

- Breadth of the distributor's line
- Past record of meeting delivery commitments
- Responsiveness of salesman when expediting is needed
- Ability to expedite the factory
- Price

The purchasing agent is the principal point of contact with the distributor and most of the items on the list above reflect his concerns for

completing the job. He naturally selects the distributor that he considers the most effective. Price is at the bottom of the list, not because it is unimportant, but because many purchasing agents believe that prices are so competitive that they are not the determining factor in selecting a distributor. Breadth of line does not mean that the distributor with the broadest line is selected; instead, the OEM chooses the distributor whose line encompasses the largest portion of his bill of materials. Thus, he reduces the number of distributors he must deal with on an ongoing basis and cuts purchasing overhead.

One of the arts of distribution is to reduce the number of manufacturers stocked while maintaining breadth of line. This can be accomplished by eliminating manufacturers with overlapping product lines and by influencing the OEM's selection of components. The distributor has some flexibility in this regard because most OEMs now allow the distributor to choose the brand of component he wishes to supply (which is obviously subject to the OEM's approved vendor list).

OEMs expect distributors to help them manage the assets that they have in components inventory. The distributor provides this assistance by:

- Special stocking arrangements
- Flexible purchase agreements
- Ability to handle changes in schedule
- Flexibility in credit arrangements

Control of parts inventory is extremely complex and many OEMs find it difficult to accomplish. In the inventory crunch of 1974-75, even the largest OEMs lost control and had to write off millions of dollars of components inventory. Distributors, with their increasing sophistication in computer control of inventory, have a valuable service to offer.

Distributors, like the local bank, offer a local source of credit that is greatly appreciated by small OEMs, who often cannot obtain any other type of financing. An astute distributor, who is in closer contact with local OEMs than a remote components manufacturer, has a firm understanding of trends in the electronic marketplace, and who can judge the viability of his customers' products, can safely offer credit to OEMs even though their financial statements are in marginal shape.

Most OEMs try to run their purchasing departments in a professional manner and avoid personal contacts which might influence the purchase decision. Nevertheless, purchasing agents will still seek to have good rapport with distributor salesmen. In a minority of accounts, the purchase decision may be made in a less professional manner.

7.6 Distributor Profile

Alfred P. Sloan, Jr., in his book, My Years with General Motors, addressed the question of why the automobile industry adopted the franchised dealer form of retail distribution. He states that with the advent of the used car trade in the 1920s, "The merchandising of automobiles became more of a trading proposition than an ordinary selling proposition. ... Trading is a knack not easy to fit into the conventional type of managerially controlled scheme of organization." Sloan acted on his belief that auto dealers should be independent of the auto manufacturers and was concerned about establishing policies that would allow his dealers to function as profitable, independent businessmen. Sloan's chapter, *Distribution and the Dealers*, describes so many problems of automobile distribution in the 1920s that they frequently resemble those same problems of electronic component distribution in the 1970s.

The "trading knack" is as important in electronic distribution as it is in auto dealerships. It is difficult to determine when a salesman has the "trading knack." The most popular litmus test is the one that measures the number of orders closed. The pervasive use of this test may help to explain why successful distributor salesmen enjoy rapid increases in salary and are likely to be recruited by other distributors.

One of the major problems for distribution management is the development of an environment that will allow the "trading knack" to flourish; this requires a more entrepreneurial environment than that of the component manufacturer. Incentive plans of various kinds are used for this purpose including profit sharing, commissions based on sales or gross margins, retirement plans, and ROI compensation for general managers. More important perhaps than the details of a specific plan is the method by which it is implemented. The individual who participates in the plan must truly believe that his performance is important to the success of the business and that his contributions to that success will be rewarded fairly and impartially.

This section provides a profile of the industrial distributor and the environment within which he works. It describes his role, the manner in which components sales are approached by the components manufacturers' salesmen, representatives, and distributor salesmen. Lastly, it discusses relations between the distributor and the component manufacturer.

CLASSIC DISTRIBUTOR ROLE

The classic distributor role is to provide service to the OEM buyer. Service is of utmost importance because the distributor has no means of product differentiation. Therefore, he must provide better service to set himself apart from other distributors who handle the same or similar products.

The distributor's economic reason for existing is that he can market small quantities of the component manufacturers product less expensively than can the component manufacturer himself. This occurs because the distributor is able to share his order entry and warehousing expenses among many components manufacturers. Moreover, the distributor provides a ready outlet for products. Manufacturers can introduce new products without making any investment in a national sales organization, which conserves their capital and lowers the risk of loss.

The services an industrial distributor provides to an OEM are intended to help him solve some of the problems discussed in the previous section. They include:

- Supply of Printed Technical Information
- Simplification of Purchasing
- Anticipation of Trends
- Local Stock
- Acting as a Bank

7.6 Distributor Profile

- Fixed, Fair Prices
- Service after Sales

Printed technical information includes catalogs, application notes, and data sheets. This information is supplied by the distributor salesman to the design engineer and is most effective when presented in a selective way, so that it actually helps the engineer solve a problem on which he is currently working. Printed matter may often be supplemented by technical seminars. Generally, the distributor arranges the seminar and supplies the audience and meeting place, with the actual lecture given by an expert from the manufacturer.

Simplification of purchasing is achieved because the existence of the distributor makes it possible for the OEM's purchasing agent to buy from many different component manufacturers with one purchase order. Flexible purchase agreements and the ability to respond to the OEM's changes in schedule are important as well.

Anticipation of trends allows the distributor to have ample stock on hand before the demand begins. This may help to smooth the component manufacturer's production cycle and provide available parts to OEMs when there might otherwise be none.

Local stocking allows the OEM to carry a portion of his inventory at the distributors, which thereby lowers his carrying costs.

By acting as a bank, distributors provide a ready source of credit to small OEMs, which they could not obtain elsewhere. The distributors presence as a *local* businessman helps him make accurate credit judgments.

Fixed, fair prices develop because distributors sell from price lists established by their manufacturers, which are for small quantity purchases (generally a maximum of 100 or 1,000 units). They allow purchasing agents to obtain components at a reasonable price when the order is too small to justify any effort at negotiation. Certainly, price cutting from these price lists does occur; however, when the practice is widespread on a given component, the list is usually revised. As a result, the competitive pressures help to keep the price list fair. When a component manufacturer reduces list prices, he usually maintains the gross margin so that the distributor's profitability will be unaffected.

In the last 15 years, the trend has been for some distributors to handle an increasing volume of above-list price sales, perhaps as high as 50 to 60 percent of their total sales (see Section 7.2, **THE MISSING MIDDLE**). This may reduce their list price sales as OEMs will buy a percentage of extra components on the Volume Purchase Agreement for maintenance and repair and laboratory stock (these components were formerly bought at distributor list prices). The distributor is then asked to provide the same service on this stock that he formerly provided on stock purchased at list price. Since volume margins are smaller, this practice has a tendency to pressure distributor profits.

Service after sales is important to the OEM's purchasing agent. When the OEM's new product first starts down the production line is when he discovers shortages, sometimes due to his own omissions. Stopping the production line for the lack of components is expensive and purchasing agents appreciate and value the distributor's help in providing shipment status, expediting shipments, handling changes in requirements, and searching for scarce parts or good substitutes.

COMPONENTS SALES

Electronic components are sold by three different classes of people:

- Factory Salesmen
- Factory Representatives (Reps)
- Distributor Salesmen

7.6 Distributor Profile

Factory salesmen typically work on a salary with an override commission. This commission is payable on all orders in the salesman's territory even when a distributor handles the sale. Where the equipment is designed in one salesman's territory and produced in anothers, the commission on components purchased for production may be split. Since these salesmen represent only one manufacturer, they frequently are highly motivated to work closely with the design engineers during product design, and spend only a fraction of their time closing orders. Where the order size is appropriately small, they work closely with their local distributors and provide assistance to them. Factory salesmen carry no local inventory, but do offer free samples.

The representative is legally an agent of the component manufacturer. He does not buy the product from the manufacturer and resell it to the OEM; instead, he takes orders on behalf of the manufacturer. His role is justified by the fact that he usually represents more than one noncompetitive manufacturer. Thus, he can provide a sales presence in the territory more inexpensively than either manufacturer could provide it for himself. His agency agreement with the manufacturer specifies a territory and a commission. The commission is approximately 5 percent and is payable on *all* orders in his territory, even if a distributor handles the sale; it may be split in the same way a factory salesman's commission may be split. Reps have been known to build very lucrative territories, and in some cases have higher incomes than the component manufacturer's sales manager. Manufacturers are reluctant to replace reps with factory salesmen in these cases because the order rate in the territory usually falls off due to the new man's lack of personal contacts, or experience. Since the representative's business is of such a personal nature, it usually cannot be sold to someone who would lack the necessary contacts.

The representative works similarly to the factory salesman. He too is highly motivated to get the product designed in. Perhaps his incentive is not quite so high as that of the factory salesman, for he can always shift his attention to some other line that requires less effort on his part. Reps tend to have a technical background, work closely with design and specifying engineers, and spend only a fraction of their time closing orders. They too work closely with local distributors and provide assistance where necessary. Reps generally carry no local inventory, but do offer free samples.

The distributor salesman works for the distributor who is an independent businessman and is not an agent of the manufacturer. He buys from the components manufacturer and resells to the OEM. He is a franchisee of the manufacturer under the terms of the Wright-Patman Act; this Act generally requires that the same item be sold to members of the same class of purchasers at the same price. The components manufacturer is permitted to sell his product to the distributor for less than he sells it to the OEM because the two are members of a different class. The manufacturer publishes a price list that gives prices usually up to the 100- or 1,000-piece quantity. Each item will be sold to the distributor at a single price, which is less than the list price for that item. This discount averages 25 percent in the industry; it depends on the price list quantity break and varies from item to item. Although the distributor works on a gross margin basis, he in turn compensates his salesmen on a salary plus override commission basis.

The distributor salesman essentially has no territorial protection, which is unlike the representative or factory salesmen who draw a commission whether they sell the product or not, providing the sale occurs in their territory. Once a distributor has purchased a part, his salesman

is free to sell it to anyone he chooses. With the advent of computer-controlled inventory and air shipment, it is not uncommon for an OEM in California to buy from a distributor in Chicago. However, most of a distributor's sales usually come from his local geographic region. He may have a "territory" for all practical purposes if his component manufacturers franchise only one distributor in that geographic region.

Distributors often carry competing lines; this is particularly common in semiconductors because OEMs demand multiple sources (see Section 7.5, **THE SIGNIFICANCE OF SEMICONDUCTORS**, for a discussion of causes). Once the distributor stocks competing lines, the component manufacturer will franchise additional distributors in the same area to ensure his market penetration. The stocking of competitive lines occurs in most commodity products, such as semiconductors, resistors, and capacitors, but is less common in proprietary products like cables and connectors. Most distributors try to stock proprietary products as well as commodity products.

Distributor salesmen commonly have less incentive than representatives to get a given manufacturer's brand designed in. Particularly in commodity products, they may elect to supply another brand themselves or may ultimately lose the purchase order to a competing distributor who stocks the same brand. They do have an incentive to get their company's product mix well represented, since purchasing agents tend to choose the distributor whose products cover the largest portion of their bill of materials. The methods they use to accomplish this include keeping the OEM's engineers well supplied with technical literature and by inviting them to technical seminars. When their products are not on the approved vendor list, they will strive diligently to see that those brand names are represented. Distributor "outside" salesmen generally make better penetration into all departments of a company when it is small enough to buy most of its products from distributors. In the larger companies, factory salesmen and reps tend to cover the OEM's design activities.

Distributor salesmen spend the bulk of their time with purchasing agents, and they are successful if they can close orders well. Distributors report that they have many successful salesmen who have little or no technical background; however, their ability to communicate effectively is of primary importance. This ability can be acquired if the salesman can pick up new technical jargon relatively quickly. Distributors employ staff specialists in microprocessors and other fields to assist and train their salesmen.

Stocking representatives represent a fourth type of sales organization. They are a combination of a representative and distributor, and are usually specialists. An advantage is that they can combine their distributor-type sales calls with their rep-type sales calls. They also have an effectively exclusive territory for the distributor side of the business if they rep the product that they also distribute. They represent a small fraction of total industrial distribution sales volume.

DISTRIBUTOR/MANUFACTURER RELATIONS

Component manufacturers are the driving force behind many of the changes in electronic distribution. They force customers for the distributors as well as changes in the distributors' internal operations.

Customers have been directed to distributors by component manufacturers who are reluctant to add sales staff as they add new products and who generally believe that distributors can process orders at a lower cost. Semiconductor manufacturers, who must constantly seek larger markets to compensate for lower unit prices, have encouraged distributors to

7.6 Distributor Profile

work with the higher volume accounts.

Changes in the distributors' internal operations have included the addition of value-added services, PROM programming, and microprocessor centers. Distributors added these new functions at the insistence of component manufacturers who sold them on the idea with promises of added profits. Distributor pricing policies commonly were not considered in advance and the distributor found himself providing a new service without added compensation. These problems have eventually tended to resolve themselves.

Component manufacturers frequently believe that distributors are not loyal to their products because they often handle competitive lines. They also do not like distributors to criticize their products. Distributors, for this reason, usually try to avoid discussions about factory quality and rejects; instead, they prefer to have any negative information flow directly from the customer to the factory.

Conversely, distributors resent their manufacturers' frequent lack of distributor loyalty. They believe some manufacturers franchise many distributors in the same geographical area until the result is that no one can make a profit. They believe that some manufacturers do not give all distributors equal attention and that they sometimes use the distributor as a dumping ground for excess production.

Distributors are also of the opinion that most component manufacturers do not understand the value of the services they provide. They are particularly concerned when their average 25 percent gross margin is compared with the typical 5 percent rep commission. The services that they provide to the manufacturer that the rep does not provide include:

- Reduction of the component manufacturers' finished-goods inventory
- Providing customer credit
- Prompt payment for components purchased
- Feedback of current market trends
- Presence at small accounts

This comparison of commission to mark-up is particularly inappropriate because the rep draws a commission on distributor sales.

Distributors may believe that they are "last on the list" during times of component shortage when it becomes necessary for component manufacturers to allocate their output. This is one of the reasons that distributors tend to be prompt in their payment to the manufacturer; however, they are not above taking advantage of all invoicing delays to maximize their efficient use of assets. Typically, sales to distributors are on 2 percent, 10-day terms, but with normal billing cycles, this amounts to a 30-day receivable.

Astute component manufacturers realize they must create a demand for their product outside the distribution channel. This is called "pull-through" because this outside demand is said to pull the parts through the distributor. This could be accomplished by the in-house sales staff, by publication of technical articles, and by advertising.

Most manufacturers have one man who is totally responsible for distributor sales, and he may have one or two assistants. His job is to capture the attention of the distributor salesmen, and an advertising and promotional budget is provided for this purpose, which may run 1 to 2 percent of distributor sales. He may sponsor cooperative advertising, which shares the cost with the distributor and shows both companies in the ad. He may offer incentive programs for the distributor salesman who sells the most of a given product. Finally, he will run sales meetings periodically to promote his company's product to the distributor's salesmen and product managers.

The component manufacturer's distributor sales manager is also responsible for management of returns, price protection, receivables,

7.6 Distributor Profile

stock rotation, and for monthly sales analyses. This is a complex problem in the dynamic electronics components marketplace. One manager described a component whose price had been reduced twice in such a short period of time that he had price protection credit memos two generations deep. Some component manufacturers are never able to straighten out the price protection accounting problem, and all rely on computers to help them keep informed of the situation. They believe that distributors will take advantage of any errors on their part to lengthen receivables and obtain the maximum price reductions.

Component manufacturers' sales to distributors are actually not final because of the virtually universal provision for price protection. This clause in a franchise agreement usually provides that the component manufacturer will issue credit to the distributor for his stock when price reductions occur; this credit is equal to the number of items in stock multiplied by the price reduction. Distributor sales are actually not final because of this clause. Several component manufacturers lost heavily in 1974-5 because they had recorded distributor sales and later had to reverse profit entries when price protection clauses became operative. Currently, however, some manufacturers—including AMD, Intersil, and Intel—take the sale only when the distributor moves the product off his shelf, although they will obviously take the cash as soon as possible. Others, like Hewlett-Packard, simply watch their distributor inventories very closely. In any event, DATAQUEST does not believe that this change in accounting policy will reduce the willingness of component manufacturers to deal with distributors.

7.7 Companies

OVERVIEW

This section discusses specific companies. First, the companies that we believe are the 14 largest industrial distributors are compared and contrasted to achieve an overview of their general similarities and differences. Five of these companies are then selected for analysis in greater depth.

Industrial distributors exist in some measure to provide the convenience of a local inventory of electronic parts to their customers. Competition for market share tends to be on a local basis, and a local distributor can compete successfully with a national distributor if he has a more intimate knowledge of his territory.

Figure 7.7-1 gives a graphic presentation of the stocking locations of the 14 largest distributors. In this figure, it is obvious that Hamilton-Avnet and Cramer are truly national in scope. Schweber and Kierulff have roughly half as many outlets. Schweber is not well represented in the Pacific and Mountain regions. Interestingly, the next two—Wyle and Pioneer—are strictly regional and do not attempt to cover the nation. Wyle, with only six locations, has larger sales than some distributors with as many as 20 locations.

Table 7.7-1 gives some pertinent statistical data on the same 14 industrial distributors. There are some 1,500 distributors in the United States that serve a $2.0 billion market. The 14 companies listed have an estimated 55 percent of this market when their sales are adjusted to consider the varying calendar dates of annual report data into account. Many of these distributors are subsidiaries of companies involved in other businesses, and this table gives the share of corporate sales that are in industrial electronic distribution, except for Arrow and Newark.

In the case of Arrow and Newark, the sales figures include the distribution of electrical parts to contractors; for this reason, they are listed below Pioneer, even though the sales figures are larger. Pioneer's sales have been adjusted to exclude their sales of consumer electronic parts and products, and to include the sales of an unconsolidated distribution subsidiary.

Table 7.7-1 also gives the average sales per location. With the exception of JACO, Hamilton and Wyle have the two highest averages on the list, and both companies tend to be dominant in the area in which they are located. JACO is unusual because it has three distribution businesses, each of which handles a different component, and only two locations. Each business is represented at both locations, and it might be accurate to state that JACO actually has six locations. In this case, average sales per location would be $5.2 million.

Table 7.7-1 also lists the number of manufacturers stocked by each distributor, as well as the number of customers served. In recent years many distributors have reduced the number of manufacturers whose parts they stock; in particular, both Hamilton-Avnet and Cramer emphasize the fact that the bulk of their sales come from a minority of the manufacturers. The number of accounts served by these distributors may vary from 6,900 to 49,000, as indicated. Please note that the total number of distributor purchasing sources in the United States is estimated at 60,000 accounts, which means that many of Hamilton's customers must also be Cramer's customers. It is not unusual for each purchasing source to work with six or seven distributors in a given year.

Table 7.7-2 gives the product mix and associated businesses of the 14 largest distributors. All of them except JACO handle broad lines that include semiconductors, capacitors, resistors, connectors, relays, and switches. The largest companies—such as Hamilton, Wyle, and Cramer—have over 50 percent of their sales in semiconductors; whereas, distribution as a whole has 41 percent of all sales in semi-

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Figure 7.7-1

THE MAJOR INDUSTRIAL ELECTRONIC DISTRIBUTORS STOCKING LOCATIONS

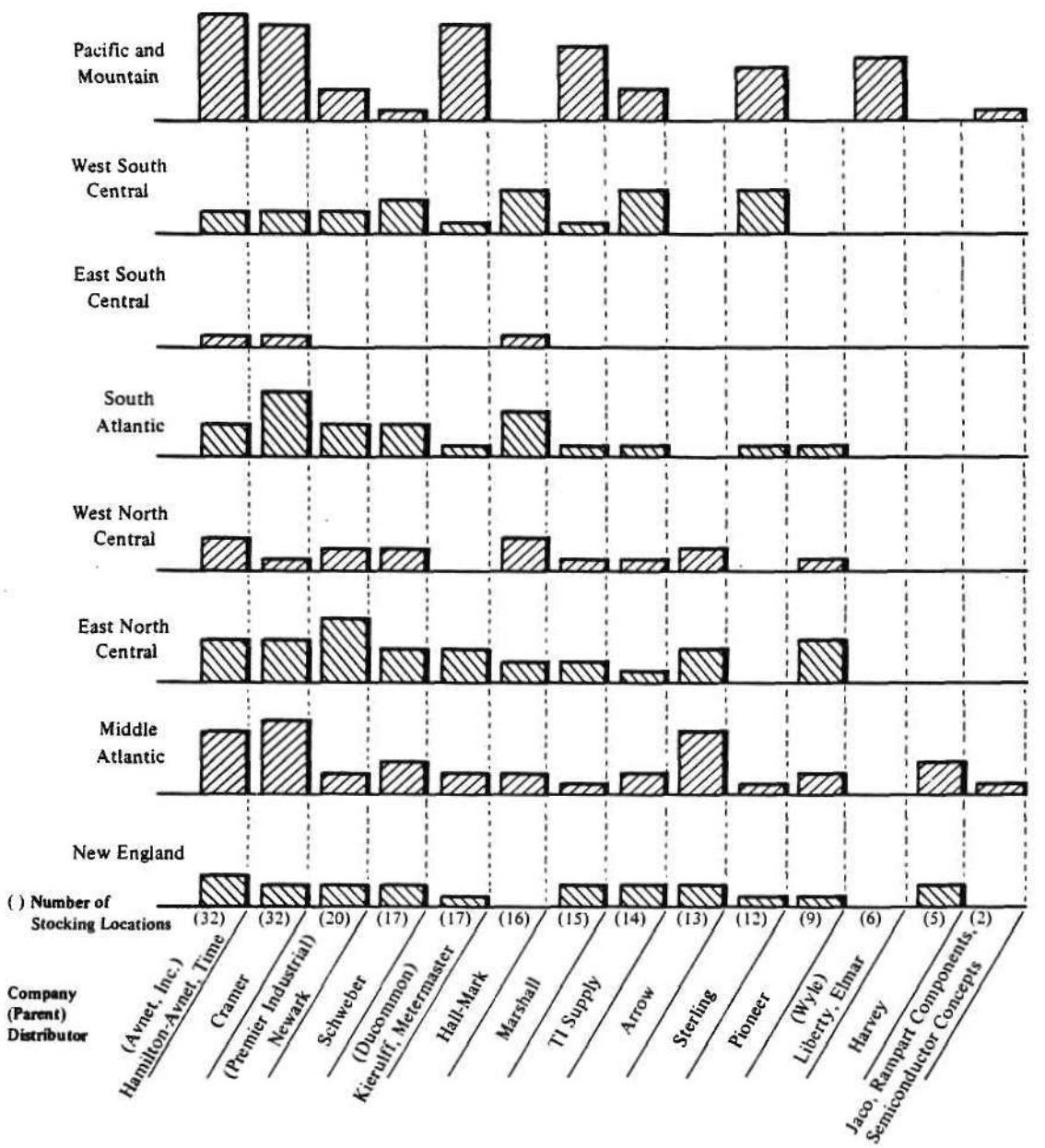

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Table 7.7-1

MAJOR INDUSTRIAL ELECTRONIC DISTRIBUTORS – STATISTICAL INFORMATION
(Dollars in Millions)

Company	Reported Sales Indust. Dist.	Annual Report Date	% Sales In Industrial Electronic Distribution	No. of U.S. Stocking Locations	Average Sales Per Location	No. of Mfgs. Stocked (% of Sales Represented)	Customers
Avnet	$230	Jun. 76	37%	32	$7.2	12 (80%) 55 (100%)	49,000
Cramer	122	Sept. 75	100%	32	3.8	20 (73%) 91 (100%)	45,000
Wyle	61	Jan. 76	46%	6	9.3	55 (100%)	–
Schweber	62	Dec. 75	100%	17	3.6	28 (100%)	–
Kierulff	51-44	Dec. 75	32-28%	17	3.2-2.6	55 (100%)	–
Pioneer	35.6-36.6[3]	Mar. 76	75-77%	9	3.9-4.1[1]	68 (100%)	–
Arrow	56.6[1]	Dec. 75	42-46%	13	2.8-3.1[1]	102 (100%)	Over 9,000
Newark	50.4[1]	Sept. 76	18-22%	20	1.4-1.7	88 (100%)	–
Hall-Mark	33	Dec. 75	–	16	2	54 (100%)	–
Jaco	31	Dec. 75	–	2	15.2[2]	20-25[2](100%)	–
Sterling	28	Mar. 76	53%	12	2.3	72 (100%)	–
TI Supply	25	Dec. 75	–	14	1.8	29 (100%)	–
Marshall	25	May 76	60%	15	1.67	19 (100%)	–
Harvey	19.8	Jan. 76	63%	5	3.96	68 (100%)	6,900

[1] These figures include sales of electrical parts through 11 branches for Arrow, 15 branches for Newark. Sales per location have been corrected.

[2] Jaco has three divisions: Jaco, Semiconductor Concepts, and Rampart. All three share the two locations, each stocks 20 to 25 manufacturers.

[3] Sales have been adjusted to include the non-consolidated Pioneer – Washington Electronics, and to exclude the Srepco Consumer Parts and Products Division.

Source: Annual Reports & 10 K's
DATAQUEST, Inc.

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Table 7.7-2

THE MAJOR INDUSTRIAL ELECTRONIC DISTRIBUTORS – PRODUCT MIX AND ASSOCIATED BUSINESS

Company	Types of Components Sold (Percent Sales by Type)	Other Businesses (Percent Contribution to Sales)
Wyle	Semiconductors (50%), Connectors (14%), Resistors (13%), Capacitors (11%), Relays and Switches (9%)	Machine tool and electronic manufacturing (27%), Trucking (16%), Aerospace Testing and Systems Engineering (11%)
Avnet	Semiconductors (62%), Connectors (24%)	Consumer products (26%), Wire and Cable (21%), Automotive Spare parts (13%), Electrical Spare parts, (11%)
Cramer	Semiconductors (43%), Connectors (13%), Capacitors, Resistors, Relays and Switches	None
Schweber	Semiconductors, Resistors, Capacitors	None
Kierulff	Semiconductors, Connectors, Capacitors	Metals Distribution (49-66%), Pyrolytic Graphite (1-4%), Automatic Reinforcing Bar Processing Equipment (1-9%)
Pioneer	Semiconductors (33%), Capacitors, Connectors, Resistors, Relays & Switches	Consumer Part and Product Distributors (25%), Instrument Distribution (10%)[1]
Arrow	Semiconductors (at least 20%), Capacitors Resistors, and Connectors	Smelting and Refining of Recycled Lead (auto batteries) (25%), Consumer Parts and Product Distribution (25%)
Newark	Semiconductors, Capacitors, Resistors, Connectors, Relays/Switches	Distribution of Maintenance Products (58%), Manufacture of Fire Fighting Products (11%)
Hall-Mark	Semiconductors, Capacitors, Resistors Connectors, Relay/Switches	—
Jaco	Jaco – Capacitors Semiconductors Concepts – Semiconductors Rampart – Relays/Switches, Connectors, Resistors	—
Sterling	Semiconductors, Connectors, Resistors, Capacitors, Relays/Switches	Consumer Product Distribution (24%), Component Manufacturing (19%), Computer Systems (4%)
TI Supply	TI Semiconductors, Connectors, Capacitors, Relays/Switches, Resistors	—
Marshall	Semiconductors, Connectors, Resistors, Relays/Switches	– Systems for component assembly operations, – Distribution of supplies for component assembly, – Distribution of wire termination products
Harvey	Semiconductors, Capacitors, Resistors, Connectors, Relays/Switches	Consumer Part and Product Distribution (15%), Food Brokerage (18%), Manufacture of Electronic Equipment (4%)

[1] These percentages apply when Pioneer – Washington sales are included.

Source: Industry Buyers Guides
Annual Reports & 10K's

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conductors.

It is interesting to note the other businesses in which companies that have industrial electronic distribution subsidiaries are involved. Consumer part and product distribution is a popular activity and is conducted by Hamilton, Pioneer, Arrow, Sterling, and Harvey. Usually this business includes sale of stereo components and CB radios as well as electronic parts for hobbyists. Hobbyist part distribution frequently preceded the industrial distribution business, and as the businesses grew, they were typically separated into different profit centers.

These companies are often involved in other kinds of distribution or wholesaling. Avnet distributes automotive and electrical spare parts; Kierulff (Ducommon) is a metals distributor; Pioneer distributes instruments; Newark distributes maintenance products; Marshall distributes wire termination products and supplies for component assembly; and Harvey is involved in frozen food brokerage.

Many of these companies have manufacturing operations, some of which have a nontechnological content. In some cases, such as Arrow's acquisition of a company that recycles old auto batteries, these operations were chosen because they were thought to be countercyclical to the distribution business. Other manufacturing operations include Avnet's consumer products and wire and cable; Kierulff's (Ducommon) Pyrolytic Graphite and Automatic reinforcing bar processing equipment; Wyle's machine tool and electronic manufacturing; Newark's fire-fighting products; Sterling's components manufacturing; Marshall's systems for component assembly; and Harvey's electronic equipment.

Finally, a few of these companies have service-oriented businesses. These include Wyle's trucking and testing businesses and Sterling's computer systems business.

SPECIFIC COMPANY ANALYSIS

Five publicly-traded distributors were selected for an analysis in greater depth. In this section, a short narrative discussion is presented on the history of each company and its current operations. The emphasis is on industrial distribution and the techniques and factors that each management has identified as being important to that business. However, a brief description is provided of the other business in which the companies with distribution subsidiaries are involved.

A computer analysis of each of the five companies' historical financial statements is also provided in Chapter 12 of this notebook. This analysis is of the entire company in each case, because this is the only financial information published, even though as little as 37 percent of its sales may be in industrial electronic distribution. This is reasonable on two grounds. First, the types of other businesses in which these companies are involved tend to be similar; the discussion of the previous section together with Table 7.7-2 covers this in some detail. Second, if one is interested in financial stability, he should be concerned about the entire corporation and not just the distribution segment. It is entirely possible that the distribution subsidiary could be strong, but handicapped because the parent company is weak.

The sales and earnings for the distribution subsidiaries are broken out in Table 7.7-3. These earnings are before interest and taxes and, depending on the debt burden, the net earnings could in some cases be small; for example, Cramer has a two to one liability to equity ratio and netted only 0.1 percent in 1975.

Some interesting correlations should be mentioned in connection with Table 7.7-3. Hamilton-Avnet, Pioneer Standard, and Wyle are among the most profitable distributors; they have average sales per location that are among the highest in the industry (see Table

7.7 Companies

Table 7.7-3

SALES AND OPERATING EARNINGS OF SELECTED INDUSTRIAL DISTRIBUTORS[1] (Dollars in Millions)

Company	Fiscal Year End	Distributors' Percent of Corporate Sales (1976)	1977 (est) Sales	1977 (est) Earnings ($)	1977 (est) Earnings (%)	1976 Sales	1976 Earnings ($)	1976 Earnings (%)	1975 Sales	1975 Earnings ($)	1975 Earnings (%)
Avnet[2]	June	37%	–	–	–	$231.0	24.6	10.6	$206.0	23.7	11.5
Cramer	September	100	–	–	–	–	–	–	122.0	3.9	3.1
Wyle	January	46	$80.0	5.6	7.0	55.7	2.6	4.5	63.1	3.1	4.9
Pioneer[3]	March	77	45.0	–	–	36.5	2.7	7.2	33.0	2.7	8.2
Sterling	March	53	–	–	–	27.1	1.3	4.6	28.7	1.5	5.2

Company	Fiscal Year End	1974 Sales	1974 Earnings ($)	1974 Earnings (%)	1973 Sales	1973 Earnings ($)	1973 Earnings (%)	1972 Sales	1972 Earnings ($)	1972 Earnings (%)
Avnet[2]	June	$224.0	28.0	12.5	$143.0	15.6	10.9	$88.3	8.2	9.3
Cramer	September	151.0	9.7	6.4	122.0	7.5	6.1	88.2	2.7	3.1
Wyle	January	60.5	5.7	9.3	42.1	3.7	8.8	31.1	2.2	7.0
Pioneer[3]	March	27.9	2.2	7.9	22.0	1.8	8.0	16.8	1.3	7.6
Sterling	March	29.2	1.2	4.0	25.1	0.5	2.1	–	–	–

Company	Fiscal Year End	1971 Sales	1971 Earnings ($)	1971 Earnings (%)
Avnet[2]	June	$64.4	5.0	7.7
Cramer	September	60.1	2.8	4.6
Wyle	January	28.6	–	–
Pioneer[3]	March	15.1	0.9	6.2
Sterling	March	–	–	–

[1] Earnings are before interest and taxes.

[2] Earnings before interest and taxes were obtained by allocation.

[3] Includes some retail distribution. This is offset by the (unconsolidated) sales of Pioneer-Washington.

Source: 10 K's and DATAQUEST, Inc.

7.7-1). They emphasize employee motivation and go to some length to structure incentive programs for their employees that are tailored to the distribution business. Hamilton has a liability to equity ratio of .67, and Pioneer's is .69; both companies' balance sheets are considered conservative.

Wyle has also had an effective record; it has the highest sales per outlet in the group. It has been a good performer most years, but is the subsidiary of a miniconglomerate that experienced profit problems with some of its acquisitions in the early 1970s. Consequently, Wyle corporate carries a high debt load and has a liability to equity ratio of 1.76 to 1.00.

Sterling is similar to Wyle in that it is also the subsidiary of a miniconglomerate. Sterling corporate was still divesting itself of subsidiaries in 1975-76; it now has a liability to equity ratio of 2.37 to 1.00. The company has the lowest sales per outlet in the group and does not seem to be geographically concentrated in one area.

Cramer is the only distributor besides Hamilton that has a truly national coverage. Unfortunately, it has a large debt burden and has pledged all its assets to a consortium of banks; its liability to equity ratio is 2.00 to 1.00.

A review of the history of these five distributors does not make a strong case either for or against the conglomerate approach. Hamilton-Avnet does well, even though it is involved in a number of businesses. Pioneer has done well regardless of the fact it is 100 percent in consumer and industrial distribution. Similarly, the other three distributors have representatives on both sides of the conglomerate fence, and it is not clear that this causes a significant difference in operating results.

Avnet, Inc.

The Hamilton-Time Electronic Marketing Group is the largest division of Avnet, Inc., which includes distributors under the name of Hamilton-Avnet and Time Electronics West. This division had 1976 sales (year ending August 30, 1976) of $230 million and accounted for 37 percent of Avnet's gross sales and 32 percent of earnings. The electronic marketing group is also the largest distributor in the United States and is one of the most profitable as well, with a margin of 4.8 percent after-tax. Hamilton-Time had a five-year compound annual growth rate of 20 percent in sales and is well-represented nationally with stocking outlets. Its outlets have one of the highest average sales rates at $7.2 million per location.

Hamilton-Time is highly regarded by others in electronic distribution and by components manufacturers who supply products to distributors. A large part of the credit for their success is given to Mr. Tony Hamilton, who is said to be an extremely dynamic leader. He was involved in the procurement of electronic parts prior to forming his distribution enterprise, and at that time, most equipment manufacturers purchased directly from component suppliers. Hamilton was one of the first companies to serve as a distributor in this marketplace.

Hamilton has done one of the better jobs of personnel development in the distribution industry. The company defines precisely what decisions the managers of local stocking branches are permitted to make. More key management decisions are made at the home office than is true of other distributors, which considerably reduces the dependence on the local manager and allows Hamilton's branches to act in concert on a national level.

The local managers are provided with procedures and methods for running their branches that are simple but effective. These procedures cover such areas as packing and shipping, inventory control, and sales planning.

Hamilton seems to be able to retain its best employees longer. Good distribution salesmen and branch managers have a strong entrepreneurical motive and it is common for them to switch jobs frequently in search of greater rewards. However, Hamilton has strived to satisfy these employee demands within the organization. They provide an incentive plan for nearly every employee, which amounts to 10 percent of base salary for clerical people and nearly two-thirds for those in management.

Hamilton, although it is the largest electronic distributor, handles fewer lines than many of its competitors; in fact, 80 percent of its sales are accounted for by just 12 lines, whereas many competitors maintain 75 to 100 lines. Hamilton believes that by limiting its lines, they can do a better job of controlling inventory and understanding, selling, and servicing the line. In many cases, they are the largest customer of their supplier.

Avnet's other divisions are the consumer products group, the wire and cable group, the automotive group, and the electrical engineering group. These other businesses fit well into a corporate framework that includes electronic distribution since some of them are involved in distribution of other products. Their manufacturing activities tend to be in areas that are either not so business cycle-sensitive as distribution, or are in fields such as auto replacement parts, which are countercyclical; therefore, they tend to smooth earnings.

The Consumer Products Group includes Channel Master, the nation's leading TV antenna producer, and one of the leaders in replacement color TV tubes. It also sells moderately-priced home entertainment products under the BIC brand. Interestingly, BIC formerly was a distributor of Garrad turntables, and in 1974 was forced to make its own turntables when its 37-year contract with Garrad was terminated.

The Wire and Cable Group manufacturers

Avnet, Inc.

and sells insulated electrical wire products for the electrical, automotive, electronic, and OEM markets. Products are sold through distributors, mass merchandisers, and directly to manufacturers.

The Automotive Group operates in the replacement parts sector of the automotive aftermarket. It supplies automotive rebuilders with components and machinery used in the remanufacture of items such as alternators and starters. Moreover, this group makes and sells electrical and electronic replacement ignition parts for service stations and supplies a broad line of parts and supplies to new car dealers, fleets, and industrial customers.

The Electrical and Engineering Group distributes electric motors and controls and supplies parts for the rebuilding, repair, and replacement of industrial, air conditioning, and refrigeration motors. The group also has units that operate in the lamp, lighting, and medical computer market.

Avnet, Inc.

Avnet, Inc.
767 Fifth Avenue
New York, NY 10022

Investment Data

Listed On	NYSE "AVT"
Fiscal Year Ends	June 30
Recent Price (January 31, 1977)	18 1/8
Current Yield	2.8%

Balance Sheet (June 30, 1976)

Working Capital	$176.0 million
Long Term Debt	$ 37.3 million
Shareholders' Equity	$200.4 million
Return on Average Equity	19.0%
Shares Outstanding	
Preferred	549,297
Common	12,393,392

Operating Performance (Fiscal Year Ending June 30)

	1972	1973	1974	1975	1976
Revenue ($ Millions)	$357.6	$440.7	$571.0	$541.5	$621.5
Pretax Income ($ Millions)	$ 31.9	$ 44.0	$ 57.8	$ 53.0	$ 72.5
Pretax Margin (%)	8.9%	10.0%	10.1%	9.8%	11.7%
Effective Tax Rate (%)	49.7%	50.7%	50.7%	50.4%	51.2%
Net Income ($ Millions)	$ 16.0	$ 21.7	$ 28.5	$ 26.3	$ 35.4
Average Number of Shares Outstanding (Millions)	15.2	15.2	15.3	15.3	15.4
Per Share					
Earnings ($)	$ 1.05	$ 1.43	$ 1.87	$ 1.72	$ 2.31
Dividends ($)	$ 0.30	$ 0.30	$ 0.30	$ 0.34	$ 0.50
Price Range ($)	10-16	6-13	6-12	4-10	6-21
P/E Range	10-15	4-9	3-6	2-6	3-9

Source: DATAQUEST, Inc.

Cramer

Cramer Electronics has been in distribution of industrial electronic parts for over 20 years. It is in no other business besides industrial distribution of electronic parts, having divested itself of four retail stores in 1973. Cramer had 1975 sales (year ending September 27) of $122 million, and was second to Hamilton-Avnet; it had a five-year compound annual growth in sales of 17 percent. The company is fairly highly leveraged with a liability to equity that has averaged 1.5 to 2.5 to 1.0 during the last five years. This, together with the fact that it has no other countercyclical business, has caused its growth to be somewhat spotty. Sales increased by 38 percent between 1972 and 1973, but *decreased* by 19 percent between 1974 and 1975; during this period, earnings averaged 0.1 percent to 2.2 percent of sales. In March 1976, the banks required that Cramer stockholders authorize a grant of a security interest in virtually all of Cramer's assets, including inventory.

Cramer, together with Hamilton-Avnet and perhaps Schweber, deserves to be called a national distributor and has 32 stocking outlets throughout the country. These outlets are well located geographically, but have average sales per location of only $3.8 million compared to Avnet's $7.2 million.

Cramer has traditionally been a broad line distributor and attempted to stock a large variety of components to simplify its customer's procurement problems by reducing the number of its distributors. In the last several years, the breadth of the line has proven to be a problem, and Cramer has reduced the number of the manufacturers they stock; in 1975, 20 manufacturers represented 73 percent of Cramer's sales. In the last five years, there was an increasing concentration on semiconductor sales and these devices increased from 31 to 43 percent of Cramer's business. During this period, Cramer introduced on-line terminals for inventory status, order entry, and inventory control. Management credits this computer system for helping them better control its inventory.

Cramer

Cramer Electronics, Inc.
85 Wells Avenue
Newton, MA 02159

Investment Data

Listed On	ASE "CRM"
Fiscal Year Ends	September 27-October 3
Recent Price (January 31, 1977)	4 1/4
Current Yield	0%

Balance Sheet (September 27, 1975)

Working Capital	$23.9 million
Long Term Debt	$ 8.6 million
Shareholders' Equity	$21.1 million
Return on Average Equity	0.6%
Shares Outstanding	2,131,700

Operating Performance (Fiscal Year Ending September 30)

	1972	1973	1974	1975
Revenue ($ Millions)	$88.2	$121.8	$151.0	$122.0
Pretax Income ($ Millions)	$ 1.2	$ 5.6	$ 6.4	$ 0.2
Pretax Margin (%)	1.3%	4.6%	4.2%	0.2%
Effective Tax Rate (%)	47.9%	52.0%	50.0%	50.0%
Net Income ($ Millions)	$ 0.6	$ 2.7	$ 3.2	$ 0.1
Average Number of Shares Outstanding (Millions)	2.2	2.2	2.2	2.1
Per Share				
Earnings ($)	$0.28	$ 1.23	$ 1.42	$ 0.06
Dividends ($)	$0.00	$ 0.00	$ 0.00	$ 0.00
Price Range ($)	5-14	4-9	3-8	2-6
P/E Range	18-50	3-7	2-6	33-100

Source: DATAQUEST, Inc.

Pioneer

Pioneer Standard was organized in 1963 through consolidation of two Ohio-based distributing companies. Pioneer is a regional distributor, and its sales are confined primarily to a 12-state area centering in Ohio and including Michigan, Pennsylvania, South Carolina, and Kentucky. The company grew through internal expansion and acquisition until in 1976, it operated in three areas: the consumer part and product business (Srepco); the instrumentation business; and the industrial distribution business. Pioneer Standard owns 50 percent of an affiliated company: Pioneer/Washington. The financial statements of Pioneer/Washington are not consolidated with those of Pioneer Standard. Pioneer-Washington's sales and earnings in the last three years were as shown in Table 7.7-6.

Table 7.7-6

Pioneer-Washington
SALES AND EARNINGS (1974-76)

Year	Sales	Earnings	
		Dollars	Percent
1974	$ 7,994,270	$357,830	4.4%
1975	9,214,205	223,480	2.4%
1976	11,043,758	256,773	2.3%

Source: Pioneer
DATAQUEST, Inc.

When Pioneer Standard and Pioneer/Washington's sales are combined, approximately 65 percent of the sales are in industrial distribution. Of the remaining sales, 10 percent are in instrumentation and 25 percent are in consumer part and product distribution. Essentially all of Pioneer's sales are in some type of distribution, although perhaps not industrial distribution. The company also manufactures a line of instruments and sensors in the instrument division; these devices are sold to the process control industry.

Pioneer has one of the higher profit margins in the industry and is a growth company that is conservatively financed. Net profit after interest and taxes has been between 3.8 and 4.1 percent for the last five years; growth in sales has been 18 percent a year compounded, with very little fluctuation in the growth rate from year to year. In 1976, the sales growth exceeded the earnings growth for the first time because management decided to keep people on in anticipation of an upturn in the economy. The liability to equity ratio has been between .69 and .75, which is a conservative number for the distribution business. Management believes that its market has a growth rate of 12 percent a year and strives to maintain a minimum growth rate of 15 percent a year, which has been well within the financial capability of the company. While additional debt has been required to finance growing inventories and receivables, this debt growth has been matched by a growth in stockholders' equity; thus, balance sheet ratios have been maintained.

Pioneer believes that the most profitable sales are those made closest to home. Accordingly, its expansions in the past have typically been in geographical regions contiguous to those in which it already operates. The company generally moves a salesman into a region when there are enough orders from that region to support him. As business develops, some lines are stocked, until eventually a new stocking branch is opened. Pioneer is divided into five divisions and decentralizes decision making where possible to the division level; for example, 92 percent of all purchasing is done by the division that sells the part.

Pioneer competes through better service rather than by price cutting. They emphasize service by providing technical information through seminars and literature, and service through on time deliveries, equipment calibration, and value-added services. Management has instituted profit sharing programs for all of its employees. Sales people are compensated through a program based on the gross margin

so that they will not engage in price cutting. Local managers are compensated by a program that emphasizes return on investment so that they will watch inventories as well as margins. Pioneer believes that it was this program that helped them avoid some of the recent crises in semiconductor inventories.

Pioneer's industrial component sales are only 33 percent semiconductor. This is a smaller share than the 50 to 60 percent semiconductor share of sales exhibited by the large national distributors. Like many other distributors, Pioneer has narrowed its product line during the last ten years; thus, it can offer better service to the manufacturers that the company represents. Only 68 lines are currently represented, which is down from an original total of 300; no further reduction in lines is anticipated.

Pioneer

Pioneer-Standard Electronics, Inc.
4800 East 131st Street
Cleveland, OH 44105

Investment Data

Listed On	OTC "PIOS"
Fiscal Year Ends	March 31
Recent Price (January 31, 1977)	11 3/4
Current Yield	1.7%

Balance Sheet (March 31, 1976)

Working Capital	$8.4 million
Long Term Debt	$1.3 million
Shareholders' Equity	$9.1 million
Return on Average Equity	16.3%
Shares Outstanding	768,081

Operating Performance (Fiscal Year Ending March 31)

	1972	1973	1974	1975	1976
Revenue ($ Millions)	$ 16.9	$ 22.0	$ 27.9	$ 33.0	$ 36.5
Pretax Income ($ Millions)	$ 1.3	$ 1.9	$ 2.3	$ 2.7	$ 2.7
Pretax Margin (%)	7.9%	8.4%	8.3%	8.1%	7.3%
Effective Tax Rate (%)	49.0%	48.7%	48.1%	48.9%	48.1%
Net Income ($ Millions)	$ 0.7	$ 1.0	$ 1.2	$ 1.4	$ 1.4
Average Number of Shares Outstanding (Millions)	0.8	0.8	0.8	0.8	0.8
Per Share					
Earnings ($)	$0.90	$ 1.24	$ 1.56	$ 1.77	$ 1.80
Dividends ($)	$0.11	$0.12	$0.16	$0.18	$0.20
Price Range ($)	7-17	6-17	7-15	4-10	5-12
P/E Range	8-19	5-14	4-10	2-6	3-7

Source: DATAQUEST, Inc.

Sterling

Sterling Electronics was incorporated under Nevada law in 1966, as a successor to an earlier Texas business. From the beginning, it has been engaged in various forms of electronic distribution including components, replacement parts, test equipment, and sound reproduction. The company entered other businesses through acquisition in the late 1960s including components manufacturing , seismic and marine services, and metals and machinery manufacturing and distribution.

Sterling's acquisition program gave unfavorable results. Between 1969 and 1972, the liability to equity ratio climbed from 1.00 to a maximum of 2.74 in 1972. Reported profits were negative in 1971 and 1972, and although positive in other years, they have been accompanied by extraordinary items that make interpretation difficult. The company's net worth has fallen continuously from $20 million in 1969 to $6.4 million in 1976; moreover, a divestment or cessation of some segment of the business has occurred almost every year since 1969. The most recent was the sale of West Chester Electrical Supply to its original owner for a total of $1.7 million ($1.2 million cash, and $0.5 million in Sterling stock). This division had 1974 sales of $8.1 million and an operating profit of 9 percent (before interest and tax). By 1976 Sterling had improved its liability to equity ratio to 2.37 and achieved a profit before extraordinary items of 1.6 percent.

Sterling now has four operating groups: the industrial marketing group (53 percent of sales and profits); the component manufacturing group (19 percent of sales, 25 percent of profits); the retail merchandising group (24 percent of sales, 8 percent of profits); and the computer systems group (4 percent of sales, 14 percent of profits). The industrial marketing group is one of Sterling's better performers and had sales of $27 million and a margin of 4.6 percent before interest and taxes. Its 12 locations are widely dispersed geographically, but do not cover the country well enough to consider Sterling a national distributor. It does not appear that the company is a dominant distributor in any location, and some of the geographical areas in which it has outlets, such as the West Coast, are highly competitive. Sterling's average sales per outlet are relatively low for the industry, at $2.3 million. It represents 72 manufacturers of semiconductors, connectors, resistors, relays, and switches.

The company began work on a computerized order entry and inventory management system for the industrial distribution group in 1975. The programming is being conducted by the computer systems group, and it was scheduled to be completed in the summer of 1975; however, it had only reached the test stage in Houston by March of 1976.

Sterling's components manufacturing group includes the manufacture of illuminated display panels for instruments and aircraft, television antennas, transformers, power supplies, and panel meters. The retail marketing group sells electronic components and products to consumers, including stereo and CB radio equipment; This group has 24 stores in Texas and Louisiana. The computer systems group sells software, programming, and data processing services, some to other divisions of Sterling.

Sterling

Sterling Electronics Corporation
4211 Southwest Freeway
Houston, TX 77027

Investment Data

Listed On	ASE "SEC"
Fiscal Year Ends	March 28-April 3
Recent Price (January 31, 1977)	1-5/8
Current Yield	0%

Balance Sheet (April 3, 1976)

Working Capital	$10.8 million
Long Term Debt	$ 6.5 million
Shareholders' Equity	$ 6.3 million
Return on Average Equity	9.6%
Shares Outstanding	3,630,861

Operating Performance (Fiscal Year Ending April 3)

	1972	1973	1974	1975	1976
Revenue ($ Millions)	$43.2	$49.9	$50.7	$51.6	$50.3
Pretax Income ($ Millions)	($ 0.6)	$ 1.3	$ 1.8	($ 3.7)	$ 1.0
Pretax Margin (%)	(1.3%)	2.5%	3.6%	(7.3%)	2.0%
Effective Tax Rate (%)	(13.9%)	59.0%	45.5%	(25.6%)	48.6%
Net Income ($ Millions)	($ 3.6)	$ 0.2	$ 1.9	($ 3.8)	$ 0.6
Average Number of Shares Outstanding (Millions)	3.8	4.0	4.0	4.0	3.9
Per Share					
Earnings ($)	($0.93)	$0.06	$0.48	($0.96)	$0.15
Dividends ($)	$ 0.0	$ 0.0	$ 0.0	$ 0.0	$ 0.0
Price Range ($)	1-5	1-3	1-2	1-2	1-3
P/E Range	d	17-50	2-4	d	7-20

d=deficit

Source: DATAQUEST, Inc.

Wyle

Wyle Laboratories was founded in 1949 as the first testing laboratory specializing in functional and environmental testing of aircraft components. The company grew through the acquisition process until it reached the point in 1976 where only 10 percent of gross sales were generated by the original testing business. The first acquisition in distribution was that of Elmar in 1967, which was followed by acquisition of Liberty Electronics and then Seattle, Phoenix, and San Diego distributorships in 1969. Wyle had these five locations until 1972, when a sixth location was opened in Denver.

Wyle's other acquisitions were in the industrial manufacturing and transportation areas. Industrial manufacturing includes electronic products such as equipment cabinets and terminals, and mechanical products like hydraulic lifts, machines for straightening and cutting coiled wire and bus stock, and pipe-threading machines; and transportation includes both normal and refrigerated trucking operations. Wyle experienced profit difficulties and experienced a net loss in 1971, 1972, and 1973, which was attributed to the trucking and industrial manufacturing groups. During this period, the distribution group performed admirably as it increased sales from $28 to $42 million, and earnings before interest and taxes from $1.6 to $3.7 million. Subsequently, the other divisions of Wyle returned to profitability and distribution's sales increased from $42 million in 1973 to $55.7 million in 1976. However, distribution's earnings before interest and taxes did not keep pace and were $2.6 million in 1976, which is down from $3.7 million in 1973.

Wyle Laboratories is a fairly highly leveraged corporation and has a liability to total equity ratio, which has been between 1.8 and 2.3 during the last five years. Net profit after interest and tax has been between 1.7 and 2.2 percent of sales during this same time and was a deficit before that.

Wyle is a large regional distributor with all its outlets located in the Pacific and Mountain region; they operate under either the Liberty or Elmar name. Wyle has the largest average sales per location of any distributor at $9.3 million annually, and the company has a reasonably broad line of components and stocks parts from 55 manufacturers. Top lines in the semiconductor industry are represented and this category now accounts for about 50 percent of Wyle's sales. The other half of the distribution business is represented by important manufacturers of connectors, resistors, capacitors, relays, and switches.

Wyle has recently emphasized the technical training of its salesmen and has opened technology centers at its El Segundo and Mountain View facilities. These centers stock microprocessor design aids such as kits and program development devices (which sell in the $10,000 range).

The company has worked to develop an on-line computer system for inventory status and order entry as well as inventory control; it was completed in 1975 and expanded in capacity in 1976. This system has virtually automated the processing of orders and allowed faster more precise customer service. Furthermore, it provides valuable management reports of marketing data and inventory status.

Wyle

Wyle Laboratories
128 Maryland Street
El Segundo, CA 90245

Investment Data

Listed On	ASE "WYL"
Fiscal Year Ends	January 31
Recent Price (January 31, 1977)	5 3/4
Current Yield	4.2%

Balance Sheet (January 31, 1976)

Working Capital	$26.2 million
Long Term Debt	$26.4 million
Shareholders' Equity	$24.5 million
Return on Average Equity	8.2%
Shares Outstanding	
Preferred	36,205
Common	2,887,902

Operating Performance (Fiscal Year Ending January 31)

	1972	1973	1974	1975	1976
Revenue ($ Millions)	$76.4	$92.6	$118.6	$131.1	$120.1
Pretax Income ($ Millions)	($ 1.8)	$ 2.5	$ 5.3	$ 5.6	$ 3.6
Pretax Margin (%)	(2.3%)	2.7%	4.4%	4.3%	3.0%
Effective Tax Rate (%)	0.0%	63.0%	50.0%	47.0%	43.9%
Net Income ($ Millions)	($ 1.9)	($ 1.5)	$ 4.7	$ 2.9	$ 2.0
Average Number of Shares Outstanding (Millions)	3.5	3.5	3.8	3.6	3.2
Per Share					
Earnings ($)	($0.56)	($0.44)	$ 1.25	$ 0.83	$ 0.62
Dividends ($)	$0.00	$0.00	$ 0.00	$ 0.20	$ 0.24
Price Range ($)	3-7	2-5	2-5	3-6	3-7
P/E Range	d	d	2-4	4-7	5-11

d=deficit

Source: DATAQUEST, Inc.

7.8 Glossary

Asset Turns—The ratio of sales to total assets.

Bill Back—A contract provision that provides for the purchaser to pay a price premium for the parts in the event he does not take the full dollar value committed.

Bill of Materials—An engineering drawing that lists all purchased components in a piece of electronic equipment.

Consignment—An agreement in which the distributor stock remains the property of the manufacturer.

Contingent Inventory—Stock items that are held against a possible future order.

Co-Op Advertising—Distributor advertising that is partially paid for by a credit from the manufacturer of the advertised product.

Drag Business—Component sales that are "dragged" into a distributor by sales of more popular items.

FAE—Field Applications Engineer.

Franchise Agreement—An agreement between a distributor and a manufacturer that sets the price at which he buys products and defines other terms and conditions, such as price protection and stock rotation. The Wright Patman Act gives the legal definition of a franchise.

Gray Market—A market for components other than the conventional one between manufacturer, distributor, and OEM.

Industrial Distributor—A distributor that buys from a components or parts manufacturer and sells to an equipment manufacturer.

Inventory Turns—The number of times inventory is turned over in a given year. Derived by dividing cost of sales by average inventory.

Inventory "Turns"—This quantity is derived by dividing sales by average inventory.

Jellybean—A commodity-type product.

Juice Sales—A selling technique which relies primarily on the salesman's rapport with the purchaser. This rapport may be enhanced by green stamps, football tickets, lunches, or other "juice."

Line Item—A component listing on a bill of materials.

Love em, Load em, and Leave em—A process whereby a component manufacturer induces a distributor to stock his product, but does not provide any follow-up support.

Mixing Privileges—A contract provision allowing a purchaser to vary the quantity of various part types without a cost penalty provided the total dollar volume of the order is maintained.

Muscle—A manufacturer of a component that sells well has the ability to command the distributor's attention. He is said to "muscle out" the other distributors.

MRO—Maintenance and Repair Order.

Narrow Line Distributor—A distributor with a limited number of lines.

OEM—Original Equipment Manufacturer.

Piggyback Orders—A distributor will agree to supply a portion (10 to 20 percent) of the material needed by a high-volume equipment manufacturer. The distributor provides a buffer stock to take up the month-to-month variation

7.8 Glossary

in the quantities needed and charges a slightly higher price than the component manufacturer (10 to 20 percent).

Presence—A component manufacturer who effectively communicates with his distributors and has an understanding of their problems is said to have presence.

Promo—A promotional activity.

Price List—Refers usually to the manufacturer's suggested price list that he provides to distributors. In practice, this sets the maximum prices at which distributors can sell.

Price Protection—A common clause in distributor agreements. This clause gives the distributor credit for his inventory when prices are lowered by the manufacturer and prevents him from losing money on his stock.

Pull Through—A manufacturer's promotional efforts are said to pull his product through the distribution channel.

Push Money—Incentive payments to distributor salesmen that cause them to favor a given manufacturer's product.

Rep—An abbreviation for manufacturer's representative.

Retail Distributor—A distributor that sells to consumers.

Restocking Charge—A charge to cover the cost of restocking returned merchandise.

Returns—Items returned to a manufacturer or distributor either because of faulty performance, misshipment, or they were no longer needed.

Sales Agency Agreement—An agreement between a representative and a manufacturer that defines his territory and establishes a commission structure.

SAM—Served Available Market.

Ship and Debit—Usually applies to orders above the quantities covered by published price lists. The distributor ships the parts and debits the component manufacturer for the difference between his distributor price and a pre-negotiated high-quantity price. Shipment is from distributor stock.

SPD—Supplementary Program for Distribution. Pioneered by Motorola in the early 1960s.

Specialist—A distributor that concentrates in one product category, e.g., capacitors.

Spif—A promotional prize awarded to distributor salesmen when they achieve a given quota of sales of a component manufacturer's product.

Stagnant Inventory—Stock items that do not sell.

Stock Rotation—A policy instituted by the components manufacturer that requires the distributor to return old parts periodically so they can be replaced with up-to-date ones.

TAM—Total Available Market.

VPA—Volume Purchase Agreement.

7.8 Distribution in the 1980s

Distribution should have increasing importance in the 1980s. The low cost of order processing distributors should keep the industry competitive for processing smaller accounts that tend to be neglected by most suppliers. The trend in the semiconductor industry toward larger-sized manufacturers should reinforce the need of the small component buyer for component distributors. Finally, burgeoning microprocessor and microcomputer sales should "drag" along sales of other components—including subsystem components like floppy discs and CRT terminals.

This chapter analyzes these trends and, in the last section, gives market data from 1974 to 1979, projected to 1984. An historic analysis of geographic market share is also given.

7.8.1 Forces at Work

As the 1980s dawn, a new era is opening for industrial electronic component distributors. A restructuring is taking place in the semiconductor industry; this restructuring is likely to force large semiconductor purchasers to make long-term commitments with their vendors. Smaller and more variable needs of both large and small companies will then have to be met through distribution.

Recently, a new category of devices has begun to pass through distribution: the subsystem component. These items, principally floppy discs, CRT terminals, printers, microprocessor boards, and development systems, are often purchased by the same customers who buy semiconductor components; as a result, distributors become natural selling channels. Currently, it appears that this emerging segment of the distribution business will be dominated by the largest distributors.

Other forces may favor larger distributors in addition to the one previously mentioned. Unfortunately, financial constraints make it difficult for a distributor to significantly increase market share through internal growth. Thus, the only alternative appears to be acquisitions and mergers. These forces may help to explain Arrow's recent acquisition of some of Cramer's branches and its current offer to purchase the rest of the company.

Distributors' share of the semiconductor business seems to vary with the business cycle. The final part of this section explains that variation and shows how semiconductors are becoming a more important segment of the electronic components distribution business.

Semiconductor Industry Restructuring

The 1980s should be the era of VLSI. During this period, we should see the introduction of 256K RAMs, 32-bit microprocessors, and multi-megabit bubble memories. These products will probably enjoy some of the best markets the industry has ever seen, but these seemingly technological miracles will be brought forth only at great cost to semiconductor manufacturers. Currently, almost one dollar of new assets (plant, equipment, and working capital) is required for a semiconductor company to add one dollar of VLSI sales revenue, and this ratio may increase throughout the 1980s. Formerly, an SSI or MSI factory could produce two dollars of sales for each dollar of assets.

VLSI factories, in addition to being expensive, take longer to build. Currently, it takes 2½ years from start to bring a factory on stream compared to as little as 1 to 1½ years in the early 1970s.

Product development is also becoming more expensive. Although the more complex VLSI devices may someday sell for as little as today's MSI and LSI devices, they are becoming much more expensive to design. It is conceivable that the metal interconnection path on a VLSI circuit will someday be as complex as the entire road

system of the United States. The engineering effort required to develop this pattern is immense: one major manufacturer is said to have spent $20 million to develop the components, software, and board products for a new microprocessor family.

While VLSI technology becomes more complex, challenging, and difficult, its use in electronic equipment can significantly reduce manufacturing costs. We estimate that a system manufactured with VLSI components rather than with SSI and MSI components can be produced for as little as one-third to one-fifth the cost. Naturally, this factor leads to great demand for VLSI components. We believe that this demand, together with the previously cited difficulties of design and manufacture, will cause the 1980s to be an era of relative scarcity.

The increasing importance of VLSI in electronic equipment from both a cost and performance point of view has made it possible for semiconductor firms to integrate vertically and offer board and system products. For some firms, the revenue from these products is as high as one-third to one-half of sales. Most of these board products offered by the semiconductor industry move through distribution.

The availability of VLSI components has opened start-up opportunities in electronic equipment manufacturing. For example, Apple Computer may be one of the growth successes of the 1980s. Currently, the firm approaches $70 million in sales and in 1980 expects to buy more bits of memory than were produced in the world in 1975. The proliferation of VLSI-consuming firms like Apple has been partly responsible for the sharp increase in distributor accounts.

Some semiconductor companies have met their needs for capital by selling all, or a portion of, their stock to large corporate investors. Others are able to obtain capital from other lines of business or to fund growth through internally generated capital and increased debt. Even so, most firms find it necessary to focus their effort on only a segment of the semiconductor market. Mostek, for instance, has successfully focused on the memory business. We believe that this trend will continue until there are only three to five major competitors in the microprocessor, memory, and other major markets. Furthermore, it is likely that these vendors will choose their own second sources and exchange masks with them as a means of reducing product development expense.

The number of electronic manufacturers who buy more than $100 million of semiconductor parts should increase to an estimated 31 by 1985. These firms will probably manufacture some of their own components, but will remain dependent on the semiconductor industry for the highest technology VLSI parts. In the coming age of scarcity, these firms may be able to obtain the parts they need only by making long-term (three to five year) commitments to their semiconductor vendors.

Distributors' opportunity in the 1980s is to satisfy the unanticipated needs of these large buyers, and to satisfy the needs of firms too small to attract the attention of the semiconductor industry. The distributor will likely act as an inventory buffer and appear to the semiconductor company as a steady component consumer even

though the needs of his customers vary widely. (See discussion on "Inventory Sharing," page 7.3-5). Distribution's principle problem is likely to be that of gaining access to semiconductor components in a period of scarcity.

The successful distributors in the 1980s should be those who are able to develop meaningful long range market development plans. These plans should include a strategy for each market, selection of compatible product lines and vendors, and a selection of winning semiconductor companies. Semiconductor firms are likely to favor those distributors who seem to have the most rational market approach, just as they now favor those equipment manufacturers believed to be most successful in their own markets.

The New Subsystem Components

We define the subsystem components market to include only sales to firms that incorporate these products into hardware which they manufacture. These customers are also buyers of other components like resistors and capacitors and, obviously, are currently customers of industrial electronic component distributors. Moreover, some of these customers buy subsystem components from systems distributors as well. A system distributor sells systems and subsystems but does not sell components. Table 7.8-1 shows how this market is segmented and how it is projected to grow.

Table 7.8-1

ESTIMATED NORTH AMERICAN INDUSTRIAL AND SYSTEMS DISTRIBUTORS SUBSYSTEM COMPONENTS RESALES TO MANUFACTURERS

(Millions of Dollars)

	1978	1979	1984
Industrial Electronic Distributor Sales			
Semiconductor Company Products	$110	$150	$460
Non-Semiconductor Company Products	15	40	275
System Distributor Sales			
Non-Semiconductor Company Products	10	20	50
Total	$135	$210	$785

Source: DATAQUEST, Inc. November 1979

7.8.1 Forces at Work

The industrial subsystem components market has the advantage that the buyers of these units generally expect only a minimum of software and service support from their distributors. Since these units are incorporated into some larger piece of "hardware" and then resold, the equipment manufacturer, himself, generally develops the software and service capability needed to support his product. Distributor overhead is reduced because these customers do not demand extensive software and service support. One successful distributor made quite a point of his belief that profits in this business could be higher than in components distribution. This situation is possible because the cost to process a line item tends to be independent of the price of the line item. Since subsystem components have higher line item prices than components, profits improve.

The market definition presented here is subtle, and perhaps an example will clarify it. If a thermal printer were sold by a distributor to a home computer manufacturer and then incorporated into his product, that sale would be counted. If the same printer were sold to a doctor to help him expand the capability of his home computer, that sale would not be counted. The second sale is undesirable in that it is likely to lead to customer demands for expensive service and software support—support that cannot be provided within the current margin structure.

Industrial electronic distributors enjoy a great advantage in reaching this market because they are the "channel of choice" for the semiconductor industry. Virtually all of the development systems, microprocessors and microprocessor boards that are sold through distribution are sold through industrial distributors rather than system distributors. Thus, when the buyer of a microprocessor board wants a CRT terminal, a floppy disc, or a printer, his first stop is the same distributor. Table 7.8-2 lists some of the causes for a proliferation of microprocessor-using firms which parallel the causes for the explosion in distributor's component customer base during the last decade (from 6,000 to 60,000 accounts in the United States).

7.8.1 Forces at Work

Table 7.8-2

ACCOUNT PROLIFERATION
CAUSES FOR THE EXPLODING CUSTOMER BASE

In Semiconductor Components	In Subsystem Components
Rapidly Decreasing Costs	Rapidly Decreasing Costs
Increasing Functional Capability	Increasing Functional Capability
Semiconductors Substituting for Other Technologies	Microcomputers Replacing Human Decision Making
Growth of Small Electronic Manufacturers	Growth of Firms Using Microcomputers

Source: DATAQUEST, Inc.
November 1979

Manufacturers of subsystem components have begun to realize that industrial electronic distributors can represent a lucrative channel for them. Currently, industrial components distributors typically account for less than 5 percent of the subsystems manufacturer's product sales. As a result, they do not fear distributor domination of their sales and tend to favor distributors who can command a nationwide market. Some semiconductor firms, on the other hand, fear distributor dominance and try to develop policies which will keep any one distributor from accounting for too high a portion of sales. Currently, subsystem component manufacturers are evolving their distributor agreements. Many have agreed to price structures and return policies similar to those of the semiconductor industry. Subsystem components also tend to be proprietary to a single manufacturer—there is little demand for second sourcing and little competitive distribution; usually a manufacturer will franchise only a single distributor in a given area.

The sale of subsystem components requires a substantial commitment on the part of a distributor. Usually, floor space must be set aside for showroom and inventory purposes, a special staff must be hired to communicate with customers, and substantial funds must be committed to inventory. We estimate that the total asset investment in a successful, operating branch is approximately $860,000. If this investment is funded partly (60 percent) out of earnings and partly (40 percent)

through debt, the number of systems branches a distributor can open in a given year is limited by total profits. Table 7.8-3 shows how a distributor's capacity for system branch expansion depends on total sales. It assumes that profits before taxes are at the industry average of 7.5 percent and that half the after-tax profit is invested in system branch expansion.

Table 7.8-3

INDUSTRIAL ELECTRONIC DISTRIBUTOR'S
CAPACITY FOR ANNUAL SYSTEM BRANCH EXPANSION

NATIONWIDE DISTRIBUTION SALES	POTENTIAL NEW SYSTEM BRANCHES
$400 million	15
$300 million	11
$200 million	7
$100 million	4
$ 50 million	2

Source: DATAQUEST, Inc.
November 1979

Clearly, the largest distributors will probably be able to open systems branches and saturate most geographic areas before smaller firms have a chance to get started. This strategy would allow a large distributor to dominate the subsystem market in a manner not possible in components distribution. We believe that Hamilton-Avnet, with estimated 1979 distribution sales of over $400 million and a market share of about 15 percent, is pursuing this strategy. It is estimated that in 1979 Hamilton-Avnet accounted for over 70 percent of the subsystem component sales (from non-semiconductor manufacturers) of industrial electronic component distributors.

7.8.1 Forces at Work

Merger, Acquisition Forces

In most industries, there is a positive correlation between market share and profitability. For this reason, many firms try to increase market share. Currently, the distribution business is structured so that no firm has more than 15 percent of the total market. Furthermore, financial constraints make it difficult for any one firm to increase share of market.

Table 7.8-4 gives maximum internally funded distributor growth rates for various combinations of interest rates and equity, and shows that 14 to 19 percent is the maximum growth rate. These figures assume a 7.5 percent pretax profit margin and a sales to assets ratio of 2.5 to 1. When the sales to assets ratio falls to 1.8 to 1, the maximum growth rate at 15 percent interest falls to 14.7 percent. This shows the importance of asset management in a highly leveraged situation.

Table 7.8-4

FINANCIAL LIMITS TO INTERNALLY FUNDED DISTRIBUTOR GROWTH

	Percent of Balance Sheet in Equity	
	60%	30%
Maximum Internally Funded Growth Rate at:		
10% Interest Rate	13.9%	22.9%
15% Interest Rate	13.1%	18.8%

Source: DATAQUEST, Inc.
November 1979

The yearly average growth rate of the industrial distribution market has been approximately 12 percent. Since this market is about $2.8 billion in 1979, a company that desired to increase its market share 1 percent would have to add $28 million in sales in one year, in addition to the 12 percent growth. Table 7.8-5 shows the resultant growth rate required for various sized companies. This information viewed with Table 7.8-4 shows that, in a given year, even the largest distributor would have difficulty increasing market share by more than 1 percent through internally funded

growth. "Small" distributors with less than $200 million in sales are essentially unable to increase market share without some source of funds from a parent company or a non-distribution business.

Table 7.8-5

ANNUAL PERCENTAGE SALES GROWTH REQUIRED FOR 1 PERCENT INCREASE IN MARKET SHARE

Current Sales	1% of 1979 Distributor Market	Growth for 1% Increase in Market Share	Market Growth	Total Growth Required
$400 million	$28 million	7.0%	12%	19.0%
$200 million	$28 million	14.0%	12%	26.0%
$100 million	$28 million	28.0%	12%	40.0%
$ 50 million	$28 million	56.0%	12%	68.0%

Source: DATAQUEST, Inc.
November 1979

The other obvious avenue to growth is through a process of merger or acquisition. This move can be especially attractive if two distributors do not compete in the same geographic regions and if they offer products that are reasonably compatible.

Distribution's Market Share

Distributors' share of semiconductor consumption has remained relatively constant over time, as shown in Table 7.8-6, except for the recession year of 1975. In this year, many electronic equipment manufacturers cut back their commitments with their semiconductor vendors, and were later forced to make up these deficiencies with purchases through distributors. Once distributors gained this portion of the semiconductor market, the gain was permanent.

7.8.1 Forces at Work

Table 7.8-6

ESTIMATED DISTRIBUTOR SEMICONDUCTOR RESALES
AS A PERCENTAGE OF NORTH AMERICAN SEMICONDUCTOR CONSUMPTION

	1974	1975	1976	1977	1978	1979
Distributor Sales	22.6%	26.1%	25.0%	24.5%	26.8%	27.0%
Growth (shrinkage) in Total North American Semiconductor Consumption	15.6%	(20.1%)	30.0%	15.2%	22.6%	30.1%

Source: DATAQUEST, Inc.
November 1979

In spite of the data mentioned above, most distributors feel that distribution is increasing its share of market year-by-year. The explanation for this belief can be found in at least two facts:

- Semiconductors represent an increasing share of the total components consumption. We estimate this share will increase from 33 percent in 1974 to 41 percent in 1984.
- As a result, semiconductors will represent an increasing share of distributor sales, from an estimated 28 percent in 1974 to 31 percent in 1984.

In other words, semiconductors are becoming increasingly important to distributors, but distributors, since the recession of 1975, have not significantly increased their share of semiconductor sales.

Manufacturers of non-semiconductor components seem to be increasingly turning to distribution. We estimate that distributors' share of total components distribution will increase from 26 percent in 1974 to 30 percent in 1984. As in the case of subsystem components, it appears that distributors are able to find customers that are otherwise not available to components manufacturers.

7.8.2 Subsystem Distribution

Industrial electronic component distributors provide an important channel of distribution for subsystem components. Subsystem components include floppy discs, mini and microcomputers, printers, and CRT terminals. We call these devices "components" because many industrial customers purchase them to incorporate with another piece of hardware, in the same way they would buy a transistor, diode, or IC. This section provides a perspective, discusses market characteristics, provides a financial discussion of branch requirements, and gives some sales data.

Perspective

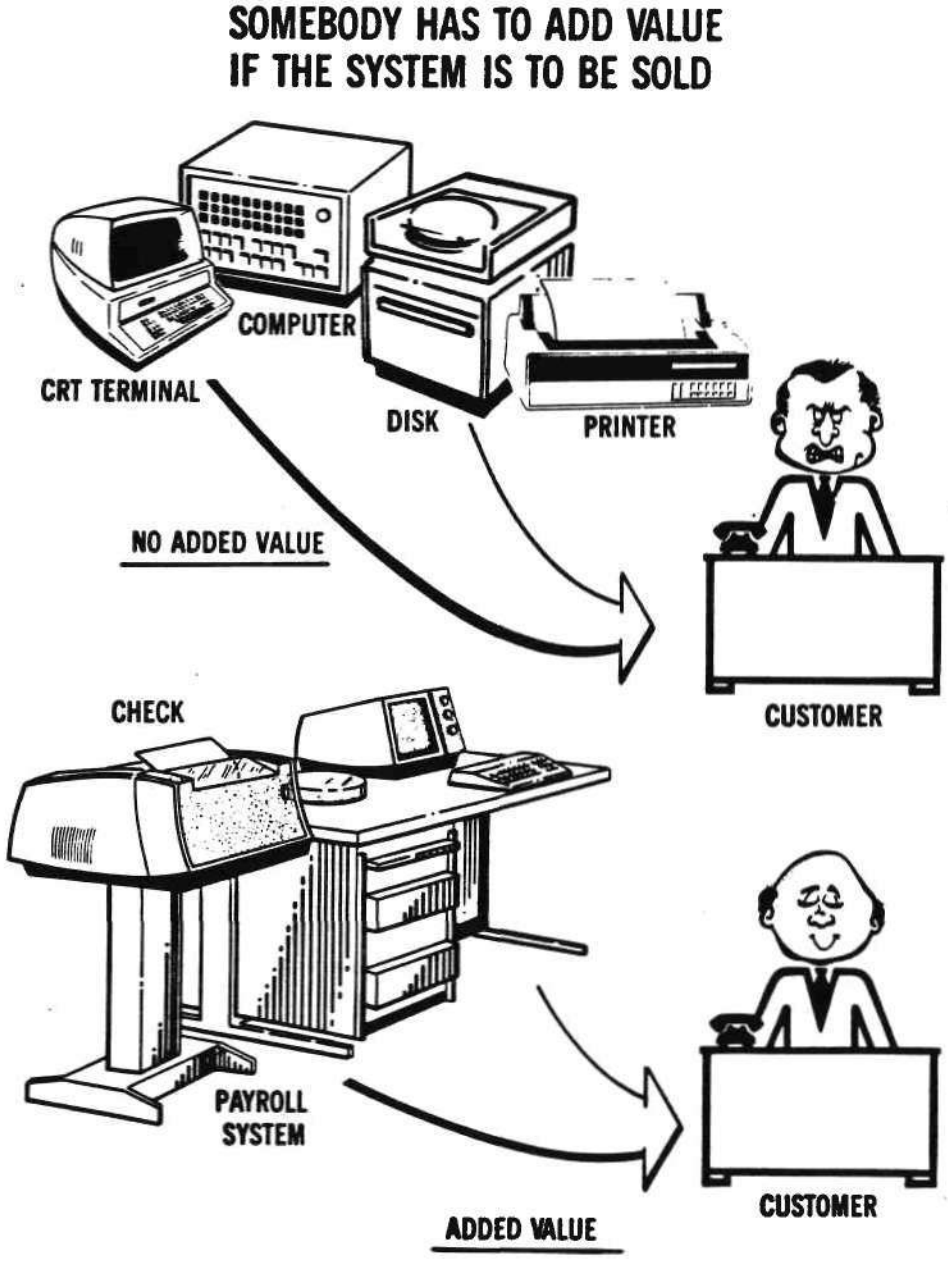
As Figure 7.8-1 suggests, the ultimate customer for a subsystem component is not really looking for a computer, disc, printer, or terminal. Instead, he wants a solution to his problem, whatever it may be. No subsystem component will solve his problem directly—something must be added to it so that, together with other subsystem components, it can solve his problem. This added value may be in the form of hardware, firmware, or software. Added value can be substantial; typically, the total value of all subsystem components is only one-half to one-third the final system price. Hardware is a general term that describes any physical device like a semiconductor part, resistor, or capacitor that might be used to make the equipment. Once the equipment is physically assembled, it generally must be programmed in some fashion before it is considered to be a system.

Most systems employ some sort of computing device: either a minicomputer or a microprocessor. These devices are general purpose; they perform a specific function only when they have been programmed. A program is simply a list of instructions that the computer can follow. A payroll program, for instance, might include instructions which cause the computer to compute benefits, make tax deductions, debit the firm's bank account, or print a check. The list of instructions which makes up a program could be stored as software or firmware. Software lists are stored in some sort of erasable computer memory like a semiconductor RAM or a floppy disc. Firmware lists are stored in read-only memories (ROMs) or programmable ROMs (PROMs). ROMs have their software lists permanently recorded at the factory. PROMs can be erased with ultra-violet light and reprogrammed in the field.

Microprocessor development systems are used to develop ROM or PROM programs. (Curiously enough, the development system is itself an assemblage of subsystem components. It has a special ROM program that allows it to perform its specialized function. Many subsystem components sold by distributors are used by customers to expand the capacity of their development systems.) Essentially, the development system merely provides a "soft" way of storing and editing a program that will later be incorporated in a ROM or PROM. This capability greatly speeds programming because mistakes can be corrected quickly when the program is stored in an electrically erasable media like RAM or floppy disc. Many development systems have added features (called editors, compilers, assemblers, etc.) to speed the programmer's task. Since these subsystem components are general purpose, they are useful to many kinds of end-users. Marketing, however, is different because each group of users is a different class of customer.

7.8.2 Subsystem Distribution

Figure 7.8-1



7.8.2 Subsystem Distribution

Figure 7.8-2 illustrates the difficulty: computers are so versatile that they can solve many different problems—but to solve these problems, one must have expertise in that problem area as well as programming skill. Companies, like IBM, that sell large expensive computers do not generally program for customer applications. Instead, the customers themselves generally hire their own programming staff.

In the minicomputer business, some 3,000 to 4,000 systems integrators have sprung up. Generally, these systems integrators choose an applications area, such as manufacturing control or accounting, and provide a system to solve related problems. The system is generally "hooked together" from components in much the same way one would assemble a hi-fi set from separate receiver, turntable, and speaker. The unique value of the system is provided by the software. The systems integrator is usually able to sell the same system to more than one customer.

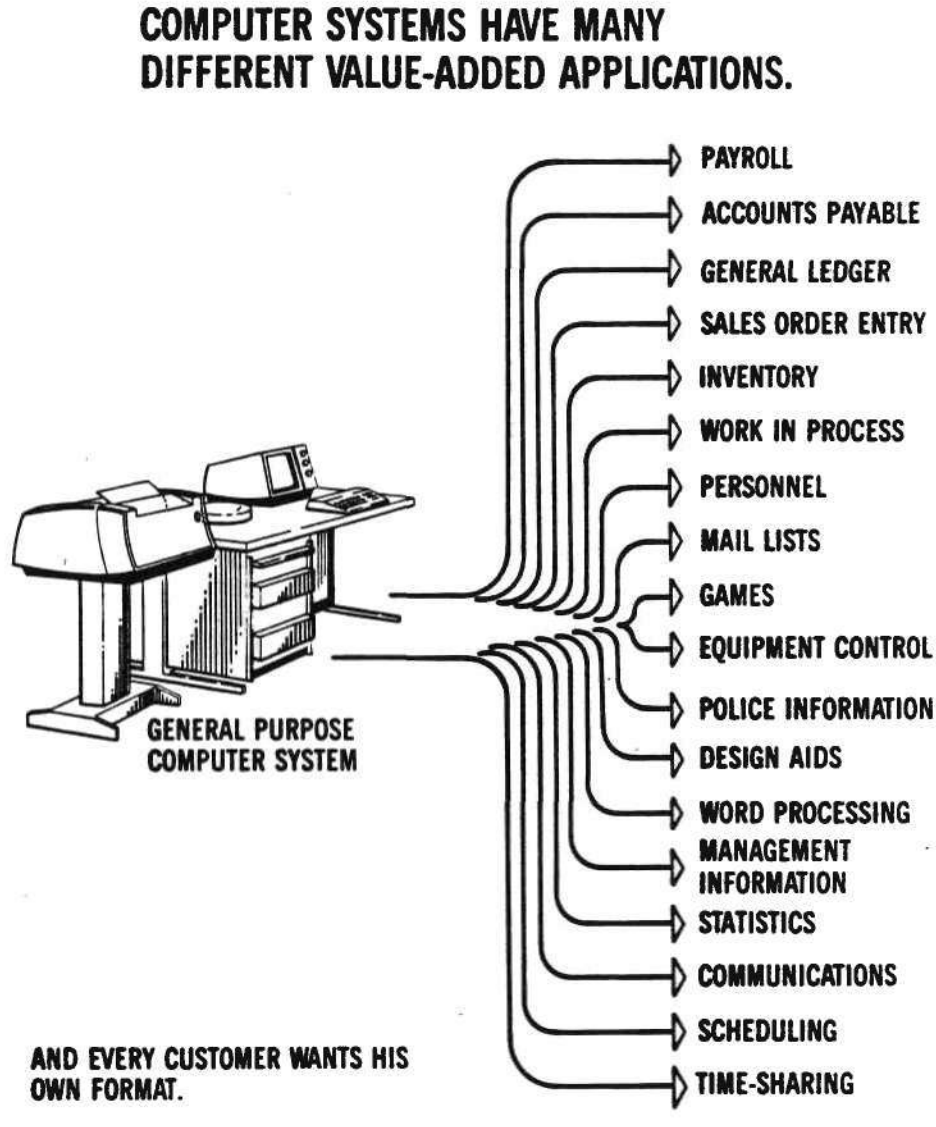
Microprocessor-based systems are even cheaper than minicomputer-based systems. Many microcomputers are used in "dedicated" applications that may be produced in quantities of 50 units or more to reduce the programming cost per system. A system for controlling the temperature of a supermarket is an example of a dedicated system. The manufacturer of such a system might buy either microcomputers on boards, or individual microprocessor components.

Microcomputer systems represent one large area of microprocessor applications. In a microcomputer, a microprocessor is programmed to provide some basic language like FORTRAN or COBOL to the user. It is packaged together with memory, input/output devices and some sort of control panel. Some distributors sell microcomputer systems in addition to other subsystem components but, generally, users are not in the industrial market. Most often, the microcomputer system is sold to an end user. This sort of sale requires much more software support than most distributors are equipped to give.

The application flexibility of computer-like devices leads to the complex distribution system shown in Figure 7.8-3. Definitions for the various functions are provided in Table 7.8-7. The key element in the definition of the (industrial) electronic distributor is the fact that his products are sold to manufacturers who also buy components.

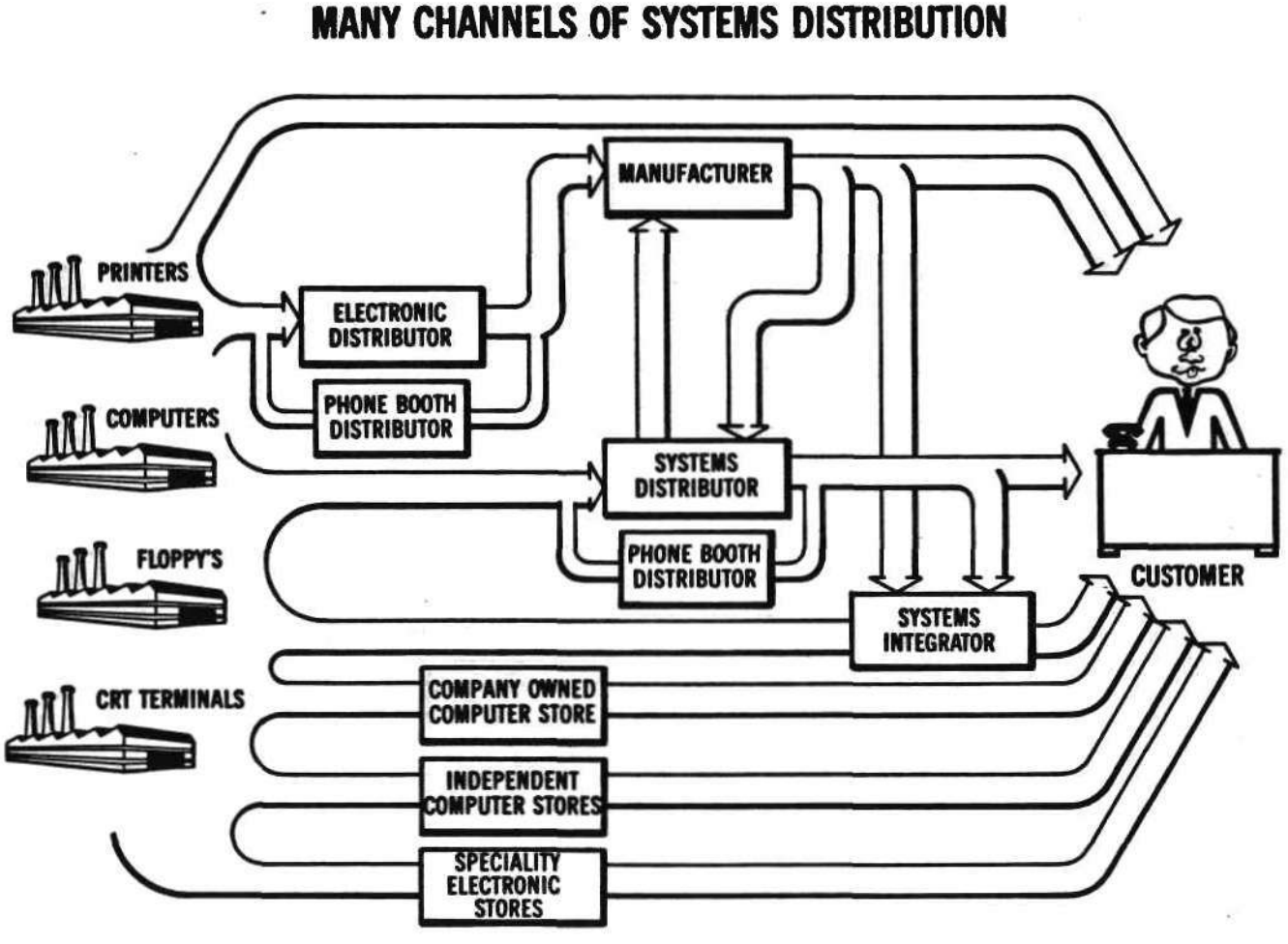
7.8.2 Subsystem Distribution

Figure 7.8-2



7.8.2 Subsystem Distribution

Figure 7.8-3



7.8.2 Subsystem Distribution

Table 7.8-7

DEFINITIONS

MANUFACTURER (Original Equipment Manufacturer)

Has a resale number
Also buys components

ELECTRONIC DISTRIBUTOR

Sells to manufacturers
Sells components
Sells subsystem components

SYSTEMS DISTRIBUTORS

Sells to system integrators
Sells turnkey systems to users
Sells to users who do their own integration
Does not add value
Does not sell components

SYSTEMS INTEGRATORS

Adds value through software
Adds value through systems integration
Adds value through maintenance
Sells high-priced systems to users

COMPUTER STORE

Sells medium priced turnkey systems to users
Sells software
Sells add-on peripherals

SPECIALTY ELECTRONIC STORE

Sells low-priced turnkey systems to users
Sells software
Sells add-on peripherals
Sells many other electronic items

PHONE BOOTH DISTRIBUTOR

Sells to manufacturers or users
Does not provide sales support
Has inadequate inventory
Discounts from list price

Source: DATAQUEST, Inc.
November 1979

7.8.2 Subsystem Distribution

"Phone booth" distributors are common in subsystems distribution. The distributor management and pricing policies of many non-semiconductor manufacturers of subsystem components have led to disorderly marketing characterized by the presence of "phone booth" distributors. These distributors take advantage of the manufacturers quantity discount, but do not provide the key functions of a true distributor: local inventory, sales support, and credit management. Their price cutting, however, makes it impossible for any other distributor to obtain adequate enough margins to provide these functions. Orderly marketing occurs only if the manufacturers of subsystem components take measures to discourage "phone booth" distributors. A discussion of appropriate policies is given in the next section.

Market Characteristics

Subsystem components manufacturers that are not semiconductor companies share a common characteristic; distribution sales represent a small portion of their sales and a small portion of the market. Figure 7.8-4 illustrates the situation in the printer market: IBM makes their own printers, accounting for over half the market. Of the remaining half, only low-cost printers are accessible to distribution; of this segment, distributors handle only one-seventh to one-fifth of the total. Though small now, the low-cost segment of these markets is growing rapidly. In effect, microprocessor sales "drag" along sales of these subsystem components. We estimate that the current growth rate of subsystem component dollar sales varies from a low of approximately 20 percent for low-cost printers to over 60 percent for 8-bit board level microcomputers.

Since most non-semiconductor manufacturers of subsystem components have a relatively small fraction of their sales through distribution, they do not have the same concern about distributor dominance as do semiconductor firms. Accordingly, they tend to favor the larger distributors who can offer nationwide coverage. Moreover, they are usually willing to grant exclusive rights to a distributor in a given geographic area. Since customers do not demand multi-sourcing, distributors need not carry competing lines and manufacturers can give non-competing franchises.

Most non-semiconductor manufacturers of subsystem components are accustomed to using step pricing rather than single column pricing. In addition, they provide the same prices to all buyers. These policies lead to disorderly distribution markets and make it impossible for distributors to maintain adequate margins. Step pricing provides discounts from single quantity list price for various quantity purchases; 10 to 24 units might be sold at a 25 percent discount; 100 or more units at a 30 percent discount. These prices are available to all buyers, whether or not they are franchised distributors. The result of this policy is that "phone booth" distributors enter the market. These distributors place an annual order for 50 or 100 units and take delivery of only a few items. They then place an advertisement in the newspaper offering these same units for sale at a discount from the manufacturers single quantity list price—the resulting spread between their sell and buy prices might be only 10 to 15 percent. In this way, the distributor hopes to obtain enough business so that all of the

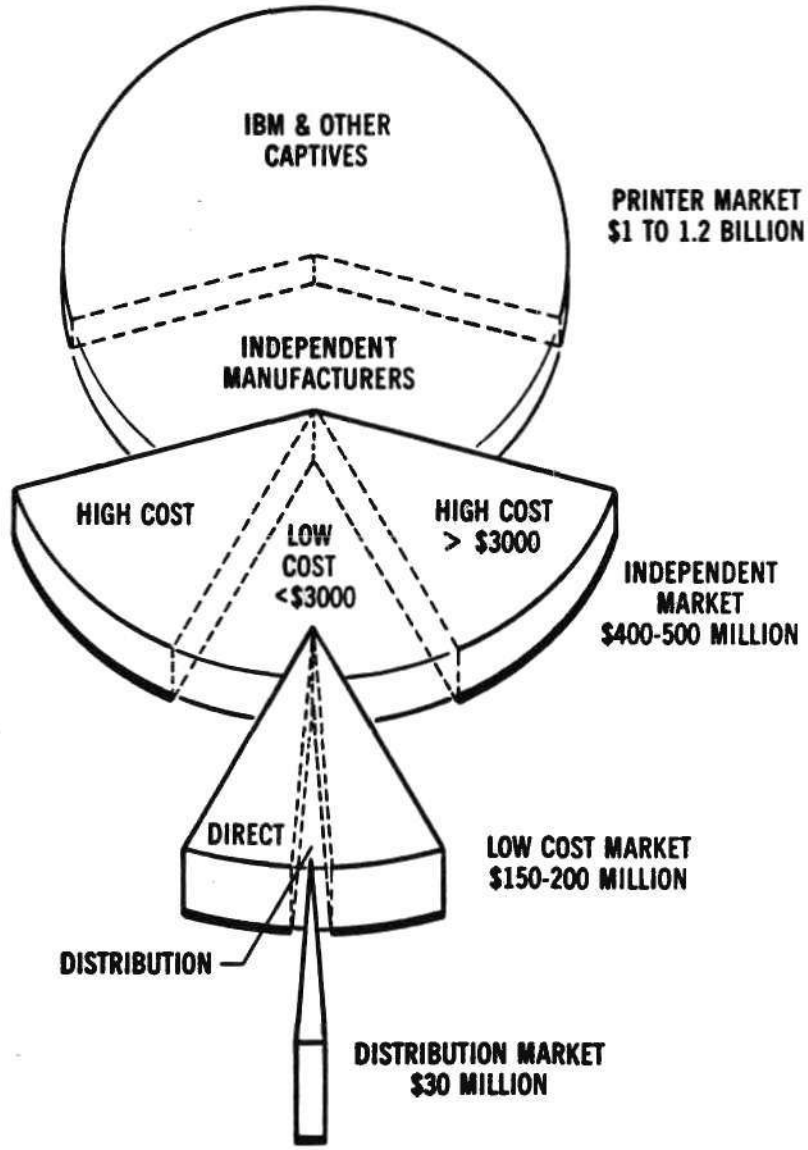
7.8.2 Subsystem Distribution

50 or 100 units originally committed are sold and that no added premium need be paid to the manufacturer. Often, products are sold only slightly above cost if the end of their annual commitment is nearing and the required quantity is not sold. Obviously, list prices are more or less meaningless in this situation.

7.8.2 Subsystem Distribution

Figure 7.8-4

PRINTERS: A TYPICAL SYSTEMS COMPONENT MARKET



7.8.2 Subsystem Distribution

Industrial electronic component distributors have introduced the concept of single-column pricing to their non-semiconductor subsystem component suppliers. (Single-column pricing is used by most semiconductor firms.) This pricing technique leads to much more orderly markets. It establishes a distributor price which is set at perhaps a 25 to 35 percent discount from the unit quantity price. This price is available only to distributors who sign a franchise agreement. The distributor price is independent of the quantity purchased; thus, no distributor has a cost which would allow him to undercut another distributor. Though quantity is not explicit, most manufacturers do not franchise a distributor until he has made some investment in inventory and provided a sales forecast. Most cancellation clauses have a 30- to 90-day notice period, so it is possible for a manufacturer to replace a distributor that is not selling the planned volume of product. The manufacturer himself may discourage or refuse to accept direct factory orders in quantities that the distributor is supposed to handle. Thus, single-column pricing allows a manufacturer to select his channel of distribution and ensures that the distributor will have sufficient margin so that he can provide the service required to achieve complete market penetration. The "phone booth" distributors who skimp on service and neglect market development are eliminated.

Branch Requirements

Although the distribution of subsystem components is similar to that of components, it is generally necessary to set aside a separate showroom and inventory area for each branch. In addition, several specialists are employed who can explain the features of the subsystem components to customers. Usually, inside sales, credit and collections, database management, and administration are shared with the components distribution part of the business.

Table 7.8-8 indicates some of the specialized branch requirements for subsystem distribution. Starting inventory may be $250,000. This figure may represent 15 or more product lines with an inventory in each line of $10,000 to $20,000 or more. Floor space is 3,000 sq.ft. Typically, some of the inventory is in the showroom, but this does not eliminate warehouse space because the shipping cartons must be stored so that display items can be repackaged when sold. Inventory turns should be 6 to 8 per year. This number is much higher than the component average, but is achieved by leading distributors. (Turns are counted from the time of manufacturer's invoice to the time of distributor's invoice.) It is achievable because unit prices are higher than that of most components and fewer units are inventoried; the implication is that no product should be carried unless it is being sold at the approximate rate of one unit per month.

The estimated employed assets at breakeven are $860,000. This figure assumes a sales rate of $200,000 per month. If 60 percent of the assets are provided through retained earnings, equity investment is $516,000; the rest is provided by debt, either in the form of payables or notes. Inventory at the running rate of $200,000 per month is estimated to be $400,000. The remainder of the investment is in receivables, land, buildings, and equipment.

7.8.2 Subsystem Distribution

Table 7.8-8

BRANCH REQUIREMENTS FOR SUBSYSTEM DISTRIBUTION

Multi-product Starting Inventory	$250,000
Floor Space*	
Showroom 1,500 sq.ft. Warehouse 1,500 sq.ft.	3,000 sq.ft.
Specialized Staff	3.5 persons
Time to Break Even	6 months
Average Discount	15-30%
Inventory Turns	6-8 per year
Ultimate Sales Rate	$200,000/month
Payables	30 days
Receivables	50-60 days
Estimated Assets Employed at Break-even Point	$860,000

*Shipping cartons must be stored for re-use after sale.

Source: DATAQUEST, Inc.
November 1979

7.8.2 Subsystem Distribution

Sales

Current, non-semiconductor manufacturers of subsystem components sold through distributors are listed in Table 7.8-9. Texas Instruments is listed here because one of its equipment divisions supplies the silent terminal printer. Table 7.8-10 gives the estimated 1978 and 1979 sales in each of these product groups. The board level microcomputers are generally 12- and 16-bit devices. As noted earlier, these products sold through distributors are at the low-cost end of their respective markets. The distributor's estimated average selling prices in 1978 were $2,000 for printers, $600 for floppy discs, $2,000 for board level microcomputers and $900 for CRT terminals.

Table 7.8-9

SUBSYSTEM COMPONENTS SOLD
THROUGH ELECTRONIC DISTRIBUTORS

LOW COST PRINTERS	
Centronics	Hamilton-Avnet
Data Products	Wyle
Texas Instruments	Pioneer, Hallmark
Control Data	Kierulff
FLOPPY DISCS	
Shugart	Hamilton-Avnet
Memorex	Wyle
Control Data	Kierulff
12- AND 16-BIT BOARD LEVEL COMPUTERS	
DEC	Hamilton-Avnet
Data General	Schweber, Hallmark
LOW-COST CRT TERMINALS	
Hazeltine	Hamilton Avnet
Lear Siegler	Wyle, Cramer, Pioneer

Source: DATAQUEST, Inc.
November 1979

7.8.2 Subsystem Distribution

Table 7.8-10

ESTIMATED 1978 AND 1979 NON-SEMICONDUCTOR SUBSYSTEM COMPONENT RESALES THROUGH U.S. DISTRIBUTORS

(Millions of Dollars)

	1978 Value	1979 Value
Printers	$ 3.9	$10.6
Discs	3.5	10.0
Board Level Microcomputers	2.8	10.8
CRT Terminals	4.6	6.0
Total	$14.8	$37.4

Source: DATAQUEST, Inc.
November 1979

7.8.9 Glossary

Asset Turns—The ratio of sales to total assets.

Bill Back—A contract provision that provides for the purchaser to pay a price premium for the parts in the event he does not take the full dollar value committed.

Bill of Materials—An engineering drawing that lists all purchased components in a piece of electronic equipment.

Consignment—An agreement in which the distributor stock remains the property of the manufacturer.

Contingent Inventory—Stock items that are held against a possible future order.

Co-Op Advertising—Distributor advertising that is partially paid for by a credit from the manufacturer of the advertised product.

Drag Business—Component sales that are "dragged" into a distributor by sales of more popular items.

FAE—Field Applications Engineer.

Franchise Agreement—An agreement between a distributor and a manufacturer that sets the price at which he buys products and defines other terms and conditions, such as price protection and stock rotation. The Wright Patman Act gives the legal definition of a franchise.

Gray Market—A market for components other than the conventional one between manufacturer, distributor, and OEM.

Industrial Distributor—A distributor that buys from a components or parts manufacturer and sells to an equipment manufacturer.

Inventory Turns—The number of times inventory is turned over in a given year. Derived by dividing cost of sales by average inventory.

Inventory "Turns"—This quantity is erroneously called inventory turns and is derived by dividing total sales revenue by average inventory.

Jellybean—A commodity-type product.

Juice Sales—A selling technique which relies primarily on the salesman's rapport with the purchaser. This rapport may be enhanced by green stamps, football tickets, lunches, or other "juice."

7.8.9 Glossary

Line Item—A component listing on a bill of materials.

Love 'em, Load 'em, and Leave 'em—A process whereby a component manufacturer induces a distributor to stock his product, but does not provide any follow-up support.

Mixing Privileges—A contract provision allowing a purchaser to vary the quantity of various part types without a cost penalty provided the total dollar volume of the order is maintained.

Muscle—A manufacturer of a component that sells well has the ability to command the distributor's attention. He is said to "muscle out" the other distributors.

MRO—Maintenance and Repair Order.

Narrow Line Distributor—A distributor with a limited number of lines.

OEM—Original Equipment Manufacturer.

Piggyback Orders—A distributor will agree to supply a portion (10 to 20 percent) of the material needed by a high-volume equipment manufacturer. The distributor provides a buffer stock to take up the month-to-month variation in the quantities needed and charges a price slightly higher than the component manufacturer (10 to 20 percent).

Presence—A component manufacturer who effectively communicates with his distributors and has an understanding of their problems is said to have presence.

Promo—A promotional activity.

Price List—Refers usually to the manufacturer's suggested price list that he provides to distributors. In practice, this sets the maximum prices at which distributors can sell.

Price Protection—A common clause in distributor agreements. This clause gives the distributor credit for his inventory when prices are lowered by the manufacturer and prevents him from losing money on his stock.

Pull Through—A manufacturer's promotional efforts are said to pull his product through the distribution channel.

Push Money—Incentive payments to distributor salesmen that cause them to favor a given manufacturer's product.

7.8.9 Glossary

Rep—An abbreviation for manufacturer's representative.

Retail Distributor—A distributor that sells to consumers.

Restocking Charge—A charge to cover the cost of restocking returned merchandise.

Returns—Items returned to a manufacturer or distributor either because of faulty performance, misshipment, or lack of need.

Sales Agency Agreement—An agreement between a representative and a manufacturer that defines his territory and establishes a commission structure.

SAM—Served Available Market.

Ship and Debit—Usually applies to orders above the quantities covered by published price lists. The distributor ships the parts and debits the component manufacturer for the difference between his distributor price and a pre-negotiated high-quantity price. Shipment is from distributor stock.

SPD—Supplementary Program for Distribution. Pioneered by Motorola in the early 1960s.

Specialist—A distributor that concentrates on one product category, e.g., capacitors.

Spif—A promotional prize awarded to distributor salesmen when they achieve a given quota of sales of a component manufacturer's product.

Stagnant Inventory—Stock items that do not sell.

Stock Rotation—A policy instituted by the components manufacturer that requires the distributor to return old parts periodically so they can be replaced with up-to-date ones.

TAM—Total Available Market.

VPA—Volume Purchase Agreement.

7.9 Market Statistics

Market statistics are presented in this section. Table 7.9-1 gives semiconductor resales by technology. Table 7.9-2 gives the ratio of these sales to the total North American market as given in Appendix A. These figures overstate the distributor share on a unit basis since resales are based on distributor selling prices. Table 7.9-3 presents subsystem component resales, Table 7.9-4 states territory definitions, and Table 7.9-5 gives sales by territory.

Table 7.9-1

ESTIMATED NORTH AMERICAN INDUSTRIAL ELECTRONIC DISTRIBUTOR SEMICONDUCTOR RESALES

(Millions of Dollars)

	1974	1975	1976	1977	1978	1979	1984
Total Semiconductor	$512.0	$472.0	$589.0	$664.0	$875.0	$1,120	$2,218
Integrated Circuits	$288.3	$255.7	$359.0	$417.0	$591.7	N/A[1]	N/A
Bipolar Digital	$139.6	$ 98.6	$133.2	$150.9	$223.7	N/A	N/A
MOS	$ 72.2	$ 80.7	$134.1	$152.3	$229.1	N/A	N/A
Linear	$ 76.5	$ 76.4	$ 91.7	$113.8	$138.9	N/A	N/A
Discrete	$206.7	$193.2	$202.7	$215.2	$244.2	N/A	N/A
Optoelectronic	$ 17.0	$ 23.1	$ 27.3	$ 31.8	$ 39.1	N/A	N/A

[1]Not Available

Source: DATAQUEST, Inc.
November 1979

7.9 Market Statistics

Table 7.9-2

ESTIMATED NORTH AMERICAN INDUSTRIAL ELECTRONIC
DISTRIBUTOR RESALES AS A PERCENTAGE OF NORTH AMERICAN CONSUMPTION

	1974	1975	1976	1977	1978	1979	1984
Total Semiconductor	22.6%	26.1%	25.0%	24.5%	26.3%	26.3%	27.0%
Integrated Circuits	22.9%	25.1%	25.3%	23.3%	25.7%	N/A[1]	N/A
Bipolar Digital	24.4%	27.2%	27.3%	25.8%	31.1%	N/A	N/A
MOS	16.3%	18.7%	20.3%	18.0%	19.9%	N/A	N/A
Linear	31.3%	34.1%	34.0%	32.1%	31.9%	N/A	N/A
Discrete	23.7%	29.1%	25.6%	26.2%	27.9%	N/A	N/A
Optoelectronic	13.9%	18.0%	19.0%	30.3%	26.8%	N/A	N/A

[1] Not Available

Source: DATAQUEST, Inc.
November 1979

7.9 Market Statistics

Table 7.9-3

ESTIMATED NORTH AMERICAN INDUSTRIAL ELECTRONIC SUSYSTEM COMPONENT RESALES

(Millions of Dollars)

	1978	1979	1984
Semiconductor Company Products			
Development Tools	$ 80.0	$102.0	N/A[1]
Board-level Microcomputers	42.4	53.5	N/A
Subtotal	$122.4	$155.5	$ 750.0
Non-Semiconductor Company Products			
Printers	$ 3.9	$ 10.6	N/A
Floppy Discs	3.5	10.0	N/A
Board-level Microcomputers	2.8	10.8	N/A
CRT Terminals	4.6	6.0	N/A
Total	$137.2	$192.9	$1,450.0

[1]Not Available

Source: DATAQUEST, Inc.
November 1979

7.9 Market Statistics

Table 7.9-4

TERRITORY DEFINITION

TERRITORY	AREA COVERED
Arizona	Arizona
Canada	Canada
Chicago	N. Illinois, NW Indiana, E. Iowa, Upper Michigan, SW corner Lower Michigan Wisconsin (minus NW corner)
Colorado	Colorado, W. Nebraska
Connecticut	Connecticut (minus SW corner)
Florida	Florida (minus Panhandle)
Indianapolis	Indiana (minus NW corner, SW corner)
Kansas City	Kansas, W. Missouri, E. Nebraska, W. Iowa
Los Angeles	S. California (minus San Diego), SW Nevada
Michigan	Lower Michigan (minus SW corner), Toledo, Ohio
Mineapolis	Minnesota, NW Wisconsin, North Dakota, South Dakota, N. Iowa
New England	Maine, New Hampshire, Vermont, Rhode Island, Massachusetts
New Mexico	New Mexico (plus El Paso, Texas)
New York City	N.Y.C., NE New Jersey, Long Island, SW Connecticut
Upstate New York	New York (minus Long Island), NW New Jersey
North Carolina	North Carolina, East Tennessee
Ohio	Ohio (minus Toledo)
Other Central	Kentucky, W. Tennessee, Mississippi
Other West	Idaho, Montana, Wyoming, Alaska, Hawaii
Philadelphia	E. Pennsylvania, S. New Jersey, Delaware
Pittsburgh	W. Pennsylvania, West Virginia

7.9 Market Statistics

Table 7.9-4

TERRITORY DEFINITION

TERRITORY	AREA COVERED
St. Louis	E. Missouri, S. Illinois, Kentucky
San Diego	San Diego County, Imperial County
San Francisco	N. California, NW Nevada
Seattle	Washington, Oregon
South East	Alabama, Georgia, South Carolina, Florida Panhandle
Texas	Texas (minus El Paso), Oklahoma, Arkansas, Louisiana
Utah	Utah, E. Nevada
Washington, D.C.	Washington, D.C., Maryland, N. Virginia

Source: DATAQUEST, Inc.
November 1979

7.9 Market Statistics

Table 7.9-5

SALES
NORTH AMERICAN GEOGRAPHIC SEMICONDUCTOR TAMS
NINE MAJOR SEGMENTS
(Percent of Total Market)

	1974	1975	1976	1977	1978
Los Angeles	14.0%	14.0%	15.0%	13.8%	13.8%
San Francisco	9.9	10.5	10.8	9.8	12.7
New York City	9.8	9.7	9.5	9.3	9.1
New England	7.6	7.5	8.6	8.1	8.1
Chicago	8.2	7.5	7.7	6.0	5.7
Texas	6.7	6.5	6.0	5.7	5.9
Ohio	4.4	4.8	4.3	4.6	5.1
Philadelphia	5.5	6.5	5.1	4.6	3.7
Washington, D.C.	4.6	3.2	3.4	3.5	3.4
Total Percentage 9 Major Segments	70.7%	69.7%	70.4%	65.4%	67.5%

Source: DATAQUEST, Inc.
November 1979

Table 7.9-5 (Continued)

SALES
NORTH AMERICAN GEOGRAPHIC SEMICONDUCTOR TAMS
TEN SECONDARY SEGMENTS
(Percent of Total Market)

	1974	1975	1976	1977	1978
Canada	2.3%	2.4%	2.3%	3.1%	3.6%
Florida	3.2	3.0	2.8	2.9	2.7
Minneapolis	2.8	2.2	2.4	2.3	2.7
Seattle	2.0	2.2	2.1	2.1	2.2
Connecticut	1.8	3.2	3.1	2.8	2.3
San Diego	1.4	1.5	1.7	1.8	2.1
Michigan	1.6	1.7	2.1	2.6	2.2
Arizona	1.3	1.3	1.2	2.1	1.7
Colorado	1.6	1.7	1.5	1.5	1.7
New Mexico	.5	.4	.6	1.3	.6
Total Percentage Secondary Segments	18.5%	19.6%	19.8%	22.5%	21.8%

Source: DATAQUEST, Inc.
November 1979

7.9 Market Statistics

Table 7.9-5 (Continued)

NORTH AMERICAN SEMICONDUCTOR TAMS NINE MINOR SEGMENTS

(Percent of Total)

	1974	1975	1976	1977	1978
Upstate New York	3.4%	3.3%	3.1%	2.9%	2.4%
Southeast	2.0	2.4	1.7	2.6	2.1
Kansas City	1.0	1.1	1.1	1.3	1.2
St. Louis	1.0	.9	.9	1.1	1.0
North Carolina	.9	.4	.5	1.5	1.2
Indianapolis	.9	.9	.9	.9	1.0
Utah	.7	.6	.5	.6	.8
Pittsburgh	.9	.9	.9	.9	.7
Other Central and Other West	___	.2	.2	.3	.3
Total Percentage 9 Minor Segments	10.8%	10.7%	9.8%	12.1%	10.7%

Source: DATAQUEST, Inc.
November 1979