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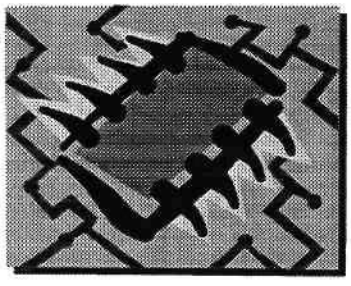
SEMICON/West 1998 Seminar



July 15, 1998
Sheraton Palace
2 Montgomery Street
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1998 SEMICON/West Seminar—July 15

Foundry Manufacturing: Does Technology Investment Deliver ROA?

James Hines

Principal Analyst
Semiconductor Contract Manufacturing

Overview

- Characteristics of the SCM (foundry) market
- Forecast
- Foundry capacity versus demand
- The SCM "technology glut"
- Conclusions

Semiconductor Contract Manufacturing

- Worldwide SCM market of $5.2 billion in 1997
- Dedicated foundry model established by TSMC in 1987
- Industry response to capital-intensive nature of semiconductor manufacturing
  - Economies of scale
  - Improved manufacturing efficiencies
  - Focus on process technology
- Fundamental structural change, here to stay

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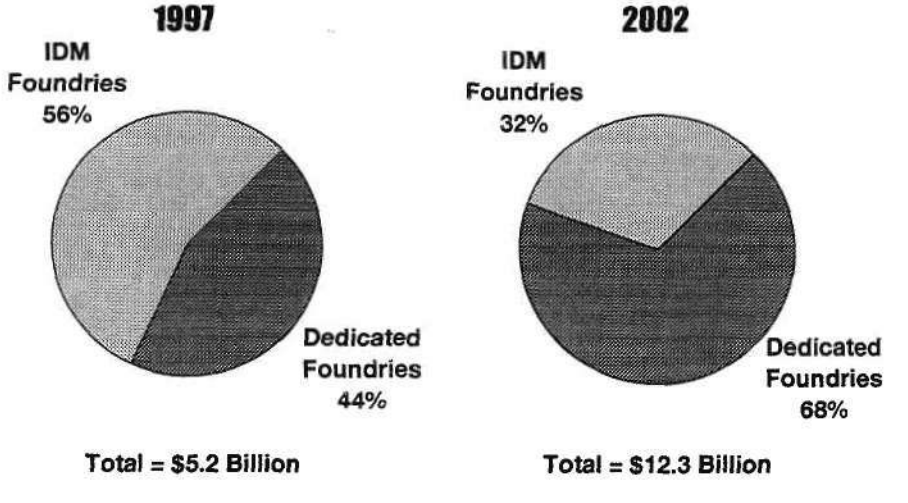
Dedicated Foundries Increasing Share of SCM Market



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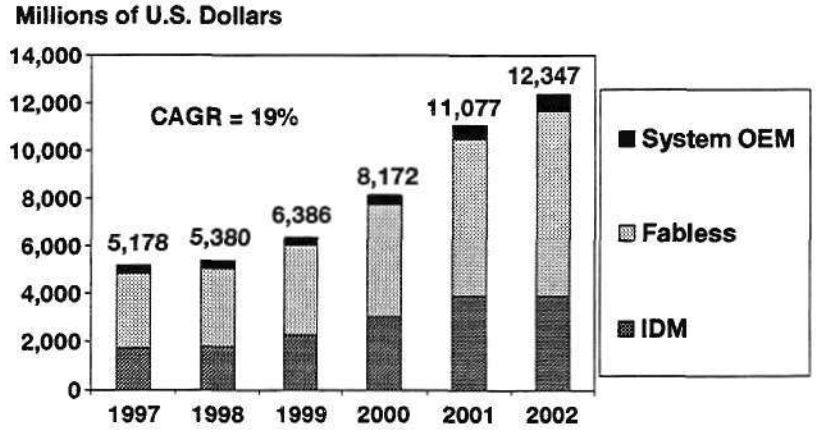
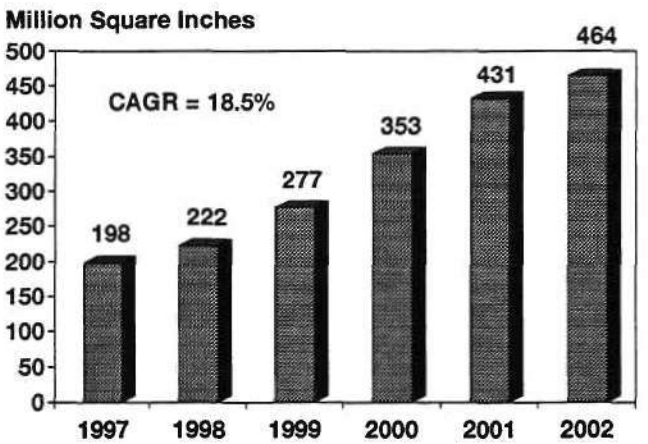
SCM Forecast Issues

- Asian economic slowdown affecting SCM demand
- Semiconductor market growth stalled
  - 1.4% growth in 1998
  - Lower demand from fabless and IDMs
- Oversupply keeping pressure on wafer prices
- 300mm transition increases IDM demand starting in 2001

Fabless Demand Driving SCM Market Growth



SCM Demand Forecast as Total Silicon Area



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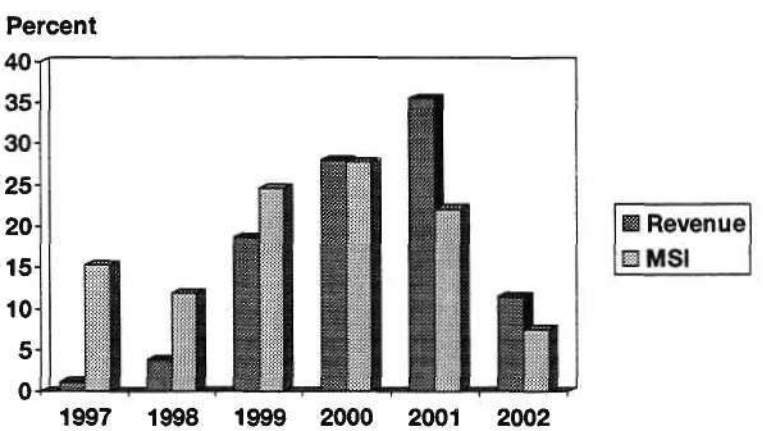
Comparison of SCM Annual Growth Rates



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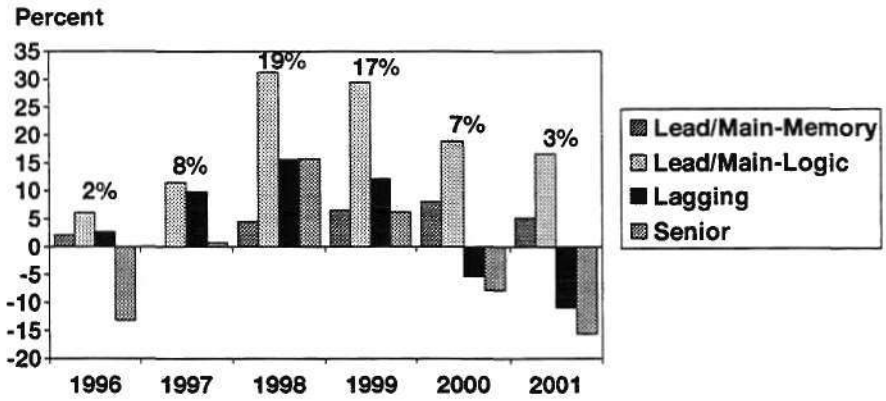
Excess Foundry Capacity

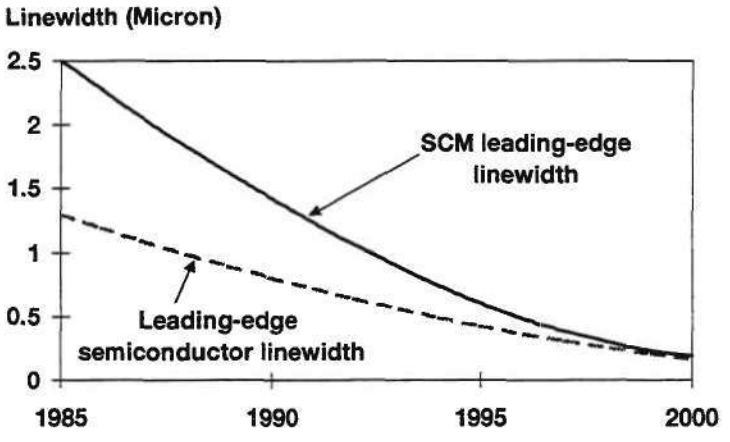


Source: Dataquest Year-End 1997 SCM Forecast

Foundry Capacity Correction Under Way

- Slowing demand growth
  - Asian economic slowdown
  - Semiconductor market stagnation
- Foundry overcapacity has become acute
  - Excess capacity of 30-40% in 1998
  - Likely in oversupply until 2000
- Foundries are responding quickly
  - Capacity expansion plans delayed
  - Reduced capital spending in H2/98 and 1999

Accelerated Technology Progression of Foundries



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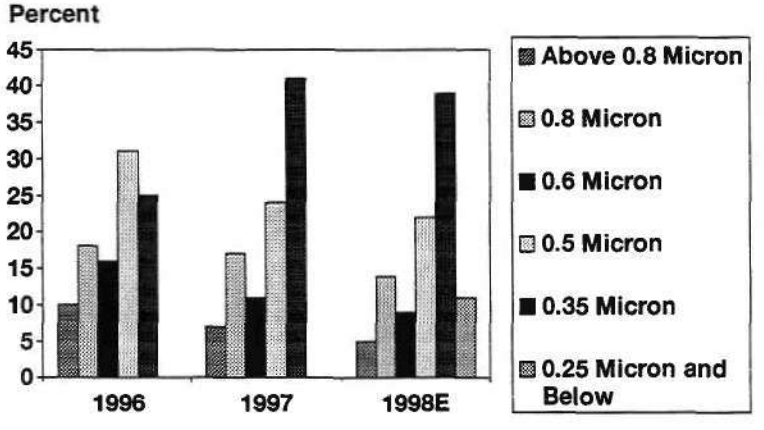
Foundry Capacity Is Shifting to Leading Edge Technologies ...



Source: Dataquest fab database

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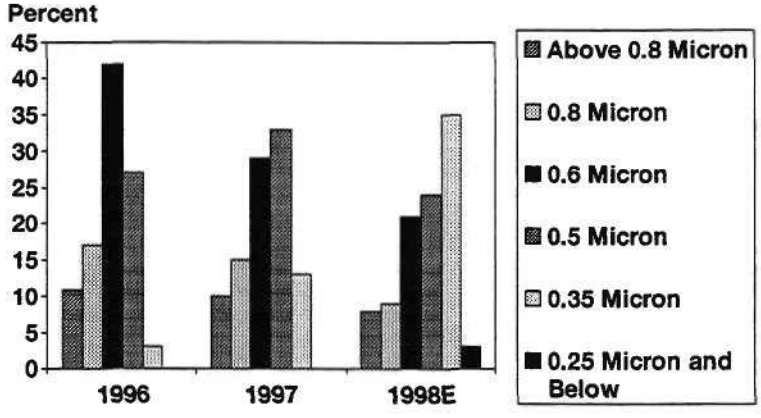
... But Fabless Demand Is Lagging

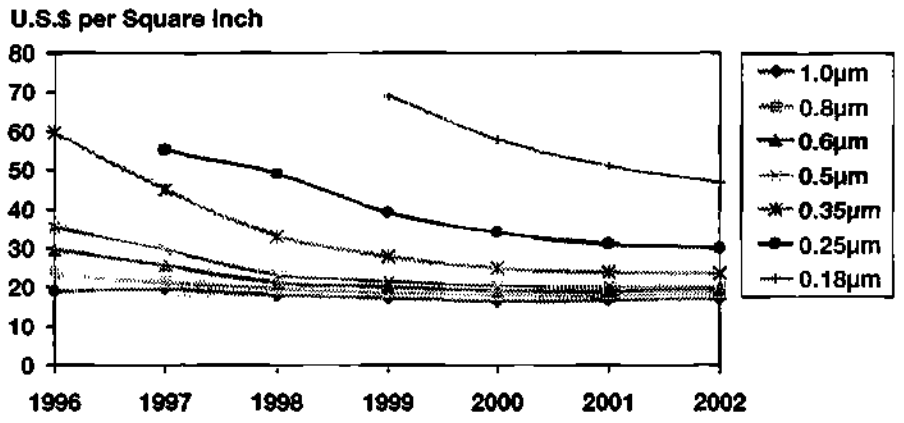


Source: Fabless Semiconductor Association Wafer Demand Surveys and Dataquest estimates

What Is Causing the Technology Glut in the Foundry Industry?

- Accelerated deployment of process technology by foundries
  - Aggressive investment in leading-edge technology
  - Movement of process development from fab to equipment supplier
- Sluggish migration of fabless IC designs to the leading-edge process technology
  - Lack of adequate EDA solutions: the "design gap"
  - "Pad-limited" designs: no economic incentive to move to smaller linewidth

SCM Wafer Pricing Trends



Source: Dataquest

Area of 8-inch wafer = 48.7 square inches

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Implications of a Foundry Technology Glut

- Foundries are forced to load leading-edge fabs with designs based on lagging technology
- Lower wafer prices drag down revenue per square inch of leading-edge fabs
- Foundries realize lower return on assets (ROA)
- Possible responses:
  - Stop investing in technology
  - Stimulate demand for leading-edge process technology

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Overcoming the Technology Glut

- Develop other sources of demand for leading-edge foundry services
  - IDMs
  - System OEMs
- Close the "design gap"
  - Integrated EDA and process technology development
  - Collaboration between EDA and equipment suppliers
- Interesting business combinations could arise

Is the Fabless Model Too Young to Have a Renaissance?

- Industry conditions similar to when the fabless model was born (1985)
  - Massive overcapacity
  - Corporate restructuring
- Elements in place for another fabless boom
  - Ample foundry capacity and technology
  - Low wafer prices
  - Available pool of IC design talent
- Present semiconductor downturn could hasten industry adoption of fabless/foundry model

Summary

- The foundry model represents a fundamental shift in the industry infrastructure
- Long-term outlook for SCM remains positive
- Foundry oversupply has become acute
- Foundries are responding by cutting capital spending in H2/98 and 1999
- Present technology glut could prompt new strategies and alliances
- Possible "Fabless Renaissance"

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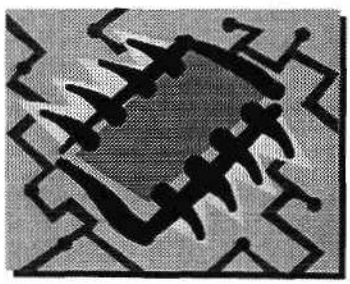

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SEMICON/West 1998 Seminar
July 15, 1998
Sheraton Palace, San Francisco

7:15 AM **Registration and Continental Breakfast**

8:00 AM **Welcome**
Clark J. Fuhs
Vice President and Director, Semiconductor Manufacturing Programs, Semiconductors Group
Dataquest

8:10 AM **Wafer Fab Equipment and Silicon Outlook: Searching for the "Up" Button**
Clark J. Fuhs
Vice President and Director, Semiconductor Manufacturing Programs, Semiconductors Group
Dataquest
Klaus-Dieter Rinnen Ph.D.
Principal Analyst, Semiconductor Equipment, Manufacturing, and Materials Worldwide, Semiconductors Group
Dataquest

8:50 AM **Seminar Theme Overview and Introduction**
Clark J. Fuhs
Vice President and Director, Semiconductor Manufacturing Programs, Semiconductors Group
Dataquest

9:00 AM **Keynote: The PC Market—The Need for Speed**
Randy Johnson
Director, Corporate Procurement, PCA Components
Compaq Computer Corporation

9:35 AM **Break**

10:00 AM **DRAM Market Driver: Manufacturing Economics or Technology Trends?**
Takashi Ogawa
Senior Industry Analyst, Semiconductor Equipment, Manufacturing, and Materials Worldwide
Semiconductors Group
Dataquest

10:30 AM **Foundry Manufacturing: Does Technology Investment Deliver ROA?**
James Hines
Principal Analyst and Program Manager, Semiconductor Contract Manufacturing Services Worldwide
Semiconductors Group
Dataquest

11:00 AM **Moore's Law: Economic Engine or Technology Road Map?**
Ron Dornseif
Principal Analyst, Semiconductor Equipment, Manufacturing, and Materials Worldwide, Semiconductors Group
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11: 30 AM **Seminar Concludes**

Wafer Fab Equipment and Silicon Outlook: Searching for the "Up" Button

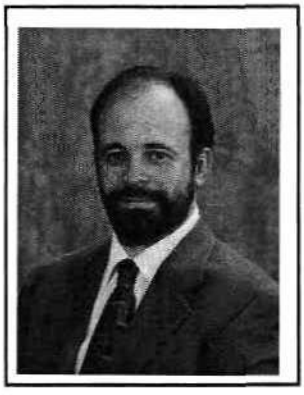
Clark J. Fuhs
Vice President and Director
Semiconductor Manufacturing Programs
Semiconductors Group
Dataquest

Mr. Fuhs is vice president and director of Dataquest's Semiconductor Manufacturing programs, which include the Semiconductor Equipment, Manufacturing, and Materials (SEMM) program and the Semiconductor Contract Manufacturing (SCMS) program. He is responsible for research and analysis of semiconductor materials and trends in IC manufacturing techniques along with forecasting capital spending and the wafer fab equipment market. He is also responsible for directing analysts and worldwide research activities in semiconductor manufacturing including foundry, fab capacity, silicon supply and demand, and trends in the manufacturing infrastructure for the industry.

Before joining Dataquest in 1993, Mr. Fuhs was strategic marketing manager for Genus Inc., a manufacturer of advanced chemical vapor deposition (CVD) and high-energy ion implantation equipment. During his 10 years at Genus, he held positions of product manager, several responsibilities in product marketing, and process engineer in the metal CVD group. Mr. Fuhs was responsible for correlating process techniques with demand for equipment and materials. He has been involved with the Modular Equipment Standards Committee of SEMI, a trade organization, as chairman of a task force, authoring a standard. His experience also includes Chevron Oil, where he was a process engineer in the Richmond, California, refinery responsible for the hydrogen manufacturing plant.

Mr. Fuhs earned a bachelor of science degree in chemical engineering from Purdue University in West Lafayette, Indiana, and received an M.B.A. from the University of California at Berkeley.

Wafer Fab Equipment and Silicon Outlook: Searching for the "Up" Button



Klaus-Dieter Rinnen, Ph.D.
Principal Analyst
Semiconductor Equipment, Manufacturing, and Materials Worldwide
Semiconductors Group
Dataquest

Dr. Rinnen is a principal analyst for Dataquest's Semiconductor Equipment, Manufacturing, and Materials Worldwide program in the Semiconductors group. He is responsible for research and analysis of semiconductor equipment and trends in IC manufacturing technology and capacity with a specific focus on the lithography, process control, RTP, and diffusion and implant segments.

Before joining Dataquest, Dr. Rinnen was at Applied Materials, Santa Clara, and AT&T Bell Laboratories, Murray Hill. His responsibilities at Applied Materials were in CVD process development, which included a role in customer service. His position at AT&T Bell Labs and education provided him with a 10-year background in optics and laser applications.

Dr. Rinnen earned a diploma degree in physics with minors in physical chemistry and mechanical engineering in Germany and a Ph.D. in applied physics from Stanford University.

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1998 SEMICON/West Forum—July 15

Wafer Fab Equipment and Silicon Outlook: Searching for the "Up" Button

Clark I. Fuhs — VP/Director
Klaus Rinnen — Principal Analyst
Semiconductor Equipment, Manufacturing, and Materials Program

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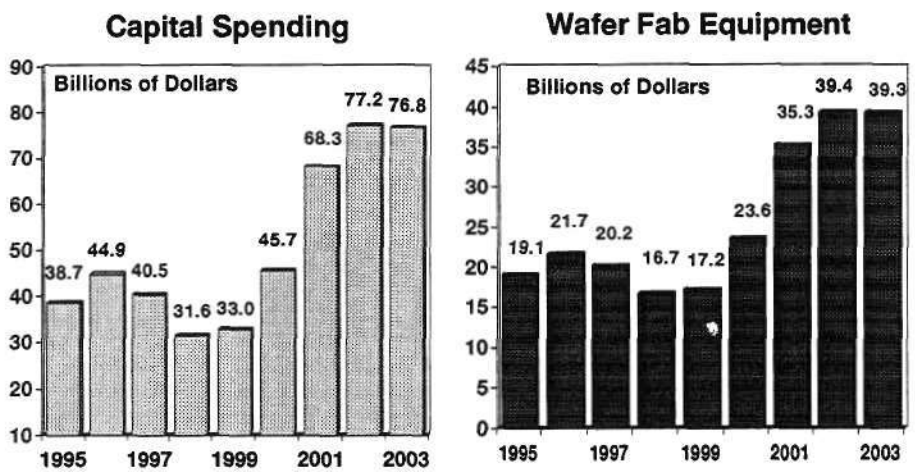
Overview

- Forecast: Overview and report card
- Semiconductor market issues
  - Impacts on 1998 and 1999 capital spending
- Capacity status
- Silicon wafer demand outlook
- Regional forecast assumptions
- High visibility equipment segments
- 300mm
- Conclusions and implications

Capital Spending Forecast



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Wafer Fab Equipment Forecast Review

- 1996: Transition year after peak growth in 1995
  - Second half held a major downturn
- 1997-1999: Three "pause" years
  - Extended by weak economic conditions
- 1997: A year of technology investment
  - Stronger than expected—more players
  - Quarterly run rates approached Q2/96 peak
- 1998: Year of economic correction
- Accelerated growth resumes late Q4/99 soonest
  - Basically in a "sit and wait for demand" mode

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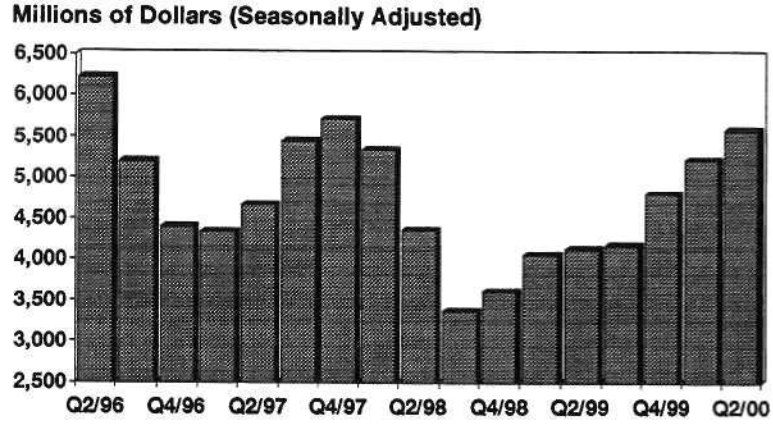
Wafer Fab Equipment Quarterly Revenue Forecast



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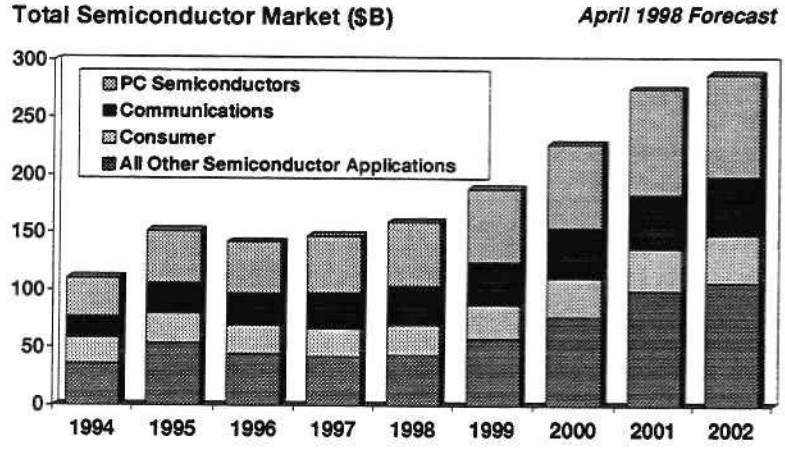
PC and Communications Drive Long-Term Growth for Semiconductors



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What's the Electronic Equipment Growth in 1998?

	1997		1998	
	$B	Growth	$B	Growth
Data Processing	293.9	9.3	324.2	10.3
Communications	214.2	13.1	229.4	7.1
Consumer	165.6	-0.9	169.3	2.2
Transportation	43.0	2.9	46.0	7.1
Industrial	133.5	5.3	141.7	6.1
Mil/Aero	56.5	2.4	58.3	3.2
TOTAL	906.6	6.8	968.9	6.9

Recent Asian financial crisis impact reduces 1998 growth to 4.4%

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Impact of Semiconductor Demand Stalling in 1998

- Asian economic slowdown impacting demand
- Reduction in semiconductor forecast for 1998
  - Original 8% growth forecast now optimistic
  - Most likely forecast +1.4%, essentially flat
  - Represents 15% swing from year ago forecast
- Bottom line
  - Adds a "holding pattern" year to forecast
  - Delays recovery pattern one year
  - Next 12 months becomes a "minimum investment" period

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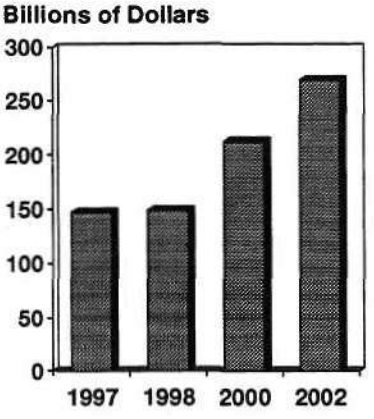
Chip Demand for Spending Model



- Reduced demand
  - View as permanent loss of market or permanent delay
- Lower 1998 by 6-7%
  - Carried through all future years
- Semiconductor market
  - Market size in 2002 reduced from $287B to $270B

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Previous Wafer Fab Equipment Forecasts: Question in Chip Demand Stalls Market

	7/95 Forecast (%)	7/97 Forecast (%)	7/98 Forecast (%)
1996	21	13	13
1997	-5	-10	-7
1998	2	7	-17
1999	16	26	3
2000	32	44	37

- DRAM pricing still depressed
- Recovery dashed in 1998 by economic issues: One-year delay
- Technology buying now more selective
- Weak 1998 chip market means weak 1999 equipment growth

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Building an "Upside Possibility" Case for Spending in 1999

- Need a stronger chip market in 1998
- Current semiconductor demand for 1998: +1.4%
  - Models only a seasonal pickup in H2/98
- Upside 1999 spending assumptions
  - 2H/98 PC recovery initiated
  - Semiconductor growth in 1998: 7-9%
  - Economic conditions stabilize in A/P year-end
  - Sets stage for very strong 1999 chip market
- Likely first places to reinitiate spending early
  - Intel, foundries

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How Will the "Upside Possibility" Case for Spending in 1999 Unfold?

- By mid-1999
  - DRAM market still in oversupply & break-even
  - MPU, PC chip capacity utilization up
  - Consumer electronics areas also up
- Likely first places to reinitiate spending early
  - Intel
  - Foundries
  - Select others
- Logic equipment sets lead recovery
- Wafer Fab Equipment +10-11% to $18.4 billion
- DRAM capacity follows as projected in 2000

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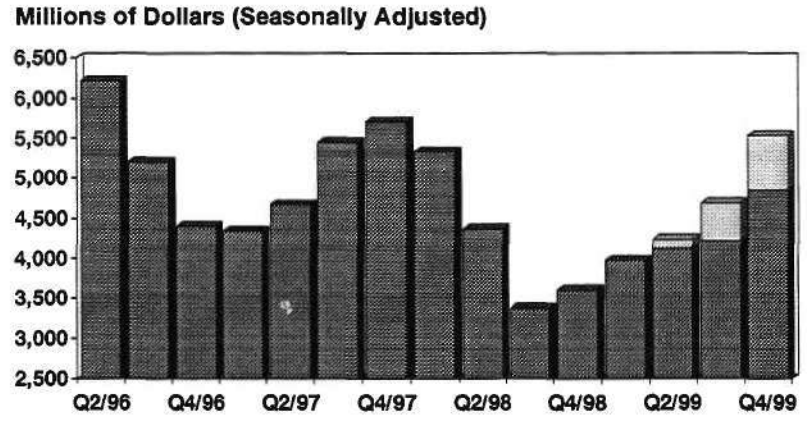
Wafer Fab Equipment Quarterly Revenue Forecast: Upside 1999 Case



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Fundamental Overcapacity Issues Still Need to Be Reconciled

- Capacity buying will drive sustainable recovery
- Capital ratio to revenues now correcting
  - Below 22% for three years 1998-2000
  - Supported by cumulative investment model
- Silicon consumption in DRAM
  - Accelerating shrinks and transition to 64Mb
  - In oversupply until 2000
- Foundry capacity outlook
  - Responding with spending cuts early
  - Likely in oversupply until 2000

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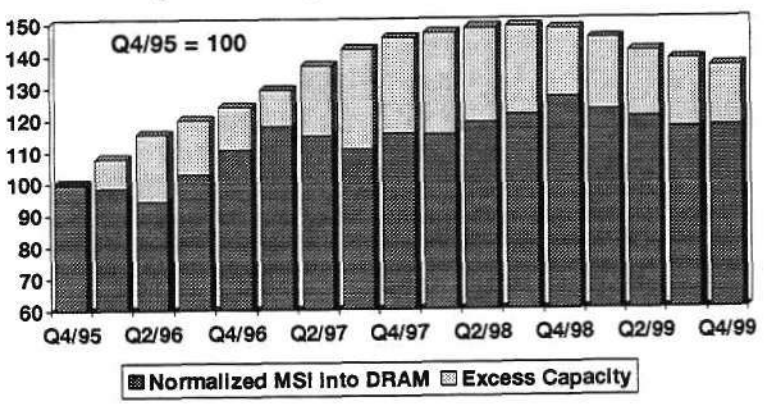
Silicon Consumption in DRAM: More than "Capacity Attrition" Is Needed



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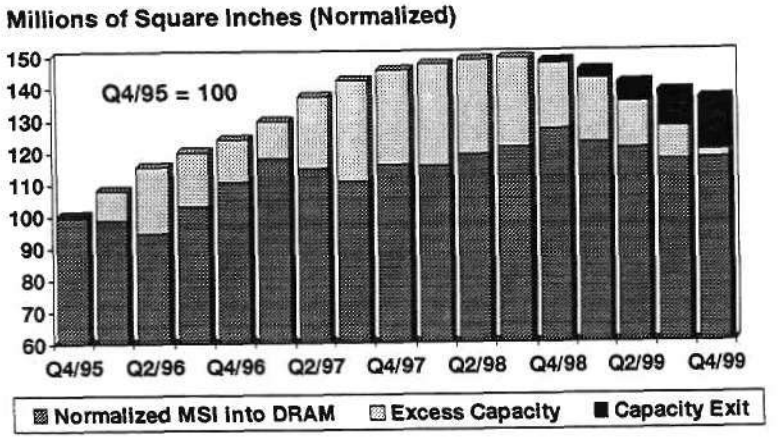
Balanced DRAM Market by End 1999: Requires "Active Exit" of Capacity



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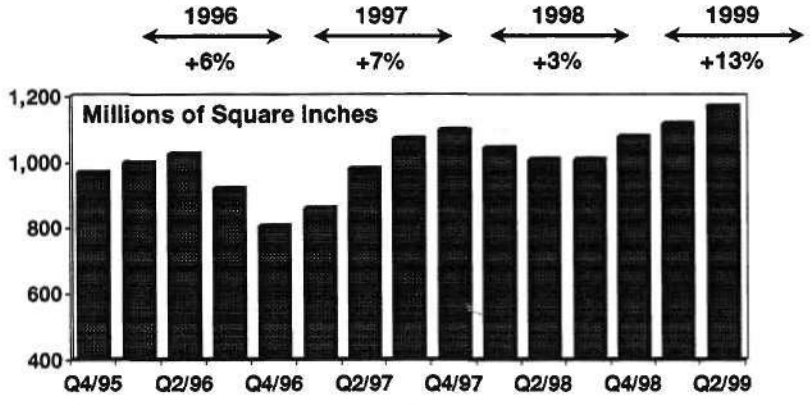
Silicon Wafer Quarterly Area History and 1998-1999 Forecast



Note: Includes test/monitor wafers, which increase from 20% to 24% of the market during 1995-1998

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Major 1998-1999 Forecast Assumptions: Korean and Taiwan Companies

- Korean companies
  - From 1996 to 1998, spending shrunk from $7.4 billion to $2.0 billion
  - Looking for return of Korean spending in 1999, perhaps 25-30% growth
- Taiwan
  - 1998: foundry up 20%, memory down 45%
  - Overall 1998 island spending down 7%
  - Foundry spending correction to continue
  - Expecting 20% lower 1999 spending
  - Upside case for 1999 is flat spending

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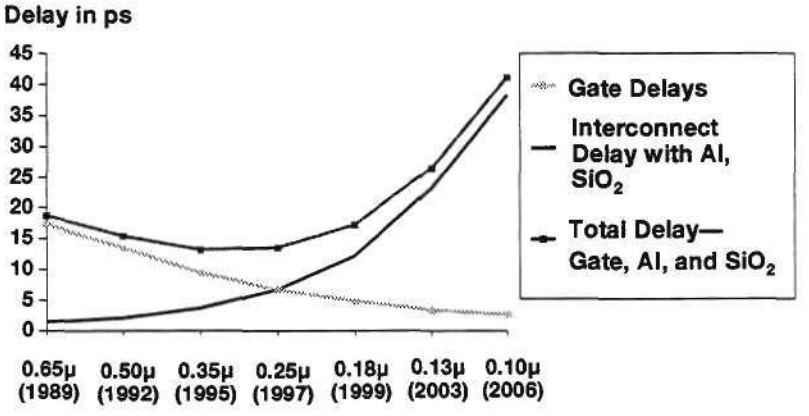
Major 1998-1999 Forecast Assumptions: Japan and Other Majors

- Japanese companies
  - Down 30% in 1998, below downside case
  - Liquidity and local economic issues
  - Modest 6-8% spending recovery in 1999
  - Upside case limited
- U.S. and European majors
  - Down 5-10% in 1998, below downside case
  - Response to demand issues
  - Forecasting 7-10% spending recovery in 1999
  - Upside possibility for 1999 is +13-15%

Equipment Technology Issues: Where Is the Action?

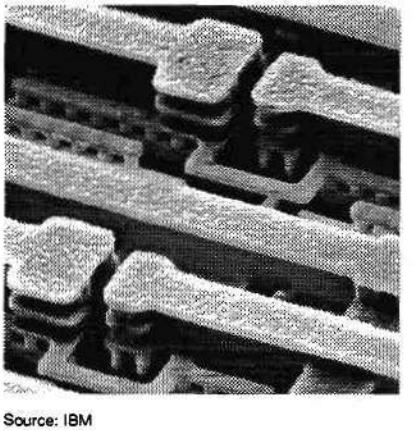
Interconnect Challenges for Logic: Density and Speed



Source: Mark Bohr, Intel, 1995 IEDM, SIA Roadmap

IBM Announces Copper Technology for Production

- Sept. 22, 1997
- 6 levels of copper
- Dual Damascene
- SiO_2 initially >low k
- Burlington VT 1H98
- 10- to 15-year effort
- Details: IEDM—Dec. 97
- DQ speculations



Source: IBM

Interconnect Module Impact for Copper with Dual Damascene

Module	Today: Conventional	Tomorrow: Damascene	Future: Dual Damascene
Lithography	2	2	2
Deposition	3 (1-D, 2-M)	4 (2-D, 2-M)	2 (1-D, 1-M)
Etch	2 (1-D, 1-M)	2 (D)	2 (D)
CMP	2 (1-D, 1-M)	2 (M)	1 (M)
Total (Modules/Layer)	9	10	7

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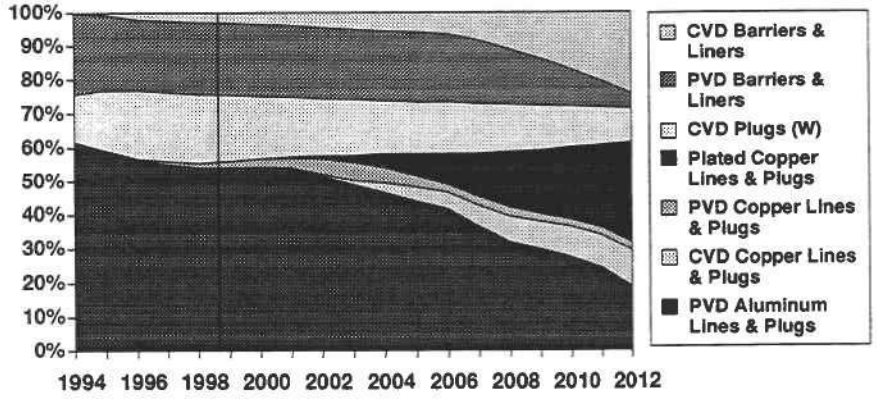
Impact of Interconnect Solutions on BEOL Metal Equipment Mix

Annual MLM Metal Equipment Sales — % $ Mix



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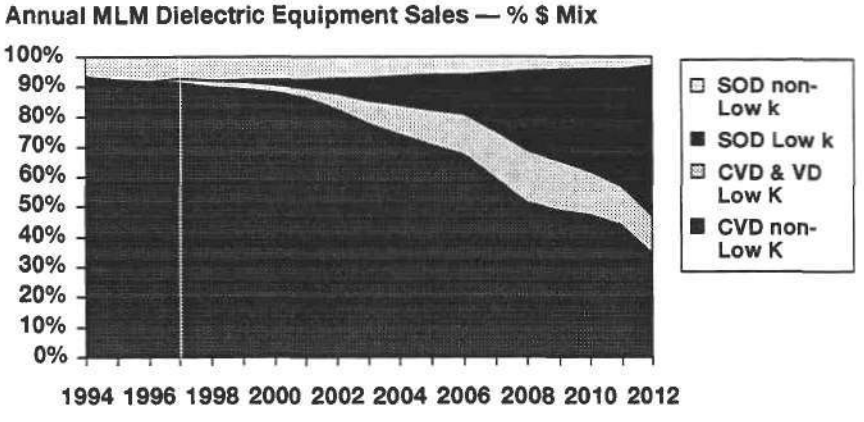
Impact of Interconnect Solutions on BEOL Dielectric Equipment Mix



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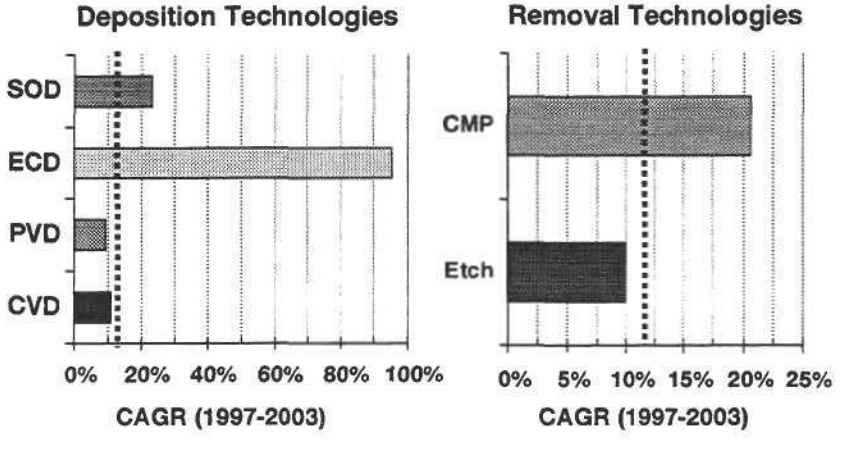
Impact on Equipment Segment Growth: ECD, SOD, and CMP Are Hot Growth Areas



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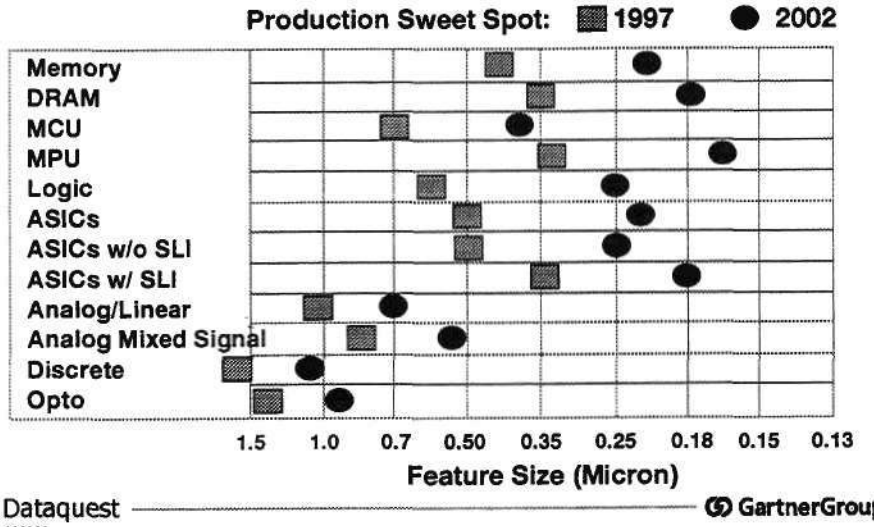
Feature Size Reduction in Semiconductors: Fuel for High Growth in Lithography



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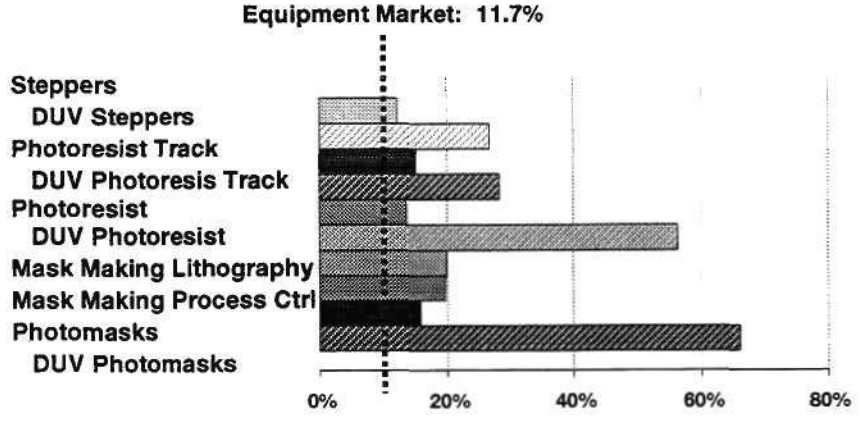
Growth for Lithography Segments: Leading Edge Applications Drive Growth



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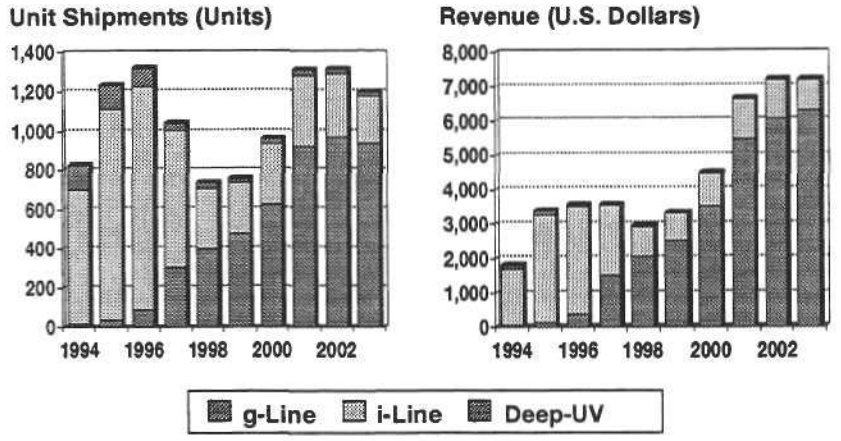
Stepper Forecast: DUV Ramp Is Strong but Slowing ... I-Line Is NOT Dead!



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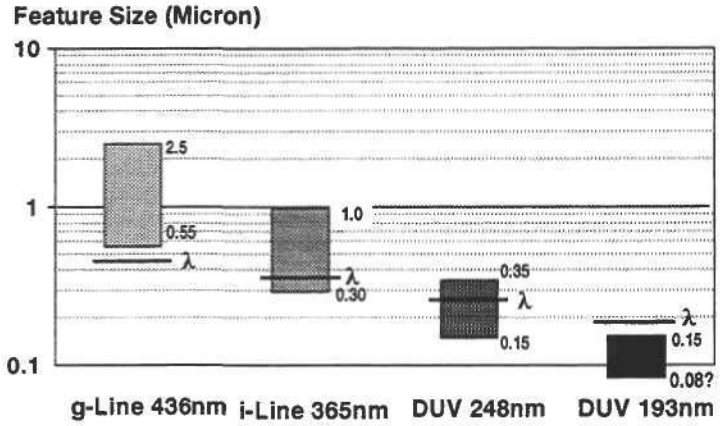
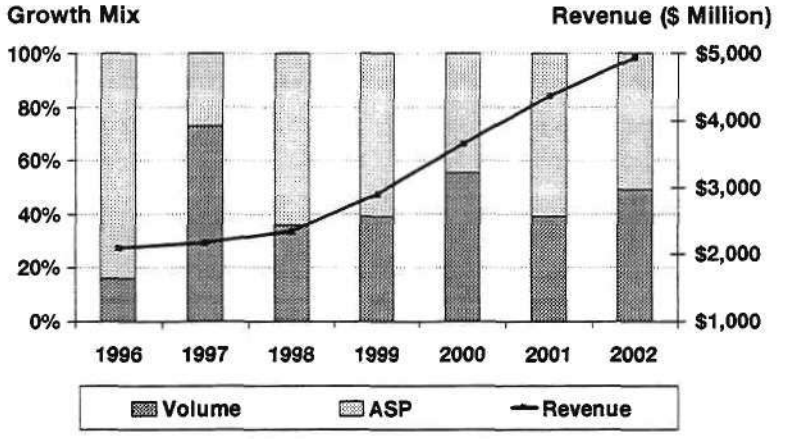
Mask Technology Is Key in Extension of Optical Lithography



Dataquest
983806
GartnerGroup

Photomask from Commodity to Value Pricing: ASP Growth Dominates



Dataquest — GartnerGroup
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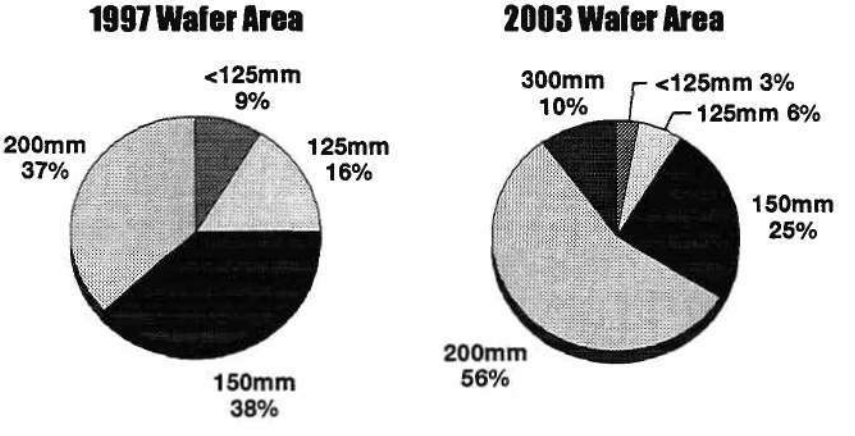
Wafer Size Distribution Forecast: 200mm Ramps and 300mm Starts



Dataquest — GartnerGroup
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Major 1998-2000 Forecast Assumptions: 300mm Investment

- Original forecast pushed out one year
  - 8-10 pilot lines in place by year-end 2001
  - Siemens appears on schedule year-end 1998
- Timing of feasibility spending
  - Started in 1997, goes through 2001
  - Bulk in 1999-2000
  - Initial production 2001-2002, ramp 2003 to 2004
- Japanese companies
  - Bring equipment into an "R&D Center" rather than a dedicated 300mm line
  - Keeps investment down in short term

Dataquest — GartnerGroup
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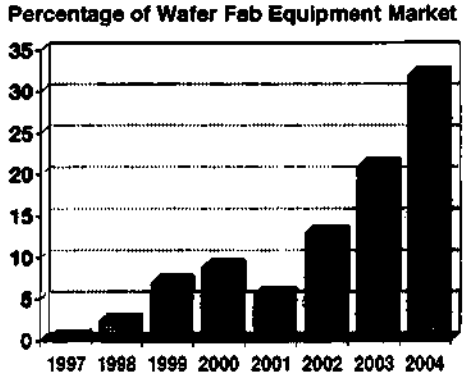
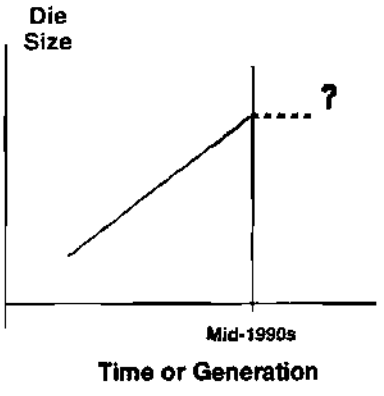
Percentage of Wafer Fab Equipment Shipped as 300mm



- Equipment sales to follow traditional "double hump" pattern for new technology
- Initial sales should be larger than in past size transitions
- 300mm generation should follow 200mm penetration path by 10 to 11 years
- Economics questionable before 2002

Dataquest — GartnerGroup
983810

Is the Motivation for Larger Wafers Still There, and as Intense?



- The 100 Rule governs
- Is the die size increasing at the same rate as before? At all?
- Is there a departure in strategy for the MPU with the Pentium II and Slot 1?
- More shrinks per DRAM generation—causing wafer sizes to have longer lives
- Will SLI and ASIC strategies enter as a driver?

Conclusions

- Near-term outlook
  - 1998 a "holding pattern" year for demand
  - Next 12 months: minimum investment
- Capacity overhangs market next 12-18 months
- Interconnect changes foster new materials and processes: ECD, SOD, and CMP
- Rapid shrinks bode well for lithography
  - DUV stepper ramp continues at slower rate
  - Photomask industry is strongest gainer
- Need healthy chip industry to drive next boom
- Upside 1999 spending depends on strong H2/98

Acknowledgments

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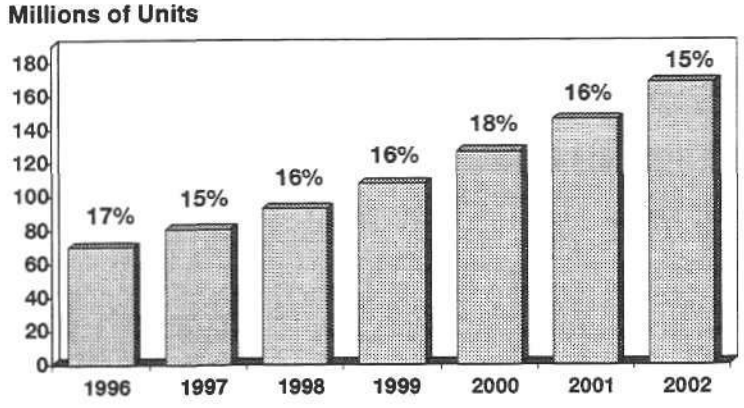
- Joan Brown
- Ronald Dornseif
- James Hines
- Klaus Rinnen
- James Seay
- George Shiffler
- Barbara Van
- Amy Worley

SEMI—Industry Strategy Symposium 1998

Supplemental Slides

GartnerGroup

Worldwide PC Forecast



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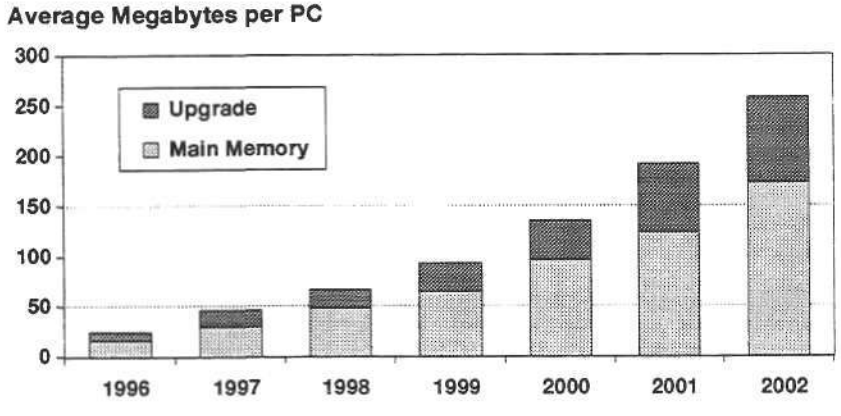
DRAM Megabytes per System



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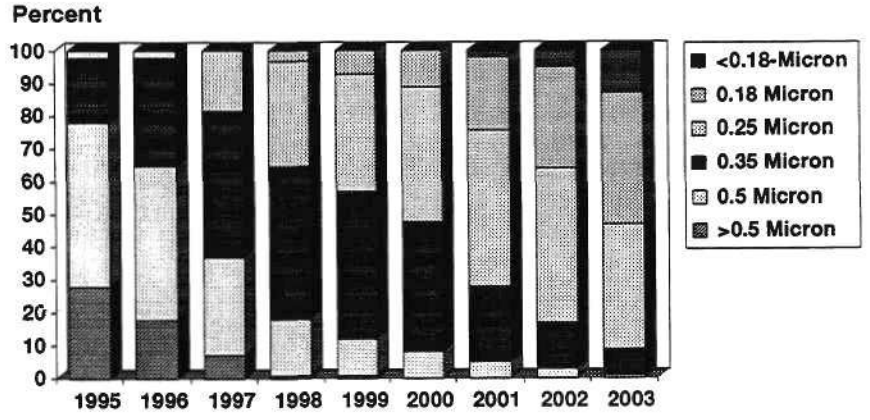
Allocation of Equipment by Line Width Driven by Volume Production



Dataquest — GartnerGroup

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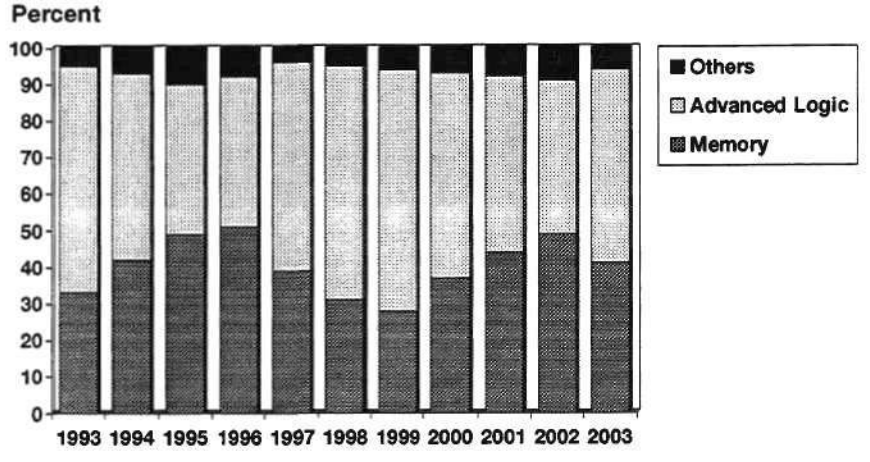
Capital Spending Mix by Application: Cycles Driven by Memory



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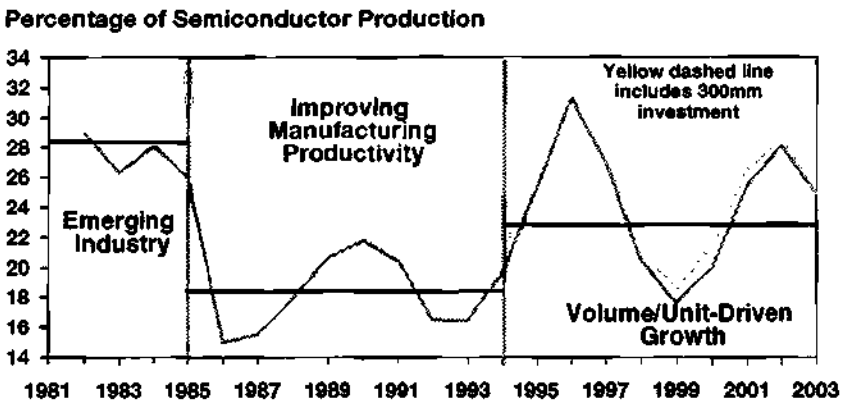
Capital Spending as a Percentage of Semiconductors: Finally Correcting



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Top 10 Capital Spenders in 1998

1997 Rank	1998 Rank		Projected 1998 Spending ($M)	Percent Change
1	1	Intel	3,700	-18
12	2	Motorola	1,550	34
2	3	Siemens AG	1,351	-22
10	4	UMC Group (incl JVs)	1,316	10
5	5	NEC	1,258	-14
21	6	Advanced Micro	1,200	66
11	7	IBM Microelectronics	1,200	2
9	8	TSMC Group (incl JVs)	1,095	-11
18	9	Winbond Group (incl JVs)	1,083	24
7	10	Toshiba	1,031	-25

Dataquest — GartnerGroup

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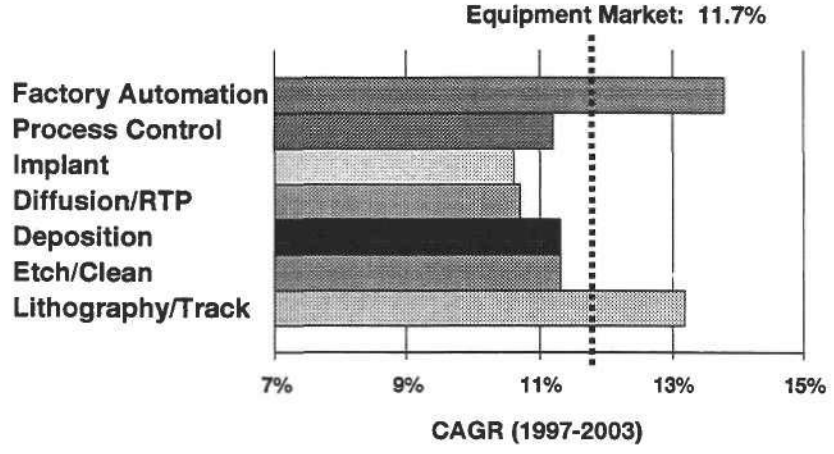
Growth Rates for the Major Wafer Fab Equipment Segments



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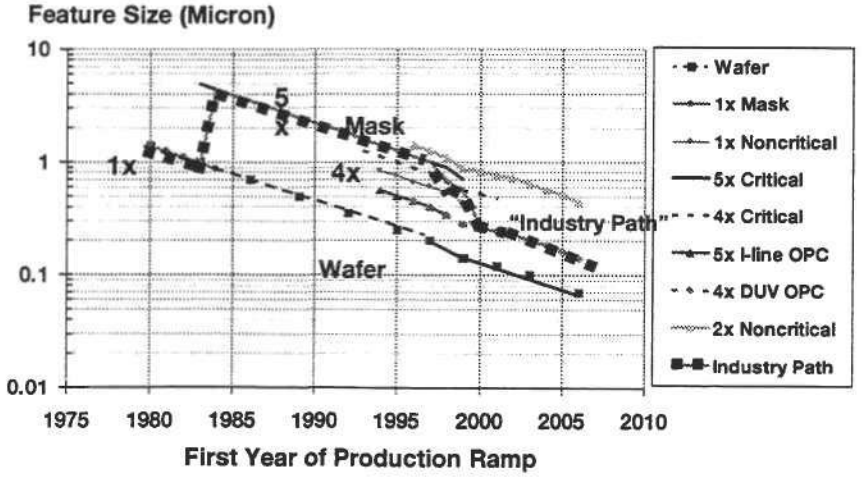
Comparison of Wafer and Mask Minimum Feature Sizes for Advanced Photomasks



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Photomask Volume Forecast: Continued Growth with Strong Shift to Sub-0.5 Micron

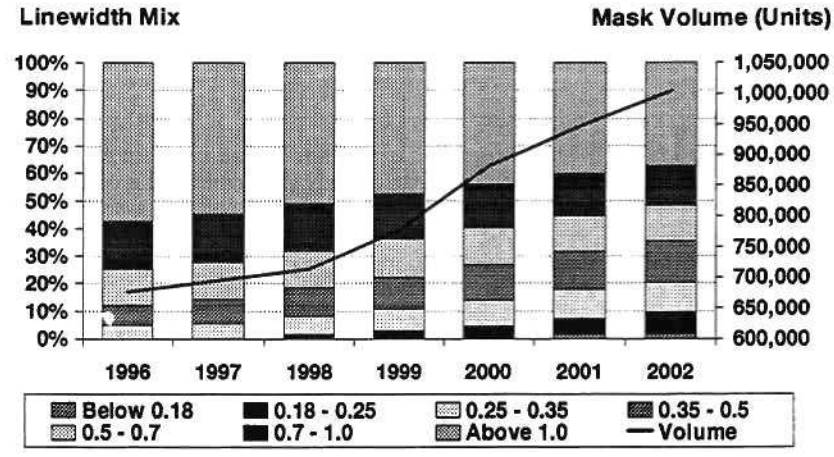

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Table 1

Capital Spending Forecast, 1997-2003 (Millions of U.S. Dollars)

	1997	1998	1999	2000	2001	2002	2003	1997-2003 CAGR (%)
Total Capital Spending	40,505	31,583	32,990	45,749	68,302	77,164	76,784	11.2
Percent Growth	-9.9	-22.0	4.5	38.7	49.3	13.0	-0.5	
Percent of Semiconductors	*27.3*	*21.0*	*18.6*	*21.4*	*26.4*	*28.5*	*24.8*	
(if 300mm pilot excluded)	*27.2*	*20.6*	*17.6*	*20.0*	*25.5*	*28.1*	*24.8*	
Americas	14,178	11,721	12,951	16,002	21,544	25,029	28,124	12.1
Percent Growth	0.5	-17.3	10.5	23.6	34.6	16.2	12.4	
Japan	7,986	5,586	6,356	9,084	13,477	14,173	12,144	7.2
Percent Growth	-17.3	-30.0	13.8	42.9	48.4	5.2	-14.3	
Europe	4,089	3,822	3,968	5,512	8,108	9,735	9,002	14.1
Percent Growth	-18.8	-6.5	3.8	38.9	47.1	20.1	-7.5	
Asia/Pacific	14,253	10,453	9,715	15,151	25,173	28,227	27,514	11.6
Percent Growth	-11.7	-26.7	-7.1	55.9	66.2	12.1	-2.5	

Source: Dataquest (July 1998)

Table 2

Wafer Fab Equipment Forecast, 1997-2003 (Millions of U.S. Dollars)

	1997	1998	1999	2000	2001	2002	2003	1997-2003 CAGR (%)
Total Wafer Fab Equipment	20,171	16,689	17,179	23,542	35,266	39,382	39,258	11.7
Percent Growth	*-7.0*	*-17.3*	*2.9*	*37.0*	*49.8*	*11.7*	*-0.3*	-
Americas	6,720	6,004	6,619	8,042	10,583	12,308	14,009	13.0
Percent Growth	15.3	-10.7	10.2	21.5	31.6	16.3	13.8	-
Japan	5,047	3,783	4,122	5,945	8,903	9,205	7,950	7.9
Percent Growth	-22.9	-25.0	9.0	44.2	49.8	3.4	-13.6	-
Europe	2,380	2,350	2,501	3,311	4,593	5,146	5,001	13.2
Percent Growth	-15.4	-1.3	6.4	32.3	38.7	12.0	-2.8	-
Asia/Pacific	6,024	4,552	3,936	6,244	11,187	12,724	12,298	12.6
Percent Growth	-7.2	-24.4	-13.5	58.6	79.2	13.7	-3.3	-

Source: Dataquest (July 1998)

Table 3
Wafer Fab Equipment Revenue Forecast of Selected Equipment Segments, 1997-2000, 2003

Equipment Segment	1997	1998	1999	2000	.....	2003	1997-2003 CAGR
($ million)							
Worldwide Fab Equipment	*20,171*	*16,689*	*17,179*	*23,542*	.....	*39,258*	*11.7%*
% Change	*-7.0%*	*-17.3%*	*2.9%*	*37.0%*	.....	*-0.3%*	
Steppers	3,562	2,908	3,114	4,397	.....	7,100	12.2%
Track	1,206	987	1,115	1,637	.....	2,800	15.1%
Automated Wet Stations	954	804	769	1,017	.....	1,689	10.0%
Dry Etch	2,939	2,316	2,331	3,131	.....	5,177	9.9%
Dry Strip	321	265	272	357	.....	540	9.1%
Chemical Mechanical Polishing	518	489	528	806	.....	1,587	20.5%
Spin-on Deposition	117	102	107	148	.....	404	23.0%
Tube CVD	603	505	512	753	.....	1,047	9.6%
Non-Tube Reactor CVD	2,078	1,761	1,804	2,365	.....	3,910	11.1%
Sputtering	1,389	1,168	1,184	1,530	.....	2,350	9.2%
Electrochemical Deposition	6	30	49	72	.....	351	95.0%
Epitaxial Silicon Reactors	226	174	175	253	.....	370	8.6%
Diffusion	533	383	381	529	.....	793	6.9%
RTP	273	251	255	368	.....	688	16.7%
Medium Current Implant	272	201	192	251	.....	336	3.6%
High Current Implant	394	292	289	430	.....	699	10.0%
High Voltage Implant	246	204	209	325	.....	631	17.0%
CD-SEM	327	265	288	414	.....	684	13.1%
Thin Film Measurement	224	184	191	262	.....	445	12.2%
Patterned Wafer Inspection	564	472	485	674	.....	1,107	11.9%
Factory Automation	1,056	888	842	1,070	.....	2,116	12.3%

Note: The selected segments will not add to the total wafer fab equipment market
Source: Dataquest (July 1998)

Notes

Keynote: The PC Market—The Need for Speed

Randy Johnson
Director, Corporate Procurement, PCA Components
Compaq Computer Corporation

Mr. Johnson is director of Compaq's Corporate Procurement Group for Printed Circuit Assembly (PCA) Components, where he is responsible for developing sourcing strategies for semiconductors and interconnect consistent with Compaq's product requirements and manufacturing deployment strategies.

Before joining Compaq in 1990, Mr. Johnson was with Texas Instruments, managing the Defense Electronics High Density Interconnect Laboratory, which specializes in multichip modules and other high-density IC packaging technologies. During his 15 years with TI, Mr. Johnson held positions in the Process Automation Center, which specializes in plasma etcher design, and in the Defense Electronics Group, which specializes in advance electronics packaging design.

Mr. Johnson earned a bachelor of science degree in mechanical engineering from Southern Methodist University in Dallas, Texas.

The PC Market—
The Need for Speed

Randy Johnson
Director, Corporate Procurement
Semiconductors and Interconnect

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Compaq Computer Corporation

- Compaq is the largest PC supplier in the world
- Compaq is the second largest computer company in the world
- Compaq plays a leading role in industry standards groups
- Compaq can and does affect the market
- Compaq takes an active role in developing PC architecture, the technology and design.
- Compaq is broadening its reach to other areas where data is managed and processed.

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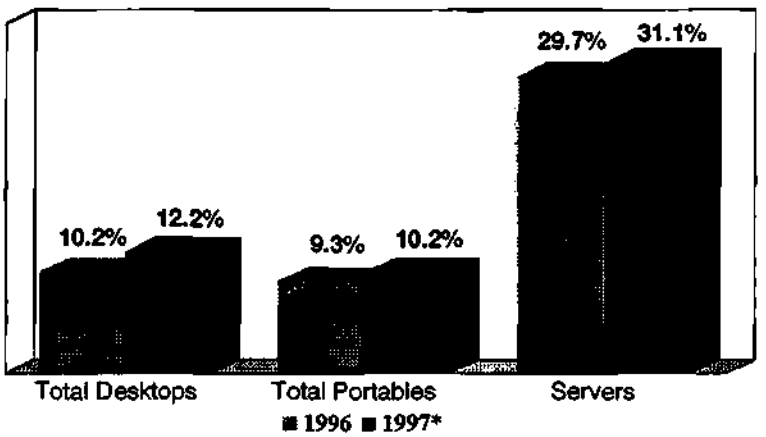
Worldwide Market Share



Source: IDC, WW PC Tracker, 12/97
* Compaq Market Intelligence Group estimate based on IDC actuals through 3Q97

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The Need for Speed?

- Customer Needs
- Innovation
- Technology Conversion
- Material Turnover

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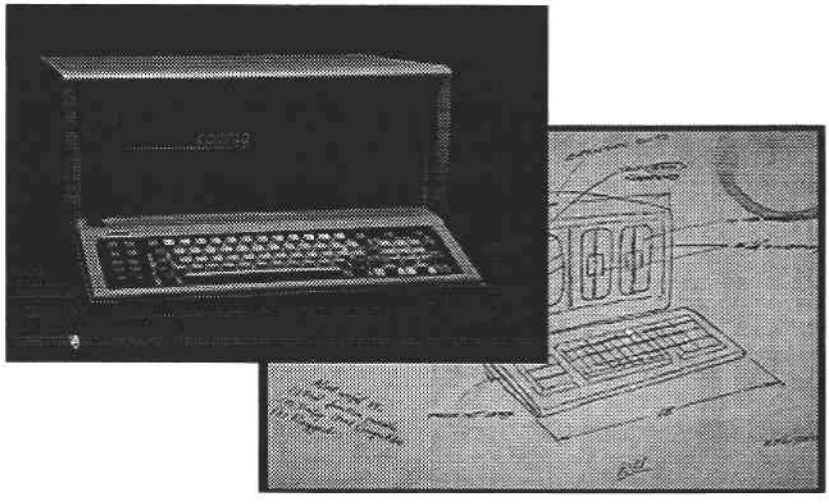
Compaq in the Beginning



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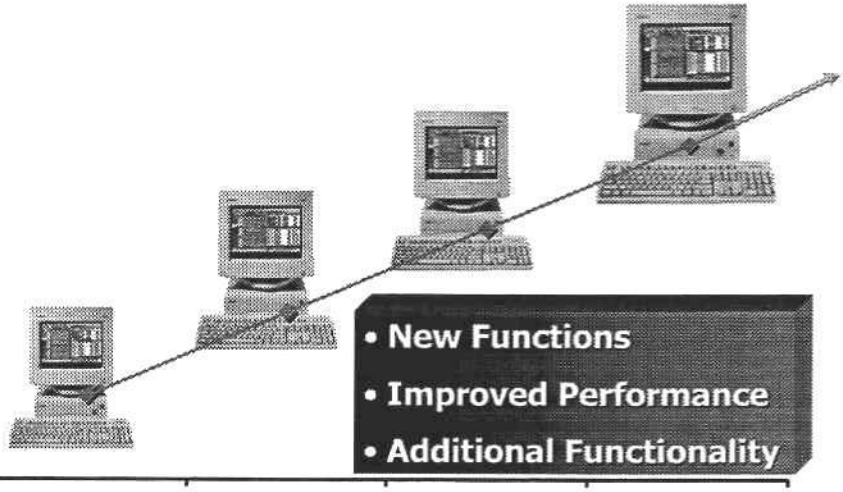
Moore's Law



Progression of Technology

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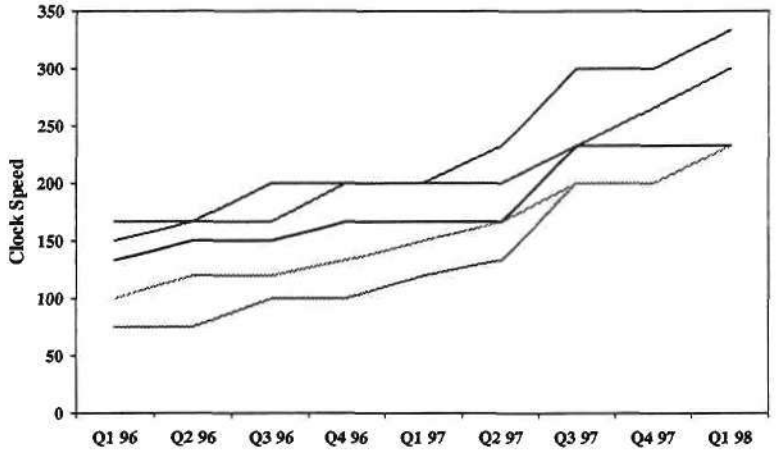
Desktop PC Processor Trends



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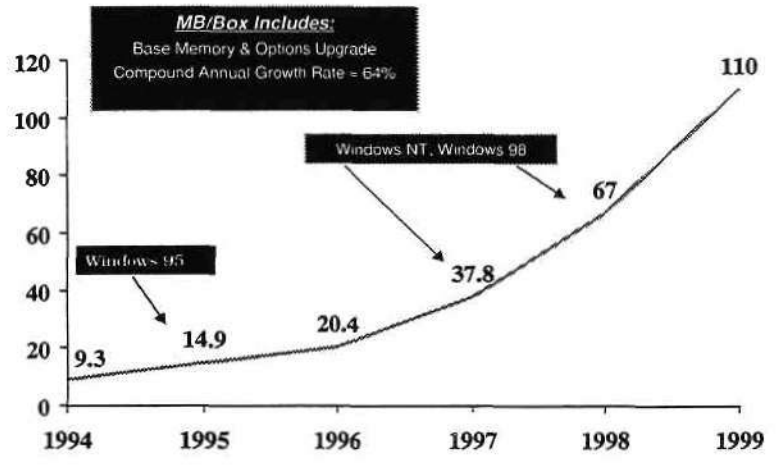
DRAM MB per Box Trends



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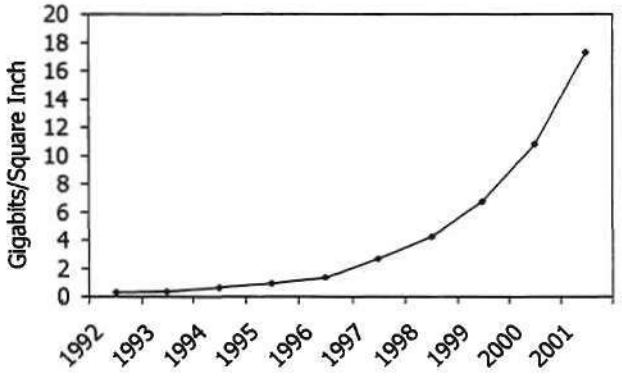
Highest Density Rigid Disk Drives



1999-2001 Projected

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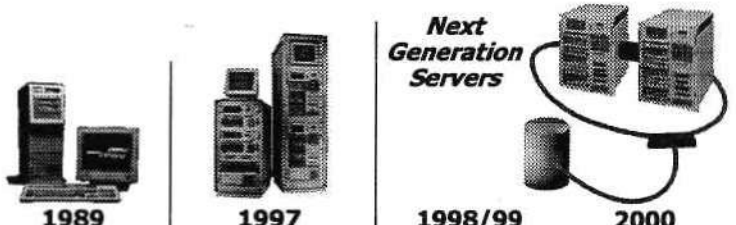
Exceptional Price and Performance For All Enterprise Applications



	1989	1997	1998/99	2000
Database Performance	150 tpm*	11,055 tpm	60/80,000 tpm	100,000 tpm
Memory	256 MB	4 GB	8 GB	16 GB
Disk Capacity	2 GB	3.5 TB	50 TB	>200 TB
Backup Performance	.5 GB/Hr	*200 GB/Hr*	*2 TB/Hr*	*Continuous*
$/TPM	$400 - 500	$44	$35/$20	$15

* Estimate of past performance

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Compaq Offers Full Range of Products
Deskpro Products for the Enterprise
Compaq Proliant
Storage & Options
Massively Parallel Himalaya® System
Mobile Products
Netelligent Communication Platform
Compaq's Handheld PC Companion
Presario Products for the Home
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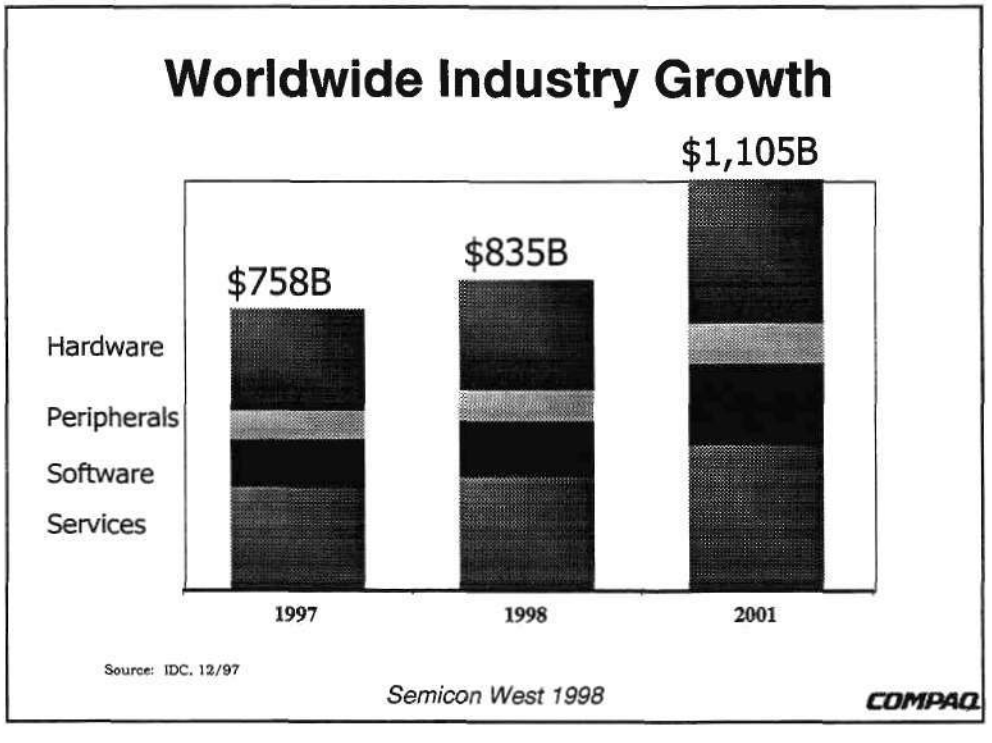
Worldwide Industry Growth
$1,105B
$835B
$758B
Hardware
Peripherals
Software
Services
1997
1998
2001
Source: IDC, 12/97
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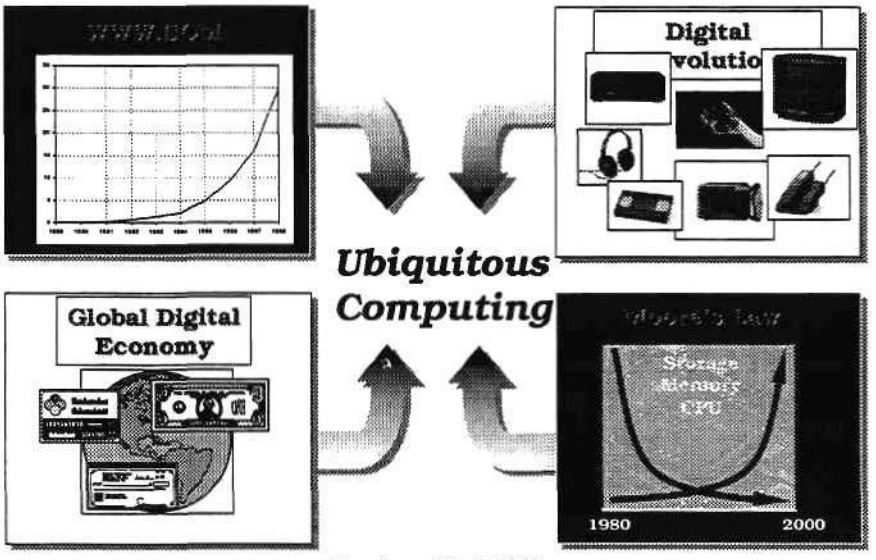
Industry Inflection Point



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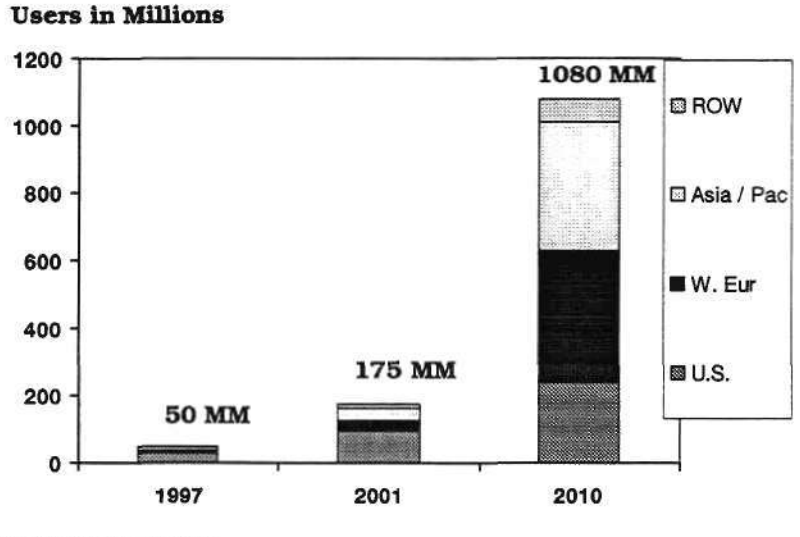
The Growth of the Internet



Source: IDC/Compaq Estimates

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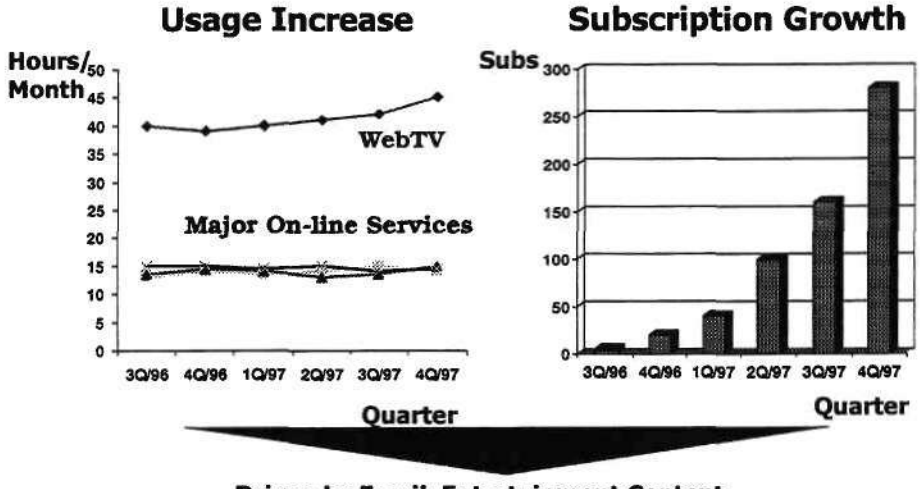
Actual Market Behaviors - WebTV



Driven by Email, Entertainment Content, Games, and Pushed News and Information

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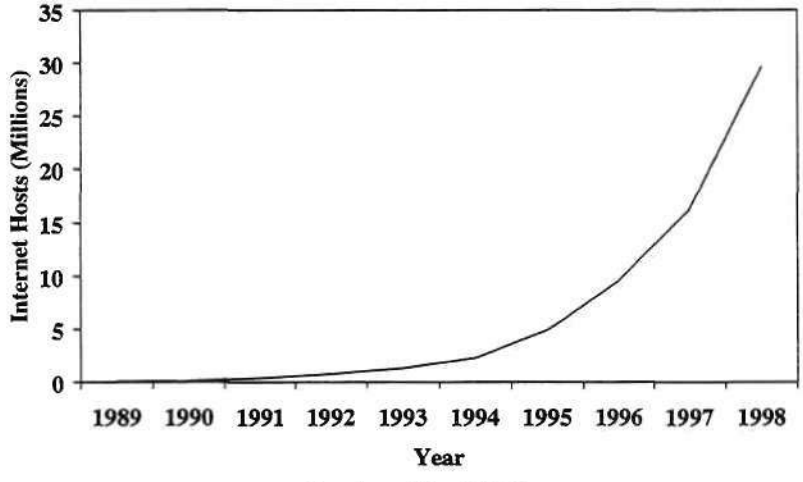
Growth of the Number of Internet Hosts



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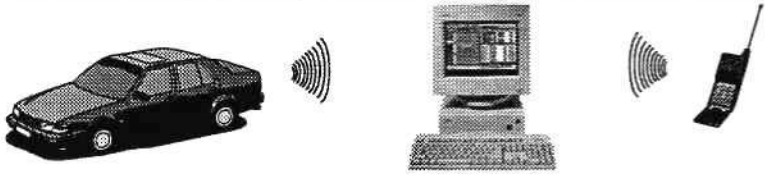
Ubiquitous IP Connectivity

IP connectivity will be needed and available essentially everywhere.

It will become an indispensable part of the infrastructure of every road, building, room, wall, vehicle, device, pocket, and purse in the developed world.

It will be IP connectivity, i.e. the exchange of real IP packets mediated by a conforming IP software stack.



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Auto Computing Evolves

Today
"Embedded Computing"

Tomorrow
"Visible Computing"

The Future
"Invisible Computing"
The Car IS the Computer

Control Functions

Engine
Braking
Transmission
Traction

Additional Functions

Additional Functions

Radar
Collision Avoidance
"Soft Options"

Data Functions

Audio
Cellular
Monitoring
Entertainment
Navigation

Integration
Additional Functionality
Single User Interface

Additional Functions

Control functions dominate

Explosion in data functions

Merging of control and data functions in "smart car"

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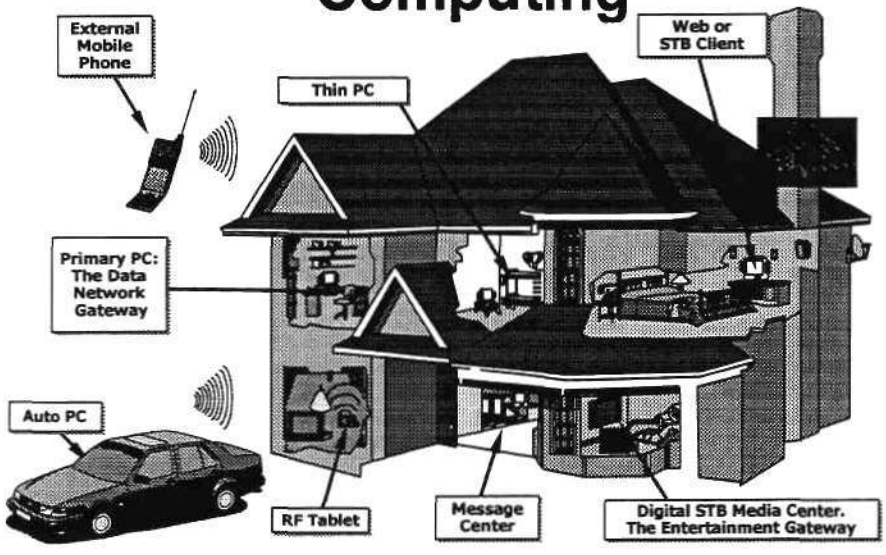
Ubiquitous Home Computing



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The Digital Television Initiative

THE DTV TEAM

BRINGING THE DIGITAL ENTERTAINMENT REVOLUTION HOME

microelectronics group

COMPAQ Microsoft intel. Lucent Technologies

- ✓ Progressive scan 720v x 1280h x 24fps ("720p" format)
- ✓ Delivers cost-effective, interactive, internet-friendly viewing
- ✓ 1080i TVs - $ 4,000 to $ 6,000 -- 780p displays - PC monitor prices
- ✓ The future of television broadcasting

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Challenges

Time to Market

Product Delivery

Understanding the Market

- Market Research is Critical!
- Who is the Customer?
- How will the product be delivered?

Product Development Cycles

Business Group	Development	Product Launch
Consumer	6-9 Months	3+ per year
Commercial	9-12 Months	1+ per year
Enterprise	12-18 Months	1+ per year

Product Development

Engineering is given the directive:

- What the product has to have
- How much it can cost and what it will sell for
- When it MUST ship

Component Selection Criteria

- Quality
- Price....Price....Price
- Stability, Reliability, Support
- Best of Class
- Must Ship on Time
- Delivery must be flexible

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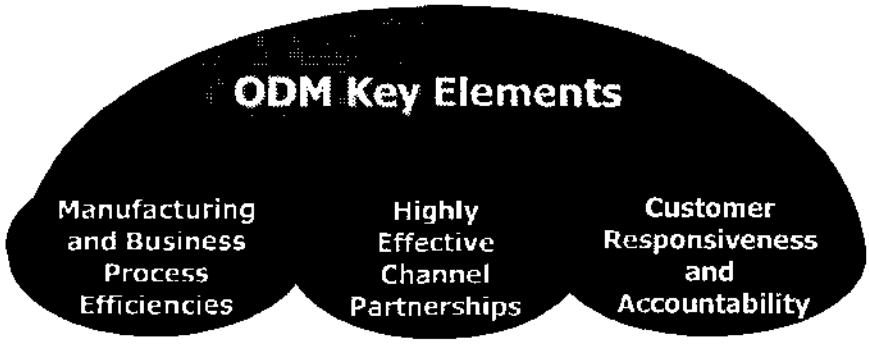
Optimized Distribution Model



- **BTO**
- **CTO**
- **CCP**

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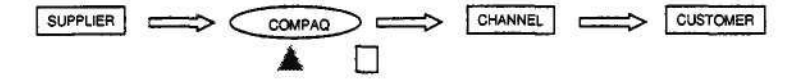
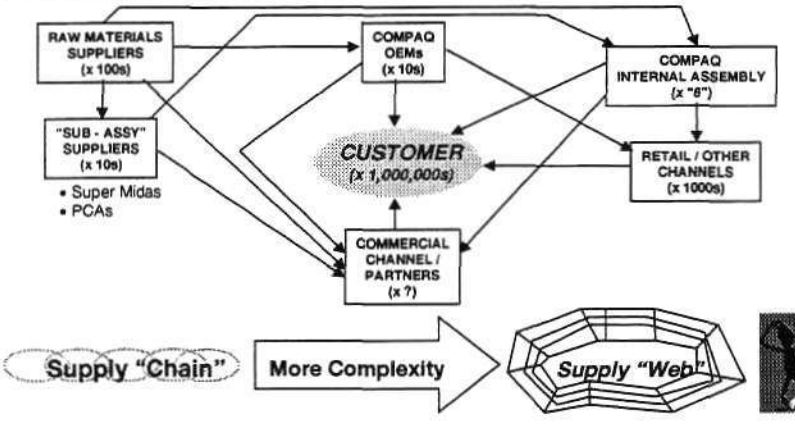
Supply "Chain" Environment Continues to Shift Due to Industry Evolution

From



To (a simplified complex illustration)



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Collaborative Delivery Model

Time to Volume

Step Ramp

Flexible Delivery

Production

The Name of the Game:
It's Not About Accurate Forecasts,
It's All About How You Manage Demand Variability

Semicon West 1998

COMPAQ

Satisfying Demand Variability Flexible Delivery

- Inventory must compensate for historic demand variability relative to cycle time
- Inventory is bad . . .
- Cycles times must be reduced to minimize inventory requirements upstream in the supply chain

The Supplier Who Can Deliver....

Useful innovation

When the customer wants it

The way the customer wants it

...will win in the end

So . . .

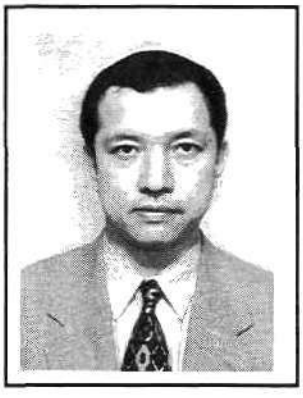
- Know your customer
- Know your customers customer
- Understand his process and challenges

And Remember . . .

Marketing is,
in many ways,
paving the path of least resistance
for the buyer.

Notes

DRAM Market Driver: Manufacturing Economics or Technology Trends?



Takashi Ogawa
Senior Industry Analyst
Semiconductor Equipment, Manufacturing, and Materials Worldwide
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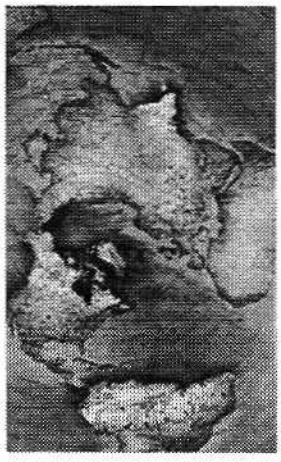
Mr. Ogawa is a senior industry analyst for the Semiconductors group and is responsible for research and analysis for the Semiconductor Equipment, Manufacturing, and Materials program in Japan.

Before joining Dataquest, Mr. Ogawa worked as a researcher and engineer in the Electronics Division of Sumitomo Metal Mining Co. Ltd. for 11 years and was engaged in many engineering projects, ranging from semiconductor materials to IC packaging technology. His main fields are high-temperature electronics materials and CVD equipment. He also worked as a member of the Investigation Committee of Japan Electronic Development Association for seven years.

Mr. Ogawa received a master of science degree in physics from Science University of Tokyo, faculty of science and engineering.



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1998 SEMICON/West Seminar—July 15

DRAM Market Driver: Manufacturing Economics or Technology Trends?

Takashi Ogawa

Senior Industry Analyst,
Semiconductors Japan

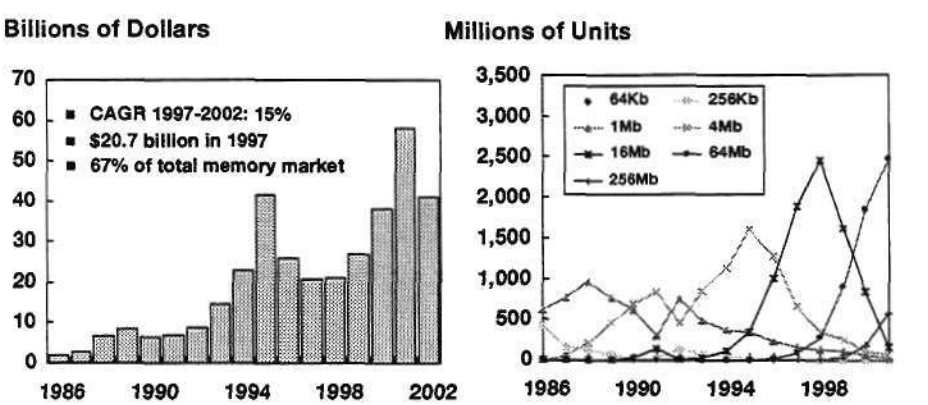
983851

Agenda

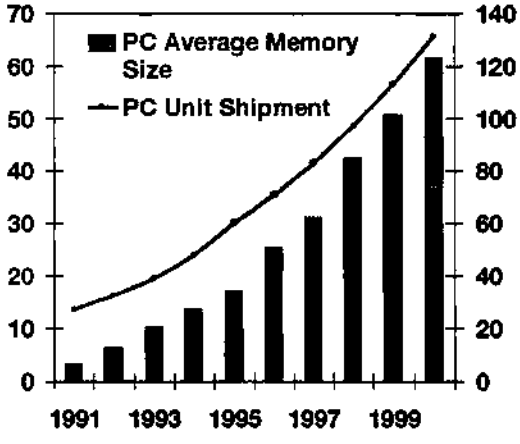
- DRAM end user's demand
- DRAM density shift
- Manufacturing economics issues
- Summary

DRAM End-User Demand

DRAM Market Trends and Forecast



PC Market Still Drives DRAM Demand in the Mid-Term



- PC unit shipments: More than double from 1997 through 2001
- DRAM in PCs: Likely to more than quadruple during the period
  - Ramp-ups of Pentium II and Windows NT
- DRAM Market for PCs
  - Over 70% of the total DRAM bits

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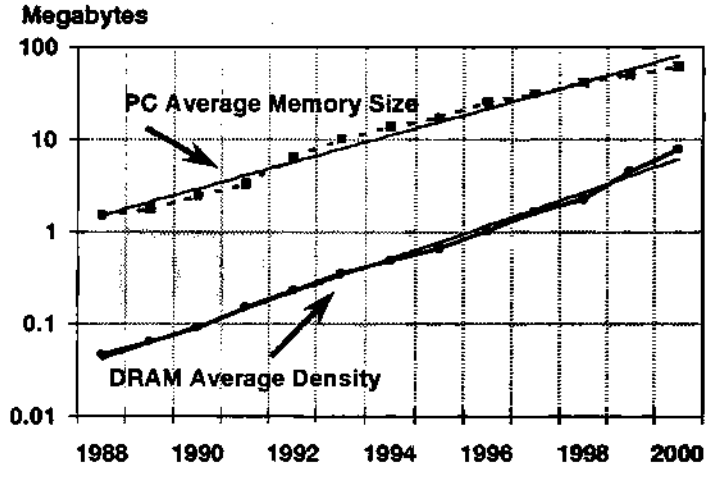
How Is DRAM Chip Density Correlated with PC Main Memory Size?



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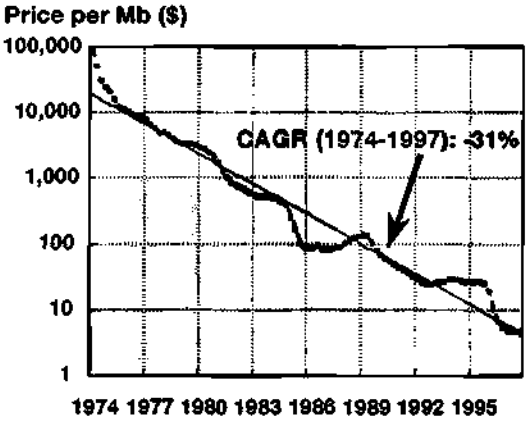
Purchaser Is More Concerned about Price per Bit



- PC market growth
  - Unit GAG 1997-2002: 16%
  - Revenue CAGR 1997-2002: 9%
  - Low-cost PC ($1,000) appears
- PC OEMs will purchase whichever DRAM density reduces their DRAM cost the most, not pay for any technology

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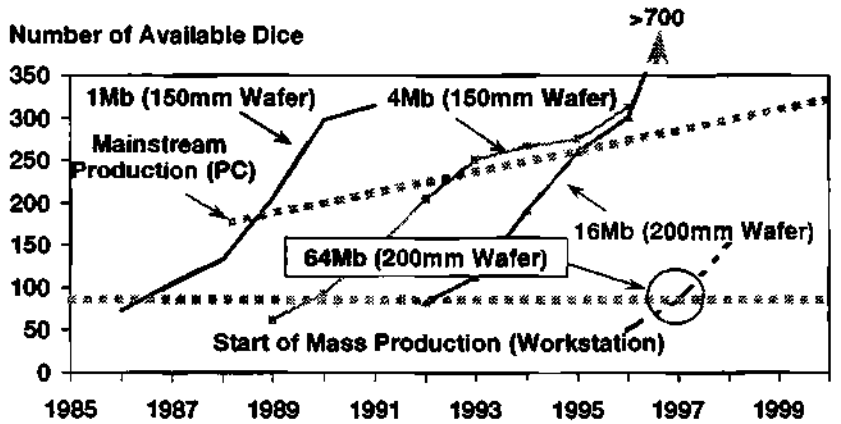
What Is Customer's or Market's Purchasing Behavior?



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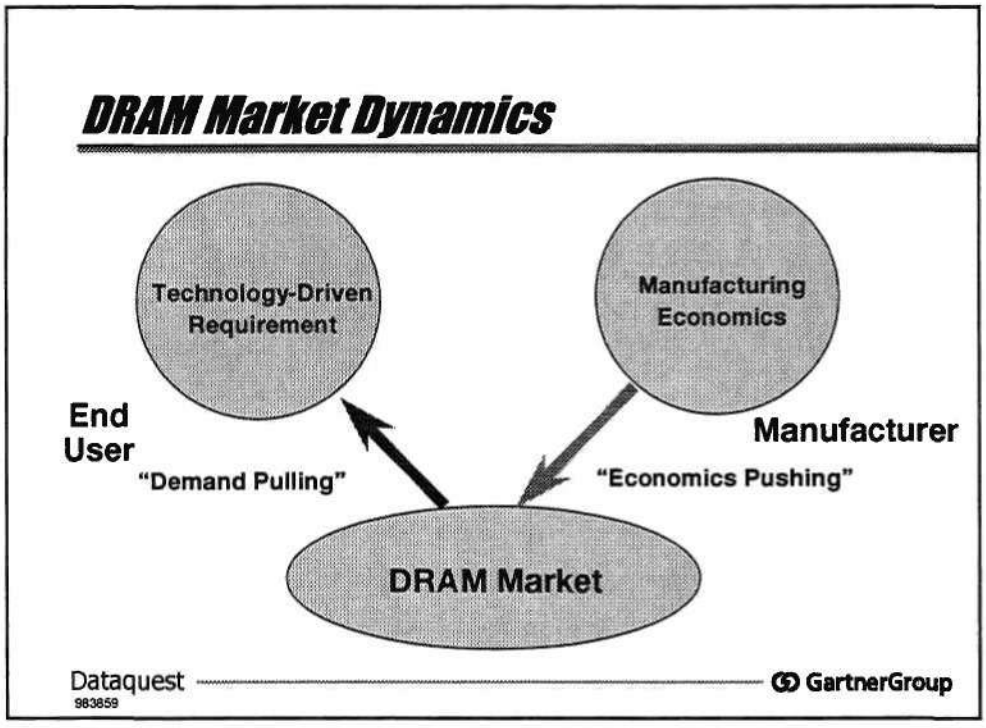
DRAM Market Dynamics
Technology-Driven Requirement
Manufacturing Economics
End User
Manufacturer
"Demand Pulling"
"Economics Pushing"
DRAM Market
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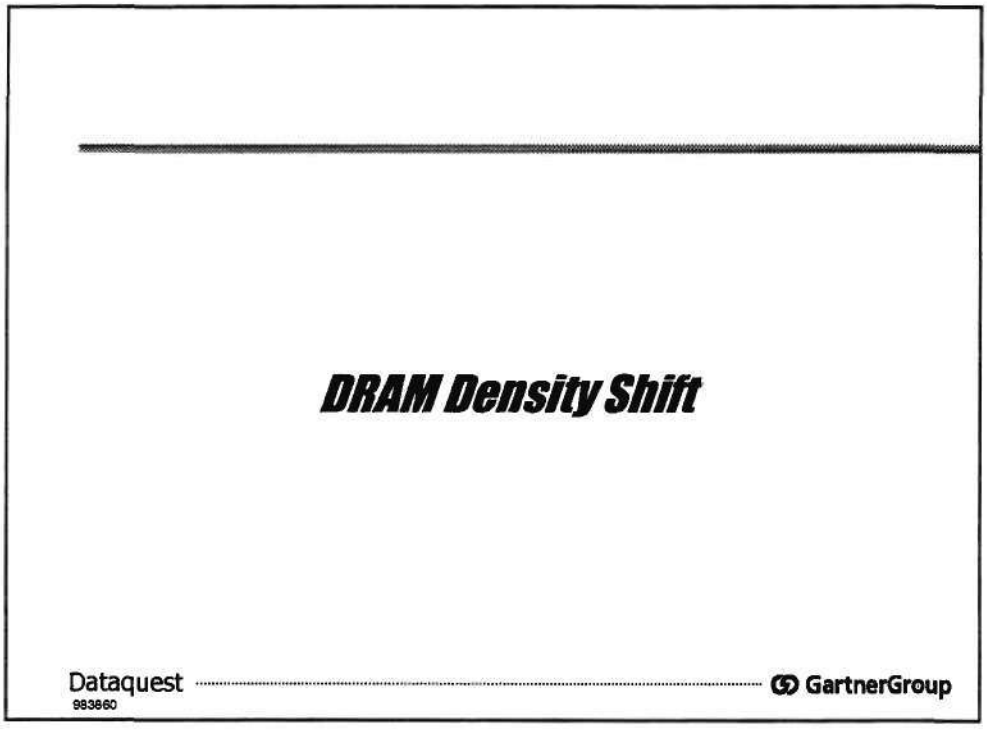
DRAM Density Shift
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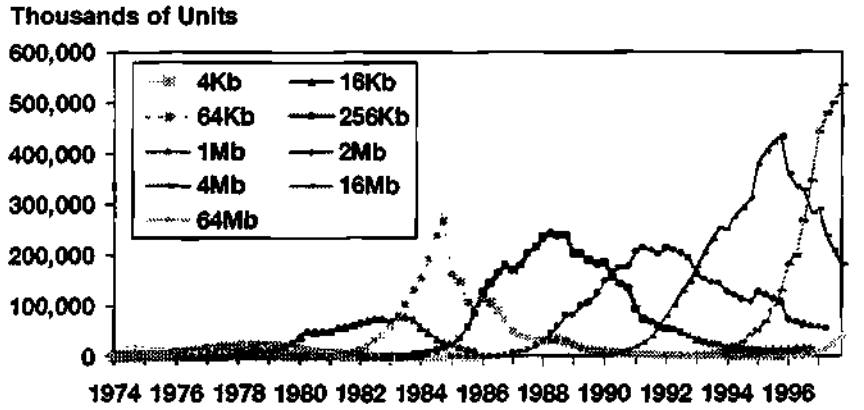
Historical DRAM Unit Shipments



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DRAM Density Crossover Points

Transition	4Kb to 16Kb	16Kb to 64Kb	64Kb to 256Kb	256Kb to 1Mb	1Mb to 4Mb	4Mb to 16Mb
Price per Bit	Q2/79	Q1/83	Q3/85	Q1/90	Q3/91	Q3/94
Bits	Q3/78	Q2/82	Q3/85	Q4/88	Q4/91	Q4/95
Units	Q3/79	Q2/83	Q1/86	Q2/90	Q1/93	Q4/96

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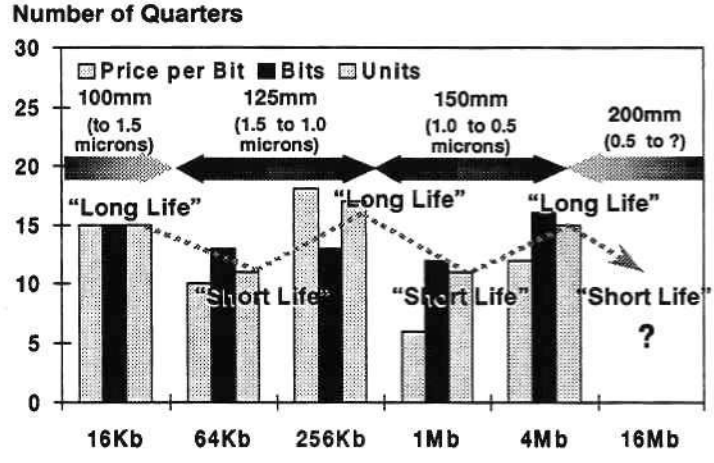
Why Has Alternating Life Cycle Period Appeared?



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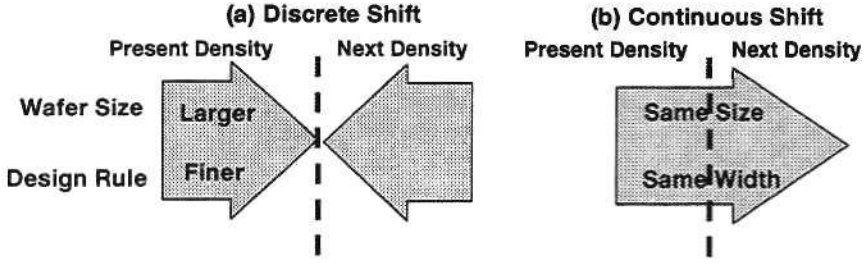
Is Initial Cost Gap for the Shift Influential in Life Cycle Period?



- Initial manufacturing cost gap in (a) is larger than in (b)
- Will the larger cost gap make it favorable for manufacturers to stay longer at present density?

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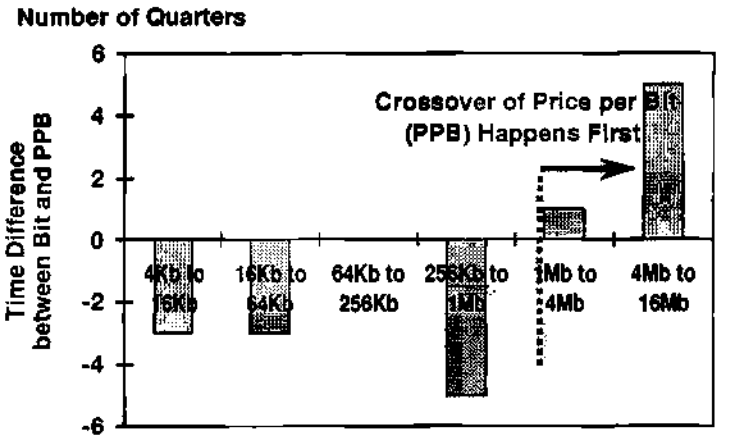
Movement to Economics-Driven Market



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DRAM Density Shift

- DRAM density shifts to the next generation with abnormal alternate "long life" or "short life," relating to the initial manufacturing cost gap for the transition
- Purchasing behavior keeps the "hundred rule" for high-end market but demands higher wafer efficiency for mainstream market
- After 1Mb, DRAM market has become economics driven

- On the other hand, how are these market characteristics related to manufacturing economics?
- How and when will the transition from 16Mb to 64Mb in mainstream market occur with technology changes?

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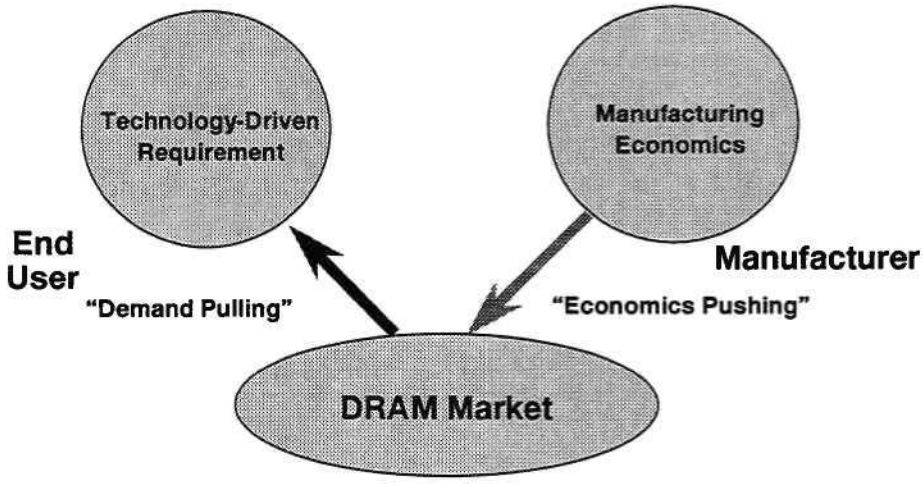
Manufacturing Economics Issues



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Wafer Cost Factors

- Variable wafer cost
  - Materials/consumable (wafers, photoresist, gas, chemicals, etc.)
  - Direct labor cost
- Fixed wafer cost
  - Depreciation of wafer fab equipment
  - Depreciation of wafer fab facilities
  - Utilities (electric, gas, water, etc.)
  - Fixed labor cost

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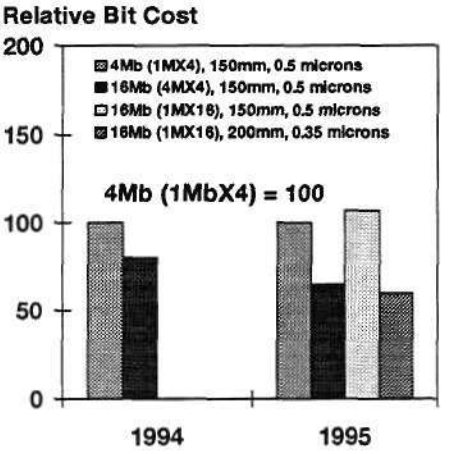
How Was Manufacturing Economics Incorporated with Market Dynamics?



DRAM Products in Early to Mid-1995

	Average Die Size (mm^2)	Estimated Net Yield (%)
4Mb (1Mx4)	50	88 to 90
16Mb (1Mx16)	90 to 95	50
16Mb (4Mx4)	80	70 to 75

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Factors for Wafer Cost Increase in the Next Generation

- Wafer fab equipment
  - DUV lithography (excimer stepper, DUV track)
  - Planalization (CMP)
  - HDP Etch/CVD
  - Metrology
  - Others
- Materials
  - High-quality wafers
  - Photoresist
- Process complexity (cell structure, etc.)

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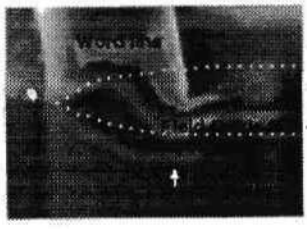
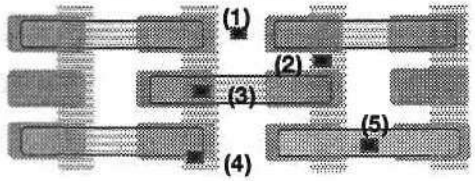
Critical Defect Level to Be More Crucial





COP Word Line Active Area Capacity

Position of COP	Expected Failure
(1) Under field oxide	Degradation of isolation characteristics
(2) Under field oxide and word line	Degradation of isolation characteristics
(3) Under gate oxide	Thinness of gate oxide film
(4) Under memory cell node	Increase of leakage current
(5) Under bit line node	Disconnection

Source: M. Muranaka, et al. Jpn J. Appl. Phys. 37(1998)

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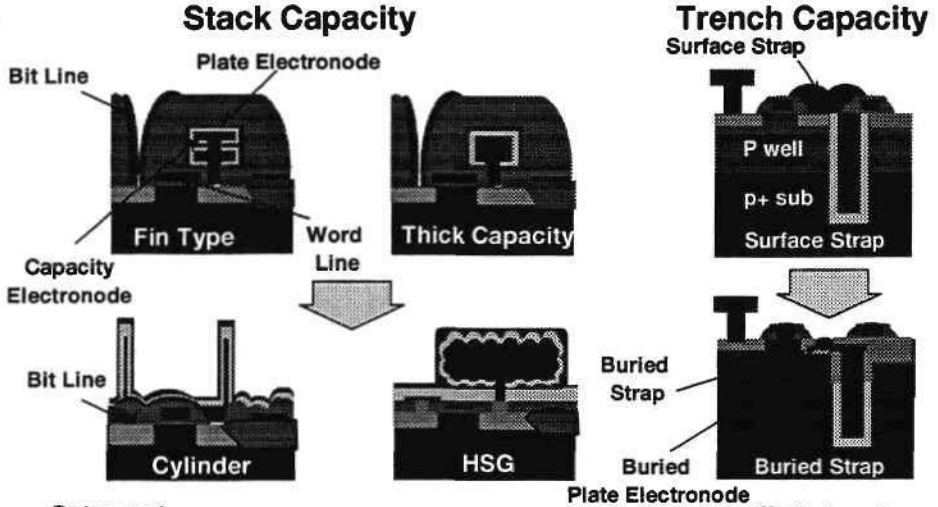
Process Complexity



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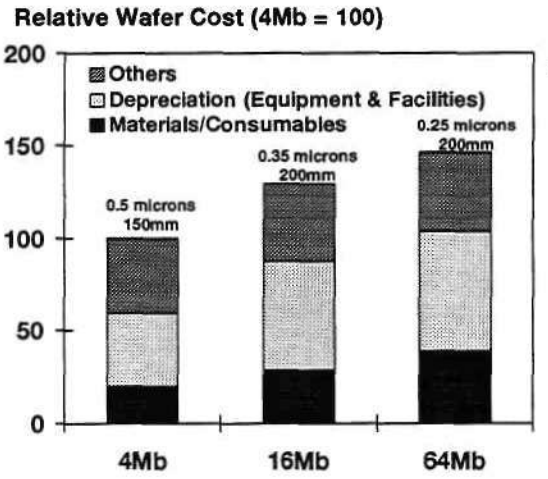
Wafer Cost Estimates for 64Mb



- Assumption
  - Cost for 4Mb = 100
  - Wafer capacity: 30K/mon.
  - Depreciation Conditions: Fixed
  - Yield: Fixed

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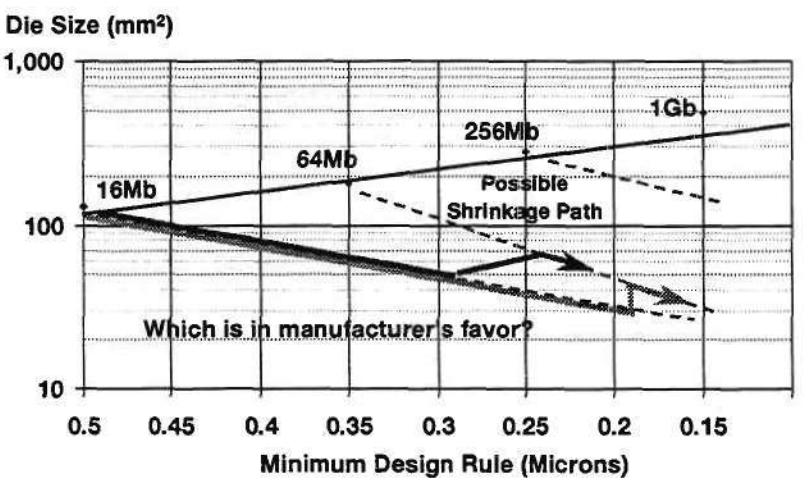
Does Manufacturing Economics Decide the Density Migration? (1)



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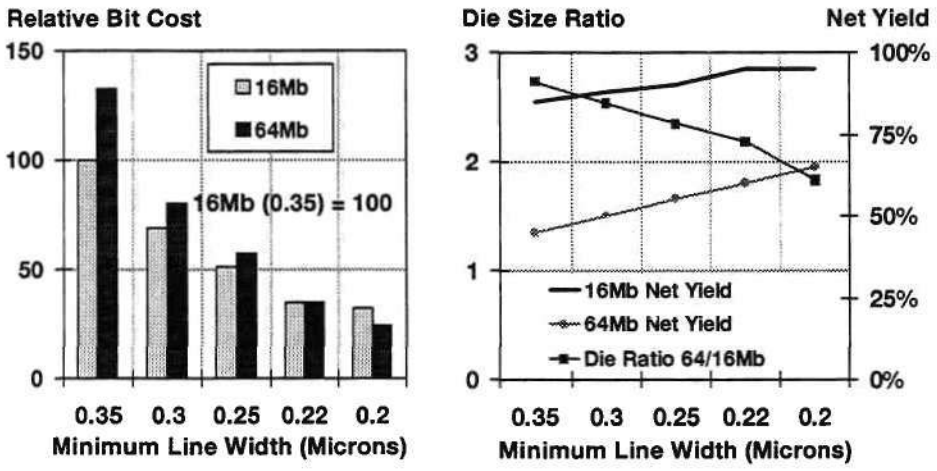
Does Manufacturing Economics Decide the Density Migration? (2)



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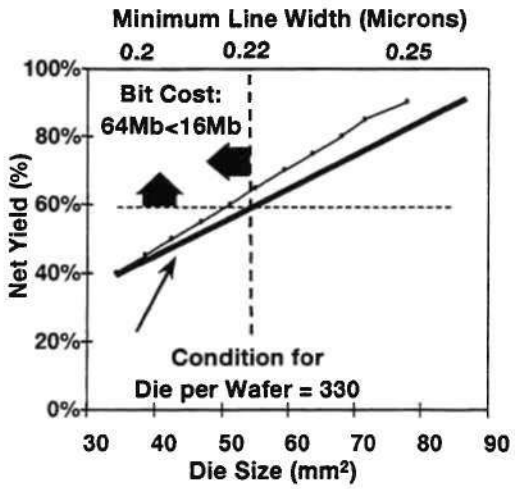
How Will Manufacturer's Wants Meet with Purchasing Behavior or Need?



- Critical net die per wafer for mainstream market (purchase behavior)
  - 1Mb: 170 dice per wafer
  - 4Mb: 230 dice per wafer
  - 16Mb: 280 dice per wafer
  - 64Mb: 330-340 dice per wafer
- Past period from "high-end" to "mainstream"
  - 2 to 3 years
- Most likely condition for 16 to 64Mb in mainstream market: 0.22 microns and net yield over 60%

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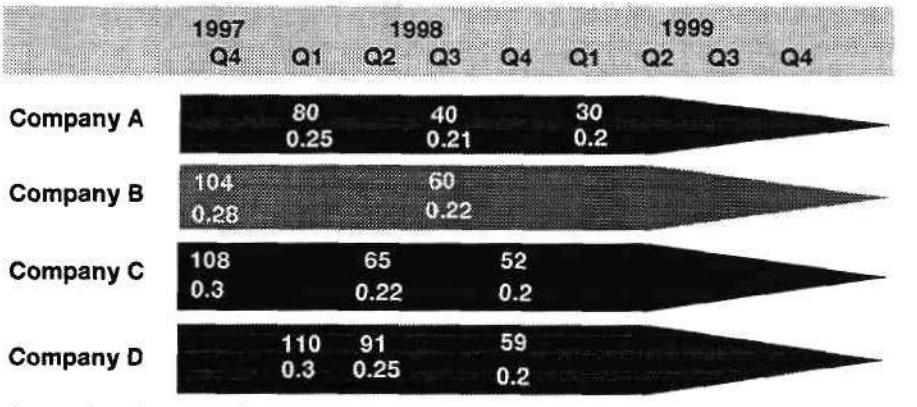
When Will It Happen? DRAM Manufacturer's Road Map for 64Mb



Upper: Die Size (mm^2), Lower: Minimum Line Width (Microns)

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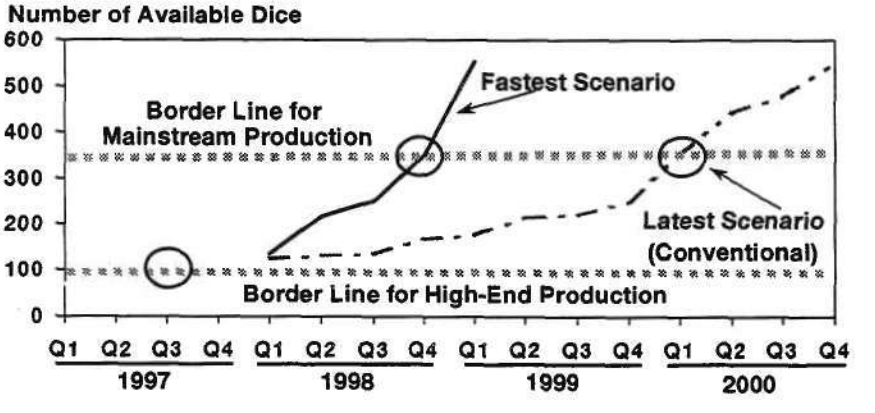
When Will 16Mb-to-64Mb Transition Occur in Mainstream Market?



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Summary

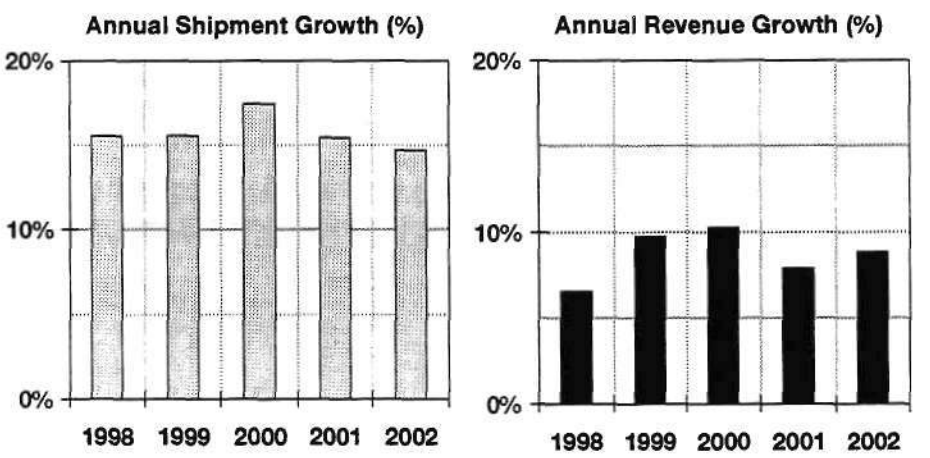
- Decisive factor of DRAM density drive: balance between "demand pull" and "economics push" with technology changes.
- Today, abandonment for short-term profitability and severe competition force suppliers to reach the condition for the density shift, earlier than in the past
- Likely condition for 16 to 64Mb in mainstream market: 0.22-micron rules and net die yield over 60 percent
- Timing of the shift: Q1/1999 in the earliest scenario and Q2/2000 in the latest scenario; need to closely watch the yield trend during 1998

Acknowledgments

- George Iwanyc
- Masahiro Suzuki—Dataquest Japan
- Jim Handy
- James Seay
- Ron Bohn
- Klaus Rinnen
- Clark Fuhs

Supplemental Slides

PC Growth Forecast, 1997-2002



0.25-Micron Equipment and Materials

	0.35 Micron	0.25 Micron
Wafer Fab Equipment	**ASP**	
Stepper	I-line: $2.5M	KrF Excimer: $4.2M
Track	I-line: $1.1M	DUV: $2.0M
Plasma Etch	Low Density: $1.0M	High Density: $1.5M
CMP	-	$1.0M
Metrology	$0.3M	$0.65M
Materials		
Wafer	CZ: a	Epi: 1.5 x a
Photoresist	I-line: $450-500/gal (Novolak)	KrF:$1,500-1,800/gal (Chemical Amplified)

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High- and Low-Demand Scenarios for Epitaxial Wafers

	High-Demand Scenario			Low-Demand Scenario		
	16Mb	64Mb	256Mb	16Mb	64Mb	256Mb
IBM	Epitaxia	Epitaxia	Epitaxia	Epitaxia	Epitaxia	Epitaxia
Siemens	Epitaxia	CZ	Epitaxia	Epitaxia	CZ	H-Annealed
NEC	CZ	Epitaxia	Epitaxia	CZ	Epitaxia	Epitaxia
Hitachi	Epitaxia	Epitaxia	Epitaxia	CZ	Epitaxia	Epitaxia
Toshiba	H-Annealed	H-Annealed	Epitaxia	H-Annealed	H-Annealed	H-Annealed
Fujitsu	H-Annealed	Epitaxia	Epitaxia	H-Annealed	Epitaxia	Epitaxia
Samsung	CZ	Epitaxia	Epitaxia	CZ	CZ	CZ
Hyundai	CZ	Epitaxia	Epitaxia	CZ	CZ	CZ

CZ = Czochralski silicon wafer
H-Annealed = Hydrogen-annealed wafer

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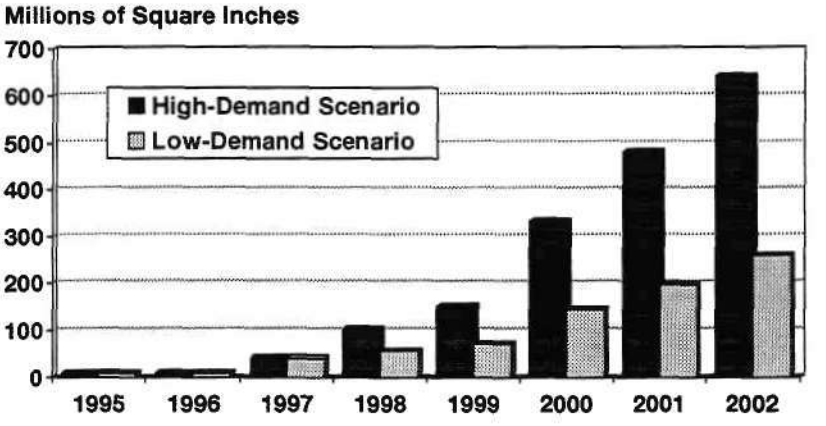
Fresh Outlook for Epitaxial Wafer Demand in DRAM Manufacturing



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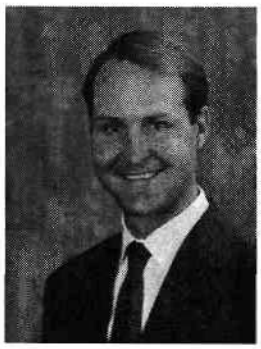
Notes

Foundry Manufacturing: Does Technology Investment Deliver ROA?



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Mr. Hines is a principal analyst and program manager for the Worldwide Semiconductor Contract Manufacturing Services program of the Semiconductors group at Dataquest. His responsibilities include market research and analysis of the semiconductor foundry industry, industry capacity forecast, and fabless IC companies. In addition, he provides research and analysis of the semiconductor factory automation market and manages the fab database for the Semiconductor Equipment, Manufacturing, and Materials Worldwide program.

Mr. Hines has over nine years of experience in the semiconductor equipment industry with Genus Inc. and Applied Materials where he has held a variety of strategic and product marketing positions. Before this, he worked in the Semiconductor Group of Texas Instruments.

Mr. Hines received a bachelor of science degree in mechanical engineering from the University of California at Santa Barbara.

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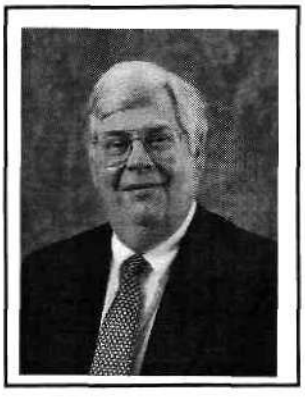
Moore's Law: Economic Engine or Technology Road Map?



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Principal Analyst
Semiconductor Equipment, Manufacturing, and Materials Worldwide
Semiconductors Group
Dataquest

Mr. Dornseif is a principal analyst for Dataquest's Semiconductor Equipment, Manufacturing, and Materials program in the Semiconductors group. Mr. Dornseif is responsible for research and analysis of semiconductor equipment and trends in IC manufacturing techniques, with specific responsibility for deposition, CMP, etch, and clean equipment markets.

Mr. Dornseif has more than 20 years of management and engineering accomplishment in the semiconductor industry with Intel Corporation, Genus Inc., and Watkins-Johnson Company's Semiconductor Equipment Group. His experience includes positions in product development, operations, marketing, strategic business development, and quality and reliability.

Mr. Dornseif holds a bachelor of science degree and a master of science degree in electrical engineering from the University of Illinois, and an M.B.A. from Santa Clara University. Before redirecting his education toward a business focus, he also attended Stanford University's graduate school of electrical engineering.

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1998 SEMICON/West Seminar—July 15

Moore's Law: Economic Engine or Technology Road Map?

Ron Dornself

Principal Analyst
Semiconductor Equipment, Manufacturing, and Materials Worldwide

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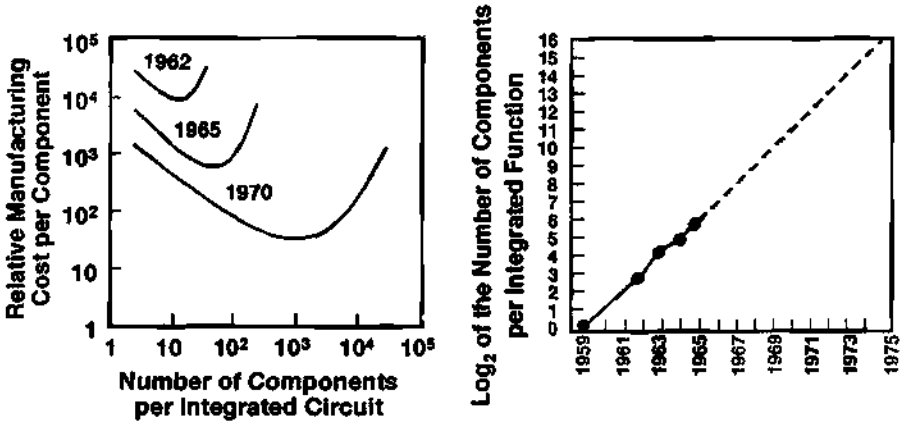
Outline

- Moore's Law
- Device limits
- Demand limits
- Conclusions

Original Moore's Law Figures Electronics, April 1995



Moore's Law

"The definition of "Moore's Law" has come to refer to almost anything related to the semiconductor industry that when plotted on semi-log paper approximates a straight line. I hesitate to review its origins and by doing so restrict its definition."

Gordon Moore, 1995

Moore's Law—Most Common Forms

Semiconductor cost per function declines geometrically with shrinking feature size

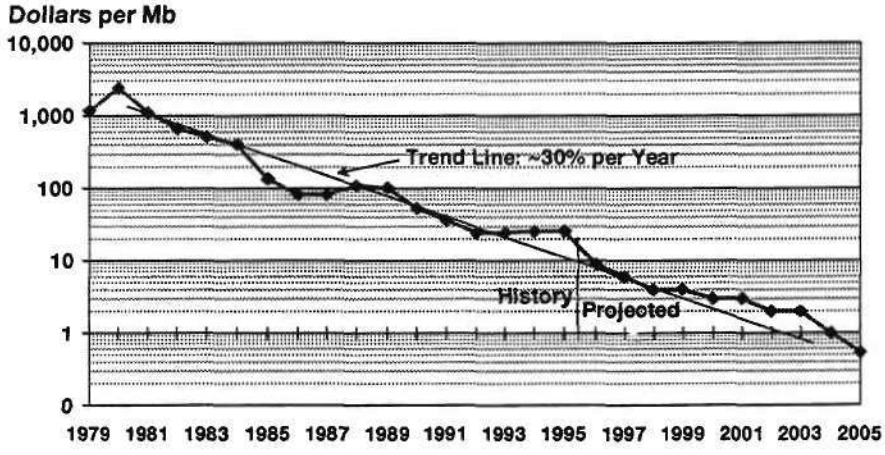
Corollaries

- Shrinking feature size vs. time
- Increasing transistors per cm^2 vs. time
- Increasing function (bits, MIPS, etc.) per chip vs. time
- Increasing die size vs. time

Moore's Law: IC Design Scaling — The Technical Engine

- Scaling factor, N>1
- Linear dimension: 1/N
- Device density: N^2
- Supply and logic voltage: 1/N
- Gate transit time (delay): 1/N
- Current: 1/N
- Capacitance: 1/N
- Switching energy: $1/N^2$
- Power dissipation: $1/N^2$
- Power density: constant
- Impedance: constant

Moore's Law: The Economic Engine



Source: Dataquest

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Elements of Moore's Law

Declining cost per function > 30%/year

- Decreasing cost (numerator)
  - Feature size shrinks: more die/wafer processed (wp)
  - Larger wafers: more die/wp
  - Higher yields: more net die/wp
  - Lower equipment, material, process cost/wp
- Increasing function (denominator)
  - Feature size shrinks: more T/cm^2
  - Larger die: more T/chip
  - Design, material, process improvements: better performance, T/cm^2

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National Technology Road Map for Semiconductors

- SIA sponsored, Sematech published
- Industry goal setting, planning tool
- Industry collaborative committees
- Window covers15 years and 7 technology generations
- 7 technology groups and 4 cross-cut groups: Establishes objectives/timing; identifies challenges, requirements, and potential solutions
- Over 200 page book, published every 3 years
- SIA Road Map: The caretaker of "Moore's Law"

Moore's Law: What Is It, Really?

- Insightful observation turned self-fulfilling prophecy?
- Technology road map?
- Economic engine of semiconductor industry?
- Set of *supply-side* enabling relationships?
- Semiconductor industry's strategic planning tool?
- All the above?

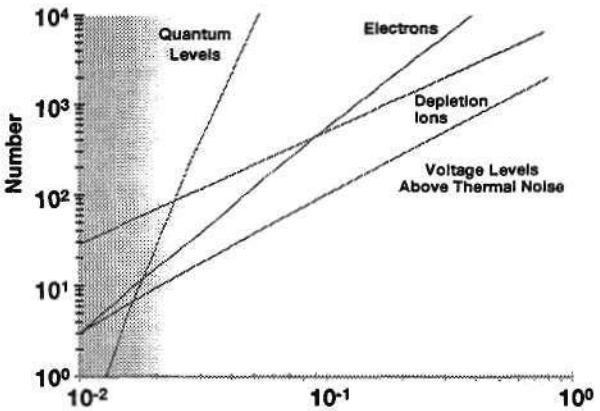
Moore's Law: What Is It, Really?

- *A set of supply-side enabling relationships*
- Assumes insatiable demand and price elasticity
- True in the past? Yes!
- True in the future? Has its boundary conditions.
- Limits:
  - Device limits
  - Demand limits
  - Manufacturing cost limits

Device Limits

Mother Nature Places Limits on Si Devices

- Silicon transistor technology
- 0.03 to 0.02 micron limit
- When?
- Manufacturing limits before?
- Replacement technology?
- Lead time for replacement?
- Applicability of current manufacturing technology?



Source: Carver Mead, ISS 1995

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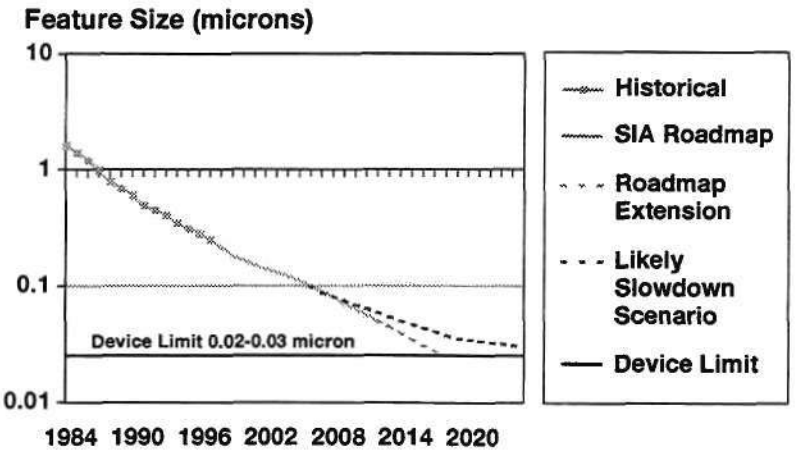
Device Limits: The Technical Engine Slows Down



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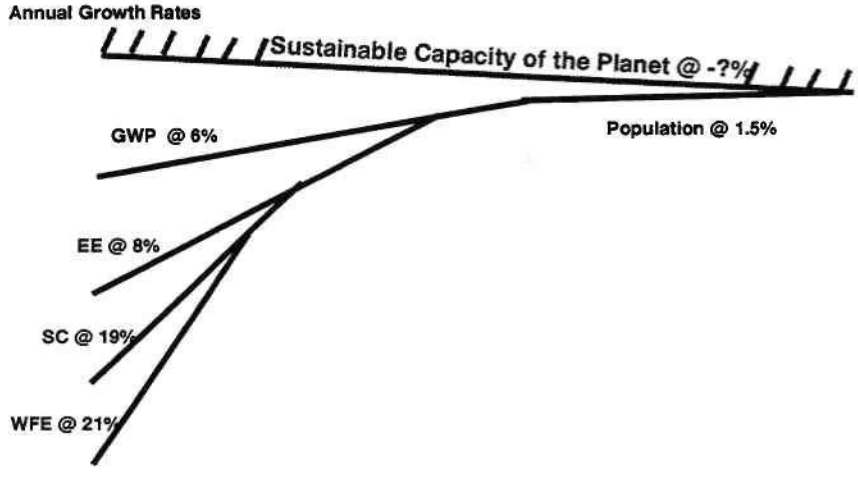
Demand Limits

Demand Saturation? The Ultimate Limit

- "Killer apps" needed to sustain
  - PC, telecommunications
  - Internet, speech
  - Next?
- Inversion of food chain growth rates
  - WFE_{gr} >IC_{gr} >EE_{gr} >GWP_{gr} >Population growth
- Rate of absorption varies with per-capita income
- Everyone is in it together
  - Affluence: GRP_{gr} >>> Population growth
  - Poverty: GRP_{gr} <<< Population growth

There Are Limits to High Growth Rates Question Is Timing?



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Semiconductor Food Chain There Are Limits to High Growth Rate

	10-Year CAGR	1995 Supplier Content	Estimated Content Limit	Inflexion "Point" Year
Sustainable Capacity of the Planet	- ?%		?	The ultimate question
Population Growth	1.5% (1994)	?	?	?
Gross World Product	6%	?	?	?
Electronic Equipment	8%	2.7%	10-12%	2070-2080
Semiconductor	19%	19.0%	30-50%	2004-2006
Wafer Fab Equipment	21%	12.5%	13-15%	2004-2006

Source: Dataquest

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Industry Dynamics Shifting: Supply-Line Push to Buy-Line Pull

- PCs are dominant driver of semiconductor market
- PC market segmenting
  - High end (>$2000): performance/technology driven
  - Low end A (<$1500): limited function/econ. driven
  - Low end B ($<$1000): very limited fn. /econ. driven
- Supply line in chaos
  - Capacity glut
  - Accelerating 64M looking for profit
  - Technology glut visible
  - 300mm push-out
  - Asian financial situation

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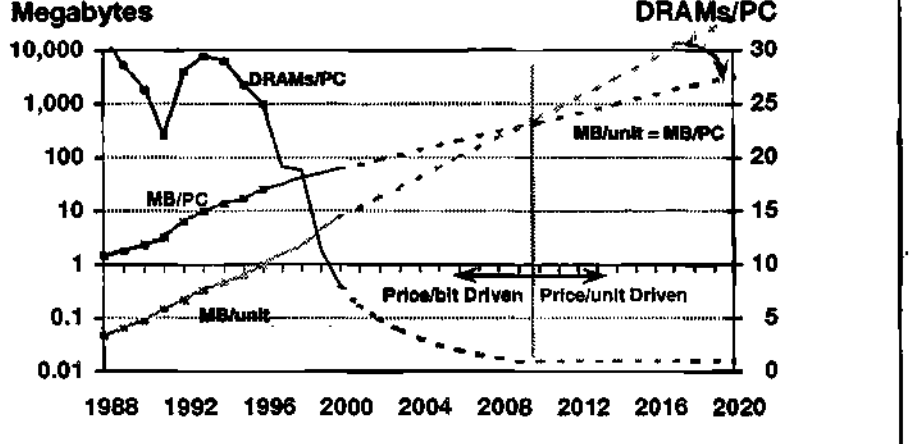
PC Demand for DRAM: Trending to 1 Unit/PC



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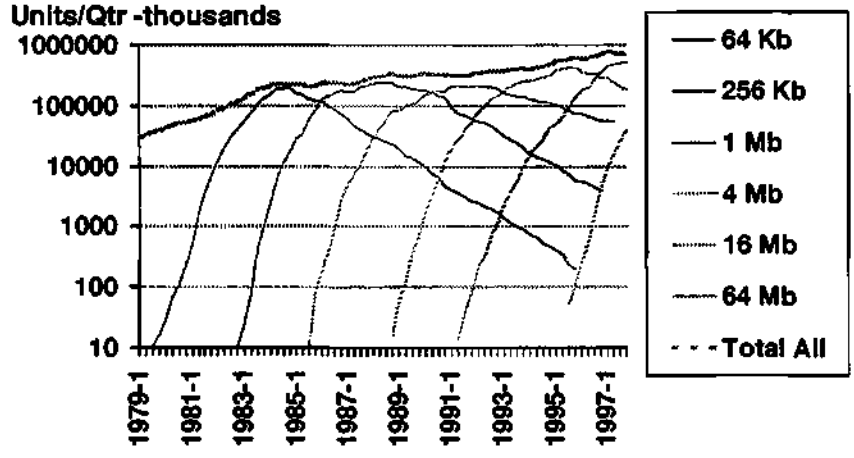
DRAM Historical Unit Shipments
(data smoothed)



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Implications of 1 DRAM Chip per PC

- Chip density growth slows to PC density growth
- Bus width and granularity will force 2-3 chip min.
  - Buyers decide configuration
  - OEM main memory: 1 high-density chip for appl.
  - Add-on memory: 1-2 lower-density chips as req'd
  - Buying based on price/bit with price/unit max
- Delayed ramp rate and longer DRAM life cycles
  - High-end PC drives introduction timing of DRAMs
  - Low-end PC drives high volume timing
  - More DRAM generations in production

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Implications of 1 DRAM Chip per PC

- Technology & DRAM generations forever decoupled
  - Less frequent DRAM generations, or
  - 1/2 density DRAM generations
  - Mfg. focus shifts from more bits/die to smaller die for fixed bits and more die/wafer
  - Smaller die postpones larger wafers
  - More units to satisfy total WW bit demand
  - More fabs, equipment, wafers? Maybe.
- Silicon efficiency *rate* slows
- Technology glut produced (capability>demand)

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Conclusions: Rules of the Game Are Changing

- Industry shifting to demand-paced environment
  - IC business, mfg. & buying models changing
  - Cost/function rate will slow, impacting demand
- Moore's Law/SIA Road Map:
  - Remember, it's supply-line capability focused
  - Producing a technology glut
  - Must bring capability in balance with demand
- Equipment
  - IC & feature generations forever decoupled
  - Slower function growth stresses mfg. economics
  - Cycles will worsen
  - Equip. COO: THE emerging competitive advantage

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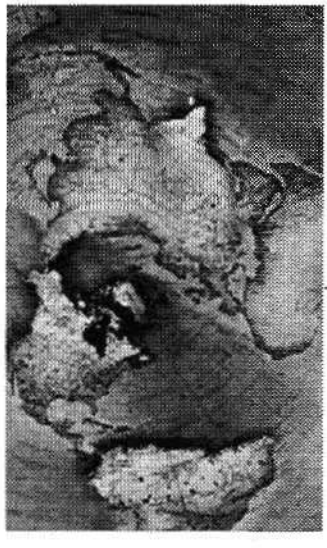

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Semiconductor Road Map

Minimum Feature Size (Micron)	0.25	0.18	0.15	0.13	0.10	0.07
Year of First Shipment	1997	1999	2001	2003	2006	2009
Maximum Wafer Size (mm)	200	300	300	300	300	450
Density (µP)—Transistors/cm² (Millions)	3.7	6.2	10.0	18.0	39.0	84.0
Chip Size (µP) (mm²)	300	340	385	430	520	620
On-Chip, Across Chip, Clock Frequency (MHz) (High-Performance Logic)	750	1,200	1,400	1,600	2,000	2,500
Maximum Power, High Performance with Sink (W)	70	90	110	130	160	170
Minimum Power Supply Voltage (Volts)	1.8-2.5	1.5-1.8	1.2-1.5	1.2-1.5	0.9-1.2	0.6-0.9
Maximum Number of Wiring Lines	6	6-7	7	7	7-8	8-9
Maximum Interconnect Length (Meters/Chip)	820	1,480	2,160	2,840	5,140	10,000
Via Aspect Ratio (*Additive for Dual Damascene)	2.2	2.2*	2.4*	2.5*	2.7*	2.9*
Metal Height/Width Ratio (*Additive for DD)	1.8	1.8*	2.0*	2.1*	2.4*	2.7*
IMD Effective Dielectric Constant (k)	3.0-4.1	2.5-3.0	2.0-2.5	1.5-2.0	1.5-2.0	<1.5

Source: National Technology Road Map for Semiconductors, 1997

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Semiconductor Food Chain
Size, Growth, and Supplier Contribution

	1995 Estimates	10 year CAGR (%) (Differing periods)	Supplier Content (%)
Gross World Product	$28,954 B	6 %	
Electronic Equipment	$791 B	8 %	2.7 %
Semiconductor	$151 B	19 %	19.0 %
Wafer Fab Equipment	$19 B	21 %	12.5 %

Source: Dataquest

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Notes