## **Focus Conference**

# The Productivity Age: Design Alternatives Become Solutions

Sponsored by the CAD/CAM Industry Service

December 9 and 10, 1985 Hyatt Palo Alto Palo Alto, California



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## 1985 CAD/CAM INDUSTRY FOCUS CONFERENCE

#### December 9 and 10, 1985 The Hyatt Palo Alto Palo Alto, California

#### MONDAY, December 9 7:30 a.m. to 8:30 a.m. 8:30 a.m. Jim Newcomb Vice President and Group Director Industrial Automation Group Dataquest Incorporated 8:45 a.m. Beth Tucker Senior Industry Analyst **CAD/CAM Industry Service** Dataquest Incorporated 9:30 a.m. Tony Spadarella Research Analyst **CAD/CAM Industry Service** Dataquest Incorporated 10:15 a.m. 10:45 a.m. Kelly Leininger Research Assistant CAD/CAM Industry Service Dataquest Incorporated 11:30 a.m. Sheridan Tateuno Industry Analyst Japanese Semiconductor Industry Service Dataquest Incorporated 12:15 p.m. 1:30 p.m. Terry Zimmerman Vice President, Marketing FutureNet Corporation 2:15 p.m. Peter Whyte Vice President, Strategic Planning E-CAD, Inc. 3:00 p.m. Coffee Break ...... Redwood Foyer 3:15 p.m. John Newkirk Chief Executive Officer Silicon Solutions Corporation 4:00 p.m. Jeff Hotchkiss General Manager Teradyne, Inc. 4:45 p.m. Steven Coit Partner Merrill, Pickard, Anderson, & Eyre 5:30 p.m. to 7:00 p.m.

## TUESDAY, December 10

8:30 a.m.	The PCB Connection
9:15 a.m.	Developing an Open Network for IC Design
10:00 a.m.	Coffee Break
10:30 a.m.	User Interfaces Impact Productivity
11:15 a.m.	Where are MPUs Going?
12:00 Noon	Lunch
1:30 p.m.	Unified Design—is it for Real?
2:15 p.m.	ASIC, USIC, or CSIC?
3:00 p.m.	Coffee Break
3:15 p.m.	The Impact of Silicon Compilers on Productivity
4:00 p.m.	The Global Productivity Imperative
4:45 p.m.	Conference Wrap-up Redwood i Beth Tucker Senior Industry Analyst CAD/CAM Industry Service Dataquest Incorporated



## CAD/CAM INDUSTRY FOCUS CONFERENCE EVALUATION QUESTIONNAIRE

Palo Alto, California December 9-10, 1985

Thank you for attending our CAD/CAM Industry Focus Conference. Would you please assist us in planning our next conference by completing and returning this questionnaire?

1. Please rate each presentation on a scale of 1 to 10 (where 10 is highest in terms of your approval):

		CONTENT	DELIVERY	COMMENTS	
		(1 to 10)	(1 to 10)	(Use reverse side if necessary)	
	Tucker, Measuring the Intengibles				
	Spadarella, Automatic IC Generation			<u> </u>	•
	Leininger, Design Center Survey				•
	Tetsuno, Japanese Technology: The Future				
	Zimmerman, PCs: How Much Can They Really Do	?			
	Whyte, Software: The Real IC Designer				,
	Newfdrk, Fitting in Application Accelerators				
	Hotchkiss, Linking Design and Test	12	10	TIZEMENDOUS CAPTELTS	PERIVERS
	Colt, The Golden Egg		<u>.</u>		•
	Feltman, The PCB Connection				
	Bourbon, Developing Open Network for IC Design				,
	Balley, User Interfaces Impact Productivity				
	Thomsen, Where are MPUs Going?				
	Solomon, Unified Design—Is it for Reat?				
	Feirbairn, ASIC, USIC, or CSIC?				
	Kuenster, Silicon Compilers/Productivity				
	Finegold, Global Productivity Imperative				1
2.	Overall meeting rating (1 to 10):				
3.	How would you rate the conference facilities (1	to 10)?			
	Location Guest Rooms Meat	s	Meeting R	ooms	
4.	Topics that would be of interest to you for future	9 CAD/CAI	M Industry	Focus Conferences:	
		<u> </u>			

(OVBI)

					<u> </u>	
<u></u>			Industry Con-	- Castanasa i		
e. Your pr	imary interest	in the CAD/CAM	industry Focu	8 Comerence II	3 as a:	

## **Dataquest**



#### CAD/CAM INDUSTRY SERVICE FOCUS CONFERENCE December 9 through 10, 1985 Palo Alto, California

#### List of Attendees

AWI Surface Mount Technology Ed Bingle, Design Supervisor

Advanced Micro Devices, Inc.

J. Phillip Downing, Vice President,
Corporate Technology

Alpha Partners Brian Grossi, General Partner

Apollo Computer, Inc. Raymond McCann, Market Manager, ECAD

Applied Micro Circuits Corporation Bernie Rosenthal, CAD Marketing Manager

Array Technology

Bill O'Neil, Vice President,
Engineering

Arthur Young & Company Angelo Danna, Partner Mark Nexsen, Principal

Bank of America

Don Cvietusa, Vice President
Alan Jepsen, Corporate Banking
Officer
Sally Otton, Assistant Vice President

Bank of Boston William Parker, Banking Officer

Bitstream, Inc. Ann Roe-Hafer, Director, Marketing

Burr, Egan, Deleage & Company Thomas Winter, Partner

CADAM, Inc. Rhonda Lindsey, CAD/CAM Market

Industry Analyst

CAD/CAM Specialists, Inc. Deniel DeWitt, Psychologist

Organizational Development

Daniel Garms, Executive Vice President

Michael McDonald, President

Cadcor Company David Jewell, Vice President,

Operations

Cadnetix Corporation Buck Feltman, Vice President, Marketing

California Devices, Inc. James Tobias, Vice President

Design Technology

Cambridge Electronic Industries David Cutts, Strategic Planner

Cericor, Inc. David Bailey, President & Chief

Executive Officer

Cirrus Logic, Inc. Suhas Patil, Vice President,

Research & Development

Citicorp Industrial Credit

Mano Appapillai, Vice President

Daisy Systems Corporation

Aryeh Finegold, President

Data General Corporation

Boli Medappa, Competitive Consultant Uday Watwe, Product Manager

Dataquest Incorporated

Irene Barth, Conference Assistant Greg Chagaris, Industrial Marketing Manager Ralph Dickman, Industrial Marketing Manager Kathy Hurley, Research Analyst John Jackson, National Sales Manager Debra Jacob, Conference Assistant Kelly Leininger, Research Assistant Eileen Barth-Lynch, Research Analyst James Newcomb, Vice President & Group Director, CAD/CAM Industry Service Jewel Peyton, Director, Corporate Communications Don Roberts, Manager, Training & Development Tony Spadarella, Research Analyst Lynn Stern, Conference Coordinator Sheridan Tatsuno, Industry Analyst Japanese Semiconductor Industry Mel Thomsen, Associate Director, Semiconductor Industry Service Beth Tucker, Senior Industry Analyst Paul van Dillen, Industrial

Marketing Manager

Digital Equipment Corporation Fanjeev Aggarwal, CAD Strategic Marketing Specialist Bill Goerke, Senior Vice President, E-CAD, Inc. Marketing & Sales Robert Lorentzen, Product Manager Peter Whyte, Vice President, Strategic Planning Edge Computer Corporation Douglas Crawford, Western Regional Manager Engineering Systems Products William Fabel, Program Manager Exar Corporation Yukio Nishikawa, Director, Engineering Ferranti Interdesign Inc. John Doyle, CAD Manager Ford Aerospace & Communications Clayton Showen, Manager Equipment & Corporation Engineering FutureNet Corporation Terry Zimmerman, Vice President, Marketing Development GE Venture Capital Eric Young, Vice President

Russel Craig, Vice President,

Strategic Planning

GenRad, Inc.

General Electric Company

Claire Heiss, Manager, Manufacturing

Gould AMI Semiconductors

Bruce Bourbon, Vice President, Marketing

Grace Ventures Corporation

Susan Woods, Assistant Vice President

Grove Hill Industries, Inc.

Barry Soloway, President & Chief Executive Officer

Hewlett-Packard Company

Gene Barduson, Manager, Marketing Division Curt Dowdy, Product Manager Brad Miller, Marketing Manager John Moss, Marketing Manager Robert Santos, Product Marketing Manager Nick Shain, Application Engineer Jim Stroh, Product Marketing Manager Mark Tolliver, Marketing Manager, Design Systems Group

Hillman Ventures, Inc.

Howard Geiger, Jr., Vice President

IBM Corporatiion

Frank Magistro Christina Schott, Marketing Manager, EDA

ICD Austria

Hubert Gammer, Director Monika Pacher, Director IKOS Systems, Inc.

William Loesch, President

Ing. C. Olivetti & C., S.p.A.

Ugo De Riu, Distributed Data Processing Division Manager Carlo Ronca, Distributed Data Processing Director

Institutional Venture Partners

Mary Jane Elmore, General Partner

Intergraph Corporation

Dennis Addidgo, District Sales Manager

Integrated Logic Systems, Inc.

Jeffrey Jacobsen, Vice President, Marketing & Sales

Intel Corporation

Doug Finke, Marketing Engineer

Intersil, Inc.

Charles Shaw, Director, Computer Aided Design

InterWest Partners

Flip Gianos, General Partner

J.H. Whitney & Company

William Harding, Associate John Larson, Partner

Los Alamos National Laboratories

Bob Morrison, Staff Member

Mayfield Fund	A. Grant Heidrich, General Partner Michael Levinthal, General Partner F. Gibson Myers, General Partner William Unger, Partner
McDonnell Douglas, ISG	Mike Landers, Manager, Marketing Research William White, Product Marketing
Mead Imaging	Charles Sharp, Director Printer Product Planning
Mentor Graphics Corporation	Dick Kaiser, Product Manager
Merrill, Pickard, Anderson & Eyre	Stephen Coit, General Partner
Mini Micro Magazine	Arlette Gaulene
Monolithic Memories, Inc.	H.T. Chua. Vice President Carl Hudson, Engineering Support Manager
NEC Corporation	Takayuki Yanagawa, General Manager
Oak Investment Partners	Jeffrey West, General Partner
Priam Corporation	Albert Hartman, Manager, MCAD/CAE

R&D Funding Corporation Irv Weiman, Vice President

Racal-Redac, Inc.	Jeil Allison, CAL marketing Group
Ridge Computers	Mike Harrigan, Product Marketing
Rockwell International Corporation	William Pearce, Director, CAD Development, Advanced Engineering
SDA Systems, Inc.	James Solomon, President
SGS Semiconductor Corporation	Giancarlo Ronzi, Director, Design
Scientific Calculations, Inc.	Michael Davin, Director, International & North American Sales
Seattle Silicon Technology, Inc.	Gordon Kuenster, President Diane Kuenster
Seeq Technology, Inc.	Larry Bullard, Manager CAD & Tooling
Siemens Data Systems	Wolfgang Gnettner, Manager, Product Planning
Sierra Semiconductor Corporation	Lawrence Goldstein, Director Design Automation
Silicon Design Labs, Inc.	James Hammock, Chief Operating Officer

Racal-Redac, Inc.

Jeff Allison, CAE Marketing Group

David Reiser, Director, Marketing

John Newkirk, Chief Executive Officer Silicon Solutions Corporation Frank Lynch, Director, Marketing Silvar-Lisco Tom Blank, Director, CAD Stanford University Roberta Gray, Market Segment Sun Microsystems, Inc. Manager Doug Bering, Development Engineering Tandem Computers, Inc. Manager Tektronix, CAE Systems Division Robert Harrison, Product Marketing Manager Kelly Rupp, Product Marketing Manager Steve Sapiro, Chief Scientist Telesis Systems Corporation Robert Fulks, Consultant Douglas Hajjar, President & Chief Executive Officer Teradyne, Inc. Jeff Hotchkiss, General Manager

Robert Geissberger, President

Mike Thomas, Partner

The Photo-Tech Company

Thomas Group, Inc.

Union Bank

Dirk Geiger, Loan Officer

Valley Data Sciences

Keith Barnes, Director, Marketing Robert Soto, President

VLSI Technology, Inc.

Douglas Fairbairn, Vice President

Weitek Corporation

Scott Lewis, Director, Strategic Development John Rizzo, Director, Marketing

Xilinix, Inc.

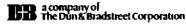
David Lautzenheiser, Director Technical Marketing Kathie Priebe, Director, Software Development

Zycad Corporation

Dave Allenbaugh, Product Marketing Manager Dick Ebert, Director, Marketing John Fahlberg, Senior Vice President, Operations



## **Dataquest**



#### CAD/CAM INDUSTRY SERVICE FOCUS CONFERENCE December 9 through 10, 1985 Palo Alto, California

#### List of Attendees

Dennis Addidgo Intergraph Corporation

Fanjeev Aggarwal Digital Equipment Corporation

Dave Allenbaugh Zycad Corporation

Jeff Allison Racal-Redac, Inc.

Mano Appapillai Citicorp Industrial Credit

David Bailey Cericor, Inc.

Gene Barduson Hewlett-Packard Company

Keith Barnes Valley Data Sciences

Irene Barth Dataquest Incorporated

Doug Bering Tandem Computers, Inc.

Ed Bingle AWI Surface Mount Technology

Tom Blank Stanford University

Bruce Bourbon Gould AMI Semiconductors

Larry Bullard Seeq Technology, Inc.

Greg Chagaris Dataquest Incorporated

H.T. Chua Monolithic Memories, Inc.

Stephen Coit Merrill, Pickard, Anderson & Eyre

Russel Craig GenRad, Inc.

Douglas Crawford Edge Computer Corporation

David Cutts Cambridge Electronic Industries

Don Cvietusa Bank of America

	Ange	l٥	Danna
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Michael Davin

Ugo De Riu

Daniel DeWitt

Ralph Dickman

Curt Dowdy

J. Phillip Downing

John Doyle

Dick Ebert

Mary Jane Elmore

William Fabel

John Fahlberg

Douglas Fairbairn

Buck Feltman

Arych Finegold

Doug Finke

Robert Fulks

Hubert Gammer

Daniel Garms

Arlette Gaulene

Dirk Geiger

Howard Geiger, Jr.

Robert Geissberger

Flip Gianos

Wolfgang Gnettner

Arthur Young & Company

Scientific Calculations, Inc.

Ing. C. Olivetti & C., S.p.A.

CAD/CAM Specialists, Inc.

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Hewlett-Packard Company

Advanced Micro Devices, Inc.

Ferranti interdesign Inc.

Zycad Corporation

Institutional Venture Partners

Engineering Systems Products

Zycad Corporation

VLSI Technology, Inc.

Cadnetix Corporation

Daisy Systems Corporation

Intel Corporation

Telesis Systems Corporation

ICD Austria

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Union Bank

Hillman Ventures, Inc.

The Photo-Tech Company

InterWest Partners

Siemens Data Systems

Bill Goerke

Lawrence Goldstein

Roberta Gray

Brian Grossi

Ann Roe-Hafer

Douglas Hajjar

James Hammock

William Harding

Mike Harrigan

Robert Harrison

Albert Hartman

A. Grant Heidrich

Claire Heiss

Jeff Hotchkiss

Carl Hudson

Kathy Hurley

John Jackson

Debra Jacob

Jeffréy Jacobsen

Alan Jepsen

David Jewell

Dick Kaiser

Gordon Kuenster Diane Kuenster

Mike Landers

John Larson

E-CAD, Inc.

Sierra Semiconductor Corporation

Sun Microsystems, Inc.

Alpha Partners

Bitstream, Inc.

Telesis Systems Corporation

Silicon Design Labs, Inc.

J.H. Whitney & Company

Ridge Computers

Tektronix, CAE Systems Division

Priam Corporation

Mayfield Fund

General Electric Company

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Michael J. Levinthal

Scott Lewis

Rhonda Lindsey

William Loesch

Robert Lorentzen

Eileen Barth-Lynch

Frank Lynch

Frank Magistro

Raymond McCann

Michael McDonald

Boli Medappa

Brad Miller

Bob Morrison

John Moss

F. Gibson Myers

James Newcomb

John Newkirk

Mark Nexsen

Yukio Nishikawa

Bill O'Neil

Sally Otton

Monika Pacher

William Parker

Xilinix, Inc.

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Mayfield Fund

Weitek Corporation

CADAM, Inc.

IKOS Systems, Inc.

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Nick Shain Hewlett-Packard Company

Charles Sharp Mead Imaging
Charles Shaw Intersil, Inc.

Christina Schott

Clayton Showen Ford Aerospace & Communications
Corporation

IBM Corporation

James Solomon SDA Systems, Inc.

Barry Soloway Grove Hill Industries, Inc.

Robert Soto Valley Data Sciences

Tony Spadarella Dataquest Incorporated

Lynn Stern Dataquest Incorporated

Jim Stroh Hewlett-Packard Company

Sheridan Tatsuno Dataquest Incorporated

Mike Thomas

Mel Thomsen

James Tobias

Mark Tolliver

Beth Tucker

William Unger

Paul van Dillen

Uday Watwe

Irv Weiman

Jeffrey West

William White

Peter Whyte

Thomas Winter

Susan Woods

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Oak Investment Partners

McDonnell Douglas, ISG

E-CAD, Inc.

Burr, Egan, Deleage & Company

Grace Ventures Corporation

NEC Corporation

GE Venture Capital

FutureNet Corporation





WELCOME AND CONFERENCE INTRODUCTION

James R. Newcomb
Vice President and Group Director
Dataquest Incorporated

Mr. Newcomb is a Vice President of Dataquest and Group Director of the Industrial Automation Group, which encompasses the CAD/CAM Industry Service and the Robotics Industry Service. He is responsible for the group's strategic direction, overall planning, operations management, and the establishment of business platforms. Previously, he was employed at Auto-trol Technology Corporation, where he held various positions within the corporate marketing organization. Prior to that, he was employed in the Reprographic Manufacturing Group of Xerox Corporation, in positions involving strategic planning, systems integration, advanced manufacturing engineering, and program planning. Mr. Newcomb's professional experience has provided him with an in-depth knowledge of design and manufacturing automation technologies and markets involving CAD/CAM/CAE, EDA, robotics, artificial intelligence, and automation systems design implementation. Mr. Newcomb received a B.S.M.E. degree from Rochester Institute of Technology. He is a member of the Society of Manufacturing Engineers, Computer Automated Systems Association, Machine Vision, Robotics Industry Association, National Computer Graphics Association, and IEEE.

Dataquest Incorporated
DESIGN AUTOMATION FOCUS CONFERENCE
December 9 and 10, 1985
Palo Alto, California

## **Dataquest**

a company of The Dun & Bradstreet Corporation

**DUN & BRADSTREET** 

A.C. NIELSEN COMPANY

DATAQUEST INCORPORATED

## MEMBERS OF DUN & BRADSTREET FAMILY OF INFORMATION COMPANIES

- DUN & BRADSTREET
  - LARGEST BUSINESS INFORMATION SERVICE COMPANY IN THE WORLD
  - 48,000 EMPLOYEES IN 25 COUNTRIES
  - \$2.2 BILLION IN YEARLY REVENUES

# A.C. NIELSEN COMPANY DATAQUEST INCORPORATED

- DATAQUEST INCORPORATED
  - SUBSIDIARY OF A.C. NIELSEN COMPANY SINCE 1978
  - HIGH-TECHNOLOGY RESEARCH ARM OF A.C. NIELSEN COMPANY
- A.C. NIELSEN COMPANY
  - WORLD'S LARGEST MARKET RESEARCH ORGANIZATION
  - \$750 MILLION COMPANY--FOUNDED 1923

## CAD/CAM INDUSTRY SERVICE -- 1985

## THE INFORMATION PLATFORM

MARKET	TURN- KEY	COMPUTERS			PHI RMI -	.	PERI- PHERAL	SOFTWARE/ SERVICES
APPLI- CATION	MECHA	NICAL AEC		РС	8	IC	EDA	MAPPING
REGION	NOF AME	···· I FURC		PE	FAR EAST		EAST	REST OF WORLD
PRODUCT TYPE	PERSONAL STA			ANDALONE HOST			-DEPENDENT	
PRICE		5 THAN 30K		\$30K-\$90K				MORE THAN \$90K

SOURCE DATAQUEST

Dataquest

BB a company of The Dun & Bradstreet Corporation



MEASURING THE INTANGIBLES

Beth W. Tucker Senior Industry Analyst Dataquest Incorporated

Ms. Tucker is a Senior Industry Analyst for Dataquest's CAD/CAM Industry Service. She is responsible for the management of research activities involving all electronic CAD/CAM applications, including integrated circuits, printed circuit boards, and electronic design automation. In addition, she is responsible for managing the service's industry data base, survey activities, and consulting projects. Prior to joining Tucker was Manager of Market Dataquest, Ms. Planning in Microelectronics Division of Calma Company, a subsidiary of General Electric. In that capacity, she was responsibile for identifying market opportunities and strategies for the company's electronic CAD product She also contributed to the development of marketing programs at the corporate level. Earlier, she worked for Monroe Systems, where she was responsible for market research and development of small business computer products. Ms. Tucker received an A.A. degree in Computer Technology from Morris County College in New Jersey, and is doing course work at San Jose State University.

Dataquest Incorporated
DESIGN AUTOMATION FOCUS CONFERENCE
December 9 and 10, 1985
Palo Alto, California

## **AGENDA**

- REVISED FORECAST
- FOCUS RESEARCH GROUP HIGHLIGHTS

## FORECAST CHANGE

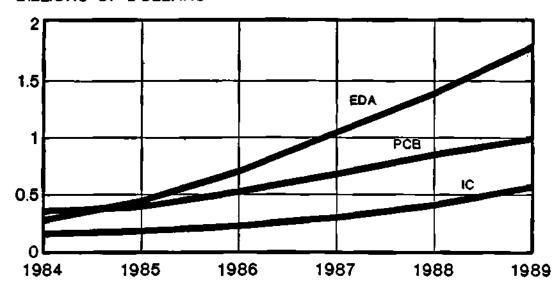
- 1985 ECONOMICS
- HOST-DEPENDENT IN DECLINE
- PERSONAL COMPUTER INCREASE
- FALLING ASPs

- SEMICONDUCTOR INDUSTRY

# DECLINING 30% THIS Y THE

# ESTIMATED ELECTRONIC CAD/CAM MARKET BY APPLICATION

## **BILLIONS OF DOLLARS**



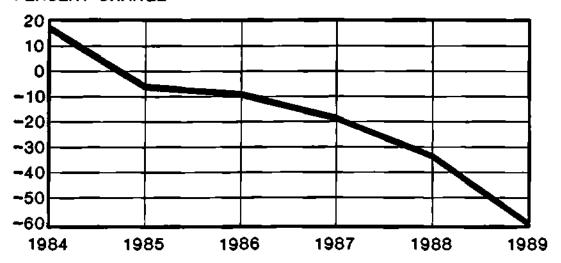
Source: DATAQUEST

## ESTIMATED ECAD MARKET (Millions of Dollars)

	1984	<u> 1985</u>	<u>1986</u>	1987	1988	<u>1989</u>	CAGR
EDA	\$ 276	\$ 442	\$ 701	\$1,042	\$1,387	\$1,798	31%
IC	157	181	224	298	408	571	46%
PCB	355	392	525	679	850	991	30%
Total	\$ <del>788</del>	\$1,015	\$1,450	\$2,019	\$2,645	\$3,360	34%

# ELECTRONIC CAD/CAM HOST-DEPENDENT PRODUCT TYPE

## PERCENT CHANGE

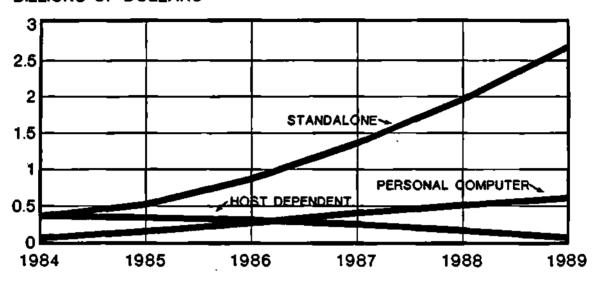


## HOST-DEPENDENT PORECAST (Revenue Percent Change)

	1984	1985	<u>1986</u>	<u>1987</u>	1988	1989
Percent Change	17	-,6	-9	-19	-34	-60

## ESTIMATED ELECTRONIC CAD/CAM MARKET BY PRODUCT TYPE

## **BILLIONS OF DOLLARS**



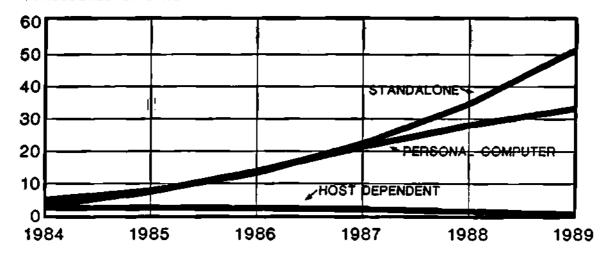
Source: DATAQUEST

#### ESTIMATED ECAD MARKET BY PRODUCT TYPE (Millions of Dollars)

	<u>1984</u>	1985	<u>1986</u>	<u>1987</u>	1988	<u>1989</u>	CAGR
Standalone	\$ 361	\$ 521	\$ 873	\$1,362	\$1,963	\$2,686	498
Host-Dependent	364	342	310	252	168	67	-29%
Personal Computer	63	152	<u>2</u> 67	405	514	607	57%
Total	\$ 788	\$1.015	\$1.450	\$2.019	\$2.645	\$3.360	34 %

## ESTIMATED ELECTRONIC CAD/CAM MARKET BY PRODUCT TYPE

## WORKSTATION SHIPMENTS (Thousands of Units)



Source: DATAQUEST

#### ESTIMATED ECAD MARKET BY PRODUCT TYPE (Workstation Shipments)

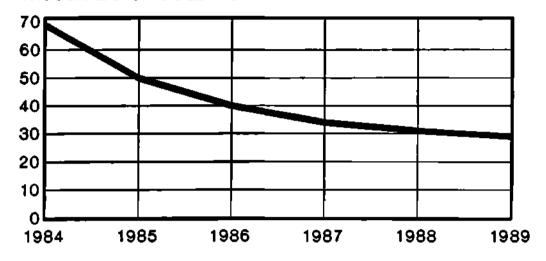
	<u>1984</u>	<u>1985</u>	<u>1986</u>	1987	1988	<u>1989</u>	CAGR
Standalone	5,073	7,813		22,251		51,443	59%
Host-Dependent	2,553	2,517	· ·	2,086	, –	626	~25%
Personal Computer					<u>28,112</u>	<u>33,282</u>	60 <u>%</u>
Total	10,805	17,868	29,562	45,737	64,171	85,341	51%

#### "PEOPLE BUY TRUCKERS \$80,000 TRUCKS, YET THEY WON'T SPEND AS MUCH MONEY ON DESIGN AUTOMATION."

Source: Focus Group Participant

#### ELECTRONIC CAD/CAM ESTIMATED AVERAGE SYSTEMS SELLING PRICE

#### THOUSANDS OF DOLLARS



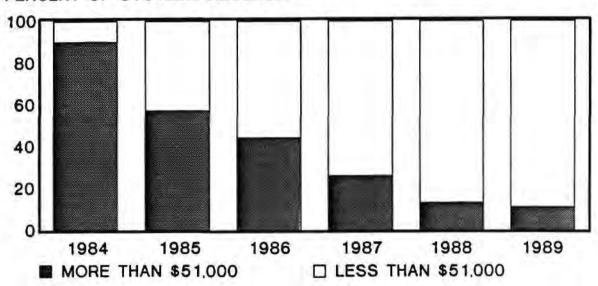
Source: DATAQUEST

#### ESTIMATED ECAD MARKET AVERAGE SELLING PRICE (Thousand of Dollars)

	<u>1984</u>	<u>1985</u>	<u>1986</u>	1987	1988	<u>1989</u>	CAGR
ASP	\$ 69	<b>£</b> 50	\$ 40	<b>4</b> 34	<b>e</b> 31	# 20	_169

#### ESTIMATED ELECTRONIC CAD/CAM MARKET BY PRICE-PER-SEAT SEGMENTS

#### PERCENT OF SYSTEMS REVENUE



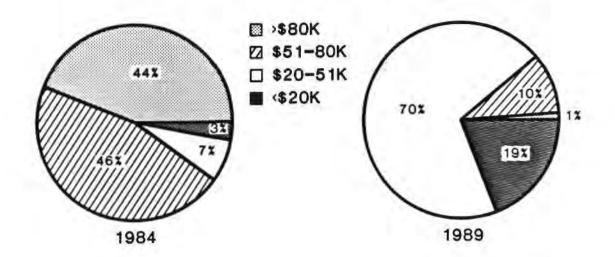
Source: DATAQUEST

#### ESTIMATED ECAD MARKET BY AVERAGE PRICE PER SEAT (Percent of Revenue)

199	34 1	1985 1	986 1	987 1	988 1989	1
Less Than \$51,000	LO	43	56	74	87 89	
Greater Than \$51,000	90	57	44	26	13 11	

#### ESTIMATED ELECTRONIC CAD/CAM MARKET BY PRICE-PER-SEAT SEGMENTS

#### PERCENT OF SYSTEMS REVENUE



Source: DATAQUEST

# ESTIMATED ECAD MARKET BY AVERAGE PRICE PER SEAT SEGMENT (Percent of Revenue)

Price Per Seat	1984	1985	1986	1987	1988	1989
Less Than \$20,000	3	15	21	23	21	19
\$20,000-51,000	7	28	35	51	66	70
\$51,000-80,000	46	39	32	19	10	10
Greater Than \$80,000	44	18	12	7	3	1

#### FOCUS GROUP HIGHLIGHTS

- VENDOR/CUSTOMER RELATIONSHIP
- CHANGING GROUND RULES
- CREATIVITY
- SERVICE AND SUPPORT
- GOALS OF PRODUCTIVE SYSTEMS

# "BECAUSE THE INDIVIDUAL VENDORS THAT ARE VERY STRONG IN ONE AREA MIGHT BE WEAK IN OTHERS, YOU CAN'T AFFORD TO GO WITH THEM ACROSS THE BOARD."

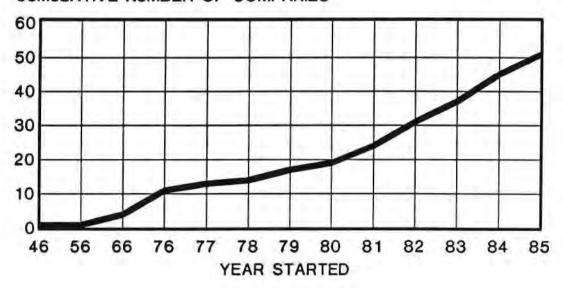
Source: Focus Group Participant

#### TUCKER'S CAD/CAM LAW

- THE CAD VENDOR/CUSTOMER
  RELATIONSHIP IS NOT A MARRIAGE,
  IT IS AN AFFAIR
  - SOMETHING FLASHIER, FASTER, BETTER, AND CHEAPER WILL ALWAYS COME ALONG

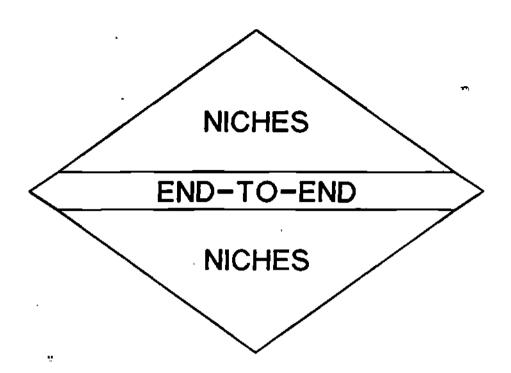
#### **ELECTRONIC CAD/CAM VENDORS**





Source: DATAQUEST

- 51 VENDORS NOW SELLING
ELECTRONIC APPLICATIONS
IN CADICAM



# "IF THE BIG GUYS WERE LAGGING, THEN THERE WOULD BE OPPORTUNITY, AND THE LITTLE GUYS WOULD SPRING UP AGAIN, AND THEY'D SATISFY THE DEMAND."

Source: Focus Group Participant

### **PRESENT**

**BIG GUYS** 

'AVIS'

LITTLE GUYS

### **CHANGING GROUND RULES**

- DATA BASE
- INTEGRATION
- SUPPORT
- FUNCTIONALITY
- PERFORMANCE
- PRICE MUST BE A GIVEN

**PRESENT** 

**FUTURE** 

**BIG GUYS** 

"AVIS"

LITTLE GUYS

LITTLE GUYS

**BIG GUYS** 

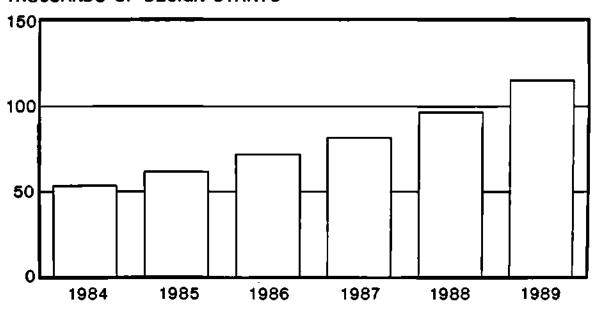
"AVIS"

# "IT'S THE ART THAT'S VALUABLE, NOT THE MECHANICS."

Source: Focus Group Participant

#### ESTIMATED ANNUAL IC DESIGN STARTS

THOUSANDS OF DESIGN STARTS



Source: DATAQUEST

# ESTIMATED ANNUAL IC DESIGN STARTS (Thousands of Designs)

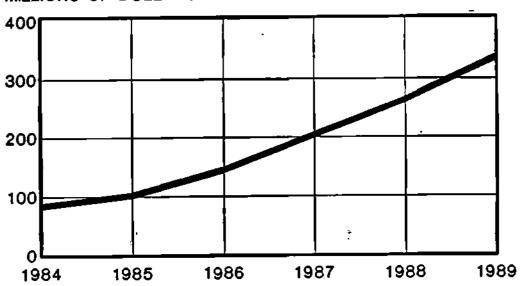
	<u>1984</u>	<u>1985</u>	1986	1987	<u>1988</u>	1989	CAGR
Design Starts	54	62	72	82	97	115	17%

# "IN OUR COMPANY, WE ARE NOT INTERESTED IN BEING CUSTOMER SUPPORT."

Source: Focus Group Participant

#### **ECAD SERVICE REVENUE**





### ESTIMATED ECAD SERVICE REVENUE (Millions of Dollars)

<u>1984</u> <u>1985</u> <u>1986</u> <u>1987</u> <u>1988</u> <u>1989</u> <u>CAGR</u> Service Revenue \$ 84 \$102 \$ 145 \$ 204 \$ 264 \$ 336 32\$

### PRODUCT JUSTIFICATION

- ROI
- DESIGNS PER ENGINEER
- COMPLEXITY
- TIME
- REWORKS
- SUCCESS RATIO

### PRODUCT JUSTIFICATION

- IS AN ITERATIVE PROCESS AND MUST COMPARE ACTUALS VERSUS ESTIMATES
- IS BASED ON COMMON SENSE

#### PRODUCTIVITY ISSUES

GOAL:

MEET DEADLINES

STRATEGY:

- INTEGRATION
- ACCELERATORS
- SIMULATORS
- PERSONAL COMPUTERS

#### PRODUCTIVITY ISSUES

GOAL:

MEET DEADLINES AND GET

IT RIGHT THE FIRST TIME

STRATEGY:

SIMULATION

• TEST GENERATION

CORRECT BY CONSTRUCTION

COMPILATION

 DATA BASE MANAGEMENT AND CONTROL

#### **SUMMARY**

- CHANGING GROUND RULES
- LIVE WITH COMPETITION
- INCREASED AUTOMATION MEANS INCREASED SUPPORT

# "PRODUCTIVITY EQUALS DOLLARS"

Source: Focus Group Participant

PERPOR STABILITY,

THE FOCUS GROUP PERCENTIONS

WHERE DOES 17 PANK?

MBOVE OR BELOW

SYSTEM FUNCTIONARY





AUTOMATIC IC GENERATION

Tony Spadarella Research Analyst Dataquest Incorporated

Mr. Spadarella is a Research Analyst for Dataquest's CAD/CAM Industry Service. He is responsible for research and analysis of the integrated circuit, printed circuit board, and electronic design automation CAD/CAM segments. He also supports general research activities. Before coming to Dataquest Mr. Spadarella was on the technical staff of Calma Company's Research and Development division, documenting the company's electronic design products, operating systems, and communications products. He also researched automated technical publications systems. Prior to that, he was with Singer-Link's Advanced Products organization, where he designed visual data bases and analyzed training requirements for flight Mr. Spadarella received a B.A. degree in simulation applications. English from Georgetown University in Washington D.C. and an M.A. degree in English from the University of Southern California in Los Angeles. He has done additional post graduate studies in marketing and advertising at Golden Gate University in San Francisco. He also teaches courses in technical writing at San Jose State University.

Dataquest Incorporated
DESIGN AUTOMATION FOCUS CONFERENCE
December 9 and 10, 1985
Palo Alto, California

# PRODUCTIVITY = CHANGE

#### **CHANGES IN:**

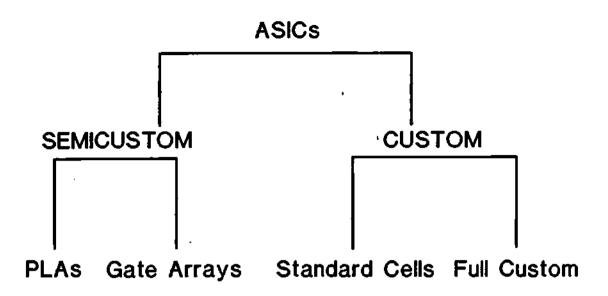
- ICs
- IC DESIGN TOOLS
- IC DESIGN METHODOLOGY

### **AGENDA**

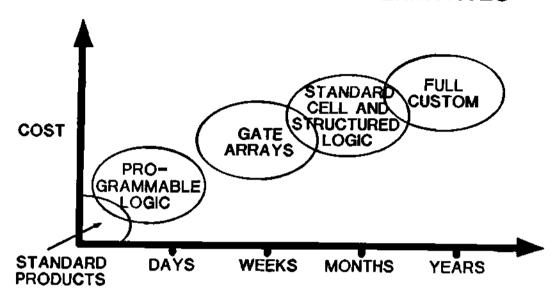
- ASIC MARKET
- AUTO IC LAYOUT
- IC CAD FORECAST

# **ASICs**

A PPLICATIONS PECIFIC
I NTEGRATED
CIRCUITS



#### ASIC IMPLEMENTATION ALTERNATIVES

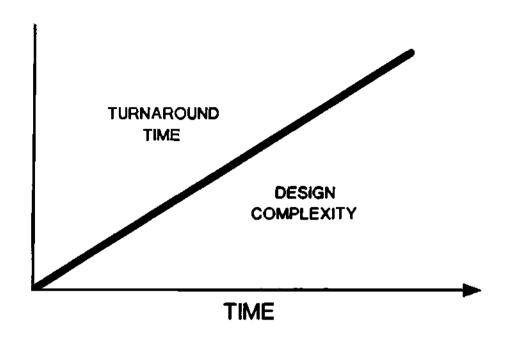


# **AVERAGE GATE COUNT**

1985

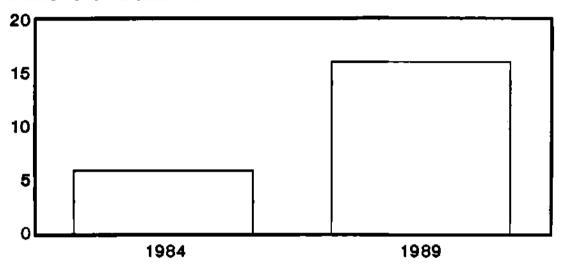
1987

2,500 - 4,000 8,000 - 13,000



# ESTIMATED TOTAL WORLDWIDE ASIC MARKET

#### **BILLIONS OF DOLLARS**

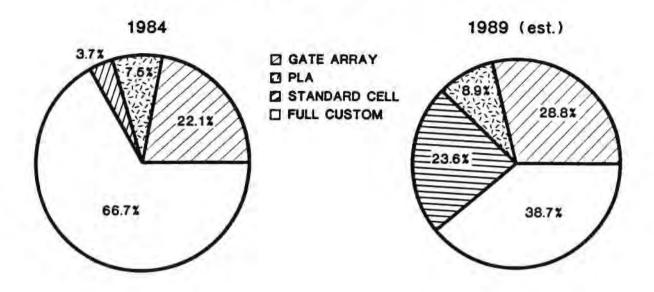


Source: DATAQUEST

### TOTAL WORLDWIDE ASIC MARKET (Billions of Dollars)

	1984	1989	CAGR	
ASIC	<b>\$5.9</b>	\$16.1	22%	

#### ASIC MARKET

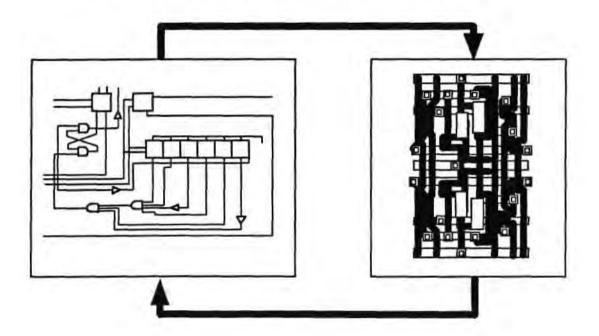


Source: DATAQUEST

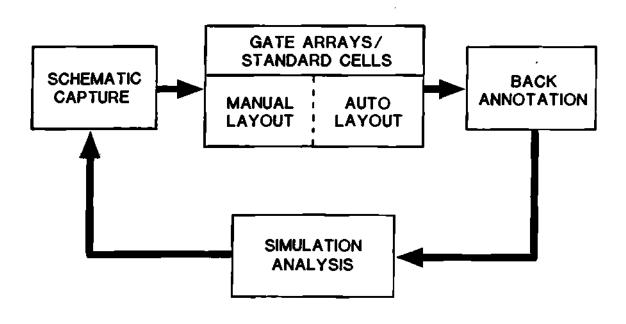
### ASIC MARKET (Millions of Dollars)

	1984	1989	CAGR
PLA	\$251.0	\$ 910.5	29.48
Gate Array	737.6	2932.7	31.8%
Standard Cell	122.9	2401.9	81.2%
Full Custom	2230.9	3950.0	12.1%

# TRADITIONAL APPROACH



#### **ASIC DESIGN PROCESS**



## **AUTO IC LAYOUT**

- QUICKER TURNAROUND
- LOWER NRE COSTS
- PROJECT CONTROL
- BETTER DESIGNS
- SECURITY

#### SCHEMATIC CAPTURE

- TIME INTENSIVE
- INDEPENDENT OF DESIGN RULE CHECKING
- POTENTIAL SOURCE OF ERRORS
- COMPLICATES LAYOUT PROCESS

## **AUTOMATED IC DESIGN**

INTEGRATED SOLUTION -

LOGICAL DESIGN

+

PHYSICAL LAYOUT

#### **IDEAL INTEGRATED SOLUTION:**

- "WHAT IF" ANALYSIS
- DATA BASE MANAGEMENT
- COMMON INTERFACE
- AUTOMATIC LAYOUT
- AUTOMATIC TEST GENERATION
- DESIGN DOCUMENTATION
- DESIGN VERIFICATION AND RULE CHECKING

## **AUTOMATED IC DESIGN**

TWO APPROACHES:

- EVOLUTIONARY
- REVOLUTIONARY

## **AUTO IC DESIGN**

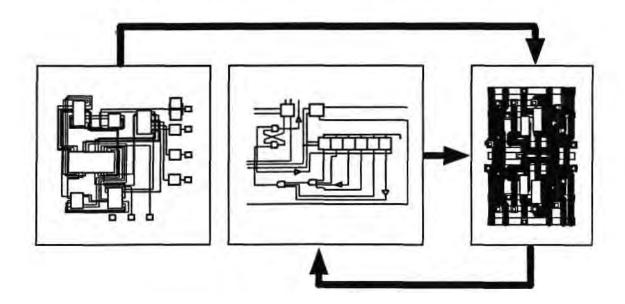
#### **EVOLUTIONARY APPROACH**

CURRENT DESIGN TOOLS

+

SILICON COMPILATION TECHNIQUES

## **EVOLUTIONARY APPROACH**

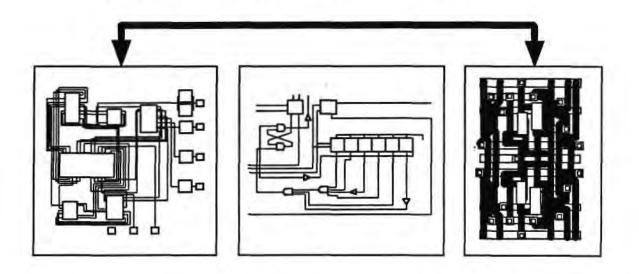


## **AUTO IC DESIGN**

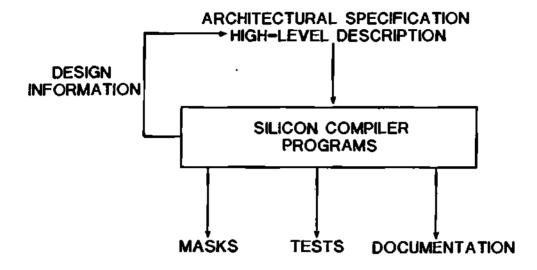
#### REVOLUTIONARY APPROACH

# "TRUE" OR FULL SILICON COMPILATION

## REVOLUTIONARY APPROACH



#### TRUE SILICON COMPILATION



#### SILICON COMPILER PROGRAMS

#### AUTOMATED:

- DETAIL DESIGN
- DESIGN VERIFICATION
- PHYSICAL DESIGN
- BACK-END VERIFICATION/DRC
- MASK GENERATION

# SILICON COMPILATION--A DESIGN TECHNIQUE

SILICON COMPILER--A CAD PRODUCT

#### **QUESTION:**

WHAT DO SILICON COMPILERS PRODUCE?

**──→** GATE ARRAYS?

→ STANDARD CELLS?

FULL CUSTOM ICs?

## **ANSWER:**

YES ...

- GATE ARRAYS WITH WIRE CHANNEL EXPANSION
- STANDARD CELLS MIXED WITH COMPILED BLOCKS
- FULL CUSTOM ACHIEVED BY BLOCK-LEVEL DESIGN TECHNIQUES

#### SILICON COMPILATION

#### BENEFITS:

- CREATIVITY TOOL
- DATA BASE MANAGEMENT
- STANDARD DESIGN PRACTICE
- REDUCED TURNAROUND TIME
- AUTOMATIC LAYOUT

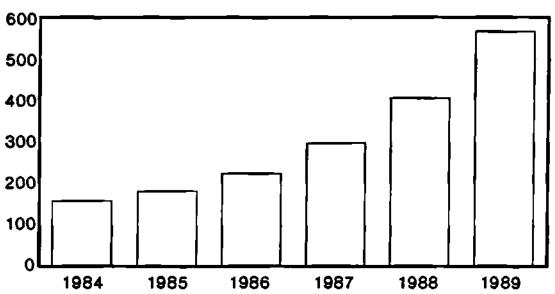
## SILICON COMPILERS

#### NEEDS:

- AUTOMATED TEST GENERATION
- MORE PARAMETRIC MODELS
- HIGHER COMFORT LEVEL

#### IC CAD WORLDWIDE FORECAST





Source: DATAQUEST

## IC CAD WORLDWIDE FORECAST (Millions of Dollars)

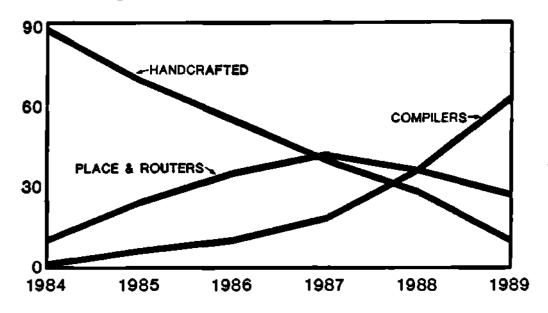
	1984	<u> 1985</u>	<u>1986</u>	<u>1987</u>	1988	1989	CAGR
IC CAD	\$157	\$181	\$224	\$298	\$408	\$571	29.5%

## IC CAD WORKSTATION SHIPMENTS

#### **UNITS**

1984 1989 (Est.) 1,211 8,751

# IC CAD WORKSTATIONS ESTIMATED PERCENT CHANGE

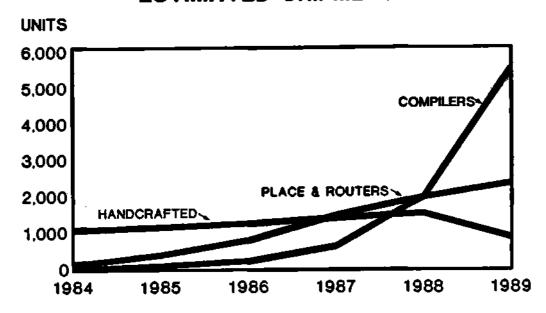


Source: DATAQUEST

IC CAD WORKSTATIONS (Percent Change)

	1984	<u>1985</u>	1986	1987	1988	1989
Compilers	1	6	10	18	36	63
Hand-Crafted	89	70	55	40	28	10
Place and Routers	10	24	35	42	36	27
Total	100	100	100	100	100	100

# IC WORKSTATIONS ESTIMATED SHIPMENTS



Source: DATAQUEST

## IC WORKSTATIONS ESTIMATED SHIPMENTS (Units)

	1984	<u>1985</u>	1986	<u>1987</u>	<u>1988</u>	<u>1989</u>	CAGR
Compilers	12	99	228	629	1975	5513	2418
Hand-Crafted	1075	1155	1255	1397	1536	875	-48
Place and Routers	124	396	798	1467	1975	2363	80€
Total	1211	1650	2281-	3493	5486	8751	49%

• SILICON COMPILATION IS A REPLACEMENT TECHNOLOGY

- SILICON COMPILATION IS A REPLACEMENT TECHNOLOGY
- THIRD-PARTY AGREEMENTS

- SILICON COMPILATION IS A REPLACEMENT TECHNOLOGY
- THIRD-PARTY AGREEMENTS
- DESIGN SERVICE AND TRAINING

- SILICON COMPILATION IS A REPLACEMENT TECHNOLOGY
- THIRD-PARTY AGREEMENTS
- DESIGN SERVICE AND TRAINING
- COOPERATION WITH ASIC HOUSES AND IC MANUFACTURERS

# CONCLUSION: AUTOMATED IC DESIGN

- SILICON COMPILER REVOLUTION LEADING AN EVOLUTION
- CAD VENDORS DRIVE THIS MARKET





DESIGN CENTER SURVEY

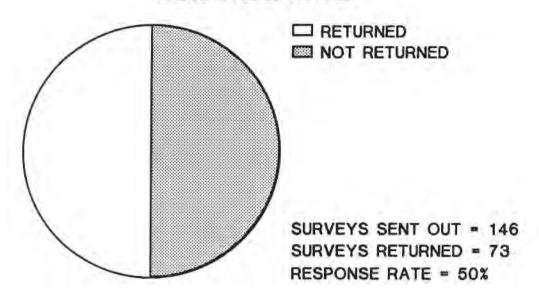
Relly Leininger Research Assistant Dataquest Incorporated

Ms. Leininger is a Research Assistant for the CAD/CAM Industry Service. She is responsible for research assistance in the electronic CAD/CAM segments, company profile research, data base support, and survey research. Ms. Leininger is doing degree work at San Jose State University.

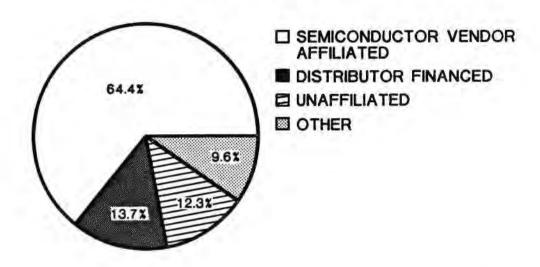
Dataquest Incorporated
DESIGN AUTOMATION FOCUS CONFERENCE
December 9 and 10, 1985
Palo Alto, California

- DEMOGRAPHICS
- DESIGN ENVIRONMENT
- USAGE
- FUTURE PLANS
- BOTTLENECKS

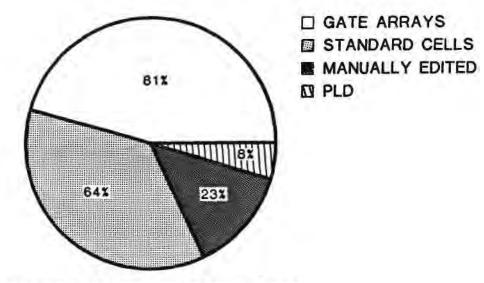
# DESIGN CENTER SURVEY RESPONSE RATE



# DESIGN CENTER SURVEY DISTRIBUTION OF RESPONSES BY COMPANY TYPE



#### **DESIGN CENTER SURVEY**

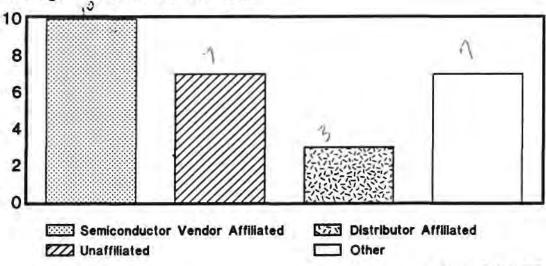


AVERAGE NUMBER OF GATES: 4,900

## DESIGN ENVIRONMENT

# DESIGN CENTER SURVEY DISTRIBUTION OF INSTALLED BASE BY COMPANY TYPE

Average Workstations Per Site



Source: DATAQUEST

#### DISTRIBUTION OF INSTALLED BASE BY COMPANY TYPE (Average Workstations Per Site)

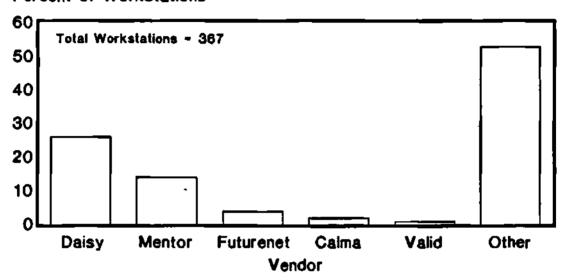
Semiconductor	Vendor	Affiliated	10
Unaffiliated			7
Distributor A	ffiliate	ed	3
Other			7

Source: DATAQUEST

- 6 -1985 Dataquest Incorporated-Reproduction Prohibited

# DESIGN CENTER SURVEY CAD/CAM INSTALLED BASE

#### Percent of Workstations



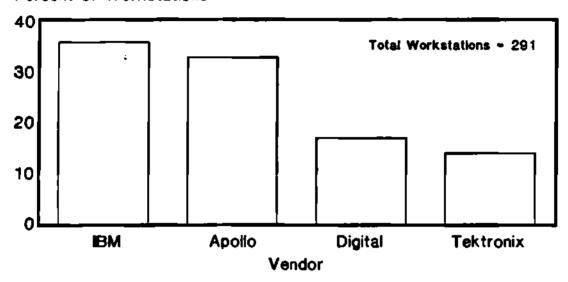
Source: DATAQUEST

 $\langle \gamma_i \rangle$ .

## CAD/CAM INSTALLED BASE (Percent of Workstations)

## DESIGN CENTER SURVEY NON-CAD/CAM INSTALLED BASE

#### Percent of Workstations

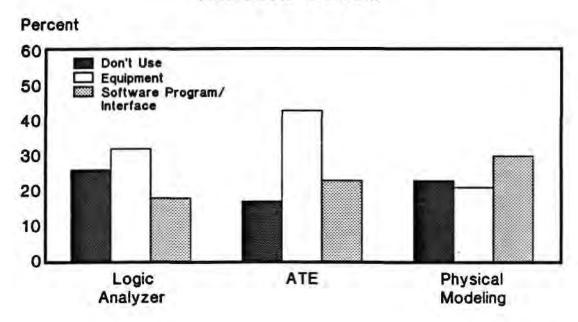


Source: DATAQUEST

#### NON-CAD/CAM INSTALLED BASE (Percent of Workstations)

IBM	36
Apollo	33
Digital	17
Tektronix	14

## DESIGN CENTER SURVEY TESTING TOOLS



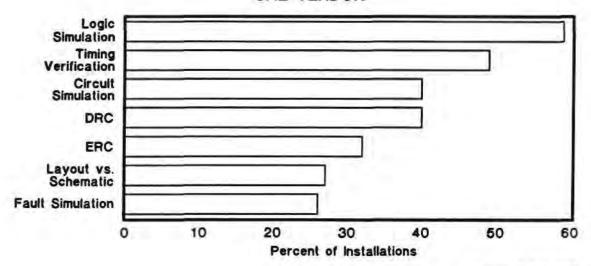
Source: DATAQUEST

### TESTING TOOLS (Percent)

	Don't Use	Equipment	Software Program/ Interface
Logic Analyzer	26	32	18
ATE	17	43	23
Physical Modeling	23	21	30

#### DESIGN CENTER SURVEY SOFTWARE ANALYSIS TOOLS INSTALLED BASE

#### CAE VENDOR



Source: DATAQUEST

# SOFTWARE ANALYSIS TOOLS INSTALLED BASE CAE VENDOR (Percent of Installations)

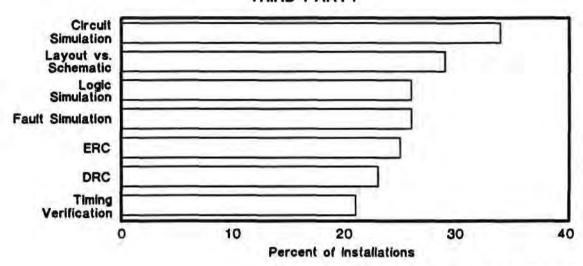
Logic Simulation	59
Timing Verification	49
Circuit Simulation	40
DRC	40
ERC	32
Layout vs. Schematic	27
Fault Simulation	26

Source: DATAQUEST

- 10 -1985 Dataquest Incorporated-Reproduction Prohibited

#### DESIGN CENTER SURVEY SOFTWARE ANALYSIS TOOLS INSTALLED BASE

#### THIRD PARTY



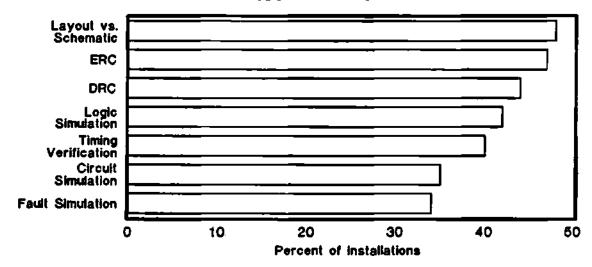
Source: DATAQUEST

# SOFTWARE ANALYSIS TOOLS INSTALLED BASE THIRD PARTY (Percent of Installations)

Circuit Simulation	34
Layout vs. Schematic	29
Logic Simulation	26
Fault Simulation	26
ERC	25
DRC	23
Timing Verification	21

# DESIGN CENTER SURVEY SOFTWARE ANALYSIS TOOLS INSTALLED BASE

#### **DEVELOPED IN-HOUSE**



Source: DATAQUEST

# SOFTWARE ANALYSIS TOOLS INSTALLED BASE DEVELOPED IN-HOUSE (Percent of Installations)

Layout vs. Schematic	48
ERC	47
DRC	44
Logic Simulation	42
Timing Verification	40
Circuit Simulation	35
Fault Simulation	34

Source: DATAQUEST

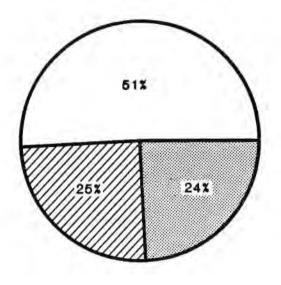
- 12 - 1985 Dataquest Incorporated-Reproduction Prohibited

### **DESIGN CENTER SURVEY**

- NUMBER OF ENGINEERS: 503
- ENGINEERS PER DESIGN CENTER: 7
- DESIGN STARTS: 3.259
- DESIGN STARTS PER ENGINEER: 7

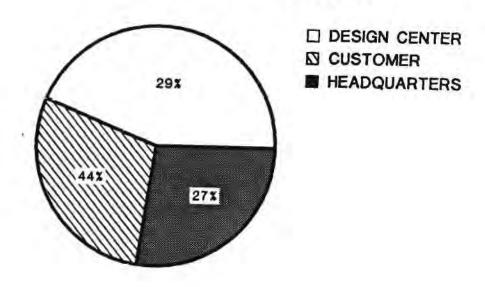
## **USAGE**

## DESIGN CENTER SURVEY WHO DOES THE DESIGN?

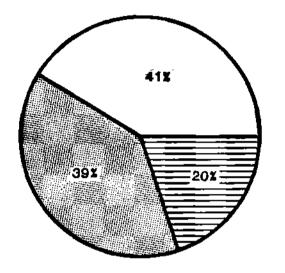


- ☐ IN-HOUSE ENGINEER
- ☑ COMBINATION OF IN-HOUSE ENGINEER AND CUSTOMER ENGINEER
- CUSTOMER ENGINEER

# DESIGN CENTER SURVEY WHO DOES SIMULATION?

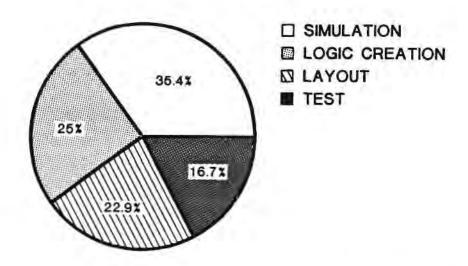


## DESIGN CENTER SURVEY SIMULATION SYSTEM TYPE

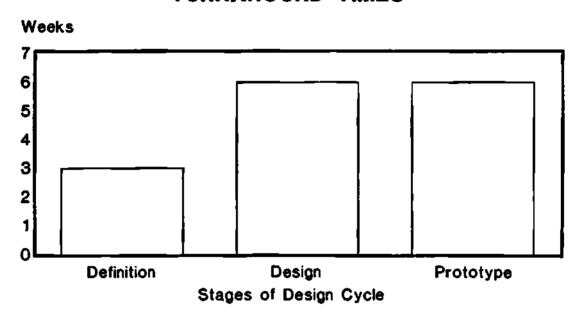


- ☐ WORKSTATION
- **MAINFRAME/MINI**
- **ACCELERATOR**

# DESIGN CENTER SURVEY AVERAGE DISTRIBUTION OF TIME PER DESIGN PHASE



## DESIGN CENTER SURVEY TURNAROUND TIMES

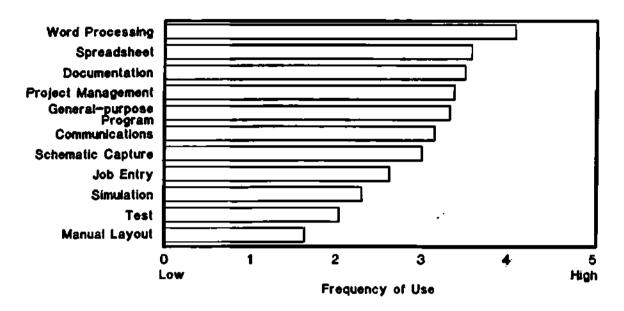


Source: DATAQUEST

### TURNAROUND TIMES (Stages of Design Cycle)

Definition 3 Weeks
Design 6 Weeks
Manufactured For Protype 6 Weeks

# DESIGN CENTER SURVEY USE OF PERSONAL COMPUTER SOFTWARE TOOLS



Source: DATAQUEST

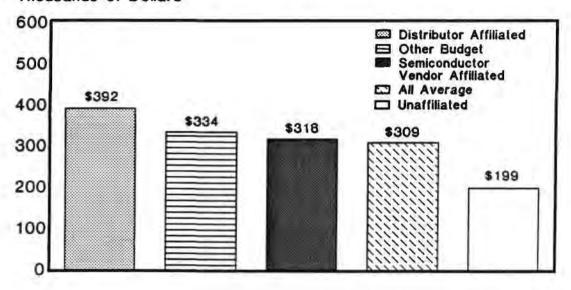
#### USE OF PERSONAL COMPUTER SOFTWARE TOOLS (Frequency of Use)

Word Processing	4.08
Spreadsheet	3.57
Documentation	3.50
Project Management	3.38
General-Purpose Program	3.32
Commnications	3.15
Schematic Capture	3.00
Job Entry	2.62
Simulation	2.30
Test	2.03
Manual Layout	1.63

### **FUTURE PLANS**

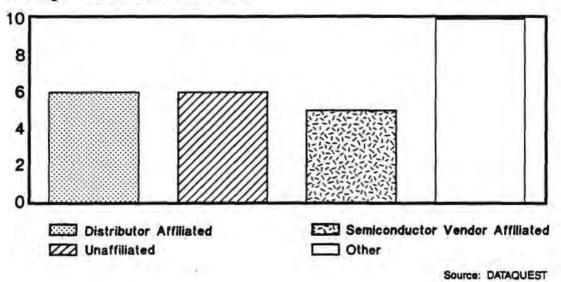
## DESIGN CENTER SURVEY AVERAGE BUDGET PER COMPANY TYPE

Thousands of Dollars



# DESIGN CENTER SURVEY WORKSTATION PURCHASE PLANS BY COMPANY TYPE

Average Workstations Per Site

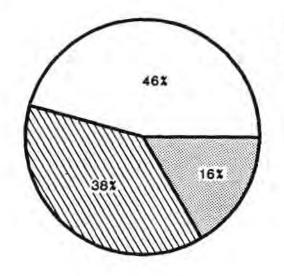


WORKSTATION PURCHASE PLANS BY COMPANY TYPE

(Average Workstations Per Site)

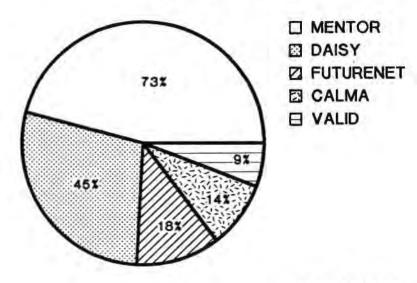
Semiconductor Vendor Affiliated	5
Distributor Affiliated	6
Unaffiliated	6
Other	10

## DESIGN CENTER SURVEY PURCHASE PLANS BY PRODUCT TYPE

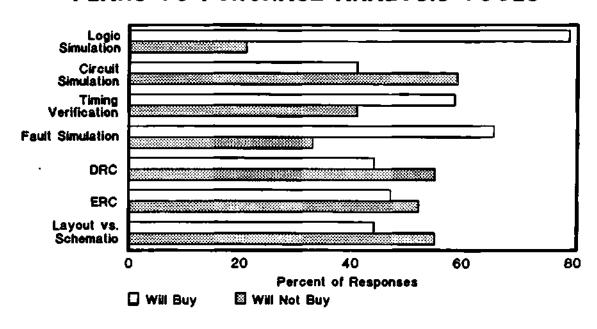


- ☐ STANDALONE
- M PC BASED
- M HOST DEPENDENT

# DESIGN CENTER SURVEY WORKSTATION PURCHASE PLANS BY VENDOR



## DESIGN CENTER SURVEY PLANS TO PURCHASE ANALYSIS TOOLS



Source: DATAQUEST

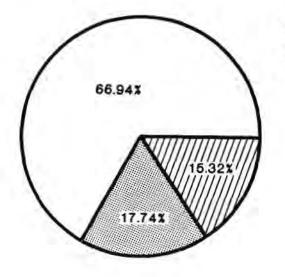
### PLANS TO PURCHASE ANALYSIS TOOLS (Percent of Responses)

	Will Buy	Will Not Buy
Logic Simulation	79	21
Circuit Simulation	41	59
Timing Verification	59	41
Pault Simulation	66	34
DRC	45	55
ERC	48	58
Layout vs. Schematic	45	55

Source: DATAQUEST

- 26 - 1985 Dataquest Incorporated-Reproduction Prohibited

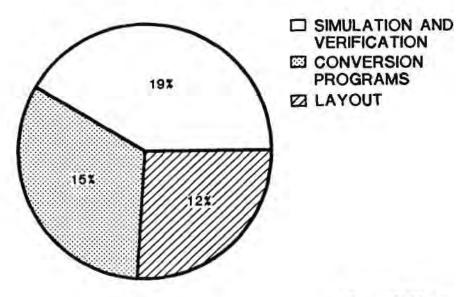
## DESIGN CENTER SURVEY DISTRIBUTION OF SYSTEM ARCHITECTURE

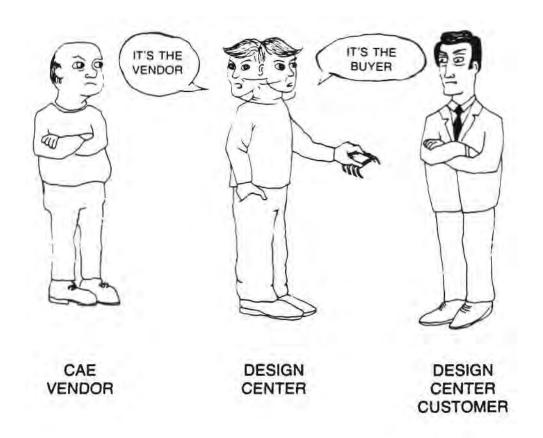


- ☐ WORKSTATION
- **■** HOST
- ACCELERATOR

## BOTTLENECKS

## DESIGN CENTER SURVEY BOTTLENECKS





#### **SUMMARY**

- PERSONAL COMPUTER
- CUSTOMER/VENDOR RELATIONSHIP
- TOOLS DEVELOPED IN-HOUSE
- TUCKER'S CAD/CAM LAW
- ACCELERATORS





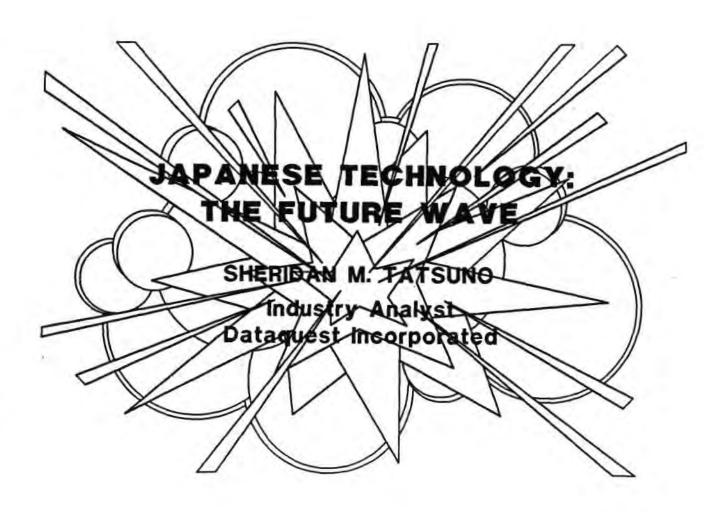
Dataquest Incorporated
A Subsidiary of A.C. Nielsen Company
1290 Ridder Park Drive
San Jose, California 95131
408/971-9000 / Telex 171973

JAPANESE TECHNOLOGY -- THE FUTURE WAVE

Sheridan M. Tatsuno
Industry Analyst
Japanese Semiconductor Industry Service
Dataquest Incorporated

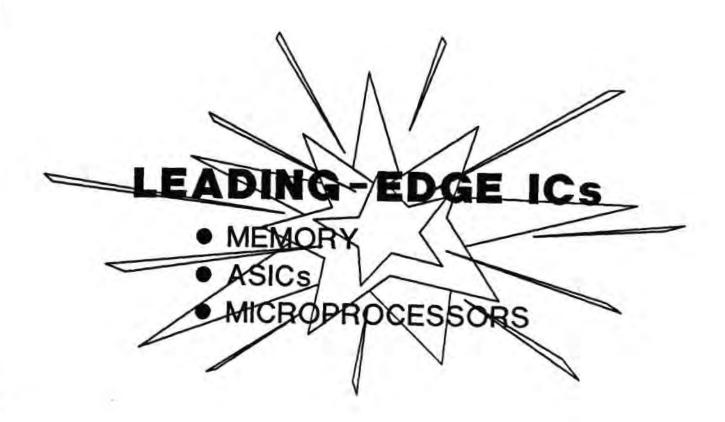
Mr. Tatsuno is an Industry Analyst for Dataquest's Japanese Semiconductor Industry Service. He is responsible for analyzing trends in Japanese government policies and financial markets. He is also responsible for analyzing technology trends within the industry, and specifically tracks R&D spending, patent applications, and new product developments quarterly. He has seven years of experience in market research, planning, and international finance with Bechtel and Woodward-Clyde Consultants. Mr. Tatsuno has a B.A. degree in Political Science from Yale University and a Master's degree in planning and Policy Analysis from Harvard University's Kennedy School of Government. In addition to these credentials, Mr. Tatsuno is fluent in Japanese, French, and Spanish, and has authored a book called The Technopolis Vision: Japan's High-Tech Strategy for the 1990's and Beyond.

Dataquest Incorporated
DESIGN AUTOMATION FOCUS CONFERENCE
December 9 and 10, 1985
Palo Alto, California



### **OVERVIEW**

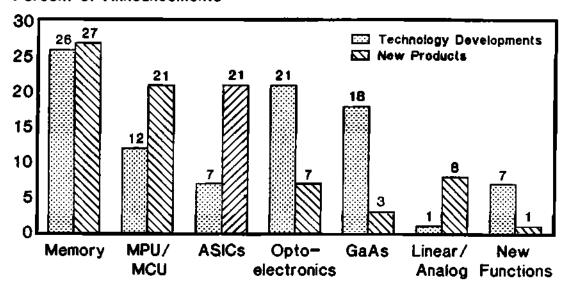
- LEADING-EDGE ICs
- JOINT R&D PROJECTS
- NEXT-GENERATION ICs
- NEXT-GENERATION COMPUTERS
- MARKET OPPORTUNITIES



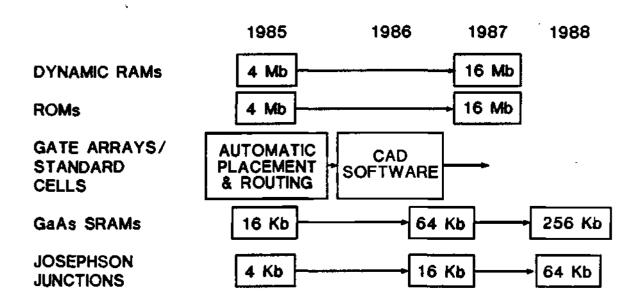
#### JAPANESE SEMICONDUCTOR TECHNOLOGY

1984

Percent of Announcements



#### FORECAST OF NTT RESEARCH PAPERS

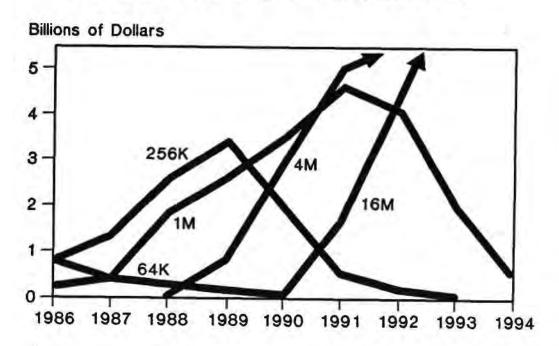


#### **MEGABIT DYNAMIC RAM TRENDS**

#### **DESIGN RULE**

<u>Year</u>	Device	Start	End	Technology
1983	1 <b>M</b> b	1.25	0.80	Steppers (5x, 1x)
1985	4Mb	0.80	0.50	Steppers (5x, 1x)
1990	16Mb	0.50	0.30	Synchrotron X-ray
1995	64 <b>M</b> b	0.25	80.0	Synchrotron radiation E-beam overexposure
				Bias exposure photolitho
1998	256Mb	0.10	0.05	Synchrotron radiation
2000+	1Gb	0.05	0.01	Bioelectronics

### DRAM MARKET FORECAST



#### **WORLDWIDE EPROM MARKET SHARE**

Rank	<u>64K</u>	128K	256K	<u>512K</u>
1	Hitachi	Hitachi	Intel	Intel
2	Mitsubishi	intel	AMD	AMD
3	Fujitsu	Mitsubishi	Hitachi	Hitachi
4	Intel	AMD	Toshiba	Fujitsu
5	TI	Fujitsu	Fujitsu	
Japanese				
Share:	68%	79%	41%	2%
1984 Avg.	68%	56%	18%	0
1985 Market Size:	\$286M	\$249M	\$ 189M	\$23M
OIZO:	4200W	42-3III	4 103W	450IAI

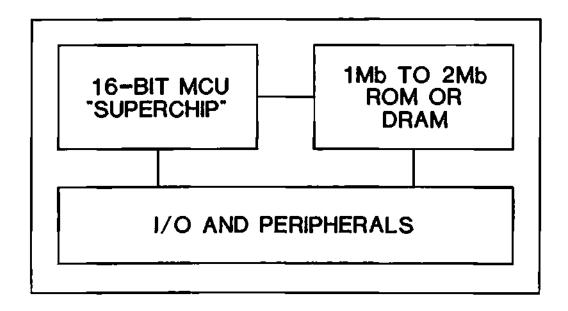
### SMART CARDS--THE NEXT PC MARKET?

Start	Group Leader	Application	IC Device
Dec. 1984	Mitsui Bank	Banking and Shopping	64K EPROM with 8-bit MPU
March 1985	Seibu Bank	Medical	16K EEPROM with CPU
May 1985	Sumitomo Bank	Shopping	64K EEPROM with CPU
July 1985	Toyo Trust Bank	Financial  Management	64K EPROM with CPU
Aug. 1985	Dai-Ichi Kangyo	Banking	64K EPROM with CPU
Oct. 1985	Sanwa Bank	Shopping	64K EEPROM with CPU
Oct. 1985	Fuji Bank	Corporate Banking	16K EEPROM with CPU
Oct. 1985	Daiwa Bank	Shopping	16K EEPROM with CPU
Oct. 1985	Toshiba	Point-of-Sale	64K EEPROM with CPU

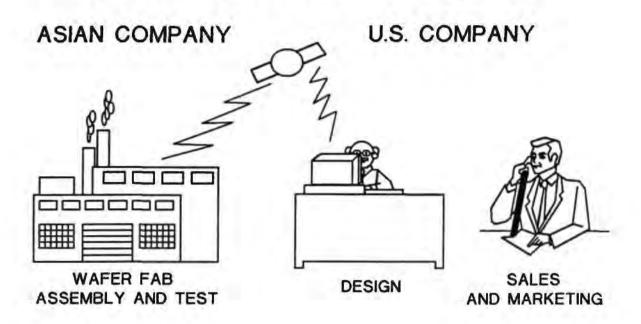
### JAPANESE EPROMs/EEPROMs

Company	EPROM	EEPROM
Fujitsu	256K CMOS	64K CMOS
Hitachi	256K/1Mb CMOS	64K CMOS
Mitsubishi	1Mb NMOS	256K CMOS
NEC	256K/1Mb CMOS	
Oki	64K NMOS	16K CMOS (Exel)
Ricoh	256K CMOS	
Suwa Seikosha	64K/128K CMOS	
Toshiba	256K CMOS	64K 'Flash' CMOS

## THE SHIFT TO STANDARD CELLS

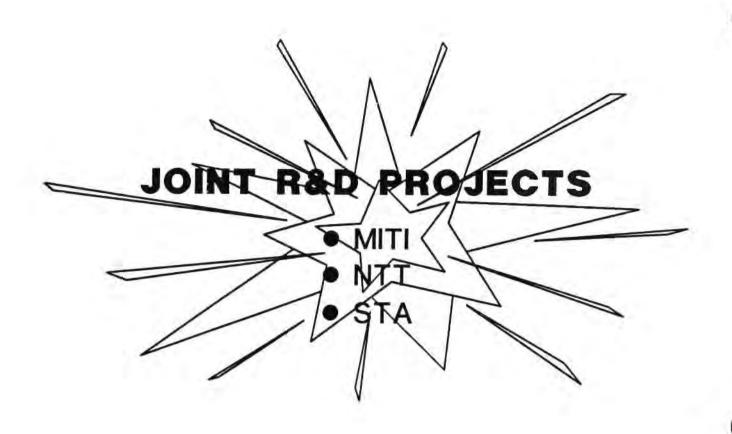


## "DESIGN BOUTIQUE" STRATEGY

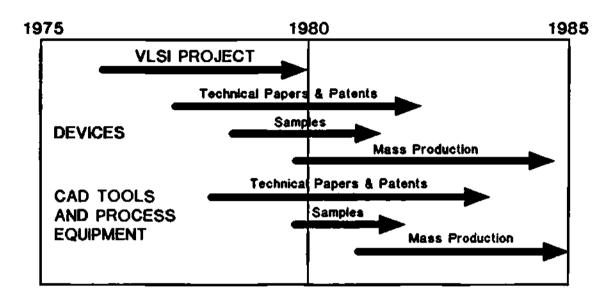


## JAPANESE 32-BIT MICROPROCESSORS

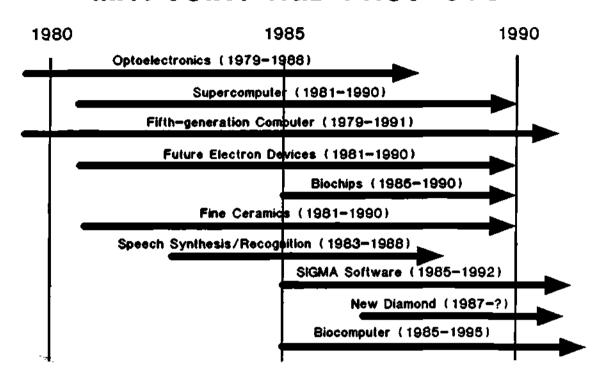
Year	Company	Product Line	Ties
1986	NEC	V60 (first generation)	Sony and Zilog
1987		V70 (second generation)	(V20/V30)
1986	Hitachi	68000Compatible CMOS	Motorola
		TRON Project	Tokyo University
1986	Fujitsu	80286 (16-/32-bit MPU)	Intel -
1986	Oki	Proprietary MPU	<del></del>
1987	Mitsubishi	TRON Project	Tokyo University
1987	Toshiba	Proprietary MPU	Zilog (Z8000)



## JAPANESE IC DEVELOPMENT CYCLE

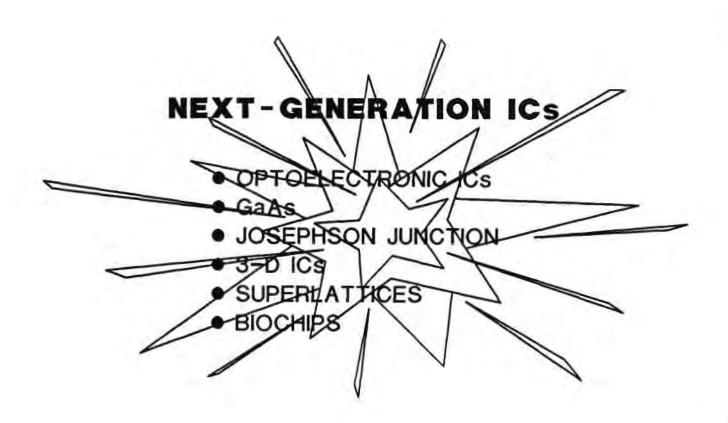


## MITI JOINT R&D PROJECTS

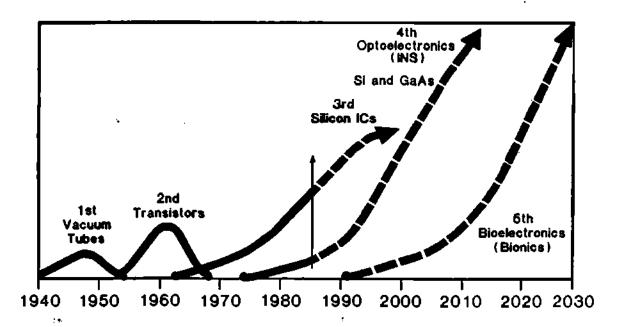


## OTHER GOVERNMENT-SPONSORED R&D PROJECTS

Agency	Project	Time Frame
NTT	INS computer	1984-1990
STA	Perfect GaAs crystals	1981-1986
STA	Amorphous compounds	1981-1986
STA	Nanomechanisms	1985-1990
STA	Solid-state surfaces	1985-1990



## OPTOELECTRONICS: THE NEXT GENERATION



## GaAs RESEARCH (1985)

Device	Company	Speed
4K SRAM	Fujitsu	1.7 ns
	Hitachi	2.2 ns
	NEC	2.4 ns
3.000-gate logic	NEC	30.0 ps
MESFET	Oki	14.7 ps
Gate arrays	Toshiba (2,000 gates)	42.0 ps
	Oki (1.000 gates)	390.0 ps
HEMT	Fujitsu	0.9 ns

## JOSEPHSON JUNCTIONS

Company	<u>Device</u>	Speed
Hitachi	Control terminal transistor	20 ps
NEC	4 x 4-bit parallel multiplier with 249 logic gates	350 ps
NEC	4 x 4-bit multiplier	280 ps

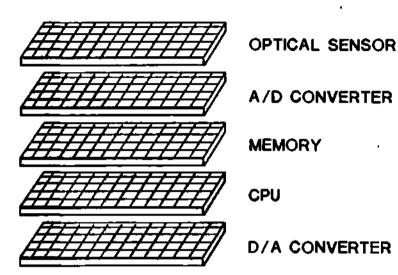
### **FUTURE ELECTRON DEVICES PROJECT**

Themes	81	82	83	84	85	86	87	88	89	90
		PHA	SE 1		PHASE 2		PHASE 3			
Superlattices (SL)	Ba	sic SL	Structe	ur e	Bas	ic Dev	ices	Integration		
	New Material System									
-	PHASE 1				PHASE 2			. PHASE 3		
Three- Dimensional ICs	Mu	Itilayer	Struct	ure	Test Element Group					
(3-D ICs)	Basic Technology Process Technology Device Design System Design									
	PHASE 1 PHASE 2 PHASE 3									
Hardened ICs	Testing Technique Test Device Integration									
	Device, Process Modification									

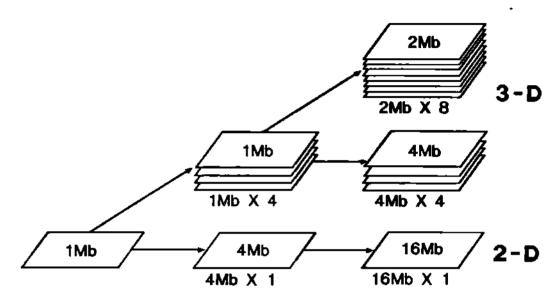
## FIVE-LEVEL 3-D IC

#### **ADVANTAGES**

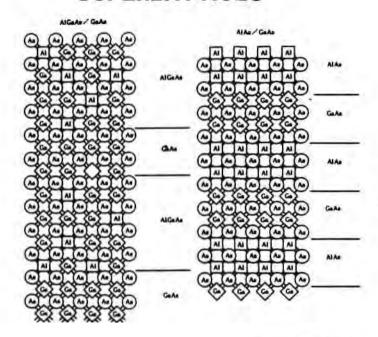
HIGHER DENSITIES
HIGHER SPEEDS
PARALLEL
PROCESSING
MULTIPLE
FUNCTIONS



## MEGABIT MEMORIES -- THE SHIFT TO 3-D ICs



### SUPERLATTICES



#### **BIOCHIP RESEARCH**

#### COMPANY

#### RESEARCH FOCUS

ASAHI CHEMICAL LIGHT-SENSITIVE ORGANIC SEMICONDUCTOR

DOJIN CHEMICAL THIN-FILM BIOCHIP SUBSTRATE

FUJITSU BIOSENSORS, THIN-FILMS, BIOCHIPS HITACHI BIOCHIPS, ARTIFICIAL INTELLIGENCE

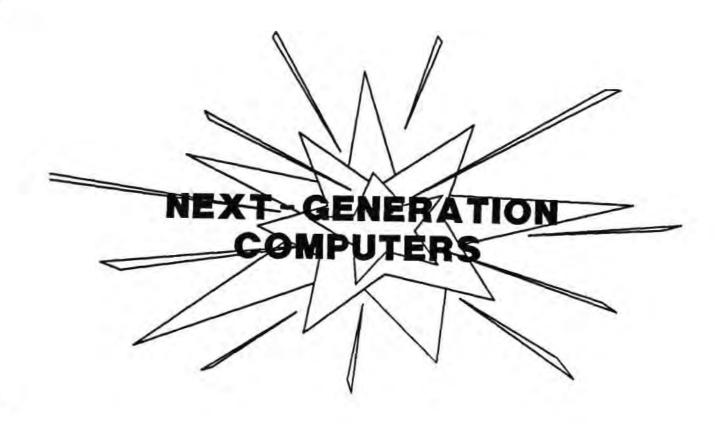
KURARAY IMPLANTABLE BIOSENSORS
MITI ORGANIC SUPERCONDUCTORS

MATCHICLETA MATCHICATER SOLUBLE BUOTORSOLUTIONS

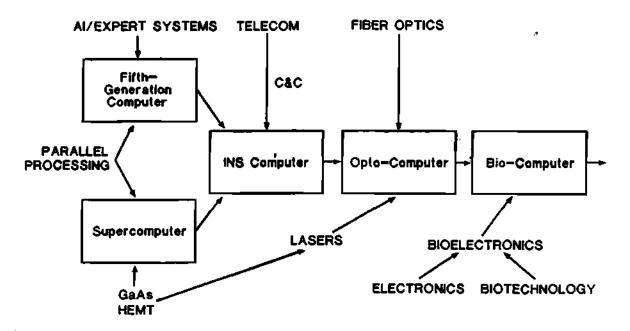
MATSUSHITA WATER-SOLUBLE PHOTORESIST

MITSUBISHI ENZYME BIOSENSORS
NEC MEDICAL BIOSENSORS
SHARP

SHARP BIOCHIPS, BIOCOMPUTERS TOSHIBA MULTI-ION BIOSENSORS



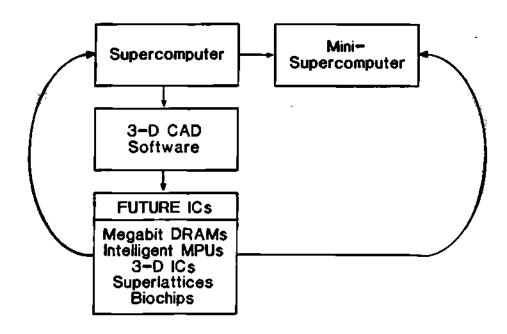
### JAPAN'S NEXT-GENERATION COMPUTERS



## MITI SUPERCOMPUTER PROJECT (1981-1989)

	Fujitsu	Hitachi	Mitsubishi	NEC	<u>Oki</u>	Toshiba
Semiconductors						,
Josephson Junction	X	X		X		
GaAs Digital ICs			X	X		X
HEMT	X				X	•
ECL Logic		X	X			
Systems						
Architecture	X					
Large-Capacity Storage				X		
Parallel Processors			X		X	X
Software		X				

#### **FUTURE SUPERCOMPUTER CAD TOOLS**



## MITI FIFTH-GENERATION COMPUTER CHIPS (1979-1991)

**FUNCTION** 

**DEVICE REQUIRED** 

Natural language processing

Voice recognition and synthesis chips

Megabit DRAMs and ROMs
D/A and A/D converters

Image processing

Graphics chips

Optoelectronic ICs (OEICs)

Semiconductor lasers CCD image sensors

Parallel processors

32-bit microprocessors (MPUs)

"Intelligent" MPUs with lasers (Si/GaAs)

inference machines and

data flow

GaAs and other III-V devices

Josephson junctions

High-electron mobility transistors (HEMT)

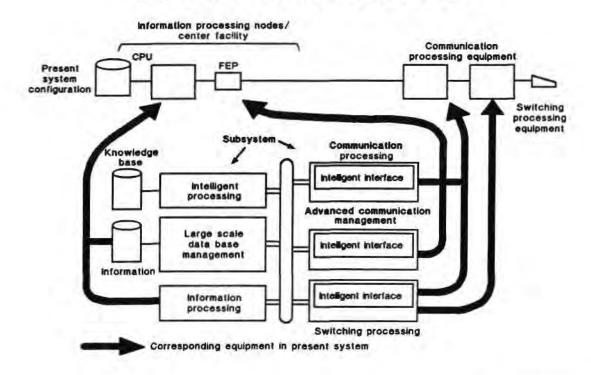
VLSI architecture

VLSI CAD tools

7(%)

VLSI testing equipment

#### CONCEPT OF INS COMPUTER



## IC RESEARCH FOR INS COMPUTER

- MEGABIT MEMORY PROCESSING
   (4/16/64Mb) -- E-BEAM FOR SUBMICRON;
   SYNCHROTRON OPTICAL RADIATION FOR
   SUB-HALF-MICRON
- HIGH SPEED LOGIC--GaAs ICs, JOSEPHSON JUNCTIONS, BALLISTIC TRANSISTORS
- OPTICAL TRANSMISSION--SEMICONDUCTOR LASERS AND OPTOELECTRONIC ICs (OEICs)

### IC RESEARCH FOR INS COMPUTER

- MOBILE AND SATELLITE TRANSMISSION—— GaAs MICROWAVE
- ELECTRONIC SWITCHING AND DIPS COMPUTER--16-BIT AND 32-BIT MPUs
- VIDEO PROCESSING——CCD SENSORS, WAFER SCALE VIDEO CHIPS
- DIGITAL SUBSCRIBER LOOPS—AUDIO AND VIDEO CODES
- TELEPHONE CIRCUITS—SUBSCRIBER LINE INTERFACE CIRCUITS (SLICs) AND ONE—CHIP TELEPHONE LSIS

## THE SIXTH-GENERATION COMPUTER -MITI'S BIO-COMPUTER PROJECT

- \$40 MILLION FUNDING (1985-1995)
- MIMICS HUMAN BRAIN FUNCTIONS (PATTERN RECOGNITION, REASONING, AND LEARNING)
- FOUR RESEARCH AREAS:
  - NEW COMPUTER ARCHITECTURE
  - BIOCHIP DEVELOPMENT
  - NEURAL SYSTEMS OF LOWER ANIMALS
  - NONDESTRUCTIVE, NONCONTACT METHODS FOR MEASURING HUMAN BRAIN ACTIVITY



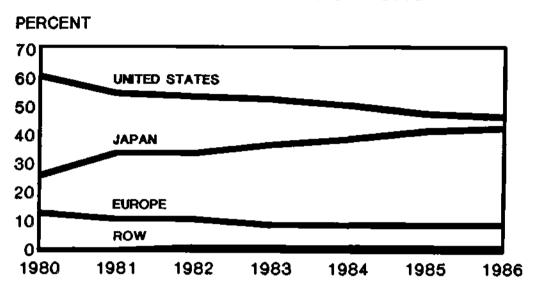
## **WORLDWIDE SEMICONDUCTOR REVENUES**

(Millions of Dollars)

	1984	1985	PERCENT CHANGE	1986	PERCENT CHANGE
U.S.A.	13,333	9,729	(27.0)	10,513	8.1
JAPAN ,	8,687	8,186	( 5.8)	9,172	12.0
EUROPE	4.805	4,700	( 2.2)	5,454	16.0
ROW	2.073	1,433	(30.9)	1,612	12.5
TOTAL	28,898	24,048	(16.8)	26,751	11.2

## **REGIONAL MARKET SHIFTS**

## **TOTAL SEMICONDUCTORS**



## **REGIONAL MARKET SHIFT**

## REGIONAL MANUFACTURERS' SHARE OF TOTAL SEMICONDUCTORS (Percent)

	1980	1981	1982	1983	1984	1985	1986
WORLD	100	100	100	100	100	100	100
UNITED STATES	61	55	54	53	51	48	47
JAPAN	26	34	34	37	39	42	43
EUROPE	13	11	11	9	9	9	9
ROW	0	0	1	1	1	1	1

## CAPITAL SPENDING BY JAPANESE SEMICONDUCTOR COMPANIES

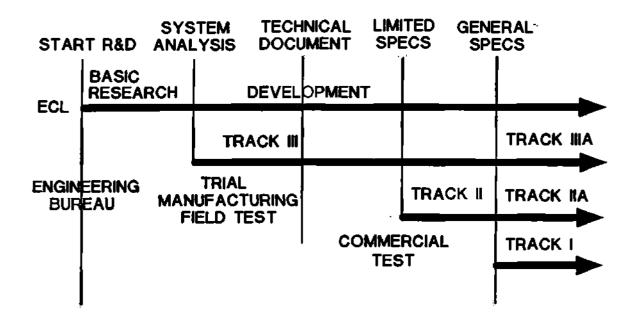
(Millions of Dollars)

	CAPITAL	EXPENDITURES	PERCENT OF SEMICONDUCTOR SALE		
	1984	1985 (Est.)	PERCENT CHANGE	1985 (Est.)	
NEC	591	420	(28.9)	23	
HITACHI	548	297	(45.8)	20	
TOSHIBA	624	480	(23.1)	35	
FUJITSU	527	280	(46.9)	38	
MATSUSHITA	401	340	(15.2)	39	
MITSUBISHI	295	224	(24.1)	28	
SHARP	118	160	35.6	47	
SANYO	148	184	24.3	37	
OKI	118	100	(15.3)	<u>34</u>	
TOTAL	3,370	2.485	(26.3)	<del>301</del>	

## STRATEGIC ALLIANCES (1985)

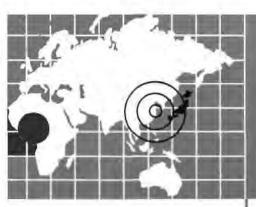
U.S. FIRM	JAPANESE FIRM	RESEARCH FOCUS
Hewlett-Packard	Toshiba	VLSI technology exchange
LSI Logic	Toshiba	'Sea of Gates' development
Westinghouse, General Electric	Mitsubishi	Diodes, power transistors
Tektronix	Sony	MPU development support system for NEC series
Veeco	Kanematsu Semiconductor	lon implanters
Vitelic	NMB Semiconductor	CMOS 1Mb DRAM
Tektronix, Digital Research, HP (Yokogawa)	NEC	MPU development support system for NEC V series

#### NTT RESEARCH AND DEVELOPMENT



## JOINT R&D WITH NTT

U.S. COMPANY	RESEARCH FOCUS
IBM	LINK-UP OF IBM'S SYSTEM NETWORK
	ARCHITECTURE WITH NTT NETWORK
AT&T	JOINT VAN DEVELOPMENT AND MARKETING
EATON	JOINT DEVELOPMENT OF OXYGEN
	ION IMPLANTERS
MOTOROLA	JOINT IC RESEARCH FOR INS COMPUTER
TEXAS INSTRUMENTS	JOINT IC RESEARCH FOR INS COMPUTER
ENERGY CONVERSION	JOINT DEVELOPMENT OF AMORPHOUS
DEVICES (ECD)	MEMORIES



A semimonthly report on Japanese and Asian High-Technology Industries

# I.C. ASIA

Compiled by DATAQUEST's Japanese Semiconductor Industry Service



12/04/85

I.C. ASIA 1985-30

Subscription Information on Back Page I.C. ASIA is a news digest published semimonthly by DATAQUEST's Japanese Semiconductor Industry Service (JSIS). To order a one-year subscription (22 issues), mail your check or money order for \$430 to:

I.C. ASIA 1290 Ridder Park Drive, M.S. 2-305 San Jose, CA 95131-2398

#### MAJOR EVENTS

SEMICONDUCTOR MAKERS REVISE PLANS FOR FY85, Pg. 2 YAMAGUCHI NIPPON PLANS TO PRODUCE 1Mb DRAM, Pg. 4 SEIKO EPSON TO BEGIN 256K SRAM PRODUCTION, Pg. 5 TOSHIBA REVISES GATE ARRAY SALES PLAN, Pg. 6

The exchange rate used in this issue is ¥206/US\$.

Each month I.C. Asia presents indicators on the IC industry in Asia. This set covers exports of integrated circuits from Japan to the ten largest countries of destination. The data shown below cover only finished goods at export value.

#### EXPORTS OF INTEGRATED CIRCUITS FROM JAPAN\* SEPTEMBER 1985

			Sep	September 1985			Total (JanSep. 1985)				
-	king Aug.	Country	Units (Thousands)	Volue (Millions of Yen)	Value Change from Sep. 184 (%)	Units (Thousands)	Value (Millions of Yen)	Value Change from Jan.—Sep. (光)			
-	-	United States	25,984	11,874	-60	285,860	170,011	-31%	_		
2	2	West Germony	11,675		-377			14%			
234567	3	Hong Kong	24,573		-513		45,237	-29%			
4	5	Taiwan	21,474		-3		28,599	13%			
5	4	Korea	21,226	3,868	-113		28,707	145			
6	6	Singapore	8,645	1,626	-569	97,339	14,381	-29%			
	7	United Kingdom		865	-32			-25%			
8		Brazil	1,296	542	23		6,371	-6%			
9	9	China	3,195	465	2369		3,883	332%			
10	12	Italy	1,238		869	10,563	4,218	88%			
	Subt	otal (top 10)	121,701	29,524		1,251,730	364,247				
-	Total	(163 countries)	138,292	31,713	-688	1,337,014	390,135		-17%		
		a percen- total	9.3	930		949	9.36	D.			

·Excludes hybrids

Source: Japanese Ministry of Finance: DATACLEST

#### INDUSTRY

64K DRAMs and 128K EPROMs in Short Supply

Semiconductor Makers Revise Plans for FY85 There have been shortages of 64K DRAMs and 128K EPROMs recently due to makers' rapid reductions in production. Major makers' 64K DRAM production, which reached 10 million units per month late last year, has declined to 1 million to 2 million units monthly. Some manufacturers have stopped production altogether. Inventories of 64K DRAMs are down sharply, and it is expected that the shortage of supply will become critical toward the end of this year.

Major semiconductor manufacturers have announced their financial statements for the first half of fiscal 1985, which started in April. Since their sales during the period decreased dramatically from the year before, sales and capital expenditure plans for fiscal 1985 have been revised downward. Major makers' revised production and investment plans are shown in the following table.

## MAJOR JAPANESE SEMICONDUCTOR MANUFACTURERS' REVISED FISCAL 1985 PLANS (Billions of Yen)

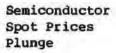
	Production					Capital Expenditure		
	Initial Plan	Pirst Halt Production	Change from First Half FY84	Revised Plan	Change from FY84	Initial Plan	Revised	Change from FY84
N&C	650	236	(190)	510	(144)	140	120	(246)
Hitachi	540	215	(204)	430	(20%)	130	9.0	13181
Toshiba	500	105	(10 %)	185	(118)	120	100	(324)
Pujitau	340	105	(201)	220	(178)	100	68	(488)
Matsushita Electronics (Year-end; December)	300	N/A	N/A	220	0	90	70	(20-304)
Mitsubishi Electric	270	7.4	(364)	165	(30%)	70	50	(134)
Tokyo Sanyo (Year-end: November)	140	N/A	H/A	115	54	46	46	464
Oki Electric	100	37	(104)	- 81	(5%)	_32	_25	(314)
Total (8 firms)	2,840	N/A	N/A	2,126	(144)	728	577	(286)

Note: Fujitsu's capital expenditure is tor all electronic devices; approximately 90 percent will be spent on assiconductor investment. NEC's production includes overseas value added. Oki's production is an estimate.

N/A . Noc Available.

Source: Dempa Shimoun

256K DRAM Price Down to ¥350 per Unit The lowball 256K DRAM price for large users in the Tokyo market declined to ¥350 (\$1.70) per unit the first week of November, down 23.6 percent from a month ago. There is a strong probability that the average price of the 256K DRAM will drop further to ¥200 (\$0.97) by the end of the year. Keen sales competition has led to the continuing oversupply.



8-Bit MPU Price Down

Semiconductor Price Information Spot market semiconductor prices, which had been rising since last spring, have plunged again due to decreasing exports and prolonged sluggish domestic demand. Steep drops have occurred in DRAMs and EPROMs. Prices of 64K DRAMs are less than ¥90 (\$0.44) per unit and 256K DRAMs are selling for ¥260 to ¥280 (\$1.26 to \$1.36) per unit. The 128K EPROM price has decreased by 5 to 10 percent from a month ago; it is currently ¥320 (\$1.55) per unit.

Prices of 8-bit microprocessors have decreased in the Tokyo market, due mainly to sluggish demand for OA equipment. The average wholesale price for large users is ¥210 (\$1.02) per unit or less for the 8085A model as well as for the 280A. This is a 10 to 15 percent decline from last summer's price. The 80C49 price has also declined by 10 percent to ¥500 (\$2.43) per unit or lower.

#### SEMICONDUCTOR PRICES IN TOKYO AS OF NOVEMBER 12, 1985\*

	Price	Price
Part	(Yen)	(Dollars)
Logic		
4001	¥18-¥20	\$0.09-\$0.10
4007	¥18-¥20	\$0.09-\$0.10
7400	¥18-¥20	\$0.09-\$0.10
7404	¥19-¥20	\$0.09-\$0.10
Micro Devices		
8085A	¥190-¥230	\$0.92-\$1.12
8086 (5MHz)	¥1,050-¥1,250	\$5.10-\$6.07
68000 (8MHz)	¥2,200-¥2,400	\$10.68-\$11.65
Memory		
64K DRAM	¥120-¥140	\$0.58-\$0.68
256K DRAM	¥350-¥450	\$1.70-\$2.18
16K SRAM (CMOS)	¥180-¥210	\$0.87-\$1.02
64K SRAM (CMOS)	¥380-¥460	\$1.84-\$2.23
64K EPROM	¥230-¥270	\$1.12-\$1.31
128K EPROM	¥370-¥470	\$1.80-\$2.28
256K EPROM	¥600-¥680	\$2.91-\$3.30

Exchange rate = ¥206/US\$1

Source: Japan Economic Journal

<sup>\*</sup>Yen wholesale price for large users, 90- to 120-day promissory notes.

#### COMPANY

Asahi Glass Signs Contract with VTI

Matsushita Completes Submicron VLSI Research Building

Mitsubishi Announces Half-Year Financial Report

NEC Controls 64K DRAM Production

Yamaguchi Nippon Plans to Produce 1Mb DRAM Asahi Glass Co., Ltd., has signed a sales agency contract with VISI Technology, Inc., (VTI) of the United States and has begun selling the U.S. company's products, including semicustom LSIs, in the Japanese market. Sales of the VTI products in the initial year are targeted at ¥l billion (\$4.9 million).

Matsushita Electric Industrial Co., Ltd., held a ceremony on October 28 to mark the completion of its Submicron VLSI Research Building within the company's Semiconductor Research Center, which was set up last year. The six-story building, with 17,000 square meters of floor space, has been furnished with the most advanced equipment for VLSI research and development. Investment in the building totaled approximately ¥20 billion (\$97 million).

Mitsubishi Electric Corporation has announced its financial statement for the first half of fiscal 1985, which started in April. Sales during the period totaled ¥882.543 billion (\$4.3 billion), up 0.9 percent over the year before. Operating profits and net profits of the term registered ¥28,275 billion (\$137 million) and ¥12.275 billion (\$60 million), down 19.4 percent and 14.7 percent, respectively.

NEC Corporation has stopped fabrication of 64K DRAMs, in an effort to reduce inventory rapidly. Assembly and test of the 10 to 15 million units on hand will be continued. At present, the company assembles and tests 2 million to 3 million 64K DRAMS per month. This will be reduced to 1 million units by March 1986. NEC will maintain a portion of its 64K DRAM fabrication facilities so that production can be reopened at a later date.

Yamaguchi Nippon Denki, a subsidiary of NEC Corporation, held a ceremony for completion of its headquarters factory in Yamaguchi prefecture on November 13. Construction of the first line of this advanced VLSI factory was completed in April and the plant is now producing 4 million units per month. Koji Kobayashi, chairman of NEC Corporation, and Atsuyoshi Ouchi, NEC vice chairman, held a press interview at the opening. They said that NEC plans to make Yamaguchi Nippon Denki a main production factory for 1Mb DRAMs. In the second phase of

NBC Officers Discuss Semiconductor Business

NMB to Introduce Technology from U.S. Firms

Seiko Epson to Begin 256K SRAM Production construction, the 256K RAM production line will be strengthened so that 256K static RAMs can be produced in the future. When the second part of the construction work has been completed, VLSI production will be doubled to 8 million units per month.

A. Ouchi, vice chairman of NBC Corporation, and T. Matsumura, senior vice president of the company, talked about the company's semiconductor business in the current fiscal year at a press interview on October 30. Among the points they covered in the discussion were:

- Production of semiconductors and other electronic components will total ¥660 billion (\$3,204 million), down 6 percent from the year before.
- Although capital expenditure plans have been lowered, research and development investment in the Silicon Research Center in Sagamihara will be doubled to ¥19 billion (\$92 million).
- Semiconductor exports will total ¥86 billion (\$417 million), down 39 percent from the year before.
- Sample shipment of 1Mb DRAMs is scheduled to begin late this year or early next year.

NMB Semiconductor Co., Ltd., has signed a technology agreement with two U.S. companies under which it will begin production of 64K SRAMs and 1Mb DRAMs late this year or early in 1986. The U.S. firm that is licensing 64K SRAM technology to NMB has not yet been disclosed, but the devices to be produced will be 35-, 45-, and 55-nanosecond CMOS models. Monthly production will initially be 500,000 units. The 1Mb DRAM technology has been licensed by Vitelic Corp. Production will begin in January or February 1986 at a monthly rate of 500,000 units. Fifty percent of the products will be supplied to Vitelic on a foundry basis.

Seiko Epson Corporation has disclosed that it will begin volume production of 256K SRAMs at its Fujimi Factory in Nagano prefecture in July 1986. The company established the 256K SRAM production line in Fujimi Factory in April of this year, but it has not been brought up yet due to the sluggish semiconductor demand. The 256K SRAM production capacity at Fujimi is 20 million units per year. Sample shipment is scheduled to begin late this year.

Toshiba Sales Gain 9 Percent in First Half of FY85 Toshiba Corporation announced its financial statement for the first half of fiscal 1985, which began in April. Sales during the period totaled ¥1,323.5 billion (\$6.4 billion), up 9 percent over the year before. Operating profits decreased by 9 percent to ¥62.034 billion (\$301 million), and net profits of the term registered ¥38.134 billion (\$185 million), up 11 percent. The company expects that total sales and profits during the current fiscal year will be as follows:

- Sales: ¥2,620 billion (\$12 billion), up
   4 percent over the previous year
- Operating profits: ¥117 billion (\$568 million), down 19 percent from the previous year
- Net Profits: ¥38.1 billion (\$185 million), down
   4 percent from the previous year

Toshiba Corporation has agreed with SGS Microelettronica SpA of Italy on a joint development and mutual second-source supply of telecommunication LSIs. The two firms signed a contract in 1982 regarding CMOS fine-process technology.

Toshiba Corporation has revised its gate array sales plan for fiscal 1985, which will end in March 1986, to ¥15 billion (\$73 million), up 25 percent over the previous year. The initial plan was ¥20 billion (\$97 million). The revision is due to the continuing decline in prices; actual demand for gate arrays has still been brisk.

United Microelectronics Corp. (UMC) of Taiwan has reported revenue of NT\$949 million and profits of NT\$89 million in the first three quarters of 1985. Vice President John Hsuan expects business to be up 20 percent in 1986.

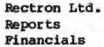
Taiwan Liton Electronics Co. has recently announced several new products. One is an infrared photocoupler for use in both industrial control devices and consumer electronic remote control devices. The company has also developed a microcontroller-equipped pedometer that can be attached to sport shoes to keep track of mileage.

Toshiba, SGS Strengthen Relationship

Toshiba Revises Gate Array Sales Plan

UMC Reports Financials

Liton Introduces New Products



Rectron Ltd., a Taiwanese rectifier and diode manufacturer, recorded NT\$482 million in revenues for the first nine months of 1985, a 40 percent decline from the same period last year. Total revenues for the year are expected to be NT\$600 million, with profits of NT\$60 million.

#### PRODUCT

Hitachi Announces High-End Model of 6305 Series

NEC Develops CMOS 8-Bit MCU

NEC to Ship V40 and V50 MPUs

Tokyo Sanyo Develops Ultrasmall Hybrid ICs Hitachi Ltd. has developed a new model of the 6305 series of CMOS 8-bit microcontrollers, the 2TAT, and will begin sample shipment on December 20. The new device, numbered the HD637052, is the highest-end model of the 6305 series, and has a built-in A/D converter of 8-bit x 8 channels and a dual-port RAM. It is available in three clock frequencies: 1 MHz, 1.5 MHz, and 2 MHz. Sample prices are ¥3,200 (\$15.53) to ¥3,600 (\$17.48) per unit.

NEC Corporation has developed a CMOS 8-bit, single-chip microcontroller, the uPD78312, and will put it on the market in December. The newly developed device is equipped with a 16-bit ALU and a register. The production plan is 50,000 units monthly in early 1986, reaching a total of 200,000 units in fiscal 1986. It will be priced at ¥2,000 (\$9.71) per unit for 10,000-unit orders.

NEC Corporation has announced development of the V40 and V50 MPUs, which are included in the company's V series of original CMOS micro devices. Sample shipment will begin in December. Sample prices are ¥8,000 (\$38.83) per unit for the V40 and ¥10,000 (\$48.54) per unit for the V50. Monthly production will initially be 50,000 units, and will be increased to 100,000 units during 1986.

Tokyo Sanyo Electric Co., Ltd., has developed three models of ultrasmall car audio hybrid ICs. The models are the STK3400A and 3400B, which are multiplex stereo decoders equipped with FM noise cancellers, and the STK 3600, a 5-band graphic equalizer. Monthly production is targeted at 500,000 units up to the end of 1986. Sample shipment began in November. The STD 3400A/B is priced at ¥600 (\$2.91) per unit and the STK 3600 at ¥300 (\$1.46) per unit.

Toshiba to Market CMOS LSIs for Multibus II Toshiba Corporation has begun marketing two models of CMOS LSIs for Multibus II interface. Toshiba has commercialized the LSIs under a second-source contract with Intel Corp. of the United States. The models are the BAC84110 for bus control and the MIC84120 for interruption control. Both models are for parallel systems. Sample price is ¥30,000 (\$146) per kit. Production is planned at several hundred thousand units per month during 1986.

#### EQUIPMENT AND MATERIALS

Semiconductor Manufacturing Equipment Makers Face Tough 1986

Applied Materials President Meets with the Press While semiconductor demand is expected to recover in early 1986, the severe situation for semiconductor manufacturing equipment makers will likely continue through late next year or into 1987. Since major semiconductor manufacturers have decided to shrink their capital expenditure plans for the current fiscal year by close to 30 percent, semiconductor manufacturing equipment makers are receiving 30 percent to 40 percent fewer orders than last year. Even if semiconductor demand recovers as expected, orders for manufacturing equipment are not likely to come until late 1986 or early 1987. This means that the first half of the next year will be the most difficult time for semiconductor manufacturing equipment makers.

James C. Morgan, president of Applied Materials Inc. of the United States, recently held a press interview in Tokyo. He stated that:

- Applied Materials Japan's sales in the previous fiscal year, which ended in October, totaled ¥12.959 billion (\$63 million), up 4 percent over the year before.
- The company will begin production of CVD equipment at its technology center in Japan in late January 1986.
- New models of CMOS epitaxial growth equipment and CVD equipment will be shipped in 1986.

Tokyo Electron's Profits Expected to Drop by Half

Sumitomo Electric Develops New IC Package Substrate

Sumitomo Metal to Market Semiconductor Manufacturing Equipment

XMR Diffusion Equipment to be Marketed in Japan The company previously announced that each year, one of its four board meetings will be held in Japan. The first meeting in Japan will be in December of this year.

Due to the sluggish demand for semiconductor manufacturing equipment, Tokyo Electron Ltd.'s sales and profits in the current fiscal year, which will end in September 1986, are expected to show a decline. Operating profits in the year are anticipated to total ¥10 billion (\$49 million), nearly 50 percent lower than what was expected in the previous year. The company's total sales are estimated to total some ¥130 billion (\$63 million), down 10 percent from the original plan.

Sumitomo Electric Industries, Ltd. has developed a nitride aluminum ceramic to be used as a package substrate material for ICs. The thermal conductivity of the newly developed ceramic is 10 times higher than that of alumina and the thermal expansivity is about the same as that of silicon. Therefore, a large-size silicon chip can be placed directly on the substrate. The new material is expected to accelerate the development of supercomputers. Sample shipment of the ceramic will begin in spring of 1986.

Sumitomo Metal Mining Co., Ltd., recently developed a semiconductor manufacturing machine capable of 4Mb DRAM production, and placed it on the market on November 1. The equipment can draw 0.2-micron circuit patterns by employing electron cyclotron resonance (ECR) technology. The company hopes to sell about 100 units annually in three years.

XMR Corp. of the United States has developed diffusion equipment for semiconductor production using excimer lasers. The company has made an agreement with Mitsui & Co., Ltd., to market the equipment in Japan starting in March 1986. Mitsui's sales target of XMR products in the initial year is ¥100 million (\$485,000), which will be increased to ¥1 billion (\$4.85 million) in three years.

#### TECHNOLOGY

Gallium Arsenide Activities in Japan The following table shows the activities of the main Japanese companies in the gallium arsenide area.

### ACTIVITIES OF MAJOR JAPANESE COMPANIES IN GAAS TECHNOLOGIES

Сотралу	Materials	IC Devices	GHz Systems	Lasers	Optical Processors	Piber- optic LANs
Pujitsu	Yes	Yes	Yes		Yes	Yes
Hitachi		Yes	Yes	Yes	Yes	Yes
Matsushita		Yes	Yes	Yes	Yes	Yes
Mitsubishi		Yes	Yes	Yes		Yes
NEC		Yes	Yes	Yes	Yes	
NTT		Yes			Yes	
Sharp		Yes	Yes	Yes	Yes	
Sony		Yes		Yes	Yes	
Sumi tomo	Yes	Yes		Yes		
Toshiba		Yes	Yes	Yes	Yes	Yes

Source: DATAQUEST December 1985

Hitachi Shelves Trench-Type Capacitor for 1Mb DRAM Hitachi Ltd. has decided not to employ trench-type capacitor structure in 1Mb DRAMs for the time being. The company believes that conventional planar capacitors are superior to the trench type in regard to production efficiency. Hitachi's decision leaves NEC Corporation as the only 1Mb DRAM maker that uses the trench capacitor. Hitachi plans to begin sample shipment of its 1Mb DRAM this month.

#### OTHERS

Personal Computer Demand Decreases Demand for personal computers has been declining rapidly. Domestic (Japanese) shipments in fiscal 1985, which will end in March 1986, are expected to total ¥370 billion (\$1.8 billion), ¥70 billion (\$340 million) lower than the initial forecast by the Japan Electronic Industry Development Association (JEIDA). The decrease in demand for personal computers is largely due to the rapid spread of low-price word processors. Word processor production in Japan in the current fiscal year is expected to reach 750,000 units, four times as many as that in fiscal 1984. On the other hand, shipments of 8-bit personal computers for home use have dropped 20 percent compared with the year before.

ComputerLand Names New Japan President

EIAJ Compiles Southeast Asian Electronics Industry Report ComputerLand Japan Ltd. has appointed Kris Tamaki as new president as of November 5. Mr. Tamaki, a Sansei (third-generation Japanese-American), was dispatched to Japan by ComputerLand's U.S. neadquarters in September 1984. Shoichi Yokoyama, former president, has retired and will act as an adviser to the company.

The Electronics Industries Association of Japan (EIAJ) has compiled a research report by the 1985 Southeast Asia Electronics Industry Research Mission. It was the eighth research mission dispatched to the Southeast Asian area. The report says that the electronics industry in the area is not as advanced as was expected. Details include:

## 1985 PRODUCTION FORECAST (Thousands of Units)

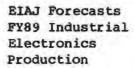
	Singapore	Hong Kong	Taiwan	South Rorea
Television (Black and White)	30		1,380	4,100
Color Television	3,840	900	2,000	4,400
VTR	-	4-	384	1,100
Audio	18,700	19,900	18,800	19,000
Telephone	1,020	6,300	1,680	5,000
Personal Computer	2,900	2,580	2,500	2,800
Calculator	1.5	6,120	18,000	2,400
Watch	-	10,900	4	5,000
Television Game	G <u>€</u>	1,200	-	500
Microwave Oven	960		4.	2,000

Source: EIAJ

# FORECAST OF EACH COUNTRY'S ELECTRONIC INDUSTRY PRODUCTION INDEX (1984 = 100)

		Singapore	Hong Kong	Taiwan	South Korea
June	1985	80	70	78	85
1985	Total	80	65	75	85
1986	Porecast	85	60	70	100

Source: EIAJ



The EIAJ recently compiled a forecast of the industrial electronics business in Japan. It reports that the business is expected to reach \$11,341.3 billion (\$55 billion) in fiscal 1989. The average annual increase is forecast at 12.4 percent. The details of the forecast are:

#### FORECAST INDUSTRIAL ELECTRONICS PRODUCTION IN JAPAN

		1989	Percent Growth from 1988	Total Percent Growth from 1984-1989	CAGR 1984-1989
Industrial Electronics	¥	11,341.3	11.78	80%	12.4%
Wired Telecommunication		1,798.9	6.6%	50%	8.58
Equipment Wireless Telecommunication		21,2012	4.00		4110
	¥	912.7	9.58	498	8.3%
Equipment		89.5	7.8%	50%	8.5%
Broadcasting Equipment	¥			47%	8.08
Wireless Telecom Unit	*	542.7	9.5%	25.6	
Wireless Applied Unit	¥	280.5	10.0%	548	9.0%
Electronics Applied					
Equipment	¥	6,975.3	13.48	95%	14.3%
Computer and Related					
Equipment	¥	6,000.0	14.18	100%	14.98
Except Computer	¥	975.3	9.28	68%	11.0%
Electronic Measuring					
Instrument	¥	975.7	12.88	78%	12.2%
Business Machine	¥	678.7	10.18	76%	11.98
Word Processor	¥	252.0	14.5%	177%	22.6%

Source: EIAJ

Update on the 1986 JSIS Conference in Hakone, Japan, April 13-15: Featured speakers will include Dr. Tsugio Makimoto, Deputy General Manager, Hitachi Ltd.; and Don Brooks, President of Fairchild Camera and Instrument. Call (408) 971-9010 for more information. I.C. ASIA is a news digest published semimonthly by DATAQUEST's Japanese Semiconductor Industry Service (JSIS). To order a one-year subscription (22 issues), mail your check or money order for \$430 to:

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Compiled by DATAQUEST's

Japanese Semiconductor Industry Service



11/22/85

I.C. USA 1985-7

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#### INDUSTRY

U.S. Capital Spending Declines DATAQUEST believes that capital spending by U.S. semiconductor firms will decline 23.8 percent in 1985. The table below shows our estimates for the major U.S. companies.

# CAPITAL SPENDING BY MAJOR U.S. SEMICONDUCTOR MANUFACTURERS

			Percent Change
Company	1984	1985	1984-1985
AMD	237	198	(16.5%)
AMI	38	30	(20.0%)
Fairchild	195	170	(12.8%)
Intel	388	275	(29.1%)
Mostek	123	62	(50.0%)
Motorola	412	330	(20.0%)
National	300	242	(19.3%)
Signetics	133	65	(51.1%)
Texas Instruments	\$ 472	\$ 348	(26.3%)
Others	753	604	(19.8%)
Total	\$3,051	\$2,324	(23.8%)

Source: DATAQUEST

Motorola and Intel in DRAM Shakeout Intel has withdrawn from the DRAM market completely and Motorola has announced that it will stop making 64K DRAMs. This news came only one week after Texas Instruments set a distributor price floor of 90 cents for 64K DRAMs. Prices have generally been 60 to 70 cents since last summer. Motorola and Intel have both reported losses recently. Intel's second quarter, \$23 million operating loss was its first in 15 years. The question: Will TI follow Intel and Motorola's lead and get out of the DRAM market?

Senators Want More Access to Japanese Technology U.S. Senate members want American firms to have regular access to Japanese scientific and technical information. They want the amount currently available to be expanded. They have called for the Commerce Department to spend \$1 million for collection and translation of documents and to coordinate dissemination of the information.

The proposed Commerce Department group would:

- Prepare annual reports on important Japanese technical developments
- Assist professional societies and private business groups to gather, translate, and distribute the technical literature
- Publish an annual directory of private and government collection/translation services

The legislation is sponsored by Senators Jay Rockefeller of West Virginia and Max Baucus of Montana.

SRC May Use Capital Reserves The Semiconductor Research Corp. (SRC) uses funding from 35 member companies to support cooperative research projects. However, income has been cut as member companies' sales and purchases have declined due to the slump. Ninety percent of the SRC's income is devoted to supporting university-level semiconductor research. To avoid cutting research funds, the SRC may dip into its capital reserves next year. The SRC is supporting projects in 0.25-micron CMOS, GaAs, semiconductor design, and semiconductor manufacturing.

#### FROM CAPITOL HILL

U.S.-Japan Sectoral Discussions

EPROM Dumping Case Passes First Hurdle

Is There a U.S. EPROM Industry?

Administration Will Initiate 256K DRAM Dumping Case A report summarizing the status of the bilateral market-oriented, sector-specific (MOSS) talks has been jointly issued by the United States and Japan. These talks cover several electronics sectors, including telecommunications and medical equipment. The joint statement claimed "important progress," but the U.S. electronics industry is highly skeptical of this claim--especially on the further liberalization of various telecommunications markets.

The EPROM dumping case filed by AMD, Intel, and National Semiconductor against eight Japanese EPROM producers has passed its first hurdle. The International Trade Commission made a preliminary finding that the U.S. EPROM producers are being injured by Japanese imports. This is the first step in the sequence, which ultimately could lead to dumping duties being imposed on the Japanese companies. The action next shifts over to the Commerce Department for its preliminary evaluation of the extent of dumping. The American companies allege that the Japanese have been selling 256K EPROMs for \$4, while it costs them more than \$6 to build them.

At the International Trade Commission hearing on EPROMS, the lawyers for the Japanese side claimed that because U.S. firms assemble EPROMS outside the United States, there is no U.S. EPROM industry. Japanese companies also allege that U.S. firms sell product in Japan at less than production cost. Both claims are likely to fall on deaf ears in Washington. The first argument is seen as a legal ploy to circumvent U.S. trade laws. The second allegation has not been supported by any evidence.

For the first time, the U.S. administration will self-initiate a dumping case, probably covering all high-density DRAMs. With the initiation of this case, essentially all DRAMs would come under a dumping investigation. The administration expects this action to yield a number of benefits. First, it would demonstrate to Congress that the administration's newly created trade "strike force" is taking substantive actions to deal with unfair trade actions. Second, it is expected to pressure the Japanese into dealing effectively with the 301 case. The Japanese have recently initiated a proposed

settlement directly with the affected U.S. companies. DATAQUEST believes, however, that the U.S. companies will hold out for what they perceive as badly needed U.S. government action.

"Strike Force" May Cause Friction

One factor that could adversely influence the U.S. administration's effectiveness in dealing with semiconductor trade issues is the growing friction between the Office of the Special Trade Representative and the Department of Commerce. This problem surfaced when President Reagan gave Secretary of Commerce Malcolm Baldridge the responsibility of overseeing the administration's trade strike force. As DATAOUEST anticipated, the friction is growing as the strike force's recommendations begin to take shape and the U.S. trade representative sees its turf getting infringed upon. The new 256K dumping case will give the Commerce Department a substantive role in any negotiations on semiconductors, but the U.S. trade representative actually objected to the initiation of the case, anticipating the problems it would create. The U.S. trade representative has sought to keep the two cases separate.

DATAQUEST Reviews Dumping Procedure

Because several semiconductor dumping cases have been initiated, and with the potential for more in the future, DATAQUEST is reviewing the procedure. There are two separate parts to a dumping investigation; a determination of injury and a determination on the extent of dumping, if any. The International Trade Commission makes the injury determination, while the Commerce Department handles the determination of dumping margins. The schedule for these cases is fairly tightly dictated by U.S. law. Most cases take 290 days to complete, with delays granted for extraordinary circumstances if a case is complex. The ITC first makes a preliminary injury determination 45 days after a complaint is filed. If a favorable determination is made, the Commerce Department then takes several months to estimate the preliminary dumping margins. The matter then enters the last phase, with the final determination of dumping margins by the Commerce Department and a final determination by the International Trade Commission on injury. The dumping law and its past applications do not fit well with the fast-paced nature of the semiconductor industry. DATAQUEST expects that the U.S. semiconductor industry may soon seek changes in the law.

#### COMPANY

National, Linear Tech Patent Suit May be Split

General Electric Licenses Silicon Compilers System

Silicon Compilers Signs with General Dynamics

Gould AMI Signs Pact with Seattle Silicon National Semiconductor Corp. will ask the U.S. District Court to split a nine-patent suit into two cases, with National's patent infringement charges to be heard first. Linear Technology's countersuit charging patent misuse and antitrust violations would wait until the validity of the patents is determined. National claims that a third-party expert determined that Linear was using National trade secrets. Linear claims that the license fee and royalty requested for use of the patented technology was "discriminatory and anticompetitive."

General Electric's Custom Integrated Circuit (CIC)
department has agreed to use Silicon Compilers
Inc.'s Genesil system in its design centers in
San Jose, California, and Research Triangle Park,
North Carolina. General Electric's CIC department
is concerned with application-specific ICs. Silicon
Compilers has agreed to similar arrangements with
Gould AMI Semiconductors, International
Microelectronics Products, NCR, and VLSI
Technology, Inc.

Silicon Compilers has signed a \$1 million, three-year technical assistance agreement with General Dynamics for the application of silicon compilation to the design of VLSI semiconductors for General Dynamics' military and aerospace programs. In return, General Dynamics will assist Silicon Compilers in furthering its knowledge of Department of Defense IC design requirements and defense contracts. In addition, General Dynamics invested \$4.2 million in Silicon Compilers, obtaining a 5 percent interest in the company.

Gould AMI Semiconductors has signed an agreement with Seattle Silicon Technology to provide systems manufacturers with a simplified means of designing ASICs and transferring final design data to Gould AMI for fabrication. By the agreement, Gould AMI has provided Seattle Silicon with its proprietary geometric design rules and the performance characteristics of selected fabrication processes. Seattle Silicon has incorporated the data into its Concorde VLSI compiler software system for use on a variety of CAD workstations.

Cirrus Logic and AMD to Exchange Silicon Compiler Technology Cirrus Logic and Advanced Micro Devices have signed an agreement to exchange information on silicon compiler technology. Under the agreement, Cirrus Logic will design a CMOS evaluation device for AMD in exchange for 1.6-micron double metal CMOS wafers. Cirrus plans to complete the design for the Am29ClO microcontroller by the end of this year. AMD will evaluate Cirrus Logic's compiler technology with the Am29ClO. Cirrus Logic will obtain the rights to sell the controller as a module within more complex logic ASIC products.

NCR Expands Standard Cell Capabilities

NCR has enlisted two independent design centers to expand its standard cell IC capabilities. Micronix Integrated Systems of Laguna Hills, California, covers the Southern California region, and Electronic Technology of Cedar Rapids, Iowa, will serve the midwest. NCR has enlarged its standard cell program to include production of military and other hi-rel ICs. The firm will offer its devices over the military temperature range with MIL-STD-883C, Class B, Method 5004 screening.

ZyMOS Capital Purchase Offer Withdrawn

Penn Central Corp. and Hambrecht & Quist will not purchase Intermedics' 47 percent share of 2yMOS Corporation of San Jose, California. The investment would have brought needed capital into 2yMOS and into Exel Microelectronics, which Penn Central and H&Q were reportedly negotiating to acquire along with the stake in 2yMOS. Exel said the withdrawal has had a serious effect, and layoffs have since been announced. ZyMOS said that its make-or-break crisis passed with last spring's 30 percent staff reduction, and the deal's collapse will not have serious consequences. ZyMOS was planning to acquire Exel to add EEPROM cells to its library and introduce IBM PC AT-compatible standard product circuits.

Seeq and Atmel in Lawsuit; Seeq Objections Upheld

A Superior Court judge has upheld an objection raised by Seeq Technology Corp. and removed some parts of Atmel Corp.'s lawsuit charging wire—tapping and invasion of privacy. Seeq did not succeed in having a paragraph removed from the suit charging it with "bad faith." The suits started last spring when Seeq charged Atmel's founder with theft of trade secrets and employees when he left Seeq. The two companies also disagree over which trade secrets should be kept sealed during the trial. General Instruments (GI), which provided

Atmel with seed money and facilities in Chandler, Arizona, is planning to take an active role in the suit. Seeq does not want GI to have access to certain documents.

Sun Microsystems of Mountain View, California, will supply workstations to Toshiba Corp. of Japan over the next five years. The contract is valued at \$5 million. The workstations will be used for mechanical and electrical CAD. Toshiba may also configure Sun workstations for OEM production. Sun has also signed a technology-sharing agreement with Toshiba and will have access to a Japanese version of UNIX.

Siltec Corp. of Menlo Park, California, has licensed wafer technology to Lucky Advanced Materials Inc., a subsidiary of the Korean Lucky-Goldstar group. L-G is one of South Korea's largest industrial conglomerates and has recently become involved in the worldwide semiconductor business. Siltec will receive \$4 million in cash and royalties based on future sales volume. A Korean site for a facility handling 6-inch wafers and producing 20 million square inches a year will be announced soon. The plant is expected to be operational within 12 months. Lucky-Goldstar will not be part of a joint venture or take an equity position in Siltec, which has licensed technology to Rhone-Poulenc (France) and Toyo Soda (Japan).

Texet Semiconductor of Allen, Texas, has filed for Chapter 11 protection. Most operations have been suspended for two weeks. A cash squeeze from slow sales leaves Texet with \$3.3 million in assets and \$12 million in liabilities. The company said it is discussing additional funding with several venture capital groups.

ABM Semiconductor of San Jose, California, has received an unspecified amount of capital from Kodenshi Corp. of Japan. Kodenshi is now represented on ABM's board of directors by president Hirokazu Nakajima. ABM will market the roughly 200 optoelectronics products produced by the Japanese company. These standard products will complement ABM's custom work.

Toshiba and Sun Microsystems Agree on Workstations

Siltec Wafer Technology Licensed to Lucky

Texet Semiconductor Bankrupt

Kodenshi Provides Cash to ABM Companies Hard Hit by Industry Recession As a result of the prolonged industry downturn, many semiconductor manufacturers are posting losses, some, like AMD and Intel, for the first time in many years. Siliconix, a participant in the nonvolatile, steadily growing industrial linear IC market, and VLSI Technology, Inc., a maker of ASICs, are two bright spots on an otherwise bleak scene.

#### QUARTERLY REVENUES OF SELECTED SEMICONDUCTOR COMPANIES (Millions of Dollars)

Company	Most Recent Quarter	Sales	Net Earnings	Net Profit Margin
AMD	2 (9/30)	\$ 128.100	(\$15.275)	( 11.9%)
Intel	3 (9/30)	\$ 311.741	(\$ 3.600)	( 1.2%)
Micron Technology	4 (8/31)	\$ 6.200	(\$ 7.300)	(117.7%)
Motorola	3 (9/30)	\$1,380.000	(\$37.000)	( 2.8%)
National	1 (9/20)	\$ 423.400	(\$53.500)	( 12.6%)
Siliconix	3 (9/15)	\$ 26.300	\$ 2.300	8.78
VLSI Technology	3 (9/30)	\$ 20.049	\$ 0.022	0.1%
Xicor	3 (9/12)	\$ 7.027	(\$11.113)	(158.1%)

Source: DATAQUEST

More Layoffs and Shutdowns Announced The table below shows recently announced semiconductor-related pay cuts, layoffs, and shutdowns.

Company	Pay Cut	Layoff	Shutdown
AMD			10 days at Christmas
Intel	4 to 8%		6 days at
			Christmas
Motorola	5 to 10%	150-200	
SEH America		185	
Ultratech Stepper		75	

Source: DATAQUEST

Fairchild to Sell Headquarters and Plants Complex Pairchild Camera & Instrument Corp. has decided to sell its entire 546,000-square-foot, four-building headquarters and manufacturing complex in Mountain View, California. The asking price is not yet available. Fairchild, a subsidiary of Schlumberger, recently announced that it was moving its headquarters from the Mountain View site to a 55,000-square-foot facility in Cupertino, California.

#### PRODUCTS

"Transputer" from Inmos

Fairchild Introduces "Clipper"

Update on Chips & Technologies

New Raytheon Semicustom Linear Offering Inmos is beginning a push into microprocessors with its new, reduced instruction set, the Model IMS T414 Transputer, which uses its Occam operating system. The transputer has been under beta testing for some time. The IMS T414 integrates a 10 MIPS 32-bit microprocessor, four interprocessor links, 2 Kbytes of static RAM, 32-bit memory interface, and memory controller. It is made with double-metal, twin-well CMOS, with 1.5-micron channel widths. Boards, available immediately, have 64-Kbyte, 1-Mbyte, or 4-Mbyte memory. The price of the T414 is \$500 in 100-unit quantities.

Pairchild Camera & Instrument has introduced its Clipper CMOS 32-bit RISC as a three-chip UNIX supervisory module. General samples of the \$2,541 chip set are expected by June. Speed is 5 MIPS for the double-metal, 2-micron CMOS chips.

Founded in January 1985, Chips & Technologies of Milpitas, California, provides integrated semiconductor solutions for microcomputer companies, initially focusing on the PC AT. Integrated chip sets allow quick addition of graphics, LANs, and microperipheral systems logic. The ASIC-standard CHIPSet is 100 percent compatible with IBM's enhanced graphics adapter (EGA) card. C&T is working on additional 80286-based and next-generation 80386 CHIPSets. The PC AT CHIPSet replaces 25 ICs with four devices. Video 7, Inc. of Milpitas has developed an all-in-one IBM PC graphics card using C&T's EGA kit. The \$599 card would replace \$1,500 worth of separate boards. C&T is subcontracting with Toshiba and Fujitsu for the CMOS and bipolar arrays used in its ASIC solutions.

Raytheon has developed a semicustom analog IC to replace entire PCBs. The RLA 120 replaces networks of resistors, transistors, and differential gain blocks configured as op amps and comparators. The user specifies interconnections. The RLA120 is fabricated using a proprietary dual-metal bipolar process. The bottom layer incorporates architectural and structural components and power buses. The top layer is factory-customized to the desired configuration. Completed circuits can be made in 24-pin DIPs or leadless chip carrier packages. Turnaround time is six to eight weeks with \$17,000 to \$24,000 charged for nonrecurring engineering. Unit prices range from \$8 to \$12.

VTI Introduces CMOS PLDs VLSI Technology Inc. has introduced a low-cost, high-speed, mask-programmable HCMOS logic chip. The devices—the VP16RP8M and VP16RP8M-25—are compatible with 20-pin HAL and PAL devices. The chips have 25ns propagation times and use just one-quarter of the power of a standard bipolar chip. The chip is a semicustom logic array using custom metal mask programming. Pricing in quantities of more than 5,000 ranges from \$1.90 to \$2.50.

VTI Announces Digital Signal Processors VLSI Technology Inc. has announced two CMOS
16 x 16-bit parallel multiplier-accumulators. The
VL2010 is a CMOS pin-compatible replacement for the
AMD 29501 and TRW TDC1010J. The VL2044 is identical
except the preload function is eliminated. The
chips are fabricated with 2-micron CMOS technology.
Samples in a 64-pin CERDIP are available. Plastic
DIP and PLCC packages will be available next year.

ZyMOS Adds Cell to Analog Library ZyMOS Corp. has added a third linear cell kit part, 2y40117, to its analog library, offering a dual-supply A-D converter, single-supply comparator, single- and dual-supply DACs, and single-supply op amp in one package. The 2y40117 is available as a 40-pin DIP prototyping tool.

CMOS Filters Announced by Linear Technology Linear Technology Corp. of Milpitas, California, is offering CMOS universal switched-capacitor filters in single, dual, and triple versions. Center frequency is tunable up to 40 kHz. The LTC1059, LTC1060, and LTC1061 have center frequency accuracy of ± 0.8 percent and Q accurate to 5 percent. "A" versions take accuracy to ± 0.3 percent and 3 percent on Q. Prices range from \$3.25 to \$8.25 in 100-lot quantities.

LSI Logic Corp. Introduces New Logic Arrays LSI Logic Corp. of Milpitas, California, has brought the company's dual-layer HCMOS down to 1.5-micron features with the LL9000 series of logic arrays. Software support is available immediately for the eight new chips at ten design centers worldwide. The company says that there is a 30 percent premium over 2-micron prices, with a 25 percent performance gain. Pin counts up to 224 are available in plastic and ceramic packages.

Maxim Adds to Up/Down Counter Family

D-to-A Converter from Analog Devices

Mitsubishi Announces Gate Arrays

Intel Introduces New Chip Maxim Integrated Products of Sunnyvale, California, now has four presettable 4-digit up-down counters with LED drivers. All versions contain a comparison value latch, 4-digit magnitude comparator with equal output, zero detector, counter preset circuit, and display latch. Signals up to 5 MHz can be counted. Versions are available for common anode LEDs (300mA) and common cathode LEDs (50mA).

Analog Devices Inc. of Norwood, Massachusetts, has introduced a CMOS quad 8-bit DAC with separate reference inputs for each DAC, and a triple 8-bit DAC with three on-board video converters and ECL RAM look-up tables. The AD 7225 24-pin DAC operates with dual (+11.4V to +16.5V) or single (14.25V to 15.75V) power supplies. Applications are: sine/cosine generation, digital word multiplication, AC signal attenuation, filtering, and summing polynomial terms. The HDL3805/3806 triple DAC is made for raster scan graphics, television video reconstruction, digital VCOs, analytical instrumentation, and other critical applications.

Mitsubishi Electronics America of Sunnyvale,
California, has entered the semicustom market with
2- and 3-micron CMOS gate arrays. Up to 4,800 gates
are available in 3-micron, and up to 8,000 in
2-micron. The gates are made using a double-metal,
poly-gate process. The M300 series consists of ten
3-micron array packages. The first two 2-micron
families, the M60018/19, will be available in
nine-package types within two months. Daisy,
Mentor, and Valid workstations provide support.

Intel has introduced a new 32-bit microprocessor, the 80386 or iAPX386, which can process about twice as much information as the current one and work with more than 4 billion bits of information or about 2,000 typewritten pages. However, at this point, few tasks actually require the power of the new chip, so the market may be slow to take off. Last year, only \$1 million worth of 32-bit MPUs were sold. DATAQUEST has predicted sales of only \$10 million this year. Nevertheless, the market is expected to grow to \$200 million by 1990, with related 32-bit microperipheral and microcontroller chips adding up to \$1 billion to that figure.

5-MIPS Multiprocessor Family from Intel Intel Corp. has extended its 80286 MPU line with a new multiprocessor family at 5 MIPS. The family is based on a new 286/310 AP series, a single processor using the 8-MHz 80286, which offers up to 80 percent more performance than the old 6-MHz version. The Apex multiprocessor supports up to four 8-MHz 286 MPUs within the chassis, and up to 16 users. The system holds up to 9MB of memory, 40 or 140MB of disk storage, 60MB of tape backup, 80287 numeric coprocessor, 320KB diskette and 2 to 18 serial I/O channels. The entry-level, 8-user system is priced at \$11,200 each for 50 or more OEM units. An upgrade for the earlier 286/310 costs \$4,995.

Zilog Super8 Microcontroller Released Zilog's new high-performance, 8-bit, Super8 microcontroller was recently released and is based on the Z8 MCU. Clock rate is 12 MHz, with an increase to 20 MHz expected. The Super8 has an onchip DMA controller, more UART functions, more instructions, and doubled register file. User-defined special macrocode functions take advantage of the Forth language. Super8 architecture is said to reduce code by as much as 30 percent over the 8051. The chip is a 2-micron NMOS part made by the Z4 process. Later versions will appear in CMOS. The first chip in the Super8 family is priced at \$10 each in quantities of 10,000 or more, and is a ROM-less, plastic 48-pin DIP chip.

AMD Introduces New Processor Advanced Micro Devices is now producing the Am7970 CCITT Group 3/facsimile-standard compression/expansion processor in volume. It can handle bit-mapped graphics, drawings, sketches, foreign alphabets, and Chinese and Kanji characters. Throughput is 2 to 8 Mbps. DMA is on-chip; there is a local document store bus and a CPU bus for 8086 tie-in. One hundred-lot quantities of 68-pin ceramic LCC are currently available at \$245 each.

#### TECHNOLOGY

DSP Compiler Developed at University of Edinburgh A research team at the University of Edinburgh in Scotland has developed a silicon compiler that allows digital signal processing multichip VLSI systems to be designed automatically in less than a month. The new silicon compiler, FIRST (Fast Implementation of Realtime Signal Transforms) compiler system, automatically synthesizes complex silicon systems from high-level functional

specifications. The multichip VLSI systems have applications in fifth-generation computing systems involving speech, vision, graphics, telecommunications, radar, and sonar. The new compiler is an extension of the team's work on silicon compilers for gate array chips, which led to a spin-off commercial company, Lattice Logic, in Edinburgh.

Current Logic Load Outstrips Today's CAE Tools The manager of IBM's System Technology division, Peter Bottorff, warns that the logic design of current automated design tools is barely adequate for today's design tasks, despite the increase in the number and type of workstations. Immense package densities demand tools with more power. CAE workstations and PCs lack the storage needed for the 500,000-plus elements typical today. He is concerned about interface problems between current workstations and large computers. He also warned buyers that it may take as long as two years for design software to be debugged.

New BiCMOS Processes from Motorola and Hitachi

Motorola and Hitachi each addressed BiCMOS processes at the recent IEEE International Conference on Computer Design. Motorola says it can make 1.5-micron BiCMOS processes yield 6,000-gate logic arrays comparable to dense CMOS. Hitachi claims to have a BiCMOS 64K SRAM with 15ns address time. The approach is expected to become popular for very high-speed VLSI. BiCMOS circuits are effective high-current output drivers, and can be used internally to enhance VLSI. CMOS circuits are buffered from loading and ECL compatibility is easier. The 1.5-micron process requires 14 masks. Hitachi has added the speed from bipolar to highdensity, low-power CMOS SRAMs. The technology will also be applied to ECL interface RAMs to reduce power consumption.

Mark your calendar now for the 1986 Japanese Semiconductor Industry Conference, April 13-15, at the beautiful Hakone Prince Hotel in Hakone, Japan. I.C. USA is a news digest published semimonthly by DATAQUEST's Japanese Semiconductor Industry Service (JSIS). To order a one-year subscription (22 issues), mail your check or money order for \$430 to:

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PCs--HOW MUCH CAN THEY REALLY DO?

Terry A. Zimmerman Vice President of Marketing FutureNet Corporation

Mr. Zimmerman is Vice President of Marketing at FutureNet Corporation, where he is responsible for product and corporate strategic marketing. He has more than 20 years of industry experience and previously held domestic and international marketing posts with several computer and high-technology firms including General Signal Corporation, Pertec Computer Corporation, Litton Industries, and North American Rockwell Corporation. Mr. Zimmerman received a B.S.E.E. degree from California State Polytechnic University and has done graduate work in Marketing and Business Administration.

+ How fast is FAST?

\*\* POPULE 911 THUNG the Kids to school

\* Too much capability

\* WHY do CAE CUSTOMENS BUY?

WANT TO IMPROVE Productivity

\* " SMANT GOIF"

SYSTEM A SYSTEM BY
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Dataquest Incorporated
DESIGN AUTOMATION FOCUS CONFERENCE
December 9 and 10, 1985
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SOFTWARE: THE REAL IC DESIGNER

Peter Whyte
Vice President of Strategic Development
E-CAD Incorporated

Mr. Whyte is Vice President of Strategic Development for E-CAD Incorporated. He was a founder and President of SIMON Software Inc. prior to the merger of E-CAD and SIMON in February 1985. Both companies are authors and marketers of application software for IC design. Previously, Mr. Whyte was Vice President of New Product Development at Atari, Inc., and head of mergers and acquisitions at Wells Fargo Bank. He has also served at the board level for Staveley Industries in the United Kingdom, and was responsible for Staveley's United States interests. Mr. Whyte received a B.S. degree from Leeds University in England and an M.A. degree in Business Administration, also from Leeds University.

PARALLEL ARCHITECTURES

- ARE YOU WILLING TO UNBUNDEE ,

OPPINIZE YOUR SEN FOR PARALLEL

MACHINES ON WILL YOU REQUIRE

YOUR HUNTO PROVIDE CONTIER

TELHNOLOGY

ESAC'S \* EXPERT SOFTWARE Application Companies

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DESIGN AUTOMATION FOCUS CONFERENCE
December 9 and 10, 1985
Palo Alto, California

# ECAD SYSTEM \$ HW 40% 0/5 10% APP SW 50%

# SOFTWARE THE REAL I.C. DESIGNER Petg: Whyte, ECAD, Inc.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 1 \*

During this talk I would like to accomplish two things:

I would like to demonstate that to keep up with the evering need for increased size and complexity in I.C. design, we have no alternative but to look to software for the power and functionality we need

And along the way I would like to make a case for the greater recognition of the contribution of Application Software concanges to the continued development of Electronic CAD.

\* Right at the beginning I would like to bring to your attention the Design Dilemma, which will come up at various points in the talk.

#### ################### COMP POWER SLIDE ####################

\* For the sake of clarity, I would like to <u>pefine some of the terms</u> I will be using, stanting with EDAD.

#### \*\*\*\*\*\*\*\*\*\*\*\*\*\*

- \* Some people use the name <u>ECAD</u> to describe electronic CAD, and at ECAD inc. we like to encourage that line of thought, you can probably understand why.
- \* So throughout the talk I will be using <u>Electronic DAD</u> to refer to the market and  $\overline{\text{EDAD}}$  to refer to the company.
- \* I would also like to avoid any distinctions between Electronic CAD and Electronic CAE . For the purposes of this talk I am going to use <u>Electronic CAD</u> to refer to the <u>gomplete design and verification blocks</u>; including all the steps between concept and mask.
- \* Most of the remarks refer to the <u>custom and semiroustom</u> I.C. market, although they obviously tie in to considerations in the <u>system and P.C.B.</u> markets.

#### 

\* Next, a definition of <u>productivity</u>. This conference is on the question of productivity and maybe by the end of the sessions we will all understand what it means in our industry. I don't want to second gives anybody and so I'm going to concentrate on a fairly narrow definition, that nevertheless is meaningful in the part of the industry in which we operate. ---- <u>PRODUCTIVITY IS EQUIYATENT</u> TO SUPPLIENT OF The Productive of the concentrate.

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\* This definition of productivity is from the point of view of the user, who is obviously very important. However there is another way of cafining productivity which is important to DAD vencors, and by implication also to the customer.

#### 

- \* Let me introduce you to  $\underline{D}_{C_1, D} = \underline{D}_{C_2, D} = \underline{D}_{C} = \underline{D}_{$
- \* Finally, in terms of definitions, I would like to commerc on what constitutes software in this context. Clearly we are talking about programs that combine expert knowledge of the processes involved with excellence in software engineering. These factors are complimentary. At ECAD, for example, almost all our development staff have a background in the Electronics industry first, and in software engineering second.

#### \*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE IC des + soft eng \*\*\*\*\*

- I wondered what level to pitch this talk at, and I asked <u>Dataquest</u> for their opinion. They said well there are going to be <u>GGD\_\_Yendows</u>. I.C. <u>Yendows</u>. <u>Yendows</u>. <u>Yendows</u>. <u>Yendows</u>. <u>Yendows</u>. and <u>financial analysts</u> in the audience, a pretty mixed bunch, so why bon't you pitch it at a level that we at Dataquest will understand? Right there I stopped talking, because I knew that whatever I said next would be misconstrued. ———So its somewhat beneral.
- \* <u>Considerable research however</u>, has been put into some of the conclusions reached here, and if any of you would like to discuss any of them in greater detail I will be happy to do so after the presentation.

#### \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 2 REPEAT \*\*\*\*\*\*\*\*\*

- \* Doming to the first subject, Software productivity:
- \* In the past, software has been too often regarded as an according to bardware. This next slide demonstrates the way that some people have viewed software.

#### \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE SA LIFEBELT \*\*\*\*\*\*

\* However, by the end of my talk here I hope to convince you that the proper way to look at it is as shown on the next slice, here....

#### \*\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 55 USS ENTERPRISE \*\*\*\*\*

- \* When IBT says that 90% of its profits in the 90%s will come from software, and  $\underline{Daisy}$  opens out its anonitecture to outside hardware, and the majority of the added value of every system sold is in the software, then maybe the  $\underline{time\ nas\ come\ for\ us\ to\ take\ this\ thing\ seriously}$ .
- \* To Dataquest's credit they are wrestling with the very difficult problems of definition, for example how to deal with applications software bundled on a workstation, and we are delighted to be of assistance in helping them to come up with a <u>more representative picture</u>.
- The reason I bring this up is that this increasing part of the market, that is Applications Software, is in our opinion, absolutley the place where the greatest advances in Electronic CAD productivity are going to be made, and, most interestingly, it is also the least captive part of the system and getting more so every day. This has got very significant marketing ramifications for us all.
- In particular it raises some interesting questions about how and where the end user is going to buy the software, e.g. is the a trend transfer one stop shopping and a complete solution, or is the most recent trend in fact in the other direction, whereby customers are assembling a suite of tools from various sources that best match their needs?
- \* I know that some of you in the audience are wondering <u>how real are</u> these <u>Appileations software companies</u>. How far can they go and how big can they grow? As I hope to show the answers to these are a long way and a lot bigger than they are now.

#### \*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 7 KEY SOFT CO CONSIDS\*

\* Now, looking at the Electronic CAD market through the <u>eyes\_of\_a software\_company</u>, the things which are <u>important</u> are:

Design Methodology Computational Complexity Compatibility Harware platforms

\* Looking now at each of these in turn:

#### \*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 8 METHODOLOGIES \*\*\*\*\*

- \* METHODOLOGY All important. There are certain <u>components common to several or all the design methodologies</u> where algorithmic breakthroughs are needed to advance design productivity.
- \* For example on of the biggest needs of current <u>silicon combilers</u> is for an <u>efficient compactor</u>, able to handle a variety of shapes and sizes. Such a compactor would also be of great benefit to automated layout of custom circuits and to cell generation for use in semi-dustom design.

- \* Similarly all methocologies need an answer to the problem of  $\underline{t}\underline{e}\underline{g}\underline{t}\underline{g}$  years generation in particular, and to  $\underline{t}\underline{e}\underline{g}\underline{t}\underline{g}\underline{b}\underline{i}\underline{l}\underline{i}\underline{t}\underline{y}$  in general.
- At ECAD we believe the solution will come from solving the most difficult companies of the problem independently, and to provide compatible modules that the designer can use to design in today's environment, not in some mythical environment of tomorrow. The today of tomorrow will come from solving these difficult, fundamental contract or problems and internating the solutions into already existing design metadogless. The problem is not amenable to an instant "contract solution". Nor does it make sense to try and change the way designers design.
- \* There are centain market dynamics at work that suggest the <u>Experienced</u> designers who know what they're doing are the ones who will <u>determine what they're doing are the ones who will determine wethorology eventually becomes cominant.</u>
- \* We do not subscribe to the theory of the <u>phantom army of 200,000</u>, or was it 300,000 no its 400,000 system designers being the major market influence. They will end up being a major market, but the influencers and the <u>pateway to the winning design methodologies</u> lie with the 3000 experienced IC designers.
- To give an example, I understand from Prof. Robrer at Carregie Mellon that there are <u>between 2000 and 3000 vax 780 on equivalents</u> engaged on <u>Circuit simulation</u> at any given time. Those designers are not going to give up all that fun in favor of a different design methodology until they know it works.
- \* Methocology and <u>computational\_complexity</u> often go hand in hand. Sometimes on is an attempt to dincumvent the other. The next slice shows one way of expressing computational complexity.

#### \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 9 TRIANGLE COMP COMPLX\*

- \* COMPUTATIONAL COMPLEXITY The reason there are no one step solutions is that before any automated design system can work there remain some fundamental computational proplems to be solved.
- \* Most of these relate to sheer numbers. A design that represents 50 modules or 200 blocks will end up representing 2 million polygons. Handling 200 blocks is beyond the ability of most automated systems now, and <u>handling 2 million polygons</u> in anything but the most structures of structured arrays is a pipedream.
- \* The areas where the computational complexity hits hardest are circuit simulation, reperation of fault test vectors and design verification. Other areas that still await new or improved algorithms are stick layout systems, automatic routing of any height any width cells, compaction of ladesigns, and automatic comparison and translation between various levels of design hierarchy.

#### \*\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 10 COMPATIBLITY \*\*\*\*

- \* COMPATIBILITY A proplem. What is there really to say about compatibility? I suppose I should say that most of the programs we produce at ECAD speak to each other, and that once or twice we have even got two pieces of hardware to talk to each other......sort of.
- \* In talking about compatibility I would like to extend that to <u>quarating</u> systems for a minute and make an observation about how reality cities from what we read and hear. AT EDAD we have about two purched installations of our software on mainframes or superminis, and that again or more on workstations, —— we con't sell on AD's. Of our cusic ers who have a choice, <u>95% are ruppoint vms in preference to unix</u>. The reason I have is to illustrate that developers of all kinds head to take account of what their customers are coing how and what their requirements are if they are to be successful.
- # HARDWARE PLATFORMS Examining now the melationship between hardware and software. In general it may appear that hardware provides objected and software provides application specific solutions. However, the divicing line is not always that clear:

#### \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 11 COMP POWER REPEAT

- \* Remembering now the <u>increase in speed</u> provided to the average Electronic CAD user by <u>hardware advances</u> over the last five years, this shows that the speed has increased by a factor of about 4.
- \* There have during this time been improvements in cost effectiveness, which are very important, but the net result is that improvements in hardware power have not done much to advance the cause of more productive Electronic CAD.
- \* Now I would like to <u>contrast</u> this with the improvemnts that have come from the development of <u>applications software</u>.
- \* Here I have to apologize for being <u>parochial</u> and referring to ESAD Incidata. I did ask our <u>competitors for comparative data</u> to use in this talk but for some reason they seemed reluctant to provide it.

#### \*\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 12 DRAC SPREED INC \*\*\*

- \* The graph shows that in a period of just over two years we have increased the speed of Dracula by over 250 times compared to the solution to design verification that was available before Dracula came along. We have done this by a program of constant algorithmic development starting with Dracula I, then Dracula II and, would you believe Dracula II.
- \* The last development is significant because it is a  $\frac{b_1 e_2 e_3 e_4 e_5}{601 ution}$ , and the development of more hierarchical solutions is  $\frac{b_1 e_2 e_3 e_4}{600 utions}$  about of Electronic CAD.

#### \*\*\*\*\*\* SLIDE 13 SIMON V SPICE \*\*\*\*

- \* Also, lets look at Spice, a venerable program in wide use, loved and hated in about equal amounts. Over the the last 15 years since WE last elegists thanched the program, the total speed up by hardware means as burnts to less than 10x if you discount supercomputers, and that indicate vectorizes and parallel vensions, which are really software activate bospinations.
- \* however, in the <u>MSS cigital gomain</u>, which is where the bulk of casigns are today, it is not neccessary to spend half a million on a rillion dollars on hardware to run spice. There are a number of new similations, not based on the traditional spice algorithms, that can perfor a much faster and in a more cost effective manner.
- \* Again my apologies for being parochial. I promise to give equal air time to any competitors who will send me their benchmarks. The graph of  $g_{1000}$   $g_{2000}$  against spice shows a speed up of up to  $g_{200}$  on circuits we can compare. Now I hasten to acc this is not on all circuits.
- \* However, their are two important points here; first if you want to stay on a vax you can run a 50,000 transistor circuit in the time it uses to take to run a 1000 transistor circuit, secondly the increase in the run time of this type of algorithm is approximately linear, whereas solde is at least a square law, therefore the potentials to simulate huge circuits or alternatively to optimize the design by repeated iteration both now exist.
- \* So it seems that, <u>in the past</u>, at least in two areas, productivity advances from software have totally <u>overtspadowed that from hardwale</u>. I would now like to turn to <u>the future</u> and look at what we might expect from from current developments in both hardware and software.
- First, a restatement of the problem. Currently we are pushing a million transistors on a chip. Data quest is forecasting <u>17 million</u> by 1990. There will be certain highly structured designs where compute power wont be a problem. However there is always going to be a part of the market that is pushing for more functionality, higher censities and more speed. In general this part will be at the forefront of development.

\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 185 RELATIVE COMP NEEDS \*

- \* This slipe gives us some idea of just how great the problem brulb get if we don't do something about it. <u>How do we solve this problem</u>?
- \* There are <u>three areas</u>, all of which are currently receiving attention.

New design methodologies Enute force it through hardware Develop new algorithms for existing design methodologies

- \* New\_lesian\_methodalogies\_app\_\_solut\_\_to\_\_provice\_sour\_relief. Sometay silicon combilers will really work and will allow the design of huge circuits. Standard cells and gate arrays seem to be having a much more immediate impact in the market place.
- Here I should add that at Edad we try to be independent of design methodologies. We sell through pretty well all of the work started demparies, our dustoner base splits fown about 50/50 between seni-duston and full duston, and we number 3 silicon compiler companies along our clients.
- \* Which even way we look at it however, in conemal <u>new membersuckiesies</u> have stoned be tied to new software developments and more computing nower because of the sheer size of the increases.
- \* Coming to <u>hardware</u>, there has been a lot of interest recently in accelerators, risc machines and parallel processors. Any EDAD watchers in the audience will be glad to know that this has not escaped our attention. In fact, for some time we have been nunning <u>benchmarks</u> with a variety of hardware to try to establish what the practical possibilities are.
- \* For obvious reasons I have to maintain confidentiality on this but I would like to share with you some of our findings as they relate to the productivity increases possible through the various hardware options.
- \* I should stress that we are dealing with <u>real CAD programs</u>, not academic benchmarks, and that the equipment congerned is cost effective in such a way as to present a viable alternative to the Electronic CAD user. (no Chay II's)

\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 15 HARDWARE OPTIONS \*\*

\* The <u>options</u> we considered are:

Super-mini
Microprocessor
Clustered super-minis
Risc Engines
Panallel microprocessors
Panallel risc engines
Vector processing
Super-computers
Solutions on Silicon

\* Coming to the <u>results</u> of our investigations:

\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 16 SPEED UP GEN PURPS \*

- \* The graph shows the results. This <u>first graph is for general purposes</u> <u>bardware</u> speed ups in Electronic CAD. There are a couple of areas where we can get greater speed ups of limited problem sets and I'll come to those later, on the second graph.
- \* The horizontal axis of the graph represents time, expressed as the next five years, and the vertical axis represents <u>computing power</u>, expressed in MIPS. These are <u>general purpose MIPS</u>, equivalent to those we believe

becale will actually see, not special purpose FIFD on  $m_{\pi}$  (special per second. For comparison, a Vax 780 is taken as one peneral purpose  $\pi$  ,  $\pi$ 

 $\star$  . On the graph there are three distinct areso in which the recode  $s_1$ 

One, in the Area of 15 to 20 MIPs provided by a completable. of <u>sarallel risc</u> engines.

Two, in the area of 5 to 10 MIPs, provided by galegies wichoptocessing, single miso engines on clustered CPuls.

Three, in the area of 2 to 4 MIP's, provided by <u>SIALLE ETLE</u> <u>On Microphocessors</u>.

- \* The <u>Maximum area of speeding</u> for practical purposes would be a <u>page</u> engine <u>Dased Dased Dasalel</u> <u>processor</u>, operating in the range <u>15-20-2550</u>. Done of the factors that will determine just where the figure will be alled the power of the basic risc engine, the number of processors that can be usefully applied in parallel, and the proportion of the abolication software that can take advantage of either risc or parallelism.
- \* As an example let me go through how I arrive at the 15-20 figure: This is based on the assumption that we are getting a speed of about 8 MIPS from the best rise engines running on the most suitable programs. The swe find that in a program like Draguia, which is inherently yery parallel, about 90% of the code is applicable to processing in parallel, of course has the effect of dictating that even if we reduce the time to run this % to zero the program will speed up a maximum of ten times.
- \* However, in the <u>real world</u> we are not going to be able to recade it to zero. By experiment we find that the <u>optimize reader of processors</u> is in the range  $\frac{4-to-9}{2}$ . Adding more processors after 9 coes not make ially increase run speed.
- Knowing this we can <u>gerive an equation</u> that will give us the expected pechease in run time, or alternatively the expected increase in MIPS.
- \* This is that the total run time is reduced to 10% of the original plus 90% divided by the number of processors, all of the second half of the equation further divided by the increased power of each rise processor.
- In figures this means that a run that originally took  $100 \, \mathrm{minutes}$  on a vax.  $780 \, \mathrm{now}$  takes 8 minutes with 4 processors, or 5 minutes with 9 processors. In terms of MIPS this gives 12 with 4 processors or 20 with 8 processors. All of this takes no account of losses incurred in coupling the processors.
- \* This for a highly specialized piece of hardware that probably canada coanything else but hun specific pieces of application software. Compare this with a <u>Vax 8600</u>, which at 4 mips is a multi-user, general purpose machine. It makes some of these general purpose machines not look so bac after all!
- \* Now with totally new software, structured for parallel processing from the word go it might be possible to best these. First the rost world

is not like that, ID designers have a god to do and they need bracktral tools to so it now, so for all practical purposes these figures are the limit to which we can expect help from handware in increasing procedulity in Electronic CAD.

්රිත්ත් විශ්කාව සහව සිටහිස් සුවුස්වුවට සුවුස්වල සිටුව වෙන්වෙන්න සිට වෙන්න සිටුව සි these in the next graph:

#### \* 165 SPECIAL PURPOSE SPEED UP

- \* Vector processing, super computers and solutions on silicol office <u>during</u> oppers of mainitude. However, for various reasons none of them set to offer <u>complete solution</u>s from an applications software point of thew.
- Vector processing requires <u>extensive poplification to the software</u>, a definite no-no, and it seems to have reached somewhat of a plateau as fer as current Electronic CAD programs go.
- Super computers, while obviously effective have <u>questions of cost</u> effectiveness attached to them.
- Solutions on silicon require that the alcorithms used be stable, and that the number of primatives used is manageable.
- Solutions on silicon. I nearly said silicon solutions, seem to be the most interesting of these, and I believe John Newking from Silicon Solutions will be talking about this next.
- So this means that hardware solutions are going to be limited to account one order of magnitude. This of course will just not be in any way adequate for the increase in compute power needed by the increase in direult size and complexituy.
- This just wont out the mustard when compared against either the needs of the market or the 250x historically from software, and it will not be meanly adequate to do the job.

#### \*\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE # ? SOLUTIONS TO COMP GAP REP \*

- Now I would like to look at the third area in which we huse look for improvements, namely the development of Software CAD tools.
- Not all areas of Electronic CAD will benefit, or need to perfit, edually from fiture cevelopment.

#### \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 185 COMP NEEDS REP \*\*\*\*\*

The front end, schematic capture etc., <u>doesn't really maid</u> & compute power problem, and it is possible that one ofcer of magnitude will suffice...

The logic and fault simulation levels have a ladim company problem but are partially ammiable to a fixer section. Silicon because of the low number of primitives they ceal with and the relative stability of the algorithms.

The back end of the process, circuit simulation are layout venification have a <u>large\_compute\_problem\_and\_associated</u> orders of magnitude more primitives to deal with and a social subject of rapid algorithmic development. They are not, in general amenable to fixed in silicon solutions.

- \* What this means is that in the worst problem areas we are going to have a compute gap of two and mayoe things occars of magnitude.
- Perversely, incheasing automation of the design process is not less to make thinking of putting any rand of antificial intelligence in theme, then we are more dependent than ever on new algorithms.
- \* The hardware limitation has some very <u>important connotations</u> for the Electronic CAD user that co <u>beyond mere speed</u>.

Firstly, to take advantage of the improvements offered, it is essential that <u>existing code can be run</u> on the systems with as fewer modifications as possible, preferably none.

Secondly, the systems integrators had better to all they can to make sure the special purpose handware transparent to the user.

Thirdly, software producers should make sure they deliver their products to market by the best means possible, which means marketing through a number of channels.

\* These points are important because there are a lot of software Electronic tools out them already, and users are not just going to throw them away. This indicates that the successful tools are going to be explutionary, rather than revolutionary, and that which even way we loo at it we are dependent on application software development.

#### \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE HAUND LAW #\*\*\*\*\*\*\*

- \* So far we have concentrated on speed. Now, referring bad- to bridgeng's Law, I would like to examine some of the areas of <u>functionality</u>. Functionality and speed are of course tied to one another, and abids to the software portion of the Law. Also tied in with functionality as a tomesolutions at component level, mentioned earlies, which indicades to methodology bast of the equalities.
- \* Budge Muster 而是不是了数型的等点的一句的一个单位一直可能通过更过的一直可能将来了的工作的不是了一个。

results that will benefit a number of design methodologies are, in dividuality the following:

\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 20 DEV AID ACDICTOTY \*

Sympolic compaction

Adonatic layout systems

Test vector generation

Mixec mode simulators

Analogue/digital circuit simulation

Thanslation programs between dienarchies

One cata base hierarchical systems

Compatible interfaces between programs

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE & REPER! TALK SULJ \*\*\*\*

- \* Now I would like to turn briefly to the second subject in the talk, their is the proper recognition of Application software companies.
- \* Overall, we have to develop an appreciation of application springs and expensive propagation of taxation and the areas of taxation and the financial communities. Nowacays it seems that everything has to have a synonym to make it catchy, and so I thought I would come up with the this:

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 21 ESACS \*\*\*\*\*\*\*\*\*

- \* ESAD's ---- Expent Software Applications pompagies, we come to see a lot more of these in the Electronic CAD market place.
- \* I thought of lots of ways of trying to <u>convince the aucience</u> here that software companies are for real, and I finally came up with a way to call that is to show you some of the <u>costs</u> of running one of these things

\*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 22 SOFTWARE COSTS \*\*\*\*

This next chart shows some of the evenual costs of a puece of spitual exerting of all fetime. As you can see maintenance accounts for a whospure great 67% of all costs over the life of the software. I have two comments on that, one I wish it wasn't thue, and two I wish we could charge the customer like that. Whosps, whatever happened to the idea that software was free after you had developed it.

\*\*\*\*\*\*\*\*\*\* SLIDE 55 COMPONENT SYS COST \*

To give you an idea of what I mean, lets take a look at a typical Electronic CAD "system". Simplistically I would allocate the components into MANDWARD. DELECTION SYSTEM SOCIAMBLE AND HAD ICATION STITUSES, with approximate proportions 40%, 10%, and 50%. Any harware vencors never I don't want to get into a discussion of how accurate these proportions are, except to say that a majority of the price of an electronic CAD system is concerned with application specific software.

#### \*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 23 RELATIVE SYS COSTSK

- \* Now lets look what is happening to the <u>nelative\_gosts\_of\_softwake\_in\_o</u> <u>system</u>. ---- By golly look at that, not only is it getting more expensive but there is going to be more ofit. maybe we had better start taking this stuff seriously.
- \* In summary, what are the implications of all this for productivity in Electropic CAD? Well they are these:

#### \*\*\*\*\*\*\*\*\*\*\*\*\*\* SLIDE 24 \*\*\*\*\*\*\*\*\*\*\*

At the <u>top\_design\_level\_IC</u> designers are going to assemble their <u>own\_suites\_of\_programs</u>. To get productivity they will choose the best post components. There is no one stop shop they can get all they need from one source.

Productivity will come from encosing the <u>best component</u> solutions at each level in the design hieranchy.

There will be a <u>hierarchy of hardware</u>, and all they software tools had better be prepared to run at all levels, subject to physical capacities.

Software will be a <u>bigger and bigger proportion</u> of the system cost. ( I like that one). This is already apparent on the microvax II.

Maintenance will become a bigger pant of the software cost.

Successful software will be that which wins first the <u>accepance of the 3000</u>, and the easiest way to co that is to allow then to use design methodologies they are comfortable with.

- \* We will see a certain amount of <u>encryption of alconithes on lesilicon</u>, along with <u>risc and parallel</u> architectures, but the <u>major increases</u> in Electronic CAD productivity will come <u>from new alconithes and software sevelopment</u>.
- \* Finally, I would like to share with you the somewhat startling conclusion we came to during the look we took at the different architectures. You will remember we looked at....

..... et noteulonge ed?





#### FITTING IN APPLICATION ACCELERATORS

John Newkirk Chief Executive Officer Silicon Solutions Corporation

Mr. Newkirk is Chief Executive Officer and founder of Silicon Solutions Corporation. Before founding Silicon Solutions, he was an Assistant Professor of Electrical Engineering at Stanford University, where he and Vice President of Engineering Robert Mathews established and taught the graduate VLSI design course. Prior to that, he did consulting work for several high-technology companies including Hewlett-Packard and Xerox Corporation. Mr. Newkirk received M.S. and Ph.D. degrees in Electrical Engineering from Stanford University and a B.S.E.E. degree from the Massachusetts Institute of Technology. He is the author of numerous technical papers.

Dataquest Incorporated
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December 9 and 10, 1985
Palo Alto, California



#### OUTLINE

- WHO NEEDS SPEED?
- TECHNOLOGY ALTERNATIVES
- ACCELERATOR EVOLUTION
- A FEW MODELS AND METRICS
- AN APPROACH TO CAE/CAD ACCELERATORS

SILICON

#### WHO NEEDS SIMULATION SPEED

'What is your key bottleneck in IC Design?'

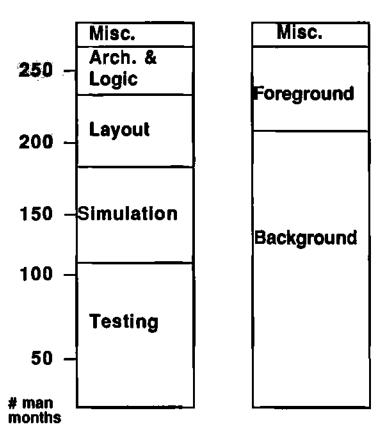
	<1	1-10	10-25	25-50	50+
1-2		Sim Spd		Sim Spd	
3-10	PG	Sim Spd		Sim Spd Compl Spd: (Zycad)	Sim Spd
10-25	Spice (Linear)	Sim Spd (DML)	Sim Spd	Sim Spd Sim Spd Sim Spd	Sim Spd
IC Designs Per Year 25+	Reliability	Spice (GaAs)	Sim Spd	1	i i

Size of Design (000s of transistors)

Source: Strategic, Inc Survey



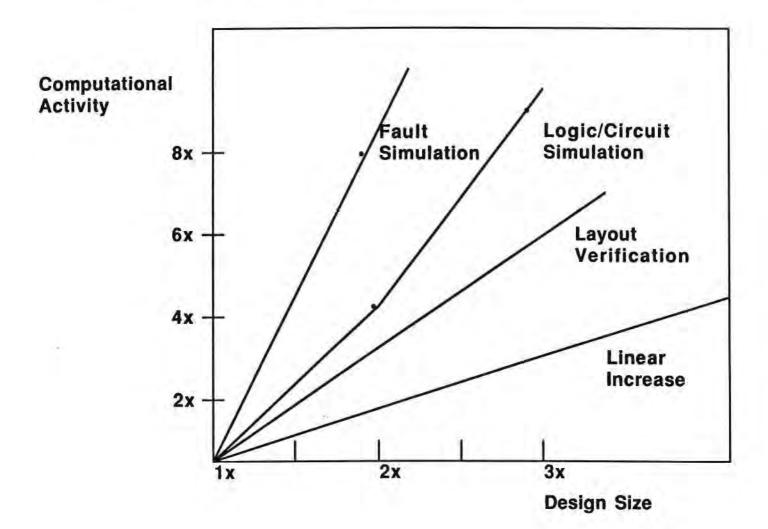
#### CASE HISTORY OF AN IC DESIGN



-45,000 transistor chip
-Graphics-based CAD system plus mainframe

Source: Industry Data

#### **DESIGN STEP COMPLEXITY**





#### TACKLING HEAVY COMPUTATIONAL LOADS

#### VIRTUES OF GENERAL-PURPOSE MACHINES:

- -Multiple applications
- -Programmable
- -Upgradeable and portable
- -Timeshared/many users

#### APPLICATION ACCELERATORS EMPHASIZE:

- Performance
- Low cost per equivalent CPU cycle



#### **ACCELERATION EVOLUTION**

#### **ARCHITECTURE ALTERNATIVES**

- -Parallel processing independent processes
  - design verification
- -Vector processing pipelining circuit simulation
- -Dedicated hardware -raw horsepower
  - · logic/fault simulation



#### **EVALUATING ACCELERATORS**

- COMPARISON AGAINST "GENERAL PURPOSE" HARDWARE OFTEN MISLEADING
  - -Both are dedicated processors
- SIMPLISTIC COMPARISONS EQUALLY UNACCEPTABLE
  - -Key issue: Throughput and Productivity

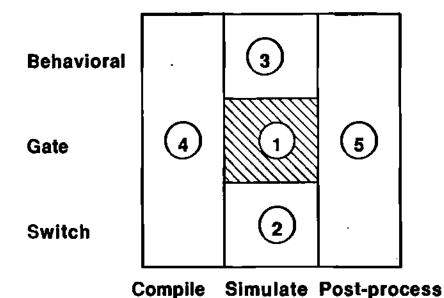


#### **EVALUATING ACCELERATORS**

- USEFUL METRIC SIMULATION RUNS PER HOUR
  - Pre and post-processing time
  - Computational intensity
  - Gate, Fault, Behavioral, Modeler mix
  - I/O Intensity
- OTHER METRICS
  - -Ease of use
  - -Accessibility in multi-user environment



# EVOLUTION OF SIMULATION ACCELERATION LOGIC SIMULATION



- 1. Point Acceleration of Gate Level
- 2. Addition of Switch Level
- 3. Enabling Behavioral Simulation in Accelerator Environment
- 4. Addressing compile bottleneck
- 5. Accelerating post-processing



#### A MODEL OF SIMULATION ACCELERATION

#### Impact of Accelerating Gate-Level Simulation

(7P( = GENTERME Purpuse Computer

	Logic Simulation		Fault Simulation		
•	GPC	ACC	GPC	ACC	
Compile	12▶0*	1 <del>2-</del> →0*	12	12	
Simulate	86	-	4300**	43**	
Post-Process	<u>2</u> 100—▶88	<u>2</u> 1 <del>4→2</del>	4314	<u>2</u> 57	
Speed vs GPC		7-44x		76x	

<sup>\*</sup> Repeat runs

<sup>\*\*</sup> Conservative estimate



### A MODEL OF SIMULATION ACCELERATION

Impact of Accelerating Whole Process

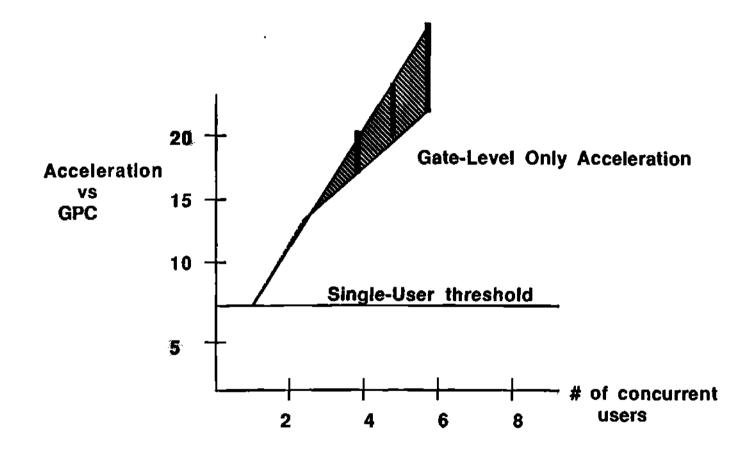
	<u>GPC</u> :	Accelerate Simulation
Compile	12	12
Simulate*	86	-
Post-Process	2	
	100	14
Speed vs GPC		7x

Accelerate Compile	
1	
-	
3	
33x	

\* short run

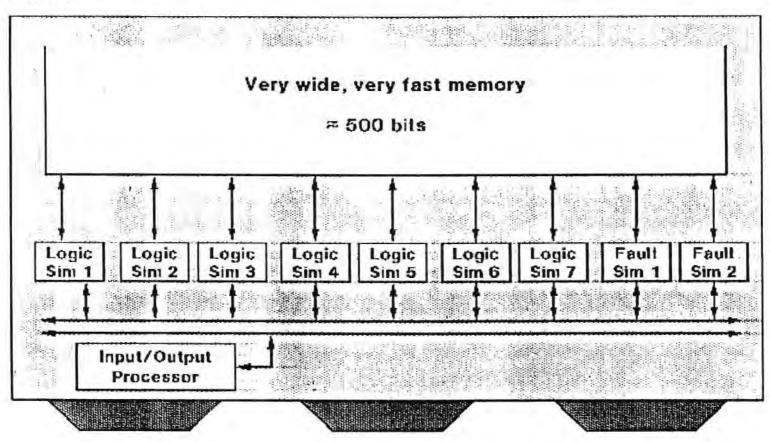


# A MODEL OF SIMULATION ACCELERATION Multi-User Environment

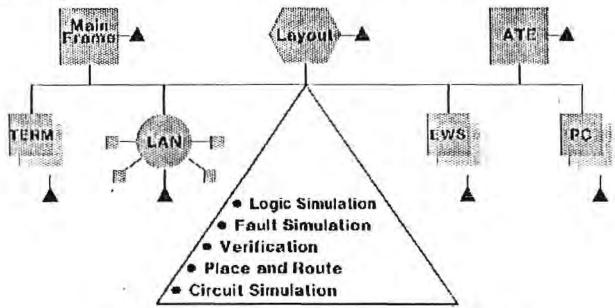


# SILICON

#### **ACCELERATION BOARD**



#### CAE PRODUCT STRATEGY



A FAMILY OF ACCELERATORS CONFIGURED TO SUIT THE NEEDS OF THE MARKETPLACE SILICON SOLUTIONS

# SUMMARY (FEELS MECHANICAL SOLUTIONS (AN BE ADDRESSED IN THE SAME MANNER)

• APPLICATION ACCELERATORS:

A long-term solution

• EVOLUTIONARY PATH:

End-to-end solutions
Tuned architectures

Network resources

• KEY CUSTOMER NEEDS:

Tight Integration

Transparency

Price/performance

· SOLUTION:

A modular approach





#### LINKING DESIGN IN TEST

Jeff Hotchkiss
Manager, Design and Test Automation Group
Teradyne Incorporated

Mr. Hotchkiss is Manager of the Design and Test Automation Group at Teradyne Incorporated. The Design and Test Automation Group is a new business unit that he was instrumental in starting in early 1984. Previously, he worked in a variety of sales and marketing positions at Teradyne. Mr. Hotchkiss received a B.S. degree from Bucknell University in Pennsylvania and an M.B.A. degree from the Sloan School of the Massachusetts Institute of Technology.

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Palo Alto, California

NEGATIVE IMPACT ON LIFE CYCLE PROFITS CAUSINBY: TIME TO MANKET 30% AFTER TAX PETURN Source Mckinnsey & Co.

DEBIGN TEAM A DESIGN SHIP

- B FINISHES EMPLUEN EVEN WITH A LATTER

PROTOTYPE BECAUSE TEST WAS INCLUDEDING

THE PROTOTYPH'S PROCESS

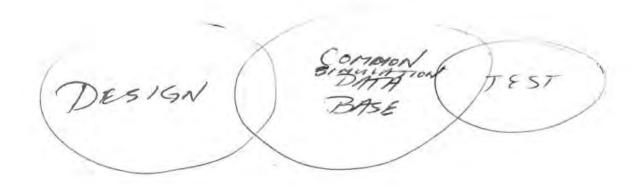
- JAPAN HAS BAEN QUICK TO REMITE

THIS

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- AMERICAN COMPANIES TYPICARLY MEASURE
AN ENGINEER'S PRODUCTIVITY THAN THE
PROPUCTIVITY STAGE AND NOT THAN
THE TEST STAGE







THE GOLDEN EGG -- ARE WE STILL CHASING IT?

Stephen E. Coit
General Partner
Merrill, Pickard, Anderson & Eyre

Mr. Coit is a General Partner of Merrill, Pickard, Anderson, & Eyre, a venture capital partnership located in Palo Alto, California. He was previously Vice President of Marketing at Raster Technologies, Inc. Earlier, Mr. Coit was Director of International Market Development at Prime Computer, Inc., and a Product Manager at Hewlett-Packard. He is currently a director of Graphics Software Systems and Raster Technologies, Inc. Mr. Coit received an A.B. degree in Applied Mathematics from Harvard University, and an M.B.A. from Harvard Business School.

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## - MANKET ANALOGY - OIL INDUSTRY

- MANY COMPANIES (SMAIL) PONING
HOURS IN THE GROUPD. THEY

(OME UP EMPTY, BIG COMPANIES

WATT TANZING THE "EMPTY HOLES"

OF YOUNG COMPANIES AS WHERE

MOT TO GO. THE DIFFORMATION

LEARNED IS CHEAR.

WHAT CONSTITUTES A MAMILET

I A MARKET THAT A SALESMAN CAN

LASILY IDENTIFY AND FIND PROSPECTS"

THE RESELLER - CASE D

"ON SAIE NOW"

- BUT WHY HAVEN'T THE END-USEILS

BOYGHT TILL' NOW

DESIGN.

INTEGRATION

SINTEGRATION

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#### MERRILL, PICKARD, ANDERSON & BYRE

TWO PALO ALTO SQUARE SUITE 425 PALO ALTO, CALIFORNIA 94306 TELEPHONE: (415) 856-8880

THE GOLDEN EGG--ARE WE STILL CHASING IT?

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# The Venture Cycle - The Boom





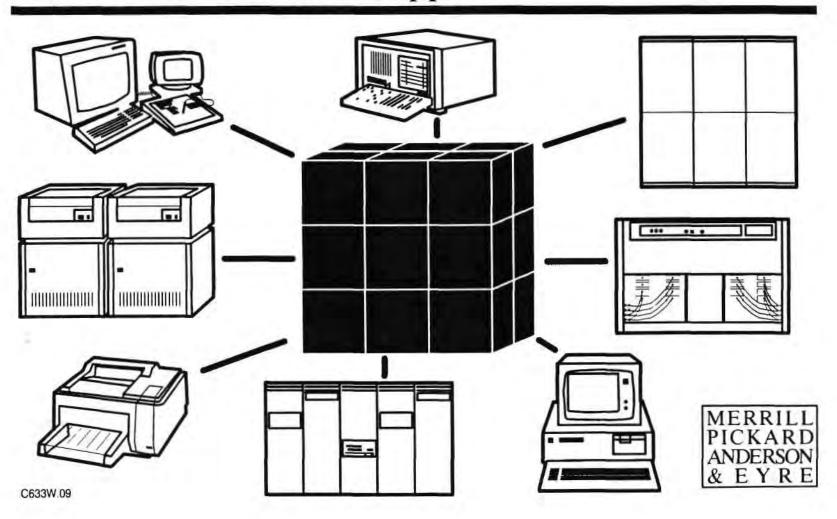
# The Venture Cycle - The Bust



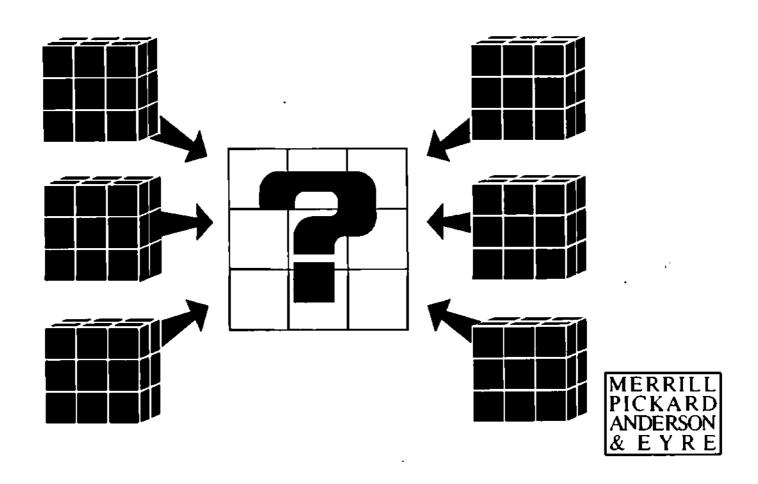


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# Case A: The Full Line Supplier

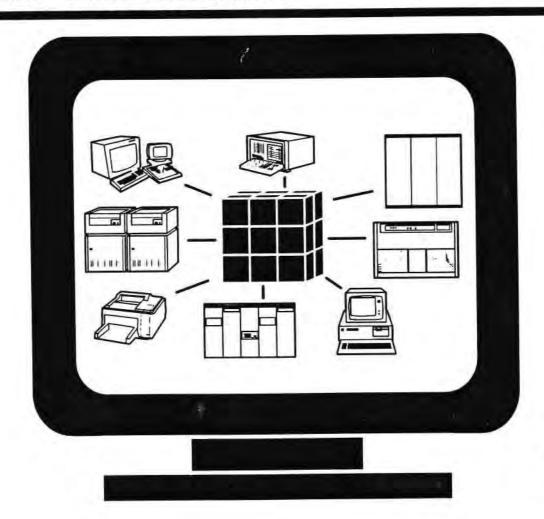


# Case B: The Integrator



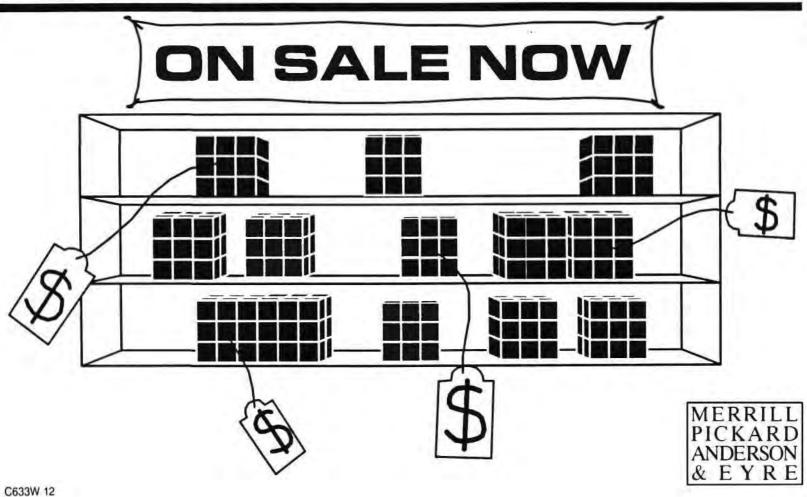
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# Case C: The User Interfacer

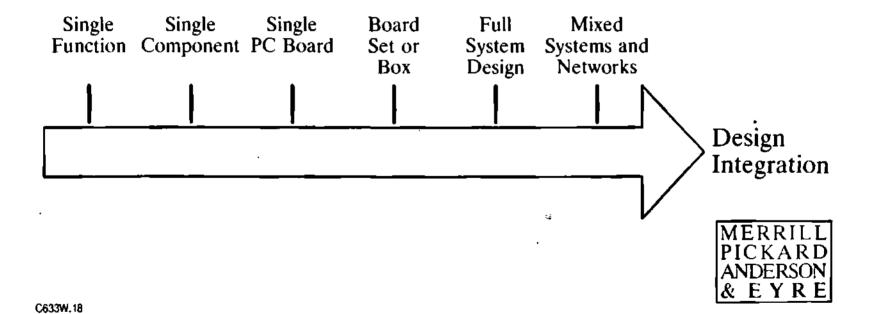


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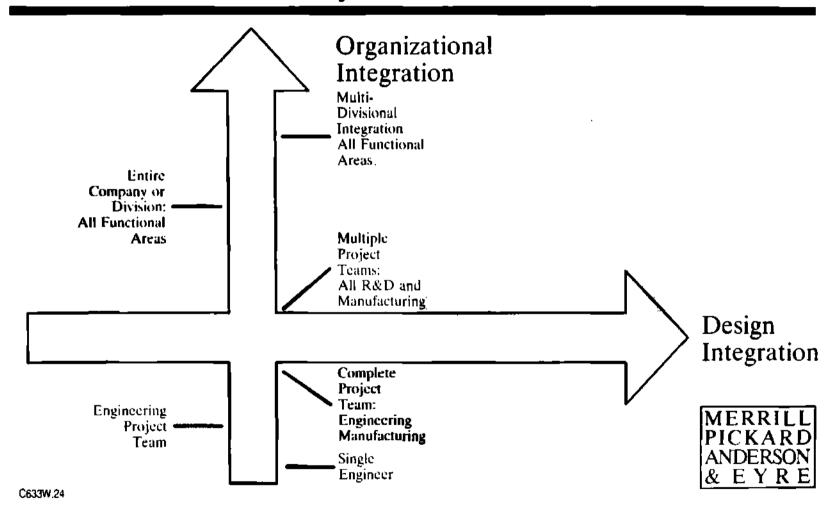
Case D: The Reseller

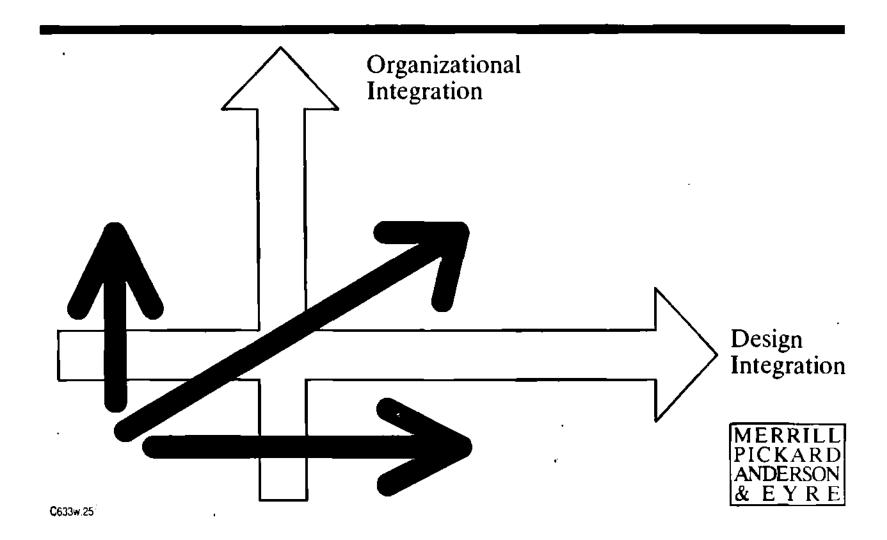


# **CAE Market Maturity**



## CAE Market Maturity





#### Common Pitfalls

- Underestimating Competitive and Economic Barriers to Entry
- Focusing on Technologies and Products, Not Markets
- Misdefining a "Market"



### Identifying New Venture Opportunities in "The Productivity Age"

- One-Upmanship Is the Riskiest Game of All
- There is No Substitute for Familiarity with a Specific Market
- Always Consider Exploiting New Technologies as a User



# MERRILL PICKARD ANDERSON & EYRE





Dataquest Incorporated
A Subsidiary of A.C. Nielsen Company

1290 Ridder Park Drive San Jose, California 95131

408/971-9000 / Telex 171973

THE PCB CONNECTION

Buck Feltman
Vice President of Marketing
Cadnetix Corporation

Mr. Peltman joined Cadnetix as Vice President of Marketing in October 1983. Prior to joining Cadnetix, Mr. Feltman was employed by Texas Instruments, Inc., where he was Marketing Manager for the Semicustom Integrated Circuits Division and Manager of New Business Development. Mr. Feltman received a B.S. degree in Electrical Engineering from Auburn College and an M.B.A. degree from Rollins College in Florida.

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#### DEVELOPING AN OPEN NETWORK FOR IC DESIGN

Bruce R. Bourbon Vice President of Marketing Gould AMI Semiconductors

Mr. Bourbon is Vice President of Marketing for Gould AMI Semiconductors. He is responsible for all strategic, tactical, and military marketing activities related to both standard products and application-specific integrated circuits (ASICs), as well as silicon foundry services. Before joining Gould, he was employed by Rockwell International's Electronics Group, where he held various manangement positions. Prior to that, he worked for Macrodata Corporation as Director of Software Engineering. Mr. Bourbon received a B.S.E.E. degree from California Polytechnic State University in Pomona and an M.S.E.E. degree from the University of California at Los Angeles.

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# DEVELOPING AN OPEN NETWORK FOR ASIC DESIGN BRUCE R. BOURBON, VICE PRESIDENT - MARKETING GOULD AMI SEMICONDUCTORS

#### (SLIDE 1)

I WOULD LIKE TO EXPRESS MY APPRECIATION AT BEING INVITED TO
ADDRESS SUCH A DISTINGUISHED AUDIENCE. I SAY THAT FOR TWO
REASONS: FIRST, I HAVE HAD THE OPPORTUNITY TO WORK WITH SOME OF
YOU INDIVIDUALLY AS OUR COMPANIES HAVE FORGED AGREEMENTS, AND SO
I PERSONALLY KNOW OF YOUR ACCOMPLISHMENTS IN PLACING IC DESIGN
TOOLS WITHIN REACH OF VIRTUALLY EVERY SYSTEMS DESIGNER. SECOND,
I AM PLEASED BECAUSE IT IS YOUR AREA OF BUSINESS THAT IS LEADING
ALL OF US INTO THE PUTURE. BY THE WAY, I HOPE THOSE PURISTS IN
THE AUDIENCE WILL BEAR WITH ME WHEN I USE THE GENERIC TERM "CAD"
-- IT'S A LOT EASIER TO SAY THAN CAE & CAD VENDORS!

#### (SLIDE 2)

NO DOUBT, AS WE SIT HERE TODAY, IN MANY WAYS IT'S A GLOOMY SCENARIO. THE PAST 12 MONTHS HAVE BEEN TOUGH WITH EACH DAY (SLIDE 2A) SEEMING TO OPEN WITH A PEW MORE DARK CLOUDS ON THE HORIZON. THERE HAVE BEEN MANY COMPARISONS BETWEEN THIS YEAR'S DOWNTURN AND THE LAST SLUMP IN 1981. ONE COMMENT THAT HAS BEEN MADE OFTEN BY SOME INDUSTRY FORTUNE TELLERS IS THAT, WHILE BUSINESS WAS DEAD IN 1981, (SLIDE 2B) IC MANUPACTURERS COULD STILL SEE THE PROVERBIAL GLOW ON THE HORIZON.

(SLIDE 2C) THAT IS, THEY COULD PREDICT THE SPECIFIC PRODUCTS THAT WOULD ONCE AGAIN BRING ABOUT HIGH DEMAND FOR CHIPS AND FUEL THE RESURGENCE OF SALES. (SLIDE 2D) THIS TIME — THE AUGURS SAY — THERE ARE NO PRODUCTS ON THE HORIZON TO LEAD US ALL OUT OF THIS SLUMP. THIS APPARENT REDUCTION IN ELECTRONIC PRODUCT INNOVATION ALONG WITH INTENSE PRESSURE FROM JAPAN, CERTAINLY HAS PUT A DAMPER ON SPIRITS, NOT TO MENTION SALES DOLLARS. IN JULY, WE LOOKED TO SEPTEMBER AND THE HOPE OF SOME ASTOUNDING NEW ELECTRONIC CHRISTMAS PRODUCT. (SLIDE 2E) UNFORTUNATELY, IT LOOKS LIKE CABBAGE PATCH KIDS AND OTHER DOLLS ARE STILL IN VOGUE — AND THERE ARE NO CHIPS IN THEIR STUFFING.

(SLIDE 2F) WELL, DESPITE ALL OF THE DOOM AND GLOOM PREDICTED BY INDUSTRY FORTUNE TELLERS WHO SAY THIS DOWNTURN IS THE ULTIMATE PIT WITH NO PRODUCTS ON THE HORIZON TO LEAD US OUT OF THE SLUMP, WE AT GOULD AMI TAKE EXCEPTION TO THAT PICTURE. THE DOWNTURN IS SEVERE -- BUT IT IS DIFFERENT. (SLIDE 2G) WHILE MAJOR END PRODUCT INNOVATIONS OR NEW IC PRODUCTS MAY NOT LEAD US OUT, THERE'S ONE DRAMATIC EVOLUTION TAKING PLACE WHICH WILL DO THAT.

WHAT WILL LEAD US OUT IS NOT A STANDARD PRODUCT -- LIKE
MICROPROCESSORS, 1-MEGABIT DRAMS, GRAPHICS CONTROLLER CHIPS, OR
EVEN DIGITAL SIGNAL PROCESSORS -- (SLIDE 2H) BUT RATHER THE
TECHNOLOGY PRODUCTS THAT YOU AS CAD VENDORS HAVE BEEN INVENTING,
PRODUCING AND ENHANCING ALONE AND IN CONJUNCTION WITH
APPLICATION-SPECIFIC IC - OR ASIC VENDORS.

IN FACT, IN MANY WAYS, LOOKING AT OUR ASIC AND CAE SEGMENT,
PERHAPS WE ARE NOT EVEN SO MUCH IN A DOWNTURN. (SLIDE 3) THE
GROWTH WE SEE HERE WOULD CERTAINLY TEND TO INDICATE THIS. (SLIDE
4) AND BY 1990, WE SEE CONTINUED GREAT OPPORTUNITIES. PERHAPS
WE ARE REALLY IN A PERIOD OF MAJOR TRANSITION WHEN MANY
TECHNOLOGIES ARE EMERGING WHICH (SLIDE 5) WILL RESHAPE THE ENTIRE
IC INDUSTRY AND THE WAY THAT CONCEPTS BECOME CHIPS. AND YOUR
INDUSTRY IS ONE OF THE MAJOR FORCES SCULPTING THE SHAPE OF THINGS
TO COME.

WHAT SPECIFIC AREAS ARE SHAPING THE CHANGES? AS STATED, (SLIDE 6A) CAD HARDWARE AND SOFTWARE TOOLS; (SLIDE 6B) NETWORKS SUCH AS ETHERNET THAT LINK A MYRIAD OF HARDWARE TOOLS PERFORMING THE SAME, SIMILAR AND DIFFERENT FUNCTIONS LIKE PIECES IN A JIGSAW PUZZLE; (SLIDE 6C) INTERFACE STANDARDS LIKE EDIF (ELECTRONIC DESIGN INTERFACE FORMAT) THAT BLEND SOFTWARE CAPABILITIES DEVELOPED BY COMPANIES INTERNALLY AND THOSE PURCHASED COMMERCIALLY; (SLIDE 6D) AND ASICS THAT CAN CONSOLIDATE BOARDS OF CHIPS INTO ONE SMALL, NEAT PACKAGE.

THE IC INDUSTRY HAS ALWAYS HAD AS ITS UNWRITTEN MOTTO, (SLIDE 7A)

"FASTER, (SLIDE 7B) CHEAPER, (SLIDE 7C) SMALLER." THOSE OF US IN

ASIC HAVE TAKEN THAT MOTTO LITERALLY AND DEVELOPED CHIPS THAT

REPLECT SYSTEM USE RATHER THAN INDIVIDUAL COMPONENT FUNCTION.

(SLIDE 8) WHILE STANDARD PRODUCT MANUFACTURERS ARE FOCUSING ON

DEVELOPING COMPLEX MICROPROCESSOR CHIPS, WE ARE SHRINKING THEM TO

SINGLE CELLS THAT ARE ONLY ONE PART OF ONE CHIP. AND YOU ARE AN

INTEGRAL FORCE IN THAT CAPABILITY BECAUSE YOU HAVE OBVIOUSLY

ADHERED TO THE SAME MOTTO. IN LESS THAN A DECADE, (SLIDE 9A) YOU

HAVE TAKEN IC DESIGN TECHNOLOGY FROM HUGE MAINFRAMES TO (SLIDE

9B) DESKTOP PCS.

YOU HAVE FORGED THE TECHNOLOGY TO PUT SOPHISTICATED DESIGN TOOLS ON THE DESKS OF ALL SYSTEMS ENGINEERS IN WHAT WE AT GOULD AMI REFER TO AS "DESKTOP IC DESIGN." AND YOU HAVE DEVELOPED THE SYSTEMS THAT ARE THE TOOLS FOR OUR ENGINEERS TO SHRINK CHIPS TO CELLS. BECAUSE OF YOUR ACHIEVEMENTS, WE FOUNDRIES CAN PROVIDE THE COMPONENTS AND DEVELOP THE FABRICATION TECHNOLOGY TO LEAD SYSTEM MANUPACTURERS INTO THE PUTURE.

FROM THAT MORE GLOBAL PERSPECTIVE, LET'S TAKE A LOOK AT THE PRESENT SCENARIO AND HOW ONE ASIC FOUNDRY SEES CAD VENDORS SHAPING THE PUTURE WITH TODAY'S TOOLS.

TODAY, WE ARE SEEING SEVERAL EPFECTS OF CUSTOMER DEMANDS FOR NEW PRODUCTS. FOR EXAMPLE, (SLIDE 10A) SYSTEM COMPANIES ARE FACED WITH EVER DECLINING SYSTEM LIPE CYCLES, (SLIDE 10B) COUPLED WITH THE CONTINUING PRESSURE TO INCREASE THE PACE OF NEW PRODUCT INTRODUCTION (SLIDE 11). THIS SITUATION, IN TURN, (SLIDE 10C) PRESSURES COMPANIES TO REDUCE SYSTEM DEVELOPMENT SPAN TIME, THATIS, THE TIME WHEN A MANUPACTURER IDENTIFIES A MARKET NEED TO THE ACTUAL MARKET INTRODUCTION OF A NEW PRODUCT.

(SLIDE 10D) AS SYSTEM DEVELOPMENT SPAN TIMES DECLINE, THEN SO DO THE SPAN TIMES THAT CAN BE ALLOWED FOR DEVELOPMENT OF THE SYSTEM COMPONENTS. THIS CONSTANT URGENCY TO INTRODUCE NEW PRODUCTS RAPIDLY WAS ITSELF CONVERTED BY THE CAD INDUSTRY INTO A NEW MARKET OPPORTUNITY. YOU HAVE CREATED THE DESIGN TOOLS WHICH INCREASE PRODUCTIVITY AND WHICH ALLOW DESIGN TASKS TO BE DONE IN SHORTER AND SHORTER SPAN TIMES -- THUS ENABLING SYSTEM COMPANIES TO MEET THE PRESSURES OF CUSTOMER DEMAND AND COMPETITION WITHOUT HAVING TO DEPEND SOLELY ON THE EXPENSIVE AND SPACE-CONSUMING PROCESS OF USING MULTIPLE STANDARD PRODUCTS TO PERFORM FUNCTIONS WHICH COULD BE DESIGNED INTO A SINGLE CHIP.

(SLIDE 12) A SECOND FACTOR PRESSURING SYSTEMS COMPANIES IS THE COMPETITION OF COST. TO BE A LEADER REQUIRES BOTH UNPARALLELED SYSTEM CAPABILITY AS WELL AS COMPETITIVE PRICING. SYSTEM COMPANIES HAVE, THEREFORE, ALWAYS TURNED TO HIGHER LEVELS OF INTEGRATION TO REDUCE SYSTEM PART COUNTS. JUST AS THE CAD BUSINESS TOOK THE PROBLEM OF DECREASING LIPE CYCLES AND TURNED IT INTO A MARKET OPPORTUNITY, SO TOO HAVE WE IN THE COMPONENTS BUSINESS TAKEN THE NEED FOR GREATER LEVELS OF INTEGRATION AND PROVIDED CUSTOMIZED CIRCUITS THAT USE VLSI TECHNOLOGY TO PROVIDE THESE BENEFITS TO CUSTOMERS.

(SLIDE 13) THE USE OF ASICS AS SOLUTIONS TO SYSTEM PROBLEMS HAS SEVERAL KEY ADVANTAGES WHEN COMPARED WITH STANDARD PRODUCT IC SOLUTIONS. THESE ADVANTAGES HELP CUSTOMERS WITH THEIR MARKET NEEDS WHILE COMPLEMENTING AND EXPLOITING THE BENEFITS OF CAD DEVELOPMENTS. (SLIDE 14) PIRST, ASICS ARE OBVIOUSLY JUST THAT: SYSTEMS SOLUTIONS RATHER THAN COMPONENT-FUNCTION SOLUTIONS.

(SLIDE 15) NEXT, TODAY'S ASIC DEVICES ALLOW HIGH LEVELS OF INTEGRATION AS MEASURED IN TERMS OF GATE EQUIVALENTS. TODAY'S PRODUCTION 2u CMOS DOUBLE-LAYER METAL PROCESSES ALLOW THE IMPLEMENTATION OF MORE THAN 10,000 GATES IN A GATE ARRAY -- MORE IN A STANDARD CELL CIRCUIT.

(SLIDE 16) THE USE OF ASICS IS BEING PROPELLED BY GREATLY REDUCED DESIGN COSTS AND SPANS FOR IMPLEMENTING DESIGN IDEAS AS

CUSTOMIZED ICS. THESE REDUCED COSTS AND SPANS ARE PRIMARILY THE RESULT OF IMPROVED CAD SOFTWARE SYSTEMS THAT GUARANTEE ACCURATE COMPUTER SIMULATION OF THE DESIGN AND ENSURE THAT THE ASIC MASK DESIGN CREATES A CIRCUIT WHOSE SILICON BEHAVIOR EXACTLY MATCHES COMPUTER SIMULATION OF THE DESIGN. IN OTHER WORDS, YOU HAVE GIVEN ENGINEERS THE TOOLS TO DO THEIR BREADBOARDING ON A COMPUTER RATHER THAN SITTING AT A BENCH AND LITERALLY HANDWIRING COMPONENTS TO A WIREWRAP BOARD AND THEN TESTING IT. (SLIDE 17) THE CONCEPT OF USING COMPUTER SIMULATION TO VALIDATE A DESIGN AND THEN USING THE VERIFIED DESIGN DESCRIPTION TO CREATE THE MASK DESIGN IS OFTEN CALLED "CORRECT—BY—CONSTRUCTION," BECAUSE IT ENSURES THAT IF THE LOGIC DESIGN IS DONE CORRECTLY, THE SILICON WILL WORK THE FIRST TIME. AND IT IS A CAPABILITY AVAILABLE NOW.

(SLIDE 18) ANOTHER MAJOR FACTOR THAT IS CAUSING THE USE OF ASIC DEVICES TO GROW IS THE TREMENDOUS EXPANSION OF THE INSTALLED BASE OF ENGINEERING WORKSTATIONS. YOU CAD VENDORS HAVE PLACED ASIC DESIGN WITHIN THE REACH OF SYSTEMS DESIGNERS. (AS AN ASIDE, I'LL SAY THAT WE IC VENDORS APPLAUD THAT BECAUSE WHEN THE CAD TOOLS ARE IN THE HANDS OF SYSTEMS DESIGNERS, THEN SO TOO ARE ASICS.

AND WE CAN USE OUR RESOURCES FOR PABRICATION, WHICH IS OUR BUSINESS, AND USE OUR ENGINEERING RESOURCES TO CREATE NEW COMPONENTS FOR LIBRARIES ACCESSIBLE BY ALL, NOT JUST ONE CUSTOMER.)

(SLIDE 19) IT IS ALSO IMPORTANT TO NOTE THAT THE INCREASED PROPRIETARY PROTECTION AFFORDED BY ASIC DEVICES ALSO FUELS THEIR FOPULARITY. A DESIGN WHICH IS CONTAINED IN AN ASIC DEVICE IS MORE DIFFICULT TO COPY THAN THE SOFTWARE IN A STANDARD PRODUCT-BASED MICRO P/C-BASED SYSTEM SOLUTION. THUS, SYSTEMS COMPANIES GAIN ANOTHER COMPETITIVE EDGE.

(SLIDE 20) FINALLY, THE TREND TOWARD ASIC IS GATHERING MOMENTUM BECAUSE OF THE EXPLOSION IN THE USE OF PC-BASED DESIGN TOOLS.

COMPANIES LIKE FUTURENET, P-CAD, VIEWLOGIC AND OTHERS AGAIN SHOW HOW A NEW MARKET SEGMENT WAS CREATED BY EXPLOITING A GIVEN SITUATION. THE PERVASIVE PC'S, USED AS OFFICE TOOLS TO REPLACE TYPEWRITERS AND CALCULATORS, HAVE BECOME PERSONAL ENGINEERING WORKSTATIONS FOR DOCUMENTATION, COMMUNICATION, AS WELL AS ENGINEERING TASKS SUCH AS PC BOARD DESIGN AND SOPHISTICATED IC DESIGN. JUST THINK, THREE YEARS AGO CUSTOMIZED ICS WERE THE SEMICONDUCTORS OF THE KNOWLEDGEABLE FEW. TODAY, THEY CAN BE OBTAINED BY ANYONE WHO HAS A PC AT HIS DESK.

IT IS CLEAR THAT SHORTENING SYSTEM DESIGN TIMES AND LIFE CYCLES WILL INCREASINGLY CAUSE FOCUS ON REDUCING SYSTEM DEVELOPMENT SPAN TIMES, AND THE TREND TOWARD THE USE OF ASICS WILL CONTINUE TO CREATE DEMAND FOR CAD CAPABILITY THAT IS COMPLETE IN TERMS OF THE DESIGN FUNCTIONS SUPPORTED AND FAST IN TERMS OF THE TIME IT TAKES TO PERFORM A GIVEN SET OF FUNCTIONS.

(SLIDE 22) AT ANY POINT IN TIME, THE MOST COMPLICATED ASIC DEVICES REQUIRE LEADING-EDGE COMPUTING POWER TO KEEP DEVELOPMENT SPANS WITHIN REASON. TODAY'S MOST COMPLICATED CHIPS ARE BEING DESIGNED FOR USE IN TOMORROW'S MOST COMPLICATED SYSTEMS. AND THIS IS A NEVER-ENDING CYCLE.

OUR WORLD TODAY: (SLIDE 23A) SHORT SYSTEM LIFE CYCLES, (SLIDE 23B) SHORT DESIGN TIMES, (SLIDE 23C) HIGHER LEVELS OF INTEGRATION, (SLIDE 23D) GROWTH OF THE ASIC MARKET, (SLIDE 23E) PERVASIVENESS OF WORKSTATIONS AND PCs, (SLIDE 23F) INCREASED PROPRIETARY IC DESIGN THROUGH USE OF CUSTOMER DESIGNED ASICS, (SLIDE 23G) REDUCED COSTS OVERALL -- ALL OF THESE FACTORS HAVE EITHER BEEN CREATED OR EXPLOITED BY YOU TO THE BENEFIT OF SYSTEM COMPANY CUSTOMERS AND THE IC INDUSTRY.

WITH PROGRESS, HOWEVER, ALSO COMES CHALLENGE. AND TODAY YOU
COLLECTIVELY FACE A NUMBER OF SIGNIFICANT CHALLENGES. THE FIRST
CHALLENGE YOU MUST MEET IS OF YOUR OWN MAKING, (SLIDE 24) DUE TO
COMPETITION AND A DESIRE TO DISTINGUISH ONESELF FROM THE
COMPETITION, YOU HAVE COLLECTIVELY OVERSOLD WORKSTATION
CAPABILITY.I WILL REFER TO THIS CHALLENGE BY USING THE
EUPHEMISTIC TERM, "THE GREAT PROMISES OF CAD MARKETING." A MORE
CIVIL TERM FOR "THE BIG LIES." NOW DON'T CRINGE -- YOU'RE
CERTAINLY NOT ALONE IN THIS PHENOMENON AS THE IC INDUSTRY ITSELF
HAS, UPON OCCASION (REALISTICALLY MORE OFTEN THAN NOT), OVERSOLD
BOTH CAPABILITY AND AVAILABILITY. AND WE, TOO, HAVE HAD TO PAY
THE PRICE.

SOME OF THE GREAT PROMISES ARE THESE:

(SLIDE 25) o "WE HAVE A FULLY INTEGRATED SYSTEM WITH A COMMON DATABASE."

(SLIDE 26) • "WITH A PC ON YOUR DESK, YOUR DESIGN PROBLEMS ARE OVER."

(SLIDE 27) O "OUR WORKSTATION SOFTWARE CAPABILITIES ARE
VIRTUALLY UNLIMITED." AND..."IF YOU DON'T SEE IT NOW, WE'LL HAVE
IT IN THE NEXT SYSTEM RELEASE, MAYBE NEXT QUARTER."

(SLIDE 28) O AND THEN THERE'S THE "OPEN ARCHITECTURE" PROMISE
"SO YOU WANT TO USE YOUR IN-HOUSE SOFTWARE FOR SOME FUNCTIONS -NO PROBLEM."

o "OUR SILICON COMPILER ALLOWS YOU TO GO DIRECTLY

FROM A HIGH-LEVEL HARDWARE DESCRIPTION LANGUAGE TO A TOOLING

TAPE, WHICH WILL -- OF COURSE -- PRODUCE WORKING PIRST SILICON IN

THE FOUNDRY OF YOUR CHOICE."

(SLIDE 29) o "OUR SYSTEM IS SO USER FRIENDLY THAT TRAINING IS SUPERPLUOUS."

WE'VE ALL HEARD THESE PROMISES, AND WE ALL KNOW THAT NONE OF THEM IS COMPLETELY TRUE. THE CHALLENGE THEN IS TO MAKE THESE PROMISES A REALITY AND THEN RAPIDLY FORGE AHEAD WITH NEW ADVANCES SO THAT USERS CAN CONTINUE TO INCREASE THEIR CAPABILITY AND MEET THE EXPECTATIONS WHICH HAVE BEEN LAID OUT FOR THEM.

(SLIDE 30) THE SECOND CHALLENGE IS TO ELIMINATE VERTICAL FOCUS; THAT IS, CONCENTRATING SO HEAVILY ON YOUR OWN PRODUCT MIGRATION PLANS THAT YOU FORGET THAT CUSTOMERS DRIVE EACH OF US TOWARD SIMPLICITY AND OPEN SYSTEMS CAPABILITY. AFTER ALL, IT WAS THE CUSTOMER'S NEEDS IN THE FIRST PLACE THAT HAVE DRIVEN US TO THE PRESENT PROMISING OPPORTUNITY.

THIS CUSTOMER-DRIVEN INFLUENCE IS MOST OBVIOUS IN THE TREMENDOUS INTEREST IN THE (SLIDE 31) CONCEPT OF SILICON COMPILATION. WE ALL KNOW THAT SILICON COMPILATION IS IN ITS INFANCY AND PROBABLY STILL A FEW YEARS OFF AS AN ACROSS-THE-BOARD ALTERNATIVE IN ASIC DESIGN. THE CURRENT INTEREST IN SILICON COMPILATION IS SO GREAT THAT IC VENDORS HAVE ESTABLISHED RELATIONSHIPS WITH THE SILICON COMPILATION COMPANIES FOR FOUNDRY SERVICES NOW -- EVEN THOUGH THE ACTUAL NUMBER OF CIRCUITS IN PRODUCTION THAT HAVE BEEN DEVELOPED THROUGH THIS METHOD IS MINUTE COMPARED TO TOTAL ASIC PRODUCTION.

(SLIDE 32) THIS INTEREST IN SILICON COMPILATION IS BECAUSE

SYSTEMS ENGINEERS ARE MUCH LIKE CONSUMERS IN THEIR ATTITUDE

TOWARDS DESIGN TOOLS. JUST AS APPLE, IBM AND OTHERS HAVE LEARNED

THAT CONSUMERS DO NOT WANT TO BE QUASI-PROGRAMMERS IN ORDER TO

USE A PC, SO ARE ENGINEERS TELLING US THAT THEY DO NOT WANT TO

BECOME IC DESIGNERS IN ORDER TO DESIGN ASICS FOR THEIR SYSTEMS.

THEY WANT THE BENEFITS OF CUSTOMIZED CHIPS WITHOUT THE

COMPLEXITY, HIGH COST, LONG DEVELOPMENT TIMES, INTENSE

ENGINEERING EFFORT, AND PLAIN HASSLE.

- 13 -

(SLIDE 33) THE ASIC DESIGNER WANTS SIMPLICITY AND A PULLY AUTOMATED DESIGN SYSTEM WHERE COMPUTING POWER CAN BE MATCHED TO THE PROBLEM TO (SLIDE 34) OBTAIN THE SPAN TIME REQUIRED BY THE DEMANDS OF THE MARKET. IP THE USE OF ASIC DEVICES IS TO CONTINUE ITS MUSHROOMING GROWTH, (SLIDE 35) THE CAD SYSTEMS AVAILABLE NOW MUST BE EASILY INTERCONNECTED, (SLIDE 36) CHEAP ENOUGH SO ALL OF THE ENGINEERS IN A COMPANY HAVE INDIVIDUAL ACCESS TO THEM, (SLIDE 37) AUTOMATED FOR LOW COST SO DEVELOPMENT SPANS ARE COMPETITIVE WITH THE READY AVAILABILITY OF STANDARD PRODUCTS AND ELECTRICALLY PROGRAMMABLE LOGIC DEVICES. AND THIS WILL HAPPEN, BECAUSE OUR CUSTOMERS DEMAND IT AND, TOGETHER, YOU CAD VENDORS AND WE ASIC FOUNDRIES HAVE THE TECHNOLOGY TO MAKE IT WORK. THAT KNOWLEDGE IS THE BASIS FOR OUR MOVE INTO THE FUTURE. YOUR ROLE IN BRINGING IT ABOUT WILL BE EVEN GREATER THAN OURS.

LET'S SEE HOW I BELIEVE THE FUTURE SCENARIO WILL UNFOLD. (SLIDE 39A) WE ALL KNOW THAT FULL-SERVICE ASIC VENDORS AND SYSTEM MANUFACTURERS WHO ARE CURRENTLY DESIGNING ASIC DEVICES BOTH REQUIRE A CAD DESIGN ENVIRONMENT CONTAINING (SLIDES 39B - F) VARIOUS LEVELS OF COMPUTE CAPABILITY. THE DESIGNER MUST HAVE THE CAPABILITY TO MATCH THE POWER TO HIS PROBLEM; THAT IS, TO USE THAT FUNCTIONAL CAPABILITY AND ASSOCIATED COMPUTE POWER WHICH WILL PROVIDE THE NECESSARY CONTROL IN THE REQUIRED SPAN TIME FOR A PARTICULAR TASK.

NOW THE CAD INDUSTRY HAS ALREADY CREATED THE ASIC DESIGN PRODUCTS THAT LAY THE GROUNDWORK FOR AN IDEAL DESIGN ENVIRONMENT. BUT THERE IS A MISSING LINK. IF YOU REMEMBER THE BIG LIES, OR MARKETING PROMISES, YOU WILL RECALL THAT WE SAID (SLIDE 49A) PCs ON EVERYONE'S DESK (SLIDE 49B), FULLY INTEGRATED SYSTEMS (SLIDE 49C), OPEN ARCHITECTURES (SLIDE 49D), UNLIMITED WORKSTATION CAPABILITY (SLIDE 49E), AND USER FRIENDLINESS -- ALL AT A COST PURCHASING AGENTS WOULD DIE FOR -- WERE HERE ALREADY AND SOLVED ALL OF THE CUSTOMERS' PROBLEMS. THEY DON'T. THEY ONLY SOLVE HALF OF THEM. BECAUSE THOSE PROMISES ADDRESS THE PROBLEMS OF INDIVIDUAL DESIGNERS DOING WORK INDIVIDUALLY (SLIDE 50A). AND SYSTEMS DESIGN IS THE RESULT OF TWO TEAM EFFORTS: A TEAM OF ENGINEERS AT A SYSTEM MANUFACTURER WORKING IN CONCERT WITH A TEAM OF ENGINEERS AT THE FOUNDRY. (SLIDE 51) THE MISSING LINK TO THE IDEAL ASIC DESIGN ENVIRONMENT THAT CAD WILL SHAPE IS ... (SLIDE 52) NETWORK TECHNOLOGY SUPPORTED BY AN OPEN SYSTEMS CONCEPT.

NETWORK TECHNOLOGY IS THE ANSWER AND IT'S AVAILABLE NOW -- IF CAD VENDORS CHOOSE TO TAKE ADVANTAGE OF IT. AND YOU MUST UTILIZE IT IF YOU ARE TO MAKE GOOD YOUR PROMISE OF AN OPEN SYSTEM ARCHITECTURE.

NETWORKING TECHNOLOGY WILL EVOLVE IN TWO WAYS. (SLIDE 53) THE FIRST IS BY USING THE CONCEPT OF OPEN ARCHITECTURE TO ITS FULLEST MEANING. ASIC DESIGNERS CAN CREATE A NETWORK TAILORED TO THEIR NEEDS IN THE FOLLOWING MANNER: FIRST, THEY CAN SELECT THE COMMERCIALLY AVAILABLE CAD SYSTEMS NECESSARY TO MEET THEIR PARTICULAR NEEDS. THIS CAN BE A MIX OF PCs, WORKSTATIONS, SILICON COMPILER SYSTEMS AND OTHER DESIGN SYSTEMS ALREADY IN PLACE. (SLIDE 54) NEXT THEY CAN INTEGRATE THEIR INTERNALLY DEVELOPED SOFTWARE WITH THESE SYSTEMS. (SLIDE 55) THE RESULT IS AN OUTPUT OF DESIGN DATA THAT INTERPACES WITH THE COMPANY'S UNIQUE MANUPACTURING AND TESTING REQUIREMENTS. (SLIDE 56) OPEN SYSTEMS ARE A KEYSTONE TO ENSURE THAT DATA CAN BE PASSED AMONG DISSIMILAR COMPUTERS RUNNING DIFFERENT APPLICATION SOFTWARE UNDER DIFFERENT OPERATING SYSTEMS. SOME OF THE SOFTWARE WILL NECESSARILY BE COMMERCIALLY DEVELOPED AND SOME OF IT WILL NECESSARILY BE DEVELOPED INTERNALLY -- AS THE DESIGN TASKS DICTATE.

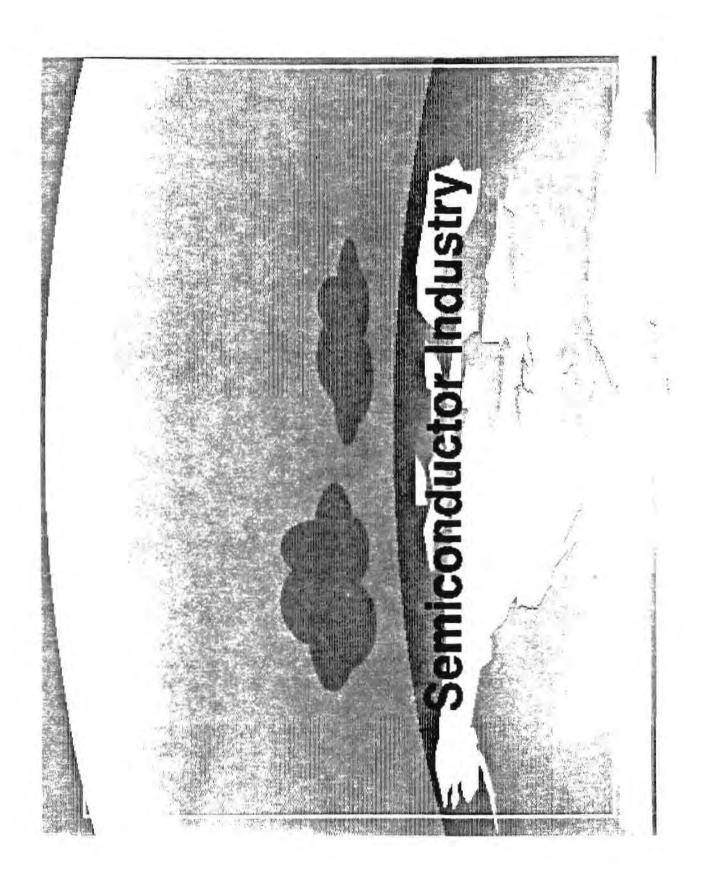
THE OPPORTUNITY IS GREAT ... AND SO ARE THE EXPECTATIONS! USERS WILL TIRE OF PROMISES NOT KEPT AND INFLATED PERFORMANCE CLAIMS. IF THE CAD INDUSTRY DOES NOT CREATE AN OPEN SYSTEMS ENVIRONMENT, USERS WILL EVENTUALLY FORCE THE SITUATION BY CREATING THESE NETWORKS THEMSELVES. AND THEN YOU WILL HAVE THE SAME SCENARIO I DESCRIBED AT THE BEGINNING OF MY SPEECH: NEW TECHNOLOGY BEING DRIVEN BY CUSTOMER PRESSURES RATHER THAN YOUR INDUSTRY SHAPING CUSTOMER ADVANCEMENTS. (SLIDE 57A) THE SUCCESSFUL CAD VENDOR DOES NOT GIVE LIP SERVICE TO THE NEED FOR OPEN SYSTEMS DESIGN ENVIRONMENT, BUT PROVIDES ASIC DESIGN CAPABILITIES WHICH CAN BE EASILY INTEGRATED INTO SUCH A DESIGN ENVIRONMENT.

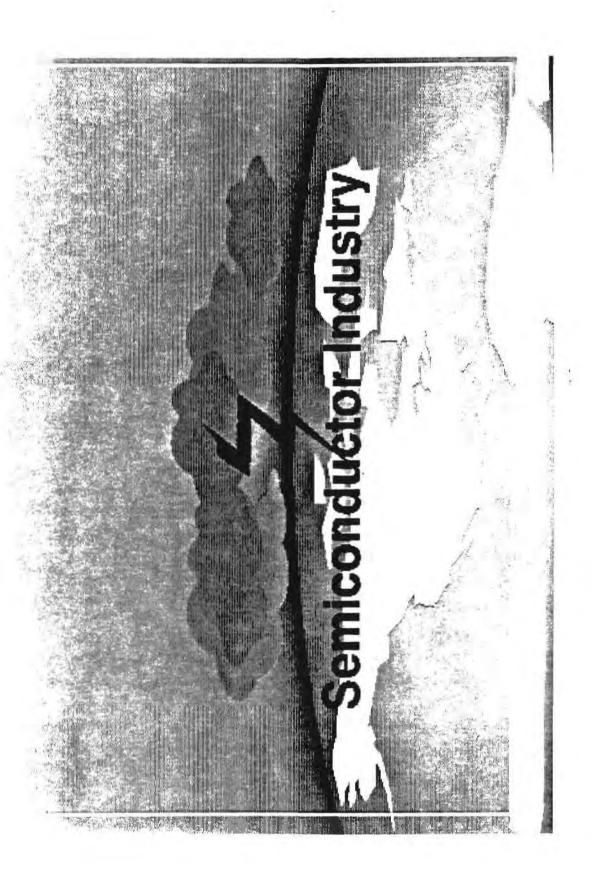
(SLIDE 57B) YOU MUST ALSO PROVIDE THE HARDWARE INTERCONNECTION CAPABILITY TO SUPPORT THE MAJOR NETWORKING PROTOCOLS SUCH AS ETHERNET AND THE TOKEN-PASSING BUS AND RING STANDARDS. (SLIDE 57C) IN ADDITION, YOU MUST DRIVE THE CREATION OF DATA FORMAT INTERCHANGE STANDARD SUCH AS EDIF IN ORDER TO ENSURE THAT FILES CAN BE READILY PASSED ACROSS THE NETWORK.

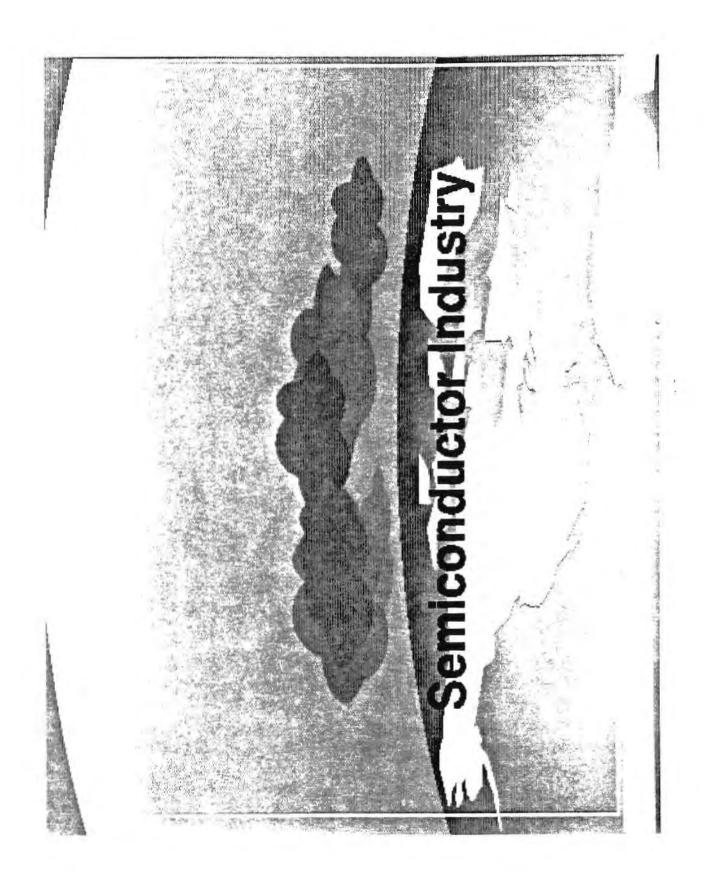
(SLIDE 58) AS FOR THE ASIC VENDORS, WE MUST BE PREPARED TO SUPPORT THE STANDARD DATA INTERCHANGE FORMATS TO ENSURE THAT DESIGN DATA CREATED IN THE DESIGN NETWORK ENVIRONMENT CAN BE READILY TRANSFERRED TO OUR FOUNDRIES FOR SILICON FABRICATION.

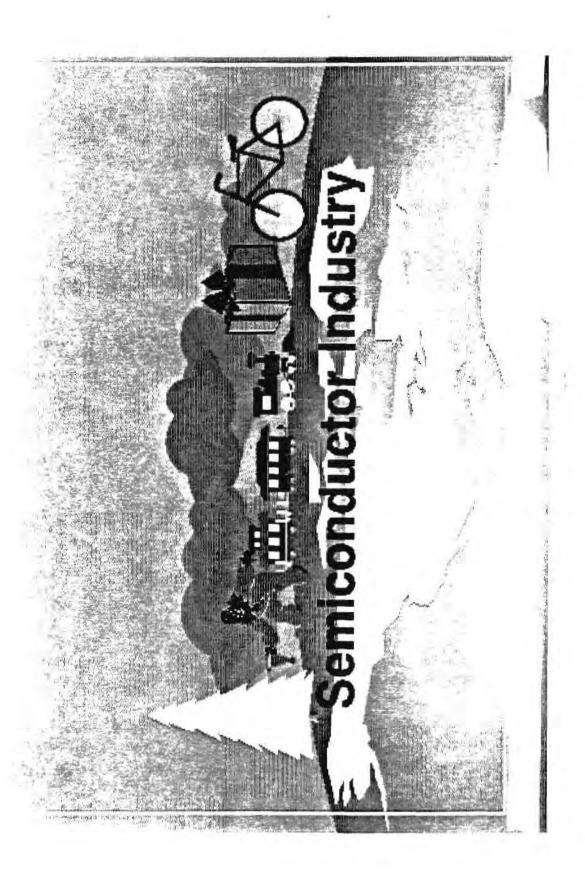
(SLIDE 59) TO CREATE A TRUE OPEN SYSTEMS NETWORK, EVERY CAD VENDOR MUST RECOGNIZE THAT IT ALONE IS NOT LIKELY TO CREATE THE GALACTIC ASIC DESIGN ENVIRONMENT. (SLIDE 60) THE BREADTH OF DESIGN TASKS AND THE TAILORING OF THE DESIGN EFFORT TO SPECIFIC IC MANUFACTURING AND TEST CAPABILITY MAKE IT UNLIKELY THAT ANY SINGLE VENDOR CAN ENTIRELY SOLVE THE PROBLEM. CO-EXISTENCE WITH OTHER VENDORS AND WITH USER SOFTWARE IS REALISTIC AND ESSENTIAL ... AFTER ALL, THE LEVELS OF COST, CAPABILITY AND APPLICATION AMONG SYSTEMS COMPANIES WILL ALWAYS DIFFER SIGNIFICANTLY ENOUGH, SO THE COMPLEMENTARY USAGE OF TOOLS IS THE IDEAL.

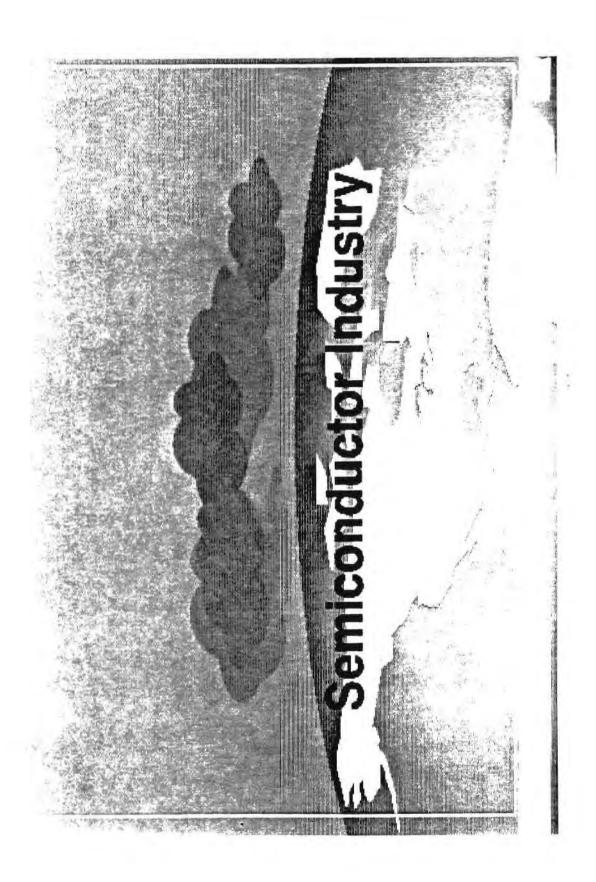
(SLIDE 61A) THE TIME HAS COME TO TAKE THE BUILDING BLOCKS OF AN ASIC DESIGN ENVIRONMENT AS CREATED BY THE COMMERCIAL CAD VENDORS (SLIDE 61B), COUPLE THEM WITH TODAY'S NETWORK TECHNOLOGY AND EMERGING STANDARDS FOR DATA INTERCHANGE. AND CREATE THE IDEAL ASIC DESIGN ENVIRONMENT (SLIDE 62). ONLY THROUGH REALIZING PROMISES MADE BY THE CAD INDUSTRY WILL THE INDUSTRY CONTINUE TO GROW. THESE PROMISES CANNOT BE KEPT IN A CLOSED SYSTEM ENVIRONMENT. WE ASIC VENDORS LOOK NOT TO A STANDARD PRODUCT FOR OUR FUTURE GROWTH, BUT TO YOUR CONTINUED SUCCESS IN CREATING PROGRESS THROUGH CAPABILITY. (SLIDE 63) ASIC IS OUR RISING SUN.



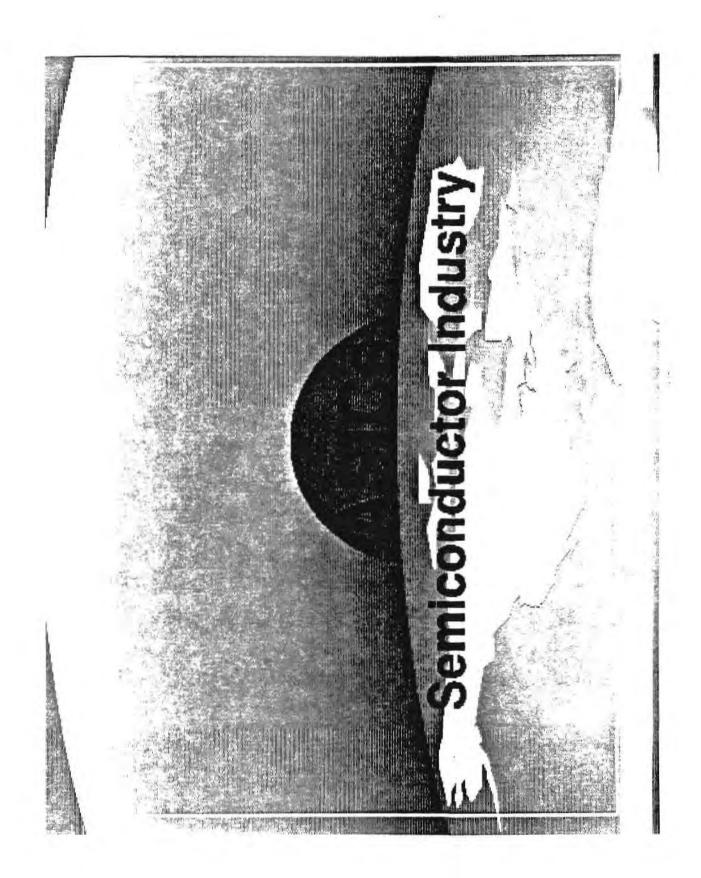






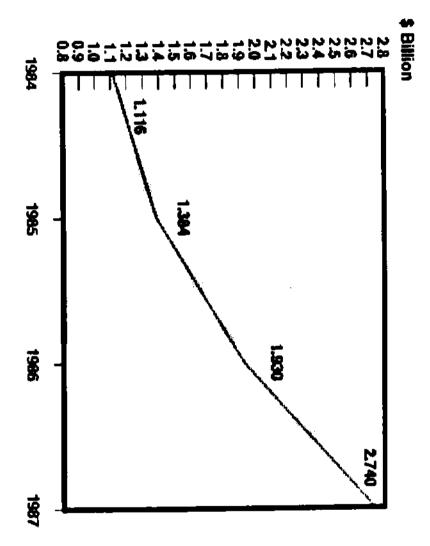






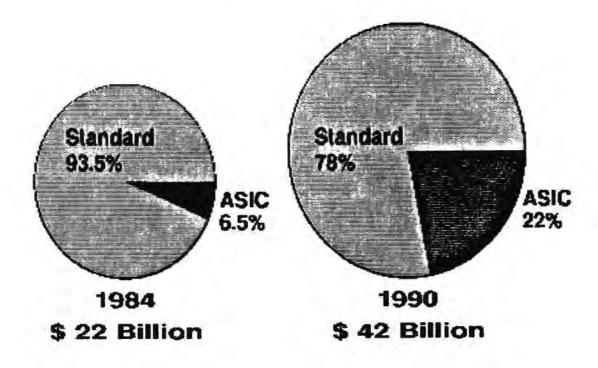






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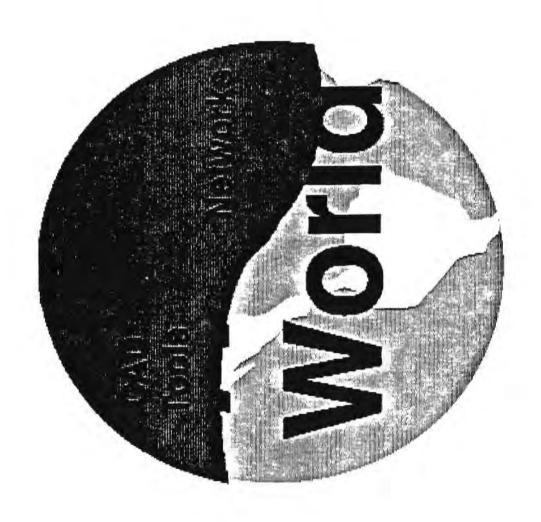
### **ASIC Share of Merchant IC Revenues**

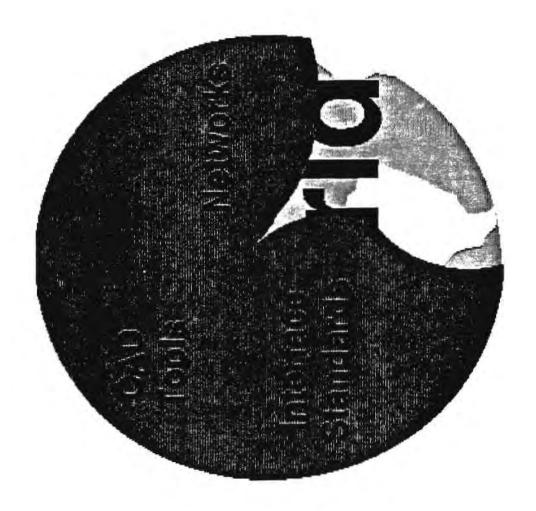


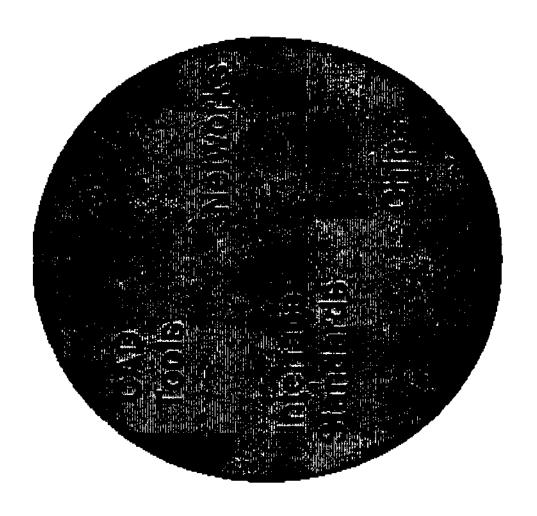
Source: The Technology Research Group, 1985

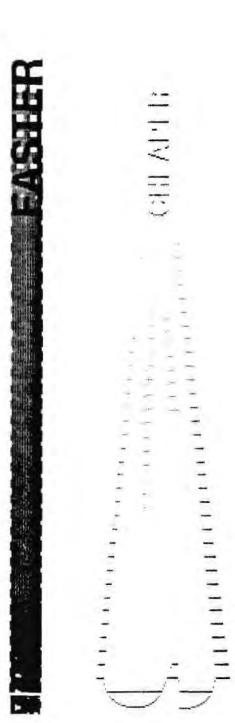




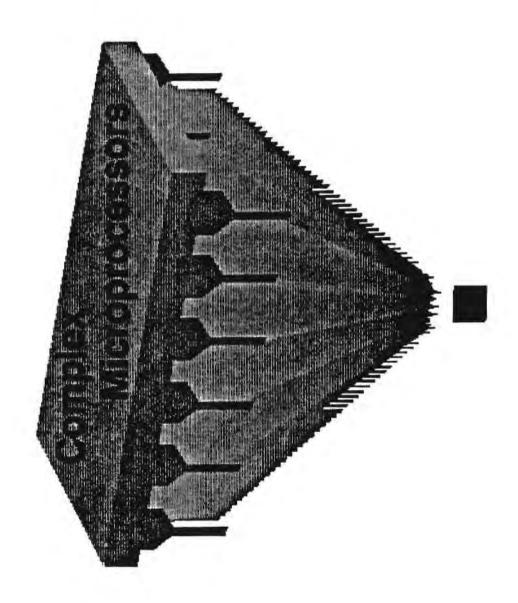


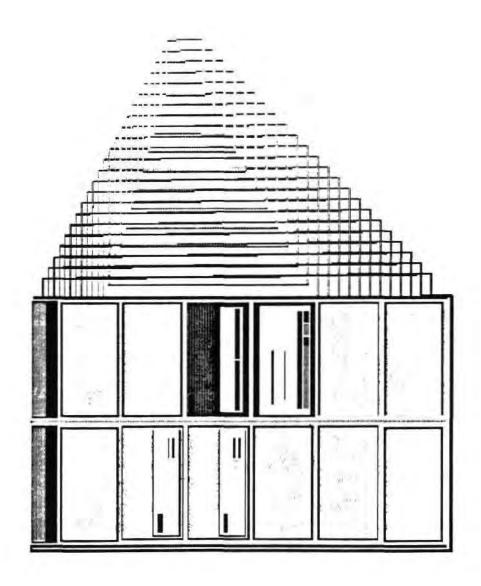


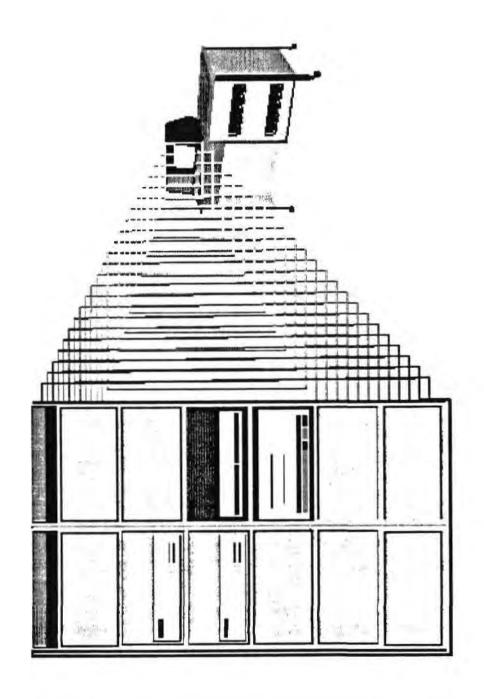








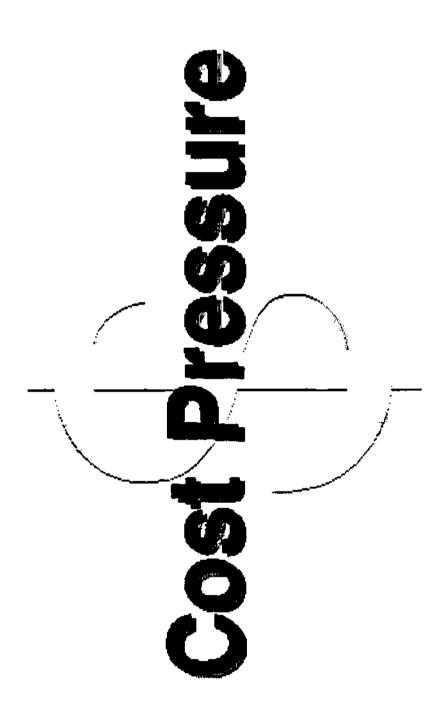




**Rapid Product Introductions** 

Reduced System Development Spans

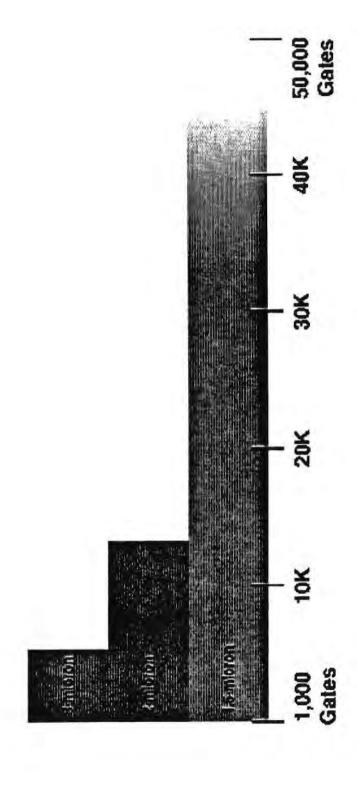
**Reduced Component Development Spans** 

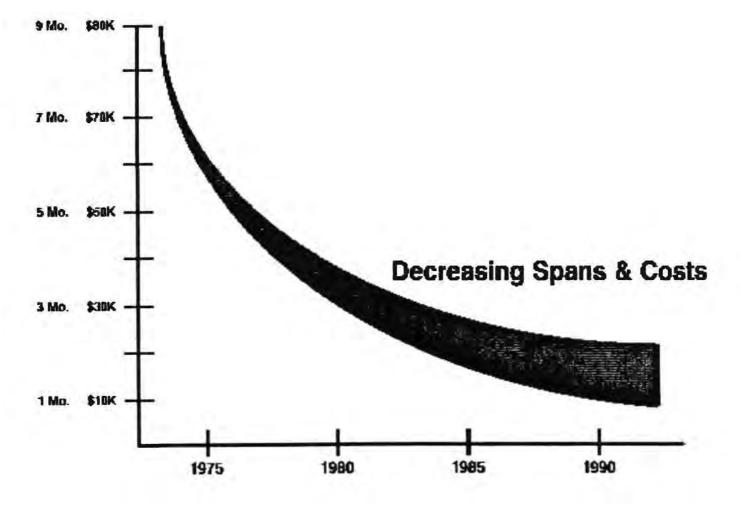


## ASIC Advantages

### **System Solutions**

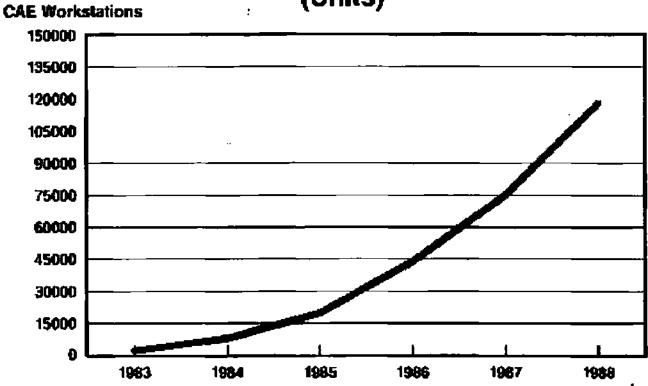
Integration Levels by Technology





### **Success The First Time**

### Installed Base of CAE Workstations (Units)



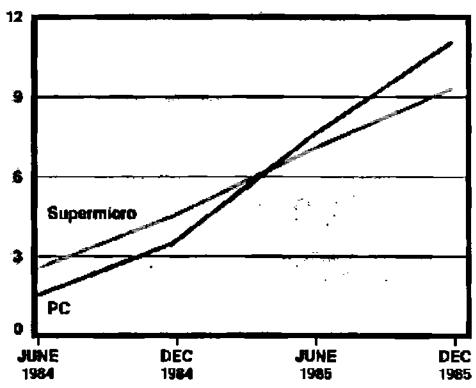
Source: Technology Research Group

# **Proprietary Protection**

### 184

### **Installed Base of CAE Stations**

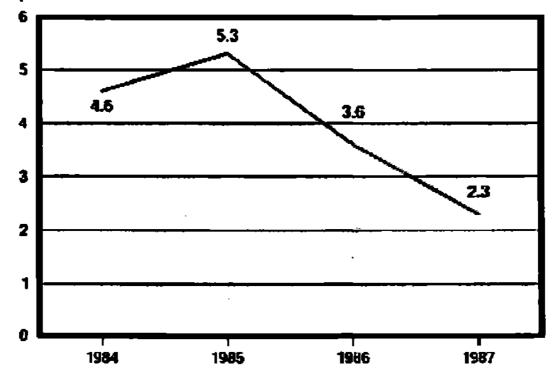
### Thousands of CPUs



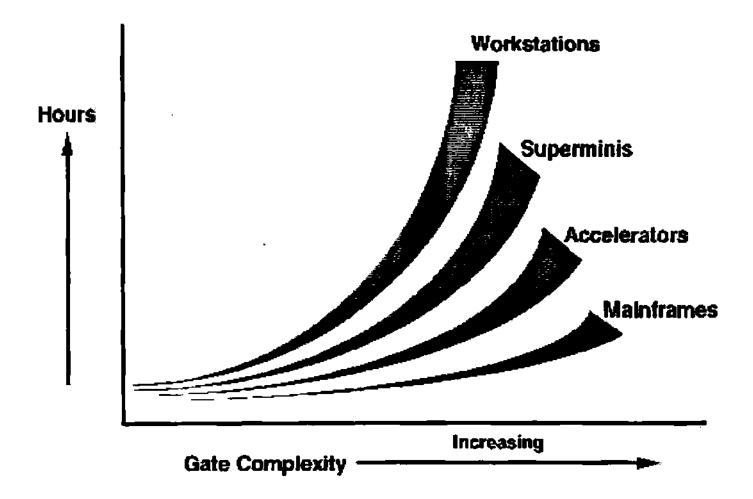
Source: The Technology Research Group, 1985

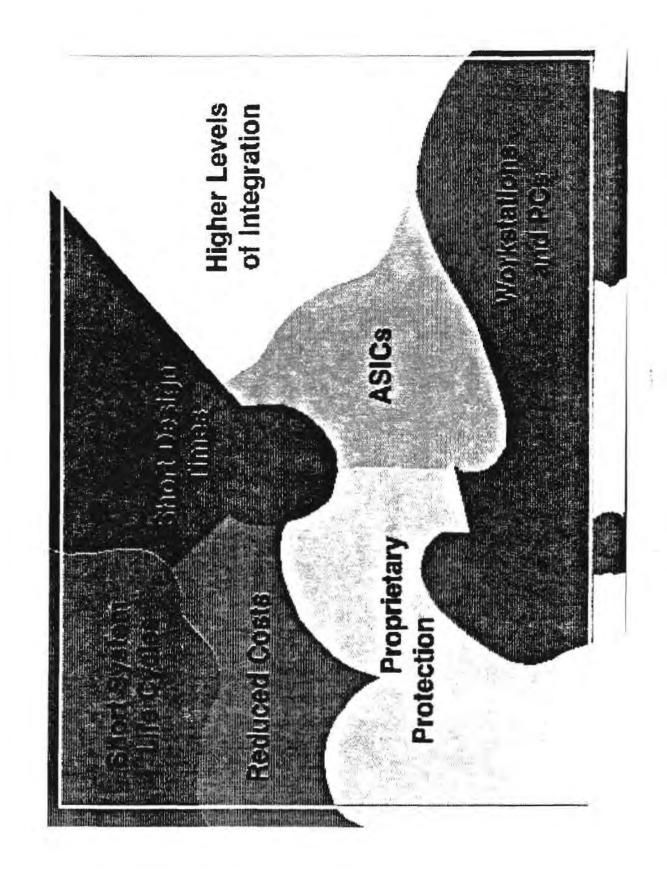
### **Sharing of CAE Workstations**

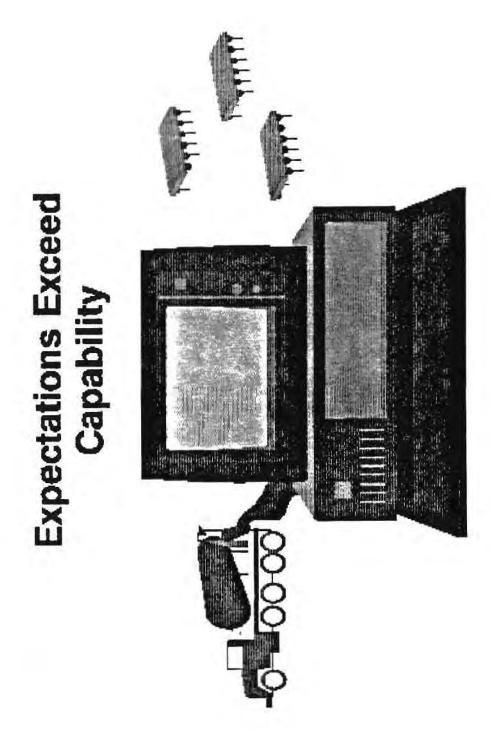
### **Users per Workstation**



Source: The Technology Research Group



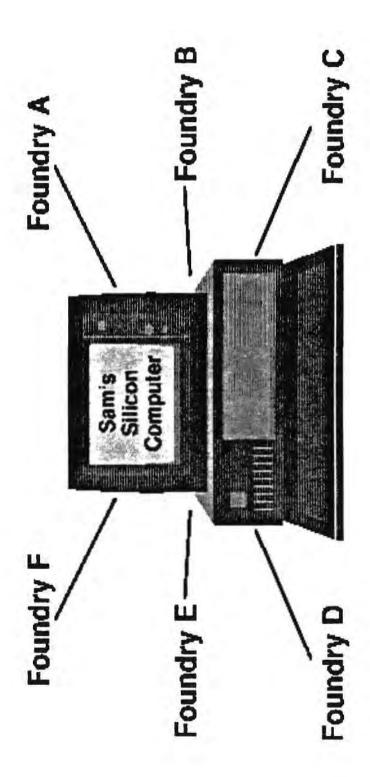






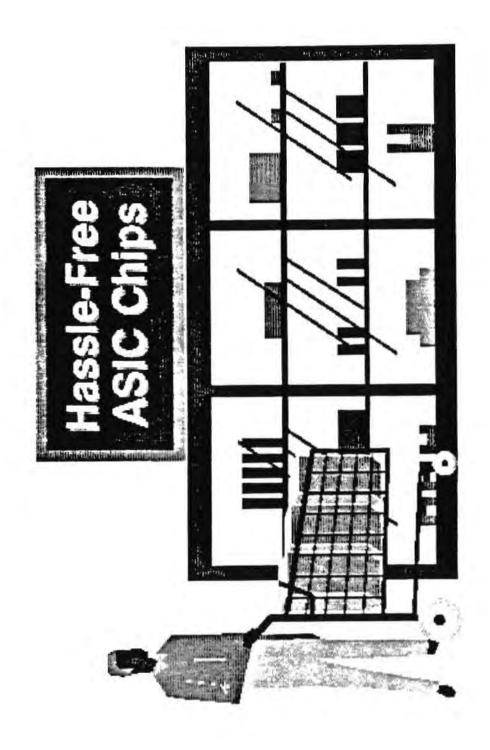
### **Fully Integrated System**

### Capability Unlimited



## Simplicity Open Systems Capability









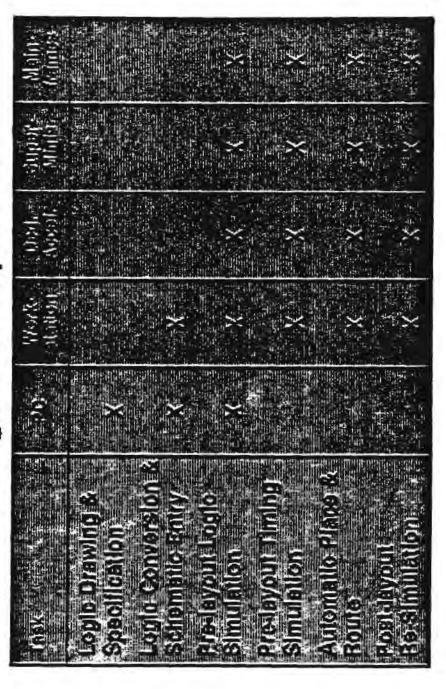
# Interconnected

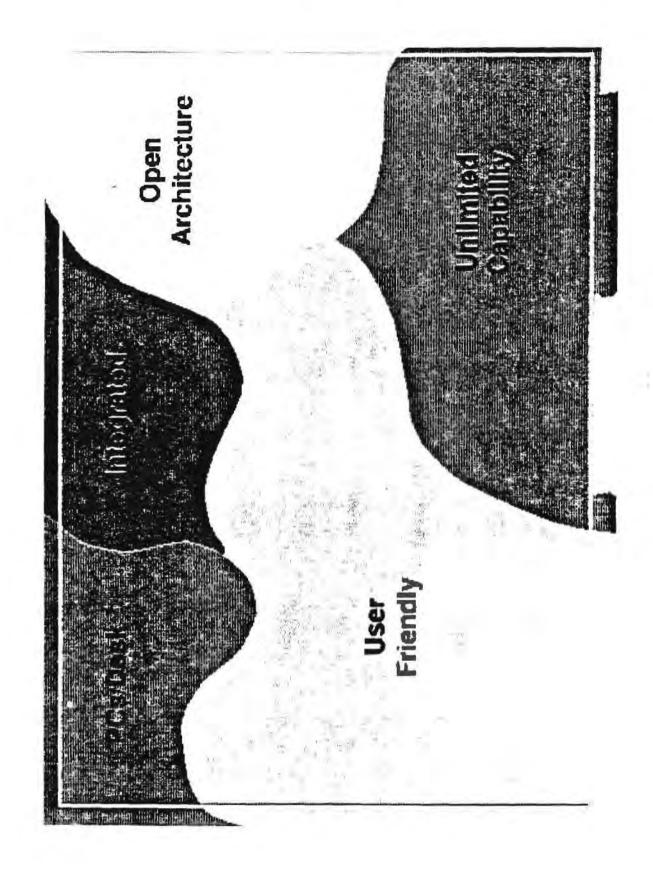
## Reasonably Priced

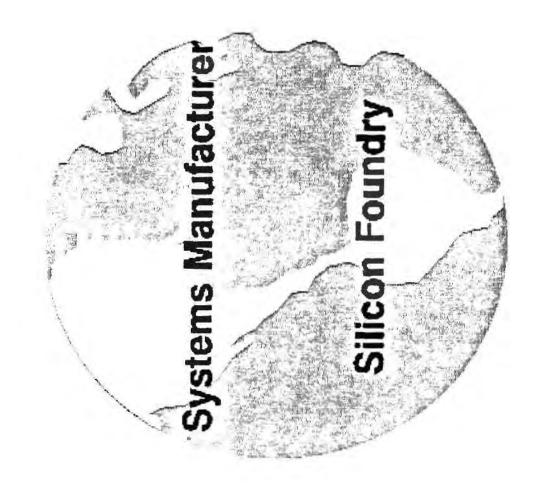
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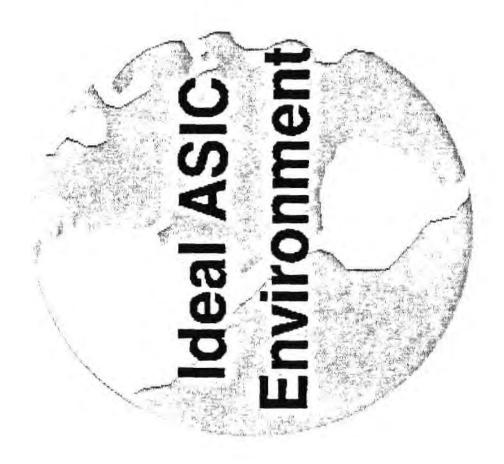
## Automated

Design Tool Options



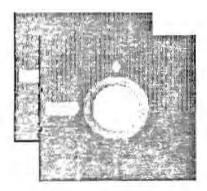


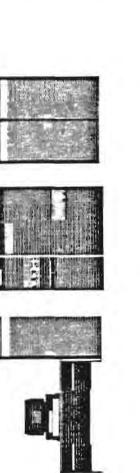




## Networking

4

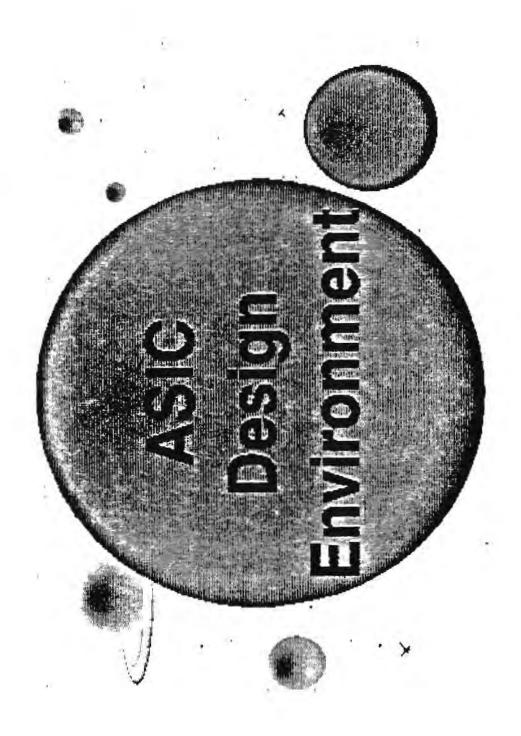


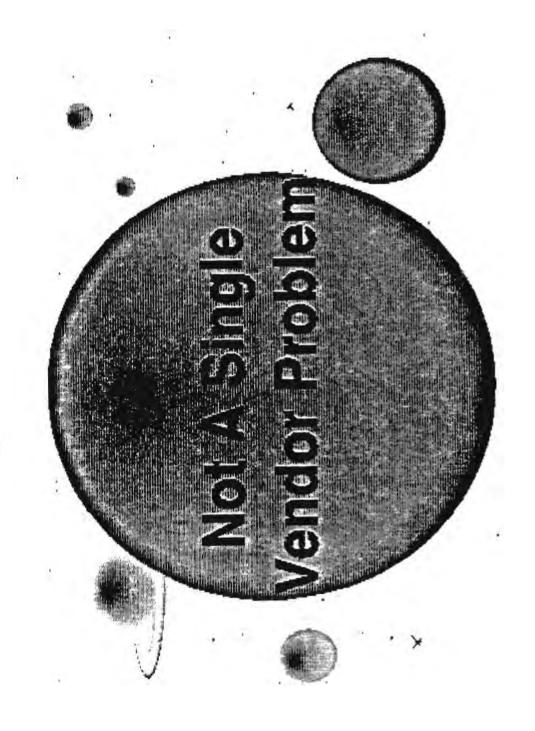




- Open Systems
- Hardware Interconnection
- Data Format Interchange Standards

### **Support Interchange Formats**





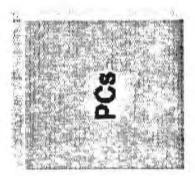




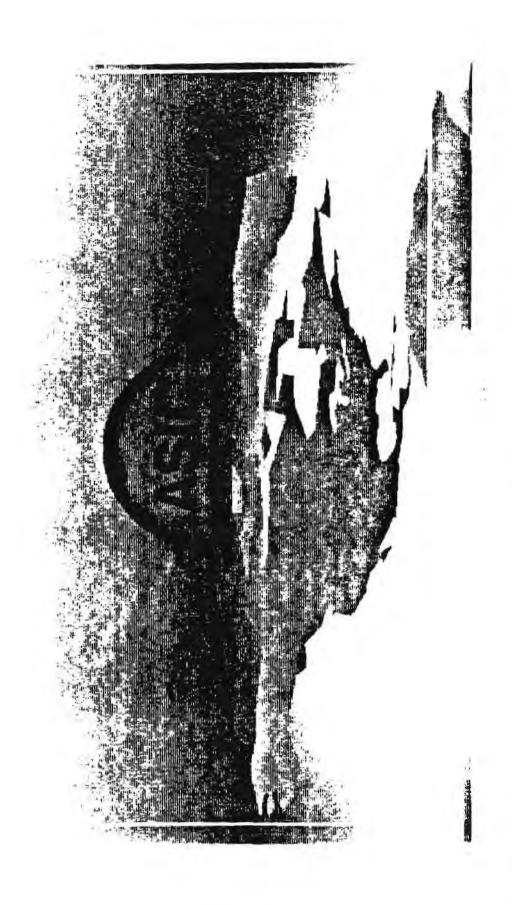






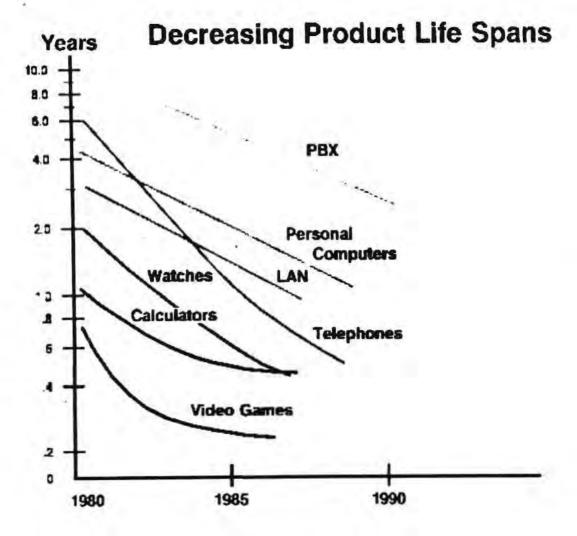
















### USER INTERFACES IMPACT PRODUCTIVITY

David L. Bailey
President and Chief Executive Officer
Cericor Incorporated

Mr. Bailey is President and Chief Executive Officer of Cericor Incorporated. Before joining Cericor, he was founder, President, and Chief Executive Officer of IOMEGA, a multimillion dollar computer company. There he was responsible for funding, hiring key personnel, managing product development, and establishing marketing strategies for the United States and Europe. Prior to that, Mr. Bailey was with IBM for 15 years at various management levels with a wide variety of computer products.

Dataquest Incorporated
DESIGN AUTOMATION FOCUS CONFERENCE
December 9 and 10, 1985
Palo Alto, California

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A COPY WILL BE MAILED TO YOU WHEN DATAQUEST RECEIVES IT FROM THE SPEAKER.





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WHERE ARE MPU'S GOING?

Mel Thompsen
Associate Director
Semiconductor Industry Service
Semiconductor Application Markets Service
Dataquest Incorporated

Mr. Thompsen is Associate Director of Dataquest's Semiconductor Industry Service and the Semiconductor Application Markets Service. responsible for analyzing the market environment and future technology trends for microprocessors, microcontrollers, and microperipherals. Previously, he held positions as Field Applications Engineer and later as Product Marketing Manager for Zilog, Inc. There he had marketing responsibility for microcomputer boards, memory components, microperipheral components. Mr. Thompsen was also a Product Marketing Manager for Aehr Test Systems and was responsible for marketing dynamic burn-in systems used for reliability testing of digital integrated circuits. He has also held positions as a Senior Design Engineer at Heathkit, and as a Design Engineer at Magnavox, Inc. and at Sylvania Systems Division. Mr. Thompsen received a B.S.E.E. degree from the University of Michigan and an M.S.E.B. degree from Purdue University.

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### NEW DIRECTIONS IN SILICON

Semiconductor Industry Service
Dataquest Incorporated

TWO DRIVING FORCES IN THE SEMICONDUCTOR INDUSTRY HAVE BEEN THE ABILITY TO PUT EVER-INCREASING NUMBERS OF TRANSISTORS ON A SINGLE DIE AND THE ABILITY TO MANUFACTURE THOSE DICE FOR LOWER AND LOWER COSTS.

### PHYSICAL PARAMETER CHANGES FROM 1959 TO 1975

PARAMETER

**CHANGE** 

**FEATURE SIZE** 

11% DECREASE PER YEAR

COMPONENTS/UNIT AREA

INCREASE 8.7 TIMES PER

DECADE

DIE AREA

9% INCREASE PER YEAR

COMPONENTS/CHIP

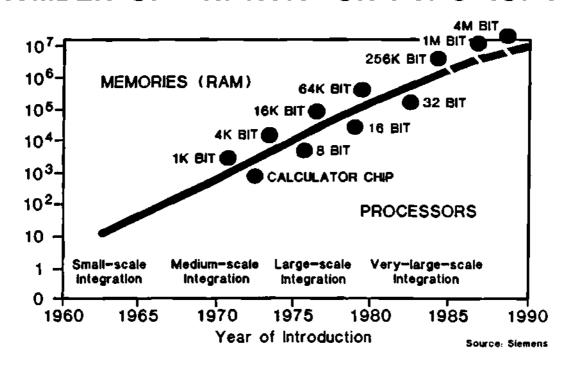
INCREASE 5.7 TIMES PER

DECADE

THE NUMBER OF COMPONENTS PER CHIP HAS INCREASED BY A FACTOR OF 49 EACH DECADE.

Source: DATAQUEST

### NUMBER OF TRANSISTOR FUNCTIONS



### SCIENTISTS HAVE PREDICTED THAT BY 1999, THE INDUSTRY WILL BE ABLE TO PUT A BILLION TRANSISTORS ON A CHIP.

### A BILLION TRANSISTORS REQUIRES TRANSISTORS WITH 0.3 TO 0.4u CHANNEL LENGTHS.

TRANSISTORS WITH 0.5u CHANNEL LENGTHS ARE ALREADY WORKING IN THE LABORATORIES.

### A BILLION TRANSISTORS IS:

- 64 TO 125 MEGABYTES OF ROM
- 32 MEGABYTES OF DRAM
- 8 MEGABYTES OF SRAM

### 5 TO 10 MILLION LOGIC GATES

100K GATES - 1 CPU

A BILLION TRANSISTORS IS A FEW MAINFRAMES PER CHIP

4,000	68020 MICROPROCESSORS
1,000	VAXs
200	AMDAHL 580s
100	SIERRAS
20	CRAY lis

Source: DATAQUEST

### FUTURE INTEGRATED CIRCUITS

- REDUNDANCY
- SELF TEST AND DIAGNOSTIC
- ADAPTIVE CIRCUITS
- SELF REPAIR?

### **FUTURE WORKSTATIONS**

- PRODUCTIVITY
- MASSIVE CELLS
- EXPERT SYSTEMS
- HUMAN INTERFACE
- SIMULATION

# NEW DIRECTIONS IN SILICON

# MEMORY MICROPROCESSORS GALLIUM ARSENIDE

# NEW DIRECTIONS IN SILICON

MEMORY
MICROPROCESSORS
GALLIUM ARSENIDE

# NEW DIRECTIONS IN SILICON

# MEMORY MICROPROCESSORS GALLIUM ARSENIDE

### 32-BIT MICROPROCESSORS

NATIONAL SEMICONDUCTOR

**MOTOROLA** 

AT&T

**TEXAS INSTRUMENTS** 

**FAIRCHILD** 

**INMOS** 

INTEL

**ZILOG** 

32032, 32332

68020

32100, 32200

32032

**CLIPPER** 

**TRANSPUTER** 

80386

Z80000

Source: DATAQUEST





UNIFIED DESIGN-IS IT FOR REAL?

James E. Solomon
President and Chief Executive Officer
SDA Systems

Mr. Solomon is President, Chief Executive Officer, and founder of SDA Systems. Prior to founding SDA, he was responsible for the development of several major product families at National Semiconductor Corporation. These included digital signal processing, data acquisition, telecommunications, Bi-Fet, and other analog product families. Mr. Solomon received a B.A. degree and a Master's degree in Electrical Engineering from the University of California at Berkeley. He is an IEEE Fellow and holds 23 patents in various electronic areas.

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# Unified Design - Is It Real?

Jim Solomon SDA Systems



### **Outline**

- 1. Tomorrow's ASIC
- 2. The Productivity Issue
- 3. Super-Chip Design Methods
- 4. Unified Design
- 5. How Big is the Business?
- 6. Where is the Business Going?

### What Is Tomorrow's ASIC?

The State-of-the-Art:

1.5 Micron CMOS, \$500 wafers

Today: 500,000 Transistors/Chip

COST/CHIP = \$50

# Super-Chip from View of Board Designer:

- Economics are Overwhelming
  - Cost, Size, Performance
- But Needs Quick Turn-Around, Low Risk

## The ASIC Productivity Issue

For a 1,000,000 Transistor Chip:

- Can No Longer Design 4 Transistors/Day
  - 1000 Man-Years/Chip
- Gate Array and Standard Cell Break Down
- Need New Design Method

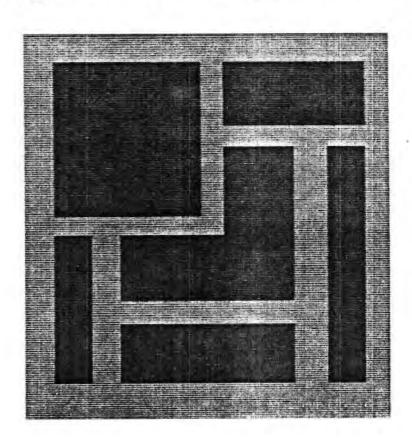
# The Essence of Super-Chip Design:

- Let Designer Work at High Level
  - Work with Large Well Understood Blocks
  - Details Handled Automatically

# The Super-Chip Design Method: Macro-Cell

### The Key Tools:

- Block Compilier
- Block Place and Route
- Functional Simulate



# What Does a Macro-Cell System Look Like?

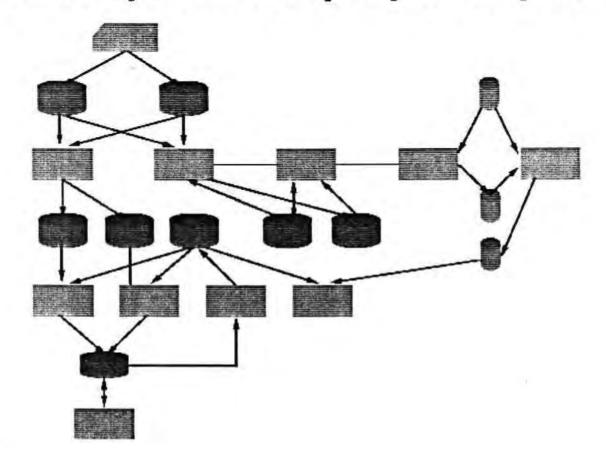
### For the System Designer:

- Schematics and Simulation
- ALL Details of IC Design Hidden
- He Won't Pay Today's Prices for Mask Details
- The System is 1 to 2 Years Away

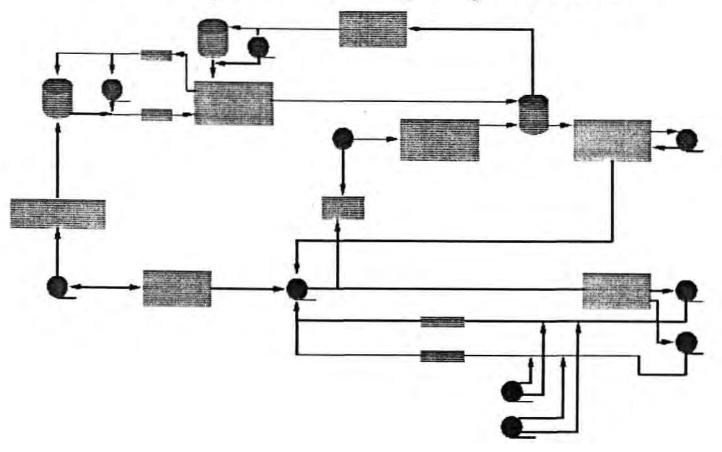
# The Macro-Cell CAD System for the Foundry

- Library Development System
- Automatic Generation of Layout
- Modeling and Simulation

# CAD System Company Y - Japan



# CAD System Company X - USA

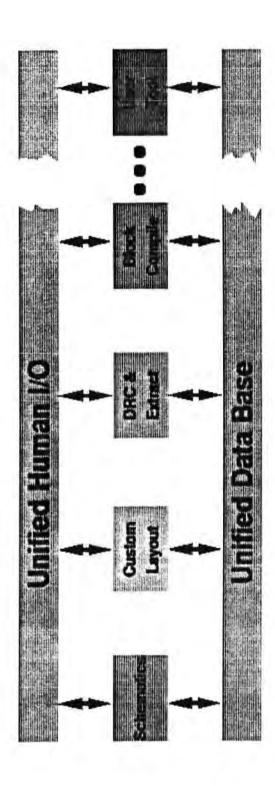


# Does it Really Matter if the System is Unified?

# For Automated Million Transistor Design, Unification is Critical:

- Huge Data Bases
- Fast Data Flow Between Tools
- Unified Human Interface
- The Designer is Completely Reliant on Design System

The New ASIC Design System



# People Want Companies to Fit Into Buckets:



- No ASIC
- Not Unified
- PCB Focus



- Unified Framework
- Solid Library Support
- Macro-Cell
- Standard Cell

"Compiler" Companies



- Narrow Technology
- Weak Library Tools

# Worldwide Revenues for ASIC Design Systems Capacity Calculation

### For:

Chip Revenues 1986-88: \$17 Billion

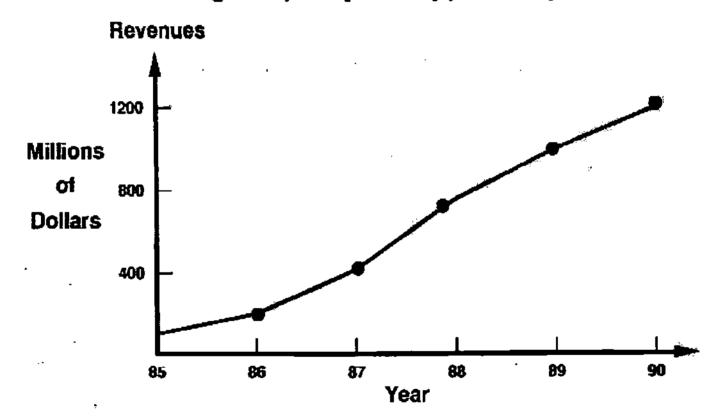
**45K Designs** 

5 Man-Mo/Design

\$ 60K ASP per System

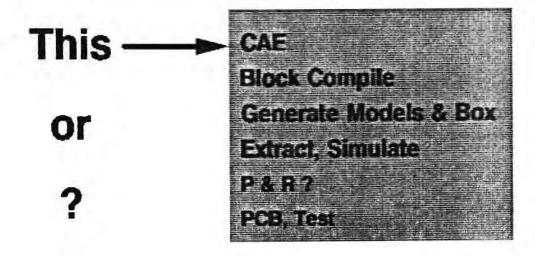
Total 3-Year Design System Revenues: \$ 754 Million

# Worldwide Revenues for ASIC Design Systems Based on Design Capacity to Support Chip Revenues



# A Big Question:

What Exactly Will the System Designer's Workstation Include?



# Summary

- System Needs & ASIC Technology are Driving Large ASIC's
- Large ASIC's Force New Design Styles
- Current Foundry Tools are Inadequate for Big Chips
- Initial ASIC CAD Opportunity: Foundries
- System Houses Buy Simplified Version of Foundry System



# Dataquest BB a company of The Dun & Bradstreet Corporation

ASIC, USIC, or CSIC?

Douglas G. Fairbairn
Vice President of Design Technology
VLSI Technology Incorporated

Mr. Pairbairn is the Vice President of Design Technology at VLSI Technology Incorporated (VTI). He was a founder of VTI in 1980, and is currently responsible for all IC design tool development, marketing, and support. Before founding VTI, he was founder and publisher of VLSI Design Magazine, which was sold to CMP Publications in 1983. Mr. Fairbairn was with Xerox Palo Alto Reserach Center from 1972 until 1980. While at Xerox, he served as Architect Project Manager for the development of the first 16-bit portable computer and for an advanced office terminal system.

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Palo Alto, California

# THE AGE OF PRODUCTIVITY... DESIGN ALTERNATIVES BECOME SOLUTIONS Dataquest Focus Conference

# THE ASIC AND CAE REVOLUTIONS: THE FIVE YEAR MILESTONE

DOUGLAS G. FAIRBAIRN VLSI TECHNOLOGY, INC.

**DECEMBER 10, 1985** 



### A SHORT HISTORY...

- MAJOR ASIC AND CAE COMPANIES ESTABLISHED 5 YEARS AGO.
- ESTABLISHED SEMICONDUCTOR AND CAD COMPANIES ENTERED MARKET IN 1983-85
- SOME PRODUCTS HAVE ALREADY BEGUN TO LOOK LIKE COMMODITIES
- FIRST ROUND OF DROP OUTS AND CONSOLIDATION COMPLETE



### ASIC VS. MICROPROCESSOR REVOLUTION

- MICROPROCESSOR TECHNOLOGY LEADERSHIP WAS ESTABLISHED BY NEW COMPANIES
- MICROPROCESSOR MARKET FOCUS WAS SHARPER IN NEW COMPANIES
- ESTABLISHED COMPANIES ADDED MICROPROCESSORS TO COMPLEMENT PRODUCT LINES; FEW HAVE BEEN SUCCESSFUL

ASIC IS FOLLOWING THE SAME PATTERN

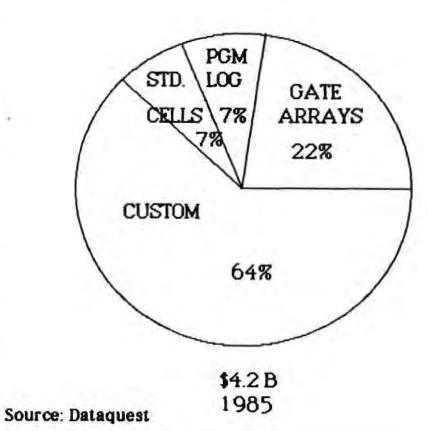


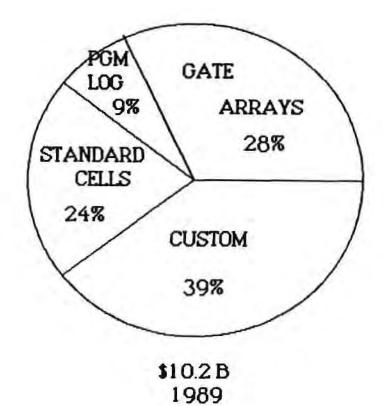


# WHAT OPPORTUNITIES AND CHALLENGES

# AWAIT US DURING THE NEXT 5 YEARS?

#### THE OPPORTUNITY





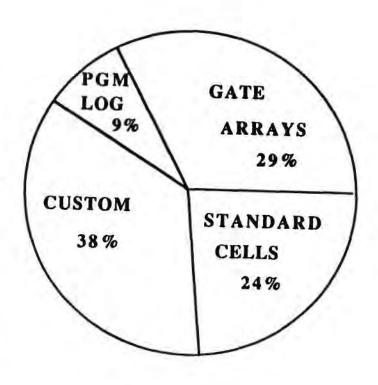


#### CHALLENGES: PHYSICAL DESIGN AND TEST

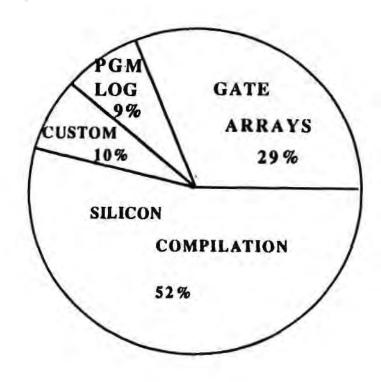
- WHAT METHODOLOGIES WILL DOMINATE?
- WHO WILL SUPPLY THE SOLUTIONS?
- WHAT WILL BE THE RELATIONSHIP BETWEEN CAE AND ASIC VENDORS?
- WHO WILL GUARANTEE THE RESULTS?



#### SILICON COMPILERS WILL DOMINATE ASIC



1989 DATAQUEST



1989 VTI



#### WHO WILL BE THE COMPILER SUPPLIERS?

- MOST SUPPLIERS WILL BE SEMICONDUCTOR COMPANIES
  - SUPPLYING BUILDING BLOCKS IS TRADITIONAL ROLE
  - CLOSEST TIE TO PROCESS TECHNOLOGY
  - STRONG DESIGN SKILLS
  - GUARANTEES TO USERS
- CHALLENGE: ATTRACTING AND INTEGRATING STRONG SOFTWARE PERSONNEL
- ALL MAJOR SEMICONDUCTOR COMPANIES WILL BE SUPPLIERS



## SILICON COMPILATION SYSTEMS HIGH LEVEL USER REQUIREMENTS

- EVOLUTIONARY VS. REVOLUTIONARY

  GATE ARRAYS --> STD. CELLS --> SILICON COMPILATION
- OPEN SYSTEM SUPPORT FOR
  - HAND-CRAFTED CUSTOM
  - STANDARD CELLS
  - MEGACELLS
  - MEMORIES (SRAM, E<sup>2</sup>, ETC.)
  - ANALOG
- SECOND SOURCING (FOR QUOTES, NOT FOR SILICONI)



#### WHAT WILL MAKE COMPILERS TAKE OFF?

- USER CONFIDENCE
- WIDER AVAILABILITY
- INTEGRATION WITH CAE
- FULL AUTOMATION

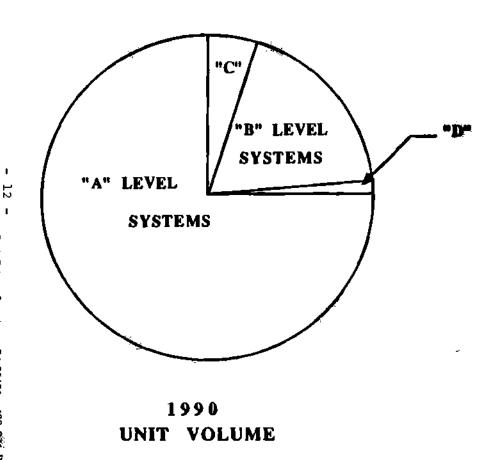


## ASIC AND CAE ARE ENTERING A NEW DOMAIN...PUSH-BUTTON PHYSICAL DESIGN

- AVAILABLE FOR GATE ARRAYS AND STANDARD CELLS
- FULLY AUTOMATED COMPILER-BASED DESIGN WILL FOLLOW
- WIDESPREAD ACCEPTANCE HAS NOT BEEN PROVEN



#### PROJECTED MARKET SEGMENTATION: ASIC DESIGN TOOLS



A SCHEMATIC ENTRY AND SIMULATION

B "PUSH-BUTTON" PHYSICAL DESIGN

C PHYSICAL DESIGN AT SYMBOLIC & FLOOR PLAN LEVELS. NO XISTOR DESIGN.

D IC DESIGN AT TRANSISTOR AND POLYGON LEVELS

#### TEST PROGRAM DEVELOPMENT CHALLENGE

- LACK OF KNOWLEDGE OF TEST-RELATED ISSUES
  - BUILT-IN TEST
  - AUTOMATIC TEST GENERATION
  - FAULT GRADING
- AVAILABLE TOOLS HAVE BEEN
  - TOO SLOW AND EXPENSIVE
  - NOT ADEQUATE FOR THE JOB
  - TOO DIFFICULT TO USE
- CRITICAL QUALITY ISSUE FOR ASIC VENDORS



# USER DESIGN WILL REQUIRE NEW LEVEL OF COOPERATION BETWEEN ASIC AND CAE VENDORS



#### RAPID CHANGE IN TOOLS AND LIBRARIES

#### TOOLS (WORKSTATION VENDOR)

- DESIGN TIME
- EASE OF USE AND REDUCED LEARNING TIME
- NEW COMPUTING TECHNOLOGY

#### LIBRARIES (ASIC VENDOR)

- DENSITY
- SPEED
- ANALOG AND ELECTRICALLY ERASEABLE

171973

#### CRITICAL TOOL ← LIBRARY INTERFACES

DESIGN TOOL LIBRARY ELEMENT

SIMULATOR TIMING MODEL

FAULT MODEL

PHYSICAL DESIGN CELL GEOMETRY

WIRE SPACING/CONTACT RULES

POWER DISTRIBUTION LATCH UP/ESD RULES

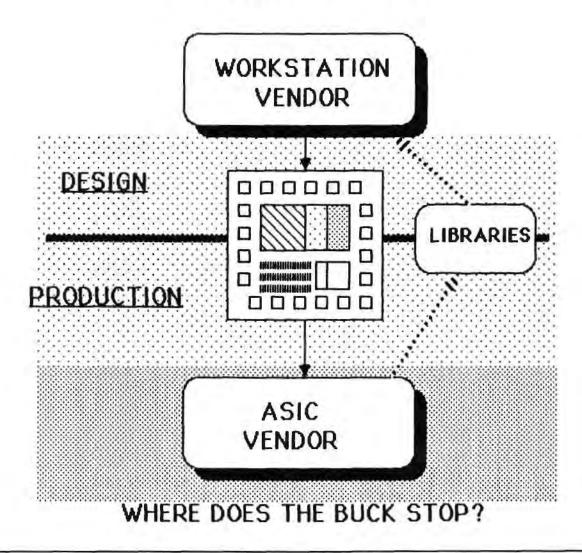
VERIFICATION TOOLS GENERAL LAYOUT TOOLS

**ELECTRICAL RULES** 

#### NO ACCEPTED STANDARDS



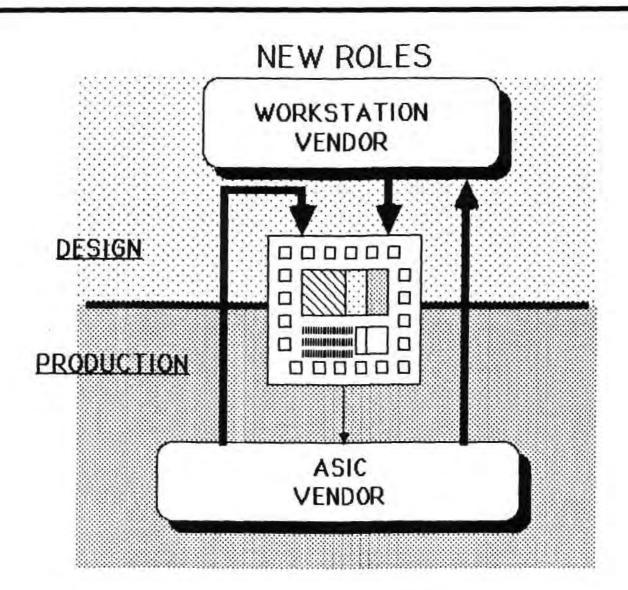
#### **CONVENTIONAL ROLES**



## REALIZING THE OPPORTUNITY MEANS MEETING THE CHALLENGES

- USERS WANT THE LATEST TECHNOLOGY AVAILABLE IN THE MOST FLEXIBLE ENVIRONMENTS
- USERS WANT TO CONCENTRATE ON THE LOGICAL DESIGN
- USERS WANT GUARANTEES THAT THEIR DESIGNS
  - CAN BE MANUFACTURED COST EFFECTIVELY
  - WILL MATCH THEIR SIMULATED RESULTS
  - ARE FULLY CHARACTERIZED AND TESTED







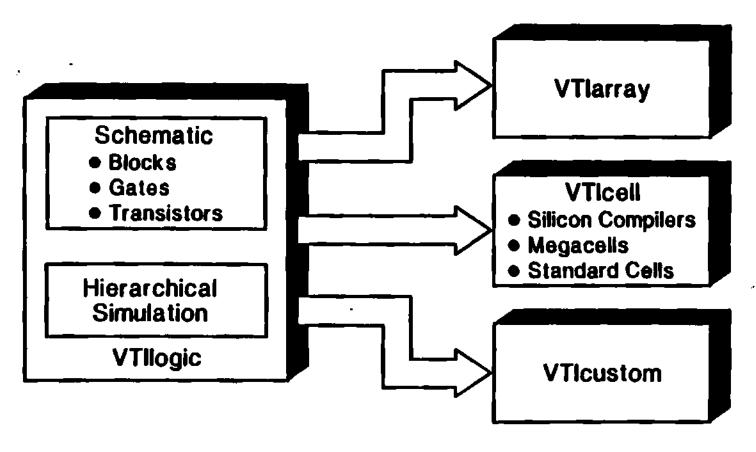
#### **VTI OFFERS AN ALTERNATIVE:**

- LEADER IN ASIC DESIGN TECHNOLOGY
- WORLD CLASS WAFER FAB WITH GUARANTEES
- TOTAL SERVICE ORIENTATION

SILICON AND SOFTWARE FROM THE SAME VENDOR



#### **VTI IC DESIGN TOOLS**





#### **VTI'S VLSI DESIGN SYSTEM OFFERS**

- CLOSEST TIE WITH THE LATEST TECHNOLOGY
- EASY-TO-USE PHYSICAL DESIGN TOOLS
  - PUSH-BUTTON GATE ARRAY DESIGN
  - PUSH-BUTTON STANDARD CELL DESIGN
  - SEMI-AUTOMATED COMPILER-BASED DESIGN
  - COMPILER GENERATION TOOLS
- SIMPLIFIED TEST PROGRAM DEVELOPMENT
- GUARANTEED RESULTS
  - SIMULATION
     DESIGN-RULE CHECKS







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THE IMPACT OF SILICON COMPILERS ON PRODUCTIVITY

Gordon Ruenster
President
Seattle Silicon Technology

Mr. Kuenster is President of Seattle Silicon Technology, which was formed in April 1983. Before joining Seattle Silicon, he was involved in several venture capital investments in northwest high-technology companies. Prior to that, he was President of Advanced Technology Laboratories. After ATL's acquisition by Squibb Corporation, he became President of Squibb Medical Systems Group and a Director of the parent corporation. Mr. Kuenster received a B.S.E.E. degree from Illinois Institute of Technology and serves on the Boards of Directors of Opcon, Quantum Medical Systems, Pacific Science Center, and Washington Technology Center.

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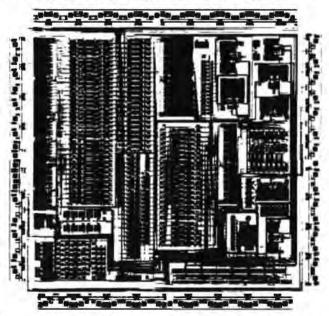
#### THE IMPACT OF SILICON COMPILERS ON PRODUCTIVITY

Gordon Kuenster
President
Seattle Silicon Technology
12356 Northup Way
Bellevue, WA 98005

The advent of integrated circuits some twenty years ago caused an industrial revolution of the same order as many of the major inventions of the last century. These circuits and their impact on the computer industry have fostered increasingly rapid advances in diverse fields from aerospace to medicine which would not have otherwise been possible. Generally these circuits have been applied as mass produced standard parts in aggregation to build computers, controllers, telecommunication devices and all other electronic devices. More efficient custom circuits have been developed for those applications where the production volume and high development expense have justified their use. Recently, however, it has been possible to quickly design very specific circuits for lower volume applications through the use of structured arrays, gate arrays and standard cells. These methods tend to break down however, when larger or more diverse circuits are required. The recent introduction of more advanced design tools called Silicon Compilers is allowing the designer to take advantage of the productivity of very specific integrated circuits for sophisticated applications, even at very low production volumes.

Silicon Compilers represent a new design methodology for Application Specific Integrated Circuits (ASICs). This new design methodology enables designers to achieve densities and complexities comparable to full custom using techniques similar to gate arrays and standard cells. The result is that a high-level design can be quickly implemented and evaluated without requiring detailed IC design knowledge.

As the typical size of the Application Specific Integrated Circuits (ASIC'S) surpasses 10,000 gates, conventional design methods break down. Just as it is almost impossible to count to 10,000 without making an error, it is also very cumbersome to design and document a design with a detail gate level description of 10,000 gates or more. These detail design descriptions can



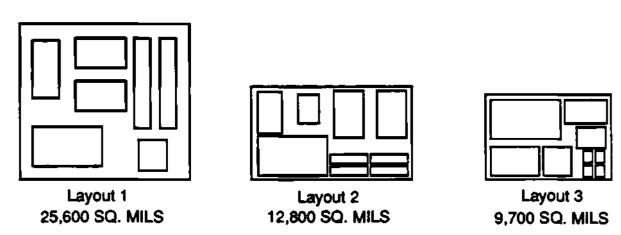
The E-Mu Systems Inc. 50,000 device digital sound emulator chip was originally compiled for a 3µ, single metal process. Midway into the routing phase of the design, one of the potential foundries announced the availability of a 2µ double metal process. The designer was able to switch technologies in the middle of the design, a possibility available only to those working with silicon compilation.

\_ IFigure 1

occupy more than one hundred pages of schematic description, compared to a one or two page description of a compiled circuit. As in the case of conventional word processors, making a design change with a silicon compiler is simple and can be accomplished without having to recheck the entire circuit. As designs progress to the 50,000 gate level and up, high level design methods become mandatory (see figure 1).

With more conventional methods of geometry layout, a skilled integrated circuit designer can lay down approximately ten transistors on an average day. Using the currently available Silicon Compilers, a novice can lay down thousands of transistors per hour. These transistors can also be assured of being design-rule correct by construction. This very rapid geometry construction permits the integrated circuit designer to try many alternatives, comparing the performance and economic parameters.

Experiments with the Seattle Silicon compilers have demonstrated repeated decreases in silicon area from repeated trials. Experiments have shown that three or four trials usually achieve optimum results. In the experiments, the optimum architecture or layout was 30 to 40 per-cent smaller than the initial trial (see figure 2). In fact, user gratification was so high, it was shown that engineers did not want to stop experimenting with designs until subsequent trials actually resulted in layouts that were larger than the previous trials. Given the capability of silicon compilers, it may be necessary for engineering management to impose more discipline in the design process to cause the integrated circuit designers to stop designing when the resultant layout is adequate, considering performance and design cost trade-offs.



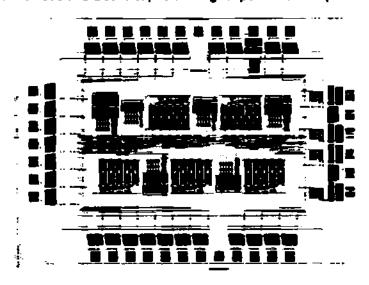
These figures illustrate how a designer using silicon compilation can optimize chip size through architectural experimentation. In the above example a single designer spent three days to optimize a multifunction automobile light controller chip

#### Figure 2

Although the productivity improvements for skilled designers are impressive, the more important capability of silicon compilers may be the extension of this capability to lessor skilled engineers. Given that there are some 3 to 5 thousand integrated circuit designers in the world, the extension of this capability to a large new group of engineers makes custom integrated circuits available to a much larger group of users. The extension of low cost custom integrated circuits to new groups allows small companies and those companies who may have been low-tech to leap into a competitive position with the larger or more advanced companies who have always considered custom integrated circuits for appropriate applications. In a real sense, silicon compilers increase the competitiveness of a very large number of electronics companies. This increased competiveness will certainly have a beneficial impact on consumers who will now have a greater group of suppliers to choose from. This increased competiveness will certainly create an array of products that will be unprecedented. Product life cycles will shrink and the performance and economic advantages of much more productive designs will be generally available. All companies will be compalled to use these more productive tools to remain competitive. It should be pointed out that these tools are improving and gaining capability at a rapid pace. Therefore it can be expected that these effects will be even more dramatic in the future.

Another impact that could be expected is the creation of new start-up companies with relatively little capital. A new start-up could consist of only a few engineers capable of creating very sophisticated electronic equipment without teams of technicians or draftsmen. Computer verification is rapidly replacing breadboard testing permitting the creation of new companies with a minimum of capital.

When breadboarding is called for, these tools allow breadboarding in silicon instead of wire-wrap or multi-layer boards. This has cost advantages as well as performance advantages, particularly when high speed operation is required. In many cases, silicon breadboarding is less expensive than conventional methods and also is capable of higher performance operation (see figure 3).



Sigma Research developed the above chip as an implementation of a Residue Number System for high-speed digital signal processing. TTL parts offered no clear circuit design models. Therefore, the designer combined PLAs and adders of various sizes and codings, then compiled and simulated the trial designs. This "silicon breadboarding" led to a chip which incorporates six PLAs and five 5-bit adders.

#### Figure 3

The most productive aspect of sillcon compilers, however, may be the increased capability for designers to put an entire system (including memory and analog) or major part of a system on a single chip. Reducing a system to a single chip improves performance, reliability and size, and lowers cost. Incorporating all of the various circuit elements on the single silicon chip also eliminates the need for many of the package pins. Because the presence of the pins and the required buffers inherently degrades performance, elimination of the requirement automatically improves the circuit capability. Increased functionality, shorter design cycles and lower costs are all benefits of Silicon Compilation, the new ASIC design methodology.





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THE GLOBAL PRODUCTIVITY IMPERATIVE

Aryeh Pinegold President Daisy Systems Corporation

Mr. Finegold is a founder of Daisy Systems Corporation, and has served as President and Chief Executive Officer of the firm since its incorporation in August 1980. Before founding Daisy Systems, he spent four years in various engineering management positions at Intel Corporation. Prior to that, he spent six years at Elbit Computers Ltd., where he held several engineering positions. Mr. Finegold received a B.S. degree from Technion Institute—Israel Institute of Technology.

Dataquest Incorporated
DESIGN AUTOMATION FOCUS CONFERENCE
December 9 and 10, 1985
Palo Alto, California

#### **DAISY SYSTEMS**

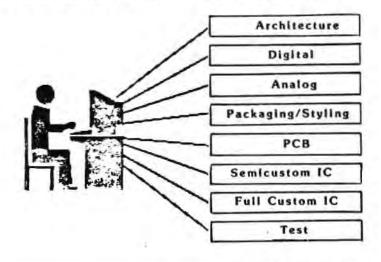


### Delivering Innovative Solutions To Increase Engineering Productivity

#### **CAE: A CHANGING MARKET**

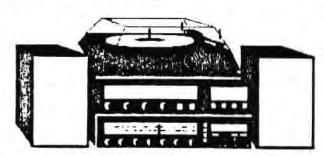
- CAE Recognized as Competitive Necessity
- Purchase Decisions Made at Corporate Level
- Complete CAE Environment Required
- Complete Application Spectrum Needed

## INCREASED PRODUCTIVITY USING COMPLETE APPLICATION SPECTRUM



#### STEREO SYSTEM CONCEPT...

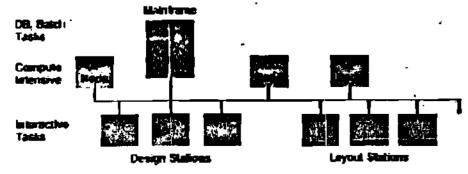
- Modular Building Blocks
- "Create" Your Own System



#### TET APPLIES TO CAE.

- Low Cost PC-Based Design Station
- Fastest Accelerators
- Most Interactive Layout
- General Purpose Computing Platform
- Access to Corporate Mainframe

## THE IDEAL CORPORATE CAE ENVIRONMENT



#### Improved Productivity through

- Same User Interface
- Same Software (Same Results)
- Same Communication/Distributed File System

#### PERSONAL LOGICIAN (DNIX)

- IBM PC AT + Daisy Graphics
- UNIX Operating System
- Remote
   Execution
   Capability

THE DESIGNER'S DREAM...
THE CORPORATE CAE SOLUTION

• Logician VX

#### THE MegaLOGICIAN

- General Purpose Design Automation Accelerator
  - Logic Simulation
  - Timing Verification
  - Fault Simulation
  - Placement and Routing
- Network Resource

#### ROLE OF MAINFRAME ...

- Batch Processing
- Database Management

#### DESIGN MANAGER

- Electronic Database Namagement for Large Designs
- Change Management— Check-Out-Check-in Control
- Freeze and Release Control
- . Three Levels of Protection -Data, Corruption, Access

#### DAISY'S OPEN SOLUTION

Malatrame DEC/IBM VX Hede VX Node Maga Chip Concustons LOGICIAN Board Master Personal LOGICIAN LOGICIAN Chip Moster

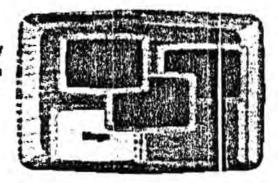
- DAISY-OND; All Over
- · Identical Software (PC, WE, WAX, MF)
- . Access to CAD-CAM-CAE Soles

Design Dubbben Management (COM)

Desirbuted Dalabase Over Ethernet-DECret

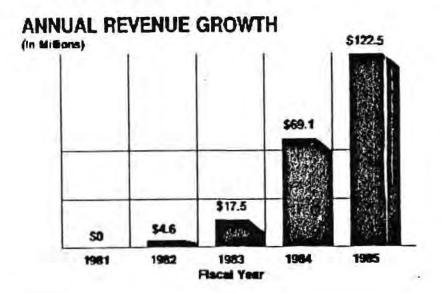
#### DAISY IS OPEN SYSTEMS

- Software Portsbility
- Terminal Emulation
- Remote Execution
- Open Database

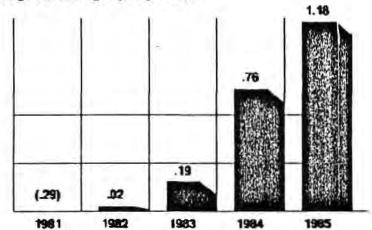


#### KEY TO FUTURE SURVIVAL -GLOBAL PRODUCTIVITY

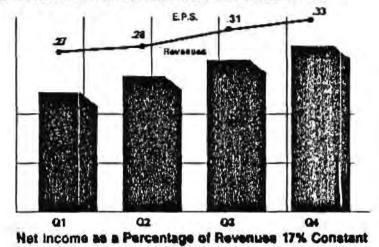
- Integrated CAE Environment
- Complete Application Solution







#### QUARTERLY REVENUE/E.P.S. GROWTH







## PRODUCTIVITY ALTERNATIVES: DESIGN ALTERNATIVES BECOME SOLUTIONS

CONFERENCE WRAP-UP

#### PRODUCTIVITY ALTERNATIVES

#### **HARDWARE**

- COMPUTATIONAL ALIGNMENT
- PCs
- APPLICATION ACCELERATORS
- DECREASING PRICES/INCREASING PENETRATION

#### PRODUCTIVITY ALTERNATIVES

#### SOFTWARE

- HIGHER-LEVEL DESIGNS
- ANALYSIS
- OFFICE AUTOMATION
- DATA BASES
- USER INTERFACE
- ATG

#### PRODUCTIVITY ALTERNATIVES

#### **METHODOLOGY**

- AUTOMATIC ROUTING
- SILICON COMPILATION
- SYSTEMS LEVEL DESIGN
- DISTRIBUTED PROCESSING

#### 1986 CAD/CAM RESEARCH PROJECTS

#### 1986 CAD/CAM RESEARCH PLANS

#### FORECASTS:

- QUANTIFY SIMULATION MARKET
- QUANTIFY APPLICATION ACCELERATOR MARKET
- PUBLISH 1985 ACTUALS AND REVISED FORECAST THROUGH 1990

#### 1986 CAD/CAM RESEARCH PLANS

#### APPLICATION SURVEYS

- EDA END USER
- PRINTED CIRCUIT BOARD
  - END USER
  - SURFACE-MOUNTED DEVICES
  - HYBRIDS
- ELECTROMECHANICAL STUDY
- QUARTERLY FOCUS RESEARCH GROUPS

#### 1986 CAD/CAM RESEARCH PLANS

#### NON-U.S. MARKETS

- EUROPEAN MARKET SHARES AND FORECASTS
- JAPAN END-USER SURVEY
- TAIWAN, KOREA, AND SINGAPORE FAR EAST MARKETS

## 1986 CAD/CAM RESEARCH PLANS

#### GENERAL BUSINESS

- CHANNELS OF DISTRIBUTION STUDY
- QUARTERLY CAD/CAM MARKET REVIEWS
- DEMOGRAPHICS

