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Focus Conference

"Workstations"
The Evolution of an Industry

Sponsored by the
CAD/CAM Industry Service

August 13 and 14, 1984
Boston Marriott Burlington Hotel
Burlington, Massachusetts

Dataquest

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San Jose, California 95131
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Telex: 171973

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FOCUS CONFERENCE AGENDA

"Workstations"

The Evolution of an Industry

Sponsored by the CAD/CAM Industry Service

August 13 and 14, 1984
Boston Marriott Burlington Hotel
Burlington, Massachusetts

MONDAY, AUGUST 13

8:30 a.m.	**Workstation Industry Overview** James Newcomb, Director Design and Manufacturing Automation Group Dataquest Incorporated
9:20 a.m.	**Architectures, Graphics, and Performance** David Burdick, Industry Analyst CAD/CAM Industry Service Dataquest Incorporated
10:10 a.m.	Coffee Break
10:30 a.m.	**Workstations, The Transfer of Technologies** David Nelson, Senior Vice President Apollo Computer Corp.
11:30 a.m.	Lunch
1:00 p.m.	**The Role of VLSI Technology in the Workstation Marketplace** James Clark, Chief Technical Officer Silicon Graphics Incorporated
1:50 p.m.	**The Role of Proprietary Architectures in Workstation Design** David Folger, President Ridge Computer Company
2:40 p.m.	**Systems Architecture—Utilizing Standards** Scott McNeally, President Sun Microsystems
3:30 p.m.	**The Utilization of Artificial Intelligence in Developing User Interfaces and Next Generation Workstations** Richard Rifenburgh Chairman of the Board/CEO Perq Systems Corp.
4:20 p.m.	**Communications Integration** Thomas Bredt, Vice President and Director Telecommunications Industry Service Dataquest Incorporated
5:30 to 7:00 p.m.	Cocktail Party

TUESDAY, AUGUST 14

8:30 a.m.	**Network Configurations** Peter Shaw, President Syte Technologies
9:20 a.m.	**Start-up: Building the Management Team** Arthur Campbell, President Mosaic Technologies
10:10 a.m.	Coffee Break
10:30 a.m.	**Product Mix: The Integration of Internal and External Technologies** Jerry Rotds, Sr. Vice President Sales and Marketing Gould Incorporated
11:20 a.m.	**Marketing: The OEM Approach** Donald McDougall Vice President and General Manager Data General Corporation
12:10 p.m.	Lunch
1:30 p.m.	**Workstations: Flexible Systems Architecture in a High-Performance Graphics Environment** Dennis Peck, President Saber Technology
2:20 p.m.	**Display Technologies: Impact on Workstations** Richard Fichera Director of Marketing Raster Technologies Incorporated
3:10 p.m.	**Application-Specific Hardware—A Component Approach** Arthur Collmeyer, President Weitek Corporation
4:00 p.m.	**Conference Wrap-Up** James Newcomb, Director Design and Manufacturing Automation Group Dataquest Incorporated

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CAD/CAM FOCUS CONFERENCE EVALUATION QUESTIONNAIRE

Burlington, Massachusetts
August 13–14, 1984

Thank you for attending our CAD/CAM Industry Focus Conference. Would you please assist us in planning our next conference by completing and returning this questionnaire?

1. Please rate each presentation on a scale of 1 to 10 (where 10 is highest in terms of your approval):

	CONTENT (1 to 10)	DELIVERY (1 to 10)	COMMENTS (Use reverse side if necessary)
Newcomb, *Workstation Industry Overview*			
Burdick, *Architectures, Graphics, and Performance*			
Nelson, *Workstations, Transfer of Technologies*			
Clark, *Role of VLSI Technology in the Workstation Marketplace*			
Folger, *Role of Proprietary Architectures in Workstation Design*			
McNeally, *Systems Architecture—Utilizing Standards*			
Rifenburgh, *Utilization of Artificial Intelligence in Developing User Interfaces and Next Generation Workstations*			
Bredt, *Communications Integration*			
Shaw, *Network Configurations*			
Campbell, *Startup: Building the Management Team*			
Rotds, *Product Mix: Integration of Internal and External Technologies*			
McDougall, *Marketing: The OEM Approach*			
Peck, *Workstations: Flexible Systems Architecture in a High-Performance Graphics Environment*			
Fichera, *Display Technologies: Impact on Workstations*			
Collmeyer, *Application-Specific Hardware — A Component Approach*			

2. How would you rate the conference facilities (1 to 10)?

   Location _____ Guest Rooms _____ Meals _____ Meeting Rooms _____ Recreational Facilities _____

3. How would you rate the service quality and staff attitude (1 to 10)?

   The hotel staff _____ DATAQUEST staff _____

(over)

4. What did you like most about the Focus Conference? _____

_____

5. What did you like least about the Focus Conference? _____

_____

6. Suggestions for improving the Focus Conference: _____

_____

7. Topics that would be of interest to you for the next Focus Conference: _____

_____

8. Do you prefer _____ longer, _____ shorter, or _____ the same length conference?

9. Do you prefer _____ more, _____ less, or _____ the same amount of free time?

10. Your primary interest in the display and graphics terminal industry is as a: _____ Manufacturer

_____ Service Vendor _____ User _____ Financial Analyst _____ Other _____
(Please Specify)

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CAD/CAM INDUSTRY CONFERENCE

August 13 and 14, 1984

Burlington, Massachusetts

Final List of Attendees

A T & T Bell Labs	Andy Nagle Supervisor
	Basant R. Chawla Department Head
Adage, Inc.	Clarence A. Tilger Director of Market Planning
Air Products and Chemicals	Timothy Pickering Technology Assessment Analyst
American Micro Systems	Gary Miles CAD Planning Manager
Analog Design Tools, Inc.	Richard N. Lanham Vice President, Marketing & Sales
Apollo Computer	David Nelson Senior Vice President
	Debra Sheedy
	John Cencioso
	Lou Reynolds Product Group Manager
	Stephen Weinberger Director Market Development
	Win Burke Director of Product Marketing

Applicon	Francis Donlan Director of Engineering
	Jeffery Simon Manager Systems Marketing
	Richard Miller Director of Marketing
Arthur Young and Company	George Southwick Partner
Bank of America	Al Schumer Assistant Vice President
	Dave Woonton Assistant Vice President
Bishop Graphics	Loren T. Bersack Director Product Development
Boeing Aircraft Corporation	Richard Hedlund Electronic CAD Manager
Burr, Egan, Deleage & Co.	Esther B. Sharp Associate
CAD/CAM Specialists, Inc.	Dan Garms Vice President
	Michael W. McDonald President
CIE Terminals	Roger Budris Manager Advanced Planning
CPT Corporation	Pamela A. Jensen Senior Market Research Specialist
Cadmus Computer Systems	Jeff Singer Vice President, Engineering
CalComp	Craig Montgomery Product Line Manager
	Mike Watterson Product Line Manager
	Wendy Abramowitz
	Janifer Jones

Cericor Incorporated	David Bailey President
	William Shea Regional Sales Manager
Ciprico Incorporated	Bruce Brunette Director, Marketing
Computervision	Leslie Swanson Product Specialist
	Robert Horn
	Robert Resslhuber Product Specialist
	Arnie Epstein Director, Systems Architecture
	Hank Kellogg Marketing Analyst
	James Cook Director of Technical Research
	Jitendira Singh
	Mark Krentzman
	Neil Sawe
	Owen Knox
	Stephanie Marrus
Data General Corporation	Donald McDougall Vice President & General Manager
Dataquest Incorporated	Beth Tucker Industry Analyst
	Bob Smith Marketing Manager
	Brad Smith Associate Director

	Chuck Kanupke Vice President TCIS East Coast
	Dave Burdick Industry Analyst
	Don Johnson Research Associate
	Eileen Barth Research Associate
	Frank Florence Marketing Manager
	H. Edward White Associate Director OAS
	Irene Barth Librarian
	Jim Newcomb Director
	Kelly Leininger Research Clerk
	Pamela Shook Group Administrator
	Thomas Bredt Vice President and Director
	Wendy Ledamun Research Associate
Diconix	Ernest Truax Manager Product Planning
Digital Equipment Corporation	Barry Reynolds Finance Business Manager
	Dorothy Rado Business Manager Marketing
	John Clarke
	John Dimack Engineering Operations Manager
	Libby Aston Engineering Supervisor

	Nick Johnson Technologist
	Norm Tripp Product Manager
	Prakash Bhalerao Engineering Group Manager
	Roslyn Morvay Product Marketing Manager
	Tim Yeaton Finance Manager
	Susan Marie Marketing Analyst
Eastman Kodak Company	John C. Batterson Planning Specialist
Edge Computer Corporation	J. Douglas Crawford Director, Sales
Electronic Business	Cindy A. Thames Senior Editor
Evans and Sutherland	Edward C. Cheadle CAD/CAM Specialist
Fairchild	John Andrews CAD Staff Engineer
GenRad Incorporated	S. Russel Craig Director, Corporate Marketing
General Computer Company	Kevin Curran President
	Pax Goodson Marketing Manager
General Electric Company	Dale W. Rowe General Manager 66TD
	James Whitten Manager Design Engineering
	Marshall Kidd Manager Technical Analyst
	Robert W. Baeder Staff Executive

Gould Incorporated	Dana A. Gauthier Manager Planning & Financial Services
	Joseph Heaney
Hewlett-Packard	Billy Abrams
	Alan Benjamin Product Marketing Engineer
	Jim Lyons Product Marketing Manager
IBM	A. C. Ewing Graphics Adminstrator
	L. Wilcox Product Planner
	Richard Ma Senior Marketing Analyst
	Steve Vaughn Advisory Engineer
ICM, Incorporated	Brian W. Kirschner Vice President, Research & Development
	Dr. L. L. Barinka Preisdent
IDS Growth Spectrum Advisors	Michael F. Guilford Senior Analyst
Impell Corporation	Pat Strange Director
Intel Corporation	Sudhir Bhagwan Assistant General Manager
Jennison Associates	David T. Poiesz Vice President
Jupiter Systems, Inc.	Jon G. Peddie President
LSI Logic Corporation	Richard Perry Software Marketing Manager

Lexidata Corporation	Forrest Gasik Manager, Forecasting
	Shelly Lowenthal Engineering Manager
Loomis, Sayles & Company	Jaye E. Morency Securities Analyst
Matra Datavision	John Keller Manufacturing Manager
Mayfield Fund	Grant Heidrich General Partner
McAuto	Jeff Barnell Hardware Product Manager
Megatek Corporation	Greg Elmassian Senior Engineer
	Susan Harvey Corporate Planning Manager
Mosaic Technology	Arthur Campbell President
	David S. Lobel Board Memeber
Motorola Incorporated	Arthur R. Miller Strategy and Bus. Dev., High End MPU
National Semiconductor	John Payne Marketing Manager
	N. T. Hsu Senior Engineering Manager
Nixdorf	Lorraine Chouinard Product Line Manager
Oak Management Corporation	Carla Haugen Associate
Olivetti Research & Development	Charles Erickson Manager
Omnicad Corporation	Edward J. Morton

Pacific Telesis Group	Bill R. Frazer Director
Paragon Technology	Philip Monego President
Parallax Graphics	Jim A. Summers President
Perq Systems	Richard Cox Director, Marketing Planning
	Jim Gay Vice President, Product Management
Prime Computer Corporation	Barry Wolman Director, Systems Development
	Celia Bland Manager Workstation Marketing
	Edward Vravlick Systems Consultant
	Marvin Miller Product Integration Manager
Prudential Bache Securities	Laura Conigliaro Vice President
	Christine Chien
	Michael Weisberg Director, Technology Research
Pyramid Technology Corporation	Frank Madren Vice President, Marketing
	William Gimple Vice President, Research and Dev.
RCA	J.W. Scherer Manager Product Marketing
Racal-Redac	R. Davis
	Ray Spencer

Raster Technologies	Richard Fichera Director of Marketing
Resolutions Systems Incorporated	Isaac Nassi Vice President
Ridge Computer Company	David Folger President
	Harry Taxin Vice President, Marketing & Sales
Saber Technology	Dennis Peck President
	Don Rector
Sanders Associates	Patty Craig Software Engineer
	Ronald Derby Corporate Marketing Research Manager
Siemens Aktiengesellschaft-Dep E TDV	Wolfram Howein Dipl. - Ing
Silicon Graphics Incorporated	Craig S. Olson Product Manager
	Jim Clark Chief Technical Officer
	Vernon Anderson Chairman
Spectragraphics	John Moreland Director, Marketing
	Ray Barger Vice President, Marketing
Sun Microsystems	Scott McNeally President
Syte Information Technologies	Peter Shaw President
T. Rowe Price	Michael Christodolou

Teradyne	Phil Odence Applications Engineer
Terak Corporation	Tom Zender Director of Marketing
Wang Labs	Dan Miley
	Gary Neil Director, Industry Marketing Programs
	Leigh Herndon
Wayne Kerr	Ken Berquist Vice President
	Ted Sisley Product Manager
Weitek Corporation	Arthur Collmeyer President
	Lynette DeNike Consultant

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Apollo Computer	Anil Gadre
Apollo Computer	David Nelson Senior Vice President
Apollo Computer	Linda Sartes
Apollo Computer	Lou Reynolds Product Group Manager
Apollo Computer	Stephen Weinberger Director Market Development
Apollo Computer	Win Burke Director of Product Marketing
Applicon	Francis Donlan Director of Engineering
Applicon	Jeffery Simon Manager Systems Marketing

Applicon	Richard Miller Director of Marketing
Arthur Young and Company	George Southwick Partner
Bank of America	Al Schumer Assistant Vice President
Bank of America	Dave Woonton Assistant Vice President
Boeing Aircraft Corporation	Richard Hedlund Electronic CAD Manager
CAD/CAM Specialists, Inc.	Dan Garms Vice President
CAD/CAM Specialists, Inc.	Michael W. McDonald President
CAE Terminals	Roger Budris Manager Advanced Planning
Cadmus Computer Systems	Jeff Singer Vice President, Engineering
CalComp	Craig Montgomery Product Line Manager
CalComp	Mike Watterson Product Line Manager
CalComp	Rich Peters Vice President, Business Development
Calma Company	James Mannos Director, Systems Engineer
Calma Company	Tom Teeters Director of Corporate Marketing
Calma Company	Van Lewing Vice President, Electronics
Calma Company	William Blasdell Vice President System Programs

Century Capital Assoc.	Arthur Vitolo
Ciprico, Incorporated	Bruce Brunette Director, Marketing
Computervision Corporation	Arnie Epstein Director of Systems Architecture
Computervision Corporation	Hank Kellogg Marketing Analyst
Computervision Corporation	James Cook Director of Technical Research
Computervision Corporation	Mark Krentzman
Computervision Corporation	Matt Peterson Director, Systems Marketing
Computervision Corporation	Michael Barry Director, Workstation Systems Dev.
Computervision Corporation	Stephanie Marrus
Counterpoint Computer	Pauline Alker President
Cybernex	James B. Money Vice President, Marketing
Data General Corporation	Donald McDougall Vice President & General Manager
Dataquest Incorporated	Beth Tucker Industry Analyst
Dataquest Incorporated	Bob Smith Marketing Manager
Dataquest Incorporated	Brad Smith Associate Director
Dataquest Incorporated	Chuck Kanupke Vice President TCIS East Coast
Dataquest Incorporated	Dave Burdick Industry Analyst

Dataquest Incorporated	Debra Jacob Secretary
Dataquest Incorporated	Eileen Barth Research Associate
Dataquest Incorporated	Frank Florence Marketing Manager
Dataquest Incorporated	H. Edward White Associate Director OAS
Dataquest Incorporated	Irene Barth Librarian
Dataquest Incorporated	Jim Newcomb Director
Dataquest Incorporated	Kelly Leininger Research Clerk
Dataquest Incorporated	Pamela Shook Group Administrator/Reserach Assistant
Dataquest Incorporated	Sharlene Burden Sales Support Rep.
Dataquest Incorporated	Thomas Bredt Vice President and Director
Dataquest Incorporated	Wendy Ledamun Research Associate
Diconix	Ernest Trvax Manager Product Planning
Digital Equipment Corporation	Barry Reynolds Finance Business Manager
Digital Equipment Corporation	Chan Yan Chow Engineering Manager
Digital Equipment Corporation	Cheryl Vedoe Product Manager
Digital Equipment Corporation	Dorothy Rado Business Manager Marketing

Digital Equipment Corporation	John Clarke
Digital Equipment Corporation	John Dimack Engineering Operations Manager
Digital Equipment Corporation	Ken Brabitz Planning Manager
Digital Equipment Corporation	Libby Aston Engineering Supervisor
Digital Equipment Corporation	Nick Johnson Technologist
Digital Equipment Corporation	Norm Tripp Product Manager
Digital Equipment Corporation	Peter Dauidoss Product Manager
Digital Equipment Corporation	Prakash Bhalerao Engineering Group Manager
Digital Equipment Corporation	Roslyn Morbay Product Marketing Manager
Digital Equipment Corporation	Sri Sriran Marketing Specialist
Digital Equipment Corporation	Susan Blount Senior Marketing Specialist
Digital Equipment Corporation	Tim Yeaton Finance Manager
E.R.S.O.	K. C. Chen Engineer
Eastman Kodak Company	John C. Batterson Planning Specialist
Formative Technologies, Inc.	Jose A. Villalobos Vice President, Marketing
Fujitsu America Inc.	Katsuhide Hirai Manager, Applications

GenRad Incorporated	S. Russel Craig Director, Corporate Marketing
General Computer Company	Kevin Curran President
General Computer Company	Pax Goodson Marketing Manager
General Electric Company	James Whitten Manager Design Engineering
General Electric Company	Marshall Kidd Manager Technical Analyst
General Electric Company	Robert W. Baeder Staff Executive
General Electronic Company	Dale W. Rowe General Manager 66TD
Gould Incorporated	Dana A. Gauthier Manager Planning & Financial Services
Gould Incorporated	Joseph Heaney Senior Vice President, Sales & Marketing
Hewlett-Packard Company	Alan Benjamin Product Marketing Engineer
Hewlett-Packard Company	Jim Casey Manager CAD/CAM Strategic Marketing
Hewlett-Packard Company	Jim Lyons Product Marketing Manager
IBM	A. C. Ewing Graphics Adminstrator
IBM	Junius Brown Program Manager-Business Plans
IBM	Richard Ma Senior Marketing Analyst
IBM	Robert McGoldrick Manager Technology Development

ICM, Incorporated	Brian W. Kirschner Vice President, Research & Development
ICM, Incorporated	Dr. L. L. Barinka President
IDS Growth Spectrum Advisors	Michael F. Guilford Senior Analyst
Impell Corporation	Pat Strange Director
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LSI Logic Corporation	Mike Connell CAD Marketing Manager
LSI Logic Corporation	Richard Perry Software Marketing Manager
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Lexidata Corporation	Shelly Lowenthal Engineering Manager
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Matra Datavision	John Keller Manufacturing Manager
McAuto	Jeff Barnell Hardware Product Manager
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Megatek Corporation	Hiram French Vice President, Marketing

Megatek Corporation	Susan Harvey Corporate Planning Manager
Mentor Graphics	Michael Bosworth Director of Marketing
Metheus Corporation	Ken Tang Senior Accounts Manager
Mosaic Technology	Arthur Campbell President
NCC Corporation	Jack Mullins Liason from NCR Corporation
NEC Electronics USA, Inc.	Hotaek Rhim Manager Semi-Custom Design
NEC Electronics USA, Inc.	Robert Scott Technical Staff Member
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Nixdorf	Lorraine Chouinard Product Line Manager
Oak Management Corporation	Carla Haugen Associate
Olivetti Research & Development	Charles Erickson Manager
Pacific Telesis Group	Bill R. Frazer Director
Paragon Technology	Philip Monego President
Parallax Graphics	Jim A. Summers President
Perq Systems	Richard Cox Director, Marketing Planning
Perq Systems Corporation	Richard Rifenburgh Chairman of the Board/CEO

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Prime Computer Corporation	Celia Bland Manager Workstation Marketing
Prime Computer Corporation	Edward Vravlick Systems Concusltant
Prime Computer Corporation	Maxin Smith Director Technical Strategies
Prime Computer Corporation	Michael Payne Director, CAD/CAM Reserach & Dev.
Prime Computer Corporation	Peter Mills Manager Workstation Programs
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Prudential-Bache Securities	Christine Chien
Prudential-Bache Securities	Michael Weisberg Director of Technology Research
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Pyramid Technology	Frank Madren Vice President, Marketing
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Wang Labs	Gary Neil Director, Industry Marketing Programs
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Wayne Kerr	Ted Sisley Product Manager
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Weitek Corporation	Arthur Collmeyer President

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	James Mannos
	Tom Teeters
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Computervision Corporation	Michael Barry
	James Cook
	Hank Kellogg
	Mark Krentzman
	Stephanie Marrus
	Matt Peterson
Counterpoint Computer	Pauline Alker
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Data General Corporation	Donald McDougall

Dataquest Incorporated	Eileen Barth
	Irene Barth
	Thomas Bredt
	Sharlene Burden
	Dave Burdick
	Frank Florence
	Debra Jacob
	Chuck Kanupke
	Wendy Ledamun
	Kelly Leininger
	Jim Newcomb
	Pamela Shook
	Bob Smith
	Brad Smith
	Beth Tucker
	H. Edward White
Diconix	Ernest Trvax
Digital Equipment Corporation	Libby Aston
	Prakash Bhalerao
	Susan Blount
	Ken Brabitz
	Chan Yan Chow
	John Clarke
	John Dimack

	Nick Johnson
	Roslyn Morbay
	Dorothy Rado
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	Hiram French
	Susan Harvey
Mentor Graphics	Michael Bosworth
Metheus Corporation	Ken Tang
Mosaic Technology	Arthur Campbell

NBI, Incorporated	Sky Stevenson
NCC Corporation	Jack Mullins
NEC Electronics USA, Inc.	Hotaek Rhim
	Robert Scott
National Semiconductor	N. T. Hsu
	Ke Shih
Nixdorf	Lorraine Chouinard
Oak Management Corporation	Carla Haugen
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Valid Logic	Frank Lynch
Wang Labs	Gary Neil
	Ann Palermo
Weitek Corporation	Lynette DeNike
Weitek Corporattion	Arthur Collmeyer

Nielsen Dataquest

WORKSTATION INDUSTRY OVERVIEW

James R. Newcomb
Director, Design and Manufacturing Automation Group
Dataquest Incorporated

Mr. Newcomb is Director of DATAQUEST's Design and Manufacturing Automation Group. Before joining DATAQUEST, he was with Auto-trol Technology Corporation, where he held various executive positions, including Manager of Marketing. Prior to that, Mr. Newcomb was employed by Xerox Corporation, where he held positions as Manager of Systems Integration, Manager of Advanced Manufacturing Engineering, and Divisional Program Planner. Earlier, he worked in an engineering capacity with Strippit-Hoidaille. His professional experience has provided him with an in-depth knowledge of manufacturing automation systems. Mr. Newcomb received a B.S.M.E. degree from Rochester Institute of Technology. He is a member of the American Society of Mechanical Engineering, SME, RI/SME, and CASA/SME.

Dataquest Incorporated
WORKSTATION FOCUS CONFERENCE
August 13 and 14, 1984
Burlington, Massachusetts

FOCUS ON WORKSTATIONS

AUGUST 13-14, 1984

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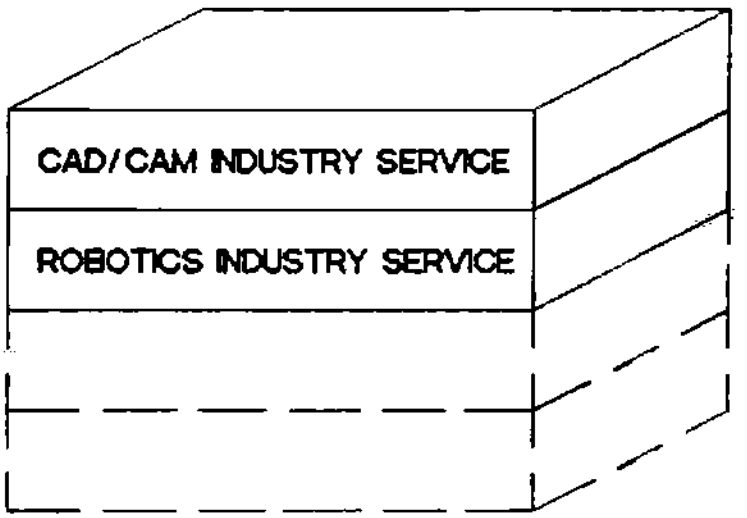
TECHNOLOGY INFORMATION DIVISION
DESIGN AND MANUFACTURING AUTOMATION GROUP



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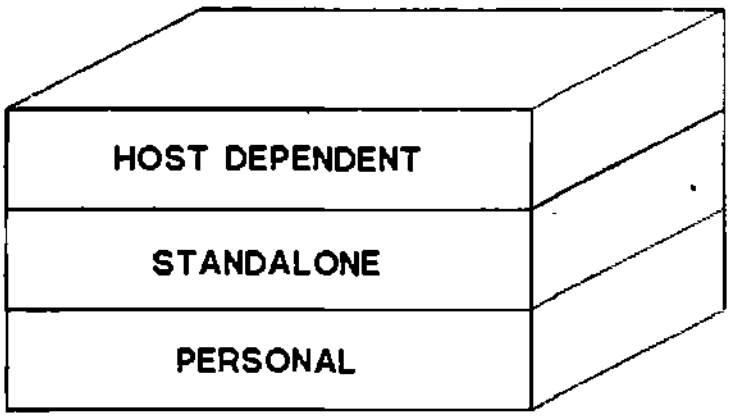
WORKSTATIONS
DEFINITION--SEGMENTATION



Source: DATAQUEST

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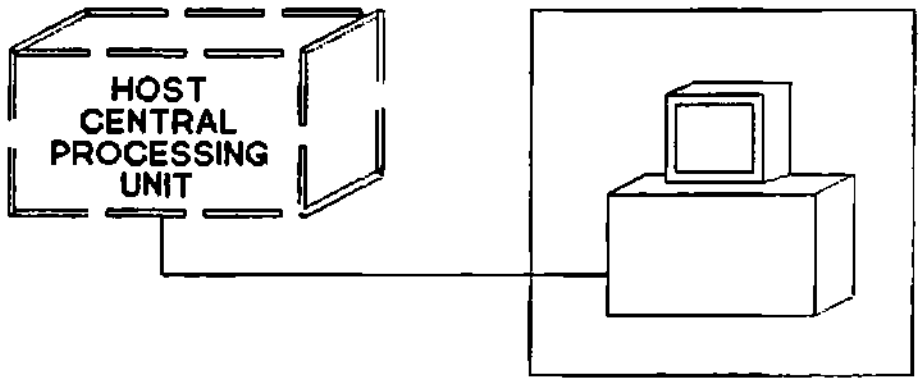
WORKSTATIONS

HOST DEPENDENT WORKSTATION



- NON-RESIDENT CENTRAL PROCESSING UNIT
- NO LOCAL OPERATING SYSTEM

Source: DATAQUEST

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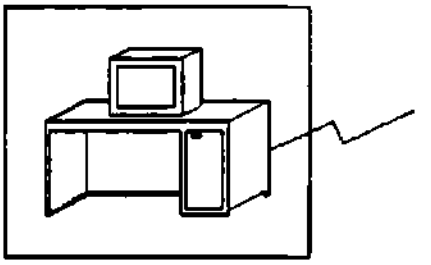
WORKSTATIONS

STANDALONE WORKSTATION



- O/S IS RESIDENT IN PHYSICAL DEVICE
- VIRTUAL-OPERATING SYSTEM
- MULTI-TASKING
- SUPPORTS NETWORKED COMMUNICATIONS
- INTEGRATED GRAPHICS
- NO SPECIAL POWER/ENVIRONMENT REQUIREMENTS

Source: DATAQUEST

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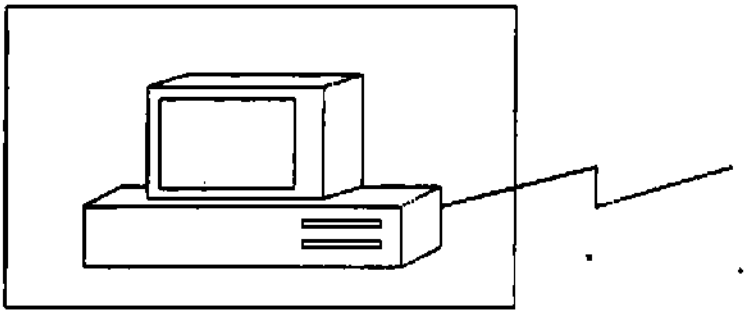
WORKSTATIONS

PERSONAL WORKSTATIONS



- LOCAL 8/16 BIT CENTRAL PROCESSING UNIT
- NON-VIRTUAL MACHINE
- SINGLE PROCESSING

Source: DATAQUEST

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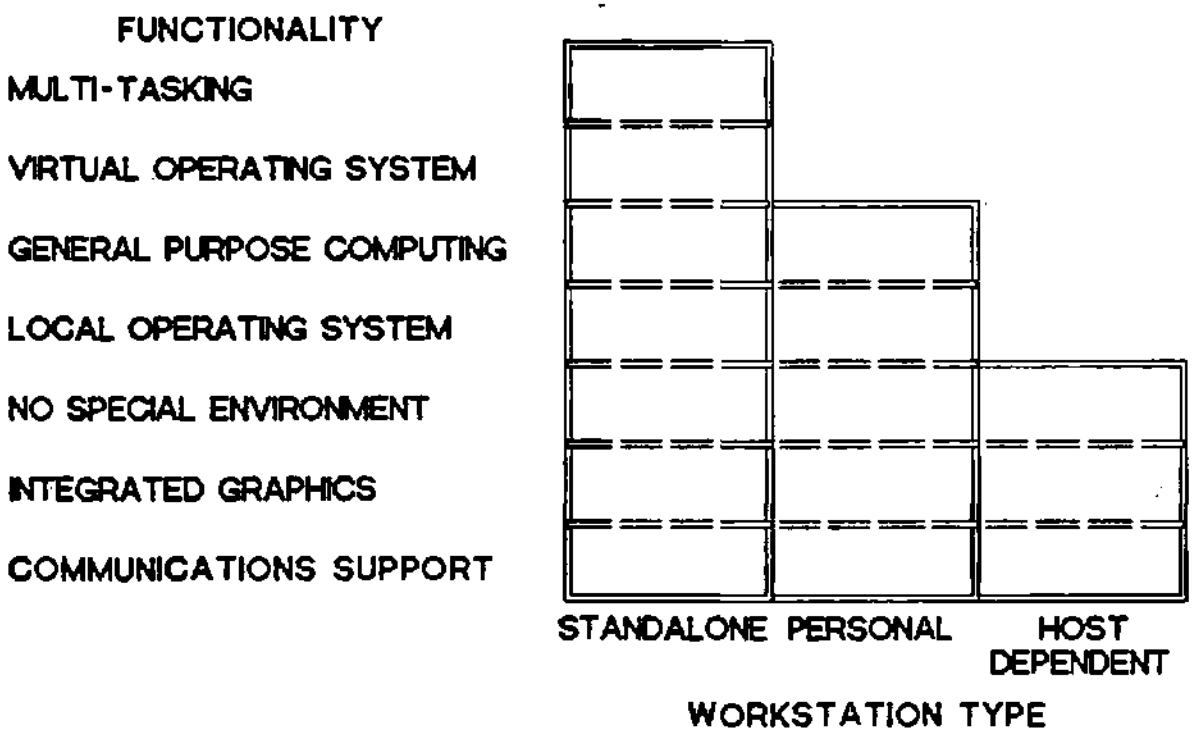
WORKSTATIONS



Source: DATAQUEST

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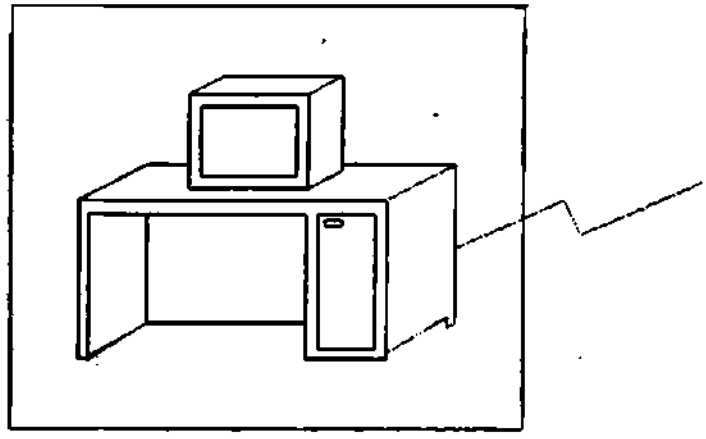
FOCUS ON
STANDALONE WORKSTATIONS



Source: DATAQUEST

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STANDALONE WORKSTATIONS

WHY?

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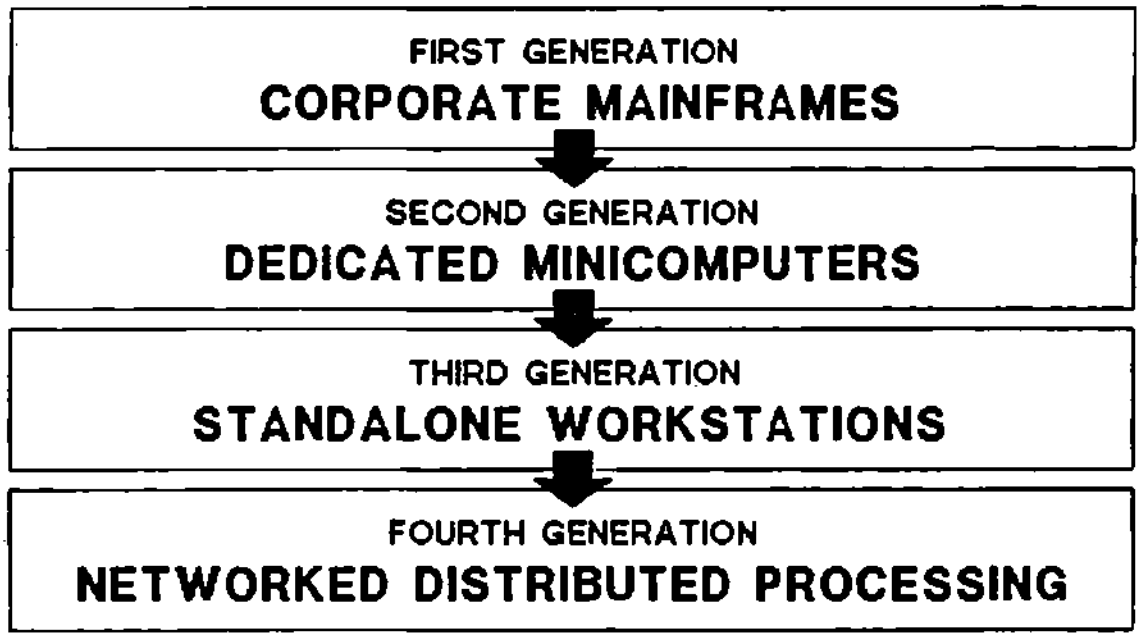
WORKSTATION
EVOLUTION



Source: DATAQUEST

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FIRST GENERATION CORPORATE MAINFRAMES

- SINGLE APPLICATION ORIENTATION
- NO INTEGRATION
- LIMITED COMMUNICATIONS
- UNPREDICTABLE PERFORMANCE
- INCOMPATIBLE SW/HW

Source: DATAQUEST

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SECOND GENERATION DEDICATED MINICOMPUTERS

- MULTIPLE DATA BASES
- INCOMPATIBLE SW/HW
- LIMITED COMMUNICATIONS
- NON-STANDARD INTERFACES
- FINITE INTEGRATION

Source: DATAQUEST

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WORKSTATIONS

"AWARENESS--CONCERNS""

- DIMINISHING PRODUCT LIFE CYCLES
- INCREASING PRODUCT DESIGN CYCLES
- LIMITED POOL OF ENGINEERING TALENT

Source: DATAQUEST

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A SOLUTION

IMPROVED ALLOCATION OF COMPUTER PROCESSING POWER

Source: DATAQUEST

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THIRD GENERATION STANDALONE WORKSTATIONS

- PREDICTABLE LEVELS OF PERFORMANCE
- IMPROVED PRICE/PERFORMANCE RATIOS
- INTEGRATED HW/SW
- UTILIZATION IN NORMAL ENVIRONMENTS
- INITIAL STANDARDIZATION
- AFFORDABLE GROWTH

Source: DATAQUEST

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FOURTH GENERATION
NETWORKED DISTRIBUTED PROCESSING

- HIGH PERFORMANCE STANDALONE CAPABILITY
- MAXIMUM RESOURCE SHARING
- FASTER RESPONSE TIME
- IMPROVED COMMUNICATION
- TIGHTLY COUPLED INTEGRATION

Source: DATAQUEST

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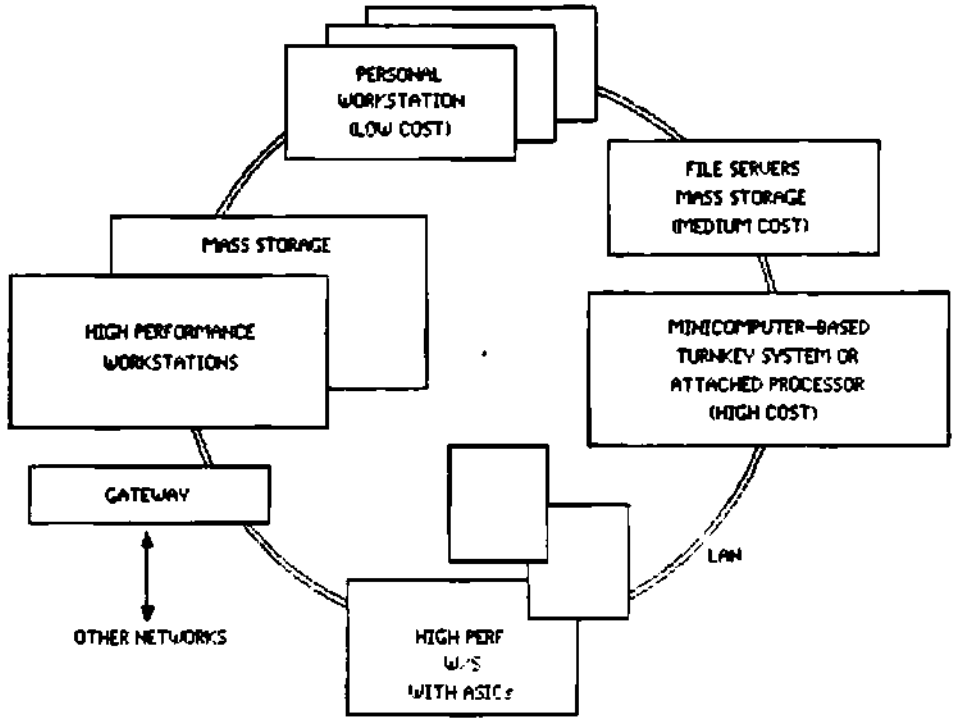
HETEROGENEOUS SYSTEM COLLECTION



Source: DATAQUEST

WORKSTATIONS SYSTEMS AND COMPONENTS

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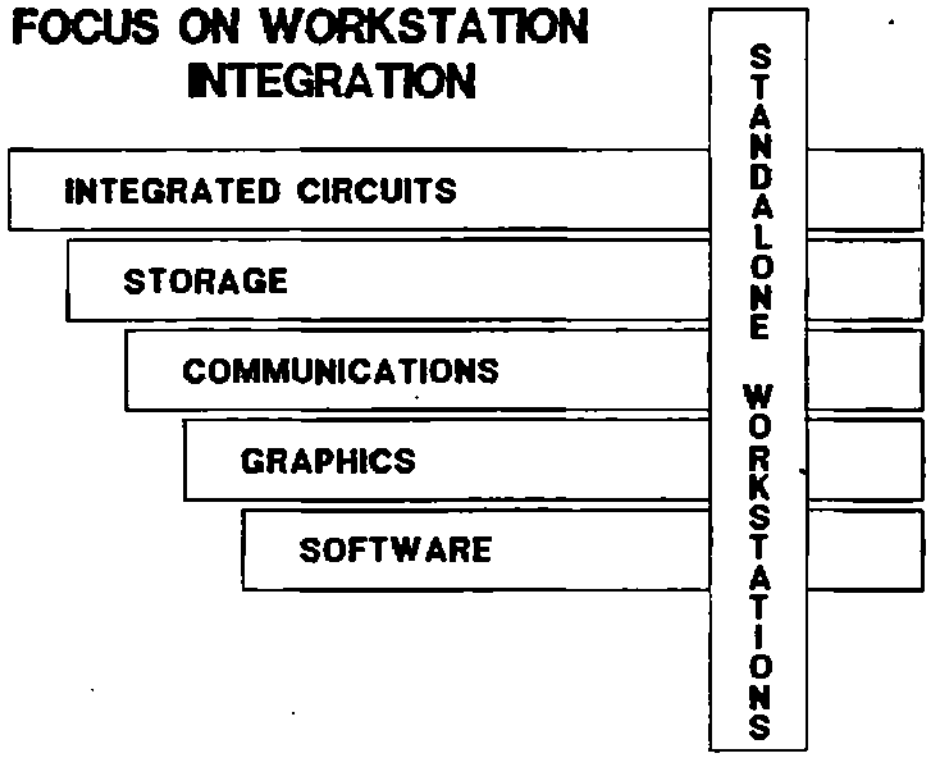
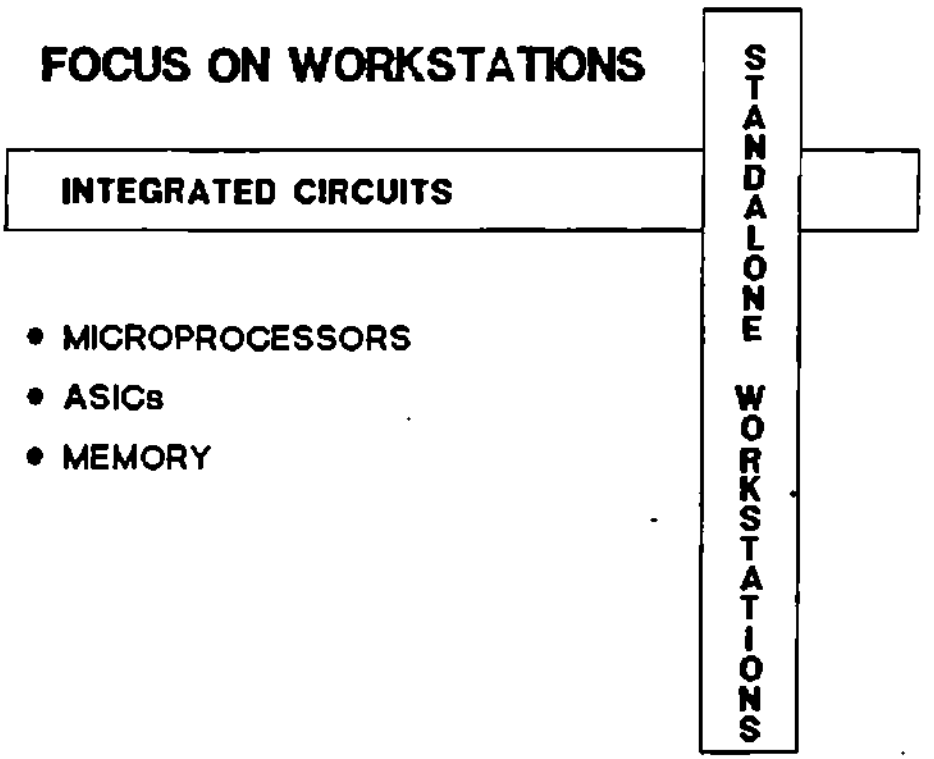
FOCUS ON WORKSTATION INTEGRATION



FOCUS ON WORKSTATIONS



WORKSTATIONS

TWO APPROACHES OF MICROPROCESSOR INTEGRATION

CAPTIVE	MERCHANT
HP	MOTOROLA
DEC	NATIONAL
ATT/WE	NCR
	INTEL
	TI
	NEC
	ZILOG

Source: DATAQUEST

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MICROPROCESSORS - - TODAY

- INTEGRATION OF EXISTING TECHNOLOGIES
  - MORE I/O FUNCTIONALITY
- ADDITION OF SYSTEMS FUNCTIONALITY
  - PIPELINING
  - VIRTUAL MEMORY SUPPORT
  - MEMORY MANAGEMENT
  - CACHE MEMORY
- MIGRATION TO 32 BIT MPUs

Source: DATAQUEST

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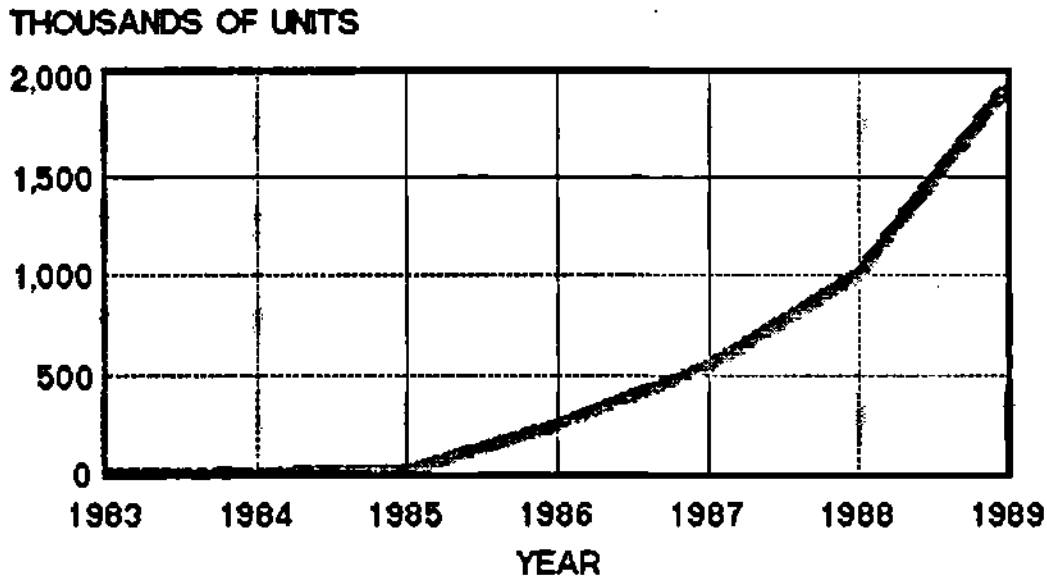
MICROPROCESSOR FORECAST
32 BIT MPUs

CAGR = 74.8%



Source: DATAQUEST

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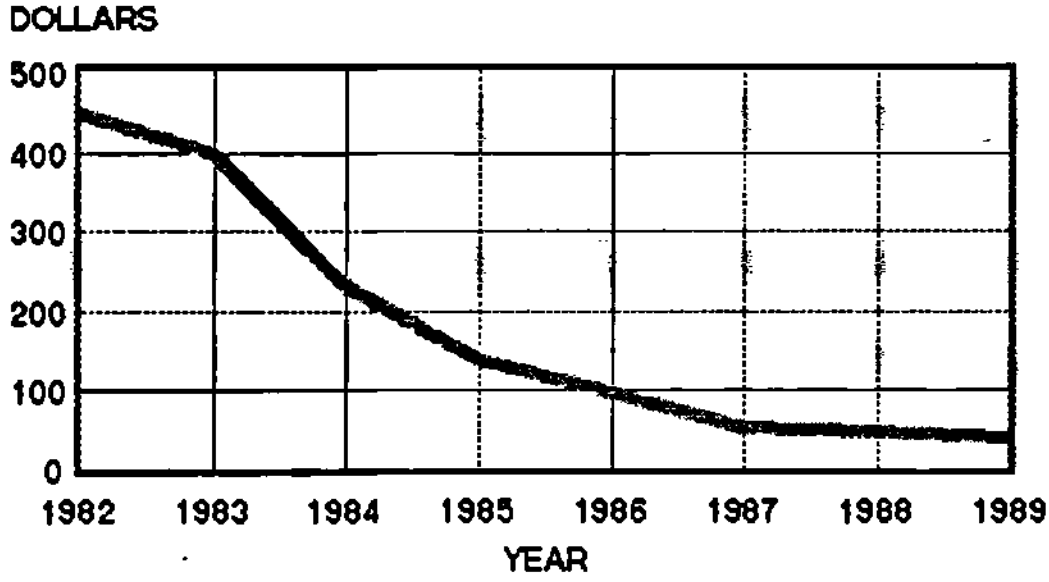
MICROPROCESSOR ASP FORECAST
32 BIT MPUs

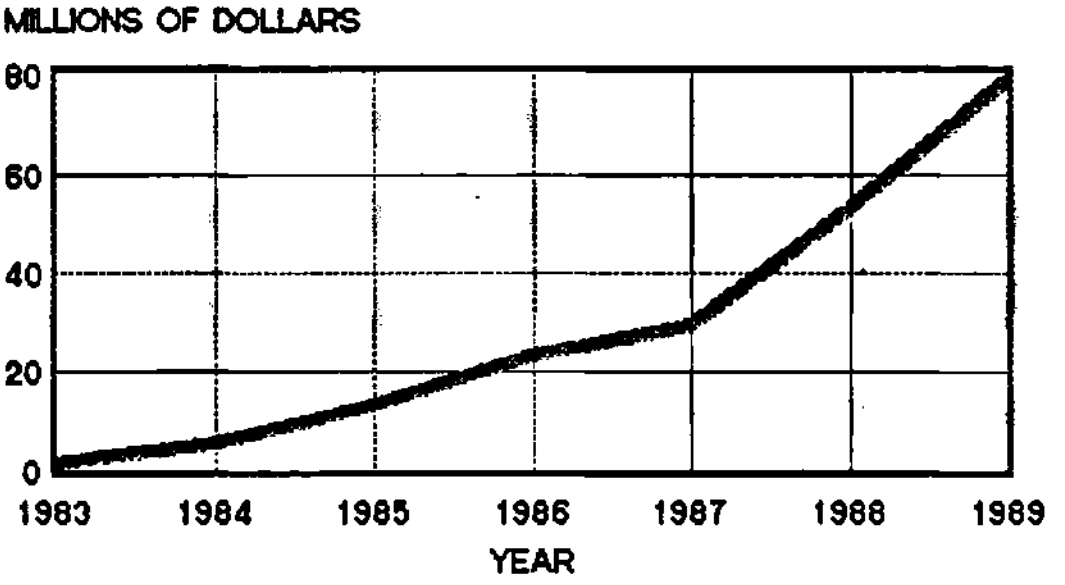
CAGR = -31.6%



Source: DATAQUEST

MICROPROCESSOR REVENUE FORECAST
32 BIT MPUs

CAGR = 91.7%



Source: DATAQUEST

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MICROPROCESSORS--TRENDS

- UPWARD COMPATIBILITY WITH EXISTING INSTRUCTION SETS
- CHALLENGING THE PERFORMANCE OF MINICOMPUTERS
- HIGHER CLOCK SPEEDS
  - 10 MHz TO 25 MHz NOW
  - 50 MHz 3 TO 5 YEARS
  - 100 MHz COMING
- DEVICES/DIE INCREASING
  - 100K-400K NOW
  - 700K BY 1986
  - 1 MILLION DEVICES SOON
- UTILIZATION OF COPROCESSORS

Source: DATAQUEST

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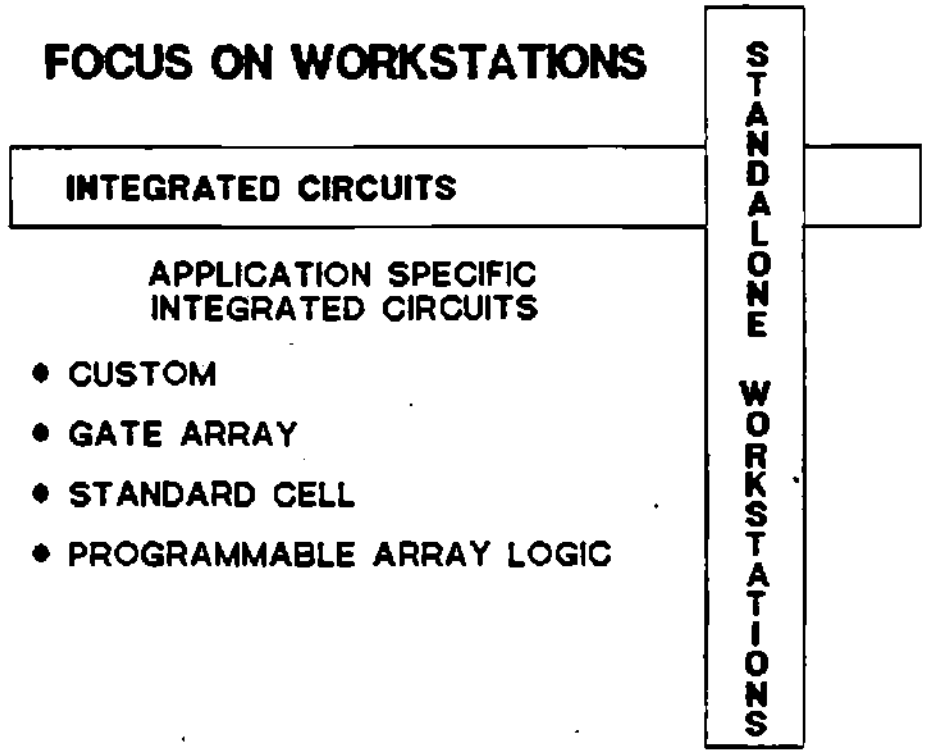
FOCUS ON WORKSTATIONS

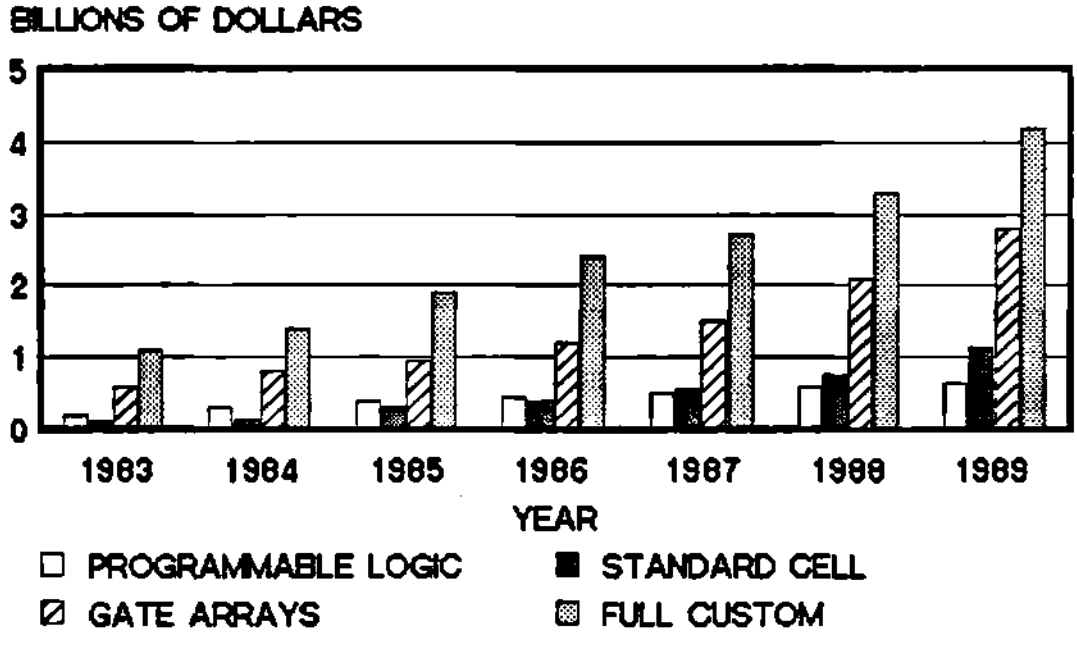


WHY ASICs ARE WINNING--TODAY

- POWER INEXPENSIVE MICROPROCESSORS
- SELF-FULLFILLING PROPHECY
- ASIC--FOCUSED START-UP COMPANIES
- PROVISION OF POWERFUL DESIGN TOOLS
- ACCEPTANCE OF CMOS VLSI
- SOPHISTICATION OF USERS

Source: DATAQUEST

ESTIMATED WORLDWIDE ASIC CONSUMPTION



Source: DATAQUEST

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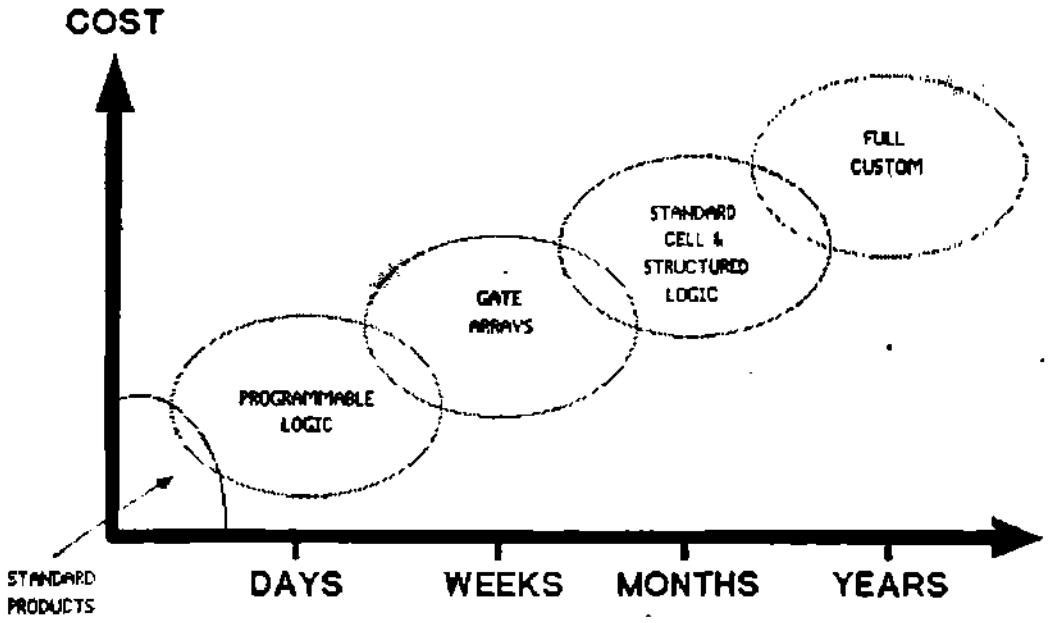
IMPLEMENTATION ALTERNATIVES



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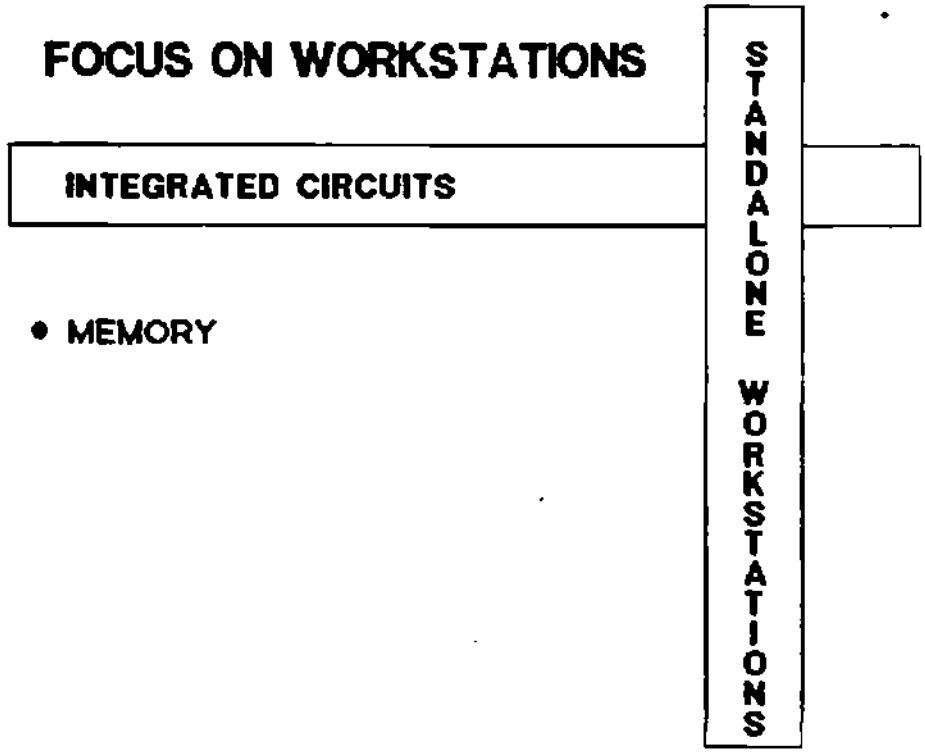
FOCUS ON WORKSTATIONS



- MEMORY

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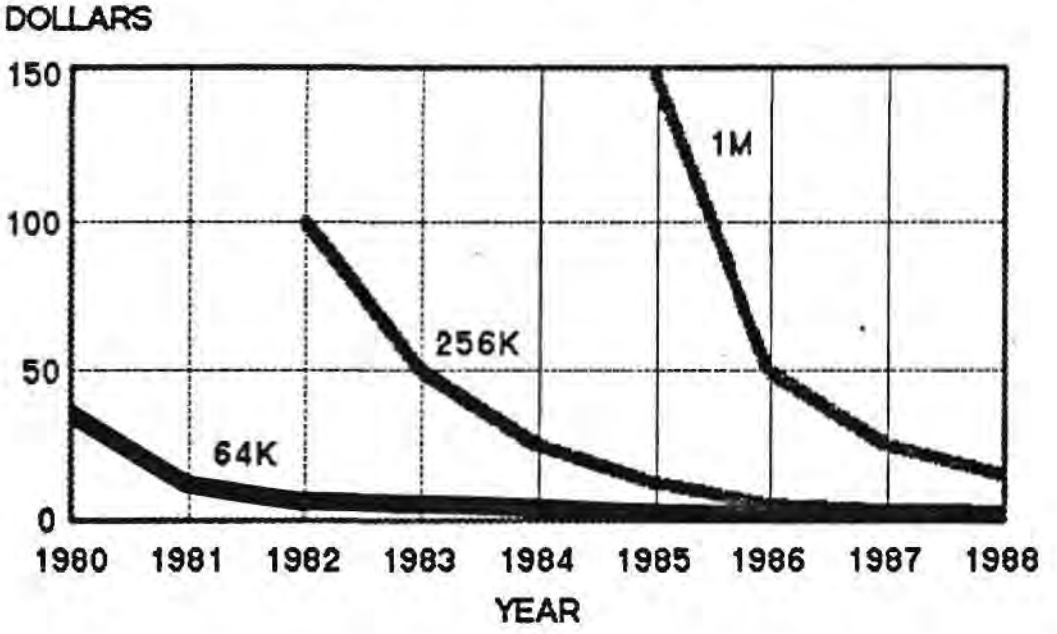
MEMORY FORECAST--DYNAMIC RAMS
AVERAGE SELLING PRICE



Source: DATAQUEST

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MEMORY REQUIREMENTS

1,024 X 1,024 RESOLUTION

NO. OF COLORS	NO. OF BIT PLANES	MEMORY CBYTES	NUMBER OF CHIPS			
			16K	64K	256K	1M
1	1	128K	64	16	4	1
16	4	512K	256	64	16	4
256	8	1MB	512	128	32	8
4,096	12	1.5MB	768	192	48	12
16M	24	4MB	1,536	384	96	24

Source: DATAQUEST

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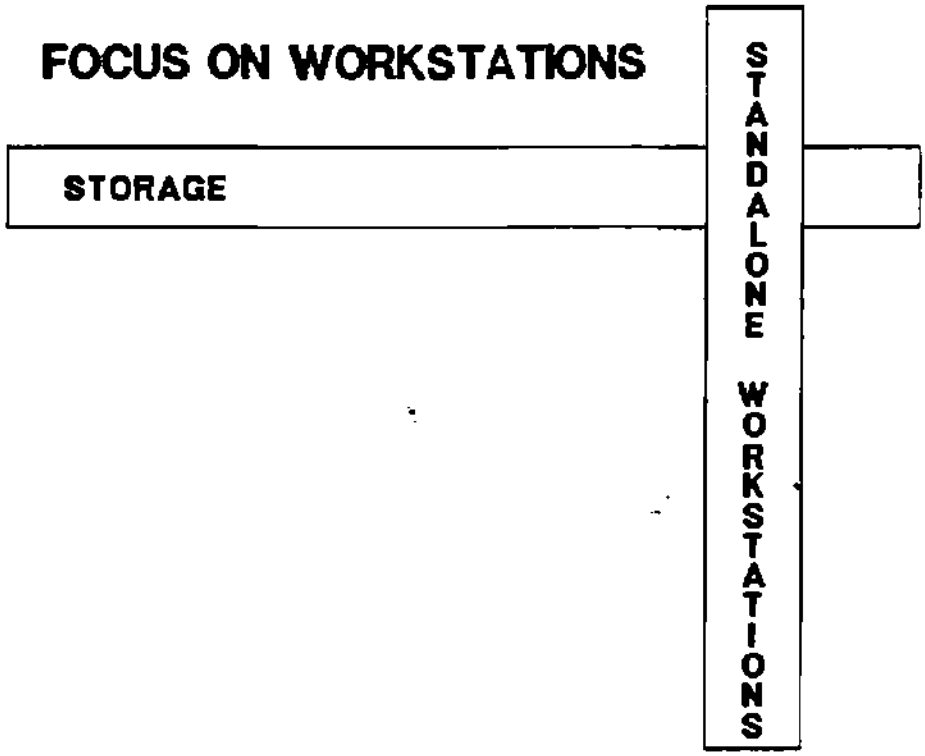
FOCUS ON WORKSTATIONS



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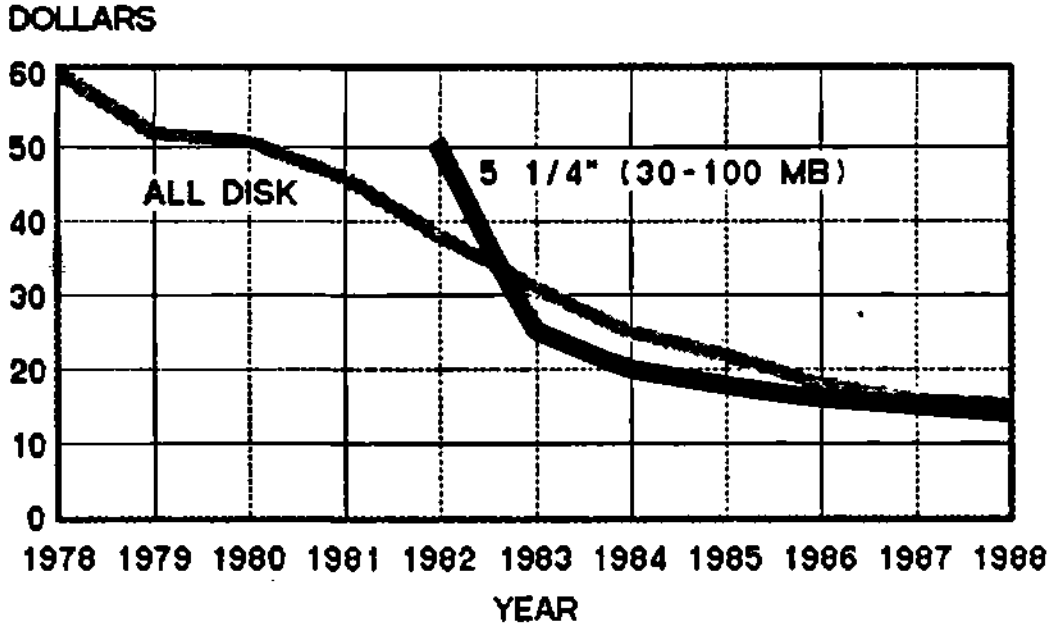
STORAGE FORECAST
COST PER MB OF ON-LINE STORAGE



Source: DATAQUEST

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TRENDS IN COMPUTER STORAGE

- LOWER COST PER MB
- HIGHER AREAL DENSITIES
- SMALLER FORM FACTORS
- PERFORMANCE ENHANCEMENTS
- PERSONAL STORAGE
- EXPLOSION IN PRODUCT AVAILABILITY

Source: DATAQUEST

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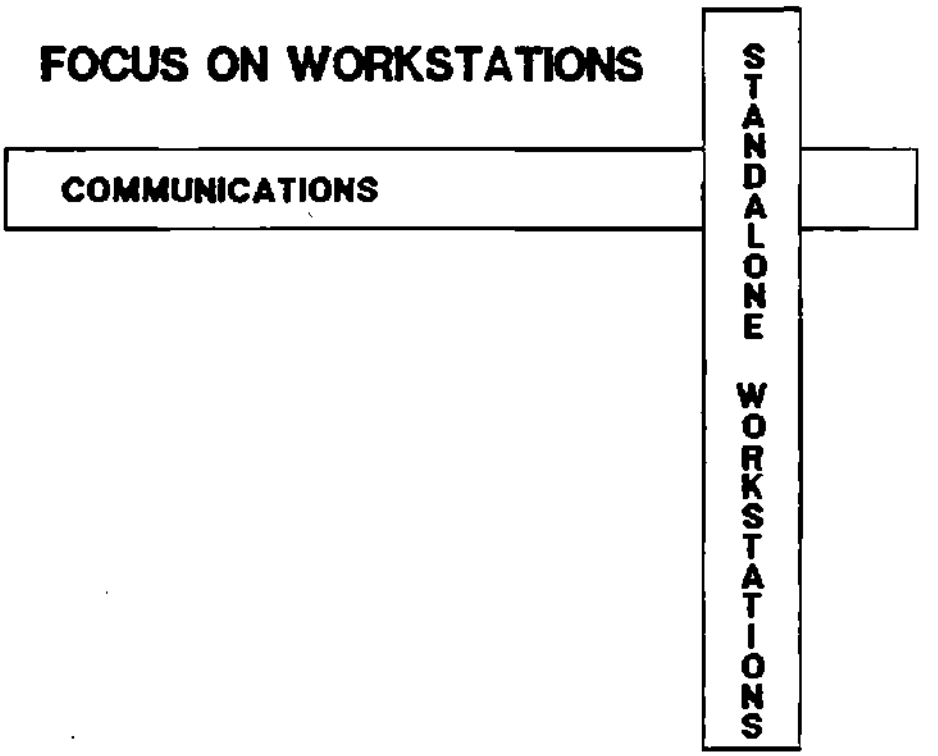
FOCUS ON WORKSTATIONS



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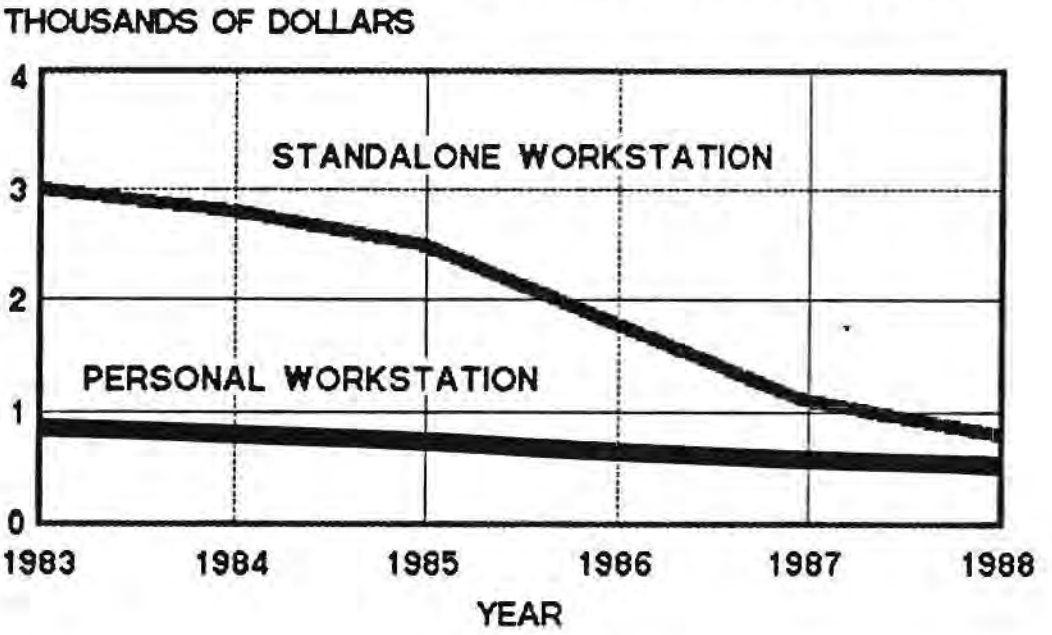
COMMUNICATIONS FORECAST
COST PER NETWORK CONNECTION



Source: DATAQUEST

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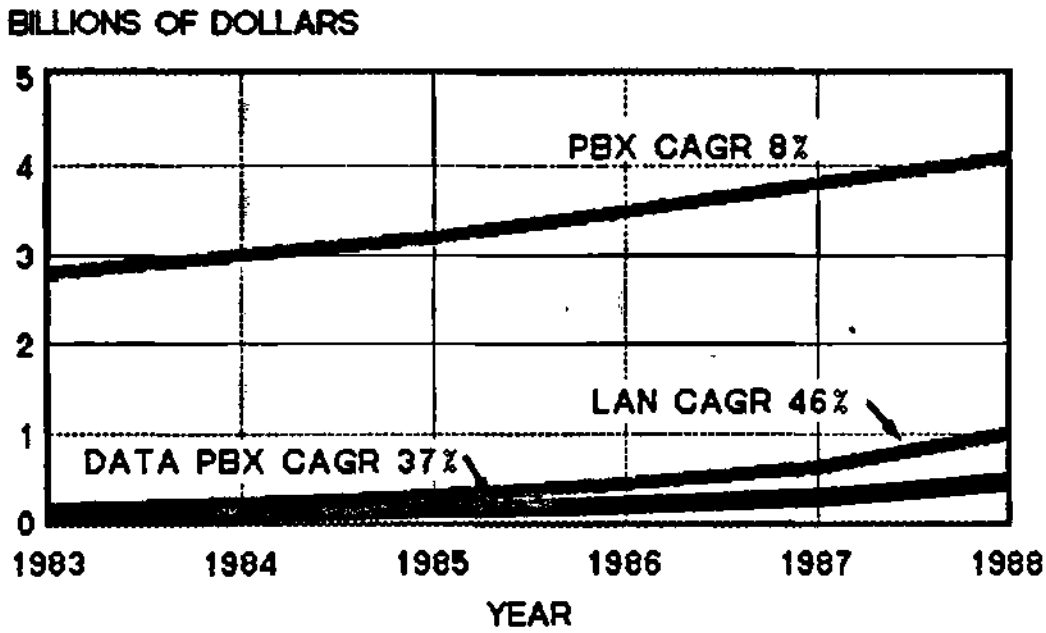
COMMUNICATIONS FORECAST



Source: DATAQUEST

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COMMUNICATIONS--ISSUES

- PROPRIETARY VS. STANDARD NETWORKS
- HOW DOES UNIX FIT
- OPERATING SYSTEM NETWORKS
- PRICE/PERFORMANCE RATIOS
- ROLE OF PBXs AND DATA PBXs

Source: DATAQUEST

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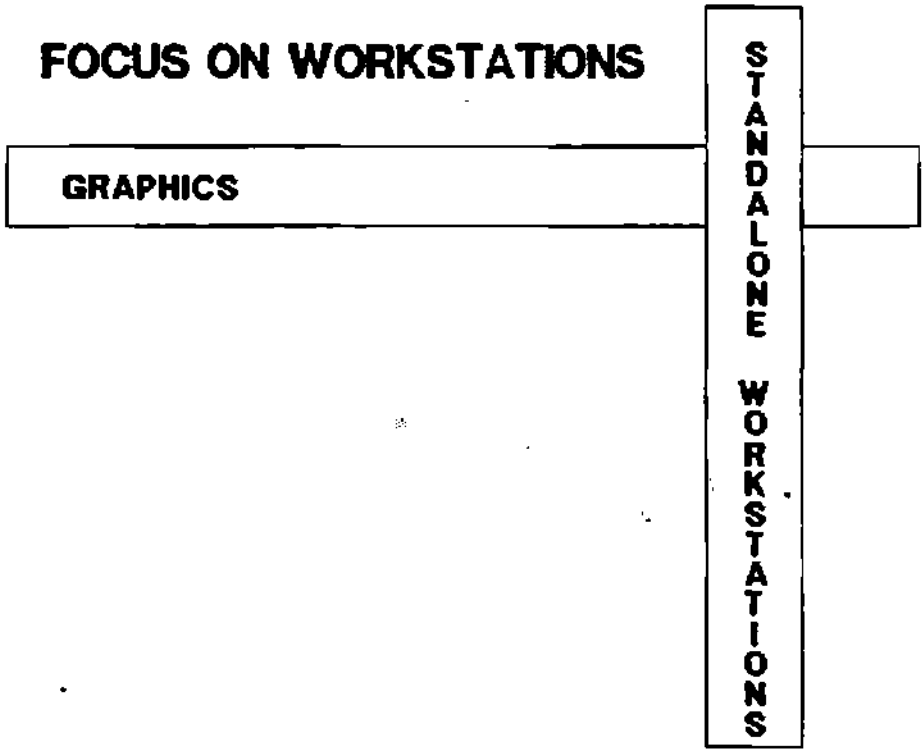
FOCUS ON WORKSTATIONS



GRAPHICS EVOLUTION

- STORAGE DEVICES/HOST DEPENDENCY
- RASTER/HOST DEPENDENCY
- RASTER WITH LOCAL GRAPHICS PROCESSING

Source: DATAQUEST

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THIRD GENERATION GRAPHICS ARCHITECTURES

- UTILIZATION OF LOCAL VLSI
- HIGH SPEED MATRIX ENGINES
- ADVANCED SHADING AND RENDERING CIRCUITRY
- LOCAL GEOMETRY PROCESSING
- HIGHER RESOLUTION DISPLAY TECHNOLOGIES
- EVER DECREASING COSTS

Source: DATAQUEST

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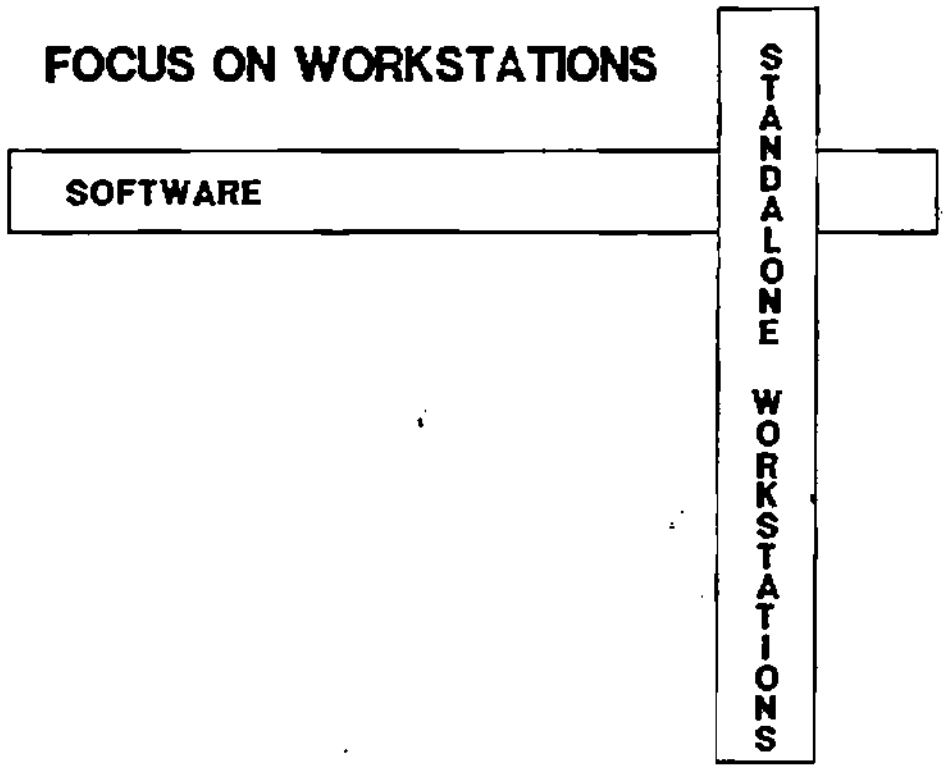
FOCUS ON WORKSTATIONS



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SOFTWARE--THE PAST

- S/W AND O/S HARDWARE DEPENDENCY
- LIMITED PROGRAMMING TOOLS
- LONG DEVELOPMENT TIMES
- LIMITED PORTABILITY/LIMITED LEVERAGE

Source: DATAQUEST

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SOFTWARE

- COMPUTER AIDED SOFTWARE ENGINEERING
- UNIX AND "UNIX LIKE" O/S
- STANDARDIZATION
- MIGRATION OF SW INTO FIRMWARE ⟶ HARDWARE

Source: DATAQUEST

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WORKSTATIONS

SYNOPSIS

- DESIGN OF CLOSELY COUPLED SYSTEMS (HIGHER LEVELS OF SYSTEMS INTEGRATION)
- EVOLUTION OF COMPLEX MULTI-PROCESSOR DESIGNS
- FUSION OF GRAPHICS AND IMAGING TECHNOLOGIES
- ACCEPTANCE OF STANDARDS (DEVELOPMENT OF OPTIMAL SOLUTIONS FOR SPECIFIC APPLICATIONS
- PUSHING PERFORMANCE TOWARDS HUMAN PERCEPTION

Source: DATAQUEST

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FUTURES

- A SINGLE LEVEL, NETWORK-WIDE DEMAND PAGED ADDRESS SPACE
- PROVISION OF A UNIFORM INTERFACE BETWEEN ALL SYSTEMS AND RESOURCES
- CONFIGURATION ARCHITECTURE THAT SUPPORTS A WIDE RANGE OF PERFORMANCE LEVELS
- TECHNOLOGICAL INDEPENDENCE

Source: DATAQUEST

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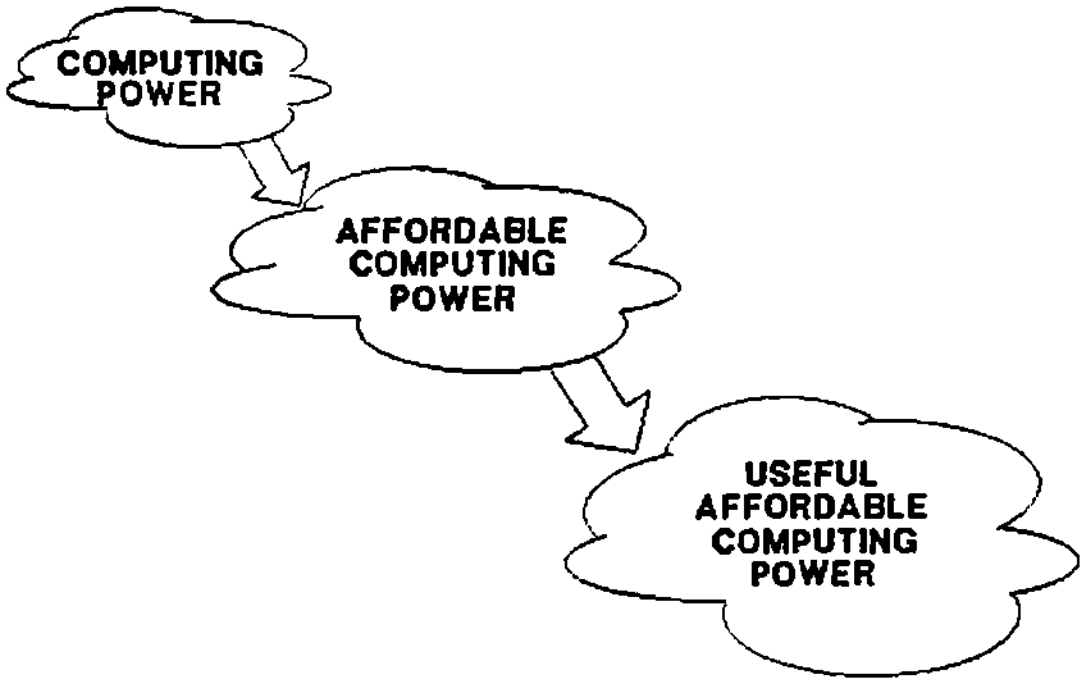
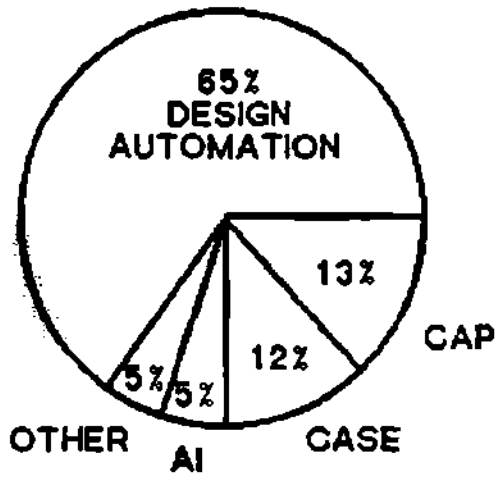


STANDALONE WORKSTATIONS

(REVENUE)

1984 MARKETS



DESIGN AUTOMATION

MECHANICAL APPLICATIONS	37%
ELECTRONIC APPLICATIONS	13%
AEC APPLICATIONS	10%
MAPPING APPLICATIONS	3%
OTHER APPLICATIONS	2%

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MARKET CREDIBILITY

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Nielsen Dataquest

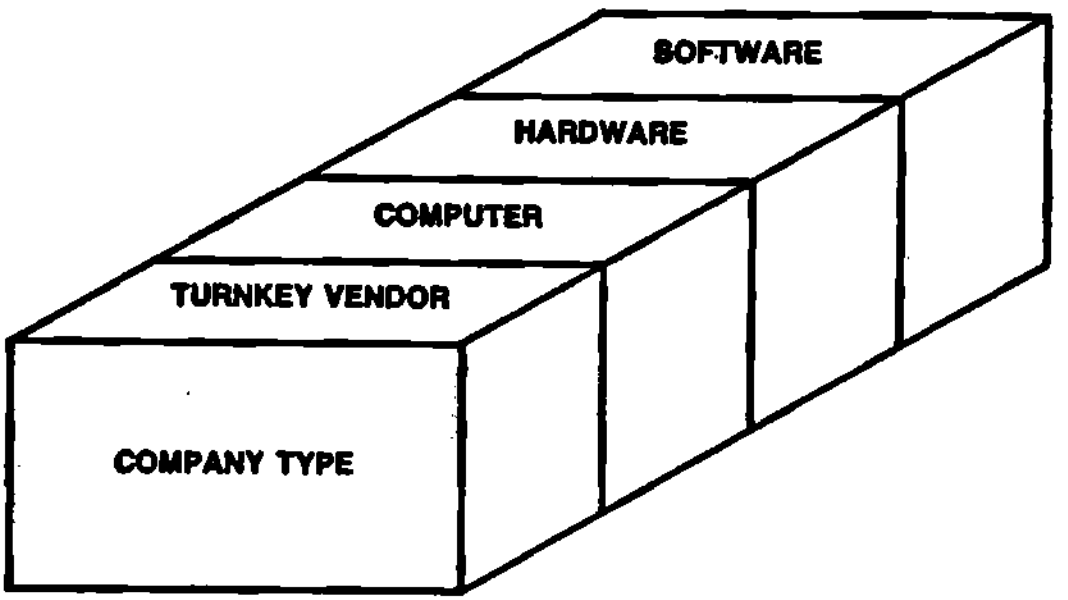
ARCHITECTURES, GRAPHICS, AND PERFORMANCE

David Burdick
Industry Analyst
Dataquest Incorporated

Mr. Burdick is an Industry Analyst in DATAQUEST's CAD/CAM Industry Service. Before joining DATAQUEST, he held System Engineering positions with Auto-trol Technology Corporation, where he was the key technical consultant for turnkey CAD/CAM systems. Prior to that, he worked as a Design Engineer for International Harvester and was involved in the design and implementation of large-scale CAE/CIM systems. Mr. Burdick has in-depth knowledge of image processing, graphics interfaces, workstation design, and AEC application areas, including piping, structural, and HVAC design. Mr. Burdick received a B.S.M.E. degree from Bradley University in Peoria, Illinois.

Dataquest Incorporated
WORKSTATION FOCUS CONFERENCE
August 13 and 14, 1984
Burlington, Massachusetts

CAD/CAM INDUSTRY SERVICE DATABASE SEGMENTATION



Source: DATAQUEST

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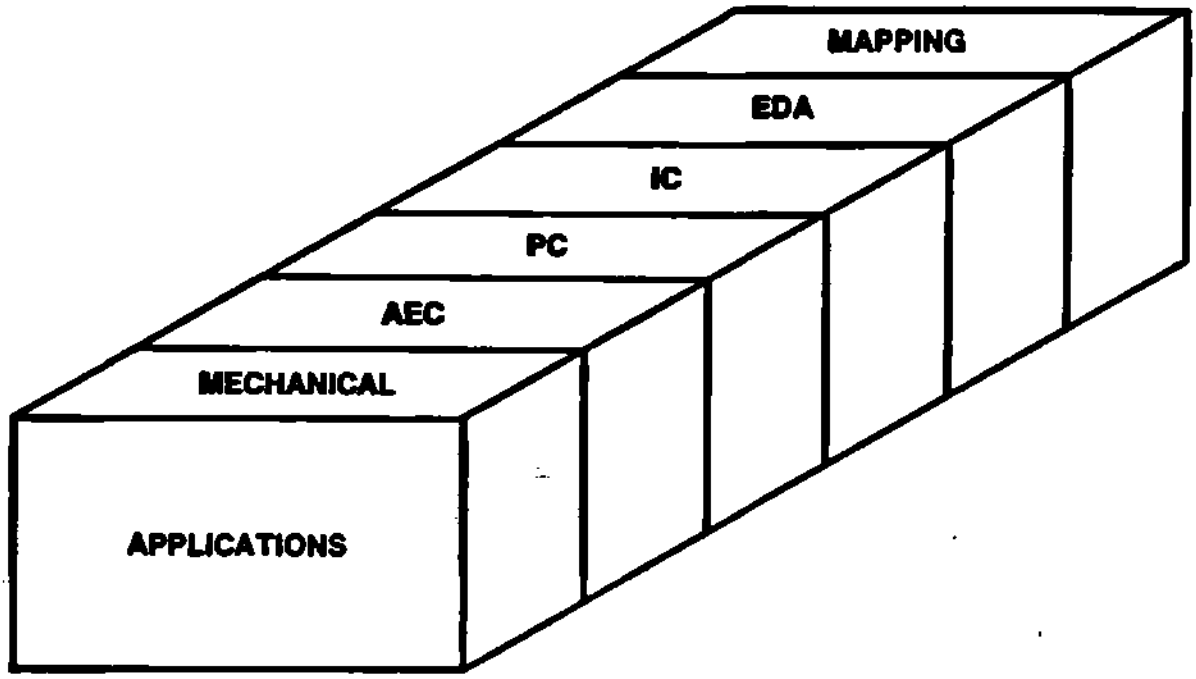
CAD/CAM INDUSTRY SERVICE DATABASE SEGMENTATION



Source: DATAQUEST

AEC = ARCHITECTURAL, ENGINEERING AND CONSTRUCTION

PC = PRINTED CIRCUIT BOARD

IC = INTEGRATED CIRCUIT

EDA = ELECTRONIC DESIGN AUTOMATION

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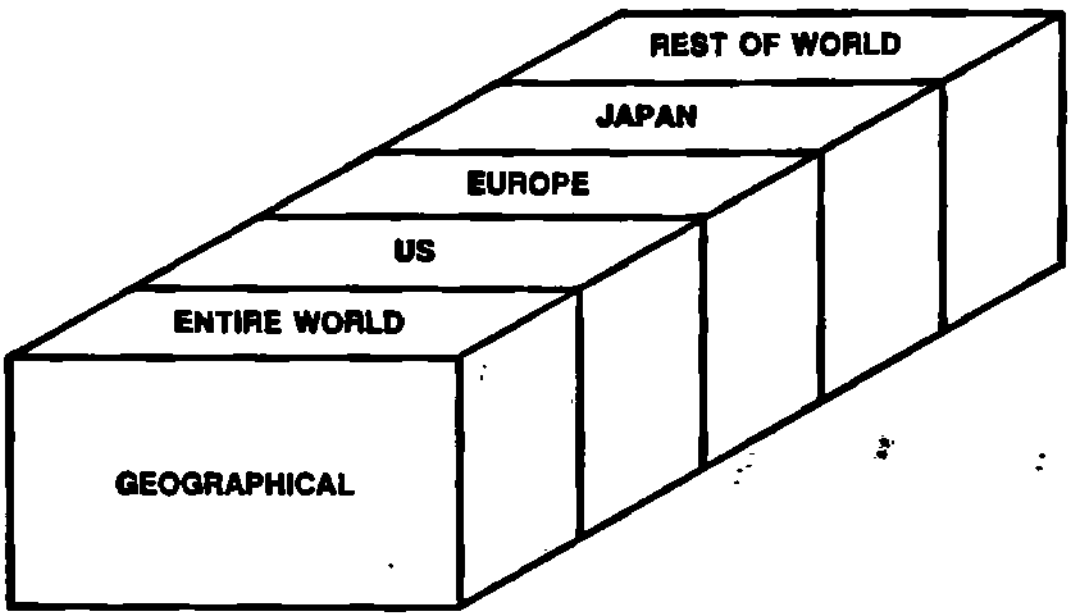
CAD/CAM INDUSTRY SERVICE DATABASE SEGMENTATION



Source: DATAQUEST

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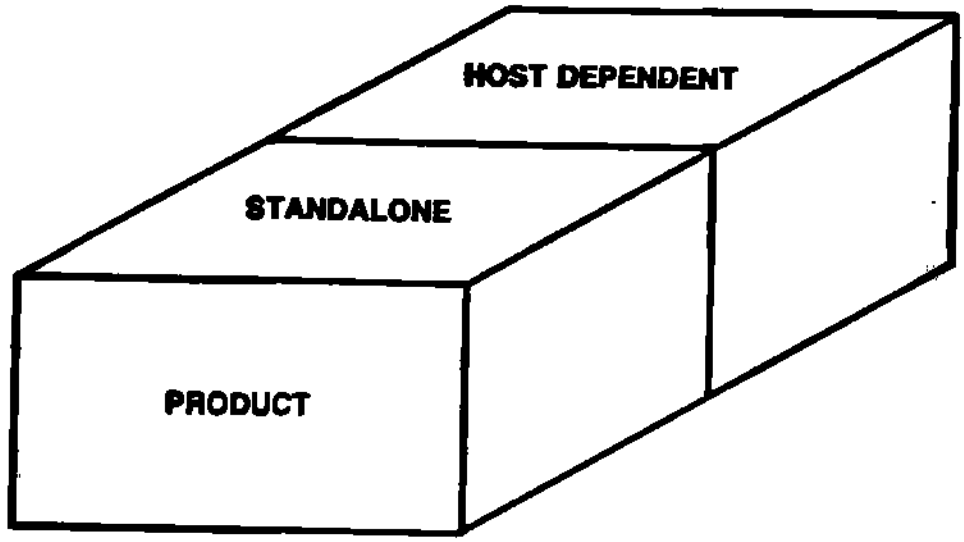
CAD/CAM INDUSTRY SERVICE DATABASE SEGMENTATION



Source: DATAQUEST

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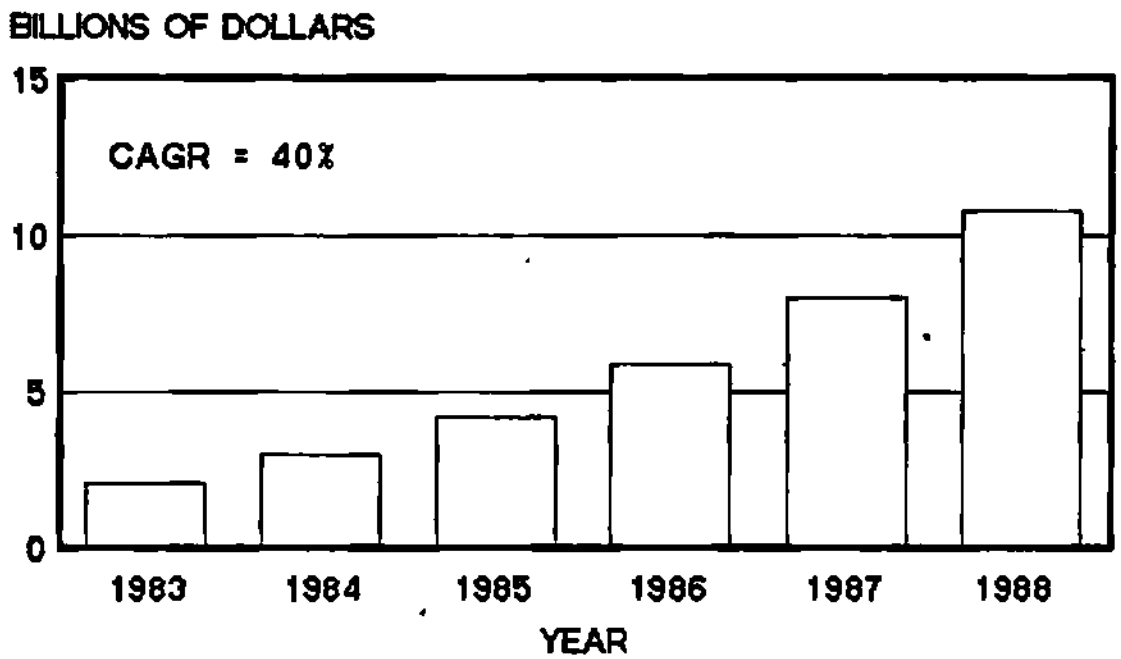
MARKET SIZING

Dataquest Incorporated, A Subsidiary of A.C. Nielsen Company / 1290 Ridder Park Drive / San Jose, CA 95131 / (408) 971-9000 / Telex 171973

CAD/CAM TOTAL REVENUE



Source: DATAQUEST

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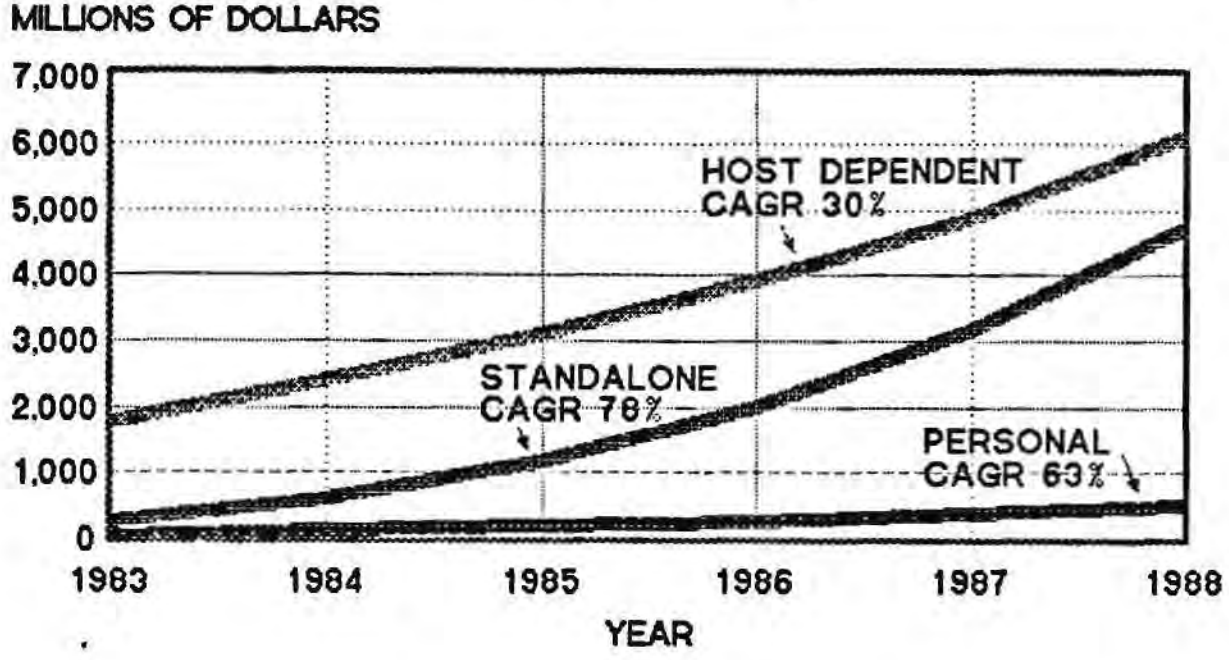
CAD/CAM REVENUE BY WORKSTATION TYPE

HW SSW



Source: DATAQUEST

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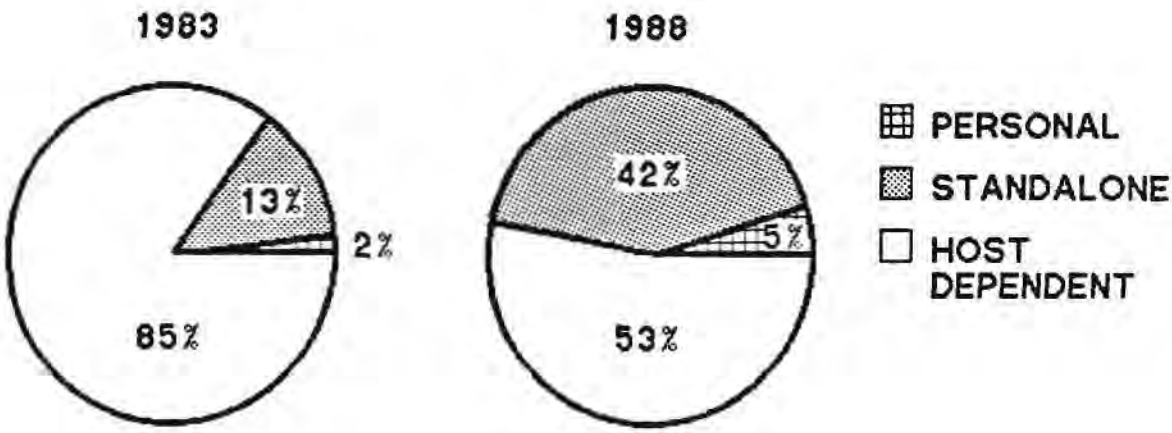
CAD/CAM WORKSTATIONS
PERCENT OF REVENUE



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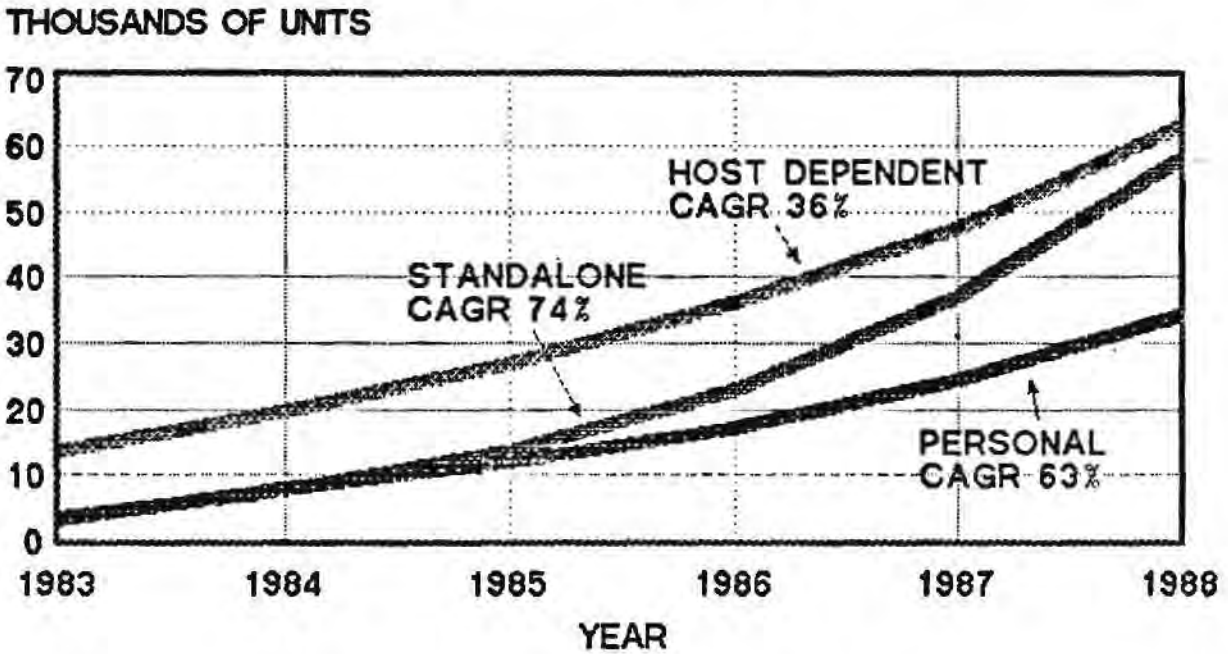
CAD/CAM UNITS
BY WORKSTATION TYPE



Source: DATAQUEST

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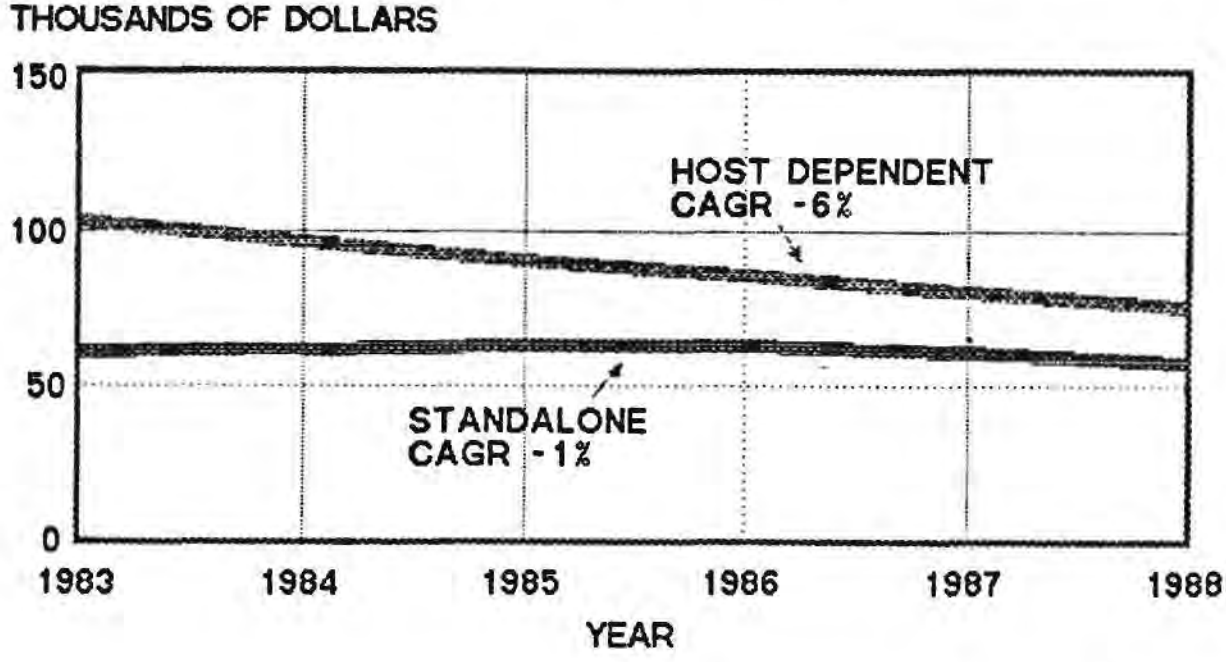
AVERAGE CAD/CAM WORKSTATION PRICE HARDWARE AND SOFTWARE



Source: DATAQUEST

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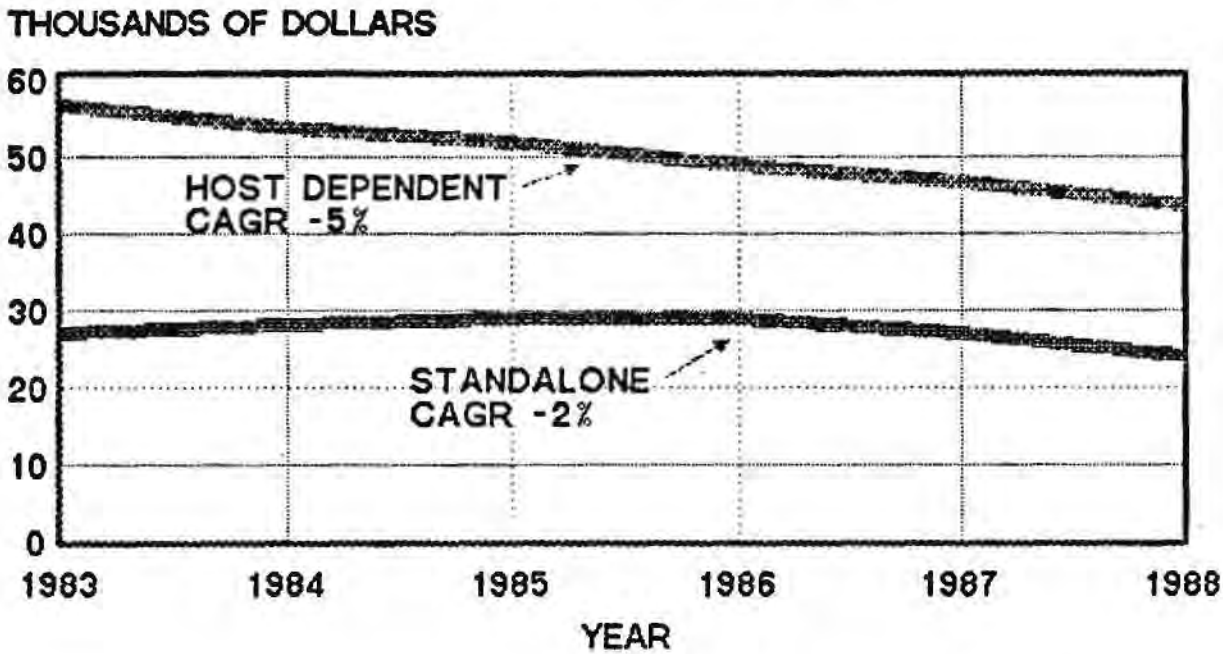
AVERAGE CAD/CAM WORKSTATION PRICE HARDWARE ONLY



Source: DATAQUEST

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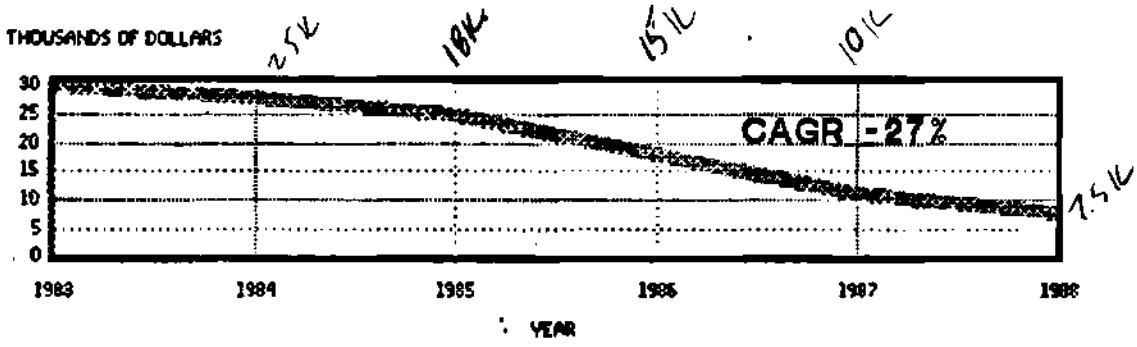
AVERAGE WORKSTATION PRICE/PERFORMANCE



BASE SYSTEM

- 0.5 - 1.0 MIPS
- MONOCHROMATIC
- 50MB DISK
- 1MB MEMORY
- ETHERNET
- UNIX

KEY INFLUENCES

- 256K RAMS
- HIGHER PERFORMANCE CPUs
- INCREASING COMPETITION

Source: DATAQUEST

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THE TECHNOLOGICAL CHALLENGES WORKSTATIONS FACE IN CAD/CAM

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SYSTEM FUNCTIONS

- VARIOUS DATA TYPES
- COMPUTE INTENSIVE FUNCTIONS
  - MATRIX MANIPULATION
  - FLOATING POINT CALCULATIONS
  - LARGE VIRTUAL ADDRESS SPACE REQUIREMENTS
- SOPHISTICATED GRAPHICS
  - HIGH SPEED RASTER OPERATIONS
  - COMPLEX GEOMETRY FORMS
  - SHADING AND RENDERING

Source: DATAQUEST

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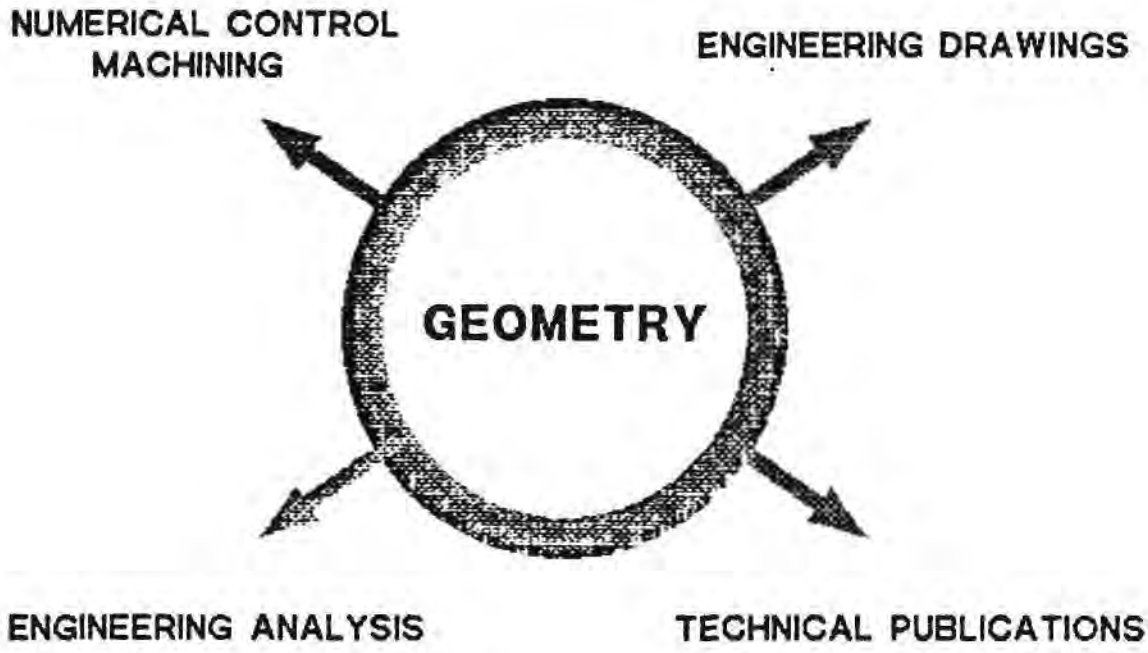
ENGINEERS CREATE, MODIFY, AND COMMUNICATE IDEAS THROUGH A LANGUAGE CALLED

"GEOMETRY"



Source: DATAQUEST

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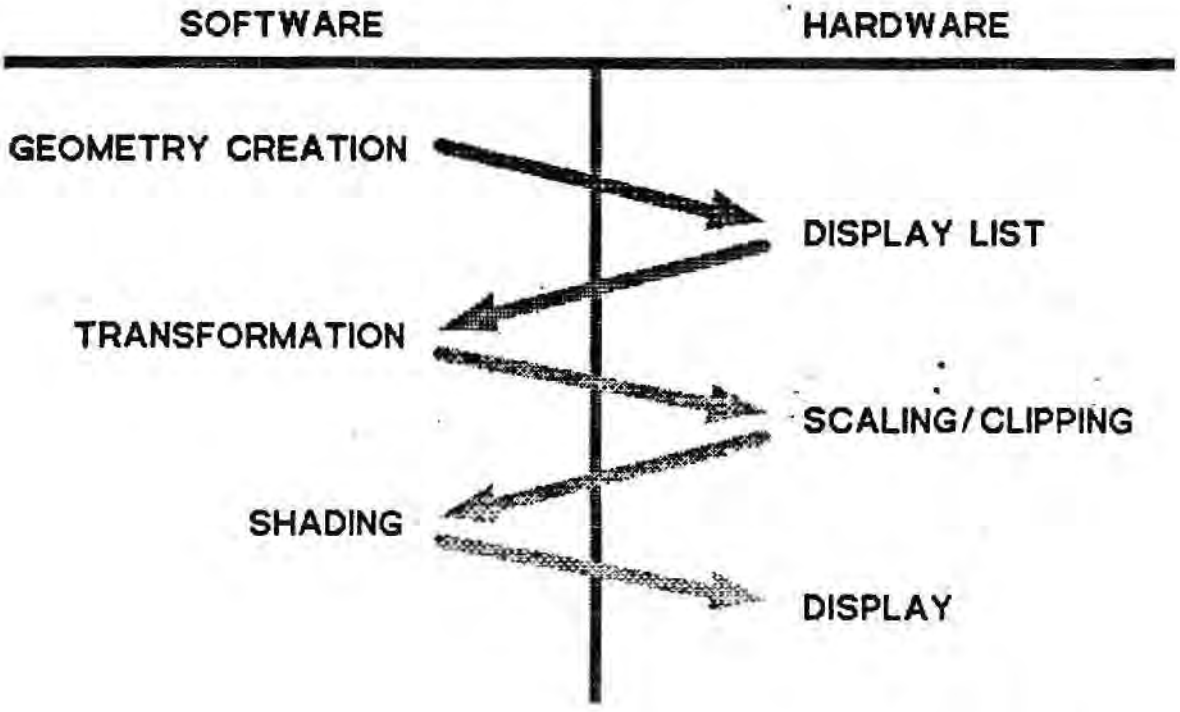
THE GRAPHIC PROCESS--PAST



Source: DATAQUEST

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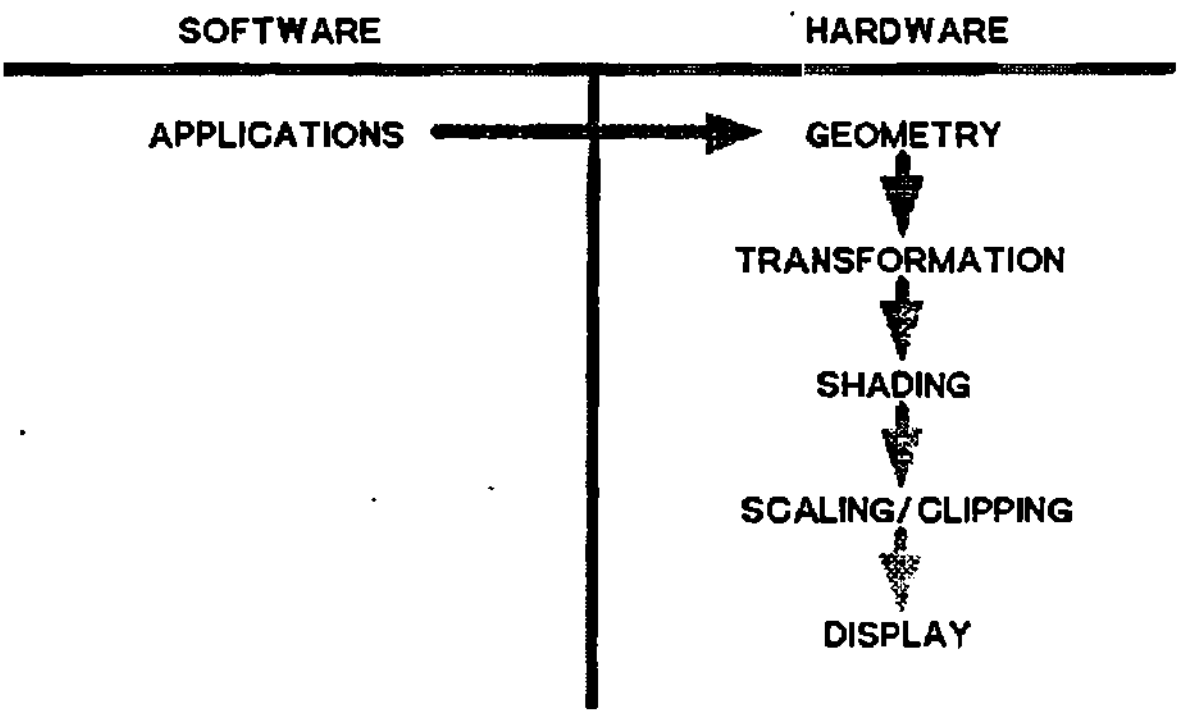
THE GRAPHIC PROCESS--TODAY



Source: DATAQUEST

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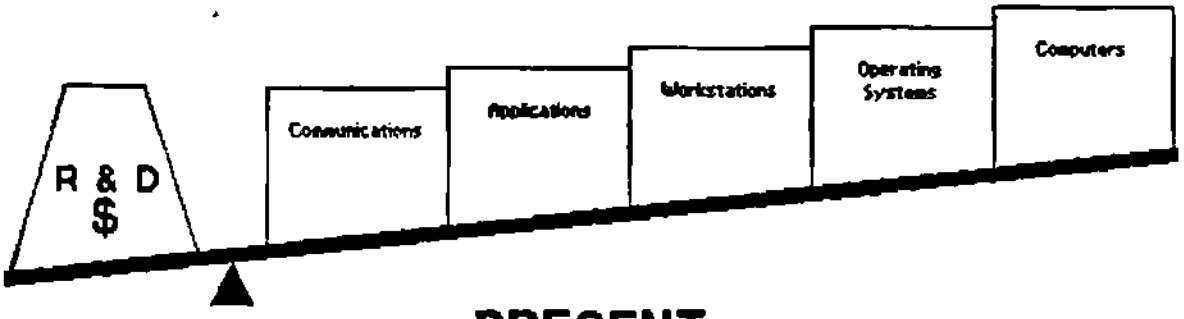
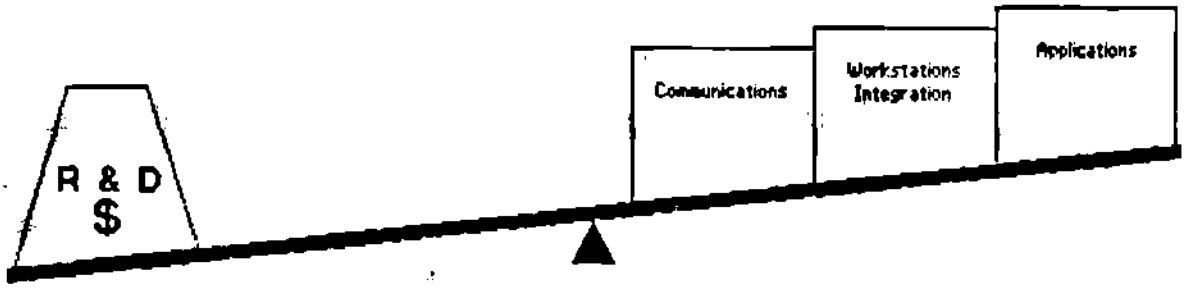
THE CAD/CAM OEM ENVIRONMENT

PAST



PRESENT



Source: DATAQUEST

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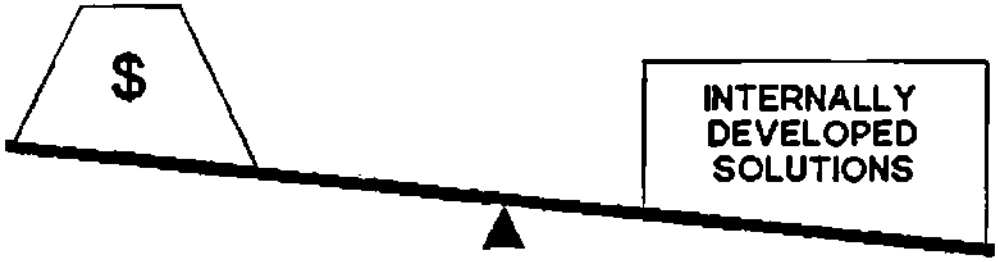
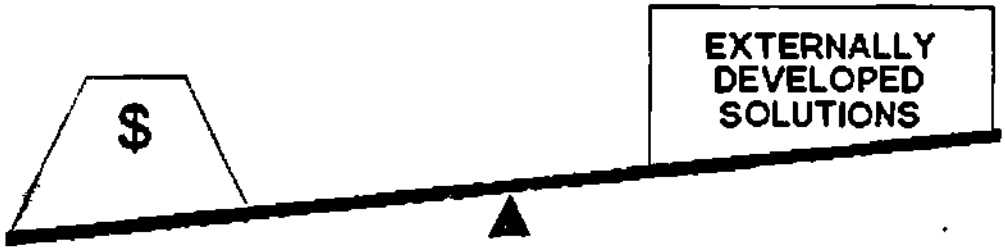
GROSS MARGINS

PAST

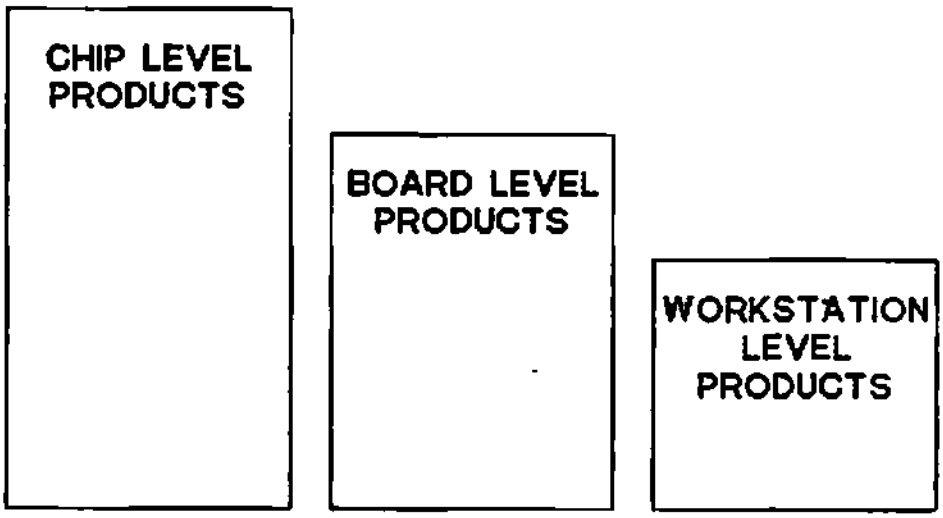


PRESENT



Source: DATAQUEST

DEGREES OF INTEGRATION



Source: DATAQUEST

TIME TO MARKET
VS.
DEGREE OF INTEGRATION

Source: DATAQUEST

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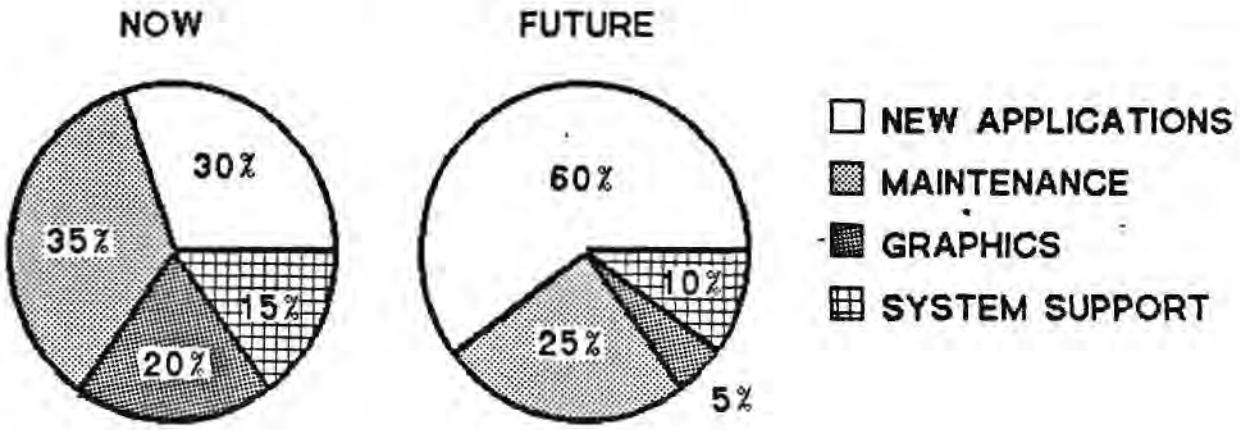
CAD/CAM SOFTWARE DEVELOPMENT MIX



Source: DATAQUEST

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THE NEW DEVELOPMENT ENVIRONMENT

- LOCAL VLSI FOR ALL GRAPHIC FUNCTIONS
- INCREASED PORTABILITY--REDUCED MACHINE DEPENDENCE
- VENDORS USING WORKSTATIONS FOR DEVELOPMENT--C.A.S.E.
- MORE EFFICIENT DATA STRUCTURES
- SMARTER COMPILING AND DEBUGGING TOOLS

Source: DATAQUEST

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WORKSTATIONS, THE TRANSFER OF TECHNOLOGIES

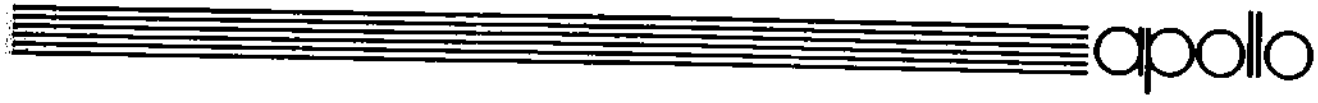
Dr. David L. Nelson
Senior Vice President
Apollo Computer Incorporated

Dr. Nelson is a founder of Apollo Computer Incorporated and has served as Vice President of Research and Development since the incorporation of the company in February 1980. From March 1977 to January 1980, Dr. Nelson served as Director of Research at Prime Computer, Inc. Prior to that, he was Manager of Research and Development at Digital Equipment Corporation. Dr. Nelson received a B.S. degree from the University of Wisconsin and a Ph.D. degree from the University of Maryland.

Dataquest Incorporated
WORKSTATION FOCUS CONFERENCE
August 13 and 14, 1984
Burlington, Massachusetts

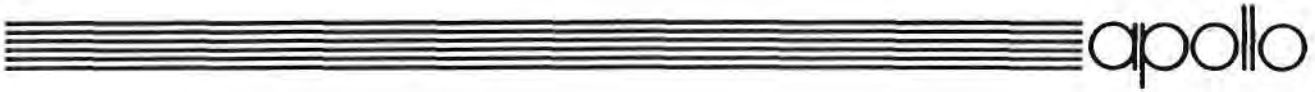
PERSPECTIVES ON THE COMPUTER INDUSTRY:

EMERGENCE OF WORKSTATIONS



COMPUTER INDUSTRY IS TECHNOLOGY DRIVEN

COMPUTER TECHNOLOGY HAS BEEN CONSISTENT AND PREDICTABLE FOR THE PAST 25 YEARS . . . BUT, . . .



. . . ALL TRENDS EVENTUALLY BREAK DOWN, CAUSING INTERESTING QUALITATIVE CHANGES.

apollo

TECHNOLOGY IMPROVEMENT RATES (1964-1990)

YEAR	KBITS/CHIP	K$/MIP	$(CPU+MEM)	MBYTE/MIP	IMPROVEMENT RATES MEMORY	PROCESSOR	SYSTEM
1964	0	$500	$1500	1.0	100%	30%	—
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1974	1	$40	$136	1.2	100%	30%	—
1976	4	$24	$52	1.4	100%	30%	61%
1978	14	$14	$24	1.7	90%	30%	50%
1980	42	$8	$12	2.0	70%	30%	38%
1982	107	$5	$6.8	2.5	60%	30%	34%
1984	273	$2.9	$3.8	3.0	60%	30%	34%
1986	700	$1.7	$2.1	3.6	60%	30%	33%
1988	1792	$1.0	$1.2	4.3	60%	30%	32%
1990	4600	$.60	$.70	5.1	60%	30%	32%

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TECHNOLOGY IMPROVEMENT RATES

CONSTANTS	VARIABLES
COST PER POUND	ELECTRONIC DENSITY
POWER PER CUBIC FT	BITS/CIP (70-100%/YR)
COST PER WATT	LOGIC (40%/YR)
COST PER CUBIC FT	DISK STORAGE (30%/YR)

AGGREGATE SYSTEM 30-40%/YR

$(1.35)^{7} \approx 10$

FACTOR OF TEN IMPROVEMENT
EVERY SEVEN YEARS

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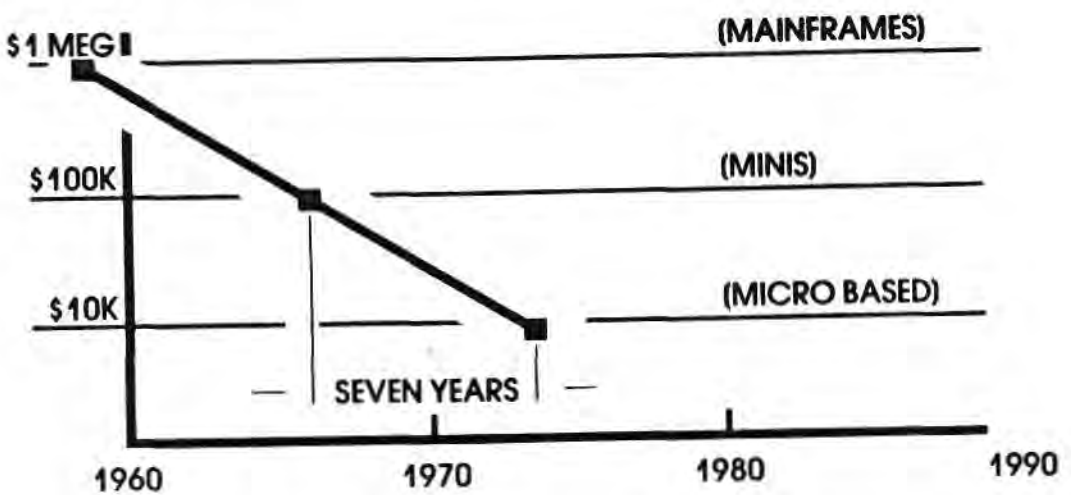
MARKET ENTRY POINT



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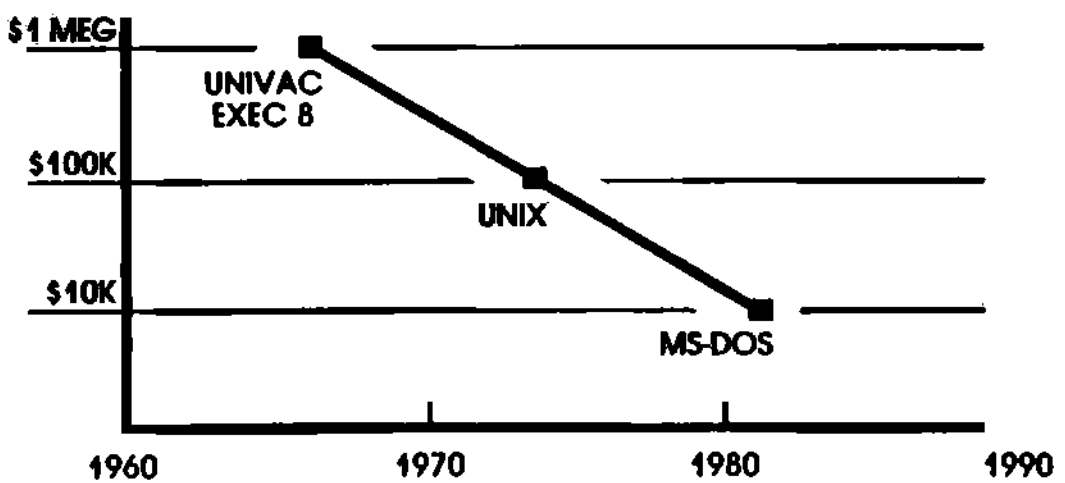
HIERARCHICAL FILE SYSTEM



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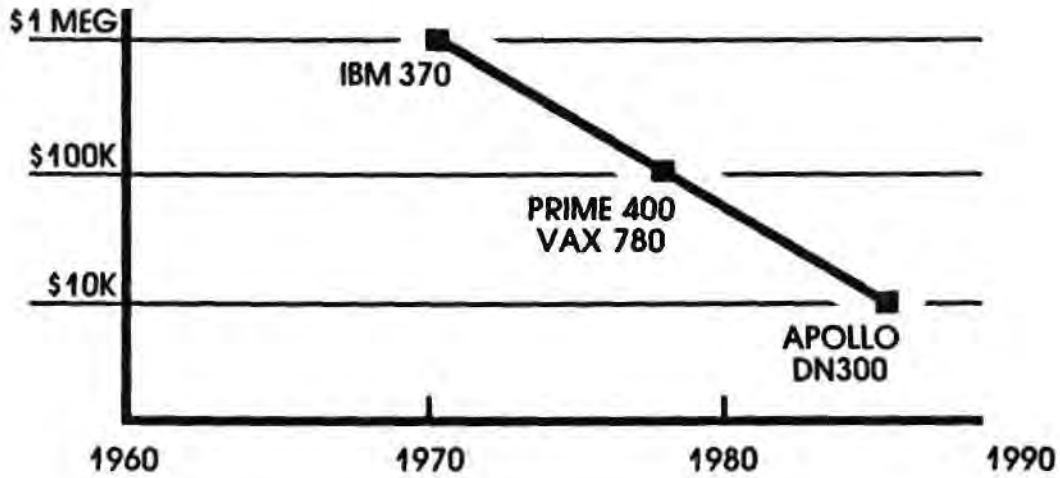
DEMAND PAGED VIRTUAL MEMORY



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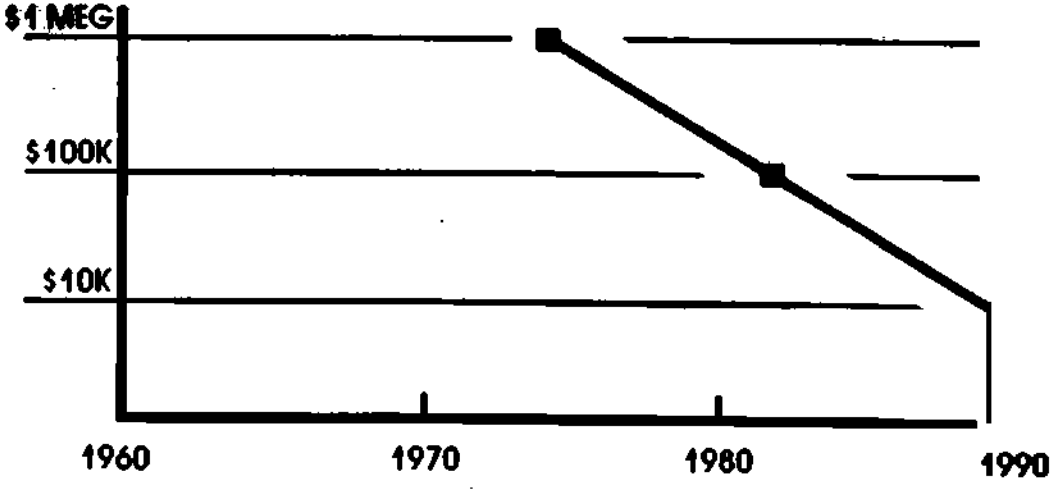
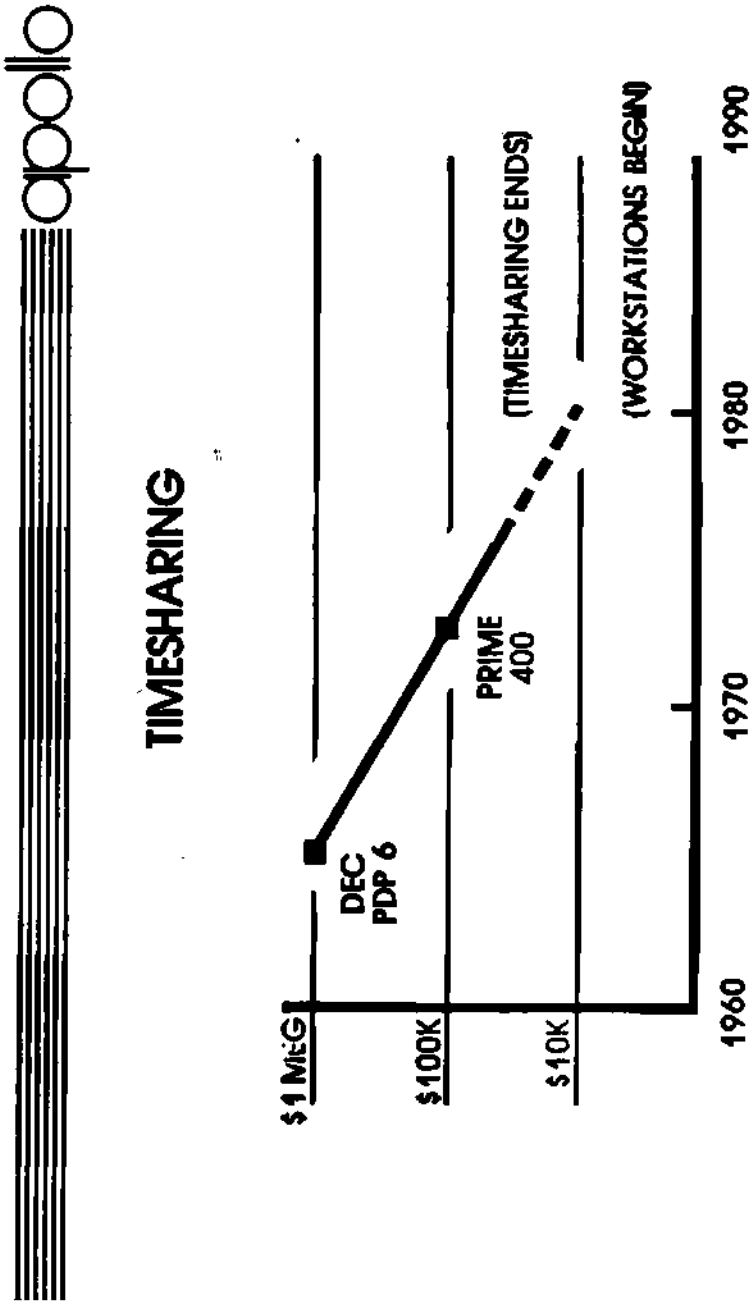
10 MEG BYTE SYSTEM

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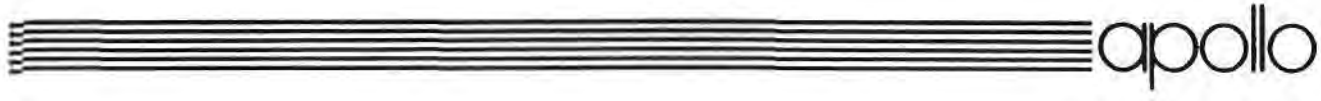
TIMESHARING
$1 MEG
$100K
$10K
DEC PDP 6
PRIME 400
(TIMESHARING ENDS)
(WORKSTATIONS BEGIN)
1960
1970
1980
1990



IMPLICATIONS OF THE END OF TIMESHARING

- OPPORTUNITY FOR QUALITATIVE IMPROVEMENTS IN THE USER INTERFACE (CONCURRENCY, WINDOWS, GRAPHICS, ETC.)
- PREDICTABLE LEVEL OF PERFORMANCE/USER
- REQUIREMENT FOR LAN AND A DISTRIBUTED SYSTEM ARCHITECTURE TO ALLOW EASY SHARING

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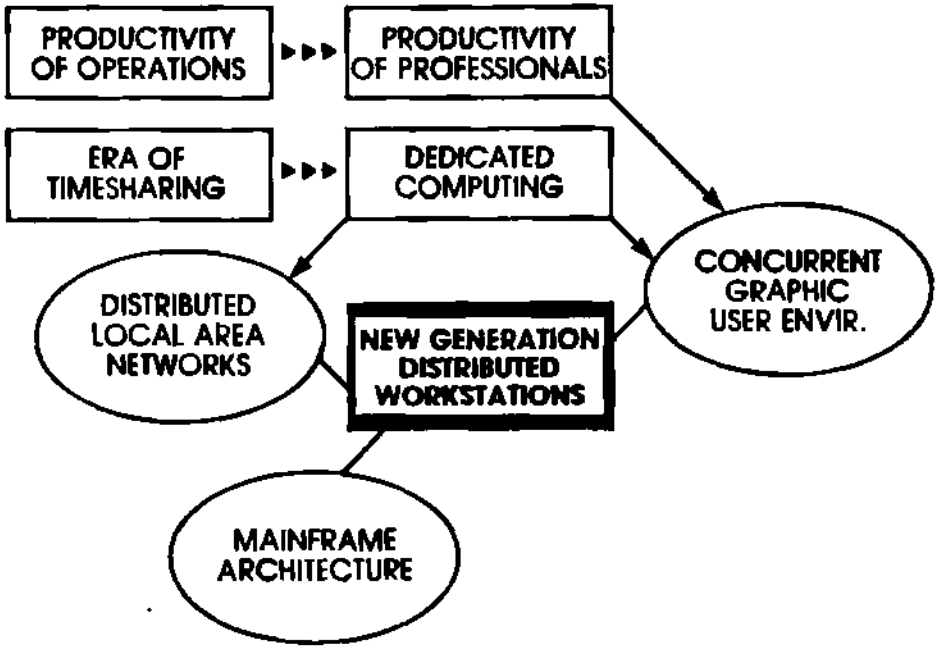

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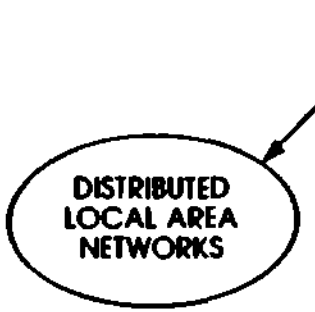
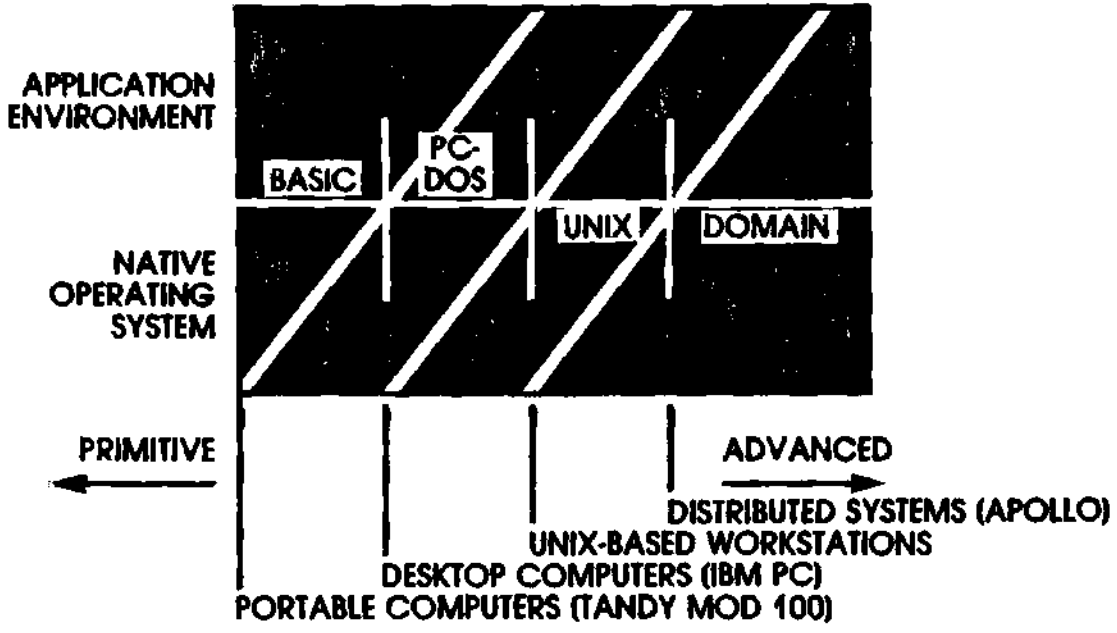


MAJOR ARCHITECTURAL PROBLEM:

- SERVICE PROTOCOLS
- NETWORK VIRTUAL MEMORY
- REMOTE PROCEDURE CALL

apollo



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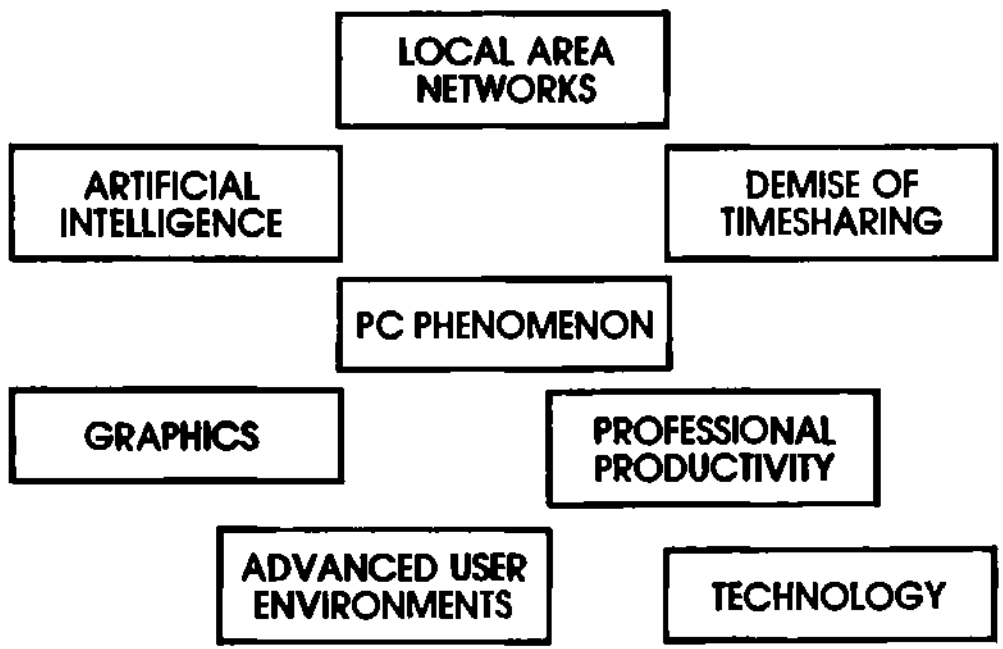
PREDICTED RAM/DISK MEMORY CAPACITY

	RAM MEM/DISK MEM (MEGABYTES)			
SYSTEM PRICE	1983	1985	1987	1989
$120K	4/200	9/400	20/800	45/1600
$ 60K	2/100	4/200	10/400	22/800
$ 30K	1/50	2.2/100	5/200	11/400
$ 15K	.5/25	1.1/50	2.5/100	5.7/200
$ 7.5K	.25/12	.5/25	1.2/50	2.8/100

→ INCREASING FUNCTIONALITY, CONSTANT COST

→ CONSTANT FUNCTIONALITY, DECREASING COST

ASSUMES: 50% IMPROVEMENT RATE FOR RAM
41% IMPROVEMENT RATE FOR DISKS



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FUTURE INFLUENCES

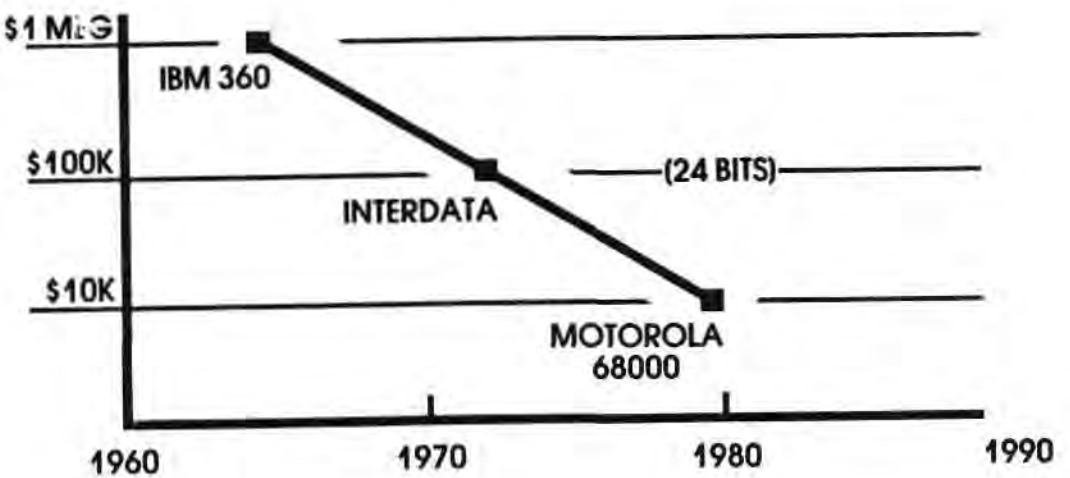
- CONTINUED PROGRESSION OF COMPUTING CLOSER TO THE USER (FROM CENTER TO OFFICE TO BRIEFCASE)
- EASE OF USE, "SEAMLESS" INTEGRATION
- GROWING INFLUENCE OF AI IN CAD/CAM
- LANS: FAST, LARGE, SWITCHED, AND GATEWAYED.

CONCLUSION

THE COMPUTER INDUSTRY IS WITNESSING A MAJOR TRANSFORMATION IN THE STYLE AND USE OF COMPUTERS . . . MORE SIGNIFICANT THAN TIMESHARING MORE THAN 15 YEARS AGO.

apollo

LARGE ADDRESS SPACE



The Role of Geometry in the Workstation Marketplace

James H. Clark

Silicon Graphics, Inc.
Mountain View, Ca.

Introduction

The workstation era in computing has evolved from the availability of 32-bit microprocessor CPU's, "portable" operating systems, programming language developments, declining memory costs, low-cost graphics, and communications networking technology. More recent developments have enabled custom VLSI technology to inexpensively increase graphics speeds by factors of several hundred or more. In this presentation, each of these developments will be discussed and applications that require geometric manipulation in their graphics systems will be highlighted. In the process, the historical roots of Bit-mapped graphics will be presented and contrasted with those of Geometric graphics. Particular emphasis will be placed on the applications that use each capability.

Computing Costs vs. Human Costs: 1974-1984

In the past ten years, the price/performance for a typical computer system has decreased from $1.5M/MIP in 1974 to about $40K/MIP in 1984, corresponding to roughly a 43% per year compounded decrease, as shown in Figure 1. During the same period, the burdened salary of a typical engineer has risen from about $36k/year to roughly $75K/year. In the early 1980's, for the first time the computer user was more expensive than the computer.

These trends indicated a need for both a professional personal computer and an efficient interface to it. Graphics has become this modern interface because it is such an essential part of engineering work. Thus the "workstation", as it is discussed here, is minimally defined as a combination of some form of raster graphics system with a general-purpose computing environment in one physical package.

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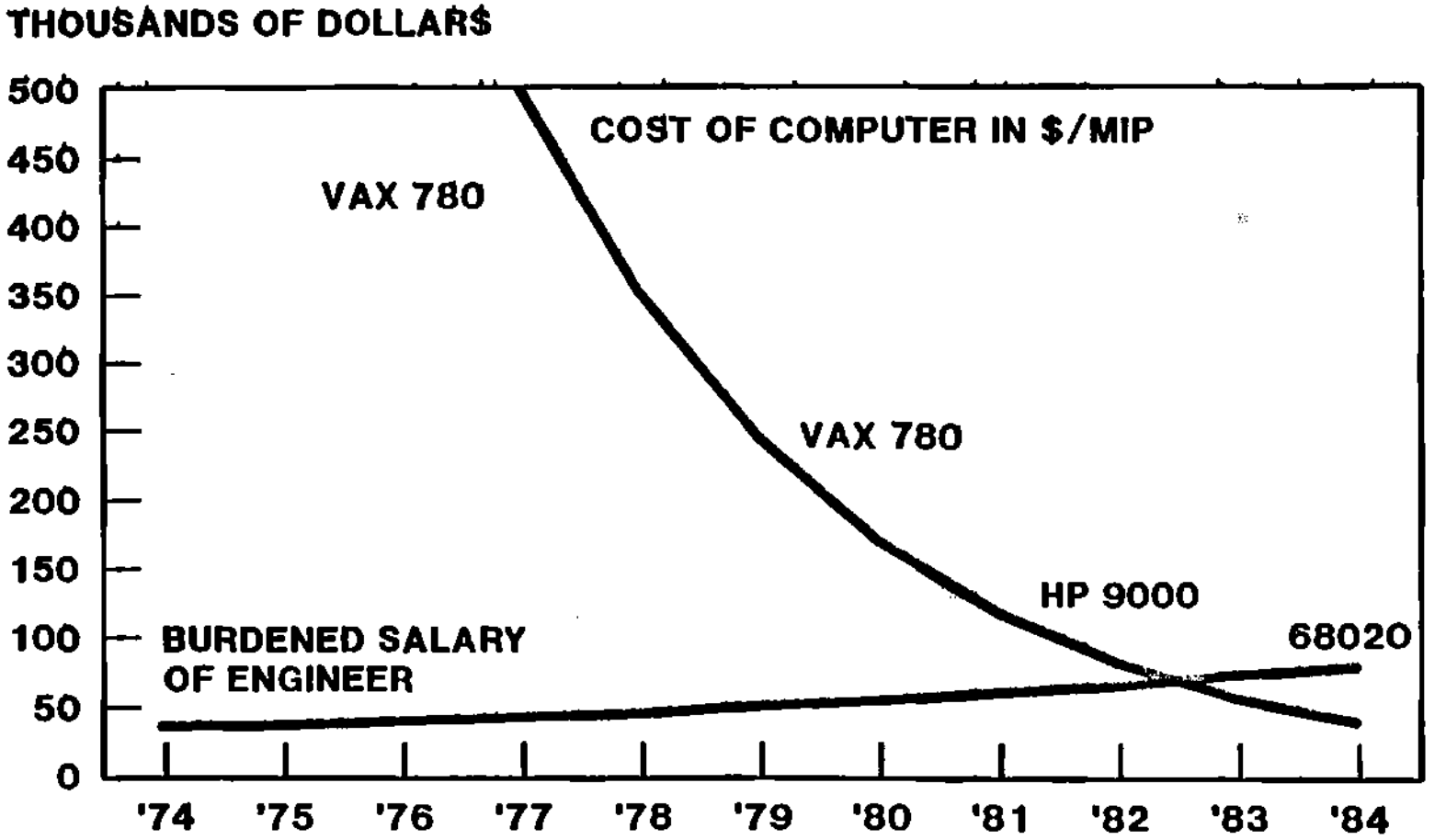


Figure 1: $/MIP vs. $/Person

The Modern Workstation Environment

The modern professional workstation provides a general-purpose computer that may be used alone or connected in a network with a wide variety of computing and support resources. A typical environment might consist of workstations, mainframe computers, terminals, hard copy media, database systems, and so forth as shown in Figure 2. Both high-speed computing and high-speed graphics are an integral part of this professional computing environment.

What distinguishes one workstation environment from another? In addition to cost, some pertinent issues are addressed by the following questions:

1. **Applications Environment** - Is the workstation general-purpose, allowing applications software for many applications on one machine? What applications are available on the workstation? How fast does it process an application?

2. **Computing Environment** - How are the workstations interconnected or networked? What are the Operating System, available languages and applications development tools? In the workstation's environment, can one do everything that is possible in a time-sharing system, such as share data transparently and work at any physical workstation?

3. **Graphics Environment** - Is the interface high-level, application (user-space) oriented and conveniently coupled with the computing capability? Is there support for 3D wire-frame and shaded pictures. How fast is it? Is it color or B&W, high-resolution? Is there multi-window support?

General-purpose Computing

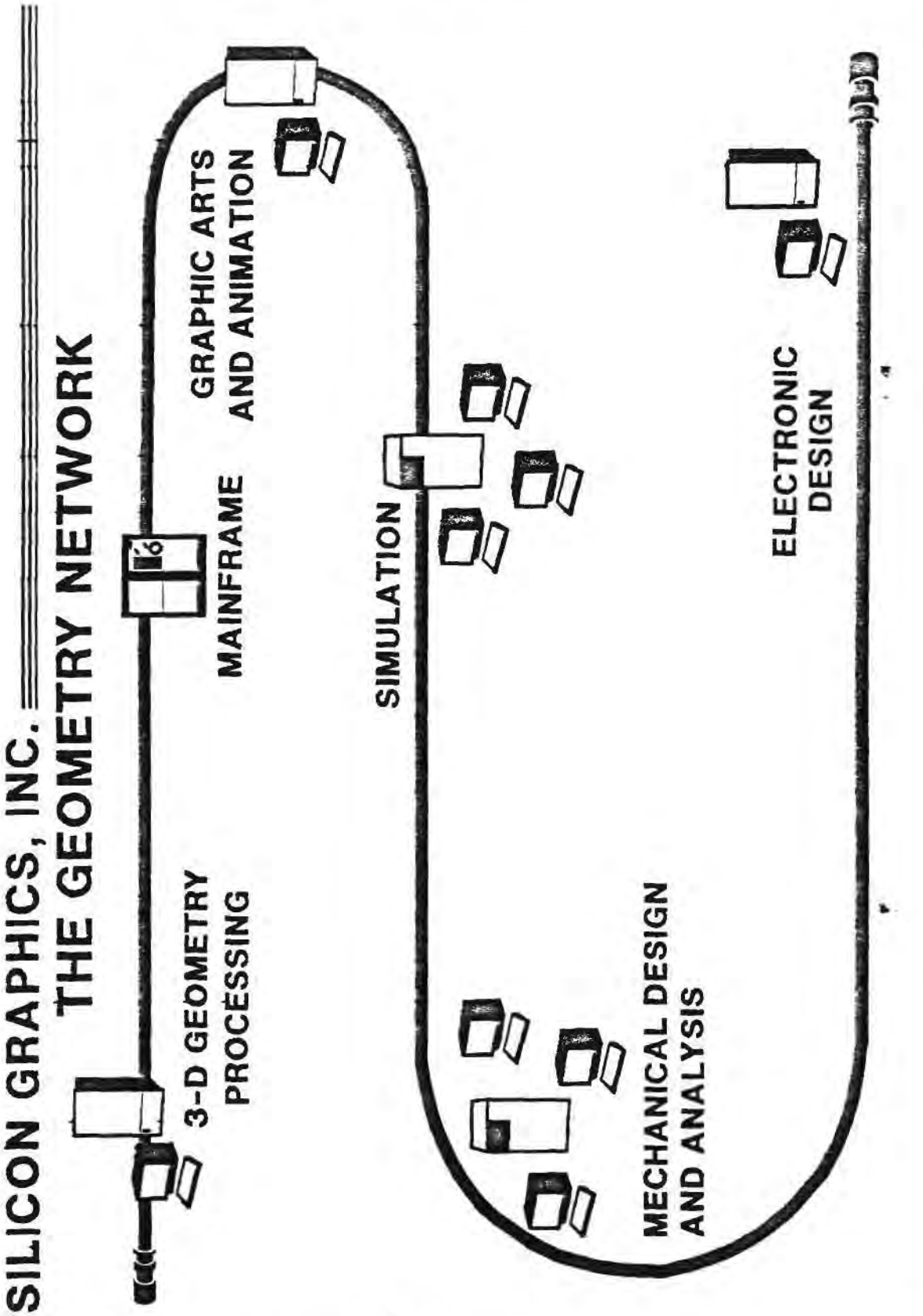
The computing capability of today's workstation is enabled by numerous technological developments, including

1. Declining costs and increased speeds of microprocessor CPU's, semiconductor memory and secondary storage media.

2. Improved operating systems, compiler techniques, languages and applications development tools.

3. Communications networking hardware and standard network software protocols for communication.

Figure 2: The Geometry Network



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General-purpose Hardware Developments

The 32-bit microprocessor available today has the computing speed of super-minicomputers of less than ten years ago. These microprocessors provide the foundation of most workstations' general-purpose computing capability. VLSI technology has moved the CPU from sets of discrete parts to custom integrated circuitry. Concurrent with microprocessor developments, Winchester disk technology is providing remarkable secondary storage capacities, while improved and more dense semiconductor memories continue to lead the revolution in computing systems. These trends are expected to continue to yield more and more powerful general-purpose systems for very low cost.

UNIX: The Portable Operating System.

If UNIX has not already become the de facto standard operating system for workstations and most minicomputers, it certainly appears to be on its way. It is the single most widely used operating system in universities -- thus virtually every technical undergraduate in the country is familiar with it. Moreover, there are more systems programmers for UNIX than for any other operating systems because Computer Science students have been able to access the source programs for UNIX -- UNIX was the first widely available "open" operating system. Developed in the early 1970's at Bell Labs, UNIX provides a rich and usable environment for applications development. The major question about UNIX in most people's minds is which version -- System V and successors distributed by Bell Labs, or 4.2 BSD implemented by the University of California at Berkeley.

The two systems have slightly different sets of utility programs, and each has features not in the other. The fundamental differences between them as they are distributed, and the effects on applications, are outlined below.

1. **Demand Paging** - With demand paging, physical memory may be less than the logical memory required by an application. Many engineering applications require a large virtual program and data space, and demand paging. In an engineering environment, this is the biggest shortcoming of System V as it is distributed by Bell.(Berkeley UNIX was developed primarily because of this shortcoming.)

2. **File Structure** - At Berkeley, it was felt that a different file system organization would provide faster file system performan than Bell UNIX. The mechanism used to speed it up is more effective only when the disk is 75%

utilized. When less than 25% of the disk is free, experience has shown that the system is not as fast as the standard UNIX file system.

3. **Network Protocols** - System V has no standard support for network communications and interprocess communications. 4.2 BSD incorporates a communications protocol defined for the ARPANET by the Department of Defense. (The development of 4.2BSD was funded by the DOD.) These modules are easily ported to any UNIX version, so it is of no particular advantage to any system.

The main point about any operating system feature is its effect on the application or its development. Demand Paging is essential to any engineering workstation and should be totally transparent to the application. The value of the reoraginzed file system is often debated, at least as implemented. Networking is essential today as well -- the shortcomings of 4.2BSD networking are treated in the next section.

The ideal engineering UNIX system is one that incorporates demand paging and utilities of both System V and 4.2 BSD with expanded networking features to enable a distributed system. Bell Labs will continue to support, develop and standardize UNIX, whereas UC Berkeley is not in the UNIX business. Thus an integration of the useful 4.2 features into Bell-distributed UNIX will probably dominate the UNIX workstation market eventually -- it leaves the applications development and support environment least affected.

Ethernet: The Open Network Architecture.

Any distributed workstation environment must support a means for sharing data and resources on a network. Two basic technologies are in predominate:

1. **Token Ring** - This communications technology requires that all resources on the network be in a closed loop. Each node is allowed to send information to another in the ring after a token passes it -- thus, messages are synchronized and require the active participation of all nodes on the network. The network must be disabled to install or remove a node, and it is therefore more susceptible to failures of any node.

2. **Ethernet** - The Ethernet is not a closed loop. An Ethernet module communicating with another first "listens" to the network to see if it is in use. If not, it sends its file or message to the recipient. A "collision" occurs if two different nodes simultaneously sense that the network is quiescent and begin transmitting at the same time. The message is garbled, so each must "back-off" and re-transmit its message after a randomly chosen interval, which decreases the likelihood that they will again simultaneously transmit.

Messages are asynchronous. Nodes are passive unless they are using the Ethernet, so they may be removed and inserted at will.

The most significant difference between these two technologies is that the Ethernet is an "open" architecture that has been adopted as a standard by Xerox, Intel, Hewlett Packard, Digital Equipment Corporation, Silicon Graphics, SUN Microsystems, and many others. All commonly used token ring approaches are "closed." No standard token ring approach has been widely adopted -- each company that employs it has its own closed system.

Network Protocols.

Both Ethernet and token ring require a protocol, or "language", for message transmission. There are two published standards being used in most Ethernet installations, XNS and IP/TCP.

XNS (Xerox Network Software) is a simple local area network communications protocol defined at Xerox PARC, where the Ethernet was invented. It has the advantage of being tailored for local communications, and thus has no excessive baggage associated with each message. IP/TCP was defined for the ARPANET and imposed on the Berkeley 4.2 developers by ARPA. IP/TCP has the disadvantage of having all baggage necessary to route messages to any point on the ARPANET, which is not a local area network, but is nationwide.

Distributed System

An open network architecture requires facilities other than explicit file transfers between nodes and remote logins to other nodes and foreign hosts. It should allow any system user to refer to and use any file on the system implicitly, without explicit file copy. More generally, it should allow a virtual "system call" or shell command -- where the command is actually executed should be transparent to the user. This encompasses the distributed file system notion and more.

Graphics: The Principal Computer Interface

Vision is the most used human sense, so quite naturally graphics has become our most important form of computer interface. As with computer systems, however, graphics systems vary in their suitability for certain applications. The goal of the engineering or technical workstation should be to provide a graphics system suitable for technical applications. The graphics system should be as close to the application as possible.

Two basic approaches to graphics are used in workstations, bit-mapped and geometric. Bit-mapped graphics was developed for page imaging applications and has operations tailored for image manipulation of single bit images. It does not extend conveniently to color. Geometric graphics was developed as a tool to assist in the design and analysis of engineering problems. Geometric operations are tailored for the manipulation and display of geometric objects in the frame of reference of the designer. It assumes that the image is a rendering, or artifact, of the geometric design process, not the object of it.

Bit-mapped Graphics

Bit-mapped graphics was first developed at Xerox PARC in 1974 for the Xerox Alto. This was the first professional workstation. Because of the nature of Xerox's business, it was designed primarily for page layout and imaging applications -- thus it used a bit-mapped raster display. The bit-mapped display is used in these applications because the image of a page to be produced on a laser printer is constructed from a large two-dimensional array of binary digits.

In the Alto, one microprogrammed processor did everything -- it was the graphics processor, disk controller, ethernet controller and central processor all in one. High-level language compilers were written for the Alto, and most programmers used them, but when something had to run very fast, custom microprograms were implemented for it.

A very important one of these custom microprograms was the "bit-blt", which means Bit Block Transfer. It was developed because of the relatively large amount of time required to draw, redraw and manipulate a page image on the Alto. With the bit-blt in microcode, one could more quickly modify a bit-image. Because construction of the bit image was relatively time consuming and generalized, bit-blt operations allow the image to be "un"-altered with the "exclusive or", and the image was infrequently regenerated.

The focus of bit-blt or bit-mapped graphics systems is therefore in creating, manipulating and storing a bit-image, as in page layout systems. They are specialized for such applications and do not use specialized, higher-level processors to assist in manipulations of geometric objects, such as most engineering applications require. Their primary benefit is that they typically utilize a single processor for everything, thus reducing their costs. The Apple Macintosh is the best realization of a bit-mapped graphics workstation.

Geometric Graphics Systems

Geometric graphics originated with Sketchpad, which is a graphics system implemented on the TX-2 computer at MIT in 1964 by Ivan Sutherland. As an engineer and scientist, Sutherland was interested in providing a graphical interface that allowed interactive, computer-assisted design of geometric engineering objects. In Sketchpad, objects were designed and manipulated in terms of the application's geometric coordinate system, or as we commonly say now, "user coordinates", "user space", or "world coordinates." The image created by a geometric graphics system is simply a rendering of the geometric objects being designed and manipulated -- it is not an important entity in isolation, since it can easily be regenerated from the geometric description.

Fundamental geometric notions in use today were defined in Sketchpad. Because the geometric objects are described in one coordinate system (the user coordinates of the application) while the renderings of these objects are described in another (the image or screen coordinate system of the display), the notions of "windows" (user-space), "viewports" (screen-space), and a means for "mapping" from one to the other were defined. Likewise, because a window on the user's drawing space might include only part of the whole drawing, "clipping" of information had to be performed before the mapping. Finally, because the user's application space is geometric, objects might be arbitrarily translated, rotated or scaled ("transformed") in the space and multiple "instances" of objects might be made before they are passed through the window, undergo clipping and so forth. Although Sketchpad was primarily a 2D system, it defined these concepts in a general way that was applicable to 3D design as well.

Design as envisioned by Sutherland was interactive and in real-time. Since the clipping and mapping functions defined in Sketchpad were very compute intensive, Sutherland

concentrated on hardware to perform the functions as fast as possible. The "clipping-divider" designed by Bob Sproull with Ivan Sutherland at Harvard University in 1968 was the first hardware implementation of a system to implement the concepts defined in Sketchpad. This device used SSI semiconductor technology and by itself require four 19 inch racks. In 1969, Sutherland joined the faculty at the University of Utah and with David Evans founded E&S Computer Corporation.

Working as a student of Sutherland's in 1972, the author designed the first completely three dimensional interactive surface design system. This system consisted of two general-purpose computers (a PDP-10 and an LDS-2 processor), a matrix multiplier, a clipper and perspective divider and an analog vector generator. The hardware was designed for the project, and it used more modern MSI technology. The system's output was directed to a dual-CRT head-mounted display designed by Sutherland. It used as input a mechanical, 3D "wand." The total system, excluding the PDP-10, required four nineteen inch racks of equipment and if produced and sold would have been priced at about $250,000. The geometric computing part of the graphics system was valued at about $70,000.

Starting in 1979, the author and coworkers at Stanford University began a research project with the goal of designing and implementing the first VLSI chip dedicated to these geometric functions. This chip, called the Geometry Engine, is shown in Figure 3. Twelve copies of the Geometry Engine chip arranged in processing pipeline shown in Figure 4 perform more than ten million floating point or integer operations per second.

The Geometry Engine is much more than a fast floating-point ALU. In addition to incorporating all of the processing necessary to do each of the geometric operations discussed previously, the Geometry Engine also performs perspective division, and rather than processing just vectors, it processes solid, color, and shaded objects. In addition, it generates parametric cubic curves and rational bicubic surfaces, which are important in the design of automobiles and aircraft. It is a customized floating-point array processor for graphics. Because it is implemented in custom silicon, the Geometry Engine is easily replicated and costs very little.

Floating-point chip sets currently available provide alternatives to the Geometry Engine, but they do not have floating-point divide -- they provide only the basic

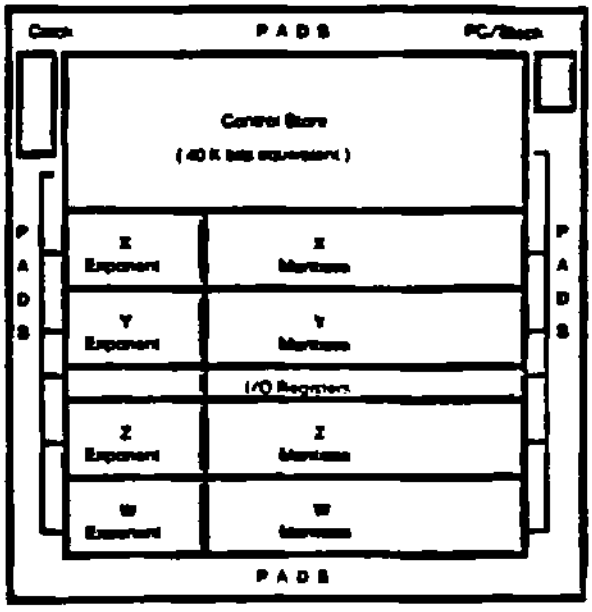

Figure 3: Geometry Engine Floor Plan

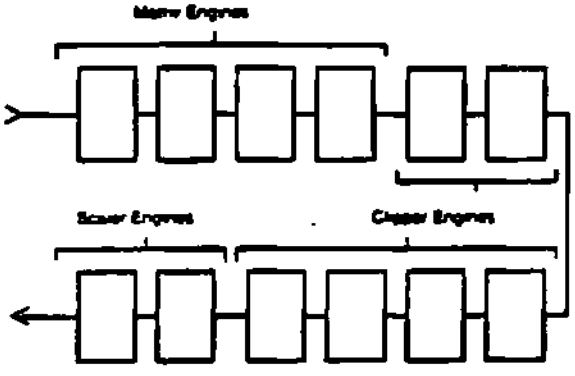

Figure 4: Geometry System

add/multiply/subtract math operations. Divides require other chips and support logic, and each divide requires substantially longer than the multiply, since it is a table lookup followed by at least three multiplies to obtain the requisite precision. Divides are essential for both clipping and 3D perspective geometric graphics. Moreover, these math chips alone incorporate none of the algorithms for processing graphical data or manipulating solid objects with shading. Thus, in order to accomplish the Geometry

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Engine's set of functions, substantially more hardware would be required in conjunction with these chip sets. The result is both more costly and slower.

User-space or Screen-space

From the above historical account, we see that the primary difference between Bit-mapped graphics and Geometric graphics is that Geometric graphics systems provide primitive operations that are relative to the coordinate system of the geometric application, while bit-mapped graphics systems focuse on primitive operations that are relative to the screen coordinate system of the bit-image application. Typical geometric graphics primitives are **rotate, translate, scale, line, polygon, surface** and so forth, all in the coordinate system of the geometric application. Typical bit-mapped graphics primitives are **bit-bit, rectangle copy** and so forth, all relative to the coordinate system of the raster hardware.

With the exception of the IRIS workstation by Silicon Graphics Inc., all workstations on the market are bit-mapped graphics workstations, and most of them are also black and white rather than color. This is because "bit-blt" and such operations are binary operations, meaning they deal with operands that are rectangular arrays of pixels that are a single bit each. Even those that are color treat the bit-planes that stack up to form a set of color planes in a bit-mapped manner. Those that incorporate Geometric graphics do so in software, with differences in speed by factors of several hundred.

Importance of Graphics Speed

Why is speed so important in a graphics system, be it geometric or bit-mapped? Some applications, such as simulation, absolutely require it. Others simply may need it to improve productivity, since workstations are interactive systesm, which implies that the user is waiting for a result to appear on the graphic display. If a graphics system cannot respond interactively, the user must do the task differently.

Some arguments occasionally support doing the job in a different way -- to use a more "batch" oriented approach. Sometimes this is the case -- interactivity does not replace thought. Batch-processing arguments were commonplace in the early days of timesharing, but "interactive engineering" is "productive engineering" in most of my experience, and if the graphics system can be produced for the same cost but much more

speed, the user is more productive. As Figure 1 points out, user time is now more valuable than computer time. With a slow graphics system user time is wasted, not computer time.

Why Design Our Own VLSI Circuits?

Fast geometric graphics makes no sense without special-purpose hardware to do the computations required. However, specialized hardware always adds extra cost. In the general-purpose computing area, microprocessors have ushered in the era of low-cost computing. In the geometric graphics domain, the Geometry Engine has ushered in a new era of low-cost geometric graphics.

More generally, however, the modern **system** designer must be able to design her/his own integrated circuits, because technology has provided the ability to put very complex **subsystems** on a single integrated circuit. Carver Mead has used the following argument: "In the limiting case, technology will allow us to put an entire system on a single integrated circuit. We will therefore either design that system ourselves or buy it from someone else." Although it is difficult to conceive of a complete system on only one IC, the argument provides an interesting perspective. The essential point is that as systems get larger it becomes increasingly difficult for the semiconductor manufacturer to second guess what the system designer would like for building blocks. Moreover, the building blocks require small scale circuits to "glue" them together.

Gate arrays and standard cells only partially solve the problem. Gate arrays do not currently allow very high densities. Perhaps worse, they do not currently provide a means for integrating RAM and ROM with logic. Standard cells, on the other hand, while allowing higher densities, impose a certain architectural style of thinking on the designer, since they are primarily used to replace the MSI building blocks that designers have been using. Each of these techniques allows faster implementation than full custom design, however.

Perhaps the biggest advantage of full-custom integrated circuits is in the architectural freedom they provide. This freedom can be exploited to employ parallelism in ways that are rare or nonexistent in other integrated circuit techniques. The Geometry Engine is one of the better known examples, but other highly parallel architectures dedicated to various special problems are certain to be in the future. Silicon Graphics Inc. will ensure

that the workstation marketplace benefits from highly parallel architectures for graphics and computing applications. System design now implies integrated circuit design The VLSI era is the era of the system designer.

Conclusions and Summary

From the foregoing remarks, the technical workstation should be a balanced combination of general-purpose computing and either bit-mapped or geometric graphics, depending upon the application.

For the computing part, demand paged UNIX is the preferred operating system, and it should provide both System V and 4.2 BDS utilities. For compatibility with the widest variety of other systems, Ethernet provides a more open network architecture than a token passing scheme, and both IP/TCP and XNS communications protocols are desirable. The communications file sharing environment should be as transparent as possible, allowing the "virtual system call" if possible. The ability to login to "foreign" hosts as an intelligent graphics or text terminal and transfer files are also important.

For the graphics part, pure page imaging applications are perhaps better served with Bit-mapped graphics systems. Most technical and engineering applications are better served with Geometric graphics systems. The geometric graphics system, being much higher level, requires extensive software to make the graphics easily used by the application -- drawing surfaces, curves and color, geometric objects in 3D user space should be as simple as drawing a line in screen space or modifying a pixel. Since technical work requires documentation, the system should provide means to produce it, allowing a mixture of text and graphics. The graphics system should also provide a multiple window environment that allows the user to multiplex between several tasks.

Speed in both computing and graphics are important, but slow graphical display tends to make the system non-interactive in engineering design and analysis. With a slow graphics system user time is waisted, not computer time. Silicon Graphics Inc. is dedicated to seeing that both the computing and graphics speed needed by engineering applications are treated on an equal footing.

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Nielsen Dataquest

THE ROLE OF PROPRIETARY ARCHITECTURES IN WORKSTATION DESIGN

David Folger
President/Chief Executive Officer
Ridge Computers

Mr. Folger is a founder of Ridge Computers and has served as President, Chief Executive Officer, and Director since the company was incorporated in 1980. Prior to joining Ridge, he worked at IBM Corporation, at Zilog, Inc., and Exxon Enterprises. He received a B.S. degree from Harvey Mudd College, and an M.S. degree in Electrical Engineering from the University of California at Berkeley.

Dataquest Incorporated
WORKSTATION FOCUS CONFERENCE
August 13 and 14, 1984
Burlington, Massachusetts

THE ROLE OF PROPRIETARY ARCHITECTURES IN WORKSTATION DESIGN

DATAQUEST FOCUS CONFERENCE
AUGUST 13 & 14, 1984

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RIDGE PERSONAL MAINFRAMES

- Mainframe computation performance for individual users
- Efficient handling of large programs and databases
- High performance, interactive graphics
- Software compatibility:
  - UNIX* System V (with virtual memory)
  - Berkeley 4.2 UNIX
  - Languages (FORTRAN, Pascal, C, MAINSAIL*)
- High performance network capabilities
- Office environment compatibility
- High reliability

* UNIX is a trademark of Bell Laboratories
Mainsail is a trademark of Xidak, Inc.

RIDGE

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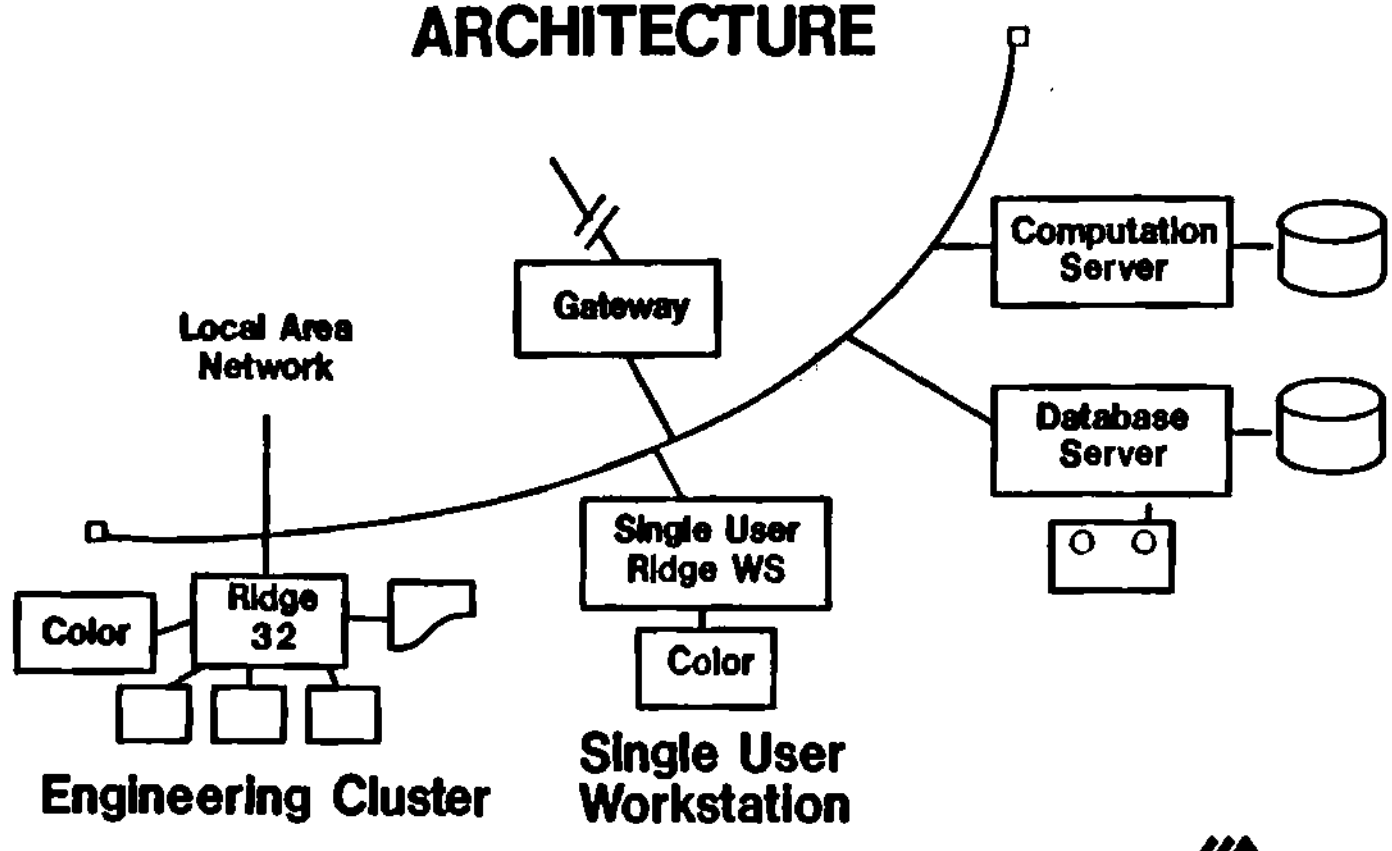
RIDGE NETWORK SYSTEM ARCHITECTURE



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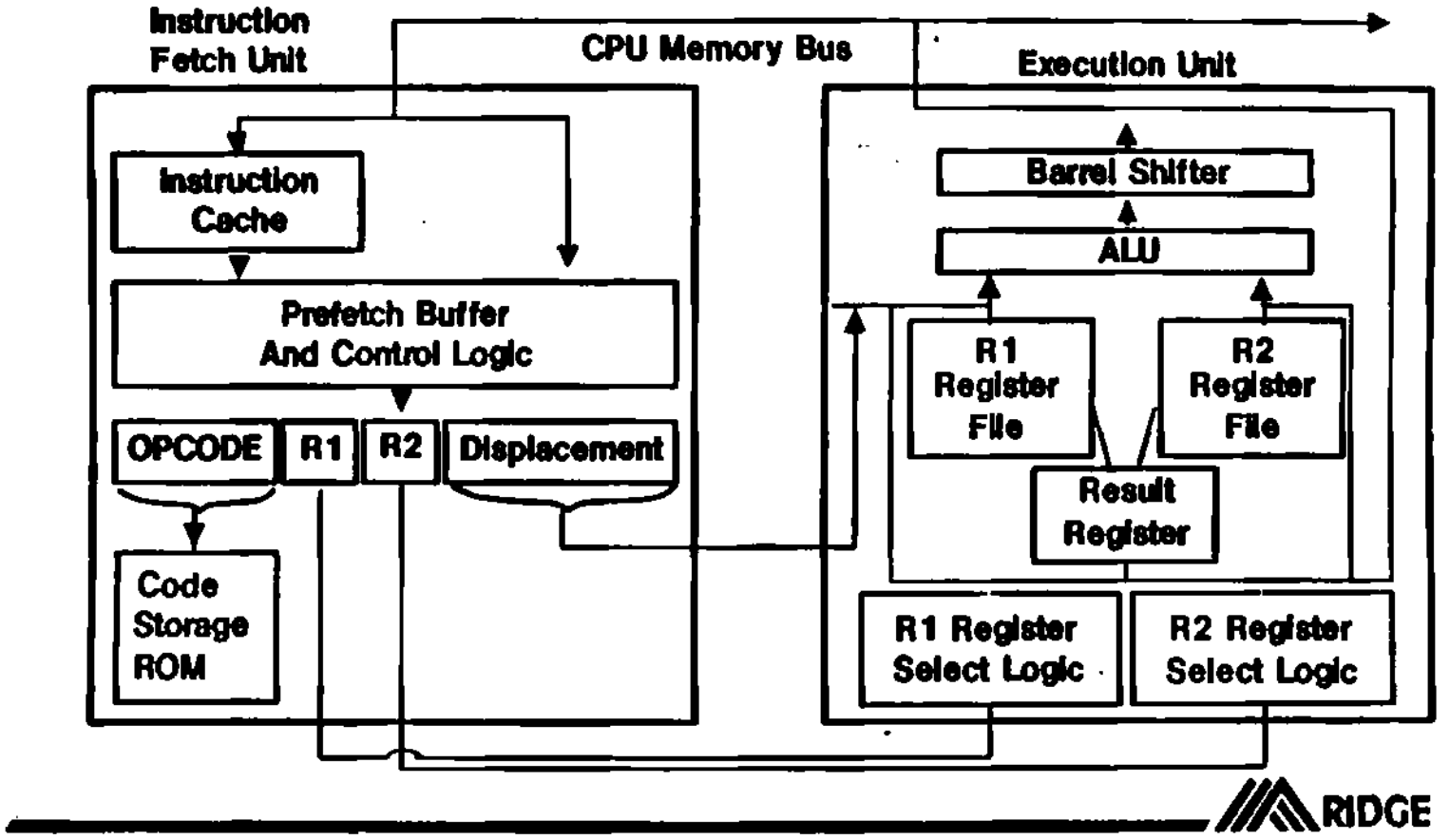
INSTRUCTION ARCHITECTURE

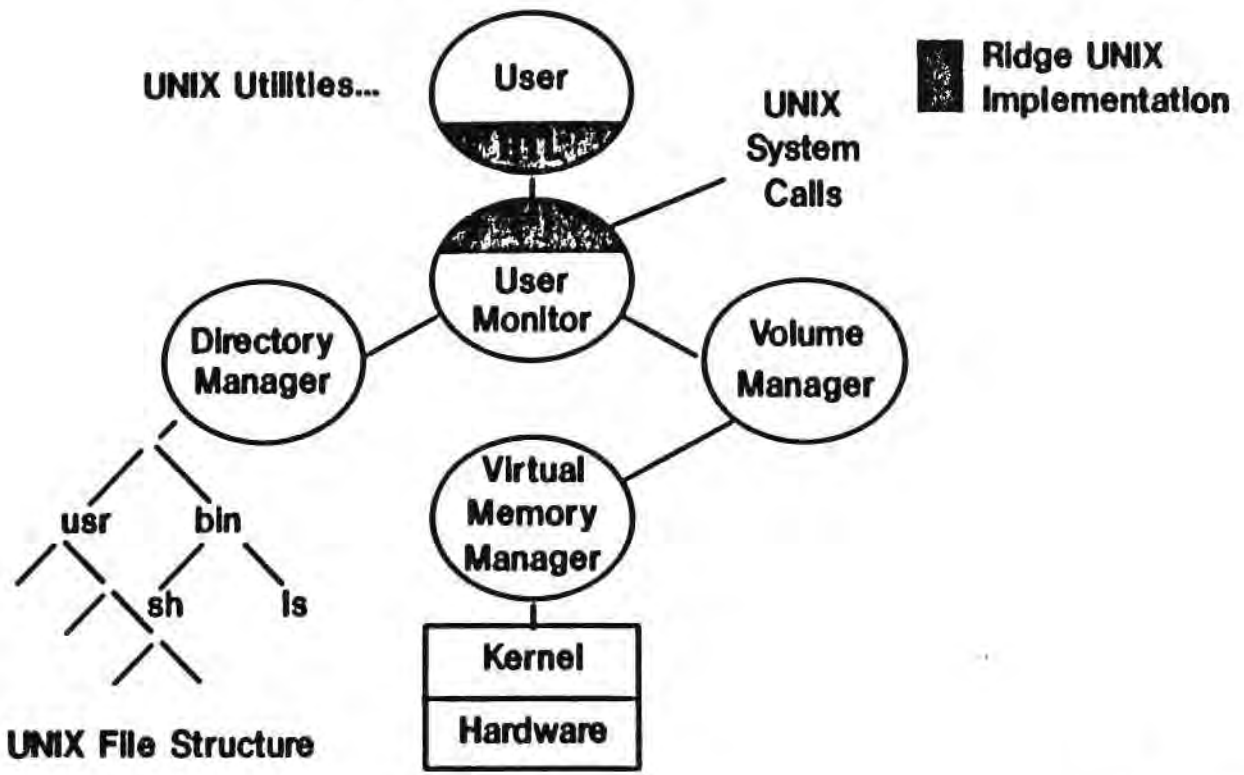
- RISC - Reduced Instruction Set Computer
- One instruction per 125 nanosecond clock
- No limits on addressability
- Register-Oriented
  - 16 General purpose registers
  - 16 Special registers for kernel use
- Load/Store memory reference format
- Clean instruction abort
- Compare and branch instructions
- Branch prediction

RIDGE

RIDGE 32 CPU INTERNAL STRUCTURE



ROS OVERVIEW



RIDGE

RIDGE SOFTWARE ENVIRONMENT

- UNIX System V with virtual memory
- Berkeley UNIX 4.2 enhancements

  4 G-byte code space and 4 G-byte data space
- Linear addressing with 32-bit addresses
- Shared code among multiple processes; private data space for each process
- Paged virtual memory
- Message-based interprocess communications:
  - Asynchronous and network transparent
  - Multiple incoming message queues
  - Links to other processes' message queues
  - Short messages (32-bytes)
  - Long messages for data and file access (4K-byte pages)

RIDGE

RIDGE 32 HARDWARE

- 32-bit, 8 MIPS CPU
- Up to 8M byte main memory
  60M, 142M, 445M byte Winchester discs
- 8" floppy disc
- RS-232 and printer/plotter ports
- Options (up to nine):
  - High resolution monochrome and color graphics
  - Ethernet
  - Magnetic tape system
  - Parallel interface

RIDGE

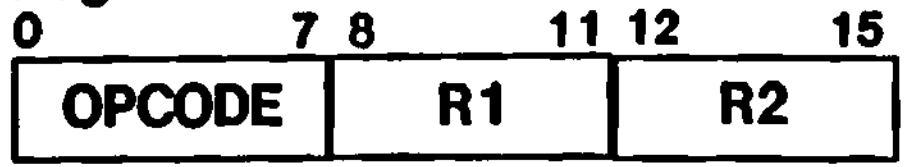
IPC UNIQUE FEATURES

- Short messages in registers
- Long messages copy page pointers
- Static links minimize overhead
- Data structures in per-process protected segments
- Kernel calls function as microcoded instructions
- 40 instructions to send, context switch, and receive message

RIDGE

INSTRUCTION FORMATS

Register

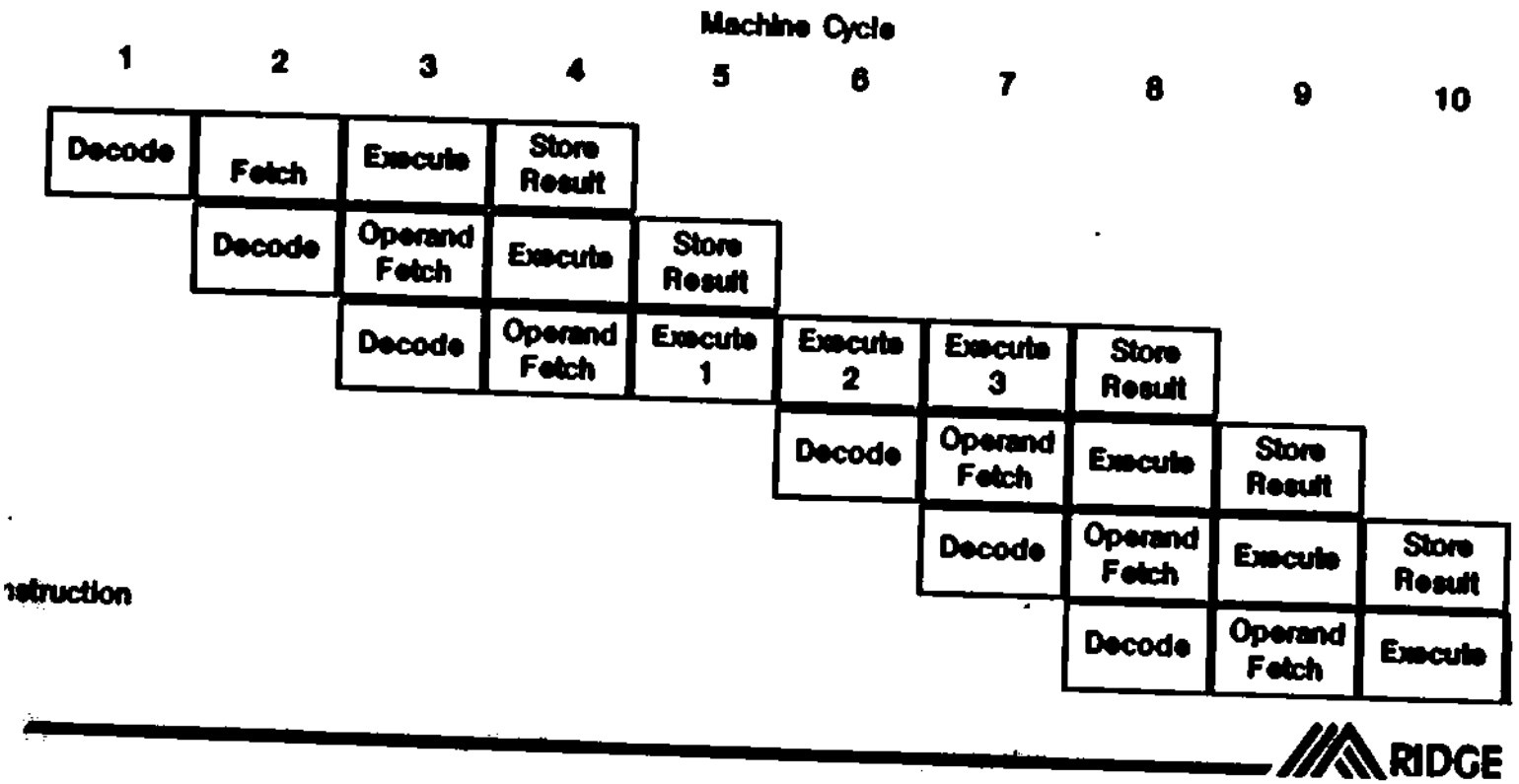


Short Displacement

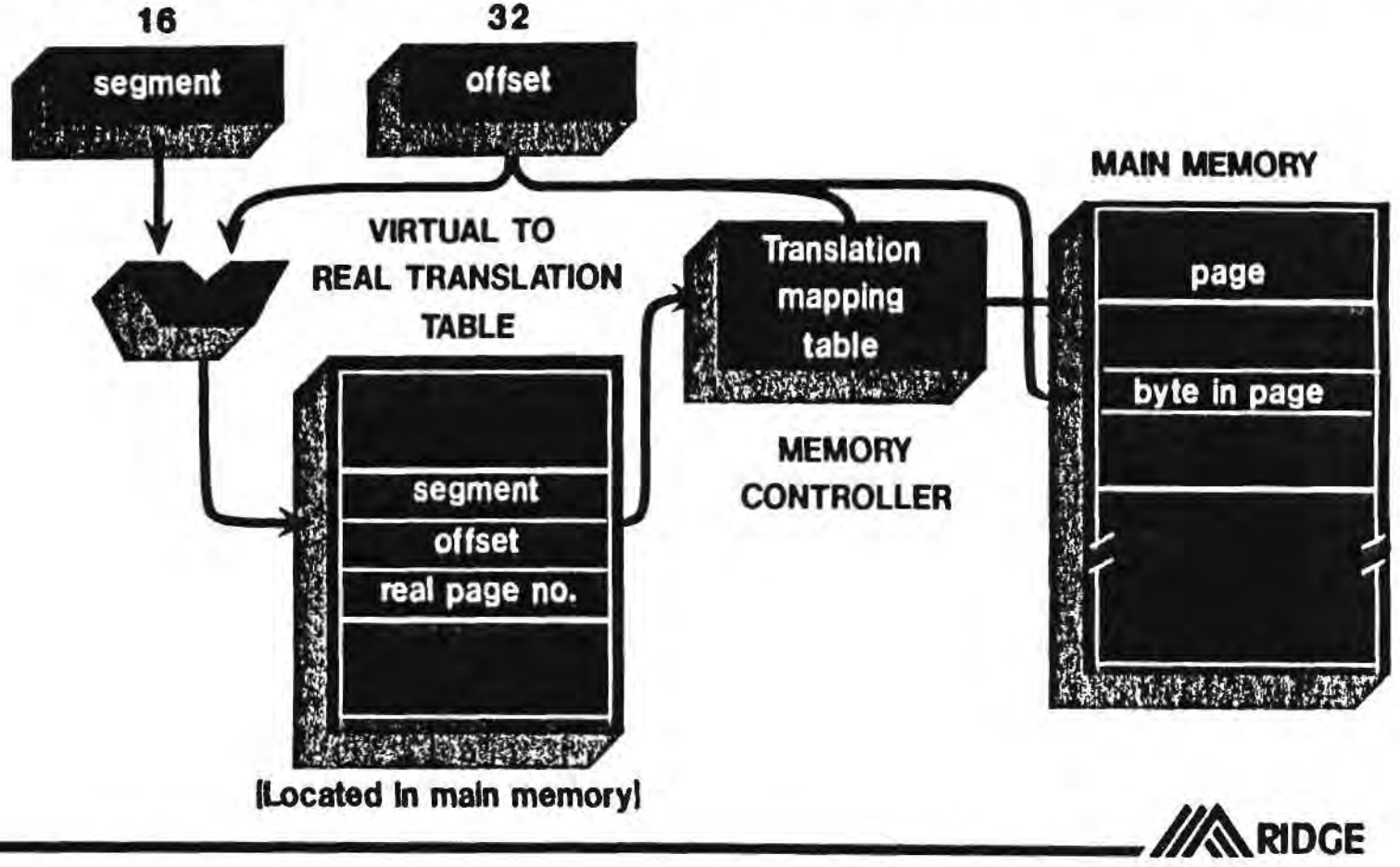
Long Displacement

RIDGE

RIDGE 32 CPU
INSTRUCTION PIPELINING

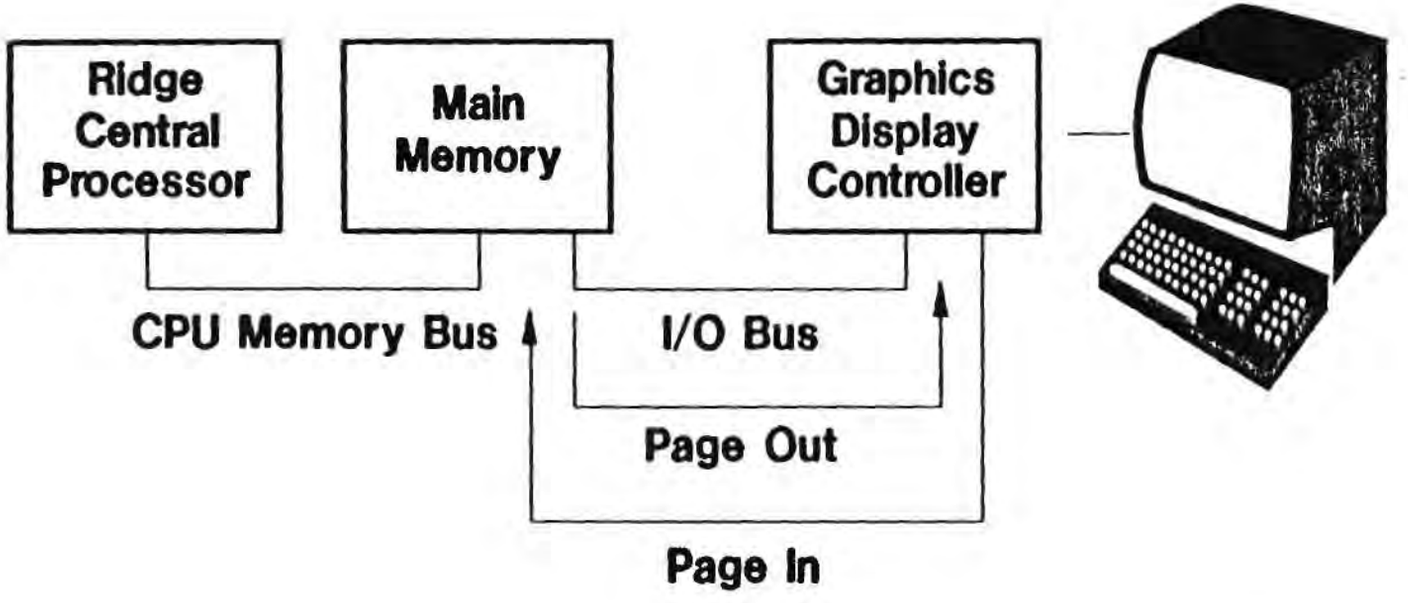


RIDGE 32 VIRTUAL ADDRESS TRANSLATION



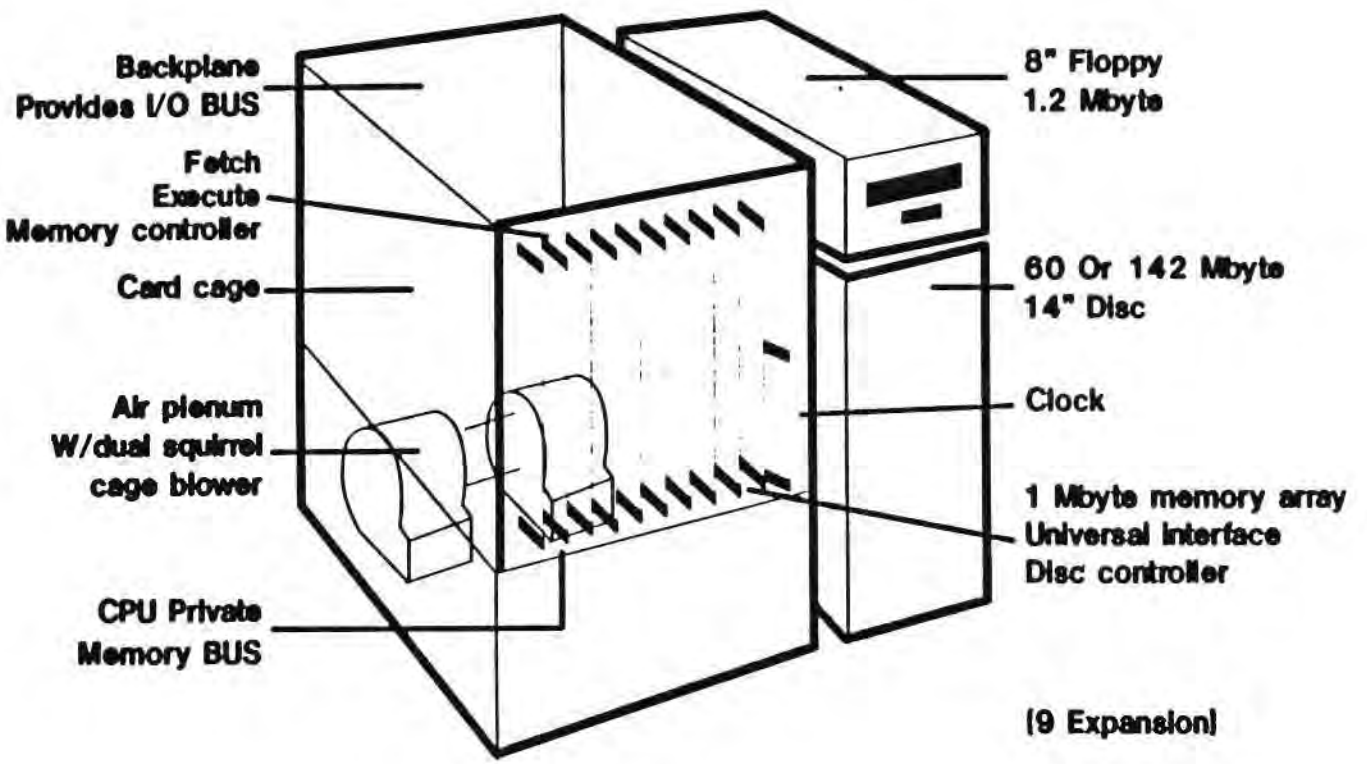
RIDGE

MONOCHROME GRAPHICS SYSTEM



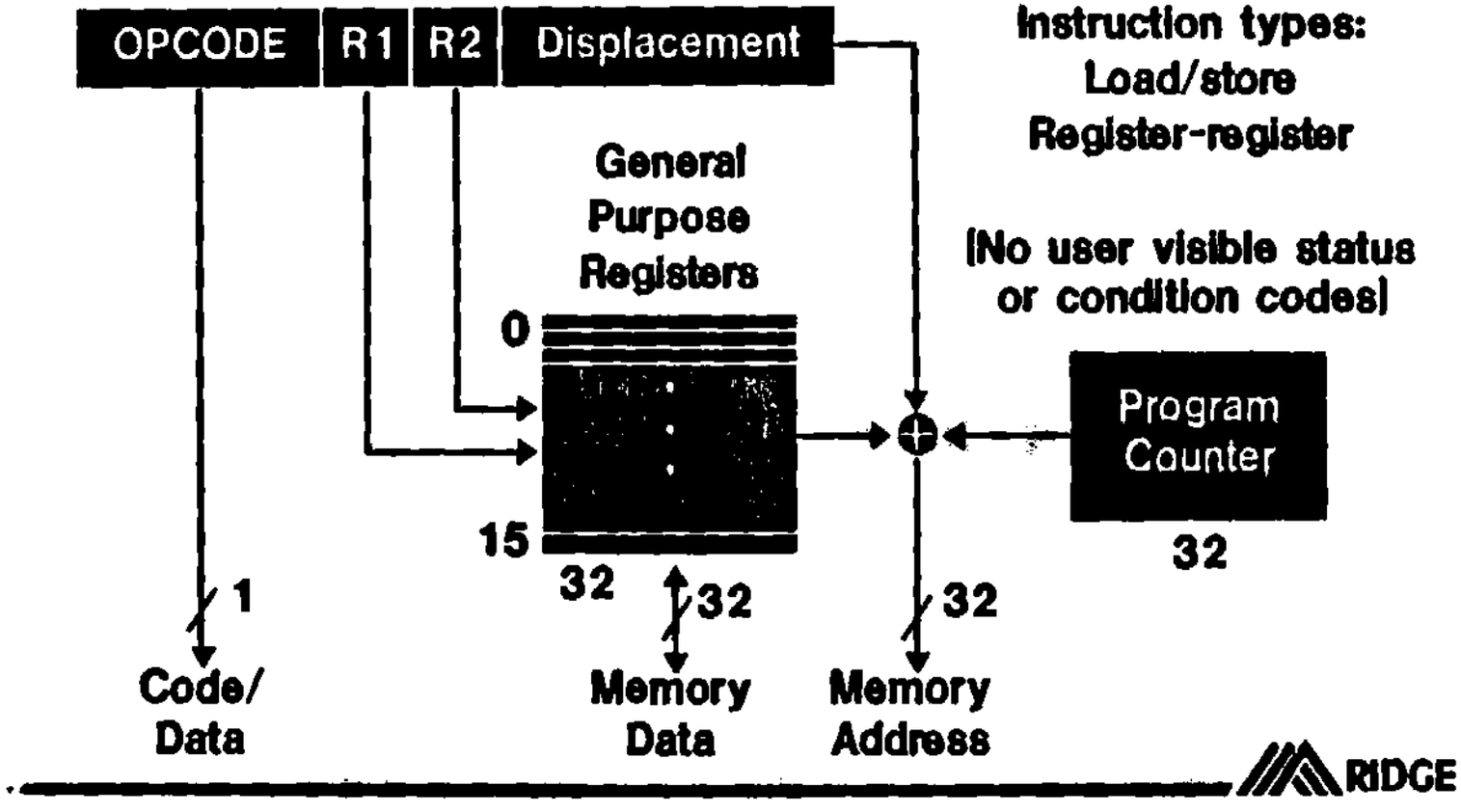
RIDGE

RIDGE 32 INTERNAL LAYOUT



RIDGE

SOFTWARE VISIBLE MODEL OF PROCESSOR



Nielsen Dataquest

SYSTEMS ARCHITECTURE--UTILIZING STANDARDS

Scott McNeally
President
Sun Microsystems, Incorporated

Mr. McNeally is President of Sun Microsystems, Incorporated, which he cofounded with three colleagues in 1982. Previously, he was Director of Operations at Onyx Systems, a microcomputer systems manufacturer. Prior to that, he was a member of the corporate manufacturing staff at FMC, and held various operations and sales positions at Rockwell International. Mr. McNeally received a degree in Economics from Harvard University, and an M.B.A. degree from Stanford University.

Dataquest Incorporated
WORKSTATION FOCUS CONFERENCE
August 13 and 14, 1984
Burlington, Massachusetts

SYSTEMS ARCHITECTURE UTILIZING STANDARDS

SCOTT MCNEALY

PRESIDENT

SUN MICROSYSTEMS, INC.

JULY 1984

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Architecture of a Scientific Computing Environment

Abstract

Scientific computing in this country needs a combination of technologies to accomplish research and development goals in the next few years. This article proposes an architecture for the scientific computing environment using microprocessor–based personal workstations accessing back–end computing resources. Systems built by multiple vendors will be connected using local network technology and standard network protocols. This paper describes the architecture of this new environment and the role UNIX will play in its emergence and growth.

Introduction

To provide a quality scientific computing environment we need to characterize the computing needs of scientists and engineers. We need maximally productive computing environments to offset the shortage of trained engineering and scientific personnel. We need productive engineering environments to compensate for the decreased lifetimes of products. We need an architecture which allows us to incorporate new technology easily and with minimal impact on users of the system.

Professionals need a responsive interactive system, the ability to run large computations and, in a laboratory environment, the ability to collect and analyze experimental data. Inexpensive microprocessor–based workstations with bitmap displays, leveraging the low cost of memories and virtual memory microprocessors such as the Motorola 68010 and 68020, provide cost–effective interactive response. Local area networks can tie such workstations to back–end machines: large superminicomputers, mainframes and supercomputers. Peripherals such as disks, tapes, communications interfaces and printers can likewise be shared by accessing them over the local area network. Data collected in a laboratory by a suitable embedded microprocessor can be moved to a personal workstation for graphical inspection, stored in a network–accessible data base, and processed on back end machines.

No single vendor can produce the component technologies to make this system cost–effectively. It is not possible for a single organization to simultaneously track advances in languages, user interfaces, data bases, graphics, specialized high–performance symbolic and numeric architectures and expert systems, let alone the many application areas for these component technologies. Multi–vendor systems will be required and must depend on standards to interconnect the components.

Architectural principles for the new environment

We now list seven architectural principles we see as key to the construction of a new multi–vendor open system environment. We seek a conservative synthesis of proven ideas so that we can have a high degree of confidence in the viability of the system architecture. All the principles and approaches proposed here have been proven in systems which are in use today; we have avoided ideas whose long–term value is unproven.

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1. Take a network service approach

We can identify two major approaches to connecting a network of personal machines. The first, which we call the network operating system or closed system approach, is typified by the Apollo DOMAIN system [DOMAIN] or the Locus system defined at UCLA [Locus]. These systems represent an attempt to extend the monolithic operating systems which were present on mainframes and superminicomputers to the local network environment. They tend to be inflexible, with a strong advantage to components of the system provided by the primary vendor over "foreign" peripherals.

The other approach is a loosely-coupled and open system design which gives network services primacy over the network operating system. An important system which first took this approach was the Pilot system [Pilot]. This model of a network system has also been incorporated in the Berkeley version of UNIX known as 4.2BSD, which derived the flavor of much of its networking subsystem from the Pilot design. These systems allow an open-ended set of network services to be defined, independent of the system calls of the operating system. Extensions to the system facilities occur in applications programs, not in extensions to the system. Thus the functionality of the system can be grown, the system can be developed and enhanced without touching the underlying operating system. This makes the code more portable and avoids disturbing the system with continual system interface changes: crucial goals which we stated earlier.

The 4.2BSD system contains sufficient facilities in the system interface that an open network system can be built without changing the system calls. Open systems derived from 4.2BSD and based on the network service approach are being constructed at Sun Microsystems and other vendors. 4.2BSD provides a portable and standard open-systems base for the new scientific computing environment.

2. Share resources while minimizing competition

Our measure of system performance sees quality in both predictable low-latency response and in high throughput. These are often contradictory goals. Dedicating peripherals gives low-latency response and high throughput, but is not cost-effective. In centralizing services we place predictability and responsiveness of the servers, and thereby the quality of the system, at risk. A central file server or compute server will be practical only if it does not become overloaded and thereby defeat predictable workstation response.

Sharing access to devices on a local network is essential to cost-effective computing. Disk drives, tape drives, printers and other peripherals are subject to economies of scale. Centralizing file servers provides a significant cost and maintenance advantage over systems where each user has only a local disk. For example, the larger capacity disk drives are both cheaper per megabyte of storage and also faster than the small, inexpensive disk drives which one can afford to provide with each workstation. Even if the costs were the same, considerations for shared data access and the difficulty of determining the amount of disk storage required by each user make it difficult to effectively provide each user with local disk storage.

Architectures for file server nodes to maximize throughput are an area of current study. Effective use of cache memories at server nodes should eventually result in server-based systems with performance equalling or surpassing that of systems which provide smaller and slower peripherals to each user. Nodes providing compute service can be scheduled in a job-shop or batch mode fashion, rather than timeshared, to increase predictability, and minimize competition, at the expense of some flexibility.

3. Provide a uniform base level of services

The simplest form of connections between machines is to allow file transfer, remote login and remote command execution. Providing these services to all machines in an

environment with uniform syntax should be a first priority. This level of service is the basis of the success of networks such as the ARPANET. Having this uniform level of services is far more important than any of the services described below and should always be provided for all possible machines.

Small, single task personal computers such as the IBM/PC or the Macintosh will have client telnet and FTP implementations so that they can access any file on the network, back themselves up to any other machine, and act as terminals to larger hosts. Larger hosts can exchange files in a symmetric manner, and a terminal attached to any of the larger hosts can serve to log in to any other host.

The DARPA standard TCP/IP/UDP (stream and datagram) transmission protocols, FTP (file transfer) and Telnet (remote login) protocols provide a widely-accepted and implemented standard for this base level connection. Ethernet provides a high-bandwidth and inexpensive, vendor-independent hardware interconnect.

4. Use standard operating system interfaces

In the microprocessor market there are several important operating systems. In the 8-bit world we have Apple/DOS and CP/M, in the 16-bit world MS/DOS, and in the 32-bit world UNIX and the new Macintosh operating system. Each of these defines an applications program interface for which large numbers of applications exist. Providing users access to one or more of these system interfaces can bring along a large number of applications at low cost.

UNIX is the most important operating system standard, because it runs on a wide range of machines. UNIX meets two needs: the need for a standard applications interface, and the need for a systems building block for constructing a open network system. The last version of UNIX to come from the research group which originated UNIX, Version 7, defines the basic applications interface for all widely used versions of UNIX. Applications programming features added in System V are not nearly as essential as the Version 7 facilities. We believe that the slightly extended Version 7 interface, as codified in the vendor-independent */usr/group* standard, is the best basis for an applications program standard. Further evolution of the system facilities from this base (with the exception of networking facilities) is, in general, unnecessary and undesirable.

4.2BSD is the only version of UNIX which defines a standard and stable yet extensible interface to networking facilities. Experience to date with the system suggests no major obstacles which need to be rectified. It will be several years before an alternative standard interface for a networked UNIX system can be developed. This suggests that adoption of the 4.2BSD network interface by the industry would be a positive step. Since an implementation of the interface is readily and freely available, it has already been adopted by a number of vendors.

5. Implement processes, monitors and remote procedure call

We believe that the extension of current systems to provide multiple processes per address space and monitors for synchronization should be the highest priority area of extension to 4.2BSD UNIX, because complicated interactive programs and network services are most naturally expressed using concurrency. Process/monitor technology as implemented in [Mesa] and [Modula-2] has been proven to work quite well to meet these needs. Operating systems such as UNIX do not provide support for these language facilities today. These facilities will be needed to be provided to support more modern languages, including ADA. The facilities can be added as library routines for use with older languages such as C. Extensions to C and UNIX to achieve this have been designed and implemented at Sun; we intended to publish them after further review, implementation, and use [Nugget].

We prefer to use these tightly coupled processes together with remote procedure calls [RPC] to build our distributed systems. This provides a clear distinction between local and remote programs. It also allows substantial hardware simplifications: with coupled

processes sharing complete address spaces, they avoid the need to share individual memory pages, avoiding *based* pointers, and allowing simplified hardware architectures as we can use data caches which do not need reference to translated addresses in the critical timing paths.

6. Have a uniform file system interface

Most operating systems now provide hierarchical file systems similar to the one provided in the original UNIX [UNIX]. Providing a network service which makes all files in the network environment available transparently is an enormous advantage. Operating system independence in the protocol is very desirable because, for example, we would like to be able to access the file system both from IBM PC's, Macintosh'es, and more powerful workstations such as the Sun, and use the protocol to access files stored on other systems such as VAX/VMS and IBM mainframes (that is, under VM/CMS). A networked file system based on these principles is being constructed at Sun Microsystems.

A dangerous trap to be avoided here is indefinite extension of the protocol for the network file system. We believe that the level of functionality of the 4.2BSD UNIX file system is adequate for the basic network file system, and that additional functionality such as that described in [Gifford] can be added transparently by different implementors of network file systems, without affecting the client code.

7. Access data base services using rpc protocols

We suggest providing data base access through applications-level network services, rather than as part of the operating system facilities. This allows a range of implementations of data base services based on applications needs, and can yield modular and well-specified systems. The distributed version of MicroINGRES, as currently available in a network of Sun Workstations, is an example of this style.

Both high-performance and high-availability systems can be constructed atop an efficient remote-procedure-call mechanism in a distributed environment. This architectural approach also allows construction of highly available or reliable data storage systems [Gifford] [ISIS].

Conclusions

The most important goal in creating a scientific computing environment is ensuring predictable response time. In a professional environment you often need access to more cycles than your workstation can supply, and these cycles can be cost-effectively supplied by back-end compute servers. A loosely coupled system permits a cost-effective mix of workstations and server machines to be used.

To build components for the next generation scientific computing system we must start by taking a network service approach. The most suitable base operating system to use is 4.2BSD, as its networking facilities can be used to write network applications and protocols without changing the programming interface of the system. Back-end computational and server nodes can be placed on the network and scheduled to provide predictable response time. 4.2BSD comes with remote login and file transfer services which can be extended to other machines in the network because the standard TCP/IP protocols on which they are based are available for a wide variety of machines.

The 4.2BSD system provides a standard applications interface, derived from UNIX Version 7, which meets the needs of most applications. You can look to the emerging vendor-independent */usr/group* standard for a definition of the common set of facilities to be provided. There is little to be gained by additional evolution of the programming interface beyond the facilities of 4.2BSD; most further evolution can take place using application-level protocols.

To support high-performance network services, we will need to extend the C language and program execution environment with support for lightweight processes and monitors for synchronization. Remote procedure call can be used to connect processes on possibly different machines, and is a natural extension of current programming styles.

The UNIX file system abstraction, as defined in Version 7 UNIX, and made less UNIX-specific in 4.2BSD, is a suitable basis for a network file system facility. We can avoid the temptation to make continual changes to the file system abstraction by dealing with data base services such as locking, transactions and fine-grained protection using applications-level protocols based on remote procedure call rather than building such functionality into the basic network file system.

A cost-effective and flexible system can be constructed, using the principles summarized above, without inventing new hardware or software technology, using 4.2BSD UNIX as a base. Forthcoming advances in microcomputer technology, cost reductions in memories, and high-performance supercomputers can then be easily integrated into our working environments.

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THE UTILIZATION OF ARTIFICIAL INTELLIGENCE IN DEVELOPING USER INTERFACES AND NEXT-GENERATION WORKSTATIONS

Richard Rifenburgh
Chairman of the Board--Chief Executive Officer
PERQ Systems Corporation

Mr. Rifenburgh, in his role as chairman of the board and chief executive officer, has developed PERQ Systems Corporation into a leading high-performance graphics systems company. He brought with him over 25 years of experience in the computer industry when he joined the company in 1983. Mr. Rifenburgh was formerly president and CEO of Mohawk Data Sciences Corporation. Since 1968, Mr. Rifenburgh has also founded or served as a director for a number of public and private companies including Rand Capital Corporation, a venture capital concern, and Sage Systems, an electronic office products manufacturer. Because of his expertise in the financial as well as the technical side of the computer industry, the Computer and Communications Industry Association elected Mr. Rifenburgh its chairman in 1984.

Dataquest Incorporated
WORKSTATION FOCUS CONFERENCE
August 13 and 14, 1984
Burlington, Massachusetts

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COMPUTER EVOLUTION

- Mainframes
- Minicomputers
- Workstations

EVOLUTION OF PROCESSING

- Mechanical calculators
- Numerical processing
- Symbolic processing

ASPECTS OF ARTIFICIAL INTELLIGENCE

- Problem solving
- Logical reasoning
- Language understanding
- Programming
- Learning
- Expertise
- Robotics and vision
- Systems and languages

PROBLEM SOLVING

- Search techniques
- Exhaustive searches
- Heuristic searches
- Backgammon, chess

LOGICAL REASONING

- Theorem proofs
- Data reduction
- Database query

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LANGUAGE UNDERSTANDING

- Natural language interfaces
- Speech understanding
- Language translation

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PROGRAMMING

- Automatic programming
- Learning programs

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LEARNING

- Example
- Performance
- Instruction

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EXPERTISE

- Expert systems
- Knowledge databases

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ROBOTICS AND VISION

- Industrial robots
- Object recognition
- Surveillance

SYSTEMS AND LANGUAGES

- Tools and ideas
  - Time-sharing
  - List processing
  - Interactive debugging
- Specialized programming languages
  - Lisp
  - Prolog
  - Planner

ARTIFICIAL INTELLIGENCE SYSTEMS TODAY

- INTERNIST/CADUCEUS - University of Pittsburgh
- PROSPECTOR - SRI International
- DIPMETER ADVISOR - Schlumberger
- DRILLING ADVISOR - Teknowledge/Elf-Aquitaine

INTERNIST/CADUCEUS

- 80% of all internal medicine
- 500 diseases
- 3500 manifestations of diseases
- Preparing to undergo clinical trials

OTHER EXPERT SYSTEMS

- **PROSPECTOR - Geological expert system**
- **DIPMETER ADVISOR - Oil well log analysis**
- **DRILLING ADVISOR - Drilling problem diagnosis**

PERQ WORKSTATION FAMILY

PERQ A1 (LN-3500)

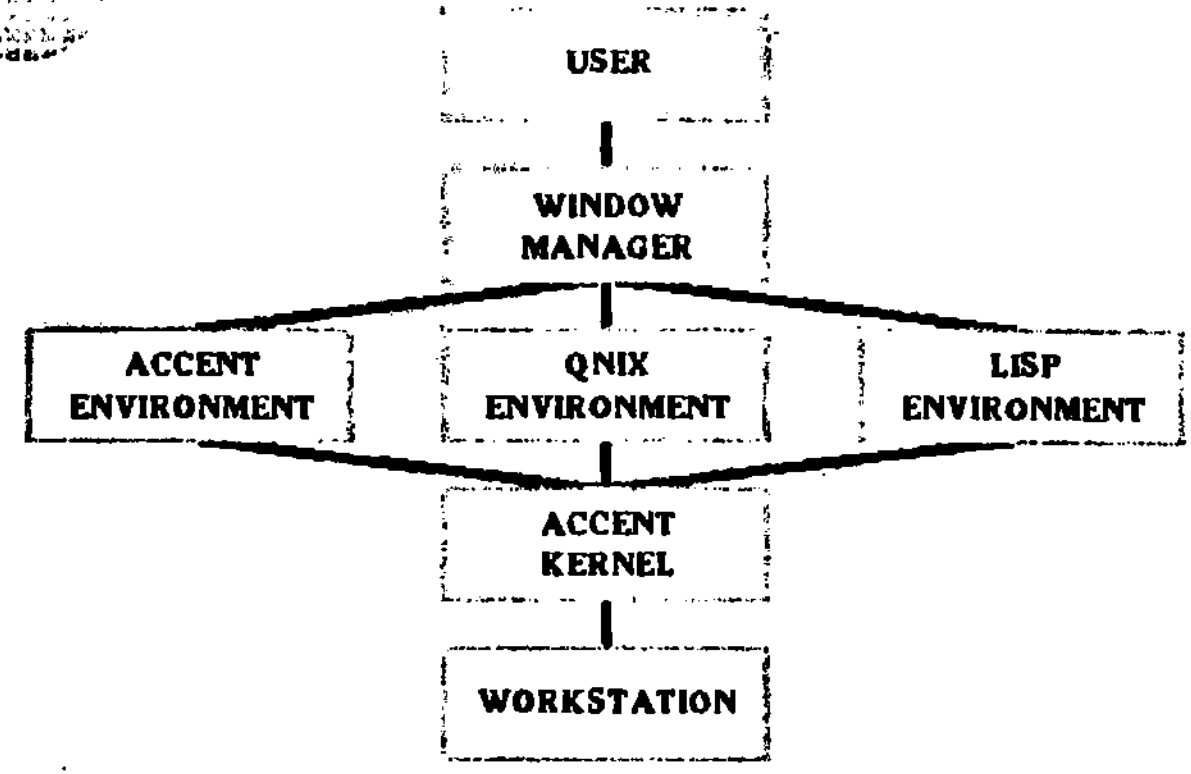
- **Common Lisp language**
- **Supermini performance**
- **Low cost - less than $40,000**
- **Based on ACCENT**
- **Operates with LINQ**

PERQ AI

LN-3500 CONFIGURATION

- **16K Writable Control Store**
- **2 Mbyte memory**
- **43 Mbyte 5 1/4" disk**
- **Landscape display**
- **Ethernet interface**

ACCENT OPERATING SYSTEM



ACCENT OPERATING SYSTEM

LISP ENVIRONMENT

- **Full common Lisp implementation**
- **Compiler and interpreter**
- **Screen editor based on EMACS and extensible in LISP**

ACCENT OPERATING SYSTEM

QNIX ENVIRONMENT

- **Complete UNIX System V environment, licensed from AT&T**
- **Provides System V system calls**
- **Over 150 utilities**
- **Use of the network is transparent**
- **Standard UNIX shell**

ACCENT OPERATING SYSTEM

NATIVE ACCENT ENVIRONMENT

- **Client-server paradigm**
- **Consistent user interface**
- **Screen oriented editor**
- **Over 100 utilities**
- **Integrated on-line HELP facility**

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ACCENT OPERATING SYSTEM

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CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

NATURAL LANGUAGE INTERFACES

- **Help systems**
- **Database queries**
- **Operating system interfaces**

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CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

SPECIFICATION WORLD

- Expert system
- Productivity aid
- Quality improvement

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CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

INTEGRATED DATABASE MANAGEMENT

- **Application oriented**
- **Constraint management**
- **Application based data links**

CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

CONTINGENCY MANAGEMENT

- Consistency checking
- Application specific
- Automatic reconciliation

CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

ON-LINE HANDBOOKS

- **Engineering handbook data**
- **Application relative**
- **Context oriented**
- **Ease of use**

CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

GOVERNMENTAL CODE CHECKING

- **Design verification**
- **Design recommendations**
- **Multiple regulations**
- **Safety considerations**

CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

CONSTRAINT LANGUAGES

- Engineering aid
- Equation solving

CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

INTERACTIVE APPLICATION DEVELOPMENT

- **Object oriented programming**
- **Programming development environments**

CAD APPLICATION EXAMPLE

FORMDRAW DRAFTING SYSTEM

- Expert system
- Descriptive geometry
- Architecture
- Process and instrumentation design

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CAD - AI IN THE FUTURE

JAPANESE FIFTH GENERATION

- 1982 ----- 10K - 100K LIPS
- 1992 ----- 100M - 1000M LIPS

CAD - AI IN THE FUTURE

FUTURE CAD SCENARIO

- **Design by specification**
- **Progressive clarification of requirements**
- **User design of aesthetics**
- **Machine generated implementations**
- **Automatic constraint reconciliation**
- **Extremely high interactivity**

THE UTILIZATION OF ARTIFICIAL INTELLIGENCE

IN DEVELOPING USER INTERFACES

AND NEXT GENERATION WORKSTATIONS

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COMPUTER EVOLUTION

* MAINFRAMES
* MINICOMPUTERS
* WORKSTATIONS

The driving force in Artificial Intelligence has been the availability of sufficient computing power to allow the implementation of interesting applications at a viable cost. Artificial Intelligence applications inherently require vast amounts of computational capability and data storage. The evolution from mainframes to minicomputers to workstations has brought the cost of computing per user into a range where economic application of artificial intelligence techniques is feasible.

EVOLUTION OF PROCESSING

* MECHANICAL CALCULATORS
* NUMERICAL PROCESSING
* SYMBOLIC PROCESSING

The very first computers were nothing more than mechanical calculators. As the first computers evolved they were in the main directed toward replacing the mechanical calculator. Therefore, computers were first programmed so that the internal states represented numbers. Numerical processing has been the basis of most business and scientific processing to date. However, there is no fundamental reason why the internal states of a computer need represent only numbers---the internal states of a computer could just as easily be representative of any symbols that we desire. It is this extension of the computer to the more generalized form of symbolic processing which is the fundamental difference between traditional computing and artificial intelligence.

ASPECTS OF ARTIFICIAL INTELLIGENCE

* PROBLEM SOLVING
* LOGICAL REASONING
* LANGUAGE UNDERSTANDING
* PROGRAMMING
* LEARNING
* EXPERTISE
* ROBOTICS AND VISION
* SYSTEMS AND LANGUAGES

In this talk I will not even try to tackle the problem of exactly what artificial intelligence is, since that is the subject of considerable debate and is best left to those who concern themselves with such things. It is often said that if it works, it isn't artificial intelligence anymore. Chess programs and spelling checkers were once the subject of much AI attention---today they are so commonplace that they are not generally considered to be AI.

Instead I will address the areas in which work is being done by AI researchers to give an overview of the breadth of what AI is and to give some food for thought as to how it might be applied to the CAD problem.

PROBLEM SOLVING

* SEARCH TECHNIQUES

* EXHAUSTIVE SEARCHES

* HEURISTIC SEARCHES

* BACKGAMMON, CHESS

The area that most people associate with AI is the generalized area of problem solving, particularly as it relates to games. In this class of problem you are generally evaluating a vast number of potential solutions to a problem to find the best one. Traditional programs approach this problem by attempting to evaluate every possible potential solution--- the so-called exhaustive search technique. While this technique is fine for simple problems, it falls apart when addressing problems like a best chess move, where there are literally billions of potential solutions to evaluate each time.

To resolve this problem, AI introduces the idea of a heuristic search. A heuristic search is done on the basis of some rules of thumb to narrow down drastically the number of potential solutions which must be evaluated. This is in fact exactly what a human being does when he considers a chess move. By narrowing down the number of solutions that must be evaluated, the program may not make the best possible move, but depending on the heuristics (rules of thumb) employed, it can make a good, in fact usually a very good, move. The process of interviewing experts in a given field to determine a good set of heuristics for a given problem is referred to as knowledge engineering.

LOGICAL REASONING

★ THEOREM PROOFS

★ DATA REDUCTION

★ DATABASE QUERY

The next area of interest to AI researchers is the area of logical reasioning. These programs deal with a set of data (or facts) and attempt to deduce from the facts, logical conclusions. One aspect of this is the proof of various mathematical proofs, given the facts associated with mathematics. Another more practical application is in the reduction of large amounts of data given facts about the logical relationships between the data. In an even more practical sense, logical reasoning is applicable to the day-to-day problem of database queries.

LANGUAGE UNDERSTANDING

* NATURAL LANGUAGE INTERFACES
* SPEECH UNDERSTANDING
* LANGUAGE TRANSLATION

One area which has received much publicity lately is the whole area of language understanding. The natural language interface is the most widely known application of language understanding, although speech understanding and language translation employ the same principles. An English natural language interface is in fact a language translator from English to a machine command language. One of the first applications of natural language interfaces was to the problem of database query to assist managers in accessing the often complex data structures contained in many common business applications.

PROGRAMMING

★ AUTOMATIC PROGRAMMING

★ LEARNING PROGRAMS

Automatic programming is the dream of many, but to AI researchers it is a solvable problem being investigated at many research laboratories across the country. Systems exist today which ask relative simple questions about a program specification and generate optimized, error-free code for a narrow range of expertise. The main advantage of these systems come in the area of program maintenance, where small changes to the specification can be made to fix the elusive bug, and a new set of error-free code can be automatically generated.

Another related area is programs which become smarter as they run. These programs change themselves over time in response to the user and its application. For example, a program may learn that you often mis-type a particular command in the same way, and adjust its syntax to compensate for your errors.

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LEARNING

* EXAMPLE
* PERFORMANCE
* INSTRUCTION

This leads to the area of learning systems in general. Unfortunately, this has been one of the least productive areas of AI research. Basically, learning systems learn by example, by actually performing a task and observing the result, or by the user instructing the program as to how to perform a particular task.

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EXPERTISE

* EXPERT SYSTEMS

* KNOWLEDGE DATABASES

Clearly the most touted area of artificial intelligence is the area of expert systems. In simple terms an expert system uses rules (heuristics) in conjunction with a data set in order to reach conclusions about a particular problem. The rules are generally derived by knowledge engineers working with established experts in a particular area to develop a set of heuristics that possess much of the reasoning power of the expert himself. While the systems generally cannot be any better than the expert himself, its ability to process larger amounts of data with much higher consistency often produces results that are, practically speaking, beyond the capability of the expert upon which it is based.

ROBOTICS AND VISION

* INDUSTRIAL ROBOTS
* OBJECT RECOGNITION
* SURVEILLANCE

In terms of practical applications, robotics represent the largest market to date for applied AI systems. While the robot market in the US has been relatively slow to develop, the Japanese have been far more agressive. As a result many companies in the US have active programs in place to close the robot gap.

Tied into robotics are vision applications both for robots and for vision generally. Much of the early research in vision has centered on object recognition and comparison for robots and for inspection systems. In surveillance systems changes in camera images are processed to determine the precise nature of the change.

SYSTEMS AND LANGUAGES

★ TOOLS AND IDEAS

- TIME-SHARING
- LIST PROCESSING
- INTERACTIVE DEBUGGING

★ SPECIALIZED PROGRAMMING LANGUAGES

- LISP
- PROLOG
- PLANNER

One area that AI people point with pride is their contribution to the development of tools and ideas. Time-sharing, list processing, and interactive debugging are all concepts originally conceived by groups of AI researchers. There has also been considerable work on specialized programming languages which more appropriately address the needs of the AI programmer, and which are beginning to gain acceptance outside the immediate AI community.

ARTIFICIAL INTELLIGENCE SYSTEMS TODAY

* INTERNIST/CADUCEUS - University of Pittsburgh
* PROSPECTOR - SRI International
* DIPMETER ADVISOR - Schlumberger
* DRILLING ADVISOR - Teknowledge/Elf-Aquitaine

Often we refer to AI as if it were something in the future. Actually it here today, and in daily use in a number of very practical applications. Some of the most noteworthy are indicated on this slide.

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INTERNIST/CADUCEUS

* 80% OF ALL INTERNAL MEDICINE
* 500 DISEASES
* 3500 MANIFESTATIONS OF DISEASES
* PREPARING TO UNDERGO FORMAL CLINICAL TRIALS

The Internist system was developed at the University of Pittsburgh as an expert system in the area of internal medicine. It already has incorporated 80% of the available knowledge about internal medicine. It knows about 500 diseases and 3500 manifestations of these diseases. It is preparing to undergo formal clinical trials. The future is now. This system routinely performs analyses as well as most internists, and better than doctors from other specialities.

OTHER EXPERT SYSTEMS

* PROSPECTOR - GEOLOGICAL EXPERT SYSTEM
* DIPMETER ADVISOR - OIL WELL LOG ANALYSIS
* DRILLING ADVISOR - DRILLING PROBLEM DIAGNOSIS

The Prospector system developed at SRI is an expert in geology and mineralogy. It has found mineral deposits valued in the hundreds of millions of dollars. In one case it found a deposit under a mining company waste site.

The Dipmeter advisor developed by Schlumerger does oil well log analysis. Schlumberger each year issues credits of about $40M due to errors made in well log analysis. The automation of this tedious process save Schlumberger several million dollars each year.

The Drilling Advisor, developed by Teknowledge for the French oil company, Elf A'quitine analyzes drilling problems and provides recommended courses of action. Considering that the operating cost of an oil rig typically costs over $100,000 per day, and the abandonment of an oil well due to problems typically costs several million dollars, it is easy to see why Elf A'quitine expects the system to return its full development cost on its first successful application.

The point here is that expert systems with impressive returns on investment are already in use. If you are wondering when you should begin to investigate this technology, the time is now.

A representative of Elf A'quitine once commented, '(get quote from 'Fifth Generation about gold nuggets)

PERQ/LINQ SYSTEM DESCRIPTION

(INSERT OVERVIEW OF PERQ/ACCENT MULTIPLE ENVIRONMENT SYSTEM AT THIS POINT)

CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

NATURAL LANGUAGE INTERFACES

* HELP SYSTEMS
* DATABASE QUERIES
* OPERATING SYSTEM INTERFACES

Now I would like to discuss some possible application areas for AI in CAD systems of various types.

CAD systems by their very nature are geometric, not textual. Users generally point at things as opposed to typing text. As a result, natural language interfaces are not as applicable to CAD systems as they are to some of the more traditional applications. They are extremely useful, however, in the implementation of help systems, and as a tool for doing queries on databases. They are also valuable when applied to the operating system interface, since many users of application programs are not generally familiar with the syntax of operating system commands. A natural language interface frees the user from having to remember whether the first or second file in an append command of the operating system is the appendee or appendor.

CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

SPECIFICATION WRITING

* EXPERT SYSTEM
* PRODUCTIVITY AID
* QUALITY IMPROVEMENT

The entire area of specification writing is the focus of some interest among CAD companies. Many users are as concerned about the specifications as they are about the ultimate implementations. The profitability in many industries, such as architecture and construction, are as determined as much by the specification, proposal and pricing as they are by the actual implementation.

This area lends itself well to the concept of expert systems. Specifications can be more thorough and consistent, and better advantage can be made of past experience by incorporating it into the knowledge base.

CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

INTEGRATED DATABASE MANAGEMENT

* APPLICATION ORIENTED

* CONSTRAINT MANAGEMENT

* APPLICATION BASED DATA LINKS

The control of a database in a CAD system is in many ways far more sophisticated than traditional databases. For one thing, the data tends to be interlinked in far more complicated ways. For example, an engineer changing one small part in a system may effect any number of other parts in obscure ways. It could affect the tensile strength of a bridge beam, or the systems performance on a particular FCC or UL test, or it could affect circuit loading so that other parts would have to be changed.

Databases in engineering applications have literally hundreds of constraints between various items in the database. These application-based data links all must be addressed each time any part in the system is changed. The complexity of this task is enormous, as many of us well know.

CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

CONTINGENCY MANAGEMENT

* CONSISTENCY CHECKING
* APPLICATION SPECIFIC
* AUTOMATIC RECONCILIATION

This entire area of contingency management is one of the most lucrative areas to which to apply AI techniques. For example, when the design of a pipe system in a building is completed, an AI program could check all the pipe and joint sizes and types to insure that they are consistent with each other and with the specification of the liquid or gas flow in the pipe. If inconsistencies were noted, they could be identified to the designer who could then request the program to automatically resolve the differences, adjusting pipe and joint sizes and strengths to be consistent with the overall specifications.

Timings in logic circuits could be handled in a similar manner.

CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

ON-LINE HANDBOOKS

* ENGINEERING HANDBOOK DATA
* APPLICATION RELATIVE
* CONTEXT ORIENTED
* EASE OF USE

One of AI's contribution to the word processing world was the spelling checker. In much the same vein the opportunity exists to bring the engineering handbooks on line to the designer in the same way that the dictionary was brought on-line to the writer. By making this reference material relative to the application and responsive to the content in which the designer is working will provide an easy to use aid that could speed up the design process for many of the more tedious checks which must be routinely made by designers.

CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

GOVERNMENTAL CODE CHECKING

* DESIGN VERIFICATION
* DESIGN RECOMMENDATIONS
* MULTIPLE REGULATIONS
* SAFETY CONSIDERATIONS

One of the more interesting and lucrative areas for the application of expert systems is in the area governmental codes and regulations. The incredible number of governmental regulations which apply to even the simplest piece of hardware staggers the imagination. In this era of multinational trade, virtually every engineer must daily deal with not only the federal, state, and city regulations, but also the regulations of England, Germany, Japan.... Add on to this, the whole subject of safety and product liability.... It is difficult to imagine that the present situation can continue without some expert assistance.

CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

CONSTRAINT LANGUAGES

* ENGINEERING AID

* EQUATION SOLVING

One of the more specialized areas of AI is the concept of constraint languages. Constraint languages allow a user to supply any of the variables to a set of equations and solve the missing variables. This relatively simple aid greatly simplifies the use of equations in many traditional engineering applications.

CAD APPLICATIONS OF ARTIFICIAL INTELLIGENCE

INTERACTIVE APPLICATION DEVELOPMENT

* OBJECT ORIENTED PROGRAMMING

* PROGRAMMING DEVELOPMENT ENVIRONMENTS

One of the major contributions of the AI community over the years has been their contributions to the idea of interactive programming. The development environments now in daily use by knowledge engineers provide an interactive development environment generally considered to be superior to any of the traditional development environments. In the past these techniques were considered too large and cumbersome to be of practical interest, but as the compute power per user has gone continually upward with the popularity of workstations, the Lisp development environment is receiving increasing attention and justifiably so.

CAD APPLICATION EXAMPLE

FORMDRAW DRAFTING SYSTEM

* EXPERT SYSTEM
* DESCRIPTIVE GEOMETRY
* ARCHITECTURE
* PROCESS AND INSTRUMENTATION DESIGN

An example of expert system techniques applied to the user interface of a computer aided design package is offered by the Formdraw package marketed by Formtek of Pittsburgh. Data entry is provided in the traditional manner by what appears on the surface to be a simple 2D-drafting system. In fact, the system is an expert system on descriptive geometry. That is to say that it understands the various principles of descriptive geometry. For example, it understands what an intersection is, and if you tell it to make two lines intersect, it will do so. If you tell it to make to parallel lines intersect it will advise you that parallel lines cannot intersect.

In addition, Formdraw can also be an expert system on architecture in their architecture system. So that it understands the concept of 'walls', and understands the unique qualities of the intersection of walls. It also understands that 'windows' go in walls. It also understands that walls do not intersect at windows, so if you asked the system to 'intersect' two walls, and the intersection occurred at a window, the system would advise you that walls do not normally intersect at a window. If you attempted to delete a wall, it would know that those things in the walls, such as windows, must also be deleted.

CAD - AI IN THE FUTURE

JAPANESE FIFTH GENERATION

* 1982 ----- 10 - 100M LIPS

* 1992 ----- 100 - 1000M LIPS

I could not give a talk on AI without mentioning the Japanese Fifth Generation. The Japanese have announced a plan, referred to as the 'Fifth Generation', to develop computer systems by 1992 capable of from 100 million to 1 billion LIPS (Logical Inferences Per Second). This represents an increase of 10,000 times. four orders of magnitude, from the present technology of less than 100K LIPS. Imagine, if you will, a system capable of 10,000 times the reasoning power of our present systems. This means that a problem which takes three hours to solve today could be done in one second in 1992 or a years worth of computing could be accomplished in one half a day.

The Japanese feel that if they could develop this technology ahead of the rest of the world, they could establish superiority, not only in this field, but in many other fields which have as their basis engineering solutions to problems. They believe that these KIPS (Knowledge Information Processings Systems) would provide them with superior design and manufacturing capability which would manifest itself in superior, lower cost, and higher quality products.

CAD - AI IN THE FUTURE

FUTURE CAD SCENARIO

* DESIGN BY SPECIFICATION
* PROGRESSIVE CLARIFICATION OF REQUIREMENTS
* USER DESIGN OF AESTHETICS
* MACHINE GENERATED IMPLEMENTATIONS
* AUTOMATIC CONSTRAINT RECONCILIATION
* EXTREMELY HIGH INTERACTIVITY

Consider if you will what design may be like with the availability of this incredible computing capability.

Design would be more of a process of refining a specification, then the working out of a detailed implementation. Instead of working on details, a designer would respond to a series of inquiries about the requirements of a design. For example, the designer of a hospital would answer questions as to the number of beds, climate, would there be a maternity ward, etc.

The user would specify factors of aesthetics, such as the number of floors --- which would be automatically laid out by the system. The system might respond and tell you that the maximum number of floors allowed by the adjacency requirements and the underlying ground conditions was four.

If the user specified a more efficient window design, the system would automatically adjust the size of the heating and air conditioning plant.

In circuit design, a similar process would take place. The CAE system would ask what kind of circuit you wanted to design... a controller perhaps; What kind of device? A disk. And on and on, until the controller was fully specified. Then the designer would decide, with the aid of the system, whether the controller should be a printed circuit board, a gate array, or a custom VLSI chip. The decision made, the system would implement the detailed design.

Is this far fetched? Well I broke my teeth on a '???'. It seems entirely realistic to me.

Nielsen Dataquest

COMMUNICATIONS INTEGRATION

Thomas H. Bredt
Vice President
Director, Telecommunications Industry Service
Dataquest Incorporated

Dr. Bredt is a Vice President of DATAQUEST and Director of the Telecommunications Industry Service. His major areas of responsibility include system-to-system communication, terminal-to-system connections, local area networks, public data networks, and protocol standards. Before joining DATAQUEST, Dr. Bredt was at Hewlett-Packard for eight years where he participated in the development of computer systems, manufacturing applications, and data communication products. His most recent position was Engineering Manager for HP's Information Networks Division, and manager of the company-wide Data Communications Strategy. Prior to his experience at HP, Dr. Bredt worked at Bell Laboratories and was a member of the Electrical Engineering faculty at Stanford University for seven years. Dr. Bredt's undergraduate degree is in Science Engineering from the University of Michigan. He has a Master's Degree in Electrical Engineering from New York University, and a Ph.D. in Computer Science from Stanford.

Dataquest Incorporated
WORKSTATION FOCUS CONFERENCE
August 13 and 14, 1984
Burlington, Massachusetts

COMMUNICATIONS INTEGRATION

THOMAS H. BREDT
VICE PRESIDENT
DIRECTOR, TELECOMMUNICATIONS INDUSTRY SERVICE

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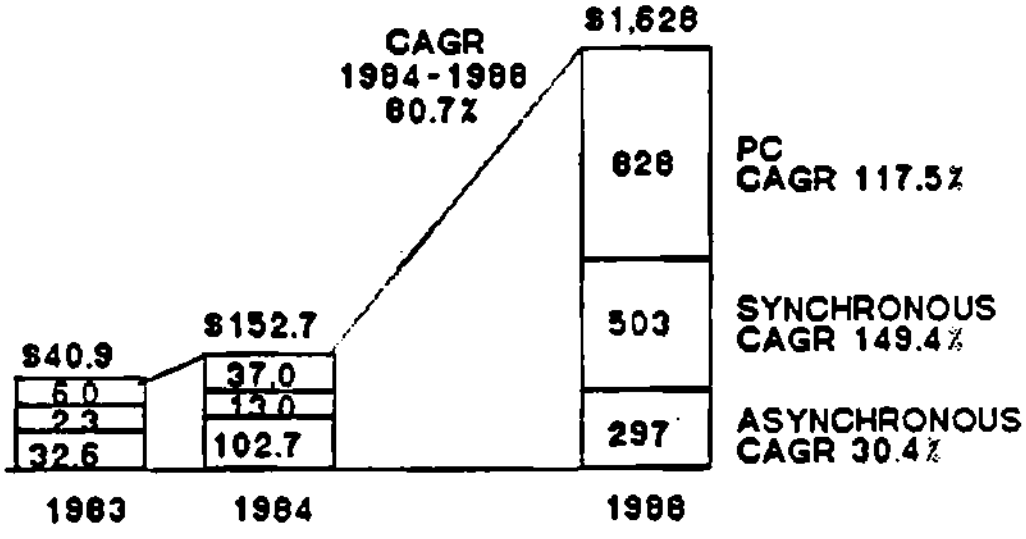
ESTIMATED U.S. REVENUE FOR VOICE/DATA WORKSTATIONS (IF-SOLD, END-USER)

(MILLIONS OF DOLLARS)



SOURCE DATAQUEST

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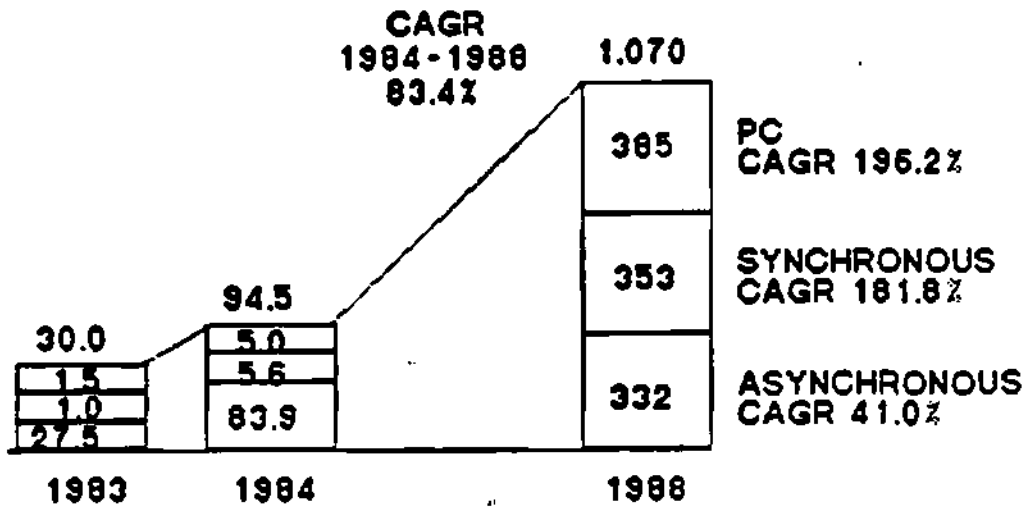
ESTIMATED U.S. SHIPMENTS OF VOICE/DATA WORKSTATIONS

(THOUSANDS OF UNITS)



SOURCE DATAQUEST

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VOICE/DATA WORKSTATION

1988 AVERAGE SELLING PRICE

ASYNCHRONOUS	$ 695
SYNCHRONOUS	$1,425
PERSONAL COMPUTER	$2,150

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VOICE/DATA WORKSTATION MARKET TRENDS

- EARLY TERMINAL PRODUCTS WILL LEAD TO PRODUCT FAMILIES
- PERSONAL COMPUTER WILL HAVE 36 PERCENT OF UNIT SHIPMENTS BY 1988
- INTEGRATED TELEPHONES WITH SOFTWARE SUPPORT FOR CALENDAR AND TIME MANAGEMENT WILL BE OPTION FOR EVERY TERMINAL AND PERSONAL COMPUTER PRODUCT BY 1988
- NEW MARKET ENTRANTS AND TERMINAL VENDORS WILL COMPETE FOR POSITION AS INDEPENDENT SUPPLIERS OF VOICE/DATA WORKSTATIONS
- SHAKEOUT WILL OCCUR AS VENDORS SEEK CORRECT BLEND OF PRODUCT DESIGN, PRICE, AND DISTRIBUTION STRATEGIES
- PROPRIETARY DESIGNS FROM PBX MANUFACTURERS WILL COMPETE WITH NONPROPRIETARY DESIGNS FROM WORKSTATION AND COMPUTER MANUFACTURERS

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ESTIMATED U.S. SHIPMENTS OF VOICE/DATA WORKSTATIONS

(THOUSANDS OF UNITS)

RANK	COMPANY	1983	MARKET SHARE
1	NORTHERN TELECOM	15.0	50.0%
2	TYMSHARE	9.9	33.0%
3	GTE	2.4	8.0%
4	MITEL	1.5	5.0%
5	DAVOX	1.0	3.3%
	OTHERS	.2	.7%
	TOTAL	30.0	100.0%

SOURCE DATAQUEST

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ESTIMATED U.S. REVENUE FOR VOICE/DATA WORKSTATIONS (IF-SOLD, END-USER)

RANK	COMPANY	1983 ($M)	MARKET SHARE
1	NORTHERN TELECOM	$19.5	47.7%
2	TYMSHARE	8.9	21.8%
3	MITEL	6.0	14.7%
4	GTE	3.6	8.8%
5	DAVOX	2.3	5.6%
	OTHERS	.6	1.4%
	TOTAL	$40.9	100.0%

SOURCE DATAQUEST

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CABLE-BASED LOCAL AREA NETWORKS

APPLICATION AREAS	VENDORS
COMPUTER TO COMPUTER	NETWORK SYSTEMS
TERMINAL TO COMPUTER	BRIDGE COMMUNICATIONS, INTERLAN, SYTEK, UNGERMANN-BASS
PERSONAL COMPUTER RESOURCE SHARING	3COM, CORVUS, NESTAR
OFFICE WORKSTATION NETWORKS	DATAPOINT, WANG, XEROX
FACTORY NETWORKS	CONCORD DATA SYSTEMS
SPECIAL NETWORKS (E.G., CAD)	APOLLO

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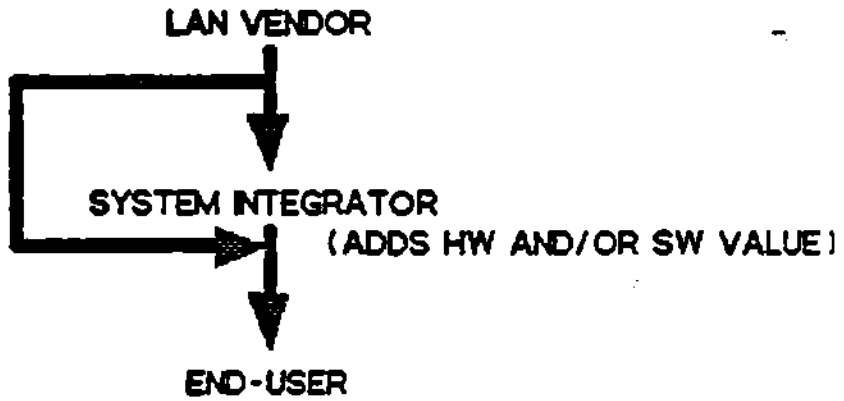
MARKETING CHANNELS FOR LOCAL AREA NETWORKS



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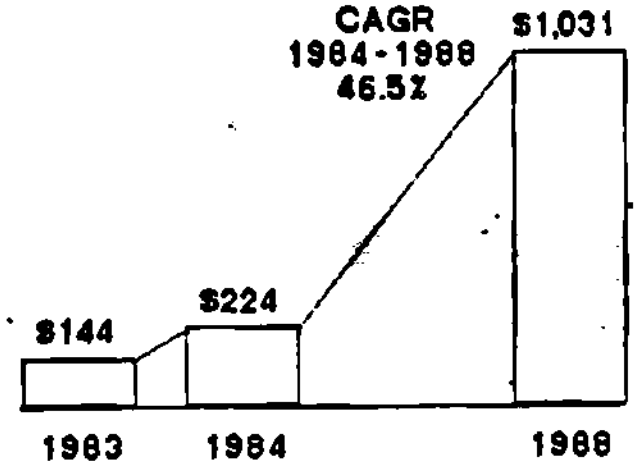
ESTIMATED U.S. MARKET FOR LOCAL AREA NETWORKS

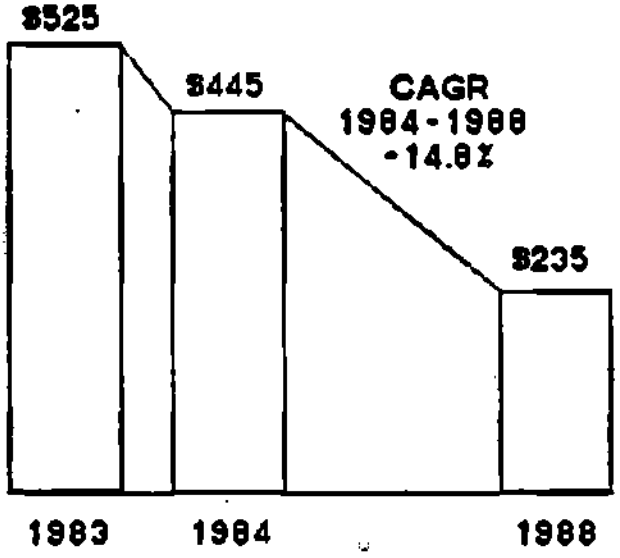
(MILLIONS OF DOLLARS)



SOURCE DATAQUEST

ESTIMATED LOCAL AREA NETWORK AVERAGE RS-232-C CONNECTION COST

(HARDWARE EQUIPMENT ONLY, U.S. DOLLARS)



SOURCE DATAQUEST

LOCAL AREA NETWORK MARKET TRENDS

- STEADY PROGRESS ON STANDARDS FEEDING STRONG GROWTH
- IEEE 802.3 AND IEEE 802.5 WILL BE DOMINANT OFFICE NETWORK STANDARDS
- BROADBAND NETWORKS WILL BE USED IN FACTORIES AND AS BACKBONE INFORMATION HIGHWAYS IN LARGE BUILDINGS
- PERSONAL COMPUTER MANUFACTURERS MOVING QUICKLY TO INTEGRATE RESOURCE SHARING NETWORKS INTO PRODUCT LINES
- VLSI CHIP DELAYS SLOW REALIZATION OF MARKET POTENTIAL
- DATA BANDWIDTH FOR COMPUTER-COMPUTER FILE TRANSFER, IMAGE PROCESSING, AND GROUP IV FACSIMILE WILL PROVIDE WINDOW OF OPPORTUNITY
- MAKE-VERSUS-BUY IS A BOARDROOM DECISION FOR OEMS, SYSTEM INTEGRATORS, AND COMPUTER MANUFACTURERS

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ESTIMATED U.S. REVENUE FOR LOCAL AREA NETWORKS

(HARDWARE EQUIPMENT ONLY)

RANK	COMPANY	1983 ($M)	MARKET SHARE
1	NETWORK SYSTEMS	$37.0	25.7%
2	UNGERMANN-BASS	17.5	12.2%
3	SYTEK	16.9	11.7%
4	DATAPOINT	15.1	10.5%
5	3COM	9.3	6.5%
6	CORVUS	8.9	6.2%
7	INTERLAN	6.7	4.7%
	OTHERS	32.6	22.5%
	TOTAL	$144.0	100.0%

SOURCE: DATAQUEST

DATA PBX DEFINITIONS

- A DIGITAL PBX THAT ALLOWS TERMINALS TO SWITCH AND CONTEND FOR COMPUTER RESOURCES
- SWITCHING ENABLES TERMINAL USER TO ACCESS DIFFERENT APPLICATIONS PROGRAMS ON DIFFERENT COMPUTERS
- CONTENTION ALLOWS MORE TERMINALS TO ATTEMPT TO ACCESS FEWER COMPUTER PORTS
- DATA SWITCHING/CONTENTION ONLY; NO VOICE SWITCHING AS WITH VOICE/DATA PBX

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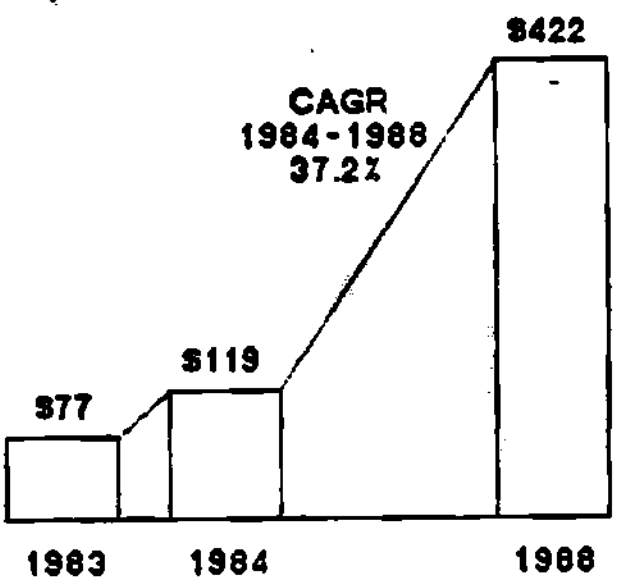
ESTIMATED U.S. REVENUE FOR DATA PBX MARKET (IF-SOLD, END-USER)

(MILLIONS OF DOLLARS)



SOURCE DATAQUEST

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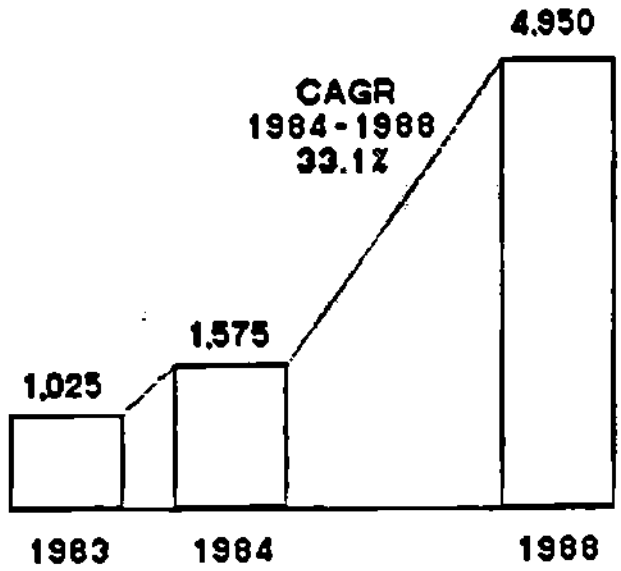
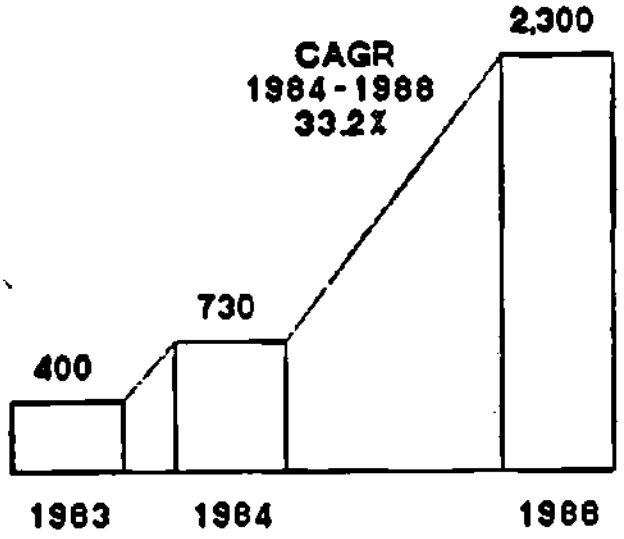
ESTIMATED U.S. SYSTEM SHIPMENTS FOR DATA PBX MARKET



SOURCE DATAQUEST

ESTIMATED U.S. LINE SHIPMENTS FOR DATA PBX MARKET

(THOUSANDS OF LINES)



SOURCE DATAQUEST

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DATA PBX TRENDS

- DISTRIBUTED ARCHITECTURES TO INSTALL NODES WHERE TERMINALS ARE LOCATED
- T1 (1.544 MBPS) LINKS BETWEEN NODES FOR HIGH-SPEED TRANSMISSION
- USE OF VOICE/DATA MULTIPLEXERS FOR SIMULTANEOUS VOICE AND DATA TRANSMISSION OVER EXISTING IN-PLANT TELEPHONE WIRING
- PRICE-COMPETITIVE ALTERNATIVE FOR LOCAL AREA NETWORKING
- MARKET GROWTH OVER THE PERIOD RESULTING FROM INCREASING MINICOMPUTER AND ASYNCHRONOUS TERMINAL POPULATIONS

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ESTIMATED U.S. REVENUE FOR THE DATA PBX MARKET (IF-SOLD, END-USER)

RANK	COMPANY	1983 ($M)	MARKET SHARE
1	MICOM	$33.0	42.9%
2	DEVELCON	15.0	19.5%
3	GANDALF	14.0	18.2%
4	INFOTRON	6.6	8.6%
5	CODEX (MOTOROLA)	4.0	5.2%
6	M/A COM LINKABIT	3.0	3.9%
	ALL OTHERS	1.4	1.7%
	TOTAL	$77.0	100.0%

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VOICE/DATA PBX MARKET

ESSENTIALLY NONBLOCKING:

- 100 PERCENT OF AVAILABLE DATA PORTS AT 19.2 KBPS ASYNCHRONOUS
- 100 PERCENT OF AVAILABLE DATA PORTS AT 56 KBPS SYNCHRONOUS
- 10 CCS VOICE TRAFFIC TO EACH VOICE STATION
- 30 CCS VOICE TRAFFIC FOR EACH ANALOG TRUNK

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PRIVATE BRANCH EXCHANGES

- VIRTUALLY ALL OF THE PBX SYSTEMS INTRODUCED IN THE LAST 18 MONTHS ARE ESSENTIALLY NONBLOCKING
- DATAQUEST PREDICTS THAT BY 1988, 85 PERCENT OF ALL PBX SYSTEMS SOLD IN THE UNITED STATES WILL BE DIGITAL, INTEGRATED VOICE AND DATA SYSTEMS OF ESSENTIALLY NONBLOCKING ARCHITECTURE (BASED ON DOLLAR VOLUME)

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A NEW PBX MARKET SEGMENT

THE ULTRALOW-COST PBX

- ANALOG VOICE ONLY
- FIXED SIZE--NOT EXPANDABLE ABOVE 40 LINES
- SUPPORTS 2500-TYPE TELEPHONE SETS ONLY
- SIMPLE FEATURES--NO BELLS AND WHISTLES
- IF-SOLD, END-USER VALUE OF $210 PER LINE (1984)
  CAGR: 1984-1988 = 131.8%
  1984: $5M
  1988: $145M

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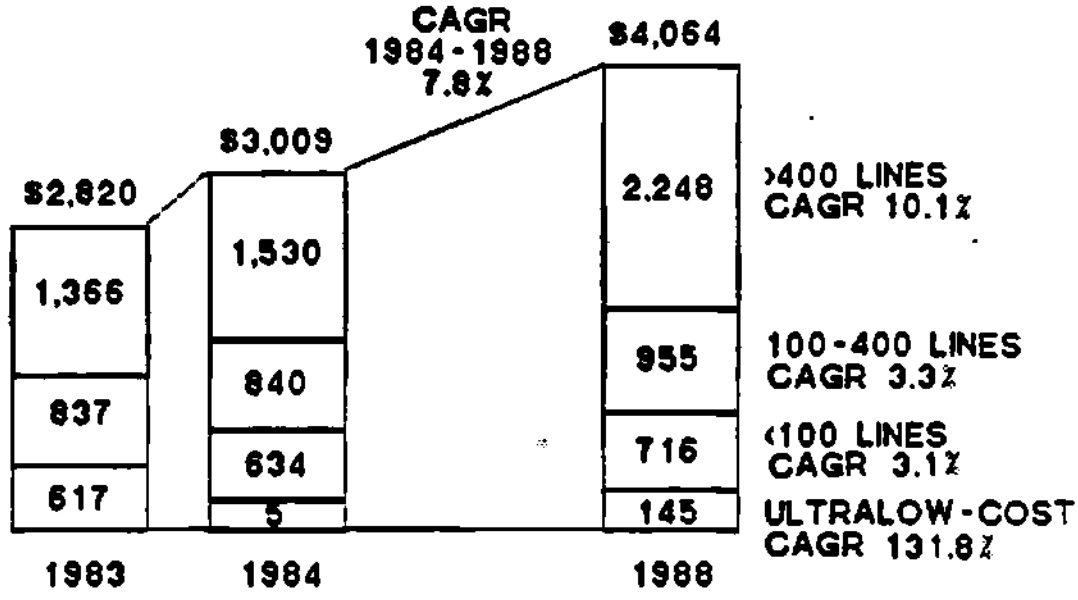
ESTIMATED U.S. REVENUE FOR THE PBX MARKET (IF-SOLD, END-USER)

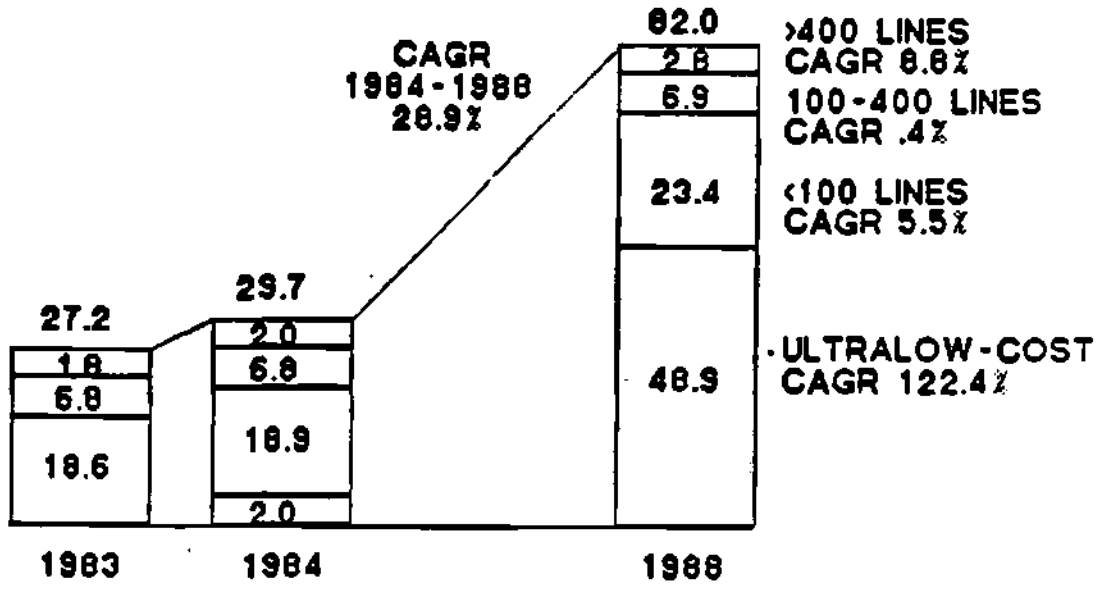
(MILLIONS OF DOLLARS)



SOURCE DATAQUEST

ESTIMATED U.S. SYSTEM SHIPMENTS FOR THE PBX MARKET

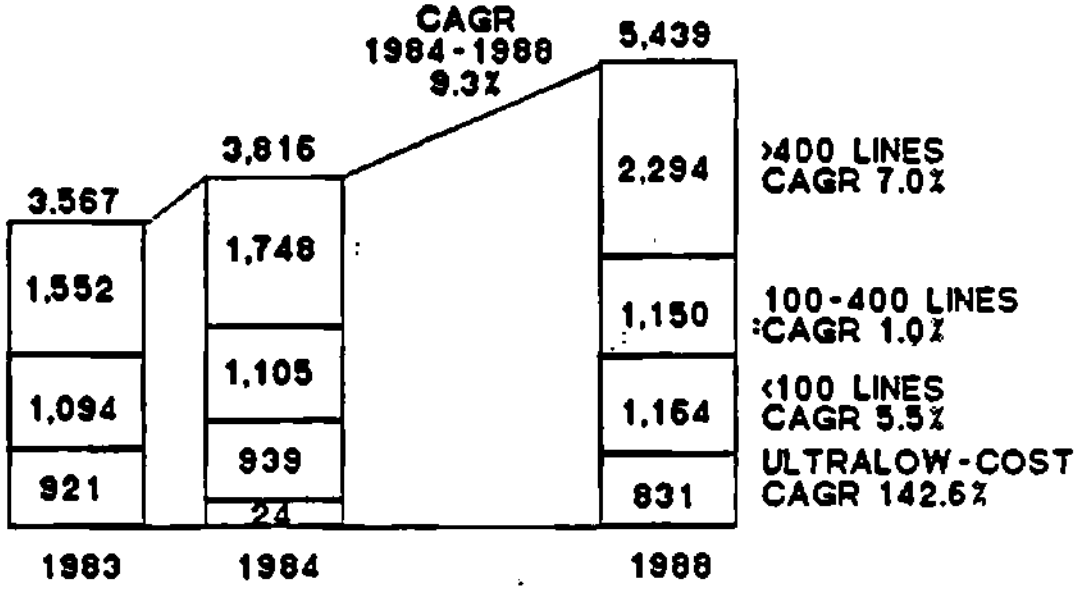
(THOUSANDS OF SYSTEMS)



SOURCE DATAQUEST

ESTIMATED U.S. LINE SHIPMENTS FOR THE PBX MARKET

(THOUSANDS OF LINES)



SOURCE DATAQUEST

ESTIMATED U.S. PBX PRICE PER LINE (IF-SOLD, END-USER)

(DOLLARS PER LINE)

SEGMENT	1983	1984	1988	CAGR 1984-1988
> 400 LINES	$880	$875	$980	2.9%
100-400 LINES	$765	$760	$830	2.2%
<100 LINES	$670	$675	$615	-2.3%
ULTRALOW-COST	N/A	$210	$175	-4.5%
TOTAL MARKET	$791	$788	$747	-1.3%

SOURCE DATAQUEST

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PBX INDUSTRY TRENDS

- INTENSE PRICE COMPETITION TO GAIN/KEEP MARKET SHARE
- AT&T DIVESTITURE WILL AMPLIFY NEED TO FOCUS ON DISTRIBUTION
- ABILITY TO MANAGE SOFTWARE DEVELOPMENT WILL BE KEY TO FUTURE SUCCESS
- DATA TERMINAL CONNECTIONS WILL BECOME MORE COST-EFFECTIVE WITH AVAILABILITY OF COMPUTER-PBX INTERFACES
- PBX MANUFACTURERS WILL EMPHASIZE INTEGRATED DESKTOP WORKSTATIONS TO MOVE INTO OFFICE AUTOMATION MARKET
- COMPUTER-COMPUTER COMMUNICATION AND IMAGE PROCESSING WILL LEAD TO NEW PBX ARCHITECTURES THAT MOVE INFORMATION IN PACKET FORM

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PRIVATE BRANCH EXCHANGES

- TO EXPLOIT DIGITAL SWITCHING, EACH PBX MANUFACTURER HAS INTRODUCED A DESKTOP RS-232 SERIAL DATA COMMUNICATIONS ADAPTOR
  - — NORTHERN TELECOM ADD-ON DATA MODULE
  - — ROLM DATA TERMINAL INTERFACE
  - — INTECOM DATA OPTION BOARD

- VARIOUS MODELS OF THESE ADAPTORS CONNECT TO ASYNCHRONOUS DEVICES AT SPEEDS UP TO 19,200 BITS PER SECOND AND SYNCHRONOUS DEVICES AT SPEEDS UP TO 64,000 BITS PER SECOND

- PRICES ARE TYPICALLY $300 FOR ASYNCHRONOUS ADAPTORS AND $800 FOR SYNCHRONOUS ADAPTORS

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PRIVATE BRANCH EXCHANGES

- PBX VENDORS NOW VIEW THEIR NEXT OPPORTUNITY IS TO CAPTURE THE DESKTOP OF THE OFFICE WORKER
  - TELEPHONE
  - SPEAKERPHONE
  - NAME/ADDRESS/TELEPHONE NUMBER FILE
  - PERSONAL CALENDAR
  - REMINDER SLIPS
  - CLOCK
  - DISPLAY TERMINAL

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PRIVATE BRANCH EXCHANGES

- SOME PBX MANUFACTURERS WILL DEVELOP THEIR OWN DISPLAY TELEPHONE TERMINALS
  - — ROLM CYPRESS
  - — NORTHERN TELECOM DISPLAYPHONE
- SOME PBX MANUFACTURERS WILL SELECT AN OEM PRODUCT
  - — ZAISAN ES.1

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PRIVATE BRANCH EXCHANGES

- THE NEXT FRONTIER IS EFFICIENT CONNECTION OF MULTIPLE TERMINALS VIA THE PBX TO A HOST COMPUTER
- TODAY, EACH PORT ON A HOST DATA PROCESSING OR OFFICE AUTOMATION COMPUTER MUST HAVE A CORRESPONDING LINE AND ADAPTOR ON THE PBX
- GATEWAYS TO IBM HOSTS HAVE BEEN INTRODUCED BY ROLM AND NORTHERN TELECOM

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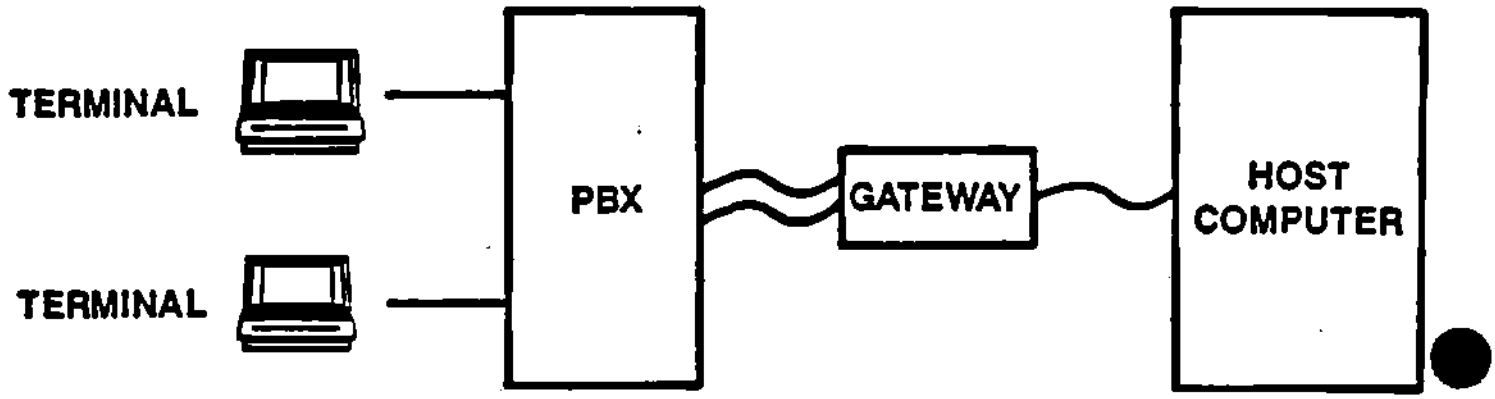
PRIVATE BRANCH EXCHANGES



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PRIVATE BRANCH EXCHANGES

- TWO METHODS OF CONNECTING MULTIPLE TERMINALS TO HOSTS VIA PBXs HAVE BEEN PROPOSED

- COMPUTER-PBX-INTERFACE (CPI)
  - 1.544 MILLION BITS PER SECOND
  - 24 FULL DUPLEX CONNECTIONS
  - EACH CONNECTION 0-56,000 BPS
  - CONTROL IS EMBEDDED IN EACH CONNECTION
  - PROMOTED BY DIGITAL EQUIPMENT CORPORATION AND BY NORTHERN TELECOM

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PRIVATE BRANCH EXCHANGES

- DIGITAL MULTIPLEX INTERFACE (DMI)
  - ANNOUNCED NOVEMBER 2nd
  - 1.544 MILLION BITS PER SECOND
  - UP TO 155 FULL DUPLEX CONNECTIONS
  - EACH CONNECTION USES ONLY BANDWIDTH REQUIRED
  - CONTROL IS ALLOCATED TO ONE 64,000 BIT PER SECOND CONNECTION
  - PROMOTED BY AT&T, HEWLETT-PACKARD, AND BY WANG

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THE BATTLE FOR THE WIRING CLOSET

	1983 DATA LINES SHIPPED (THOUSANDS)
DATA PBX	400.000
LOCAL AREA NETWORK	72.500
VOICE/DATA PBX	35.700
TOTAL	508.200

Source: DATAQUEST

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THE VITAL LINK IS COMMUNICATIONS

- INTEGRATED VOICE AND DATA WORKSTATIONS
- CABLE BASED LOCAL AREA NETWORKS
- DATA PBXs
- VOICE AND DATA PBXs

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Nielsen Dataquest

NETWORK CONFIGURATIONS

Peter J. Shaw
President and Chief Executive Officer
Syte Information Technology

Mr. Shaw is founder, president, and CEO of Syte Information Technology. Mr. Shaw has held engineering, marketing, and sales positions with several other companies, including Perkin-Elmer, and was named president of Megatek Corporation in 1981. Mr. Shaw is a director of two San Diego based companies, Telesoft Corporation and Systech Corporation, and a former director of Data Systems Corporation. He is founding director and a member of the National Computer Graphics Association, and served as chairman of the Vendor Advisory Committee for the SIGGRAPH special interest group of the Association for Computing Machinery. Mr. Shaw received his bachelor's degree in engineering from the City College of New York and his M.B.A. degree from the University of Connecticut.

Dataquest Incorporated
WORKSTATION FOCUS CONFERENCE
August 13 and 14, 1984
Burlington, Massachusetts

DATAQUEST CONFERENCE

AUGUST 13-14, 1984

"WORKSTATIONS"

THE EVOLUTION OF AN INDUSTRY

NETWORK CONFIGURATIONS

PETER J. SHAW, PRESIDENT

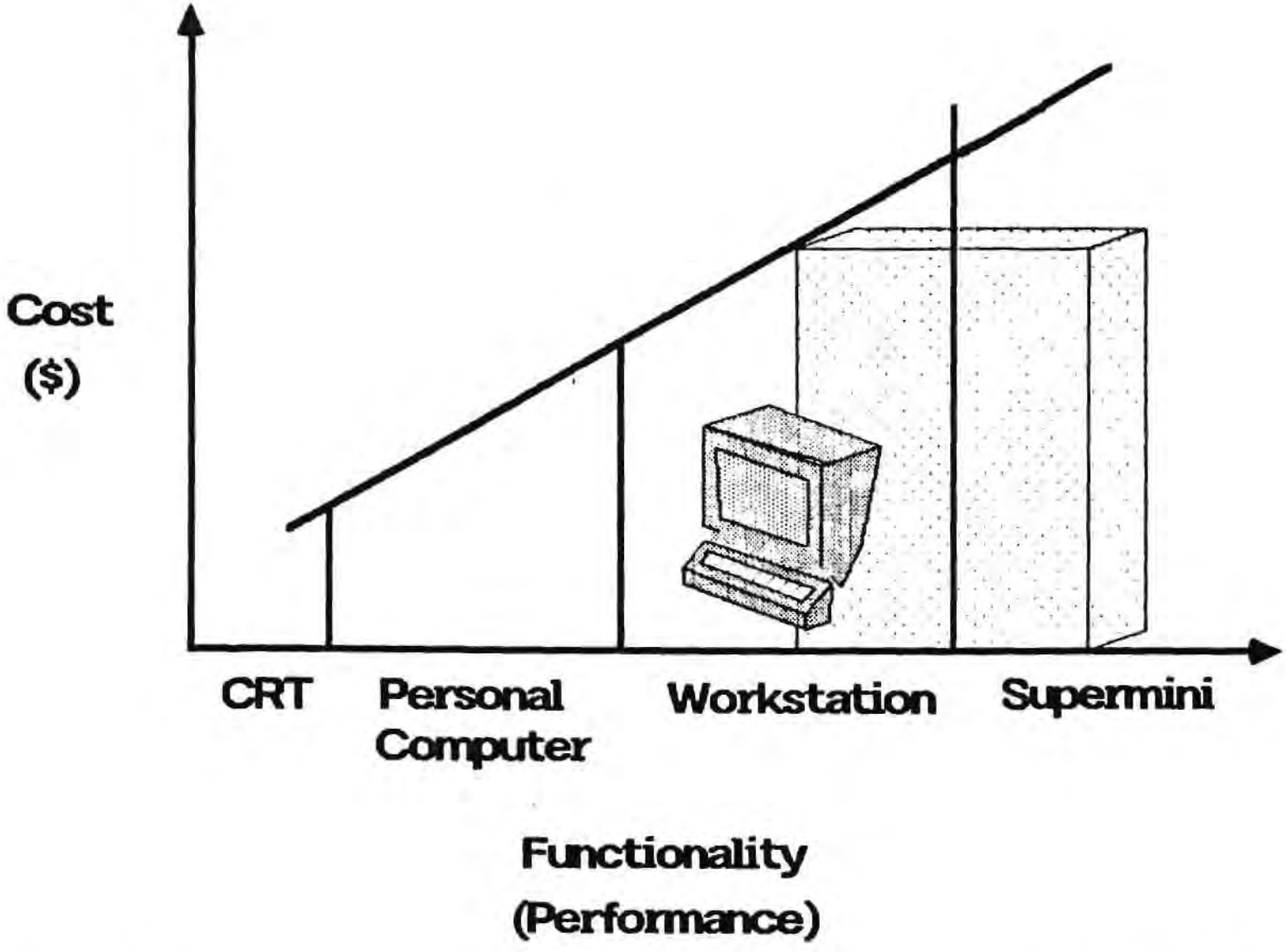
SYTE INFORMATION TECHNOLOGY INCORPORATED

SAN DIEGO, CALIFORNIA

CONFIGURING A NETWORK

Consider

- Computational Power
- Utility - Application
- Cost
- Flexibility
- Expansion



Workstation: A Definition

- Single User
- Single Processor
- Single Function
- 1 - 4 Megabytes, RAM
- Mid and High Resolution Graphics
- 50 Megabyte Disk Space/User

ENGINEERING/SCIENTIFIC NETWORK

A Definition:

- A COMBINATION Of Computing Peripheral, And Communications Elements
- Working Together
- To Serve Multiple Application Requirements

NETWORK FUNCTIONALITY

Flexible, Expandable:

- **Multiple Levels of Computing**
- **Multiple Operating System Support**
- **Wide Range Of Multi-Vendor Peripherals**
- **A Standard, Accessible Network Medium**
- **Communication Between Networks**

CONFIGURATION ALTERNATIVES

A SINGLE SOLUTION

SATISFIES NO ONE

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A Series of Single User Workstations May Not Be Enough

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WORKSTATION

Benefits:

- Predictable Response
- High Degree of Interaction
  - Good User/Machine Interface
- Psychology of Ownership

SUPERMINICOMPUTER

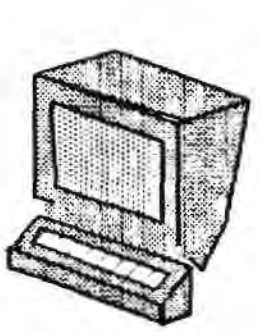
When:

- A Very Large Job
  - The Job Is Too Big

- A Very Small Job
  - The Jobs Are Too Small

NETWORKED SUPERMINI:

A Modern Architecture



Special Purpose
Computing Accelerators

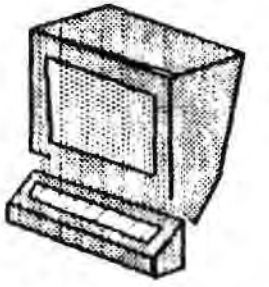
Alphanumeric
Terminal Support

Supermini
Baseline

1 MIP, 1 Megabyte RAM

Expandable In
Multiples Of Baseline

Graphics
Terminal
Support



Tightly Coupled,
Bit-Mapped Graphics.
Mid And High Resolution,
Monochrome And Color.

Peripherals

Mass Storage
100 Megabytes Disk,
Minimum Tape

Network On/Or
Global Communications

Legend
Tightly Coupled
Communication Line

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NETWORKS

Elements Of A Network:

- Workstations
- Multi-User, Powerful, Computers
  - With Graphics
  - Without Graphics
  - Variable Performance
- Special Purpose Accelerators
- Clusters
- Mass Storage and Peripherals
- Communications

CONCEPT:

Networked Computers

vs.

A Computer Across The Network

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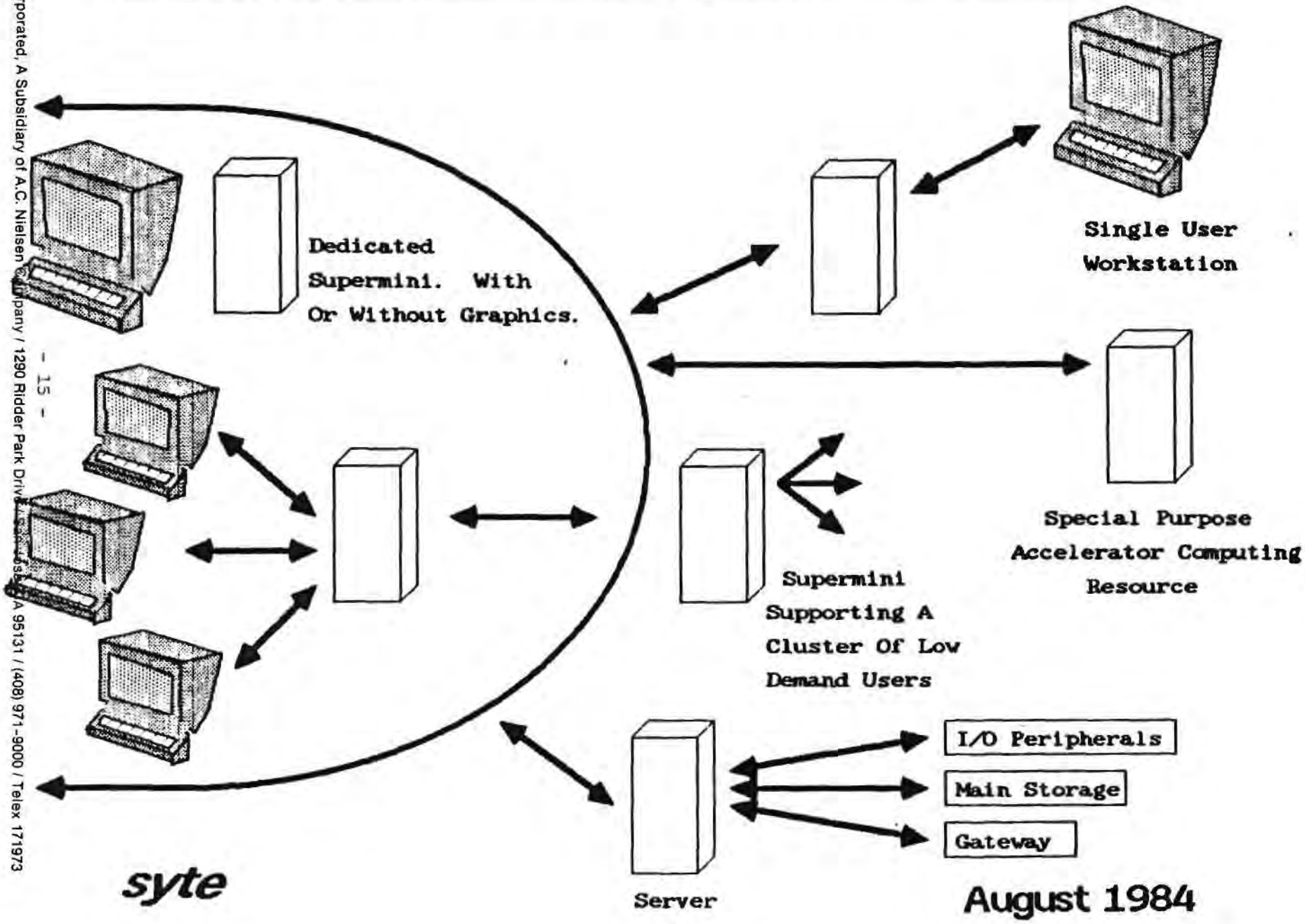
ELEMENTS OF AN ADVANCED NETWORK

1984 - 1985

- Software Dependent
- Resource Sharing
- 10 - 15 MBits/Sec
- Workstation and Supermini

NETWORKED CONFIGURATION



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A NETWORK CONFIGURATION, OR WHAT TYPE OF EQUIPMENT IS CONNECTED TO A NETWORK, WILL VARY AS WIDELY AS THE APPLICATIONS ATTEMPTED AND THE BUDGET CONSTRAINS. TO TRY TO DEFINE THE OPTIMUM NETWORK WITHOUT UNDERSTANDING THE PARTICULAR ENVIRONMENT (PHYSICAL, TECHNICAL, SOCIAL OR PSYCHOLOGICAL, AND FINANCIAL) IS AN EXERCISE DOOMED TO FAILURE. THE NETWORK MUST REFLECT THE INDIVIDUAL GOALS AND CONSTRAINTS OF THE ORGANIZATION IT ATTEMPTS TO SERVE. AND AS THAT ORGANIZATION AND ITS NEEDS CHANGE, SO MUST THE NETWORK.

BUT, RATHER THAN DEFINE THE NETWORK NOW, LET'S FIRST TALK ABOUT SOMETHING MUCH MORE BASIC, SOMETHING I'D LIKE TO CALL AN "ELEMENT"; AND, SINCE WE ARE NOW TALKING ABOUT COMPUTERS, LET'S CREATE A "COMPUTING ELEMENT".

PEOPLE BUY COMPUTERS AND SOFTWARE AND GRAPHICS AND, YES, NETWORKS TOO, FOR ONE SIMPLE REASON: THEY HAVE A PROBLEM TO SOLVE OR INFORMATION TO OBTAIN OR A PRODUCT THEY WOULD LIKE TO CREATE. THEY HAVE A COMPUTING APPLICATION.

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IN ORDER TO REACH A SOLUTION CORRECTLY AND EFFICIENTLY, ALL APPLICATIONS REQUIRE AT LEAST ONE STRONG COMPUTING ELEMENT. AND BY COMBINING THIS COMPUTING ELEMENT WITH OTHER ELEMENTS, BE THEY COMPUTING, OR GRAPHICS, OR SOFTWARE, OR NETWORK, WE CAN CREATE THE "ENVIRONMENT" IN WHICH THE USER CAN SATISFY HIS REQUIREMENTS. I THINK THAT THIS IS WHERE MANY SYSTEM DESIGNERS TAKE THE WRONG TURN. THEY LOOK AT THE FOREST, BUT SOMEHOW MISS THE TREES. THE ROOTS ARE NEGLECTED, THE TRUNK IS NOT SECURE, BUT QUICKLY THEY ADD THE BRANCHES, CONCENTRATING FIRST NOT ON THE COMPUTING ELEMENT, BUT RATHER ON GRAPHICS RESOLUTION AND NUMBER OF COLORS; NETWORK MEDIUM INSTEAD OF FUNCTIONALITY AND EXPANDABILITY; THE GENERIC NAME OF THE DEVICE (WORKSTATION, FOR EXAMPLE) RATHER THAN WHAT IS REQUIRED OF THE DEVICE; AND ISOLATED SPECIFICATIONS RATHER THAN SYSTEM THROUGHPUT.

IT ALL STARTS WITH THE BASICS, THE COMPUTING ELEMENT. DEVELOP OR ACQUIRE A POWERFUL, FLEXIBLE, EXPANDABLE COMPUTING ELEMENT CAPABLE OF COMMUNICATION WITH THE USER AND/OR THE NETWORK OR THE GLOBAL ENVIRONMENT AND USE IT AS THE BASIC ELEMENT OF THE NETWORK. BUILD THE FOUNDATION, GROW THE ROOTS. IT MATTERS NOT WHAT STYLE THE HOUSE IS OR WHAT NAME THE TREE GOES BY, BECAUSE WITHOUT THE UNDERLYING STRUCTURE, THE HOUSE WILL FALL, THE TREE WILL NOT GROW, AND THE NETWORK WILL NOT BE EFFECTIVE.

ONCE THE COMPUTING ELEMENTS HAVE BEEN DEFINED, THEY MUST BE COMBINED WITH ADDITIONAL HARDWARE AND SOFTWARE TO CREATE A NETWORK, DIFFERENT ELEMENTS WORKING AND COMMUNICATING TOGETHER TO SOLVE COMPUTING APPLICATIONS.

NOW, HAVING LAID THE GROUNDWORK, I WILL CONCENTRATE ON DEFINING AND TYING DIFFERENT ELEMENTS OF A NETWORK TOGETHER, AND, FOR THE PURPOSE OF THIS SESSION, CONCENTRATE ON ELEMENTS IMPORTANT IN ENGINEERING AND SCIENTIFIC COMPUTING APPLICATIONS.

THE VARIOUS ELEMENTS OF A NETWORK NEED TO BE AS DIVERSE AS THE TYPES OF APPLICATIONS RUN BY USERS ON THE NETWORK. IF WE WERE TO EXAMINE A TYPICAL ENGINEERING OR R & D DEPARTMENT OF A TYPICAL CORPORATION, WE WOULD SEE THE DEMAND FOR A WIDE RANGE OF DEVICES ON A NETWORK.

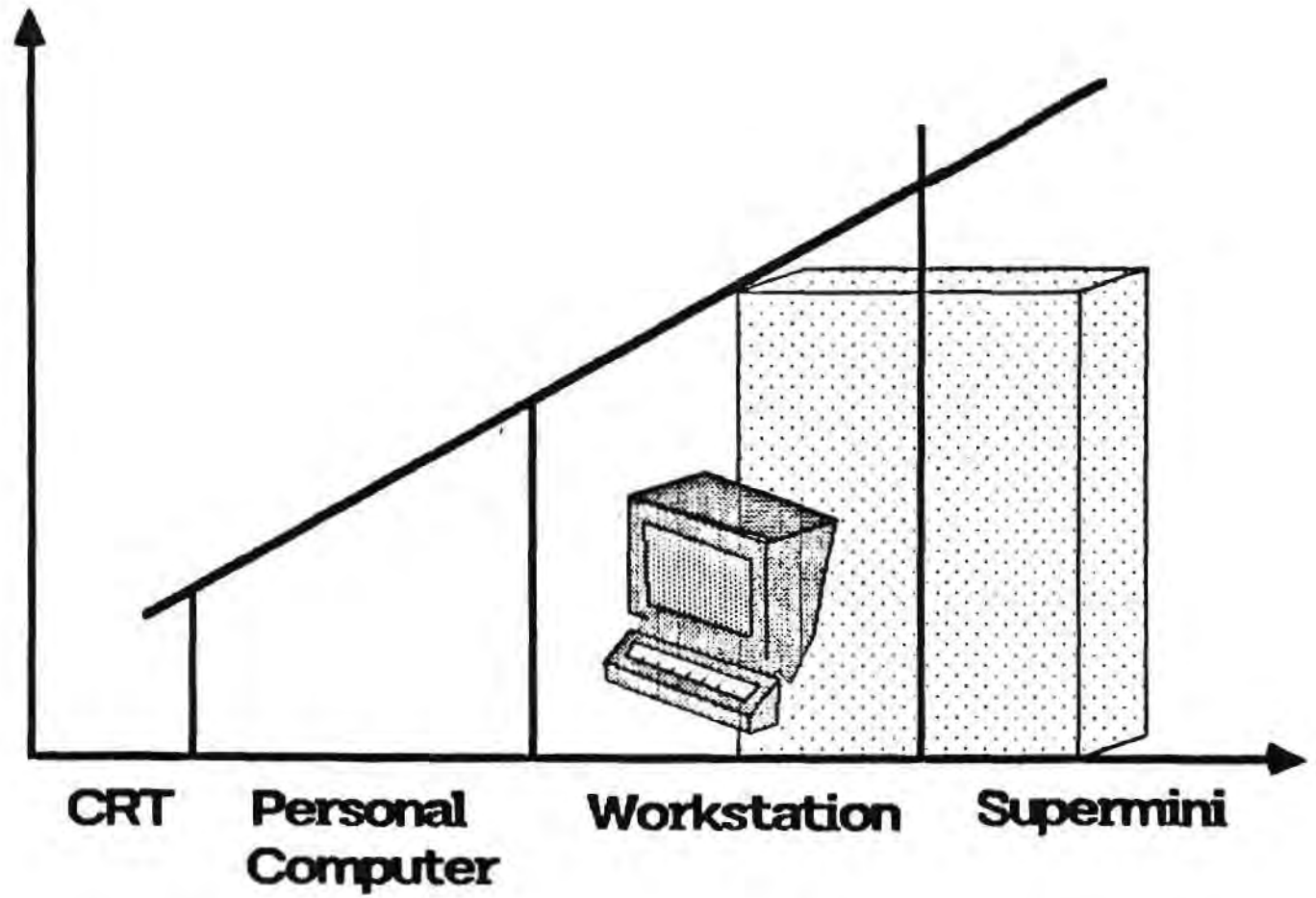
COMPUTING RESOURCES ON A NETWORK CAN RANGE FROM A SIMPLE VDT CONNECTED VIA LOW SPEED RS 232 COMMUNICATIONS TO A TIME-SHARING MICRO TO A SUPER-MINI DEDICATED TO A SINGLE USER. GRAPHICS MAY OR MAY NOT BE REQUIRED. AND EVEN WHEN GRAPHICS IS NEEDED, THE NUMBER OF COLORS, RESOLUTION, AND FUNCTIONABILITY MAY VARY SIGNIFICANTLY.

IN CONFIGURING A NETWORK THAT WILL MEET THE NEEDS OF A PARTICULAR ORGANIZATION, A CAREFUL STUDY MUST BE COMPLETED TO DETERMINE THE TYPE OF WORK TO BE DONE, THE DIFFERENT AVAILABLE HARDWARE AND SOFTWARE TO DO THE WORK, AND THE AMOUNT OF MONEY AVAILABLE TO IMPLEMENT THE SYSTEM.

IN DESIGNING A NETWORK, CARE MUST BE TAKEN SO THAT FUTURE NEEDS CAN EASILY BE ACCOMMODATED. THIS MEANS NOT ONLY ADDITIONAL LIKE DEVICES, BUT ALSO NEW COMPUTATIONAL ELEMENTS THAT WILL TAKE ADVANTAGE OF NEW TECHNOLOGIES AND NEW APPLICATIONS, AND WHICH WILL MEET THE FINANCIAL ABILITIES OF THE USERS IN THE ORGANIZATION.

A NETWORK MUST BE FUNCTIONAL, FLEXIBLE, AND ECOMONICAL.

A TYPICAL GRAPH OF THE TYPE OF MACHINES THAT MAY BE REQUIRED BY NETWORK USERS MIGHT LOOK LIKE THIS:



FOR TODAY'S PURPOSES, LET US CONCENTRATE ON WORKSTATIONS AND SUPERMINIS AND THEIR ROLE ON A NETWORK.

FIRST, LET'S DEFINE WHAT WE MEAN BY WORKSTATION AND, FURTHERMORE, LET'S TAILOR OUR DEFINITION TO ENGINEERING AND SCIENTIFIC ENVIRONMENTS. THE WORD WORKSTATION TAKES ON A WHOLE NEW DEFINITION IN THE OFFICE ENVIRONMENT. THE DEFINITION I WOULD LIKE TO USE IS:

ENGINEERING/SCIENTIFIC WORKSTATION

DEFINITION:

- SINGLE-USER
- SINGLE CENTRAL PROCESSOR
- SINGLE FUNCTION
- 1 - 4 MEGABYTE MEMORY, MINIMUM
- MID OR HIGH RESOLUTION GRAPHICS
- 50 MEGABYTE DISK SPACE/USER

SECOND, LET'S DEFINE WHAT WE MEAN BY A NETWORK; AND AGAIN LET'S LIMIT OUR DEFINITION TO A NETWORK USED IN AN ENGINEERING AND SCIENTIFIC ENVIRONMENT:

ENGINEERING/SCIENTIFIC NETWORK

DEFINITION:

- A COMBINATION OF VARIOUS COMPUTING, PERIPHERAL, AND COMMUNICATIONS ELEMENTS.
- WORKING TOGETHER.
- TO SERVE MULTIPLE APPLICATIONS REQUIREMENTS.

PLEASE NOTE TWO KEY WORDS IN THE PREVIOUS SLIDE: COMBINATION AND MULTIPLE.

LET ME BRING THESE TO YOUR ATTENTION AGAIN. A USEFUL NETWORK MUST COMBINE WIDE RANGING LEVELS OF COMPUTATION, POWER, AND FUNCTIONALITY WITH PERIPHERALS AND COMMUNICATIONS IN ORDER THAT IT FULFILLS THE REQUIREMENTS OF MULTIPLE APPLICATIONS ON THE NETWORK.

IN ORDER TO ACCOMMODATE MULTIPLE APPLICATIONS, THE NETWORK SHOULD HAVE AVAILABLE:

- COMBINATIONS OF ELEMENTS WITH DIFFERENT LEVELS OF COMPUTING PERFORMANCE AND FUNCTIONALITY;
- DIFFERENT OPERATING SYSTEMS TO ACCOMMODATE A WIDE VARIETY OF APPLICATIONS SOFTWARE AND TO ALLOW EXISTING USERS TO PRESERVE THEIR SOFTWARE INVESTMENT AND STILL TAKE ADVANTAGE OF NEW OPERATING ENVIRONMENTS;
- COMMUNICATIONS BETWEEN DIFFERENT USER ENVIRONMENTS.
- STANDARD HARDWARE AND SOFTWARE INTERFACES, ACCESSIBLE BY INDEPENDENT EQUIPMENT VENDORS (E.G., ETHERNET, TCP/IP);
- PERIPHERALS FROM A WIDE VARIETY OF VENDORS TO SATISFY SPECIFIC USER NEEDS;

TO SUM IT UP, A SINGLE NETWORK SOLUTION THAT PROVIDES FEW ALTERNATIVES TO THE USERS IS GENERALLY A COMPROMISE THAT SATISFIES NO ONE OR A SPECIFIC CONFIGURATION THAT WORKS WELL FOR A PARTICULAR CLASS OF USERS, BUT LACKS EITHER THE PERFORMANCE OR ECOMONIC JUSTIFICATION FOR A WIDE RANGE OF APPLICATIONS.

NOW THAT WE HAVE DEFINED WORKSTATIONS AND NETWORKS AS THEY PERTAIN TO ENGINEERING AND SCIENTIFIC ENVIRONMENTS, LET'S LOOK AT THE ADVANTAGES OF WORKSTATIONS. THEN LET'S LOOK AT THE SUPERMINI AND POINT OUT THE DIFFERENCE BETWEEN IT AND A WORKSTATION, AND PERHAPS AGREE ON WHEN A SUPERMINI ON A NETWORK MIGHT ACTUALLY BE MORE APPROPRIATE FOR A PARTICULAR CLASS OF APPLICATIONS THAN A WORKSTATION. AFTER THAT, I WILL SUGGEST THAT THE ULTIMATE ENVIRONMENT MAY BE THE COMBINATION OF WORKSTATION ELEMENTS AND SUPERMINI ELEMENTS IN ONE INTEGRATED NETWORK. A NETWORK OF COMPUTING ELEMENTS MUST SERVE THE APPLICATION REQUIREMENTS AND FINANCIAL CONSTRAINTS OF ALL THE USERS. AND IT IS VERY PROBABLE THAT THE PROPER CONFIGURATION IS NOT WORKSTATIONS ONLY, BUT A COMPATIBLE MIXTURE OF DIFFERENT LEVELS OF COMPUTING ELEMENTS.

THE INTEGRATED WORKSTATION HAS SOME CLEAR ADVANTAGES, AND I BELIEVE THAT IT WILL BECOME THE DOMINANT COMPUTING ELEMENT IN THE FUTURE. LET'S EXAMINE THE REASONS:

1) WORKSTATIONS, BETTER THAN MINIS, PROVIDE THE USER WITH A PREDICTABLE RESPONSE. THE RESOURCES ARE DEDICATED AND WITHIN A SPECIFIC CLASS OF APPLICATIONS, THE MACHINE ACTS IN A CONSISTENT MANNER.

2) WORKSTATIONS PROVIDE THE USER WITH A HIGH DEGREE OF INTERACTION. THEY ARE GENERALLY EASY AND COMFORTABLE TO USE. THEIR BIT-MAPPED DISPLAYS AND, TYPICALLY, THEIR WINDOW-MANAGED, MOUSE-ORIENTED INTERFACE, CREATE AN EFFICIENT, PRODUCTIVE, AND "FRIENDLY" OR FRIENDLIER ENVIRONMENT.

3) THE WORKSTATION BECOMES THE PRIVATE PROPERTY OF THE USER. PSYCHOLOGICALLY, THE PROGRAMMER, DEVELOPER, OR IMPLEMENTOR OWNES THE MACHINE. FEELING GOOD, IMPORTANT, AND IN CONTROL ALL MAKE THE WORKSTATION POPULAR WITH THE USER.

AT TWO OPPOSITE ENDS OF THE SPECTRUM, HOWEVER, THE WORKSTATION BECOMES LESS THAN THE IDEAL SOLUTION: THE JOB MAY BE TOO BIG, OR THE JOB MAY BE TOO SMALL.

LARGE COMPUTE-INTENSIVE, MULTI-TASKING APPLICATIONS VERY OFTEN REQUIRE COMPUTING RESOURCES OR SPECIAL PURPOSE ACCELERATORS THAT ARE NOT AVAILABLE WITH A TYPICAL WORKSTATION. THE POWER OF A SUPERMINI, INDEPENDENT OF COST, MAY BE REQUIRED JUST TO GET THE JOB DONE.

ALTERNATELY, SOME APPLICATIONS MAY REQUIRE VERY SMALL AMOUNTS OF COMPUTER RESOURCE AND, ALTHOUGH A TYPICAL WORKSTATION COULD EASILY HANDLE THE JOB, THE EXPENSE OF DEDICATING THE ENTIRE MACHINE TO A SINGLE-USER IS HIGHER THAN THE APPLICATION CAN JUSTIFY OR MORE THAN AN ALTERNATE SOLUTION MAY COST. A SUPERMINI SUPPORTING MULTIPLE USERS MAY PROVIDE THE PERFORMANCE LEVELS DEFINED FOR SPECIFIC APPLICATIONS WHILE SHARING THE COST OF A MACHINE ACROSS A NUMBER OF USERS. THE RESULT: A COST/USER LOWER THAN THE COST OF A DEDICATED MACHINE WHILE THE USER RECEIVES ADEQUATE OR APPROPRIATE RESPONSE IN A MULTI-USER ENVIRONMENT.

ADD TO THIS A NETWORKING ELEMENT, PERHAPS SIMILAR TO THAT USED BY WORKSTATIONS AND WE HAVE CREATED WHAT I CALL A NETWORK SUPERMINICOMPUTER. LET'S EXAMINE ITS FEATURES.

FIRST, IT IS BUILT AROUND A BASIC COMPUTING ELEMENT, PERHAPS EVEN THE SAME ONE THAT FORMS THE FOUNDATION OF OUR WORKSTATION. NEXT, AND MOST IMPORTANTLY, IT CAN PROVIDE MULTIPLE LEVELS OF PROCESSING POWER USING THE COMPUTING ELEMENT AS BASE LEVEL 1 AND COMPATIBLE MACHINES 3-5 TIMES MORE POWERFUL THAN THE SINGLE ELEMENT MACHINE.

ALSO, ANY LEVEL OF COMPUTING PERFORMANCE CAN BE DEDICATED TO ONE USER OR SPREAD AMONG MANY USERS, DEPENDING UPON APPLICATION REQUIREMENTS AND USER DEMANDS. GRAPHICS IS CERTAINLY A REQUIRED OPTION, BUT ITS FEATURES AND BENEFITS SHOULD BE AVAILABLE TO MULTIPLE USERS. ALSO, DEPENDING UPON THE APPLICATION OR MIX OF APPLICATIONS, USERS SHOULD BE ABLE TO SELECT FROM A VARIETY OF GRAPHIC DEVICES COLOR OR MONOCHROME, TIGHTLY COUPLED OR TERMINAL DEVICES, 2D AND 3D, INEXPENSIVE TO FULL FEATURE. COMPUTE AND DISPLAY INTENSIVE APPLICATIONS LIKE SOLID MODELING ANALYSIS AND RENDERING SHOULD HAVE SPECIAL PURPOSE DEVICES AVAILABLE TO EFFICIENTLY CALCULATE AND DISPLAY DATA.

ON THE OTHER HAND, MANY APPLICATIONS CALL FOR A SIMPLE ALPHA-NUMERIC TERMINAL AS THE I/O DEVICE OR PERHAPS A CLUSTER OF TERMINALS IS THE APPROPRIATE SOLUTION. NO NEED TO INCREASE SYSTEM COSTS -- LOW-COST TERMINALS MUST BE AVAILABLE.

MULTI-USER MACHINES OR NETWORKS WITH MANY USERS IMPLY DIFFERENT APPLICATIONS. THUS, A TRUE MULTIUSER ENVIRONMENT SHOULD HAVE AVAILABLE A LARGE SET OF TOOLS FOR DEVELOPMENT AND EXECUTION. MULTIPLE CONCURRENT OPERATING SYSTEMS, EASILY AVAILABLE TO EACH USER, WOULD BE IDEAL. DIFFERENT OPERATING SYSTEMS SHOULD COMPLEMENT EACH OTHER WITH RESPECT TO THE TYPE OF APPLICATIONS THAT THEY ARE MOST IDEALLY SUITED. UNIX, FOR INSTANCE, FOR SOFTWARE DEVELOPMENT, SMALLTALK FOR GRAPHICS AND SIMULATION, PICK PERHAPS, FOR DATABASE.

AND LET'S NOT FORGET COMMUNICATIONS. THE ABILITY TO FREELY COMMUNICATE WITH OTHER ELEMENTS ON THE NETWORK, AS WELL AS OTHER NETWORKS OR ENVIRONMENTS, IS IMPORTANT IF WE ARE TO RETAIN FLEXIBILITY AND COMPANY-WIDE ACCESS, SUBJECT TO SECURITY CHECKS, TO ALL INFORMATION.

AS WITH MOST THINGS IN THIS WORLD, THERE IS NOT ONE PERFECT SOLUTION. BUT A NETWORK THAT SUPPORTS DIFFERENT ELEMENTS THAT MEET THE NEEDS OF A DIVERSE NUMBER OF USERS AND APPLICATIONS IS SURELY SUPERIOR TO A NETWORK THAT SUPPORTS ONLY ONE SPECIFIC CLASS OF MACHINES.

FURTHERMORE, I MAINTAIN THAT A NETWORK THAT NOT ONLY SUPPORTS BUT INTEGRATES DIFFERENT CLASSES OF WORKSTATIONS AND MULTIPLE-USER SUPERMINIS IS MORE PROBABLE TO MEET THE REQUIREMENTS OF THE ENGINEERING AND SCIENTIFIC DEPARTMENTS THAT WE SERVE. THE ABILITY TO CONTINUE TO LOWER THE COST PER USER, NOT ONLY BY REDUCING THE PRICE PER ELEMENT, BUT ALSO BY BEING ABLE TO SHARE CERTAIN ELEMENTS, WHEN APPROPRIATE, MAKES THE DAY A LOT CLOSER WHEN THE ENGINEERING AND SCIENTIFIC NETWORK IS INTEGRATED, OR EXPANDED, WITH THE COMPUTING REQUIREMENTS OF OTHER DEPARTMENTS. BUT THAT'S THE TOPIC OF ANOTHER TALK.

NOW, LET'S GO ONE STEP FURTHER AND SEE WHAT HAPPENS WHEN WE ATTEMPT TO INTEGRATE DIFFERENT COMPUTING ELEMENTS INTO ONE NETWORK ENVIRONMENT.

MOST NETWORKS, TODAY, PROVIDE A MORE EFFICIENT, HIGHER SPEED MECHANISM TO TRANSFER INFORMATION FROM ONE NETWORK ELEMENT TO ANOTHER THAN THE TYPICAL SERIAL COMMUNICATIONS AVAILABLE WITH MOST COMPUTERS. THIS IS WHAT I CALL A NETWORK OF COMPUTERS.

THE NEXT STEP IS A COMPUTING NETWORK, OR THE CREATION OF A COMPUTER ACROSS THE NETWORK, A NETWORK ENVIRONMENT. IN THIS CASE, A USER SEES NOT ONLY THE MACHINE THAT HE HAPPENS TO BE SITTING IN FRONT OF, BUT, RATHER, ALL OF THE COMPUTING RESOURCES ON THE NETWORK APPEAR TO BE AVAILABLE TO ANY ONE OF MANY SINGLE USERS.

TODAY'S NETWORKS ARE FAST ENOUGH TO ALLOW FOR THE CREATION OF SUCH A COMPUTING ENVIRONMENT. YET VERY FEW COMPANIES HAVE DEVELOPED THE SOPHISTICATED SOFTWARE REQUIRED TO CREATE THIS ENVIRONMENT. THE DAY IS NOT FAR OFF, HOWEVER, WHEN THIS TYPE OF SOFTWARE WILL BE READILY AVAILABLE. TRUE NETWORKING SOFTWARE, WHEN COMBINED WITH ADVANCED, POWERFUL, FLEXIBLE COMPUTING ELEMENTS, WILL PROPEL US INTO A NEW ERA OF COMPUTING: THE COMPUTING NETWORK.

AT CURRENT NETWORK SPEEDS, EVEN A COMPUTING NETWORK MAY NOT BE FAST ENOUGH TO CLOSELY COUPLE MULTIPLE CPU'S AND PROVIDE A LARGE NUMBER OF USERS WITH THE LEVEL OF PERFORMANCE, AT A NEW LOW LEVEL OF COST, IN A MULTIUSER ENVIRONMENT, THAT HAS BEEN AVAILABLE FROM LARGE DEC, DATA GENERAL, GOULD, OR OTHER SUCH MACHINES. AND UNTIL 50-100 MBIT PER SECOND NETWORKS ARE RELIABLE AND AFFORDABLE, THE EFFICIENCIES AND PERFORMANCE OF A MULTI-PROCESSOR MACHINE MAY BE DIFFICULT TO DUPLICATE OVER A NETWORK.

THE DAY WILL COME, HOWEVER, WHEN THE COMBINATION OF SUPER FAST, EFFICIENT, SOFTWARE INTENSIVE, COST EFFECTIVE NETWORKS WITH MODERN WORKSTATION AND SUPERMINI COMPUTING ELEMENTS ARE JOINED TO FORM A SUPERMINI ACROSS THE NETWORK. A COMPUTING RESOURCE OF AWESOME PROPORTIONS WILL BE THE RESULT.

THUS, DEPENDING UPON THE APPLICATION, EVEN A NETWORKED SOLUTION WILL REQUIRE AT LEAST TWO LEVELS OF COMPUTER TO MEET THE NEEDS OF A DIVERSE NUMBER OF USERS AND APPLICATIONS. A SOFTWARE-DEPENDENT, RESOURCE-SHARING NETWORK OF WORKSTATIONS AND SUPERMINIS, SINGLE AND MULTIUSER, EASILY CONFIGURED TO MEET THE REQUIREMENTS OF A PARTICULAR ENVIRONMENT SHOULD BE THE ARCHITECTURAL COMMON DENOMINATOR FROM WHICH TO DEVELOP THE SPECIFIC SOLUTION FOR AN INDIVIDUAL INSTALLATION.

LET'S GO BACK TO BASICS. START WITH A POWERFUL, FLEXIBLE COMPUTING ELEMENT. USE IT TO CREATE CONFIGURATIONS THAT MEET THE REQUIREMENTS OF THE WIDE VARIETY OF APPLICATIONS TO BE RUN. CONNECT THE ELEMENTS AND CREATE NOT A NETWORK OF COMPUTERS, BUT RATHER A COMPUTING NETWORK.

BUILD A STRONG FOUNDATION. REMEMBER, COMPUTERS AND NETWORKS SHOULD BE THE SLAVES. THEY ARE THERE TO SERVE THEIR MASTERS, THE USERS. START BY DEFINING THE PROBLEM AND THEN PROVIDE THE NETWORK ELEMENTS THAT WILL MOST EFFECTIVELY SOLVE PROBLEMS, NOT CREATE NEW ONES.

IT'S ELEMENTARY!

THANK YOU FOR YOUR ATTENTION. I WOULD BE HAPPY TO ANSWER ANY QUESTIONS.

Nielsen Dataquest

START-UP: BUILDING THE MANAGEMENT TEAM

Arthur T. Campbell
President
Mosaic Technologies, Inc.

Mr. Campbell joined Mosaic Technologies, Inc., in late 1983 as President, Chief Executive Officer, and Director. From 1970 until joining Mosaic Technologies, he was employed by Digital Equipment Corporation in various management and marketing and sales positions. Most recently, he was the general manager of Digital's Terminals Product Group. Mr. Campbell has been directly involved with the computer industry in management, sales and marketing, and engineering capacities for more than twenty years. Mr. Campbell received a B.S.E.E. from Tufts University, an M.S.E.E. from Northeastern University, and an M.B.A. from Harvard University.

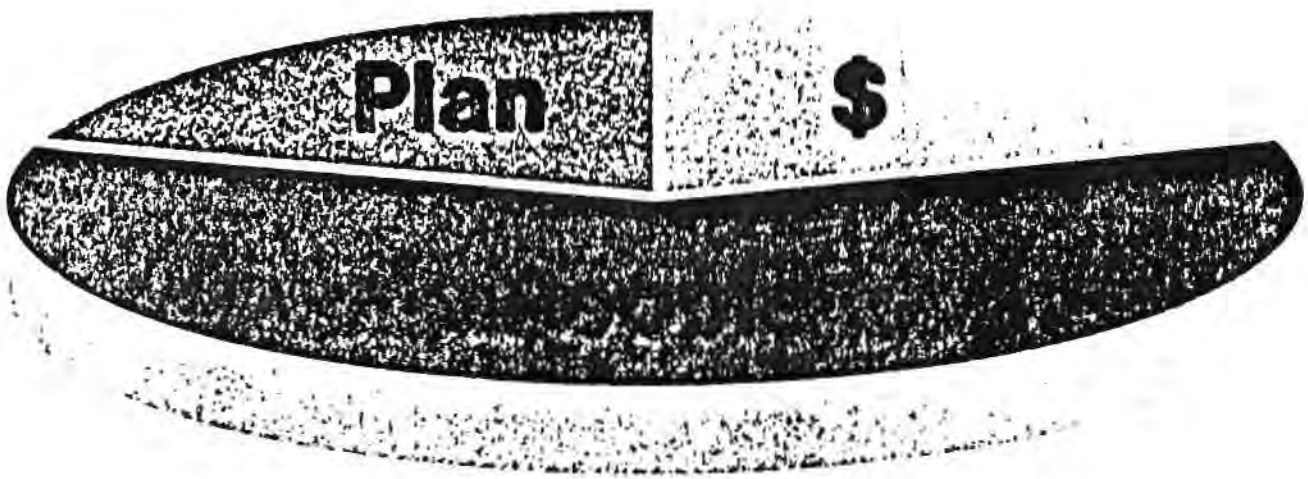
Dataquest Incorporated
WORKSTATION FOCUS CONFERENCE
August 13 and 14, 1984
Burlington, Massachusetts

BUILDING THE STARTUP TEAM

"People Make the Difference"

Mosaic Technologies, Inc.

A NEW COMPANY IS:



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FINDING THE RIGHT PEOPLE

- ☐ Skills
- ☐ Find and Integrate
- ☐ Culture
- ☐ Organizational Tasks
- ☐ Execute

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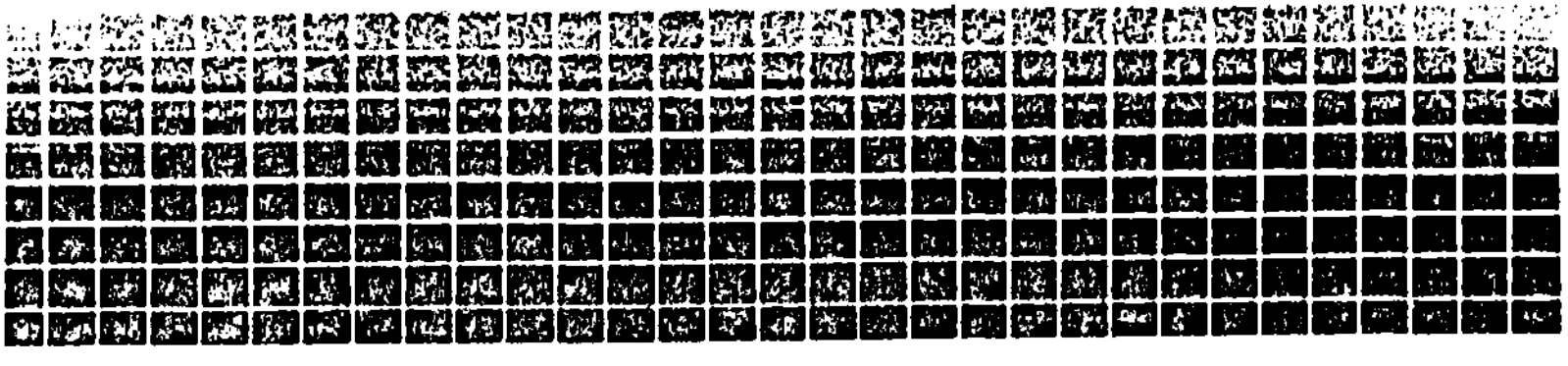
MOSAIC IS

- A Graphics Computer System Company
- Focused on the Technical Markets



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WHAT

- High Performance, Integrated Graphics Technical Workstations
- Covering $25,000 - $60,000 Price Range
- New Standards of Price Performance
- Parallel Processing Hardware Architecture
- Object Oriented Software Architecture

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WHO

- 16 Months Old
- 90 Employees
- Announced 8 Shared Vision Systems in July
- 1st Shipment In August

Mosaic

TECHNICAL USER NEEDS

- ☐ Responsive System
- ☐ Sophisticated Application Software Environment
- ☐ Customization and Growth Capabilities
- ☑ Cost Effectiveness

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Mosaic

TECHNICAL USER NEEDS	MOSAIC PROVIDES
☐ Responsive System	☐ Integrated Design ☐ 32-Bit Computer System ☐ Bit-Slice Graphics Processor
☐ Sophisticated Application Software Environment	☐ Object Oriented Graphics and Data Management Environment ☐ Software Standards
☐ Customization and Growth Capabilities	☐ Open Architecture ☐ Standards
☐ Cost Effectiveness	☐ New Standard in Price-Performance

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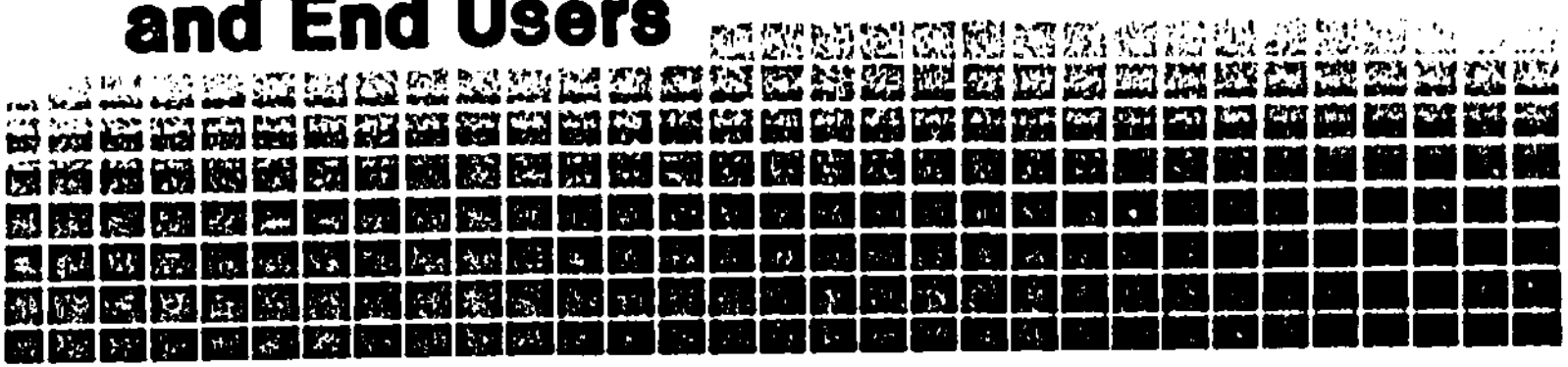
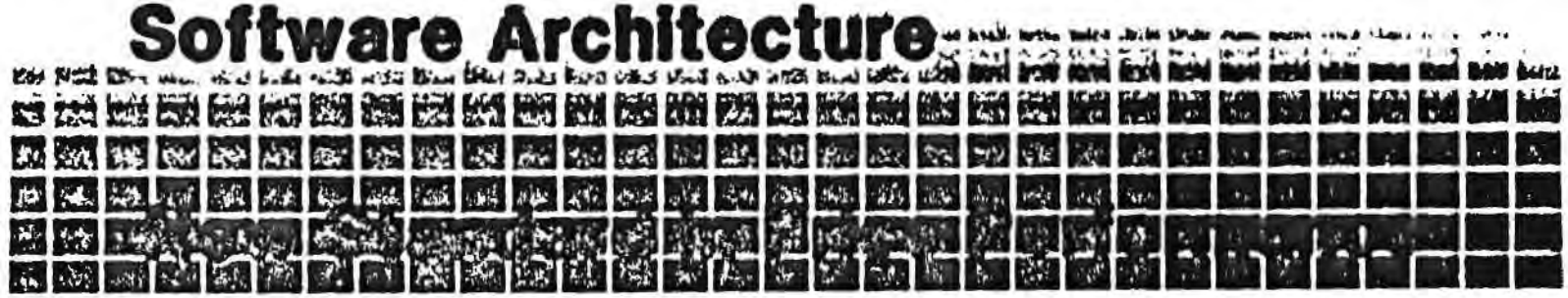
MOSAIC'S GOAL

- Premiere Graphics Computer System
- Supplier to Technical OEM's and End Users



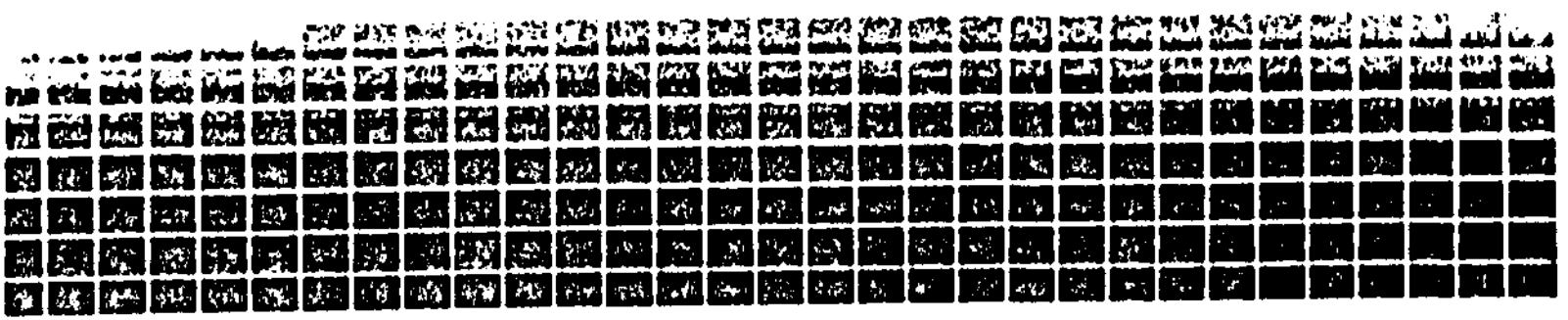
MOSAIC UNIQUENESS

- Integrated Graphics Computer System
- High Performance
- Open Architecture
- Networked, Object Oriented Software Architecture



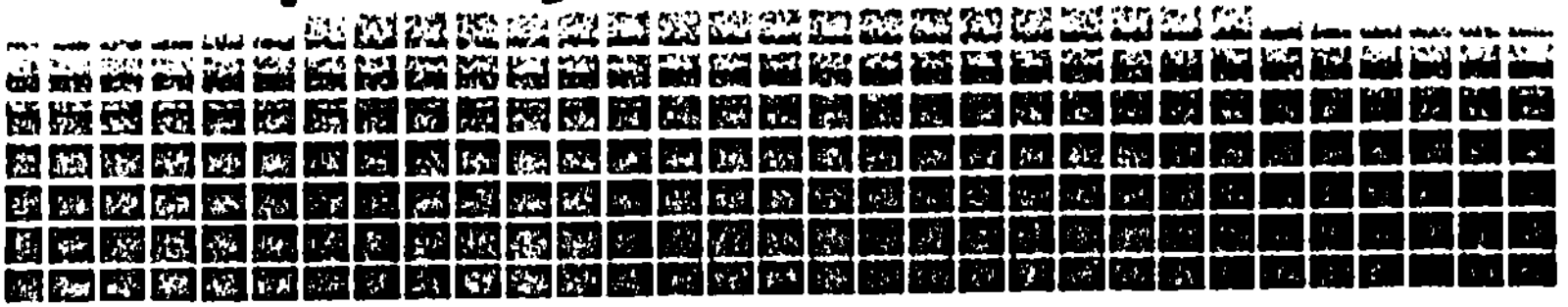
BUILDING THE TEAM

UNIQUE SKILLS AND ENTREPRENEURIAL ATTITUDES



TEAM EXPERIENCE

- Market and Application
- Functional Areas
- Computer Systems



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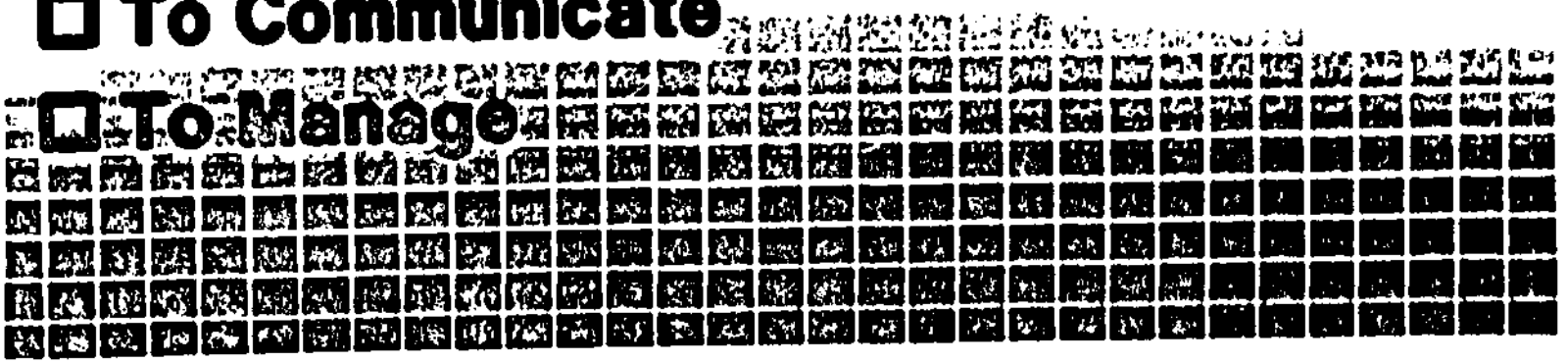
TEAM ABILITIES

- ☐ To Focus
- ☐ To Plan
- ☐ To Execute
- ☐ To Communicate
- ☐ To Manage



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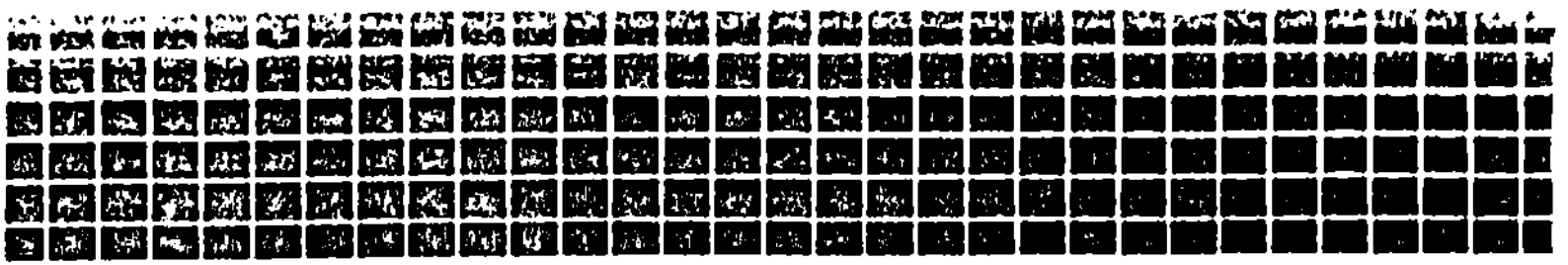
THE CULTURE

- ☐ Common Goal
- ☐ Results Oriented
- ☐ Responsive to Change
- ☐ Realistic
- ☐ People Oriented

THE KEY INGREDIENTS

- ☑ Experience
- ☑ Teamwork
- ☑ Desire to Win.



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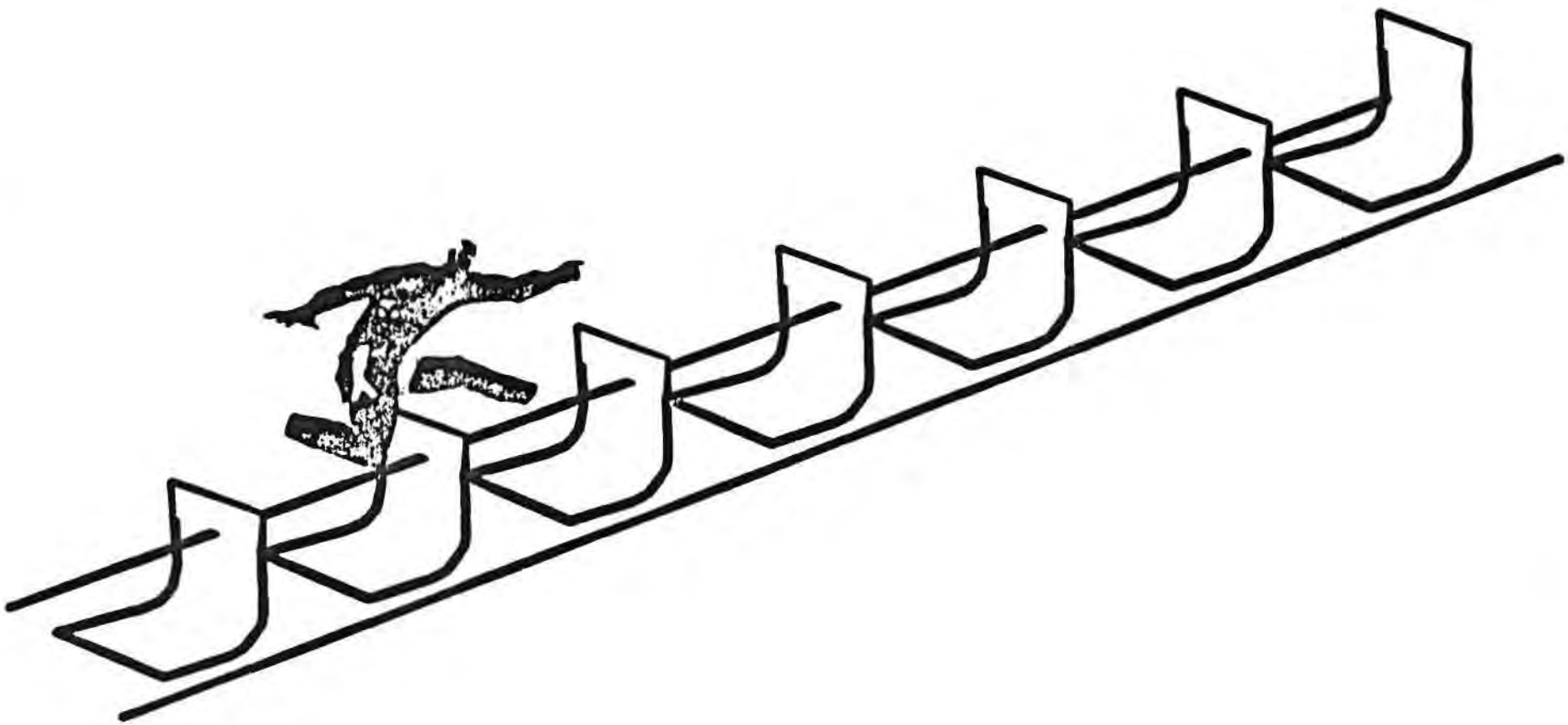
THE STARTUP HIGH HURDLES



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HURDLE # 1
Organization and Finance

- ☐ Technical Workstation Focus
- ☐ Unique Solution Mapped to Focus Need
- ☐ Outstanding Engineering Team

HURDLE #2
Engineering

? Development Time
? Resources
? Product Performance
? Product Cost

- ☐ Computer Systems Skills
- ☐ Schedule Driven
- ☐ Performance Oriented Design Center
- ☐ Cost Consciousness

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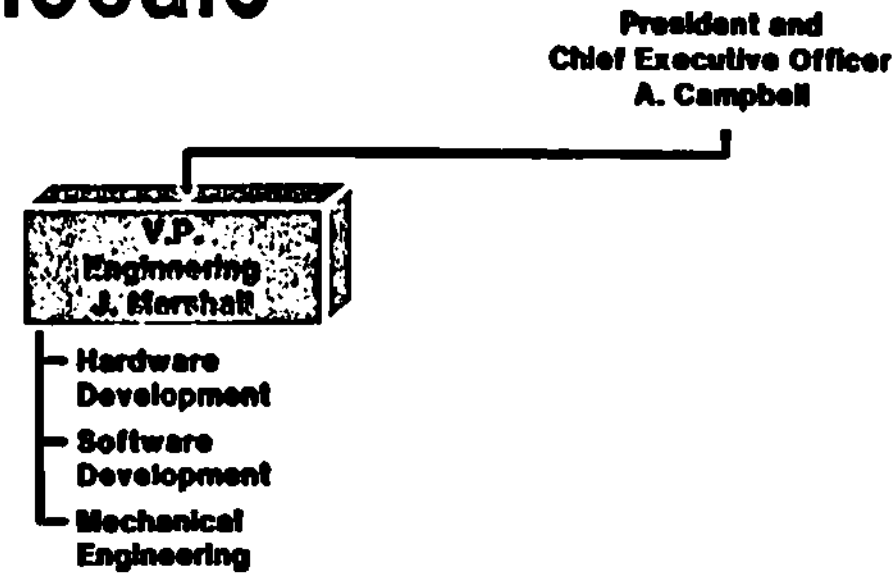
Mosaic



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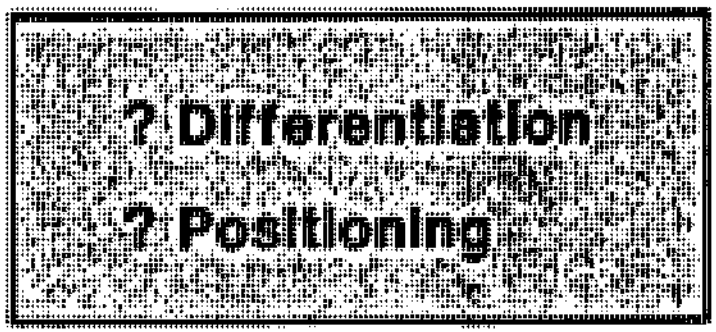
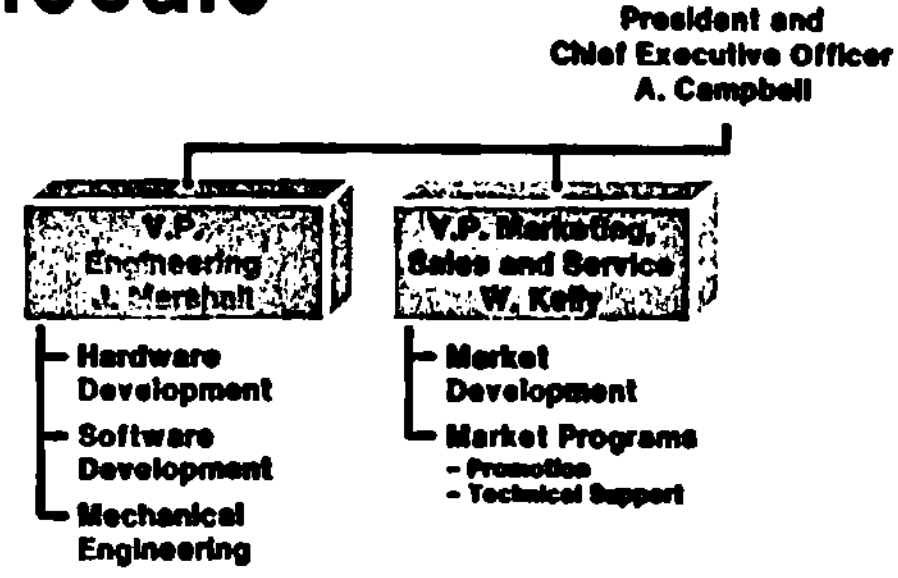
HURDLE #3
Marketing



- ☐ Market Focus - CAE, CAD, CAM, Technical Applications
- ☐ Competitive Understanding - Products and Strategies
- ☐ Tactical Skills

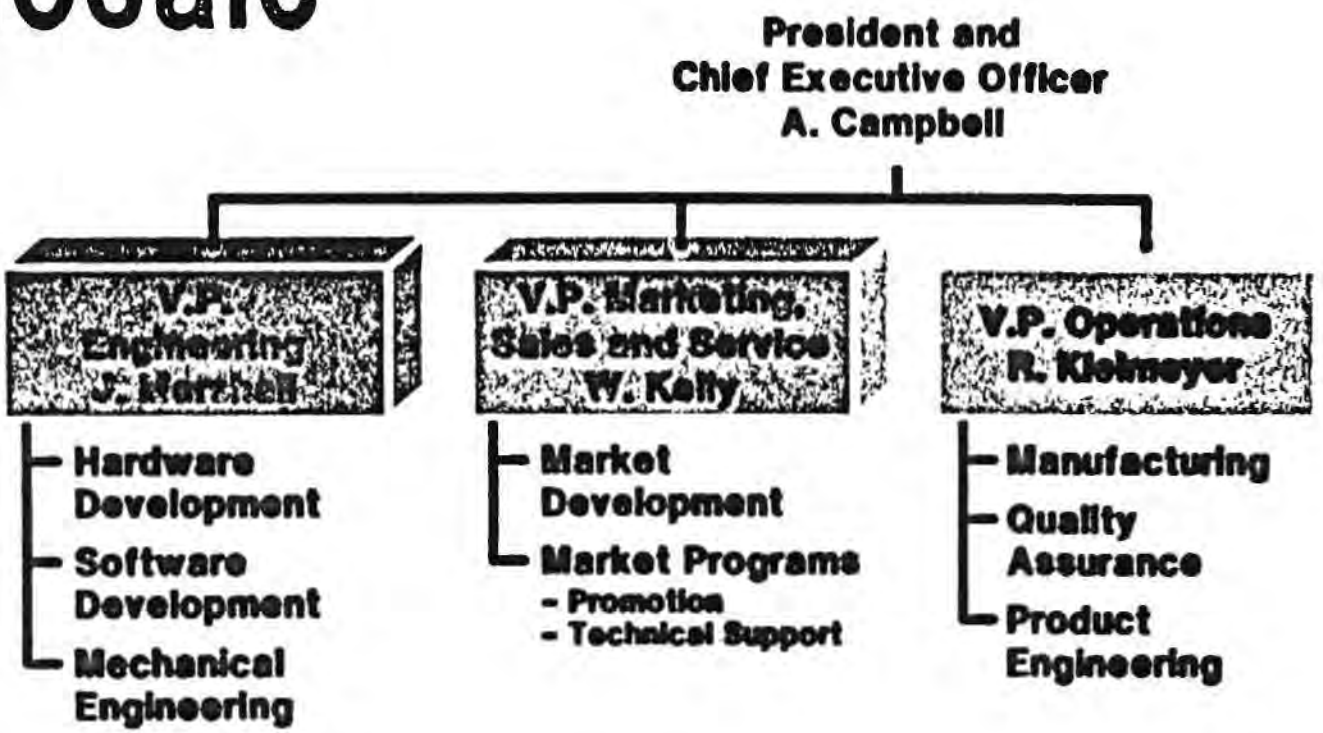
Mosaic



HURDLE #4
Manufacturing

- ☐ Start-Up Company Manufacturing Experience
- ☐ High Volume Manufacturing Experience
- ☐ Quality Orientation
- ☐ Systems and Controls Oriented

Mosaic



HURDLE #5
Sales

? Customers
? Pricing
? Promotion

- ☐ Sales Mgmt. Experience - Computer Systems, Workstations
- ☐ Target Account Focus
- ☐ Outstanding Sales Skills
- ☐ Happiness is a Tough Competitive Win

HURDLE #6
Customer Support

? Support Base
? Resource Distribution
? Volume Build-Up

- ☐ Computer Systems Experience
- ☐ Planning and Control Skills
- ☐ Services as Business Leverage
- ☐ Customer Satisfaction Driven

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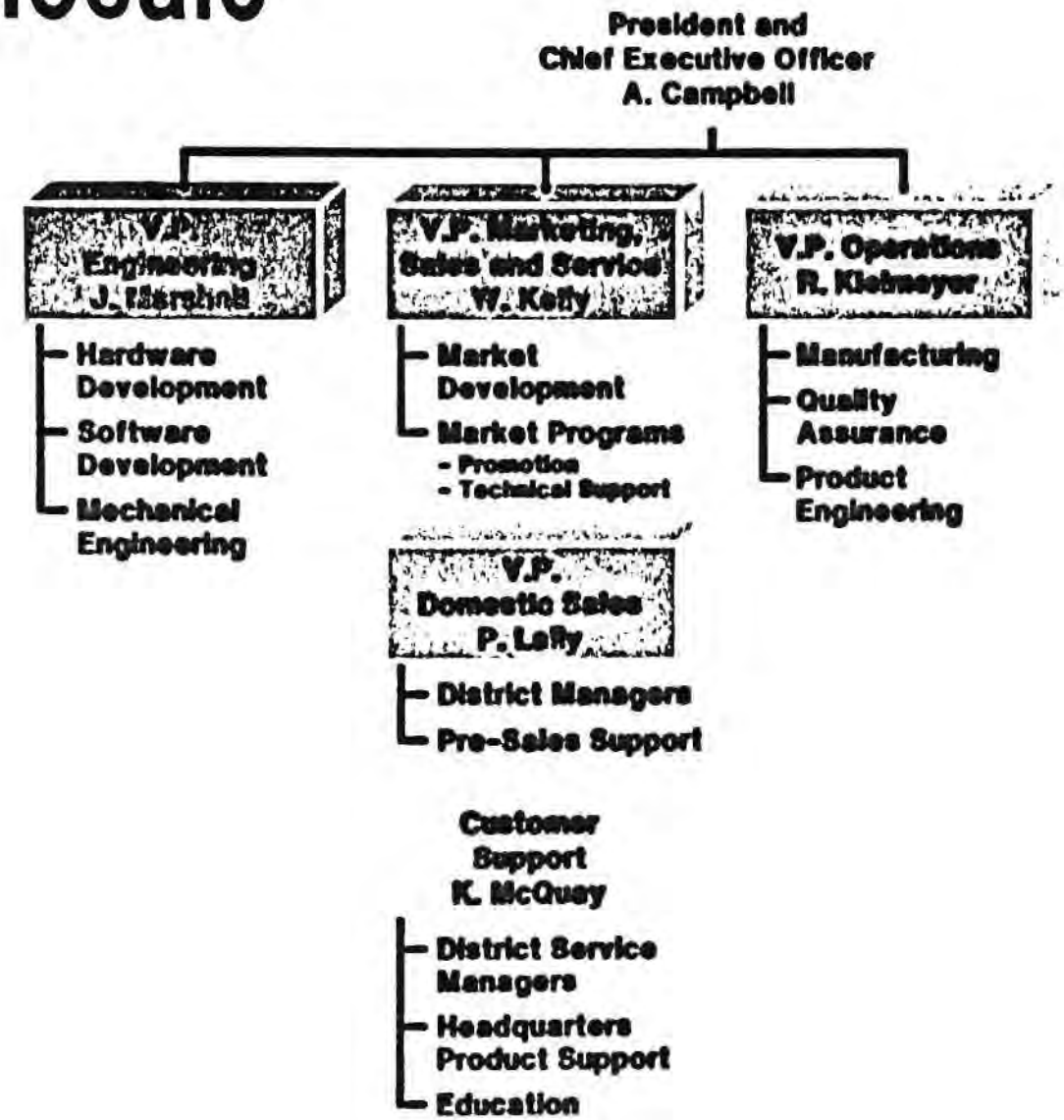
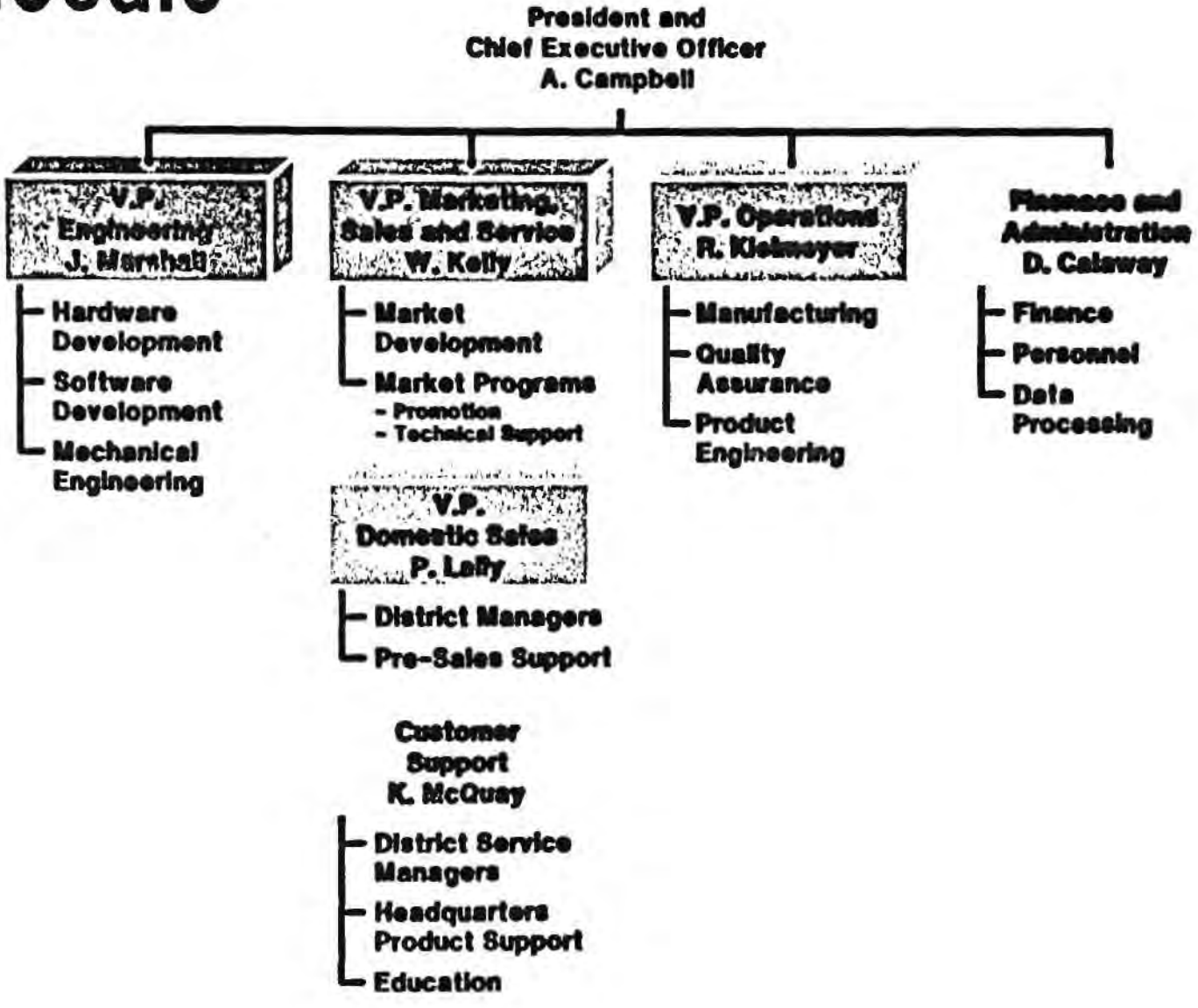


HURDLE # 7
Do it Again

- ☐ Long Term Orientation
- ☐ Build a Company, Not Just a Product
- ☐ Market Focus ◄► Technology Management

Mosaic



BUILDING THE COMPANY
PEOPLE
PEOPLE

The Standard in Graphics Computer Systems

Nielsen Dataquest

FLEXIBLE SYSTEMS ARCHITECTURE

Dennis Peck
President and CEO
Saber Technology Corporation

Mr. Peck is responsible for all aspects of Saber's operation including long-range corporate planning and development, and overseeing the company's professional growth. Mr. Peck has an extensive background in sales, marketing, and general management, including almost 20 years experience in the computer systems industry. Prior to joining Saber in February, 1984, Mr. Peck served as general manager of NCR Corporation's $350 million medium and large-scale computer system business unit in San Diego. He was responsible for NCR's largest development and production business unit. Mr. Peck obtained his M.B.A. and B.A degrees from Bowling Green State University in Ohio.

Dataquest Incorporated
WORKSTATION FOCUS CONFERENCE
August 13 and 14, 1984
Burlington, Massachusetts

FLEXIBLE SYSTEM ARCHITECTURE WORKSTATIONS

DENNIS M. PECK

SABER TECHNOLOGY CORPORATION
SAN JOSE, CALIFORNIA

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FLEXIBLE SYSTEM ARCHITECTURE

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I. COMPANY INTRODUCTION

A. FOUNDED 1982 TO BECOME A SUBSTANTIAL COMPANY BY SUCCESSFULLY DEVELOPING AND MARKETING A FAMILY OF NEXT GENERATION WORKSTATIONS.

B. RELEASED INITIAL PRODUCT AT NCGA IN MAY.

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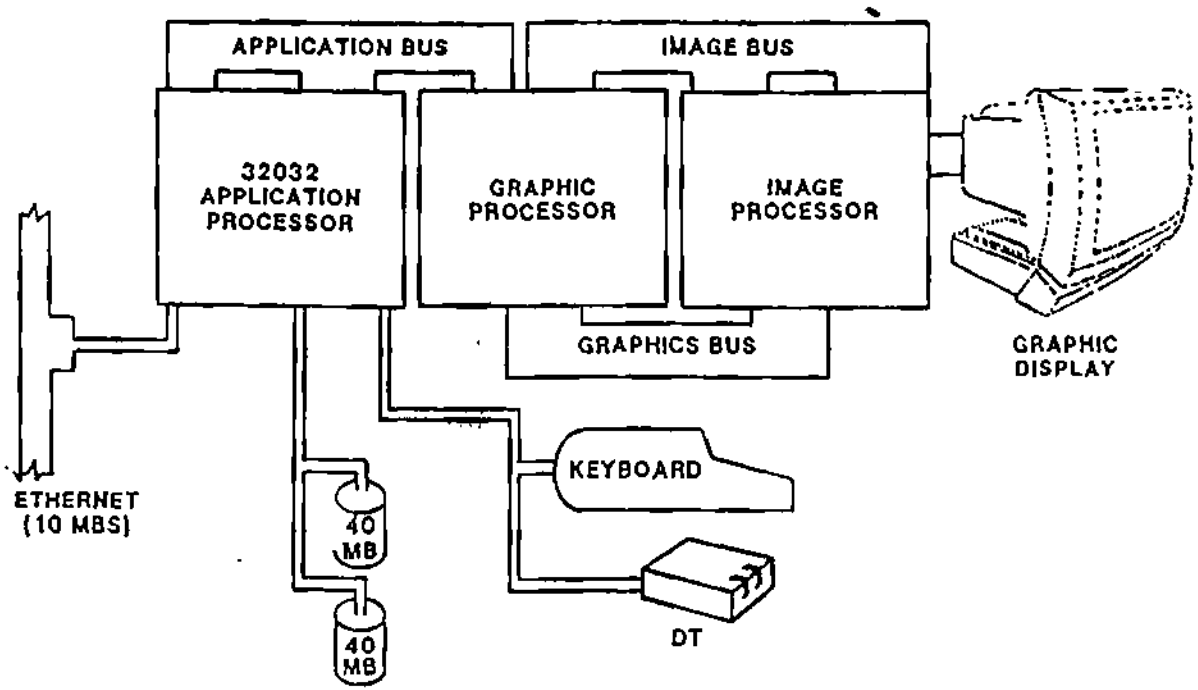
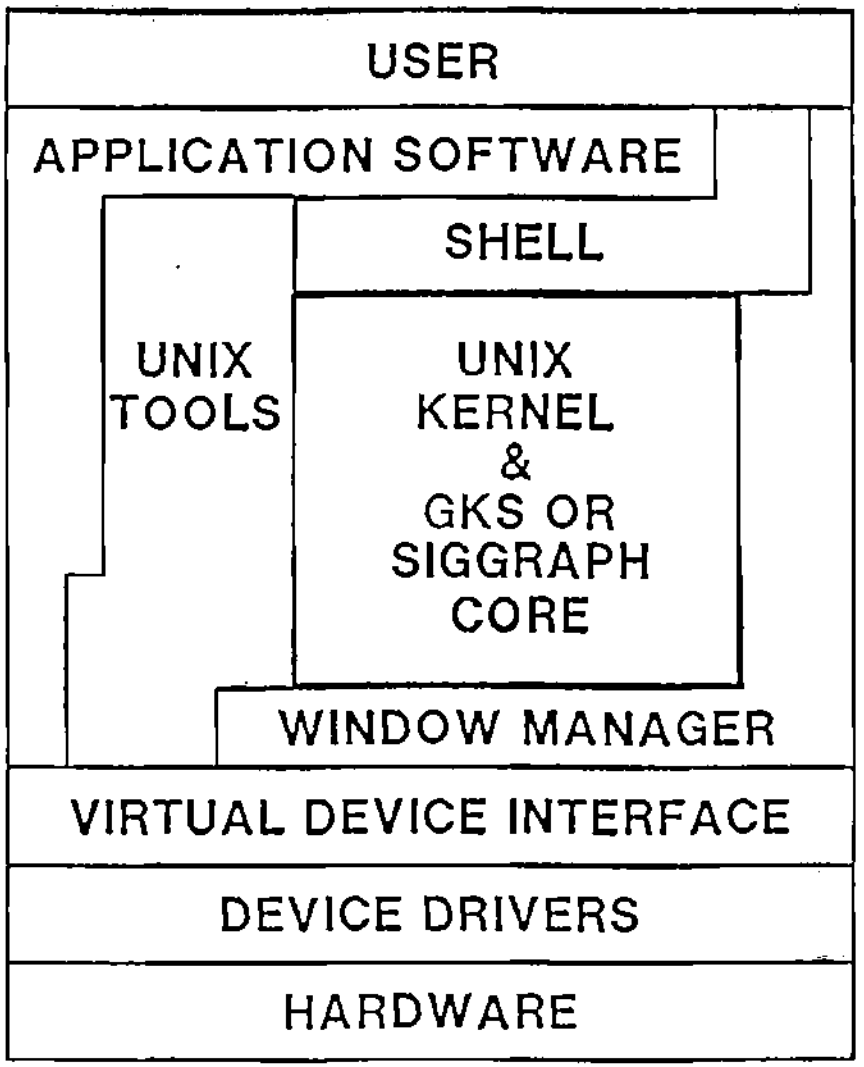
SABER TRIBUS ARCHITECTURE

HARDWARE



- APPLICATIONS PROCESSOR
- GRAPHICS PROCESSOR
- IMAGE PROCESSOR
- DISPLAY
- BUS STRUCTURE
- PERIPHERALS

SABER SOFTWARE



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SABER MAINFRAME COMMUNICATIONS

II. WHAT IS A FLEXIBLE SYSTEM ARCHITECTURE

A. A SYSTEM THAT MEETS A WIDE RANGE OF APPLICATION NEEDS

1. CAD ARCHITECTURAL
2. CAD MECHCANICAL
3. CAD ELECTRICAL
4. CAE
   - A. PCB LAYOUT
   - B. I.C. DESIGN
   - C. LOGIC/CIRCUIT SIMULATION

B. A SYSTEM THAT CAN GROW IN PLACE

1. MIGRATION PATH ENGINEERING
   - A. ADD PERIPHERALS, FEATURES, ACCELERATORS AS THE NEED ARISES

C. A SYSTEM THAT WILL HAVE A LONG USEFUL LIFE

III. WHY EMPLOY A FLEXIBLE SYSTEM ARCHITECTURE

A. END USER

1. SAME SYSTEM INTERFACE ACROSS APPLICATIONS

- A. LOWER TRAINING COSTS
- B. ECONOMY OF SCALE IN MAINTENANCE

2. COMPATIBLE SYSTEM TO MEET FUTURE NEEDS

3. LEVERAGED PURCHASES

4. LOWER COST OF OWNERSHIP

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B. SYSTEM RESELLER

1. COMPATIBLE HARDWARE /SOFTWARE PLATFORM FOR MULTIPLE APPLICATIONS

   A. ONE SOFTWARE PORT TO A FAMILY OF PRODUCTS

2. ECONOMIES OF SCALE

3. LOWER SUPPORT COST

4. MORE RESPONSIVE SUPPORT ORGANIZATION

5. LONGER PRODUCT LIFE CYCLE

6. IMPROVED MARGINS

C. SYSTEM MANUFACTURER

1. MEETS WIDE RANGE OF MARKET REQUIREMENTS

2. EXPERIENCE CURVE ECONOMIES

3. IMPROVED OVERHEAD MANAGEMENT

   A. TEST ENGINEERING

   B. MANUFACTURING ENGINEERING

   C. QUALITY CONTROL

4. IMPROVED SUPPORT COST MANAGEMENT

5. ENHANCED PRODUCT LIFE CYCLE AND MARGINS

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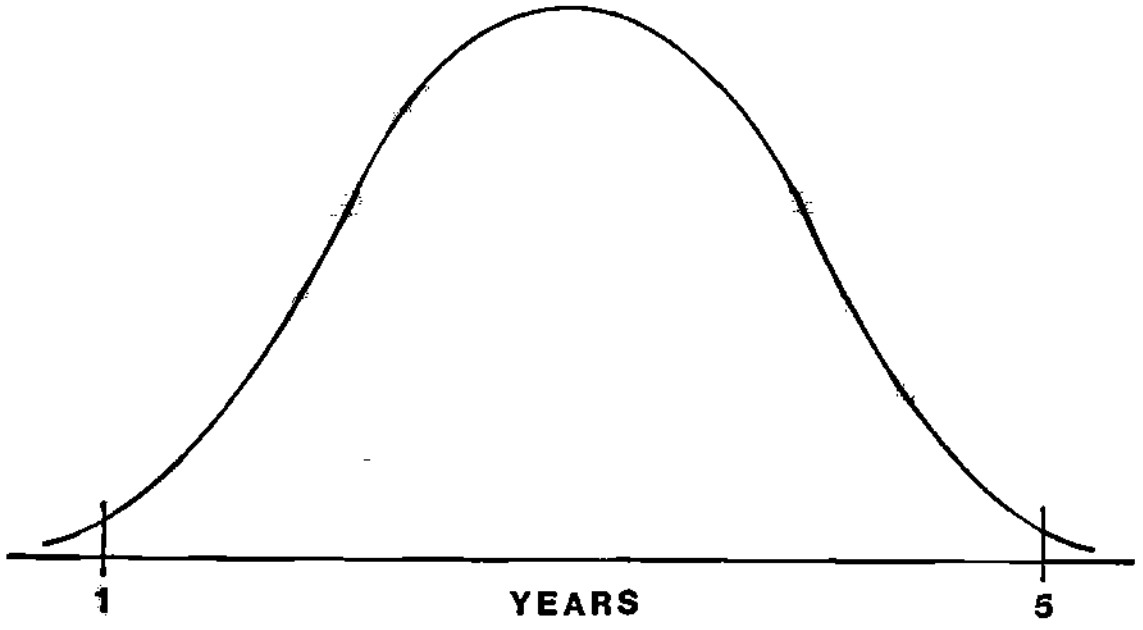
HOW

THE IMPLEMENTATION OF A FLEXIBLE SYSTEM ARCHITECTURE

LIFECYCLE PLANNING



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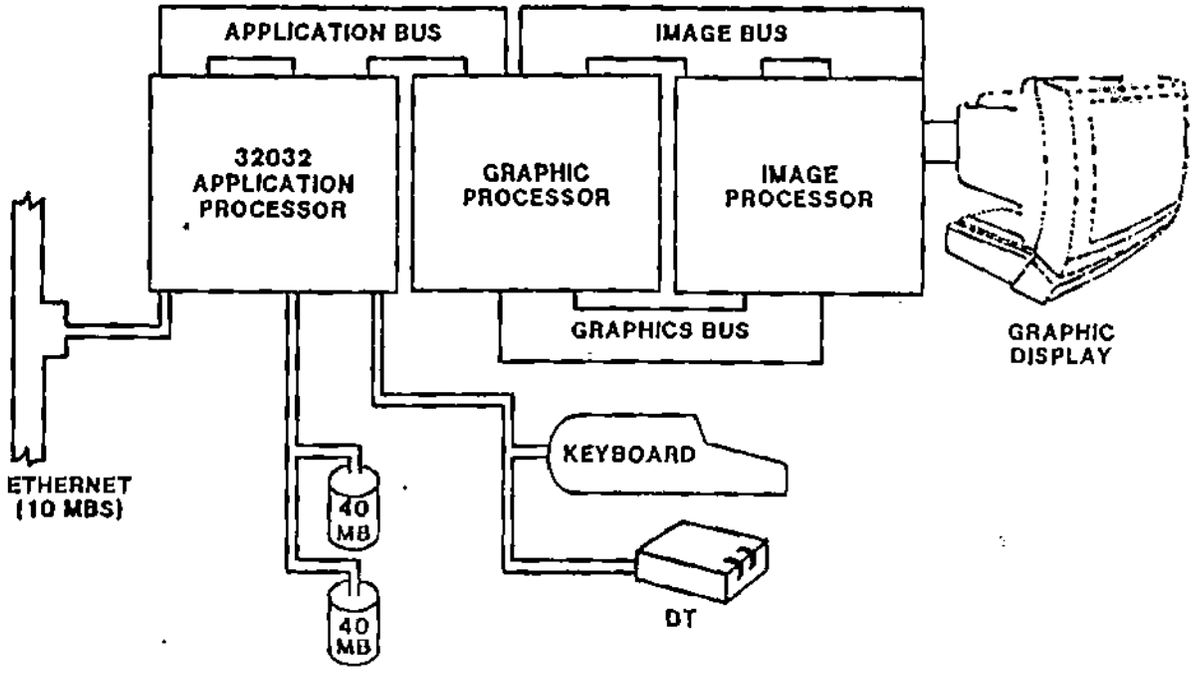
GRAPHICS PROCESSOR



- HIGH PERFORMANCE OP CODE/DATA BUS DESIGNED TO SUPPORT APPLICATION ACCELERATORS:
  - MATRIX TRANSFORMATION
  - ARRAY PROCESSING
  - HIGH SPEED FILL
  - TILE GENERATORS
  - MESH GENERATORS
- SCALABLE HARWARE FONT PROCESSING
- DIRECT ACCESS TO MASS STORAGE

A. EXPANDABLE

1. MAIN MEMORY 1-16 MB
2. ADDITIONAL DISC AND TAPE
3. COMMUNICATION - LANS, COAX, RS 232, SNA
4. FLEXIBLE I/O - TABLETS, PLOTTER, MICE

B. LONG LIFE CYCLE

1. 256 K MEMORY CHIPS

2. IMPROVED PERFORMANCE

A. DUAL PROCESSOR - INCREASED PERFORMANCE 1.8

B. CACHE

C. UNIX ACCELERATORS

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D. CHIP EVOLUTION

1. 32132 - 12 (1985) INCREASED PERFORMANCE .2
2. 32232 - 12 (1985) INCREASED PERFORMANCE .5
3. 32332 - 15 (1986) INCREASED PERFORMANCE 2.3
4. 32C432 - 15 (1987) INCREASED PERFORMANCE 4.7

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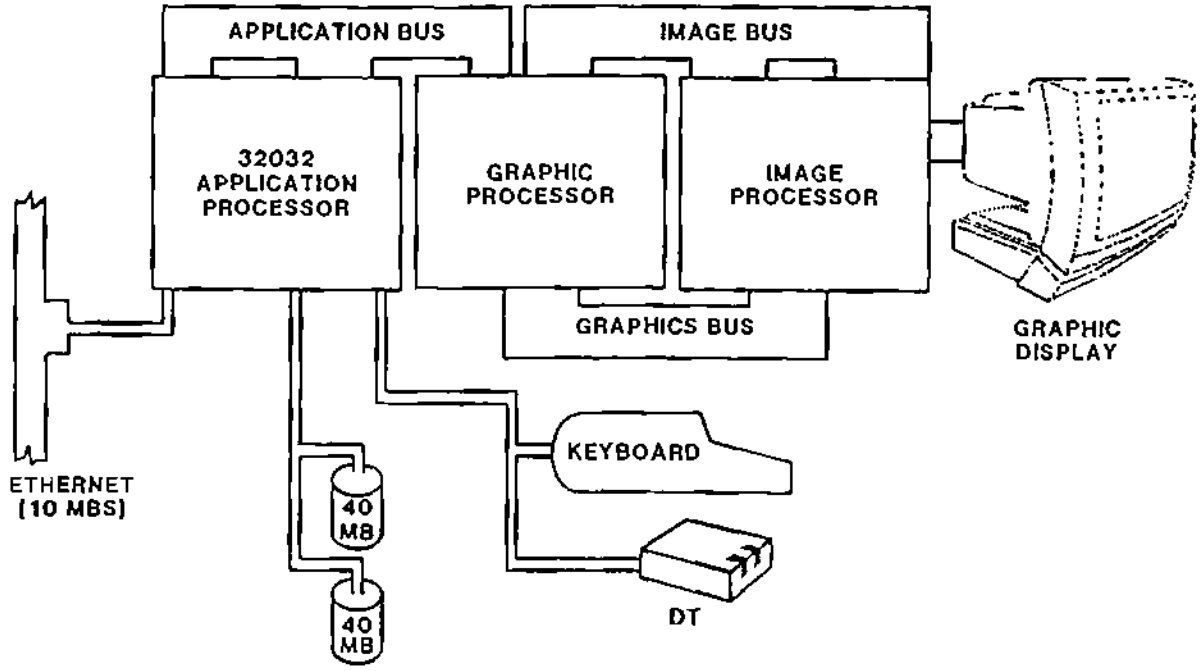
GRAPHICS PROCESSOR



- HIGH PERFORMANCE OP CODE/DATA BUS DESIGNED TO SUPPORT APPLICATION ACCELERATORS:
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  - HIGH SPEED FILL
  - TILE GENERATORS
  - MESH GENERATORS
- SCALABLE HARWARE FONT PROCESSING
- DIRECT ACCESS TO MASS STORAGE

A. EXPANDABLE

1. PLUG IN ACCELERATORS

2. FIVE SLOT CHASIS

3. MATRIX TRANSFORMATIONS 120 K MATRIX TRANSFORMATIONS PER SECOND

4. POLYGON LINE FILL

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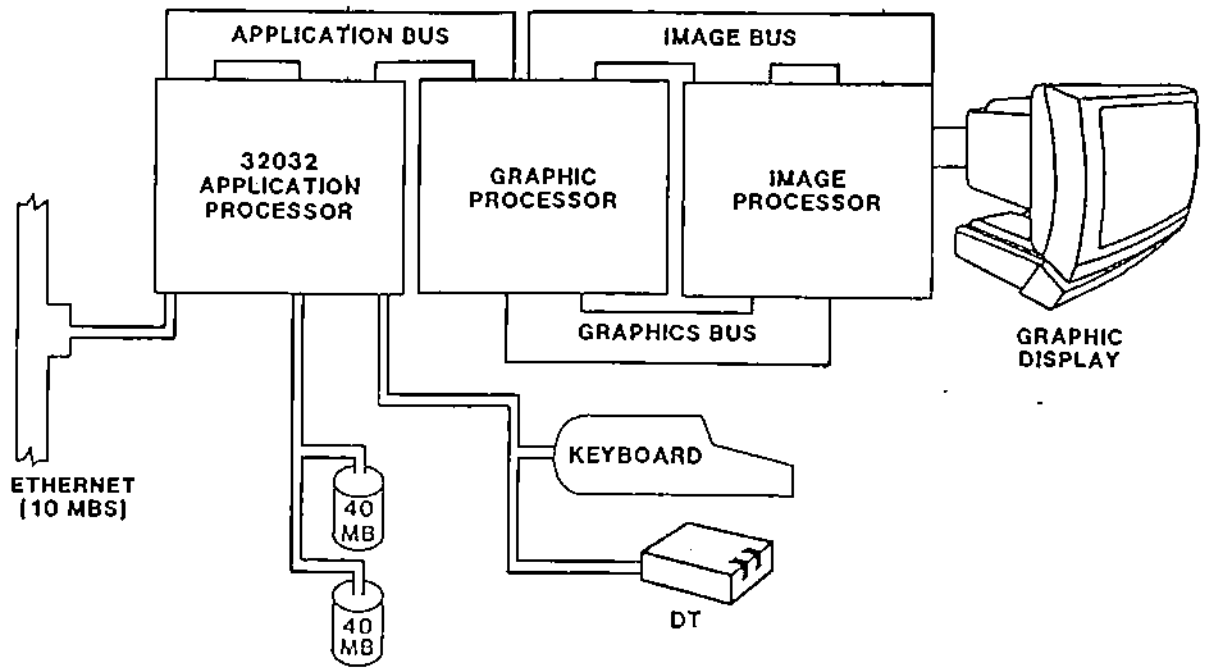
IMAGE PROCESSOR



- 2 MEGAPIXEL IMAGE PLANES
- 2 TO 24 PIXELS
- HIGH SPEED MEMORY ALLOWS MEMORY UPDATE SIMULTANEOUSLY WITH SCREEN UPDATE
- MEMORY CONFIGURED AS CONTINUOUS OR LAYERED IN BLOCKS DOUBLE BUFFERING
- 180MHz DAC WITH 8BIT RESOLUTION
- HIGH SPEED VIDEO LOOKUP TABLES FOR COLOR CONTROL
- FULL LOGICAL OPERATION SUPPORT

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B. EXTENDED LIFE CYCLE

1. ADDITIONAL ACCELERATORS

A. TILE GENERATORS

B. MESH GENERATORS

C. SIMULATION FUNCTIONS

2. LOWER COST

A. CUSTOM VLSI

A. IMAGE PROCESSOR EXPANDABILITY

1. 2 TO 24 M BYTE IMAGE PLANES
2. EXPANSION CHASSIS
3. HIGH SPEED DAC'S
4. 180 MHZ

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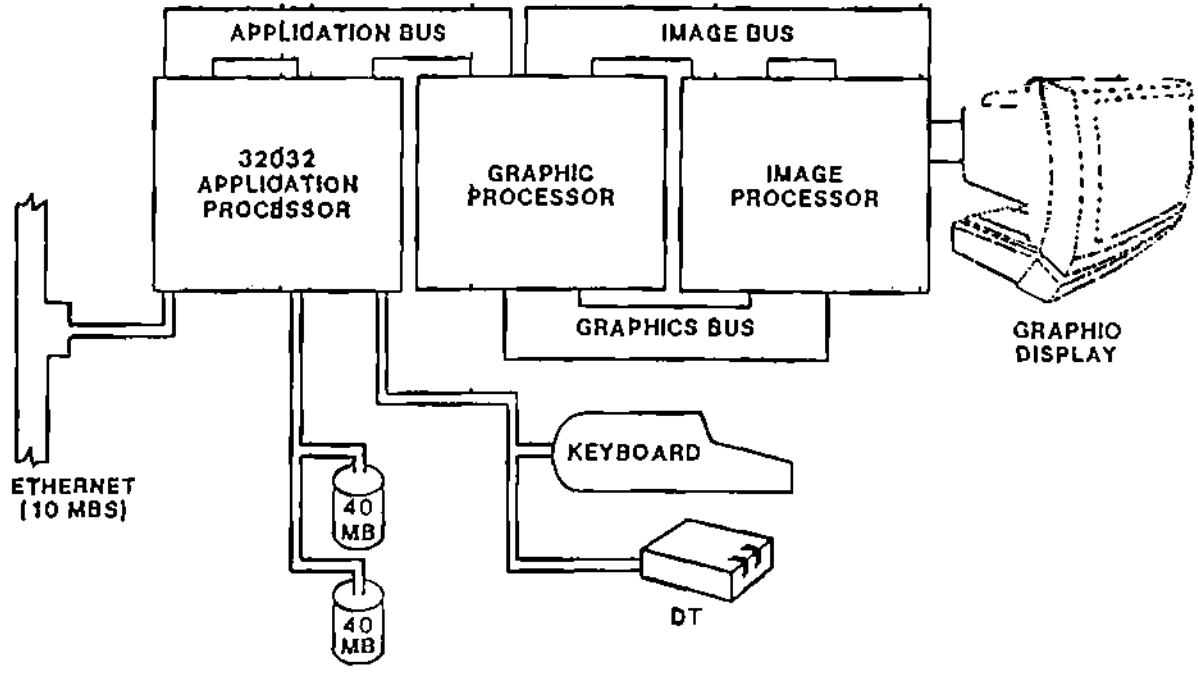
B. EXPANDED LIFE CYCLE

A. HIGHER DENSITY MEMORY CHIPS

B. LSI/VLSI IMAGE CONTROL UNIT

C. IMPROVED BANDWIDTH

DISPLAY OBJECTIVES



- FLICKER FREE (NON INTERLACED)
- ULTRA HIGH RESOLUTION (2M PIXELS)
- BRIGHT (FOR OFFICE USE)
- MINIMAL FOOTPRINT
- DIN SPEC DESIGN

A. DISPLAY FLEXIBILITY

1. MONOCHROME

2. COLOR

3. BANDWIDTH

4. RESOLUTION

5. EROGONOMICS

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B. LIFECYCLE PLANNING

1. RESOLUTION REVOLUTION

2. IMAGE DYNAMICS

3. HIGHER BANDWIDTH

4. COST REDUCTION

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SOFTWARE

- UNIX (4.2)
- ETHERNET DISTRIBUTED MASS STORAGE ENHANCEMENTS
- SIGGRAPH CORE (2D & 3D) PRIMITIVES
- GKS PRIMITIVES (2D) (3D)
- "C", PASCAL, FORTRAN 77
- PROGRAMMERS WORK BENCH
- WINDOW MANAGER

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A. SOFTWARE EXPANDIBILITY

1. ADHERANCE TO STANDARDS

A. 4.2 BSD

B. SIGGRAPH CORE

C. GKS CORE

D. VDI

2. OPTOMIZE FOR PERFORMANCE

A. OS AND LANGUAGES

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SABER MAINFRAME COMMUNICATIONS

B. LIFECYCLE PLANNING

1. UNIX STANDARDS

2. WINDOWS

3. FILE

4. NETWORKING

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A. NETWORKING EXPANDIBILITY

1. RS 232
2. LANS
3. HIGH SPEED LINKS

B. LIFE CYCLE PLANNING

INTEGRATED SYSTEMS

2. GATEWAY

3. SERVER ORIENTED NETWORK

SUMMARY

- FLEXIBLE ARCHITECTURE OFFER ECONOMIES TO:
  - END USER
  - SYSTEM HOUSE
  - OEM SUPPLIER
- LONGER LIFE CYCLE

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WHEN EVALUATING WORK STATION FROM A FLEXIBLE SYSTEM ARCHITECTURE

- PROCESSOR
- GRAPHICS
- IMAGE PROCESSOR
- MONITOR
- BASIC SOFTWARE AND TOOLS
- NETWORKING

PERFORMANCE ENHANCEMENT

VIA

APPLICATION-SPECIFIC HARDWARE

Arthur J. Collmeyer, WEITEK

Background

Advances in integrated circuit technology, coupled with advances in communication/networking technology have altered significantly the economics of computing. The microprocessor-based workstation has replaced the time-sharing terminal, giving the user the opportunity to interact with a dedicated computing resource, which in turn communicates efficiently with other computers in a networked environment. Apart from its potential for truly interactive computing, distributed computing is today an economically viable and often compelling alternative to centralized computing.

To maintain economic viability across a broad range of applications, distributed computing incorporates the concept of servers, which are shared resources, accessible by users via the network. Examples are file servers, peripheral servers (e.g., plotters, printers, etc.) and compute servers. Compute servers enable convenient access to more powerful computing facilities, for background processing or computationally-intensive tasks.

Problem: Computationally-Intensive Applications

The number of applications which stand to benefit from user interaction with a (dedicated) computer is great indeed. Many of these involve computationally-intensive tasks, tasks which place extreme demands on the computing resource. Such applications (e.g., CAE, CAD) depend on effective integration of servers into workstation networks. Moreover, in these applications, the capability of the server tends to limit the proliferation of workstations; as servers grow in power, the number of workstations capable of being supported increases.

Computationally-intensive tasks can be divided into two classes: numeric and non-numeric. Where arithmetic operations (multiply, divide, square root, etc.) predominate or real (floating point) numbers are involved, the task is described as numeric. Where sorting, searching, decision making (pointer arithmetic, compares, etc.) predominate, the task is described as non-numeric. Examples of computationally-intensive tasks - with their descriptors - are:

> Circuit Simulation (numeric)
> Logic Simulation (non-numeric)
> Placement/Routing (non-numeric)
> Design Rule Checking (non-numeric)
> Solid Modeling (numeric)
> Structural Analysis (numeric)

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Solution: Application Specific Hardware

To cope with the demands of computationally-intensive tasks, a number of options are available to system designers. The search for efficient (sometimes called "clever") algorithms is the most popular and can yield dramatic results. Novel hardware, optimized for the task, is another popular remedy. The combination of the two can be particularly effective. Indeed, it can be so effective as to enable the construction of extremely compact, practically useful hardware assists. Such compact hardware assists, which derive their power from the workstation and their input/output signals from its backplane, are known as accelerators. While they may or may not be dedicated to their workstation hosts, they rarely serve more than one user at a time.

Where the task, the algorithm, or the technology preclude a compact hardware assist, the economics of scale favor the construction of a high-performance, application-specific system capable of serving multiple users simultaneously. Such systems are referred to as application-specific servers.

Cost Effectiveness

To measure the cost effectiveness of application-specific hardware, one requires a unit of throughput. In a particular non-numeric application; namely, logic simulation, this unit is the event per second. Precise as it sounds, this unit requires considerable qualification, especially if one intends to make benchmark comparisons. Undaunted, I have attempted to extract from the literature of several vendors, the salient parameters of their logic simulation-specific hardware. Dividing the throughput by the cost of the equipment, servers would appear to be 100 to 1000 times as cost effective as workstations - or, for that matter, as the popular supermini. A recently developed accelerator, burdened with the cost of a workstation host is 100 times as cost effective, and quite adequate to support a single user-designer. Both products have been implemented without the benefit of custom LSI. Clearly, the potential of application-specific hardware in non-numeric applications is dramatic.

In numeric applications, such as circuit simulation, the cost effectiveness can often be approximated by the cost per MFLOP (million floating point operations per second). It is claimed that a popular array processor can execute SPICE five times faster than the popular supermini with floating point accelerator. Inasmuch as these two machines differ in their MFLOP rating by a factor of 40, one must be careful in correlating throughput with MFLOP's. Still, it is a valid indicator.

MFLOP's have long been precious. Until recently, the cheapest MFLOP in the world cost $20,000 ready-to-serve. Today, high-performance VLSI devices are coming into the market with the potential to drastically alter the economics in numeric applications. With these devices, accelerators of 10 MFLOP's and servers of 1000 MFLOP's can be constructed to assist applications such as circuit simulation, at a fraction of the cost of today's computing resources. Arithmetic bottlenecks will continue to be more costly to remove than non-numeric bottlenecks (after all, a MFLOP is the most costly MIP), but complexity of the respective solutions is converging rapidly.

Outlook

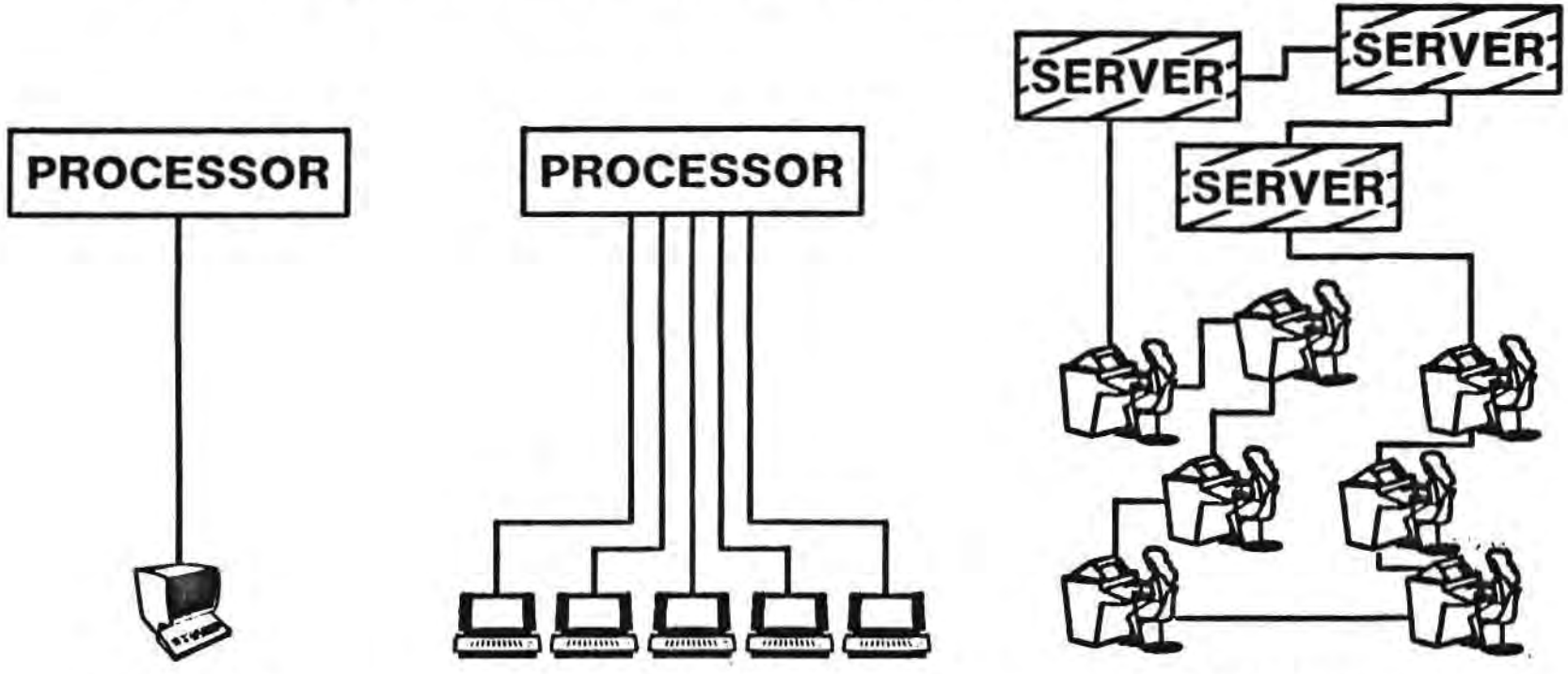
In surveying the prospects for application-specific hardware, one must examine the driving forces, technological and commercial. It goes without saying that the increasing availability of highly-integrated, high-performance digital circuitry is a major driving force, with the potential to dominate. Today, however, the prime technological enabler is the application insight developed and honed by the turnkey system companies. Driven by the immense market opportunity, competition among these companies is fierce. To grow their businesses, these suppliers must (1) justify their systems against the broadest possible ensemble of application-related tasks, and (2) position themselves to capture as much of the customer's budget for computing as possible.

Against this background, the haze begins to melt. Clearly, there are many unresolved computational bottlenecks. With increasing availability of VLSI to resolve these bottlenecks, and the increasingly stiff penalties assessed against those who fail to respond to the needs of the marketplace, it is likely that application-specific hardware will proliferate. (Who will resist? Certainly not the mainframe makers.) Moreover, VLSI and competition will force marketplace pricing. Finally, the accelerator - favored by existing (workstation) companies - will present formidable competition to the server.

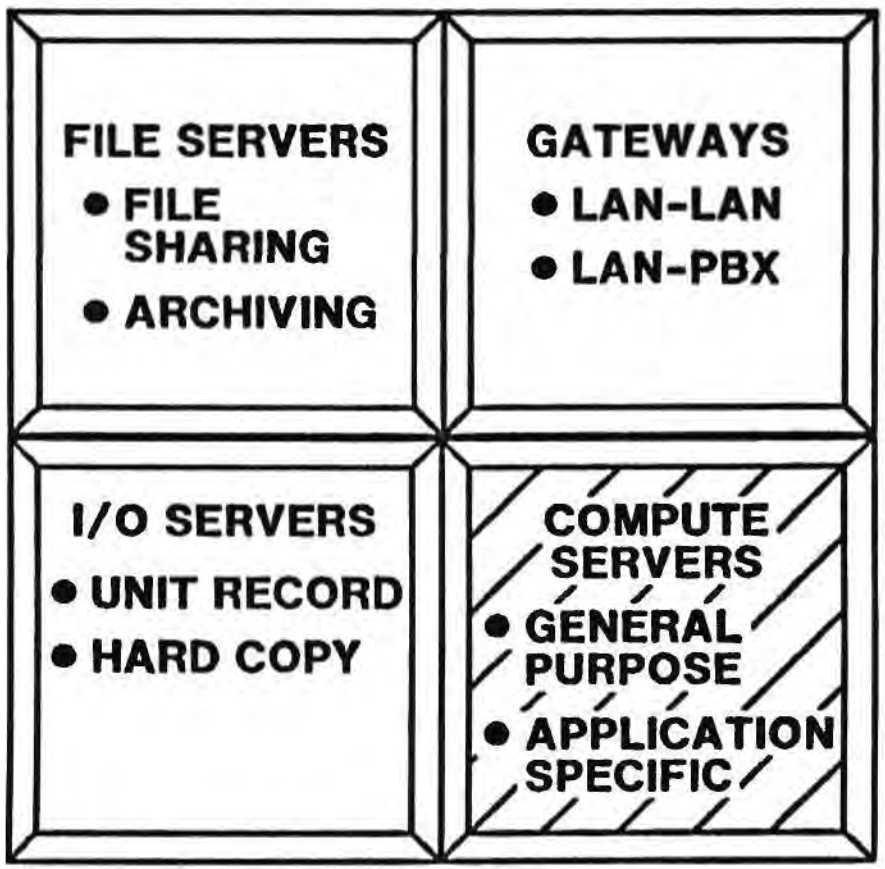
Summary

The technological evolution which has made it possible to distribute computing to the point of need will continue to undermine the role of the general-purpose computational server, as it enables powerful 32-bit microprocessors to broaden the application of workstations, and powerful application-specific hardware to augment the capabilities of workstations in the computationally-intensive applications. Application-specific hardware, in particular, cuts two ways. First, by offering substantially greater economy than general-purpose computers, application-specific hardware is bound to erode the mainframe share of the engineering computing budget. Second, by covering effectively for the limitations of workstations in computationally-intensive applications, application-specific hardware will facilitate the growth of distributed computing.

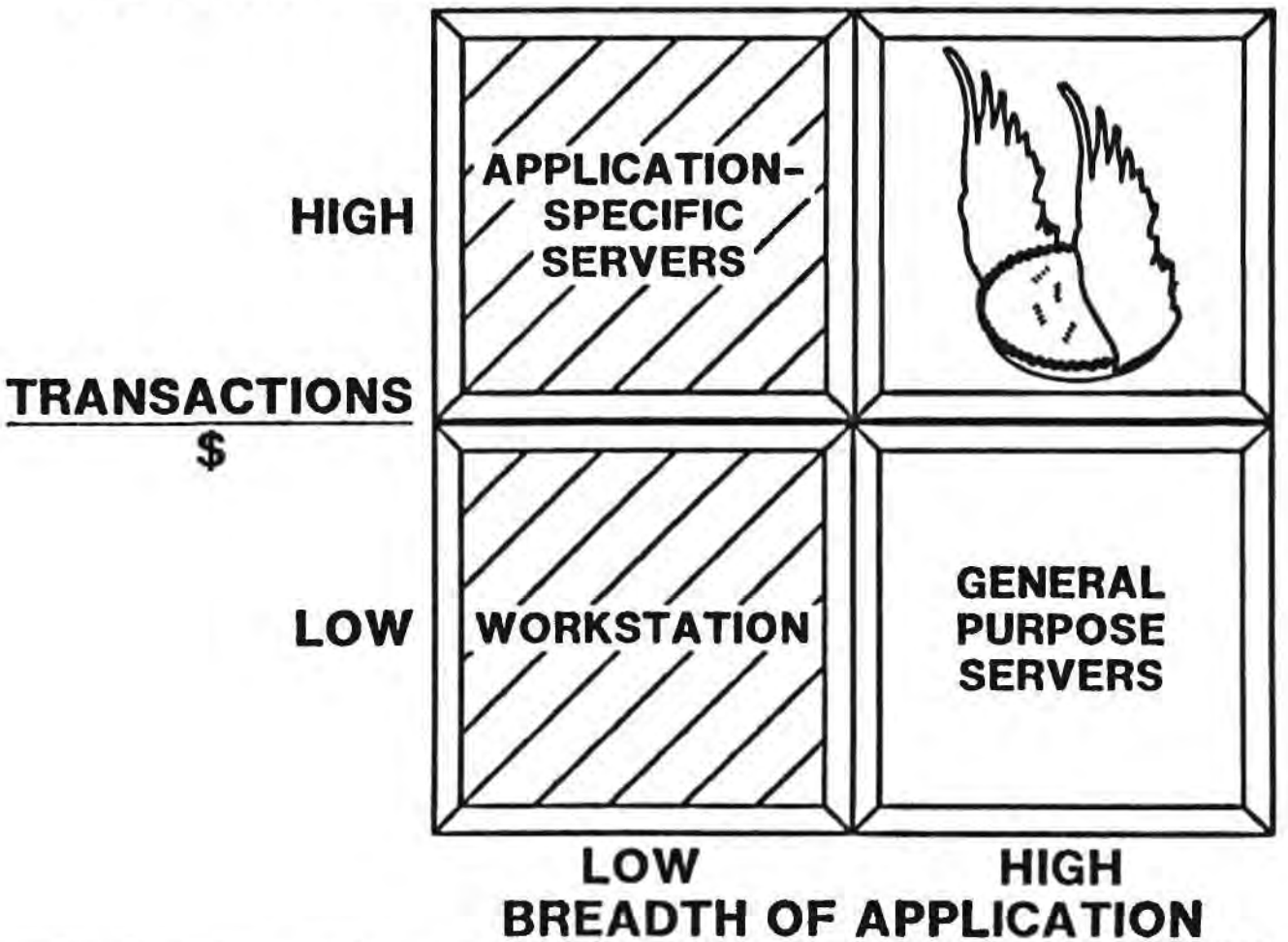
EVOLUTION OF DISTRIBUTED COMPUTING



CLASSES OF SERVERS



TWO TYPES OF COMPUTE SERVERS



WEITEK

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COMPUTATIONALLY INTENSIVE APPLICATIONS

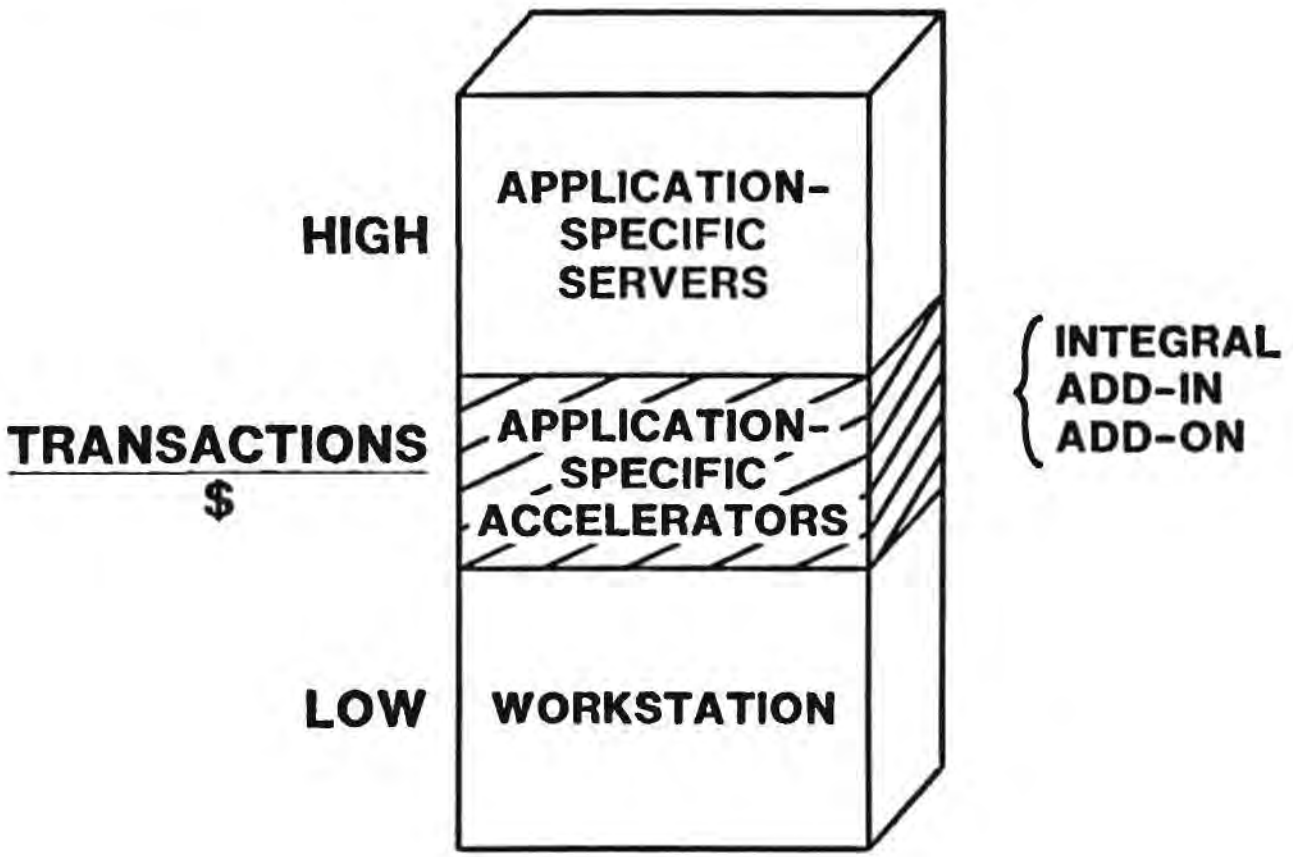
NUMERIC

- CIRCUIT SIMULATION
- SOLID MODELING
- STRUCTURAL ANALYSIS
- IMAGE PROCESSING...

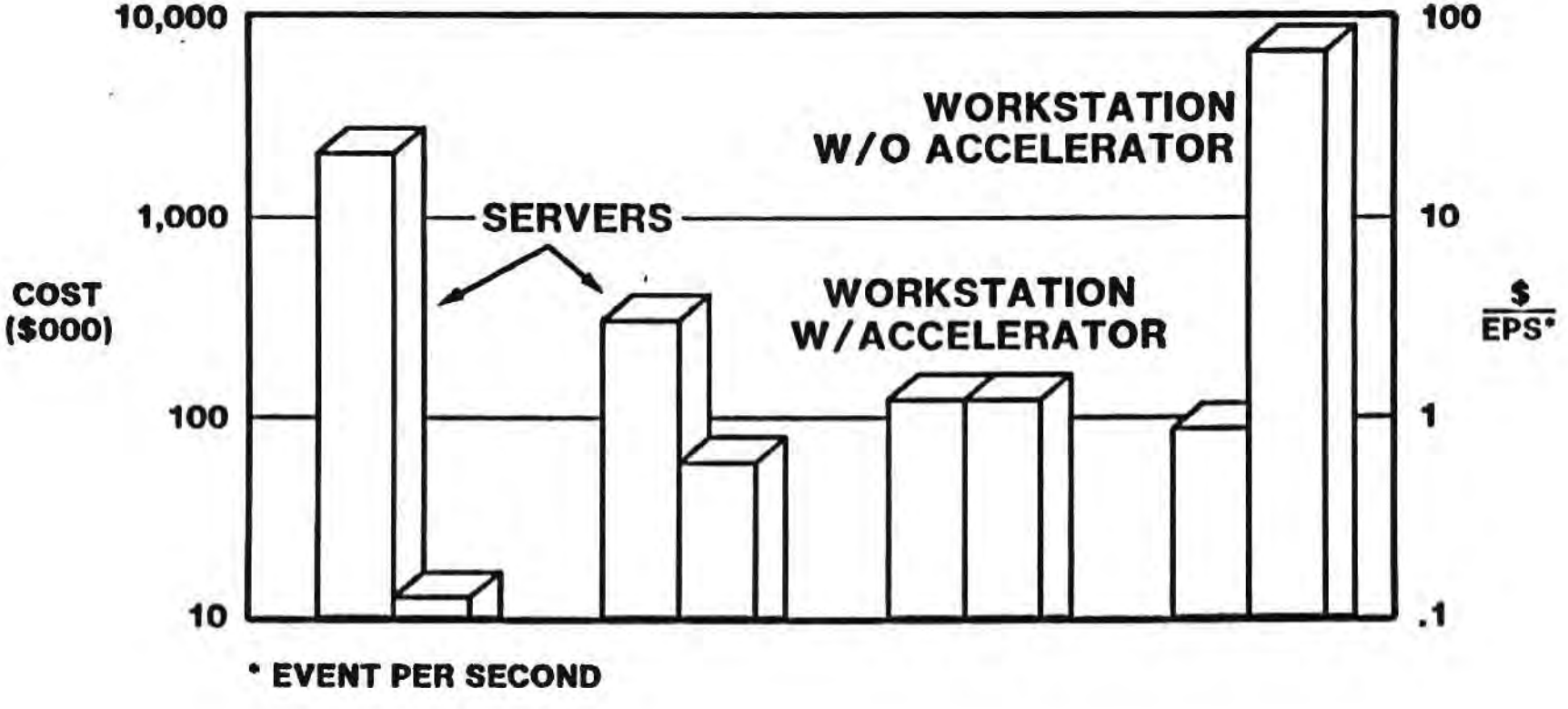
NON-NUMERIC

- LOGIC SIMULATION
- PLACEMENT/ROUTING
- DESIGN RULE CHECKING
- LAYOUT VERIFICATION...

THE SERVER/ACCELERATOR DICHOTOMY



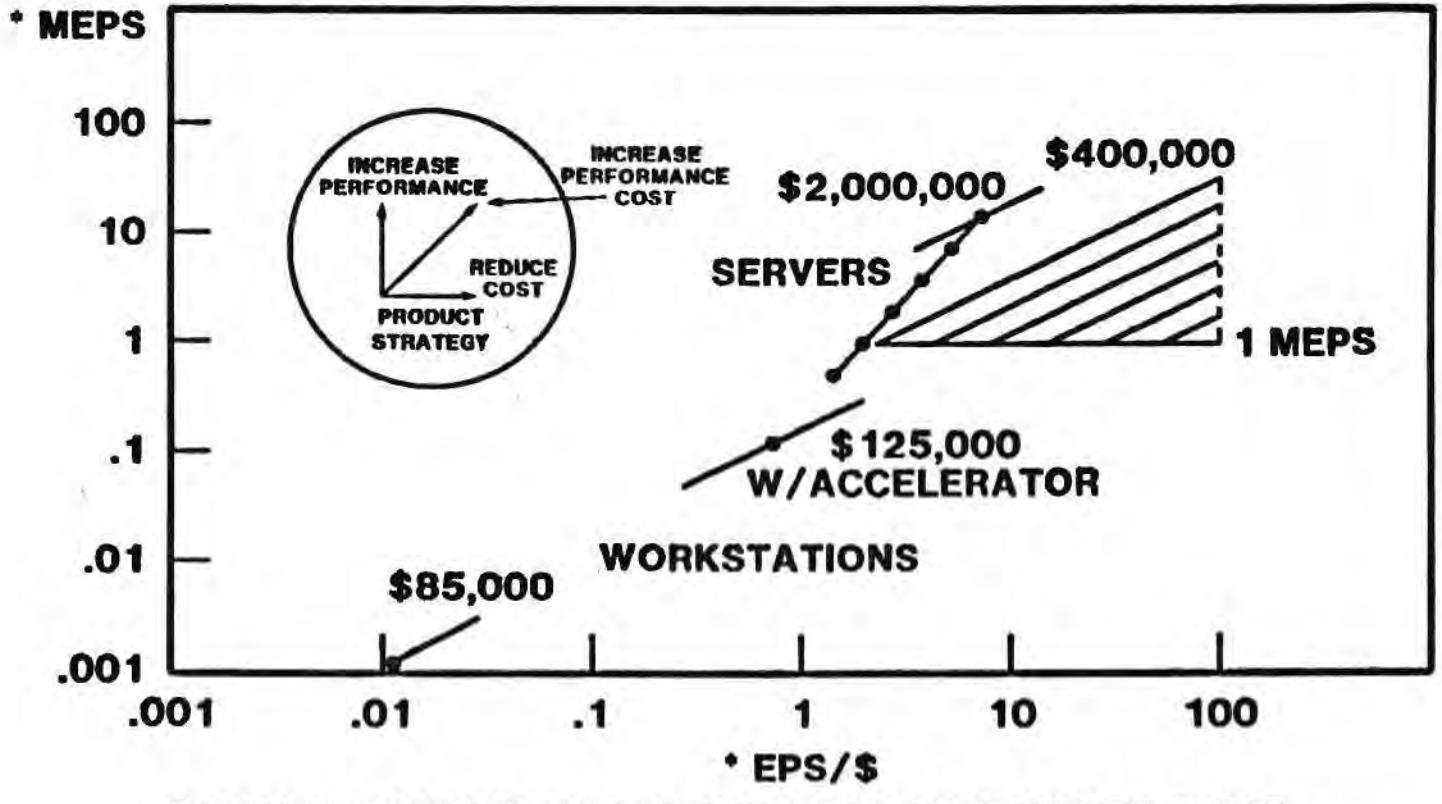
ECONOMICS OF APPLICATION-SPECIFIC SERVERS
(A NON-NUMERIC APPLICATION)



SERVERS VS WORKSTATIONS
(A NON-NUMERIC APPLICATION)

UNIT	FIGURE OF MERIT	
	$	$/EPS
WORKSTATION	1.0	150
W/ACCELERATOR	1.5	2
SERVER ($300K)	3.5	1

NON-NUMERIC SERVERS/ACCELERATORS
(EXAMPLE: LOGIC SIMULATION)



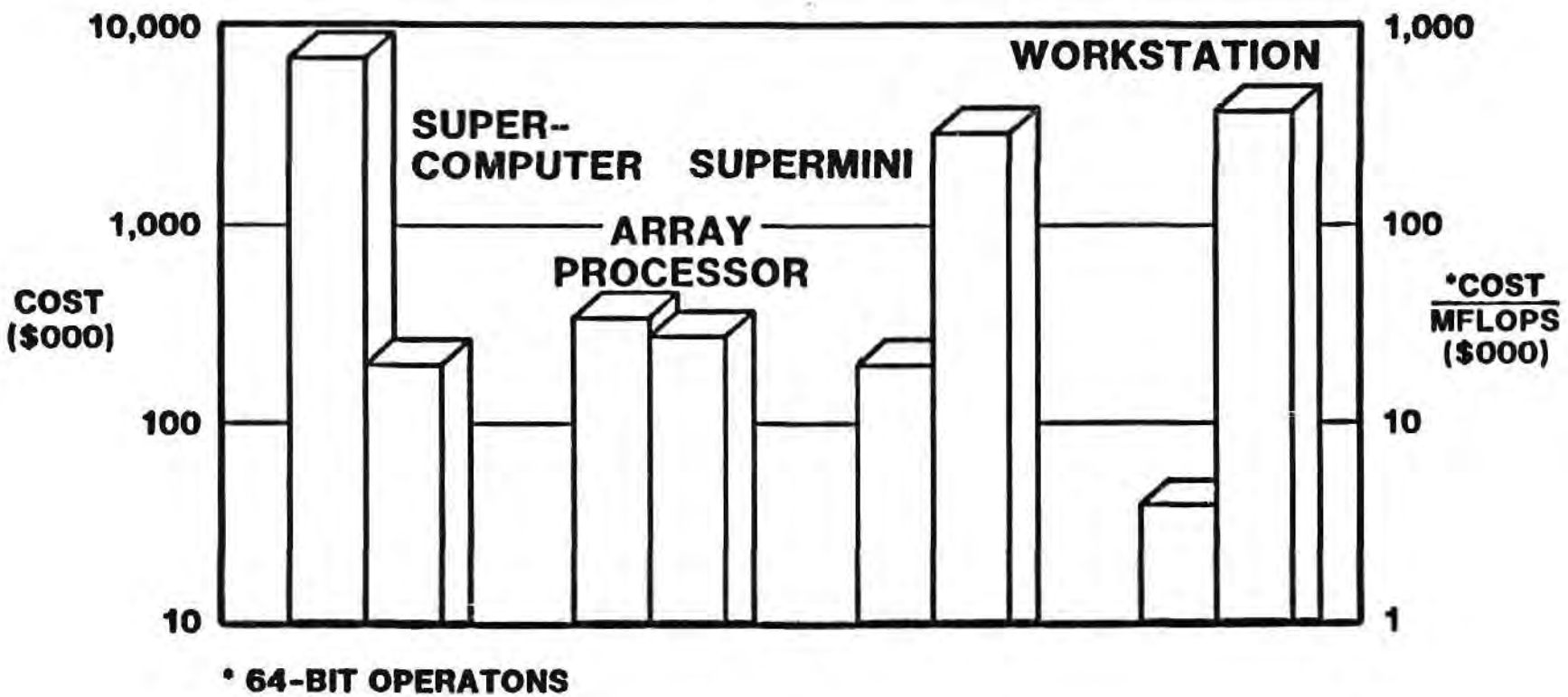
* SERVER COMPUTATIONS DERIVED FROM SERVER PRICE; ACCELERATOR COMPUTATION INCLUDES PRICE OF WORKSTATION

COMPUTATIONALLY INTENSIVE APPLICATIONS

NUMERIC

- CIRCUIT SIMULATION
- SOLID MODELING
- STRUCTURAL ANALYSIS
- IMAGE PROCESSING...

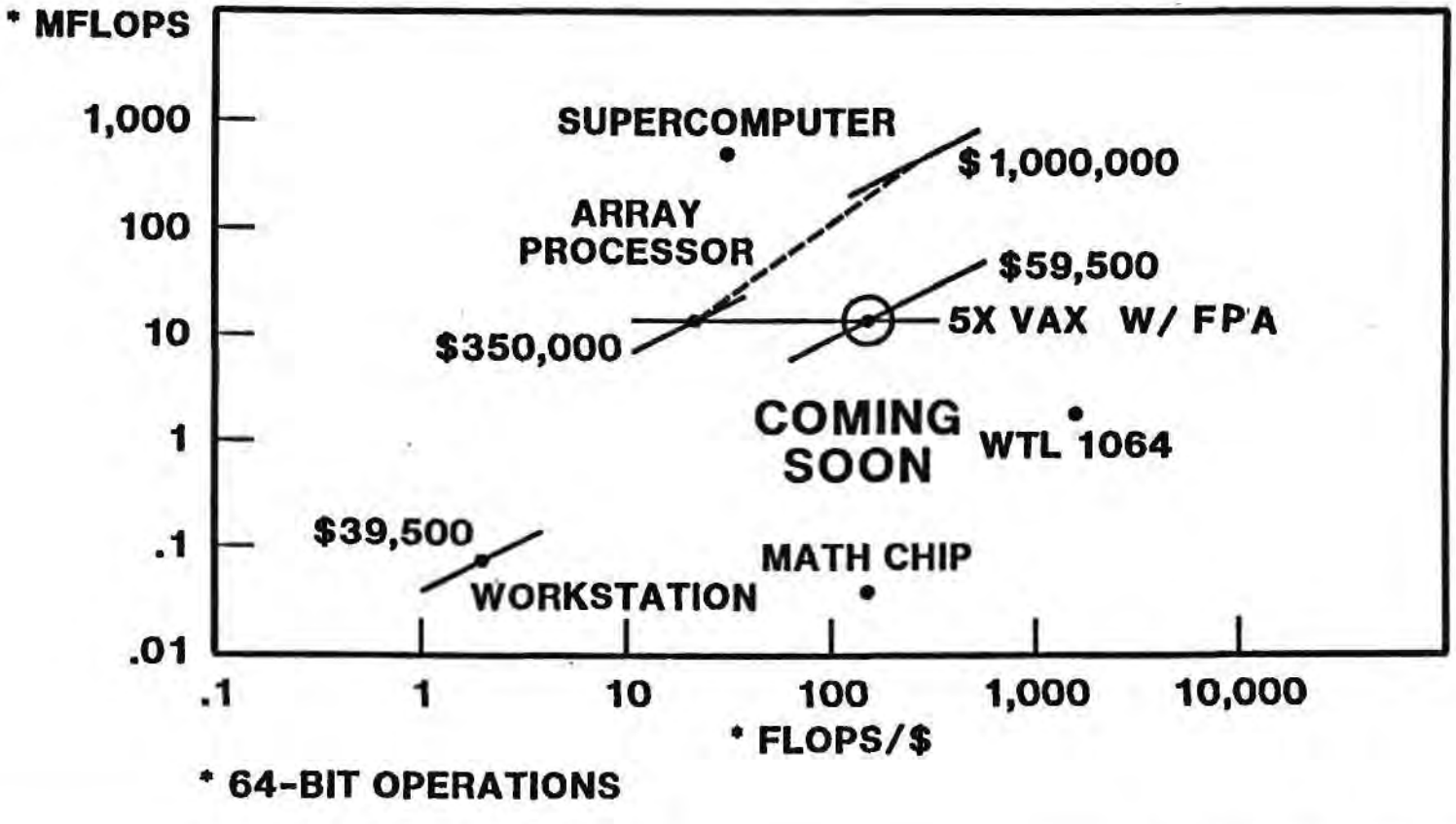
ECONOMICS OF APPLICATION-SPECIFIC SERVERS
(NUMERIC APPLICATIONS)



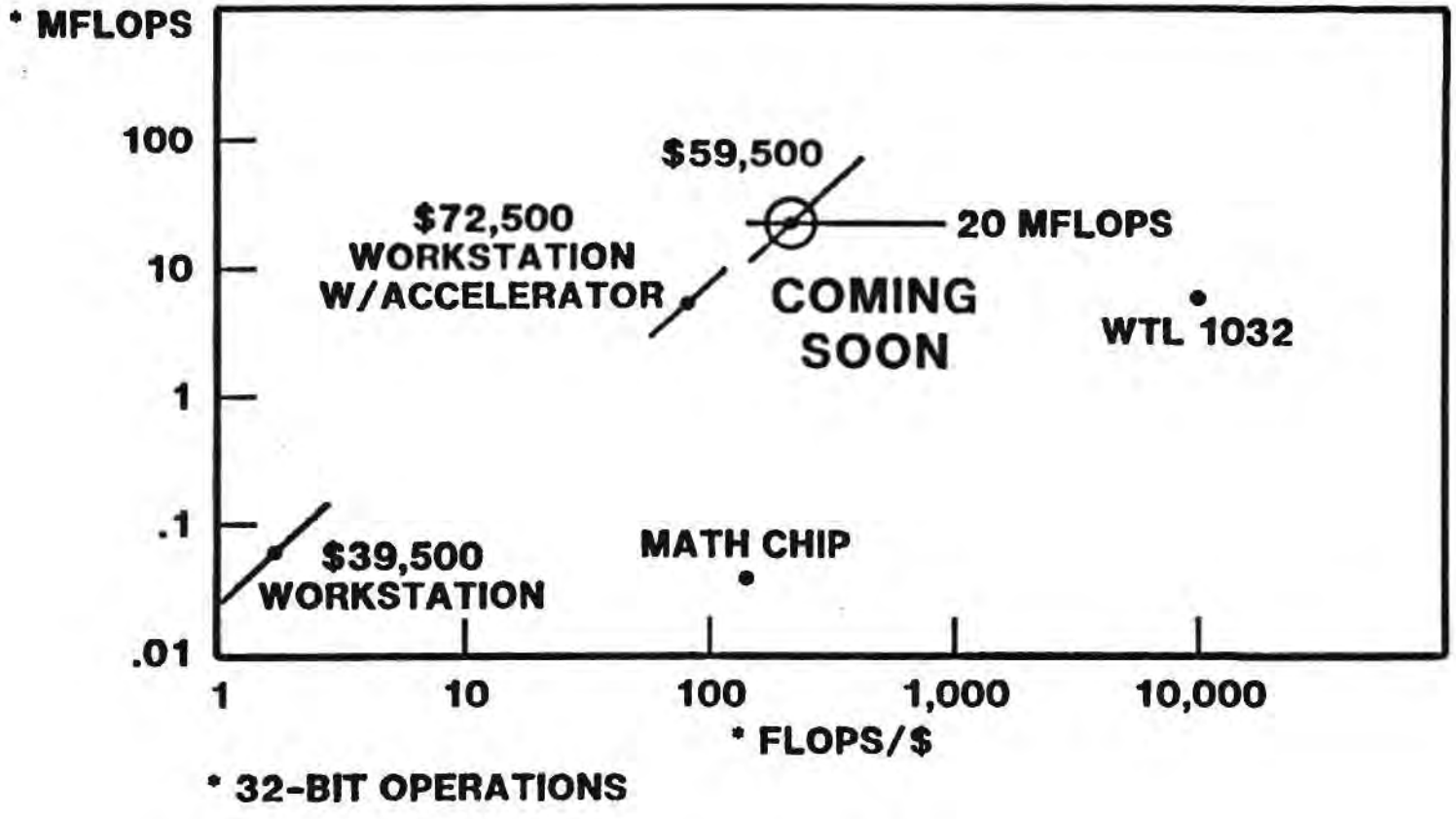
SERVERS VS WORKSTATIONS
(NUMERIC APPLICATIONS)

UNIT	FIGURE OF MERIT	
	$	$/MFLOPS
WORKSTATION	1	15
ACCELERATOR	?	?
ARRAY PROCESSOR	10	1

NUMERIC SERVERS/ACCELERATORS
(EXAMPLE: CIRCUIT SIMULATION)



NUMERIC SERVERS/ACCELERATORS
(EXAMPLE: KINEMATICS; SOLID MODELING)



IMPACT OF APPLICATION SPECIFIC HARDWARE

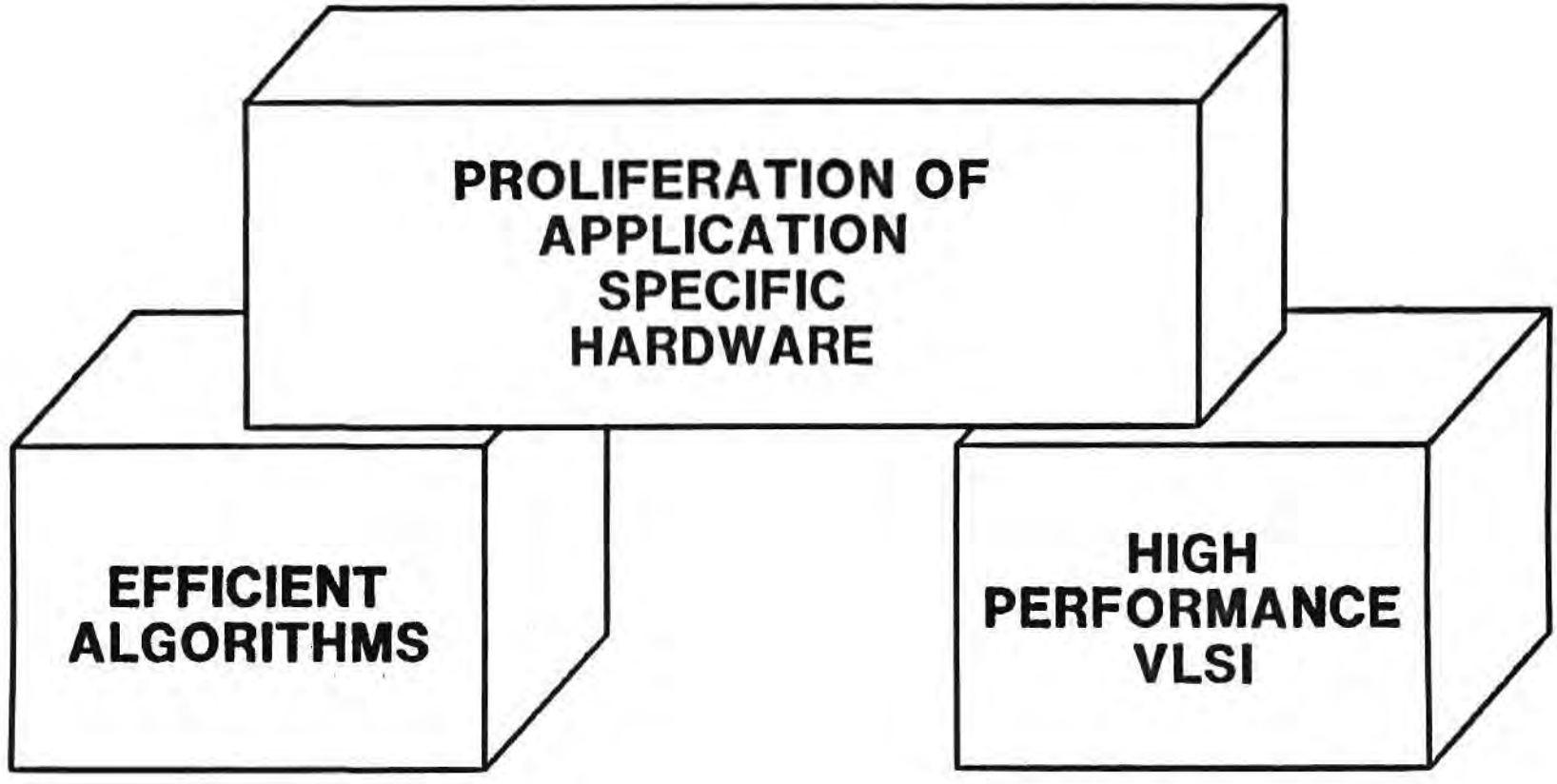
NON-NUMERIC APPLICATIONS

- IMPACT DRAMATIC, EVEN NOW!
- 100X TO 1000X IMPROVEMENT IN TRANSACTIONS PER DOLLAR.
- SERVERS SUPPORT LARGE USER NETWORKS OF LOW COST WORKSTATIONS.
- ACCELERATORS PROVIDE COMPARABLE ECONOMY.

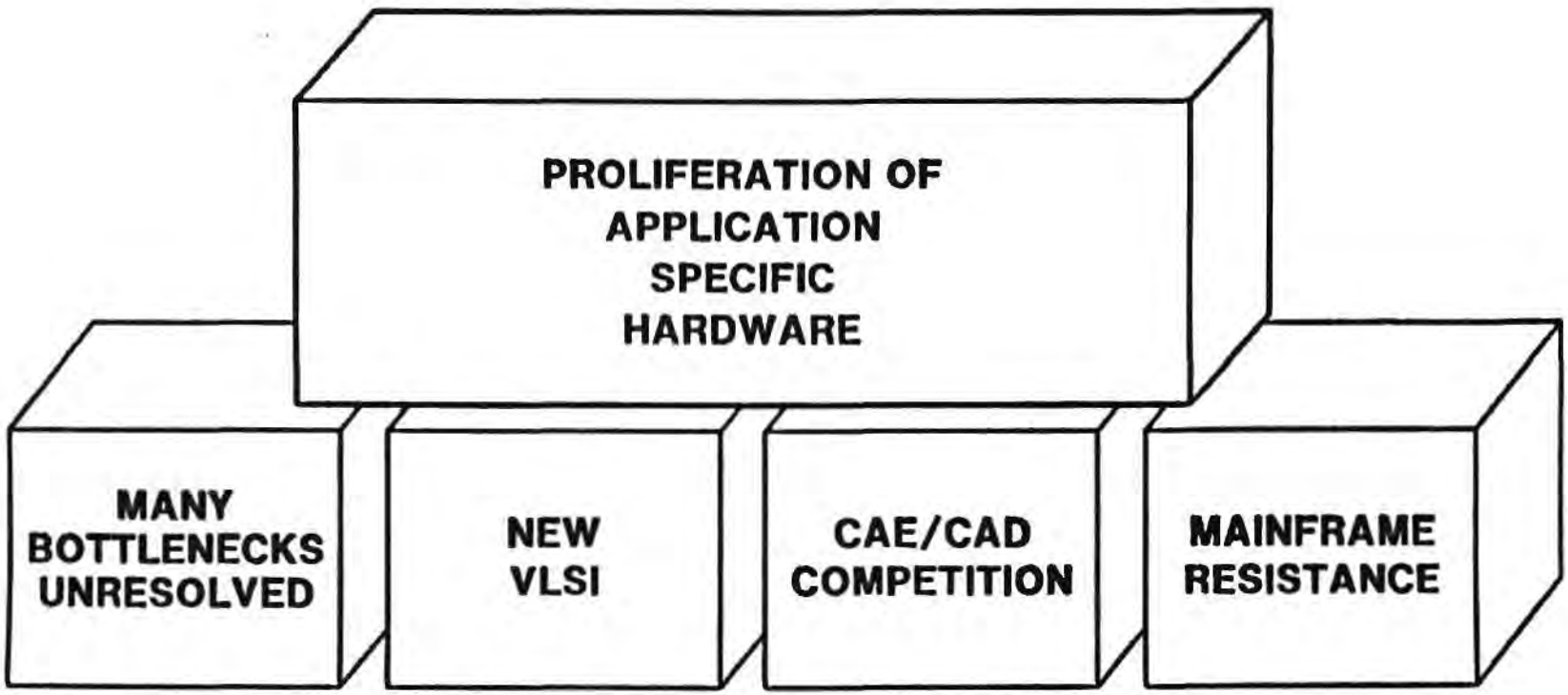
NUMERIC APPLICATIONS

- IMPACT DRAMATIC, BEGINNING IN 1985.
- 10X TO 100X IMPROVEMENT IN TRANSACTIONS PER DOLLAR.

ENABLING TECHNOLOGIES



OUTLOOK



SUMMARY

- **BY OFFERING SUBSTANTIALLY GREATER ECONOMY THAN GENERAL PURPOSE COMPUTERS, APPLICATION SPECIFIC HARDWARE WILL SURELY LIMIT THE MAINFRAME SHARE OF THE ENGINEERING COMPUTING BUDGET.**

SUMMARY

- MOREOVER, APPLICATION SPECIFIC HARDWARE
  WILL EFFECTIVELY MASK
  THE LIMITED COMPUTATIONAL ABILITIES
  OF WORKSTATIONS.
  HENCE, APPLICATION SPECIFIC HARDWARE
  WILL FACILITATE GROWTH OF DISTRIBUTED COMPUTING.

FOCUS CONFERENCE

Electronic Design Automation: The Technology Renaissance

Sponsored by the CAD/CAM Industry Service

May 10 & 11, 1984
Sunnyvale Hilton Inn
Sunnyvale, California

Nielsen Dataquest

CONFERENCE PROGRAM

THURSDAY, MAY 10

7:30 a.m. to 8:45 a.m.

Conference Registration

8:45 a.m.

Welcome and Conference Introduction

James Newcomb, Director
CAD/CAM Industry Service
Dataquest Incorporated

9:00 a.m.

EDA Industry Overview

Beth Tucker, Industry Research Manager
CAD/CAM Industry Service
Dataquest Incorporated

9:45 a.m.

What's All The Excitement About—How Can An Industry Grow So Fast?

Thomas Bruggere, President
Mentor Graphics

10:30 a.m.

Coffee Break

10:45 a.m.

Application-Specific Hardware

Jared Anderson, President
Valid Logic Systems, Inc.

11:30 a.m.

EDA Design Center Strategies

Del Mank, Vice President, Marketing and Sales
California Devices, Inc.

12:15 p.m. to 1:15 p.m.

Lunch

1:30 p.m.

Microprocessor Revolution Leads to the ASIC Evolution

Kenneth McKenzie, Associate Director
Semiconductor Industry Service
Dataquest Incorporated

2:15 p.m.

Coffee Break

2:30 p.m.

Users' Points of View—Panel Discussion

- Expectations
- Needs
- Futures
- Applications

4:30 p.m. to 6:00 p.m.

Cocktails and Hors d'Oeuvres

FRIDAY, MAY 11

8:15 a.m.

Silicon Compilers are a 1984 Technology

Phil Kaufman, President
Silicon Compilers, Inc.

9:00 a.m.

EDA is for PCB CAD Too

Bruce Holland, President
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Harvey Jones, Senior Vice President
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12:15 p.m.

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Beth Tucker, Industry Research Manager
CAD/CAM Industry Service
Dataquest Incorporated

12:30 p.m. to 1:30 p.m.

Buffet Lunch

CONFERENCE INFORMATION

HOTEL ACCOMMODATIONS

Conference attendees are responsible for making their own hotel reservations. For your convenience, the Sunnyvale Hilton Inn is holding a block of rooms for those attending the conference. To make reservations, call the Hilton directly at (408) 738-4888 and mention that you are attending the DATAQUEST Focus Conference.

TRANSPORTATION

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DATAQUEST CALLS IT EDA

THE NEED

Electronic design automation (EDA) is the CAD/CAM industry's youngest, most explosive, most dynamic segment. EDA products and systems address a broad spectrum of phases within the entire electronic product design cycle. DATAQUEST calls this segment EDA because it encompasses more than just computer-aided engineering (CAE), or applications related only to electrical engineers. In addition to logic or circuit design and simulation, EDA may also include:

- Full-custom layout
- Semicustom layout
- Printed circuit board layout
- Documentation
- Test pattern analysis

CAE products also address the needs of mechanical, civil, and architectural engineers. We believe that the EDA segment is significant enough to warrant its own name—ELECTRONIC DESIGN AUTOMATION.

THE FOCUS CONFERENCE

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The conference will explore the issues that affect EDA from the vendor's, user's, and investor's points of view. Focus Conference highlights are:

- EDA industry dynamics
- EDA market size and forecasts
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- Users' applications and expectations
- Hardware and software issues
- Product life cycles
- Design cycles
- Futures

WHO SHOULD ATTEND

Everyone should attend the Technology Renaissance Focus Conference who needs to know and understand the EDA industry and how it is changing the way electronic products are designed. This includes:

- Management
- Engineers and Product Developers
- CAD System Managers
- CAD/CAM Marketing Professionals
- Workstation Marketing Professionals
- Computer Marketing Professionals
- Venture Capitalists
- Investment Portfolio Managers
- Strategic Planners

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- Graphics
- Dedicated hardware
- Electronic design automation
- Integrated circuit CAD/CAM
- Printed circuit board CAD/CAM
- Mechanical CAD/CAM
- Architecture, engineering, and construction CAD
- Applications software
- Personal computer-based CAD/CAM systems

CONFERENCE INFORMATION

LOCATION

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Address: Sunnyvale Hilton Inn
1250 Lakeside Drive
Sunnyvale, California 94086

Telephone: (408) 738-4888

CONFERENCE FEE

The fee for the Electronic Product Design Focus Conference is:

- Each attendee who is a client of any DATAQUEST industry service $325
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The conference fee includes a conference binder with copies of the material presented at the conference, and lunches. ***Conference fees must be paid in advance.*** Checks, money orders, purchase order numbers, American Express, Mastercard, or Visa will be accepted.

REGISTRATION

To register, mail the reservation form on the tear-off card, or telephone Ms. Pam Shook at (408) 971-9000, extension 316, or Telex 171973. Space is limited, so be sure to register early.

CONFERENCE SCHEDULE

Conference registration will take place starting at 7:30 a.m. on Thursday, May 10. Thursday's program will begin at 8:45 a.m. and will conclude with a DATAQUEST-hosted cocktail party from 4:30 to 6:00 p.m. On May 11, the program will start at 8:15 a.m. and conclude after a buffet luncheon.

CANCELLATION POLICY

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San Jose, California 95131
(408) 971-9000
Telex 171973

Reply Card

☐ Please register me for the 1984 Conference. *Electronic Design Automation: The Technology Renaissance*
(Please type, print or attach business card.)

Last Name _____ First _____ M.I. ___

Title _____

Company _____

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City _____ State _____ Zip _____

Telephone ( ) _____

☐ Please send me information on DATAQUEST's CAD/CAM Industry Service

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Form of Payment:

☐ Check enclosed ☐ Money Order enclosed

☐ Purchase Order# _____

☐ Am. Express# _____ Exp. date _____

☐ Visa# _____ Exp. date _____

☐ Mastercard# _____ Exp. date _____

Signature _____

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San Jose, CA 95131-9980

FOCUS CONFERENCE

Electronic Design Automation: The Technology Renaissance

Sponsored by the CAD/CAM Industry Service

May 10 & 11, 1984
Sunnyvale Hilton Inn
Sunnyvale, California

Nielsen Dataquest

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THURSDAY, MAY 10

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8:45 a.m.

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9:00 a.m.

EDA Industry Overview

Beth Tucker, Industry Research Manager
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9:45 a.m.

What's All The Excitement About—How Can An Industry Grow So Fast?

Thomas Bruggere, President
Mentor Graphics

10:30 a.m.

Coffee Break

10:45 a.m.

Application-Specific Hardware

Jared Anderson, President
Valid Logic Systems, Inc.

11:30 a.m.

EDA Design Center Strategies

Del Mank, Vice President, Marketing and Sales
California Devices, Inc.

12:15 p.m. to 1:15 p.m.

Lunch

1:30 p.m.

Microprocessor Revolution Leads to the ASIC Evolution

Kenneth McKenzie, Associate Director
Semiconductor Industry Service
Dataquest Incorporated

2:15 p.m.

Coffee Break

2:30 p.m.

Users' Points of View—Panel Discussion

- Expectations
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Telex 171973

Reply Card

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(Please type, print or attach business card.)

Last Name _____ First _____ M.I. ___

Title _____

Company _____

Street _____

City _____ State _____ Zip _____

Telephone ( ) _____

☐ Please send me information on DATAQUEST's CAD/CAM Industry Service.

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☐ $325 DATAQUEST client attendee

☐ $395 individual or nonclient company attendee

Form of Payment:

☐ Check enclosed ☐ Money Order enclosed

☐ Purchase Order# _____

☐ Am. Express# _____ Exp. date _____

☐ Visa# _____ Exp. date _____

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Focus Conference

Electronic Design Automation: The Technology Renaissance

Sponsored by the
CAD/CAM Industry Service

May 10 and 11, 1984
Sunnyvale Hilton Inn
Sunnyvale, California

1290 Ridder Park Drive
San Jose, California 95131
(408) 971-9000
Telex: 171973

Sales/Service offices:

UNITED KINGDOM
DATAQUEST UK Limited
144/146 New Bond Street
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United Kingdom
(01) 409-1427
Telex: 266195

GERMANY
DATAQUEST GmbH
In der Schneithohl 17
D-6242 Kronberg 2
West Germany
(06173) 6921
Telex: 410939

FRANCE
DATAQUEST SARL
41, rue Ybry
92522 Neuilly-sur-Seine Cedex
France
(01) 758-1240
Telex: 630842

JAPAN
DATAQUEST Japan, Ltd.
Azabu Heights, Suite 410
1-5-10, Roppongi, Minato-ku
Tokyo 106, Japan
(03) 582-1441
Telex: J32768

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FOCUS CONFERENCE AGENDA

Electronic Design Automation: The Technology Renaissance

Sponsored by the CAD/CAM Industry Service

May 10 and 11, 1984

Sunnyvale Hilton Inn, Sunnyvale, California

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9:00 a.m.	**EDA Industry Overview** Beth Tucker, Industry Research Manager CAD/CAM Industry Service Dataquest Incorporated
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10:30 a.m.	Coffee Break
10:45 a.m.	**Application-Specific Hardware** Jared Anderson, President Valid Logic Systems, Inc.
11:30 a.m.	**Design Interface Strategies** Kent Jaeger, Manager, Design Interface California Devices, Inc.
12:15 p.m. to 1:15 p.m.	Lunch
1:30 p.m.	**The Synergy of ASICs and EDA** Kenneth McKenzie, Associate Director Semiconductor Industry Service Dataquest Incorporated
2:15 p.m.	Coffee Break
2:30 p.m.	**Users' Points of View—Panel Discussion** • Expectations • Needs • Futures • Applications
4:30 p.m. to 6:00 p.m.	Cocktails and Hors d'Oeuvres

FRIDAY, May 11

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10:45 a.m.	**The EDA Industry: Unique Requirements Mandate Unique Support** Thomas Binder, Vice President Marketing and Sales Silvar-Lisco
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Nielsen Dataquest

CAD/CAM FOCUS CONFERENCE EVALUATION QUESTIONNAIRE
Sunnyvale, California — May 10 and 11, 1984

Thank you for attending our CAD/CAM Industry Focus Conference. Would you please assist us in planning our next Focus Conference by completing and returning this questionnaire?

1. Please rate each presentation on a scale of 1 to 10 (where 10 is highest in terms of your approval):

	CONTENT (1 to 10)	DELIVERY (1 to 10)	COMMENTS (Use reverse side if necessary)
Tucker, *EDA Industry Overview*	_____	_____	_____
Langler, *What's All The Excitement About*	_____	_____	_____
Anderson, *Application-Specific Hardware*	_____	_____	_____
Jaeger, *Design Interface Strategies*	_____	_____	_____
McKenzie, *The Synergy of ASICs and EDA*	_____	_____	_____
Panel Discussion, *Users' Points of View*	_____	_____	_____
Kaufman, *Integrated Systems Technology*	_____	_____	_____
Feltman, *EDA Is for PCB CAD Too*	_____	_____	_____
Heidrich, *The World According to Venture Capital*	_____	_____	_____
Binder, *The EDA Industry*	_____	_____	_____
Jones, *Coping with a Changing Industry*	_____	_____	_____

2. How would you rate the conference facilities (1 to 10)?

   Location _____ Guest Rooms _____ Meals _____ Meeting Rooms _____ Recreational Facilities _____

3. How would you rate the service quality and staff attitude (1 to 10)?

   The hotel staff _____ DATAQUEST staff _____

4. What did you like most about the Focus Conference? _____

   _____

5. What did you like least about the Focus Conference? _____

   _____

6. Suggestions for improving the Focus Conference: _____

   _____

(over)

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7. Topics that would be of interest to you for the next Focus Conference: _____

_____

8. Do you prefer ☐ longer, ☐ shorter, or ☐ the same length conference?

9. Do you prefer ☐ more, ☐ less, or ☐ the same amount of free time?

10. Your primary interest in the CAD/CAM Industry is as a: ☐ Manufacturer

☐ Service Vendor ☐ User ☐ Financial Analyst ☐ Other_____

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Name and Company (optional)

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Nielsen Dataquest

CAD/CAM Focus Conference

May 10 and 11, 1984

Sunnyvale, California

List of Attendees

Bob Anderson	GenRad, Inc.
Jared Anderson	Valid Logic Systems, Inc.
Lloyd Anderson	Dataproducts
Phil Arana	Calma Company
Joseph Augustino	HHB-Softron
Raj Badhwar	Calma Company
Alan Bagley	Hewlett-Packard
David L. Bailey	Cericor, Inc.
Hal Barbaur	GenRad
Andy Barnes	DATAQUEST Incorporated
Bill Barret	Caddrx
Tom Binder	Silvar-Lisco
Bill Bowman	Hewlett-Packard
Darko Brodarac	Robert Bosch GMBH Reutlingen
Sharlene Burden	DATAQUEST Incorporated
Dave Burdick	DATAQUEST, Incoporated
Charles Bures	Data General Corp.
Bob Burkhardt	Advance Micro Devices, Inc.
Gil Burns	Teradyne, Inc.
Donald Butler	General Instrument Corp.

Nelson Bye	Data General Corp.
Frank Calabretta	Holt, Inc.
Steve Chadima	Regis McKenna
Wade Chanz	E.R.S.O.
Wei-tau Chiang	Intel Corp.
Art Collmeyer	Weitek
Laura Conigliaro	Prudential Bache
Mike Connell	LSI Logic Corp.
Jim Cooper	Tektronix
Don Corson	Hewlett-Packard
John Crist	Tektronix
Dave Crockett	DATAQUEST, Incorporated
P. Csao	E.R.S.O.
Tennyson Csen	E.R.S.O.
Ang Danna	Arthur Young & Company
Sam Daram	Calma Company
Ugo De Riu	Olivetti System Development Div.
John DiGirolamo	GenRad, Inc.
Bob Draeger	Tektronix
Francois Durif	GenRad, Inc.
Bob Duyn	VLSI Techology, Inc.
Mary Jane Elmore	Institutional Investment Partners
Doug Fairbeirn	VLSI Technology, Inc.
Daniel Fan	Hewlett-Packard
Buck Feltman	Cadnetix, Inc.

Ralph Finley	DATAQUEST Incorporated
Suzanne Finocchio	Bank of America
Kamran Firooz	Hewlett-Packard Manufacturing Test Div.
David Flaningam	Test Systems Strategies, Inc.
Frank Florence	DATAQUEST Incorporated
Rick Fluegel	Matrix Partners
Jim Fogle	Teradyne, Inc.
Curt Francis	Advanced Micro Devices, Inc.
Brian Gardiner	Calma Company
Jim Gay	Perq Systems Corp.
Majid Ghafghaichi	Data General Corp.
John Gilbert	Cigna Investment Management
Tom Gnuse	Prime Capital Management
Chris Goldstein	Applicon
Stan Graham	Modern Electrosystems, Inc.
Roberto Grasso	Ing. C. Olivetti & C., SPA
W. RobertGreer	Automated Systems Inc.
Horst Gschwendtner	Robert Bosch GMBH
Dave Gullickson	Versatec
Guy Haas	Computervision Corp.
Kevin Hall	Calma Company
James Harrison	Adler & Company
Gib Hattery	CAE Systems, Inc.
Ron Hayman	Motorola, Inc.

Grant Heidrich	Mayfield Fund
Henry S. Hofmann	Hewlett-Packard Technology Center
William G. Holt	Holt Inc.
Jeff Hotchkiss	Teradyne, Inc.
Mike W. Hu	Televideo
Paul Huber	Megatek Corp.
Russel Huber	Computervision Corp.
Claudia Huntington	Capital Research
J. E. Iwerson	Bell Labs
John Jackson	DATAQUEST, Incoporated
Debra Jacob	DATAQUEST, Incoporated
Kent Jaeger	California Devices, Inc.
Jan Janse	Siemens Research Labs
Bob J. Jenkins	Motorola, Inc.
Richard Jennings	VIA Systems, Inc.
Alan Jepsen	Bank of America
Harvey Jones	Daisy Systems Corp.
Robert Joseph	Phillips Test & Measuring Instruments
Bill Kaiser	Apollo Computer
Thanasis Kalekos	Versatec
Ram Kasargod	IDS
Phillip A. Kaufman	Slicon Compilers, Inc.
Dave Kaverman	Hewlett-Packard
Norman F. Kelly	Altos Computer Systems
Bill Knox	CAE Systems Inc.

Mike Knudsen	CalComp
Michael Kretsch	Exlsi
Rob Kuhling	Calma Company
Gerard Langler	Mentor Graphics Corp.
Wendy Ledamun	DATAQUEST, Incoporated
Frank Lee	Monolithic Memories
Kelly Leininger	DATAQUEST, Incoporated
Carol Lemlein	Teradyne, Inc.
Robert Leurz	Eastman Kodak Company
Van Lewing	Calma Company
Rhonda Y. Lindsey	CADAM Inc.
Shiminz Lins	E.R.S.O.
Ed Locke	United Technologies MOSTEK
Jim Long	Fujitsu Microelectronics
Bob Lorentzen	Zymos
Peter Lowell	Modern Electrosystems, Inc.
Francis T. Lynch	Valid Logic Systems
R. Van Maas	Philips
Mark Maltese	Versatec
Bob Martin	Tektronix
Edie Mata	Fujitsu Microelectronics
Roland Mattison	VIA Systems, Inc.
Samuel F. McKay	Ventech Partners
Ken McKenzie	DATAQUEST Incorporated
Daniel C. McNiell	Gould, Inc.

Robert Mclellan	Bell Northern Research
David H. Miller	Applicon
Linda Miller	InterWest Partners
Richard Mirabella	Phoenix Data Systems
Philip Monego	Paragon Technology Corp.
Bob Moore	Hewlett-Packard
Eric Mudama	GenRad, Inc.
Carolyn Mullery	Calma Company
Barrie Murray-Upton	Racal-Redac Limited
Karl Nakamura	Grid Systems
John Nam	Modern Electrosystems, Inc.
Richard Nedbal	Personal Cad Systems
Jim Newcomb	DATAQUEST, Incorporated
Dave Niehaus	Calma Company
Jack Nilsson	Hewlett-Packard
Earl North	Circuit Tools, Inc.
John O'Brien	Teradyne, Inc.
Elizabeth Obershaw	Hewlett-Packard
Dewitt Ong	Intel Corp.
Alan Oppeinheimer	Apollo Computer
Han Park	Qume Corp.
Dennis Patton	Ridge Computers
Nikola Pavicic	Modern Electrosystems, Inc.
Evelyn Peairs	Calma Company
Jeff Pepper	Perq Systems

Richard Perry	LSI Logic Corp.
Rich Peters	CalComp
Jewel Peyton	DATAQUEST, Incoporated
Ronald J. Piziali	Arthur Young & Company
Katy Plumb	First Interstate Bank of California
Jay Popper	Standard Microsystems Corp.
Roy Prasad	Personal Cad Systems
Andy Prophet	DATAQUEST, Incoporated
Jamshed Qamar	OKI Semiconductors
F. Ramsay	Ferranti Electronics
Karen Regnante	Mosaic Technology
Douglas Ritchie	National Semiconductor
Carlo Ronca	Olivetti System Development Div.
Frank Sammann	DATAQUEST Incorporated
Mary Ellen Saxby	DATAQUEST, Incoporated
Katherine Schapiro	Harris Bretall
Cesare Segre	Ing. C. Olivetti and C., SPA
C. Seih	E.R.S.O.
John Sheehan	Intel Corp.
Steve Shively	International Microcircuits, Inc.
Pam Shook	DATAQUEST, Incoporated
Chester Silvestri	Megatest
Mike Sisavic	Metheus Corp.
G. Skorup	South African Micorelectronics Systems
Joseph Sliwkowski	Telesis Systems Corp.

William Smit	University of Pretoria
Jack Spigarelli	Cericor, Inc.
Rich Stamm	Data General Corp.
J. Stevenson	Philips
Gary Stump	Tektronix
Leslie Swanson	Computervision Corp.
Tom Teeters	Calma Company
Carol Tegnell	Scientific Calculations, Inc.
Robert S. Tepper	A T & T Bell Laboratories
Ben Thomas	Calma Company
Mel Thompson	DATAQUEST, Incoporated
Rick Timmons	Wyle Labs
Paul R. Topping	McDonnell Dougals Automation (McAuto)
Beth Tucker	DATAQUEST, Incorporated
Steve Vaughn	IBM
Dave Vogte	Teradyne, Inc.
Kris Vorm	Calma Company
Fred Wagner	IBM
Martin Walker	Analog Design Technology
Irving Weiman	R&D Funding Corp. Pru-Bache
Michael Weisberg	Prudential Bache
Patrick Welch	Hewlett-Packard
Jerry Werner	VLSI Design Magazine
Gary Westbrook	Calma Company

David Wharton	GenRad, Inc.
Alan Winslow	Tektronix
Larry Yamada	Calma Company

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CAD/CAM Industry Conference

May 10-11, 1984

Sunnyvale, California

Final List of Attendees

Scott Alan	Gould Electronics
Bob Anderson	GenRad, Inc.
Colleen Anderson	Valid Logic Systems, Inc.
Jared Anderson	Valid Logic Systems, Inc.
Lloyd Anderson	Dataproducts
Phil Arana	Calma Company
Joseph Augustino	HHB-Softron
Rajiv Badhwir	Calma Company
David L. Bailey	Cericor, Inc.
Hal Barbaur	GenRad
Andy Barnes	DATAQUEST Incorporated
Bill Barrett	Caddrx
Tom Binder	Silvar-Lisco
Bill Bowman	Hewlett-Packard
Darko Brodarac	Robert Bosch GMBH Reutlingen
Sharlene Burden	DATAQUEST Incorporated
Dave Burdick	DATAQUEST, Incoporated
Charles Bures	Data General Corp.
Bob Burkhardt	Advance Micro Devices, Inc.

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Gil Burns	Teradyne, Inc.
Donald Butler	General Instrument Corp.
Nelson Bye	Data General Corp.
Frank Calabretta	Holt, Inc.
Xaviar Candia	Calma Company
Wade Chang	E.R.S.O.
Tennyson Chen	E.R.S.O.
Wei-tau Chiang	Intel Corp.
Art Collmeyer	Weitek
Laura Conigliaro	Prudential Bache
Mike Connell	LSI Logic Corp.
Jim Cooper	Tektronix
Jan A. Cornish	Versatec
Don Corson	Hewlett-Packard
John Crist	Tektronix
Ang Danna	Arthur Young & Company
Sam Daram	Calma Company
Ugo De Riu	Olivetti Systems
Chuck Decker	Electro Technology Industries, Inc.
Bob Draeger	Tektronix
Francois Durif	GenRad, Inc.
Dennis Elkins	NCA Corp.
Mary Jane Elmore	Institutional Investment Partners
William Escudero	Televideo

Daniel Pan	Hewlett-Packard
George Faraco	Electronic Trend Publications
Buck Feltman	Cadnetix, Inc.
Ralph Finley	DATAQUEST Incorporated
Suzanne Finocchio	Bank of America
Kamran Firooz	Hewlett-Packard Corp.
David Flaningam	Test Systems Strategies, Inc.
Frank Florence	DATAQUEST Incorporated
Rick Flugel	Matrix Partners
Fogle, Jim	Teradyne, Inc.
Curt Francis	Advanced Micro Devices, Inc.
Dan Garms	CAD/CAM Specialists, Inc.
Jim Gay	Perq Systems Corp.
Tom Gnuse	Prime Capital Management
Chris Goldstein	Applicon
Stan Graham	Modern Electrosystems, Inc.
Roberto Grasso	Ing. C. Olivetti & C., SPA
Robert W. Greer	Automated Systems Inc.
Horst Gschwendtner	Robert Bosch GMBH
Dave Gullickson	Versatec
Guy Haas	Computervision Corp.
Kevin Hall	Calma Company
Bruce Hanson	Gould Electronics
James Harrison	Adler & Company

Gib Hattery	CAE Systems, Inc.
Ron Hayman	Motorola, Inc.
Grant Heidrich	Mayfield Fund
Henry S. Hofmann	Hewlett-Packard
Sheila A. Holland	Hitachi America Limited
William G. Holt	Holt Inc.
Stefano Horpurgo	Olivetti and C; SPA
Jeff Hotchkiss	Teradyne, Inc.
Mike W. Hu	Televideo
Paul Huber	Megatek Corp.
Claudia Huntington	Capital Research
J. E. Iwerson	Bell Labs
John Jackson	DATAQUEST, Incoporated
Debra Jacob	DATAQUEST, Incoporated
Kent Jaeger	California Devices, Inc.
K. Charles Janac	Stanford University
Jan Janse	Philips Research Labs
Richard Jennings	VIA Systems, Inc.
Alan Jepsen	Bank of America
Harvey Jones	Daisy Systems Corp.
Robert Joseph	Philips Test & Measuring Instrument
Bill Kaiser	Apollo Computer
Thanasis Kalekos	Versatec

Ram Kasargod	IDS
Phillip A. Kaufman	Slicon Compilers, Inc.
Dave Kaverman	Hewlett-Packard
Norman P. Kelly	Altos Computer Systems
Bill Knox	CAE Systems Inc.
Mike Knudsen	CalComp
Michael Kretsch	Exlsi
Gerard Langler	Mentor Graphics Corp.
Lucio Lanza	Daisy Systems Corp.
Wendy Ledamun	DATAQUEST, Incoporated
Greg Ledenbach	National Semiconductor
Frank Lee	Monolithic Memories
Kelly Leininger	DATAQUEST, Incoporated
Carol Lemlein	Teradyne, Inc.
Van Lewing	Calma Company
Shyiuing Lin	E.R.S.O.
Rhonda Y. Lindsey	CADAM Inc.
Robert Lurz	Eastman Kodak Company
Francis T. Lynch	Valid Logic Systems
R. Van Maas	Philips
Leslie Marshall	Calma Company
Bob Martin	Tektronix
Edie Mata	Fujitsu Microelectronics
Roland Mattison	VIA Systems, Inc.

Michael W. McDonald	CAD/CAM Specialists, Inc.
Ken Mckenzie	DATAQUEST Incorporated
Daniel C. McNiell	Gould, Inc.
Robert McLellan	Bell Northern Research
Charles Miller	Analog Design Technology
David H. Miller	Applicon
Linda Miller	InterWest Partners
Richard Mirabella	Phoenix Data Systems
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Elizabeth Obershaw	Hewlett-Packard
Dewitt Ong	Intel Corp.
Alan Oppeinheimer	Apollo Computer
Han Park	Qume Corp.

Evelyn Peairs	Calma Company
Jeff Pepper	Perq Systems
Michele Perrota	Daisy Systems Corp.
Richard Perry	LSI Logic Corp.
Ross Peters	Murray Electronics PLC
Jewel Peyton	DATAQUEST, Incoporated
Cathy Pierson	Oak Management
Roland J. Piziali	Arthur Young & Company
Jay Popper	Standard Microsystems Corp.
Roy Prasad	Personal Cad Systems
Jamshed Qamar	OKI Semiconductors
F. Ramsay	Ferranti Electronics
Karen Regnante	Mosaic Technology
Robert Resslhuber	Computervision Corp.
Carlo Ronca	Olivetti System Development Div.
Mary Ellen Saxby	DATAQUEST, Incoporated
Kathrine Schapiro	Harris Bretall
John Seaton	Gould Electronics
Paul F. Seckendorf	Silvar-Lisco
C. Seih	E.R.S.O.
Ariel Sella	Softel-Advanced Technology
John Sheehan	Intel Corp.
Steve Shively	International Microcircuits, Inc.
Pamela Shook	DATAQUEST, Incoporated

Scott Shull	Intel Corp.
Chester Silvestri	Megatest
Mike Sisavic	Metheus Corp.
G. Skorup	South African Microelectronics Sys.
Joseph Sliwkowski	Telesis Systems Corp.
William Smit	University of Pretoria
Jack Spigarelli	Cericor, Inc.
Rosann Stach	NCA Corp.
Rich Stamm	Data General Corp.
J. Stevenson	Philips
Mrogan W. Stuart	NCA
Gary Stump	Tektronix
Leslie Swanson	Computervision Corp.
Carol Tegnell	Scientific Calculations, Inc.
Robert S. Tepper	A T & T Bell Laboratories
Ben Thomas	Calma Company
Mel Thompson	DATAQUEST, Incoporated
Rick Timmons	Wyle Labs
Paul R. Topping	McDonnell Douglas Automation
Walter Trevaskis	A T & T
Y. C. Tsai	E.R.S.O.
Graham S. Tubbs	Intel Corp.
Beth Tucker	DATAQUEST, Incorporated

Ruth Tucker	Versatec
Bill Unger	Mayfield Fund
Steve Vaughn	IBM
Dave Vogte	Teradyne, Inc.
Kris Vorm	Calma Company
Fred Wagner	IBM
Irving Weiman	R&D Funding Corp. Pru-Bache
Michael Weisberg	Prudential Bache
Patrick Welch	Hewlett-Packard
Jerry Werner	VLSI Design Magazine
Gary Westbrook	Calma Company
Alan Winslow	Tektronix
Larry Yamada	Calma Company
Bryan Yates	Calma Company

Nielsen Dataquest

CAD/CAM Focus Conference

May 10 and 11, 1984

Sunnyvale, California

List of Attendees

Robert S.Tepper	A T & T Bell Laboratories
James Harrison	Adler & Company
Bob Burkhardt	Advance Micro Devices, Inc.
Curt Francis	
Norman F.Kelly	Altos Computer Systems
Martin Walker	Analog Design Technology
Bill Kaiser	Apollo Computer
Alan Oppeinheimer	
Chris Goldstein	Applicon
David H. Miller	
Ang Danna	Arthur Young & Company
Ronald J. Piziali	
W. Robert Greer	Automated Systems Inc.
Suzanne Finocchio	Bank of America
Alan Jepsen	
J. E. Iwerson	Bell Labs
Robert Mclellan	Bell Northern Research
Rhonda Y. Lindsey	CADAM Inc.

Bill Knox	CAE Systems Inc.
Gib Hattery	
Bill Barret	Caddrx
Buck Feltman	Cadnetix, Inc.
Mike Knudsen	CalComp
Rich Peters	
Kent Jaeger	California Devices, Inc.
Phil Arana	Calma Company
Raj Badhwar	
Sam Daram	
Brian Gardiner	
Kevin Hall	
Rob Kuhling	
Van Lewing	
Carolyn Mullery	
Dave Niehaus	
Evelyn Peairs	
Tom Teeters	
Ben Thomas	
Kris Vorm	
Gary Westbrook	
Larry Yamada	
Claudia Huntington	Capital Research
David L. Bailey	Cericor, Inc.
Jack Spigarelli	

John Gilbert	Cigna Investment Management
Earl North	Circuit Tools, Inc.
Guy Haas	Computervision Corp.
Russel Huber	
Leslie Swanson	
Andy Barnes	DATAQUEST Incorporated
Sharlene Burden	
Ralph Finley	
Frank Florence	
Ken McKenzie	
Frank Sammann	
Dave Burdick	
John Jackson	
Debra Jacob	
Wendy Ledamun	
Kelly Leininger	
Jewel Peyton	
Andy Prophet	
Mary Ellen Saxby	
Pam Shook	
Mel Thompson	
Dave Crockett	
Jim Newcomb	
Beth Tucker	

Harvey Jones	Daisy Systems Corp.
Charles Bures	Data General Corp.
Nelson Bye	
Majid Ghafghaichi	
Rich Stamm	
Lloyd Anderson	Dataproducts
Wade Chanz	E.R.S.O.
P. Csao	
Tennyson Csen	
Shiminz Lins	
C. Seih	
Robert Leurz	Eastman Kodak Company
Michael Kretsch	Exlsi
F. Ramsay	Ferranti Electronics
Katy Plumb	First Interstate Bank of California
Jim Long	Fujitsu Microelectronics
Edie Mata	
Hal Barbaur	GenRad
Bob Anderson	
John DiGirolamo	
Francois Durif	
Eric Mudama	
David Wharton	

Donald Butler	General Instrument Corp.
Daniel C. McNiell	Gould, Inc.
Karl Nakamura	GRID Systems
Joseph Augustino	HHB-Softron
Katherine Schapiro	Harris Bretall
Alan Bagley	Hewlett-Packard
Bill Bowman	
Don Corson	
Daniel Fan	
Dave Kaverman	
Bob Moore	
Jack Nilsson	
Elizabeth Obershaw	
Patrick Welch	
Firooz Kamran	
Henry S. Hoffman	
William G. Holt	Holt Inc.
Frank Calabretta	Holt, Inc.
Steve Vaughn	IBM
Fred Wagner	IDS
Ram Kasargod	Ing. C. Olivetti & C., SPA
Roberto Grasso	
Cesare Segre	
Mary Jane Elmore	Institutional Investment Partners

Wei-tau Chiang	Intel Corp.
Dewitt Ong	
John Sheehan	
Linda Miller	InterWest Partners
Steve Shively	International Microcircuits, Inc.
Mike Connell	LSI Logic Corp.
Richard Perry	
Rick Fluegel	Matrix Partners
Grant Heidrich	Mayfield Fund
Paul R. Topping	McDonnell Dougals Automation (McAuto)
Paul Huber	Megatek Corp.
Chester Silvestri	Megatest
Gerard Langler	Mentor Graphics Corp.
Mike Sisavic	Metheus Corp.
Stan Graham	Modern Electrosystems, Inc.
Peter Lowell	
John Nam	
Nikola Pavicic	
Frank Lee	Monolithic Memories
Karen Regnante	Mosaic Technology
Ron Hayman	Motorola, Inc.
Bob J. Jenkins	
Douglas Ritchie	National Samiconductor
Jamshed Qamar	ORI Semiconductors

Ugo De Riu	Olivetti System Development Div.
Carlo Ronca	
Philip Monego	Paragon Technology Corp.
Jeff Pepper	Perq Systems
Jim Gay	
Richard Nedbal	Personal Cad Systems
Roy Prasad	
R. Van Maas	Philips
J. Stevenson	
Robert Joseph	Philips Test & Measuring Instruments
Richard Mirabella	Phoenix Data Systems
Tom Gnuse	Prime Capital Management
Laura Conigliaro	Prudential Bache
Michael Weisberg	
Han Park	Qume Corp.
Irving Weiman	R&D Funding Corp. Pru-Bache
Barrie Murray-Upton	Racal-Redac Limited
Steve Chadima	Regis McKenna
Dennis Patton	Ridge Computers
Horst Gschwendtner	Robert Bosch GMBH
Darko Brodarac	
Carol Tegnell	Scientific Calculations, Inc.
Jan Janse	Siemens Research Labs

Tom Binder	Silvar-Lisco
Phillip A. Kaufman	Silicon Compilers, Inc.
G. Skorup	South African Micorelectronics Systems
Jay Popper	Standard Microsystems Corp.
Jim Cooper	Tektronix
John Crist	
Bob Draeger	
Bob Martin	
Gary Stump	
Alan Winslow	
Joseph Sliwkowski	Telesis Systems Corp.
Mike W. Hu	Televideo
Gil Burns	Teradyne, Inc.
Jim Fogle	
Jeff Hotchkiss	
Carol Lemlein	
John O'Brien	
Dave Vogte	
David Flaningam	Test Systems Strategies, Inc.
Ed Locke	United Technologies MOSTEK
William Smit	University of Pretoria
Richard Jennings	VIA Systems, Inc.
Roland Mattison	
Jerry Werner	VLSI Design Magazine

Doug Fairbeirn	VLSI Technology, Inc.
Bob Duyn	
Francis T. Lynch	Valid Logic Systems
Jared Anderson	
Samuel F. McKay	Ventech Partners
Dave Gullickson	Versatec
Thanasis Kalekos	
Mark Maltese	
Art Collmeyer	Weitek
Rick Timmons	Wyle Labs
Bob Lorentzen	Zymos

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WELCOME AND CONFERENCE INTRODUCTON

James R. Newcomb
Director, CAD/CAM Industry Service
Dataquest Incorporated

Mr. Newcomb is Director of DATAQUEST's CAD/CAM Industry Service. Before joining DATAQUEST, he was with Auto-trol Technology Corporation, where he held various executive positions, including Manager of Marketing. Prior to that, Mr. Newcomb was employed by Xerox Corporation, where he held positions as Manager of Systems Integration, Manager of Advanced Manufacturing Engineering, and Divisional Program Planner. Earlier, he worked in an engineering capacity with Strippit-Hoidaille. His professional experience has provided him with an in-depth knowledge of CAD, CAM, CAE, robotics technology, artificial intelligence, and manufacturing automation systems. Mr. Newcomb has a B.S.M.E. from Rochester Institute of Technology. He is a member of the American Society of Mechanical Engineering, SME, RI/SME, and CASA/SME.

Dataquest Incorporated
ELECTRONIC DESIGN AUTOMATION FOCUS CONFERENCE
May 10-11, 1984
Sunnyvale, California

DATAQUEST'S CAD/CAM INDUSTRY SERVICE WELCOMES YOU TO THE 1984 EDA FOCUS CONFERENCE

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ELECTRONIC DESIGN AUTOMATION

"THE TECHNOLOGY RENAISSANCE"

WELCOME

DATAQUEST CORPORATE OVERVIEW

CAD/CAM INDUSTRY SERVICE

CAD/CAM MARKET

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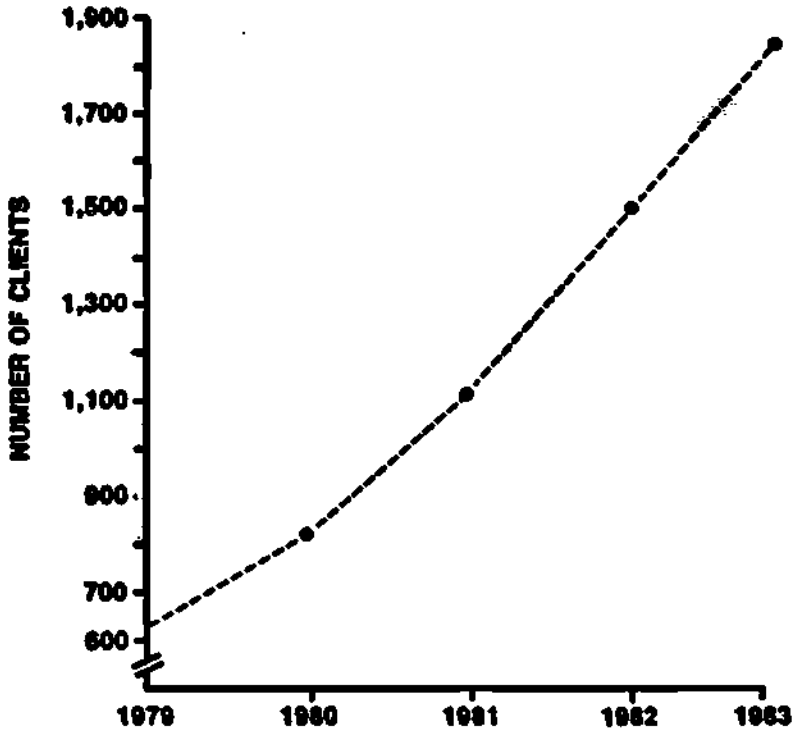
DATAQUEST BUSINESS GROWTH



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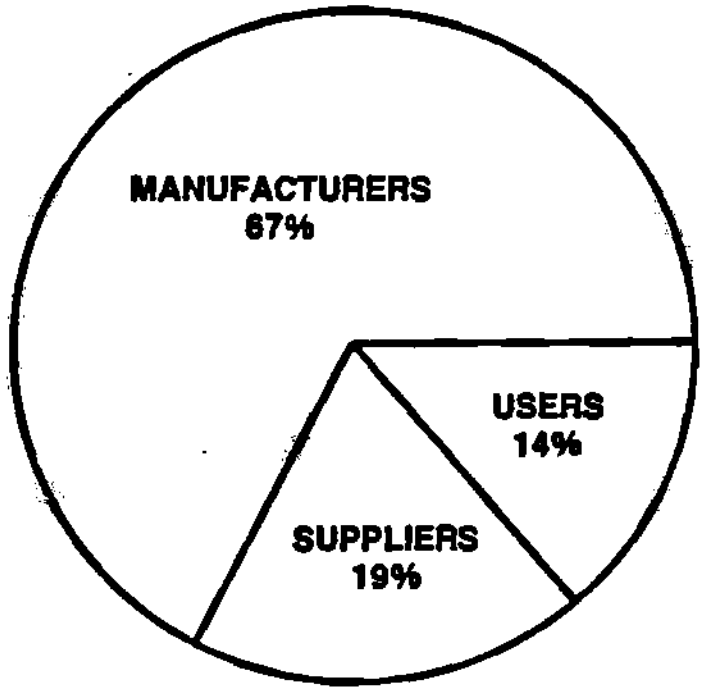
DATAQUEST TECHNOLOGY CLIENTS
(By Type of Business)



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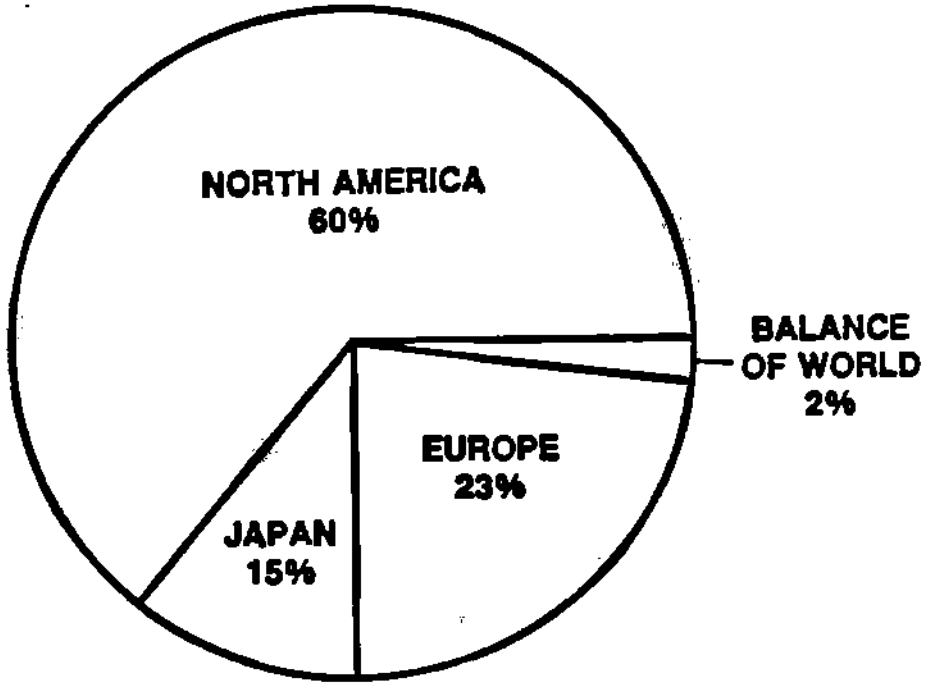
DATAQUEST TECHNOLOGY CLIENTS
(By Geographic Area)



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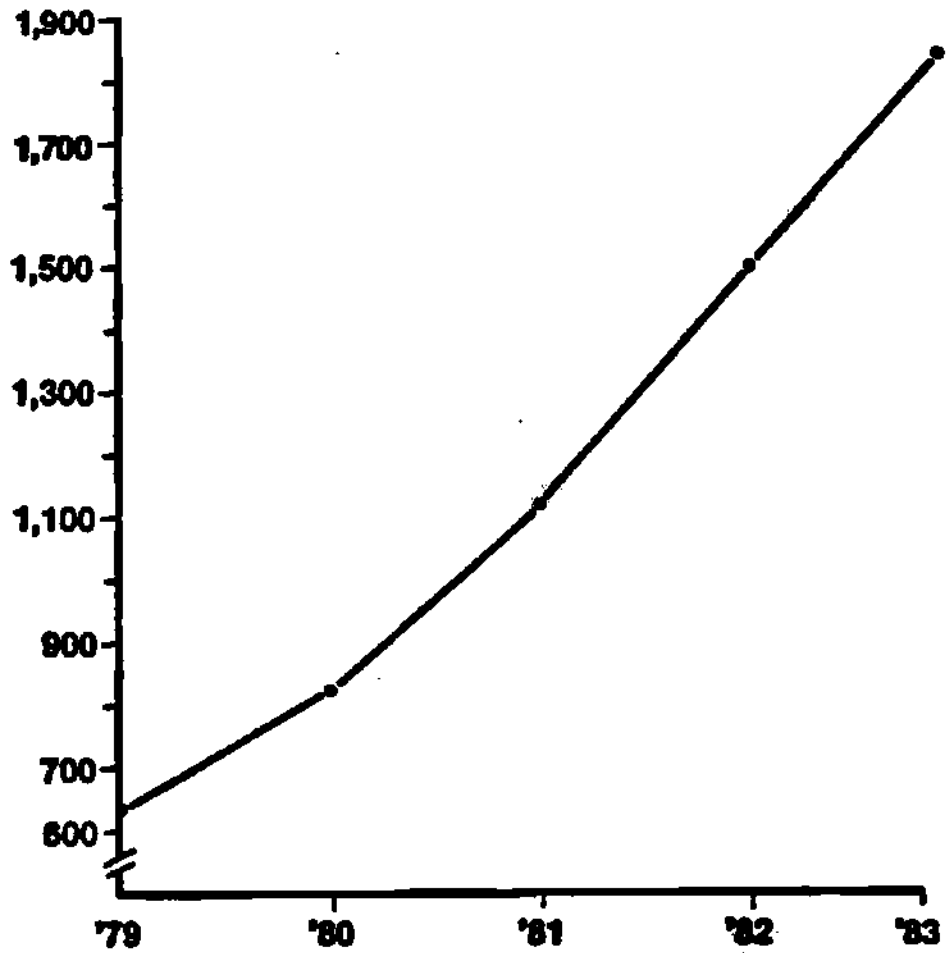
TECHNOLOGY SERVICES

SUBSCRIBER GROWTH



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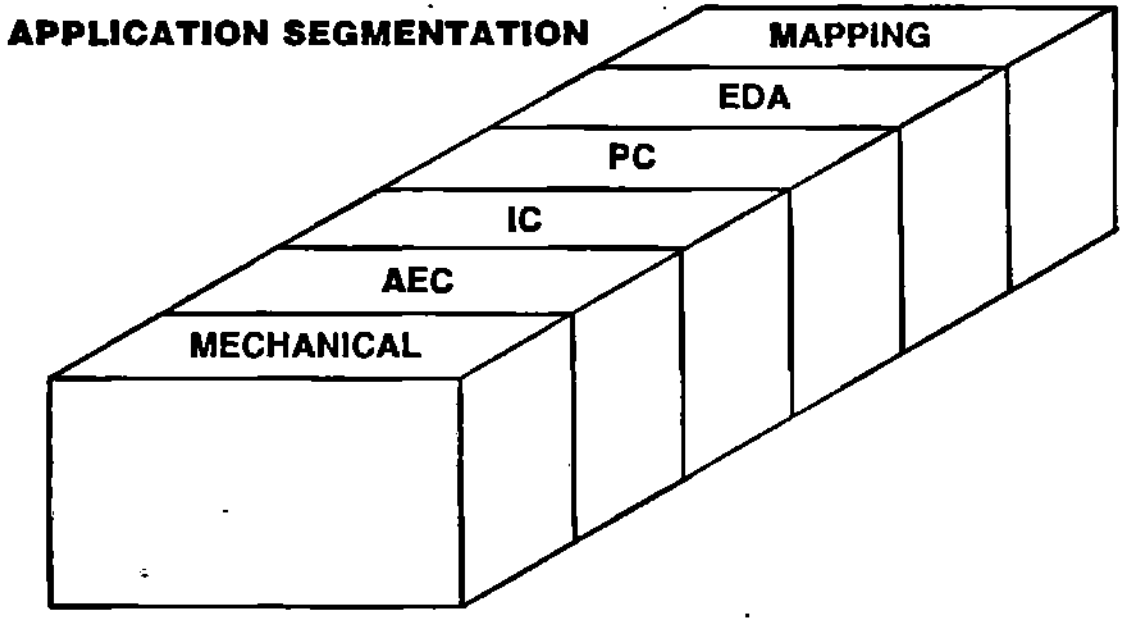
CAD/CAM INDUSTRY SERVICE



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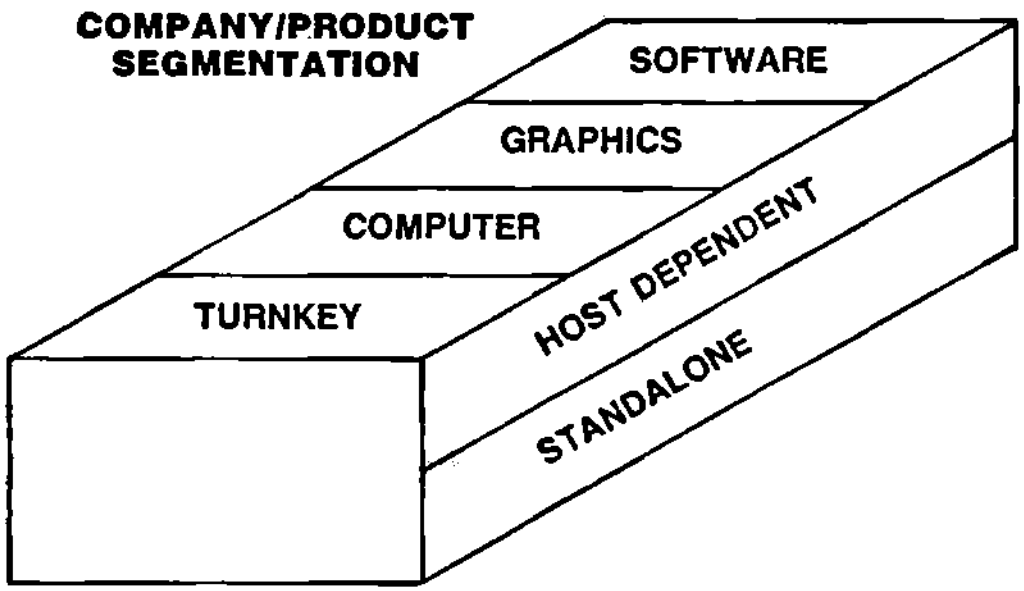
CAD/CAM INDUSTRY SERVICE



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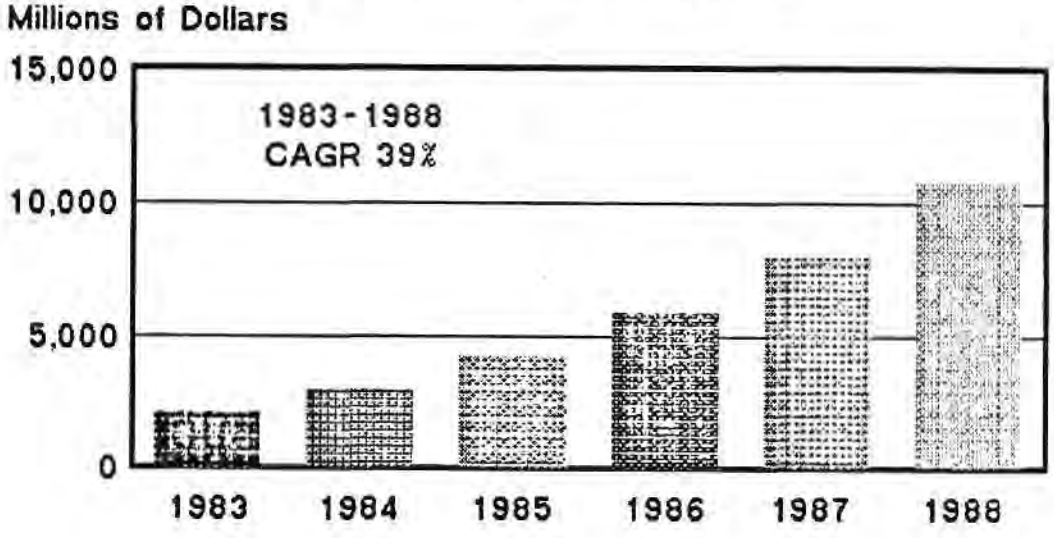
CAD/CAM
TOTAL ANNUAL REVENUE

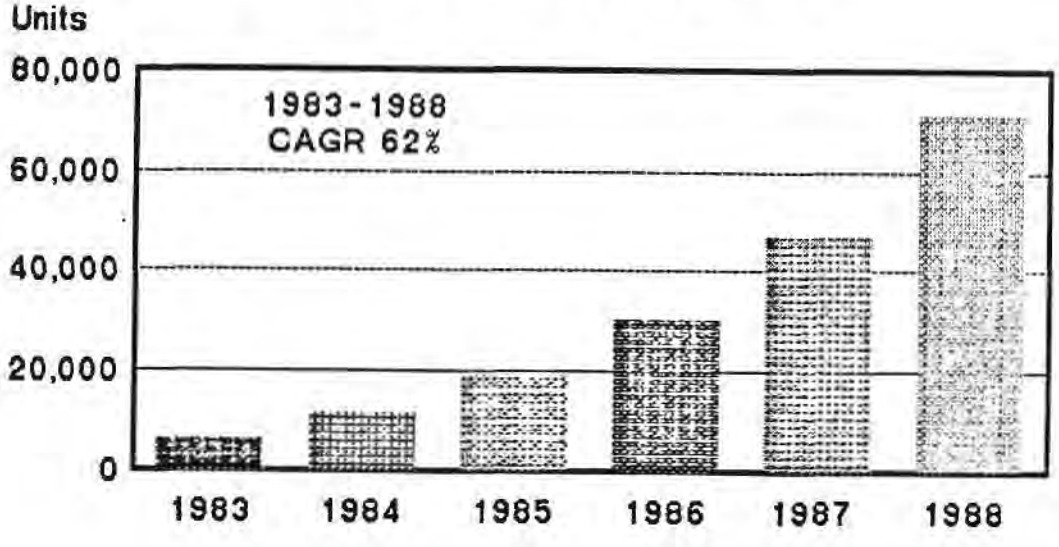
ALL APPLICATIONS/WORLDWIDE



Source: DATAQUEST

CAD/CAM SYSTEMS SHIPPED

ALL APPLICATIONS/WORLDWIDE



Source: DATAQUEST

FOCUS ON EDA

- INDUSTRY OVERVIEW
- EVOLUTION OF AN INDUSTRY
- SEMICONDUCTOR REVOLUTION
- VENDORS AND USERS
- FUTURES, TRENDS BECOME REALITIES

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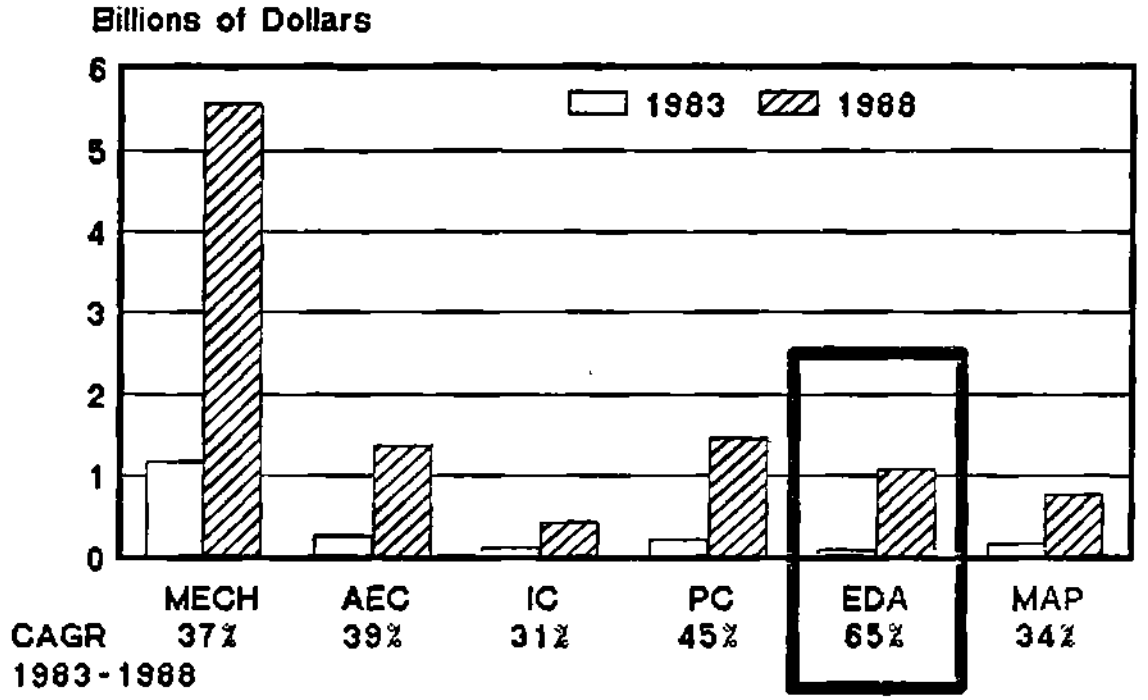
CAD/CAM
REVENUE BY APPLICATION



Source: DATAQUEST

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EDA

Nielsen Dataquest

EDA INDUSTRY OVERVIEW

Beth W. Tucker
Industry Research Manager
CAD/CAM Industry Service
Dataquest Incorporated

Ms. Tucker is Industry Research Manager for DATAQUEST's CAD/CAM Industry Service. In this position, she is responsible for analyzing and reporting on the electronics segment of the CAD/CAM industry. Prior to joining DATAQUEST, Ms. Tucker was Market Planning Manager of Calma Company's Microelectronics Division, where she was responsible for identifying market opportunities and developing marketing strategies for the company's electronic CAD product line. She later contributed to the development of marketing information systems at Calma's corporate level. Prior to that, she was a Senior Market Research Analyst with Monroe Systems for Business, where she was responsible for market research and development of small business computer products. Ms. Tucker holds an A.A. degree in Computer Technology from Morris County College in New Jersey and is doing course work in Business Administration at San Jose State University.

Dataquest Incorporated
ELECTRONIC DESIGN AUTOMATION FOCUS CONFERENCE
May 10-11, 1984
Sunnyvale, California

INTRODUCTION

DATAQUEST is sponsoring this Focus Conference on Electronic Design Automation (EDA) because it is the youngest, most dynamic segment within the CAD/CAM industry today. A five-year compound annual growth rate of 65 percent also makes EDA the fastest-growing CAD application segment. The DATAQUEST conference will focus on defining the EDA market segment, the companies included in the segment, market size and forecasts, and significant trends.

What is Electronic Design Automation? EDA is an integrated set of design tools for electrical engineers designing electronic circuits and products. The key difference between EDA and other electronic CAD tools is the integration, or linkage, of the different phases within any design cycle, versus a discrete and isolated computer-aided design solution.

The application of EDA systems incorporates more than computer-aided engineering for electrical engineers. EDA has evolved to include not only automation of logic design and analysis, but automation of physical layout, engineering administration, and testing, to some degree. DATAQUEST believes that the accomplishments of EDA vendors, and the product differentiation that they offer are significant enough to warrant distinction from computer-aided engineering applications for mechanical or other engineering disciplines. Thus,

DATAQUEST CALLS IT EDA

THE EDA PERSPECTIVE

To put EDA in its proper perspective, we believe that a brief historical overview of DATAQUEST's CAD/CAM applications segments would be valuable. Upon its formation in 1981, the CAD/CAM Industry Service segmented the market into four applications: mechanical; architecture, engineering, and construction; mapping; and electronics. Responding to the market's and our clients' needs, we then refined the definition of the electronics segment to differentiate computer-aided design for integrated circuits and printed circuit boards.

In the publication of our 1983 estimates and forecasts, we further refined the electronics segment to include CAD systems used in electronic design automation. Thus, the CAD/CAM market is segmented based upon the following applications:

- Mechanical
- Architecture, Engineering, and Construction
- Mapping

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- Electronic Design Automation
- Integrated Circuit
- Printed Circuit Board

ELECTRONIC CAD DEFINITIONS

To avoid confusion, we will define what we mean by IC and PC CAD, and EDA. The frame of reference in which these terms are defined is a simplistic overview of the phases in the electronic product design cycle listed below:

- Specification
- Design and Analysis
- Physical Layout
  - Full Custom IC
  - Gate Array
  - Standard Cell
  - Printed Circuit Board
- Design Verification
- Analysis
- Test
- Manufacturing

IC CAD/CAM

IC CAD/CAM systems are used by layout designers to create the physical geometries of an integrated circuit. The layout designer typically works with hard copy forms of schematics created by an electrical engineer, and graphically translates the schematics into patterns to be recognized by a pattern generation machine for mask or direct-write geometries. As of 1984, most of the IC CAD/CAM systems available offer discrete functionality; i.e., they usually address only drafting and the analysis related to design or electrical rules verification. IC CAD systems typically do not address other phases of the design cycle.

Companies included in DATAQUEST's IC CAD/CAM data base are:

- Applicon
- Calma Company
- Computervision
- Scientific Calculations
- Via Systems

With a few exceptions, most IC CAD systems are host-dependent 16-bit computers, running in a centralized environment. Prior to the acceptance of semicustom circuits, IC CAD systems were used to design the geometries of full custom ICs. With the commercialization of semicustom ICs, these CAD systems may also be used to create the geometries of individual standard cells and the manufactured layers of gate arrays.

PCB CAD/CAM

CAD/CAM systems that are used to design printed circuit boards are going through an evolution, such that DATAQUEST now recognizes two distinct types of systems. Although the boundaries may not always be clearly separate, PCB CAD systems are differentiated on the basis of functionality, end-user, and type of hardware.

The first type is systems used for artwork-only creation, with little to no electrical intelligence associated with the data base. Systems within this category are used by drafting personnel in engineering services departments to create the geometries used for photoplotters, silk screens, numerical controls, drill paths, and documentation. The actual traces may be created interactively (i.e., manually) or automatically, as with packaging and placement functions. Some systems in this category have the ability to create schematics that are used for net list generation as input to an automatic router, back annotation, and documentation. Digitizers are often an integral part of these systems. The environment in which this type of system operates is usually a centralized CAD shop, with host-dependent computers and stations.

The second type of PCB CAD system is more comprehensive in nature. It is typically a 16- or 32-bit standalone system, with communication capabilities for use in a networked environment. In addition to engineering services' drafting personnel, it can also be used by electrical engineers to create PC board logic designs. The data base is often structured so that net lists can be generated as input to other simulation and analysis programs, in addition to placement and routing programs. These PCB vendors may directly sell analysis programs, or they may have joint marketing agreements with software companies.

Companies in DATAQUEST's PCB CAD/CAM data base include:

- Applicon
- Cadnetix
- Calay
- Calma Company
- Computervision
- Digital Equipment
- EAS
- Gerber Scientific
- IBM
- Paragon Technology
- Prime Computer
- Racal-Redac
- Scientific Calculations
- Telesis Systems
- Vectron Graphics
- Versatec

The phases in the design cycle that are addressed by PCB CAD/CAM vendors include the physical layout of printed circuit boards, design rule verification, and to some degree, design and analysis, post-layout analysis, and test.

Electronic Design Automation

EDA systems are used by electrical engineers and engineering staffs to create and design electronic products, including integrated circuits, printed circuit boards, and actual systems. EDA systems emphasize an integrated and comprehensive design tool solution, addressing all phases of the design cycle. The systems themselves are typically standalone, or if not standalone, they are relatively less expensive than traditional host-dependent CAD systems. They typically employ 16/32-bit microprocessor technology, and operate in a decentralized, networked environment.

When DATAQUEST first created a separate applications segment for EDA systems, they were used mostly for logic or circuit design, and for analysis programs such as circuit and logic simulation, timing verification, and fault simulation. Today, however, EDA systems address a broad range of applications, including physical layout of printed circuit boards and full custom ICs, and placement and routing programs for gate arrays and standard cells. And the market continues to expand its scope. For example, an integral part of an EDA system may also include dedicated hardware engines used to speed the process of simulating complex circuitry. Hardware logic analyzers integrated with design data bases are also used and sold by EDA vendors.

Not only do EDA systems directly address electrical engineers' needs for design tools, but they also include functionality for word processing, technical publications, project management, and electronic mail.

Companies in DATAQUEST's EDA data base currently include the following:

- CAE Systems
- Cadtec
- Calma Company
- Daisy Systems
- Intergraph
- Mentor Graphics
- Metheus
- Silvar-Lisco
- Valid Logic

DATAQUEST believes that the list of vendors participating in the EDA segment will continue to grow. We believe that other major turnkey companies and computer companies will enter this market during the next several years, and that the market will become somewhat fragmented.

EDA MARKET SIZE

The electronic design automation segment grew 328 percent in 1983. The worldwide revenues of $90 million were highly concentrated in four of the ten companies currently selling EDA systems. Dataquest estimates that the EDA segment will increase approximately 136 percent during 1984, reaching $211 million in worldwide revenues.

Market Forecast

DATAQUEST estimates that the EDA market segment will grow at an average compound annual growth rate (CAGR) of 65 percent during the next five years, and that the market will be more than $1 billion in 1988. Workstation shipments are expected to grow by 67 percent per year, increasing from 1,329 units in 1983 to approximately 17,112 units in 1988. The table below represents our yearly estimates:

EDA MARKET ESTIMATES AND FORECASTS
(Millions of Dollars)

	1983	1984	1985	1986	1987	1988
Revenue	90	211	357	533	772	1,092
Workstations	1,325	3,223	5,421	8,002	11,774	17,112

The EDA segment has gained a tremendous amount of momentum, considering its relatively early stage of development. We believe that this momentum will carry through 1988 due to:

- Demand
- Expanded product lines
- Incorporation of new hardware technologies
- New entrants
- Application niches

Quarterly revenue of the three market leaders continues to increase at outstanding rates. There has been much publicity about the successful accomplishments of EDA companies, which is in keeping with their general high-awareness marketing strategies. The table below represents the sum of quarterly results of Daisy Systems, Mentor Graphics, and Valid Logic:

EDA QUARTERLY SALES
(Millions of Dollars)

	1981	1982	1983	1984
Quarter 1	0	1.17	7.16	39.21
Quarter 2	0	2.08	12.33	N/A
Quarter 3	0	3.88	19.24	N/A
Quarter 4	0.21	3.81	31.69	N/A

N/A = Not Available

Market Share Estimates

DATAQUEST currently follows ten companies in the EDA segment. Four of them comprise 88 percent of the 1983 revenues, while the other six companies comprise the remaining 12 percent. The table below represents our market share estimates:

EDA 1983 MARKET SHARE ESTIMATES
(Millions of Dollars)

	Revenue	Market Share
Daisy Systems	$28.4	31%
Mentor Graphics	26.0	29%
Silvar-Lisco	9.0	10%
Valid Logic	16.1	18%
Other*	10.5	12%

*Other includes: Cadtec, CAE, Calma, Control Data, Intergraph, and Metheus

Electronic CAD/CAM Estimates

DATAQUEST estimates that the entire electronic CAD/CAM segment is growing at an average CAGR of 47 percent. EDA is growing the fastest, at a 65 percent CAGR, followed by printed circuit CAD/CAM with a 45 percent CAGR and integrated circuit CAD/CAM with a 31 percent CAGR.

DATAQUEST believes that another segmentation of the electronic CAD market is meaningful due to the close relationships and slight overlaps between the IC, PC, and EDA segments. The second market segmentation is based upon the electronic product design cycle discussed earlier in this paper. We have estimated the size and growth of the electronic CAD/CAM market-based system usage within the following design phases:

- Logic design and analysis
- Full custom IC layout
- Gate array layout
- Standard cell layout
- Printed circuit board layout

The table below shows our estimates for workstation shipments, either standalone or host-dependent, that will be used in the previously described design cycle.

ELECTRONIC CAD SYSTEM USAGE
(Workstation Units)

	1983	1988	CAGR
Logic Design and Analysis	1,240	14,253	63%
Full Custom	778	3,782	37%
Gate Array	80	2,915	105%
Standard Cell	54	2,976	123%
Printed Circuit	2,072	14,321	47%

These numbers represent the sum of total workstations in the IC, PCB, and EDA CAD/CAM segments; however, they were calculated based on design cycle phases, not on the type of company selling the workstation. For example, an EDA system can be used to do logic design, full custom layout, or printed circuit board layout. Conversely, a PC CAD system may be used for logic design and analysis in addition to printed circuit board layout.

We believe that the above design cycle segmentation, in conjunction with our standard applications segmentation, provides an accurate overall picture as to which company is selling a system, and what the system is being used for.

Systems used for printed circuit board layout is the largest segment in 1983 because vendors in the PC CAD/CAM segments have been established longer. We believe that these systems will decrease as a percentage of total system shipments because of increased usage in other design phases.

We expect that systems used for design automation, or logic design and analysis, gate array, and standard cell placement and routing will increase as a percentage of total shipments through 1988. All three have large CAGRs, which is due in part from the small base at which they are starting. Additionally, their growth is spurred by the acceptance of semicustom circuits and design methodologies.

In summary, we believe that the systems usage for companies currently in the IC, PC, and EDA segments will become increasingly difficult, as some start to expand their current product strategies and address design phases outside of their traditional markets.

DRIVING FACTORS

Circuit Complexity

Much has been said about the increasing complexity of integrated circuits. It is not feasible to create a VLSI circuit today without the aid of some type of computer-assisted design, analysis, or engineering program. It is not the intention of this DATAQUEST Focus Conference to discuss the growing complexity of circuits, but to draw a parallel to the need for engineering design tools to meet the needs of today's design engineers in working with these circuits.

Phrases like "productivity" and "speed to market" are associated with the EDA market. Productivity and speed to market, as it turns out, are EDA products' biggest benefits.

The goal is to reduce the time required to design a product, while maintaining or improving circuit functionality and complexity. The end result is a higher return on investment and a faster payback period for the company designing, manufacturing, or marketing a circuit, when compared with the product life cycle. Productivity and speed to market apply not only to semiconductor manufacturers, but to system or computer manufacturers.

Semicustom Circuits

With the increasing acceptance of gate array ICs and standard cell design methodologies, the time it takes to design and market a product is shortened even more than when compared to using an EDA system for full custom ICs. Not only is the design cycle shortened, but engineers who have not been trained to design specifically on silicon can now create semicustom circuits. The end result is a circuit that is customized to a particular application, has better functionality, and possibly has reduced product cost through the use of fewer printed circuit boards in a given system.

In his speech later today, Ken McKenzie, Associate Director of DATAQUEST's Semiconductor Industry Service, will further explore the relationship and synergy between semicustom chips and electronic design automation systems.

We believe that one of the goals of an EDA vendor with semicustom design capability is to put the task of creating integrated circuits into the hands of engineers designing entire systems, who are accustomed to using TTL parts. The total available market would then increase from approximately 3,000 silicon design engineers to approximately 450,000 total design engineers.

Hardware Technology

To effectively penetrate a market of approximately 450,000 worldwide electrical engineers, two actions must be taken simultaneously: decrease system costs and maintain an equal or better level of system functionality.

The typical system hardware of an EDA vendor today consists of the following:

- 16/32-bit microprocessor
- 1- to 4-MB memory
- 60- to 160-MB Winchester-type disk drive
- 1-MB flexible disk drive
- High-performance graphics terminal, preferably color
- Applications software

Peripherals such as plotters, printers, communications, file servers, or tape drives, are available in addition to the above, depending on user requirements. The average selling price of the system hardware described above is approximately $60,000. The cost of the hardware continues to decrease over time as performance continues to increase.

DATAQUEST believes that to penetrate the market to the point where the majority of engineers have some type of interactive design tool on their desks, hardware prices must decrease more steeply than the predicted 15 percent per year for OEM cost, and 7.5 percent per year for end-user price. This is discussed further under the Trends section.

TRENDS

Due to the embryonic state of the EDA segment, practically everything that occurs within it is a significant trend. Major events such as product announcements, mergers and acquisitions, bankruptcies, third-party software agreements, public offerings, and new entrants, occur on a regular and frequent basis. The following trends are those that DATAQUEST believes have the most impact on the present EDA market.

Marketing/Sales

To say that the EDA segment is highly competitive is a gross understatement, but it is true. DATAQUEST expects the EDA segment to maintain this high level of competition during the next several years, for the following reasons:

- Buy market share
- New entrants
- Many vendors (in relation to market life cycle)
- Lean and mean
- Functionality race
- Market educational requirements
- Market needs and demands

The market leaders have set the industry pace. New entrants must be willing and able to meet this pace. Maintaining intense sales and marketing positions, however, can be a financial drain on a company, or even a barrier to entry.

The following figures represent the sums of Daisy Systems', Mentor Graphics', Silvar-Lisco's, and Valid Logic's fiscal expenses as a percentage of revenue for each of their respective fiscal years.

EXPENSES AS A PERCENTAGE OF REVENUE
(Millions of Dollars)

	1982	1983
Revenue	10.6	63.7
Marketing, General and Administrative	66%	40%
Research and Development	43%	16%

Expenses are expected to be high during the first several years of operation (notice 1982 was not profitable). However, DATAQUEST believes that the EDA segment will continue to reflect higher than average marketing and sales expenses as a percentage of revenue. We do not believe that competition will become less intense than it is today. The

companies analyzed in the above figure, besides being the only public, nonsubsidiary EDA companies, are also the 1983 market leaders. We believe that they will continue to fight for their present positions as new companies enter the market.

Functionality

Closely related to the market competitiveness is product functionality, as evidenced by the major product announcements of almost all EDA vendors during the past seven months.

Product introductions are not haphazard, although some might be reactionary. Perhaps it is pure coincidence that three companies introduced a hardware simulation engine within five months of one another. Perhaps it was because they were all at relatively similar stages of organizational development and maturity. Nonetheless, it seems safe to conclude that what one company starts, others will follow.

In addition to the applications offered on current EDA systems, DATAQUEST believes that the following system functions will be added to EDA vendors' product portfolios:

- Enhanced behavorial-level simulators
- Enhanced modeling tools
- Emphasis on structured logic design
- Operating system software development tools
- Application system software development tools
- Automatic test equipment interfaces
- Automated testing software
- Integration of analog circuit design
- Integration of PCB routers and system functionality
- Silicon compilers
- Integration with mechanical CAD data bases
- Interfaces to CAM/CIM, if not the actual software products
- Standard data base interfaces
- Artificial intelligence

EDA vendors continue to strive toward a "complete" product. With 1983 R&D expenses approximately 16 percent of revenue, not only are vendors making enhancements (and bug fixes) to existing products, but the leaders continue to reach for state-of-the-art. Going back to the system benefits of increased productivity and speed to market, DATAQUEST believes that development efforts will continue to focus on automating the entire electronic product design cycle.

INTERFACES

In order to accomplish complete design automation, EDA vendors must contend with two forces. First, they must work with their target market's existing design tools. Although low-cost, interactive graphics systems have not been used very long for design automation, users do have a considerable investment in either in-house developed tools or tools purchased from software companies. To ease the acceptance of EDA systems, vendors must provide capabilities that interface with their users' existing tools.

The second force, and one that works against EDA vendors, is time. Given EDA's relatively early stage of development, it is virtually impossible to develop all software at once. Hence, there is additional need to provide interfaces to existing design aids and to other CAD/CAM systems. DATAQUEST does not believe that this is a negative factor, since it is ultimately most beneficial to the user and to the vendor that can support the widest capabilities.

Finally, interfaces in terms of libraries and data base structure are critical to the widespread acceptance of semicustom circuits. It is in the best interest of both EDA vendors and silicon foundries or semiconductor manufacturers to determine and agree upon standard interfaces. This way, EDA vendors would not lose sales because of the lack of a particular foundry's library. The foundry would benefit from increased distribution channels through each of the EDA vendors' sales forces and installed bases.

Application-Specific Hardware

The underlying goal to increase productivity affects many aspects of EDA. Interactive software tools are available on low-cost workstations to aid the design engineer. Interfaces to batch-oriented software analysis programs bridge the gap between the standalone user and the host-dependent user. Finally, hardware dedicated to and designed for specific computer-bound tasks is available to work with EDA design data bases.

Simulation engines, for example, can complete a simulation pass in seconds, where it might have taken software methods hours to complete. Dr. Jared Anderson, President of Valid Logic Systems, Inc., will address the use of application-specific hardware in the EDA market segment.

The EDA segment is not alone in its use of application-specific hardware. The CAD/CAM, computer, and graphics industries are applying more and more hardware dedicated to specific tasks. Examples of such hardware may include: pipeline processors; geometry engines; tiling engines; array processors; and co-processors, in addition to simulation engines.

DATAQUEST believes that this is a significant trend occurring within the entire CAD/CAM industry, and that it will be especially evident within the EDA segment.

PERSONAL ENGINEERING WORKSTATIONS

There is no question as to acceptance of electronic design automation systems as the solution to engineering design tasks. However, vendors and users agree that the average selling price of workstations must decrease in order to penetrate the electrical engineering community.

In addition to traditional host-dependent systems and standalone workstations, personal computers (PCs) are emerging aa an important type of hardware in the entire CAD/CAM marketplace. DATAQUEST believes that PCs will play an increasing role in electronic CAD applications.

Based on current performance levels, PCs are best suited for applications that are less compute-intense, such as schematics drafting and physical layout. There are, however, several vendors that presently sell PC-based CAD systems that include forms of analysis and simulation. DATAQUEST believes that the very low-end market will be segmented based on performance and end use. We believe that low-end PCs will be used mainly for drafting purposes in large companies that use networking capabilities to communicate with the design automation process, or by small companies with less need for higher performance, higher cost, comprehensive systems.

We also believe that the low-end PC market will serve engineers and their requirements for analysis and simulation, as well as for schematic creation. To do this, however, will require different hardware technology than what is currently available from standalone workstation and personal computer manufacturers. The price of a standalone workstation must decrease to the $10,000 to $20,000 range, and the performance of the personal computer must increase to be competitive with that of a standalone workstation.

DATAQUEST recognizes this new hardware segment as personal engineering workstations (PEWS). We believe that PEWS will include medium- to high-performance graphics capabilities, local area networking capabilities, 32- or 16/32-bit microprocessors, application-specific integrated circuits (ASICs), and low to medium storage capabilities. PEWS will be configured to attain high levels of productivity, with the inherent ability to share resources. DATAQUEST believes that volume shipments of PEWS will begin in late 1984 or early 1985.

It is through PEWS, and their networking with personal computers, standalone workstations, and host-independent computers, that the mass of the engineering market will be penetrated.

NICHE APPLICATIONS

The EDA segment is growing at a phenomenal rate. Product introductions occur regularly and frequently. Different companies are entering the market. Product and company differentiation is becoming increasingly more difficult to recognize. DATAQUEST believes that the EDA segment is large enough to support many vendora, as the other CAD/CAM application segments currently do. However, we believe that product differentiation will begin to occur, as new entrants address niche applications.

The current EDA vendors and the companies expected to enter the market in the near future have similar product portfolios. Though they differ in corporate and marketing strategies, and actual product functionality, DATAQUEST believes that there is presently little true product differentiation between the major vendors.

We believe that the market will evolve to include companies addressing specific application or target market niches, that may include the following:

- Printed circuit board design automation: We believe that companies selling high performance standalone systems with schematics entry capability and an intelligent data base will expand their product offerings to include more design automation software.

- Analog circuit design: Although analog circuit design is not the critical bottleneck in a design cycle, we believe that companies will begin to offer standalone and/or integrated systems with capability to incorporate analog and digital circuit design.

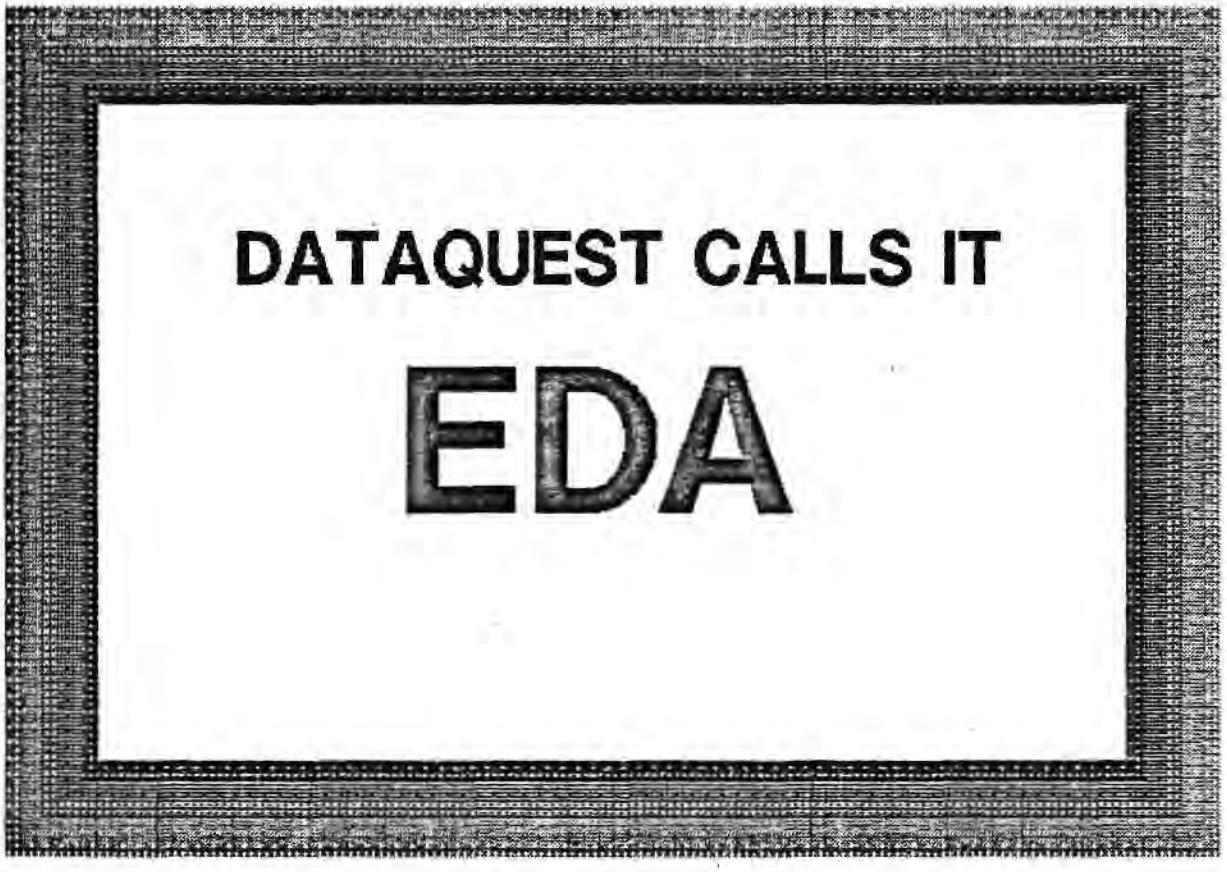
- Silicon compilers: We believe that silicon compilers are the next generation of design automation, and that they will become commercially used and accepted. Vendors may incorporate compilers into their current product lines, or new companies will emerge with compilers as their main products.

- Semiconductor distributors: With the availability of standalone workstations and semicustom circuits, distributors will emerge as an important distribution channel for both types of products.

- Software-only companies: The ability to accomplish a design task through application software is the true added value to any CAD/CAM system. We believe that more companies will emerge with software-only products as design tasks become increasingly complex. We also believe that more and more third-party software activity, mergers, and acquisitions will occur.

CONCLUSIONS

The electronic design automation segment of the CAD/CAM industry is complex, and undergoing constant change. DATAQUEST believes that it will play an ever-increasing role in the electronic CAD/CAM application segments and in the design of electronic products. We believe that successful vendors recognize the importance of truly integrating all phases of the design cycle with common data bases, interfaces, and systems. Engineers creating products in 1988 will enjoy the conveniences and productivity increases that EDA systems will provide them. It is these engineers that will make the EDA segment climb to more than $1 billion in 1988. It is these engineers that will create state-of-the-art electronic circuits, systems, and products through the use of electronic design automation tools.



ELECTRONIC DESIGN AUTOMATION

INTEGRATION

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EDA INDUSTRY OVERVIEW

- DEFINITIONS
- MARKET SIZE
- DRIVING FACTORS
- TRENDS

CAD/CAM
APPLICATION SEGMENTS

MECHANICAL	AEC	MAPPING	ELECTRONICS

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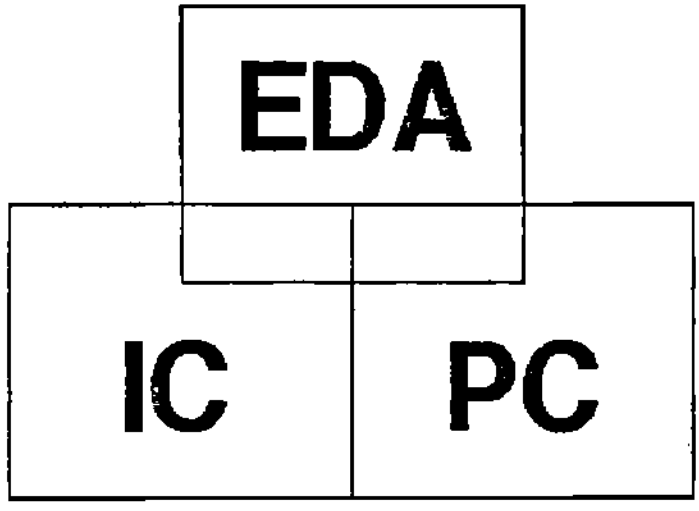
ELECTRONIC CAD/CAM SEGMENTS



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SPEC

DESIGN & ANALYSIS

FC GA SC PC

VERIFICATION

ANALYSIS

TEST

↓

MFG

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IC CAD/CAM

- LAYOUT DESIGNER
- PHYSICAL GEOMETRIES
- CENTRALIZED CAD SHOPS
- FULL CUSTOM CIRCUIT
- TYPICALLY HOST-DEPENDENT

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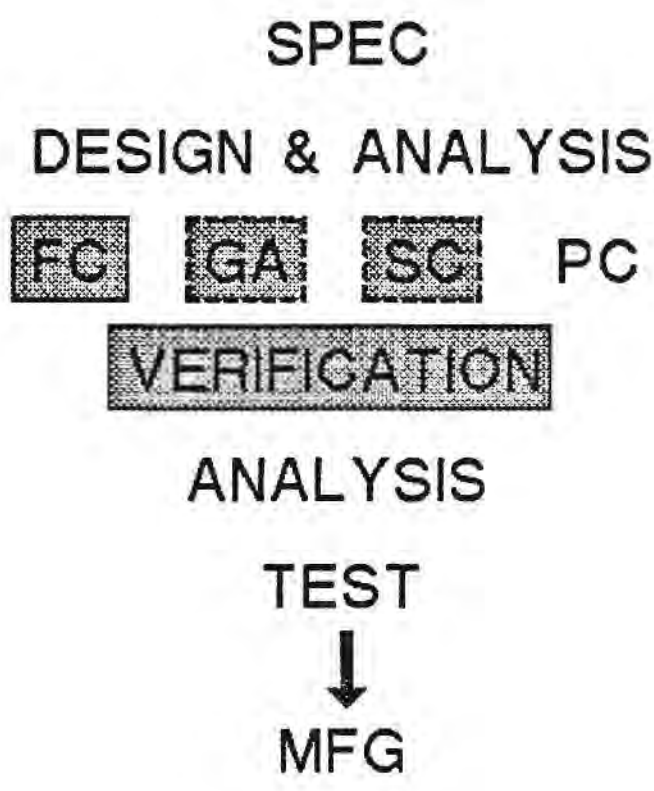

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PCB CAD/CAM

ARTWORK ONLY

- DRAFTING PERSONNEL
- ARTWORK CREATION
- CENTRALIZED CAD SHOP
- STANDALONE OR HOST-DEPENDENT

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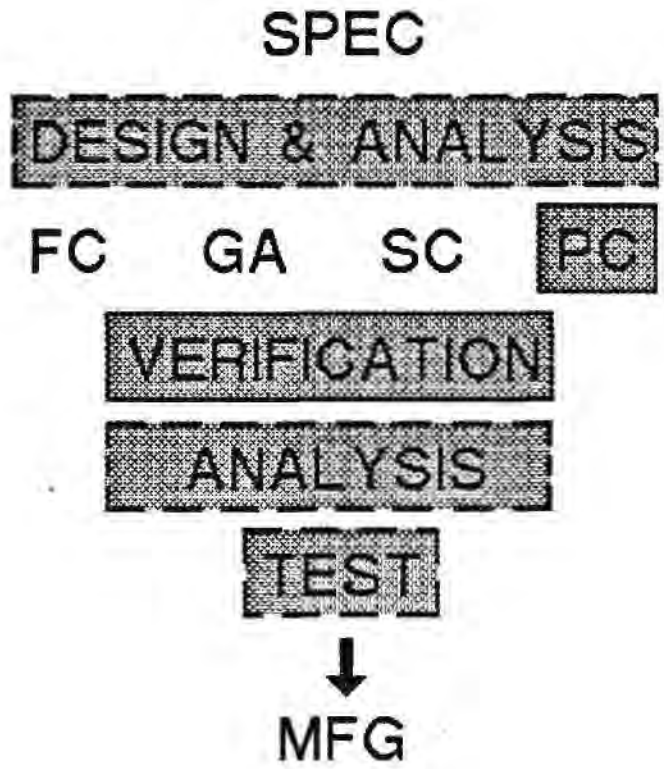
PCB CAD/CAM

COMPREHENSIVE

- ELECTRICAL ENGINEER
- SCHEMATIC CAPTURE
- DECENTRALIZED
- TYPICALLY STANDALONE



EDA

- ELECTRICAL ENGINEER
- LOGIC AND CIRCUIT DESIGN AND ANALYSIS
- PHYSICAL LAYOUT
- DECENTRALIZED
- STANDALONE

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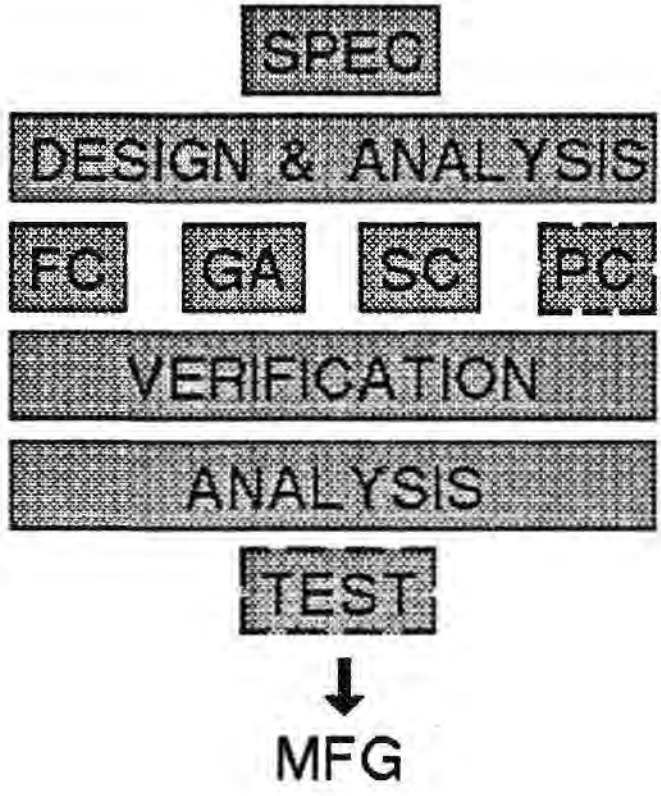

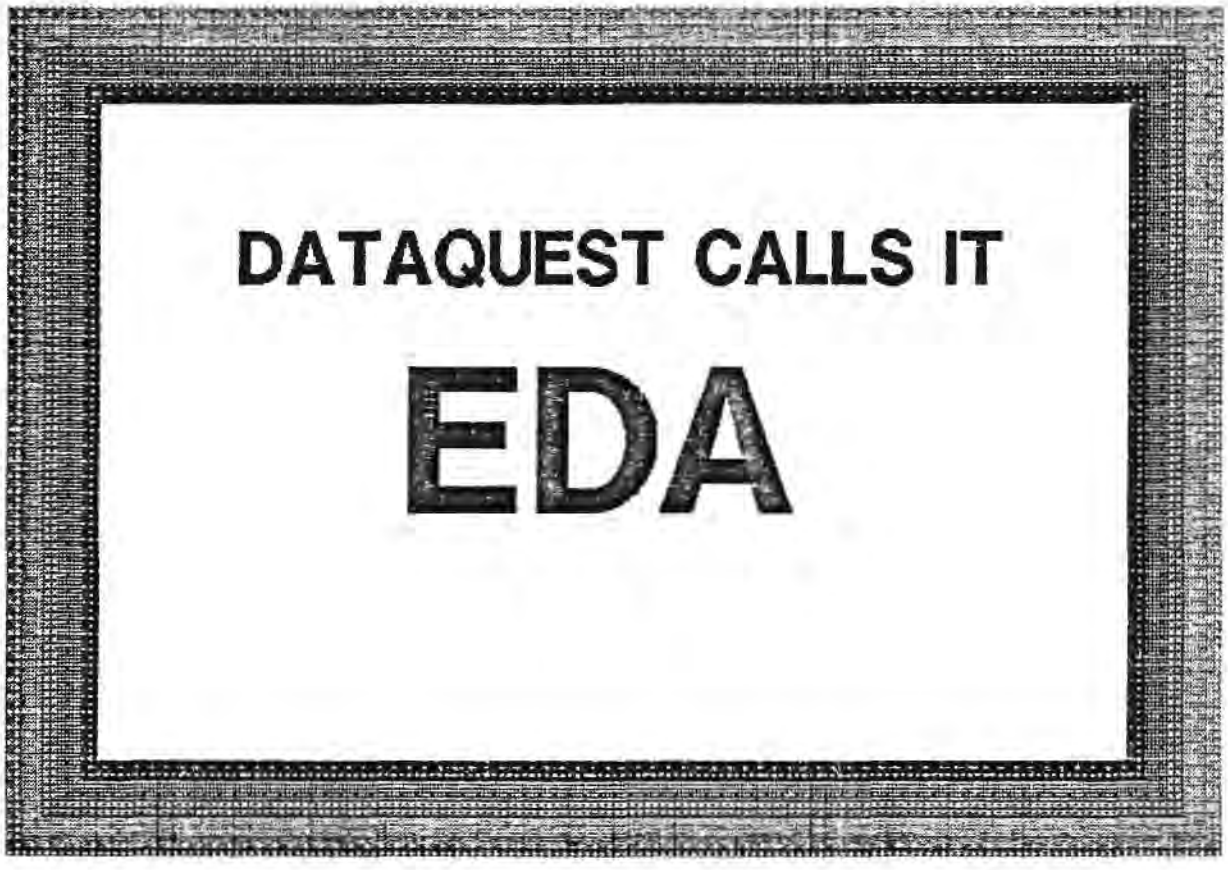

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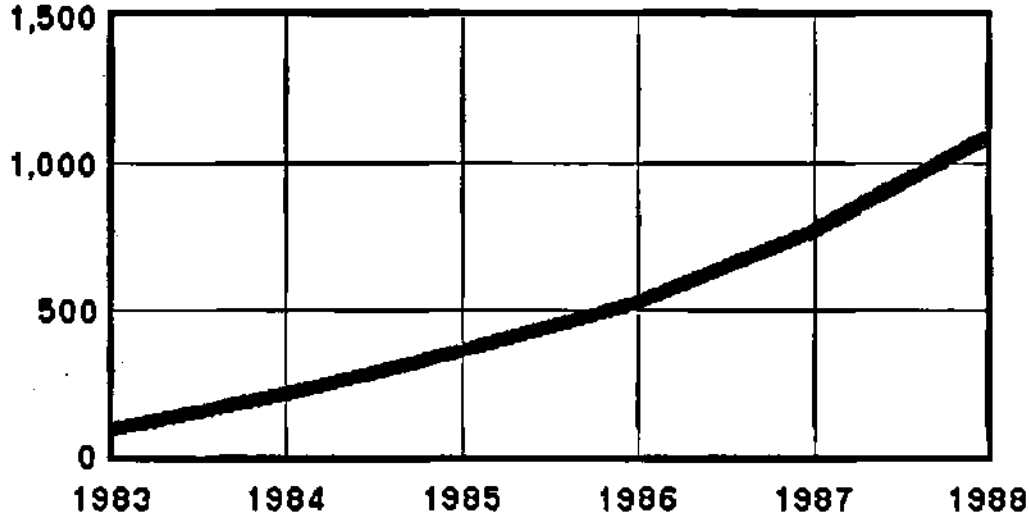
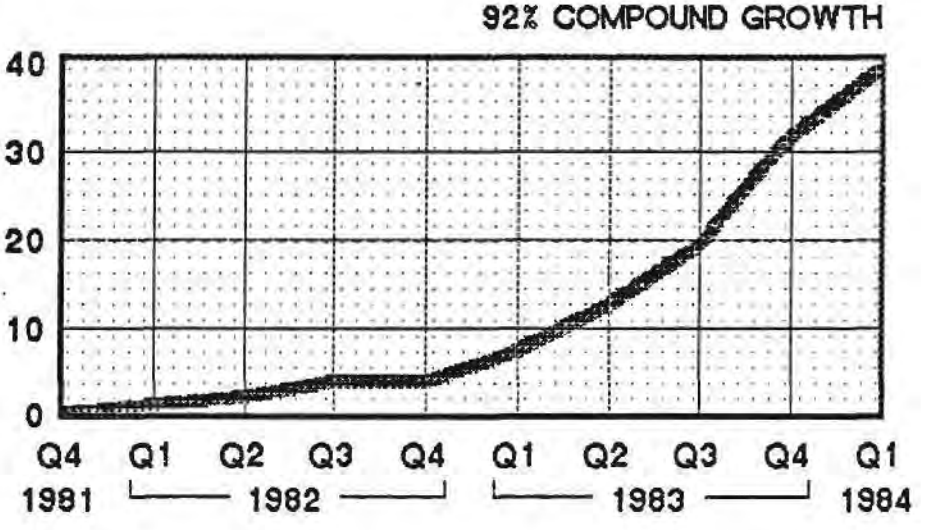
EDA MARKET ESTIMATES

(Millions of Dollars)



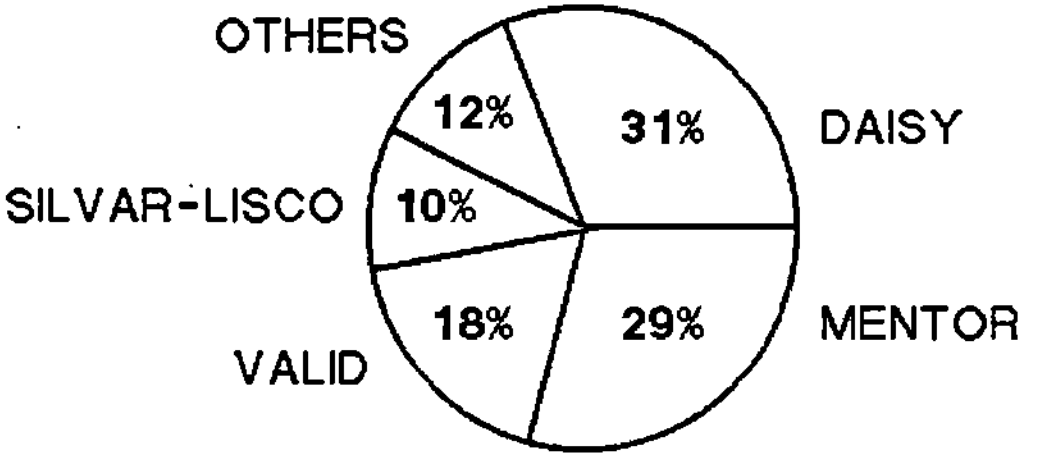
Source: DATAQUEST

EDA QUARTERLY SALES
DAISY, MENTOR, VALID
(Millions of Dollars)



Source: DATAQUEST

1983
MARKET SHARE ESTIMATES



Source: DATAQUEST

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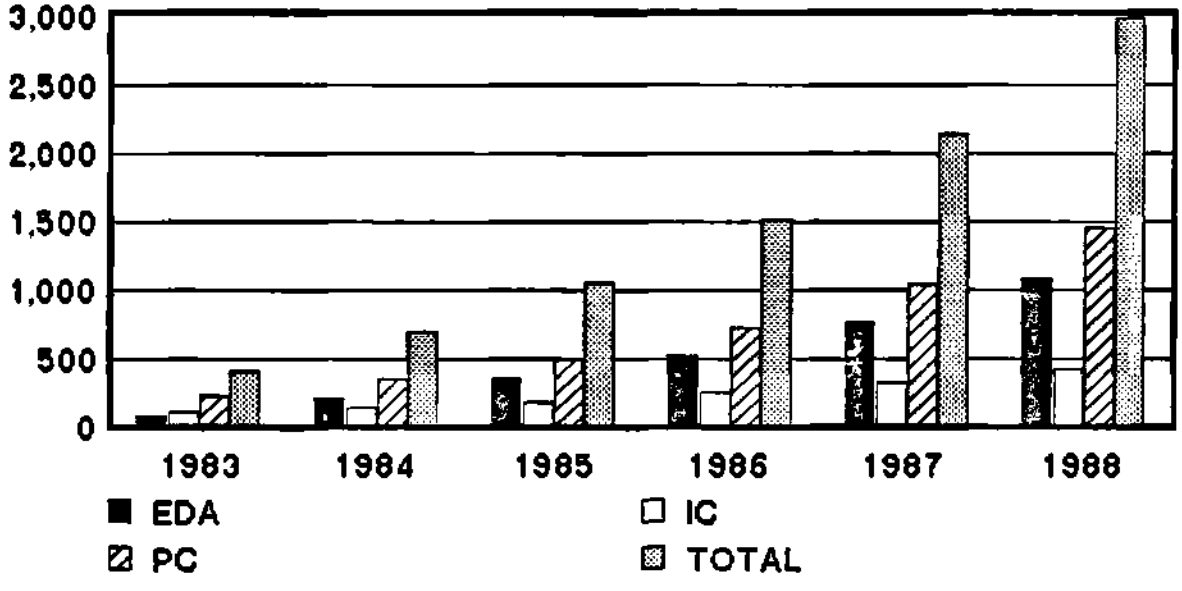
ELECTRONIC CAD/CAM MARKET ESTIMATES

(Millions of Dollars)



Source: DATAQUEST

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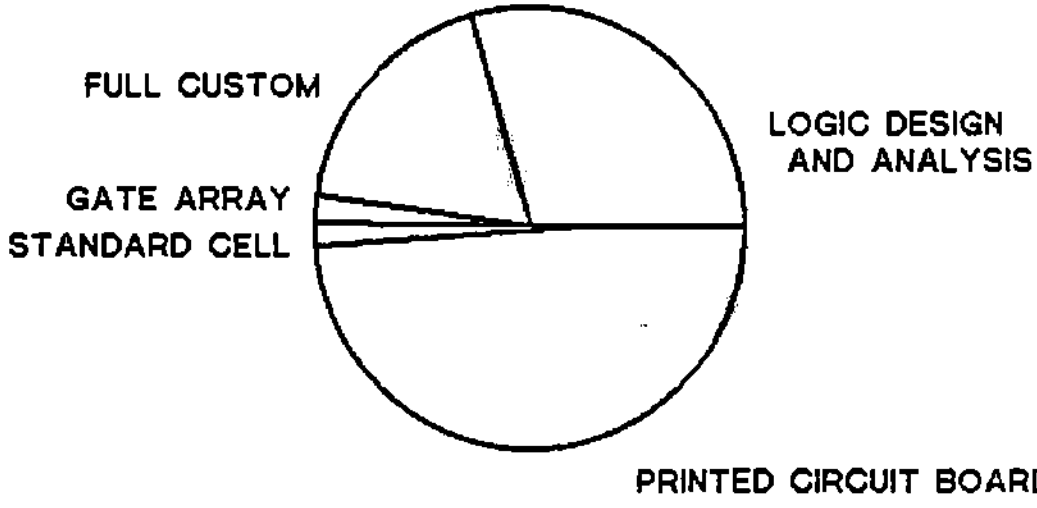
1983
ELECTRONIC CAD SYSTEM USAGE
(Workstation Units)



Source: DATAQUEST

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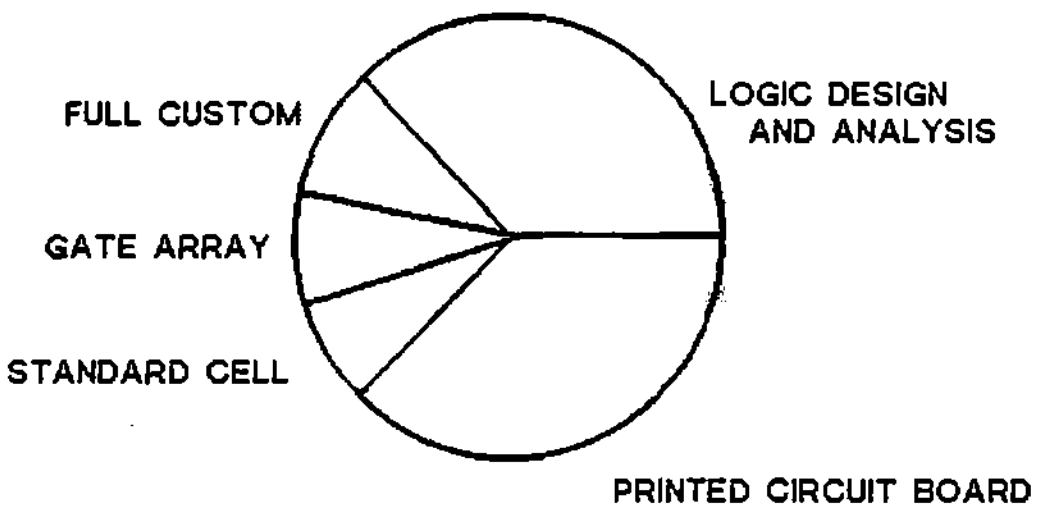
1988
ELECTRONIC CAD SYSTEM USAGE
(Workstation Units)



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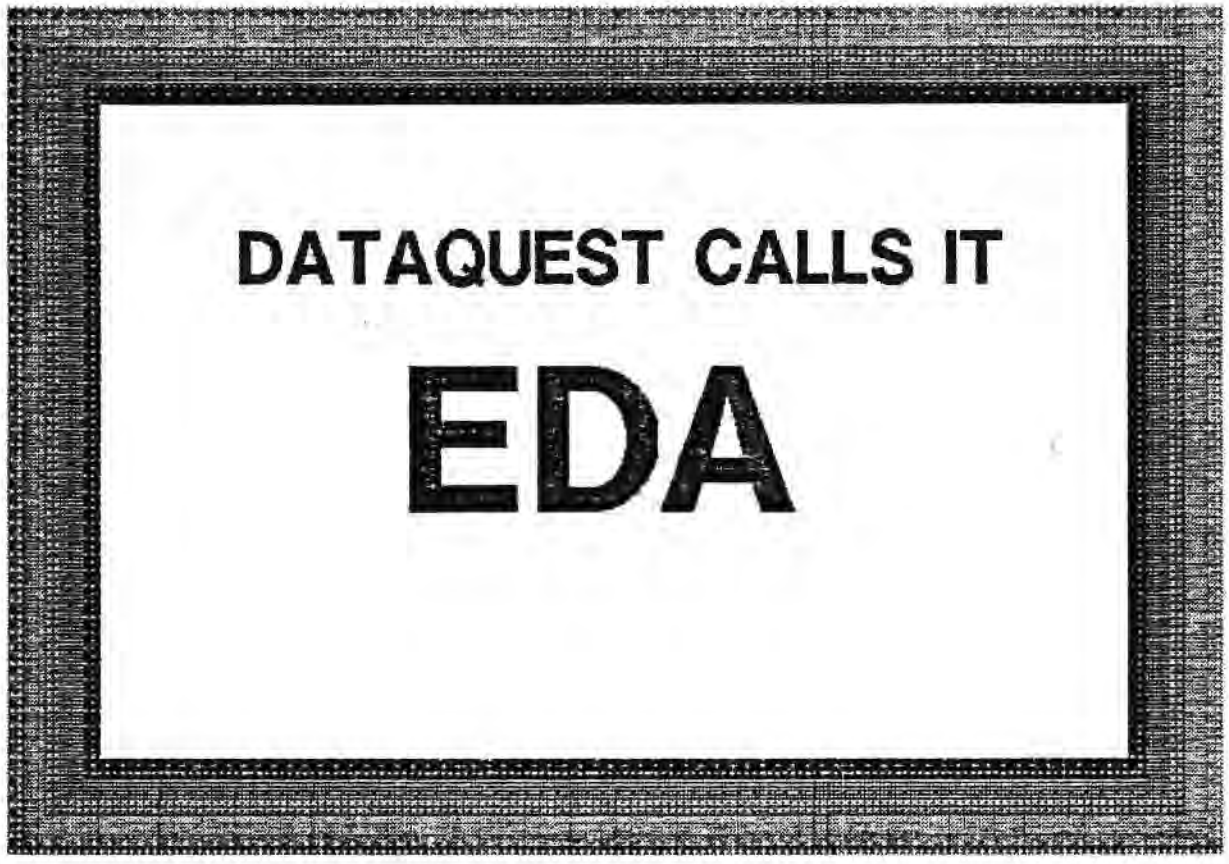

DRIVING FACTORS

- CIRCUIT COMPLEXITY

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DRIVING FACTORS

- CIRCUIT COMPLEXITY
- SEMICUSTOM CIRCUITS

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DRIVING FACTORS

- CIRCUIT COMPLEXITY
- SEMICUSTOM CIRCUITS
- HARDWARE TECHNOLOGY

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TRENDS

- MARKETING/SALES

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TRENDS

- MARKETING/SALES
- FUNCTIONALITY

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TRENDS

- MARKETING/SALES
- FUNCTIONALITY
- INTERFACES

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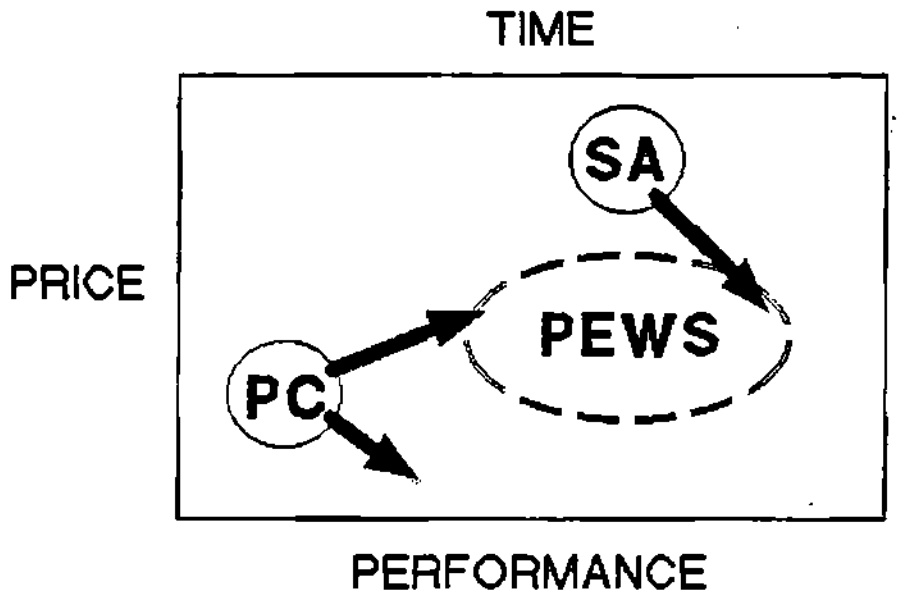
TRENDS

- MARKETING/SALES
- FUNCTIONALITY
- INTERFACES
- APPLICATION-SPECIFIC HARDWARE

TRENDS

- MARKETING/SALES
- FUNCTIONALITY
- INTERFACES
- APPLICATION-SPECIFIC HARDWARE
- PERSONAL ENGINEERING WORKSTATIONS

PERSONAL ENGINEERING WORKSTATIONS



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TRENDS

- MARKETING/SALES
- FUNCTIONALITY
- INTERFACES
- APPLICATION-SPECIFIC HARDWARE
- PERSONAL ENGINEERING WORKSTATIONS
- NICHE APPLICATIONS

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SUMMARY

- TRENDS
- DRIVING FACTORS
- MARKET SIZE
- DEFINITIONS

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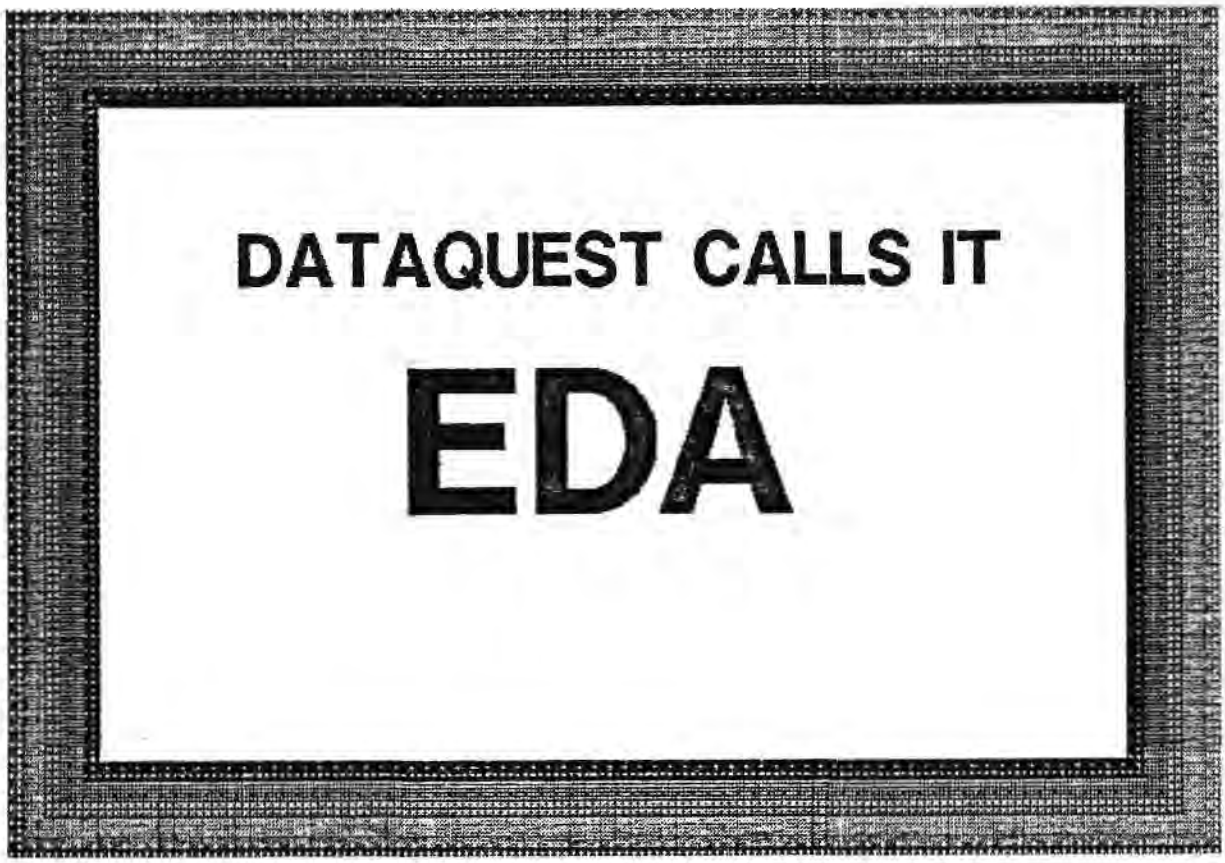

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Nielsen Dataquest

WHAT'S ALL THE EXCITEMENT ABOUT
OR
HOW CAN AN INDUSTRY GROW SO FAST

Gerard H. Langler
Vice President, Marketing
Mentor Graphics Corporation

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Dataquest Incorporated
ELECTRONIC DESIGN AUTOMATION FOCUS CONFERENCE
May 10-11, 1984
Sunnyvale, California

What's All The Excitement About
or
How Can An Industry Grow So Fast

Gerard H. Langeler
MENTOR GRAPHICS CORPORATION
8500 S.W. Creekside Place
Beaverton, Oregon 97005-7191
(503) 626-7000

The market for Computer Aided Engineering products didn't exist in 1981, yet many industry observers predict a market size of over $1 billion by 1987! How can an industry grow so fast?

To answer this question we need to look at what is fueling the growth, and just as importantly the limits to growth. By focusing our attention on the limits to growth, we can determine whether all this euphoria is realistic or whether this market is just a high technology flash in the pan.

The limits to growth for any industry or company are a direct function of both internal and external elements. Internal limits center on such things as cash position, manufacturing capacity, market coverage, management ability and something the Boston Consulting Group calls the "Maximum Sustainable Growth Rate" which is approximated by return on net assets minus the interest rate on debt times the debt to equity ratio. External limits are focused on such issues as degree of pent-up demand, economic cycles, capital availability and most importantly the return on net assets a customer can expect from newly acquired CAE systems.

It turns out that in the short term (e.g., next one to two years) the limits to growth for the CAE industry are largely internal, not external! While the significant CAE players are public companies with excellent cash positions, and all have such large capitalizations that return on assets is not yet a meaningful number, the other internal limits are very much in play.

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Dramatically lengthening semiconductor lead times put an artificial constraint on manufacturing capacity in the short term. The leading CAE companies have relatively small sales and support organizations (though growing fast) so market coverage limits industry growth at present. Finally, some CAE companies have the management experience and depth to handle over $100 million in sales, growing at over 100% per year. Some will struggle under such pressure.

In contrast, there are few external limits to growth in the short term. There is a large amount of pent up demand, stemming from years of "shoemaker's children" phenomena among electronic engineers. We are in the middle of a strong upturn in the business cycle, led by capital spending.

Over the long term, the more enduring factors of return on investment come into play. Given the very high software content to the vlaue added portion of the business, internal return on net assets is likely to be quite high. Coupled with the traditional aversion to debt by successful high technology firms, the maximum sustaninable growth rate for leading CAE firms is likely to remain quite high.

The real limit to long term growth in this industry will be found in the return on investment customers experience when they purchase a CAE system. Most customers focus on measuring productivity gains to determine the value of their investment. While productivity gains are very important in terms of a shorter time to market serving to lower costs and improve market share, there is a larger mostly unrecognized factor - price flexibility.

If you give me a choice of getting to market three months early, or getting there on time with product innovation able to support a 5% or 10% higher price, I will normally choose the second option. CAE systems which not only promote productivity but also provide tools for innovation allow for such gains.

This kind of thinking can lead to sophisticated analysis which can prove beyond a shadow of a doubt that CAE is a good investment, often yielding 50% to 100% annual return on investment. However, even this may pale in comparison to the real return on CAE-survival. It is the

impression of many people (not just vendors) that failure to adopt CAE tools will spell economical doom for any firm competing in the fast moving electronics industry. With that attitude the growth potential for leading CAE firms is indeed spectacular.

So, how fast can the industry really grow? Our best estimates are 200%-300% in 1984. 40%-70% per year in the 1985-1990 time frame and at least 25% to 35% per year during the 1990's.

Along the way, you are going to see some interesting changes. First of all, during 1984 and 1985 some of the walking wounded will stop walking. Some will just go away, others will merge or get acquired. For the long term leaders, look to Mentor Graphics, Daisy, one of the instrument companies (probably Hewlett-Packard) and one of the CAD/CAM companies (probably Computervision).

Rapid growth and rapid change, it makes for a most exciting business.

/tp

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WHAT'S ALL THE EXCITEMENT ABOUT?

or

HOW CAN AN INDUSTRY GROW SO FAST?

Gerard H. Langeler
Mentor Graphics Corp.

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LIMITS TO INDUSTRY GROWTH

A. Internal

B. External

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INTERNAL (COMPANY) LIMITS TO GROWTH

1. Short term
   a. Cash
   b. Manufacturing capacity
   c. Market coverage

2. Long term
   a. Maximum sustainable growth rate (RONA - INTEREST ON DEBT)
   b. Management ability

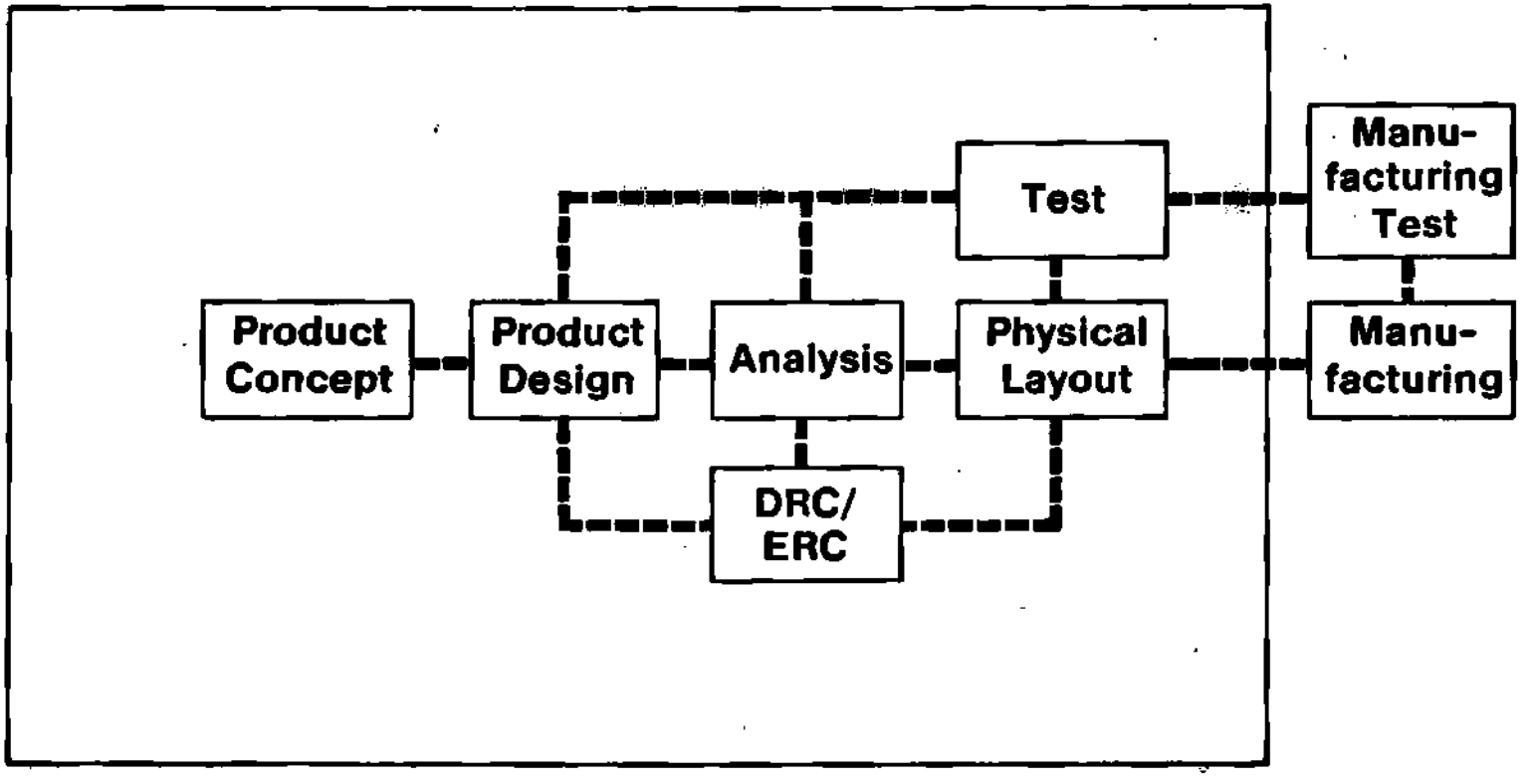
EXTERNAL (MARKET) LIMITS TO GROWTH

1. Short term
   a. Degree of pent up demand
   b. Economic cycle

2. Long term
   a. RONA (eg. productivity gains & innovation gains)
   b. Capital availability

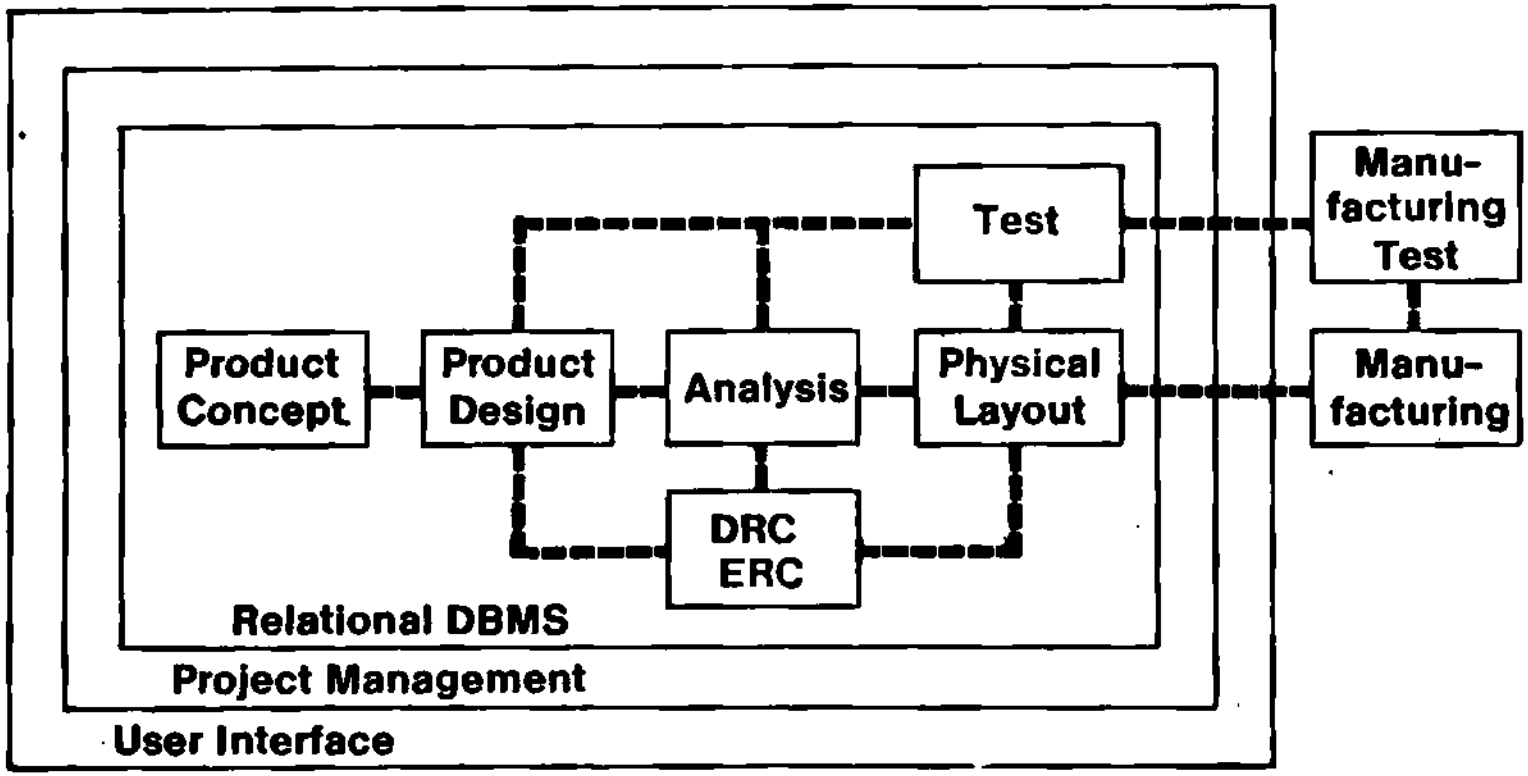
THE MENTOR GRAPHICS GOAL

"Enable its customers to compete better by improving productivity and innovation in electronics design."

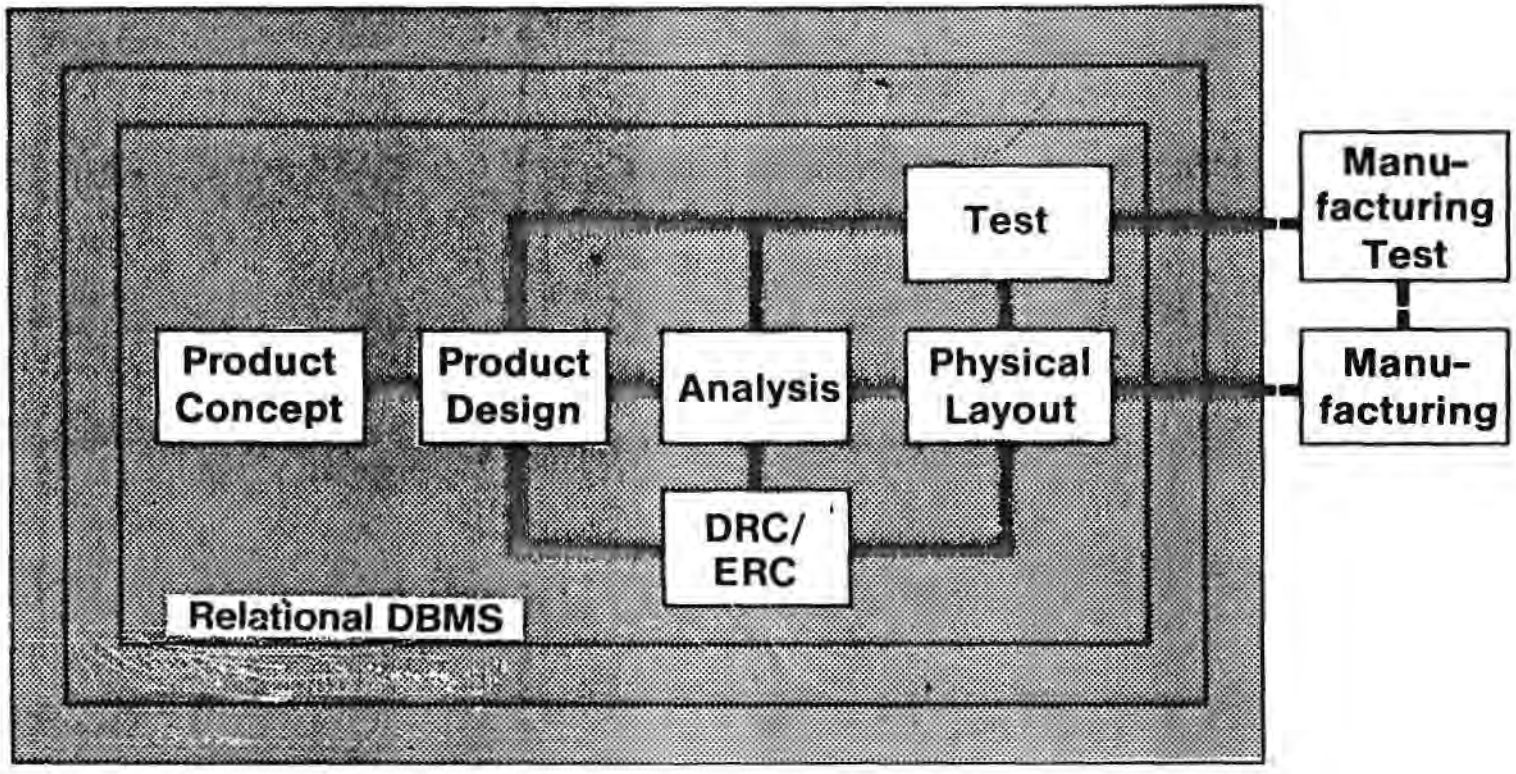


MENTOR GRAPHICS TOOLS ADDRESS

- Custom IC Design
- Standard Cell Design
- Gate Array Design
- PCB/Systems Design



DATABASE MANAGEMENT IS AS IMPORTANT AS THE DESIGN PROCESS ITSELF



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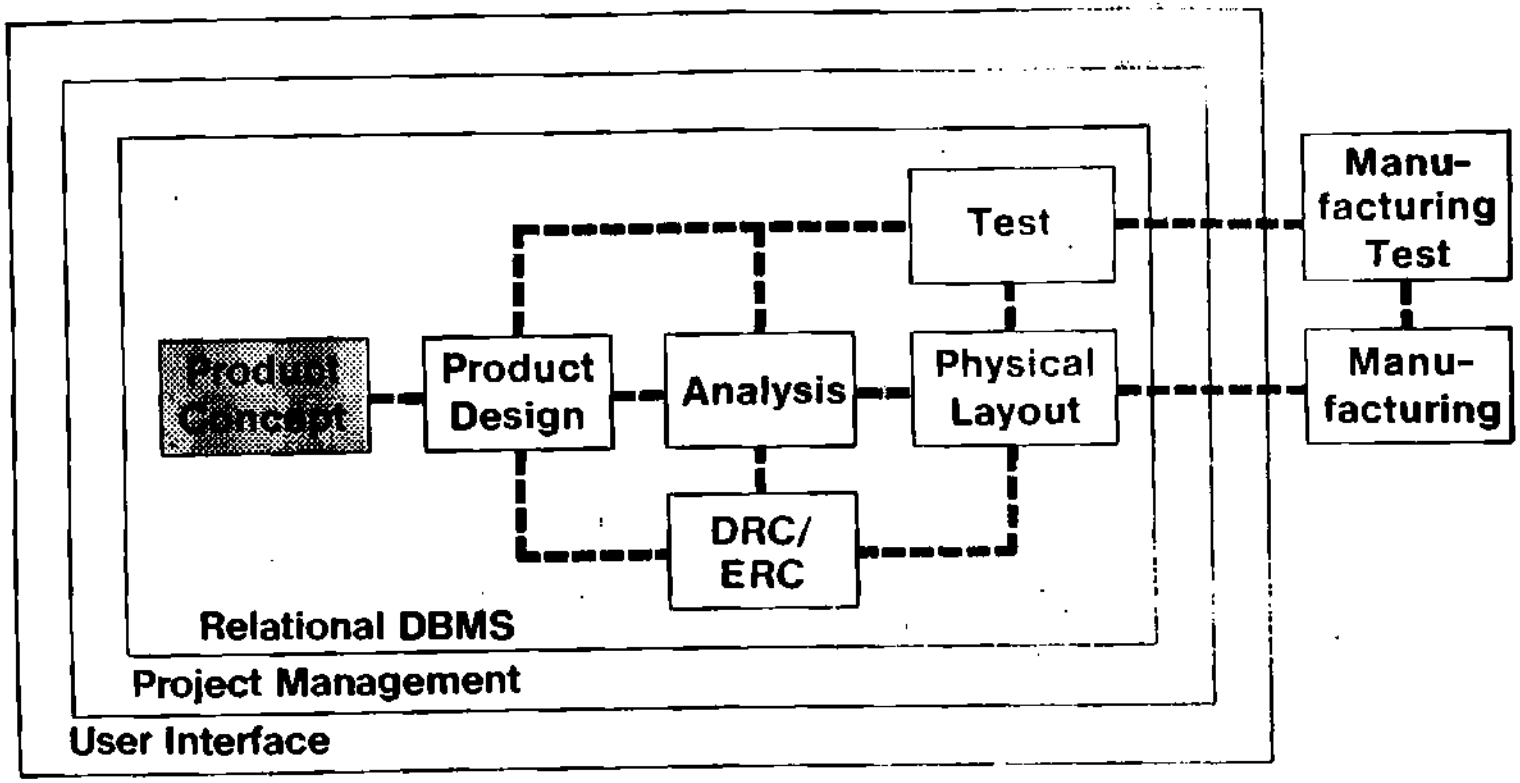
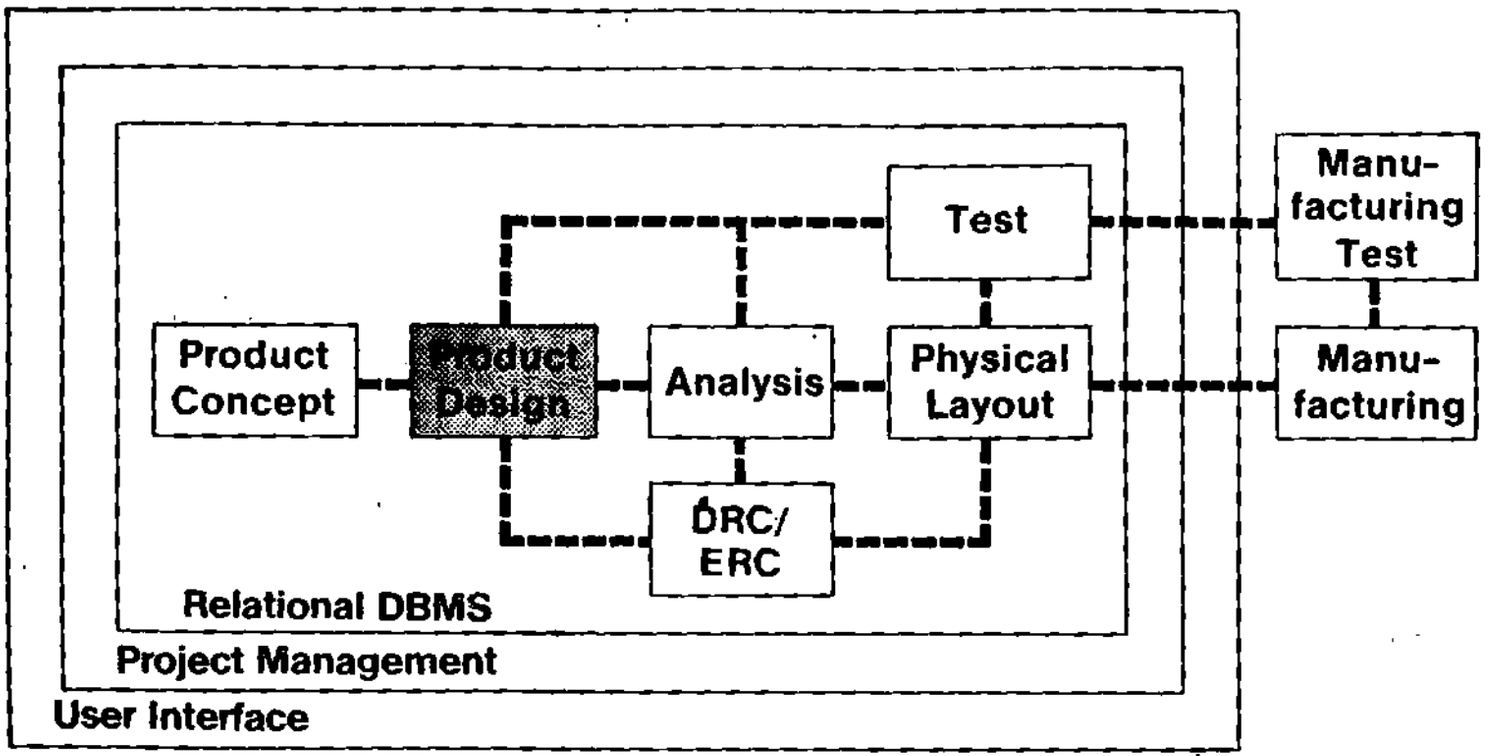
CONCEPTUAL DESIGN

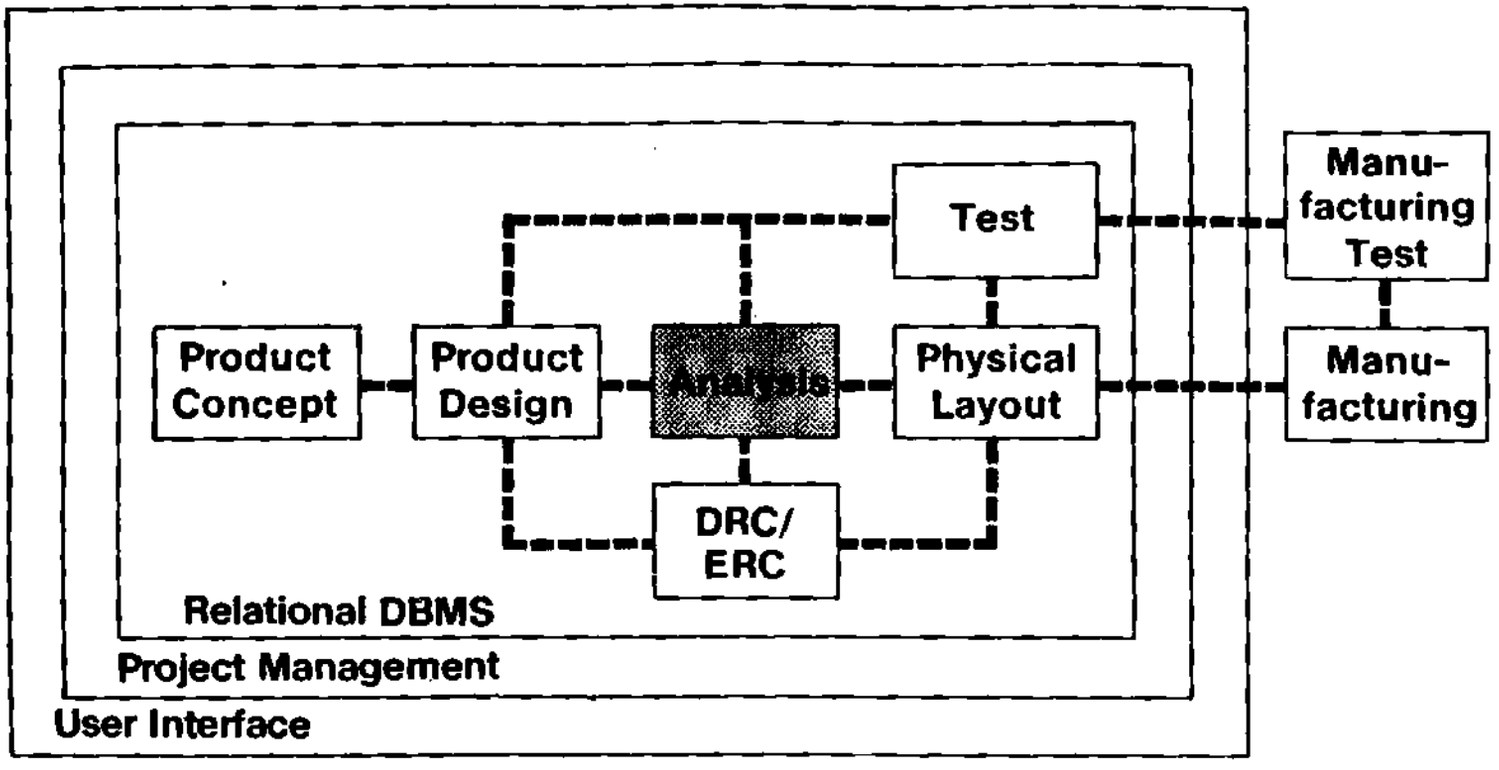
The difference between engineering and schematic drawing.



DESIGN TOOLS: THE EFFICIENT MEANS TO AN EFFECTIVE PRODUCT



ANALYSIS TOOLS: WHAT ENGINEERS REALLY CARE ABOUT



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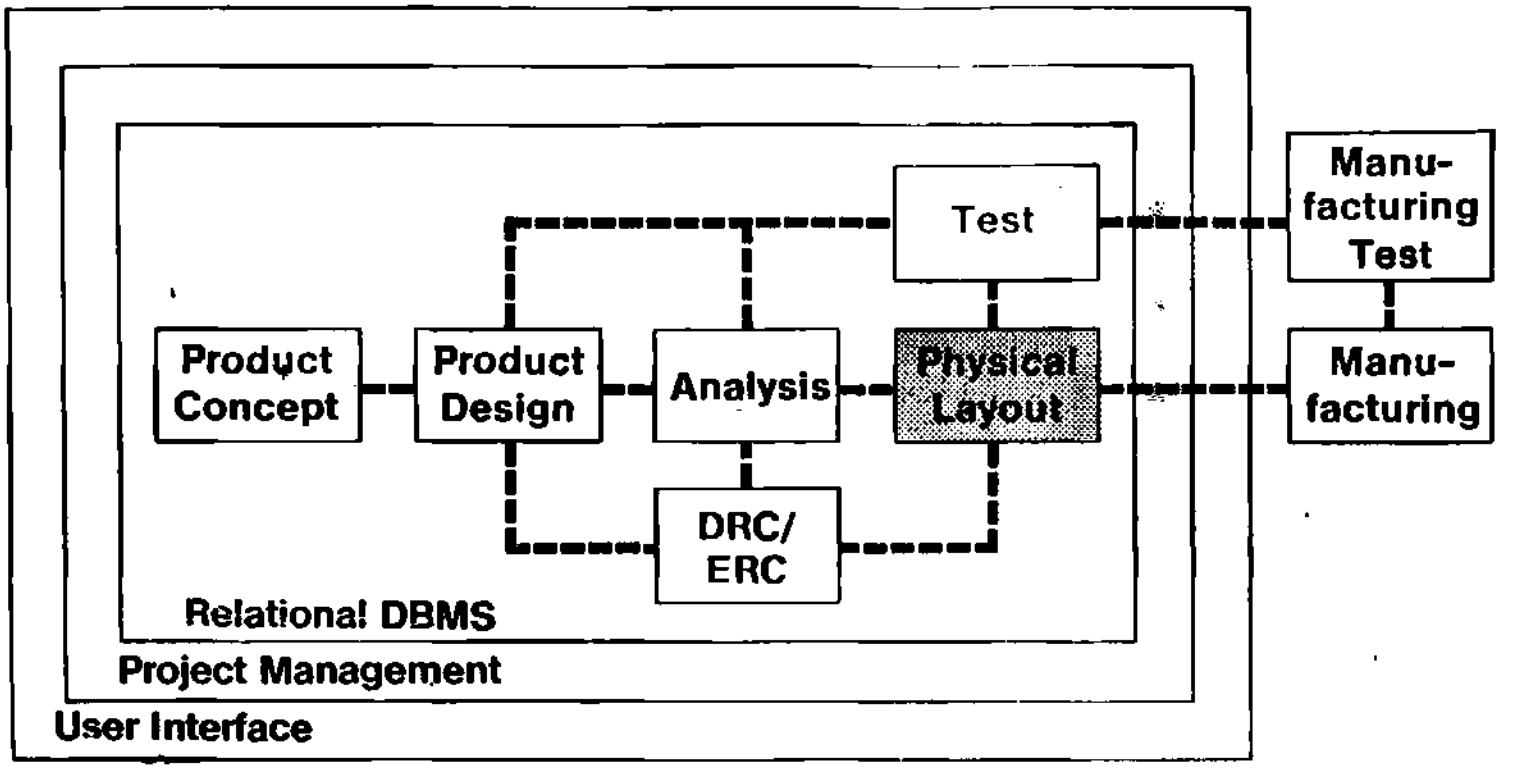
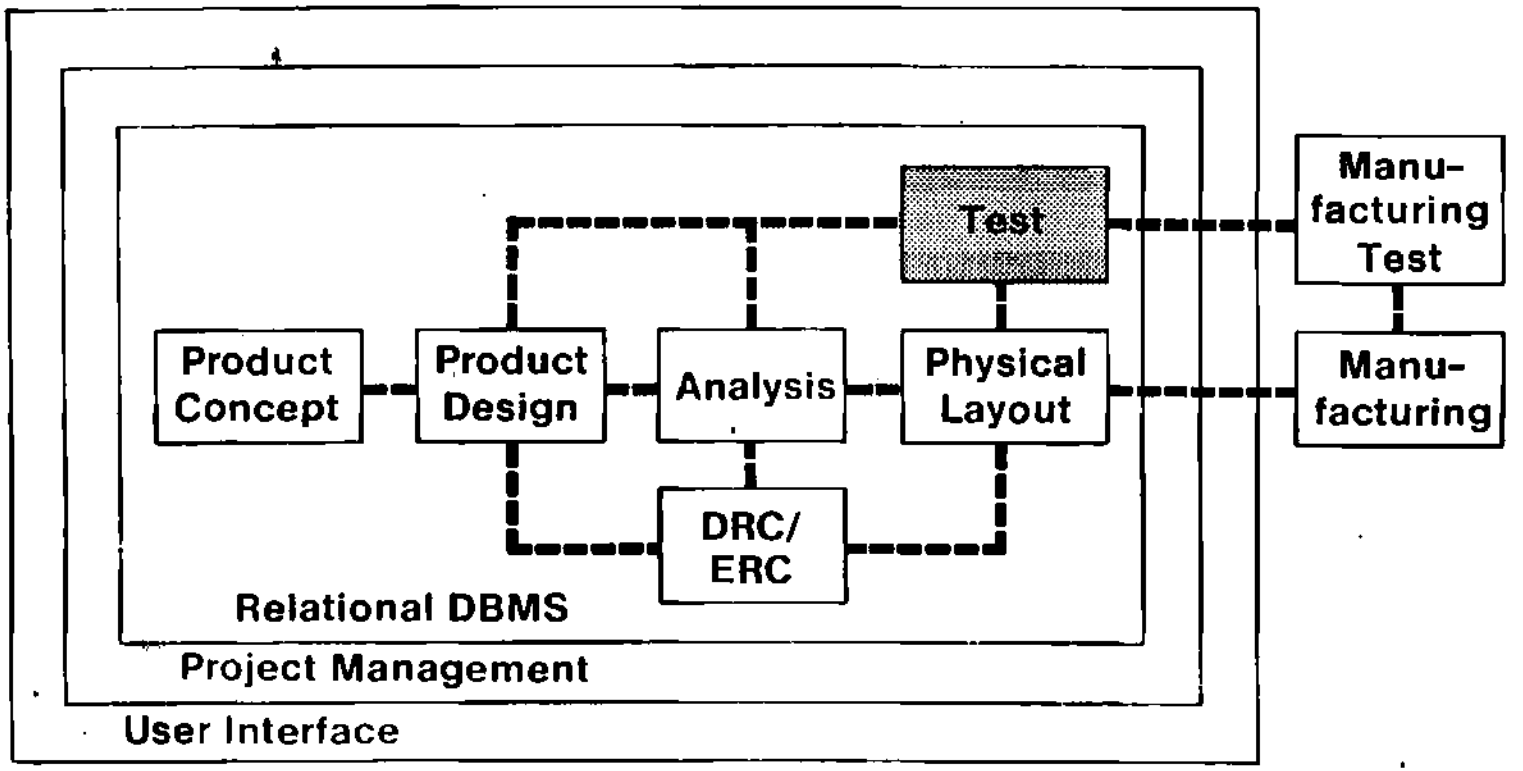
PHYSICAL LAYOUT TOOLS

Taking theory to reality.

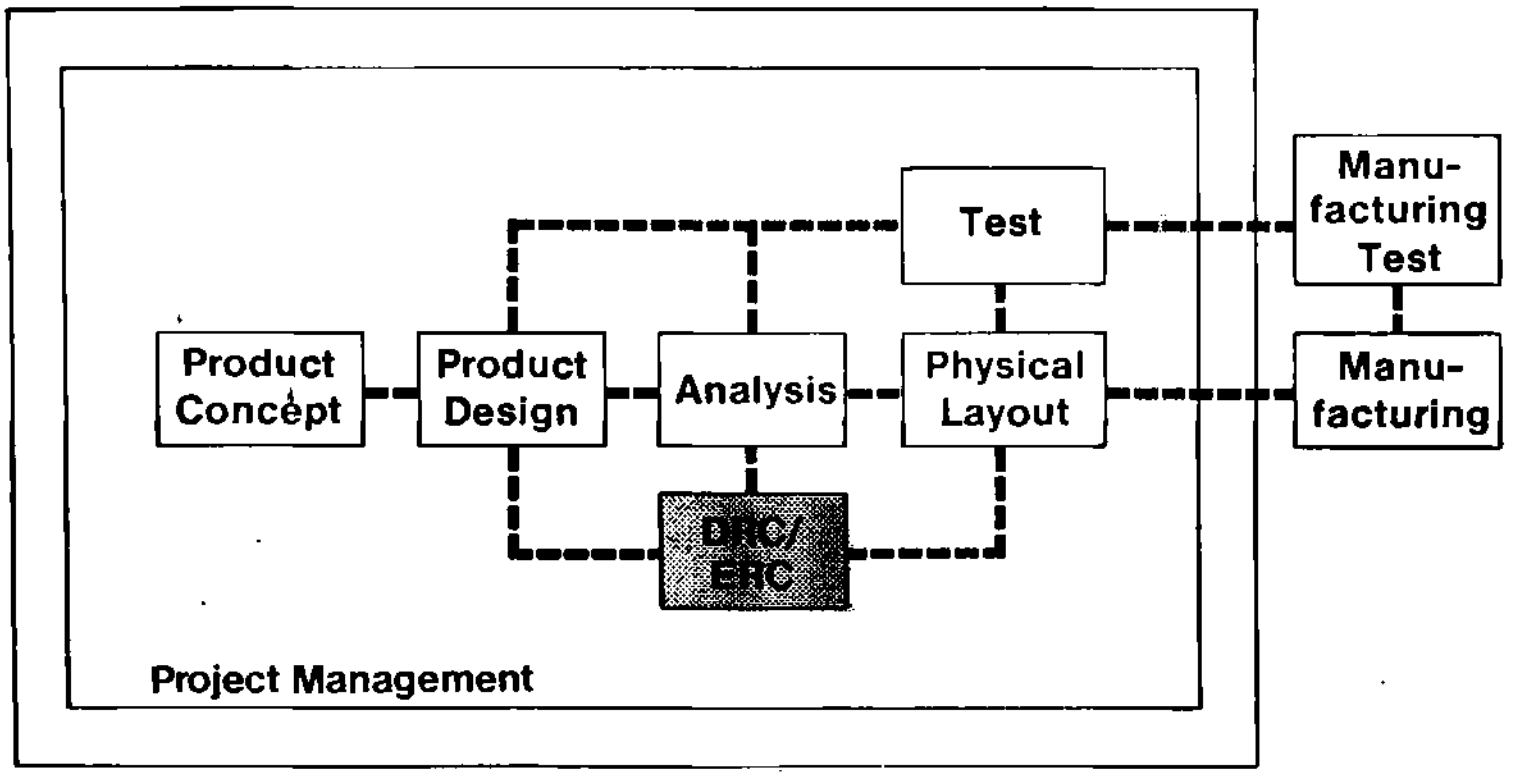


TEST AND MEASUREMENT TOOLS: VERIFYING THE END PRODUCT



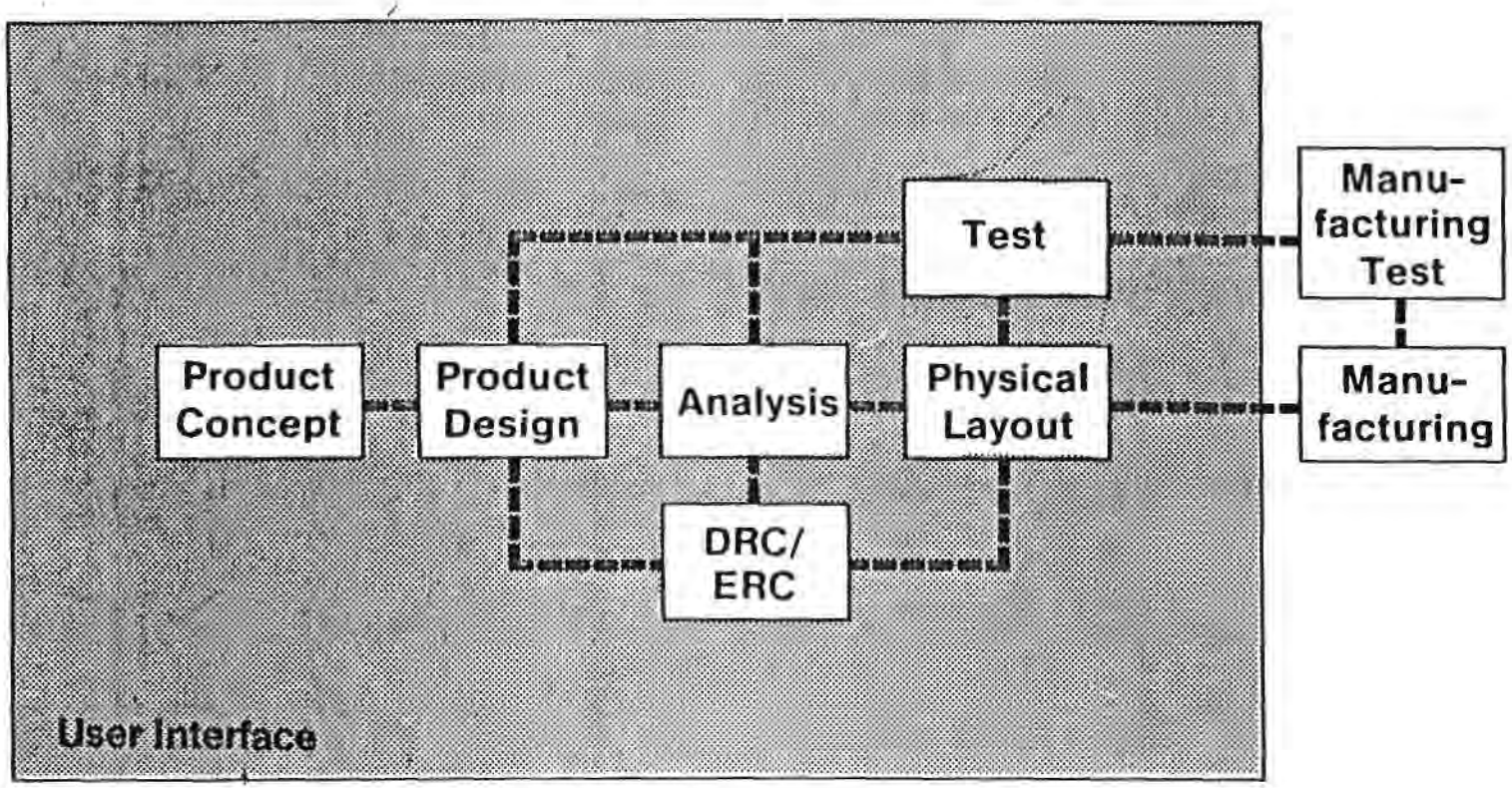
PROJECT MANAGEMENT TOOLS

Covering the 60% of the day engineers spend outside "design engineering".



USER INTERFACE TOOLS

Accessing all tools through a unified portal



CUSTOMER RETURN ON NET ASSETS
(Payback On CAE Systems)

1. Cost savings are nice

2. Time to market reductions are nicer

3. Price flexibility is the largest potential return

WHAT TO WATCH FOR

1. Some dead bodies
2. Some acquisitions/consolidations
3. Continued exciting growth

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WHO WILL LEAD CAE?

Two from current leaders	One from column A	One from column B
Mentor Graphics	Hewlett-Packard	Computervision
Daisy Systems	Tektronix	Calma
	GenRad	Racal-Redac
		Intergraph

HOW FAST CAN CAE GROW?

1984	→	200% - 300%
1985 - 1990	→	40% - 70%
1990's	→	25% - 35%

Nielsen Dataquest

APPLICATION-SPECIFIC HARDWARE

Dr. Jared A. Anderson
President and Chief Executive Officer
Valid Logic Systems, Incorporated

Dr. Anderson is a founder of Valid Logic Systems, Inc. Prior to founding Valid, Dr. Anderson was President, Director, and Chief Executive Officer of Two Pi Corporation. He was also the inventor of Two Pi's 32-bit IBM-compatible minicomputer. Dr. Anderson personally negotiated the sale of Two Pi to N.V. Philips in 1976. Previously, Dr. Anderson was Vice President of Research and Development at Computer Machinery Corporation, a manufacturer of shared-processor data entry systems. Dr. Anderson was also President and co-founder of Decision Inc., a supplier of disk and tape controllers for Data General minicomputers. Before forming Decision Inc., Dr. Anderson headed major research projects involving multidisciplinary teams of scientists, engineers, and contract personnel. Dr. Anderson holds a Ph.D degree in Physics from the University of California at Berkeley, where he participated in a research project that culminated in the awarding of the 1968 Nobel Prize in Physics to Professor Luis W. Alvarez.

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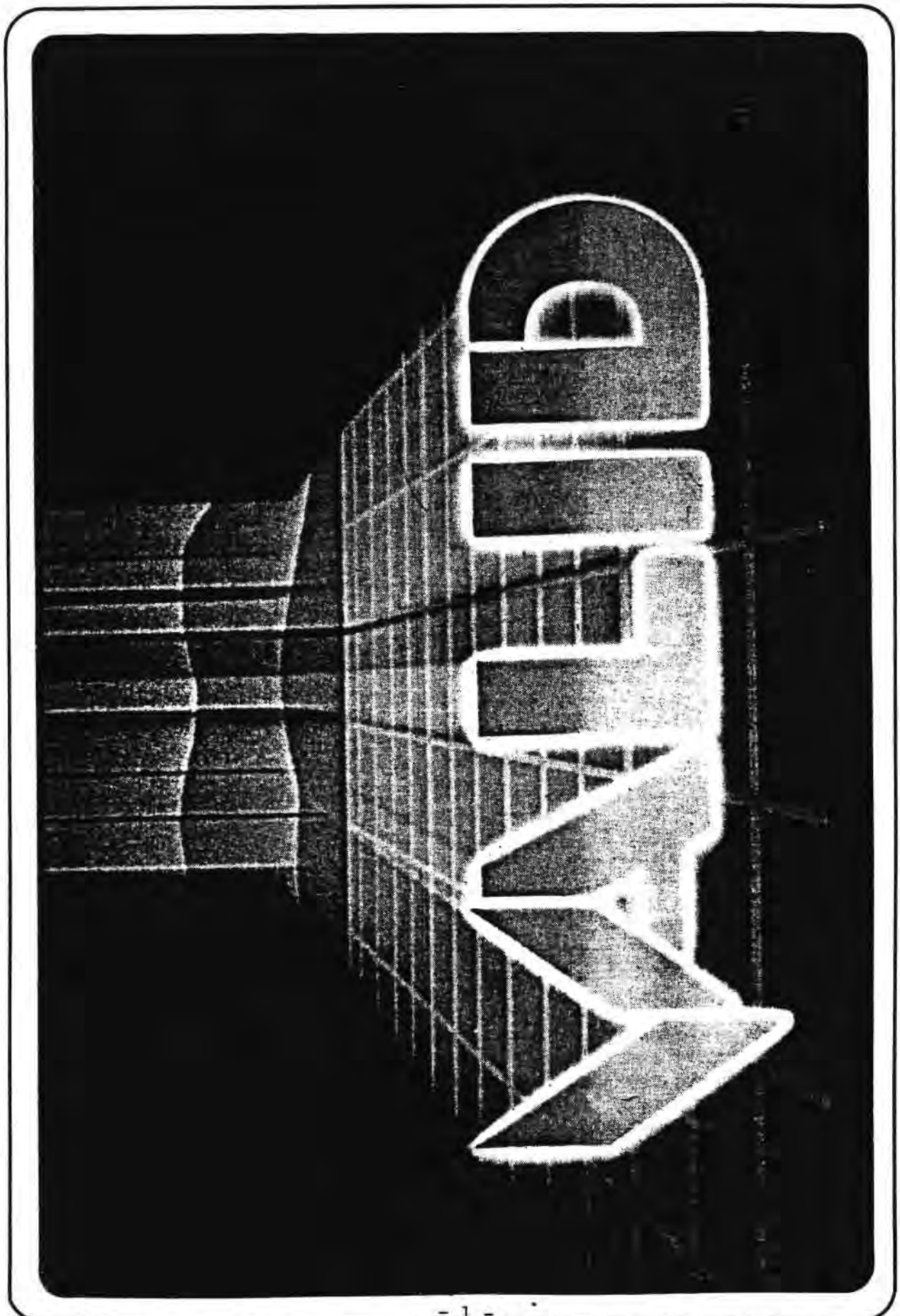
ELECTRONIC DESIGN AUTOMATION FOCUS CONFERENCE
May 10-11, 1984
Sunnyvale, California



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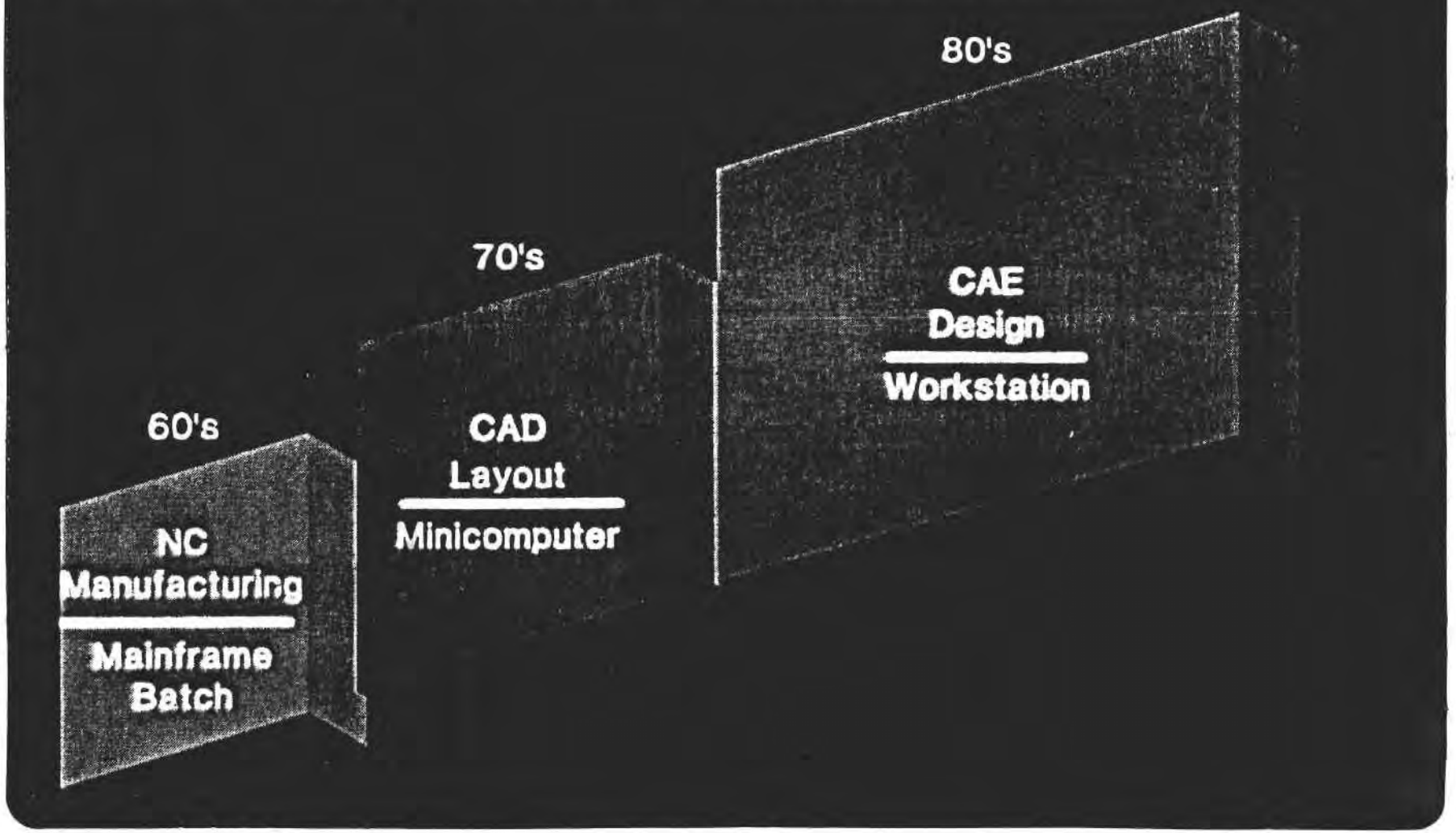
DESIGN AUTOMATION EVOLUTION



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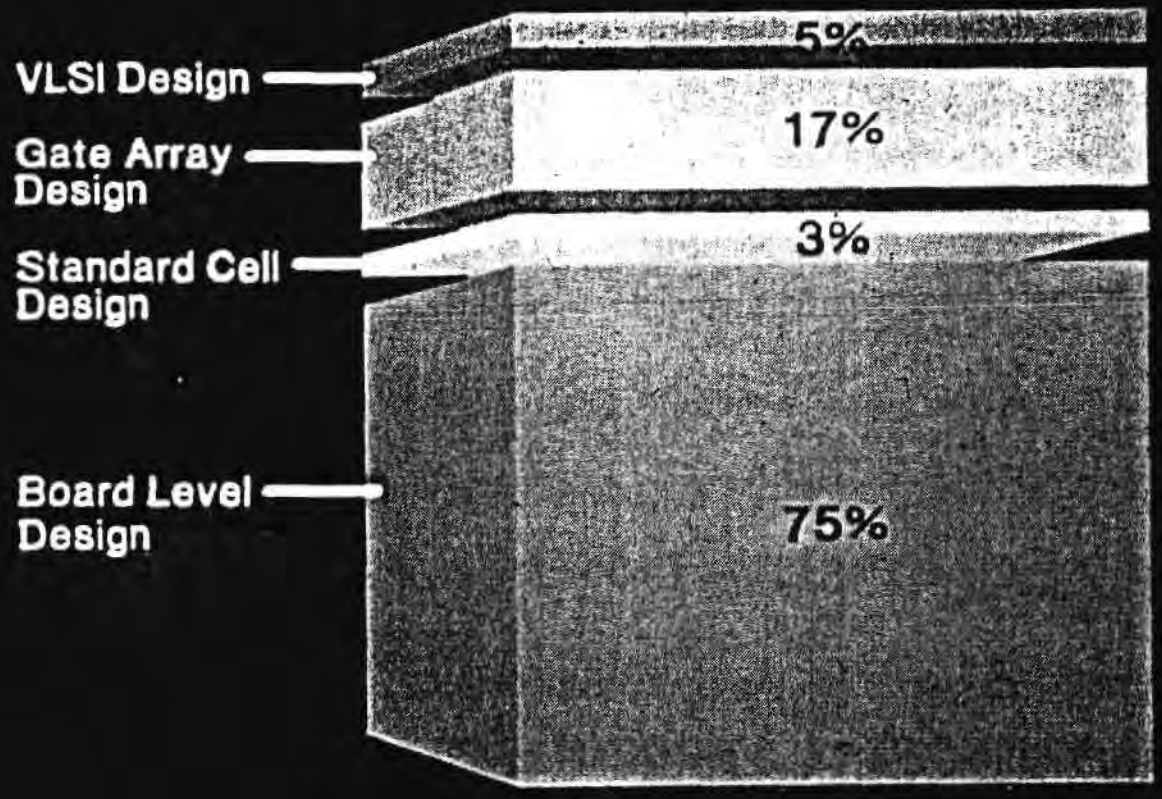
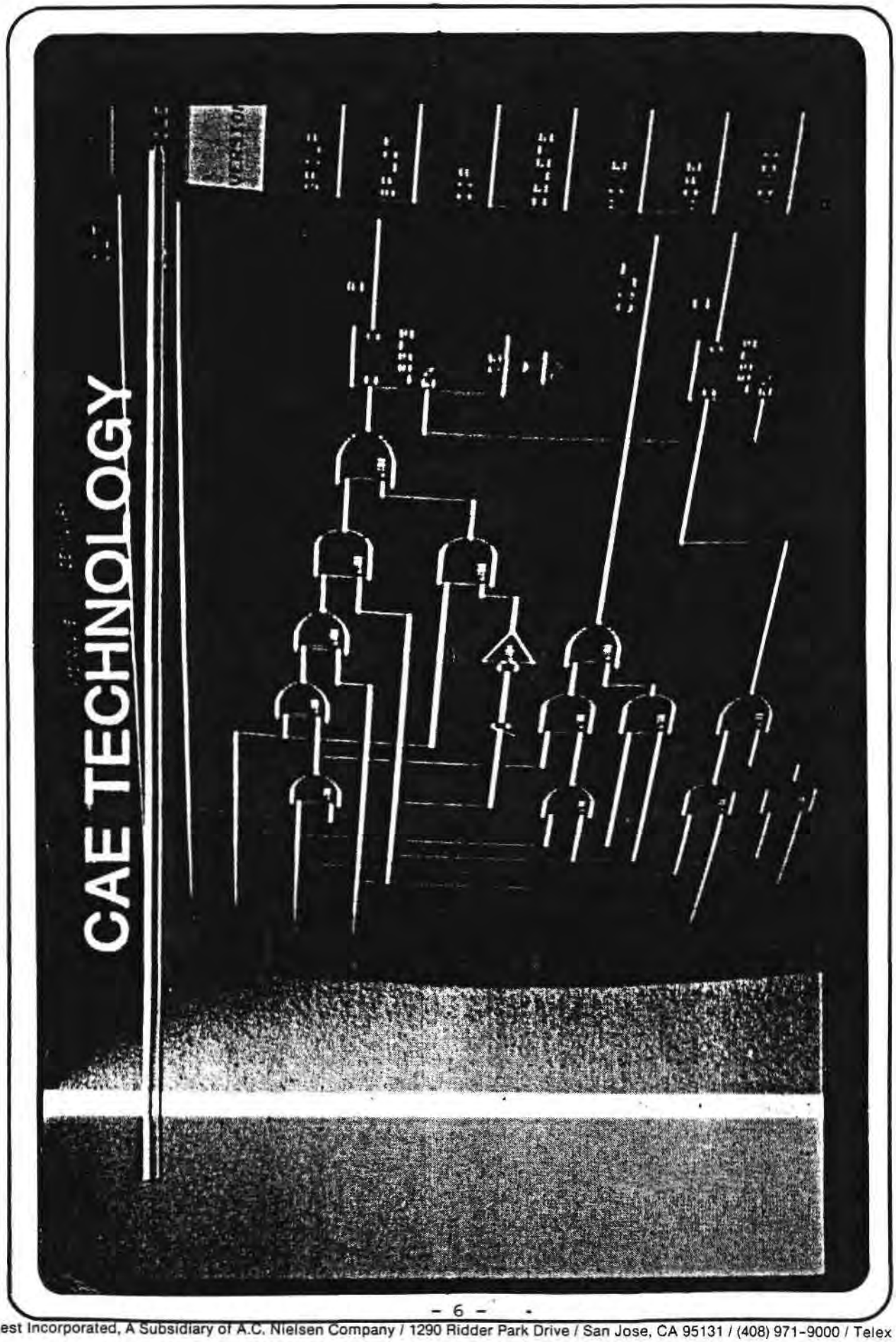
MARKET SEGMENTS





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CAE CAPABILITES

Workstation

Graphics

Analysis

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APPLICATION SPECIFIC WORKSTATIONS

Specialized for Application Programs; e.g. Electronic Design, Mechanical Design, Structural etc.

Significant Speed Improvements Gained By the Addition of Application-Specific Hardware

An Application-Specific Workstation Can Execute the Target Program Faster than a Large Super Computer

840292

VALID

EXAMPLES: ASW's

Speed Improvement of 500 x in Simulation Speed

Valid's Realfast™

Functional Enhancement Allowing Hardware Modeling

Valid's Realchip™

840294

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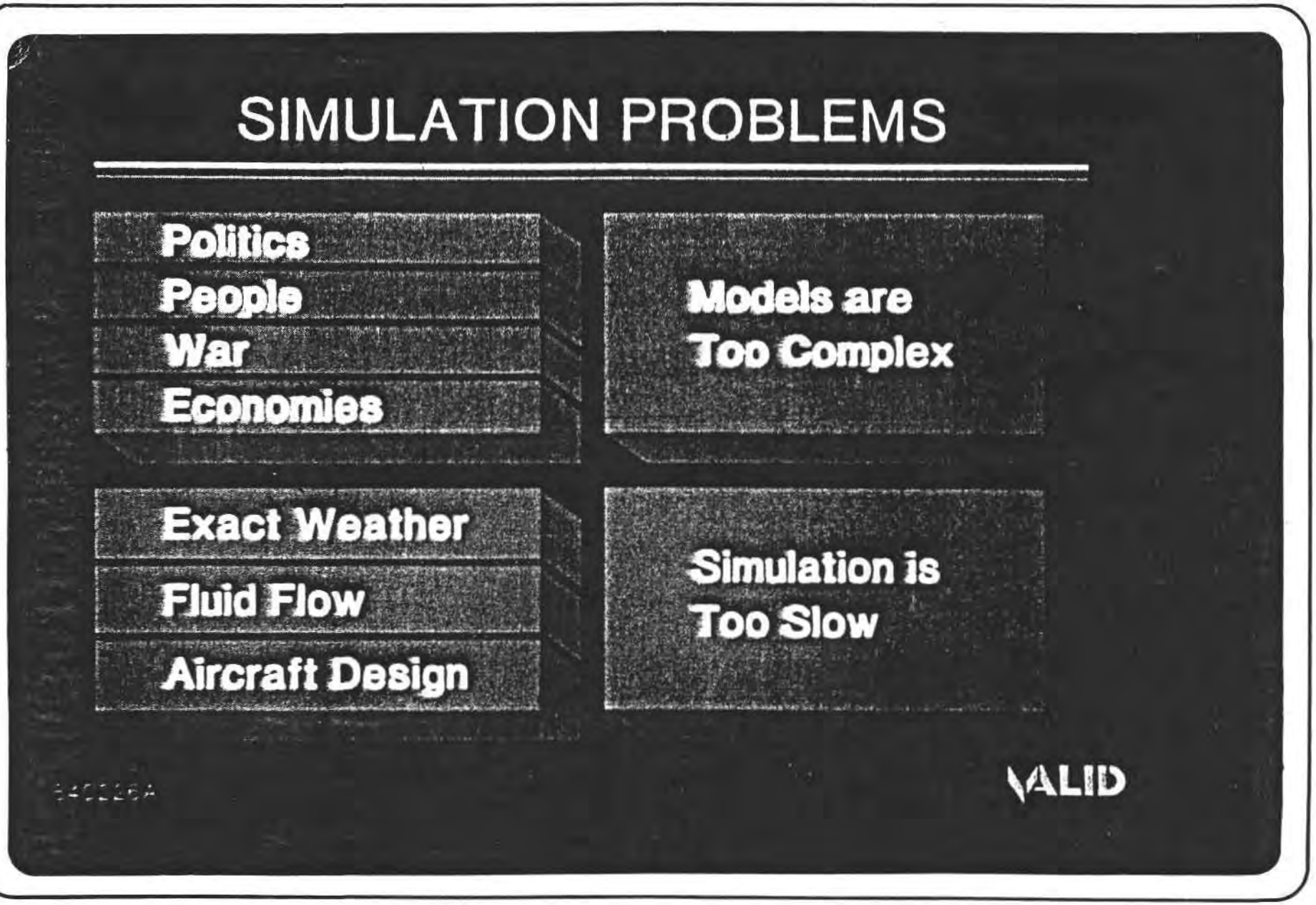

ELECTRONIC SIMULATION
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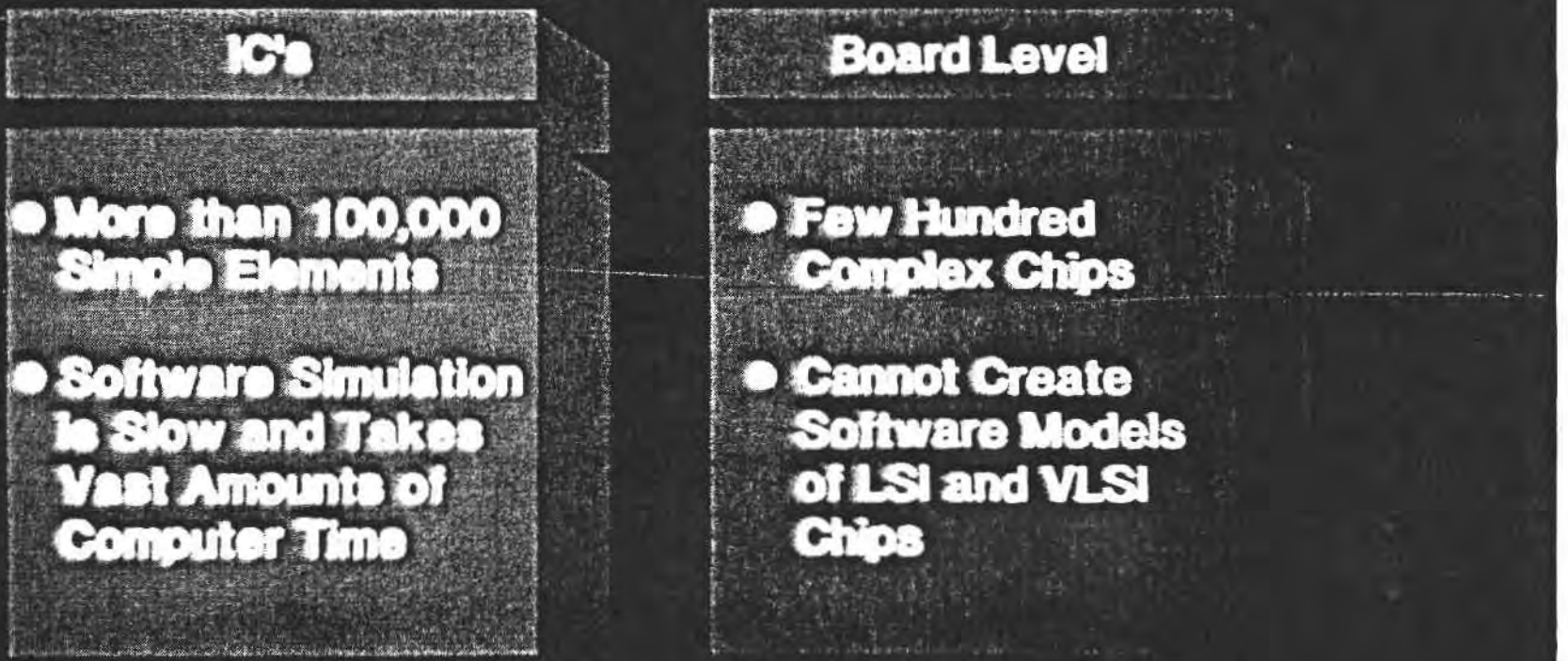
SIMULATION PROBLEMS



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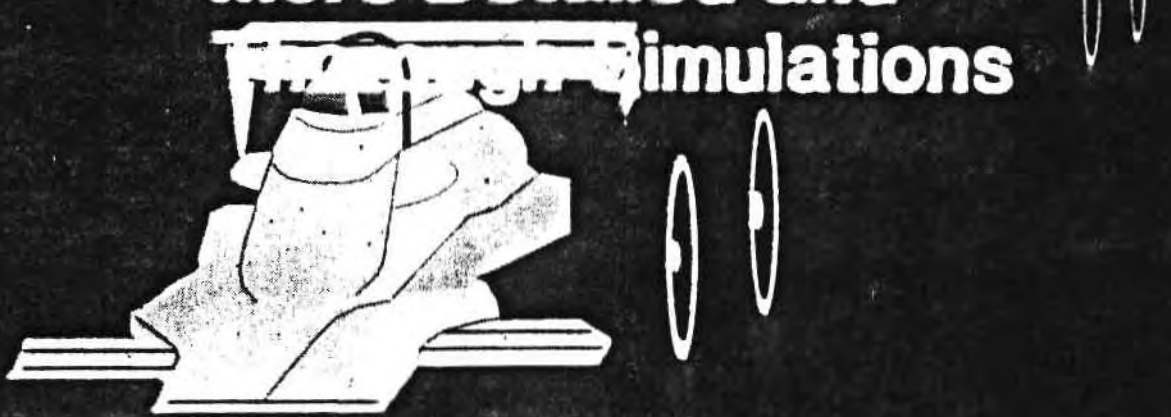
REALFAST™ SIMULATION ACCELERATOR

Purpose: Speed

Result: Allowing Larger, More Detailed and Faster Simulations



840234

VALID

REALFAST™
HOW FAST IS FAST?

Executes 500,000 Circuit Evaluations Per Second

- **Up to 1,000,000 Circuit Elements (Primitives)**

Other Accelerators

- **Daisy's Megalogician**
  - **Comparable Cost**
  - **Five Times Slower**
- **Zycad's Accelerator**
  - **Comparable Speeds**
  - **Five Times the Cost**

840235

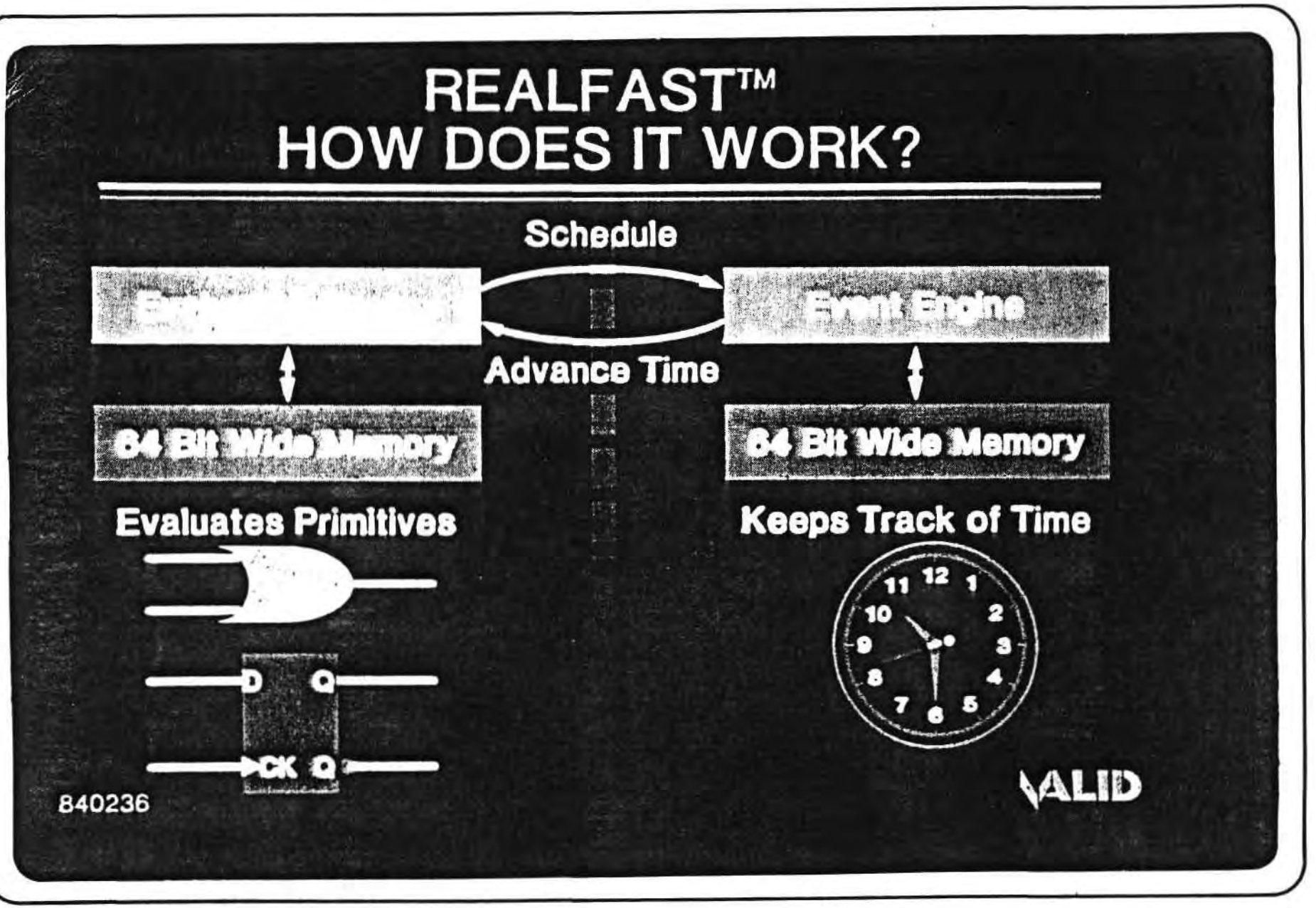
VALID

REALFAST™: WHY IS THE COST PERFORMANCE SO MUCH BETTER?

- **Simple Architecture Allows for High-Speed Execution**
  - **RISC (Reduced Instruction Set Computer)**
- **Wide Memories Allowing High Information Bandwidth**

840236

VALID

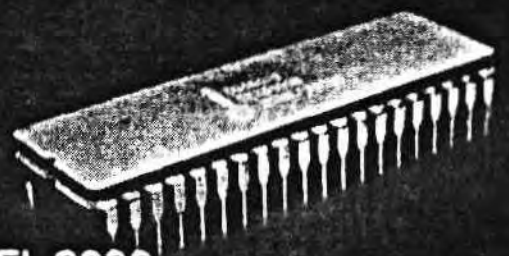


SIMULATION MODELS

SIMPLE IC

1	2	Out
0	0	0
1	0	0
0	1	0
1	1	1

SIMULATION MODEL



INTEL 8086

VALID

A SOLUTION:
HARDWARE MODELS
VALID

REALCHIP™ MODEL
VALID

MANY MODELS ARE REQUIRED

DESIGN ENGINEERS

10%
IC's

90%
Board Level Systems

VALID

REALFAST™ /REALCHIP™

REALFAST™

- 500,000 Events/Second Makes Sequential Fault Simulation Practical

REALCHIP™

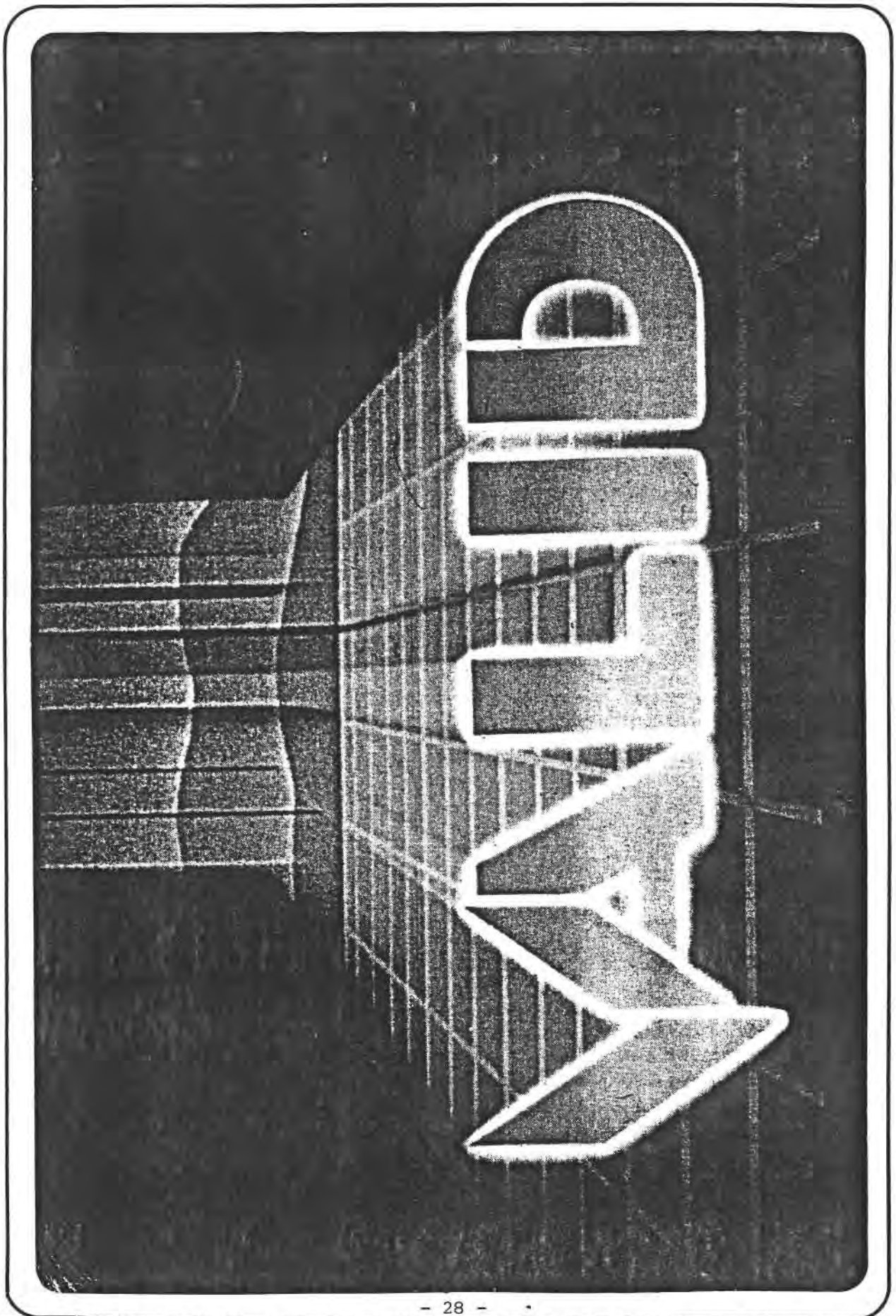
- Provides Simulation Models of Complex VLSI Parts

VALID

TYPICAL TARGET APPLICATIONS

Electrical	• Logic Simulation • Circuit Simulation • Routing
Mechanical	• 3-D Modeling • Simulation • Thermal Analysis
Structural	• Finite Element Analysis (NASTRAN) • Loading Calculations
Hydrodynamic	• Navier-Stokes Equation

VALID



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DESIGN INTERFACE STRATEGIES

Kent Jaeger
Manager of Design Interface
California Devices, Inc.

Mr. Jaeger joined California Devices, Inc., in July 1983 as Area Marketing and Major Programs Manager. His present responsibilities as Manager of Design Interface include management of all product and technical marketing areas. Prior to joining California Devices, Inc., Mr. Jaeger worked at Texas Instruments where he was responsible for major programs in both the Bipolar Gate Array and Standard Cell product groups. Later he had management responsibility for CMOS Gate Array programs. Mr. Jaeger received a B.S. degree in Industrial Distribution from Clarkson College of Technology in Potsdam, New York.

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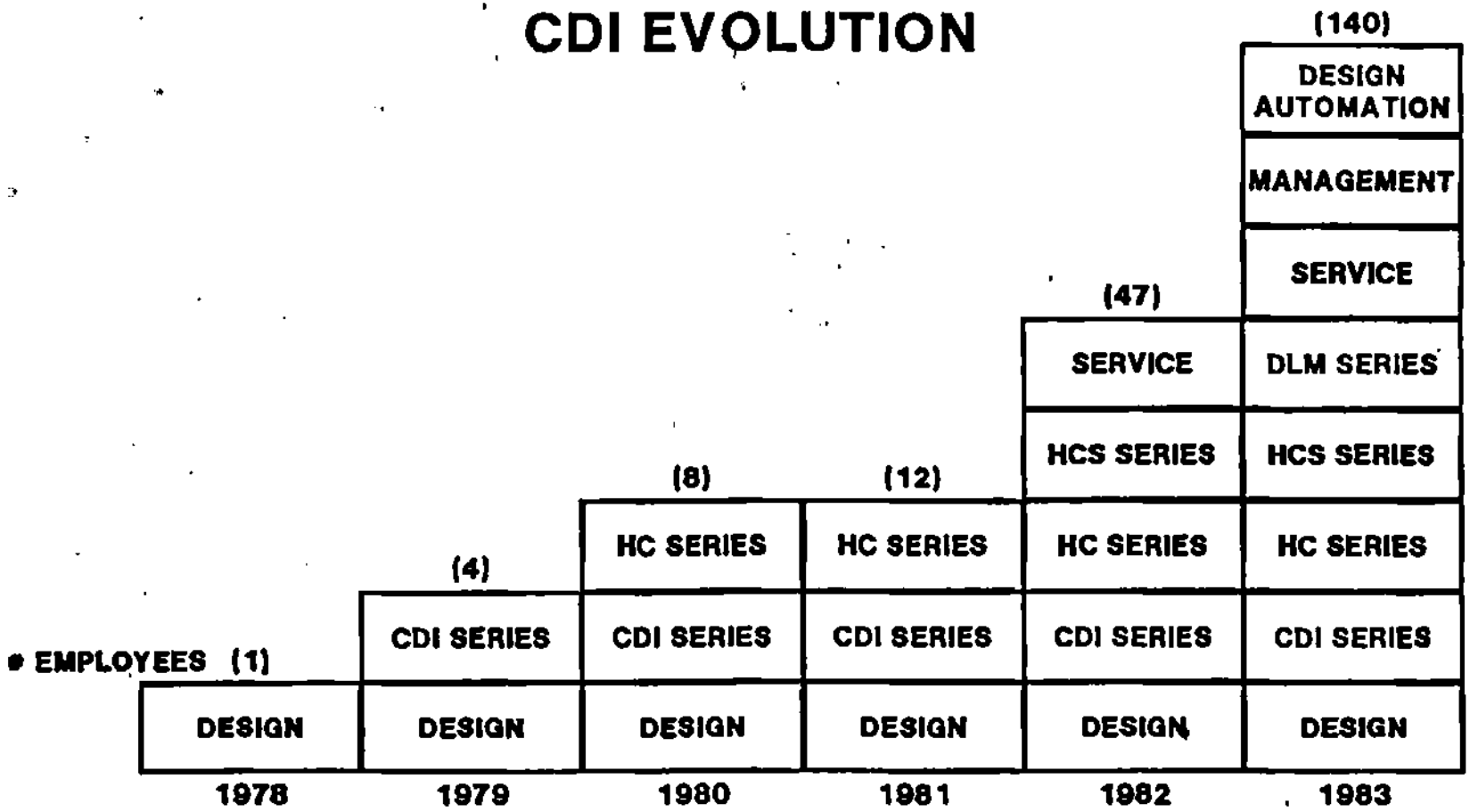
ELECTRONIC DESIGN AUTOMATION FOCUS CONFERENCE
May 10-11, 1984
Sunnyvale, California

CDI CALIFORNIA DEVICES INC.

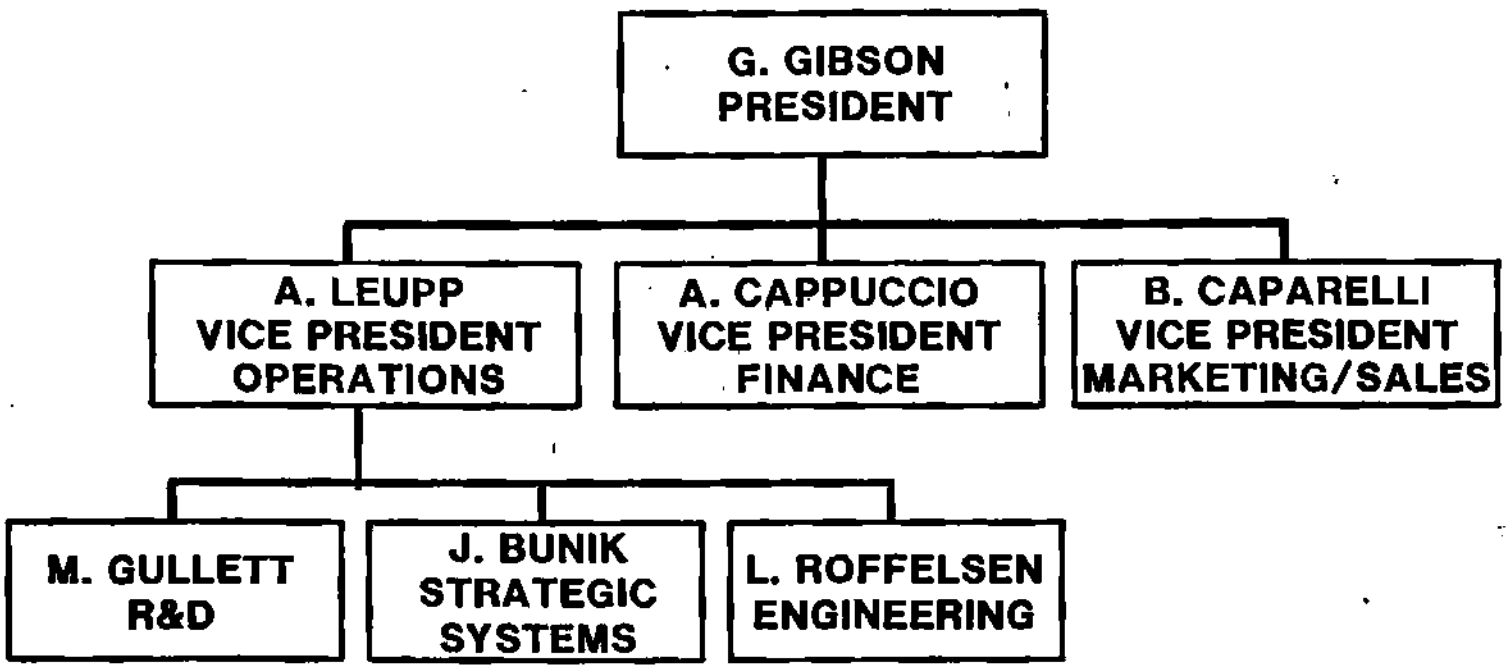
- INTRODUCTION TO CDI
- DESIGN AUTOMATION CAPABILITIES
- DESIGN CENTERS
- INTERFACE ALTERNATIVES

CALIFORNIA DEVICES INC.

CDI EVOLUTION



MANAGEMENT TEAM



CDI CALIFORNIA DEVICES INC.

CDI PRODUCTS

PRODUCT	FEATURES	TECHNOLOGY
CDI	HIGH VOLTAGE RADIATION TOLERANCE 100-800 GATES 22-72 I/O'S 3 MHz CLOCK	6.3μ METAL GATE CMOS SINGLE LEVEL METAL
HCS	LS TTL COMPATIBLE 300-1780 GATES 40-92 I/O'S 20 MHz CLOCK	4μ SILICON GATE CMOS SINGLE LEVEL METAL
DLM	6 TTL LOAD DRIVE SMALL SILICON DIE SIZE 225-10, 260 GATES 30-156 I/O'S 52 MHz CLOCK	3μ SILICON GATE CMOS DUAL LEVEL METAL

DESIGN AUTOMATION

- HISTORICAL PERSPECTIVE
  - MAJORITY OF CAPABILITIES DEVELOPED FOR INTERNAL USE (IBM, BELL LABS, TI)
  - REQUIRED EXTENSIVE COMPUTING CAPABILITIES
  - RECENT UNIVERSITY AND GOVERNMENTAL ACTIVITIES HAVE SPAWNED MORE EFFICIENT COMMERCIAL CAPABILITIES

DESIGN AUTOMATION OBJECTIVES

- PROVIDE TOOL ACCESS AND CAPABILITY TO ENSURE LOGIC FUNCTIONALITY, ELECTRICAL INTEGRITY, AND TESTABILITY
- STRUCTURE DESIGN SYSTEM TO ALLOW WIDE VARIETY OF DESIGN INPUTS AT VARIOUS POINTS IN THE DESIGN PHASE
- VALIDATE AND VERIFY EACH ELEMENT OF DATA REGARDLESS OF ENTRY FORMAT OR POINT

CALIFORNIA DEVICES INC.

ADVANTAGES OF COMMERCIAL SOFTWARE TOOLS

- RAPID ESTABLISHMENT OF FULL CAPABILITIES
- INCREASED SUPPORT AND CONTINUED DEVELOPMENT
- LARGE USER BASE FOR RAPID DEBUG
- TECHNOLOGY INDEPENDENT
- PORTABILITY FOR IN-HOUSE CUSTOMER USE

DESIGN AUTOMATION CAPABILITIES

- **DESIGN ANALYSIS AND DEVELOPMENT:**
  - DAISY LOGICIAN WORKSTATIONS
  - GENRAD'S HILO SIMULATION SYSTEMS (PRIME 750 VAX 11/780)
- **AUTOMATED PLACE AND ROUTE:**
  - DAISY GATEMASTER WORKSTATIONS
  - SCIENTIFIC CALCULATIONS SCIMEDS SYSTEM (VAX 11/780)
- **AUTOMATED VERIFICATION:**
  - PHOENIX DATA SYSTEMS' MASKAP PROGRAM
  - APPLICON DRC PROGRAM

SEMICUSTOM DESIGN CENTERS

- **HISTORICAL PERSPECTIVE**
  - **ESTABLISHMENT OF REGIONAL DESIGN CENTERS BY MAJOR S.C. MANUFACTURES**
  - **UTILIZED INTERNALLY DEVELOPED D.A. SYSTEMS WITH LARGE HARDWARE REQUIREMENTS**
  - **ONLY VIABLE OPTION AT THAT POINT IN TIME**
  - **DUE TO RESOURCE AND CAPITAL INVESTMENTS, TREND TO OPERATE AS PROFIT AND LOSS CENTERS**

SEMICUSTOM DESIGN CENTERS

- WITH THE EVOLUTION OF D.A. CAPABILITIES (HARDWARE & SOFTWARE), ESTABLISHMENT OF LARGE OF REGIONAL DESIGN CENTERS NOT ESSENTIAL FOR SUCCESSFUL COMPLETION OF SEMICUSTOM DESIGN

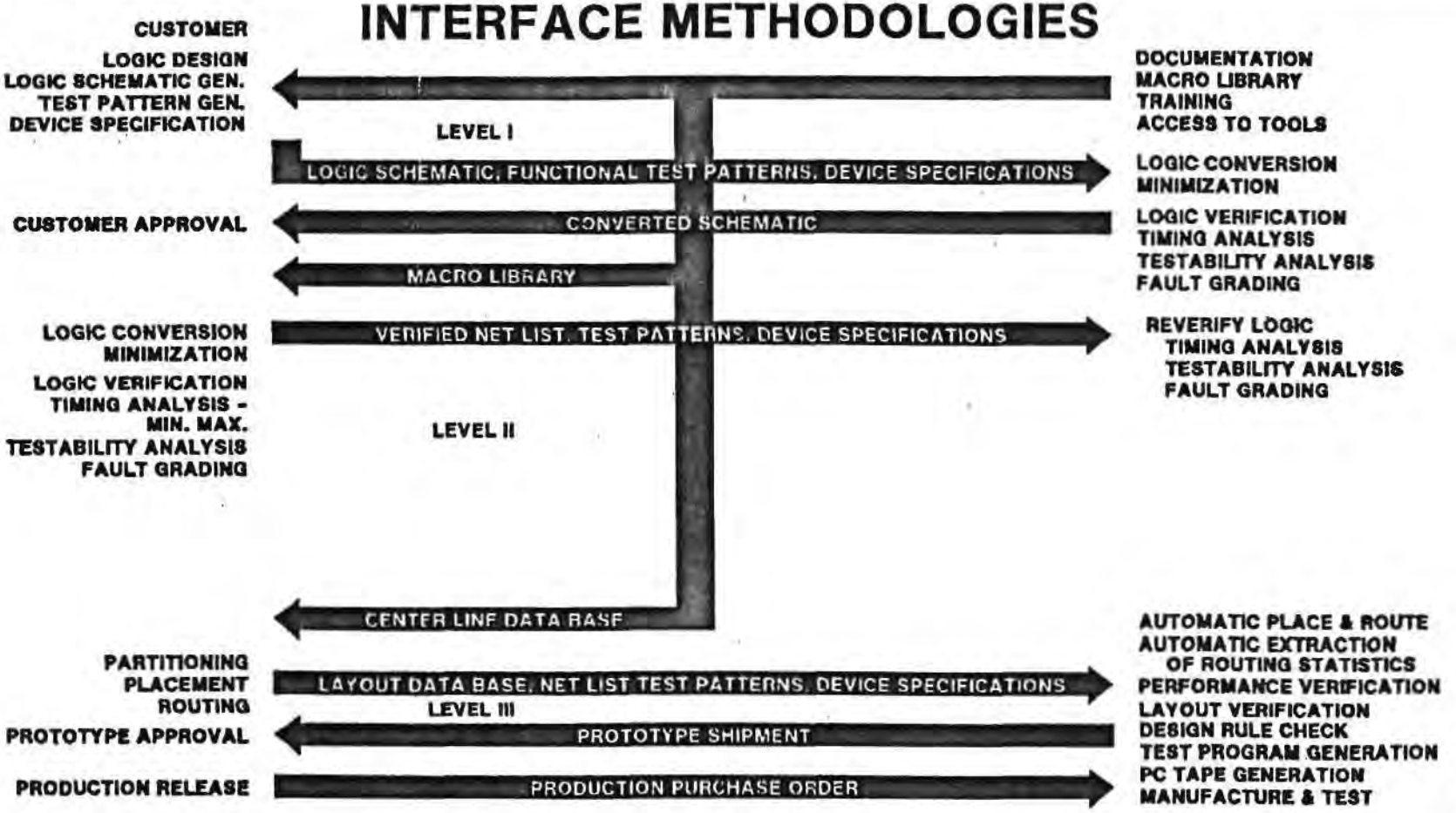
CDI CALIFORNIA DEVICES INC.

CDI DESIGN CENTER STRATEGY

- **PRESENT STATUS**
  - 3500 SQUARE FOOT TRAINING FACILITY - SAN JOSE
  - MULTI WORKSTATION/MINICOMPUTER TERMINAL ENVIRONMENT
  - CAPACITY TO TRAIN 48-60 PEOPLE PER MONTH
  - APPLICATION AND DESIGN ASSISTANCE AVAILABLE
- **FUTURE PLANS**
  - EXTENDED REGIONAL SUPPORT THROUGH NATIONWIDE DISTRIBUTION NETWORK
  - SUPPORT INCLUDES APPLICATION ASSISTANCE, PRODUCT SPECIALIST, TRAINING, DOCUMENTATION BANK, DESIGN TOOLS AND ASSISTANCE

CALIFORNIA DEVICES INC.

INTERFACE METHODOLOGIES

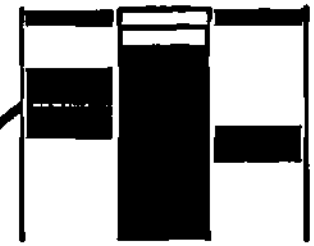


CDI CALIFORNIA DEVICES INC.

INTERFACE OPTIONS

LEASE WORKSTATION

CDI MAIN FRAME



CUSTOMER CONNECTS VIA TELE-LINK WITH CDI MAIN FRAME

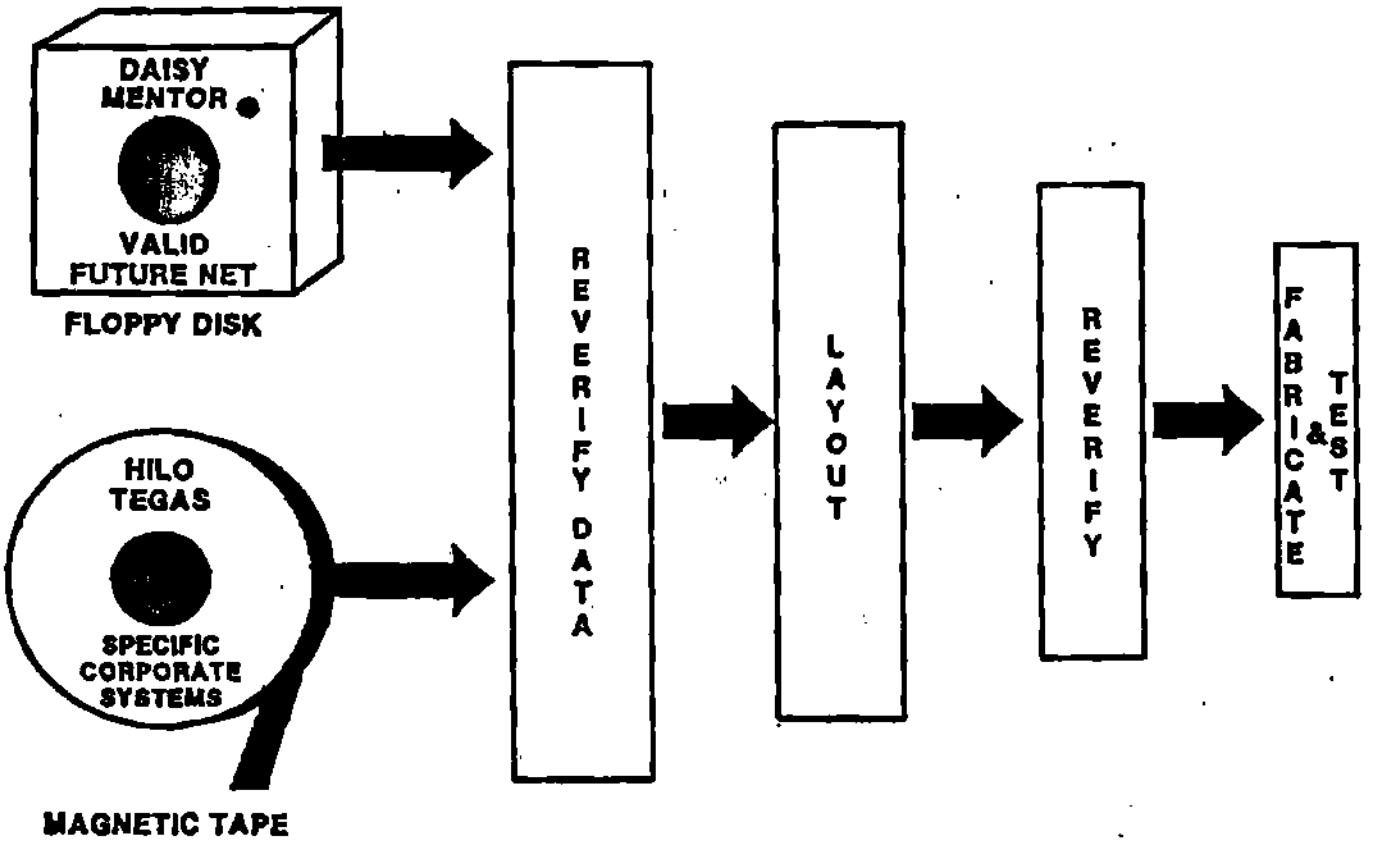
CUSTOMER WORKS AT CDI DESIGN CENTER

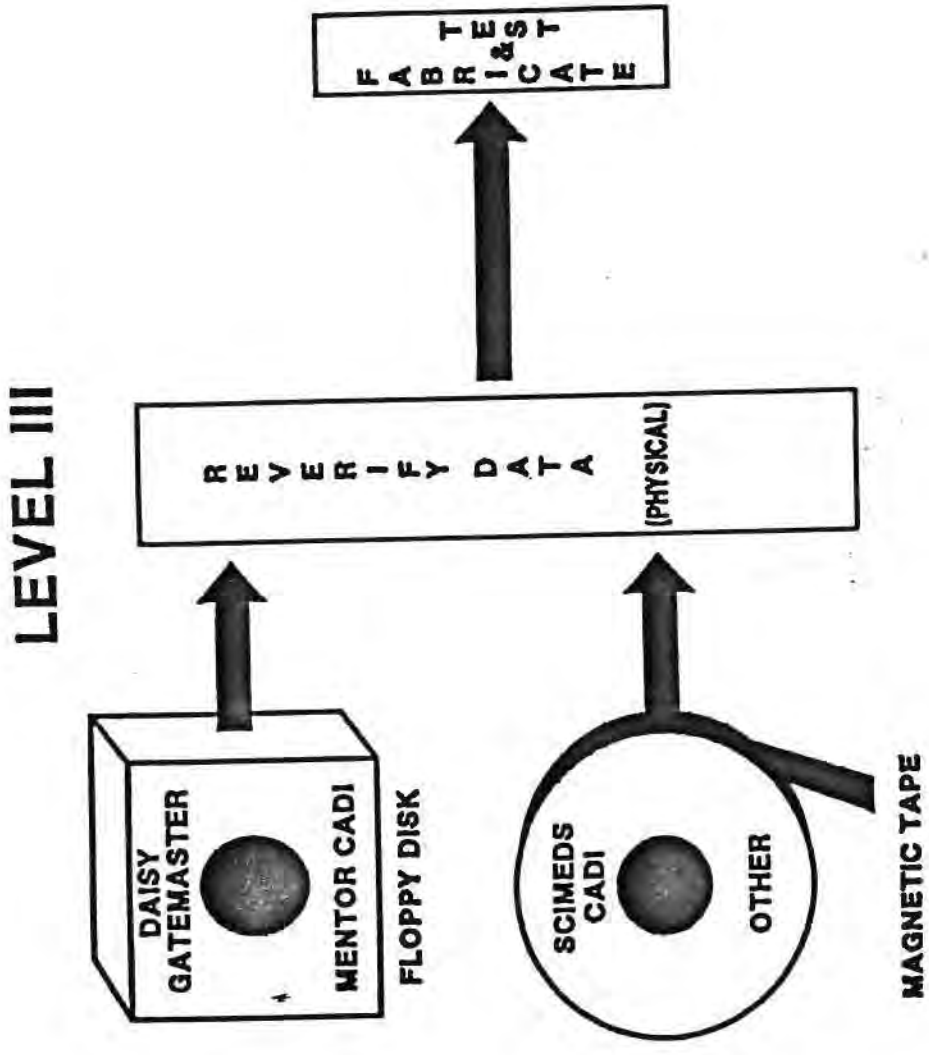
CDI CALIFORNIA DEVICES INC.

DLM MACRO LIBRARIES

- **MACRO LIBRARIES ARE AVAILABLE FOR THE FOLLOWING DESIGN SYSTEMS:**
  - **DAISY LOGICIAN AND GATEMASTER WORKSTATION**
  - **MENTOR WORKSTATION**
  - **VALID LOGIC WORKSTATION**
  - **GENRAD'S HILO SIMULATION SYSTEMS**
  - **TEGAS SIMULATION SYSTEMS**
  - **FUTURENET SCHEMATIC DESIGN SYSTEM**
  - **ADDITIONAL COMMERCIAL AND SPECIFIC CORPORATE DESIGN LIBRARIES UNDER DEVELOPMENT**

LEVEL II




LEVEL III
REVERIFY DATA (PHYSICAL)
FABRICATE I&S
DAISY GATEMASTER
MENTOR CADI
FLOPPY DISK
SCIMEDS CADI
OTHER
MAGNETIC TAPE

Nielsen Dataquest

THE SYNERGY OF ASICs AND EDA

Kenneth V. McKenzie
Associate Director, Semiconductor Industry Service
Dataquest Incorporated

Mr. McKenzie is Associate Director of DATAQUEST's Semiconductor Industry Service. He is responsible for all research activities on semiconductors and related products. His other duties include internal data processing coordination for the Semiconductor Industry Service and research into specific end-user markets. During Mr. McKenzie's 14 years in the electronics industry, he has held management positions in both design engineering and marketing. His most recent position was as Marketing Manager at Zilog, Inc. Prior to that, Mr. McKenzie was Marketing Manager for 8-bit microprocessors at Intel Corporation.

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May 10-11, 1984
Sunnyvale, California

THE SYNERGY

OF APPLICATION-SPECIFIC INTEGRATED CIRCUITS AND ELECTRONIC DESIGN AUTOMATION

KEN McKENZIE
ASSOCIATE DIRECTOR
SEMICONDUCTOR INDUSTRY SERVICE
DATAQUEST INCORPORATED

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WHAT IS AN ASIC?

- CUSTOM
- GATE ARRAY
- STANDARD CELL
- PROGRAMMABLE ARRAY LOGIC (PAL®)

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WHY PREVIOUS ASIC GENERATIONS FAILED

- LACK OF ECONOMICAL USER DESIGN TOOLS
- USER/VENDOR LOGISTICS
- LIMITED SECOND-SOURCING
- PRIMITIVE HIGH-PIN-COUNT PACKAGING

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ASIC TECHNOLOGY--TODAY

- EVOLUTION TO STRUCTURED ELEMENTS
- CMOS FOR LOW POWER AND SPEED
- CHIP CARRIER AND PIN-GRID PACKAGING
- TREND TOWARD INDUSTRY STANDARDS

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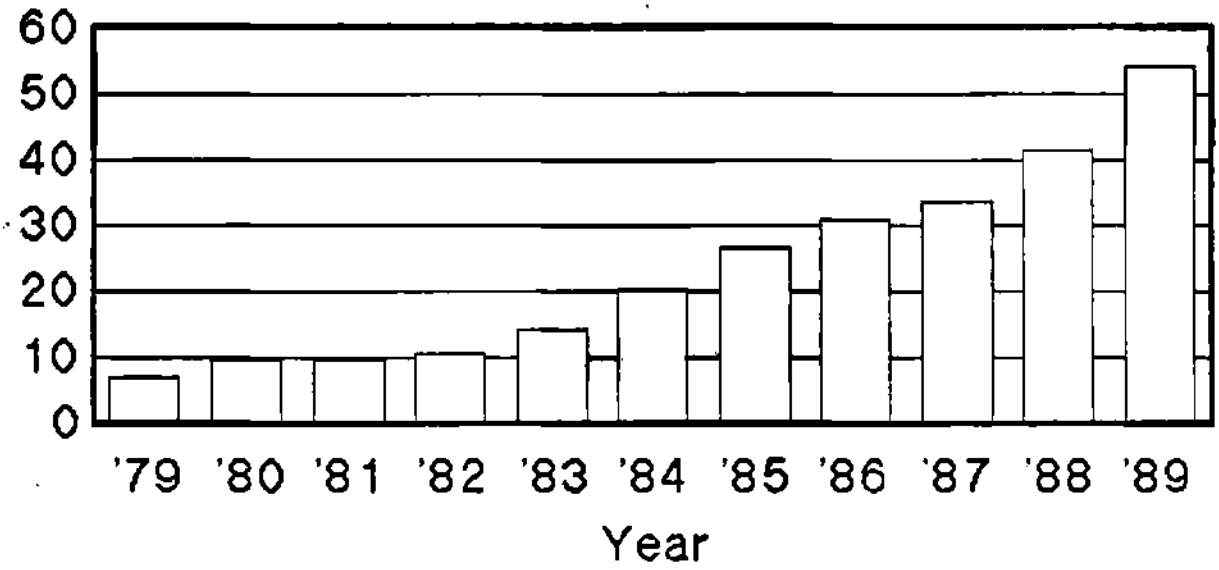
MARKET OVERVIEW

WORLDWIDE INTEGRATED CIRCUITS

(Billions of Dollars)



Source: DATAQUEST

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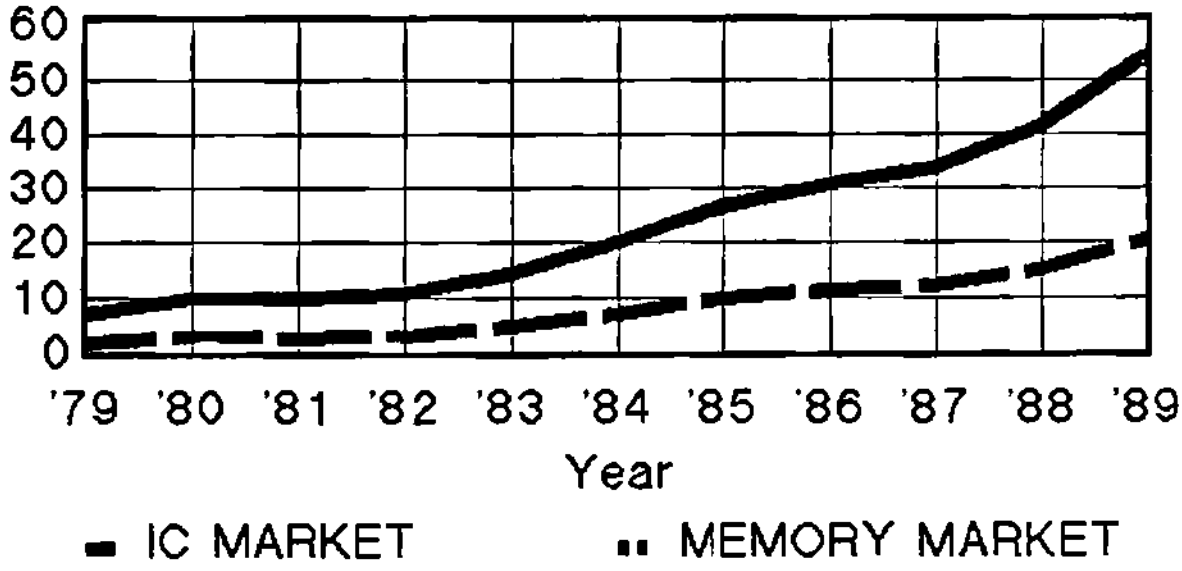
MARKET OVERVIEW

WORLDWIDE IC AND MEMORY

(Billions of Dollars)



Source: DATAQUEST

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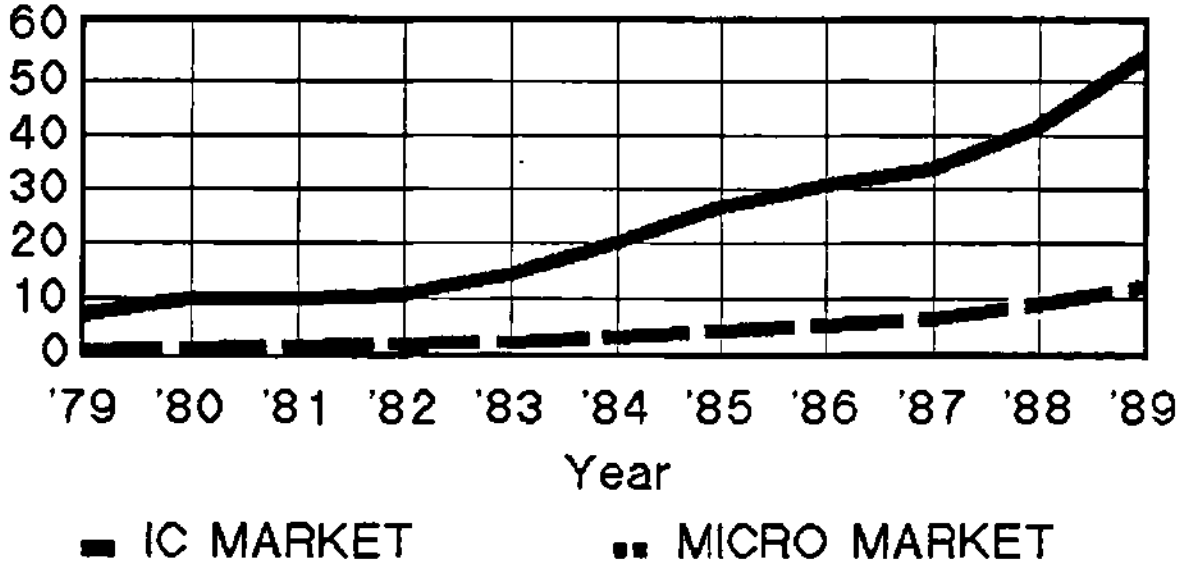
MARKET OVERVIEW

WORLDWIDE IC AND MICRO

(Billions of Dollars)



Source: DATAQUEST

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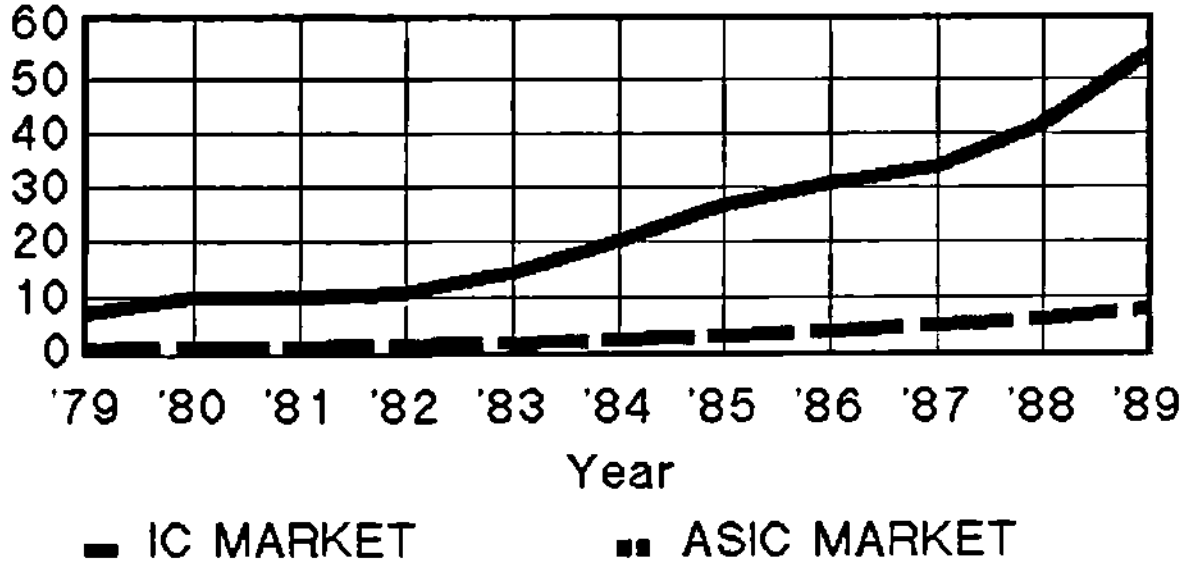
MARKET OVERVIEW

WORLDWIDE IC AND ASIC

(Billions of Dollars)



Source: DATAQUEST

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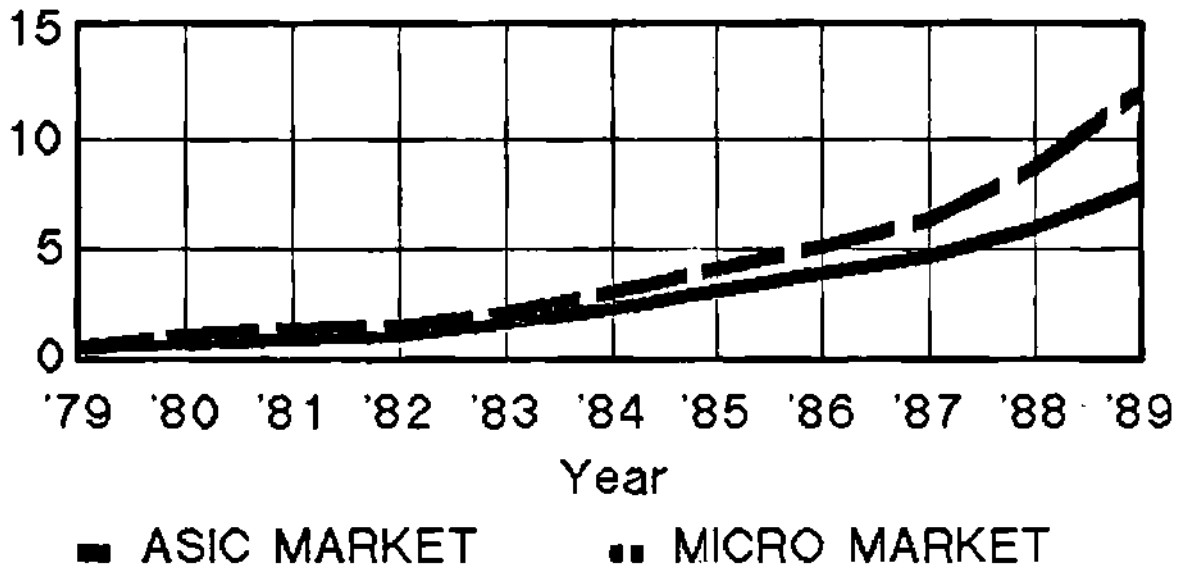
MARKET OVERVIEW

WORLDWIDE MICRO AND ASIC

(Billions of Dollars)



Source: DATAQUEST

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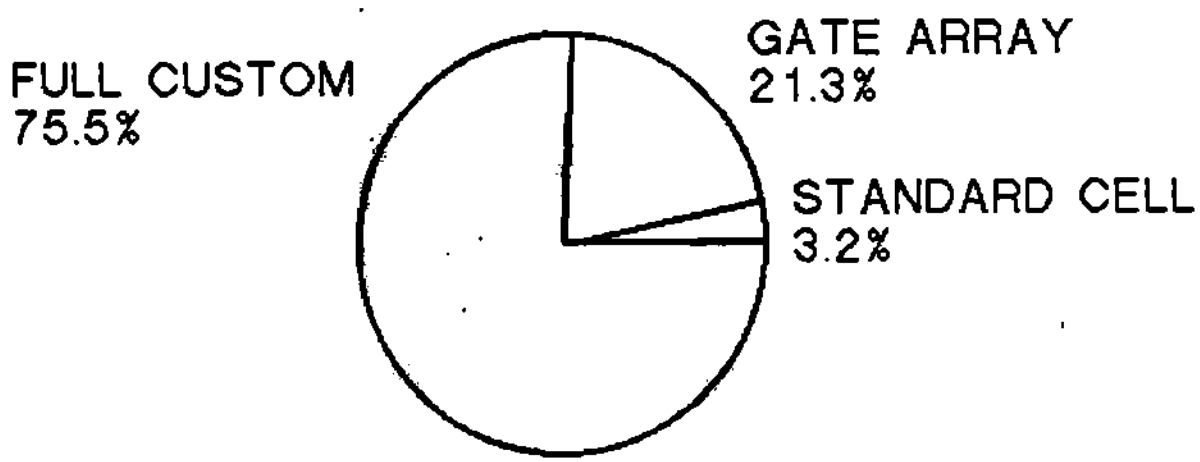
MARKET OVERVIEW

WORLDWIDE ASIC MARKET

1983 SHIPMENTS ($)

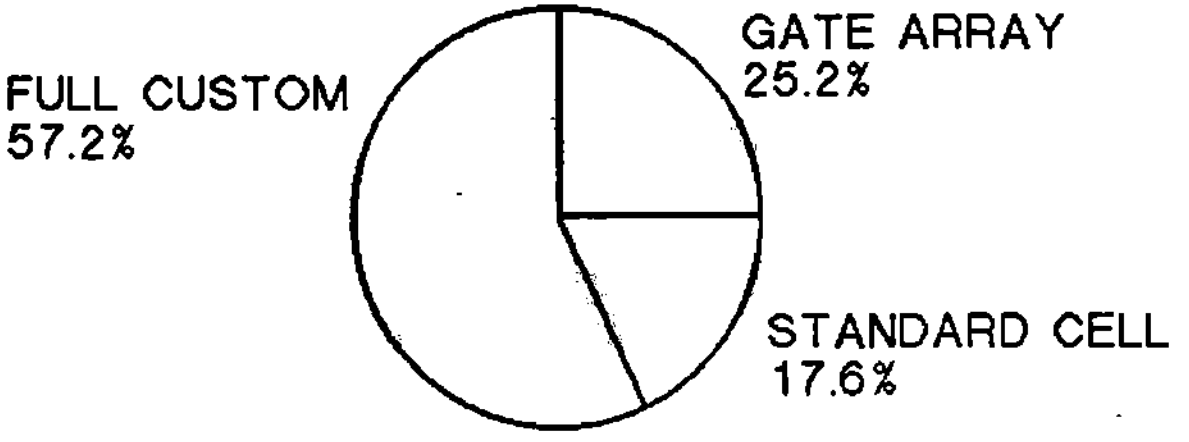


Source: DATAQUEST

MARKET OVERVIEW

WORLDWIDE ASIC MARKET

1989 SHIPMENTS ($)



Source: DATAQUEST

WHY ASICS ARE WINNING--TODAY

- POWERFUL, INEXPENSIVE MICROPROCESSORS
- SOPHISTICATION OF USERS
- ASIC-FOCUSED START-UP COMPANIES
- ACCEPTANCE OF CMOS VLSI
- SHORTAGE OF TTL "GLUE"

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THE IMPACT OF CMOS VLSI

HIGH-SPEED VLSI MUST BE IN CMOS

- PACKAGING TECHNOLOGY
- POWER DISSIPATION
- RELIABILITY

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THE IMPACT OF CMOS VLSI

LOW POWER LOWERS TOTAL SYSTEM COST

- SWITCHING POWER SUPPLY $
- COOLING FAN $
- FEATURE CONTENT VS. SYSTEM FOOTPRINT
- NOISE IMMUNITY AND SERVICE

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EDA DRIVEN BY VLSI ADVANCEMENTS

- MICROPROCESSORS
- MICROCONTROLLERS
- MICROPERIPHERALS
- DYNAMIC RAMS
- ASICS

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MICROPROCESSORS--TODAY

8-BIT

- MATURE (1972)
- GIVING WAY TO 8/16-BIT
- CMOS FAMILIES DELAYED
- FUNCTIONAL INTEGRATION

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MICROPROCESSORS--TODAY

16-BIT

- 4 PLAYERS--2 CLEAR WINNERS
- GOING 16/32-BIT
- CMOS--THE HOT TOPIC
- FUNCTIONAL INTEGRATION

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MICROPROCESSORS--TODAY

32-BIT

- LITTLE REAL ACTION
- SUPERSETS OF EXISTING 16-BIT MICROS
- VIRTUAL MEMORY SUPPORT
- CHIP CARRIER AND PIN-GRID PACKAGING

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MICROPROCESSORS--THE FUTURE

- HIGH-SPEED (20 MHz)
- TOTAL CMOS FAMILIES
- TRUE 32-BIT MPU
- ON-CHIP MEMORY MANAGEMENT
- PARALLEL, PIPELINED ARCHITECTURES
- APPLICATION-SPECIFIC MPUS

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DYNAMIC RAMS--TODAY

64K BIT

- MANY SUPPLIERS
- U.S. GAINING MARKET SHARE
- PRICING FLAT TO UP
- SUPPLY/DEMAND BALANCE--YEAR END

256K BIT

- LITTLE NON-JAPANESE ACTION
- HIGH PRICES ($30 ASP-1984)
- VOLUME IN 1985-1986

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DYNAMIC RAMS--THE FUTURE

- SHORTER PRODUCT LIFE CYCLES
- CMOS
- X4 AND X8 ORGANIZATIONS
- MINIMAL AREA PACKAGING (MAP)
- HIGH SPEEDS (50-100 NS)

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MICROCONTROLLERS--THE FUTURE

- CMOS FAMILIES
- HIGH-PIN-COUNT PACKAGING
- 16/32 BIT ARCHITECTURES
- ANALOG I/O
- ON-CHIP LAN
- APPLICATION-SPECIFIC MCUS

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MICROPERIPHERALS--THE FUTURE

- LONGER PRODUCT LIFE
- MPU INDEPENDENCE
- CONFIGURATION LANGUAGE
- RELATED FUNCTION INTEGRATION
- ON-CHIP FIFO AND PROCESSING

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APPLICATION-SPECIFIC ICS--THE FUTURE

- COMBINED GATE ARRAY AND STANDARD CELL
- MPU, MPR, MCU AS STANDARD CELLS
- SOFTWARE DATA SHEETS
- INDUSTRY STANDARDS
- COMBINED DIGITAL AND ANALOG FUNCTIONS

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CAD TOOLS--TODAY

- MULTIUSER
- SHARED RESOURCE
- STAR OR CLUSTERED COMMUNICATIONS
- TASKS VS. USERS--PERFORMANCE LIMITS
- COMPLEX MULTIUSER SOFTWARE

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CAD TOOLS--THE FUTURE

- SINGLE DEDICATED USER
- LOOSE-COUPLED 16-BIT AND 32-BIT MPUS
- HIGH-SPEED LAN COMMUNICATIONS
- STANDALONE/MULTITASKING
- OPERATOR-SENSITIVE SOFTWARE (NLI, AI)

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EDA WORKSTATIONS--THE FUTURE

- WORKSTATIONS THE SIZE OF TODAY'S PCS
- INTERNAL 1MB TO 4MB RAM
- TRANSPARENT VIRTUAL MEMORY
- VOICE I/O
- LOCAL OPTICAL DISK

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CAD TOOLS--THE FUTURE

- CAD TOOLS SMALLER THAN TODAY'S PCS
- INTERNAL 1MB TO 4MB RAM
- TRANSPARENT VIRTUAL MEMORY
- VOICE I/O
- LOCAL OPTICAL DISK

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EDA AND ASICS

- ASIC GROWTH DRIVES EDA FEATURES
- EDA "EASE-OF-USE" OPENS ASIC MARKETS

THANK YOU--VLSI

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Nielsen Dataquest

USER PANEL DISCUSSION

Bob Burkhardt
Manager, Bipolar Design Automation
Advanced Micro Devices Incorporated

Mr. Burkhardt has been Manager of Bipolar Design Automation at Advanced Micro Devices, Inc., for the past 2-1/2 years. He has been employed at AMD for more than 10 years. His previous positions at AMD include Design Engineer, Test Engineer, Project Engineer, Project Engineering Supervisor, General Foreman (Test Area), and Manager of Test Engineering. Mr. Burkhardt received a B.S.E.E. degree from California State Polytechnic University.

Dataquest Incorporated
ELECTRONIC DESIGN AUTOMATION FOCUS CONFERENCE
May 10-11, 1984
Sunnyvale, California

ELECTRONIC DESIGN AUTOMATION

I. APPLICATIONS

II. WHY AUTOMATE

III. EXPECTATIONS

IV. FUTURES

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I. Applications

- Custom Integrated Circuits
- LSI/VLSI Complexity
  - o System Design
  - o Logic Design
  - o Mask Layout
  - o Verification
  - o Prototype Development

II. Why Automate

- Complexity
- Too Cumbersome
- Many Benefits

he AmZ8163/AmZ8167, which measures 15 x 19 feet in layout, will only measure 155 x 185 mils on the finished chip.

- WE DETERMINED OUR OLD APPROACH WAS TOO CUMBERSOME.

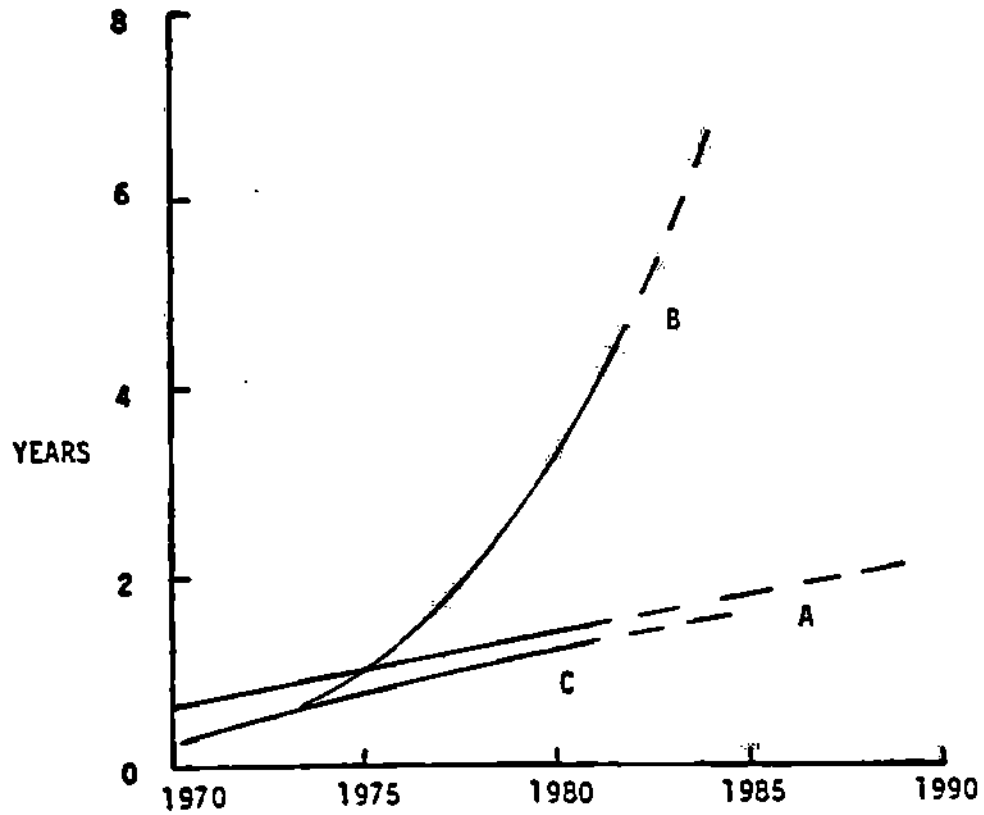
  o WE WOULD PLOT THE ENTIRE CIRCUIT AT 1016X.

  o WE CHECKED THE CIRCUIT BY HAND ON THE FLOOR.

  o WE TOOK DAYS TO DO DRC CHECKS ON OUR SMALL COMPUTER.

CHIP SIZE (MIL)	280 x 280	280 x 280
SCALE	1016X	254X
RESOLUTION (UM)	1	4
DRAWING SIZE (FT.)	24 x 24	6 x 5
# MYLARS	49	4
PLOTS PER LAYERS	16	1

DESIGN VS. TECHNOLOGY DEVELOPMENT
CYCLE TIMES

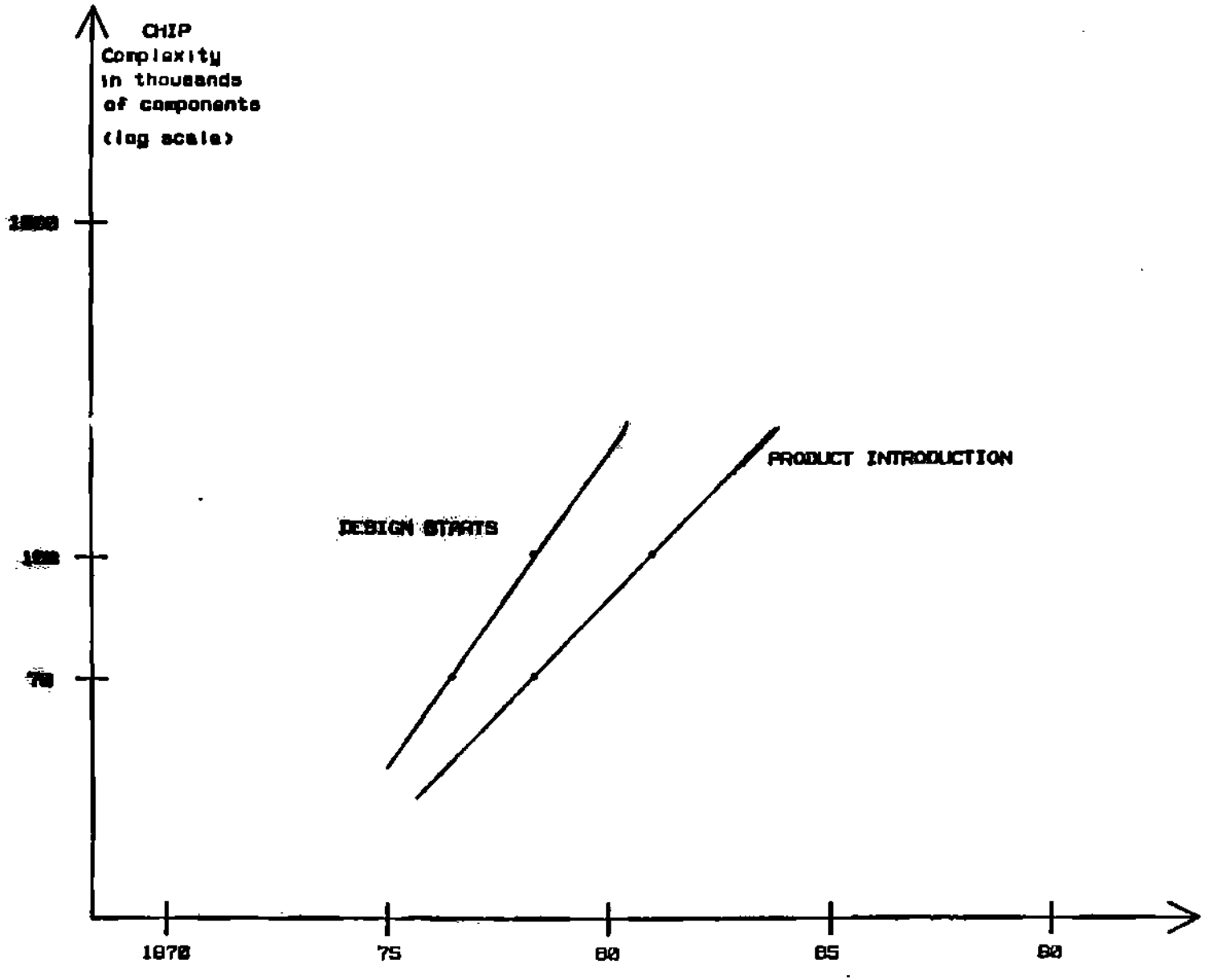


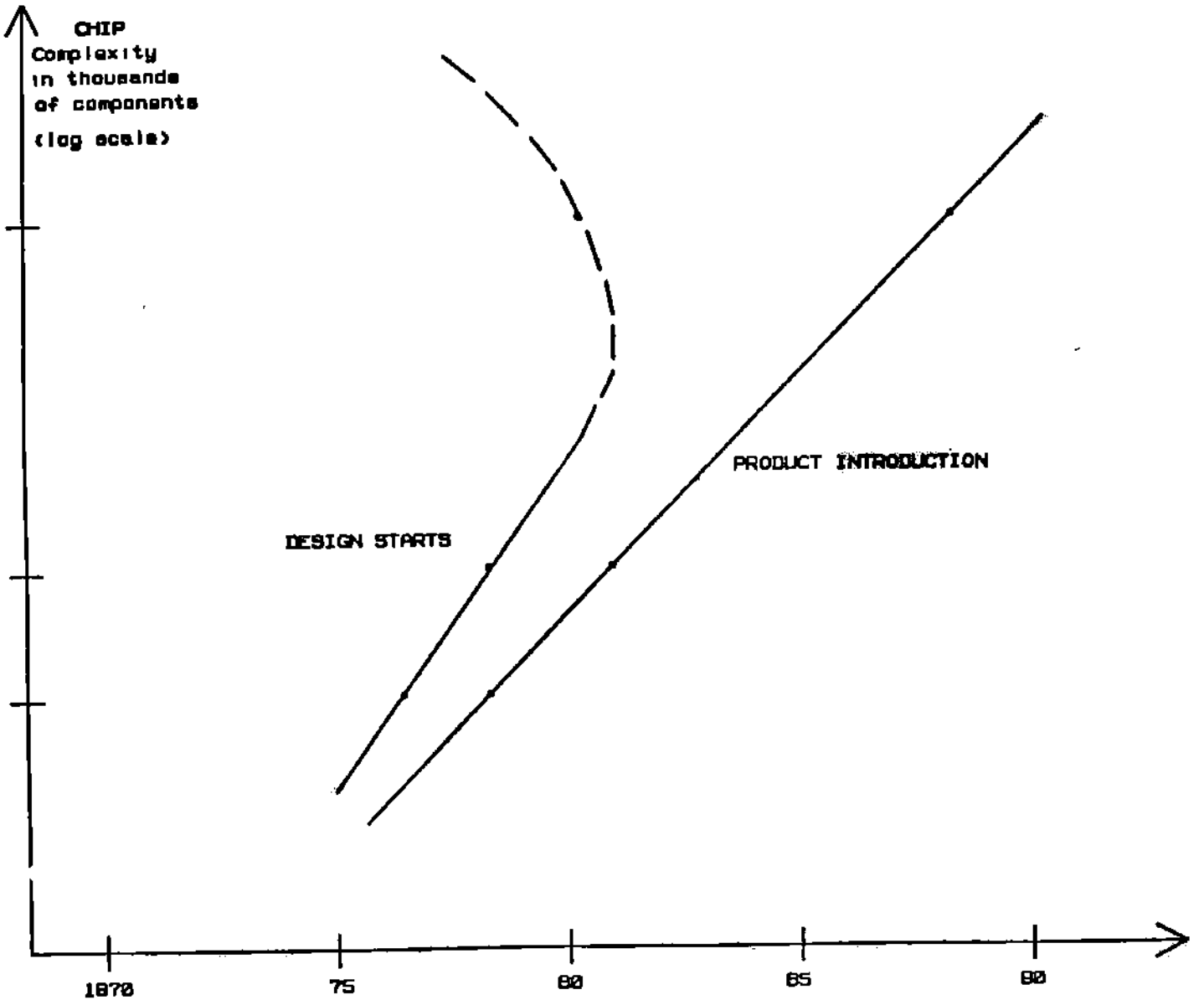
A. LEAD TIME FROM RELEASE OF DESIGN RULES TO PRODUCTION

B. DESIGN TIME FOR A LOGIC PRODUCT.

C. DESIGN TIME FOR A MEMORY PRODUCT.

As one can see in figure 1, the time to develop a new technology is in the 1-2 year time frame. However, the time to design a new logic circuit is in the 4 year time frame.





BENEFITS OF DESIGN AUTOMATION

- o Sooner to Market
- o Lower Design Cost
- o Fewer Errors
- o Products Built on Current Technology
- o Higher Engineering Leverage
  - HIGHER RETURN ON ENG'G INVESTMENT
  - MORE PRODUCTS OUT OF EACH LOGIC/CKT ENGINEER
  - FASTER CORPORATE GROWTH

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III. Expectations

- Essentials
- Highly Desireable
- Other Features

Engineering Workstation History

5/82 Established Selection Committee

8/82 Demonstrations

➡ 9/82 First Cut Specification

10/82 - 2/83 Trial Evaluations

5/83 Second Detailed Specification
Based on "Current" Capabilities

2/83 Decision Matrix
Failed to Qualify Any One

8/83 Reduced Specification

9/83 Decision Matrix

10/83 Initial System

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Engineering Work Station
Selection Criteria

I. Essential Features

1. Powerful, fast graphics editor
2. Plot capability
3. Interface to netlist driven software
4. Mask layout capability
5. Data base capable of storing all information known about a design except for layout details
6. Capacity sufficient to handle 100 D-size drawings
7. High speed IBM interface
8. Ability to support a hierarchical design
9. 9-track tape availability
10. Local applications and maintenance support

II. Highly Desireable Features

1. Portable software
2. Release control and security system
3. Ability to supply many systems per year
4. Local general purpose processing
5. Interactive logic simulation with behavioral models
6. Ability to run university software

III. Other Desireable Features

1. Local networking
2. Word processing
3. Electronic mail
4. Timing verification

Engineering Workstation History

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9/83 Decision Matrix

10/83 Initial System

Decision Matrix

Schematic Editor

Netlist Generator

Logic Simulator

Timing Verifier

PLA Optimizer

Layout Editor

Auto Router

Network Extractor

Design Rules Checker

Continuity Checker

General Purpose Computing Power

Engineering Workstation History

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8/82 Demonstrations

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10/83 Initial System

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ENGINEERING WORK STATION

SELECTION CRITERIA

I. ESSENTIAL FEATURES

1. POWERFUL, FAST GRAPHICS EDITOR
2. PLOT CAPABILITY
3. INTERFACE TO NETLIST DRIVEN SOFTWARE
4. MASK LAYOUT CAPABILITY
5. DATA BASE CAPABLE OF STORING ALL INFORMATION KNOWN ABOUT A DESIGN EXCEPT FOR LAYOUT DETAILS
6. CAPACITY SUFFICIENT TO HANDLE 100 D-SIZE DRAWINGS
7. HIGH SPEED IBM INTERFACE
8. ABILITY TO SUPPORT A HIERARCHICAL DESIGN
9. 9-TRACK TAPE AVAILABILITY
10. LOCAL APPLICATIONS AND MAINTENANCE SUPPORT

II. HIGHLY DESIREABLE FEATURES

1. PORTABLE SOFTWARE
2. RELEASE CONTROL AND SECURITY SYSTEM
3. ABILITY TO SUPPLY MANY SYSTEMS PER YEAR
4. LOCAL GENERAL PURPOSE PROCESSING
5. INTERACTIVE LOGIC SIMULATION WITH BEHAVIORAL MODELS
6. ABILITY TO RUN UNIVERSITY SOFTWARE

III. OTHER DESIREABLE FEATURES

1. LOCAL NETWORKING
2. WORD PROCESSING
3. ELECTRONIC MAIL
4. TIMING VERIFICATION

Engineering Work Station
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ENGINEERING WORK STATION

SELECTION CRITERIA

I. ESSENTIAL FEATURES

✓ 1. POWERFUL, FAST GRAPHICS EDITOR

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✓ 6. CAPACITY SUFFICIENT TO HANDLE 100 D-SIZE DRAWINGS

? 7. HIGH SPEED IBM INTERFACE

✓ 8. ABILITY TO SUPPORT A HIERARCHICAL DESIGN

✓ 9. 9-TRACK TAPE AVAILABILITY

✓ 10. LOCAL APPLICATIONS AND MAINTENANCE SUPPORT

II. HIGHLY DESIREABLE FEATURES

SOME 1. PORTABLE SOFTWARE

SOME 2. RELEASE CONTROL AND SECURITY SYSTEM

✓ 3. ABILITY TO SUPPLY MANY SYSTEMS PER YEAR

✓ 4. LOCAL GENERAL PURPOSE PROCESSING

\- 5. INTERACTIVE LOGIC SIMULATION WITH BEHAVIORAL MODELS

\- 6. ABILITY TO RUN UNIVERSITY SOFTWARE

III. OTHER DESIREABLE FEATURES

✓ 1. LOCAL NETWORKING

\- 2. WORD PROCESSING

✓ 3. ELECTRONIC MAIL

SOME 4. TIMING VERIFICATION

Engineering Workstation Futures

- o High Speed Communications
- o Hardware Simulation
- o Circuit Emulation
- o Placement/Routing
- o Design Data Base Management
  - Security
  - Project Management
  - Release Control

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Engineering Workstation Success

- Heavy Vendor/Customer Interface
- This is an iterative process
- It is very difficult
  - o to clearly specify needs
  - o to build what you want versus what you specify
- Responsiveness

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CAE FOR SEMICUSTOM INTEGRATED CIRCUITS

Steve Shively
Computer-Aided Engineering Manager
International Microcircuits Incorporated

Mr. Shively is Manager of Computer-Aided Engineering at International Microcircuits Inc., and is currently chairman of the Mentor User's Group. Mr. Shively has worked at IMI for 15 months and has integrated the Mentor system into the IC design process at IMI to include schematic capture, simulation, test vector generation, and schematic to layout verification. Mr. Shively was previously with Intel Corporation, where he designed bipolar IC processes and was later responsible for developing the graphics methodology for using Ultratech IX reticle stepper masking technology.

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CAE for SEMICUSTOM INTEGRATED CIRCUITS

INTERNATIONAL MICROCIRCUITS INCORPORATED

International Microcircuits Incorporated (IMI) has been manufacturing semi-custom integrated circuits (gate arrays) since 1974. Since then IMI has grown to include our own facilities for manufacturing of CMOS integrated circuits. IMI provides extensive design engineering support to customers who are unfamiliar with IC's, logic verification of customer's designs, and prototype parts for customer evaluation before production begins. IMI has complete in-house design automation tools, production wafer fabrication capabilities, assembly facilities, and a production test floor.

IMI did around $12 million in sales in 1983, and growth for 1984 looks very promising. IMI maintains over 100 employees, in excess of 25,000 square feet housing all phases of manufacturing. IMI has had over 300 customers to date comprising well over 750 unique, customer defined designs.

Nearly all of IMI's current business stems from gate array products; however, standard cell designs will soon be available, and several standard parts have been designed (such as multipliers, 2901's, etc).

Late in 1982, IMI decided that CAE workstations had the potential to be a major part of the logic designer's future; furthermore, that IMI should be prepared to interface cleanly with a large segment of the logic design community.

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SEMICUSTOM IC TRENDS

Growth of semi-custom IC markets is projected to continue through 1991 at an annual rate of 32% (according to SIA & EDN). The size and number of semi-custom IC vendors has grown tremendously in recent years. Manufacturers will need to continually improve the speed and effiency of their design process to provide a relatively quick turn-around time to remain competitive.

Increasing design complexity will make the job of reducing design times more and more difficult. The number of gates per IC has been increasing consistently; this trend will continue. Larger designs require more time for nearly every step in the design process; logic specification, simulation, fault simulation, layout, and test generation are all included. We are constantly looking for a faster, more efficient way to perform each of these tasks.

The increasing performance of CMOS semi-custom IC's has caused several additional burdens on computer aided design: delays introduced by metal lines must be carefully monitored to insure correct circuit performance, transistor delays must be carefully characterized and modelled, and fabrication techniques must evolve to handle the shrinking geometries.

These trends clearly present the need to reduce the length and number of design cycle iterations. Most logic designs today are changed many times in their design lifetime; but the catch is that changes appear throughout the design cycle which will waste resources. More powerful design analysis tools must be used to prevent erroneous designs iterations.

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WHY USE CAE WORKSTATIONS?

Why are semicustom IC manufacturers so eager to use CAE workstations ? There are dozens of resons why they're important to us, but generally the reasons fall into one of three categories: 1) Design Aids for the Customer, 2) Enhancement of the Customer interface, and 3) Enhancement to internal design methodologies.

As a design aid to the customer, CAE workstations are at home in their intended environment. These tools have evovled to replace breadboards for design and paper for documentation. These systems are relatively low cost compared to the alternatives of purchasing batch-oriented computer equipment to perform simulations and other verification needs.

Use of CAE systems will enhance a vendor's interface with customers. If both vendor and customer design, verify , and store their design data electronically, then the vendor can insure the customer that the manufactured part will meet the specifications of the customer - even on large, complex designs. Also, the customer can have easy access to large Macro Cell libraries containing primitive and high order logic functions to use in his design. Information can be exchanged through a common media.

Semicustom vendors may enhance their design flows by using CAE systems to drive automatic placement and routing programs. A key aspect of IC layout is relating layout geometries to the logic schematic. CAE workstations also provide a ability to electronically capture and document their designs; the large number of designs projected for the next 5 years will demand some effective documentation techniques. But overall, use of CAE systems by semicuston IC makers is the ability to provide relatively simple access to IC silicon technology to its customers.

CAE TOOL NEEDS

In a semicustom environment, throughput is an extremely important issue; therefore, the single most important need from CAE systems is more power at a lower cost. Although the CAE system manufacturers currently boast awesome power at your fingertips, the fact is that design verification needs will continue to be greater than the CPU cycles available to the designer in his own real-time environment. IMI experience has shown that simulation alone will take more than the power available in any workstation; and let's not forget the many other functions such as timing verification, fault simulation, test vector generation, etc. that must also be performed.

Faster machines will help reduce the time to complete a typical design; and/or allow much larger designs to be performed. But most critically, more powerful systems will allow the user to perform more verfication steps which is key to making a design work correctly the first time in silicon.

Another area of need is in phsyical layout tools for gate arrays. *Efficient* phsyical layout automation is a prime concern for gate array manufacturers. Although some people are impressed by today's offerings in this area, IMI has found severe drawbacks to current auto-routing techniques. Silicon costs money; it is not the largest cost of all IC's, but it is always significant. Furthermore, remember that semicustom IC designs are going to continue to grow in size. Current auto-routing uses much more silicon than hand-mapped gate arrays.

As noted earlier, changes to a design happen frequently. When this occurs, it would be optimum to make the change in one place and have it propagate throughout the entire design cycle in a timely fashion. Reality dictates that one change the necessary steps and reduce the amount of the process it takes to get parts; in other words, the designer will want to make the change on a layout. Auto-routing results in a jumble of wires which defeats fast fixes to most circuits.

A small but rapidly growing need is a graphical interface between CAE systems. Perhaps this should be accomplished by establishing a standard intermediate format containing graphical information within a netlist; CAE vendors would then have to provide a means to input this information to their

respectivedatabases. An option to the standards is for a set of database trnaslation programs to allow conversion of, for example, a Daisy schematic onto a Valid workstation. This, however, seems to be the least likely since each CAE vendor would naturally like to protect the proprietary nature of the database.

Database translation is needed for easier interface to a growing set of customers using a variety of CAE systems. The advantage of translating schematic databases to other systems is clear for semicustom IC vendors: it would allow the vendor to customize his CAE interfaces around one system, instead of many types of systems.

A more global need is for a set of integrated conceptual design tools. This design environment would aid the designer in defining his logic problem, allowing the problem statement to be some kind of algorithmic description. Furthermore, this initial description should contain any specifics which become design implementation constraints. But most importantly, the initial specification would be used to verify the design as it progresses.

This type of tool would help provide assurance that the design is error free from the initial logic specification to test vector generation and prototype testing of parts by testing the final product based on the initial problem specification. This would, of course, demand that testability of logic integrated circuits be considered as part of the original design phase.

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EXPECTATIONS OF CAE MARKET

The greatest expectation I have about the CAE industry is that more economical workstations will become available. The use of IC technology in workstations guarantees continued price reduction, and demand from the market will continue to drive down prices as well.

We in the electronics industry have seen major improvements in the performance of computer systems since the introduction of semiconductor transistors. It is clear that this trend will continue for many years to come. My expectation of CAE vendors is to continue to provide more powerful hardware aa they themselves grow.

Finally, I expect CAE vendors to provide more verification tools and some sophisticated design aids. The market will demand these as the use of CAE workstations spread and users become familiar with what these systems can and can not do for them.

As a result of these expectations, most logic designers will perform their complete design function on the CAE workstation. Currently, only a part of the design work can be performed on a workstation; while conceptual design, performance specification, and test generation are missing, and other features (such as auto-routing, prototype testing, etc.) are very weak. These expectations are necessary to fulfill the needs of logic design on a CAE system.

FUTURE TRENDS

There are two future trends in the CAE industry which are evident at this time: 1) the move to specialized hardware for typically CPU intensive tasks, and 2) more powerful & less costly systems.

Specialized hardware for logic simulation is already here, evidenced by products like the Megalogician & Zycad Logic Evaluator. Prototype test equipment has been recently introduced, also. We will probably see fault simulation, analog simulation, and test vector generation in hardware in the near future. The advantages for this approach is that hardware is much faster than software and can be integrated into a workstation environment.

The trend towards more powerful and less costly systems should continue. In fact, an acceleration of this trend is expected because of the effects of technology feeding technology. That is, most workstation hardware is now being designed on workstations, thereby increasing the effiency of the design of the next generation products. In my knowledge, this is the case for Daisy, Valid, and Mentor-Apollo.

INTERNATIONAL MICROCIRCUITS INCORPORATED

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INTERNATIONAL MICROCIRCUITS INCORPORATED

- INCORPORATED 1972
- MANUFACTURING GATE ARRAYS SINCE 1974
- $12M SALES 1983
- 100 PEOPLE
- 25,000 SQUARE FEET
- 750+ INTEGRATIONS TO DATE
- 300+ CUSTOMERS

IMI

CAE FOR SEMI-CUSTOM INTEGRATED CIRCUITS

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SEMICUSTOM IC TRENDS

- INCREASING DEMAND FOR SEMICUSTOM CIRCUITS
- INCREASIGING DESIGN COMPLEXITY
- INCREASING PERFORMANCE OF IC'S

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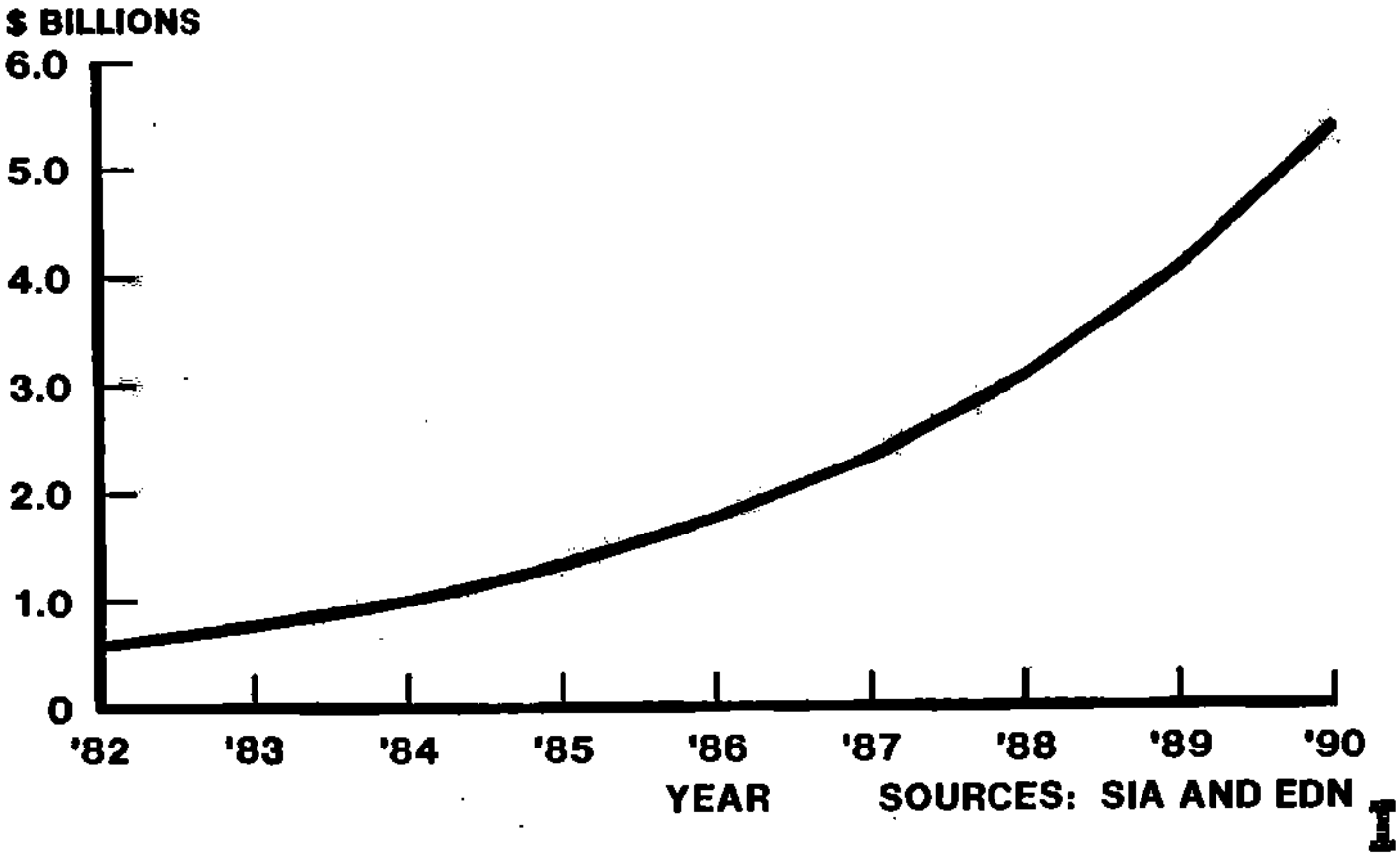
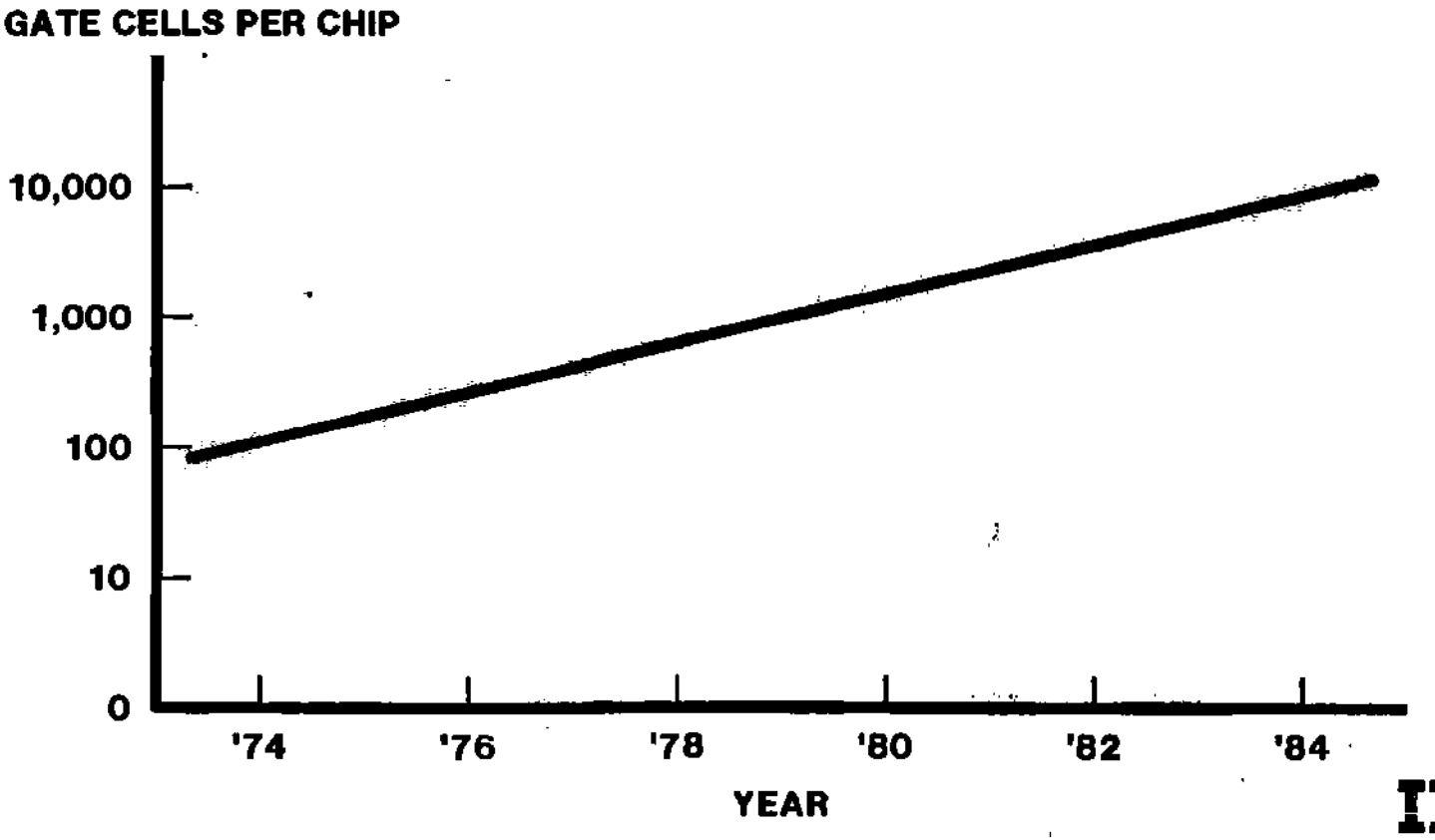
SEMICUSTOM IC MARKET GROWTH



INTERNATIONAL MICROCIRCUITS ARRAY DENSITY TREND



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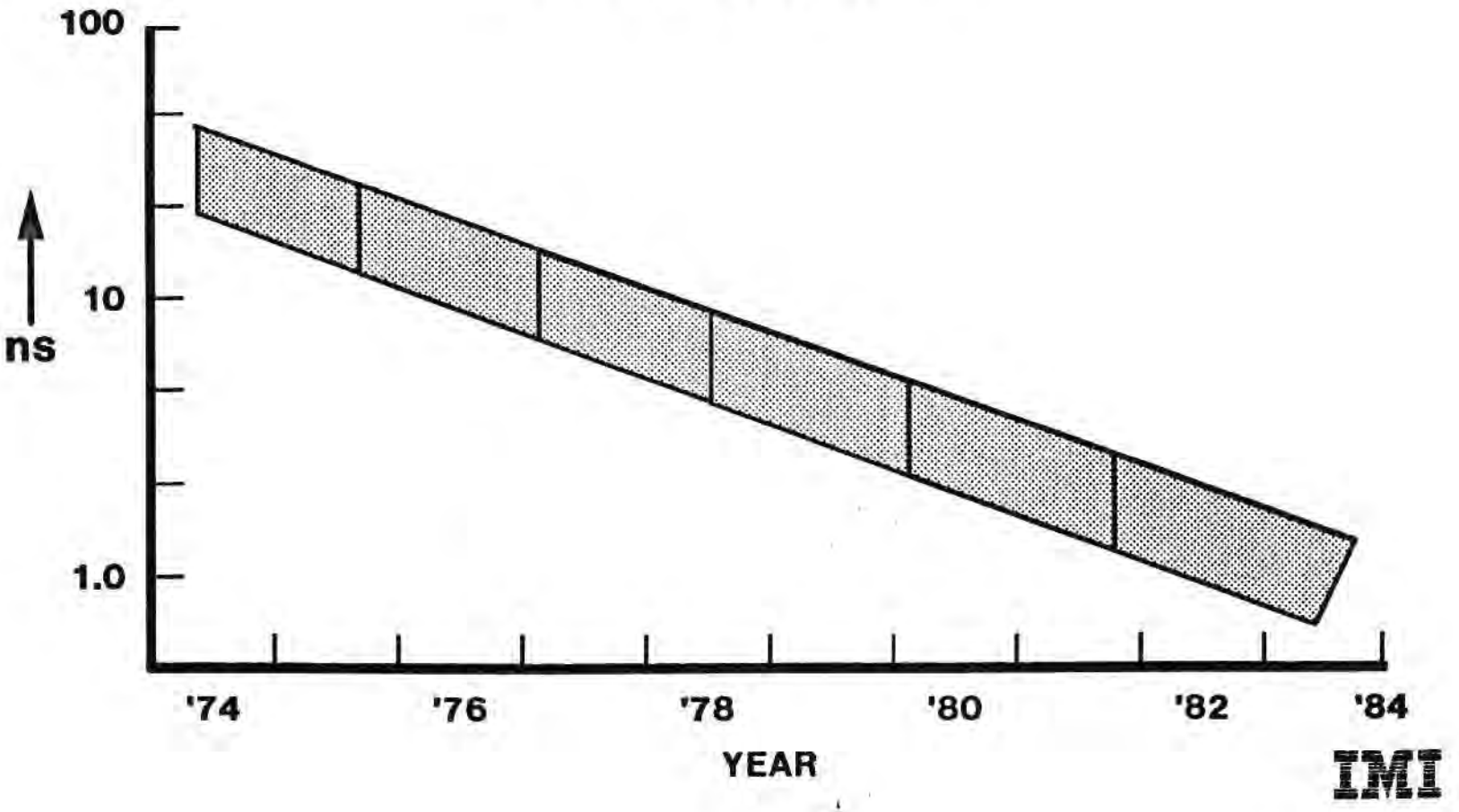
INVERTER DELAY
CMOS ARRAYS



SEMICUSTOM IC TRENDS

- TRENDS IMPLY NEED TO REDUCE THE LENGTH AND NUMBER OF DESIGN CYCLE ITERATIONS IN ORDER TO MEET GROWING DEMAND

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WHY USE CAE WORKSTATIONS?

- **DESIGN AIDS FOR CUSTOMERS**
  - **LOGIC SPECIFICATION & DOCUMENTATION**
  - **INTEGRATED LOGIC VERIFICATION TOOLS**
  - **RELATIVE LOW COST VS ALTERNATIVES**

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WHY USE CAE WORKSTATIONS?

- **ENHANCEMENT OF CUSTOMER INTERFACE**
  - **CORRECT TRANSFER OF LARGE DESIGNS**
  - **ACCESS TO LARGE MACRO CELL LIBRARIES**
  - **FEEDBACK INTO CUSTOMER'S DESIGN FLOW**

IMI

WHY USE CAE WORKSTATIONS?

- **ENHANCEMENT OF IMI DESIGN FLOW**
  - **INTERFACE TO PHYSICALIZATION**
  - **SCHEMATIC-DRIVEN DOCUMENTATION**
  - **PROVIDE CUSTOMERS SIMPLE ACCESS TO IC TECHNOLOGY**

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CAE TOOL NEEDS

- **MORE POWER AT LOWER COSTS**
  - **REDUCE DESIGN CYCLE**
  - **LARGER DESIGN CAPACITY**
  - **MORE DESIGN VERIFICATION**

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CAE TOOL NEEDS

- **EFFICIENT PHYSICAL LAYOUT AUTOMATION**
  - **REDUCE SILICON COSTS**
  - **LARGER DESIGNS ON SILICON**
  - **EDIT CAPABILITY OF LAYOUT**

IMI

CAE TOOL NEEDS

- **GRAPHICAL INTERFACE BETWEEN CAE SYSTEMS**
  - **CAE INDUSTRY STANDARDS OR**
  - **CAE SYSTEM DATABASE TRANSLATIONS**
  - **SEMICUSTOM VENDOR INTERFACE SUPPORT REQUIREMENTS**

IMI

CAE TOOL NEEDS

- **CONCEPTUAL DESIGN TOOLS**
  - **LOGIC SPECIFICATION**
  - **TEST VECTOR GENERATION**
    - **TESTABILITY IS A DESIGN ISSUE**
  - **PROTOTYPE TESTING**

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EXPECTATIONS OF CAE MARKET

- MORE ECONOMICAL WORKSTATIONS
- MORE POWERFUL WORKSTATIONS
- MORE DESIGN AIDS & VERIFICATION TOOLS
- RESULT: MOST LOGIC DESIGNS PERFORMED ON WORKSTATIONS

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FUTURE TRENDS

- **SPECIALIZED HARDWARE**
  - **LOGIC SIMULATION IS HERE**
  - **PROTOTYPE TESTING RECENTLY INTRODUCED**
  - **FAULT SIMULATION**
  - **ANALOG SIMULATION**
  - **TEST VECTOR GENERATION**

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FUTURE TRENDS

- **MORE POWERFUL & LESS COSTLY SYSTEMS**
  - **IC PRICE-PERFORMANCE TRENDS WILL CONTINUE**
  - **TECHNOLOGY FEEDS TECHNOLOGY**
  - **MENTOR - APOLLO**
  - **DAISY**
  - **VALID**

IMI

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USER PANEL DISCUSSION

Karl Nakamura
Senior Member of the Technical Staff
GRiD Systems

Mr. Nakamura is a Senior Member of the Technical Staff at GRiD Systems. He has been with GRiD for more than three years, and has participated on the GRiD Compass design team. Previously, Mr. Nakamura was with Hewlett-Packard as a Research and Development Engineer in the Scientific Instruments Division. Mr. Nakamura received an M.S.E.E. degree from Stanford University.

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May 10-11, 1984
Sunnyvale, California

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INTEGRATED SYSTEMS TECHNOLOGY: VLSI DESIGN AUTOMATION FOR SYSTEMS ENGINEERS

Phillip A. Kaufman
President
Silicon Compilers Incorporated

Mr. Kaufman is President of Silicon Compilers Incorporated and has 18 years of experience developing and managing software, systems, and integrated circuit programs and organizations, and strategic and product planning. He was previously with Intel Corporation, where he served as Director of Engineering, in Corporate Strategic Planning, and as General Manager of the Microprocessor Operation. Mr. Kaufman was the driving force behind both the development and acceptance of the IEEE Floating Point Standard and the organization of the Xerox/Digital Equipment/Intel joint program that resulted in the Ethernet standard. Prior to joining Intel, Mr. Kaufman was Director of Engineering and Director of Planning at Computer Automation Incorporated. Mr. Kaufman received B.S.E.E. and M.S.E.E. degrees from the University of Michigan.

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INTEGRATED SYSTEMS TECHNOLOGY:

VLSI DESIGN AUTOMATION FOR SYSTEMS ENGINEERS

Phillip A. Kaufman
Silicon Compilers Incorporated

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INTEGRATED SYSTEMS TECHNOLOGY: VLSI DESIGN AUTOMATION FOR SYSTEMS ENGINEERS

INTRODUCTION

Since the advent of the transistor, semiconductor technology has had a profound effect upon the design and construction of all types of systems. The impact of semiconductor technology has grown rapidly as the technology evolved from transistors to integrated circuits and as the available integrated circuit density has increased. With the evolution from SSI to MSI to LSI to VLSI, the complexity of all types of systems has increased dramatically while costs have declined and reliability has improved. Today, it is a well accepted fact that competitive systems products must make maximum use of Very Large Scale Integration.

Despite the revolution in available silicon density, there has been surprisingly little change in the past twenty years in the way in which systems and integrated circuits are designed. Systems designers still rely primarily upon standard products developed by integrated circuit suppliers. The integrated circuits themselves are developed by a relatively small number of IC design craftsmen. Computer Aided Design (CAD) and Computer Aided Engineering (CAE) have helped to address the problems of designing ever more complex components. However, CAD and CAE have focused primarily upon individually computerizing many of the classical steps required to implement VLSI components. As a result, despite all of the efforts that have gone into CAD development for IC design, the best that has been accomplished has been to keep the already very long development times from growing totally out of sight as complexity has increased.

The advent of the microprocessor caused a dramatic revolution in the way in which systems were designed. No longer was it necessary for the system implementor to design the entire product from functionally small individual components. Now the system implementor could design much of the functionality through software and use powerful low cost microprocessors to implement the heart of the system. The first users of microprocessors found that they had a substantial advantage over their competitors. But the microprocessor revolution is over. With microprocessors appearing everywhere in virtually every system, their use has become evolutionary rather than revolutionary.

Microprocessors also achieved one goal that is often overlooked. They became the way that integrated circuit suppliers could define very complex components which could exploit the available silicon density and still address a very broad market. This characteristic is extremely important since, other than memory devices, microprocessors are in general the only very complex Integrated Circuits with a large enough market to justify the enormous development costs. Standard product manufacturers find

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it very difficult to define a large number of products that have sufficient functionality to fully exploit the available silicon density while still having a broad enough market to justify the investment. This difficulty arises from the fact that today's VLSI devices are not so much individual components as they are complete systems and subsystems. Unless many, many systems designers build virtually the same system, it is very difficult to sell large volumes of a complex integrated circuit.

With VLSI components becoming major parts of end systems, it is no longer possible for the integrated circuit design engineer to also have sufficient applications knowledge to define the components needed. Thus, we have come to somewhat of an impasse in the industry. The systems designers who have the applications knowledge and have the need to integrate their systems into one or more VLSI circuits do not have the IC design knowledge or the tools to execute the design. At the same time the IC designers do not have the systems applications knowledge or the volume markets necessary to develop components that are actually major parts of complex systems.

THE CUSTOM REVOLUTION

Custom and semi-custom technologies have lately received a great deal of attention. The attention, from the systems developer, arises from a recognition of the many benefits of using high density silicon in systems products. The attention, from the integrated circuit suppliers, comes from a recognition of the difficulty of defining many high density standard products and the large potential market represented by custom and semi-custom designs. Dataquest has estimated that by 1990 nearly half of all integrated circuits shipped will be some form of Application Specific Integrated Circuit (ASIC) (Figure 1). The ASIC market segment includes all forms of custom, semi-custom, and mask programmable devices. The custom and semi-custom segments alone will account for in excess of $10 Billion in 1990 shipments. These forecasts, however, beg the question of just who will design all of these custom and semi-custom ICs and what type of design tools the designers will use. The forecasts of very rapid growth in the ASIC market are certainly justified in terms of the number of systems built per year and the potential that exists for penetrating this market. The forecasts can not be met, however, unless systems engineers are able to do the designs and unless tools exist to execute the designs rapidly and cost effectively.

Existing approaches to user designed VLSI have focused upon ways to eliminate the need to design polygons and transistors by using predesigned cells such as are used in Gate Array and Standard Cell systems. These approaches make significant sacrifices in silicon density in order to use predesigned (and often preplaced) cells. Little has been done to make the task of designing complex systems more efficient.

What has actually happened with the use of Gate Arrays and Standard Cell systems is to set the systems design engineer's design methodology back ten years. Over the last ten years, the systems engineer has been given ever more complex building blocks from which he could construct very complex systems. He could use Medium Scale Integrated circuits (MSI), Large Scale Integrated circuits (LSI), and Very Large Scale Integrated circuits (VLSI) and not have to decompose his design into literally hundreds of thousands of gates or transistors. The effect of most Gate Array and Standard Cell systems is to take away from the engineer his MSI, LSI, and VLSI catalogs and give him back a catalog of Small Scale Integrated circuits (SSI) while asking him to design systems substantially more complex than those designed ten years ago.

For the custom revolution to be realized, a new design technology is required. A technology that allows systems engineers to rapidly and efficiently design integrated systems. One that addresses the entire-design engineering process focusing upon design methodology and a complete integrated set of tools that not only implements efficient silicon realizations of the design but that substantially shortens the design time. In today's rapidly evolving markets, time to market is often the single most critical edge that a manufacturer can have. With the ever increasing complexity of VLSI, time to market becomes a design-time issue far more than a manufacturing-turn-around time issue. The optimum solution is a systems-integration technology that combines the shortest possible design time with the most cost-effective silicon implementation.

INTEGRATED SYSTEMS TECHNOLOGY

Integrated Systems Technology encompasses the products, services, and expertise that allows the systems engineer to take advantage of the benefits of VLSI and rapidly and efficiently design end systems products. With Integrated Systems Technology, the systems engineer can fully exploit the reduced size, increased speed, lower cost, lower power, and product uniqueness potential of VLSI. No longer is it necessary to have a large team of IC design craftsmen in order to implement efficient integrated circuits. The systems engineer can develop systems on silicon without the need to be retrained as an integrated circuit designer and without paying the cost and chip-size penalties associated with compromise technologies.

There are two key aspects of any design technology: design efficiency and implementation efficiency. Design efficiency refers to the time and manpower required to perform the design. Implementation efficiency refers to the cost effectiveness of the resulting design. Unless both types of efficiency are available, the applicability of a design technology is severely limited.

The basis for a real Integrated Systems Technology is silicon compilation. Silicon compilation provides both an extremely

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productive design methodology and integrated circuit implementations that are essentially as dense as hand-crafted designs. Design efficiency is achieved by addressing the entire design cycle, from concept to tape-out, and providing a complete set of tools that maximizes the design engineer's leverage. Silicon implementation efficiency is achieved by actually constructing the exact required functionality using a built-in set of knowledge based rules.

SILICON COMPILATION

Silicon compilation is far more than Computer-Aided-Design (CAD) or Computer-Aided-Engineering (CAE). It is true design automation. This distinction is both qualitative and quantitative and results in a very different focus in both developing and using the silicon compilation system. Classical CAD and CAE approach the automation of design by looking at the way in which design and implementation have been done in the past and looking for opportunities to shorten each step. Silicon compilation, on the other hand, looks to the design cycle and asks the question "Where can the engineer's knowledge and expertise be best exploited and where can the capabilities of the computer not only ease the task but even eliminate major parts of the design effort?"

The difference between CAD/CAE and design automation is illustrated in Figure 2. The top line in the Figure portrays the classical IC design cycle from definition to tape-out. Each step of the process involves both design and verification or simulation of the design work. In addition, of course, each step must be verified to be sure that the work done matches the work done in the prior step. CAD and CAE address primarily the implementation steps after the higher level design work has already been completed. We even speak of "design entry" meaning capturing of a design that is essentially accomplished without the assistance of the system. The only real assistance that the CAD/CAE system provides is to replace paper with a CRT screen, maintain a database of the design, and perform basic error checking. Thus, the definition phase is unaffected while each of the subsequent steps is compressed slightly. In sharp contrast to this approach, the design automation of silicon compilation not only shortens the definition and architectural phase, it improves the quality of the work and totally eliminates the later stages. The result is complex designs executed in a few months by one or two engineers, compared to similar designs done by tens of engineers over a multi-year project.

Silicon compilation has many features and attributes of interest to the systems design engineer. These are summarized in Figure 3. Silicon compilation is a complete design automation capability. It covers the entire design cycle and eliminates the need for the design engineer to perform the routine and labor-intensive implementation tasks. The design begins at the functional or micro-architectural level where the engineer can think in terms

of major functional blocks and the way in which they are connected. From the block level design the compiler synthesizes three different views of the design: layout geometry, functional simulation models, and timing models. Thus, the design is immediately ready to simulate and verify. In addition, the design is foundry-independent. The silicon compiler yields an optimum combination of both design efficiency and silicon efficiency.

DESIGN EFFICIENCY

Design efficiency in the silicon compilation methodology is achieved by matching the tools to the way in which an engineer really works. Engineering is a process of balancing often conflicting design goals and successive refinement of a design. An initial specification for a design is never absolutely complete and seldom adequately reflects all of the metrics to be used in making design tradeoffs. Real designs are accomplished by selecting an implementation approach, partially implementing the approach in order to evaluate the results, and then altering the approach as needed to best match the project's goals and constraints. Unfortunately, until now, the task of doing a partial implementation in order to get real results to evaluate was so expensive that it has been impossible to evaluate several alternative approaches and select the optimum one. Because of the ability of a silicon compiler to take an initial design specification and immediately turn it into an implementation, it is now possible to explore multiple implementation alternatives. This exploratory-design phase yields many benefits. A compiler designed to accept minimal input information and interactively return design parameters such as speed, power, and die size allows the design engineer to use his creativity to explore many alternatives in ways that were previously impossible. The result is often a far superior design to any that could be achieved before.

An additional benefit of the concept of exploratory design is that it leads directly to a design methodology well suited to iterative design. Real engineering is iterative. It is necessary to incrementally refine definition and implementation while simultaneously evaluating and verifying the implementation. A silicon compiler developed with the philosophy of being the design engineer's partner accepts a little input and provides maximum feedback on the results of that input. It also treats the layout geometry, functional simulation, and timing analysis of the design in progress as three views of the same design. This approach enables and encourages exploratory design and iterative design resulting in rapid convergence on an optimum implementation.

HIERARCHICAL DESIGN

Hierarchical design, or structured design, is a design approach developed to make it possible to manage very complex design tasks, be they integrated circuits, software, or any other type

of design. The key attribute of hierarchical design is the breaking down of a design into a small number of relatively large functions and then recursively breaking down each of these functions to lowerest level until the design is completed. Figure 4 illustrates a pyramid of design levels, beginning at the top with large VLSI-level functions and descending through LSI, MSI, all the way to polygons. While CAD/CAE systems stress the need to perform hierarchical design in order to manage the immense complexity of VLSI design and provide tools to assist the designer in this process, the pyramid must still be traversed from top to bottom. This process of successive decomposition to the levels of gates, transistors, or polygons, is very time consuming and error prone. A silicon compiler, on the other hand, provides the designer with maximum leverage by allowing the design to focus at the highest possible levels and letting the design-automation system perform the necessary decomposition. This leverage is illustrated in Figure 5. By allowing the designer to completely execute a design at the level of large modules and blocks, without descending the hierarchy into a sea of details, the silicon compiler provides dramatic leverage for the designer. Without this leverage, no design system is adequate to the enormously complex task of designing a complex VLSI system.

IMPLEMENTATION EFFICIENCY

Implementation, or silicon, efficiency is determined primarily by the quality of circuit and interconnect wiring execution. A silicon compiler has a substantial advantage in silicon efficiency over other approaches to custom or semi-custom implementation. In either gate array or standard cell design systems, small predesigned cells are interconnected to meet the needs of the design. In these approaches, cells are quite small and are designed without regard for how the cells will be combined to construct larger functions. The result is that a very high percentage of the chip area ends up being used for interconnect wiring. Wiring, however, is the most expensive chip resource. The heavy use of inter-cell wiring in gate array and standard cell systems results in very inefficient implementations.

Another factor affecting silicon efficiency is the appropriateness of the available cells for the particular design being executed. A library-based system will always be limited by the available library. Often a 'next larger' cell is used because exactly the function needed is not available. A silicon compiler, however, is not based upon a library of objects (cells). Rather, it is based upon a knowledge base of rules for the construction of large families of functions. Thus, a compiler constructs exactly the function required.

The compiler composes large functions that are exactly the functions required for the design. Thus, the amount of interconnect wiring is minimized and the compiler is able to

achieve essentially the same densities as a hand-crafted design. Actual density comparisons of production designs developed with a silicon compiler show that the total chip area per transistor and the percentage of chip area devoted to interconnect are comparable to the best hand-crafted designs. With the additional capability of doing exploratory design with the compiler, typical designs have the opportunity to be even denser than hand-crafted designs.

In the past, custom or semicustom designs could be justified by the size and cost savings achieved in the overall system. These designs did not themselves have to compete solely as stand-alone circuits. They could not compete because of the density penalty involved in the design technique. Seldom, if ever, did one see merchant-market standard parts designed with the same design tools used for custom or semi-custom design. The picture changes dramatically with a silicon compiler. The compiler implements integrated circuits of "merchant-market quality". The result is that custom parts need no longer be much more expensive than equivalent functionality standard parts. In addition, standard parts can now be implemented with the time to market advantage of the most effective custom design tools.

APPLICATIONS AREAS

A silicon compiler has a very broad area of application. The unique combination of design efficiency and silicon efficiency makes a silicon compiler appropriate across a wide range of complexities and volume. Figure 7 illustrates application areas as a function of both volume and complexity. At low volumes and relatively low complexities gate arrays are an appropriate implementation technique. They are, however, quite limited in density and complexity and are not as cost effective as compiled or hand-crafted implementations. At slightly higher complexities standard cell systems become more desirable than gate arrays. The somewhat larger cells of a standard cell system and the greater density compared to gate arrays makes them more attractive. At the extremes of ultra high volumes and complexities hand-crafted designs will always prevail. Across the broadest range of volumes and complexities, however, a silicon compiler is optimum. Its high densities make it preferable to gate arrays or standard cells at moderate to high volumes. Its rapid design capabilities, including exploratory design, make the silicon compiler the only feasible tool for high complexity designs. While gate arrays will persist as a viable technology for low complexity, low volume, quick turnaround time, the growth of gate arrays into higher and higher densities will be limited by the much more attractive silicon compilation technology. Standard cell systems are apt to be replaced entirely by the much more capable silicon compilation technology.

REAL DESIGNS

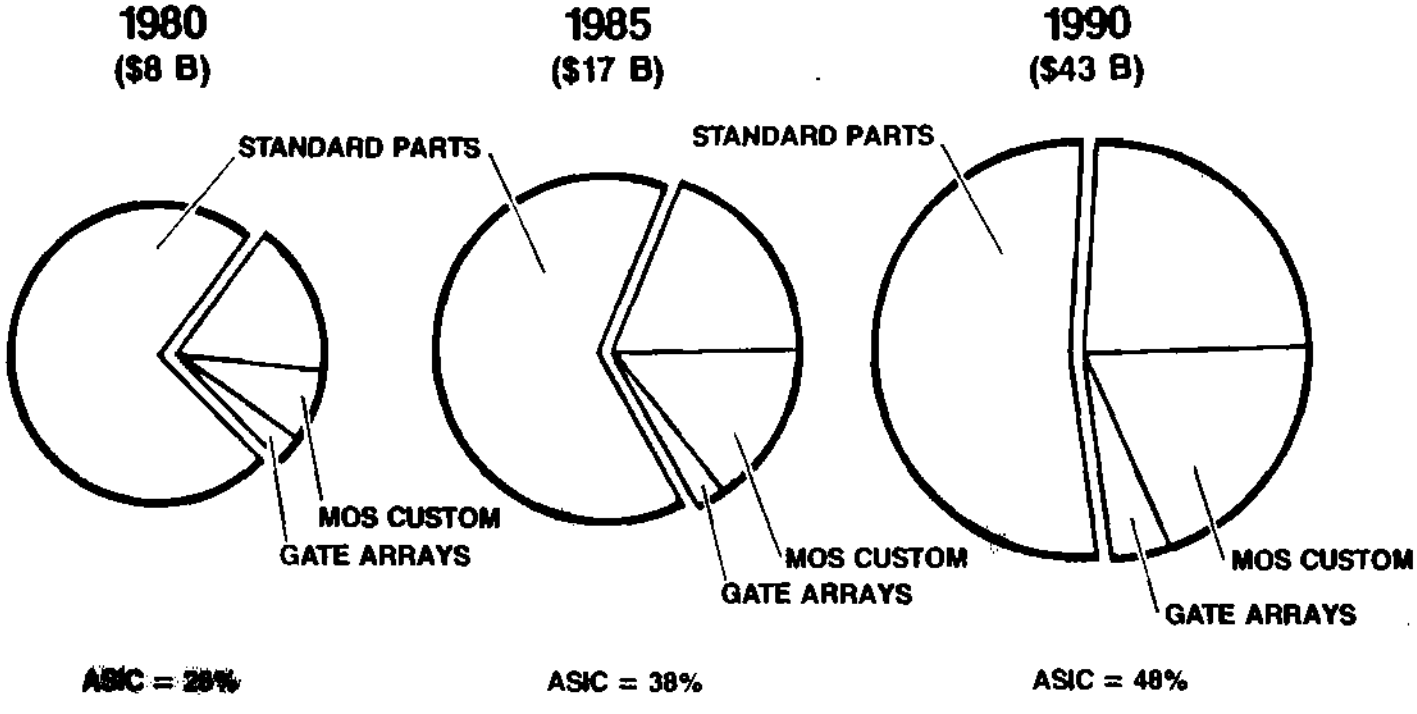
No design technology can be proven effective without actually using it. Prototypes of Silicon Compilers Incorporated's compiler have actually been used to develop several major VLSI components. These components illustrate the power of Integrated Systems Technology: dramatic reductions in development time and very high density implementations. Figure 6 shows the MicroVAX 1 (tm) component developed by Silicon Compilers Incorporated for Digital Equipment Corporation. This part brings the VAX (tm) computer out of the computer room and onto a desk top. The entire VAX processor, including virtual memory management, is contained on just two Quad boards. Development took just seven months from contract inception to working silicon. Transistor density is comparable to that of the best commercial microprocessors on the market. By simultaneously developing both the MicroVAX system and the custom part, Digital Equipment Corporation was able to bring the final product to market in approximately one year versus the multi-year typical development cycles associated with other custom or semi-custom approaches.

Other components developed by Silicon Compilers Incorporated include the world's first commercial Ethernet (tm) controller and a RasterOp graphics chip. The Ethernet controller is sold under license from Silicon Compilers by SEEQ Technologies Inc. The RasterOp chip allowed Sun Microsystems Inc. to reduce the size of their advanced workstation product and bring the product to market just ten months from the beginning of its definition.

SUMMARY

Integrated Systems Technology, based upon silicon compilation, allows the systems engineer to exploit the capabilities of Very Large Scale Integrated circuits. Without retraining to become an IC designer, the systems engineer can produce components with densities that arefully competitive with commercial hand-crafted designs. By addressing the entire design cycle and, in particular, focusing upon the definition and architecture phases, the total time from concept to market is dramatically reduced. Silicon compilation brings a totally new level of design capability to systems developers - true Design Automation. The impact will be a dramatic increase in the number of custom designs and significant reductions in time to market. Standard part suppliers will also benefit from the use of silicon compilers. For the first time they will have available design tools capable of rapidly designing merchant-market-quality parts.

Custom IC Design Market



ASIC = Application Specific Integrated Circuits

Source: Dataquest, Incorporated 1982

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Figure 1

Design Leverage Comparison

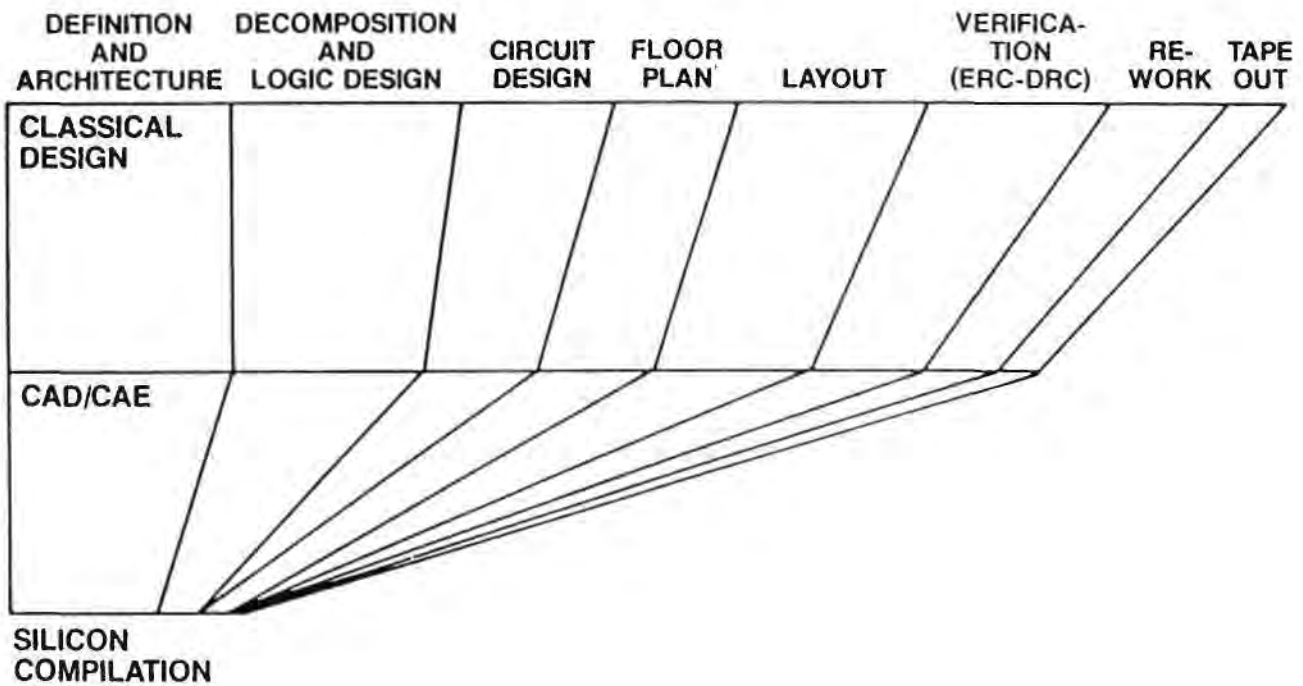

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Figure 2

Silicon Compilation-Overview

- **Complete Design Automation**
- **High Level Micro Architecture Input**
- **Synthesis of All Required Views**
  - **Layout Geometry**
  - **Functional Simulation Models**
  - **Timing Analysis Models**
- **Technology Independence**
- **Optimum Combination of**
  - **Design Efficiency**
  - **Silicon Efficiency**

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Figure 3

Design Efficiency: Implementation Medium

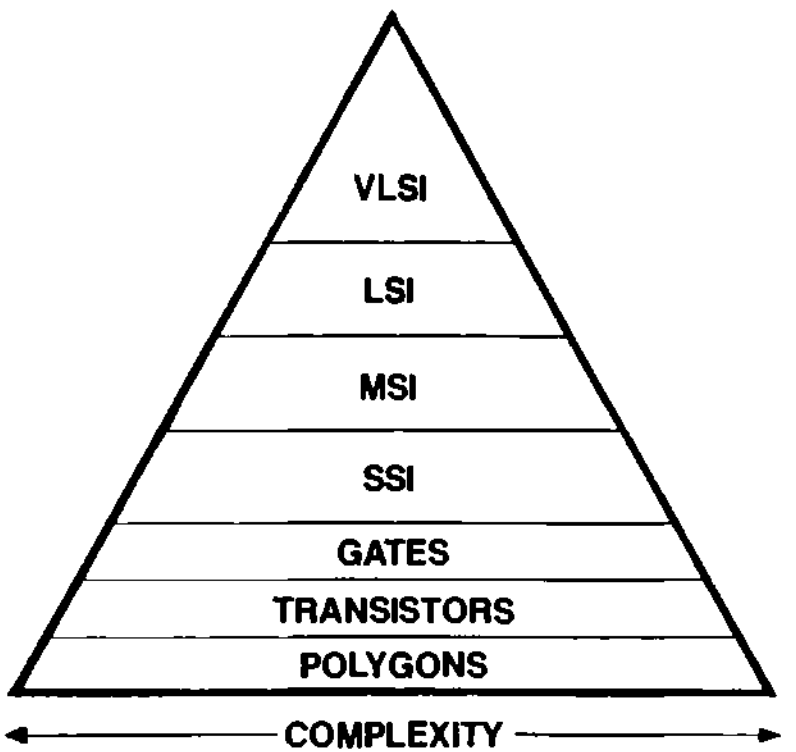

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Figure 4

Design Efficiency: Complexity Management

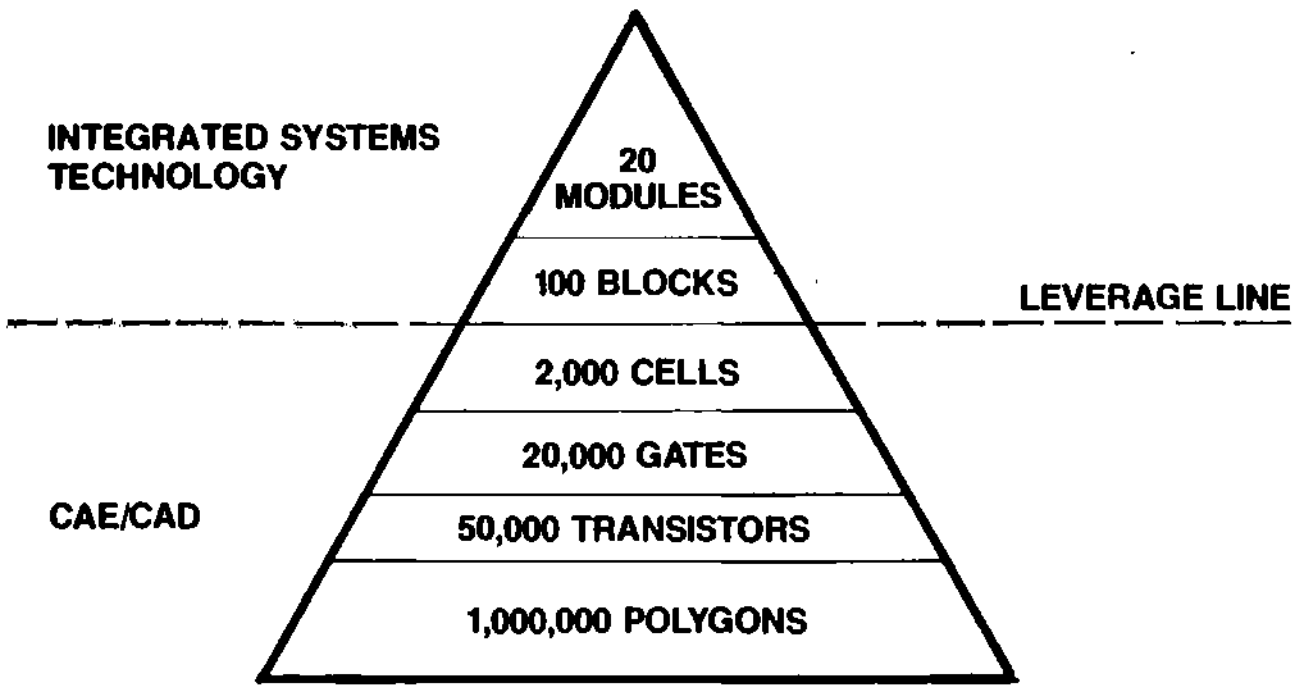

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Figure 5

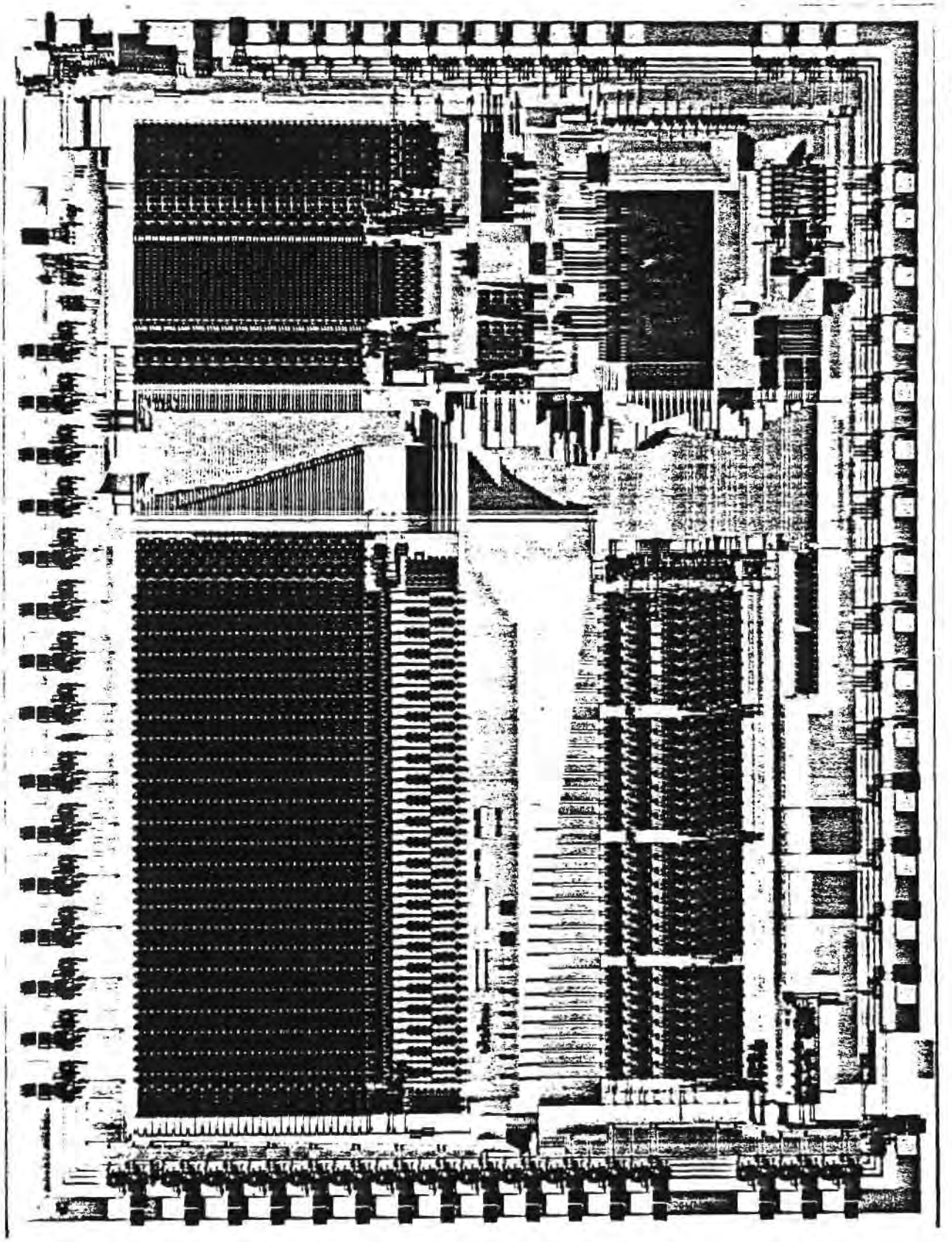

Figure 6

Applications Areas

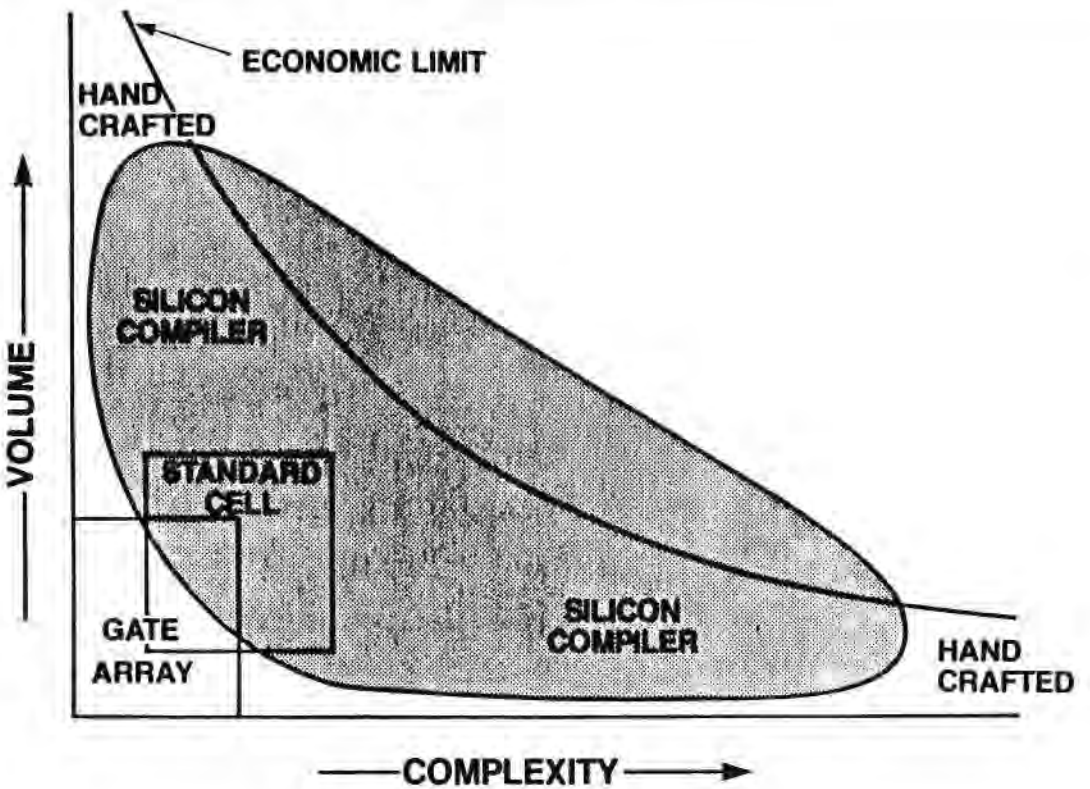

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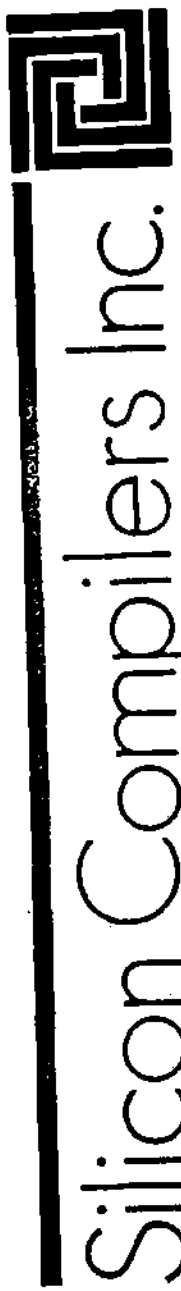
Figure 7



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Integrated Systems Technology:

VLSI System Technology for Systems Engineers

090

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Today, Competitive Systems Require...

Maximum Use of Very Large Scale Integration

Silicon Compilers Inc.

VLSI Benefits

- **Smaller Size**
- **Lower Cost**
- **Higher Performance**
- **Higher Functionality**
- **Higher Reliability**

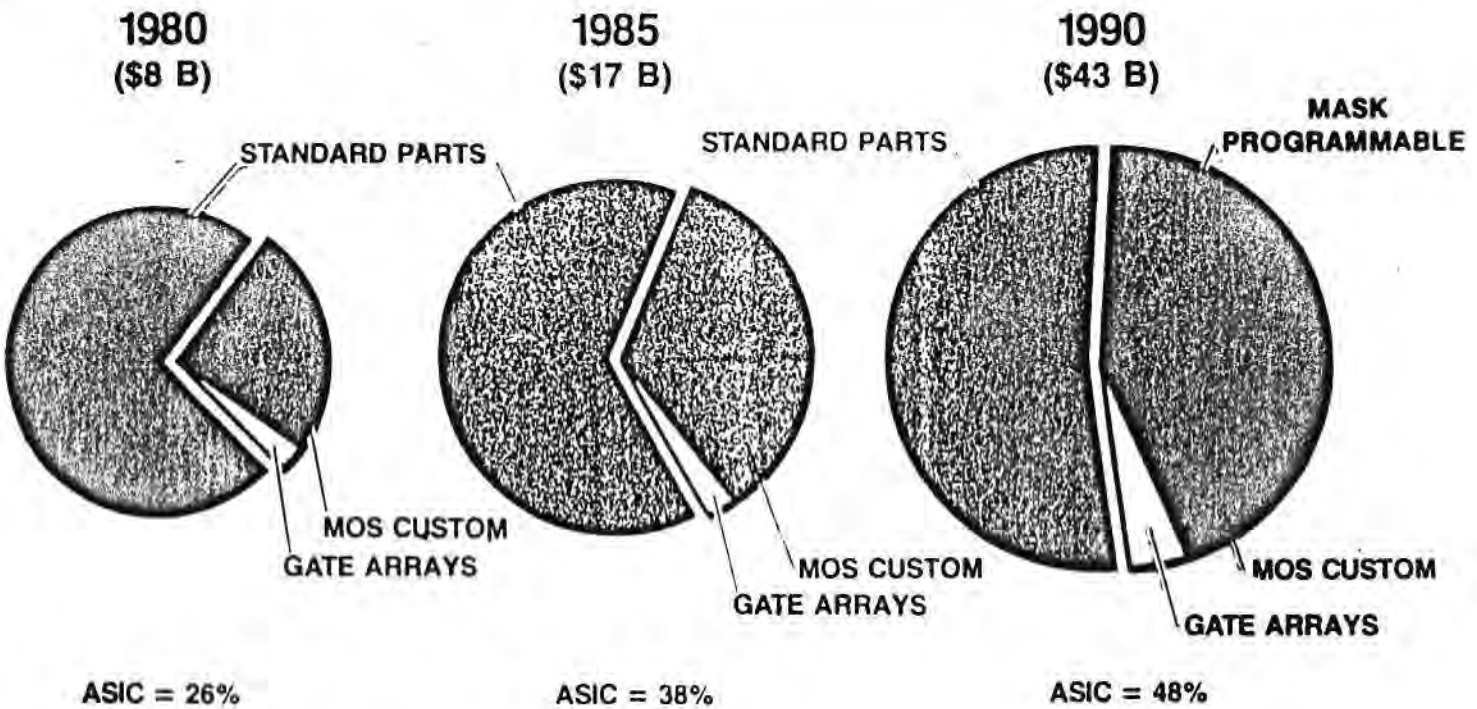
Standard Products are Limited

- Force Fit for Applications
- Do Not Offer Product Uniqueness
- Difficult for Vendors to Define Sufficient Functionality and Generality
- Best for Memories and Microprocessors
- Insufficient for Optimum System Integration
- The Microprocessor Revolution is Over

Custom...The Next Systems Revolution

- **Required for a Competitive Edge**
- **Silicon Density Allows Truly Integrated Systems**
- **All of the Benefits of Very Large Scale Integration**
- **Foundries Make Production Available**

Custom IC Design Market



ASIC = Application Specific Integrated Circuits

Source: Dataquest, Incorporated 1982

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Barriers to Integration

- VLSI Design Requires
  - Skilled IC Design **Craftsmen**
  - Long Lead Times
  - Large Development **Costs**

  OR

- Compromise Design Approach
  - Limited Density
  - Limited Tools

The Missing Link

INTEGRATED SYSTEMS TECHNOLOGY

that allows systems engineers to rapidly and efficiently design electronic end products

Silicon Compilers Inc.

Integrated Systems Technology Goals

- **Exploit Silicon in Systems**
- **Obtain Size, Speed, Cost, Power, Uniqueness Benefits of VLSI**
- **Use by Systems Engineers**
- **Rapid Design**
- **Efficient Silicon**
- **Process Portability**

Silicon Compilation

THE KEYSTONE OF INTEGRATED SYSTEMS TECHNOLOGY

- **Complete Design Methodology and Tools**
- **Matched to Real Engineering Process**
- **Encapsulates IC Design Knowledge**
- **Optimum Designs by Systems Engineers**

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Silicon Compilation

IS NOT Computer-Aided Design
IS NOT Computer-Aided Engineering

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Silicon Compilation

IS Design Automation

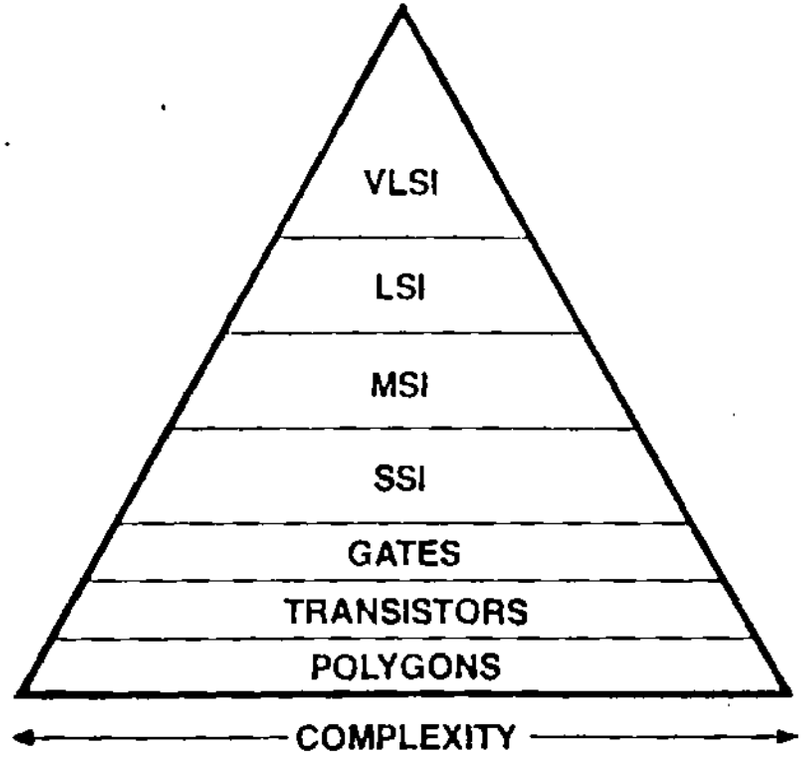
Silicon Compilation-Overview

- **Complete Design Automation**
- High Level Micro Architecture Input
- Synthesis of All Required Views
  - Layout Geometry
  - Functional Simulation Models
  - Timing Analysis Models
- Technology Independence
- Optimum Combination of
  - Design Efficiency
  - Silicon Efficiency

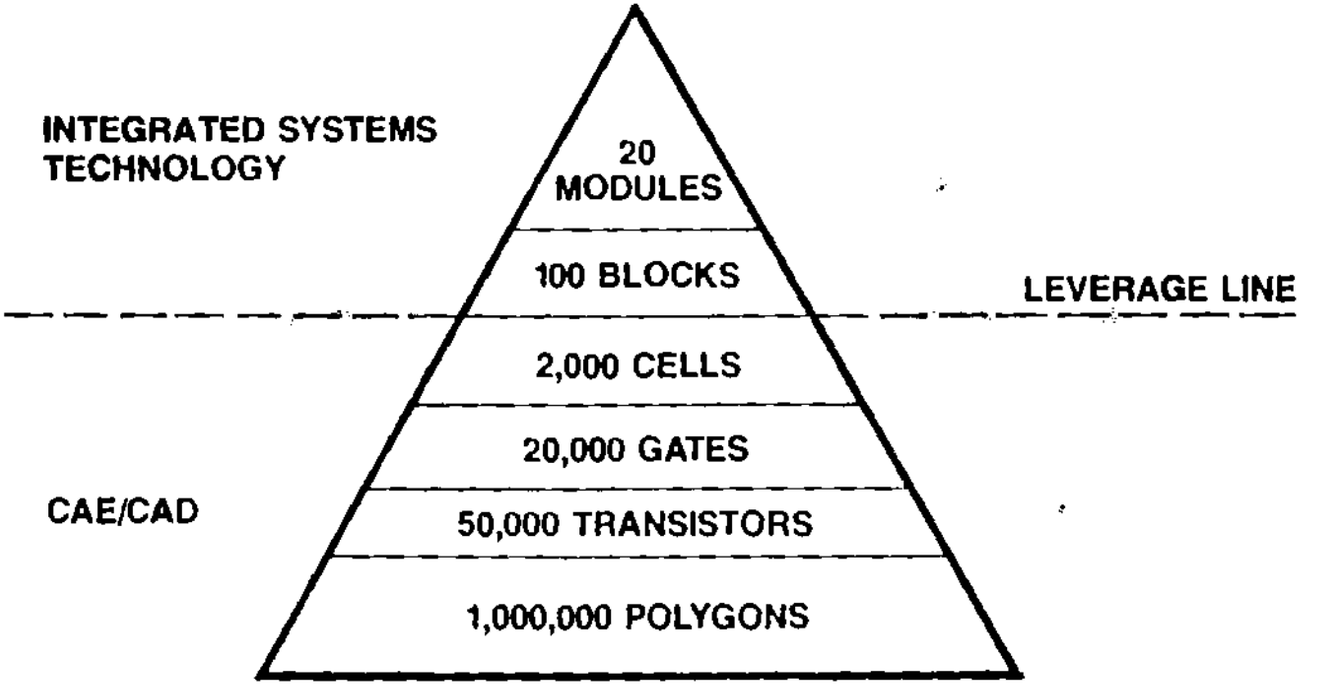
Design Efficiency

- Hierarchically Structured
  - Complexity Management
- Rapid Design Feedback
  - Exploratory Design
- Interactive and Incremental
  - Iterative Design

Design Efficiency: Implementation Medium



Design Efficiency: Complexity Management



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Silicon Efficiency

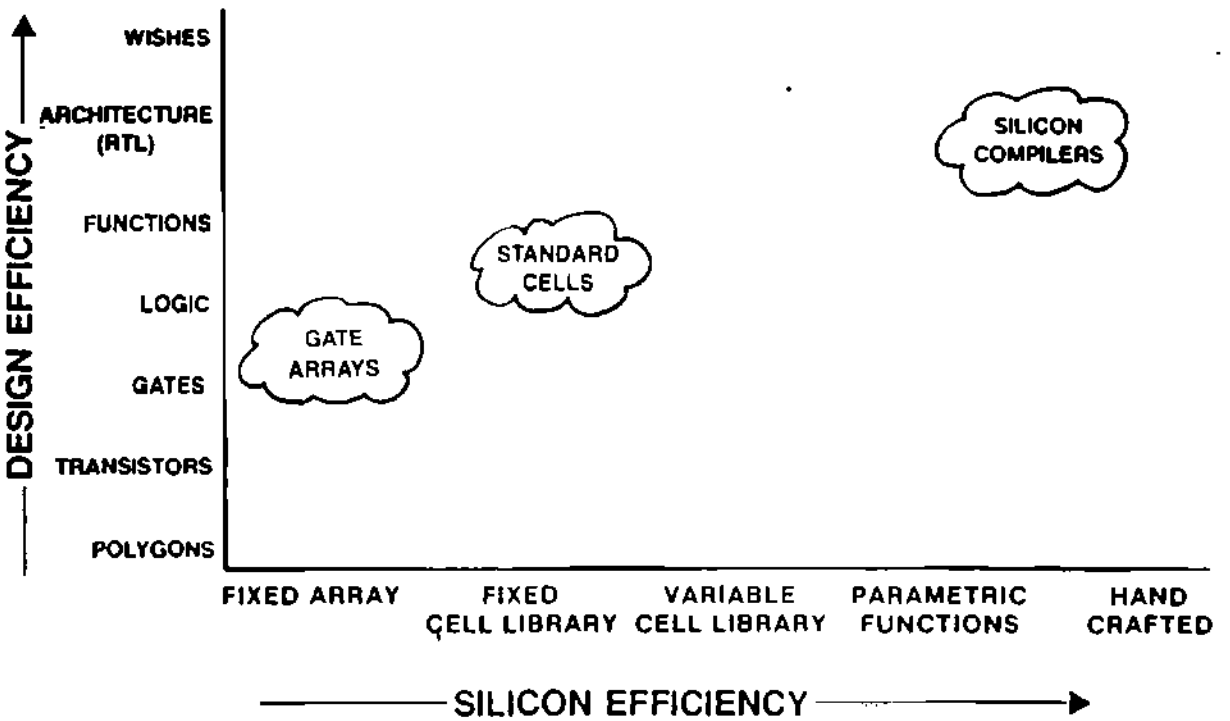
- **Builds Exactly the Functions Needed**
- Optimum Implementation
- Minimum Interconnect Wiring
- **Merchant Market Quality Implementation**

Silicon Efficiency Analysis

	iAPX 80286™	MicroVAX™ 1
Die Area (sq. mils)	119K	97K
# of Transistors	52K	37K
# of Blocks	55	18
Area/Transistor (sq. mils)	2.3	2.6
% Area for Routing	38%	43%

* Normalized to the same feature size. ROM not considered on 286.

VLSI Design



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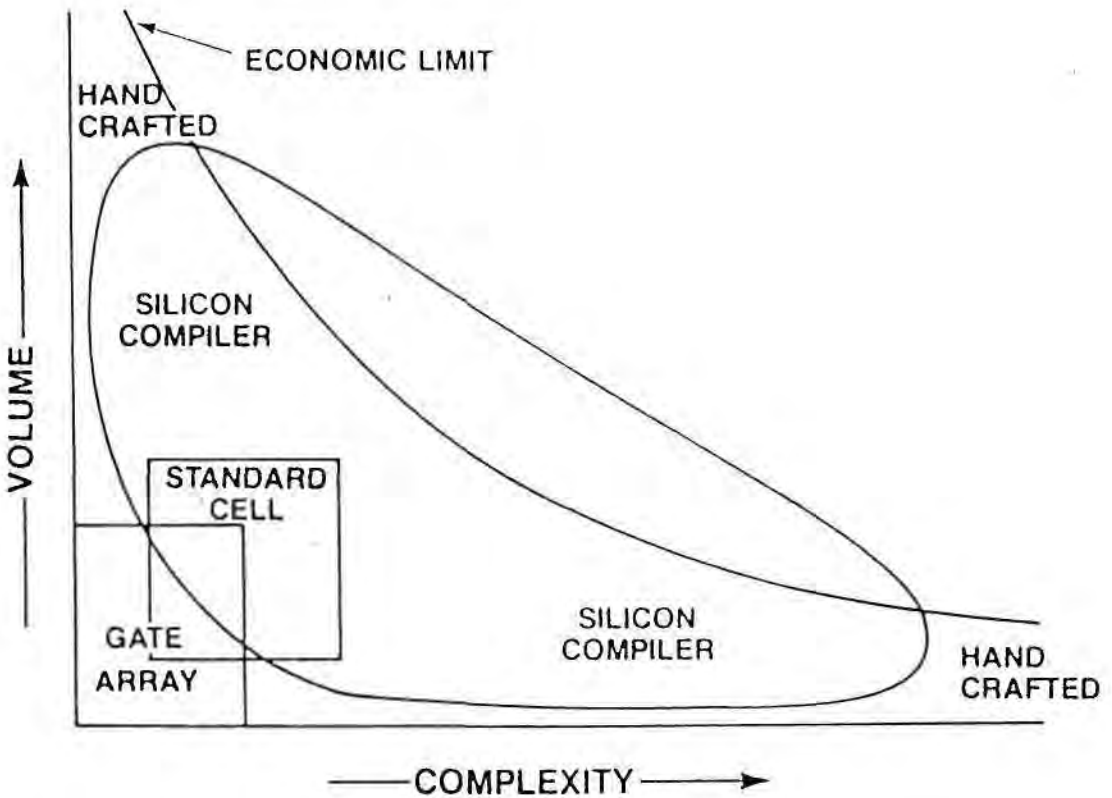
Applications Areas



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Silicon Compilation: Myths and Reality

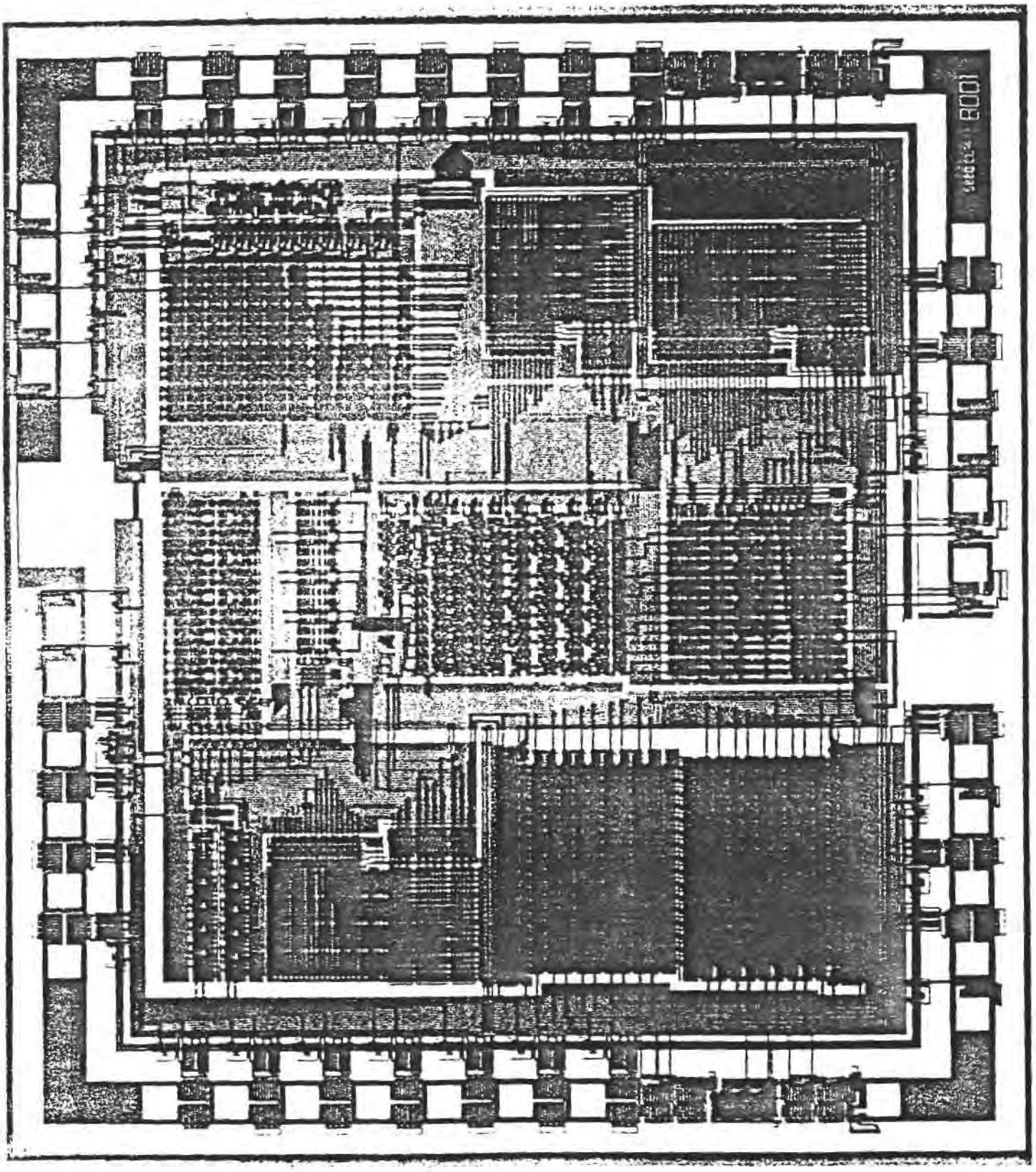
- **Myths**
  - **Just a Research Topic**
  - **Limited to Fixed Architectures**
  - **Someday . . .**
  - **Spec In - Chip Out**
  - **The Panacea**

- **Realities**
  - **Proven Capabilities**
  - **Industrial Strength**
  - **Available soon from Silicon Compilers Incorporated**

Ethernet Controller

Seeq Technology, Inc.

020



Graphics RasterOp Controller

SUN Microsystems, Inc.

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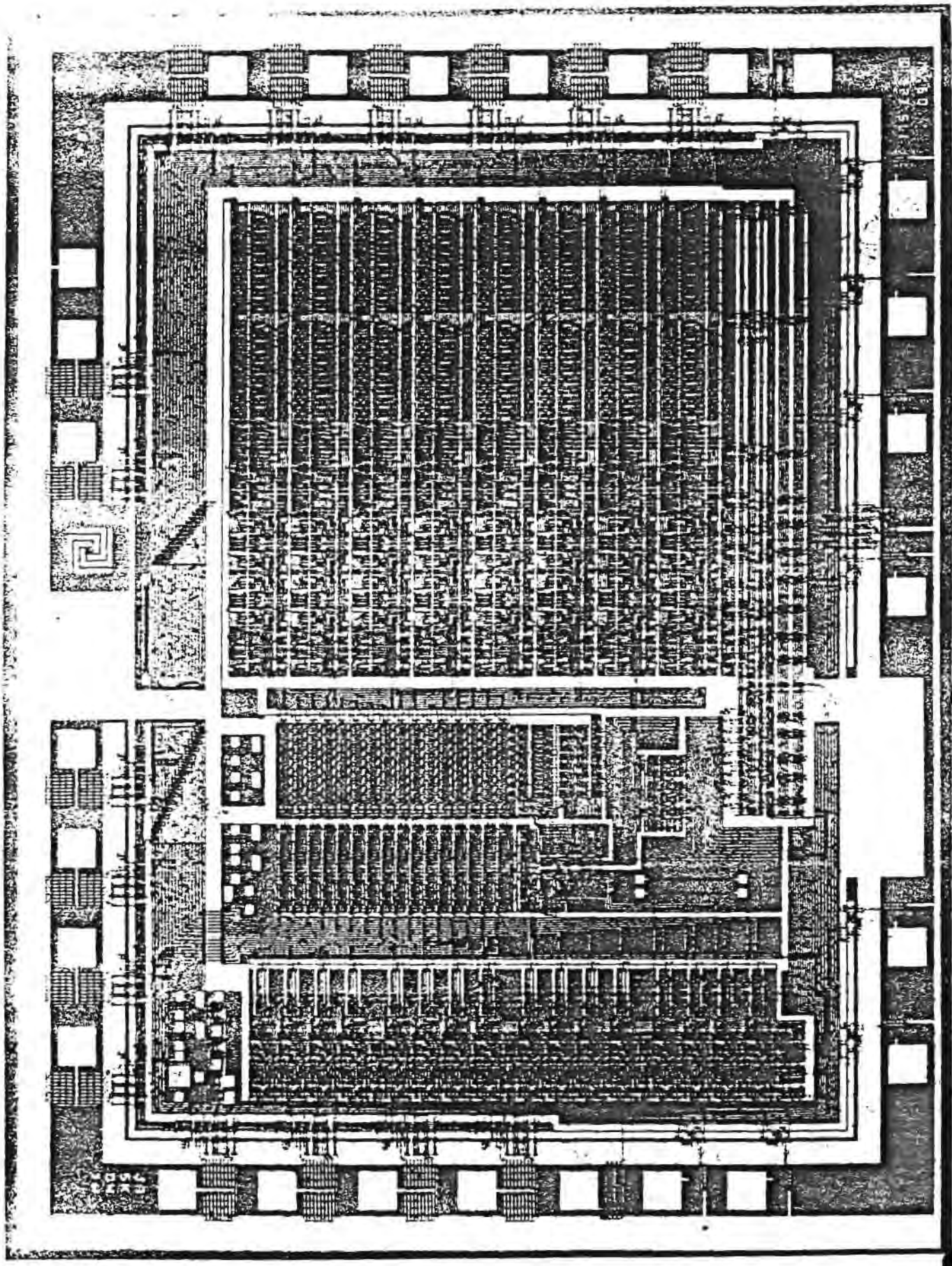

MicroVAX™ 1

Digital Equipment Corp.

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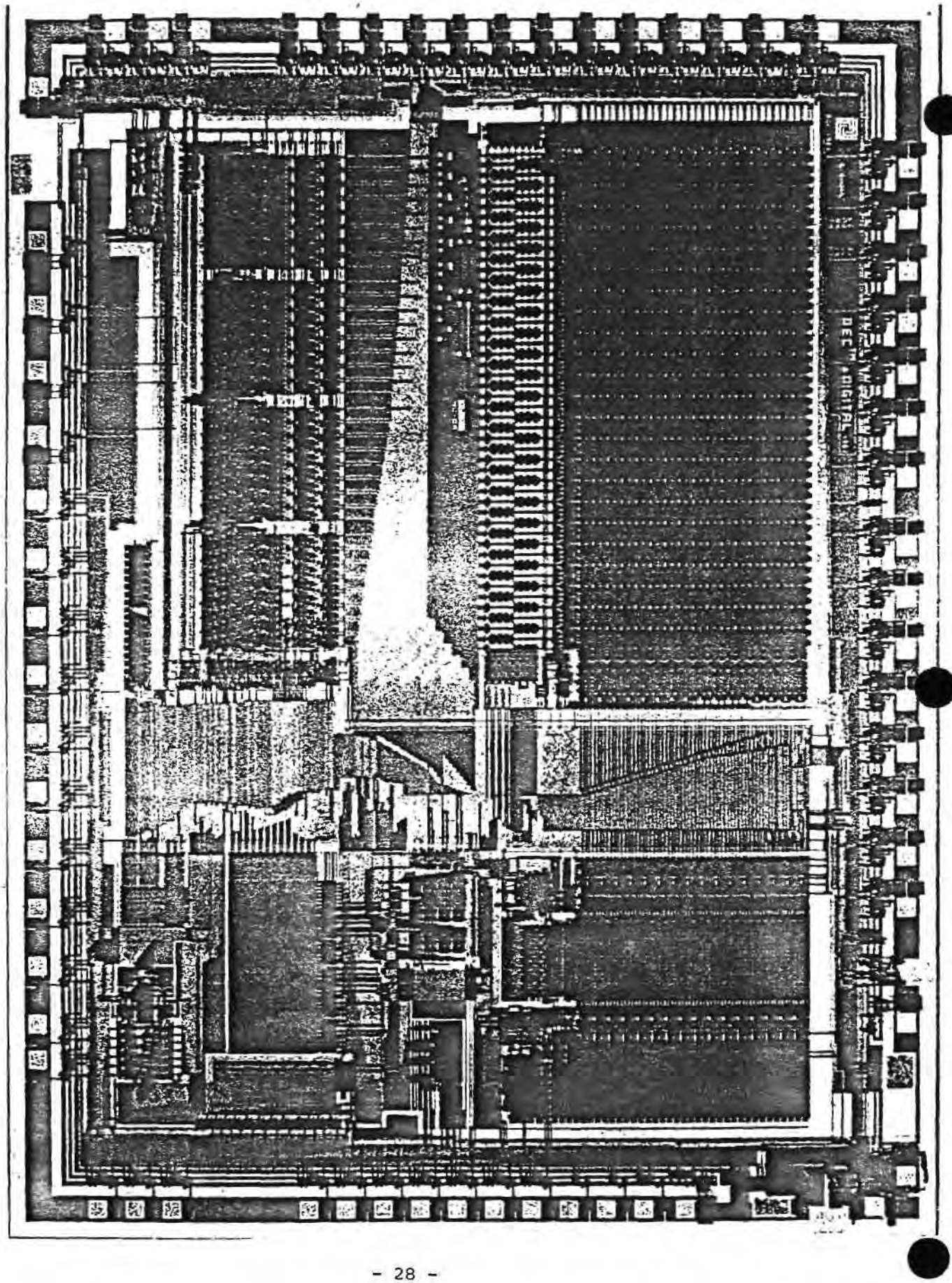

Silicon Compilers Inc.

INTEGRATED SYSTEMS TECHNOLOGY

**Allowing systems designers
rapid and efficient development
of electronic end products.**

Nielsen Dataquest

EDA FOR PRINTED CIRCUIT BOARDS

Buck Feltman
Vice President of Marketing
Cadnetix Corporation

Mr. Feltman is Vice President of Marketing at Cadnetix Corporation. Previously, he spent 17 years at Texas Instruments in Sales and Marketing and Systems Engineering, where his most recent position was Division Manager of Gate Array, Standard Cells, and Customized Cells. His earlier experience at Texas Instruments included a position as head of the New Business Development Center for Market Operations. In this capacity, he planned and implemented a program that resulted in placement of 12 world-wide Regional Technology Centers for Texas Instruments. Mr. Feltman received a B.S. degree in Electrical Engineering from Auburn University in Alabama, and an M.B.A. degree from Rollins College in Winter Park, Florida.

Dataquest Incorporated
ELECTRONIC DESIGN AUTOMATION FOCUS CONFERENCE
May 10-11, 1984
Sunnyvale, California

EDA for Printed Circuit Boards

Presented at Dataquest Focus Conference
May 10-11, 1984

Buck Feltman
Vice President - Marketing
Cadnetix Corporation

Although the electronic design automation (EDA) market has been in existence since the early 1970's, the market has entered a new, high-growth phase. While the Dataquest definition of EDA includes both integrated circuit (IC) and printed circuit board (PCB) engineering applications, the primary application of EDA equipment is IC development. The market for EDA workstations and has grown from nothing to $86 million in only three years. This exceptional rate of growth has tended to overshadow the market for workstations in printed circuit board applications, which grew at a 100% annual rate over the same period to $80 million in 1983. Figure 1 shows the Dataquest projections as they have segmented the market. Although the projections recognize differences between PCB CAD and IC CAD, the segments are not differentiated in the EDA application, often referred to as CAE.

A different segmentation of the market for electronic design automation equipment is shown in Figure 2, which also lists the more critical tasks associated with each application. The lists for printed circuit boards are very similar to the ones for integrated circuits, but the differences in equivalent items are not apparent. For instance, fault simulation is vastly different in the two situations as fault modes are entirely different. Likewise, simulation and timing analysis, placement, routing, and design rule checking have entirely different meanings for PC boards and integrated circuits. There are many differences in the two applications of EDA, and it is useful to examine each application segment, as the organizational benefits of electronic design automation must comprehend the entire design process.

Electronic Design Automation for Printed Circuit Boards

Printed circuit board EDA tends to be perceived as a drafting tool and many view it as old technology. In reality, the problems associated with printed circuit board design are complex and are not solved adequately by the systems available today.

The length of time required to complete a design from the initial concept is one the most critical problems facing electronic equipment manufacturers today. Complex systems may require years to complete. Both simple and complex systems may miss market windows if design and development takes longer than

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ELECTRONIC CAD MARKET FORECAST

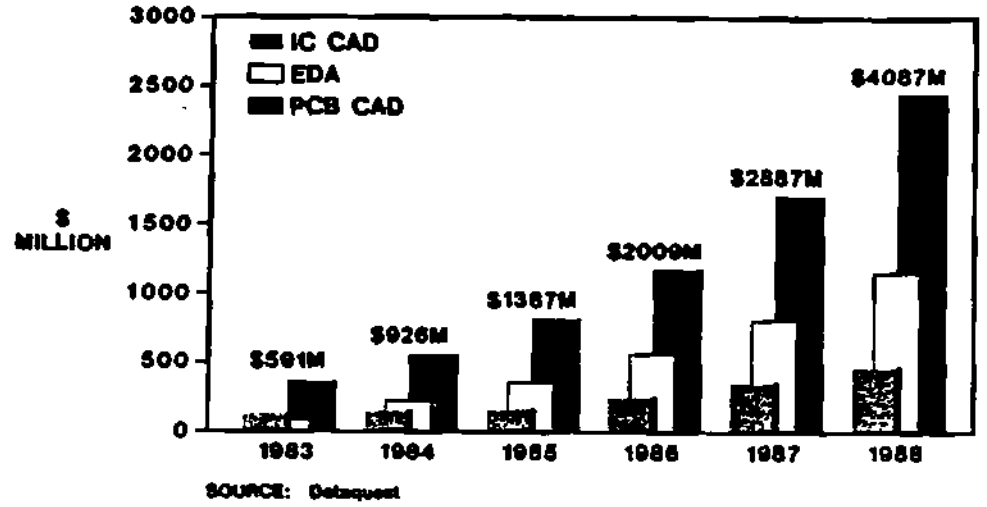

Figure 1. EDA Market Projections.

	DESIGN ENGINEERING (EDA)	PHYSICAL LAYOUT (CAD)
PRINTED CIRCUIT BOARDS	Schematic Entry Simulation & Timing Analysis Fault Simulation/ Test Design	Autolayout Design Rule Checking
INTEGRATED CIRCUITS	Schematic Entry Simulation & Timing Analysis Fault Simylation/ Test Design	Auto-layout Design Rule Checking Model Extraction

Figure 2. Electronic Design Automation Market Segmentation

planned. It is difficult to isolate any specific task in the design process as the cause of all or most of the problems, rather, the design process should be examined for tasks which may be automated or streamlined. One of the more common problems, and one which spans the entire design process, is documentation.

The maintenance of accurate records is a major problem which can be automated and, as a result, streamlines the design process. Figure 3 depicts a generic design process and lists the documentation products of each step. The process usually starts with a loosely described concept, which is modified as the design progresses, causing design changes at all points in the process. The specification and functional design are often not well documented, and changes, regardless of the source, must be recycled through all design documents, requiring endless re-drawing. Automated drafting of new documents saves some initial labor, but the real saving comes when changes are required. The draftsman makes only the change and does not have to re-draw the document. In many organizations, documents are not re-drawn every time a change is made, rather, changes are accumulated for a period, resulting in inconsistent records being used by designers and others involved in design.

Automatic PCB design systems also can significantly impact the time required for building breadboards and for developing PCB artwork. The physical layout of a breadboard may be performed on a CAD system for automatic wire-wrapping, eliminating a cumbersome manual task. Physical layout of a simple PC board may be reduced from the four to eight weeks required for manually developing artwork using mylar and tape, to a week or less to perform the same task on a CAD system which produces photoplot artwork on film.

Design verification is another area where design cycle time may be improved. This problem has two parts, the easier one involving the consistency between the engineer's schematic and the resulting layout. Automatic PCB design systems can compare the schematic to the layout for consistency, but in most operations, the layout draftsman also enters the schematic. The solution is to provide the design engineer with an entry device so that he develops the schematic and keeps it up to date. This has not been practical in the past due to the cost and low functionality of available equipment.

Several companies offer low-cost products based upon personal computers, but none of them provide a complete solution. The primary criticism relates to their limited processing power, prohibiting reasonable implementations of functions such as simulation, timing analysis or PCB layout. It is feasible to use personal computer-based systems for front-end schematic entry devices, interfacing to other systems for the complex functions, but this configuration creates a problem. The need for back-annotation of changes made during the layout process requires close coupling between the systems, which is an

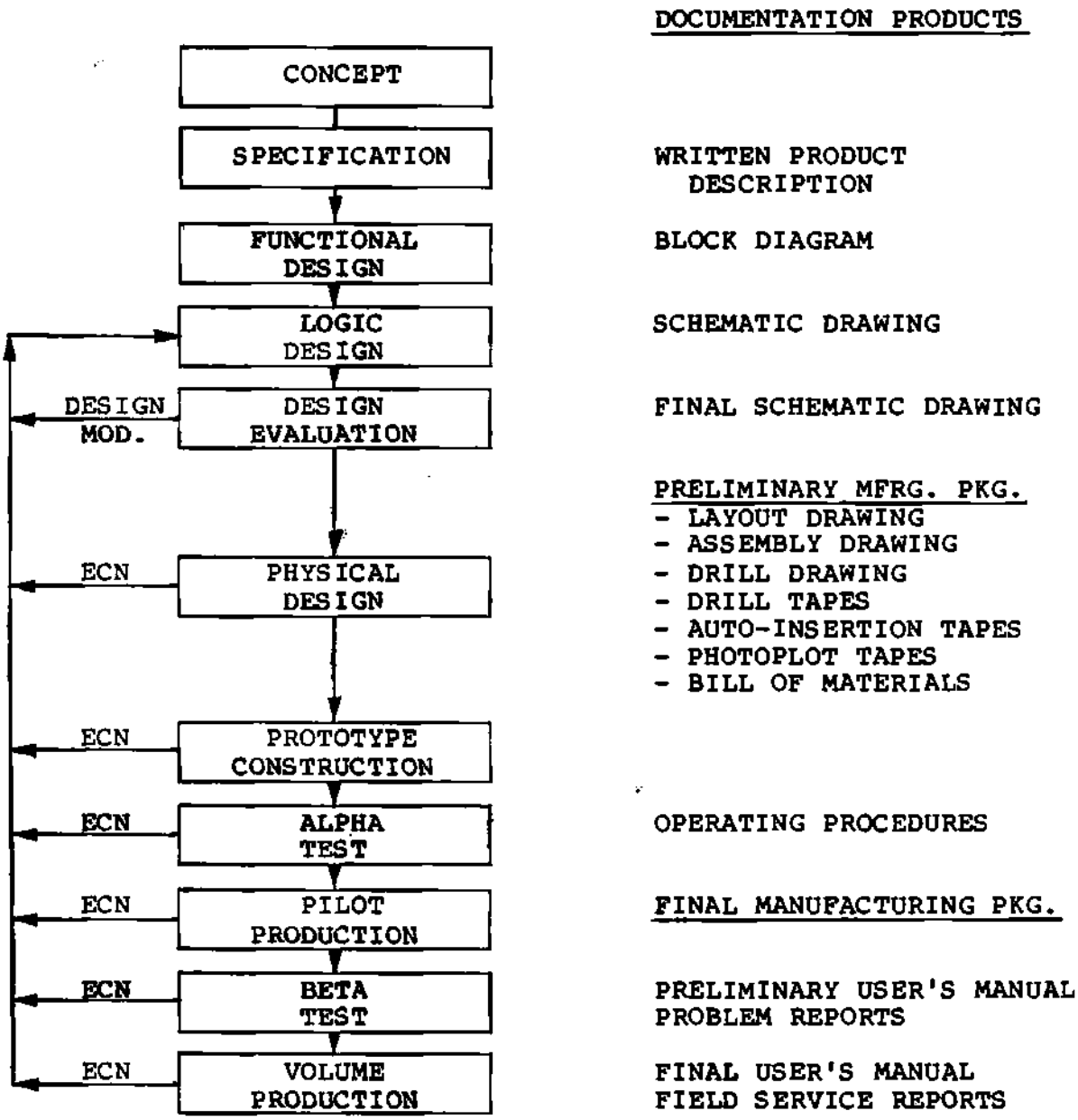

Figure 3. The Electronic Hardware Design Process

impracticality for competing vendors. The more efficient approach is to offer a low-cost terminal integrated with the full-function CAD system.

The more difficult task in design verification involves engineering design and development. The task today is performed by building breadboards and using a logic analyzer to test the circuit. It is certainly feasible to use computer simulation to model the circuit and perform the same tests, and integrated circuit design relies very heavily upon computers for design verification, due to the high expense of fabricating prototypes. Breadboarding has been the lower cost alternative for printed circuit board design and, consequently, computer simulation has not been widely accepted for this purpose. The situation is changing, however, as new circuit technologies are raising the cost of breadboarding for design verification.

Several trends in equipment design are changing the nature of printed circuit board design and the required design tools. Semicustom VLSI circuits, which are rapidly growing in use, obviously must be incorporated into PC board systems, but have relatively long design cycle times. The semicustom IC must be designed concurrently with the PC board, otherwise, significant delays may be incurred. The breadboarding approach to design and test ensures that design will be dependent upon IC availability, and will be delayed until functioning prototypes can be designed and fabricated. The use of computer simulation eliminates this dependence and allows design and test of both the PCB and semicustom IC to proceed concurrently.

The use of semicustom VLSI circuits also introduces some new problems into the design task, causing the transition from EDA to CAD to become fuzzy and the engineer's role to increase. Due to the complexity of VLSI, large, high pin-count packages must frequently be used. Pin-grid arrays, chip carriers and small-outline IC's address this need but require the use of multilayer PC boards and fine-line geometries for PC board signal traces. This, in turn, introduces problems of cross-talk and interference between signals, which requires engineering interaction in the layout process. The packages required for VLSI also tend to dissipate large amounts of heat relative to their surface area, causing thermal problems when several VLSI devices are used. Again, engineering expertise is required to solve a layout-related problem.

Many electronic systems also tend to use large board sizes and/or dense component placement. Both raise the complexity of PC board design to the extent that manual artwork development is no longer practical. Automation of the layout process is required to perform the task within any reasonable period of time.

Printed Circuit Board Design Automation Solutions

An obvious solution to the design documentation problem is the integrated system, which provides the necessary capabilities at each step in the process, from specification to manufacturing. Each technical discipline involved in the process has unique requirements of hardware and software which must all be tightly linked into a cohesive, comprehensive system. The system designer needs block diagram drafting capability, functional-level simulation and text processing. The circuit designer requires the same capabilities in addition to logic simulation, timing analysis and fault simulation. The PCB layout draftsman needs automatic placement, automatic routing and design rule checking. The manufacturing operation requires assembly drawings, drill drawings, NC drill tapes, auto-insertion tapes, photoplot tapes, bill of materials and automatic test files.

In terms of hardware, the engineer's need may be satisfied with a high-resolution, black & white CRT and the substantial processing power required for simulations. Layout draftsmen need a high-resolution color display with significant processing power for automatic operations. Both disciplines require relatively large amounts of mass storage capability and, for efficient communications, a local area network link to all workstations. Peripheral devices are also required by all workstation users for archiving purposes and hardcopy output. A local area network should provide the capability for all users to share the same peripherals, reducing the average system cost per user.

An additional benefit of stand-alone workstations used with networking relates to the cost of implementing a complete design automation system. It is wise to convert a layout drafting department gradually, to minimize inconvenience and risk. Full-function workstations may be added at any time, requiring capital investment only for the additional system. Host-dependent systems, in contrast, require the significant investment in a host computer before the first workstation may be used. Additional workstations do not add any processing power, and consequently, degrade system performance as they are added to the host. Further, when the host is inoperative, all workstations become inoperative. Stand-alone systems have full capability without the host so that additional workstations have no effect upon performance, and the loss of one system, or even the network communications link, has no effect upon other workstations.

The networking concept also raises an interesting possibility for the processing power requirements of simulation and automatic layout. Special processing engines may be developed, which provide dedicated hardware, optimized for each specific task, at a cost far lower than general purpose hardware. The network allows access to all users, again keeping the average system cost low while providing extremely high performance for every user.

The Cadnetix Approach

Cadnetix Corporation currently offers the CDX-5000 Automatic CAD Workstation and the CDX-5001 Interactive CAD Workstation for the physical design of printed circuit boards. Both systems provide 32-bit performance with high-resolution graphics display. The user interface is object-oriented and has seven action keys with three keys on an optical mouse to provide 80% of the required functions. Keystrokes are minimized and learning is made easier by keeping all system operations consistent. The CDX-5000 provides automatic signal trace routing and both systems generate complete manufacturing data.

Next week, the Ethernet local area network and a dedicated file server will be announced, which provide communications and file sharing between workstations, peripheral device sharing and additional mass storage. This summer, an EDA workstation will be introduced, providing a tightly-coupled schematic entry and engineering analysis tool for printed circuit board design. This new product will complement the present CAD products to provide a complete front-to-back solution for printed circuit board design and development.

Conclusion

While the functions and operating sequences required to support EDA for integrated circuit applications are very similar to those for printed circuit board applications, there are significant differences. Technical differences and the available alternatives may be distilled to comparisons of functional value. The value of schematic entry is high for both IC and PC applications due to the benefits of automating documentation management. Simulation and timing analysis have high value to IC development, but only moderate value to PC development, due to the relative cost of available alternatives. Likewise, fault simulation and test program development have high value in IC design, but low value in PCB design.

In summary, EDA has a lower functional value for PCB design and is therefore more price sensitive than EDA for IC design. This requires low-cost engineering workstations to meet cost requirements and tight coupling between EDA and CAD to maximize system functionality. No vendor presently offers a system addressing both the EDA and CAD problems for PC board development, but Cadnetix intends to be the first with product announcements scheduled for the next three months.

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THE WORLD ACCORDING TO VENTURE CAPITAL

A. Grant Heidrich
General Partner
Mayfield Fund

Mr. Heidrich is a General Partner at Mayfield Fund, which is collectively involved in the management of nearly $200 million of venture capital. Mr. Heidrich has worked closely with early stage funding of computer and health care companies. He represents Mayfield Fund on Silicon Graphics' Board of Directors. Prior to joining Mayfield, Mr. Heidrich was a Vice President of Wood River Capital Corporation, a New York-based venture capital fund. Mr. Heidrich received an undergraduate degree in Human Biology from Stanford University and an M.B.A. degree from Columbia University.

Dataquest Incorporated
ELECTRONIC DESIGN AUTOMATION FOCUS CONFERENCE
May 10-11, 1984
Sunnyvale, California

What's All The Excitement About
or
How Can An Industry Grow So Fast

Gerard H. Langeler
MENTOR GRAPHICS CORPORATION
8500 S.W. Creekside Place
Beaverton, Oregon 97005-7191
(503) 626-7000

The market for Computer Aided Engineering products didn't exist in 1981, yet many industry observers predict a market size of over $1 billion by 1987! How can an industry grow so fast?

To answer this question we need to look at what is fueling the growth, and just as importantly the limits to growth. By focusing our attention on the limits to growth, we can determine whether all this euphoria is realistic or whether this market is just a high technology flash in the pan.

The limits to growth for any industry or company are a direct function of both internal and external elements. Internal limits center on such things as cash position, manufacturing capacity, market coverage, management ability and something the Boston Consulting Group calls the "Maximum Sustainable Growth Rate" which is approximated by return on net assets minus the interest rate on debt times the debt to equity ratio. External limits are focused on such issues as degree of pent-up demand, economic cycles, capital availability and most importantly the return on net assets a customer can expect from newly acquired CAE systems.

It turns out that in the short term (e.g., next one to two years) the limits to growth for the CAE industry are largely internal, not external! While the significant CAE players are public companies with excellent cash positions, and all have such large capitalizations that return on assets is not yet a meaningful number, the other internal limits are very much in play.

Dramatically lengthening semiconductor lead times put an artificial constraint on manufacturing capacity in the short term. The leading CAE companies have relatively small sales and support organizations (though growing fast) so market coverage limits industry growth at present. Finally, some CAE companies have the management experience and depth to handle over $100 million in sales, growing at over 100% per year. Some will struggle under such pressure.

In contrast, there are few external limits to growth in the short term. There is a large amount of pent up demand, stemming from years of "shoemaker's children" phenomena among electronic engineers. We are in the middle of a strong upturn in the business cycle, led by capital spending.

Over the long term, the more enduring factors of return on investment come into play. Given the very high software content to the vlaue added portion of the business, internal return on net assets is likely to be quite high. Coupled with the traditional aversion to debt by successful high technology firms, the maximum sustaninable growth rate for leading CAE firms is likely to remain quite high.

The real limit to long term growth in this industry will be found in the return on investment customers experience when they purchase a CAE system. Most customers focus on measuring productivity gains to determine the value of their investment. While productivity gains are very important in terms of a shorter time to market serving to lower costs and improve market share, there is a larger mostly unrecognized factor - price flexibility.

If you give me a choice of getting to market three months early, or getting there on time with product innovation able to support a 5% or 10% higher price, I will normally choose the second option. CAE systems which not only promote productivity but also provide tools for innovation allow for such gains.

This kind of thinking can lead to sophisticated analysis which can prove beyond a shadow of a doubt that CAE is a good investment, often yielding 50% to 100% annual return on investment. However, even this may pale in comparison to the real return on CAE-survival. It is the

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impression of many people (not just vendors) that failure to adopt CAE tools will spell economical doom for any firm competing in the fast moving electronics industry. With that attitude the growth potential for leading CAE firms is indeed spectacular.

So, how fast can the industry really grow? Our best estimates are 200%-300% in 1984. 40%-70% per year in the 1985-1990 time frame and at least 25% to 35% per year during the 1990's.

Along the way, you are going to see some interesting changes. First of all, during 1984 and 1985 some of the walking wounded will stop walking. Some will just go away, others will merge or get acquired. For the long term leaders, look to Mentor Graphics, Daisy, one of the instrument companies (probably Hewlett-Packard) and one of the CAD/CAM companies (probably Computervision).

Rapid growth and rapid change, it makes for a most exciting business.

/tp

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DEFINITION

- RISK EQUITY

NEW

GROWING

TROUBLED COMPANIES

MANAGED BY OTHERS

FULL SPECTRUM OF
VENTURE CAPITALISTS

Organization

Size of Funds

Geography

Industry Preferences

Stagers of Investment

C A P I T A L I N F U S I O N S

1983 $4.1 Billion

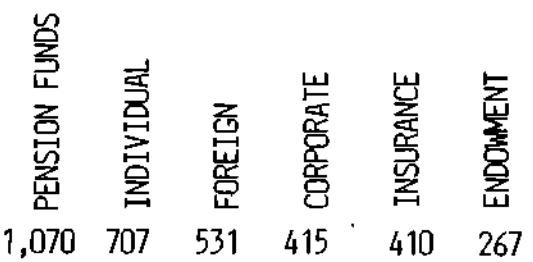
1982

$4.8 Billion

Prior to 1978 $2.6 Billion

$11.5 Billion

SOURCES OF FUNDS - 1983



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To Private Funds

MAYFIELD

- Private Partnership
- $200,000,000
- Western United States
- High Technology
- Early Stage

REPRESENTATIVE INVESTMENTS

Adept Technology, Inc.	Genentech, Inc.
Atari, Inc.	GRiD Systems Corp.
Avantek, Inc.	Linear Technology, Corp.
Businessland, Inc.	LSI Logic Corp.
Cadnetix Corp.	Megatest Corp.
Cadtrak Corp.	Quantum Corp.
Compaq Computer Corp.	Seeq Technology, Inc.
Cypress Semiconductor Corp.	Silicon Graphics, Inc.
Dysan Corp.	Storage Technology Corp.
Equatorial Communications Co.	Tandem Computers, Inc.

INVESTMENT CRITERIA

- Management
- Managment
- Management
- Concept
- Growing Market
- Proprietary Product
- Reasonable Valuation

BUSINESS PLAN REVIEW

- Product Description
- Strategy and Market Overview
- Operations Plan
- Management and Key Personnel
- Financial Projections
- Proposed Financing

H O W L O N G ?

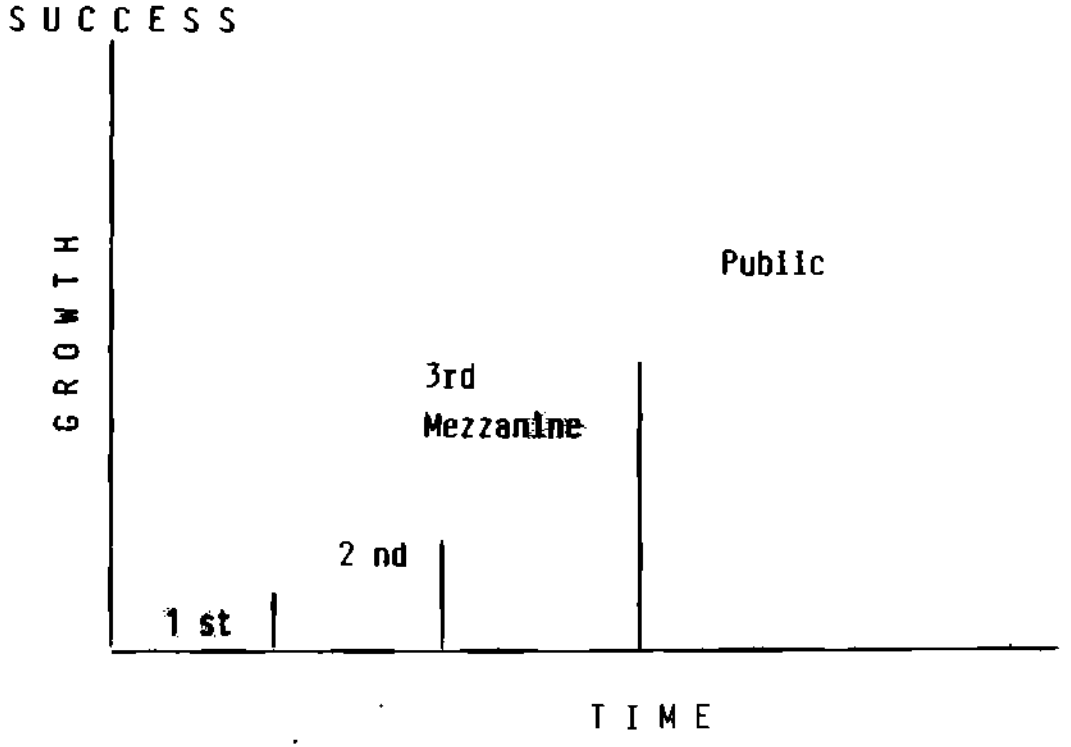
People

Concept

Markets

Technology

Business Plan



T R E N D S

- HIGH LEVELS OF ACTIVITY
- LARGE REQUIREMENTS FOR CAPITAL
- MORE CORPORATE VENTURING
- MORE MERGER ACQUISITIONS
- HIGH TECHNOLOGY INVESTMENT BANKING

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THE EDA INDUSTRY
UNIQUE REQUIREMENTS MANDATE UNIQUE SUPPORT

Thomas O. Binder
Vice President, Marketing and Sales
Silvar-Lisco

Mr. Binder is Vice President, Marketing and Sales, at Silvar-Lisco. He is responsible for the company's field-based customer support resources. Prior to joining Silvar-Lisco, he was with Calma Company. Before joining Calma, Mr. Binder held various field sales and customer support responsibilities with AccuRay Corp., a supplier of computer-based process control systems. Mr. Binder received a degree in Mechanical Engineering from the University of Cincinnati and an M.B.A. degree from Indiana University.

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May 10-11, 1984
Sunnyvale, California

The EDA Industry
Unique Requirements Mandate Unique Support

Thomas O. Binder
Vice President, Marketing and Sales
Silvar-Lisco
Menlo Park, California

I. Traditional Product Support

The products supplied to the electronic industry by Electronic Design Automation (EDA) vendors require similar product support as technology based products which have been supplied to industry for decades. Their support begins with the delivery of quality products, which are the result of both high quality design and development and high quality product testing and production.

The quality product must be properly installed and the support provided to insure a rapid and effective start-up and implementation.

Training support is necessary to assist the user in rapidly becoming productive in utilizing the EDA System and achieving the maximum benefits.

In addition to the initial training support, continuing application consulting is necessary so the initial results can be maintained and so that changing application requirement and personnel turnover can be accommodated without loss of effective product utilization.

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Occasionally the product will have some failures which must be corrected rapidly so as to prevent any significant loss of product utilization. Even worse, failures which are not corrected quickly will result in loss of user confidence in the product and a resulting tendency to reduce reliance on a tool which was originally acquired to improve productivity.

But these are traditional requirements which describe the majority of design and production tools. What about the EDA Industry and its characteristics and requirements? Surely this industry has unique requirements which mandate that unique support capabilities be developed and supplied with the EDA Systems in which you all have an interest.

II. EDA Industry: Unique Requirements

The EDA Industry and the users of EDA tools have many characteristics which make them unique and, thus, cause them to have unique requirements in the areas of product and customer support. The electronics industry has created the need for an EDA System that is truly "state-of-the-art" and this industry is changing faster than any technology in the history of the world. The users of an EDA System comprise a wide variety of manufacturers ranging from relatively small, localized enterprises to huge, multinational companies.

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And while electronic technology is changing rapidly, all other aspects of the electronic industry are changing just as fast.

All of these facets of the EDA user community mandate that the support provided by EDA vendors meet the resulting unique requirements.

III. Unique Support

A. Multiple Hardware Environments

The application addressed by EDA System cover a wide variety of tasks and a wide range in the magnitude of the tasks. Consequently, the overall EDA application must be partitioned into appropriate levels of computational capability.

In addition, you may want to change those functional assignments based on the size of a specific design. For instance, a logic simulation for a relatively small circuit, or cell, may be adequately accomplished on an engineering workstation. However, the same simulation for a larger circuit, say a large scale integrated circuit, would more efficiently be done on a supermini, and a VLSI circuit may well require a mainframe for efficient logic level simulation.

To accommodate this unique requirement, support for your EDA System must be available at each of these levels of computational capability. This requires that the EDA tools can be implemented at each level, on a variety of CPU types, and that full file compatibility and consistent user interface is available at each level.

B. Multiparty Relationships

Many users of an EDA System look to outside resource for the production of the circuits which they design and layout. The EDA System being used must be compatible with the fabrication processes and standard building blocks used by these outside production resources, typically referred to as "foundries".

This compatibility is assured through a multiparty relationship which is supported, and even developed, by the supplier of the EDA System with the user and the foundary.

The continuing support of this relationship by the supplier of the EDA System is necessary to maintain current compatibility with the foundary as the building block designs are characterized, expanded and modified and/or the fabrication processes are enhanced to take advantage of the latest technology advances.

C. Multiple Design Methodologies

Because of the multiplicity of design and implementation methodologies, an EDA System must be able to support a wide range of applications. Since different parts of an entire system will be partitioned into different physical implementations and EDA System must support a full range of physical device designs.This can include printed circuit boards, gate arrays, standard cells, standard integrated circuits, as well as others.

D. Changing Technology

Perhaps the most critical area of support is that necessary to accommodate the rapidly changing technology exhibited by the electronic industry. A supplier of an EDA System must provide the support necessary to allow the user to continually take advantage of the technological changes being experienced in the electronics industry.

As circuits in general become larger and more dense through advances in manufacturing technology, the EDA System must grow to allow design, verification, and automatic layout of the circuit. And as the new technologies impose new functional demands on the EDA System, ongoing enhancements must be provided through product development support to meet these demands.

For example, gate arrays are increasing in size from a few hundred gates up to 10,000 gates and beyond. An aggressive product support program which includes planned enhancements to satisfy there requirements is a critical element in the support program.

Another example would be standard cell technology which has seen the advent of irregular cells, two-layer metal processes, and two-layer metal/one-layer polysilicon processes to improve circuit performance and density. Support of the EDA System used for the standard cell layout must include enhancements which accommodate these technological advances and allow the EDA System to have a long., productive life.

E. Multinational Relationships

The electronic industry is international in scope and is getting more so every day. Large systems companies have established facilities worldwide and need to have consistency of EDA tools throughout these widespread resources. Second-source agreements between merchant integrated circuit vendors have taken on a true multinational flavor with many combinations of U.S., Japanese, and European suppliers in cooperative ventures.

And integrated circuit merchants themselves are addressing the international markets by establishing design centers in other countries.

The EDA System selected to implement these strategies must be implemented in these different geographic areas; and consequently, the EDA System must be supported in their different geographic areas.

Support at the local level, whether it be for installation or training or maintenance is mandatory to achieve the necessary level of system utilization.

An example is a merchant integrated circuit supplier located in California, with a design center in Europe and a design center in the Far East. All three locations require local support for the common EDA Systems used at each site.

IV. Summary

The EDA Industry exhibits certain characteristics which result in a unique set of support requirements. These include:

A. Multiple Hardware Environments
B. Multiparty Relationships
C. Multiple Design Methodologies
D. Changing Technology
E. Multinational Relationships

These unique requirements apply equally well to users of EDA Systems in a wide variety of situations. And the underlying industry characteristics which mandate these unique support requirements will be with us for a long time.

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COPING WITH A CHANGING INDUSTRY AND CHANGING TECHNOLOGIES

Harvey Jones
Senior Vice President of Marketing
Daisy Systems Corporation

Mr. Jones is Senior Vice President of Marketing and a founder of Daisy Systems Corporation. He joined the company in June 1981 as Vice President of Marketing. Previously, Mr. Jones spent seven years at Calma Company, where his last position was Vice President of Business Development. He received a B.S. degree from Georgetown University, and an M.S. degree in Management from Massachusetts Institute of Technology.

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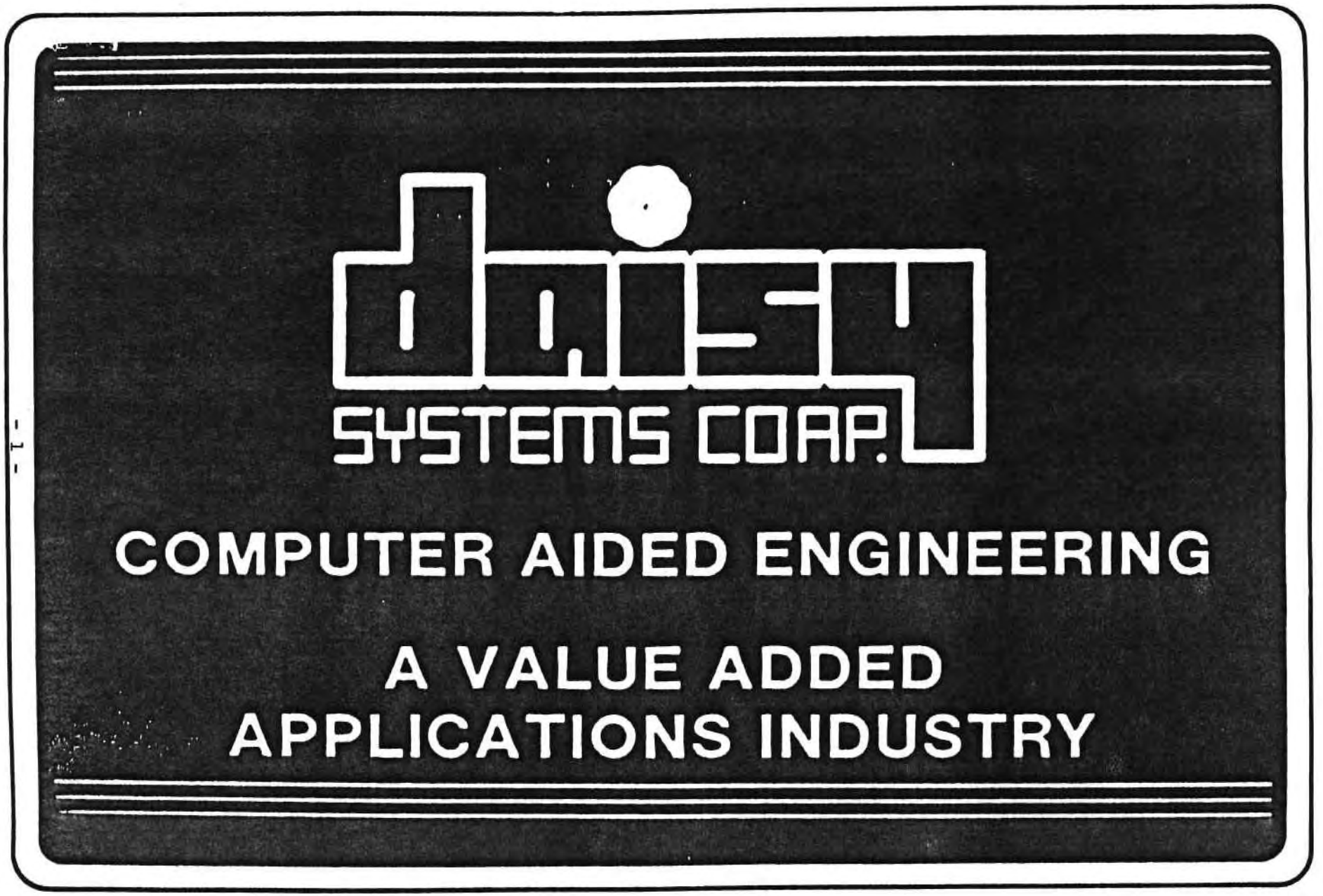

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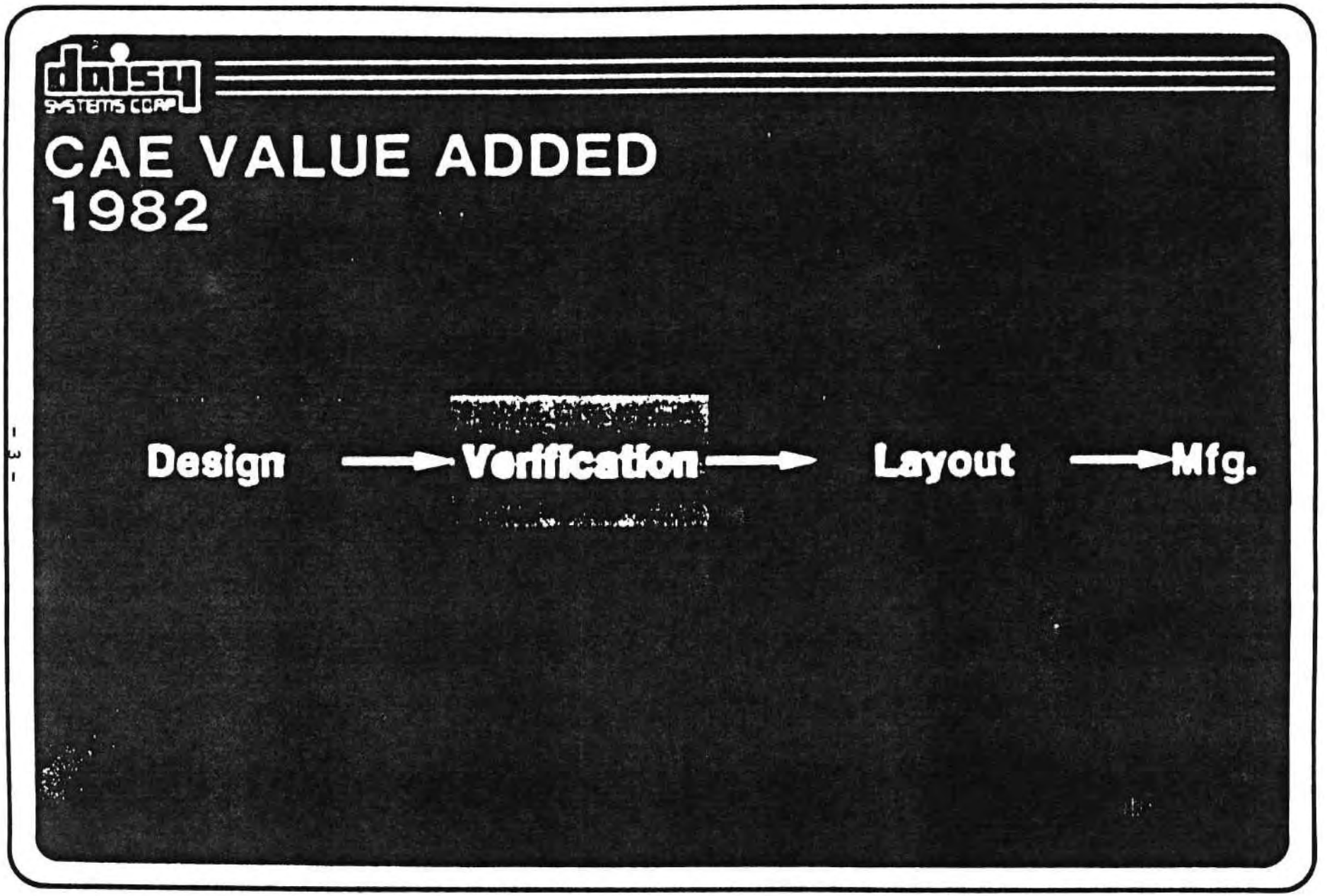
HOW BROAD IS THE MARKET?

- **All Electronics Technologies:**
  Printed Circuits, Gate Arrays,
  Standard Cells, VLSI
- **All Electronics Market Segments:**
  Computers, Communications,
  Military and Aerospace, Consumer ...
- **Worldwide Geographic Distribution:**
  U.S., Europe, Japan



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CAE VALUE ADDED 1983
Design
Verification
Layout

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COMPLETE INTEGRATED SOLUTION

- Schematic Capture
- Documentation
- Report Generation
- Logic Simulation
- Timing Verification
- Circuit Simulation
- Gate Array
- Standard Cell
- Full Custom VLSI

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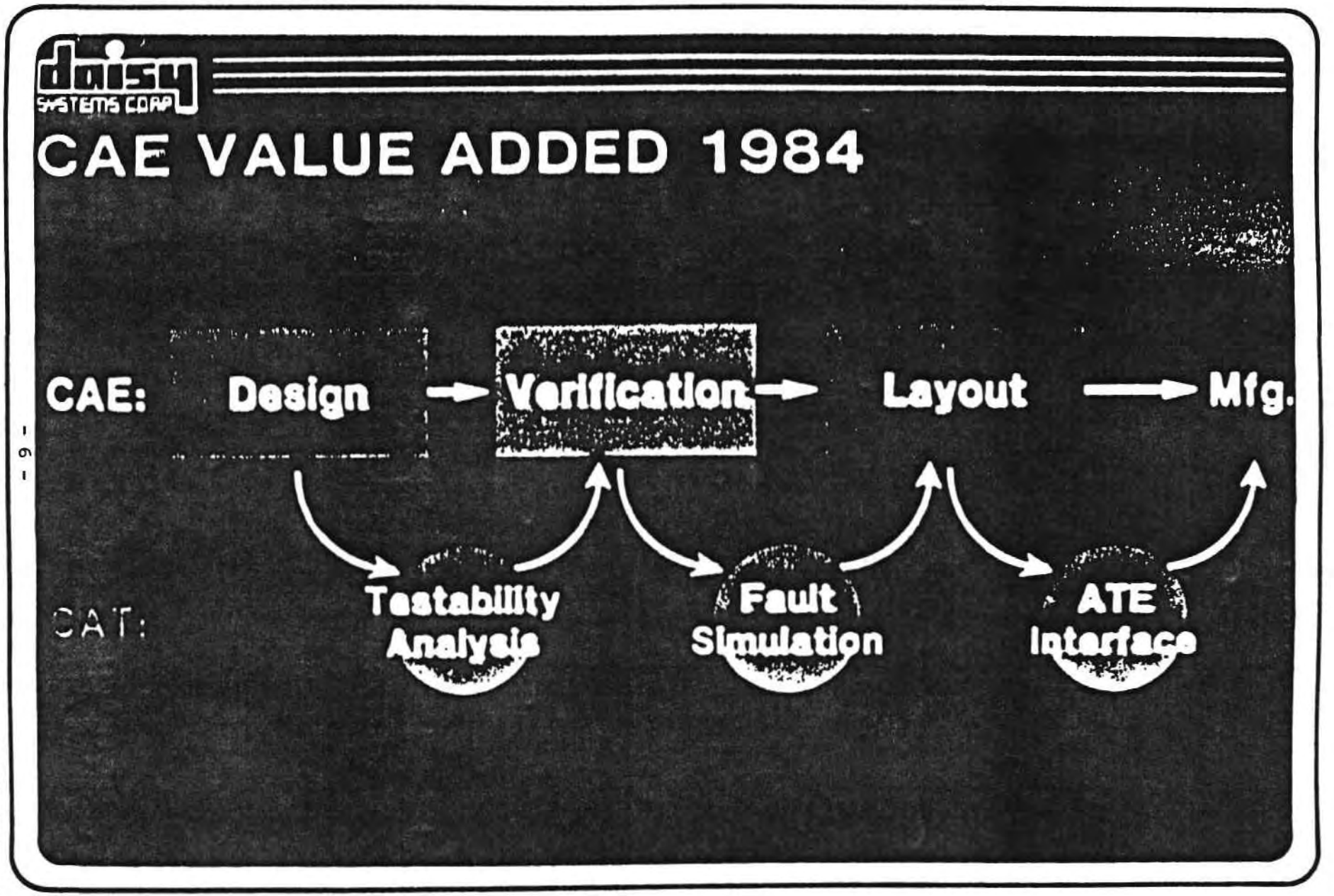

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(Partial List)

- AMCC
- AMI
- CDI
- EXAR
- Fujitsu
- IMP
- LSI Logic
- Motorola
- National
- NCR
- NEC
- RCA
- Siliconix
- TI

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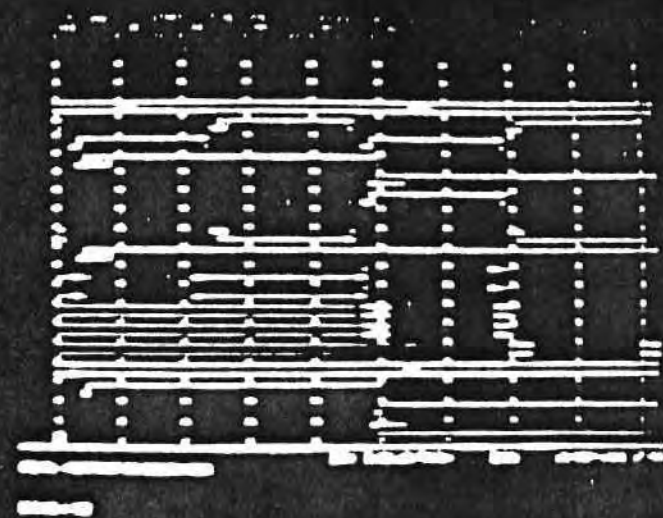
SIMULATION TOOLS

- CAE Driving Force
- The Goal: Total Systems Simulation
- The Demand: Insatiable



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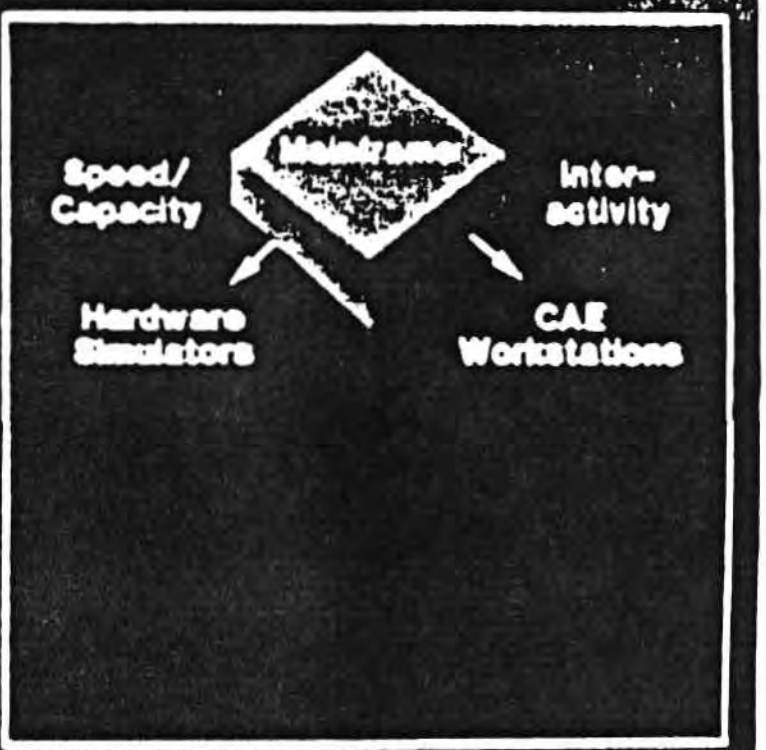
SIMULATION: 2ND GENERATION

- 1981 - Present
- CAE Workstations
  - Highly Interactive
  - Knowledge-Based
- Hardware Simulators
  - Increased Performance
  - Increased Capacity



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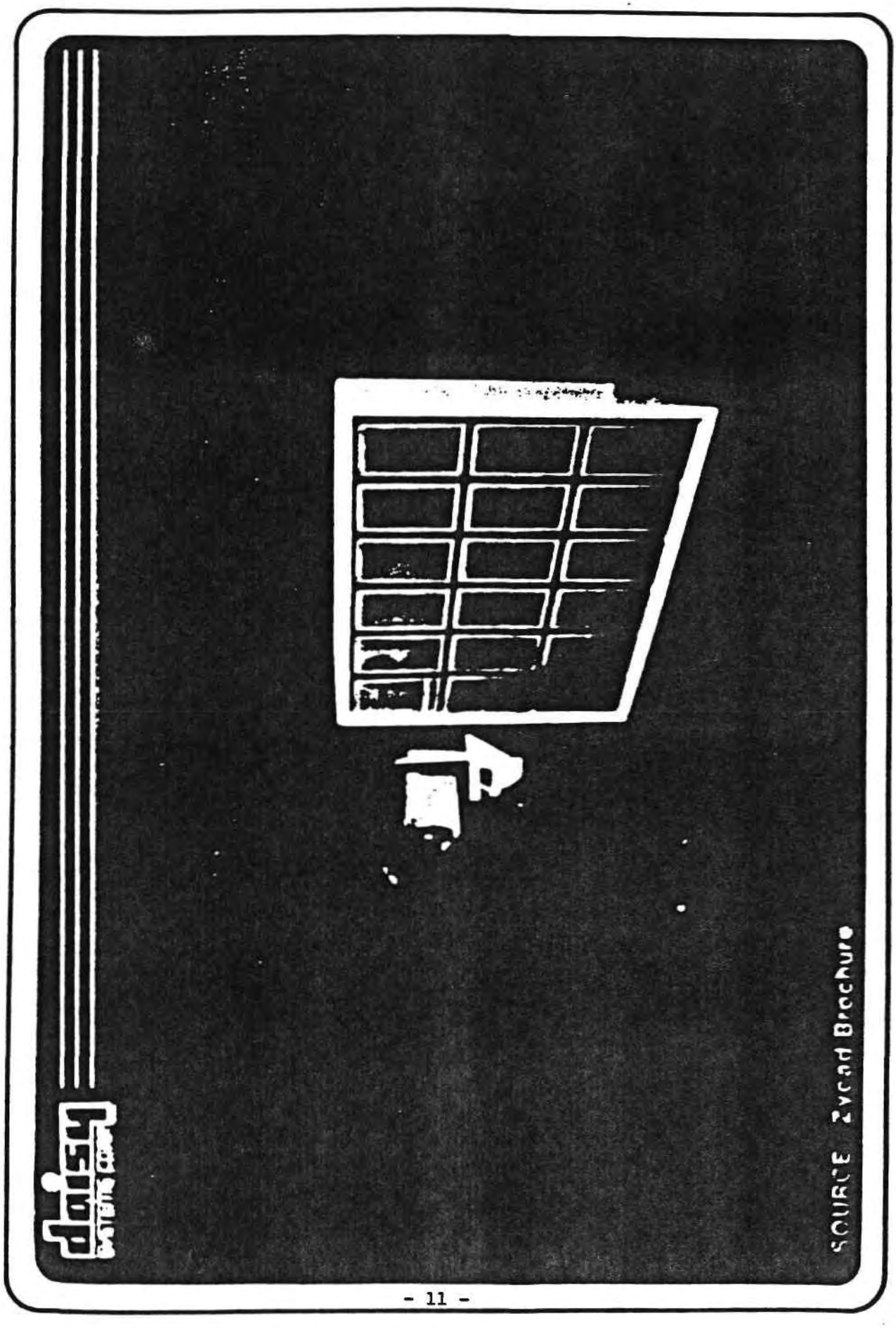
SIMULATION: 1ST GENERATION

- 1970's
- Mainframe-Based
- Batch Execution
- Limited Capacity
- Restricted Performance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SQUIRE 2yead Brochure

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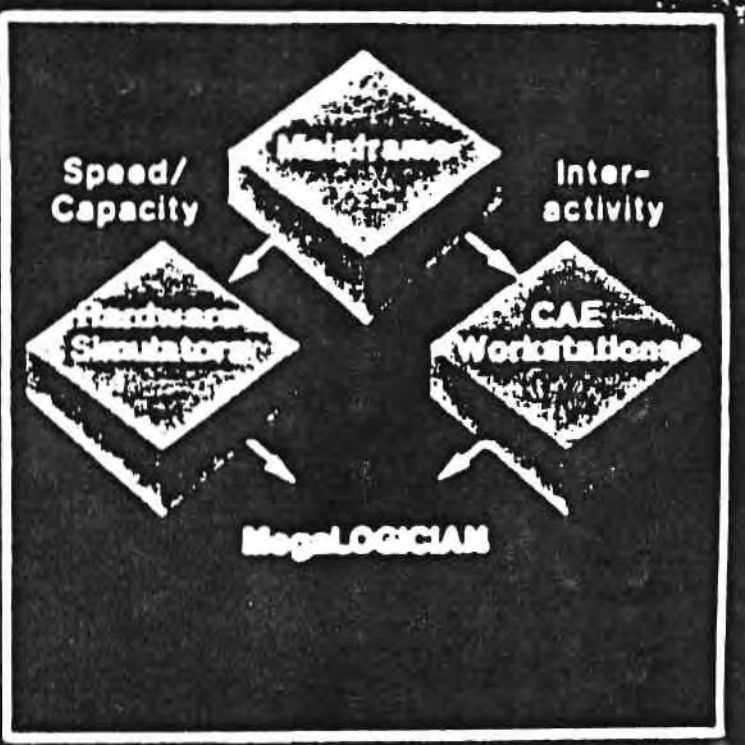
1984: THE STATE OF THE ART

- Workstation Interactivity
- SuperComputer Performance
- 5th Generation Architecture
- Workstation Economics



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MEGALOGICIAN

- 1 Million Gate Capacity
  = 10x State of the Art
- 100K Evaluations per Second
  = 100x State of the Art
- Fully Integrated

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THE NEED:

- SYSTEM LEVEL VERIFICATION

THE PROBLEM:

- SPEED
- CAPACITY
- VLSI MODELS

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COMPLETE INTEGRATED SOLUTION

Design ⟶ Verification ⟶ Layout

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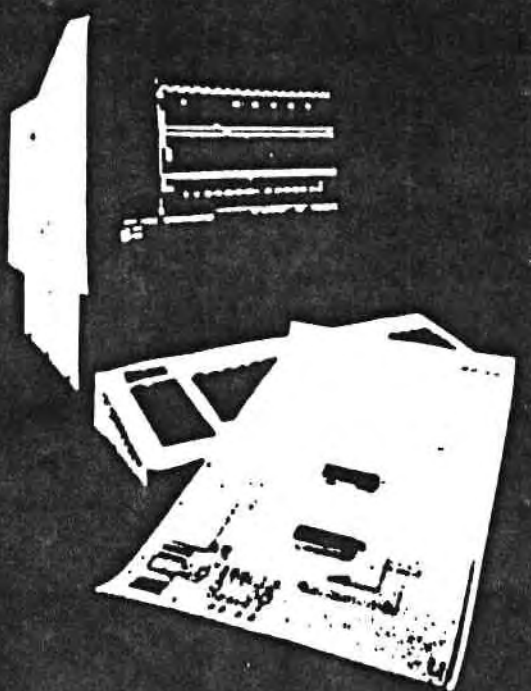
MegaLOGICIAN PMX

SOLUTION FOR VLSI MODELING



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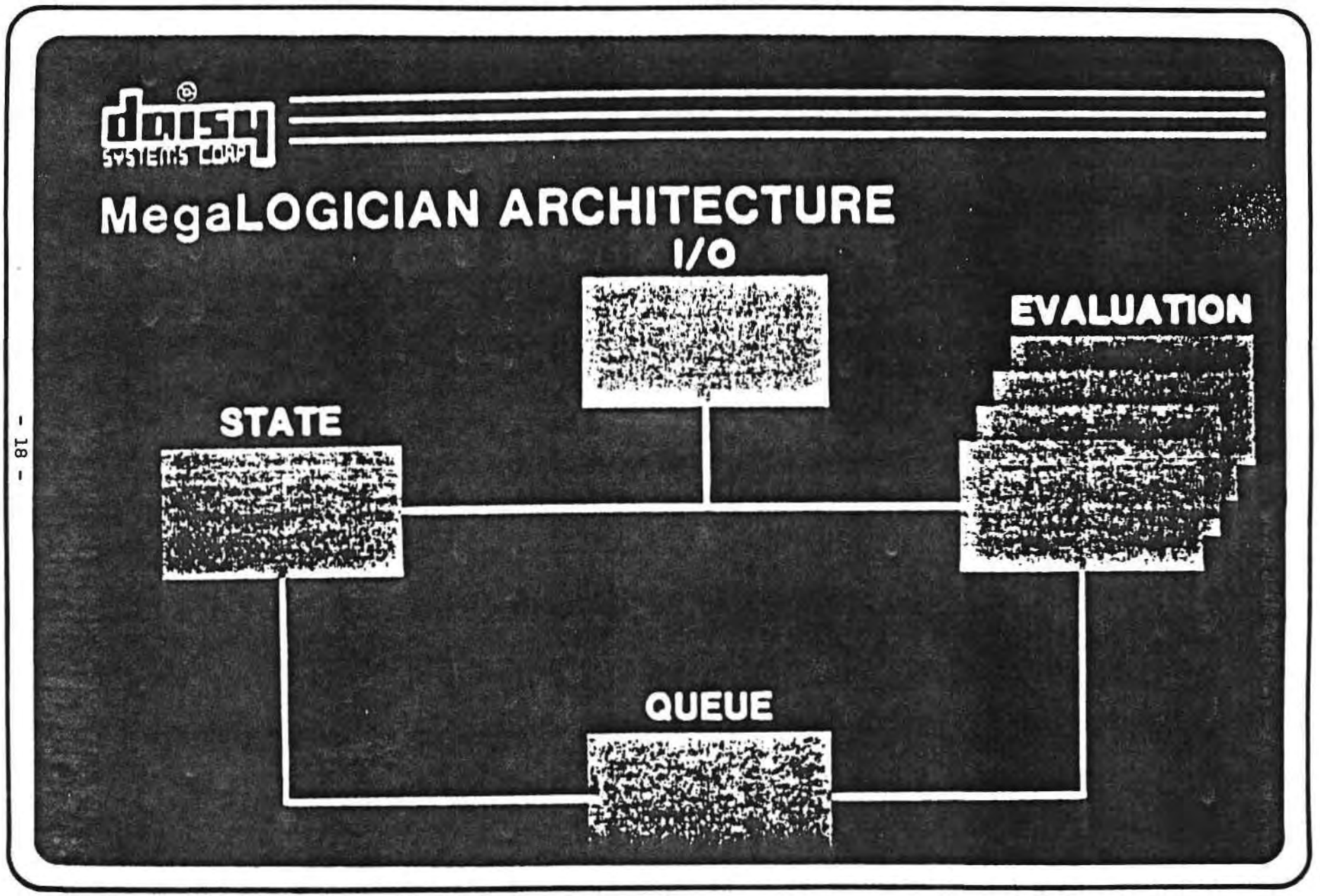
PMX PHYSICALLY MODELS:

- VLSI COMPONENTS (EG. µPROCESSORS)
- GATE ARRAY AND STANDARD CELL COMPONENTS
- PC BOARDS
- SUBSYSTEMS



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PMX BENEFITS:

- COMPLETE SYSTEM VERIFICATION
- FUNCTIONAL, INTERACTIVE TESTER

RESULT:

- NO NEED FOR PROTOTYPE, (RIGHT THE FIRST TIME)

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STRATEGIC CAE CONSIDERATIONS

- Functionality
- Price/Performance
- Service and Support
- Product Migration

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SYSTEMS CORP.
ENGINEERING ENVIRONMENT
Application Specific Design Systems
Gate Array
VLSI
Silicon Vendor Networking
MegaLOGICIAN
ETHERNET™ LAN
Low Cost Design Systems

FUNCTIONALITY

- From Design Entry to Implementation
- Simulation of Entire Systems
- Design for Test

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PRICE/ PERFORMANCE

- Design Station for Every Engineer
- Reduced Station Cost
- Without Sacrificing Performance

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SERVICE AND SUPPORT

- Reliable Products
- Strong Applications Staff (20% of Company)
- Formalized Customer Feedback

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- Strong Applications Staff (20% of Company)
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PRODUCT MIGRATION

- 8086→80286
- Application Accelerators
- Standard Operating Systems

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EDA INDUSTRY OVERVIEW

Beth W. Tucker
Industry Research Manager
CAD/CAM Industry Service
Dataquest Incorporated

Ms. Tucker is Industry Research Manager for DATAQUEST's CAD/CAM Industry Service. In this position, she is responsible for analyzing and reporting on the electronics segment of the CAD/CAM industry. Prior to joining DATAQUEST, Ms. Tucker was Market Planning Manager of Calma Company's Microelectronics Division, where she was responsible for identifying market opportunities and developing marketing strategies for the company's electronic CAD product line. She later contributed to the development of marketing information systems at Calma's corporate level. Prior to that, she was a Senior Market Research Analyst with Monroe Systems for Business, where she was responsible for market research and development of small business computer products. Ms. Tucker holds an A.A. degree in Computer Technology from Morris County College in New Jersey and is doing course work in Business Administration at San Jose State University.

Dataquest Incorporated
ELECTRONIC DESIGN AUTOMATION FOCUS CONFERENCE
May 10-11, 1984
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