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Jean A. Hoerni

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PATENT NOTEBOOKS

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ur patent notebook should contain a complete description and record of:

1. Any activity in connection with the conception and building and testing o an idea which may be patentable;
2. The dates on which such idea was conceived and built and tested;
3. Subsequent activity relating to construction, testing or demonstrating th idea, or of any improvements, changes or new uses;
4. References to persons who assisted or who are familiar with the idea or a phases of its subsequent development;
5. Cross-references to any other test data, technical reports, data files or other written material relating to the idea or its subsequent development and testing.

ENTRY PROCEDURE

ur patent notebook should serve to provide a continuous chronological record ur activities of the nature described above. It must also be in such form th can be used as evidence in a legal proceeding. To these ends the following ocedure should be carefully followed:

1. Form of Entry
   a. Make all entries legibly, neatly and in ink. (Do not use pencil and do not use your notebook as a "scratch pad.")
   b. Date all entries at the beginning. (Write dates out completely.)
   c. Sign name in full and again date entry at its conclusion.
   d. Do not leave extensive blank spaces. Begin all entries on the line following the last line of the preceding entry. If there are unusual long gaps in time between successive entries (e.g. due to illness or vacation), a record of the facts should be made.
   e. Graphs, photographs, sketches, etc. on separate sheets can be securel cemented or stapled over a blank section of a page in the notebook. Each such inserted sheet should also be separately signed, dated and witnessed.
   f. Do not erase or modify entries once made. If modifications are required, make a new entry.

2. Witnessing
   a. Each entry should be witnessed by two competent persons who have read the entry and are technically qualified to understand it. Each witne must sign his name in full. (Note: A joint inventor cannot serve as a witness for a co-inventor.)
   b. If the entry is one recording actual tests or demonstrations, the witness must also witness such and check all connections, structure, etc. of the equipment. He should then state over his signature that he act ally witnessed such tests and checked such connections, etc.

GENERAL

1. Do not include statements implying lack of interest, abandonment or unimportance of the idea.
2. Keep notebooks in safe place. This notebook is charged to you and you ar responsible for its safekeeping. When the notebook is filled or if you leave the division which issued it, it must be returned to your division

November 7, 1957

Calculation of surface concentration, using sheet resistivity and junction depth

Sheet resistivity $\rho_s = 4{,}53 \frac{V}{I}$ ← from 4 point probes

$$\sigma_s = \frac{1}{4{,}53}\frac{I}{V} = \int_0^{x_j} q\mu C\, dx$$

Case of gaussian distribution

$$C(x,t) = \frac{Q}{\sqrt{\pi Dt}} e^{-\frac{x^2}{4Dt}}$$

$$\frac{1}{4{,}53}\frac{I}{V} = q\frac{Q}{\sqrt{\pi Dt}}\int_0^{x_j} e^{-\frac{x^2}{4Dt}}\mu\left(\frac{Q}{\sqrt{\pi Dt}}e^{-\frac{x^2}{4Dt}}\right)dx = q\frac{2}{\sqrt{\pi}}Q\int_0^{y_j} e^{-y^2}\mu\left(\frac{Q}{\sqrt{\pi Dt}}e^{-y^2}\right)dy \qquad y=\frac{x}{2\sqrt{Dt}}$$

We express $\sqrt{Dt}$ in terms of x_j, the junction depth with a bulk concentration C_B. Let C_s be $C(0,t) = \frac{Q}{\sqrt{\pi Dt}}$

$$C(x,t) = C_s(t)\, e^{-x^2/4Dt} \qquad \frac{C_s}{C_B} = e^{x_j^2/4Dt}$$

$$x_j = 2\sqrt{Dt}\sqrt{\ln\frac{C_s}{C_B}}$$

$$\frac{I}{Vx_j} = \frac{4{,}53\, q C_s}{\sqrt{\ln\frac{C_s}{C_B}}}\int_0^{y_j} e^{-y^2}\mu\left(C_s e^{-y^2}\right)dy = f(C_s, C_B) \qquad (1)$$

2) Case of erfc distribution

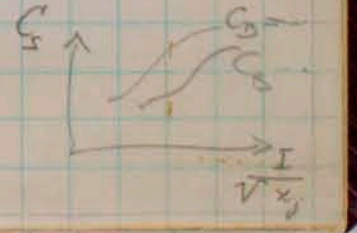
$$C(x,t) = C_0 \operatorname{erfc}\frac{x}{2\sqrt{Dt}}$$

$$\frac{1}{4{,}53}\frac{I}{V} = qC_0\int_0^{x_j}\operatorname{erfc}\frac{x}{2\sqrt{Dt}}\mu\left(C_0\operatorname{erfc}\frac{x}{2\sqrt{Dt}}\right)dx = 2\sqrt{Dt}\,qC_0\int_0^{y_j}\operatorname{erfc} y\, dy\,\mu(C_0\operatorname{erfc} y) \qquad y_j = \frac{x_j}{2\sqrt{Dt}}$$

$C_s = C_0$ ⇒ $C(x,t) = C_s \operatorname{erfc}\frac{x}{2\sqrt{Dt}}$; $C_B = C_s\operatorname{erfc}\frac{x_j}{2\sqrt{Dt}}$; $\frac{x_j}{2\sqrt{Dt}} = \operatorname{erfc}^{-1}\frac{C_B}{C_s}$; $\sqrt{Dt} = \frac{x_j}{2\operatorname{erfc}^{-1}}$

$$\frac{I}{Vx_j} = \frac{4{,}53\, qC_s}{\operatorname{erfc}^{-1}\frac{C_B}{C_s}}\int_0^{y_j}\operatorname{erfc} y\,\mu(C_s\operatorname{erfc} y)\,dy = g(C_s, C_B)$$

$$\frac{I}{Vx_j} = 4{,}53\cdot 1{,}6\cdot 10^{-19}\frac{C_s}{y_j}\int_0^{y_j}(\operatorname{erfc} y)\mu(C_s\operatorname{erfc} y)\,dy$$



November 13, 57

Eq. (2) has been integrated numerically

$$\frac{I}{V x_j} = 7{,}25 \cdot 10^{-19} \frac{C_s}{\sqrt{\ln \frac{C_s}{C_B}}} \int_0^{y_j} e^{-y^2} \mu(C_s e^{-y^2})\, dy \quad ;$$

y	e^{-y^2}	C_s/C_B	$\sqrt{\ln \frac{C_s}{C_B}}$
0	1	10	1,516
0,5	0,777	10^2	2,145
1	0,368	10^3	2,625
1,5	0,106	10^4	3,03
2	0,0183	10^5	3,39
2,5	0,00193	10^6	3,715
3	$1{,}234 \cdot 10^{-4}$	10^7	4,01
3,5	$5 \cdot 10^{-6}$	10^8	4,29
		10^9	4,56

Mobilities given by graph JH 11-6-57

$$C_s = \frac{Q}{\sqrt{\pi D t}}$$

$\frac{I}{V x_j}$: Hole case

C_B ↓ \ C_s →	10^{15}	10^{16}	10^{17}	10^{18}	10^{19}	10^{20}	10^{21}	10^{22}
10^{13}	0,142	0,90	3,87	14,8	59,8 (65,5)	250	1070	4630
10^{14}	0,193	1,10	4,45	16,5	~~59,6~~	269	1140	4920
10^{15}		1,47	5,40	19,0	73,2	295	1230	5260
10^{16}			7,12	22,9	842	329	1350	5680
10^{17}				29,9	101,2	378	1510	6220
10^{18}					131,9	456	1730	6960
10^{19}						616	2220	8000

$\frac{I}{V x_j}$: Election case

C_B ↓ \ C_s →	10^{15}	10^{16}	10^{17}	10^{18}	10^{19}	10^{20}	10^{21}	10^{22}
10^{13}	0,406	2,81	16,8	75,2	297	1230	5350	
10^{14}	0,628	3,42	19,4	84,0	324	1330	5730	
10^{15}		4,64	23,6	97,0	361	1452	6180	
10^{16}			31,7	117,5	416	1620	6770	
10^{17}				154,9	501	1870	7550	
10^{18}					652	2250	8680	
10^{19}						2950	10460	

December 1, 1957 Jean A. Hoerni

Method of protecting exposed p-n junctions at the surface of silicon transistors by oxide masking techniques.

The general idea underlying this invention is the building up of an oxide layer prior to diffusion of dopant atoms at those places on the surface of the transistor at which p-n junctions are expected to emerge from the body of the semiconductor. The oxide layer so obtained is an integrant part of the device and will protect the otherwise exposed junctions from ~~subsequent~~ contamination and possible electrical leakage due to subsequent handling, cleaning, canning of the device.

A second advantage resulting from the use of the technique to be described is the possibility of making contacts to the emitter, base and collector of a transistor on the same side of the wafer. In this way, the contact to the collector on the back side of a thick wafer and its accompanying high series resistance may be avoided. The passive areas of the junctions can be kept at a minimum (compatible with areas required to attach a lead to the exposed part of the base of the transistor), irrespective of the overall size of the wafer.

The basic procedure to be used is as follows: A wafer (of usual dimensions) is cleaned and preoxidized. Using photoresist technique, or other masking techniques, the oxide is removed on a series of islands, of size comparable with the area desired for the emitter of the

Jean A. Hoerni

transistor.

Top view of wafer

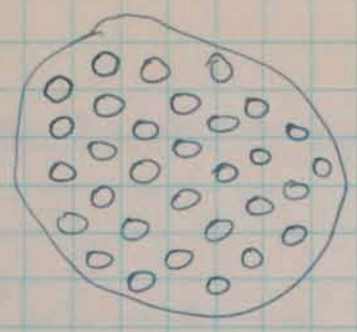


Fig. 1

Oxide layer removed within circles

The base and emitter regions are obtained by diffusion of impurities giving the desired conductivity type. The cross-section of across one of the unoxidized islands looks so after diffusion (for p type ~~bar~~ bulk material and a p-n-p transistor):

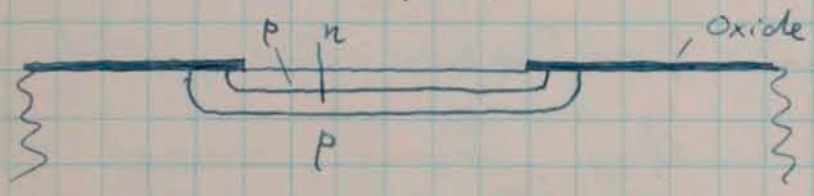
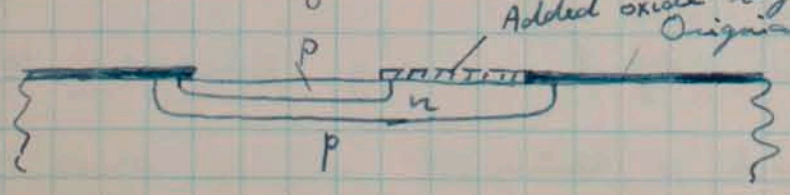


Fig. 2

It will be seen that in this way the parts of the silicon surface where the junctions emerge are masked at all times by the oxide layer. It is known that most impurities of interest (except Gallium) do not diffuse into the silicon wherever an oxide layer is present. Contacts have to be made to the three regions, which requires that parts of the oxide layer be removed to permit these contacts. The structure shown on Fig. 2 is not suitable in that the width of the base exposed to the surface is only a few microns, and is too small to make a suitable contact. A design imposing this ~~situation~~ situation is shown on Fig. 3:



Read and understood Dec 1, 1957
R. N. Noyce

April 29, 1958

Study of pnpn switching transistors

Dot	β_{pnp}	α_{pnp}	α_{npn}	W_{npn}^{base}
1	4	0,8	0,20	240
2	7	0,87	0,13	235
3	partial short			
4	5	0,83	0,17	237
5	6,5	0,87	0,13	228
6	4	0,8	0,20	226
7	2,5	0,72	0,18	217
8	5,6	0,85	0,15	215
9	3,0	0,75	0,25	212
10	2,8	0,74	0,26	218
11	partial short			
12	5,5	0,85	0,15	207
13	2,5	0,72	0,28	199
14	2,7	0,73	0,27	194

Dot	β_{pup}	α_{pup}	α_{upn}	W^{base}_{upn}
15	2,4	.71	.29	189
16	no contact			
17	sh			
18	2,7	.73	.27	189
19	5,0	.83	.17	186
20	5,6	.85	.15	185
21	4,4	.82	.18	174
22	3,2	.76	.24	167
23	3,2	.76	.24	169
24	2,2	.69	.31	162
25	no dot			
26	2,2	.69	.31	145
27	2,2	.69	.31	142
28	3,4	.78	.22	144
29	soft			
30	4,0	.80	.20	139
31	3,5	.78	.22	132
32	2,0	.67	.33	134
33	2,2	.69	.31	135
34	2,0	.67	.33	115
35	2,2	.69	.31	118
36	~~2,2~~			
37	6,0	.86	.14	119
38	6,0	.86	.14	102
39	4,8	.83	.17	100
40	sh			
41	3,2	.77	.23	101
42	2,0	.67	.33	105
43	2,2	.69	.31	100
44	sh			
45	4,0	.80	.20	77
46	3,0	.75	.25	69
47	3,5	.78	.22	66
48	2,5	.72	.28	70
49	2,6	.72	.28	70
50	5,6	.85	.15	55
51	sh			
52	sh			
53	2,6	.72	.28	50
54	1,7	.63	.37	49
55	soft			
56	sh			
57	sh			
58	sh			

Nov. 5, 58

Effect of gold and iron doping on ~~transistor~~ lifetimes in transistors

From a batch of NPN, emitter predeposited wafers, following tests have been made:

1) One test wafer was partly Ni plated on the back and diffused for 22 min at 1227° in furnace # 3. Mostly sharp transistors with β between 100 and 200 were obtained (no punch-through). The diffusion equivalent to the regular production time of 30 min at 1000°C is 17 min at 1227. We diffuse longer to get β's as high as possible. This test also shows no sign of ~~past~~ contamination brought about by previous gold diffusion in furnace # 3.

2) One wafer was evaporated with gold and diffused under the same conditions. No transistor action was observed, due to conversion of the collector to p type. Emitter-base junctions were still OK, although not quite sharp.

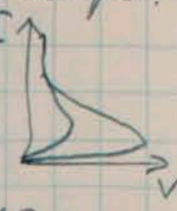
3) A wafer was evaporated with gold and diffused for 5 min. The back side was then etched to remove the gold-silicon eutectic, and half of it was Ni plated. The wafer was then diffused for 17 extra minutes. Opposite to the Ni plate, the transistors were sharp with β > 100, showing not much difference with wafer 1. On the other half of the wafer, conditions similar to wafer 2 were observed. On the borderline one transistor showed ~~ch~~ conductivity modulation in the ~~transis~~ collector typical of the effect observed on regular transistor of high collector resistivity.

4) A wafer was half plated with Ni and diffused in the production furnace - at 1000 °C for 25 min. It was then ~~plated~~ evaporated with gold and diffused for 15 min in furnace # 3 at 988 °C. High β units were obtained everywhere, showing no apparent effect of the gold.

5) A wafer was half evaporated with Fe and diffused for 21 min (3 in N_2, 18 in O_2) in furnace # 14 at 1227 °C. All transistors except 1 were soft (≈ 50 μa - 100 μa at 50 V) with β between 2 and 10, distributed in an erratic way over the wafer. The wafer was placed on a grooved boat, and it was clear that Fe had splashed over the whole back side of the wafer. Removal from furnace was relatively fast.

6) A wafer was evaporated with Au and diffused 30 min in furnace # 2 at 988 °C. The back side was etched and the wafer was then diffused in the same furnace for 22 min at 1227 °C. Same results

as in case 2) were obtained. The resistance between emitter and collector is very high (~ MΩ) but at higher currents drops. This is probably due to the fact that at higher temperature the gold atoms become ionized and the conduction is thereby raised.



7) Essentially a repeat of 5) (Fe) was made in furnace #3. After diffusion of 22 min, the transistors and diodes showed considerable softness. There was no marked difference between the evaporated and non evaporated areas. Beta values were 50 and larger in the center of the wafer and dropped to about 10 near the edges. Removal from furnace was slower than in 5).

8) A wafer evaporated with Fe was diffused (in O_2 throout) in furnace #3 for 10 min, then etched on the back, Ni plated on half the back side and rediffused for 12 min. Collector characteristics were soft throout, but β were 60 to 100 over the Ni area and 20 to 30 elsewhere. The removal was faster than in 7). It appears that Ni has restored lifetime but not the softness.

9) At this stage, a Ni plated test wafer was diffused 22 min. in #3. β's of 150 were obtained, sharp characteristics, and no sign of contamination could be detected.

10) A NPN wafer was evaporated with Fe, and then Ni plated on half of the back side. After diff. of 22 min in furnace #3, no significance in β could be detected (range 70 to 150). All transistors were soft (>1 ma at 10 V).

11) A PNP wafer was Fe evaporated on half of the back side and ~~diffused for 10 min~~ Ni plated on the other half. After diff. of 9 min in #3, betas of 15 to 40, and sharp characteristics were obtained in the Ni area (this is the normal result for PNP's). On the Fe side, β ranged from 2 to 12, mostly around 4-5; transistors were very soft and showed emitter-base shorts.

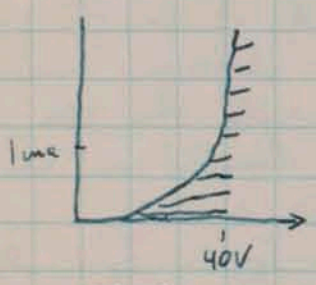
12) A repeat of 8) on a ~~PNP~~ NPN wafer gave essentially the same result. The softness was about the same on the two areas, β ~ 75 on Ni area, β ~ 10 to 20 on no Ni area.

13) The 2 halves of an NPN wafer evaporated with Fe were diffused in O_2 throout for 22 min. One half was "slow cooled" by removing the boat slowly and leaving the wafer on the boat. The other half was "quenched" by removing the boat rapidly and dumping the wafer on the diffusion table. Betas were respectively 150-200 and 5 to 8, all soft.
However; after heat treatment at 600°C for 10 min in argon and quench, β rose

in the second wafer back to 50. This is a serious objection to using Fe since this heat treatment is required by alloying operations.

14) A NPN wafer was evaporated with Au on half of the back side and diffused for 22+ min. ~~Ato~~ Results similar to 2) were obtained where Au was present, transistors with very high sat. resistance (~ 10000 Ω) elsewhere. "Alloying" at 600°C in Argon for 10 min. did not change characteristics appreciably. After leaving the wafer overnight at 600° (and removing quickly), it was observed that where no gold had been originally present, betas were between ~~100~~ 60 and 150 with sharp characteristics (except for shorts or punch-thru) and elsewhere transistors were also obtained with β between 4 and 10 mostly soft or shorted. R_{sat} ~ 200 Ω. Evidently, Au has gone out during annealing and the collectors had reverted to n type.

15) A NPN wafer was diffused in the production diffusion furnace at 1200°C for 35 min. Then half of the back side was evaporated with gold and the wafer was diffused at 1091°C in O_2 for 15 min. Betas between 5 and 10 were obtained everywhere. R_{sat} was of the order of 100000 at low collector currents and 3000 at higher currents. Collector characteristics were



~~After annealing at 600°C overnight~~ sharp where the gold had been plated, not elsewhere. After annealing at 600°, beta was reduced to a range between 2 and ~~6~~ 3, R_{sat} (with points) dropped to as low as 125 Ω. Charact. were sharp where the gold was originally plated, not elsewhere. Slight emitter base shorts were present.

After heating up again at 1091°C for 3 min., the wafer reverted to the high saturation resistance state shown at the start, beta increasing slightly to around 5.

Note: it was discovered that the wafer was not diffused at 1200, the furnace having broken down. Test 15) is therefore not significant as far as β values are concerned. These are the same as observed on ~~no~~ Au regular wafers after predeposition.

16) A repeat of 14) was made. However, the wafers, both NPN and PNP were first diffused at 1230°C (in furnace 7), for 22 and 10 min respectively and then gold evaporated, and then diffused again in furnace 3 for 15 min at 1080°C. NPN showed collector inversion, PNP low betas around 0.5 to 2. After overnight annealing at 610°C, NPN had reverted to high beta (150), low R_{sat}, most of the ~~first~~ dots ~~being~~ showing either low breakdown or shorts. The PNP had not essentially changed. It should be noted that most PNP transistors (except near the bottom of the wafer) were shorted due to the additional diffusion at 1080°C.

17) Au NPN wafer was, after diffusion, evaporated with gold, diffused at 972° for 15 min and removed from the furnace as follows: fast to the mouth of the furnace and let stand there on the boat. Betas were up to 150 and more, quite a few shorts, R_{sat} low.

18) Exactly the same treatment was given to two fragments of a PNP wafer, one Au evaporated, the other Ni plated. For the Ni sample β ranged between 10 and 15, some sharp, several soft. For the Au sample, β ranged from 1 to 2, characteristics mostly sharp.

It appears from these two runs that the electron lifetime is p material is less affected by the gold than the hole lifetime in n material. This would lead to the ideal conditions in NPN transistors where we want to reduce the storage time (hence hole lifetime) in the collector, but would like to keep high β (hence high electron lifetime) in the base.

19) Another NPN batch was ordered. This run was not as good as the previous one in that a test wafer (diffused at 1200°C for 35 min in the production furnace) showed softness, several shorts, and β in the vicinity of 40 only in the absence of Ni. After evaporating Au on the other half of the test wafer and diffused it in furnace #3 for 20 min at 972, characteristics became sharp and β rose to about 60. Another wafer was diffused with Au the same way and some transistors mounted with leads bonded to the silicon directly

C_{TG}	C_{OB} 0 ma 10 V	C_{OB} 1 ma 10 V	h_{FE} at 90 ma	t_d	t_r	t_s	t_f	V_{CE} sat	I_{B1}	I_{B2}	I_C	V_{BE} on
56	15.8	38	50		48	90	50	55	9 V	7 ma	11 ma	90 ma	5 V

There seems to be enough improvement in t_s to justify putting a run through the usual mounting procedure.

20) Au NPN wafer was, after diffusion of 35 min at 1200°C, evaporated with Au, and diffused at 1011°C for 15 min in furnace #3. Characteristics were sharp, $\beta \approx 25$-30, but R_{sat} was around 1500 Ω.

21) Au NPN wafer was, after diffusion of 35 min at 1200°C, evaporated with Au, and diffused at 982°C for 15 min in furnace #3. Characteristics were not quite sharp, $\beta \sim 35$-40, $R_{sat} \sim 300\,\Omega$. A fragment of the wafer not treated with Au showed $\beta \sim 30$, much softer characteristics, and several shorts. Two wafers will be processed in this way and mounted on the line.

22) The result of the run mounted on the line mentioned in the last paragraph gave was as follows

$t_d \simeq 40$ $t_r = 65$ $t_s = 30$ $t_f = 25$, $\beta \sim 20$, R_L $V_{CE}(sat) \simeq 2$ to 3

Dec 3,58 23) In order to reduce $V_{CE}(sat)$, we investigate the possibility of using initial material of lower resistivity. Using $\rho = 0.5\ \Omega$ cm, we diffused a wafer the regular way (diff. time of emitter 28 sec at 1200°C). A portion of the back side was Au evaporated and diffused for 15 min. at 982. No difference on the DC curve tracer was observed except that the characteristics were sharper where Au was present. Several transistors were shorted. The base was thin, as shown by the occurence of punch-through. $\beta \sim 100$ to 180, $BV_{BCO} = 70$, $V_{asympt.} = 19$.

24) Another wafer of 0.5 Ω cm was subjected to the same diffusion but diffused with the gold for 15 min at 1091°. Results: $\beta \sim 18$ R_{CS} (with points and thick wafer) ~ 5000, $BV_{BCO} \sim 85$, $V_{asym} \sim 35$

25) The same wafer was reinserted for 4 min in furnace 3 at a temperature of 1011. Then $\beta \sim 40$-50, $R_{CS} \sim 1000$, $BV_{BCO} \sim 75$ $V_{asympt} \sim 25$.

Jan. 1, 59 26) Two wafers of .5 Ω cm have been mounted through the line, after Au treatment (no Ni) at 972°C for ~~10~~ 15 min. Yield was very low (13 transistors). Typical results were

$t_s = 32$ $t_r = 40$, $t_s = 20$, $t_f = 15$

This did not change after $4\frac{1}{2}$ days storage at 300°C. This is one of the most interesting results so far. $V_{CE}(sat)$ values did change in an erratic way, changing by factors from 0.5 to 2. These values were erratic in the first place (from .8 to 6.5 V).

In order to improve the yield Ni treatment prior to Au treatment is tried.

27) Another crystal of .5 Ω cm has been grown and used to repeat run 26. After Au treatment at 967°C for 15 min, the yield on a test wafer was

OK	43%	} "Good" units 63 %	$\beta \sim 100$
Punchthrough	20%		
LB	17%		
EC shorts	20%		

A test wafer diffused with Ni (no Au) gave the following

OK	57%	} "Good" units 60 %	$\beta \sim 30$
PT	3%		
soft	4%		
LB	9%		
EB	3%		
EC	24%		

12

January 20, 1959 Jean A. Hoerni

Use of selective ~~lifetime~~ control of electron and hole lifetimes in semiconductor devices

Several characteristics of semiconductor devices are strongly dependant on the recombination rate, or lifetime, of elections and holes in excess of carrier equilibrium densities. So far, technological progress has moved in the direction of ever increasing lifetime values. Present obtainable lifetimes are indeed high enough that it is now possible and feasable to reduce them in a controlled manner to a level consistent with best device behavior. Considering the particular case of a transistor, it is found, however, that the lifetime requirements are not the same in the different regions of the transistor. In partialar, high lifetime values are desirable in the base material (since they yield high current gains), whereas low lifetimes values are desirable in the collector material (in order to reduce storage effects when turning off a transistor used in switching applications). In double diffused transistors, it is found, that contrary to these equirements that the lifetime is lower in the (diffused) base than it is in the collector (made of undiffused semiconductor).

The purpose of this disclosure is to describe a way in which the lifetimes can be selectively controlled over semi-

conductor regions of different polarities (p or n). In the particular case of the double diffused transistor mentioned above, this procedure makes possible a reduction in collector lifetime (leading to faster switching response) without sacrifice in base lifetime (or current gain).

The procedure to be described makes use of the properties of specific impurities to affect the recombination rate of electrons and holes to a different extent*. It can be shown that the

* In the steady state (or, in the general case, when trapping effects can be neglected), electron and hole recombination rates, or electron and hole lifetimes, are always necessarily the same in a given semiconductor region. Electron and hole lifetimes defined in the text refer to lifetimes τ_{no} and τ_{po} prevailing in strongly p-type material, or strongly n-type material respectively. electron and hole lifetimes, τ_{no} and τ_{po} respectively, are related to the capture cross-section of the impurities in question by

$$\tau_{no} = \frac{1}{v_n N \sigma_{no}} \quad \text{and} \quad \tau_{po} = \frac{1}{v_p N \sigma_{po}} \qquad (1)$$

where v_n are v_p are the carrier thermal velocities, N is the density of impurity centers, and σ_{no} and σ_{po} are the capture cross-sections in strongly p-type and n-type material. On the basis of formula (1) selective lifetime controlled may be achieved by doping the transistor with impurities for which the difference between σ_{no} and σ_{po} is large. In our

particular application of a npn transistor, the condition for reducing the storage time without affecting the current gain is therefore $\sigma_{po} \gg \sigma_{no}$. In the case of a pnp transistor the equivalent condition is $\sigma_{no} \gg \sigma_{po}$.

In silicon or germanium, impurities suitable for lifetime control are those which cause deep energy levels close to the middle of the energy gap between the valance and the conduction band. To mention a few, gold, iron, nickel, copper, zinc, silver, manganese, platinum, have been found to have this property. Contrary to the usual dopants of the third and fifth column of the periodic table, the deep level impurities diffuse at a fast rate, so that it is quite feasable to dope a transistor structure uniformely with them over a time period in which further diffusion of the already present p and n regions is negligible. Capture cross-sections of the deep level impurities are generally unknown, or only known at doping levels of little interest in device fabrication. The available evidence, however, indicates that they are large in some cases and likely to fulfill the inequalities quoted above.

The following gives the particular application of gold doping to in double diffused silicon npn transistors. Subsequent to the usual diffusion of the base and emitter dopants, gold is plated or evaporated on the collector side, and diffused into the

transistor over a time period and at a temperature compatible with uniform final doping and optimum concentration. Representative values are 30 minutes and 980 °C. Under these conditions, the author has found that the current gain, or h_{FE} values are hardly affected, whereas the storage time after turn off of the transistor is reduced by a factor of 5 to 10. The differential effect of gold on τ_{po} and τ_{no} is observed in an even more striking way if pnp transistors of equivalent design are doped with gold under the same conditions. Here the current gain values depend on hole lifetime and drop to less than one hundredth of their original values*. Clearly in the pnp case, another impurity of effect opposite to gold, remains to be found.

Jean A. Hoerni 1-20-59

Read + understood 1-21-59, Jan 20, 1959
R.N. Noyce

January 28, 1959

A cure to possible dendrite formation on silver topped transistors: Use the seal in glass which hopefully is being worked on with the primary purpose of protecting the junctions.

Jean A. Hoerni

January 29, 1959 Effect of copper on lifetimes

1) An npn wafer ($\rho = 1.7\ \Omega$cm) was diffused without Ni, evaporated with Cu on half of it and diffused in furnace #3 for 15 min. at 975°C. Collector characteristics were very soft throughout. Where no Cu was present β was ~ 80, EB diodes sharp. With Cu, β was between 10 and 20, EB diodes soft. The presence of Cu raised the saturation resistance by a factor of less than 2. Annealing for 10 min at 580° did not raise β significantly

2) A wafer of the same run was tested with Ni and diffused 5 additional minutes at 1200°. Some units were sharp (or showing PT) but there were still many softs or LB. This seems to indicate that this particular batch of wafers is not a good one.

3) Evaporating a wafer of the same series and diffusing at 1230 for 5 min gave low β-values (5 to 10), considerable softness (2 ma at 80 V). R_{sat} ~ 100–200 Ω (with points).

4) One PNP wafer was, after emitter predeposition, evaporated with Cu over half of the backside and diffused at 1225 for 9 min. in the Burrel furnace in oxygen. Gettering took place on areas opposite to Cu. Betas were around 8–18 all over the wafer. This indicates that the hole lifetime in n-type material is not affected as much as the electron lifetime in p-type material, and fulfils therefore the conditions laid out at the end of the disclosure on page 15.

5) Another PNP wafer was subjected to the same treatment, except that the diffusion time was raised to 11 min, and that the first part of that diffusion took place in nitrogen (to avoid sputtering of the copper). Betas of 15 to 20 were obtained throughout, sharp characteristics on the Cu area (and also in part opposite to the unmetalized area). It was observed also that switching (due the metal contact on the back-side — the SiO_2 layer had been removed before Cu evaporation) in general took place at higher currents (~ 300 ma) opposite to the copper than elsewhere (~ 50 ma). There were exceptions.

January 30, 1959

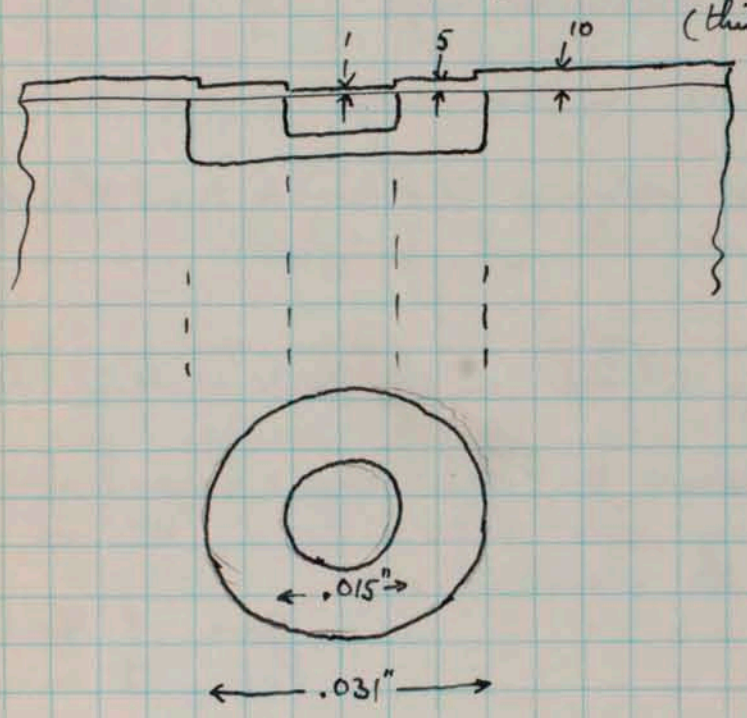
6) Two PNP wafers, diffused 11 and 13 min with Cu, have been sent through the line, being mounted with Al contacts.

March 2, 1959

A method of manufacture of PNP transistors with oxide protected junctions

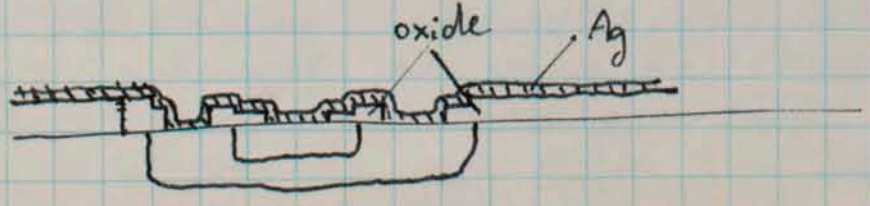
This method outlines some ideas discussed on p. 3 with newer techniques using silver as a contact metal.

Starting with a p-type wafer, the wafer is base and emitter diffused in the manner indicated on pages 3 and 4. We end up with the following structure:



(thickness of oxide in fringes .273 μ)

At this stage we use a photoresist method to remove the oxide on a dot contained inside the emitter dot and on a ring contained inside the base ring. Then silver is evaporated over the whole wafer.



The wafer is then alloyed. Only the areas of silicon that are

in contact with silver alloy to give Ag-Si eutectic layers. Then the remaining (unalloyed) silver on top of the oxidised portions of the wafer is etched off. One way to do this is to cover the (alloyed) silver dot and rings with a photoresist mask and etch off the silver in ferric nitrate. Another way is to use the differential adhesion of silver on silicon and silicon oxide to rub off the silver on oxidised areas without affecting the silver on the dots and rings. If necessary, a separate alloying can be made in the alloy surface subsequent to evaporation, in case that imperfect alloying is obtained on the step heater of the evaporator.

Wafers are then Al plated and alloyed on the back side (after back lapping down to standard thickness), then diced (no mesa is necessary here) and mounted in the standard way.

Jean A. Hoerni

April 17, 1959

Study of boron diffusion for base doping of NPN transistors

In order to make transistors in the way described on p. 3, we need an impurity for base doping which is masked by an oxide layer. Since Ga is not masked, we have to try boron. Preliminary results indicate that the most promising way is to predeposit a boron-glass layer on the silicon with BCl_3 at a suitable temperature, remove the layer in HF and then diffuse at higher temperature (around 1200°C) to the desired ~~temp~~ junction depth. The predeposition temperature is to be determined from the final V/I value required. It has been found that less uniformity and too high V/I values are obtained if the boron glass layer is left over the wafer during the diffusion phase (It then tends to act as an infinite source giving doping corresponding to the high temper.)

T (predep.)	V/I (after predep.)	V/I (HF rinse, 30 min diff. 1215°)	V/I (No rinse, 30 min diff 1215)
962	80 ± 5	> 100	2 to 4
1048	4.2 ± .2		
1016	15 ± 1.5	24 ± 1	1.8 to 4

Another run gave

1015	13.5	After HF rinse 5 hrs at 1235 V/I = 12.3 ± .8 (on two wafers)
938	60 ± 2	1 hr dry O_2 → 220 ± 10 1 hr O_2 + steam → 80 ± 5

It seems that more boron is outgassing in wet than in dry oxygen. This is in line with the fact that oxide is not supposed to mask against certain impurities in an atmosphere saturated with water vapor

978	28 ± 1.5	After 1 hr dry O_2	26 ± 1.5 Ω	x_j = 13 fr.
980	~35	"	~39	

April 23, 59

Study of h_{fe} behavior on test wafers on FT 4100.

a) One wafer was taken out of a run where the preran test wafer had shown a β of 13 for 16 min diffusion at 1200. It was diffused for the same time, split in two, Au plated on one half and rediffused at 1040 for 12 min. Both showed β of 40 to 50, soft where there was no Au.

June 24, 1959

Method of reducing emitter sheet resistance by metallizing the emitter area to within 2 microns of the base emitter junction

In order to improve the behavior of a transistor, particularly h_{fe} at high currents, it is advantageous to reduce the sheet resistance of the emitter, among other things, down to a minimum, and this right up to the edge of the emitter base junction. A convenient

May 20, 1959
J Hoerni

4200 X
Oxide No Mesa metalized NPN

		100μa		15ma	15ma			[illegible]	[illegible]				15ma	15/5ma
			10V			30 v	30 v	10V	0.5v	10v	10v			
						~~25~~ 30 °C	150°C			20 mc		R_B=10Ω	R_L=40	R_L=[illegible]
BVCEO	BVCBO	BVEBO	IB	VCE(S)	VBE(S)	ICBO	ICBO	Cob	CTe	hfe	rbCc	LVCER	t(d+r)	t(s+f)
56	99	9.3	6.1	0.70	.93	.0009	~~[illegible]~~	19.2	57	3.4	200	77		
51	93	9.2	5.1	0.64	.95	.0010		19.6	57	3.4	205	74		
56	93	9.7	6.4	.79	.95	.0012		19.6	58	2.9	198	79		
~~90~~	~~160~~											~~114~~		
53	91	9.5	5.4	.62	.96	.0011		19.8	58	3.6	218	74		
56	95	8.3	5.5	.71	.96	.0012		19.4	56	3.4	214	78		
55	76	9.2	5.6	.73	.95	.0009		19.9	56	3.2	194	77		
44	95	10.2	2.9	.55	.97	.0017	1.1	20.7	53	4.1	258	69		
43	87	10.3	2.8	.54	.98	.0007	.6	21.1	53	4.0	278	65		
50	90	9.8	3.2	.62	.98	.0007	.64	19.6	53	3.9	242	74		
53	100	9.3	4.7	.68	.95	.0017	1.4	19.3	59	3.3	180	81		
56	96	(6.3)	4.6	.75	.95	.0017	1.3	20.1	58	2.2	183	77		
43	79	10.3	2.8	.45	.98	.0013	1.0	20.7	52	4.2	278	64		
51	~~100~~ 98	9.8	3.5	.64	.96	.0008	.8	19.6	55	3.8	212	78		
51	87	9.1	4.7	.67	.96	.0016	1.2	19.7	59	3.3	188	80		
56	102	8.4	4.7	.86	.96	.0018	1.4	19.3	58	3.3	180	87		
42	84	10.3	2.7	.51	.97	.0011	.80	21.2	52	4.1	274	68		
47	93	10.2	3.0	.58	.97	.0009	.70	20.1	52	4.0	247	72		

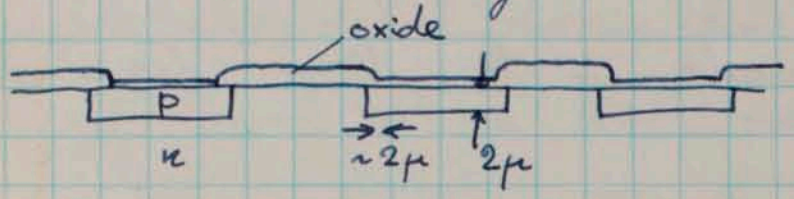
Witnessed measurements + recording of data R.W. Lowe May 20 '59

way to do so can be deduced from the invention described on pp. 3 and 17. Consider the simplest case of a wafer with diodes made by oxide masking.

Step 1 : coating wafer with uniform oxide layer

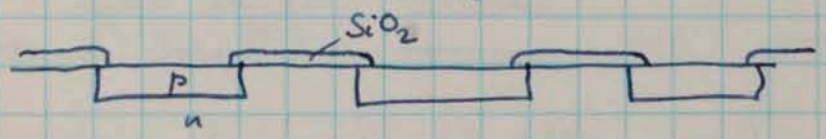
Step 2 : removing oxide on pattern of dots.

Step 3 : predepositing and diffusing base impurity. During the diffusion phase an oxide layer (thinner than the layer on masked areas) is grown

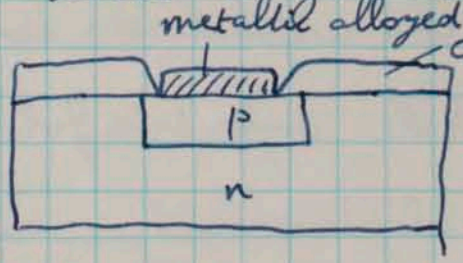


(p n case considered here as example

Step 4 : the oxide layer is etched just for the time necessary to expose the p type areas



Step 5 : a metal is evaporated on the top of the wafer. Due to differential adhesion, it can be removed on oxidized areas but not on the bare silicon. The metal is alloyed and the wafer subsequently diced to give the final diode structure

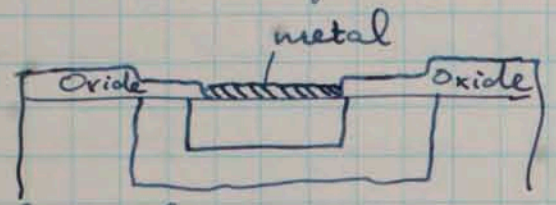


It will be seen that by this method the distance between the metallic layer of low resistivity and the junction is of the same order as the penetration of the p-type dopant under the surface (e.g. around 2 microns). Even if the metal slops over on the oxide layer, the junction isn't

June 24, 1959

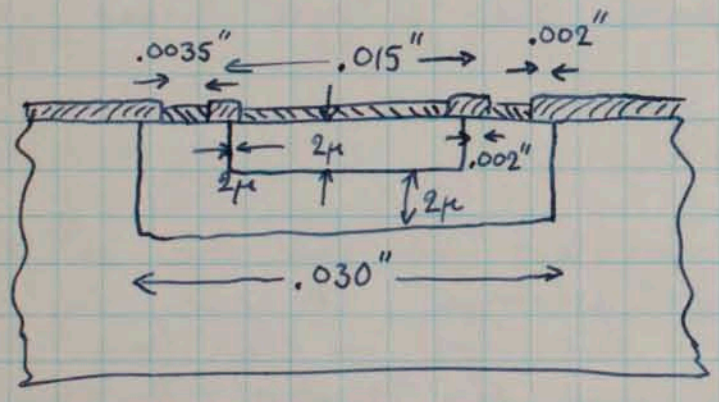
shorted ~~since~~ because of the intermediate thin layer of oxide. Moreover the junction is fully protected by this same oxide layer for ever thereafter.

The same method can be applied to the emitter of a transistor giving the final structure



[The base contact is made in the way described on pages 3 and 17]

A characteristic transistor would look like



Oxide layer
Alloyed metal layer

← Note inches and micron units!

A practical realization of this structure has been made by using silver as the metal contact. Gold is another likely metal, as well as aluminum.

Jean A. Hoerni
June 24, 1959

Read & understood
Jay T. Last June 24, 1959.

Dec 13, 1959

Content of oxygen in our material (P. Flint)

Due to lower stirring less oxygen in our material. We observe 4×10^{14} donors, compared with Fuller and Logan's $2 \cdot 10^{16}$. Got it down on p type wafers

March 3, 1960

Noyce
Moore
Freund
Grinich
Last
Roberts

On the application of the Merck growing technique to device structures

On the use of grown crystal films

Here are some thoughts on possible immediate applications of the film growing technique described by the Merck people ~~(Krode)~~ during their visit here last month.

It seems to me that, while it is conceivable that this process may eventually throw out of business ~~the~~ diffusion techniques presently used in the manufacture of silicon devices, (and therefore make useless a large part of ~~the~~ our related technology, oxide protection, alloying, etc.), it would be desirable to try to incorporate this new technique into our existing technology. That is to say, I believe that significant improvements can be made on some of our devices by using the growing technique at the early stage of device fabrication and by using diffusion and oxide masking techniques at the final fabrication stage. I will quote two examples ~~which~~ to illustrate the above statement.

i) PIN diode

A N-type wafer is grown by the Merck technique up to a thickness of 5 mils, say. Then the dopant is removed from the gaseous ambient, ~~as~~ so that ~~of~~ a top layer of intrinsic ℓ

resistivity and thickness from a fraction of to several mils is grown on top of the previous layer. The wafer is then oxidized and our usual masking and diffusion techniques are used to create P-type regions, with the PI junction protected by an oxide layer. It is worth pointing out that the degree of control of this structure would be considerably better than in the present all-diffusion scheme, where the thickness of the I region depends strongly on small relative variations of the two diffusion fronts approaching each other from opposite sides of the wafers.

2) Power transistors

The possibility of growing an NN^+ wafer by the Merck technique and subsequently diffusing a P-type base and N-type emitter (by 4000 or 4200 techniques) will obviously result in a greatly lowered collector resistance if the size of the grown N region is made of the order of the penetration by diffusion of the base dopant. The extension to PNIP structures is obvious. It should also be noted that for mesa transistors the base layer could also be laid out during the growing process, so that only the emitter would have to be diffused.

I recommend that in view of the willingness of Merck to supply us with samples, NN^+ or IN^+ slices of the type described above be ordered, so that compound grown-diffused structures may be obtained at an early date

Jean A. Hoerni

April 15, 60

On 4600 transistors

Attempts to dope 4500 transistors with copper are being made. Run 4600-1 was doped with Cu after boron ~~diffusion~~ predep. for 35 min at ~~1200 C~~ 1100 C After that, it went back to the line (Pt base ring, etc.). 5 units were mounted but none showed a difference in $t_s + t_f$ compared with standard units of similar betas.

Run 4600-2

April 27, 60 No great difference was obtained when wafers were first Ni plated and diffused and then redifused with Cu on the top of the Ni.

Another wafer was diffused without nickel in the ordinary fashion. Au evaporated on the back and diffused at 750°C for ½ hr. Mesas showed fair gettering action (not quite sharp), normal betas (around 50) but no effect on storage time as determined on the wafer.

The other fragment of the previous wafer was treated the same way except that it went for 1½ min at 1000°C Betas were down to 7.

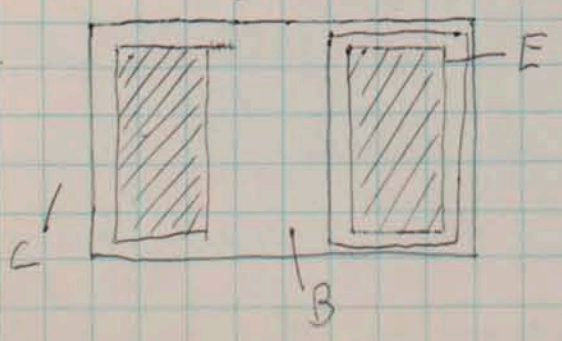
April 28, 60 Another fragment of the same wafer was ~~de~~ Au evaporated after diffusion and diffused for ~~20 sec~~ 30 sec at 1000°C Betas were down to 10 – 12

		I_c	I_{b_1}	I_{b_2}	t_s	t_f	β
Reference transistor (no Au)	⊗	20	+5	−5	40	106	12.5
			+10	−10	50	110	
		20	+ 2.5	−2.5	100	120	15
			+5	−5	300	180	
Fragment ⊗ annealed ~30 sec @ 750C ⊗		20	+5	−5	62	118	16
			+10	−10	72	118	

May 24, 1960 11:45 AM

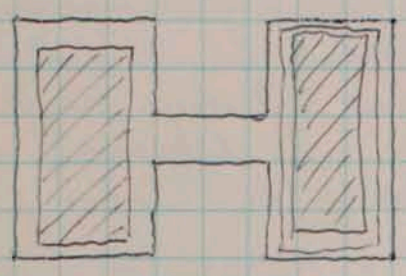
DCTL transistor design

In our present design for such a transistor to be used in micrologic units, we have the following structure.

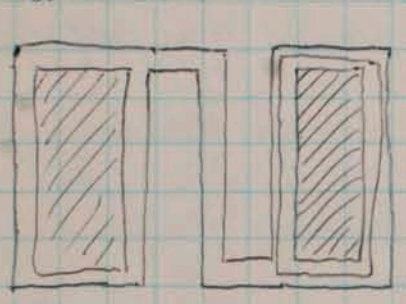


The high base resistance necessary to a DCTL transistor is obtained by removing the base contact as far away as possible from the E, B. junction.

The proposed structure is as follows



Another alternative



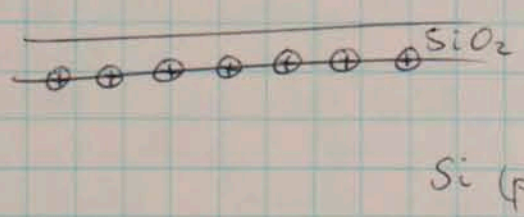
For the same overall geometry the base resistance is increased by a factor equal to the constriction of the intermediate path.

A secondary advantage is a reduction in base-collector capacitance.

June 27, 1960

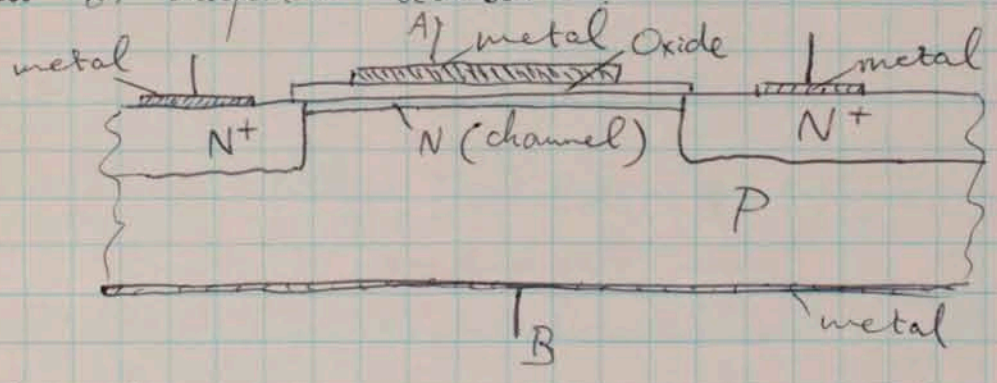
Logic using unipolar transistors

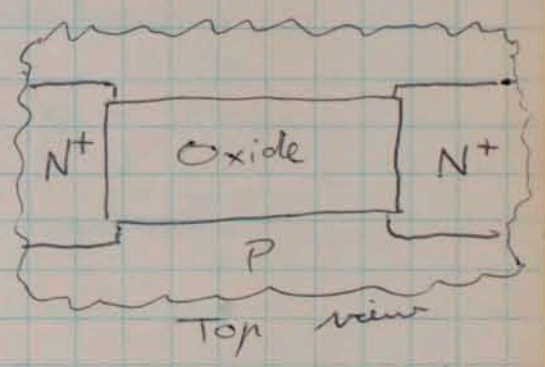
The scheme described by Wallmark and Marcus (IRE Trans. Electr. Comp. EC 8, 98, 1959) is not very attractive because of the practical difficulties involved in diffusing and lapping to shape their unipolar transistor elements. The techniques proposed here are based on the appearance of inversion layers on p type silicon covered by an SiO_2 layer and doped with suitable fast moving impurities like Mn or Ca.



The impurities in question are locked in at the $Si - SiO_2$ interface and give rise to donor states (either in their elemental form or in their pairing to oxygen), after heat treatment in the range of

600° to 900°C. These donor states induce n type conductivity in the bulk of the Silicon p-type under the surface and, if the resistivity of the material is high enough, an inversion layer will result. The conductivity of this channel can be pinched off a), by applying a reverse bias on the junction created between the channel and the underlying p-type material or b), by applying a field through the oxide by means of a metal electrode on the outside surface of the oxide. Channels of suitable dimensions can be obtained by selectric etching of the oxide. Since no channel or n type layer is present where no oxide is present, it is necessary to diffuse n-type regions where contacts to the channel are to be made. The simplest structure is a field effect or unipolar transistor

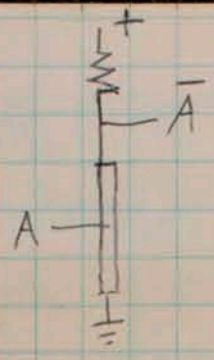


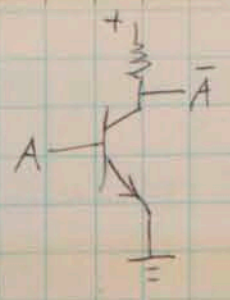


The channel conductance is controled by applying a voltage either to electrode A, or to electrode B.

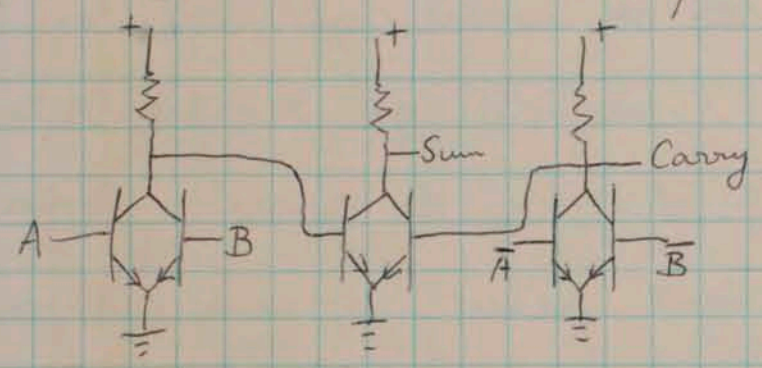
Let us use the following symbol for a unipolar transistor with an n type channel of the above type. It will be noted that the

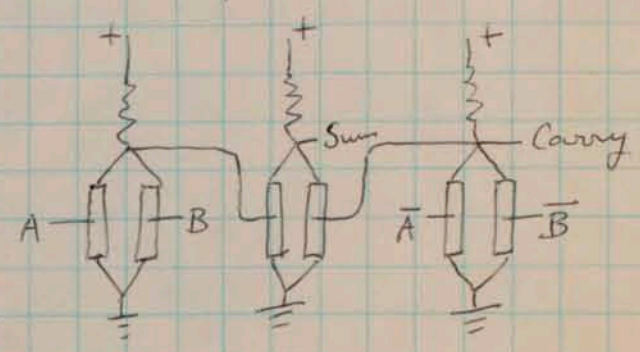
basic function of such a unit in series with a resistor and a power source is an inverter.

Namely 

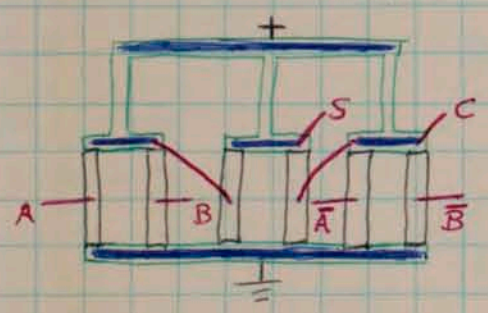
This does the same function as 

It follows that any logic function made of NPN diffused transistors may be made also by replacing these transistors by unipolar transistors. Consider the half adder as an example





The unipolar half adder may be built as follows, provided that top side contacts of type A described on p.27 are used.



Diffused n-layer

Metalized diffused n-layer

Connections

October 11, 1960

On the effect of Nickel on PNP beta degradation on opening test

Severe degradation of standard 4500 transistors beta is observed when the transistor is kept in saturation by applying, for instance 300 ma in the collector and 50 ma in the base. The beta drop may exceed 50% after a few hours On NPN transistors, however, beta goes up under the same conditions, although by a lesser amount. In both cases

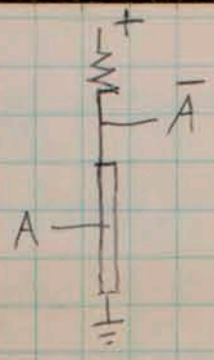
M-O-S Diodes

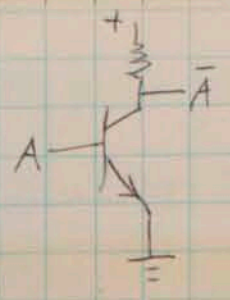
f = 500 kc/sec

T = 29°C

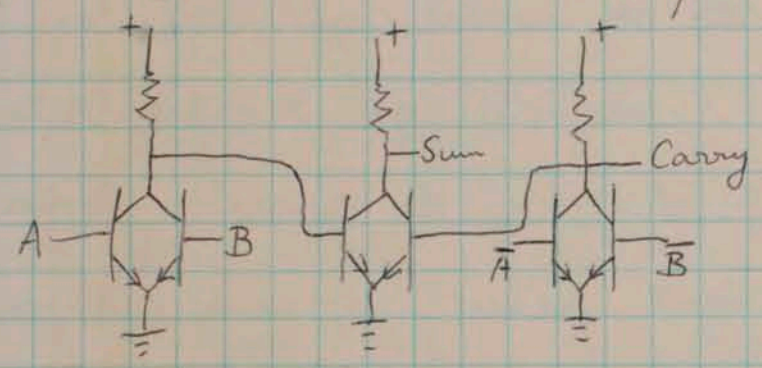
Bias [V]	#1		#2		#3	
	C [pF]	R [kΩ]	C [pF]	R [kΩ]	C [pF]	R [kΩ]
0	42.3	79.7	44.5	66.7	34.2	87.5
1	42.0	78.5	43.7	67.0	33.7	86.0
2	41.3	75.9	42.2	68.5	32.7	85.0
3	40.0	73.5	39.7	71.0	30.7	81.5
4	37.7	73.6	34.5	79.2	25.6	68.3
5	32.1	73.0	28.8	97.5	15.5	54.3
6	18.8	64.7	21.9	128	4.9	114.0
7	6.2	116	12.2	160	2.8	650
8	2.8	552	6.7	240	2.5	1.5 MΩ
9	2.3	1.4 MΩ	3.4	550		
10			2.8	1.3 MΩ		

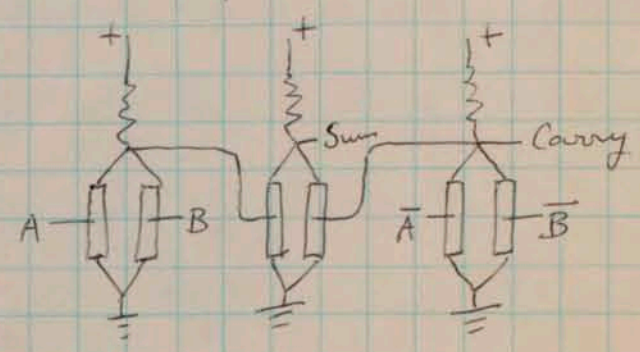
H. Wolf

Namely 

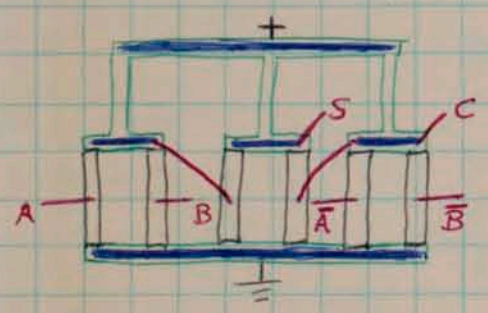
This does the same function as 

It follows that any logic function made of NPN diffused transistors may be made also by replacing these transistors by unipolar transistors. Consider the half adder as an example





The unipolar half adder may be built as follows, provided that top side contacts of type A described on p.27 are used.



Diffused n-layer

Metalized diffused n-layer

Connections

October 11, 1960

On the effect of Nickel on PNP beta degradation on opening test

Severe degradation of standard 4500 transistors beta is observed when the transistor is kept in saturation by applying, for instance 300 ma in the collector and 50 ma in the base. The beta drop may exceed 50% after a few hours On NPN transistors, however, beta goes up under the same conditions, although by a lesser amount. In both cases

the beta change is recovered by heat treating at 300°C.
The asymmetric effect points out to the influence of a charged impurity which is moved through the silicon under the drift fields appearing under the operating test, and which is brought back to its initial equilibrium value under thermal treatment.

Since nickel is a common fast moving impurity in our transistors, its possible influence was investigated by making a PNP run without nickel treatment. Units were mounted in the conventional way, but did not undergo the 70 hrs aging period at 300°C. Results on low and medium current beta on 4 units did not show any degradation.

Unit	I_b	h_{fe} original $(t=0)$	1hr 10'	3hr 55'	7hr 5'	22hrs
1	10μa	35	39	38	39	39
	.2 ma	49	50	50	50	51
2	10μa	38	39	40	41	43
	.2 ma	49	47	47	48	49
3	10μa	290	300	300	300	310
	.04 ma	290	300	300	300	310
4	10μa	296	29 30	30	30	31
	.25 ma	37	39	39	38	40

Units 1 and 2 were bonded with Au wires
" 3 " 4 " " " Al "

30 December 22, 1960

References on light emission or absorption in Silicon

Haynes & Westphal PR 101, 1676 (1956) – "Radiation resulting from recombination of electrons and holes in Silicon" Discusses forward biased pn junctions and emission spectra both for intrinsic radiation and extrinsic radiation in presence of various dopants.

MacFarlane & Roberts PR 98, 1865 (1955) – "Infrared absorption of Silicon near the lattice edge". Data on absorption edge, band gap width ~~and~~ at various temperatures.

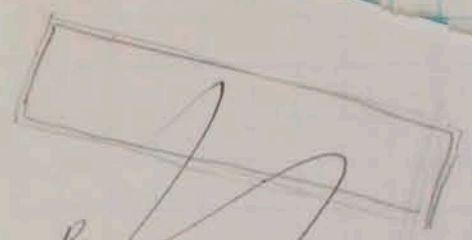
Predeposit
Boron on one side

Remove on other side

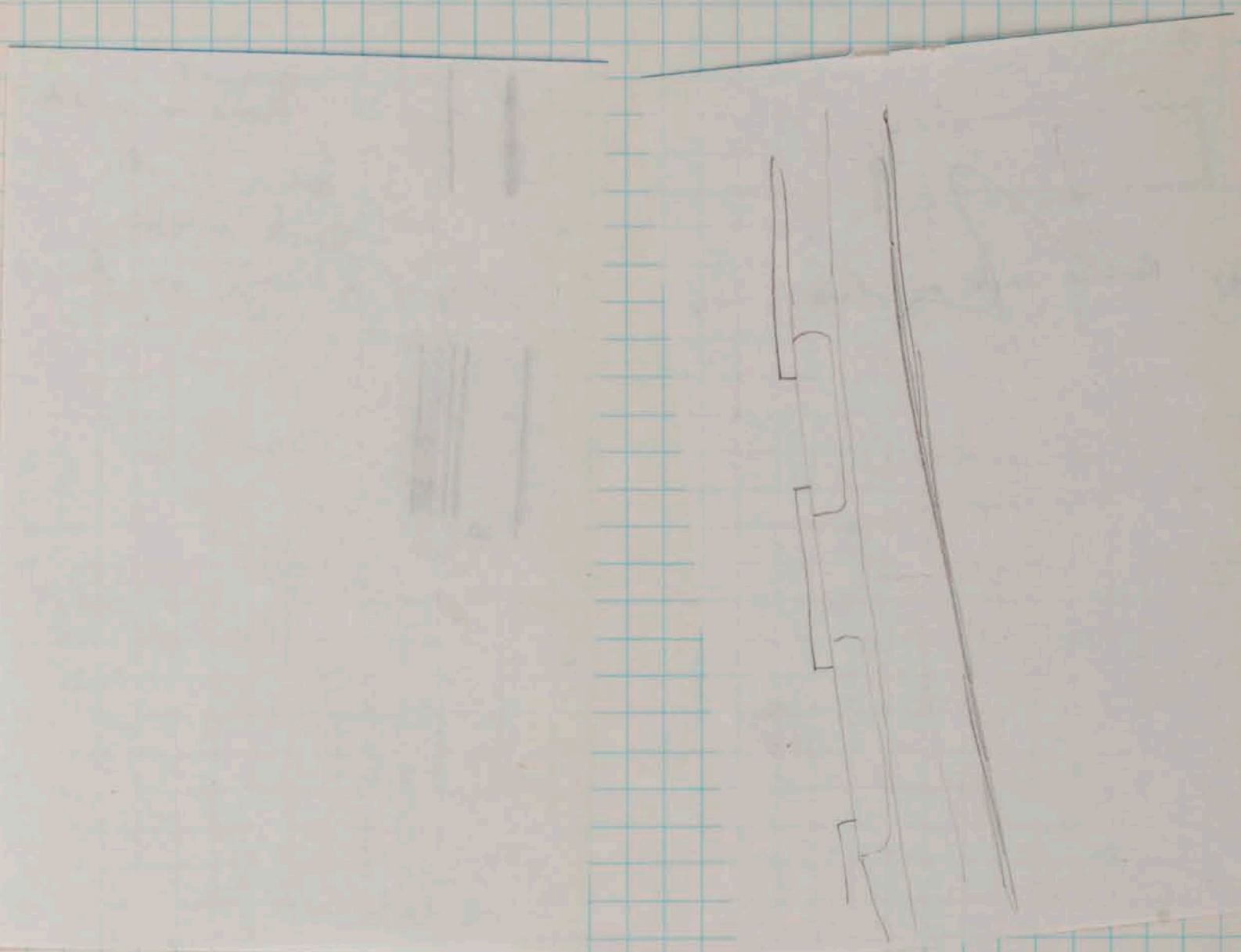
Oxide mask

Predeposit antimony on other side

1)



2) Remove oxide on back



PATENT DISCLOSURE

Ref: Pgs. 3 and 4 of Fairchild Notebook No. 3; December 1, 1957
Jean A. Hoerni

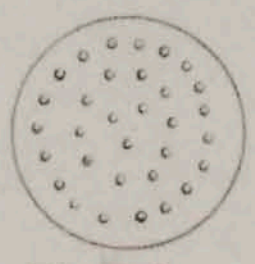
Method of Protecting Exposed p-n Junctions at the Surface of Silicon Transistors by Oxide Masking Techniques

The general idea underlying this invention is the building up of an oxide layer prior to diffusion of dopant atoms at these places on the surface of the transistor at which p-n junctions are expected to emerge from the body of the semiconductor. The oxide layer so obtained is an integrant part of the device and will protect the otherwise exposed junctions from contamination and possible electrical leakage due to subsequent handling, cleaning, canning of the device.

A second advantage resulting from the use of the technique to be described is the possibility of making contacts to the emitter, base, and collector of a transistor on the same side of the wafer. In this way, the contact to the collector on the back side of a thick wafer and its accompanying high series resistance may be avoided. The passive areas of the junctions can be kept at a minimum (compatible with areas required to attach a lead to the exposed part of the base of the transistor), irrespective of the overall size of the wafer.

The basic procedure to be used is as follows: a wafer (of usual dimensions) is cleaned and pre-oxidized. Using photoresist technique, or other masking techniques, the oxide is removed on a series of islands, of size comparable with the area desired for the emitter of the transistor.

Top view of wafer.



Oxide layer removed within circles.

Figure 1.

The base and emitter regions are obtained by diffusion of impurities giving the desired conductivity type. The cross-section across one of the un-oxidized islands looks so after diffusion (for p type bulk material and a p-n-p transistor):

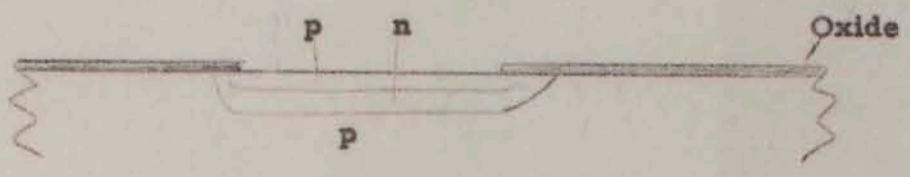


Figure 2.

It will be seen that in this way the parts of the silicon surface where the junctions emerge are masked at all times by the oxider layer. It is known that most impurities of interest (except Gallium) do not diffuse into the silicon wherever an oxide layer is present. Contacts have to be made to the three regions, which requires that parts of the oxide layer be removed to permit these contacts. The structure shown on Figure 2 is not suitable in that the width of the base exposed to the surface is only a few microns, and is too small to make a suitable contact. A design improving this situation is shown on Figure 3:

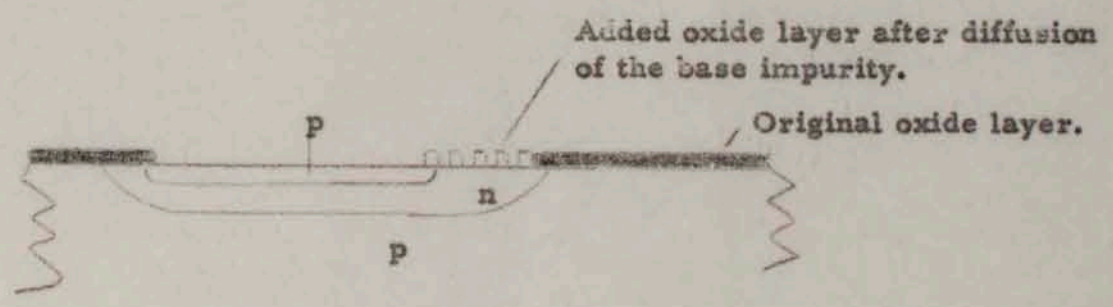


Figure 3.

JAH:mlw
1/14/59

PATENT DISCLOSURE

Ref: Pgs. 12,13,14 and 15 of
Fairchild Notebook No.3
January 20, 1959
Jean A. Hoerni

Selective Control of Electron and Hole Lifetimes in Semiconductor Devices

Several characteristics of semiconductor devices are strongly dependent on the recombination rate, or lifetime, of electrons and holes in excess of carrier equilibrium densities. So far, technological progress has moved in the direction of ever increasing lifetime values. Present obtainable lifetimes are indeed high enough that it is now possible and feasable to reduce them in a controlled manner to a level consistent with best device behavior. Considering the particular case of a transistor, it is found, however, that the lifetime requirements are not the same in the different regions of the transistor. In particular, high lifetime values are desirable in the base material (since they yield high current gains), whereas low lifetime values are desirable in the collector material (in order to reduce storage effects when turning off a transistor used in switching applications). In double diffused transistors, it is found that, contrary to these requirements, the lifetime is lower in the diffused base than it is in the collector (made of undiffused semiconductor).

The purpose of this disclosure is to describe a way in which the lifetimes can be selectively controlled over semiconductor regions of different polarities (p or n). In the particular case of the double diffused transistor mentioned above, this procedure makes possible a reduction in collector lifetime (leading to faster switching response) without sacrifice in lease lifetime (or current gain).

The procedure to be described makes use of the properties of specific impurities to affect the recombination rate of electrons and holes to a different extent. In the steady state (or, in the general case, when trapping effects can be neglected), electron and hole recombination rates, or electron and hole lifetimes, are always necessarily the same in a given semiconductor region. Electron and hole lifetimes defined in the text refer to lifetimes τ_{no} and τ_{po} prevailing in strongly p-type material, or strongly n-type material respectively. It can be shown that the electron and hole lifetimes, τ_{no} and τ_{po} respectively, are related to the capture cross-section of the impurities in question by

$$\tau_{no} = \frac{1}{v_n N \sigma_{no}} \quad , \quad \tau_{po} = \frac{1}{v_p N \sigma_{po}} \qquad (1)$$

where v_n and v_p are the carrier thermal velocities, N is the density of impurity centers, and σ_{no} and σ_{po} are the captive cross-sections in strongly p-type and n-type material. On the basis of formula (1) selective lifetime

control may be achieved by doping the transistor with impurities for which the difference between σ_{no} and σ_{po} is large. In our particular application of a npn transistor, the condition for reducing the storage time without affecting the current gain is therefore $\sigma_{po} \gg \sigma_{no}$. In the case of a pnp transistor the equivalent condition is $\sigma_{no} \gg \sigma_{po}$.

In silicon or germanium, impurities suitable for lifetime control are those which cause deep energy levels close to the middle of the energy gap between the valence and the conduction band. To mention a few, gold, iron, nickel, copper, zinc, silver, manganese, platinum, have been found to have this property. Contrary to the usual dopants of the third and fifth column of the periodic table, the deep level impurities diffuse at a fast rate, so that it is quite feasable to dope a transistor structure uniformly with them over a time period in which further diffusion of the already present p and n regions is negligible. Capture cross-sections of the deep level impurities are generally unknown, or only known at doping levels of little interest in device fabrication. The available evidence, however, indicates that they are are large in some cases and likely to fulfill the inequalities quoted above.

The following give the particular application of gold doping in double diffused silicon npn transistors. Subsequent to the usual diffusion of the base and emitter dopants, gold is plated or evaporated on the collector side, and diffused into the transistor over a time period and at a temperature compatible with optimum concentration and uniform final doping. Representative values are 30 minutes and 980 C. Under these conditions, the author has found that the current gain, or h_{FE} values are hardly affected, whereas the storage time after turn off of the transistor is reduced by a factor of 5 to 10. The differential effect of gold on σ_{no} and σ_{po} is observed in an even more striking way if pnp transistors of equivalent design are doped with gold under the same conditions. Here the current gain values depend on hole lifetime and drop to less than one hundredth of their original values. Clearly in the pnp case, another impurity of effect opposite to gold remains to be found.

Read and Understood_____
R. N. Noyce
January 20, 1959

Date _____ NPN FT ~~4100~~ 4205 EVALUATION SHEET Lot _____ Batch _____ Rack _____

Operator _____ Sheet _____ of _____

I_C	10μa	100μa		150ma	150ma	150ma			0ma	0ma	50ma	10ma	100ma	150ma	150ma	
I_B			100μa		15ma	15ma			0ma	0ma				15ma	15/5ma	
V_C				10v			60 v	60 v	10v	0.5v	10v	10v				
							~~25°C~~ 30°	150°C					R_B=10Ω	R_L=40	R_L=40	
#	BVCEO	BVCBO	BVEBO	IB	VCE(S)	VBE(S)	ICBO μa	ICBO μa	Cob	CTe	hfe	rbCc	LVCER	t(d+r)	t(s+f)	
1	108	108	8.5	4.5	1.24	1.05	.00056	.70	11			255	125			
2	102	104	8.1	6.2	1.73	1.08	.00						115			
3	115	120	8.6	5.4	1.19	1.05	.00						145			
4	138	145	9.7	3.9	2.40	1.00	.00						145			
~~5~~	108	110	8.3	5.4	1.58	1.07	.00						98			
6	113	147	9.4	3.8	1.26	.94	.00						148